2116B COMPUTER

HEWLETT · PACKARD

VOLUME 2

INSTALLATION AND MAINTENANCE

HEWLETT hp PACKARD

2116B

VOLUME TWO

INSTALLATION AND MAINTENANCE MANUAL

UPDATING SUPPLEMENT

16 NOV 1970

MANUAL IDENTIFICATION

Manual Serial No. Prefix: 944-

Manual Printed: OCT 1970

Manual Part Number: 02116-9153

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Serial No. Prefix	Change
ALL	1 thru 9
959-	10
977-	11

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes
A300	Power Supply Assembly	02116-6124	–	10,11

Changes 1 through 11 dated 16 November 1970.

11000 Wolfe Road, Cupertino, California 95014, Tel. (408) 257-7000, TWX 910-338-0221

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CHANGE	DESCRIPTION
1	Page 1-12, figure 1-9. At the "PIN INDICATION" columns for the 86-pin connector, swap the "FOIL SIDE" and "COMPONENT SIDE" column titles.
2	Page 4-8, table 4-3. In the "PROGRAM PROCEDURE PART NO." column, change "02116-91764" to read "02116-91792", change "02116-91765" to read "02116-91792", change "02116-91766" to read 02116-91793", and change "02116-91767" to read "02116-91793".
3	Page 4-49, figure 4-4. Add pin 58 where signal $\overline{RF2}$ leaves timing generator card A106.
4	Page 4-85, figure 4-21. Change signal designation CF2 to $\overline{CF2}$.
5	Page 4-88, figure 4-26. Change signal designation CF1 to $\overline{CF1}$.
6	Page 4-125, 4-129, 4-133, and 4-137, figures 4-49, 4-51, 4-53, and 4-55, respectively. Change the designation of the signal leaving A108-8 and entering A20-70 from $\overline{SLM}$ to $\overline{SLME}$.
7	Pages 4-127, 4-131, and 4-135, figures 4-50, 4-52, and 4-54, respectively. Change the designation of the signal leaving A108-32 and entering A20-76 from $\overline{SRM}$ to $\overline{SRME}$.
8	Page 4-134, paragraph 4-307, line 7. Change signal designation $S\overline{RM}$ to $\overline{SRM}$.
9	Page 4-182, paragraph 4-446, line 1. Change instruction designation CL$\hat{O}$ to CLO.
10	Make the following changes to the manual for computers having serial number 959–.

a. Updating pages 5-88A and 5-88B of this supplement. Detach and insert these pages immediately following page 5-88 of the manual.

b. Updating pages 5-90A/5-90B and 5-90C/5-90D of this supplement. Detach and insert these pages immediately following page 5-90 of the manual.

c. Updating page 5-91A of this supplement. Detach and insert this page immediately following page 5-91 of the manual.

d. Page 6-36, table 6-12. Change figure reference "6-12" in the "FIG. & INDEX NO." column to read "6-12A-". Add "11; 0490-0892; Relay; 2.25K ohm coil, 10A, 120VAC, (K2); 28480; 0490-0892; 1" in the applicable columns of the table.

e. Updating page 6-37A of this supplement. Detach and insert this page immediately following page 6-37 of the manual.

f. Updating pages 6-38A and 6-38B of this supplement. Detach and insert these pages following page 6-38 of the manual.

g. Page 6-49, table 6-19. Add "0490-0892; Relay, 2.25K ohm coil; 28480; 0490-0892; 1" and "0811-2735; Resistor, Fxd, WW, 2500 ohms, 3%, 10W; 28480; 0811-2735; 1" in the applicable columns of the table.

h. Manual title page. Change the referenced serial number prefix to 959–.

CHANGE	DESCRIPTION
11	Make the following changes to the manual for computers having serial number prefix 977-.

a. Page 5-73, table 5-23 and figure 5-32. At reference designation R83 of table 5-23, change the entry to read "R83; 0757-0198; Resistor, Fxd, Met Flm, 100 ohms, 1%, 1/2W; 28480; 0757-0198". In figure 5-32, change the revision code from "683" to "1025".

b. Updating pages 5-88A and 5-88B of this supplement. Detach and insert these pages immediately following page 5-88 of the manual.

c. Updating pages 5-90A/5-90B, 5-90C/5-90D, and 5-90E/5-90F of this supplement. Detach and insert these pages immediately following page 5-90 of the manual.

d. Updating pages 5-91A and 5-91B of this supplement. Detach and insert these pages immediately following page 5-91 of the manual.

e. Page 6-26, table 6-8. At index number 15, change the entry to read "15; 0757-0198; Resistor, Fxd, Met Flm, 100 ohms, 1%, 1/2W, (R83); 28480; 0757-0198; 1."

f. Page 6-28, figure 6-8. Change the revision code from "638" to "1025".

g. Page 6-36, table 6-12. Change figure reference "6-12" in the "FIG. & INDEX NO." column to read "6-12A-". Add "11; 0490-0892; Relay, 2.25K ohm coil, 10A, 120VAC, (K2); 28480; 0490-0892; 1" in the applicable columns of the table.

h. Updating page 6-37A of this supplement. Detach and insert this page immediately following page 6-37 of the manual.

i. Updating page 6-38A and 6-38B of this supplement. Detach and insert these pages immediately following page 6-38 of the manual.

j. Page 6-49, table 6-19. Make the following changes in the applicable columns of the table:

   (1) Add "0490-0892; Relay, 2.25K ohm coil; 28480; 0490-0892; 1."

   (2) For HP part no. 0686-2215, change the TQ from "2" to "1".

   (3) Add "0757-0198; Resistor, Fxd, Met Flm, 100 ohms, 1%, 1/2W; 28480; 0757-0198; 1".

   (4) Add "0811-2735; Resistor, Fxd, WW, 2500 ohms, 3%, 10W, 28480; 0811-2735; 1".

k. Manual title page. Change the referenced serial number prefix to 977-.

VOLUME TWO

INSTALLATION AND MAINTENANCE MANUAL

MODEL 2116B COMPUTER

Serial Numbers Prefixed: 944-

Note

This manual applies directly to the Hewlett-Packard Model 2116B Computers having serial number prefix 944-. Manual changes or corrections affecting this and future prefix numbers will be documented in updating supplements.

To order additional copies of this manual, specify part number 02116-9153.

02116-9153

11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

Printed: OCT 1970

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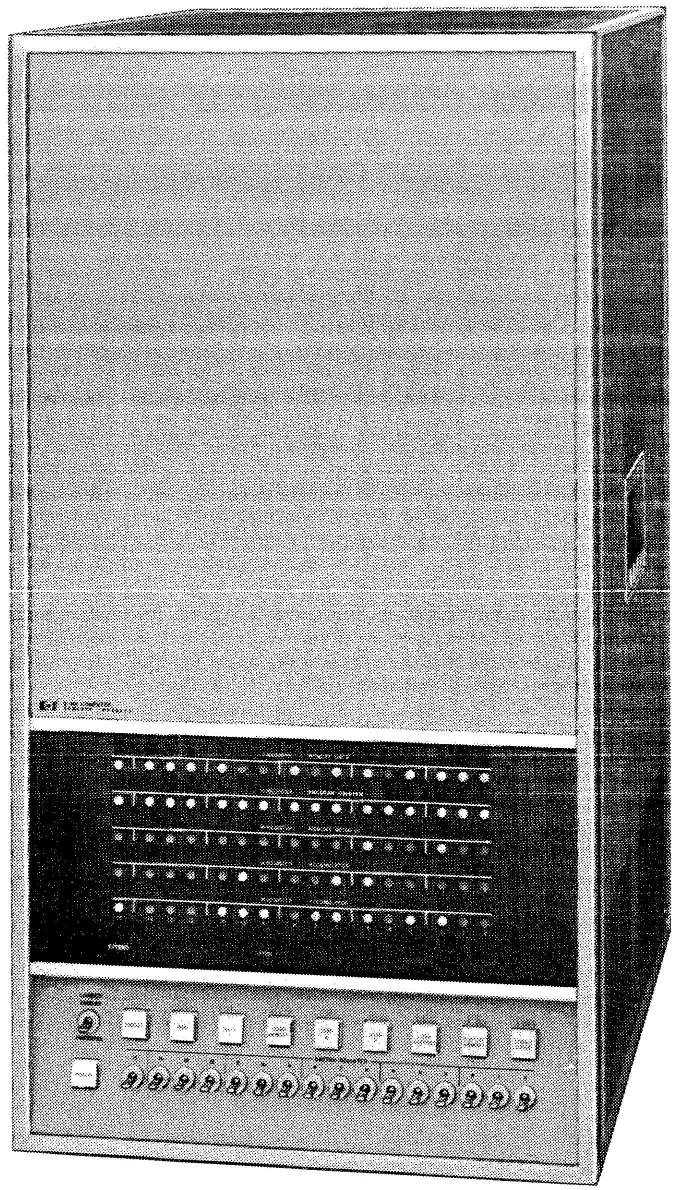

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Figure 1-1. Hewlett-Packard Model 2116B Computer

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. Volume Two is the second in a series of three volumes that document the Hewlett-Packard Model 2116B Computer (figure 1-1). Volume Two contains detailed descriptions, instructions, and diagrams for installation, maintenance, troubleshooting, and repair of the computer. Unless otherwise stated in this manual or in future supplements, Volume Two is applicable to 2116B Computers having serial-number prefix 944- and higher.

1-3. Volume Two is a reference work intended for users who are familiar with the circuit theory and maintenance procedures of the 2116B or similar computers in the Hewlett-Packard line. Also, a thorough understanding of the information presented in Volume One, Specifications and Basic Operation Manual for the Model HP 2116B Computer, is essential to using and understanding the material presented in this volume.

1-4. This volume has two purposes. First, it provides general information, installation instructions, and overall maintenance data for the computer. Second, it provides testing, troubleshooting, and repair instructions for four major functional sections of the computer. These sections are the control, arithmetic, memory, and power supply sections (see figure 1-2). The I/O section is documented separately in Volume Three, Input/Output System Operation Manual for the Model 2116B Computer. Computer optional features are documented in separate manuals and supplements.

1-5. The sections and appendices of Volume Two contain the following information:

a. Section I, General Information. Section I contains information for users who require a knowledge of the physical makeup of the computer and an understanding of its maintenance features. Included are a description of the various electronic assemblies that comprise the computer, an explanation of controls and indicators, a description of identification numbers used in the computer, a description of standard accessory equipment supplied with the computer, an explanation of the principal built-in maintenance features, and a list of recommended servicing equipment.

b. Section II, Installation. Section II describes unpacking procedures, provides primary power data, explains initial inspection procedures, and presents other information required for installing the computer.

c. Section III, Theory of Operation. Section III describes the circuit theory of the control, arithmetic, memory, and power supply sections.

d. Section IV, Troubleshooting. Section IV presents step-by-step procedures for testing the computer. The results of these tests form the basis of fault-localizing procedures, which use servicing diagrams presented in the section. These diagrams, together with logic equations and timing charts, aid in the rapid isolation of computer faults.

e. Section V, Maintenance. Section V provides preventive-maintenance instructions and adjustment information. Also included are schematic diagrams, parts location diagrams, wiring data, and other data required for testing, troubleshooting, maintenance, and repair.

f. Section VI, Replaceable Parts. Section VI contains lists of replaceable parts. These lists give the name of each part, and specify the characteristics of electronic components. The parts lists also give manufacturers' names, manufacturers' part numbers, and the total quantity of each part installed in the computer. The parts lists and total-quantity figures apply to the basic computer configuration.

g. Appendix A, Basic Logic Symbols. Appendix A describes the logic symbols used in this manual. The explanations also apply to logic symbols in manuals for optional devices, provided the manuals were written by Hewlett-Packard. Also furnished in Appendix A are diagrams and other data for the integrated circuits used in the computer. For data on integrated circuits in optional devices, refer to the manual for the device concerned.

h. Appendix B, Backdating Information. Appendix B provides backdating information, making Volume Two applicable to computers with serial-number prefixes lower than 944-.

i. Updating Supplements. If required, updating supplements are included with Volume Two. These make Volume Two applicable to computers with serial-number prefixes higher than 944-.

1-6. GENERAL DESCRIPTION.

1-7. COMPUTER ASSEMBLIES.

1-8. The major assemblies that make up the computer are listed in table 1-1 and shown in figures 1-3, 1-4, and 1-5. The following paragraphs describe these assemblies.

1-9. CIRCUIT CARDS. As the term is used with the 2116B Computer, a circuit card is an assembly consisting of electronic components mounted on an insulating card. An

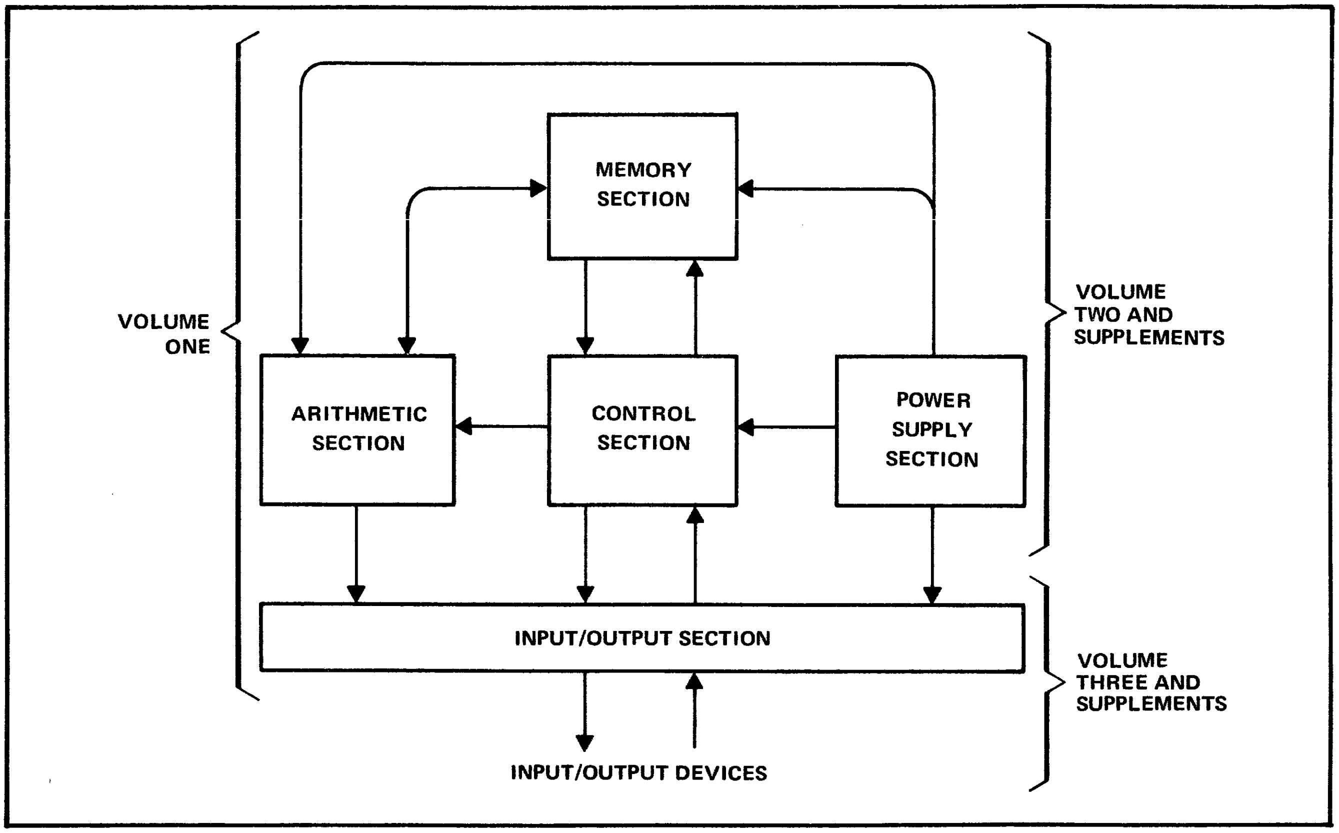

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Figure 1-2. Major Functional Sections of the 2116B Computer

etched-foil pattern on the card makes connections between the components. The entire unit, referred to as a card, plugs into a connector in the computer. A similar unit which is permanently wired to other assemblies, is referred to as a board.

1-10. The computer logic circuits are made up entirely of card assemblies, which plug into fixed connectors in the card cage. In some cases a second connector, on the end of a flexible cable, fits on the front end of the card. Each card assembly is assigned a reference designation beginning with the letter "A", to which is added a number indicating tne card-cage slot in which the card is installed. Each card also has a part number. If more than one card of a given type is used, each of the cards has the same part number but a different reference designation.

1-11. Cards with reference designations A1 through A22 contain principally the memory-section circuits, and the cards are installed in the top row of card slots in the card cage. Cards A101 through A120, containing principally the control-section and arithmetic-section circuits, are situated in the center row of card-cage slots. Cards A201 through A222, containing principally I/O-section circuits, are installed in the bottom row of slots.

1-12. The cards shown in figure 1-3 are those used for the basic computer configuration. For optional features, additional cards may be installed in the card cage.

1-13. Two more cards, part of the basic computer configuration, are part of the power supply section and are situated in the power supply at the back of the computer cabinet.

1-14. DISPLAY BOARD ASSEMBLY. The display board assembly, reference designation A501, provides a visual indication of computer operating conditions, and displays the contents of the principal computer registers. The unit mounts in the computer door assembly, as shown in figures 1-3 and 1-1. Connection to the display board assembly is made by the display cables (figure 1-3), which plug onto the front ends of arithmetic-section and control-section cards in the card cage. An additional cable, referred to as the strip cable, connects the display board assembly with the power supply section. On the back of the display board are three switches, used for troubleshooting purposes, and two spare lamps.

1-15. CONTROL PANEL ASSEMBLY. The control panel assembly, reference designation A502, mounts the operator's controls. The unit is situated immediately beneath the display board assembly, as shown in figures 1-3 and 1-1. The controls on the panel are principally of the push-switch type, some with internal indicating lamps. Connection to the control panel assembly is made by the control cable (figure 1-3), which plugs onto the front end of front panel coupler card A101. Additional connections are made by wires in tne strip cable, which connect with the power supply section and with power fail interrupt card A1 in the card cage.

Table 1-1. Major Electronic Assemblies, Basic Computer Configuration

DESIGNATION	PART NO.	QTY	NOMENCLATURE
A1	02116-6175	1	Power fail interrupt card
A2	02116-6300	1	Memory module decoder card
A12,A13	02116-6298	2	Sense amplifier card
A14,A15	02116-6266	2	Driver/switch card
A16,A18	02116-6265	2	Inhibit driver card
A20	02116-6069	1	Direct memory logic card
A101	02116-6208	1	Front panel coupler card
A102,A103,A104,A105	02116-6026	4	Arithmetic logic card
A106	02116-6281	1	Timing generator card
A107	02116-6027	1	Instruction decoder card
A108	02116-6029	1	Shift logic card
A121	02116-6284	1	Overvoltage protection assembly
A201	02116-6041	1	I/O control card
A202	02116-6194	1	I/O address card
A301	02116-6014	1	Logic supply regulator card
A302	02116-6015	1	Memory supply regulator card
A303	-	1	Capacitor board assembly
A304	-	1	Large heat sink assembly
A305	-	1	Small heat sink assembly
A306	-	1	Component board assembly
A307	-	1	Component board assembly
A308	-	1	Component board assembly
A309	-	1	Component board assembly
A310	-	1	Component board assembly
A311	-	1	Transformer assembly
A312	-	1	AC input section
A400	02116-6288	1	Core stack assembly
A402	02116-0096	1	Temperature sensing assembly
A501	02116-6043	1	Display board assembly
A502	02116-0005	1	Control panel assembly
NOTE: Assemblies for optional features are not listed in this table.			

1-16. POWER SUPPLY ASSEMBLY. The power supply assembly, reference designation A300, is at the rear of the computer cabinet (figure 1-4). Access to this part of the computer is gained by removing the card cage retaining screws, sliding out the card cage, and swinging the cage open. When sliding the card cage back into the cabinet, it is necessary to first squeeze together the two tab catches.

1-17. The power supply, made up of 12 subassemblies, provides the regulated and unregulated dc voltages required by the computer. The power supply also provides regulated dc voltages for plug-in cards in the card cage which are associated with optional devices. All optional units external to the computer cabinet furnish their own ac and dc voltages, derived from a separate connection to the ac power line.

1-18. CORE STACK ASSEMBLY. The core stack assembly, reference designation A400, is at the rear of the card cage (figure 1-5). The unit provides the computer with its core storage capability. The associated temperature sensing assembly, reference designation A402, controls the level of certain operating voltages (+32 and +22 volts) in accordance with the air temperature near the stack.

1-19. BACKPLANE CONNECTORS. The backplane connectors are at the rear of the card cage (figure 1-5). The connectors receive the plug-in cards installed in the card cage, and provide connections to the cards.

1-20. CONTROLS AND INDICATORS.

1-21. The locations of operator's controls and indicators are shown in figures 1-6 and 1-7. The reference designation of each control and indicator, together with a description of the purpose of each, is given in tables 1-2 and 1-3.

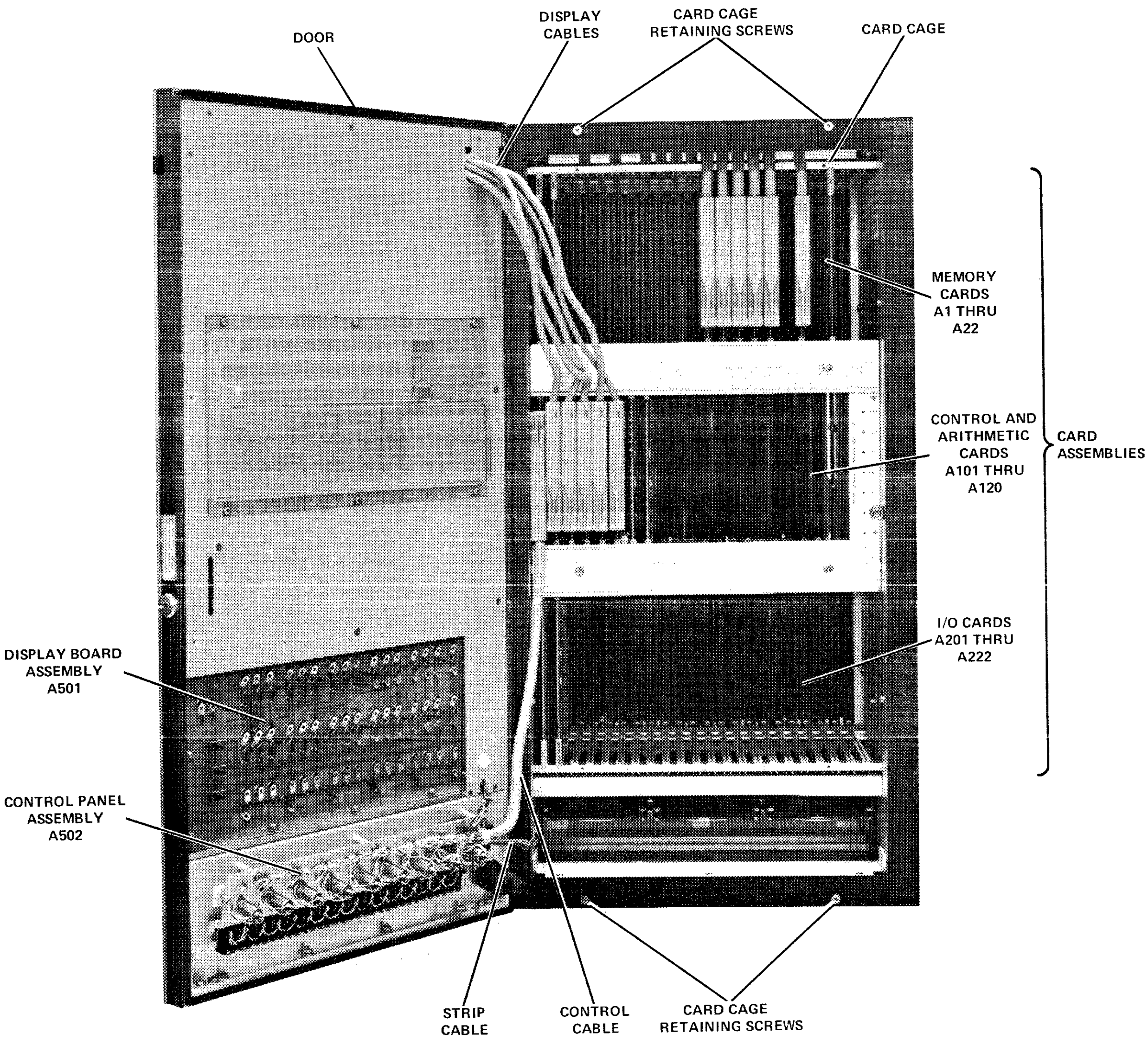

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Figure 1-3. Interior View of Computer, Card Cage Closed

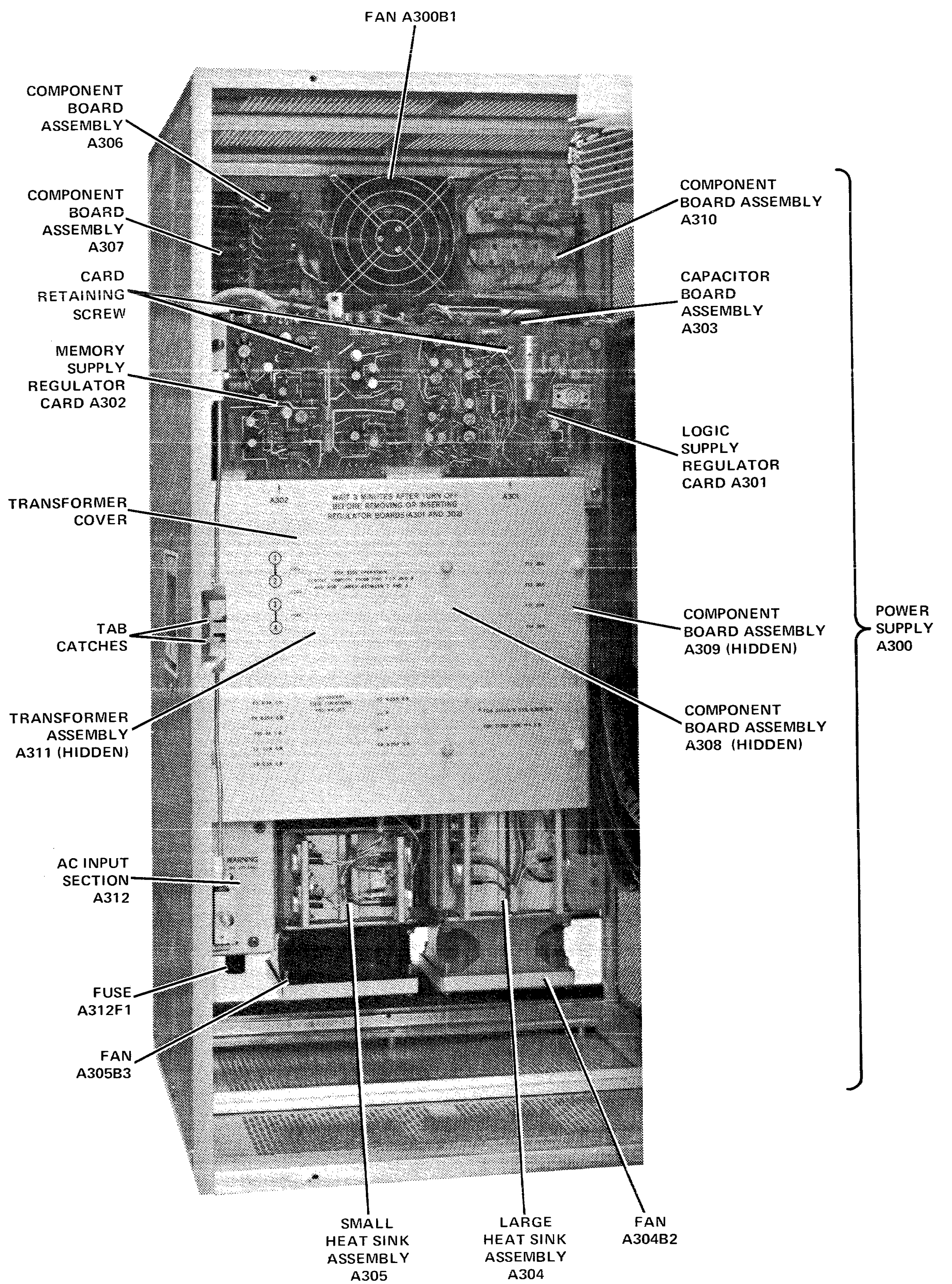

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Figure 1-4. Interior View of Computer, Card Cage Open

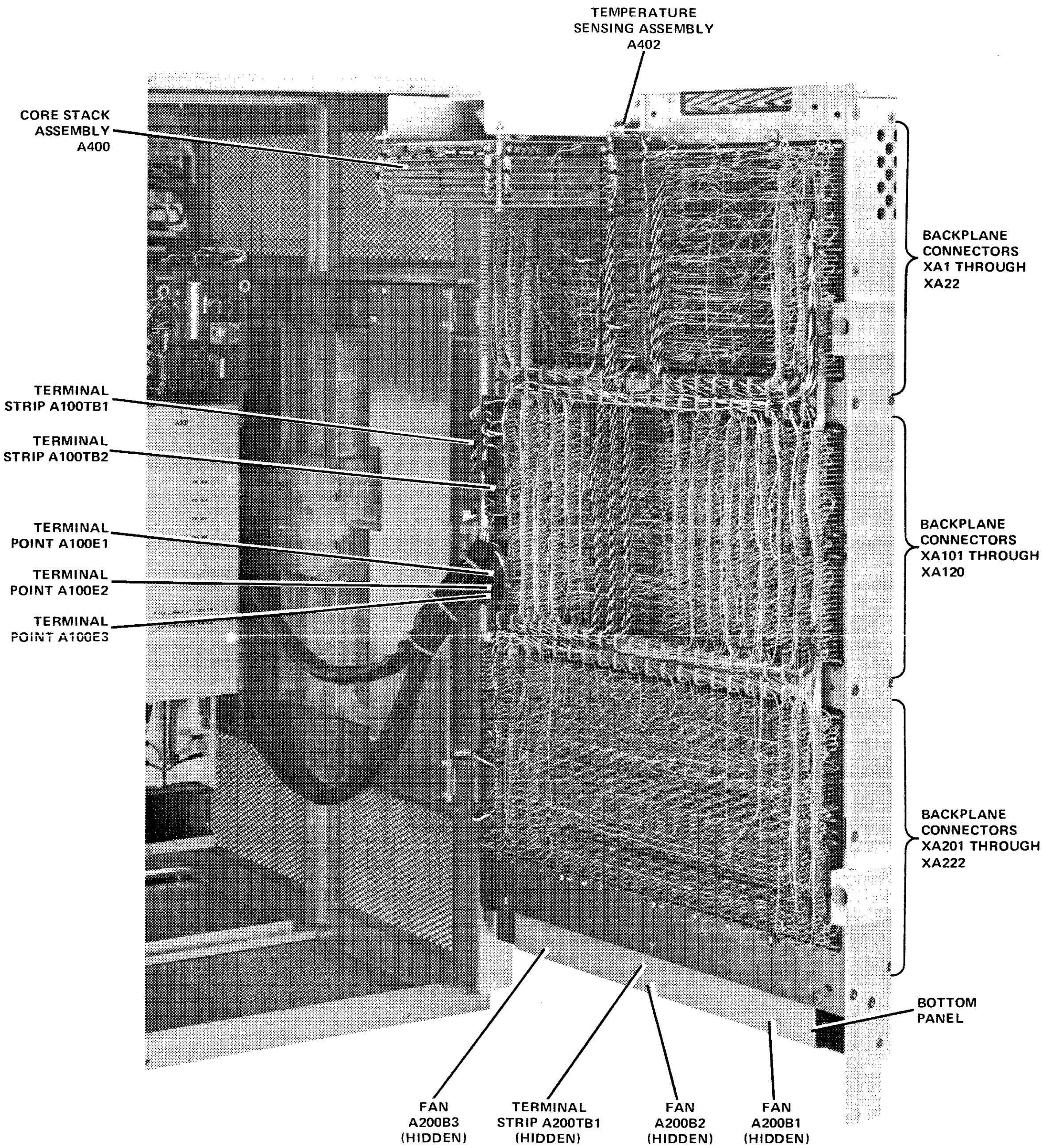

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Figure 1-5. Rear View of Card Cage

Table 1-2. Indicators on Display Board Assembly A501

ILLUSTRATION CALLOUT (FIGURE 1-6)	PANEL MARKING	REFERENCE DESIGNATION	DESCRIPTION	USE
1	T-REGISTER MEMORY DATA	A501DS1 thru A501DS16	Indicator lamps	Displays the contents of the T-register.
2	P-REGISTER PROGRAM COUNTER	A501DS17 thru A501DS32	Indicator lamps	Displays the contents of the P-register.
3	M-REGISTER MEMORY ADDRESS	A501DS33 thru A501DS48	Indicator lamps	Displays the contents of the M-register
4	A-REGISTER ACCUMULATOR	A501DS49 thru A501DS64	Indicator lamps	Displays the contents of the A-register.
5	B-REGISTER ACCUMULATOR	A501DS65 thru A501DS80	Indicator lamps	Displays the contents of the B-register.
6	EXTEND	A501DS86	Indicator lamp	Lights when the Extend FF is set.
7	OVERFLOW	A501DS85	Indicator lamp	Lights when the Overflow FF is set.
8	FETCH	A501DS84	Indicator lamp	Lights when the computer is in the fetch phase.
9	INDIRECT	A501DS83	Indicator lamp	Lights when the computer is in the indirect phase.
10	EXECUTE	A501DS82	Indicator lamp	Lights when the computer is in the execute phase.
11	PARITY HALT	A501DS81	Indicator lamp	Used by an optional feature. Refer to Memory Parity Check Operating and Service Manual (part no. 12591-9001).

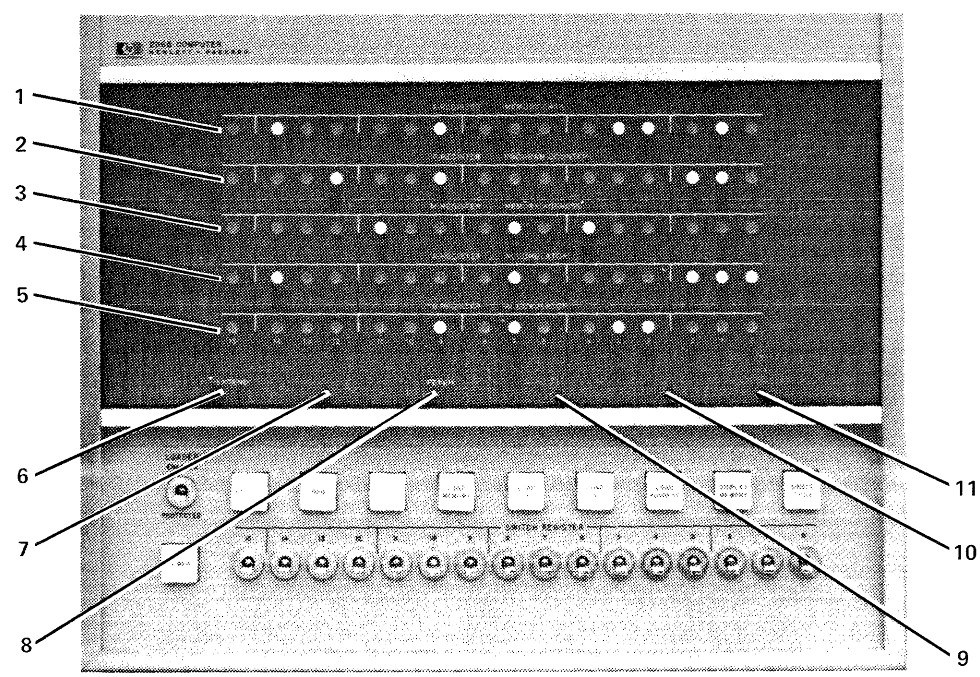

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Figure 1-6. Display Board Assembly A501, Indicators

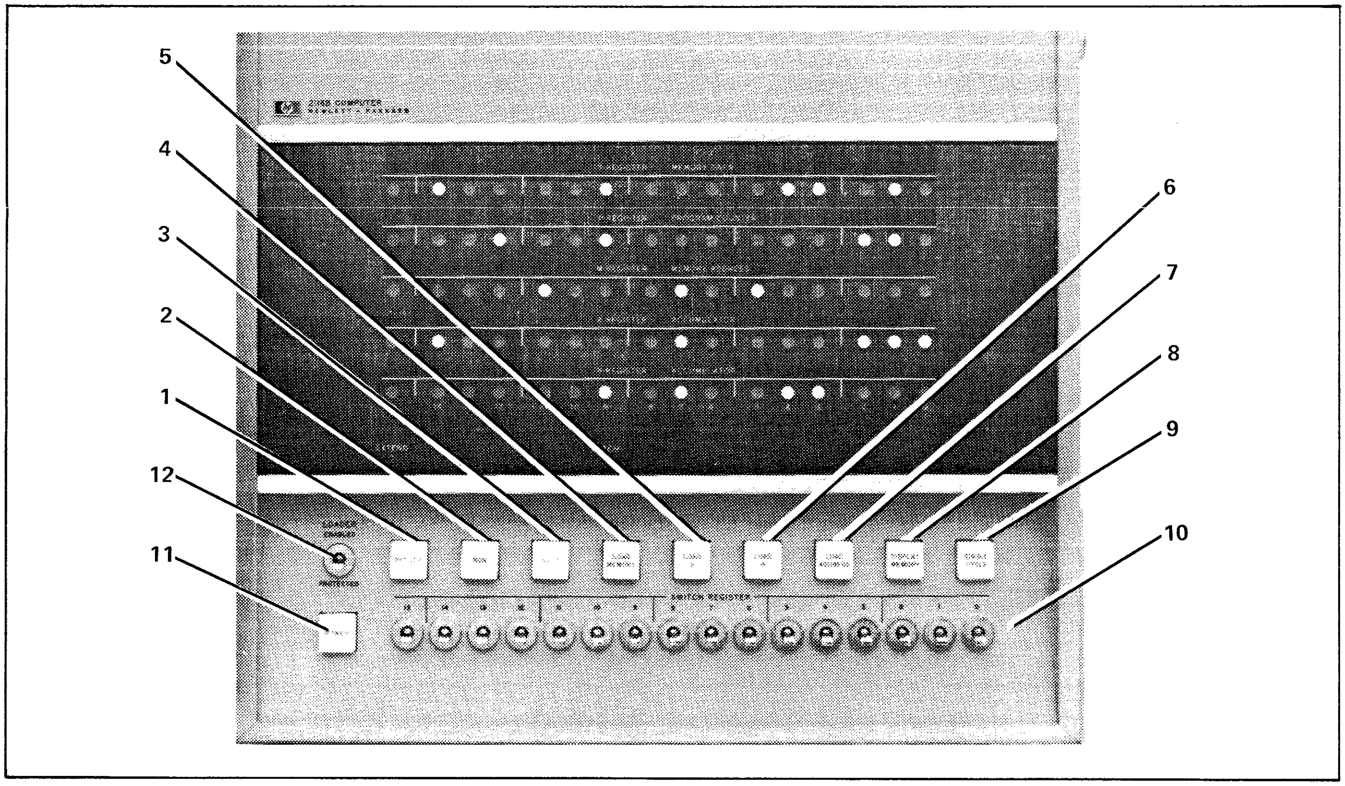

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Figure 1-7. Control Panel Assembly A502, Controls and Indicators

Table 1-3. Controls and Indicators, Control Panel Assembly A502

ILLUSTRATION CALLOUT (FIGURE 1-7)	PANEL MARKING	REFERENCE DESIGNATION	DESCRIPTION	USE
1	PRESET	A502S108 and A502DS108	Lighted push-switch (momentary action)*	When pressed, the switch places the computer in the fetch phase. It also resets the entire I/O system and the power-fail interrupt system by: a. Clearing the Interrupt Control FF on I/O Control Card A201. b. Clearing the Flag FF and Control FF on each I/O interface card. c. Setting the Flag Buffer FF (if any) and the Flag FF on each I/O interface card. d. Clearing the Flag Buffer FF, Flag FF, and IRQ FF on Power Fail Interrupt Card A1.

Table 1-3. Controls and Indicators, Control Panel Assembly A502 (Cont)

ILLUSTRATION CALLOUT (FIGURE 1-7)	PANEL MARKING	REFERENCE DESIGNATION	DESCRIPTION	USE
				The indicator lights when a power-fail interrupt occurs as a result of low line-voltage applied to the computer, or as a result of low line-voltage applied to the 2150B I/O and Memory Extender (if used). The indicator also lights in the event of overheating in any of the following: a. Memory module decoder card A2. b. Large heat sink assembly A304. c. Small heat sink assembly A305. d. 2160A Power Supply Extender (if used). e. 2150B I/O and Memory Extender (if used). The indicator also lights when power is initially applied to the computer. After being lighted for any reason, the indicator remains lighted until the PRESET switch is pressed. The lamp immediately relights if an undervoltage or overheating condition continues.
2	RUN	A502S107 and A502DS107	Lighted push-switch (momentary action)*	When pressed, starts the program in the phase (fetch, indirect, or execute) indicated on display panel A501. The address of the instruction performed (or continued) is displayed in the P-register before the push-switch is pressed. While the program is running, the RUN indicator is lighted.
3	HALT	A502S106 and A502DS106	Lighted push-switch (momentary action)	When pressed, stops the program at the end of the current phase. The HALT indicator is lighted when the program is not running.
4	LOAD MEMORY	A502S105	Push-switch (momentary action)*	When pressed, stores the contents of the SWITCH REGISTER switches (S-register) in the core storage location specified by the M-register. Then increments the P-register by 1, sets the contents of the M-register equal to the contents of the P-register, and leaves the computer in fetch phase.

Table 1-3. Controls and Indicators, Control Panel Assembly A502 (Cont)

ILLUSTRATION CALLOUT (FIGURE 1-7)	PANEL MARKING	REFERENCE DESIGNATION	DESCRIPTION	USE
5	LOAD A	A502S104	Push-switch (momentary action)*	When pressed, loads the contents of the S-register into the A-register.
6	LOAD B	A502S103	Push-switch (momentary action)*	When pressed, loads the contents of the S-register into the B-register.
7	LOAD ADDRESS	A502S102	Push-switch (momentary action)*	When pressed, loads the contents of the S-register into the M-register and P-register, and leaves the computer in fetch phase.
8	DISPLAY MEMORY	A502S101	Push-switch (momentary action)*	When pressed, displays in the T-register the contents of the core storage location specified by the M-register. Then advances the P-register by 1, sets the contents of the M-register equal to the contents of the P-register, and leaves the computer in fetch phase.
9	SINGLE CYCLE	A502S100	Push-switch (momentary action)*	When this switch is pressed, the computer performs one machine cycle in the phase indicated on display panel A501. The address of the instruction performed is 1 less than the number displayed in the P-register.
10	SWITCH REGISTER	A502S0 through A502S15	Toggle switches	Provides the means for manually entering data, addresses, or instructions into the computer. The low-order bit is SWITCH REGISTER switch 0. A switch is set to the up position for logic 1, to the down position for logic 0. After a number is entered, one of the following push-switches is pressed: a. LOAD ADDRESS. b. DISPLAY MEMORY. c. LOAD MEMORY. d. LOAD A. e. LOAD B.
11	POWER	A502S109 and A502DS109	Lighted push-switch (push-on, push-off)	The switch turns the computer on or off. The indicator is lighted when the computer is on, extinguished when the computer is off.
12	LOADER	A502S110	Toggle switch	In the ENABLED position, allows the program to reference the protected area in memory where the binary loader program is stored.

*Inoperative when a program is running.

1-22. IDENTIFICATION.

1-23. COMPUTER SERIAL NUMBER.

1-24. The computer is identified by an 8-digit (000—00000) serial number marked on the rear of the computer (see figure 1-8). The first three digits are a serial-number prefix used to indicate design changes. If the serial-number prefix on the computer does not agree with the prefix number on the title page of this manual, look for manual-change information in Appendix B of this volume or in a supplement accompanying this volume.

1-25. COMPUTER MODEL NUMBER.

1-26. The computer model number (2116B) is marked beneath the serial number on the back of the computer. The model number is also marked on the front door of the computer.

1-27. OPTION NUMBERS.

1-28. On the rear of the computer, beneath the model number, is marked the identifying number of each factory-installed optional feature. When optional features are supplied for installation in the field, the installation instructions require that the appropriate option number be marked in the same place as for a factory-installed option.

1-29. To determine the meaning of option numbers, refer to a Hewlett-Packard sales catalog, or request the nearest Hewlett-Packard Sales and Service office to furnish a list of optional features for the 2116B. (Sales and Service Offices are listed in the back of this manual.)

1-30. ASSEMBLY PART-NUMBERS.

1-31. The majority of the electronic assemblies in the computer are plug-in circuit cards. A typical card, of the type installed in the card cage, is shown in figure 1-9. In the illustration, the part number is in the upper left corner of the card. Also shown in the illustration are the identifying numbers and letters of the card pins, and the means used for identifying integrated circuits (microcircuits) mounted on the card.

1-32. Assemblies other than circuit cards usually are not marked with their part number. Part numbers for these assemblies are found in section VI of this volume, where all electronic assemblies are identified by their location in the computer and their appearance.

1-33. CIRCUIT-CARD REVISION CODES.

1-34. Marked beneath the part number on each circuit card is a revision code (see figure 1-9). The first character of the code is a letter which identifies the etched-foil pattern on the card. The next three digits, referred to as a date code, identify the electrical characteristics of the card with components mounted. The date code is followed by a 1- or 2-digit number which identifies the Hewlett-Packard division which manufactured the assembly.

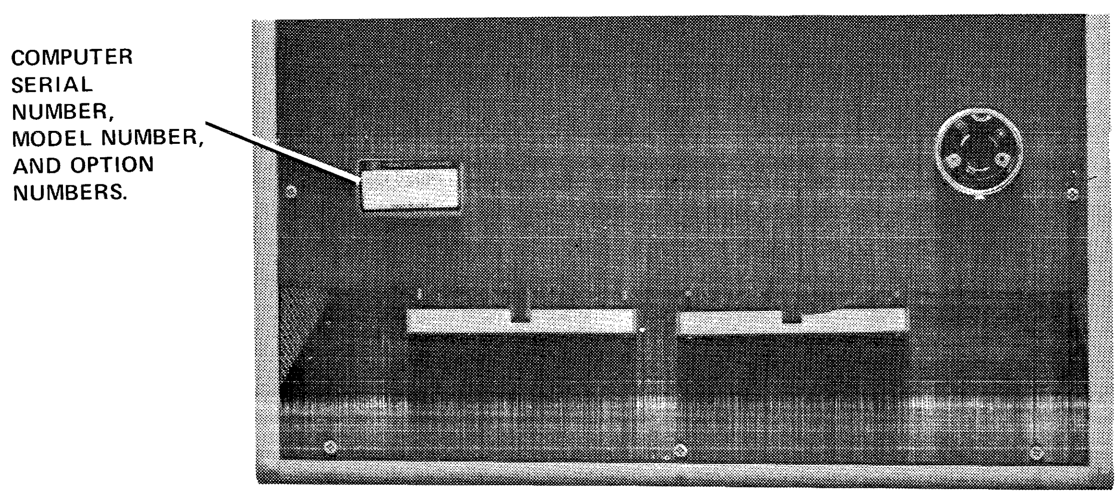

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Figure 1-8. Rear View of Computer, Showing Identifying Numbers

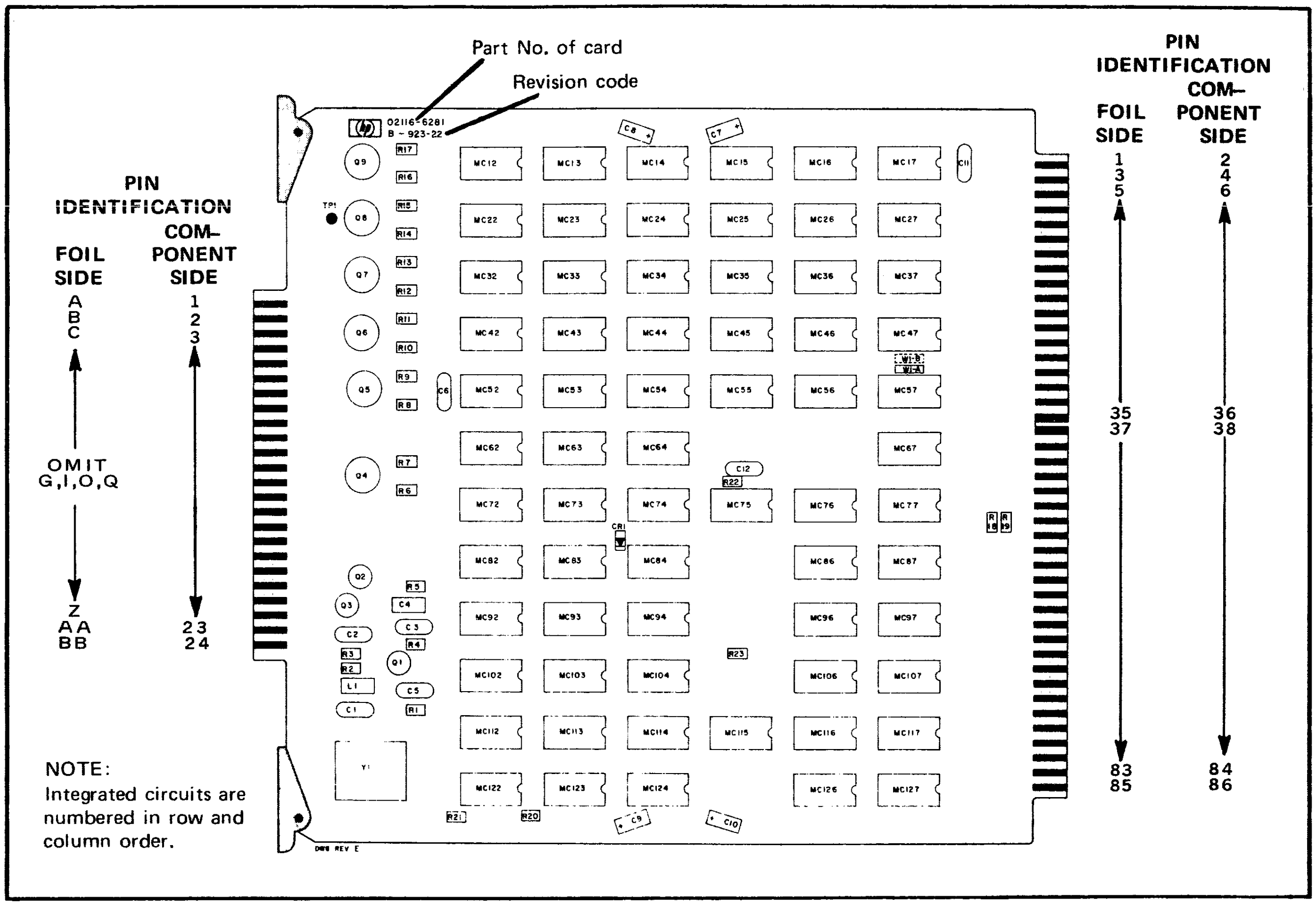

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Figure 1-9. Typical Card-Cage Circuit Card

1-35. DOCUMENTATION OF EQUIPMENT IMPROVEMENTS.

1-36. When factory changes are made in the design and construction of the computer, manuals issued with the computer cover the changes by means of an updating supplement.

1-37. The factory may request that changes be made to the computer after it is in the field. When instructions are issued for making such a change, updating supplements or change sheets are issued for all manuals affected by the change.

1-38. STANDARD ACCESSORIES.

1-39. Standard accessories for the 2116B Computer consist of a rack mounting kit and an accessory kit (figure 1-10). The accessory kit contains an ac power cable, an extender card, an extender cable, and a paper-tape loading instruction card. The rack mounting kit and accessory kit are furnished with the computer, and need not be ordered separately.

1-40. RACK MOUNTING KIT.

1-41. The rack mounting kit allows the computer to be installed in a standard 19-inch equipment rack.

1-42. AC POWER CABLE.

1-43. The ac power cable is a heavy-duty electrical cable, 10 feet in length, used for supplying 115-volt or 230-volt power to the computer. The cable has a 3-prong male connector, NEMA type 5-15P, for insertion into a NEMA type 5-15R or 5-20R female connector serving as the source of ac power for the computer. If local building codes prohibit use of the NEMA 5-15P connector, it must be replaced with an acceptable type.

1-44. EXTENDER CARD.

1-45. The extender card allows circuit cards in the card cage to be extended for troubleshooting.

1-46. EXTENDER CABLE.

1-47. The extender cable allows cards that have a cable plugged to their 48-pin connector to be used with the extender card.

1-48. TAPE-LOADING INSTRUCTION CARD.

1-49. An instruction sheet, encased in clear plastic, provides information on how to load binary paper tapes into the computer. The computer is shipped with the

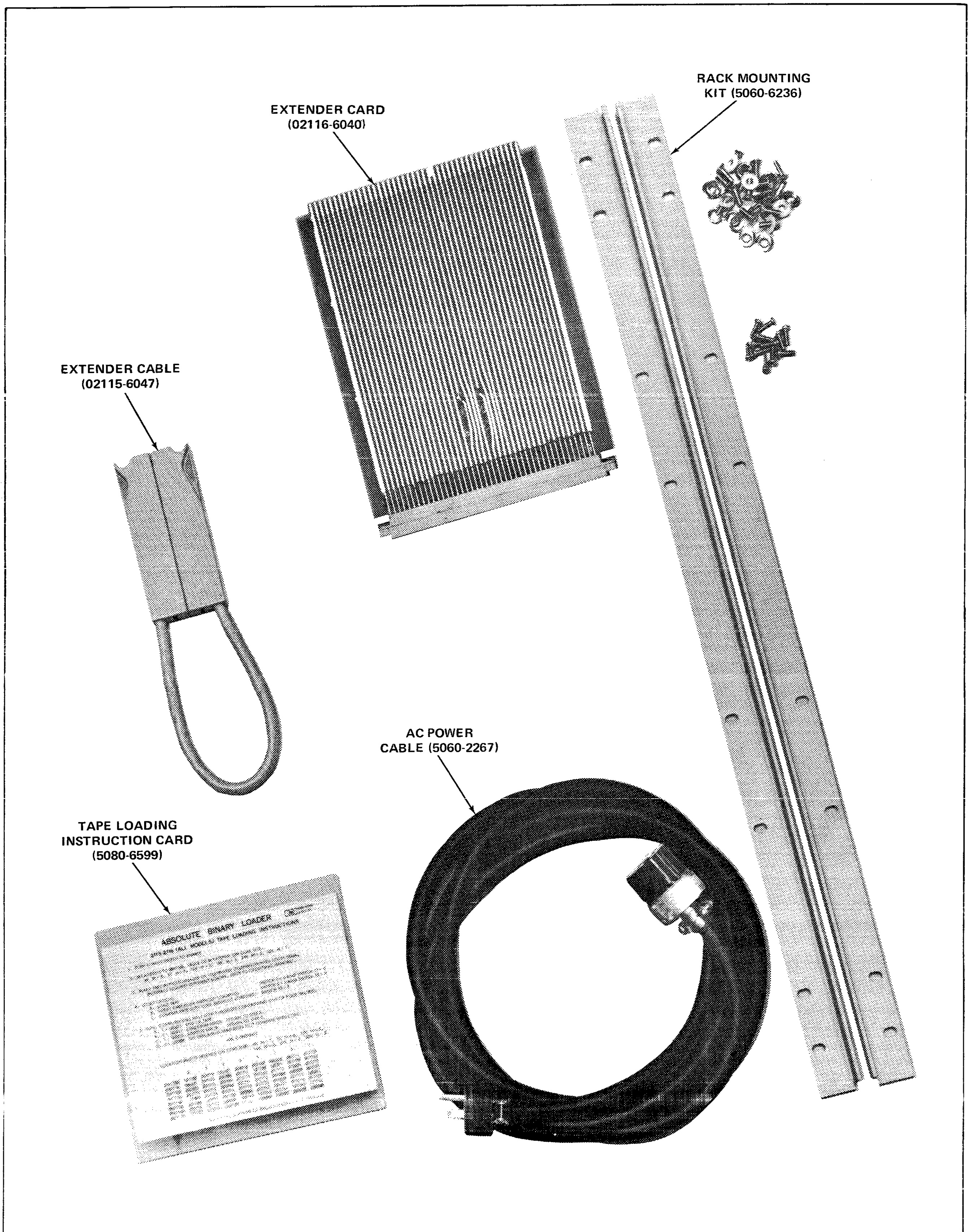

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Figure 1-10. Accessory Kit (02116-6296) and Rack Mounting Kit (5060-6236) required binary-tape loader program stored in core memory. Included on the instruction card is a listing of the loader program, which may be manually reloaded into the computer if the original stored program is destroyed.

1-50. MAINTENANCE.

1-51. PRINCIPAL MAINTENANCE FEATURES.

1-52. Maintenance features for adjusting and servicing the computer are shown in figures 1-11 and 1-12. A brief description of each feature is given in table 1-4.

1-53. MAINTENANCE TOOLS, MATERIALS, AND EQUIPMENT.

1-54. TOOLS. A standard electronics tool kit will provide the tools required for normal servicing of the computer. The kit must include a soldering iron designed for removing and installing 14-pin integrated circuits, and a rubber bulb with a suction tube for withdrawing molten solder. Also required is a torque wrench, capable of indicating 15 inch-pounds, with 3/8-inch, 7/16-inch, and 9/16-inch sockets.

Table 1-4. Computer Maintenance Features

ILLUSTRATION AND CALLOUT NUMBER	PANEL MARKING	REFERENCE DESIGNATION	DESCRIPTION	USE
Fig. 1-11 (1,10)	-	-	Card retainer	Keeps circuit cards in place.
Fig. 2-11	⏚	A121TP1	Test jack	Ground-return test point.
	+32	A121TP2	Test jack	+32 volt supply test point.
	+22	A121TP3	Test jack	+22 volt supply test point.
Fig. 1-11 (1, 10)	+12	A121TP4	Test jack	+12 volt supply test point.
Fig. 1-11 (2)	+4.5	A121TP5	Test jack	+4.5 volt supply test point.
Fig. 1-11 (3)	-2	A121TP6	Test jack	-2 volt supply test point.
Fig. 1-11 (4) Fig. 1-11 (5)	-12	A121TP7	Test jack	-12 volt supply test point.
Fig. 1-11 (6)	-22	A121TP8	Test jack	-22 volt supply test point.
Fig. 1-11 (7) Fig. 1-11 (8) Fig. 1-11 (9) Fig. 1-11 (11)	INSTRUCTION	A501S113	Slide switch	Prevents the P-register contents from being changed, thereby causing the same instruction to be executed repeatedly.
Fig. 1-11 (12)	PHASE	A501S112	Slide switch	Causes the computer to remain in the phase existing at the time the switch is set.
Fig. 1-11 (13)	MEMORY	A501S111	Slide switch	Turns memory section off. Makes all memory locations appear as if containing zeroes.
	-	A300J1	Power connector	AC power input to computer.
Fig. 1-12 (1)	-	-	Foam air filter	Filters cooling air.
Fig. 1-12 (2)	-	-	Foam air filter	Filters cooling air.
Fig. 1-12 (3) Fig. 1-12 (4)	-	-	Identification label	Used to identify computer model number and serial number to determine technical-manual effectivity. Optional features installed in the computer are also listed on this label.
Fig. 1-12 (5)	-	A300J2*	Cable connector	Connector for cable to optional power supply extender and/or memory and I/O extender.

*The manual for the 2160A Power Supply Extender refers to this connector on the 2116B as J2.

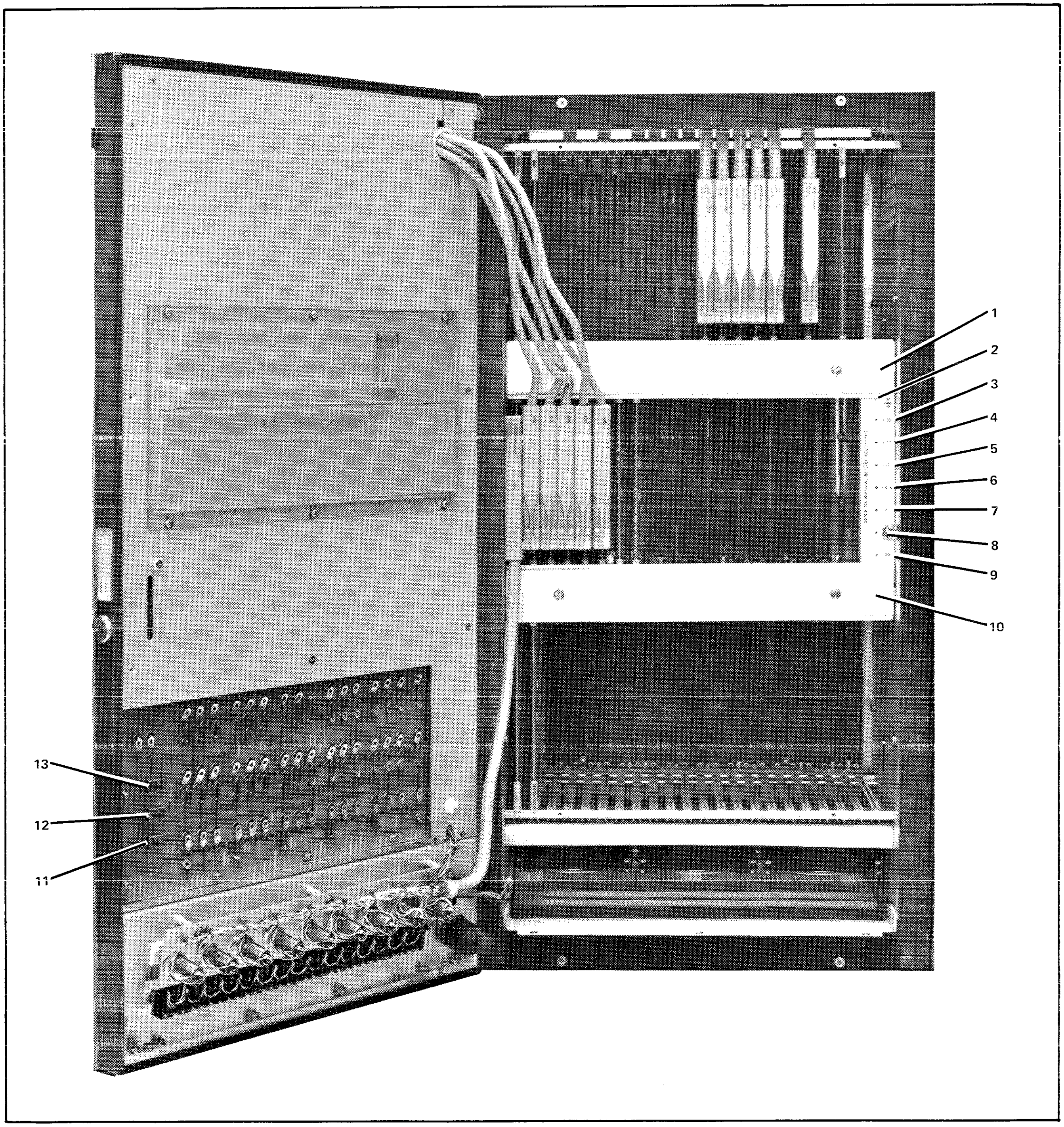

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Figure 1-11. Maintenance Features of Display Board Assembly A501 and Card Cage

1-55. If changes are made to backplane wiring, the following wiring tools are required:

a. A-MP TERMI-POINT Strip-Fed Service Tool, Amp part no. 69525-1.

b. A-MP TERMI-POINT Mandrel for above tool, Amp part no. 69551-1, used with no. 26 wire (American Wire Gauge), 7 strands, wire insulation thickness 0.022 to 0.045 inches, wiring-post size 0.031 x 0.062 inch.

c. A-MP TERMI-POINT Pull Test Tool, Amp part no. 69358-2, 2.25 lbs test force, for 0.031 x 0.062 inch wiring post.

d. A-MP TERMI-POINT Extraction Tool, Amp part no. 69357-3, used for removing Amp 1-330495-5 clip.

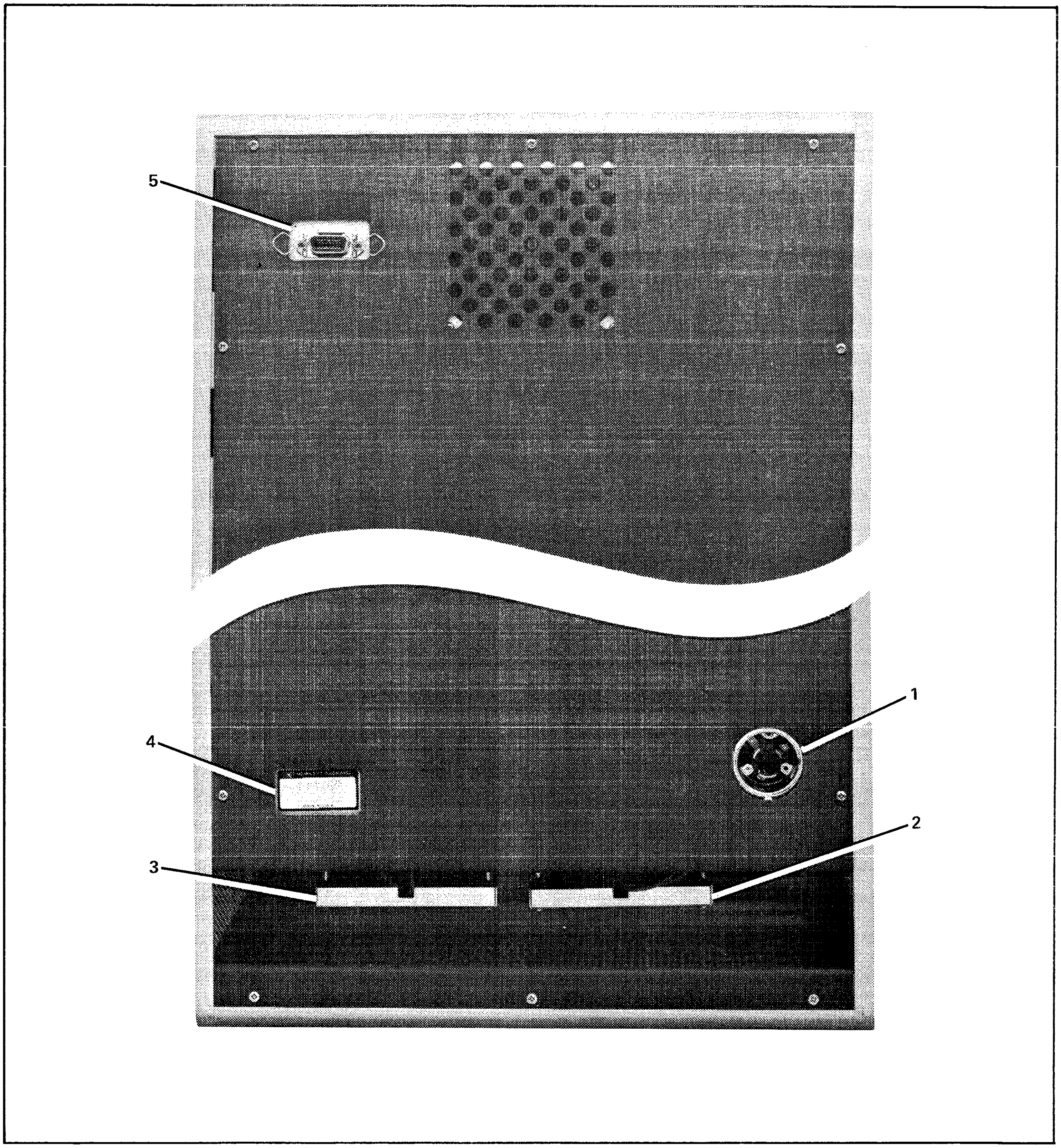

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Figure 1-12. Maintenance Features at Rear of Computer

1-56. In addition to the wiring tools, the following tool is required if a contact in a backplane socket must be replaced: A-MP TERMI-TWIST Contact Replacement Tool, Amp part no. 69514-1, for 0.031 x 0.062 inch wiring post.

1-57. The A-MP tools may be obtained from Amp Incorporated, Harrisburg, Pennsylvania. However, these tools are rarely required and it may be preferable to have backplane wiring work done by Hewlett-Packard service personnel. A list of Hewlett-Packard Sales and Service Offices is furnished at the back of this volume.

1-58. PARTS AND MATERIALS. Spare parts that may be required for the computer are listed in section VI of this volume. Part numbers and ordering information are included.

1-59. Materials and chemicals normally used for electronics service work must be available to the serviceman. These must include heat-conductive silicone compound (Dow-Corning No. 5 Silicon Dielectric Compound, or equivalent).

1-60. SERVICING EQUIPMENT. Equipment recommended for maintenance, troubleshooting, and repair of the computer is listed in table 1-5. Equipment equivalent to that specified may be substituted.

1-61. FIELD OFFICE ASSISTANCE.

1-62. Should servicing assistance be required, contact the nearest Hewlett-Packard Sales and Service Office. These offices are listed at the back of this volume.

Table 1-5. Recommended Test Equipment and Servicing Devices

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED HP MODEL
Dual-trace oscilloscope	Rise time: $\leq$ 10 ns. Vertical deflection: 1 volt/division and 10 volts/division (including attenuator probe). Horizontal sweep speed: 0.1 microseconds/division to 1 second/division.	HP 180A Oscilloscope with 10004A Probe and the following plug-in units: HP 1801A Dual Channel Vertical Amplifier HP 1820A Time Base or HP 1821A Time Base and Delay Generator
Digital voltmeter	At least 4-digit readout. Minimum input resistance: 10 megohms. Full-scale ranges: 9.999 and 99.99V dc.	HP 3439A Digital Voltmeter with HP 3441A Range Selector
AC voltmeter	Expanded-scale or digital-readout type, capable of reading the ac voltage supplied to the computer to ± 1%. Voltage range must be at least 100-115 volts (for a 115-volt computer), or 200-230 volts (for a 230-volt computer).	HP 3445A AC/DC Range Unit. (Also performs functions of HP 3441A Range Selector listed above. Requires HP 3439A Digital Voltmeter.)
Multimeter	Accuracy: ± 3% of full scale. Full-scale ranges: 100 mV to 300V (dc and ac), 10 ohms center-scale to 10 megohms center-scale.	HP 427A
Logic probe	Indication: logic true > +1.4 volts.	HP 10525A
Variable auto-transformer	Capable of reducing computer input line-voltage to 98 volts rms (196 volts for a 230-volt computer), and able to furnish the power required by the computer (1000 to 1600 watts, depending on the optional features installed).	None
Centigrade thermometer	General-purpose type, accurate to ± 1° C.	HP 0440-0004
High-pressure air source	25-50 psi pressure	None
Vacuum cleaner	Must have flexible hose with small nozzle, vacuum port for hose, and pressure port for hose.	None

NOTES:

1. The logic probe is optional. Operating voltage for the probe can be obtained from the +4.5 volt test jack on overvoltage protection assembly A121. Insert a plug into the test jack and connect the probe, using the alligator clip on the adaptor supplied with the probe. Use care not to cause a short.
2. Ambient-temperature and humidity specifications of test equipment must suit the computer environment.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section presents instructions for installing the HP 2116B Computer. Included are procedures for initial inspection, setting up, and making a performance test of the computer. Also described are claims procedures and methods of repacking the computer for shipment.

2-3. INSPECTION OF SHIPMENT.

2-4. The computer and its accessories may be shipped in more than one container. When the shipment is received, check the carrier's papers to ensure that they indicate the same number of containers that has been received.

2-5. If external damage to the shipping carton or cartons is evident, or if a carton is water-stained, ask the carrier's agent to be present when the carton is opened.

2-6. When ready to unpack the shipment, open the carton or cartons, and find the envelope marked "CUSTOMER RECORDS". One of the items in this envelope is a list of the equipment shipped. Check this against the original ordering papers sent to Hewlett-Packard to ensure that all items correspond.

2-7. Unpack the carton or cartons, and examine each item for external damage. Look for such things as broken controls, dented corners, bent panels, and scratches. Also check the rigid foam-plastic cushioning material (if used) for signs of deformation which could indicate rough handling in transit.

2-8. Open the door of the computer, and check for loose parts inside the computer. Remove the card cage retaining screws (shown in figure 1-3), pull out the card cage, and swing it to the right. Examine the interior of the computer for loose parts or other signs of damage. Press upward on the air filters beneath fans A304B2 and A305B3 (figure 1-4) to ensure that the filters are fully seated.

2-9. If the above examination reveals damage to the computer or its accessories, follow the damage-claim procedure described in paragraph 2-43. Retain the shipping containers and packing materials for examination in the settlement of claims, or for future use.

2-10. Upon completing the inspection for damage in transit, proceed with a physical inventory of the material received, as described in the following paragraphs.

2-11. PHYSICAL INVENTORY.

2-12. MANUALS.

2-13. Check the manuals furnished with the shipment to ensure that all manuals listed in the "CUSTOMER RECORDS" envelope have been received.

2-14. EQUIPMENT.

2-15. Check the model number marked on the front door of the computer to ensure that a 2116B has been received.

2-16. Check the model number marked on the back of the computer (figure 1-8) to ensure that a 2116B is indicated. Also check the serial number on the back of the computer and the number given in the "CUSTOMER RECORDS" envelope to ensure that the numbers conform. Compare the list of optional features marked on the back of the computer to be sure that it includes all optional features listed in the "CUSTOMER RECORDS" envelope.

2-17. Insofar as possible, check to ensure that each equipment item listed in the "CUSTOMER RECORDS" envelope has been received. In the case of certain optional features, it may be necessary to refer to the Operating and Service Manual for the optional feature to determine how to identify it. If an option consists of more than one physical unit, make sure that all parts have been received.

2-18. PROGRAM TAPES.

2-19. Check the punched tapes received with the shipment to ensure that all those listed in the "CUSTOMER RECORDS" envelope have been received.

2-20. INSTALLATION PROCEDURE.

2-21. ENVIRONMENTAL REQUIREMENTS.

2-22. The computer must be installed in a location where the ambient temperature is 0° to 55° C (32° to 131° F) when the computer is operating. Relative humidity must be 50 to 95 percent within the temperature range 25° to 40° C; no moisture condensation, water drips, or spray can be permitted. When the computer is turned off, the permissible temperature range is -40° to 75° C (-40° to 167°F).

2-23. To maintain proper cooling, there must be at least two inches of clear space to the rear and sides of the computer, and three inches above the computer. Clearance at the back must be at least five inches to permit passage of cooling air and to prevent sharp bends in cables entering the computer.

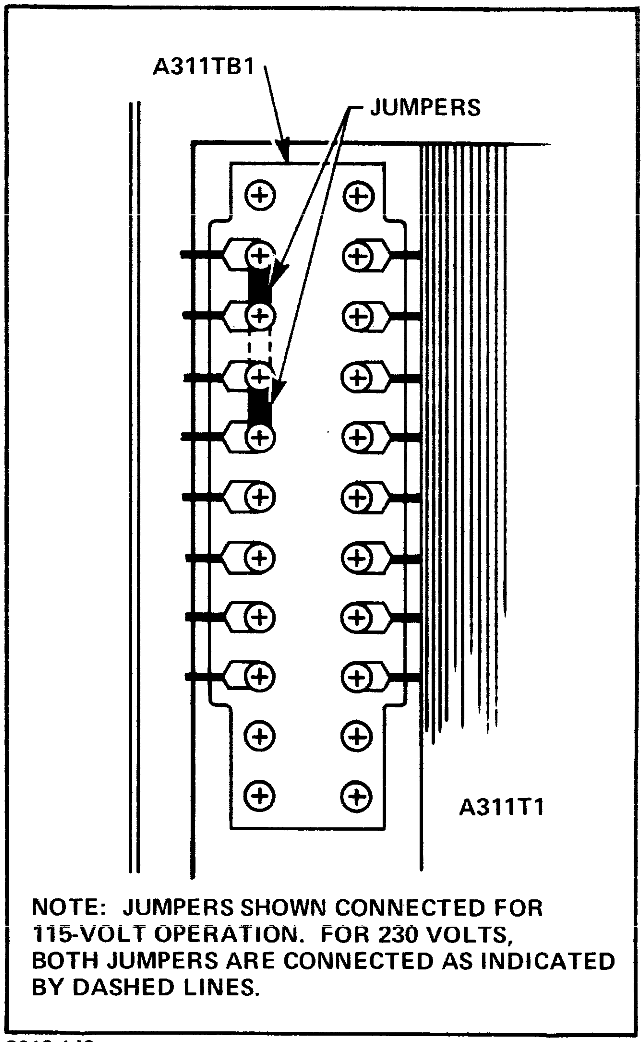

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Figure 2-1. Location of Voltage-Change Jumpers

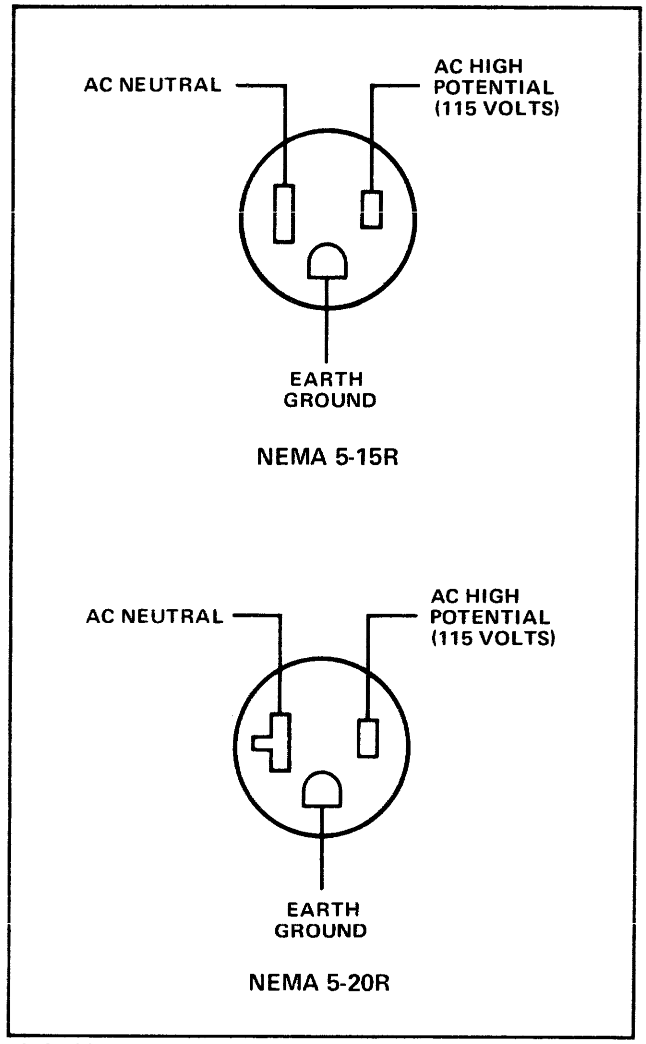

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Figure 2-2. NEMA 5-15R and 5-20R Female Connector, Mating Side

2-24. POWER REQUIREMENTS.

2-25. The computer operates from a power source supplying a nominal ac voltage of 115 or 230 volts rms ±10 percent, single-phase. The required power frequency is 47.5 to 70 Hz. The power consumption ranges from 1000 to 1600 watts, depending on the optional features included in the computer. Note that optional features not within the computer cabinet, and which make separate connection to the power line, have their own power specifications, and the power they require is additional to that consumed by the computer.

2-26. Movable jumpers in the computer permit use of the 2116B on either 115- or 230-volt power lines. The computer is shipped with these jumpers connected in accordance with the customer's order. However, before the computer is connected to the power line, the jumpers must be checked to ensure that they are correctly connected. This is done as follows:

a. Make sure the computer power cable is not plugged into a voltage source.

b. Swing the card cage out of the computer cabinet.

c. Remove the plate covering transformer A311T1, by pulling out the four white studs in the plate. The plate is shown in figure 1-4.

d. Locate terminal strip A311TB1. This terminal strip is mounted on the power transformer, and is the top terminal strip on the left side of the transformer.

e. Check the jumpers on the terminal strip to ensure that they are properly connected. (See figure 2-1.)

f. Replace the transformer cover.

2-27. AC POWER OUTLET AND EXTERNAL GROUND.

2-28. The ac outlet which will supply power to the computer must be checked to ensure that it furnishes the voltage for which the computer is connected. Furthermore, the ac outlet and its associated wiring and fuses (or circuit breakers) must be capable of carrying at least 15 amps for a 115-volt computer, or 7 amps for a 230-volt computer.

2-29. The ac power cable supplied with the computer fits a NEMA (National Electrical Manufacturers Association) type 5-15R or 5-20R female power outlet (figure 2-2). If the computer is to be installed in a building, make sure the local electrical codes permit use of this type of electrical outlet for the line voltage and load current used by the computer. (The 5-15R or 5-20R connector must not be used for 230-volt operation.) If necessary, change the plug on the ac power cable to fit an acceptable type of outlet, as described in paragraph 2-34.

2-30. Check at the ac outlet with a voltmeter to be sure the required voltage is supplied, and that it is single-phase. If the computer is connected for 115-volt operation, the voltage must be 103.5 to 126.5 volts ac (rms). For 230-volt operation, the voltage must be 207 to 253 volts ac (rms). Bear in mind that the electrical load imposed by the computer and its optional features may reduce the line voltage below its no-load value.

2-31. If the voltage is in the correct range, check the ac outlet to ensure that it is correctly wired with respect to high-potential ac voltage, ac neutral, and earth ground. Use a low impedance voltmeter, 20,000 ohms per volt or less, for making these measurements. If the outlet is improperly wired, correction must be made by a qualified electrician, and local electrical codes must be observed if the installation is in a building.

2-32. If the electrical system has only two wires (that is, if there is no separate earth ground wire), the computer will operate with the earth ground lead in the ac power cable unconnected. However, for safety reasons, it is strongly recommended that attachment be made to a good earth ground. This connection must be made through the earth ground wire in the ac power cable used by the computer.

2-33. For installation in a ship, airplane, motor vehicle, or train, the earth ground wire in the computer ac power cable must be connected to the hull or metal frame of the vehicle.

2-34. AC POWER CABLE.

WARNING

If the connector at either end of the 5060-2267 AC Power Cable is changed, the replacement connector must be correctly wired to the cable. If the connector is incorrectly wired, fuse A312F1 in the computer will not remove voltage from the computer ac circuits when the fuse blows. The resulting high voltage at exposed terminals inside the computer presents a hazard to the computer serviceman. A similar precaution applies when an extension cable is used.

2-35. Check AC Power Cable 5060-2267 to be sure it is long enough to connect the computer with the ac outlet to be used. If necessary use a longer cable or add an extension cable. Also, make sure the connector on the cable fits the ac outlet. Any added cabling must have three conductors, with each conductor no. 14 American Wire Gauge or heavier, and connectors must be rated at 15 amps or more.

2-36. If an extension cord is used, or if the connector at either end of AC Power Cable 5060-2267 has been removed, make sure that fuse A312F1 remains on the high-potential side of the power line. This is done as follows:

a. Plug the power cable into the back of the computer. Do not make connection with the ac power source.

b. Plug the extension cord, if used, into the power cable. Do not make connection with the ac power source.

c. Extend the card cage.

d. Remove the bottom panel, situated beneath the backplane connectors (figure 1-5). Do this by removing the screws at the sides of the card cage which hold the panel in place.

e. Set an ohmmeter to the R x 1 scale, and zero the meter.

f. Connect one lead of the ohmmeter to the high-potential prong of the male connector which will plug into the ac source.

g. Connect the other ohmmeter lead to terminal A200TB1-9, at the bottom of the card cage. Figure 1-5 shows the location of this terminal strip. Terminal 9 is the farthest terminal on the strip from the card cage hinges.

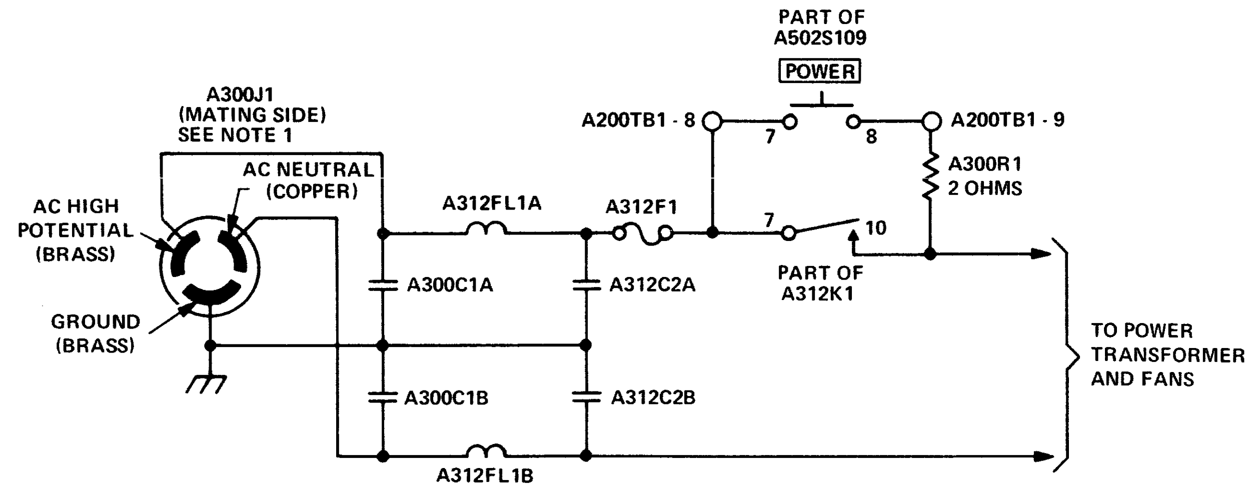
h. Check the ohmmeter reading. If an open circuit is indicated, press the POWER switch (A502S109) on the control panel assembly. When the POWER switch is closed, the ohmmeter reading should be approximately zero (see figure 2-3). If the reading is approximately two ohms or if it is infinity, the power cable connections are incorrect. Make the necessary corrections as described in step "m" below.

i. If the preceding test is satisfactory, press the POWER switch once. The ohmmeter should indicate infinity. If the reading is not infinity, the power cable connections are incorrect.

j. If the preceding step is satisfactory, remove the ohmmeter lead from the high potential prong of the power connector, and connect it to the ac neutral prong of the connector.

k. Check the ohmmeter reading. Approximately two ohms should be indicated. If the resistance is zero or infinity, the power cable connections are incorrect.

l. If the preceding step is satisfactory, check the resistance between the earth ground prong of the power con-



NOTES:

1. WARNING. FOR SAFETY REASONS, THE AC LINE MUST BE CONNECTED AS SHOWN, PLACING FUSE A312F1 ON THE HIGH POTENTIAL SIDE OF THE LINE.

2. THIS SYMBOL INDICATES CONNECTION TO THE COMPUTER FRAME.

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Figure 2-3. AC Distribution Diagram

nector and the frame of the computer. Zero ohms should be indicated. If the reading is infinity, the power cable is incorrectly wired.

m. If any of the preceding measurements is incorrect, make the necessary changes in connector wiring. If an extension cord is used, change connections in one of the extension-cord connectors, rather than in the factory-wired 5060-2267 AC Power Cable. After making the correction, repeat the entire check procedure, starting with step e above.

n. After completion of the test, replace the bottom panel.

2-37. MOUNTING.

WARNING

If the 2116B is mounted in a rack which has slide-out drawers, heavy doors, or heavy protruding devices, the rack must be bolted to the floor or heavily weighted at the base. Otherwise, when the 2116B card cage is extended, there is danger of the rack tipping forward. This possibility does not exist when the 2116B is placed on a bench or table top.

2-38. The computer is designed either for bench installation or for mounting in a standard 19-inch equipment rack. When installed on a shelf, bench, or table, the computer need not be fastened down except for shipboard, aircraft, or other mobile use. For these mobile installations, shock mounts must be used. When installed in a rack, mount the computer in accordance with the instructions included in the rack-mounting kit. The entire rack must be shock mounted in mobile installations.

2-39. After the computer has been mounted, install and connect optional devices which are external to the computer. (Internal devices are factory-installed.)

2-40. Set the LOADER switch to the PROTECTED position and connect the computer and external devices to the ac power source. Then perform steps a, f, and g of paragraph 5-24. When this has been completed, make a performance check of the computer and all optional features as explained in the next paragraph.

2-41. PERFORMANCE CHECK.

2-42. The performance check of the computer consists of two parts. The first part is a pretest checkout of computer controls and program-loading ability. This is referred to as the basic checkout. The second part is a performance test, using diagnostic programs. Instructions for both the basic checkout and diagnostic test are given in section IV of this volume. Performance checks of optional devices are described in the manuals for the devices.

2-43. CLAIMS.

2-44. If the computer is incomplete or damaged when received, or if it fails to meet specifications, notify the nearest Hewlett-Packard Sales and Service Office. (Sales and Service Offices are listed in the back of this volume.) If damage occurred in transit, notify the carrier also. Hewlett-Packard will arrange for replacement or repair without waiting for settlement of claims against the carrier.

2-45. REPACKAGING FOR SHIPMENT.

2-46. SHIPMENT USING ORIGINAL PACKAGING.

2-47. The same containers and materials used in factory packaging can be used for reshipment of the computer. Alternatively, containers and packing materials may be obtained from Hewlett-Packard Sales and Service Offices. If the computer is being sent to the factory for servicing, attach a tag to the computer with the return address and indicating the type of service required, the computer model number, and the full serial number of the computer. Mark the container "FRAGILE" to assure careful handling. In any correspondence, refer to the computer by model number and full serial number.

2-48. SHIPMENT USING NEW PACKAGING.

2-49. The following instructions should be followed when packaging the computer with commercially available materials:

a. Wrap the computer in heavy paper or sheet plastic. If shipping the computer back to the factory, first attach a tag to the computer with the return address and indicating the type of service required, the computer model number, and full serial number.

b. Use a strong shipping container. A double-wall carton of 350-pound test material is adequate.

c. Use enough shock absorbing material (3- to 4-inch layer) on all sides of the computer to provide a firm cushion and to prevent movement inside the container. Use particular care to protect corners, the control panel, and the display panel.

d. Seal the shipping container securely, and mark it "FRAGILE".

e. In any correspondence with the factory, refer to the computer by model number and full serial number.

2-50. WARRANTY.

2-51. The terms of the warranty for the HP 2116B Computer are described in the warranty notice inside the front cover of this manual. For any additional information concerning the warranty, contact the nearest Hewlett-Packard Sales and Service Office.

SECTION III

THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section explains the theory of operation of the 2116B Computer. The discussion is conducted at the block-diagram level, with circuit-diagram analysis of complex nondigital circuits. Complex logic circuits are also given detailed treatment in this section. However, complete coverage of logic circuits is reserved for section IV of this volume, where troubleshooting charts together with the logic diagrams in section V present a fully detailed view of computer functioning. Throughout the theory discussions the term "current flow" refers to electron flow.

3-3. REFERENCE INFORMATION.

3-4. The following paragraphs present general information which is required for understanding the theory discussions in this section.

3-5. ABBREVIATIONS.

3-6. Abbreviations of flip-flop names, and abbreviated designations of signals, are defined in table 5-7.

3-7. BINARY VOLTAGE LEVELS.

3-8. The binary signal levels in the computer are approximately +2.3 volts and +0.2 volts. The levels may vary from these approximate amounts, depending on the type of integrated circuit providing the signal, its condition, and its load. The minimum and maximum input and output voltages for each type of integrated circuit are specified in table A-7.

3-9. In this manual, the +2.3 volt logic level is referred to by term "true", and the +0.2 volt level is referred to as "false".

3-10. LOGIC CIRCUITS.

3-11. The logic circuits principally employ positive logic. That is to say, all inputs to an "and" or "nand" gate must be +2.3 volts for coincidence to occur. Similarly, if any input to an "or" or "nor" gate is +2.3 volts, the output is +2.3 volts for an "or" gate or +0.2 volts for a "nor" gate. The output from the "set" side of a flip-flop is approximately +2.3 volts when the flip-flop is set, and +0.2 volts when the flip-flop is reset.

3-12. The logic symbols used in this manual are described in appendix A.

3-13. SIGNAL NAMES.

3-14. Signals are named in one of the following ways:

a. As a condition which either exists or does not exist.

b. In accordance with the name of a flip-flop or panel switch which is the source of the signal.

c. In accordance with the name of the bus which carries the signal.

d. As a command or order, expressed in the imperative grammatical mode.

3-15. Since most circuits in the computer employ positive logic, signal names are positive-true. The following paragraphs describe the expression "positive-true name" as applied to each of the four types of signal names.

3-16. When a signal is named in accordance with a condition, the signal level is +2.3 volts when the condition exists, and +0.2 volts when the condition does not exist. For instance, the MRT signal is +2.3 volts during memory read time, and +0.2 volts at other times. Similarly, the "not" OPO signal is +2.3 volts when a one-phase instruction is not being performed.

3-17. When a signal is named in accordance with the flip-flop which is its source, the signal taken from the set side of the flip-flop is +2.3 volts when the flip-flop is in the set condition, and +0.2 volts when the flip-flop is in the reset condition. For instance, when the Flag Buffer FF is in the set state, the FBFF signal is +2.3 volts.

3-18. When a signal is named in accordance with the bus which carries it, the signal is +2.3 volts when the bus carries a logic 1, and +0.2 volts when it carries a logic 0.

3-19. When a signal is named in the imperative mode, it becomes +2.3 volts to bring about the action commanded. For instance, the Flag FF is cleared when the CLF (clear flag) signal changes from +0.2 volts to +2.3 volts.

3-20. FUNCTIONAL SECTIONS.

3-21. From a functional standpoint, the computer consists of five sections. These are the control section, arithmetic section, memory section, input/output section, and power supply section. Various optional devices can augment these sections by extending their capabilities. The circuit theory of the optional features is dealt with in the technical manual for the device concerned.

3-22. The physical grouping of electronic assemblies in the computer corresponds to the functional sections. As figure 1-3 shows, the circuit cards for the memory, control, arithmetic, and I/O sections are grouped together in the card cage in accordance with function. On the back of the card cage (figure 1-5), behind the memory cards, the core stack assembly is mounted. The power supply is installed in the back of the computer cabinet. Controls and indicators for the various functional sections are mounted on the door assembly (figures 1-6 and 1-7).

3-23. Figure 3-1 illustrates the internal makeup and functional relationships of the five major computer sections.

3-24. CONTROL SECTION.

3-25. The control section directs the overall functioning of the computer. The control function is exerted by pulse signals which result from decoded instruction words read from the memory section. These control signals are furnished at a rate, and have a duration, that is determined by the timing circuits.

3-26. TIMING CIRCUITS.

3-27. The timing circuits consist of the basic timing circuits and the memory timing circuits. These are described in the paragraphs which follow.

3-28. BASIC TIMING CIRCUITS. The basic timing circuits make up part of timing generator card A106. They consist of an oscillator, a frequency divider, time-strobe generator circuits, and a time period generator. These are illustrated in block diagram form in figure 3-2, and described in the following paragraphs.

3-29. Oscillator. A crystal-controlled Colpitts oscillator, consisting of transistor A106Q1 and its associated components (figure 3-3), produces a 10-MHz signal which is the fundamental timing element within the computer. The output of the oscillator is amplified by A106Q2, buffered by A106Q3, and furnished to the frequency divider. The output of A106Q3 is shown in figure 4-16.

3-30. Frequency Divider. The frequency divider consists of flip-flops $\overline{CF1}$ and $\overline{CF2}$ (figure 3-4). The J and K inputs to each of these flip-flops are connected to 4.5 volts. The flip-flops therefore function as divide-by-two counters, each triggered by a negative-going input to pin 1. The CF1 FF receives the output of the 10-MHz oscillator, and furnishes a square wave with a period of 200 ns. The CF2 FF receives this signal, and provides a square wave with a period of 400 ns. (See figure 4-15.)

3-31. Two "and" gates combine the outputs of the CF1 and CF2 FFs to produce the CL1 and CL2 signals. (See figure 4-15.)

3-32. Time Strobe Circuits. The time strobe circuits (figure 3-4) produce two signals, TS and TSA. The signals occur simultaneously, and have a duration of 45 to 50 ns. The TS pulse is used in the control and arithmetic sections when a short pulse, synchronized with computer timing, is required. The TSA pulse is used for the same purpose by certain optional devices. The timing of TS and TSA, relative to other computer timing pulses, is illustrated in figure 4-15.

3-33. The TS and TSA pulse are produced by the "not" output of the CF1 FF, "anded" with the same signal delayed approximately 50 ns. The delay results from capacitor A106C6, the value of which is selected to produce the required wait after the CF1 FF becomes reset. The termination of the TS and TSA pulses occurs when the CF1 FF is set.

3-34. The two "and" gates A106MC42A and A106MC75B perform corresponding functions for the TS and TSA signals, respectively.

3-35. If a component in the discharge path of A106C6 is changed, it may also be necessary to change the capacitor itself in order to retain the required 45-50 ns duration of TS and TSA. (Components in the discharge path are A106MC52A, A106MC52B, and A106MC52R2.) The value of A106C6 typically ranges between 100 and 180 pF.

3-36. Time Period Generator. The time period generator consists of a ring counter and associated "and" gates (figure 3-5). The unit produces eight basic pulses, synchronized with the 10-MHz oscillator, and used for timing purposes throughout the computer. These pulses are referred to as clock pulses, and are designated "T0" through "T7". They are furnished in the sequence in which they are numbered, with each pulse rising as the preceding one falls. After pulse T7, pulse T0 is again produced without interruption of the sequence. Each pulse has a duration of 200 ns. The eight pulses, lasting for 1.6 microseconds, make up the basic machine cycle of the computer. This cycle starts at the beginning of pulse T0, and ends at the end of pulse T7.

3-37. As well as identifying the clock pulses, the terms "T0" through "T7" designate the time periods corresponding to the pulses. For example, time period T3 is the time during which the T3 pulse is true.

3-38. In addition to the T0 through T7 pulses, the time period generator also produces double-length pulses, lasting for 400 ns. These are named in accordance with the two sequential clock pulses during which they are furnished. For instance, the T0T1 pulse is true during time periods T0 and T1.

3-39. One more pulse produced is the T7S pulse, which is true during the last quarter of time period T7.

3-40. The various pulses furnished by the time period generator are included in figure 4-15. The T6 pulse is used only by cards A109 and A110, which comprise the optional Extended Arithmetic Unit. Microcircuits on these two cards contain TTL gates which receive the T6 pulse. The input

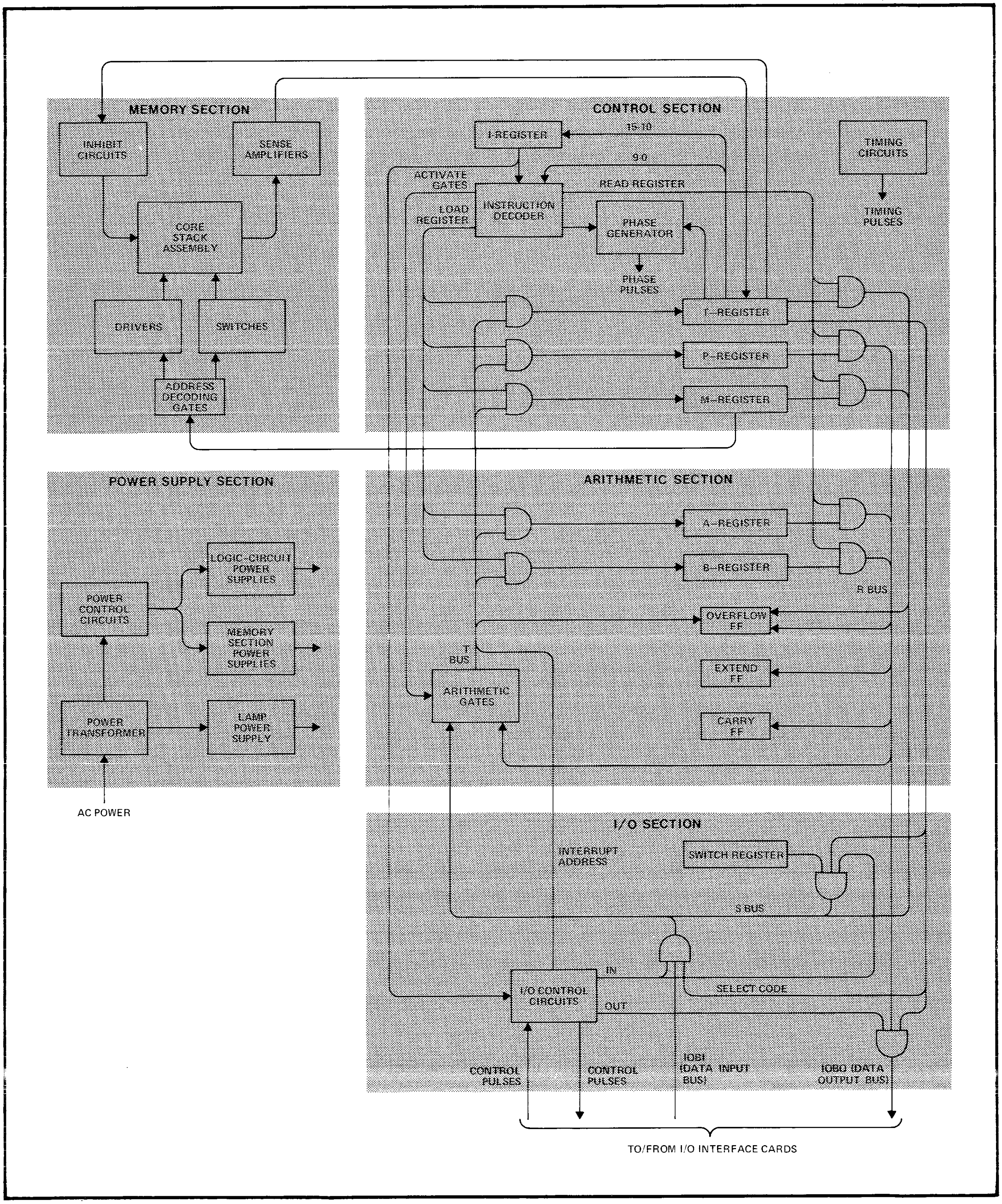

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Figure 3-1. 2116B Computer, Functional Block Diagram

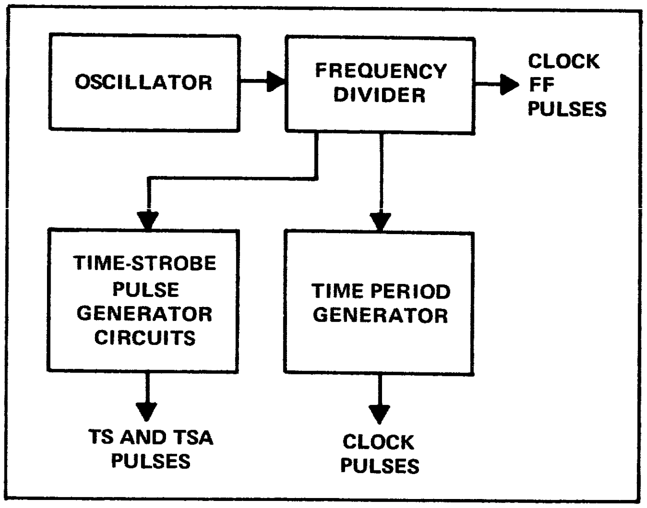

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Figure 3-2. Basic Timing Circuits, Block Diagram

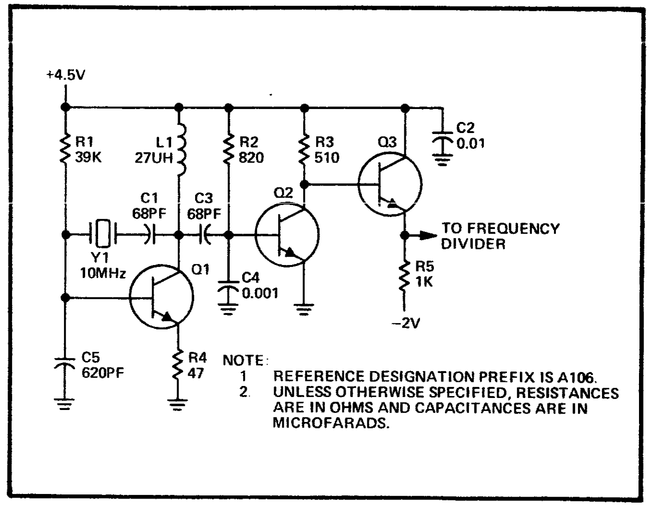

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Figure 3-3. Oscillator, Schematic Diagram

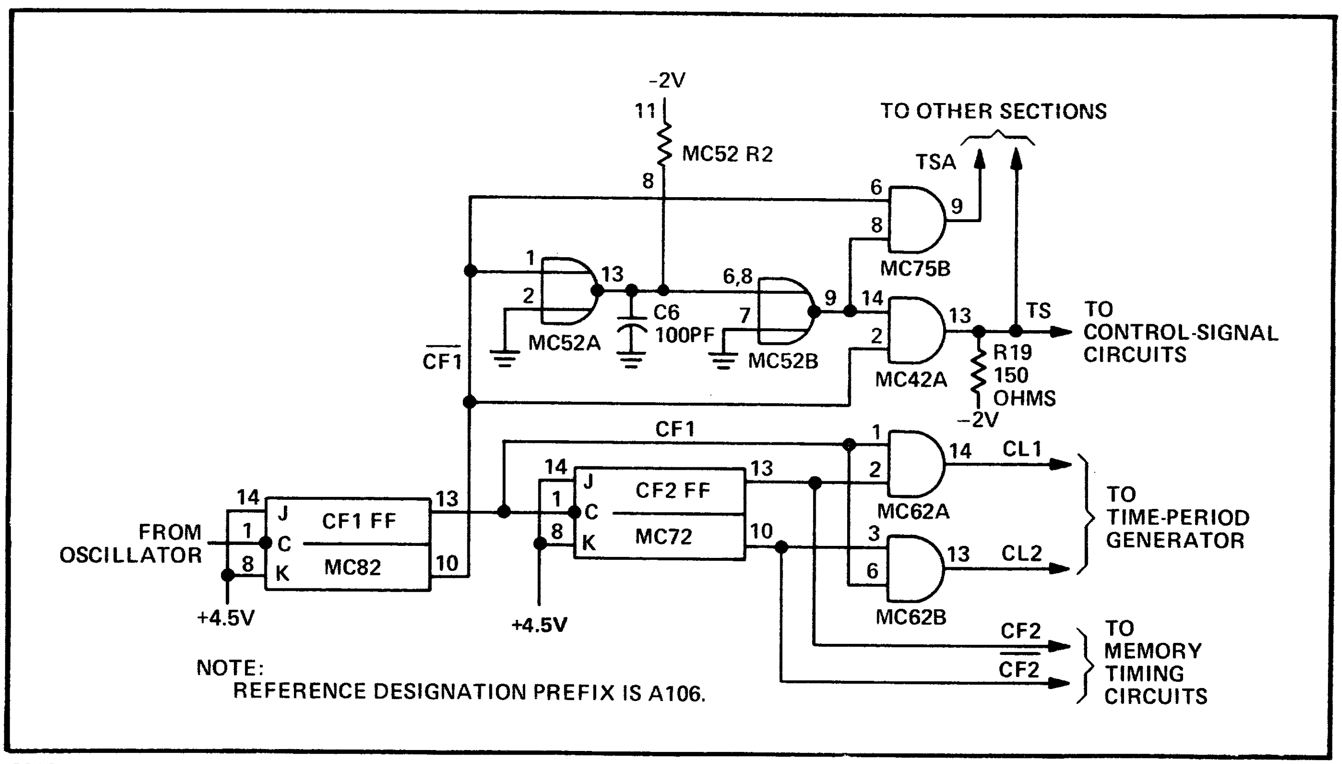

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Figure 3-4. Frequency Divider and Time Strobe Circuits, Logic Diagram

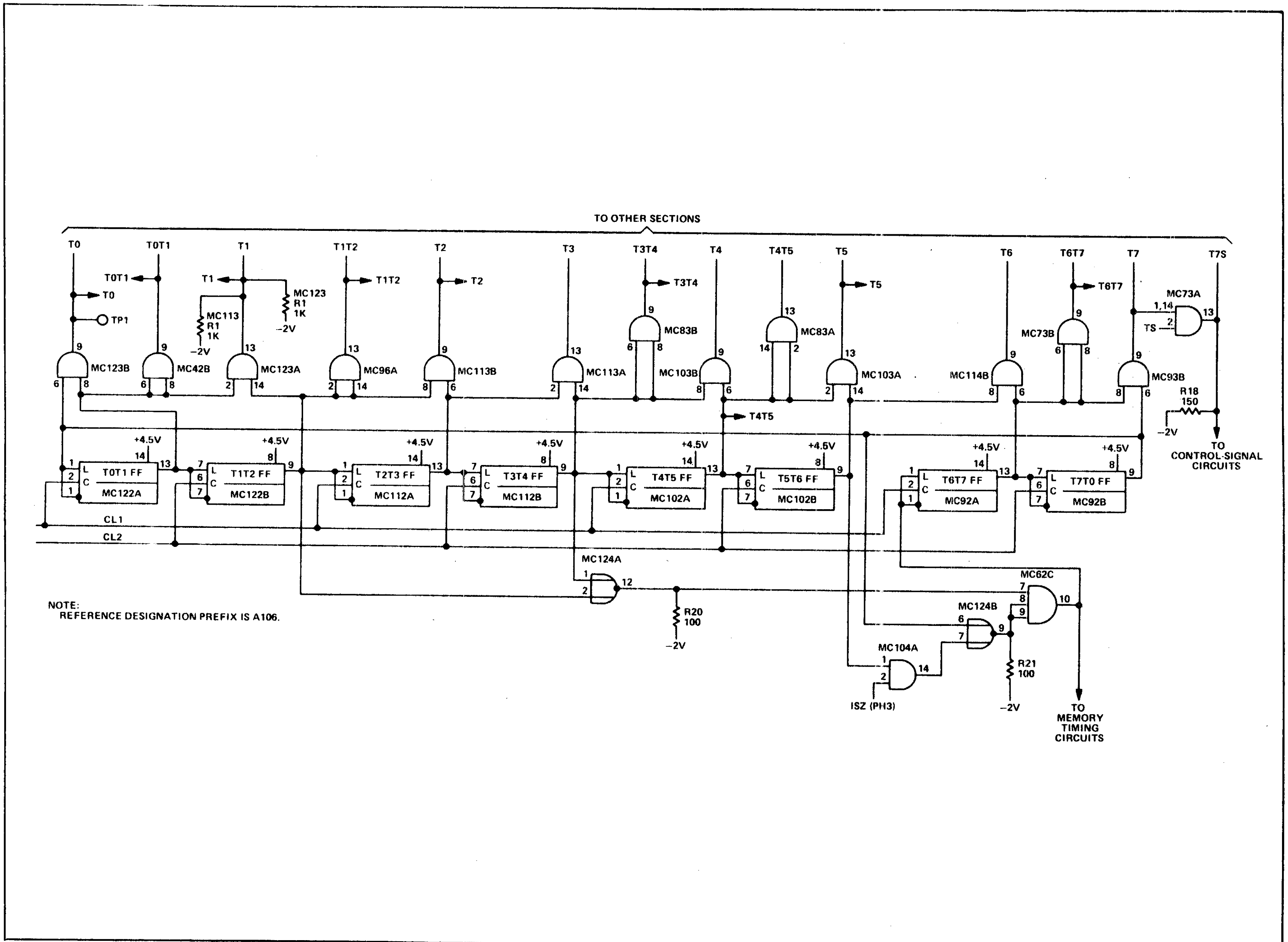

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Figure 3-5. Time Period Generator, Logic Diagram circuits to the gates furnish resistive paths to -2 volts. These resistances function as pull-down resistors, required for development of the T6 pulse. If the A109 and A110 cards are not installed, the absence of pull-down resistors results in the T6 pulse remaining permanently true.

3-41. The ring counter consists of eight latch flip-flops. Of these, two are set at any given time, and the remaining six are clear. The two set flip-flops are always adjacent to each other (as the flip-flops are shown in figure 3-5), except that once during each cycle the two set flip-flops are the T7T0 FF and the T0T1 FF.

3-42. The ring counter is operated by the CL1 and CL2 signals, which trigger alternate flip-flops in the counter. From the CL1 and CL2 waveform in figure 4-15, it can be seen that the flip-flops operate in a leap-frog fashion. That is, the positive-going edge of each CL1 and CL2 pulse clears the trailing flip-flop of the two that are set, and sets the flip-flop immediately ahead of the other flip-flop.

3-43. When power is applied to the computer, the flip-flops in the ring counter assume a random state. Within one machine cycle (four CL1 pulses and four CL2 pulses), the ring counter is in the required condition, with two adjacent flip-flops set and the remaining flip-flops clear. At this time the clock pulse furnished is T6, and for this reason the clock pulses in figure 4-15 begin with T6. The circuits which bring about the initial condition are the following A106 "nand" gates: MC124A, MC124B, and MC62C. The "nand" gate MC104A is enabled only during an ISZ instruction; operation of this gate is dealt with in the explanation of the ISZ instruction in section IV.

3-44. MEMORY TIMING CIRCUITS. The memory timing circuits, on timing generator card A106, provide pulse signals for controlling the transfer of data to and from the core stack assembly. The signals are generated from clock pulses, panel controls, and pulses received from the instruction decoder. Through the use of gates, the memory timing circuits produce from these inputs the required pulses for controlling core-memory writing and reading. Since the memory timing signals are produced by simple gating circuits, detailed discussion of the circuits is unnecessary. It should be noted, however, that the MWL pulse remains permanently true if neither of the following cards is installed: card A3 (Parity Error Option) and card A21 (Memory Protect Option). As with the T6 pulse, pull-down resistors on the optional cards are required for production of the MWL pulse.

3-45. CONTROL SECTION REGISTERS.

3-46. The registers in the control section are the transfer register (T-register), memory address register (M-register), program address register (P-register), and instruction register (I-register).

3-47. T-REGISTER. The T-register receives 16-bit words which will be stored in, or which have been read from, the core memory section (see figure 3-1). The various stages of the T-register are on four arithmetic logic cards, with reference designations A102, A103, A104, and A105.

3-48. M-REGISTER. The M-register specifies the core memory address in which a word will be stored, or from which a word will be retrieved (see figure 3-1). The various stages of the M-register are on arithmetic logic cards A102, A103, A104, and A105.

3-49. P-REGISTER. The P-register specifies the core memory address from which the next instruction word will be read (see figure 3-1). When the P-register contents are used, they are gated onto the R bus, passed through the arithmetic gates, and gated into the M-register. From here, the address is forwarded to the memory section. The various stages of the P-register are on arithmetic logic cards A102, A103, A104, and A105.

3-50. I-REGISTER. The I-register is a 6-bit register which receives bits 15 through 10 of each instruction word read from the core memory section (see figure 3-1). The I-register holds these bits while they are decoded by the instruction decoder. The register is on instruction decoder card A107.

3-51. INSTRUCTION DECODER.

3-52. The instruction decoder examines each instruction word read from the memory section, and produces control pulses in accordance with the type of instruction indicated. These pulses activate flip-flops, gates, and registers in the memory, arithmetic, control, and I/O sections to bring about the functions required by the instruction.

3-53. When an instruction word is read from the memory section, it is placed in the T-register (see figure 3-1). Bits 15 through 10 are forwarded to the 6-bit I-register, and from there to the instruction decoder. Bits 9 through 0 of the T-register are furnished directly to the instruction decoder.

3-54. During the course of each instruction, the instruction decoder gates register contents onto the R bus or S bus, loads registers from the T bus, and activates the arithmetic gates to bring about the required functions.

3-55. In the case of a memory reference instruction, the instruction decoder brings about the reading of the required word from the memory section. This is done by activating the memory timing circuits with appropriate control pulses. The word read is placed in the T-register. This destroys the instruction word itself. However, six bits of the word remain in the I-register. These bits, together with various flip-flops set earlier in the instruction, control the computer during the remainder of the instruction.

3-56. The instruction decoder is on instruction decoder card A107 and shift logic card A108.

3-57. PHASE GENERATOR.

3-58. The phase generator produces four pulse-type signals which determine the basic function performed by the computer during each 1.6-microsecond machine cycle. The four signals are named phase 1, 2, 3, and 4, in accordance with the four types of machine cycle. These machine cycles serve the following purpose:

a. Phase 1, referred to as the fetch phase, is the machine cycle in which an instruction word is obtained from the memory section. This is the first phase of each instruction, and in some cases the entire instruction is completed during this machine cycle.

b. Phase 2, called the indirect phase, is used when indirect addressing is indicated by the instruction word. (Bit 15 of the word, when logic 1, specifies indirect addressing.) Indirect addressing is used only with memory reference instructions. In instruction words of this type, bits 9 through 0 normally are an operand address in the current page. With indirect addressing, however, the 16-bit word in the memory location indicated by these bits is itself used as an address. Another reference is then made to the memory section to obtain the operand. In this case, 15 bits are available for specifying the address; therefore any page can be referenced. The computer is in phase 2 for the machine cycle during which the 15-bit address word is used. Multiple-step indirect addressing is also possible. If bit 15 of the word obtained during phase 2 is logic 1, another phase 2 machine cycle is performed, and the word acquired in the first phase 2 is used as the address from which another address word is obtained. Phase 2 machine cycles continue until a word is acquired in which bit 15 is logic 0. This word is the address of the operand, and a final phase 2 is performed to acquire this operand.

c. Phase 3, the execute phase, is a machine cycle in which the computer operates as indicated by the instruction word acquired in the preceding fetch phase.

d. Phase 4, the interrupt phase results from an interrupt by an I/O device. Phase 4 suspends the computer program for performance of an instruction stored at the core location corresponding to the type of interrupt. Another use of phase 4 is for the execution of a program jump when ac line voltage fails.

3-59. An additional phase, phase 5, is used by the direct memory access system. Since DMA is an optional feature, phase 5 is explained in the Operating and Service Manual for DMA.

3-60. Phase 2, if performed, follows phase 1 or a prior phase 2. Phase 3 follows phase 1 or phase 2. The last phase of an instruction is phase 1 (for a single-phase instruction), or phase 3 (for a multiple-phase instruction). Phase 4 can come between any two phases.

3-61. Lamps on display board assembly A501 light when the computer is in the fetch, indirect, or execute phase. Because of the speed of operation of the computer, these lamps serve a useful function only when the computer is stopped or when it is being stepped with the SINGLE CYCLE switch.

3-62. The phase generator is on timing generator card A106.

3-63. ARITHMETIC SECTION.

3-64. The arithmetic section of the computer performs the addition, subtraction, or other data manipulation for each instruction requiring such operations. The data manipulation is performed by three major circuit groups: the accumulators, the computational registers, and the arithmetic gates. (See figure 3-1.)

3-65. ACCUMULATORS.

3-66. The computer has two accumulators: the A-register and the B-register. Each accumulator holds a 16-bit data word before during, and after data manipulation is performed on the word.

3-67. Normally, only one accumulator is used during the course of an instruction, the accumulator in use being specified by the instruction word. However, the other accumulator can be addressed in the same manner as a core storage location, thereby permitting inter-accumulator operations. For instance the contents of the A-register can be compared with the contents of the B-register, using a single instruction. Also, either accumulator can be addressed by an instruction which does not involve the other accumulator. In this type of operation the data in the addressed accumulator is treated as if it were in a core storage location.

3-68. The address of the A-register is 00000 (octal). The address of the B-register is 00001 (octal).

3-69. The various stages of the two accumulators are on arithmetic logic cards A102, A103, A104, and A105.

3-70. COMPUTATIONAL REGISTERS.

3-71. Three 1-bit computational registers aid in performing data manipulation and recording the results obtained. The registers are the Overflow, Extend, and Carry FFs. The Overflow FF is used to hold control information, and to record positive arithmetic overflows from the accumulators. The Extend FF detects negative arithmetic overflows from the accumulators, and links the two accumulators during rotate instructions. The Carry FF detects and stores certain control and bit conditions.

3-72. Lamps on display board assembly A501 light when the Overflow or Extend FF is set.

3-73. The Overflow, Extend, and Carry FF's are on shift logic card A108.

3-74. ARITHMETIC GATES.

3-75. The principal data-manipulations in the computer are performed by the arithmetic gates (figure 3-1). The gates use timing and control signals to regulate the transfer of data from the R and S buses to the T bus. In doing this, the gates can perform any of the following arithmetic operations:

a. Add the number on the R bus to the number on the S bus.

b. Add 1 or 2 to the number on the R bus.

c. Combine the number on the R bus with the number on the S bus, using any of the following logic functions: "and", inclusive "or", exclusive "or".

d. Complement the number on the R bus.

e. Shift the number on the R bus to the right one position, to the left one position, or to the left four positions.

f. Transfer data unchanged from the R or S bus to the T bus.

3-76. After passing through the arithmetic gates, data can be loaded into the T-register, P-register, M-register, A-register, or B-register, or Overflow FF.

3-77. MEMORY SECTION.

3-78. The 2116B memory section employs a core storage unit of the conventional coincident-current parallel-readout type. In its basic configuration, the computer has one 8,192-word (8K) core stack assembly. As an optional feature, one more 8K core stack assembly can be installed in the computer cabinet. Furthermore, one or two additional 8K core stacks can be added to the system in a cabinet external to the computer.

3-79. The discussion which follows deals with a memory section incorporating either one or two 8K core stack assemblies. For the circuit theory of systems which include one or two additional stacks (24K or 32K systems), refer to the Operating and Service Manual for the 2150B Input/Output and Memory Extender.

3-80. The core stack assembly includes provisions for storing a parity bit with each word. Use of this feature is optional, and the circuit theory is covered in the Operating and Service Manual for the 12591A Parity Error Option.

3-81. Before reading the theory discussion of the memory section, the reader must be familiar with the principles of core storage memories. An explanation of this type of storage device can be found in most text books dealing with the basics of digital computers.

3-82. CORE STACK ASSEMBLY.

3-83. The 8K core stack is made up of a diode matrix, and ferrite cores which provide 8,192 word-storage locations. The diode matrix, at the top of the assembly, consists of 256 diodes on a mounting board. Below this are five additional mounting boards with core matrices installed on the top and bottom of each board. The construction is such that for each word there is more than one core on a physical plane.

3-84. Each word-location in the core stack assembly consists of 17 ferrite cores. Of these, 16 are used for storing a data word, while the remaining core is reserved for a parity bit. If the parity-check feature is not installed, the 17th core remains unused.

3-85. ORGANIZATION OF DATA.

3-86. The word-locations in the core stack assembly are divided into two 4K groups, referred to as the upper module and lower module. In the basic 8K core stack assembly, word-locations in the lower module are assigned addresses from 00000 through 07777, while the upper module contains locations 10000 through 17777. The terms "lower" and "upper" refer to the octal addresses pertaining to the two modules, rather than the physical relationship of the modules.

3-87. Each 4K module is divided into four "pages", each consisting of 1,024 words.

3-88. Figure 3-6 shows the octal addresses in each module and page.

	1ST 8K CORE STACK	2ND 8K CORE STACK
LOWER MODULE 4,096 WORDS (4 PAGES)	00000 to 01777	20000 to 21777
	02000 to 03777	22000 to 23777
	04000 to 05777	24000 to 25777
	06000 to 07777	26000 to 27777
UPPER MODULE 4,096 WORDS (4 PAGES)	10000 to 11777	30000 to 31777
	12000 to 13777	32000 to 33777
	14000 to 15777	34000 to 35777
	16000 to 17777	36000 to 37777

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Figure 3-6. Organization of Data in Core Stack Assembly

3-89. MEMORY READ OPERATIONS.

3-90. When a word is to be read from the core stack assembly, its address is first placed in the 16-bit M-register (refer to figure 3-1). The address is then forwarded to the memory section, the word is acquired from the specified word-location, and the T-register receives the word read. This operation is performed for each of the three basic types of readout operation, which are as follows:

a. Readout of a word for display in the T-register.

b. Readout of an instruction word to be performed by the computer.

c. Readout of an operand which will be used by the program.

3-91. READOUT FOR DISPLAY. When a word is to be displayed in the T-register the computer must not be running, otherwise the word will not remain in the register long enough for visual perception. The readout for display is brought about by setting into the SWITCH REGISTER switches the address of the required word. Then the LOAD ADDRESS switch is pressed, followed by the DISPLAY MEMORY switch. When the LOAD ADDRESS switch is pressed, the number in the switch register is placed on the S bus. From there it passes unchanged through the arithmetic gates, and is loaded into the M-register.

3-92. Next, the DISPLAY MEMORY switch is pressed. The address decoding gates in the memory section decode the contents of the M-register, and the word at the specified address is read from memory, sensed by the sense amplifiers, and placed in the T-register. The word is then available for visual inspection in the T-register display lamps.

3-93. The memory readout operation leaves zeros in the 16 ferrite cores at the addressed location. Therefore, it is necessary to rewrite the word in these cores. This is done immediately after the memory readout has taken place, and occurs without manual intervention by the operator. Immediately after the memory readout operation the M-register still indicates the addressed location, and the memory timing circuits restore the word in the memory section by attempting to store logic 1 in each bit position of the addressed word-location. However, the inhibit circuits prevent this in the ferrite cores that originally contained logic 0. The word that was read out is in the T-register, and from this word the inhibit circuits determine the cores that must remain in the logic 0 state.

3-94. INSTRUCTION-WORD READOUT. The second type of memory readout occurs when the computer acquires an instruction word to be performed by the program. The P-register contains the address of the instruction, and at the start of each phase-1 machine cycle the P-register contents are gated onto the R bus, passed through the arithmetic gates, and loaded into the M-register (figure 3-1). When the address passes through the arithmetic gates, logic 1 is added to the number. As well as being loaded into the M-register, the modified address is placed in the P-register in preparation for acquisition of the next instruction word.

3-95. When the address of the instruction word to be acquired is loaded into the M-register, it is decoded in the memory section, and the word is read from its memory location and rewritten as before. In this case, after the word is placed in the T-register, bits 15 through 10 are forwarded to the I-register, and the I-register and T-register contents are decoded to determine the kind of instruction to be performed.

3-96. In the type of memory readout previously described, a word was acquired from the memory section for display purposes. This operation was not followed by decoding of the word by the instruction decoder. It is the decoding process which brings about actions in the computer under control of the instruction, and this is the distinguishing feature between words treated as data and words which are handled as instructions. The difference in the way words are treated after they are read from the memory section is controlled by the phase generator.

3-97. OPERAND READOUT. The third method of addressing a core memory location is used by memory reference instructions. Instructions of this type acquire an operand from the memory section, and perform an arithmetic or logic operation using the operand. The operand word is acquired either by direct addressing or by indirect addressing, as designated by bit 15 of the instruction word. If bit 15 is logic 0, the operand is acquired from the memory section by direct addressing. If the bit is logic 1, indirect addressing is employed.

3-98. Direct Addressing. When direct addressing is used, the computer enters phase 3 (the execute phase) after acquiring the instruction word in phase 1. In phase 3 the operand is acquired from the memory section, and acted upon in accordance with the type of instruction being performed.

3-99. When direct addressing is used, the operand must be obtained either from memory page zero, or from the same memory page in which the instruction word is located. Bit 10 of the instruction word identifies the page to be used, logic 0 indicating page zero and logic 1 the current page.

3-100. When the instruction word is acquired from the memory section, it is placed in the T-register (figure 3-1). When the word is decoded and found to be a memory reference instruction, bits 9 through 0 of the T-register are gated onto the S bus, passed unchanged through the arithmetic gates, and are loaded into the M-register. This takes place near the end of phase 1. If the memory page being referenced is the current page, positions 15 through 10 of the M-register retain the contents they had when the instruction word was acquired. These bits designate the core stack, module, and page to be referenced, and since they remain unchanged, the operand is obtained from the page in which the instruction word is stored. If bit 10 of the instruction word indicates page zero, bits 15 through 10 of the M-register are cleared, and page zero of the basic core stack assembly is referenced.

3-101. After the M-register is loaded, the computer enters phase 3, and the referenced word is acquired from the memory section and placed in the T-register. The use then made of the operand depends on the type of instruction being performed.

3-102. Indirect Addressing. With indirect addressing, the instruction word is acquired from the memory section and placed in the T-register as before. The M-register is also loaded with the operand address in the same manner as for direct instruction addressing. However, because bit 15 of the instruction word is logic 1, the computer enters phase 2 (the indirect phase) after the completion of phase

1. In phase 2 the referenced word is acquired from page zero or the current page and placed in the T-register as before. However, the word acquired is not treated as an operand to be operated on by the instruction, nor is it handled as an instruction word. Instead, it is forwarded to the M-register and treated as an address word. This time, bits 14 through 0, rather than 9 through 0, are routed from the T-register to the M-register. Consequently, any address in any of the core stack assemblies can be referenced.

3-103. When the word is acquired from the memory section during phase 2, it is placed in the T-register in the normal way. Bit 15 of the word is then checked to determine whether another indirect addressing operation is to be performed. If bit 15 is logic 1, the new word is treated as an address word, the word is forwarded to the M-register, and another phase 2 machine cycle is performed. The computer continues to perform phase 2 machine cycles until a word is acquired in which bit 15 is logic 0. The computer then enters a phase 3 machine cycle, and the word acquired in the last phase 2 cycle is treated as an operand.

3-104. MEMORY WRITE OPERATIONS.

3-105. Memory write operations are very similar to memory read operations. First, bits 9 through 0 of the instruction word are routed from the T-register to the M-register. M-register bits 15 through 10 are cleared if page zero is being referenced. Following this, the word to be written is gated onto the T-bus and loaded into the T-register. Then, the word currently stored in the addressed memory location is read out by placing the ferrite cores at that location in the zero state. However, instead of being placed in the T-register, the word read from the memory section is discarded. (That is, no flip-flops are set by the pulses from the sense amplifiers.) Finally, the word formerly placed in the T-register is written in the addressed location. This is done in the same manner as rewriting a word that has been read out of the memory section.

3-106. DETAILED DISCUSSION OF MEMORY SECTION.

3-107. BLOCK DIAGRAM ANALYSIS. When memory reading or writing is performed, the address decoding gates (figure 3-1) examine bits 11 through 0 of the M-register to determine the word-location to be referenced. These 12 bits can indicate any octal address from 0000 through 7777, corresponding to the 4,096 locations in the lower or upper module of the core stack assembly.

3-108. Bits 11 through 6 of the M-register indicate the Y drive-line to be used (see figure 3-7). These bits are decoded to yield their octal equivalent, in the form of two octal digits. Bits 11, 10, and 9 give the most-significant-digit (MSD), and bits 8, 7, and 6 give the least-significant-digit (LSD). Together, these two digits identify one of the 64 Y drive-lines in the core stack assembly.

3-109. Bits 5 through 0 of the M-register are decoded in a manner similar to that used for bits 11 through 6, to yield a 2-digit octal number identifying the X drive-line.

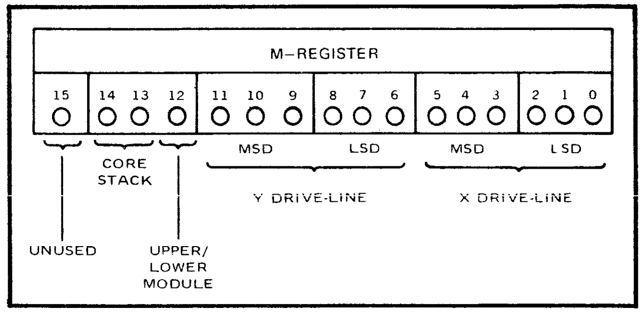

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Figure 3-7. Significance of M-register Contents

3-110. Bits 14 through 12 of the M-register are also examined in the memory section to identify completely the memory location to be referenced. Bit 12 identifies the module, logic 0 indicating the lower module and logic 1 the upper module. Bits 13 and 14 designate the core stack assembly, if more than one is installed.

3-111. Y-Line Selection. Figure 3-8 illustrates in block diagram form the selection of the Y-line for core stack assembly A400. The address decoding gates shown in the diagram receive bits 11 through 9 or 8 through 6 of the M-register. Each set of three bits results in an output pulse from one of the eight gates to which the bits are furnished. The Y0/1 signal is an enable pulse, and is always present when decoding takes place for memory module 0 or 1. These are the lower and upper modules in core stack assembly A400. For core stack assembly A401 (if used) the corresponding signal is Y2/3. These two signals determine which of the two Y driver/switch cards will be used, and thereby determine the core stack to be addressed.

3-112. As a result of the decoding process, a pulse is furnished to one of the eight drivers and another pulse to one of the eight switches. Thus, for each 2-digit octal number (MSD and LSD), one Y driver and one Y switch are selected. A total of 64 combinations is possible.

3-113. When the selected driver and selected switch each receive an input pulse, electron-current flows from the switch to the driver (when reading), or from the driver to the switch (when writing). This current flows through the addressed Y-line, which is numbered in accordance with the MSD and LSD which select it.

3-114. The Y-lines pass through the ring-shaped ferrite cores shown in figure 3-8. Each core in the illustration represents the 16 cores of a word location. It will be noted that every Y-line is shown passing through two cores, representing two 16-bit words. One of these words is in the upper module of the core stack assembly, and the other is in the lower module. The X-line (described later) passes through the same cores, and determines which of the two words will be read out. For one of the two words the X-line current aids the Y-line current, resulting in all cores being set to the zero state (if not already in that condition), causing readout of the word. For the second word, the

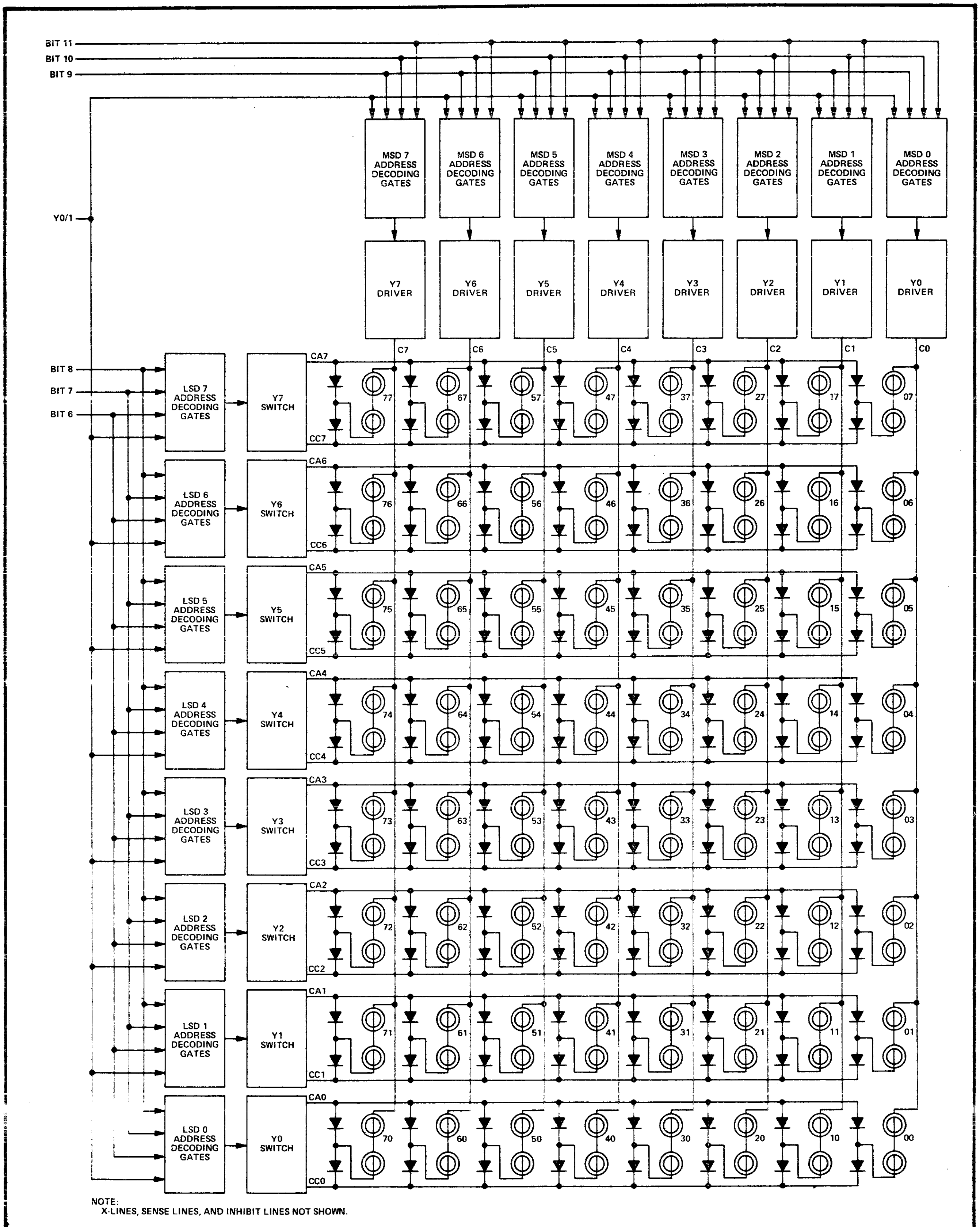

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Figure 3-8. Y-Line Selection Circuits, Core Stack A400, Block Diagram

X-line current opposes the Y-line current, preventing readout of the word. It is this technique which permits the use of an 8k core stack assembly, rather than a 4k stack.

3-115. In addition to the two 16-bit words indicated by each core in figure 3-8, each Y-line also passes through the ferrite cores for other words. Because the cores for these words are not traversed by the selected X-line, readout does not take place.

3-116. The diodes in figure 3-8 are in the diode matrix, on the core stack assembly. When reading, the bottom diode in each pair permits electron flow from the switch to the driver, and the top diode offers a high-resistance path to minimize current flow through it. When writing, the roles of the two diodes are reversed.

3-117. Each switch in figure 3-8 has two outputs. These are designated CC (common cathode) and CA (common anode) in accordance with the diode electrodes to which they connect. Each CC or CA designation is followed by the identifying number of associated switch, 7 through 0.

3-118. The drivers each have one output, identified by the letter C (core), followed by the identifying number of the driver.

3-119. It is important to note that the diode matrix shown in figure 3-8 does not represent a plane of the core stack assembly. The matrix in figure 3-8 has an 8 x 8 configuration, while the core-plane matrix is 64 x 64. Figure 3-9 shows a core-plane matrix, and indicates the manner in which the Y- and X-lines are connected. The numbered Y-lines in figures 3-8 and 3-9 correspond.

3-120. X-Line Selection. The X-line circuits for core stack assembly A400 are shown in figure 3-10. They differ from the Y-line circuits in the following respects:

a. The address decoding gates receive bits 5 through 3, or 2 through 0, of the M-register.

b. Instead of the Y0/1 enable pulse, either an X0 or an X1 pulse is furnished to each gate. (For core stack assembly A401, the corresponding signals are X2 and X3.)

c. For the cores in the upper module, X-line read or write current is in the reverse direction from that in the Y-lines.

3-121. As pointed out earlier, a reversed-current technique with the X-lines permits the selection of a word in either the lower or upper module, using only a single pair of X and Y drive lines. The current reversal is brought about by the X0 and X1 pulses. If bit 12 of the M-register is logic 0, indicating the lower module, the X0 pulse is furnished to the X address decoding gates. If bit 12 is logic 1, the X1 pulse if furnished.

3-122. Table 3-1 shows the direction of the current flow for all operating combinations.

3-123. LOGIC DIAGRAM ANALYSIS. Figure 3-11 is a logic diagram showing read and write operations at one address in the lower module and one address in the upper module. In addition to a portion of the basic core stack assembly, A400, portions of the following circuit cards are shown:

a. Driver/switch cards A14 and A15.

b. Inhibit driver cards A16 and A18.

c. Sense amplifier cards A12 and A13.

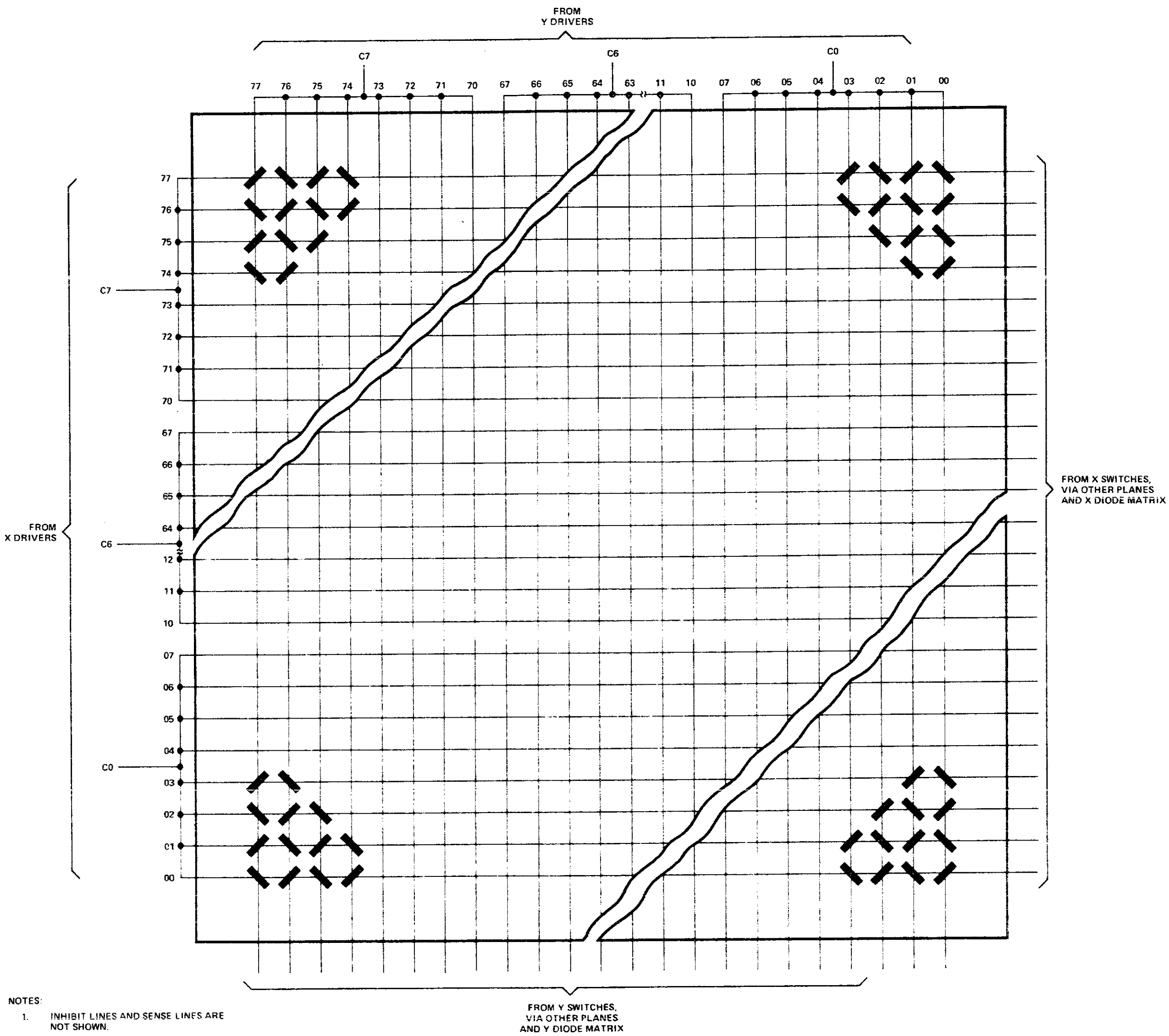
3-124. Of the two driver/switch cards, A14 is used for the Y-lines, and A15 for the X-lines. Inhibit driver card A18 provides inhibit current for the lower module in the core stack assembly, and A16 provides for the upper module. Sense amplifier card A13 is used with the lower module, and A12 with the upper module.

3-125. Lower Module Read Operation. The following paragraphs describe a typical memory readout operation, using address 05270 (octal). Figure 3-12 shows the timing relationships.

3-126. Bits M11 through M6 designate the Y-line to be used, and bits M5 through M0 identify the X-line. These bits are furnished to driver/switch cards A14 and A15 (figure 3-11) by direct memory logic card A20, which receives them from the M-register. The bits are furnished to the driver/switch card as soon as they are loaded into the M-register. This occurs at the end of T7TS of a phase 1, phase 2, or phase 3 machine cycle. During the last phase of the instruction, the M-register normally receives its contents from the P-register. The number has 1 added to it (2 for a program skip) before it is received by the M-register, and the number indicates the address of the next instruction to be performed. In the case of a program jump, the address is received from the T-register, rather than from the P-register.

3-127. If the M-register is loaded during phase 1 (fetch phase), the number received is one of the following:

a. The address of the next instruction (if the current instruction is a single-phase instruction).



NOTES:
1. INHIBIT LINES AND SENSE LINES ARE NOT SHOWN.
2. NOT ALL FERRITE CORES ARE SHOWN. A CORE IS SITUATED AT EACH INTERSECTION OF Y AND X DRIVE LINES.

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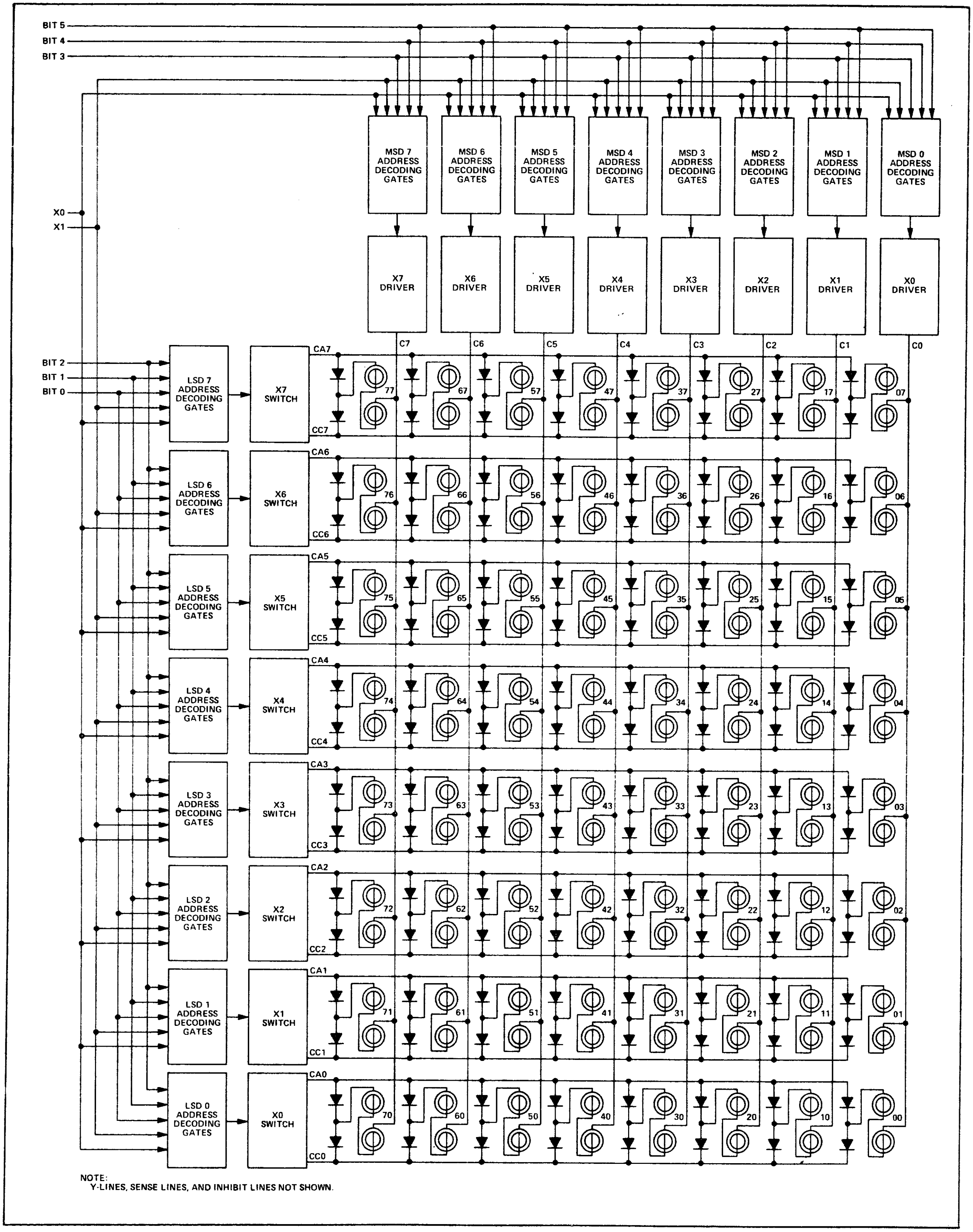
Figure 3-9. Core Plane Matrix



2019-183

Figure 3-10. X-Line Selection Circuits, Core Stack A400, Block Diagram

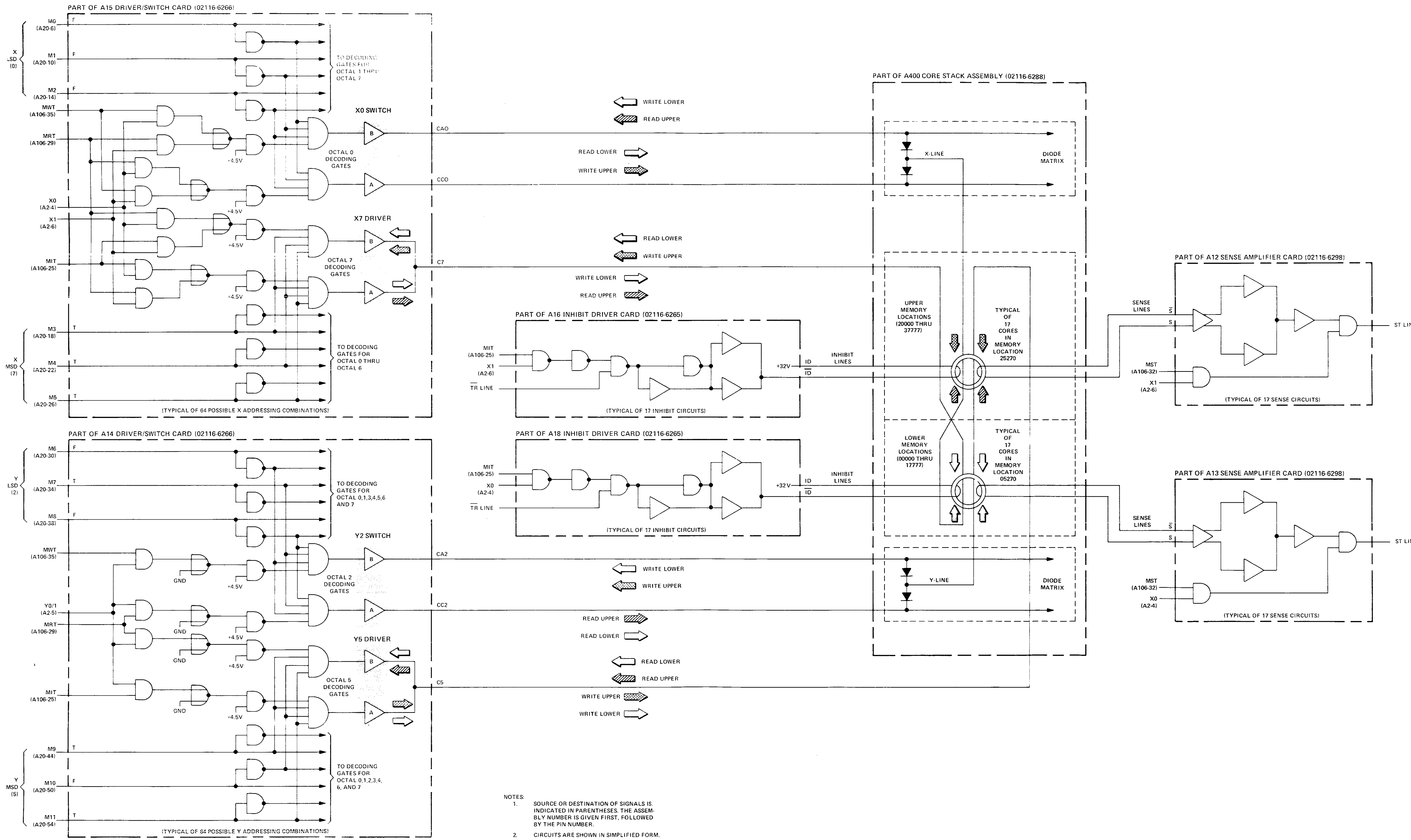


Figure 3-11. Memory Section, Partial Logic Diagram

Table 3-1. Electron Flow in Drivers and Switches

	Y-LINE ELECTRON FLOW		X-LINE ELECTRON FLOW	
MODULE	READ	WRITE	READ	WRITE
Lower	Switch to driver	Driver to switch	Switch to driver	Driver to switch
Upper	Switch to driver	Driver to switch	Driver to switch	Switch to driver

b. The address of an address word (if the next phase is indirect phase).

c. The address of an operand (if the next phase is execute phase).

3-128. If the M-register is loaded in phase 2 (indirect phase), the number received is the address of an address word (if the next phase will be another phase 2), or the number is the address of an operand (if the next phase will be execute phase).

3-129. The 12 low-order M-register bits are furnished to the X and Y address decoding gates on the driver/switch cards. The Y0/1 and X0 signals, also forwarded to these gates, become true at the end of T7TS. These last two signals are a result of decoding M-register bits 14, 13, and 12 by memory module decoder card A2, and the signals designate the lower module of core stack assembly A400. (In the present example, bits 14, 13, and 12 are 000.)

3-130. At T0TS the X and Y address decoding gates are strobed by the MRT signal from the memory timing circuits. As a result, the following switches and drivers receive true inputs: Y driver 5B, Y switch 2A, X driver 7B, X switch 0A. Electron flow then takes place in the Y-lines and X-lines in the direction indicated by the "read lower" arrows in figure 3-11.

3-131. The simultaneous flow of current in the Y-lines and X-lines results in 16 ferrite cores experiencing full readout current. These cores are in the lower module. In the upper module, the cores at the corresponding address (octal 10000 greater) experience opposing Y and X currents, and no readout takes place. Additional cores in each module are also traversed by the selected Y-line and X-line. These experience only half the required readout current. This is insufficient to set the cores to the logic 0 state, and no readout takes place.

3-132. At the addressed location, cores in the logic 1 state are transferred to logic 0. The sense line running through each of these cores generates a voltage, which is forwarded to one of the 16 sense amplifiers. If a core contained logic 0 before being read out, no voltage is generated.

3-133. Each sense line crosses the core plane diagonally, reversing direction when it emerges from the plane, to cross again in the opposite direction. Because of this method of wiring the core plane, the sense line in some cases passes through a core in one direction, and in other cases in the opposite direction. As a result, the voltage between the two ends of the sense winding could be of either polarity, depending on the direction in which the core is traversed. In other words, the ends of the sense line which are positive and negative depend on the address being read out.

3-134. For each module, 16 sense amplifiers are used, one amplifier for each bit read out. If the bit read is logic 1, the sense amplifier furnishes a true signal to the sense amplifier output gate. (See figure 3-11.)

3-135. At T2, the pulse from each conducting sense amplifier is gated into the T-register. The MST pulse accomplishes this gating, using the X0 pulse as an enable. The sense amplifiers for the upper module remain cut off at this time because no cores in the upper module experience full readout current. Since these amplifiers indicate logic 0's, their outputs must not be gated into the T-register. The X1 pulse, indicating the upper module, remains false when the lower module is being read, accomplishing the desired purpose by disabling the output gates for the upper-module sense amplifiers.

3-136. The T-register, formerly cleared at T0TS by the RST pulse, receives the logic 1's from the lower-module sense amplifiers, and the appropriate positions of the register are set. Register positions corresponding to sense amplifiers not yielding a logic 1 remain in the reset state.

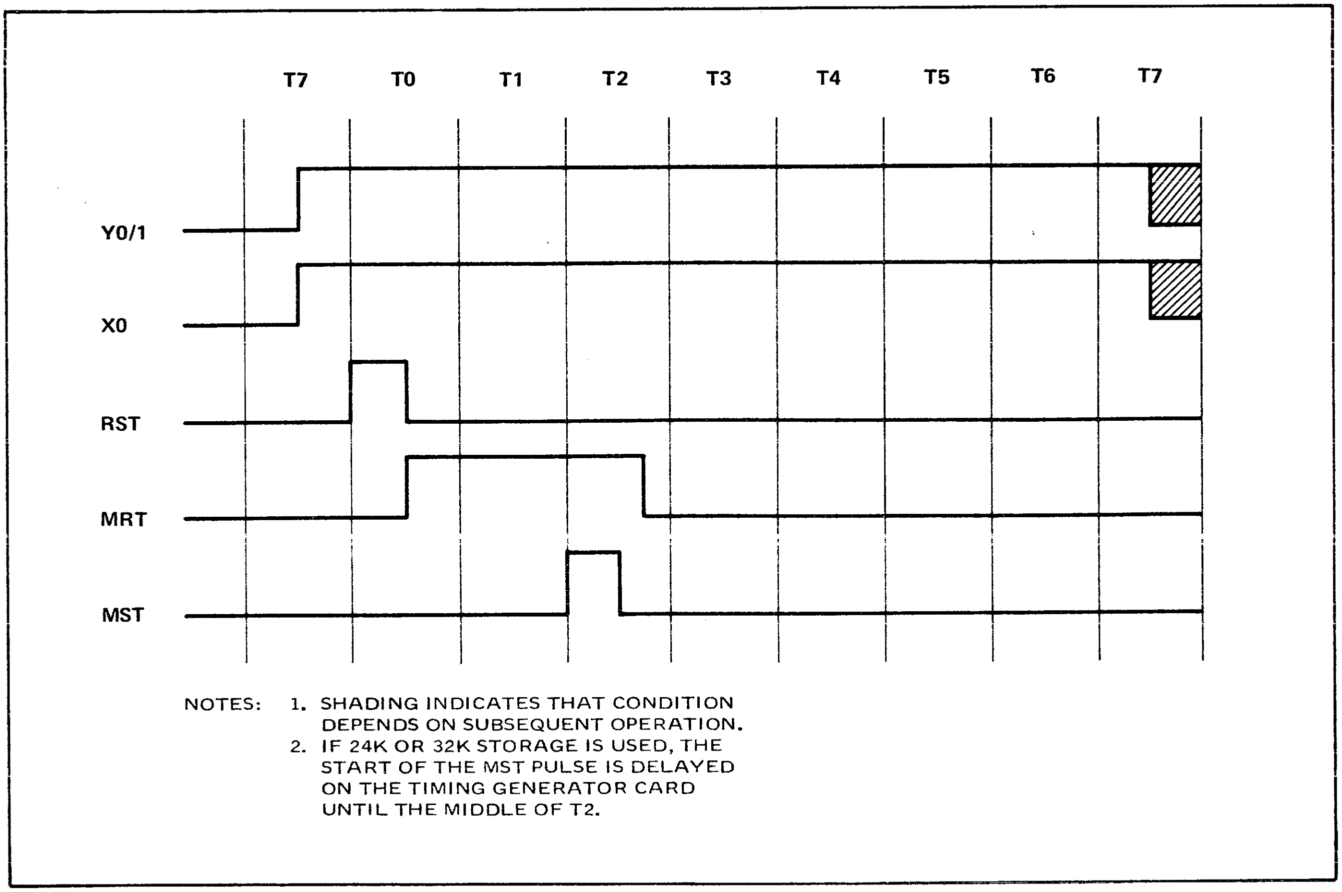


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Figure 3-12. Memory Readout, Timing Diagram

3-137. Subsequent use made of the word in the T-register depends on whether it is an instruction word, address word, or operand word, as explained earlier.

3-138. Lower Module Write Operation. The following paragraphs describe a typical memory write operation, using address 05270 (octal). Figure 3-13 shows the timing relationships.

3-139. When a memory write operation is performed, the word to be written is in the T-register. This word can either be one that has just been read from the memory section, or it can be a new word which is to be stored. In either case, the machine cycle in which writing takes place begins by reading out a word from the addressed location. This word is either discarded, or placed in the T-register. The readout operation clears all ferrite cores at the addressed location to logic 0. When writing is performed, cores in which logic 1 is to be stored are set by a current pulse in the Y-line and X-line. For each core that is to store logic 0, current flow in an inhibit line produces a magnetic field opposing the field created by the Y-line and X-line. The cores traversed by the activated inhibit lines therefore remain in the logic 0 state acquired during readout.

3-140. Starting in the last half of T3, the memory timing circuits provide an MIT pulse to the inhibit driver cards (figure 3-11). Inhibit driver card A18, used for the lower module, also receives a true X0 input. Of the 16 inhibit drivers on this card, some receive a logic 1 from the T-register, and the others receive a logic 0. (These bits are furnished on the TR lines.) If an inhibit driver receives logic 0, current flows in the corresponding inhibit line for the duration of the MIT pulse.

3-141. As well as being supplied to the inhibit driver cards, the MIT pulse is furnished to driver/switch cards A14 and A15. The memory address used during readout continues to be supplied to the address decoding gates on these cards. Consequently, application of the MIT pulse results in selection of the previously addressed driver. Note, however,

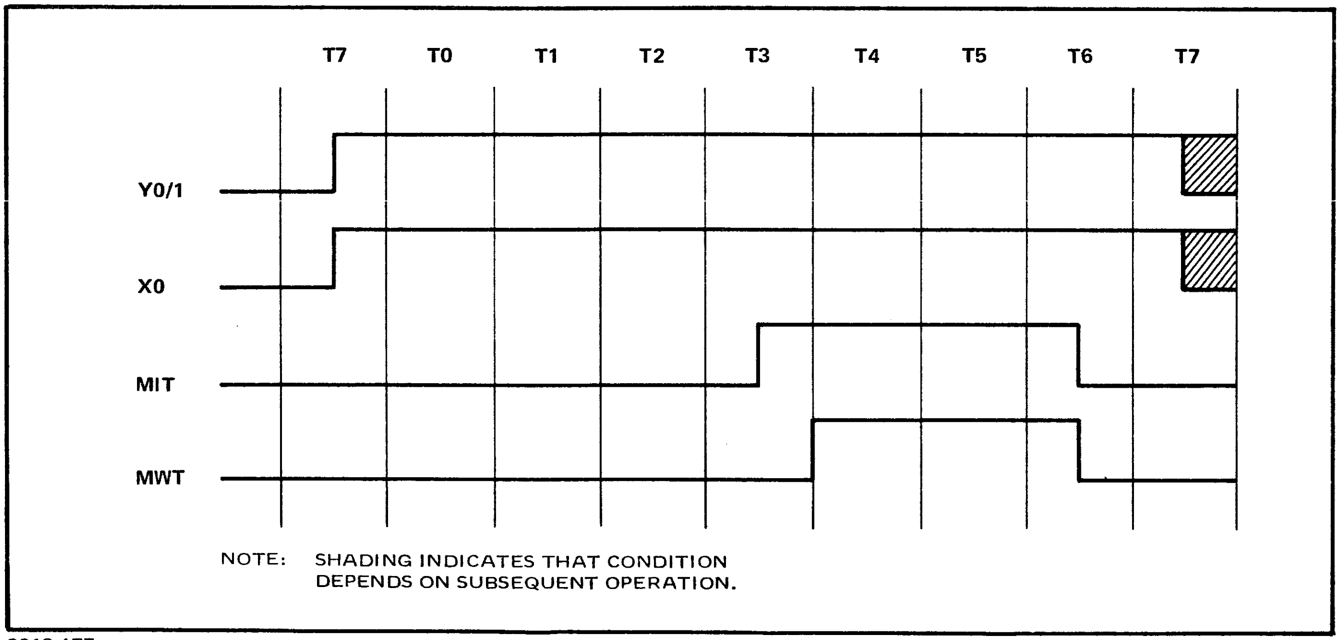

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Figure 3-13. Memory Write, Timing Diagram

that of each pair of amplifiers in the driver, the opposite one is selected from that used for reading. As a result, current will flow in the opposite direction through the Y-line and X-line than was the case with reading.

3-142. After selection of the Y and X drivers, operations await the selection of a Y and X switch. This occurs at T4, when the memory timing circuits provide the MWT signal to the two driver/switch cards. Here, as with the driver, the same switch is selected as was the case with reading, but the opposite amplifier of each pair is used.

3-143. Current now flows in the Y-line and X-line for the duration of the MWT pulse. This current flow is in the opposite direction from that used for reading, and the cores of the selected word are set to the logic 1 state if they do not receive inhibit current.

3-144. Upper Module Read and Write Operations. Reading and writing in the upper module of the core stack assembly are similar to the corresponding operations in the lower module. However, because M-register bit 12 is logic 1, the X1 signal is furnished in place of the X0 signal. As a result, the X drivers and switches selected for reading or writing are the opposite ones in each pair from those used in lower module operations. Consequently, the X-line current flows in the opposite direction. The Y-line current remains unchanged.

3-145. SCHEMATIC DIAGRAM ANALYSIS. In the explanation which follows, table 3-2 identifies the reference designations of memory cards for various addresses.

3-146. Memory Module Decoder. Memory module decoder card A2 decodes bits 12 through 14 of the M-register to determine the core stack assembly to be used (if more than one is installed), and to determine whether the upper or lower module will be referenced. An additional function of the card is to prevent memory readout for locations which are protected by the LOADER switch. The schematic diagram for A2 card is in section V.

3-147. In the basic computer configuration, a single core stack assembly is installed. The memory module decoder card furnishes the Y0/1, X0, and X1 signals required for reading or writing in this stack. The signals are decoded by "and" gates MC15A, MC35A, and MC35C. The remaining gates in this group are used only when additional storage capacity is installed.

3-148. The large gates at the bottom of the schematic diagram are used for memory protection. Gate MC27 experiences coincidence when the upper module of the basic core stack assembly is addressed. Gate MC77 then experiences coincidence if the LOADER switch is at the PROTECTED position and M-register bits 11 through 6 are all logic 1. Figure 3-7 shows that the high-order octal digits of the address are then 177. When these conditions exist, the "not" MPT signal becomes false and no reading or writing can take place in addresses 17700 through 17777.

3-149. Gate MC37 is used for memory protection when two core stacks are installed. In this situation, gate MC27 is disabled by the false input to pin 1. If a memory extender is used, gate MC47 is used if it has a single stack, MC57 if it has two stacks.

3-150. Driver/Switches. In the basic computer configuration, two driver/switch cards are used. One has reference designation A14, and is used for the Y-lines. The other is A15, and is used for the X-lines. If a second core stack

Table 3-2. Memory Card Assignments

STACK AND MODULE	ADDRESS RANGE (OCTAL)	DRIVER/SWITCH CARD	SENSE AMPLIFIER CARD	INHIBIT DRIVER CARD
A400 lower	00000-07777	A14 (Y drive) A15 (X drive)	A13	A18
A400 upper	10000-17777	A14 (Y drive) A15 (X drive)	A12	A16
A401 lower	20000-27777	A8 (Y drive) A9 (X drive)	A11	A6
A401 upper	30000-37777	A8 (Y drive) A9 (X drive)	A10	A4

assembly is installed, two additional cards, A8 and A9, serve the Y-lines and X-lines, respectively, in the second stack. All four cards are identical, and have the same part number (02116-6266).

3-151. Each card has eight drivers and eight switches. These correspond to the drivers and switches shown in figure 3-8 and 3-10. Each card also has two address decoding gates for every driver (one gate for reading and one for writing), and two decoding gates for every switch (again, one for reading and one for writing).

3-152. Figure 3-14 shows one of the drivers, one of the switches, and their associated address decoding gates. Also shown is part of the core stack assembly. Transistors Q33, Q32, Q31, Q35, and Q34, and the components immediately associated with them, constitute the switch. Transistors Q58, Q57, Q56, and the associated components, are the driver. The driver and switch shown in figure 3-14 correspond, respectively, to MSD 5 and LSD 6.

3-153. "Nand" gates MC106A and MC106B are the address decoding gates for the driver. They are enabled when the X or Y MSD is 5. For the driver/switch card used with the Y-line, MC106B is used when reading, and MC106A when writing. This use of different gates is necessary because current must flow through the driver in opposite directions for the read and write operations, and the gates serve to establish the direction of current flow.

3-154. When the lower module is addressed, the gates on the driver/switch card for the X-line function in the same manner as the gates on the Y-line card. However, when the upper module is referenced, MC106A and MC106B reverse their functions. That is, MC106A is used when reading, and MC106B when writing. As a result, current in the X-line flows in the opposite direction from that used when addressing the lower module.

3-155. The address decoding gates for drivers not shown in figure 3-14 function in the same manner as MC106A and MC106B, but each pair of gates is associated with a different MSD.

3-156. Turning now to the address decoding gates for the switches, figure 3-14 shows that these are MC56A and MC56B if the LSD is 6. On the Y-line driver/switch card, MC56B is used when reading, MC56A when writing. These functions are the same for the X-line card when the lower module is referenced, but are reversed for the upper module.

3-157. Tables 3-3 and 3-4 list the address decoding gates used for the various memory addresses. It will be noted that the data in the body of the two tables is identical. The difference between the tables is in the column headings, and for operations in the lower module even the column headings are essentially identical.

3-158. Examining, now, the driver circuits, in the driver shown in figure 3-14 current flow takes place either through transistor Q56 or transistor Q57 when reading or writing is conducted. If the read or write operation is initiated by "nand" gate MC106A, Q56 conducts. If MC106B initiates the operations, Q57 conducts. In the first case, the output pulse from the "nand" gate is coupled across transformer T11, and the resulting negative pulse at the base of Q56 causes current flow in the Y-line or X-line when the switch at the other end of the line is activated. When transistor Q57 is used, the pulse from the "nand" gate MC106B is first amplified by Q58. The circuits of the remaining drivers on the card are identical with the driver shown in figure 3-14.

3-159. In the switch circuit in figure 3-14, parallel transistors Q34 and Q35 conduct when Q57 in the driver circuit conducts. Transistor Q31 in the switch conducts when Q56 in the driver conducts.

Table 3-3. Address Decoding Gates for Y-lines

Y MSD	ADDRESS DECODING GATE*		Y LSD	ADDRESS DECODING GATE*	
	READ	WRITE		READ	WRITE
7	MC126B	MC126A	7	MC66B	MC66A
6	MC116B	MC116A	6	MC56B	MC56A
5	MC106B	MC106A	5	MC46B	MC46A
4	MC107B	MC107A	4	MC47B	MC47A
3	MC97B	MC97A	3	MC37B	MC37A
2	MC96B	MC96A	2	MC36B	MC36A
1	MC86B	MC86A	1	MC26B	MC26A
0	MC76B	MC76A	0	MC16B	MC16A

NOTE:
*Reference designation prefix is A14 for octal addresses 00000 through 17777, A8 for 20000 through 37777.

Table 3-4. Address Decoding Gates for X-lines

X MSD	ADDRESS DECODING GATE*		X LSD	ADDRESS DECODING GATE*	
	READ LOWER, WRITE UPPER	WRITE LOWER, READ UPPER		READ LOWER, WRITE UPPER	WRITE LOWER, READ UPPER
7	MC126B	MC126A	7	MC66B	MC66A
6	MC116B	MC116A	6	MC56B	MC56A
5	MC106B	MC106A	5	MC46B	MC46A
4	MC107B	MC107A	4	MC47B	MC47A
3	MC97B	MC97A	3	MC37B	MC37A
2	MC96B	MC96A	2	MC36B	MC36A
1	MC86B	MC86A	1	MC26B	MC26A
0	MC76B	MC76A	0	MC16B	MC16A

NOTES:
"Lower" and "upper" refer to the lower and upper modules in the core stack assembly.
*Reference designation prefix is A15 for octal addresses 00000 through 17777, A9 for 20000 through 37777.

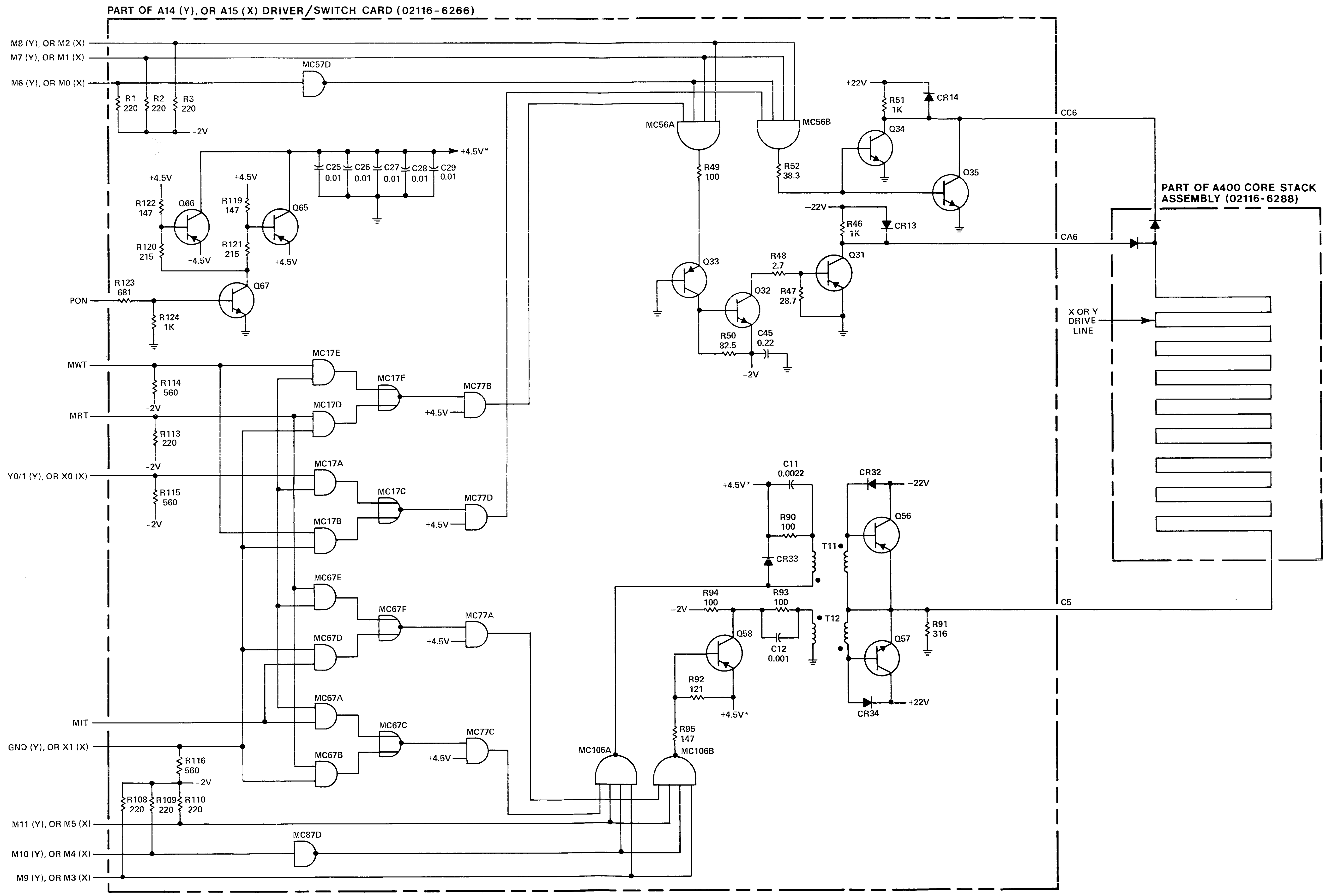

Figure 3-14. Driver and Switch, Schematic Diagram

3-160. Included on each driver/switch card is a circuit which prevents memory reading or writing during power turn-on. Random computer conditions during power sequencing thus are unable to cause destruction of data in the core stack assembly. The circuit is included in figure 3-14, and consists of transistors Q65, Q66, and Q67, and their associated components. When the PON signal is present, the +4.5V* voltage is available, and is furnished as an operating voltage to the address decoding gates for all drivers on the card. During power turn-on PON is false and the +4.5V* voltage becomes zero volts. Under this condition the driver gates do not function, and no driver can be activated. The PON signal does not protect stored data during power shut down because it remains true for about 8 ms after removal of ac line voltage. The regulated dc voltages, on the other hand, may start to shut down in as little as 1 ms. For this reason the program should always be stopped before power is turned off.

3-161. The PON signal is applied to the base of transistor Q67, which functions as a driver for Q66 and Q65. When the PON signal is true, Q66 and Q65 in parallel permit current to flow to +4.5 volts. When PON becomes false, Q67 cuts off. Transistors Q66 and Q65 cut off in turn, and the core stack assembly can no longer receive Y-line or X-line current. Because the bases of Q66 and Q65 are returned to +4.5 volts, these transistors cut off very rapidly when Q67 ceases conduction.

3-162. <u>Sense Amplifiers</u>. In the basic computer configuration, two sense amplifier cards are used. Their reference designations are A13 and A12. Card A13 is used with the lower memory module, and A12 is used with the upper module. If a second core stack assembly is installed, two more sense amplifier cards, A11 and A10, are used. Card A11 is for the lower module of core stack A401, and A10 is for the upper module. All four cards are alike.

3-163. Installed on each card are 17 sense amplifiers. The circuits are identical, therefore only one will be described. Figure 3-15 is a schematic diagram of the sense amplifier used with the low-order bit read from the core stack assembly.

3-164. The purpose of the sense amplifier is to detect and amplify the voltage induced on a sense line when a ferrite core containing logic 1 is read out. This voltage is at least 35 mV. If the core contains logic 0, the voltage induced in the sense line will be less than 9 mV.

3-165. As noted earlier, the voltage induced in the sense line can be of either polarity, depending on the direction in which the sense line passes through the ferrite core being read.

3-166. The sense amplifier consists of a differential preamplifier, followed by a 2-transistor dual amplifier, succeeded by an emitter-follower output stage. When readout of a logic 1 occurs, half the sense line voltage appears across resistor R7 and half across R6. These two voltages are applied to the two inputs of MC1, the differential preamplifier. Pin 8 or pin 6 of MC1 furnishes a negative-going pulse to the base of transistor Q1 or Q2. Normally, these transistors are in the cutoff condition. Assuming Q1 receives the negative input, it conducts, and applies a positive-going pulse to Q3. As a result, emitter-follower Q3 furnishes a positive pulse to MC17A. This pulse has a duration of about 200 ns.

3-167. The MST pulse gates the logic 1 from the sense amplifier into the T-register.

3-168. Included on each sense amplifier card is transistor Q164 and its associated components. This transistor serves to establish the bias current for the 17 integrated-circuit preamplifiers on the card.

3-169. <u>Inhibit Drivers</u>. In the basic computer configuration, two inhibit driver cards are used. One, with reference designation A18, is employed with the lower module of A400, the basic core stack assembly. The second, A16, is used with the upper module.

3-170. If a second core stack assembly (A401) is installed in the computer, two additional inhibit drivers cards are used. These have reference designations A6 and A4. Card A6 is used with the lower module A401, and card A4 is used with the upper module.

3-171. Each card contains 17 inhibit drivers. Since the circuits of all are identical, only one will be described. Figure 3-16 is a schematic diagram of the inhibit driver used for the low-order bit of the word being written.

3-172. The function of the inhibit driver is to prevent setting the applicable ferrite core to logic 1 if bit 0 of the T-register is logic 0. This is done by producing a current in the inhibit winding of the appropriate plane in the core stack. The magnetic field associated with the current opposes the magnetic field produced by the Y-line and X-line, thereby preventing a change in the state of the ferrite core. The inhibit current flows when the MIT pulse is true.

3-173. The MIT pulse is gated with the X0, X1, X2, or X3 signal, in accordance with the inhibit driver card in use. By this means, inhibit current is allowed to flow only in the memory module being written in. The signals are associated with the following modules:

a. X0 is true when writing in the lower module of A400.

b. X1 is true when writing in the upper module of A400.

c. X2 is true when writing in the lower module of A401.

d. X3 is true when writing in the upper module of A401.

3-174. The gated MIT pulse passes through "nand" gate MC17A if T-register position 0 contains logic 0. The false

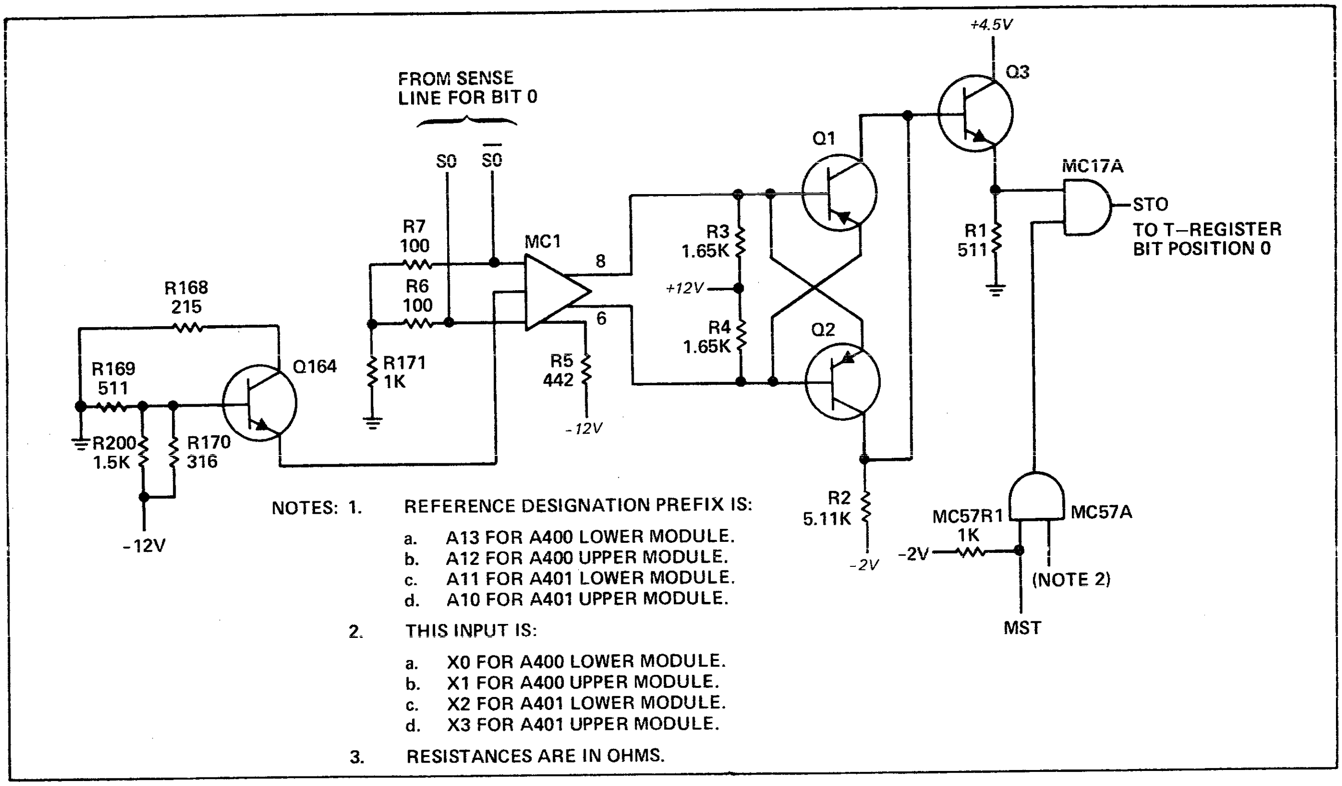

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Figure 3-15. Sense Amplifier, Schematic Diagram

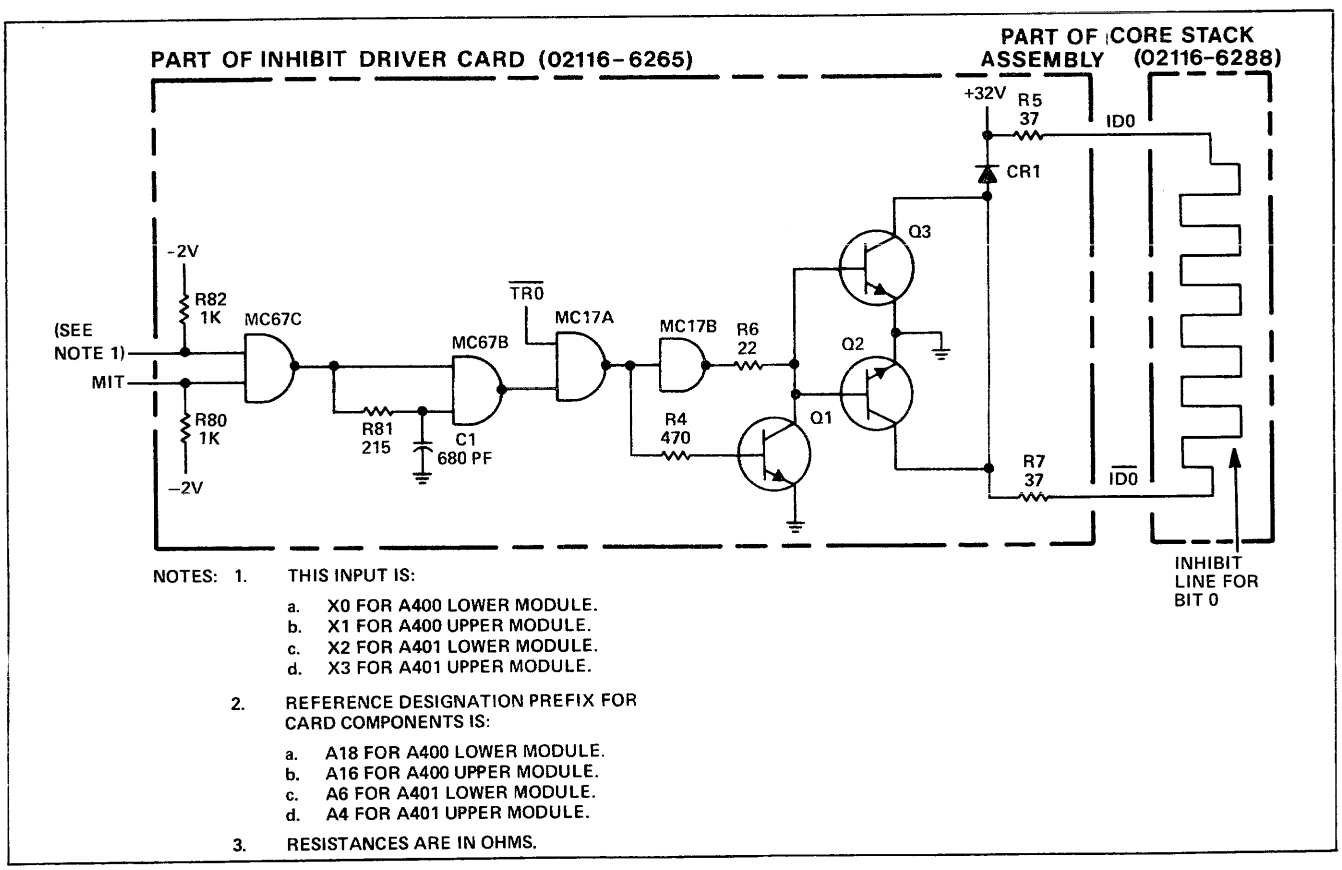

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Figure 3-16. Inhibit Driver, Schematic Diagram output of the "nand" gate is inverted and applied to the base of parallel transistors Q2 and Q3. Transistor Q1 serves as a speed-up transistor. When NPN transistors Q2 and Q3 conduct, inhibit current flows through the inhibit line to the +32 volt source.

3-175. At the end of the MIT pulse, transistors Q2 and Q3 return to the cutoff state. Diode CR1 provides a path to maintain current flow as the magnetic field around the inhibit line collapses. This protects transistors Q2 and Q3 against excessive voltage induced by the collapsing field.

3-176. INPUT/OUTPUT SECTION.

3-177. The circuit theory of the input/output section is presented in Volume III, Input/Output System Operation Manual for the Model 2116B Computer. Additional information is given in the Operating and Service Manuals and Interface Kit Manuals for I/O devices used by the computer. A further source of information is: A Pocket Guide to Interfacing Hewlett-Packard Computers, (part no. 5950-8718).

3-178. POWER SUPPLY SECTION.

3-179. The power supply section of the 2116B computer provides the regulated and unregulated dc voltages required by the computer. Protective circuits are included, which remove dc power from the computer in the event of excessive heat in the computer cabinet, low ac line-voltage, excessively high dc voltage, or excessive dc current.

3-180. Optional devices which install in the computer cabinet receive their operating voltages from the 2116B power supply section. If these optional features require more power than the power supply section is capable of furnishing, an auxiliary power source (referred to as a power supply extender), installed in a separate cabinet, provides additional dc power. The externally-furnished voltages connect in parallel with the corresponding dc voltages produced in the 2116B power supply.

3-181. All optional devices which are not within the 2116B computer cabinet provide their own operating voltages, derived from a separate connection to the ac power line.

3-182. The power supply section furnishes the following dc voltages to other sections of the computer:

a. -2 volts regulated.

b. +4.5 volts regulated.

c. +7 volts unregulated.

d. +12 volts regulated.

e. -12 volts regulated.

f. +22 volts regulated.

g. -22 volts regulated.

h. +32 volts regulated.

i. +35.5 volts unregulated.

3-183. Additional dc voltages are produced for use within the power supply section itself.

3-184. AC DISTRIBUTION.

3-185. The distribution of ac power in the computer is shown in figure 3-17. All components shown in the illustration are in the power supply section, with the exception of POWER switch A502S109 and fans A200B1, A200B2, and A200B3. The POWER switch is on control panel assembly A502, and the fans are at the bottom of the card cage.

3-186. The ac operating power for the computer, single-phase 115 or 230 volts, is furnished to connector A300J1 (figure 3-17). POWER switch A502S109 applies or removes this power from the power supply section. The switch is of the push-on, push-off type. One push is required to close the switch, a second to open it.

3-187. When the POWER switch is pressed on, ac power is applied through resistor A300R1 to transformer A311T1 and to the six fans in the computer cabinet. The transformer furnishes low-voltage ac to all power supplies. Resistor A300R1 reduces the initial ac line current as power supply filter capacitors acquire a charge. (The power supplies use solid-state rectifiers, which require no warmup time.)

3-188. When the filter capacitors become substantially charged, relay A312K1 energizes and resistor A300R1 is shorted out. Full ac voltage is then applied to transformer A311T1, and power control circuits make dc voltages available to the computer in a predetermined sequence.

3-189. DC POWER CONTROL.

3-190. Figure 3-18 shows the manner in which dc power is applied to and removed from the computer.

3-191. As noted earlier, when the POWER switch is closed ac voltage is furnished to the computer power transformer. Figure 3-18 shows that other contacts of the switch connect the coil of relay A312K1 to the unregulated +4.5 volt source. When the filter capacitors for +4.5 volts and -5.6 volts become substantially charged, relay A312K1 energizes and full ac line voltage is applied to the power transformer. Also, contacts 2 and 1 of A312K1 furnish +4.5 volts through normally-closed thermal switches to power fail card A1. Circuits on this card produce a true PSO signal, which is forwarded to logic supply regulator card A301. This card, together with memory supply regulator card A302, controls the application of the seven regulated voltages to the computer.

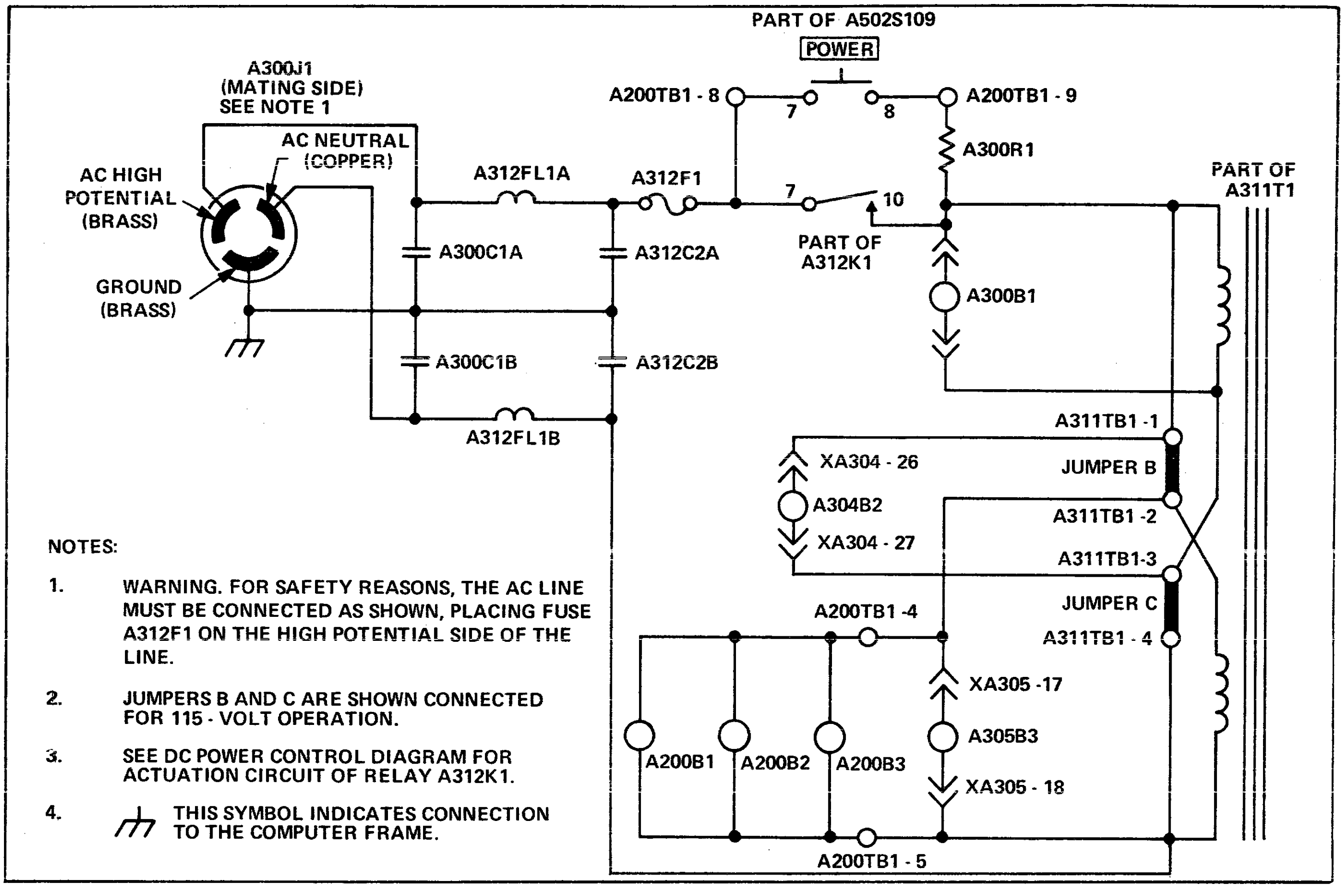

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Figure 3-17. AC Distribution, Wiring Diagram

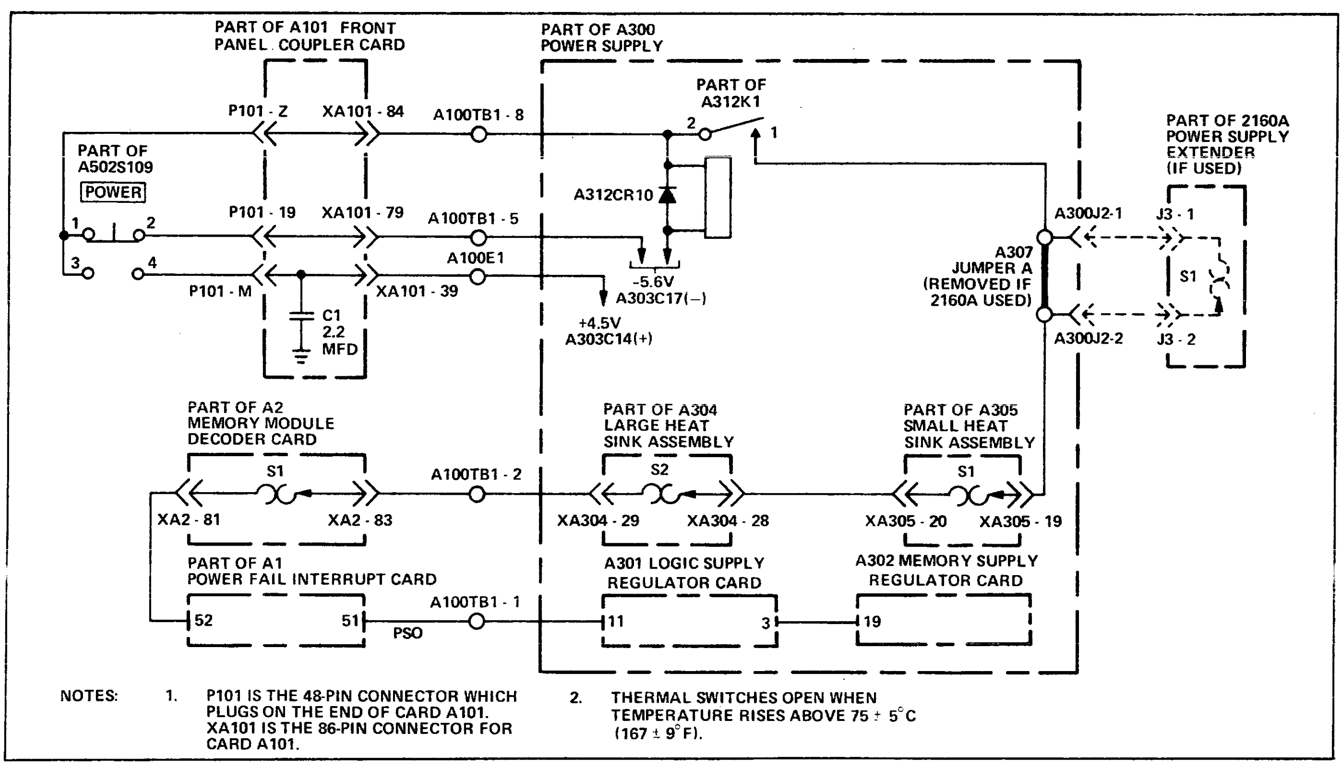

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Figure 3-18. DC Power Control, Wiring Diagram

3-192. Regulated -2 volts is furnished to the computer when filter capacitors charge sufficiently to allow the -2 volt voltage regulator to function. The dc power control circuits then furnish the computer with the remaining six regulated voltages. These are supplied in a predetermined sequence. Then; if all thermal switches shown in figure 3-18 are closed, the computer is ready for use. The computer is in the halted condition, and the following indicators are lighted: POWER, PRESET, HALT, and FETCH. Register display lamps on display board assembly A501 are lighted or off in a random pattern.

3-193. If one or more thermal switches are open during the power-on sequence, or if any of the regulated voltages is not furnished, the dc shut-down sequence is initiated. Shut-down starts about 300 ms after regulated +4.5 volts is first made available. If unregulated +4.5 or -5.6 volts is not furnished, the dc power-on sequence does not start and relay A312K1 remains de-energized.

3-194. When the POWER switch is pressed to turn off the computer, unregulated +4.5 volts is removed from the coil of A312K1. However, diode A312CR10 provides a path for the current induced in the relay coil by its own collapsing magnetic field, holding the relay energized a short time longer. The diode also eliminates arcing at contacts 3 and 4 of the POWER switch, and prevents the application of voltage spikes to power fail card A1. When POWER switch contacts 3 and 4 open, +4.5 volts is immediately removed from pin 52 of power fail card A1. The PSO signal becomes false about 8 ms later, and the power control circuits remove dc voltages from the computer in a predetermined sequence. As well as furnishing a false PSO signal, card A1 also generates a power-fail program interrupt, and if programmed to do so the computer stores register contents and performs other actions in preparation for later startup. The 8 ms delay in producing the PSO signal is the time available for the power-fail program. During this time voltage regulators are able to maintain dc levels despite the falling voltage from filter capacitors. As a nominal and conservative figure, at least 200 instructions can be performed in this time.

3-195. In the event of complete loss of ac line-voltage, or if the line voltage drops below 100 to 102 volts rms (200 to 204 volts for a 230-volt computer), power fail interrupt card A1 generates a power-fail interrupt. Then, when filter capacitors have discharged to the extent that one of the voltage regulators can no longer maintain the required voltage level, the dc shut-down sequence is performed. When the line voltage returns to normal dc voltages are again supplied, but the computer is halted.

3-196. Thermal switches A305S1, A304S2, and A2S1 in figure 3-18 remove dc power from the computer in the event of overheating during operation. When overheating occurs, one of the thermal switches opens, +4.5 volts is removed from card A1, and a power-fail interrupt occurs. Eight milliseconds later the PSO signal becomes false, and the dc shut-down sequence is initiated. In this case, relay A312K1 remains energized, ac distribution in the computer remains unchanged (figure 3-17), and the fans in the computer cabinet maintain their cooling function. When the thermal switch closes the normal dc power-on sequence is performed, but the computer is halted.

3-197. In addition to low line voltage and overheating, a third fault can cause dc power shut-down. If one of the dc regulated voltages fails, partial or complete shut-down of the remaining regulated voltages takes place.

3-198. Specific information on the dc turn-on and shut-down sequence is presented later in this section.

3-199. +7 VOLT POWER SUPPLY.

3-200. The +7 volt power supply is a full-wave bridge rectifier, furnishing unregulated and unfiltered dc power. The circuit is shown in the A300 power supply schematic in section V. This voltage is used for lighting all lamps on display panel assembly A501 and control panel assembly A502, with the exception of the POWER indicator. No other use is made of the +7 volt power.

3-201. +4.5 VOLT AND -2 VOLT POWER SUPPLIES.

3-202. The +4.5 volt and -2 volt power supplies furnish the operating voltages required by the logic circuits in the computer. (Logic elements on power fail interrupt card A1 and certain I/O interface cards require +12 volts as well.) A block diagram of the +4.5 and -2 volt power supplies is presented in figure 3-19. The diagram is simplified to the extent that the +4.5 volt and -2 volt power sources are shown as independent units, whereas in actuality they both derive their power from a single tapped secondary on the power transformer. Unregulated voltages shown in figure 3-19 are approximate, and will vary in accordance with component differences, the amount of current required for optional devices, and power-line voltage variations.

3-203. The +4.5 volt power source and the +4.5 volt regulator make up the +4.5 volt power supply. The power source provides approximately 7.9 volts unregulated dc. Of this, 3.4 volts is dropped across the +4.5 volt regulator, leaving regulated +4.5 volts across Ra, the computer circuits which use this voltage. These circuits are situated on cards in the card cage.

3-204. The -2 volt source and the -2 volt regulator make up the -2 volt power supply. The power source provides approximately 10.1 volts unregulated dc. Of this, 3.6 volts is dropped across the regulator. The resulting 6.5 volts is applied across Rb, which represents the load imposed by the CTL logic circuits in the card cage. Although it furnishes 6.5 volts, the output of the regulator is at a potential of -2 volts with respect to ground; therefore the regulator and its power source are referred to as the -2 volt regulator and -2 volt power source. As well as being applied to Rb, the output of the -2 volt regulator is furnished to Rc, which represents the pull-down resistors in the card cage. In some cases these resistors are discrete components, and in other instances they form part of integrated circuits in micropacks. Also to be considered as part of Rc are paths from -2 volts to ground within the power supply section itself. These paths to ground in the power supply result in a current of 0.5 to 0.75 amp.

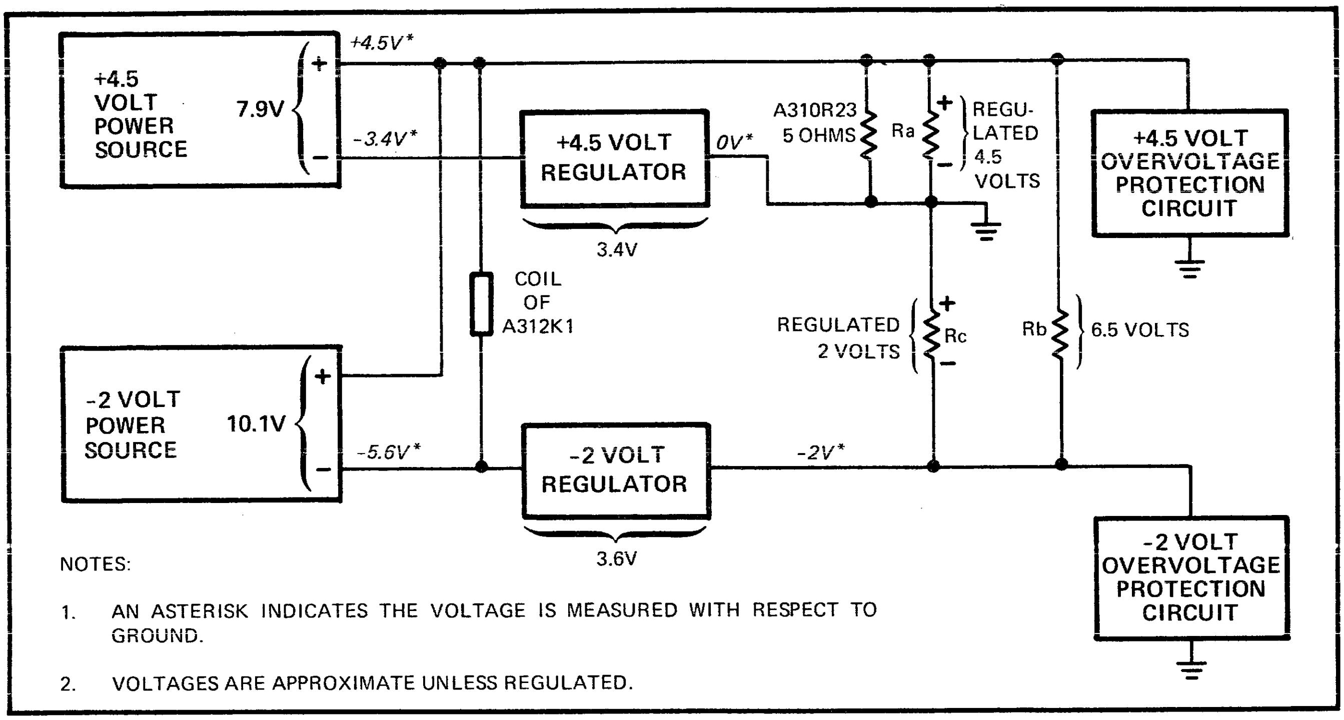

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Figure 3-19. +4.5 Volt and -2 Volt Power Supplies, Simplified Block Diagram

3-205. The +4.5 and -2 volt regulators can each furnish a maximum current of 22.5 amps. In figure 3-19 it will be noted that the +4.5 volt regulator is between the power source and ground, rather than in the more usual position between the power source and the high potential end of the load. The reason for this is that the top end of Ra and Rb are electrically common, and if the +4.5 volt regulator were in the common return of Ra and Rb to the power sources, the +4.5 volt regulator would be required to handle up to 45 amps. Also, the +4.5 volt regulator would not be able to control the +4.5 volt output without affecting the output of the -2 volt regulator. Another reacting element between the two power supplies is the common current which flows through Rc and Ra. Both Rc and Ra may include circuits on optional cards. If Rc becomes sufficiently small in resistance because of added cards, the current through Rc will exceed the normal current through Ra. Current then ceases to flow through the +4.5 volt regulator, and excessive current flows through Ra. As a result, the voltage across Ra rises above 4.5 volts. To prevent difficulty from this effect, resistor A310R23 is installed in the power supply. This resistor draws current from the +4.5 volt power supply in addition to that drawn by Ra, and as a result the current through Rc will not exceed that through Ra and A310R23.

3-206. Included in figure 3-19 is the coil of A312K1. The bottom end of this coil connects to the negative terminal of the -2 volt source, which has a potential of -5.6 volts with respect to ground. The top end of the coil connects to +4.5 volts. The potential across the coil is therefore about 10.1 volts.

3-207. The overvoltage protection circuits for the +4.5 and -2 volt power supplies prevent damage to components due to excessively high output voltage from the power supply. If, because of a fault in the voltage regulator, the power supply output voltage rises, the overvoltage protection circuit permits heavy current to flow. The excessive current causes current limiting in the voltage regulator, and the voltage is no longer applied to the computer load. If the defect in the voltage regulator prevents current limiting, the power supply fuse blows, again removing dc voltage from the load circuits.

3-208. SCHEMATIC-DIAGRAM ANALYSIS OF +4.5 AND -2 VOLT POWER SOURCES. Figure 3-20 is a schematic diagram of the +4.5 volt and -2 volt power sources. Included in the diagram is a portion of the regulator for each of these two voltages.

3-209. Both power sources use a single tapped secondary winding of transformer A311T1. The +4.5 volt power source consists of the center portion of the winding, diodes CR1 and CR2, capacitors C5, C6, A303C14, and A303C15, and resistor A303R26. Fuses F14 and F11 provide overload protection.

3-210. Silicon diodes CR1 and CR2 form a full-wave rectifier, providing approximately 7.9 volts dc which is filtered by A303C14 and A303C15. Capacitors C5 and C6 bypass rf noise spikes produced each ac cycle when diode conduction cuts off. Resistors A303R26 and A310R23 discharge the filter capacitors when power is removed from the computer.

3-211. The -2 volt power source used the entirety of each half of the secondary winding shown in figure 3-20. Silicon diodes CR3 and CR4 form a full-wave rectifier, with capacitors C4 and C7 serving to bypass voltage spikes. Capacitors A303C17 and A303C18 are filter capacitors, and resistor A303R27 discharges these two capacitors when power is removed. Fuses F13 and F12 provide overload protection.

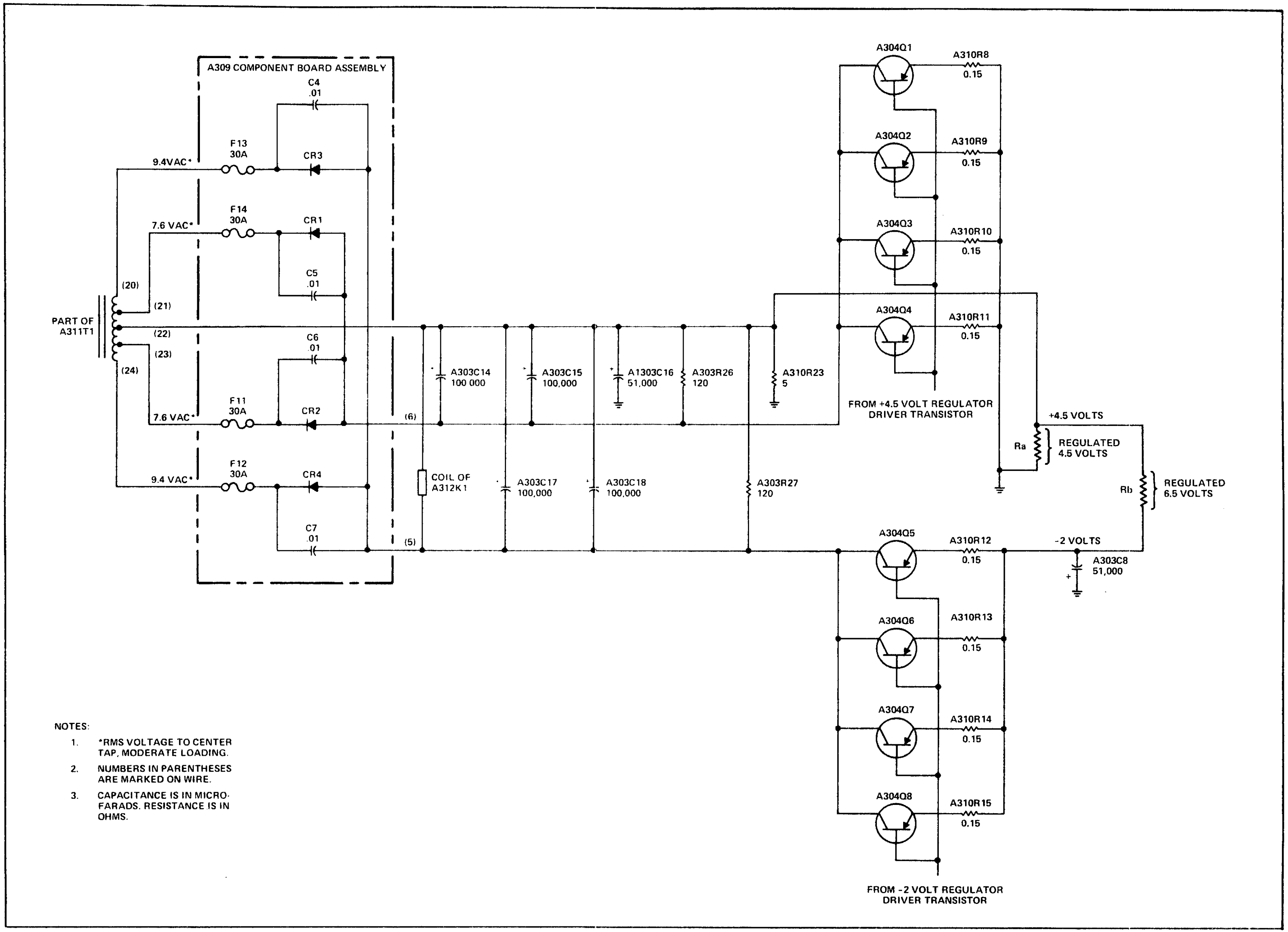

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Figure 3-20. +4.5 Volt and -2 Volt Power Sources, Schematic Diagram

3-212. SCHEMATIC-DIAGRAM ANALYSIS OF +4.5 VOLT VOLTAGE REGULATOR. The +4.5 volt regulator consists of portions of large heat sink assembly A304, a portion of logic supply regulator card A301, resistors A310R8 through A310R11, and resistors A307R45 and A308R17. The circuit is shown in figure 3-21. Included in the schematic diagram are the circuits for +4.5 volt current limiting.

3-213. The voltage regulator is of the series type. By varying the voltage drop across transistors Q1, Q2, Q3, and Q4, the regulator maintains a fixed voltage across the +4.5 volt computer load. When fully loaded, the +4.5 volt regulator and filter capacitors maintain a regulated +4.5 volt output for at least one millisecond after removal of the ac line voltage.

3-214. The +4.5 volt sense input to the regulator is applied to the base of transistor Q30. This transistor and Q31 form a differential amplifier, with resistor R66 providing the means for adjusting the level of the regulated +4.5 volts to the required voltage. Resistors R67 and R65 keep the adjustment of the base voltage of Q31 within normal range, and provide for a vernier action in the adjustment of R66.

3-215. Assuming the +4.5 sense voltage rises above normal, conduction through Q30 decreases, conduction through Q31 increases, and the voltage applied to the base of transistor Q32 becomes less negative. As a result, conduction in Q32 decreases, and the voltage at the base of Q10 becomes less negative. The voltage applied to the bases of Q1, Q2, Q3, and Q4 moves in the positive direction, and these transistors conduct less heavily. As a result, the voltage drop across Q1, Q2, Q3, and Q4 increases, and the regulated +4.5 volts returns toward normal.

3-216. If the regulated +4.5 volts decreases in value, the opposite action to that described above takes place.

3-217. Resistors A310R8 through A310R11 serve to equalize the current through the four series regulator transistors. Because of minor differences among these transistors, one will conduct more than the others. If countermeasures are not taken, this transistor will heat up slightly more than the others, conduct more as a result, and thermal runaway will take place, destroying the transistor. Then the transistor which conducts next-most-heavily will destroy itself, and so on. Resistors A310R8 through A310R11 prevent this current hogging. If a transistor conducts more than the others, the increased voltage drop across its emitter transistor opposes the increase in bias current, preventing runaway. Each transistor establishes its own state of balance.

3-218. The regulator circuit requires the following operating voltages: +20, +23.3, +9, and -12.4 volts. These voltages, used only within the power supply itself, are produced by simple full-wave rectifiers and zener-diode circuits, which require no discussion.

3-219. SCHEMATIC-DIAGRAM ANALYSIS OF +4.5 VOLT CURRENT LIMITER. Transistor Q33 (figure 3-21) is used to control current limiting. The current limiting circuit also uses some of the components employed for voltage regulation. If an excessive load is imposed on the +4.5 volt power supply, Q33 reduces current flow through Q1, Q2, Q3, and Q4, preventing overheating and damage to components. The reduced current through the load reduces the voltage across the load. The voltage regulating circuits oppose this tendency, but the current limiter over-rides the voltage regulator, and the +4.5 volt supply breaks out of regulation in the downward direction. As a result, dc shut-down takes place.

3-220. Resistor A310R11 (figure 3-21) is in the ground side of the +4.5 volt circuit. The voltage drop across the resistor is applied to transistor Q33, and if excessive current is drawn from the +4.5 volt source, Q33 conducts heavily. Voltage at the base of Q32 becomes less negative, causing decreased conduction through Q32. The base of Q10 becomes less negative, moving the bases of Q1, Q2, Q3, and Q4 in the positive direction. This results in decreased conduction by Q1, Q2, Q3, and Q4.

3-221. Transistor Q33 functions as an analog circuit, rather than a switching circuit.

3-222. Resistor R69 is the current-limiting adjustment (CLA). It is adjusted to cause current-limiting at the proper point. If components in the current-limiting circuit are changed, readjustment of R69 may be necessary; however, this adjustment requires special loading and test equipment, and must not be performed in the field. If adjustment is needed, logic supply regulator card A301 must be returned to the factory, where suitable equipment for making the adjustment is available.

3-223. +4.5 VOLT SHUT-DOWN. The +4.5 volt power supply is shut down as a result of any of the following:

a. The computer has been turned off by means of the POWER switch.

b. Overheating in the computer cabinet or in the 2160B Power Supply Extender (if used) has caused a thermal switch to open.

c. AC line voltage has become zero volts.

d. AC line voltage has become abnormally low.

e. The output of the -2 volt power supply has dropped below normal or become zero volts.

3-224. When shut-down of the +4.5 volt supply occurs, the flow of current through the computer load is stopped by the +4.5 volt current limiter. If the computer has been turned off, or if ac line voltage has lowered or become zero, the +4.5 volt current is cut off before the +4.5 volt filter capacitors have appreciably discharged. If shut-down occurs because of reason "b" or "e" above, the +4.5 volt power source continues to function, and the +4.5 volt filter capacitors remain fully charged.

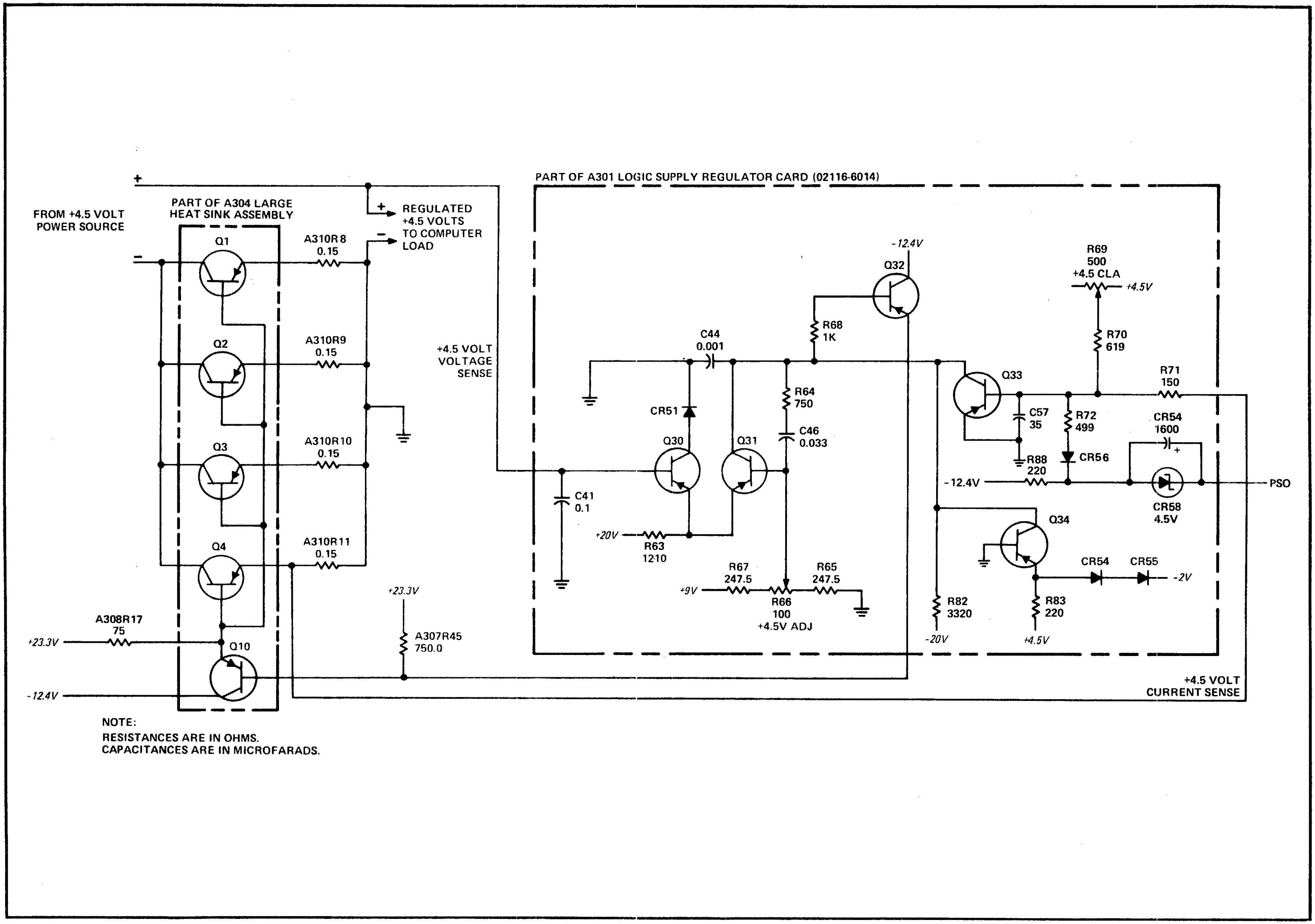

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Figure 3-21. +4.5 Volt Voltage Regulator, Current Limiter, and Shut-Down Circuits, Schematic Diagram

3-225. After dc shut-down resulting from any cause, bypass capacitors on cards in the card cage must discharge before +4.5 volts is completely removed from the computer circuits. About 70 ms is required to discharge these bypass capacitors. (In the case of the +12 volt power supply, several seconds is required if this circuit is only lightly loaded by optional devices.)

3-226. When shut-down occurs because of a fault condition (that is, for any reason other than operation of the POWER switch), the +4.5 volt power is automatically restored if the fault clears. However, a POFP pulse is generated during dc power turn-on. As a result, the program does not restart, and the computer will be in the same state as when power is applied by operating the POWER switch.

3-227. Examining in detail the first two methods of bringing about dc shut-down, if the computer is turned off or if a thermal switch opens the PSO signal becomes false (see figures 3-18 and 3-21). The voltage at the base of transistor Q33 moves in the negative direction, bringing about heavy conduction in Q33. As a result, transistors Q1, Q2, Q3, and Q4 are cut off. When the PSO signal becomes false, power fail interrupt card A1 produces a power fail interrupt, and if programmed to do so the computer stores the contents of registers and performs other functions in preparation for later start-up. (If the program is not running when the power fail interrupt occurs, the power fail program is not performed.)

3-228. The third type of shut-down for the +4.5 volt supply occurs when the ac line voltage drops to zero or becomes abnormally low. First, a power fail interrupt takes place when the line voltage drops below a point which is between 100 and 102 volts rms. (In a 230-volt computer this point is between 200 and 204 volts rms.) The interrupt is produced by power fail interrupt card A1. If the line voltage continues to drop, or if it has become zero volts almost instantly, the various power supply regulators endeavor to maintain their output voltage levels, drawing upon the energy stored in the filter capacitors. A point will be reached when one of the regulators will be unable to maintain its output voltage. The regulator in which this first occurs depends on the loading imposed on each power supply by the various optional devices installed in the computer. If line voltage is still being furnished when a dc voltage drops out of regulation, rectifier ripple will appear on the output of the dc voltage. After the first dc voltage has dropped below its regulated value, other dc voltages are shut down in the manner described later in this section.

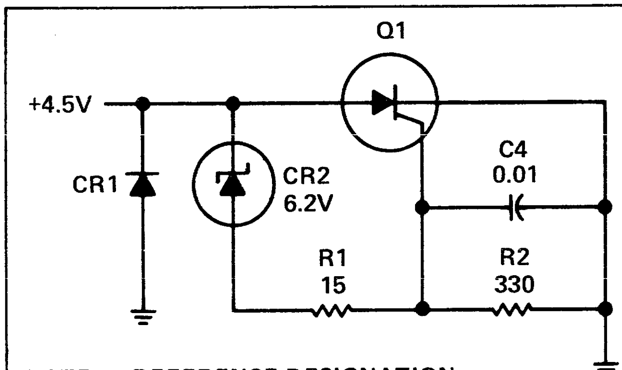
3-229. Turning to the last method of shutting down the +4.5 volt supply, if the -2 volt power supply output becomes abnormally low or fails completely, the voltage applied to diode CR55 becomes less negative. As a result, grounded-base transistor Q34 conducts, leading to the cutting off of Q1, Q2, Q3, and Q4.

3-230. When shut-down of the +4.5 volt power supply occurs because the computer has been turned off or because the ac line voltage has become zero, relay A312K1 de-energizes. Abnormally low ac line voltage may also de-energize A312K1, depending on the ac level reached.

3-231. Further information on the shut-down and turn-on of the +4.5 volt power supply is provided later in this section, when the shut-down and turn-on sequence of power supplies is dealt with.

3-232. SCHEMATIC-DIAGRAM ANALYSIS OF +4.5 VOLT OVERVOLTAGE PROTECTION CIRCUIT. The +4.5 volt overvoltage protection circuit prevents excessive voltage from being applied to the computer load. This high voltage could result from failure of the +4.5 volt voltage regulator.

3-233. The overvoltage protection circuit is shown in figure 3-22. When the regulated +4.5 volts is at its normal value, the voltage across the series circuit consisting of zener diode CR2, resistor R1, and resistor R2, is insufficient to cause avalanche breakdown in the diode. However, if the voltage rises to between +5 and +8 volts, CR2 enters the breakdown region. The resistance of CR2 decreases, and the voltage drop across R2 increases. As a result, silicon-controlled rectifier Q1 conducts at saturation, placing a low resistance across the computer load and making the voltage across the load above 0.9 volts. The heavy current drawn from the +4.5 volt power supply causes current limiting of the power supply output. (Since the voltage regulator may be defective, the current limiter may also be inoperative. If this is the case, the heavy current will result in a blown fuse.) The loss of +4.5 volts across the computer load leads to dc shut-down.



NOTE: REFERENCE DESIGNATION PREFIX IS A121.

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Figure 3-22. +4.5 Volt Overvoltage Protection Circuit, Schematic Diagram

3-234. Diode CR1 prevents current from flowing in the reverse direction through the +4.5 volt power supply. This might occur when another dc voltage is shorted to +4.5 volts. One of the supplies will force current in the reverse direction through the other supply, the power supply receiving the reverse current depending on the voltage and internal impedance of the two supplies concerned. Diode CR1 provides a low resistance path to protect the +4.5 volt power supply from damage due to this cause.

Table 3-5. Overvoltage Limits

NOMINAL REGULATED VOLTAGE	VOLTAGES THAT ACTIVATE THE OVERVOLTAGE PROTECTION CIRCUITS
+4.5	+5.0 To +8.0
- 2.0	-2.5 To -8.0
+12.0	+13.0 To +18.0
-12.0	- 13.0 To - 18.0
+22.0	+23.0 To +28.5
- 22.0	- 23.0 To - 28.5
+32.0	+36.8 To +42.8

3-235. Overvoltage protection is provided for all regulated voltages furnished to the computer. Table 3-5 lists the voltage required to activate each protection circuit.

3-236. SCHEMATIC-DIAGRAM ANALYSIS OF VOLTAGE REGULATOR, CURRENT LIMITER, AND OVERVOLTAGE PROTECTION CIRCUIT FOR -2 VOLTS. The voltage regulator, current limiter, and overvoltage protection circuit for the -2 volt power supply are similar to those used for +4.5 volts, and therefore require no additional circuit theory discussion. When fully loaded, the -2 volt regulator and filter capacitors maintain a regulated -2 volt output for at least one millisecond after removal of the ac line voltage.

3-237. +12, -12, +22, -22, and +32 VOLT POWER SUPPLIES.

3-238. The remaining five regulated power supplies closely resemble the +4.5 and -2 volt supplies. Therefore, no circuit-theory discussion is furnished for these supplies. It must be pointed out, however, that the +22 volt, -22 volt, and +32 volt outputs vary in accordance with the air temperature near the core stack assembly. The circuits for bringing this about are shown in section V in the overall interconnection diagram and the schematic diagram for the A300 power supply. Two thermal sensing resistors, situated on temperature sensing assembly A402, change resistance in accordance with the air temperature near the core stack assembly. As a result, on card A302 the voltage at the base of A302Q54A (for the +22 volt supply) and the base of A302Q61A (for the +32 volt supply) changes in accordance with the temperature. This leads to a variation in the output voltages of the two power supplies, counteracting the change in corestack operation which results from the temperature variation. The output of the -22 volt supply also varies in accordance with temperature. This results from the application of +22 volts to one end of resistor R158 in memory supply regulator card A302. As the +22 volt output changes, the -22 volt regulator varies the -22 volt output by the same amount. Tables 5-2 and 5-3 show the variation in +22, -22, and +32 volts as temperature changes. As with the +4.5 and -2 volt power supplies, the filter capacitors and regulators for +12, -12, +22, -22, and +32 volts maintain a normal regulated output voltage for at least one millisecond after removal of the ac line voltage.

3-239. POWER TURN-ON AND SHUT-DOWN.

3-240. The seven regulated voltages used by the logic and memory circuits are applied to and removed from the computer load circuits in a controlled sequence. These seven voltages are -2, +4.5, +12, -12, +22, -22, and +32 volts. Two further outputs are provided by the power supply; these are +7 volts unregulated and +35.5 volts unregulated. Neither of these voltages enters in the turn-on or shut-down sequence. Additional subsidiary voltages are produced for use within the power supply section itself. Like +7 volts and +35.5 volts, these do not enter into the controlled turn-on or shut-down sequence.

3-241. When the POWER switch is pressed on, the seven controlled voltages are applied to their respective loads in a predetermined sequence. Similarly, when the computer is turned off the controlled voltages are shut down in an orderly manner. In the event of failure of some of the controlled voltages, certain other voltages are shut down. If a thermal switch opens, all controlled voltages are removed in the same sequence as when the POWER switch is pressed off.

3-242. The turn-on or shut-down of the seven controlled voltages is accomplished by making the series regulator transistors for each voltage conduct or cut off. In the case of the +4.5 volt power supply, the series regulator transistors are in the ground return to the power source (figures 3-20 and 3-21, A304Q1 through A304Q4), and it is here that the voltage source is connected to or cut off from the computer load. The series regulator transistors for the remaining six controlled voltages are in the ungrounded (high potential) side of the applicable power supply output.

3-243. TURN-ON SEQUENCE. The power supply turn-on sequence is illustrated in figures 4-89 through 4-92 in Section IV. When the POWER switch is pressed on, the first voltage furnished at full level to the computer load is -2 volts. This voltage is followed by +4.5 volts. Other voltages are furnished in the sequence indicated.

3-244. The waveforms shown in figures 4-89 and 4-90 are for computer turn-on with filter capacitors initially discharged. When power is turned off the series regulator transistors cut off each power supply from its load, and several minutes is required to fully discharge the filter capacitors. Therefore, if the computer is turned on after being off for only a brief time, the waveforms differ somewhat from those shown, and the time required for each voltage to reach operating level is shorter. Further, the waveforms illustrated are for power supplies which are loaded to their maximum capability. With lighter loading, waveforms and timing will differ from those shown, both for turn-on and shut-down.

3-245. The turn-on sequence is determined by the connections between the control circuits for each power supply. This is illustrated in figure 3-23. Each block in the figure represents the power supply named. Before it can furnish an output, every power supply except that for -2 volts must receive the output voltage furnished by the power supply shown to its left. The +12 volt supply requires an input from both the +32 and -12 volt supplies. Figure 4-90 shows that the +12 volt supply reaches operating level before the +32 volt supply, even though the +12 volt supply requires an input from the +32 volt supply. The reason for this is that the +12 volt supply does not require full voltage from the +32 supply in order to furnish full output.

3-246. -2 Volt Turn-On. When the POWER switch is pressed on, the various subsidiary voltages in the power supply section become available as soon as their filter capacitors charge. The filter capacitors for -2 and +4.5 volts also start to charge (figure 5-44). The series regulator transistors for -2 volts (A304Q5 through A304Q8) begin to conduct, as do the corresponding transistors for +4.5 volts (A304Q1 through A304Q4).

3-247. The -12.4 volt power source generates 17.9 volts, from which 4.5 volts normally is subtracted as a result of the series-opposing connection between the +4.5 and -12.4 volt power supplies. At first, however, while the +4.5 volt bus is near ground potential, the -12.4 volt power supply furnishes nearly -17.9 volts. This voltage is applied to resistor R88 on logic supply regulator card A301 (figure 5-44). At this time the PSO signal is not furnished because +4.5 volts is not being supplied to power fail interrupt card A1, which generates PSO. Current flows through resistor R88 and through transistor Q5 on card A1 (figure 5-8), to the +4.5 volt bus, which is near ground potential. Current flow through resistor R88 begins to charge capacitor C54. As it charges, the capacitor bypasses current around zener diode CR58, preventing the diode from entering avalanche breakdown.

3-248. The potential at the anode of CR58 is negative as C54 commences to charge from the -12.4 volt source. This negative voltage is applied to the bases of transistors Q33 and Q38. Diodes CR56 and CR57, together with associated resistors, form an "or" gate. This gate allows application of the potential at the anode of CR58 to Q33 and Q38, while preventing shorting together the -2 volt and +4.5 volt sense voltages.

3-249. The negative potential at the bases of Q33 and Q38 causes these transistors to conduct, bringing about current limiting in the series regulator transistors for +4.5 and -2 volts. As a result, the +4.5 and -2 volt outputs are reduced in amplitude after rising for about 20 milliseconds (figure 4-89). However, the +4.5 volt filter capacitors at the input to the series regulator transistors continue to charge, and the +4.5 volt bus continues to rise above ground level. As the +4.5 volt bus becomes more positive, the -17.4 volt output becomes less negative. At the same time, capacitor C54 continues to charge. A point is reached at which the voltage across C54 is sufficiently great to permit zener diode CR58 to break into avalanche conduction. The bases of Q33 and Q38 become less negative, current limiting ceases, and the filter and bypass capacitors at the outputs of the +4.5 and -2 volt series regulator transistors begin to charge again. The output filter capacitor for +4.5 volts is A303C16, and that for -2 volts is A303C8. The bypass

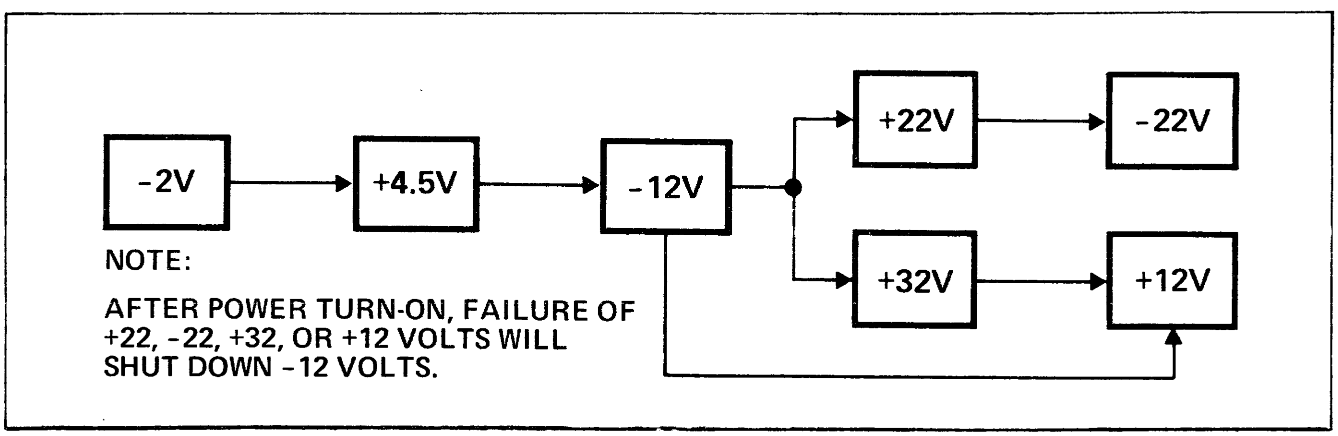

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Figure 3-23. Power Supply Interdependence capacitors for these voltages are situated on various circuit cards in the card cage. When these filter and bypass capacitors are completely charged, the full +4.5 and -2 volts are applied to the computer load circuits. Note in figure 4-89 the change in the rate of rise of +4.5 volts when -2 volts reaches about -1.75 volts. This results from transistor Q34 being cut off.

3-250. The -2 volt output is applied through diodes CR55 and CR54 to the emitter of transistor Q34 on card A301. This is a grounded-base PNP transistor with the potential of the base positive with respect to the emitter; consequently, the transistor normally is cut off. However, if the 2-volts power supply is inoperative, the base of Q34 is negative with respect to its emitter and Q34 conducts heavily. As a result, current limiting in transistors A304Q5 through A304Q8 prevents the +4.5 volt power from reaching the computer load circuits. Thus, if -2 volts is not furnished during turn-on, neither is +4.5 volts. If the -2 volt power supply is operative, Q34 continues to monitor this source after power turn-on, and Q34 shuts down the +4.5 volt supply if -2 volts fails.

3-251. When +4.5 volts rises to its full potential after turn-on, the PSO signal from card A1 also rises to +4.5 volts. At this time the 4.5 volt drop across CR58 results in a potential at the bases of Q33 and Q38 which keeps these transistors cut off. As a result, current limiting does not take place. However, if a thermal switch is open during power turn-on, the PSO signal is false (figure 3-18). With PSO false, the 4.5 volt drop across CR58 results in a negative potential at the bases of Q33 and Q38 (relative to the emitter of each transistor), and the current limiting which occurs during turn-on remains in effect. Consequently, +4.5 and -2 volts are not applied to the computer load circuits.

3-252. -12, +22, -22, +12, and +32 Volt Turn-On. The controlling elements in the turn-on process for -12, +22, -22, +12, and +32 volts are gates MC1B and MC1A on logic supply regulator card A301 (figure 5-44). Gate MC1A monitors the seven regulated voltages during computer coincidence and its true output keeps transistor Q43 cut off. If one of the voltages fails, Q43 conducts and brings about shut-down of -12 volts. When -12 volts is shut down, the +22, -22, +12, and +32 volt supplies also are shut down (figure 3-23). Shut-down is brought about by cutting off the series regulator transistor for the voltage concerned.

3-253. During turn-on, a means must be provided for bypassing this voltage monitoring system until all power supplies are operative. Gate MC1B performs this function. When +4.5 volts is available, capacitor C56 starts to charge. While it is charging, the output of MC1B is true and Q43 is cut off. The capacitor becomes substantially charged in about 0.3 second. At this time the output of MC1B becomes false, and MC1A must then furnish a true output in order to prevent shut-down. The output of gate MC1A is true if all seven regulated voltages are available.

3-254. The seven regulated voltages monitored by gate MC1A are furnished to the gate in the following manner:

a. +4.5 volts is furnished to one end of resistor R113, the other end of which is connected to the gate.

b. -2 volts affects the gate by shutting down the +4.5 volt supply if -2 volt failure occurs.

c. +12 volts if furnished through two resistors and a zener dropping diode to pin 1 of the gate, with diode CR63 functioning as a clamp.

d. -12 volts affects the gate by shutting down the +12 volt and +32 volt supplies if -12 volt failure occurs.

e. -22 volts affects the gate by keeping transistor Q44 cut off, thereby permitting the application of +4.5 volts through resistor R113 without significant drop in voltage.

f. +22 volts affects the gate by shutting down the -22 volt supply if +22 volts fails.

g. +32 volts is furnished through two resistors and a zener dropping diode to pin 14 of the gate, with diode CR62 functioning as a clamp.

3-255. When power turn-on takes place, the -12 volt output starts to rise. However, Q43 on card A301 begins to conduct as various filter capacitors charge, and current limiting takes place for -12 volts. As a result, the voltage across the -12 volt load returns toward zero (figure 4-90). Then, when the +4.5 volt output is available, gate MC1B cuts off Q43, and -12 volts again commences to increase. The series regulator transistor for this voltage functions as a constant current source, and the voltage rise is almost linear as filter and bypass capacitors charge from the regulator output. The filter capacitor is A303C10, and the bypass capacitors are installed on various circuit cards in the card cage.

3-256. The -12 volt output is applied to the +22 volt and +32 volt regulators through temperature sensing resistors R220 and R221 on temperature sensing assembly A402. When -12 volts starts to rise, the +22 volt and +32 volt outputs also commence to rise. Because of the differing current limit adjustments for the +22 and +32 volt supplies, the different loads, and the different amounts of capacitance requiring charging, the two voltages rise at a different rate from each other and from the -12 volt output. The final level of the +22 and +32 volt supplies is determined by the temperature near the core stack assembly. This temperature affects resistors R220 and R221, changing the voltage applied from the -12 volt source to the +22 and +32 volt regulators. (See tables 5-2 and 5-3 in Section V.)

3-257. The output from the +32 and -12 volt supplies are applied to the +12 volt regulator circuit. When the +32 volt output becomes slightly positive, the +12 volt output commences to rise.

3-258. The output of the +22 volt power supply is applied to the -22 volt regulator. As a result, -22 volts increases as +22 volts rises and as the -22 volt output filter capacitor and bypass capacitors charge. The ultimate level of the -22 volt output is determined by the final level of the +22 volt output, which in turn is established by the temperature near the core stack assembly.

3-259. As the interior of the computer cabinet warms up during operation, and as ambient temperature changes, the resistance of R220 and R221 on A402 changes. This brings about a change in the +22 and +32 volt outputs. The shift in the +22 volt level, in turn, causes the -22 volt output to change. The voltages decrease in magnitude with rising temperature, and thereby minimize the effects of temperature change on the ferrite cores in the core stack assembly. The change in -22 and +22 volts affects the X and Y drive current provided by the driver switch cards (A8, A9, A14, and A15). The change in +32 volts affects the inhibit current furnished by the inhibit driver cards (A4, A6, A16, and A18).

3-260. SHUT-DOWN SEQUENCE. Power shut-down can be a result of any of the following:

a. Pressing the POWER switch off.

b. AC power-line failure (excessively low line voltage or no line voltage).

c. Failure or overloading of one of the seven controlled voltages, which may lead to shut-down of some or all of the other controlled voltages.

d. Overheating which causes one of the thermal switches to open.

3-261. When a controlled voltage fails or is overloaded, or when a thermal switch opens, only dc shut-down takes place. When this occurs, the affected voltage or voltages are cut off by their series regulator transistors, but the ac circuits and the dc power sources remain in operation.

3-262. Shut-Down by Power Switch. When the POWER switch is pressed off, relay A312K1 de-energizes (figures 3-17 and 3-18), and filter capacitors throughout the power supply begin to discharge. At the moment the switch opens, +4.5 volts is removed from pin 52 of power fail interrupt card A1. A power-fail interrupt occurs. The POFP pulse produced during shut-down stops the program (if running). The POFP pulse also turns off the I/O system and interrupt priority system. If the program is stopped by the POFP pulse during a memory reference instruction, memory write errors may occur. Therefore, it is advisable to stop the program before pressing the POWER switch off.

3-263. Approximately 8 milliseconds after contacts 3 and 4 of the POWER switch open, the PSO signal becomes false. This false signal, furnished to pin 11 of logic supply regulator card A301, starts the dc power supply shut-down sequence (figures 4-91 and 4-92).

3-264. The false PSO signal is forwarded through zener diode CR58 and other components to the base of transistor Q33 on card A301. The 4.5 volt drop across the zener diode results in the application of a negative voltage to Q33. As a result, series regulator transistors Q1 through Q4 in large heat sink assembly A304 cut off the flow of current from the +4.5 volt supply.

3-265. The false PSO signal is also furnished to the base of transistor Q38, stopping the flow of current from the -2 volt supply by cutting off transistors Q5, Q6, Q7, and Q8 in large heat sink assembly A304.

3-266. To shut down the remaining controlled voltages, the false PSO signal is applied to gate MC1A on logic supply regulator card A1. The gate no longer experiences coincidence, transistor Q43 conducts, and the -12 volt series regulator transistor stops the flow of current from the -12 volt power source. With the loss of -12 volts, the remaining controlled voltages are shut down. (See figure 3-23.)

3-267. When dc shut-down occurs for each controlled voltage, the filter capacitors on the input side of the series regulator transistors discharge through resistors provided for the purpose.

3-268. When the filter capacitors for -5.6 volts have discharged sufficiently, relay A312K1 de-energizes, and the power supply subsidiary voltages are turned off. To fully discharge all filter capacitors, approximately 3 minutes is required.

3-269. Shut-Down Due to AC Power-Line Failure. If the ac line-voltage drops below a level between 100 and 102 volts rms (200 to 204 volts for a 230-volt computer), a power-fail program interrupt occurs. If programmed to do so, and if the computer is running, the computer then performs a power-fail program. The dc voltage regulators and filter capacitors can maintain normal dc voltage for at least 1 millisecond after complete ac line voltage failure. During this time the power fail program can perform at least 200 instructions. At the end of the program the computer halts if so programmed. (To avoid loss of data in core storage, a programmed halt should be performed.) If the ac line voltage has dropped below about 80 volts rms (160 volts for a 230-volt computer), or has failed completely, filter capacitors discharge and the power supply series regulator transistors can no longer maintain the required voltage levels. The voltage which drops out of regulation first, and the ac line voltage at which this occurs, depends on the loading of the various regulators. This, in turn, depends on the quantity and type of optional devices which have been installed in the computer.

3-270. When the first voltage drops out of regulation, other controlled voltages which depend on the affected voltage are shut down. Figure 3-23 illustrates the requirement of each controlled power supply with respect to outputs from other supplies. If any power supply drops out of regulation, the supplies to the right in the illustration are shut down. Also, if any supply to the right of the -12 volt supply loses regulation, -12 volts is shut down, resulting in all supplies shown to the right of the -12 supply being shut down.

3-271. A condition that could result from a continued abnormally low line voltage is that certain controlled voltages are shut down, while others continue to be furnished to the computer load.

3-272. When +12 volts is shut down, and if +4.5 volts is still available, power fail interrupt card A1 produces a power on/off pulse (POFP). This pulse turns off the I/O system and the interrupt priority system, and stops the computer if it is running.

3-273. If the ac line voltage becomes sufficiently low or if it drops to zero, relay A312K1 de-energizes (figure 3-18). When line voltage returns to normal, the computer undergoes the normal power-on sequence and will then be ready for use, but will not be running.

3-274. If the ac line voltage is low enough to cause dc power shut-down, but is not sufficiently low for A312K1 to de-energize, power transformer A311T1 continues to furnish voltage to the subsidiary rectifiers in the power supply. The series regulator transistors for the controlled voltages maintain the shut-down condition. Upon restoration of normal ac line voltage, the normal power turn-on sequence takes place except that relay A312K1 has remained energized and resistor A300R1 remains shorted out.

3-275. Shut-Down Due to Failure of a Controlled Voltage. If one of the controlled power supplies (+4.5, -2, +12, -12, +22, -22, or +32 volts) experiences failure, other controlled supplies may be shut down. Figure 3-23 illustrates the requirement of each controlled power supply with respect to outputs from other supplies. A power fail interrupt occurs when shut-down of this type takes place. (Since a regulated dc voltage has failed, the power fail program may not function correctly.)

3-276. When +12 volts is shut down, and if +4.5 volts is still available, power fail interrupt card A1 produces a power on/off pulse (POFP). This pulse turns off the I/O system and the interrupt priority system, and stops the computer if it is running.

3-277. Failure of a voltage regulator circuit might result in a subnormal voltage from one of the controlled supplies. If small, the drop in voltage may not be enough to disable MC1A on card A301. If this occurs, all power supplies continue to furnish voltage to the computer. The worst case is for +32 volts. This voltage is applied to gate MC1A through zener voltage-dropping diode CR64, rated at 17.8 volts. Subtracting this amount from 32 volts leaves 14.2 volts. Clamp diode CR62 establishes a potential of +4.5 volts at the junction of the two diodes. Therefore, the +32 volt output must drop below 22.3 volts in order to bring about a decrease in potential at the junction of the diodes. This effect produces the following result during power turn-on. The +32 volt output rises more slowly during turn-on than the other controlled voltages. However, it need reach only 22.3 volts to furnish a full input to gate MC1A, permitting this gate to function before the output of gate MC1B becomes false.

3-278. Another result of voltage regulator failure could be an abnormally high voltage from the power supply. If the voltage becomes sufficiently high, the overvoltage protection circuit imposes a short on the power supply output (see table 3-5). As a result of the short, shut-down takes place for the affected voltage. This, in turn, may shut down other controlled voltages, as illustrated in figure 3-23. As previously noted, if shut-down occurs for any power supply to the right of the -12 volt supply in the illustration, the -12 volt supply itself is shut down, resulting in shut-down of all supplies shown to the right of the -12 volt supply.

3-279. Shut-Down Due to Open Thermal Switch. When a thermal switch opens, a power-fail interrupt occurs. The PSO signal becomes false (figure 3-18) and as a result, the seven controlled voltages are shut down by their series regulator transistors. However, relay A312K1 remains energized and the fans continue to function. The +7 volt lamp voltage and the subsidiary voltages produced for use within the power supply section continue to be available. If there is sufficient cooling to permit the thermal switch to close after dc shut-down, the computer undergoes the normal power turn-on sequence except that A312K1 is already energized. The computer is available for use after this turn-on, but is not running.

3-280. PON SIGNAL. A power-on-normal (PON) signal is furnished by power fail interrupt card A1 when +4.5 and -2 volts are available to the computer. The PON signal becomes true approximately 0.1 second after these voltages are furnished to the computer load, and the signal remains true while both voltages are available.

3-281. When it is false, the PON signal protects stored data by preventing memory readout during the transient conditions of power turn-on. The false PON signal also prevents certain operations of I/O devices, such as drum or disc writing, during power turn-on and shut-down.

3-282. The PON signal is furnished to driver switch cards A8, A9, A14, and A15. Here the PON signal, when false, prevents activation of core memory X and Y drive lines. Memory readout therefore cannot occur. The PON signal also affects the state of the "not" memory-normal-switch ("not" MNS) signal furnished to timing generator card A106. When PON is false, "not" MNS is true, and control signals used for writing and reading in core memory remain false, providing further protection against destruction of stored data.

3-283. The function of the PON signal on I/O interface cards is described in the operating and service manual for the device concerned.

3-284. As noted, the PON signal becomes true approximately 0.1 second after +4.5 and -2 volts are furnished to card A1 (figure 5-7) during turn-on. The potential of Q3 is then approximately +2.5 volts with respect to ground. Since the collector connects to +4.5 volts, the base of the transistor is negative with respect to its collector and the transistor conducts. Capacitor C5 commences to charge. After approximately 0.1 second, the capacitor is sufficiently charged to cause the $\overline{PON}$ signal to become true. The switching action of driver MC17A steepens the leading edge of the PON signal from the exponential charge-curve of capacitor C5.

3-285. POFP PULSE. During dc turn-on and shut-down a power on/off pulse (POFP) is produced by power fail interrupt card A1. The pulse is produced for any power shut-down, regardless of cause, which shuts down the +12 volt power supply.

3-286. The POFP pulse ensures that the computer is halted, that it is in the fetch phase, and that the I/O system and interrupt priority system are turned off. To bring about these conditions, the POFP pulse sets or clears flip-flops as follows:

a. POFP resets the Run 1 and Run 2 FFs on timing generator card A106. This ensures that the computer is halted.

b. POFP sets the Phase 1 FF on timing generator card A106. This places the computer in the fetch phase.

c. POFP initiates reset of the Interrupt Control FF on I/O control card A201, and reset of the Flag and Control FFs on each I/O interface card. This turns off the I/O system.

d. POFP resets the Flag FF on power fail interrupt card A1. This disables the priority line for all devices that have a lower interrupt priority than that of the power fail interrupt. Since the power fail interrupt has the highest priority, the entire priority system is disabled. Before the computer is started, the interrupt priority system is made effective by pressing the PRESET switch, thereby resetting the Flag FF on card A1.

3-287. A single POFP pulse is produced each time the computer is turned on or off. The pulse is also produced when +12 volts fails or when +12 volts is shut down by an open thermal switch or by failure of another voltage. The POFP pulse, which is true for about 40 milliseconds, is produced by transistors Q2, Q3, and Q4 and their associated components, on card A1 (figure 5-7). When +4.5 volts and -2 volts become available during power turn-on the base of Q3 is negative with respect to its emitter, and the transistor conducts. Before +12 volts is furnished, the base of Q4 is more positive than its collector, and the transistor is cut off. Transistor Q2, however, conducts heavily and furnishes nearly +4.5 volts to pin 6 of gate MC57B. As a result, the POFP signal becomes true. The true output of Q2 also resets the Flag FF on card A1. When +12 volts is furnished to the cathode of CR7, Q2 cuts off and the POFP pulse becomes false.

3-288. During shut-down, the POFP pulse becomes true when +12 volts is removed from the cathode of diode CR7. The pulse remains true until +4.5 volts is shut down.

3-289. POWER-FAIL INTERRUPT CIRCUITS. If the ac line-voltage drops below a level between 100 and 102 volts rms (200 to 204 volts if the computer is connected for 230-volt operation), a power-fail interrupt occurs. The priority of this interrupt is 4, and it causes a program jump to core-memory address 00004. From that point, operations depend on whether a power-fail interrupt program is stored in memory. The program is written to suit the needs of the particular installation, but in general it stores the contents of registers and performs other actions in preparation for later start-up at the point of program termination.

3-290. The circuits which initiate the power-fail interrupt are on power fail interrupt card A1 (figure 5-7). Pins 79 and 80 of this card receive a voltage furnished by a center-tapped secondary winding on transformer A311T1 in the power supply section. With normal ac line-voltage, pins 79 and 80 receive 18 volts ac rms, with the voltage at the two pins 180 degrees out of phase. This ac voltage is rectified by diodes CR1 and CR2, which together constitute a full-wave rectifier. Resistor R3, with capacitors C2 and C3, filter the rectified voltage.

3-291. The rectified voltage, is applied to a voltage divider made up of resistors R6, R7, and R8. Potentiometer R7 is adjusted so that with normal ac line-voltage transistor Q7 conducts and Q8 is cut off. The collector source for Q8 is pin 3 of gate MC97B, which normally is slightly negative.

3-292. If the ac line-voltage becomes excessively low Q7 cuts off, Q8 conducts, and gate MC97B experiences coincidence. As a result, a power-fail interrupt occurs. Further discussion of the circuits which produce the interrupt is presented in paragraph 4-81.

3-293. GROUND CIRCUITS.

3-294. AC NEUTRAL.

3-295. In keeping with international safety regulations, the power-line ac neutral input to the computer is not connected to the computer frame.

3-296. FRAME GROUND.

3-297. Schematic diagrams which show frame ground connections are the following:

a. A300 power supply assembly schematic (figure 5-44).

b. A502 control panel assembly schematic (figure 5-47).

c. Overall interconnection diagram (figure 5-49).

3-298. The earth-ground conductor in the ac power cable is connected to the frame of the computer at the base of connector A300J1.

3-299. The power supply dc ground-return circuit is connected to the computer frame at the anode of diode A308CR9. This diode bolts to a metal bracket attached to the computer frame. No insulating washer is used for mounting the diode, and its anode is therefore electrically connected to the mounting bracket.

3-300. The frame of the card cage is connected to the power supply dc ground-return circuit at point E2, where the ground strap from the power supply bolts to the frame of the card cage. DC ground return is also connected to the card cage frame in overvoltage protection assembly A121.

3-301. The door is connected to the dc ground-return circuit at a lug beside POWER switch A502S109.

3-302. CARD GROUND.

3-303. For each etched-circuit card in the card cage, ground connection is made at backplane pins 1, 2, 85, and 86. In most cases, these pins serve for both dc ground-return and signal ground-return. In some instances, additional pins are used for signal ground-return in order to eliminate coupling due to voltage drop in common ground returns.

3-304. Cards which have a 48-pin connector on the front use pins 1, A, 24, and BB of the connector for signal ground-return. In some cases additional pins also are employed.

3-305. BUS BARS.

3-306. Three square bus bars are installed on the right side of the power supply section. At the top, they curve over capacitor board assembly A303. At the bottom, flexible metal straps are attached to make connection with the card cage. The front bus bar carries regulated +4.5 volts. The middle bus bar is at ground potential. The rear bus bar carries regulated -2 volts.

SECTION IV

TROUBLESHOOTING

4-1. INTRODUCTION.

4-2. This section of the manual contains testing and troubleshooting data for the computer's control section, arithmetic section, memory section, input/output section, and power supply section. The test data is used to check the overall performance of the computer. The troubleshooting data is used to check the computer sections at the circuit level.

4-3. TEST DATA.

4-4. Test data for the computer consists of the basic checkout (paragraph 4-9) and the diagnostic checkout (paragraph 4-17). Performing the basic checkout test procedure is the first step of computer testing. This procedure consists of step-by-step instructions for using front panel switches and indicators to make a preliminary check of the computer's performance before more detailed testing is attempted. Trouble symptoms detected in making this check are analyzed to establish which circuit function is most probably causing the trouble indication. References are provided to detailed troubleshooting data for the suspected circuit. If no trouble symptoms are detected in the course of performing the basic checkout procedure, the computer is assumed to be capable of loading, storing, and at least partially executing diagnostic test programs.

4-5. Performing the diagnostic checkout test procedure is the next step of computer testing. Diagnostic test programs are used to dynamically check the operation of the circuits in the control, arithmetic, memory, and input/output sections of the computer. Trouble symptoms are indicated by error halts displayed at the front panel. By carefully analyzing the error halt condition, the cause of the trouble can be traced to one or more instructions in the test program which the computer failed to process. References are provided to detailed troubleshooting data for the circuits suspected of causing the failure. If no error halts are detected in the course of performing the diagnostic checkout procedure, the computer is assumed to be ready to resume normal operation.

4-6. TROUBLESHOOTING DATA.

4-7. The troubleshooting data in this section is used for checking the computer at the circuit level to isolate trouble symptoms, which are detected during the course of computer testing, to a replaceable assembly or part. Troubleshooting data included in this section consists of a program instruction index and troubleshooting reference guide, logic equations, circuit descriptions, test procedures, and troubleshooting diagrams. The purpose and use of this data is explained in paragraphs 4-38 through 4-55.

4-8. Troubleshooting data contained in other sections of this manual and in other manuals is described in paragraphs 4-56 through 4-59.

4-9. BASIC CHECKOUT.

4-10. GENERAL.

4-11. The basic checkout test procedure is performed using operating switches and indicators to check the overall performance of the computer. This test procedure should be conducted immediately after the computer is installed, and as required thereafter as part of a regularly scheduled preventive maintenance program, as the first step of troubleshooting, and after repairs or modifications are made to the computer. The basic checkout should always be performed prior to attempting to perform the diagnostic checkout. Successful completion of all test steps in the basic checkout procedure ensures that the computer is operational to the extent that diagnostic test programs can be loaded into memory and at least partially executed.

4-12. REQUIRED TEST EQUIPMENT.

4-13. No test equipment is required for performing the basic checkout procedure. However, it is recommended that the following test equipment, or its equivalent (refer to table 1-5), be prepared for operation in the event it is required for troubleshooting:

a. HP 180A Plug-In Oscilloscope Main Frame.

b. HP 1801A Vertical Amplifier (plug-in for HP 180A).

c. HP 1820A Time Base (plug-in for HP 180A).

d. HP 10004A Miniature Resistive Divider Probes (10:1).

e. HP 3439A Plug-in Digital Voltmeter.

f. HP 3441A Range Selector (plug-in for HP 3439A).

g. HP 427A Multi-Function Meter.

h. HP 10525A Logic Probe.

4-14. TEST PROCEDURE.

4-15. The basic checkout procedure consists of a series of tests that check the operation of key circuit functions in the computer. The purpose of these tests is to provide an expedient means of detecting obvious trouble symptoms. The results of each test, when compared to expected normal results, provides an indication as to whether or not the circuit under test is functioning normally. Instructions are included for analyzing trouble symptoms, and references are provided to troubleshooting data for the circuits most likely to be causing the trouble indication. Troubles encountered during the performance of the basic checkout must be corrected before diagnostic testing is attempted.

4-16. Instructions for performing the basic checkout procedure are contained in the following steps:

Note

If computer power is on at the start of this procedure, check the status of all front panel indicators before turning off the power. If possible, check the indicators while the computer is in the run mode, and again while the computer is in the halt mode. Carefully note and record any trouble symptoms which are observed, as well as those reported by the computer operator. This information may prove useful in the troubleshooting process.

a. At the front panel of the computer, press and release the POWER switch to turn off power.

b. Open the door assembly and remove the four retaining screws securing the card cage to the mainframe. Fully extend the card cage from the cabinet and swing it out to the servicing position.

WARNING

Dangerous ac line voltage is present in the computer even though the POWER switch has been turned off at the front panel. Protective panels and covers installed on the power supply, on the bottom of the card cage, and over the wiring side of the POWER switch are designed to prevent personal contact with components that are wired directly to the hot side of the ac line. Use caution when servicing in these areas even though the protective panels and covers are in place. If it is necessary to remove a protective panel or cover during servicing, first turn off all ac line voltage from the computer by disconnecting the power cord from ac power input connector A300J1 at the rear panel of the computer. If it is necessary to apply power to the computer while a protective panel or cover is removed, use extreme caution to avoid contact with the exposed area. Refer to paragraph 5-7 for additional safety information before proceeding.

c. Inspect the electrical assemblies and parts comprising the door assembly, backplane, and power supply for visible indications of trouble, such as burned wiring, broken wiring connections, loose or improper cable connections, or plug-in cards installed in wrong slots or improperly seated in mating connectors. Also inspect for excess dirt accumulations or foreign matter that could restrict airflow through the cabinet and cause overheating. Take immediate action to correct any condition that may be the cause of trouble. Note those conditions that do not require immediate corrective action, but which should be serviced when regularly scheduled preventive maintenance is performed.

d. At the front panel of the computer, check that the LOADER switch is in the PROTECTED position. On the display board located behind the front panel, check that the MEMORY, PHASE, and INSTRUCTION switches are in the NORM position. If these switches are not set as specified, set them to the NORM position before proceeding.

Note

If the 12588A Power Failure Interrupt With Automatic Restart Option (option 008) is installed, the computer program may start automatically when power is turned on. To prevent this from happening, press and hold either the HALT switch or the PRESET switch whenever the POWER switch is pressed and released to turn on power.

e. Press and release the POWER switch to turn on power. Check that fans A300B1 at the top of the power supply, A304B2 and A305B3 on the bottom of the heat sink assemblies, and A200B1, A200B2, and A200B3 on the bottom of the card cage are operating properly. Check each fan for abnormal airflow and audible indications of defective motor bearings, fan blade obstructions, or other indications of abnormal operation. If all fans are operating normally, proceed to step "f". Otherwise, select the applicable step from those following and proceed as directed:

(1) If all fans are inoperative, press and release the POWER switch to turn off power. Check the condition of fuse A312F1 (see figure 4-93). If the fuse is blown, replace it and repeat step "e" above. If the fuse blows again, refer to paragraph 4-502 and troubleshoot for a short in the ac distribution circuits. If the fuse was intact when checked, refer to paragraph 4-504 and troubleshoot for an open condition in the ac distribution circuits.

Table 4-8. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION MNEMONIC	INSTRUCTION TYPE	DEFINITION AND DESCRIPTION	REFERENCES PARA-GRAPH	REFERENCES FIGURE
MAC	Special	Macroinstruction. This instruction provides up to 2048 entries to macroinstruction subroutines. It is used only by special options and special software, and is not included as one of the instructions in the basic instruction set for the computer. The basic computer processes a MAC instruction in the same manner as a NOP instruction.	NA	NA
MIA	Input/Output	Merge Input into A-Register. The contents of the buffer register on the interface card residing in the addressed I/O channel are merged with the contents of the A-register by performing the inclusive "or" function. The results of the merger are stored in the A-register. The previous contents of the A-register are lost.	4-418	4-73
MIB	Input/Output	Merge Input into B-Register. The contents of the buffer register on the interface card residing in the addressed I/O channel are merged with the contents of the A-register by performing the inclusive "or" function. The results of the merger are stored in the B-register. The previous contents of the B-register are lost.	4-418	4-73
NOP	Register Reference (SRG)	No Operation. No processing operation is performed. Only a memory cycle occurs.	4-259	4-46
OTA	Input/Output	Output from A-Register. The contents of the A-register are loaded into the buffer register on the interface card residing in the addressed I/O channel. If the buffer register has less than 16 bit positions, the least significant bits from the A-register are normally loaded. The contents of the A-register remain unaltered.	4-430	4-75
OTB	Input/Output	Output from B-Register. The contents of the B-register are loaded into the buffer register on the interface card residing in the addressed I/O channel. If the buffer register has less than 16 bit positions, the least significant bits from the B-register are normally loaded. The contents of the B-register remain unaltered.	4-430	4-75
RAL	Register Reference (SRG)	Rotate all A-Register bits Left one place. The bit in position 15 is rotated around to bit position 0.	4-287	4-51
RAR	Register Reference (SRG)	Rotate all A-Register bits Right one place. The bit in position 0 is rotated around to bit position 15.	4-293	4-52

(2) If one or more but not all fans are inoperative, press and release the POWER switch to turn off power. Disconnect the power cord from ac power input connector A300J1 at the rear panel of the computer and check the wiring to the inoperative fan (see figure 3-17). If defective wiring is not the cause of the trouble, replace the inoperative fan, and repeat step "e".

CAUTION

Do not continue with this procedure unless all fans are operating normally. Loss of air flow from an inoperative or improperly operating fan may cause overheating which could result in serious damage to computer components. Turn off power and do not attempt further operation until the trouble has been corrected.

f. Make a general inspection of the indicators on the front panel of the computer. Then select the applicable step from those following and proceed as directed:

(1) If all indicators are off, refer to paragraph 4-504 and troubleshoot the ac distribution circuits. (Bear in mind that fans are receiving ac power.)

(2) If only the POWER indicator is on and all other indicators are off, replace fuse A311F10 (see figure 4-93). If fuse replacement fails to correct the trouble, refer to paragraph 4-506 and troubleshoot the +7-volt lamp supply circuit.

(3) If at least some of the indicators are on, check whether the indicators listed in table 4-1 are providing normal indications. If all indicators are normal, proceed with step "g". If an abnormal indication is encountered, take the corrective action specified in the table.

g. At the front panel of the computer, press and release the PRESET switch and check that the PRESET indicator goes off. If the indication is normal, proceed to step "h". If the indication is abnormal, refer to paragraph 4-81 and troubleshoot the circuits associated with the PRESET switch.

Note

Throughout this manual, displays by binary indicators 0 through 15 of the T-REGISTER MEMORY DATA display, P-REGISTER PROGRAM COUNTER display, M-REGISTER MEMORY ADDRESS display, A-REGISTER ACCUMULATOR display, and B-REGISTER ACCUMULATOR display are expressed as six digit octal numbers. For example, a sixteen bit binary display of 0 000 110 111 010 101 (corresponding to indicators 15 through 0 as viewed from left to right at the computer front panel, with indicators that are on representing a binary 1, and indicators that are off representing a binary 0) is expressed as 006725. Settings for the switches in the SWITCH REGISTER are also expressed as six digit octal numbers. For example, the setting 1 011 100 001 111 000 for switches 15 through 0 (as viewed from left to right at the front panel, with switches set to the up position representing a binary 1, and switches set to the down position representing a binary 0) is expressed as 134170.

h. Set the SWITCH REGISTER to 000000 (switches 15 through 0 in the down position), and in turn, press and release the LOAD MEMORY, LOAD A, LOAD B, and LOAD ADDRESS switches. Then set the SWITCH REGISTER to 177777 (switches 15 through 0 in the up position). Press and release the LOAD A switch and check the A-REGISTER ACCUMULATOR display for an indication of 177777 (indicators 15 through 0 on). If the indication is normal, proceed to step "i". If all indicators in the display fail to go on, refer to paragraph 4-86 and troubleshoot the circuits associated with the LOAD A switch. If only one of the indicators in the display fails to go on, replace the associated indicator lamp. If lamp replacement fails to correct the trouble, refer to paragraph 4-86 and troubleshoot the circuits associated with the unresponse indicator.

i. Set the SWITCH REGISTER to 000000 (switches 15 through 0 in the down position). Press and release the LOAD A switch and check the A-REGISTER ACCUMULATOR display for an indication of 000000 (indicators 15 through 0 off). If the indication is normal, proceed to step "j". If all indicators in the display fail to go off, refer to paragraph 4-86 and troubleshoot the circuits associated with the LOAD A switch. If only one of the indicators in the display fails to go off, refer to paragraph 4-86 and troubleshoot the circuits associated with the unresponsive indicator.

Table 4-1. Front Panel Indicator Initialization, Checkout and Trouble Analysis

INDICATOR	NORMAL INDICATION	IF INDICATION IS ABNORMAL
POWER	On	Replace POWER indicator lamp A502DS109. If lamp replacement fails to correct the trouble, refer to paragraph 4-68 and troubleshoot the circuits associated with the POWER indicator.
RUN	Off	Press and release the HALT switch. If the RUN indicator remains on, refer to paragraph 4-71 and troubleshoot the circuits associated with the RUN indicator. If pressing the HALT switch turns off the RUN indicator, refer to paragraph 4-512 and troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal.
HALT	On	Press and release the HALT switch. If the HALT indicator is now on, refer to paragraph 4-512 and troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal. If the HALT indicator remains off, replace indicator lamp A502DS107. If lamp replacement fails to correct the trouble, refer to paragraph 4-76 and troubleshoot the circuits associated with the HALT indicator.
FETCH	On	Press and release the PRESET switch. If the FETCH indicator is now on, refer to paragraph 4-512 and troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal. If the FETCH indicator remains off, replace indicator lamp A501DS84. If lamp replacement fails to correct the trouble, refer to paragraph 4-167 and troubleshoot the circuits associated with the FETCH indicator.
INDIRECT	Off	Press and release the PRESET switch. If the indicator is now off, refer to paragraph 4-512 and troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal. If the INDIRECT indicator remains on, refer to paragraph 4-171 and troubleshoot the circuits associated with the INDIRECT indicator.
EXECUTE	Off	Press and release the PRESET switch. If the EXECUTE indicator is now off, refer to paragraph 4-512 and troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal. If the EXECUTE indicator is still on, refer to paragraph 4-176 and troubleshoot the circuits associated with the EXECUTE indicator.
PRESET	On	Replace indicator lamp A502DS108. If lamp replacement fails to correct the trouble, refer to paragraph 4-81 and troubleshoot the circuits associated with the PRESET indicator.
PARITY HALT	Off	Refer to the operating and service manual for the HP 12591A Parity Error Option (manual part no. 12591-9001) and troubleshoot the circuits associated with the PARITY HALT indicator.

j. Set the SWITCH REGISTER to 177777. Press and release the LOAD B switch and check the B-REGISTER ACCUMULATOR display for an indication of 177777. If the indication is normal, proceed to step "k". If all indicators in the display fail to go on, refer to paragraph 4-92 and troubleshoot the circuits associated with the LOAD B switch. If only one of the indicators in the display fails to go on, replace the associated indicator lamp. If lamp replacement fails to correct the trouble, refer to paragraph 4-92 and troubleshoot the circuits associated with the unresponsive indicator.

k. Set the SWITCH REGISTER to 000000. Press and release the LOAD B switch and check the B-REGISTER ACCUMULATOR display for an indication of 000000. If the indication is normal, proceed to step "l". If all indicators in the display fail to go off, refer to paragraph 4-92 and troubleshoot the circuits associated with the LOAD B switch. If only one of the indicators in the display fails to go off, refer to paragraph 4-92 and troubleshoot the circuits associated with the unresponsive indicators.

l. Set the SWITCH REGISTER to 177777. Press and release the LOAD ADDRESS switch and check both the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display for an indication of 177777. If the indication by both displays is normal, proceed to step "m". If all indicators in either or both displays fail to go on, refer to paragraph 4-98 and troubleshoot the circuits associated with the LOAD ADDRESS switch. If only one indicator in either display fails to go on, replace the associated indicator lamp. If lamp replacement fails to correct the trouble, refer to paragraph 4-98 and troubleshoot the circuits associated with the unresponsive indicator.

m. Set the SWITCH REGISTER to 000000. Press and release the LOAD ADDRESS switch and check both the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display for an indication of 000000. If the indication by both displays is normal, proceed to step "n". If all indicators in either or both displays fail to go off, refer to paragraph 4-98 and troubleshoot the circuits associated with the LOAD ADDRESS switch. If only one indicator in either display fails to go off, refer to paragraph 4-98 and troubleshoot the circuits associated with the unresponsive indicator.

n. Set the SWITCH REGISTER to 177777. Press and release the LOAD MEMORY switch and check the T-REGISTER MEMORY DATA display for an indication of 177777. If the indication is normal, proceed to step "o". If all indicators in the display fail to light, refer to paragraph 4-106 and troubleshoot the circuits associated with the LOAD MEMORY switch. If only one indicator in the display fails to go on, replace the associated indicator lamp. If lamp replacement fails to correct the trouble, refer to paragraph 4-106 and troubleshoot the circuits associated with the unresponsive indicator.

o. Set the SWITCH REGISTER to 000000. Press and release the LOAD MEMORY switch and check the T-REGISTER MEMORY DATA display for an indication of 000000. If the indication is normal, proceed to step "p". If all indicators in the display fail to go off, refer to paragraph 4-106 and troubleshoot the circuits associated with the LOAD MEMORY switch. If only one of the indicators in the display fails to go off, refer to paragraph 4-106 and troubleshoot the circuits associated with the unresponsive indicator.

p. Set the SWITCH REGISTER to 177770 and press and release the LOAD ADDRESS switch. While observing the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display, press and release the LOAD MEMORY switch seven times and check that both displays are incremented by a count of one each time the LOAD MEMORY switch is pressed and released. (Both displays should indicate 177777 after the LOAD MEMORY switch has been pressed and released seven times.) Then press and release the LOAD MEMORY switch again. (Both displays should now indicate 000000.) If the indications by both displays were normal, proceed to step "q". If an indication by either or both displays was abnormal, refer to paragraph 4-106 and troubleshoot the circuits associated with the LOAD MEMORY switch. (Check the circuits associated with the carry bit signals as the first step of troubleshooting if either or both displays failed to "wrap around" from 177777 to 000000 when the LOAD MEMORY switch was pressed and released the eighth time.)

q. Set the SWITCH REGISTER to 177770 and press and release the LOAD ADDRESS switch. While observing the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display, press and release the DISPLAY MEMORY switch seven times and check that both displays are incremented by a count of one each time the DISPLAY MEMORY switch is pressed and released. (Both displays should indicate 177777 after the DISPLAY MEMORY switch has been pressed and released seven times.) If the indication by both displays is normal, proceed to step "r". If the indication by either or both displays is abnormal, refer to paragraph 4-116 and troubleshoot the circuits associated with the DISPLAY MEMORY switch.

r. Set the SWITCH REGISTER to 177770 and press and release the LOAD ADDRESS switch. While observing the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display, press and release the SINGLE CYCLE switch seven times and check that both displays are incremented by a count of one each time the SINGLE CYCLE switch is pressed and released. (Both displays should indicate 177777 after the SINGLE CYCLE switch has been pressed and released seven times.) If the indication is normal, proceed to step "s". If the indication by either or both displays is abnormal, refer to paragraph 4-124 and troubleshoot the circuits associated with the SINGLE CYCLE switch.

Note

Use care when performing steps "s" and "t" following to prevent the absolute loader program from being destroyed. If this should happen, reload the required instructions in the protected area of memory using the procedure presented in paragraph 4-27 and repeat steps "s" and "t" before proceeding to step "u".

s. Using the verification procedure presented in paragraph 4-28 and the information presented in table 4-4 or 4-5, as applicable, check the status of all 64 instructions in the Basic Binary Loader program located in the protected area of memory. If all instructions are correct, proceed to step "t". If an incorrect program instruction is encountered, attempt to load the correct instruction into the applicable memory location using the instruction loading procedure presented in paragraph 4-27 and the information presented in table 4-4 or 4-5. Then reverify the contents in the memory location to ensure that the instruction was loaded properly. If the contents of the memory location are still incorrect, troubleshoot the circuits comprising the memory section of the computer. Refer to paragraph 4-156 and check the memory timing circuits as the first step of troubleshooting.

t. Again, using the verification procedure presented in paragraph 4-28 and the information presented in table 4-4 or 4-5, recheck the status of the first 12 memory locations in the protected area of memory (addresses 0m7700 through 0m7713). If all 12 instructions are still correct, proceed to step "u". If any one or all of the instructions are now incorrect, refer to paragraph 4-478 and troubleshoot the circuits associated with memory write circuits.

Note

Make sure the LOADER switch has been reset to the PROTECTED position before proceeding.

u. At the front panel of the computer, proceed as follows:

Note

Steps (1) through (8) below contain a step-by-step procedure for manually loading a test program into the computer memory in preparation for performing steps "v" through "y". The test program consists of five instructions that can be stored in any five consecutive memory locations in a memory page (other than protected, reserved, or unaccessible locations). The memory locations specified for these instructions are typical, and may be changed to any unused area in memory to prevent destroying program data or instructions already stored in the specified locations. Therefore, if a starting address other than 004000 is used, refer to the information given in figure 4-1 and modify the octal values accordingly for the SWITCH REGISTER settings given in steps (1), (6), and (8).

(1) Set the SWITCH REGISTER to 004000 (typical address for the first instruction of the program) and press and release the LOAD ADDRESS switch.

(2) Set the SWITCH REGISTER to 002400 (CLA) and press and release the LOAD MEMORY switch.

(3) Set the SWITCH REGISTER to 060001 (LDA) and press and release the LOAD MEMORY switch.

(4) Set the SWITCH REGISTER to 006400 (CLB) and press and release the LOAD MEMORY switch.

(5) Set the SWITCH REGISTER to 164000 (LDB, I) and press and release the LOAD MEMORY switch.

(6) Set the SWITCH REGISTER to 026000 (JMP) and press and release the LOAD MEMORY switch.

(7) Set the SWITCH REGISTER to 177777, and in turn, press and release the LOAD A switch and the LOAD B switch.

(8) Set the SWITCH REGISTER to 004000 (the starting address of test program), and press and release the LOAD ADDRESS switch. Then proceed to step "v".

v. Refer to table 4-2. While observing the front panel for the indications specified in the table, press and release the SINGLE CYCLE switch exactly nine times. If all indications are normal, proceed to step "w". If an indication associated with the FETCH, INDIRECT, or EXECUTE indicators is abnormal, refer to paragraph 4-164 and troubleshoot the phase logic circuits. If an indication associated with either the A-REGISTER ACCUMULATOR display or the B-REGISTER ACCUMULATOR display is abnormal, determine which instruction failed to process. Then refer to the listing for the instruction in table 4-8 for applicable troubleshooting references.

w. Check the M-REGISTER MEMORY ADDRESS display for an indication of 004000 (the starting address used for test program at step "u" (1) above). If the indication is normal, proceed to step "x". If the indication is abnormal, refer to the listing for the JMP instruction in table 4-8 for further troubleshooting references.

Table 4-2. Phase Logic Indicators, Checkout and Trouble Analysis

TIMES SINGLE CYCLE SWITCH IS PRESSED	CIRCUIT ACTION	INDICATION AT FRONT PANEL				
		FETCH INDICATOR	INDIRECT INDICATOR	EXECUTE INDICATOR	A-REGISTER ACCUMULATOR DISPLAY	B-REGISTER ACCUMULATOR DISPLAY
0	Initial indication.	On	Off	Off	177777	177777
1	Fetch and execute CLA instruction and set phase 1.	On	Off	Off	000000	177777
2	Fetch LDA instruction and set phase 3.	Off	Off	On	000000	177777
3	Execute LDA instruction and set phase 1.	On	Off	Off	177777	177777
4	Fetch and execute CLB instruction and set phase 1.	On	Off	Off	177777	000000
5	Fetch LDB, I instruction and set phase 2.	Off	On	Off	177777	000000
6	Set indirect address and set phase 2.	Off	On	Off	177777	000000
7	Set phase 3.	Off	Off	On	177777	000000
8	Execute LDB, I instruction and set phase 1.	On	Off	Off	177777	177777
9	Fetch and execute JMP instruction and set phase 1.	On	Off	Off	177777	177777

x. Press and release the RUN switch and check that the RUN indicator goes on and the HALT indicator goes off. If the indication is normal, proceed to step "y". If the indication for either the RUN or the HALT indicator is abnormal, refer to paragraph 4-71 and troubleshoot the circuits associated with the RUN switch and RUN indicator.

y. Press and release the HALT switch and check that the RUN indicator goes off and the HALT indicator goes on. If the indication is normal, proceed to step "z". If the indication for either the RUN or the HALT indicator is abnormal, refer to paragraph 4-76 and troubleshoot the circuits associated with the HALT switch and HALT indicator.

z. If all indications in the preceding steps were normal, slide the card cage into the cabinet and close the door assembly. Then refer to paragraph 4-17 and perform the diagnostic checkout procedure.

4-17. DIAGNOSTIC CHECKOUT.

4-18. GENERAL.

4-19. Diagnostic checkout consists of running a series of test programs that automatically perform a dynamic test of computer operation by exercising major portions of the circuit functions in the control, arithmetic, memory, and input/output sections. The diagnostic checkout test procedure should be conducted immediately after the computer is installed, and as required thereafter as part of a regularly scheduled preventive maintenance program, during troubleshooting, and after making repairs or modifications to the computer. Perform the basic checkout procedure (paragraph 4-9) before attempting the diagnostic checkout procedure to ensure that the computer is capable of loading, storing, and processing diagnostic test programs. Then refer to paragraphs 4-20 through 4-37 for information and instructions applicable to performing the diagnostic test procedure.

4-20. REQUIRED DOCUMENTATION AND TAPES.

4-21. Diagnostic test programs are supplied in absolute form on punched paper tapes. Before a tape reading device can be used to read the test programs from these tapes and input the instructions and data into the memory locations assigned to the program, an absolute loader program must be stored in the protected area of computer memory (the uppermost 64 memory locations). Procedures for verifying program instructions located in the protected area of memory, for loading required instructions into the protected area of memory, and for using Hewlett-Packard input devices to load absolute programs from punched paper tapes are included in paragraphs 4-23 through 4-34.

4-22. The diagnostic tests used for checking the circuits of the basic computer are listed in table 4-3. This table also lists the part numbers of the diagnostic program procedures (contained in the Manual of Diagnostics) and the corresponding diagnostic program tapes required for performing these tests. Diagnostic test procedures and tapes used for checking optional processing and interface circuits installed in the computer are referenced in the operating and service manual for the particular option. After locating the required documents and tapes listed in table 4-3, refer to the test procedure given in paragraph 4-35. A thorough knowledge of the reference information presented in paragraphs 4-23 through 4-34 is essential when performing the test procedure.

Note

The letter which follows program tape part numbers identifies a particular revision of the tape and is subject to change. Always use the latest revision of a program tape even if different from that specified in table 4-3, together with the appropriate diagnostic program procedure contained in the Manual of Diagnostics.

Table 4-3. Diagnostic Program Tapes and Procedures for Testing the Basic Computer

TEST	PROGRAM TAPE PART NO.	PROGRAM PROCEDURE PART NO.
Alter-Skip Instruction Test	20400A	02116-91761
Memory Reference Instruction Test	20401B	02116-91762
Shift-Rotate Instruction Test	20402D	02116-91763
High Memory Address Test	20404A	02116-91764
Low Memory Address Test	20403A	02116-91765
High Memory Checkerboard Test	20426A	02116-91766
Low Memory Checkerboard Test	20427A	02116-91767
Interrupt Test	20415A	02116-91768
*Power Fail Interrupt Test	20434B	02116-91759

*Use the Power Fail With Auto Restart Test (program tape part no. 20428A and program procedure part no. 02116-91769) in place of this test if option 008 is installed in the computer.

4-23. ABSOLUTE LOADER PROGRAMS.

4-24. DESCRIPTION. Absolute loader programs are stored in the computer's memory for the purpose of loading other programs that are in absolute form, such as those produced by the Assembler or the Basic Control System absolute output option. They are also used for loading standard software systems that are in absolute form (e.g., FORTRAN, ALGOL, Assembler, Basic Control System, and Symbolic Editor).

4-25. STORAGE. Absolute loader programs are stored in the protected area of memory (the highest 64 locations). Tables 4-4 and 4-5 contain octal listings of program instructions for two absolute loader programs, either of which may be present in these locations.

4-26. PROGRAM LISTINGS. Table 4-4 contains the listing for the standard Basic Binary Loader (BBL) program. Table 4-5 contains the listing for the Basic Binary Disc Loader (BBDL) program. Except as specified in paragraph 4-30, both loader programs perform essentially the same function, and either program may be used for loading the diagnostic test programs listed in table 4-3. However, only the BBDL program can be used for loading programs written exclusively for a disc memory device. Therefore, in computer systems employing a disc memory, the BBDL program must be stored in the protected area of the computer's memory.

4-27. LOADING PROCEDURE. To load program instructions into the protected area of memory, refer to table 4-4 or 4-5, whichever is applicable, and proceed as follows:

Note

Be sure to use the proper values for the variables listed in table 4-4 or 4-5.

a. Set the LOADER switch to ENABLED.

b. Enter the address of the instruction into the SWITCH REGISTER.

c. Press and release the LOAD ADDRESS switch.

d. Enter the instruction into the SWITCH REGISTER.

e. Press and release the LOAD MEMORY switch.

f. Repeat steps "b" through "e" for each instruction loaded. (Steps b and c can be omitted if loading into consecutive memory locations.) Then set the LOADER switch to PROTECTED and perform the verification procedure presented in the following paragraph.

4-28. VERIFICATION PROCEDURE. To verify the instructions stored in the protected area of memory, refer to table 4-4 or 4-5, whichever is applicable, and proceed as follows:

a. Enter the address of the instruction to be verified into the SWITCH REGISTER.

b. Press and release the LOAD ADDRESS switch.

c. Set the LOADER switch to ENABLED.

Table 4-4. Listing of Absolute Instructions for Basic Binary Loader (BBL) Program

ADDRESS	0	1	2	3	4	5	6	7
0m7700:	107700	063770	106501	004010	002400	006020	063771	073736
0m7710:	006401	067773	006006	027717	107700	102077	027700	017762
0m7720:	002003	027712	003104	073774	017762	017753	070001	073775
0m7730:	063775	043772	002040	027751	017753	044000	dddddd	002101
0m7740:	102000	037775	037774	027730	017753	054000	027711	102011
0m7750:	027700	102055	027700	dddddd	017762	001727	073776	017762
0m7760:	033776	127753	dddddd	1037cc	1023cc	027764	1025cc	127762
0m7770:	173775	153775	1n0100	177765	dddddd	dddddd	dddddd	dddddd

Variables:
m = 1 for 8K, 3 for 16K, 5 for 24K, 7 for 32K memory
n = 6 for 8K, 4 for 16K, 2 for 24K, 0 for 32K memory
cc = punched tape reader or teleprinter address
dddddd = indeterminable (Load all zeros in memory locations designated "indeterminable" when loading the BBL per paragraph 4-27. Disregard as insignificant the content of memory locations designated as "indeterminable" when verifying the BBL per paragraph 4-28.)

Table 4-5. Listing of Absolute Instructions for Basic Binary Disc Loader (BBDL) Program

ADDRESS	0	1	2	3	4	5	6	7
0m7700:	107700	002401	063726	006700	017742	007306	027713	002006
0m7710:	027703	102077	027700	077754	017742	017742	074000	077757
0m7720:	067757	047755	002040	027740	017742	040001	177757	037757
0m7730:	000040	037754	027720	017742	054000	027702	102011	027700
0m7740:	102055	027700	dddddd	006600	1037cc	1023cc	027745	1074cc
0m7750:	002041	127742	005767	027744	dddddd	1n0100	0200zz	dddddd
0m7760:	107700	063756	102606	002700	1026qq	001500	102602	063777
0m7770:	102702	102602	103706	1027zz	067776	074077	024077	177700

Variables:
m = 1 for 8K, 3 for 16K, 5 for 24K, 7 for 32K memory
zz = first disc channel
qq = second disc channel
cc = punched tape reader or teleprinter address
n = 6 for 8K, 4 for 16K, 2 for 24K, 0 for 32K memory
dddddd = indeterminable (Load all zeros in memory locations designated "indeterminable" when loading the BBDL per paragraph 4-27. Disregard as insignificant the content of memory locations designated as "indeterminable" when verifying the BBDL per paragraph 4-28.)

d. Press and release the DISPLAY MEMORY switch. The content of the memory location selected in step "a" above is now indicated by the T-REGISTER MEMORY DATA display. Each time the DISPLAY MEMORY switch is pressed and released, the content of the next consecutive memory location is displayed. Because the M-register is incremented by one each time the DISPLAY MEMORY switch is pressed, the address indicated by the M-REGISTER MEMORY ADDRESS display is always one address higher than the address of the data currently displayed by the T-REGISTER indicators.

e. Set the LOADER switch to PROTECTED after all desired locations in the protected area of memory have been displayed.

4-29. PROCEDURES FOR LOADING PROGRAMS STORED ON PAPER TAPE. Typical Hewlett-Packard input configurations that can be used in conjunction with the BBL or BBDL loader programs to read program instructions and data from punched paper tapes and transfer it into the computer memory are as follows:

a. HP 2737A Punched Tape Reader interfaced through the HP 12532A High-Speed Punched Tape Input Interface option.

b. HP 2748A Punched Tape Reader interfaced through the HP12597A-02 Tape Reader Interface option.

c. HP 2758A Punched Tape Reader interfaced through the HP12597A-02 Tape Reader Interface option.

d. HP 2752A Teleprinter interfaced through the HP 12531B Teleprinter Input/Output Interface option.

4-30. If one of the punched tape reader configurations ("a" through "c" above) is used in conjunction with the BBL loader program, three loading options can be selected. These options, and the settings required for bits 0 and 15 of the SWITCH REGISTER to select them, are specified in table 4-6. Only the "load tape" option can be selected for the punched tape reader configurations ("a" through "c" above) if the BBDL loader program is used, and for the teleprinter configuration ("d" above) regardless of which loader program is used.

4-31. General procedures for using the HP 2737A and 2752A to load programs from punched paper tapes are presented in paragraphs 4-32 and 4-33. Refer to the operating and service manual for the HP 2748A (manual part no. 02748-90023) or the HP 2758A (manual part no. 02758-90173) for specific operating instructions if these devices are used for loading.

4-32. HP 2737A Punched Tape Reader. If using the HP 2737A Punched Tape Reader to load program tapes, proceed as follows:

a. At the punched tape reader, set the POWER switch to ON.

b. Place the RUN/LOAD lever in the LOAD position.

c. Carefully position the program tape in the tape reading mechanism and place the RUN/LOAD lever in the RUN position.

Note

The address specified in step "d" following applies when loading the test programs listed in table 4-3, but may differ for other programs. Check the documentation applicable to the program being loaded for the correct address when performing this step. (The letter "m" in the address is a variable which is defined in tables 4-4 and 4-5.)

d. Enter 0m7700 (the starting address of the absolute loader program) into the SWITCH REGISTER. Then press the LOAD ADDRESS switch.

e. Refer to table 4-6 and enter the appropriate settings for bits 0 and 15 into the SWITCH REGISTER. Set the LOADER switch to ENABLED. Then, in turn, press and release the PRESET and RUN switches. The computer should go into the run mode (RUN indicator on) and the program tape should process through the tape reading mechanism of the punched tape reader. When the computer halts (RUN indicator off, HALT indicator on), set the LOADER switch to PROTECTED, and check the T-REGISTER MEMORY DATA indicators. If the program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program loading, refer to table 4-7.) If the indication is normal, proceed with the applicable instructions for running the program now in memory. If the indication is abnormal, refer to table 4-7 and proceed as directed.

Table 4-6. Punched Tape Reader Loading Options

OPTION	SWITCH REGISTER SETTINGS	
	Bit 15	Bit 0
Load tape	0	0
*Verify checksum without loading	0	1
*Compare the contents of the tape with the contents of memory without loading	1	0/1

*Selectable only in configurations using the HP 2737A, 2748A, or 2758A Punched Tape Reader in conjunction with the BBL loader program.

Note

If the computer does not automatically halt when the end of the tape is read by the reader, and the reader feed mechanism continues operating and feeds the tape completely through the reader (rather than stopping with the end of the tape retained in the reader), press and release the HALT switch at the front panel of the computer. Then check the loader program in the protected area of memory using the procedure given in paragraph 4-28. If the loader program is correct, refer to paragraph 4-392 and troubleshoot the circuits that process the halt instruction.

f. After loading, remove the tape from the reader, rewind it, and return it to the appropriate storage box.

4-33. HP 2752A Teleprinter. If using the teleprinter to load program tapes, proceed as follows:

a. At the teleprinter, set the LINE/OFF/LOCAL switch to LINE.

b. Carefully position the program tape in the teleprinter tape reader.

c. Set the START/STOP/FREE switch to START.

Note

The address specified in step "d" following applies when loading the test programs listed in table 4-3, but may differ for other programs. Check the documentation applicable to the program being loaded for the correct address when performing this step. (The letter "m" in the address is a variable which is defined in tables 4-4 and 4-5.)

d. At the computer front panel, enter 0m7700 (the starting address of the absolute loader program) into the SWITCH REGISTER and press the LOAD ADDRESS switch. Set the LOADER switch to ENABLED, then, press the PRESET and RUN switches. The computer should go into the run mode (RUN indicator on) and the program tape should process through the tape reader of the teleprinter. When the computer halts (RUN indicator off, HALT indicator on), set the LOADER switch to PROTECTED, and check the T-REGISTER MEMORY DATA indicators. If the test program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program loading, refer to table 4-7.) If the indication is normal, proceed with the applicable instructions for running the program now in memory. If the indication is abnormal, refer to table 4-7 and proceed as directed.

Note

If the computer does not automatically halt when the end of the tape is read by the reader, and the reader feed mechanism continues operating and feeds the tape completely through the reader (rather than stopping with the end of the tape retained in the reader), press and release the HALT switch at the front panel of the computer. Then check the loader program in the protected area of memory using the procedure given in paragraph 4-28. If the loader program is correct, refer to paragraph 4-392 and troubleshoot the circuits that process the halt instruction.

e. At the teleprinter, set the START/STOP/FREE switch to STOP, remove the tape from the reader, rewind, and return it to the appropriate storage box.

4-34. LOADING HALTS. After all program data is read from a test tape and transferred into memory, the associated tape reader and the computer will halt with a normal indication of 102077 (end-of-tape condition) displayed by the T-REGISTER MEMORY DATA indicators. This signals the operator to continue with the applicable procedure for running the program now stored in memory. If a halt occurs while a tape is being loaded and an indication other than 102077 is displayed, refer to table 4-7 and proceed as directed.

4-35. TEST PROCEDURE.

4-36. TEST SEQUENCE. The diagnostic checkout procedure for the basic computer is performed using the diagnostic program tapes and procedures listed in table 4-3.

Table 4-7. Loading Halts

T-REGISTER MEMORY DATA DISPLAY	EXPLANATION	REQUIRED ACTION
102077	End-of-tape. Ten consecutive feed frames have been detected and interpreted as an end-of-tape condition.	This indication is normal. Proceed with the applicable procedure for running the program which was loaded into the computer memory.
102011	Checksum error. The A-register contains the checksum from the tape. The B-register contains the computed checksum.	Using the procedures given in paragraphs 4-29 through 4-33, as applicable, reload the program into computer memory. Then execute the checksum option again. If a checksum error still occurs, check the program and/or the computer for the cause of the error.
102055	Address error. An attempt has been made to destroy the loader program, or to load outside the memory limits.	Using the procedures given in paragraphs 4-29 through 4-33, as applicable, recheck all steps and attempt to load the program again. If an address error still occurs, check the program and/or the computer for the cause of the error.
102000	Compare error. The tape being read does not compare with memory. The A-register contains the word from the tape which did not agree.	To find the address of the word in memory which did not compare with the word in the A-register, press the SINGLE CYCLE switch twice. The contents of the T-register, minus one, is the address of the word. Using the procedures given in paragraphs 4-29 through 4-33, as applicable, reload the program into computer memory. Then execute the compare option again. If a compare error still occurs, check the program and/or the computer for the cause of the error.

Using the referenced procedures (located in the Manual of Diagnostics) load and run, in sequence, the alter-skip, memory reference, and shift-rotate test programs. Then load and run, in any desired order, the remaining test programs listed in table 4-3, followed by the test programs for any optional processing and interface circuits installed in the computer. If all test programs are run without error, the computer is ready to resume normal operation.

4-37. ERROR HALTS. If an error halt is encountered in the course of running a diagnostic test program, use the information presented in the diagnostic program procedure to determine which instruction, or sequence of instructions, in the program was not processed by the computer. Then refer to the information presented in table 4-8 of this section for references to applicable circuit level troubleshooting information.

4-38. TROUBLESHOOTING REFERENCE INFORMATION.

4-39. GENERAL.

4-40. Troubleshooting reference information consists of data and diagrams that are used for analyzing and localizing trouble symptoms experienced during checkout. Effective use of this information facilitates isolating the trouble to a replaceable or repairable assembly or part, making the required repair, and preparing the computer for return to service. The purpose and use of this information, consisting of the following items, is described in paragraphs 4-41 through 4-59:

a. Program instruction formats.

b. Program instruction index and troubleshooting reference guide.

c. Logic equations.

d. Circuit descriptions and test procedures.

e. Troubleshooting diagrams.

f. Information in other sections of this manual.

g. Information in other manuals.

4-41. PROGRAM INSTRUCTION FORMATS.

4-42. Program instruction formats are shown in figure 4-1. This figure summarizes information needed for using machine language to program the computer. Bit patterns are shown for the basic instruction set which is comprised of memory reference instructions, input/output instructions, register reference instructions in the shift-rotate group (SRG), and register reference instructions in the alter-skip group (ASG). For detailed information on machine language programming, refer to Volume One, the Specifications and Basic Operation Manual (manual part no. 02116-9152) for the computer.

4-43. PROGRAM INSTRUCTION INDEX AND TROUBLESHOOTING REFERENCE GUIDE.

4-44. The program instruction index and troubleshooting reference guide is presented in table 4-8. This table consists of an alphabetical listing, by mnemonic, of the instructions comprising the basic instruction set for the computer. The main purpose of this table is to provide references to the circuit level troubleshooting data within this section of the manual that applies to the instructions listed. In addition, table 4-8 lists the type, definition, and a brief descriptive summary for each instruction. For more detailed information on each instruction, refer to the paragraph and figure listed in the "REFERENCES" column of the table, and to Volume One, the Specifications and Basic Operation Manual (manual part no. 02116-9152) for the computer.

4-45. LOGIC EQUATIONS.

4-46. Logic equations are presented in table 4-9. The equations express the input signal conditions that are required to produce a given output signal. Output signals are listed alphanumerically, by mnemonic, in the "SIGNAL" column. (Signal mnemonics are defined in table 5-7). Two operators are used in the "EQUATION" column. A "+" is used to indicate a logical "or" condition and a "*" is used to indicate a logical "and" condition. For example, the expression C = A+B states that if either A or B is true, then C is true. (The exclusive "or" condition is not used in expressing these equations.) The expression C = A*B states that if both A and B are true, then C is true. A bar over a term is used to indicate a logical inverse or negative quantity.

4-47. For clarity, the equations are expressed with a minimum of "or" terms. Instead, each "or" term in an equation is preceded by an equals sign, rather than a "+" operator, and expressed as a separate equation (refer to the equations for signal ADF as an example). When several equations are presented for a given signal, such as ADF, any one of the equated conditions can produce the signal. It should be noted that the equations are in a reduced form for use in troubleshooting and do not necessarily reflect the logic design of the computer.

Note

Text continues on page 4-39

BASIC INSTRUCTION FORMATS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	D/I	INSTRUCTION				Z/C	MEMORY ADDRESS									
2	REG REF. GROUP				REGISTER MICROINSTRUCTIONS											
3	I/O GROUP				INSTRUCTION						SELECT CODE					

1 MEMORY REFERENCE INSTRUCTIONS
2 REGISTER REFERENCE INSTRUCTIONS
3 INPUT/OUTPUT INSTRUCTIONS

BASIC INSTRUCTION SET

TYPE	MNEMONIC	DESCRIPTION
Memory Reference	AND	"And" (M) to A; result in A
	XOR	"Exclusive or" (M) to A; result in A
	IOR	"Inclusive or" (M) to A; result in A
	JSB	Jump to subroutine, save P
	JMP	Jump, unconditionally
	ISZ	Increment (M); skip if result zero
	ADA/B	Add (M) to A or B; result in A or B
	CPA/B	Compare (M) with A or B, skip if unequal
	LDA/B	Load (M) into A or B
	STA/B	Store A or B into M; A/B unchanged
Register Reference		SHIFT-ROTATE GROUP
	NOP	No operation
	CLE	Clear E (Extend)
	SLA/B	Skip if least significant bit of A/B is zero
	A/BLS	A/B arithmetic left shift one bit
	A/BRS	A/B arithmetic right shift one bit
	RA/BL	Rotate A/B left one bit
	RA/BR	Rotate A/B right one bit
	A/BLR	A/B left shift one bit, sign cleared
	ERA/B	Rotate E right one bit with A or B
	ELA/B	Rotate E left one bit with A or B
	A/BLF	Rotate A or B left four bits
		ALTER-SKIP GROUP
	CLA/B	Clear A or B
	CMA/B	Complement A/B (ones complement)
	CCA/B	Clear-complement A/B (set to -1)
	CLE	Clear E (Extend)
	CME	Complement E
	CCE	Clear-complement E (set E)
	SEZ	Skip if E is zero
	SSA/B	Skip if sign of A/B is zero (positive)
	SLA/B	Skip if least significant bit of A/B is zero
	INA/B	Increment A/B by one
	SZA/B	Skip if A/B is zero
	RSS	Reverse skip sense
Input/Output		OVERFLOW
	STO	Set overflow bit
	CLO	Clear overflow bit
	SOC	Skip if overflow bit clear
	SOS	Skip if overflow bit set
	HLT	Halt program
	STF	Set flag bit of selected I/O channel
	CLF	Clear flag of selected I/O channel
	SFC	Skip if flag clear
	SFS	Skip if flag set
	MIA/B	Merge ("or") I/O channel into A/B
	LIA/B	Load I/O channel into A/B
	OTA/B	Output A/B to I/O channel
	STC	Set control bit of selected channel
	CLC	Clear control bit of selected channel

- (M) = Contents of Memory Location M
- Overflow instructions are coded under I/O group

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MEMORY REFERENCE INSTRUCTIONS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D/I	INSTRUCTION				Z/C	MEMORY ADDRESS									
AND		0	0	1	0											
XOR		0	1	0	0											
IOR		0	1	1	0											
JSB		0	0	1	1											
JMP		0	1	0	1											
ISZ		0	1	1	1											
ADA		1	0	0	0											
ADB		1	0	0	1											
CPA		1	0	1	0											
CPB		1	0	1	1											
LDA		1	1	0	0											
LDB		1	1	0	1											
STA		1	1	1	0											
STB		1	1	1	1											

TRUTH TABLE

	AND	XOR	IOR
A Contents	0 0 1 1	0 0 1 1	0 0 1 1
Memory	0 1 0 1	0 1 0 1	0 1 0 1
Result (in A)	0 0 0 1	0 1 1 0	0 1 1 1

1 = True, 0 = False

INPUT/OUTPUT INSTRUCTIONS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE 3				A/B	*	H/C	INSTRUCTION			SELECT CODE					
MAC	1	0	0	0		0										
HLT	1	0	0	0		1		0	0	0						
STF	1	0	0	0		1	0	0	0	1						
CLF	1	0	0	0		1	1	0	0	1						
SFC	1	0	0	0		1	0	0	1	0						
SFS	1	0	0	0		1	0	0	1	1						
MIA	1	0	0	0	0	1		1	0	0						
MIB	1	0	0	0	1	1		1	0	0						
LIA	1	0	0	0	0	1		1	0	1						
LIB	1	0	0	0	1	1		1	0	1						
OTA	1	0	0	0	0	1		1	1	0						
OTB	1	0	0	0	1	1		1	1	0						
STC	1	0	0	0	0	1		1	1	1						
CLC	1	0	0	0	1	1		1	1	1						
STO	1	0	0	0		1	0	0	0	1	0	0	0	0	0	1
CLO	1	0	0	0		1	1	0	0	1	0	0	0	0	0	1
SOC	1	0	0	0		1		0	1	0	0	0	0	0	0	1
SOS	1	0	0	0		1		0	1	1	0	0	0	0	0	1

* Identifies Macroinstructions (0) or standard Input/Output instructions (1).

Figure 4-1. Program Instruction Formats
(Sheet 1 of 2)

Register Reference Instructions (Shift-Rotate Group)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE 2				A/B	0	D/E	COL 1			2	D/E	3	COL 4		
NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CLE	0	0	0	0		0					1					
SLA	0	0	0	0	0	0							1			
SLB	0	0	0	0	1	0							1			
ALS	0	0	0	0	0	0	1	0	0	0		X		X	X	X
BLS	0	0	0	0	1	0	1	0	0	0		X		X	X	X
ARS	0	0	0	0	0	0	1	0	0	1		X		X	X	X
BRS	0	0	0	0	1	0	1	0	0	1		X		X	X	X
RAL	0	0	0	0	0	0	1	0	1	0		X		X	X	X
RBL	0	0	0	0	1	0	1	0	1	0		X		X	X	X
RAR	0	0	0	0	0	0	1	0	1	1		X		X	X	X
RBR	0	0	0	0	1	0	1	0	1	1		X		X	X	X
ALR	0	0	0	0	0	0	1	1	0	0		X		X	X	X
BLR	0	0	0	0	1	0	1	1	0	0		X		X	X	X
ERA	0	0	0	0	0	0	1	1	0	1		X		X	X	X
ERB	0	0	0	0	1	0	1	1	0	1		X		X	X	X
ELA	0	0	0	0	0	0	1	1	1	0		X		X	X	X
ELB	0	0	0	0	1	0	1	1	1	0		X		X	X	X
ALF	0	0	0	0	0	0	1	1	1	1		X		X	X	X
BLF	0	0	0	0	1	0	1	1	1	1		X		X	X	X

SELECTION TABLE

1	2	3	4
ALS ARS RAL RAR ALR ERA ELA ALF	CLE	SLA	ALS ARS RAL RAR ALR ERA ELA ALF
BLS BRS RBL RBR BLR ERB ELB BLF	CLE	SLB	BLS BRS RBL RBR BLR ERB ELB BLF

COMBINING GUIDE

1. Choose up to 4 instructions, one from each column of the Selection Table.
2. Use a one-bit for Bit 9 to Enable column 1 instructions, and a one-bit for Bit 4 to Enable column 4 instructions. Figure above shows column 1 enabled (executed first) with duplicate column 4 pattern (executed last) indicated by X's.
3. Use a one-bit for Bit 5 to select column 2 (CLE), or a zero-bit to exclude CLE.
4. Use a one-bit for Bit 3 to select column 3 (SLA/B), or a zero-bit to exclude SLA/B.

Register Reference Instructions (Alter-Skip Group)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE 2				A/B	1	COL 1		COL. 3		2	4	5	6	7	8
CLA	0	0	0	0	0	1	0	1								
CLB	0	0	0	0	1	1	0	1								
CMA	0	0	0	0	0	1	1	0								
CMB	0	0	0	0	1	1	1	0								
CCA	0	0	0	0	0	1	1	1								
CCB	0	0	0	0	1	1	1	1								
SEZ	0	0	0	0		1					1					
CLE	0	0	0	0		1			0	1						
CME	0	0	0	0		1			1	0						
CCE	0	0	0	0		1			1	1						
SSA	0	0	0	0	0	1						1				
SSB	0	0	0	0	1	1						1				
SLA	0	0	0	0	0	1							1			
SLB	0	0	0	0	1	1							1			
INA	0	0	0	0	0	1								1		
INB	0	0	0	0	1	1								1		
SZA	0	0	0	0	0	1									1	
SZB	0	0	0	0	1	1									1	
RSS	0	0	0	0		1										1

SELECTION TABLE

1	2	3	4	5	6	7	8
CLA CMA CCA	SEZ	CLE CME CCE	SSA	SLA	INA	SZA	RSS
CLB CMB CCB	SEZ	CLE CME CCE	SSB	SLB	INB	SZB	RSS

COMBINING GUIDE

1. Choose up to 8 instructions, one from each column of the Selection Table.
2. Use the specified two-bit combinations of Bits 9 and 8, plus A/B Bit 11, to encode column 1 instructions.
3. Use the specified two-bit combinations of Bits 7 and 6 to encode column 3 instructions.
4. Use a one-bit in Bits 5, 4, 3, 2, 1, plus A/B Bit 11, to encode column 2, 4, 5, 6, 7 instructions respectively.
5. Use a one-bit for Bit 0 to encode column 8.

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Figure 4-1 Program Instruction Formats
(Sheet 2 of 2)

Table 4-8. Program Instruction Index and Troubleshooting Reference Guide

INSTRUCTION MNEMONIC	INSTRUCTION TYPE	DEFINITION AND DESCRIPTION	REFERENCES PARA-GRAPH	REFERENCES FIGURE
ADA	Memory Reference	Add to A-Register. The contents of the addressed memory location are added to the contents of the A-register. The sum is stored in the A-register, and the contents of the memory location are unaltered. The result of the addition may set the Extend FF or Overflow FF.	4-233	4-42
ADB	Memory Reference	Add to B-Register. The contents of the addressed memory location are added to the contents of the B-register. The sum is stored in the B-register, and the contents of the memory location are unaltered. The result of the addition may set the Extend FF or Overflow FF.	4-233	4-42
ALF	Register Reference (SRG)	Rotate all A-Register bits Left Four places. The bits in positions 15, 14, 13, and 12 are rotated around into bit positions 3, 2, 1, and 0, respectively. This is equivalent to four successive RAL instructions.	4-317	4-56
ALR	Register Reference (SRG)	Shift A-Register bits 0 through 14 Left one place, arithmetically, and clear the sign bit. Bit position 0 is cleared, and the bit shifted out of position 14 is lost. Bit position 15 (sign bit) is cleared.	4-299	4-53
ALS	Register Reference (SRG)	Shift A-Register bits 0 through 14 Left one place, arithmetically. Bit position 0 is cleared, and the bit shifted out of bit position 14 is lost. Bit position 15 (sign bit) is not affected.	4-275	4-49
AND	Memory	"And" to A-Register. The contents of the addressed memory location are logically "anded" to the contents of the A-register. The result is stored in the A-register, and the contents of the memory location are unaltered.	4-195	4-36
ARS	Register Reference (SRG)	Shift A-Register bits 0 through 15 Right one place, arithmetically. The bit shifted out of position 0 is lost. The bit value of position 15 (sign (sign bit) is shifted into position 14, but the bit in position 15 is unaltered.	4-281	4-50
BLF	Register Reference (SRG)	Rotate all B-Register bits Left Four places. The bits in positions 15, 14, 13, and 12 are rotated around into bit positions 3, 2, 1, and 0, respectively. This is equivalent to four successive RAL instructions.	4-317	4-56

Table 4-8. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA-GRAPH	FIGURE
BLR	Register Reference (SRG)	Shift B-Register bits 0 through 14 Left one place, arithmetically, and clear the sign bit. Bit position 0 is cleared, and the bit shifted out of position 14 is lost. Bit position 15 (sign bit) is cleared.	4-299	4-53
BLS	Register Reference (SRG)	Shift B-Register bits 0 through 14 Left one place, arithmetically. Bit position 0 is cleared, and the bit shifted out of bit position 14 is lost. Bit position 15 (sign bit) is not affected.	4-275	4-49
BRS	Register Reference (SRG)	Shift B-Register bits 0 through 15 Right one place, arithmetically. The bit shifted out of position 0 is lost. The bit value of position 15 (sign bit) is shifted into position 14, but the bit in position 15 is unaltered.	4-281	4-50
CCA	Register Reference (ASG)	Clear then Complement A-Register. Clears all 16 bit positions to zeros and then loads ones in all 16 bit positions. (This is the two's complement form of -1).	4-333	4-59
CCB	Register Reference (ASG)	Clear then Complement B-Register. Clears all 16 bit positions to zeros and then loads ones in all 16 bit positions. (This is the two's complement form of -1).	4-333	4-59
CCE	Register Reference (ASG)	Clear then Complement E-Register. Clears and then sets the Extend FF.	4-349	4-62
CLA	Register Reference (ASG)	Clear A-Register. Clears all 16 bit positions to zero.	4-323	4-57
CLB (ASG)	Register Reference (ASG)	Clear B-Register. Clears all 16 bit positions to zero.	4-323	4-57
CLC	Input/Output	Clear Control bit on the I/O channel addressed by the select code. Clears the Control FF on the interface card residing in the addressed I/O channel to prevent the external device from interrupting. A CLC instruction addressed to select code 00 (octal) clears all Control FFs, effectively inhibiting all external devices from interrupting. A CLF instruction (see below) can be combined with the CLC instruction.	4-436	4-76

Table 4-8. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA-GRAPH	FIGURE
CLE	Register Reference (SRG and ASG)	Clear E-Register. Clears the Extend FF.	4-264 and 40339	4-47 and 4-60
CLF	Input/Output	Clear Flag bit on the I/O channel addressed by the select code. Clears the Flag FF on the interface card residing in the addressed I/O channel to permit the external device to send a flag signal when ready. A CLF instruction addressed to select code 00 (octal) clears the Interrupt System Enable FF to disable the entire interrupt system, but does not affect the status of the Flag FFs on the individual interface cards.	4-403	4-70
CLO	Input/Output	Clear overflow Register. Clears the Overflow FF.	4-446	4-78
CMA	Register Reference (ASG)	Complement A-Register. Reverses the state of all 16 bit positions.	4-328	4-58
CMB	Register Reference (ASG)	Complement B-Register. Reverses the state of all 16 bit positions.	4-328	4-58
CME	Register Reference (ASG)	Complement E-Register. Reverses the state of the Extend FF.	4-344	4-61
CPA	Memory Reference	Compare to A-Register, skip if unequal. The contents of the addressed memory location are compared with the contents of the A-register. If the two 16-bit words are different, the P- and M-registers are incremented by two instead of one, and the next instruction in the program sequence is skipped. If the two words are identical, the P- and M-registers are incremented by one, and the program proceeds normally to the next instruction in sequence. The contents of neither the A-register nor the addressed memory location are altered.	4-239	4-43
CPB	Memory	Compare to B-Register, skip if unequal. The contents of the addressed memory location are compared with the contents of the B-register. If the two 16-bit words are different, the P- and M-registers are incremented by two instead of one, and the next instruction in the program sequence is skipped. If the two words are identical, the P- and M-registers are incremented by one, and the program proceeds normally to the next instruction in sequence. The contents of neither the A-register nor the addressed memory location are altered.	4-239	4-43

Table 4-8. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA-GRAPH	FIGURE
ELA	Register Reference SRG)	Rotate E-Register Left with A-Register, one place. The bit in position 15 of the A-register is rotated into the Extend FF. The Extend FF bit is rotated into bit position 0 of the A-register.	4-311	4-55
ELB	Register Reference (SRG)	Rotate E-Register Left with B-Register, one place. The bit in position 15 of the B-register is rotated into the Extend FF. The Extend FF bit is rotated into bit position 0 of the B-register.	4-311	4-55
ERA	Register Reference (SRG)	Rotate E-Register Right with A-Register, one place. The bit in position 0 of the A-register is rotated into the Extend FF. The Extend FF bit is rotated into bit position 15 of the A-register.	4-305	4-54
ERB	Register Reference (SRG)	Rotate E-Register Right with B-Register, one place. The bit is position 0 of the B-register is rotated into the Extend FF. The Extend FF bit is rotated into bit position 15 of the B-register.	4-305	4-54
HLT	Input/Output	Halt. Stops the computer and holds or clears the Flag FF on the interface card residing in the addressed I/O channel. Execution of this instruction has the same effect as pressing and releasing the HALT switch (the HALT indicator goes on, all front panel control switches are enabled, and no interrupts can occur.) The HLT instruction word will be displayed in the T-register, and the P-register will indicate the halt memory location plus one.	4-392	4-68
INA	Register Reference (ASG)	Increment A-Register by one. Steps the count held in the A-register by one. The result of this operation may set the Extend FF or Overflow FF.	4-372	4-66
INB	Register Reference (ASG)	Increment B-Register by one. Steps the count held in the A-register by one. The result of this operation may set the Extend FF or Overflow FF.	4-372	4-66
IOR	Memory Reference	Inclusive "Or" to A-Register. The contents of the addressed memory location are combined with the contents of the A-register by an inclusive "or" logic operation. The result is stored in the A-register, and the contents of the addressed memory location are unaltered.	4-207	4-38

Table 4-8. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION MNEMONIC	INSTRUCTION TYPE	DEFINITION AND DESCRIPTION	REFERENCES PARA-GRAPH	REFERENCES FIGURE
ISZ	Memory Reference	Increment and Skip if Zero. The count stored in the addressed memory location is stepped by one. If as a result of this operation the count in the memory location advances to zero, the P- and M-registers are incremented by two instead of one, and the next instruction in the program sequence is skipped. If the count in the memory location advances to some value other than zero, the P- and M-registers are incremented by one, and the program proceeds normally to the next instruction in sequence. Incrementing the A- and B-registers with this instruction has no effect on the Extend or Overflow FFs.	4-226	4-41
JMP	Memory Reference	JUMP. Sets the P- and M-registers to the address contained in the instruction word. The next instruction read from memory will be from this memory location.	4-220	4-40
JSB	Memory Reference	Jump to Subroutine. Execution of this instruction, located in memory location "P", causes program control to jump unconditionally to memory location "X" which is specified in the address portion of the JSB instruction. The contents of the P-register ("P") plus one is stored in "X" as the return address for the main program. The next instruction executed will be that contained in location "X + 1". A return to the main program sequence at "P + 1" can be achieved by a jump indirect through location "X".	4-213	4-39
LDA	Memory Reference	Load into A-Register. The A-register is cleared and then loaded with the contents of the address memory location. The contents of the memory location are unaltered.	4-245	4-44
LDB	Memory Reference	Load into B-Register. The B-register is cleared and then loaded with the contents of the address memory location. The contents of the memory location are unaltered.	4-245	4-44
LIA	Input/Output	Load Input into A-Register. The contents of the buffer register on the interface card residing in the addressed I/O channel are loaded into the A-register. Previous contents in the A-register are lost.	4-424	4-74
LIB	Input/Output	Load Input into B-Register. The contents of the buffer register on the interface card residing in the addressed I/O channel are loaded into the B-register. Previous contents in the B-register are lost.	4-424	4-74

Table 4-8. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA-GRAPH	FIGURE
RBL	Register Reference (SRG)	Rotate all B-Register bits Left one place. The bit in position 15 is rotated around to bit position 0.	4-287	4-51
RBR	Register Reference (SRG)	Rotate all B-Register bits Right one place. The bit in position 0 is rotated around to bit position 15.	4-293	4-52
RSS	Register Reference (ASG)	Reverse Skip Sense. When processed along (not combined with any of the ASG skip instructions), this instruction causes an unconditional skip. When combined with one or more other ASG skip instructions (SEZ, SSA, SSB, SLA, SLB, SZA, or SZB), this instruction causes a skip if a non-zero condition is sensed. If the instruction word includes SSA/B and SLA/B, both bits (15 and 0) must be a logical 1 for the skip to occur. In all other cases a skip occurs if any non-zero condition is sensed.	4-384	NA
SEZ	Register Reference (ASG)	Skip if E-Register is Zero. The next instruction is skipped if the Extend FF is clear.	4-354	4-63
SFC	Input/Output	Skip if Flag Clear. The next instruction is skipped if the Flag FF on the interface card residing in the addressed I/O channel is set. Checks the status of the Interrupt System Enable FF if select code 00 (octal) is used in the instruction word.	4-413	4-72
SLA	Register Reference (ASG and SRG)	Skip if Least significant bit of the A-Register is zero. The next instruction is skipped if the FF in bit position 0 is clear (an even number stored in the A-register).	4-366 and 4-269	4-65 and 4-48
SLB	Register Reference (ASG and SRG)	Skip if Least significant bit of the B-Register is zero. The next instruction is skipped if the FF in bit position 0 is clear (an even number stored in the B-register).	4-366 and 4-269	4-65 and 4-48
SOC	Input/Output	Skip if Overflow Register is Clear. The next instruction is skipped if the Overflow FF is clear. The Overflow FF will be set or cleared following execution of this instruction, depending on the status of the H/C bit in the instruction word, whether a skip occurs or not.	4-451	4-79

Table 4-8. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA-GRAPH	FIGURE
SOS	Input/Output	Skip if Overflow Register is Set. The next instruction is skipped if the Overflow FF is set. The Overflow FF will be set or cleared following execution of this instruction, depending on the status of the H/C bit in the instruction word, whether a skip occurs or not.	4-451	4-79
SSA	Register Reference (ASG)	Skip if Sign bit of A-Register is zero. The next instruction is skipped if the FF in bit position 15 (sign bit is clear (positive).	4-360	4-64
SSB	Register Reference (ASG)	Skip if Sign bit of B-Register is zero. The next instruction is skipped if the FF in bit position 15 (sign bit) is clear (positive).	4-360	4-64
STA	Memory Reference	Store A-Register contents. The contents of the A-register are stored in the addressed memory location. The prior contents of the memory location are lost, but the A-register contents are unaltered.	4-251	4-45
STB	Memory Reference	Store B-Register contents. The contents of the B-register are stored in the addressed memory location. The prior contents of the memory location are lost, but the B-register contents are unaltered.	4-251	4-45
STC	Input/Output	Set Control bit on the I/O channel addressed by the select code. Sets the Control FF on the interface card residing in the addressed I/O channel. This enables the external device to perform its input or output function, and its flag to interrupt the program.	4-436	4-76
STF	Input/Output	Set Flat bit on the I/O channel addressed by the select code. Sets the Flag FF on the interface card residing in the addressed I/O channel. This causes an interrupt during the next machine cycle if the interrupt system is enabled, and if the Control FF on the interface card is set. A STF instruction addressed to select code 00 (octal) sets the Interrupt System Enable FF to enable the entire interrupt system.	4-398	4-69
STO	Input/Output	Set Overflow Register. Sets the Overflow FF.	4-441	4-77
SZA	Register Reference (ASG)	Skip if A-Register is Zero. The next instruction is skipped if the contents of the A-register are equal to zero (all 16 bit positions clear).	4-378	4-67
SZB	Register Reference (ASG)	Skip if B-Register is Zero. The next instruction is skipped if the contents of the B-register are equal to zero (all 16 bit positions clear).	4-378	4-67

Table 4-8. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA-GRAPH	FIGURE
XOR	Memory Reference	Exclusive "Or" to A-Register. The contents of the addressed memory location are combined with the contents of the A-register by an exclusive "or" logic operation. The result is stored in the A-register, and the contents of the addressed memory location are unaltered.	4-201	4-37

Table 4-9. Logic Equations

SIGNAL	EQUATION
AAF	= AA FF
AA FF	
J	= P123G*T0*TAN1*TAN2*TAN3*$\overline{TB14}$*$\overline{TB13}$*$\overline{TB12}$
K	= T7
CLOCK	= TS
ADD	= EIR*IR14*$\overline{IR13}$*$\overline{IR12}$
ADF	= ADD*PH3*T3T4
	= ASG*T4T5
	= ISZ*PH3*T3T4
	= JSB*PH3*T1T2
	= P123*T6T7
	= PH4*T3T4
ANF	= EIR*PH3*T3T4*$\overline{IR14}$*IR13*IR12*$\overline{IR11}$
A REGISTER	
AR0 FF	
J	= TB0
K	= $\overline{TB0}$
CLOCK	= STBA
AR1 FF	
J	= TB1
K	= $\overline{TB1}$
CLOCK	= STBA
AR2 FF	
J	= TB2
K	= $\overline{TB2}$
CLOCK	= STBA
AR3 FF	
J	= TB3
K	= $\overline{TB3}$
CLOCK	= STBA
AR4 FF	
J	= TB4
K	= $\overline{TB4}$
CLOCK	= STBA
AR5 FF	
J	= TB5
K	= $\overline{TB5}$
CLOCK	= STBA
AR6 FF	
J	= TB6
K	= $\overline{TB6}$
CLOCK	= STBA
AR7 FF	
J	= TB7
K	= $\overline{TB7}$
CLOCK	= STBA
AR8 FF	
J	= TB8
K	= $\overline{TB8}$
CLOCK	= STBA
AR9 FF	
J	= TB9
K	= $\overline{TB9}$
CLOCK	= STBA
AR10 FF	
J	= TB10
K	= $\overline{TB10}$
CLOCK	= STBA
AR11 FF	
J	= TB11
K	= $\overline{TB11}$
CLOCK	= STBA
AR12 FF	
J	= TB12
K	= $\overline{TB12}$
CLOCK	= STBA
AR13 FF	
J	= TB13
K	= $\overline{TB13}$
CLOCK	= STBA
AR14 FF	
J	= TB14
K	= $\overline{TB14}$
CLOCK	= STBA
AR15	
J	= TB15
K	= $\overline{TB15}$
CLOCK	= STBA
AS	= EAU OPTION
ASG	= EIR*PH1*$\overline{IR15}$*$\overline{IR14}$*$\overline{IR13}$*$\overline{IR12}$*IR10
BAF	= BA FF
BA FF	
J	= P123G*T0*TAN2*TAN3*$\overline{TB14}$*$\overline{TB13}$*$\overline{TB12}$*$\overline{TB3}$*$\overline{TB2}$*$\overline{TB1}$*TB0
K	= T7
CLOCK	= TS
B REGISTER	
BR0 FF	
J	= TB0
K	= $\overline{TB0}$
CLOCK	= STBB
BR1 FF	
J	= TB1
K	= $\overline{TB1}$
CLOCK	= STBB
BR2 FF	
J	= TB2
K	= $\overline{TB2}$
CLOCK	= STBB
BR3 FF	
J	= TB3
K	= $\overline{TB3}$
CLOCK	= STBB
BR4 FF	
J	= TB4
K	= $\overline{TB4}$
CLOCK	= STBB

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
BR5 FF	
J	= TB5
K	= $\overline{TB5}$
CLOCK	= STBB
BR6 FF	
J	= TB6
K	= $\overline{TB6}$
CLOCK	= STBB
BR7 FF	
J	= TB7
K	= $\overline{TB7}$
CLOCK	= STBB
BR8 FF	
J	= TB8
K	= $\overline{TB8}$
CLOCK	= STBB
BR9 FF	
J	= TB9
K	= $\overline{TB9}$
CLOCK	= STBB
BR10 FF	
J	= TB10
K	= $\overline{TB10}$
CLOCK	= STBB
BR11 FF	
J	= TB11
K	= $\overline{TB11}$
CLOCK	= STBB
BR12 FF	
J	= TB12
K	= $\overline{TB12}$
CLOCK	= STBB
BR13 FF	
J	= TB13
K	= $\overline{TB13}$
CLOCK	= STBB
BR14 FF	
J	= TB14
K	= $\overline{TB14}$

SIGNAL	EQUATION
CLOCK	= STBB
BR15 FF	
J	= TB15
K	= $\overline{TB15}$
CLOCK	= STBB
C0	= C FF*T6T7
C1	= C0*RB0+C0*SB0+RB0*SB0
C2	= C1*RB1+C1*SB1+RB1*SB1
C3	= C2*RB2+C2*SB2+RB2*SB2
C4	= C3*RB3+C3*SB3+RB3*SB3
C5	= C4*RB4+C4*SB4+RB4*SB4
C6	= C5*RB5+C5*SB5+RB5*SB5
C7	= C6*RB6+C6*SB6+RB6*SB6
C8	= C7*RB7+C7*SB7+RB7*SB7
C9	= C8*RB8+C8*SB8+RB8*SB8
C10	= C9*RB9+C9*SB9+RB9*SB9
C11	= C10*RB10+C10*SB10+RB10*SB10
C12	= C11*RB11+C11*SB11+RB11*SB11
C13	= C12*RB12+C12*SB12+RB12*SB12
C14	= C13*RB13+C13*SB13+RB13*SB13
C15	= C14*RB14+C14*SB14+RB14*SB14
C16	= C15*RB15+C15*SB15+RB15*SB15
CF1	
J	= 1
K	= 1
CLOCK	= 100NS
CF2	
J	= 1
K	= 1
CLOCK	= CF1
C FF	
J	= ASG*EFF*T3*TR5*TB0(B)
	= ASG*$\overline{EFF}$*T3*TR5*$\overline{TR0}$
	= ASG*T4*TR4*$\overline{TR0}$*$\overline{RB15}$
	= ASG*T4*TRY*$\overline{TR3}$*TR0(B)
	= ASG*T4*TR4*TR0(B)*RB15

SIGNAL	EQUATION
	= ASG*T4*TR4*TR0(B)*RB0
	= ASG*T4*$\overline{TR4}$*TR3*TR0(B)
	= ASG*T4*TR3*TR0(B)*RB15
	= ASG*T4*TR3*TR0(B)*RB0
	= ASG*T4*TR3*$\overline{TR0}$*$\overline{RB0}$
	= ASG*T5*TR1*($\overline{TAN4}$+$\overline{TAN3}$+$\overline{TAN2}$+$\overline{TAN1}$)
	= ASG*T5*$\overline{TR4}$*$\overline{TR3}$*$\overline{TR1}$*($\overline{TAN4}$*$\overline{TAN3}$*$\overline{TAN2}$*$\overline{TAN1}$)
	= ASG*T5*TR1*$\overline{TR0}$*TAN4*TAN3*TAN2*TAN1
	= CPR*PH3*T4*($\overline{TAN4}$+$\overline{TAN3}$+$\overline{TAN2}$+$\overline{TAN1}$)
	= ISZ*PH3*T4*C16
	= SKF*T4
	= SRG*T4*TR3*$\overline{RB0}$
K	= T0
CLOCK	= TS
CIN	= DMA OPTION
CL1	= CF1*CF2
CL2	= CF1*$\overline{CF2}$
CLC	= IOG*T4*TR11*TR8*TR7*TR6
CLF	= IOG*T4*TR9
CM1	= DMA OPTION
CM2	= DMA OPTION
$\overline{CMF}$	= $\overline{CMFE}$*$\overline{CMFB}$
CMFE	= ASG*TR9
	= PH4*T1T2
	= PH4*T5
$\overline{CMFE}$	= $\overline{ASG}$*$\overline{PH4}$
	= $\overline{ASG}$*$\overline{T1T2}$*$\overline{T5}$
	= $\overline{PH4}$*$\overline{TR9}$
	= $\overline{T1T2}$*$\overline{T5}$*$\overline{TR9}$
CMFB	= EAU OPTION
COUT	= DMA OPTION
CPR	= EIR*IR14*$\overline{IR13}$*IR12
CR1	= DMA OPTION
CR2	= DMA CPTION
CRS	= POPIO+CLC*SCO
CTFF	
SET	= (IT FF*DELAY)*$\overline{IT\ FF}$
CLEAR	= CRS
	= IOG*STC*TS

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
	= IOG*CLC*TS
	= IOG*STF*TS
	= IOG*CLF*TS
	= PH4*T3(B)
	= SYNC2*SYNC1*PH5*T3(B)
DISPLAY MEMORY FF	
SET	= DMSW*$\overline{RF2}$
CLEAR	= $\overline{DMSW}$
DMS	= DISPLAY MEMORY FF
DMSW	= DISPLAY MEMORY SWITCH ON
$\overline{DMSW}$	= DISPLAY MEMORY SWITCH OFF
EFF	= EXTEND FF
E IND	= EXTEND FF
EIR	= $\overline{IIR}$*($\overline{PH3}$+$\overline{DMS}$*$\overline{LDS}$)
ENF	= T2
$\overline{EOF}$	= $\overline{EOFE}$*$\overline{EOFH}$
EOFB	= EAU OPTION
EOFE	= ASG*T3*$\overline{TR9}$
	= CPR*PH3*T3T4
	= $\overline{CPR}$*PH3*T5*IR12
	= JSB*PH3*T3T4
	= P123*T0T1
	= PH3*T3T4*IR14*IR13*$\overline{IR12}$
	= PH3*T3T4*$\overline{IR14}$*IR13*$\overline{IR12}$
	= SEO*T2
	= STR*PH3*T2
EPH	= $\overline{EPI}$*$\overline{PH5}$
ESR	= IEN*$\overline{HLS}$*$\overline{POPIO}$*IC FF
EXTEND FF	
J	= ADD*PH3*T4*C16
	= ASG*T3*TR7
	= ASG*T5*TR2(B)*C16
	= SRG*T3*TR8*TR7*$\overline{TR6}$*RB15(B)
	= SRG*T3*TR8*$\overline{TR7}$*TR6*RB0(B)
	= SRG*T5*TR2*TR1*$\overline{TR0}$*RB15(B)
	= SRG*T5*TR2*$\overline{TR1}$*TR0*RB0(B)
K	= ASG*T3*TR7*$\overline{TR6}$

SIGNAL	EQUATION
	= ASG*T3*$\overline{TR7}$*TR6
	= SRG*T3*TR8*TR7*$\overline{TR6}$*$\overline{RB15}$
	= SRG*T3*TR8*$\overline{TR7}$*TR6*$\overline{RB0}$
	= SRG*T4*TR5
	= SRG*T5*TR2*TR1*$\overline{TR0}$*$\overline{RB15}$
	= SRG*T5*TR2*$\overline{TR1}$*TR0*$\overline{RB0}$
CLOCK	= TS
HIN	= IOG*$\overline{TR8}$*$\overline{TR7}$*$\overline{TR6}$
HLS	= HALT SWITCH OUTPUT
HLS FF	
SET	= HLS
CLEAR	= $\overline{HLS}$
IAK	= $\overline{IC\ FF}$*PH1*T1
IEN(10)	= IEN(6)*PRH(10)
IEN(6)	= IEN FF
IEN FF	
SET	= STF*SC0
CLEAR	= CLF*SC0
IIR	= PH5
ILS	= INSTRUCTION LOOP SWITCH
INT	= ESR*FLG0
	= ESR*FLG1
	= ESR*FLG2
	= ESR*FLG3
IOBI 0	= IOG*IOI*SC*DATA BIT
	= SWR0*ISR
	= IOG(B)*IOI*SCM0*SCL4*CI0 FF
	= DMA OPTION
	= MP OPTION
IOBI 1	= IOG*IOI*SC*DATA BIT
	= SWR1*ISR
	= IOG(B)*IOI*SCM0*SCL4*CI1 FF
	= DMA OPTION
	= MP OPTION
IOBI 2	= IOG*IOI*SC*DATA BIT
	= SWR2*ISR
	= IOG(B)*IOI*SCM0*SCL4*CI2 FF

SIGNAL	EQUATION
	= DMA OPTION
	= MP OPTION
IOBI 3	= IOG*IOI*SC*DATA BIT
	= SWR3*ISR
	= IOG(B)*IOI*SCM0*SCL4*CI3 FF
	= DMA OPTION
	= MP OPTION
IOBI 4	= IOG*IOI*SC*DATA BIT
	= SWR4*ISR
	= IOG(B)*IOI*SCM0*SCL4*CI4 FF
	= DMA OPTION
	= MP OPTION
IOBI 5	= IOG*IOI*SC*DATA BIT
	= SWR5*ISR
	= IOG(B)*IOI*SCM0*SCL4*CI5 FF
	= DMA OPTION
	= MP OPTION
IOBI 6	= IOG*IOI*SC*DATA BIT
	= SWR6*ISR
	= DMA OPTION
	= MP OPTION
IOBI 7	= IOG*IOI*SC*DATA BIT
	= SWR7*ISR
	= DMA OPTION
	= MP OPTION
IOBI 8	= IOG*IOI*SC*DATA BIT
	= SWR8*ISR
	= DMA OPTION
	= MP OPTION
IOBI 9	= IOG*IOI*SC*DATA BIT
	= SWR9*ISR
	= DMA OPTION
	= MP OPTION
IOBI 10	= IOG*IOI*SC*DATA BIT
	= SWR10*ISR
	= DMA OPTION
	= MP OPTION

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
IOBI 11	= IOG*IOI*SC*DATA BIT
	= SWR11*ISR
	= DMA OPTION
	= MP OPTION
IOBI 12	= IOG*IOI*SC*DATA BIT
	= SWR12*ISR
	= DMA OPTION
	= MP OPTION
IOBI 13	= IOG*IOI*SC*DATA BIT
	= SWR13*ISR
	= DMA OPTION
	= MP OPTION
IOBI 14	= IOG*IOI*SC*DATA BIT
	= SWR14*ISR
	= DMA OPTION
	= MP OPTION
IOBI 15	= IOG*IOI*SC*DATA BIT
	= SWR15*ISR
	= DMA OPTION
	= MP OPTION
	= PE OPTION
IOBI 16	= IOG*IOI*SC*DATA BIT
IOBO 0	= IOCO*RB0
	= DMA OPTION
	= MP OPTION
IOBO 1	= IOCO*RB1
	= DMA OPTION
	= MP OPTION
IOBO 2	= IOCO*RB2
	= DMA OPTION
	= MP OPTION
IOBO 3	= IOCO*RB3
	= DMA OPTION
	= MP OPTION
IOBO 4	= IOCO*RB4
	= DMA OPTION
	= MP OPTION
IOBO 5	= IOCO*RB5
	= DMA OPTION
	= MP OPTION
IOBO 6	= IOCO*RB6
	= DMA OPTION
	= MP OPTION
IOBO 7	= IOCO*RB7
	= DMA OPTION
	= MP OPTION
IOBO 8	= IOCO*RB8
	= DMA OPTION
	= MP OPTION
IOBO 9	= IOCO*RB9
	= DMA OPTION
	= MP OPTION
IOBO 10	= IOCO*RB10
	= DMA OPTION
	= MP OPTION
IOBO 11	= IOCO*RB11
	= DMA OPTION
	= MP OPTION
IOBO 12	= IOCO*RB12
	= DMA OPTION
	= MP OPTION
IOBO 13	= IOCO*RB13
	= DMA OPTION
	= MP OPTION
IOBO 14	= IOCO*RB14
	= DMA OPTION
	= MP OPTION
IOBO 15	= IOCO*RB15
	= DMA OPTION
IOCC	= IOG*T4T5*TR8*TR7*$\overline{TR6}$
IODO	= DMA OPTION
IOF	= EIR*PH3*T3T4*$\overline{IR14}$*$\overline{IR13}$* IR12*$\overline{IR11}$
	= IOG*T4T5
IOG	= EIR*PH1*IR15*$\overline{IR14}$*$\overline{IR13}$* $\overline{IR12}$
IOGE	= IOG*$\overline{MPC}$
IOGE(B)	= IOGE*DELAY
IOI	= IOG*T4T5*TR8*$\overline{TR7}$
	= SEO*T2
	= DMA OPTION
IOO	= IOG*T3T4*TR8*TR7*$\overline{TR6}$
	= SRG*T3*TR8*TR7*$\overline{TR6}$
	= DMA OPTION
IOS	= IOGE(B)*SCM0*SCL1
IR10 FF	
J	= TR10
CLOCK	= PH1*T2*TS
DIRECT CLR	= PH1*T1
IR11 FF	
J	= TR11
CLOCK	= PH1*T2*TS
DIRECT CLR	= PH1*T1
IR12 FF	
J	= TR12
CLOCK	= PH1*T2*TS
DIRECT CLR	= PH1*T1
IR13 FF	
J	= TR13
CLOCK	= PH1*T2*TS
DIRECT CLR	= PH1*T1
IR14 FF	
J	= TR14
CLOCK	= PH1*T2*TS
DIRECT CLR	= PH1*T1
IR15 FF	
J	= TR15
CLOCK	= PH1*T2*TS
DIRECT CLR	= PH1*T1
IRQ(1-17)	= I/O
ISG	= EAU OPTION
ISR	= IOG*IOS*TR8*$\overline{TR7}$
	= SEO
ISZ	= EIR*$\overline{IR14}$*IR13*IR12*IR11
IT FF	
SET	= STM

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
CLEAR	= TO*TS
JMP	= EIR*$\overline{IR14}$*IR13*$\overline{IR12}$*IR11
JSB	= EIR*$\overline{IR14}$*$\overline{IR13}$*IR11*IR11
LADS	= LOAC ADDRESS FF
LADSW	= LOAD ADDRESS SWITCH ON
$\overline{LADSW}$	= LOAD ADDRESS SWITCH OFF
LAS	= LOAD A FF
LASW	= LOAD A SWITCH ON
$\overline{LASW}$	= LOAD A SWITCH OFF
LBS	= LOAD B FF
LBSW	= LOAD B SWITCH ON
$\overline{LBSW}$	= LOAD B SWITCH OFF
LMS	= LOAD MEMORY FF
LMSW	= LOAD MEMORY SWITCH ON
$\overline{LMSW}$	= LOAD MEMORY SWITCH OFF
LOAD A FF	
SET	= LASW*$\overline{RF2}$
CLEAR	= $\overline{LASW}$
LOAD B FF	
SET	= LBSW*$\overline{RF2}$
CLEAR	= $\overline{LBSW}$
LOAD ADDRESS FF	
SET	= LADS*$\overline{RF2}$
CLEAR	= $\overline{LADS}$
LOAD MEMORY FF	
SET	= LMSW*$\overline{RF2}$
CLEAR	= $\overline{LMSW}$
LPS	= LOADER PROTECT SWITCH
M0	= MR0*$\overline{PH5}$+DM0*PH5
M1	= MR1*$\overline{PH5}$+DM1*PH5
M2	= MR2*$\overline{PH5}$+DM2*PH5
M3	= MR3*$\overline{PH5}$+DM3*PH5
M4	= MR4*$\overline{PH5}$+DM4*PH5
M5	= MR5*$\overline{PH5}$+DM5*PH5
M6	= MR6*$\overline{PH5}$+DM6*PH5
M7	= MR7*$\overline{PH5}$+DM7*PH5
M8	= MR8*$\overline{PH5}$+DM8*PH5
M9	= MR9*$\overline{PH5}$+DM9*PH5
M10	= MR10*$\overline{PH5}$+DM10*PH5

SIGNAL	EQUATION
M11	= MR11*$\overline{PH5}$+DM11*PH5
M12	= MR12*$\overline{PH5}$+DM12*PH5
M13	= MR13*$\overline{PH5}$+DM13*PH5
M14	= MR14*$\overline{PH5}$+DM14*PH5
MAC	= EIR*PH1*IR15*$\overline{IR14}$*$\overline{IR13}$* $\overline{IR12}$*$\overline{IR10}$
MD2	= EAU CPTION
MIT	= MTE*ISZ*PH3*$\overline{T0T1}$*$\overline{T1T2}$* $\overline{T3T4}$*$\overline{T5T6}$*$\overline{T6T7}$*$\overline{T7T0}$
	= MTE*ISZ*PH3*$\overline{T4T5}$*T5T6
	= MTE*ISZ*PH3*CF2 FF*T5T6
	= MTE*$\overline{ISZ}$*$\overline{PH3}$*$\overline{CF2\ FF}$*T3T4
MMD13	= M13
MMD14	= MEMORY OPTION
MMD	= MEMORY OPTION
MNS	= MEMORY NCRMAL SWITCH
MP1	= EAU CPTION
MP2	= EAU CPTION
MP3	= EAU CPTION
MP4	= EAU OPTION
MP5	= EAU CPTION
MPC	= PARITY ERROR OPTION
MPT0	= +4.5V
MPT1	= MPT0
MPT2	= MPT1
MPT3	= MPT2
MPT4	= MPT3
MPT	= LPS*M12*M11*M10*M9*M8* M7*M6*MPT1*MPT2*MMD14* MMD13
	= LPS*M12*M11*M10*M9*M8* M7*M6*MPT2*$\overline{MPT3}$*$\overline{MMD14}$* MMD13
	= LPS*M12*M11*M10*M9*M8* M7*M6*MPT3*$\overline{MPT4}$*MMD14* $\overline{MMD13}$
	= LPS*M12*M11*M10*M9*M8* M7*M6*MPT4*MMD14*MMD13* TTK
MR0	= MR0 FF
$\overline{MR0}$	= $\overline{MR0\ FF}$
MR1	= MR1 FF
$\overline{MR1}$	= $\overline{MR1\ FF}$
MR2	= MR2 FF
$\overline{MR2}$	= $\overline{MR2\ FF}$

SIGNAL	EQUATION
MR3	= MR3 FF
$\overline{MR3}$	= $\overline{MR3\ FF}$
MR4	= MR4 FF
$\overline{MR4}$	= $\overline{MR4\ FF}$
MR5	= MR5 FF
$\overline{MR5}$	= $\overline{MR5\ FF}$
MR6	= MR6 FF
$\overline{MR6}$	= $\overline{MR6\ FF}$
MR7	= MR7 FF
$\overline{MR7}$	= $\overline{MR7\ FF}$
MR8	= MR8 FF
$\overline{MR8}$	= $\overline{MR8\ FF}$
MR9	= MR9 FF
$\overline{MR9}$	= $\overline{MR9\ FF}$
MR10	= MR10 FF
$\overline{MR10}$	= $\overline{MR10\ FF}$
MR11	= MR11 FF
$\overline{MR11}$	= $\overline{MR11\ FF}$
MR12	= MR12 FF
$\overline{MR12}$	= $\overline{MR12\ FF}$
MR13	= MR13 FF
$\overline{MR13}$	= $\overline{MR13\ FF}$
MR14	= MR14 FF
MR15	= MR15 FF
M REGISTER	
MR0 FF	
J	= TB0
K	= $\overline{TB0}$
CLOCK	= STM0-5
MR1 FF	
J	= TB1
K	= $\overline{TB1}$
CLOCK	= STM0-5
MR2 FF	
J	= TB2
K	= $\overline{TB2}$
CLOCK	= STM0-5
MR3 FF	
J	= TB3
K	= $\overline{TB3}$
CLOCK	= STM0-5

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
MR4 FF	
J	= TB4
K	= $\overline{TB4}$
CLOCK	= STM0-5
MR5 FF	
J	= TB5
K	= $\overline{TB5}$
CLOCK	= STM0-5
MR6 FF	
J	= TB6
K	= $\overline{TB6}$
CLOCK	= STM6-9
MR7 FF	
J	= TB7
K	= $\overline{TB7}$
CLOCK	= STM6-9
MR8 FF	
J	= TB8
K	= $\overline{TB8}$
CLOCK	= STM6-9
MR9 FF	
J	= TB9
K	= $\overline{TB9}$
CLOCK	= STM6-9
MR10 FF	
J	= TB10
K	= $\overline{TB10}$
CLOCK	= STM10-11
DIRECT CLR	= RSM10-15
MR11 FF	
J	= TB11
K	= $\overline{TB11}$
CLOCK	= STM10-11
DIRECT CLR	= RSM10-15
MR12 FF	
J	= TB12
K	= $\overline{TB12}$
CLOCK	= STM12-15
DIRECT CLR	= RSM10-15

SIGNAL	EQUATION
MR13 FF	
J	= TB13
K	= $\overline{TB13}$
CLOCK	= STM12-15
DIRECT CLR	= RSM10-15
MR14 FF	
J	= TB14
K	= $\overline{TB14}$
CLOCK	= STM12-15
DIRECT CLR	= RSM10-15
MR15 FF	
J	= TB15
K	= $\overline{TB15}$
CLOCK	= STM12-15
DIRECT CLR	= RSM10-15
MRT	= MTE*TO*DELAY
	= MTE*TOT1*$\overline{\text{CF2 FF}}$
	= MTE*T1T2*CF2 FF
MST	= (W1 AT A) MTE*$\overline{LMS}$*$\overline{ISG}$*$\overline{JSB}$ *$\overline{STR}$*$\overline{AAF}$*$\overline{BAF}$*T2*T1T2*CF2
	= (W1 AT A) MTE*$\overline{LMS}$*$\overline{ISG}$*$\overline{AAF}$ $\overline{BAF}$*$\overline{PH3}$·T2·T1T2·CF2
	= (W1 AT B) MTE*$\overline{LMS}$*$\overline{ISG}$*$\overline{JSB}$ *$\overline{STR}$*$\overline{AAF}$*$\overline{BAF}$*T2*CF1
	= (W1 AT B) MTE*$\overline{LMS}$*$\overline{ISG}$*$\overline{AAF}$ *$\overline{BAF}$*$\overline{PH3}$*T2*$\overline{CF1}$
MTE	= MNS*$\overline{MPT}$*P123B
	= MNS*$\overline{LPS}$*P123B
MWL	= MTE*ISZ*PH3
	= MTE*PH3*STR
	= MTE*PH3*JSB
	= MTE*AAF
	= MTE*BAF
	= MTE*ISG
	= MTE*LMS
MWT	= MTE*ISZ*PH3*$\overline{T7T0}$*$\overline{T6T7}$* $\overline{T5T6}$*$\overline{T3T4}$*$\overline{T1T2}$*$\overline{T0T1}$
	= MTE*ISZ*PH3*T5T6*$\overline{T4T5}$
	= MTE*$\overline{ISZ}$*T4T5
	= MTE*$\overline{PH3}$*T4T5
OHC1	= DMA OPTION
CHC2	= DMA OPTION
OLC1	= DMA OPTION
OLC2	= DMA OPTION

SIGNAL	EQUATION
OPO	= EIR*PH1*$\overline{IR14}$*$\overline{IR13}$*$\overline{IR12}$
OUT	= DMA OPTION
OVD	= EAU OPTION
OVERFLOW FF	
J	= ADD*PH3*T4*TB15*RB15* SB15
	= ADD*PH3*T4*$\overline{TB15}$*RB15* SB15
	= ASG*T5*TR2(B)*TB15*RB15* SB15
	= ASG*T5*TR2(B)*$\overline{TB15}$*RB15* SB15
	= IOS*STF
K	= IOS*CLF
CLOCK	= TS
OVF IND	= OVERFLOW FF
OVR	= EAU OPTION
PARITY HALT	= PEI
P123	= PH1+PH2+PH3+PH5
P123(B)	= P123
P123G	= P123*$\overline{PH5}$
PEH	= PARITY OPTION
PEI	= PARITY OPTION
PH1 FF	
J	= JMP*PH2*$\overline{\text{SET PH4}}$*$\overline{TR15}$
	= LPMS
	= PH3*$\overline{\text{SET PH4}}$
	= PH4
	= PRS FF
K	= SET PH2
	= SET PH3
	= SET PH4
CLOCK	= LNS*T7*TS
PH2 FF	
J	= PH1*TR15
	= $\overline{OPO}$*PH1*$\overline{\text{SET PH4}}$*TR15
K	= SET PH1
	= SET PH3
	= SET PH4
CLOCK	= LNS*T7*TS
PH3 FF	
J	= $\overline{JMP}$*$\overline{OPO}$*PH1*$\overline{\text{SET PH4}}$*$\overline{TR15}$

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
	= $\overline{JMP}$*PH2*$\overline{SET\ PH4}$*$\overline{TR15}$
	= DMS*STEP1*$\overline{STEP2}$
	= LMS*STEP1*$\overline{STEP2}$
K	= SET PH1
	= SET PH4
CLOCK	= LNS*T7*TS
PH4 FF	
J	= $\overline{JMP}$*$\overline{JSB}$*INT*RF1
	= INT*RF1*$\overline{IR15}$
K	= SET PH1
CLOCK	= LNS*T7*TS
PH1	= EPH*RF2*PH1 FF
PH2	= EPH*RF2*PH2 FF
PH3	= EPH*RF2*PH3 FF
PH4	= EPH*RF2*PH4 FF
PH5	= DMA OPTION
PIND	= +12V
PNS	= PHASE NORMAL SWITCH
POFP	= ENF.POWER FAIL FLAG BUFFER FF
PON	= +4.5V
POPIO	= POFP*T5
POPIO(B)	= POPIO
P REGISTER	
PR0 FF	
J	= TB0
K	= $\overline{TB0}$
CLOCK	= STP0-9
PR1 FF	
J	= TB1
K	= $\overline{TB1}$
CLOCK	= STP0-9
PR2 FF	
J	= TB2
K	= $\overline{TB2}$
CLOCK	= STP0-9
PR3 FF	
J	= TB3
K	= $\overline{TB3}$
CLOCK	= STP0-9
PR4 FF	
J	= TB4
K	= $\overline{TB4}$
CLOCK	= STP0-9
PR5 FF	
J	= TB5
K	= $\overline{TB5}$
CLOCK	= STP0-9
PR6 FF	
J	= TB6
K	= $\overline{TB6}$
CLOCK	= STP0-9
PR7 FF	
J	= TB7
K	= $\overline{TB7}$
CLOCK	= STP0-9
PR8 FF	
J	= TB8
K	= $\overline{TB8}$
CLOCK	= STP0-9
PR9 FF	
J	= TB9
K	= $\overline{TB9}$
CLOCK	= STP0-9
PR10 FF	
J	= TB10
K	= $\overline{TB10}$
CLOCK	= STP10-11
PR11 FF	
J	= TB11
K	= $\overline{TB11}$
CLOCK	= STP10-11
PR12 FF	
J	= TB12
K	= $\overline{TB12}$
CLOCK	= STP12-15
PR13 FF	
J	= TB13
K	= $\overline{TB13}$
CLOCK	= STP12-15
PR14 FF	
J	= TB14
K	= $\overline{TB14}$
CLOCK	= STP12-15
PR15 FF	
J	= TB15
K	= $\overline{TB15}$
CLOCK	= STP12-15
PRESET LAMP	= POWER FAIL FLAG FF
PRH	= DMA OPTION
PRH5/4	= POWER FAIL FLAG FF
PRH SIGNALS	= I/O OPTIONS
PRS	= PRSW*$\overline{RF2}$
PRSW	= PRESET SWITCH ON
$\overline{PRSW}$	= PRESET SWITCH OFF
PSO	=(+4.5V)*(+18V)*(-12V)*(-5V)*(+12V)
RARB	= AAF*$\overline{JSB}$*P123*T1
	= AAF*$\overline{PH3}$*P123*T1
	= ADD*PH3*T3T4
	= ASG*T3*$\overline{TR8}$
	= ASG*T4T5
	= CPR*PH3*T3T4
	= EIR*PH3*T3T4*$\overline{IR14}$*$\overline{IR11}$
	= IOG*T3*$\overline{TR6}$
	= IOG*T4T5*$\overline{TR6}$
	= SRG*T3
	= SRG*T4T5
	= STR*PH3*T2
RB0	= ISZ*PH3*T3T4
	= RARB*AR0 FF
	= RBRB*BR0 FF
	= RPRB*PR0 FF
RB1	= RARB*AR1 FF
	= RBRB*BR1 FF
	= RPRB*PR1 FF
RB2	= RARB*AR2 FF
	= RBRB*BR2 FF
	= RPRB*PR2 FF

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
RB3	= RARB*AR3 FF
	= RBRB*BR3 FF
	= RPRB*PR3 FF
RB4	= RARB*AR4 FF
	= RBRB*BR4 FF
	= RPRB*PR4 FF
RB5	= RARB*AR5 FF
	= RBRB*BR5 FF
	= RPRB*PR5 FF
RB6	= RARB*AR6 FF
	= RBRB*BR6 FF
	= RPRB*PR6 FF
RB7	= RARB*AR7 FF
	= RBRB*BR7 FF
	= RPRB*PR7 FF
RB8	= RARB*AR8 FF
	= RBRB*BR8 FF
	= RPRB*PR8 FF
RB9	= RARB*AR9 FF
	= RBRB*BR9 FF
	= RPRB*PR9 FF
RB10	= RARB*AR10 FF
	= RBRB*BR10 FF
	= RPRB*PR10 FF
RB11	= RARB*AR11 FF
	= RBRB*BR11 FF
	= RPRB*PR11 FF
RB12	= RARB*AR12 FF
	= RBRB*BR12 FF
	= RPRB*PR12 FF
RB13	= RARB*AR13 FF
	= RBRB*BR13 FF
	= RPRB*PR13 FF
RB14	= RARB*AR14 FF
	= RBRB*BR14 FF
	= RPRB*PR14 FF
RB15	= RARB*AR15 FF

SIGNAL	EQUATION
	= RBRB*BR15 FF
	= RPRB*PR15 FF
RBRB	= ADD*PH3*T3T4
	= ASG*T3*$\overline{\text{TR8}}$
	= ASG*T4T5
	= BAF*$\overline{\text{JSB}}$*P123*T1
	= BAF*$\overline{\text{PH3}}$*P123*T1
	= CPR*PH3*T3T4
	= EIR*PH3*T3T4*$\overline{\text{IR14}}$*$\overline{\text{IR11}}$
	= IOG*T3*$\overline{\text{TR6}}$
	= IOG*T4T5*$\overline{\text{TR6}}$
	= SRG*T3
	= SRG*T4T5
	= STR*PH3*T2
RF1	= RF1 FF
RF2	= RF2 FF
RL4	= SRG*T3*TR8*TR7*TR6
	= SRG*T5*TR2*TR1*TR0(B)
RLL	= SRG*T3*$\overline{\text{TR8}}$*TR7*TR6
	= SRG*T5*$\overline{\text{TR2}}$*TR1*TR0(B)
RMSB	= JSB*PH3*T3T4
	= P123*T0
RNS	= RUN SWITCH
RO	= EAU OPTION
RCT5	= EAU OPTION
RPB	= P123(B)*T0
RPE	= POFP
RPRB	= JSB*PH3*T1T2
	= OPO*T6T7
	= PH3*T6T7
	= PH4*T1T2
	= PH4*T3T4
	= PH4*T5
RF1 FF	
J	= RNS*STEP1 FF*$\overline{\text{STEP2 FF}}$
K	= HIN+RNS+POFP+LPMS
CLOCK	= T5
DIRECT CLR	= HLS FF

SIGNAL	EQUATION
RF2 FF	
J	= STEP1 FF*$\overline{\text{STEP2 FF}}$
K	= $\overline{\text{RF1 FF}}$
CLOCK	= T7S
DIRECT CLR	= LPMS+POFP
RNS	= RNS FF
RNS FF	
SET	= RNSW
CLEAR	= $\overline{\text{RNSW}}$
RNSW	= RUN SWITCH ON
$\overline{\text{RNSW}}$	= RUN SWITCH OFF+POFP
RRS	= SRG*T3*$\overline{\text{TR8}}$*TR7*TR6
	= SRG*T5*$\overline{\text{TR2}}$*TR1*TR0
RSDS	= EAU OPTION
RSM6-9	= PH4*T7
RSM10-15	= $\overline{\text{OPO}}$*PH1*TS*$\overline{\text{IR10}}$
RSET	= EAU OPTION
RST	= P123*T0*TS
RT	= EAU OPTION
RTSB	= $\overline{\text{CPR}}$*PH3*T5*IR12
	= EIR*$\overline{\text{JSB}}$*PH3*T3T4
	= $\overline{\text{OPO}}$*PH1*T6T7
	= PH2*T6T7
RUN	= RF2
SB0	= ASG*T4T5*$\overline{\text{T6T7}}$*TR2
	= ASG*$\overline{\text{ILS}}$*T4T5*TR2
	= JSB*PH3*T1T2*$\overline{\text{T6T7}}$
	= JSB*$\overline{\text{ILS}}$*PH3*T1T2
	= PH4*T3T4*$\overline{\text{T6T7}}$
	= PH4*$\overline{\text{ILS}}$*T3T4
	= IOI*IOBI 0
	= RMSB*MR0
	= RTSB*TR0
SB1	= IOI*IOBI 1
	= RMSB*MR1
	= RTSB*TR1
SB2	= IOI*IOBI 2
	= RMSB*MR2

$$
\begin{aligned}
STBA \quad &= SWST * TS \\
&= EIR * PH3 * T4 * TS * IR14 * \overline{IR12} * \overline{IR11} \\
&= EIR * PH3 * T4 * TS * \overline{IR14} * \overline{IR11} \\
&= \overline{CPR} * AAF * PH3 * T5 * TS * IR12 \\
&= ASG * T3 * TS * \overline{IR11} \\
&= ASG * T5 * TS * TR2 \\
&= SRG * T3 * TS * TR9 * \overline{IR11} \\
&= SRG * T5 * TS * TR4 * \overline{IR11} \\
&= IOG * TS * TR8 * \overline{TR7} * \overline{IR11}
\end{aligned}
$$

$$
\begin{aligned}
STBB \quad &= SWSB * TS \\
&= EIR * PH3 * T4 * TS * IR14 * \overline{IR12} * IR11 \\
&= \overline{CPR} * BAF * PH3 * T5 * TS * IR12 \\
&= ASG * T3 * TS * IR11 \\
&= ASG * T5 * TS * IR11 \\
&= SRG * T3 * TS * TR9 * IR11 \\
&= SRG * T5 * TS * TR4 * IR11 \\
&= IOG * TS * TR8 * \overline{TR7} * IR11
\end{aligned}
$$

$$
\begin{aligned}
STBT \quad &= SWST * TS \\
&= AAF * P123 * T1 * TS \\
&= BAF * P123 * T1 * TS \\
&= ISZ * PH3 * T4 * TS \\
&= JSB * PH3 * T2 * TS \\
&= STR * PH3 * T2 * TS
\end{aligned}
$$

STM Ø-5 $= SWSM * TS$

$= EIR * \overline{OPO} * PH1 * T7 * TS$

$= OPO * T7 * TS$

$= PH2 * T7 * TS$

$= PH3 * T7 * TS$

$= PH4 * T7 * TS$

STM 6-9 $= SWSM * TS$

$= EIR * \overline{OPO} * PH1 * T7 * TS$

$= OPO * T7 * TS$

$= PH2 * T7 * TS$

$= PH3 * T7 * TS$

STM 1Ø-15 $= SWSM * TS$

$= OPO * T7 * TS$

$= PH2 * T7 * TS$

$= PH3 * T7 * TS$

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
	= RTSB*TR2
SB3	= IOI*IOBI 3
	= RMSB*MR3
	= RTSB*TR3
SB4	= IOI*IOBI 4
	= RMSB*MR4
	= RTSB*TR4
SB5	= IOI*IOBI 5
	= RMSB*MR5
	= RTSB*TR5
SB6	= IOI*IOBI 6
	= RMSB*MR6
	= RTSB*TR6
SB7	= IOI*IOBI 7
	= RMSB*MR7
	= RTSB*TR7
SB8	= IOI*IOBI 8
	= RMSB*MR8
	= RTSB*TR8
SB9	= IOI*IOBI 9
	= RMSB*MR9
	= RTSB*TR9
SB10	= IOI*IOBI 10
	= RMSB*MR10
	= RTSB*TR10
SB11	= IOI*IOBI 11
	= RMSB*MR11
	= RTSB*TR11
SB12	= IOI*IOBI 12
	= RMSB*MR12
	= RTSB*TR12
SB13	= IOI*IOBI 13
	= RMSB*MR13
	= RTSB*TR13
SB14	= IOI*IOBI 14

SIGNAL	EQUATION
	= RMSB*MR14
	= RTSB*TR14
SB15	= IOI*IOBI 15
	= RMSB*MR15
	= RTSB*TR15
SCL0	+++ +++ +++ +++ = PH5*TR2*TR1*TR0
SCL1	+++ +++ +++ = PH5*TR2*TR1*TR0
SCL2	+++ +++ +++ = PH5*TR2*TR1*TR0
SCL3	+++ +++ = PH5*TR2*TR1*TR0
SCL4	+++ +++ +++ = PH5*TR2*TR1*TR0
SCL5	+++ +++ = PH5*TR2*TR1*TR0
SCL6	+++ +++ = PH5*TR2*TR1*TR0
SCL7	+++ = PH5*TR2*TR1*TR0
SCM0	+++ +++ +++ +++ = PH5*TR5*TR4*TR3
SCM1	+++ +++ +++ = PH5*TR5*TR4*TR3
SCM2	+++ +++ +++ = PH5*TR5*TR4*TR3
SCM3	+++ +++ = PH5*TR5*TR4*TR3
SCM4	+++ +++ +++ = PH5*TR5*TR4*TR3
SCM5	+++ +++ = PH5*TR5*TR4*TR3
SCM6	+++ +++ = PH5*TR5*TR4*TR3
SCM7	+++ = PH5*TR5*TR4*TR3
SCS	= SINGLE CYCLE FF
SCSW	= SINGLE CYCLE SWITCH ON
++++ SCSW	= SINGLE CYCLE SWITCH OFF
SEO	= LAS+LMS+LPMS+SWSB
SFC	+++ +++ = IOG*TR8*TR7*TR6
SFS	+++ = IOG*TR8*TR7*TR6
SINGLE CYCLE FF	
SET	+++ = SCSW*RF2
CLEAR	++++ = SCSW
SIR	= T5
SKF(XX)	= IOG*SFS*(XX)FLAG FF
SKF(XX)	+++++++ = IOG*SFC*(XX)FLAG*FF
SL14	= SL14E+SL14B
SL14B	= EAU OPTION

SIGNAL	EQUATION
SL14E	+++ = SRG*T3*TR6
	+++ = SRG*T5*TR0
SLM	= SLME+SLMB
SLMB	= EAU OPTION
SLME	+++ = SRG*T3*TR6
	+++ = SRG*T5*TR0
SMAR1	= DMA OPTION
SMAR2	= DMA OPTION
SRE	= PARITY ERROR OPTION
SRG	++++ ++++ = EIR*PH1*IR15*IR14* ++++ ++++ ++++ IR13*IR12*IR10
SRM	= SRME+SRMB
SRMB	= EAU OPTION
SRME	+++ = SRG*T3*TR7*TR6
	+++ = SRP*T3*TR8*TR6
	+++ = SRG*T5*TR1*TR0
	+++ = SRG*T5*TR2*TR0
STBA	= SWSA*TS
	= EIR*PH3*T4*TS*IR14* ++++ ++++ IR12*IR11
	++++ ++++ = EIR*PH3*T4*TS*IR14*IR11
	+++ = CPR*AAF*PH3*T5*TS*IR12
	++++ = ASG*T3*TS*IR11
	= ASG*T5*TS*TR2
	++++ = SRG*T3*TS*TR9*IR11
	++++ = SRG*T5*TS*TR4*IR11
	+++ ++++ = IOG*TS*TR8*TR7*IR11
STBB	= SWSB*TS
	= EIR*PH3*T4*TS*IR14* ++++ IR12*IR11
	+++ = CPR*BAF*PH3*T5*TS*IR12
	= ASG*T3*TS*IR11
	= ASG*T5*TS*IR11
	= SRG*T3*TS*TR9*IR11
	= SRG*T5*TS*TR4*IR11
	+++ = IOG*TS*TR8*TR7*IR11
STBT	= SWST*TS
	= AAF*P123*T1*TS
	= BAF*P123*T1*T3
	= ISZ*PH3*T4*TS

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
	= JSB*PH3*T2*TS
	= STR*PH3*T2*TS
STC	= IOG*T4*TR11*TR8*TR7*TR6
STEP1 FF	
DATA	= RNS+SCS+DMS+LMS
CLOCK	= T2
STEP2 FF	
DATA	= STEP1 FF
CLOCK	= T1
STF	= IOG*T3*$\overline{TR8}$*$\overline{TR7}$*TR6
	= SRG*T3*$\overline{TR8}$*$\overline{TR7}$*TR6
STM 0-5	= SWSM*TS
	= EIR*$\overline{OPO}$*PH1*T7*TS
	= OPO*T7*TS
	= PH2*T7*TS
	= PH3*T7*TS
	= PH4*T7*TS
STM 6-9	= SWSM*TS
	= EIR*$\overline{OPO}$*PH1*T7*TS
	= OPO*T7*TS
	= PH2*T7*TS
	= PH3*T7*TS
STM10-15	= SWSM*TS
	= OPO*T7*TS
	= PH2*T7*TS
	= PH3*T7*TS
STP 0-9	= SWSP*TS
	= JMP*PH1*T5*TS*$\overline{IR10}$
	= JMP*PH1*T7*TS*$\overline{TR15}$
	= JMP*PH2*T7*TS*$\overline{TR15}$
	= JSB*PH3*T4*TS
	= OPO*T7*TS
	= PH3*T7*TS
	= PH4*T2*TS
	= PH4*T4T5*TS
STP10-15	= SWSP*TS
	= JMP*PH1*T5*TS*$\overline{IR10}$
	= JMP*PH2*T7*TS*$\overline{TR15}$

SIGNAL	EQUATION
	= JSB*PH3*T4*TS
	= OPO*T7*TS
	= PH3*T7*TS
	= PH4*T2*TS
	= PH4*T4T5*TS
STR	= EIR*IR14*IR13*IR12
SWCR1	= DMA OPTION
SWCR2	= DMA OPTION
SWSA	= LAS*T2
SWSB	= LBS*T2
SWSM	= LPMS*T2
SWSP	= LPMS*T2
SWST	= LMS*T2
T0	= T0T1*T7T0
T1	= T0T1*T1T2
T2	= T1T2*T2T3
T3	= T2T3*T3T4
T3(B)	= T3
T4	= T3T4*T4T5
T5	= T4T5*T5T6
T6	= T5T6*T6T7
T7	= T6T7*T7T0
T7S	= T7*TS
T0T1 FF	
DATA	= T7T0
CLOCK	= CL1
T1T2 FF	
DATA	= T0T1
CLOCK	= CL2
T2T3 FF	
DATA	= T1T2
CLOCK	= CL1
T3T4 FF	
DATA	= T2T3
CLOCK	= CL2

SIGNAL	EQUATION
T4T5 FF	
DATA	= T3T4
CLOCK	= CL1
T5T6 FF	
DATA	= T4T5
CLOCK	= CL2
T6T7 FF	
DATA	= T5T6
CLOCK	= CL1
T7T0 FF	
DATA	= T6T7
CLOCK	= CL2
TAN1	= $\overline{TB3}$*$\overline{TB2}$*$\overline{TB1}$*$\overline{TB0}$
TAN2	= $\overline{TB7}$*$\overline{TB6}$*$\overline{TB5}$*$\overline{TB4}$
TAN3	= $\overline{RB11}$*$\overline{TB10}$*$\overline{TB9}$*$\overline{TB8}$
TAN4	= $\overline{TB15}$*$\overline{TB14}$*$\overline{TB13}$*$\overline{TB12}$
TB0	= ADF*RB0*SB0*C0
	= ADF*RB0*$\overline{SB0}$*$\overline{C0}$
	= ADF*$\overline{RB0}$*SB0*$\overline{C0}$
	= ADF*$\overline{RB0}$*$\overline{SB0}$*C0
	= ANF*RB0*SB0
	= CHF*$\overline{RB0}$
	= EFF*SRG*T3*TR8*TR7*$\overline{TR6}$
	= EFF*SRG*T5*TR2*TR1*$\overline{TR0}$
	= EOF*RB0*$\overline{SB0}$
	= EOF*$\overline{RB0}$*SB0
	= IOF*RB0
	= IOF*SB0
	= RL4*RB12
	= RL4*SB12
	= RLL*RB15
	= RLL*SB15
	= RSM6-9*SRA0
	= SLM*RB15
	= SLM*SB15
	= SRM*RB1
	= SRM*SB1
	= SWSM*TS

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION	SIGNAL	EQUATION	SIGNAL	EQUATION
TB1	= ADF*RB1*SB1*C1 ←←← ←← = ADF*RB1*SB1*C1 ←←← ←←← = ADF*RB1*SB1*C1 ←←← ←← = ADF*RB1*SB1*C1 = ANF*RB1*SB1 ←←← = CMFE*RB1 ←←← = EOF*RB1*SB1 ←←← = EOF*RB1*SB1 = IOF*RB1 = IOF*SB1 = RL4*RB13 = RL4*SB13 = RLL*RB0 = RLL*SB0 = RSM6-9*SRA1 = SLM*RB0 = SLM*SB0 = SRM*RB2 = SRM*SB2				
TB2	= ADF*RB2*SB2*C2 ←←← ←← = ADF*RB2*SB2*C2 ←←← ←←← = ADF*RB2*SB2*C2 ←←← ←← = ADF*RB2*SB2*C2 = ANF*RB2*SB2 ←←← = CMFE*RB2 = EOF*RB2*SB2 ←←← = EOF*RB2*SB2 = IOF*RB2 = IOF*SB2 = RL4*RB14 = RL4*SB14 = RLL*RB1 = RLL*SB1 = RSM6-9*SRA2 = SLM*RB1 = SLM*SB1 = SRM*RB3 = SRM*SB3				
TB3	= ADF*RB3*SB3*C3 ←←← ←← = ADF*RB3*SB3*C3				

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
TB3	= ADF*$\overline{RB3}$*SB3*$\overline{C3}$
TB3	= ANF*RB3*SB3
TB3	= CMFE*$\overline{RB3}$
TB3	= EOF*RB3*$\overline{SB3}$
TB3	= EOF*$\overline{RB3}$*SB3
TB3	= IOF*RB3
TB3	= IOF*SB3
TB3	= RL4*RB15
TB3	= RL4*SB15
TB3	= RLL*RB2
TB3	= RLL*SB2
TB3	= RSM6-9*SRA3
TB3	= SLM*RB2
TB3	= SLM*SB2
TB3	= SRM*RB4
TB3	= SRM*SB4
TB4	= ADF*RB4*SB4*C4
TB4	= ADF*$\overline{RB4}$*SB4*$\overline{C4}$
TB4	= ADF*$\overline{RB4}$*$\overline{SB4}$*C4
TB4	= ADF*RB4*$\overline{SB4}$*$\overline{C4}$
TB4	= ANF*RB4*SB4
TB4	= CMFE*$\overline{RB4}$
TB4	= EOF*RB4*$\overline{SB4}$
TB4	= EOF*$\overline{RB4}$*SB4
TB4	= IOF*RB4
TB4	= IOF*SB4
TB4	= RL4*RB1
TB4	= RL4*SB1
TB4	= RLL*RB3
TB4	= RLL*SB3
TB4	= RSM6-9*SRA4
TB4	= SLM*RB3
TB4	= SLM*SB3
TB4	= SRM*RB5
TB4	= SRM*SB5
TB5	= ADF*RB5*SB5*C5
TB5	= ADF*$\overline{RB5}$*SB5*$\overline{C5}$
TB5	= ADF*$\overline{RB5}$*$\overline{SB5}$*C5
TB5	= ADF*RB5*$\overline{SB5}$*$\overline{C5}$
TB5	= ANF*RB5*SB5
TB5	= CMFE*$\overline{RB5}$
TB5	= EOF*RB5*$\overline{SB5}$
TB5	= EOF*$\overline{RB5}$*SB5
TB5	= IOF*RB5
TB5	= IOF*SB5
TB5	= RL4*RB2
TB5	= RL4*SB2
TB5	= RLL*RB4
TB5	= RLL*SB4
TB5	= RSM6-9*SRA5
TB5	= SLM*RB4
TB5	= SLM*SB4
TB5	= SRM*RB6
TB5	= SRM*SB6
TB6	= ADF*RB6*SB6*C6
TB6	= ADF*$\overline{RB6}$*SB6*$\overline{C6}$
TB6	= ADF*$\overline{RB6}$*$\overline{SB6}$*C6
TB6	= ADF*RB6*$\overline{SB6}$*$\overline{C6}$
TB6	= ANF*RB6*SB6
TB6	= CMFE*$\overline{RB6}$
TB6	= EOF*RB6*$\overline{SB6}$
TB6	= EOF*$\overline{RB6}$*SB6
TB6	= IOF*RB6
TB6	= IOF*SB6
TB6	= RL4*RB3
TB6	= RL4*SB3
TB6	= RLL*RB5
TB6	= RLL*SB5
TB6	= RSM6-9*SRA6
TB6	= SLM*RB5
TB6	= SLM*SB5
TB6	= SRM*RB7
TB6	= SRM*SB7
TB7	= ADF*RB7*SB7*C7
TB7	= ADF*$\overline{RB7}$*SB7*$\overline{C7}$
TB7	= ADF*$\overline{RB7}$*$\overline{SB7}$*C7
TB7	= ADF*RB7*$\overline{SB7}$*$\overline{C7}$
TB7	= ANF*RB7*SB7
TB7	= CMFE*$\overline{RB7}$
TB7	= EOF*RB7*$\overline{SB7}$
TB7	= EOF*$\overline{RB7}$*SB7
TB7	= IOF*RB7
TB7	= IOF*SB7
TB7	= RL4*RB4
TB7	= RL4*SB4
TB7	= RLL*RB6
TB7	= RLL*SB6
TB7	= RSM6-9*SRA7
TB7	= SLM*RB6
TB7	= SLM*SB6
TB7	= SRM*RB8
TB7	= SRM*SB8
TB8	= ADF*RB8*SB8*C8
TB8	= ADF*$\overline{RB8}$*SB8*$\overline{C8}$
TB8	= ADF*$\overline{RB8}$*$\overline{SB8}$*C8
TB8	= ADF*RB8*$\overline{SB8}$*$\overline{C8}$
TB8	= ANF*RB8*SB8
TB8	= CMFE*$\overline{RB8}$
TB8	= EOF*RB8*$\overline{SB8}$
TB8	= EOF*$\overline{RB8}$*SB8
TB8	= IOF*RB8
TB8	= IOF*SB8
TB8	= RL4*RB5
TB8	= RL4*SB5
TB8	= RLL*RB7
TB8	= RLL*SB7
TB8	= RSM6-9*SRA8
TB8	= SLM*RB7
TB8	= SLM*SB7
TB8	= SRM*RB9
TB8	= SRM*SB9
TB9	= ADF*RB9*SB9*C9
TB9	= ADF*$\overline{RB9}$*SB9*$\overline{C9}$
TB9	= ADF*$\overline{RB9}$*$\overline{SB9}$*C9
TB9	= ADF*RB9*$\overline{SB9}$*$\overline{C9}$
TB9	= ANF*RB9*SB9
TB9	= CMFE*$\overline{RB9}$
TB9	= EOF*RB9*$\overline{SB9}$
TB9	= EOF*$\overline{RB9}$*SB9
TB9	= IOF*RB9
TB9	= IOF*SB9
TB9	= RL4*RB5
TB9	= RL4*SB5
TB9	= RLL*RB8
TB9	= RLL*SB8
TB9	= RSM6-9*SRA9
TB9	= SLM*RB8

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
TB9	= SLM*SB8
TB9	= SRM*RB10
TB9	= SRM*SB10
TB10	= ADF*RB10*SB10*C10
TB10	= ADF*$\overline{\text{RB10}}$*SB10*$\overline{\text{C10}}$
TB10	= ADF*$\overline{\text{RB10}}$*$\overline{\text{SB10}}$*C10
TB10	= ADF*RB10*$\overline{\text{SB10}}$*$\overline{\text{C10}}$
TB10	= ANF*RB10*SB10
TB10	= CMFE*$\overline{\text{RB10}}$
TB10	= EOF*RB10*$\overline{\text{SB10}}$
TB10	= EOF*$\overline{\text{RB10}}$*SB10
TB10	= IOF*RB10
TB10	= IOF*SB10
TB10	= PL4*RB6
TB10	= RL4*SB6
TB10	= RLL*RB9
TB10	= RLL*SB9
TB10	= RSM6-9*SRA10
TB10	= SLM*RB9
TB10	= SLM*SB9
TB10	= SRM*RB11
TB10	= SRM*SB11
TB11	= ADF*RB11*SB11*C11
TB11	= ADF*$\overline{\text{RB11}}$*SB11*$\overline{\text{C11}}$
TB11	= ADF*$\overline{\text{RB11}}$*$\overline{\text{SB11}}$*C11
TB11	= ADF*RB11*$\overline{\text{SB11}}$*$\overline{\text{C11}}$
TB11	= ANF*RB11*SB11
TB11	= CMFE*$\overline{\text{RB11}}$
TB11	= EOF*RB11*$\overline{\text{SB11}}$
TB11	= EOF*$\overline{\text{RB11}}$*SB11
TB11	= IOF*RB11
TB11	= IOF*SB11
TB11	= RL4*RB7
TB11	= RL4*SB7
TB11	= RLL*RB10
TB11	= RLL*SB10
TB11	= RSM6-9*SRA11
TB11	= SLM*RB10
TB11	= SLM*SB10
TB11	= SRM*RB12
TB11	= SRM*SB12
TB12	= ADF*RB12*SB12*C12
TB12	= ADF*$\overline{\text{RB12}}$*SB12*$\overline{\text{C12}}$
TB12	= ADF*$\overline{\text{RB12}}$*$\overline{\text{SB12}}$*C12
TB12	= ADF*RB12*$\overline{\text{SB12}}$*$\overline{\text{C12}}$
TB12	= ANF*RB12*SB12
TB12	= CMFE*$\overline{\text{RB12}}$
TB12	= EOF*RB12*$\overline{\text{SB12}}$
TB12	= EOF*RB12*$\overline{\text{SB12}}$
TB12	= IOF*RB12
TB12	= IOF*SB12
TB12	= RL4*RB8
TB12	= RL4*SB8
TB12	= RLL*RB11
TB12	= RLL*SB11
TB12	= RSM6-9*SRA12
TB12	= SLM*RB11
TB12	= SLM*SB11
TB12	= SRM*RB13
TB12	= SRM*SB13
TB13	= ADF*RB13*SB13*C13
TB13	= ADF*$\overline{\text{RB13}}$*SB13*$\overline{\text{C13}}$
TB13	= ADF*$\overline{\text{RB13}}$*$\overline{\text{SB13}}$*C13
TB13	= ADF*RB13*$\overline{\text{SB13}}$*$\overline{\text{C13}}$
TB13	= ANF*RB13*SB13
TB13	= CMFE*$\overline{\text{RB13}}$
TB13	= EOF*RB13*$\overline{\text{SB13}}$
TB13	= EOF*$\overline{\text{RB13}}$*SB13
TB13	= IOF*RB13
TB13	= IOF*SB13
TB13	= RL4*RB9
TB13	= RL4*SB9
TB13	= RLL*RB12
TB13	= RLL*SB12
TB13	= RSM6-9*SRA13
TB13	= SLM*RB12
TB13	= SLM*SB12
TB13	= SRM*RB14
TB13	= SRM*SB14
TB14	= ADF*RB14*SB14*C14
TB14	= ADF*$\overline{\text{RB14}}$*SB14*$\overline{\text{C14}}$
TB14	= ADF*$\overline{\text{RB14}}$*$\overline{\text{SB14}}$*C14
TB14	= ADF*RB14*$\overline{\text{SB14}}$*$\overline{\text{C14}}$
TB14	= ANF*RB14*SB14
TB14	= CMFE*$\overline{\text{RB14}}$
TB14	= EOF*RB14*$\overline{\text{SB14}}$
TB14	= EOF*$\overline{\text{RB14}}$*SB14
TB14	= IOF*RB14
TB14	= IOF*SB14
TB14	= RL4*RB10
TB14	= RL4*SB10
TB14	= RLL*RB13
TB14	= RLL*SB13
TB14	= RSM6-9*SRA14
TB14	= SLM*RB13
TB14	= SLM*SB13
TB14	= SRM*RB15
TB14	= SRM*SB15
TB15	= ADF*RB15*SB15*C15
TB15	= ADF*$\overline{\text{RB15}}$*SB15*$\overline{\text{C15}}$
TB15	= ADF*$\overline{\text{RB15}}$*$\overline{\text{SB15}}$*C15
TB15	= ADF*RB15*$\overline{\text{SB15}}$*$\overline{\text{C15}}$
TB15	= ANF*RB15*SB15
TB15	= CMFE*$\overline{\text{RB15}}$
TB15	= EOF*RB15*$\overline{\text{SB15}}$
TB15	= EOF*$\overline{\text{RB15}}$*SB15
TB15	= IOF*RB15
TB15	= IOF*SB15
TB15	= RL4*RB11
TB15	= RL4*SB11
TB15	= RLL*RB14
TB15	= RLL*SB14
TB15	= RSM6-9*SRA15
TB15	= SLM*RB14
TB15	= SLM*SB14
TB15	= SRG*T3*$\overline{\text{TR8}}$*$\overline{\text{TR7}}$*RB15(B)
TB15	= SRG*T5*$\overline{\text{TR2}}$*$\overline{\text{TR1}}$*RB15(B)
TB15	= SRG*EFF*T3*TR8*$\overline{\text{TR7}}$*TR6
TB15	= SRG*EFF*T5*TR2*$\overline{\text{TR1}}$*TR0
TB15	= SRM*RB0
TB15	= SRM*SB0
TE1	= DMA OPTION
TE2	= DMA OPTION
TEV	= EAU CPTION
TOD	= EAU CPTION

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION
T REGISTER	
TR0 FF	
J	= TB0
K	= $\overline{\text{TB0}}$
CLOCK	= STBT
DIRECT SET	= ST0
DIRECT CLR	= RST
TR1 FF	
J	= TB1
K	= $\overline{\text{TB1}}$
CLOCK	= STBT
DIRECT SET	= ST1
DIRECT CLR	= RST
TR2 FF	
J	= TB2
K	= $\overline{\text{TB2}}$
CLOCK	= STBT
DIRECT SET	= ST2
DIRECT CLR	= RST
TR3 FF	
J	= TB3
K	= $\overline{\text{TB3}}$
CLOCK	= STBT
DIRECT SET	= ST3
DIRECT CLR	= RST
TR4 FF	
J	= TB4
K	= $\overline{\text{TB4}}$
CLOCK	= STBT
DIRECT SET	= ST4
DIRECT CLR	= RST
TR5 FF	
J	= TB5
K	= $\overline{\text{TB5}}$
CLOCK	= STBT
DIRECT SET	= ST5
DIRECT CLR	= RST
TR6 FF	
J	= TB6
K	= $\overline{\text{TB6}}$
CLOCK	= STBT
DIRECT SET	= ST6
DIRECT CLR	= RST
TR7 FF	
J	= TB7
K	= $\overline{\text{TB7}}$
CLOCK	= STBT
DIRECT SET	= ST7
DIRECT CLR	= RST
TR8 FF	
J	= TB8
K	= $\overline{\text{TB8}}$
CLOCK	= STBT
DIRECT SET	= ST8
DIRECT CLR	= RST
TR9 FF	
J	= TB9
K	= $\overline{\text{TB9}}$
CLOCK	= STBT
DIRECT SET	= ST9
DIRECT CLR	= RST
TR10 FF	
J	= TB10
K	= $\overline{\text{TB10}}$
CLOCK	= STBT
DIRECT SET	= ST10
DIRECT CLR	= RST
TR11 FF	
J	= TB11
K	= $\overline{\text{TB11}}$
CLOCK	= STBT
DIRECT SET	= ST11
DIRECT CLR	= RST
TR12 FF	
J	= TB12
K	= $\overline{\text{TB12}}$
CLOCK	= STBT
DIRECT SET	= ST12
DIRECT CLR	= RST
TR13 FF	
J	= TB13
K	= $\overline{\text{TB13}}$
CLOCK	= STBT
DIRECT SET	= ST13
DIRECT CLR	= RST
TR14 FF	
J	= TB14
K	= $\overline{\text{TB14}}$
CLOCK	= STBT
DIRECT SET	= ST14
DIRECT CLR	= RST
TR15 FF	
J	= TB15
K	= $\overline{\text{TB15}}$
CLOCK	= STBT
DIRECT SET	= ST15
DIRECT CLR	= RST
TR0	= TR0 FF
$\overline{\text{TR0}}$	= $\overline{\text{TR0 FF}}$
TR1	= TR1 FF
$\overline{\text{TR1}}$	= $\overline{\text{TR1 FF}}$
TR2	= TR2 FF
$\overline{\text{TR2}}$	= $\overline{\text{TR2 FF}}$
TR3	= TR3 FF
$\overline{\text{TR3}}$	= $\overline{\text{TR3 FF}}$
TR4	= TR4 FF
$\overline{\text{TR4}}$	= $\overline{\text{TR4 FF}}$
TR5	= TR5 FF
$\overline{\text{TR5}}$	= $\overline{\text{TR5 FF}}$
TR6	= TR6 FF
$\overline{\text{TR6}}$	= $\overline{\text{TR6 FF}}$
TR7	= TR7 FF
$\overline{\text{TR7}}$	= $\overline{\text{TR7 FF}}$
TR8	= TR8 FF
$\overline{\text{TR8}}$	= $\overline{\text{TR8 FF}}$
TR9	= TR9 FF
$\overline{\text{TR9}}$	= $\overline{\text{TR9 FF}}$
TR10	= TR10 FF
$\overline{\text{TR10}}$	= $\overline{\text{TR10 FF}}$
TR11	= TR11 FF
$\overline{\text{TR11}}$	= $\overline{\text{TR11 FF}}$

Table 4-9. Logic Equations (Continued)

SIGNAL	EQUATION	SIGNAL	EQUATION	SIGNAL	EQUATION
TR12	= TR12 FF				
$\overline{\text{TR12}}$	= $\overline{\text{TR12 FF}}$				
TR13	= TR13 FF				
$\overline{\text{TR13}}$	= $\overline{\text{TR13 FF}}$				
TR14	= TR14 FF				
$\overline{\text{TR14}}$	= $\overline{\text{TR14 FF}}$				
TR15	= TR15 FF				
$\overline{\text{TR15}}$	= $\overline{\text{TR15 FF}}$				
TR0(B)	= DMA OPTION				
TR1(B)	= DMA OPTION				
TR2(B)	= DMA OPTION				
TR3(B)	= DMA OPTION				
TR4(B)	= DMA OPTION				
TR5(B)	= DMA OPTION				
TR6(B)	= DMA OPTION				
TR7(B)	= DMA OPTION				
TR8(B)	= DMA OPTION				
TR9(B)	= DMA OPTION				
TR10(B)	= DMA OPTION				
TR11(B)	= DMA OPTION				
TR12(B)	= DMA OPTION				
TR13(B)	= DMA OPTION				
TR14(B)	= DMA OPTION				
TR15(B)	= DMA OPTION				
TS	= $\overline{\text{CF1}}$*DELAY				
TSA	= $\overline{\text{CF1}}$*DELAY				
TTK	= MEMORY OPTION				
WCR1	= DMA OPTION				
WCR2	= DMA OPTION				
X0	= MMD14*MMD13*$\overline{\text{M12}}$*$\overline{\text{TTK}}$				
X1	= $\overline{\text{MMD14}}$*$\overline{\text{MMD13}}$*$\overline{\text{M12}}$				
X2	= $\overline{\text{MMD14}}$*$\overline{\text{MMD13}}$*M12				
X3	= $\overline{\text{MMD14}}$*MMD13*M12				
Y0/1	= $\overline{\text{MMD14}}$*$\overline{\text{MMD13}}$+MMD14* MMD13*$\overline{\text{TTK}}$				
Y2/3	= $\overline{\text{MMD14}}$*MMD13				

4-48. CIRCUIT DESCRIPTION AND TEST PROCEDURES.

4-49. Descriptions and test procedures for the circuit functions comprising the control, arithmetic, memory, input/output, and power supply sections of the computer are presented in paragraphs 4-60 through 4-513. The circuit descriptions include information which is helpful during troubleshooting. The test procedures include test data and suggested test methods which can be used to substantiate or disclaim that the circuit under test is the cause of the trouble. In the event that the circuit under test is not the cause of the trouble, references are provided to troubleshooting data for related circuit functions which could cause the trouble symptom. If it is determined that the circuit under test is the cause of the trouble, use of the equations and troubleshooting diagrams in this section, together with the detailed schematic diagrams, parts location diagrams, and interconnection and wiring information in section V will provide the additional data needed to isolate the trouble to a replaceable or repairable assembly or part.

4-50. TROUBLESHOOTING DIAGRAMS.

4-51. The troubleshooting diagrams presented in figures 4-2 through 4-93 of this section consist of timing diagrams, waveforms, and servicing diagrams. The purpose and use of these diagrams is described in the following paragraphs.

4-52. TIMING DIAGRAMS. Timing diagrams are provided to show timing relationships between signals associated with a given circuit function. The timing diagram for the basic timing circuit (figure 4-15) is a typical example. The signals shown in timing diagrams are "idealized" (i.e. not shown as they would actually appear on an oscilloscope). This can be seen by comparing the 10MHz oscillator output and time T0 signal as they are shown in figure 4-15 to the actual oscilloscope waveforms shown in figure 4-16.

4-53. WAVEFORM DIAGRAMS. Waveform diagrams are provided to show computer signals as they actually appear on an oscilloscope. The waveforms in figure 4-16 are a typical example. All waveforms in this manual were observed on an HP 180A Plug-in Oscilloscope Main Frame equipped with an HP 1801A Vertical Amplifier, an HP 1820A Time Base, and HP 10004A Miniature Resistive Divider Probes (10:1). Unless otherwise noted in the waveform diagram or in text, oscilloscope connections and settings are as specified in table 4-10.

4-54. SERVICING DIAGRAMS. The servicing diagrams in this section include schematic diagrams, logic diagrams, and block diagrams that show signal flow and interconnections for a complete circuit function. The purpose of these diagrams is to provide the information needed at circuit level that will enable the user to localize a trouble symptom to a faulty assembly, and in some instances, isolate the trouble directly to the part that failed. Typical servicing diagrams are shown in figures 4-3, 4-36, and 4-81.

Table 4-10. Oscilloscope Settings and Connections

Channel A:	
Input	As specified
Input coupling	DC
Polarity	Positive
Volts/cm	As specified
Channel B:	
Input	As specified
Input coupling	DC
Polarity	Positive
Volts/cm	As specified
Triggering:	
Mode	Internal
Source	Channel B
Slope	Positive
Coupling	DC
Display mode	Chopped
Time/cm	As specified
Magnification	x1
Graticule divisions	Centimeters

4-55. To understand and properly use the servicing block diagrams presented for the instruction processing circuits (figures 4-36 through 4-79), refer to figure 4-36 as a typical example and review the following information:

a. The signal flow and timing shown on each diagram is applicable to the phase during which the instruction is executed. Some instructions are executed during the fetch phase (phase 1), while others are executed during the execute phase (phase 3).

b. The timing and phase signals used in executing the instruction are shown extending from the block representing timing generator card A106. This block is located on the left side of each diagram.

c. The bit pattern for the instruction, as stored in the instruction register (I-register), is indicated in a separate block for instruction decoder card A107. This block is located in the top-left of each diagram.

d. Blocks representing the circuits that decode and process the instruction are grouped at the top-right of each diagram.

e. Blocks representing the circuits that increment the P- and M-registers are grouped at the bottom-right of each diagram.

f. Blocks representing the circuits that perform the memory operation which occurs when the instruction is processed are grouped at the left of each diagram.

g. Blocks, or groups of blocks, representing circuits that perform special operations during the processing of a given instruction are included on each diagram as required.

h. The "and" gate symbol, as used on these diagrams, indicates that the associated signals at the input of the symbol are logically combined in some manner to produce the signal at the output of the symbol, but are not necessarily "anded".

i. The numbers within the blocks and symbols, where the signal flow lines originate or terminate, correspond to the pins on the 86-pin connector of the associated plug-in card assembly.

j. An asterisk within a block or symbol denotes the termination of a signal flowing within the associated plug-in card assembly (i.e. the signal is not routed through the backplane to reach its destination).

k. The mnemonics on the signal flow lines are defined in table 5-7 of section V.

l. Equations for the signals shown are given in table 4-9.

m. In the timing diagram presented in the lower-left corner, the signals shown are "idealized", as explained in paragraph 4-52. A vertical arrow pointing downward denotes a signal that is continuously false during the timing cycle. A vertical arrow pointing upward denotes a signal that is continuously true during the timing cycle. Some signals (i.e., SBO, RBO, etc.) are active at various times during the processing of an instruction. Only the condition needed to execute the instruction are shown in the timing diagram. Data and unused active control signals are not shown.

4-56. INFORMATION IN OTHER SECTIONS.

4-57. Information in other sections of this manual which will be required during troubleshooting includes the circuit descriptions and related diagrams presented in section III, the maintenance instructions, tables, and diagrams presented in section V, and the replaceable parts information presented in section VI. Total familiarity with the content, purpose and use of the information presented in these sections is recommended before attempting to troubleshoot or repair the computer.

4-58. INFORMATION IN OTHER MANUALS.

4-59. Information in other manuals which may be required during troubleshooting includes that presented in Volume One, Specifications and Basic Operation manual (manual part no. 02116-9152), Volume Three, Input/Output System Operation manual (manual part no. 02116-9154), the applicable operating and service manual supplements to Volume Two and Volume Three which document processing options and interface options, installed in the computer and the applicable diagnostic test procedures contained in the Manual of Diagnostics. Familiarity with the content, purpose, and use of the information presented in these manuals is recommended before attempting to troubleshoot or repair the computer.

4-60. CONTROL SECTION AND ARITHMETIC SECTION TROUBLESHOOTING.

4-61. GENERAL.

4-62. Troubleshooting the control and arithmetic sections of the computer consists of performing the basic checkout (paragraph 4-9) and the diagnostic checkout (paragraph 4-17) to test the overall operation of the circuits comprising these sections. Trouble symptoms encountered during the performance of the checkout procedures are used to determine which circuit function is most likely to be causing the trouble indication. References are then provided to applicable circuit level troubleshooting data for the suspected circuit function.

4-63. Troubleshooting data for the control and arithmetic sections consists of descriptions, test procedures, and troubleshooting diagrams for the following circuit functions:

a. Front panel switch and indicator circuits (paragraph 4-65).

b. Timing circuits (paragraph 4-151).

c. Phase logic circuits (paragraph 4-164).

d. A- and B-register addressing circuits (paragraph 4-187).

e. Memory reference instruction processing circuits (paragraph 4-193).

f. Register reference instruction processing circuits (paragraph 4-257).

g. Input/output instruction processing circuits (paragraph 4-390).

4-64. When troubleshooting this section of the computer, refer to sections V and VI of this manual for detailed schematic and logic diagrams, parts location diagrams, interconnection and wiring information, replaceable parts information, and corrective maintenance instructions.

4-65. FRONT PANEL SWITCH AND INDICATOR CIRCUITS.

4-66. Troubleshooting data for the circuits associated with the following switches and indicators are presented in the referenced paragraphs:

a. A- and B-REGISTER indicators (paragraphs 4-86 and 4-92).

b. DISPLAY MEMORY switch (paragraph 4-116).

c. EXECUTE indicator (paragraph 4-176).

d. EXTEND indicator (paragraphs 4-264, 4-339, and 4-372).

e. FETCH indicator (paragraph 4-167).

f. HALT switch and indicator (paragraph 4-76).

g. INDIRECT indicator (paragraph 4-171).

h. INSTRUCTION switch (paragraph 4-146).

i. LOAD A switch (paragraph 4-86).

j. LOAD ADDRESS switch (paragraph 4-98).

k. LOAD B switch (paragraph 4-92).

l. LOAD MEMORY switch (paragraph 4-106).

m. M-REGISTER indicators (paragraphs 4-98, 4-116, and 4-124).

n. MEMORY switch (paragraph 4-136).

o. OVERFLOW indicator (paragraphs 4-441 and 4-446).

p. P-REGISTER indicators (paragraphs 4-98, 4-116, and 4-124).

q. PARITY indicator (paragraph 4-67).

r. PHASE switch (paragraph 4-141).

s. POWER indicator (paragraph 4-68) and switch (paragraph 4-485).

t. PRESET switch and indicator (paragraph 4-81).

u. RUN switch and indicator (paragraph 4-71).

v. SINGLE CYCLE switch (paragraph 4-124).

w. SWITCH REGISTER switches (paragraphs 4-86, 4-92, 4-98, and 4-106).

x. T-REGISTER indicators (paragraphs 4-106 and 4-116).

4-67. Use the operating and service manual for the HP 12591A Parity Error Option (manual part no. 12591-9001) to troubleshoot the circuits associated with the PARITY indicator.

4-68. POWER INDICATOR. The following paragraphs provide a description and test procedure for the circuits associated with POWER indicator DS109 located on control panel assembly A502.

4-69. Description. The circuit for the POWER indicator is shown in figure 4-2. Indicator lamp DS109 is powered by the Power Indicator (PIND) signal at pin 49 of power fail interrupt card A1. Dropping resistor A1R4 is connected between the +12-volt dc supply and one side of the lamp filament. The other side of the lamp filament is connected to ground through terminal G on display board A501.

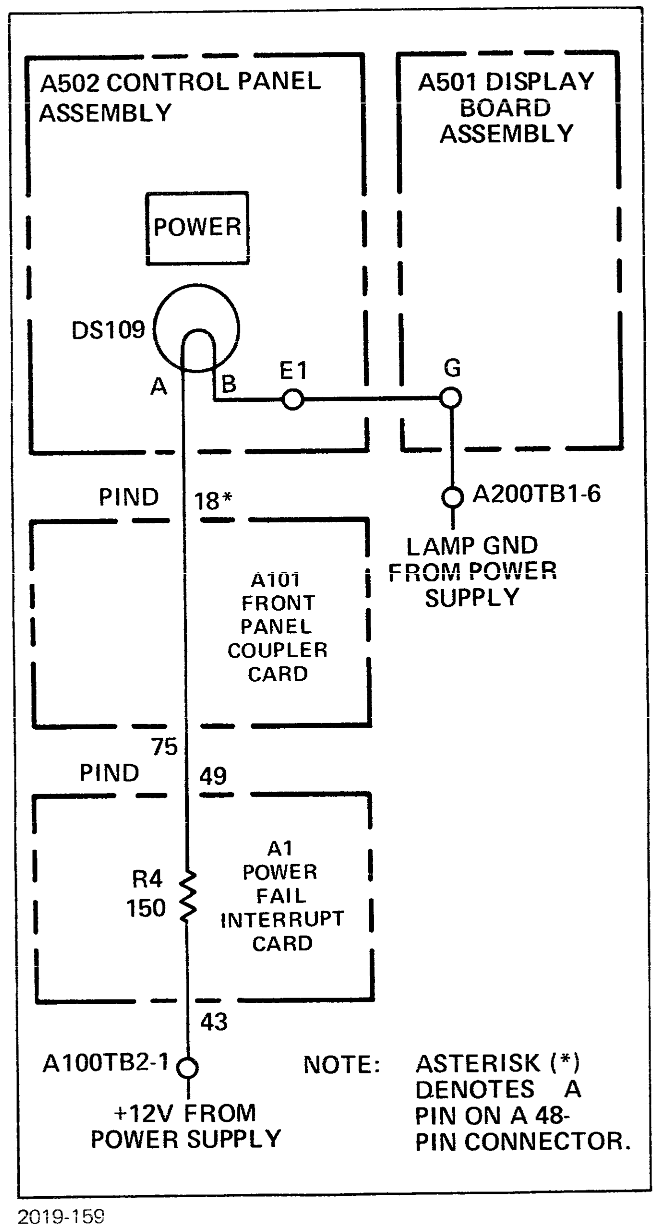


Figure 4-2. POWER Indicator Circuit, Servicing Diagram

4-70. Test Procedure. Using a multi-function meter and the information presented in figure 4-2, proceed as follows:

a. Press the POWER switch to turn on power. Then check the +12-volt dc supply at A100TB2-1. If normal, proceed to step "b". If abnormal, refer to paragraph 4-508 and troubleshoot the power supply.

b. Press and release the POWER switch to turn off power. After checking to ensure that indicator lamp A502DS109 is not defective, make continuity and resistance checks of points between A501-G and A100TB2-1.

4-71. RUN SWITCH AND INDICATOR. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with RUN switch S107 and RUN indicator lamp DS107 which are located on control panel assembly A502.

4-72. Description. The circuits associated with the RUN switch and RUN indicator are shown in figure 4-3. The timing diagram included in this figure shows the sequential events that occur when the RUN switch is pressed and released. In the following description it is assumed that initially all flip-flops shown are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the RUN and HALT switches are in the released position as shown.

4-73. The RUN switch is a momentary-action type switch. When pressed, it places +4.5 volts at input pin 2 of MC65 (RNS FF) causing the output at pin 13 to go false. This false signal is felt at input pin 6. Input pin 7 of MC65 is false due to open contacts 1 and 3 of the pressed RUN switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signal RNS at pin 44 of front panel coupler card A101. As long as the RUN switch is pressed, signal RNS remains true. When the RUN switch is released, +4.5 volts is transferred to input pin 7 of MC65 which causes output pin 9 to go false.

4-74. Signal RNS is transferred through pin 70 of timing generator card A106 to input pin 14 of "and" gate MC86D and input pin 6 of "and" gate MC76B. When signal RNS is true, output pin 13 of MC86D goes true. This true signal is transferred to pin 1 of STEP 1 FF MC94A. At the first time T2, the STEP 1 FF sets and remains set until the first time T2 after the RUN switch is released. The output at pin 13 of the STEP 1 FF is transferred to pin 7 of STEP 2 FF MC94B which sets at the next time T1 and remains set until the first time T1 after the RUN switch is released. The output of the STEP 1 FF is also transferred to input pin 9 of "and" gate MC76C. Input pin 7 of MC76C is held true at this time by "nor" gate MC87A. Thus, output pin 10 of MC76C goes true at time T2 and remains true until the following time T1 when STEP 2 FF sets (1.4 microseconds). This output is transferred through MC76B to input pin 14 of MC84 (RUN FF 1) and to input pin 14 of MC74 (RUN FF 2). At the end of time T5, RUN FF 1 will set. At the end of time T7S, RUN FF 2 will set. These flip-flops will remain set until a PRESET or HALT signal is received at pins 8 or 9 respectively of RUN FF 1 resetting this flip-flop. The outputs of both RUN flip-flops are transferred to the phase logic circuit along with the output of MC76C. The output at pin 13 of RUN FF 2 is also transferred to the base of transistor Q5 turning it on and completing the ground connection for the RUN indicator. The false output at pin 10 of RUN FF 2 is transferred to the base of transistor Q4 turning it off and turning off the HALT indicator. At time T1 after the STEP 1 FF has been set, the STEP 2 FF is set. Its output is transferred to input pin 2 of MC87A causing output pin 13 of MC87A to go false. This causes output pin 10 of MC76C to go false and remove the input from RUN FF 1 (through MC76B) and from RUN FF 2 and the phase logic circuits.

4-75. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-3, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +7-volt dc supply at pin A of RUN indicator A502DS107. If normal, proceed to step "c". If abnormal, check the connection between A502DS107-A and A501-(+).

c. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S107. If normal, proceed to step "d". If abnormal, check the connection between A502S107-1,2 and A101-39,40.

d. At the computer front panel, press and release the POWER switch to turn off power. After checking to ensure that indicator lamp A502DS107 is not defective, proceed to step "e".

e. Using the extender card (part no. 02115-6047) and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

f. At the computer front panel, press and release the POWER switch to turn on power.

g. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-70.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

h. At the computer front panel, press and hold the RUN switch and check the oscilloscope display for a +4.5-volt level. Then release the RUN switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A101MC65, A101MC83, and the RUN switch A502S107 as the most probable cause of trouble.

i. Place the channel A oscilloscope probe on A106MC87-13.

j. At the computer front panel, press and hold the RUN switch and check the oscilloscope display for a +4.5-volt level. Then release the RUN switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, check MC86D, STEP 1 FF MC94A, and STEP 2 FF MC94B as the most probable cause of trouble.

k. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10.1 probe).

(5) Channel A input: A206MC76-10.

(6) Channel B input: A106TP1 (time T0).

l. At the computer front panel, repeatedly press and release the RUN switch. After one machine cycle (1.6 μs) a pulse 1.4 μs in duration should be observed. If the oscilloscope display is normal, proceed to step "m". If the oscilloscope display is abnormal, check A106MC76C as the most probable cause of trouble.

m. Place the channel A oscilloscope probe on A106MC76-13. At the computer front panel, repeatedly press and release the RUN switch and check the oscilloscope display for a 1.4 μs pulse occuring every 1.6 μs. If the oscilloscope display is normal, proceed to step "n". If the oscilloscope display is abnormal, check A106MC76B as the most probable cause of trouble.

n. Place the channel A oscilloscope probe on A106MC84-13 (RUN FF 1). At the computer front panel, press and release the RUN switch and check the oscilloscope display for a +4.5-volt level. Then press and release the HALT switch and check the oscilloscope for a 0-volt level. If the oscilloscope display is normal, proceed to step "o". If the oscilloscope display is abnormal, check pin 1 of MC84 for a 45 ηs to 55 ηs pulse occuring every 1.6 μs and pin 8 of MC84 for a 0-volt level. With the oscilloscope probe on pin 9 of MC84 press and release the HALT switch and check the oscilloscope display for a voltage level change from 0-volts to +4.5-volts back to 0-volts. If the indication at pin 1 is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits. If the indication at pin 8 is abnormal, refer to paragraph 4-81 and troubleshoot the circuits associated with the PRESET switch. If the indication at pin 9 is abnormal, refer to paragraph 4-76 and troubleshoot the circuits associated with the HALT switch.

o. Place the channel A oscilloscope probe on A106MC74-13 (RUN FF 2). At the computer front panel, press and release the RUN switch and check the oscilloscope display for a +4.5-volt level. Then press and release the HALT switch and check the oscilloscope for a 0-volt level. If the oscilloscope display is normal, proceed to step "p". If the oscilloscope display is abnormal, check pin 1 of MC74 for a 45 ηs to 55 ηs pulse occuring every 1.6 μs, and check pin 8 of MC74 for a +4.5-volt level. If the indication at pin 1 is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits. If the indication at pin 8 is abnormal, check diode CR1 for an open condition.

p. Place the channel A oscilloscope probe on pin 7 of the 48-pin connector of A106 and check the oscilloscope display for a +7-volt level. At the computer front panel, press and release the RUN switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check transistor Q5 for an open or shorted condition.

q. At the computer front panel, press and release the POWER switch to turn off power.

r. Using a multi-function meter, check the line between pin 7 of cable 106 and RUN indicator A502DS107-B for continuity.

s. If all indications of the above test procedure are normal, the RUN switch and indicator circuits are operating normally. If one or more indications of the above test procedure are abnormal, refer to the related test procedures, diagrams, and schematics and troubleshoot the related circuits.

4-76. HALT SWITCH AND INDICATOR. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with HALT switch S106 and HALT indicator lamp DS106 located on control panel assembly A502.

4-77. Description. The circuits associated with the HALT switch and HALT indicator are shown in figure 4-3. The timing diagram included in this figure shows the sequential events that occur when the HALT switch is pressed and released. In the following description it is assumed that initially RUN FF 1 and RUN FF 2 flip-flops are in the set condition, the RUN indicator is on, the HALT indicator is off, and the contacts of the RUN and HALT switches are in the released position as shown.

4-78. The HALT switch is a momentary-action type switch. When pressed, it places +4.5 volts through pins R and 54 of front panel coupler card A101 and pin 50 of timing generator card A106 to input pin 6 of HLS FF MC64 on the timing generator card. The output at pin 9 of MC64 will go false. This false signal is felt at input pin 2. Input pin 1 of MC64 is false due to open contacts 1 and 3 of the pressed HALT switch. Input pins 1 and 2 being false cause output pin 13 to go true. As long as the HALT switch is pressed, the output at pin 13 remains true. As soon as the HALT switch is released +4.5 volts is transferred to input pin 1 of MC64 which causes output pin 13 to go false.

4-79. The true condition at output pin 13 of MC64 is transferred to the direct reset input pin 9 of MC84 (RUN FF 1) causing its output pin 10 to go true. Output pin 10 of RUN FF 1 is connected through diode CR1 to the reset input pin 8 of MC74 (RUN FF 2) and at time T7S this flip-flop is reset. The outputs of both RUN flip-flops are transferred to the phase logic circuitry and by resetting these flip-flops no signals can be generated from the phase logic circuitry and all machine processing will stop. The output at pin 10 of RUN FF 2 is also transferred to the base of NPN transistor Q4 turning it on, completing the ground connection for the HALT indicator turning it on. The false output at pin 13 of RUN FF 2 is transferred to the base of transistor Q5 turning it off and turning off the RUN indicator.

4-80. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-3, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +7-volt dc supply at pin A of HALT indicator A502DS106. If normal, proceed to step "c". If abnormal, check the connection between A502DS106-A and A501-(+).

c. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of HALT switch A502S106. If normal, proceed to step "d". If abnormal, check the connection between A502S106-1,2 and A101-39.40.

d. At the computer front panel, press and release the POWER switch to turn off power. After checking to ensure that indicator lamp A502DS106 is not defective, proceed to step "e".

e. Using the extender card (part no. 02116-6040) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

f. At the computer front panel, press and release the POWER switch to turn on power.

g. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-50.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

h. At the computer front panel, press and hold the HALT switch and check the oscilloscope display for a +4.5-volt level. Then release the HALT switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A101MC84, and the HALT switch A502S106 as the most probable cause of trouble.

i. Place the channel A oscilloscope probe on A106MC64-13.

j. At the computer front panel, press and hold the HALT switch and check the oscilloscope display for a +4.5-volt level. Then release the HALT switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, check MC64 as the most probable cause of trouble.

k. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC84-10.

(6) Channel B input: A106TP1 (time T0).

l. At the computer front panel, press and release the RUN switch and check the oscilloscope display for a 0-volt level. Then press and release the HALT switch and check the oscilloscope for a +4.5-volt level. If the oscilloscope display is normal, proceed to step "m". If the oscilloscope display is abnormal, check A106MC84-1 for 200 ηs pulse occuring every 1.6 μs, check pin 8 for a 0-volt level, with the oscilloscope probe on A106MC84-14, repeatedly press and release the RUN switch and check the oscilloscope display for a 1.4 μs pulse occuring every 1.6 μs. If pin 1 is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits. If pin 8 is abnormal, refer to paragraph 4-81 and troubleshoot the PRESET switch circuit. If pin 14 is abnormal, refer to paragraph 4-71 and troubleshoot the RUN switch circuits.

m. Place the oscilloscope probe on A106MC74-10 (RUN FF 2). At the computer front panel, press and release the RUN switch and check the oscilloscope display for a 0-volt level. Then press and release the HALT switch and check the oscilloscope for a +4.5-volt level. If the oscilloscope display is normal, proceed to step "n". If the oscilloscope display is abnormal, check A106MC74-1 for a 45 ηs to 55 ηs pulse occuring every 1.6 μs, and check pin 8 for a +4.5-volt level. If pin 1 is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits. If pin 8 is abnormal, check diode CR1 for an open condition.

n. Place the oscilloscope probe on pin 8 of the 48-pin connector of A106 and check the oscilloscope display for a 0-volt level. At the computer front panel, press and release the RUN switch and check the oscilloscope display for a +7-volt level. If the oscilloscope display is normal, proceed to step "o". If the oscilloscope display is abnormal, check transistor Q4 for an open or shorted condition.

o. At the computer front panel, press and release the HALT switch and the POWER switch to turn off power.

p. Using a multi-function meter, check the connection between pin 8 of cable 106 and the HALT indicator A502DS106-B for continuity.

q. If all indications of the above test procedure are normal, the HALT switch and indicator circuits are operating normally. If one or more indications of the above test procedure are abnormal, refer to the related test procedures, diagrams, and schematics and troubleshoot the related circuits.

4-81. PRESET SWITCH AND INDICATOR. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with PRESET switch S108 and PRESET indicator lamp DS108 located on control panel assembly A502.

4-82. Description. The circuits associated with the PRESET switch and PRESET indicator are shown in figure 4-4. The timing diagram included in this figure shows the sequential events that occur when the PRESET switch is pressed and released. In the following description it is assumed that initially all flip-flops except the PH1 flip-flop are in the reset condition, the PRESET indicator is on, the RUN indicator is off, the HALT indicator is on, the FETCH indicator can be off or on, and the contacts of the PRESET switch are in the released position as shown.

4-83. The PRESET switch is a momentary-action type switch. When pressed, it places +4.5 volts through the switch and pin J of front panel coupler card A101 to pin 2 of "and" gate MC83A. The signal RF2 is transferred to pin 1 of MC83A and RUN FF 2 reset output pin 10 on timing generator card A106. Therefore the machine must be in a halt mode for the PRESET switch to be effective. The signal PRS at output pin 14 of MC83A is transferred through pin 30 of the front panel coupler card, and pin 78 of power fail interrupt card A1, to input pin 6 of MC47 (FLAG FF) on the power fail interrupt card. With a true signal at input pin 6 of MC47, the FLAG FF is reset and output pin 9 will go false if input pin 1 of MC47 is false. This causes transistor Q1 of the power fail card to stop conducting and the PRESET indicator to go out.

4-84. Signal PRS is also transferred through pin 78 of timing generator card A106 to input pin 6 of MC115 (PRS FF) on the timing generator card. This causes output pin 9 of MC115 to go false. This false output is transferred to input pin 2 of MC115. Input pin 1 of MC115 is false due to open contacts 1 and 3 of the pressed PRESET switch. The two false inputs at pins 1 and 2 of MC115 cause output pin 13 to go true. This true output is transferred to input pin 14 of "and" gate MC114A and at time T5 causes the signal POPIO to be generated at output pin 13 of MC114A. This signal is transferred through pin 61 of the timing generator card to the I/O control card A201 where it conditions the I/O section for data transfer. The true output of MC115 is also transferred through the single input "and" gates MC106C and MC106A to the reset input pin 8 of MC84 (RUN FF1) to the direct reset pin 9 of MC74 (RUN FF 2) and through "and" gate MC53B to the set input pin 14 of MC44 (PH1 FF). This forces RUN FF 1 to be reset at the first time T5 after the PRESET switch is pressed, RUN FF 2 to be reset immediately assuring that the RUN indicator will be off and the HALT indicator will be on, and causing PH1 FF to be set if the PHASE switch (PNS) is in the NORM position, at the first time T7 and TS after the PRESET switch is pressed and turn on the FETCH indicator. Thus, pressing the PRESET switch will precondition the computer for phase 1 (FETCH phase) operation.

4-85. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-4, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +7-volt dc supply at pin A of PRESET indicator A502DS108. If normal, proceed to step "c". If abnormal, check the connection between A502DS108-A and A501-(+).

c. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S108. If normal, proceed to step "d". If abnormal, check the connection between A502S108-1,2 and A101-39,40.

d. At the computer front panel, press and release the POWER switch to turn off power. After checking to ensure that indicator lamp A502DS108 is not defective, proceed to step "e".

e. Using the extender card (part no. 02115-6047) extend power fail interrupt card A1 from the card cage.

f. At the computer front panel, press and release the POWER switch to turn on power.

g. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A1-78.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

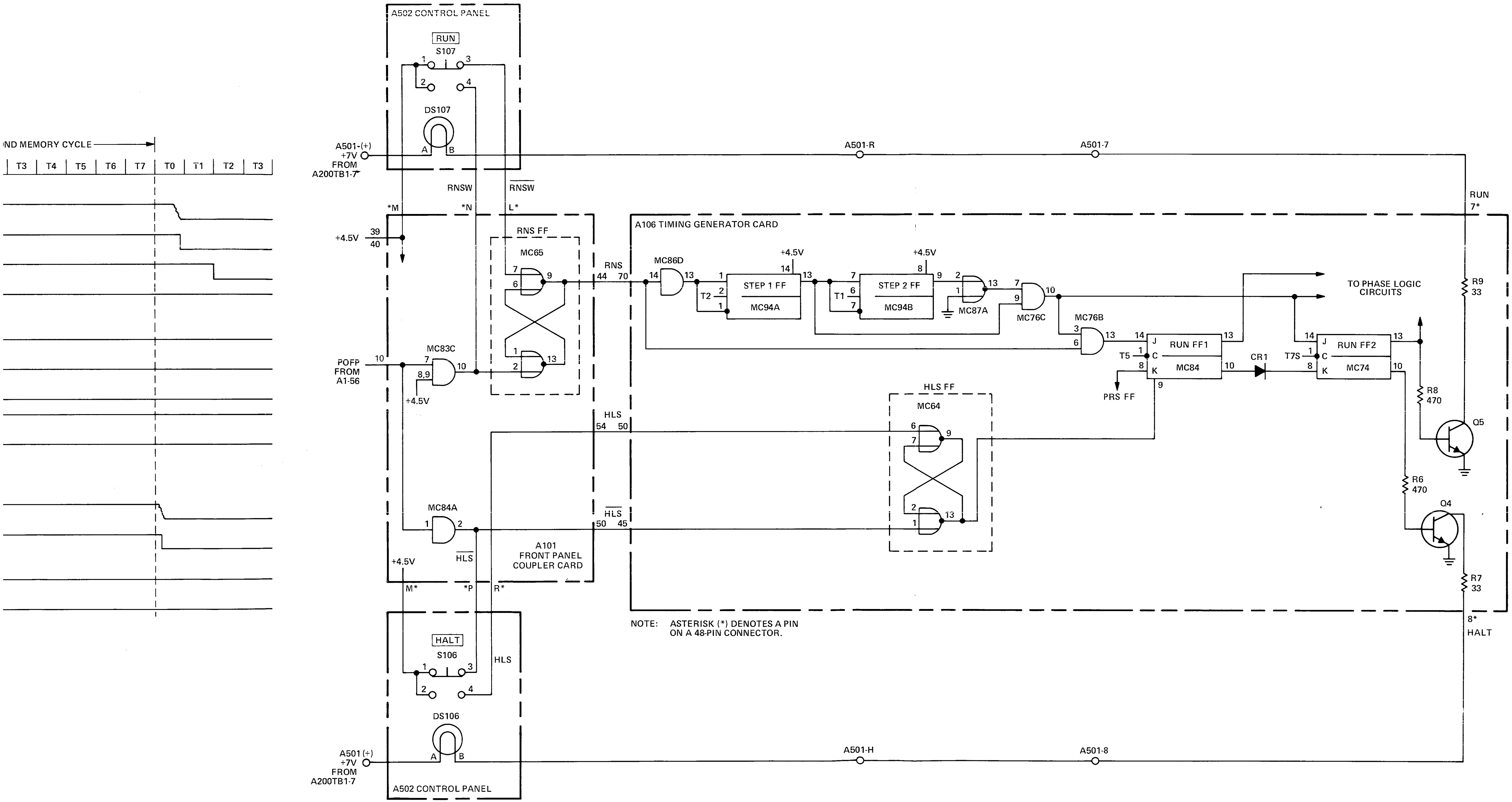
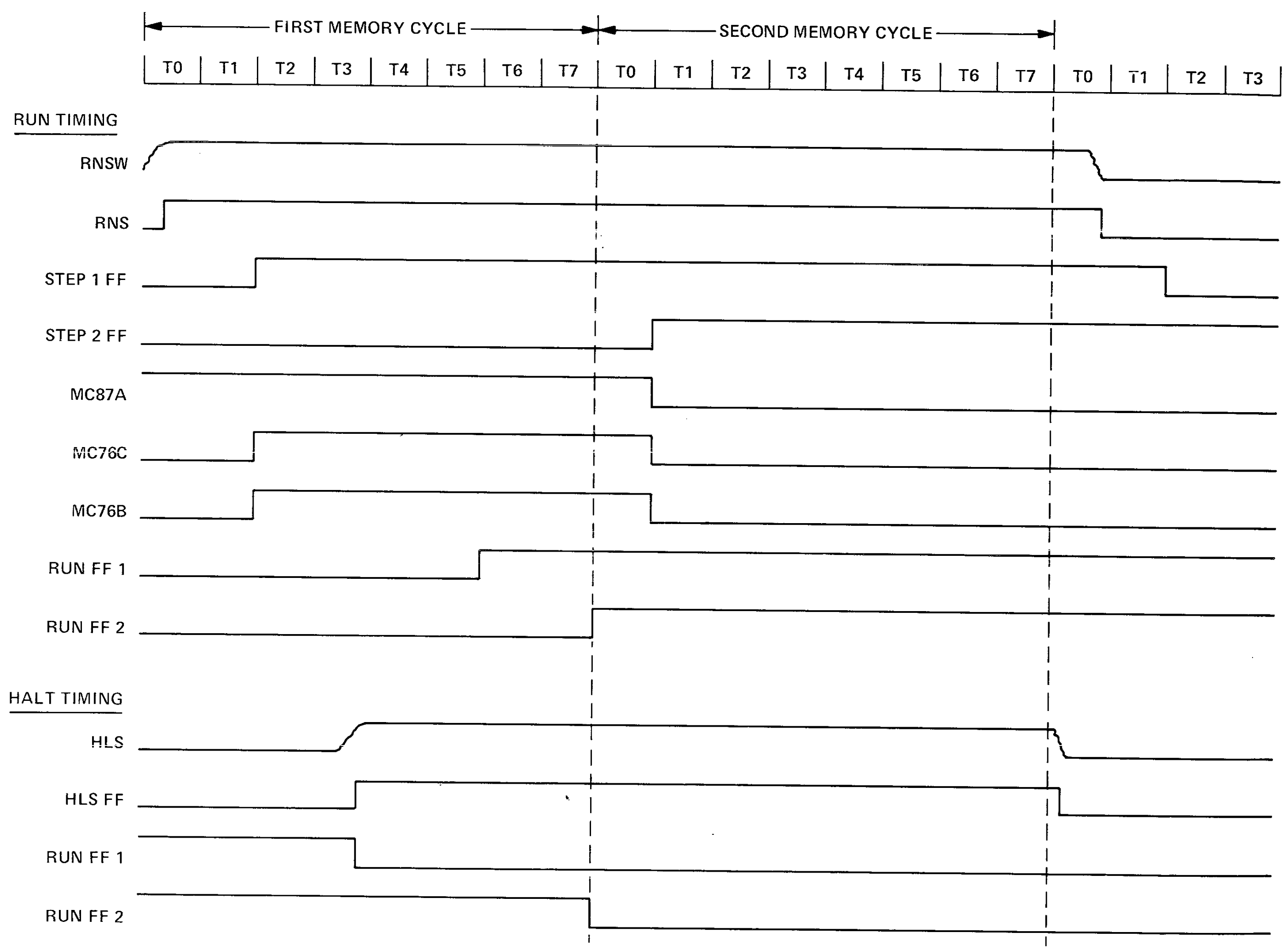
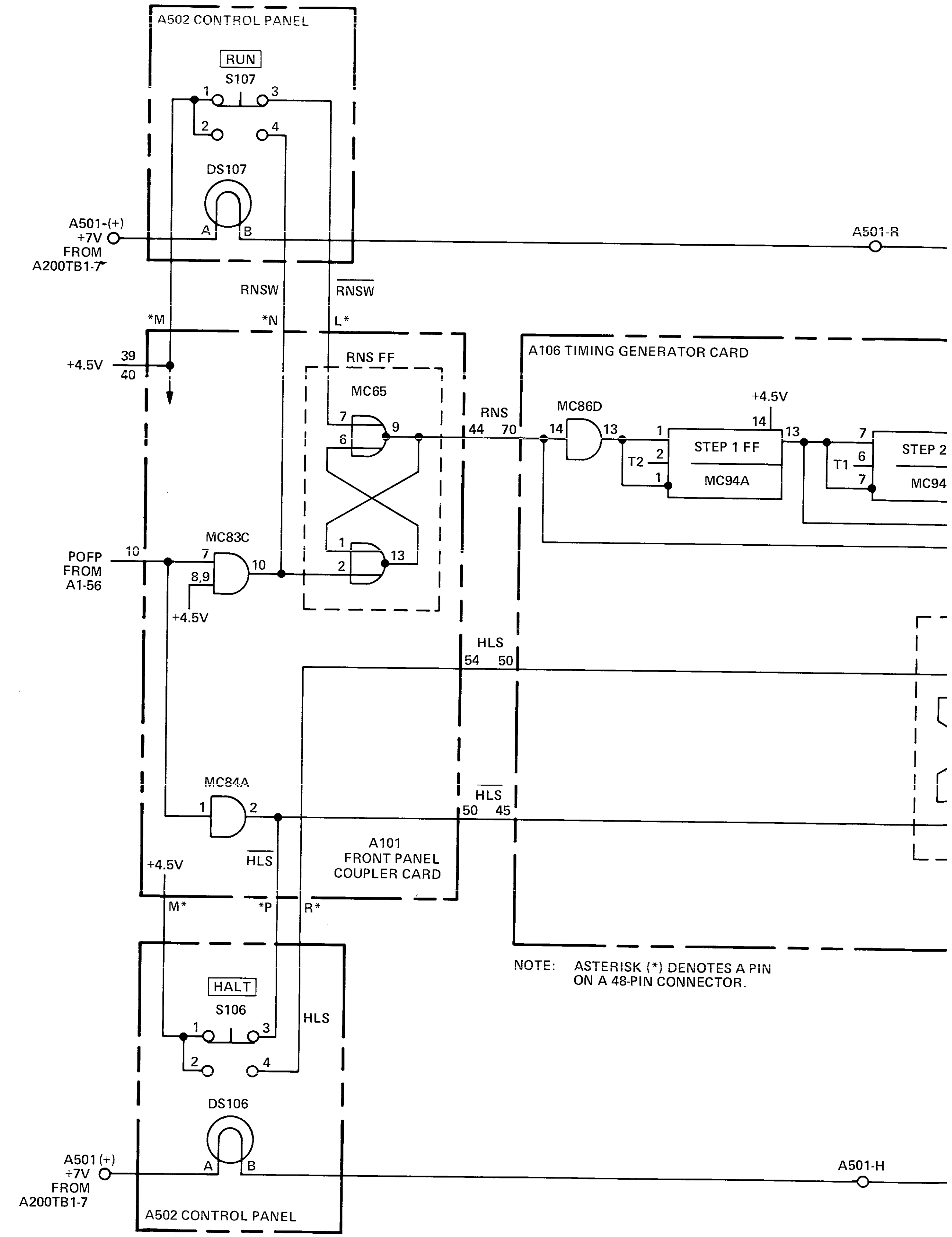


Figure 4-3. RUN and HALT Switch and Indicator Circuits, Servicing Diagram


FIRST MEMORY CYCLE
SECOND MEMORY CYCLE
T0 T1 T2 T3 T4 T5 T6 T7 T0 T1 T2 T3 T4 T5 T6 T7 T0 T1 T2 T3
RUN TIMING
RNSW
RNS
STEP 1 FF
STEP 2 FF
MC87A
MC76C
MC76B
RUN FF 1
RUN FF 2
HALT TIMING
HLS
HLS FF
RUN FF 1
RUN FF 2


A502 CONTROL PANEL
RUN
S107
DS107
A501-(+)
+7V
FROM
A200TB1-7
A501-R
RNSW
RNS FF
MC65
A106 TIMING GENERATOR CARD
+4.5V
RNS
MC86D
STEP 1 FF
MC94A
STEP 2
MC94
POFP
FROM
A1-56
MC83C
HLS
MC84A
A101
FRONT PANEL
COUPLER CARD
NOTE: ASTERISK (*) DENOTES A PIN ON A 48-PIN CONNECTOR.
HALT
S106
DS106
A501 (+)
+7V
FROM
A200TB1-7
A501-H
A502 CONTROL PANEL

2019-160

h. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a +4.5-volt level. Then release the PRESET switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A101MC83 and the PRESET switch A502S108 as the most probable cause of trouble.

i. Place the channel A oscilloscope probe on A1MC47-9.

j. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a 0-volt level. Then release the PRESET switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, refer to the power fail interrupt schematic and check MC47 and its input circuits as the most probable cause of trouble.

k. Place the channel A oscilloscope probe on the collector of transistor Q1 and check the oscilloscope display for a +7-volt level. If the oscilloscope display is normal, proceed to step "l". If the oscilloscope display is abnormal, check transistor Q1 for a shorted condition, resistor R1 for an open condition, and the connection between A1-35 and A502DS108-B for continuity.

l. At the computer front panel, press and release the POWER switch to turn off power.

m. Using the extender card and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

n. At the computer front panel, press and release the POWER switch to turn on power.

o. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC115-13.

(6) Channel B input: A106TP1 (time T0).

p. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a +4.5-volt level. Then release the PRESET switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check MC115 (PRS FF) and the connection between A101-30 and A106-78 as the most probable causes of trouble.

q. Place the channel A oscilloscope probe on A106MC114-13. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a 200 ηs pulse occuring every 1.6 μs. If the oscilloscope display is normal, proceed to step "r". If the oscilloscope display is abnormal, check A106MC114-2 for the 200 ηs pulse above referred to. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

r. Place the channel A oscilloscope probe on A106MC84-8 (RUN FF 1). At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a +4.5-volt level. If the oscilloscope display is normal, proceed to step "s". If the oscilloscope display is abnormal, check A106MC106-9 in the same manner.

s. If, at this point in the test procedure, all checks have indicated normal operation but the RUN or HALT indicators are not off and on respectively, refer to paragraphs 4-71 and 4-76 and troubleshoot the RUN and HALT switches. If the checks have indicated normal operation and the RUN and HALT indicators are off and on respectively, proceed to step "t".

t. Place the channel A oscilloscope probe on A106MC53-13. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a +4.5-volt level. Then release the PRESET switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "u". If the oscilloscope display is abnormal, check A106MC53-6 for a +4.5-volt level.

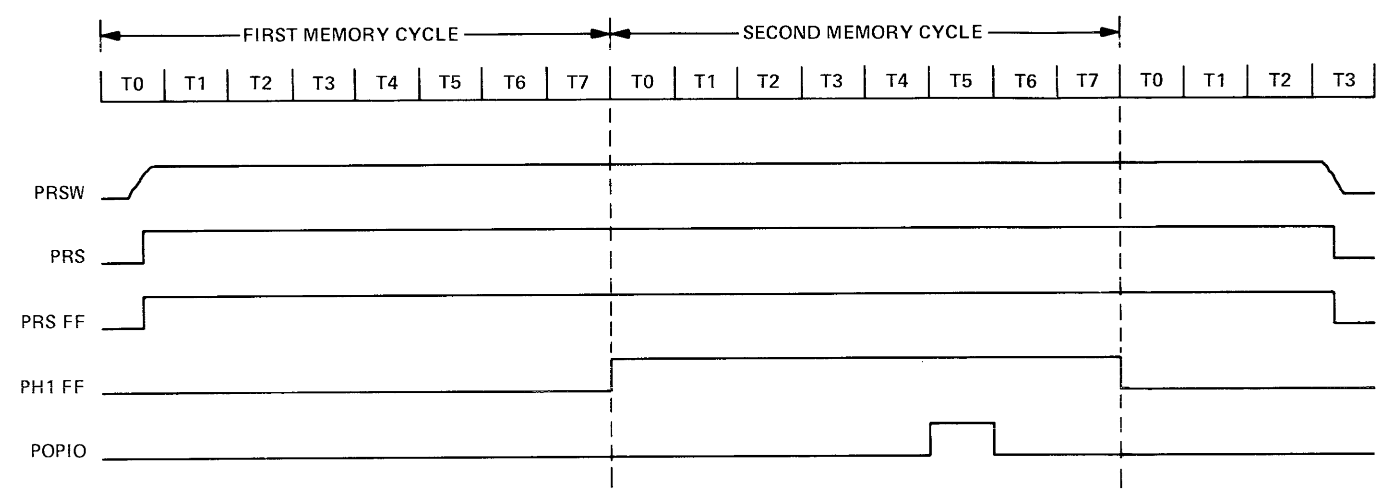
u. Place the channel A oscilloscope probe on A106MC44-13 (PH1 FF) and check the oscilloscope display for a +4.5-volt level. If the oscilloscope display is normal, proceed to step "v". If the oscilloscope display is abnormal, check A106MC44-1 for a 45 ηs to 55 ηs pulse occuring every 1.6 μs and A106MC44-8 for a 0-volt level. If these pins are abnormal, refer to paragraphs 4-141 and 4-164 and the timing generator schematic and check the PHASE switch circuits, the phase logic circuits and A106MC35 as the most probable cause of trouble.

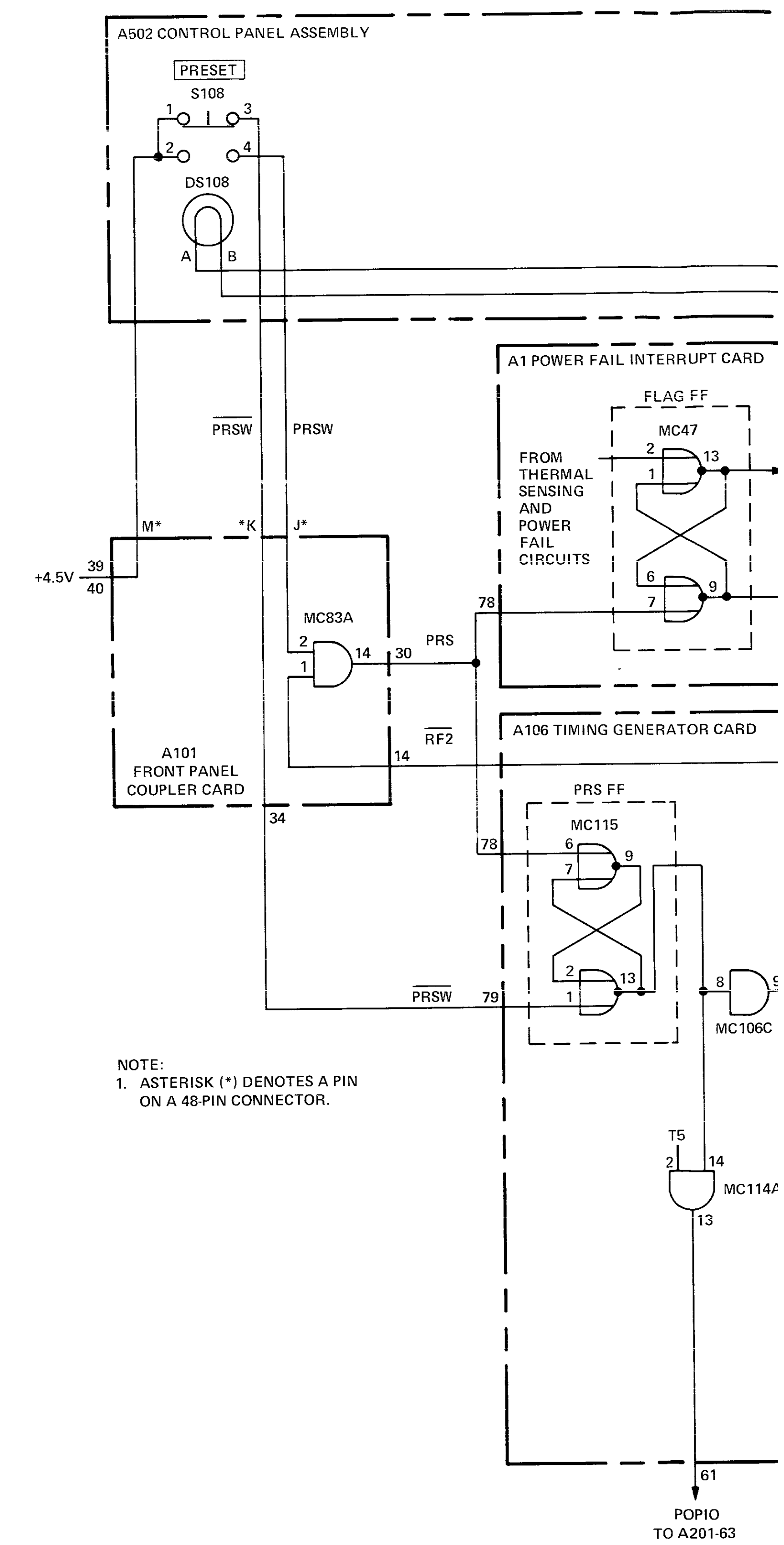
v. Place the channel A oscilloscope probe on the collector of transistor A106Q6 and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "w". If the oscilloscope display is abnormal, check transistor A106Q6 for an open condition.

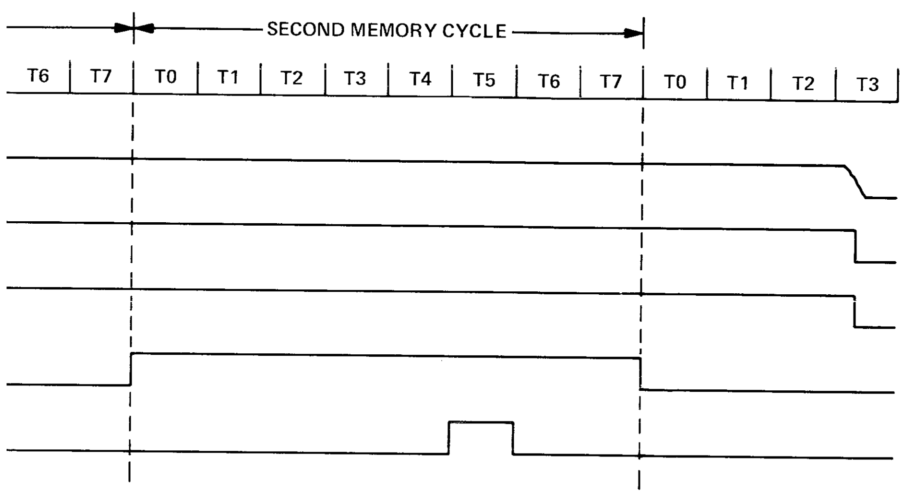
w. At the computer front panel, press and release the POWER switch to turn off power.

x. Using a multi-function meter, check the line between pin 3 of cable 106 and the FETCH indicator A501DS84 and A501-(+) for continuity.

y. If all indications of the above test procedure are normal, the PRESET switch and indicator circuits are operating normally.


FIRST MEMORY CYCLE
SECOND MEMORY CYCLE
T0
T1
T2
T3
T4
T5
T6
T7
PRSW
PRS
PRS FF
PH1 FF
POPIO


A502 CONTROL PANEL ASSEMBLY
PRESET
S108
DS108
A1 POWER FAIL INTERRUPT CARD
FLAG FF
MC47
FROM THERMAL SENSING AND POWER FAIL CIRCUITS
PRSW
+4.5V
MC83A
PRS
RF2
A101 FRONT PANEL COUPLER CARD
A106 TIMING GENERATOR CARD
PRS FF
MC115
MC106C
T5
MC114A
POPIO TO A201-63 (I/O SECTION)
NOTE:
1. ASTERISK (*) DENOTES A PIN ON A 48-PIN CONNECTOR.



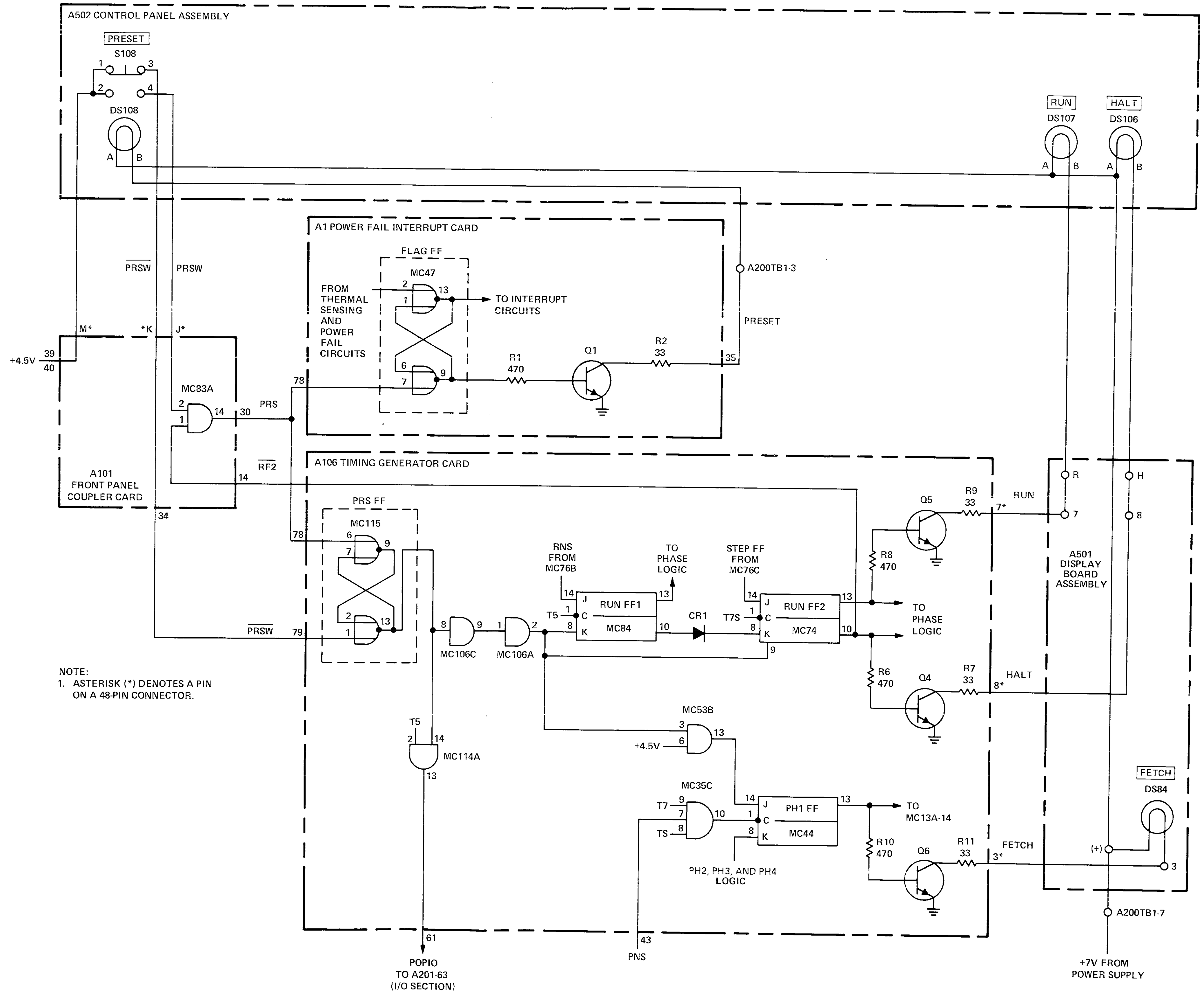


Figure 4-4. PRESET Switch and Indicator Circuit, Servicing Diagram

4-86. LOAD A SWITCH, A-REGISTER INDICATORS, AND SWITCH REGISTER SWITCHES. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with LOAD A switch S104 and the SWITCH REGISTER switches located on control panel assembly A502, and the A-REGISTER indicators located on display board assembly A501.

4-87. Description. The circuits associated with the LOAD A switch are shown in figure 4-5. The timing diagram included in this figure shows the sequential events that occur when the LOAD A switch is pressed and released. In the following description it is assumed that initially all flip-flops shown are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the LOAD A switch are in the released position as shown.

4-88. The LOAD A switch is a momentary-action type switch. When pressed, it places +4.5 volts through the switch and pin T of front panel coupler card A101 to pin 3 of "and" gate MC93B. The signal $\overline{RF2}$ is transferred to A101MC93-6 from A106MC74-10 (RUN FF 2) on timing generator card A106. Therefore the machine must be in a halt mode for the LOAD A switch to be effective. With a true signal at input pins 3 and 6 of MC93B output pin 13 will go true. This true signal is transferred to A101MC85-2 (LOAD A FF) causing A101MC85-13 to go false. This false signal is felt at A101MC85-6. Input pin 7 of MC85 is false due to open contacts 1 and 3 of the pressed LOAD A switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signal LAS at pin 62 of front panel coupler card A101. As long as the LOAD A switch is pressed, signal LAS remains true. As soon as the LOAD A switch is released, +4.5 volts is transferred to A101MC85-7 which causes output pin 9 to go false.

4-89. The signal LAS is transferred through pin 62 of the front panel coupler card, and pin 80 of the timing generator card to pin 1 of "and" gate MC117A and pin 14 of "and" gate MC116A. At time T2 the signal SWSA is generated by MC117A at output pin 14. This signal is transferred through pin 84 of the timing generator card and pin 35 of the instruction decoder card A107 to pin 2 of "and" gate MC77A. At time T2 and TS the signal STBA is generated at the output pin 13 of MC77A. This signal is transferred through pin 50 of the instruction decoder card and pin 38 of the arithmetic logic cards A102 through A105 to the clock input pin 1 of the A-register flip-flops and is used to clock the data on the T-bus into the A-register flip-flops.

4-90. As soon as the signal LAS is true at pin 14 of MC116A the signal SEO is generated at pin 13 of MC116A of the timing generator card. This signal is transferred through pin 72 of the timing generator card and pin 22 of the shift logic card A108 where it is used to generate the signal ISR, which enables the switch register gates on the front panel coupler card and transfers the switch register data to the IOBI lines. At time T2 the signal SEO also generates the signal IOI which is used to gate the data on the IOBI lines to the S-bus. The signal SEO is also transferred to pin 77 of the instruction decoder card where at time T2 it is used to generate the negative going signal EOFE at pin 13 of MC112A on the instruction decoder card. The signal EOFE is transferred through pin 67 of the instruction decoder card and pin 83 of the direct memory logic card A20 where it is used to generate the negative going signal EOF at pin 9 of "and" gate MC107B on the direct memory logic card. This signal is transferred through pin 75 of the direct memory logic card and pin 76 of the arithmetic logic cards. The signal EOF is used in the arithmetic logic cards to gate the data on the S-bus and R-bus to the T-bus. (The R-bus is cleared to all "zeros" at this time.) The T-bus data is then placed into the A-register flip-flops by the clock pulse STBA and each "1" bit will be indicated by a lighted A-register indicator lamp. Thus the LOAD A switch, when pressed, transfers the switch register data into the A-register and each switch that was in the up ("1") position will cause the corresponding A-register indicator lamp to light.

4-91. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-5, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S104. If normal, proceed to step "c". If abnormal, check the connection between A502S104-1,2 and A101-39,40 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047) and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

e. At the computer front panel, press and release the POWER switch to turn on power.

f. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-80.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

g. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD A switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "h". If the oscilloscope display is abnormal, check A101MC85, A101MC93B, and the LOAD A switch A502S104 and A106MC74 as the most probable cause of trouble.

h. Place the oscilloscope probe on A106M116-13.

i. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD A switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "j". If the oscilloscope display is abnormal, check A106MC116 as the most probable cause of trouble.

j. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC117-14.

(6) Channel B input: A106TP1 (time T0).

k. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a 200 ηs pulse occuring every 1.6 μs. If the oscilloscope display is normal, proceed to step "l". If the oscilloscope display is abnormal, check A106MC117-2 for the 200 ηs pulse referred to above. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

l. At the computer front panel, press and release the POWER switch to turn off power.

m. Using the extender card, extend shift logic card A108 from the card cage.

n. At the computer front panel, press and release the POWER switch to turn on power.

o. Place the channel A oscilloscope probe on pin 84 of the shift logic card.

p. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD A switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check A108MC106A and A108MC-127A as the most probable cause of trouble.

q. Place the channel A oscilloscope probe on pin 44 of the shift logic card. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a 200 ηs pulse occuring every 1.6 μs. If the oscilloscope display is normal, proceed to step "r". If the oscilloscope display is abnormal, check MC44A and MC64A as the most probable cause of trouble.

r. At the computer front panel, press and release the POWER switch to turn off power.

s. Using the extender card, extend instruction decoder card A107 from the card cage.

t. At the computer front panel, press and release the POWER switch to turn on power.

u. Place the channel A oscilloscope probe on pin 67 of the instruction decoder card. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "v". If the oscilloscope display is abnormal, check MC112A and MC122A as the most probable cause of trouble.

v. Place the channel A oscilloscope probe on pin 50 of the instruction decoder card. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "w". If the oscilloscope display is abnormal, check MC77A as the most probable cause of trouble.

w. At the computer front panel, press and release the POWER switch to turn off power.

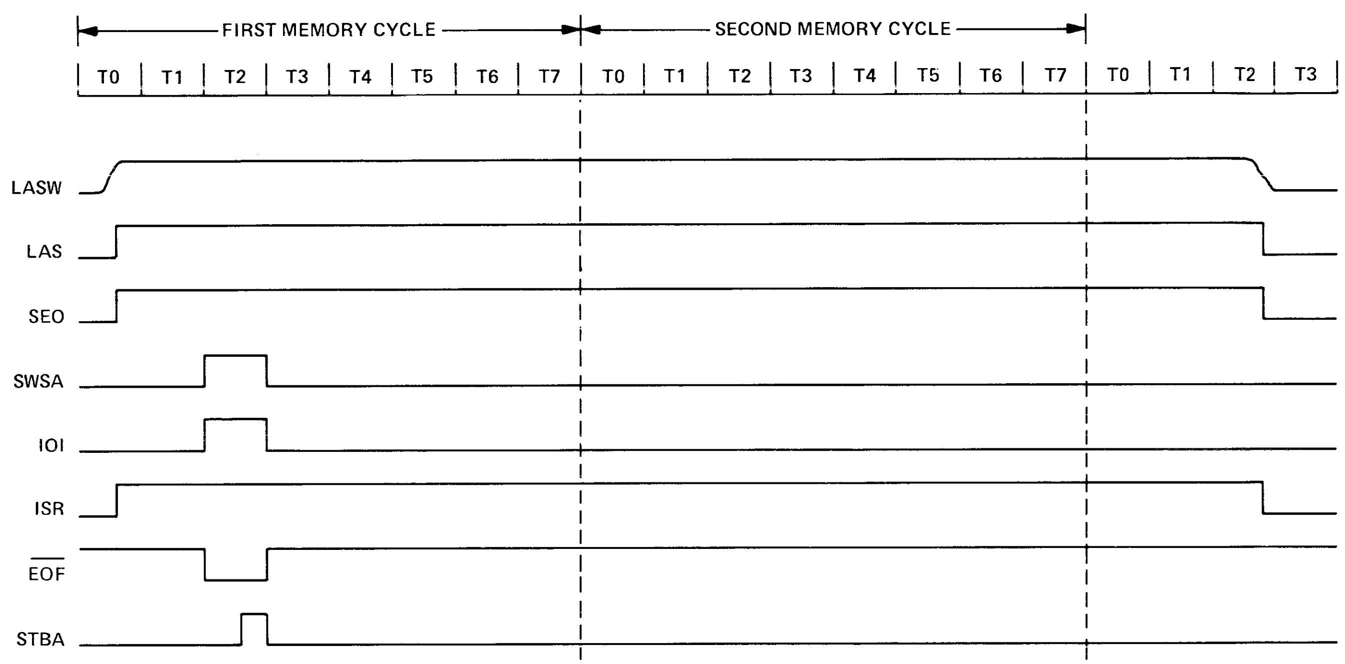
x. Using the extender card, extend direct memory logic card A20 from the card cage.

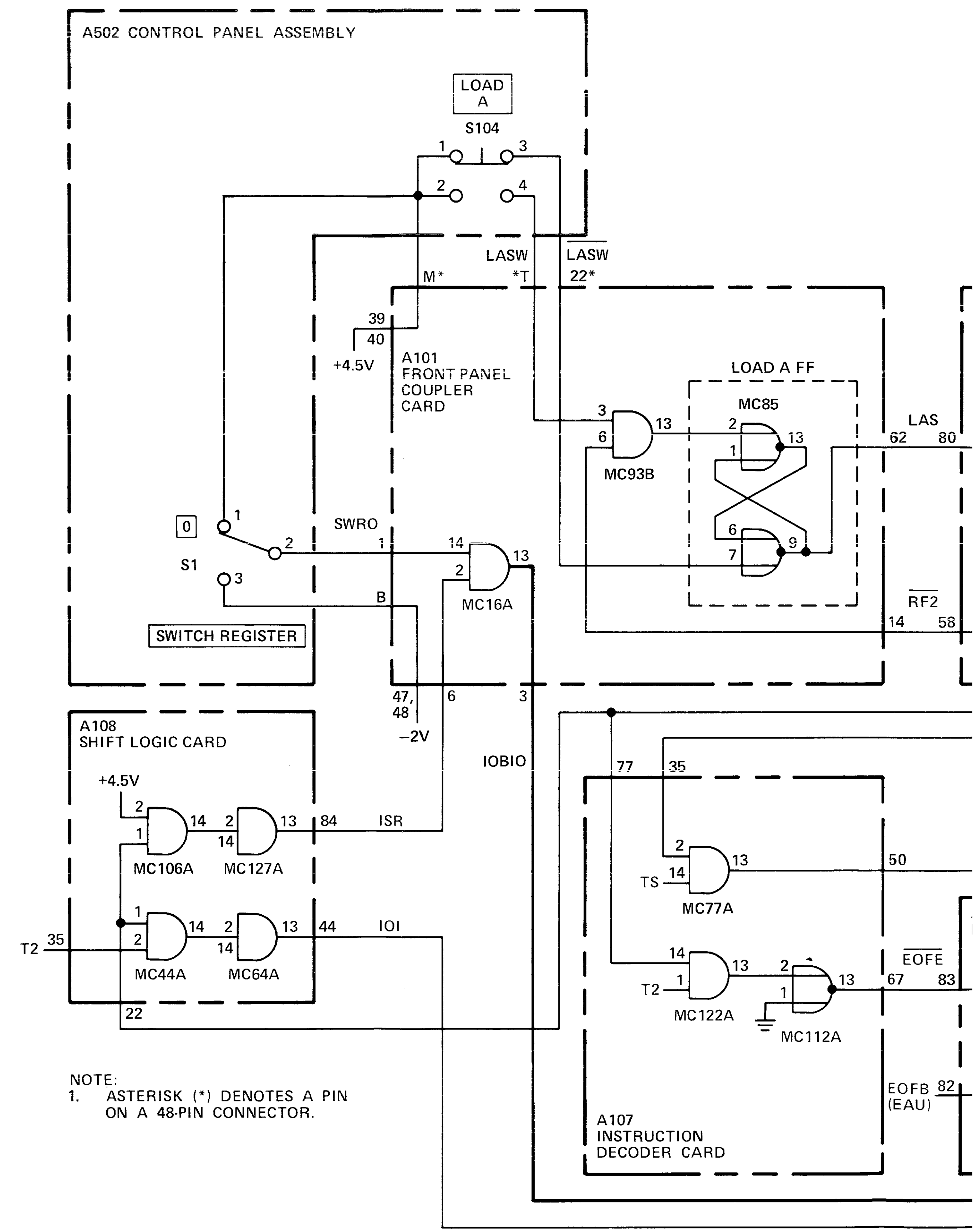
y. At the computer front panel, press and release the POWER switch to turn on power.

z. Place the channel A oscilloscope probe on pin 75 of the direct memory logic card. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "aa". If the oscilloscope display is abnormal, check MC97B and MC107B as the most probable cause of trouble.

aa. If, at this point in the test procedure, all checks have indicated normal operation but by pressing the LOAD A switch the switch register data is not being properly transferred into the A-register and displayed by the A-register indicator lamps, refer to figure 4-5 and check the arithmetic logic card A102 through A105 that controls the A-register bit or bits in question. Also check the particular switch register switch or switches on control panel A502 and the switch register gate or gates on front panel coupler card A101 for proper operation. Also check the cable connection from the arithmetic logic card, through the A-register indicator lamp or lamps, to the +7-volt connection on display board assembly A501-(+) for continuity.

bb. If all indications of the above test procedures are normal, the LOAD A switch and circuits are operating normally.





NOTE:
1. ASTERISK (*) DENOTES A PIN ON A 48-PIN CONNECTOR.

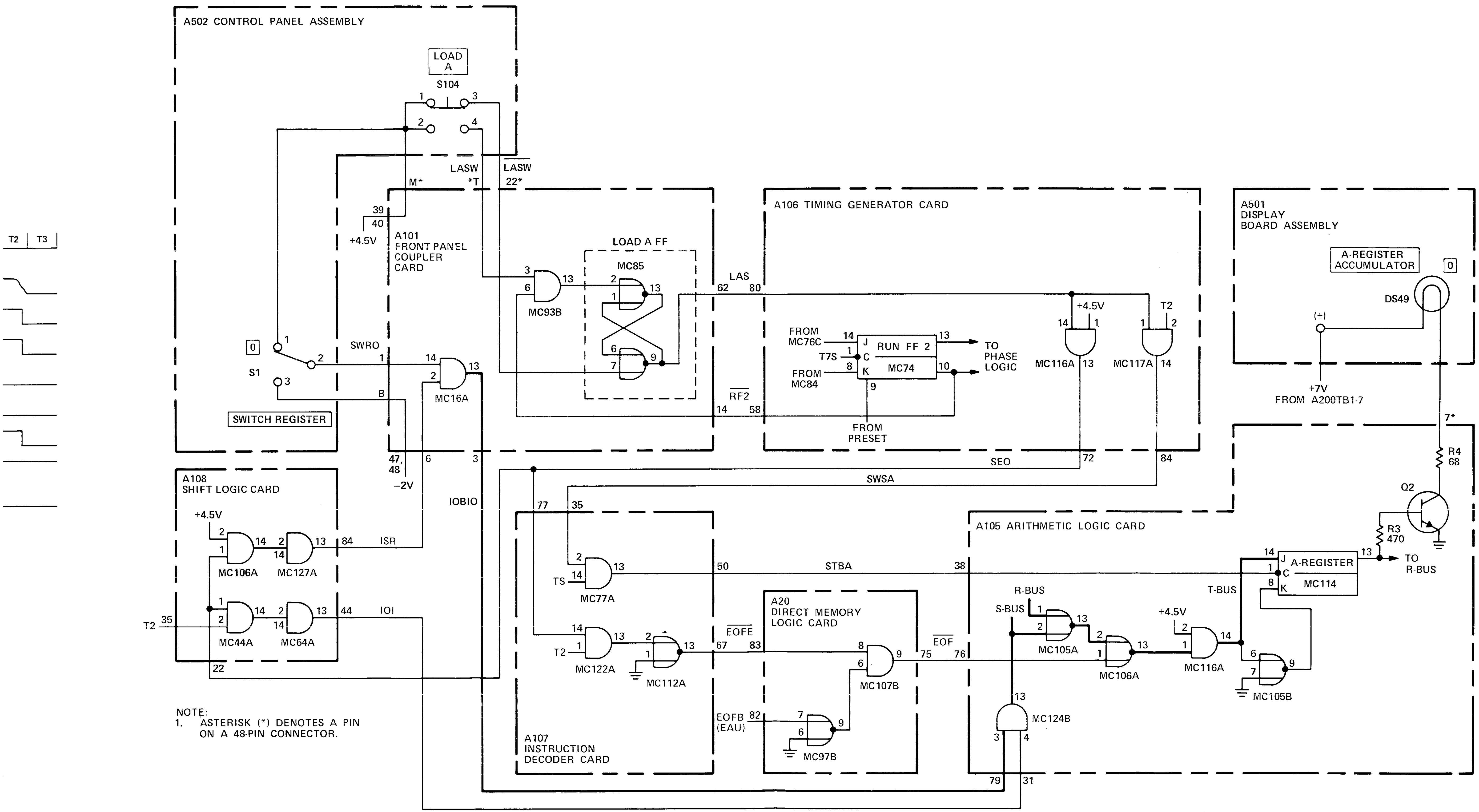


Figure 4-5. LOAD A Switch Circuit, Servicing Diagram

4-92. LOAD B SWITCH, B-REGISTER INDICATORS, AND SWITCH REGISTER SWITCHES. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with LOAD B switch S103 and the SWITCH REGISTER switches located on control panel assembly A502, and the B-REGISTER indicators located on display board assembly A501.

4-93. Description. The circuits associated with the LOAD B switch are shown in figure 4-6. The timing diagram included in the figure shows the sequential events that occur when the LOAD B switch is pressed and released. In the following description it is assumed that initially all flip-flops shown are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the LOAD B switch are in the released position as shown.

4-94. The LOAD B switch is a momentary-action type switch. When pressed, it places +4.5 volts through the switch and pin U of front panel coupler card A101 to pins 8 and 9 of "and" gate MC93C. The signal $\overline{\text{RF2}}$ is transferred to A101MC93-7 from A106MC74-10 (RUN FF 2) on timing generator card A106. Therefore the machine must be in a halt mode for the LOAD B switch to be effective. With a true signal at input pins 8, 9 and 7 of MC93C output pin 10 will go true. This true signal is transferred to A101MC95-2 of (LOAD B FF) causing A101MC95-13 to go false. This false signal is felt at A101MC85-6. Input pin 7 of MC95 is false due to open contacts 1 and 3 of the pressed LOAD B switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signal LBS at pin 66 of front panel coupler card A101. As long as the LOAD B switch is pressed, signal LBS remains true. As soon as the LOAD B switch is released, +4.5 volts is transferred to A101MC95-7 which causes output pin 9 to go false.

4-95. The signal LBS is transferred through pin 66 of the front panel coupler card, and pin 65 of the timing generator card to pin 6 of "and" gate MC117B and pin 2 of "and" gate MC116B. At time T2 the signal SWSB is generated by MC117B at output pin 13. This signal is transferred through pin 71 of the timing generator card and pin 24 of the instruction decoder card A107 to pin 6 of "and" gate MC77B. At time T2 and TS the signal STBB is generated at the output pin 9 of MC77B. This signal is transferred through pin 51 of the instruction decoder card and pin 26 of the arithmetic logic cards A102 through A105 to the clock input pin 1 of the B-register flip-flops and is used to clock the data on the T-bus into the B-register flip-flops.

4-96. As soon as the signal LBS is true at pin 2 of MC116B the signal SEO is generated at pin 13 of MC116B of the timing generator card. This signal is transferred through pin 72 of the timing generator card and pin 22 of the shift logic card A108 where it is used to generate the signal ISR, which enables the switch register gages on the front panel coupler card and transfers the switch register data to the IOBI lines. At time T2 the signal SEO also generates the signal IOI which is used to gate the data on the IOBI lines to the S-bus. The signal SEO is also transferred to pin 77 of the instruction decoder card where at time T2 it is used to generate the negative going signal $\overline{\text{EOFE}}$ at pin 13 of MC112A on the instruction decoder card. The signal $\overline{\text{EOFE}}$ is transferred through pin 67 of the instruction decoder card and pin 83 of the direct memory logic card A20 where it is used to generate the negative going signal $\overline{\text{EOF}}$ at pin 9 of "and" gate MC107B on the direct memory logic card. This signal is transferred through pin 75 of the direct memory logic card and pin 76 of the arithmetic logic cards. The signal $\overline{\text{EOF}}$ is used in the arithmetic logic cards to gate the data on the S-bus and R-bus to the T-bus. (The R-bus is cleared to "zeros" at this time.) The T-bus data is then placed into the B-register flip-flops by the clock pulse STBB and each "1" bit will be indicated by a lighted B-register indicator lamp. Thus the LOAD B switch, when pressed, transfers the switch register data into the B-register and each switch that was in the up ("1") position will cause the corresponding B-register indicator lamp to light.

4-97. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-6, proceed as follows:

a. At the front of the computer, open the door assemlby to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S103. If normal, proceed to step "c". If abnormal, check the connection between A502S103-1,2 and A101-39,40 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047) and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

e. At the computer front panel, press and release the POWER switch to turn on power.

f. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-65.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the trouble-shooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

g. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD B switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "h". If the oscilloscope display is abnormal, check A101MC95, A101MC93C, and the LOAD B switch A502S103 and A106MC74 as the most probable cause of trouble.

h. Place the oscilloscope probe on A106MC116-13.

i. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD B switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "j". If the oscilloscope display is abnormal, check A106MC116 as the most probable cause of trouble.

j. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC117-13.

(6) Channel B input: A106TP1 (time T0).

k. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "l". If the oscilloscope display is abnormal, check A106MC117-3 for the 200 ηs pulse referred to above. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

l. At the computer front panel, press and release the POWER switch to turn off power.

m. Using the extender card, extend shift logic card A108 from the card cage.

n. At the computer front panel, press and release the POWER switch to turn on power.

o. Place the channel A oscilloscope probe on pin 84 of the shift logic card.

p. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD B switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check A108MC106A and A108MC127A as the most probable cause of trouble.

q. Place the channel A oscilloscope probe on pin 44 of the shift logic card. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "r". If the oscilloscope display is abnormal, check MC44A and MC64A as the most probable cause of trouble.

r. At the computer front panel, press and release the POWER switch to turn off power.

s. Using the extender card, extend instruction decoder card A107 from the card cage.

t. At the computer front panel, press and release the POWER switch to turn on power.

u. Place the channel A oscilloscope probe on pin 67 of the instruction decoder card. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "v". If the oscilloscope display is abnormal, check MC112A and MC122A as the most probable cause of trouble.

v. Place the channel A oscilloscope probe on pin 51 of the instruction decoder card. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "w". If the oscilloscope display is abnormal, check MC77B as the most probable cause of trouble.

w. At the computer front panel, press and release the POWER switch to turn off power.

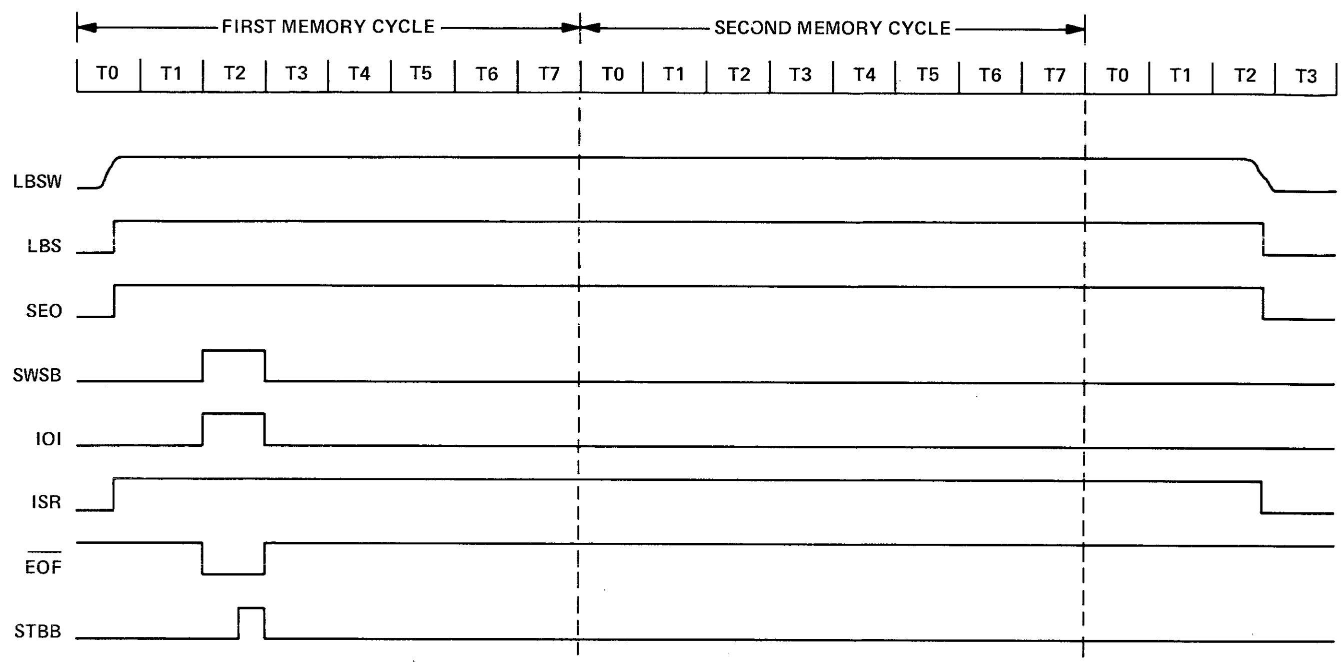
x. Using the extender card, extend direct memory logic card A20 from the card cage.

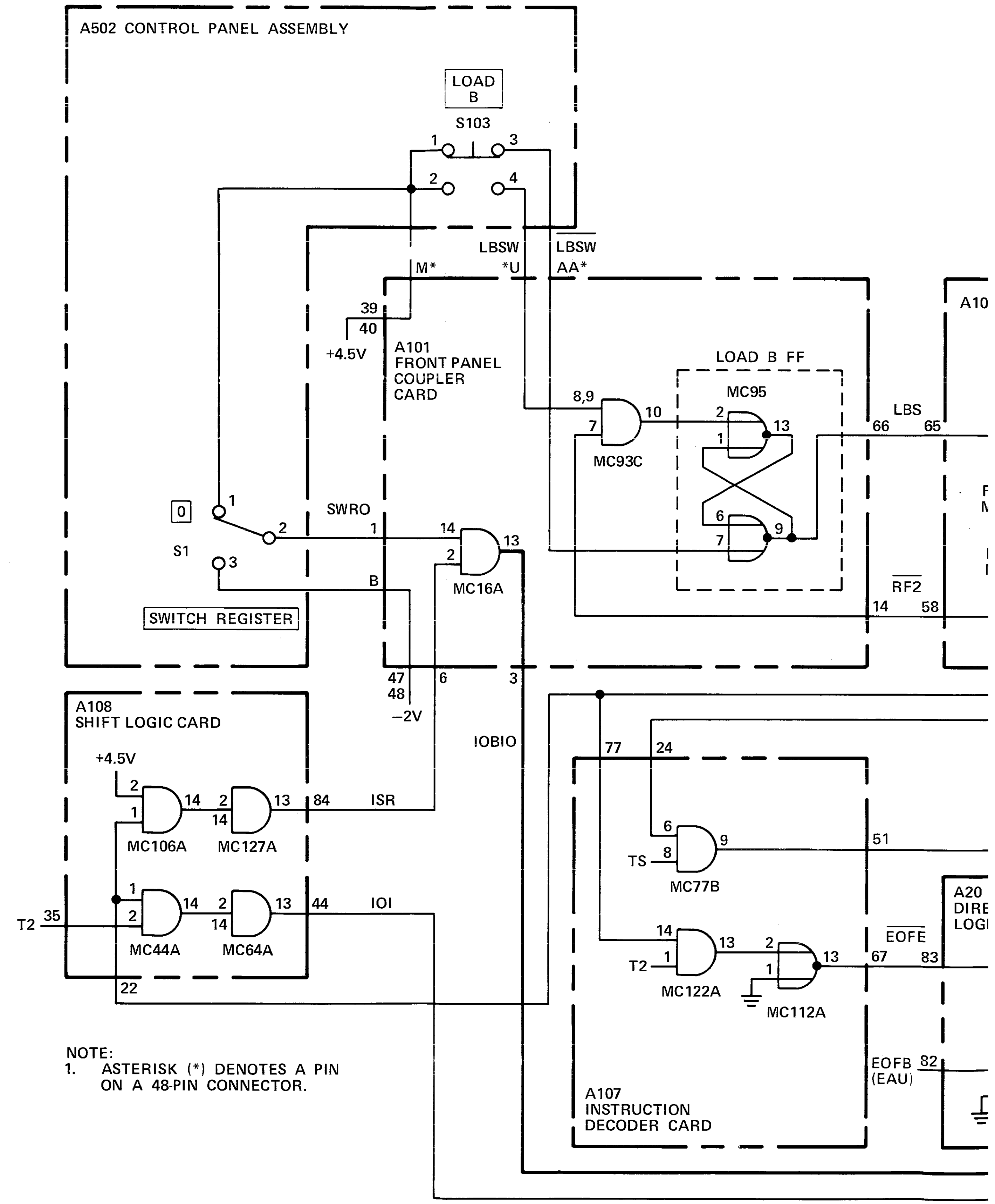
y. At the computer front panel, press and release the POWER switch to turn on power.

z. Place the channel A oscilloscope probe on pin 75 of the direct memory logic card. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a negative going 100 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "aa". If the oscilloscope display is abnormal, check MC97B and MC107B as the most probable cause of trouble.

aa. If, at this point in the test procedure, all checks have indicated normal operation but by pressing the LOAD B switch the switch register data is not being properly transferred into the B-register and displayed by the B-register indicator lamps, refer to figure 4-6 and check the arithmetic logic card A102 through A105 that controls the B-register bit or bits in question. Also check the particular switch register switch or switches on control panel A502 and the switch register gate or gates on front panel coupler card A101 for proper operation. Also check the cable connection from the arithmetic logic card, through the B-register indicator lamp or lamps, to the +7-volt connection on display board assembly A501-(†) for continuity.

bb. If all indications of the above test procedure are normal, the LOAD B switch and circuits are operating normally.


FIRST MEMORY CYCLE
SECOND MEMORY CYCLE
T0 T1 T2 T3 T4 T5 T6 T7 T0 T1 T2 T3 T4 T5 T6 T7 T0 T1 T2 T3
LBSW
LBS
SEO
SWSB
IOI
ISR
EOF
STBB


A502 CONTROL PANEL ASSEMBLY
LOAD B
S103
LBSW
LBSW
M*
*U
AA*
+4.5V
A101 FRONT PANEL COUPLER CARD
LOAD B FF
MC95
MC93C
LBS
A10
SWRO
S1
SWITCH REGISTER
MC16A
RF2
−2V
IOBIO
A108 SHIFT LOGIC CARD
+4.5V
MC106A
MC127A
ISR
IOI
MC44A
MC64A
T2
TS
MC77B
MC122A
MC112A
EOFE
EOFB (EAU)
A107 INSTRUCTION DECODER CARD
NOTE:
1. ASTERISK (*) DENOTES A PIN ON A 48-PIN CONNECTOR.

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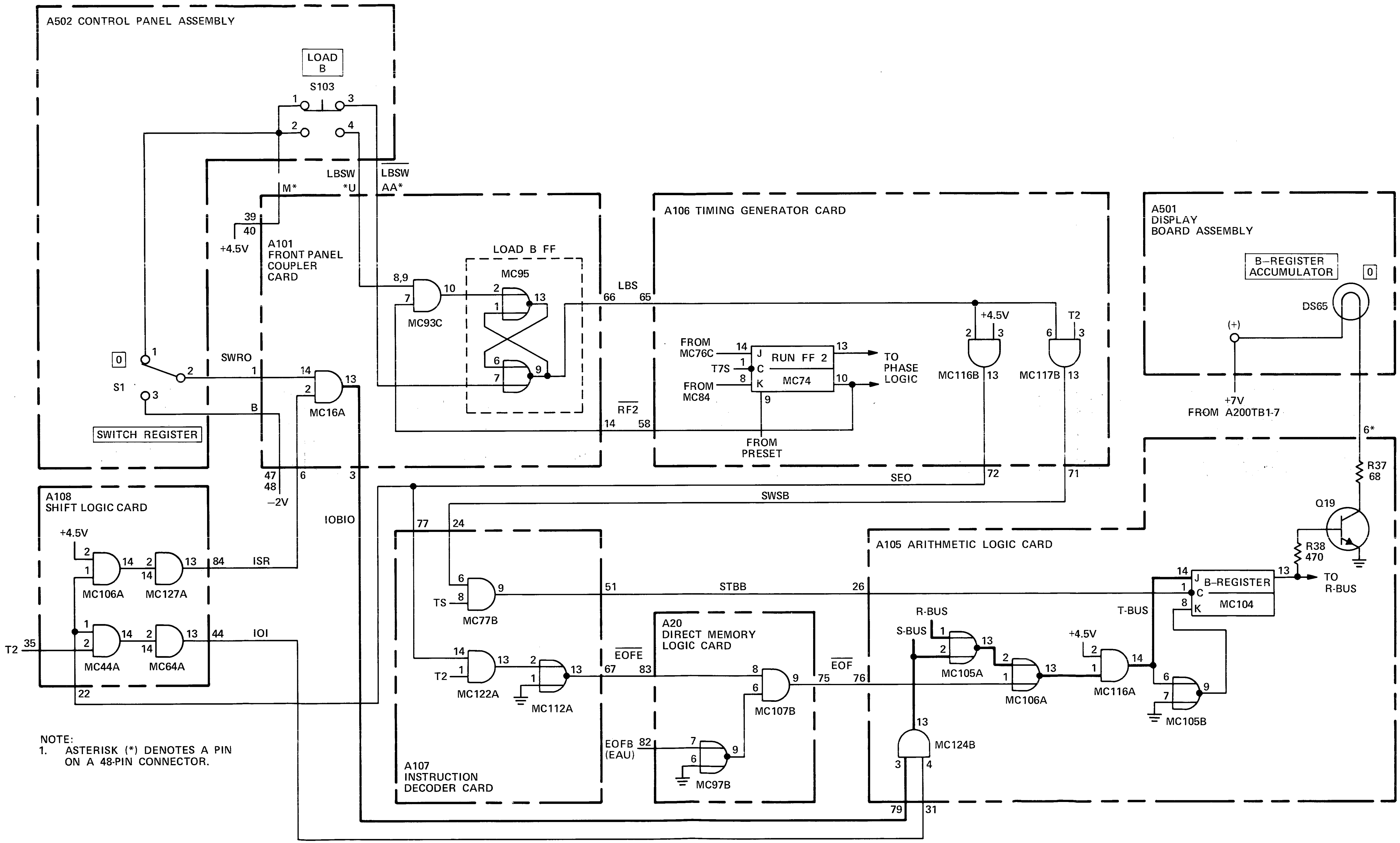


NOTE:
1. ASTERISK (*) DENOTES A PIN ON A 48-PIN CONNECTOR.

Figure 4-6. LOAD B Switch Circuit, Servicing Diagram

4-98. LOAD ADDRESS SWITCH, P- AND M-REGISTER INDICATORS, AND SWITCH REGISTER SWITCHES. The following paragraphs provide a description and trouble-shooting procedure for the circuits associated with LOAD switches located on control panel assembly A502, and the P- and M-register indicators located on display board assembly A501.

4-99. Description. The circuits associated with the LOAD ADDRESS switch are shown in figure 4-7. The timing diagram included in this figure shows the sequential events that occur when the LOAD ADDRESS switch is pressed and released. In the following description it is assumed that initially all flip-flops shown are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the LOAD ADDRESS switch are in the released position as shown.

4-100. The LOAD ADDRESS switch is a momentary-action type switch. When pressed, it places +4.5 volts through the switch and pin V of front panel coupler card A101 to pin 2 of "and" gate MC103A. The signal RF2 is transferred to pin 1 of MC103A from A106MC74-10 (RUN FF 2) on timing generator card A106. Therefore the machine must be in a halt mode for the LOAD ADDRESS switch to be effective. With a true signal at input pins 1 and 2 of MC103A output pin 14 will go true. This true signal is transferred to A101MC105-2 (LOAD ADDRESS FF) causing A101MC105-13 to go false. This false signal is felt at input pin 6 of MC105. Input pin 7 of MC105 is false due to open contacts 1 and 3 of the pressed LOAD ADDRESS switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signals LADS at pin 70 of front panel coupler card A101. As long as the LOAD ADDRESS switch is pressed, signal LADS remains true. As soon as the LOAD ADDRESS switch is released, +4.5 volts is transferred to A101MC105-7 which causes output pin 9 to go false.

4-101. The signal LADS is transferred through pin 70 of the front panel coupler card, and pin 68 of the timing generator card to pin 8 of "and" gate MC116D, pin 9 of "and" gate MC117C, pin 6 of "and" gate MC107B, and pin 7 of "and" gate MC106B. At time T2 the signal SWSM is generated by MC117C at output pin 10. This signal is transferred through pin 73 of the timing generator card and pin 26 of instruction decoder card A107 to pins 7 and 14 of "and" gates MC55B and MC66A respectively. At time T2 and TS the signals STM (0-15) are generated and transferred through pins 20, 21, 27, and 28 of the instruction decoder card. These signals are transferred from the instruction decoder card, through pins 22 and 29 of the arithmetic logic cards A102 through A105 to the clock input pin 1 of the M-register flip-flops and is used to clock the data on the T-bus into the M-register flip-flops.

4-102. Time T2 and signal LADS also causes the signal SWSP to be generated by MC107B at output pin 13. This signal is transferred through pin 64 of the timing generator card and pin 37 of the instruction decoder card to pins 8 and 8 of "and" gates MC34C and MC36B respectively. At time T2 and TS the signals STP (0-15) are generated and transferred through pins 7, 8, and 74 of the instruction decoder card. These signals are transferred from the instruction decoder card, through pins 23 and 44 of the arithmetic logic cards to the clock input pin 1 of the P-register flip-flops and is used to clock the data on the T-bus into the P-register flip-flops.

4-103. The signal LADS being applied to pin 7 of MC106B causes both RUN FF 1 (MC84) and RUN FF 2 (MC74) to be reset. It also causes the PH1 FF (MC44) to be set at the end (time T7S) of the first machine cycle after the LOAD ADDRESS switch is pressed.

4-104. As soon as the signal LADS is true at pin 8 of MC116D the signal SEO is generated at pin 10 of MC116D of the timing generator card. This signal is transferred through pin 72 of the timing generator card and pin 22 of the shift logic card A108 where it is used to generate the signal ISR, which enables the switch register gates on the front panel coupler card and transfers the switch register data to the IOBI lines. At time T2 the signal SEO also generates the signal IOI which is used to gate the data on the IOBI lines to the S-bus. The signal SEO is also transferred to pin 77 of the instruction decoder card where at time T2 it is used to generate the negative going signal $\overline{\text{EOFE}}$ at pin 13 of MC112A on the instruction decoder card. The signal $\overline{\text{EOFE}}$ is transferred through pin 67 of the instruction decoder card and pin 83 of the direct memory logic card A20 where it is used to generate the negative going signal $\overline{\text{EOF}}$ at pin 9 of "and" gate MC107B on the direct memory logic card. This signal is transferred through pin 75 of the direct memory logic card and pin 76 of the arithmetic logic cards. The signal $\overline{\text{EOF}}$ is used in the arithmetic logic cards to gate the data on the S-bus and R-bus onto the T-bus. (The R-bus is cleared to "zeros" at this time.) The T-bus data is then placed into the M- and P-register flip-flops by the clock signals STM (0-15) and STP (0-15) and each "1" bit will be indicated by a lighted M- and P-register indicator lamp. Thus the LOAD ADDRESS switch, when pressed, transfers the switch register data into the M- and P-registers and each switch that was in the up ("1") position will cause the corresponding M- and P-register indicator lamp to light.

4-105. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-7, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S102. If normal, proceed to step "c". If abnormal, check the connection between A502S102-1,2 and A101-39,40 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047) and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

e. At the computer front panel, press and release the POWER switch to turn on power.

f. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-68.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

g. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD ADDRESS switch and check the oscilloscope display of a 0-volt level. If the oscilloscope display is normal, proceed to step "h". If the oscilloscope display is abnormal, check A101MC105, A101MC103A, LOAD ADDRESS switch A502S102, and A106MC74 as the most probable cause of trouble.

h. Place the channel A oscilloscope probe on A106MC116-10.

i. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD ADDRESS switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "j". If the oscilloscope display is abnormal, check A106MC116-9 for a +4.5-volt level.

j. Place the channel A oscilloscope probe on A106MC44-13.

k. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD ADDRESS switch and check the oscilloscope display for a +4.5-volt level. If the oscilloscope display is normal, proceed to step "l". If the oscilloscope display is abnormal, check MC44, MC53, and MC106 as the most probable cause of trouble.

l. Place the channel A oscilloscope probe on A106MC106-2.

m. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD ADDRESS switch and check the oscilloscope display for a 0-volt level.

n. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC117-10.

(6) Channel B input: A106TP1 (time T0).

o. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, check A106MC117-7 for the 200 ηs pulse referred to above. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

p. Place the channel A oscilloscope probe on A106MC107-13.

q. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "r". If the oscilloscope display is abnormal, check A106MC107-3 for the 200 ηs pulse referred to above. If the display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

r. At the computer front panel, press and release the POWER switch to turn off power.

s. Using the extender card, extend shift logic card A108 from the card cage.

t. At the computer front panel, press and release the POWER switch to turn on power.

u. Place the channel A oscilloscope probe on pin 84 of the shift logic card.

v. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD ADDRESS switch and check the oscilloscope display for the 0-volt level. If the oscilloscope display is normal, proceed to step "w". If the oscilloscope display is abnormal, check MC106A and MC127A as the most probable cause of trouble.

w. Place the channel A oscilloscope probe on pin 44 of the shift logic card. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "x". If the oscilloscope display is abnormal, check MC44A and MC64A as the most probable cause of trouble.

x. At the computer front panel, press and release the POWER switch to turn off power.

y. Using the extender card, extend instruction decoder card A107 from the card cage.

z. At the computer front panel, press and release the POWER switch to turn on power.

aa. Place the channel A oscilloscope probe on pin 67 of the instruction decoder card. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "bb". If the oscilloscope display is abnormal, check MC112A and MC122A as the most probable cause of trouble.

bb. Place the channel A oscilloscope probe on pin 7 of the instruction decoder card. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. Place the oscilloscope probe on pins 8, 20, 21, 27, 28 and 74 of the instruction decoder card and check the oscilloscope for a 45 μs to 55 μs pulse occurring every 1.6 μs from each of these pins. If the oscilloscope displays are normal, proceed to step "cc". If any of the oscilloscope displays are abnormal, check MC34, MC36, MC55, MC56, and MC66 as the most probable cause of trouble.

cc. At the computer front panel, press and release the POWER switch to turn off power.

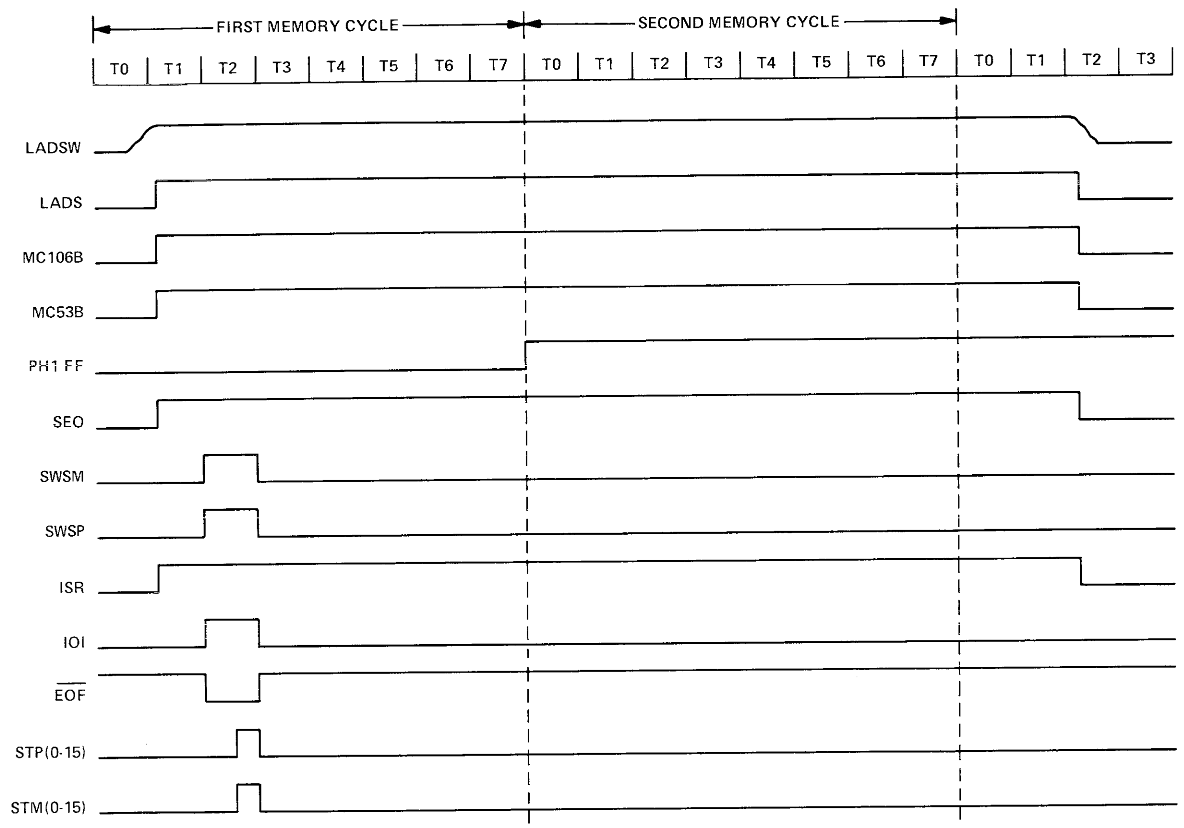
dd. Using the extender card, extend direct memory logic card A20 from the card cage.

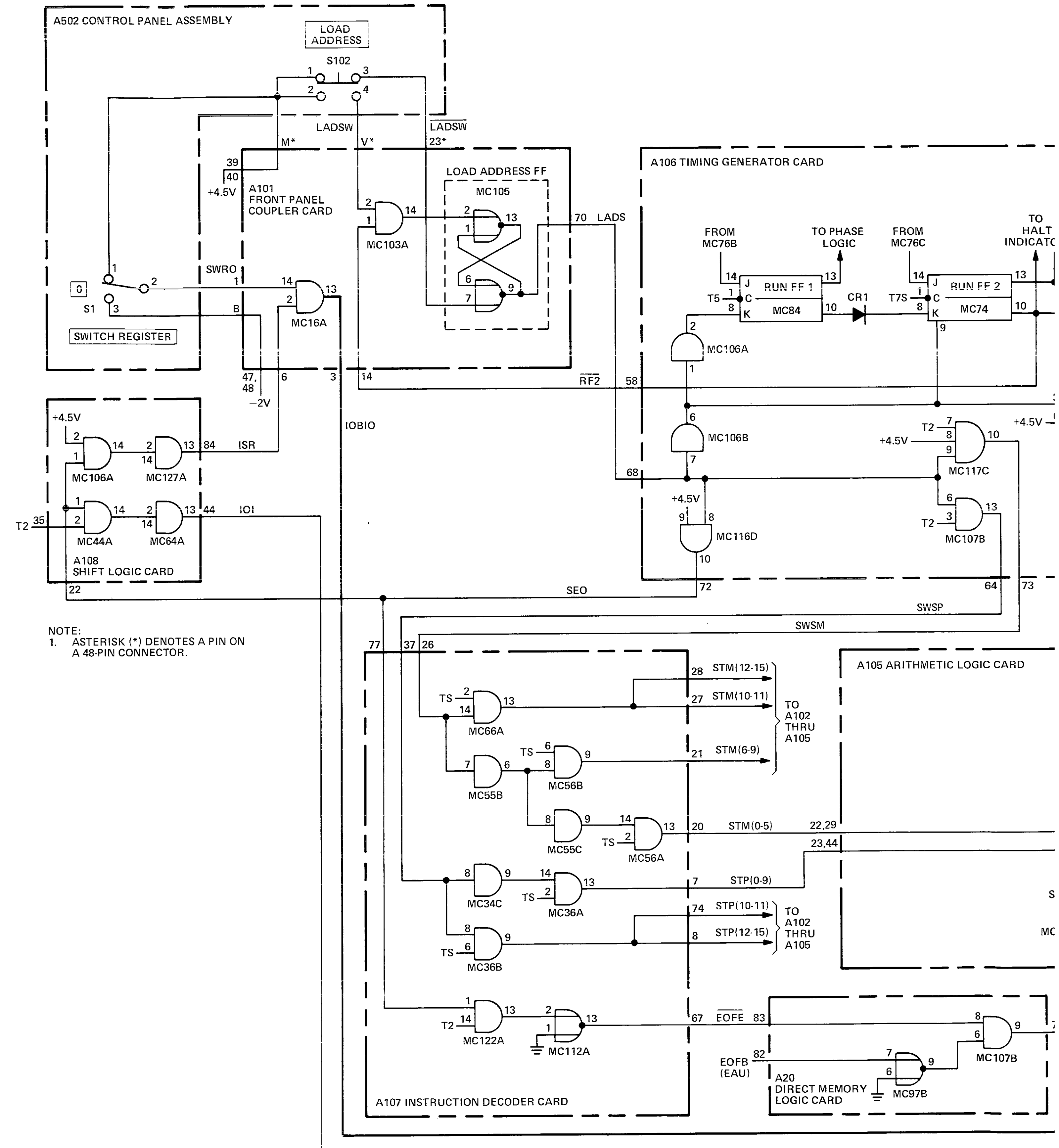
ee. At the computer front panel, press and release the POWER switch to turn on power.

ff. Place the channel A oscilloscope probe on pin 75 of the direct memory logic card and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "gg". If the oscilloscope display is abnormal, check MC97B and MC107B as the most probable cause of trouble.

gg. If, at this point in the test procedure, all checks have indicated normal operation but by pressing the LOAD ADDRESS switch the switch register data is not being properly transferred into the M- and P-registers and displayed by the M- and P-register indicator lamps, refer to figure 4-7 and check the arithmetic logic card A102 through A105 that controls the M- and P-register bit or bits in question. Also check the particular switch register switch or switches on control panel assembly A502 and the switch register gate or gates on front panel coupler card A101 for proper operation. Also check the cable connection from the arithmetic logic card, through the M- and P-register indicator lamp or lamps, to the +7-volt connection on display board assembly A501-(+) for continuity.

hh. If all indications of the above test procedure are normal, the LOAD ADDRESS switch and circuits are operating normally. If one or more indications of the above test procedure are abnormal, refer to the related test procedures, diagrams, and schematics and troubleshoot the related circuits.


FIRST MEMORY CYCLE
SECOND MEMORY CYCLE
T0 T1 T2 T3 T4 T5 T6 T7 T0 T1 T2 T3 T4 T5 T6 T7 T0 T1 T2 T3
LADSW
LADS
MC106B
MC53B
PH1 FF
SEO
SWSM
SWSP
ISR
IOI
EOF
STP(0-15)
STM(0-15)


A502 CONTROL PANEL ASSEMBLY
LOAD ADDRESS
S102
LADSW
SWITCH REGISTER
S1
A101 FRONT PANEL COUPLER CARD
LOAD ADDRESS FF
MC105
MC103A
MC16A
SWRO
IOBIO
LADS
A106 TIMING GENERATOR CARD
FROM MC76B
TO PHASE LOGIC
FROM MC76C
TO HALT INDICATOR
RUN FF 1
MC84
RUN FF 2
MC74
CR1
MC106A
MC106B
MC116D
MC117C
MC107B
A108 SHIFT LOGIC CARD
MC106A
MC127A
MC44A
MC64A
ISR
IOI
SEO
SWSP
SWSM
A107 INSTRUCTION DECODER CARD
MC66A
MC55B
MC56B
MC55C
MC56A
MC34C
MC36A
MC36B
MC122A
MC112A
STM(12-15)
STM(10-11)
STM(6-9)
STM(0-5)
STP(0-9)
STP(10-11)
STP(12-15)
TO A102 THRU A105
A105 ARITHMETIC LOGIC CARD
EOFE
EOFB (EAU)
A20 DIRECT MEMORY LOGIC CARD
MC97B
MC107B
NOTE:
1. ASTERISK (*) DENOTES A PIN ON A 48-PIN CONNECTOR.

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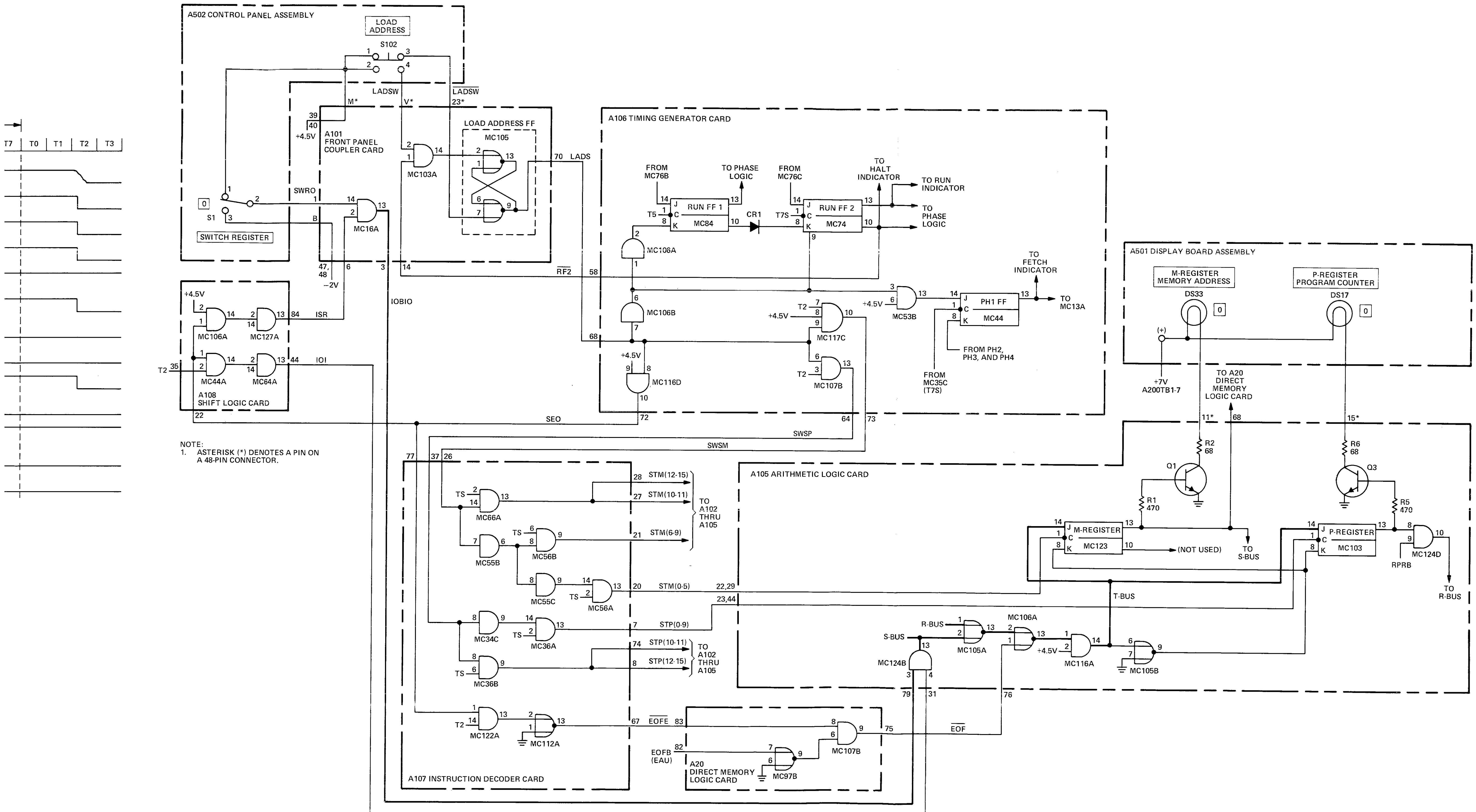

Figure 4-7. LOAD ADDRESS Switch Circuit, Servicing Diagram

4-106. LOAD MEMORY SWITCH, T-REGISTER INDICATORS, AND SWITCH REGISTER SWITCHES. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with LOAD MEMORY switch S105 and the SWITCH REGISTER switches located on control panel assembly A502, and the T-register indicators located on display board assembly A501.

4-107. Description. The circuits associated with the LOAD MEMORY switch are shown in figure 4-8. The timing diagram included in this figure shows the sequential events that occur when the LOAD MEMORY switch is pressed and released. In the following description it is assumed that initially all flip-flops shown on the timing generator card A106 are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the LOAD MEMORY switch are in the released position as shown.

4-108. The LOAD MEMORY switch is a momentary-action type switch. When pressed, it transfers +4.5 volts through the switch, and pin S of the front panel coupler card A101 to pin 2 of "and" gate MC93A. The signal $\overline{RF2}$ is transferred to A101MC93-1 from A106MC74-10 (RUN FF 2) on the timing generator card A106. Therefore, the computer must be in the halt mode for the switch to be effective. With a true signal at input pins 1 and 2 of MC93A output pin 14 will go true. This true signal is transferred to A101MC75-2 (LOAD MEMORY FF) causing A101MC75-13 to go false. This false signal is felt at A101MC75-6. Input pin 7 of MC75 is false due to open contacts 1 and 3 of the pressed LOAD MEMORY switch. Input pins 6 and 7 being false cause output pin 9 to go true and generator signal LMS at pin 58 of front panel coupler card A101. As long as the LOAD MEMORY switch is pressed, signal LMS remains true. As soon as the LOAD MEMORY switch is released, +4.5 volts it transferred to A101MC75-7 which causes output pin 9 to go false.

4-109. The signal LMS is transferred through pin 58 of the front panel coupler card, pin 46 of the timing generator card and through "and" gate MC86C to the set and reset pin 1 of STEP 1 FF MC94A. The first time T2 after the switch has been pressed STEP 1 FF will be set and will remain set until the first time T2 after the switch is released. The output pin 13 of STEP 1 FF is transferred to the set and reset input pin 7 of the STEP 2 FF MC94B which is set at the next time T1 and remains set until the time T1 after the switch is released. The output of STEP 1 FF is also felt at pin 9 of "and" gate MC76C. The output of STEP 2 FF is transferred to input pin 2 of "nor" gate MC87A causing its output pin 13 to go false. This false output is felt at input pin 7 of "and" gate MC76C causing its output pin 10 to go false. This action results in a 1.4 μs pulse being generated at the output pin 10 of MC76C. This pulse from pin 10 of MC76C is transferred to the phase logic pin 3 of MC33 B, and to the set input pin 14 of RUN FF 2 MC74 and at time T7S the output pin 13 of MC74 goes true causing the RUN indicator to go on for 1.6 μs and enabling "and" gate MC27A. The reset output pin 10 of MC74 goes false at the same time the set output goes true. This false output causes the HALT indicator to go out and the LOAD MEMORY switch gate MC93A on the front panel coupler card to be disabled thereby disabling the switch for 1.6 μs. The signal LMS is also transferred through "and" gate MC96C to input pin 6 of "and" gate MC33B causing the output pin 13 of MC33B to go true. This true output is transferred throughout the phase logic and causes all flip-flops to be reset except PH3 FF which it causes to be set at time T7 and TS. The signal LMS is also transferred to special logic which is used when attempting to load data into memory locations 000000 or 000001 (the A- or B-registers). The signal LMS is also transferred to the memory timing circuits where it is used to inhibit the signal MST thereby preventing the sense amplifier data being transferred into the T-register. It is also used to enable the signal MWL which will allow the new T-register data to be transferred into memory. The signal LMS is also transferred to input pins 7 and 2 of "and" gates MC116C and MC107A respectively where the signals SEO and SWST are generated at the output pins 10 and 14 respectively of the respective gates and pins 72 and 62 respectively of the timing generator card. The output pin 13 of PH3 FF is transferred to input pin 14 of "and" gate MC15A and through "and" gate MC25A to input pin 2 of "and" gate MC37A. The output of "and" gate MC27A which is generated by the set output pin 13 of RUN FF 2 is transferred to input pins 2 and 14 of MC15A and MC37A respectively and allow the signal PH3 to be generated at the output pin 13 of MC37A. The signals PH3 and P123 are transferred out of the timing generator card on pins 60 and 23 respectively. The signal P123 is transferred through "and" gate MC56B to the memory timing logic where it is used to enable the memory timing signal MTE which allows the necessary memory timing to be generated and the new data to be written into memory.

4-110. The signal SEO is transferred to pin 22 of the shift logic card A108 where it is used to generate the signal ISR which enables the switch register gates on the front panel coupler card transferring the switch register data onto the IOBI lines. It is also used in the shift logic card at time T2 to generate the signal IOI at pin 44 of the card. The signal IOI is transferred to pin 31 of the arithmetic logic cards A102 through A105 where it is used to gate the data on the IOBI lines onto the S-bus. The signal SEO is also transferred to pin 77 of the instruction decoder card where it is used at time T2 to generate the negative going signal $\overline{EOFE}$ at pin 67 of that card. The signal $\overline{EOFE}$ is transferred from pin 67 of the instruction decoder card to pin 83 of the direct memory logic card A20 where it is used to generate the negative going signal $\overline{EOF}$ at pin 75 of that card. The signal $\overline{EOF}$ is transferred to pin 76 of the arithmetic logic cards where it is used to transfer the R- and S-bus data onto the T-bus at time T2.

4-111. At time T0 the signal P123 causes the signal RST to be generated at pin 58 of the instruction decoder card. This signal is transferred to pin 7 of the arithmetic logic cards where it is used as a direct reset signal for all T-register flip-flops.

4-112. At time T2 the signal SWST was generated in the timing generator card. At time T2 and TS the signal SWST causes the signal STBT to be generated at pin 63 of the instruction decoder card. The signal STBT is transferred to pin 51 of the arithmetic logic cards where it is used to clock the T-bus data into the T-register flip-flops. Each "1" bit being indicated by a lighted T-register indicator lamp on the door assembly.

4-113. At time T6T7 the signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) are generated within the instruction decoder card. These signals are transferred to the arithmetic logic cards where they are used to transfer the P-register data to the R-bus, set bit zero of the S-bus to a "1", add the R- and S-bus data together and transfer this combined data (P-register plus one) to the T-bus, and store the T-bus data into the P- and M-register flip-flops. This new P- and M-register data being indicated by the P- and M-register indicator lamps on the door assembly.

4-114. Thus by pressing the LOAD MEMORY switch the data toggled into the switch register is transferred via the T-register into the memory location addressed by the M-register and the P- and M-registers are incremented by one.

4-115. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-8, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S105. If normal, proceed to step "c". If abnormal, check the connection between A502S105-1,2 and A101-39,40 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047) and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: channel B.

(3) Time/cm: 0.2 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1

(5) Channel A input: A106-46.

(6) Channel B input: A106TP1 (Time T0).

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

f. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD MEMORY switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check A101MC75, A101MC93A, LOAD MEMORY switch A502S105, and A106MC74 as the most probable cause of trouble.

g. Place the channel A oscilloscope probe on A106MC116-10.

h. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD MEMORY switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A106MC116 as the most probable cause of trouble.

i. Place the channel A oscilloscope probe on A106-MC86-9.

j. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD MEMORY switch and check the oscilloscope display for a 0-volt level.

k. At the oscilloscope, make the following settings and and connections:

(1) Time/cm: 1.0 μs

(2) Channel A input: A106MC107-14.

l.. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "o". If the oscilloscope display is abnormal, check A106MC107-1 for the 200 ηs pulse referred to above. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

m. At the oscilloscope, make the following settings and connections:

(1) Time/cm: 2ms.

(2) Channel A input: A106MC24-13.

n. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 1.4 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "o". If the oscilloscope display is abnormal, check A106MC24, A106MC33, A106MC76, A106MC87, A106-MC94, and A106MC96 as the most probable cause of trouble.

o. Place the channel A oscilloscope probe on pin 60 of the timing generator card.

p. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check A106MC15-2 for a 1.6 μs pulse every time the switch is pressed. If this display is abnormal, check A106MC27 as the most probable cause of trouble.

q. Place the channel A oscilloscope probe on pin 23 of the timing generator card.

r. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "s". If the oscilloscope display is abnormal, check A106MC37, and A106MC25 as the most probable cause of trouble.

s. Place the channel A oscilloscope probe on A106MC56-6.

t. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "u". If the oscilloscope display is abnormal, the most probable cause of trouble is A106MC56.

u. At the computer front panel, press and release the POWER switch to turn off power.

v. Using the extender card, extend shift logic card A108 from the card cage.

w. At the computer front panel, press and release the POWER switch to turn on power.

x. Place the channel A oscilloscope probe on pin 84 of the shift logic card and adjust time/cm to 1.0 μs.

y. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a +4.5-volt level. Then release the LOAD MEMORY switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "z". If the oscilloscope display is abnormal, check A108MC106 and A108MC127 as the most probable cause of trouble.

z. Place the channel A oscilloscope probe on pin 44 of the shift logic card. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "aa". If the oscilloscope display is abnormal, check A108MC44 and A108MC64 as the most probable cause of trouble.

aa. At the computer front panel, press and release the POWER switch to turn off power.

bb. Using the extender card, extend instruction decoder card A107 from the card cage.

cc. At the computer front panel, press and release the POWER switch to turn on power.

dd. Place the channel A oscilloscope probe on pin 63 of the instruction decoder card.

ee. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "ff". If the oscilloscope display is abnormal, check A107MC92 as the most probable cause of trouble.

ff. Place the channel A oscilloscope probe on pin 67 of the instruction decoder card.

gg. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "hh". If the oscilloscope display is abnormal, check A107MC112 and A107MC122 as the most probable cause of trouble.

hh. At the oscilloscope, make the following settings and connections:

(1) Channel B volts/cm: 0.1 (if using 10:1 probe).

(2) Channel B input: A107-72.

ii. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "jj". If the oscilloscope display is abnormal, check A107MC106, A107MC107, and A107MC126 as the most probable cause of trouble.

jj. Place the oscilloscope probe on pin 81 of the instruction decoder card.

kk. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "ll". If the oscilloscope display is abnormal, check A107MC116, A107MC97, A107MC96, and A107MC106 as the most probable cause of trouble. Also check that the INSTRUCTION switch on the display board assembly A501 is in the NORM position.

ll. Place the channel A oscilloscope probe on pin 75 of the instruction decoder card.

mm. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the display is normal, proceed to step "nn". If the display is abnormal, check A107MC107 and A107MC-127 as the most probable cause of trouble.

nn. Place the channel B oscilloscope probe on pin 58 of the instruction decoder card.

oo. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "pp". If the oscilloscope display is abnormal, check A107MC114 and A107MC125 as the most probable cause of trouble.

pp. Place the channel A oscilloscope probe on pin 7 of the instruction decoder card.

qq. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse every time the switch is pressed. Place the oscilloscope probe on pins 8, 20, 21, 27, 28, and 74 of the instruction decoder card and check the oscilloscope display for a 45 ηs to 55 ηs pulse from each of these pins every time the switch is pressed. If the oscilloscope displays are normal, proceed to step "rr". If any of the oscilloscope displays are abnormal, check A107MC34, A107MC35, A107MC36, A107MC53, A107-MC55, A107MC56, A107MC63 and A107MC66 as the most probable cause of trouble.

rr. At the computer front panel, press and release the POWER switch to turn off power.

ss. Using the extender card, extend direct memory logic card A20 from the card cage.

tt. At the computer front panel, press and release the POWER switch to turn on power.

uu. Place the channel B oscilloscope probe on pin 75 of the direct memory logic card.

vv. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "ww". If the oscilloscope display is abnormal, check A20MC97 and A20MC107 as the most probable cause of trouble.

ww. If, at this point in the test procedure, all checks have indicated normal operation but by pressing the LOAD MEMORY switch the switch register data is not being properly transferred into the addressed memory location and the P- and M-registers are not being properly incremented, refer to figure 4-8 and check the arithmetic logic card A102 through A105 that controls the bit or bits in question. Also check the particular switch register switch or switches on control panel assembly A502 and the switch register gate or gates on front panel coupler card A101 for proper operation. Also check the cable connection from the arithmetic logic card, through the M- and P-register indicator lamp or lamps, to the +7-volt connection on display board assembly A501-(+) for continuity.

xx. If all indications of the above test procedure are normal, the LOAD MEMORY switch and circuits are operating normally.

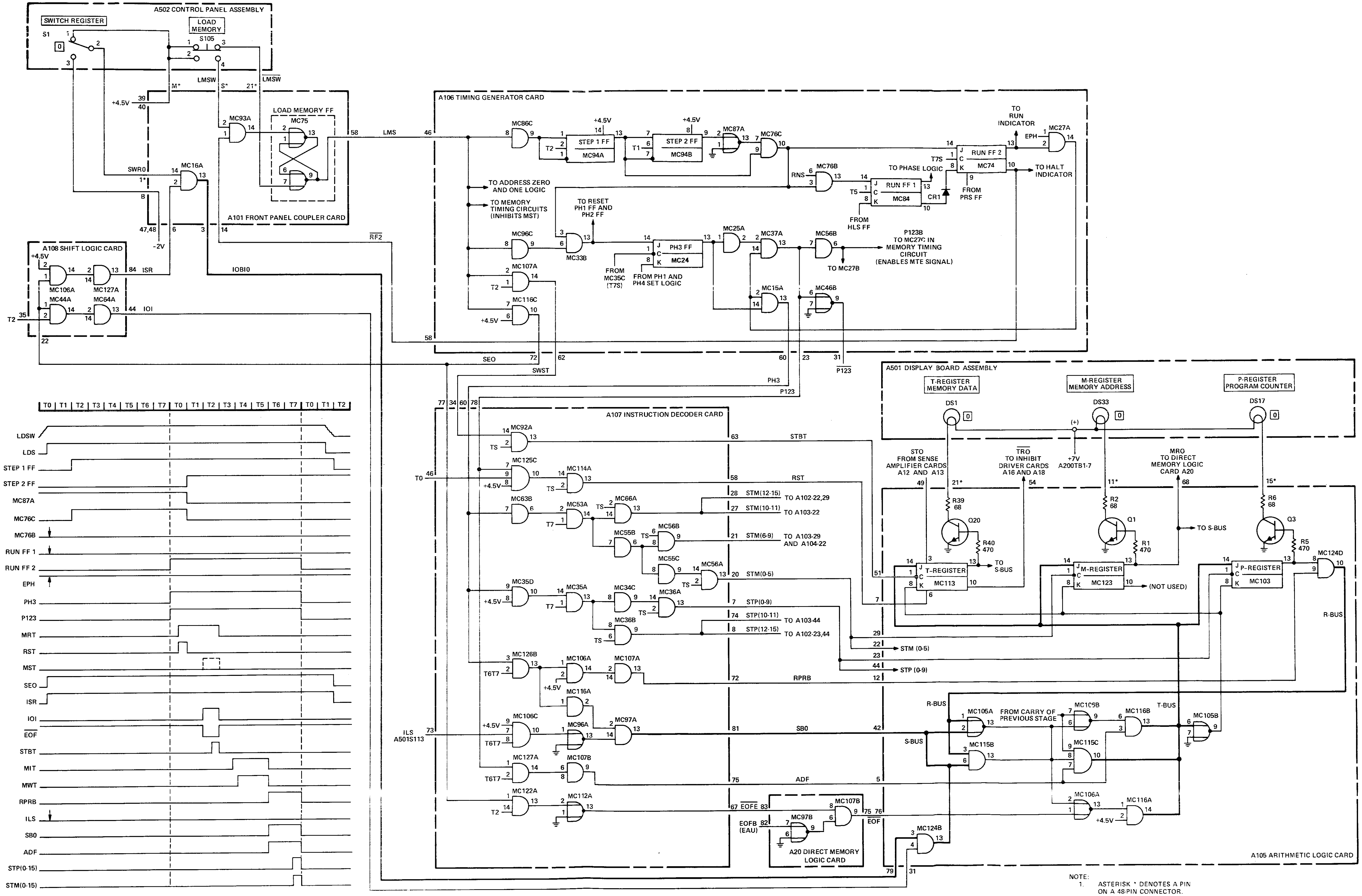

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Figure 4-8. LOAD MEMORY Switch Circuit, Servicing Diagram

4-116. DISPLAY MEMORY SWITCH AND T-, P-, AND M-REGISTER INDICATORS. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with DISPLAY MEMORY switch S101 located on control panel assembly A502, and the T-, P-, and M-register indicators located on display board assembly A501.

4-117. Description. The circuits associated with the DISPLAY MEMORY switch are shown in figure 4-9. The timing diagram included in this figure shows the sequential events that occur when the DISPLAY MEMORY switch is pressed and released. In the following description it is assumed that initially all flip-flops shown on the timing generator card A106 are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the DISPLAY MEMORY switch are in the released position as shown.

4-118. The DISPLAY MEMORY switch is a momentary-action type switch. When pressed, it transfers +4.5 volts through the switch, and pin W of the front panel coupler card A101 to pin 3 of "and" gate MC103B. The signal $\overline{RF2}$ is transferred to A101MC103-6 from A106MC74-10 (RUN FF 2) on the timing generator card A106. Therefore, the computer must be in the halt mode for the switch to be effective. With a true signal at input pins 3 and 6 of MC103B output pin 13 will go true. This true signal is transferred to A101MC115-2 (DISPLAY MEMORY FF) causing output pin 13 to go false. This false signal is felt at input pin 6 of MC115. Input pin 7 of MC115 is false due to open contacts 1 and 3 of the pressed DISPLAY MEMORY switch. Input pins 6 and 7 of MC115 being false cause output pin 9 to go true and generate signal DMS at pin 74 of front panel coupler card A101. As long as the DISPLAY MEMORY switch is pressed, signal DMS remains true. As soon as the DISPLAY MEMORY switch is released, +4.5 volts is transferred to input pin 7 of MC115 which causes output pin 9 to go false.

4-119. The signal DMS is transferred through pin 74 of the front panel coupler card, pin 59 of the timing generator card, through "and" gate MC86B to the set and reset pin 1 of STEP 1 FF MC94A. The first time T2 after the switch has been pressed STEP 1 FF will be set and will remain set until the first time T2 after the switch is released. The output pin 13 of STEP 1 FF is transferred to A106MC94-7 (STEP 2 FF) which becomes set at the next time T1 and remains set until the time T1 after the switch is released. The output of STEP 1 FF is also felt at pin 9 of "and" gate MC76C. The output of STEP 2 FF is transferred to input pin 2 of "nor" gate MC87A causing its output pin 13 to go false. This false output is felt at input pin 7 of "and" gate MC76C causing its output pin 10 to go false. This action results in a 1.4 μs pulse being generated at the output pin 10 of MC76C. This pulse from pin 10 of MC76C is transferred to pin 3 of "and" gate MC33B of the phase logic, and to the set input pin 14 of RUN FF 2 MC74 and at time T7S the output pin 13 of MC74 goes true causing the RUN indicator to go on for 1.6 μs and enabling "and" gate MC27A. The reset output pin 10 of MC74 goes false at the same time the set output goes true. This false output causes the HALT indicator to go out and the DISPLAY MEMORY switch gate MC103B on the front panel coupler card to be disabled thereby disabling the switch for 1.6 μs. The signal DMS is also transferred through "and" gate MC96D to input pin 6 of "and" gate MC33B causing the output pin 13 of MC33B to go true when input pin 3 is also true. This true output is transferred throughout the phase logic and causes all flip-flops to be reset except PH3 FF which it causes to be set at time T7S. The output at pin 13 of PH3 FF is transferred to input pin 14 of "and" gate MC15A and through "and" gate MC25A to input pin 2 of "and" gate MC37A. The output of "and" gate MC27A which is generated by the set output pin 13 of RUN FF 2 is transferred to input pins 2 and 14 of MC15A and MC37A respectively and allow the signals P123 and PH3 to be generated at the output pin 13 of MC37A and pin 13 of MC15A respectively. The signals PH3 and P123 are transferred out of the timing generator card on pins 60 and 23 respectively. The signal P123 is transferred through "and" gate MC56B to the memory timing logic where it is used to enable the memory timing signal MTE which allows the necessary memory timing to be generated and the memory data to be read into the sense amplifiers and thence into the T-register during time T2.

4-120. At time T0 the signal P123 causes the signal RST to be generated at pin 58 of the instruction decoder card. This signal is transferred to pin 7 of the arithmetic logic cards where it is used as a direct reset signal for all T-register flip-flops.

4-121. At time T6T7 the signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) are generated within the instruction decoder card. These signals are transferred to the arithmetic logic cards where they are used to transfer the P-register data to the R-bus, set bit zero of the S-bus to a "1", add the R- and S-bus data together and transfer this combined data (P-register plus one) to the T-bus, and store the T-bus data into the P- and M-register flip-flops. This new P- and M-register data being indicated by the P- and M-register indicator lamps on the door assembly.

4-122. Thus by pressing the DISPLAY MEMORY switch the data within the addressed memory location is transferred into the T-register and the P- and M-registers are incremented by one.

4-123. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-9, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S101. If normal, proceed to step "c". If abnormal, check the connection between A502S101-1,2 and A101-39,40 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047) and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 1.0 μs.

(4) Channel B volts/cm: 0.1 (if using 10:1 probe).

(5) Channel B input: A106-59.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

f. At the computer front panel, press and hold the DISPLAY MEMORY switch and check the oscilloscope display for a +4.5-volt level. Then release the DISPLAY MEMORY switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check A101MC115, A101MC103B, DISPLAY MEMORY switch A502S101, and A106MC74 as the most probable cause of trouble.

g. Place the channel B oscilloscope probe on A106MC96-13.

h. At the computer front panel, press and hold the DISPLAY MEMORY switch and check the oscilloscope display for a +4.5-volt level. Then release the DISPLAY MEMORY switch and check the oscilloscope display for a 0-volt level.

i. Place the channel B oscilloscope probe on pin 13 of MC24.

j. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, check A106MC24, and A106MC33 as the most probable cause of trouble.

k. Place the channel B oscilloscope probe on A106MC86-6

l. At the computer front panel, press and hold the DISPLAY MEMORY switch and check the oscilloscope display for a +4.5-volt level. Then release the DISPLAY MEMORY switch and check the oscilloscope display for a 0-volt level.

m. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel B volts/cm: 0.1 (if using 10:1 probe).

(5) Channel B input: A106MC76-10.

(6) Channel B input: A106TP1 (time T0).

n. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.4 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "o". If the oscilloscope display is abnormal, check A106MC94, and A106MC87 as the most probable cause of trouble.

o. Place the channel B oscilloscope probe on pin 60 of the timing generator card.

p. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope is abnormal, check A106MC15-2 for a 1.6 μs pulse every time the switch is pressed. If this display is abnormal, check A106MC27 as the most probable cause of trouble.

q. Place the channel B oscilloscope probe on pin 23 of the timing generator card.

r. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "s". If the oscilloscope display is abnormal, check A106MC37, and A106MC25 as the most probable cause of trouble.

s. Place the channel B oscilloscope probe on A106MC56-6.

t. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed.

u. At the computer front panel, press and release the POWER switch to turn off power.

v. Using the extender card, extend instruction decoder card A107 from the card cage.

w. At the computer front panel, press and release the POWER switch to turn on power.

x. Place the channel B oscilloscope probe on pin 58 of the instruction decoder card.

y. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "z". If the oscilloscope display is abnormal, check A107MC114 and A107MC125 as the most probable cause of trouble.

z. Place the channel B oscilloscope probe on pin 72 of the instruction decoder card.

aa. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "bb". If the oscilloscope display is abnormal, check A107MC106, A107MC107, and A107MC126 as the most probable cause of trouble.

bb. Place the channel B oscilloscope probe on pin 81 of the instruction decoder card.

cc. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "dd". If the oscilloscope display is abnormal, check A107MC116, A107MC97, A107MC96, and A107MC106 as the most probable cause of trouble. Also check that the INSTRUCTION switch on the display board assembly A501 is in the NORM position.

dd. Place the channel B oscilloscope probe on pin 75 of the instruction decoder card.

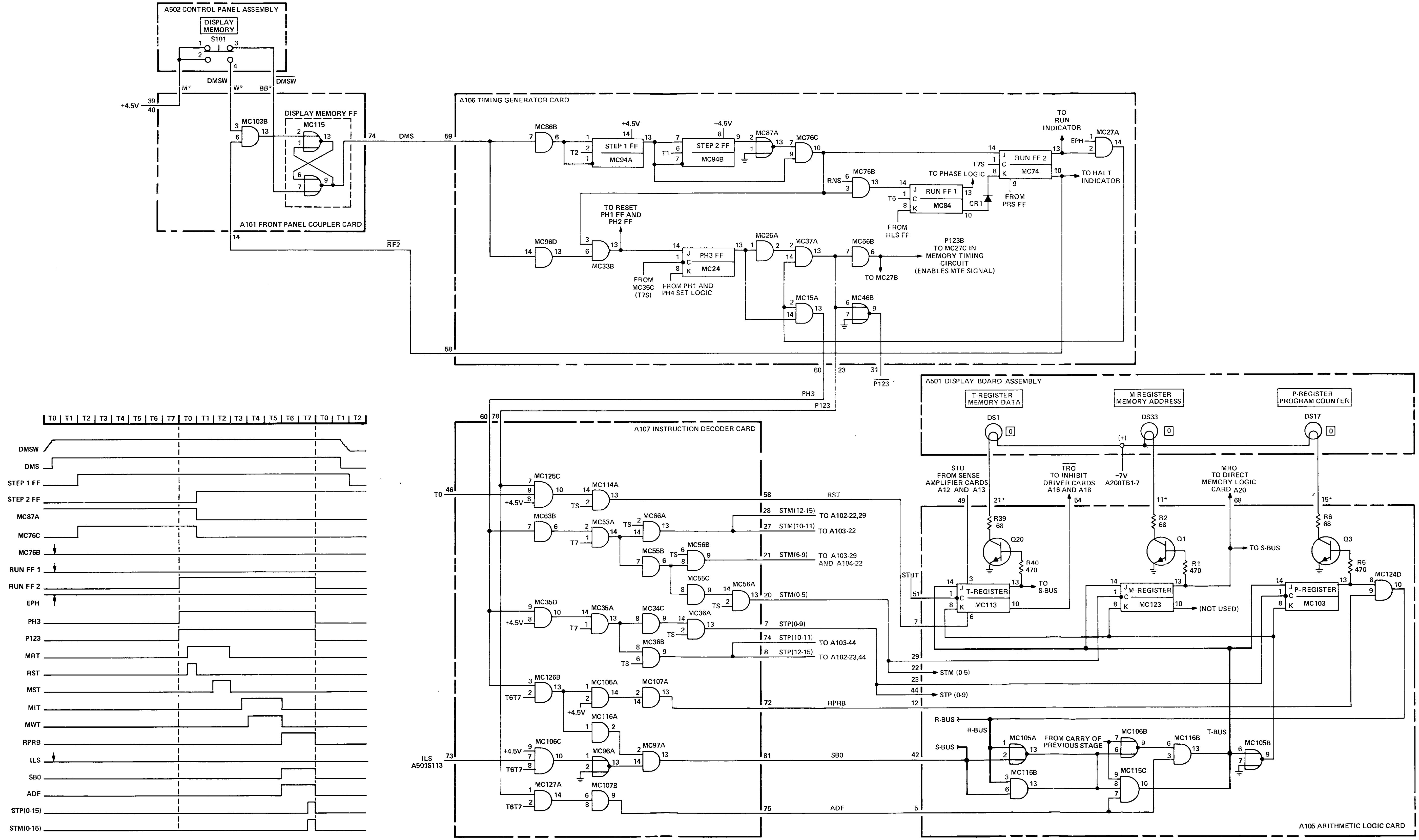
ee. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the display is normal, proceed to step "ff". If the display is abnormal, check A107MC107 and A107MC127 as the most probable cause of trouble.

ff. Place the channel B oscilloscope probe on pin 7 of the instruction decoder card.

gg. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse every time the switch is pressed. Place the oscilloscope probe on pins 8, 20, 21, 27, 28, and 74 of the instruction decoder card and check the oscilloscope display for a 45 ηs to 55 ηs pulse from each of these pins every time the switch is pressed. If the oscilloscope displays are normal, proceed to step "hh". If any of the oscilloscope displays are abnormal, check A107MC34, A107MC36, A107MC55, A107MC56, and A107MC66 as the most probable cause of trouble.

hh. If, at this point in the test procedure, all checks have indicated normal operation but by pressing the DISPLAY MEMORY switch the memory data is not being properly transferred into the T-register or the P- and M-registers are not being properly incremented, refer to figure 4-9 and check the arithmetic logic card A102 through A105 that controls the bit or bits in question. Also check the cable connection from the arithmetic logic card, through the T-, M-, and P-register indicator lamp or lamps, to the +7-volt connection on display board assembly A501-(+) for continuity.

ii. If all indications of the above test procedure are normal, the DISPLAY MEMORY switch and circuits are operating normally.



NOTES:

1. ASTERISK * DENOTES A PIN ON A 48-PIN CONNECTOR.

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Figure 4-9. DISPLAY MEMORY Switch Circuit, Servicing Diagram

4-124. SINGLE CYCLE SWITCH AND P- AND M-REGISTER INDICATORS. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with SINGLE CYCLE switch S100 located on control panel assembly A502 and the P- and M-register indicators located on display board assembly A501.

4-125. Description. The circuits associated with the SINGLE CYCLE switch are shown in figure 4-10. A timing diagram showing the sequential events events that occur when the SINGLE CYCLE switch is pressed is given in figure 4-10. In the following description it is assumed that initially all flip-flops shown on the timing generator card A106 are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the SINGLE CYCLE switch are in the released position as shown.

4-126. The SINGLE CYCLE switch is a momentary-action type switch. When pressed, it transfers +4.5 volts through the switch, and pin X of the front panel coupler card A101 to pin 7 of "and" gate MC103C. The signal $\overline{RF2}$ is transferred to pins 8 and 9 of MC103C from A106MC74-10 (RUN FF 2) on the timing generator card A106. Therefore, the computer must be in the halt mode for the switch to be effective. With a true signal at input pins 7, 8, and 9 of MC103 output pin 10 will go true. This true signal is transferred to A101MC125-2 (SINGLE CYCLE FF) causing output pin 13 to go false. This false signal is felt at input pin 6. Input pin 7 of MC125 is false due to open contacts 1 and 3 of the pressed SINGLE CYCLE switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signal SCS at pin 78 of front panel coupler card A101. As long as the SINGLE CYCLE switch is pressed, signal SCS remains true. As soon as the SINGLE CYCLE switch is released, +4.5 volts is transferred to input pin 7 of MC125 which causes output pin 9 to go false.

4-127. The signal SCS is transferred through pin 78 of the front panel coupler card, pin 56 of the timing generator card, through "and" gate MC86, to A106MC94-1 (STEP 1 FF). The first time T2 after the switch has been pressed STEP 1 FF will be set and will remain set until the first time T2 after the switch is released. The output pin 13 of STEP 1 FF is transferred to A106MC94-7 (STEP 2 FF) which is set at the next time T1 and remains set until the time T1 after the switch is released. The output of STEP 1 FF is also felt at pin 9 of "and" gate MC76C. The output of STEP 2 FF is transferred to input pin 2 of "nor" gate MC87A causing its output pin 13 to go false. This false output is felt at input pin 7 of "and" gate MC76C causing its output pin 10 to go false. This action results in a 1.4 μs pulse being generated at the output pin 10 of MC76C. This pulse from pin 10 of MC76C is transferred to the phase logic and to A106MC74-14 (RUN FF 2) MC74 and at time T7S the output pin 13 of MC74 goes true causing the RUN indicator to go on for 1.6 μs and enabling "and" gate MC27A. The reset output pin 10 of MC74 goes false at the same time the set output goes true. This false output causes the HALT indicator to go out for 1.6 μs and the SINGLE CYCLE SWITCH GATE MC103C on the front panel coupler card to be disabled thereby disabling the switch for 1.6 μs.

4-128. The output from pin 14 of MC27 is transferred to the phase logic and allows the currently active phase flip-flops output to be transferred throughout the computer for 1.6 μs (one machine cycle).

4-129. Thus the SINGLE CYCLE switch, when pressed, allows the currently active phase to be operated for only one machine cycle.

4-130. Test procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-10, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S100. If normal, proceed to step "c". If abnormal, check the connection between A502S100-1,2 and A101-39,40 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047) and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 1.0

(4) Channel B volts/cm: 0.1 (if using 10:1 probe).

(5) Channel B input: A106-56.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the trouble-shooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

f. At the computer front panel, press and hold the SINGLE CYCLE switch and check the oscilloscope display for a +4.5-volt level. Then release the SINGLE CYCLE switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check A101MC125, A101MC103C, SINGLE CYCLE switch A502S100, and A106MC74 as the most probable cause of trouble.

g. Place the channel B oscilloscope probe on A106MC86-2.

h. At the computer front panel, press and hold the SINGLE CYCLE switch and check the oscilloscope display for a +4.5-volt level. Then release the SINGLE CYCLE switch and check the oscilloscope display for a 0-volt level.

i. Place the channel B oscilloscope probe on A106MC76-10, and set triggering source to channel B.

j. At the computer front panel, repeatedly press and release the SINGLE CYCLE switch and check the oscilloscope display for a 1.4 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, check A106MC94, and A106MC87 as the most probable cause of trouble.

k. Place the channel B oscilloscope probe on A106MC74-13.

l. At the computer front panel, repeatedly press and release the SINGLE CYCLE switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "m". If the oscilloscope display is abnormal, check A106MC74-1 for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

m. Place the channel B oscilloscope probe on A106MC27-14.

n. At the computer front panel, repeatedly press and release the SINGLE CYCLE switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed.

o. If all indications of the above test procedure are normal, the SINGLE CYCLE switch and circuits are operating normally.

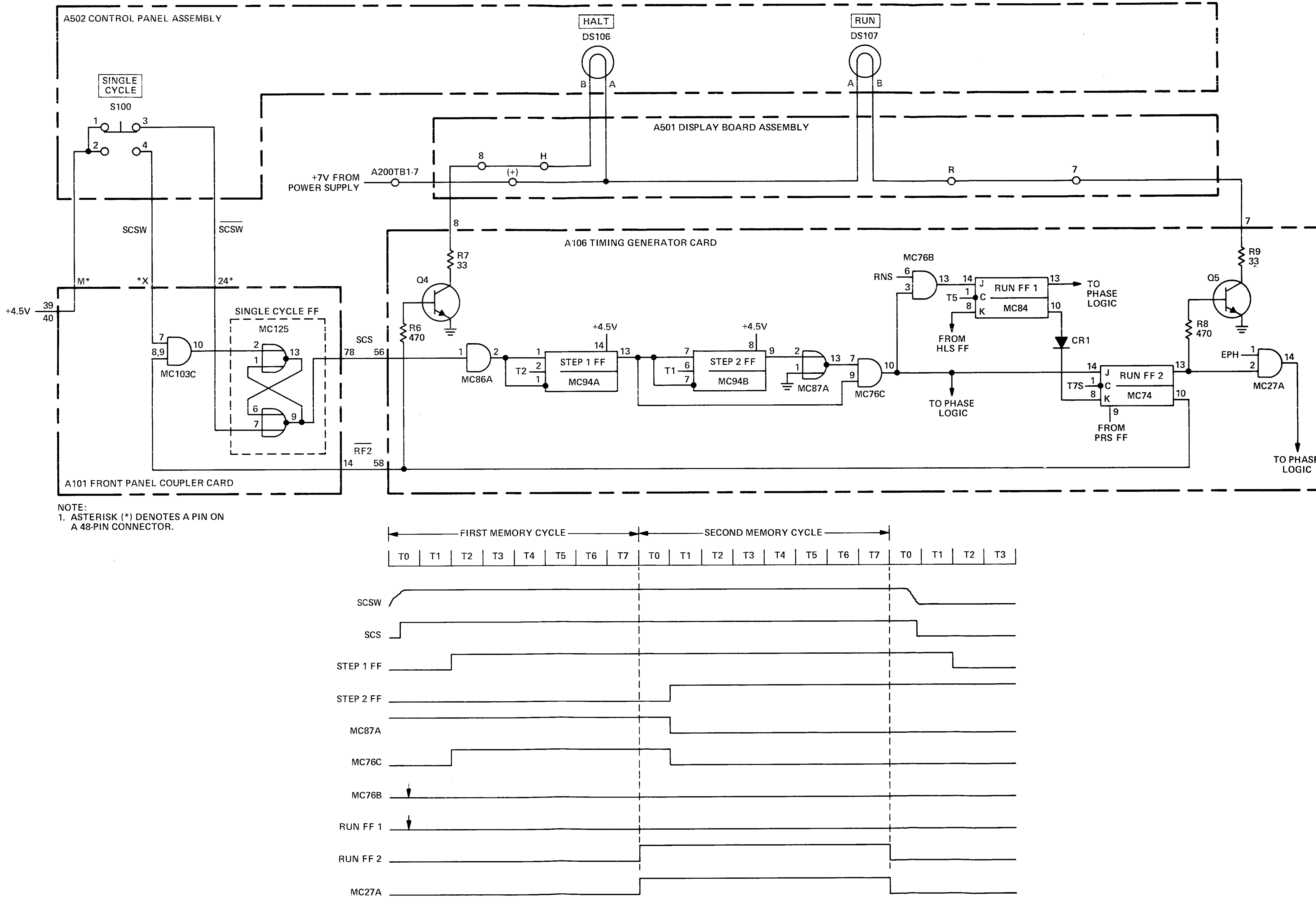

Figure 4-10. SINGLE CYCLE Switch Circuit, Servicing Diagram

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4-131. LOADER SWITCH. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with the LOADER switch S110 which is located on the control panel assembly A502.

4-132. Description. The circuits associated with the LOADER switch are shown in figure 4-11. In the following description it is assumed that the LOADER switch is in the PROTECTED position as shown.

4-133. The LOADER switch is a toggle type switch. When placed in the PROTECTED position, it transfers +4.5 volts through the switch, and pin Y of the front panel coupler card A101 as signal LPS. Signal LPS is transferred from pin 82 of the front panel coupler card through the backplane wiring to pin 49 of memory module decoder card A2 and through resistor R10 of that card to pin 12 of "and" gate MC77. The other input pins of MC77 are tied to memory address decoding signals which decode the uppermost 64 locations of memory. When one of these 64 locations is addressed and the signal LPS is true at pin 12 the output signal $\overline{\text{MPT}}$ at pin 8 of MC77 will go false. The signal $\overline{\text{MPT}}$ is transferred through pin 78 of the memory module decoder card, and pin 12 of timing generator card A106, to pin 7 of "and" gate MC27C. When the signal $\overline{\text{MPT}}$ goes false it disables MC27C and causes its output signal MTE at pin 10 to go false. The signal MTE going false disables all memory timing signals and thus will not allow data to be transferred into or out of memory.

4-134. Thus when the LOADER switch is in the PROTECTED position, data cannot be transferred into or out of the uppermost 64 locations of memory.

4-135. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-11, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pin 3 of A502S110. If normal, proceed to step "c". If abnormal, check the connection between A502S110-3 and A101-39,40 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047), extend memory module decoder card A2 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A2-49.

f. At the computer front panel, assure that the LOADER switch is in the PORTECTED position and check the oscilloscope display for a +4.5-volt level. Then place the LOADER switch in the ENABLED position and check the oscilloscope for a 0-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check the connection from A2-49 to A502S110-2 for continuity and check the LOADER switch for proper wiring and operation.

g. Place the channel A oscilloscope probe on pin 78 of the memory module decoder card.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can

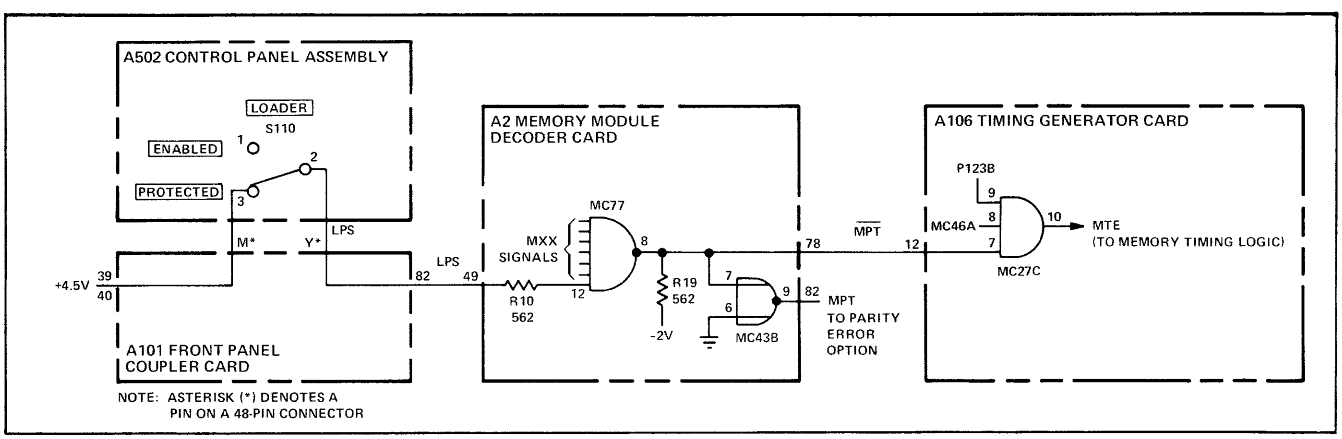

Figure 4-11. LOADER Switch Circuit, Servicing Diagram

vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

h. At the computer front panel, assure that the LOADER switch is in the PROTECTED position and that the M-register is not addressing any of the uppermost 64 locations of memory. Then check the oscilloscope display for a +4.5-volt level.

i. Address any of the uppermost 64 locations of memory by placing the address (ex. 177770) in the switch register and pressing the LOAD ADDRESS switch. Check the oscilloscope display for a 0-volt level.

j. If the oscilloscope display for step "h" is abnormal, check A2MC77 as the most probable cause of trouble. If the oscilloscope display for step "i" is abnormal, refer to paragraphs 4-458 and 4-474 and troubleshoot the memory module decoder card.

k. At the computer front panel, press and release the POWER switch to turn off power.

l. Using the extender card and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

m. At the computer front panel, press and release the POWER switch to turn on power.

n. Place the channel A oscilloscope probe on A106MC27-10.

o. At the computer front panel, assure that the LOADER switch is in the PROTECTED position and that the M-register is addressing any of the uppermost 64 locations of memory. Then check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "p". If the oscilloscope display is abnormal, check A106MC27 as the most probable cause of trouble and refer to paragraph 4-136 and troubleshoot the MEMORY switch circuits.

p. At the computer front panel, assure that the LOADER switch is in the PROTECTED position. Address any of the lower locations of memory by placing the address in the switch register and pressing the LOAD ADDRESS switch. Then check the oscilloscope display for a +4.5-volt level. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check A106MC27 as the most probable cause of trouble and refer to paragraph 4-136 and troubleshoot the MEMORY switch circuits.

q. If all indications of the above test procedure are normal, the LOADER switch and circuits are operating normally.

4-136. MEMORY SWITCH. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with the MEMORY switch S111 located on display board assembly A501.

4-137. Description. The circuits associated with the MEMORY switch are shown in figure 4-12. In the following description it is assumed that the MEMORY switch is in the NORM position as shown.

4-138. The MEMORY switch is a slide type switch. When placed in the NORM position, it transfers the signal PON from power fail card A1, through front panel coupler card A101, and through the MEMORY switch and pin 17 of the front panel coupler card as signal MNS. Signal MNS is transferred from pin 22 of the front panel coupler card through the backplane wiring to pin 74 of memory module decoder card A2 to pin 7 of "nor" gate MC87B. When the signal MNS is true at pin 7 of MC87B the output signal $\overline{\text{MNS}}$ at pin 9 will go false. The signal $\overline{\text{MNS}}$ is transferred through pin 76 of the memory module decoder card, and pins 19, 20, 22, and 26 of timing generator card A106, to pins 1, 2, 3, and 14 of "and" gate MC47A. When the signal $\overline{\text{MNS}}$ goes false it disables MC47A and causes its output at pin 13 to go false. This false output is transferred to pin 1 of "nor" gate MC46A and causes its output at pin 13 to go true. This true output is transferred to pin 8 of MC27C which is the controlling gate for the signal MTE. When all inputs to MC27C are true the signal MTE will be generated and allow the transfer of data into and out of memory.

4-139. Thus when the MEMORY switch is in the NORM position, data can be transferred into or out of memory. When the switch is in the OFF position all memory data transfers are disabled.

4-140. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-12, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check for a +4.5-volt level at A501-F. If normal, proceed to step "c". If abnormal, check the connection between A501-F and A1-58 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047), extend memory module decoder card A2 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

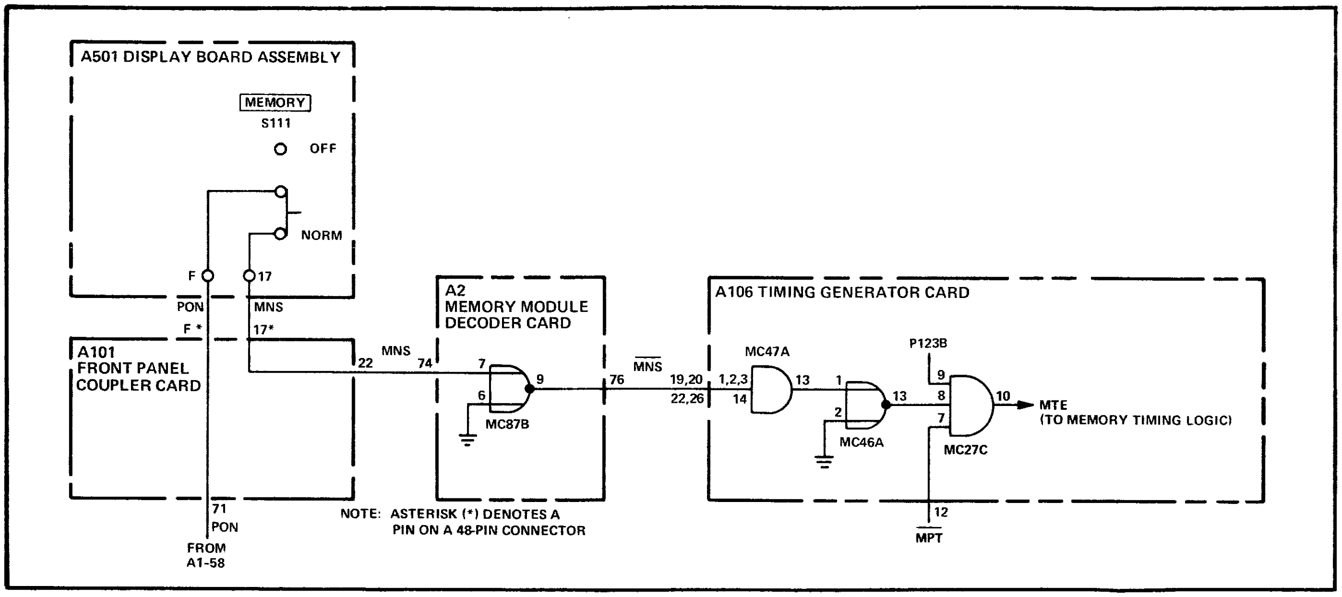

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Figure 4-12. MEMORY Switch Circuit, Servicing Diagram

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A2-74.

f. At the computer display board assembly, assure that the MEMORY switch is in the NORM position and check the oscilloscope display for a +4.5-volt level. Then place the MEMORY switch in the OFF position and check the oscilloscope for a 0-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check the connection from A2-74 to A501-17 for continuity and check the MEMORY switch as the most probable cause of trouble.

g. Place the channel A oscilloscope probe on pin 76 of the memory module decoder card.

Note

In the following steps, any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

h. At the computer display board assembly, assure that the MEMORY switch is in the NORM position and check the oscilloscope display for a 0-volt level. Then place the MEMORY switch in the OFF position and check the oscilloscope for a +4.5-volt level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A2MC87 as the most probable cause of trouble.

i. At the computer front panel, press and release the POWER switch to turn off power.

j. Using the extender card and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

k. At the computer front panel, press and release the POWER switch to turn on power.

l. Place the channel A oscilloscope probe on A106MC27-10.

m. At the computer display board assembly, assure that the MEMORY switch is in the NORM position and check the oscilloscope display for a +4.5 volt level. Then place the MEMORY switch in the OFF position and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "n". If the oscilloscope display is abnormal, check A106MC27, A106MC46, and A106MC47 for proper operation and refer to the LOADER switch test procedure.

n. If all indications of the above test procedure are normal, the MEMORY switch and circuits are operating normally.

4-141. PHASE SWITCH. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with the PHASE switch S112 located on display board assembly A501.

4-142. Description. The circuits associated with the PHASE switch are shown in figure 4-13. In the following description it is assumed that the PHASE switch is in the NORM position as shown.

4-143. The PHASE switch is a slide type switch. When placed in the NORM position, it transfers +4.5 volts through front panel coupler card A101, and through the PHASE switch and pin E of the front panel coupler card as signal PNS. Signal PNS is transferred from pin 18 of the front panel coupler card through the backplane wiring through pin 43 of timing generator card A106, to pin 7 of "and" gate MC35C. When the signal PNS goes false (The PHASE switch is placed in the LOOP position.) it disables MC35C and inhibits its output at pin 10, which is the clock pulse to the phase logic flip-flops. This causes the currently active phase to remain set.

4-144. Thus when the PHASE switch is in the NORM position, the phase flip-flops are clocked normally and change according to the computer logic. When the switch is in the LOOP position the clock pulse is inhibited and the phase logic cannot change.

4-145. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-13, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check for a +4.5-volt level at A501-M. If normal, proceed to step "c". If abnormal, check the connection between A501-M and A101-39,40 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047) and the extender cable (part no. 02116-6040), extend timing generator card A106 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-43.

f. At the computer display board assembly, assure that the PHASE switch is in the NORM position and check

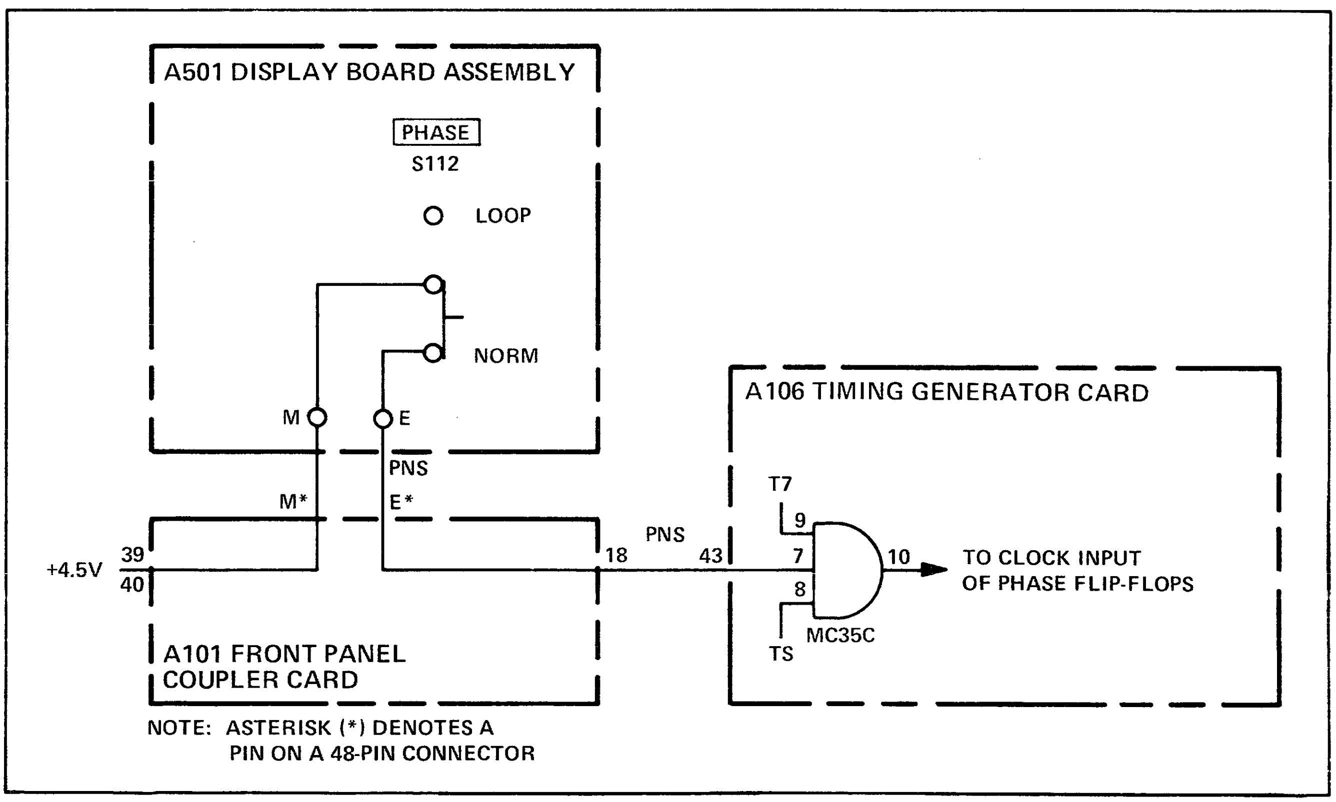

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Figure 4-13. PHASE Switch Circuit, Servicing Diagram the oscilloscope display for a +4.5-volt level. Then place the PHASE switch in the LOOP position and check the oscilloscope for a 0-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check the connection from A106-43 to A501-E for continuity and check the PHASE switch as the most probable cause of trouble.

g. Place the channel A oscilloscope probe on A106MC35-10.

h. At the computer display board assembly, assure that the PHASE switch is in the NORM position and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. Then place the PHASE switch in the LOOP position and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A106-MC35 as the most probable cause of trouble and refer to paragraph 4-153 and troubleshoot the basic timing circuits.

i. If all indications of the above test procedure are normal, the PHASE switch and circuits are operating normally.

4-146. INSTRUCTION SWITCH. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with the INSTRUCTION switch S113 located on display board assembly A501.

4-147. Description. The circuits associated with the INSTRUCTION switch are shown in figure 4-14. In the following description it is assumed that the INSTRUCTION switch is in the NORM position as shown.

4-148. The INSTRUCTION switch is a slide type switch. When placed in the NORM position, it transfers 0-volts from the INSTRUCTION switch and pin H of the front panel coupler card A101 as signal ILS. Signal ILS is transferred from pin 26 of the front panel coupler card through the backplane wiring to pin 73 of instruction decoder card A107, to pin 7 of "and" gate MC106C. When the signal ILS goes true (The INSTRUCTION switch is placed in the LOOP position.) it enables MC106C and causes its output at pin 10 to go true. This true output is transferred to pin 1 of "nor" gate MC96A and causes its output at pin 13 to go false. This false output is transferred to pin 14 of "and" gate MC97A and disables this gate which is the controlling gate for the signal SBO. By disabling MC97A the signal SBO is inhibited and the P- and M-registers will remain in their current configuration.

4-149. Thus when the INSTRUCTION switch is in the NORM position, the signal SBO can be generated and the normal incrementing of the P- and M-registers can take place. When the switch is in the LOOP position, signal SBO cannot be generated and the P- and M-registers cannot be incremented.

4-150. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-14, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

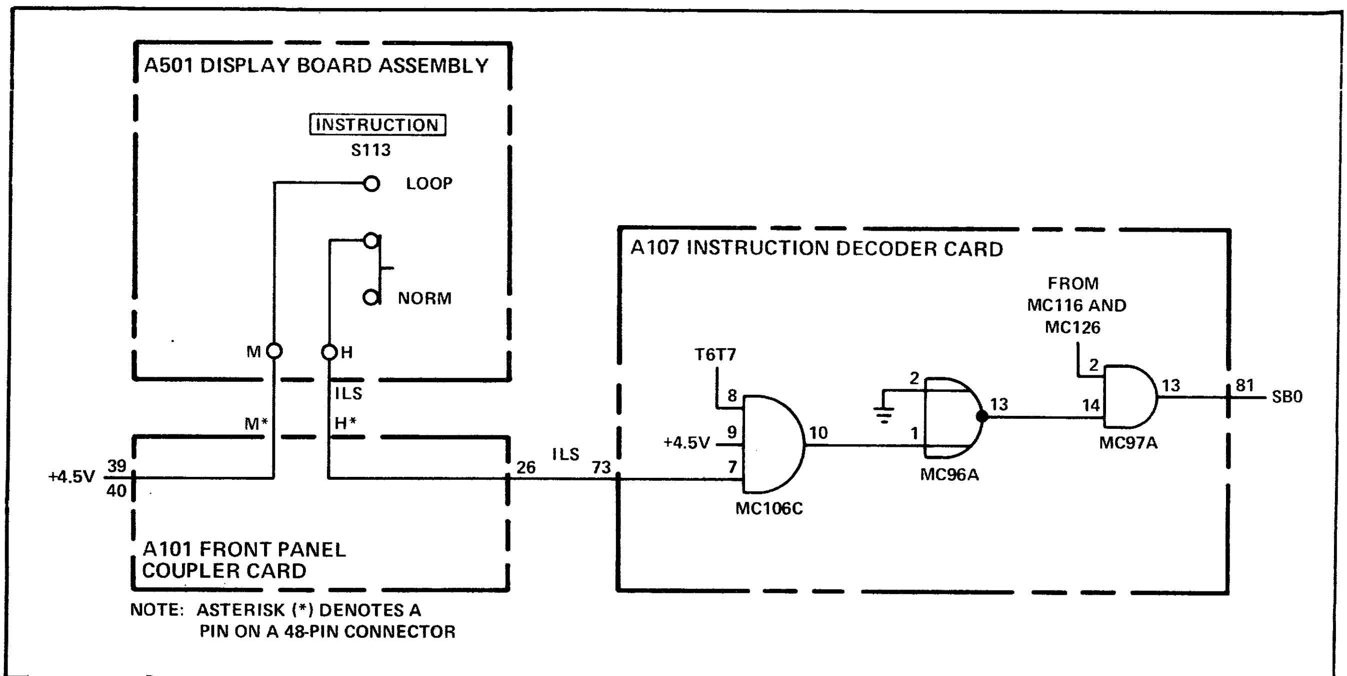

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Figure 4-14. INSTRUCTION Switch Circuit, Servicing Diagram

b. Using the multi-function meter, check for a +4.5-volt level at A501-M. If normal, proceed to step "c". If abnormal, check the connection between A501-M and A101-39,40 for continuity.

c. At the computer front panel, press and release the POWER switch to turn off power.

d. Using the extender card (part no. 02115-6047), extend instruction decoder card A107 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A107-73.

f. At the computer display board assembly, assure that the INSTRUCTION switch is in the NORM position and check the oscilloscope display for a 0-volt level. Then place the INSTRUCTION switch in the LOOP position and check the oscilloscope for a +4.5-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check the connection from A107-73 to A501-H for continuity and check the INSTRUCTION switch as the most probable cause of trouble.

g. Place the channel A oscilloscope probe on A107MC96-13.

Note

In the following steps any reference to a signal voltage level of +4.5-volts is to be considered a logic "1" level except a specific voltage tie as shown on the troubleshooting and servicing diagrams. Any reference to a signal voltage level of 0-volts is to be considered a logic "0" level. A logic "1" (true) voltage level can vary between approximately +1.8 volts to +3.0 volts. A logic "0" (false) voltage level can vary between approximately 0 volts to +1.5 volts. Refer to Appendix A for specific logic voltage levels required to drive a specific logic circuit. For additional information concerning waveforms and oscilloscope settings, refer to paragraph 4-53 and table 4-10.

h. At the computer display board assembly, assure that the INSTRUCTION switch is in the NORM position and check the oscilloscope display for a +4.5-volt level. Place the INSTRUCTION switch in the LOOP position and check the oscilloscope display for a 400 ηs negative-going pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A107MC96 and A107MC106 as the most probable cause of trouble and refer to paragraph 4-153 and troubleshoot the basic timing circuits.

i. If all indications of the above test procedure are normal, the INSTRUCTION switch and circuits are operating normally.

4-151. TIMING CIRCUITS.

4-152. The timing circuit function is comprised of the basic timing circuit and the memory timing circuit. Troubleshooting data for the basic timing circuit is presented in paragraphs 4-153 through 4-155. Troubleshooting data for the memory timing circuit is presented in paragraphs 4-156 through 4-163.

4-153. BASIC TIMING. The following paragraphs provide a description and test procedure for the basic timing circuit which is located on timing generator card A106.

4-154. Description. Basic computer timing is derived from a free-running, crystal-controlled, 10-MHz oscillator. A timing diagram showing the basic timing signal outputs is presented in figure 4-15, and typical signal waveforms are presented in figures 4-16 through 4-20. Refer to paragraphs 3-28 through 3-43 in Section III for a detailed description of the circuits used in generating these signals, and to figure 5-24 in section V for a detailed logic diagram.

4-155. Test Procedure. Using a dual-trace oscilloscope and the diagrams referenced in the preceding paragraph, proceed as follows:

a. Press and release the POWER switch to turn off power.

b. Using the extender card (part no. 02116-6040) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

c. Press and release the POWER switch to turn on power.

d. Using the information provided in figure 4-16, check the 10-MHz oscillator output and time TO waveforms. (The 10-MHz waveform must have an overall amplitude of 2 to 7 volts peak-to-peak, with the positive-going peak reaching the +1.5-volt level or higher, and the negative-going peak reaching the +1-volt level or lower.) If both waveform indications are normal, proceed to step "j". If the waveforms cannot be displayed on the oscilloscope, perform steps "e" through "i" following.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 us.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-3 (External Clock signal).

f. Adjust the oscilloscope to observe the output of the 10-MHz oscillator (External Clock signal). The output should be similar to that shown in figure 4-16 and as described in step "d" above. If the indication is normal, proceed to step "g". If the indication is abnormal, troubleshoot the 10-MHz oscillator circuit.

g. Connect the channel A oscilloscope probe to A106-55 and then to A106-67 to check signals TS and TSA, respectively (see figure 4-15). If both signals are normal, proceed to step "h". If signal TS is normal, but signal TSA is abnormal, MC75 is the most probable cause of trouble. If signal TSA is normal, but signal TS is abnormal, MC42 is the most probable cause of trouble. If signals TS and TSA are both abnormal, MC52 or MC82 (CF1 FF) is the most probable cause of trouble.

h. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: channel B.

(3) Time/cm: 0.2 us.

(4) Channel A and channel B volts/cm: 0.2 (if using 10:1 probes).

(5) Channel A input: MC62-14 (signal CL1).

(6) Channel B input: A106-55 (signal TS).

i. Adjust the oscilloscope to observe signal CL1 on channel A (see figure 4-15). Then connect the channel A input to MC62-13 to observe signal CL2. If both signals are normal, troubleshoot the ring counter and the associated output and control gates. If both signals are abnormal, MC72 (CF2 FF) is the most probable cause of trouble. If one signal or the other is abnormal, but not both, MC62 is the most probable cause of trouble.

j. Using the information provided in figures 4-15 and 4-17 through 4-20, check the remaining signal outputs from the basic timing circuit. If all waveform indications are normal, the basic timing circuit is operating properly. If an abnormal waveform indication is observed, troubleshoot accordingly.

Note

To check the operation of the basic timing circuits during a 2.0-microsecond machine cycle, refer to the test procedure presented in paragraph 4-163 (steps "f" and "g").

4-156. MEMORY TIMING. The following paragraphs provide a description and test procedure for the memory timing circuit which is located on timing generator card A106.

4-157. Description. The memory timing circuit is shown in detail in figure 5-24. Memory timing signals MRT, MST, MWT, and MIT control the read and write operations performed in the memory section of the computer. Memory timing signal MWL is a status signal used for control by the memory protect option and memory parity check option (refer to the applicable operating and service manuals for these options if installed in the computer).

4-158. The memory timing signals are derived from basic timing signal inputs which include "not" CF1, CF2, "not" CF2, T0, T0T1, T1T2, T2, T4T5, T5T6, and T6T7. The generation of the memory timing signals is controlled by signal inputs from the phase logic circuits (PH3 and P123B signals), A- and B-register addressing circuits (AAF and BAF signals), instruction decoding logic (JSB, STR, and ISZ signals), memory protect circuits ("not" MPT signal), MEMORY switch A501S111 and LOAD MEMORY switch A502S105 at the front panel ("not" MNS and LMS signals), and the extended arithmetic unit option (ISG signal; refer to the operating and service manual for this option if installed in the computer).

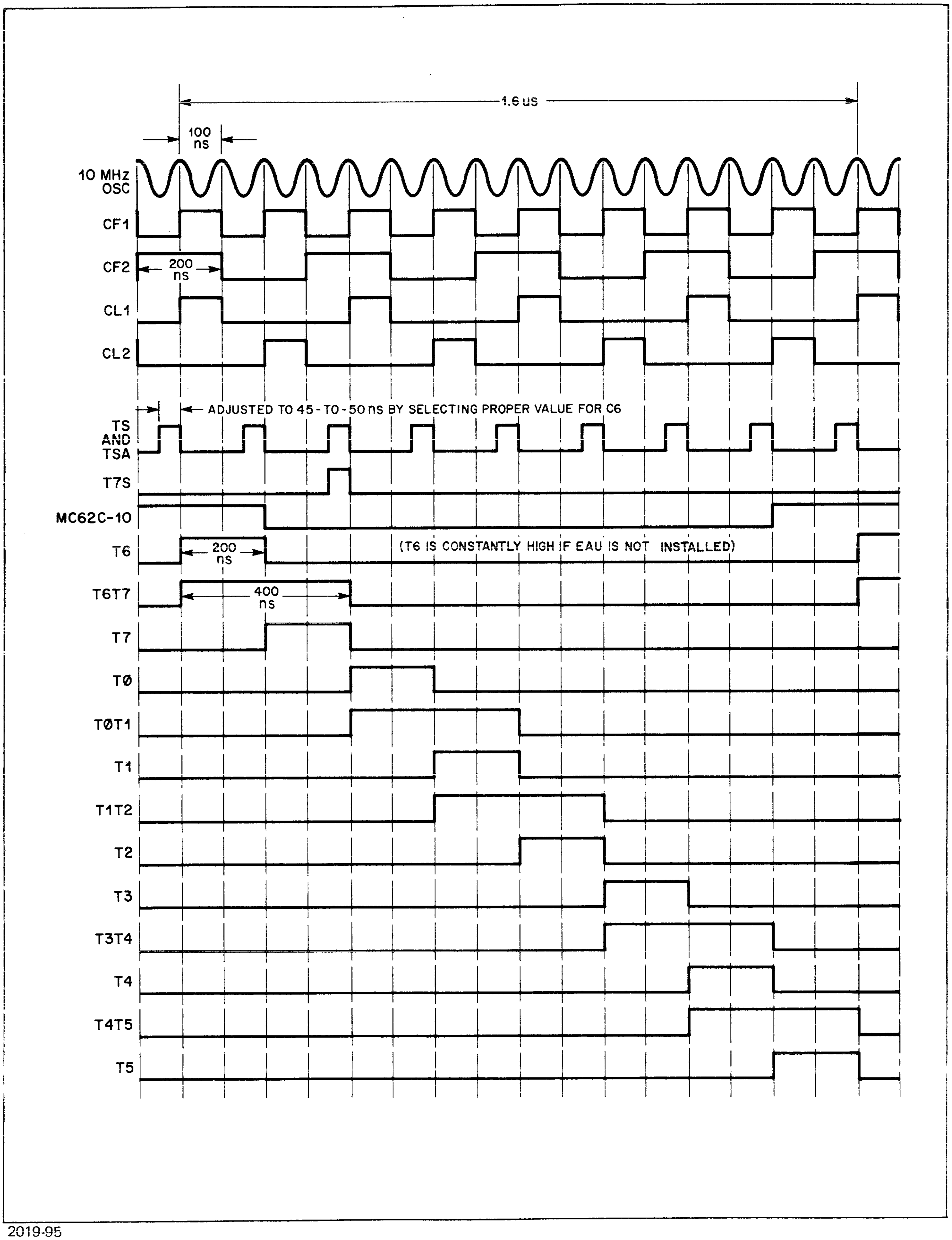
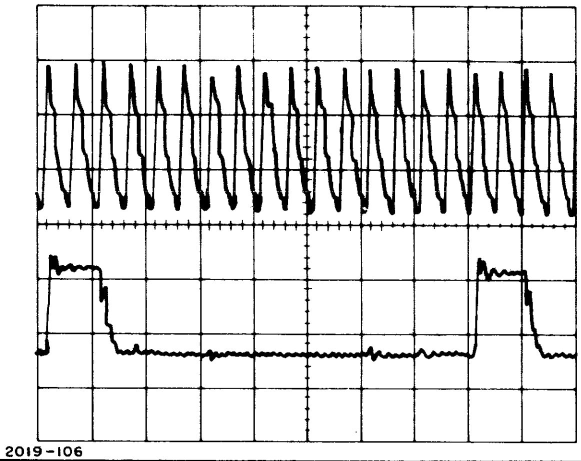


Figure 4-15. Basic Timing Circuit, Timing Diagram



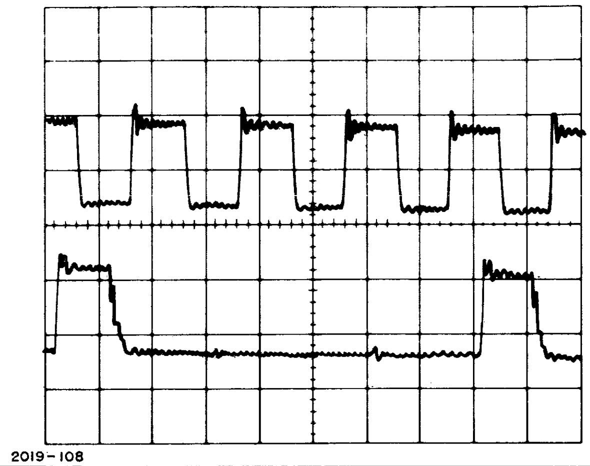
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (10 MHz):
Input A106-3
Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-16. 10-MHz Oscillator Output and Time T0 Waveforms



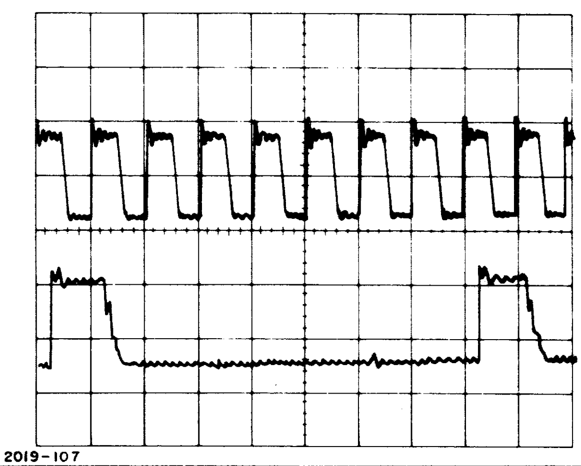
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (CF2):
Input A106MC72-13
Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-18. Signal CF2 and Time T0 Waveforms



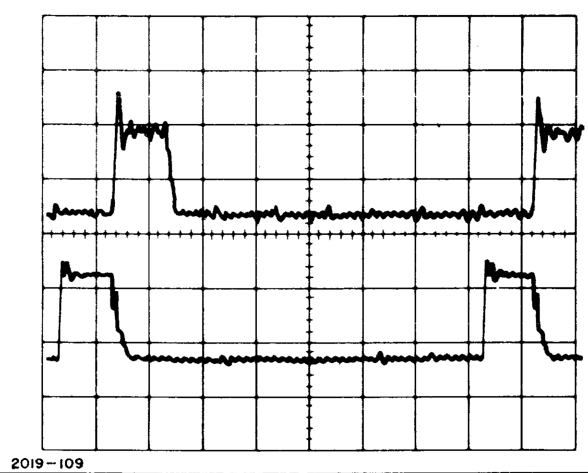
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (CF1):
Input A106MC82-13
Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-17. Signal CF1 and Time T0 Waveforms



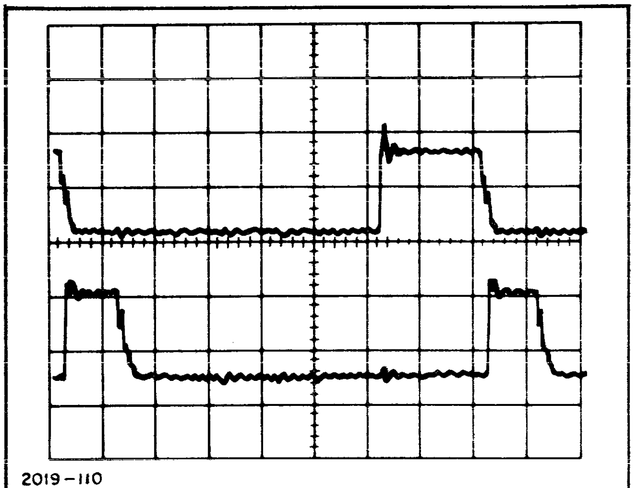
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (T1):
Input A106-53
Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-19. Time T1 and Time T0 Waveforms



OSCILLOSCOPE CONNECTIONS AND SETTINGS

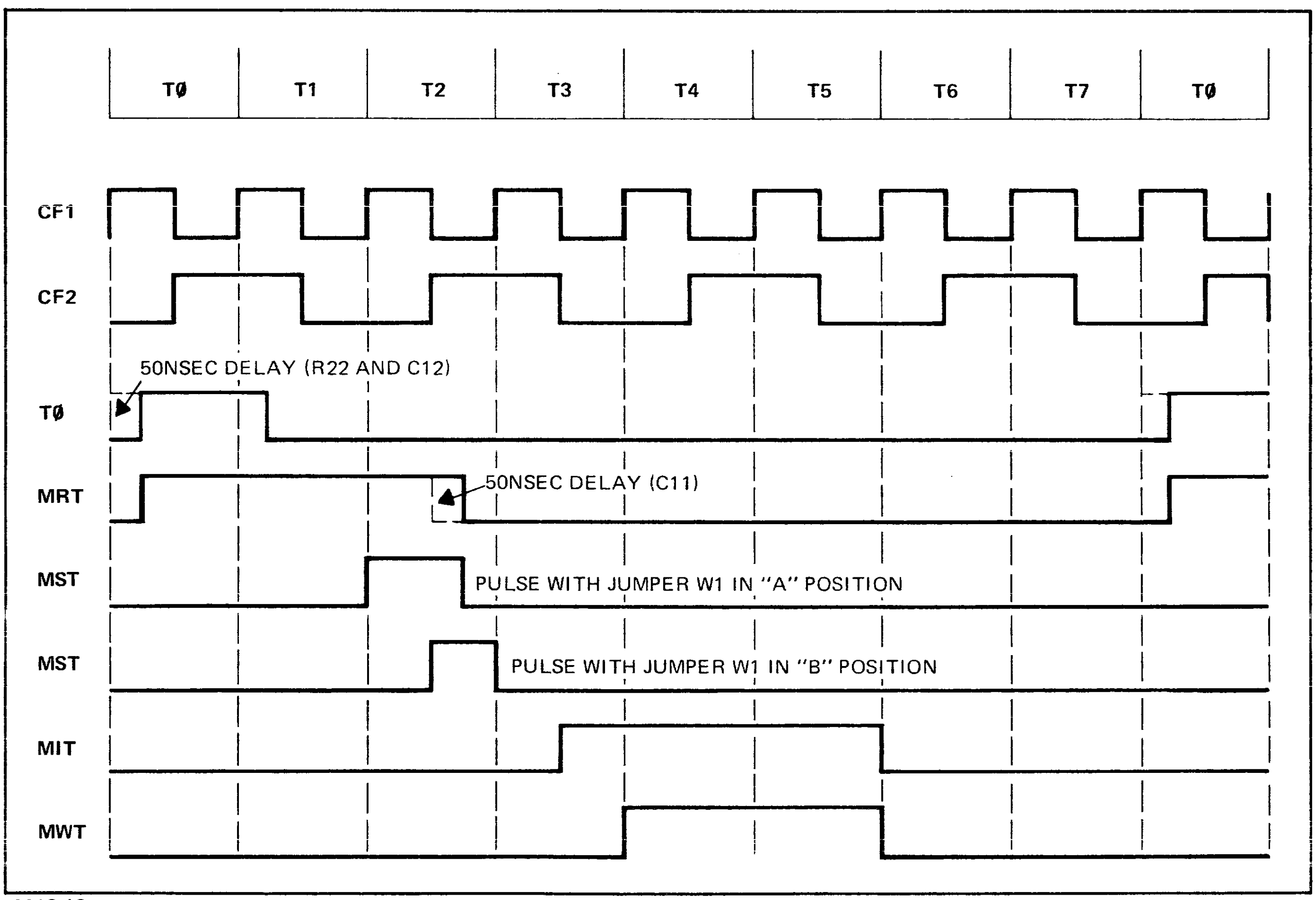
Channel A (T6T7):
- **Input** A106-30
- **Volts/cm** . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
- **Input** A106TP1
- **Volts/cm** . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

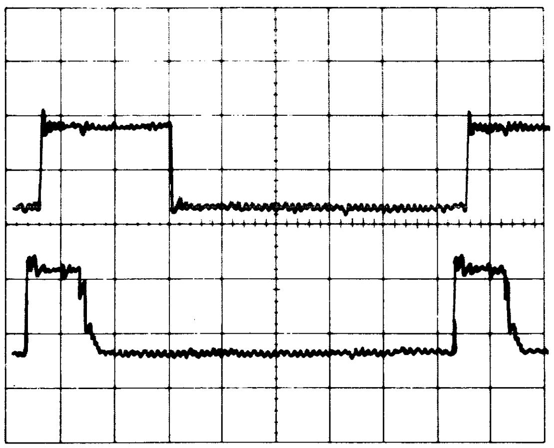
Figure 4-20. Time T6T7 and Time T0 Waveforms

4-159. Figures 4-21 through 4-25 show timing and waveforms for the memory read and write periods occurring during a normal 1.6-microsecond machine timing cycle. In order for the memory timing signals to be generated as shown in figure 4-21, the state of the control signal inputs specified in the preceding paragraph must be such that gates MC27C and MC77C are enabled and providing true outputs, and gate MC204B is disabled and providing a false output. Under these circuit conditions, memory timing enable signal MTE is true, and the basic timing circuit generates a 1.6-microsecond machine timing cycle. (If gate MC27C is disabled, signal MTE will be false and all memory timing signal outputs will be inhibited during the machine cycle. If gate MC104B is enabled, the basic timing circuit will generate a 2.0-microsecond machine timing cycle and the memory timing signals will be generated as explained in paragraphs 4-160 through 4-162 which follow.) During the memory read period (TOTS through T2), signal MRT is generated at the output of gate MC57A, and signal MST is generated at the output of gate MC57B. As noted in figure 4-21, the pulse width at the output of gate MC57B is controlled by the position of jumper W2. (Also note that if gate MC77C is disabled during the memory read period, signal MST will not be generated). During the memory write period (T3TS through T5), gates MC55A, MC36B, MC36B, MC36C, and MC37B work in combination to generate signal MIT. Similarly, gates MC55A, MC26B, and MC67B work in combination to generate signal MWT at



2019-19

Figure 4-21. Memory Timing Circuit (1.6 Microsecond Machine Cycle), Timing Diagram



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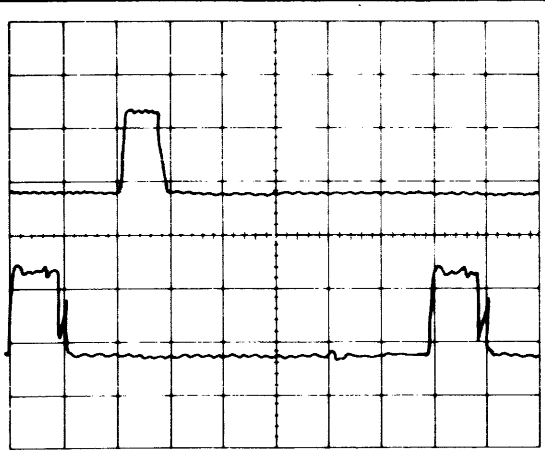
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (MRT):
Input A106-29
Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-22. Signal MRT and Time T0 Waveforms During 1.6 Microsecond Machine Cycle



2019-20

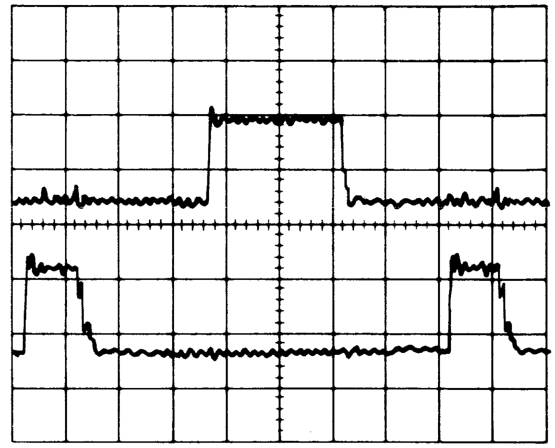
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (MST):
Input A106-32
Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-23. Signal MST and Time T0 Waveforms During 1.6 Microsecond Machine Cycle



2019-113

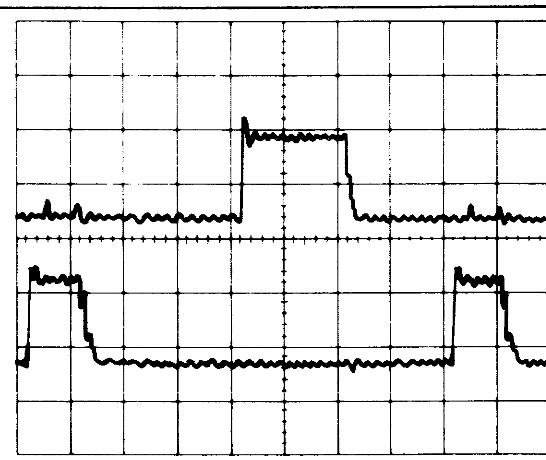
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (MIT):
Input A106-25
Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-24. Signal MIT and Time T0 Waveforms During 1.6 Microsecond Machine Cycle



2019-114

OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (MWT):
Input A106-35
Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-25. Signal MWT and Time T0 Waveforms During 1.6 Microsecond Machine Cycle time T4T5. Signal MWL is inhibited and remains false during a 1.6-microsecond machine cycle, unless circuit conditions are such that gate MC77C is inhibited and causes gate MC55B to produce a true output.

4-160. Figures 4-26 through 4-30 show timing and waveforms for a read and write cycle that occurs when an ISZ instruction is processed and the machine cycle is stretched by an additional 0.4 microseconds. In order for the memory timing signals to be generated as shown in figure 4-26, the state of the control signal inputs specified in paragraph 4-158 must be such that gates MC27C, MC77C, and MC104B are enabled and providing true outputs. This circuit condition will exist only when an ISZ instruction is processed, and is the only condition under which the basic timing circuit will generate a 2.0-microsecond machine timing cycle. During the read portion of this machine cycle, the MRT and MST signals are generated in exactly the same manner as described in the preceding paragraph. However, with the ISZ signal true, the operation of the basic timing circuit and the generation of the MIT and MWT signals is modified, as explained in the following paragraphs, due to the true signal output at gate MC104B.

4-161. The gating network consisting of gates MC124A, MC104A, MC124B, and MC62C controls the operation of the T6T7 FF in the basic timing circuit. During a normal 1.6-microsecond machine cycle, the output at MC62C is true during time T5T6, as shown in figures 4-15 and 4-26. This permits two consecutive CL1 clocking pulses to set the T6T7 FF at the 1.2-microsecond point in the machine cycle, and to reset the T6T7 FF at the 1.6-microsecond point in the machine cycle. With the output from gate MC104B true, however, the operation of the gating network is modified so that the output of MC62C is false during the time that the T6T7 FF is normally clocked. As shown in figure 4-26, this delays the clocking of the T6T7 FF by two time periods, or 0.4 microseconds, and a 2.0-microsecond machine cycle results.

4-162. During the 2.0-microsecond machine cycle, gates MC16C, MC16A, and MC37B work in combination to generate signal MIT, and gates MC104C, MC26C, and MC67B work in combination to generate signal MWT. Signal MWL, generated at the output of gate MC67A, is true during the entire machine cycle. As shown in figure 4-26, signal T6 is not generated during a 2.0-microsecond machine cycle, because the T5T6 FF and the T6T7 FF are not set during the same time period as they normally are during a 1.6-microsecond machine cycle.

4-163. <u>Test Procedure.</u> Using a dual-trace oscilloscope and the diagrams referenced in the preceding description, proceed as follows:

a. Press and release the POWER switch to turn off power.

b. Using the extender card (part no. 02116-6040) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

c. Press and release the POWER switch to turn on power.

d. At the front panel of the computer, proceed as follows:

Note

> Steps (1) through (6) below contain a step-by-step procedure for manually loading a test program into the computer's memory. These instructions can be stored in any two consecutive memory locations in a memory page (other than protected, reserved, or unaccessible areas of memory). The locations specified below for these instructions are typical, and may be changed to any suitable area in memory not being used to prevent destroying program data or instructions already stored in the specified locations. If a starting address other than 004000 is used, modify the octal values accordingly for the SWITCH REGISTER settings given in steps (1), (3), and (5).

(1) Set the SWITCH REGISTER to 004000 (typical address for the first instruction) and press and release the LOAD ADDRESS switch.

(2) Set the SWITCH REGISTER to 003000 (CMA) and press and release the LOAD MEMORY switch.

(3) Set the SWITCH REGISTER to 026000 (JMP) and press and release the LOAD MEMORY switch.

(4) Set the SWITCH REGISTER to 177777 and press and release the LOAD A switch.

(5) Set the SWITCH REGISTER to 004000 (starting address) and press and release the LOAD ADDRESS switch.

(6) Press and release the RUN switch and proceed to step "e".

e. Using the information provided in figures 4-22 through 4-25, check the MRT, MST, MIT, and MWT signal waveforms. If all waveform indications are normal, proceed to step "f". If one or more waveform indications are abnormal, refer to the timing information provided in figure 4-21, and to the applicable equations in table 4-8, and check the related timing and control input signals. If all input signals are normal, the trouble is in the memory timing circuit. (Check signal MTE as the first step of troubleshooting.) If one or more input signals are abnormal, troubleshoot the circuit functions providing the faulty input signal.

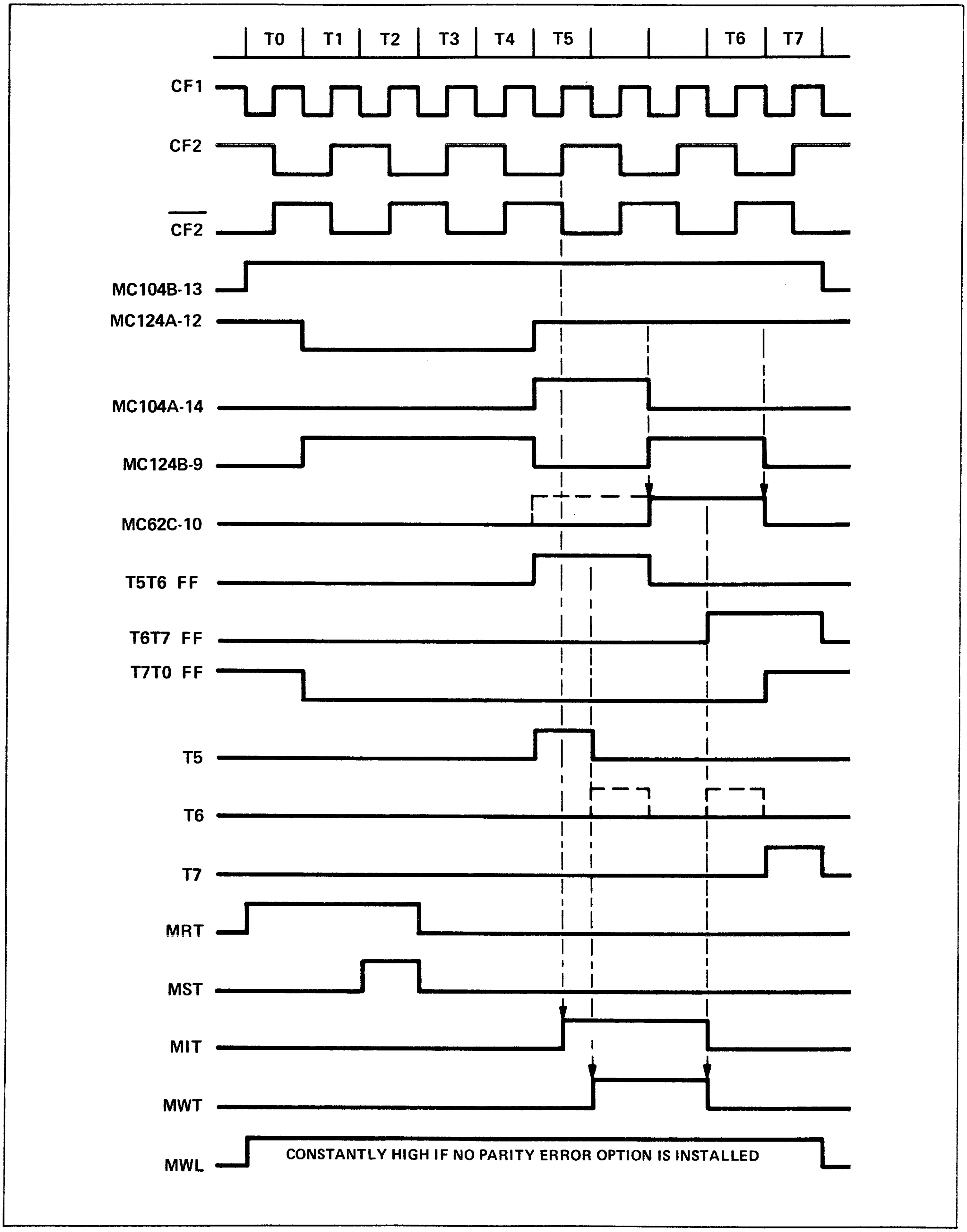


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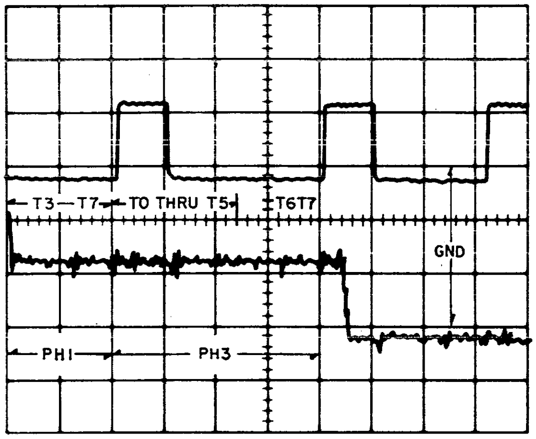
Figure 4-26. Memory Timing Circuit (2.0 Microsecond Machine Cycle), Timing Diagram



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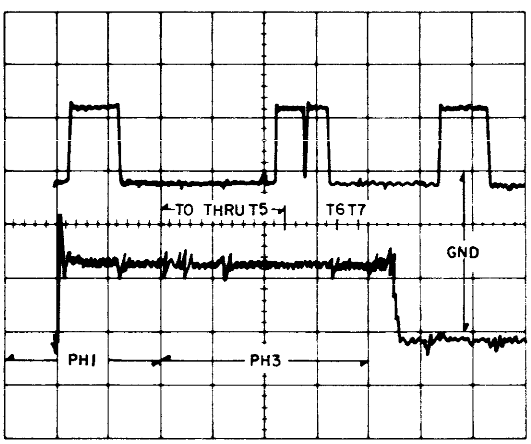
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (MRT):
- Input A106-29
- Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (ISZ):
- Input A106-24
- Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.5 us

Figure 4-27. Signals MRT and ISZ Waveforms During 2.0 Microsecond Machine Cycle



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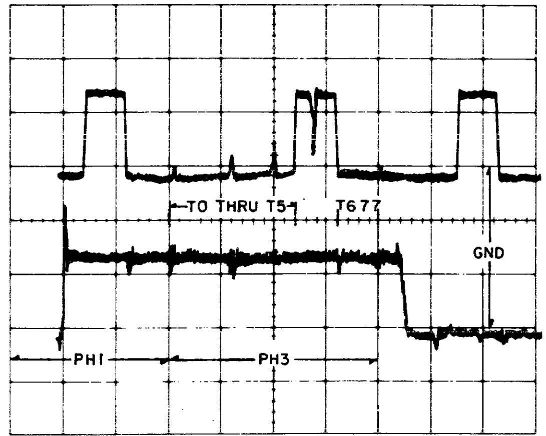
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (MIT):
- Input A106-25
- Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (ISZ):
- Input A106-24
- Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.5 us

Figure 4-28. Signals MIT and ISZ Waveforms During 2.0 Microsecond Machine Cycle



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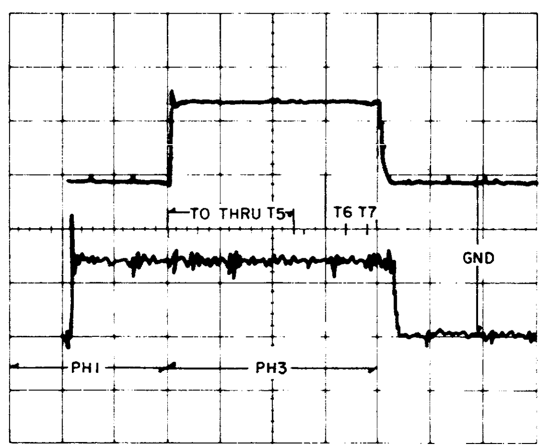
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (MWT):
- Input A106-35
- Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (ISZ):
- Input A106-24
- Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.5 us

Figure 4-29. Signals MWT and ISZ Waveforms During 2.0 Microsecond Machine Cycle



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OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (MWL):
- Input A106-33
- Volts/cm . . . . 0.2 (if using 10:1 probe)

Channel B (ISZ):
- Input A106-24
- Volts/cm . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . 0.5 us

Figure 4-30. Signals MWL and ISZ Waveforms During 2.0 Microsecond Machine Cycle

f. At the front panel of the computer, proceed as follows:

Note

Any three consecutive locations in a memory page can be used to store the program instructions specified in the following procedure. If a starting address other than 004000 is used, modify the octal values accordingly for the SWITCH REGISTER settings given in steps (1), (3), and (4).

(1) Set the SWITCH REGISTER to 004000 (typical address for the first instruction) and press and release the LOAD ADDRESS switch.

(2) Set the SWITCH REGISTER to 036001 (ISZ) and press and release the LOAD MEMORY switch.

(3) Set the SWITCH REGISTER to 026000 (JMP) and press and release the LOAD MEMORY switch twice.

(4) Set the SWITCH REGISTER to 004000 (starting address) and press and release the LOAD ADDRESS switch.

(5) Press and release the RUN switch. Then proceed to step "g".

g. Using the information provided in figures 4-27 through 4-30, check the MRT, MIT, MWT, and MWL signal waveforms. If all waveform indications are normal, the memory timing circuit is operating properly. If one or more waveform indications are abnormal, refer to the timing information provided in figure 4-26, and to the applicable equations in table 4-9, and check the related timing and control input signals. If all input signals are normal, the trouble is in the memory timing circuit. (Check the signal output at gate MC104B as the first step of troubleshooting.) If one or more input signals are abnormal, troubleshoot the circuit functions providing the faulty input signal.

4-164. PHASE LOGIC CIRCUITS.

4-165. The phase logic circuits generate the control signals that provide the four machine phases for the basic computer. The four phases are the fetch phase (phase 1), the indirect phase (phase 2), the execute phase (phase 3), and the interrupt phase (phase 4). These phases are shown with respect to the basic timing and memory timing cycles in figures 4-31 through 4-34.

4-166. A phase is set for one complete machine cycle (time T0 through time T7). One or another (but only one) of these phases is set during every machine cycle. The phase setting signals are generated by the logic of the basic timing circuits and the logic of the various instructions to be processed. When a phase is set, it will remain set until the end of the current machine cycle. At the end of the current machine cycle the same phase can remain set or a different phase can be set. But, a new phase cannot be set during a currently operating phase.

4-167. FETCH PHASE. The following paragraphs provide a description and test procedure for the circuits used by the fetch phase (phase 1). The processing operations are summarized in table 4-11. Point-to-point signal flow during phase 1 is shown in figure 4-31.

4-168. Description. Phase 1 can be thought of as the computers basic phase. During this phase the content of the currently addressed memory location is transferred into the T-register and is interpreted as an instruction. If bit 15 of the instruction is true (indirect bit), the computer will set the indirect phase (phase 2) and will operate under phase 2 control during the next machine cycle. If bit 15 of the instruction is not true but the instruction has been decoded as a two phase instruction, the computer will set the execute phase (phase 3) and will operate under phase 3 control during the next machine cycle. If bit 15 of the instruction is not true and the instruction has not been decoded as a two phase instruction, phase 1 will remain set and the computer will operate under phase 1 control during the

Table 4-11. Fetch Phase Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear IR	Clear TR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 in M (10-15) If I: Set PH2 If D: Set PH3	

next machine cycle. Phase 4 (interrupt) constitutes an exception to the above in that it takes precedence over the operation of all other phases upon their completion.

4-169. Test Procedure. To test the fetch phase circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board A501, set the INSTRUCTION and PHASE switches to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

4-170. The computer is now in the run mode executing the JMP instruction and is locked into the fetch phase. Using a dual-trace oscilloscope, check the signals shown in figure 4-31. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

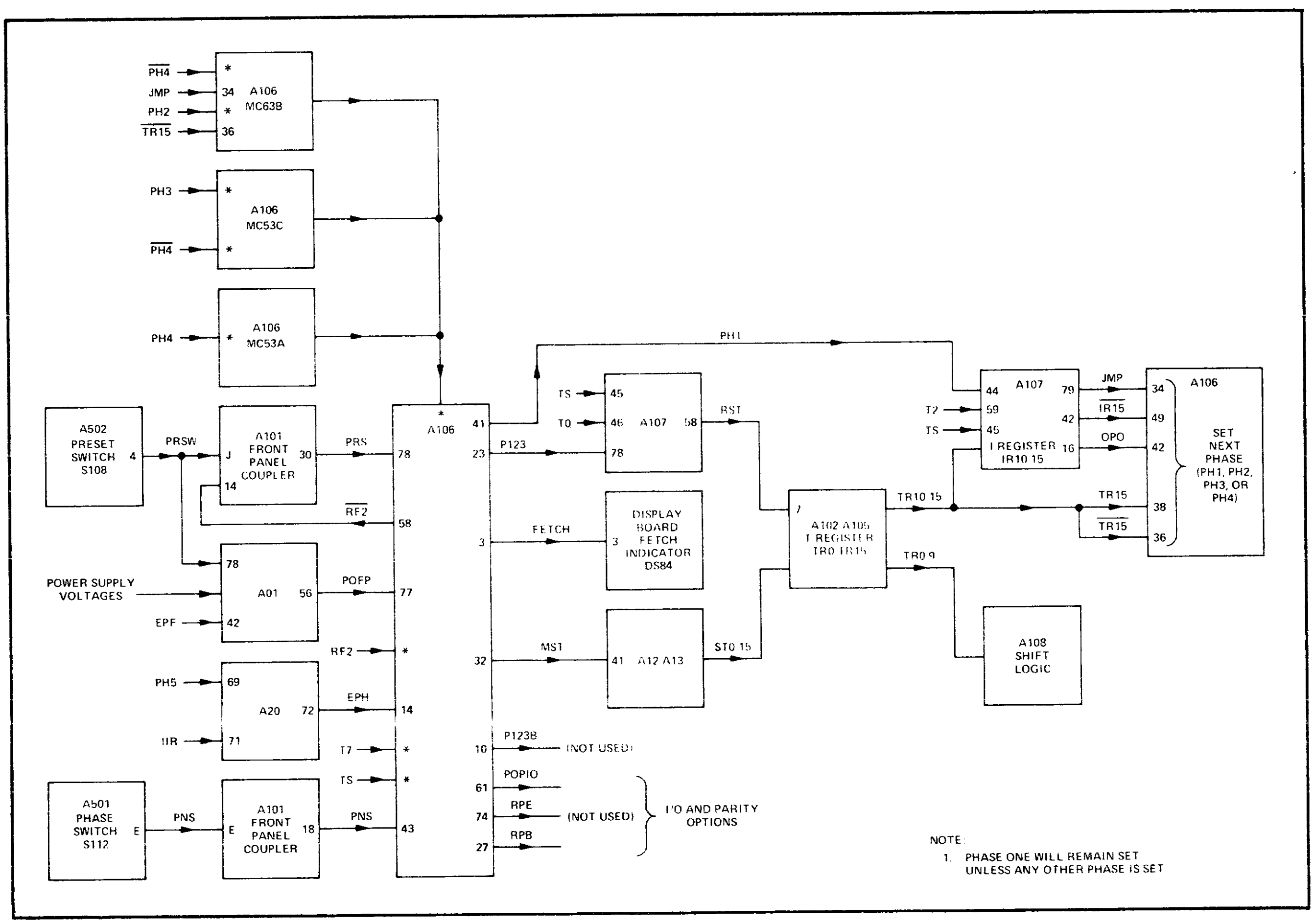

Figure 4-31. Fetch Phase Circuit, Servicing Diagram

4-171. INDIRECT PHASE. The following paragraphs provide a description and test procedure for the circuits used by the indirect phase (phase 2). The processing operations are summarized in table 4-12. Point-to-point signal flow during phase 2 is shown in figure 4-32.

4-172. Description. Phase 2 is generated by bit 15 (indirect bit) of the instruction word being true during a memory reference type instruction. During phase 2 the content of the currently addressed memory location is transferred into the T-register, interpreted as a new address and transferred to the M-register. If bit 15 of this new address is true, the computer will again set phase 2 and will operate under its control during the next machine cycle. If bit 15 of the address is not true, the computer will execute the instruction read into the I-register during the preceding phase 1. The data contained in the last addressed location will be used, and the computer will operate under phase 1 or phase 3 control during the next machine cycle. Phase 2 operation permits addressing any of the possible 32,768 memory locations and can be repeated indefinitely each machine cycle by bit 15 of each addressed location being true.

4-173. The instruction with bit 15 true is read from memory during phase 1. Bit 15 being true causes the next phase generated to be phase 2. The INDIRECT indicator is lit and the T-register is cleared (signal RST). The M-register continues to address the same location that was read into it during phase 1. The contents of that location are read into the T-register at time T2 (signal MST). The T-register data is then read onto the S-bus (signal RTSB). The S-bus data is transferred to the T-bus (signal $\overline{\text{EOF}}$) and stored in the M-register (signals STM 0-15). If bit 15 of the T-register is again true, phase 2 will remain set and the above process will be repeated. If bit 15 of the T-register is false, the instruction read into the I-register during the preceding phase 1 will be executed under either phase 1 or phase 3 control using the data contained in the last addressed location.

4-174. Test Procedure. To test the indirect phase, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 127001 (JMP-I instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 101001 and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. At the computer front panel, press and release the RUN switch.

4-175. The computer is now in the run mode executing the JMP-I instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-32. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Table 4-12. Indirect Phase Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)		WRITE (TR to Mem)				
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
JMP-I	2	Clear TR						If D: TR to P, M and set PH1 If I: TR to M and set PH2	

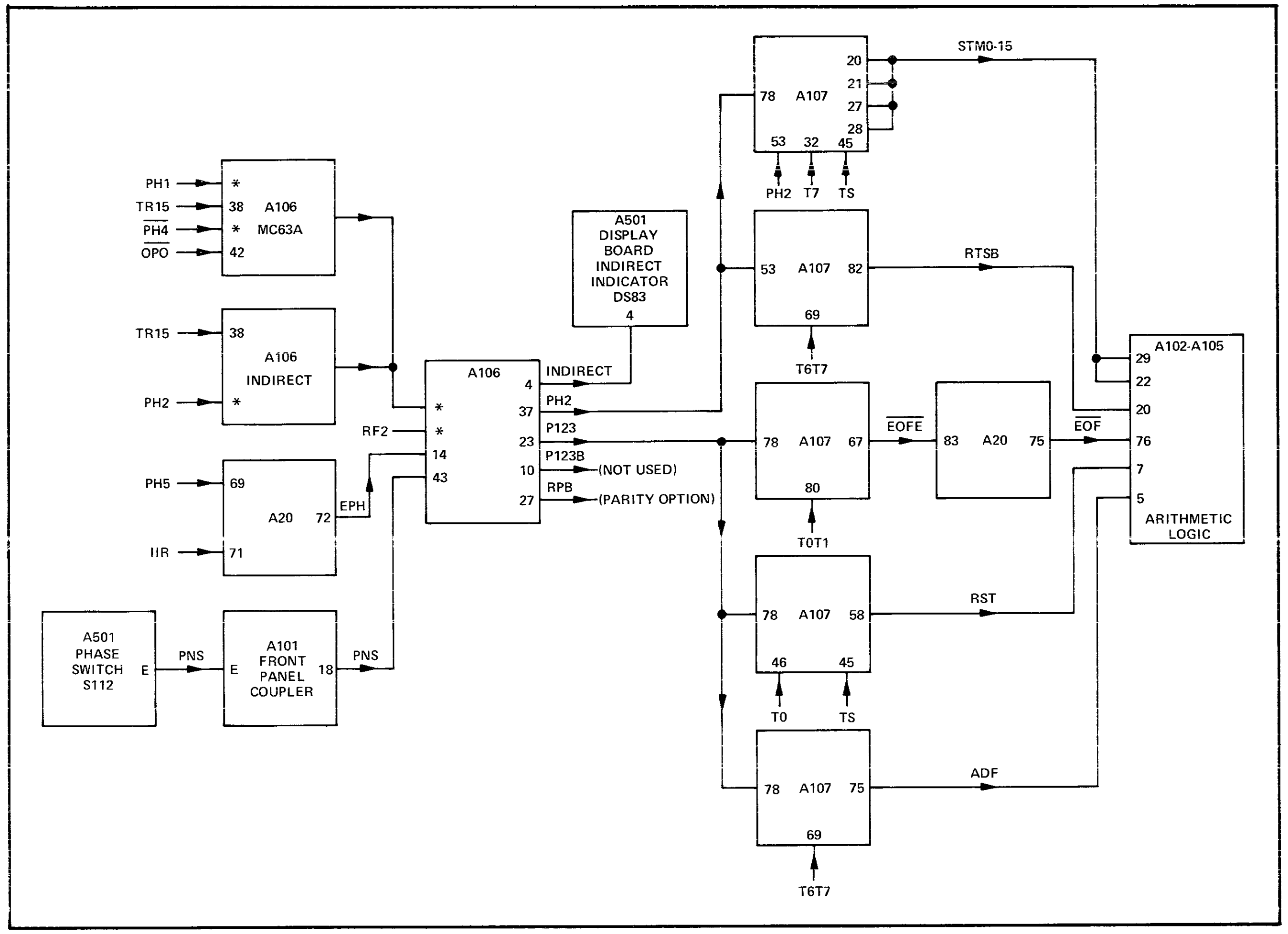

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Figure 4-32. Indirect Phase Circuit, Servicing Diagram

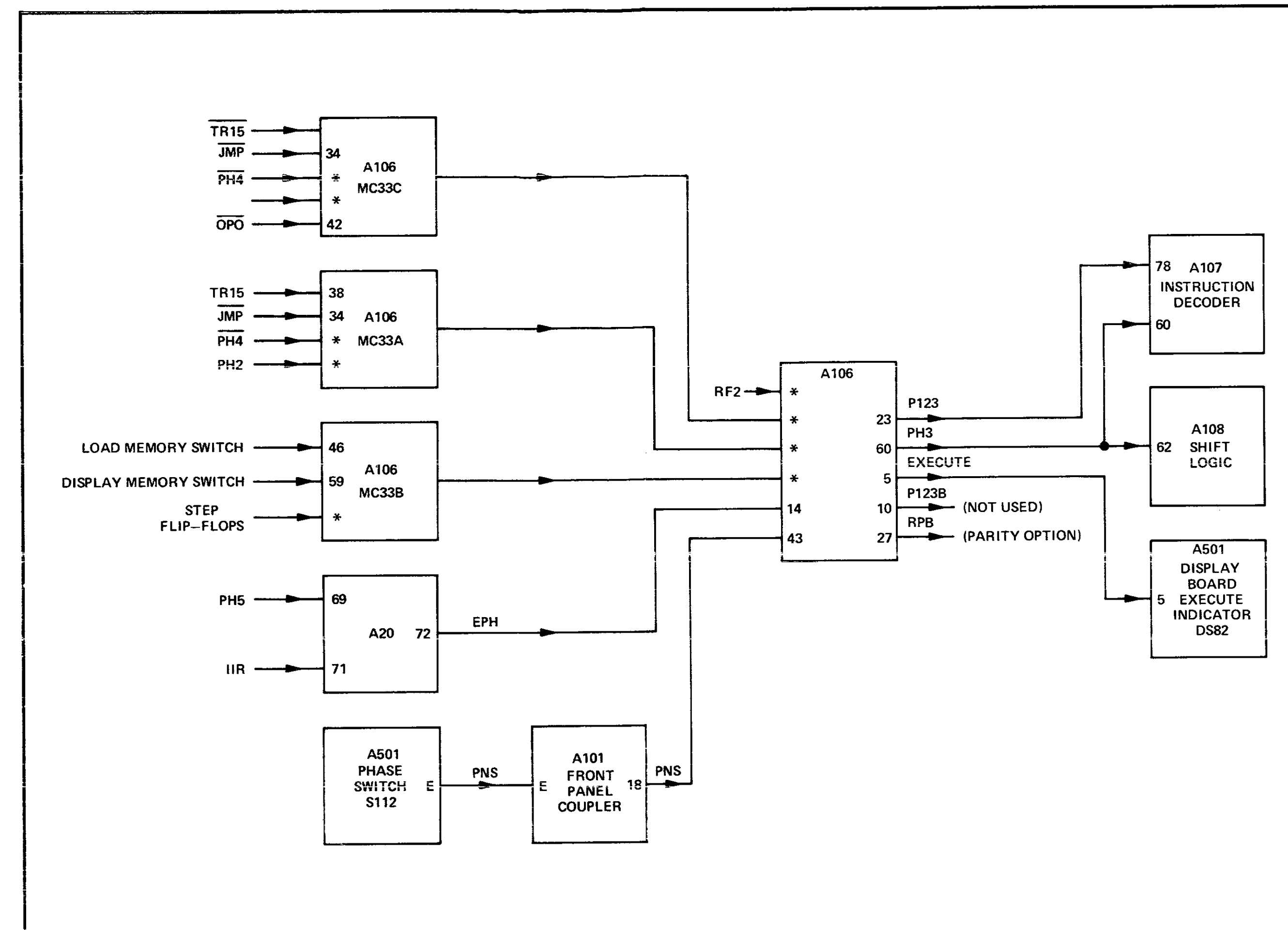

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Figure 4-33. Execute Phase Circuit, Servicing Diagram

4-176. EXECUTE PHASE. The following paragraphs provide a description and test procedure for the circuits used by the execute phase (phase 3). Point-to-point signal flow during phase 3 is shown in figure 4-33.

4-177. Description. Phase 3 processes the data referenced by a memory reference or two-phase instruction according to the specific instruction. Refer to the specific instruction description for further information. Phase 1 will immediately follow phase 3 operation unless an interrupt (phase 4) has been generated.

4-178. Test Procedure. To test the EXECUTE phase circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 070000 (STA instruction) and press and release the LOAD A switch.

b. Set the SWITCH REGISTER to 000000 and press and release the LOAD ADDRESS switch.

c. Press and release the SINGLE CYCLE switch.

d. Open the door assembly. At display board A501, set the PHASE and INSTRUCTION switches to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

4-179. The computer is now in the run mode executing the STA instruction and is locked into the execute phase. Using a dual-trace oscilloscope, check the signals shown in figure 4-33. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Note

Signal PNS is inhibited when the PHASE switch is in the LOOP position.

4-180. INTERRUPT PHASE. The following paragraphs provide a description and test procedure for the circuits used by the interrupt phase (phase 4). The processing operations are summarized in table 4-13. Point-to-point signal flow during phase 4 is shown in figure 4-34.

Note

If the PRESET indicator is on, the INTERRUPT PHASE is inoperative. The priority chain is broken by PRESET. Refer to paragraph 4-83 for a description of this indicator and related circuits.

4-181. Description. Any input/output device attached to the computer can interrupt the computers operation by requesting service by the computer. When an input/output device does request service, phase 4 is generated. At the end of the currently operating phase, phase 4 will be activated (exceptions to this are the JMP-I and JSB instructions). Phase 4 causes the P-register to be decremented by one and the select code of the interrupting device to be forced into the M-register forming the address of the next instruction. Phase 1 is then set and the computer is ready to process the instruction in the interrupt location. Phase 4 cannot occur again until phase 1 is complete (exceptions to this are the JMP-I instruction which must complete phase 1 and phase 2, and the JSB instruction which must complete two phase-one operations).

4-182. During times T1 through T5 of phase 4, the P-register number is read onto the R-bus (signal RPRB), complemented and transferred to the T-bus (signal CMF), stored back into the P-register (signal STP 0-15), read onto the R-bus again (signal RPRB), incremented and transferred to the T-bus (signals SBO and ADF), stored back into the P-register (signal STP 0-15), read for the third time onto the R-bus (signal $\overline{\text{RPRB}}$), complemented and transferred to the T-bus (signal $\overline{\text{CMF}}$), and stored in the P-register (signal STP 0-15). Thus the P-register is decremented by one.

4-183. During time T7 bits 6 through 15 of the M-register are cleared (signal RSM 6-15), the interrupt address is read directly onto the T-bus from the central interrupt register which is located on the I/O Address card (part no. 02116-6194), signals TB0 through TB5, and stored into the M-register (signal STM 0-5). Phase one is set and the computer is ready to process the instruction in the interrupt address.

4-184. Test Procedure. To test the interrupt phase circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly. The following test requires that an input/output device interface card be plugged into slot 203 of the computer.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 103100 (CLF-0 instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 102100 (STF-0 instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 102700 (STC-0 instruction) and press and release the LOAD MEMORY switch.

e. Set the SWITCH REGISTER to 102110 (STF-10 instruction) and press and release the LOAD MEMORY switch.

f. Set the SWITCH REGISTER to 102710 (STC-10 instruction) and press and release the LOAD MEMORY switch.

g. Set the SWITCH REGISTER to 102000 (HLT instruction) and press and release the LOAD MEMORY switch.

h. Set the SWITCH REGISTER to 000000 (NOP instruction) and press and release the LOAD MEMORY switch.

i. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

j. Set the SWITCH REGISTER to 000010 (interrupt location) and press and release the LOAD ADDRESS switch.

k. Set the SWITCH REGISTER to 002004 (INA instruction) and press and release the LOAD MEMORY switch.

l. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

m. Continuously press and release the RUN switch. The A-register will increment by one if the interrupt circuits are operating correctly.

Note

Refer to Volume Three of this manual for additional input/output section information.

Table 4-13. Interrupt Phase Processing Operations

TIME PERIODS	T0	T1	T2	T3	T4	T5	T6	T7
INTERRUPT 4		Read P to R Bus CMF Store T Bus in P		Read P to R Bus Read "1" to S Bus ADF Store T Bus in P		Read P to R Bus CMF Store T Bus in P		Reset M (6-15) Store T Bus (0-5) in M Set PH1

4-185. If the A-register does not increment by one, indicating the interrupt circuits are not operating properly, proceed as follows:

a. Set the SWITCH REGISTER to 001005 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 000000 (NOP instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Press and release the RUN switch.

4-186. The computer is now in the run mode continuously looping the program beginning at location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-34. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source. Set oscilloscope time/cm for 2 μs per division.

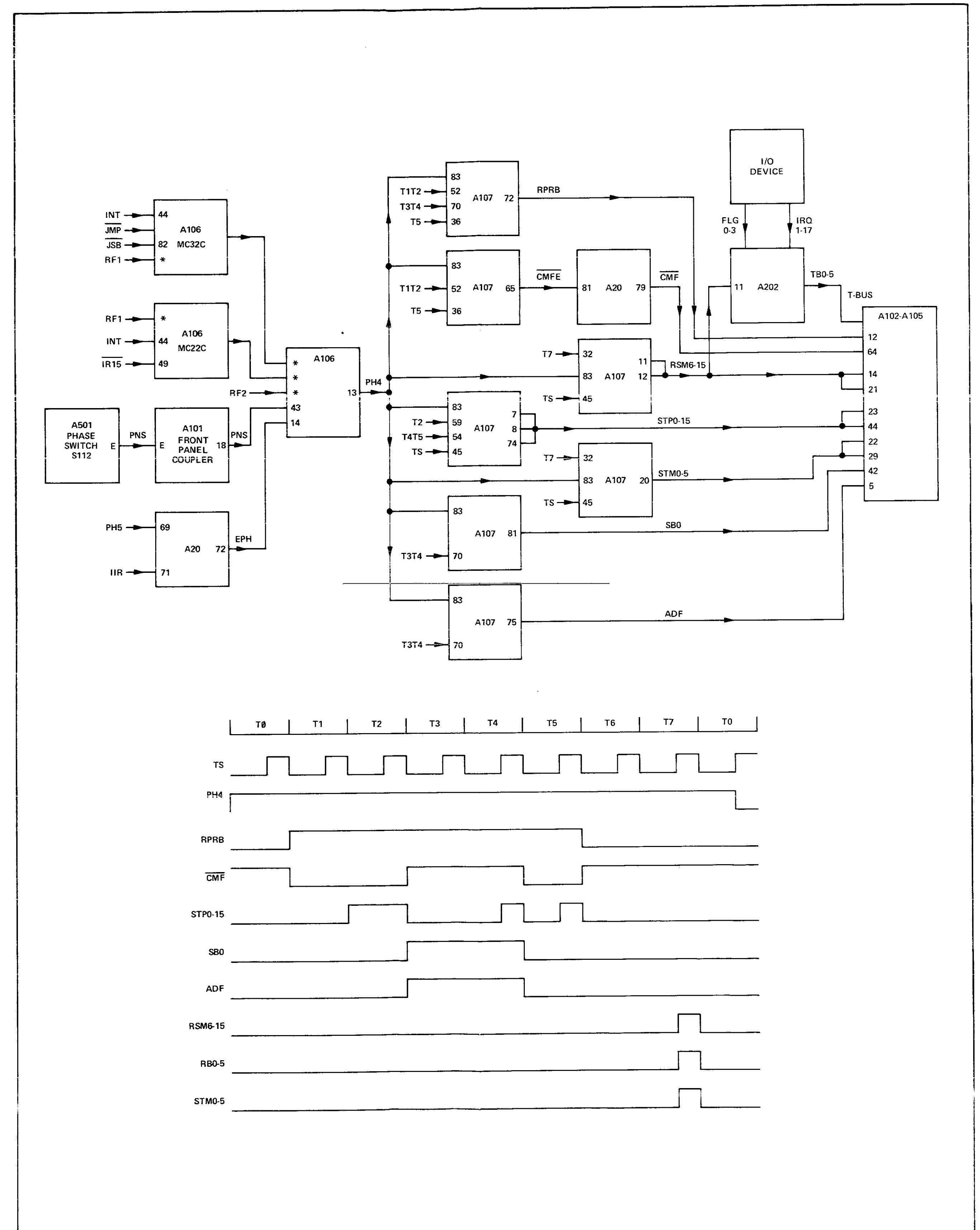

Figure 4-34. Interrupt Phase Circuit, Servicing Diagram

4-187. A- AND B- REGISTER ADDRESSING CIRCUITS.

4-188. The following paragraphs provide a description and test procedure for the circuits used in addressing the A- and B-registers. Point-to-point signal flow is shown in figure 4-35.

4-189. DESCRIPTION. Memory locations 000000 and 000001 are non-usable locations. Whenever these locations are addressed, the data in the A- or B-register is transferred to the T-register just as though the data was coming from memory.

4-190. At time T0 of every machine cycle the signals RMSB and $\overline{\text{EOF}}$ are generated by instruction decoder card A108. These signals are applied to arithmetic logic cards A102 through A105 and transfer the number contained in the M-register to the T-bus via the S-bus. The number on the T-bus is decoded by the TAN gates and the signals from these TAN gates are transferred to shift logic card A108 along with signals TB1, TB2, TB3, TB12, TB13, and TB14 from the T-bus. If the number in the M-register is 000000, the signal AAF will be generated at the end of time T0. If the number in the M-register is 000001, the signal BAF will be generated at the end of time T0. The signal AAF or BAF will remain true until the following time T0. AAF or BAF will cause signal RARB or RBRB to be generated and transfer the A- or B-register data onto the R-bus. The signal $\overline{\text{EOF}}$ is generated during times T0 and T1 and transfers the R-bus data to the T-bus. The signal STBT is generated during the end of time T1 and causes the T-bus data to be stored in the T-register. Either signal AAF or BAF will inhibit the signal MST and prevent data being read from memory into the T-register. Thus, when addressing locations 000000 or 000001, the data displayed in the T-register will come from either the A- or B-register and not from the addressed memory location.

4-191. TEST PROCEDURE. To test the AAF or BAF signal circuits, proceed as follows:

a. Set the SWITCH REGISTER to 000000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 010000 (AND instruction, A-register) or to 010001 (AND instruction, B-register) and press and release the LOAD A switch.

c. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

d. At the computer front panel, press and release the RUN switch.

4-192. The computer is now in the run mode executing the AND instruction and referencing either the A- or B-register. Using a dual-trace oscilloscope, check the signals shown in figure 4-35. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Note

Signal SBO is inhibited when the INSTRUCTION switch is in the LOOP position.

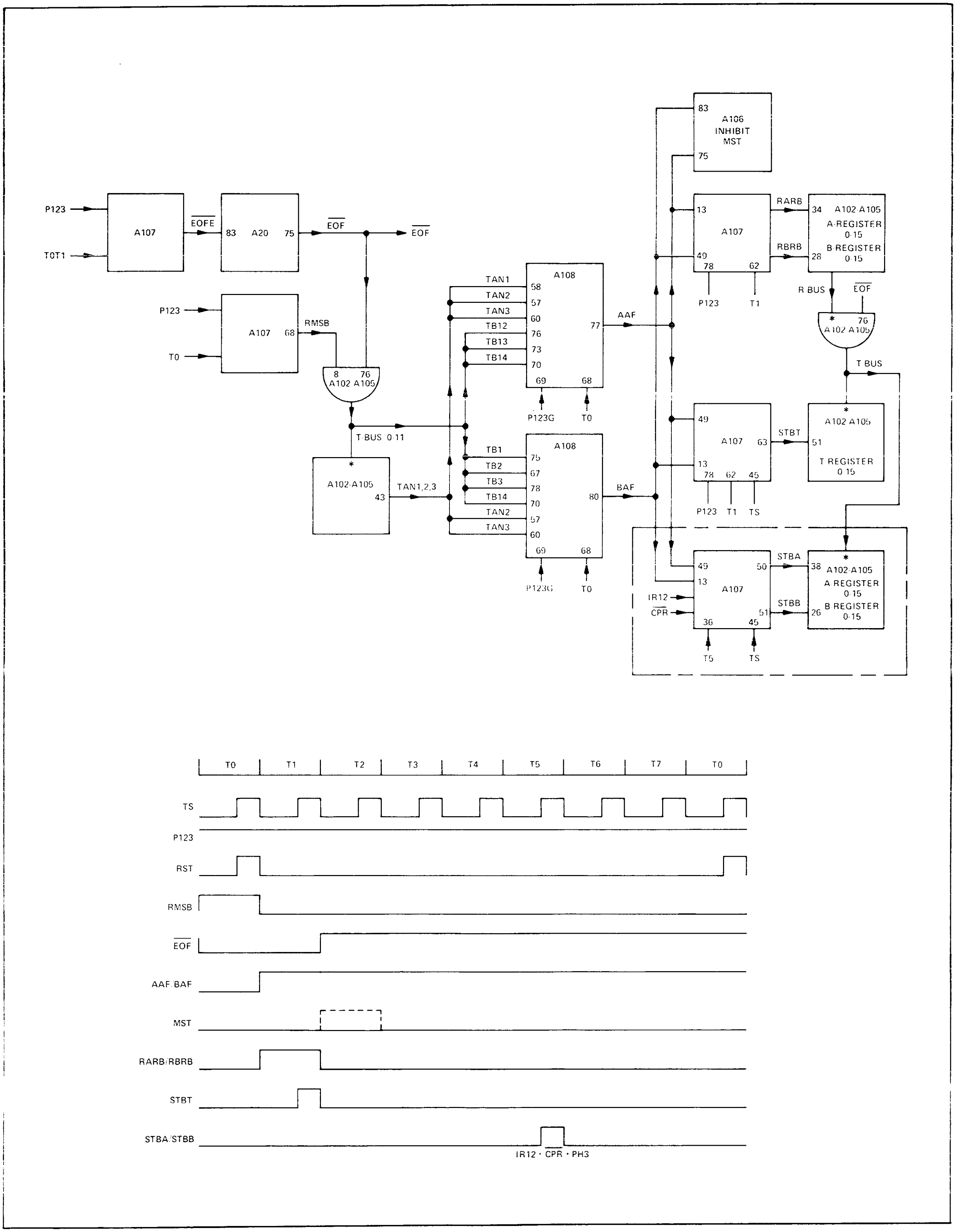

Figure 4-35. A- and B-Register Addressing Circuits, Servicing Diagram

4-193. MEMORY REFERENCE INSTRUCTION PROCESSING CIRCUITS.

4-194. The circuits that process the 14 memory reference instructions are shown in figures 4-36 through 4-45. Memory reference instructions are used in the computer program to address a selected memory location and specify a desired arithmetic or control operation involving the memory location which is addressed. The format for these instructions is shown in figure 4-1. The paragraphs which follow describe the purpose and use of each instruction and explain how the processing circuits implement and execute the instructions. Tables summarizing the processing operations, and servicing diagrams showing signal flow and timing within the processing circuits, are included for reference during explanation and troubleshooting. Suggested troubleshooting test procedures are presented for each instruction.

4-195. AND INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the AND instruction. Processing operations are summarized in table 4-14. Point-to-point signal flow during phase 3 is shown in figure 4-36. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-196. Description. The AND instruction is used to combine ("and") the data in the addressed memory location with data in the A-register. The result is stored in the A-register. The data in the addressed memory location remains unchanged, but the previous A-register data is destroyed. At the end of the processing cycle the P- and M-registers are incremented by one and the next phase is set.

4-197. The AND instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the data from the addressed memory location is read into the T-register. Bit configuration 0010 in the I-register causes signals RARB, RTSB, ANF, and STBA to be generated during time T3T4. These signals control the "anding" of the A- and T-register data, and store the result in the A-register at time T4TS.

4-198. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) cause the P-and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-199. Test Procedure. To test the AND instruction processing circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 013001 (AND instruction) and press the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press the RUN switch.

4-200. The computer is now in the run mode and executing the AND instruction continuously. Using a dual-trace oscilloscope, check the signals shown in figure 4-36. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SBO is inhibited when the INSTRUCTION switch is in the LOOP position. If all signals indicated above are correct, vary the data being "anded" and check for incorrect results. This will indicate a bad "and" gate on one of the Arithmetic Logic cards, A102 through A105.

Table 4-14. AND Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASES		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear IR	Clear TR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) If I: Set PH2 If D: Set PH3	
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
EXECUTE	3	Clear TR			Read A to R Bus Read TR to S Bus ANF Store T Bus in A			Read P to R Bus Read "1" to S Bus ADF Store T Bus in P, M Set next phase	

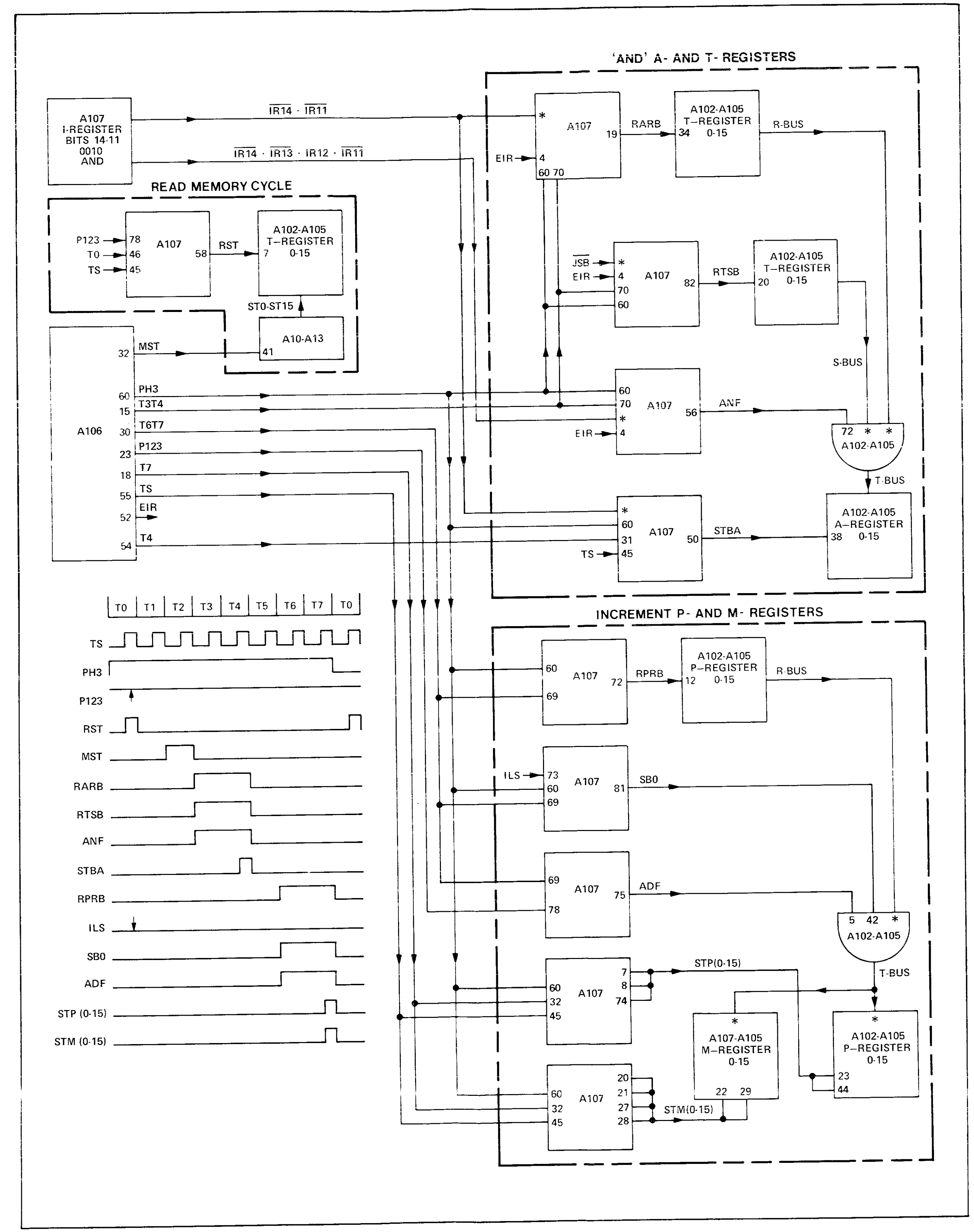

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Figure 4-36. AND Instruction Processing Circuits, Servicing Diagram

4-201. XOR INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the XOR instruction. Processing operations are summarized in table 4-15. Point-to-point signal flow during phase 3 is shown in figure 4-37. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-202. Description. The XOR instruction reads a number from memory, combines that number with another number from the A-register, and stores the resulting number in the A-register. The number in memory remains unchanged, but the previous number in the A-register is destroyed. At the end of the processing cycle the P- and M-registers are incremented by one and the next phase is set.

4-203. The XOR instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 0100 in the I-register causes signals RTSB, RARB, $\overline{\text{EOF}}$, and STBA to be generated during time T3T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), and the number in the A-register to the R-bus (signal RARB), combine these numbers (signal $\overline{\text{EOF}}$), and read the result back into the A-register via the T-bus (signal STBA).

4-204. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-205. Test Procedure. To test the XOR instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 023001 (XOR instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the RUN switch.

4-206. The computer is now in the run mode executing the XOR instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-37. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SBO is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-15. XOR Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6 T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) If I: Set PH2 If D: Set PH3
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3
EXECUTE	3	Clear TR			EOF A, TR to A			P + 1 to P, M Set next phase

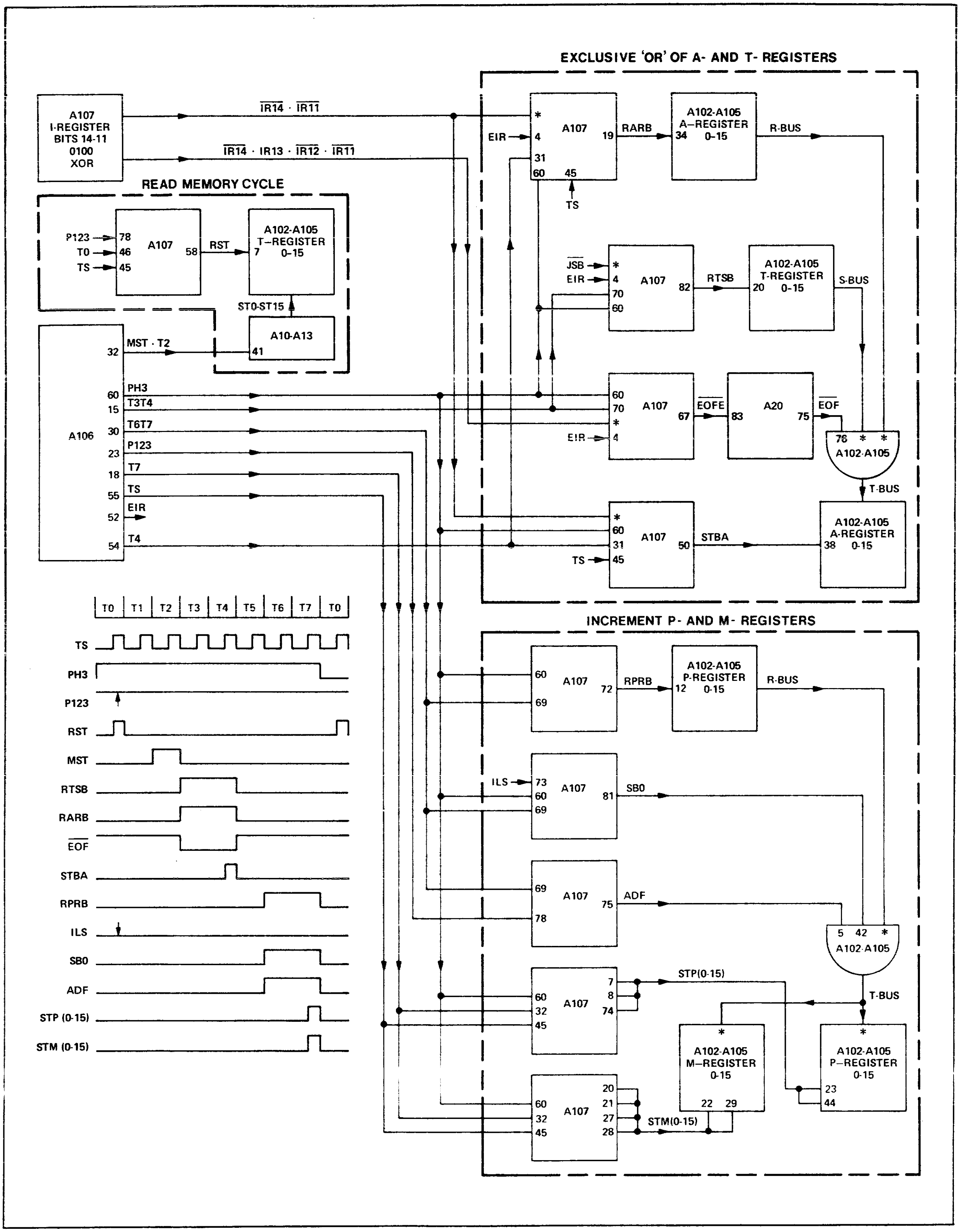

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Figure 4-37. XOR Instruction Processing Circuits, Servicing Diagram

4-207. IOR INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the IOR instruction. Processing operations are summarized in table 4-16. Point-to-point signal flow during phase 3 is shown in figure 4-38. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-208. Description. The IOR instruction reads a number from memory, combines that number with another number from the A-register, and stores the resulting number in the A-register. The number in memory remains unchanged, but the previous number in the A-register is destroyed. At the end of the processing cycle the P- and M-registers are incremented by one and the next phase is set.

4-209. The IOR instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 0110 in the I-register causes signals RTSB, RARB, IOF, and STBA to be generated during time T3T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), and the number in the A-register to the R-bus (signal RARB), combine these numbers (signal $\overline{\text{IOF}}$), and read the result back into the A-register via the T-bus (signal STBA).

4-210. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-211. Test Procedure. To test the IOR instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 033001 (IOR instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the RUN switch.

4-212. The computer is now in the run mode executing the IOR instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-38. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SBO is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-16. IOR Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) If I: Set PH2 If D: Set PH3	
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
EXECUTE	3	Clear TR			IOF A, TR to A			P + 1 to P, M Set next phase	

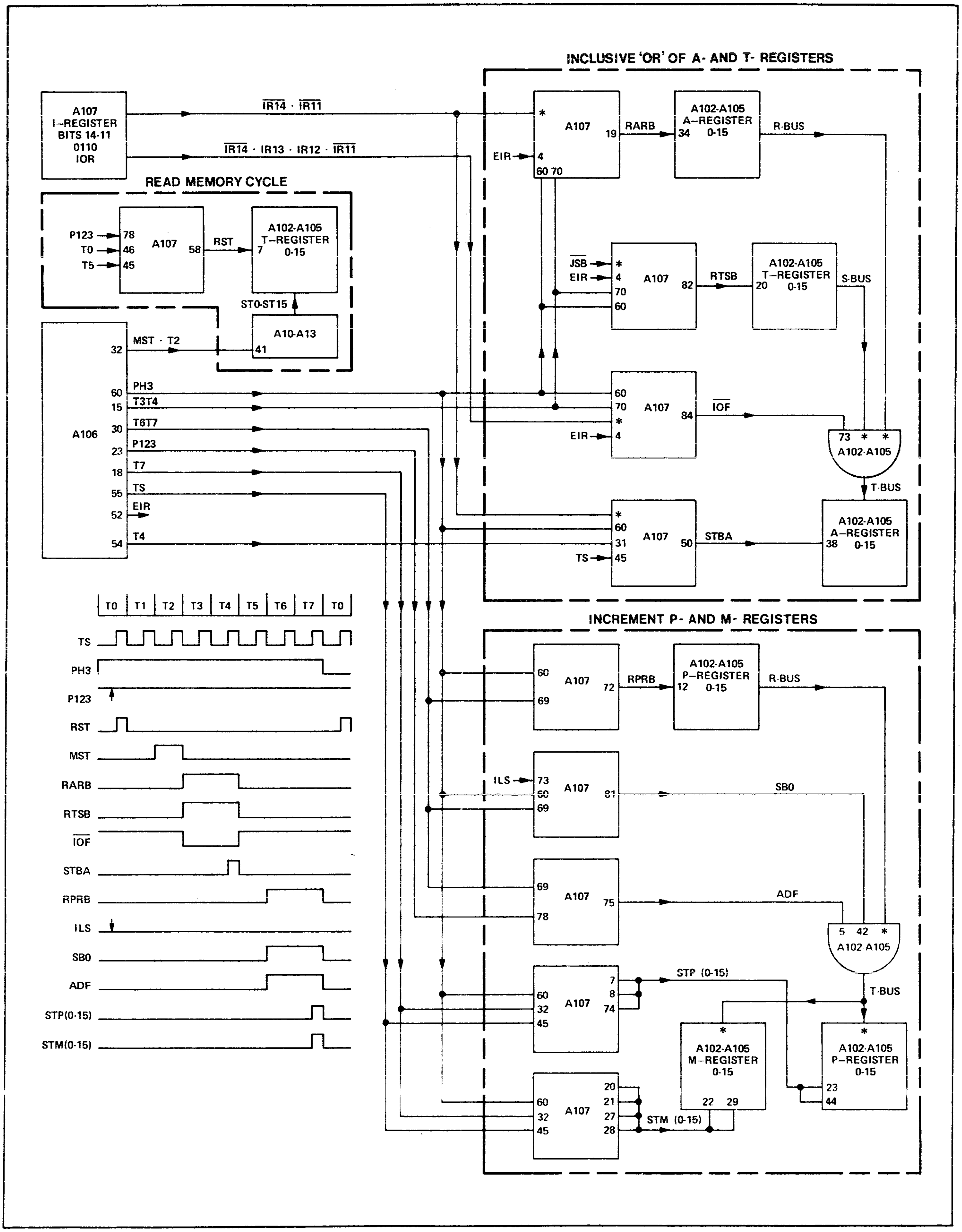

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Figure 4-38. IOR Instruction Processing Circuits, Servicing Diagram

4-213. JSB INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the JSB instruction. Processing operations are summarized in table 4-17. Point-to-point signal flow during phase 3 is shown in figure 4-39. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-214. Description. The JSB instruction inhibits the read-memory cycle, reads the P-register number onto the R-bus, increments it by one, and stores the resulting number in the addressed memory location. The instruction then reads the M-register number onto the S-bus, and stores this number in the P-register. At the end of the processing cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-215. The JSB instruction is read from memory during phase 1 and executed during phase 3. Bit configuration 0011 in the I-register causes signals JSB, RPRB, SBO, ADF, and STBT to be generated. The read-memory cycle during phase 3 of this instruction is inhibited (signal JSB). During times T1 and T2 of phase 3 the number in the P-register is read onto the R-bus (signal RPRB), incremented by one (signals SBO and ADF), and stored in the T-register via the T-bus (signal STBT). The T-register number is then written into the addressed memory location during the write-memory cycle.

4-216. During times T3 and T4 signals RMSB, $\overline{EOF}$, and STP(0-15) cause the number in the M-register (address portion of the JSB instruction) to be read onto the S-bus (signal RMSB), transferred to the T-bus (signal $\overline{EOF}$), and stored in the P-register by signal STP(0-15).

4-217. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-218. Test Procedure. To test the JSB instruction circuits, proceed as follows:

Note

If addresses other than 001001 and 001005 are used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch. Then, press and release the LOAD MEMORY switch ten times (This sets locations 001000 through 001012 to 001000).

b. Set the SWITCH REGISTER to 001001 and press and release the LOAD ADDRESS switch.

c. Set the SWITCH REGISTER to 017004 (JSB instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001005 and press and release the LOAD ADDRESS switch.

e. Set the SWITCH REGISTER to 017000 (JSB instruction) and press and release the LOAD MEMORY switch.

f. Set the SWITCH REGISTER to 001001 and press and release the LOAD ADDRESS switch.

g. Press and release the SINGLE CYCLE switch twice. Location 001004 should contain 001002, and the P- and M-registers should contain 001005.

h. Repeat step g above. Location 001000 should contain 001006, and the P- and M-registers should contain 001001.

Table 4-17. JSB Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) If I: Set PH2 If D: Set PH3	
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
EXECUTE	3	Clear TR Inhibit Mem. Data	P + 1 to TR		M to P			P + 1 to P, M Set next phase	

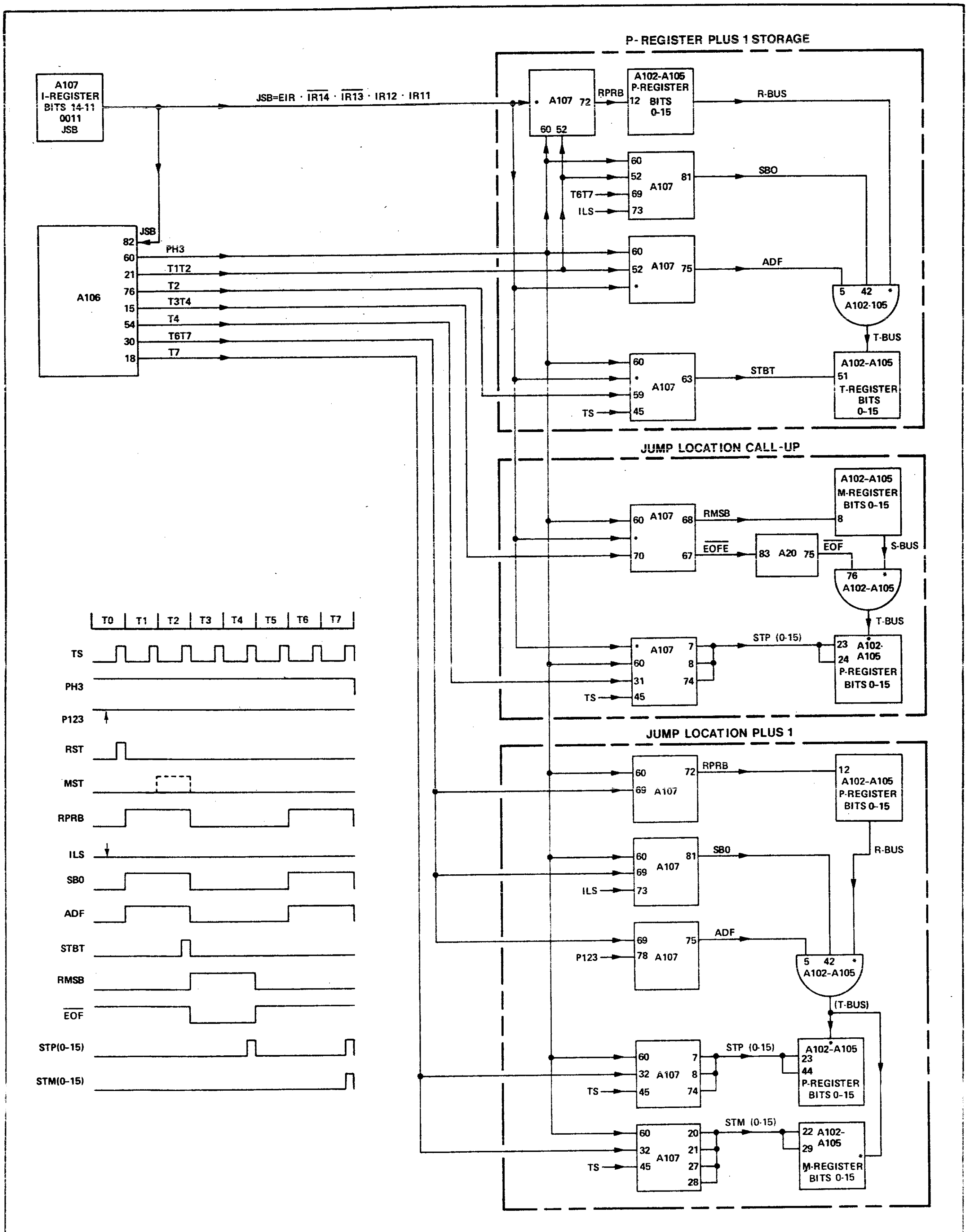

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Figure 4-39. JSB Instruction Processing Circuits, Servicing Diagram

i. At the computer front panel, press and release the RUN switch.

4-219. The computer is now in the run mode executing the JSB instructions in locations 001001 and 001005. Using a dual-trace oscilloscope, check the signals shown in figure 4-39. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

4-220. JMP INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the JMP instruction. Processing operations are summarized in table 4-18. Point-to-point signal flow during phase 1 is shown in figure 4-40. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-221. Description. The JMP instruction causes the address portion of the instruction (bits 0 through 9) to be transferred to the P- and M- registers. The next phase is then set.

4-222. The JMP instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction is read from memory to the T-register and bits 10 through 15 of the T-register are transferred to the I-register. Bit configuration 0101 0/1 in the I-register causes signals $\overline{\text{OP0}}$, JMP, and $\overline{\text{IR10}}$ or IR10 to be generated during times T0 through T3. These signals cause the signals RTSB, ADF, STP(0-15), RSM(10-15), and STM(0-9) to be generated during times T5 through T7.

4-223. During times T5 through T7 signal STP(10-15) causes P-register bits 10 through 15 to be set to zeros if signal $\overline{\text{IR10}}$ is true. If $\overline{\text{IR10}}$ is false, signal STP(10-15) will not be generated. Signal RTSB causes the T-register number to be read onto the S-bus. Signal ADF transfers the S-bus number to the T-bus. Signal STM(0-9) causes bits 0 through 9 of the T-bus to be stored in the M-register. Signal RSM(10-15) causes bits 10 through 15 of the M-register to be set to zeros if signal $\overline{\text{IR10}}$ is true. If $\overline{\text{IR10}}$ is false, signal RSM(10-15) will not be generated. The next phase (phase 1, phase 2, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-224. Test Procedure. To test the JMP instruction circuits, proceed as follows:

Note

If addresses other than 001000 and 001001 are used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 027001 (JMP instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Press and release the SINGLE CYCLE switch once. The P- and M-registers should contain 001001.

f. Repeat step e above. The P- and M-registers should now contain 001000.

g. At the computer front panel, press and release the RUN switch.

4-225. The computer is now in the run mode executing the JMP instructions in locations 001000 and 001001. Using a dual-trace oscilloscope, check the signals shown in figure 4-40. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Table 4-18. JMP Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH (JMP)	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)			If Z: 0 to P	If Z: 0 to M (10-15) If D: TR to P, M (0-9) and set next phase If I: TR to M (0-9) and set PH2	

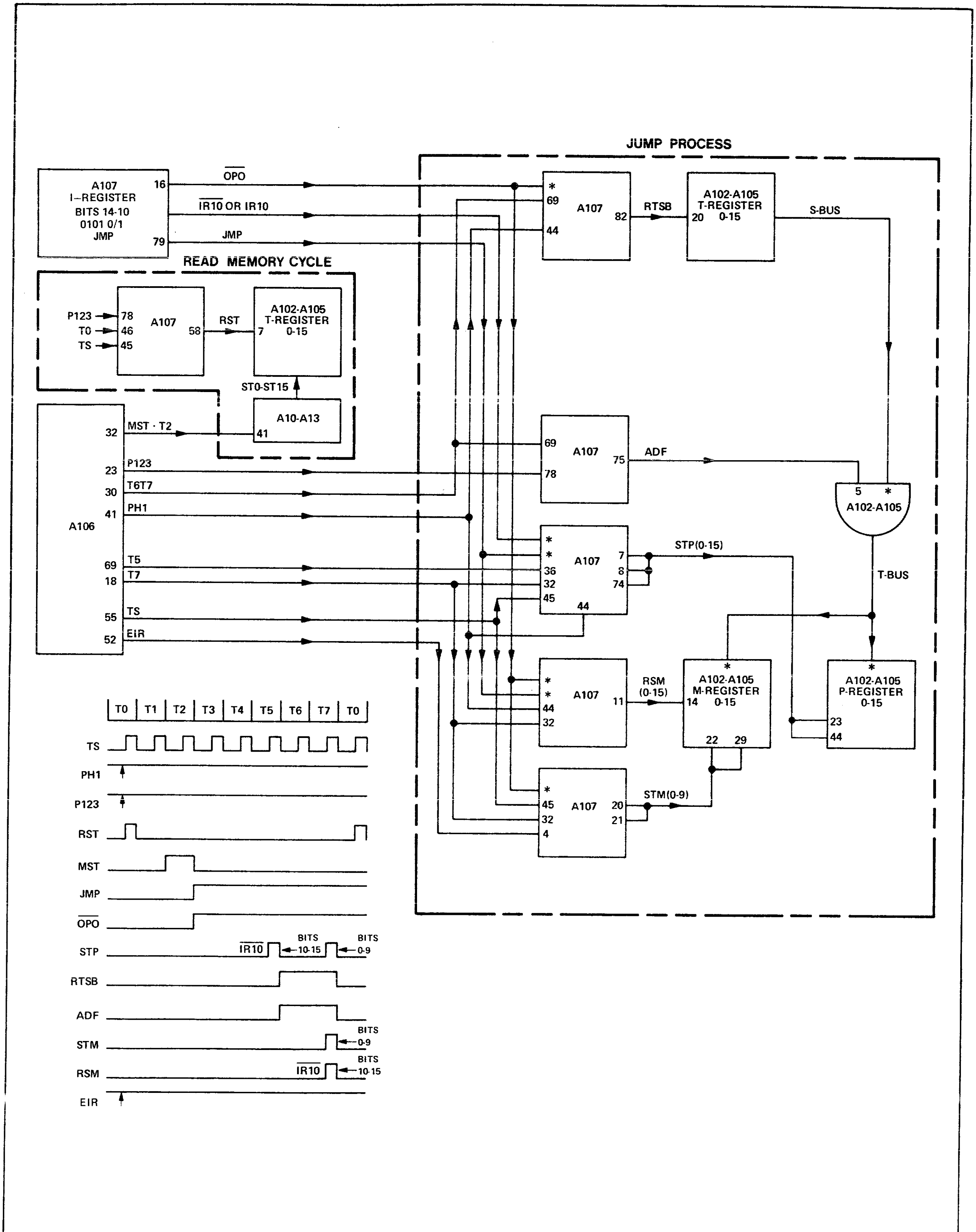

Figure 4-40. JMP Instruction Processing Circuits, Servicing Diagram

4-226. ISZ INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the ISZ instruction. Processing operations are summarized in table 4-19. Point-to-point signal flow during phase 3 is shown in figure 4-41. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-227. Description. The ISZ instruction reads a number from memory, increments the number by one, and stores the incremented number in its original location. If, after being incremented, the number is not zero, the program continues with the next instruction in sequence. If, however, the number is zero after being incremented, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one).

4-228. The ISZ instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 0111 in the I-register causes signals RTSB, RB0, ADF, and STBT to be generated during times T3 through T5. These signals transfer the number in the T-register to the S-bus (signal RTSB), increment the number by one (signals RB0 and ADF), and read it back into the T-register via the T-bus (signal STBT). Signal C16 is generated during times T3 through T5 if the incremented number equals zero. Signal C16 sets the Carry FF (CFF) at time T4TS. Signal CFF causes C0 to be generated at time T6T7.

4-229. Two additional time periods (0.4 μsec) are generated between time periods T5 and T6 to allow the incremented number in the T-register to be written back into the addressed memory location. Refer to paragraph 4-160 for a description of memory timing for the ISZ instruction.

4-230. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-231. Test Procedure. To test the ISZ instruction circuits, proceed as follows:

Note

If a starting address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 (starting address) and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 037003 (ISZ instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch twice.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD MEMORY switch. (This initializes the number in the memory location addressed by the ISZ instruction.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. At the computer front panel, press and release the RUN switch.

4-232. The computer is now in the run mode executing the ISZ instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-41. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-19. ISZ Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)		WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) If I: Set PH2 If D: Set PH3	
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
EXECUTE	3	Clear TR			TR + 1 to TR If C16: Set Carry Inhibit Write		Write (Add 0.4 μ Sec)	P + 1 + Carry to P, M Set next phase	

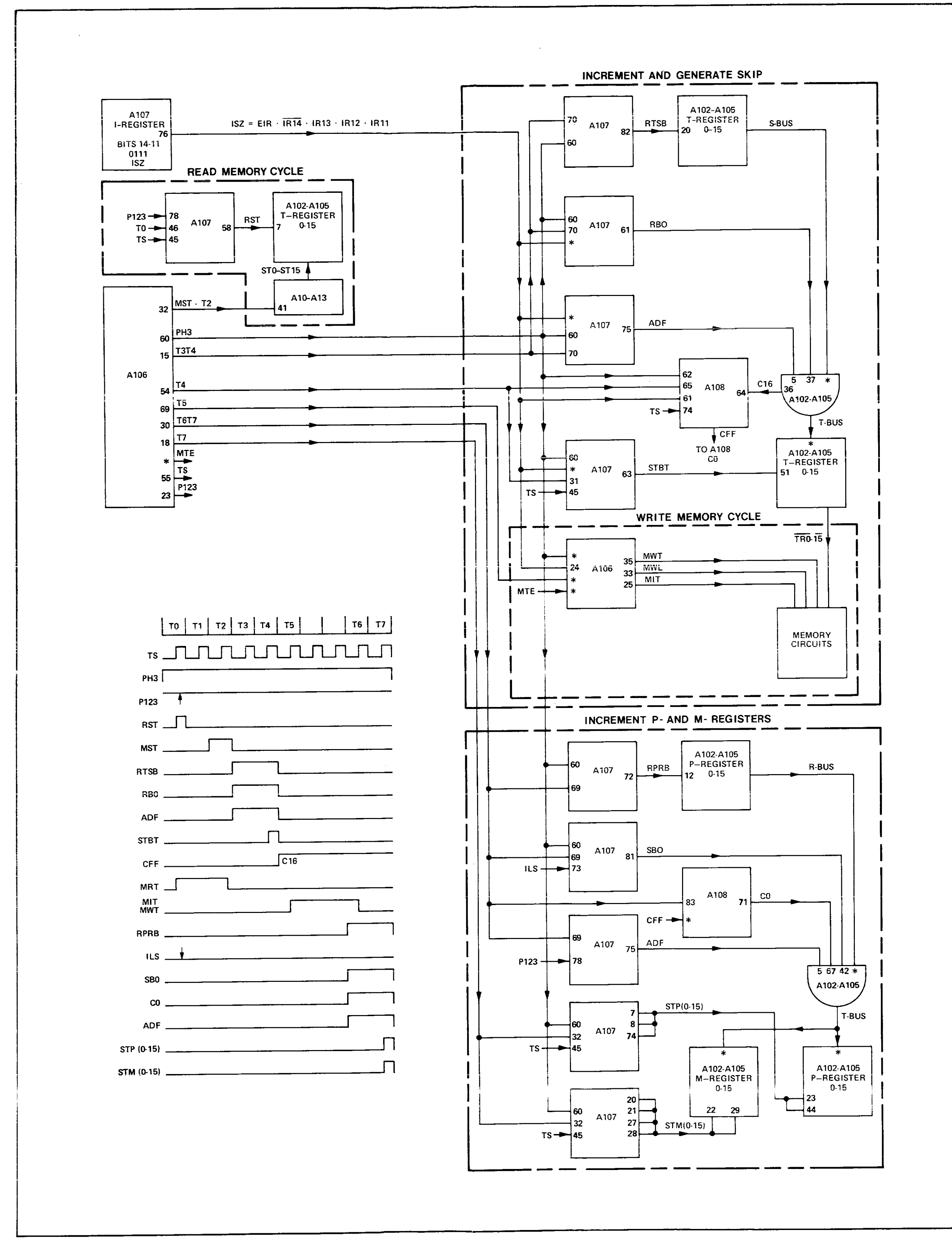

Figure 4-41. ISZ Instruction Processing Circuits, Servicing Diagram

4-233. ADA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the ADA/B instruction. Processing operations are summarized in table 4-20. Point-to-point signal flow during phase 3 is shown in figure 4-42. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-234. Description. The ADA/B instruction reads a number from memory, adds that number to another number from the A- or B-register, and stores the resulting number in the A- or B-register. The number in memory remains unchanged, but the previous number in the A- or B-register is destroyed. The result of the addition may set the Extend or Overflow registers. At the end of the machine cycle the P- and M-registers are incremented by one and the next phase is set.

4-235. The ADA/B instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 1000 or 1001 in the I-register causes signals ADD, RTSB, RARB or RBRB, ADF, and STBA or STBB to be generated during times T3 through T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), and the number in the A- or B-register to the R-bus (signal RARB or RBRB), add these numbers together (signal ADF), and read the result back into the A- or B-register via the T-bus (signal STBA or STBB).

4-236. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-237. Test Procedure. To test the ADA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 043001 (ADA instruction) or 047001 (ADB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 052525 and press and release the LOAD A switch, if testing the ADA instruction, or the LOAD B switch if testing the ADB instruction.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch twice. The A-register should now contain 125252.

h. At the computer front panel, press and release the RUN switch.

4-238. The computer is now in the run mode executing the ADA or ADB instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-42. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-20. ADA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) If I: Set PH2 If D: Set PH3	
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
EXECUTE	3	Clear TR			If A: ADF A, TR to A IF B: ADF B, TR to B If C16: Set E			P + 1 to P, M Set next phase	

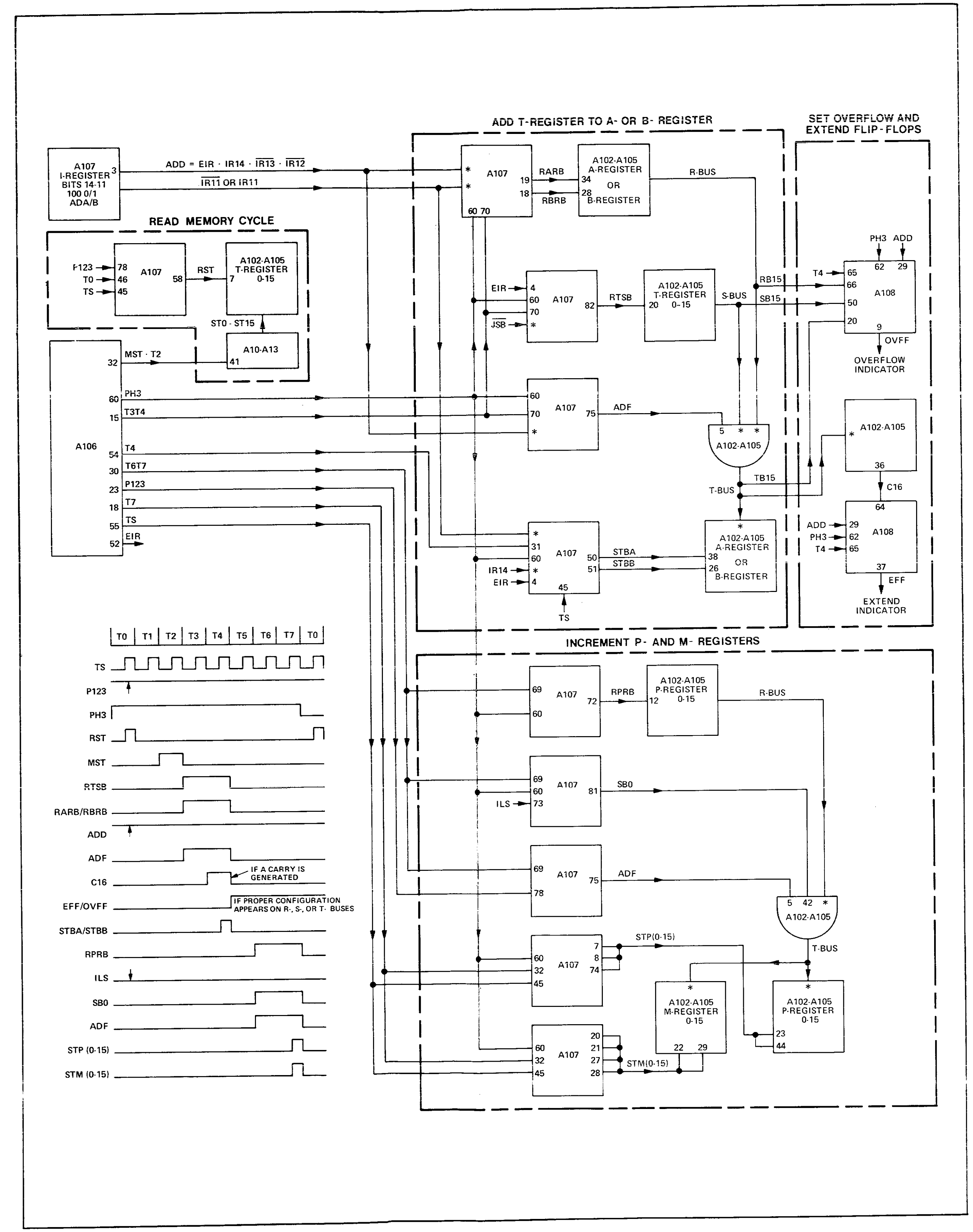

Figure 4-42. ADA/B Instruction Processing Circuits, Servicing Diagram

4-239. CPA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CPA/B instruction. Processing operations are summarized in table 4-21. Point-to-point signal flow during phase 3 is shown in figure 4-43. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-240. Description. The CPA/B instruction reads a number from memory, compares that number with another number from the A- or B-register. If the compare is unequal the Carry FF is set which causes signal C0 to be generated. The numbers in memory and the A- or B-register remain unchanged. At the end of the machine cycle the P- and M-registers are incremented by one or by two if signal C0 is generated and the next phase is set.

4-241. The CPA/B instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 1010 or 1011 in the I-register causes signals RTSB, RARB or RBRB, and $\overline{EOF}$ to be generated during times T3 through T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), transfer the number in the A- or B-register to the R-bus (signal RARB or RBRB), combine these numbers and transfer the resultant number to the T-bus (signal $\overline{EOF}$), and check the T-bus for zero via the TAN gates. If the T-bus is not zero (S-bus and R-bus are unequal), the Carry FF will be set at the end of time T4TS and cause signal C0 to be generated during time T6T7.

4-242. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-243. Test Procedure. To test the CPA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 053003 (CPA instruction) or 057003 (CPB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the CPA instruction, or the LOAD B switch if testing the CPB instruction.

e. Set the SWITCH REGISTER to 001003 and press and release the LOAD ADDRESS switch.

f. Set the SWITCH REGISTER to 077777 (for unequal compare) or to 000000 (for equal compare) and press and release the LOAD MEMORY switch.

g. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

h. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

i. At the computer front panel, press and release the SINGLE CYCLE switch twice. The P- and M-registers should increment by one and contain 01001 if using an unequal compare, or 01000 if using an equal compare.

j. At the computer front panel, press and release the RUN switch.

2-244. The computer is now in the run mode executing the CPA or CPB instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-43. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-21. CPA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)		WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) If I: Set PH2 If D: Set PH3	
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
EXECUTE	3	Clear TR			If A: EOF A, TR to T Bus If B: EOF B, TR to T Bus If T Bus not zero, set Carry			P + 1 + Carry to P, M Set next phase	

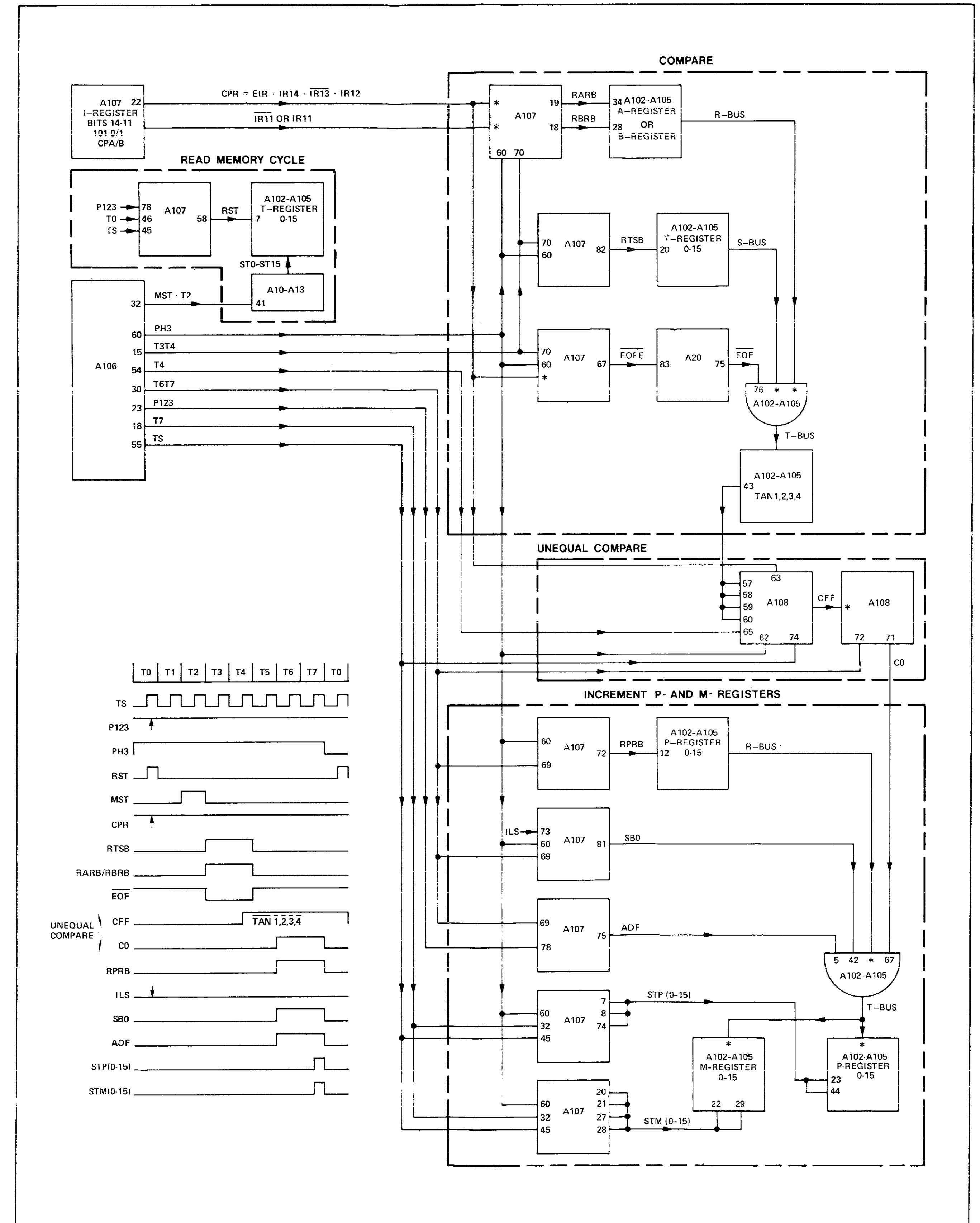

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Figure 4-43. CPA/B Instruction Processing Circuits, Servicing Diagram

4-245. LDA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the LDA/B instruction. Processing operations are summarized in table 4-22. Point-to-point signal flow during phase 3 is shown in figure 4-44. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-246. Description. The LDA/B instruction reads a number from memory, transfers and stores that number in the A- or B- register. The number in memory remains unchanged, but the previous number in the A- or B-register is destroyed. At the end of the machine cycle the P- and M-registers are incremented by one and the next phase is set.

4-247. The LDA/B instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 1100 or 1101 in the I-register causes signals LOD, RTSB, $\overline{\text{EOF}}$, and STBA or STBB to be generated during times T3 through T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), then to the T-bus (signal $\overline{\text{EOF}}$), and store it in the A- or B-register (signal STBA or STBB).

4-248. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-249. Test Procedure. To test the LDA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 063001 (LDA instruction) or 067001 (LDB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the LDA instruction, or the LOAD B switch if testing the LDB instruction.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch twice. The A-register should now contain 052525.

h. At the computer front panel, press and release the RUN switch.

4-250. The computer is now in the run mode executing the LDA or LDB instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-44. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-22. LDA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)		WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) If I: Set PH2 If D: Set PH3	
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
EXECUTE	3	Clear TR			If A: TR to A If B:TR to B			P + 1 to P, M Set next phase	

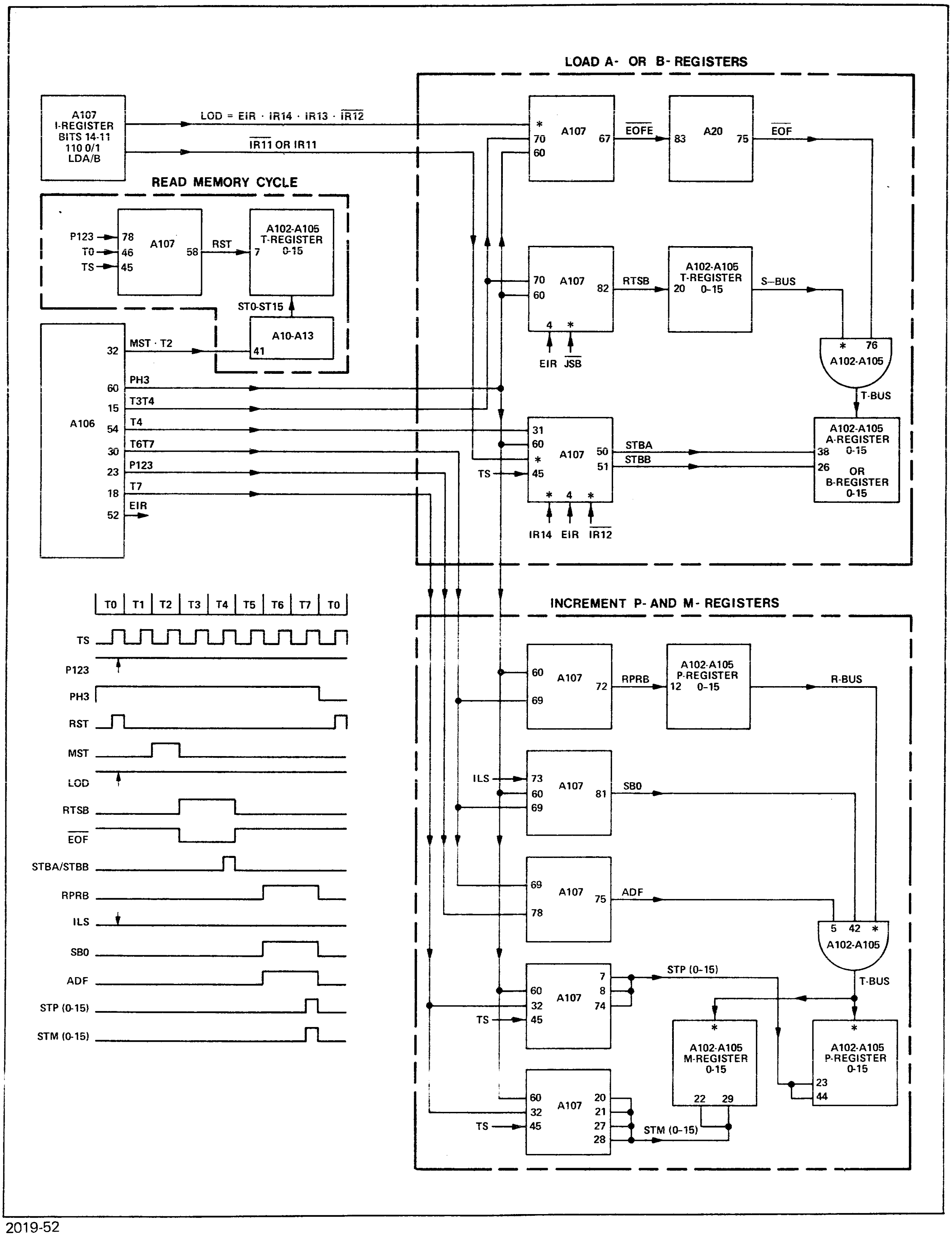

Figure 4-44. LDA/B Instruction Processing Circuits, Servicing Diagram

4-251. STA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the STA/B instruction. Processing operations are summarized in table 4-23. Point-to-point signal flow during phase 3 is shown in figure 4-45. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-252. Description. The STA/B instruction reads a number from the A- or B-register, and stores the resulting number in the addressed memory location. The number in the A- or B-register remains unchanged, but the previous number in the addressed memory location is destroyed. At the end of the machine cycle the P- and M-registers are incremented by one and the next phase is set.

4-253. The STA/B instruction is read from memory during phase 1 and executed during phase 3. During times T1 and T2 of phase 3 the number in the A- or B-register is read into the T-register. Bit configuration 1110 or 1111 in the I-register causes signals RARB, or RBRB, $\overline{EOF}$, and STBT to be generated during times T1 and T2. These signals transfer the number in the A- or B-register to the R-bus (signal RARB or RBRB), then to the T-bus (signal $\overline{EOF}$), and store it in the T-register (signal STBT). The number is then written into the addressed memory location during the write-memory cycle.

4-254. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-255. Test Procedure. To test the STA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 073001 (STA instruction) or 077001 (STB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the STA instruction, or the LOAD B switch if testing the STB instruction.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch twice. Location 001001 should now contain 000000.

h. At the computer front panel, press and release the RUN switch.

4-256. The computer is now in the run mode executing the STA or STB instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-45. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-23. STA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) If I: Set PH2 If D: Set PH3	
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
EXECUTE	3	Clear TR Inhibit Mem. Data	If A: A to TR If B: B to TR					P + 1 to P, M Set next phase	

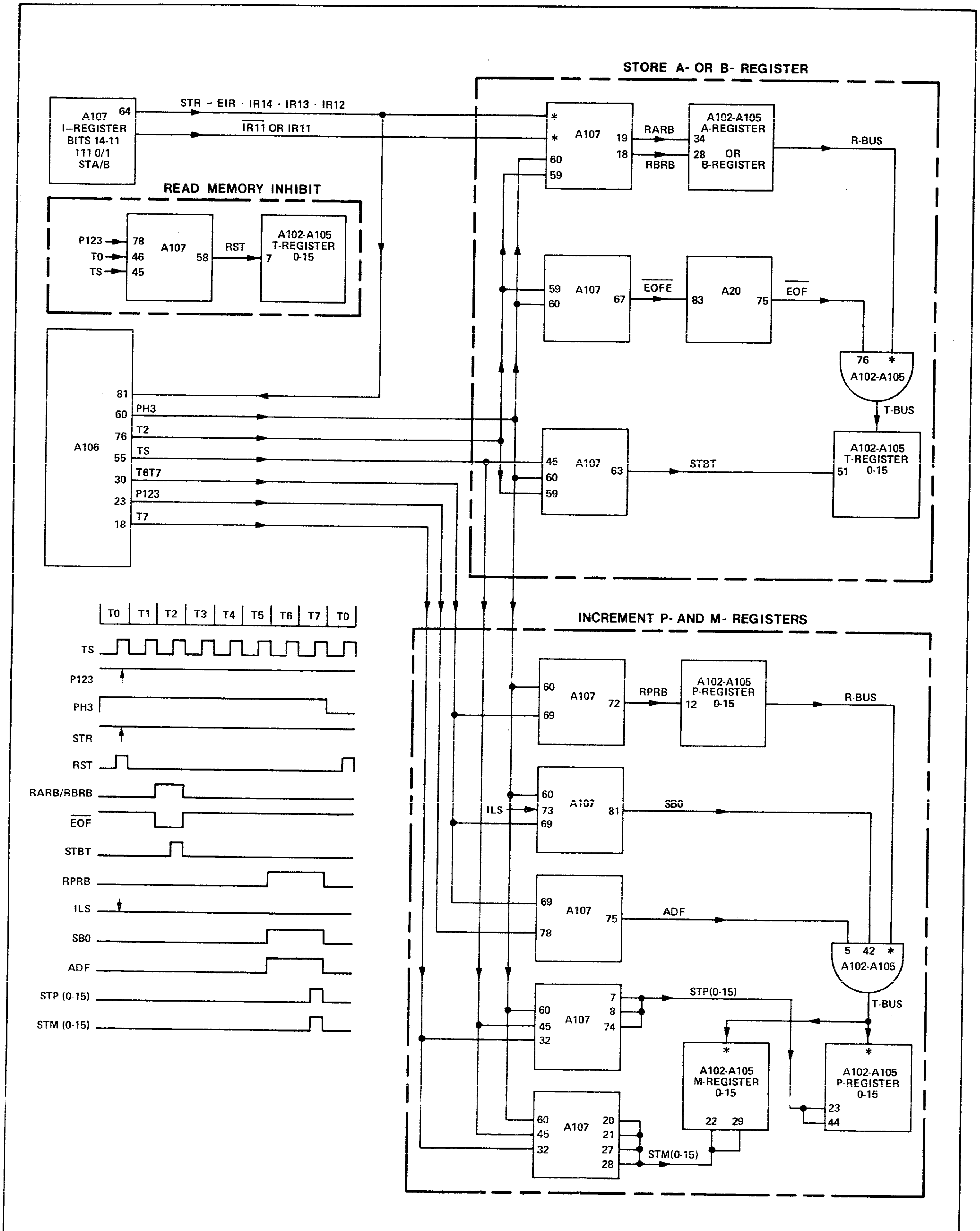

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Figure 4-45. STA/B Instruction Processing Circuits, Servicing Diagram

4-257. REGISTER REFERENCE INSTRUCTION PROCESSING CIRCUITS.

4-258. The circuits that process the 39 register reference instructions are shown in figure 4-46 through 4-67. Register reference instructions are used in the computer program to address a selected data register and specify a desired arithmetic or control operation involving the register which is addressed. The format for these instructions is shown in figure 4-1. The paragraphs which follow describe the purpose and use of each instruction and explain how the processing circuits implement and execute the instructions. Tables summarizing the processing operations, and servicing diagrams showing signal flow and timing within the processing circuits, are included for reference during explanation and troubleshooting. Suggested troubleshooting test procedures are presented for each instruction.

Note

Shift or rotate instructions can be processed during times T3 and T5 of the same machine cycle. Only time T3 processing is illustrated in the figures and explained in the text of these instructions. Time T5 processing uses identical signals between the various circuit cards. However, both processes should be checked as circuit structure varies within the circuit cards.

4-259. NOP INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the NOP instruction. Processing operations are summarized in table 4-24. Point-to-point signal flow during phase 1 is shown in figure 4-46.

4-260. Description. The NOP instruction provides a one machine cycle (1.6 μsec) program delay. At the end of the machine cycle the P- and M-registers are incremented by one and the next phase is set.

4-261. The NOP instruction is read from memory and executed during phase 1. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-262. Test Procedure. To test the NOP instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 000000 and press and release the LOAD A switch and LOAD B switch.

b. Open the door assembly. At display board assembly A501, set the MEMORY switch to the OFF position.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

4-263. The computer is now in the run mode executing the NOP instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-46. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Table 4-24. NOP Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) Set next phase	

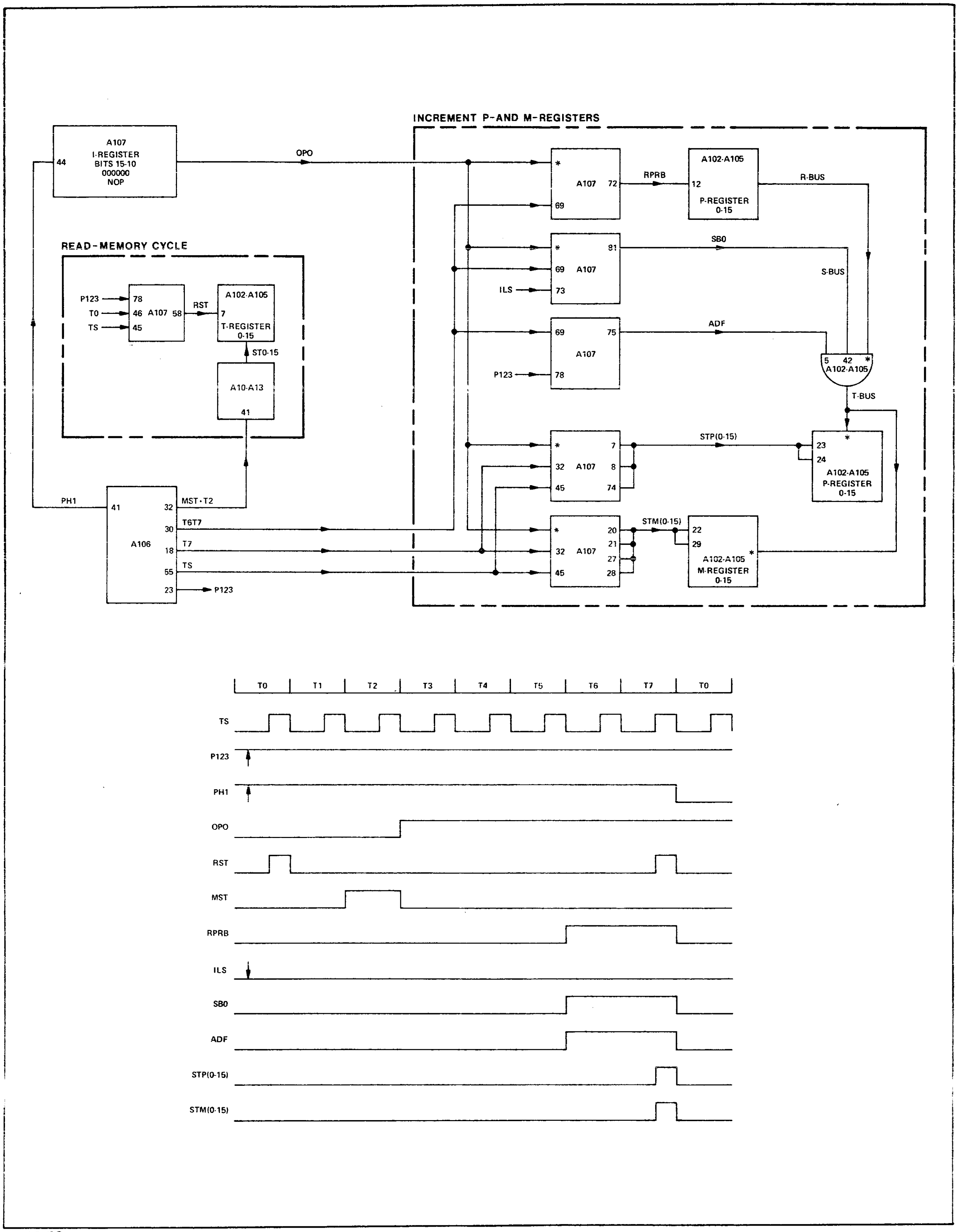

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Figure 4-46. NOP Instruction Processing Circuits, Servicing Diagram

4-264. CLE INSTRUCTION (Shift-Rotate Group). The following paragraphs provide a description and test procedure for the circuits that process the CLE instruction. Processing operations are summarized in table 4-25. Point-to-point signal flow during phase 1 is shown in figure 4-47.

4-265. Description. The CLE instruction resets the Extend register (E-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 in the I-register causes signals SRG, OPO, and RARB to be generated during times T3 and T4. These signals in combination with signal TR5 from the T-register cause the E-register to reset at time T4TS. The A-register data is read onto the R-bus (signal RARB) during times T3 through T5 but is not used.

4-266. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-267. Test Procedure. To test the CLE instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 000040 (CLE instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

4-268. The computer is now in the run mode executing the CLE instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-47. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-25. CLE Instruction (Shift Rotate Group) Processing Operations

TIME PERIODS	T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)		WRITE (TR to Mem)				
FETCH 1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS				T3 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B Reset E Flip-flop	T4 Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	T5 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		

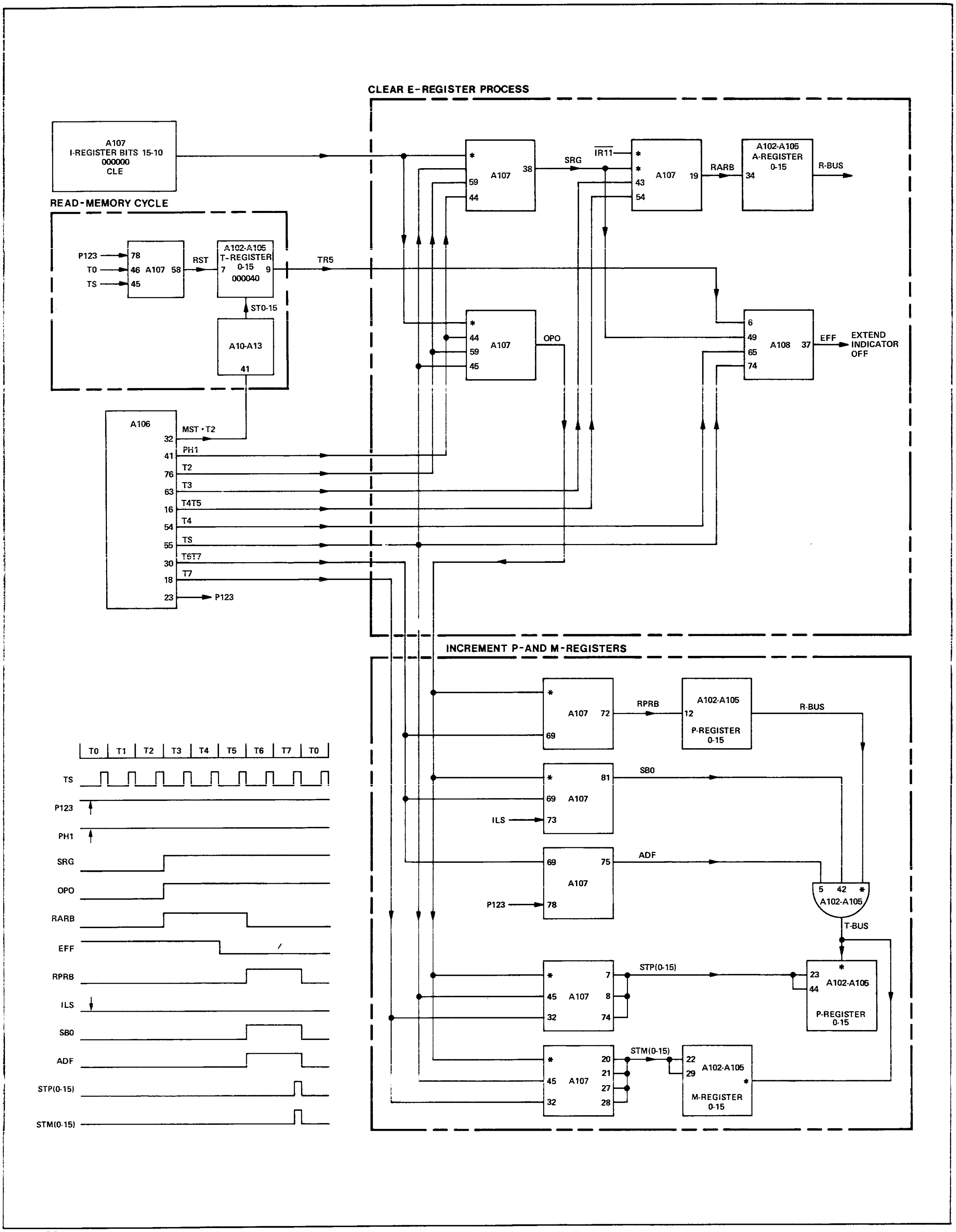

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Figure 4-47. CLE Instruction (Shift-Rotate Group) Processing Circuits, Servicing Diagram

4-269. SLA/B INSTRUCTION (Shift-Rotate Group). The following paragraphs provide a description and test procedure for the circuits that process the SLA/B instruction. Processing operations are summarized in table 4-26. Point-to-point signal flow during phase 1 is shown in figure 4-48.

4-270. Description. The SLA/B instruction reads a number from the A- or B-register and compares bit zero of the A- or B-register (RBO) with bit zero of the T-register (TRO). If the comparison is equal, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If the comparison is unequal, the program continues with the next instruction is sequence.

4-271. The SLA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during times T3 and T4. These signals in combination with signal TR3 from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), and the Carry FF (CFF) to set at time T4TS if bit zero of the R-bus and bit zero of the T-register are equal. Signal CFF causes signal CO to be generated at time T6T7.

4-272. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal CO will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-273. Test Procedure. To test the SLA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001010 (SLA instruction) or to 004010 (SLB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 (equal compare and press and release the LOAD A switch if testing the SLA instruction, or the LOAD B switch if testing the SLB instruction.) (Substitute 000001 to 000000 for an unequal compare.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001001 in them.

h. Repeat step g above. The P- and M-registers should have 001000 in them.

i. At the computer front panel, press and release the RUN switch.

4-274. The computer is now in the run mode executing the SLA or SLB instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-48. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal TO at A106-TP1, and use channel B as the triggering source.

Note

Signal SBO is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-26. SLA/B Instruction (Shift Rotate Group) Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	*Execute			P + 1 + Carry to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS		T3 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B			T4 Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry Read A/B to R Bus Set Carry if RB0 = 0 and TR0 = 0, or RB0 = 1 and TR0 = 1		T5 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		

*Combination of SSA/B, SLA/B, and RSS is a special case; see paragraph 4-384.

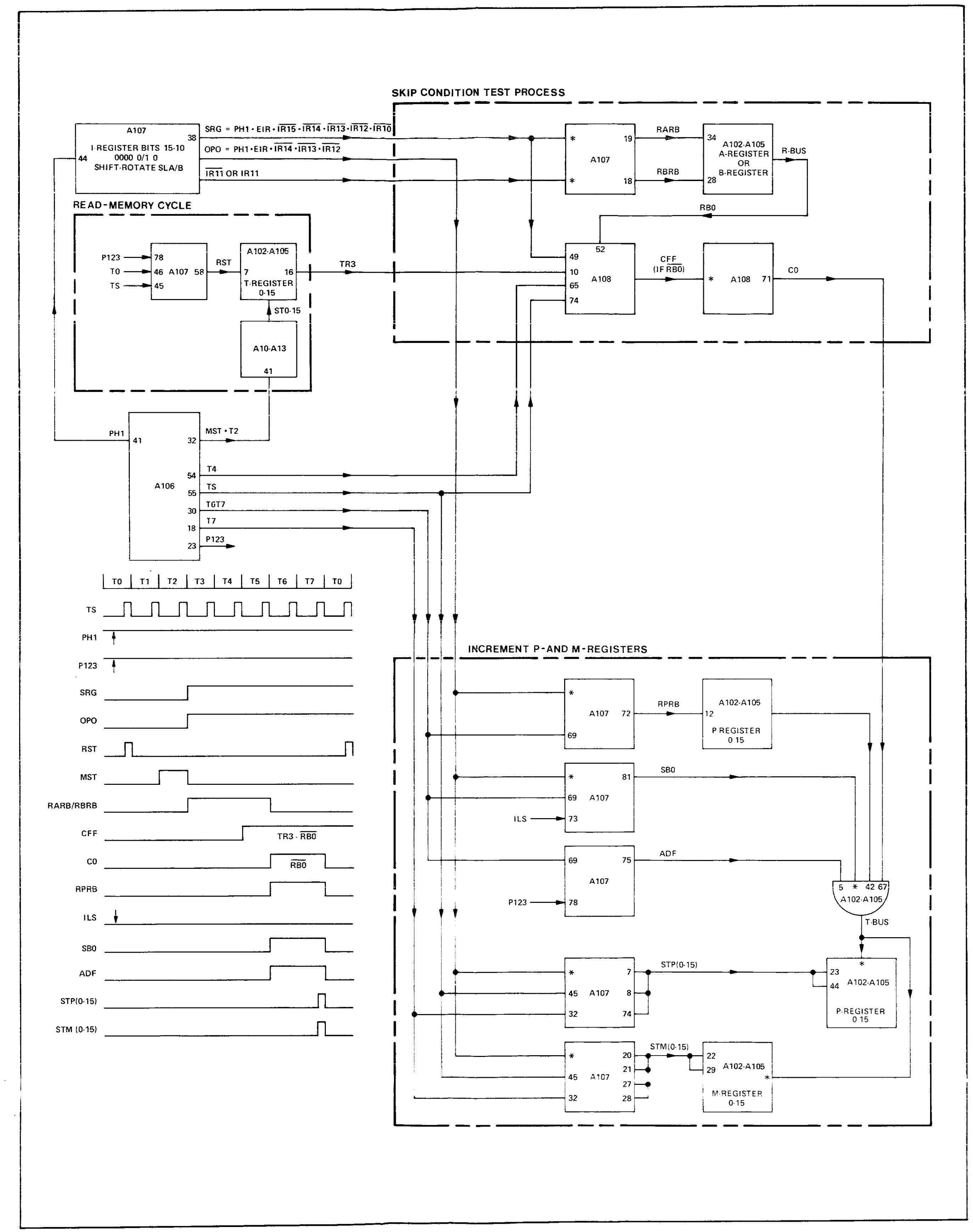

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Figure 4-48. SLA/B Instruction (Shift-Rotate Group) Processing Circuits, Servicing Diagram

4-275. A/BLS INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the A/BLS instruction. Processing operations are summarized in table 4-27. Point-to-point signal flow during phase 1 is shown in figure 4-49.

4-276. Description. The A/BLS instruction reads a number from the A- or B-register and moves all bits of that number except bit 15 one position to the left. Bit 14 is discarded; replaced by bit 13. Bit 15 remains unchanged (refer to table 4-27). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-277. The A/BLS instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, TR7, TR8, and TR9 from the T-register cause the signals SLM, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the left (signal $\overline{\text{SLM}}$), and the number stored back into the A- or B- register (signal STBA or STBB).

4-278. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-279. Test Procedure. To test the A/BLS instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Press and release the LOAD MEMORY switch (ALS instruction), or set the SWITCH REGISTER to 005000 (BLS instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the ALS instruction, or the LOAD B switch if testing the BLS instruction. (To check bit 15, set the SWITCH REGISTER to 152525.)

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register will have 025252 in it.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052524 in it.

h. At the computer front panel, press and release the RUN switch.

4-280. The computer is now in the run mode executing the ALS or BLS instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-49. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

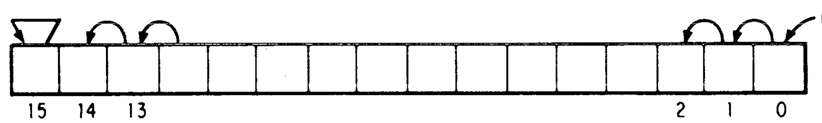
Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-27. A/BLS Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	T4 Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	T5 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus SLM Shift R Bus to T Bus Store T Bus in A or B				

Note: Data movement is as follows:



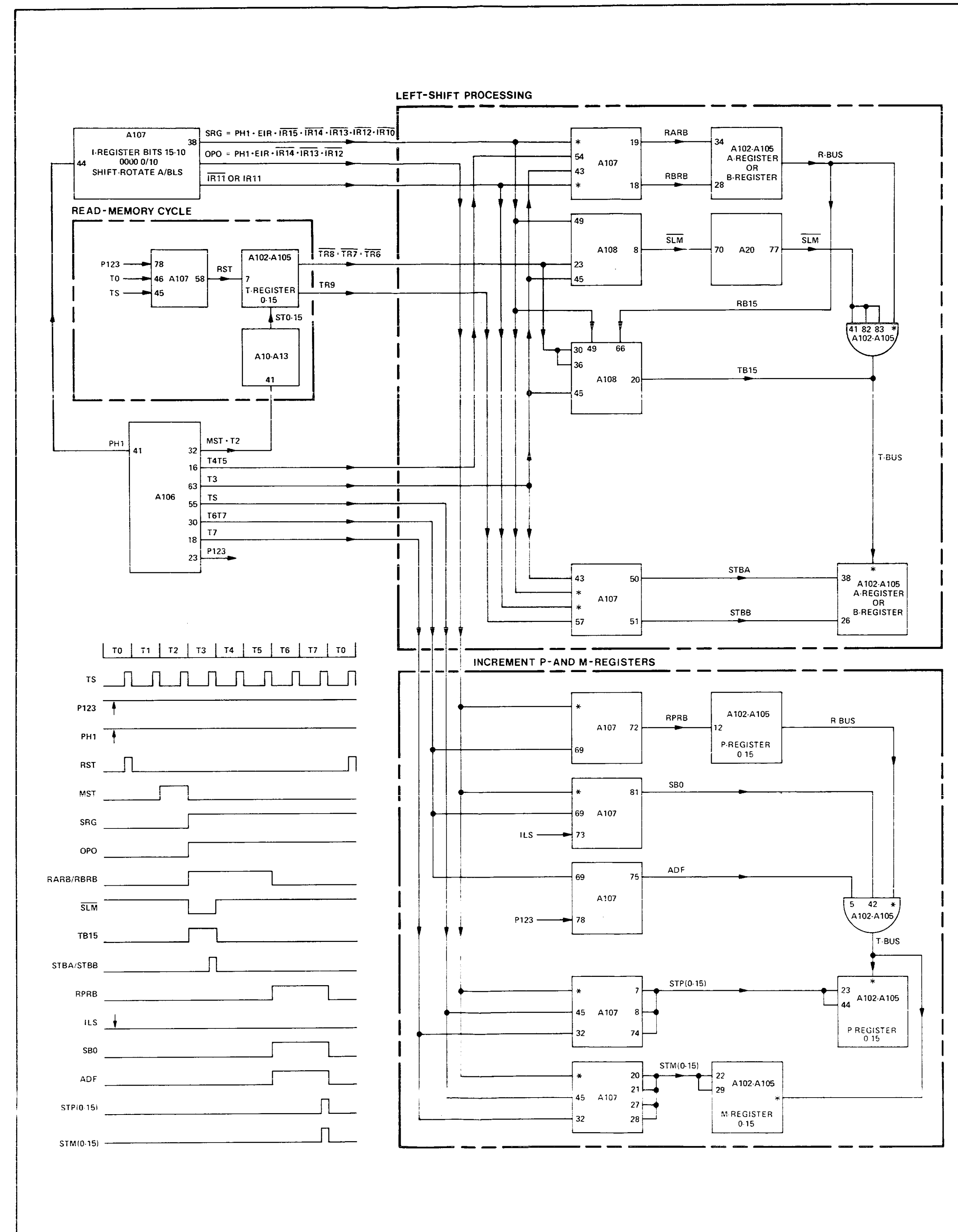


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Figure 4-49. A/BLS Instruction Processing Circuits, Servicing Diagram

4-281. A/BRS INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits used by the A/BRS instruction. Processing operations are summarized in table 4-28. Point-to-point signal flow during phase 1 is shown in figure 4-50.

4-282. Description. The A/BRS instruction reads a number from the A- or B-register and moves all bits of that number one position to the right. Bit zero is discarded; replaced by bit one. Bit 15 remains unchanged (table 4-28). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-283. The A/BRS instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, $\overline{\text{TR7}}$, $\overline{\text{TR8}}$, and TR9 from the T-register cause the signals $\overline{\text{SRM}}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the right (signal $\overline{\text{SRM}}$), and the number stored back into the A- or B- register (signal STBA or STBB).

4-284. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-285. Test Procedure. To test the A/BRS instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001100 (ARS instruction) or 005100 (BRS instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the ARS instruction, or LOAD B switch if testing the BRS instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register will have 025252 in it.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 012525 in it.

h. At the computer front panel, press and release the RUN switch.

4-286. The computer is now in the run mode executing the ARS or BRS instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-50. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

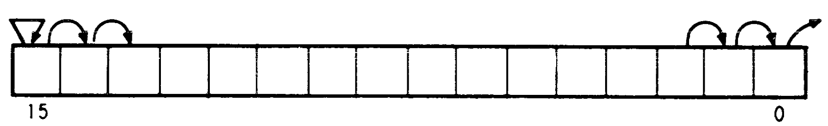
Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-28. A/BRS Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	T4 Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	T5 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B				

Note: Data movement is as follows:



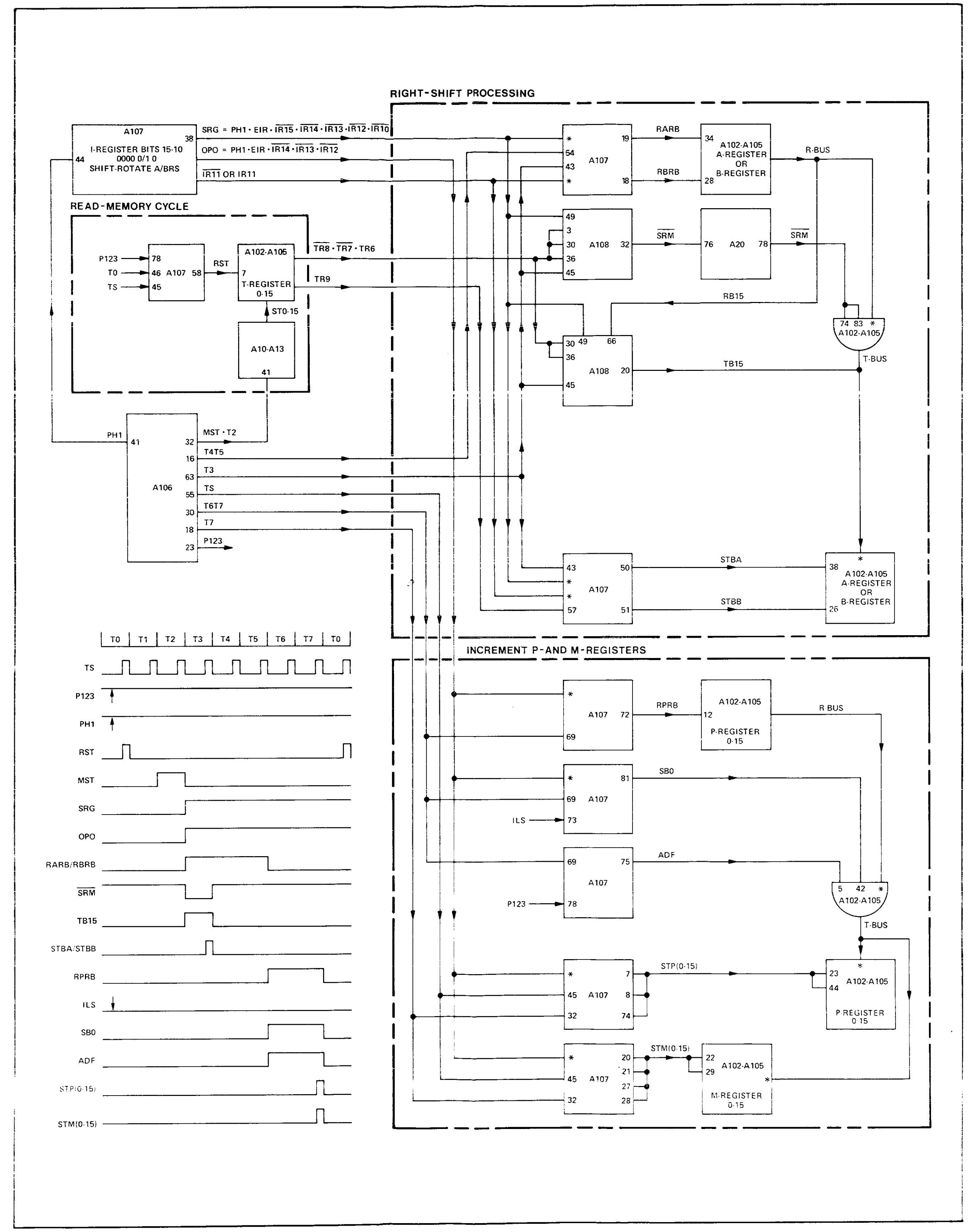


Figure 4-50. A/BRS Instruction Processing Circuits, Servicing Diagram

4-287. RA/BL INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the RA/BL instruction. Processing operations are summarized in table 4-29. Point-to-point signal flow during phase 1 is shown in figure 4-51.

4-288. Description. The RA/BL instruction reads a number from the A- or B-register and moves all bits of that number one position to the left. Bit 15 is placed in bit position zero (see table 4-29). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-289. The RA/BL instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals $\overline{\text{TR6}}$, TR7, $\overline{\text{TR8}}$, and TR9 from the T-register cause the signals $\overline{\text{SLM}}$, $\overline{\text{RLL}}$, $\overline{\text{SL14}}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the left (signals $\overline{\text{SLM}}$, $\overline{\text{RLL}}$, and $\overline{\text{SL14}}$), and the number stored back into the A- or B- register (signal STBA or STBB).

4-290. During time T6T7 signals RPRB, SB0, ADF, STP (0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-291. Test Procedure. To test the RA/BL instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001200 (RAL instruction) or 005200 (BAL instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the RAL instruction, or LOAD B switch if testing the BAL instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000, and the A-register should have 125252.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052525 in it.

h. At the computer front panel, press and release the RUN switch.

4-292. The computer is now in the run mode executing the RAL or BAL instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-51. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

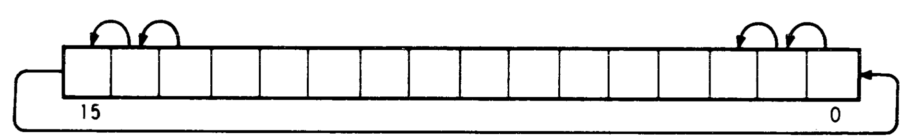
Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-29. RA/BL Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS									

SHIFT-ROTATE INSTRUCTIONS	T3	T4	T5
	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B
	Read A or B to R Bus Shift R Bus to T Bus SLM, RLL, SL14 Store T Bus in A or B		

Note: Data movement is as follows:



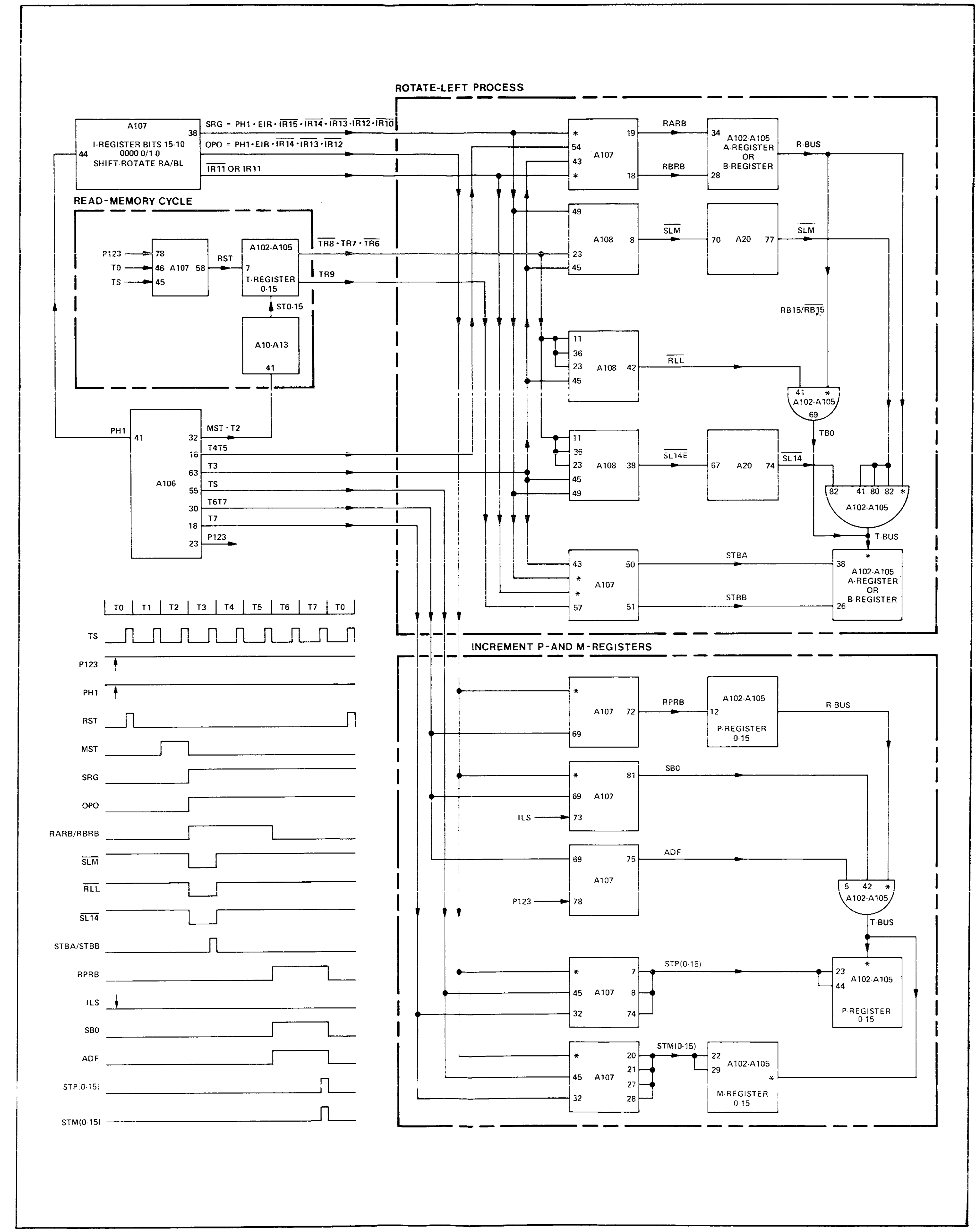


Figure 4-51. RA/BL Instruction Processing Circuits, Servicing Diagram

4-293. RA/BR INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the RA/BR instruction. Processing operations are summarized in table 4-30. Point-to-point signal flow during phase 1 is shown in figure 4-52.

4-294. Description. The RA/BR instruction reads a number from the A- or B-register and moves all bits of that number one position to the right. Bit zero is placed in bit position 15 (see table 4-30). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-295. The RA/BR instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, TR7, $\overline{\text{TR8}}$, and TR9 from the T-register cause the signals $\overline{\text{SRM}}$, $\overline{\text{RRS}}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the right (signal $\overline{\text{SRM}}$ and $\overline{\text{RRS}}$), and the number stored back into the A- or B- register (signal STBA or STBB).

4-296. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-297. Test Procedure. To test the RA/BR instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001300 (RAR instruction) or to 005300 (RBR instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the RAR instruction, or LOAD B switch if testing the RBR instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register will have 125252 in it.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052525 in it.

h. At the computer front panel, press and release the RUN switch.

4-298. The computer is now in the run mode executing the RAR or RBR instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-52. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

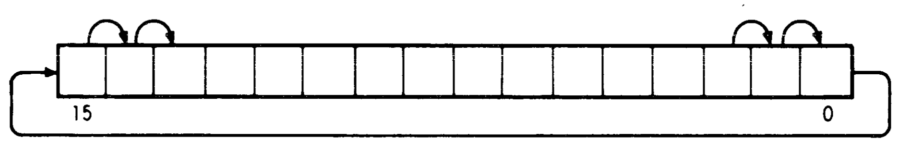
Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-30. RA/BR Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3	T4	T5		
					All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus SRM, RRS Store T Bus in A or B				

Note: Data movement is as follows:



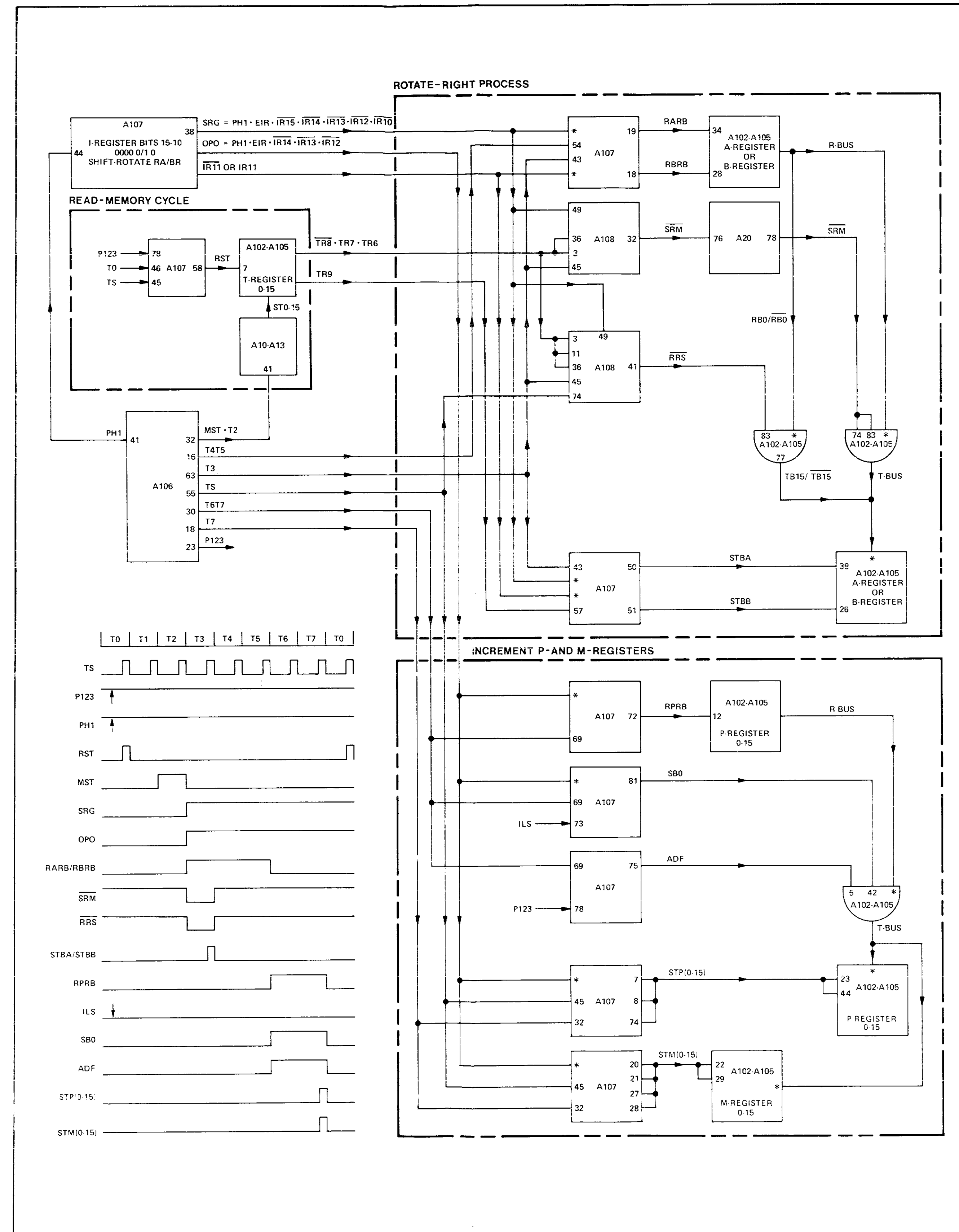


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Figure 4-52. RA/BR Instruction Processing Circuits, Servicing Diagram

4-299. A/BLR INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits used by the A/BLR instruction. Processing operations are summarized in table 4-31. Point-to-point signal flow during phase 1 is shown in figure 4-53.

4-300. Description. The A/BLR instruction reads a number from the A- or B-register and moves all bits of that number one position to the left. Bit 14 is discarded; replaced by bit 13. Bits 15 and 0 are cleared to "zero" (table 4-31). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-301. The A/BLR instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OP0, and RARB or RBRB to be generated during time T3. These signals in combination with signals $\overline{\text{TR6}}$, $\overline{\text{TR7}}$, TR8, and TR9 from the T-register cause the signals $\overline{\text{SLM}}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the left (signal $\overline{\text{SLM}}$), and the number stored back into the A- or B- register (signal STBA or STBB).

4-302. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-303. Test Procedure. To test the A/BLR instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001400 (ALR instruction) or 005400 (BLR instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the ALR instruction, or the LOAD B switch if testing the BLR instruction. (To check bit 15, set the SWITCH REGISTER to 152525.)

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS SWITCH

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register will have 025252 in it.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052524 in it.

h. At the computer front panel, press and release the RUN switch.

4-304. The computer is now in the run mode executing the ALR or BLR instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-53. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

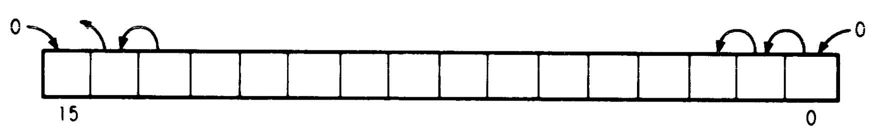
Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-31. A/BLR Instruction Processing Operations

TIME PERIODS	T0	T1	T2	T3	T4	T5	T6	T7
PHASE	READ (Mem to TR)			WRITE (TR to Mem)				
FETCH 1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M	
SHIFT-ROTATE INSTRUCTIONS				T3: All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	T4: Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	T5: All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
				Read A or B to R Bus Shift R Bus to T Bus SLM Store T Bus in A or B				

Note: Data movement is as follows:



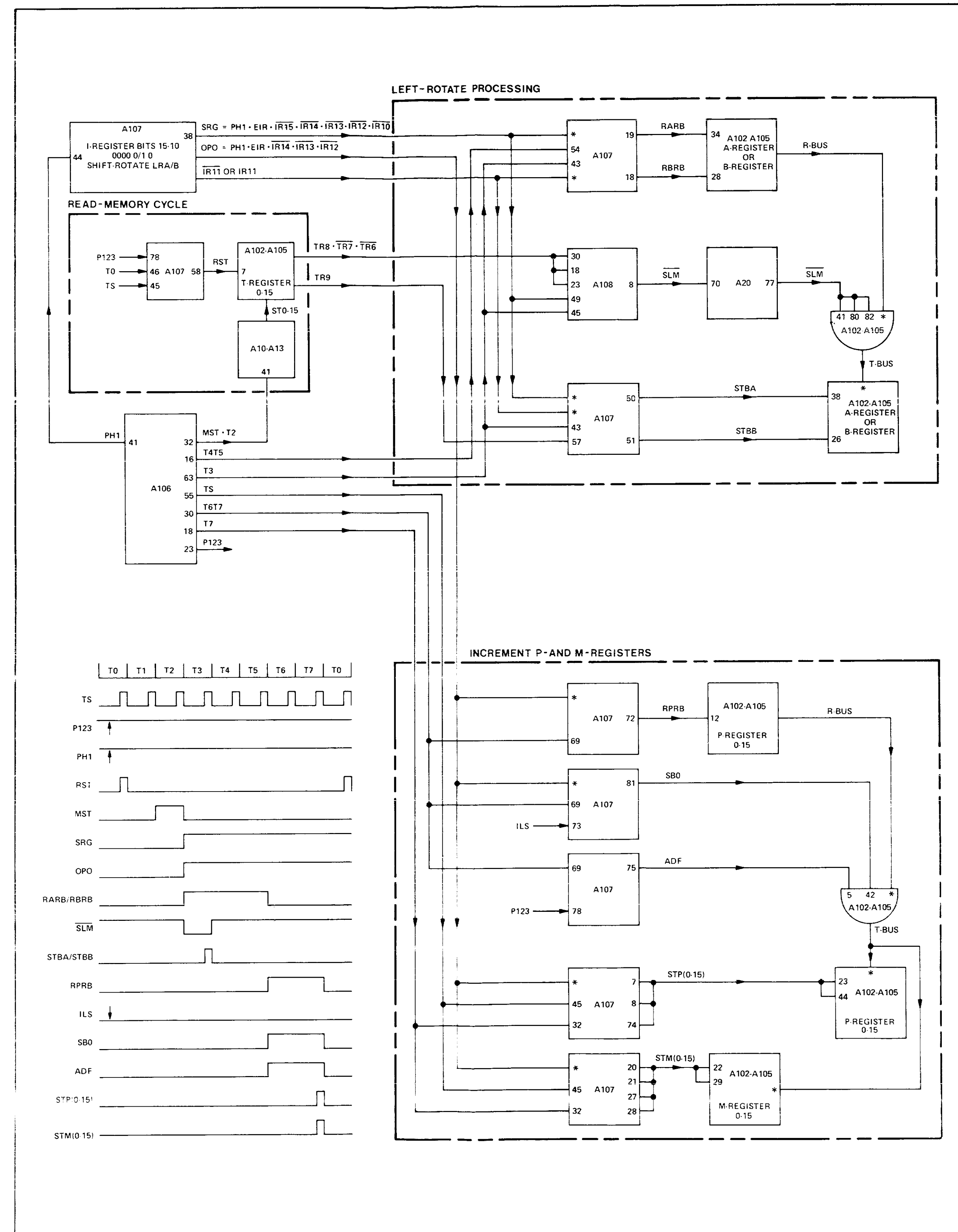


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Figure 4-53. A/BLR Instruction Processing Circuits, Servicing Diagram

4-305. ERA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the ERA/B instruction. Processing operations are summarized in table 4-32. Point-to-point signal flow during phase 1 is shown in figure 4-54.

4-306. Description. The ERA/B instruction reads a number from the A- or B-register and moves all bits of that number one position to the right. Bit zero is placed in the Extend register (E-register), and the E-register bit is placed in the bit 15 position (table 4-32). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-307. The ERA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OP0, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, $\overline{\text{TR7}}$, TR8, and TR9 from the T-register cause the signals $\overline{\text{SRM}}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the right and the E-register cleared or set depending on the state of signal RB0 (signal $\overline{\text{SRM}}$). The number is then stored back into the A- or B-register (signal STBA or STBB).

4-308. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-309. Test Procedure. To test the ERA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001500 (ERA instruction) or 005500 (ERB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the ERA instruction, or the LOAD B switch if testing the ERB instruction. (To check bit 15, set the SWITCH REGISTER to 152525.)

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them, the A-register should have 025252 or 125252 in it, and the E-register will be set (EXTEND indicator should go on).

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 112525 or 152525 in it, and the E-register will be cleared (EXTEND indicator should go out).

h. At the computer front panel, press and release the RUN switch.

4-310. The computer is now in the run mode executing the ERA or ERB instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-54. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

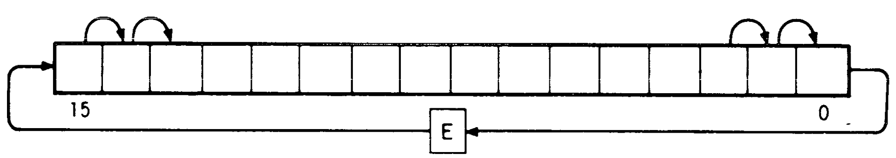
Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-32. ERA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR		Execute		P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3	T4	T5		
					All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	**Clear E and Skips** If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	**All Shifts and Rotates** Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus SLM Store T Bus in A or B				

Note: Data movement is as follows:



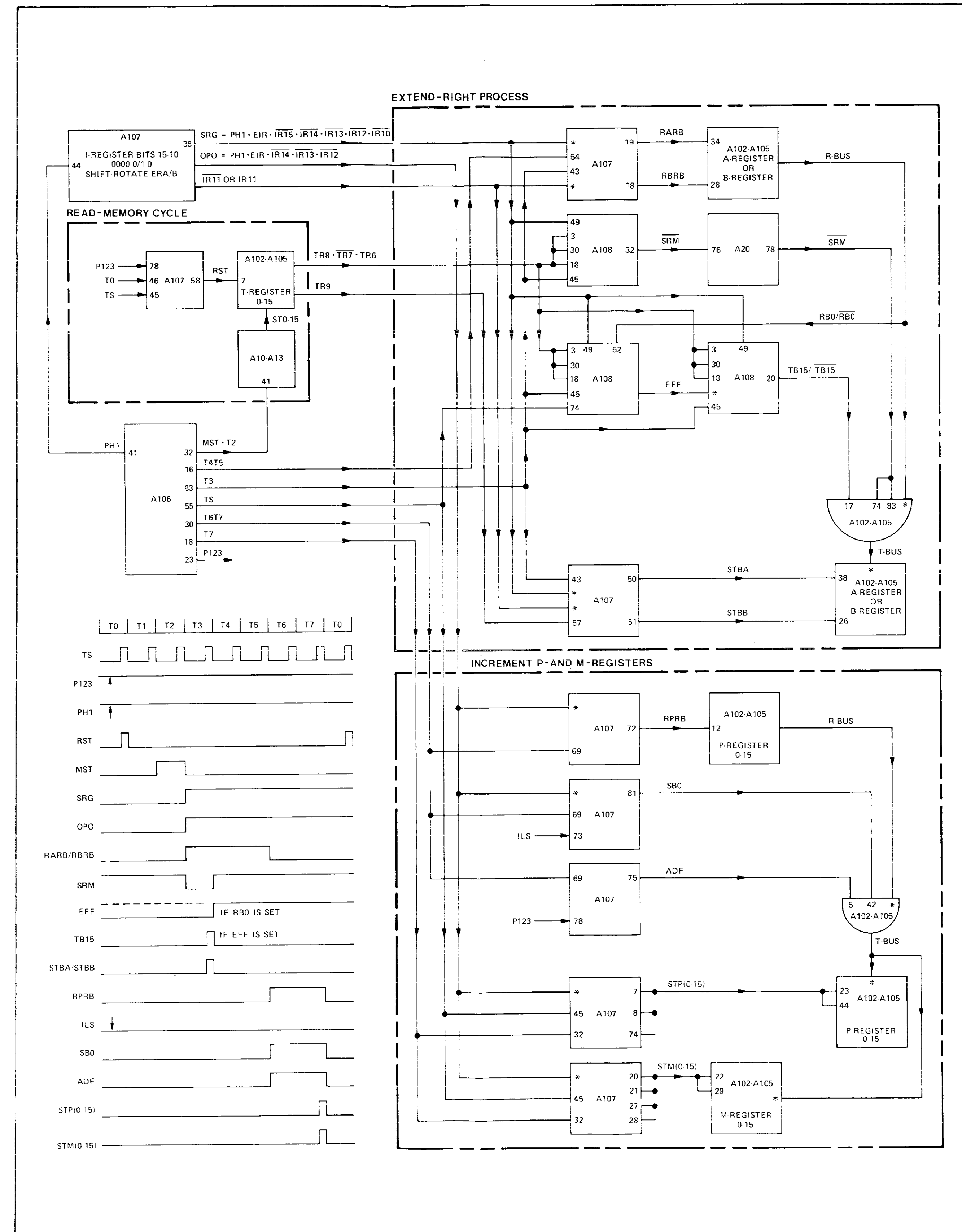


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Figure 4-54. ERA/B Instruction Processing Circuits, Servicing Diagram

4-311. ELA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the ELA/B instruction. Processing operations are summarized in table 4-33. Point-to-point signal flow during phase 1 is shown in figure 4-55.

4-312. Description. The ELA/B instruction reads a number from the A- or B-register and moves all bits of that number one position to the left. Bit 15 is placed in the Extend register (E-register), and the E-register bit is placed in the bit zero position (see table 4-33). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-313. The ELA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OP0, RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, $\overline{\text{TR7}}$, TR8, and TR9 from the T-register cause the signals $\overline{\text{SLM}}$, $\overline{\text{SL14}}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the left and the E-register cleared or set depending on the state of signal RB0. (signal $\overline{\text{SLM}}$ and $\overline{\text{SL14}}$). The number is then stored back into the A- or B-register (signal STBA or STBB).

4-314. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-315. Test Procedure. To test the ELA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001600 (ELA instruction) or 005600 (ELB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 152525 and press and release the LOAD A switch if testing the ELA instruction, or LOAD B switch if testing the ELB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register should have 125252 or 125253 in it and the E-register should be set.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052525 or 052527 in it and the E-register should be cleared.

h. At the computer front panel, press and release the RUN switch.

4-316. The computer is now in the run mode executing the ELA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-55. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

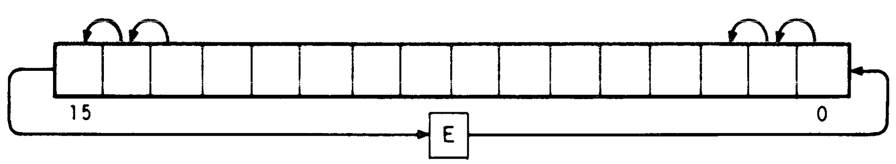
Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-33. ELA/B Instruction Processing Operations

TIME PERIODS	T0	T1	T2	T3	T4	T5	T6	T7
PHASE	READ (Mem to TR)			WRITE (TR to Mem)				
FETCH 1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	

SHIFT-ROTATE INSTRUCTIONS	T3	T4	T5
	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B
	Read A or B to R Bus Shift R Bus to T Bus SLM, SL14 Store T Bus in A or B		

Note: Data movement is as follows:



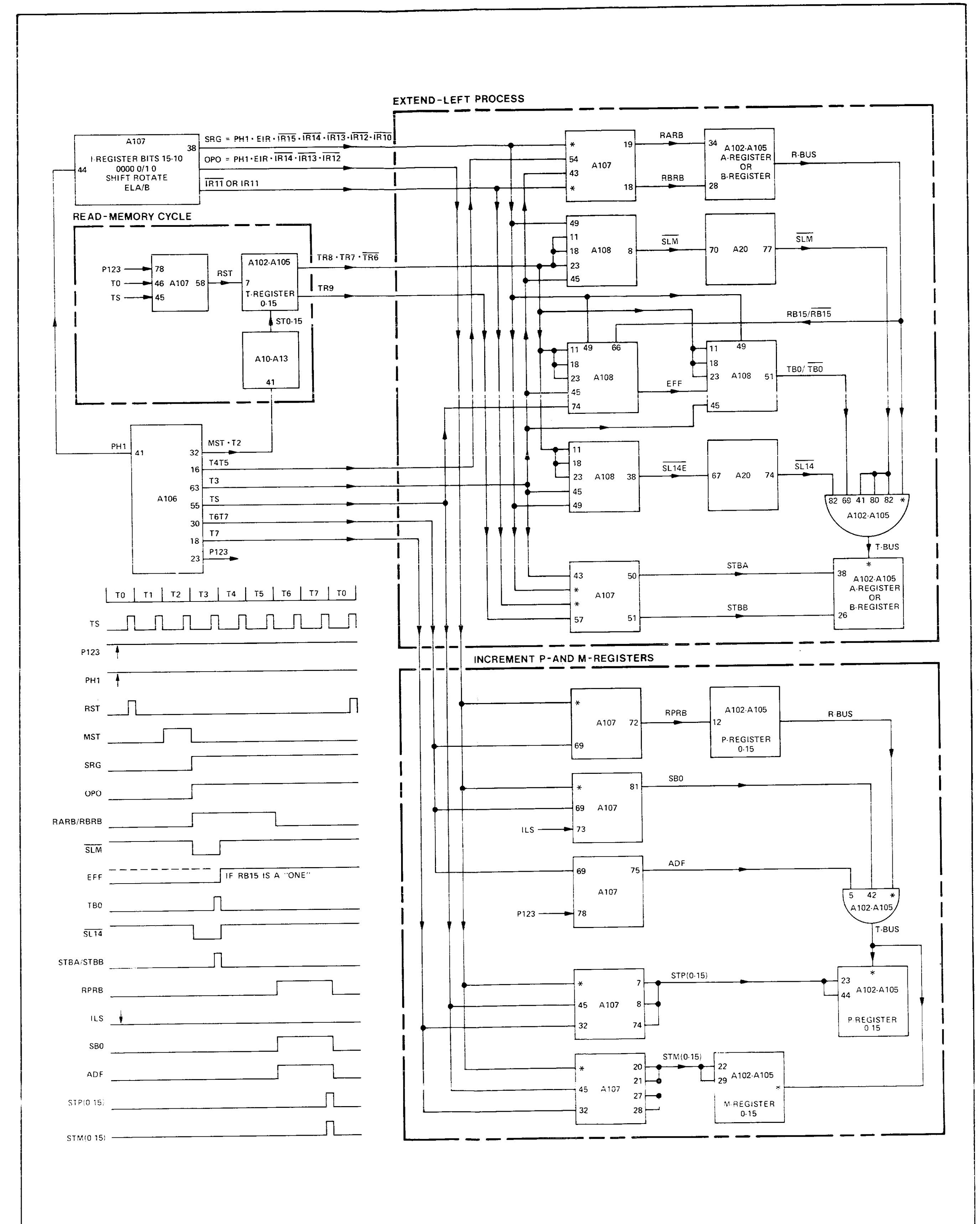


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Figure 4-55. ELA/B Instruction Processing Circuits, Servicing Diagram

4-317. A/BLF INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the A/BLF instruction. Processing operations are summarized in table 4-34. Point-to-point signal flow during phase 1 is shown in figure 4-56.

4-318. Description. The A/BLF instruction reads a number from the A- or B-register and moves all bits of that number four positions to the left. The high order bits are placed in the low order bit position (see table 4-34). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-319. The A/BLF instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OP0, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, $\overline{\text{TR7}}$, TR8, and TR9 from the T-register cause the signals $\overline{\text{RL4}}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved four positions to the left (signal $\overline{\text{RL4}}$), and the number stored back into the A- or B- register (signal STBA or STBB).

4-320. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-321. Test Procedure. To test the A/BLF instruction circuits, proceed as follows:

Note

> If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001700 (ALF instruction) or 005700 (BLF instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 152525 and press and release the LOAD A switch if testing the ALF instruction, or LOAD B switch if testing the BLF instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should remain at location 001000, and the A-register should have 052535 in it.

g. Repeat step f above. The P- and M-registers will remain at location 001000, and the A-register should have 052725 in it.

h. At the computer front panel, press and release the RUN switch.

4-322. The computer is now in the run mode executing the ALF instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-56. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

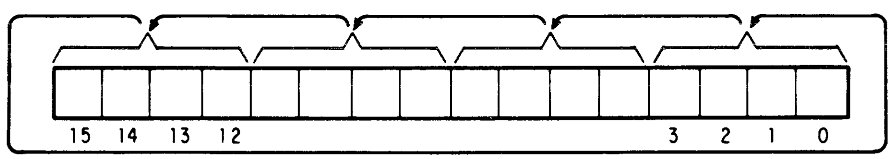
Note

> Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-34. A/BLF Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	T4 Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	T5 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus RL4 Store T Bus in A or B				

Note: Data movement is as follows:



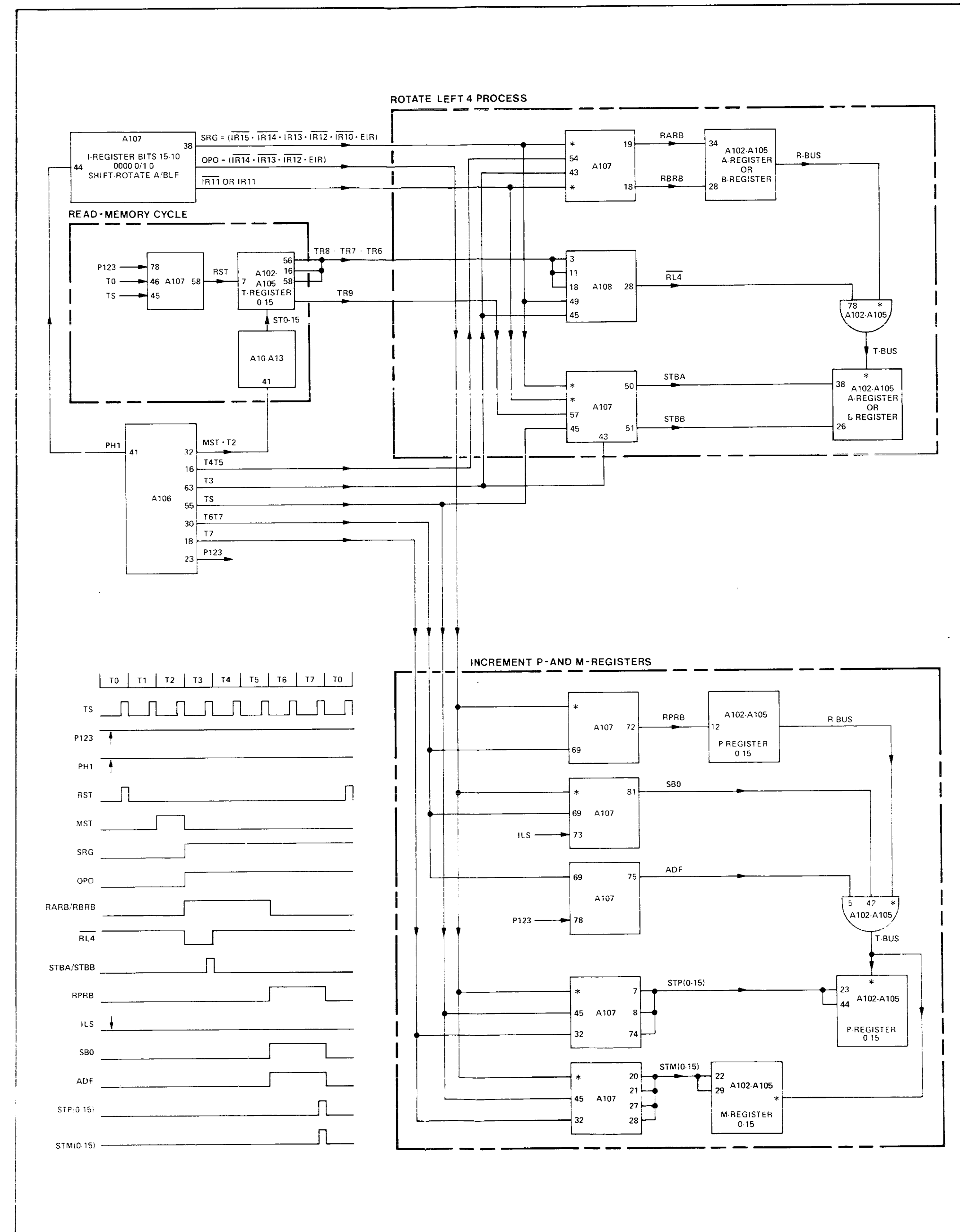


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Figure 4-56. A/BLF Instruction Processing Circuits, Servicing Diagram

4-323. CLA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CLA/B instruction. Processing operations are summarized in table 4-35. Point-to-point signal flow during phase 1 is shown in figure 4-57.

4-324. Description. The CLA/B instruction resets the A- or B-register. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 or 00011 in the I-register causes signals ASG and OP0 to be generated during time T3. These signals in combination with signal TR8 from the T-register cause the signals $\overline{\text{EOF}}$ and STBA or STBB to be generated also at time T3. These signals cause the R- and S-buses to be combined and transferred to the T-bus (signal $\overline{\text{EOF}}$), and the T-bus data (zeros) to be stored in the A- or B-register (signal STBA or STBB).

4-325. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-326. Test Procedure. To test the CLA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002400 (CLA instruction) or 006400 (CLB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 177777 and press and release the LOAD A switch if testing the CLA instruction, or LOAD B switch if testing the CLB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The A-register should be cleared to zero.

g. At the computer front panel, press and release the RUN switch.

4-327. The computer is now in the run mode executing the CLA instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-57. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-35. CLA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3 No Read (R Bus all zeros) EOF Store T Bus in A/B	T4	T5		

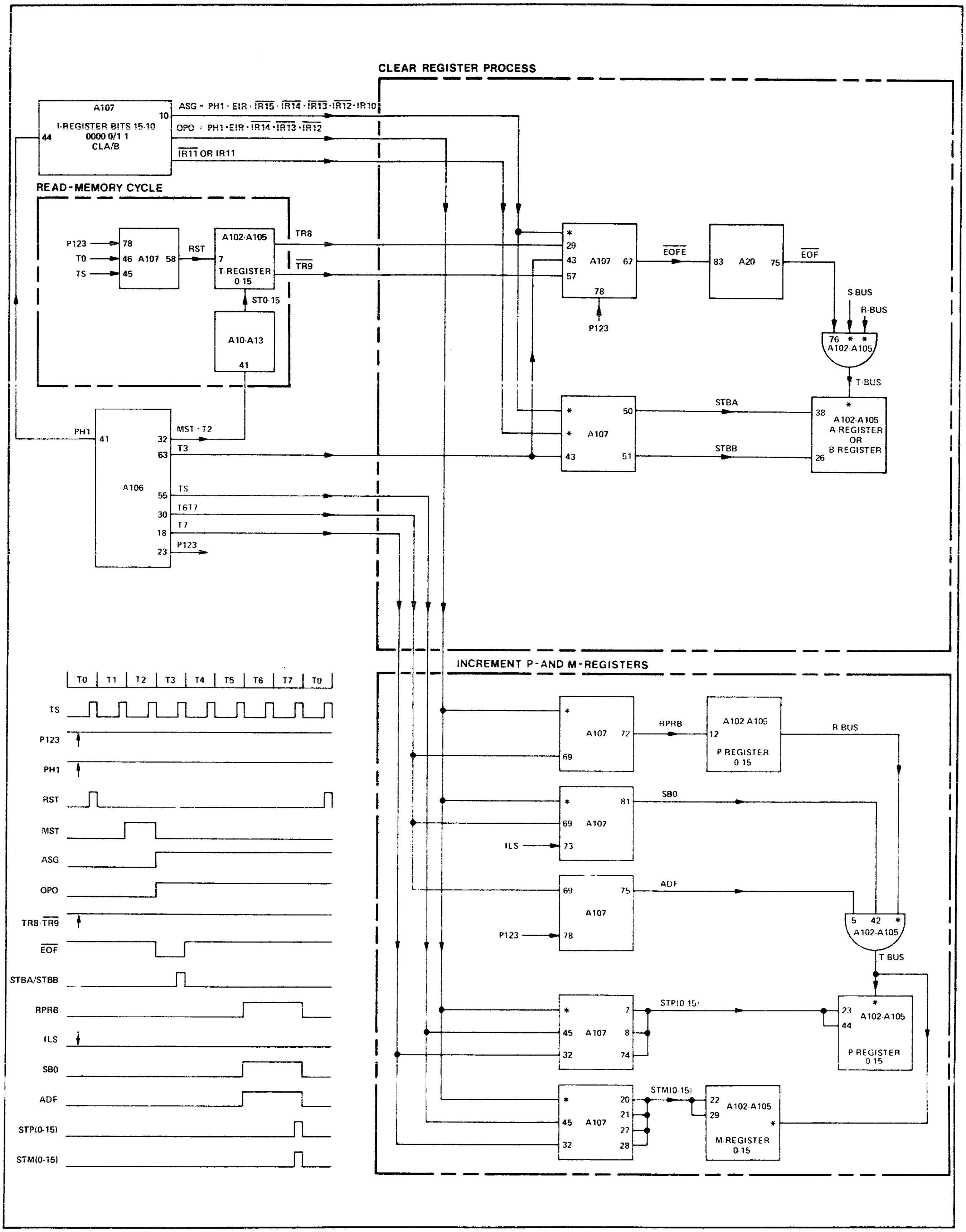

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Figure 4-57. CLA/B Instruction Processing Circuits, Servicing Diagram

4-328. CMA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CMA/B instruction. Processing operations are summarized in table 4-36. Point-to-point signal flow during phase 1 is shown in figure 4-58.

4-329. Description. The CMA/B instruction compliments the data in the A- or B-register. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 or 00011 in the I-register causes signals ASG and OP0 to be generated during time T3. These signals in combination with signal $\overline{\text{TR8}}$ and TR9 from the T-register cause the signals RARB or RBRB, $\overline{\text{CMF}}$, and STBA or STBB to be generated also at time T3. These signals cause the A- or B-register data to be read onto the R-bus (signal RARB or RBRB), the R-bus to be complimented and transferred to the T-bus (signal $\overline{\text{CMF}}$), and the T-bus data to be stored in the A- or B-register (signal STBA or STBB).

4-330. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-331. Test Procedure. To test the CMA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 003000 (CMA instruction) or 007000 (CMB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 177777 and press and release the LOAD A switch if testing the CMA instruction, or the LOAD B switch if testing the CMB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch twice. The A-register data should be complemented to "zeros" and then back to "ones".

g. At the computer front panel, press and release the RUN switch.

4-332. The computer is now in the run mode executing the CMA instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-58. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-36. CMA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR		Execute		P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3 Read A/B to R Bus CMF Store T Bus in A/B	T4	T5		

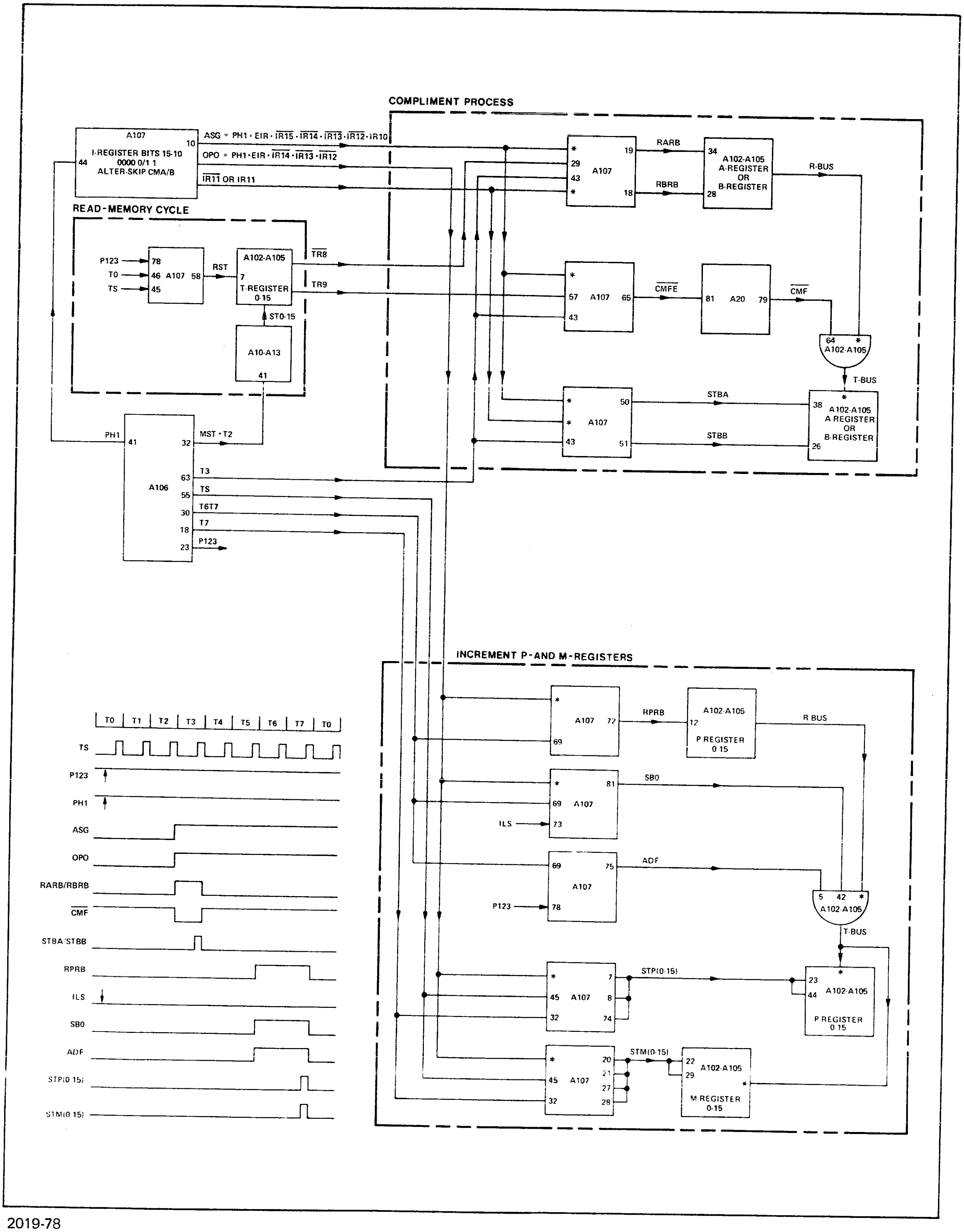

Figure 4-58. CMA/B Instruction Processing Circuits, Servicing Diagram

4-333. CCA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CCA/B instruction. Processing operations are summarized in table 4-37. Point-to-point signal flow during phase 1 is shown in figure 4-59.

4-334. Description. The CCA/B instruction compliments the data (zeros) on the R-bus and transfers this complimented data (ones) to the T-bus. The T-bus data is then stored in the A- or B-register. At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-335. The CCA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 or 00011 in the I-register causes signals ASG and OP0 to be generated during time T3. These signals in combination with signals TR8 and TR9 from the T-register cause the signals $\overline{\text{CMF}}$, and STBA or STBB to be generated. These signals cause the R-bus data (zeros) to be complimented and transferred to the T-bus (signal $\overline{\text{CMF}}$), and the complimented data (ones) to be stored into the A- or B-register (signal STBA or STBB).

4-336. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-337. Test Procedure. To test the CCA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 003400 (CCA instruction) or 007400 (CCB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the CCA instruction, or the LOAD B switch if testing the CCB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register should have 177777 in it.

g. At the computer front panel, press and release the RUN switch.

4-338. The computer is now in the run mode executing the CCA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-59. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-37. CCA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)		WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR		Execute		P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					No Read (R Bus all zeros) CMF Store T Bus in A/B				

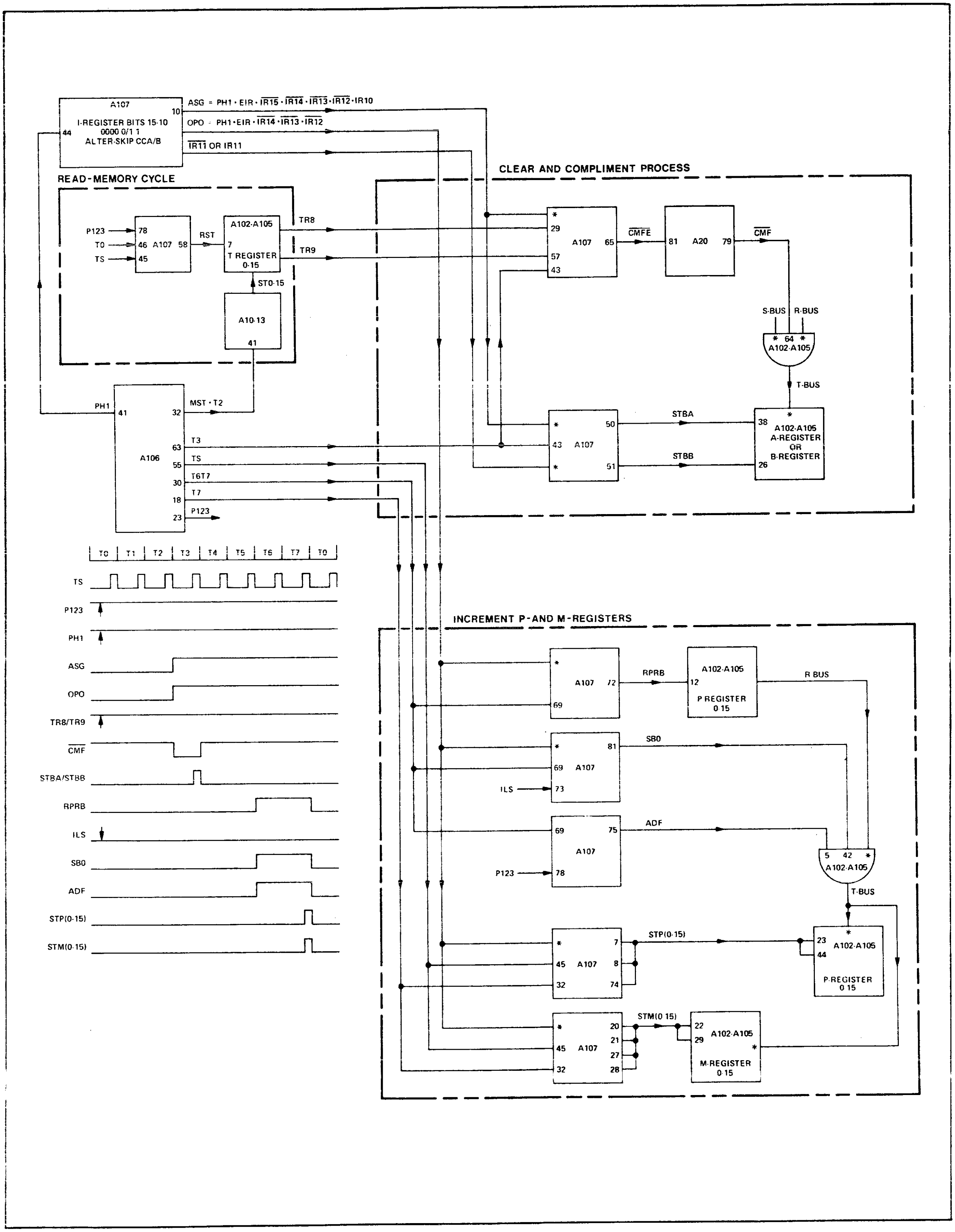

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Figure 4-59. CCA/B Instruction Processing Circuits, Servicing Diagram

4-339. CLE INSTRUCTION (Alter-Skip Group). The following paragraphs provide a description and test procedure for the circuits that process the CLE instruction. Processing operations are summarized in table 4-38. Point-to-point signal flow during phase 1 is shown in figure 4-60.

4-340. <u>Description.</u> The CLE instruction resets the Extend register (E-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 in the I-register causes signals ASG, OP0, and RARB to be generated during time T3. These signals in combination with signals TR6 and $\overline{TR7}$ from the T-register cause the E-register to reset at time T3TS. The A-register data is read onto the R-bus (signal RARB) during time T4T5 but is not used.

4-341. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-342. <u>Test Procedure.</u> To test the CLE instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002100 (CLE instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

4-343. The computer is now in the run mode executing the CLE instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-60. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-38. CLE Instruction (Alter-Skip Group) Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)		WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3: Reset E Flip-flop	T4:	T5:		

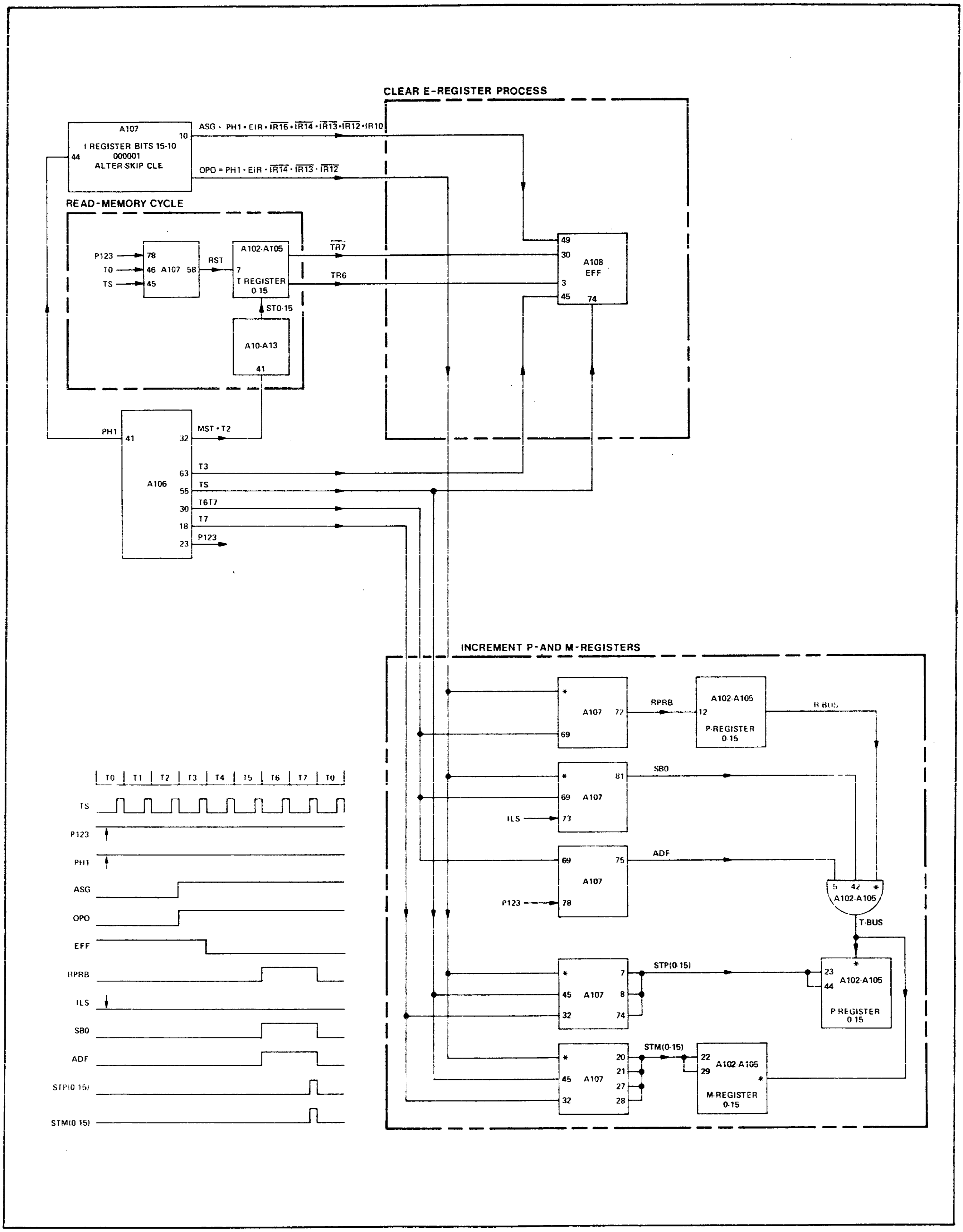

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Figure 4-60. CLE Instruction (Alter-Skip Group) Processing Circuits, Servicing Diagram

4-344. CME INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CME instruction. Processing operations are summarized in table 4-39. Point-to-point signal flow during phase 1 is shown in figure 4-61.

4-345. Description. The CME instruction reverses the state of the Extend register (E-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 in the I-register causes signals ASG and OP0 to be generated during time T3. These signals in combination with signals $\overline{TR6}$ and TR7 from the T-register cause the E-register to reverse its state at time T3TS. The A-register data is read onto the R-bus (signal RARB) during time T4T5 but is not used.

4-346. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-347. Test Procedure. To test the CME instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002200 (CME instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the RUN switch.

4-348. The computer is now in the run mode executing the CME instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-61. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-39. CME Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS			T3: Complement E Flip-flop			T4	T5		

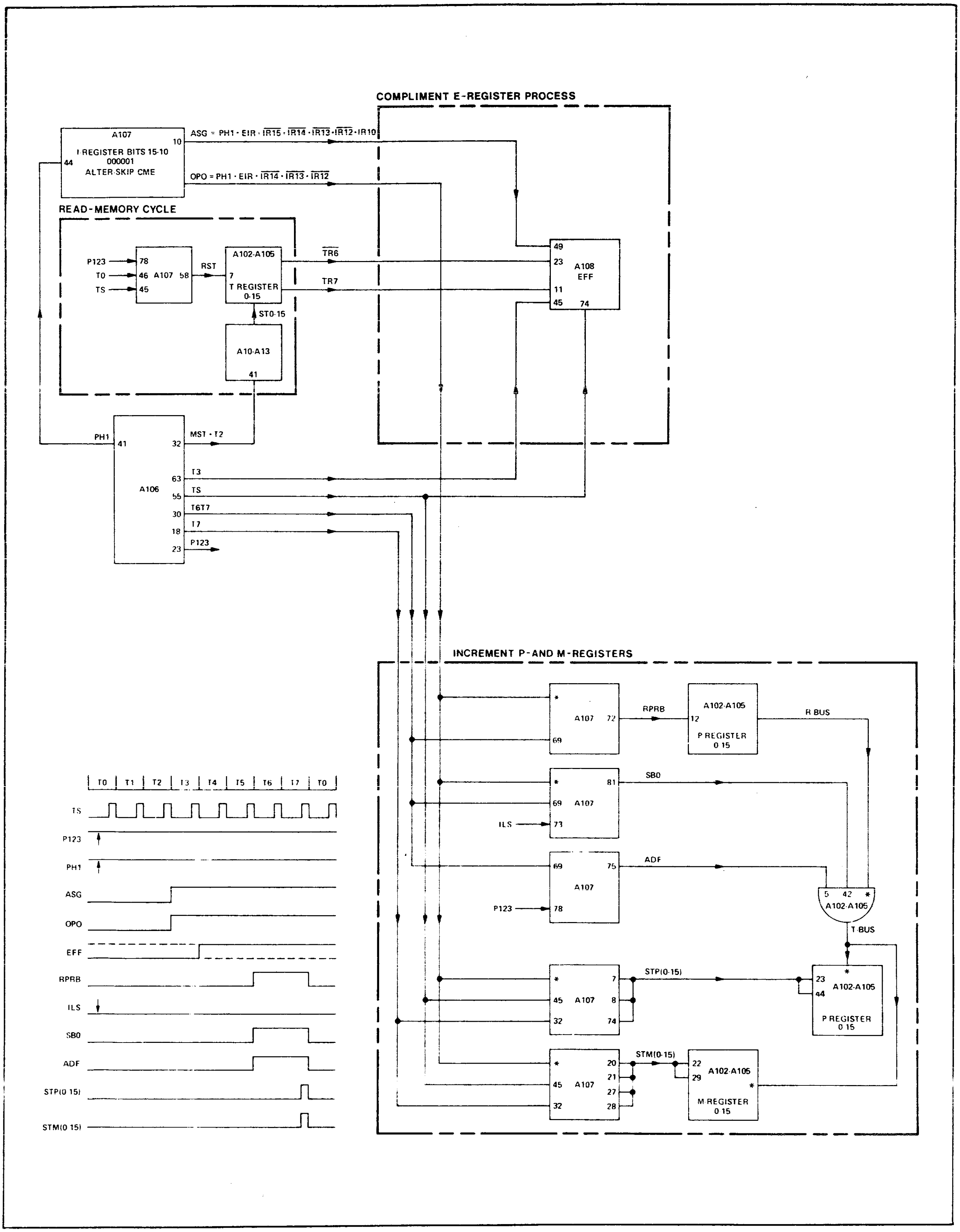

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Figure 4-61. CME Instruction Processing Circuits, Servicing Diagram

4-349. CCE INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CCE instruction. Processing operations are summarized in table 4-40. Point-to-point signal flow during phase 1 is shown in figure 4-62.

4-350. Description. The CCE instruction sets the Extend register (E-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 in the I-register causes signals ASG and OP0 to be generated during time T3. These signals in combination with signals TR6 and TR7 from the T-register cause the E-register to set at time T3TS.

4-351. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-352. Test Procedure. To test the CCE instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002300 (CCE instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

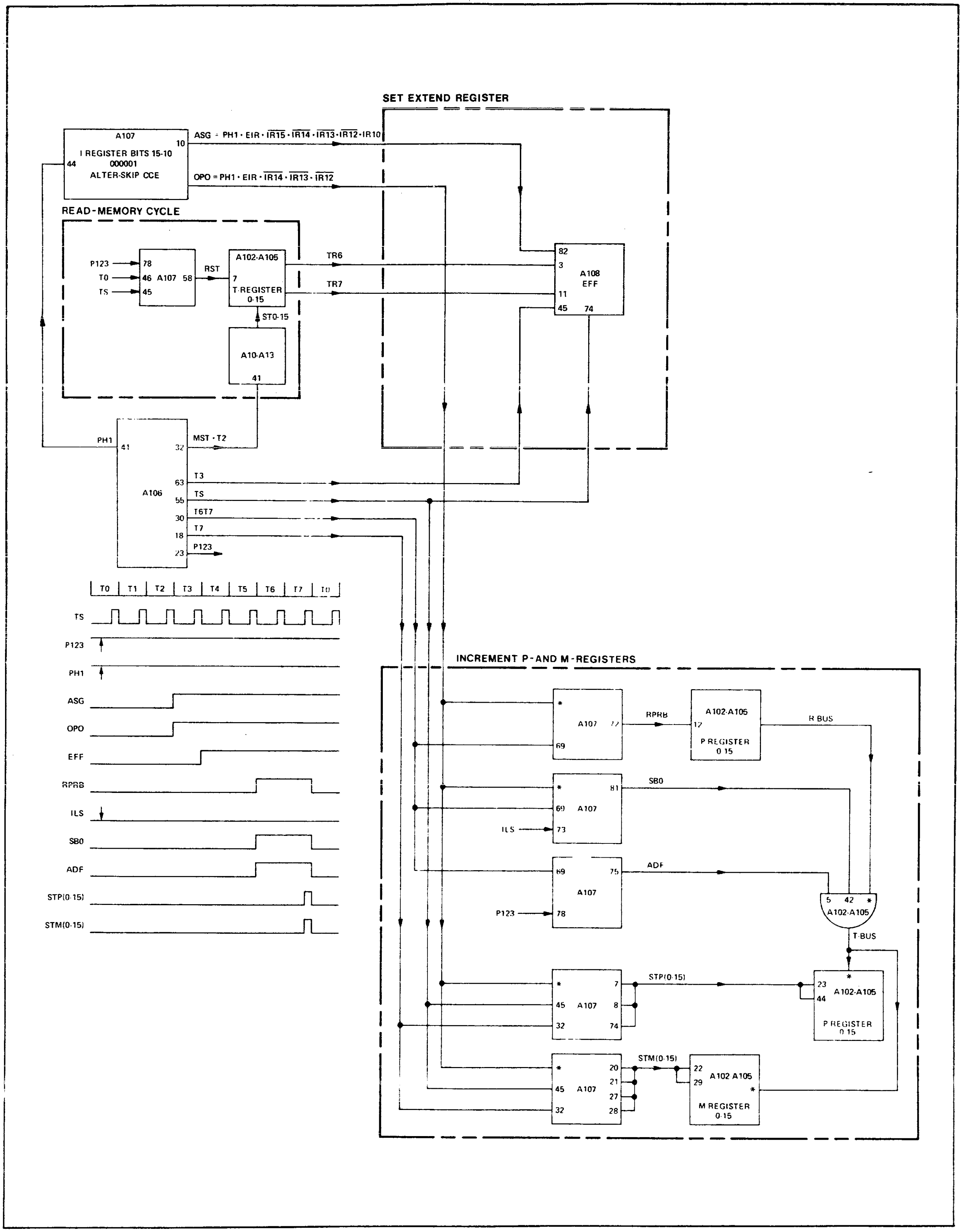
4-353. The computer is now in the run mode executing the CCE instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-62. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-40. CCE Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3	T4	T5		
CCE					Set E Flip-flop				



2019-73

Figure 4-62. CCE Instruction Processing Circuits, Servicing Diagram

4-354. SEZ INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SEZ instruction. Processing operations are summarized in table 4-41. Point-to-point signal flow during phase 1 is shown in figure 4-63.

4-355. Description. The SEZ instruction compares bit zero from the T-register with the reset output of the E-register. If both signals are true, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If both signals are false or one true and one false, the program continues with the next instruction in sequence.

4-356. The SEZ instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 in the I-register causes signals ASG and OP0 to be generated during time T3. These signals in combination with signal TR5 from the T-register cause T-register bit zero ($\overline{\text{TR0}}$) signal and the signal from the reset side of the E-register flip-flop ($\overline{\text{EFF}}$) to be compared and the Carry FF (CFF) to set at time T3TS if signals $\overline{\text{TR0}}$ and $\overline{\text{EFF}}$ are both true. Signal CFF causes signal C0 to be generated at time T6T7.

4-357. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-458. Test Procedure. To test the SEZ instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002040 (SEZ instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the RUN switch.

4-359. The computer is now in the run mode executing the SEZ instruction in location 001000. If the E-register is "zero" the JMP instruction will be executed. Using a dual-trace oscilloscope, check the signals shown in figure 4-63. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-41. SEZ Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P +1 +Carry to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3: Set Carry if: E = 0 and TR0 = 0, or E = 1 and TR0 = 1	T4:	T5:		

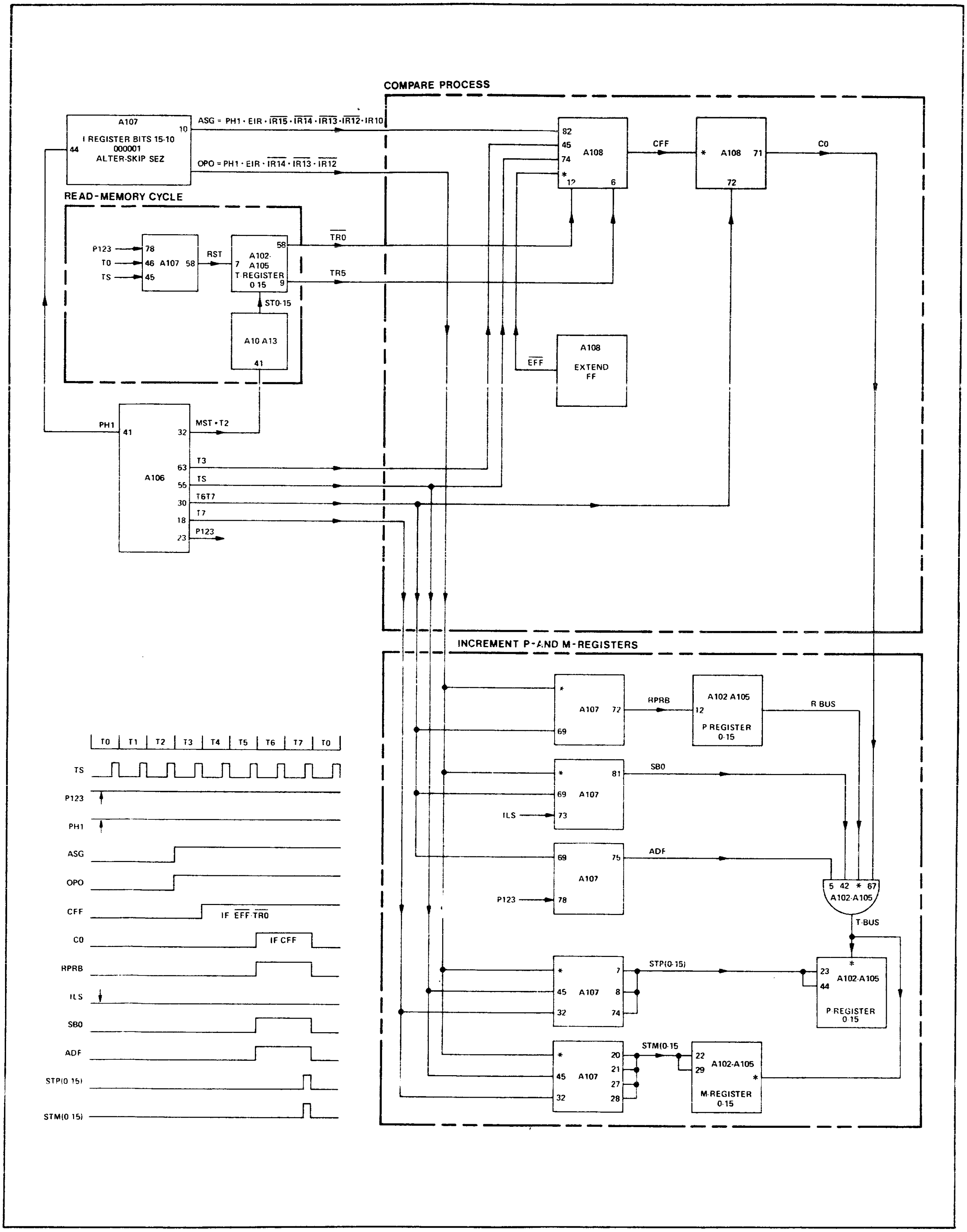


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Figure 4-63. SEZ Instruction Processing Circuits, Servicing Diagram

4-360. SSA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SSA/B instruction. Processing operations are summarized in table 4-42. Point-to-point signal flow during phase 1 is shown in figure 4-64.

4-361. Description. The SSA/B instruction reads a number from the A- or B-register and compares bit 15 of the A- or B-register with bit zero of the T-register (TR0). If the comparison is equal, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If the comparison is unequal, the program continues with the next instruction in sequence.

4-362. The SSA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 or 00011 in the I-register causes signals ASG, OP0, and RARB or RBRB to be generated during times T3 and T4. These signals in combination with signal TR4 from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), and the Carry FF (CFF) to set at time T4TS if bit zero of the T-register (TR0) and bit 15 of the R-bus (RB15) are equal (both true or both false). Signal CFF causes signal C0 to be generated at time T6T7.

4-363. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-364. Test Procedure. To test the SSA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002020 (SSA instruction) or 006020 (SSB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 (equal compare) and press and release the LOAD A switch if testing the SSA instruction, or the LOAD B switch if testing the SSB instruction. (Substitute 100000 for 000000 for an unequal compare.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001001 in them.

h. Repeat step g above. The P- and M-registers should have 001000 in them.

i. At the computer front panel, press and release the RUN switch.

4-365. The computer is now in the run mode executing the SSA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-64. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-42. SSA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	*Execute			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3	T4: Read A/B to R Bus Set Carry if: RB15 = 0 and TR0 = 0; or RB15 = 1 and TR0 = 1	T5		

*Combination of SSA/B, SLA/B, and RSS is a special case; see paragraph 4-384.

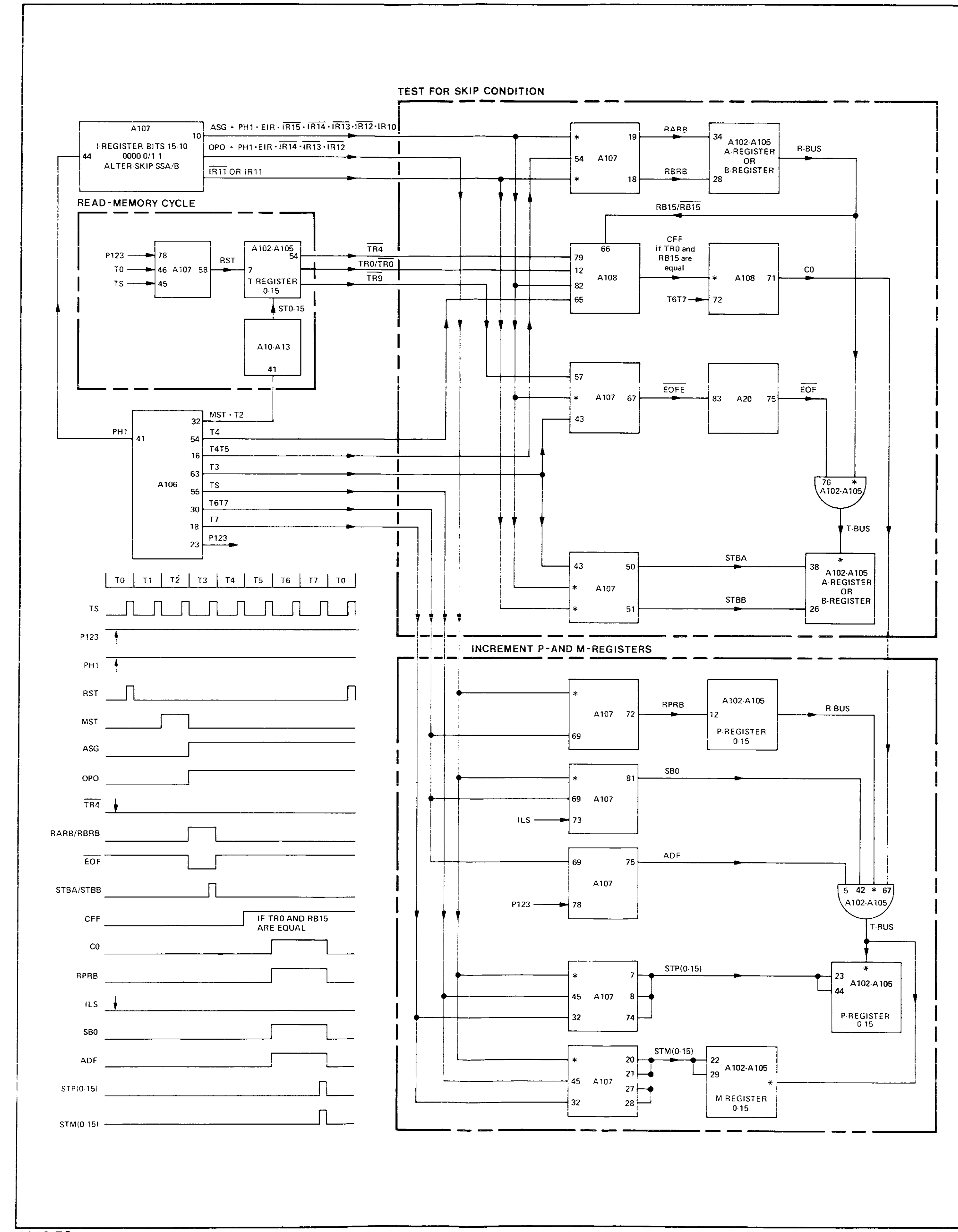

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Figure 4-64. SSA/B Instruction Processing Circuits, Servicing Diagram

4-366. SLA/B INSTRUCTION (Alter-Skip Group). The following paragraphs provide a description and test procedure for the circuits that process the SLA/B instruction. The processing operations are summarized in table 4-43. Point-to-point signal flow during phase 1 is shown in figure 4-65.

4-367. Description. The SLA/B instruction reads a number from the A- or B-register and compares bit zero of the A- or B-register with bit zero of the T-register. If the comparison is equal, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If the comparison is unequal, the program continues with the next instruction in sequence.

4-368. The SLA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 or 00011 in the I-register causes signals ASG, OP0, and RARB or RBRB to be generated during times T3 and T4. These signals in combination with signal TR3 from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), and the Carry FF (CFF) to set at time T4TS if bit zero of the R-bus (signal RB0) and bit zero of the T-register (signal TR0) are equal (both true or both false). Signal CFF causes signal C0 to be generated at time T6T7.

4-369. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-370. Test Procedure. To test the SLA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002010 (SLA instruction) or 006010 (SLB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 (equal compare) and press and release the LOAD A switch if testing the SLA instruction, or the LOAD B switch is testing the LSB instruction. (Substitute 000001 to 000000 for an unequal compare.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001001 in them.

h. Repeat step g above. The P- and M-registers should have 001000 in them.

i. At the computer front panel, press and release the RUN switch.

4-371. The computer is now in the run mode executing the SLA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-65. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-43. SLA/B Instruction (Alter-Skip Group) Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	*Execute			P +1 +Carry to P, M Set PH1	

ALTER-SKIP INSTRUCTIONS	T3	T4	T5
		Read A/B to R Bus Set Carry if: RB0 = 0 and TR0 = 0, or RB0 = 1 and TR0 = 1	

*Combination of SSA/B, SLA/B, and RSS is a special case; see paragraph 4-384.

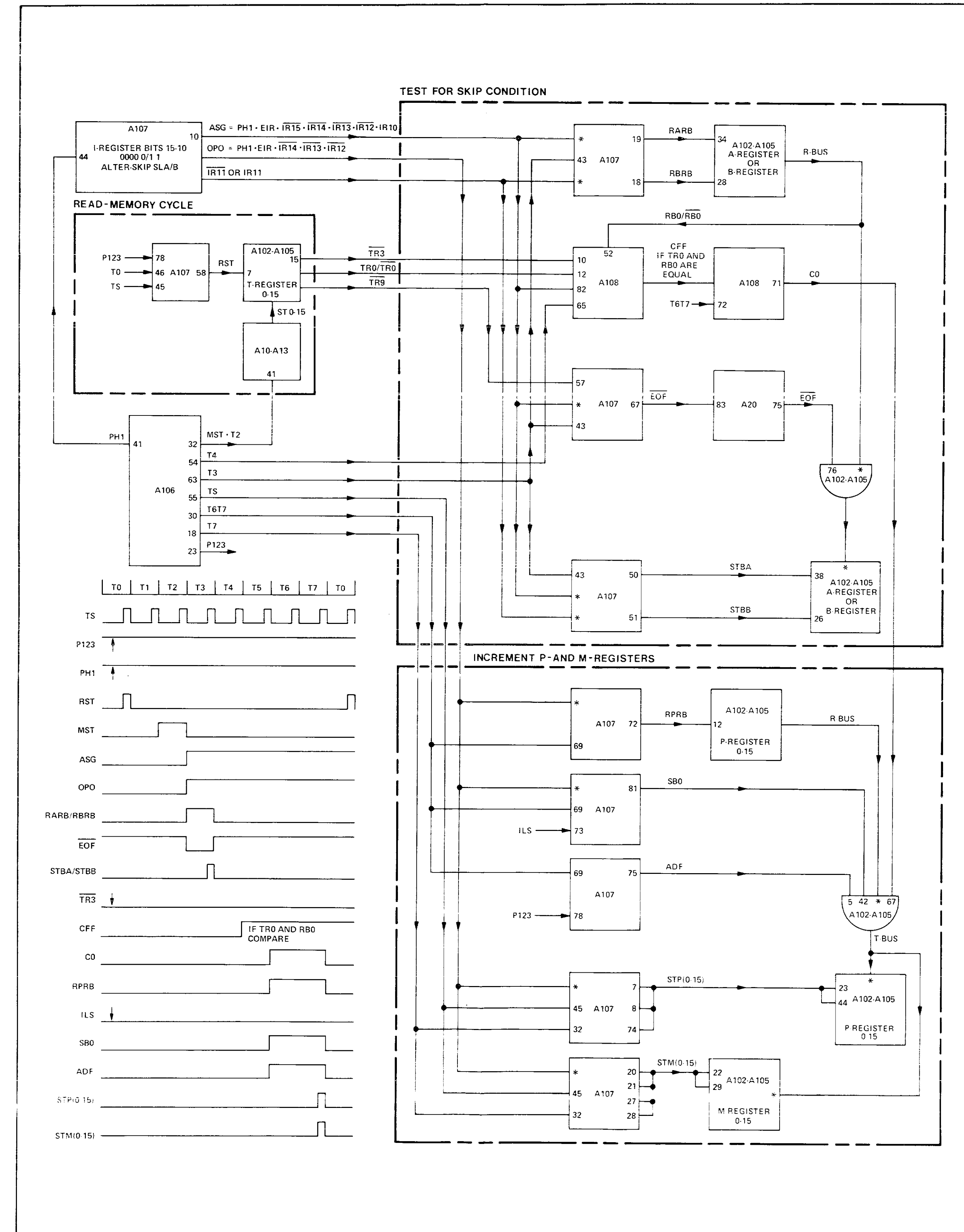

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Figure 4-65. SLA/B Instruction (Alter-Skip Group) Processing Circuits, Servicing Diagram

4-372. INA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the INA/B instruction. The processing operations are summarized in table 4-44. Point-to-point signal flow during phase 1 is shown in figure 4-66.

4-373. Description. The INA/B instruction reads a number from the A- or B-register and increments that number by one. The incremented number is then stored back in the A- or B-register. At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

3-374. The INA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the in instruction code is read into the I-register. Bit configuration 000 0/11 in the I-register causes signals ASG, OP0, RARB or RBRB, SB0, ADF, and STBA or STBB to be generated during time T4T5. These signals in combination with signal TR2 from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB) incremented by one and transferred to the T-bus (signals SB0 and ADF), and stored in the A- or B-register (signal STBA or STBB).

4-375. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-376. Test Procedure. To test the INA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002004 (INA instruction) or 006004 (INA instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the INA instruction, or the LOAD B switch if testing the INB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001000 in them and the A-register will have 000001 in it.

h. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the RUN switch.

4-377. The computer is now in the run mode executing the INA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-66. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-44. INA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3	T4 Read A/B to R Bus Read "1" to S Bus ADF Store T Bus in A/B If C16: Set E	T5 *Combination of SSA/B, SLA/B, and RSS is a special case; see text.		

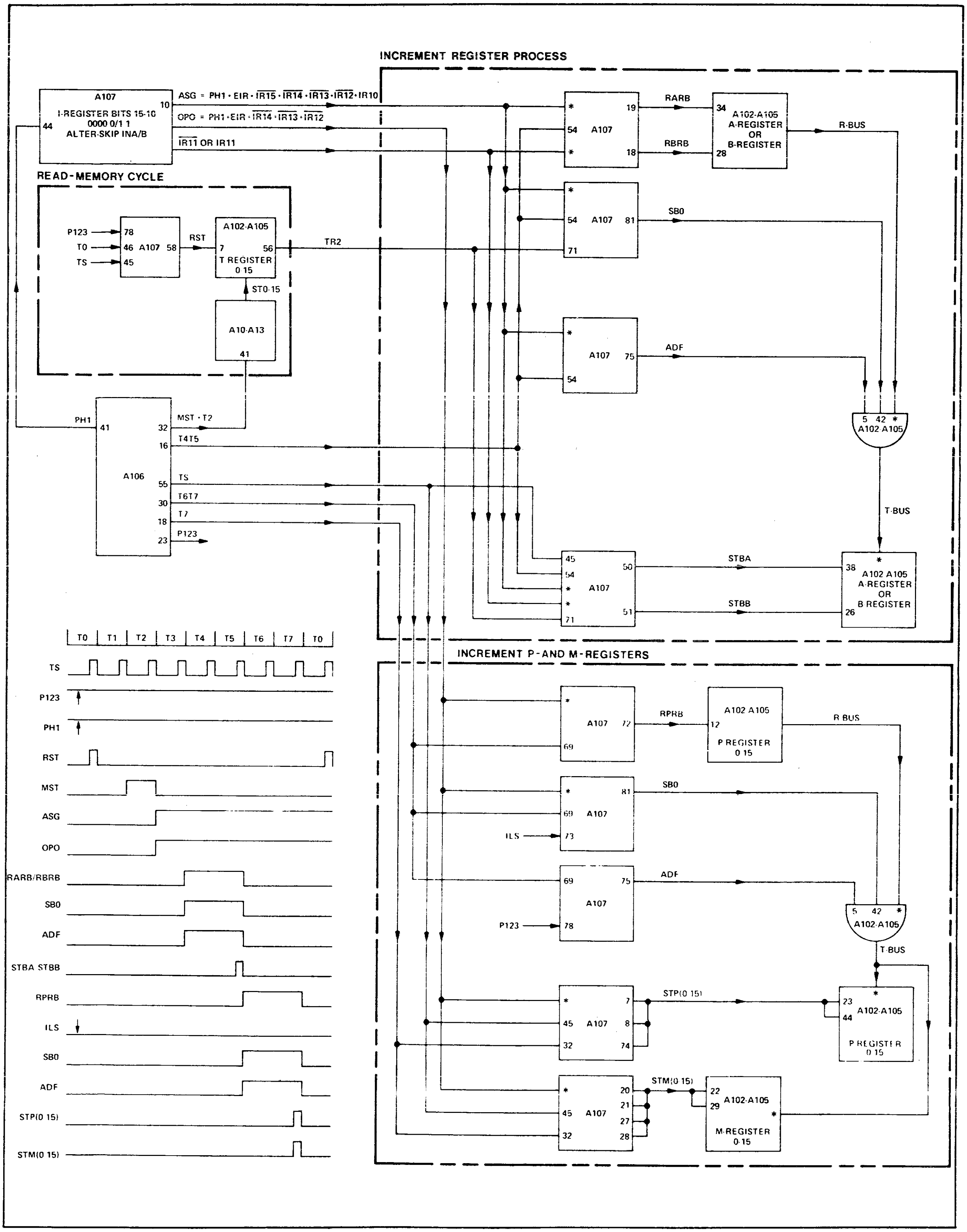

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Figure 4-66. INA/B Instruction Processing Circuits, Servicing Diagram

4-378. SZA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SZA/B instruction. Processing operations are summarized in table 4-45. Point-to-point signal flow during phase 1 is shown in figure 4-67.

4-379. Description. The SZA/B instruction reads a number from the A- or B-register and checks it for an all "zero" condition. If all the bits of the number are zero, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If all the bits of the number are not zero, the program continues with the next instruction in sequence.

4-380. The SZA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 or 00011 in the I-register causes signals ASG, OP0, RARB or RBRB, and ADF to be generated during times T3 through T5. These signals in combination with signals $\overline{TR0}$ and $\overline{TR1}$ from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), transferred to the T-bus (signal ADF), and the Carry FF (CFF) to set at time T5TS if all the bits of the T-bus are equal to zero (TAN gates signals). Signal CFF causes signal C0 to be generated at time T6T7.

4-381. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. In combination with signal C0 will cause the P- and M-register to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-382. Test Procedure. To test the SZA/B instruction circuits, proceed as follows:

Note

> If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002002 (SZA instruction) or 006002 (SZB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 (all bits zero test) and press and release the LOAD A switch if testing the SZA instruction, or the LOAD B switch if testing the SZB instruction. (Substitute 000001 to 000000 for all bits not zero test.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001001 in them.

h. Repeat step g above. The P- and M-registers should have 001000 in them.

i. At the computer front panel, press and release the RUN switch.

4-383. The computer is now in the run mode executing the SZA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-67. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

> Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-45. SZA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3	T4	T5: Read A/B to R Bus IOF R Bus to T Bus Set Carry if: T Bus all zeros and TR0 = 0, or T Bus all ones and TR0 = 1		

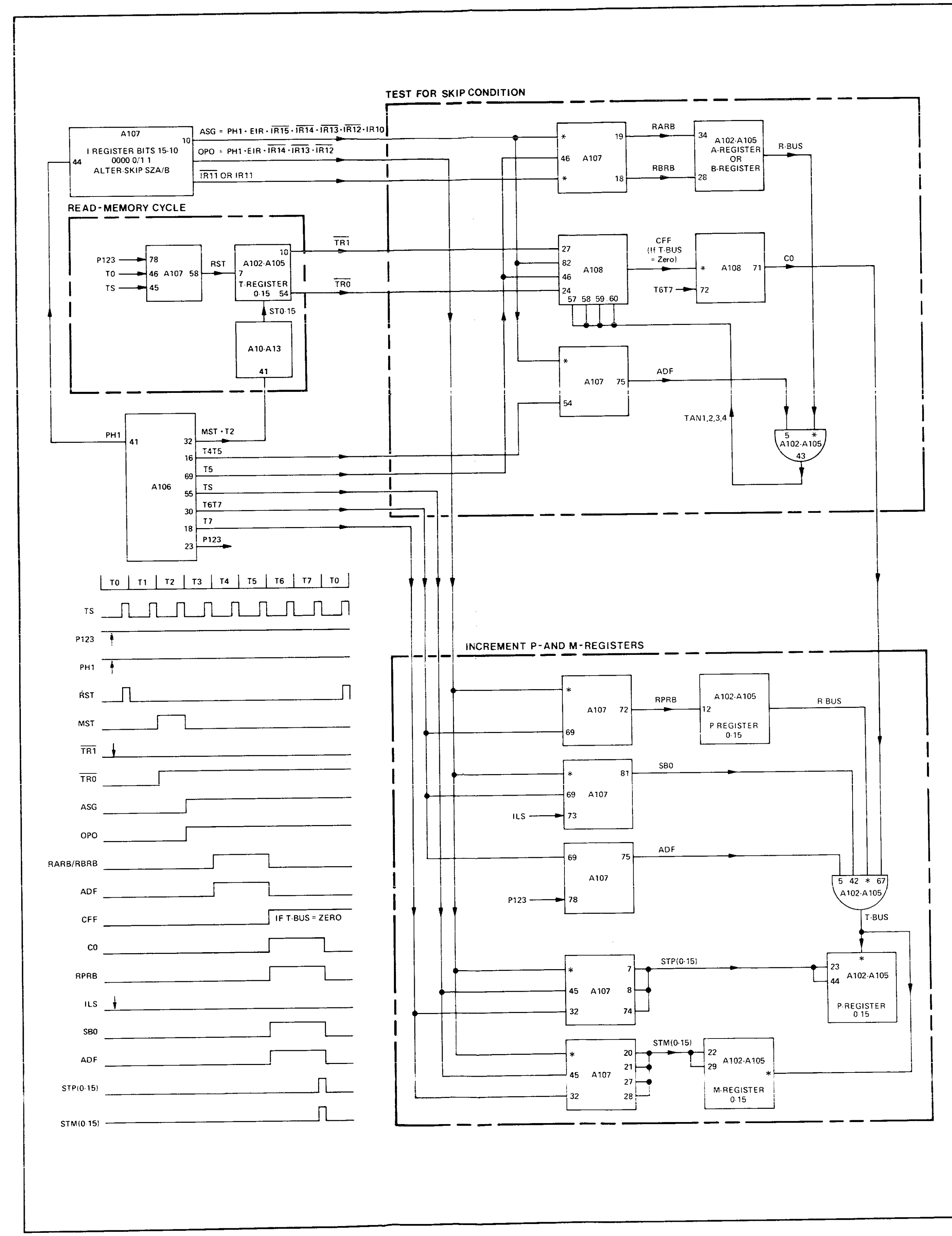

Figure 4-67. SZA/B Instruction Processing Circuits, Servicing Diagram

4-384. RSS INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the RSS instruction.

4-385. Description. The RSS instruction, when processed alone (not in combination with any of the other ASG skip instructions), or when processed in combination with any of the ASG non-skip instructions, causes an unconditional skip to occur. Normally the other ASG skip instructions will cause a skip to occur when a zero condition (RB15 or RB0 are false) is sensed. When the RSS instruction is used in combination with any of the other ASG skip instructions a skip will occur when a non-zero condition (RB15 or RB0 are true) is sensed. Only when used in combination with the SSA/B and SLA/B instructions, must bits 15 and 0 both be true for the skip to occur. At the end of the machine cycle the P-register number is incremented by one if no skip condition has been generated, or is incremented by two if a skip condition has been generated. The incremented number is then stored in the P- and M-registers and the next phase is set.

4-386. The RSS instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 00001 or 00011 in the I-register causes signals ASG and OP0 to be generated during time T3. These signals in combination with signal TR0 from the T-register cause the Carry FF (CFF) to be set. Signal CFF causes signal C0 to be generated at time T6T7.

4-387. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-388. Test Procedure. The RSS instruction is tested in combination with the SEZ instruction (paragraph 4-354). To test the RSS instruction circuits proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002041 (SEZ and RSS instructions) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the RUN switch.

4-389. The computer is now in the run mode executing the SEZ and RSS instructions in location 001000. The signal C0 will be generated if the E-register is set. Using a dual-trace oscilloscope, check the signals shown in figure 4-63. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

4-390. INPUT/OUTPUT INSTRUCTION PROCESSING CIRCUITS.

4-391. The circuits that process the 17 input/output instructions are shown in figures 4-68 through 4-79. Input/output instructions are used in the computer program to address a selected input/output location (select code) and specify a desired data transfer or control operation involving the select code which is addressed. (Four instructions included in the input/output instruction set are used to perform control operations involving the overflow register. For this reason, these four instructions are sometimes considered to be part of the register reference instruction set. However, for troubleshooting purposes they are treated as input/output instructions because they use the input/output instruction format.) Input/output instruction formats are shown in figure 4-1. The paragraphs which follow describe the purpose and use of each instruction, and explain how the processing circuits implement and execute the instructions. Tables summarizing the processing operations, and servicing diagrams showing signal flow and timing within the processing circuits, are included for reference during explanation and troubleshooting. Suggested troubleshooting test procedures are presented for each instruction.

4-392. HLT INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the HLT instruction. Processing operations are summarized in table 4-46. Point-to-point signal flow during phase 1 is shown in figure 4-68.

4-393. Description. The HLT instruction clears RUN FF 1 and RUN FF 2, turns off the RUN indicator, turns on the HALT indicator and the FETCH indicator, and enables the front panel switches. It also causes the A- or B-register data to be transferred to the T-bus but makes no use of this data. It clears any addressed I/O device FLAG FF if bit 9 of the instruction (signal TR9) is true. At the end of the machine cycle, the P-register number is incremented by one and stored in the P- and M-registers and phase 1 is set.

4-394. The HLT instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 (IR15 through IR10) in the I-register causes signals IOG, OPO, and RARB or RBRB to be generated during time T3 through T5. These signals in combination with signals $\overline{TR6}$, $\overline{TR7}$, and $\overline{TR8}$ from the T-register cause the signal HIN to be generated at time T3 which clears the RUN FF 1 (RF1) at time T5. Clearing RUN FF 1 causes PH1 FF to set and the FETCH indicator to go on allowing RUN FF 2 (RF2) to clear at time T7S. Clearing RUN FF 2 causes the HALT indicator to go on, the RUN indicator to go off, and the front panel switches to be enabled. During times T3 through T5 the A- or B-register data is read onto the R-bus (signal RARB or RBRB), and transferred to the T-bus (signal $\overline{IOF}$) but is not used. During time T4 the INTERRUPT SYSTEM ENABLE FF and the I/O device FLAG FF whose address appears in the last six bits of the HLT instruction are cleared. (signals TR9 and CLF).

4-395. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer stops ready to process the next instruction.

4-396. Test Procedure. To test the HLT instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 103001 (HLT instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the RUN switch. The computer will appear to remain in the halt mode.

4-397. Using a dual-trace oscilloscope check the signals shown in figure 4-68 at the backplane connectors or at a specific card by using the extender card and the extender cable. The signals are generated each time the RUN switch is pressed. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SBO is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-46. HLT Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR				P + 1 to P, M Reset Run FF Set PH1	

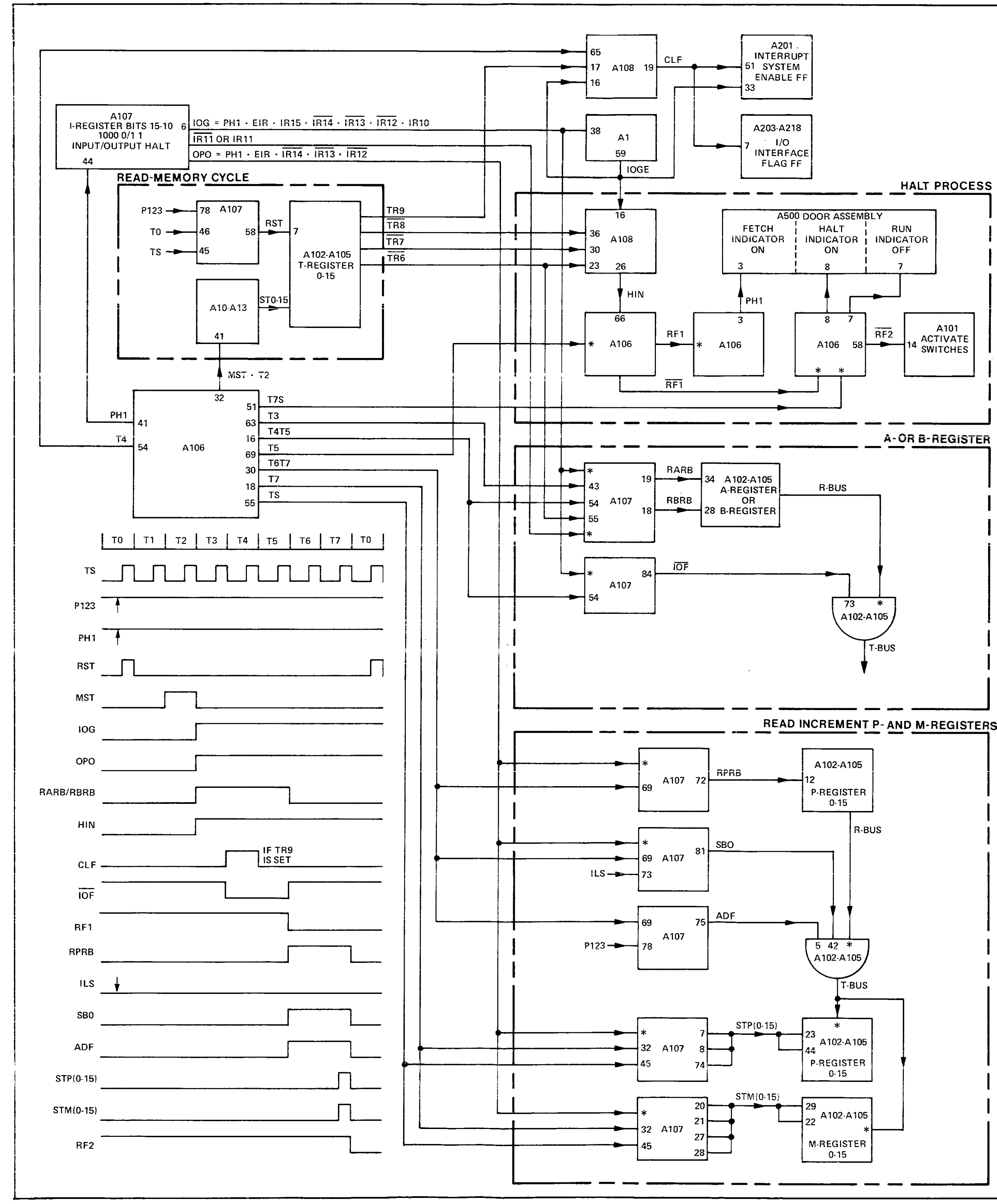

Figure 4-68. HLT Instruction Processing Circuits, Servicing Diagram

4-398. STF INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the STF instruction. Processing operations are summarized in table 4-47. Point-to-point signal flow during phase 1 is shown in figure 4-69.

4-399. Description. The STF instruction sets the flag flip-flop addressed in the select code portion of the instruction. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the $\overline{\text{TR8}}$, $\overline{\text{TR7}}$, and TR6 signals from the T-register cause the STF signal to be generated at time T3. The IOGE signal in combination with the TR5, TR4, TR3, TR2, TR1, and TR0 signals from the T-register are used to address the desired computer or interface flip-flop. The STF signal then sets the flip-flop.

4-400. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.
ready to process the next instruction.

4-401. Test Procedure. To test the STF instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1021XX (STF instruction) and press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

4-402. The computer is now in the run mode executing the STF instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-69. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-47. STF Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR to IR	Set Flag: Select Code			P + 1 to P, M Set next phase	

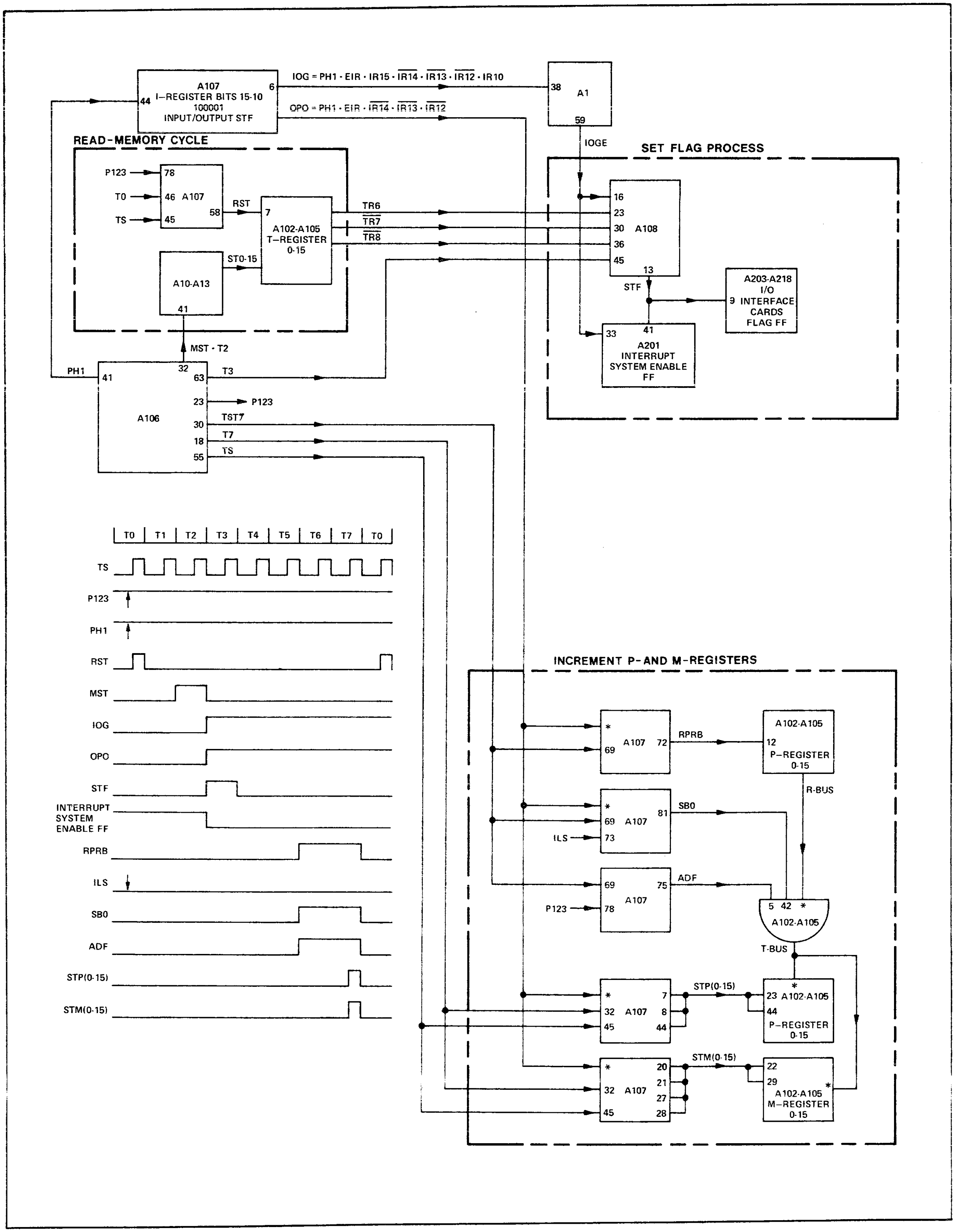

Figure 4-69. STF Instruction Processing Circuits, Servicing Diagram

4-403. CLF INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CLF instruction. Processing operations are summarized in table 4-48. Point-to-point signal flow during phase 1 is shown in figure 4-70.

4-404. Description. The CLF instruction clears the Flag flip-flop addressed in the select code portion of the instruction. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the TR9 signal from the T-register causes the CLF signal to be generated at time T4. The IOGE signal in combination with the TR5, TR4, TR3, TR2, TR1, and TR0 signals from the T-register are used to address the desired computer or interface flip-flop. The CLF signal then clears the flip-flop.

4-405. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-406. Test Procedure. To test the CLF instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1031XX (CLF instruction) and press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

4-407. The computer is now in the run mode executing the CLF instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-70. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-48. CLF Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR to IR	Set Flag: Select Code	Clear Flag: Select Code		P + 1 to P, M Set next phase	

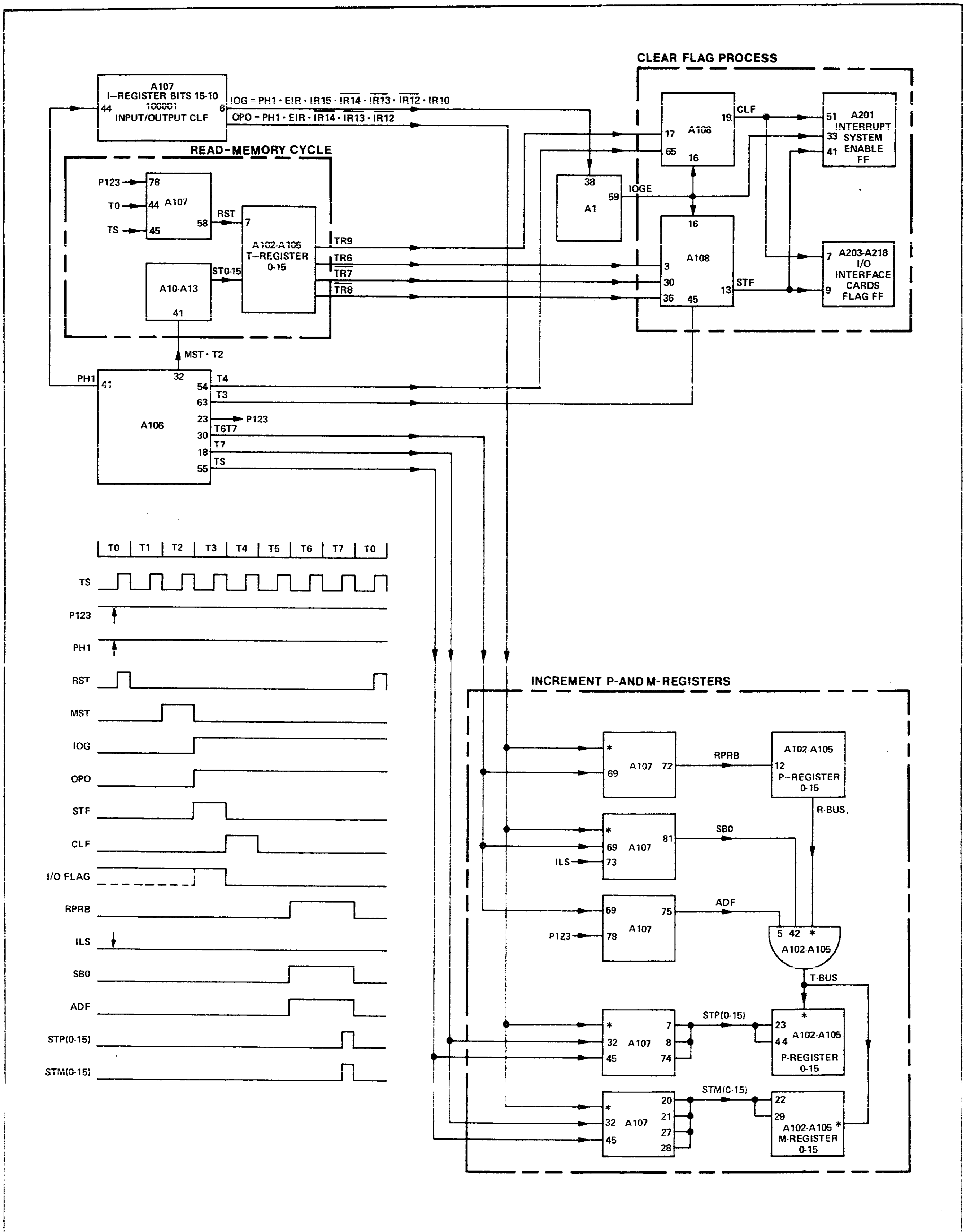

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Figure 4-70. CLF Instruction Processing Circuits, Servicing Diagram

4-408. SFC INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SFC instruction. Processing operations are summarized in table 4-49. Point-to-point signal flow during phase 1 is shown in figure 4-71.

4-409. Description. The SFC instruction causes the computer program to skip the next instruction if the addressed Flag flip-flop is cleared. This allows the computer to test the status of the input/output interface under program control. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 in the I-register causes the IOG and OPO signals to be generated during times T3 through the following time T0. The IOGE signal together with the $\overline{\text{TR8}}$, TR7, and $\overline{\text{TR6}}$ signals cause the SFC signal to be generated. The SFC signal is routed to the interface cards. The state of the addressed Flag flip-flop is compared with the SFC signal. If the Flag flip-flop is not set, the SKF signal is generated. If the SKF signal is generated it will set the Carry flip-flop at time T4TS. At time T6T7 the set Carry flip-flop will generate the CO signal.

4-410. The CO signal is used with the SBO signal to increment the P- and M-registers by two instead of the normal one. This causes the computer to skip the next program instruction. If the CO signal is not generated, the normal increment by one operation will occur. During times T6 and T7 the RPRB, SBO, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-411. Test Procedure. To test the SFC instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1022XX to test the SFC instruction. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 027000 (JMP instruction). Press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

f. At the computer front panel, press and release the RUN switch.

4-412. The computer is now in the run mode executing the SFC instruction. The state of the addressed Flag flip-flop is being tested. Check the signals shown in figure 4-71 using a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SBO is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-49. SFC Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR to IR	SFC to Interface	SKF sets Carry FF		P + 1 + Carry to P, M Set next phase	

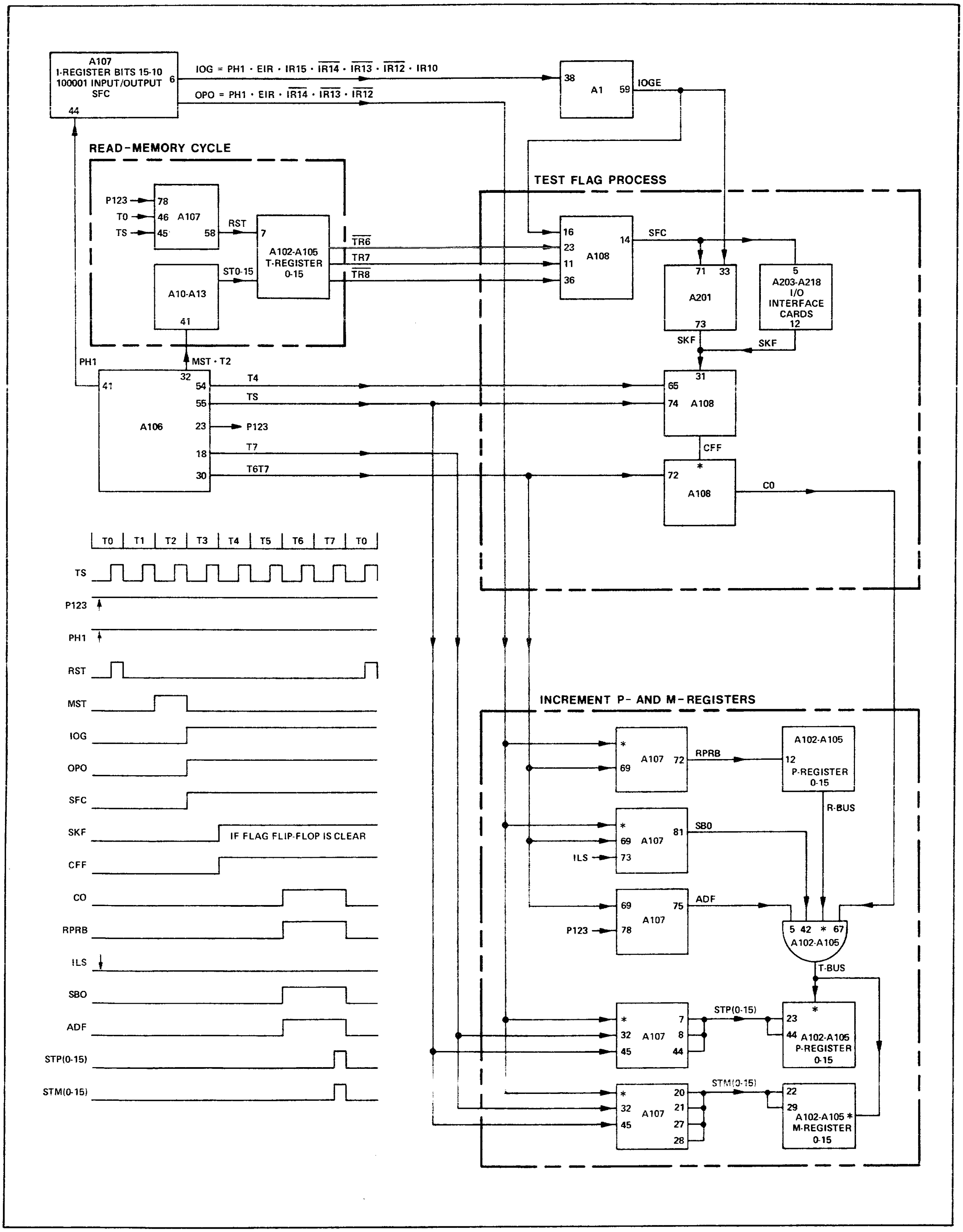

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Figure 4-71. SFC Instruction Processing Circuits, Servicing Diagram

4-413. SFS INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SFS instruction. Processing operations are summarized in table 4-50. Point-to-point signal flow during phase 1 is shown in figure 4-72.

4-414. Description. The SFS instruction causes the computer program to skip the next instruction if the addressed Flag flip-flop is set. This allows the computer to test the status of the input/output interface under program control. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 in the I-register causes the IOG and OPO signals to be generated during times T3 through the following time T0. The IOGE signal together with the $\overline{TR8}$, TR7, and TR6 signals cause the SFS signal to be generated. The SFS signal is routed to the interface cards. The state of the addressed Flag flip-flop is compared with the SFS signal. If the Flag flip-flop is set, the SKF signal is generated. If the SKF signal is generated it will set the Carry flip-flop at time T4TS. At time T6T7 the set Carry flip-flop will generate the C0 signal.

4-415. The C0 signal is used with the SB0 signal to increment the P- and M-registers by two instead of the normal one. This causes the computer to skip the next program instruction. If the C0 signal is not generated, the normal increment by one operation will occur. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-416. Test Procedure. To test the SFS instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1023XX to test the SFS instruction. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 027000 (JMP instruction). Press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

f. At the computer front panel, press and release the RUN switch.

4-417. The computer is now in the run mode executing the SFS instruction. The state of the addressed Flag flip-flop is being tested. Check the signals shown in figure 4-72 using a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-50. SFS Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	IR to IR	SFS to Interface	SKF sets Carry FF		P + 1 + Carry to P, M Set next phase	

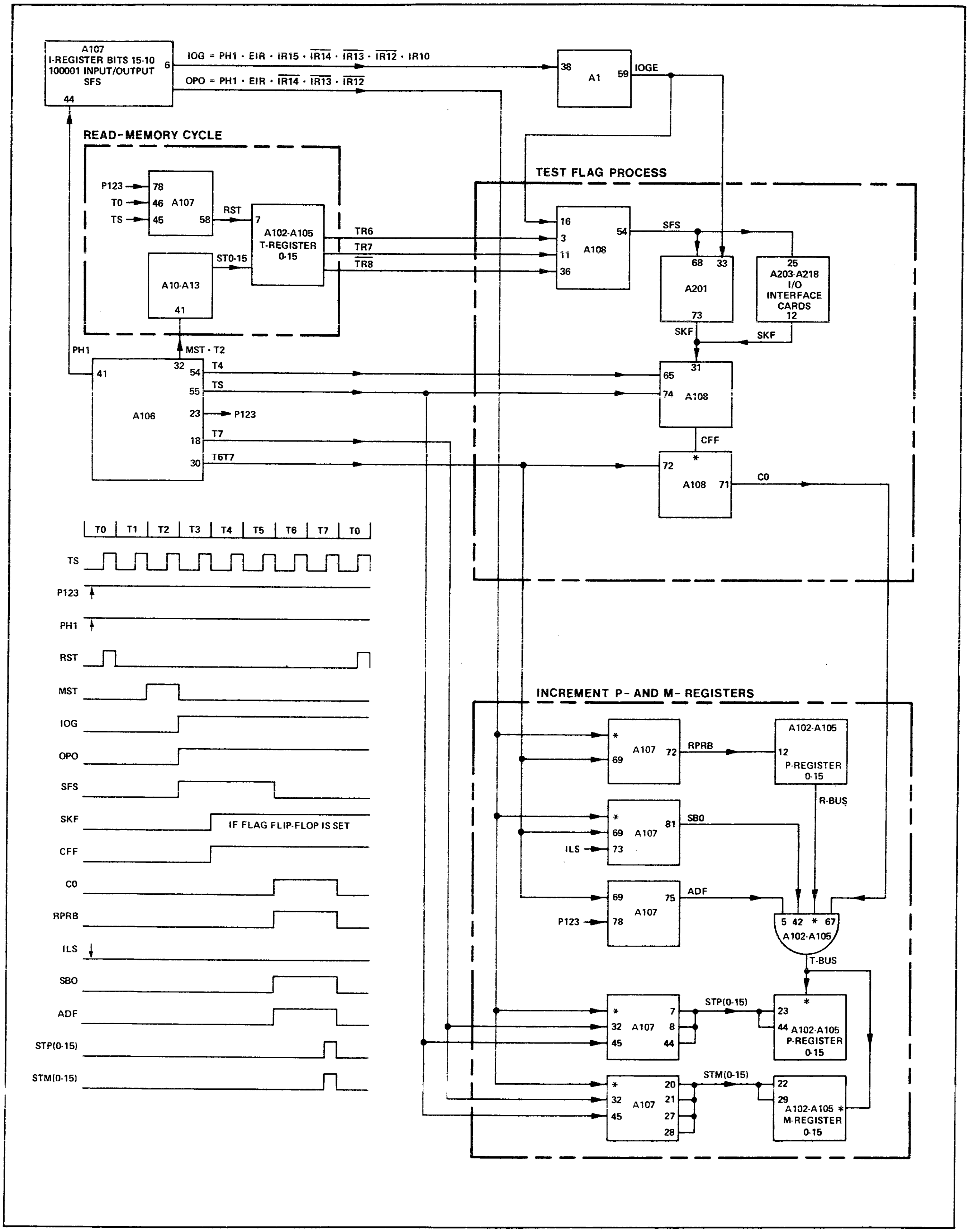


Figure 4-72. SFS Instruction Processing Circuits, Servicing Diagram

4-418. MIA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the MIA/B instruction. Processing operations are summarized in table 4-51. Point-to-point signal flow during phase 1 is shown in figure 4-73.

4-419. Description. The MIA/B instruction merges input data into the 8 least significant bits of a specified register ($\overline{\text{IR11}}$ specifies the A-register and IR11 specifies the B-register). If bit nine of the T-register (TR9) is true, the Flag flip-flop on the addressed interface card will be cleared. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the TR9 signal (if this bit is set) from the T-register causes the CLF signal to be generated at time T4. The IOGE signal in combination with the TR8, and $\overline{\text{TR7}}$ signals from the T-register causes the IOI signal to be generated during times T4 and T5. The IOG signal causes the $\overline{\text{IOF}}$ signal to be generated during times T4 and T5. The IOG, $\overline{\text{TR6}}$, and $\overline{\text{IR11}}$/IR11 signals cause the appropriate RARB or RBRB signal to be generated during times T4 and T5.

4-420. The IOI, $\overline{\text{IOF}}$, and RARB or RBRB signals route the input data onto the computer bus lines and combine it with the contents of the indicated register. The IOI signal reads the data from the interface card onto the IOBI lines and then onto the S-Bus lines. The RARB or RBRB signal reads the data in the indicated register onto the R-Bus lines. The $\overline{\text{IOF}}$ signal combines the data on the R- and S-Bus lines and reads the merged data onto the T-bus lines. At time TS of time T5, the IOG and TR8 and $\overline{\text{TR7}}$ signals generate the STBA or STBB signal which stores the data on the T-bus lines into the indicated A- or B-register.

4-421. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-422. Test Procedure. To test the MIA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. Set the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1024XX. This will test the MIA instruction. To test the MIB instruction use 1064XX. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

e. At the computer front panel, press and release the RUN switch.

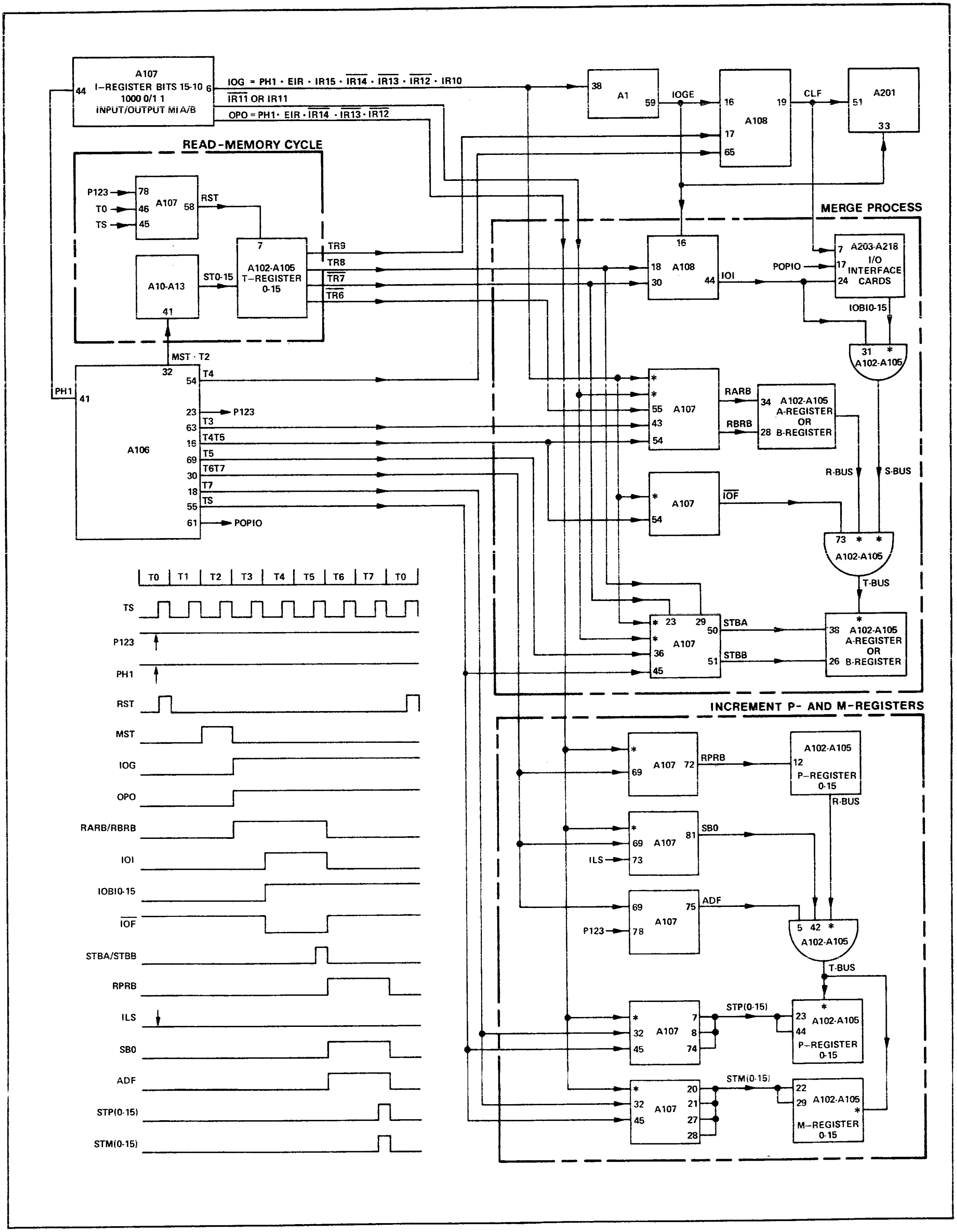
4-423. The computer is now in the run mode executing the MIA instruction. The contents of the addressed input/output device data register will be loaded into the A-register. By using select code 01 and keying data into the SWITCH REGISTER, the bit pattern of the data may be easily modified. Check the signals shown in figure 4-73 with a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-51. MIA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR to IR		Read A/B to R Bus Buffer to S Bus IOF Store T Bus in A/B If TR9 = 1, CLF		P + 1 to P, M Set next phase	



2019-83

Figure 4-73. MIA/B Instruction Processing Circuits, Servicing Diagram

4-424. LIA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the LIA/B instruction. Processing operations are summarized in table 4-52. Point-to-point signal flow during phase 1 is shown in figure 4-74.

4-425. Description. The LIA/B instruction transfers input data into a specified register ($\overline{\text{IR11}}$ specifies the A-register and IR11 specifies the B-register). If bit nine of the T-register (TR9) is true, the Flag flip-flop on the addressed interface card will be cleared. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 in the I-register causes the signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the TR9 signal (if this bit is set) from the T-register causes the CLF signal to be generated at time T4. The IOGE signal in combination with the TR8, and $\overline{\text{TR7}}$ signals from the T-register causes the IOI signal to be generated during times T4 and T5. The IOG signal causes the $\overline{\text{IOF}}$ signal to be generated during times T4 and T5.

4-426. The IOI, $\overline{\text{IOF}}$, and STBA or STBB signals route the input data onto the computer bus lines and store it in the indicated register. The IOI signal reads the data from the interface card onto the IOBI lines and then onto the S-Bus lines. The $\overline{\text{IOF}}$ signal transfers the data on the S-Bus lines to the T-Bus lines. At time TS of time T5, the IOG, $\overline{\text{IR11}}$ or IR11, TR8 and $\overline{\text{TR7}}$ signals generate the STBA or STBB signal which stores the data on the T-Bus lines into the indicated A- or B-register.

4-427. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-428. Test Procedure. To test the LIA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1025XX. This will test the LIA instruction. To test the LIB instruction use 1065XX. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

e. At the computer front panel, press and release the RUN switch.

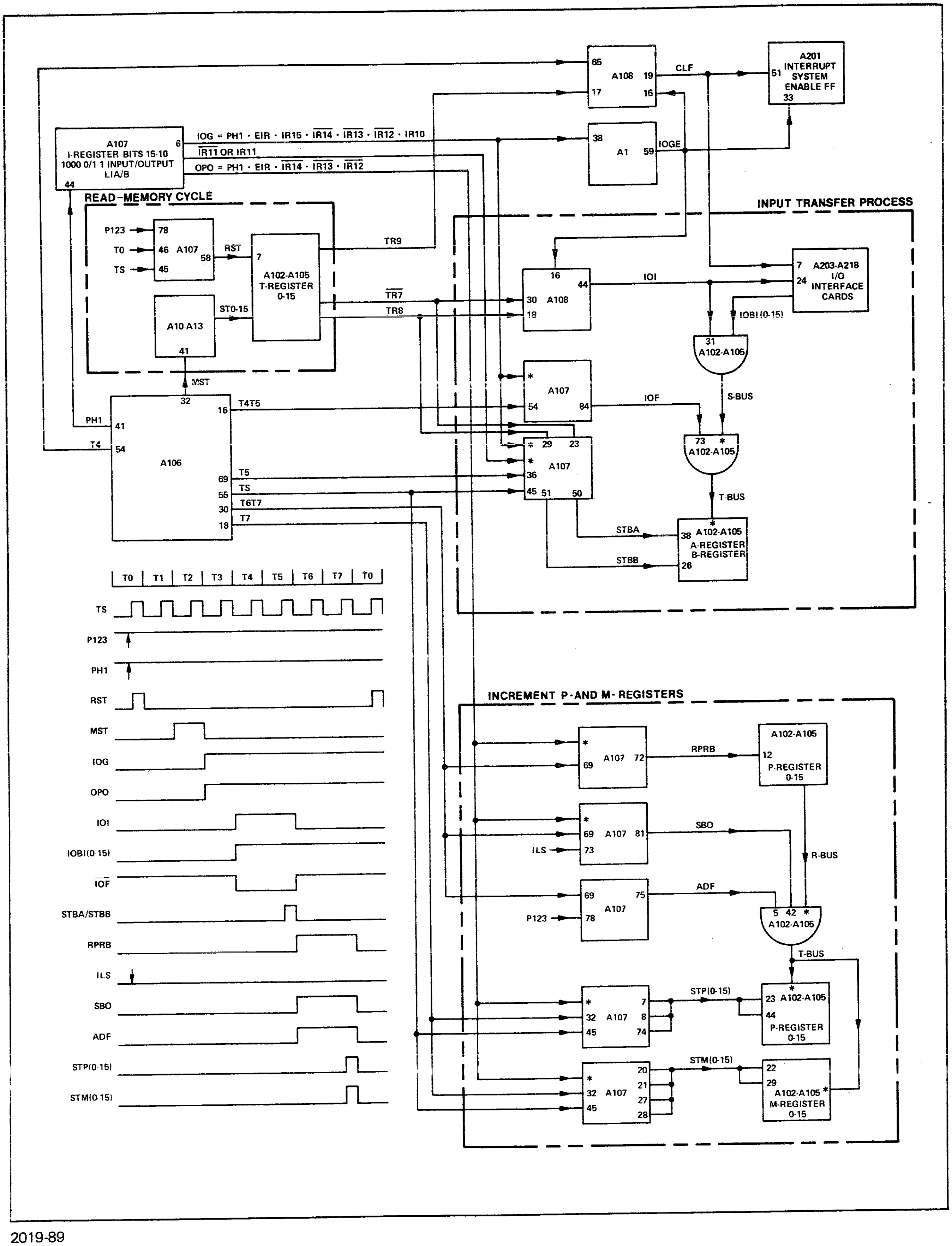
4-429. The computer is now in the run mode executing the LIA instruction. The contents of the addressed input/output device data register will be loaded into the A-register. By using select code 01 and keying data into the SWITCH REGISTER, the bit pattern of the data may be easily modified. Check the signals shown in figure 4-74 with a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1 and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-52. LIA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR to IR		Buffer to S Bus IOF Store T Bus in A/B If TR9 = 1, CLF		P + 1 to P, M Set next phase	



2019-89

Figure 4-74. LIA/B Instruction Processing Circuits, Servicing Diagram

4-430. OTA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the OTA/B instruction. Processing operations are summarized in table 4-53. Point-to-point signal flow during phase 1 is shown in figure 4-75.

4-431. Description. The OTA/B instruction transfers output data from a specified register to an output device ($\overline{\text{IR11}}$ specifies the A-register and IR11 specifies the B-register). If bit nine of the T-register (TR9) is true, the Flag flip-flop on the addressed interface card will be cleared. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 in the I-register causes the signals IOG and OPO to be generated during times T3 through the following time T0. The IOG, $\overline{\text{TR6}}$, and $\overline{\text{IR11}}$ or IR11 signals cause the appropriate RARB or RBRB signal to be generated at time T3. The IOGE signal in combination with the TR9 signal (if this bit is set) from the T-register causes the CLF signal to be generated at time T4. The IOGE signal in combination with the TR8, TR7, and $\overline{\text{TR6}}$ signals from the T-register causes the IOO and IOCO signals to be generated during times T4 and T5.

4-432. The RARB or RBRB, IOCO, and IOO signals route the output data onto the computer bus lines and then to the addressed output interface card. The RARB or RBRB signal reads the data from the register onto the R-bus lines. The IOCO signal transfers the data to the IOBO lines. The IOGE signal together with T-register bits TR0 through TR5 provide select code signals to the interface card. The IOO signal transfers the data on the IOBO lines onto the addressed interface card.

4-433. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-434. Test Procedure. To test the OTA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1026XX. This will test the OTA instruction. To test the OTB instruction use 1066XX. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

e. At the computer front panel, press and release the RUN switch.

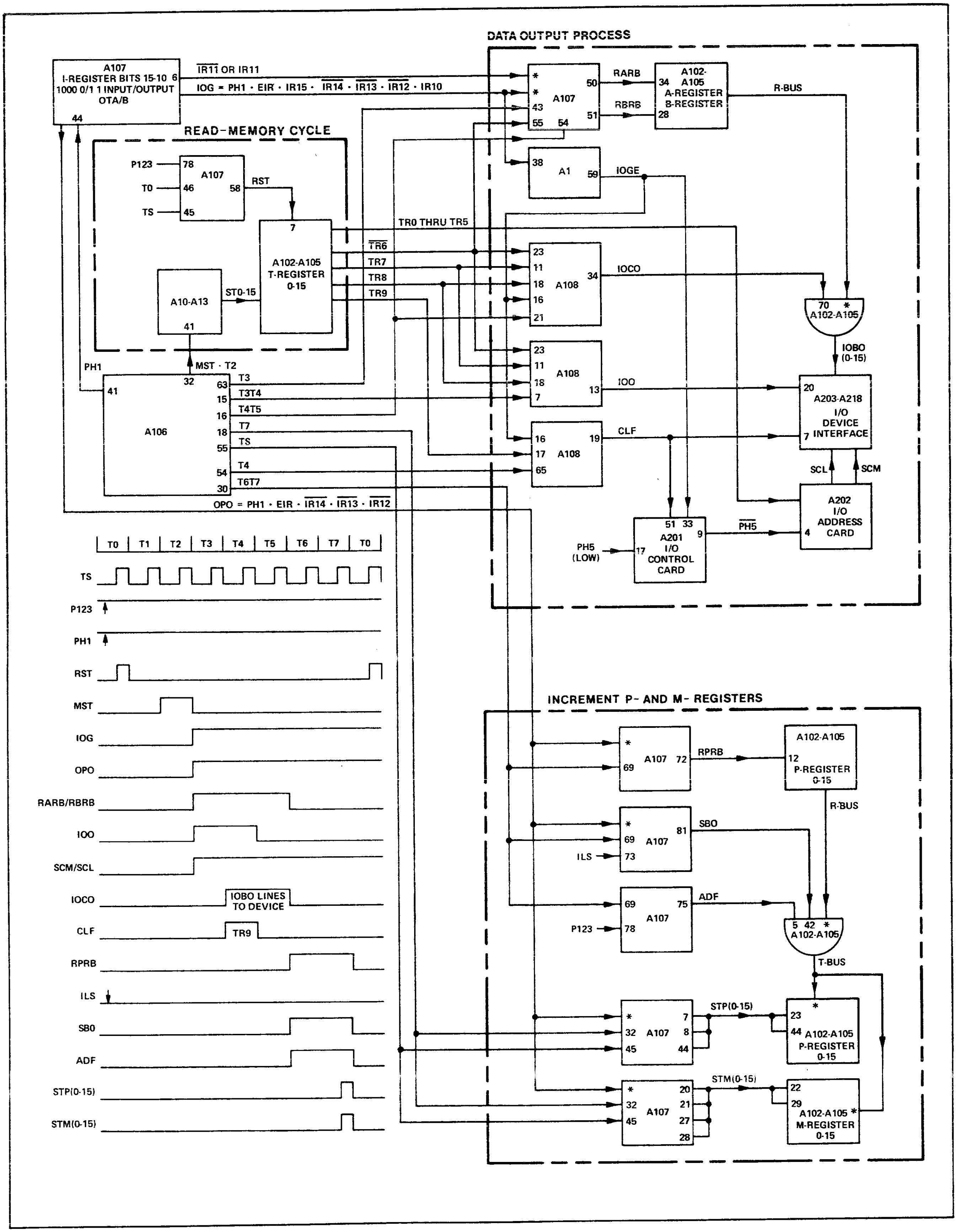
4-435. The computer is now in the run mode executing the OTA instruction. The contents of the A-register will be loaded into the addressed input/output device data register. Check the signals shown in figure 4-75 with a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-53. OTA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR to IR		Read A/B to R Bus R Bus to Buffer If TR9 = 1, CLF		P + 1 to P, M Set next phase	



2019-90

Figure 4-75. OTA/B Instruction Processing Circuits, Servicing Diagram

4-436. STC/CLC INSTRUCTIONS. The following paragraphs provide a description and test procedure for the circuits that process the STC and CLC instructions. Processing operations are summarized in table 4-54. Point-to-point signal flow during phase 1 is shown in figure 4-76.

4-437. Description. The STC instruction sets the addressed Control flip-flop. The CLC instruction clears the addressed Control flip-flop. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 in the I-register causes the IOG and OPO signals to be generated during times T3 through the following time T0. The IOGE signal together with the $\overline{\text{TR11}}$ or TR11, TR8, TR7, and TR6 signals generate the STC or CLC signals. A true TR11 bit will cause the CLC instruction to be generated. A false TR11 bit will cause the STC signal to be generated. If the TR9 bit is true the IOGE signal will cause a CLF signal to be generated at time T4. The STC or CLC signals together with the select code signals cause the Control flip-flop on the addressed interface card to be set or cleared respectively. If the CLF signal has been generated the Flag flip-flop will also be cleared.

4-438. During the T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-439. Test Procedure. To test the STC and CLC instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1027XX. This will test the STC instruction. To test the CLC instruction, use 1067XX. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

e. At the computer front panel, press and release the RUN switch.

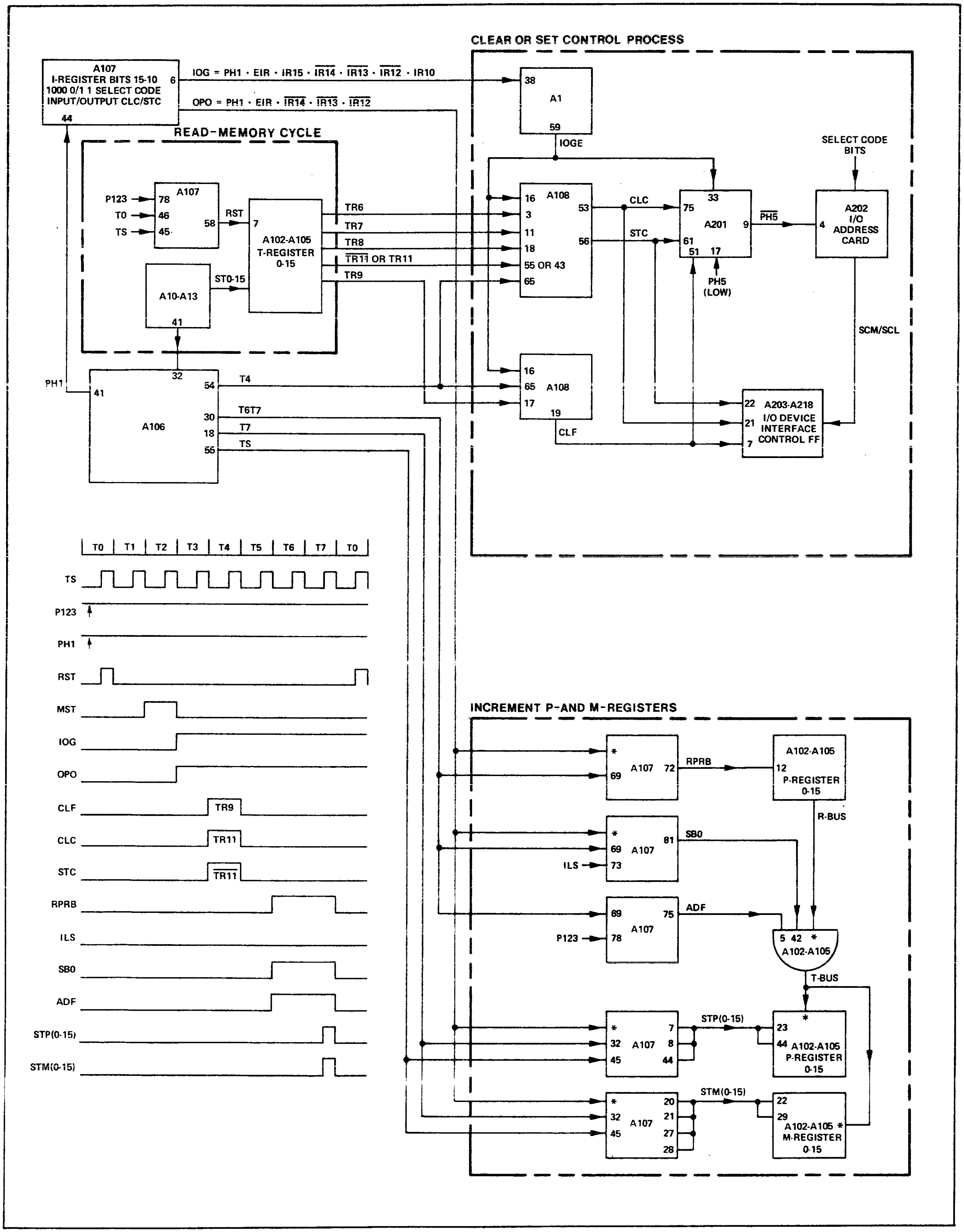
4-440. The computer is now in the run mode executing the STC (CLC) instruction. The addressed Control flip-flop will be set (cleared). Check the signals shown in figure 4-76 with a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use this as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-54. STC/CLC Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH STC	1	Clear TR	Clear IR	TR to IR	Set Control (Sel. Code			P + 1 to P, M Set next phase	
FETCH CLC	1	Clear TR	Clear IR	TR to IR	Clr. Control (Sel. Code)			P +1 to P, M Set next phase	



2019-91

Figure 4-76. STC/CLC Instruction Processing Circuits, Servicing Diagram

4-441. STO INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the STO instruction. Processing operations are summarized in table 4-55. Point-to-point signal flow during phase 1 is shown in figure 4-77.

4-442. Description. The STO instruction sets the Overflow register (O-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the $\overline{TR8}$, $\overline{TR7}$, and TR6 signals from the T-register cause the STF signal to be generated at time T3. The IOGE signal in combination with the $\overline{TR5}$, $\overline{TR4}$, $\overline{TR3}$, $\overline{TR2}$, $\overline{TR1}$, and TR0 signals from the T-register cause the IOS signal to be generated. At time T3TS the IOS and STF signals set the Overflow register and generate the overflow indication on the front panel.

4-443. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-444. Test Procedure. To test the STO instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 102101 (STO instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

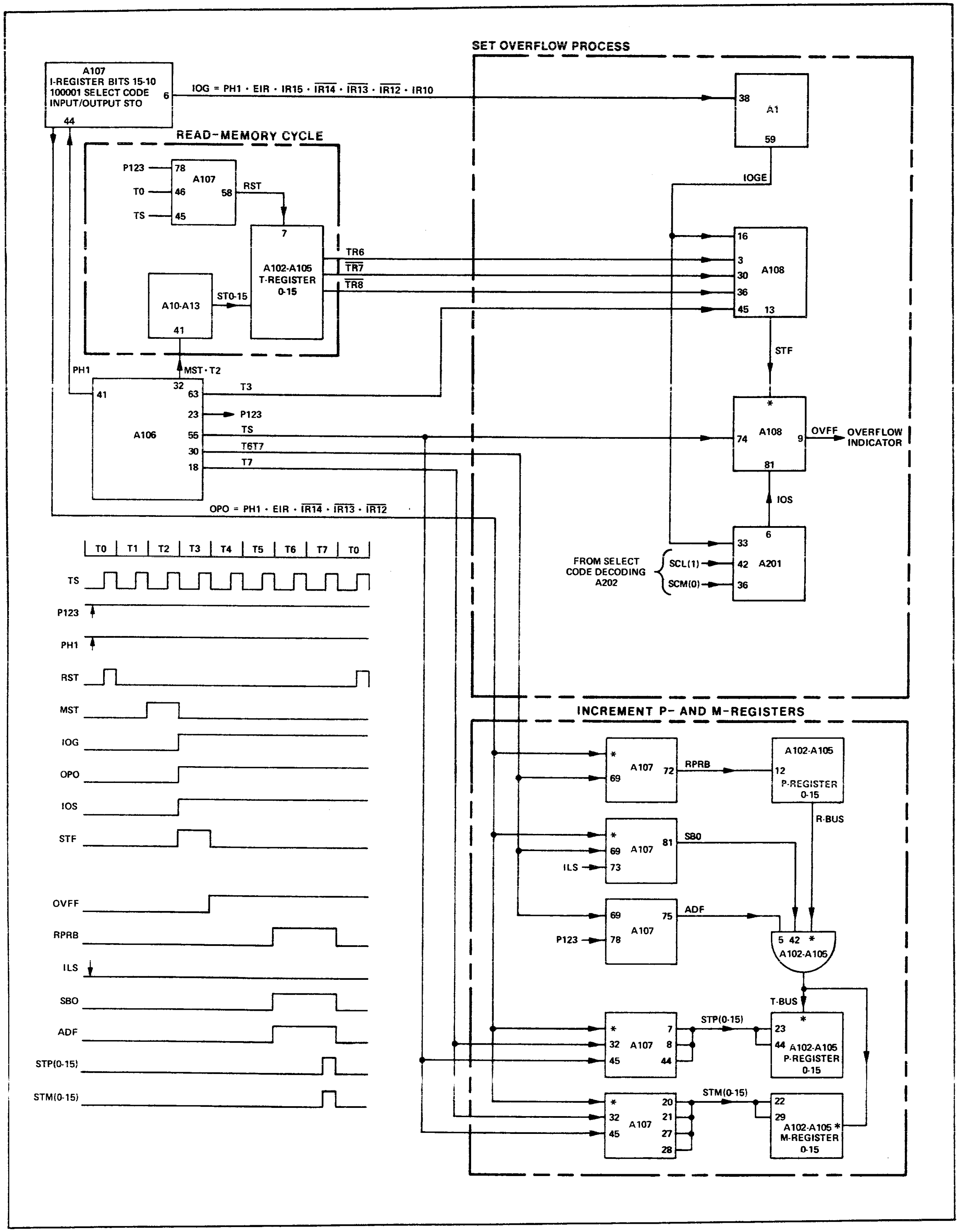
4-445. The computer is now in the run mode executing the STO instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-77. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SBO is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-55. STO Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR to IR	STF to Overflow FF			P + 1 to P, M Set next phase	



2019-82

Figure 4-77. STO Instruction Processing Circuits, Servicing Diagram

4-446. CLO INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CLO instruction. Processing operations are summarized in table 4-56. Point-to-point signal flow during phase 1 is shown in figure 4-78.

4-447. Description. The CLO instruction clears the Overflow register (O-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the TR9 signal from the T-register causes the CLF signal to be generated at time T4. The $\overline{\text{IOGE}}$ signal in combination with the $\overline{\text{TR5}}$, $\overline{\text{TR4}}$, $\overline{\text{TR3}}$, $\overline{\text{TR2}}$, $\overline{\text{TR1}}$, and TR0 signals from the T-register cause the IOS signal to be generated. At time T4TS the IOS and CLF signals clear the Overflow register and remove the overflow indication on the front panel.

4-448. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-449. Test Procedure. To test the CLO instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 103101 (CLO instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

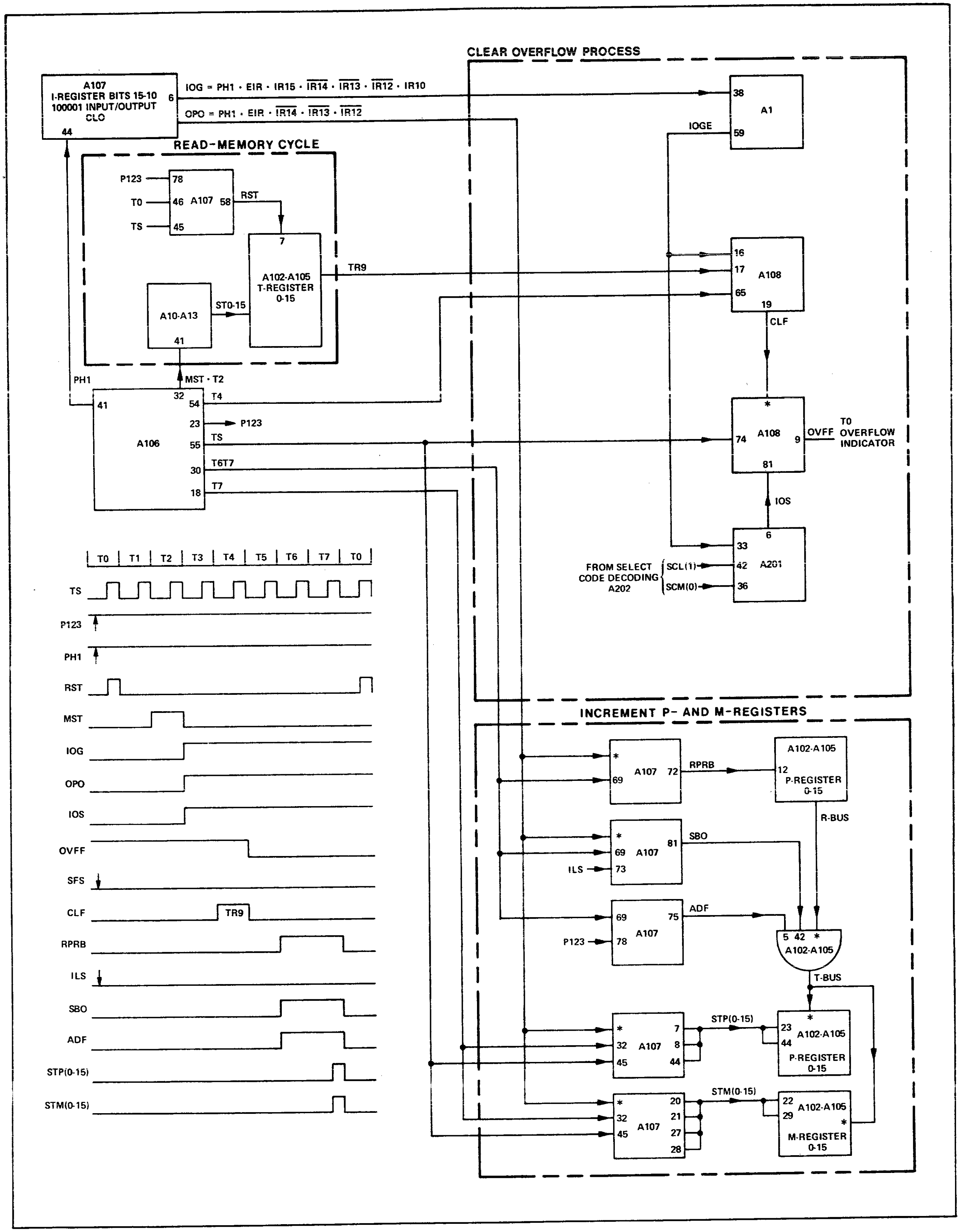
4-450. The computer is now in the run mode executing the CLO instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-78. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-56. CLO Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR to IR		CLF to Overflow FF		P + 1 to P, M Set next phase	



2019-81

Figure 4-78. CLO Instruction Processing Circuits, Servicing Diagram

4-451. SOS/SOC INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process SOS and SOC instructions. Processing operations are summarized in table 4-57. Point-to-point signal flow during phase 1 is shown in figure 4-79.

4-452. Description. The SOS instruction causes the computer to skip the next program instruction if the Overflow flip-flop is set. The SOC instruction causes the computer to skip the next program instruction if the Overflow flip-flop is clear. The SOS and SOC instructions are read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 in the I-register causes the IOG and OPO signals to be generated during times T3 through the following time T0. At time T3 the $\overline{\text{TR8}}$, TR7, and TR6 signals together with the IOGE signal generate the SFS signal. If TR6 is false for the SOC instruction, the SFC signal will be generated instead. The IOGE signal together with the select code bits cause the IOS signal to be generated.

4-453. If the Overflow flip-flop is set and the SOS instruction is being executed, the SFS and IOS signals will generate the SKF signal. If the Overflow flip-flop is clear and the SOC instruction is being executed, the SFC and IOS signals will generate the SKF signal. If TR9 has been set, the CLF signal will be generated at time T4. The CLF signal will clear the Interrupt Control flip-flop on the I/O Control card. This prevents I/O interrupts during normal CLF instructions and is coincidental to the SOS and SOC instructions. The Interrupt Control flip-flop is set during T7TS. The CLF signal together with the IOS signal cause the Overflow flip-flop to be cleared at time T4TS.

4-454. The SKF signal sets the Carry flip-flop at time T4TS. During times T6 and T7 the output of the Carry flip-flop, C0, is used to increment the P- and M-registers by two instead of one. This causes the computer to skip the next program instruction. The Carry flip-flop is cleared at time T0 of the following machine cycle.

4-455. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to increment by one if an SKF signal has not been generated. The next phase (phase 1) is then set, and the computer is ready to process the next instruction.

4-456. Test Procedure. To test the SOS and SOC instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 102301. This will test the SOS instruction. To test the SOC instruction, use 102201. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction). Press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

f. At the computer front panel, press and release the RUN switch.

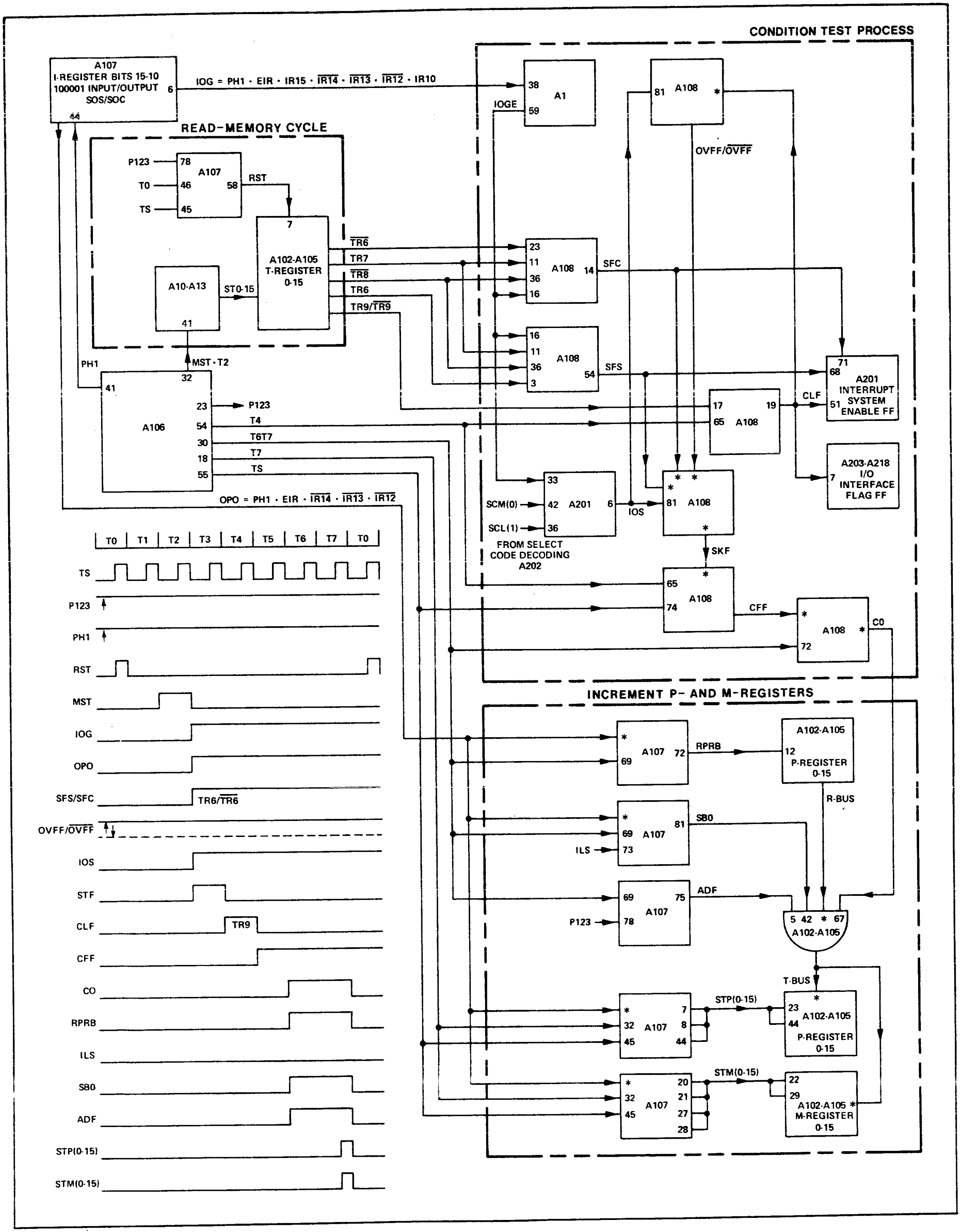
4-457. The computer is now in the run mode executing the SOS (SOC) instruction. Using a dual-trace oscilloscope check the state of the signals shown in figure 4-79. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-57. SOS/SOC Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)				WRITE (TR to Mem)			
FETCH SOS	1	Clear TR	Clear IR	TR to IR OVF	SFS to OVF	SKF to Carry FF		P + 1 + Carry to P, M Set next phase	
FETCH SOC		Clear TR	Clear IR	TR to IR	SFC to OVF	SKF to Carry FF		P +1 +Carry to P, M Set next phase	



2019-80

Figure 4-79. SOS/SOC Instruction Processing Circuits, Servicing Diagram

4-458. MEMORY SECTION TROUBLESHOOTING.

4-459. GENERAL.

4-460. The core memory in the 2116B Computer is of conventional design, except that the use of a reverse-current technique in the X drive-lines permits use of an 8K (8, 192-word) core stack assembly, rather than the more usual 4K stack. The computer can contain either one or two 8K stacks. An additional one or two 8K stacks may be used in an I/O and memory extender unit external to the computer.

4-461. Figure 3-1 is an overall block diagram of the computer, including the memory section. When a word is to be read from memory, the address is placed in the M-register. The address is decoded by the address decoding gates, which select the appropriate driver and switch. Current then flows from the driver to the switch, or vice versa, and the cores of the selected word are set to the zero state. For each core that contained logic 1, a sense amplifier detects an output from the core. The sense amplifier sets the corresponding position of the T-register to logic 1. Since the T-register is cleared before the word is read out, the register contents become the same as the word read from memory. The word read out must then be restored in the memory location from which it was acquired. To do this, the memory section attempts to store logic 1 in every bit position of the word. However, the inhibit driver for each bit of the word senses the corresponding bit in the T-register, and if the bit is logic 0 the inhibit driver prevents the writing of logic 1 in the appropriate bit position of the selected word location in memory. By this means the word read from memory is restored in the original location.

4-462. The read operation described above is also performed for a memory write operation, except that the word read out is not stored in the T-register. Instead, a new word is placed in the T-register, and the new word is stored rather than the original word. Refer to paragraph 3-77 for a more detailed account of memory operation.

4-463. When troubleshooting the memory section, it is necessary to determine which of the following types of faults exist:

a. Addressing fault.

b. Read fault.

c. Write fault.

4-464. The type of fault can be determined from the symptoms observed, from running the diagnostic programs, and by using panel controls to store and read test words. As a further means of determining the type of fault, small test programs can be manually inserted to read or write in the memory section. During these test operations oscilloscope examination of waveforms will serve as an aid in determining the type of fault. It should be noted that when an addressing fault exists it affects both read and write operations. Therefore, if a word is written in a given location and then read back, operation may appear normal because the word will have been written in and read from the wrong location.

4-465. Loading the entire core memory with known contents can serve as an aid to troubleshooting. A simple method of doing this is described below. The procedure stores any desired 16-bit word in all memory locations except the protected area containing the binary loader program. After loading, the computer continues to reload each memory location, thereby providing continued use of all addressing, write, and read circuits to permit oscilloscope examination of waveforms. The procedure for bringing this about is as follows:

Note

> Do not omit step "a" below, otherwise data in the protected area will be destroyed.

a. Make sure the LOADER switch is in the PROTECTED position.

b. Press and release the PRESET switch.

c. Set all SWITCH REGISTER switches to logic 0 (down) position.

d. Press and release the LOAD ADDRESS switch.

e. Set the SWITCH REGISTER switches to 070000 (octal).

f. Press and release the LOAD A switch.

g. Press and release the SINGLE CYCLE switch.

h. Set the PHASE switch to LOOP position.

i. Set into the SWITCH REGISTER switches the 16-bit test word which is to be stored.

j. Press and release the LOAD A switch.

k. Press and release the RUN switch.

4-466. When using the above procedure, less than one second is required for storing the test word in all memory locations except the protected area. The word is stored in each location in turn, proceeding in memory-address sequence. After the test word has been stored in all memory locations, the test word will continue to be rewritten in the same sequence of addresses until the HALT switch is pressed. The word cannot be changed while the computer is running because the SWITCH REGISTER switches are disabled. To use a different test word, press and release the HALT switch, set the desired test word in the SWITCH REGISTER switches, press and release the LOAD A switch, and press and release the RUN switch.

4-467. FIGURE AND TABLE REFERENCES FOR TROUBLESHOOTING.

4-468. When performing troubleshooting in the memory section, the following figures and tables will be found useful: figures 3-1, 3-7, and 3-11, and tables 3-1, 3-2, 3-3, and 3-4.

4-469. Additional illustrations which will serve as an aid in troubleshooting are the troubleshooting block diagram in figure 4-80, the illustration in figure 4-81 showing selection of a typical core memory location, and the waveforms in figures 4-82 through 4-88. The waveforms show signals at the indicated points when writing or reading logic 1's throughout core memory (except the protected area) with the procedure described in paragraph 4-465. Included in each waveform illustration is timing pulse T0, which serves to indicate the timing relationship of the pulses shown. It will be noted that in some of the waveforms the trace baseline continues beneath or above the pulse. This results from the lack of a pulse when the M-register designates an address in the protected area. The Y-axis driver/switch output in figure 4-82 is a result of readout, while the waveform in figure 4-83 is a result of writing. In figures 4-84 and 4-85 two pulses appear in the upper part of each illustration. This results from the current-reversal that takes place for the X drive-lines when reading and writing in the upper module of the core stack assembly. One pulse in each pair (the one corresponding to the Y-axis operation) is used when reading or writing in the lower module. The second pulse of each pair is for the upper module. In figure 4-86, the second pulse is produced when writing takes place. This pulse is stopped by the gate to which it is applied; only the first pulse, occurring during readout, passes the gate. This is illustrated in figure 4-87, which shows the gate output. In the final waveform illustration, figure 4-88, two baseline traces appear above the pulse. One baseline occurs when the M-register designates addresses in the protected area, and the other occurs when the M-register indicates location 000000 and 000001, the A- and B-register respectively.

4-470. ADDRESSING CIRCUITS.

4-471. DESCRIPTION. The selection of a particular word-location in the core stack assembly is a function of the following cards;

a. Timing generator card A106.

b. Arithmetic logic cards A102, A103, A104, and A105.

c. Direct memory logic card A20.

d. Memory module decoder card A2.

e. Driver/switch cards A8, A9, A14, and A15. (Cards A8 and A9 are not installed when only a single 8K core stack assembly is used.)

4-472. Timing Generator Card. The timing generator card produces timing and control signals for the memory section. Refer to paragraph 4-156 for complete memory timing information.

4-473. Arithmetic Logic Cards. The arithmetic logic cards contain the M-register, which specifies the address in memory in which reading or writing will take place.

4-474. Direct Memory Logic Card. The direct memory logic card contains circuits which are intermediary combining circuits for memory addressing and logic control. When used without the DMA optional feature, the circuits on the direct memory logic card merely act as buffering circuits for the memory addressing and logic control signals. When used with the DMA optional feature, the direct memory logic card circuits allow the DMA optional feature to control the memory addressing and logic control signals.

4-475. Memory Module Decoder Card. The memory module decoder card determines, from the specified memory address, the core stack in which the addressed location is situated, and whether the addressed location is in the lower or upper module of the stack. The core stack specified by the memory module decoder card may be in the I/O and memory extender, if this optional feature is used. When the LOADER switch is in the PROTECTED position, the memory module decoder card also provides a signal which prevents core memory reading or writing when an address is specified which is one of the highest 77 (octal) addresses of the total core memory capacity installed. Refer to paragraph 3-146 for complete memory module decoder circuit information.

4-476. Driver/Switch Cards. The driver/switch cards decode the address specified by the M-register for reading or writing in core memory, and furnish the required X and Y drive-line currents for the addressed memory location. Refer to paragraph 3-150 for complete driver switch circuit information.

4-477. TEST PROCEDURE. The procedure to be used for troubleshooting the addressing circuits depends on whether the failing addresses are known, and from other symptoms observed. As a general-purpose procedure, the following technique may be used:

a. Load all locations in memory, except the protected area, with logic 1's, using the method described in paragraph 4-465.

b. With an oscilloscope, examine the output of each address decoding gate on the driver/switch cards. If failing groups of addresses are known, only the gates for these addresses need be examined. (Refer to tables 3-3 and 3-4 for the gates corresponding to each address. Figure 3-7 shows the arrangement of digits in the address.)

c. If the decoding gates furnish an output pulse, the fault lies in the driver or switch circuit corresponding to the failing addresses. If a decoding gate does not furnish an output, the fault is between the gate and the M-register. In either case make oscilloscope, voltmeter, and ohmmeter checks to locate the defective component or faulty connection.

4-478. READ AND WRITE CIRCUITS.

4-479. DESCRIPTION. The read and write circuits control data bits as they are stored in, and removed from, the core memory. These functions are performed by the following circuit cards:

a. Timing generator card A106.

b. Sense amplifier cards A10, A11, A12, and A13. (Cards A10 and A11 are not installed if only a single 8K core stack assembly is used.)

c. Arithmetic logic cards A102, A103, A104, and A105.

d. Inhibit driver cards A4, A6, A16, and A18. (Cards A4 and A6 are not installed when only a single 8K core stack assembly is used).

4-480. Timing Generator Card. The timing generator card produces timing and control signals for the memory section. Refer to paragraph 4-156 for complete memory timing information.

4-481. Sense Amplifier Cards. The sense amplifier cards each contain 17 amplifier circuits which sense the pulses from the 17 ferrite cores of the addressed location in memory. A pulse is produced when a core storing a logic 1 is switched to the logic 0 state during memory read time. One of the 17 sense amplifiers on each card is used only when the memory-parity optional feature is installed in the computer. One sense amplifier card is used for each module (upper or lower) of each core stack assembly.

4-482. Arithmetic Logic Cards. The arithmetic logic cards contain the T-register, which receives the word read from core memory via the sense amplifier circuits. The T-register also provides the word to be written in memory via the inhibit driver circuits.

4-483. Inhibit Driver Cards. The inhibit driver cards each contain 17 inhibit drivers which sense the bit-positions of the T-register. For each bit-position containing logic 0, an inhibit driver is turned on and prevents the writing of logic 1 in the corresponding bit position of the addressed memory location during memory write time and memory inhibit time. One of the 17 inhibit drivers on each card is used only when the memory-parity optional feature is installed in the computer. One inhibit driver card is used for each module (upper or lower) of each core stack assembly. Refer to paragraph 3-169 for complete inhibit driver circuit information.

4-484. TEST PROCEDURE. The procedure to be used for troubleshooting the read and write circuits depends on the symptoms observed. As a general-purpose procedure, the following technique may be used:

a. Load all locations in core memory, except the protected area, with logic 1's, using the method described in paragraph 4-465. Alternatively, if symptoms indicate that logic 0's are not being read or written properly, load core memory with logic 0's.

b. With an oscilloscope, examine the output of the inhibit driver corresponding to the bit that fails. If all bits of the word fail, examine the signals that control the inhibit function. If this function is satisfactory, examine the output of the sense amplifier corresponding to the bit that fails. If all bits fail, examine the signals that control writing.

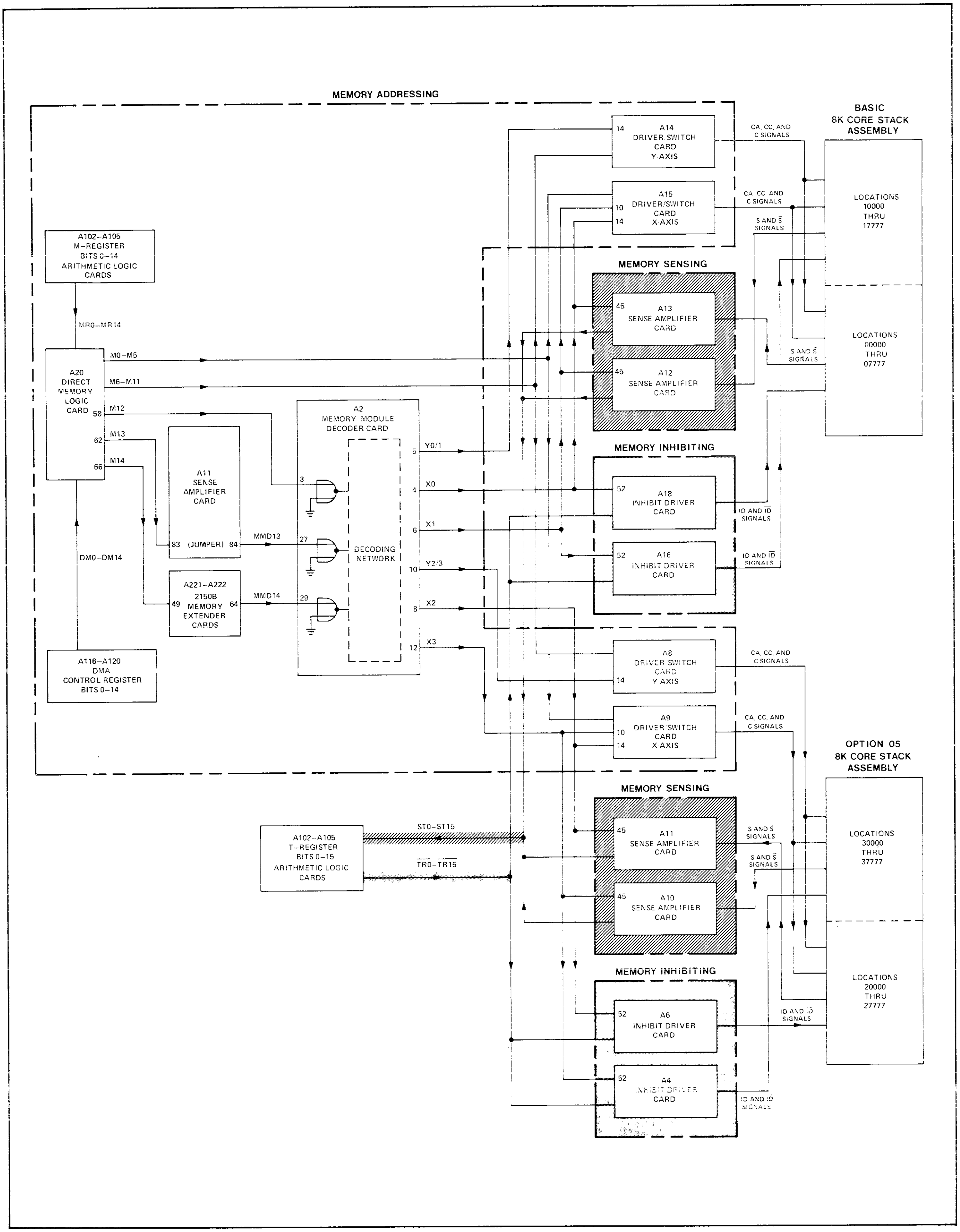


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Figure 4-80. Memory Section, Servicing Diagram

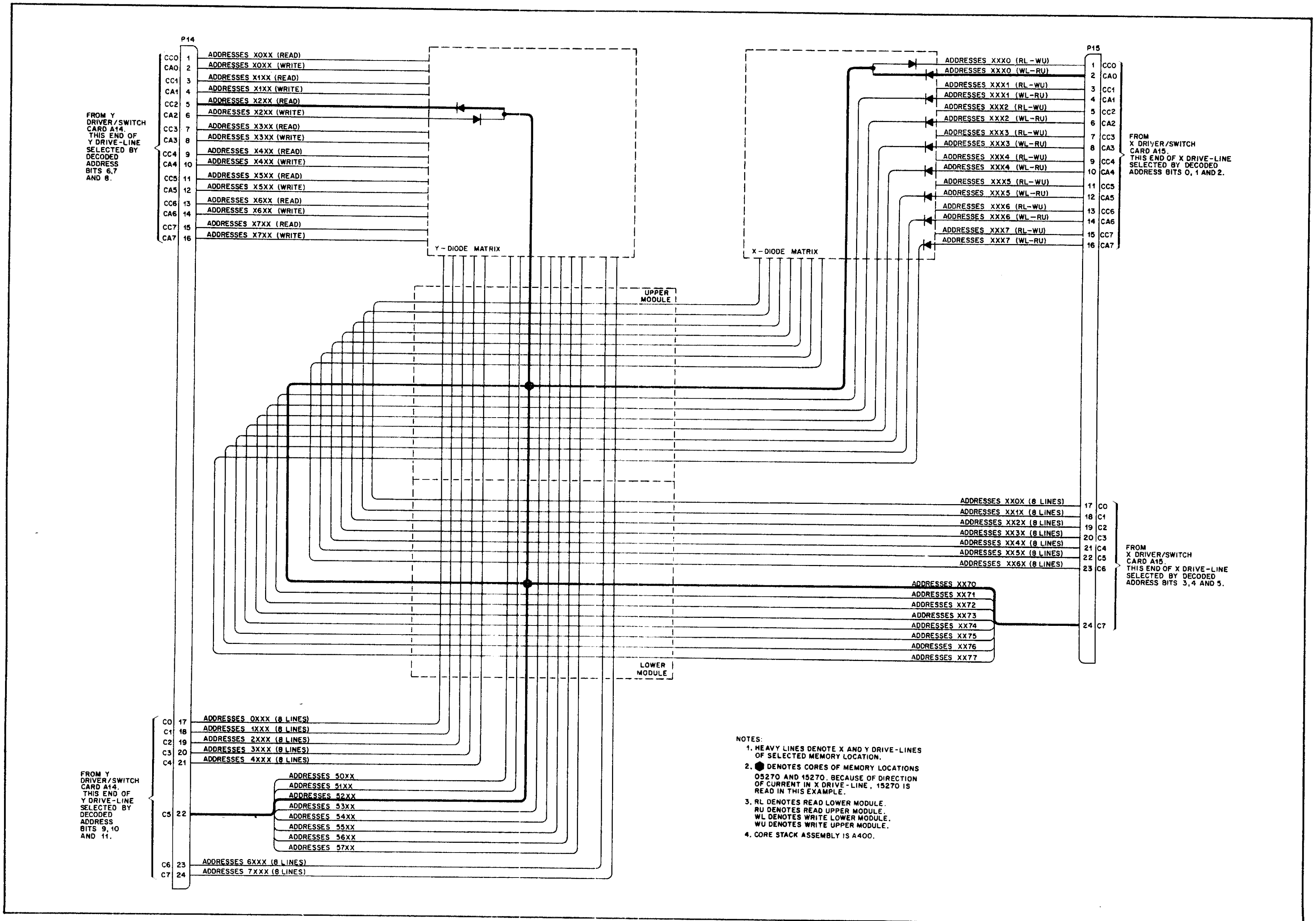

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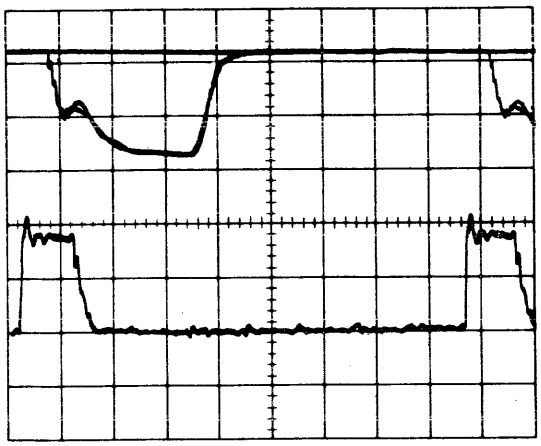
Figure 4-81. Typical Address Selection Circuits, Readout Address 15270 (Octal)



2019-102

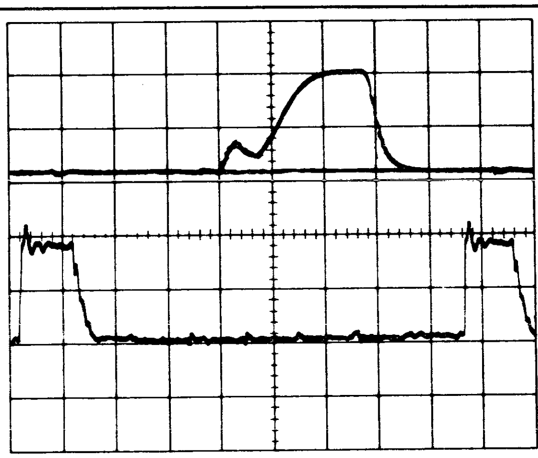
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (Y driver/switch output, readout):
Input A8TP2/A14TP2
Volts/cm . . . . .1 (if using 10:1 probe)

Channel B (TO):
Input A106TP1
Volts/cm . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-82. Y Driver/Switch Output Waveform, Readout Lower or Upper Module



2019-101

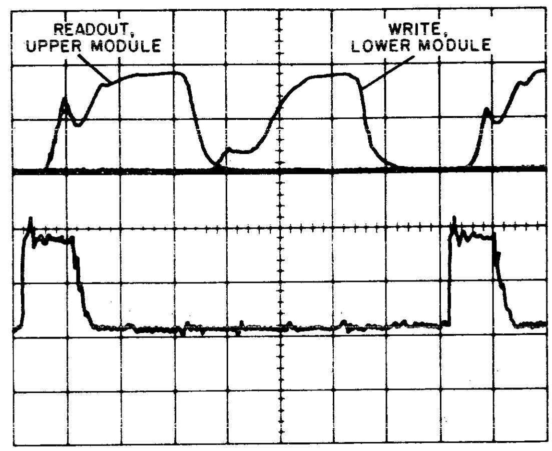
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (Y driver/switch output, write):
Input A8TP1/A14TP1
Volts/cm . . . . .1 (if using 10:1 probe)

Channel B (TO):
Input A106TP1
Volts/cm . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-83. Y Driver/Switch Output Waveform, Write Lower or Upper Module



2019-99

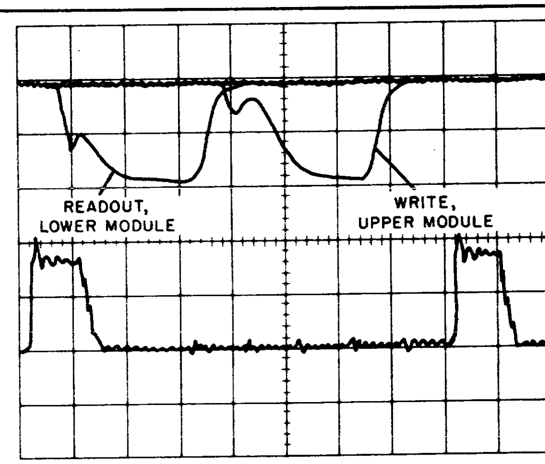
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (X driver/switch output):
Input A9TP1/A15TP1
Volts/cm . . . . .1 (if using 10:1 probe)

Channel B (TO):
Input A106TP1
Volts/cm . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-84. X Driver/Switch Output Waveform, Readout Upper Module, Write Lower Module



2019-100

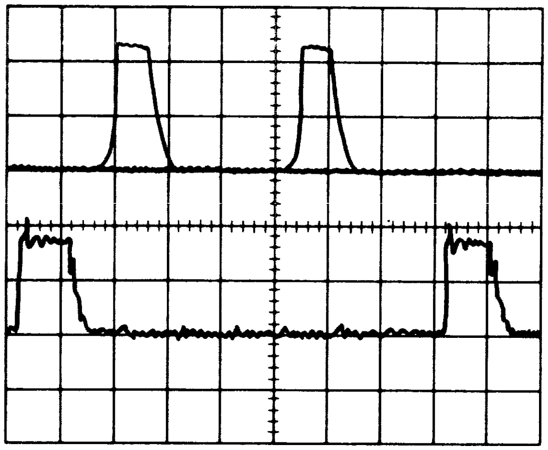
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (X driver/switch output):
Input A9TP2/A15TP2
Volts/cm . . . . .1 (if using 10:1 probe)

Channel B (TO):
Input A106TP1
Volts/cm . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-85. X Driver/Switch Output Waveform, Readout Lower Module, Write Upper Module



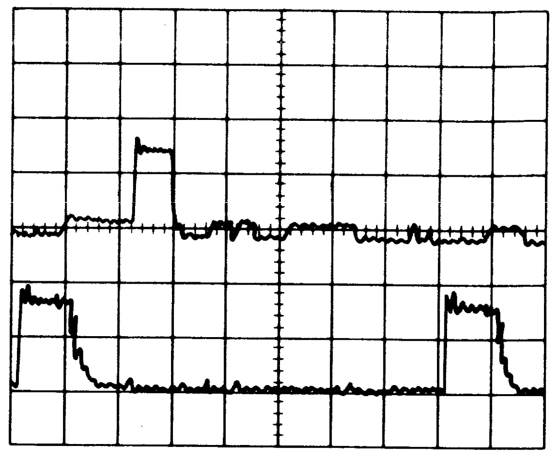
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (sense amplifier output):
Input A12MC17-14
Volts/cm . . . . . . .0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-86. Typical Sense Amplifier Output Waveform



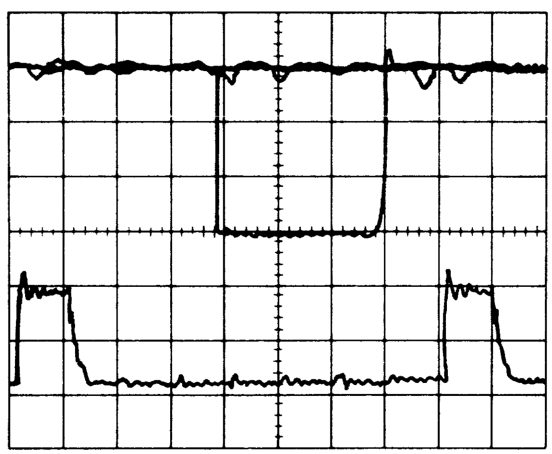
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (Gated sense amplifier output):
Input A12MC17-13
Volts/cm . . . . . . .0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . 0.2 us

Figure 4-87. Typical Sense Amplifier Gated Output Waveform



OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (inhibit driver output):
Input . . . . .A16CR1 anode
Volts/cm . . . . .1 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . . .0.2 (if using 10:1 probe)

Time /cm . . . . 0.2 us

Figure 4-88. Typical Inhibit Driver Output Waveform

4-485. POWER SUPPLY SECTION TROUBLESHOOTING.

4-486. GENERAL.

4-487. The troubleshooting instructions which follow are based on the assumption that the basic checkout procedure has been performed up to a certain point, at which an abnormal condition has been encountered.

4-488. As with other troubleshooting procedures described in this section, only the most usual faults and the most probable causes are dealt with. From the information given, the great majority of faults can be corrected without undue loss of time if the serviceman understands the circuit theory of the power supply section. Refer to paragraph 3-178 for a detailed account of power supply operation.

4-489. The 2116B power supply section produces seven regulated voltages for the circuit cards in the card cage. These voltages, +4.5, -2, +32, +22, +12, -12, and -22 volts, are referred to as controlled voltages because they are turned on and off in a controlled manner. The first two of these voltages, +4.5 and -2 volts, furnish the operating potentials required by most of the logic circuits in the computer. The remaining five voltages are used principally by the computer memory section.

4-490. Two additional voltages are furnished by the power supply section. These are unregulated voltages, and their potentials are +7 volts and +35.5 volts. The +7 volt power is used for lighting all indicator lamps with the exception of the POWER indicator lamp, which operates from regulated +12 volts. The +35.5 volt power is used by optional circuit cards which install in the input/output section (figure 5-5) of the card cage.

4-491. Distribution of dc voltages in the computer is shown in figure 5-49, the overall interconnection diagram, and in table 5-8, the backplane wiring list. To find any given voltage in the backplane wiring list, refer to table 5-7, the signal index.

4-492. In addition to the dc voltages furnished for use outside the power supply section, additional subsidiary voltages are produced for use within the power supply section itself. If failure or overloading occurs for one of the seven regulated voltages, some or all of the remaining six voltages may be shut down. Figure 3-23 illustrates the requirements of each power supply with respect to the outputs from other supplies. When a power supply is shut down the series regulator transistors for the supply cut off the flow of current from the power supply to its load. The voltage source itself remains turned on.

4-493. When failure of some or all regulated voltages takes place, a power-fail interrupt is not generated.

4-494. When optional circuit cards in the computer card cage increase the load on the +4.5 and/or -2 volt power supplies beyond the capabilities of the power supplies, a power supply extender is used. This unit furnishes +4.5 and -2 volt power which connects in parallel with the same voltages produced in the computer. Power failure in the extender will cause a power-fail interrupt in the computer. Power failure in the extender will also cause shut-down of voltages in the computer because the -2 or +4.5 volt power supply in the computer is overloaded when failure occurs in the extender.

4-495. PRECAUTIONS.

WARNING

Before removing the transformer cover (figure 1-4) during troubleshooting, press the POWER switch off, unplug the ac power cable, and wait 3 minutes for filter capacitors to discharge. If this procedure is not followed, ac line-voltage and dc voltages with heavy current capability exist at exposed terminals beneath the transformer cover. If the metal cover touches one of these terminals when being removed, the result may be death, injury, an unpleasant electric shock, or damage to equipment.

CAUTION

Before removing or installing a circuit card in the power supply section, press the POWER switch off and wait 3 minutes for filter capacitors to discharge. Failure to observe this precaution may result in damage to components.

CAUTION

Do not apply power to the computer when an overvoltage protection circuit is disconnected. An overvoltage condition can destroy components on cards in the card cage. To check operation of the power supply without the overvoltage protection circuits, first remove all cards from the card cage, with the exception of power fail interrupt card A1, memory module decoder card A2, and front panel coupler card A101. These cards must be in place before the power supply can be turned on. However, bear in mind that an overvoltage condition can destroy components on these cards. The power supply will operate without card A2 if the thermal switch circuit for this card is shorted (see figure 3-18).

4-496. SHORT-CIRCUIT ISOLATION. To isolate a dc-voltage short in the computer, it is necessary to slide all cards out two to three inches from the card-cage excepting the cards in slots A1, A2 and A101. The 48-pin connectors, where used, should also be removed from the ends of the cards. The cards in slots A1, A2, and A101 must remain in place in the card cage, otherwise it will not be possible to turn on the power supply. The 48-pin connector on card A101 must also be in place in order to allow power turn-on.

4-497. All controlled voltages except +4.5 volts function normally when entirely unloaded. The +4.5 volt supply requires a minimum load, otherwise dc shut-down takes place. This load is provided internal to the power supply by resistor A310R23 in the power supply section.

4-498. To prevent the memory voltages (+12, -12, +22, -22, and +32 volts) from being applied to the computer load circuits, remove memory supply regulator card A302 from the power supply section. Then, when power is re-applied only +4.5 and -2 volts are furnished to the computer.

4-499. To prevent any controlled voltage from being applied to the computer load circuits, remove logic supply regulator card A301 from the power supply section. Then press the POWER switch on.

4-500. POWER SUPPLY EXTENDER. If a power supply extender is used, it must be eliminated as a source of trouble before troubleshooting is performed on a fault which may be in the +4.5 or -2 volt power supply. To do this, turn off the computer and reduce power supply loading by a sliding all optional cards (shown in figure 5-5) from the card cage about two inches. Next, detach the extender from the computer. Then press the POWER switch on. If the fault symptom disappears check each optional card for a possible short condition by pressing the POWER switch off, inserting one card into its original slot, and pressing the POWER switch on. Repeat this procedure for each optional card, removing each card after it has been checked. If the fault symptom does not reoccur, refer to the manual for the power supply extender for troubleshooting procedures.

4-501. TURN-ON AND SHUT-DOWN WAVEFORMS. Figures 4-89 through 4-92 are waveforms of the seven controlled voltages during turn-on and shut-down initiated by the POWER switch. These waveforms were observed using an HP 181A Storage Oscilloscope and are given here as an aid to understanding the power supply operation.

4-502. TROUBLESHOOTING PROCEDURE FOR SHORT IN AC DISTRIBUTION CIRCUITS.

4-503. If fuse A312F1 is open and a replacement fuse blows, read the warning and cautions in paragraph 4-495. Press the POWER switch off, unplug the ac power cable, open the card cage, and search by sight and smell for scorched electrical insulation in the power supply. Remove the transformer cover (figure 1-4) and examine the power transformer and its connecting wires for burn discoloration. Replace any damaged components and wires. Then make ohmmeter checks to ascertain the cause of damage, and correct the fault. If no evidence of burn damage is found, proceed as follows:

a. Make sure the ac power cable is unplugged.

b. Remove the fuses for the secondary windings of transformer A311T1 (figure 5-44). To do this, remove all fuses beneath the transformer cover (figure 4-93), and remove the four fuses from component board assembly A309 (figure 4-93). Removal of the secondary-winding fuses will permit a check to ensure that the overload is not in the dc circuits. It is also possible that the wrong type of fuse has been installed for one of the dc voltages, causing the primary fuse to blow instead of a secondary fuse.

c. After removing secondary-winding fuses, install a new fuse in the holder for A312F1.

d. Plug in the computer and press the POWER switch on. If fuse A312F1 blows again, proceed to step "e" below. If the fuse does not blow, the trouble is in the dc power supplies or is a result of excessive dc loading. If a power supply extender is used, first eliminate it as a source of the trouble as described in paragraph 4-500. If the trouble is in the computer itself, isolate the defective or overloaded dc power supply. Do this by replacing secondary-winding fuses until fuse A312F1 blows when the computer is turned on. Turn off the computer before installing each secondary-winding fuse, and install fuses in the sequence listed below. When the defective or shorted power supply is found, remove circuit cards from the card cage to eliminate a possible short circuit, as described in paragraph 4-496. If the shorted condition disappears when cards are removed, determine the defective card by sliding cards into their sockets one by one. Press the POWER switch off before installing each card. If removal of cards does not eliminate the trouble, the short is in the power supply section, card-cage backplane, or the overvoltage protection assembly A121. Perform troubleshooting in the affected power supply, backplane voltage bus, in overvoltage protection assembly A121. Start at the applicable secondary winding, and check voltages until an abnormal condition is found. For wiring information, refer to the schematic diagrams in figures 5-31 and 5-44, and the parts location and connection diagrams in figures 5-29, 5-32 through 5-43, and 5-45. Note that the voltages listed in the tables in figure 5-44 are for the normal operating condition, in which current limiting does not take place and a normal load is imposed on the power supply. If the fault causes excessive power supply loading (possibly because of functioning of the overvoltage protection circuit), current limiting occurs and voltages may differ from those listed but still may be correct. When determining the dc power supply at fault, replace fuses in the following sequence:

(1) Fuses for -2 volts (F12 and F13).

(2) Fuses for +4.5 volts (F11 and F14).

(3) Fuses for -12 volts (F5 and F6).

(4) Fuses for +22 and -22 volts (F4 and F7).

(5) Fuse for +32 volts (F9). If fuse F5 or F6 blows after F9 is installed, the +12 volt power supply is defective or overloaded. (The +12 volt supply is not turned on until +32 volts is available.)

e. If fuse A312F1 blows when all secondary-winding fuses have been removed, a short or excessively low resistance exists in the ac wiring in the computer. This wiring is shown in figures 3-17, 5-42, 5-43, 5-48, and 5-49. Because of the low resistance of the power transformer primary windings, troubleshooting with an ohmmeter is not practical. Therefore, the fault must be isolated by disconnecting various parts of the ac circuit in turn. (Insulate loose wires with electrical tape to avoid a short.) After disconnecting each circuit, apply power to determine whether fuse A312F1 still blows. Because the secondary-winding fuses are removed during this procedure, no appreciable heating takes place in the computer circuits and disconnecting the fans is not harmful.

4-504. TROUBLESHOOTING PROCEDURE FOR OPEN IN AC DISTRIBUTION CIRCUITS.

4-505. If symptoms indicate an open in the computer ac distribution circuits, first make sure that power is available at the ac outlet into which the computer is plugged. Also make sure fuse A312F1 is intact. Then read the warning and cautions in paragraph 4-495, press the POWER switch off, unplug the ac power cable, open the card cage, and search by sight and smell for scorched electrical insulation. Remove the transformer cover (figure 1-4) and examine the power transformer and its connecting wires for burn discoloration. Replace any damaged components or wires. Then make ohmmeter checks to ascertain the cause of damage, and correct the fault. Refer to figures 3-17, 5-42, 5-43, 5-48, and 5-49 for wiring information. If no evidence of burn damage is found, use an ohmmeter to make continuity checks of the ac power cable and the ac circuits in the computer. Press the POWER switch to close its contacts in order to facilitate testing.

4-506. TROUBLESHOOTING PROCEDURE FOR +7 VOLT POWER SUPPLY.

4-507. If only the POWER indicator lights, read the warning and cautions in paragraph 4-495. Then examine fuse A310F10. If the fuse is intact, make voltmeter and ohmmeter checks for an open in the +7 volt circuit. If the fuse is open, make ohmmeter checks for a short. To facilitate the ohmmeter checks, remove fuse A310F10 until the short is found. When making the voltmeter and ohmmeter checks for a short or open, refer to figures 5-34, 5-42, 5-44, 5-46, 5-47, 5-48, and 5-49 for wiring information.

4-508. TROUBLESHOOTING PROCEDURE FOR INOPERATIVE POWER LAMP.

4-509. The POWER lamp operates from regulated +12 volts. If the lamp fails to light and the lamp itself is not defective, dc shut-down has probably occurred. Read the warning and cautions in paragraph 4-495, refer to figures 3-18, 3-23, and 5-31 through 5-49 for information, and proceed as follows:

a. Check the -2, +4.5 and -12 volt supplies at the appropriate test jacks on overvoltage protection assembly A121. If -2 and +4.5 volts are present and -12 volts is not, memory voltage shut-down has taken place. (The memory voltages are +32, +22, +12, -12, and -22 volts.) Check all voltages at the test jacks on A121 to verify the condition indicated. If only the memory voltages have been shut down, the fault is in one of the memory-voltage power supplies; proceed to step "e". If all voltages have been shut down, a thermal switch is open, the fault is on power fail interrupt card A1, or the -2 volt power supply is defective or overloaded; proceed to step "b". If only -2 volts is available, the +4.5 volt power supply is faulty or overloaded; proceed to step "e".

b. If all voltages have been shut down, make sure the thermal switches are closed. Do this by measuring the voltage between terminal A100TB1-5 and terminal XA2-81 (figure 3-18) with computer power on. (The attachment of the negative test lead to A100TB1-5, rather than to ground, is necessary because the series regulator transistors for -2 volts are cut off.) If the potential is approximately 10 volts dc, all thermal switches are closed; proceed to step "d".

c. If a thermal switch is open, make voltage checks along the thermal switch line to locate the open switch. When it is found, press the POWER switch off, unplug the ac power cable, allow 3 minutes for filter capacitors to discharge, and make ohmmeter checks of the circuits in the overheated unit to locate the fault. Bear in mind that excessively high ambient temperature (over 55 degrees C, 131 degrees F) can cause a thermal switch to open. If this is the case, the environment is not suitable for the computer.

d. If thermal switches are closed, check the PSO signal at terminal A100TB1-1 (figure 3-18). In order to produce PSO, the +4.5 volt supply must be on. To turn on this supply, remove power from the computer, then ground the negative (bottom) side of capacitor A301C54, and re-apply power. If the PSO signal is then found to be false, the circuits on power fail interrupt card A1 which produce the signal are faulty, or the +4.5 volt power supply is defective or overloaded. Check at the appropriate test jack on overvoltage protection assembly A121 for the presence of +4.5 volts. If this voltage is available, the circuits which produce the PSO signal are faulty. Locate the defective component or faulty connection by voltmeter and ohmmeter checks. If +4.5 volts is not available, proceed to step "e". First, remove the ground from capacitor A301C54.

e. Examine all fuses beneath the transformer cover and on component board assembly A309 (figure 4-93). If fuses are intact, proceed to step "f". If a fuse is open, replace it. If operation is then normal, the fuse had probably deteriorated and become defective. If the fuse blows again when power is applied, and the fuse is F2, F3, or F8 (which furnish subsidiary voltages used only within the power supply section), make voltmeter and ohmmeter checks in the power supply section to locate the fault. If the fuse is not F2, F3, or F8, the fuse is furnishing current for a logic-circuit voltage or memory voltage. Press the POWER switch off, wait 3 mintues, remove all cards from the card-cage except A1, A2 and A101, then remove logic cutoff of the series regulator transistors on the large and small heat sinks, bringing about isolation of the filter capacitors for the logic-circuit and memory voltages. If a replacement fuse blows after application of power, a filter capacitor or series regulator transistor is probably shorted. If the fuse does not blow, re-install card A301 and perform troubleshooting in the faulty power supply with a voltmeter and ohmmeter. Because a fuse blows, it may be assumed that the trouble is in the power supply section. (An excessive load imposed on the failing power supply from outside the power supply section would result in current-limiting shutdown, rather than a blown fuse.)

f. If fuses are intact, and only memory voltages are absent, proceed to step "h". If fuses are intact and +4.5 and/or -2 volts has been shut down, first make sure the trouble is not in the power supply extender (if any) as described in paragraph 4-500. Then, if the fault is in the computer, proceed to step "g".

g. If fuses are intact and logic-circuit voltages as well as memory voltages have shut down, replace logic supply regulator card A301, apply voltage to the computer, and check the voltages at A121. If replacement of card A301 fails to restore normal operation, or if a spare card is not available, turn off power and ground the negative (bottom) side of capacitor C54 on logic supply regulator card A301 (figure 5-32). This will disable the shut-down circuits for +4.5 and -2 volts. Restore power and check at A121 to determine whether it is +4.5 or -2 volts which is at fault. Having found the failing voltage, locate the defective component by means of voltmeter and ohmmeter checks. Start at the applicable secondary winding, and check voltages until abnormal conditions are found. Note that the voltages listed in the tables in figure 5-44 are for the normal operating condition in which current limiting does not take place. If the fault causes excessive power supply loading (possibly because of functioning of the overvoltage protection circuit), current limiting occurs and voltages may differ from those listed but still may be correct. To eliminate card-cage cards as the source of a short, refer to paragraph 4-496. After finding the defective component or faulty connection, remove the ground from capacitor C54.

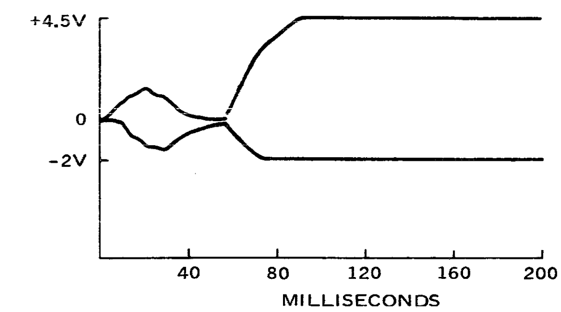
h. If shut-down has occurred for the memory voltages only, replace memory supply regulator card A302. If this fails to restore normal operation, replace logic supply regulator card A301. If the POWER indicator still does not light, or if spare cards are not available, turn off power and place a short across capacitor C56 on logic supply regulator card A301 (figure 5-32). This short will disable the shut-down circuits for the memory voltages. Restore power and check at A121 to determine which voltage is faulty. Having found the failing voltage, locate the fault by means of voltmeter and ohmmeter checks. Start at the applicable secondary winding, and check voltages until abnormal conditions are found. Note that the voltages listed in the tables in figure 5-44 are for the normal operating condition in which current limiting does not take place. If the fault causes excessive power supply loading (possibly because of functioning of the overvoltage protection circuit), current limiting occurs and voltages may differ from those listed but still may be correct. To eliminate card-cage cards as the source of a short, refer to paragraph 4-496. After finding the faulty component, remove the short from capacitor C56.

4-510. TROUBLESHOOTING PROCEDURE FOR FAILURE OF PON SIGNAL.

4-511. The PON signal is produced by power fail interrupt card A1 (figure 5-8). The pulse is true when +4.5 and -2 volts are both available to the computer load circuits. Upon failure of either of these two voltages, PON becomes false and the remaining controlled voltages are shut down. To troubleshoot the circuits which produce the signal, use an ohmmeter. However, first be sure the signal is not false because of failure or overload of the +4.5 or -2 volt power supply. To ascertain whether one of these voltages has failed, press the POWER switch off, ground the negative (bottom) side of capacitor C54 on logic supply regulator card A301, and re-apply power. If +4.5 and -2 volts are then available at the test jacks on overvoltage protection assembly A121, the circuits which produce the PON signal are faulty. Remove the ground from capacitor C56 after completing the check.

4-512. TROUBLESHOOTING PROCEDURE FOR FAILURE OF POFP PULSE.

4-513. If symptoms indicate failure of the POFP pulse, check the pulse by connecting an oscilloscope to pin 56 of power fail interrupt card A1. Each time the computer is turned on or off by the POWER switch, a positive pulse should be observed. If the POFP pulse is not present, troubleshoot the circuits on the A1 card which generate the pulse (figure 5-8). Start by making sure the PON signal is true when power is on.

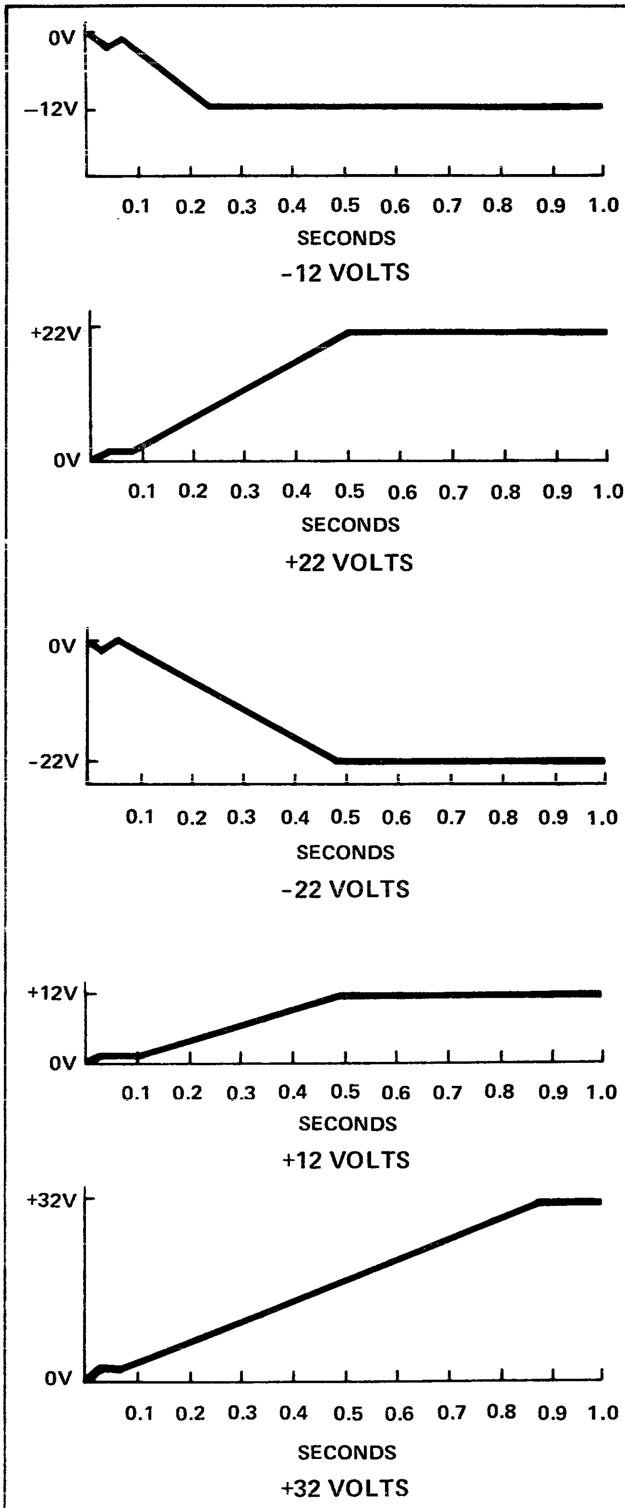


NOTES:

1. ALL FILTER CAPACITORS FULLY DISCHARGED BEFORE STARTING.
2. MAXIMUM LOAD IMPOSED ON BOTH VOLTAGES.

2019-17

Figure 4-89. Turn-On Waveforms, +4.5 and -2 Volts



NOTES:

1. ALL FILTER CAPACITORS FULLY DISCHARGED BEFORE STARTING.
2. MAXIMUM LOAD IMPOSED ON ALL VOLTAGES.
3. AMBIENT TEMPERATURE, 21°C (70°F).

2019-18

Figure 4-90. Turn-On Waveforms, -12, +22, -22, +12 and +32 Volts

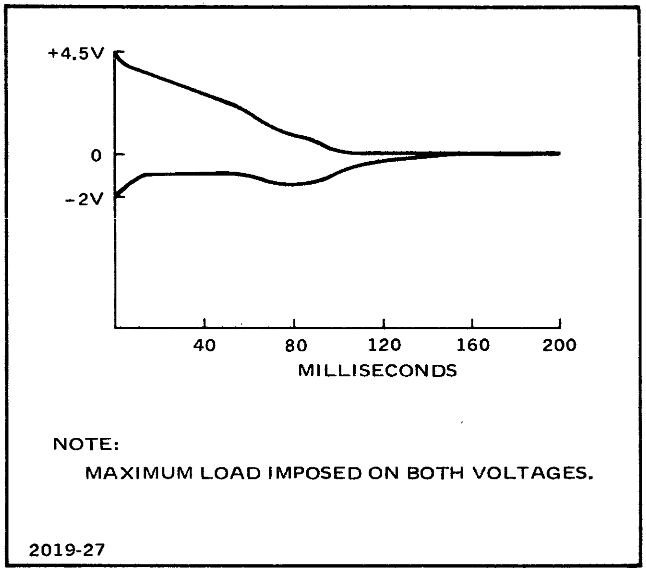


Figure 4-91. Shut-Down Waveforms, +4.5 and -2 Volts

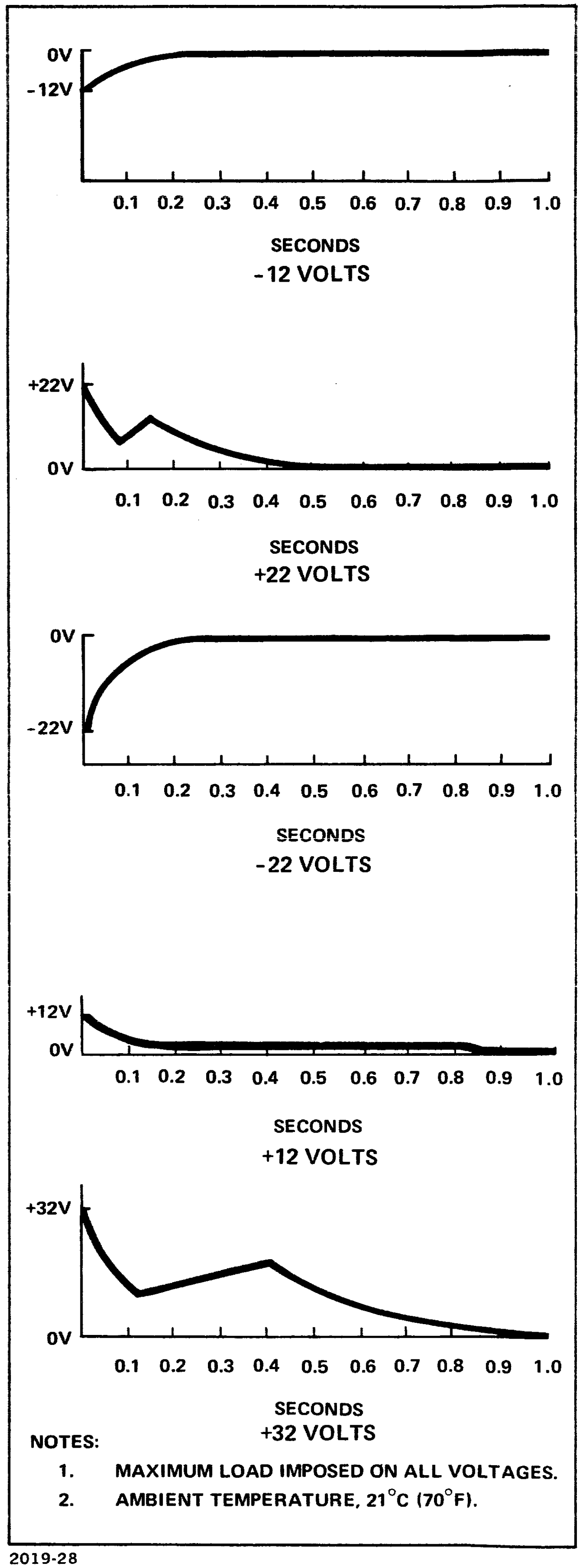
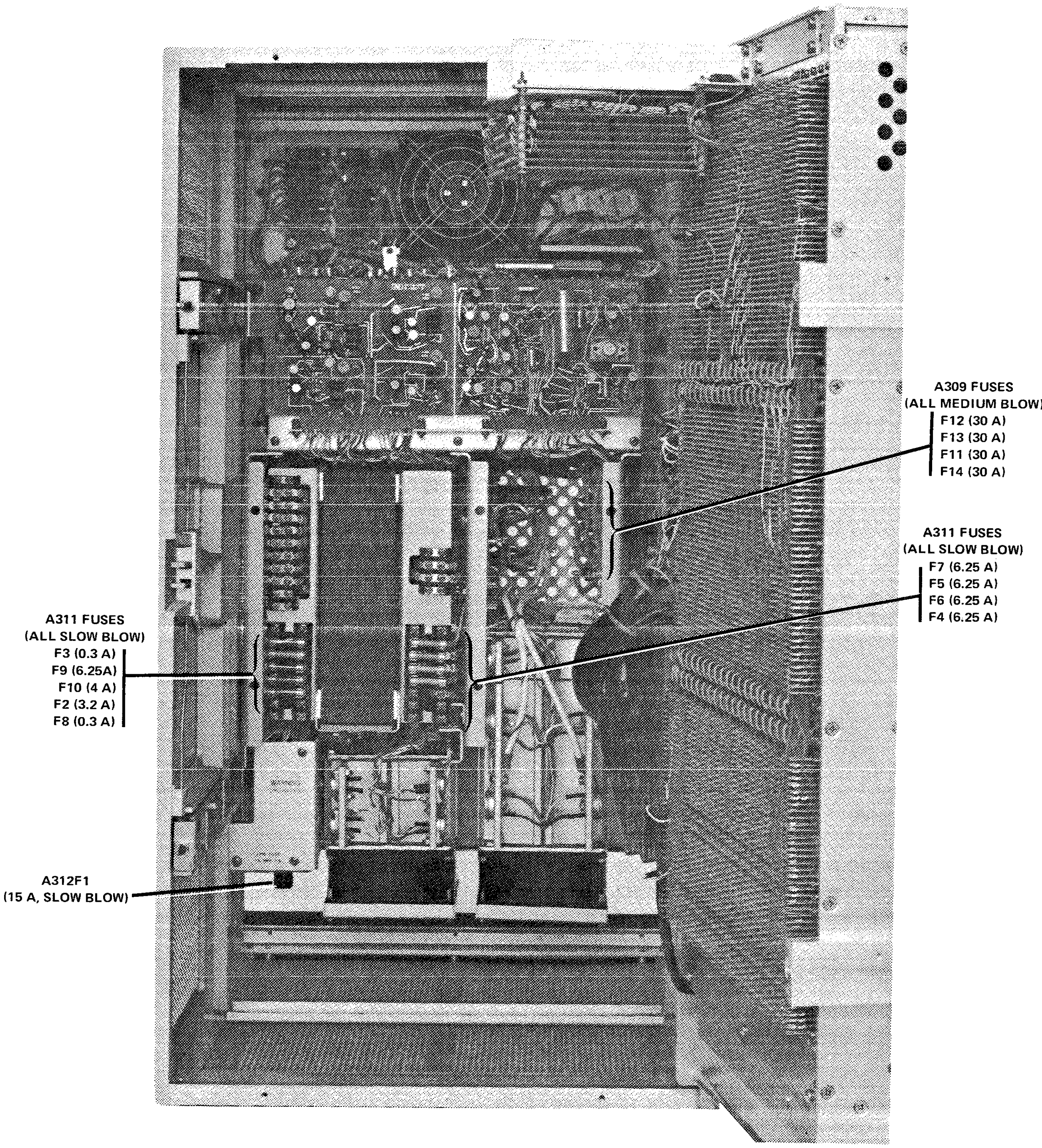


Figure 4-92. Shut-Down Waveforms, -12, +22, -22, +12, and +32 Volts



2019-6

Figure 4-93. Fuse Locations

SECTION V

MAINTENANCE

5-1. INTRODUCTION.

5-2. This section describes preventive and corrective maintenance for the 2116B Computer. Not included are maintenance procedures for I/O devices, I/O interface cards, the direct memory access feature, the extended arithmetic unit, and other optional features. Maintenance information for these items is provided in the documentation for the optional feature concerned.

5-3. Preventive maintenance is performed at scheduled intervals, and its purpose is to prevent or minimize equipment deterioration. Included in the preventive maintenance procedures are performance tests which check computer operation.

5-4. Corrective maintenance is performed when required, and its purpose is to restore normal operation to the computer after a fault has been isolated to a replaceable component. Fault isolation methods are presented in section IV.

5-5. Each maintenance procedure is described in full in this section. When feasible, the detailed description is followed by a summary which repeats the main features of the procedure. This summary may be used as a guide for the performance of maintenance after the reader has become familiar with the detailed description and has put it to practical use at least once.

5-6. To determine the locations of components and assemblies for the performance of maintenance, refer to the parts location diagrams presented later in this section. Also refer to the diagrams in section VI.

5-7. SAFETY PRECAUTIONS.

WARNING

When the computer is on, use caution when working inside the computer cabinet. Many exposed conductors carry low dc voltages which are capable of supplying heavy currents if short-circuited resulting in high heat and the possibility of painful burns. Use caution when manipulating metal tools or probes. A wrist watch, or a metal necklace, bracelet, or ring, must not be worn. Avoid dropping tools, screws, or other metal objects onto conductors. Remove power and recover dropped objects at once; if forgotten, damage could result later. AC power-line voltage is exposed when certain covers are removed; these covers are listed in the following paragraph. Exercise extreme caution when working in the computer with these covers removed, and never work under this condition unless another person is nearby and within sight. If feasible, unplug the ac power cable before performing any work inside the computer. Dangerous voltage exists even when the POWER switch is off. If working in the power supply section, wait 3 minutes for filter capacitors to discharge after removing power. Be sure to read paragraph 2-27 and 2-34 of this volume, and carry out the procedures described. Danger of death or serious injury exists if the precautions above are not observed. If due care is exercised, the computer is not dangerous. Respect high voltage, and it will respect you.

5-8. HIGH VOLTAGE POINTS.

5-9. The highest voltage in the computer is the ac line voltage. This voltage (see figure 3-17) is exposed when any of the following covers is removed:

a. The transformer cover (figure 1-4).

b. The cover or housing of ac input section A312 (figure 1-4).

c. The left side cover of the computer cabinet.

d. The bottom panel on the card cage (figure 1-5).

e. The shrink tubing covering the back of the POWER switch on control panel assembly A502.

5-10. TRANSFORMER COVER.

5-11. Before removing the transformer cover (figure 1-4), be sure the ac power cable is unplugged, and allow 3 minutes for filter capacitors to discharge. If these precautions are not observed, exposed terminals beneath the cover could be touched by the metal cover as it is removed; these terminals carry ac line voltage and low voltages with heavy current capabilities.

5-12. HEAT SINK ASSEMBLIES.

5-13. The collectors of transistors on the large and small heat sink assemblies (A304 and A305, figure 1-4) are electrically common with exposed portions of the heat sinks. These exposed areas therefore have dc potentials as high as 32 volts.

5-14. DISPLAY BOARD ASSEMBLY A501.

5-15. The center contacts for lamps on display board assembly A501 are metal strips which swing aside to permit lamp removal. When these strips are swung aside, the edges of the strips can cause cuts if care is not exercised. Use a cloth pad for moving the strips.

5-16. TEST EQUIPMENT GROUND.

5-17. If test equipment has a metal case, the negative test lead preferably should not be internally connected to the case. Instead, the case should be connected to a good earth ground through the test equipment power cord. This precaution prevents the danger of shock or possibility of short when the negative lead is connected to a point not at ground potential.

5-18. PREVENTIVE MAINTENANCE.

5-19. GENERAL.

5-20. The following preventive maintenance procedures are performed at monthly or semimonthly intervals, the frequency depending on the physical conditions prevailing at the particular site. Performance once per month is adequate for most sites, and is applicable to computers which operate 24 hours per day, 7 days per week.

5-21. EQUIPMENT REQUIRED.

5-22. The following items are required for the performance of preventive maintenance:

a. Diagnostic program tapes, as listed in Table 4-3.

b. Source of compressed air for cleaning air filters, or two cleaned filters.

c. Source of low pressure air, such as vacuum cleaner air outlet, for blowing dust from computer.

d. One digital voltmeter of the type listed in Table 1-5.

e. One general purpose Centigrade thermometer, accurate to at least ±1 degree for measuring ambient temperature.

5-23. PROCEDURE.

5-24. Before starting preventive maintenance, set up the thermometer for measuring ambient temperature. The thermometer must be near the computer, but away from cold drafts and heat radiating objects. Do not place the thermometer on or in the computer. Plug in the digital voltmeter and turn it on. Then proceed as follows.

a. Diagnostic Program and Lamp Test. Run diagnostic programs as described in paragraph 4-17. During the program check all register lamps to ensure that they light and extinguish. Also check the operation of the EXTEND, OVERFLOW, FETCH, INDIRECT, and EXECUTE lamps, and ensure that the POWER lamp is lighted. Start and stop the program and ensure that the RUN and HALT lamps function correctly. Upon completion of the program stop the computer and check the operation of the PRESET lamp and switch, and the LOAD MEMORY, LOAD A, LOAD B, LOAD ADDRESS, DISPLAY MEMORY, and SINGLE CYCLE switches. If problems are encountered during the diagnostic program or in the functioning of switches or lamps, refer to section IV and correct the problems before proceeding.

b. Cables. With the POWER switch off, open the door assembly and check cables running to the door and core stack assembly for cracks, burns, wear, or pinching. Also inspect the ac power cable, paying particular attention to the portions of the cable near the connectors. Repair if necessary.

c. Cards and Plugs. Check all circuit cards and plugs for proper seating. Adjust where necessary.

d. Air Filters. Clean the air filters at the bottom of the large and small heat sink assemblies in the power supply (figure 5-1). Use the following procedure:

(1) Swing the card cage open.

(2) Remove the two air filters from the computer. On older models of the computer this is done by removing the clamp that holds each filter. On newer models, the filters are removed by first extracting the metal banana plug at each corner of the filter.

Table 5-1. Voltage Regulator Outputs

NOMINAL VOLTAGE	DC VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM
-2	-1.900	-2.000	-2.100
+4.5	+4.365	+4.500	+4.635
-12	-11.76	-12.00	-12.24
+22	(See table 5-2)		
-22	(See table 5-2)		
+32	(See table 5-3)		
+12	+11.40	+12.00	+12.60

WARNING

In the next step, use the compressed air nozzle with care. Never direct a compressed air stream toward a person.

(3) Take the air filters out of the computer room and blow the dirt from each filter. Blow in the opposite direction from that in which air normally moves through the filter. Then reinstall each filter. If compressed air is not available at the computer site, install two spare filters which have been cleaned elsewhere.

e. Dust. If required, blow dust and other light debris from the computer, using the blower output from a vacuum cleaner or other source of low pressure air. Loosen encrusted dust with a brush, and pay particular attention to heat dissipating areas.

f. Fans. Turn on the computer and check for proper action of the six cooling fans. Ensure that no object interferes with the rotation of the fan blades.

g. Voltage Checks. Before making voltage checks, the voltmeter must be allowed the warmup time prescribed by the manufacturer of the instrument. Also, the computer must run, with any type of program, for at least 15 minutes before making the voltage measurements. Voltage checks are then made as indicated below. If any voltage is not within the specified limits, make the necessary corrections.

(1) Stop the computer program.

(2) Measure the seven dc voltages listed in table 5-1. These voltages are available at test jacks on the overvoltage protection assembly.

(3) Set the voltmeter for reading rms ac voltage, and check each of the seven voltages listed in table 5-1 for ripple. For each voltage, the indicated ripple should be less than 10 millivolts.

5-25. Upon completing preventive maintenance procedures for the computer, correct any defects found, rerun the diagnostic programs, then proceed with preventive maintenance for I/O devices and optional features used by the computer.

5-26. PREVENTIVE MAINTENANCE SUMMARY.

5-27. Preventive maintenance for the 2116B Computer consists of the following:

a. Run the diagnostic programs, test lamps and switches, then turn off the computer.

b. Check cables for wear.

c. Check cards and plugs for proper seating.

d. Clean air filters.

e. Blow out dust, then turn on the computer.

f. Check operation of the six fans.

g. Check the voltages at the overvoltage protection assembly. (Refer to Tables 5-1, 5-2, and 5-3.)

h. Rerun the diagnostic programs.

i. Perform preventive maintenance for optional devices used by the computer.

Table 5-2. Output of +22 Volt and -22 Volt Regulators

TEMP. (° C)	DC VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM
0	23.30	23.80	24.30
1	23.26	23.76	24.26
2	23.22	23.72	24.22
3	23.18	23.68	24.18
4	23.14	23.64	24.14
5	23.10	23.60	24.10
6	23.06	23.56	24.06
7	23.02	23.52	24.02
8	22.98	23.48	23.98
9	22.94	23.44	23.94
10	22.90	23.40	23.90
11	22.86	23.36	23.86
12	22.82	23.32	23.82
13	22.78	23.28	23.78
14	22.74	23.24	23.74
15	22.70	23.20	23.70
16	22.66	23.16	23.66
17	22.62	23.12	23.62
18	22.58	23.08	23.58
19	22.54	23.04	23.54
20	22.50	23.00	23.50
21	22.46	22.96	23.46
22	22.42	22.92	23.42
23	22.38	22.88	23.38
24	22.34	22.84	23.34
25	22.30	22.80	23.30
26	22.26	22.76	23.26
27	22.22	22.72	23.22

NOTE: Voltages listed are negative for the -22 volt regulator

Table 5-2. Output of +22 Volt and -22 Volt Regulators (Cont)

TEMP. (° C)	DC VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM
28	22.18	22.68	23.18
29	22.14	22.64	23.14
30	22.10	22.60	23.10
31	22.06	22.56	23.06
32	22.02	22.52	23.02
33	21.98	22.48	22.98
34	21.94	22.44	22.94
35	21.90	22.40	22.90
36	21.86	22.36	22.86
37	21.82	22.32	22.82
38	21.78	22.28	22.78
39	21.74	22.24	22.74
40	21.70	22.20	22.70
41	21.66	22.16	22.66
42	21.62	22.12	22.62
43	21.58	22.08	22.58
44	21.54	22.04	22.54
45	21.50	22.00	22.50
46	21.46	21.96	22.46
47	21.42	21.92	22.42
48	21.38	21.88	22.38
49	21.34	21.84	22.34
50	21.30	21.80	22.30
51	21.26	21.76	22.26
52	21.22	21.72	22.22
53	21.18	21.68	22.18
54	21.14	21.64	22.14
55	21.10	21.60	22.10

NOTE: Voltages listed are negative for the -22 volt regulator

Tab

TEMP. (° C)
0
1
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e. Blow out dust, then turn on the computer.

f. Check operation of the six fans.

g. Check the voltages at the overvoltage protection ·mbly. (Refer to Tables 5-1, 5-2, and 5-3.)

h. Rerun the diagnostic programs.

i. Perform preventive maintenance for optional ices used by the computer.

Table 5-2. Output of +22 Volt and -22 Volt Regulators

TEMP. (° C)	DC VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM
0	23.30	23.80	24.30
1	23.26	23.76	24.26
2	23.22	23.72	24.22
3	23.18	23.68	24.18
4	23.14	23.64	24.14
5	23.10	23.60	24.10
6	23.06	23.56	24.06
7	23.02	23.52	24.02
8	22.98	23.48	23.98
9	22.94	23.44	23.94
10	22.90	23.40	23.90
11	22.86	23.36	23.86
12	22.82	23.32	23.82
13	22.78	23.28	23.78
14	22.74	23.24	23.74
15	22.70	23.20	23.70
16	22.66	23.16	23.66
17	22.62	23.12	23.62
18	22.58	23.08	23.58
19	22.54	23.04	23.54
20	22.50	23.00	23.50
21	22.46	22.96	23.46
22	22.42	22.92	23.42
23	22.38	22.88	23.38
24	22.34	22.84	23.34
25	22.30	22.80	23.30
26	22.26	22.76	23.26
27	22.22	22.72	23.22

NOTE: Voltages listed are negative for the -22 volt regulator

Table 5-2. Output of +22 Volt and -22 Volt Regulators (Cont)

TEMP. (° C)	DC VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM
28	22.18	22.68	23.18
29	22.14	22.64	23.14
30	22.10	22.60	23.10
31	22.06	22.56	23.06
32	22.02	22.52	23.02
33	21.98	22.48	22.98
34	21.94	22.44	22.94
35	21.90	22.40	22.90
36	21.86	22.36	22.86
37	21,82	22.32	22.82
38	21.78	22.28	22.78
39	21.74	22.24	22.74
40	21.70	22.20	22.70
41	21.66	22.16	22.66
42	21.62	22.12	22.62
43	21.58	22.08	22.58
44	21.54	22.04	22.54
45	21.50	22.00	22.50
46	21.46	21.96	22.46
47	21.42	21.92	22.42
48	21.38	21.88	22.38
49	21.34	21.84	22.34
50	21.30	21.80	22.30
51	21.26	21.76	22.26
52	21.22	21.72	22.22
53	21.18	21.68	22.18
54	21.14	21.64	22.14
55	21.10	21.60	22.10

NOTE: Voltages listed are negative for the -22 volt regulator

Table 5-3. Output of +32 Volt Regulator

TEMP. (° C)	VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM
0	33.10	33.60	34.10
1	33.03	33.53	34.03
2	32.97	33.47	33.97
3	32.90	33.40	33.90
4	32.84	33.34	33.84
5	32.78	33.28	33.78
6	32.71	33.21	33.71
7	32.65	33.15	33.65
8	32.58	33.08	33.58
9	32.52	33.02	33.52
10	32.46	32.96	33.46
11	32.39	32.89	33.39
12	32.33	32.83	33.33
13	32.26	32.76	33.26
14	32.20	32.70	33.20
15	32.14	32.64	33.14
16	32.07	32.57	33.07
17	32.01	32.51	33.01
18	31.94	32.44	32.94
19	31.88	32.38	32.88
20	31.82	32.32	32.82
21	31.75	32.25	32.75
22	31.69	32.19	32.69
23	31.62	32.12	32.62
24	31.56	32.06	32.56
25	31.50	32.00	32.50
26	31.43	31.93	32.43
27	31.37	31.87	32.37

Table 5-3. Output of +32 Volt Regulator (Cont)

TEMP. (° C)	VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM
28	31.30	31.80	32.30
29	31.24	31.74	32.24
30	31.18	31.68	32.18
31	31.11	31.61	32.11
32	31.05	31.55	32.05
33	30.98	31.48	31.98
34	30.92	31.42	31.92
35	30.86	31.36	31.86
36	30.79	31.29	31.79
37	30.73	31.23	31.73
38	30.66	31.16	31.66
39	30.60	31.10	31.60
40	30.54	31.04	31.54
41	30.47	30.97	31.47
42	30.41	30.91	31.41
43	30.34	30.84	31.34
44	30.28	30.78	31.28
45	30.22	30.72	31.22
46	30.15	30.65	31.15
47	30.09	30.59	31.09
48	30.02	30.52	31.02
49	29.96	30.46	30.96
50	29.90	30.40	30.90
51	29.83	30.33	30.83
52	29.77	30.27	30.77
53	29.70	30.20	30.70
54	29.64	30.14	30.64
55	29.58	30.08	30.58

5-28. CORRECTIVE MAINTENANCE.

5-29. ELECTRICAL ADJUSTMENTS.

5-30. VOLTAGE REGULATOR ADJUSTMENT.

5-31. Introduction. The computer has seven adjustable voltage regulators, furnishing the following nominal voltages: +4.5, -2, +12, -12, +22, -22, and +32 volts. The outputs of some of these voltage regulators affect the outputs of others; therefore, adjustment of one regulator may necessitate adjustment of additional regulators. Furthermore, the regulators must be adjusted in a prescribed sequence.

5-32. The output voltage to which each regulator is adjusted, and the sequence of adjustment, are shown in table 5-4. Also listed in the table is the potentiometer which is adjusted for each of the seven regulated voltages. The outputs of the +22, -22, and +32 volt regulators are set in accordance with the ambient temperature at the time of adjustment; tables 5-5 and 5-6 show the voltages required for various temperatures.

5-33. When adjustment procedures have been completed, all voltages are rechecked. The regulators are readjusted, if required, again following the sequence specified in table 5-4.

5-34. Equipment. Adjustment of the voltage regulators requires the following equipment:

a. One digital voltmeter, of the type listed in Table 1-5.

b. One Centigrade thermometer (for measuring room temperature), accurate to at least ±1 degree.

5-35. Procedure. Adjustment of each of the seven voltage regulators is essentially the same, and the procedure given below applies to each of the regulators. The adjustment starts with preliminary procedures, including a check of the ac power line voltage. If more than one voltage regulator is adjusted, the preliminary procedures (steps "a" through "f" below) need not be repeated after adjusting the first regulator. The adjustment procedure is as follows:

a. Place the thermometer near the computer. Select a position free of cold drafts and away from heat-radiating objects. Do not place the thermometer on or in the computer. Allow time for the thermometer to reach ambient temperature before reading it.

b. Turn on the voltmeter. Before using the instrument allow the warmup time prescribed by the manufacturer.

c. If the computer is off, turn it on by pressing the POWER switch. Also turn on all optional devices used by the computer. Allow 15 minutes warmup time for the computer. During this time, a program (of any type) must be running. The program will exercise the core stack assembly and bring it to normal operating temperature.

d. When the computer and voltmeter have warmed up, stop the computer program. Then set the voltmeter to the proper ac range and measure the power line voltage applied to the computer. If the computer is connected for 115-volt operation, the line voltage should be between 103.5 and 126.5 volts rms. For 230-volt operation, the line voltage should be between 207.0 and 253.0 volts rms.

e. If the power line is above or below the permissible limits, do not attempt to adjust the voltage regulators. Turn off the computer and associated optional devices, and leave them off until the line voltage fault has been corrected. If the line voltage is satisfactory, proceed with the voltage regulator adjustment.

Table 5-4. Voltage Adjustments

ADJUSTMENT SEQUENCE	NOMINAL VOLTAGE	ADJUSTMENT POTENTIOMETER	VOLTAGE RANGE		
			MINIMUM	CENTER	MAXIMUM
1st	-2	R76*	-1.980	-2.000	-2.020
2nd	+4.5	R66*	+4.455	+4.500	+4.545
3rd	-12	R125**	-11.88	-12.00	-12.12
4th	+22	R140**		(See table 5-5)	
5th	-22	R155**		(See table 5-5)	
6th	+32	R170**		(See table 5-6)	
7th	+12	R96*	+11.88	+12.00	+12.12

NOTES:
* Situated on Logic Supply Regulator Card A301.
** Situated on Memory Supply Regulator Card A302.

Table 5-5. Adjustment of +22 Volt and -22 Volt Regulators

TEMP. (° C)	NOMINAL VOLTAGE	TEMP. (° C)	NOMINAL VOLTAGE
0	23.80	28	22.68
1	23.76	29	22.64
2	23.72	30	22.60
3	23.68	31	22.56
4	23.64	32	22.52
5	23.60	33	22.48
6	23.56	34	22.44
7	23.52	35	22.40
8	23.48	36	22.36
9	23.44	37	22.32
10	23.40	38	22.28
11	23.36	39	22.24
12	23.32	40	22.20
13	23.28	41	22.16
14	23.24	42	22.12
15	23.20	43	22.08
16	23.16	44	22.04
17	23.12	45	22.00
18	23.08	46	21.96
19	23.04	47	21.92
20	23.00	48	21.88
21	22.96	49	21.84
22	22.92	50	21.80
23	22.88	51	21.76
24	22.84	52	21.72
25	22.80	53	21.68
26	22.76	54	21.64
27	22.72	55	21.60

NOTES:

1. Voltages listed are negative for the -22 volt regulator.
2. Voltage must be adjusted to within ±0.1 volt of the amount shown.

Table 5-6. Adjustment of +32 Volt Regulator

TEMP. (° C)	NOMINAL VOLTAGE	TEMP. (° C)	NOMINAL VOLTAGE
0	33.60	28	31.80
1	33.53	29	31.74
2	33.47	30	31.68
3	33.40	31	31.61
4	33.34	32	31.55
5	33.28	33	31.48
6	33.21	34	31.42
7	33.15	35	31.36
8	33.08	36	31.29
9	33.02	37	31.23
10	32.96	38	31.16
11	32.89	39	31.10
12	32.83	40	31.04
13	32.76	41	30.97
14	32.70	42	30.91
15	32.64	43	30.84
16	32.57	44	30.78
17	32.51	45	30.72
18	32.44	46	30.65
19	32.38	47	30.59
20	32.32	48	30.52
21	32.25	49	30.46
22	32.19	50	30.40
23	32.12	51	30.33
24	32.06	52	30.27
25	32.00	53	30.20
26	31.93	54	30.14
27	31.87	55	30.08

NOTE: Voltage must be adjusted to within ±0.1 volt of the amount shown.

f. If the computer is running, stop the program by pressing the HALT switch.

g. Set the voltmeter for measuring the dc voltage to be adjusted.

h. Connect one lead of the voltmeter to the ground test jack on overvoltage protection assembly A121. (Observe polarity.)

i. Connect the other lead of the voltmeter to the test jack on the overvoltage protection assembly marked with the dc voltage to be adjusted.

j. With a small screwdriver, adjust the voltage regulating potentiometer to bring the regulated voltage to about the center of the required range. (Refer to table 5-4.) Note that the adjustment voltage range is narrower than the range specified in table 5-1, 5-2, or 5-3.

k. When the voltage has been brought within the required range, measure the voltages listed below it in table 5-4. (The voltages are all available at test jacks on the overvoltage protection assembly.) If any voltage is not within the limits specified in table 5-4, adjust it. Then proceed with measuring the remaining voltages listed in table 5-4, and adjust any of these not within the required limits.

l. When the regulators have been checked and adjusted, make a final measurement of the seven adjustable regulated voltages. Readjust as required, again in the sequence specified in table 5-4. At the end of the adjustment procedure, make a final check of the seven voltages.

5-36. Summary of Voltage Regulator Adjustment. The principal steps in adjusting a voltage regulator are as follows:

a. Measure the power line voltage. The voltage should be 103.5 to 126.5 volts (207.0 to 253.0 volts for 230-volt operation).

b. Connect the voltmeter to the appropriate test jack on the overvoltage protection assembly.

c. Adjust the appropriate voltage regulating potentiometer in accordance with table 5-4.

d. Check the remaining voltages listed in table 5-4. Adjust as required.

e. Measure all voltages available at the test jacks on the overvoltage protection assembly. Readjust as necessary. After completion of adjustments, make a final check of all voltages.

5-37. CURRENT LIMITER ADJUSTMENT. The computer has two adjustable current limiters; these are used for the +4.5 volt and -2 volt power supplies. Maladjustment of these regulators is indicated by an inability to correctly adjust the voltage regulator for the dc voltage concerned. (Inability to adjust a voltage regulator may also be due to other causes.)

5-38. The potentiometers for adjusting the +4.5 and -2 volt current regulators are R69 and R84 respectively, situated on logic supply regulator card A301. The potentiometers are factory sealed, and must not be adjusted in the field. (Test and loading equipment for making the adjustment normally is not available at field installations.) If adjustment of potentiometer R69 or R84 seems required, consult the nearest Hewlett-Packard Sales and Service Office.

5-39. POWER FAIL ADJUSTMENT. The following procedure describes how to adjust for the threshold voltage (power line voltage) at which the power fail interrupt occurs (100 to 102 volts rms ac for 115-volt operation, 200 to 204 volts rms ac for 230-volt operation). The adjustment procedure applies to a computer which does not use the Power Fail Interrupt With Automatic Restart Option (option 08). To determine whether the computer has this option, turn off computer power with the POWER switch, and partially withdraw the card from card cage slot 1. If this card has part number 12588-6001 marked on it, refer to the operating and service manual for the 08 option for the power fail adjustment procedure. (The manual part number is 12588-9002.) If the card in slot 1 has part number 02116-6175 marked on it, the procedure which follows is applicable.

5-40. Two methods of making the power fail adjustment are presented. First, a precise adjustment procedure is described, which accurately sets the threshold voltage. Then a coarse adjustment procedure is described, which can be used as a temporary measure until equipment for making the precise adjustment is obtained.

CAUTION

The power fail interrupt causes a program jump to core storage location 4. If there is no power fail interrupt program in the computer, location 4 should contain a halt instruction. Otherwise a jump may occur from location 4 to a program which will destroy wanted data or cause undesired operation of I/O devices or controlled equipment.

5-41. Equipment Required. The coarse adjustment requires one Hewlett-Packard Extender Board (part no. 02116-6040).

5-42. The precise adjustment requires the following:

a. One Hewlett-Packard Extender Board (part no. 02116-6040).

b. One ac digital voltmeter with at least a 3-digit display, or an expanded scale ac voltmeter. The meter must be capable of reading ac voltage to within ±1 percent of the true value.

c. One general-purpose oscilloscope.

d. One variable autotransformer capable of supplying sufficient power for the computer. The 2116B requires 1000 to 1600 watts, depending on the optional features used. (To reduce the power requirement of the computer to a minimum, all printed circuit cards for optional features can be removed before making the adjustment. Be sure to turn off power before removing or installing cards. (Remove cards by sliding them out two to three inches.) The autotransformer must be capable of reducing the power-line voltage to 100 volts rms if the computer is connected for 115-volt operation, or to 200 volts rms if the computer is connected for 230-volt operation. If only the more commonly available 115-volt type of autotransformer can be obtained, a 230-volt computer can be temporarily connected for 115-volts for the purposes of making the adjustment, and operated from a 115-volt power source. If this is done, be sure to reconnect the computer for 230-volt functioning after completing the adjustment.

5-43. Precise Adjustment. The precise power fail adjustment is made as follows:

a. Turn on the voltmeter and oscilloscope. Allow the prescribed warmup time before using these instruments.

b. Turn off the computer by means of the POWER switch.

c. Remove the Parity Error card (part no. 12591-6001) from slot 3 if the computer has this optional card installed.

d. Using the extender board, extend the power fail interrupt card for test. This card is in slot 1.

e. Connect the autotransformer between the computer and the power line.

f. Connect the voltmeter for measuring the output voltage of the transformer.

g. Set the autotransformer to furnish 115 volts rms to the computer (230 volts if the computer is connected for 230-volt operation).

h. Turn on the computer by pressing the POWER switch. Allow 15 minutes warmup time for the computer before making the adjustment. A program can be run during this time, if desired.

i. Adjust the oscilloscope for 1 volt/centimeter vertical deflection, and a sweep rate of 1 millisecond/centimeter.

j. Connect the ground lead of the oscilloscope to the negative lead of capacitor C2 on the power fail interrupt card. (This point is at card ground potential.)

k. After the computer and test instruments have warmed up, stop the computer (if it is running) by pressing the HALT switch.

l. Adjust the oscilloscope to set the horizontal trace at the center of the screen. Connect the oscilloscope probe to test jack TP on the power fail interrupt card.

m. Press the PRESET switch.

n. With the autotransformer, adjust the power input to the computer to 100 volts rms (200 volts for a 230-volt computer).

o. On the power fail interrupt card, adjust potentiometer R7 to the center of its range of rotation.

p. Adjust the oscilloscope to obtain a display of two positive-going pulses. Do not alter the vertical gain.

q. Adjust potentiometer R7 on the power fail interrupt card until the positive peaks of the pulses are +1.0 to +1.5 volts. (See figure 5-1.) The pulse base line on the oscilloscope is below ground level; be sure to measure the pulse peaks with respect to ground, not with respect to the base line.

NOTE

After R7 has been set, the peak amplitude may drift above or below the +1.0 to +1.5 volt range. This is a normal condition caused by power line voltage variations.

r. With the autotransformer, adjust the power input to the computer to 102 volts rms (204 volts for a 230-volt computer).

s. Check the power fail adjustment by running the Power Fail Interrupt Test diagnostic program (tape no. 20434A or its latest revision). While the program is running, reduce the power input to the computer to 100 volts rms (200 volts for a 230-volt computer). A power fail interrupt should occur as the voltage is being reduced.

t. Turn off the computer by means of the POWER switch.

u. Remove the extender board, and install the power fail interrupt card in slot 1. Components on the board must be to the right.

v. Install the parity error card in slot 3, if this card is used. Components on the board must be to the right.

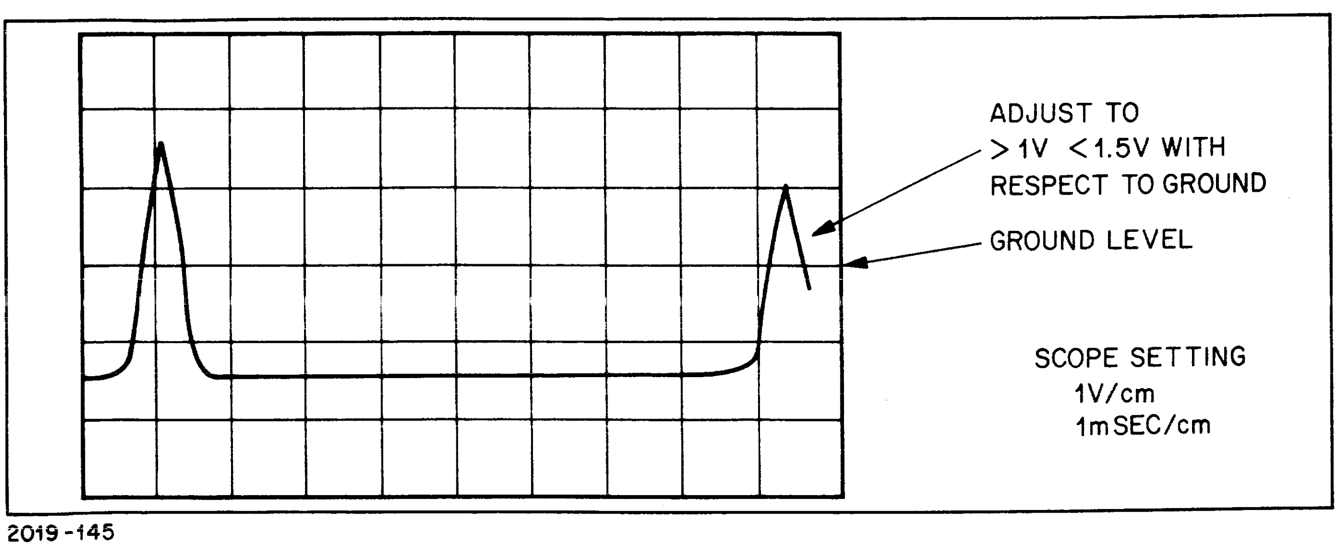

Figure 5-1. Properly Adjusted Power Fail Pulses

w. Unplug the autotransformer.

x. Plug the computer power cord into the electrical outlet, and turn on computer power.

5-44. Coarse Adjustment. A coarse adjustment of the power fail threshold voltage can be made without the use of a variable ac source, oscilloscope or voltmeter. However, this procedure is recommended for temporary purposes only, and must be followed by proper adjustment as soon as practicable. The only equipment required is the Extender Board (part no. 02116-6040). An oscilloscope will be helpful, but is not essential. The procedure is as follows:

a. Turn on the oscilloscope, if one is available. Allow the prescribed warmup time before use.

b. Turn off the computer by means of the POWER switch.

c. Remove the Parity Error card (part no. 12591-6001) from slot 3 if the computer has this optional card installed.

d. Using the extender board, extend the power fail interrupt card for test. This card is in slot 1.

e. Turn on the computer by pressing the POWER switch. Allow 15 minutes warmup time for the computer before making the adjustment. A program can be run during this time, if desired.

f. Adjust the oscilloscope for 1 volt/centimeter vertical deflection, and a sweep rate of 1 millisecond/centimeter.

g. Connect the ground lead of the oscilloscope to the negative lead of capacitor C2 on the power fail interrupt card. (This point is at card ground potential.)

h. After the computer and oscilloscope have warmed up, stop the computer (if it is running) by pressing the HALT switch.

i. Adjust the oscilloscope to set the horizontal trace at the center of the screen.

j. Connect the oscilloscope, if used, to test jack TP on the power fail interrupt card.

k. On the power fail interrupt card, rotate potentiometer R7 fully counterclockwise.

l. Press the PRESET switch.

m. Rotate R7 slowly clockwise until pulses are observed on the oscilloscope or until the PRESET indicator lights.

n. Rotate R7 one-quarter turn counterclockwise from the point at which pulses were observed or at which the PRESET indicator lighted.

o. Press the POWER switch off and replace all circuit cards in their normal positions. Components on the cards must face to the right.

p. Restore the computer to normal use, and observe its operation. If the power failure interrupt occurs without noticeable line voltage problems, rotate R7 counterclockwise one-sixteenth of a turn. If power fail interrupts still occur, obtain the proper equipment and make the precise adjustment of R7.

5-45. MECHANICAL ADJUSTMENTS.

5-46. CARD CAGE DETENT ADJUSTMENT. The card cage detent mechanism ensures that the card cage is held in the correct position for sliding the cage in and out of the computer cabinet. Two spring plungers form the principal operating units, as illustrated in figure 5-2. Each plunger consists of a hollow set screw containing a spring loaded detent stud. When the card cage is swung shut, the spring loaded stud snaps into a groove, and the cage is held in the correct position for sliding into the computer cabinet.

5-47. Adjustment of the spring plunger is necessary if the plunger is too high or too low. If the plunger is too low, excessive force is needed to swing the card cage into and out of the detent position. If the plunger is too high, the card cage will not be held in the correct position for sliding the cage in and out of the computer cabinet. Furthermore, if the plunger is too high it may fail to withdraw the card cage slide from the computer cabinet when the card cage is pulled out.

5-48. The spring plungers are adjusted by turning them with a screwdriver. (A nylon locking stud in the side of each plunger holds the plunger in its adjusted position.) The adjustment procedure is as follows:

a. Press the POWER switch off.

b. Slide the card cage from the computer cabinet.

c. Unscrew both spring plungers until no detent action occurs when the card cage is swung open and shut.

d. Screw down one of the plungers until satisfactory detent action is encountered.

e. Screw down the second plunger until excessive force is required to swing the card cage into and out of the detent position. Then unscrew the second plunger until satisfactory detent action occurs.

5-44A. SENSE AMPLIFIER 02115-6001 ADJUSTMENT.

Note

Sense amplifier 02116-6298 is not adjustable.

5-44B. Equipment. Adjustment of the sense amplifier requires the following equipment:

a. One extender card (02116-6040).
b. One extender cable (02115-6047).
c. One high-frequency oscilloscope.
d. One non-magnetic screwdriver.

5-44C. Procedure. Adjustment of each sense amplifier circuit is the same and the procedure given below applies to each of these circuits.

a. At the computer front panel, press and release the POWER switch to turn off power.

b. Open the door assembly to expose the circuit cards.

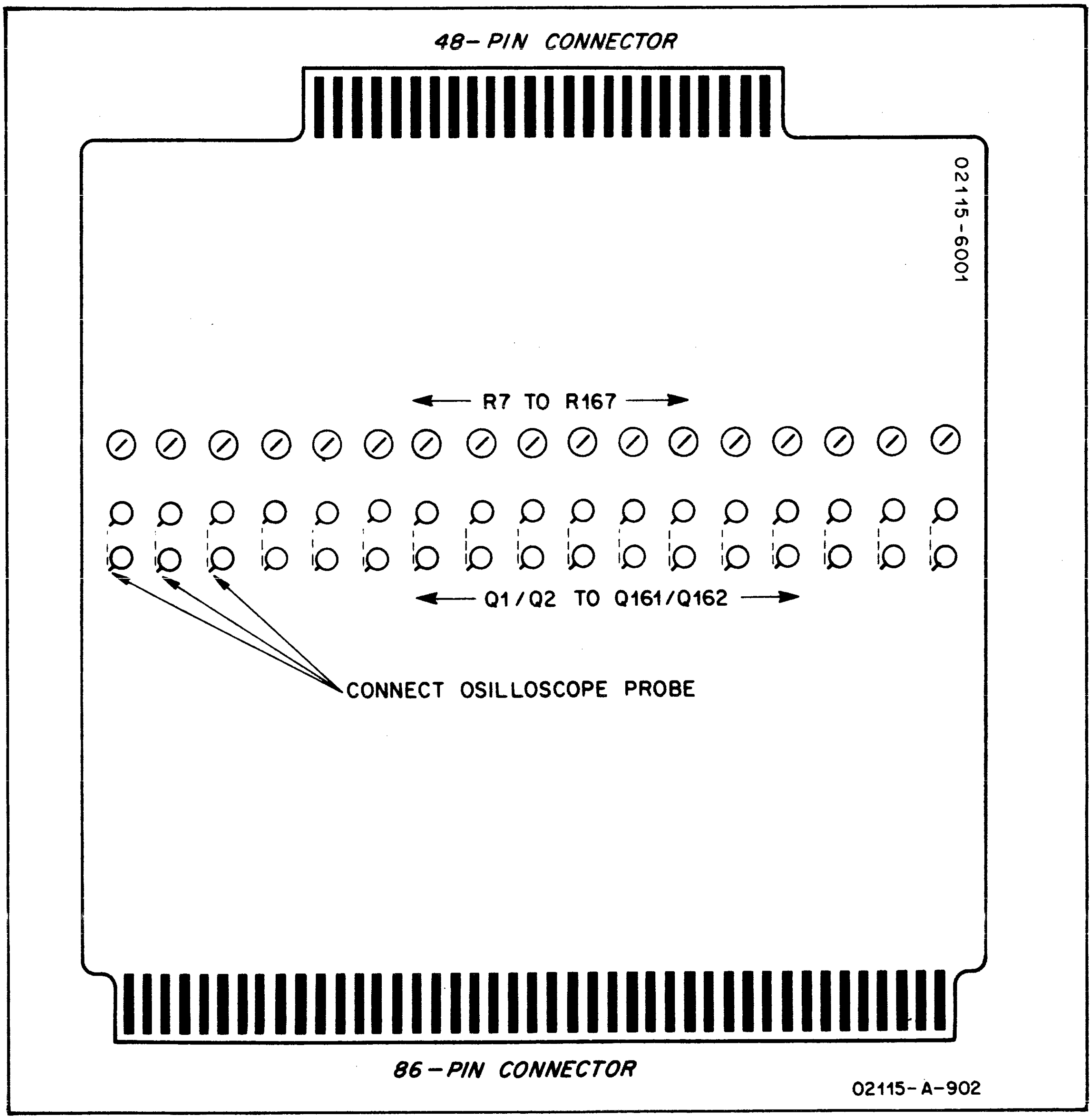

Figure 5-1A. Adjustment Locations on Sense Amplifier Board

c. At the front of the card cage assembly, locate the sense amplifier cards A10, A11, A12, and A13.

d. Remove the core stack cable connector from one sense amplifier card.

e. Remove the sense amplifier card from the card slot.

f. Insert the extender card into the sense amplifier card slot.

g. Insert the sense amplifier card into the extender card. (Be sure the card is oriented properly.)

h. Connect the extender cable to the sense amplifier card and the core stack cable connector.

i. At the computer front panel, press and release the POWER switch to turn power on.

Note

Do not omit step "j" below, otherwise data in the protected area will be destroyed.

j. Make sure the LOADER switch is at the PROTECTED position.

k. Press and release the PRESET switch.

l. Set all SWITCH REGISTER switches to logic 0 (down) position.

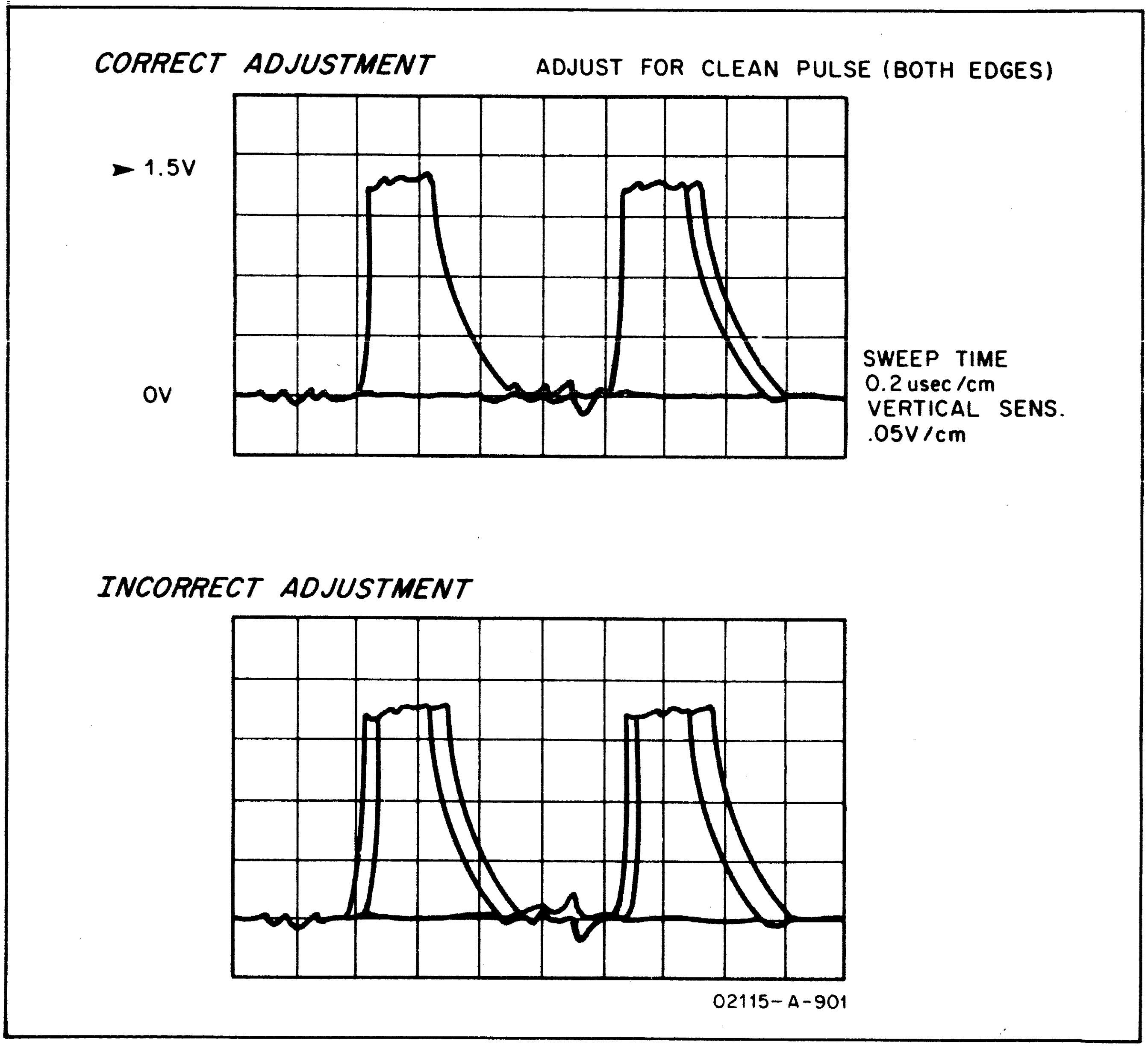

Figure 5-1B. Sense Amplifier Balancing Waveforms

m. Press and release the LOAD ADDRESS switch.

n. Set the SWITCH REGISTER switches to 070000 (octal).

o. Press and release the LOAD A switch.

p. Press and release the SINGLE CYCLE switch.

q. Set the PHASE switch (on the back of the door assembly) to the LOOP position.

r. Set into the SWITCH REGISTER switches the 16-bit test word which is to be stored (177777).

s. Press and release the LOAD A switch.

t. Press and release the RUN switch.

u. Connect the oscilloscope synchronization probe to the timing generator card test point A106TP1 (time T0).

v. Consecutively connect the oscilloscope test probe to the collectors of the output transistor pairs (Q1/Q2, Q11/Q12, Q21/Q22, etc. through Q161/Q162) and adjust the corresponding balance adjustment (R7, R17, R27, etc. through R167) for the cleanest possible pulse. Use only the first displayed pulse for observation; disregard succeeding pulses. See figure B-1 for adjustment locations. See figure B-2 of correct and incorrect waveforms.

w. When all transistor pairs of one sense amplifier card have been checked; press and release the HALT switch, remove the extender cable, sense amplifier and the extender card and reinstall the sense amplifier card in its original position.

x. Repeat steps "d" through "w" for all remaining sense amplifier cards.

y. After all sense amplifier cards have been checked, adjusted, and returned to their original positions, the memory diagnostics should be run to ensure memory stability.

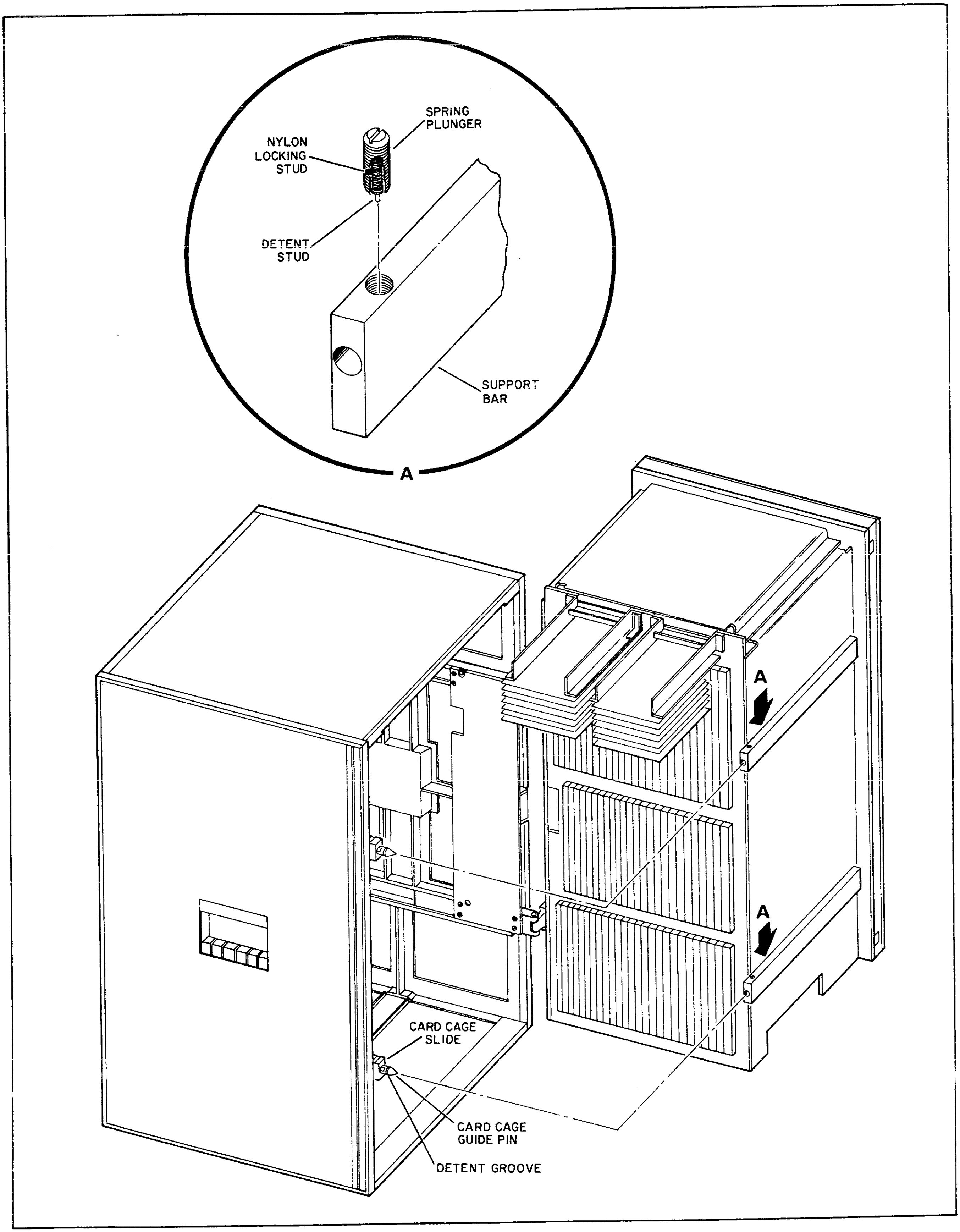

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Figure 5-2. Card-Cage Detent Adjustment

5-49. CARD CAGE ROLLER ADJUSTMENT. The card cage slides into the computer cabinet on ball bearing rollers. (See figure 5-3.) Three of these rollers are used for each card cage slide; two are situated at the bottom of the slide and one at the top. The top roller can be raised or lowered, and locked into position, to permit the card cage to slide properly in and out of the computer cabinet.

5-50. Adjustment of a card cage roller is necessary if the roller is too high or too low. If the roller is too high, the card cage does not slide freely in and out of the computer cabinet. If the roller is too low, the card cage wobbles when it slides in or out.

5-51. Each of the upper ball bearing rollers is mounted on a screw which has an eccentric shoulder. By turning the screw, the roller is moved up or down. One-half turn of the screw moves the roller from its highest position to its lowest position. A cap nut locks the eccentric screw in the position required.

5-52. The adjustment procedure for the upper or lower roller on the left side of the computer (viewing the computer from the front) is as follows:

a. Turn off the computer by means of the POWER switch.

b. Remove the left side-cover of the computer cabinet.

c. Slide the card cage from the computer cabinet.

d. Swing the card cage open.

e. Loosen the cap nut which locks the roller to be adjusted. When doing this, use a screwdriver to prevent the eccentric screw from turning.

f. With the screwdriver, turn the eccentric screw to raise the ball bearing against the surface on which it rolls.

g. Holding the eccentric screw in adjustment with the screwdriver, tighten the cap nut.

h. Check the adjustment by moving the card cage slide in and out of the computer cabinet. The slide should move freely, but should have no vertical play. Repeat the adjustment if necessary.

i. Replace the side cover on the computer cabinet.

5-53. The adjustment procedure for the upper or lower roller on the right side of the computer (viewing the computer from the front) is described below. The procedure requires two persons.

a. Turn off the computer by means of the POWER switch.

b. Remove the right side-cover of the computer cabinet.

c. Slide the card cage from the computer cabinet.

d. Swing the card cage open.

NOTE

In steps e through i which follow, the weight of the card cage must be supported by one person while a second person makes the adjustments.

e. Remove the support plate from the inner right side of the computer cabinet.

f. Loosen the cap nut which locks the roller that is to be adjusted. When doing this, use a screwdriver to prevent the eccentric screw from turning.

g. Turn the eccentric screw to raise the ball bearing roller against the surface on which it rolls.

h. Hold the eccentric screw in adjustment and tighten the cap nut.

i. Install the support plate.

j. Check the adjustment by sliding the card cage in and out of the computer cabinet. The cage should move freely, but the card cage slide should have no vertical play. Repeat the adjustment if necessary.

k. Install the side cover on the computer cabinet.

5-54. DOOR HINGE. There is no adjustment for the door hinge.

5-55. CARD CAGE HINGE. There is no adjustment for the card cage hinge. Sagging of the card cage indicates that the right-hand card cage slides need adjustment.

5-56. DOOR LATCH. There is no adjustment for the door latch. During assembly of the computer the two vertical catch rods actuated by the door latch are ground at the ends to provide the required latching action.

5-57. REMOVAL AND REPLACEMENT PROCEDURES.

5-58. The following paragraphs describe the methods for removing and installing various assemblies and units in the computer. Before performing any of the procedures, read the entire description of the procedure. Heed all warning and caution notices.

CAUTION

Failure to observe the precaution in the following procedure description may result in damage to components on circuit cards.

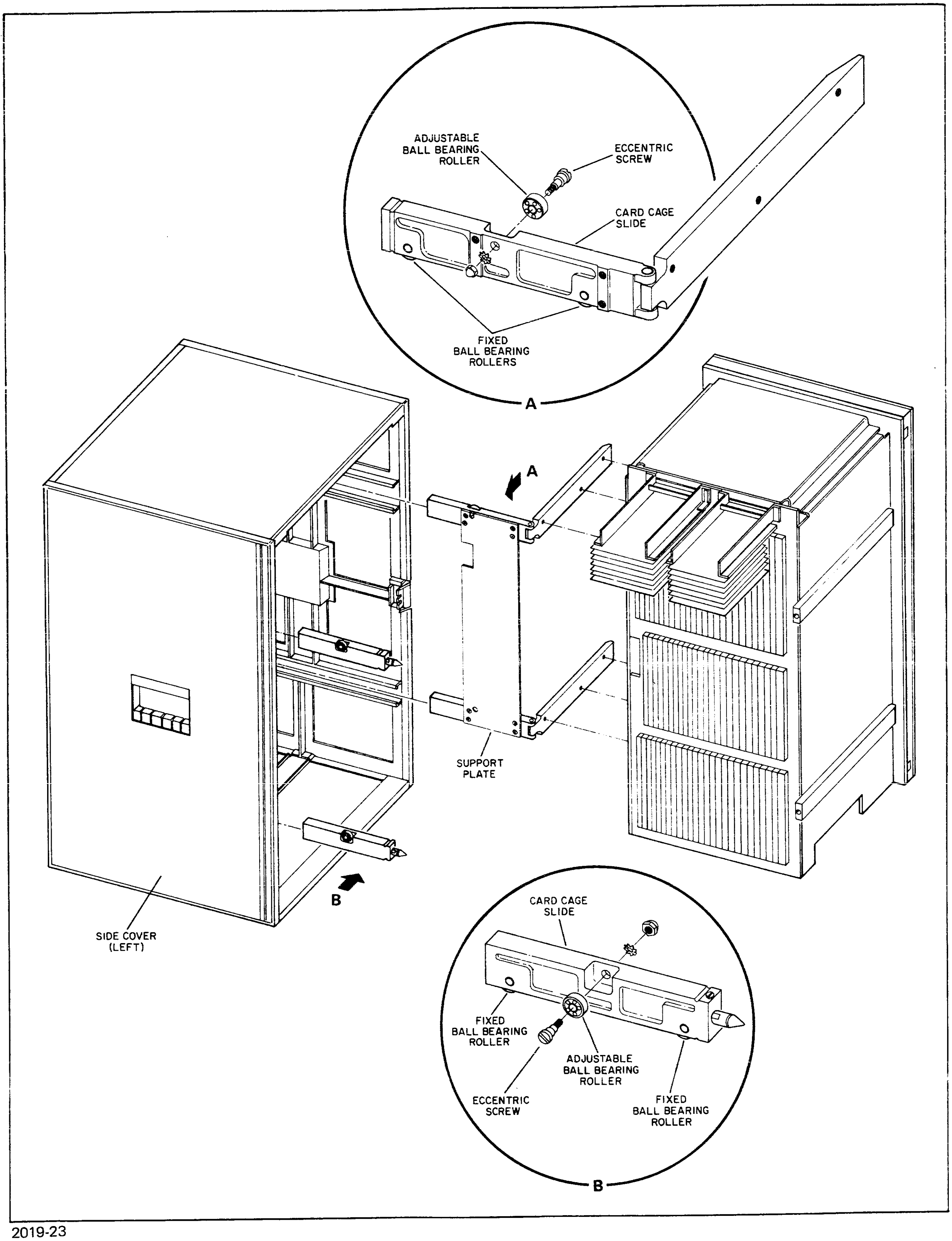

Figure 5-3. Card-Cage Slide Adjustment

5-59. CARD REMOVAL AND REPLACEMENT. Before removing or installing cards in the power supply section, turn off power and allow 3 minutes for filter capacitors to discharge.

5-60. Before removing or installing cards in the card cage, turn off power and allow 5 seconds for bypass capacitors to discharge.

5-61. To remove a card from the power supply section, first take out the retaining screw near the center of the card (figure 1-4). Then withdraw the card by pulling it upward.

5-62. To remove a card from the card cage, first take off the card retainer. Remove the front connector from the card (if any), loosen the card by pulling outward on the plastic levers at the top and bottom of the card, then withdraw the card.

5-63. When removing or installing cards from the card cage, use extreme care not to damage traces or protruding components on the card or on adjacent cards.

5-64. Cards must be installed in the card cage with components to the right.

5-65. Cards in the card cage are keyed to prevent full insertion if upside down, but they are not keyed to prevent installation in the wrong slot. Therefore, make sure that the reference designation on the card extractor lever corresponds to the number of the slot being used. Similarly, care must be exercised that the two cards in the power supply section are not interchanged.

CAUTION

Failure to observe the following precaution may result in shorting the +7 volt supply.

5-66. LAMP REPLACEMENT. Before removing a lamp from display board assembly A501, turn off power. Otherwise, when the metal strip which makes contact with the base of the lamp is swung aside, it may contact a point at ground potential and cause a short.

CAUTION

Failure to observe the following precautions may result in damage to components.

5-67. REPLACEMENT OF SEMICONDUCTOR DEVICES. When replacing semiconductor devices, be sure not to omit the insulating washer which separates the device from the mounting surface, if such a washer is used. These washers are shown in the applicable parts location diagrams in this section.

5-68. When directed to do so by a note on a parts location diagram, be sure to use silicone heat-conducting compound when installing a semiconductor device.

5-69. POWER TRANSFORMER REPLACEMENT. If power transformer A311T1 requires replacement, return the computer to the factory. Refer to paragraph 2-45 for instructions on packing and shipping the computer.

5-70. INTEGRATED CIRCUIT REPLACEMENT. Do not attempt to remove or install an integrated circuit unless a soldering iron specially made for this purpose is available. A rubber bulb with a suction tube for withdrawing molten solder is also an essential tool.

WARNING

When replacing a filter capacitor as described below, be sure polarity is correct. Reversed polarity will lead to heating within the capacitor and the possibility of explosion.

5-71. FILTER CAPACITOR REPLACEMENT. To replace a filter capacitor which is under filter capacitor assembly A303, refer to figure 5-34 to determine the location of the capacitor, then proceed as follows:

a. Press the POWER switch off.

b. Unplug the ac power cable from the ac outlet or from the back of the computer.

c. Wait 3 minutes for filter capacitors to discharge.

d. Remove the rear cover from the computer.

e. Loosen the five rear retaining screws for capacitor board assembly A303 (figure 5-4).

f. Remove logic supply regulator card A301.

g. Remove memory supply regulator card A302.

h. Remove the screw from the negative terminal of the capacitor to be replaced.

i. Remove the nut from the positive terminal of the capacitor to be replaced.

j. Remove the small screw from the left end of the front (+4.5 volt) bus bar.

k. Remove the four nuts which hold down the front edge of the capacitor board.

l. Remove the three screws along the bottom of the capacitor board bracket in front of the capacitors, and remove the bracket.

m. Lift the front edge of the capacitor board, raising capacitors still fastened to it, and remove the capacitor to be replaced. If necessary, remove capacitors which are in front of it. Mark the reference designation on each good capacitor as it is removed. If the capacitor board cannot be raised high enough to clear the stud in the positive terminal of a capacitor, remove the stud with an Allen wrench. If the board still cannot be raised high enough, remove the right side cover of the computer cabinet, and loosen the +4.5 volt bus bar.

n. Remove the defective capacitor. Remove the stud from the positive terminal of the capacitor, mark the capacitor as faulty, and discard it in a waste receptacle. Do not place the defective capacitor with or near good capacitors.

o. Install the replacement capacitor. Use great care in ensuring that polarity is correct. Before installing the capacitor, determine from figure 5-34 the side of the capacitor which will be in front, and mark that side "front".

p. Reinstall any capacitors which were removed to gain access to the faulty capacitor. Use great care in ensuring that polarity is correct, and that each capacitor is replaced in its original position. Before installation, mark each capacitor with its reference designation (refer to figure 5-34) and mark the front side.

q. Reassemble all parts that were removed or loosened, using the reverse order from disassembly. Be sure that screws are tight, but do not strip threads. Replace all covers, close the card cage and slide the cage into the computer.

WARNING

Because of the possibility of explosion and resulting injury, be sure all covers are installed and the card cage is slid into the computer, before performing the next steps.

r. Plug in the ac power cable.

s. Make preparations for measuring the seven regulated voltages, as described in paragraph 5-24, step g. However, do not allow the prescribed 15-minute warmup period for the computer.

t. Press the POWER switch on.

u. Quickly measure the voltage and ripple of the seven regulated voltages. Because of the lack of warmup, voltage deviations slightly greater than normal can be tolerated.

v. If any voltage is incorrect or has excessive ripple, turn off the computer immediately. Wait at least one hour for any incorrectly connected capacitor to cool, then make sure that filter capacitors have been correctly installed.

w. If the voltages are within the prescribed limits or only slightly beyond them, run any type of program for about 15 minutes, stop the computer, and recheck voltage levels and ripple. All measurements should now be within the prescribed limits.

5-72. REPLACEMENT OF CORE STACK ASSEMBLY. If a core stack assembly is defective, it must be returned to the factory for repair or replacement. The removal procedure is as follows:

CAUTION

Do not attempt to disassemble a core stack assembly. Irreparable damage may result. Do not remove diodes from the diode matrix assembly. Core stacks are easily damaged if mishandled.

a. Press the POWER switch off.

b. Unplug the ac power cable from the ac outlet or from the back of the computer.

c. Swing the card cage open.

d. Remove the nine screws around the side and rear edges of the card cage top cover.

e. Remove the card cage top cover.

f. Remove the three screws at the top of the card cage, across the front, which hold the memory cable spacing bracket.

g. Remove the memory cable spacing bracket.

h. Unplug the memory cables from the cards in the card cage.

i. Starting with the screws farthest from the card cage hinge, carefully remove the four screws which hold the core stack assembly in place, and remove the assembly.

5-73. Installation procedure is the reverse of the above. When installing the memory cable bracket, exercise care not to pinch the memory cables.

5-74. BACKPLANE CONNECTOR REPLACEMENT. Because of the numerous wires attached to backplane connectors, replacement of a connector should not be attempted in the field. If replacement is necessary, return the computer to the factory for installation of a new backplane. See a paragraph 2-45 for information on packing the computer for shipment.

5-75. REPLACEMENT OF BACKPLANE-CONNECTOR CONTACTS AND BACKPLANE WIRING. For replacing backplane-connector contacts, and for removing and installing wires to these contacts, use the tools listed in paragraph

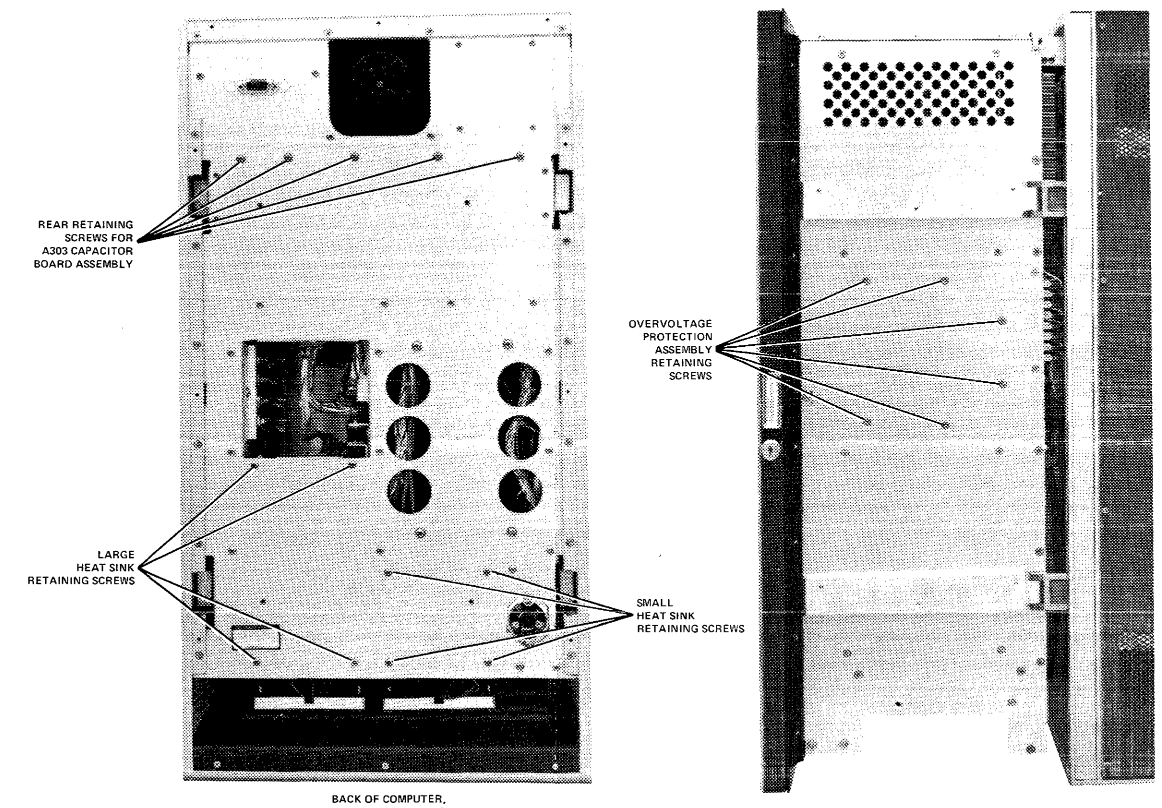

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Figure 5-4. Removal of Assemblies

1-55 and 1-56. Instructions for using these tools are furnished in the following pamphlets, published by AMP Incorporated, Harrisburg, Pennsylvania:

a. A-MP TERMI-POINT Handbook, Amp publication no. 5070.

b. A-MP TERMI-POINT Tool and Clip Selection Chart, Amp publication no. GP 1935.

c. A-MP TERMI-POINT Manual Tool Mandrel Specifications, AMP publication no. GP 2075.

d. A-MP TERMI-POINT Component Color Code Data, Amp publication no. GP 1944.

e. Quality Control Procedure for A-MP TERMI-POINT Clip Applications, Amp publication no. GP 1920.

f. A-MP TERMI-POINT Extraction Tool, Amp publication no. IS 1942.

g. A-MP TERMI-POINT Pull Test Tool, Amp publication no. IS 1933.

h. Operator's Quality Check Procedure for A-MP TERMI-POINT Clip Application, Amp publication no. GP 2019.

i. A-MP TERMI-TWIST Contact Replacement Tool, Amp publication no. IS 2038.

5-76. The following information is pertinent to use of the wiring tools:

a. Wiring post size is 0.031 x 0.062 inch.

b. Wires between backplane connectors are 26 gauge (American Wire Gauge), 7 strand, and insulation thickness is between 0.022 and 0.045 inch.

5-77. Wires which run from A100TB1, A100TB2, and A200TB1 to backplane connectors have a quick-disconnect lug which solders onto a contact for the backplane connector. A light soldering iron is used for removing and attaching these lugs.

5-78. The -2 volt, +4.5 volt, and ground-return circuits for all cards in the card cage are routed through small bus bars which are visible between the backplane connectors when they are viewed from the card side. The -2 volt backplane bus connects to pins 47 and 48 of all cards in the card cage. The +4.5 volt bus connects to pins 39 and 40 of all cards, and the card cage ground bus connects to pins 1, 2, 85, and 86. The card cage buses cannot be reached without major disassembly of the card cage, and if work is required on these buses, the entire computer must be returned to the factory.

5-79. CONNECTION TO LUGS. Crimp-type lugs are used in the power supply section and at the three terminal strips on the card cage. If it becomes necessary to replace one of these, use a solder lug. If a solder lug of the required size is not available, the crimp-type lug may be reused by soldering to it. With either type of lug do not permit solder to run onto the portion of the lug which will be under a screw. (Hold this portion of the lug uppermost when soldering.) Observe the usual precautions for obtaining a good solder connection.

5-80. WIRE BUNDLING. If it becomes necessary to remove the ties which hold a wire bundle together, do not replace the ties with lacing cord. There are wires as small as 26 gauge (American Wire Gauge) in some bundles; lacing cord can sever the conductors in these wires, leaving no external evidence on the wire insulation. For wire bundling, use the following ties, tightened lightly with a pair of pliers:

a. Cable strap (HP part no. 1400-0493), for wire bundles 1/16 inch to 1-1/8 inches diameter.

b. Cable clamp (HP part no. 1400-0482), for wire bundles from 1/4 inch to 3 inches diameter.

5-81. MAINTENANCE TABLES AND DIAGRAMS.

5-82. The tables and illustrations in the remainder of this section contain reference data for troubleshooting and repair. The information consists of a signal index (list of signals and their sources), wiring information, parts location data, component characteristics information, and schematic diagrams.

5-83. ABBREVIATIONS AND MNEMONIC DESIGNATIONS.

5-84. Abbreviations of signal names (commonly referred to as mnemonic designations) are defined in table 5-7, the Signal Index. Other abbreviations used in this section are defined in table 6-18.

5-85. WIRING DATA.

5-86. Table 5-7, the Signal Index, lists all signals that enter or leave cards installed in the card cage. For each signal, a reference number is provided. This number permits the signal to be found in table 5-8, the Backplane Wiring List, which shows connections to other cards in the card cage.

5-87. As well as listing signals transferred between cards, the Signal Index includes signals that do not leave a card. These signals are named in accordance with the flip-flop which is their source. The Signal Index thus can be used to determine the card on which a particular flip-flop is located.

5-88. As noted, the Backplane Wiring List shows connections between cards installed in the card cage. Wiring between the card cage and other units is shown in figure 5-49, the Overall Interconnection Diagram. Wiring for the power supply section is shown in figures 5-32 through 5-44. Wiring to display board assembly A501 and control panel assembly A502 is shown in figures 5-47 and 5-48.

5-89. SCHEMATIC DIAGRAMS.

5-90. Schematic diagrams are included in this section for all electrical assemblies comprising the computer in its basic configuration, with the exception of I/O Control card A201 and I/O address card A202, which are covered in Volume III. The schematic diagrams in this section are arranged according to reference designation of the electrical assembly.

5-91. Next to the schematic diagram for each plug-in card is a Pin Index. This furnishes the reference number for each signal that enters or leaves the card by its 86-pin connector. The reference number permits interconnections to be found in the Backplane Wiring List. If a card has a 48-pin plug in addition to the 86-pin connector, connections to the plug can be found in the door assembly schematic diagram (if the cable from the plug goes to the door assembly), or in the applicable manual (if the cable from the plug goes to an optional device).

5-92. In the upper left corner of each plug-in card schematic is the name of the card, its part number, and a 3-digit number indicating the date code (revision level) of the card. This manual is issued with schematic diagrams for cards installed in computers with serial-number prefix 944-. If the serial-number prefix is different, the applicable schematic diagrams are included in Appendix B (for lower serial-number prefixes), or in updating supplements furnished with this manual (for higher serial-number prefixes).

5-93. When using the schematic diagrams, be sure to read all notes.

5-94. PARTS INFORMATION.

5-95. Parts information is furnished in the form of a Parts Location Diagram and a Reference Designation Index, for each electrical assembly. Parts information is not included for the core stack assembly because it must not be disassembled.

5-96. PARTS LOCATION DIAGRAMS. The Parts Location Diagrams show the appearance and location of the electrical parts on each assembly. The parts are identified by the reference designations used on the schematic diagrams.

5-97. The Parts Location Diagrams apply to computers with serial-number prefix 944-. If different diagrams are required for computers with other prefixes, the diagrams are furnished in Appendix B or in updating supplements.

5-98. On the Parts Location Diagrams for plug-in cards, the card part number appears at the top of the card (e.g.: 02116-6175 for the A1 power fail interrupt card). This number is marked on the card itself. Beneath the part number are a letter and two sets of digits (e.g.: D-821-6 for the A1 power fail interrupt card). These also are marked on the card. The letter identifies the version of the etched circuit on the card. The three digits which follow are the date code. Following the date code are one or two digits which identify the Hewlett-Packard division which manufactured the card.

5-99. REFERENCE DESIGNATION INDEXES. A Reference Designation Index is furnished for each electrical assembly, listing parts in the assembly alphanumerically by reference designation. The index provides the HP part number, principal electrical characteristics, and manufacturer's part number, for each component. Included is a code number identifying the manufacturer. The name and address of the manufacturer corresponding to each code number is furnished in table 6-21.

5-100. The information in Reference Designation Indexes is intended as an aid to troubleshooting. When ordering replacement parts, refer to section VI.

Table 5-7. Signal Index

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
-2V	216	Power Supply	Supply voltage
+4.5V	217	Power Supply	Supply voltage
-5.6V	369	Power Supply	Supply voltage
+7V	218	Power Supply	Supply voltage
+12V	1	Power Supply	Supply voltage
-12V	2	Power Supply	Supply voltage
18 VAC	39	Power Supply	Supply voltage
+22V	3	Power Supply	Supply voltage
-22V	4	Power Supply	Supply voltage
+35.5V	27	Power Supply	Supply voltage
+32V	5	Power Supply	Supply voltage
AAF	38	A108-77	A Addressable flip-flop
ADD	53	A107-3	Add instruction, decoded
ADF	65	A107-75	Add function
ANF	78	A107-56	AND function
AS	399	A109-50	Arithmetic Shift (EAU)
ASG	69	A107-10	Alter-skip group, decoded
BAF	50	A108-80	B addressable flip-flop
C0	37	A108-71	Carry bit 0
C4	136	A105-36	Carry bit 4
C8	154	A104-36	Carry bit 8
C12	171	A103-36	Carry bit 12
C16	188	A102-36	Carry bit 16
CFF	**	A108	Carry flip-flop set output
CF1	**	A106	Clock flip-flop 1 set output
CF2	**	A106	Clock flip-flop 2 set output
CIN	440	A119-41	Character in (DMA)
CL1	**	A106	Clock period 1
CL2	**	A106	Clock period 2
CLC	36	A108-53	Clear control
CLF	32	A108-19	Clear flag
CM1	432	A118-7	Character mode FF, DMA channel 1
CM2	439	A119-68	Character mode FF, DMA channel 2
$\overline{\text{CMF}}$	26	A20-79	"not" Complement function
$\overline{\text{CMFE}}$	63	A107-65	"not" Complement function
CMFB	410	A110-72	Complement function, buffered (EAU)
COUT	430	A119-63	Character out (DMA)
CPR	74	A107-22	Compare instruction, decoded
CR1	444	A119-78	Cycle request, DMA channel 1
CR2	434	A119-71	Cycle request, DMA channel 2
CRS	250	A201-65	Control reset to I/O
CTFF	**	A201	Control flip-flop set output
D1	388	A109-34	Divide operation cycle 1
D2	389	A109-33	Divide operation cycle 2
D3	390	A109-26	Divide operation cycle 3
D4	391	A109-25	Divide operation cycle 4
D5	392	A109-17	Divide operation cycle 5
D5L8	374	A109-27	Divide operation cycle 5, loop 8
D6	393	A109-18	Divide operation cycle 6

NOTE: *Indicates 48-pin connector signal.
**Indicates signal internal to one card.

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
DE-1	455	A118-53	Not used (DMA)
DE-2	456	A118-55	Not used (DMA)
DIN1	435	A119-75	DMA input (direction) FF, channel 1
DIN2	442	A119-74	DMA input (direction) FF, channel 2
DL3	404	A109-57	Double load operation cycle 3 (EAU)
DL4	405	A109-36	Double load operation cycle 4 (EAU)
DM0	413	A116/A117-41	DMA bit 0
DM1	414	A116/A117-46	DMA bit 1
DM2	415	A116/A117-45	DMA bit 2
DM3	416	A116/A117-55	DMA bit 3
DM4	417	A116/A117-65	DMA bit 4
DM5	418	A116/A117-63	DMA bit 5
DM6	419	A116/A117-71	DMA bit 6
DM7	420	A116/A117-72	DMA bit 7
DM8	421	A116/A117-83	DMA bit 8
DM9	422	A116/A117-82	DMA bit 9
DM10	423	A116/A117-6	DMA bit 10
DM11	424	A116/A117-10	DMA bit 11
DM12	425	A116/A117-12	DMA bit 12
DM13	426	A116/A117-16	DMA bit 13
DM14	427	A116/A117-7	DMA bit 14
DMS	365	A101-74	Display memory flip-flop reset output
DMSW	*	S101-4	Display memory switch output
$\overline{\text{DMSW}}$	*	S101-3	"not" Display memory switch output
DS3	371	A109-28	Double store operation cycle 3
DS34	373	A109-6	Double store operation cycles 3 and 4
DS4	372	A109-9	Double store operation cycle 4
EDT	348	A119-42	Not used (DMA)
EFF	**	A108	Extend flip-flop set output
E.IND	34	A108-37	Extend indicator
EIR	112	A106-52	Enable instruction register
ENF	256	A201-67	Enable flag
$\overline{\text{EOF}}$	25	A20-75	"not" Exclusive OR function
$\overline{\text{EOFE}}$	64	A107-67	"not" Exclusive OR function
EOFB	409	A110-26	Exclusive OR function, buffered (EAU)
EPF	481	External Device	Extender power fail
EPH	20	S20-72	Enable phase
EPO	480	External Device	Extender power on
ESR	260	A201-21	Enable service request
EXIT	402	A109-74	Exit MAC operation sequence (EAU)
FBFF	**	Interface Cards	Flag buffer flip-flop set output
FLFF	**	Interface Cards	Flag flip-flop set output
FLG0	251	Interface Cards	Flag from group 0
FLG1	252	Interface Cards	Flag from group 1
FLG2	253	Interface Cards	Flag from group 2
FLG3	254	Interface Cards	Flag from group 3
GATE	403	A109/A110-76	Gate FF (EAU)
GND	219	Power Supply	Ground

NOTE: *Indicates 48-pin connector signal.
**Indicates signal internal to one card.

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
HIN	42	A108-26	Halt instruction, decoded
HIS	347	A118-83	Hold interrupt system (DMA)
HLS	360	S106-4	Halt switch output
$\overline{\text{HLS}}$	359	S106-3	"not" Halt switch output
HLSFF	**	A106	Halt flip-flop set output
IAK	246	A201-77	Interrupt acknowledge
ICFF	**	Interface Cards	Interrupt control flip-flop set output
IDW1	451	A118-16	Input data word from DMA channel 1
IDW2	452	A118-14	Input data word from DMA channel 2
IEN(6)	248	A201-10	Interrupt enable
IEN(10)	249	A201-8	Interrupt enable
IEN(20)	247	A201-7	Interrupt enable
IHC1	453	A118-9	Input high character to DMA channel 1
IHC2	454	A118-8	Input high character to DMA channel 2
IIR	411	A20-71	Inhibit instruction register
ILS	352	S113	Instruction loop switch output
IN	482	A119-52	Not used (DMA)
INT	257	A1-28	Interrupt
IOBI0	312	A101-3	Input/output bus, input bit 0
IOBI1	313	A101-7	Input/output bus, input bit 1
IOBI2	314	A101-11	Input/output bus, input bit 2
IOBI3	315	A101-15	Input/output bus, input bit 3
IOBI4	316	A101-19	Input/output bus, input bit 4
IOBI5	317	A101-23	Input/output bus, input bit 5
IOBI6	318	A101-27	Input/output bus, input bit 6
IOBI7	319	A101-31	Input/output bus, input bit 7
IOBI8	320	A101-35	Input/output bus, input bit 8
IOBI9	321	A101-41	Input/output bus, input bit 9
IOBI10	322	A101-45	Input/output bus, input bit 10
IOBI11	323	A101-51	Input/output bus, input bit 11
IOBI12	324	A101-55	Input/output bus, input bit 12
IOBI13	325	A101-59	Input/output bus, input bit 13
IOBI14	326	A101-63	Input/output bus, input bit 14
IOBI15	327	A101-67	Input/output bus, input bit 15
IOBI16	328	I/O Sect-18	Input/output bus, input bit 16
IOBO0	141	A105-60	Input/output bus, output bit 0
IOBO1	137	A105-50	Input/output bus, output bit 1
IOBO2	131	A105-57	Input/output bus, output bit 2
IOBO3	128	A105-35	Input/output bus, output bit 3
IOBO4	158	A104-60	Input/output bus, output bit 4
IOBO5	155	A104-50	Input/output bus, output bit 5
IOBO6	149	A104-57	Input/output bus, output bit 6
IOBO7	146	A104-35	Input/output bus, output bit 7
IOBO8	176	A103-60	Input/output bus, output bit 8
IOBO9	172	A103-50	Input/output bus, output bit 9
IOBO10	166	A103-57	Input/output bus, output bit 10
IOBO11	163	A103-35	Input/output bus, output bit 11
IOBO12	193	A102-60	Input/output bus, output bit 12
IOBO13	189	A102-50	Input/output bus, output bit 13
IOBO14	183	A102-57	Input/output bus, output bit 14
IOBO15	180	A102-35	Input/output bus, output bit 15
IOBO16	345	– –	Not used

NOTE: *Indicates 48-pin connector signal.
**Indicates signal internal to one card.

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
IOCO	45	A108-34	Input/output control, output
IODO	429	A119-4	I/O data out (DMA)
$\overline{\text{IOF}}$	86	A107-84	"not" Inclusive OR function
IOG	87	A107-6	Input/output instruction group
IOGE	349	A1-59	Input/output instruction group, buffered
IOGE(B)	243	A201-37	Input/output instruction group, (I/O buffered)
IOI	33	A108-44	Input/output, input
IOO	30	A108-13	Input/output, output
IOS	258	A201-6	Input/output switch address
$\overline{\text{IR15}}$	76	A107-42	"not" Instruction register, bit 15
IRQFF	**	Interface Cards	Interrupt request flip-flop set output
IRQ1	277	I/O Sect	Interrupt request 1
IRQ2	278	I/O Sect	Interrupt request 2
IRQ3	279	I/O Sect	Interrupt request 3
IRQ4	280	I/O Sect	Interrupt request 4
IRQ5	281	I/O Sect	Interrupt request 5
IRQ6	282	I/O Sect	Interrupt request 6
IRQ7	283	I/O Sect	Interrupt request 7
IRQ10	284	I/O Sect	Interrupt request 10
IRQ11	285	I/O Sect	Interrupt request 11
IRQ12	286	I/O Sect	Interrupt request 12
IRQ13	287	I/O Sect	Interrupt request 13
IRQ14	288	I/O Sect	Interrupt request 14
IRQ15	289	I/O Sect	Interrupt request 15
IRQ16	290	I/O Sect	Interrupt request 16
IRQ17	291	I/O Sect	Interrupt request 17
ISEFF	**	A201	Interrupt system enable flip-flop set output
ISG	377	A109-63	Inhibit strobe generator (EAU)
ISR	51	A108-84	Input switch register
ISZ	84	A107-76	Increment, skip if zero
JMP	66	A107-79	Jump instruction, decoded
JSB	81	A107-66	Jump subroutine instruction, decoded
LADS	364	A101-70	Load address flip-flop reset output
LADSW	*	S102-4	Load address switch output
$\overline{\text{LADSW}}$	*	S102-3	"not" Load address switch output
LAS	362	A101-62	Load A flip-flop reset output
LASW	*	S104-4	Load A switch output
$\overline{\text{LASW}}$	*	S104-3	"not" Load A switch output
LBS	363	A101-66	Load B flip-flop reset output
LBSW	*	S103-4	Load B switch output
$\overline{\text{LBSW}}$	*	S103-3	"not" Load B switch output
LMS	361	A101-58	Load memory flip-flop reset output
LMSW	*	S105-4	Load memory switch output
$\overline{\text{LMSW}}$	*	S105-3	"not" Load memory switch output
LOD	**	A107	Load instruction, decoded
LPS	367	S110-2	Loader protect switch output
M0	6	A20-6	Memory address bit 0
M1	7	A20-10	Memory address bit 1
M2	8	A20-14	Memory address bit 2
M3	9	A20-18	Memory address bit 3
M4	10	A20-22	Memory address bit 4
M5	11	A20-26	Memory address bit 5

NOTE: *Indicates 48-pin connector signal.
**Indicates signal internal to one card.

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
M6	12	A20-30	Memory address bit 6
M7	13	A20-34	Memory address bit 7
M8	14	A20-38	Memory address bit 8
M9	15	A20-44	Memory address bit 9
M10	16	A20-50	Memory address bit 10
M11	17	A20-54	Memory address bit 11
M12	18	A20-58	Memory address bit 12
M13	19	A20-62	Memory address bit 13
M14	473	A20-66	Memory address bit 14
MAC	54	A107-5	Macro group, decoded (EAU)
MD2	376	A110-16	Multiply/Divide operation cycle 2 (EAU)
MIT	92	A106-25	Memory inhibit time
MMD13	457	A11-84	Memory module decode bit 13 (16K option)
MMD14	474	A222/A221	Memory module decode bit 14 (memory extender)
MMD GND	460	A8-1/10	Memory module decode ground
MNS	351	S111	Memory normal switch output
$\overline{\text{MNS}}$	475	A2-76	"not" Memory normal switch
MP1	383	A109-12	Multiply operation cycle 1 (EAU)
MP2	384	A109-11	Multiply operation cycle 2 (EAU)
MP3	385	A109-4	Multiply operation cycle 3 (EAU)
MP4	386	A109-3	Multiply operation cycle 4 (EAU)
MP5	387	A109-8	Multiply operation cycle 5 (EAU)
MPC	412	A21-25	Memory protect control
MPT0	462	A18-83	Memory protect 4K memory
MPT1	463	A18-81	Memory protect 8K memory
MPT2	464	A6-81	Memory protect 16K memory
MPT3	477	A221-84	Memory protect 24K memory
MPT4	478	A222-21	Memory protect 32K memory
MPT	226	A2-82	Memory protect
$\overline{\text{MPT}}$	476	A2-78	"not" Memory protect
MR0	142	A105-68	Memory register bit 0
MR1	135	A105-18	Memory register bit 1
MR2	132	A105-65	Memory register bit 2
MR3	127	A105-25	Memory register bit 3
MR4	159	A104-68	Memory register bit 4
MR5	153	A104-18	Memory register bit 5
MR6	150	A104-65	Memory register bit 6
MR7	145	A104-25	Memory register bit 7
MR8	177	A103-68	Memory register bit 8
MR9	170	A103-18	Memory register bit 9
MR10	167	A103-65	Memory register bit 10
MR11	162	A103-25	Memory register bit 11
MR12	194	A102-68	Memory register bit 12
MR13	187	A102-18	Memory register bit 13
MR14	184	A102-65	Memory register bit 14
$\overline{\text{MR0}}$	484	A105-63	"not" Memory register bit 0
$\overline{\text{MR1}}$	483	A105-19	"not" Memory register bit 1
$\overline{\text{MR2}}$	486	A105-66	"not" Memory register bit 2
$\overline{\text{MR3}}$	485	A105-24	"not" Memory register bit 3
$\overline{\text{MR4}}$	488	A104-63	"not" Memory register bit 4
$\overline{\text{MR5}}$	487	A104-19	"not" Memory register bit 5
$\overline{\text{MR6}}$	490	A104-66	"not" Memory register bit 6
$\overline{\text{MR7}}$	489	A104-24	"not" Memory register bit 7
$\overline{\text{MR8}}$	492	A103-63	"not" Memory register bit 8
$\overline{\text{MR9}}$	491	A103-19	"not" Memory register bit 9
$\overline{\text{MR10}}$	494	A103-66	"not" Memory register bit 10

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
$\overline{\text{MR11}}$	493	A103-24	"not" Memory register bit 11
$\overline{\text{MR12}}$	495	A102-63	"not" Memory register bit 12
MRT	94	A106-29	Memory read time
MST	111	A106-32	Memory strobe time
MTE	**	A106	Memory timing enable
MWL	123	A106-33	Memory write level
MWT	124	A106-35	Memory write time
OASL	380	A110-31	Overflow due to arithmetic shift left (EAU)
OHC1	447	A118-10	Output high character from DMA channel 1
OHC2	448	A118-12	Output high character from DMA channel 2
OLC1	449	A118-19	Output low character from DMA channel 1
OLC2	450	A118-13	Output low character from DMA channel 2
OPO	**	A107	One phase operation
$\overline{\text{OPO}}$	71	A107-16	"not" One phase operation
OUT	431	A119-65	Output high character (DMA)
OVD	378	A110-56	Overflow due to divide operation (EAU)
OVFF	**	A108	Overflow flip-flop set output
OVF	29	A108-9	Overflow indicator
OVR	396	A110-35	Overflow register (EAU)
$\overline{\text{OVR}}$	397	A110-64	"not" Overflow register (EAU)
P123	91	A106-23	Phase 1, phase 2, or phase 3
P123G	21	A20-65	Phase 1, phase 2, or phase 3 with phase 5
PEH	214	A3-62	Parity error halt
PEI	215	A3-61	Parity error indicator
PH1FF	**	A106	Phase 1 flip-flop set output
PH1	98	A106-41	Phase 1, fetch
PH2FF	**	A106	Phase 2 flip-flop set output
PH2	98	A106-37	Phase 2, indirect
PH3FF	**	A106	Phase 3 flip-flop set output
PH3	115	A106-60	Phase 3, execute
PH4FF	**	A106	Phase 4 flip-flop set output
PH4	88	A106-13	Phase 4, interrupt
PH5	428	A119-8	Phase 5 (DMA)
$\overline{\text{PH5}}$	259	A201-9	"not" Phase 5
PIND	368	A1-49	Power indicator lamp
PNS	350	S112	Phase normal switch
POFP	354	A1-56	Power on/off pulse
PON	353	A1-58	Power on normal
POPIO	102	A106-61	Power on pulse to I/O
POPIO(B)	311	A201-72	Power on pulse to I/O (buffered)
PRESET LAMP	479	A1-35	Preset lamp indicator
PRH6	468	A119-31	Priority high select code 6 (DMA)
PRH5/4	309	A1-3	Priority high select code 5/priority low select code 4
PRH6/5	310	A3-27	Priority high select code 6/priority low select code 5
PRH10	292	A119-9	Priority high select code 10
PRH11/10	293	A203-3	Priority high select code 11/priority low select code 10
PRH12/11	294	A204-3	Priority high select code 12/priority low select code 11
PRH13/12	295	A205-3	Priority high select code 13/priority low select code 12
PRH14/13	296	A206-3	Priority high select code 14/priority low select code 13
PRH15/14	297	A207-3	Priority high select code 15/priority low select code 14
PRH16/15	298	A208-3	Priority high select code 16/priority low select code 15

NOTE: *Indicates 48-pin connector signal.
**Indicates signal internal to one card.

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
PRH17/16	299	A209-3	Priority high select code 17/priority low select code 16
PRH20/17	300	A210-3	Priority high select code 20/priority low select code 17
PRH21/20	301	A211-3	Priority high select code 21/priority low select code 20
PRH22/21	302	A212-3	Priority high select code 22/priority low select code 21
PRH23/22	303	A213-3	Priority high select code 23/priority low select code 22
PRH24/23	304	A214-3	Priority high select code 24/priority low select code 23
PRH25/24	305	A215-3	Priority high select code 25/priority low select code 24
PRH26/25	306	A216-3	Priority high select code 26/priority low select code 25
PRH27/26	307	A217-3	Priority high select code 27/priority low select code 26
PRH30/27	308	A218-3	Priority high select code 30/priority low select code 27
PRSFF	**	A106	Preset flip-flop set output
PRS	355	A101-30	Preset switch gated
PRSW	*	S108-4	Preset switch output
$\overline{\text{PRSW}}$	356	S108-3	"not" Preset switch output
PSO	461	A1-51	Power supply on
RARB	57	A107-19	Read A register to the R bus
RB0	61	A107-61	R bus, bit 0
RB14	197	A102-71	R bus, bit 14
RB15	196	A102-30	R bus, bit 15
RBRB	72	A107-18	Read B register to the R bus
RF1	**	A106	Run 1 flip-flop set output
$\overline{\text{RF2}}$	114	A106-58	"not" Run 2 flip-flop
$\overline{\text{RL4}}$	43	A108-28	"not" Rotate left 4 bits
$\overline{\text{RLL}}$	47	A108-42	"not" Rotate left to least significant bit
RMSB	82	A107-68	Read M register to the S bus
RNS	358	A101-44	RNS flip-flop reset output
RNSW	*	S107-4	Run switch output
$\overline{\text{RNSW}}$	*	S107-3	"not" Run switch output
RO	398	A109-46	Rotate (EAU)
ROT5	379	A109-82	Rotate at T5 (EAU)
RPB	93	A106-27	Reset parity bit
RPE	– –	A106-74	Reset parity error (not used)
RPRB	83	A107-72	Read P register to the R bus
$\overline{\text{RRS}}$	35	A108-41	"not" Rotate right to sign bit
RSDS	381	A21-15	Reset, double store operation
RSM(6-9)	70	A107-12	Reset M register bits 6 thru 9
RSM(10-15)	56	A107-11	Reset M register bits 10 thru 15
RSET	370	A109-42	Reset CARX flip-flop (EAU)
RST	79	A107-58	Reset T register
RT	400	A109-52	Right shift or rotate
$\overline{\text{RT}}$	401	A109-58	"not" Right shift or rotate
RTSB	85	A107-82	Read T register to the S bus
RUN	465	A202-32	Run signal
S1FF	**	A106	Step 1 flip-flop set output
S2FF	**	A106	Step 2 flip-flop set output
SB0	67	A107-81	S bus, bit 0
SB15	195	A102-6	S bus, bit 15
SCL(0)	261	A202-65	Select code least significant digit, octal 0
SCL(1)	262	A202-67	Select code least significant digit, octal 1
SCL(2)	263	A202-61	Select code least significant digit, octal 2
SCL(3)	264	A202-63	Select code least significant digit, octal 3

NOTE: *Indicates 48-pin connector signal.
**Indicates signal internal to one card.

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
SCL(4)	265	A202-51	Select code least significant digit, octal 4
SCL(5)	266	A202-52	Select code least significant digit, octal 5
SCL(6)	267	A202-49	Select code least significant digit, octal 6
SCL(7)	268	A202-50	Select code least significant digit, octal 7
SCM(0)	269	A202-75	Select code most significant digit, octal 0
SCM(1)	270	A202-77	Select code most significant digit, octal 1
SCM(2)	271	A202-71	Select code most significant digit, octal 2
SCM(3)	272	A202-73	Select code most significant digit, octal 3
SCM(4)	273	A202-56	Select code most significant digit, octal 4
SCM(5)	274	A202-57	Select code most significant digit, octal 5
SCM(6)	275	A202-54	Select code most significant digit, octal 6
SCM(7)	276	A202-55	Select code most significant digit, octal 7
SCS	366	A101-78	Single cycle flip-flop reset output
SCSW	*	S100-4	Single cycle switch output
$\overline{\text{SCSW}}$	*	S100-3	"not" Single cycle switch output
SEO	118	A106-72	Switch exclusive OR
SFC	41	A108-14	Skip if flag clear, decoded
SFS	48	A108-54	Skip if flag set, decoded
SIR	245	A201-35	Service interrupt request
SKF	255	A201-73	Skip on flag signal
$\overline{\text{SL14}}$	23	A20-74	"not" Shift left, bit 14
$\overline{\text{SL14E}}$	46	A108-38	"not" Shift left, bit 14
SL14B	408	A109-49	Shift left bit 14, buffered (EAU)
$\overline{\text{SLM}}$	22	A20-77	"not" Shift left magnitude
$\overline{\text{SLME}}$	40	A108-8	"not" Shift left magnitude
SLMB	406	A109-44	Shift left magnitude, buffered (EAU)
SMAR1	441	A119-72	Step memory address register, DMA channel 1
SMAR2	433	A119-69	Step memory address register, DMA channel 2
SPAR	466	A220-84	Spare line from I/O extender option
SRA0-77	– –	A202	Service request address 0-77
SRCS	375	A109-31	Shift rotate count started (EAU)
SRE	31	A3-35	Not used (parity error)
SRG	75	A107-38	Shift rotate group, decoded
$\overline{\text{SRM}}$	24	A20-78	"not" Shift right magnitude
$\overline{\text{SRME}}$	44	A108-32	"not" Shift right magnitude
SRMB	407	A109-41	Shift right magnitude, buffered (EAU)
SRQ10	329	A203-19	Service request from select code 10
SRQ11	330	A204-19	Service request from select code 11
SRQ12	331	A205-19	Service request from select code 12
SRQ13	332	A206-19	Service request from select code 13
SRQ14	333	A207-19	Service request from select code 14
SRQ15	334	A208-19	Service request from select code 15
SRQ16	335	A209-19	Service request from select code 16
SRQ17	336	A210-19	Service request from select code 17
SRQ20	337	A211-19	Service request from select code 20
SRQ21	338	A212-19	Service request from select code 21
SRQ22	339	A213-19	Service request from select code 22
SRQ23	340	A214-19	Service request from select code 23
SRQ24	341	A215-19	Service request from select code 24
SRQ25	342	A216-19	Service request from select code 25
SRQ26	343	A217-19	Service request from select code 26
SRQ27	344	A218-19	Service request from select code 27
ST0	227	A12-3, A13-3	Set T register bit 0

NOTE: *Indicates 48-pin connector signal.
**Indicates signal internal to one card.

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
ST1	228	A12-7,A13-7	Set T register bit 1
ST2	229	A12-11,A13-11	Set T register bit 2
ST3	230	A12-15,A13-15	Set T register bit 3
ST4	231	A12-19,A13-19	Set T register bit 4
ST5	232	A12-23,A13-23	Set T register bit 5
ST6	233	A12-27,A13-27	Set T register bit 6
ST7	234	A12-31,A13-31	Set T register bit 7
ST8	235	A12-35,A13-35	Set T register bit 8
ST9	236	A12-51,A13-51	Set T register bit 9
ST10	237	A12-55,A13-55	Set T register bit 10
ST11	238	A12-59,A13-59	Set T register bit 11
ST12	239	A12-63,A13-63	Set T register bit 12
ST13	240	A12-67,A13-67	Set T register bit 13
ST14	241	A12-71,A13-71	Set T register bit 14
ST15	242	A12-75,A13-75	Set T register bit 15
ST16	459	A12-79,A13-79	Set T register bit 16
STBA	77	A107-50	Store T bus in A register
STBB	60	A107-51	Store T bus in B register
STBT	62	A107-63	Store T bus in T register
STC	49	A108-56	Set control
STF	28	A108-5	Set flag
STM(0-5)	73	A107-20	Store T bus bits 0 thru 5 in M register
STM(6-9)	58	A107-21	Store T bus bits 6 thru 9 in M register
STM(10-11)	59	A107-27	Store T bus bits 10 thru 11 in M register
STM(12-15)	96	A107-28	Store T bus bits 12 thru 15 in M register
STP(0-9)	55	A107-7	Store T bus bits 0 thru 9 in P register
STP(10-11)	52	A107-74	Store T bus bits 10 thru 11 in P register
STP(12-15)	68	A107-8	Store T bus bits 12 thru 15 in P register
STR	80	A107-64	Store instruction, decoded
SWCR1	445	A119-80	Step word count register, DMA channel 1
SWCR2	437	A119-79	Step word count register, DMA channel 2
SWR0 thru SWR15	*	S0 thru S15	Switch register bits 0 thru 15
SWSA	120	A106-84	Switch store in A register
SWSB	105	A106-71	Switch store in B register
SWSM	106	A106-73	Switch store in M register
SWSP	117	A106-64	Switch store in P register
SWST	116	A106-62	Switch store in T register
T0	109	A106-28	Time period 0
T1	100	A106-53	Time period 1
T2	119	A106-76	Time period 2
T3	103	A106-63	Time period 3
T3(B)	244	A201-81	Time period 3 (buffered)
T4	113	A106-54	Time period 4
T5	104	A106-69	Time period 5
T6	122	A106-11	Time period 6
T7	108	A106-18	Time period 7
T7S	99	A106-51	Time period 7 with strobe
T0T1	121	A106-17	Time periods 0 and 1
T1T2	90	A106-21	Time periods 1 and 2
T2T3	382	A110-21	Times 2 and 3 (EAU)
T3T4	89	A106-15	Time periods 3 and 4

NOTE: *Indicates 48-pin connector signal.
**Indicates signal internal to one card.

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
T4T5	107	A106-16	Time periods 4 and 5
T6T7	110	A106-30	Time periods 6 and 7
TAN1	129	A105-43	T bus bits 0 thru 3 "anded"
TAN2	147	A104-43	T bus bits 4 thru 7 "anded"
TAN3	164	A103-43	T bus bits 8 thru 11 "anded"
TAN4	181	A102-43	T bus bits 12 thru 15 "anded"
TB0	198	A105-69	T bus bit 0
TB1	199	A105-13	T bus bit 1
TB2	200	A105-55	T bus bit 2
TB3	201	A105-17	T bus bit 3
TB4	202	A104-69	T bus bit 4
TB5	203	A104-13	T bus bit 5
TB6	204	A104-55	T bus bit 6
TB7	205	A104-17	T bus bit 7
TB8	206	A103-69	T bus bit 8
TB9	207	A103-13	T bus bit 9
TB10	208	A103-55	T bus bit 10
TB11	209	A103-17	T bus bit 11
TB12	210	A102-69	T bus bit 12
TB13	211	A102-13	T bus bit 13
TB14	212	A102-55	T bus bit 14
TB15	213	A102-17	T bus bit 15
TE1	438	A119-66	Transfer enable FF, DMA channel 1
TE2	446	A119-62	Transfer enable FF, DMA channel 2
TEV	395	A109-56	Time bits, even numbered (EAU)
THERM SW	467	A2-81	Thermal switch output
TOD	394	A109-45	Time bits, odd numbered (EAU)
TR0	140	A105-58	T register bit 0
TR1	125	A105-9	T register bit 1
TR2	139	A105-56	T register bit 2
TR3	134	A105-16	T register bit 3
TR4	157	A104-58	T register bit 4
TR5	143	A104-9	T register bit 5
TR6	95	A104-56	T register bit 6
TR7	152	A104-16	T register bit 7
TR8	175	A103-58	T register bit 8
TR9	160	A103-9	T register bit 9
TR10	174	A103-56	T register bit 10
TR11	169	A103-16	T register bit 11
TR12	192	A102-58	T register bit 12
TR13	178	A102-9	T register bit 13
TR14	191	A102-56	T register bit 14
TR15	186	A102-16	T register bit 15
$\overline{TR0}$	138	A105-54	"not" T register bit 0
$\overline{TR1}$	133	A105-10	"not" T register bit 1
$\overline{TR2}$	130	A105-53	"not" T register bit 2
$\overline{TR3}$	126	A105-15	"not" T register bit 3
$\overline{TR4}$	156	A104-54	"not" T register bit 4
$\overline{TR5}$	151	A104-10	"not" T register bit 5
$\overline{TR6}$	148	A104-53	"not" T register bit 6
$\overline{TR7}$	144	A104-15	"not" T register bit 7
$\overline{TR8}$	173	A103-54	"not" T register bit 8
$\overline{TR9}$	168	A103-10	"not" T register bit 9
$\overline{TR10}$	165	A103-53	"not" T register bit 10
$\overline{TR11}$	161	A103-15	"not" T register bit 11
$\overline{TR12}$	190	A102-54	"not" T register bit 12

Table 5-7. Signal Index (Continued)

SIGNAL MNEMONIC	REF NO.	SOURCE	DEFINITION
$\overline{TR13}$	185	A102-10	"not" T register bit 13
$\overline{TR14}$	182	A102-53	"not" T register bit 14
$\overline{TR15}$	179	A102-15	"not" T register bit 15
$\overline{TR16}$	458	A3-53	"not" T register bit 16
TR0(B)	496	A120-4/A108-4	T register bit 0 from DMA/shift logic
TR1(B)	497	A120-6	T register bit 1 from DMA
TR2(B)	498	A120-8/A108-15	T register bit 2 from DMA/shift logic
TR3(B)	499	A120-10	T register bit 3 from DMA
TR4(B)	500	A120-12	T register bit 4 from DMA
TR5(B)	501	A120-14	T register bit 5 from DMA
TR6(B)	502	A120-16	T register bit 6 from DMA
TR7(B)	503	A120-18	T register bit 7 from DMA
TR8(B)	504	A120-33	T register bit 8 from DMA
TR9(B)	505	A120-37	T register bit 9 from DMA
TR10(B)	506	A120-44	T register bit 10 from DMA
TR11(B)	507	A120-49	T register bit 11 from DMA
TR12(B)	508	A120-59	T register bit 12 from DMA
TR13(B)	509	A120-63	T register bit 13 from DMA
TR14(B)	510	A120-67	T register bit 14 from DMA
TR15(B)	511	A120-69	T register bit 15 from DMA
TS	101	A106-55	Time strobe
TSA	469	A106-67	Time strobe A
TTK	470	A222-84	32K Memory option attached
WCR1	436	A119-77	Word count rollover, DMA channel 1
WCR2	443	A119-76	Word count rollover, DMA channel 2
X0	220	A2-4	X axis drive, addresses 00000-07777
X1	221	A2-6	X axis drive, addresses 10000-17777
X2	222	A2-8	X axis drive, addresses 20000-27777
X3	223	A2-12	X axis drive, addresses 30000-37777
Y0/1	224	A2-5	Y axis drive, addresses 00000-17777
Y2/3	225	A2-10	Y axis drive, addresses 20000-37777

Table 5-8. Backplane Wiring List

MEMORY

				MEMORY PROTECT	DIRECT MEMORY LOGIC		INHIBIT DRIVER 0		INHIBIT DRIVER 1	"X" DRIVER/SWITCH 0-1	"Y" DRIVER/SWITCH 0-1	SENSE AMPLIFIER 0	SENSE AMPLIFIER 1	SENSE AMPLIFIER 2	SENSE AMPLIFIER 3	"X" DRIVER/SWITCH 2-3	"Y" DRIVER/SWITCH 2-3		INHIBIT DRIVER 2		INHIBIT DRIVER 3	PARITY ERROR	MEMORY MODULE DECODER	POWER FAIL
REF	SIGNAL	SOURCE	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	+12V	PS										43/44	←	→	43/44									43/44
2	-12V	↑										69/70	←	→	69/70									69/70
	-12V											65/66	65/66	65/66	65/66									
3	+22V									43/44	43/44					43/44	43/44							31
4	-22V	↓								33/34	33/34					33/34	33/34							33
5	+32V	PS					43/44		43/44										43/44		43/44			29
6	M0	A20			6					60						60								
7	M1	↑			10					64						64								
8	M2				14					38						38								
9	M3				18					84						84								
10	M4				22					82						82								
11	M5				26					78						78								
12	M6				30						60						60						55	
13	M7				34						64						64						54	
14	M8				38						38						38						53	
15	M9				44						84						84						52	
16	M10				50						82						82						51	
17	M11				54						78						78						50	
18	M12				58																		3	
19	M13				62									83										
20	EPH				72																			
21	P123G				65																			
22	$\overline{\text{SLM}}$				77																			
	$\overline{\text{SLM}}$																							
23	$\overline{\text{SL14}}$				74																			
24	$\overline{\text{SRM}}$				78																			
	$\overline{\text{SRM}}$																							
25	$\overline{\text{EOF}}$	↓			75																			
26	$\overline{\text{CMF}}$	A20			79																			
27	+35.5V	PS																						
28	STF	A108																				18		
29	OVF. IND.	A108																						
30	IOO	A108		57																				
31	SRE	A3																				35		
32	CLF	A108																				51		7
33	IOI	↑		59																		15		
34	E. IND.																							
35	$\overline{\text{RRS}}$																							
36	CLC																							21
37	CO																							
38	AAF			17																		49		
39	18 VAC																							79/80
40	$\overline{\text{SLME}}$				70																			
41	SFC																							5
42	HIN			55																		69		
43	$\overline{\text{RL4}}$																							
44	$\overline{\text{SRME}}$				76																			
45	IOCO																							
46	$\overline{\text{SL 14E}}$				67																			
47	$\overline{\text{RLL}}$																							
48	SFS																							
49	STC			41																				22
50	BAF	↓		13																		50		
51	ISR	A108																						
52	STP (10-11)	A107																						
53	ADD	↑																						
54	MAC																							
55	STP (0-9)	↓																						
56	RSM (10-15)	A107																						

LOGIC

				DMA PACKER	DMA CONTROL	DMA ENCODER	DMA REGISTER 1	DMA REGISTER 2 OR DMI						EAU LOGIC	EAU TIMING	SHIFT LOGIC	INSTRUCTION DECODER	TIMING GENERATOR	ARITHMETIC LOGIC 0-3	ARITHMETIC LOGIC 4-7	ARITHMETIC LOGIC 8-11	ARITHMETIC LOGIC 12-15	FRONT PANEL COUPLER
REF	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101
1	+12V																						
2	-12V																						
	-12V																						
3	+22V																						
4	-22V																						
5	+32V																						
6	M0																						
7	M1																						
8	M2																						
9	M3																						
10	M4																						
11	M5																						
12	M6																						
13	M7																						
14	M8																						
15	M9																						
16	M10																						
17	M11																						
18	M12																						
19	M13																						
20	EPH																	14					
21	P123G															69							
22	$\overline{\text{SLM}}$																		41/82	41/82	41/82		
	$\overline{\text{SLM}}$																		80	80	80	80	
23	$\overline{\text{SL14}}$																					82	
24	$\overline{\text{SRM}}$																			83	83	83	
	$\overline{\text{SRM}}$																		74	74	74	74	
25	$\overline{\text{EOF}}$																		76	76	76	76	
26	$\overline{\text{CMF}}$																		64	64	64	64	
27	+35.5V																						
28	STF				16										15	5							
29	OVF. IND.															9							4
30	IOO				56	30	8	8								13							
31	SRE																						
32	CLF				14			51							24	19							
33	IOI				84/81	43/11	22	22								44			31	31	31	31	
34	E. IND.															37							83
35	$\overline{\text{RRS}}$															41			83				
36	CLC				60		18	18								53							
37	CO							43								71			67				
38	AAF															77	49	75					
39	18 VAC																						
40	$\overline{\text{SLME}}$															8							
41	SFC				24											14							
42	HIN															26		66					
43	$\overline{\text{RL4}}$															28			78	78	78	78	
44	$\overline{\text{SRME}}$															32							
45	IOCO															34			70	70	70	70	
46	$\overline{\text{SL 14E}}$															38							
47	$\overline{\text{RLL}}$															42						41	
48	SFS				20			31								54							
49	STC				58	17	20	20								56							
50	BAF															80	13	83					
51	ISR															84							6
52	STP (10-11)																74				44		
53	ADD															29	3						
54	MAC														62		5						
55	STP (0-9)																7		23/44	23/44	23		
56	RSM (10-15)																11				21	14/21	

INPUT/OUTPUT

		MEMORY EXTENDER X2	MEMORY EXTENDER X1	I/O EXTENDER X2	I/O EXTENDER X1	27	26	25	24	23	22	21	20	17	16	15	14	13	12	11	10	I/O ADDRESS ENCODER	I/O CONTROL
REF	SIGNAL	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201
1	+12V	43/44										← COPPER BUS →											43/44
2	-12V	69/70										← COPPER BUS →											69/70
	-12V																						
3	+22V																						
4	-22V																						
5	+32V																						
6	M0		24																				
7	M1		25																				
8	M2		28																				
9	M3		38																				
10	M4		50																				
11	M5		53																				
12	M6	24																					
13	M7	25																					
14	M8	28																					
15	M9	38																					
16	M10	50																					
17	M11	53																					
18	M12	56/65	26/62																				
19	M13																						
20	EPH																						
21	P123G																						
22	$\overline{\text{SLM}}$																						
	$\overline{\text{SLM}}$																						
23	$\overline{\text{SL14}}$																						
24	$\overline{\text{SRM}}$																						
	$\overline{\text{SRM}}$																						
25	$\overline{\text{EOF}}$																						
26	$\overline{\text{CMF}}$																						
27	+35.5V	36 ←																			→ 36		
28	STF			9 ←																	→ 9		41
29	OVF. IND.																						
30	IOO			20 ←																	→ 20		
31	SRE																						
32	CLF			7 ←																	→ 7		51
33	IOI			24 ←																		→ 24	
34	E. IND.																						
35	$\overline{\text{RRS}}$																						
36	CLC			21 ←																	→ 21		75
37	CO																						
38	AAF																						
39	18 VAC																						
40	$\overline{\text{SLME}}$																						
41	SFC			5 ←																	→ 5		71
42	HIN																						
43	$\overline{\text{RL4}}$																						
44	$\overline{\text{SRME}}$																						
45	IOCO																						
46	$\overline{\text{SL 14E}}$																						
47	$\overline{\text{RLL}}$																						
48	SFS			25 ←																	→ 25		68
49	STC				22 ←																→ 22		61
50	BAF																						
51	ISR																						
52	STP (10-11)																						
53	ADD																						
54	MAC																						
55	STP (0-9)																						
56	RSM (10-15)																						

Table 5-8. Backplane Wiring List (Continued)

MEMORY

REF	SIGNAL	SOURCE	22	MEMORY PROTECT 21	DIRECT MEMORY LOGIC 20	19	INHIBIT DRIVER 0 18	17	INHIBIT DRIVER 1 16	"X" DRIVER/SWITCH 0-1 15	"Y" DRIVER/SWITCH 0-1 14	SENSE AMPLIFIER 0 13	SENSE AMPLIFIER 1 12	SENSE AMPLIFIER 2 11	SENSE AMPLIFIER 3 10	"X" DRIVER/SWITCH 2-3 9	"Y" DRIVER/SWITCH 2-3 8	7	INHIBIT DRIVER 2 6	5	INHIBIT DRIVER 3 4	PARITY ERROR 3	MEMORY MODULE DECODER 2	POWER FAIL 1
57	RARB	A107																						
58	STM (6-9)																							
59	STM (10-11)																							
60	STBB																							
61	RB0																							
62	STBT																							
63	$\overline{CMFE}$				81																			
64	$\overline{EOFE}$				83																			
65	ADF																							
66	JMP			11																				
67	SB0																							
68	STP (12-15)																							
69	ASG																							
70	RSM 6-9																							
71	$\overline{OPO}$																							
72	RBRB																							
73	STM (0-5)																							
74	CPR																							
75	SRG																							
76	$\overline{IR15}$			33																				4
77	STBA																							
78	ANF																							
79	RST																							
80	STR																							
81	JSB																							
82	RMSB																							
83	$\overline{RPRB}$																							
84	ISZ																					44		
85	RTSB																							
86	$\overline{IOF}$																							
87	IOG	A107		16																		59		38
88	PH4	A106																						
89	T3T4																							
90	T1T2																							
91	P123			63	68																	52		
92	MIT						54		54	30	30					30	30		54		54			
93	RPB																					46		
94	MRT	A106								18	18					18	18							
95	TR6	A104																				58		
96	STM (12-15)	A107																						
97	PH2	A106		49																				
98	PH1			21																				
99	T7S																							
100	T1			24																				
101	TS																							
102	POPIO																					45		
103	T3			23																		23		
104	T5																							
105	SWSB																							
106	SWSM																							
107	T4T5																							
108	T7			61																		26		
109	T0																							
110	T6T7																							
111	MST											41	41	41	41									
112	EIR																							
113	T4	A106																						

LOGIC

REF	SIGNAL	122	121	DMA PACKER 120	DMA CONTROL 119	DMA ENCODER 118	DMA REGISTER 1 117	DMA REGISTER 2 OR DMI 116	115	114	113	112	111	EAU LOGIC 110	EAU TIMING 109	SHIFT LOGIC 108	INSTRUCTION DECODER 107	TIMING GENERATOR 106	ARITHMETIC LOGIC 0-3 105	ARITHMETIC LOGIC 4-7 104	ARITHMETIC LOGIC 8-11 103	ARITHMETIC LOGIC 12-15 102	FRONT PANEL COUPLER 101
57	RARB													65			19		34	34	34	34	
58	STM (6-9)																21			22	29		
59	STM (10-11)																27				22		
60	STBB																51		26	26	26	26	
61	RB0													43		52	61		37				
62	STBT																63		51	51	51	51	
63	$\overline{CMFE}$																65						
64	$\overline{EOFE}$																67						
65	ADF				82									12			75		5	5	5	5	
66	JMP																79	34					
67	SB0													44			81		42				
68	STP (12-15)																8					23/44	
69	ASG															82	10						
70	RSM 6-9																12			21	14		
71	$\overline{OPO}$																16	42					
72	RBRB													58			18		28	28	28	28	
73	STM (0-5)																20		22/29	29			
74	CPR															63	22						
75	SRG															49	38						
76	$\overline{IR15}$																42	49					
77	STBA																50		38	38	38	38	
78	ANF																56		72	72	72	72	
79	RST																58		7	7	7	7	
80	STR																64	81					
81	JSB																66	82					
82	RMSB													34			68		8	8	8	8	
83	$\overline{RPRB}$													4			72		12	12	12	12	
84	ISZ							69								61	76	24					
85	RTSB							60						19			82		20	20	20	20	
86	$\overline{IOF}$																84		73	73	73	73	
87	IOG																6						
88	PH4																83	13					
89	T3T4				30									74		7	70	15					
90	T1T2													51			52	21					
91	P123														13		78	23					
92	MIT																	25					
93	RPB																	27					
94	MRT																	29					
95	TR6			15											66	3				56			
96	STM (12-15)																28					22/29	
97	PH2																53	37					
98	PH1														81		44	41					
99	T7S				10										23			51					
100	T1													13	71		62	53					
101	TS															74	45	55					
102	POPIO							37										61					
103	T3													32	75	45	43	63					
104	T5													54	67	46	36	69					
105	SWSB													10			24	71					
106	SWSM													33			26	73					
107	T4T5				6	31								23		21	54	16					
108	T7				64			57						28	73	83	32	18					
109	T0							54						15	51	68	46	28					
110	T6T7					73								11	14	72	69	30					
111	MST																	32					
112	EIR																4	52					
113	T4													24	55	65	31	54					

INPUT/OUTPUT

REF	SIGNAL	MEMORY EXTENDER X2 222	MEMORY EXTENDER X1 221	I/O EXTENDER X2 220	I/O EXTENDER X1 219	27 218	26 217	25 216	24 215	23 214	22 213	21 212	20 211	17 210	16 209	15 208	14 207	13 206	12 205	11 204	10 203	I/O ADDRESS ENCODER 202	I/O CONTROL 201
57	RARB																						
58	STM (6-9)																						
59	STM (10-11)																						
60	STBB																						
61	RB0																						
62	STBT																						
63	$\overline{CMFE}$																						
64	$\overline{EOFE}$																						
65	ADF																						
66	JMP																						
67	SB0																						
68	STP (12-15)																						
69	ASG																						
70	RSM 6-9																					11	
71	$\overline{OPO}$																						
72	RBRB																						
73	STM (0-5)																						
74	CPR																						
75	SRG																						
76	$\overline{IR15}$																						
77	STBA																						
78	ANF																						
79	RST																						
80	STR																						
81	JSB																						
82	RMSB																						
83	$\overline{RPRB}$																						
84	ISZ																						
85	RTSB																						
86	$\overline{IOF}$																						
87	IOG																						
88	PH4																						53
89	T3T4																						
90	T1T2																						
91	P123																						
92	MIT		58																				
93	RPB																						
94	MRT	58																					
95	TR6																						
96	STM (12-15)																						79
97	PH2																						
98	PH1																						29
99	T7S																						
100	T1																						23
101	TS																						27
102	POPIO																						63
103	T3																						3
104	T5																						45
105	SWSB																						
106	SWSM																						
107	T4T5																						
108	T7																						
109	T0																						31
110	T6T7																						
111	MST		22																				
112	EIR																						
113	T4																						

Table 5-8. Backplane Wiring List (Continued)

MEMORY

REF	SIGNAL	SOURCE	22	21 MEMORY PROTECT	20 DIRECT MEMORY LOGIC	19	18 INHIBIT DRIVER 0	17	16 INHIBIT DRIVER 1	15 "X" DRIVER/ SWITCH 0-1	14 "Y" DRIVER/ SWITCH 0-1	13 SENSE AMPLIFIER 0	12 SENSE AMPLIFIER 1	11 SENSE AMPLIFIER 2	10 SENSE AMPLIFIER 3	9 "X" DRIVER/ SWITCH 2-3	8 "Y" DRIVER/ SWITCH 2-3	7	6 INHIBIT DRIVER 2	5	4 INHIBIT DRIVER 3	3 PARITY ERROR	2 MEMORY MODULE DECODER	1 POWER FAIL
114	$\overline{\text{RF2}}$	A106																						62
115	PH3																					43		
116	SWST																							
117	SWSP																							
118	SEO																							
119	T2																							
120	SWSA																							
121	T0T1																							
122	T6																							
123	MWL			34																		54		
124	MWT	A106								12	12					12	12							
125	TR1	A105																				83		
126	$\overline{\text{TR3}}$						8		8										8		8	73		
127	MR3			18	16																			
128	IOBO3			3																				
129	TAN1																							
130	$\overline{\text{TR2}}$						14		14										14		14	74		
131	IOBO2			4																				
132	MR2			8	12																			
133	$\overline{\text{TR1}}$						4		4										4		4	81		
134	TR3																					75		
135	MR1			10	8																			
136	C4																							
137	IOBO1			5																				
138	$\overline{\text{TR0}}$						6		6										6		6	82		
139	TR2																					76		
140	TR0																					84		
141	IOBO0			6																				
142	MR0	A105		14	4																			
143	TR5	A104																				67		
144	$\overline{\text{TR7}}$						20		20										20		20	55		
145	MR7			32	32																			
146	IOBO7			20																				
147	TAN2																							
148	$\overline{\text{TR6}}$						28		28										28		28	56		
149	IOBO6			22																				
150	MR6			37	28																			
151	$\overline{\text{TR5}}$						12		12										12		12	65		
152	TR7																					57		
153	MR5			42	24																			
154	C8																							
155	IOBO5			28																				
156	$\overline{\text{TR4}}$						22		22										22		22	66		
157	TR4																					68		
158	IOBO4			26																				
159	MR4	A104		30	20																			
160	TR9	A103																				31		
161	$\overline{\text{TR11}}$						68		68										68		68	19		
162	MR11			60	52																			
163	IOBO11			52																				
164	TAN3																							
165	$\overline{\text{TR10}}$						58		58										58		58	20		
166	IOBO10			50																				
167	MR10			58	46																			
168	$\overline{\text{TR9}}$						60		60										60		60	29		
169	TR11	A103																				21		

LOGIC

REF	SIGNAL	122	121	120 DMA PACKER	119 DMA CONTROL	118 DMA ENCODER	117 DMA REGISTER 1	116 DMA REGISTER 2 OR DMI	115	114	113	112	111	110 EAU LOGIC	109 EAU TIMING	108 SHIFT LOGIC	107 INSTRUCTION DECODER	106 TIMING GENERATOR	105 ARITHMETIC LOGIC 0-3	104 ARITHMETIC LOGIC 4-7	103 ARITHMETIC LOGIC 8-11	102 ARITHMETIC LOGIC 12-15	101 FRONT PANEL COUPLER
114	$\overline{\text{RF2}}$														54			58					14
115	PH3							67								62	60	60					
116	SWST				83									20			34	62					
117	SWSP													3			37	64					
118	SEO															22	77	72					
119	T2													22	43	35	59	76					
120	SWSA													66			35	84					
121	T0T1													36			80	17					
122	T6													30	60			11					
123	MWL																	33					
124	MWT																	35					
125	TR1			5											30				9				
126	$\overline{\text{TR3}}$															10			15				
127	MR3																		25				
128	IOBO3			45		35	34	34											35				
129	TAN1															58			43				
130	$\overline{\text{TR2}}$															33			53				
131	IOBO2			41		65	32	32											57				
132	MR2																		65				
133	$\overline{\text{TR1}}$															27			10				
134	TR3			9											32				16				
135	MR1																		18				
136	C4																		36	67			
137	IOBO1			38		42	26	26											50				
138	$\overline{\text{TR0}}$															24			54				
139	TR2			7											38		71		56				
140	TR0			3											37	12			58				
141	IOBO0			35		21	24	24											60				
142	MR0																		68				
143	TR5			13											69					9			
144	$\overline{\text{TR7}}$															30	23			15			
145	MR7																			25			
146	IOBO7			52			50	50												35			
147	TAN2															57				43			
148	$\overline{\text{TR6}}$															23	55			53			
149	IOBO6			53			52	52												57			
150	MR6																			65			
151	$\overline{\text{TR5}}$															6				10			
152	TR7			17											83	11				16			
153	MR5																			18			
154	C8																			36	67		
155	IOBO5			51		61	42	42												50			
156	$\overline{\text{TR4}}$															79				54			
157	TR4			11											72		25			58			
158	IOBO4			42		63	36	36												60			
159	MR4																			68			
160	TR9			43											61	17					9		
161	$\overline{\text{TR11}}$														70	55					15		
162	MR11																				25		
163	IOBO11			55			64	64													35		
164	TAN3															60					43		
165	$\overline{\text{TR10}}$																				53		
166	IOBO10			58			66	66													57		
167	MR10																				65		
168	$\overline{\text{TR9}}$																57				10		
169	TR11			50											84	43	14				16		

INPUT/OUTPUT

REF	SIGNAL	222 MEMORY EXTENDER X2	221 MEMORY EXTENDER X1	220 I/O EXTENDER X2	219 I/O EXTENDER X1	218 (27)	217 (26)	216 (25)	215 (24)	214 (23)	213 (22)	212 (21)	211 (20)	210 (17)	209 (16)	208 (15)	207 (14)	206 (13)	205 (12)	204 (11)	203 (10)	202 I/O ADDRESS ENCODER	201 I/O CONTROL
114	$\overline{\text{RF2}}$																					36	
115	PH3																						
116	SWST																						
117	SWSP																						
118	SEO																						
119	T2																						83
120	SWSA																						
121	T0T1																						
122	T6																						
123	MWL																						
124	MWT	83																					
125	TR1																					84	
126	$\overline{\text{TR3}}$		67																			59	
127	MR3																						
128	IOBO3				55	45															45		
129	TAN1																						
130	$\overline{\text{TR2}}$		74																			66	
131	IOBO2				53	41															41		
132	MR2																						
133	$\overline{\text{TR1}}$		72																			80	
134	TR3																					60	
135	MR1																						
136	C4																						
137	IOBO1				51	38															38		
138	$\overline{\text{TR0}}$		68																			82	
139	TR2																						
140	TR0																						
141	IOBO0				49	35															35		
142	MR0																						
143	TR5																					58	
144	$\overline{\text{TR7}}$		82																				
145	MR7																						
146	IOBO7				63	52															52		
147	TAN2																						
148	$\overline{\text{TR6}}$		80																				
149	IOBO6				61	53															53		
150	MR6																						
151	$\overline{\text{TR5}}$		76																			79	
152	TR7																						
153	MR5																						
154	C8																						
155	IOBO5				59	51															51		
156	$\overline{\text{TR4}}$		77																			78	
157	TR4																					81	
158	IOBO4				57	42															42		
159	MR4																						
160	TR9																						
161	$\overline{\text{TR11}}$	67																					
162	MR11																						
163	IOBO11				73	55															55		
164	TAN3																						
165	$\overline{\text{TR10}}$	74																					
166	IOBO10				71	58															58		
167	MR10																						
168	$\overline{\text{TR9}}$	72																					
169	TR11																						

Table 5-8. Backplane Wiring List (Continued)

MEMORY

REF	SIGNAL	SOURCE	22	21 MEMORY PROTECT	20 DIRECT MEMORY LOGIC	19	18 INHIBIT DRIVER 0	17	16 INHIBIT DRIVER 1	15 "X" DRIVER/SWITCH 0-1	14 "Y" DRIVER/SWITCH 0-1	13 SENSE AMPLIFIER 0	12 SENSE AMPLIFIER 1	11 SENSE AMPLIFIER 2	10 SENSE AMPLIFIER 3	9 "X" DRIVER/SWITCH 2-3	8 "Y" DRIVER/SWITCH 2-3	7	6 INHIBIT DRIVER 2	5	4 INHIBIT DRIVER 3	3 PARITY ERROR	2 MEMORY MODULE DECODER	1 POWER FAIL
170	MR9	A103		68	42																			
171	C12																							
172	IOBO9			54																				
173	$\overline{TR8}$						30		30										30		30	30		
174	TR10																					22		
175	TR8																					32		
176	IOBO8			45																				
177	MR8	A103		66	36																			
178	TR13	A102																				13		
179	$\overline{TR15}$						82		82										82		82	3		
180	IOBO15																							
181	TAN4																							
182	$\overline{TR14}$						74		74										74		74	4		
183	IOBO14			43																				
184	MR14			72	64																			
185	$\overline{TR13}$						76		76										76		76	11		
186	TR15																					5		
187	MR13			77	60																			
188	C16																							
189	IOBO13			46																				
190	$\overline{TR12}$						66		66										66		66	12		
191	TR14																					6		
192	TR12																					14		
193	IOBO12			44																				
194	MR12			74	56																			
195	SB15																							
196	RB15																							
197	RB14	A102																						
198	TB0	A105																						
199	TB1																							
200	TB2																							
201	TB3	A105																						
202	TB4	A104																						
203	TB5																							
204	TB6																							
205	TB7	A104																						
206	TB8	A103																						
207	TB9																							
208	TB10																							
209	TB11	A103																						
210	TB12	A102																						
211	TB13																							
212	TB14																							
213	TB15	A102																						
214	PEH	A3																				62		
215	PEI	A3																				61		
216	-2V	PS	47/48										COPPER BUS											47/48
217	+4.5V		39/40										COPPER BUS											39/40
218	+7V																							
219	GND.		1/2										COPPER BUS											1/2
	GND.	PS	85/86										COPPER BUS											85/86
220	X0	A2					52			14		45											4	
221	X1								52	10			45										6	
222	X2													45		14			52				8	
223	X3														45	10					52		12	
224	Y0/1	A2									14												5	

LOGIC

REF	SIGNAL	SOURCE	122	121	120 DMA PACKER	119 DMA CONTROL	118 DMA ENCODER	117 DMA REGISTER 1	116 DMA REGISTER 2 OR DMI	115	114	113	112	111	110 EAU LOGIC	109 EAU TIMING	108 SHIFT LOGIC	107 INSTRUCTION DECODER	106 TIMING GENERATOR	105 ARITHMETIC LOGIC 0-3	104 ARITHMETIC LOGIC 4-7	103 ARITHMETIC LOGIC 8-11	102 ARITHMETIC LOGIC 12-15	101 FRONT PANEL COUPLER
170	MR9	A103																				18		
171	C12																					36	67	
172	IOBO9				56			62	62													50		
173	$\overline{TR8}$																36					54		
174	TR10				46													9				56		
175	TR8				34											78	13	29				58		
176	IOBO8				54			56	56													60		
177	MR8	A103																				68		
178	TR13	A102			66													30					9	
179	$\overline{TR15}$																		36				15	
180	IOBO15				74	51		78	78														35	
181	TAN4																59						43	
182	$\overline{TR14}$																						53	
183	IOBO14				65		15	76	76														57	
184	MR14																						65	
185	$\overline{TR13}$																						10	
186	TR15				70													41	38				16	
187	MR13																						18	
188	C16														50		64						36	
189	IOBO13				61	54		74	74														50	
190	$\overline{TR12}$																						54	
191	TR14				68													33					56	
192	TR12				62													17					58	
193	IOBO12				57			68	68														60	
194	MR12																						68	
195	SB15																50						6	
196	RB15														77		66						30	
197	RB14	A102													25								71	
198	TB0	A105													79		51			69			81	
199	TB1																75			13			75	
200	TB2																67			55			84	
201	TB3	A105															78			17	77		45	
202	TB4	A104																		81	69			
203	TB5																			75	13			
204	TB6																			84	55			
205	TB7	A104																		45	17	77		
206	TB8	A103																			81	69		
207	TB9																				75	13		
208	TB10																				84	55		
209	TB11	A103																			45	17	77	
210	TB12	A102															76					81	69	
211	TB13																73					75	13	
212	TB14																70					84	55	
213	TB15	A102													80	64	20			77		45	17	
214	PEH	A3																	57					
215	PEI	A3																	7					
216	-2V	PS			47/48								COPPER BUS											47/48
217	+4.5V				39/40								COPPER BUS											39/40
218	+7V																							
219	GND.				1/2																			1/2
	GND.	PS			85/86																			85/86
220	X0	A2																						
221	X1																							
222	X2																							
223	X3																							
224	Y0/1	A2																						

INPUT/OUTPUT

REF	SIGNAL	SOURCE	222 MEMORY EXTENDER X2	221 MEMORY EXTENDER X1	220 I/O EXTENDER X2	219 I/O EXTENDER X1	218 (27)	217 (26)	216 (25)	215 (24)	214 (23)	213 (22)	212 (21)	211 (20)	210 (17)	209 (16)	208 (15)	207 (14)	206 (13)	205 (12)	204 (11)	203 (10)	202 I/O ADDRESS ENCODER	201 I/O CONTROL
170	MR9	A103																						
171	C12																							
172	IOBO9					67	56															56		
173	$\overline{TR8}$		68																					
174	TR10																							
175	TR8																							
176	IOBO8					65	54															54		
177	MR8	A103																						
178	TR13	A102																						
179	$\overline{TR15}$		82																					
180	IOBO15					81	74															74		
181	TAN4																							
182	$\overline{TR14}$		80																					
183	IOBO14					79	65															65		
184	MR14																							
185	$\overline{TR13}$		76																					
186	TR15																							
187	MR13																							
188	C16																							
189	IOBO13					77	61															61		
190	$\overline{TR12}$		77																					
191	TR14																							
192	TR12																							
193	IOBO12					75	57															57		
194	MR12																							
195	SB15																							
196	RB15																							
197	RB14	A102																						
198	TB0	A105																					10	
199	TB1																						9	
200	TB2																						8	
201	TB3	A105																					7	
202	TB4	A104																					6	
203	TB5																						5	
204	TB6																							
205	TB7	A104																						
206	TB8	A103																						
207	TB9																							
208	TB10																							
209	TB11	A103																						
210	TB12	A102																						
211	TB13																							
212	TB14																							
213	TB15	A102																						
214	PEH	A3																						
215	PEI	A3																						
216	-2V	PS	47/48										COPPER BUS											47/48
217	+4.5V		39/40										COPPER BUS											39/40
218	+7V																							
219	GND.		1/2																					1/2
	GND.	PS	85/86																					85/86
220	X0	A2																						
221	X1																							
222	X2																							
223	X3																							
224	Y0/1	A2																						

Table 5-8. Backplane Wiring List (Continued)

MEMORY

REF	SIGNAL	SOURCE	22	21 MEMORY PROTECT	20 DIRECT MEMORY LOGIC	19	18 INHIBIT DRIVER 0	17	16 INHIBIT DRIVER 1	15 "X" DRIVER/ SWITCH 0-1	14 "Y" DRIVER/ SWITCH 0-1	13 SENSE AMPLIFIER 0	12 SENSE AMPLIFIER 1	11 SENSE AMPLIFIER 2	10 SENSE AMPLIFIER 3	9 "X" DRIVER/ SWITCH 2-3	8 "Y" DRIVER/ SWITCH 2-3	7	6 INHIBIT DRIVER 2	5	4 INHIBIT DRIVER 3	3 PARITY ERROR	2 MEMORY MODULE DECODER	1 POWER FAIL
225	Y2/3	A2															14						10	
226	MPT	A2																				34	82	
227	ST0	A105										3/4			3/4									
228	ST1											7/8			7/8									
229	ST2											11/12			11/12									
230	ST3											15/16			15/16									
231	ST4											19/20			19/20									
232	ST5											23/24			23/24									
233	ST6											27/28			27/28									
234	ST7											31/32			31/32									
235	ST8											35/36			35/36									
236	ST9											51/52			51/52									
237	ST10											55/56			55/56									
238	ST11											59/60			59/60									
239	ST12											63/64			63/64									
240	ST13											67/68			67/68									
241	ST14											71/72			71/72									
242	ST15	A105										75/76			75/76									
243	IOGE(B)	I/O SECT																						15
244	T3(B)																							
245	SIR			36																		37		32
246	IAK			56																		38		10
247	IEN(20)																							
248	IEN(6)			53																				
249	IEN(10)																							
250	CRS																							
251	FLG0																							
252	FLG1																							
253	FLG2																							
254	FLG3																							
255	SKF																							12
256	ENF	I/O SECT																				71		46
257	INT	A1		31																		79		28
258	IOS	A201																						
259	$\overline{\text{PH5}}$	A201																						
260	ESR	I/O SECT																						
261	SCL(0)																							
262	SCL(1)			71																				
263	SCL(2)																							
264	SCL(3)																							
265	SCL(4)																							16
266	SCL(5)			12																		9		
267	SCL(6)																							
268	SCL(7)																							
269	SCM(0)			9																		7		14
270	SCM(1)																							
271	SCM(2)																							
272	SCM(3)																							
273	SCM(4)																							
274	SCM(5)																							
275	SCM(6)																							
276	SCM(7)																							
277	IRQ1																							
278	IRQ2																							
279	IRQ3	I/O SECT																						

LOGIC

REF	SIGNAL	SOURCE	122	121	120 DMA PACKER	119 DMA CONTROL	118 DMA ENCODER	117 DMA REGISTER 1	116 DMA REGISTER 2 OR DMI	115	114	113	112	111	110 EAU LOGIC	109 EAU TIMING	108 SHIFT LOGIC	107 INSTRUCTION DECODER	106 TIMING GENERATOR	105 ARITHMETIC LOGIC 0-3	104 ARITHMETIC LOGIC 4-7	103 ARITHMETIC LOGIC 8-11	102 ARITHMETIC LOGIC 12-15	101 FRONT PANEL COUPLER
225	Y2/3	A2																						
226	MPT	A2																						
227	ST0	A105																		49/1				
228	ST1																			4/2				
229	ST2																			52/2				
230	ST3																			11/1				
231	ST4																				49/1			
232	ST5																				4/2			
233	ST6																				52/2			
234	ST7																				11/1			
235	ST8																					49/1		
236	ST9																					4/2		
237	ST10																					52/2		
238	ST11																					11/1		
239	ST12																						49/1	
240	ST13																						4/2	
241	ST14																						52/2	
242	ST15	A105																					11/1	
243	IOGE(B)	I/O SECT				22	84	11	11															
244	T3(B)							5	5															
245	SIR					34	70	53	53															
246	IAK					27			44															
247	IEN(20)																							
248	IEN(6)					7			35															
249	IEN(10)																							
250	CRS					32	74	9	9							68								
251	FLG0					25			30															
252	FLG1																							
253	FLG2																							
254	FLG3																							
255	SKF					29			15								31							
256	ENF	I/O SECT				37	49																	
257	INT	A1																	44					
258	IOS	A201														29	81							
259	$\overline{\text{PH5}}$	A201																						
260	ESR	I/O SECT																						
261	SCL(0)						32																	
262	SCL(1)						80																	
263	SCL(2)						18		13															
264	SCL(3)						82	13																
265	SCL(4)						38																	
266	SCL(5)						79																	
267	SCL(6)					36	46																	
268	SCL(7)					38	50																	
269	SCM(0)					18	51	14	14															
270	SCM(1)						67																	
271	SCM(2)						69																	
272	SCM(3)																							
273	SCM(4)																							
274	SCM(5)																							
275	SCM(6)																							
276	SCM(7)																							
277	IRQ1																							
278	IRQ2																							
279	IRQ3	I/O SECT																						

INPUT/OUTPUT

REF	SIGNAL	SOURCE	222 MEMORY EXTENDER X2	221 MEMORY EXTENDER X1	220 I/O EXTENDER X2	219 I/O EXTENDER X1	218 (27)	217 (26)	216 (25)	215 (24)	214 (23)	213 (22)	212 (21)	211 (20)	210 (17)	209 (16)	208 (15)	207 (14)	206 (13)	205 (12)	204 (11)	203 (10)	202 I/O ADDRESS ENCODER	201 I/O CONTROL
225	Y2/3	A2																						
226	MPT	A2																						
227	ST0	A105		4/3																				
228	ST1			6/5																				
229	ST2			8/7																				
230	ST3			10/9																				
231	ST4			12/11																				
232	ST5			14/13																				
233	ST6			16/15																				
234	ST7			18/17																				
235	ST8		4/3																					
236	ST9		6/5																					
237	ST10		8/7																					
238	ST11		10/9																					
239	ST12		12/11																					
240	ST13		14/13																					
241	ST14		16/15																					
242	ST15	A105	18/17																					
243	IOGE(B)	I/O SECT			15																	15	34	37
244	T3(B)				11																	11		81
245	SIR				32																	32		35
246	IAK				10																	10		77
247	IEN(20)				4		8						8	8/23										7
248	IEN(6)																							5/10
249	IEN(10)														8							8		3
250	CRS				13																	13		65
251	FLG0														4	4/49						4/49	14	
252	FLG1					26	4/49							4/49	49								16	
253	FLG2					28																	13	
254	FLG3					30																	15	
255	SKF				12																	12		73
256	ENF	I/O SECT			46																	46		67
257	INT	A1																					3	
258	IOS	A201																						6
259	$\overline{\text{PH5}}$	A201																					4	9
260	ESR	I/O SECT																					12	21
261	SCL(0)				67		34							16	34							16	65	38
262	SCL(1)				71								16	34							16	34	67	42
263	SCL(2)				73							16	34							16	34		61	
264	SCL(3)				75						16	34							16	34			63	
265	SCL(4)				77					16	34							16	34				51	
266	SCL(5)				79				16	34							16	34					52	
267	SCL(6)				81			16	34							16	34						49	
268	SCL(7)				83		16	34							16	34							50	
269	SCM(0)				55																		75	36
270	SCM(1)														14	14/37						14/37	77	
271	SCM(2)						14	14/37						14/37	37								71	
272	SCM(3)				57		37																73	
273	SCM(4)				59																		56	
274	SCM(5)				61																		57	
275	SCM(6)				63																		54	
276	SCM(7)				65																		55	
277	IRQ1					50							6	33									17	
278	IRQ2					52						6	33										21	
279	IRQ3	I/O SECT				54						6	33										23	

NOTE: Shaded area denotes twisted pair. Top pin is signal, bottom pin is ground.

Table 5-8. Backplane Wiring List (Continued)

MEMORY

REF	SIGNAL	SOURCE	22	21 MEMORY PROTECT	20 DIRECT MEMORY LOGIC	19	18 INHIBIT DRIVER 0	17	16 INHIBIT DRIVER 1	15 "X" DRIVER/ SWITCH 0-1	14 "Y" DRIVER/ SWITCH 0-1	13 SENSE AMPLIFIER 0	12 SENSE AMPLIFIER 1	11 SENSE AMPLIFIER 2	10 SENSE AMPLIFIER 3	9 "X" DRIVER/ SWITCH 2-3	8 "Y" DRIVER/ SWITCH 2-3	7	6 INHIBIT DRIVER 2	5	4 INHIBIT DRIVER 3	3 PARITY ERROR	2 MEMORY MODULE DECODER	1 POWER FAIL
280	IRQ4	I/O SECT																						6
281	IRQ5			35																		77		
282	IRQ6																							
283	IRQ7																							
284	IRQ10																							
285	IRQ11																							
286	IRQ12																							
287	IRQ13																							
288	IRQ14																							
289	IRQ15																							
290	IRQ16																							
291	IRQ17																							
292	PRH 10 PRL																							
293	11/10																							
294	12/11																							
295	13/12																							
296	14/13																							
297	15/14																							
298	16/15																							
299	17/16																							
300	20/17																							
301	21/20																							
302	22/21																							
303	23/22																							
304	24/23																							
305	25/24																							
306	26/25																							
307	27/26																							
308	30/27																							
309	5/4			38																		25		3
310	PRH 6/5 PRL			51																		27		
311	POPIO(B)			29																				
312	IOBI0			79																				
313	1			80																				
314	2			78																				
315	3			75																				
316	4			81																				
317	5			82																				
318	6			84																				
319	7			83																				
320	8			64																				
321	9			65																				
322	10			67																				
323	11			62																				
324	12			70																				
325	13			73																				
326	14			76																				
327	15																					28		
328	16																							
329	SRQ10																							
330	SRQ11																							
331	SRQ12																							
332	SRQ13																							
333	SRQ14																							
334	SRQ15																							
335	SRQ16																							
336	SRQ17																							
337	SRQ20																							
338	SRQ21	I/O SECT																						

LOGIC

REF	SIGNAL	122	121	120 DMA PACKER	119 DMA CONTROL	118 DMA ENCODER	117 DMA REGISTER 1	116 DMA REGISTER 2 OR DMI	115	114	113	112	111	110 EAU LOGIC	109 EAU TIMING	108 SHIFT LOGIC	107 INSTRUCTION DECODER	106 TIMING GENERATOR	105 ARITHMETIC LOGIC 0-3	104 ARITHMETIC LOGIC 4-7	103 ARITHMETIC LOGIC 8-11	102 ARITHMETIC LOGIC 12-15	101 FRONT PANEL COUPLER
280	IRQ4																						
281	IRQ5																						
282	IRQ6				28			29															
283	IRQ7				26																		
284	IRQ10																						
285	IRQ11																						
286	IRQ12																						
287	IRQ13																						
288	IRQ14																						
289	IRQ15																						
290	IRQ16																						
291	IRQ17																						
292	PRH 10 PRL				9																		
293	11/10																						
294	12/11																						
295	13/12																						
296	14/13																						
297	15/14																						
298	16/15																						
299	17/16																						
300	20/17																						
301	21/20																						
302	22/21																						
303	23/22																						
304	24/23																						
305	25/24																						
306	26/25																						
307	27/26																						
308	30/27																						
309	5/4					57																	
310	PRH 6/5 PRL							33															
311	POPIO(B)				35																		
312	IOBI0			26			17	17											79				3
313	1			29			25	25											32				7
314	2			30			28	28											33				11
315	3			64			58	58											27				15
316	4			77			77	77												79			19
317	5			80			80	80												32			23
318	6			81			79	79												33			27
319	7			84			81	81												27			31
320	8			27			21	21													79		35
321	9			28			19	19													32		41
322	10			31			27	27													33		45
323	11			60			49	49													27		51
324	12			78			61	61														79	55
325	13			79			75	75														32	59
326	14			82				73														33	63
327	15			83																		27	67
328	16																						
329	SRQ10					22																	
330	SRQ11					28																	
331	SRQ12					20																	
332	SRQ13					26																	
333	SRQ14					33																	
334	SRQ15					44																	
335	SRQ16					29																	
336	SRQ17					37																	
337	SRQ20					71																	
338	SRQ21					66																	

INPUT/OUTPUT

REF	SIGNAL	222 MEMORY EXTENDER X2	221 MEMORY EXTENDER X1	220 I/O EXTENDER X2	219 I/O EXTENDER X1	218 (27)	217 (26)	216 (25)	215 (24)	214 (23)	213 (22)	212 (21)	211 (20)	210 (17)	209 (16)	208 (15)	207 (14)	206 (13)	205 (12)	204 (11)	203 (10)	202 I/O ADDRESS ENCODER	201 I/O CONTROL
280	IRQ4				56				6	33												27	
281	IRQ5				58			6	33													29	
282	IRQ6				60		6	33														25	
283	IRQ7				62	6	33															19	
284	IRQ10				64	33															6	33	
285	IRQ11				66															6	33	35	
286	IRQ12				68														6	33		37	
287	IRQ13				72													6	33			18	
288	IRQ14				74												6	33				31	
289	IRQ15				76											6	33					20	
290	IRQ16				78										6	33						38	
291	IRQ17				80									6	33							22	
292	PRH 10 PRL																				23		12 14 80
293	11/10																			23	3		
294	12/11																		23	3			
295	13/12																	23	3				
296	14/13																23	3					
297	15/14															23	3						
298	16/15														23	3							
299	17/16													23	3								
300	20/17													3									16
301	21/20											23	3										
302	22/21										23	3											
303	23/22									23	3												
304	24/23								23	3													
305	25/24							23	3														
306	26/25						23	3															
307	27/26					23	3																
308	30/27			3		3																	
309	5/4																						84
310	PRH 6/5 PRL																						76 82
311	POPIO(B)			17																	17		72
312	IOBI0			50		26																26	
313	1			52		29															29	28	
314	2			54		30															30	41	
315	3			56		64															64	45	
316	4			58		77															77	42	
317	5			60		80															80	30	
318	6			62		81															81		
319	7			64		84															84		
320	8			66		27															27		
321	9			68		28															28		
322	10			72		31															31		
323	11			74		60															60		
324	12			76		78															78		
325	13			78		79															79		
326	14			80		82															82		
327	15			82		83															83		
328	16			30		18															18		
329	SRQ10																				19		
330	SRQ11																			19			
331	SRQ12																		19				
332	SRQ13																	19					
333	SRQ14																19						
334	SRQ15															19							
335	SRQ16														19								
336	SRQ17													19									
337	SRQ20												19										
338	SRQ21											19											

Table 5-8. Backplane Wiring List (Continued)

MEMORY

REF	SIGNAL	SOURCE	22	MEMORY PROTECT 21	DIRECT MEMORY LOGIC 20	19	INHIBIT DRIVER 0 18	17	INHIBIT DRIVER 1 16	"X" DRIVER/ SWITCH 0-1 15	"Y" DRIVER/ SWITCH 0-1 14	SENSE AMPLIFIER 0 13	SENSE AMPLIFIER 1 12	SENSE AMPLIFIER 2 11	SENSE AMPLIFIER 3 10	"X" DRIVER/ SWITCH 2-3 9	"Y" DRIVER/ SWITCH 2-3 8	7	INHIBIT DRIVER 2 6	5	INHIBIT DRIVER 3 4	PARITY ERROR 3	MEMORY MODULE DECODER 2	POWER FAIL 1
339	SRQ22	I/OSECT																						
340	SRQ23	↑																						
341	SRQ24																							
342	SRQ25																							
343	SRQ26																							
344	SRQ27																							
345	IOBO16																							
346	LAMP GND.	↓																						
347	HIS	I/OSECT																						
348	EDT	A119																						
349	IOGE	A1		19																				59
350	PNS	A101																						
351	MNS	A101																					74	
352	ILS	A101																						
353	PON	A1								46	46					46	46							58
354	POF P	A1																						56
355	PRS	A101																						78
356	PRSW	A101																						
357	RNSW	↑																						
358	RNS																							60
359	$\overline{HLS}$																							
360	HLS																							72
361	LMS																							
362	LAS																							
363	LBS																							
364	LADS																							
365	DMS																							
366	SCS																							
367	LPS	↓																					49	
368	PIND	A101																						49
369	-5.6V	PS																						75
370	RSET	A109																						
371	DS3	↑																						
372	DS4																							
373	DS34																							
374	DT58																							
375	SRCS																							
376	MD2																							
377	ISG																							
378	OVD																							
379	ROT5																							
380	OASL																							
381	RSDS			15																		72		
382	T23																							
383	MP1																							
384	MP2																							
385	MP3																							
386	MP4																							
387	MP5																							
388	D1																							
389	D2																							
390	D3																							
391	D4																							
392	D5																							
393	D6																							
394	TOD																							
395	TEV																							
396	OVR	↓																						
397	OVR	A109																						

LOGIC

REF	SIGNAL	122	121	DMA PACKER 120	DMA CONTROL 119	DMA ENCODER 118	DMA REGISTER 117	DMA REGISTER 2 OR DMI 116	115	114	113	112	111	EAU LOGIC 110	EAU TIMING 109	SHIFT LOGIC 108	INSTRUCTION DECODER 107	TIMING GENERATOR 106	ARITHMETIC LOGIC 0-3 105	ARITHMETIC LOGIC 4-7 104	ARITHMETIC LOGIC 8-11 103	ARITHMETIC LOGIC 12-15 102	FRONT PANEL COUPLER 101
339	SRQ22					68																	
340	SRQ23					64																	
341	SRQ24					58																	
342	SRQ25					54																	
343	SRQ26					56																	
344	SRQ27					52																	
345	IOBO16																						
346	LAMP GND.																						
347	HIS					83																	
348	EDT				42																		
349	IOGE															16							
350	PNS																	43					18
351	MNS																						22
352	ILS																73						26
353	PON																						71
354	POF P																	77					10
355	PRS																	78					30
356	PRSW																	79					34
357	RNSW																						38
358	RNS																	70					44
359	$\overline{HLS}$																	45					50
360	HLS																	50					54
361	LMS																	46					58
362	LAS																	80					62
363	LBS																	65					66
364	LADS																	68					70
365	DMS																	59					74
366	SCS																	56					78
367	LPS																						82
368	PIND																						75
369	-5.6V																						79
370	RSET													63	42								
371	DS3													67	28								
372	DS4													52	9								
373	DS34													14	6								
374	DT58													71	27								
375	SRCS													83	31								
376	MD2													16	79								
377	ISG				3										63			4					
378	OVD													56	80								
379	ROT5													68	82								
380	OASL													31	5								
381	RSDS														65								
382	T23													21	35								
383	MP1													59	12								
384	MP2													5	11								
385	MP3													69	4								
386	MP4													46	3								
387	MP5													9	8								
388	D1													62	34								
389	D2													60	33								
390	D3													27	26								
391	D4													6	25								
392	D5													73	17								
393	D6													8	18								
394	TOD													82	45								
395	TEV													81	56								
396	OVR													35	22								
397	OVR													64	16								

INPUT/OUTPUT

REF	SIGNAL	MEMORY EXTENDER X2 222	MEMORY EXTENDER X1 221	I/O EXTENDER X2 220	I/O EXTENDER X1 219	27 218	26 217	25 216	24 215	23 214	22 213	21 212	20 211	17 210	16 209	15 208	14 207	13 206	12 205	11 204	10 203	I/O ADDRESS ENCODER 202	I/O CONTROL 201
339	SRQ22										19												
340	SRQ23									19													
341	SRQ24								19														
342	SRQ25							19															
343	SRQ26						19																
344	SRQ27					19																	
345	IOBO16				83	73	←													→	73		
346	LAMP GND.																						
347	HIS																						4
348	EDT				3	62	←													→	62		
349	IOGE																						33
350	PNS																						
351	MNS																						
352	ILS																						
353	PON				41	66	←													→	66		
354	POF P																						
355	PRS																						
356	PRSW																						
357	RNSW																						
358	RNS																						
359	$\overline{HLS}$																						
360	HLS																						
361	LMS			18		59	←													→	59		
362	LAS																						
363	LBS																						
364	LADS																						
365	DMS																						
366	SCS																						
367	LPS																						
368	PIND																						
369	-5.6V																						
370	RSET																						
371	DS3																						
372	DS4																						
373	DS34																						
374	DT58																						
375	SRCS																						
376	MD2																						
377	ISG																						
378	OVD																						
379	ROT5																						
380	OASL																						
381	RSDS																						
382	T23																						
383	MP1																						
384	MP2																						
385	MP3																						
386	MP4																						
387	MP5																						
388	D1																						
389	D2																						
390	D3																						
391	D4																						
392	D5																						
393	D6																						
394	TOD																						
395	TEV																						
396	OVR																						
397	OVR																						

Table 5-8. Backplane Wiring List (Continued)

MEMORY

REF	SIGNAL	SOURCE	22	21 MEMORY PROTECT	20 DIRECT MEMORY LOGIC	19	18 INHIBIT DRIVER 0	17	16 INHIBIT DRIVER 1	15 "X" DRIVER/SWITCH 0-1	14 "Y" DRIVER/SWITCH 0-1	13 SENSE AMPLIFIER 0	12 SENSE AMPLIFIER 1	11 SENSE AMPLIFIER 2	10 SENSE AMPLIFIER 3	9 "X" DRIVER/SWITCH 2-3	8 "Y" DRIVER/SWITCH 2-3	7	6 INHIBIT DRIVER 2	5	4 INHIBIT DRIVER 3	3 PARITY ERROR	2 MEMORY MODULE DECODER	1 POWER FAIL
398	RO	A109																						
399	AS	↑																						
400	RT																							
401	RT																							
402	EXIT																							
403	GATE																							
404	DL3																							
405	DL4																							
406	SLMB				73																			
407	SRMB	↓			61																			
408	SL14B	A109			84																			
409	EOFB	A110			82																			
410	CMFB	A110			80																			
411	IIR	A109		69	71																			
412	MPC	A21		25																		63		36
413	DM0	DMA			3																			
414	DM1	↑			7																			
415	DM2				11																			
416	DM3				15																			
417	DM4				19																			
418	DM5				23																			
419	DM6				27																			
420	DM7				31																			
421	DM8				35																			
422	DM9				41																			
423	DM10				45																			
424	DM11				51																			
425	DM12				55																			
426	DM13				59																			
427	DM14				63																			
428	PH5			7	69																	8		
429	IODO																							
430	COUT																							
431	OUT																							
432	C1																							
433	SMAR2																							
434	CR2																							
435	DIN1																							
436	WCR1																							
437	SWCR2																							
438	TE1																							
439	CM2																							
440	CIN																							
441	SMAR1																							
442	DIN2																							
443	WCR2																							
444	CR1																							
445	SWCR1																							
446	TE2																							
447	OHC1																							
448	OHC2																							
449	OLC1																							
450	OLC2																							
451	IDW1																							
452	IDW2																							
453	IHC1																							
454	IHC2																							
455	DE-1	↓																						
456	DE-2	DMA																						

LOGIC

REF	SIGNAL	122	121	120 DMA PACKER	119 DMA CONTROL	118 DMA ENCODER	117 DMA REGISTER 1	116 DMA REGISTER 2 OR DMI	115	114	113	112	111	110 EAU LOGIC	109 EAU TIMING	108 SHIFT LOGIC	107 INSTRUCTION DECODER	106 TIMING GENERATOR	105 ARITHMETIC LOGIC 0-3	104 ARITHMETIC LOGIC 4-7	103 ARITHMETIC LOGIC 8-11	102 ARITHMETIC LOGIC 12-15	101 FRONT PANEL COUPLER
398	RO													75	46								
399	AS													84	50								
400	RT													57	52								
401	RT													78	58								
402	EXIT													17	74								
403	GATE													76	59								
404	DL3													70	57								
405	DL4													18	36								
406	SLMB														44								
407	SRMB														41								
408	SL14B														49								
409	EOFB													26									
410	CMFB													72									
411	IIR														77			6					
412	MPC																						
413	DM0						41	41															
414	DM1						46	46															
415	DM2						45	45															
416	DM3						55	55															
417	DM4						65	65															
418	DM5						63	63															
419	DM6						71	71															
420	DM7						72	72															
421	DM8						83	83															
422	DM9						82	82															
423	DM10						6	6															
424	DM11						10	10															
425	DM12						12	12															
426	DM13						16	16															
427	DM14						7	7															
428	PH5				8	78		70							53								
429	IODO			19	4																		
430	COUT				63	36																	
431	OUT				65	6																	
432	C1				67	7																	
433	SMAR2				69		38																
434	CR2				71	27																	
435	DIN1				75			4															
436	WCR1				77			84															
437	SWCR2				79		3																
438	TE1				66	60																	
439	CM2				68	81																	
440	CIN				70	41																	
441	SMAR1				72			38															
442	DIN2				74		4																
443	WCR2				76		84																
444	CR1				78	34																	
445	SWCR1				80			3															
446	TE2				62	62																	
447	OHC1			20		10																	
448	OHC2			21		12																	
449	OLC1			22		19																	
450	OLC2			23		13																	
451	IDW1			24		16																	
452	IDW2			25		14																	
453	IHC1			32		9																	
454	IHC2			36		8																	
455	DE-1					53																	
456	DE-2					55																	

INPUT/OUTPUT

REF	SIGNAL	222 MEMORY EXTENDER X2	221 MEMORY EXTENDER X1	220 I/O EXTENDER X2	219 I/O EXTENDER X1	218 27	217 26	216 25	215 24	214 23	213 22	212 21	211 20	210 17	209 16	208 15	207 14	206 13	205 12	204 11	203 10	202 I/O ADDRESS ENCODER	201 I/O CONTROL
398	RO																						
399	AS																						
400	RT																						
401	RT																						
402	EXIT																						
403	GATE																						
404	DL3																						
405	DL4																						
406	SLMB																						
407	SRMB																						
408	SL14B																						
409	EOFB																						
410	CMFB																						
411	IIR																						
412	MPC																						
413	DM0																						
414	DM1																						
415	DM2																						
416	DM3																						
417	DM4																						
418	DM5																						
419	DM6																						
420	DM7																						
421	DM8																						
422	DM9																						
423	DM10																						
424	DM11																						
425	DM12																						
426	DM13																						
427	DM14																						17
428	PH5																						
429	IODO																						
430	COUT																						
431	OUT																						
432	C1																						
433	SMAR2																						
434	CR2																						
435	DIN1																						
436	WCR1																						
437	SWCR2																						
438	TE1																						
439	CM2																						
440	CIN																						
441	SMAR1																						
442	DIN2																						
443	WCR2																						
444	CR1																						
445	SWCR1																						
446	TE2																						
447	OHC1																						
448	OHC2																						
449	OLC1																						
450	OLC2																						
451	IDW1																						
452	IDW2																						
453	IHC1																						
454	IHC2																						
455	DE-1			26																			
456	DE-2			28																			

Table 5-8. Backplane Wiring List (Continued)

MEMORY

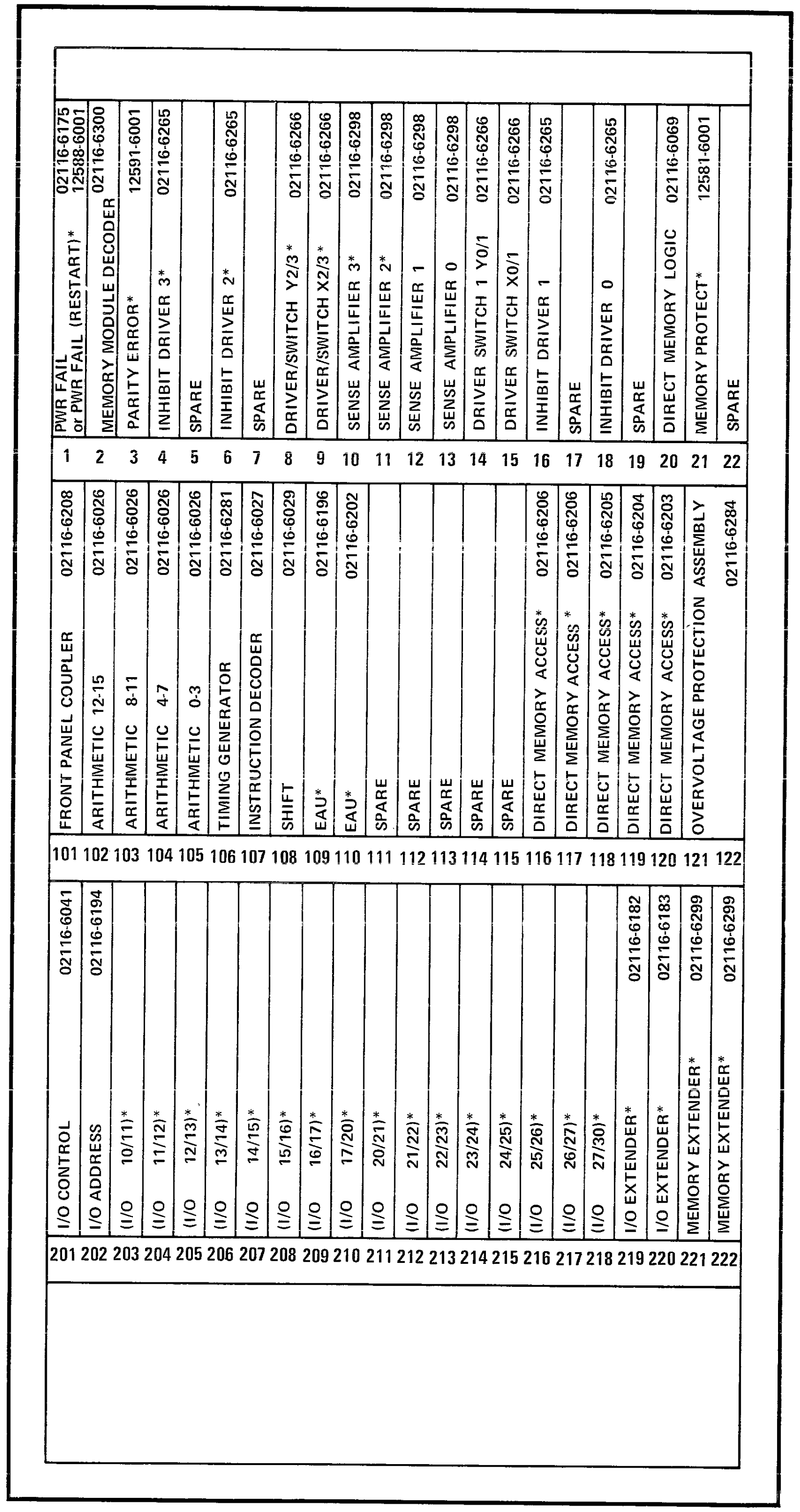
REF	SIGNAL	SOURCE	22	MEMORY PROTECT 21	DIRECT MEMORY LOGIC 20	19	INHIBIT DRIVER 0 18	17	INHIBIT DRIVER 1 16	"X" DRIVER/ SWITCH 0-1 15	"Y" DRIVER/ SWITCH 0-1 14	SENSE AMPLIFIER 0 13	SENSE AMPLIFIER 1 12	SENSE AMPLIFIER 2 11	SENSE AMPLIFIER 3 10	"X" DRIVER/ SWITCH 2-3 9	"Y" DRIVER/ SWITCH 2-3 8	7	INHIBIT DRIVER 2 6	5	INHIBIT DRIVER 3 4	PARITY ERROR 3	MEMORY MODULE DECODER 2	POWER FAIL 1
457	MMD13	A11												84									27	
458	$\overline{\text{TR16}}$	A3					80		80										80		80	53		
459	ST16	A3										79/80	79/80	79/80	79/80							60/86		
460	MMD GND.	A8									10/1						10/1							
461	PSO	A1																						51
462	MPT0	A6					83/39												83					
463	MPT1	A18					81												83				37	
464	MPT2	A6																	81				35	
465	RUN	I/O SECT																						
466	SPARE																							
467	THERM SW	A2																					81	52
468	PRH6	A119																						
469	TSA	A106		27																		17		
470	TTK	222																					25	
471	P123B	A106																						
472	+4.5V	PS																						
473	M14	A20			66																			
474	MMD14	221																					29	
475	$\overline{\text{MNS}}$	A2																					76	
	$\overline{\text{MNS}}$	A2																						
476	$\overline{\text{MPT}}$	A2																					78	
477	MPT3	221																					33	
478	MPT4	222																					31	
479	PRESET LAMP	A1																						35
480	EPO	A1																						37
481	EPF	A1																						42
482	IN	A119																						
483	$\overline{\text{MR1}}$	A105																						
484	$\overline{\text{MR0}}$	↑																						
485	$\overline{\text{MR3}}$	↓																						
486	$\overline{\text{MR2}}$	A105																						
487	$\overline{\text{MR5}}$	A104																						
488	$\overline{\text{MR4}}$	↑																						
489	$\overline{\text{MR7}}$	↓																						
490	$\overline{\text{MR6}}$	A104																						
491	$\overline{\text{MR9}}$	A103																						
492	$\overline{\text{MR8}}$	↑																						
493	$\overline{\text{MR11}}$	↓																						
494	$\overline{\text{MR10}}$	A103																						
495	$\overline{\text{MR12}}$	A102																						
496	TR0(B)	A120																						
497	TR1(B)	↑																						
498	TR2(B)																							
499	TR3(B)																							
500	TR4(B)																							
501	TR5(B)																							
502	TR6(B)																							
503	TR7(B)																							
504	TR8(B)																							
505	TR9(B)																							
506	TR10(B)																							
507	TR11(B)																							
508	TR12(B)																							
509	TR13(B)																							
510	TR14(B)	↓																						
511	TR15(B)	A120																						

LOGIC

REF	SIGNAL	SOURCE	122	121	DMA PACKER 120	DMA CONTROL 119	DMA ENCODER 118	DMA REGISTER 1 117	DMA REGISTER 2 OR DMI 116	115	114	113	112	111	EAU LOGIC 110	EAU TIMING 109	SHIFT LOGIC 108	INSTRUCTION DECODER 107	TIMING GENERATOR 106	ARITHMETIC LOGIC 0-3 105	ARITHMETIC LOGIC 4-7 104	ARITHMETIC LOGIC 8-11 103	ARITHMETIC LOGIC 12-15 102	FRONT PANEL COUPLER 101
457	MMD13	A11																						
458	$\overline{\text{TR16}}$	A3																						
459	ST16	A3																						
460	MMD GND.	A8																						
461	PSO	A1																						
462	MPT0	A6																						
463	MPT1	A18																						
464	MPT2	A6																						
465	RUN	I/O SECT																						
466	SPARE																							
467	THERM SW	A2																						
468	PRH6	A119				31			23															
469	TSA	A106					45	59	59						29	76			67					
470	TTK	222																						
471	P123B	A106																	10					
472	+4.5V	PS																						
473	M14	A20																						
474	MMD14	221																						
475	$\overline{\text{MNS}}$	A2																	19/20					
	$\overline{\text{MNS}}$	A2																	22/26					
476	$\overline{\text{MPT}}$	A2																	12					
477	MPT3	221																						
478	MPT4	222																						
479	PRESET LAMP	A1																						
480	EPO	A1																						
481	EPF	A1																						
482	IN	A119				52																		
483	$\overline{\text{MR1}}$	A105																		19				
484	$\overline{\text{MR0}}$	↑																		63				
485	$\overline{\text{MR3}}$	↓																		24				
486	$\overline{\text{MR2}}$	A105																		66				
487	$\overline{\text{MR5}}$	A104																			19			
488	$\overline{\text{MR4}}$	↑																			63			
489	$\overline{\text{MR7}}$	↓																			24			
490	$\overline{\text{MR6}}$	A104																			66			
491	$\overline{\text{MR9}}$	A103																				19		
492	$\overline{\text{MR8}}$	↑																				63		
493	$\overline{\text{MR11}}$	↓																				24		
494	$\overline{\text{MR10}}$	A103																				66		
495	$\overline{\text{MR12}}$	A102																					63	
496	TR0(B)	A120			4												4							
497	TR1(B)	↑			6																			
498	TR2(B)				8												15							
499	TR3(B)				10																			
500	TR4(B)				12																			
501	TR5(B)				14																			
502	TR6(B)				16																			
503	TR7(B)				18																			
504	TR8(B)				33																			
505	TR9(B)				37																			
506	TR10(B)				44																			
507	TR11(B)				49																			
508	TR12(B)				59																			
509	TR13(B)				63																			
510	TR14(B)	↓			67																			
511	TR15(B)	A120			69																			

INPUT/OUTPUT

REF	SIGNAL	SOURCE	MEMORY EXTENDER X2 222	MEMORY EXTENDER X1 221	I/O EXTENDER X2 220	I/O EXTENDER X1 219	27 218	26 217	25 216	24 215	23 214	22 213	21 212	20 211	17 210	16 209	15 208	14 207	13 206	12 205	11 204	10 203	I/O ADDRESS ENCODER 202	I/O CONTROL 201
457	MMD13	A11	42/62	42/65																				
458	$\overline{\text{TR16}}$	A3		83																				
459	ST16	A3		20/19																				
460	MMD GND.	A8	1/26																					
461	PSO	A1																						
462	MPT0	A6																						
463	MPT1	A18																						
464	MPT2	A6		21																				
465	RUN	I/O SECT			41		50	←													→	50	32	
466	SPARE				84		68	←													→	68		
467	THERM SW	A2																						
468	PRH6	A119																						78
469	TSA	A106																						
470	TTK	222	33 46 84	33																				
471	P123B	A106																						
472	+4.5V	PS	39	31/46																				
473	M14	A20		49																				
474	MMD14	221	64	64/51																				
475	$\overline{\text{MNS}}$	A2																						
	$\overline{\text{MNS}}$	A2																						
476	$\overline{\text{MPT}}$	A2																						
477	MPT3	221		84																				
478	MPT4	222	21																					
479	PRESET LAMP	A1																						
480	EPO	A1																						
481	EPF	A1																						
482	IN	A119																						
483	$\overline{\text{MR1}}$	A105																						
484	$\overline{\text{MR0}}$	↑																						
485	$\overline{\text{MR3}}$	↓																						
486	$\overline{\text{MR2}}$	A105																						
487	$\overline{\text{MR5}}$	A104																						
488	$\overline{\text{MR4}}$	↑																						
489	$\overline{\text{MR7}}$	↓																						
490	$\overline{\text{MR6}}$	A104																						
491	$\overline{\text{MR9}}$	A103																						
492	$\overline{\text{MR8}}$	↑																						
493	$\overline{\text{MR11}}$	↓																						
494	$\overline{\text{MR10}}$	A103																						
495	$\overline{\text{MR12}}$	A102																						
496	TR0(B)	A120																					83	
497	TR1(B)	↑																						
498	TR2(B)																						53	
499	TR3(B)																							
500	TR4(B)																							
501	TR5(B)																							
502	TR6(B)																							
503	TR7(B)																							
504	TR8(B)																							
505	TR9(B)																							
506	TR10(B)																							
507	TR11(B)																							
508	TR12(B)																							
509	TR13(B)																							
510	TR14(B)	↓																						
511	TR15(B)	A120																						



NOTES:

* OPTIONAL CARDS MAY BE ADDED AT ANY TIME IF THE CURRENT REQUIREMENTS DO NOT EXCEED THE POWER SUPPLY RATINGS

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Figure 5-5. Card-Cage Assembly, Front View

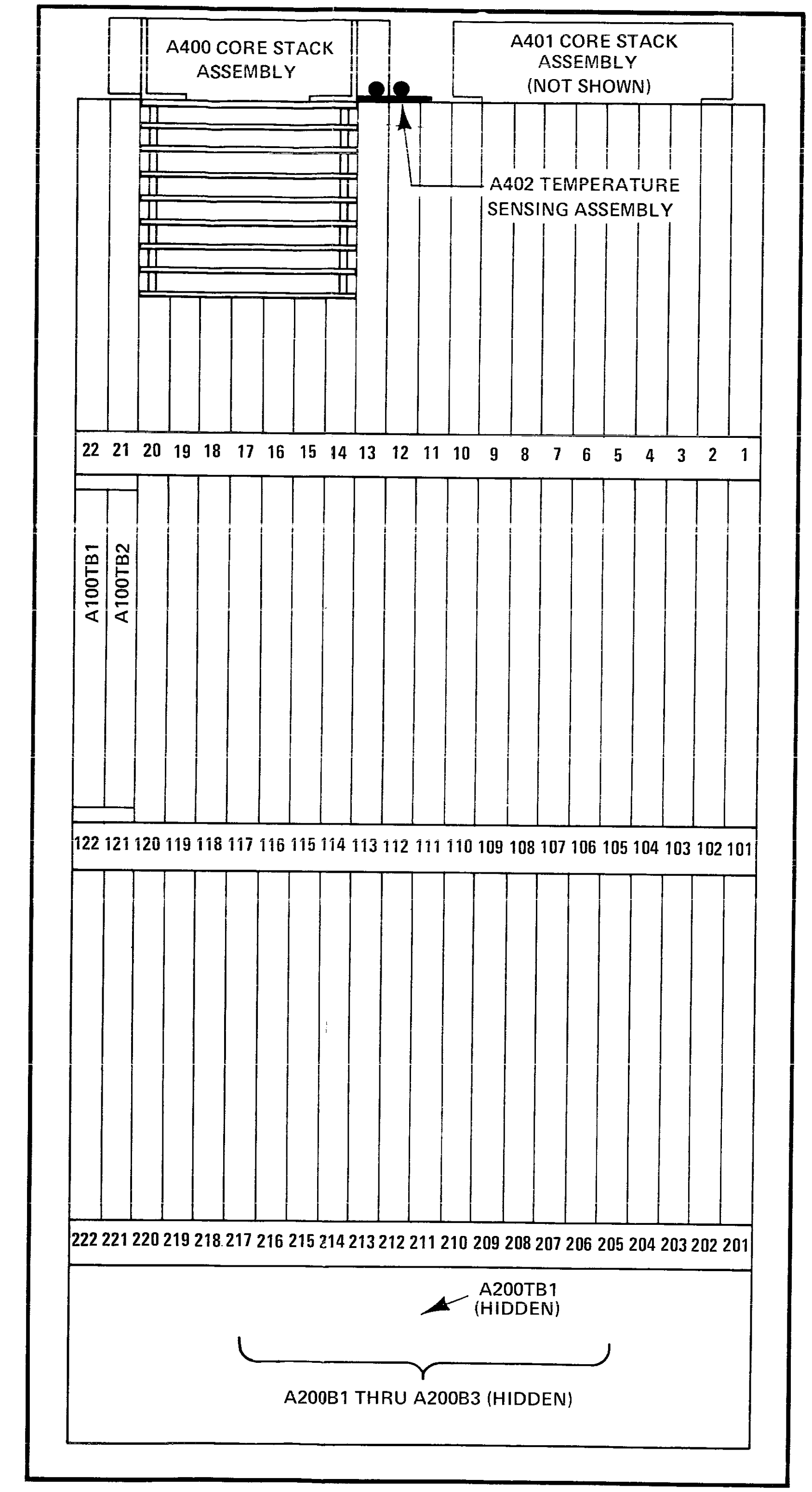

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Figure 5-6. Card-Cage Assembly, Rear View

Table 5-9. A1 Power Fail Interrupt Card (02116-6175), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 4, 5, C8 thru C10	0180-0155	Capacitor, Fxd, Elect, 2.2 μf, 20%, 20VDCW	56289	150D225X0020A2
C2, 3	0180-0097	Capacitor, Fxd, Elect, 47 μf, 10%, 35VDCW	28480	0180-0097
C6, 7	0180-0094	Capacitor, Fxd, Elect, 100 μf, 25VDCW	56289	30D107G025DH4
CR1, 2	1901-0191	Diode, Si, 100 PIV, 0.75A	28480	1901-0191
CR3, 5, 6	1901-0025	Diode, Si, 100 WV, 100 mA	28480	1901-0025
CR4	1902-0071	Diode Breakdown, 9.0V, 5%	28480	1902-0071
CR7	1902-0551	Diode Breakdown, 6.19V, 5%	28480	1902-0551
CR8	1902-3079	Diode Breakdown, Si, 4.53V	28480	1902-3079
CR9, 10	1901-0040	Diode, Si, 30 mA, 30WV	07263	FDG 1088
MC17, 27	1820-0956	Integrated Circuit, CTL	07263	SL 3459
MC25, 37, 47, 87	1820-0952	Integrated Circuit, CTL	07263	SL 3455
MC57	1820-0953	Integrated Circuit, CTL	07263	SL 3456
MC97	1820-0971	Integrated Circuit, CTL	07263	SL 3467
Q1	1854-0246	Transistor, Si, NPN	07263	2N3643
Q2 thru Q6, 8	1853-0036	Transistor, Si, PNP	04713	SP 3612
Q7	1854-0215	Transistor, Si, NPN	28480	1854-0215
R1, 19, 22	0698-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB 4715
R2	0683-3305	Resistor, Fxd, Comp, 33 ohms, 5%, 1/4w	01121	CB 3305
R3	0811-2084	Resistor, Fxd, WW, 43 ohms, 1%, 5w	28480	0811-2084
R4	0686-1515	Resistor, Fxd, Comp, 150 ohms, 5%, 1/2w	01121	EB 1515
R5	0811-0003	Resistor, Fxd, WW, 390 ohms, 1%, 1/4w	28480	0811-0003
R6	0757-0159	Resistor, Fxd, Flm, 1000 ohm, 1%, 1/2w	28480	0757-0159
R7	2100-1776	Resistor, Var, WW, 10k, 10%, 1/2w	28480	2100-1776
R8	0757-0839	Resistor, Fxd, Flm, 10k, 1%, 1/2w	28480	0757-0839
R9	0683-4725	Resistor, Fxd, Comp, 4700 ohms, 5%, 1/4w	01121	CB 4725
R10, 21, 25	0683-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4w	01121	CB 1015
R11	0757-0808	Resistor, Fxd, Flm, 301 ohms, 1%, 1/4w	28480	0757-0808
R12 thru R14	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4w	01121	CB 1025
R15	0683-1215	Resistor, Fxd, Comp, 120 ohms, 5%, 1/4w	01121	CB 1215
R16, 24	0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4w	01121	CB 5115
R17	0686-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/2w	28480	0686-2215
R18	0683-3315	Resistor, Fxd, Comp, 330 ohms, 5%, 1/4w	01121	CB 3315
R20	0757-0805	Resistor, Fxd, Flm, 221 ohms, 1%, 1/2w	28480	0757-0805
R23	0683-1005	Resistor, Fxd, Comp, 10 ohms, 5%, 1/2w	01121	CB 1005
R26	0698-3408	Resistor, Fxd, Flm, 2.15 k, 1%, 1/2w	28480	0698-3408
W2, 4	8159-0005	Jumper Wire	28480	8159-0005

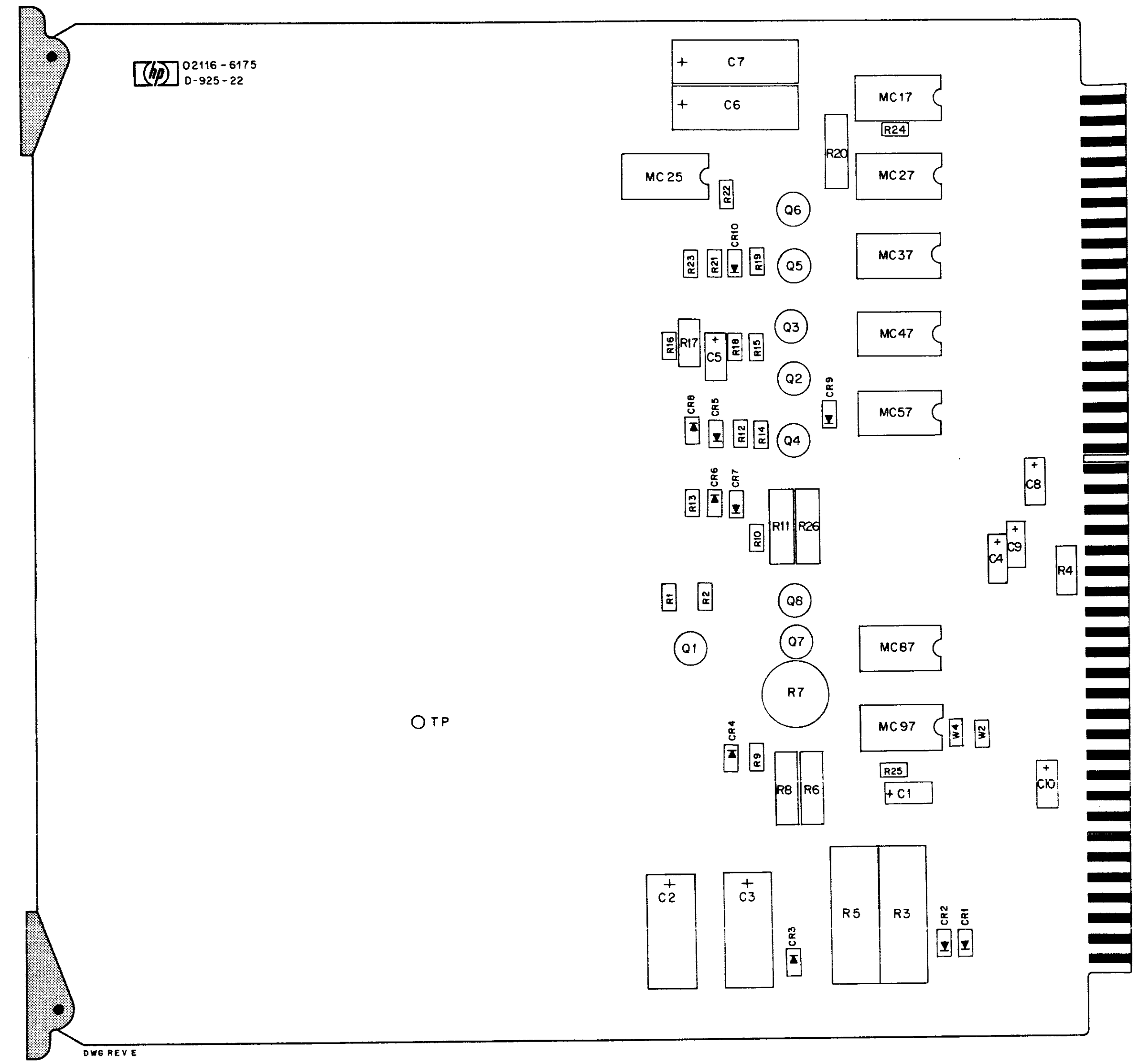
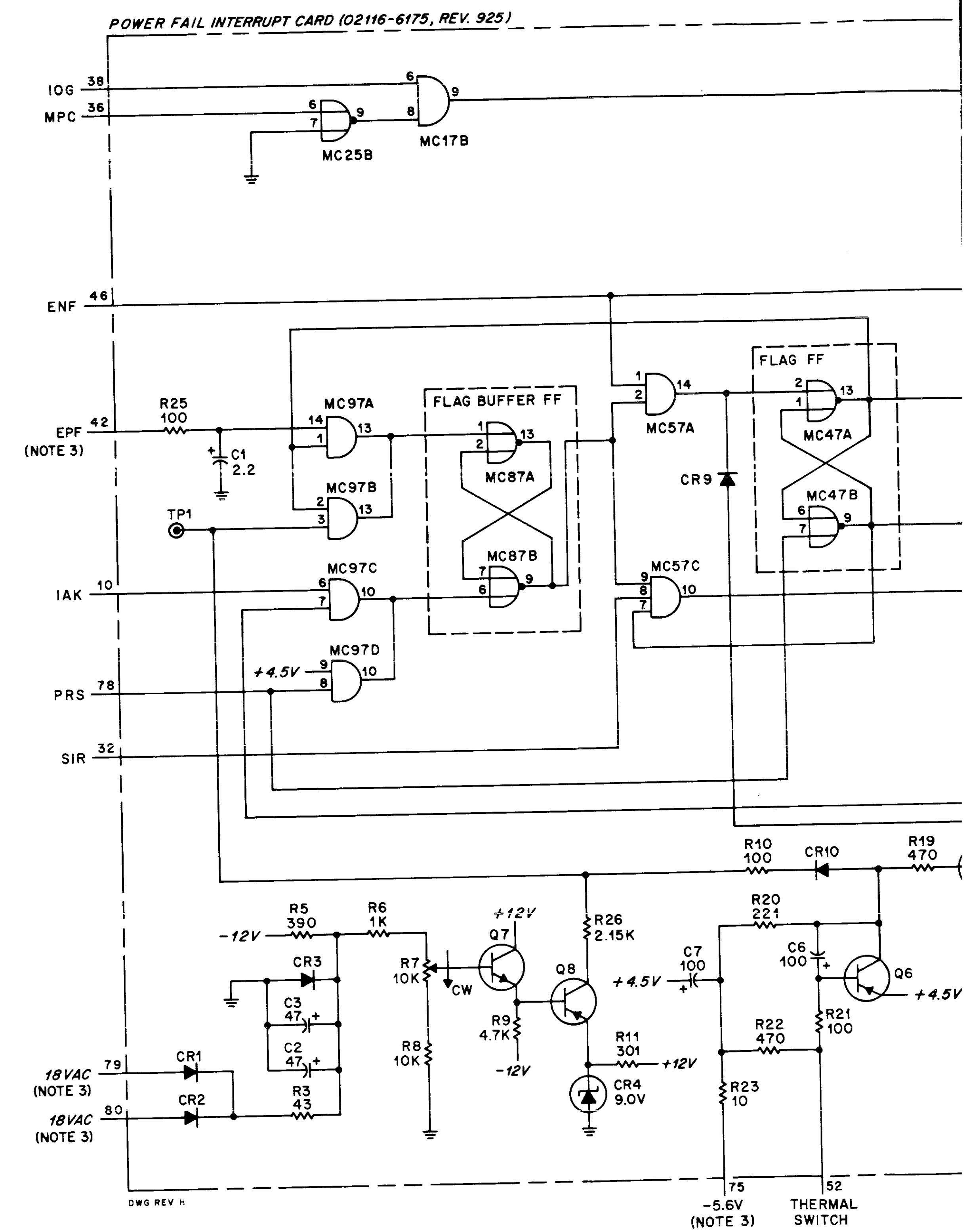


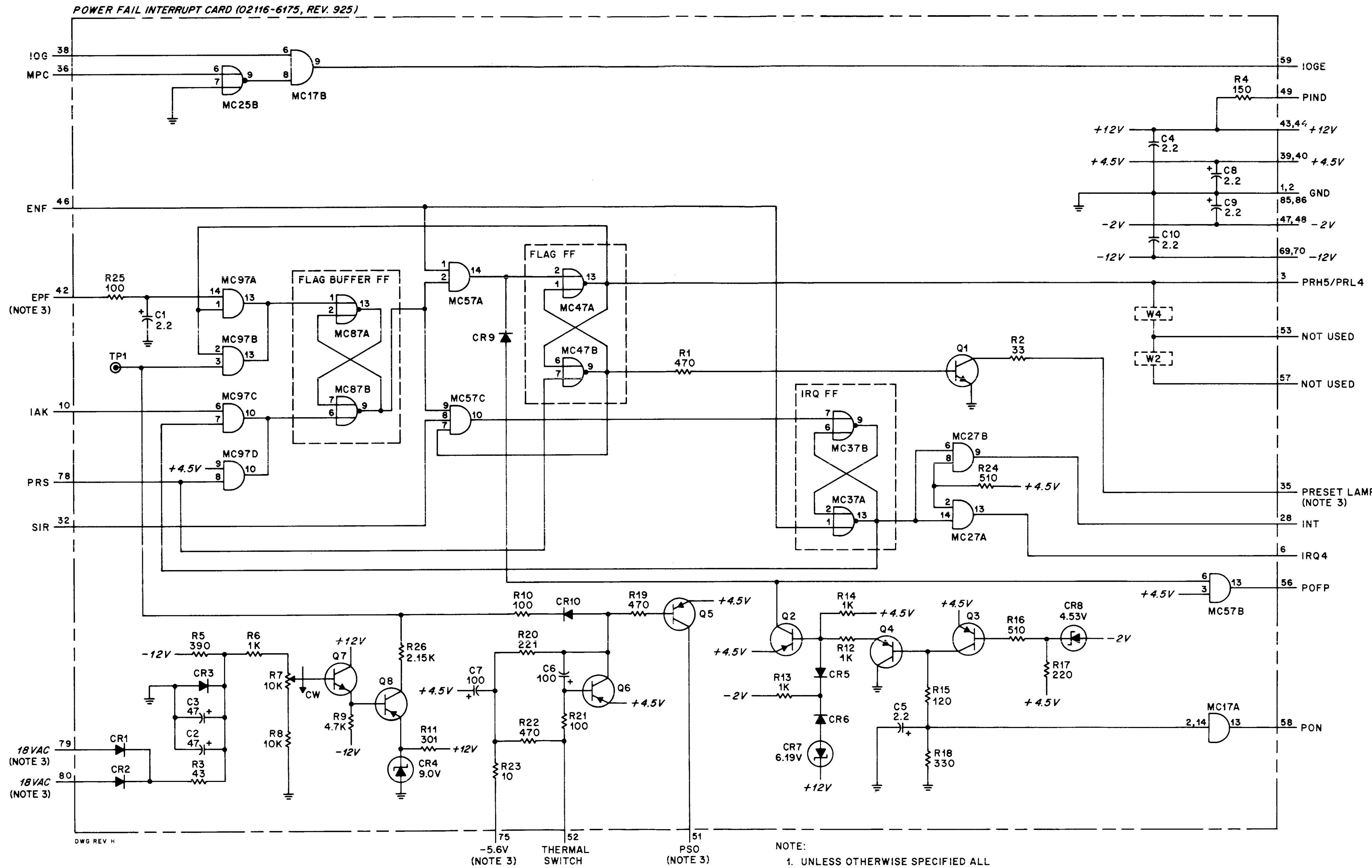
Figure 5-7. A1 Power Fail Interrupt Card (02116-6175) Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	SIGNAL	REF NO.
1	GND	219
2	GND	219
3	PRL4/	309
	PRL5	-
4,5	NC	-
6	IRQ 4	280
7	NC	-
8	NC	-
9	NC	-
10	IAK	246
11	NC	-
12	NC	-
13	NC	-
14	NC	-
15	NC	-
16	NC	-
17	NC	-
18	NC	-
19	NC	-
20	NC	-
21	NC	-
22	NC	-
23	NC	-
24	NC	-
25	NC	-
26	NC	-
27	NC	-
28	INT	257
29	NC	-
30	NC	-
31	NC	-
32	SIR	245
33	NC	-
34	NC	-
35	PRESET LAMP	480
36	MPC	412
37	NC	-
38	IOG	87
39	+4.5V	217
40	+4.5V	217
41	NC	-
42	EXT. PWR FAIL	482

PIN NO.	SIGNAL	REF NO.
43	+12V	1
44	+12V	1
45	NC	-
46	ENF	256
47	-2V	216
48	-2V	216
49	PIND	368
50	NC	-
51	PSO	483
52	THERM. SW	467
53	NC	-
54	NC	-
55	NC	-
56	POFP	354
57	NC	-
58	PON	353
59	IOGE	349
60	NC	-
61	NC	-
62	NC	-
63	NC	-
64	NC	-
65	NC	-
66	NC	-
67	NC	-
68	NC	-
69	-12V	2
70	-12V	2
71	NC	-
72	NC	-
73	NC	-
74	NC	-
75	-5.6V	369
76	NC	-
77	NC	-
78	PRS	355
79	18 VAC	479
80	18 VAC	479
81	NC	-
82	NC	-
83	NC	-
84	NC	-
85	GND	219
86	GND	219





NOTE:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
2. JUMPERS W2 AND W4 REMAIN IN PLACE IN 2116B AND 2116C.
3. REFER TO OVERALL INTERCONNECTION DIAGRAM FOR THESE CONNECTION.

Figure 5-8. A1 Power Fail Interrupt Card (02116-6175) Schematic Diagram

Table 5-10. A2 Memory Module Decoder Card (02116-6300), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 2, 3, 4	0180-0197	Capacitor, Fxd, Elect, 2.2 μf, 10%, 20VDCW	28480	0180-0197
C10	0160-2055	Capacitor, Fxd, Cer, 0.01 μf +80 -20%, 100 VDCW	56289	C023F101F103Z-E12CDH
MC13, 23, 33, 43, 87	1820-0187	Integrated Circuit, CTL	28480	1820-0187
MC15	1820-0953	Integrated Circuit, CTL	07263	SL 3456
MC25	1820-0954	Integrated Circuit, CTL	07263	SL 3457
MC27, 37, 47, 57	1820-0955	Integrated Circuit, CTL	07263	SL 3458
MC35, 45	1820-0964	Integrated Circuit, CTL	07263	SL 3461
MC77	1820-0375	Integrated Circuit, TTL	01295	SN 74H30N
R1 thru R7	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8w	28480	0757-0280
R10 thru R19	0757-0417	Resistor, Fxd, Flm, 562 ohms, 1%, 1/8w	28480	0757-0417
S1	3103-0004	Switch, Thermostat, 115V, 2A	28480	3103-0004

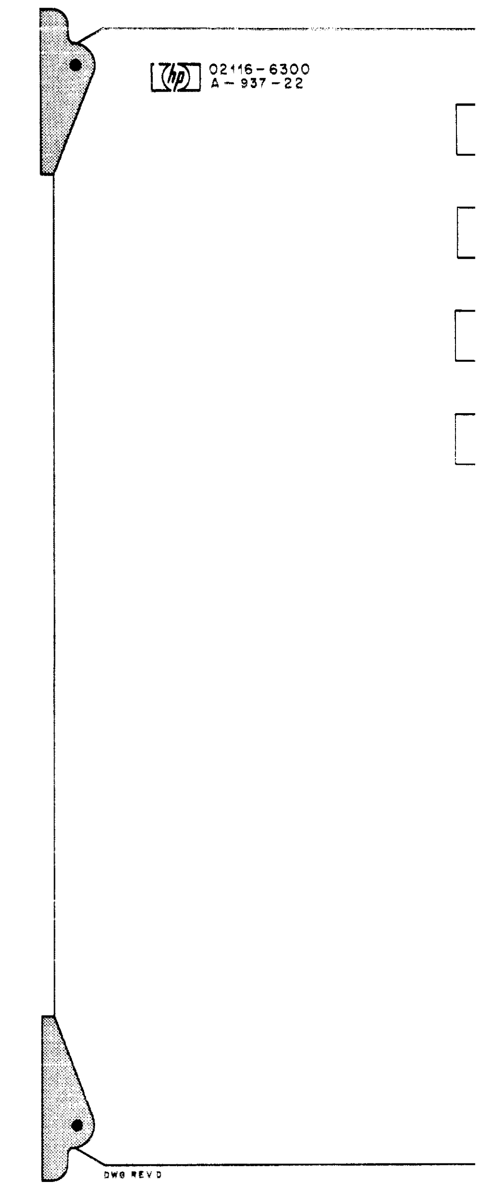


Figure 5-9.

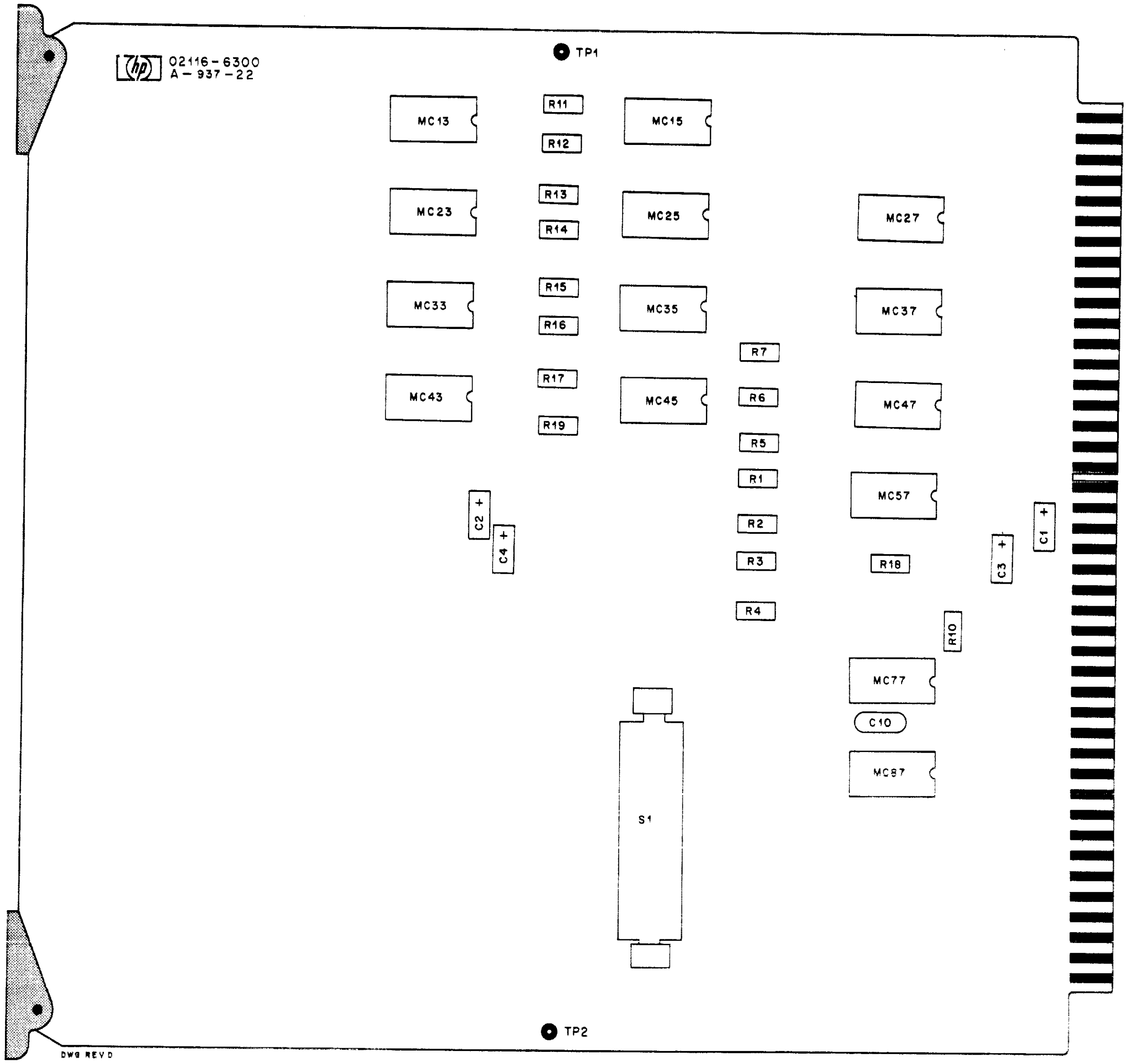
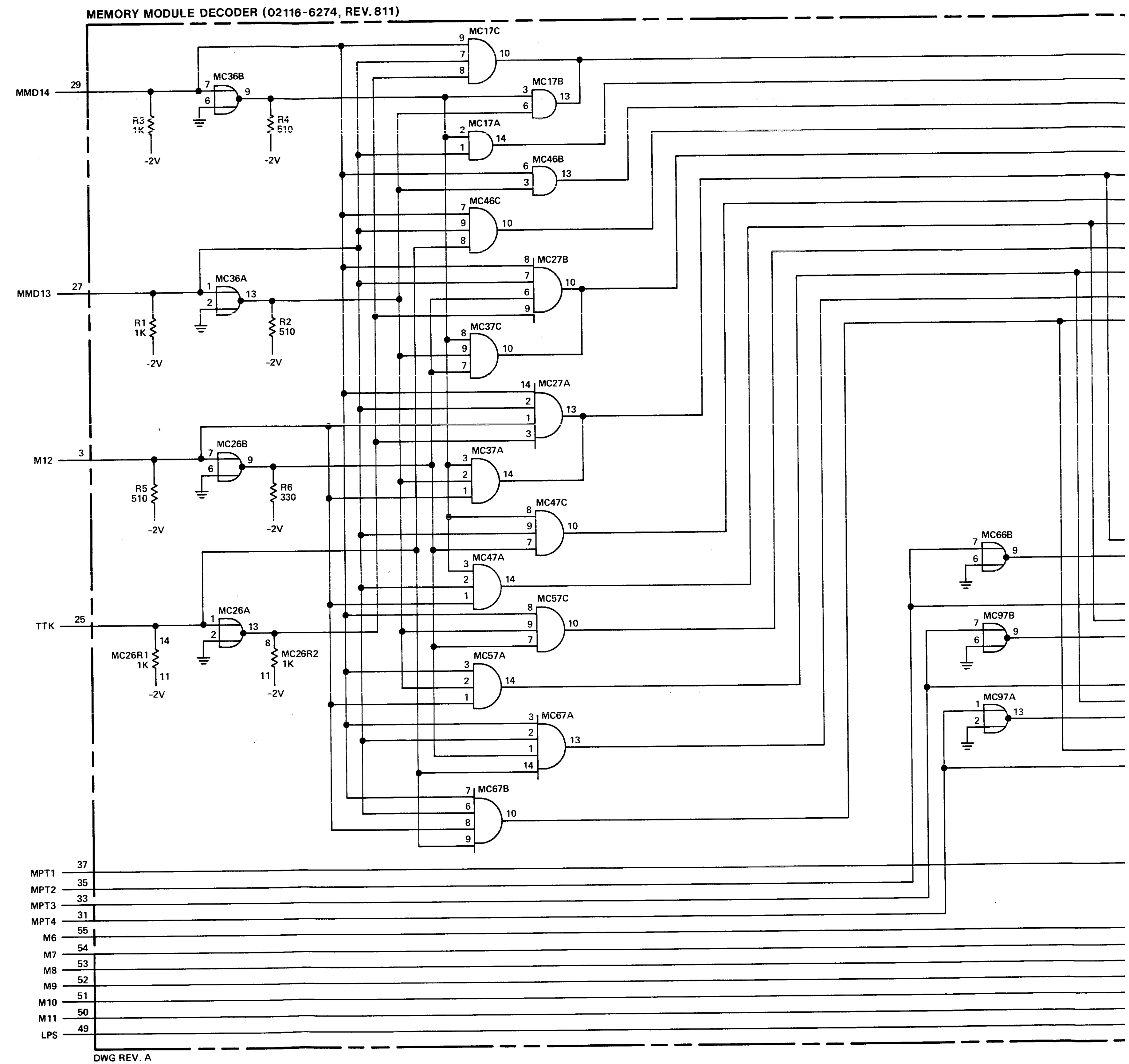


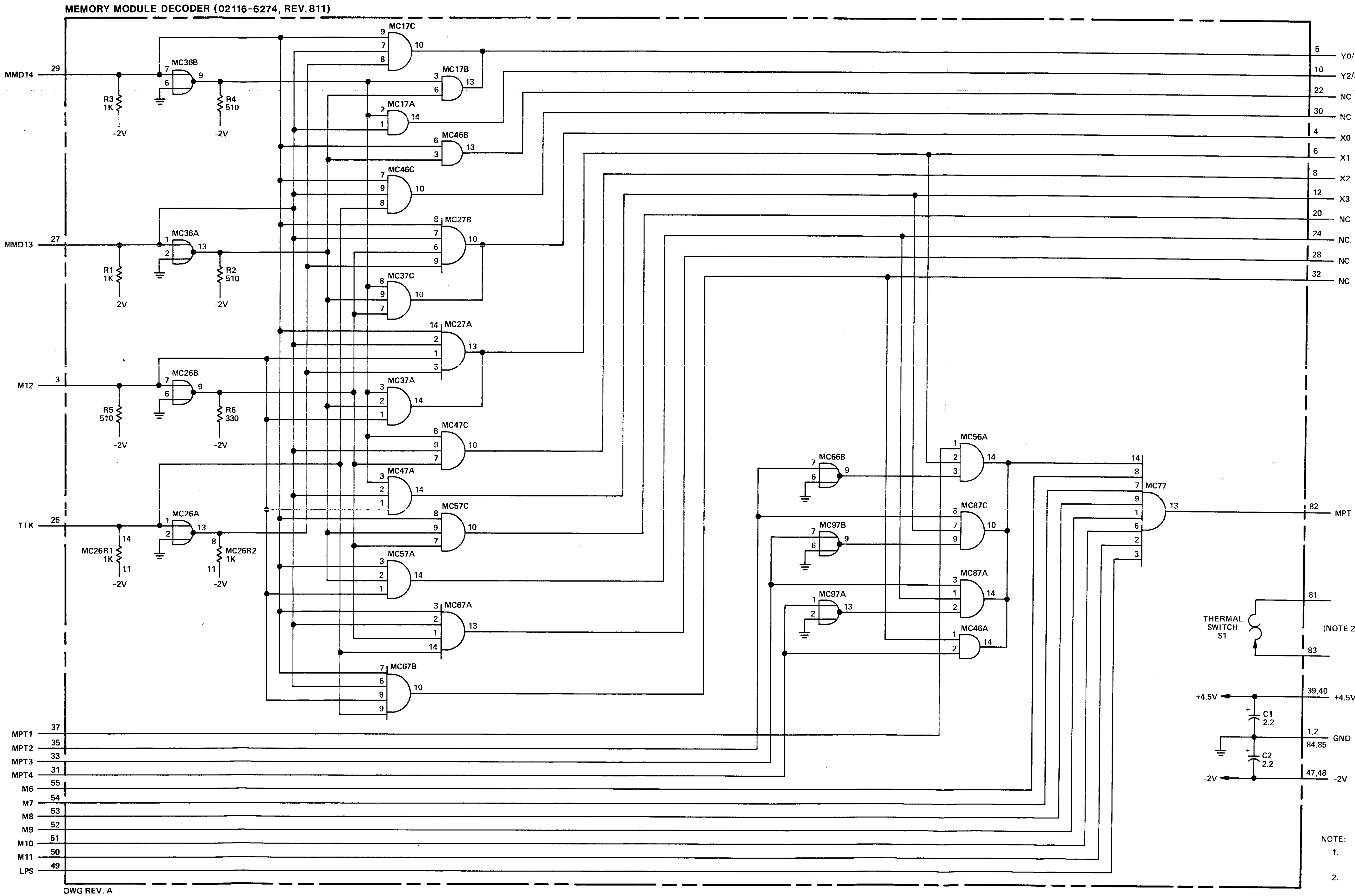
Figure 5-9. A2 Memory Module Decoder Card (02116-6300), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	SIGNAL	REF NO.
1	GND	219
2	GND	219
3	M12	18
4	X0	220
5	YO/1	224
6	X1	221
7	NC	-
8	X2	222
9	NC	-
10	Y2/3	225
11	NC	-
12	X3	223
13	NC	-
14	NC	-
15	NC	-
16	NC	-
17	NC	-
18	NC	-
19	NC	-
20	NC	-
21	NC	-
22	NC	-
23	NC	-
24	NC	-
25	TTK	470
26	NC	-
27	MMD13	457
28	NC	-
29	MMD14	474
30	NC	-
31	MPT4	478
32	NC	-
33	MPT3	477
34	NC	-
35	MPT2	464
36	NC	-
37	MPT1	463
38	NC	-
39	+4.5V	217
40	+4.5V	217
41	NC	-
42	NC	-
43	NC	-
44	NC	-

PIN NO.	SIGNAL	REF NO.
45	NC	-
46	NC	-
47	-2V	216
48	-2V	216
49	LPS	367
50	M11	17
51	M10	16
52	M9	15
53	M8	14
54	M7	13
55	M6	12
56	NC	-
57	NC	-
58	NC	-
59	NC	-
60	NC	-
61	NC	-
62	NC	-
63	NC	-
64	NC	-
65	NC	-
66	NC	-
67	NC	-
68	NC	-
69	NC	-
70	NC	-
71	NC	-
72	NC	-
73	NC	-
74	MNS	351
75	NC	-
76	$\overline{MNS}$	475
77	NC	-
78	$\overline{MPT}$	476
79	NC	-
80	NC	-
81	THERM. SW	467
82	MPT	226
83	THERM. SW	-
84	NC	-
85	GND	219
86	GND	219





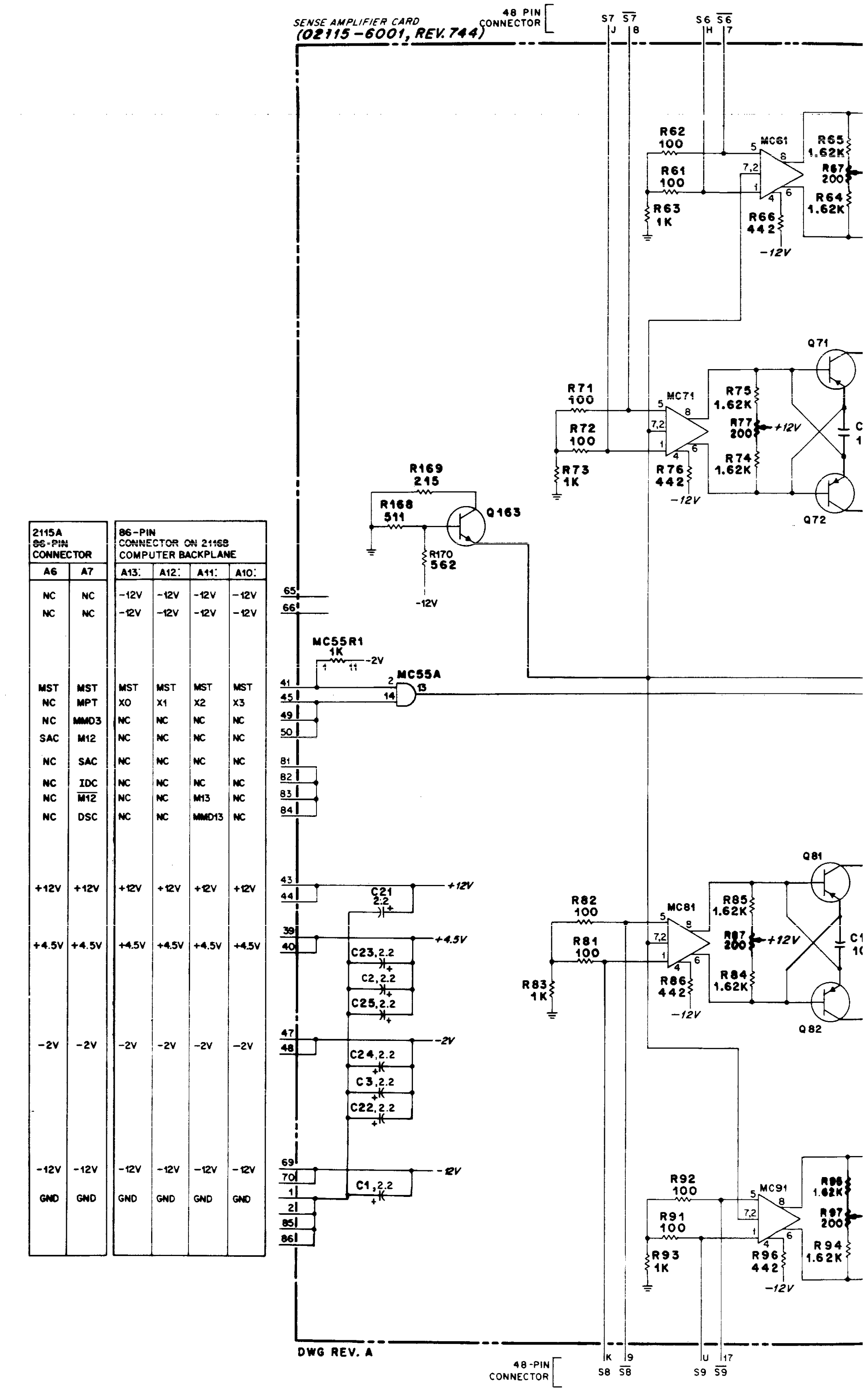
NOTE:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTANCES ARE IN OHMS ALL CAPACITANCES ARE IN MICROFARADS.
2. REFER TO OVERALL INTERCONNECTION DIAGRAM FOR CONNECTION.

Figure 5-9B. A2 Memory Module Decoder Card (02116-6274), Schematic Diagram

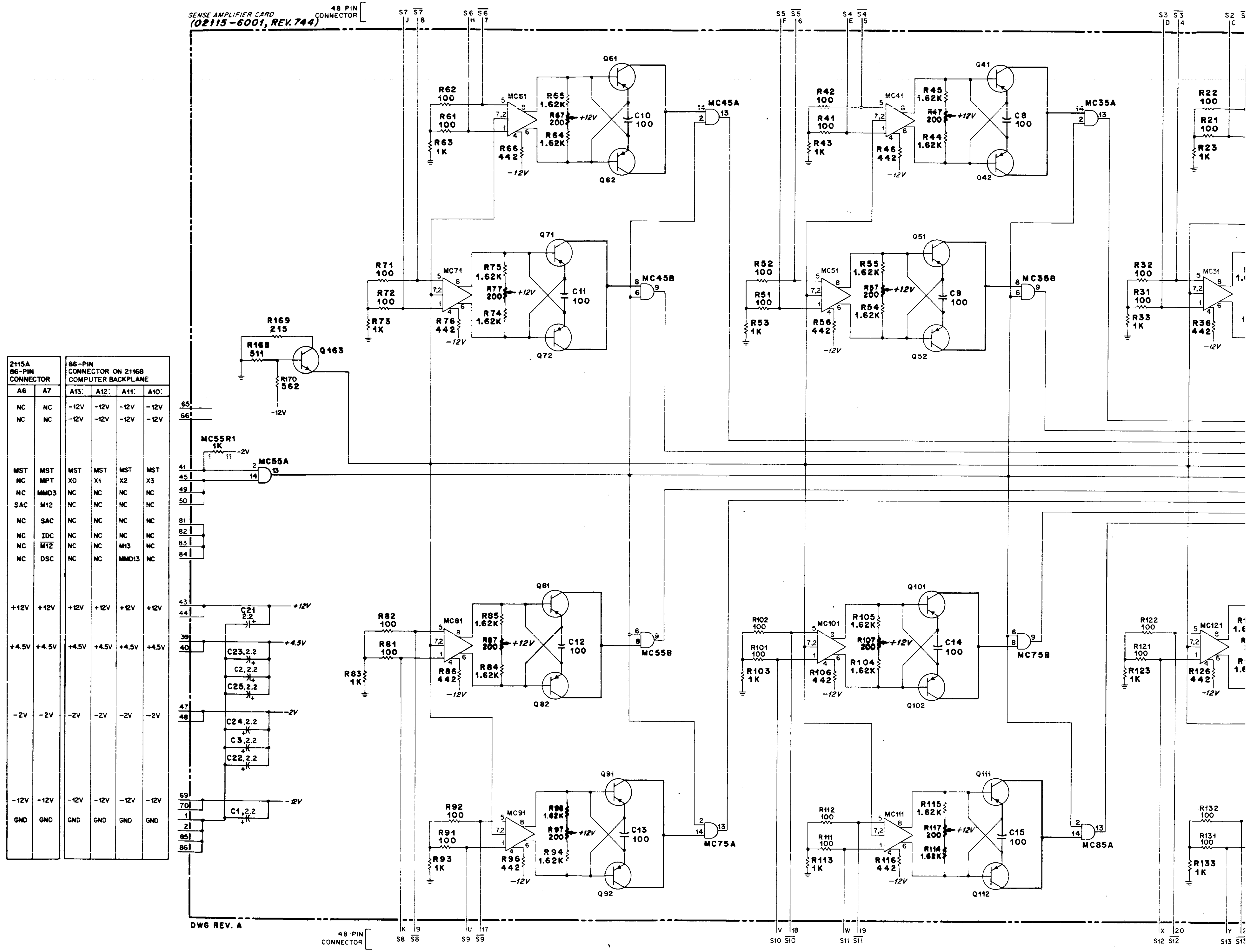
Pin Index (48 Pin Connector)

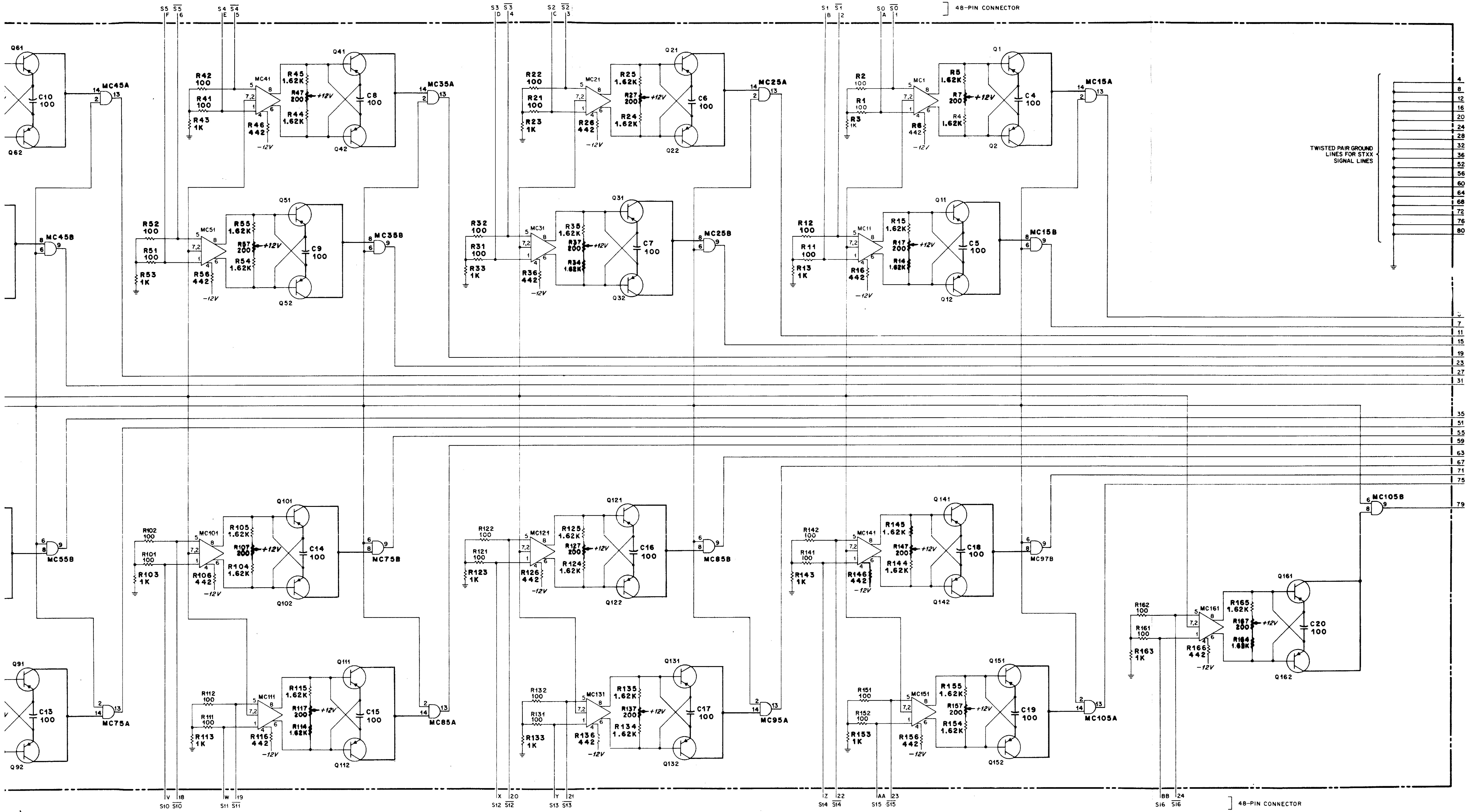
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	$\overline{S0}$	A	S0
2	$\overline{S1}$	B	S1
3	$\overline{S2}$	C	S2
4	$\overline{S3}$	D	S3
5	$\overline{S4}$	E	S4
6	$\overline{S5}$	F	S5
7	$\overline{S6}$	H	S6
8	$\overline{S7}$	J	S7
9	$\overline{S8}$	K	S8
10	NC	L	NC
11	NC	M	NC
12	NC	N	NC
13	NC	P	NC
14	NC	R	NC
15	NC	S	NC
16	NC	T	NC
17	$\overline{S9}$	U	S9
18	$\overline{S10}$	V	S10
19	$\overline{S11}$	W	S11
20	$\overline{S12}$	X	S12
21	$\overline{S13}$	Y	S13
22	$\overline{S14}$	Z	S14
23	$\overline{S15}$	AA	S15
24	$\overline{S16}$	BB	S16



(48 Pin Connector)

PIN NO.	SIGNAL
A	S0
B	S1
C	S2
D	S3
E	S4
F	S5
H	S6
J	S7
K	S8
L	NC
M	NC
N	NC
P	NC
R	NC
S	NC
T	NC
U	S9
V	S10
W	S11
X	S12
Y	S13
Z	S14
AA	S15
BB	S16





NOTES

1. UNLESS OTHERWISE S
RESISTANCES ARE IN
CAPACITANCES ARE IN

2. CONNECTIONS ARE TO
CONNECTOR AND APPL
REFERENCE DESIGNAT

3. NC DENOTES NO CONN

Figure 5-15B. A10, A11, A12,
Card (02115-600
(sheet 3 of 3)

Table 5-10A. A2 Memory Module Decoder Card (02116-6274), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,2	0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	28480	0180-0197
MC17,46	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC26,36,66,97	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC27,67	1820-0954	Integrated Circuit, CTL	07263	SL3457
MC37,47,56,57,87	1820-0964	Integrated Circuit, CTL	07263	SL3461
MC77	1820-0955	Integrated Circuit, CTL	07263	SL3458
R1,3	0683-1025	Resistor, Fxd, Comp, 1k, 5%, 1/4W	01121	CB1025
R2,4,5	0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4W	01121	CB5115
R6	0683-3315	Resistor, Fxd, Comp, 330 ohms, 5%, 1/4W	01121	CB3315
S1	3103-0004	Switch, Thermostat, 115V, 2A	28480	3103-0004

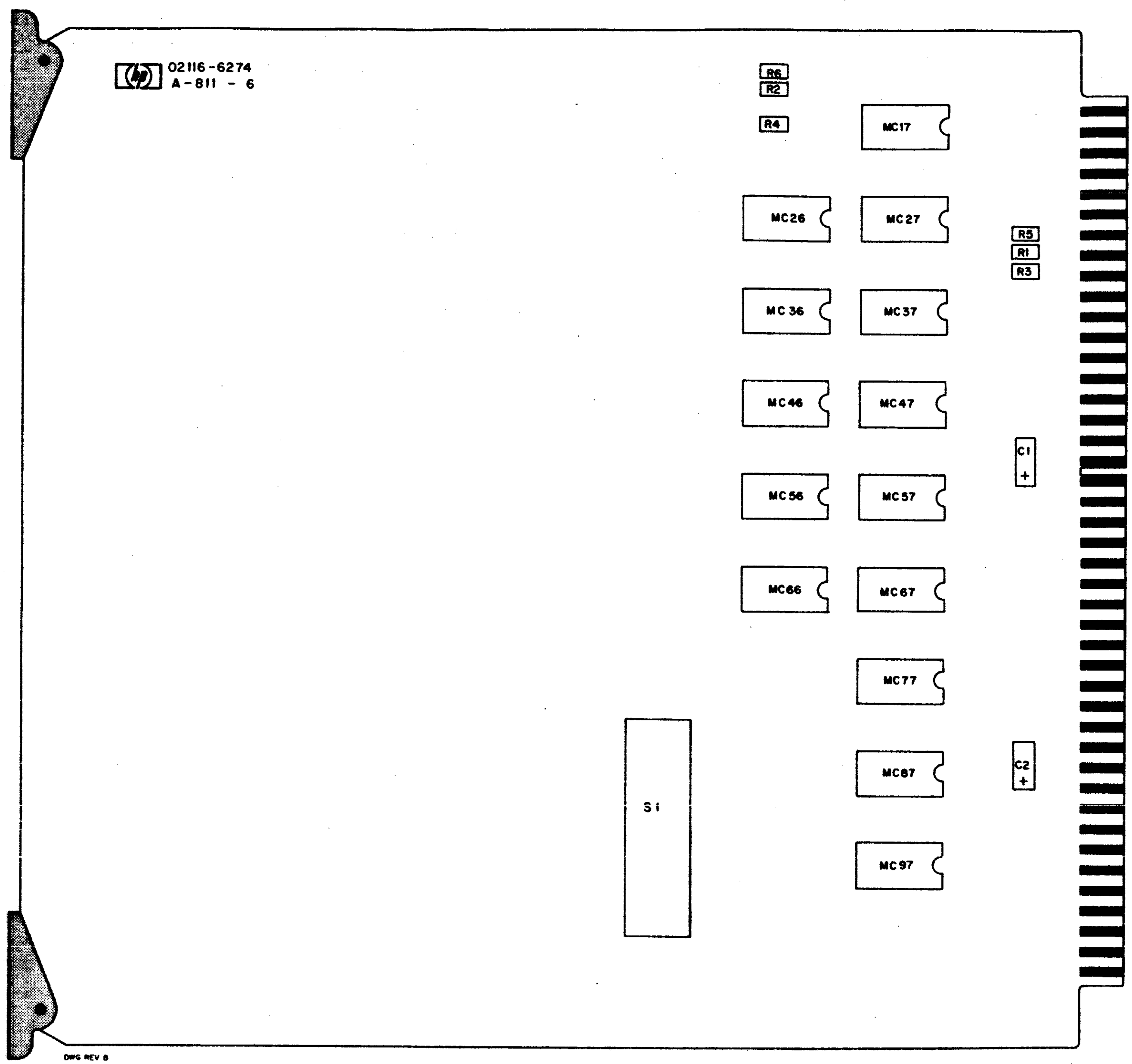
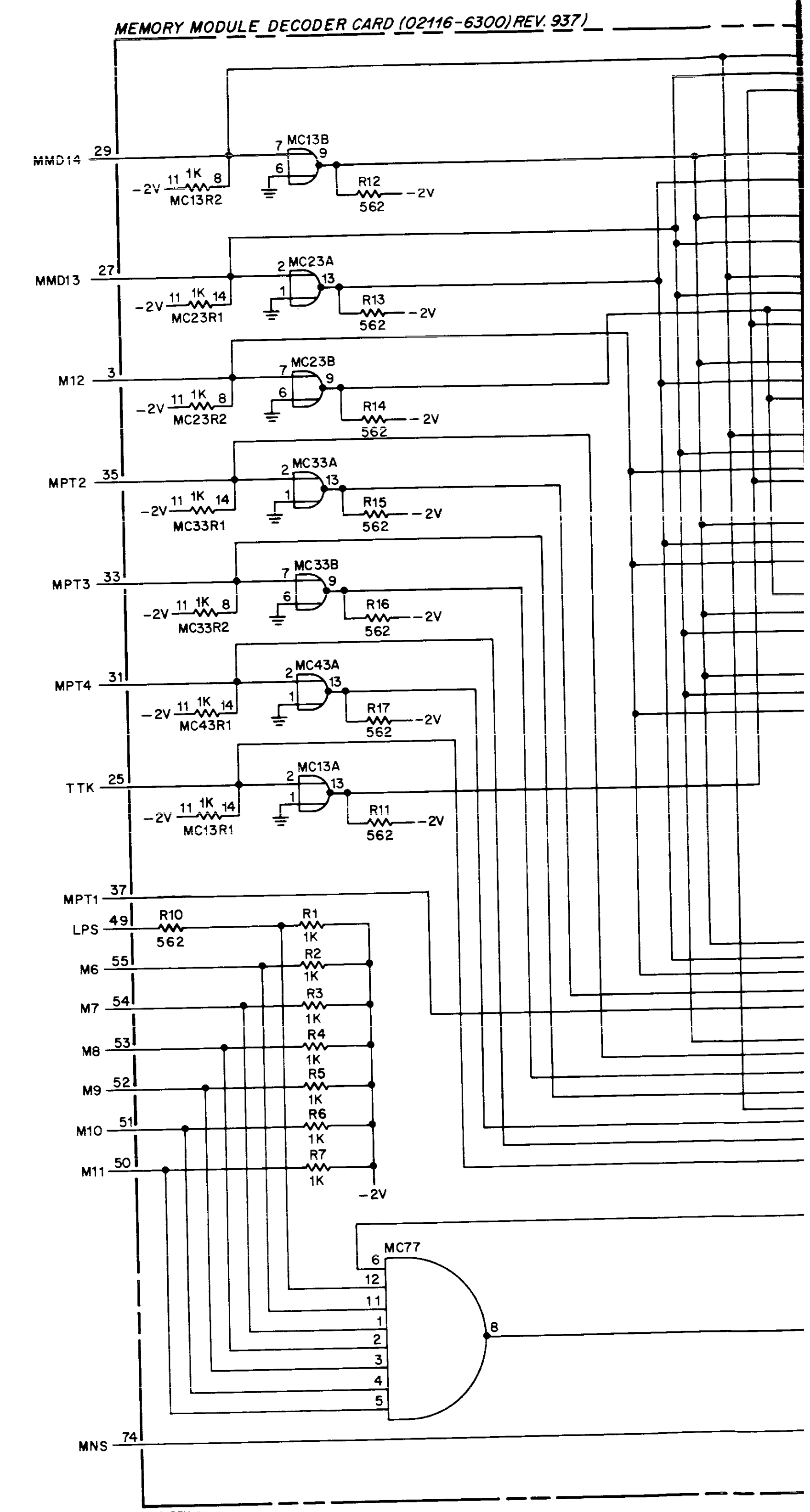


Figure 5-9A. A2 Memory Module Decoder Card (02116-6274), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	SIGNAL	REF NO.
1	GND	219
2	GND	219
3	M12	18
4	X0	220
5	YO/1	224
6	X1	221
7	NC	-
8	X2	222
9	NC	-
10	Y2/3	225
11	NC	-
12	X3	223
13	NC	-
14	NC	-
15	NC	-
16	NC	-
17	NC	-
18	NC	-
19	NC	-
20	NC	-
21	NC	-
22	NC	-
23	NC	-
24	NC	-
25	TTK	470
26	NC	-
27	MMD13	457
28	NC	-
29	MMD14	474
30	NC	-
31	MPT4	478
32	NC	-
33	MPT3	477
34	NC	-
35	MPT2	464
36	NC	-
37	MPT1	463
38	NC	-
39	+4.5V	217
40	+4.5V	217
41	NC	-
42	NC	-
43	NC	-
44	NC	-

PIN NO.	SIGNAL	REF NO.
45	NC	-
46	NC	-
47	-2V	216
48	-2V	216
49	LPS	367
50	M11	17
51	M10	16
52	M9	15
53	M8	14
54	M7	13
55	M6	12
56	NC	-
57	NC	-
58	NC	-
59	NC	-
60	NC	-
61	NC	-
62	NC	-
63	NC	-
64	NC	-
65	NC	-
66	NC	-
67	NC	-
68	NC	-
69	NC	-
70	NC	-
71	NC	-
72	NC	-
73	NC	-
74	MNS	351
75	NC	-
76	$\overline{\text{MNS}}$	475
77	NC	-
78	$\overline{\text{MPT}}$	476
79	NC	-
80	NC	-
81	THERM. SW	467
82	MPT	226
83	THERM. SW	-
84	NC	-
85	GND	219
86	GND	219



NOTE:
1. UNLESS OTHERWISE NOTED – ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
2. REFER TO OVERALL INTERCONNECTION DIAGRAM FOR CONNECTION.

(86 Pin Connector)

PIN NO.	SIGNAL	REF NO.
45	NC	-
46	NC	-
47	-2V	216
48	-2V	216
49	LPS	367
50	M11	17
51	M10	16
52	M9	15
53	M8	14
54	M7	13
55	M6	12
56	NC	-
57	NC	-
58	NC	-
59	NC	-
60	NC	-
61	NC	-
62	NC	-
63	NC	-
64	NC	-
65	NC	-
66	NC	-
67	NC	-
68	NC	-
69	NC	-
70	NC	-
71	NC	-
72	NC	-
73	NC	-
74	MNS	351
75	NC	-
76	$\overline{\text{MNS}}$	475
77	NC	-
78	$\overline{\text{MPT}}$	476
79	NC	-
80	NC	-
81	THERM. SW	467
82	MPT	226
83	THERM. SW	-
84	NC	-
85	GND	219
86	GND	219

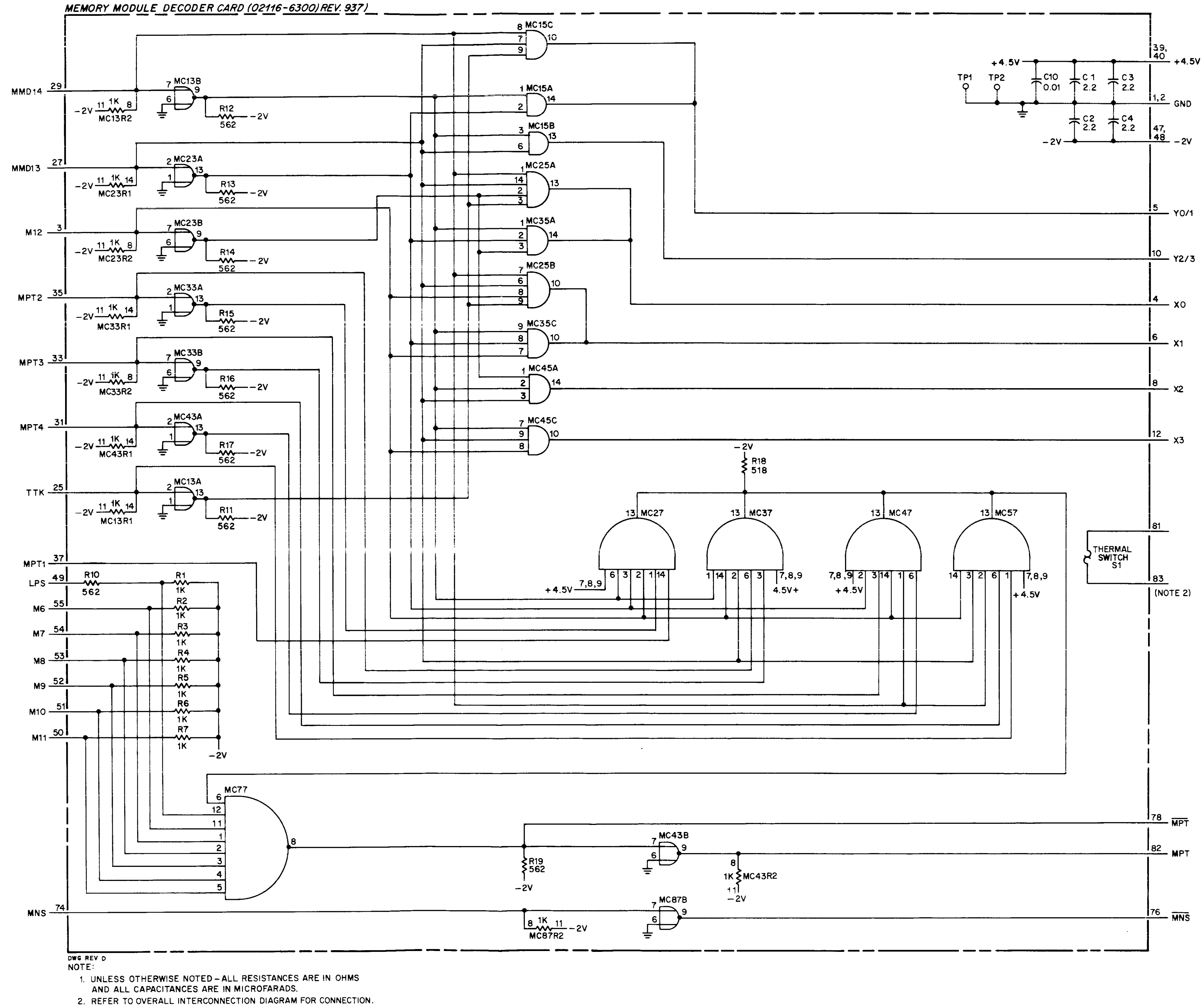


Figure 5-10. A2 Memory Module Decoder Card (02116-6300), Schematic Diagram

Table 5-11. A4, A6, A16, A18 Inhibit Driver Card (02116-6265), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1	0140-0208	Capacitor, Fxd, Mica, 680 pf, 5%	28480	0140-0208
C2 thru C5	0180-0141	Capacitor, Fxd, Elect, 50 μf, +75 -10%, 5VDCW	28480	0180-0141
C6 thru C9	0180-0155	Capacitor, Fxd, Elect, 2.2 μf, 20%, 20VDCW	56289	150D225X0020A2
CR1 thru CR17	1901-0050	Diode, Si, 75V	28480	1901-0050
MC17, 27, 37, 47, 57, 67, 77, 87, 97, 107	1820-0127	Integrated Circuit, TTL	07263	V6A900359X
Q1, 4, 7, 10, 13, 16, 19, 22, 25, 30, 33, 36, 39, 42, 45, 48, 51	1854-0094	Transistor, Si, NPN	07263	2N3646
Q2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18, 20, 21, 23, 24, 26, 27, 28, 29, 31, 32, 34, 35, 37, 38, 40, 41, 43, 44, 46, 47, 49, 50	1854-0255	Transistor, Si, NPN	07263	2N3642
R1 thru R3, R72 thru R80, 82	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4w	01121	CB1025
R4, 8, 12, 16, 20, 24, 28, 32, 36, 43, 47, 51, 55, 59, 63, 67, 71	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB4715
R5, 7, 9, 11, 13, 15, 17 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70	0811-2614	Resistor, Fxd, WW, 37 ohms, 1%, 5w	28480	0811-2614
R6, 10, 14, 18, 22, 26, 30, 34, 38, 41, 45, 49, 53, 57, 61, 65, 69	0683-2205	Resistor, Fxd, Comp, 22 ohms, 5%, 1/4w	01121	CB2205
R81	0698-3441	Resistor, Fxd, Flm, 215 ohms, 1%, 1/8w	28480	0698-3441

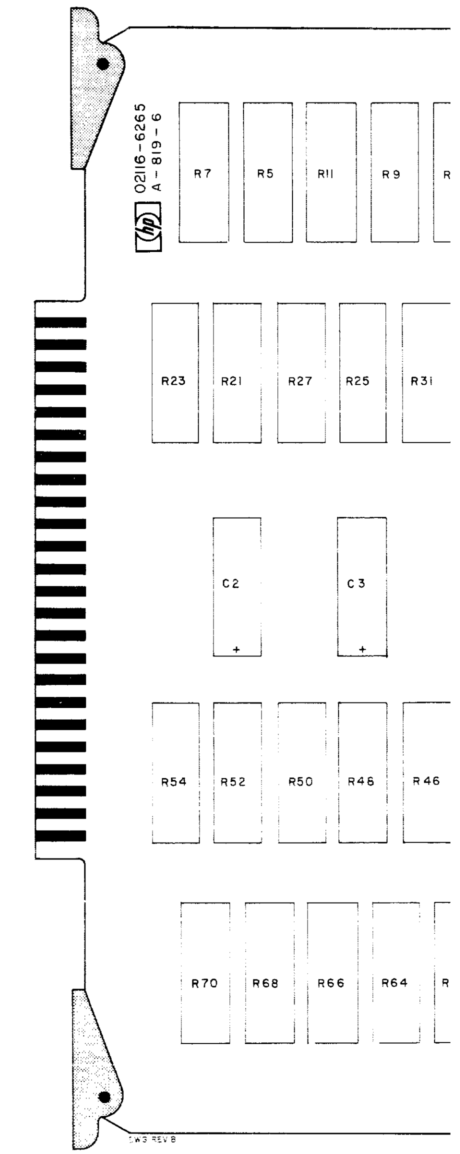


Figure 5-11. A4, A6, A16, ar

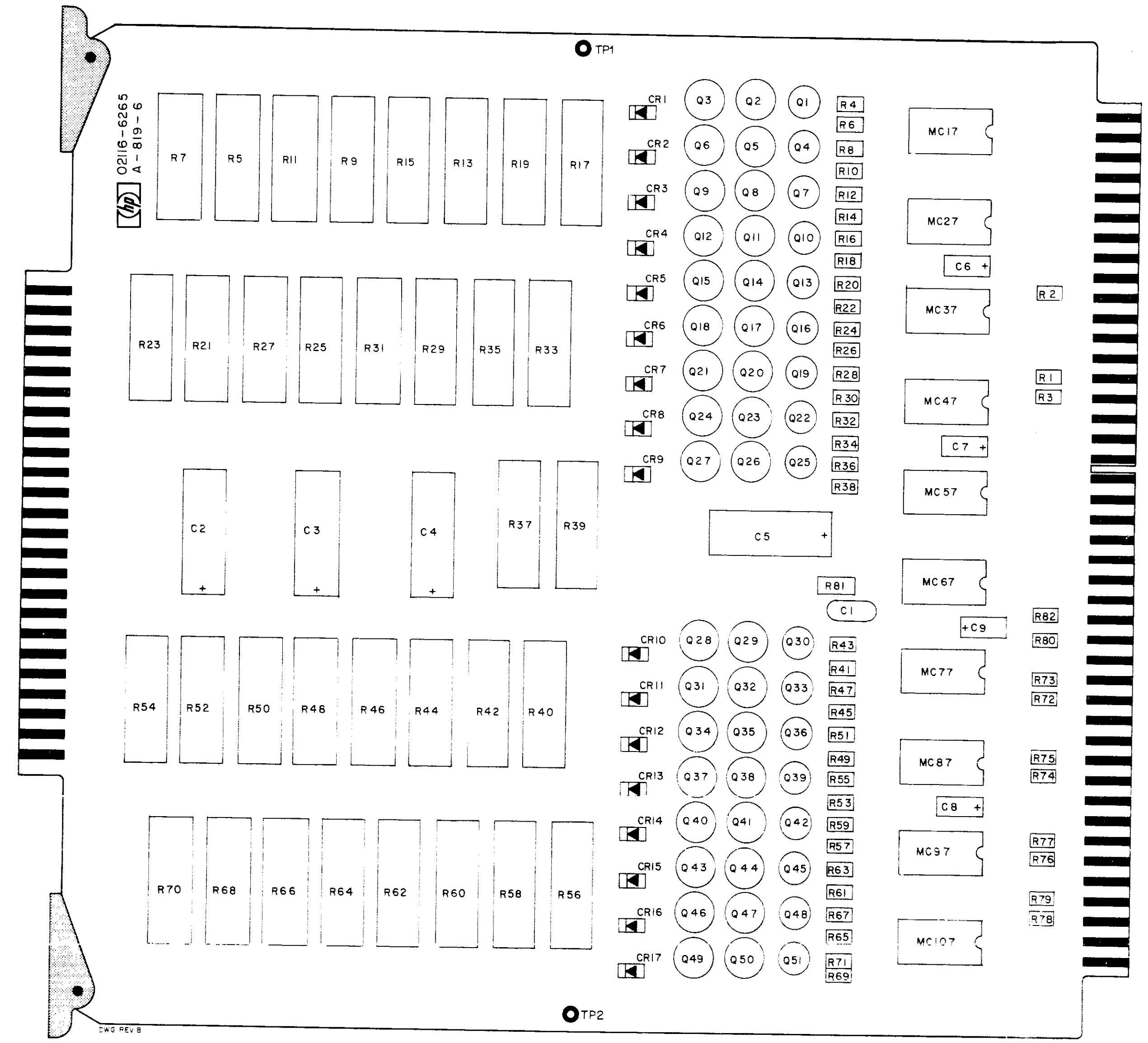


Figure 5-11. A4, A6, A16, and A19 Inhibit Driver Card (02116-6265), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	A4 SIGNAL	A4 REF NO.	A6 SIGNAL	A6 REF NO.	A16 SIGNAL	A16 REF NO.	A18 SIGNAL	A18 REF NO.
1	GND	219	GND	219	GND	219	GND	219
2	GND	219	GND	219	GND	219	GND	219
3	NC	-	NC	-	NC	-	NC	-
4	$\overline{TR1}$	133	$\overline{TR1}$	133	$\overline{TR1}$	133	$\overline{TR1}$	133
5	NC	-	NC	-	NC	-	NC	-
6	$\overline{TR0}$	138	$\overline{TR0}$	138	$\overline{TR0}$	138	$\overline{TR0}$	138
7	NC	-	NC	-	NC	-	NC	-
8	$\overline{TR3}$	126	$\overline{TR3}$	126	$\overline{TR3}$	126	$\overline{TR3}$	126
9	NC	-	NC	-	NC	-	NC	-
10	NC	-	NC	-	NC	-	NC	-
11	NC	-	NC	-	NC	-	NC	-
12	$\overline{TR5}$	151	$\overline{TR5}$	151	$\overline{TR5}$	151	$\overline{TR5}$	151
13	NC	-	NC	-	NC	-	NC	-
14	$\overline{TR2}$	130	$\overline{TR2}$	130	$\overline{TR2}$	130	$\overline{TR2}$	130
15	NC	-	NC	-	NC	-	NC	-
16	NC	-	NC	-	NC	-	NC	-
17	NC	-	NC	-	NC	-	NC	-
18	NC	-	NC	-	NC	-	NC	-
19	NC	-	NC	-	NC	-	NC	-
20	$\overline{TR7}$	144	$\overline{TR7}$	144	$\overline{TR7}$	144	$\overline{TR7}$	144
21	NC	-	NC	-	NC	-	NC	-
22	$\overline{TR4}$	156	$\overline{TR4}$	156	$\overline{TR4}$	156	$\overline{TR4}$	156
23	NC	-	NC	-	NC	-	NC	-
24	NC	-	NC	-	NC	-	NC	-
25	NC	-	NC	-	NC	-	NC	-
26	NC	-	NC	-	NC	-	NC	-
27	NC	-	NC	-	NC	-	NC	-
28	$\overline{TR6}$	148	$\overline{TR6}$	148	$\overline{TR6}$	148	$\overline{TR6}$	148
29	NC	-	NC	-	NC	-	NC	-
30	$\overline{TR8}$	173	$\overline{TR8}$	173	$\overline{TR8}$	173	$\overline{TR8}$	173
31	NC	-	NC	-	NC	-	NC	-
32	NC	-	NC	-	NC	-	NC	-
33	NC	-	NC	-	NC	-	NC	-
34	NC	-	NC	-	NC	-	NC	-
35	NC	-	NC	-	NC	-	NC	-
36	NC	-	NC	-	NC	-	NC	-
37	NC	-	NC	-	NC	-	NC	-
38	NC	-	NC	-	NC	-	NC	-
39	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
40	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
41	NC	-	NC	-	NC	-	NC	-
42	NC	-	NC	-	NC	-	NC	-
43	+32V	5	+32V	5	+32V	5	+32V	5
44	+32V	5	+32V	5	+32V	5	+32V	5
45	NC	-	NC	-	NC	-	NC	-
46	NC	-	NC	-	NC	-	NC	-
47	-2V	216	-2V	216	-2V	216	-2V	216
48	-2V	216	-2V	216	-2V	216	-2V	216

Figure 5-12. A4, A6, A16, and A18 Inhibit Driver Card (02116-6265), Schematic Diagram (Sheet 1 of 3)

Pin Index (86-Pin Connector)

PIN NO.	A4 SIGNAL	A4 REF NO.	A6 SIGNAL	A6 REF NO.	A16 SIGNAL	A16 REF NO.	A18 SIGNAL	A18 REF NO.
49	NC	-	NC	-	NC	-	NC	-
50	NC	-	NC	-	NC	-	NC	-
51	NC	-	NC	-	NC	-	NC	-
52	X3	223	X2	222	X1	221	X0	220
53	NC	-	NC	-	NC	-	NC	-
54	MIT	92	MIT	92	MIT	92	MIT	92
55	NC	-	NC	-	NC	-	NC	-
56	NC	-	NC	-	NC	-	NC	-
57	NC	-	NC	-	NC	-	NC	-
58	$\overline{\text{TR10}}$	165	$\overline{\text{TR10}}$	165	$\overline{\text{TR10}}$	165	$\overline{\text{TR10}}$	165
59	NC	-	NC	-	NC	-	NC	-
60	$\overline{\text{TR9}}$	168	$\overline{\text{TR9}}$	168	$\overline{\text{TR9}}$	168	$\overline{\text{TR9}}$	168
61	NC	-	NC	-	NC	-	NC	-
62	NC	-	NC	-	NC	-	NC	-
63	NC	-	NC	-	NC	-	NC	-
64	NC	-	NC	-	NC	-	NC	-
65	NC	-	NC	-	NC	-	NC	-
66	$\overline{\text{TR12}}$	190	$\overline{\text{TR12}}$	190	$\overline{\text{TR12}}$	190	$\overline{\text{TR12}}$	190
67	NC	-	NC	-	NC	-	NC	-
68	$\overline{\text{TR11}}$	161	$\overline{\text{TR11}}$	161	$\overline{\text{TR11}}$	161	$\overline{\text{TR11}}$	161
69	NC	-	NC	-	NC	-	NC	-
70	NC	-	NC	-	NC	-	NC	-
71	NC	-	NC	-	NC	-	NC	-
72	NC	-	NC	-	NC	-	NC	-
73	NC	-	NC	-	NC	-	NC	-
74	$\overline{\text{TR14}}$	182	$\overline{\text{TR14}}$	182	$\overline{\text{TR14}}$	182	$\overline{\text{TR14}}$	182
75	NC	-	NC	-	NC	-	NC	-
76	$\overline{\text{TR13}}$	185	$\overline{\text{TR13}}$	185	$\overline{\text{TR13}}$	185	$\overline{\text{TR13}}$	185
77	NC	-	NC	-	NC	-	NC	-
78	NC	-	NC	-	NC	-	NC	-
79	NC	-	NC	-	NC	-	NC	-
80	$\overline{\text{TR16}}$	458	$\overline{\text{TR16}}$	458	$\overline{\text{TR16}}$	458	$\overline{\text{TR16}}$	458
81	NC	-	MPT2	464	NC	-	MPT1	463
82	$\overline{\text{TR15}}$	179	$\overline{\text{TR15}}$	179	$\overline{\text{TR15}}$	179	$\overline{\text{TR15}}$	179
83	NC	-	MPT1	463	NC	-	MPT0	462
84	NC	-	NC	-	NC	-	NC	-
85	GND	219	GND	219	GND	219	GND	219
86	GND	219	GND	219	GND	219	GND	219

Figure 5-12. A4, A6, A16, and A18 Inhibit Driver Card (02116-6265), Schematic Diagram (Sheet 2 of 3)

Table 5-12. A8, A9, A14, A15 Driver/Switch Card (02116-6266), Reference Designation Index

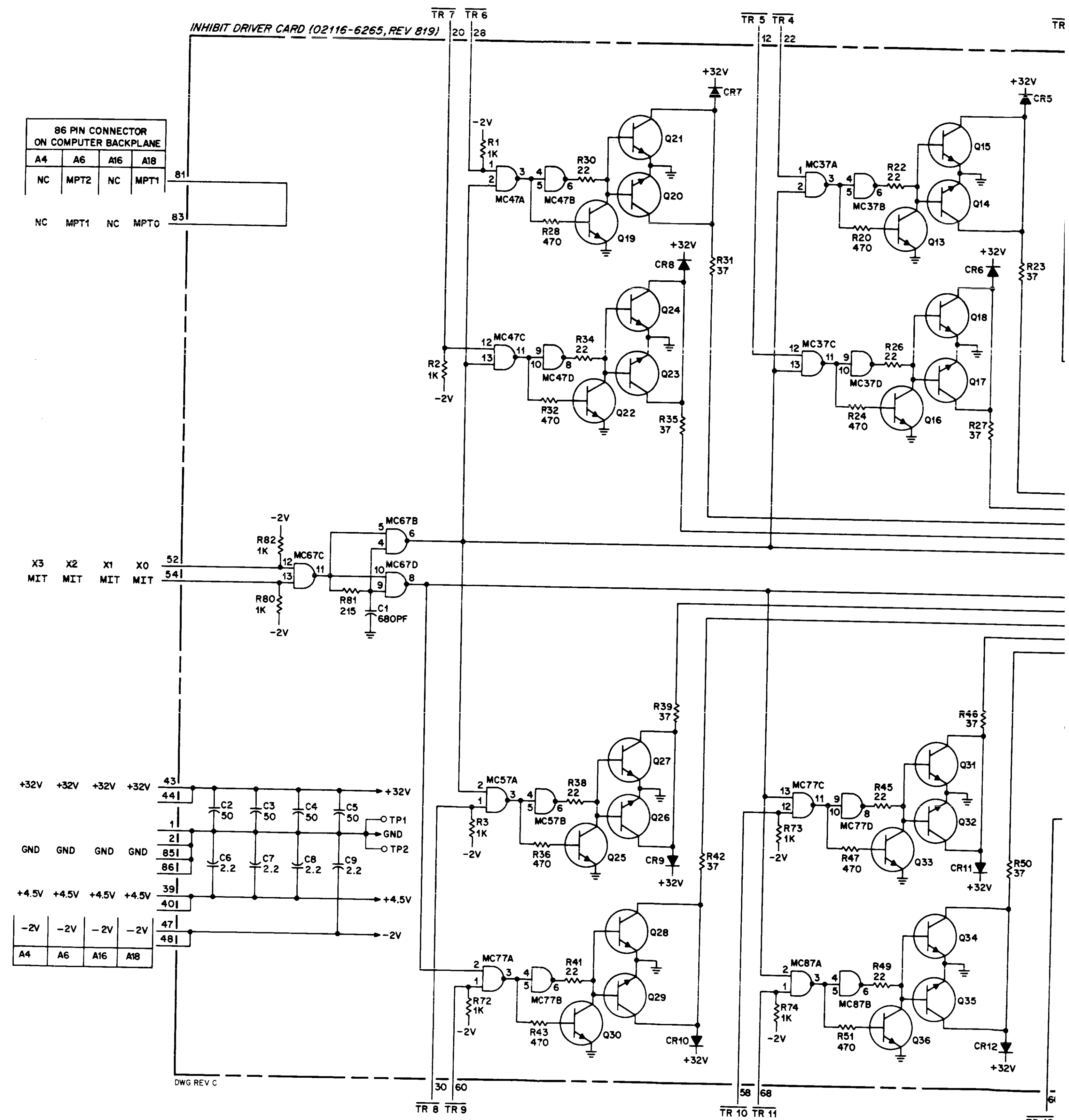
REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 3, 5, 7, 9, 11, 13, 15	0160-0154	Capacitor, Fxd, My, 0.0022 μf, 10%, 200VDCW	56289	192P22292-PTS
C2, 4, 6, 8, 10, 12, 14, 16	0160-0153	Capacitor, Fxd, My, 0.001 μf, 10%, 200VDCW	56289	192P10292-PTS
C17, 18	0160-0168	Capacitor, Fxd, My, 0.1 μf, 10%, 200VDCW	28480	0160-0168
C19, 20	0180-0049	Capacitor, Fxd, Elect, 20 μf, 50VDCW	56289	30D206G050-DC6M1
C21, 22	0140-0151	Capacitor, Fxd, Mica, 820 pf, 2%	28480	0140-0151
C23, 24, 41, 42, 43	0180-0155	Capacitor, Fxd, Elect, 2.2 μf, 20%, 20VDCW	28480	0180-0155
C25 thru C40	0160-2055	Capacitor, Fxd, Cer, 0.01 μf, +80 -20%, 100VDCW	56289	C023F101F103-ZE12CDH
C44, 45	0180-1735	Capacitor, Fxd, Elect, 0.22 μf, 10%, 35VDCW	28480	0180-1735
CR1 thru CR16, 18, 21, 24, 27, 30, 33, 36, 39	1901-0040	Diode, Si, 30 mA, 30WV	07263	FDG1088
CR17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35, 37, 38, 40	1910-0016	Diode, Germanium, 25V	28480	1910-0016
MC16, 26, 36, 37, 46, 47, 56, 66	1820-0374	Integrated Circuit, TTL	01295	SN74H21N
MC17, 67	1820-0063	Integrated Circuit, TTL	56289	USN7451A
MC57, 77, 87	1820-0054	Integrated Circuit, TTL	56289	USN7400A
MC76, 86, 96, 97, 106, 107, 116, 126	1820-0069	Integrated Circuit, TTL	56289	USN7420A
Q1, 6, 11, 16, 21, 26, 31, 36, 41, 44, 47, 50, 53, 56, 59, 62	1853-0012	Transistor, Si, PNP	04713	2N2904A
Q2, 7, 12, 17, 22, 27, 32, 37	1854-0094	Transistor, Si, NPN	07263	2N3646
Q3, 8, 13, 18, 23, 28, 33, 38, 65, 66	1853-0016	Transistor, Si, PNP	07263	2N3638
Q4, 5, 9, 10, 14, 15, 19, 20, 24, 25, 29, 30, 34, 35, 39, 40, 67	1854-0246	Transistor, Si, NPN	07263	2N3643
Q42, 45, 48, 51, 54, 57, 60, 63	1854-0013	Transistor, Si, NPN	04713	2N2218A
Q43, 46, 49, 52, 55, 58, 61, 64	1853-0015	Transistor, Si, PNP	04713	MP53640-5
R1 thru R3, R108 thru R110, 113	0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4w	01121	CB2215
R4, 9, 11, 16, 18, 23, 25, 30, 32, 37, 39, 44, 46, 51, 53, 58, 124	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8w	28480	0757-0280
R5, 12, 19, 26, 33, 40, 47, 54	0698-3433	Resistor, Fxd, Flm, 28.7 ohms, 1%, 1/8w	28480	0698-3433
R6, 13, 20, 27, 34, 41, 48, 55	0683-0275	Resistor, Fxd, Com, 2.7 ohms, 5%, 1/4w	01121	CB0275

Table 5-12. A8, A9, A14, A15 Driver/Switch Card (02116-6266), Reference Designation Index (Cont)

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R7, 14, 21, 28, 35, 42, 49, 56, 60, 63, 64, 66, 69, 70, 72, 75, 76, 78, 81, 82, 84, 87, 88, 90, 93, 94, 96, 99, 100, 102, 105, 106	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8w	28480	0757-0401
R8, 15, 22, 29, 36, 46, 50, 57	0757-0399	Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/8w	28480	0757-0399
R10, 17, 24, 31, 38, 45, 52, 59	0698-3435	Resistor, Fxd, Flm, 38.3 ohms, 1%, 1/8w	28480	0698-3435
R61, 67, 73, 79, 85, 91, 97, 103	0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8w	28480	0698-3444
R62, 68, 74, 80, 86, 92, 98, 104	0757-0403	Resistor, Fxd, Flm, 121 ohms, 1%, 1/8w	28480	0757-0403
R65, 71, 77, 83, 89, 95, 101, 107, 119, 122	0698-3438	Resistor, Fxd, Flm, 147 ohms, 1%, 1/8w	28480	0698-3438
R111, 112	0811-2084	Resistor, Fxd, WW, 43 ohms, 1%, 5w	28480	0811-2084
R114 thru R117	0683-5615	Resistor, Fxd, Comp, 560 ohms, 5%, 1/4w	01121	CB5615
R120, 121	0698-3441	Resistor, Fxd, Flm, 215 ohms, 1%, 1/8w	28480	0698-3441
R123	0757-0419	Resistor, Fxd, Flm, 681 ohms, 1%, 1/8w	28480	0757-0419
T1 thru T16	9100-1238	Transformer	90095	1 WEMA

Pin Index (48 Pin Connector)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	ID0	A	$\overline{ID0}$
2	ID1	B	$\overline{ID1}$
3	ID2	C	$\overline{ID2}$
4	ID3	D	$\overline{ID3}$
5	ID4	E	$\overline{ID4}$
6	ID5	F	$\overline{ID5}$
7	ID6	H	$\overline{ID6}$
8	ID7	J	ID7
9	NC	K	NC
10	NC	L	NC
11	ID8	M	NC
12	NC	N	NC
13	NC	P	NC
14	NC	R	$\overline{ID8}$
15	NC	S	NC
16	NC	T	NC
17	ID9	U	$\overline{ID9}$
18	ID10	V	$\overline{ID10}$
19	ID11	W	$\overline{ID11}$
20	ID12	X	$\overline{ID12}$
21	ID13	Y	$\overline{ID13}$
22	ID14	Z	$\overline{ID14}$
23	ID15	AA	$\overline{ID15}$
24	ID16	BB	$\overline{ID16}$



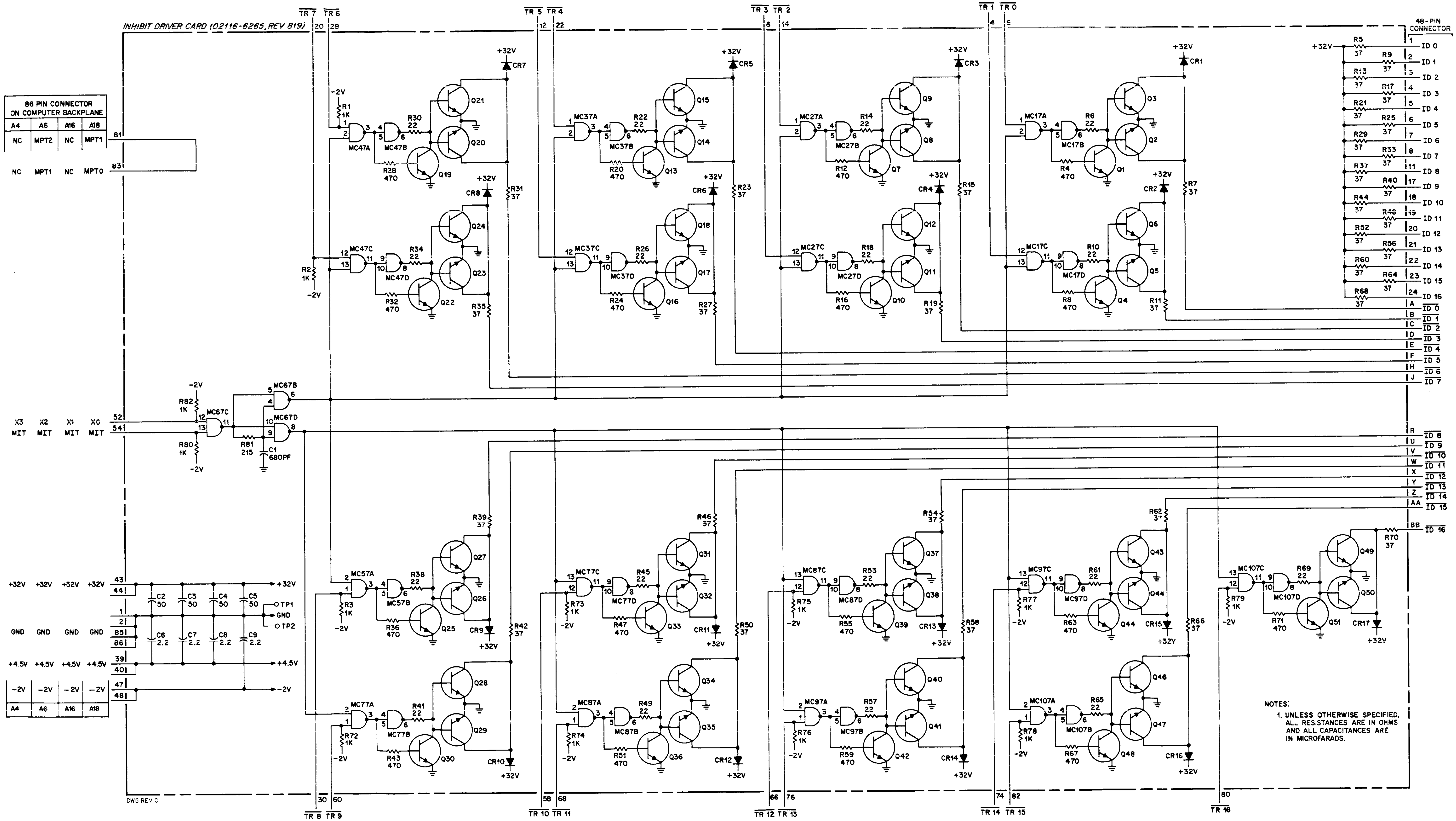


Figure 5-12. A4, A6, A16, and A18 Inhibit Driver Card (02116-6265), Schematic Diagram (Sheet 3 of 3)

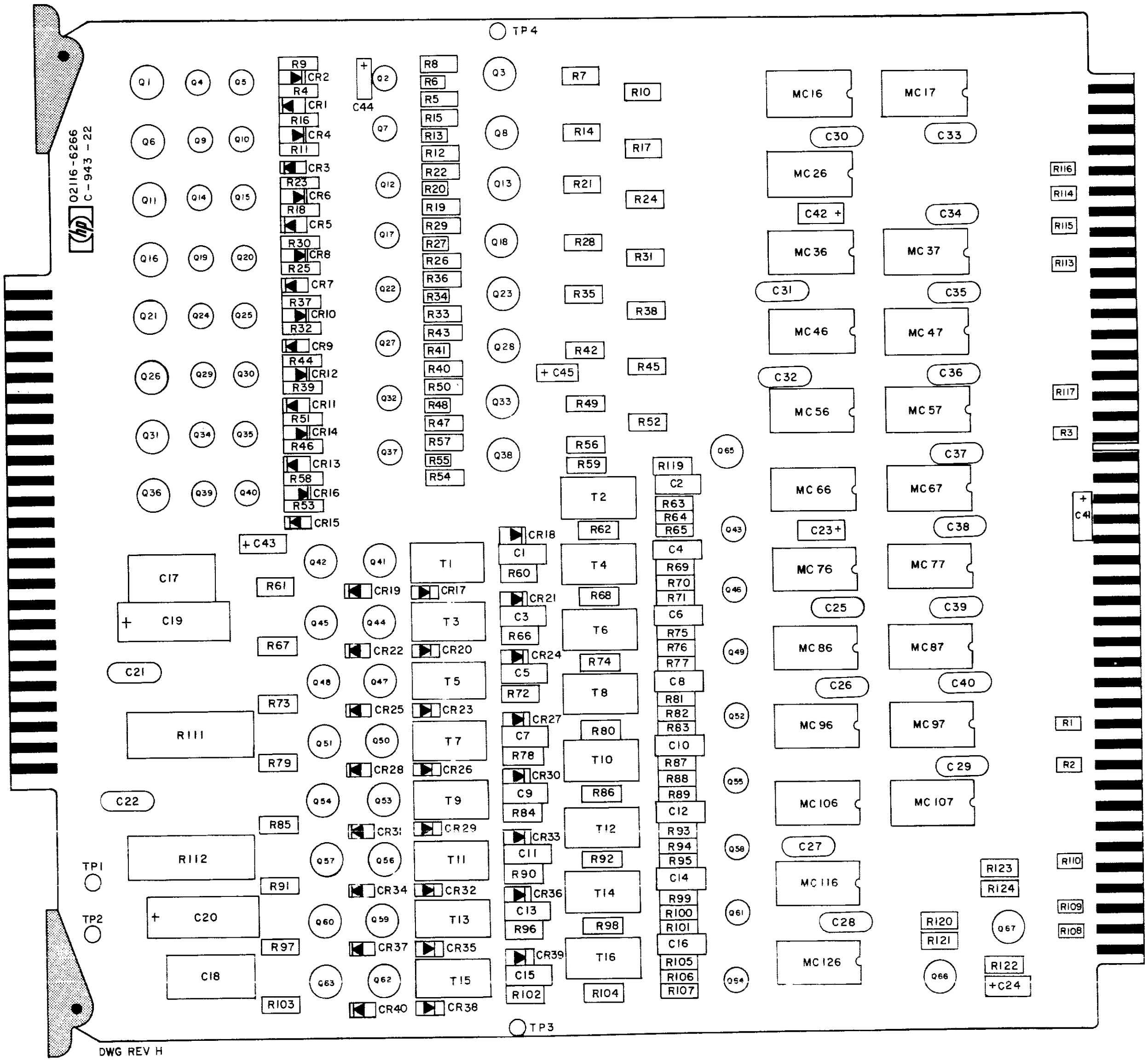


Figure 5-13. A8, A9, A14, and A15 Driver/Switch Card (02116-6266), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	A8 SIGNAL	A8 REF NO.	A9 SIGNAL	A9 REF NO.	A14 SIGNAL	A14 REF NO.	A15 SIGNAL	A15 REF NO.
1	GND	219	GND	219	GND	460	GND	460
2	GND	219	GND	219	GND	219	GND	219
3	NC	-	NC	-	NC	-	NC	-
4	NC	-	NC	-	NC	-	NC	-
5	NC	-	NC	-	NC	-	NC	-
6	NC	-	NC	-	NC	-	NC	-
7	NC	-	NC	-	NC	-	NC	-
8	NC	-	NC	-	NC	-	NC	-
9	NC	-	NC	-	NC	-	NC	-
10	GND	460	X3	223	GND	460	X1	221
11	NC	-	NC	-	NC	-	NC	-
12	MWT	124	MWT	124	MWT	124	MWT	124
13	NC	-	NC	-	NC	-	NC	-
14	Y2/Y3	225	X2	222	Y0/Y1	224	X0	220
15	NC	-	NC	-	NC	-	NC	-
16	NC	-	NC	-	NC	-	NC	-
17	NC	-	NC	-	NC	-	NC	-
18	MRT	94	MRT	94	MRT	94	MRT	94
19	NC	-	NC	-	NC	-	NC	-
20	NC	-	NC	-	NC	-	NC	-
21	NC	-	NC	-	NC	-	NC	-
22	NC	-	NC	-	NC	-	NC	-
23	NC	-	NC	-	NC	-	NC	-
24	NC	-	NC	-	NC	-	NC	-
25	NC	-	NC	-	NC	-	NC	-
26	NC	-	NC	-	NC	-	NC	-
27	NC	-	NC	-	NC	-	NC	-
28	NC	-	NC	-	NC	-	NC	-
29	NC	-	NC	-	NC	-	NC	-
30	MIT	92	MIT	92	MIT	92	MIT	92
31	NC	-	NC	-	NC	-	NC	-
32	NC	-	NC	-	NC	-	NC	-
33	-22V	4	-22V	4	-22V	4	-22V	4
34	-22V	4	-22V	4	-22V	4	-22V	4
35	NC	-	NC	-	NC	-	NC	-
36	NC	-	NC	-	NC	-	NC	-
37	NC	-	NC	-	NC	-	NC	-
38	M8	14	M2	8	M8	14	M2	8
39	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
40	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
41	NC	-	NC	-	NC	-	NC	-
42	NC	-	NC	-	NC	-	NC	-
43	+22V	3	+22V	3	+22V	3	+22V	3
44	+22V	3	+22V	3	+22V	3	+22V	3
45	NC	-	NC	-	NC	-	NC	-
46	PON	353	PON	353	PON	353	PON	353
47	-2V	216	-2V	216	-2V	216	-2V	216
48	-2V	216	-2V	216	-2V	216	-2V	216

Figure 5-14. A8, A9, A14, and A15 Driver/Switch Card (02116-6266), Schematic Diagram (Sheet 1 of 3)

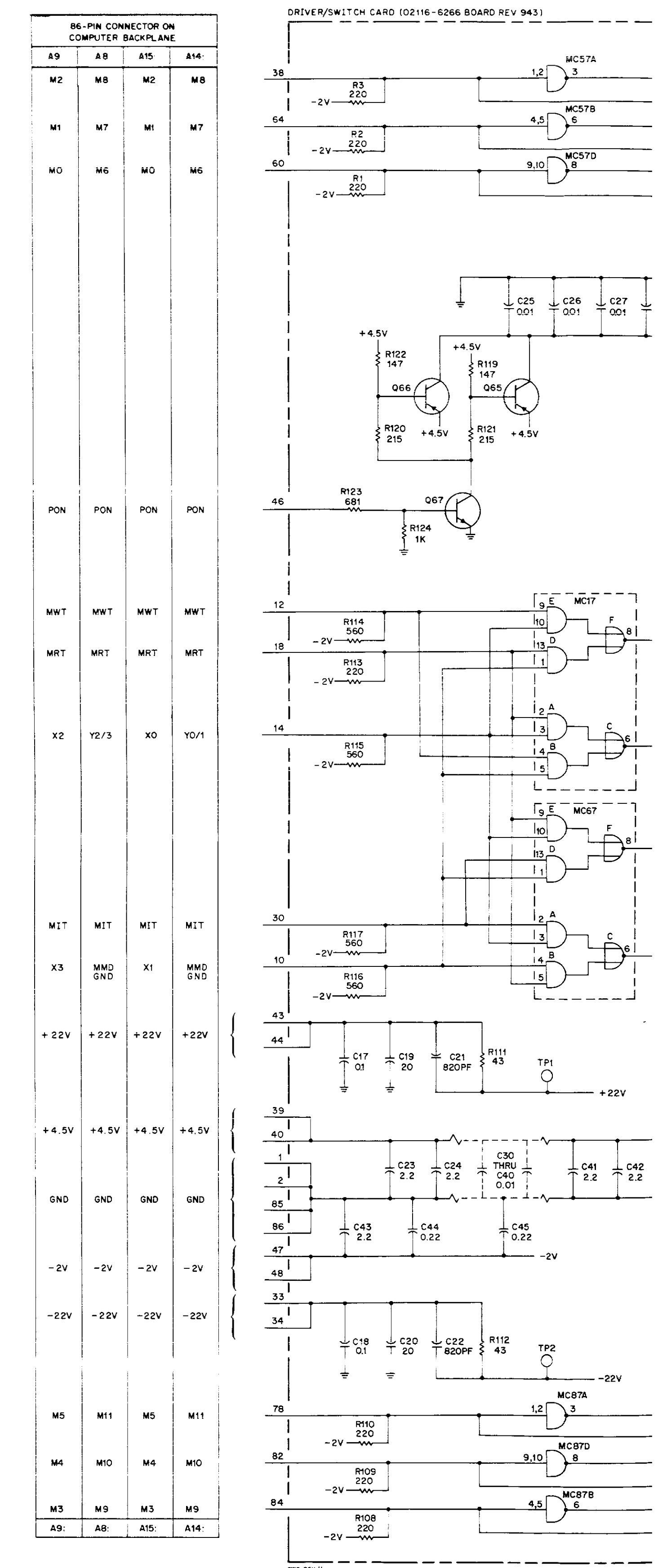
Pin Index (86 Pin Connector) (Cont)

PIN NO.	A8 SIGNAL	A8 REF NO.	A9 SIGNAL	A9 REF NO.	A14 SIGNAL	A14 REF NO.	A15 SIGNAL	A15 REF NO.
49	NC	-	NC	-	NC	-	NC	-
50	NC	-	NC	-	NC	-	NC	-
51	NC	-	NC	-	NC	-	NC	-
52	NC	-	NC	-	NC	-	NC	-
53	NC	-	NC	-	NC	-	NC	-
54	NC	-	NC	-	NC	-	NC	-
55	NC	-	NC	-	NC	-	NC	-
56	NC	-	NC	-	NC	-	NC	-
57	NC	-	NC	-	NC	-	NC	-
58	NC	-	NC	-	NC	-	NC	-
59	NC	-	NC	-	NC	-	NC	-
60	M6	12	M0	6	M6	12	M0	6
61	NC	-	NC	-	NC	-	NC	-
62	NC	-	NC	-	NC	-	NC	-
63	NC	-	NC	-	NC	-	NC	-
64	M7	13	M1	7	M7	13	M1	7
65	NC	-	NC	-	NC	-	NC	-
66	NC	-	NC	-	NC	-	NC	-
67	NC	-	NC	-	NC	-	NC	-
68	NC	-	NC	-	NC	-	NC	-
69	NC	-	NC	-	NC	-	NC	-
70	NC	-	NC	-	NC	-	NC	-
71	NC	-	NC	-	NC	-	NC	-
72	NC	-	NC	-	NC	-	NC	-
73	NC	-	NC	-	NC	-	NC	-
74	NC	-	NC	-	NC	-	NC	-
75	NC	-	NC	-	NC	-	NC	-
76	NC	-	NC	-	NC	-	NC	-
77	NC	-	NC	-	NC	-	NC	-
78	M11	17	M5	11	M11	17	M5	11
79	NC	-	NC	-	NC	-	NC	-
80	NC	-	NC	-	NC	-	NC	-
81	NC	-	NC	-	NC	-	NC	-
82	M10	16	M4	10	M10	16	M4	10
83	NC	-	NC	-	NC	-	NC	-
84	M9	15	M3	9	M9	15	M3	9
85	GND	219	GND	219	GND	219	GND	219
86	GND	219	GND	219	GND	219	GND	219

Figure 5-14. A8, A9, A14, and A15 Driver/Switch Card (02116-6266), Schematic Diagram (Sheet 2 of 3)

Pin Index (48 Pin Connector)

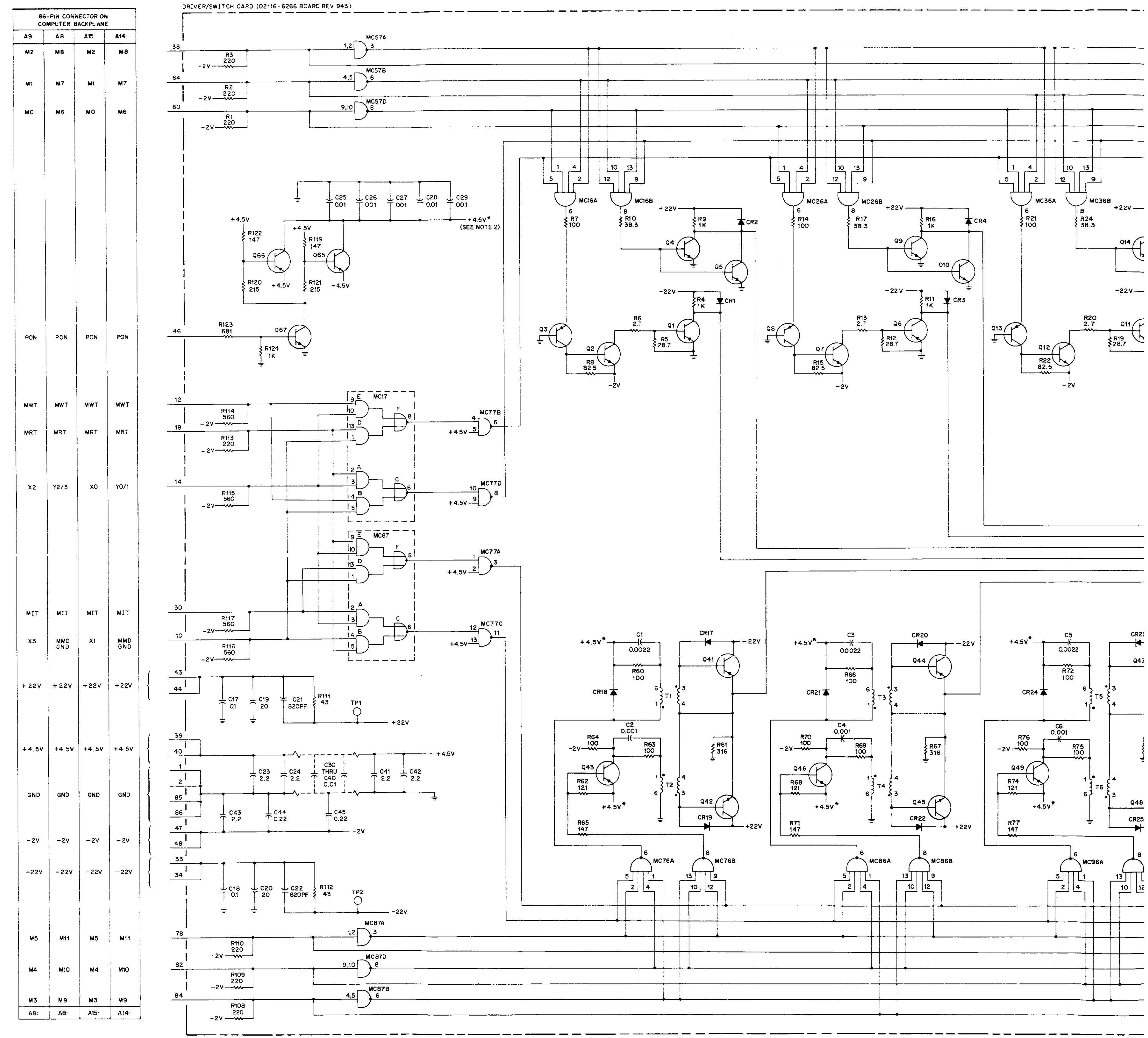
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	CC0	A	CC0
2	CA0	B	CA0
3	CC1	C	CC1
4	CA1	D	CA1
5	CC2	E	CC2
6	CA2	F	CA2
7	CC3	H	CC3
8	CA3	J	CA3
9	CC4	K	CC4
10	CA4	L	CA4
11	CC5	M	CC5
12	CA5	N	CA5
13	CC6	P	CC6
14	CA6	R	CA6
15	CC7	S	CC7
16	CA7	T	CA7
17	C0	U	C0
18	C1	V	C1
19	C2	W	C2
20	C3	X	C3
21	C4	Y	C4
22	C5	Z	C5
23	C6	AA	C6
24	C7	BB	C7

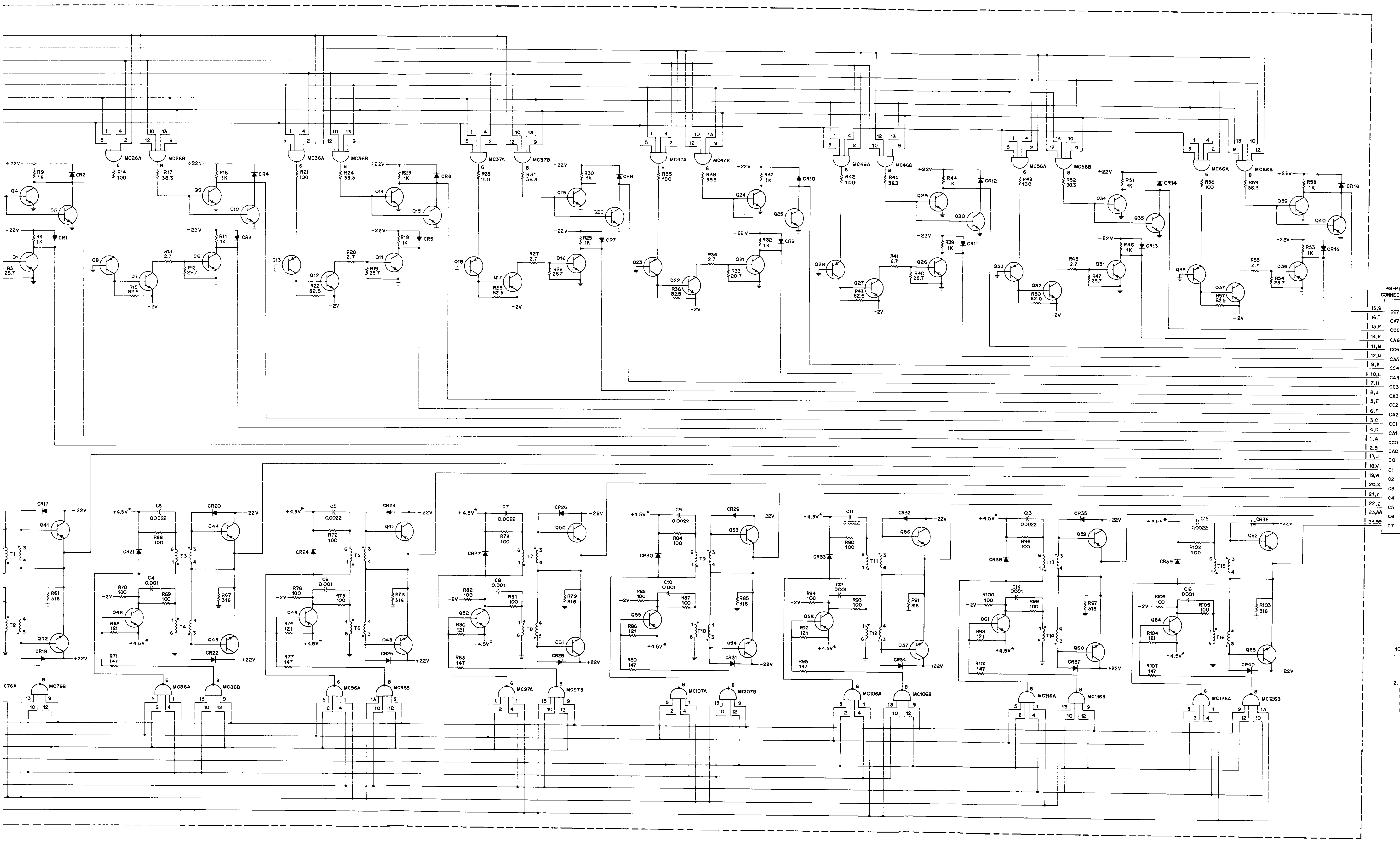


Pin Index (48 Pin Connector)

SIGNAL
CC0
CA0
CC1
CA1
CC2
CA2
CC3
CA3
CC4
CA4
CC5
CA5
CC6
CA6
CC7
CA7
C0
C1
C2
C3
C4
C5
C6
C7

PIN NO.	SIGNAL
A	CC0
B	CA0
C	CC1
D	CA1
E	CC2
F	CA2
H	CC3
J	CA3
K	CC4
L	CA4
M	CC5
N	CA5
P	CC6
R	CA6
S	CC7
T	CA7
U	C0
V	C1
W	C2
X	C3
Y	C4
Z	C5
AA	C6
BB	C7





NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS ALL CAPACITANCES ARE IN MICROFARADS.
2. * DENOTES POWER CONTROLLED PON SIGNAL. THE +4.5* SOURCE SUPPLIES POWER TO PIN 14 OF MC76, MC86, MC96, MC97, MC106, MC107, MC116, AND MC126.

Figure 5-14. A8, A9, A14, and A15 Driver/Switch Card (02116-6266), Schematic Diagram (Sheet 3 of 3)

Table 5-13. A10, A11, A12, A13 Sense Amplifier Card (02116-6298), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C9	0180-0155	Capacitor, Fxd, Elect, 2.2 μf, 20%, 20VDCW	28480	0180-0155
C10 thru C12	0160-2055	Capacitor, Fxd, Cer, 0.01 μf, +80 -20%, 100VDCW	56289	C023F101F103-ZE12CDH
MC1, 11, 21, 31, 41, 51, 61, 71, 81, 91, 101, 111, 121, 131, 141, 151, 161	1820-0183	Integrated Circuit, TTL	02735	80170
MC17, 27, 37, 47, 57, 77, 87, 97, 107	1820-0186	Integrated Circuit, TTL	28480	1820-0186
Q1, 2, 11, 12, 21, 22, 31, 32, 41, 42, 51, 52, 61, 62, 71, 72, 81, 82, 91, 92, 101, 102, 111, 112, 121, 122, 131, 132, 141, 142, 151, 152, 161, 162	1853-0036	Transistor, Si, PNP	04713	SP3612
Q3, 13, 23, 33, 43, 53, 63, 73, 83, 93, 103, 113, 123, 133, 143, 153, 163	1854-0094	Transistor, Si, NPN	07263	2N3646
Q164	1854-0215	Transistor, Si, NPN	28480	1854-0215
R1, 11, 21, 31, 41, 51, 61, 71, 81, 97, 107, 117, 127, 137, 147, 157, 167, 169	0757-0416	Resistor, Fxd, Flm, 511 ohms, 1%, 1/8w	28480	0757-0416
R2, 12, 22, 32, 42, 52, 62, 72, 82, 96, 106, 116, 126, 136, 146, 156, 166	0757-0438	Resistor, Fxd, Flm, 5.11 k, 1%, 1/8w	28480	0757-0438
R3, 4, 13, 14, 23, 24, 33, 34, 43, 44, 53, 54, 63, 64, 73, 74, 83, 84, 94, 95, 104, 105, 114, 115, 124, 125, 134, 135, 144, 145, 154, 155, 164, 165	0698-7310	Resistor, Fxd, Flm, 1.65 k, 1%, 1/8w	28480	0698-7310
R5, 15, 25, 35, 45, 55, 65, 75, 85, 93, 103, 113, 123, 133, 143, 153, 163	0698-3488	Resistor, Fxd, Flm, 442 ohms, 1%, 1/8w	28480	0698-3488
R6, 7, 16, 17, 26, 27, 36, 37, 46, 47, 56, 57, 66, 67, 76, 77, 86, 87, 91, 92, 101, 102, 111, 112, 121, 122, 131, 132, 141, 142, 151, 152, 161, 162	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8w	28480	0757-0401

Table 5-13. A10, A11, A12, A13 Sense Amplifier Card (0211

REFERENCE DESIGNATION	HP PART NO.	DESCRI
R168	0698-3441	Resistor, Fxd, Flm, 215
R170	0698-3444	Resistor, Fxd, Flm, 316
R171, 172, 173, 174, 179, 180, 181, 182, 187, 188, 189, 190, 195, 196, 197, 198 199	0757-0280	Resistor, Fxd, Flm, 1k, 1
R200	0757-0427	Resistor, Fxd, Flm, 1.50

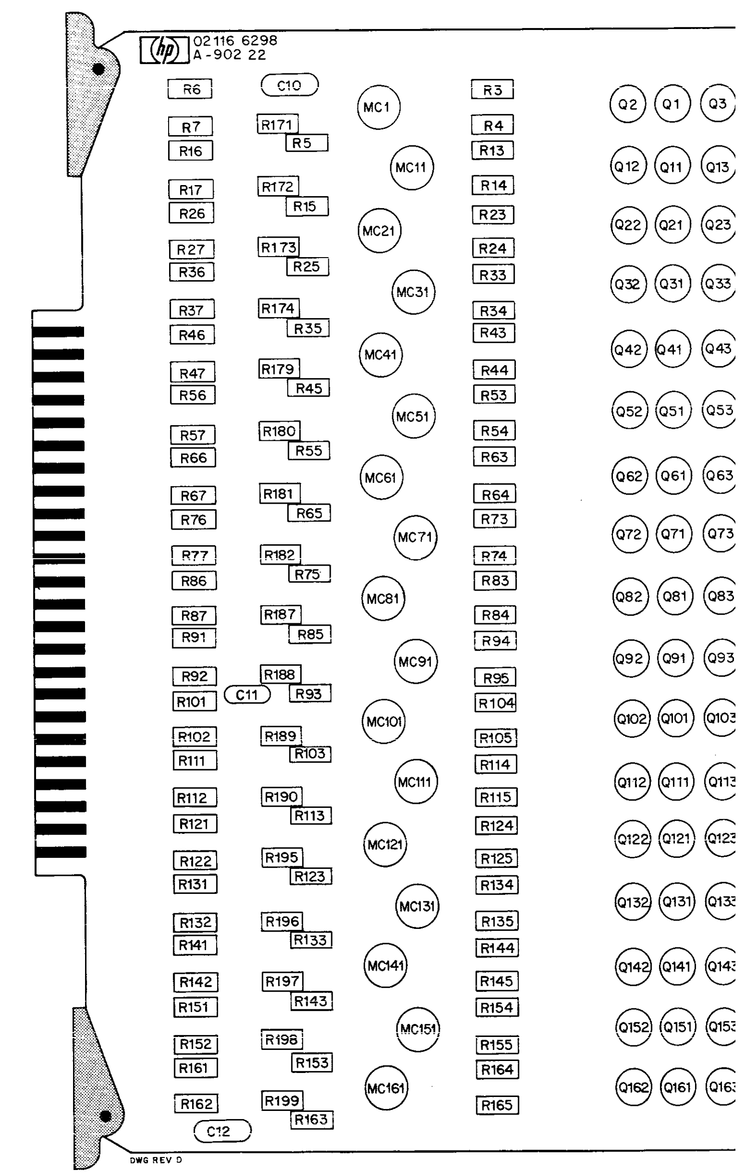


Figure 5-15. A10, A11, A12, and A13 Sense Amplifier Car

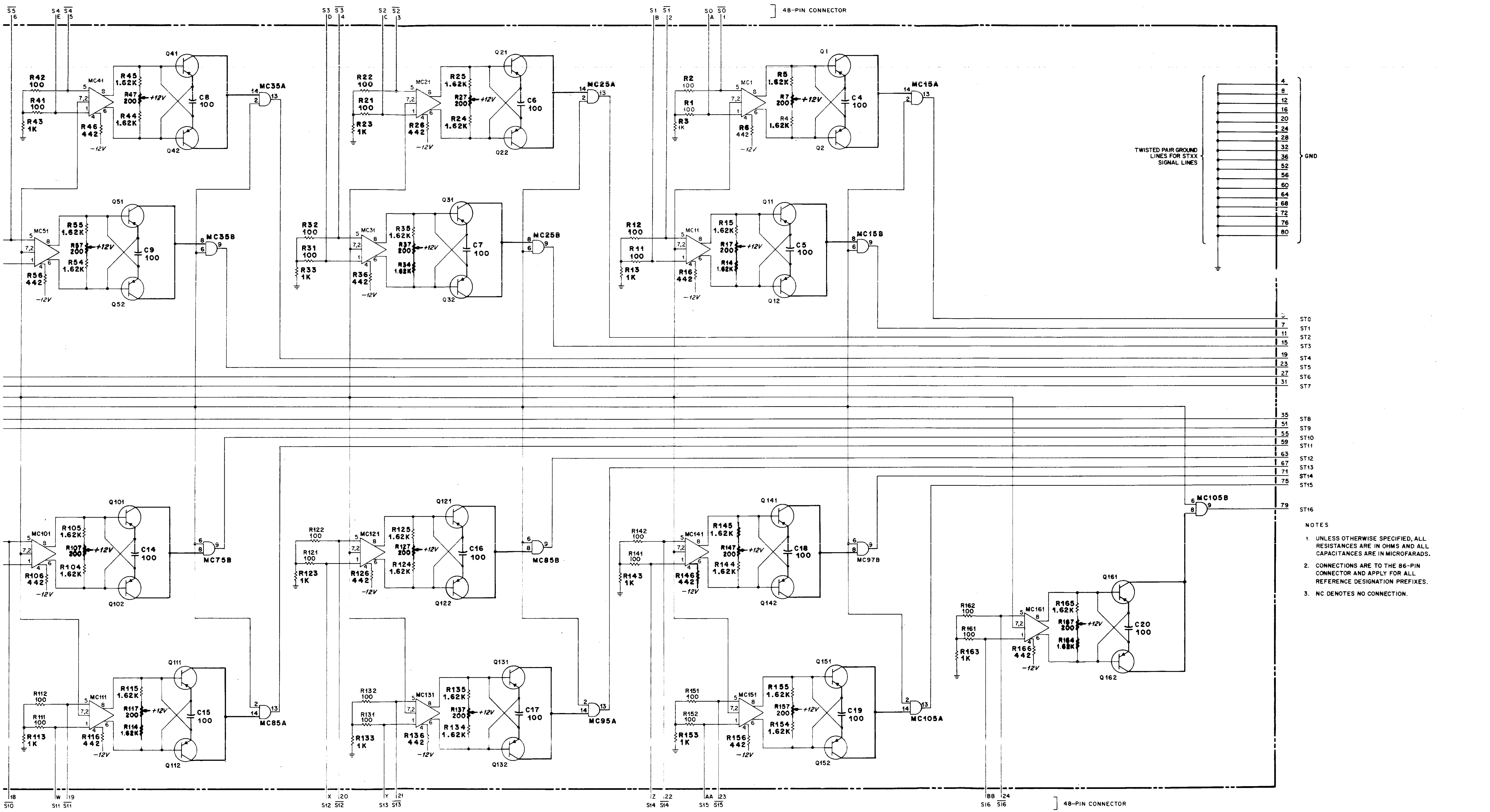
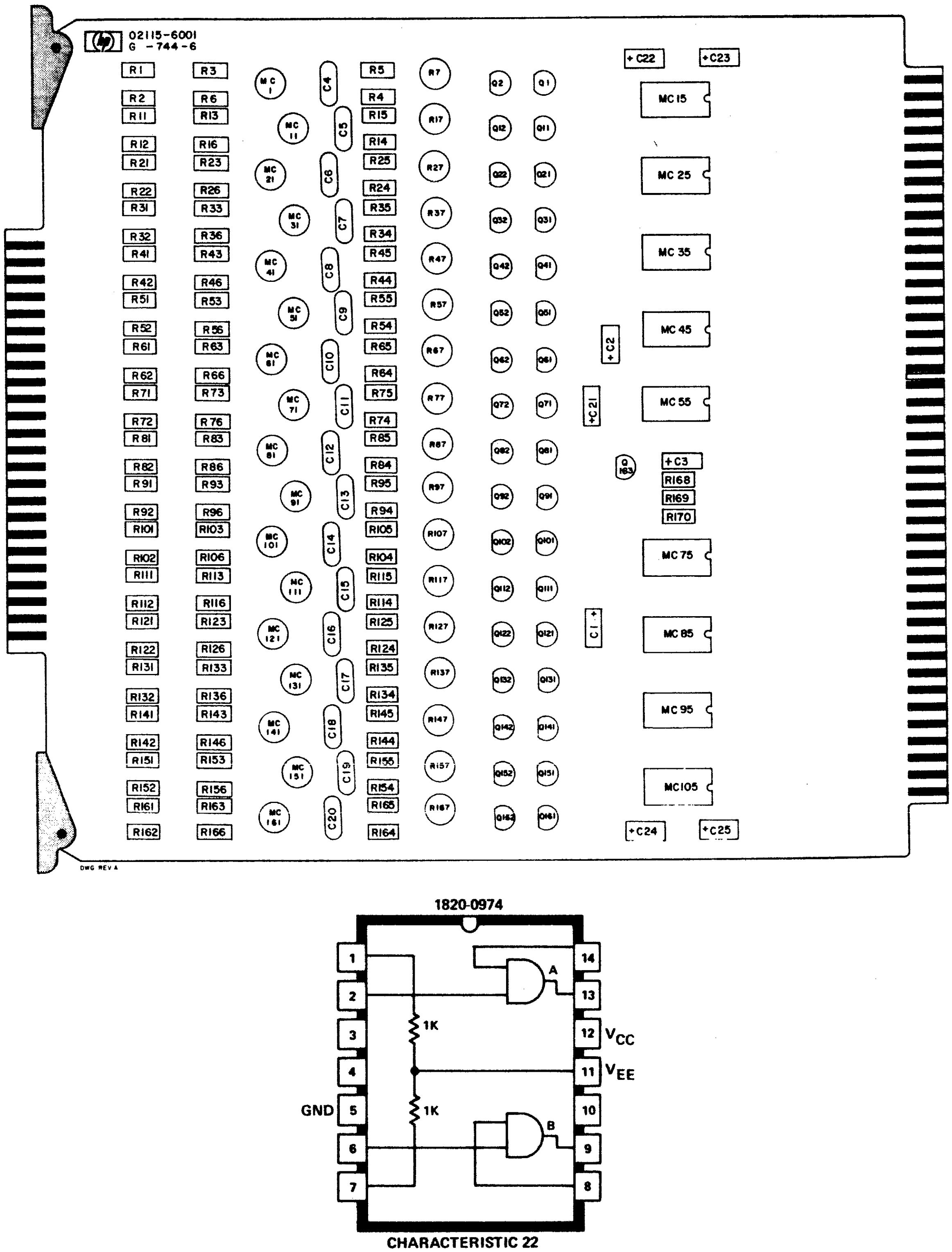


Figure 5-15B. A10, A11, A12, and A13 Sense Amplifier Card (02115-6001), Schematic Diagram (sheet 3 of 3)

Table 5-13A. A10, A11, A12, and A13 Sense Amplifier Card (02115-6001), Reference Designation Index

REFERENCE DESGINATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C3, C21 thru C25	0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	28480	0180-0155
C4 thru C20	0140-0176	Capacitor, Fxd, Mica, 100 pF, 2%	28480	0140-0176
MC1,11,21,31,41,51,61,71,81, 91,101,111,121,131,141, 151,161	1820-0183	Integrated Circuit	28480	1820-0183
MC15,25,35,45,55,75,85,95, 105	1820-0974	Integrated Circuit	07263	SL4817
Q1,2,11,12,21,22,31,32,41,42, 51,52,61,62,71,72,81,82, 91,92,101,102,111,112,121, 122,131,132,141,142,151, 152,161,162	1853-0036	Transistor, Si, PNP	04713	SP3612
Q163	1854-0215	Transistor, Si, NPN	28480	1854-0215
R1,2,11,12,21,22,31,32,41,42, 51,52,61,62,71,72,81,82, 91,92,101,102,111,112,121, 122,131,132,141,142,151, 152,161,162	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	28480	0757-0401
R3,13,23,33,43,53,63,73,83,93, 103,113,123,133,143,153,163	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280
R4,5,14,15,24,25,34,35,44,45, 54,55,64,65,74,75,84,85,94, 95,104,105,114,115,124,125, 134,135,144,145,154,155, 164,165	0757-0428	Resistor, Fxd, Flm, 1.62k, 1%, 1/8W	28480	0757-0428
R6,16,26,36,46,56,66,76,86,96, 106,116,126,136,146,156,166	0698-3488	Resistor, Fxd, Flm, 442 ohms, 1%, 1/8W	28480	0698-3488
R7,17,27,37,47,57,67,77,87,97, 107,117,127,137,147,157,167	2100-2061	Resistor, Var, 200 ohms, 10%, Lin, 1/2W	28480	2100-2061
R168	0757-0416	Resistor, Fxd, Flm, 511 ohms, 1%, 1/8W	28480	0757-0416
R169	0698-3441	Resistor, Fxd, Flm, 215 ohms, 1%, 1/8W	28480	0698-3441
R170	0757-0417	Resistor, Fxd, Flm, 562 ohms, 1%, 1/8W	28480	0757-0417



CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN ACTS AS	PROPAGATION DELAY	
	Logic 1 (Volts, Min)	Logic 0 (Volts, Max)	Logic 1 (Volts, Min)	Logic 0 (Volts, Max)		To 1 (Nanosec)	To 0 (Nanosec)
22	+1.5V	+0.4V	+2.2V	-0.3V	0	24	24

Figure 5-15A. A10, A11, A12, and A13 Sense Amplifier Card (02115-6001), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	A10 SIGNAL	A10 REF NO.	A11 SIGNAL	A11 REF NO.	A12 SIGNAL	A12 REF NO.	A13 SIGNAL	A13 REF NO.
1	GND	219	GND	219	GND	219	GND	219
2	GND	219	GND	219	GND	219	GND	219
3	ST0	227	ST0	227	ST0	227	ST0	227
4	GND	219	GND	219	GND	219	GND	219
5	NC	-	NC	-	NC	-	NC	-
6	NC	-	NC	-	NC	-	NC	-
7	ST1	228	ST1	228	ST1	228	ST1	228
8	GND	219	GND	219	GND	219	GND	219
9	NC	-	NC	-	NC	-	NC	-
10	NC	-	NC	-	NC	-	NC	-
11	ST2	229	ST2	229	ST2	229	ST2	229
12	GND	219	GND	219	GND	219	GND	219
13	NC	-	NC	-	NC	-	NC	-
14	NC	-	NC	-	NC	-	NC	-
15	ST3	230	ST3	230	ST3	230	ST3	230
16	GND	219	GND	219	GND	219	GND	219
17	NC	-	NC	-	NC	-	NC	-
18	NC	-	NC	-	NC	-	NC	-
19	ST4	231	ST4	231	ST4	231	ST4	231
20	GND	219	GND	219	GND	219	GND	219
21	NC	-	NC	-	NC	-	NC	-
22	NC	-	NC	-	NC	-	NC	-
23	ST5	-	ST5	-	ST5	-	ST5	-
24	GND	219	GND	219	GND	219	GND	219
25	NC	-	NC	-	NC	-	NC	-
26	NC	-	NC	-	NC	-	NC	-
27	ST6	233	ST6	233	ST6	233	ST6	233
28	GND	219	GND	219	GND	219	GND	219
29	NC	-	NC	-	NC	-	NC	-
30	NC	-	NC	-	NC	-	NC	-
31	ST7	-	ST7	-	ST7	-	ST7	-
32	GND	219	GND	219	GND	219	GND	219
33	NC	-	NC	-	NC	-	NC	-
34	NC	-	NC	-	NC	-	NC	-
35	ST8	-	ST8	-	ST8	-	ST8	-
36	GND	219	GND	219	GND	219	GND	219
37	NC	-	NC	-	NC	-	NC	-
38	NC	-	NC	-	NC	-	NC	-
39	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
40	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
41	MST	111	MST	111	MST	111	MST	111
42	NC	-	NC	-	NC	-	NC	-
43	+12V	1	+12V	1	+12V	1	+12V	1
44	+12V	1	+12V	1	+12V	1	+12V	1
45	X3	223	X2	222	X1	221	X0	220
46	NC	-	NC	-	NC	-	NC	-
47	-2V	216	-2V	216	-2V	216	-2V	216
48	-2V	216	-2V	216	-2V	216	-2V	216

Figure 5-15B. A10, A11, A12, and A13 Sense Amplifier Card (02115-6001), Schematic Diagram (sheet 1 of 3)

Pin Index (86 Pin Connector) (Cont)

PIN NO.	A10 SIGNAL	A10 REF NO.	A11 SIGNAL	A11 REF NO.	A12 SIGNAL	A12 REF NO.	A13 SIGNAL	A13 REF NO.
49	NC	-	NC	-	NC	-	NC	-
50	NC	-	NC	-	NC	-	NC	-
51	ST9	236	ST9	236	ST9	236	ST9	236
52	GND	219	GND	219	GND	219	GND	219
53	NC	-	NC	-	NC	-	NC	-
54	NC	-	NC	-	NC	-	NC	-
55	ST10	237	ST10	237	ST10	237	ST10	237
56	GND	219	GND	219	GND	219	GND	219
57	NC	-	NC	-	NC	-	NC	-
58	NC	-	NC	-	NC	-	NC	-
59	ST11	238	ST11	238	ST11	238	ST11	238
60	GND	219	GND	219	GND	219	GND	219
61	NC	-	NC	-	NC	-	NC	-
62	NC	-	NC	-	NC	-	NC	-
63	ST12	239	ST12	239	ST12	239	ST12	239
64	GND	219	GND	219	GND	219	GND	219
65	-12V	2	-12V	2	-12V	2	-12V	2
66	-12V	2	-12V	2	-12V	2	-12V	2
67	ST13	240	ST13	240	ST13	240	ST13	240
68	GND	219	GND	219	GND	219	GND	219
69	-12V	2	-12V	2	-12V	2	-12V	2
70	-12V	2	-12V	2	-12V	2	-12V	2
71	ST14	241	ST14	241	ST14	241	ST14	241
72	GND	219	GND	219	GND	219	GND	219
73	NC	-	NC	-	NC	-	NC	-
74	NC	-	NC	-	NC	-	NC	-
75	ST15	242	ST15	242	ST15	242	ST15	242
76	GND	219	GND	219	GND	219	GND	219
77	NC	-	NC	-	NC	-	NC	-
78	NC	-	NC	-	NC	-	NC	-
79	ST16	459	ST16	459	ST16	459	ST16	459
80	GND	219	GND	219	GND	219	GND	219
81	NC	-	NC	-	NC	-	NC	-
82	NC	-	NC	-	NC	-	NC	-
83	NC	-	M13	19	NC	-	NC	-
84	NC	-	MMD13	457	NC	-	NC	-
85	GND	219	GND	219	GND	219	GND	219
86	GND	219	GND	219	GND	219	GND	219

Figure 5-15B. A10, A11, A12, and A13 Sense Amplifier Card (02115-6001), Schematic Diagram (sheet 2 of 3)

Pin Index (86 Pin Connector)

PIN NO.	A10 SIGNAL	A10 REF NO.	A11 SIGNAL	A11 REF NO.	A12 SIGNAL	A12 REF NO.	A13 SIGNAL	A13 REF NO.
1	GND	219	GND	219	GND	219	GND	219
2	GND	219	GND	219	GND	219	GND	219
3	ST0	227	ST0	227	ST0	227	ST0	227
4	GND	219	GND	219	GND	219	GND	219
5	NC	-	NC	-	NC	-	NC	-
6	NC	-	NC	-	NC	-	NC	-
7	ST1	228	ST1	228	ST1	228	ST1	228
8	GND	219	GND	219	GND	219	GND	219
9	NC	-	NC	-	NC	-	NC	-
10	NC	-	NC	-	NC	-	NC	-
11	ST2	229	ST2	229	ST2	229	ST2	229
12	GND	219	GND	219	GND	219	GND	219
13	NC	-	NC	-	NC	-	NC	-
14	NC	-	NC	-	NC	-	NC	-
15	ST3	230	ST3	230	ST3	230	ST3	230
16	GND	219	GND	219	GND	219	GND	219
17	NC	-	NC	-	NC	-	NC	-
18	NC	-	NC	-	NC	-	NC	-
19	ST4	231	ST4	231	ST4	231	ST4	231
20	GND	219	GND	219	GND	219	GND	219
21	NC	-	NC	-	NC	-	NC	-
22	NC	-	NC	-	NC	-	NC	-
23	ST5	-	ST5	-	ST5	-	ST5	-
24	GND	219	GND	219	GND	219	GND	219
25	NC	-	NC	-	NC	-	NC	-
26	NC	-	NC	-	NC	-	NC	-
27	ST6	233	ST6	233	ST6	233	ST6	233
28	GND	219	GND	219	GND	219	GND	219
29	NC	-	NC	-	NC	-	NC	-
30	NC	-	NC	-	NC	-	NC	-
31	ST7	-	ST7	-	ST7	-	ST7	-
32	GND	219	GND	219	GND	219	GND	219
33	NC	-	NC	-	NC	-	NC	-
34	NC	-	NC	-	NC	-	NC	-
35	ST8	-	ST8	-	ST8	-	ST8	-
36	GND	219	GND	219	GND	219	GND	219
37	NC	-	NC	-	NC	-	NC	-
38	NC	-	NC	-	NC	-	NC	-
39	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
40	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
41	MST	111	MST	111	MST	111	MST	111
42	NC	-	NC	-	NC	-	NC	-
43	+12V	1	+12V	1	+12V	1	+12V	1
44	+12V	1	+12V	1	+12V	1	+12V	1
45	X3	223	X2	222	X1	221	X0	220
46	NC	-	NC	-	NC	-	NC	-
47	-2V	216	-2V	216	-2V	216	-2V	216
48	-2V	216	-2V	216	-2V	216	-2V	216

Figure 5-16. A10, A11, A12, and A13 Sense Amplifier Card (02116-6298), Schematic Diagram (Sheet 1 of 3)

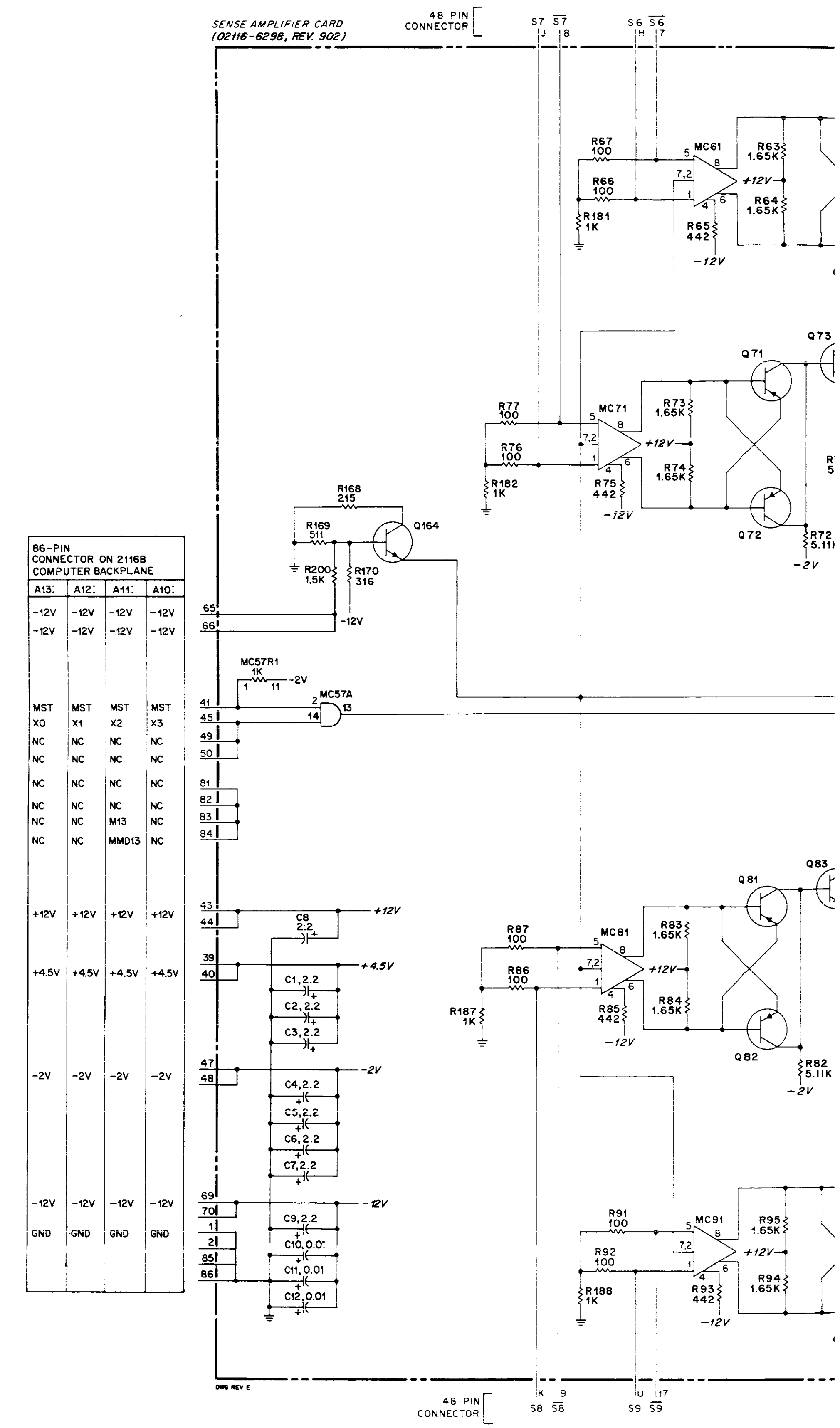
Pin Index (86 Pin Connector) (Cont)

PIN NO.	A10 SIGNAL	A10 REF NO.	A11 SIGNAL	A11 REF NO.	A12 SIGNAL	A12 REF NO.	A13 SIGNAL	A13 REF NO.
49	NC	-	NC	-	NC	-	NC	-
50	NC	-	NC	-	NC	-	NC	-
51	ST9	236	ST9	236	ST9	236	ST9	236
52	GND	219	GND	219	GND	219	GND	219
53	NC	-	NC	-	NC	-	NC	-
54	NC	-	NC	-	NC	-	NC	-
55	ST10	237	ST10	237	ST10	237	ST10	237
56	GND	219	GND	219	GND	219	GND	219
57	NC	-	NC	-	NC	-	NC	-
58	NC	-	NC	-	NC	-	NC	-
59	ST11	238	ST11	238	ST11	238	ST11	238
60	GND	219	GND	219	GND	219	GND	219
61	NC	-	NC	-	NC	-	NC	-
62	NC	-	NC	-	NC	-	NC	-
63	ST12	239	ST12	239	ST12	239	ST12	239
64	GND	219	GND	219	GND	219	GND	219
65	-12V	2	-12V	2	-12V	2	-12V	2
66	-12V	2	-12V	2	-12V	2	-12V	2
67	ST13	240	ST13	240	ST13	240	ST13	240
68	GND	219	GND	219	GND	219	GND	219
69	-12V	2	-12V	2	-12V	2	-12V	2
70	-12V	2	-12V	2	-12V	2	-12V	2
71	ST14	241	ST14	241	ST14	241	ST14	241
72	GND	219	GND	219	GND	219	GND	219
73	NC	-	NC	-	NC	-	NC	-
74	NC	-	NC	-	NC	-	NC	-
75	ST15	242	ST15	242	ST15	242	ST15	242
76	GND	219	GND	219	GND	219	GND	219
77	NC	-	NC	-	NC	-	NC	-
78	NC	-	NC	-	NC	-	NC	-
79	ST16	459	ST16	459	ST16	459	ST16	459
80	GND	219	GND	219	GND	219	GND	219
81	NC	-	NC	-	NC	-	NC	-
82	NC	-	NC	-	NC	-	NC	-
83	NC	-	M13	19	NC	-	NC	-
84	NC	-	MMD13	457	NC	-	NC	-
85	GND	219	GND	219	GND	219	GND	219
86	GND	219	GND	219	GND	219	GND	219

Figure 5-16. A10, A11, A12, and A13 Sense Amplifier Card (02116-6298), Schematic Diagram (Sheet 2 of 3)

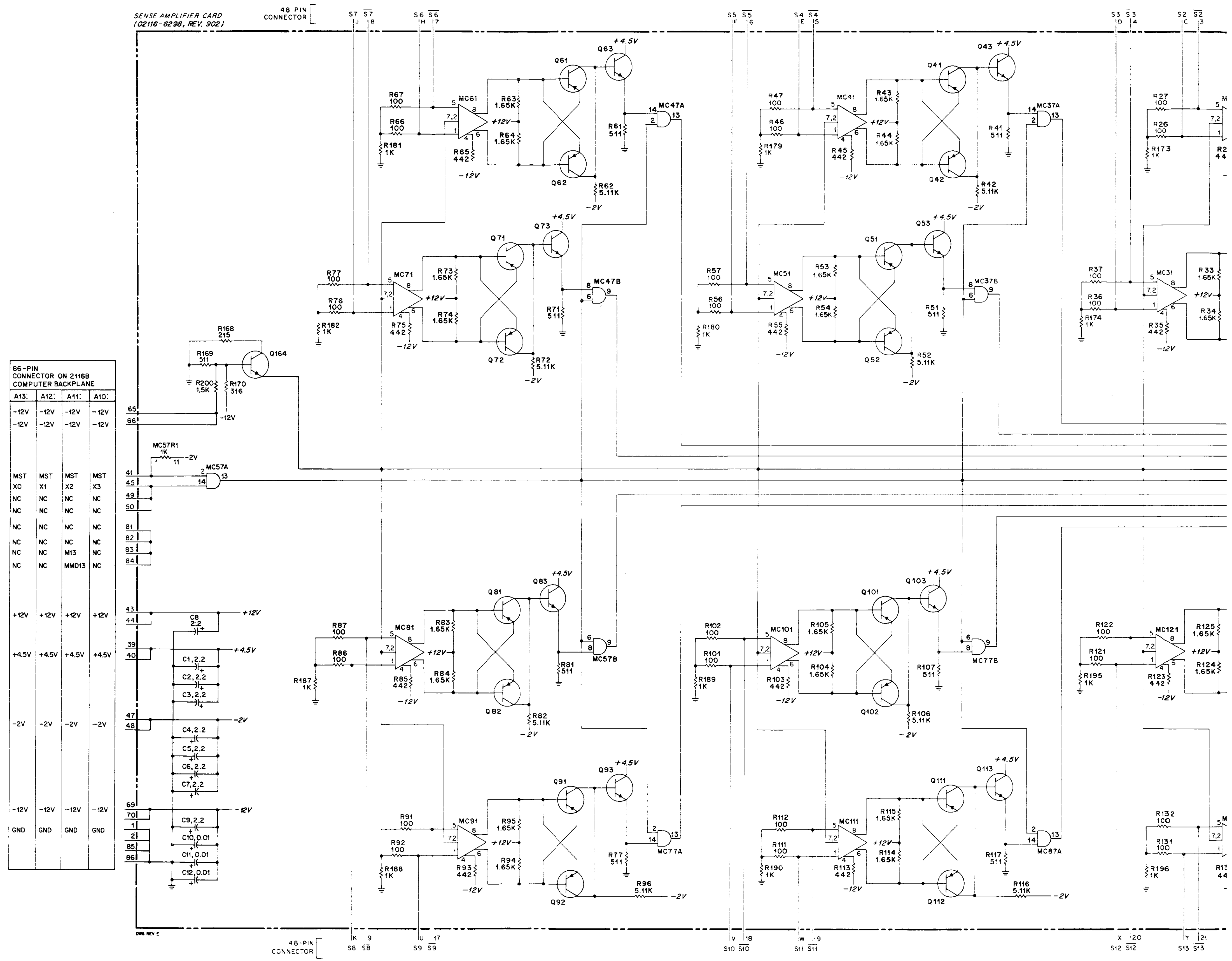
Pin Index (48 Pin Connector)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	$\overline{S0}$	A	S0
2	$\overline{S1}$	B	S1
3	$\overline{S2}$	C	S2
4	$\overline{S3}$	D	S3
5	$\overline{S4}$	E	S4
6	$\overline{S5}$	F	S5
7	$\overline{S6}$	H	S6
8	$\overline{S7}$	J	S7
9	$\overline{S8}$	K	S8
10	NC	L	NC
11	NC	M	NC
12	NC	N	NC
13	NC	P	NC
14	NC	R	NC
15	NC	S	NC
16	NC	T	NC
17	$\overline{S9}$	U	S9
18	$\overline{S10}$	V	S10
19	$\overline{S11}$	W	S11
20	$\overline{S12}$	X	S12
21	$\overline{S13}$	Y	S13
22	$\overline{S14}$	Z	S14
23	$\overline{S15}$	AA	S15
24	$\overline{S16}$	BB	S16



Pin Index (48 Pin Connector)

SIGNAL	PIN NO.	SIGNAL
$\overline{S0}$	A	S0
$\overline{S1}$	B	S1
$\overline{S2}$	C	S2
$\overline{S3}$	D	S3
$\overline{S4}$	E	S4
$\overline{S5}$	F	S5
$\overline{S6}$	H	S6
$\overline{S7}$	J	S7
$\overline{S8}$	K	S8
NC	L	NC
NC	M	NC
NC	N	NC
NC	P	NC
NC	R	NC
NC	S	NC
NC	T	NC
$\overline{S9}$	U	S9
$\overline{S10}$	V	S10
$\overline{S11}$	W	S11
$\overline{S12}$	X	S12
$\overline{S13}$	Y	S13
$\overline{S14}$	Z	S14
$\overline{S15}$	AA	S15
$\overline{S16}$	BB	S16



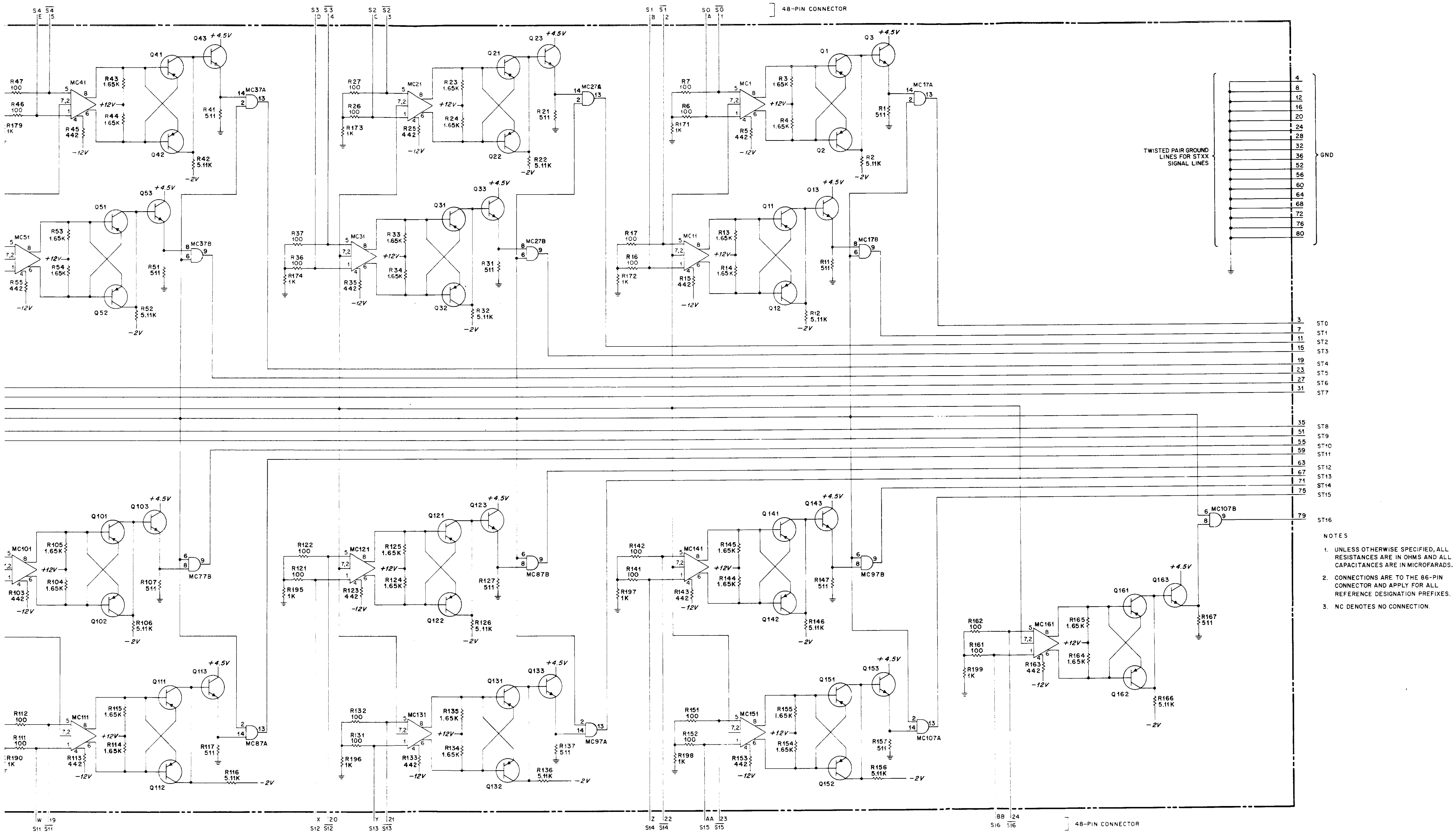


Figure 5-16. A10, A11, A12, and A13 Sense Amplifier Card (02116-6298), Schematic Diagram (Sheet 3 of 3)

Table 5-14. A20 Direct Memory Logic Card (02116-6069), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C6	0180-0197	Capacitor, Fxd, Elect, 2.2 μf, 10%, 20VDCW	28480	0180-0197
MC15, 25, 35, 45, 55, 65, 75, 95, 96, 97	1820-0187	Integrated Circuit, CTL	28480	1820-0187
MC16, 17, 26, 27, 36, 37, 46, 47, 56, 57, 66, 67, 76, 77, 86, 87, 105, 106, 107	1820-0186	Integrated Circuit, TTL	28480	1820-0187
MC85	1820-0965	Integrated Circuit, CTL	07263	SL3462
R1	0698-3443	Resistor, Fxd, Flm, 287 ohms, 1%, 1/8w	28480	0698-3443

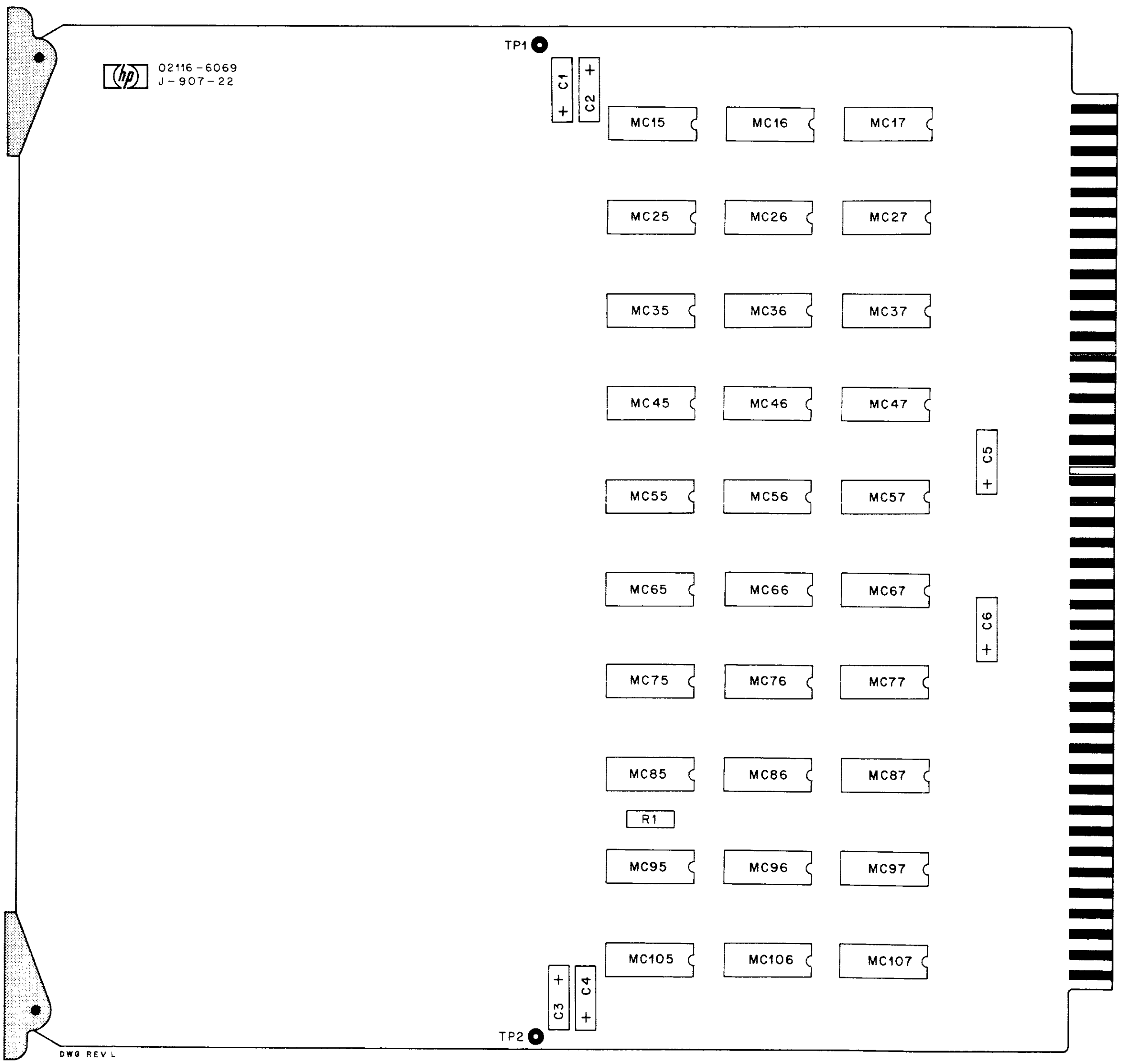


Figure 5-17. A20 Direct Memory Logic Card (02116-6069), Parts Location Diagram

Table 5-14A. A20 Direct Memory Logic Card (02115-6044), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C6	0180-0291	Capacitor, Fxd, Elect, 1.0 uF, 10%, 35 VDCW	28480	0180-0291
MC16,26,36,46,56,66,76,95, 96,97	1820-0952	Integrated Circuit	07263	SL3455
MC17,27,37,47,57,67,77,87	1820-0971	Integrated Circuit	07263	SL3467
MC85	1820-0965	Integrated Circuit, CTL	07263	SL3462
MC86,105,106,107	1820-0956	Integrated Circuit	07263	SL3459
R1 thru R30	0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4W	01121	CB2215
R31	0698-3443	Resistor, Fxd, Flm, 287 ohms, 1%, 1/8W	28480	0698-3443

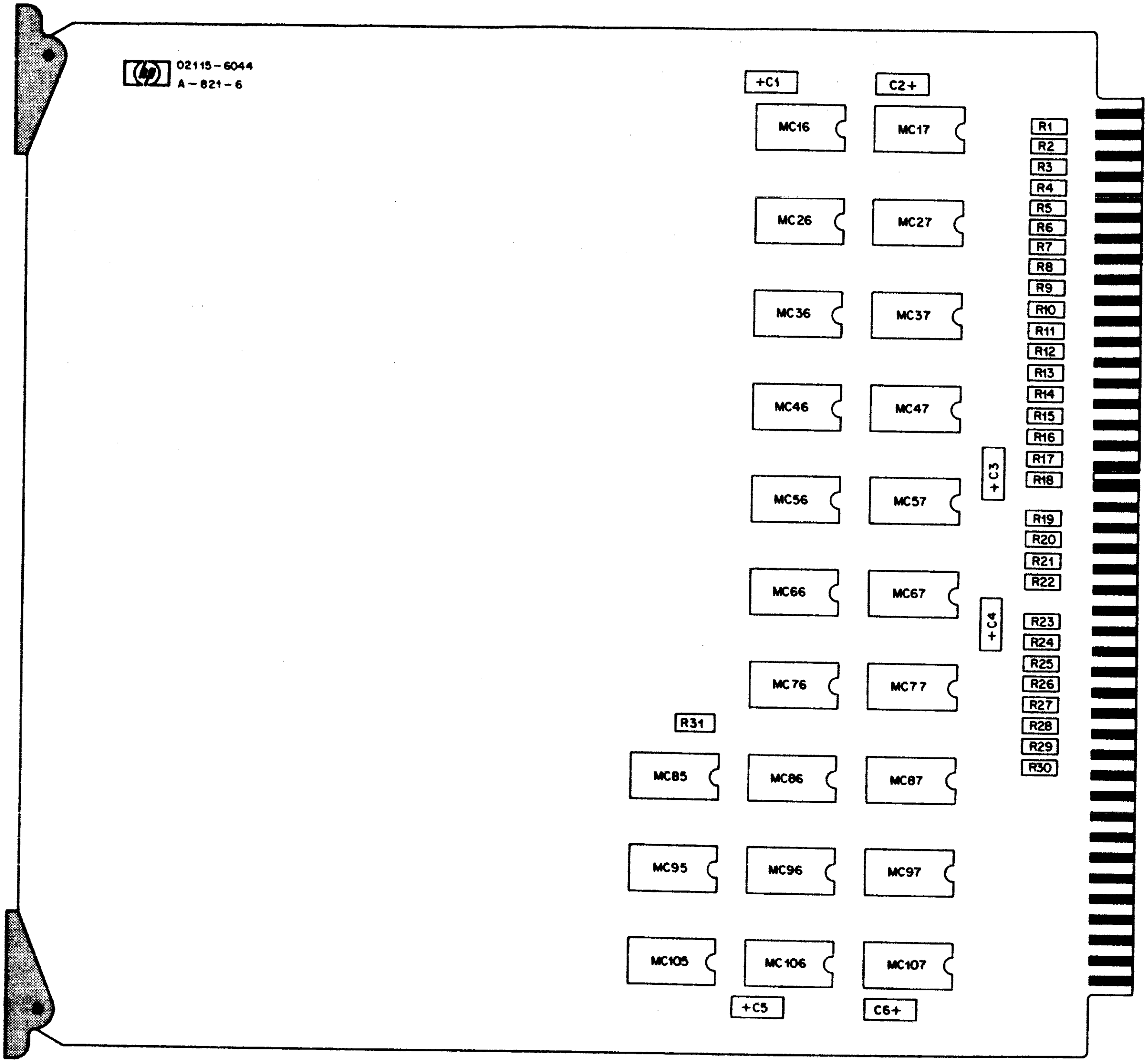
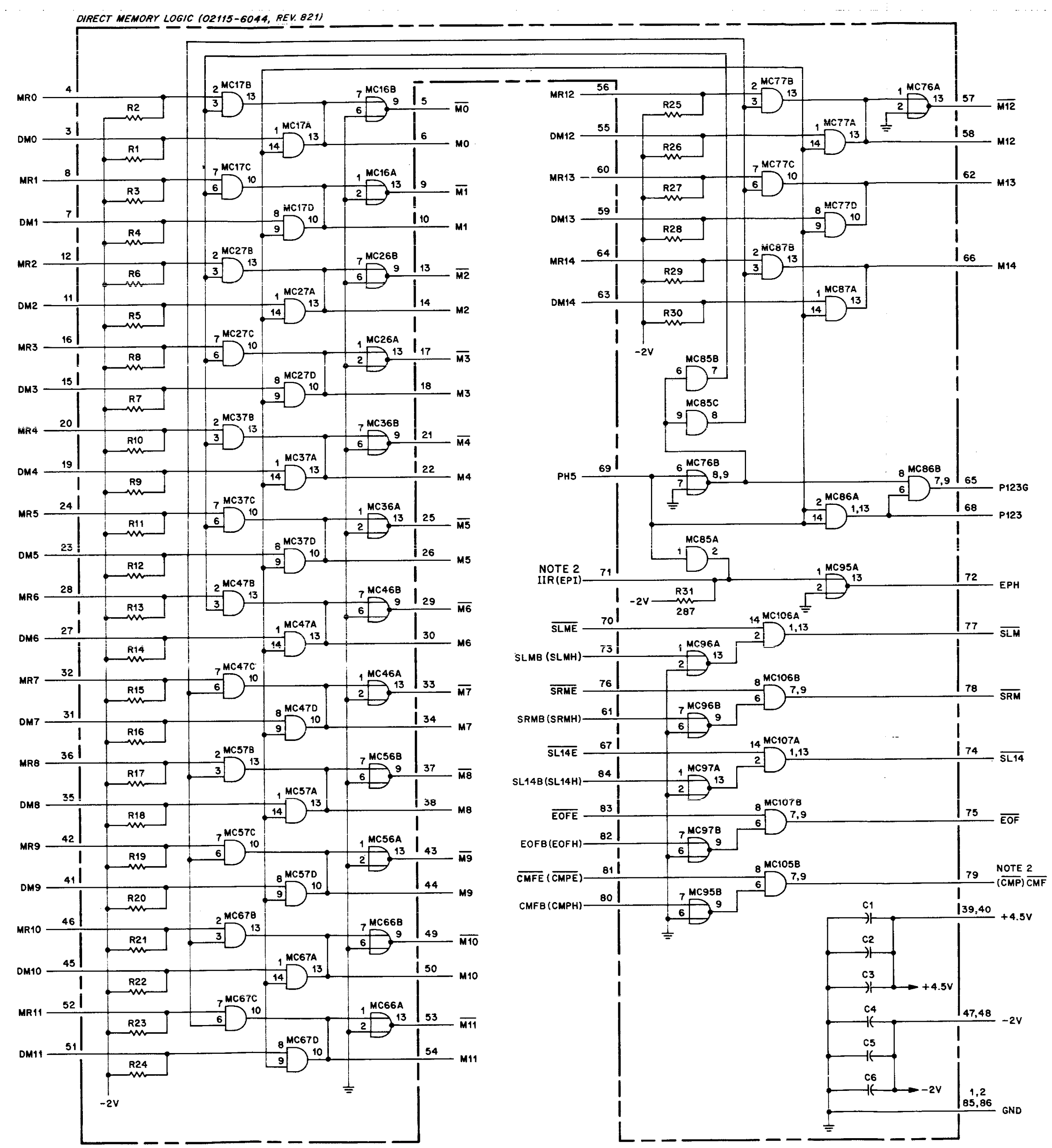


Figure 5-17A. A20 Direct Memory Logic Card (02115-6044), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	SIGNAL	REF NO.	PIN NO.	SIGNAL	REF NO.
1	GND	219	44	M9	15
2	GND	219	45	DM10	423
3	DM0	413	46	MR10	167
4	MR0	142	47	-2V	216
5	$\overline{M0}$	NC	48	-2V	216
6	M0	6	49	$\overline{M10}$	NC
7	DM1	414	50	M10	16
8	MR1	135	51	DM11	424
9	$\overline{M1}$	NC	52	MR11	162
10	M1	7	53	$\overline{M11}$	NC
11	DM2	415	54	M11	17
12	MR2	132	55	DM12	425
13	$\overline{M2}$	NC	56	MR12	194
14	M2	8	57	$\overline{M12}$	NC
15	DM3	416	58	M12	18
16	MR3	127	59	DM13	426
17	$\overline{M3}$	NC	60	MR13	187
18	M3	9	61	SRMB	407
19	DM4	417	62	M13	19
20	MR4	159	63	DM14	427
21	$\overline{M4}$	NC	64	MR14	184
22	M4	10	65	P123G	21
23	DM5	418	66	M14	473
24	MR5	153	67	$\overline{SL14E}$	46
25	$\overline{M5}$	NC	68	P123	91
26	M5	11	69	PH5	428
27	DM6	419	70	$\overline{SLME}$	40
28	MR6	150	71	IIR	411
29	$\overline{M6}$	NC	72	EPH	20
30	M6	12	73	SLMB	406
31	DM7	420	74	$\overline{SL14}$	23
32	MR7	145	75	$\overline{EOF}$	25
33	$\overline{M7}$	NC	76	$\overline{SRME}$	44
34	M7	13	77	$\overline{SLM}$	22
35	DM8	421	78	$\overline{SRM}$	24
36	MR8	177	79	$\overline{CMF}$	26
37	$\overline{M8}$	NC	80	CMFB	410
38	M8	14	81	$\overline{CMFE}$	63
39	+4.5V	217	82	EOFB	409
40	+4.5V	217	83	$\overline{EOFE}$	64
41	DM9	422	84	SL14B	408
42	MR9	170	85	GND	219
43	$\overline{M9}$	NC	86	GND	219

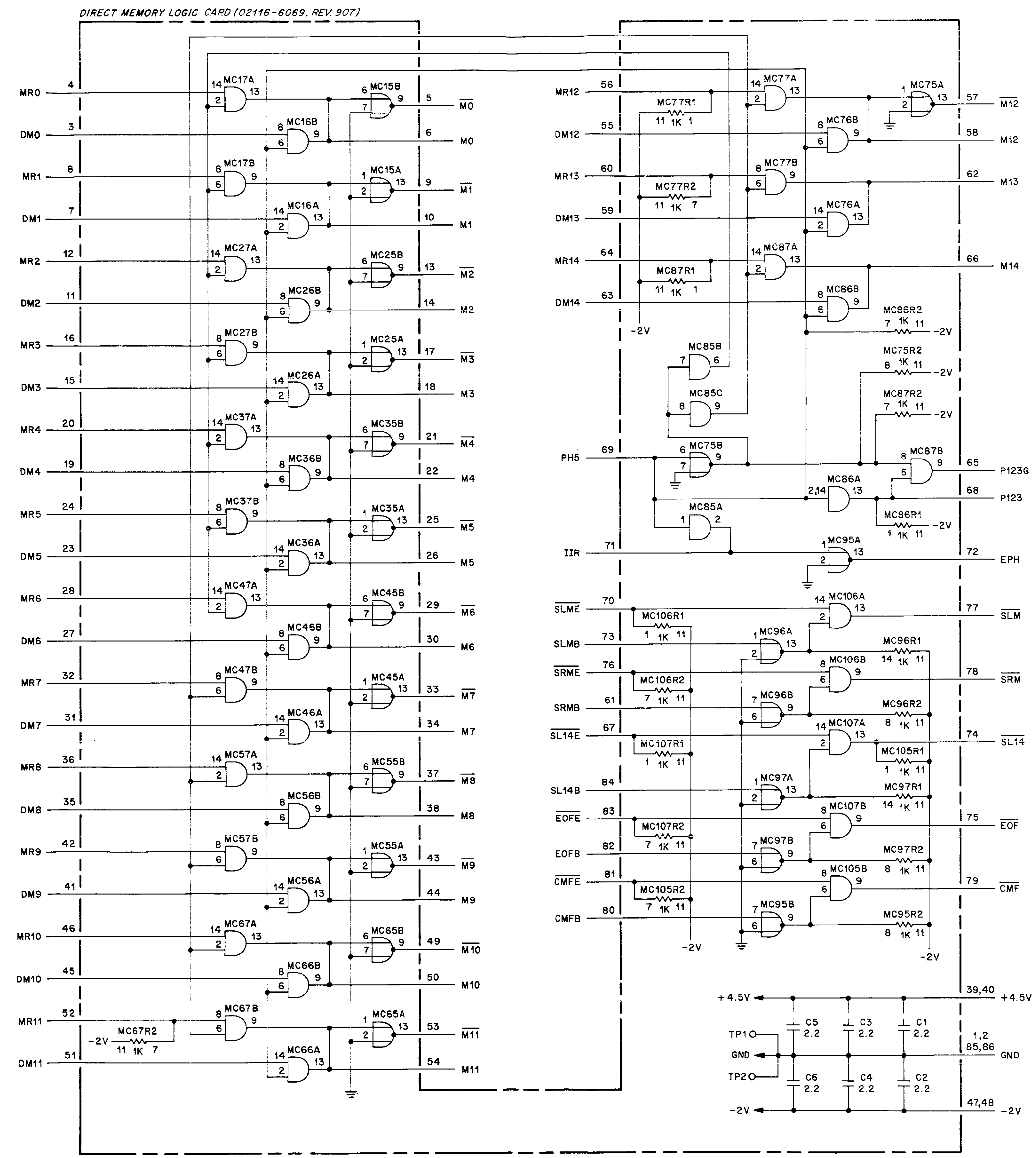


NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE 220 OHMS.
   ALL CAPACITANCE VALUES ARE 1.0UF
2. SIGNAL MNEMONICS WITHIN PARENTHESIS APPLY TO THE 2115A COMPUTER ONLY. THOSE MNEMONICS OUTSIDE THE PARENTHESIS APPLY TO BOTH THE 2115A AND 2116B COMPUTER.

Figure 5-17B. A20 Direct Memory Logic Card (02115-6044), Schematic Diagram

Pin Index (86 Pin Connector)

PIN NO.	SIGNAL	REF NO.	PIN NO.	SIGNAL	REF NO.
1	GND	219	44	M9	15
2	GND	219	45	DM10	423
3	DM0	413	46	MR10	167
4	MR0	142	47	-2V	216
5	$\overline{M0}$	NC	48	-2V	216
6	M0	6	49	$\overline{M10}$	NC
7	DM1	414	50	M10	16
8	MR1	135	51	DM11	424
9	$\overline{M1}$	NC	52	MR11	162
10	M1	7	53	$\overline{M11}$	NC
11	DM2	415	54	M11	17
12	MR2	132	55	DM12	425
13	$\overline{M2}$	NC	56	MR12	194
14	M2	8	57	$\overline{M12}$	NC
15	DM3	416	58	M12	18
16	MR3	127	59	DM13	426
17	$\overline{M3}$	NC	60	MR13	187
18	M3	9	61	SRMB	407
19	DM4	417	62	M13	19
20	MR4	159	63	DM14	427
21	$\overline{M4}$	NC	64	MR14	184
22	M4	10	65	P123G	21
23	DM5	418	66	M14	473
24	MR5	153	67	$\overline{SL14E}$	46
25	$\overline{M5}$	NC	68	P123	91
26	M5	11	69	PH5	428
27	DM6	419	70	$\overline{SLME}$	40
28	MR6	150	71	IIR	411
29	$\overline{M6}$	NC	72	EPH	20
30	M6	12	73	SLMB	406
31	DM7	420	74	$\overline{SL14}$	23
32	MR7	145	75	$\overline{EOF}$	25
33	$\overline{M7}$	NC	76	$\overline{SRME}$	44
34	M7	13	77	$\overline{SLM}$	22
35	DM8	421	78	$\overline{SRM}$	24
36	MR8	177	79	$\overline{CMF}$	26
37	$\overline{M8}$	NC	80	CMFB	410
38	M8	14	81	$\overline{CMFE}$	63
39	+4.5V	217	82	EOFB	409
40	+4.5V	217	83	$\overline{EOFE}$	64
41	DM9	422	84	SL14B	408
42	MR9	170	85	GND	219
43	$\overline{M9}$	NC	86	GND	219



NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTANCES ARE IN OHMS AND
ALL CAPACITANCES ARE IN MICROFARADS.

Figure 5-18. A20 Direct Memory Logic Card (02116-6069), Schematic Diagram

Table 5-15. A101 Front Panel Coupler Card (02116-6208), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 2	0180-0155	Capacitor, Fxd, Elect, 2.2 μf, 20%, 20VDCW	28480	0180-0155
C3	0160-0154	Capacitor, Fxd, Mica, 0.0022 μf, 10%, 200VDCW	56289	192P22292-PTS
MC16, 26, 36, 46, 56, 76, 86, 96	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC65, 75, 85, 95, 105, 115, 125	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC83, 93, 103	1820-0953	Integrated Circuit, CTL	07263	SL3456
R1 thru R3, R22 thru R34	0698-3400	Resistor, Fxd, Flm, 147 ohms, 1%, 1/2w	28480	0698-3400
R4 thru R21	0698-3399	Resistor, Fxd, Flm, 133 ohms, 1%, 1/2w	28480	0698-3399

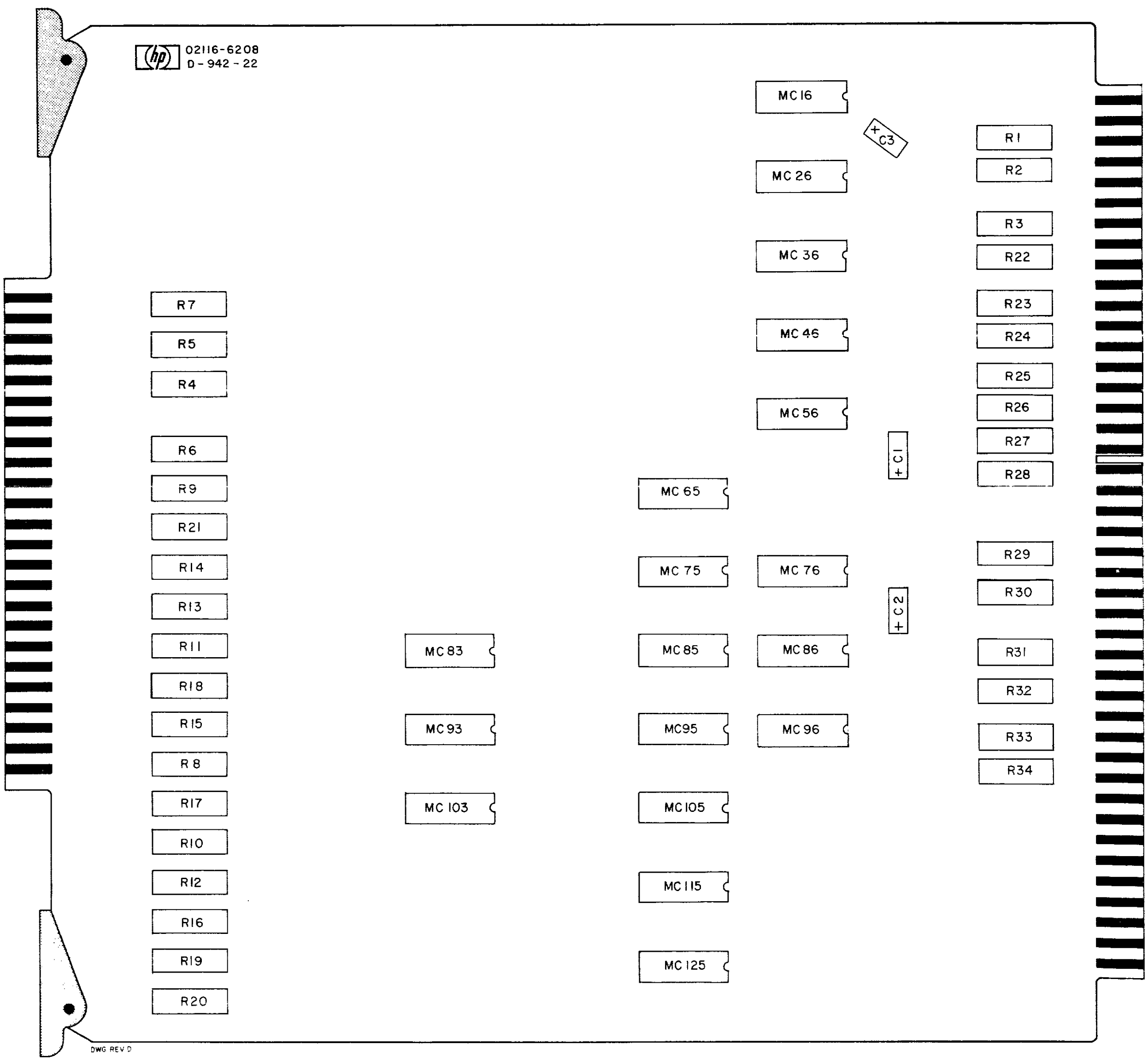


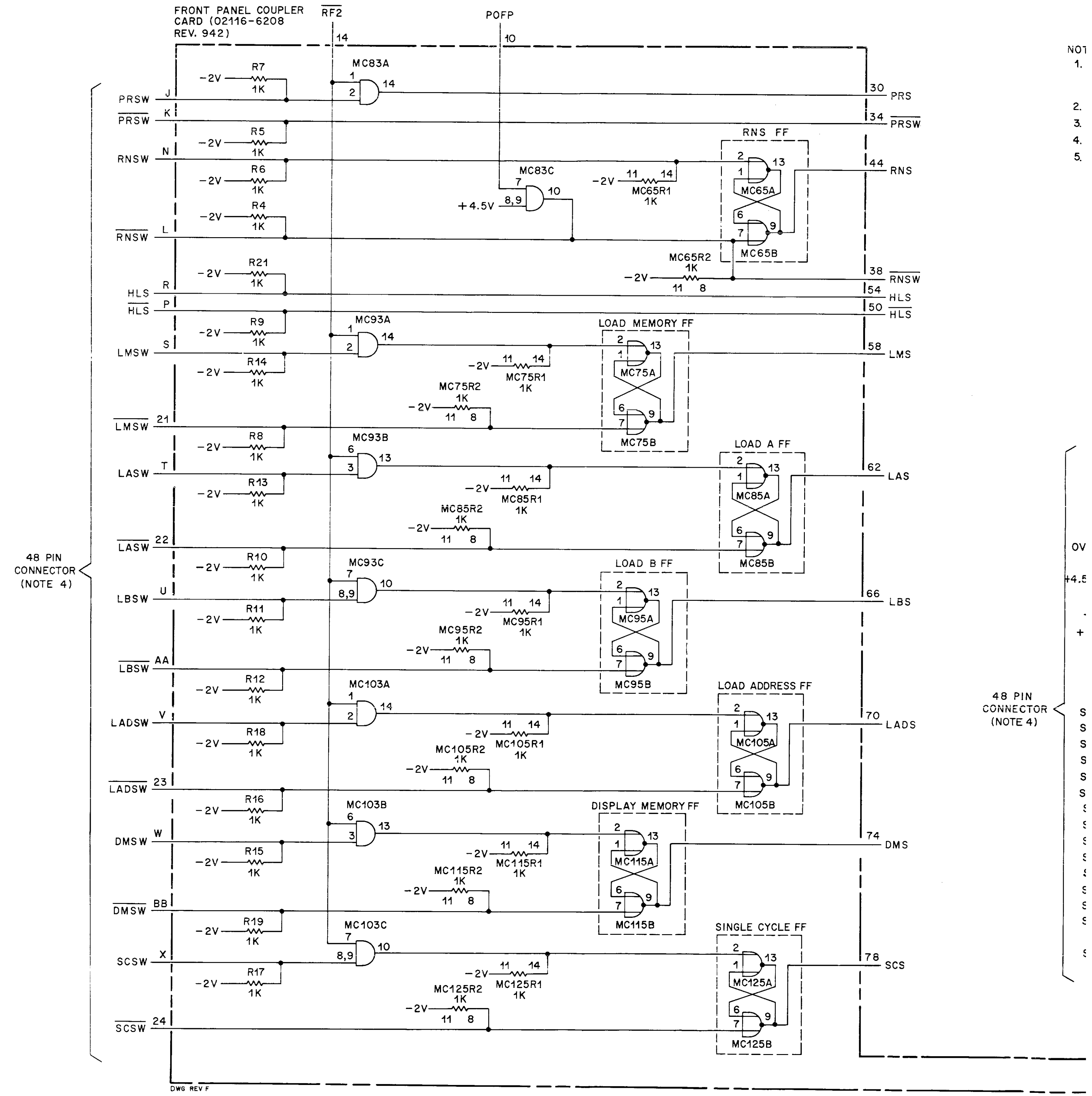
Figure 5-19. A101 Front Panel Coupler Card (02116-6208), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	SIGNAL	REF NO.	PIN NO.	SIGNAL	REF NO.
1	GND	219	44	RNS	358
2	GND	219	45	IOBI-10	322
3	IOBI-0	312	46	NC	-
4	OVF. IND.	29	47	-2V	216
5	NC	-	48	-2V	216
6	ISR	51	49	NC	-
7	IOBI-1	313	50	$\overline{\text{HLS}}$	359
8	NC	-	51	IOBI-11	323
9	NC	-	52	NC	-
10	POFP	354	53	NC	-
11	IOBI-2	314	54	HLS	360
12	NC	-	55	IOBI-12	324
13	NC	-	56	NC	-
14	$\overline{\text{RF2}}$	114	57	NC	-
15	IOBI-3	315	58	LMS	361
16	NC	-	59	IOBI-13	325
17	NC	-	60	NC	-
18	PNS	350	61	NC	-
19	IOBI-4	316	62	LAS	362
20	NC	-	63	IOBI-14	326
21	NC	-	64	NC	-
22	MNS	351	65	NC	-
23	IOBI-5	317	66	LBS	363
24	NC	-	67	IOBI-15	327
25	NC	-	68	NC	-
26	ILS	352	69	NC	-
27	IOBI-6	318	70	LADS	364
28	NC	-	71	PON	353
29	NC	-	72	NC	-
30	PRS	355	73	NC	-
31	IOBI-7	319	74	DMS	365
32	NC	-	75	PIND	368
33	NC	-	76	NC	-
34	$\overline{\text{PRSW}}$	356	77	NC	-
35	IOBI-8	320	78	SCS	366
36	NC	-	79	5.6V	369
37	NC	-	80	NC	-
38	$\overline{\text{RNSW}}$	-	81	NC	-
39	+4.5V	217	82	LPS	367
40	+4.5V	217	83	E. IND.	34
41	IOBI-9	321	84	+4.5/-5.6V	217
42	NC	-	85	GND	219
43	NC	-	86	GND	219

Pin Index (48 Pin Connector)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	SWR0	A	OVF. IND.
2	SWR1	B	-2V
3	SWR2	C	+4.5V
4	SWR3	D	+4.5V
5	SWR4	E	PNS
6	SWR5	F	MNS
7	SWR6	H	ILS
8	SWR7	J	PRSW
9	SWR8	K	$\overline{\text{PRSW}}$
10	SWR9	L	$\overline{\text{RNSW}}$
11	SWR10	M	+4.5V
12	SWR11	N	RNSW
13	SWR12	P	$\overline{\text{HLS}}$
14	SWR13	R	HLS
15	SWR14	S	LMSW
16	SWR15	T	LASW
17	PON	U	LBSW
18	PIND	V	LADSW
19	-5.6V	W	DMSW
20	EIND	X	SCSW
21	$\overline{\text{LMSW}}$	Y	LPS
22	$\overline{\text{LASW}}$	Z	+4.5V/-5.6V
23	$\overline{\text{LADSW}}$	AA	$\overline{\text{LBSW}}$
24	$\overline{\text{SCSW}}$	BB	$\overline{\text{DMSW}}$



NOTE:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
2. RESISTORS R4 THRU R21 ARE 133 OHMS.
3. REFER TO OVERALL INTERCONNECTION DIAGRAM FOR WIRING CONNECTION.
4. REFER TO DOOR ASSEMBLY SCHEMATIC DIAGRAM FOR CONNECTIONS.
5. UNLESS OTHERWISE INDICATED ALL CARD CONNECTIONS ARE TO THE 86-PIN CONNECTOR.

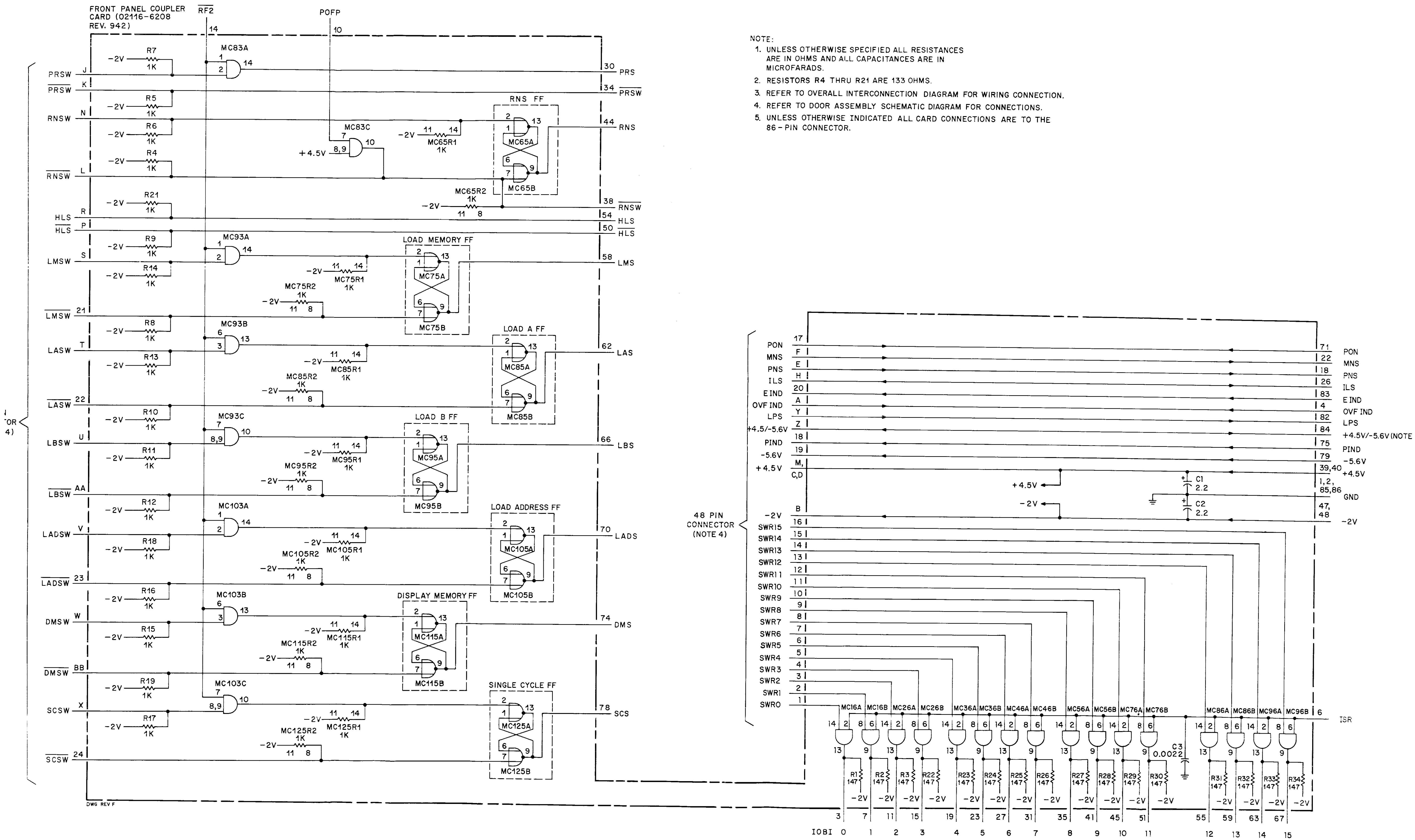


Figure 5-20. A101 Front Panel Coupler Card (02116-6208), Schematic Diagram

Table 5-16. A102, A103, A104, A105 Arithmetic Logic Card (02116-6026), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C6	0180-0155	Capacitor, Fxd, Elect, 2.2 μf, 20%, 20VDCW	28480	0180-0155
MC13, 14, 23, 24, 33, 43, 44, 53, 54, 63, 73, 74, 83, 84, 93, 103, 104, 113, 114, 123	1820-0967	Integrated Circuit, CTL	07263	SL3464
MC15, 16, 27, 36, 37 45, 46, 57, 66, 67, 75, 76, 87, 96, 97, 105, 106, 117, 126, 127	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC17, 77, 107	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC25, 26, 55, 56, 85, 86, 115, 116	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC34, 64, 94, 124	1820-0966	Integrated Circuit, CTL	07263	SL3463
MC35, 65, 95, 125	1820-0971	Integrated Circuit, CTL	07263	SL3467
MC47	1820-0954	Integrated Circuit, CTL	07263	SL3457
Q1 thru Q20	1854-0246	Transistor, Si, NPN	07263	2N3643
R1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB4715
R2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39	0683-6805	Resistor, Fxd, Comp, 68 ohms, 5%, 1/4w	01121	CB6805
R41 thru R44	0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4w	01121	CB2215

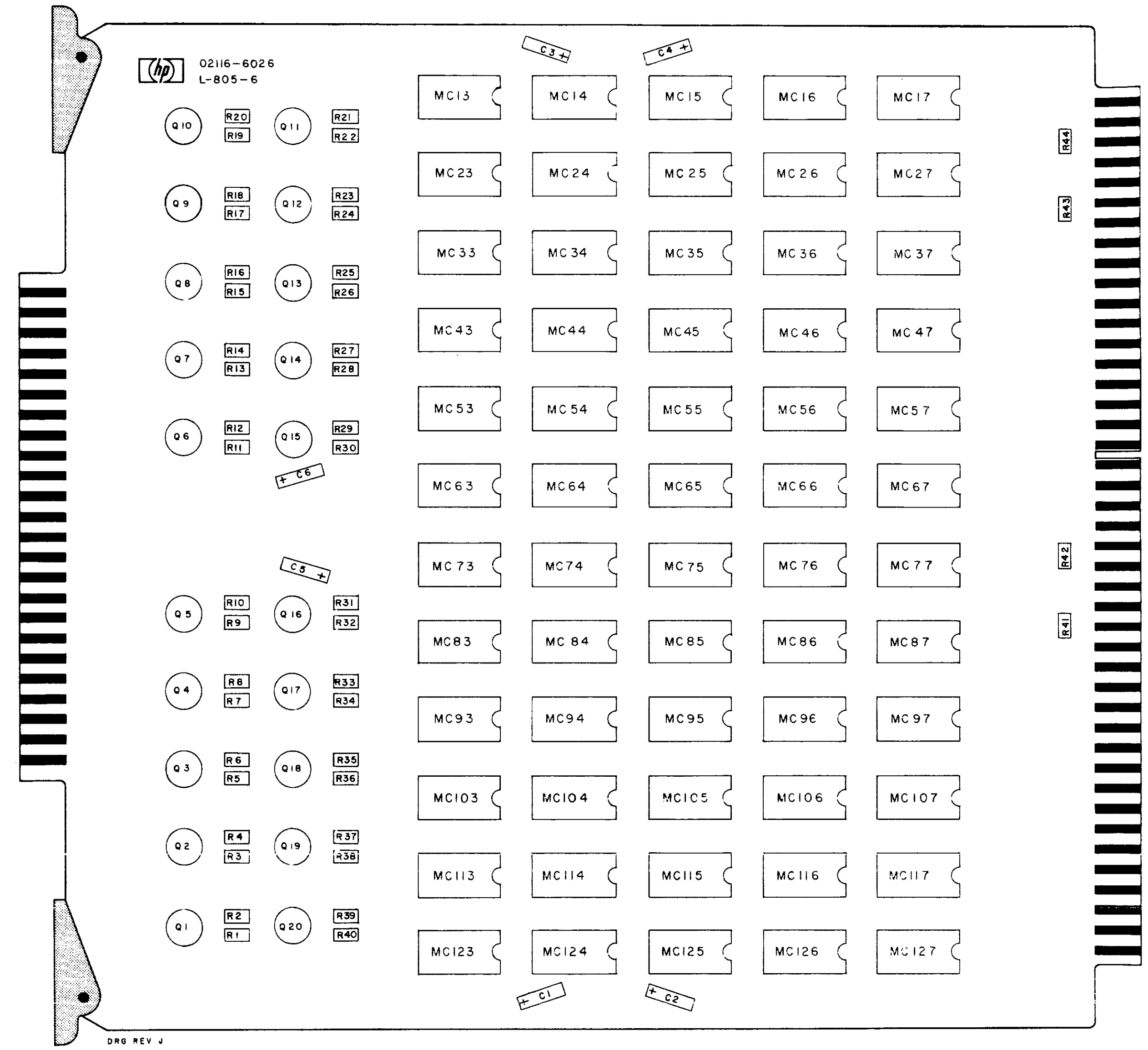


Figure 5-21. A102, A103, A104, and A105 Arithmetic Logic Card (02116-6026), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	A102 SIGNAL	A102 REF NO.	A103 SIGNAL	A103 REF NO.	A104 SIGNAL	A104 REF NO.	A105 SIGNAL	A105 REF NO.
1	GND	219	GND	219	GND	219	GND	219
2	GND	219	GND	219	GND	219	GND	219
3	NC	—	NC	—	NC	—	NC	—
4	ST13	240	ST9	236	ST5	232	ST1	228
5	ADF	65	ADF	65	ADF	65	ADF	65
6	SB15	195	SB11	—	SB7	—	SB3	—
7	RST	79	RST	79	RST	79	RST	79
8	RMSB	82	RMSB	82	RMSB	82	RMSB	82
9	TR13	178	TR9	160	TR5	143	TR1	125
10	$\overline{\text{TR13}}$	185	$\overline{\text{TR9}}$	168	$\overline{\text{TR5}}$	151	$\overline{\text{TR1}}$	133
11	ST15	242	ST11	238	ST7	234	ST3	230
12	RPRB	83	RPRB	83	RPRB	83	RPRB	83
13	TB13	211	TB9	207	TB5	203	TB1	199
14	RSM(10-15)	56	RSM(6-9)	70	NC	—	NC	—
15	$\overline{\text{TR15}}$	179	$\overline{\text{TR11}}$	161	$\overline{\text{TR7}}$	144	$\overline{\text{TR3}}$	126
16	TR15	186	TR11	169	TR7	152	TR3	134
17	TB15	213	TB11	209	TB7	205	TB3	201
18	MR13	187	MR9	170	MR5	153	MR1	135
19	$\overline{\text{MR13}}$	—	$\overline{\text{MR9}}$	491	$\overline{\text{MR5}}$	487	$\overline{\text{MR1}}$	483
20	RTSB	85	RTSB	85	RTSB	85	RTSB	85
21	RSM(10-15)	56	RSM(10-15)	56	RSM(6-9)	70	NC	—
22	STM(12-15)	96	STM(10-11)	59	STM(6-9)	58	STM(0-5)	73
23	STP(12-15)	68	STP(0-9)	55	STP(0-9)	55	STP(0-9)	55
24	NC	—	$\overline{\text{MR11}}$	493	$\overline{\text{MR7}}$	489	$\overline{\text{MR3}}$	485
25	MR15	127	MR11	162	MR7	145	MR3	127
26	STBB	60	STBB	60	STBB	60	STBB	60
27	IOBI 15	327	IOBI 11	323	IOBI 7	319	IOBI 3	315
28	RBRB	72	RBRB	72	RBRB	72	RBRB	72
29	STM(12-15)	96	STM(6-9)	58	STM(0-5)	73	STM(0-5)	73
30	RB15	196	RB11	—	RB7	—	RB3	—
31	IOI	33	IOI	33	IOI	33	IOI	33
32	IOBI 13	325	IOBI 9	321	IOBI 5	317	IOBI 1	313
33	IOBI 14	326	IOBI 10	322	IOBI 6	318	IOBI 2	314
34	RARB	57	RARB	57	RARB	57	RARB	57
35	IOBO 15	180	IOBO 11	163	IOBO 7	146	IOBO 3	128
36	C16	188	C12	171	C8	154	C4	136
37	RB12	—	RB8	—	RB4	—	RB0	61
38	STBA	77	STBA	77	STBA	77	STBA	77
39	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
40	+4.5V	217	+4.5V	217	+4.5V	217	+4.5V	217
41	$\overline{\text{RLL}}$	47	$\overline{\text{SLM}}$	22	$\overline{\text{SLM}}$	22	$\overline{\text{SLM}}$	22
42	SB12	—	SB8	—	SB4	—	SB0	67
43	TAN4	181	TAN3	164	TAN2	147	TAN1	129
44	STP(12-15)	68	STP(10-11)	52	STP(0-9)	55	STP(0-9)	55
45	TB3	201	TB15	213	TB11	209	TB7	205
46	NC	—	NC	—	NC	—	NC	—
47	-2V	216	-2V	216	-2V	216	-2V	216
48	-2V	216	-2V	216	-2V	216	-2V	216
49	ST12	239	ST8	235	ST4	231	ST0	227
50	IOBO 13	189	IOBO 9	172	IOBO 5	155	IOBO 1	137
51	STBT	62	STBT	62	STBT	62	STBT	62
52	ST14	241	ST10	237	ST6	233	ST2	229
53	$\overline{\text{TR14}}$	182	$\overline{\text{TR10}}$	165	$\overline{\text{TR6}}$	148	$\overline{\text{TR2}}$	130
54	$\overline{\text{TR12}}$	190	$\overline{\text{TR8}}$	173	$\overline{\text{TR4}}$	156	$\overline{\text{TR0}}$	138

Figure 5-22. A102, A103, A104, and A105 Arithmetic Logic Card (62116-6026), Schematic Diagram (Sheet 1 of 3)

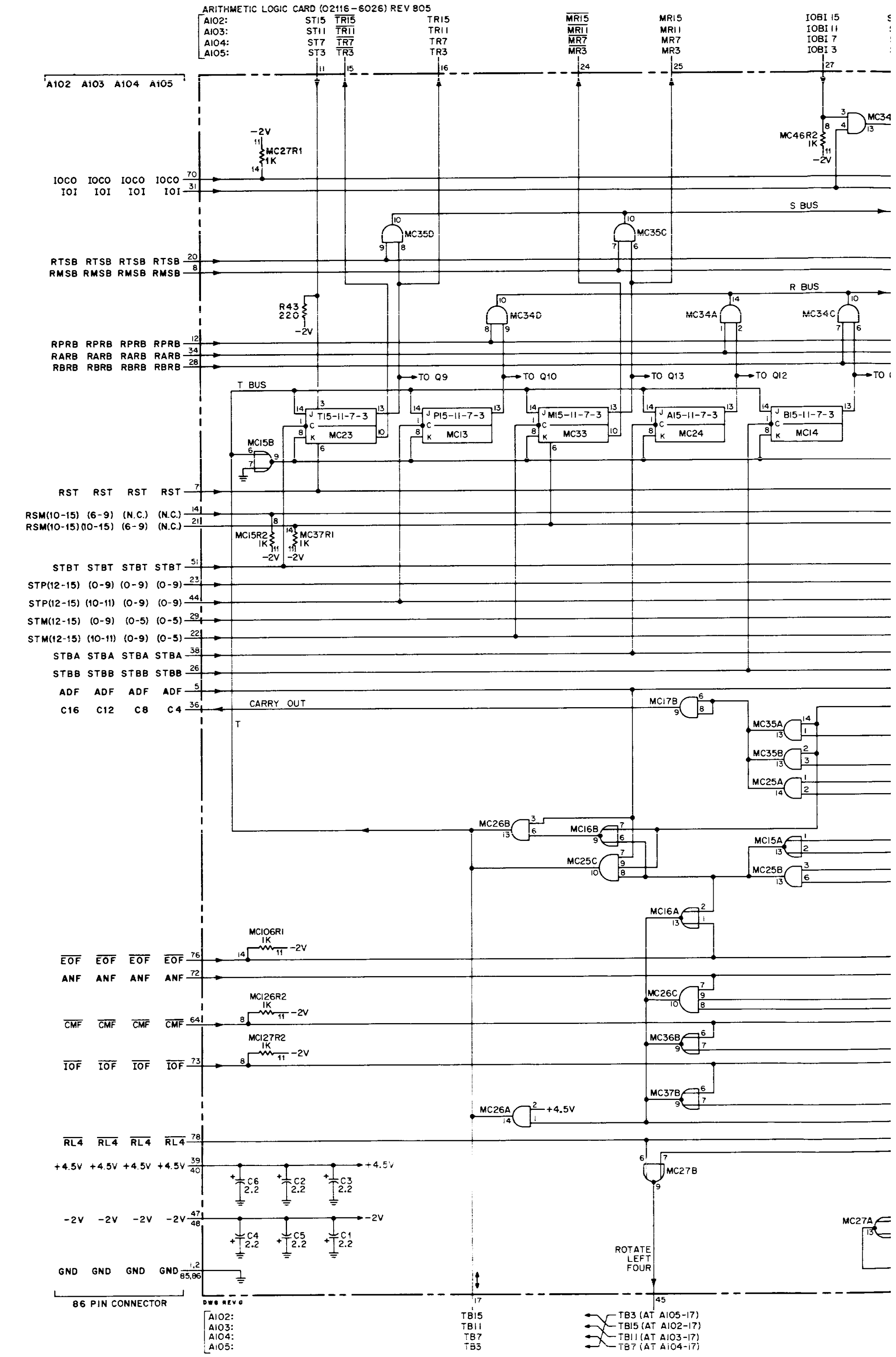
Pin Index (86 Pin Connector) (Continued)

PIN NO.	A102 SIGNAL	A102 REF NO.	A103 SIGNAL	A103 REF NO.	A104 SIGNAL	A104 REF NO.	A105 SIGNAL	A105 REF NO.
55	TB14	212	TB10	208	TB6	204	TB2	200
56	TR14	191	TR10	174	TR6	95	TR2	139
57	IOBO 14	183	IOBO 10	166	IOBO 6	149	IOBO 2	131
58	TR12	192	TR8	175	TR4	157	TR0	140
59	SB13	—	SB9	—	SB5	—	SB1	—
60	IOBO 12	193	IOBO 8	176	IOBO 4	158	IOBO 0	141
61	SB14	—	SB10	—	SB6	—	SB2	—
62	RB13	—	RB9	—	RB5	—	RB1	—
63	$\overline{\text{MR12}}$	495	$\overline{\text{MR8}}$	492	$\overline{\text{MR4}}$	488	$\overline{\text{MR0}}$	484
64	$\overline{\text{CMF}}$	26	$\overline{\text{CMF}}$	26	$\overline{\text{CMF}}$	26	$\overline{\text{CMF}}$	26
65	MR14	184	MR10	167	MR6	150	MR2	132
66	$\overline{\text{MR14}}$	—	$\overline{\text{MR10}}$	494	$\overline{\text{MR6}}$	490	$\overline{\text{MR2}}$	486
67	C12	171	C8	154	C4	136	C0	37
68	MR12	194	MR8	177	MR4	159	MR0	142
69	TB12	210	TB8	206	TB4	202	TB0	198
70	IOCO	45	IOCO	45	IOCO	45	IOCO	45
71	RB14	197	RB10	—	RB6	—	RB2	—
72	ANF	78	ANF	78	ANF	78	ANF	78
73	$\overline{\text{IOF}}$	86	$\overline{\text{IOF}}$	86	$\overline{\text{IOF}}$	86	$\overline{\text{IOF}}$	86
74	$\overline{\text{SRM}}$	24	$\overline{\text{SRM}}$	24	$\overline{\text{SRM}}$	24	$\overline{\text{SRM}}$	24
75	TB1	199	TB13	211	TB9	207	TB5	203
76	$\overline{\text{EOF}}$	25	$\overline{\text{EOF}}$	25	$\overline{\text{EOF}}$	25	$\overline{\text{EOF}}$	25
77	TB11	209	TB7	205	TB3	201	TB15	213
78	$\overline{\text{RL4}}$	43	$\overline{\text{RL4}}$	43	$\overline{\text{RL4}}$	43	$\overline{\text{RL4}}$	43
79	IOBI 12	324	IOBI 8	320	IOBI 4	316	IOBI 0	312
80	$\overline{\text{SLM}}$	22	$\overline{\text{SLM}}$	22	$\overline{\text{SLM}}$	22	$\overline{\text{SLM}}$	22
81	TB0	198	TB12	210	TB8	206	TB1	202
82	$\overline{\text{SL14}}$	23	$\overline{\text{SLM}}$	22	$\overline{\text{SLM}}$	22	$\overline{\text{SLM}}$	22
83	$\overline{\text{SRM}}$	24	$\overline{\text{SRM}}$	24	$\overline{\text{SRM}}$	24	$\overline{\text{RRS}}$	35
84	TB2	200	TB14	212	TB10	208	TB6	204
85	GND	219	GND	219	GND	219	GND	219
86	GND	219	GND	219	GND	219	GND	219

Figure 5-22. A102, A103, A104, and A105 Arithmetic Logic Card (62116-6026), Schematic Diagram (Sheet 2 of 3)

Pin Index (48 Pin Connector)

PIN NO.	A102 SIGNAL	A103 SIGNAL	A104 SIGNAL	A105 SIGNAL
1	GND	GND	GND	GND
2	GND	GND	GND	GND
3	BRD15	BRD11	BRD7	BRD3
4	BRD14	BRD10	BRD6	BRD2
5	BRD13	BRD9	BRD5	BRD1
6	BRD12	BRD8	BRD4	BRD0
7	ARD12	ARD8	ARD4	ARD0
8	ARD13	ARD9	ARD5	ARD1
9	ARD14	ARD10	ARD6	ARD2
10	ARD15	ARD11	ARD7	ARD3
11	MRD12	MRD8	MRD4	MRD0
12	MRD13	MRD9	MRD5	MRD1
13	MRD15	MRD11	MRD7	MRD3
14	MRD14	MRD10	MRD6	MRD2
15	PRD12	PRD8	PRD4	PRD0
16	TRD15	TRD11	TRD7	TRD3
17	PRD15	PRD11	PRD7	PRD3
18	PRD13	PRD9	PRD5	PRD1
19	PRD14	PRD10	PRD6	PRD2
20	TRD14	TRD10	TRD6	TRD2
21	TRD12	TRD8	TRD4	TRD0
22	TRD13	TRD9	TRD5	TRD1
23	GND	GND	GND	GND
24	GND	GND	GND	GND
A	GND	GND	GND	GND
B	GND	GND	GND	GND
C	BRD15	BRD11	BRD7	BRD3
D	BRD14	BRD10	BRD6	BRD2
E	BRD13	BRD9	BRD5	BRD1
F	BRD12	BRD8	BRD4	BRD1
H	ARD12	ARD8	ARD4	ARD0
J	ARD13	ARD9	ARD5	ARD1
K	ARD14	ARD10	ARD6	ARD2
L	ARD15	ARD11	ARD7	ARD3
M	MRD12	MRD8	MRD4	MRD0
N	MRD13	MRD9	MRD5	MRD1
P	MRD15	MRD11	MRD7	MRD3
R	MRD14	MRD10	MRD6	MRD2
S	PRD12	PRD8	PRD4	PRD0
T	TRD15	TRD11	TRD7	TRD3
U	PRD15	PRD11	PRD7	PRD3
V	PRD13	PRD9	PRD5	PRD1
W	PRD14	PRD10	PRD6	PRD2
X	TRD14	TRD10	TRD6	TRD2
Y	TRD12	TRD8	TRD4	TRD0
Z	TRD13	TRD9	TRD5	TRD1
AA	GND	GND	GND	GND
BB	GND	GND	GND	GND



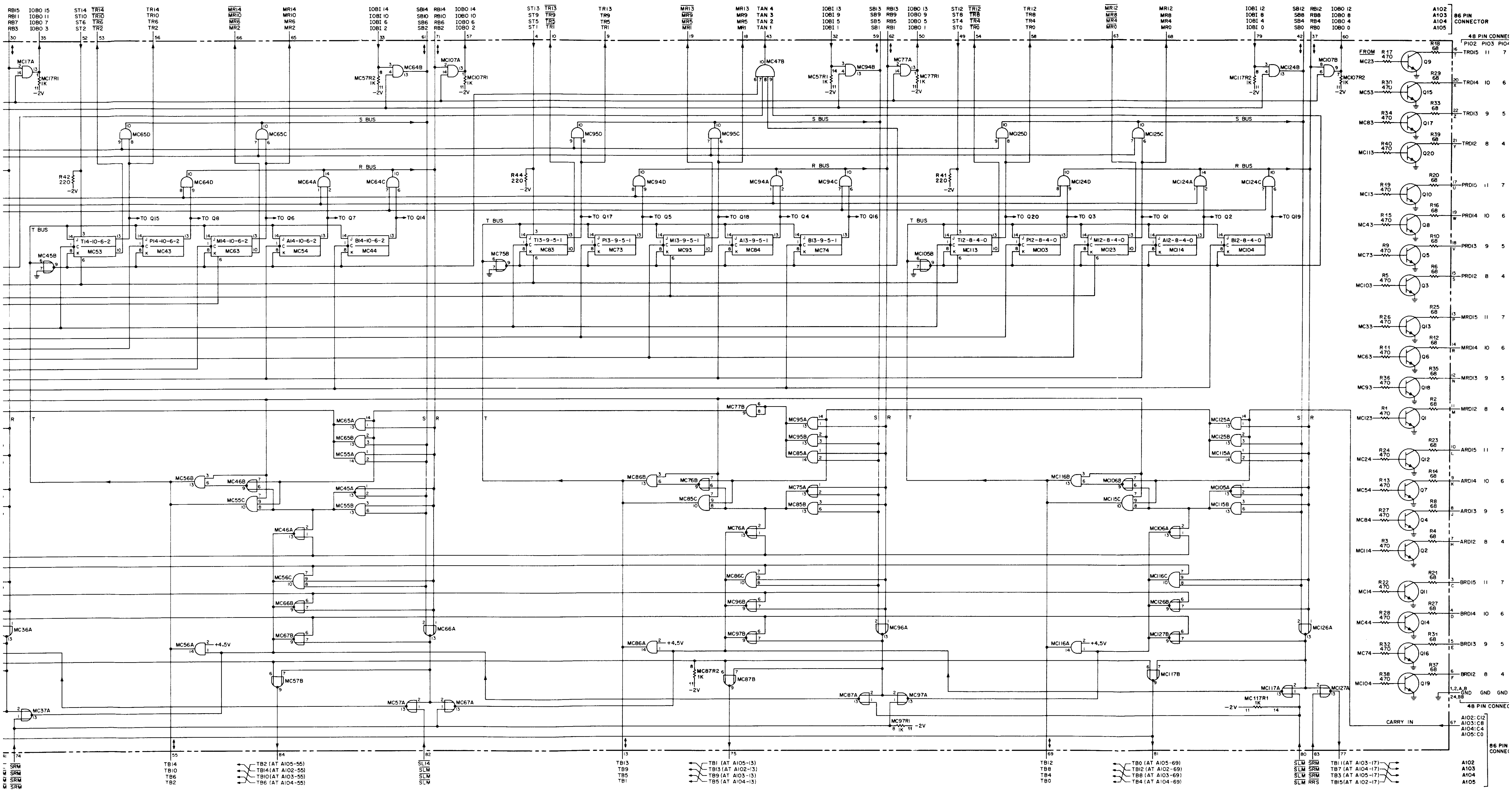
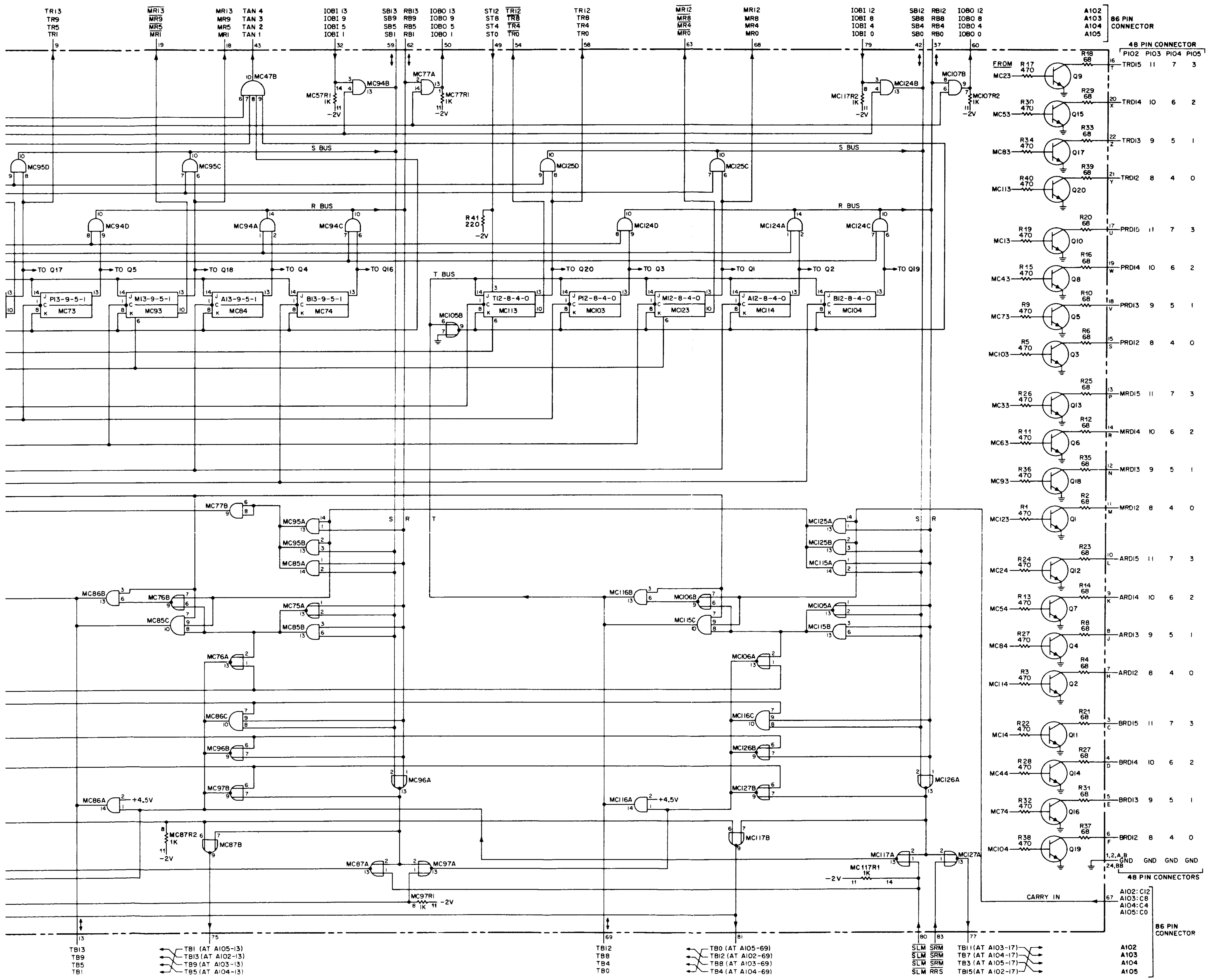


Figure 5-22. A102, A103, A104, and A105 Arithmet (62116-6026), Schematic Diagram (Sheet



NOTE:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.

Figure 5-22. A102, A103, A104, and A105 Arithmetic Logic Card (02116-6026), Schematic Diagram (Sheet 3 of 3)

Table 5-17. A106 Timing Generator Card (02116-6281), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 3	0140-0192	Capacitor, Fxd, Mica, 68 pf, 5%	28480	0140-0192
C2	0160-2055	Capacitor, Fxd, Cer, 0.01 μf, +80 -20%, 100VDCW	56289	C023F101F103-ZE12CDH
C4	0160-2588	Capacitor, Fxd, Cer, 1000 pf, 5%, 50VDCW	28480	0160-2588
C5	0160-0363	Capacitor, Fxd, Mica, 620 pf, 5%	28480	0160-0363
C6	0140-0197	Capacitor, Fxd, Mica, 180 pf, 5%, 300VDCW	04062	RDM15F181J3C
C7 thru C10	0180-0155	Capacitor, Fxd, Elect, 2.2 μf, 20%, 20VDCW	28480	0180-0155
C11	0140-0210	Capacitor, Fxd, Mica, 270 pf, 5%	28480	0140-0210
C12	0140-0225	Capacitor, Fxd, Mica, 300 pf, 1%	28480	0140-0225
CR1	1910-0022	Diode, Germanium, 5 WIV	28480	1910-0022
L1	9140-0107	Coil, Fxd, RF, 27 MH, 10%	99800	1840-38
MC12, 23, 45, 46, 52, 55, 64, 87, 97, 115, 124, 127	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC13, 15, 17, 37, 42, 57, 67, 73, 75, 83, 93, 103, 113, 114, 123	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC14, 24, 34, 44, 72, 74, 82, 84	1820-0967	Integrated Circuit, CTL	07263	SL3464
MC16, 22, 26, 27, 32, 33, 35, 36, 43, 53, 62, 76, 77, 104, 107, 117, 126	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC25, 54, 56, 86, 96, 106	1820-0965	Integrated Circuit, CTL	07263	SL3462
MC47, 63	1820-0954	Integrated Circuit, CTL	07263	SL3457
MC92, 94, 102, 112, 122	1820-0968	Integrated Circuit, CTL	07263	SL3466
MC116	1820-0971	Integrated Circuit, CTL	07263	SL3467
Q1 thru Q3	1854-0005	Transistor, Si, NPN	02735	2N708
Q4 thru Q9	1854-0246	Transistor, Si, NPN	07263	2N3643
R1	0683-3935	Resistor, Fxd, Comp, 39 k, 5%, 1/4w	01121	CB3935
R2	0683-8215	Resistor, Fxd, Comp, 820 ohms, 5%, 1/4w	01121	CB8215
R3	0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4w	01121	CB5115
R4	0683-4705	Resistor, Fxd, Comp, 47 ohms, 5%, 1/4w	01121	CB4705
R5	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4w	01121	CB1025
R6, 8, 10, 12, 14, 16	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB4715
R7, 9, 11, 13, 15, 17	0683-3305	Resistor, Fxd, Comp, 33 ohms, 5%, 1/4w	01121	CB3305
R18, 19, 22	0683-1515	Resistor, Fxd, Comp, 150 ohms, 5%, 1/4w	01121	CB1515
R20, 21	0683-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4w	01121	CB1015
R23	0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1%4w	01121	CB2215
W1	8159-0005	Jumper Wire	28480	8159-0005
Y1	0410-0035	Crystal, Quartz, 10 MC/S, 0.005%	28480	0410-0035

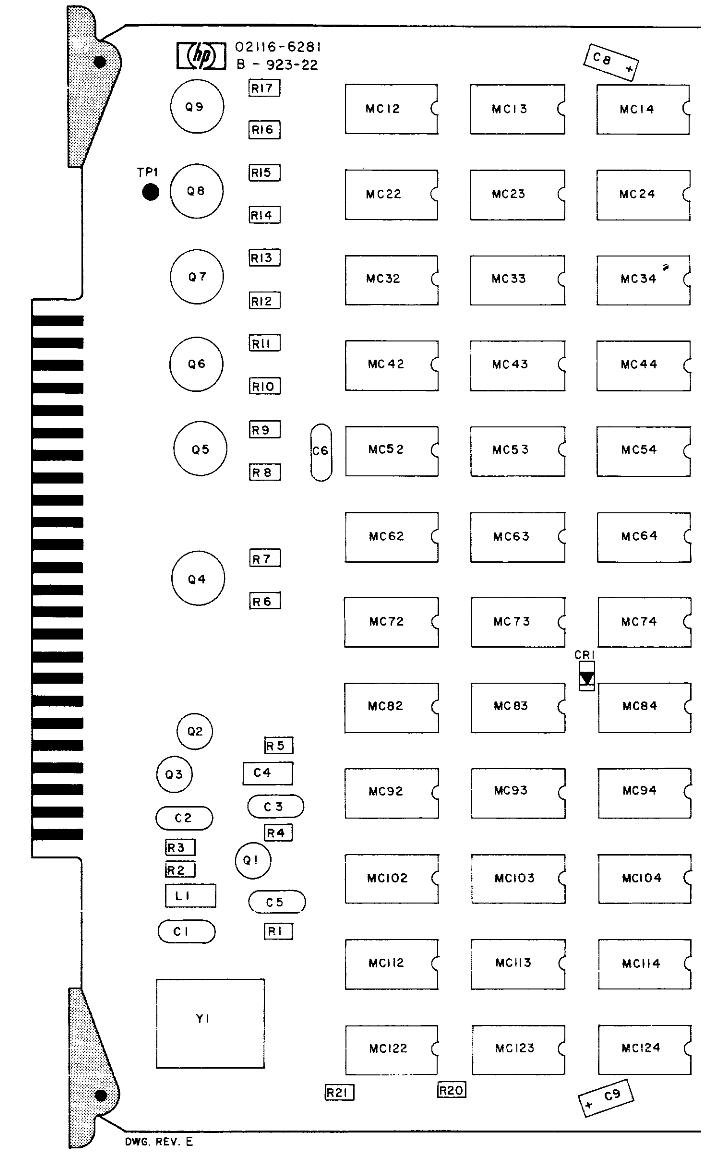


Figure 5-23. A106 Timing Generator Card (021

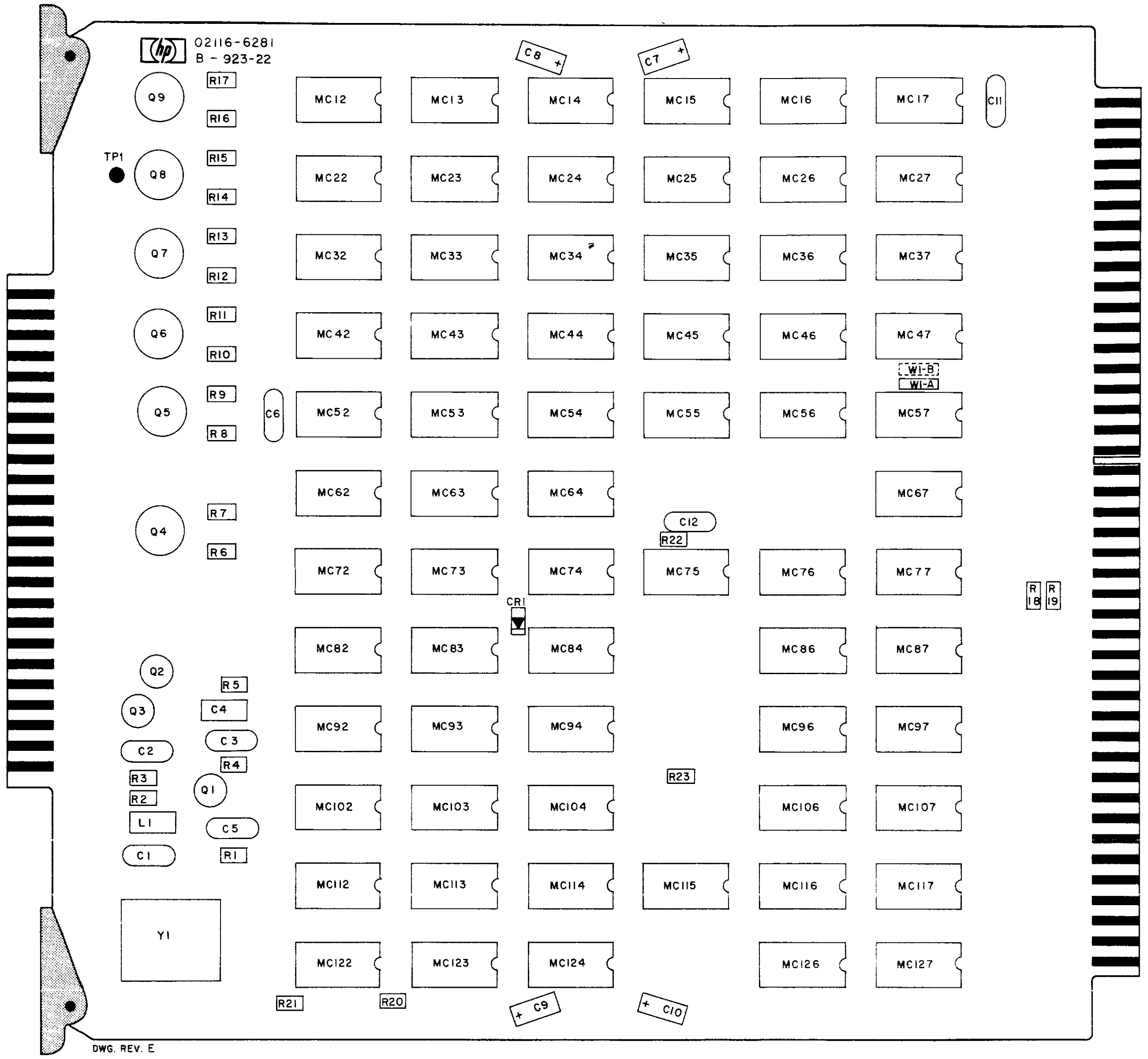


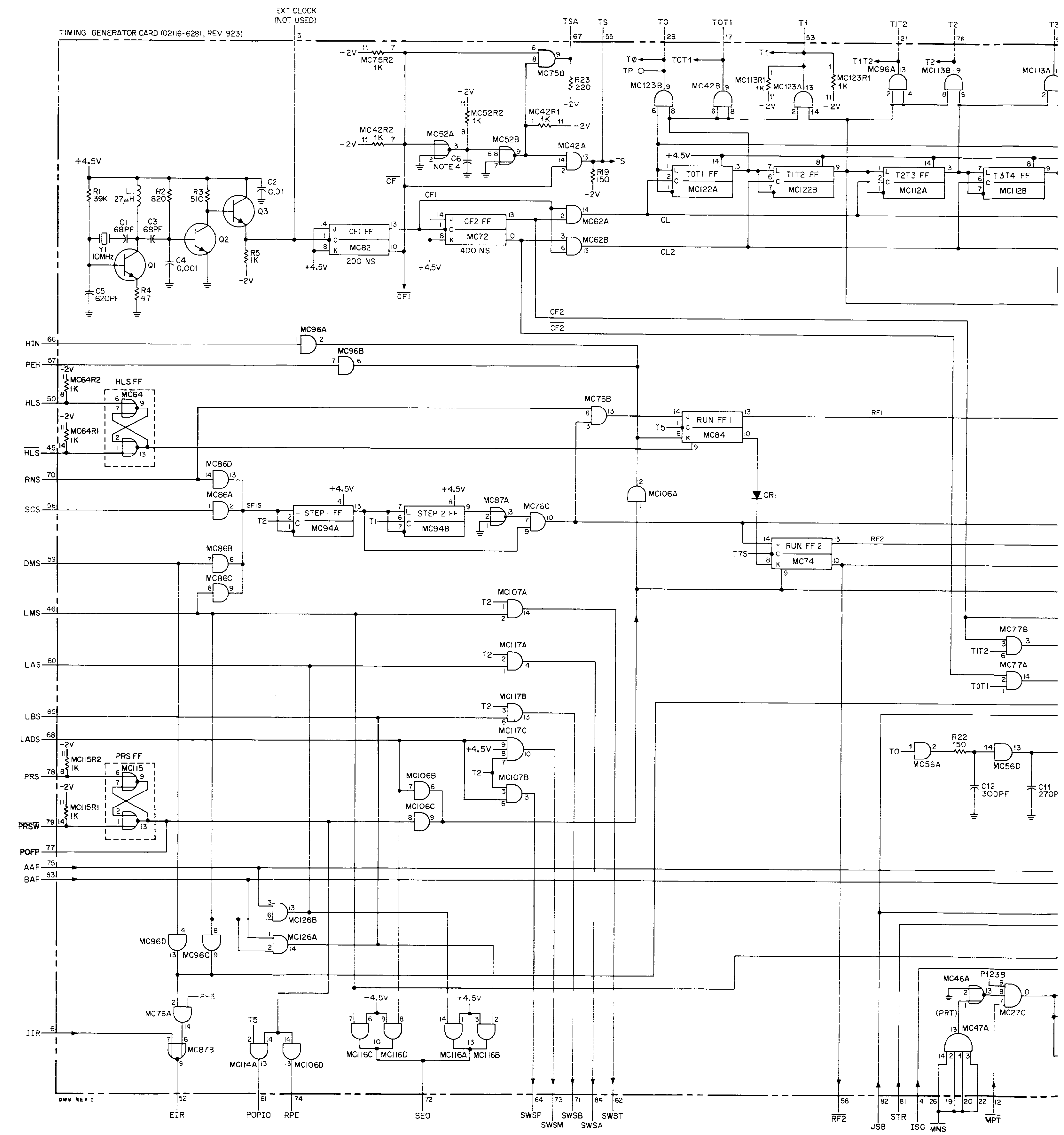
Figure 5-23. A106 Timing Generator Card (02116-6281), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	SIGNAL	REF NO.	PIN NO.	SIGNAL	REF NO.
1	GND	219	44	INT	257
2	GND	219	45	$\overline{\text{HLS}}$	359
3	NC	-	46	LMS	361
4	ISG	377	47	-2V	216
5	NC	-	48	-2V	216
6	IIR	411	49	$\overline{\text{IR15}}$	76
7	PEI	215	50	HLS	360
8	NC	-	51	T7S	99
9	NC	-	52	EIR	112
10	NC	-	53	T1	100
11	T6	122	54	T4	113
12	$\overline{\text{MPT}}$	476	55	TS	101
13	PH4	88	56	SCS	366
14	EPH	20	57	PEH	214
15	T3T4	89	58	$\overline{\text{RF2}}$	114
16	T4T5	107	59	DMS	365
17	T0T1	121	60	PH3	115
18	T7	108	61	POPIO	102
19	$\overline{\text{MNS}}$	475	62	SWST	116
20	$\overline{\text{MNS}}$	475	63	T3	103
21	T1T2	90	64	SWSP	117
22	$\overline{\text{MNS}}$	475	65	LBS	363
23	P123	91	66	HIN	42
24	ISZ	84	67	TSA	469
25	MIT	92	68	LADS	364
26	$\overline{\text{MNS}}$	475	69	T5	104
27	RPB	93	70	RNS	358
28	T0	109	71	SWSB	105
29	MRT	94	72	SEO	118
30	T6T7	110	73	SWSM	106
31	NC	-	74	NC	-
32	MST	111	75	AAF	38
33	MWL	123	76	T2	119
34	JMP	66	77	POFP	354
35	MWT	124	78	PRS	355
36	$\overline{\text{TR15}}$	179	79	$\overline{\text{PRSW}}$	356
37	PH2	97	80	LAS	362
38	TR15	186	81	STR	80
39	+4.5V	217	82	JSB	81
40	+4.5V	217	83	BAF	50
41	PH1	98	84	SWSA	120
42	$\overline{\text{OP0}}$	71	85	GND	219
43	PNS	350	86	GND	219

Pin Index (48 Pin Connector)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	GND	A	NC
2	GND	B	NC
3	FETCH	C	NC
4	INDIRECT	D	NC
5	EXECUTE	E	NC
6	PARITY	F	NC
	HALT	H	NC
7	RUN	J	NC
8	HALT	K	NC
9	NC	L	NC
10	NC	M	NC
11	NC	N	NC
12	NC	P	NC
13	NC	R	NC
14	NC	S	NC
15	NC	T	NC
16	NC	U	NC
17	NC	V	NC
18	NC	W	NC
19	NC	X	NC
20	NC	Y	NC
21	NC	Z	NC
22	NC	AA	NC
23	NC	BB	GND
24	GND		



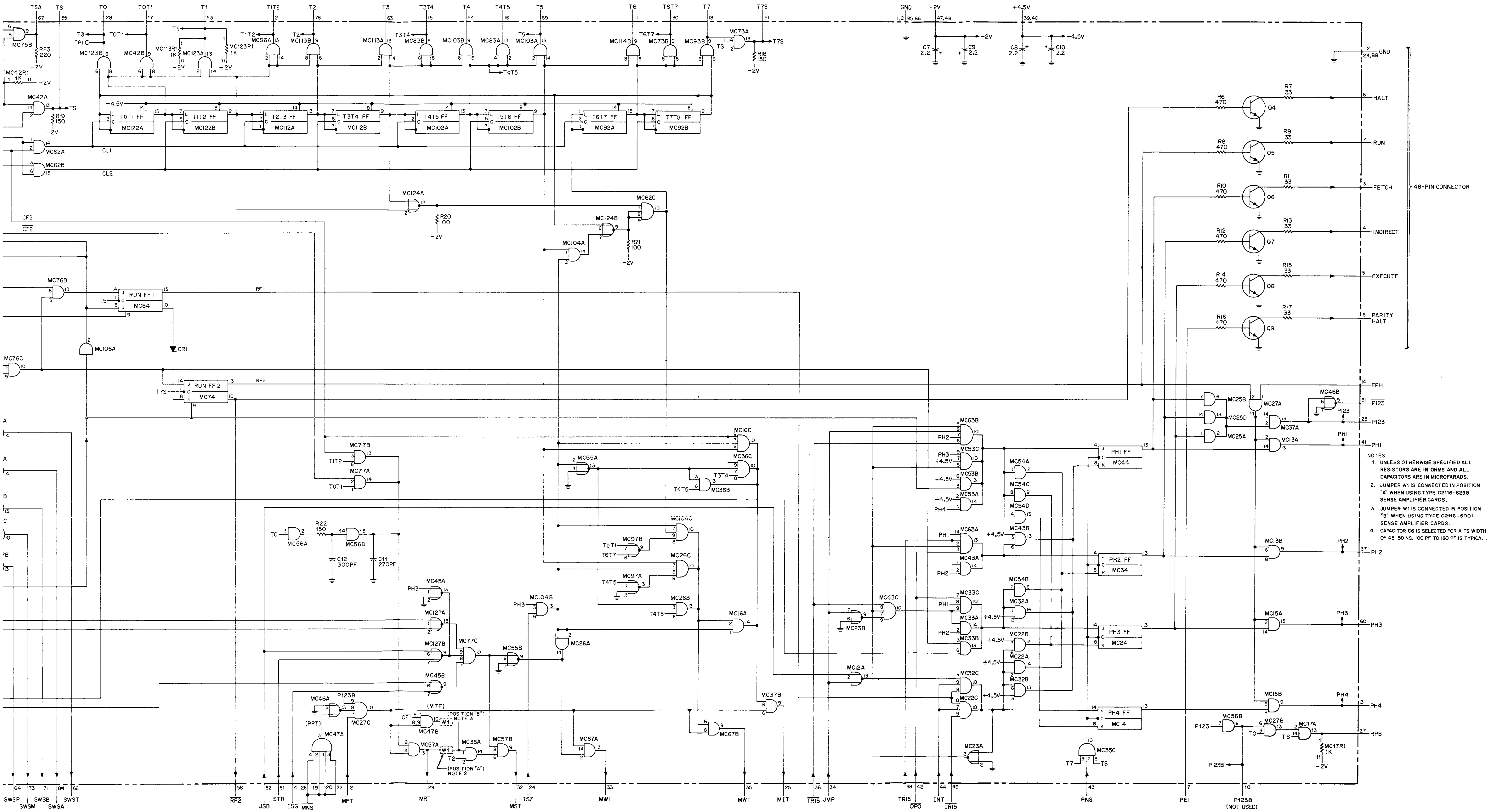


Figure 5-24. A106 Timing Generator Card (02116-6281), Schematic Diagram

.07 Instruction Decoder Card (02116-6027), Reference Designation Index

HP .RT NO.	DESCRIPTION	MFR CODE	MFR PART NO.
80-0155	Capacitor, Fxd, Elect, 2.2 μf, 20%, 20VDCW	56289	150D225X0020A2
20-0956	Integrated Circuit, CTL	07263	SL3459
20-0954	Integrated Circuit, CTL	07263	SL3457
20-0953	Integrated Circuit, CTL	07263	SL3456
20-0967	Integrated Circuit, CTL	07263	SL3464
20-0971	Integrated Circuit, CTL	07263	SL3467
20-0965	Integrated Circuit. CTL	07263	SL3462
20-0952	Integrated Circuit, CTL	07263	SL3455

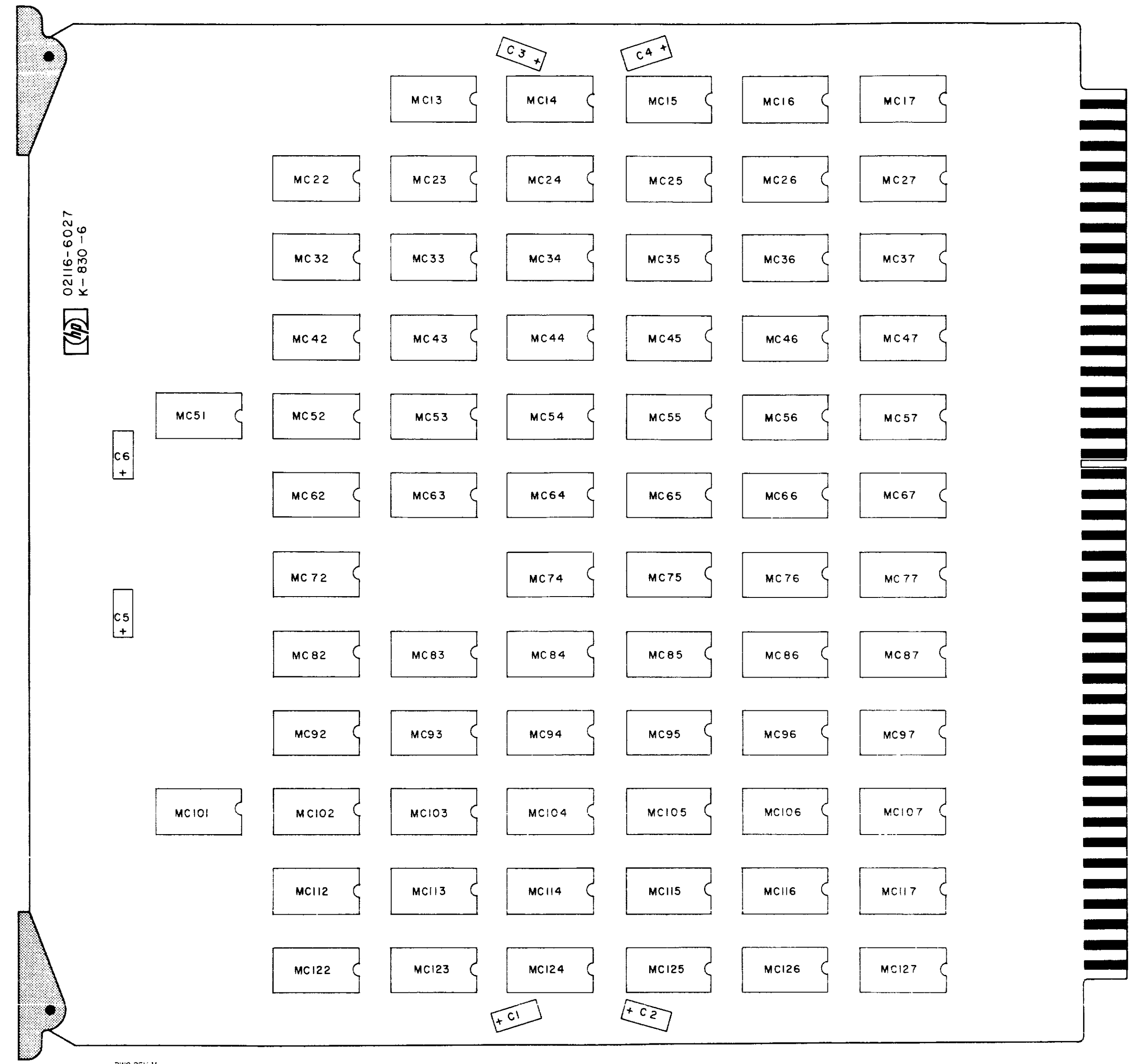
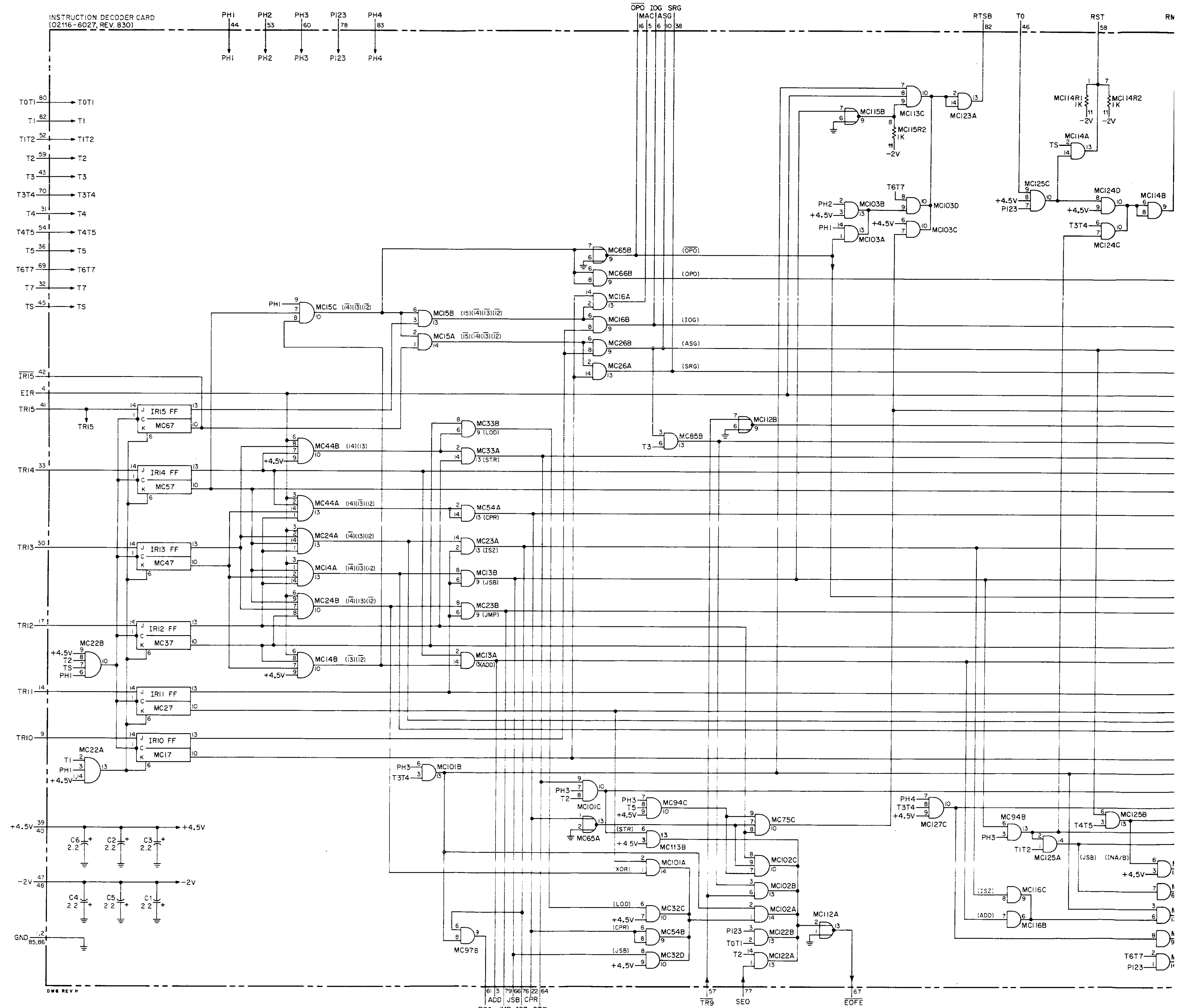


Figure 5-25. A107 Instruction Decoder Card (02116-6027), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	SIGNAL	REF NO.	PIN NO.	SIGNAL	REF NO.
1	GND	219	44	PH1	98
2	GND	219	45	TS	101
3	ADD	53	46	T0	109
4	EIR	112	47	-2V	216
5	MAC	54	48	-2V	216
6	IOG	87	49	AAF	38
7	STP(0-9)	55	50	STBA	77
8	STP(12-15)	68	51	STBB	60
9	TR10	174	52	T1T2	90
10	ASG	69	53	PH2	97
11	RSM(10-15)	56	54	T4T5	107
12	RSM(6-9)	12	55	$\overline{\text{TR6}}$	148
13	BAF	50	56	ANF	78
14	TR11	169	57	$\overline{\text{TR9}}$	168
15	NC	-	58	RST	79
16	$\overline{\text{OPO}}$	71	59	T2	119
17	TR12	192	60	PH3	115
18	RBRB	72	61	RB0	61
19	RARB	57	62	T1	100
20	STM(0-5)	73	63	STBT	62
21	STM(6-9)	58	64	STR	80
22	CPR	74	65	$\overline{\text{CMFE}}$	63
23	$\overline{\text{TR7}}$	144	66	JSB	81
24	SWSB	105	67	$\overline{\text{EOFE}}$	64
25	TR4	157	68	RMSB	82
26	SWSM	106	69	T6T7	110
27	STM(10-11)	59	70	T3T4	89
28	STM(12-15)	96	71	TR2	139
29	TR8	175	72	RPRB	83
30	TR13	178	73	ILS	352
31	T4	113	74	STP(10-11)	52
32	T7	108	75	ADF	65
33	TR14	191	76	ISZ	84
34	SWST	116	77	SEO	118
35	SWSA	120	78	P123	91
36	T5	104	79	JMP	66
37	SWSP	117	80	T0T1	121
38	SRG	75	81	SB0	67
39	+4.5V	217	82	RTSB	85
40	+4.5V	217	83	PH4	88
41	TR15	186	84	$\overline{\text{IOF}}$	86
42	$\overline{\text{IR15}}$	76	85	GND	219
43	T3	103	86	GND	219



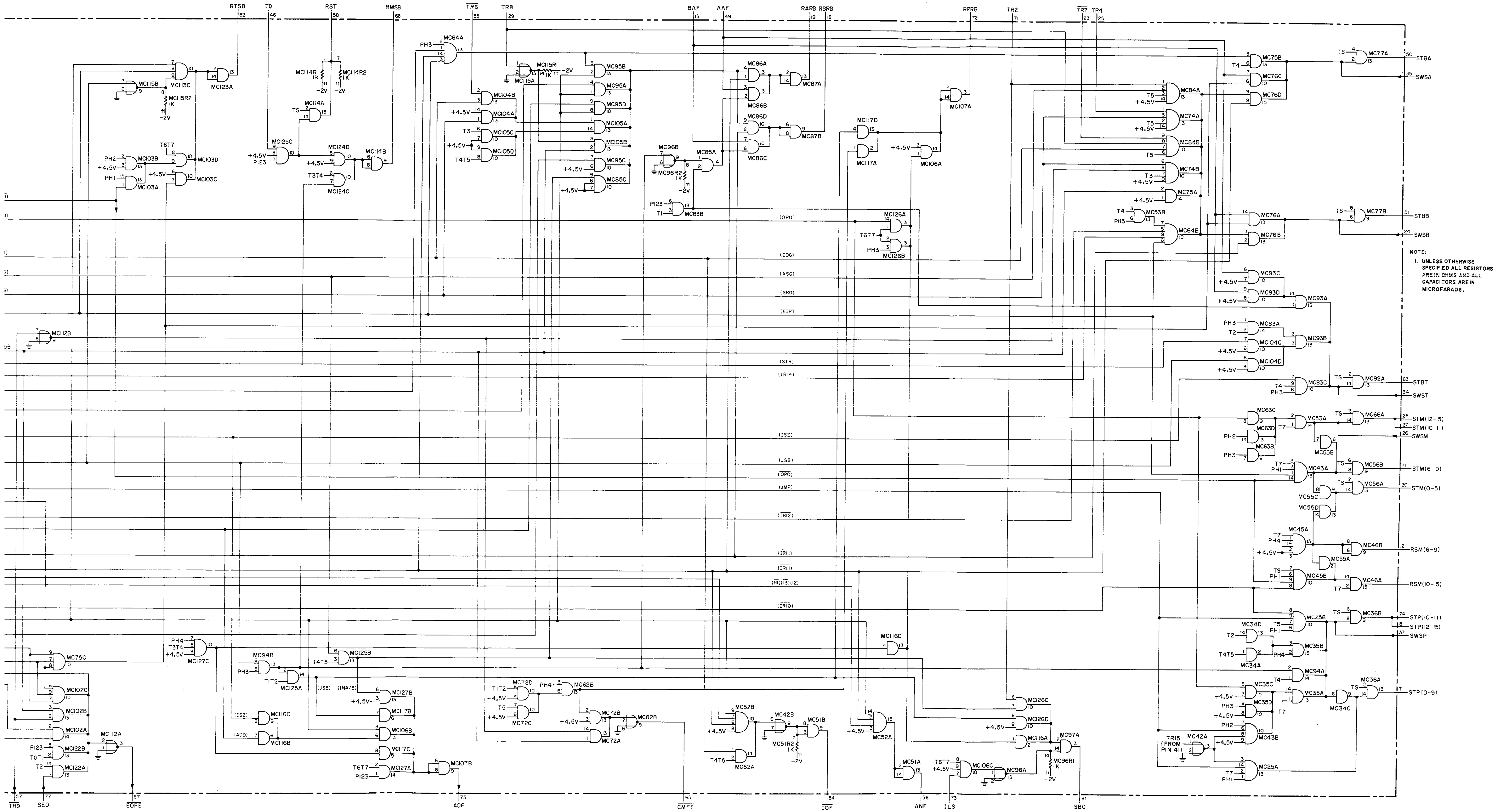


Figure 5-26. A107 Instruction Decoder Card (02116-6027), Schematic Diagram

19. A108 Shift Logic Card (02116-6029), Reference Designation Index

HP ART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
180-0155	Capacitor, Fxd, Elect, 2.2 μf, 20%, 20VDCW	56289	150D225X0020A2
820-0953	Integrated Circuit, CTL	07263	SL3456
820-0952	Integrated Circuit, CTL	07263	SL3455
820-0956	Integrated Circuit, CTL	07263	SL3459
820-0954	Integrated Circuit, CTL	07263	SL3457
820-0967	Integrated Circuit, CTL	07263	SL3464
854-0246	Transistor, Si, NPN	07263	2N3643
683-3305	Resistor, Fxd, Comp, 33 ohms, 5%, 1/4w	01121	CB3305
683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB4715

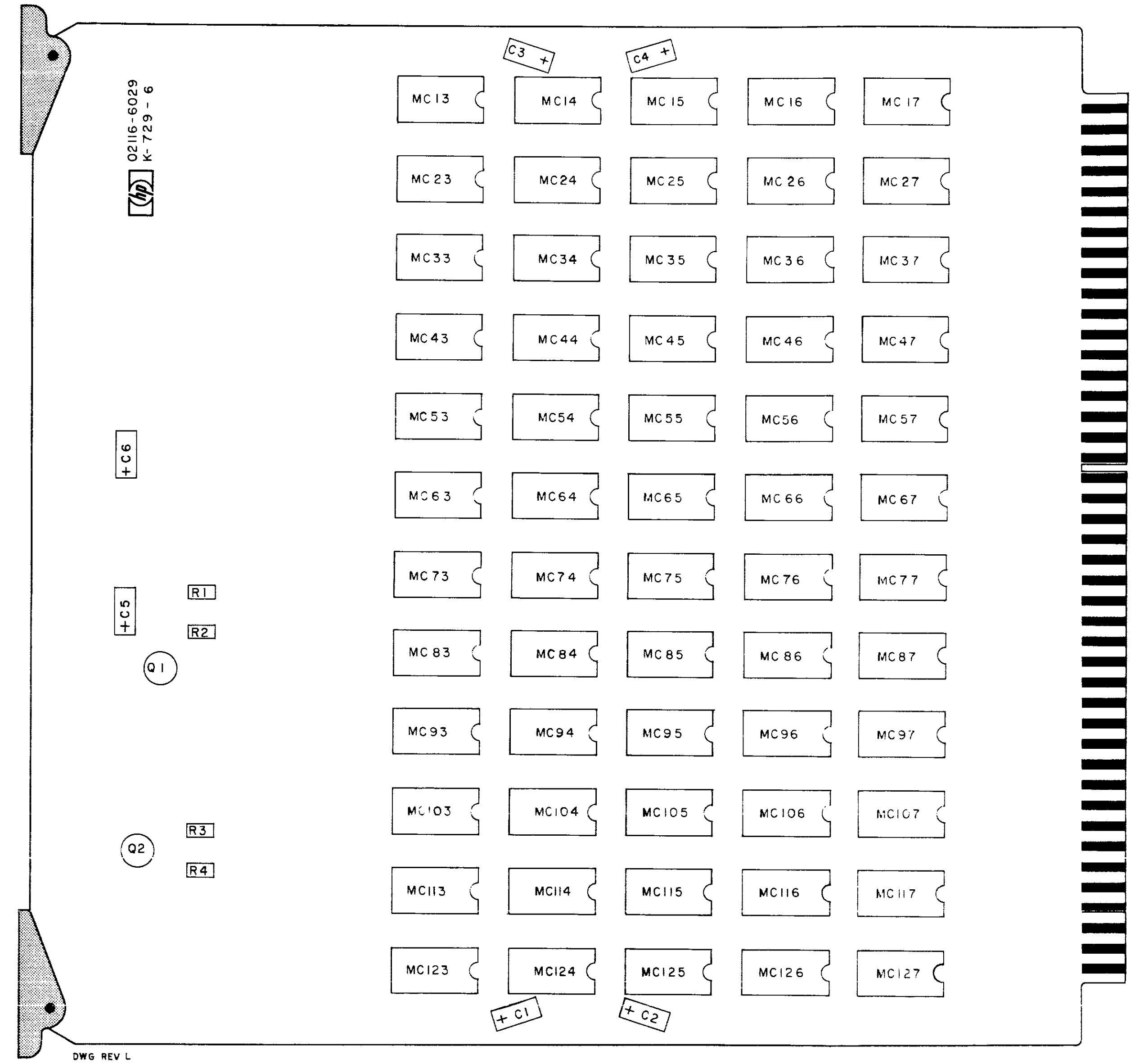
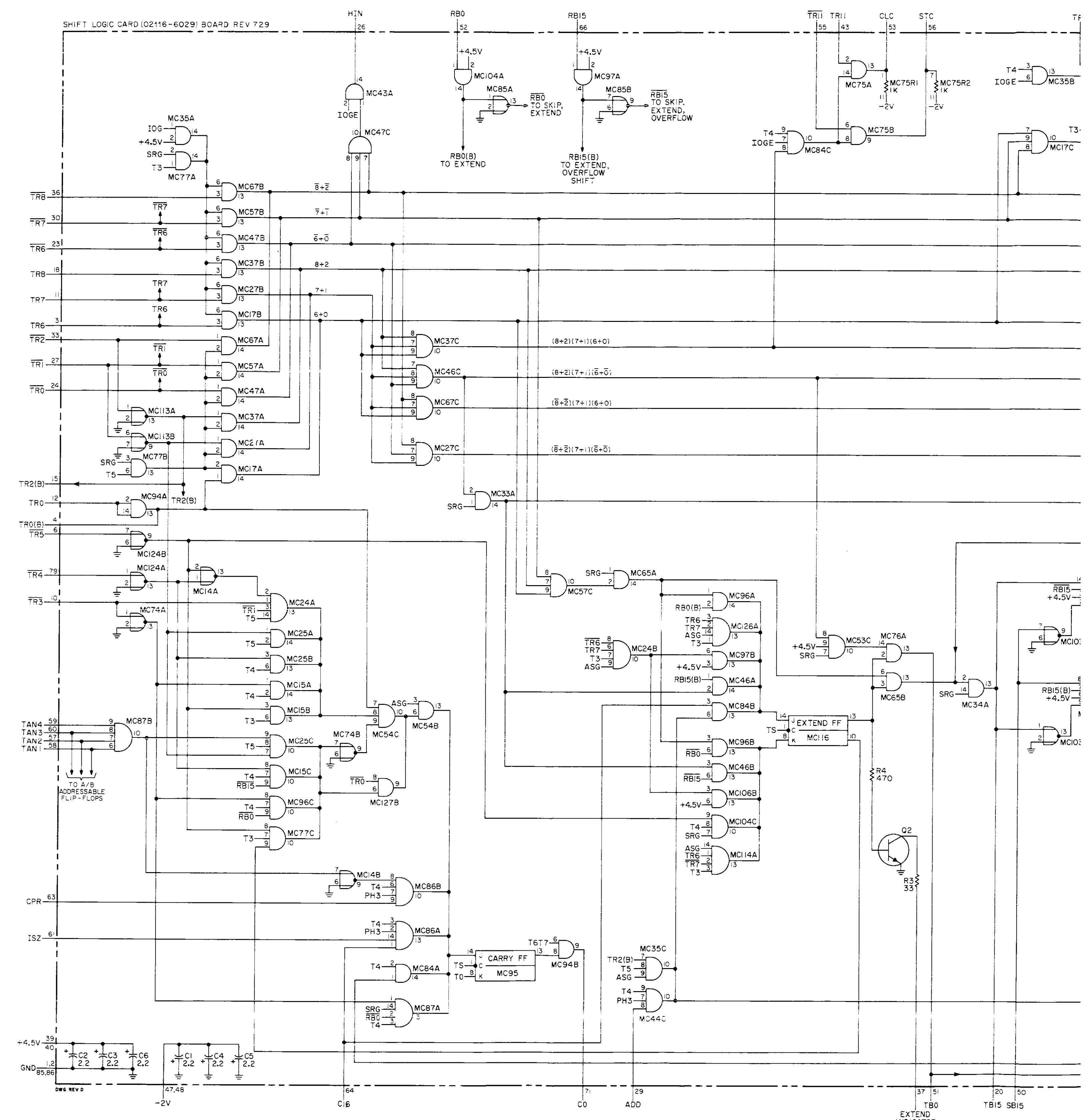


Figure 5-27. A108 Shift Logic Card (02116-6029), Parts Location Diagram

Pin Index (86 Pin Connector)

PIN NO.	SIGNAL	REF NO.	PIN NO.	SIGNAL	REF NO.
1	GND	219	44	IOI	33
2	GND	219	45	T3	103
3	TR6	95	46	T5	104
4	TR0(B)	39	47	-2V	216
5	STF	28	48	-2V	216
6	$\overline{\text{TR5}}$	151	49	SRG	75
7	T3T4	89	50	SB15	195
8	$\overline{\text{SLME}}$	40	51	TB0	198
9	OVF.IND	29	52	RB0	61
10	$\overline{\text{TR3}}$	126	53	CLC	36
11	TR7	152	54	SFS	48
12	TR0	140	55	$\overline{\text{TR11}}$	161
13	IO0	30	56	STC	49
14	SFC	41	57	TAN2	147
15	TR2(B)	31	58	TAN1	129
16	IOGE	349	59	TAN4	181
17	TR9	160	60	TAN3	164
18	TR8	175	61	ISZ	84
19	CLF	32	62	PH3	115
20	TB15	213	63	CPR	74
21	T4T5	107	64	C16	188
22	SEO	118	65	T4	113
23	$\overline{\text{TR6}}$	148	66	RB15	196
24	$\overline{\text{TR0}}$	138	67	TB2	200
25	NC	-	68	T0	109
26	HIN	42	69	P123G	21
27	$\overline{\text{TR1}}$	133	70	TB14	212
28	$\overline{\text{RL4}}$	43	71	C0	37
29	ADD	53	72	T6T7	110
30	$\overline{\text{TR7}}$	144	73	TB13	211
31	SKF	255	74	TS	101
32	$\overline{\text{SRME}}$	44	75	TB1	199
33	$\overline{\text{TR2}}$	130	76	TB12	210
34	IOCO	45	77	AAF	38
35	T2	119	78	TB3	201
36	$\overline{\text{TR8}}$	173	79	$\overline{\text{TR4}}$	156
37	E. IND	34	80	BAF	50
38	$\overline{\text{SL14E}}$	46	81	IOS	258
39	+4.5V	217	82	ASG	69
40	+4.5V	217	83	T7	108
41	$\overline{\text{RRS}}$	35	84	ISR	51
42	$\overline{\text{RLL}}$	47	85	GND	219
43	TR11	169	86	GND	219



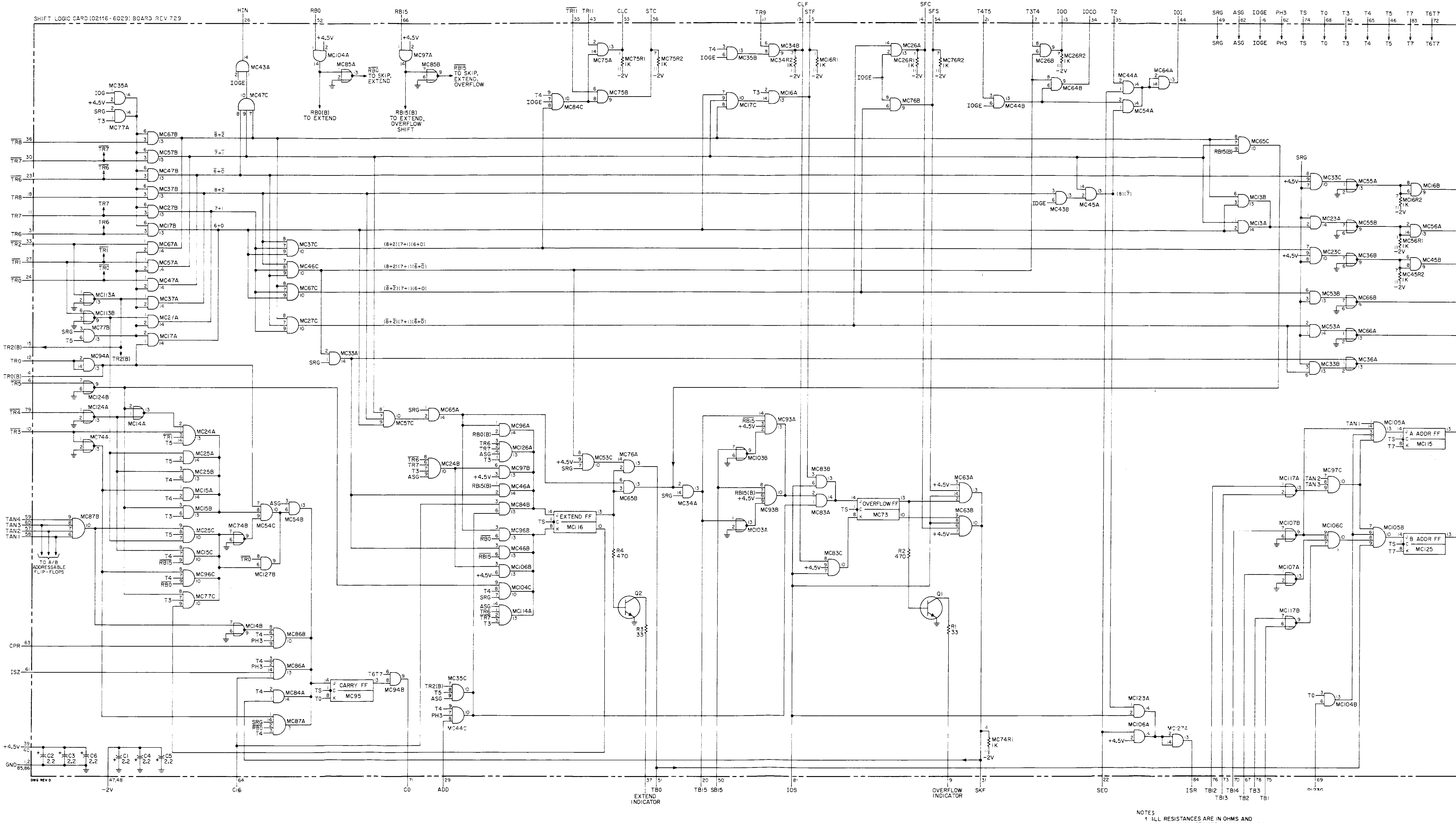


Figure 5-28. A108 Shift Logic Card (02116-6029), Schematic Diagram

Table 5-20. A121 Overvoltage Protection Assembly (02116-6284), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
A121A1	02116-6126	Overvoltage Component Board Assembly (see fig. 5-30)	28480	02116-6126
CR1, 7, 11, 15	1901-0343	Diode, Si, 50 PIV, 18A	04713	1N3491R
CR2	1902-1217	Diode, Breakdown, 6.20V, 5%, 405mA	04713	SZ11746
CR3, 9, 13	1901-0406	Diode, Si, 50 PIV, 18A	04713	IN3491/MR-322
CR8, 10	1902-1205	Diode, Breakdown, 15V, 2%	04713	IN2977RB
CR12, 14	1902-1228	Diode Breakdown, 27V, 10%, 10w	28480	1902-1228
CR16	1902-1218	Diode, Breakdown, 39V, 2% at 65 mA	04713	SZ11747
Q1, 2	1884-0047	Thyristor, SCR, 25V, 55A	01002	C45UX123
Q3 thru Q7	1884-0046	Thyristor, SCR, 50V, 25A	28480	1884-0046

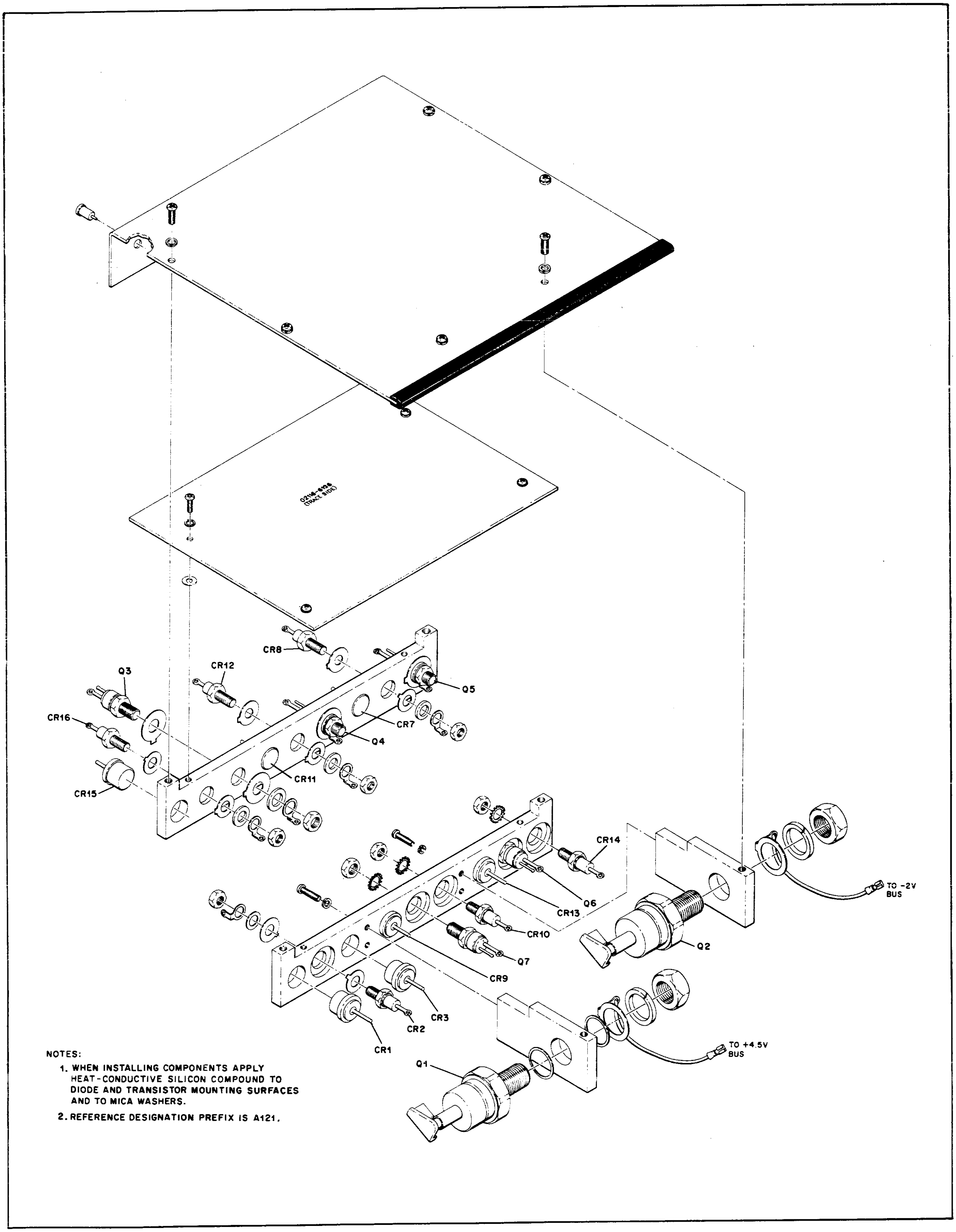


Figure 5-29. A121 Overvoltage Protection Assembly (02116-6284), Parts Location Diagram

Table 5-21. A121A1 Overvoltage Component Board Assembly (02116-6126), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C7	0160-2055	Capacitor, Fxd, Cer, 0.01 μf, +80 -20%, 100VDCW	56289	C023F101F103Z-E12CDH
CR4 thru CR6	1901-0191	Diode, Si, 0.75 A, 100 PIV	04713	SR1358-2
R1, 4	0689-1505	Resistor, Fxd, Comp, 15 ohms, 5%, 1w	01121	GB1505
R2, 3	0689-3315	Resistor, Fxd, Comp, 220 ohms, 5%, 1w	01121	EB2215
R5, 12, 13, 20, 21	0686-2205	Resistor, Fxd, Comp, 22 ohms, 5%, 1w	01121	EB2205
R6, 11, 14, 19, 22	0686-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1w	01121	EB4715
R7 thru R10, R15 thru R18, 23, 24	0813-0038	Resistor, Fxd, WW, 0.5 ohms, 10 op, 5w	28480	0813-0038
R25, 26	0811-1857	Resistor, Fxd, WW, 400 ohms, 5%, 5w	28480	0811-1857

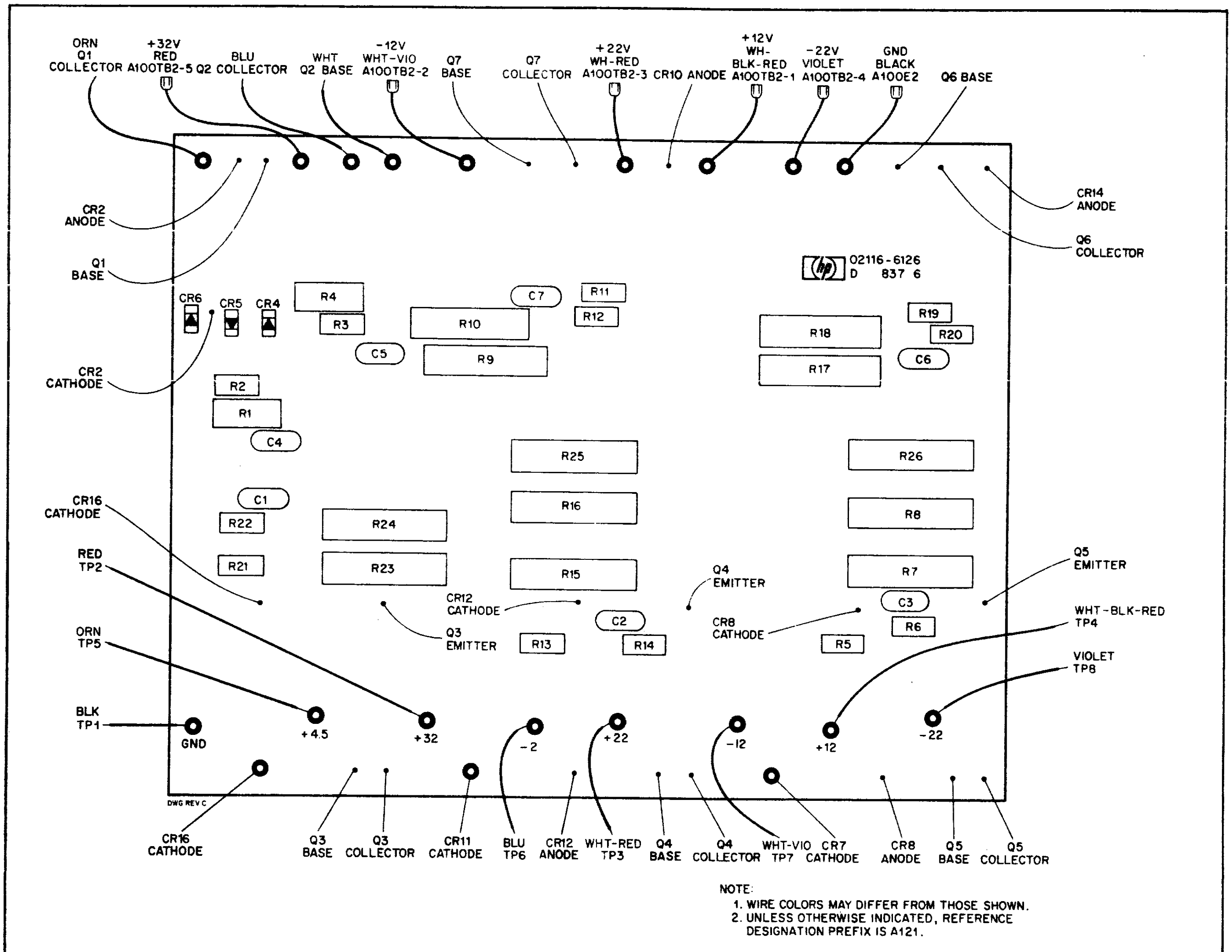
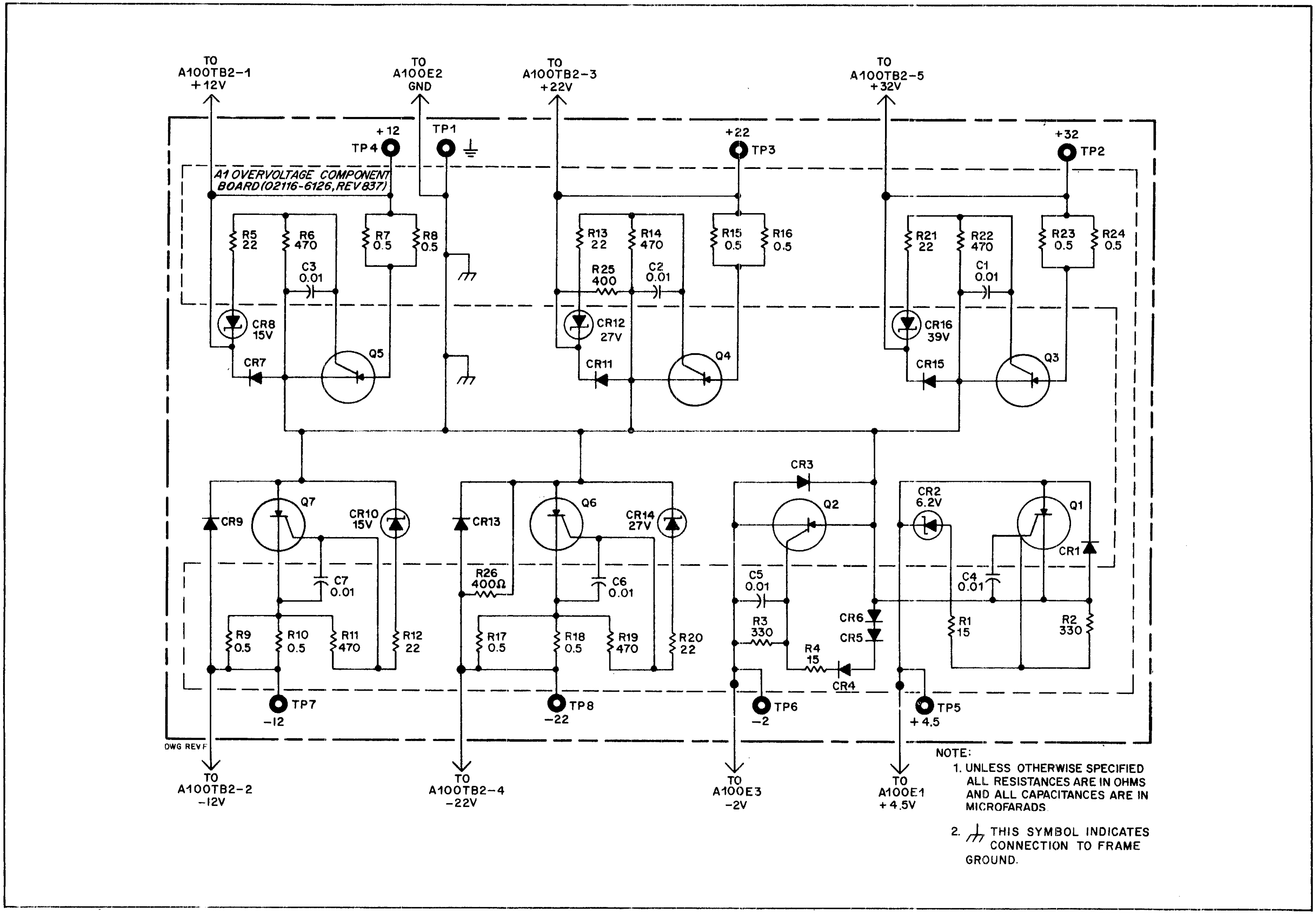


Figure 5-30. A121A1 Overvoltage Component Board (02116-6126), Parts Location Diagram



02116-6284-L

Figure 5-31. A121 Overvoltage Protection Assembly (02116-6284), Schematic Diagram

Table 5-22. A300 Power Supply Assembly (02116-6124), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
A301	02116-6014	Logic Supply Regulator Card (see fig. 5-32)	28480	02116-6014
A302	02116-6015	Memory Supply Regulator Card (see fig. 5-33)	28480	02116-6015
A303	NSR	Capacitor Board Assembly (see fig. 5-34)		
A304	NSR	Large Heat Sink Assembly (see fig. 5-35)		
A305	NSR	Small Heat Sink Assembly (see fig. 5-36)		
A306	NSR	Component Board Assembly (see fig. 5-37)		
A307	NSR	Component Board Assembly (see fig. 5-38)		
A308	NSR	Component Board Assembly (see fig. 5-39)		
A309	NSR	Component Board Assembly (see fig. 5-40)		
A310	NSR	Component Board Assembly (see fig. 5-41)		
A311	NSR	Transformer Assembly (see fig. 5-42)		
A312	NSR	AC Input Section (see fig. 5-43)		
B1	3160-0072	Fan, Tubeaxial, 115V, 60 Hz (see fig. 1-4)	28480	3160-0072
C1A, 1B	0160-3043	Capacitor, Fxd, Cer, 2 x 0.005 μf, 20%, 250 VACW, (see fig. 5-43)	56289	29C147-CDH
J1	1251-0315	Connector, Male, 250V, 10 A (see fig. 5-43)	83315	7556-G
J2	1251-0143	Connector, Female, 14 contact (see fig. 5-41)	28480	1251-0143
R1	0811-2140	Resistor, Fxd, WW, 2 ohms, 5%, 5w (see fig. 5-43)	28480	0811-2140

Table 5-23. A301 Logic Supply Regulator Card (02116-6014), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C40, 41, 42, 43, 45, 47, 48, 49, 51, 59	0150-0121	Capacitor, Fxd, Cer, 0.1 µf, +80 -20%, 50VDCW	56289	5C50BIS-CML
C44, 58	0150-0050	Capacitor, Fxd, Cer, 1000 pf, +80 -20%, 1000VDCW	56289	C067B102E102-ZE19CDH
C46, 50, 52	0160-0163	Capacitor, Fxd, My, 0.033 µf, 10%, 200VDCW	56289	192P33392-PTS
C53, 55, 57	0180-0064	Capacitor, Fxd, Elect, 35 µf, -10 +100%, 6VDCW	56289	30D156G006BB4
C54	0180-1867	Capacitor, Fxd, Elect, 1600 µf +75 -10%, 10VDCW	28480	0180-1867
C56	0180-1714	Capacitor, Fxd, Elect, 330 µf, 10%, 6VDCW	28480	0180-1714
CR50	1902-0071	Diode, Breakdown, 9.0V, 5%	28480	1902-0071
CR51, 53, 54, 55, 56, 57, 59, 61, 62, 63	1901-0025	Diode, Silicon, 100 mA, 1V	07263	FD2387
CR52	1902-0556	Diode, Breakdown, 20.0V, 5%, 1w	28480	1902-0556
CR58	1902-3079	Diode, Breakdown, 4.53V, 5%	04713	SZ10939-83
CR60	1902-0184	Diode, Breakdown, Si, 16.2V, 5%	28480	1902-0184
CR64	1902-3224	Diode, Breakdown, 17.8V, 5%, 400 mW	28480	1902-3224
CR65	1902-0017	Diode, Breakdown, 6.81, 10%	04713	SZ10939-133
MC1	1820-0954	Integrated Circuit, CTL	07263	SL3457
Q30, 31, 32, 35, 36, 37	1853-0001	Transistor, Si, PNP	28480	1853-0001
Q33, 34, 38, 43	1850-0062	Transistor, Ge, Alloy Junction	01295	GA287
Q39, 40	1854-0003	Transistor, Si, NPN	28480	1854-0003
Q41	1854-0265	Transistor, Si, NPN	28480	1854-0265
Q42, 44	1851-0017	Transistor, Ge, NPN	01295	2N1304
R61	0757-0808	Resistor, Fxd, Flm, 301 ohms, 1%, 1/4w	28480	0757-0808
R62	0761-0008	Resistor, Fxd, Met Ox, 510 ohms, 5%, 1w	28480	0761-0008
R63, 74	0751-0821	Resistor, Fxd, Flm, 1.21 k, 1%, 1/2w	28480	0757-0821
R64, 78, 98	0757-0730	Resistor, Fxd, Flm, 750 ohms, 1%, 1/4w	28480	0757-0730
R65, 67	0757-0071	Resistor, Fxd, Flm, 247.5 ohms, 1%, 1/4w	28480	0757-0071
R66, 76, 96	2100-1770	Resistor, Var, WW, 100 ohms, 5%	28480	2100-1770
R68, 81, 100	0757-0924	Resistor, Fxd, Flm, 1 k, 2%, 1/8w	28480	0757-0924
R69, 84	2100-1772	Resistor, Var, WW, 500 ohms, 5%	28480	2100-1772
R70	0757-0728	Resistor, Fxd, Flm, 619 ohms, 1%, 1/4w	28480	0757-0728
R71, 86	0757-0715	Resistor, Fxd, Flm, 150 ohms, 1%, 1/4w	28480	0757-0715
R72, 87, 119	0757-0244	Resistor, Fxd, Flm, 499 ohms, 1%, 1/4w	28480	0757-0244
R75, 102	0757-0711	Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/4w	28480	0757-0711
R77	0757-0727	Resistor, Fxd, Flm, 562 ohms, 1%, 1/4w	28480	0757-0727
R82, 80, 99	0757-0743	Resistor, Fxd, Flm, 3.32 k, 1%, 1/4w	28480	0757-0743
R83	0686-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/2w	01121	EB2215
R85	0757-0732	Resistor, Fxd, Flm, 909 ohms, 1%, 1/4w	28480	0757-0732
R88	0761-0026	Resistor, Fxd, Met Ox, 220 ohms, 5%, 1w	28480	0761-0026
R89	0757-0739	Resistor, Fxd, Flm, 2.00 k, 1%, 1/4w	28480	0757-0739
R95	0757-0814	Resistor, Fxd, Flm, 511 ohms, 1%, 1/2w	28480	0757-0814
R97	0757-0158	Resistor, Fxd, Flm, 619 ohms, 1%, 1/2w	28480	0757-0158
R101	0761-0011	Resistor, Fxd, Met Ox, 3300 ohms, 5%, 1w	28480	0761-0011

Table 5-23. A301 Logic Supply Regulator Card (02116-6014), Reference Designation Index (Cont)

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R103	0698-3134	Resistor, Fxd, Flm, 1.33 k, 1%, 1/4w	28480	0698-3134
R110	0757-0912	Resistor, Fxd, Flm, 330, 2%, 1/8w	28480	0757-0912
R111, 113	0757-0338	Resistor, Fxd, Flm, 1.00 k, 1%, 1/4w	28480	0757-0338
R112	0757-0759	Resistor, Fxd, Flm, 18.2 k, 1%, 1/4w	28480	0757-0759
R114	0757-0705	Resistor, Fxd, Flm, 47.5 ohms, 1%, 1/4w	28480	0757-0705
R115	0757-0340	Resistor, Fxd, Flm, 10.0 k, 1%, 1/4w	28480	0757-0340
R116	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4w	01121	CB1025
R117	0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4w	01121	CB5115
R118	0757-0197	Resistor, Fxd, Flm, 1500 ohms, 1%, 1/2w	28480	0757-0197

Table 5-23. A301 Logic Supply Regulator Card (02116-6014), Reference Designation Index (Cont)

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R103	0698-3134	Resistor, Fxd, Flm, 1.33 k, 1%, 1/4w	28480	0698-3134
R110	0757-0912	Resistor, Fxd, Flm, 330, 2%, 1/8w	28480	0757-0912
R111, 113	0757-0338	Resistor, Fxd, Flm, 1.00 k, 1%, 1/4w	28480	0757-0338
R112	0757-0759	Resistor, Fxd, Flm, 18.2 k, 1%, 1/4w	28480	0757-0759
R114	0757-0705	Resistor, Fxd, Flm, 47.5 ohms, 1%, 1/4w	28480	0757-0705
R115	0757-0340	Resistor, Fxd, Flm, 10.0 k, 1%, 1/4w	28480	0757-0340
R116	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4w	01121	CB1025
R117	0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4w	01121	CB5115
R118	0757-0197	Resistor, Fxd, Flm, 1500 ohms, 1%, 1/2w	28480	0757-0197

PIN INDEX

PIN	TO/FROM	PIN	TO/FROM
A	—	1	—
B	XA301-2	2	A303C9(+)
C	—	3	XA302-19
D	A307R51	4	—
E	XA301-5	5	-2V BUS
F	A303C13(+)	6	—
H	A307R47	7	A303C11(-)
J	A307R45	8	GND BUS
K	A303C10(-)	9	A306R16
L	XA301-10	10	GND BUS
M	—	11	A100TB1-1
N	XA301-12	12	A303C15(+)
P	A303C15(+)	13	A310R11
R	-2V BUS	14	A310R11
S	A303C23(-)	15	A310R15
T	—	16	—
U	—	17	—
V	—	18	—
W	—	19	—
X	XA301-20	20	A308R19
Y	GND BUS	21	A307R46
Z	A303C19(-)	22	A307R45

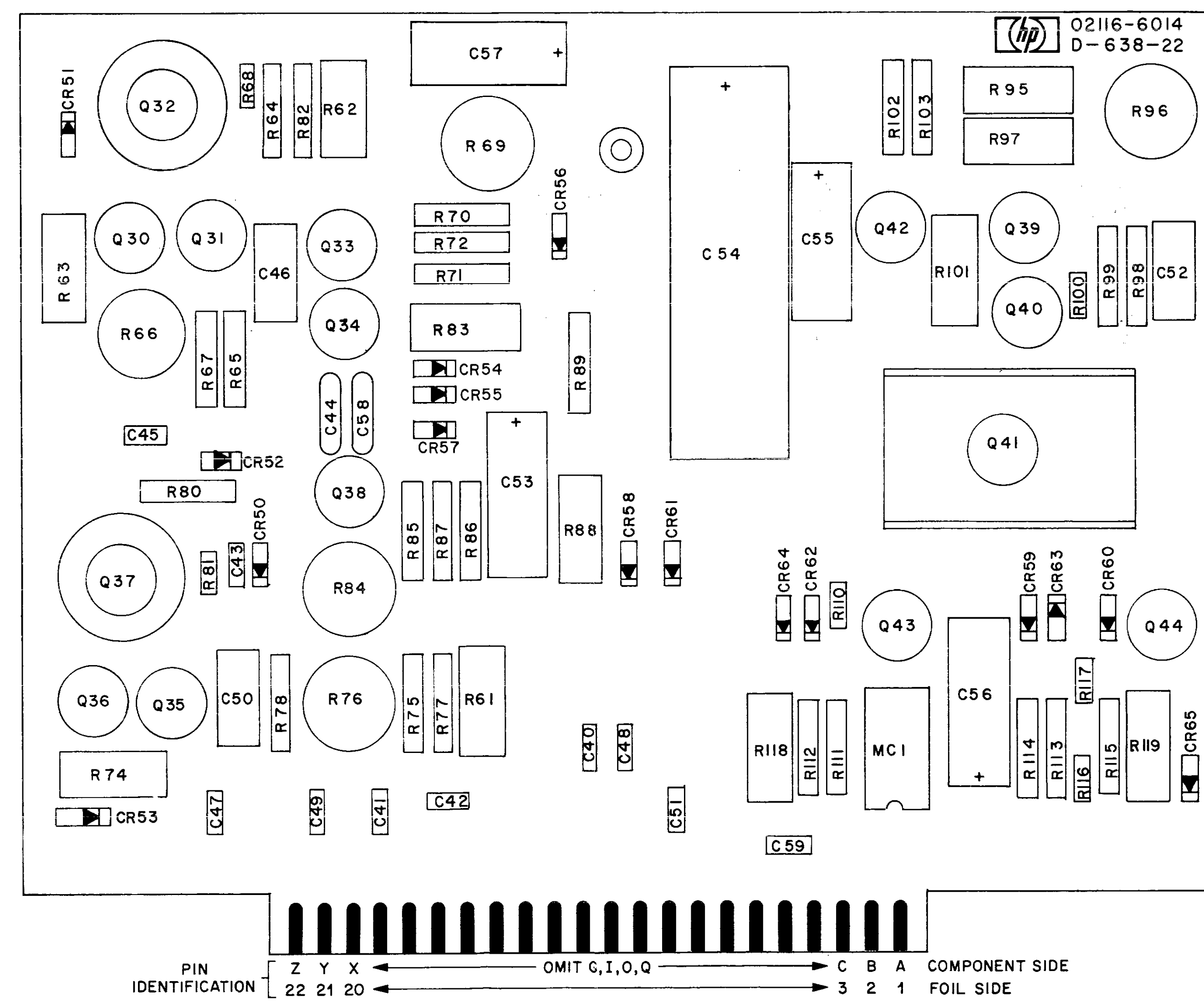


Figure 5-32. A301 Logic Supply Regulator Card (02116-6014), Parts Location and Connection Diagram

Table 5-24. A302 Memory Supply Regulator Card (02116-6015), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C70 thru C81	0150-0121	Capacitor, Fxd, Cer, 0.1 μf, +80 -20%, 50VDCW	56289	5C50B1S-CML
CR70	1902-0071	Diode, Breakdown, 9.0V, 5%	28480	1902-0071
CR71, 72, 74	1902-0379	Diode, Breakdown, 20V, 10%, 1.5w	28480	1902-0379
CR73	1902-3182	Diode, Breakdown, Si, 12.1V, 5%	28480	1902-3182
Q50, 51, 57, 58	1853-0036	Transistor, Si, PNP	28480	1853-0036
Q52, 59	1853-0041	Transistor, Si, PNP	02735	38640
Q53, 60	1850-0062	Transistor, Ge, Alloy Junction	01295	GA287
Q54, 61	1854-0221	Transistor, Si, NPN	28480	1854-0221
Q55, 62	1854-0022	Transistor, Si, NPN	07263	S17843
Q56, 64	1851-0071	Transistor, Ge, NPN	01295	2N1304
Q63	1854-0072	Transistor, Si, NPN	02735	2N3054
R125	2100-0755	Resistor, Var, WW, 1 k, 5%	28480	2100-0755
R126	0811-2033	Resistor, Fxd, WW, 1100 ohms, 1%, 1/4w	28480	0811-2033
R127	0811-2032	Resistor, Fxd, WW, 880 ohms, 1%, 1/4w	28480	0811-2032
R128	0811-2036	Resistor, Fxd, WW, 1800 ohms, 1%, 1/4w	28480	0811-2036
R129, 174	0757-0834	Resistor, Fxd, Flm, 5.62 k, 2%, 1/2w	28480	0757-0834
R130	0757-1094	Resistor, Fxd, Flm, 1.47 k, 1%, 1/8w	28480	0757-1094
R131	0757-0914	Resistor, Fxd, Flm, 390 ohms, 2%, 1/8w	28480	0757-0914
R132, 146, 161, 176	0757-0924	Resistor, Fxd, Flm, 1 k, 2%, 1/8w	28480	0757-0924
R133, 147, 162, 178, 179	0757-0900	Resistor, Fxd, Flm, 100 ohms, 2%, 1/8w	28480	0757-0900
R134	0757-0910	Resistor, Fxd, Flm, 270 ohms, 2%, 1/8w	28480	0757-0910
R135	0698-3154	Resistor, Fxd, Flm, 4.22 k, 1%, 1/8w	28480	0698-3154
R136, 150	0770-0003	Resistor, Fxd, Flm, 3300 ohms, 5%, 4w	28480	0770-0003
R140, 155	2100-1429	Resistor, Var, WW, 2000 ohms, 5%, 1w	28480	2100-1429
R143, 173	0811-2035	Resistor, Fxd, WW, 1590 ohms, 1%, 1/4w	28480	0811-2035
R144	0757-0196	Resistor, Fxd, Flm, 6.19 k, 1%, 1/2w	28480	0757-0196
R145, 175	0757-0931	Resistor, Fxd, Flm, 2 k, 2%, 1/8w	28480	0757-0931
R148	0757-0918	Resistor, Fxd, Flm, 560 ohms, 2%, 1/8w	28480	0757-0918
R149, 163, 181	0757-0442	Resistor, Fxd, Flm, 10.0 k, 1%, 1/8w	28480	0757-0442
R156, 172	0811-2039	Resistor, Fxd, WW, 8000 ohms, 1%, 1/4w	28480	0811-2039
R157	0811-2098	Resistor, Fxd, WW, 2.75 k, 1%, 1/4w	28480	0811-2098
R158	0811-2037	Resistor, Fxd, WW, 2400 ohms, 1%, 1/4w	28480	0811-2037
R159	0698-3411	Resistor, Fxd, Flm, 3.48 k, 1%, 1/2w	28480	0698-3411
R160	0757-0744	Resistor, Fxd, Flm, 3920 ohms, 1%, 1/4w	28480	0757-0744
R164	0757-0920	Resistor, Fxd, Flm, 680 ohms, 2%, 1/8w	28480	0757-0920
R165	0764-0063	Resistor, Fxd, Flm, 620 ohms, 5%, 2w	28480	0764-0063
R170	2100-0741	Resistor, Var, WW, 5 k, 5%, 1w	28480	2100-0741
R171	0811-2040	Resistor, Fxd, WW, 21.8 k, 1%, 1/4w	28480	0811-2040
R177	0764-0062	Resistor, Fxd, Met Ox, 3.6 k, 5%, 2w	28480	0764-0062
R180	0757-0916	Resistor, Fxd, Flm, 470 ohms, 2%, 1/8w	28480	0757-0916
R182	0770-0002	Resistor, Fxd, Met Ox, 2400 ohms, 5%, 4w	28480	0770-0002

PIN INDEX

PIN	TO/FROM	PIN	TO/FROM
A	A308R19	1	A100TB2-6
B	A303C11(-)	2	A303C12(+)
C	—	3	—
D	XA302-B	4	XA302-2
E	A306R54	5	A307R51
F	A303C23(-)	6	XA302-F
H	XA302-7	7	A308R19
J	A306R52	8	—
K	—	9	—
L	—	10	A307R50
M	XA302-11	11	A303E12
N	XA302-12	12	GND BUS
P	—	13	A100TB2-7
R	A303C10(-)	14	—
S	—	15	A303C13(+)
T	A306R56	16	—
U	—	17	XA302-15
V	—	18	—
W	A307R48	19	XA301-3
X	XA302-20	20	A303C26(+)
Y	—	21	A307R57
Z	XA302-22	22	A307R51
AA	XA302-R	23	A306R49
BB	XA302-24	24	A303E8

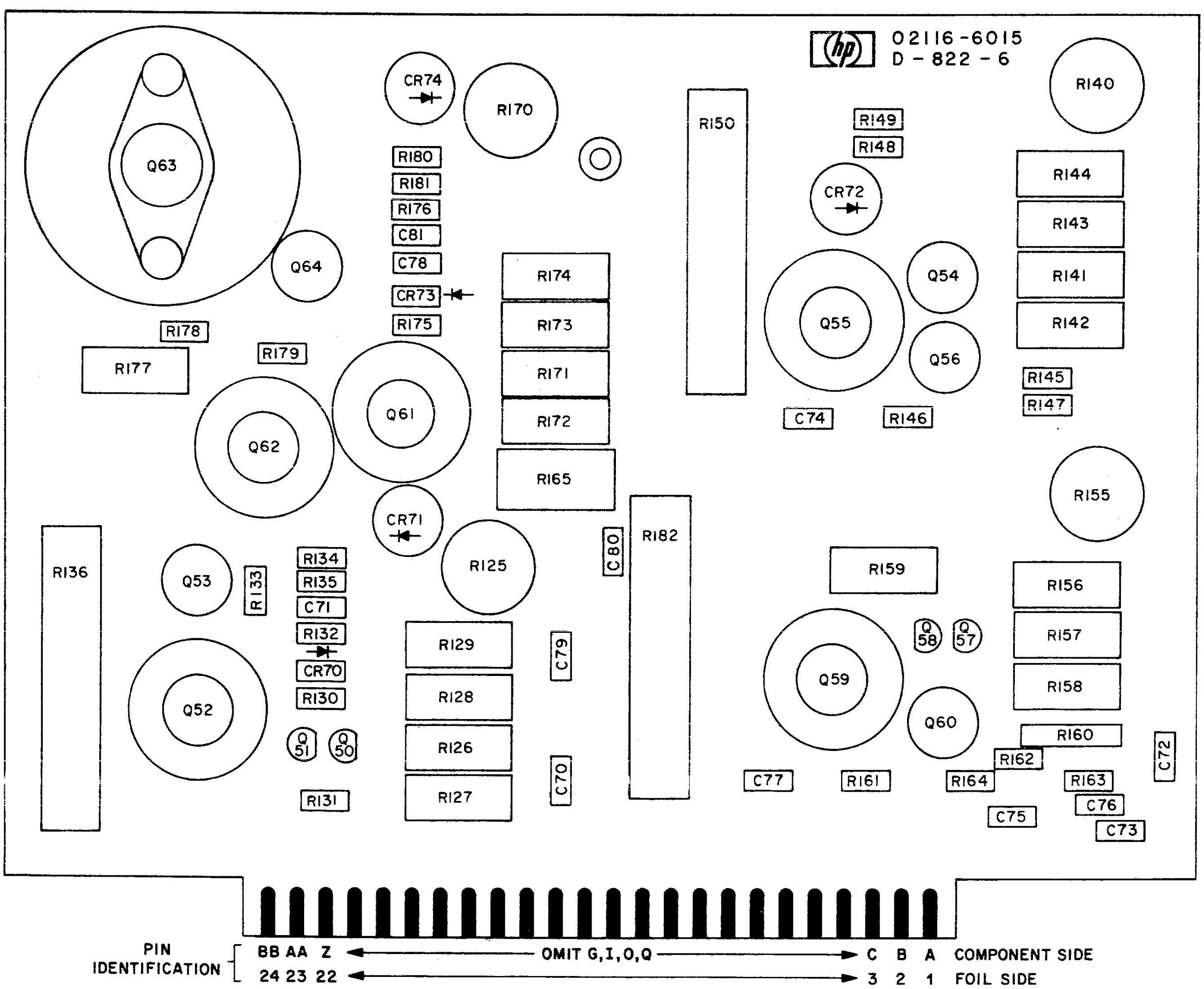


Figure 5-33. A302 Memory Supply Regualtor Card (02116-6015), Parts Location and Connection Diagram

Table 5-25. A303 Capacitor Board Assembly (02116-6038), Reference Designation Index

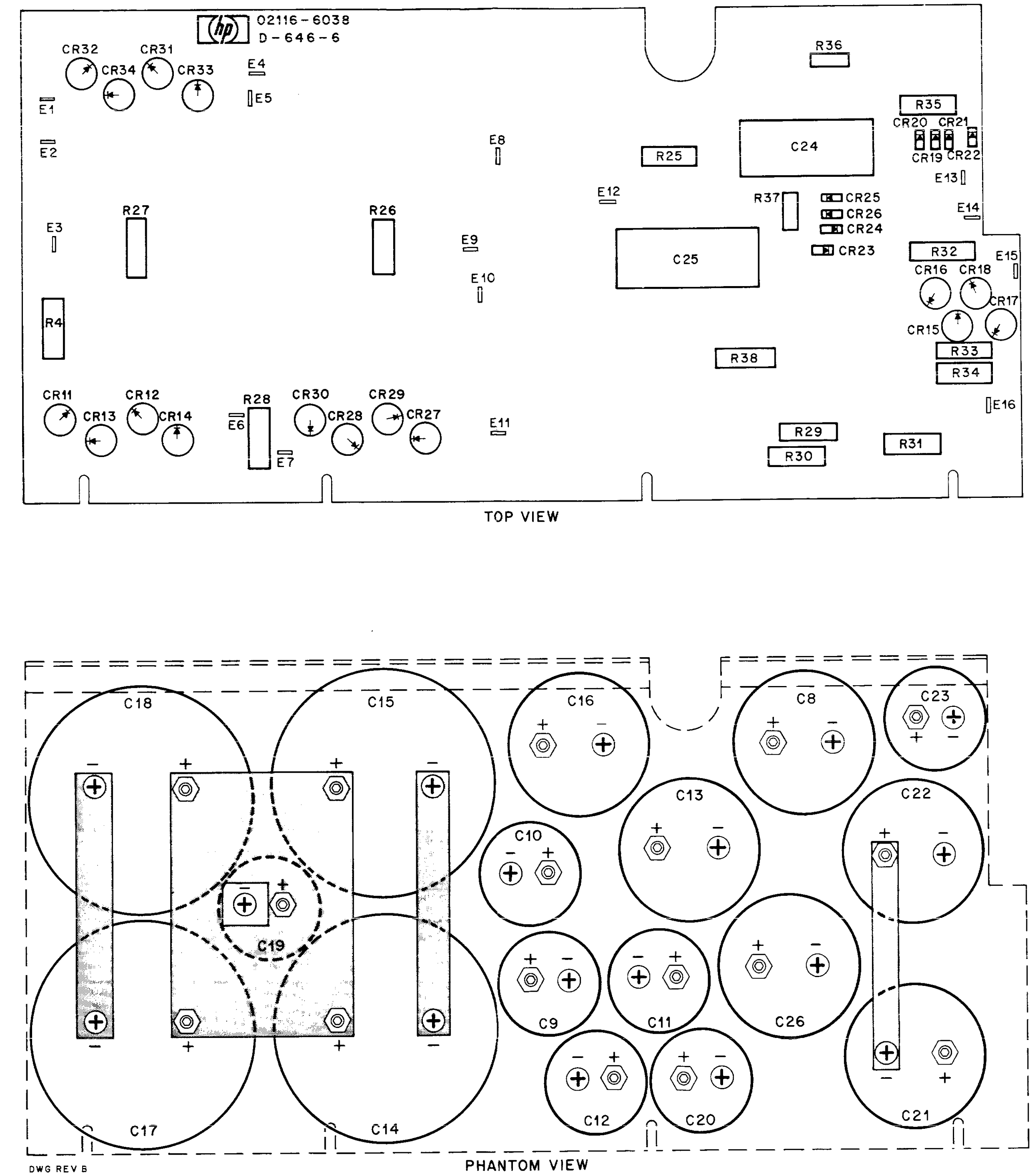
REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C8, 16	0180-1874	Capacitor, Fxd, Elect, 51,000 μf, +75 -10%, 7.5VDCW	28480	0180-1874
C9, 10	0180-1870	Capacitor, Fxd, Elect, 10,000 μf, +75 -10%, 20VDCW	28480	0180-1870
C11, 12	0180-1868	Capacitor, Fxd, Elect, 4900 μf, +75 -10%, 40VDCW	28480	0180-1868
C13	0180-1869	Capacitor, Fxd, Elect, 8700 μf, +75 -10%, 50VDCW	28480	0180-1869
C14, 15, 17, 18	0180-1875	Capacitor, Fxd, Elect, 100,000 μf, +75 -10%, 20VDCW	28480	0180-1875
C19	0180-1871	Capacitor, Fxd, Elect, 12,000 μf, +75 -10%, 25VDCW	28480	0180-1871
C20, 23	0180-1977	Capacitor, Fxd, Elect, 5900 μf, +75 -10%, 50VDCW	28480	0180-1977
C21, 22	0180-1873	Capacitor, Fxd, Elect, 21,000 μf, +75 -10%, 30VDCW	28480	0180-1873
C24, 25	0180-1866	Capacitor, Fxd, Elect, 500 μf, +75 -10%, 75VDCW	56289	39D507G075HL4-DSB
C26	0180-1978	Capacitor, Fxd, Elect, 8800 μf, +50 -10%, 75VDCW	28480	0180-1978
CR11 thru CR18, CR27 thru CR34	1901-0416	Diode, Si, 200 PIV, 3A	28480	1901-0416
CR19 thru CR26	1901-0191	Diode, Si, 0.75A, 100 PIV	04713	SR1358-2
R4, 29, 33, 34	0813-0038	Resistor, Fxd, WW, 1 ohms, 3%, 3w	28480	0813-0029
R25	0764-0017	Resistor, Fxd, Met Ox, 1.6 k, 5%, 2w	28480	0764-0017
R26, 27	0811-2138	Resistor, Fxd, WW, 120 ohms, 5%, 3w	28480	0811-2139
R28	0811-1858	Resistor, Fxd, WW, 500 ohms, 5%, 5w	28480	0811-1858
R30, 35	0812-0099	Resistor, Fxd, WW, 1 k, 5%, 5w	28480	0812-0099
R31, 32	0811-1857	Resistor, Fxd, WW, 400 ohms, 5%, 5w	28480	0811-1857
R36, 37	0686-1235	Resistor, Fxd, Comp, 12 k, 5%, 1/2w	01121	EB1235
R38	0812-0050	Resistor, Fxd, WW, 3 k, 5%, 5w	28480	0812-0050

NOTE: Capacitors C8 thru C23, and C26 are not part of Capacitor Board Assembly A303, and must be ordered separately. They are listed here for convenience only.

A303 CONNECTIONS

A303 CONNECTION	VOLTAGE	DESTINATION*
C8(-)	-2V	-2V bus
C9(+)	+12V	A100TB2-1, A306R16, XA301-2.
C10(-)	-12V	A100TB2-2, A307R48, A402-3, XA301-K, XA302-R.
C11(-)	-22V	A100TB2-4, A306R52, XA301-7, XA302-B.
C12(+)	+22V	A100TB2-3, A307R50, XA302-2.
C13(+)	+32V	A100TB2-5, A306R56, XA301-F, XA302-15.
C13(-)	GND	A308CR9, GND bus, A300J2-6
C14(+)	+4.5V	+4.5V bus
C14(-)	—	A304 (Q1, Q2, Q3, Q4).
C15(+)	+4.5V	A310R23, XA301-P, XA301-12.
C15(-)	—	A309CR1
C17(+)	—	A311TB7-22
C17(-)	-5.6V	A100TB1-5, A304 (Q5, Q6, Q7, Q8), A312K1 coil.
C18(-)	—	A309CR3
C19(-)	-12.4V	XA301-Z, XA304-1.
C20(+)	+35.5V	A100TB2-8, A306R39, A308R19.
C21(+)	+23.3V	A307R45, A307R46, A308R5, A308R17.
C22(+)	—	A311TB4-2
C22(-)	-22.6V	A307R57, A308R6, XA305-4.
C23(-)	-36.4V	XA301-S, XA302-F, XA305-2.
C26(+)	+56.4V	XA302-20, XA305-3.
E1	—	A311TB6-5
E2	—	A311TB2-3
E3	—	A311TB2-4
E4	+7V	A100TB1-7
E5	GND	A100TB1-6
E6	—	A311TB4-1
E7	—	A311TB2-2
E8	-84.5V	XA302-24
E9	—	A311TB2-5
E10	—	A311TB1-6
E11	—	A308R7
E12	+105V	XA302-11
E13	—	A311TB1-7
E14	—	A311TB2-1
E15	—	A311TB6-1
E16	—	A311TB6-4

*NOTE: Only immediate (next) destinations are shown.



NOTES:

1. CAPACITORS ARE BENEATH THE PRINTED CIRCUIT BOARD WITH THE EXCEPTION OF C24 AND C25.
2. METAL BARS (SHADED AREAS) ARE ON THE COMPONENT SIDE OF THE PRINTED CIRCUIT BOARD.
3. THE CATHODE OF ALL DIODES IS THE OUTER CASE OF THE DIODE. A BEAD IS INSTALLED ON THE CATHODE LEAD.
4. REFERENCE DESIGNATION PREFIX IS A303.

Figure 5-34. A303 Capacitor Board Assembly, Parts Location and Connection Diagram

Table 5-26. A304 Large Heat Sink Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
B2	3160-0072	Fan, Tubeaxial, 115V, 60 hz	28480	3160-0072
P1	1251-0136	Connector, 32 Pin, Male	02660	26-4100-32P
Q1 thru Q8	1850-0198	Transistor, Ge, PNP	04713	2N2156
Q10, 11	1850-0098	Transistor, Ge, PNP	28480	1850-0098
Q9	1854-0264	Transistor, Si, NPN	04713	2N3715
S2	3103-0004	Thermoswitch, 115V, 2A	28480	3103-0004
XA304	1251-0137	Connector, 32 Contact, Female	02660	26-4200-32S

PIN INDEX

PIN	TO/FROM	PIN	TO/FROM
1	A303C19(-)	17	XA304-18
2	A308R17	18	A310R13
3	A307R45	19	XA304-20
4	A308R17	20	A310R14
5	XA304-6	21	XA304-22
6	A310R8	22	A310R15
7	XA304-8	23	A307R47
8	A310R9	24	A306R16
9	XA304-10	25	–
10	A310R10	26	A311TB1-1
11	XA304-12	27	A311TB1-3
12	A310R11	28	XA305-20
13	A307R46	29	A100TB1-2
14	A308R18	30	–
15	XA304-16	31	–
16	A310R12	32	–

Figure 5-35. A304 Large Heat Sink Assembly, Parts Location and Connection Diagram (Sheet 1 of 2)

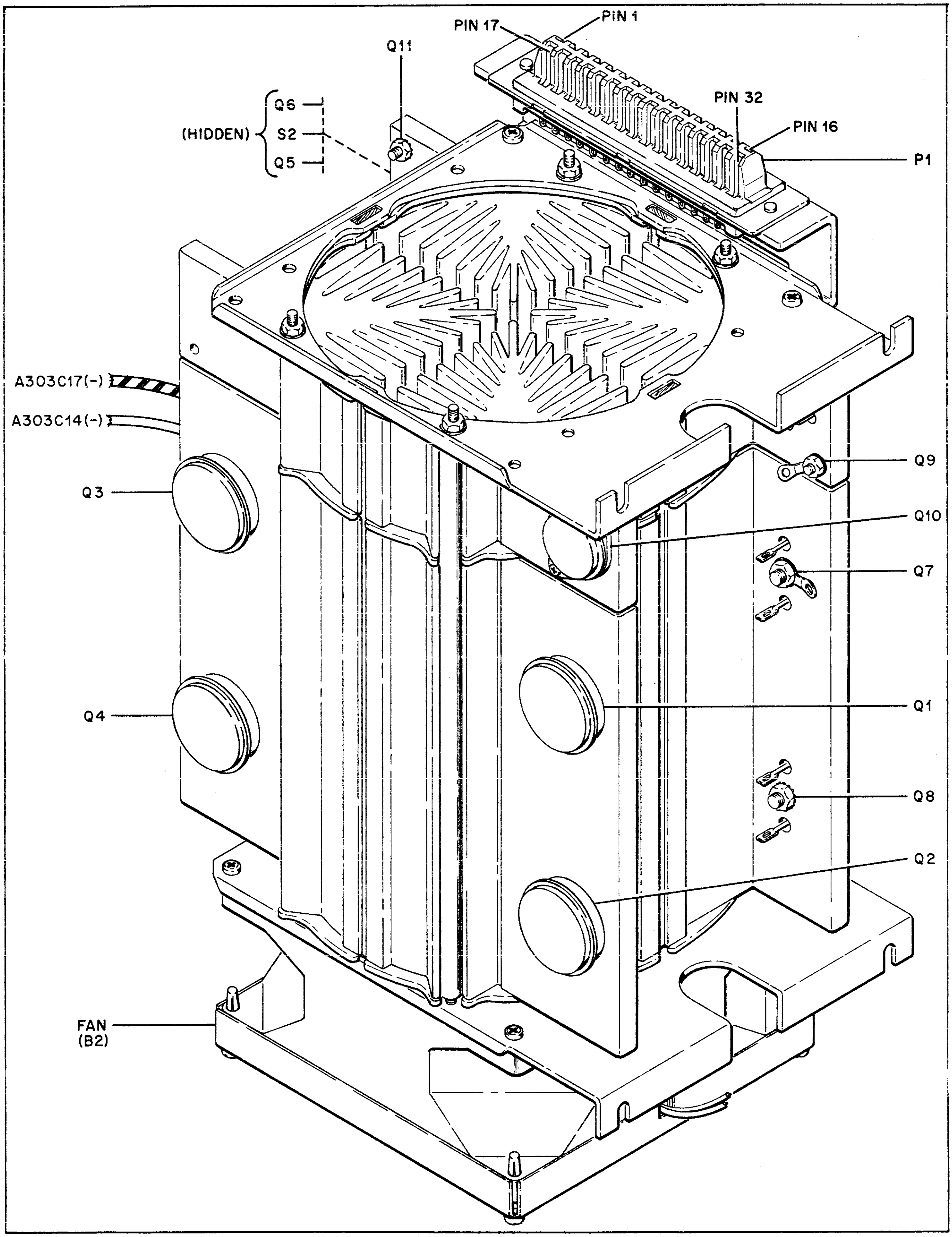


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Figure 5-35. A304 Large Heat Sink Assembly, Parts Location and Connection Diagram (Sheet 2 of 2)

Table 5-27. A305 Small Heat Sink Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
B3	3160-0072	Fan Tubeaxial, 115V, 60 hz	28480	3160-0072
P1	1251-0136	Connector, 32 Pin, Male	02660	26-4100-32P
Q12, 15, 16	1853-0063	Transistor, Si, PNP	04713	MJ2268
Q13, 17	1850-0098	Transistor, Ge, PNP	28480	1850-0098
Q14, 18, 19	1854-0264	Transistor, Si, NPN	04713	2N3715
S1	3103-0004	Thermoswitch, 115V, 2A	28480	3103-0004
XA305	1251-0137	Connector, 32 Contact, Female	02660	26-4200-32S

PIN INDEX

PIN	TO/FROM	PIN	TO/FROM
1	A308R19	17	A311TB1-2
2	A303C23(-)	18	A311TB1-4
3	A303C26(+)	19	A307-A
4	A303C22(-)	20	XA304-28
5	A307R51	21	—
6	A307R50	22	—
7	A306R54	23	—
8	A306R40	24	—
9	A306R53	25	—
10	A306R52	26	—
11	A307R57	27	—
12	A306R55	28	—
13	A306R56	29	—
14	A306R49	30	—
15	A306R39	31	—
16	A307R48	32	—

Figure 5-36. A305 Small Heat Sink Assembly, Parts Location and Connection Diagram (Sheet 1 of 2)

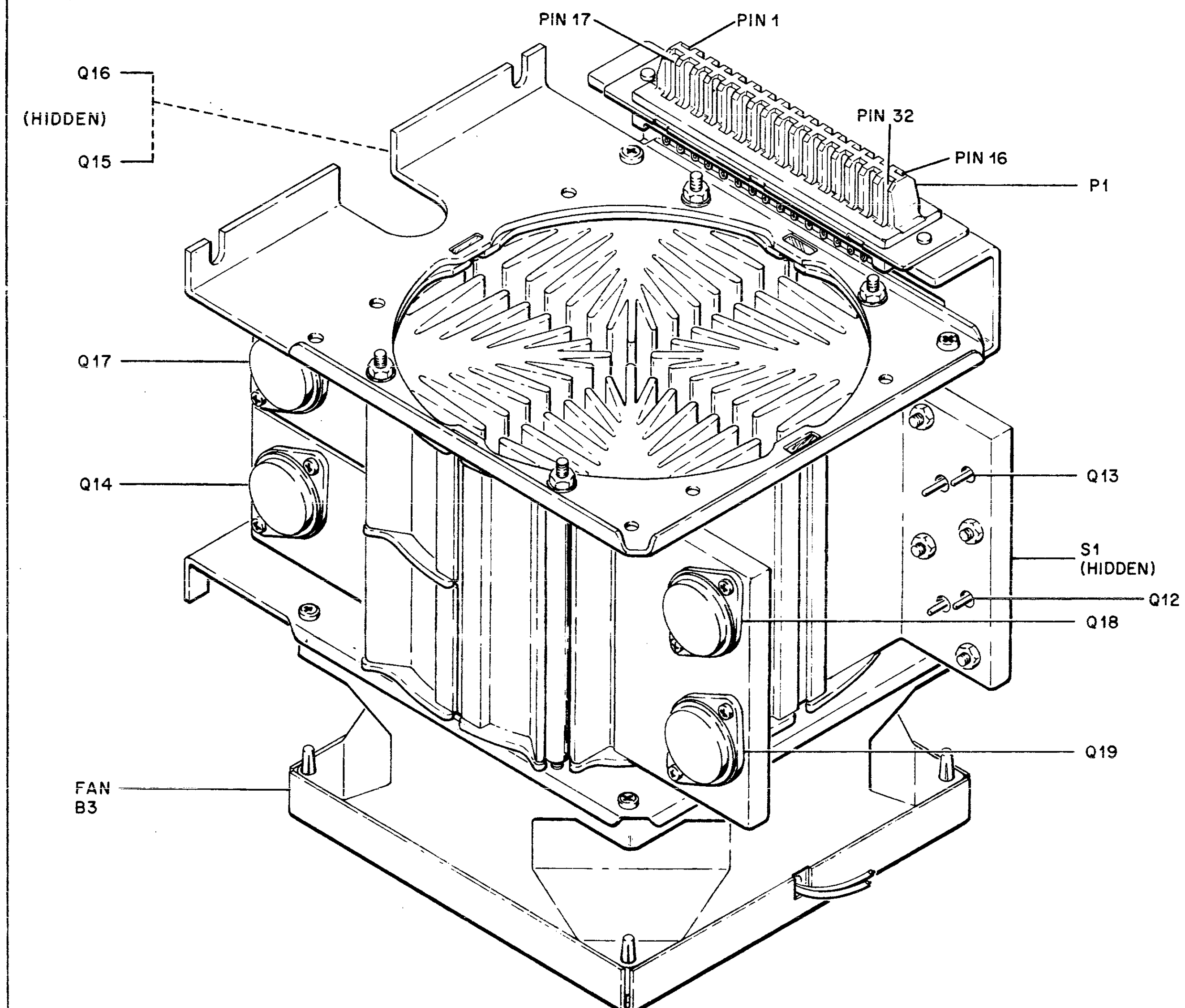

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Figure 5-36. A305 Small Heat Sink Assembly, Parts Location and Connection Diagram (Sheet 2 of 2)

Table 5-28. A306 Component Board Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R16	0811-2097	Resistor, Fxd, WW, 0.25 ohms, 3%, 5w	28480	0811-2097
R39, 49	0761-0038	Resistor, Fxd, Met Ox, 5600 ohms, 5%, 1w	28480	0761-0038
R40, 54	0811-2139	Resistor, Fxd, WW, 2.2 k, 5%, 3w	28480	0811-2097
R52, 53	0813-0029	Resistor, Fxd, WW, 1 ohm, 3%, 3w	28480	0813-0029
R55, 56	0811-0040	Resistor, Fxd, WW, 1 ohm, 1%, 5w	28480	0811-0040

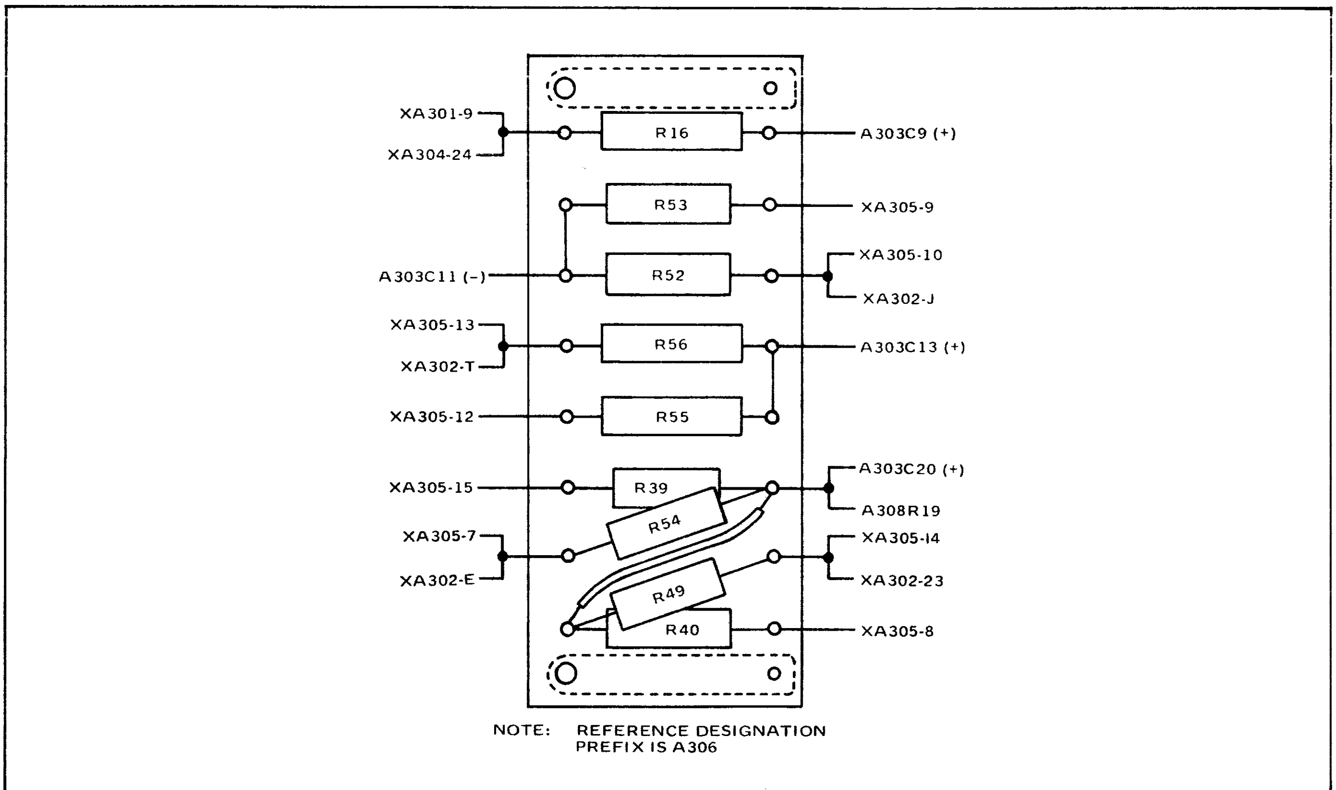

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Figure 5-37. A306 Component Board Assembly, Parts Location and Connection Diagram

Table 5-29. A307 Component Board Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R45, 46	0761-0058	Resistor, Fxd, Met Ox, 750 ohms, 5%, 1w	28480	0761-0058
R47	0812-0099	Resistor, Fxd, WW, 1 k, 5%, 5w	28480	0812-0099
R48	0811-2097	Resistor, Fxd, WW, 0.25 ohm, 3%, 5w	28480	0811-2097
R50	0811-0040	Resistor, Fxd, WW, 1 ohm, 1%, 5w	28480	0811-0040
R51	0767-0003	Resistor, Fxd, Met Ox, 1.20 k, 5%, 3w	28480	0767-0003
R57	0811-1339	Resistor, Fxd, WW, 500 ohms, 5%, 5w	28480	0811-1858
JUMPER A	No Number	Bus Wire, No. 18	00000	OBD

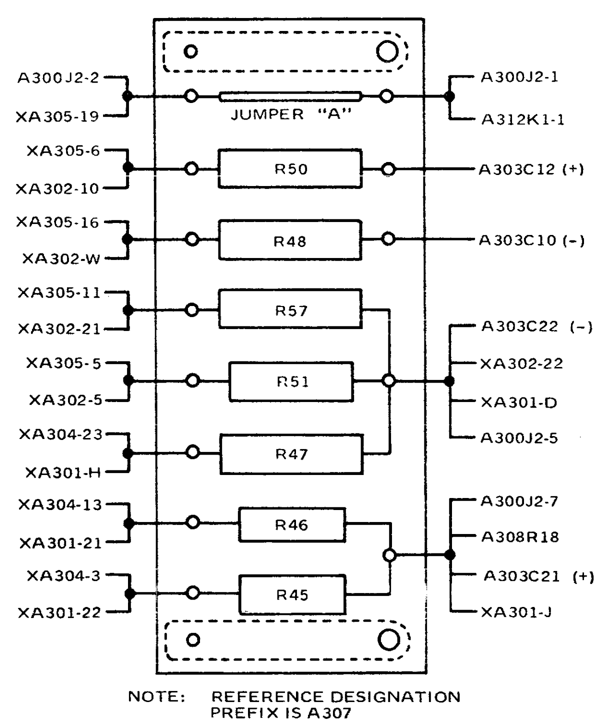

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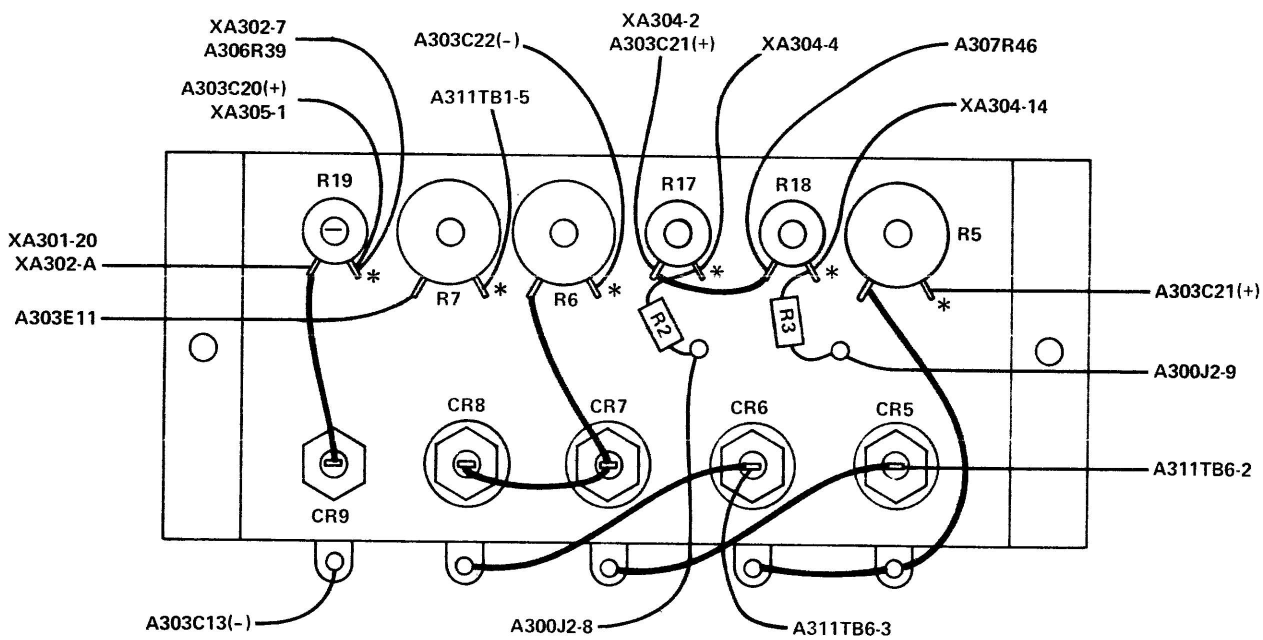
Figure 5-38. A307 Component Board Assembly, Parts Location and Connection Diagram

Table 5-30. A308 Component Board Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
CR5 thru CR8	1901-0496	Diode, Si, 100 PIV, 12A	04713	MR1121
CR9	1902-1215	Diode, Breakdown, 20.0V, 2%, 10w	04713	1N29848
R2,3	0757-0159	Resistor, Fxd, Flm, 1000 ohms, 1%, 1/2w	28480	0757-0159
R5, 6	0811-2510	Resistor, Fxd, WW, 0.1 ohm, 5%, 25w	28480	0811-2501
R7	0811-2509	Resistor, Fxd, WW, 0.5 ohm, 5%, 25w	28480	0811-2509
R17, 18	0811-2107	Resistor, Fxd, WW, 75 ohms, 5%, 10w	28480	0811-2107
R19	0815-0005	Resistor, Fxd, WW, 62 ohms, 5%, 10w	28480	0815-0005



NOTES:

1. * INDICATES ATTACHMENT TO OUTER LUGS OF RESISTORS.
2. FRAME GROUND FOR THE ENTIRE POWER SUPPLY IS MADE AT DIODE CR9.
3. DIODES CR5, CR6, CR7, AND CR8 ARE INSULATED FROM THE MOUNTING BRACKET BY MICA WASHERS AND "O" RINGS.
4. DIODE MOUNTING NUTS ARE TIGHTENED WITH A MAXIMUM TORQUE OF 12 INCH-LBS.
5. WHEN DIODES CR5, CR6, CR7, CR8, AND CR9 ARE INSTALLED USE HEAT-CONDUCTING SILICON COMPOUND (DOW-CORNING NO. 5 SILICON DIELECTRIC).
6. REFERENCE DESIGNATION PREFIX IS A308.

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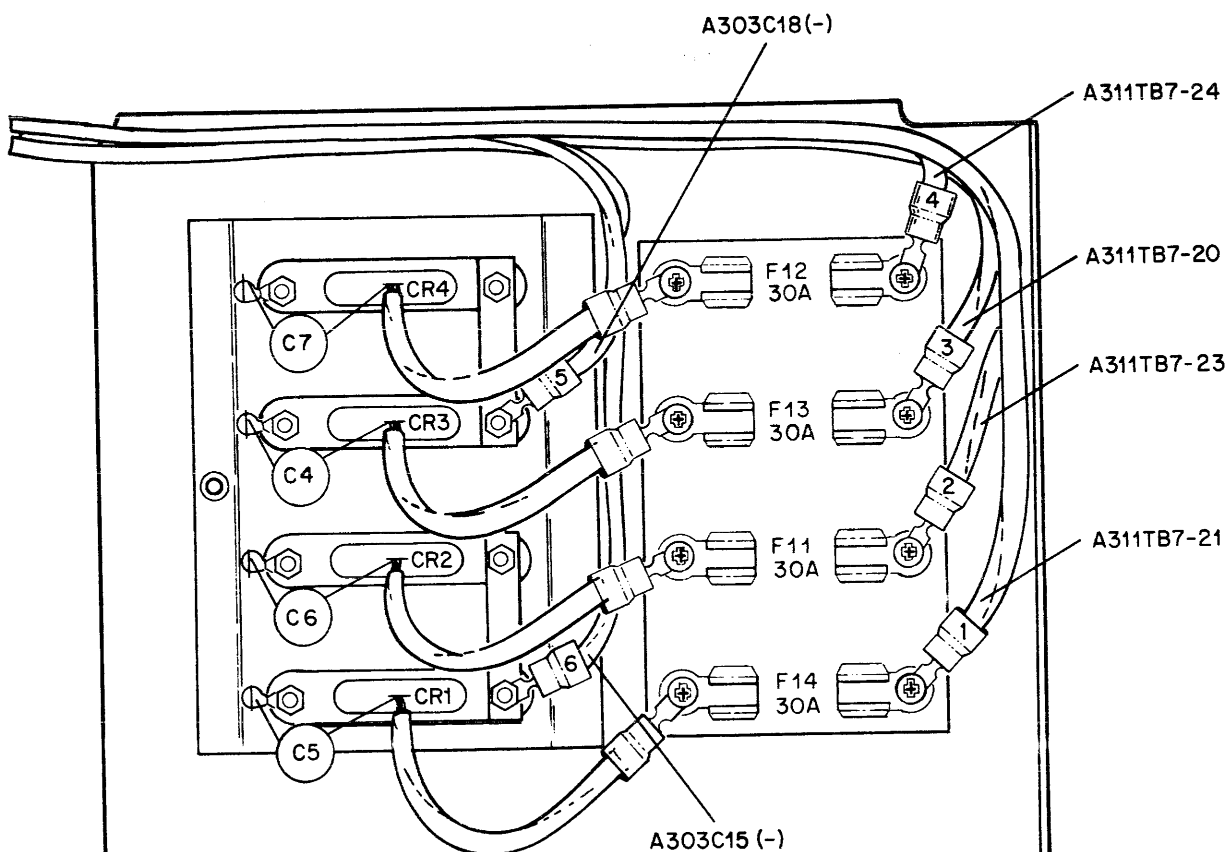
Figure 5-39. A308 Component Board Assembly, Parts Location and Connection Diagram

Table 5-31. A309 Component Board Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C4 thru C7	0150-0093	Capacitor, Fxd, Cer, 0.01 μf, +80 -20%, 100VDCW	28480	0150-0093
CR1 thru CR4	1901-0344	Diode, Si	04713	SR2014
F11 thru F14	2110-0256	Fuse, 30A, 32V, medium blow	00000	OBD



NOTE:
REFERENCE DESIGNATION PREFIX IS A309

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Figure 5-40. A309 Component Board Assembly, Parts Location and Connection Diagram

Table 5-32. A310 Component Board Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R8 thru R15	0811-2078	Resistor, Fxd, WW, 0.15 ohms, 3%, 12w	28480	0811-2078
R23	0811-2648	Resistor, Fxd, WW, 5 ohms, 3%, 12.5w	28480	0811-2648

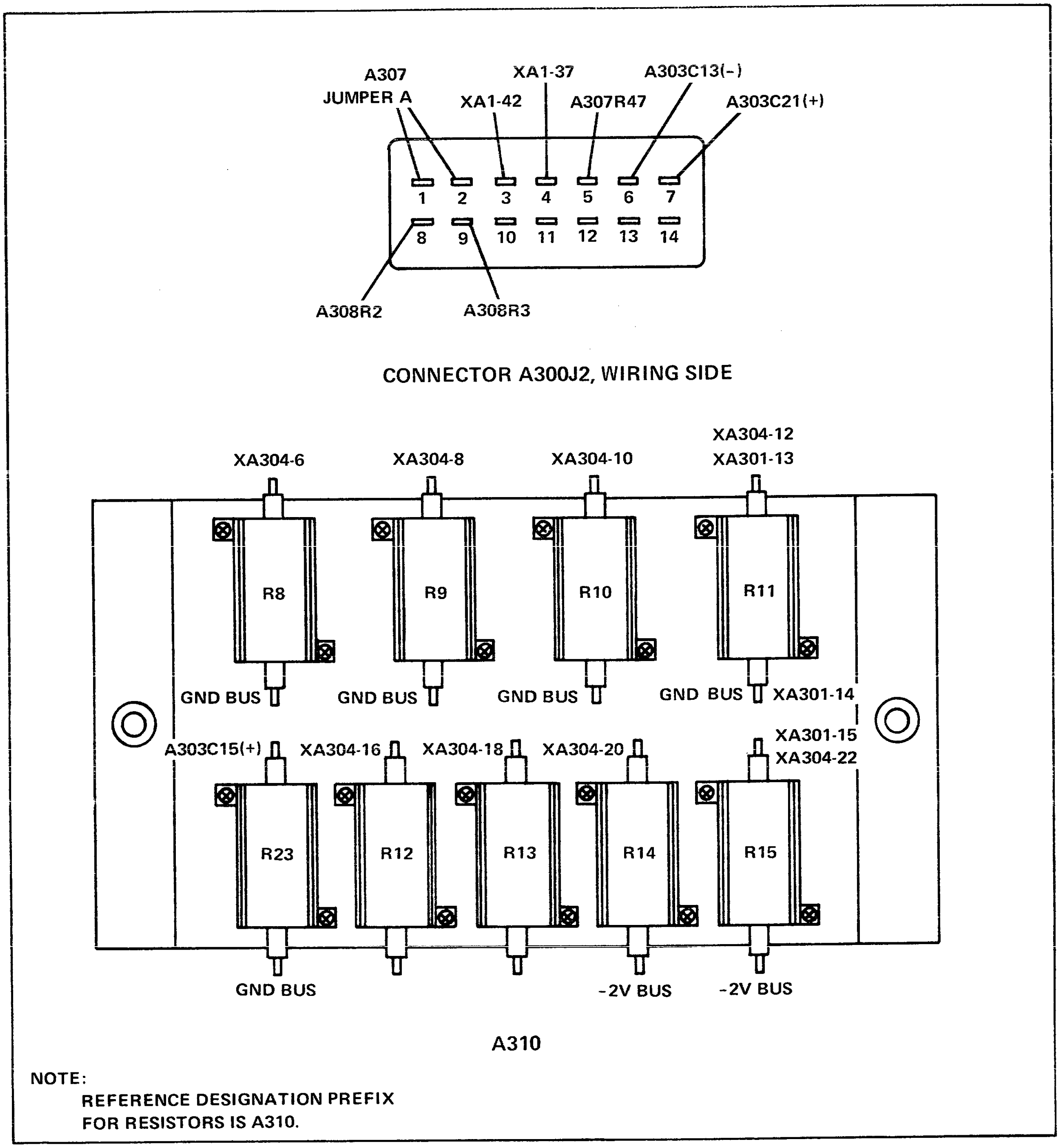

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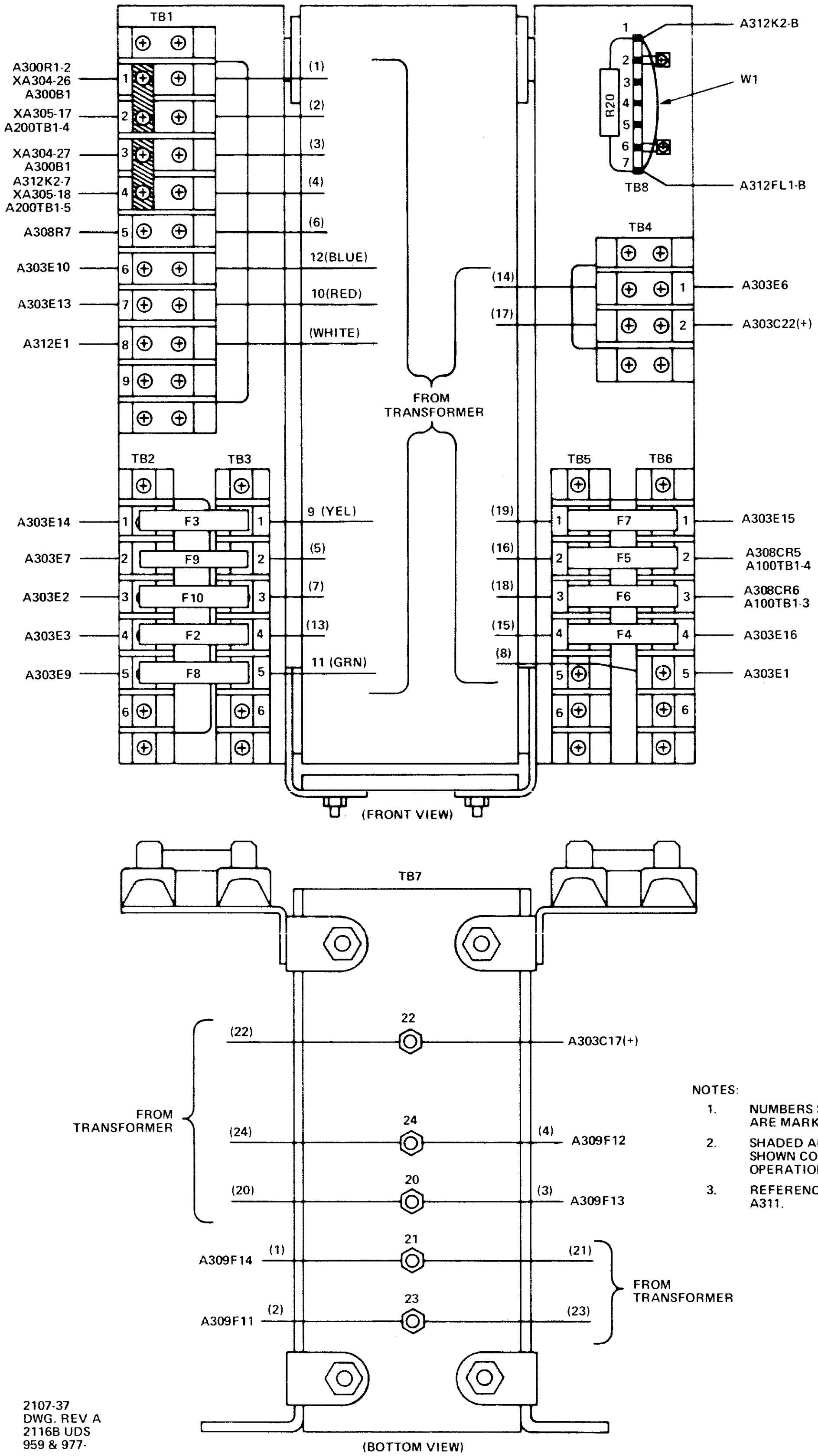
Figure 5-41. A310 Component Board Assembly and Connector A300J2, Parts Location and Connection Diagram

Table 5-33. A311 Transformer Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
F2	2110-0013	Fuse, 3.2A, 125V, slow blow	00000	OBD
F3, 8	2110-0044	Fuse, 0.3A, 250V, slow blow	00000	OBD
F4 thru F7, 9	2110-0023	Fuse, 6.25A, 250V, slow blow	00000	OBD
F10	2110-0014	Fuse, 4A, 125V, slow blow	00000	OBD
T1	9100-1219	Transformer	28480	9100-1219
TB1	0360-1256	Terminal Board	00000	OBD
TB2, 3, 5, 6	0360-1254	Terminal Board	00000	OBD
TB4	0360-1130	Terminal Board	00000	OBD
TB7	02116-0064	Terminal Block	28480	02116-0064

Table 5-33A. A311 Transformer Assembly, Reference Designation Index for Computers with Serial Number Prefixes 959- and 977-

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
F2	2110-0013	Fuse, 3.2A, 125V, slow blow	00000	OBD
F3,8	2110-0044	Fuse, 0.3A, 250V, slow blow	00000	OBD
F4 thru F7,9	2110-0023	Fuse, 6.25A, 250V, slow blow	00000	OBD
F10	2110-0014	Fuse, 4A, 125V, slow blow	00000	OBD
R20	0811-2735	Resistor, Fxd, WW, 2500 ohms, 3%, 10W	28480	0811-2735
T1	9100-1219	Transformer	28480	9100-1219
TB1	0360-1256	Terminal Board	00000	OBD
TB2,3,5,6	0360-1254	Terminal Board	00000	OBD
TB4	0360-1130	Terminal Board	00000	OBD
TB7	02116-0064	Terminal Block	28480	02116-0064
TB8	0360-1589	Terminal Board	28480	0360-1589



NOTES:
1. NUMBERS SHOWN IN PARENTHESIS ARE MARKED ON WIRE.
2. SHADED AREAS INDICATE JUMPERS SHOWN CONNECTED FOR 115-VOLT OPERATION.
3. REFERENCE DESIGNATED PREFIX IS A311.

Figure 5-42A. A311 Transformer Assembly, Parts Location Diagram for Computers with Serial Number Prefixes 959- and 977-

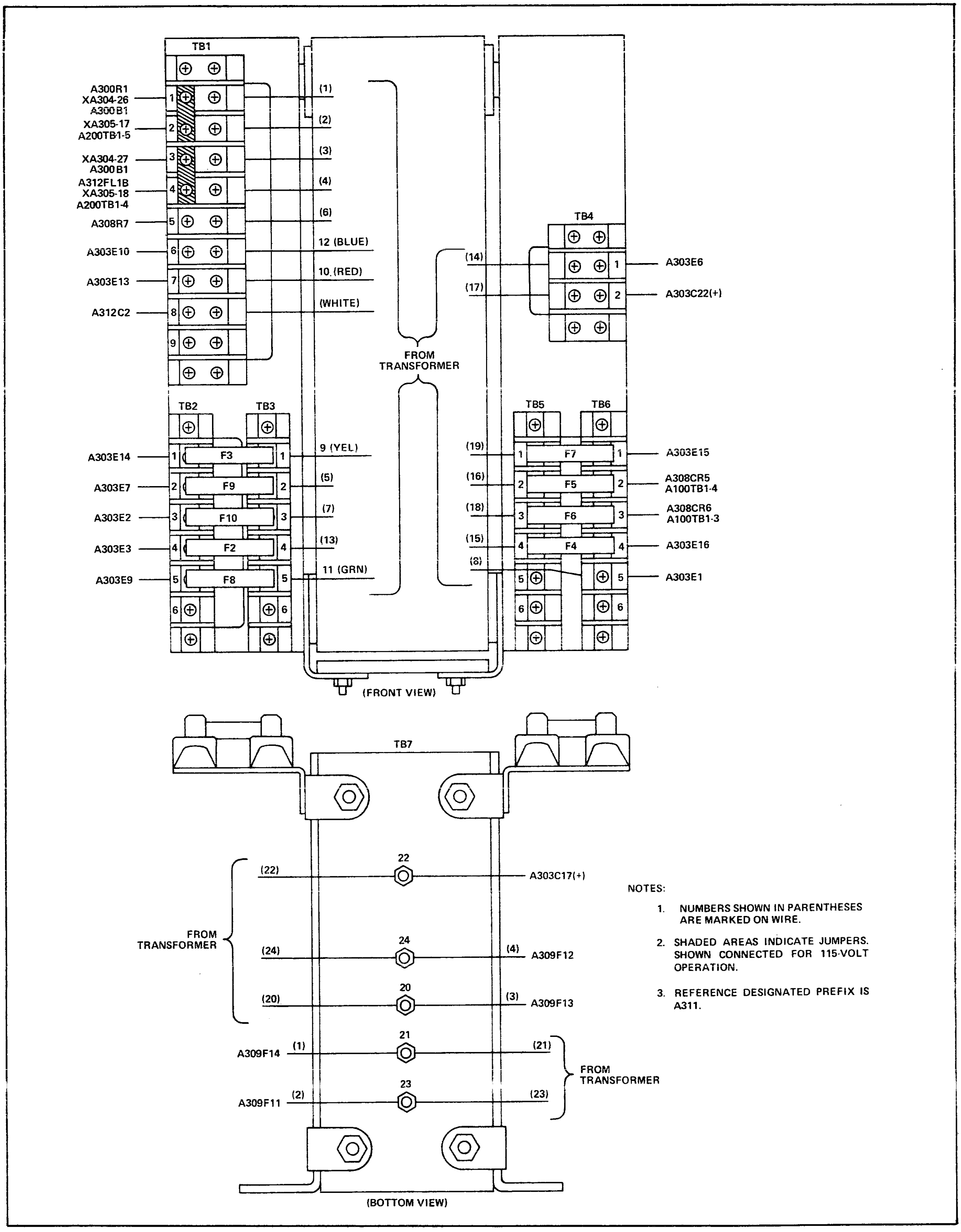


Figure 5-42. A311 Transformer Assembly, Parts Location and Connection Diagram

Table 5-34. A312 AC Input Section, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C2A, 2B	0160-3043	Capacitor, Fxd, Cer, 2 x 0.005 μf, 20% 250VDCW	56289	29C147A-CHD
CR10	1901-0045	Diode, Si, 0.75A, 100 PIV	04713	SR1358-7
F1	2110-0025	Fuse, 15A, 32V, slow blow	00000	OBD
FL1	9100-1834	Line Filter, 20A, AC	28480	9100-1834
K1	0490-0372	Relay, 12VDC 50-ohm coil	73096	WHV012D5-503
XF1	1400-0084	Fuse Holder	00000	OBD

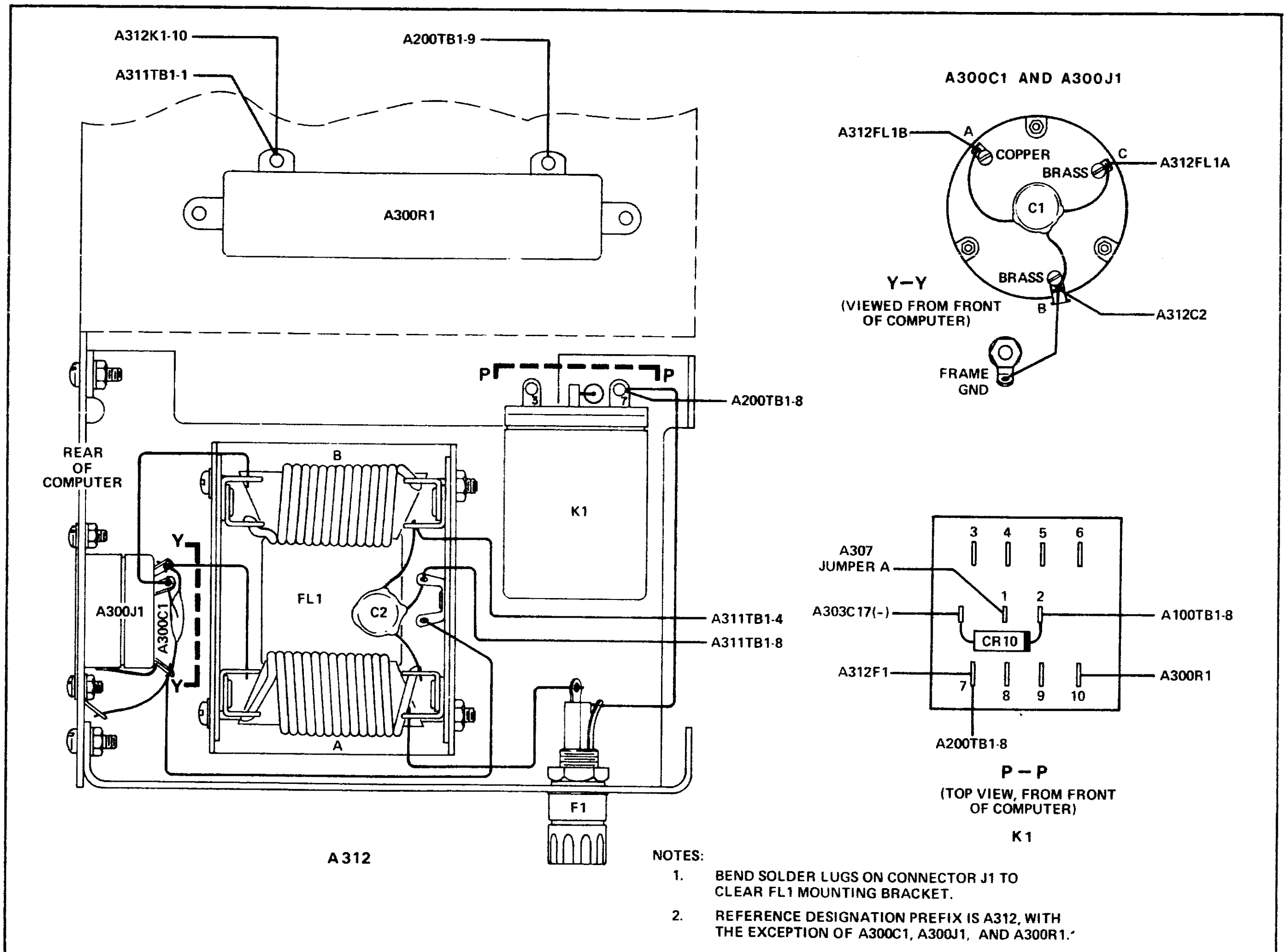


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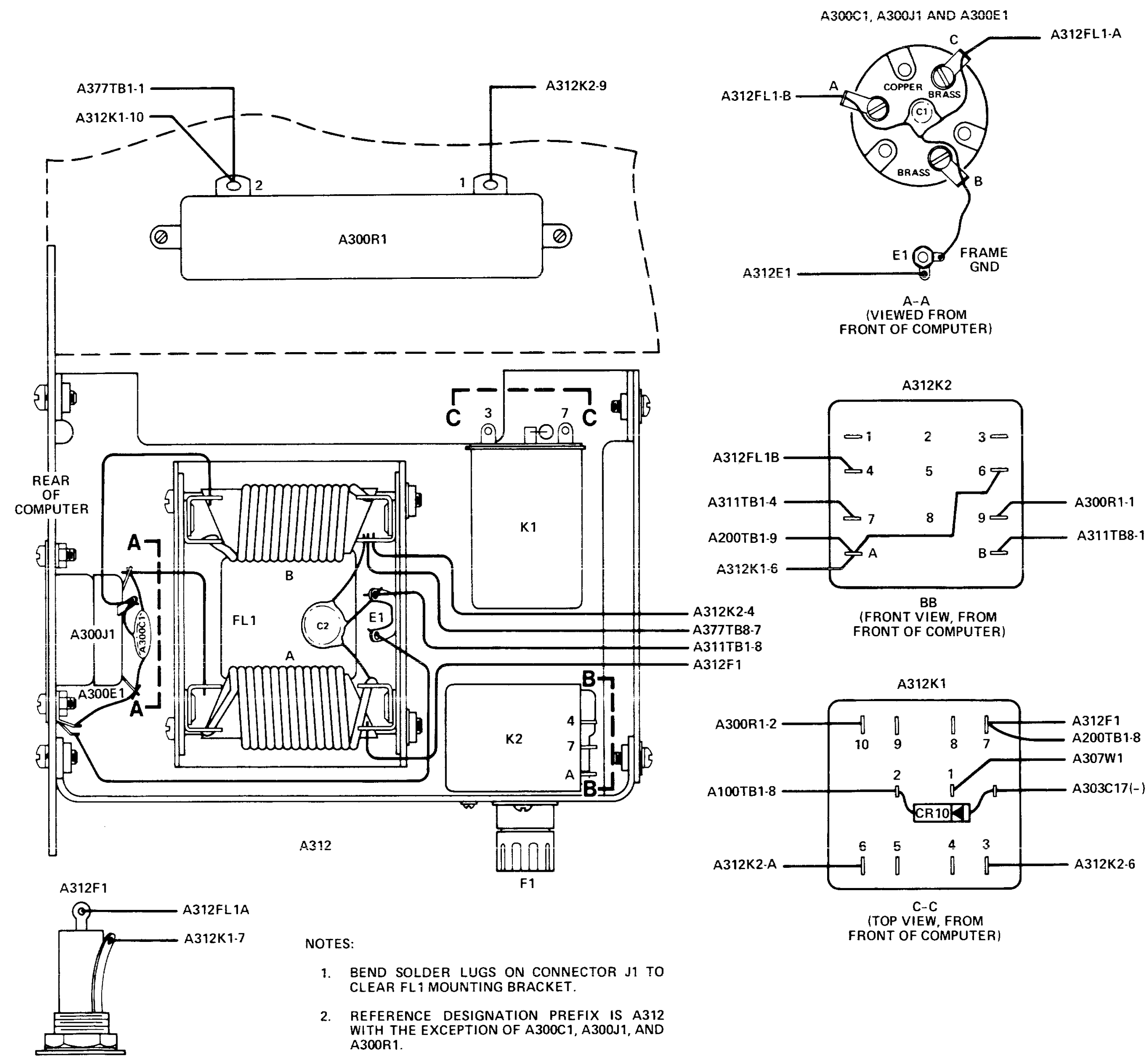
Figure 5-43. A312 AC Input Section, Capacitor A300C1, Connector A300J1, and Resistor A300R1, Parts Location and Connection Diagram

Table 5-34A. A312 AC Input Section, Reference Designation Index for Computers with Serial Number Prefixes 959- and 977-

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C2A,2B	0160-3043	Capacitor, Fxd, Cer, 2x0.005 uF, 20%, 250 VDCW	56289	29C147A-CHD
CR10	1901-0045	Diode, Si, 0.75A, 100 PIV	04713	SR1358-7
F1	2110-0025	Fuse, 15A, 32V, slow blow	00000	OBD
FL1	9100-1834	Line filter, 20A, AC	28480	9100-1834
K1	0490-0372	Relay, 12VDC 50-ohm coil	73096	WHV012D5-503
K2	0490-0892	Relay, 120VAC, 2.25K-ohm coil, 10A	28480	0490-0892
XF1	1400-0084	Fuse Holder	00000	OBD

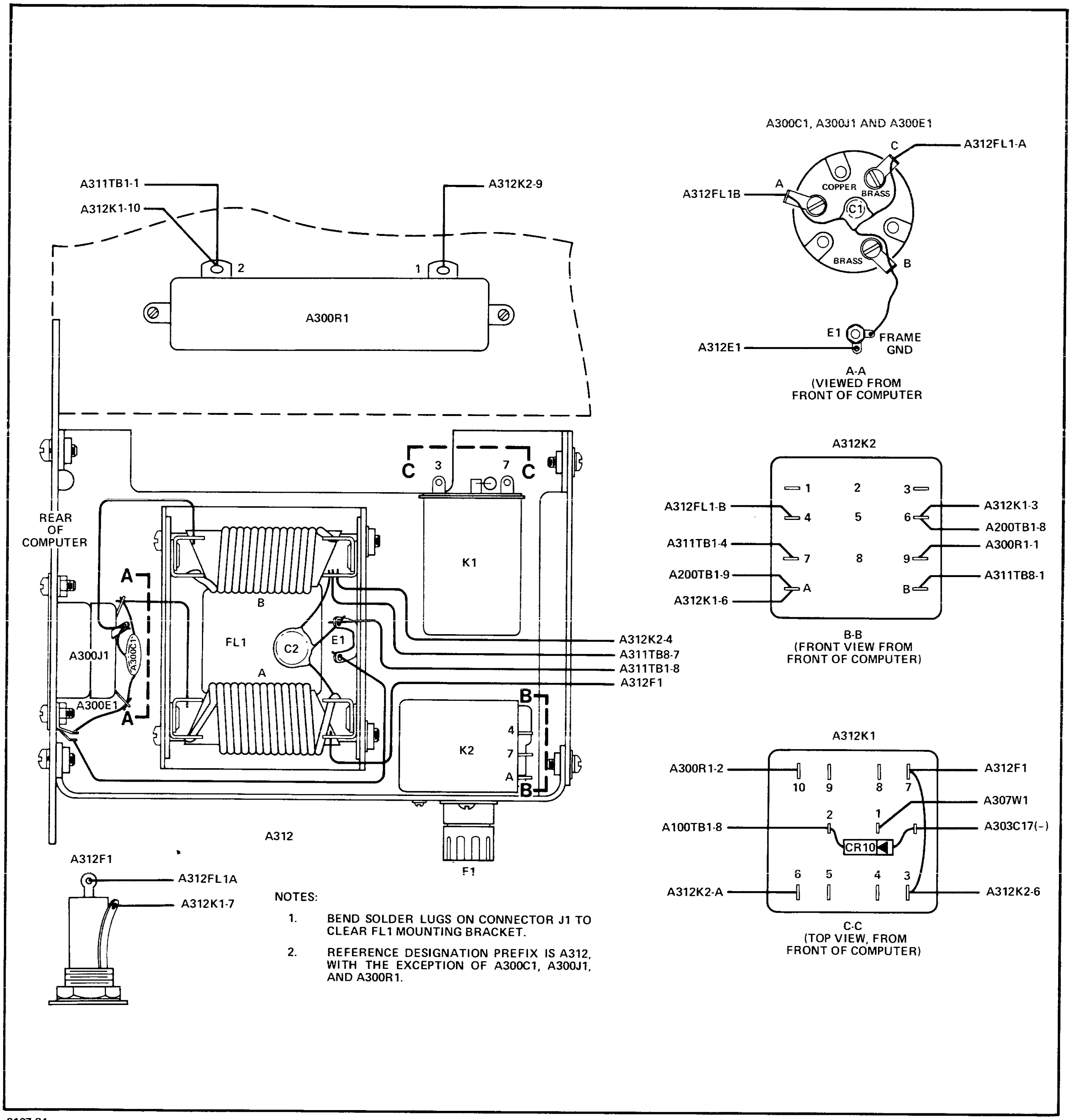


NOTES:

1. BEND SOLDER LUGS ON CONNECTOR J1 TO CLEAR FL1 MOUNTING BRACKET.
2. REFERENCE DESIGNATION PREFIX IS A312 WITH THE EXCEPTION OF A300C1, A300J1, AND A300R1.

2107-24
2116B UDS
959-

Figure 5-43A. A312 AC Input Section, Parts Location and Connection Diagram for Computers with Serial Number Prefix 959-



2107-24
2116B
977-

Figure 5-43B. A312 AC Input Section, Parts Location and Connection Diagram for Computers with Serial Number Prefix 977-

Specifications, Transformer A311T1

XFMR WIRES	AC VOLTAGE (RMS) UNLOADED	AC VOLTAGE (RMS) LOADED	MAXIMUM CURRENT (AMPS, DC)	WINDING RESISTANCE (OHMS)
1-3	115.0	115.0	– –	0.130 ± 10%
2-4	115.0	115.0	– –	0.150 ± 10%
5-6	43.4	41.8	3.0	0.125 ± 10%
7-8	8.9	8.5	4.0	0.032 ± 10%
9-10 (yellow-red)	37.6	36.0	0.1	1.448 ± 10%
11-12 (green-blue)	37.6	36.0	0.1	1.443 ± 10%
13-14	12.3	12.0	2.0	0.042 ± 10%
15-19	56.0	53.5	4.0	0.128 ± 10%
16-18	37.8	35.5	12.0	0.093 ± 10%
20-24	18.8	17.8	22.5	0.018 ± 10%
21-23	15.3	14.2	22.5	0.010 ± 10%

NOTES:

FOR SECONDARY WINDINGS, THE UNLOADED VOLTAGE IS THE OPEN-CIRCUIT VOLTAGE (FUSE REMOVED). THE LOADED VOLTAGE IS FOR A FULLY LOADED SECONDARY (MAXIMUM DC CURRENT DRAWN FROM THE RECTIFIER). DEPENDING ON THE OPTIONAL DEVICES INSTALLED, SECONDARIES MAY NOT BE FULLY LOADED WHEN FUSE IS INSTALLED.

THE MAXIMUM CURRENT CITED IS THE DC CURRENT DRAWN FROM THE RECTIFIER.

Logic Supply Regulator Card A301 Typical Voltages
(See Note 9)

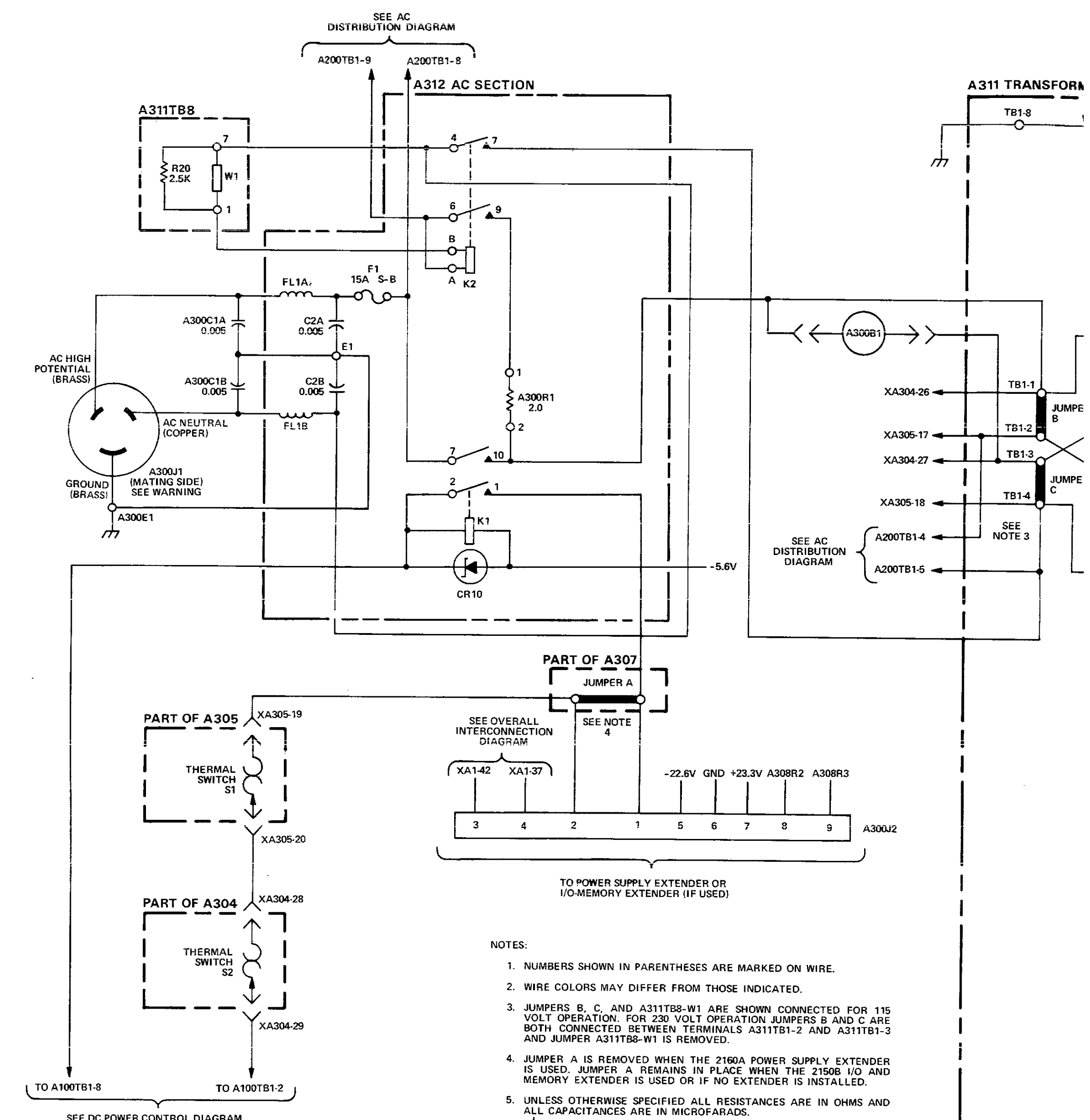
TEST POINT		DC VOLTAGE
Q30	Base	+ 4.5
Q31	Base	+ 4.5
Q32	Emitter	- 1.2
Q33	Base	+ 0.1
	Collector	- 2.3
Q35	Base	0.0
Q37	Emitter	- 3.3
Q38	Base	- 1.9
	Collector	- 4.4
Q39	Base	+ 0.7
Q41	Emitter	+12.7
Q42	Base	+11.3
	Collector	+14.0

Memory Supply Regulator Card A302 Typical Voltages
(See Note 9)

TEST POINT		DC VOLTAGE
Q50	Emitter	- 8.3
	Base	- 9.0
	Collector	-14.0
Q51	Emitter	- 8.3
	Base	- 9.0
Q52	Emitter	-13.1
Q53	Base	-11.5
Q54A	Emitter	- 0.7
	Base	0.0
	Collector	+24.5
Q55	Emitter	+23.5
Q56	Base	+21.7
Q57	Emitter	+ 0.7
	Base	0.0
	Collector	-25.2
Q58	Emitter	+ 0.7
Q59	Emitter	-24.4
Q60	Base	-21.4
Q61A	Emitter	- 0.7
	Base	0.0
	Collector	+34.0
Q63	Emitter	+32.6
Q64	Base	+30.6
A302-1 (+22V temp sense)		- 7.9
A302-13 (+32V temp sense)		- 7.9

Capacitor Board Assembly A303 Typical Voltages
(See Note 9)

TEST POINT	MEMORY 8K	MEMORY 16K
A303C14(-)	- 3.9V	- 3.4V
A303C17(-)	- 6.0V	- 5.6V
A303C19(-)	-12.9V	-12.4V
A303C20(+)	+36.9V	+35.5V
A303C21(+)	+22.4V	+23.3V
A303C22(-)	-23.8V	-22.6V
A303C23(-)	-37.2V	-36.4V
A303C26(+)	+58.0V	+56.4V
A303E8	-86.9V	-84.5V
A303E12	+107V	+105V



WARNING

FOR SAFETY REASONS THE HIGH POTENTIAL SIDE OF THE AC LINE MUST BE CONNECTED AS SHOWN, PLACING FUSE F1 ON THE HIGH POTENTIAL SIDE OF THE LINE.

IF THE NEGATIVE LEAD OF A TEST INSTRUMENT IS CONNECTED TO THE METAL CASE OF THE INSTRUMENT, THE LEAD MUST BE CONNECTED ONLY TO THE GROUND. ALSO, THE NEGATIVE LEAD MUST BE CONNECTED FIRST AND REMOVED LAST.

NOTES:

1. NUMBERS SHOWN IN PARENTHESES ARE MARKED ON WIRE.
2. WIRE COLORS MAY DIFFER FROM THOSE INDICATED.
3. JUMPERS B, C, AND A311TB8-W1 ARE SHOWN CONNECTED FOR 115 VOLT OPERATION. FOR 230 VOLT OPERATION JUMPERS B AND C ARE BOTH CONNECTED BETWEEN TERMINALS A311TB1-2 AND A311TB1-3 AND JUMPER A311TB8-W1 IS REMOVED.
4. JUMPER A IS REMOVED WHEN THE 2160A POWER SUPPLY EXTENDER IS USED. JUMPER A REMAINS IN PLACE WHEN THE 2150B I/O AND MEMORY EXTENDER IS USED OR IF NO EXTENDER IS INSTALLED.
5. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
6. THIS SYMBOL INDICATES CONNECTION TO COMPUTER FRAME MADE AT MOUNTING SCREW OF A300J1 AND AT ANODE OF A308CR9.
7. THIS SYMBOL INDICATES POWER SUPPLY COMMON RETURN.
8. ALL VOLTAGES MARKED ON THE ILLUSTRATION ARE APPROXIMATE UNLESS REGULATED.
9. VOLTAGES SPECIFIED IN THE TABLES ARE TYPICAL AND MEASURED UNDER THE FOLLOWING CONDITIONS:
   a. 115 VAC, 60 Hz MAIN POWER INPUT.
   b. ALL CARDS REMOVED FROM THE I/O SLOTS EXCEPT THE CARDS IN SLOT 201 AND 202.
   c. COMPUTER HALTED.
   d. MINIMUM WARM UP PERIOD OF 30 MINUTES PRIOR TO TAKING MEASUREMENTS.
   e. AMBIENT TEMPERATURE IS +25 DEGREES C (+77 DEGREES F).
   f. SUPPLY VOLTAGES SET TO +32V, +22.8V, -22.8V, +12V, -12V, +4.5V AND -2V (ALL ± 1%) AS MEASURED AT TEST JACKS ON OVER VOLTAGE PROTECTION ASSEMBLY A121.
10. ALL PINS SHOWN ON A304 AND A305 ARE IN CONNECTORS A304P1 AND A305P1, RESPECTIVELY.
11. THERMAL SWITCHES S1 AND S2 OPEN WHEN TEMPERATURE RISES ABOVE 75 ± 5°C (167 ± 9°F).

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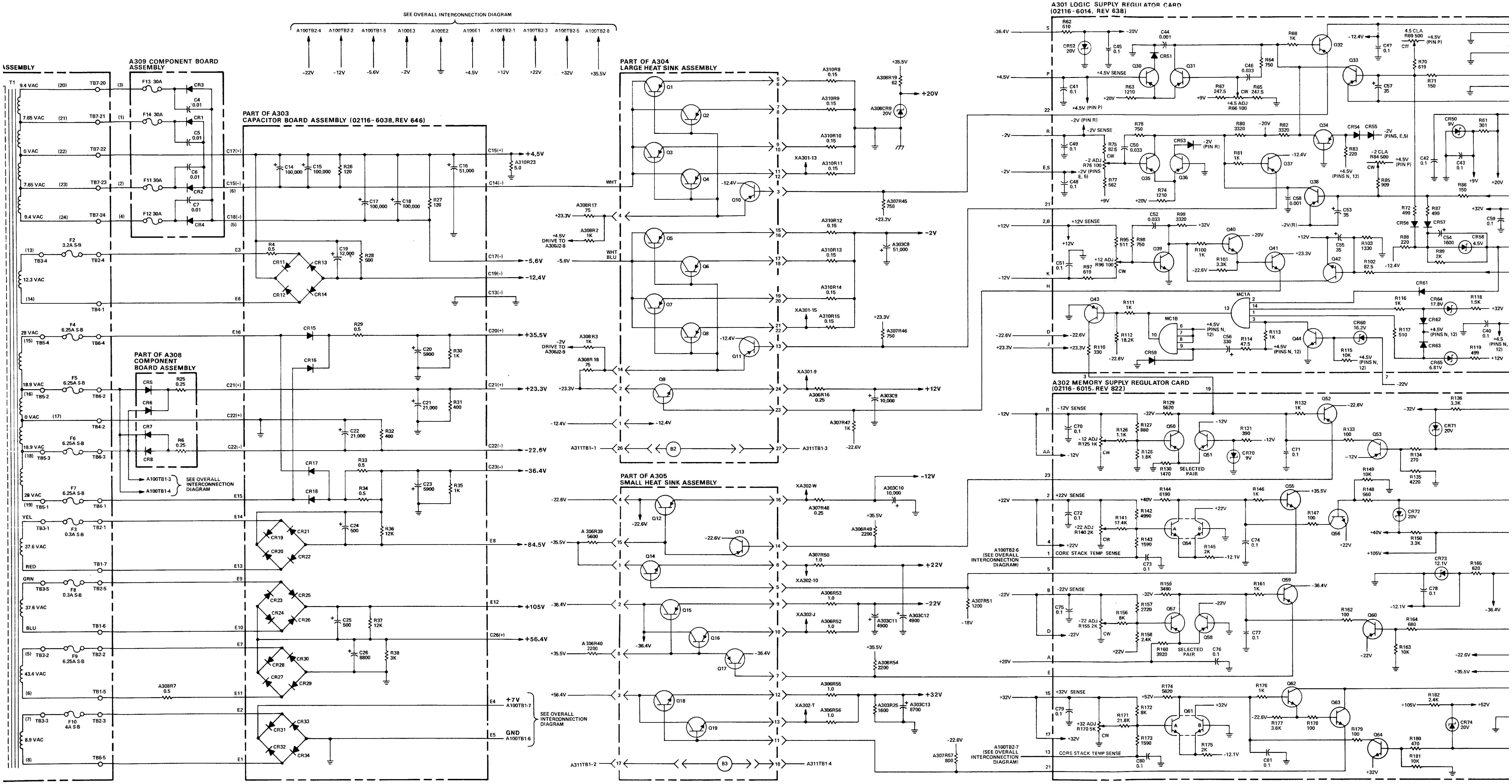


Figure 5-44A. A300 Power Supply
Schematic Diagram for Comp

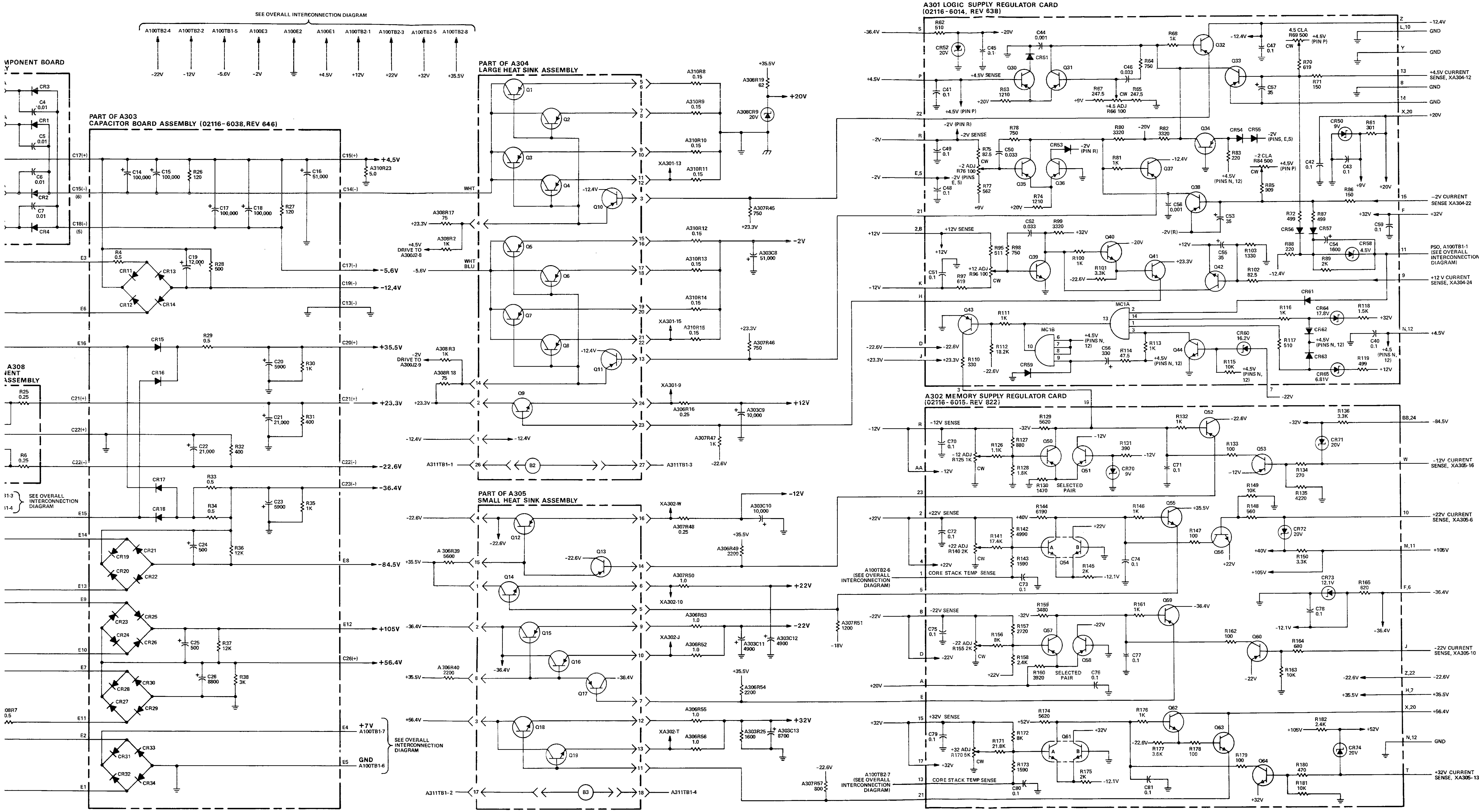


Figure 5-44A. A300 Power Supply Assembly (02116-6124), Schematic Diagram for Computers with Serial Number Prefix 959-

Specifications, Transformer A311T1

XFMR WIRES	AC VOLTAGE (RMS) UNLOADED	AC VOLTAGE (RMS) LOADED	MAXIMUM CURRENT (AMPS, DC)	WINDING RESISTANCE (OHMS)
1-3	115.0	115.0	--	0.130 ± 10%
2-4	115.0	115.0	--	0.150 ± 10%
5-6	43.4	41.8	3.0	0.125 ± 10%
7-8	8.9	8.5	4.0	0.032 ± 10%
9-10 (yellow-red)	37.6	36.0	0.1	1.448 ± 10%
11-12 (green-blue)	37.6	36.0	0.1	1.443 ± 10%
13-14	12.3	12.0	2.0	0.042 ± 10%
15-19	56.0	53.5	4.0	0.128 ± 10%
16-18	37.8	35.5	12.0	0.093 ± 10%
20-24	18.8	17.8	22.5	0.018 ± 10%
21-23	15.3	14.2	22.5	0.010 ± 10%

NOTES:

FOR SECONDARY WINDINGS, THE UNLOADED VOLTAGE IS THE OPEN-CIRCUIT VOLTAGE (FUSE REMOVED). THE LOADED VOLTAGE IS FOR A FULLY LOADED SECONDARY (MAXIMUM DC CURRENT DRAWN FROM THE RECTIFIER). DEPENDING ON THE OPTIONAL DEVICES INSTALLED, SECONDARIES MAY NOT BE FULLY LOADED WHEN FUSE IS INSTALLED.

THE MAXIMUM CURRENT CITED IS THE DC CURRENT DRAWN FROM THE RECTIFIER.

Logic Supply Regulator Card A301 Typical Voltages
(See Note 9)

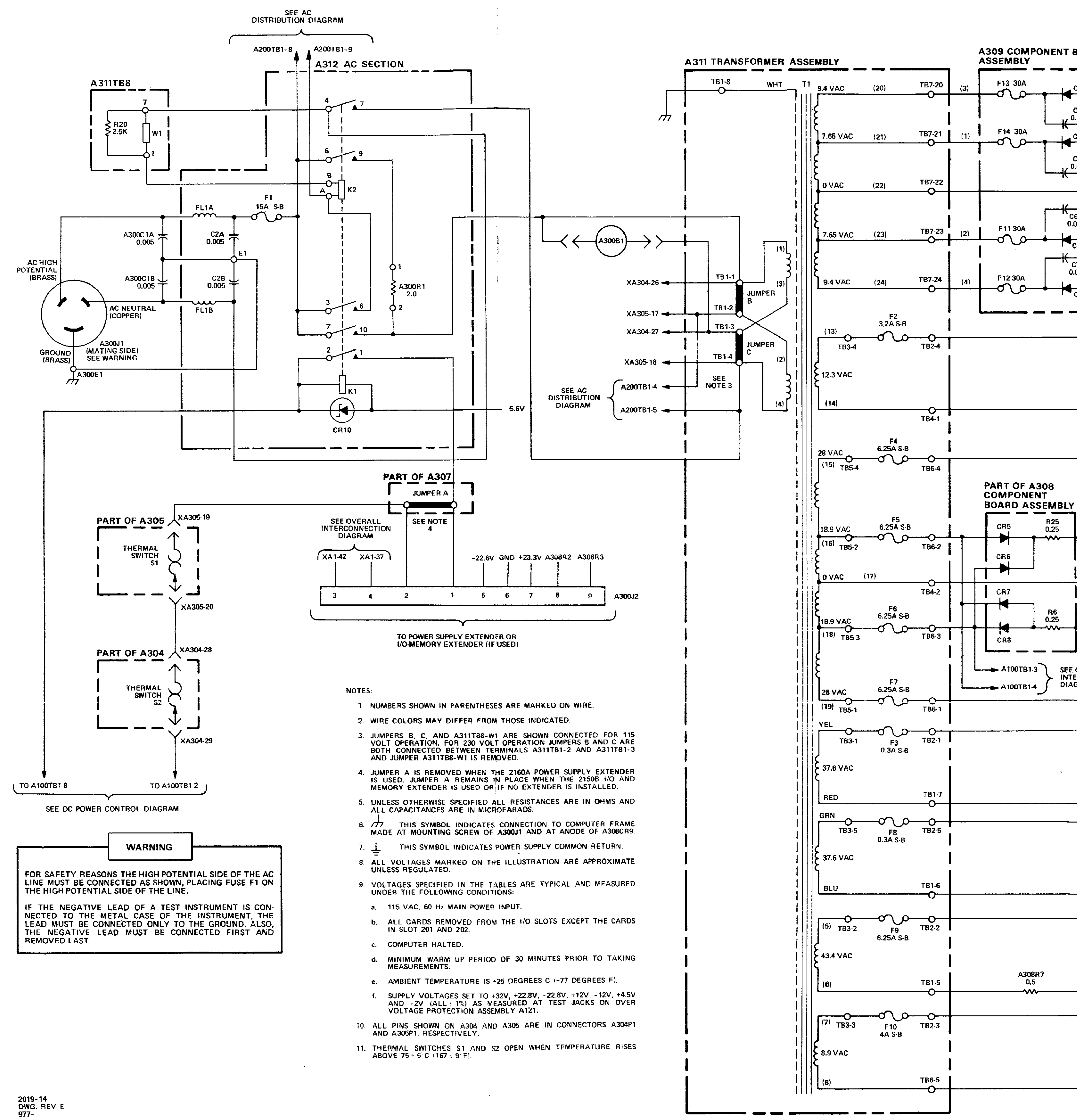
TEST POINT		DC VOLTAGE
Q30	Base	+ 4.5
Q31	Base	+ 4.5
Q32	Emitter	- 1.2
Q33	Base	+ 0.1
	Collector	- 2.3
Q35	Base	0.0
Q37	Emitter	- 3.3
Q38	Base	- 1.9
	Collector	- 4.4
Q39	Base	+ 0.7
Q41	Emitter	+12.7
Q42	Base	+11.3
	Collector	+14.0

Memory Supply Regulator Card A302 Typical Voltages
(See Note 9)

TEST POINT		DC VOLTAGE
Q50	Emitter	- 8.3
	Base	- 9.0
	Collector	-14.0
Q51	Emitter	- 8.3
	Base	- 9.0
Q52	Emitter	-13.1
Q53	Base	-11.5
Q54A	Emitter	- 0.7
	Base	0.0
	Collector	+24.5
Q55	Emitter	+23.5
Q56	Base	+21.7
Q57	Emitter	+ 0.7
	Base	0.0
	Collector	-25.2
Q58	Emitter	+ 0.7
Q59	Emitter	-24.4
Q60	Base	-21.4
Q61A	Emitter	- 0.7
	Base	0.0
	Collector	+34.0
Q63	Emitter	+32.6
Q64	Base	+30.6
A302-1 (+22V temp sense)		- 7.9
A302-13 (+32V temp sense)		- 7.9

Capacitor Board Assembly A303 Typical Voltages
(See Note 9)

TEST POINT	MEMORY 8K	MEMORY 16K
A303C14(-)	- 3.9V	- 3.4V
A303C17(-)	- 6.0V	- 5.6V
A303C19(-)	-12.9V	-12.4V
A303C20(+)	+36.9V	+35.5V
A303C21(+)	+22.4V	+23.3V
A303C22(-)	-23.8V	-22.6V
A303C23(-)	-37.2V	-36.4V
A303C26(+)	+58.0V	+56.4V
A303E8	-86.9V	-84.5V
A303E12	+107V	+105V



WARNING

FOR SAFETY REASONS THE HIGH POTENTIAL SIDE OF THE AC LINE MUST BE CONNECTED AS SHOWN, PLACING FUSE F1 ON THE HIGH POTENTIAL SIDE OF THE LINE.

IF THE NEGATIVE LEAD OF A TEST INSTRUMENT IS CONNECTED TO THE METAL CASE OF THE INSTRUMENT, THE LEAD MUST BE CONNECTED ONLY TO THE GROUND. ALSO, THE NEGATIVE LEAD MUST BE CONNECTED FIRST AND REMOVED LAST.

NOTES:

1. NUMBERS SHOWN IN PARENTHESES ARE MARKED ON WIRE.
2. WIRE COLORS MAY DIFFER FROM THOSE INDICATED.
3. JUMPERS B, C, AND A311TB8-W1 ARE SHOWN CONNECTED FOR 115 VOLT OPERATION. FOR 230 VOLT OPERATION JUMPERS B AND C ARE BOTH CONNECTED BETWEEN TERMINALS A311TB1-2 AND A311TB1-3 AND JUMPER A311TB8-W1 IS REMOVED.
4. JUMPER A IS REMOVED WHEN THE 2160A POWER SUPPLY EXTENDER IS USED. JUMPER A REMAINS IN PLACE WHEN THE 2150B I/O AND MEMORY EXTENDER IS USED OR IF NO EXTENDER IS INSTALLED.
5. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
6. THIS SYMBOL INDICATES CONNECTION TO COMPUTER FRAME MADE AT MOUNTING SCREW OF A300J1 AND AT ANODE OF A308CR9.
7. THIS SYMBOL INDICATES POWER SUPPLY COMMON RETURN.
8. ALL VOLTAGES MARKED ON THE ILLUSTRATION ARE APPROXIMATE UNLESS REGULATED.
9. VOLTAGES SPECIFIED IN THE TABLES ARE TYPICAL AND MEASURED UNDER THE FOLLOWING CONDITIONS:
   a. 115 VAC, 60 Hz MAIN POWER INPUT.
   b. ALL CARDS REMOVED FROM THE I/O SLOTS EXCEPT THE CARDS IN SLOT 201 AND 202.
   c. COMPUTER HALTED.
   d. MINIMUM WARM UP PERIOD OF 30 MINUTES PRIOR TO TAKING MEASUREMENTS.
   e. AMBIENT TEMPERATURE IS +25 DEGREES C (+77 DEGREES F).
   f. SUPPLY VOLTAGES SET TO +32V, +22.8V, -22.8V, +12V, -12V, +4.5V AND -2V (ALL ± 1%) AS MEASURED AT TEST JACKS ON OVER VOLTAGE PROTECTION ASSEMBLY A121.
10. ALL PINS SHOWN ON A304 AND A305 ARE IN CONNECTORS A304P1 AND A305P1, RESPECTIVELY.
11. THERMAL SWITCHES S1 AND S2 OPEN WHEN TEMPERATURE RISES ABOVE 75 ± 5°C (167 ± 9°F).

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ons, Transformer A311T1

AGE (RMS)		MAXIMUM CURRENT (AMPS, DC)	WINDING RESISTANCE (OHMS)
D	LOADED		
	115.0	– –	0.130 ± 10%
	115.0	– –	0.150 ± 10%
	41.8	3.0	0.125 ± 10%
	8.5	4.0	0.032 ± 10%
	36.0	0.1	1.448 ± 10%
	36.0	0.1	1.443 ± 10%
	12.0	2.0	0.042 ± 10%
	53.5	4.0	0.128 ± 10%
	35.5	12.0	0.093 ± 10%
	17.8	22.5	0.018 ± 10%
	14.2	22.5	0.010 ± 10%

NDINGS, THE UNLOADED VOLTAGE IS
OLTAGE (FUSE REMOVED). THE LOADED
FULLY LOADED SECONDARY (MAXIMUM
FROM THE RECTIFIER). DEPENDING ON
ES INSTALLED, SECONDARIES MAY NOT
HEN FUSE IS INSTALLED.

ENT CITED IS THE DC CURRENT DRAWN
.

ulator Card A301 Typical Voltages
(See Note 9)

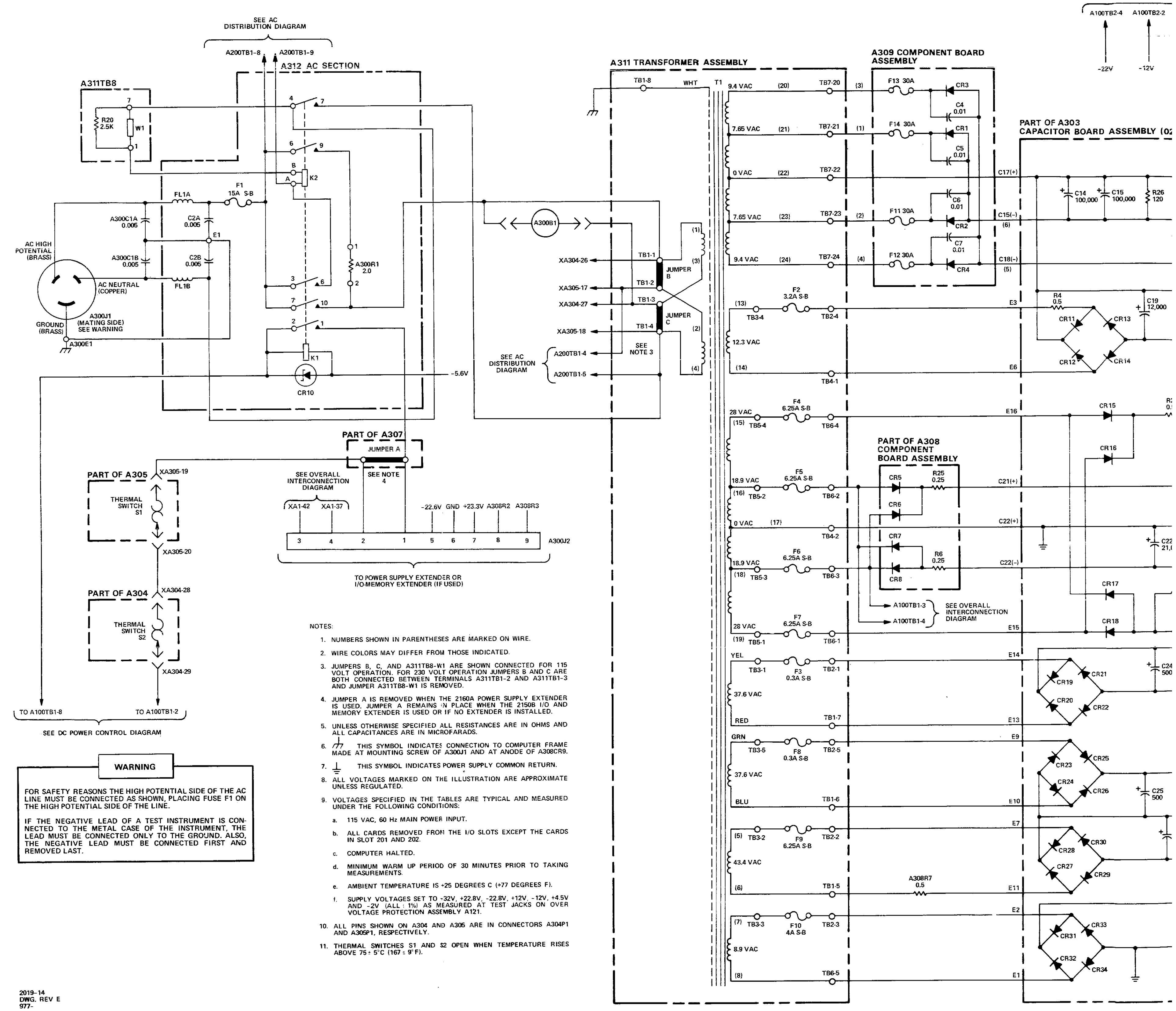
NT	DC VOLTAGE
Base	+ 4.5
Base	+ 4.5
Emitter	- 1.2
Base	+ 0.1
Collector	- 2.3
Base	0.0
Emitter	- 3.3
Base	- 1.9
Collector	- 4.4
Base	+ 0.7
Emitter	+12.7
Base	+11.3
Collector	+14.0

Memory Supply Regulator Card A302 Typical Voltages
(See Note 9)

TEST POINT		DC VOLTAGE
Q50	Emitter	- 8.3
	Base	- 9.0
	Collector	-14.0
Q51	Emitter	- 8.3
	Base	- 9.0
Q52	Emitter	-13.1
Q53	Base	-11.5
Q54A	Emitter	- 0.7
	Base	0.0
	Collector	+24.5
Q55	Emitter	+23.5
Q56	Base	+21.7
Q57	Emitter	+ 0.7
	Base	0.0
	Collector	-25.2
Q58	Emitter	+ 0.7
Q59	Emitter	-24.4
Q60	Base	-21.4
Q61A	Emitter	- 0.7
	Base	0.0
	Collector	+34.0
Q63	Emitter	+32.6
Q64	Base	+30.6
A302-1 (+22V temp sense)		- 7.9
A302-13 (+32V temp sense)		- 7.9

Capacitor Board Assembly A303 Typical Voltages
(See Note 9)

TEST POINT	MEMORY	
	8K	16K
A303C14(-)	- 3.9V	- 3.4V
A303C17(-)	- 6.0V	- 5.6V
A303C19(-)	-12.9V	-12.4V
A303C20(+)	+36.9V	+35.5V
A303C21(+)	+22.4V	+23.3V
A303C22(-)	-23.8V	-22.6V
A303C23(-)	-37.2V	-36.4V
A303C26(+)	+58.0V	+56.4V
A303E8	-86.9V	-84.5V
A303E12	+107V	+105V



SEE DC POWER CONTROL DIAGRAM

WARNING

FOR SAFETY REASONS THE HIGH POTENTIAL SIDE OF THE AC LINE MUST BE CONNECTED AS SHOWN, PLACING FUSE F1 ON THE HIGH POTENTIAL SIDE OF THE LINE.

IF THE NEGATIVE LEAD OF A TEST INSTRUMENT IS CONNECTED TO THE METAL CASE OF THE INSTRUMENT, THE LEAD MUST BE CONNECTED ONLY TO THE GROUND. ALSO, THE NEGATIVE LEAD MUST BE CONNECTED FIRST AND REMOVED LAST.

NOTES:

1. NUMBERS SHOWN IN PARENTHESES ARE MARKED ON WIRE.
2. WIRE COLORS MAY DIFFER FROM THOSE INDICATED.
3. JUMPERS B, C, AND A311TB8-W1 ARE SHOWN CONNECTED FOR 115 VOLT OPERATION. FOR 230 VOLT OPERATION JUMPERS B AND C ARE BOTH CONNECTED BETWEEN TERMINALS A311TB1-2 AND A311TB1-3 AND JUMPER A311TB8-W1 IS REMOVED.
4. JUMPER A IS REMOVED WHEN THE 2160A POWER SUPPLY EXTENDER IS USED. JUMPER A REMAINS IN PLACE WHEN THE 2150B I/O AND MEMORY EXTENDER IS USED OR IF NO EXTENDER IS INSTALLED.
5. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
6. THIS SYMBOL INDICATES CONNECTION TO COMPUTER FRAME MADE AT MOUNTING SCREW OF A300J1 AND AT ANODE OF A308CR9.
7. THIS SYMBOL INDICATES POWER SUPPLY COMMON RETURN.
8. ALL VOLTAGES MARKED ON THE ILLUSTRATION ARE APPROXIMATE UNLESS REGULATED.
9. VOLTAGES SPECIFIED IN THE TABLES ARE TYPICAL AND MEASURED UNDER THE FOLLOWING CONDITIONS:
   a. 115 VAC, 60 Hz MAIN POWER INPUT.
   b. ALL CARDS REMOVED FROM THE I/O SLOTS EXCEPT THE CARDS IN SLOT 201 AND 202.
   c. COMPUTER HALTED.
   d. MINIMUM WARM UP PERIOD OF 30 MINUTES PRIOR TO TAKING MEASUREMENTS.
   e. AMBIENT TEMPERATURE IS +25 DEGREES C (+77 DEGREES F).
   f. SUPPLY VOLTAGES SET TO +32V, +22.8V, -22.8V, +12V, -12V, +4.5V AND -2V (ALL ± 1%) AS MEASURED AT TEST JACKS ON OVER VOLTAGE PROTECTION ASSEMBLY A121.
10. ALL PINS SHOWN ON A304 AND A305 ARE IN CONNECTORS A304P1 AND A305P1, RESPECTIVELY.
11. THERMAL SWITCHES S1 AND S2 OPEN WHEN TEMPERATURE RISES ABOVE 75 ± 5°C (167 ± 9°F).

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DWG. REV E
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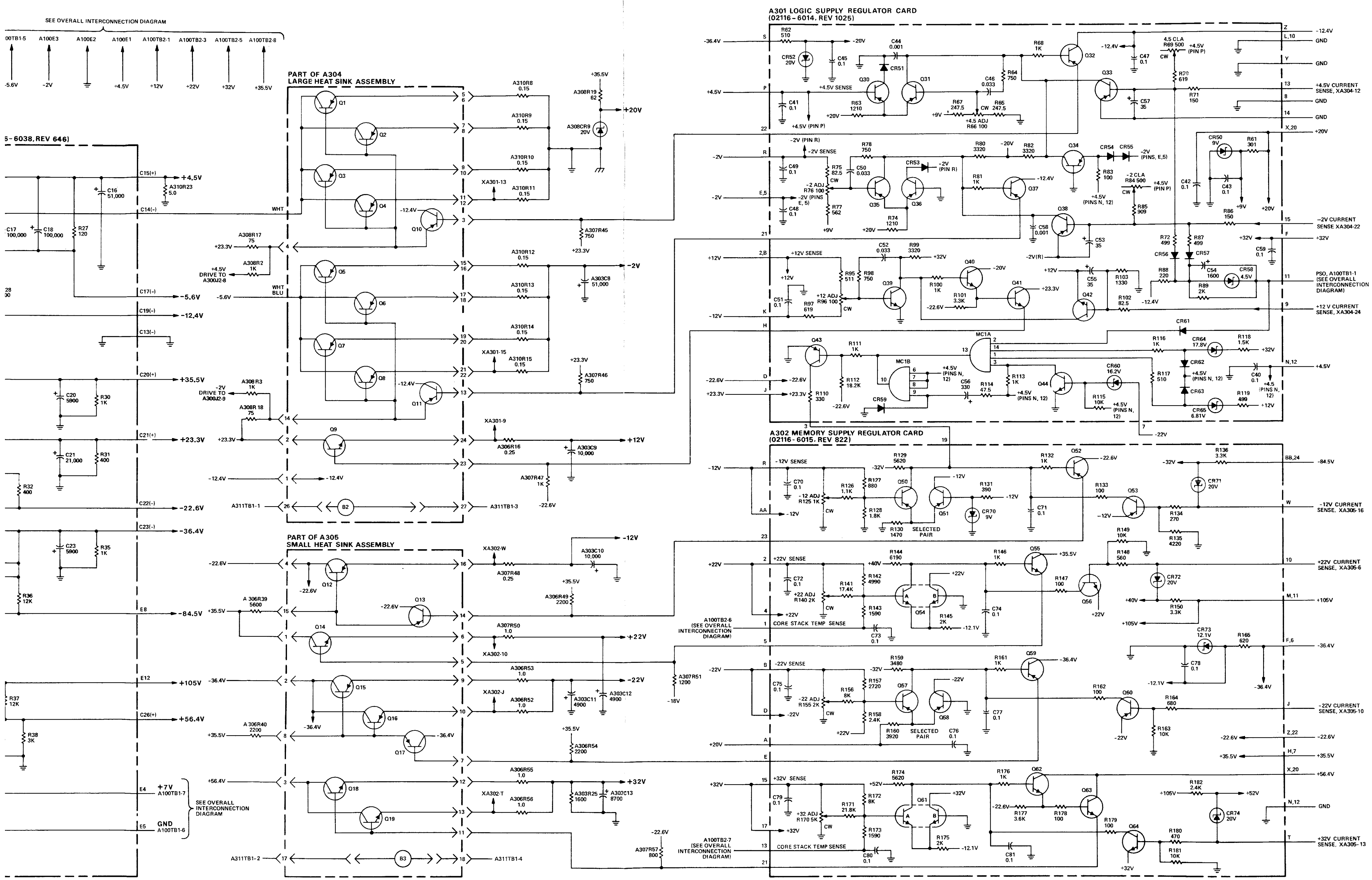


Figure 5-44B. A300 Power Supply Assembly (02116-6124), Schematic Diagram for Computers with Serial Number Prefix 977-

Specifications, Transformer A311T1

XFMR WIRES	AC VOLTAGE (RMS) UNLOADED	AC VOLTAGE (RMS) LOADED	MAXIMUM CURRENT (AMPS, DC)	WINDING RESISTANCE (OHMS)
1-3	115.0	115.0	– –	0.130 ± 10%
2-4	115.0	115.0	– –	0.150 ± 10%
5-6	43.4	41.8	3.0	0.125 ± 10%
7-8	8.9	8.5	4.0	0.032 ± 10%
9-10 (yellow-red)	37.6	36.0	0.1	1.448 ± 10%
11-12 (green-blue)	37.6	36.0	0.1	1.443 ± 10%
13-14	12.3	12.0	2.0	0.042 ± 10%
15-19	56.0	53.5	4.0	0.128 ± 10%
16-18	37.8	35.5	12.0	0.093 ± 10%
20-24	18.8	17.8	22.5	0.018 ± 10%
21-23	15.3	14.2	22.5	0.010 ± 10%

NOTES:

FOR SECONDARY WINDINGS, THE UNLOADED VOLTAGE IS THE OPEN-CIRCUIT VOLTAGE (FUSE REMOVED). THE LOADED VOLTAGE IS FOR A FULLY LOADED SECONDARY (MAXIMUM DC CURRENT DRAWN FROM THE RECTIFIER). DEPENDING ON THE OPTIONAL DEVICES INSTALLED, SECONDARIES MAY NOT BE FULLY LOADED WHEN FUSE IS INSTALLED.

THE MAXIMUM CURRENT CITED IS THE DC CURRENT DRAWN FROM THE RECTIFIER.

Logic Supply Regulator Card A301 Typical Voltages
(See Note 9)

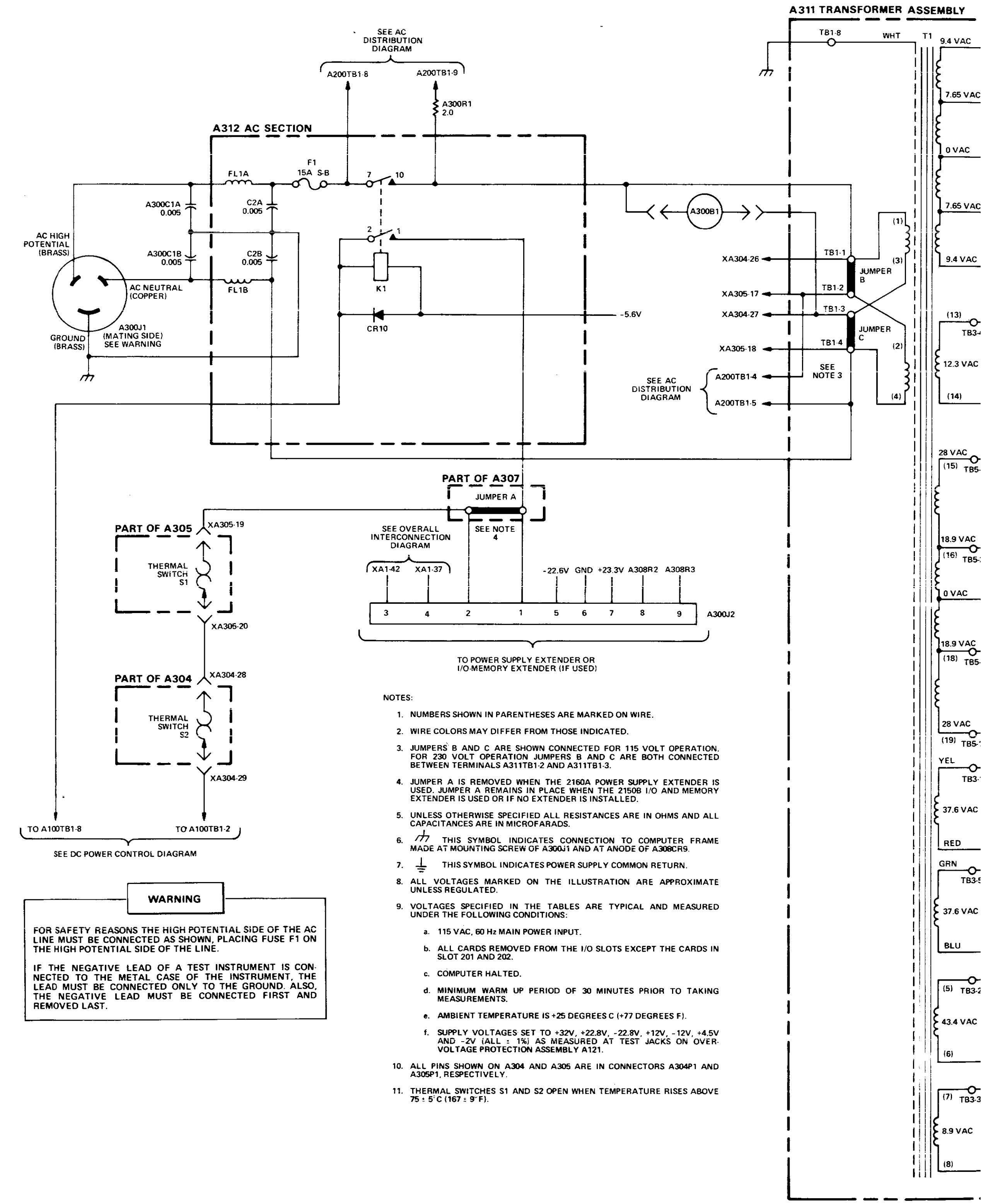
TEST POINT		DC VOLTAGE
Q30	Base	+ 4.5
Q31	Base	+ 4.5
Q32	Emitter	- 1.2
Q33	Base	+ 0.1
	Collector	- 2.3
Q35	Base	0.0
Q37	Emitter	- 3.3
Q38	Base	- 1.9
	Collector	- 4.4
Q39	Base	+ 0.7
Q41	Emitter	+12.7
Q42	Base	+11.3
	Collector	+14.0

Memory Supply Regulator Card A302 Typical Voltages
(See Note 9)

TEST POINT		DC VOLTAGE
Q50	Emitter	- 8.3
	Base	- 9.0
	Collector	-14.0
Q51	Emitter	- 8.3
	Base	- 9.0
Q52	Emitter	-13.1
Q53	Base	-11.5
Q54A	Emitter	- 0.7
	Base	0.0
	Collector	+24.5
Q55	Emitter	+23.5
Q56	Base	+21.7
Q57	Emitter	+ 0.7
	Base	0.0
	Collector	-25.2
Q58	Emitter	+ 0.7
Q59	Emitter	-24.4
Q60	Base	-21.4
Q61A	Emitter	- 0.7
	Base	0.0
	Collector	+34.0
Q63	Emitter	+32.6
Q64	Base	+30.6
A302-1 (+22V temp sense)		- 7.9
A302-13 (+32V temp sense)		- 7.9

Capacitor Board Assembly A303 Typical Voltages
(See Note 9)

TEST POINT	MEMORY 8K	MEMORY 16K
A303C14(-)	- 3.9V	- 3.4V
A303C17(-)	- 6.0V	- 5.6V
A303C19(-)	-12.9V	-12.4V
A303C20(+)	+36.9V	+35.5V
A303C21(+)	+22.4V	+23.3V
A303C22(-)	-23.8V	-22.6V
A303C23(-)	-37.2V	-36.4V
A303C26(+)	+58.0V	+56.4V
A303E8	-86.9V	-84.5V
A303E12	+107V	+105V



WARNING

FOR SAFETY REASONS THE HIGH POTENTIAL SIDE OF THE AC LINE MUST BE CONNECTED AS SHOWN, PLACING FUSE F1 ON THE HIGH POTENTIAL SIDE OF THE LINE.

IF THE NEGATIVE LEAD OF A TEST INSTRUMENT IS CONNECTED TO THE METAL CASE OF THE INSTRUMENT, THE LEAD MUST BE CONNECTED ONLY TO THE GROUND. ALSO, THE NEGATIVE LEAD MUST BE CONNECTED FIRST AND REMOVED LAST.

NOTES:

1. NUMBERS SHOWN IN PARENTHESES ARE MARKED ON WIRE.
2. WIRE COLORS MAY DIFFER FROM THOSE INDICATED.
3. JUMPERS B AND C ARE SHOWN CONNECTED FOR 115 VOLT OPERATION. FOR 230 VOLT OPERATION JUMPERS B AND C ARE BOTH CONNECTED BETWEEN TERMINALS A311TB1-2 AND A311TB1-3.
4. JUMPER A IS REMOVED WHEN THE 2160A POWER SUPPLY EXTENDER IS USED. JUMPER A REMAINS IN PLACE WHEN THE 2150B I/O AND MEMORY EXTENDER IS USED OR IF NO EXTENDER IS INSTALLED.
5. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
6. THIS SYMBOL INDICATES CONNECTION TO COMPUTER FRAME MADE AT MOUNTING SCREW OF A300J1 AND AT ANODE OF A308CR9.
7. THIS SYMBOL INDICATES POWER SUPPLY COMMON RETURN.
8. ALL VOLTAGES MARKED ON THE ILLUSTRATION ARE APPROXIMATE UNLESS REGULATED.
9. VOLTAGES SPECIFIED IN THE TABLES ARE TYPICAL AND MEASURED UNDER THE FOLLOWING CONDITIONS:
   a. 115 VAC, 60 Hz MAIN POWER INPUT.
   b. ALL CARDS REMOVED FROM THE I/O SLOTS EXCEPT THE CARDS IN SLOT 201 AND 202.
   c. COMPUTER HALTED.
   d. MINIMUM WARM UP PERIOD OF 30 MINUTES PRIOR TO TAKING MEASUREMENTS.
   e. AMBIENT TEMPERATURE IS +25 DEGREES C (+77 DEGREES F).
   f. SUPPLY VOLTAGES SET TO +32V, +22.8V, -22.8V, +12V, -12V, +4.5V AND -2V (ALL ± 1%) AS MEASURED AT TEST JACKS ON OVER-VOLTAGE PROTECTION ASSEMBLY A121.
10. ALL PINS SHOWN ON A304 AND A305 ARE IN CONNECTORS A304P1 AND A305P1, RESPECTIVELY.
11. THERMAL SWITCHES S1 AND S2 OPEN WHEN TEMPERATURE RISES ABOVE 75 ± 5°C (167 ± 9°F).

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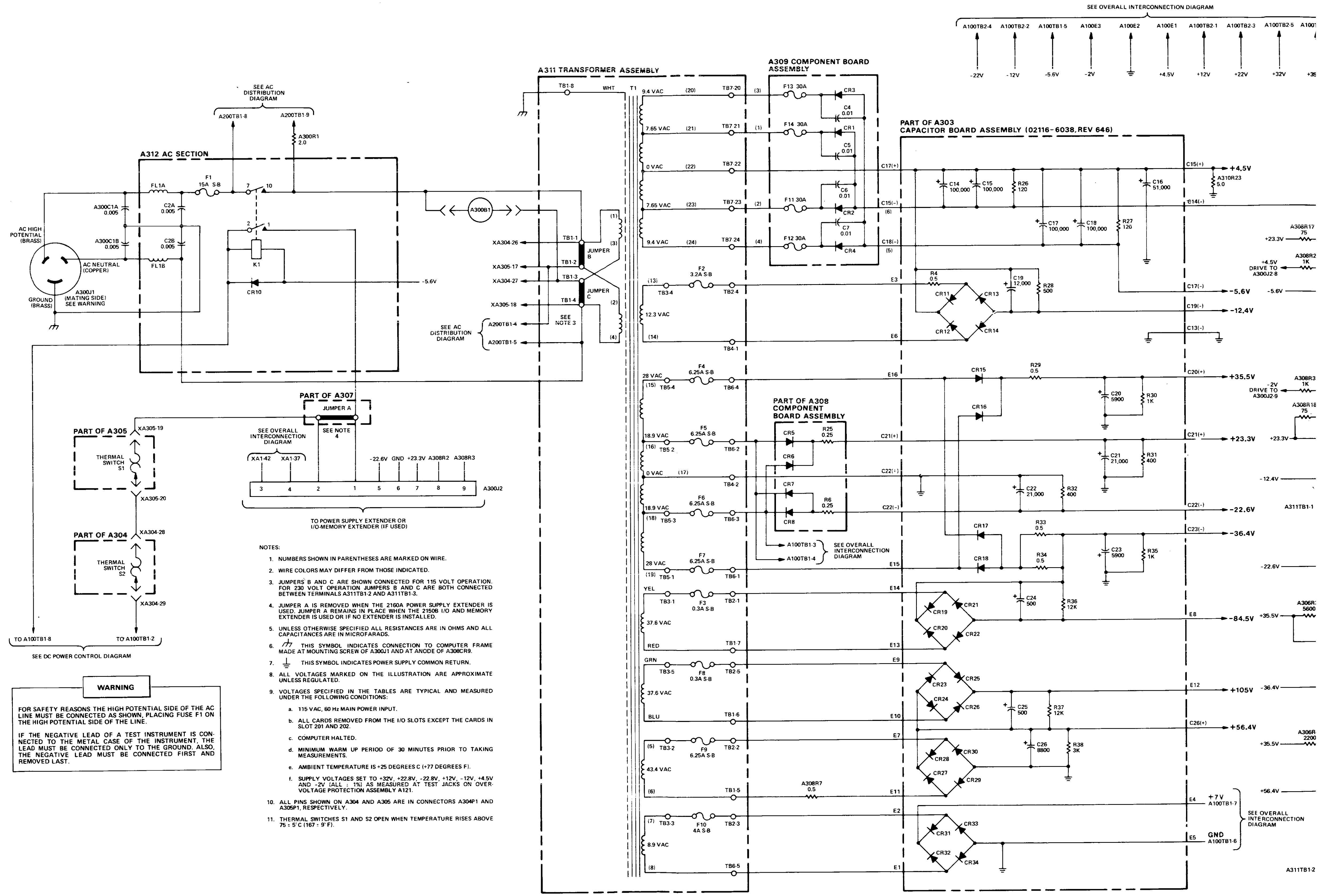
Memory Supply Regulator Card A302 Typical Voltages
(See Note 9)

TEST POINT		DC VOLTAGE
Q50	Emitter	- 8.3
	Base	- 9.0
	Collector	-14.0
Q51	Emitter	- 8.3
	Base	- 9.0
Q52	Emitter	-13.1
Q53	Base	-11.5
Q54A	Emitter	- 0.7
	Base	0.0
	Collector	+24.5
Q55	Emitter	+23.5
Q56	Base	+21.7
Q57	Emitter	+ 0.7
	Base	0.0
	Collector	-25.2
Q58	Emitter	+ 0.7
Q59	Emitter	-24.4
Q60	Base	-21.4
Q61A	Emitter	- 0.7
	Base	0.0
	Collector	+34.0
Q63	Emitter	+32.6
Q64	Base	+30.6
A302-1 (+22V temp sense)		- 7.9
A302-13 (+32V temp sense)		- 7.9

Capacitor Board Assembly A303 Typical Voltages
(See Note 9)

TEST POINT	MEMORY 8K	MEMORY 16K
A303C14(-)	- 3.9V	- 3.4V
A303C17(-)	- 6.0V	- 5.6V
A303C19(-)	-12.9V	-12.4V
A303C20(+)	+36.9V	+35.5V
A303C21(+)	+22.4V	+23.3V
A303C22(-)	-23.8V	-22.6V
A303C23(-)	-37.2V	-36.4V
A303C26(+)	+58.0V	+56.4V
A303E8	-86.9V	-84.5V
A303E12	+107V	+105V



NOTES:

1. NUMBERS SHOWN IN PARENTHESES ARE MARKED ON WIRE.
2. WIRE COLORS MAY DIFFER FROM THOSE INDICATED.
3. JUMPERS B AND C ARE SHOWN CONNECTED FOR 115 VOLT OPERATION. FOR 230 VOLT OPERATION JUMPERS B AND C ARE BOTH CONNECTED BETWEEN TERMINALS A311TB1-2 AND A311TB1-3.
4. JUMPER A IS REMOVED WHEN THE 2160A POWER SUPPLY EXTENDER IS USED. JUMPER A REMAINS IN PLACE WHEN THE 2150B I/O AND MEMORY EXTENDER IS USED OR IF NO EXTENDER IS INSTALLED.
5. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
6. THIS SYMBOL INDICATES CONNECTION TO COMPUTER FRAME MADE AT MOUNTING SCREW OF A300J1 AND AT ANODE OF A308CR9.
7. THIS SYMBOL INDICATES POWER SUPPLY COMMON RETURN.
8. ALL VOLTAGES MARKED ON THE ILLUSTRATION ARE APPROXIMATE UNLESS REGULATED.
9. VOLTAGES SPECIFIED IN THE TABLES ARE TYPICAL AND MEASURED UNDER THE FOLLOWING CONDITIONS:
   a. 115 VAC, 60 Hz MAIN POWER INPUT.
   b. ALL CARDS REMOVED FROM THE I/O SLOTS EXCEPT THE CARDS IN SLOT 201 AND 202.
   c. COMPUTER HALTED.
   d. MINIMUM WARM UP PERIOD OF 30 MINUTES PRIOR TO TAKING MEASUREMENTS.
   e. AMBIENT TEMPERATURE IS +25 DEGREES C (+77 DEGREES F).
   f. SUPPLY VOLTAGES SET TO +32V, +22.8V, -22.8V, +12V, -12V, +4.5V AND -2V (ALL ± 1%) AS MEASURED AT TEST JACKS ON OVER-VOLTAGE PROTECTION ASSEMBLY A121.
10. ALL PINS SHOWN ON A304 AND A305 ARE IN CONNECTORS A304P1 AND A305P1, RESPECTIVELY.
11. THERMAL SWITCHES S1 AND S2 OPEN WHEN TEMPERATURE RISES ABOVE 75 ± 5°C (167 ± 9°F).

WARNING

FOR SAFETY REASONS THE HIGH POTENTIAL SIDE OF THE AC LINE MUST BE CONNECTED AS SHOWN, PLACING FUSE F1 ON THE HIGH POTENTIAL SIDE OF THE LINE.

IF THE NEGATIVE LEAD OF A TEST INSTRUMENT IS CONNECTED TO THE METAL CASE OF THE INSTRUMENT, THE LEAD MUST BE CONNECTED ONLY TO THE GROUND. ALSO, THE NEGATIVE LEAD MUST BE CONNECTED FIRST AND REMOVED LAST.

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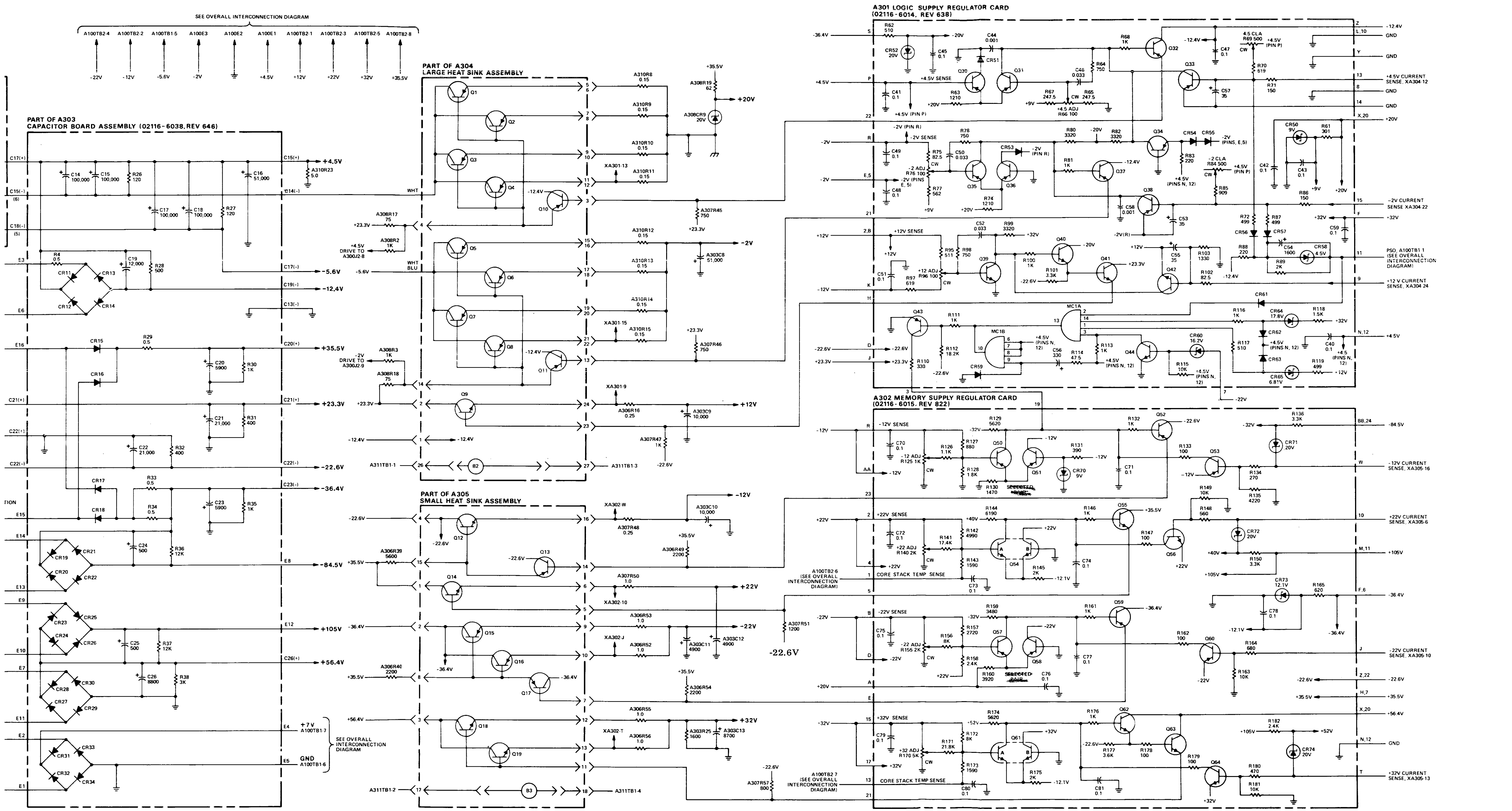

Figure 5-44. A300 Power Supply Assembly (02116-6124), Schematic Diagram

Table 5-35. A402 Temperature Sensing Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
A402R220, A402R221 A402R221	0811-2031	Resistor, Fxd, WW, 815 ohms, 3.0%, 1/4w	01686	7010

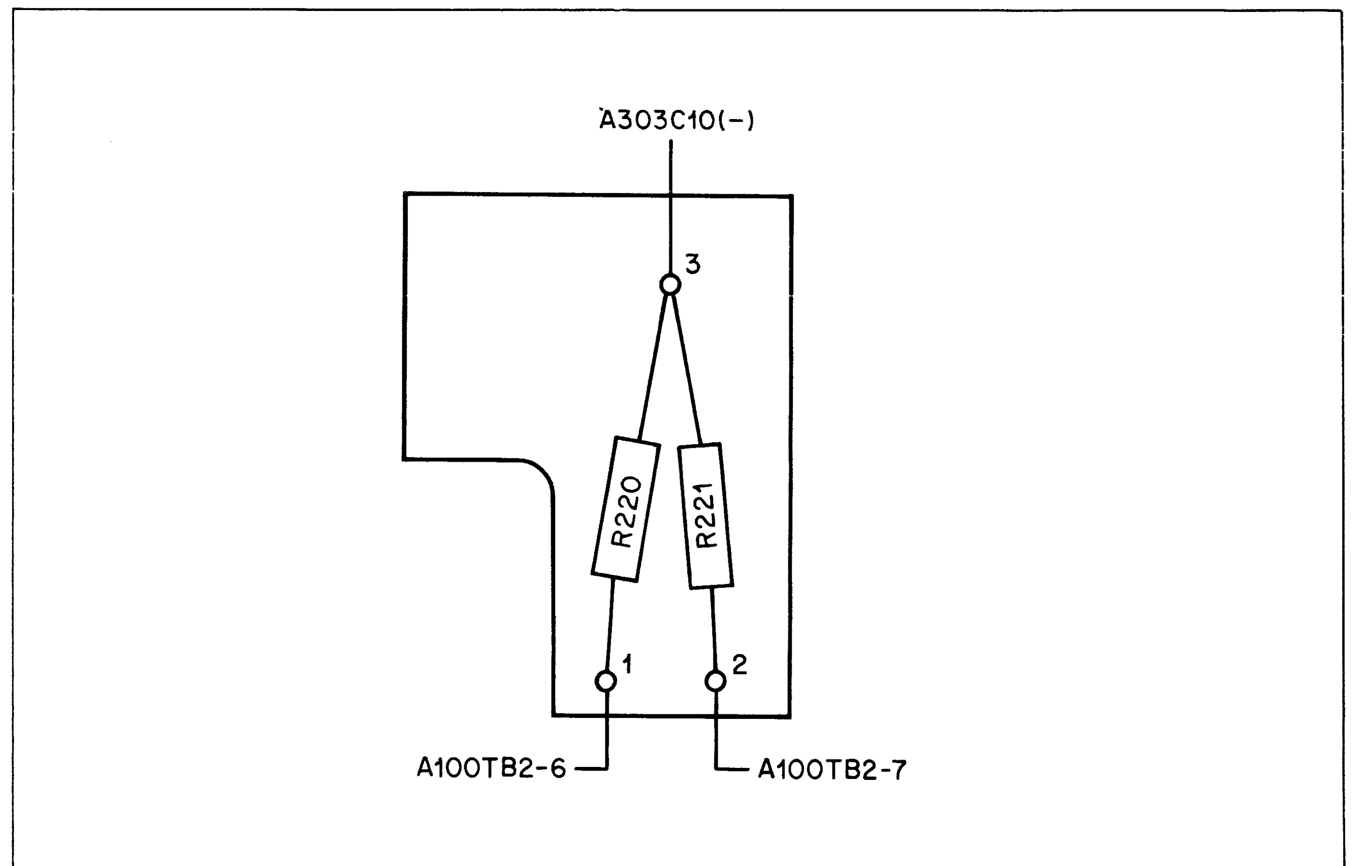

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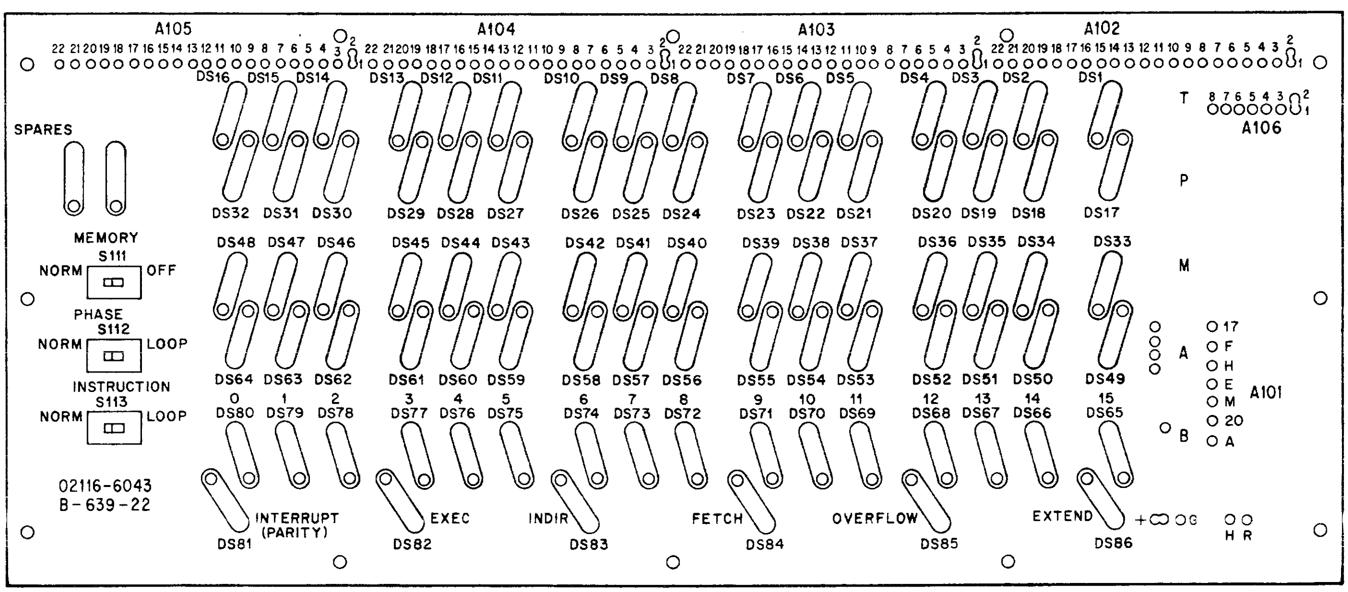
Figure 5-45. A402 Temperature Sensing Assembly, Parts Location and Connection Diagram

Table 5-36. A501 Display Board Assembly (02116-6043), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
DS1 thru DS86	2140-0035	Lamp, Incandescent, 6.3V, 0.75A	71744	1775
S111 thru S113	3101-0973	Switch, Slide, DPDT, 125V, 0.5A, AC/DC	79727	G126-0018



02116-6043-I

NOTES:

1. CONNECTIONS A101 THRU A106 ARE CABLE CONNECTIONS. REFER TO THE OVERALL INTERCONNECTION DIAGRAM AND TO THE DOOR ASSEMBLY SCHEMATIC DIAGRAM FOR FUTHER INFORMATION.

Figure 5-46. A501 Display Board Assembly (02116-6043), Parts Location Diagram

Table 5-37. A502 Control Panel Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
DS106 thru DS109	2140-0035	Lamp, Incandescent, 6.3V, 0.75A	71744	1775
S1 thru S16, S116	3101-1051	Switch, Toggle, SPST, 125V, 3A	88140	8908K507
S100 thru S108	3101-0715	Switch, Lighted Pushbutton	28480	3101-0715
S109	3101-0714	Switch, Lighted Pushbutton	28480	3101-0714

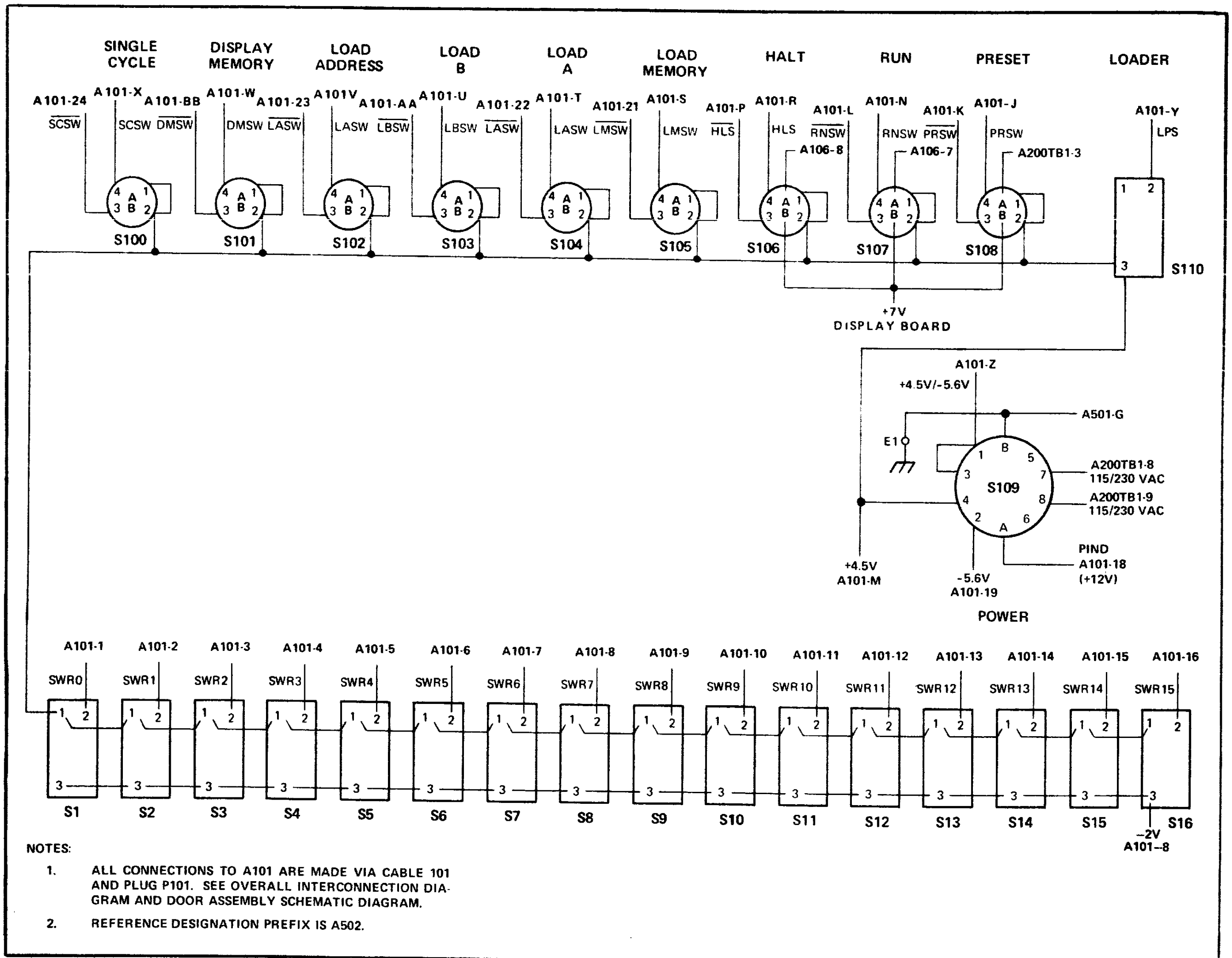


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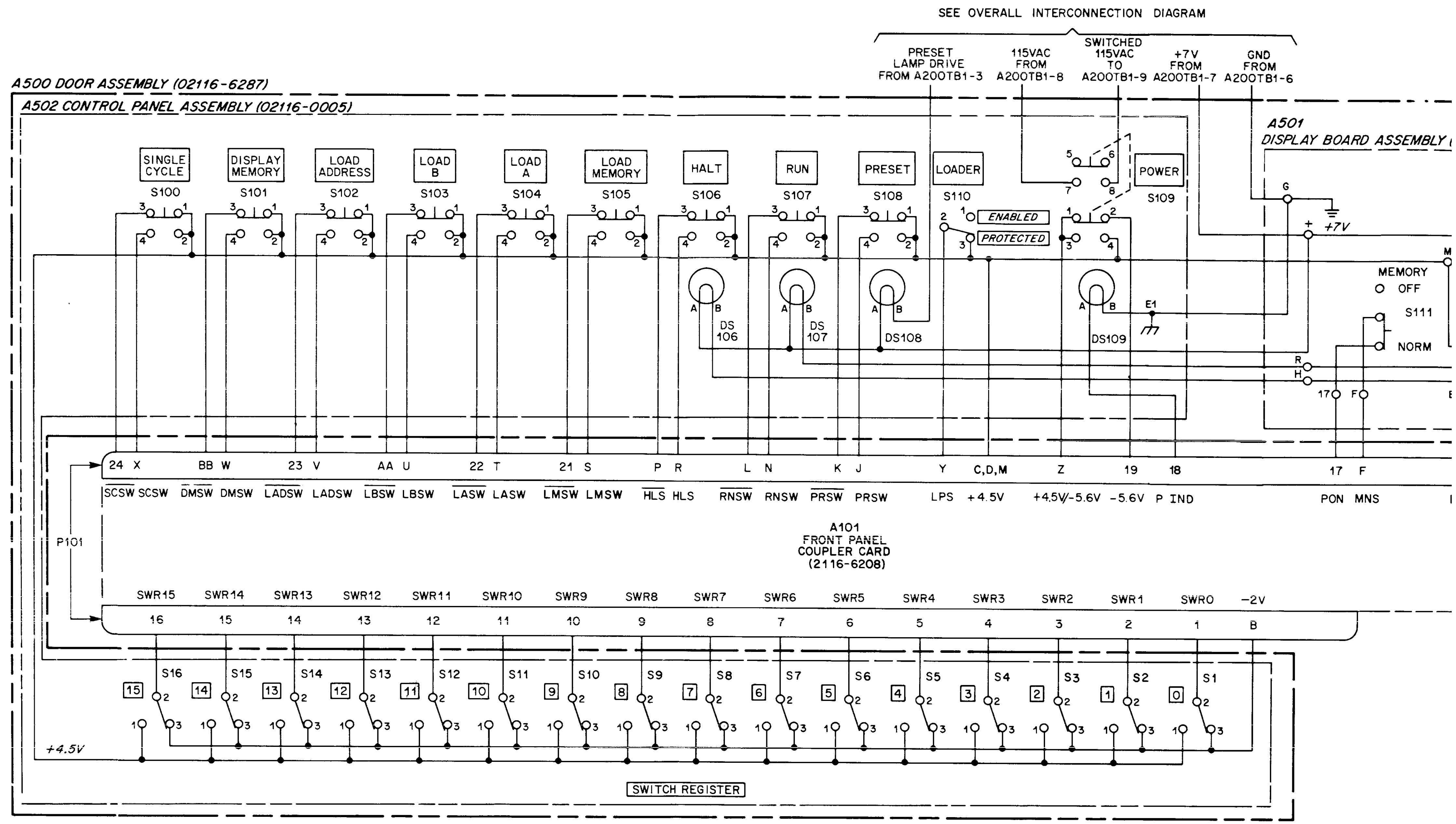
Figure 5-47. A502 Control Panel Assembly, Parts Location and Connection Diagram



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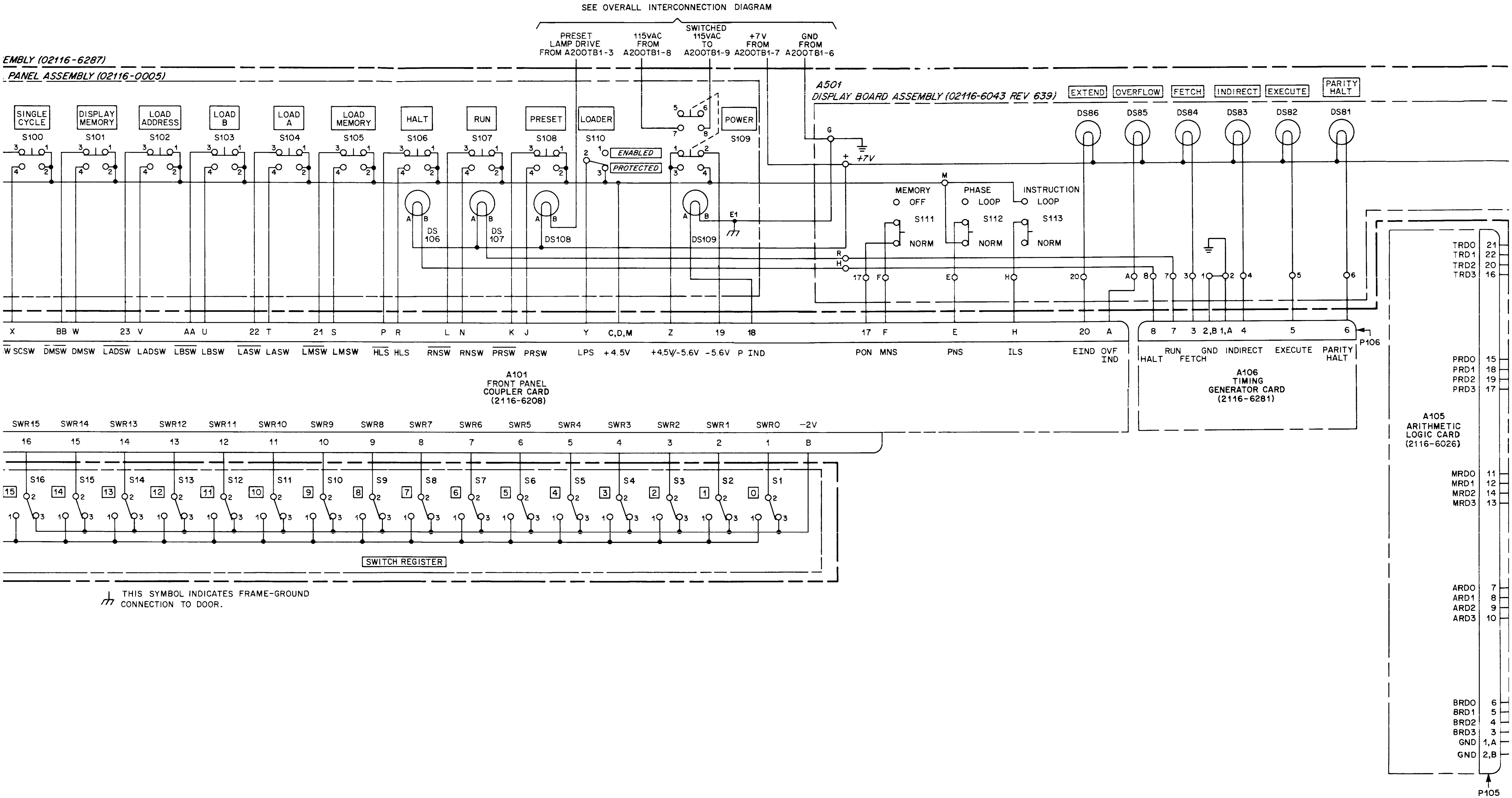
THIS SYMBOL INDICATES FRAME-GROUND CONNECTION TO DOOR.



SEE OVERALL INTERCONNECTION DIAGRAM
PRESET LAMP DRIVE FROM A200TB1-3
115VAC FROM A200TB1-8
SWITCHED 115VAC TO A200TB1-9
+7V FROM A200TB1-7
GND FROM A200TB1-6
EMBLY (02116-6287)
PANEL ASSEMBLY (02116-0005)
A501
DISPLAY BOARD ASSEMBLY (02116-6043 REV 639)
EXTEND
OVERFLOW
FETCH
INDIRECT
EXECUTE
PARITY HALT
DS86
DS85
DS84
DS83
DS82
DS81
SINGLE CYCLE
S100
DISPLAY MEMORY
S101
LOAD ADDRESS
S102
LOAD B
S103
LOAD A
S104
LOAD MEMORY
S105
HALT
S106
RUN
S107
PRESET
S108
LOADER
S110
ENABLED
PROTECTED
POWER
S109
DS 106
DS 107
DS108
DS109
E1
+7V
MEMORY
OFF
NORM
S111
PHASE
LOOP
NORM
S112
INSTRUCTION
LOOP
NORM
S113
X BB W 23 V AA U 22 T 21 S P R L N K J Y C,D,M Z 19 18 17 F E H 20 A
W SCSW DMSW DMSW LADSW LADSW LBSW LBSW LASW LASW LMSW LMSW HLS HLS RNSW RNSW PRSW PRSW LPS +4.5V +4.5V/-5.6V -5.6V P IND PON MNS PNS ILS EIND OVF IND
A101
FRONT PANEL COUPLER CARD
(2116-6208)
8 7 3 2,B 1,A 4 5 6
HALT RUN FETCH GND INDIRECT EXECUTE PARITY HALT
P106
A106
TIMING GENERATOR CARD
(2116-6281)
SWR15 SWR14 SWR13 SWR12 SWR11 SWR10 SWR9 SWR8 SWR7 SWR6 SWR5 SWR4 SWR3 SWR2 SWR1 SWR0 -2V
16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 B
S16 S15 S14 S13 S12 S11 S10 S9 S8 S7 S6 S5 S4 S3 S2 S1
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SWITCH REGISTER
THIS SYMBOL INDICATES FRAME-GROUND CONNECTION TO DOOR.
TRD0 21
TRD1 22
TRD2 20
TRD3 16
PRD0 15
PRD1 18
PRD2 19
PRD3 17
A105
ARITHMETIC LOGIC CARD
(2116-6026)
MRD0 11
MRD1 12
MRD2 14
MRD3 13
ARD0 7
ARD1 8
ARD2 9
ARD3 10
BRD0 6
BRD1 5
BRD2 4
BRD3 3
GND 1,A
GND 2,B
P105

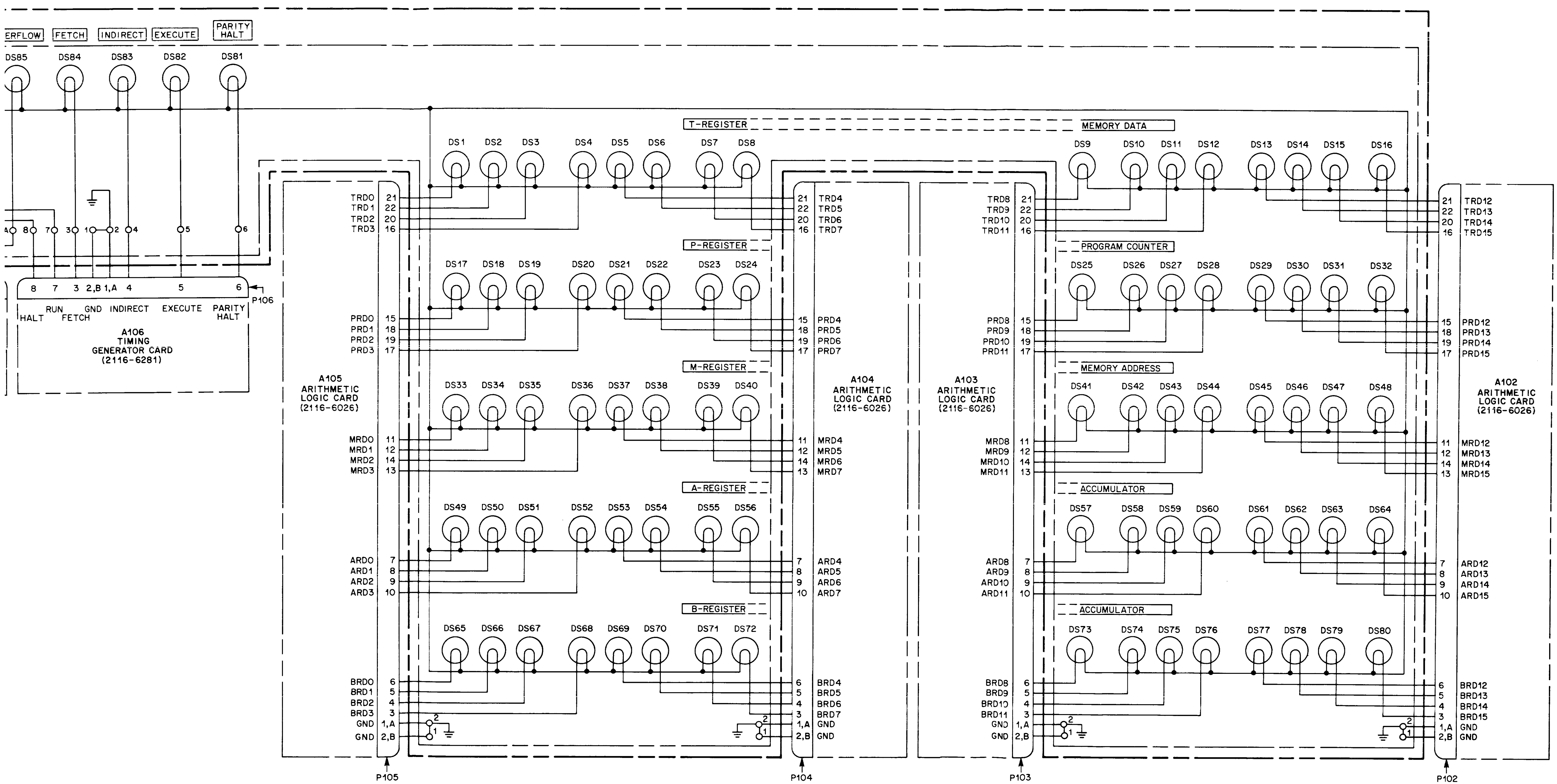
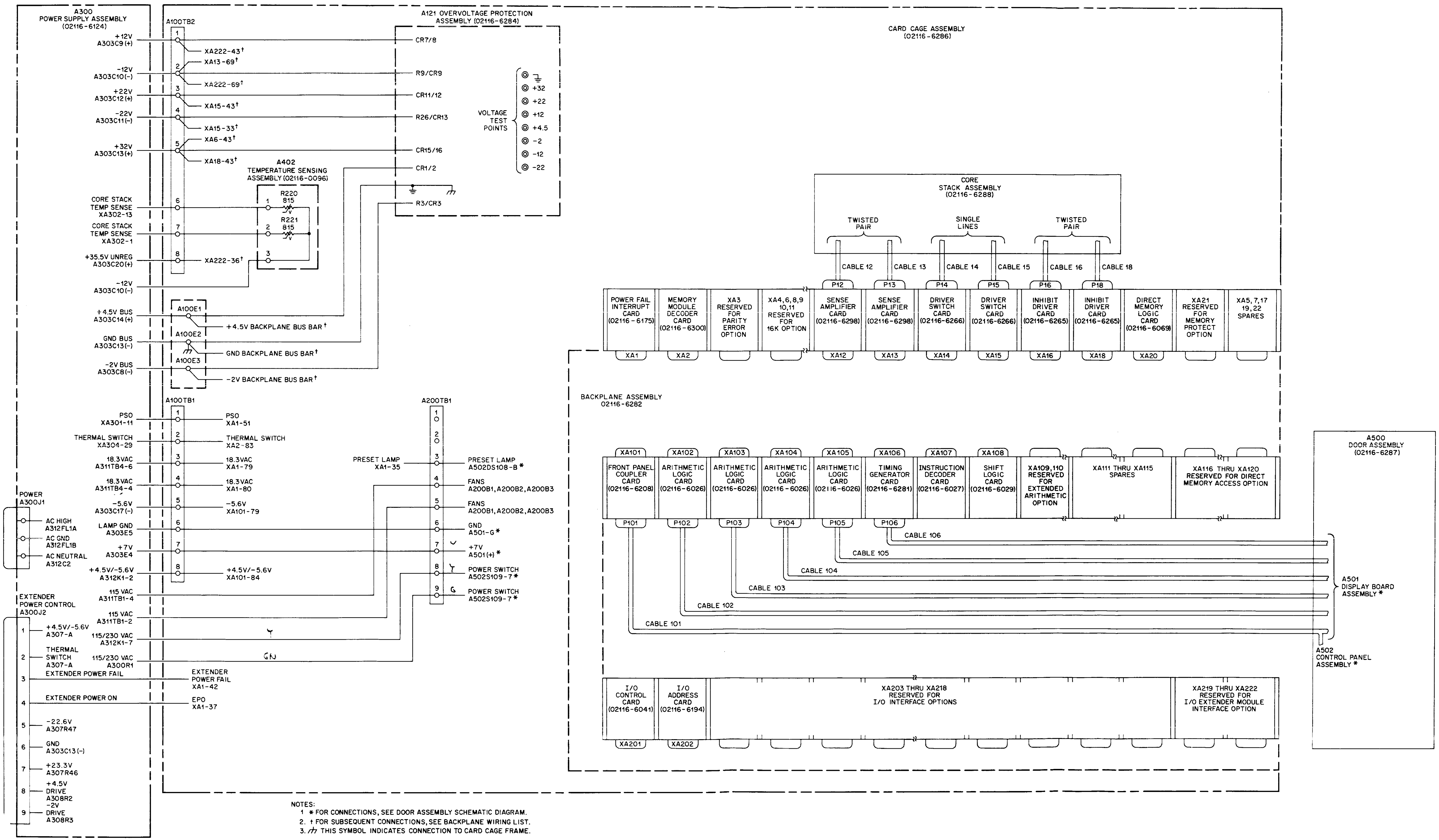


Figure 5-48. A500 Door Assembly (02116-6287), Schematic Diagram



NOTES:
1. * FOR CONNECTIONS, SEE DOOR ASSEMBLY SCHEMATIC DIAGRAM.
2. † FOR SUBSEQUENT CONNECTIONS, SEE BACKPLANE WIRING LIST.
3. THIS SYMBOL INDICATES CONNECTION TO CARD CAGE FRAME.

2019-3

Figure 5-49. Overall Interconnection Diagram

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section provides information for ordering replacement parts for the HP 2116B Computer. Tables 6-1 through 6-17 provide part numbers and descriptions of replacement parts which are identified by index numbers in figures 6-1 through 6-17. Index numbers for all exploded views in this section are arranged in order of disassembly; assembly order is merely the reverse order of disassembly. Table 6-18 defines abbreviations and reference designations used in the parts tables and in other portions of this manual. Table 6-19 provides a total quantity listing of all the electrical parts and table 6-20 provides a total quantity listing of all the mechanical parts used in the computer. The parts in tables 6-19 and 6-20 are listed in numerical order by part number. Table 6-21 identifies the manufacturers indicated by manufacturers code numbers in the replaceable parts tables.

6-3. DESCRIPTION OF PARTS TABLES.

6-4. Table 6-1 lists the assemblies, and their attaching parts, of the basic computer. Tables 6-2, 6-4, and 6-7 list replaceable parts for the three major portions of the computer: the door assembly, the card cage assembly, and the power supply and back panel assembly. The remaining parts tables list replaceable parts in the assemblies which make up the three major portions.

6-5. The electronic assemblies which make up the basic computer configuration are listed in table 1-1 at the front of this manual. The replaceable parts tables list the parts used in this basic configuration, with the exception of parts on I/O control card A201 and I/O address card A202. Parts for these two cards are listed in Volume Three, Input/Output System Operation Manual, Model 2116B Computer.

6-6. The replaceable parts tables furnish the following information:

a. The figure number of the illustration accompanying each table.

b. The index number (callout number) which identifies each replaceable part in the illustration.

c. The HP part number for each replaceable part.

d. A description of the part and its applicable reference designation.

Note

Items in the DESCRIPTION column of the replaceable parts lists are indented to indicate item relationships, as follows:

Major Assembly
*Subassembly
*Attaching Parts for Subassembly
**Subassembly Parts
**Attaching Parts for Subassembly Parts

e. A manufacturer's code number, identifying the manufacturer of the part.

f. The part number which the designated manufacturer uses to identify the part.

g. The quantity of each part used in the assembly or subassembly to which it belongs.

6-7. When a part number is included in the title of a replaceable parts table, the assembly covered by the table can be ordered as an assembled unit. If the part number of the assembly is not in the title, only component parts of the assembly can be ordered.

6-8. DESCRIPTION OF TABLE OF REFERENCE DESIGNATIONS AND ABBREVIATIONS.

6-9. The abbreviations defined in table 6-18 are used in the replaceable parts tables and in other parts of this manual. The reference designations in the table are used only on logic/schematic diagrams.

6-10. DESCRIPTION OF TOTAL-QUANTITY TABLES.

6-11. Tables 6-19 and 6-20 list the total quantity of each replaceable part used in the computer. Table 6-19 includes electrical parts used on I/O control card A201 and I/O address card A202, although they are already illustrated and listed in Volume Three of the computer documentation. They are repeated here only to provide a true total quantity listing for all parts which are considered part of the basic computer.

6-12. ORDERING PROCEDURE.

6-13. To order replacement parts or to obtain additional information about ordering, address the inquiry to the nearest Hewlett-Packard Sales and Service Office. Addresses of these offices are listed at the back of this manual.

6-14. When ordering, give the following information for each part:

a. Computer model number.

b. Computer serial number.

c. Hewlett-Packard part number.

d. Description of part.

e. The revision code of the etched-circuit card (if any) on which the part is installed.

f. Circuit reference designation. Include assembly reference designation as a prefix. For instance, order capacitor C1 of logic shift card A108 by the reference designation A108C1.

6-15. To order a part not listed in the replaceable parts tables, give a complete description of the part, and describe its function and location.

Table 6-1. HP 2116B Computer, Replaceable Parts

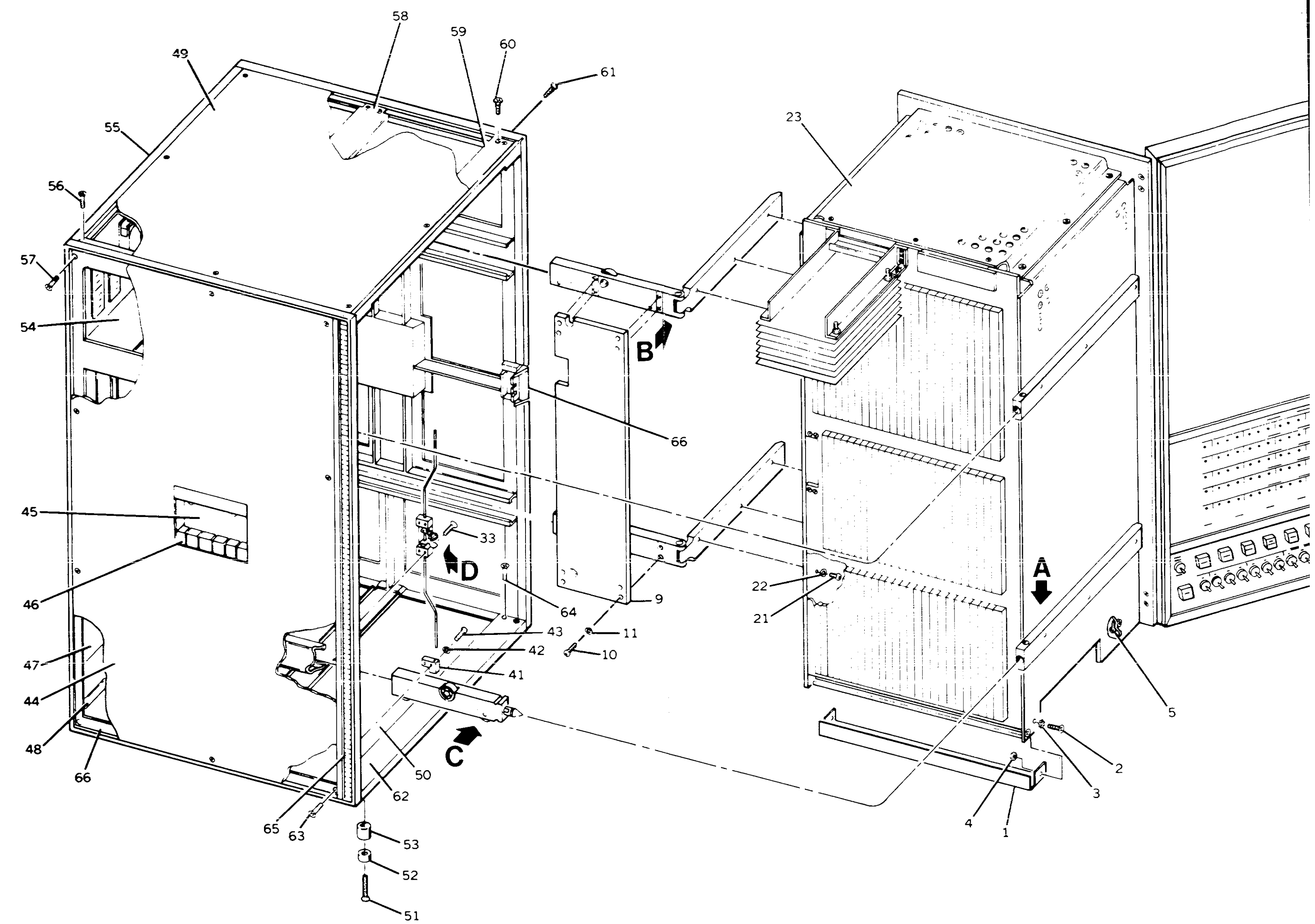
FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-1-	2116B	COMPUTER			
1	02116-0105	* Fan Cover	28480	02116-0105	1
		(Attaching Parts)			
2	2360-0200	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	2
3	2190-0047	* Washer, Recessed, No. 6	00000	OBD	2
4	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
5	1400-0126	* Cable Clamp	00000	OBD	1
		(Attaching Parts)			
	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	1
	3050-0228	* Washer, Flat, No. 6	00000	OBD	1
	2190-0006	* Washer, Lock, Split, No. 6	00000	OBD	1
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	1
		- - - x - - -			
6	02116-6287	* Door Assembly (A500)(see fig. 6-2)	28480	02116-6287	1
		(Attaching Parts)			
	2200-0709	* Screw, Nylon, FH, No. 4-40, 3/8 in.	00000	OBD	4
		- - - x - - -			
7	02116-2013	* Support Bar	28480	02116-2013	1
		(Attaching Parts)			
	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	6
	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	6
		- - - x - - -			
8	0570-1049	* Spring Plunger	01226	M-54N	2
9	02116-0028	* Support Plate	28480	02116-0028	1
		(Attaching Parts)			
10	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	8
11	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	8
		- - - x - - -			
12	02116-2015	* Bearing Shaft	28480	02116-2015	4
13	1410-0009	* Bearing, Ball, Annular	21335	SIKFS58115	2
14	0590-0010	* Cap Nut, No. 8	00000	OBD	2
15	2190-0010	* Washer, Lock, ext-tooth, No. 8	00000	OBD	2
16	02116-2003	* Eccentric Screw, No. 8	28480	02116-2003	2
17	1410-0009	* Bearing, Ball, Annular	21335	SIKFS58115	2
18	02116-2016	* Hinge Pin	28480	02116-2016	2
19	02116-2012	* Hinged Slide	28480	02116-2012	2
20	02116-2014	* Hinged Bar	28480	02116-2014	2
		(Attaching Parts)			
21	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	6
22	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	6
		- - - x - - -			
23	NSR	* Card Cage Assembly (see fig. 6-4)			
24	02116-2015	* Bearing Shaft	28480	02116-2015	4
25	1410-0009	* Bearing, Ball, Annular	21335	SIKFS58115	4
26	0590-0010	* Cap Nut, No. 8	00000	OBD	2
27	2190-0010	* Washer, Lock, ext-tooth, No. 8	00000	OBD	2
28	02116-2003	* Eccentric Screw, No. 8	28480	02116-2003	2
29	1410-0009	* Bearing, Ball, Annular	21335	SIKFS58115	2

Table 6-1. HP 2116B Computer, Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-1-					
30	02116-2023	* Insert, Catch Rod	28480	02116-2023	2
31	02116-2002	* Slide Pin	28480	02116-2002	2
32	02116-2011	* Lower Slide	28480	02116-2011	1
	02116-2010	* Upper Slide (not shown in fig. 6-1)	28480	02116-2010	1
33	2360-0204	* Screw, Machine, FH, No. 6-32, 3/4 in.	00000	OBD	4
34	02116-2034	* Tab Catch, Upper	28480	02116-2034	1
35	02116-2063	* Tab Catch, Lower	28480	02116-2063	1
		(Attaching Parts for items 34 and 35)			
36	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	2
37	2190-0108	* Washer, Lock, Split, No. 4	00000	OBD	2
		- - - x - - -			
38	1460-0742	* Spring, Compression, 5/8 in. long, 3/16 in. I.D.	00000	OBD	1
39	02116-2033	* Catch Rod	28480	02116-2033	2
40	02116-2032	* Latch Retainer	28480	02116-2032	1
41	02116-2023	* Guide, Rod, Lower	28480	02116-2023	1
	02116-2067	* Guide, Rod, Upper (not shown in fig. 6-1)	28480	02116-2067	1
		(Attaching Parts)			
42	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
43	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	2
		- - - x - - -			
44	02116-0013	* Side Cover	28480	02116-0013	2
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	20
		- - - x - - -			
45	5060-0735	* Retaining Plate, Handle	28480	5060-0735	2
		(Attaching Parts)			
	2360-0201	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	4
		- - - x - - -			
46	5060-0763	* Handle	28480	5060-0763	2
47	02116-0015	* Cover, Upper-Rear	28480	02116-0015	1
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	9
		- - - x - - -			
48	02116-0014	* Cover, Lower-Rear	28480	02116-0014	1
		(Attaching Parts)			
	2360-0192	* Screw, Machine, FH, No. 6-32, 1/4 in.	00000	OBD	3
		- - - x - - -			
49	02116-0016	* Cover, Top	28480	02116-0016	1
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	8
		- - - x - - -			
50	02116-0016	* Cover, Bottom	28480	02116-0016	1
		(Attaching Parts)			
51	2360-0209	* Screw, Machine, PH, No. 6-32, 1 in.	00000	OBD	4
52	0403-0091	* Insert, Foot	28480	0403-0091	4
53	02116-2057	* Foot, Cabinet	28480	02116-2057	4
		- - - x - - -			

Table 6-1. HP 2116B Computer, Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-1-					
54	02116-6124	* Power Supply and Back Panel Assembly (see fig. 6-7)	28480	02116-6124	1
		(Attaching Parts)			
	2510-0107	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	14
		- - - x - - -			
55	02116-2009	* Rear Brace	28480	02116-2009	2
		(Attaching Parts)			
56	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
57	2360-0201	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
		- - - x - - -			
58	02116-0012	* Center Brace	28480	02116-0012	2
		(Attaching Parts)			
	2360-0196	* Screw, Machine, FH, No. 6-32, 3/8 in.	00000	OBD	8
		- - - x - - -			
59	02116-2077	* Brace, Top-Front	28480	02116-2077	1
		(Attaching Parts)			
60	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
61	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
		- - - x - - -			
62	02116-2041	* Brace, Bottom-Front	28480	02116-2041	1
		(Attaching Parts)			
63	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
64	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
		- - - x - - -			
65	5000-0131	* Trim, Aluminum	28480	5000-0131	2
66	02116-2017	* Main Frame	28480	02116-2017	2



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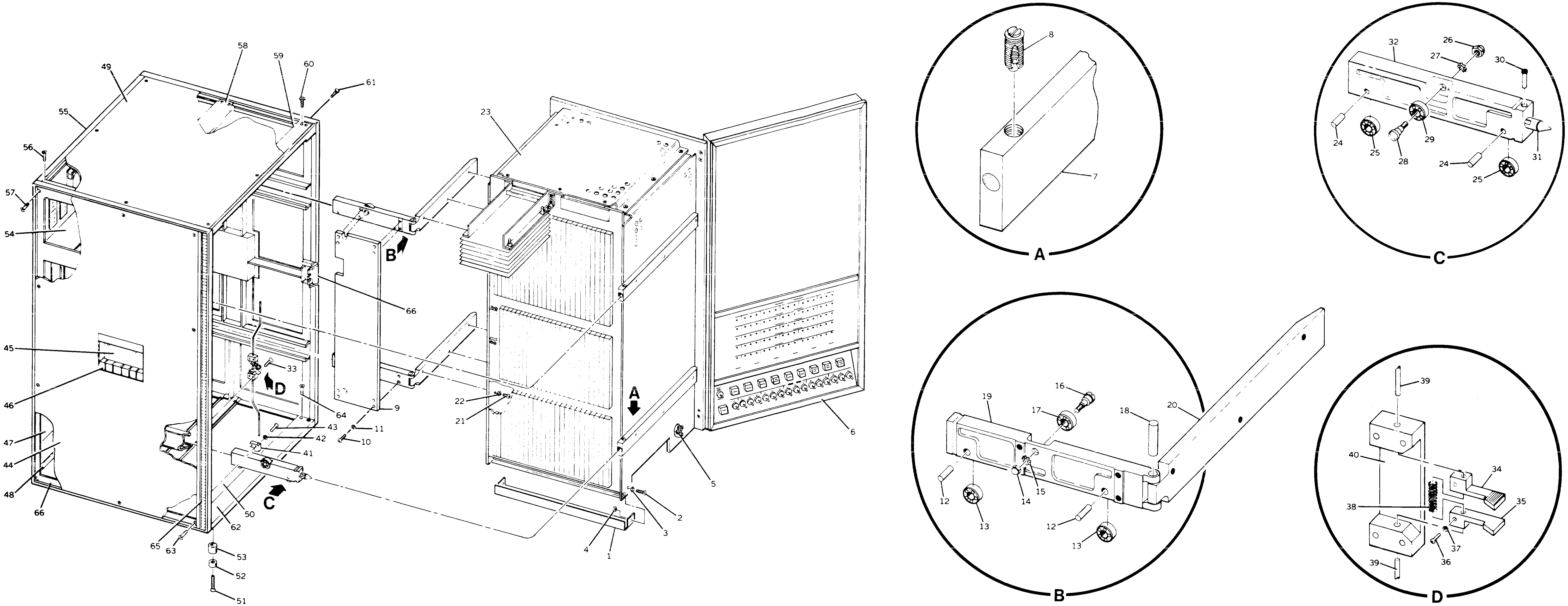

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Figure 6-1. HP2116B Computer, Exploded View

Table 6-2. A500 Door Assembly (02116-6286), Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-2-	02116-6287	DOOR ASSEMBLY (A500)(6, fig. 6-1)	28480	02116-6287	1
1	2360-0192	* Screw, Machine, FH, No. 6-32, 1/4 in.	00000	OBD	10
2	1390-0107	* Button Latch	13061	B10-B1	1
		(Attaching Parts)			
3	2360-0202	* Screw, Machine, FH, No. 6-32, 3/8 in.	00000	OBD	1
4	0590-0077	* Nut, Self-Locking, Hexagon, No. 6-32	00000	OBD	1
		---x---			
5	4040-0431	* Air Deflector	28480	4040-0431	1
		(Attaching Parts)			
6	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
7	3050-0228	* Washer, Flat, No. 6	00000	OBD	6
8	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	6
9	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	6
		---x---			
10	0400-0082	* Grommet, Nylon	28480	0400-0082	1
11	1400-0741	* Cable Clamp, Base	28480	1400-0741	1
		(Attaching Parts)			
12	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
13	3050-0226	* Washer, Flat, No. 10	00000	OBD	1
		---x---			
14	0400-0082	* Grommet, Nylon	28480	0400-0082	1
15	02116-0101	* Subpanel	28480	02116-0101	1
16	02116-6290	* Cable Assembly (A102)	28480	02116-6290	1
	02116-6291	* Cable Assembly (A103)(not shown in fig. 6-2)	28480	02116-6291	1
	02116-6292	* Cable Assembly (A104)(not shown in fig. 6-2)	28480	02116-6292	1
	02116-6293	* Cable Assembly (A105)(not shown in fig. 6-2)	28480	02116-6293	1
	02116-6294	* Cable Assembly (A106)(not shown in fig. 6-2)	28480	02116-6294	1
17	2140-0035	* Lamp, Incandescent, 6.3V, 0.75A	71744	1775	88
18	3101-0973	* Switch, Slide, DPDT, 125V, 0.5A, AC/DC (S111, S112, S113)	79727	G126-0018	3
19	02116-6043	* Display Board	28480	02116-6043	1
		(Attaching Parts)			
20	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	12
21	2190-0108	* Washer, Lock, Split, No. 4	00000	OBD	12
22	3050-0222	* Washer, Flat, No. 4	00000	OBD	12
		---x---			
23	1390-0179	* Lock and Key	74842	D5416J	1
		(Attaching Parts)			
24	No Number	* Screw, Machine, RH (furnished with item 23)			1
25	No Number	* Washer, Lock, int-tooth (furnished with item 23)			1
26	No Number	* Latch (furnished with item 23)			1
27	02116-2079	* Spacer	28480	02116-2079	1
		---x---			
28	0404-0371	* Trim, Strip, Right	28480	0404-0371	1
29	0404-0247	* Trim, Strip	28480	0404-0247	2
30	0404-0248	* Trim, Strip, Left	28480	0404-0248	1

Table 6-2. A500 Door Assembly (02116-6286), Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-2-					
31	1400-0124	* Cable Clamp	00000	OBD	5
		(Attaching Parts)			
32	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	5
33	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	5
34	3050-0228	* Washer, Flat, No. 6	00000	OBD	5
		- - - x - - -			
35	02116-0102	* Cable Clamp Bracket	28480	02116-0102	1
		(Attaching Parts)			
	2360-0200	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
36	0460-0020	* Adhesive Cork	28480	0460-0020	1
37	02116-2022	* Vertical Brace	28480	02116-2022	1
38	02116-2078	* Vertical Brace	28480	02116-2078	1
		(Attaching Parts for items 37 and 38)			
	2360-0200	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	6
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	6
		- - - x - - -			
39	02116-2021	* Horizontal Brace	28480	02116-2021	1
		(Attaching Parts)			
	2360-0200	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			
40	02116-0090	* Top Door Panel	28480	02116-0090	1
41	02116-0007	* Panel Brace	28480	02116-0007	1
		(Attaching Parts)			
42	2360-0204	* Screw, Machine, FH, No. 6-32, 3/4 in.	00000	OBD	4
43	3050-0228	* Washer, Flat, No. 6	00000	OBD	4
44	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			
45	02116-2027	* Vertical Bracket	28480	02116-2027	2
		(Attaching Parts)			
46	2360-0200	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	4
	3050-0228	* Washer, Flat, No. 6	00000	OBD	4
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	4
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
		- - - x - - -			
47	02116-2026	* Horizontal Bracket	28480	02116-2026	2
		(Attaching Parts)			
48	2360-0205	* Screw, Machine, PH, No. 6-32, 3/4 in.	00000	OBD	8
49	3050-0228	* Washer, Flat, No. 6	00000	OBD	8
50	3050-0228	* Washer, Flat, No. 6	00000	OBD	8
51	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	8
52	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	8
		- - - x - - -			
53	02116-0007	* Panel Brace	28480	02116-0007	1
54	02116-4002	* Light Mask	28480	02116-4002	1
55	02116-8302	* Negative Film	28480	02116-8302	1

Table 6-2. A500 Door Assembly (02116-6286), Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-2-					
56	4320-0096	* Extrusion, rubber	28480	4320-0096	1
57	4330-0186	* Window, Glass	28480	4330-0186	1
58	No Number	* Control Panel Assembly (A502)(see fig. 6-3)			1
59	02116-2009	* Bezel, Upper	28480	02116-2009	1
60	02116-2052	* Bezel, Lower	28480	02116-2052	1
		(Attaching Parts for items 59 and 60)			
61	2360-0200	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	8
		- - - x - - -			
62	4320-0043	* Channel, rubber	28480	4320-0043	1
63	02116-6295	* Door Frame	28480	02116-6295	1

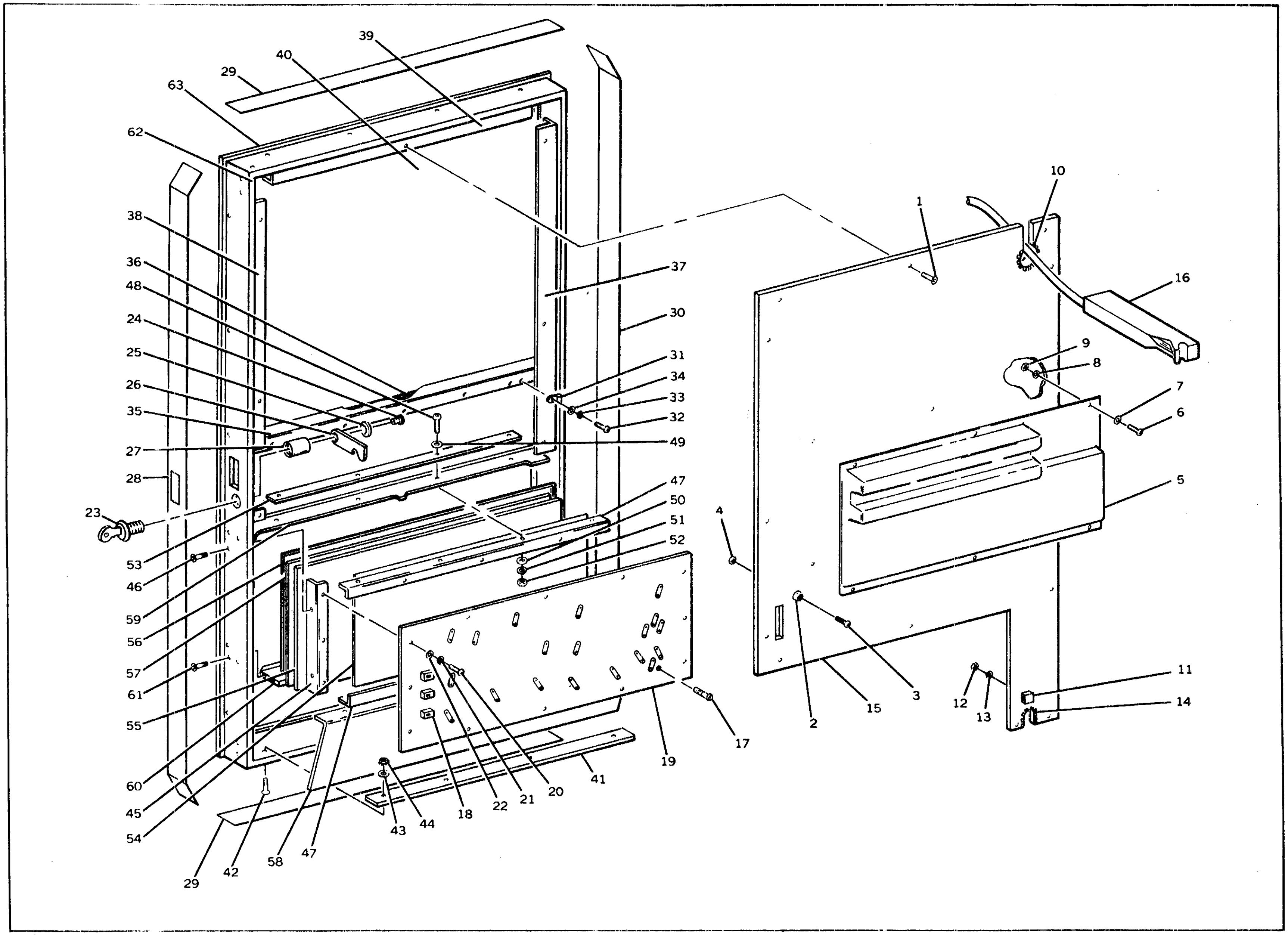

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Figure 6-2. A500 Door Assembly (02116-6286), Exploded View

Table 6-3. A502 Control Panel Assembly, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-3-	No Number	CONTROL PANEL ASSEMBLY (A502) (58, fig. 6-2)			1
1	1400-0127	* Cable Clamp	00000	OBD	1
		(Attaching Parts)			
2	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	1
3	2190-0006	* Washer, Lock, Split, No. 6	00000	OBD	1
4	3050-0228	* Washer, Flat, No. 6	00000	OBD	1
		- - - x - - -			
5	0360-0268	* Terminal Lug, No. 6	00000	OBD	1
		(Attaching Parts)			
6	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
		- - - x - - -			
7	3101-0719	* Lens (POWER)	28480	3101-0719	1
8	3101-0714	* Switch, Lighted Pushbutton (S109)	28480	3101-0714	1
		(Attaching Parts)			
9	No Number	* Washer, Lock, int-tooth (furnished with item 8)			1
10	No Number	* Nut, Plain, Hexagon (furnished with item 8)			1
		- - - x - - -			
11	0362-0188	* Cover, Power Switch	28480	0362-0188	1
12	3101-0718	* Lens (PRESET)	28480	3101-0718	1
13	3101-0716	* Lens (RUN)	28480	3101-0716	1
14	3101-0721	* Lens (HALT)	28480	3101-0721	1
15	3101-0723	* Lens (LOAD MEMORY)	28480	3101-0723	1
16	3101-0724	* Lens (LOAD A)	28480	3101-0724	1
17	3101-0722	* Lens (LOAD B)	28480	3101-0722	1
18	3101-0717	* Lens (LOAD ADDRESS)	28480	3101-0717	1
19	3101-0725	* Lens (DISPLAY MEMORY)	28480	3101-0725	1
20	3101-0720	* Lens (SINGLE CYCLE)	28480	3101-0720	1
21	3101-0715	* Switch, Lighted Pushbutton (S100 thru S108)	28480	3101-0715	9
	2140-0035	* Lamp, Incandescent, 6V, 0.75A (DS106 thru DS109)	71744	7175	4
		(Attaching Parts)			
22	No Number	* Washer, Lock, int-tooth (furnished with item 21)			1
23	No Number	* Nut, Plain, Hexagon (furnished with item 21)			1
		- - - x - - -			
24	02116-0080	* Subpanel	28480	02116-0080	1
		(Attaching Parts)			
25	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	1
26	2190-0006	* Washer, Lock, Split, No. 6	00000	OBD	1
		- - - x - - -			
27	3101-1051	* Switch, Toggle, SPST, 125V, 3A (S1 thru S16, S116)	88140	8908K507	17
		(Attaching Parts)			
28	3130-0130	* Nut, Face, 1/2 in. I.D.	28480	3130-0130	17
29	2190-0102	* Washer, Lock, int-tooth, 1/2 in. I.D.	00000	OBD	17
30	2950-0035	* Nut, Plain, Hexagon, 15/32-32	00000	OBD	17
		- - - x - - -			
31	02116-0005	* Front Panel	28480	02116-0005	1

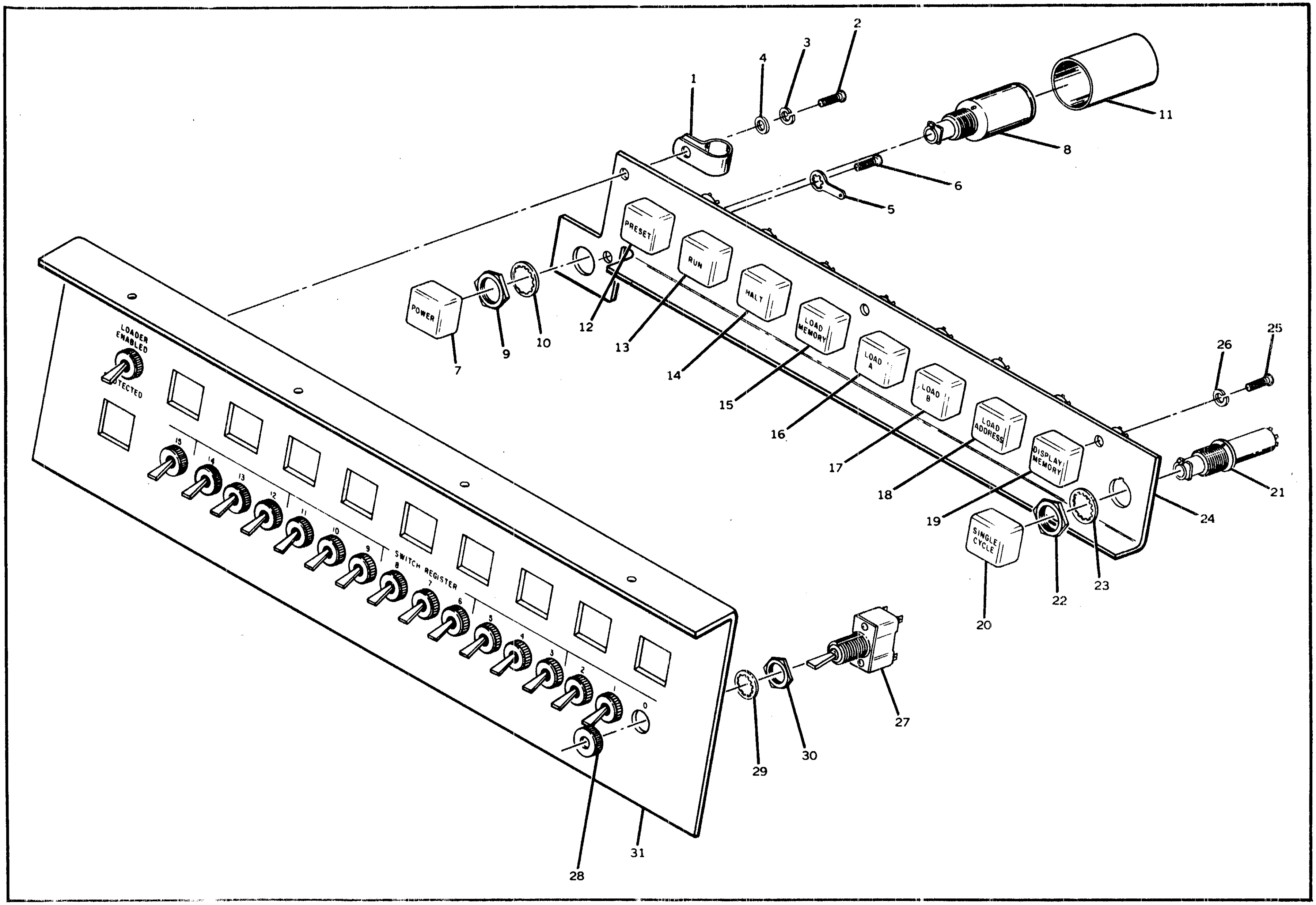

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Figure 6-3. A502 Control Panel Assembly, Exploded View

Table 6-4. Card Cage Assembly, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-4-	NSR	CARD CAGE ASSEMBLY (23, fig. 6-1)			1
1	02116-6175	* Power Fail Interrupt Card (A1)(see fig. 5-7)	28480	02116-6175	1
2	02116-6300	* Memory Module Decoder Card (A2)(see fig. 5-9)	28480	02116-6300	1
3	02116-6298	* Sense Amplifier Card (A12, A13)(see fig. 5-15)	28480	02116-6298	2
4	02116-6266	* Driver/Switch Card (A14, A15)(see fig. 5-13)	28480	02116-6266	2
5	02116-6265	* Inhibit Driver Card (A16, A18)(see fig. 5-11)	28480	02116-6265	2
6	02116-6069	* Direct Memory Logic Card (A20)(see fig. 5-17)	28480	02116-6069	1
7	02116-0085	* Card Retainer	28480	02116-0085	2
8	3190-0107	* Button Latch	13061	B10-B1	1
9	02116-2080	* Door Catch	28480	02116-2080	1
10	8120-1214	* Ground Cable, 27.5 in.	28480	8120-1214	1
11	02116-6194	* I/O Address Card (A202)(see Volume Three)	28480	02116-6194	1
12	02116-6041	* I/O Control Card (A201)(see Volume Three)	28480	02116-6041	1
13	02116-6029	* Shift Logic Card (A108)(see fig. 5-27)	28480	02116-6029	1
14	02116-6027	* Instruction Decoder Card (A107)(see fig. 5-25)	28480	02116-6027	1
15	02116-6281	* Timing Generator Card (A106)(see fig. 5-23)	28480	02116-6281	1
16	02116-6026	* Arithmetic Logic Card (A2 thru A5)(see fig. 5-21)	28480	02116-6026	4
17	02116-6208	* Front Panel Coupler Card (A101)(see fig. 5-19)	28480	02116-6208	1
18	02116-0087	* Cable Spacer	28480	02116-0087	1
		(Attaching Parts)			
19	2510-0102	* Screw, Machine, FH, No. 8-32, 3/8 in.	00000	OBD	3
		- - - x - - -			
20	02116-0089	* Top Panel	28480	02116-0089	1
		(Attaching Parts)			
21	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	6
22	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	6
23	3050-0139	* Washer, Flat, No. 8	00000	OBD	6
		- - - x - - -			
24	0811-2031	* Resistor, Fxd, WW, 815 ohms, 3.0%, 1/4w (A402R220, A402R221)	01686	7010	2
25	02116-01103	* Resistor Bracket	28480	02116-01103	1
		(Attaching Parts)			
26	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	2
27	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	2
28	3050-0139	* Washer, Flat, No. 8	00000	OBD	2
		- - - x - - -			
29	02116-6288	* Core Stack Assembly (A400)	28480	02116-6288	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	4
	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	4
	3050-0139	* Washer, Flat, No. 8	00000	OBD	4
		- - - x - - -			
30	02116-0088	* Filler Plate	28480	02116-0088	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	4
	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	4
	3050-0139	* Washer, Flat, No. 8	00000	OBD	4
		- - - x - - -			

Table 6-4. Card Cage Assembly, Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-4-					
31	02116-6284	* Overvoltage Protection Assembly (A121)(see fig. 6-5)	28480	02116-6284	1
		(Attaching Parts)			
	2360-0196	* Screw, Machine, FH, No. 6-32, 3/8 in.	00000	OBD	4
	2190-0047	* Washer, Recessed, No. 6	00000	OBD	4
		- - - x - - -			
32	02116-2072	* Support Bar	28480	02116-2072	1
		(Attaching Parts)			
	2530-0017	* Screw, Machine, FH, No. 8-32, 1/4 in.	00000	OBD	2
	2190-0048	* Washer, Recessed, No. 8	00000	OBD	2
		- - - x - - -			
33	0360-1255	* Terminal Board (A100TB1, A100TB2)	00000	OBD	2
		(Attaching Parts)			
34	2370-0030	* Screw, Machine, FH, No. 6-32, 1-1/2 in.	00000	OBD	2
35	2190-0047	* Washer, Recessed, No. 6	00000	OBD	2
36	0380-0002	* Spacer, 1/4 in.	00000	OBD	2
37	2420-0001	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	2
		- - - x - - -			
38	02116-0032	* Bottom Panel	28480	02116-0032	1
		(Attaching Parts)			
39	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
40	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	4
41	2580-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	4
		- - - x - - -			
42	02116-2040	* Bezel	28480	02116-2040	1
		(Attaching Parts)			
43	2510-0102	* Screw, Machine, FH, No. 8-32, 3/8 in.	00000	OBD	18
		- - - x - - -			
44	NSR	* Card Rack Assembly			4
		(Attaching Parts)			
45	2360-0200	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	16
46	2190-0147	* Washer, Recessed, No. 6	00000	OBD	16
		- - - x - - -			
47	02116-2075	* * PC Guide Support	28480	02116-2075	2
48	02116-4007	* * PC Guide	28480	02116-4007	22
49	02116-8199	* Indicator, Strip, Top	28480	02116-8199	1
50	02116-8200	* Indicator, Strip, Middle	28480	02116-8200	1
51	02116-8201	* Indicator, Strip, Bottom	28480	02116-8201	1
52	0360-1264	* Terminal Lug	28480	0360-1264	2
53	0360-1260	* Terminal Lug	28480	0360-1260	7
54	0360-1256	* Terminal Board (A200TB1)	28480	0360-1256	1
		(Attaching Parts)			
	2360-0205	* Screw, Machine, PH, No. 6-32, 3/4 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			
55	3160-0099	* Fan Grille	23936	5504	3
		(Attaching Parts)			
56	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	12

Table 6-4. Card Cage Assembly, Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-4-					
57	3050-0139	* Washer, Flat, No. 8	00000	OBD	12
58	2580-0003	* Nut, Assembled Washer, No. 8-32	00000	OBD	12
		- - - x - - -			
59	3160-0072	* Fan Assembly, 115V, 60Hz (A200B1, B2, B3)	23936	Model 2500	3
		(Attaching Parts)			
60	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	12
61	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	12
		- - - x - - -			
62	02116-0010	* Fan Panel	28480	02116-0010	1
		(Attaching Parts)			
63	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
64	2190-0048	* Washer, Recessed, No. 8	00000	OBD	4
	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	4
	2580-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	4
65	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	3
	2190-0017	* Washer, Lock, No. 8	00000	OBD	3
	2580-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	3
		- - - x - - -			
66	02116-0008	* Side Panel, Right	28480	02116-0008	1
67	02116-0009	* Side Panel, Left	28480	02116-0009	1
		(Attaching Parts for items 66 and 67)			
68	2530-0017	* Screw, Machine, FH, No. 8-32, 1/4 in.	00000	OBD	12
69	2190-0048	* Washer, Recessed, No. 8	00000	OBD	12
		- - - x - - -			
70	02116-6282	* Back Panel Assembly, Card Cage	28480	02116-6282	1
71	No Number	** Connector Pin	00779	67628-2	A/R
72	3050-0238	** Washer, Nonmetallic, Shouldered, No. 8	00000	OBD	4

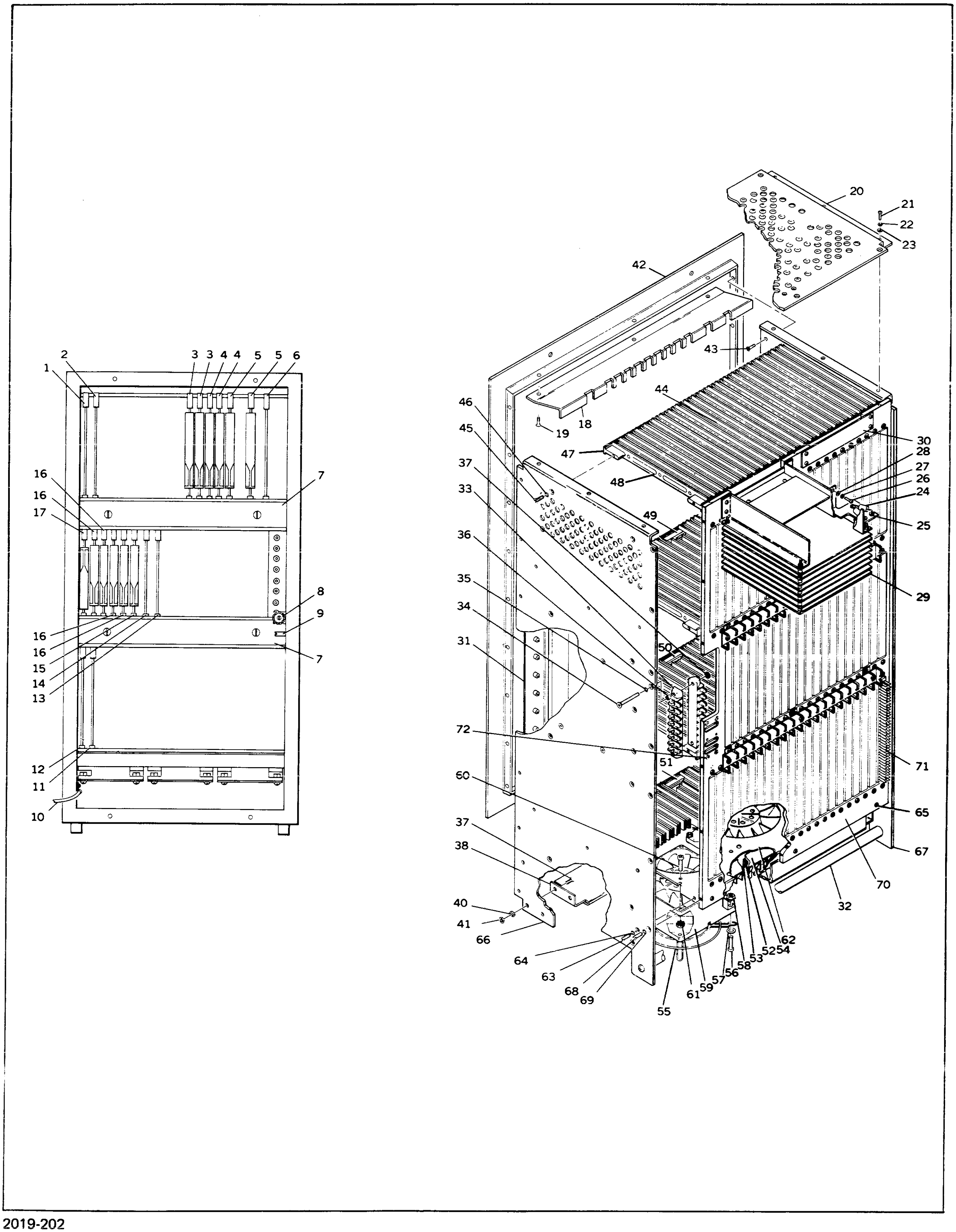

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Figure 6-4. Card Cage Assembly, Exploded View

Table 6-5. A121 Overvoltage Protection Assembly (02116-6284), Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-5-	02116-6284	OVERVOLTAGE PROTECTION ASSEMBLY (A121)(31, fig. 6-3)	28480	02116-6284	1
1	1250-0367	* Jack, Tip (TP1 thru TP8)	28480	1251-0367	8
2	4320-0002	* Gasket, Rubber	28480	4320-0002	1
3	02116-0100	* Cover, Overvoltage Protection	28480	02116-0100	1
		(Attaching Parts)			
4	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	6
5	2190-0017	* Washer, Lock, Split, No. 8	00000	OBD	6
		- - - x - - -			
6	02116-6126	* Overvoltage, Component Board Assembly (see fig. 6-6)	28480	02116-6126	1
		(Attaching Parts)			
7	2360-0109	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	4
8	2190-0007	* Washer, Lock, int-tooth, No. 6	00000	OBD	4
9	3050-0247	* Washer, Nonmetallic, No. 6	00000	OBD	4
		- - - x - - -			
10	1901-0343	* Diode, Si, 50 PIV, 18A, (CR1, CR7, CR11, CR15)	04713	IN3491R	4
11	1902-1218	* Diode, Breakdown, 39V, 2% at 65 mA (CR16)	04713	SZ11747	1
		(Attaching Parts)			
12	1200-0080	* Washer, Flat, Anodized, No. 10	28480	1200-0080	2
13	3050-0226	* Washer, Flat, No. 10	00000	OBD	1
14	3050-0270	* Terminal Lug, No. 10	00000	OBD	1
15	2470-0002	* Nut, Plain, Hexagon, No. 10	00000	OBD	1
		- - - x - - -			
16	1884-0046	* Thyristor, SCR, 50V, 25A (Q3, Q4, Q5)	28480	1884-0046	3
		(Attaching Parts)			
17	1200-0088	* Washer, Flat, Anodized	28480	1200-0088	6
18	3050-0225	* Washer, Flat, 1/4 I.D.	00000	OBD	3
19	0360-0271	* Terminal Lug, 1/4 I.D.	00000	OBD	3
20	2950-0036	* Nut, Plain, Hexagon, 1/4-28	00000	OBD	3
		- - - x - - -			
21	1902-1228	* Diode, Breakdown, 27V, 10%, 10 w (CR12)	28480	1902-1228	1
		(Attaching Parts)			
22	1200-0080	* Washer, Flat, Anodized, No. 10	28480	1200-0080	2
23	3050-0226	* Washer, Flat, No. 10	00000	OBD	1
24	3050-0270	* Terminal Lug, No. 10	00000	OBD	1
25	2470-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
		- - - x - - -			
26	1902-1205	* Diode, Breakdown, 15V, +2% (CR8)	04713	IN2979RB	1
		(Attaching Parts)			
27	1200-0080	* Washer, Flat, Anodized, No. 10	28480	1200-0080	2
28	3050-0226	* Washer, Flat, No. 10	00000	OBD	1
29	3050-0270	* Terminal Lug, No. 10	00000	OBD	1
30	2470-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
		- - - x - - -			

Table 6-5. A121 Overvoltage Protection Assembly (02116-6284), Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-5-					
31	02116-2060	* Mounting Bar, Front	28480	02116-2060	1
32	1880-0047	* Thyristor, SCR, 25V, 55A (Q1)	28480	1884-0047	1
		(Attaching Parts)			
33	1200-0089	* Washer, Flat, Anodized	28480	1200-0089	2
34	0362-0128	* Crimp Lug, Termination	00000	OBD	1
35	0360-1089	* Terminal Lug, 1/2 in. I.D.	00000	OBD	1
36	2190-0043	* Washer, Lock, Split, 1/2 in. I.D.	00000	OBD	1
37	2950-0024	* Nut, Plain, Hexagon, 1/2-20	00000	OBD	1
		- - - x - - -			
38	02116-2059	* Mounting Bar, Upper	28480	02116-2059	1
		(Attaching Parts)			
39	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	2
40	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	2
		- - - x - - -			
41	1884-0047	* Thyristor, SCR, 25V, 55A (Q2)	28480	1884-0047	1
		(Attaching Parts)			
42	0362-0128	* Crimp Lug, Termination	00000	OBD	1
43	0360-1089	* Terminal Lug, 1/2 in. I.D.	00000	OBD	1
44	2190-0043	* Washer, Lock, Split, 1/2 in. I.D.	00000	OBD	1
45	2950-0024	* Nut, Plain, Hexagon, 1/2-20	00000	OBD	1
		- - - x - - -			
46	02116-2064	* Mounting Bar, Lower	28480	02116-2064	1
		(Attaching Parts)			
47	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	2
48	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	2
		- - - x - - -			
49	1902-1217	* Diode, Breakdown, 6.2V, 5% (CR2)	04713	SZ11746	1
		(Attaching Parts)			
50	1200-0080	* Washer, Flat, Anodized, No. 10	28480	1200-0080	2
51	3050-0226	* Washer, Flat, No. 10	00000	OBD	1
52	3050-0270	* Terminal Lug, No. 10	00000	OBD	1
53	2470-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
		- - - x - - -			
54	1901-0406	* Diode, Si, 50PIV, 18A (CR3, CR9, CR13)	04713	IN3491/MR-322	3
55	1884-0046	* Thyristor, SCR, 50V, 25A (Q6, Q7)	28480	1884-0046	2
		(Attaching Parts)			
56	2190-0070	* Washer, Lock, ext-tooth, 1/4 in. I.D.	00000	OBD	2
57	2950-0036	* Nut, Plain, Hexagon, 1/4-28	00000	OBD	2
		- - - x - - -			
58	1902-1205	* Diode, Breakdown, 15V, +2% (CR10)	04713	IN2979RB	1
59	2120-0012	* Washer, Lock, ext-tooth, No. 10	00000	OBD	1
60	2470-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
		- - - x - - -			

Table 6-5. A121 Overvoltage Protection Assembly (02116-6284), Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-5-					
61	1902-1228	* Diode, Breakdown, 27V, 10w, 5% (CR14)	28480	1902-1228	1
		(Attaching Parts)			
62	2120-0012	* Washer Lock, ext-tooth, No. 10	00000	OBD	1
63	2470-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
		- - - x - - -			
64	02116-2061	* Mounting Bar, Rear	28480	02116-2061	1

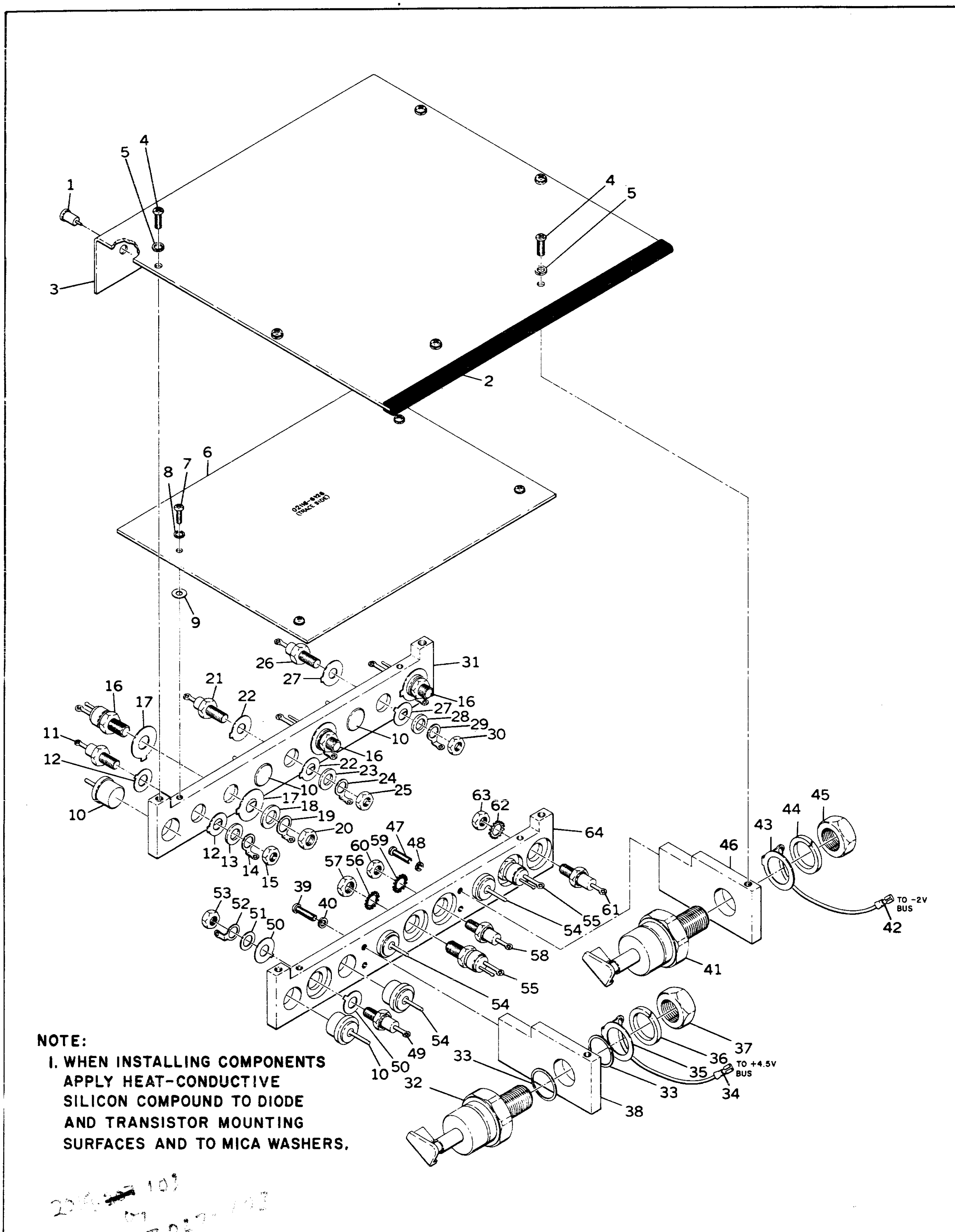

Figure 6-5. A121 Overvoltage Protection Assembly (02116-6284), Exploded View

Table 6-6. A121A1 Overvoltage Component Board Assembly (02116-6126), Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-6-	02116-6126	OVERVOLTAGE COMPONENT BOARD ASSEMBLY (A121A1) (6, fig. 6-5)	28480	02116-6126	1
1	0689-1505	* Resistor, Fxd, Comp, 15 ohms, 5%, 1 w (R1, R4)	01121	GB 1505	2
2	0686-3315	* Resistor, Fxd, Comp, 220 ohms, 5%, 1 w (R2, R3)	01121	EB 2215	2
3	0160-2055	* Capacitor, Fxd, Cer, 0.01 uf, +80 -20%, 100 VDCW (C1 thru C7)	56289	C023F101F103 ZE12-CDH	7
4	0813-0038	* Resistor, Fxd, WW, 0.5 ohms, 10%, 5 w (R7 thru R10, R15 thru R18, R23, R24)	28480	0813-0038	10
5	0811-1857	* Resistor, Fxd, WW, 400 ohms, 5%, 5 w (R25, R26)	28480	0811-1857	2
6	0686-2205	* Resistor, Fxd, Comp, 22 ohms, 5%, 1 w (R5, R12, R13, R20, R21)	01121	EB 2205	5
7	0686-4715	* Resistor, Fxd, Comp, 470 ohms, 5%, 1 w (R6, R11, R14, R19, R22)	01121	EB 4715	5
8	1901-0191	* Diode, Si, 0.75A, 100 PIV (CR4, CR5, CR6)	04713	SR 1358-2	3

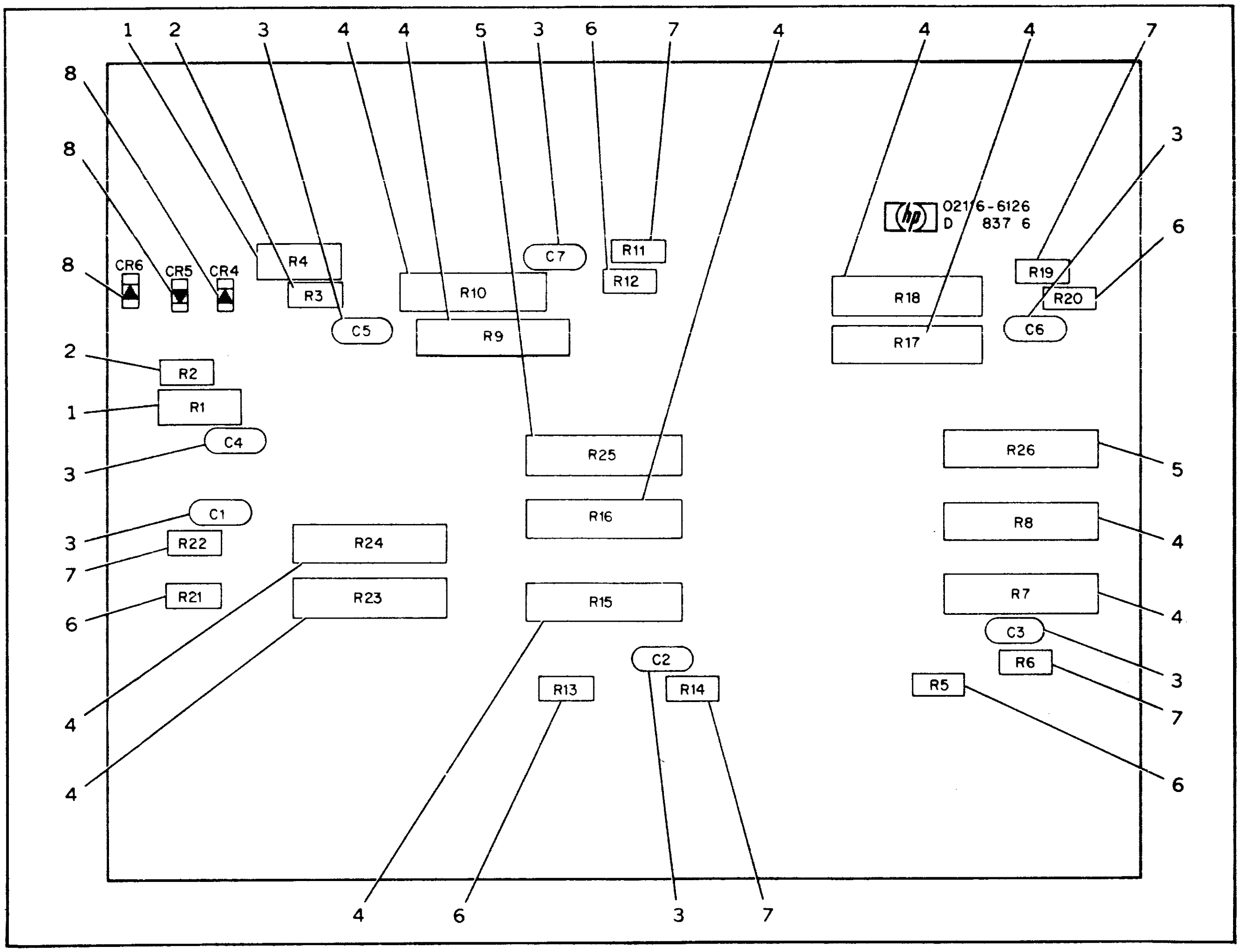

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Figure 6-6. A121A1 Overvoltage Component Board Assembly (02116-6126), Parts Identification Diagram

Table 6-7. A300 Power Supply and Back Panel Assembly (02116-6124), Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-7-	02116-6124	POWER SUPPLY AND BACK PANEL ASSEMBLY (A300) (54, fig. 6-1)	28480	02116-6124	1
1	NSR	* Component Board Assembly (A307) (see fig. 6-10)			1
		(Attaching Parts)			
	2360-0207	* Screw, Machine, PH, No. 6-32, 7/8 in.	00000	OBD	2
	3050-0228	* Washer, Flat, No. 6	00000	OBD	2
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	2
		---x---			
2	NSR	* Component Board Assembly (A306) (see fig. 6-10)			1
		(Attaching Parts)			
	2360-0207	* Screw, Machine, PH, No. 6-32, 7/8 in.	00000	OBD	2
	3050-0228	* Washer, Flat, No. 6	00000	OBD	2
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	2
		---x---			
3	3106-0099	* Grille, Fan	23936	5504	1
		(Attaching Parts)			
	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
	2580-0003	* Nut, Assembled Washer, No. 8	00000	OBD	4
		---x---			
4	3160-0072	* Fan Assembly, 115V, 60 Hz (A300B1)	28480	3160-0072	1
		(Attaching Parts)			
	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	4
	2580-0003	* Nut, Assembled Washer, No. 8-32	00000	OBD	4
		---x---			
5	2200-0141	* Screw, Machine, PH, No. 4-40, 5/16 in.	00000	OBD	1
6	2190-0003	* Washer, Lock, Split, No. 4	00000	OBD	1
7	2190-0108	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	1
8	2200-0143	* Washer, Lock, Split, No. 4	00000	OBD	1
9	5020-1922	* Spacer, Nylon	28480	5020-1922	1
10	2200-0144	* Screw, Machine, FH, No. 4-40, 3/8 in.	00000	OBD	3
11	02116-0074	* Bus Bar Brace	28480	02116-0074	1
12	02116-2069	* Bakelite Spacer	28480	02116-2069	2
13	02116-0075	* Bus Bar Brace	28480	02116-0075	1
		(Attaching Parts)			
	2360-0204	* Screw, Machine, FH, No. 6-32, 3/4 in.	00000	OBD	2
		---x---			
14	02116-0092	* Bus Bar, 2 V	28480	02116-0092	1
15	02116-0093	* Bus Bar (End Output)	28480	02116-0093	1
16	02116-0073	* Bus Bar, 4.5 V	28480	02116-0073	1
17	02116-0077	* Side Bracket	28480	02116-0077	2
		(Attaching Parts)			
18	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	4
19	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	4
		---x---			
20	NSR	* Component Board Assembly (A310) (see fig. 6-10)			1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	2
	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	2
		---x---			

Table 6-7. A300 Power Supply and Back Panel Assembly (02116-6124), Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-7-					
21	02116-0023	* Bracket, Mounting, Bus Bar	28480	02116-0023	1
		(Attaching Parts)			
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	1
		---x---			
22	02116-2035	* Bracket, Capacitor Board, large	28480	02116-2035	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	3
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	3
	3050-0228	* Washer, Flat, No. 6	00000	OBD	3
	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	3
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	3
		---x---			
23	02116-2058	* Bracket, Capacitor Board, small	28480	02116-2058	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	2
	3050-0228	* Washer, Flat, No. 6	00000	OBD	2
	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		---x---			
24	02116-6015	* Memory Supply Regulator Card (A302) (see fig. 6-9)	28480	02116-6015	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	1
	3050-0228	* Washer, Flat, No. 6	00000	OBD	1
		---x---			
25	02116-6014	* Logic Supply Regulator Card (A301) (see fig. 6-9)	28480	02116-6014	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	1
	3050-0228	* Washer, Flat, No. 6	00000	OBD	1
		---x---			
26	1251-0233	* Connector, Receptacle (XA301)	28480	1251-0233	1
27	1251-0335	* Connector, Receptacle (XA302)	28480	1251-0335	1
		(Attaching Parts for items 26, 27)			
	2200-0149	* Screw, Machine, PH, No. 4-40, 5/8 in.	00000	OBD	4
	3050-0222	* Washer, Flat, No. 4	00000	OBD	4
	0590-0076	* Nut, Self-Locking, Hexagon, No. 4	00000	OBD	4
		---x---			
28	No Number	* Capacitor Board Assembly (A303) (see fig. 6-11)			1
		(Attaching Parts)			
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	4
		---x---			
29	02116-0047	* Capacitor Board Bracket	28480	02116-0047	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	3
	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	3
		---x---			

Table 6-7. A300 Power Supply and Back Panel Assembly (02116-6124), Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-7-					
30	02116-0025	* Deck, Blank, Power Supply	28480	02116-0025	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	5
	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	5
		---x---			
31	02116-0026	* Transformer Cover	28480	02116-0026	1
		(Attaching Parts)			
32	0510-0736	* Latch, Male	28480	0510-0736	6
33	0510-0735	* Latch, Female	28480	0510-0735	6
		---x---			
34	0811-2140	* Resistor, Fxd, WW, 2 ohms, 5%, 5 w (A300R1)	28480	0811-2140	1
		(Attaching Parts)			
	2510-0111	* Screw, Machine, PH, No. 8-32, 3/4 in.	00000	OBD	2
	2580-0003	* Nut, Assembled Washer, No. 8-32	00000	OBD	2
		---x---			
35	02116-0022	* Left Brace	28480	02116-0022	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	3
	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	3
		---x---			
36	No Number	* AC Input Section (A312)(see fig. 6-12)			1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	2
	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	2
		---x---			
37	No Number	* Transformer Assembly (A311) (see fig. 6-13)			1
		(Attaching Parts)			
	2680-0103	* Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	4
	2190-0074	* Washer, Lock, Split, No. 10	00000	OBD	4
		---x---			
38	No Number	* Small Heat Sink Assembly (A305) (see fig. 6-14)			1
		(Attaching Parts)			
	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
	0590-0843	* Nut, Self-Locking, Hexagon, No. 8-32	00000	OBD	4
		---x---			
39	No Number	* Large Heat Sink Assembly (A304) (see fig. 6-16)			1
		(Attaching Parts)			
	2510-0107	* Screw, Machine, PH, 8-32, 1/2 in.	00000	OBD	4
	0590-0843	* Nut, Self-Locking, Hexagon, No. 8-32	00000	OBD	4
		---x---			
40	No Number	* Component Board Assembly (A308) (see fig. 6-15)			1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	4
	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	4
		---x---			
41	1251-0136	* Connector, Receptacle (XA304, XA305)	28480	1251-0136	2
		(Attaching Parts)			
	2200-0149	* Screw, Machine, PH, No. 4-40, 5/8 in.	00000	OBD	4

Table 6-7. A300 Power Supply and Back Panel Assembly (02116-6124), Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-7-					
	3050-0222	* Washer, Flat, No. 4	00000	OBD	4
	0590-0076	* Nut, Self-Locking, Hexagon, No. 4-40	00000	OBD	4
		---x---			
42	02116-0053	* Connector Bracket	28480	02116-0053	2
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, 6-32, 3/8 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		---x---			
43	02116-0020	* Center Brace	28480	02116-0020	1
		(Attaching Parts)			
44	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	3
45	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	3
		---x---			
46	No Number	* Component Board Assembly (A309)(see fig. 6-17)			1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	3
	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	3
		---x---			
47	02116-2068	* * Mount, Bus Bar	28480	02116-2068	1
		(Attaching Parts)			
48	2510-0063	* * Screw, Machine, FH, No. 8-32, 1-1/2 in.	00000	OBD	2
		---x---			
49	02116-0056	* * Bracket, Diode	28480	02116-0056	1
50	2110-0255	* * Fuse Mounting Bracket	28480	2110-0255	1
51	0160-3043	* Capacitor, Fxd, Cer, 2x0.005uf 20%, 250 VAC (A300C1A, C1B)	56289	29C147A-CDH	1
52	1250-0315	* Connector, Receptacle (A300J1)	28480	1250-0315	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
	2360-0268	* Terminal Lug, No. 6	00000	OBD	1
		---x---			
53	1251-0143	* Connector, Recptacle, Power (A300J2)	74868	32-2907-3	1
		(Attaching Parts)			
	0520-0103	* Screw, Machine, PH, No. 2-56, 3/8 in.	00000	OBD	2
	3050-0098	* Washer, Flat, No. 2	00000	OBD	2
	2190-0045	* Washer, Lock, Split, No. 2	00000	OBD	2
	0610-0001	* Nut, Plain, Hexagon, No. 2-56	00000	OBD	2
		---x---			
54	02116-0027	* Back Panel, Power Supply	28480	02116-0027	1

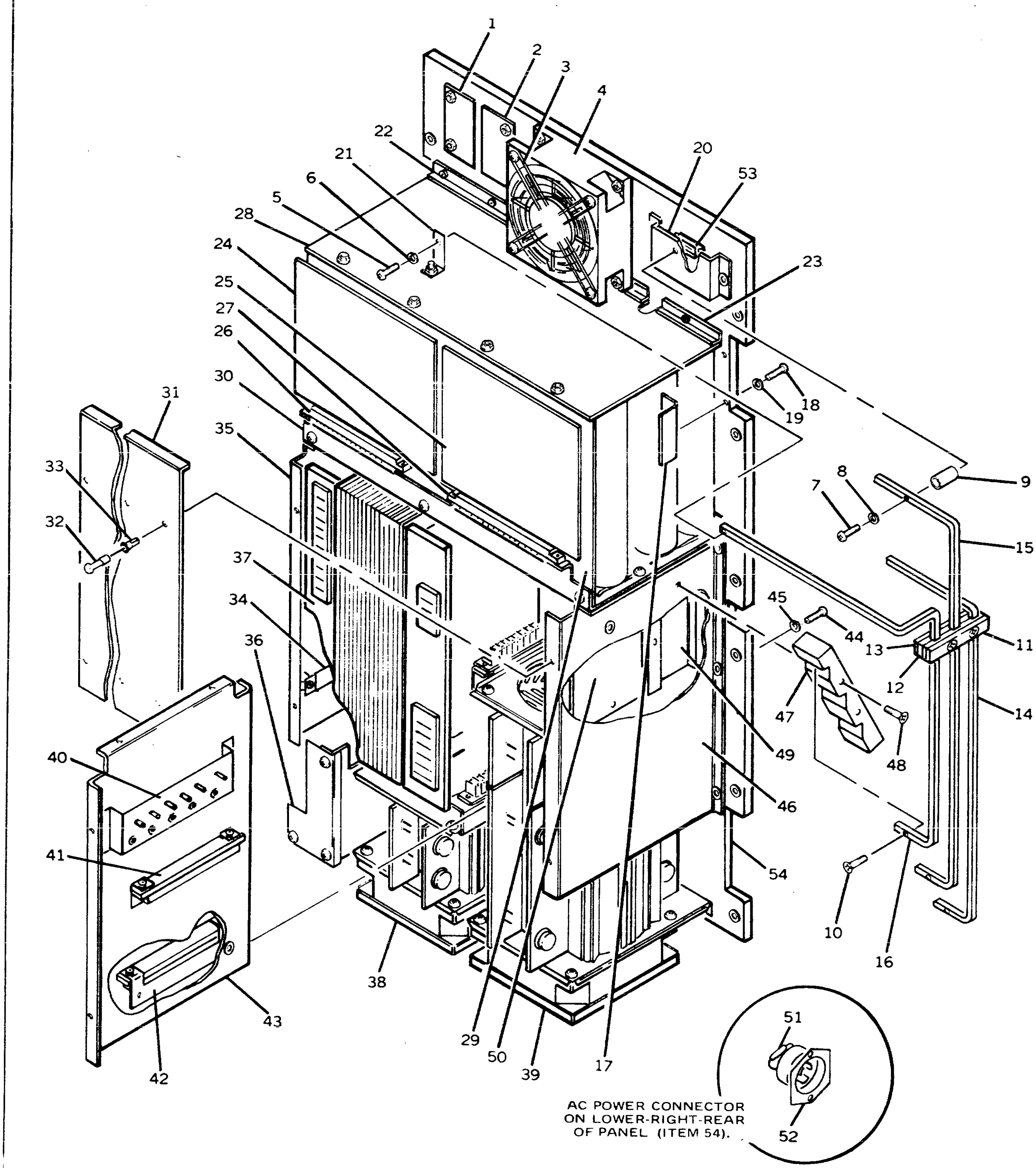

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Figure 6-7. A300 Power Supply Assembly (02116-6124), Exploded View

Table 6-8. A301 Logic Supply Regulator Card (02116-6014), Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-8-	02116-6014	LOGIC SUPPLY REGULATOR CARD (A301) (27, fig. 6-5)	28480	02116-6014	1
1	1853-0001	* Transistor, Si, PNP (Q30, Q31, Q32, Q35, Q36, Q37)	28480	1853-0001	6
2	1205-0033	* Heat Sink	28480	1205-0033	2
3	0160-0163	* Capacitor, Fxd, My, 0.033uf, 10%, 200VDCW (C46, C50, C52)	56289	192P33392-PTS	3
4	1850-0062	* Transistor, Ge (Q33, Q34, Q38, Q43)	01295	GA287	4
5	0757-0924	* Resistor, Fxd, Flm, 1k, 2%, 1/8w (R68, R81, R100)	28480	0757-0924	3
6	0757-0730	* Resistor, Fxd, Flm, 750 ohms, 1%, 1/4w (R64, R78, R98)	28480	0757-0730	3
7	0757-0743	* Resistor, Fxd, Flm, 3.32k, 1%, 1/4w (R80, R82, R99)	28480	0757-0743	3
8	1901-0025	* Diode, Si, 100mA, 1V (CR51, CR53, CR54, CR55, CR56, CR57, CR59, CR61, CR62, CR63)			10
9	0761-0008	* Resistor, Fxd, Met Ox, 510 ohms, 5%, 1w (R62)	28480	0761-0008	1
10	0757-0728	* Resistor, Fxd, Flm, 619 ohms, 1%, 1/4w (R70)	28480	0757-0728	1
11	0180-0064	* Capacitor, Fxd, Elect, 35uf, +100 -10%, 6VDCW (C53, C55, C57)	56289	30D15G006BB4	3
12	2100-1772	* Resistor, Var, WW, 500 ohms, 5%, (R69, R84)	28480	2100-1772	2
13	0757-0244	* Resistor, Fxd, Flm, 499 ohms, 1%, 1/4w (R72, R87, R119)	28480	0757-0244	3
14	0757-0715	* Resistor, Fxd, Flm, 150 ohms, 1%, 1/4w (R71, R86)	28480	0757-0715	2
15	0686-2215	* Resistor, Fxd, Comp, 220 ohms, 5%, 1/2w (R83)	01121	EB2215	1
16	0757-0739	* Resistor, Fxd, Flm, 2.00k, 1%, 1/4w (R89)	28480	0757-0739	1
17	0180-1867	* Capacitor, Fxd, Elect, 1600uf, +75 -10%, 10VDCW (C54)	28480	0180-1867	1
18	0761-0026	* Resistor, Fxd, Met Ox, 220 ohms, 5%, 1w (R88)	28480	0761-0026	1
19	1902-3079	* Diode, Breakdown, Si, 4.53V (CR58)	28480	1902-3079	1
20	0757-0711	* Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/4w (R75, R102)	28480	0757-0711	2
21	0698-3134	* Resistor, Fxd, Flm, 1.33k, 1%, 1/4w (R103)	28480	0698-3134	1
22	1851-0017	* Transistor, Ge, NPN (Q42, Q44)	01295	2N130A	2
23	0757-0814	* Resistor, Fxd, Flm, 511 ohms, 1%, 1/2w (R95)	28480	0757-0814	1
24	0761-0011	* Resistor, Fxd, Met Ox, 3300 ohms, 5%, 1w (R101)	28480	0761-0011	1
25	0757-0158	* Resistor, Fxd, Flm, 619 ohms, 1%, 1/2w (R97)	28480	0757-0158	1
26	1854-0003	* Transistor, Si, NPN (Q39, Q40)	28480	1854-0003	2
27	2100-1770	* Resistor, Var, WW, 100 ohms, 5% (R66, R76, R96)	28480	2100-1770	3
28	1854-0265	* Transistor, Si, NPN (Q41)	28480	1854-0265	1
29	1902-3224	* Diode, Breakdown, 17.8V, 5%, 400 mw (CR64)	28480	1902-3224	1
30	0757-0912	* Resistor, Fxd, Flm, 330 ohms, 2%, 1/8w (R110)	28480	0757-0912	1
31	1902-0184	* Diode, Breakdown, Si, 16.2V, 5% (CR60)	28480	1902-0184	1
32	0180-1714	* Capacitor, Fxd, Elect, 330uf, 10%, 6VDCW (C56)	28480	0180-1714	1

Table 6-8. A301 Logic Supply Regulator Card (02116-6014), Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-8-					
33	0683-5115	* Resistor, Fxd, Comp, 510 ohms, 5%, 1/4w (R117)	01121	CB5115	1
34	1902-0017	* Diode, Breakdown 6.81V, 10%, 400mw (CR65)	28480	1902-0017	1
35	0757-0340	* Resistor, Fxd, Flm, 10.0k, 1%, 1/4w (R115)	28480	0757-0340	1
36	0683-1025	* Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4w (R116)	01121	CB1025	1
37	0757-0338	* Resistor, Fxd, Flm, 1.00k, 1%, 1/4w (R111, R113)	28480	0757-0338	2
38	0757-0705	* Resistor, Fxd, Flm, 47.5 ohms, 1%, 1/4w (R114)	28480	0757-0705	1
39	1820-0954	* Integrated Circuit, CTL (MC1)	07263	SL3457	1
40	0757-0759	* Resistor, Fxd, Flm, 18.2k, 1%, 1/4w (R112)	28480	0757-0759	1
41	0757-0197	* Resistor, Fxd, Flm, 1500 ohms, 1%, 1/2w (R118)	28480	0757-0197	1
42	0150-0121	* Capacitor, Fxd, Cer, 0.1uf, +80 -20%, 50VDCW (C40 thru C43, C45, C47, C48, C49, C51, C59)	56289	5C50BIS-CML	10
43	0757-0808	* Resistor, Fxd, Flm, 301 ohms, 1%, 1/4w (R61)	28480	0757-0808	1
44	0757-0727	* Resistor, Fxd, Flm, 562 ohms, 1%, 1/4w (R77)	28480	0757-0727	1
45	0757-0732	* Resistor, Fxd, Flm, 909 ohms, 1%, 1/4w (R85)	28480	0757-0732	1
46	0757-0821	* Resistor, Fxd, Flm, 1.21k, 1%, 1/2w (R63, R74)	28480	0757-0821	2
47	1902-0071	* Diode, Breakdown, 9.0V, 5% (CR50)	28480	1902-0071	1
48	1902-0556	* Diode, Breakdown, 20.0V, 5%, 1w (CR52)	28480	1902-0556	1
49	0150-0050	* Capacitor, Fxd, Cer, 1000pf, +80 -20%, 1000 VDCW (C44, C58)	56289	C067B102E102-ZE19CDH	2
50	0757-0071	* Resistor, Fxd, Flm, 247.5 ohms, 1%, 1/4w (R65, R67)	28480	0757-0071	2

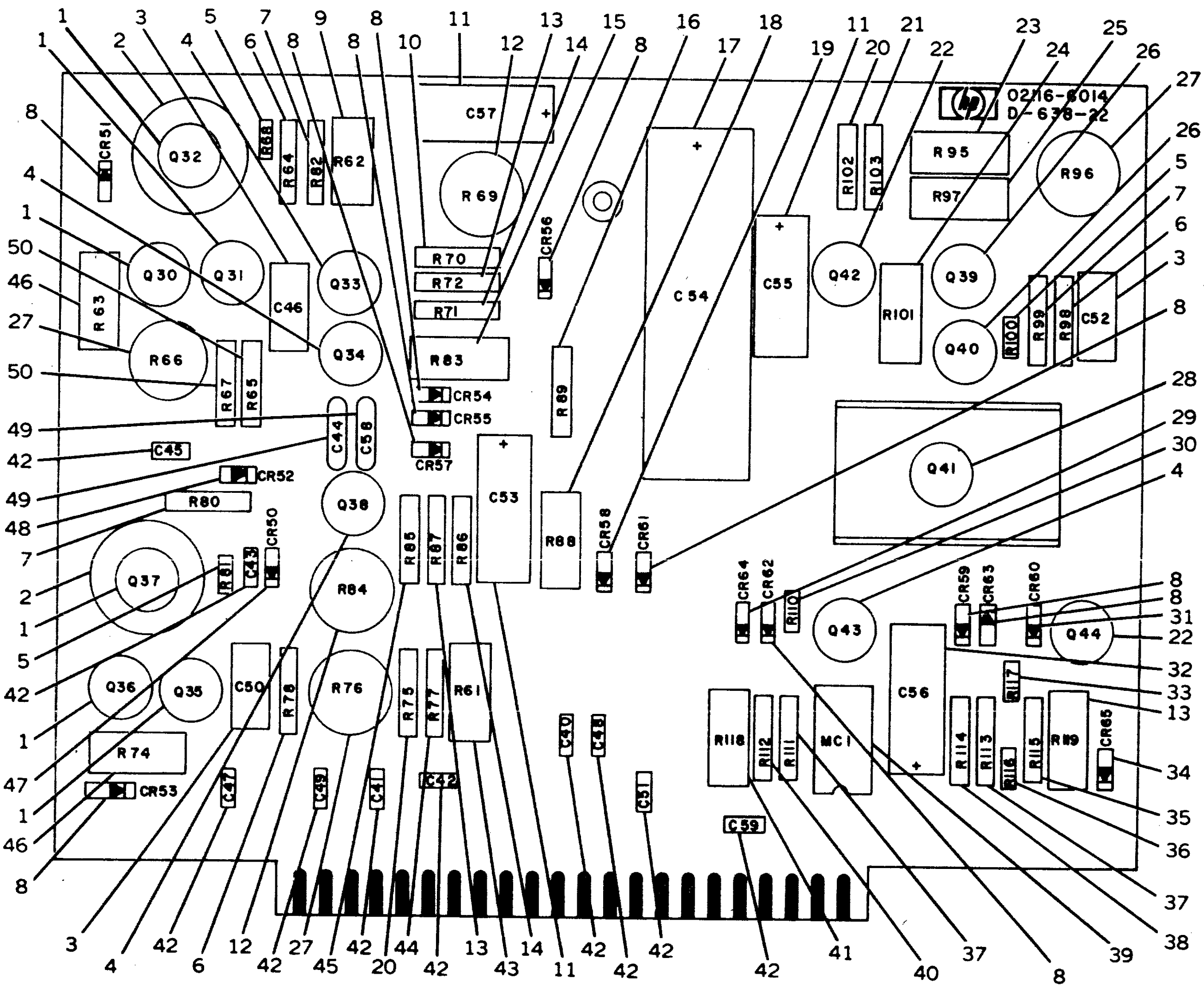

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Figure 6-8. A301 Logic Supply Regulator Card (02116-6014), Parts Identification Diagram

Table 6-9. A302 Memory Supply Regulator Card (02116-6015), Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-9-	02116-6015	MEMORY SUPPLY REGULATOR CARD (A302) (26, fig. 6-6)	28480	02116-6015	1
1	1205-0075	* Heat Sink	28480	1205-0075	1
2	1854-0072	* Transistor, Si, NPN (Q63) (Attaching Parts)	02735	2N3054	1
	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	2
	3050-0225	* Washer, Flat, No. 4	00000	OBD	4
	2190-0108	* Washer, Lock, Split, No. 4	00000	OBD	2
	2260-0001	* Nut, Plain, Hexagon, No. 4-40	00000	OBD	2
		- - - x - - -			
3	0757-0900	* Resistor, Fxd, Flm, 100 ohms, 2%, 1/8w (R133, R147, R162, R178, R179)	28480	0757-0900	5
4	1902-0379	* Diode, Breakdown, 20V, 10%, 1.5w (CR71, CR72, CR74)	28480	1902-0379	3
5	1851-0017	* Transistor, Ge, NPN (Q56, Q64)	01295	2N130A	2
6	1205-0033	* Heat Sink	28480	1205-0033	5
7	1854-0221	* Transistor, Si, NPN (Q54, Q61)	28480	1854-0221	2
8	0757-0931	* Resistor, Fxd, Flm, 2k, 2%, 1/8w (R145, R175)	28480	0757-0931	2
9	0757-0916	* Resistor, Fxd, Flm, 470 ohms, 2%, 1/8w (R180)	28480	0757-0916	1
10	0757-0442	* Resistor, Fxd, Flm, 10.0k, 1%, 1/8w (R149, R163, R181)	28480	0757-0442	3
11	0757-0924	* Resistor, Fxd, Flm, 1k, 2%, 1/8w (R132, R146, R161, R176)	28480	0757-0924	4
12	0150-0121	* Capacitor, Fxd, Cer, 0.1uf, +80 -20%, 50VDCW (C70 thru C81)	56289	SC50BIS-CML	12
13	2100-0741	* Resistor, Var, WW, 5k, 5%, 1w (R170)	28480	2100-0741	1
14	1902-3182	* Diode, Breakdown, Si, 12.1V, 5% (CR73)	28480	1902-3182	1
15	0757-0834	* Resistor, Fxd, Flm, 2.62k, 2%, 1/2w (R129, R174)	28480	0757-0834	2
16	0811-2035	* Resistor, Fxd, WW, 1590 ohms, 1%, 1/4w (R143 R173)	28480	0811-2035	2
17	0770-0003	* Resistor, Fxd, Flm, 3300 ohms, 5%, 4w (R136, R150)	28480	0770-0003	2
18	0811-2040	* Resistor, Fxd, WW, 21.8k, 1%, 1/4w (R171)	28480	0811-2040	1
19	0757-0918	* Resistor, Fxd, Flm, 560 ohms, 2%, 1/8w (R148)	28480	0757-0918	1
20	2100-1429	* Resistor, Var, WW, 2000 ohms, 5%, 1w (R140, R155)	28480	2100-1429	2
21	0757-0196	* Resistor, Fxd, Flm, 6.19k, 1%, 1/2w (R144)	28480	0757-0196	1
22	1854-0022	* Transistor, Si, NPN (Q55, Q62)	07263	S17843	2
23	0811-26110	* Resistor, Fxd, WW, 17.4k, 1%, 1/4w (R141)	28480	0811-2610	1
24	0811-2611	* Resistor, Fxd, WW, 4.99k, 1%, 1/4w (R142)	28480	0811-2611	1
25	0811-2039	* Resistor, Fxd, WW, 8000 ohms, 1%, 1/4w (R156 R172)	28480	0811-2039	2
26	0698-3411	* Resistor, Fxd, Flm, 3.48k, 1%, 1/2w (R159)	28480	0698-3411	1
27	0811-2098	* Resistor, Fxd, WW, 2.75k, 1%, 1/4w (R157)	28480	0811-2098	1
28	1853-0036	* Transistor, Si, PNP (Q50, Q51, Q57, Q58)	04713	SPS-3612	4
29	0811-2037	* Resistor, Fxd, WW, 2400 ohms, 1%, 1/4w (R158)	28480	0811-2037	1

Table 6-9. A302 Memory Supply Regulator Card (02116-6015), Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-9-					
30	0757-0744	* Resistor, Fxd, Flm, 3920 ohms, 1%, 1/4w (R160)	28480	0757-0744	1
31	1850-0062	* Transistor, Ge (Q53, Q60)	01295	GA287	2
32	0757-0920	* Resistor, Fxd, Flm, 680 ohms, 2%, 1/8w (R164)	28480	0757-0920	1
33	1853-0041	* Transistor, Si, PNP (Q52, Q59)	02735	38640	2
34	0770-0002	* Resistor, Fxd, Met Ox, 2400 ohms, 5%, 4w(R182)	28480	0770-0002	1
35	0764-0063	* Resistor, Fxd, Flm, 620 ohms, 5%, 2w (R165)	28480	0764-0063	1
36	0811-2032	* Resistor, Fxd, WW, 880 ohms, 1%, 1/4w (R127)	28480	0811-2032	1
37	0811-2033	* Resistor, Fxd, WW, 1100 ohms, 1%, 1/4w (R126)	28480	0811-2033	1
38	0811-2036	* Resistor, Fxd, WW, 1800 ohms, 1%, 1/4w (R128)	28480	0811-2036	1
39	0757-0914	* Resistor, Fxd, Flm, 390 ohms, 2%, 1/8w (R131)	28480	0757-0914	1
40	0757-1094	* Resistor, Fxd, Flm, 1.47k, 1%, 1/8w (R130)	28480	0757-1094	1
41	1902-0071	* Diode, Breakdown, 9.0V, 5% (CR70)	28480	1902-0071	1
42	0698-3154	* Resistor, Fxd, Flm, 4.22k, 1%, 1/8w (R135)	28480	0698-3154	1
43	0757-0910	* Resistor, Fxd, Flm, 270 ohms, 2%, 1/8w (R134)	28480	0757-0910	1
44	2100-0755	* Resistor, Var, WW, 1k, 5% (R125)	28480	2100-0755	1
45	0764-0062	* Resistor, Fxd, Met Ox, 3.6k, 5%, 2w (R177)	28480	0764-0062	1

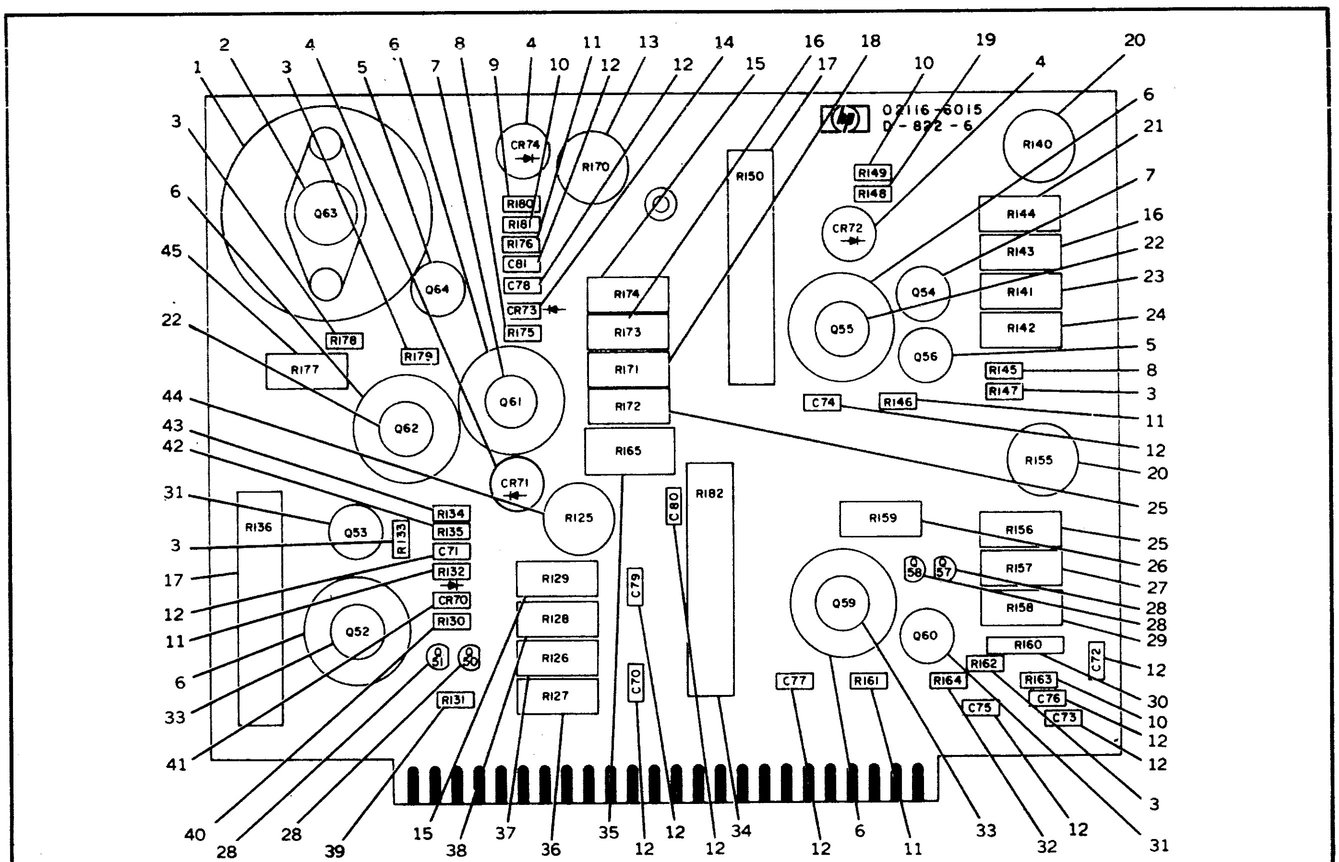

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Figure 6-9. A302 Memory Supply Regulator Card (02116-6015), Parts Identification Diagram

Table 6-10. A306, A307, and A310 Component Board Assemblies, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-10-	No Number	COMPONENT BOARD ASSEMBLY (A306, A307, A310)			3
	No Number	COMPONENT BOARD ASSEMBLY (A307)(1, fig. 6-7)			1
1	5020-0244	* Bracket	28480	5020-0244	2
2	0761-0058	* Resistor, Fxd, Met Ox, 750 ohms, 5%, 1w (R45, R46)	28480	0761-0058	2
3	0812-0099	* Resistor, Fxd, WW, 1k, 5%, 5w (R47)	28480	0812-0099	1
4	0767-0003	* Resistor, Fxd, Met Ox, 1.20k, 5%, 3w (R51)	28480	0767-0003	1
5	0811-1339	* Resistor, Fxd, WW, 500 ohms, 5%, 5w (R57)	28480	0811-1339	1
6	0811-2097	* Resistor, Fxd, WW, 0.25 ohm, 3%, 5w (R48)	28480	0811-2097	1
7	0811-0040	* Resistor, Fxd, WW, 1 ohm, 1%, 5w (R50)	28480	0811-0040	1
8	No Number	* Bus Wire, No. 18	00000	OBD	AR
9	5080-1543	* Component Board	28480	5080-1543	1
	No Number	COMPONENT BOARD ASSEMBLY (A306)(2, fig. 6-7)			1
10	5020-0244	* Bracket	28480	5020-0244	2
11	0811-2139	* Resistor, Fxd, WW, 2.2k, 5%, 3w (R40, R54)	28480	0811-2139	2
12	0761-0005	* Resistor, Fxd, Met Ox, 2200 ohms, 5%, 1w (R49)	28480	0761-0005	1
13	0761-0038	* Resistor, Fxd, Met Ox, 5600 ohms, 5%, 1w (R39)	28480	0761-0038	1
14	0811-0040	* Resistor, Fxd, WW, 1 ohm, 1%, 5w (R55, R56)	28480	0811-0040	2
15	0813-0029	* Resistor, Fxd, WW, 1 ohm, 3%, 3w (R52, R53)	28480	0813-0029	2
16	0811-2097	* Resistor, Fxd, WW, 0.25 ohm, 3%, 5w (R16)	28480	0811-2097	1
17	5080-1543	* Component Board	28480	5020-1543	1
	No Number	COMPONENT BOARD ASSEMBLY (A310)(20, fig. 6-7)			1
18	0811-2078	* Resistor, Fxd, WW, 0.15 ohm, 3%, 12w (R8 thru R15)	28480	0811-2078	8
19	0811-2648	* Resistor, Fxd, WW, 5 ohms, 3%, 12.5w (R23) (Attaching Parts for items 18 and 19)	28480	0811-2648	1
	0520-0065	* Screw, Machine, PH, No. 2-56, 1/4 in.	00000	OBD	9
	2190-0045	* Washer, Lock, Split, No. 2	00000	OBD	9
	0610-0001	* Nut, Plain, Hexagon, No. 2-56 --- x ---	00000	OBD	4
20	02116-0091	* Bracket, Resistor	28480	02116-0091	1

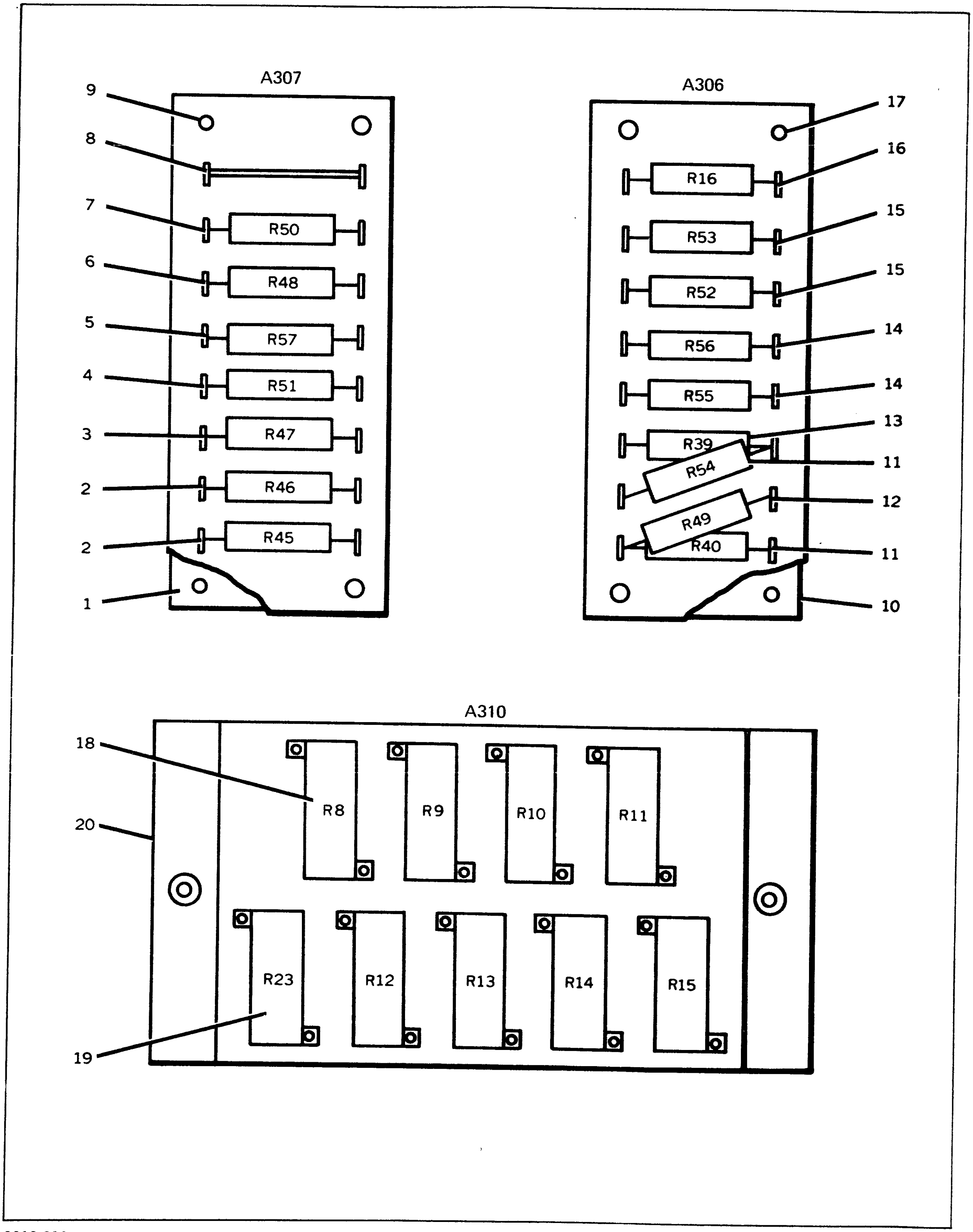

Figure 6-10. A306, A307, and A310 Component Board Assemblies, Parts Identification Diagram

Table 6-11. A303 Capacitor Board Assembly, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-11-	No Number	CAPACITOR BOARD ASSEMBLY (A303)(28, fig. 6-7)			1
1	1901-0416	* Diode, Si, 200 PIV, 3A (CR11 thru CR18, CR27 thru CR34)	28480	1901-0416	16
2	0180-1871	* Capacitor, Fxd, Elect, 12,000μf, +75 -10%, 25 VDCW (C19)	28480	0180-1871	1
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	1
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	1
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
	2680-0103	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	1
		- - - x - - -			
3	0180-1875	* Capacitor, Fxd, Elect, 270.000μf, +75 -10%, 3VDCW (C14, C15, C17, C18)	56289	36D274G003-DF2A-DQB	4
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	4
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	4
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	4
	2680-0103	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
		- - - x - - -			
4	0811-2138	* Resistor, Fxd, WW, 120 ohms, 5%, 5w (R26, R27)	28480	0811-2138	2
5	0180-1870	* Capacitor, Fxd, Elect, 10,000μf, +75 -10%, 20VDCW (C9, C10)	28480	0180-1870	2
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	2
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	2
	2680-0103	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	2
		- - - x - - -			
6	0180-1874	* Capacitor, Fxd, Elect, 51,000μf, +75 -10%, 7.5VDCW (C8, C16)	28480	0180-1874	2
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	2
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	2
	2680-0103	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	2
		- - - x - - -			
7	0180-1869	* Capacitor, Fxd, Elect, 8700μf, +75 - 10%, 20VDCW (C13)	28480	0180-1869	1
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	1
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	1
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
	2680-0103	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	1
		- - - x - - -			
8	0764-0017	* Resistor, Fxd, Met Ox, 1.6k, 5%, 2w (R25)	28480	0764-0017	1
9	0180-1866	* Capacitor, Fxd, Elect, 500μf, +75 -10%, 75VDCW (C24, C25)	56289	39D507G75-HL4-DSB	2
10	0686-1235	* Resistor, Fxd, Comp, 12k, 5%, 1/2w (R36, R37)	01121	EB1235	2
11	1901-0191	* Diode, Si, 0.75A, 100 PIV (CR19 thru CR26)	04713	SR1358-2	8

Table 6-11. A303 Capacitor Board Assembly, Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-11- 12	0180-1873	* Capacitor, Fxd, Elect, 100,000μf, +75 -10%, 20VDCW (C21, C22)	28480	0180-1873	2
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	2
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	2
	2680-0103	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	2
		- - - x - - -			
13	0180-1977	* Capacitor, Fxd, Elect, 5900μf, +75 -10%, 50VDCW (C20, C23)	28480	0180-1977	2
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	2
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	2
	2680-0103	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	2
		- - - x - - -			
14	0812-0099	* Resistor, Fxd, WW, 1k, 5%, 5w (R30, R35)	28480	0812-0099	2
15	0811-1857	* Resistor, Fxd, WW, 400, 5%, 5w (R31, R32)	28480	0811-1857	2
16	0813-0038	* Resistor, Fxd, WW, 0.5 ohm, 10%, 5w (R4, R29, R33, R34)	28480	0813-0038	4
17	02116-0067	* Bus Bar	28480	02116-0067	1
18	0180-1978	* Capacitor, Fxd, Elect, 880μf, +50 -10%, 75VDCW (C26)	28480	0180-1978	1
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	1
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	1
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
	2680-0103	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	1
		- - - x - - -			
19	0812-0050	* Resistor, Fxd, WW, 3k, 5%, 5w (R38)	28480	0812-0050	1
20	0180-1977	* Capacitor, Fxd, Elect, 5900μf, +75 -10%, 50VDCW (C20, C23)	28480	0180-1977	2
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	2
	2190-0034	* Washer, Lock, Split, No. 10	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	2
	2680-0103	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	2
		- - - x - - -			
21	02116-0068	* Bus Bar	28480	02116-0068	1
22	0811-1858	* Resistor, Fxd, WW, 500 ohms, 5%, 5w (R28)	28480	0811-1858	1
23	02116-0069	* Bus Bar	28480	02116-0069	1
24	02116-8038	* PC Board, Blank	28480	02116-8038	1

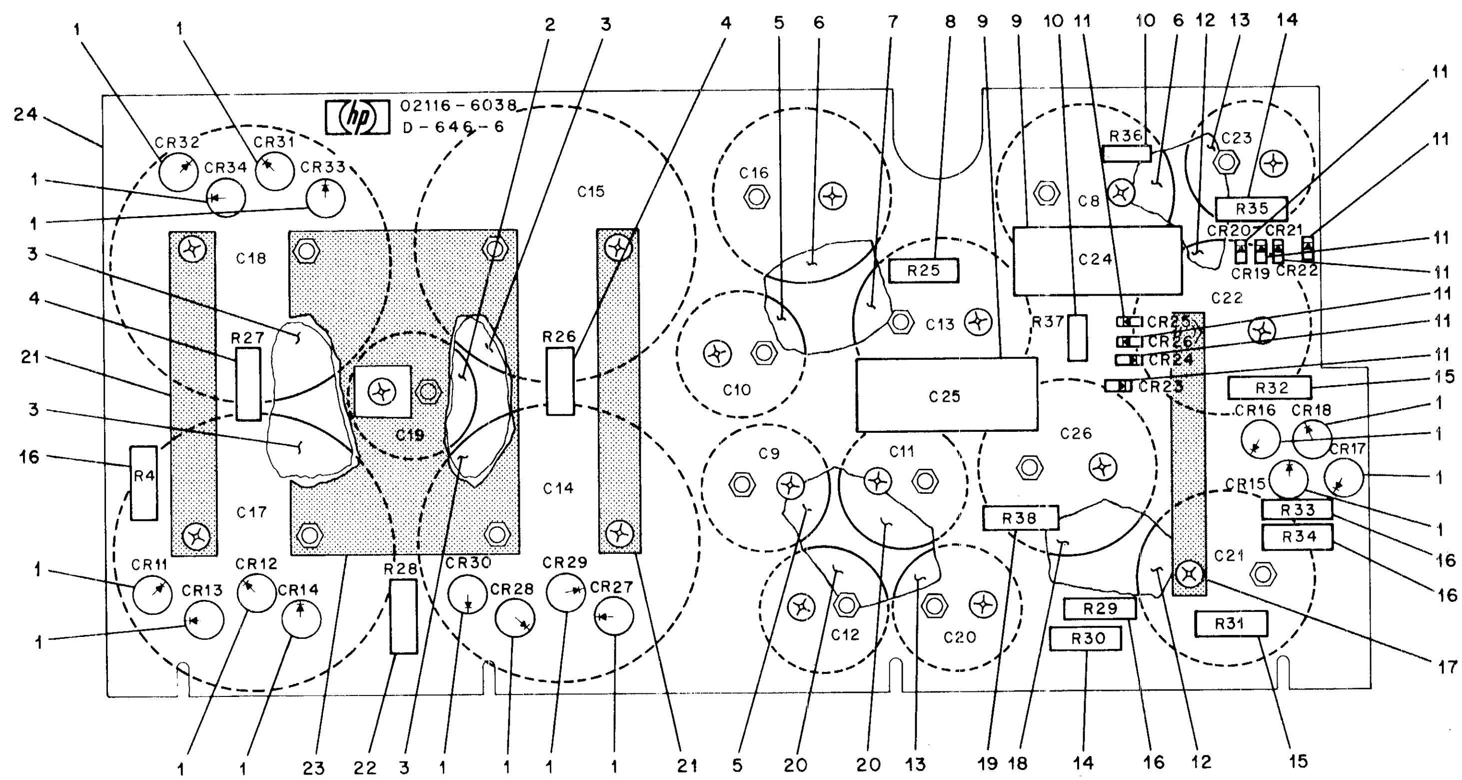

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Figure 6-11. A303 Capacitor Board Assembly, Parts Identification Diagram

Table 6-12. A312 AC Input Section, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-12-	No Number	AC INPUT SECTION (36, fig. 6-7)			1
1	02116-0078	* Shield, Filter	28480	02116-0078	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	3
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	1
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
2	0160-3043	* Capacitor, Fxd, Cer, 2x0.005uf, 20%, 250 VACW (C2A, C2B)	56289	29C147A-CHD	1
3	9100-1834	* Line Filter, 20 A, AC (FL1)	28480	9100-1834	1
4	5000-5722	* Bracket, Mounting, Filter	28480	5000-5722	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	0000	OBD	4
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	4
		- - - x - - -			
5	1901-0045	* Diode, Si, 0.75A, 100PIV (CR10)	04713	SR1358-7	1
6	0490-0372	* Relay, 50 ohm coil (K1)	04009	WHU012D5-503	1
		(Attaching Parts)			
	2580-0003	* Nut, Assembled Washer, No. 8-32	00000	OBD	1
		- - - x - - -			
7	02116-0048	* Cover, AC Housing	28480	02116-0048	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	3
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	3
	3050-0228	* Washer, Flat, No. 6	00000	OBD	3
		- - - x - - -			
8	2110-0025	* Fuse, 15A, S-B (F1)	00000	OBD	1
9	1400-0084	* Fuseholder (XF1)	00000	OBD	1
10	02116-0024	* Housing, AC Input	28480	02116-0024	1

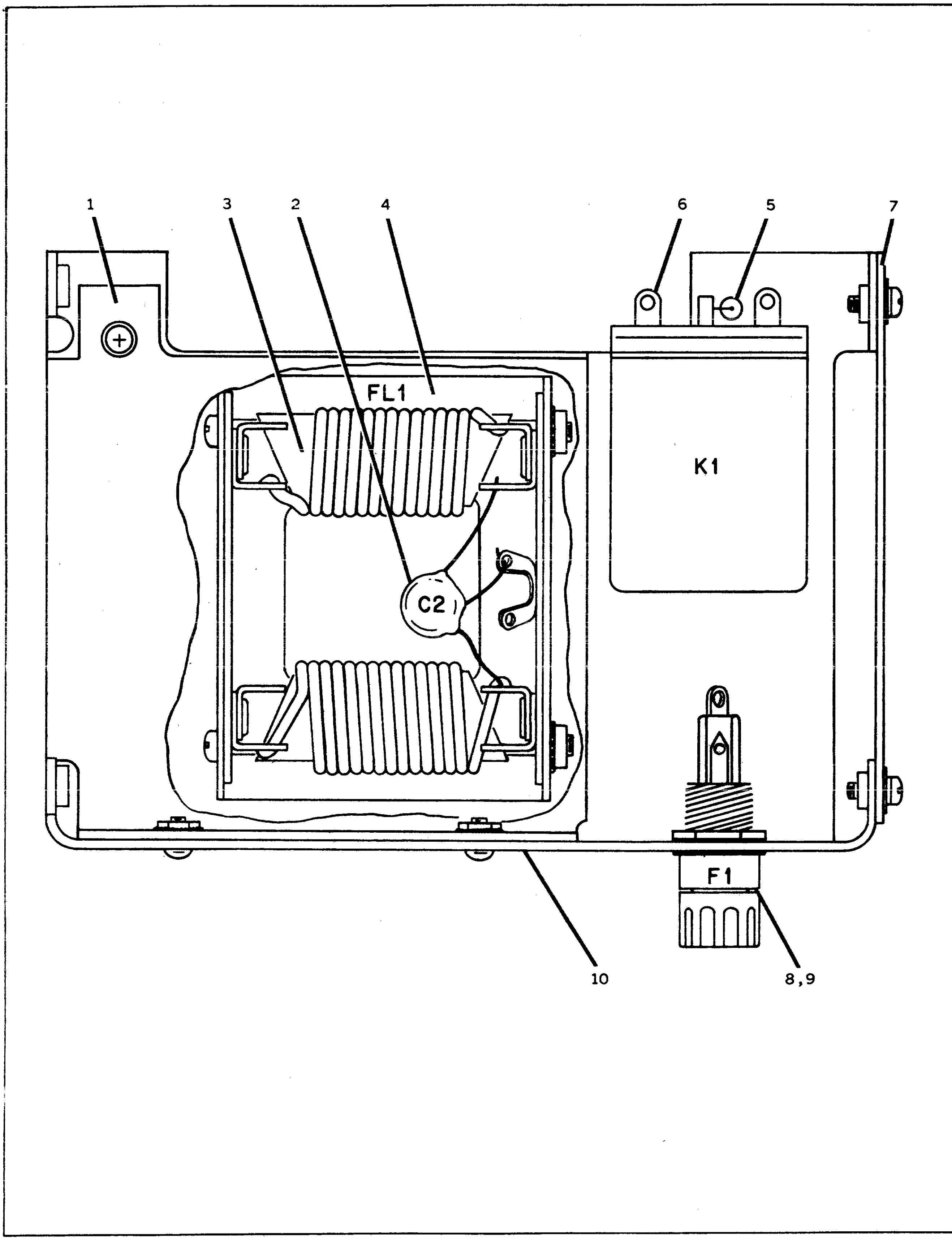

Figure 6-12. A312 AC Input Section, Parts Identification Diagram

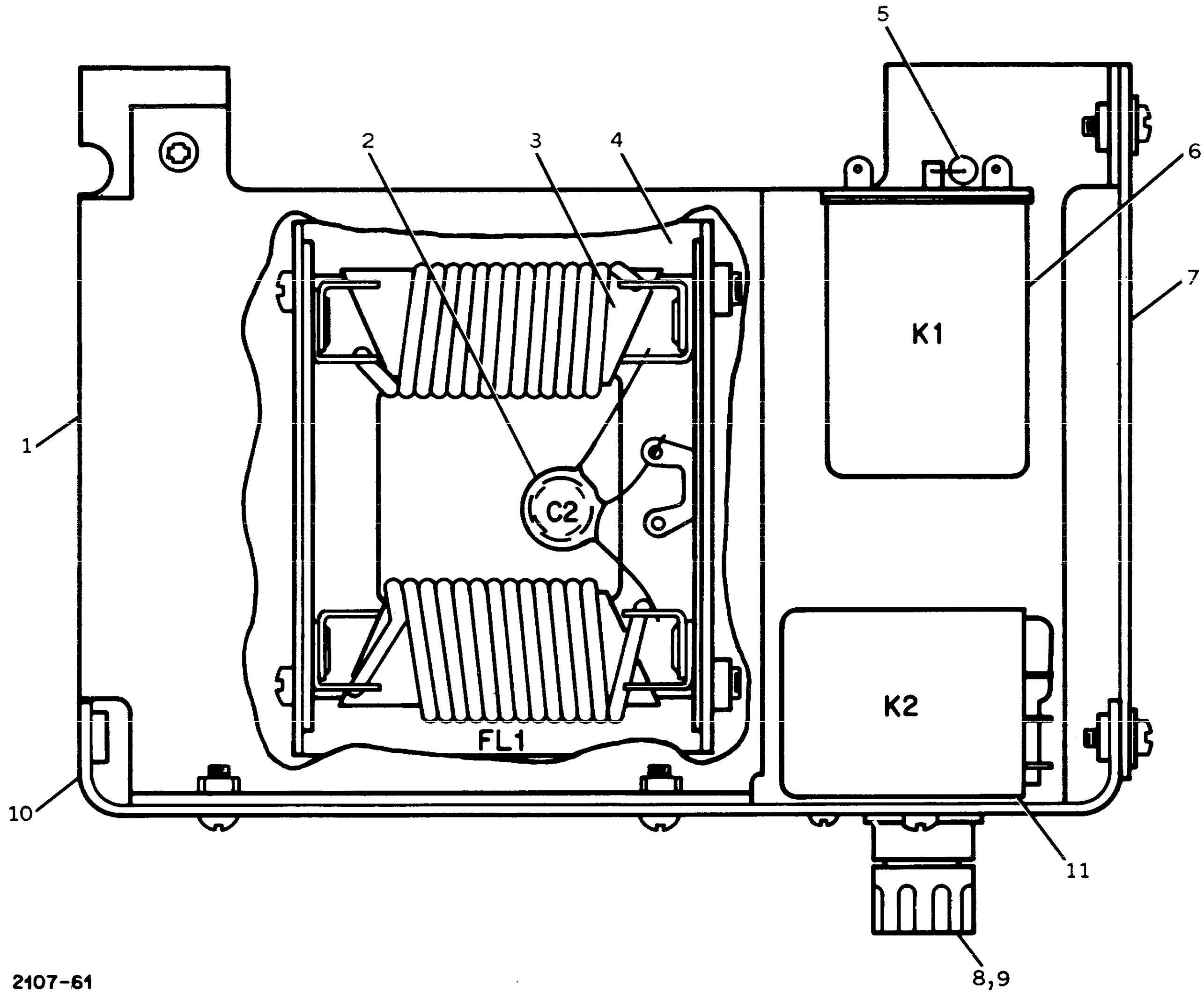

Figure 6-12A. A312 AC Input Section, Parts Identification Diagram for Computers with Serial Number Prefix 959- and 977-

Table 6-13. A311 Transformer Assembly, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-13-	No Number	TRANSFORMER ASSEMBLY (A311)(37, fig. 6-7)			1
1	0360-1279	* Shorting Strip	28480	0360-1279	2
2	0360-1256	* Terminal Board (TB1)	28480	0360-1256	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	4
		- - - x - - -			
3	2110-0044	* Fuse, 3A, S-B (F3, F8)	00000	OBD	2
4	2110-0023	* Fuse, 6.25A, S-B (F4 thru F7, F9)	00000	OBD	5
5	2110-0014	* Fuse, 4A, S-B (F10)	00000	OBD	1
6	2110-0013	* Fuse, 3.2A, S-B (F2)	00000	OBD	1
7	2110-0293	* Fuseholder Clip			18
8	0360-1254	* Terminal Board (TB2, TB3, TB5, TB6)	28480	0360-1254	4
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	8
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	8
		- - - x - - -			
9	0360-1130	* Terminal Board (TB4)	28480	0360-1130	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	4
		- - - x - - -			
10	02116-0060	* Bracket, Terminal Mounting, Right	28480	02116-0060	1
11	02116-0059	* Bracket, Terminal Mounting, Left	28480	02116-0059	1
		(Attaching Parts for items 10 and 11)			
	0570-0070	* Bolt, Machine, Hexagon Head, 1/4-20, 3-1/2 in.	00000	OBD	2
	3050-0234	* Washer, Flat, 1/4 in. I.D.	00000	OBD	6
	2190-0032	* Washer, Lock, Split, 1/4 in. I.D.	00000	OBD	2
	2950-0004	* Nut, Plain, Hexagon, 1/4-20	00000	OBD	2
		- - - x - - -			
12	02116-0002	* Bracket, Transformer	28480	02116-0002	4
		(Attaching Parts)			
	0570-1003	* Bolt, Machine, Hexagon Head, 1/4-20, 3-1/4 in.	00000	OBD	2
	3050-0234	* Washer, Flat, 1/4 in. I.D.	00000	OBD	2
	2190-0032	* Washer, Lock, Split, 1/4 in. I. D.	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, 1/4 in. I.D.	00000	OBD	2
		- - - x - - -			
13	02116-0063	* Bracket, Terminal Board	28480	02116-0063	4
		(Attaching Parts)			
	2680-0104	* Screw, Machine, FH, No. 10-32, 1/2 in.	00000	OBD	4
	2190-0074	* Washer, Lock, Split, No. 10	00000	OBD	4
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	4
		- - - x - - -			
14	2680-0108	* Screw, Machine, FH, No. 10-32, 3/4 in.	00000	OBD	5
15	3050-0226	* Washer, Flat, No. 10	00000	OBD	5
16	2190-0032	* Washer, Lock, Split, No. 10	00000	OBD	10
17	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	10
18	02116-0064	* Terminal Board (TB7)	28480	02116-0064	1
19	9100-1219	* Transformer, Power	28480	9100-1219	1

Table 6-13A. A311 Transformer Assembly, Replaceable Parts for Computers with Serial Number Prefix 959-and 977-

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-13A	No Number	TRANSFORMER ASSEMBLY (A311) (37, fig. 6-7)			1
1	0360-1279	* Shorting Strip	28480	0360-1279	2
2	0360-1256	* Terminal Board (TB1)	28480	0360-1256	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	4
		– – – x – – –			
3	2110-0044	* Fuse, 3A, S-B (F3, F8)	00000	OBD	2
4	2110-0023	* Fuse, 6.25A, S-B (F4 thru F7, F9)	00000	OBD	5
5	2110-0014	* Fuse, 4A, S-B (F10)	00000	OBD	1
6	2110-0013	* Fuse, 3.2A, S-B (F2)	00000	OBD	1
7	2110-0293	* Fuseholder Clip			18
8	0360-1254	* Terminal Board (TB2, TB3, TB5, TB6)	28480	0360-1254	4
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	8
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	8
		– – – x – – –			
9	0360-1130	* Terminal Board (TB4)	28480	0360-1130	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	4
		– – – x – – –			
10	0811-2735	* Resistor, Fxd, WW, 2500 ohms, 3%, 10W, (R20)	28480	0811-2735	1
11	0360-1589	* Terminal Board (TB8)	28480	0360-1589	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	3050-0228	* Washer, Flat, No. 6	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	2
		– – – x – – –			
12	02116-0060	* Bracket, Terminal Mounting, Right	28480	02116-0060	1
13	02116-0059	* Bracket, Terminal Mounting, Left	28480	02116-0059	1
		(Attaching Parts for items 12 and 13)			
	0570-0070	* Bolt, Machine, Hexagon Head, 1/4-20, 3-1/2 in.	00000	OBD	2
	3050-0234	* Washer, Flat, 1/4 in. I.D.	00000	OBD	6
	2190-0032	* Washer, Lock, split, 1/4 in. I.D.	00000	OBD	2
	2950-0004	* Nut, Plain, Hexagon, 1/4-20	00000	OBD	2
		– – – x – – –			
14	02116-0002	* Bracket, Transformer	28480	02116-0002	4
		(Attaching Parts)			
	0570-1003	* Bolt, Machine, Hexagon Head, 1/4-20, 3-1/4 in.	00000	OBD	2
	3050-0234	* Washer, Flat, 1/4 in. I.D.	00000	OBD	2
	2190-0032	* Washer, Lock, split, 1/4 in. I.D.	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, 1/4 in. I.D.	00000	OBD	2
		– – – x – – –			
15	02116-0063	* Bracket, Terminal Board	28480	02116-0063	4
		(Attaching Parts)			
	2680-0104	* Screw, Machine, FH, No. 10-32, 1/2 in.	00000	OBD	4
	2190-0074	* Washer, Lock, split, No. 10	00000	OBD	4
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	4
		– – – x – – –			
16	2680-0108	* Screw, Machine, FH, No. 10-32, 3/4 in.	00000	OBD	5
17	3050-0226	* Washer, Flat, No. 10	00000	OBD	5
18	2190-0032	* Washer, Lock, split, No. 10	00000	OBD	10
19	2740-0002	* Nut, Plain, Hexagon, No. 10	00000	OBD	10
20	02116-0064	* Terminal Board (TB7)	28480	02116-0064	1
21	9100-1219	* Transformer, Power	28480	9100-1219	1

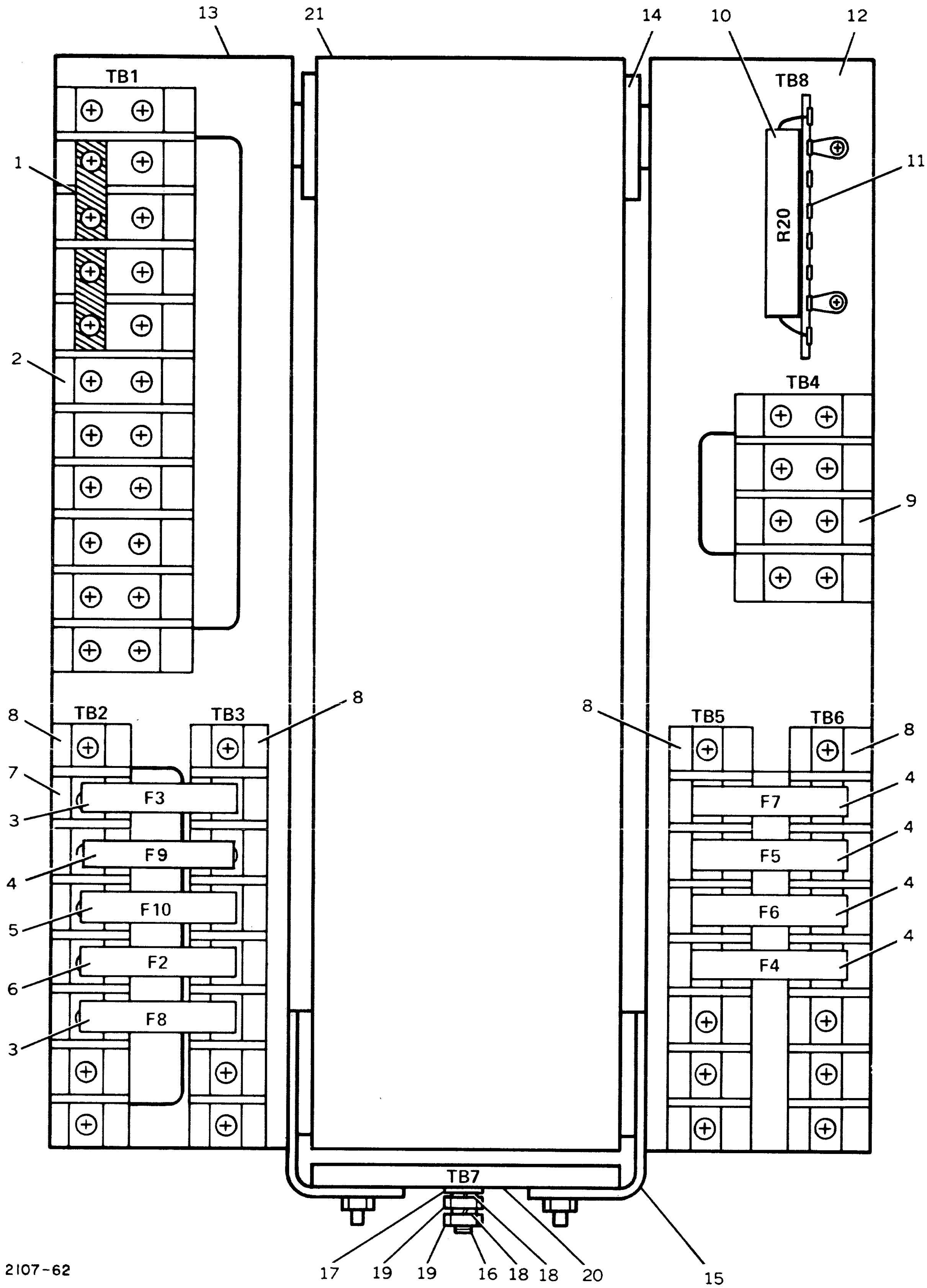

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Figure 6-13A. A311 Transformer Assembly, Parts Identification Diagram for Computers with Serial Number Prefix 959- and 977-

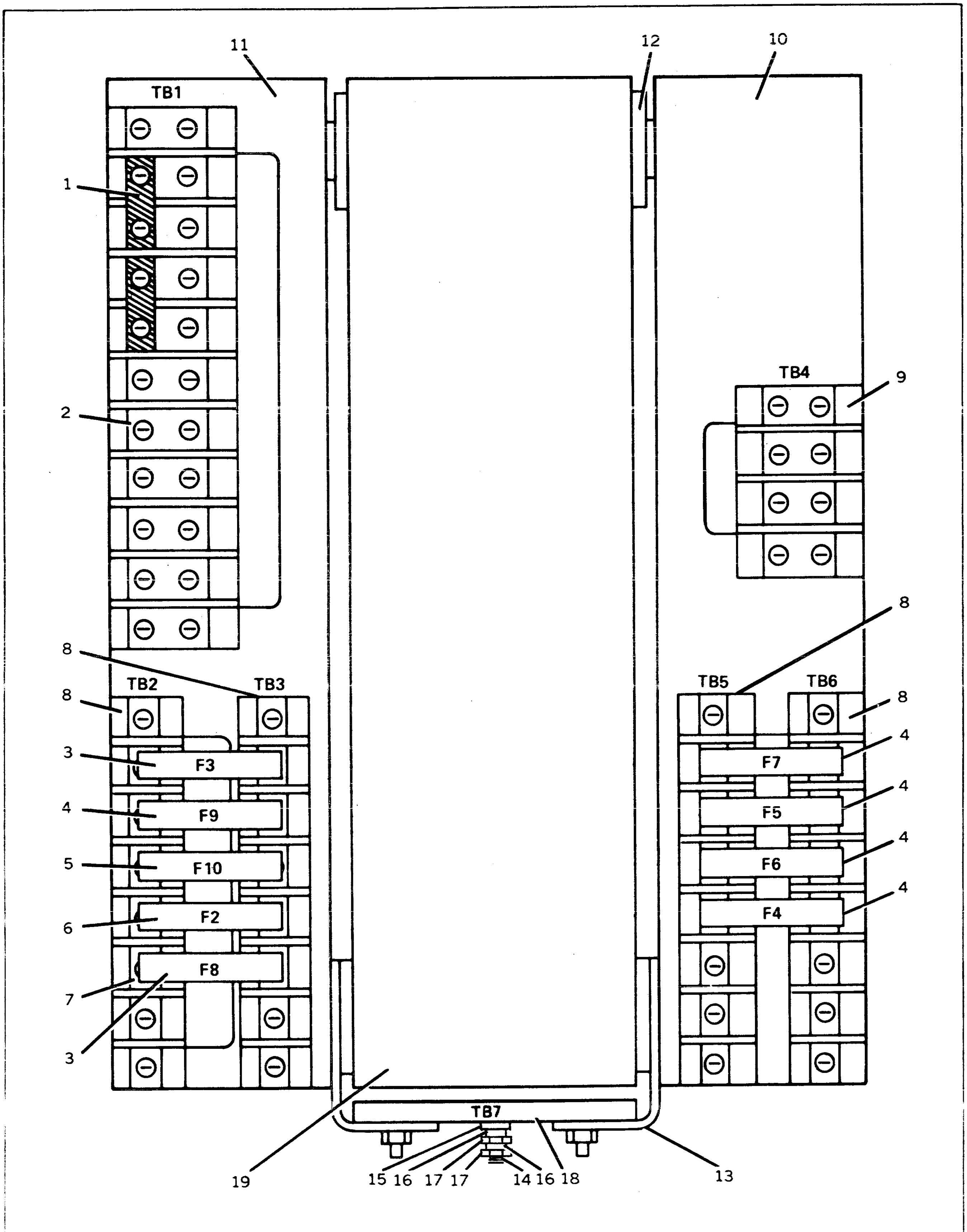

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Figure 6-13. A311 Transformer Assembly, Parts Identification Diagram

Table 6-14. A305 Small Heat Sink Assembly, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-14-	No Number	SMALL HEAT SINK ASSEMBLY (A305)(38, fig. 6-7)			1
1	1251-0137	* Connector, Receptacle, 32 contacts (P1)	71785	26-4200-325	1
		(Attaching Parts)			
	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	2
	0590-0076	* Nut, Self-Locking Hexagon, No. 4-40	00000	OBD	2
		- - - x - - -			
2	02116-0054	* Bracket, Connector	28480	02116-0054	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
3	1850-0098	* Transistor, Ge, PNP (Q13, Q17)	28480	1850-0098	2
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	0360-0268	* Terminal Lug, No. 6	00000	OBD	4
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			
4	3103-0004	* Thermoswitch, 115V, 2A (S1)	28480	3103-0004	1
5	02116-0033	* Bracket, Thermoswitch	28480	02116-0033	1
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	2
	2190-0006	* Washer, Lock, Split, No. 6	00000	OBD	2
		- - - x - - -			
6	1853-0063	* Transistor, Si, NPN (Q12, Q16)	04713	MJ2268	2
		(Attaching Parts)			
	2360-0268	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			
7	1854-0264	* Transistor, Si, NPN (Q18)	04713	2N3715	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
8	1854-0264	* Transistor, Si, NPN (Q14, Q19)	04713	2N3715	2
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	0360-0268	* Terminal Lug, No. 6	00000	OBD	4
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			
9	02116-0057	* Filter, Air	28480	02116-0057	1
10	3160-0072	* Fan Assembly, 115V, 60Hz (B3)	28480	3160-0027	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			

Table 6-14. A305 Small Heat Sink Assembly, Replaceable Parts (Continued)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-14-					
11	1850-0098	* Transistor, Ge, PNP (Q15)	28480	1850-0098	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	2
	0360-0268	* Terminal Lug, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	0000	OBD	2
		- - - x - - -			
12	1205-0067	* Heat Sink	28480	1205-0067	1

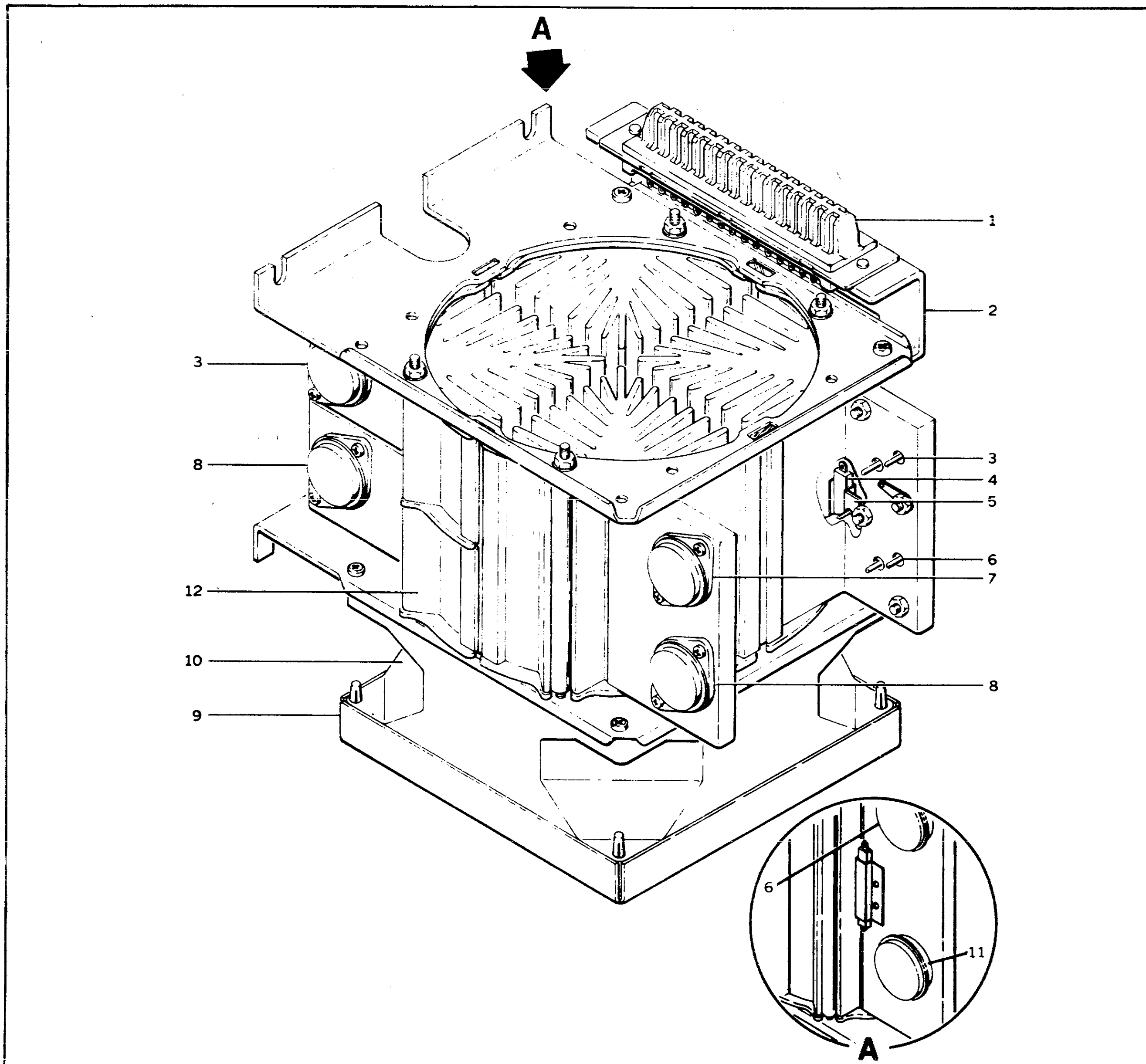

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Figure 6-14. A305 Small Heat Sink Assembly, Parts Identification Diagram

Table 6-15. A308 Component Board Assembly, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-15-	No Number	COMPONENT BOARD ASSEMBLY (A308)(40, fig. 6-7)			1
1	0815-0005	* Resistor, Fxd, WW, 62 ohms, 5%, 10w (R19)	28480	0815-0005	1
2	0811-2107	* Resistor, Fxd, WW, 75 ohms, 5%, 10w (R17, R18)	28480	0811-2107	2
		(Attaching Parts for items 1 and 2)			
3	2420-0001	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	3
4	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	3
5	3050-0228	* Washer, Flat, No. 6	00000	OBD	6
6	3050-0247	* Washer, Nonmetallic, No. 6	00000	OBD	9
7	2390-0014	* Screw, Machine, PH, No. 6-32, 2-1/4 in.	00000	OBD	3
		- - - x - - -			
8	0811-2509	* Resistor, Fxd, WW, 0.5 ohm, 5%, 25w (R7)	28480	0811-2509	1
9	0811-2510	* Resistor, Fxd, WW, 0.1 ohm, 5%, 25w (R5, R6)	28480	0811-2510	2
		(Attaching Parts for items 8 and 9)			
10	2580-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	3
11	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	3
12	3050-0139	* Washer, Flat, No. 8	00000	OBD	6
13	3050-0239	* Washer, Nonmetallic, No. 8	00000	OBD	9
14	2515-0016	* Screw, Machine, PH, No. 8-32, 2-1/2 in.	00000	OBD	3
		- - - x - - -			
15	1902-1215	* Diode, Breakdown, 20V, 2%, 10w (CR9)	04713	1N2984	1
		(Attaching Parts)			
16	2740-0002	* Nut, Plain, Hexagon, No. 10	00000	OBD	1
17	0360-0270	* Terminal Lug, No. 10	00000	OBD	1
		- - - x - - -			
18	1901-0476	* Diode, Si, 100 PIV, 12A (CR5 thru CR8)	04713	MR1121	4
		(Attaching Parts)			
19	2740-0002	* Nut, Plain, Hexagon, No. 10	00000	OBD	4
20	0360-0270	* Terminal Lug, No. 10	00000	OBD	4
21	3050-0226	* Washer, Flat, No. 10	00000	OBD	4
		- - - x - - -			
22	0757-0156	* Resistor, Fxd, Flm, 1.5 Megohm, 1%, 1/2w (R2, R3)	28480	0757-0156	2
23	0360-0279	* Standoff, No. 4-40, internal threaded base	28480	0360-0279	2
		(Attaching Parts)			
	2200-0139	* Screw, Machine, PH, No. 4-40, 1/4 in.	00000	OBD	2
	2190-0108	* Washer, Lock, Split, No. 4	00000	OBD	2
		- - - x - - -			

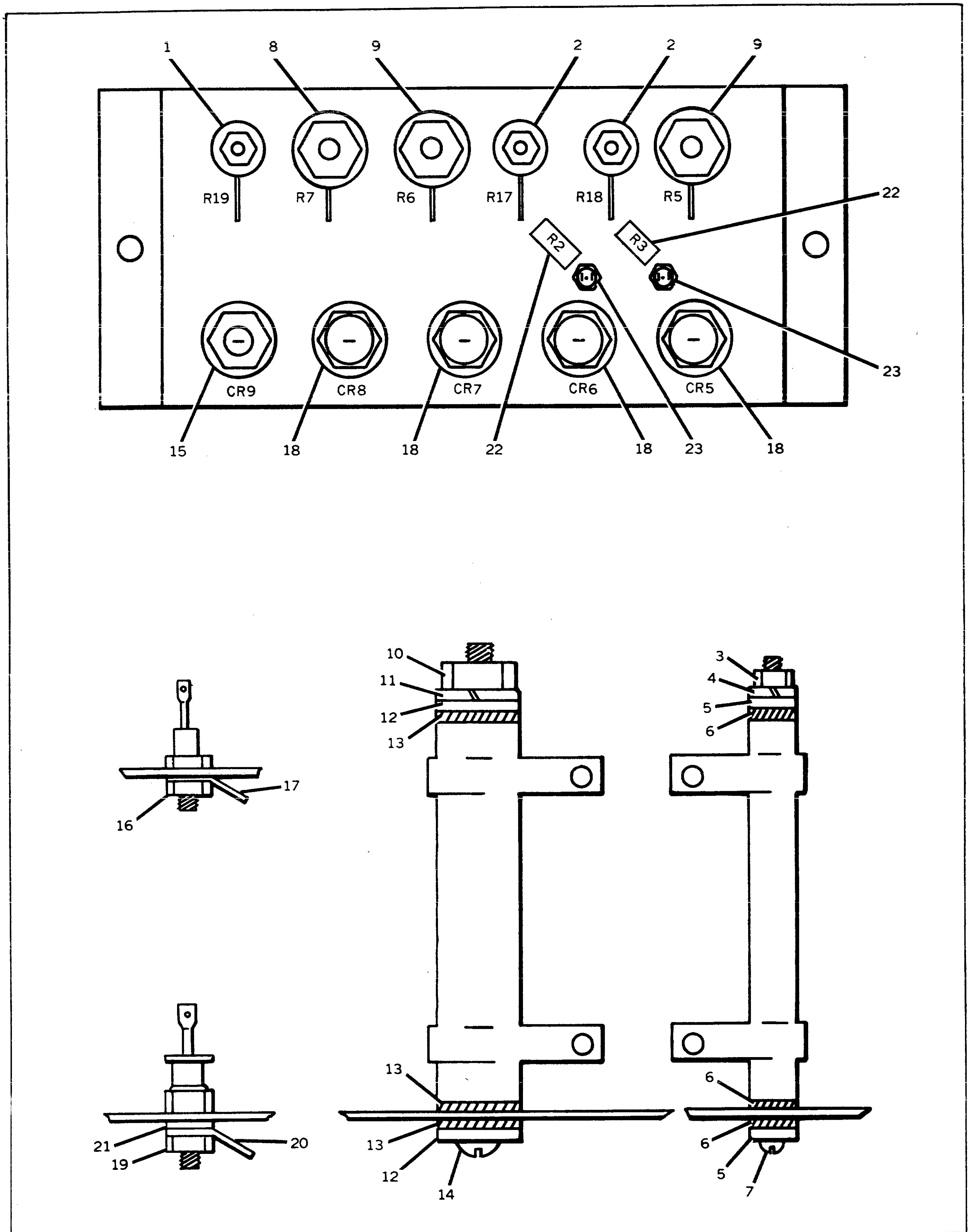

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Figure 6-15. A308 Component Board Assembly, Parts Identification Diagram

Table 6-16. A304 Large Heat Sink Assembly, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-16-	No Number	LARGE HEAT SINK ASSEMBLY (A304)(39, fig. 6-7)			1
1	1251-0137	* Connector, Receptacle, 32 contacts (P1)	71785	26-4200-32S	1
		(Attaching Parts)			
	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	2
	0590-0076	* Nut, Self-Locking, Hexagon, No. 4-40:n.	00000	OBD	2
		- - - x - - -			
2	02116-0054	* Bracket, Connector	28480	02116-0054	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
3	1850-0098	* Transistor, Ge, PNP (Q10, Q11)	28480	1850-0098	2
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	0360-0268	* Terminal Lug, No. 6	00000	OBD	4
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			
4	1854-0264	* Transistor, Si, NPN (Q9)	04713	2N3715	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	2
	0360-0268	* Terminal Lug, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
5	1850-0198	* Transistor, Ge, PNP (Q1, Q3, Q6, Q7)	04713	2N2156	4
		(Attaching Parts)			
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	0360-0268	* Terminal Lug, No. 6	00000	OBD	4
		- - - x - - -			
6	1850-0198	* Transistor, Ge, PNP (Q2, Q4, Q5, Q8)	04713	2N2156	4
		(Attaching Parts)			
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			
7	3103-0004	* Thermoswitch, 115V, 2A (S1)	28480	3103-0004	1
8	02116-0033	* Bracket, Thermoswitch	28480	02116-0033	1
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	2
	2190-0006	* Washer, Lock, Split, No. 6	00000	OBD	2
		- - - x - - -			
9	02116-0057	* Filter, Air	28480	02116-0057	1
10	3160-0072	* Fan Assembly, 115V, 60Hz (B2)	28480	3160-0072	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		- - - x - - -			
11	1205-0006	* Heat Sink	28480	1205-0006	1

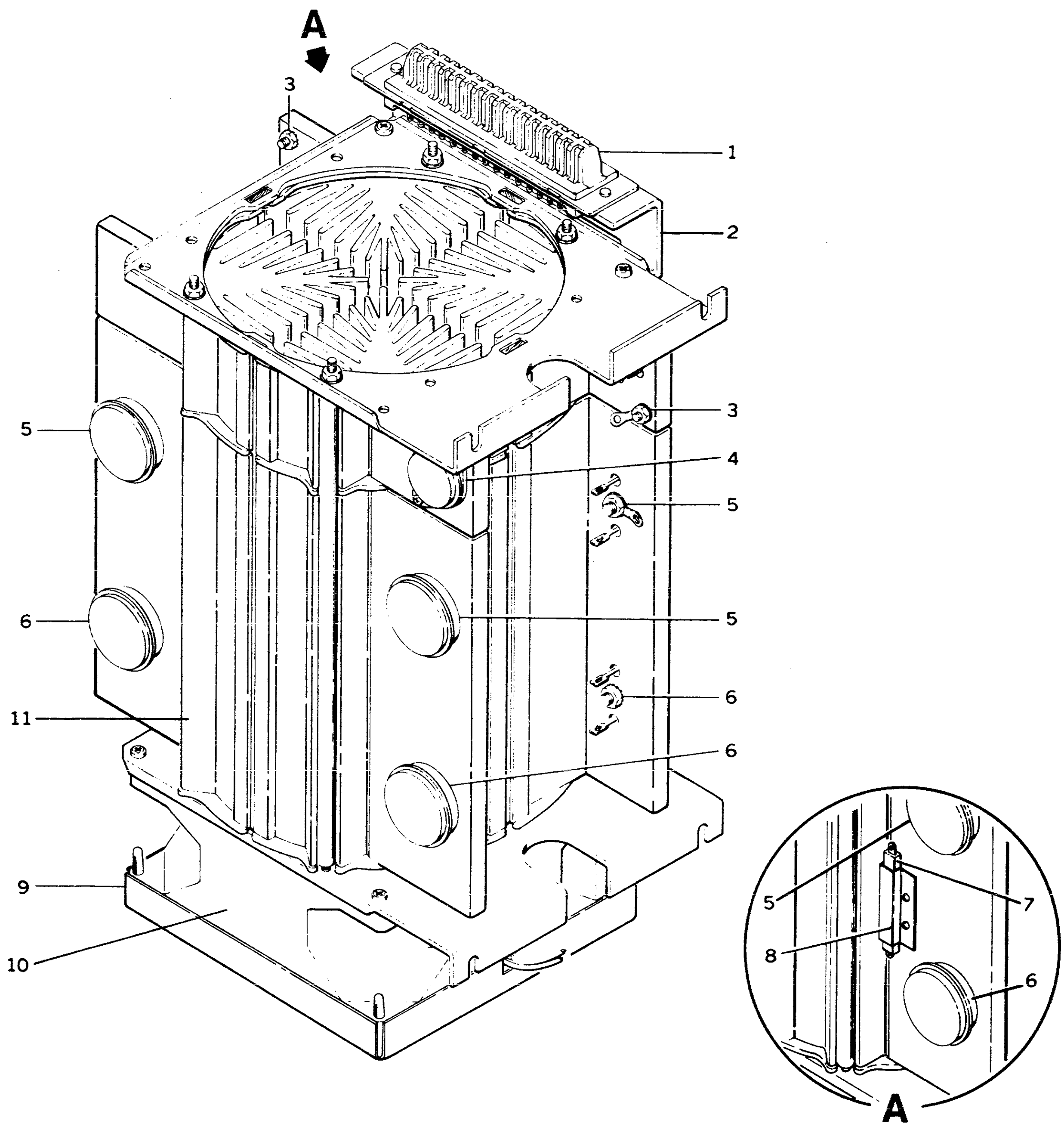

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Figure 6-16. A304 Large Heat Sink Assembly, Parts Identification Diagram

Table 6-17. A309 Component Board Assembly, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	UNITS PER ASSY.
6-17-	No Number	COMPONENT BOARD ASSEMBLY (A309) (46, fig. 6-6)			1
1	0150-0093 02116-0066	* Capacitor, Fxd, Cer, 0.01uf, +80 -20%, 100 VDCW (C4 thru C7)	28480	0150-0093	4
2	02116-0066	* Shorting Bar (Attaching Parts)	28480	02116-0066	2
	2480-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	4
	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	4
	3050-0239	* Washer, Nonmetallic, No. 8	00000	OBD	4
	3050-0139	* Washer, Flat, No. 8	00000	OBD	4
	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	4
		- - -x- - -			
3	1901-0344	* Diode, Si, (CR1 thru CR4) (Attaching Parts)	28480	1901-0344	4
	2480-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	4
	0360-0269	* Terminal Lug, No. 8	00000	OBD	4
	3050-0239	* Washer, Nonmetallic, No. 8	00000	OBD	4
	3050-0139	* Washer, Flat, No. 8	00000	OBD	4
	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	4
		- - - x - - -			
4	02116-0056	* Diode Mounting Bracket (Attaching Parts)	22480	02116-0056	1
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	2
	2190-0076	* Washer, Lock, Split, No. 8	00000	OBD	2
	3050-0139	* Washer, Flat, No. 8	00000	OBD	2
		- - - x - - -			
5	2110-0256	* Fuse, 30A, 32V, S-B (F11, F12, F13, F14)	00000	OBD	4
6	2110-0293	* Fuseholder Clip	00000	OBD	8
7	2110-0255	* Fuse Mounting Bracket (Attaching Parts)	28480	2110-0255	1
	2360-0201	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
8	02116-0021	* Right Brace	28480	02116-0021	1

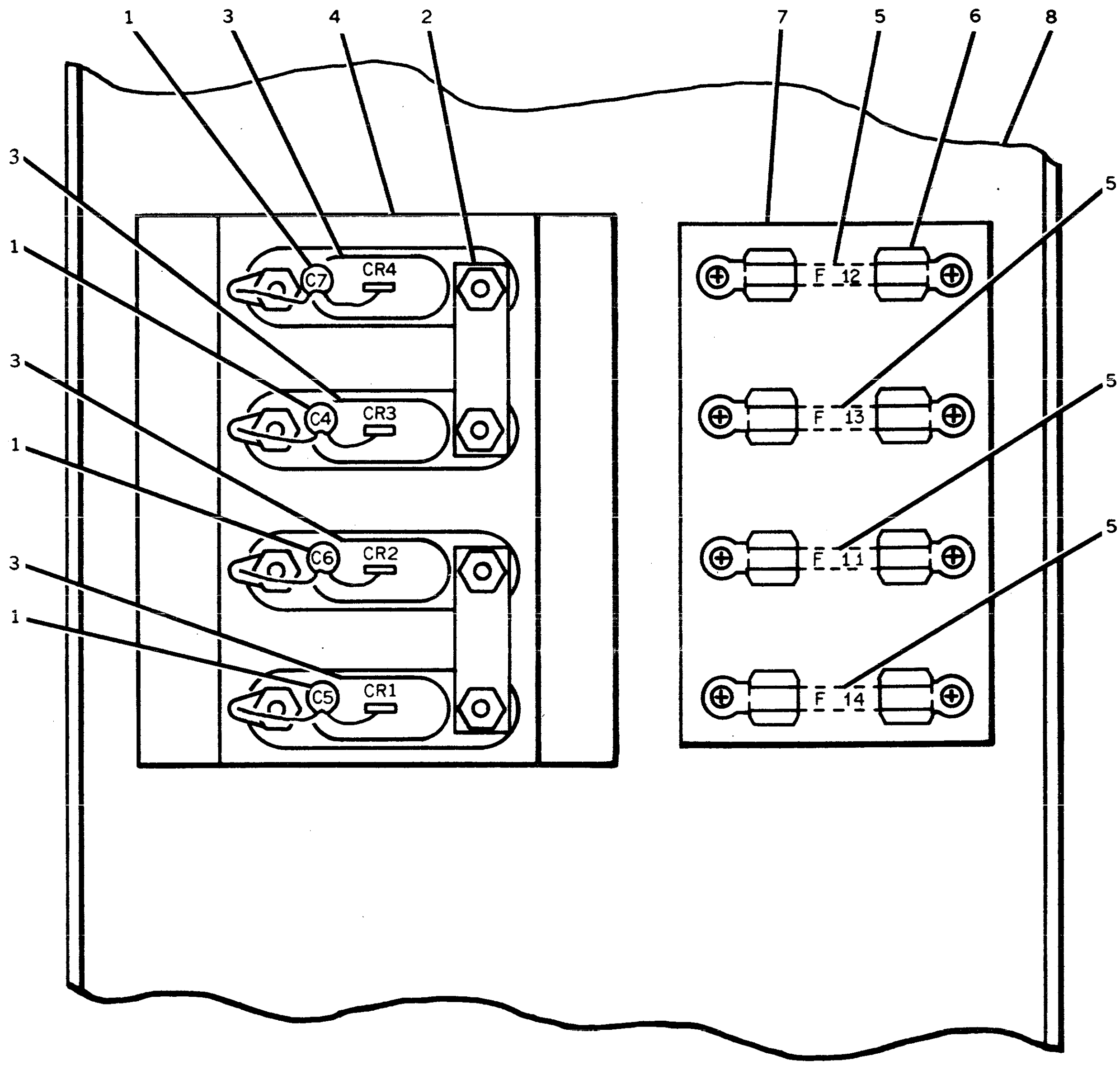

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Figure 6-17. A309 Component Board Assembly, Parts Identification Diagram

Table 6-18. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly
B	= motor
BT	= battery
C	= capacitor
CP	= coupler
CR	= diode
DL	= delay line
DS	= device signaling (lamp)
E	= misc hardware
F	= fuse
FL	= filter
J	= receptacle connector
K	= relay
L	= inductor
M	= meter
MC	= microcircuit
P	= plug connector
Q	= transistor
R	= resistor
RT	= thermistor
S	= switch
T	= transformer
TB	= terminal board
TP	= test point
U	= integrated circuit
V	= vacuum tube, neon bulb, photocell, etc.
VR	= voltage regulator
W	= cable, jumper
X	= socket
Y	= crystal
Z	= tuned cavity, network

ABBREVIATIONS

A	= amperes
AC	= alternating current
AFC	= automatic frequency control
ALUM	= aluminum
AR	= as required
ASSY	= assembly
BFO	= beat frequency oscillator
BE CU	= beryllium copper
BH	= binder head
BP	= bandpass
BRS	= brass
BWO	= backward wave oscillator
C	= capacitor
CCW	= counterclockwise
CER	= ceramic
CMO	= cabinet mount only
COEF	= coefficient
COM	= common
COMP	= composition
COMPL	= complete
CONN	= connector
CP	= cadmium plate
CRT	= cathode-ray tube
CTL	= capacitor-transistor logic
CW	= clockwise
DC	= direct current
DEPC	= deposited carbon
DPDT	= double-pole, double-throw
DPST	= double-pole, single-throw
DR	= drive
ELECT	= electrolytic
ENCAP	= encapsulated
EXT	= external
F	= farads
FH	= flat head
FIL H	= fillister head
FLM	= film
FXD	= fixed
G	= giga (10^9)
GE	= germanium
GL	= glass
GND/GRD	= ground(ed)
H	= henries
HDW	= hardware
HEX	= hexagonal
HG	= mercury
HR	= hour(s)
HZ	= hertz
ID	= inner diameter
IF	= intermediate frequency
IMPG	= impregnated
IN.	= inch, inches
INCD	= incandescent
INCL	= include(s)
INS	= insulation(ed)
INT	= internal
I/O	= input/output
K	= kilo = 1000
LH	= left hand
LIN	= linear taper
LK WASH	= lock washer
LOG	= logarithmic taper
LPF	= low pass filter
M	= milli = 10^{-3}
MEG	= mega = 10^6
MET OX	= metal oxide
MFR	= manufacturer
MHz	= megahertz
MINAT	= miniature
MOM	= momentary
MTG	= mounting
MY	= Mylar
N	= nano (10^{-9})
N/C	= normally closed
NE	= neon
NI PL	= nickel plate
NO.	= number
N/O	= normally open
NPN	= negative-positive-negative
NPO	= negative positive zero (zero temperature coefficient)
NRFR	= not recommended for field replacement
NSR	= not separately replaceable
OBD	= order by description
OD	= outer diameter
OH	= oval head
OX	= oxide
P	= peak
PC	= printed circuit
PF	= picofarads = 10^{-12} farads
PH	= Phillips head
PH BRZ	= phosphor bronze
PHL	= Phillips
PIV	= peak inverse voltage
PNP	= positive-negative-positive
P/O	= part of
POLY	= polystyrene
PORC	= porcelain
POS	= position(s)
POT	= potentiometer
PP	= peak-to-peak
PT	= point
PWV	= peak working voltage
R	= resistor
RECT	= rectifier
RF	= radio frequency
RH	= round head or right hand
RMO	= rack mount only
RMS	= root-mean square
RWV	= reverse working voltage
S-B	= slow-blow
SCR	= screw
SE	= selenium
SECT	= section(s)
SEMICON	= semiconductor
SI	= silicon
SIL	= silver
SL	= slide
SPDT	= single-pole, double-throw
SPG	= spring
SPL	= special
SPST	= single-pole, single-throw
SR	= split ring
SST	= stainless steel
STL	= steel
TA	= tantalum
TD	= time delay
TGL	= toggle
THD	= thread
TI	= titanium
TOL	= tolerance
TRIM	= trimmer
TTL	= transistor-transistor logic
TWT	= traveling wave tube
U (μ)	= micro = 10^{-6}
VAR	= variable
VDCW	= direct current working volts
W/	= with
W	= watts
WIV	= working inverse voltage
WW	= wirewound
W/O	= without

Table 6-19. Numerical Listing of Electrical Parts

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
0140-0151	Capacitor, Fxd, Mica, 820pf, 2%	28480	0140-0151	2
0140-0192	Capacitor, Fxd, Mica, 68pf, 5%	28480	0140-0192	2
0140-0197	Capacitor, Fxd, Mica, 180pf, 5%, 300VDCW	04062	RDM15F181-J3C	1
0140-0208	Capacitor, Fxd, Mica, 680pf, 5%	28480	0140-0208	1
0140-0210	Capacitor, Fxd, Mica, 270pf, 5%	28480	0140-0210	1
0140-0225	Capacitor, Fxd, Mica, 300pf, 1%	28480	0140-0225	2
0150-0050	Capacitor, Fxd, Cer, 1000pf, +80 -20% 1000VDCW	56289	C067B102-E102Z19-CDH	2
0153-0093	Capacitor, Fxd, Cer, 0.01uf, +80 -20% 100VDCW	28480	0150-0093	4
0150-0121	Capacitor, Fxd, Cer, 0.1uf, +80 -20% 50VDCW	56289	5C50BIS-CML	22
0160-0153	Capacitor, Fxd, My, 0.001uf, 10%, 200VDCW	56289	192P10292-PTS	8
0160-0154	Capacitor, Fxd, My, 0.0022uf, 10% 200VDCW	56289	192P22292-PTS	9
0160-0163	Capacitor, Fxd, My, 0.033uf, 10%, 200VDCW	56289	192P33392-PTS	3
0160-0168	Capacitor, Fxd, My, 0.1uf, 10%, 200VDCW	28480	0160-0168	2
0160-0363	Capacitor, Fxd, Mica, 620pf, 5%	28480	0160-0363	1
0160-2055	Capacitor, Fxd, Cer, 0.01uf, +80 -20%, 100VDCW	56289	C023F101F103-ZE12-CDH	27
0160-2088	Capacitor, Fxd, Cer, 1000pf, 5%, 50VDCW	28480	0160-2588	1
0160-3043	Capacitor, Fxd, Cer, 2 x 0.005uf, 20%, 250VAC	56289	29C147ACDH	2
0180-0049	Capacitor, Fxd, Elect, 20uf, 50VDCW	56289	30D206G050-DC6M1	2
0180-0064	Capacitor, Fxd, Elect, 35uf, +100 -10%, 6VDCW	56289	30D15G006BB4	3
0180-0094	Capacitor, Fxd, Elect, 100uf, 25VDCW	56289	30D107G025-DH4	2
0180-0097	Capacitor, Fxd, Elect, 47uf, 10%, 35VDCW	28480	0180-0097	2
0180-0141	Capacitor, Fxd, Elect, 50uf, +75 -10% 5VDCW	28480	0180-0141	4
0180-0155	Capacitor, Fxd, Elect, 2.2uf, 20%, 20VDCW	56289	150D225X0020-A2	52
0180-0197	Capacitor, Fxd, Elect, 2.2uf, 10%, 20VDCW	28480	0180-0197	8
0180-1714	Capacitor, Fxd, Elect, 330uf, 10%, 6VDCW	28480	0180-1714	1
0180-1735	Capacitor, Fxd, Elect, 0.22uf, 10%, 35VDCW	28480	0180-1735	2
0180-1866	Capacitor, Fxd, Elect, 500uf, +75 -10%, 75VDCW 75VDCW	56289	39D507G75HL4-DSB	2
0180-1867	Capacitor, Fxd, Elect, 1600ut, +75 -10%, 10VDCW	28480	0180-1867	1
0180-1869	Capacitor, Fxd, Elect, 8700uf, +75 -10% 20VDCW	28480	0180-1869	1
0180-1870	Capacitor, Fxd, Elect, 10000uf, +75 -10% 20VDCW	28480	0180-1870	2
0180-1871	Capacitor, Fxd, Elect, 12,000uf, +75 -10%, 25VDCW	28480	0180-1871	1

Table 6-19. Numerical Listing of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
0180-1873	Capacitor, Fxd, Elect, 100,000uf, +75 -10%, 20VDCW	28480	0180-1873	2
0180-1874	Capacitor, Fxd, Elect, 15,000uf, +75 -10%, 7.5VDCW	28480	0180-1874	2
0180-1875	Capacitor, Fxd, Elect, 270,000uf, +75 -10%, 3VDCW	56289	36D274G003-DF2A-DQB	4
0180-1977	Capacitor, Fxd, Elect, 5900uf, +75 -10%, 50VDCW	28480	0180-1977	4
0180-1978	Capacitor, Fxd, Elect, 880uf, +50 -10%, 75VDCW	28480	0180-1978	1
0360-1130	Terminal Board	28480	0360-1130	1
0360-1254	Terminal Board	28480	0360-1254	4
0360-1255	Terminal Board	00000	OBD	2
0360-1256	Terminal Board	28480	0360-1256	1
0410-0035	Crystal, Quartz, 10MC/S, 0.005%	28480	0410-0035	1
0490-0372	Relay, 50 ohm Coil	04009	WHU012D5-503	1
0683-0275	Resistor, Fxd, Comp, 2.7 ohms, 5%, 1/4w	01121	CB27G5	8
0683-1005	Resistor, Fxd, Comp, 10 ohms, 5%, 1/4w	01121	CB1005	1
0683-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4w	01121	CB1015	2
0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4w	01121	CB1025	40
0683-1215	Resistor, Fxd, Comp, 120 ohms, 5%, 1/4w	01121	CB1215	1
0683-1515	Resistor, Fxd, Comp, 150 ohms, 5%, 1/4w	01121	CB1515	3
0683-2205	Resistor, Fxd, Comp, 22 ohms, 5%, 1/4w	01121	CB2205	17
0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4w	01121	CB2215	12
0683-3305	Resistor, Fxd, Comp, 33 ohms, 5%, 1/4w	01121	CB3305	9
0683-3315	Resistor, Fxd, Comp, 330 ohms, 5%, 1/4w	01121	CB3315	1
0683-3935	Resistor, Fxd, Comp, 39k, 5%, 1/4w	01121	CB3935	1
0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB4715	48
0683-4725	Resistor, Fxd, Comp, 4700 ohms, 5%, 1/4w	01121	CB4725	1
0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4w	01121	CB5115	4
0683-5615	Resistor, Fxd, Comp, 560 ohms, 5%, 1/4w	01121	CB5615	4
0683-6805	Resistor, Fxd, Comp, 68 ohms, 5%, 1/4w	01121	CB6805	20
0683-8215	Resistor, Fxd, Comp, 820 ohms, 5%, 1/4w	01121	CB8215	1
0686-1235	Resistor, Fxd, Comp, 12k, 5%, 1/2w	01121	EB1235	2
0686-1515	Resistor, Fxd, Comp, 150 ohms, 5%, 1/2w	01121	EB1515	1
0686-2205	Resistor, Fxd, Comp, 22 ohms, 5%, 1w	01121	EB2205	5
0686-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/2w	28480	0686-2215	2
0686-3315	Resistor, Fxd, Comp, 220 ohms, 5%, 1w	01121	EB2215	2
0686-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1w	01121	EB4715	5
0689-1505	Resistor, Fxd, Comp, 15 ohms, 5%, 1w	01121	GB1505	2
0698-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4w	01121	CB1015	3
0698-3134	Resistor, Fxd, Flm, 1.33k, 1%, 1/4w	28480	0698-3134	1
0698-3154	Resistor, Fxd, Flm, 4.22k, 1%, 1/8w	28480	0698-3154	1
0698-3399	Resistor, Fxd, Flm, 133 ohms, 1%, 1/2w	28480	0698-3399	18
0698-3400	Resistor, Fxd, Flm, 147 ohms, 1%, 1/2w	28480	0698-3400	16
0698-3408	Resistor, Fxd, Flm, 2.15k, 1%, 1/2w	28480	0698-3408	1
0698-3411	Resistor, Fxd, Flm, 3.48k, 1%, 1/2w	28480	0698-3411	1
0698-3433	Resistor, Fxd, Flm, 28.7 ohms, 1%, 1/8w	28480	0698-3433	8

Table 6-19. Numerical Listing of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
0698-3435	Resistor, Fxd, Flm, 38.3 ohms, 1%, 1/8w	28480	0698-3435	8
0698-3438	Resistor, Fxd, Flm, 147 ohms, 1%, 1/8w	28480	0698-3438	10
0698-3441	Resistor, Fxd, Flm, 215 ohms, 1%, 1/8w	28480	0698-3441	4
0698-3443	Resistor, Fxd, Flm, 287 ohms, 1%, 1/8w	28480	0698-3443	1
0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8w	28480	0698-3444	9
0698-3488	Resistor, Fxd, Flm, 442 ohms, 1%, 1/8w	28480	0698-3488	17
0698-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB4715	3
0698-7310	Resistor, Fxd, Flm, 1.65k, 1%, 1/8w	28480	0698-7310	34
0751-0728	Resistor, Fxd, Flm, 619 ohms, 1%, 1/4w	28480	0757-0728	1
0757-0071	Resistor, Fxd, Flm, 247.5 ohms, 1%, 1/4w	28480	0757-0071	2
0757-0156	Resistor, Fxd, Flm, 1.5 Megohm, 1%, 1/2w	28480	0757-0156	2
0757-0158	Resistor, Fxd, Flm, 619 ohms, 1%, 1/2w	28480	0757-0158	1
0757-0159	Resistor, Fxd, Flm, 1000 ohms, 1%, 1/2w	28480	0757-0159	1
0757-0196	Resistor, Fxd, Flm, 6.19k, 1%, 1/2w	28480	0757-0196	1
0757-0197	Resistor, Fxd, Flm, 1500 ohms, 1%, 1/2w	28480	0757-0197	1
0757-0244	Resistor, Fxd, Flm, 499 ohms, 1%, 1/2w	28480	0757-0244	3
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8w	28480	0757-0280	41
0757-0338	Resistor, Fxd, Flm, 1.00k, 1%, 1/4w	28480	0757-0338	2
0757-0340	Resistor, Fxd, Flm, 10.0k, 1%, 1/4w	28480	0757-0340	1
0757-0399	Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/8w	28480	0757-0399	8
0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8w	28480	0757-0401	32
0757-0403	Resistor, Fxd, Flm, 121 ohms, 1%, 1/8w	28480	0757-0403	8
0757-0416	Resistor, Fxd, Flm, 511 ohms, 1%, 1/8w	28480	0757-0416	18
0757-0417	Resistor, Fxd, Flm, 562 ohms, 1%, 1/8w	28480	0757-0417	10
0757-0419	Resistor, Fxd, Flm, 681 ohms, 1%, 1/8w	28480	0757-0419	1
0757-0427	Resistor, Fxd, Flm, 150k, 1%, 1/8w	28480	0757-0427	1
0757-0438	Resistor, Fxd, Flm, 5.11k, 1%, 1/8w	28480	0757-0438	17
0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8w	28480	0757-0442	3
0757-0451	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8w	28480	0757-0451	34
0757-0705	Resistor, Fxd, Flm, 47.5 ohms, 1%, 1/4w	28480	0757-0705	1
0757-0711	Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/4w	28480	0757-0711	2
0757-0715	Resistor, Fxd, Flm, 150 ohms, 1%, 1/4w	28480	0757-0715	2
0757-0727	Resistor, Fxd, Flm, 562 ohms, 1%, 1/4w	28480	0757-0727	1
0757-0730	Resistor, Fxd, Flm, 750 ohms, 1%, 1/4w	28480	0757-0730	3
0757-0732	Resistor, Fxd, Flm, 909 ohms, 1%, 1/4w	28480	0757-0732	1
0757-0739	Resistor, Fxd, Flm, 2.00k, 1%, 1/4w	28480	0757-0739	1
0757-0743	Resistor, Fxd, Flm, 3.32k, 1%, 1/4w	28480	0757-0743	3
0757-0744	Resistor, Fxd, Flm, 3920 ohms, 1%, 1/4w	28480	0757-0744	1
0757-0759	Resistor, Fxd, Flm, 182k, 1%, 1/4w	28480	0757-0759	1
0757-0805	Resistor, Fxd, Flm, 221 ohms, 1%, 1/2w	28480	0757-0805	1
0757-0808	Resistor, Fxd, Flm, 301 ohms, 1%, 1/4w	28480	0757-0808	2
0757-0814	Resistor, Fxd, Flm, 511 ohms, 1%, 1/2w	28480	0757-0814	1
0757-0821	Resistor, Fxd, Flm, 1.21k, 1%, 1/2w	28480	0757-0821	2
0757-0834	Resistor, Fxd, Flm, 2.62k, 2%, 1/2w	28480	0757-0834	1
0757-0839	Resistor, Fxd, Flm, 10k, 1%, 1/2w	28480	0757-0839	1
0757-0900	Resistor, Fxd, Flm, 100 ohms, 2%, 1/8w	28480	0757-0900	5
0757-0910	Resistor, Fxd, Flm, 270 ohms, 2%, 1/8w	28480	0757-0910	1
0757-0912	Resistor, Fxd, Flm, 330 ohms, 2%, 1/8w	28480	0757-0912	1

Table 6-19. Numerical Listing of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
0757-0914	Resistor, Fxd, Flm, 390 ohms, 2%, 1/8w	28480	0757-0914	1
0757-0915	Resistor, Fxd, Flm, 430 ohms, 2%, 1/8w	28480	0757-0915	1
0757-0916	Resistor, Fxd, Flm, 470 ohms, 2%, 1/8w	28480	0757-0916	1
0757-0918	Resistor, Fxd, Flm, 560 ohms, 2%, 1/8w	28480	0757-0918	1
0757-0920	Resistor, Fxd, Flm, 680 ohms, 2%, 1/8w	28480	0757-0920	1
0757-0924	Resistor, Fxd, Flm, 1k, 2%, 1/8w	28480	0757-0924	7
0757-0931	Resistor, Fxd, Flm, 2k, 2%, 1/8w	28480	0757-0931	2
0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8w	28480	0757-1094	1
0761-0005	Resistor, Fxd, Met Ox, 2200 ohms, 5%, 1w	28480	0761-0005	1
0761-0008	Resistor, Fxd, Met Ox, 510 ohms, 5%, 1w	28480	0761-0008	1
0761-0011	Resistor, Fxd, Met Ox, 3300 ohms, 5%, 1w	28480	0761-0011	1
0761-0026	Resistor, Fxd, Met Ox, 220 ohms, 5%, 1w	28480	0761-0026	1
0761-0038	Resistor, Fxd, Met Ox, 5600 ohms, 5%, 1w	28480	0761-0038	1
0761-0058	Resistor, Fxd, Met Ox, 750 ohms, 5%, 1w	28480	0761-0058	2
0764-0017	Resistor, Fxd, Met Ox, 1.6 k, 5%, 2w	28480	0764-0017	1
0764-0062	Resistor, Fxd, Met Ox, 3.6k, 5%, 2w	28480	0764-0062	1
0764-0063	Resistor, Fxd, Flm, 620 ohms, 5%, 2w	28480	0764-0063	1
0767-0003	Resistor, Fxd, Met Ox, 1.20k, 5%, 3w	28480	0767-0003	1
0770-0002	Resistor, Fxd, Flm, 2400 ohms, 5%, 4w	28480	0770-0002	1
0770-0003	Resistor, Fxd, Flm, 3300 ohms, 5%, 4w	28480	0770-0003	1
0811-0003	Resistor, Fxd, WW, 390 ohms, 1%, 1/4w	28480	0811-0003	1
0811-0040	Resistor, Fxd, WW, 1 ohm, 1%, 5w	28480	0811-0040	3
0811-1339	Resistor, Fxd, WW, 500 ohms, 5%, 5w	28480	0811-1339	1
0811-1857	Resistor, Fxd, WW, 400 ohms, 5%, 5w	28480	0811-1857	4
0811-1858	Resistor, Fxd, WW, 500 ohms, 5%, 5w	28480	0811-1858	1
0811-2031	Resistor, Fxd, WW, 815 ohms, 3.0%, 1/4w	01686	7010	2
0811-2032	Resistor, Fxd, WW, 880 ohms, 1%, 1/4w	28480	0811-2032	1
0811-2033	Resistor, Fxd, WW, 1100 ohms, 1%, 1/4w	28480	0811-2033	1
0811-2035	Resistor, Fxd, WW, 1590 ohms, 1%, 1/4w	28480	0811-2035	1
0811-2036	Resistor, Fxd, WW, 1800 ohms, 1%, 1/4w	28480	0811-2036	1
0811-2037	Resistor, Fxd, WW, 2400 ohms, 1%, 1/4w	28480	0811-2037	1
0811-2039	Resistor, Fxd, WW, 8000 ohms, 1%, 1/4w	28480	0811-2039	4
0811-2040	Resistor, Fxd, WW, 21.8k, 1%, 1/4w	28480	0811-2040	1
0811-2078	Resistor, Fxd, WW, 0.15 ohm, 3%, 12w	28480	0811-2078	8
0811-2084	Resistor, Fxd, WW, 43 ohms, 1%, 5w	28480	0811-2084	3
0811-2097	Resistor, Fxd, WW, 0.25 ohm, 3%, 5w	28480	0811-2097	2
0811-2098	Resistor, Fxd, WW, 2.75k, 1%, 1/4w	28480	0811-2098	1
0811-2107	Resistor, Fxd, WW, 75 ohms, 5%, 10w	28480	0811-2107	2
0811-2138	Resistor, Fxd, WW, 120 ohms, 5%, 5w	28480	0811-2138	2
0811-2140	Resistor, Fxd, WW, 2 ohms, 5%, 5w	28480	0811-2140	1
0811-2509	Resistor, Fxd, WW, 0.5 ohms, 5%, 25w	28480	0811-2509	1
0811-2510	Resistor, Fxd, WW, 0.1 ohm, 5%, 25w	28480	0811-2510	2
0811-2610	Resistor, Fxd, WW, 4.99k, 1%, 1/4w	28480	0811-2610	1
0811-2611	Resistor, Fxd, WW, 17.4k, 1%, 1/4w	28480	0811-2611	1
0811-2614	Resistor, Fxd, WW, 37 ohms, 1%, 5w	28480	0811-2614	34
0811-2648	Resistor, Fxd, WW, 5 ohms, 3%, 12.5w	28480	0811-2648	1
0812-0050	Resistor, Fxd, WW, 3k, 5%, 5w	28480	0812-0050	1
0812-0099	Resistor, Fxd, WW, 1k, 5%, 5w	28480	0812-0099	3
0813-0029	Resistor, Fxd, WW, 1 ohm, 3%, 3w	28480	0813-0029	2
0813-0038	Resistor, Fxd, WW, 0.5 ohms, 10%, 5w	28480	0813-0038	14

Table 6-19. Numerical Listing of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
0815-0005	Resistor, Fxd, WW, 62 ohms, 5%, 10w	28480	0815-0005	1
1250-0315	Connector, Receptacle	28480	1250-0315	1
1251-0136	Connector, Receptacle	28480	1251-0136	2
1251-0137	Connector, Receptacle, 32 contacts	71785	26-4200-325	2
1251-0143	Connector, Receptacle, Power	74868	32-2907-3	1
1251-0233	Connector, PC Pin	28480	1251-0233	1
1251-0335	Connector, PC Pin	28480	1251-0335	1
1251-0367	Tip Jack	28480	1251-0367	8
1820-0054	Integrated Circuit, TTL	56289	USN7400A	3
1820-0063	Integrated Circuit, TTL	56289	USN7451A	2
1820-0069	Integrated Circuit, TTL	56289	USN7420A	8
1820-0127	Integrated Circuit, TTL	07263	U6A900359X	10
1820-0183	Integrated Circuit, TTL	02735	80170	17
1820-0186	Integrated Circuit, TTL	28480	1820-0186	28
1820-0187	Integrated Circuit, CTL	28480	1820-0187	15
1820-0374	Integrated Circuit, TTL	01295	SN74H21N	8
1820-0375	Integrated Circuit, TTL	01295	SN74H30N	1
1820-0952	Integrated Circuit, CTL	07263	SL3455	64
1820-0953	Integrated Circuit, CTL	07263	SL3456	74
1820-0954	Integrated Circuit, CTL	07263	SL3457	33
1820-0955	Integrated Circuit, CTL	07263	SL3458	4
1820-0956	Integrated Circuit, CTL	07263	SL3459	79
1820-0957	Integrated Circuit, CTL	07263	SL3460	2
1820-0964	Integrated Circuit, CTL	07263	SL3461	2
1820-0965	Integrated Circuit, CTL	07263	SL3462	13
1820-0966	Integrated Circuit, CTL	07263	SL3463	4
1820-0967	Integrated Circuit, CTL	07263	SL3464	40
1820-0968	Integrated Circuit, CTL	07263	SL3466	8
1820-0971	Integrated Circuit, CTL	07263	SL3467	19
1850-0062	Transistor, Ge	01295	GA287	6
1850-0098	Transistor, Ge, PNP	28480	1850-0098	13
1851-0017	Transistor, Ge, NPN	01295	2N130A	4
1853-0001	Transistor, Si, PNP	28480	1853-0001	6
1853-0012	Transistor, Si, PNP	04713	2N2904A	16
1853-0015	Transistor, Si, PNP	04713	MP53640-5	8
1853-0016	Transistor, Si, PNP	07263	2N3638	10
1853-0036	Transistor, Si, PNP	04713	SP3612	44
1853-0063	Transistor, Si, NPN	04713	MJ2268	2
1854-0003	Transistor, Si, NPN	28480	1854-0003	2
1854-0005	Transistor, Si, NPN	02735	2N708	3
1854-0013	Transistor, Si, NPN	04713	2N2218A	8
1854-0022	Transistor, Si, NPN	07263	517843	2
1854-0041	Transistor, Si, PNP	02735	38640	2
1854-0072	Transistor, Si, NPN	02735	2N3054	1
1854-0094	Transistor, Si, NPN	07263	2N3646	42
1854-0215	Transistor, Si, NPN	28480	1854-0215	2
1854-0221	Transistor, Si, NPN	28480	1854-0221	2
1854-0246	Transistor, Si, NPN	07263	2N3643	46
1854-0255	Transistor, Si, NPN	07263	2N3642	34

Table 6-19. Numerical Listing of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
1854-0264	Transistor, Si, NPN	04713	2N3715	4
1854-0265	Transistor, Si, NPN	28480	1854-0265	1
1884-0046	Thyristor, SCR, 50V, 25A	28480	1884-0046	7
1884-0047	Thyristor, SCR, 25V, 55A	28480	1884-0047	2
1901-0025	Diode, Si, 100WV, 100mA	28480	1901-0025	11
1901-0040	Diode, Si, 30mA, 30WV	07263	FDG1088	66
1901-0045	Diode, Si, 0.75A, 100 PIV	04713	SR1358-7	1
1901-0050	Diode, Si, 75V	28480	1901-0050	17
1901-0191	Diode, Si, 100 PIV,0.75A	28480	1901-0191	13
1901-0343	Diode, Si, 50 PIV, 18A	04713	SZ11747	4
1901-0344	Diode, Si	28480	1901-0344	4
1901-0406	Diode, Si, 50 PIV, 18A	04713	1N3491/MR322	3
1901-0416	Diode, Si, 200 PIV, 3A	28480	1901-0416	16
1901-0476	Diode, Si, 100 PIV, 12A	04713	MR1121	4
1902-0017	Diode, Breakdown, 6.81V, 10%, 400mw	28480	1902-0017	1
1902-0071	Diode, Breakdown, 9.0V, 5%	28480	1902-0071	6
1902-0184	Diode, Breakdown, Si, 16.2V, 5%	28480	1902-0184	1
1902-0379	Diode, Breakdown, 20V, 10%, 1.5w	28480	1902-0379	3
1902-0551	Diode, Breakdown, 6.19V, 5%	28480	1902-0551	1
1902-0556	Diode, Breakdown, 20.0V, 5%, 1w	28480	1902-0556	1
1902-1205	Diode, Breakdown, 15V, +2%	04713	1N2979RB	2
1902-1215	Diode, Breakdown, 10w, 10%, 25V	28480	1902-1215	1
1902-1217	Diode, Breakdown, 6.20V, 5%, 405mA	04713	SZ11746	1
1902-1218	Diode, Breakdown, 39V, 2% at 65mA	04713	SZ11747	1
1902-1228	Diode, Breakdown, 27V, 10%, 10w	28480	1902-1228	2
1902-3079	Diode, Breakdown, Si, 4.53V	28480	1902-3079	2
1902-3182	Diode, Breakdown, Si, 12.1V, 5%	28480	1902-3182	1
1902-3224	Diode, Breakdown, 17.8V, 5%, 400mA	28480	1902-3224	1
1910-0016	Diode, Germanium, 25V	28480	1910-0016	16
1910-0022	Diode, Germanium, 5 WIV	28480	1910-0022	4
2100-0741	Resistor, Var, WW, 5k, 5%, 1w	28480	2100-0741	1
2100-0755	Resistor, Var, WW, 1k, 5%	28480	2100-0755	1
2100-1429	Resistor, Var, WW, 2000 ohms, 5%, 1w	28480	2100-1429	2
2100-1770	Resistor, Var, WW, 100 ohms, 5%	28480	2100-1770	3
2100-1772	Resistor, Var, WW, 500 ohms, 5%	28480	2100-1772	2
2100-1776	Resistor, Var, WW, 10k, 10%, 1/2w	28480	2100-1776	1
2110-0013	Fuse, 3.2A, SB	00000	OBD	1
2110-0014	Fuse, 4A, SB	00000	OBD	1
2110-0023	Fuse, 6.25A, SB	00000	OBD	5
2110-0025	Fuse, 15A, SB	00000	OBD	1
2110-0044	Fuse, 3A, SB	00000	OBD	2
2110-0256	Fuse, 30A, 32V, SB	00000	OBD	4
2140-0035	Lamp, Incandesent, 6.3V, 0.75A	71744	1775	92
3101-0714	Switch, Lighted, Pushbutton	28480	3101-0714	1
3101-0715	Switch, Lighted, Pushbutton	28480	3101-0715	9
3101-0716	Lens (RUN)	28480	3101-0716	1
3101-0717	Lens (LOAD ADDRESS)	28480	3101-0717	1
3101-0718	Lens (PRESET)	28480	3101-0718	1
3101-0719	Lens (POWER)	28480	3101-0719	1

Table 6-19. Numerical Listing of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
3101-0720	Lens (SINGLE CYCLE)	28480	3101-0720	1
3101-0721	Lens (HALT)	28480	3101-0721	1
3101-0722	Lens (LOAD B)	28480	3101-0722	1
3101-0723	Lens (LOAD MEMORY)	28480	3101-0723	1
3101-0724	Lens (LOAD A)	28480	3101-0724	1
3101-0725	Lens (DISPLAY MEMORY)	28480	3101-0725	1
3101-0973	Switch, Slide, DPDT, 0.5A, 125V, AC/DC	79727	G126-0018	3
3101-1051	Switch, Toggle, SPST, 125V, 3A	88140	8908K507	17
3103-0004	Switch, Thermostat, 115V, 2A	28480	3103-0004	3
3160-0072	Fan Assembly, 115V, 60Hz	23936	Model 2500	6
8159-0005	Jumper Wire	28480	8159-0005	6
9100-1219	Transformer, Power	28480	9100-1219	1
9100-1238	Transformer	90095	1WEMA	16
9100-1834	Line Filter, 20A, AC	28480	9100-1834	1
9140-0107	Coil, Fxd, RF, 27 MHz, 10%	99800	1840-38	1
02116-6014	Logic Supply Regulator Card	28480	02116-6014	1
02116-6015	Memory Supply Regulator Card	28480	02116-6015	1
02116-6026	Arithmetic Logic Card	28480	02116-6026	1
02116-6027	Instruction Decoder Card	28480	02116-6027	1
02116-6029	Shift Logic Card	28480	02116-6029	1
02116-6041	I/O Control Card	28480	02116-6041	1
02116-6043	Display Board	28480	02116-6043	1
02116-6069	Direct Memory Logic Card	28480	02116-6069	1
02116-6126	Overvoltage Component Board Assembly	28480	02116-6126	1
02116-6175	Power Fail InteruptCard	28480	02116-6175	1
02116-6194	I/O Address Card	28480	02116-6194	1
02116-6208	Front Panel Coupler Card	28480	02116-6208	1
02116-6265	Inhibit Driver Card	28480	02116-6265	2
02116-6266	Driver/Switch Card	28480	02116-6266	2
02116-6281	Timing Generator Card	28480	02116-6281	1
02116-6282	Back Panel Assembly	28480	02116-6282	1
02116-6284	Overvoltage Protection Assembly	28480	02116-6284	1
02116-6288	Core Stack Assembly	28480	02116-6288	1
02116-6290	Cable Assembly	28480	02116-6290	1
02116-6291	Cable Assembly	28480	02116-6291	1
02116-6292	Cable Assembly	28480	02116-6292	1
02116-6293	Cable Assembly	28480	02116-6293	1
02116-6294	Cable Assembly	28480	02116-6294	1
02116-6298	Sense Amplifier Card	28480	02116-6298	2
02116-6300	Memory Module Decoder Card	28480	02116-6300	1
02116-8038	PC Board, Blank	28480	02116-8038	1

Table 6-20. Numerical Listing of Mechanical Parts

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
0360-0268	Terminal Lug, No. 6	00000	OBD	22
0360-0269	Terminal Lug, No. 8	00000	OBD	4
0360-0270	Terminal Lug, No. 10	00000	OBD	5
0360-0271	Terminal Lug, 1/4 I.D.	00000	OBD	1
0360-0279	Standoff, Terminal, No. 4-40	00000	OBD	2
0360-1089	Terminal Lug, 1/2 in. I.D.	00000	OBD	2
0360-1256	Terminal Board	28480	0360-1256	1
0360-1260	Terminal Lug	28480	0360-1260	7
0360-1264	Terminal Lug	28480	0360-1264	2
0360-1279	Shorting Strip	28480	0360-1279	2
0362-0128	Termination, Crimp Lug	00000	OBD	2
0362-0188	Cover, Power Switch	28480	0362-0188	1
0380-0002	Spacer, 1/4 in.	00000	OBD	2
0400-0082	Grommet, Nylon	28480	0400-0082	2
0403-0091	Insert, Foot	28480	0403-0091	4
0404-0247	Trim Strip	28480	0404-0247	2
0404-0248	Trim Strip, Left	28480	0404-0248	1
0404-0371	Trim Strip, Right	28480	0404-0371	1
0460-0020	Adhesive Cork	28480	0460-0020	1
0510-0735	Latch, Female	28480	0510-0735	6
0510-0736	Latch, Male	28480	0510-0736	6
0520-0065	Screw, Machine, PH, No. 2-56, 1/4 in.	00000	OBD	18
0520-0103	Screw, Machine, PH, No. 2-56, 3/8 in.	00000	OBD	2
0570-0070	Bolt, Machine, Hexagon Head, 1/4-20, 3-1/2 in.	00000	OBD	2
0570-1003	Bolt, Machine, Hexagon Head, 1/4-20, 3-1/4 in.	00000	OBD	2
0570-1049	Spring Plunger	01226	M-54N	2
0590-0010	Cap Nut, No. 8	00000	OBD	2
0590-0076	Nut, Self-Locking, Hexagon, No. 4-40	00000	OBD	10
0590-0077	Nut, Self-Locking, Hexagon, No. 6-32	00000	OBD	1
0590-0843	Nut, Self-Locking, Hexagon, No. 8-32	00000	OBD	8
0610-0001	Nut, Plain, Hexagon, No. 2-56	00000	OBD	4
1200-0080	Washer, Flat, Anodized	28480	1200-0080	8
1200-0088	Washer, Flat, Anodized	28480	1200-0088	2
1200-0089	Washer, Flat, Anodized	28480	1200-0089	2
1205-0006	Heat Sink	28480	1205-0006	1
1205-0033	Heat Sink	28480	1205-0033	7
1205-0067	Heat Sink	28480	1205-0067	1
1205-0075	Heat Sink	28480	1205-0075	1
1390-0107	Button Latch	13061	B10-B1	1
1390-0179	Lock and Key	74842	DS416J	1
1400-0084	Fuseholder	00000	OBD	1
1400-0124	Cable Clamp	00000	OBD	5
1400-0126	Cable Clamp	00000	OBD	1
1400-0127	Cable Clamp	00000	OBD	1
1400-0741	Cable Clamp, Base	28480	1400-0741	1
1410-0009	Bearing, Ball, Annular	21335	SIKFS58115	6
1460-0742	Spring, Compression, 5/8 in. long, 3/16 in. I.D.	00000	OBD	1
1480-0116	Extractor Pin, PC Card	28480	1480-0116	38
2110-0255	Fuse Mounting Bracket	28480	2110-0255	2
2110-0293	Fuseholder Clip	00000	OBD	26

Table 6-20. Numerical Listing of Mechanical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
2120-0012	Washer, Lock, ext-tooth, No. 10	00000	OBD	2
2190-0003	Washer, Lock, Split, No. 4	00000	OBD	1
2190-0006	Washer, Lock, Split, No. 6	00000	OBD	7
2190-0007	Washer, Lock, int-tooth, No. 6	00000	OBD	4
2190-0010	Washer, Lock, ext-tooth, No. 8	00000	OBD	2
2190-0017	Washer, Lock, Split, No. 8	00000	OBD	48
2190-0032	Washer, Lock, Split, No. 10	00000	OBD	14
2190-0034	Washer, Lock, Split, No. 10	00000	OBD	18
2190-0043	Washer, Lock, Split, 1/2 in. I.D.	00000	OBD	2
2190-0045	Washer, Lock, Split, No. 2	00000	OBD	9
2190-0047	Washer, Recessed, No. 6	00000	OBD	8
2190-0048	Washer, Recessed, No. 8	00000	OBD	18
2190-0070	Washer, Lock, ext-tooth, 1/4 in. I.D.	00000	OBD	1
2190-0074	Washer, Lock, Split, No. 10	00000	OBD	8
2190-0076	Washer, Lock, Split, No. 8	00000	OBD	34
2190-0102	Washer, Lock, int-tooth, 1/2 in. inside dia.	00000	OBD	17
2190-0108	Washer, Lock, Split, No. 4	00000	OBD	17
2190-0147	Washer, Recessed, No. 6	00000	OBD	4
2190-0851	Washer, Lock, Split, No. 6	00000	OBD	49
2200-0139	Screw, Machine, PH, No. 4-40, 1/4 in.	00000	OBD	1
2200-0141	Screw, Machine, PH, No. 4-40, 5/16 in.	00000	OBD	1
2200-0143	Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	20
2200-0144	Screw, Machine, FH, No. 4-40, 3/8 in.	00000	OBD	3
2200-0149	Screw, Machine, PH, No. 4-40, 5/8 in.	00000	OBD	6
2200-0709	Screw, Nylon, FH, No. 4-40, 3/8 in.	00000	OBD	4
2260-0001	Nut, Plain, Hexagon, No. 4-40	00000	OBD	2
2360-0109	Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	4
2360-0192	Screw, Machine, FH, No. 6-32, 1/4 in.	00000	OBD	13
2360-0193	Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	41
2360-0196	Screw, Machine, FH, No. 6-32, 3/8 in.	00000	OBD	12
2360-0197	Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	45
2360-0200	Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	21
2360-0201	Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	23
2360-0202	Screw, Machine, FH, No. 6-32, 5/8 in.	00000	OBD	1
2360-0203	Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	46
2360-0204	Screw, Machine, FH, No. 6-32, 3/4 in.	00000	OBD	10
2360-0205	Screw, Machine, PH, No. 6-32, 3/4 in.	00000	OBD	8
2360-0206	Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	3
2360-0207	Screw, Machine, PH, No. 6-32, 7/8 in.	00000	OBD	4
2360-0209	Screw, Machine, PH, No. 6-32, 1 in.	00000	OBD	4
2360-0268	Terminal Lug, No. 6	00000	OBD	5
2370-0030	Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	2
2390-0014	Screw, Machine, PH, No. 6-32, 2-1/4 in.	00000	OBD	3
2420-0001	Nut, Assembled Washer, No. 6-32	00000	OBD	97
2420-0002	Nut, Plain, Hexagon, No. 6-32	00000	OBD	51
2470-0002	Nut, Plain, Hexagon, No. 10-32	00000	OBD	5
2480-0004	Nut, Plain, Hexagon, No. 8-32	00000	OBD	8
2510-0063	Screw, Machine, FH, No. 8-32, 1-1/2 in.	00000	OBD	2
2510-0102	Screw, Machine, FH, No. 8-32, 3/8 in.	00000	OBD	21

Table 6-20. Numerical Listing of Mechanical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
2510-0103	Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	74
2510-0106	Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	24
2510-0107	Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	38
2510-0109	Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	27
2510-0111	Screw, Machine, PH, No. 8-32, 3/4 in.	00000	OBD	2
2515-0016	Screw, Machine, PH, No. 8-32, 2-1/2 in.	00000	OBD	3
2530-0017	Screw, Machine, FH, No. 8-32, 1/4 in.	00000	OBD	14
2580-0003	Nut, Assembled Washer, No. 8-32	00000	OBD	15
2580-0004	Nut, Plain, Hexagon, No. 8-32	00000	OBD	14
2680-0103	Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	21
2680-0104	Screw, Machine, FH, No. 10-32, 1/2 in.	00000	OBD	4
2680-0108	Screw, Machine, FH, No. 10-32, 3/4 in.	00000	OBD	5
2740-0002	Nut, Plain, Hexagon, No. 10-32	00000	OBD	47
2950-0004	Nut, Plain, Hexagon, 1/4-20	00000	OBD	2
2950-0024	Nut, Plain, Hexagon, 1/2-20	00000	OBD	2
2950-0035	Nut, Plain, Hexagon, 15/32-32	00000	OBD	17
2950-0036	Nut, Plain, Hexagon, 1/4-28	00000	OBD	2
3030-0248	Setscrew, No. 10-32, 3/4 in.	00000	OBD	17
3050-0098	Washer, Flat, No. 2	00000	OBD	2
3050-0139	Washer, Flat, No. 8	00000	OBD	30
3050-0222	Washer, Flat, No. 4	00000	OBD	22
3050-0225	Washer, Flat, 1/4 I.D.	00000	OBD	1
3050-0226	Washer, Flat, No. 10	00000	OBD	14
3050-0228	Washer, Flat, No. 6	00000	OBD	63
3050-0234	Washer, Flat, 1/4 in. I.D.	00000	OBD	8
3050-0238	Washer, Nonmetallic Shouldered, No. 8	00000	OBD	4
3050-0239	Washer, Nonmetallic, No. 8	00000	OBD	17
3050-0247	Washer, Nonmetallic, No. 6	00000	OBD	13
3050-0270	Terminal Lug, No. 10	00000	OBD	4
3130-0130	Nut, Face	28480	3130-0103	17
3160-0099	Fan Grille	23936	5504	3
4040-0431	Air Deflector	28480	4040-0431	1
4320-0002	Gasket, rubber	28480	4320-0002	1
4320-0043	Channel, rubber	28480	4320-0043	1
4320-0096	Extrusion, rubber	28480	4320-0096	1
4330-0186	Window, Glass	28480	4330-0186	1
5000-0131	Trim, Aluminum	28480	5000-0131	2
5000-5722	Bracket, Mounting Filter	28480	5000-5722	1
5020-0244	Bracket	28480	5020-0244	4
5020-1922	Spacer, Nylon	28480	5020-0763	1
5040-1464	Extractor, PC Card	28480	5040-1464	38
5060-0735	Retaining Plate, Handle	28480	5060-0735	2
5060-0763	Handle	28480	5060-0763	2
5080-1543	Component Board	28480	5080-1543	2
8120-1214	Ground Cable, 27-1/2 in.	28480	8120-1214	4
02116-0002	Bracket, Transformer	28480	02116-0002	1
02116-0005	Front Panel	28480	02116-0005	2
02116-0007	Panel Brace	28480	02116-0007	1
02116-0008	Side Panel, Right	28480	02116-0008	1
02116-0009	Side Panel, Left	28480	02116-0009	1

Table 6-20. Numerical Listing of Mechanical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
02116-0010	Fan Panel	28480	02116-0010	1
02116-0012	Center Brace	28480	02116-0012	2
02116-0013	Side Cover	28480	02116-0013	2
02116-0014	Cover, Lower Rear	28480	02116-0014	1
02116-0015	Cover, Upper Rear	28480	02116-0015	1
02116-0016	Top Cover	28480	02116-0016	2
02116-0020	Center Brace	28480	02116-0020	1
02116-0021	Right Brace	28480	02116-0021	1
02116-0022	Left Brace	28480	02116-0022	1
02116-0023	Bracket, Mounting, Bus Bar	28480	02116-0023	1
02116-0024	Housing, AC Input	28480	02116-0024	1
02116-0025	Deck, Blank, Power Supply	28480	02116-0025	1
02116-0026	Transformer Cover	28480	02116-0026	1
02116-0027	Back Panel	28480	02116-0027	1
02116-0028	Support Plate	28480	02116-0028	1
02116-0032	Bottom Panel	28480	02116-0032	1
02116-0033	Bracket, Thermoswitch	28480	02116-0033	2
02116-0047	Capacitor Board Bracket	28480	02116-0047	1
02116-0048	Cover, AC Housing	28480	02116-0048	1
02116-0053	Bracket, Connector	28480	02116-0053	2
02116-0054	Bracket, Connector	28480	02116-0054	2
02116-0056	Bracket, Diode Mounting	28480	02116-0056	2
02116-0057	Filter, Air	28480	02116-0057	2
02116-0059	Bracket, Terminal Mounting, Left	28480	02116-0059	1
02116-0060	Bracket, Terminal Mounting, Right	28480	02116-0060	1
02116-0063	Bracket, Terminal Board	28480	02116-0063	4
02116-0064	Terminal Board	28480	02116-0064	1
02116-0066	Shorting Bar	28480	02116-0066	2
02116-0067	Bus Bar	28480	02116-0067	1
02116-0068	Bus Bar	28480	02116-0068	1
02116-0069	Bus Bar	28480	02116-0069	1
02116-0073	Bus Bar, 4.5V	28480	02116-0073	1
02116-0074	Bus Bar Brace	28480	02116-0074	1
02116-0075	Bus Bar Brace	28480	02116-0075	1
02116-0077	Side Bracket	28480	02116-0077	2
02116-0078	Shield, Filter	28480	02116-0078	1
02116-0080	Subpanel	28480	02116-0080	1
02116-0085	Card Retainer	28480	02116-0085	2
02116-0087	Cable Spacer	28480	02116-0087	1
02116-0088	Filler Plate	28480	02116-0088	1
02116-0089	Top Panel	28480	02116-0089	1
02116-0090	Top Door Panel	28480	02116-0090	1
02116-0091	Resistor Bracket	28480	02116-0091	1
02116-0092	Bus Bar, 2V	28480	02116-0092	1
02116-0093	Bus Bar (End Output)	28480	02116-0093	1
02116-0100	Cover, Overvoltage Protection	28480	02116-0100	1
02116-0101	Subpanel	28480	02116-0101	1
02116-0102	Cable Clamp Bracket	28480	02116-0102	1
02116-0105	Fan Cover	28480	02116-0105	1

Table 6-20. Numerical Listing of Mechanical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR. CODE	MFR PART NO.	TQ
02116-2002	Slide Pin	28480	02116-2002	1
02116-2003	Eccentric Screw, No. 8	28480	02116-2003	2
02116-2009	Rear Brace	28480	02116-2009	3
02116-2010	Upper Slide	28480	02116-2010	1
02116-2011	Lower Slide	28480	02116-2011	1
02116-2012	Hinged Slide	28480	02116-2012	1
02116-2013	Support Bar	28480	02116-2013	1
02116-2014	Hinged Bar	28480	02116-2014	2
02116-2015	Bearing Shaft	28480	02116-2015	6
02116-2016	Hinged Pin	28480	02116-2016	1
02116-2017	Main Frame	28480	02116-2017	2
02116-2021	Horizontal Brace	28480	02116-2021	1
02116-2022	Vertical Brace	28480	02116-2022	1
02116-2023	Guide, Rod, Lower	28480	02116-2023	2
02116-2026	Horizontal Bracket	28480	02116-2026	1
02116-2027	Vertical Bracket	28480	02116-2027	1
02116-2032	Latch Retainer	28480	02116-2032	1
02116-2033	Catch Rod	28480	02116-2033	1
02116-2034	Tab Catch, Upper	28480	02116-2034	1
02116-2035	Bracket, Capacitor Board	28480	02116-2035	1
02116-2040	Bezel	28480	02116-2040	1
02116-2041	Front Brace, Bottom	28480	02116-2041	1
02116-2052	Bezel, Lower	28480	02116-2052	1
02116-2057	Foot, Cabinet	28480	02116-2057	4
02116-2058	Bracket, Capacitor Board	28480	02116-2058	1
02116-2059	Mounting Bar, Upper	28480	02116-2059	1
02116-2060	Mounting Bar, Front	28480	02116-2060	1
02116-2061	Mounting Bar, Rear	28480	02116-2061	1
02116-2063	Tab Catch, Lower	28480	02116-2063	1
02116-2064	Mounting Bar, Lower	28480	02116-2064	1
02116-2067	Guide, Rod, Upper	28480	02116-2067	1
02116-2068	Mount, Bus Bar	28480	02116-2068	2
02116-2069	Bakelite Spacer	28480	02116-2069	2
02116-2072	Support Bar	28480	02116-2072	1
02116-2075	PC Guide Support	28480	02116-2075	1
02116-2077	Front Brace, Top	28480	02116-2077	1
02116-2078	Vertical Brace	28480	02116-2078	1
02116-2079	Spacer	28480	02116-2079	1
02116-2080	Door Catch	28480	02116-2080	1
02116-4002	Light Mask	28480	02116-4002	1
02116-4007	PC Guide	28480	02116-4007	22
02116-6124	Power Supply and Back Panel Assembly	28480	02116-6124	1
02116-6287	Door Assembly	28480	02116-6287	1
02116-6295	Door Frame	28480	02116-6295	1
02116-8199	Indicator, Strip, Top	28480	02116-8199	1
02116-8200	Indicator, Strip, Middle	28480	02116-8200	1
02116-8201	Indicator, Strip, Bottom	28480	02116-8301	1
02116-8302	Negative Film	28480	02116-8302	1
02116-01103	Resistor Bracket	28480	02116-01103	1

Table 6-21. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 (Name to Code) and H4-2 (Code to Name) and their latest supplements. The date of revision and the date of the supplements used appear at the bottom of each page. Alphabetical codes have been arbitrarily assigned to suppliers not appearing in the H4 Handbooks.

Code No.	Manufacturer	Address
00000	U.S.A. Common	Any supplier of U.S.
00136	McCoy Electronics	Mount Holly Springs, Pa.
00213	Sage Electronics Corp.	Rochester, N.Y.
00287	Cemco Inc.	Danielson, Conn.
00334	Humidial	Colton, Calif.
00348	Microtron Co., Inc.	Valley Stream, N.Y.
00373	Garlock Inc.	Cherry Hill, N.J.
00656	Aerovox Corp.	New Bedford, Mass.
00779	Amp. Inc.	Harrisburg, Pa.
00781	Aircraft Radio Corp.	Boonton, N.J.
00815	Northern Engineering Laboratories, Inc.	Burlington, Wis.
00853	Sangamo Electric Co., Pickens Div.	Pickens, S.C.
00866	Goe Engineering Co.	City of Industry, Cal.
00891	Carl E. Holmes Corp.	Los Angeles, Calif.
00929	Microlab Inc.	Livingston, N.J.
01002	General Electric Co., Capacitor Dept.	Hudson Falls, N.Y.
01009	Alden Products Co.	Brockton, Mass.
01121	Allen Bradley Co.	Milwaukee, Wis.
01255	Litton Industries, Inc.	Beverly Hills, Calif.
01281	TRW Semiconductors, Inc.	Lawndale, Calif.
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas
01349	The Alliance Mfg. Co.	Alliance, Ohio
01589	Pacific Relays, Inc.	Van Nuys, Calif.
01670	Gudebrod Bros. Silk Co.	New York, N.Y.
01930	Amerock Corp.	Rockford, Ill.
01961	Pulse Engineering Co.	Santa Clara, Calif.
02114	Ferroxcube Corp. of America	Saugerties, N.Y.
02116	Wheelock Signals, Inc.	Long Branch, N.J.
02286	Cole Rubber and Plastics Inc.	Sunnyvale, Calif.
02660	Amphenol-Borg Electronics Corp.	Broadview, Ill.
02735	Radio Corp. of America, Semiconductor and Materials Div.	Somerville, N.J.
02771	Vocaline Co. of America, Inc.	Old Saybrook, Conn.
02777	Hopkins Engineering Co.	San Fernando, Calif.
02875	Hudson Tool & Die Co.	Newark, N.J.
03508	G.E. Semiconductor Prod. Dept.	Syracuse, N.Y.
03705	Apex Machine & Tool Co.	Dayton, Ohio
03797	Eldema Corp.	Compton, Calif.
03818	Parker Seal Co.	Los Angeles, Calif.
03877	Transitron Electric Corp.	Wakefield, Mass.
03888	Pyrofilm Resistor Co., Inc.	Cedar Knolls, N.J.
03954	Singer Co., Diehl Div. Finderne Plant	Sumerville, N.J.
04009	Arrow, Hart and Hegeman Elect. Co.	Hartford, Conn.
04013	Taurus Corp.	Lambertville, N.J.
04062	Arco Electronic Inc.	Great Neck, N.Y.
04222	Hi-Q Division of Aerovox	Myrtle Beach, S.C.
04354	Precision Paper Tube Co.	Wheeling, Ill.
04404	Dymec Division of Hewlett-Packard Co.	Palo Alto, Calif.
04651	Sylvania Electric Products, Microwave Device Div.	Mountain View, Calif.
04673	Dakota Engr. Inc.	Culver City, Calif.
04713	Motorola, Inc. Semiconductor Prod. Div.	Phoenix, Arizona
04732	Filtron Co., Inc. Western Div.	Culver City, Calif.
04773	Automatic Electric Co.	Northlake, Ill.
04796	Sequoia Wire Co.	Redwood City, Calif.
04811	Precision Coil Spring Co.	El Monte, Calif.
04870	P.M. Motor Company	Westchester, Ill.
04919	Component Mfg. Service Co.	W. Bridgewater, Mass.
05006	Twentieth Century Plastics, Inc.	Los Angeles, Calif.
05245	Components Corp.	Chicago, Ill.
05277	Westinghouse Electric Corp. Semi-Conductor Dept.	Youngwood, Pa.
05347	Ultronix, Inc.	San Mateo, Calif.
05397	Union Carbide Corp., Elect. Div.	New York, N.Y.
05574	Viking Ind. Inc.	Canoga Park, Calif.
05593	Icore Electro-Plastics Inc.	Sunnyvale, Calif.
05616	Cosmo Plastic (c/o Electrical Spec. Co.)	Cleveland, Ohio
05624	Barber Colman Co.	Rockford, Ill.
05728	Tiffen Optical Co.	Roslyn Heights, Long Island, N.Y.
05729	Metro-Tel Corp.	Westbury, N.Y.
05783	Stewart Engineering Co.	Santa Cruz, Calif.
05820	Wakefield Engineering Inc.	Wakefield, Mass.
06004	Bassick Co., Div. of Stewart Warner Corp.	Bridgeport, Conn.
06090	Raychem Corp.	Redwood City, Calif.
06175	Bausch and Lomb Optical Co.	Rochester, N.Y.
06402	E.T.A. Products Co. of America	Chicago, Ill.
06540	Amatom Electronic Hardware Co., Inc.	New Rochelle, N.Y.
06555	Beede Electrical Instrument Co., Inc.	Penacook, N.H.
06666	General Devices Co., Inc.	Indianapolis, Ind.
06751	Components Inc., Ariz. Div.	Phoenix, Ariz.
06812	Torrington Mfg. Co., West Div.	Van Nuys, Calif.
06980	Varian Assoc. Eimac Div.	San Carlos, Calif.
07088	Kelvin Electric Co.	Van Nuys, Calif.
07126	Digitran Co.	Pasadena, Calif.
07137	Transistor Electronics Corp.	Minneapolis, Minn.
07138	Westinghouse Electric Corp. Electronic Tube Div.	Elmira, N.Y.
07149	Filmohm Corp.	New York, N.Y.
07233	Cinch-Graphik Co.	City of Industry, Calif.
07256	Silicon Transistor Corp.	Carle Place, N.Y.
07261	Avnet Corp.	Culver City, Calif.
07263	Fairchild Camera & Inst. Corp. Semiconductor Div.	Mountain View, Calif.
07322	Minnesota Rubber Co.	Minneapolis, Minn.
07387	Birtcher Corp., The	Monterey Park, Calif.
07397	Sylvania Elect. Prod. Inc., Mt. View Operations	Mountain View, Calif.
07700	Technical Wire Products Inc.	Cranford, N.J.
07829	Bodine Elect. Co.	Chicago, Ill.
07910	Continental Device Corp.	Hawthorne, Calif.
07933	Raytheon Mfg. Co. Semiconductor Div.	Mountain View, Calif.
07980	Hewlett-Packard Co., Boonton Radio Div.	Rockaway, N.J.
08145	U.S. Engineering Co.	Los Angeles, Calif.
08289	Blinn, Delbert Co.	Pomona, Calif.
08358	Burgess Battery Co.	Niagara Falls, Ontario, Canada
08524	Deutsch Fastener Corp.	Los Angeles, Calif.
08664	Bristol Co., The	Waterbury, Conn.
08717	Sloan Company	Sun Valley, Calif.
08718	ITT Cannon Electric Inc., Phoenix Div.	Phoenix, Arizona
08727	National Radio Lab. Inc.	Paramus, N.J.
08792	CBS Electronics Semiconductor Operations, Div. of C.B.S. Inc.	Lowell, Mass.
08806	General Electric Co. Miniat. Lamp Dept.	Cleveland, Ohio
08984	Mel-Rain	Indianapolis, Ind.
09026	Babcock Relays Div.	Costa Mesa, Calif.
09134	Texas Capacitor Co.	Houston, Texas
09145	Tech. Ind. Inc. Atohm Elect.	Burbank, Calif.
09250	Electro Assemblies, Inc.	Chicago, Ill.
09353	C & K Components Inc.	Newton, Mass.
09569	Mallory Battery Co. of Canada, Ltd.	Toronto, Ontario, Canada
09922	Burndy Corp.	Norwalk, Conn.
10214	General Transistor Western Corp.	Los Angeles, Calif.
10411	Ti-Tal, Inc.	Berkeley, Calif.
10646	Carborundum Co.	Niagara Falls, N.Y.
11236	CTS of Berne, Inc.	Berne, Ind.
11237	Chicago Telephone of California, Inc.	So. Pasadena, Calif.
11242	Bay State Electronics Corp.	Waltham, Mass.
11312	Teledyne Inc., Microwave Div.	Palo Alto, Calif.
11314	National Seal	Downey, Calif.
11453	Precision Connector Corp.	Jamaica, N.Y.
11534	Duncan Electronics Inc.	Costa Mesa, Calif.
11711	General Instrument Corp., Semiconductor Div., Products Group	Newark, N.J.
11717	Imperial Electronic, Inc.	Buena Park, Calif.
11870	Melabs, Inc.	Palo Alto, Calif.
12040	National Semiconductor	Danbury, Conn.
12136	Philadelphia Handle Co.	Camden, N.J.
12361	Grove Mfg. Co., Inc.	Shady Grove, Pa.
12574	Gulton Ind. Inc. Data System Div.	Albuquerque, N.M.
12697	Clarostat Mfg. Co.	Dover, N.H.
12728	Elmar Filter Corp.	W. Haven, Conn.
12859	Nippon Electric Co., Ltd.	Tokyo, Japan
12881	Metex Electronics Corp.	Clark, N.J.
12930	Delta Semiconductor Inc.	Newport Beach, Calif.
12954	Dickson Electronics Corp.	Scottsdale, Arizona
13103	Thermolloy	Dallas, Texas
13396	Telefunken (GmbH)	Hanover, Germany
13835	Midland-Wright Div. of Pacific Industries, Inc.	Kansas City, Kansas
14099	Sem-Tech	Newbury Park, Calif.
14193	Calif. Resistor Corp.	Santa Monica, Calif.
14298	American Components, Inc.	Conshohocken, Pa.
14433	ITT Semiconductor, A Div. of Int. Telephone & Telegraph Corp.	West Palm Beach, Fla.
14493	Hewlett-Packard Company	Loveland, Colo.
14655	Cornell Dubilier Electric Corp.	Newark, N.J.
14674	Corning Glass Works	Corning, N.Y.
14752	Electro Cube Inc.	San Gabriel, Calif.
14960	Williams Mfg. Co.	San Jose, Calif.
15203	Webster Electronics Co.	New York, N.Y.
15287	Scionics Corp.	Northridge, Calif.
15291	Adjustable Bushing Co.	N. Hollywood, Calif.
15558	Micron Electronics	Garden City, Long Island, N.Y.
15566	Amprobe Inst. Corp.	Lynbrook, N.Y.
15631	Cabletronics	Costa Mesa, Calif.
15772	Twentieth Century Coil Spring Co.	Santa Clara, Calif.
15801	Fenwal Elect. Inc.	Framingham, Mass.
15818	Amelco Inc.	Mt. View, Calif.
16037	Spruce Pine Mica Co.	Spruce Pine, N.C.
16179	Omni-Spectra Inc.	Farmington, Mich.
16352	Computer Diode Corp.	Lodi, N.J.
16585	Boots Aircraft Nut Corp.	Pasadena, Calif.
16688	Ideal Prec. Meter Co., Inc. De Jur Meter Div.	Brooklyn, N.Y.
16758	Delco Radio Div. of G.M. Corp.	Kokoma, Ind.
17109	Thermonetics Inc.	Canoga Park, Calif.
17474	Tranex Company	Mountain View, Calif.
17554	Components Inc.	Biddeford, Ma.
17675	Hamlin Metal Products Corp.	Akron, Ohio
17745	Angstrohm Prec. Inc.	No. Hollywood, Calif.

In addition to the above:

Code No.	Manufacturer
01226	Vleir Engineering Corp, Santa Clara, Calif.
01686	RCL Electronics Inc., Manchester, N.H.
02763	Grippe Machining & Mfg. Co., Roseville, Mich
13061	Wilco Products, Detroit, Mich.

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Table 6-21. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address
17870	McGraw-Edison Co.	Manchester, N.H.
18042	Power Design Pacific Inc.	Palo Alto, Calif.
18083	Clevite Corp., Semiconductor Div.	Palo Alto, Calif.
18324	Signetics Corp.	Sunnyvale, Calif.
18476	Ty-Car Mfg. Co., Inc.	Holliston, Mass.
18486	TRW Elect. Comp. Div.	Des Plaines, Ill.
18583	Curtis Instrument, Inc.	Mt. Kisco, N.Y.
18612	Vishay Instruments Inc.	Malvern, Pa.
18873	E.I. DuPont and Co., Inc.	Wilmington, Del.
18911	Durant Mfg. Co.	Milwaukee, Wis.
19315	The Bendix Corp., Navigation & Control Div.	Teterboro, N.J.
19500	Thomas A. Edison Industries, Div. of McGraw-Edison Co.	West Orange, N.J.
19589	Concoa	Baldwin Park, Calif.
19644	LRC Electronics	Horseheads, N.Y.
19701	Electra Mfg. Co.	Independence, Kansas
20183	General Atronics Corp.	Philadelphia, Pa.
21226	Executone, Inc.	Long Island City, N.Y.
21335	Fafnir Bearing Co., The	New Britain, Conn.
21520	Fansteel Metallurgical Corp.	N. Chicago, Ill.
23042	Texscan Corp.	Indianapolis, Ind.
23783	British Radio Electronics Ltd.	Washington, D.C.
24455	G.E. Lamp Division	Nela Park, Cleveland, Ohio
24655	General Radio Co.	West Concord, Mass.
24681	Memcor Inc., Comp. Div.	Huntington, Ind.
24796	Parelco Inc.	San Juan Capistrano, Calif.
26365	Gries Reproducer Corp.	New Rochelle, N.Y.
26462	Grobet File Co. of America, Inc.	Carlstadt, N.J.
26851	Compac Hollister Co.	Hollister, Calif.
26992	Hamilton Watch Co.	Lancaster, Pa.
27251	Specialities Mfg. Co., Inc.	Stratford, Conn.
28480	Hewlett-Packard Co.	Palo Alto, Calif.
28520	Heyman Mfg. Co.	Kenilworth, N.J.
30817	Instrument Specialties Co., Inc.	Little Falls, N.J.
33173	G.E. Receiving Tube Dept.	Owensboro, Ky.
35434	Lectrohm Inc.	Chicago, Ill.
36196	Stanwyck Coil Products Ltd.	Hawkesbury, Ontario, Canada
36287	Cunningham, W.H. & Hill, Ltd.	Toronto Ontario, Canada
37942	P.R. Mallory & Co. Inc.	Indianapolis, Ind.
39543	Mechanical Industries Prod. Co.	Akron, Ohio
40920	Miniature Precision Bearings, Inc.	Keene, N.H.
42190	Muter Co.	Chicago, Ill.
43990	C.A. Norgren Co.	Englewood, Colo.
44655	Ohmite Mfg. Co.	Skokie, Ill.
46384	Penn Eng. & Mfg. Corp.	Doylestown, Pa.
47904	Polaroid Corp.	Cambridge, Mass.
48620	Precision Thermometer & Inst. Co.	Southampton, Pa.
49956	Microwave & Power Tube Div.	Waltham, Mass.
52090	Rowan Controller Co.	Westminster, Md.
52983	Sanborn Company	Waltham, Mass.
54294	Shallcross Mfg. Co.	Selma, N.C.
55026	Simpson Electric Co.	Chicago, Ill.
55933	Sonotone Corp.	Elmsford, N.Y.
55938	Raytheon Co. Commercial Apparatus & Systems Div.	So. Norwalk, Conn.
56137	Spaulding Fibre Co., Inc.	Tonawanda, N.Y.
56289	Sprague Electric Co.	North Adams, Mass.
59446	Telex Corp.	Tulsa, Okla.
59730	Thomas & Betts Co.	Elizabeth, N.J.
60741	Triplett Electrical Inst. Co.	Bluffton, Ohio
61775	Union Switch and Signal, Div. of Westinghouse Air Brake Co.	Pittsburgh, Pa.
62119	Universal Electric Co.	Owosso, Mich.
63743	Ward-Leonard Electric Co.	Mt. Vernon, N.Y.
64959	Western Electric Co., Inc.	New York, N.Y.
65092	Weston Inst. Inc. Weston-Newark	Newark, N.J.
66295	Wittek Mfg. Co.	Chicago, Ill.
66346	Minnesota Mining & Mfg. Co. Revere Mincom Div.	St. Paul, Minn.
70276	Allen Mfg. Co.	Hartford, Conn.
70309	Allied Control	New York, N.Y.
70318	Allmetal Screw Product Co., Inc.	Garden City, N.Y.
70417	Amplex, Div. of Chrysler Corp.	Detroit, Mich.
70485	Atlantic India Rubber Works, Inc.	Chicago, Ill.
70563	Amperite Co., Inc.	Union City, N.J.
70674	ADC Products Inc.	Minneapolis, Minn.
70903	Belden Mfg. Co.	Chicago, Ill.
70998	Bird Electronic Corp.	Cleveland, Ohio
71002	Birnbach Radio Co.	New York, N.Y.
71034	Bliley Electric Co., Inc.	Erie, Pa.
71041	Boston Gear Works Div. of Murray Co. of Texas	Quincy, Mass.
71218	Bud Radio, Inc.	Willoughby, Ohio
71279	Cambridge Thermionics Corp.	Cambridge, Mass.
71286	Camloc Fastener Corp.	Paramus, N.J.
71313	Cardwell Condenser Corp.	Lindenhurst L.I., N.Y.
71400	Bussmann Mfg. Div. of McGraw-Edison Co.	St. Louis, Mo.
71436	Chicago Condenser Corp.	Chicago, Ill.
71447	Calif. Spring Co., Inc.	Pico-Rivera, Calif.
71450	CTS Corp.	Elkhart, Ind.
71468	ITT Cannon Electric Inc.	Los Angeles, Calif.
71471	Cinema, Div. Aerovox Corp.	Burbank, Calif.
71482	C.P. Clare & Co.	Chicago, Ill.
71590	Centralab Div. of Globe Union Inc.	Milwaukee, Wis.
71616	Commercial Plastics Co.	Chicago, Ill.
71700	Cornish Wire Co., The	New York, N.Y.
71707	Coto Coil Co., Inc.	Providence, R.I.
71744	Chicago Miniature Lamp Works	Chicago, Ill.
71785	Cinch Mfg. Co., Howard B. Jones Div.	Chicago, Ill.
71984	Dow Corning Corp.	Midland, Mich.
72136	Electro Motive Mfg. Co., Inc.	Willimantic, Conn.
72619	Dialight Corp.	Brooklyn, N.Y.
72656	Indiana General Corp., Electronics Div.	Keasby, N.J.
72699	General Instrument Corp., Cap. Div.	Newark, N.J.
72765	Drake Mfg. Co.	Harwood Heights, Ill.
72825	Hugh H. Eby Inc.	Philadelphia, Pa.
72928	Gudeman Co.	Chicago, Ill.
72962	Elastic Stop Nut Corp.	Union, N.J.
72964	Robert M. Hadley Co.	Los Angeles, Calif.
72982	Erie Technological Products, Inc.	Erie, Pa.
73061	Hansen Mfg. Co., Inc.	Princeton, Ind.
73076	H.M. Harper Co.	Chicago, Ill.
73138	Helipot Div. of Beckman Inst., Inc.	Fullerton, Calif.
73293	Hughes Products Division of Hughes Aircraft Co.	Newport Beach, Calif.
73445	Amperex Elect Co.	Hicksville, L.I., N.Y.
73506	Bradley Semiconductor Corp.	New Haven, Conn.
73559	Carling Electric, Inc.	Hartford, Conn.
73586	Circle F Mfg. Co.	Trenton, N.J.
73682	George K. Garrett Co., Div. MSL Industries Inc.	Philadelphia, Pa.
73734	Federal Screw Products Inc.	Chicago, Ill.
73743	Fischer Special Mfg. Co.	Cincinnati, Ohio
73793	General Industries Co., The	Elyria, Ohio
73846	Goshen Stamping & Tool Co.	Goshen, Ind.
73899	JFD Electronics Corp.	Brooklyn, N.Y.
73905	Jennings Radio Mfg. Corp.	San Jose, Calif.
73957	Groov-Pin Corp.	Ridgefield, N.J.
74276	Signalite Inc.	Neptune, N.J.
74455	J.H. Winns, and Sons	Winchester, Mass.
74861	Industrial Condenser Corp.	Chicago, Ill.
74868	R.F. Products Division of Amphenol-Borg Electronics Corp.	Danbury, Conn.
74970	E.F. Johnson Co.	Waseca, Minn.
75042	International Resistance Co.	Philadelphia, Pa.
75263	Keystone Carbon Co., Inc.	St. Marys, Pa.
75378	CTS Knights Inc.	Sandwich, Ill.
75382	Kulka Electric Corporation	Mt. Vernon, N.Y.
75818	Lenz Electric Mfg. Co.	Chicago, Ill.
75915	Littlefuse, Inc.	Des Plaines, Ill.
76005	Lord Mfg. Co.	Erie, Pa.
76210	C.W. Marwedel	San Francisco, Calif.
76433	General Instrument Corp., Micamold Division	Newark, N.J.
76487	James Millen Mfg. Co., Inc.	Malden, Mass.
76493	J.W. Miller Co.	Los Angeles, Calif.
76530	Cinch-Monadnock, Div. of United Carr Fastener Corp.	San Leandro, Calif.
76545	Mueller Electric Co.	Cleveland, Ohio
76703	National Union	Newark, N.J.
76854	Oak Manufacturing Co.	Crystal Lake, Ill.
77068	The Bendix Corp., Electrodynamics Div.	N. Hollywood, Calif.
77075	Pacific Metals Co.	San Francisco, Calif.
77221	Phanostran Instrument and Electronic Co.	South Pasadena, Calif.
77252	Philadelphia Steel and Wire Corp.	Philadelphia, Pa.
77342	American Machine & Foundry Co. Potter & Brumfield Div.	Princeton, Ind.
77630	TRW Electronic Components Div.	Camden, N.J.
77638	General Instrument Corp., Rectifier Div.	Brooklyn, N.Y.
77764	Resistance Products Co.	Harrisburg, Pa.
77969	Rubbercraft Corp. of Calif.	Torrance, Calif.
78189	Shakeproof Division of Illinois Tool Works	Elgin, Ill.
78277	Sigma	So. Braintree, Mass.
78283	Signal Indicator Corp.	New York, N.Y.
78290	Struthers-Dunn Inc.	Pitman, N.J.
78424	Speciality Leather Prod. Co.	Newark, N.J.
78452	Thompson-Bremer & Co.	Chicago, Ill.
78471	Tilley Mfg. Co.	San Francisco, Calif.
78488	Stackpole Carbon Co.	St. Marys, Pa.
78493	Standard Thomson Corp.	Waltham, Mass.
78553	Tinnerman Products, Inc.	Cleveland, Ohio
78790	Transformer Engineers	San Gabriel, Calif.
78947	Ucinite Co.	Newtonville, Mass.
79136	Waldes Kohinoor Inc.	Long Island City, N.Y.
79142	Veeder Root, Inc.	Hartford, Conn.
79251	Wenco Mfg. Co.	Chicago, Ill.
79727	Continental-Wirt Electronics Corp.	Philadelphia, Pa.
79963	Zierick Mfg. Corp.	New Rochelle, N.Y.
80031	Mepco Division of Sessions Clock Co.	Morristown, N.J.
80120	Schnitzer Alloy Products Co.	Elizabeth, N.J.
80131	Electronic Industries Association. Any brand Tube meeting EIA Standards-Washington, DC.	
80207	Unimax Switch, Div. Maxon Electronics Corp.	Wallingford, Conn.
80223	United Transformer Corp.	New York, N.Y.
80248	Oxford Electric Corp.	Chicago, Ill.
80294	Bourns Inc.	Riverside, Calif.
80411	Acro Div. of Robertshaw Controls Co.	Columbus, Ohio

In addition to the above:

23936 Pamotor Inc., San Francisco, Calif.

74842 Illinois Lock Co., Wheeling, Ill.

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Table 6-21. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address
80486	All Star Products Inc.	Defiance, Ohio
80509	Avery Label Co.	Monrovia, Calif.
80583	Hammarlund Co., Inc.	Mars Hill, N.C.
80640	Stevens, Arnold, Co., Inc.	Boston, Mass.
80813	Dimco Gray Co.	Dayton, Ohio
81030	International Instruments Inc.	Orange, Conn.
81073	Grayhill Co.	LaGrange, Ill.
81095	Triad Transformer Corp.	Venice, Calif.
81312	Winchester Elec. Div. Litton Ind., Inc.	Oakville, Conn.
81349	Military Specification	. . . . . .
81483	International Rectifier Corp.	El Segundo, Calif.
81541	Airpax Electronics, Inc.	Cambridge, Maryland
81860	Barry Controls, Div. Barry Wright Corp.	Watertown, Mass.
82042	Carter Precision Electric Co.	Skokie, Ill.
82047	Sperti Faraday Inc., Copper Hewitt Electric Div.	Hoboken, N.J.
82116	Electric Regulator Corp.	Norwalk, Conn.
82142	Jeffers Electronics Division of Speer Carbon Co.	Du Bois, Pa.
82170	Fairchild Camera & Inst. Corp. Space & Defense System Div.	Paramus, N.J.
82209	Maguire Industries, Inc.	Greenwich, Conn.
82219	Sylvania Electric Prod. Inc. Electronic Tube Division	Emporium, Pa.
82376	Astron Corp.	East Newark, Harrison, N.J.
82389	Switchcraft, Inc.	Chicago, Ill.
82647	Metals & Controls Inc. Spencer Products	Attleboro, Mass.
82768	Phillips-Advance Control Co.	Joliet, Ill.
82866	Research Products Corp.	Madison, Wis.
82877	Rotron Mfg. Co., Inc.	Woodstock, N.Y.
82893	Vector Electronic Co.	Glendale, Calif.
83014	Hartwell Corp.	Los Angeles, Calif.
83058	Carr Fastener Co.	Cambridge, Mass.
83086	New Hampshire Ball Bearing, Inc.	Peterborough, N.H.
83125	General Instrument Corp., Capacitor Div.	Darlington, S.C.
83148	ITT Wire and Cable Div.	Los Angeles, Calif.
83186	Victory Eng. Corp.	Springfield, N.J.
83298	Bendix Corp., Red Bank Div.	Red Bank, N.J.
83315	Hubbell Corp.	Mundelein, Ill.
83324	Rosan Inc.	Newport Beach, Calif.
83330	Smith, Herman H., Inc.	Brooklyn, N.Y.
83332	Tech Labs	Palisade's Park, N.J.
83385	Central Screw Co.	Chicago, Ill.
83501	Gavitt Wire and Cable Co. Div. of Amerace Corp.	Brookfield, Mass.
83594	Burroughs Corp. Electronic Tube Div.	Plainfield, N.J.
83740	Union Carbide Corp. Consumer Prod. Div.	New York, N.Y.
83777	Model Eng. and Mfg., Inc.	Huntington, Ind.
83821	Loyd Scruggs Co.	Festus, Mo.
83942	Aeronautical Inst. & Radio Co.	Lodi, N.J.
84171	Arco Electronics Inc.	Great Neck, N.Y.
84396	A.J. Glesener Co., Inc.	San Francisco, Calif.
84411	TRW Capacitor Div.	Ogallala, Neb.
84970	Sarkes Tarzian, Inc.	Bloomington, Ind.
85454	Boonton Molding Company	Boonton, N.J.
85471	A.B. Boyd Co.	San Francisco, Calif.
85474	R.M. Bracamonte & Co.	San Francisco, Calif.
85660	Koiled Kords, Inc.	Hamden, Conn.
85911	Seamless Rubber Co.	Chicago, Ill.
86174	Fafnir Bearing Co.	Los Angeles, Calif.
86197	Clifton Precision Products Co., Inc.	Clifton Heights, Pa.
86579	Precision Rubber Products Corp.	Dayton, Ohio
86684	Radio Corp. of America, Electronic Comp. & Devices Div.	Harrison, N.J.
86928	Seastrom Mfg. Co.	Glendale, Calif.
87034	Marco Industries	Anaheim, Calif.
87216	Philco Corporation (Lansdale Division)	Lansdale, Pa.
87473	Western Fibrous Glass Products Co.	San Francisco, Calif.
87664	Van Waters & Rogers Inc.	San Francisco, Calif.
87930	Tower Mfg. Corp.	Providence, R.I.
88140	Cutler-Hammer, Inc.	Lincoln, Ill.
88220	Gould-National Batteries, Inc.	St. Paul, Minn.
88698	General Mills, Inc.	Buffalo, N.Y.
89231	Graybar Electric Co.	Oakland, Calif.
89473	G.E. Distributing Corp.	Schenectady, N.Y.
89665	United Transformer Co.	Chicago, Ill.
90030	United Shoe Machinery Corp.	Beverly, Mass.
90179	US Rubber Co., Consumer Ind. & Plastics Prod. Div.	Passaic, N.J.
90970	Bearing Engineering Co.	San Francisco, Calif.
91146	ITT Cannon Elect, Inc., Salem Div.	Salem, Mass.
91260	Connor Spring Mfg. Co.	San Francisco, Calif.
91345	Miller Dial & Nameplate Co.	El Monte, Calif.
91418	Radio Materials Co.	Chicago, Ill.
91506	Augat Inc.	Attleboro, Mass.
91637	Dale Electronics, Inc.	Columbus, Nebr.
91662	Elco Corp.	Willow Grove, Pa.
91737	Gremar Mfg. Co., Inc.	Wakefield, Mass.
91827	K F Development Co.	Redwood City, Calif.
91886	Malco Mfg. Co., Inc.	Chicago, Ill.
91929	Honeywell Inc., Micro Switch Div.	Freeport, Ill.
91961	Nahm-Bros. Spring Co.	Oakland, Calif.
92180	Tru-Connector Corp.	Peabody, Mass.
92367	Elgeet Optical Co. Inc.	Rochester, N.Y.
92607	Tensolite Insulated Wire Co., Inc.	Tarrytown, N.Y.
92702	IMC Magnetics Corp.	Wesbury Long Island, N.Y.
92966	Hudson Lamp Co.	Kearney, N.J.
93332	Sylvania Electric Prod. Inc. Semiconductor Div.	Woburn, Mass.
93369	Robbins & Myers Inc.	Palisades Park, N.J.
93410	Stemco Controls, Div. of Essex Wire Corp.	Mansfield, Ohio
93632	Waters Mfg. Co.	Culver City, Calif.
93929	G.V. Controls	Livingston, N.J.
94137	General Cable Corp.	Bayonne, N.J.
94142	Phelps Dodge	Yonkers, N.Y.
94144	Raytheon Co., Comp. Div., Ind. Comp. Operations	Quincy, Mass.
94148	Scientific Electronics Products, Inc.	Loveland, Colo.
94154	Wagner Elect. Corp., Tung-Sol Div.	Newark, N.J.
94197	Curtiss-Wright Corp. Electronics Div.	East Paterson, N.J.
94222	South Chester Corp.	Chester, Pa.
94330	Wire Cloth Products, Inc.	Bellwood, Ill.
94375	Automatic Metal Products Co.	Brooklyn, N.Y.
94682	Worcester Pressed Aluminum Corp.	Worcester, Mass.
94696	Magnecraft Electric Co.	Chicago, Ill.
95023	George A. Philbrick Researchers, Inc.	Boston, Mass.
95236	Allies Products Corp.,	Dania, Fla.
95238	Continental Connector Corp.	Woodside, N.Y.
95263	Leecraft Mfg. Co., Inc.	Long Island, N.Y.
95265	National Coil Co.	Sheridan, Wyo.
95275	Vitramon, Inc.	Bridgeport, Conn.
95348	Gordos Corp.	Bloomfield, N.J.
95354	Methode Mfg. Co.	Rolling Meadows, Ill.
95566	Arnold Engineering Co.	Marengo, Ill.
95712	Dage Electric Co., Inc.	Franklin, Ind.
95984	Siemon Mfg. Co.	Wayne, Ill.
95987	Weckesser Co.	Chicago, Ill.
96067	Microwave Assoc., West Inc.	Sunnyvale, Calif.
96095	Hi-Q Div. of Aerovox Corp.	Olean, N.Y.
96256	Thordarson-Meissner Inc.	Mt. Carmel, Ill.
96296	Solar Manufacturing Co.	Los Angeles, Calif.
96306	Microswitch, Div. of Minn.-Honeywell	Freeport, Ill.
96330	Carlton Screw Co.	Chicago, Ill.
96341	Microwave Associates, Inc.	Burlington, Mass.
96501	Excel Transformer Co.	Oakland, Calif.
96733	San Fernando Elect. Mfg. Co.	San Fernando, Calif.
96881	Thomson Ind. Inc.	Long Is., N.Y.
97464	Industrial Retaining Ring Co.	Irvington, N.J.
97539	Automatic & Precision Mfg.	Englewood, N.J.
97979	Reon Resistor Corp.	Yonkers, N.Y.
97983	Litton System Inc., Adler-Westrex Commun. Div.	New Rochelle, N.Y.
98141	R-Troncis, Inc.	Jamaica, N.Y.
98159	Rubber Teck, Inc.	Gardena, Calif.
98220	Hewlett-Packard Co., Moseley Div.	Pasadena, Calif.
98278	Microdot, Inc.	So. Pasadena, Calif.
98291	Sealectro Corp.	Mamaroneck, N.Y.
98376	Zero Mfg. Co.	Burbank, Calif.
98410	Etc Inc.	Cleveland, Ohio
98731	General Mills Inc., Electronics Div.	Minneapolis, Minn.
98734	Paeco Div. of Hewlett-Packard Co.	Palo Alto, Calif.
98821	North Hills Electronics, Inc.	Glen Cove, N.Y.
98978	International Electronic Research Corp.	Burbank, Calif.
99109	Columbia Technical Corp.	New York, N.Y.
99313	Varian Associates	Palo Alto, Calif.
99378	Atlee Corp.	Winchester, Mass.
99515	Marshall Ind., Capacitor Div.	Monrovia, Calif.
99707	Control Switch Division, Controls Co. of America	El Segundo, Calif.
99800	Delevan Electronics Corp.	East Aurora, N.Y.
99848	Wilco Corporation	Indianapolis, Ind.
99928	Branson Corp.	Whippany, N.J.
99934	Renbrandt, Inc.	Boston, Mass.
99942	Hoffman Electronics Corp. Semiconductor Div.	El Monte, Calif.
99957	Technology Instrument Corp. of Calif.	Newbury Park, Calif.

THE FOLLOWING HP VENDORS HAVE NO NUMBER ASSIGNED IN THE LATEST SUPPLEMENT TO THE FEDERAL SUPPLY CODE FOR MANUFACTURERS HANDBOOK.

Code No.	Manufacturer	Address
0000F	Malco Tool and Die	Los Angeles, Calif.
0000Z	Willow Leather Products Corp.	Newark, N.J.
000AB	ETA	England
000BB	Precision Instrument Components Co.	Van Nuys, Calif.
000CS	Hewlett-Packard Co., Colorado Springs	Colorado Springs, Colorado
000MM	Rubber Eng. & Development	Hayward, Calif.
000NN	A "N" D Mfg. Co.	San Jose, Calif.
000QQ	Cooltron	Oakland, Calif.
000WW	California Eastern Lab.	Burlington, Calif.
000YY	S.K. Smith Co.	Los Angeles, Calif.

In addition to the above: 90095 Technitrol Inc., Philadelphia Pa.

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APPENDIX A

BASIC LOGIC SYMBOLS

A-1. GENERAL CLASSIFICATIONS.

A-2. Three basic symbol shapes distinguish the major classes of logic circuits. These classes are gates, regenerative switching elements, and amplifiers. Each symbol, and a brief explanation of its operation, is given below. Additional markings on the basic symbols provide additional information, making possible the determination of actual circuit operation.

A-3. INVERSION.

A-4. Logic inversion is indicated by an inversion dot at the input or output of a logic symbol. When this dot appears at the input of a logic symbol, the input will be effective when the input signal is of the opposite polarity to that normally required. When the dot appears at the output of a logic symbol, the output will be of the opposite polarity to that normally delivered.

A-5. GATES.

A-6. A gate is a circuit which produces a binary output when certain input conditions are met. The gate symbol has input lines connecting to the flat side of the symbol, and output lines connecting to the curved side (see Figure A-1). Since the inputs and outputs are easily identifiable, the symbol may be shown left-facing, right-facing, or facing up or down. There are four basic types of gates, "and", "or", "nand", and "nor", each named for the logic function that it performs. Each of these gates is described below.

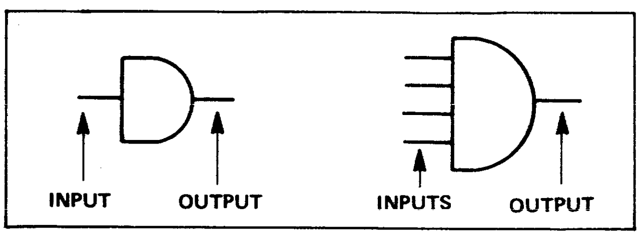

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Figure A-1. Gate Symbols

A-7. "AND" GATE.

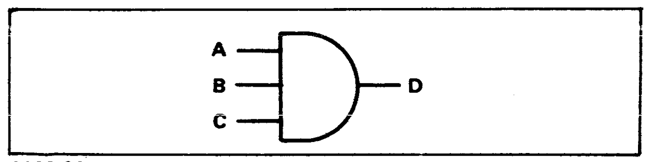
A-8. The "and" gate performs a logical "and" function. It will produce a logical-true output only when all of its input lines are true. Input A and input B and input C must be true for a true output to be generated. See Figure A-2 and Table A-1.

A-9. "OR" GATE.

A-10. The "or" gate performs a logical "or" function. It will produce a logical-true output if one or more of its input lines are true. Input A or input B or input C must be true for a true output to be generated. See Figure A-3 and Table A-2.

A-11. "NAND" GATE.

A-12. The "nand" gate is similar to the "and" gate described above except that its output is inverted. The gate will generate a logical-true output if one or more of its inputs is false. See Figure A-4 and Table A-3.

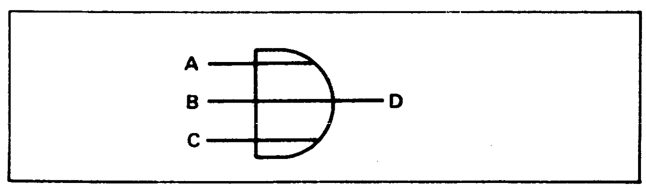


2039-26

Figure A-2. Three Input "And" Gate

Table A-1. Truth Table For Three Input "And" Gate

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

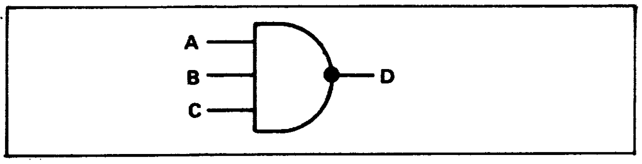


2039-27

Figure A-3. Three Input "Or" Gate

Table A-2. Truth Table For Three Input "Or" Gate

A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



2039-28

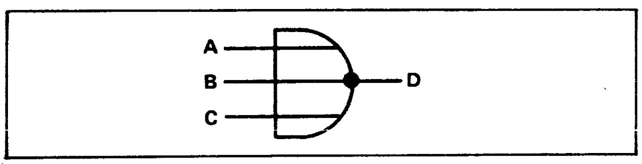
Figure A-4. Three Input "Nand" Gate

Table A-3. Truth Table for Three Input "Nand" Gate

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

A-13. "NOR" GATE.

A-14. The "nor" gate is similar to the "or" gate described above except that its output is inverted. The gate will generate a logical-false if one or more of its input lines is true. See Figure A-5 and Table A-4.



2039-29

Figure A-5. Three Input "Nor" Gate

Table A-4. Truth Table for Three Input "Nor" Gate

A	B	C	D
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

A-15. EXPANDER GATES.

A-16. To increase the number of inputs to logic gates an expander gate is used. To simplify the presentation of a logic gate with an expanded input the symbols shown in Figure A-6 are used. Figure A-7 shows the actual logic configuration. The X and $\overline{X}$ lines are not logical opposites but do carry a voltage differential. When the expander gate is not conducting (the input conditions A, B, or C false) there is a voltage differential of a few volts across the outputs X and $\overline{X}$. When the expander gate is conducting (the input conditions A, B, and C being true) the differential between the two outputs drops. The two outputs of the expander then act as a true input to the expanded gate. When more than one expander gate is used the expander gate outputs are tied in parallel as shown in Figure A-7.

A-17. REGENERATIVE SWITCHING ELEMENTS.

A-18. Regenerative switching elements include the various forms of multivibrator circuits: bistable (flip-flop), monostable (one-shot), and astable (multivibrator). According to the type of circuit, inputs cause the state of the circuit to switch, reversing the outputs (i.e., an output formerly true switches to false, and vice versa). The symbol for regenerative switching circuits is a horizontal rectangle, divided horizontally, with the upper portion representing the "set side" and the lower portion representing the "clear side". A switching element is said to be "set" when the output from the set side is true. It is "clear" when the output from the clear side is true. Inputs are on the left and outputs are on the right (see Figure A-8). To avoid confusion, these switching elements are always drawn facing the same way.

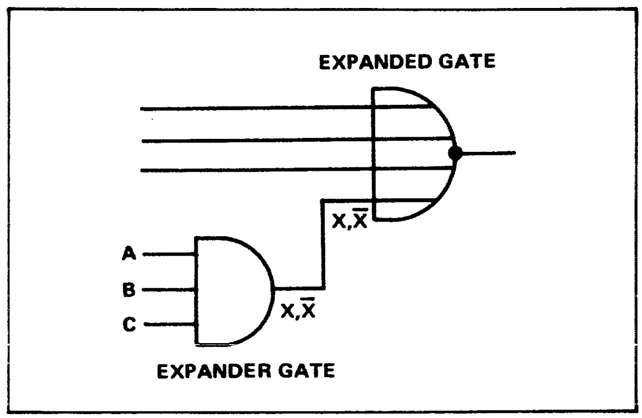


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Figure A-6. Simplified Expander Gate

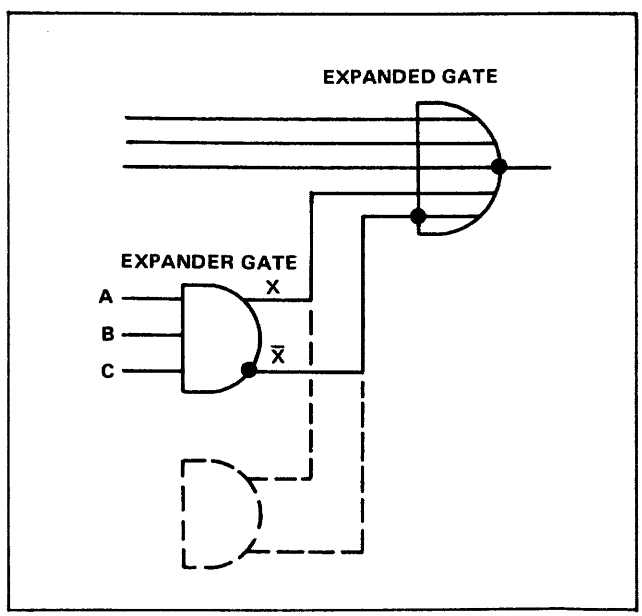

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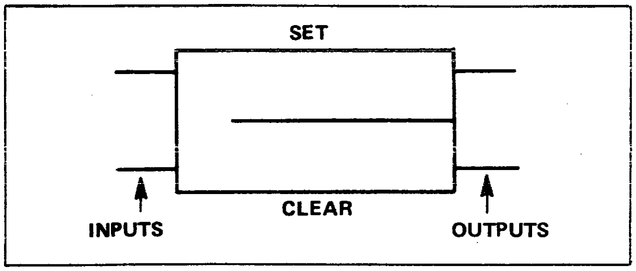
Figure A-7. Actual Expander Gate



2039-32

Figure A-8. Switching Element

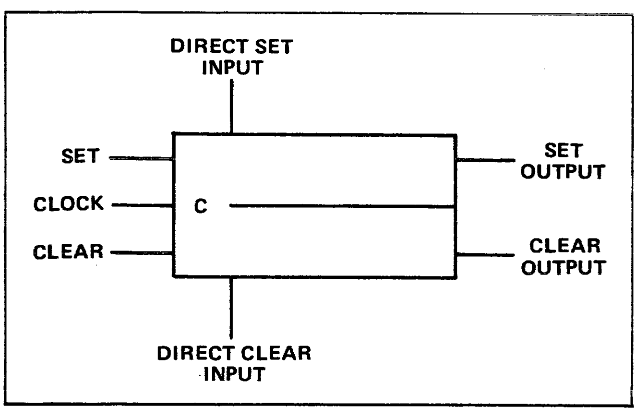
A-19. FLIP-FLOPS.

A-20. A flip-flop is a bistable switching device, meaning that it takes an external signal to set the flip-flop, and another to clear it. It will remain in its current state until switched to the opposite state by the appropriate external signal. Various forms of flip-flops exist, of which six are described here. The R-S, R-S with clock, J-K, toggle, latch, and delay flip-flops are shown below with their individual switching characteristics. The rules governing the representation of flip-flops allow the type of flip-flop used to be identified. General rules for flip-flops are as follows:

a. A flip-flop is assumed to be the simple R-S type if no other identification information is provided. When a clock input is added, identifying letters are placed inside the symbol to tell what kind of flip-flop the device is.

b. An input shown connected to the center of the input side of the symbol is a "clock" input, parallel-connected to both the set and clear inputs. This input is effective on the transition of the clocking signal; i.e., on the positive going or negative going edge of the clock pulse. No inversion dot indicates that the input is effective on the positive going edge of the clock pulse, while an inverting dot indicates that the input is effective on the negative going edge of the clock pulse (see Figure A-9).

c. An input to the top of the flip-flop at the input end indicates a direct set input. This input provides a preset or direct set to the flip-flop and operates independently of the flip-flop's clocking signal. An input to the bottom of the flip-flop at the input end indicates a direct clear input. The direct clear allows the flip-flop to be cleared independently of the flip-flop's clocking signal.

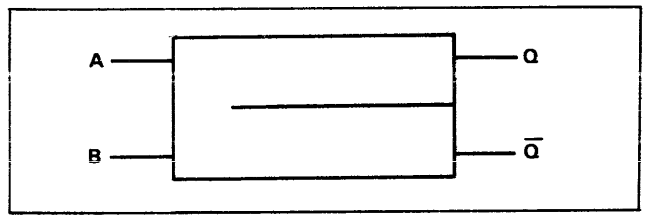


2039-33

Figure A-9. Flip-Flop (General)

A-21. R-S FLIP-FLOP.

A-22. The R-S flip-flop has a minimum of two inputs, set and clear (A and B), and usually two outputs, set output and clear output (Q and $\bar{Q}$), see Figure A-10. The $\bar{Q}$ letter indicates that the clear output, whether a 1 or a 0, is always the complement of the set output. When Q is true, then $\bar{Q}$ is false and the flip-flop is defined as being in the set state. With Q false and $\bar{Q}$ true, the flip-flop is in the clear state. The flip-flop is set by a true input to A (assuming no inversion dot on the symbol), and is cleared by a true input to B. False inputs have no effect. Simultaneous true inputs to A and B are a forbidden combination, since an indeterminate output state would result. A truth table for the three allowable input combinations is shown in Table A-5.



2039-34

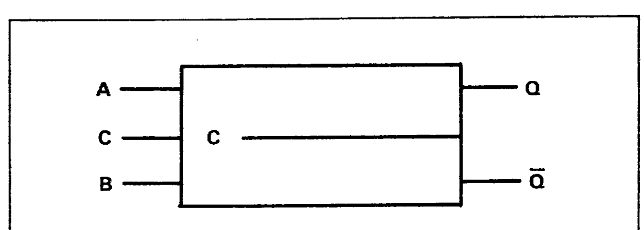
Figure A-10. R-S Flip-Flop

Table A-5. Truth Table for R-S Flip-Flop

A	B	Q	$\bar{Q}$
0	0	No Change	
1	0	1	0
0	1	0	1

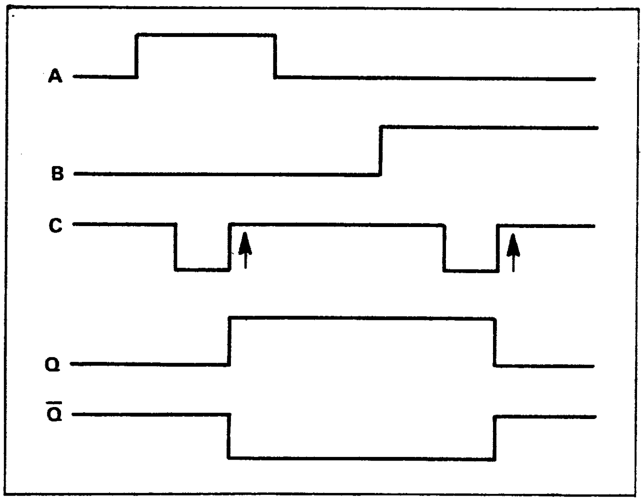
A-23. R-S FLIP-FLOP WITH CLOCK.

A-24. This flip-flop is the same as the R-S type described in the preceding paragraph, except for the addition of a clock input (see Figure A-11). A positive input to both A and C is required to set the flip-flop, and a positive input to B and C is required to clear the flip-flop. Since the clock input operates on a pulse edge, the setting or clearing signals must be present at A or B before the clock pulse transition occurs (see Figure A-12).



2039-35

Figure A-11. R-S Flip-Flop with Clock



2039-36

Figure A-12. Clocked R-S Flip-Flop Switching Waveforms

A-25. When the R-S flip-flop is used with an inverted clock input, the flip-flop switches on the negative going transition of the clock pulse (see paragraph A-20b). The symbol for an R-S flip-flop with an inverted clock is shown in Figure A-13, and the resulting switching waveforms are shown in Figure A-14.

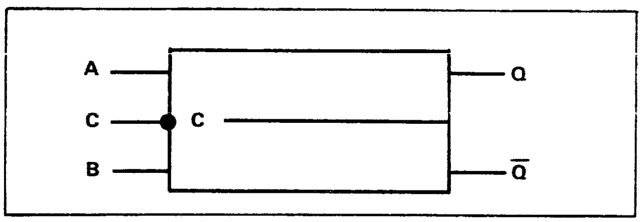


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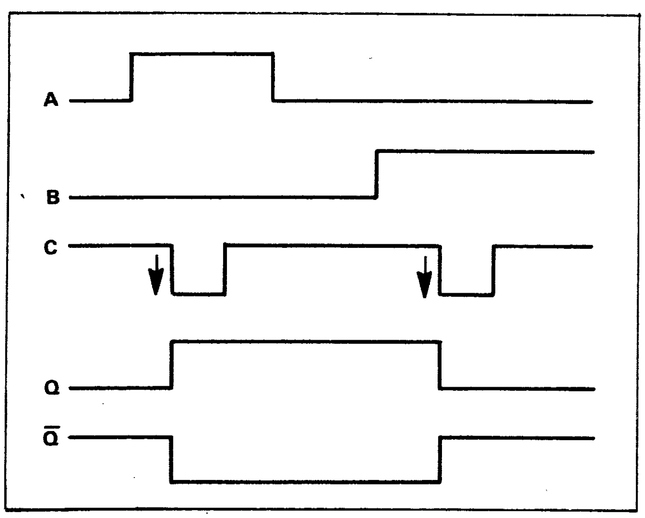
Figure A-13. R-S Flip-Flop with Inverted Clock

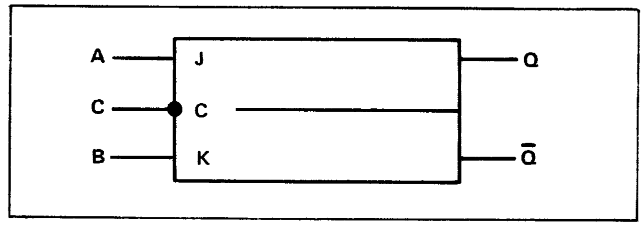


2039-38

Figure A-14. Waveforms for R-S Flip-Flop with Inverted Clock

A-26. J-K FLIP-FLOP.

A-27. In the J-K flip-flop, simultaneous true inputs for both set and clear will reverse the existing state of the flip-flop. This requires some method of storing two conditions, the previous output state and the new output state, until the clock pulse time. The set and clear inputs are labeled J and K respectively. Two flip-flops are combined in a dual-rank configuration to provide the output storage, together with the necessary gates to form a single logic element. For simplicity the internal dual-rank arrangement of the flip-flop is not usually shown (see Figure A-15 and Table A-6). The overall operation of a J-K flip-flop with a dot on the clock input is as follows:



2019-301

Figure A-15. J-K Flip-Flop

Table A-6. Truth Table For Clocked J-K Flip-Flop

A	B	Initial State		Final State	
		Q	$\overline{Q}$	Q	
1	0			1	0
0	1			0	1
1	1	0	1	1	0
1	1	1	0	0	1
0	0			No Change	

a. True input at A only. The positive-going edge of clock pulse C stores input information A in the input-rank flip-flop. The negative-going edge of the clock pulse then transfers the information to the output-rank flip-flop.

b. True input at B only. The positive-going edge of clock pulse C stores input information B in the input-rank flip-flop. The negative-going edge of the clock pulse clears the output-rank flip-flop.

c. True inputs at A and B. The positive-going edge of clock pulse C stores input information A B. The negative-going edge of the clock pulse switches the existing state of the output-rank flip-flop.

A-28. TOGGLE FLIP-FLOP.

A-29. The toggle flip-flop is distinguished by having a single input. Each time input A goes true, outputs Q and $\overline{Q}$ switch states. Since two input pulses or cycles are required to produce one complete cycle of the output, the toggle flip-flop acts as a divide-by-two element, and is commonly used in counting circuits. The letter T inside the symbol identifies the toggle flip-flop. Figures A-16 and A-17 show the symbol and switching waveforms for a toggle flip-flop.

A-30. For a toggle flip-flop with an inverted input at A the flip-flop would switch on the negative going transition of A (see Figures A-18 and A-19).

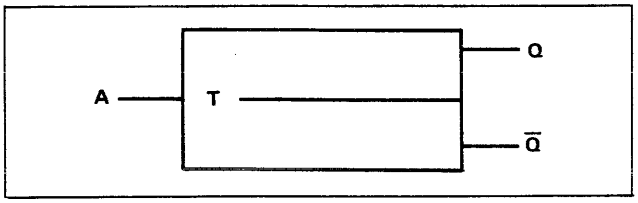


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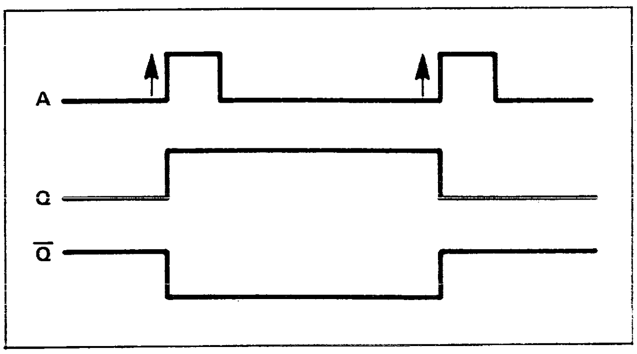
Figure A-16. Toggle Flip-Flop



2039-41

Figure A-17. Toggle Flip-Flop Switching Waveforms

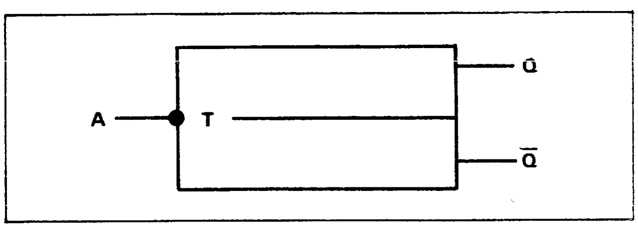


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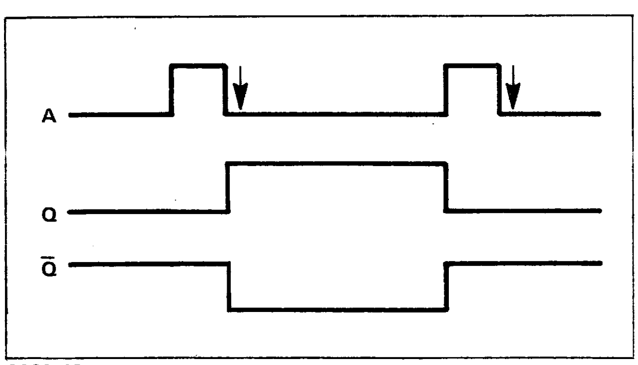
Figure A-18. Toggle Flip-Flop with Inverted Clock



2039-43

Figure A-19. Switching Waveforms for Toggle Flip-Flop with Inverted Clock

A-31. LATCHING FLIP-FLOP.

A-32. The latching flip-flop has a single signal input and a clock input. The flip-flop is identified by the letter L inside the symbol as shown (see Figure A-20). Note that the set input is responsive to positive signal levels at A, and the clear input is responsive to negative signal levels at A. When the clock input is true, the output will "follow" the input. When the clock input is false, the output is "latched" to the input state present when the clock went false. (See Figure A-21).

A-33. DELAY FLIP-FLOP.

A-34. The delay flip-flop has a single data input and a clock input. The flip-flop is identified by the letter "D" inside the symbol as shown in Figure A-22. The flip-flop performs two functions: it stores the input data and sets the output of the flip-flop. The delay flip-flop differs from the latch flip-flop previously defined in that it performs the storing and setting functions on the same edge of the clock pulse. In the example shown in Figure A-23 the flip-flop sets on the leading or true going edge of the clock pulse.

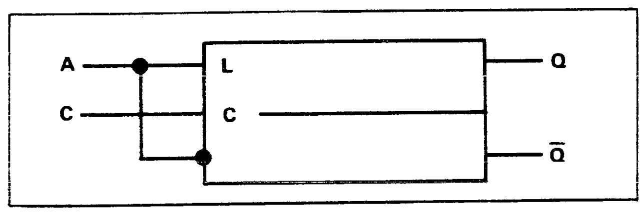


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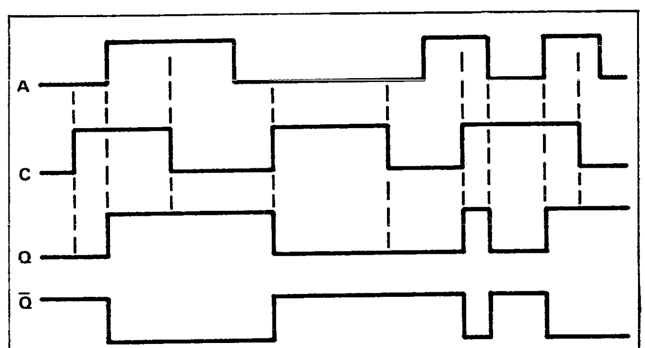
Figure A-20. Latching Flip-Flop



2039-45

Figure A-21. Latching Flip-Flop Waveforms

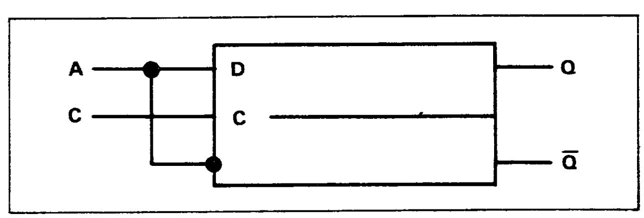


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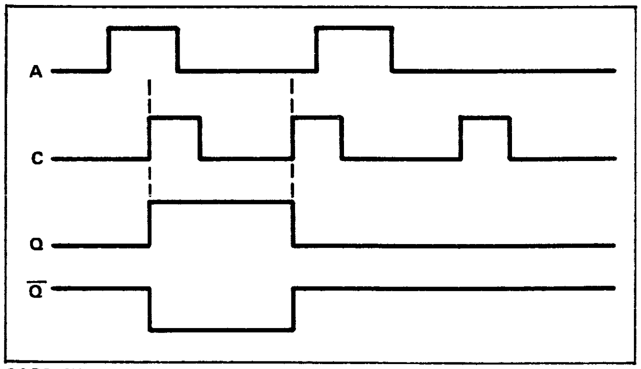
Figure A-22. Delay Flip-Flop

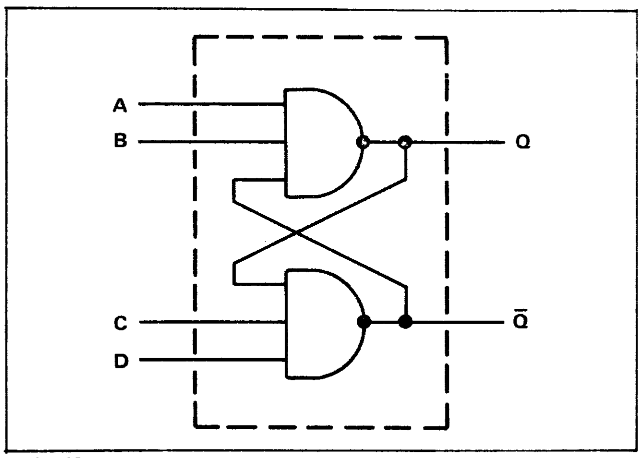


2039-47

Figure A-23. Delay Flip-Flop Switching Waveforms

A-35. GATE FLIP-FLOP.

A-36. The gate flip-flop is made up of a combination of logic gates. When the gates are connected as shown in Figure A-24 they form a storage or switching element. In the example shown the flip-flop will be set by a false input at either A or B. The flip-flop will be cleared by a false input at either C or D. The gate flip-flop is normally used in such a manner that a false input does not occur at the set and clear inputs simultaneously. The gate flip-flop may be made up of several combinations of logic gates, each with its own switching properties. The gate flip-flop is usually shown with the set output at the upper right and the clear output at the lower right. Another version of the gate flip-flop uses two "nor" gates, rather than two "nand" gates. In the "nor" gate version the flip-flop is set or cleared by a true input.



2039-48

Figure A-24. Gated Flip-Flop

A-37. AMPLIFIERS.

A-38. Amplifiers are not necessarily binary in nature; however, in logic circuits the driving signals will normally be binary and the output of the amplifier will be an amplified or modified form of the binary input. The amplifier symbol is an equilateral triangle with the input applied to the center of one side, and the output connected to the opposite point of the triangle (see Figure A-25). Like gates, the amplifier may be shown in any of four positions.

A-39. A variation of the amplifier, in the form of a dual input/output (differential amplifier) is shown in Figure A-26. An inversion dot would indicate the inversion of an output with respect to the corresponding input.

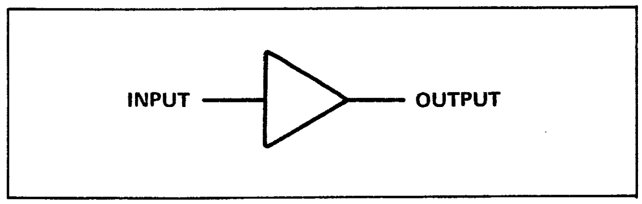


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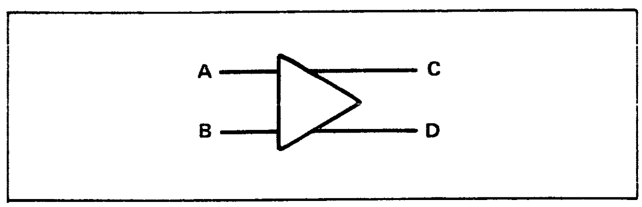
Figure A-25. Amplifier Symbol



2039-49

Figure A-26. Differential Amplifier

A-40. INTEGRATED CIRCUIT CHARACTERISTICS AND DIAGRAMS.

A-41. Contained in Table A-7 is a list of integrated circuit operating characteristics. This list is keyed to the integrated circuit diagrams illustrated in Figure A-27. The circuit diagrams are shown in numerical order of Hewlett-Packard part number. Each circuit diagram has a characteristic number which identifies a particular operating characteristic in Table A-7.

Table A-7. Integrated Circuit Characteristics

Characteristic	Input Level		Output Level		Open Input Acts As:	Propagation Delay (Max)	
	Logic 1 (Volts, Min)	Logic 0 (Volts, Max)	Logic 1 (Volts, Min)	Logic 0 (Volts, Max)		To 1 (Nanosec)	To 0 (Nanosec)
1	+2.0	+0.8	+2.4	+0.4	Logic 1	15	15
2	+2.0	+0.8	+2.4	+0.4	Logic 1	29	15
3	+2.0	+0.8	+2.4	+0.4	Logic 1	12	10
15	+1.25	+0.5	+2.35	- 0.36	Logic 0	14	12
16	+1.8	+0.0	+1.5	+0.22	Logic 0	4.5	4.0
17	+1.25	+0.5	+2.25	- 0.36	Logic 0	18	18
18	+1.33*	+0.5	+2.35	- 0.36	Logic 0	15	25
21	+1.8V	+0.0	+2.0	- 0.16	Logic 0	25**	25**
27†	—	—	—	—	—	—	—
32	+1.25	+0.5	+2.35	- 0.36	Logic 0	8	8
33	+2.0	+0.8	+2.4	+0.4	Logic 1	11	11

NOTES:
* +1.25 volts for pins 3 and 6.
** 4 nanoseconds through pins 8 and 14.
† Voltage gain: 40 decibels, typical.
Voltages and propagation delays listed in the table are applicable at temperature of 25° C (76° F).

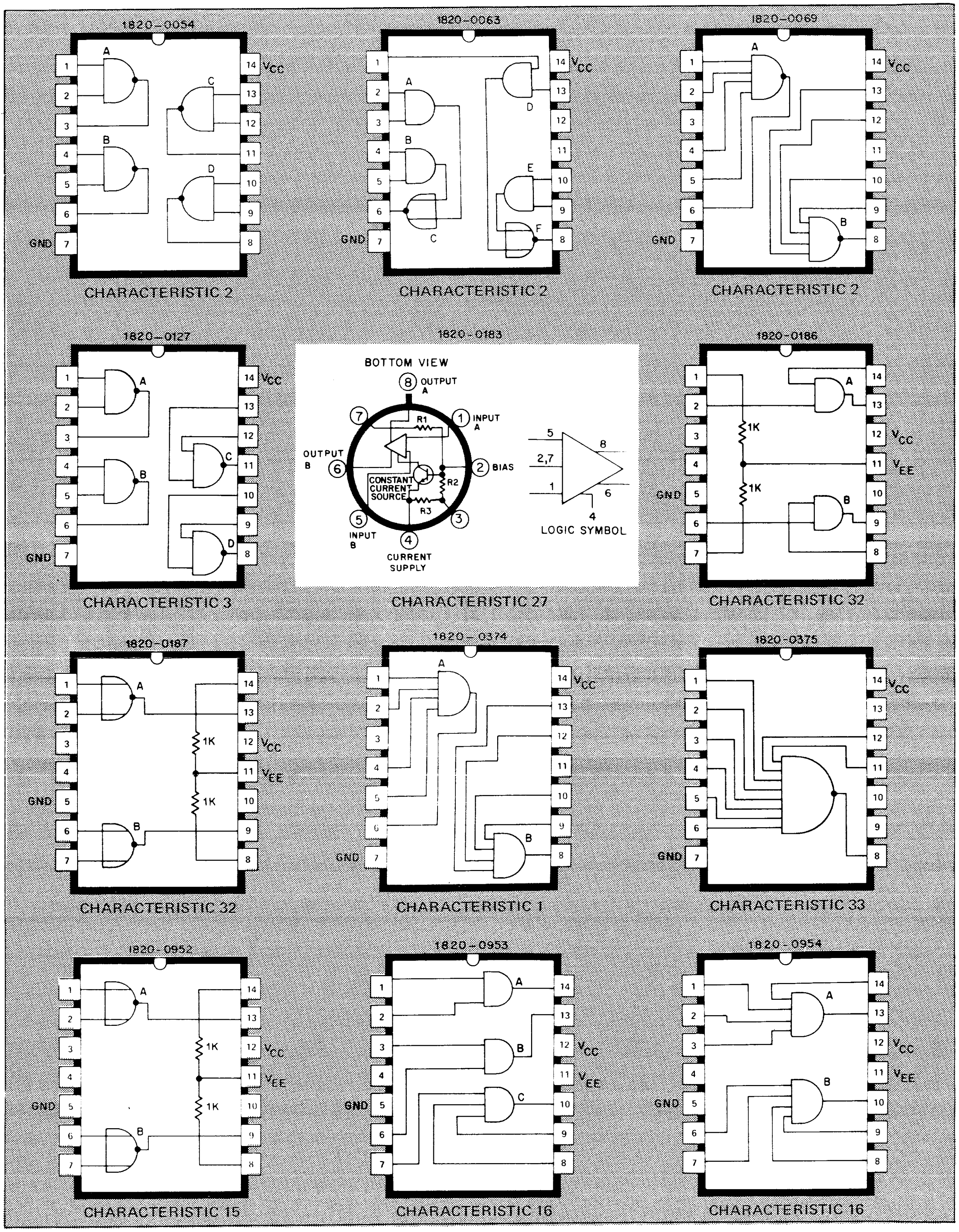


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Figure A-27. Integrated Circuit Diagrams (Sheet 1 of 2)

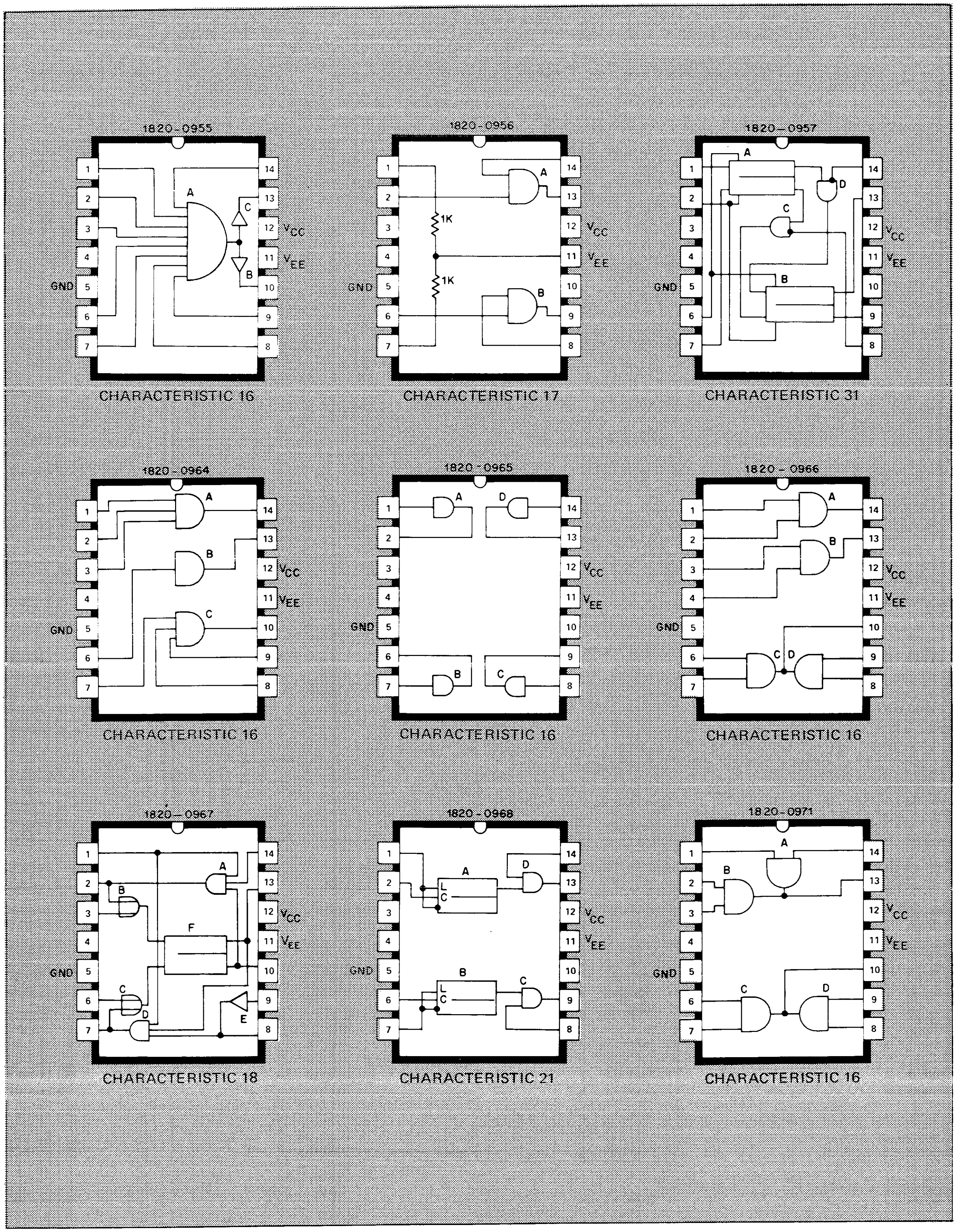

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Figure A-27. Integrated Circuit Diagrams (Sheet 2 of 2)

APPENDIX B

BACKDATING INFORMATION

B-1. INTRODUCTION.

B-2. This appendix provides the backdating information needed in adapting this manual for use with computers having serial number prefixes assigned prior to 944-. By incorporating the applicable backdating changes into the manual, the manual will correctly document the computer it accompanies.

CAUTION

The information presented in this appendix is intended only for use in making required backdating changes to the manual. Do not attempt to use this information for the purpose of making any changes to the computer hardware. To do so may result in damage to or improper operation of the computer.

B-3. DETERMINING EFFECTIVITY.

B-4. Table B-1 lists the serial number prefixes to which this backdating information is applicable, and specifies the computer configurations the prefixes identify. The encircled numbers within the table are the backdating change numbers affecting the manual. Backdating change numbers are listed in numerical order in table B-2 which summarizes the effectivity of each backdating change and details the specific changes to be made to the manual.

B-5. The prefix and configuration information listed in table B-1 reflects computer prefixes and configurations as originally manufactured and shipped from factory to field. Because of field modifications, repairs, board exchange, and other factors that may have since altered the shipped configurations, the configurations presently existing in the field may not always agree with the information presented in table B-1. For this reason it will be necessary to check each of the assemblies currently installed in a given computer to determine the extent to which the information in tables B-1 and B-2 applies. (Refer to the "Identification" paragraph in Section I of this manual for information required when making this check.) In cases where serial number prefixes, assembly part numbers, or revision codes differ from those in table B-1, consult the nearest Hewlett-Packard Sales and Service Office for required backdating information.

B-6. MAKING CHANGES TO THE MANUAL.

B-7. After determining which backdating change numbers are applicable to the computer, refer to table B-2 and make the required changes to the manual. The change information may be entered by hand, directly on the affected page, if space permits. If more convenient, enter the change number on a conspicuous part of the affected page to serve as a "flag" when making future reference to that page of the manual. The "Backdating" pages furnished with this appendix should be removed from this part of the manual and inserted in the area of the manual specified in table B-2.

Table B-1. Computer Configurations

SERIAL PREFIX NO.	COMPUTER ASSEMBLIES																
	A1	A2	A12, A13	A14, A15	A16, A18	A20	A101	A102 thru A105	A106	A107	A108	A121 and A121/A1	A201*	A202*	A218*	POWER SUPPLY	BACKPLANE
823–	02116-6175 REV. C-821-6 2 11	02116-6274 REV. A-811-6 5	02115-6001 REV. G-744-6 5	02116-6266 REV. A-817-6 7	02116-6265 REV. A-819-6	02115-6044 REV. A-821-6 5	02116-6208 REV. D-805-6 10	02116-6026 REV. L-805-6	02116-6281 REV. A-818-6 4 9	02116-6027 REV. K-822-6	02116-6029 REV. K-729-6	02116-6284 A1, 02116-6126 REV. C-714-6 OR REV. C-848-6 8	02116-6041 REV. L-839-6	02116-6194 REV. B-829-6	02116-6047 REV. B-701-6	6	1 3 4 5
824–	02116-6175 REV. C-821-6 2 11	02116-6274 REV. A-811-6 5	02115-6001 REV. G-744-6 5	02116-6266 REV. A-817-6 7	02116-6265 REV. A-819-6	02115-6044 REV. A-821-6 5	02116-6208 REV. D-805-6 10	02116-6026 REV. L-805-6	02116-6281 REV. A-818-6 4 9	02116-6027 REV. J-822-6	02116-6029 REV. K-729-6	02116-6126 REV. C-714-6 OR REV. C-848-6 8	02116-6041 REV. L-839-6	02116-6194 REV. B-824-6 OR REV. C-829-6	02116-6047 REV. B-701-6	6	1 3 4 5
842–	02116-6175 REV. C-821-6 2 11	02116-6274 REV. A-811-6 5	02115-6001 REV. G-744-6 5	02116-6266 REV. A-817-6 7	02116-6265 REV. A-819-6	02115-6044 REV. A-821-6 5	02116-6208 REV. D-805-6 10	02116-6026 REV. L-805-6	02116-6281 REV. A-818-6 4 9	02116-6027 REV. K-830-6	02116-6029 REV. K-729-6	02116-6126 REV. C-714-6 OR REV. D-837-6 8	02116-6041 REV. L-839-6	02116-6194 REV. C-829-6	02116-6047 REV. B-701-6	6	1 3 4 5
846–	02116-6175 REV. D-821-6 2 11	02116-6274 REV. A-811-6 5	02115-6001 REV. G-744-6 5	02116-6266 REV. A-817-6 7	02116-6265 REV. A-819-6	02115-6044 REV. A-821-6 5	02116-6208 REV. D-805-6 10	02116-6026 REV. L-805-6	02116-6281 REV. A-818-6 4 9	02116-6027 REV. K-830-6	02116-6029 REV. K-729-6	02116-6126 REV. C-714-6 OR REV. D-837-6 8	02116-6041 REV. L-839-6	02116-6194 REV. C-829-6	02116-6047 REV. B-701-6	6	3 4 5
850–	02116-6175 REV. D-821-6 11	02116-6274 REV. A-811-6 OR 02116-6300 REV. A-844-22 5	02115-6001 REV. G-744-6 5	02116-6266 REV. A-817-6 7	02116-6265 REV. A-819-6	02115-6044 REV. A-821-6 5	02116-6208 REV. D-805-6 10	02116-6026 REV. L-805-6	02116-6281 REV. A-818-6 4 9	02116-6027 REV. K-830-6	02116-6029 REV. K-729-6	02116-6126 REV. C-714-6 OR REV. D-837-6 8	02116-6041 REV. L-839-6	02116-6194 REV. C-829-6	02116-6047 REV. B-701-6	6	5
852–	02116-6175 REV. D-821-6 11	02116-6274 REV. A-811-6 5	02115-6001 REV. G-744-6 5	02116-6266 REV. A-817-6 7	02116-6265 REV. A-819-6	02115-6044 REV. A-821-6 5	02116-6208 REV. D-805-6 10	02116-6026 REV. L-805-6	02116-6281 REV. A-818-6 OR REV. A-912-22 4 9	02116-6027 REV. K-830-6	02116-6029 REV. K-729-6	02116-6126 REV. C-714-6 OR REV. D-837-6 8	02116-6041 REV. L-839-6	02116-6194 REV. C-829-6	02116-6047 REV. B-701-6	6	5
905–	02116-6175 REV. D-821-6 11	02116-6274 REV. A-811-6 OR 02116-6300 REV. A-844-22 5	02115-6001 REV. G-744-6 OR 02116-6298 REV. A-902-22 5	02116-6266 REV. A-817-6 OR REV. A-903-22 7	02116-6265 REV. A-819-6	02115-6044 REV. H-905-6 OR REV. J-905-6 OR REV. J-907-22	02116-6208 REV. D-805-6 10	02116-6026 REV. L-805-6	02116-6281 REV. A-818-6 OR REV. A-912-22 9	02116-6027 REV. K-830-6	02116-6029 REV. K-729-6	02116-6126 REV. D-837-6 8	02116-6041 REV. L-839-6	02116-6194 REV. C-829-6	02116-6047 REV. B-701-6	6	NO CHANGE
912–	02116-6175 REV. D-821-6 11	02116-6300 REV. A-844-22 12	02116-6298 REV. A-902-22	02116-6366 REV. A-903-22 7	02116-6265 REV. A-819-6	02116-6069** REV. J-905-6 OR REV. J-907-22	02116-6208 REV. D-805-6 10	02116-6026 REV. L-805-6	02116-6281 REV. A-818-6 OR REV. A-912-22 9	02116-6027 REV. K-830-6	02116-6029 REV. K-729-6	02116-6126 REV. D-837-6 8	02116-6041 REV. L-839-6	02116-6194 REV. C-829-6	02116-6097 REV. B-701-6	NO CHANGE	NO CHANGE
914–	02116-6175 REV. D-821-6 OR REV. D-925-22 11	02116-6300 REV. A-844-22 OR REV. A-937-22 12	02116-6298 REV. A-902-22	02116-6266 REV. A-903-22 7	02116-6265 REV. A-819-6	02116-6069** REV. J-905-6 OR REV. J-907-22	02116-6208 REV. D-805-6 OR REV. D-942-22 10	02116-6026 REV. L-805-6	02116-6281 REV. A-912-22 OR REV. B-923-22 9	02116-6027 REV. K-830-6	02116-6029 REV. K-729-6	02116-6126 REV. D-837-6 8	02116-6041 REV. L-839-6	02116-6194 REV. C-829-6	02116-6047 REV. B-701-6 OR REV. B-920-22	NO CHANGE	NO CHANGE
944–	02116-6175 REV. D-925-22	02116-6300 REV. A-937-22	02116-6298 REV. A-902-22	02116-6266 REV. B-943-22	02116-6265 REV. A-819-6	02116-6069 REV. J-907-22	02116-6208 REV. D-942-22	02116-6026 REV. L-805-6	02116-6281 REV. B-923-22	02116-6027 REV. K-830-6	02116-6029 REV. K-729-6	02116-6126 REV. D-837-6	02116-6041 REV' L-839-6	02116-6194 REV. C-829-6	02116-6047 REV. B-701-6 OR REV. B-920-22	NO CHANGE	NO CHANGE

*Refer to Volume Three for specific information regarding these assemblies.

**Revisions H-905-6, J-905-6, and J-907-6 are electrically identical. Only the revision numbers are different.

Table B-2. Backdating Manual Changes

CHANGE NO.	COMPUTER SERIAL NUMBER PREFIX	REQUIRED MANUAL CHANGE
1	823- or 824-	Make the following backplane wiring changes in table 5-8. a. Delete pin 73 from slot 118 at reference number 110 (T6T7). b. Add pin 73 to slot 118 at reference number 122 (T6). c. Delete pin 59 from slot 117 at reference number 469 (TSA).
2	823- 824- or 842-	Make the following changes: a. Incorporate change 11 of this appendix. b. In figure 5-8, delete the ground connections to pins 5 and 7 of MC25. c. At the upper-left corner of figures 5-7 and 5-8, change the card revision to "C-821-6."
3	823- 824- 842- or 846-	In table 5-8, make the backplane wiring changes listed in table B-3 of this appendix.
4	823- 824- 842- 846- or 850-	Make the following changes: a. Table 5-8. Delete pin 53 from slot 117 at reference number 245 (SIR). b. Figures 5-23 and 5-24. Incorporate change 9 of this appendix. Then, delete capacitor C12 and change the card revision to "A-818-6." c. Table 5-17. Delete the entry for reference designation C12. d. Table 6-19. Change the TQ for part number 0140-0225 from "2" to "1."
5	823- 824- 842- 846- 850- 852- or 905-	Note Change "d" following does not apply to computers with serial number prefixes 850- and 905-. Change "e" following does not apply to computers with serial number prefix 905-. Make the following changes: a. Table 1-1. At designation A2, add "or 02116-6274." b. Following page 5-40 of the manual, add pages 5-40A through 5-40C/5-40D of this appendix. c. Table 6-4, index number 2. Change the HP and MFR part numbers to 02116-6274 and the figure reference to 5-9B. d. At the applicable reference slot numbers of table 5-8, make the backplane wiring corrections listed in table B-3 of this appendix. e. Table 1-1. At designation A20, delete "02116-6069" and add "02115-6044."

Table B-2. Backdating Manual Changes (Continued)

CHANGE NO.	COMPUTER SERIAL NUMBER PREFIX	REQUIRED MANUAL CHANGE
5 (Cont)		f. Following page 5-54 of the manual, add pages 5-54A through 5-54C/5-54D of this appendix. g. Table 6-4, index number 6. Change the HP and MFR part numbers to 02115-6044 and the figure reference to 5-17B. Note Changes "h," "i," "j," and "k" following may or may not apply to computers with serial number prefix 905-. Check the assembly installed in the computer before changing the manual. h. Table 1-1. At designation A12, A13, delete "02116-6298" and add "02115-6001." i. Insert pages 5-8A, 5-8B, and 5-8C/5-8D (attached to the back of this appendix) between pages 5-8 and 5-9 of the manual. j. Following page 5-50 of the manual, add pages 5-50A through 5-50E/5-50F of this appendix. k. Table 6-4, index number 3. Change the HP and MFR part numbers to 02115-6001 and the figure reference to 5-15B.
6	823- 824- 842- 846- 850- 852- or 905-	Make the following changes: a. Figures 5-41 and 5-44. Delete reference designation "R23" and "A310R23." b. Table 5-32. Delete the entry for reference designation R23. c. Table 6-10 and figure 6-10. Delete the entry for index number 19 (R23). d. Table 6-19. Delete the entry for part number 0811-2648.
7	823- 824- 842- 846- 850- 852- 905- 912- or 914-	Make the following changes: a. Figures 5-13 and 5-14 and table 5-12. Delete reference designations "C44" and "C45" and change the value of resistors R6, R13, R20, R27, R34, R41, R48, and R55, to 5.6 ohms. Change the card revision to "A-903-22." Change the reference designation index information for the above listed resistors to show HP part number 0683-0565; value, 5.6 ohms; manufacturers part number CB 0565. b. Table 6-19. Delete the entry for part number 0180-1735. Change the entry for part number 0683-0275 to show part number 0683-0565; value, 5.6 ohms; manufacturers part number, CB 0565.

Note

Determine whether the following information given in change numbers 8 through 14 is applicable to the assemblies installed in the computer before changing the manual.

Table B-2. Backdating Manual Changes (Continued)

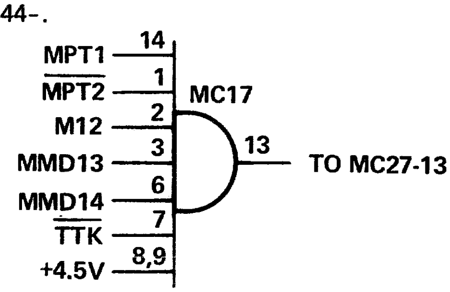
CHANGE NO.	COMPUTER SERIAL NUMBER PREFIX	REQUIRED MANUAL CHANGE
8	(As applicable, see note above)	For overvoltage protection assemblies with revision C-714-6 of assembly A121/A1, incorporate the following changes: a. Figures 5-29, 5-30, and 5-31. Remove components C1 through C7 from the 02116-6126 board and show them as part of the 02116-6284 mechanical assembly with the same electrical connections. Change the 02116-6126 board revision to "C-714-6."
9	(As applicable; see note above)	For timing generator card A106, incorporate the following changes: a. Figures 5-23 and 5-24. Delete the load resistors MC113R1 and MC123R1 from the T1 signal lead. Change the card revision to "A-912-22."
10	(As applicable; see note above)	For front panel coupler card A101, incorporate the following changes: a. Figures 5-19 and 5-20 and table 5-15. Delete the reference designation C3 and change the card revision to "D-805-6." b. Table 6-19. At the entry for part number 0160-0154, change the amount shown in the TQ column to read "8."
11	(As applicable; see note above)	For power fail interrupt card A1, incorporate the following changes: a. Figures 5-7 and 5-8. Change the value of R17 to 2.2K and the card revision to "D-821-6." b. Table 5-9. Change the information at reference designation R17 as follows: part number 0680-2225; value 2.2k; manufacturers code 01121; manufacturers part number EB2225. c. Table 6-19. At the entry for part number 0686-2215, change the TQ from 2 to "1." Also add the following: 0686-2225; Resistor, Fxd, Comp, 2.2K, 5%, 1/2W; 01121; EB2225; in the applicable columns.
12	(As applicable; see note above)	For A2 memory module decoder card (02116-6300, revision A-844-22, incorporate the following changes: a. Table 5-10. Add reference designation MC17; 1820-0955; Integrated Circuit; CTL; 07263; SL3458. b. Figure 5-9. Add integrated circuit symbol in upper-right corner of diagram labeled MC17. Change the revision number to A-844-22. c. Figure 5-10. Add the following integrated circuit diagram and change the card revision to 844–. 

Table B-3. Backplane Wiring Changes

TERMINATIONS DELETED		
REF	SIGNAL	TERMINATIONS
2	-12V	A13-65, A13-66, A12-65, A12-66, A11-65, A11-66, A10-65, A10-66
6	M0	A221-24
7	M1	A221-25
8	M2	A221-28
9	M3	A221-38
10	M4	A221-50
11	M5	A221-53
12	M6	A222-24
13	M7	A222-25
14	M8	A222-28
15	M9	A222-38
16	M10	A222-50
17	M11	A222-53
18	M12	A222-56, A222-65, A221-26, A221-62
92	MIT	A221-58
94	MRT	A222-58
111	MST	A221-22
124	MWT	A222-83
126	$\overline{\text{TR3}}$	A221-67
130	$\overline{\text{TR2}}$	A221-74
133	$\overline{\text{TR1}}$	A221-72
138	$\overline{\text{TR0}}$	A221-68
144	$\overline{\text{TR7}}$	A221-82
148	$\overline{\text{TR6}}$	A221-80
151	$\overline{\text{TR5}}$	A221-76
156	$\overline{\text{TR4}}$	A221-77
161	$\overline{\text{TR11}}$	A222-67
165	$\overline{\text{TR10}}$	A222-74
168	$\overline{\text{TR9}}$	A222-72
173	$\overline{\text{TR8}}$	A222-68
179	$\overline{\text{TR15}}$	A222-82
182	$\overline{\text{TR14}}$	A222-80
185	$\overline{\text{TR13}}$	A222-76
190	$\overline{\text{TR12}}$	A222-77
227	ST0	A221-4, A221-3 (Twisted pair, signal on higher-numbered pin)
228	ST1	A221-5, A221-6 (Twisted pair, signal on higher-numbered pin)
229	ST2	A221-7, A221-8 (Twisted pair, signal on higher-numbered pin)
230	ST3	A221-9, A221-10 (Twisted pair, signal on higher-numbered pin)
231	ST4	A221-11, A221-12 (Twisted pair, signal on higher-numbered pin)
232	ST5	A221-13, A221-14 (Twisted pair, signal on higher-numbered pin)
233	ST6	A221-15, A221-16 (Twisted pair, signal on higher-numbered pin)
234	ST7	A221-17, A221-18 (Twisted pair, signal on higher-numbered pin)
235	ST8	A222-3, A222-4 (Twisted pair, signal on higher-numbered pin)
236	ST9	A222-5, A222-6 (Twisted pair, signal on higher-numbered pin)
237	ST10	A222-7, A222-8 (Twisted pair, signal on higher-numbered pin)
238	ST11	A222-9, A222-10 (Twisted pair, signal on higher-numbered pin)
239	ST12	A222-11, A222-12 (Twisted pair, signal on higher-numbered pin)
240	ST13	A222-13, A222-14 (Twisted pair, signal on higher-numbered pin)
241	ST14	A222-15, A222-16 (Twisted pair, signal on higher-numbered pin)
242	ST15	A222-17, A222-18 (Twisted pair, signal on higher-numbered pin)
351	MNS	A2-74
457	MMD13	A222-42, A222-62, A221-42, A221-65
458	$\overline{\text{TR16}}$	A221-83
459	ST16	A221-20, A221-19 (Twisted pair, signal on pin 20)
464	MPT2	A221-21

Table B-3. Backplane Wiring Changes (Continued)

SIGNALS DELETED		
REF	SIGNAL	TERMINATIONS
460	MMD GND	A22-1, A222-26
470	TTK	A2-25, A222-84, A222-46, A222-33, A221-33
472	+4.5V	A222-39, A221-31, A221-46
473	M14	A20-66, A221-49
474	MMD14	A2-29, A222-64, A221-64, A221-51
475	$\overline{\text{MNS}}$	A2-76, A106-26, A106-19, A106-22, A106-20
476	$\overline{\text{MPT}}$	A2-78, A106-12
477	MPT3	A2-33, A221-84
478	MPT4	A2-31, A222-21

TERMINATIONS ADDED		
REF	SIGNAL	TERMINATIONS
106	SWSM	A1-64
117	SWSP	A1-65
226	MPT	A106-19, A106-26
311	POPIO(B)	A1-17
351	MNS	A106-12
367	LPS	A106-22, A106-20

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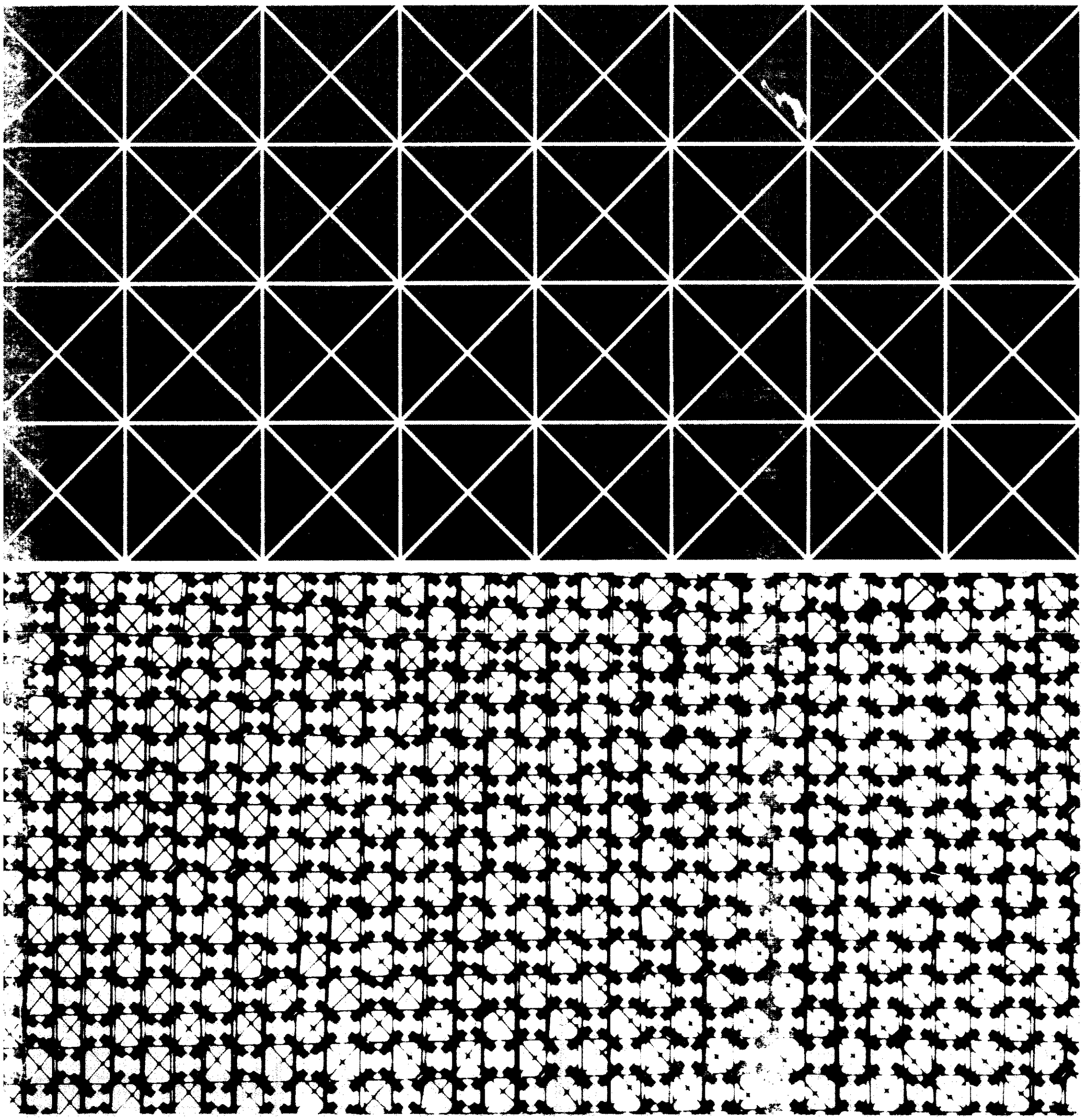

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