HEWLETT PACKARD

HP 3000 SERIES II
COMPUTER SYSTEM

SYSTEM SERVICE MANUAL

Manual Part No. 30000-90018
Microfiche Part No. 30000-90032

Printed in U.S.A. 8/76
Updates through #2 incorporated 2/77
Update 3 3/77

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LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the most recent date on which the technical material on any given page was altered. If a page is simply re-arranged due to a technical change on a previous page, it is not listed as a changed page. Within the manual, changes are marked with a vertical bar in the margin.

Pages	Effective Date
Title	Mar 1977
ii	Aug 1976
iii and iv	Mar 1977
v	Jan 1977
vi	Aug 1976
vii	Mar 1977
viii	Aug 1977
ix and x	Jan 1977
1-1	Dec 1976
1-2	Mar 1977
1-3 to 1-5	Jan 1977
1-6 to 1-27	Aug 1976
1-28 and 1-29	Jan 1977
1-30	Mar 1977
2-1 to 2-21	Dec 1976
Blank	Dec 1976
3-1 and 3-2	Dec 1976
3-3 to 3-24	Aug 1976
4-1	Jan 1977
4-2	Aug 1976
4-3 and 4-4	Jan 1977
4-5 to 4-17	Aug 1976
4-18 and 4-19	Dec 1976
4-20 to 4-22	Aug 1976
4-23	Dec 1976
4-24 to 4-32	Aug 1976
4-33	Dec 1976
4-34	Jan 1977
4-35 to 4-70	Aug 1976
4-71	Dec 1976
4-72 and 4-73	Aug 1976
Blank	Aug 1976
5-1	Dec 1976
5-2 and 5-3	Mar 1977
5-4 to 5-7	Dec 1976
Blank	Dec 1976
A-1	Jan 1977
A-2 and A-3	Aug 1976
Blank	Aug 1976
B-1 to B-42	Jan 1977
C-1 and C-2	Jan 1977

PRINTING HISTORY

New editions incorporate all update material since the previous edition. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The date on the title page and back cover changes only when a new edition is published. If minor corrections and updates are incorporated, the manual is reprinted but neither the date on the title page and back cover nor the edition change.

First Edition ..... June 1976
Second Edition ..... Aug 1976

Revised and reprinted in Aug 1976 to incorporate information concerning Fault Correcting Memory. Appendix A (IC Logic Symbology) has been removed from this manual and will appear in the Engineering Diagrams Set, part number 30000-90076.

Update 1 ..... Dec 1976
Update 2 ..... Jan 1977
Update 3 ..... Mar 1977

Update 1 adds troubleshooting information to Section II and card cage for replacement procedures in Section V.

Update 2 adds information about the 7920A Verifier Program to Section I and two new appendices (B and C).

Update 3 adds information about the 30360A HSI PCA Diagnostic (D432) to Section I.

PREFACE

This manual is intended for use by a trained Hewlett-Packard Customer Engineer (CE) trained in the principles of operation and troubleshooting procedures for the HP 3000 Series II Computer System.

This maintenance manual contains the following sections:

Section I System Verification — Verification procedures that permit the CE to determine the system operates properly.

Section II System Troubleshooting — Troubleshooting procedures designed to aid in the location of a system problem.

Section III Maintenance Panel Operating Procedures — Description and use of the HP 30354A Maintenance Panel to aid the CE analyzing system operation.

Section IV Maintenance Procedures — Repair philosophy and general servicing information (PCA jumper and switch position information), and system servicing points to aid the CE when troubleshooting the system. Principles of operation of the memory module is included in this section to assist in troubleshooting memory problems.

Section V Replaceable Parts — A list of replaceable assemblies and their part numbers. Also included is a list of replaceable cables and their part numbers, and miscellaneous items that may require replacement.

Appendix A Microdiagnostics — Instructions for executing the microdiagnostics that are built into the system.

Appendix B System Power Supplies — Detailed information on the system power supplies.

Appendix C Battery Care — Background material about system batteries and their care.

Related manuals and other documents the CE may require or find useful to maintain the system are:

HP 3000 Series II Engineering Diagrams Set, part number 30000-90076

HP 3000 Series II Computer System Reference Manual, part number 30000-90020 (System description from a hardware standpoint.)

HP 3000 Series II Computer System Operator's Guide, part number 30000-90013

HP 3000 Series II Computer System Manual of Diagnostics

HP 3000 Series II Computer System Installation Manual, part number 30000-90019.

CONVENTIONS USED IN THIS MANUAL

NOTATION	DESCRIPTION
[ ]	An element inside brackets is *optional*. Several elements stacked inside a pair of brackets means the user may select any one or none of these elements. Example: $\left[\begin{matrix}A\\B\end{matrix}\right]$ user may select A or B or neither
{ }	When several elements are stacked within braces the user **must** select one of these elements. Example: $\left\{\begin{matrix}A\\B\\C\end{matrix}\right\}$ user must select A or B or C.
italics	Lowercase italics denote a parameter which must be replaced by a user-supplied variable. Example: CALL *name* *name* one to 15 alphanumeric characters.
underlining	Dialogue: Where it is necessary to distinguish user input from computer output, the input is underlined. Example: NEW NAME? <u>ALPHA1</u>
superscript C	Control characters are indicated by a superscript C Example: Y^C
return	*return* in italics indicates a carriage return
linefeed	*linefeed* in italics indicates a linefeed
. . .	A horizontal ellipsis indicates that a previous bracketed element may be repeated, or that elements have been omitted.

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TABLES

ILLUSTRATIONS

SYSTEM VERIFICATION

SECTION I

1-1. INTRODUCTION

This section contains verification procedures that are extracts from stand-alone diagnostics to provide quick, easy to run diagnostics that verify system operation.

1-2. DIAGNOSTIC AND VERIFICATION PROGRAMS

The HP 3000 Series II Computer System uses three types of test programs. They are ON-LINE VERIFICATION PROGRAMS, STAND-ALONE DIAGNOSTICS, and MICRODIAGNOSTICS.

1-3. ON-LINE VERIFICATION PROGRAMS

The on-line verification programs are used to confirm proper operation of peripheral devices (i.e. printer, terminals, readers, punches etc). These programs run concurrently with other programs under control of the Multiprogramming Executive Operating System (MPE) and permit uninterrupted system operation. If the minimum hardware configuration required for MPE is inoperable, on-line verification programs cannot be run. The stand-alone diagnostics must then be used. The verification programs are described in the Manual of On-Line Verification Programs. The verification programs and their manual part numbers are listed in table 1-1. Access to the verification programs is obtained by entering the following:

:HELLO FIELD. SUPPORT, HP 32230
:RUN *fname*

Table 1-1. On-Line Verification Programs

PRODUCT NUMBER	DIAGNOSTIC NUMBER	DESCRIPTION	DIAGNOSTIC MANUAL PART NUMBER
30106A	D465	Card Reader	30106-90008
26XX Series L.P.	D466	Line Printer	30209-90007
2640A	D469	Display Terminal	30000-90056
2762A/B	D475	Terminal/Printer	30120-90007
2644A	D477	Display Terminal	03000-90129
2615A	D478	CRT Terminal	30122-90005
30219		Card Reader Punch	30119-90007
7260A		Optical Mark Reader	07260-90013

NOTE: Refer to paragraph 1-29 for the on-line verification procedure for the HP 30104A Paper Tape Reader and HP 30105A Paper Tape Punch.

The Optical Mark Reader on-line verification program resides in the PUB group of the SYS account.

1-4. STAND-ALONE DIAGNOSTIC PROGRAMS

The stand-alone diagnostic programs allow Customer Engineers to run maintenance and trouble-shooting tests on system hardware and peripheral devices. Each of these programs is independently-operated and runs directly on the central processor. MPE is not required and the operating system is

shut-down while stand-alone programs are running. When a problem occurs that prevents the use of both on-line or stand-alone programs, then the microdiagnostics can be used. The stand-alone diagnostics are described in the Manual of Stand-Alone Diagnostics. The stand-alone programs and their manual part numbers are listed in table 1-2. The CPU diagnostic (D420) is available from the CPU-Cold Load tape, part number 30000-10016 (11016). (−11016 is a 1600 BPI tape.)

The stand-alone diagnostic tapes are created under control of SDUPII (Standalone Diagnostic Utility Program II). Updating stand-alone diagnostics is also accomplished under control of SDUPII. For detailed information on the use and functions of SDUPII, refer to the HP 3000 Series II Computer System Diagnostic Utility Program II Manual, part number 03000-90125.

Table 1-2. Non-CPU Cold Load Diagnostics

PRODUCT NO.	DIAGNOSTIC NO.	DESCRIPTION	DIAGNOSTIC MANUAL PART NUMBER
SLEUTH	D411	SLEUTH	03000-90123
7905A	D419	Disc Subsystem (30129A)	30129-90007
30036A	D422	Multiplexer Chan.	30036-90001
2888A	D423	Disc File	30102-90015
7900A	D424	Cartridge Disc	30110-90012
30031A	D425	System Clock/Console	30031-90008
30032B	D427	Terminal Data Interface	30032-90011
2660A	D428	Fixed Head Disc	30103-90015
30030A	D429	Selector Channel	30030-90011
30007B/ 30008A/ 30009A	D430	Fault Correction Memory	30008-90001
30012A	D431	Extended Instruction Set	30012-90001
30360A	**D432**	**Hardwired Serial Interface**	**30360-90007**
7970B/E	D433	Nine Track (NRZI-PE) Mag Tape	30115-90014
30055A	D434	Synchronous Single Line Controller	30055-90008
30050A/51	D435	Universal Interface and 30219 Card Reader Punch Interface	30050-90012
30061A	D438	Terminal Controller Interface	30061-90003
30226A	D439	Plotter Interface	30226-90009

1-5. MICRODIAGNOSTICS

The microdiagnostics are microprograms that are built into the system. These are microprograms that replace the instruction set microprograms in the central processor and in some controllers. They identify problems by checking the hardware from the most basic level. The operating procedures for the built in microdiagnostics are contained in Appendix A, and also in the HP 3000 Series II Computer System Console Operator's Guide, manual part number 30000-90013. The program list is contained in the Microprogram Listing Manual, part number 30000-90023.

1-6. PURPOSE

System verification procedures are used to verify that the system operates correctly. The procedures may be run after a repair has been made, after a system modification or update has been completed, or as a confidence check if some functional area of the system is suspected of a malfunction. Section II of this manual contains procedures to isolate a fault to a functional area.

A detected malfunction will provide an error message that can be interpreted by referring to the specific diagnostic contained in the manual of stand-alone diagnostics. The diagnostic manuals also provide detailed operating instructions that allow additional testing and analysis to be performed on a suspected subsystem.

1-7. FACILITIES REQUIRED

Table 1-3 lists the diagnostic tapes required to perform the system verification. Table 1-2 lists the contents of the Non-CPU Cold Load diagnostic tape. This table lists the contents of a maximum configured system. Consult the System Configuration Guide shipped with the system to determine the specific subsystems available at a particular installation. Diagnostics on the tape are in the order listed in the table. Table 1-1 lists the contents of the on-line diagnostic tape.

Table 1-3. Diagnostic Tapes

TITLE	PART NUMBER
CPU-Cold Load	30000-10016/11016
Non CPU-Cold Load	30000-10017/11017

NOTE: −11016 and −11017 are 1600 bpi tapes.

1-8. SYSTEM VERIFICATION PROCEDURES

The system verification procedures contain the instructions required to execute the diagnostic programs. Each program is loaded using the Cold Load procedure. The verification procedures presented in this section were preconfigured using SDUP. If a diagnostic is run that has not been preconfigured, operating instructions and console messages will differ from those presented in this section. In addition to the verification procedures provided in this section, the on-line diagnostics for the peripheral equipment should also be exercised for a total system verification. Refer to the appropriate on-line diagnostic manual for the peripherals in the system.

1-9. SLEUTH 3000

SLEUTH 3000 is a stand-alone utility written in SPL/3000. It is designed to give service personnel the capability of generating unique I/O test programs that run under the control of SLEUTH 3000. These programs allow isolation of I/O problems and ease the troubleshooting of these problems. SLEUTH 3000 has the ability to run up to five different types of I/O device concurrently. It can also write and execute SIO programs, store and restore programs on magnetic tape, and edit the programs.

Peripheral devices that do not have on-line and/or stand-alone verification programs require that SLEUTH 3000 programs be written to test these devices. Several such test programs have been written for specific I/O peripherals (for example, the SLEUTH07 program described in paragraph 1-32).

SLEUTH 3000 will run on a minimum HP 3000 Series II. Refer to the HP Manual of Diagnostics for complete information on the use of SLEUTH 3000 I/O Diagnostic D411, manual part number 03000-90123.

1-10. SYSTEM CONTROL PANEL

The system control panel located at the top front of equipment bay 1 provides the system operator and service personnel the controls and lamps to perform the following functions:

- cold load and run diagnostics
- load and run user programs
- halt programs
- system dump
- observe the current instruction register
- reset the CPU
- enable or disable the auto restart function after a power failure

All switches located on the front of the control panel are three-position spring-return rocker switches. These switches have a center-off position. They are pressed on the top or bottom half to produce the desired function. When released, they return to the center position.

Located behind the upper right portion of the panel are three switches accessible when the cabinet door is opened:

CPU RESET-A two-position spring-return switch used to reset the circuits of the CPU.

PANEL DISABLE/ENABLE-A two position switch that enables or disables the system panel for use.

PF/ARS DISABLE ENABLE-A two position switch to enable or disable the auto restart program in the event of a power failure.

Table 1-4 lists and explains the function of the switches and lamps that are illustrated in figure 1-1.

1-11. MAINTENANCE PANEL

The HP 30354A Maintenance Panel can be used to perform the functions of System Control Panel. In addition, the maintenance panel can assist in localizing faults, show the contents of selected registers and the state of major signals, and modify the contents of selected registers. The function and use of the panel is described in Section III of this manual.

Table 1-4. System Control Panel Switch and Lamp Functions

PANEL MARKING	FUNCTION
CURRENT INSTRUCTION REGISTER (lamps)	Displays the content of the Current Instruction Register
SYSTEM SWITCH REGISTER (lamps and switches)	Displays the contents of the switch register as determined by pressing the switches on or off. Switches provide a 16-bit word to be used as a device number and control byte for cold load procedure.
RUN (lamp)	Indicates the system is executing a program
SYSTEM HALT (lamp)	Indicates a system halt caused by an irrecoverable error detected by the firmware.
RUN/HALT (switch)	Reverses the run/halt condition of the system.
ENABLE (switch)	Must be held in the ENABLE position to permit the LOAD or DUMP switch function to become active.
DUMP (switch)	Sends the contents of memory and CPU registers to a device specified by internal DRT jumpers.
LOAD (switch)	Used to load memory from a device specified by the SYSTEM SWITCH REGISTER contents.

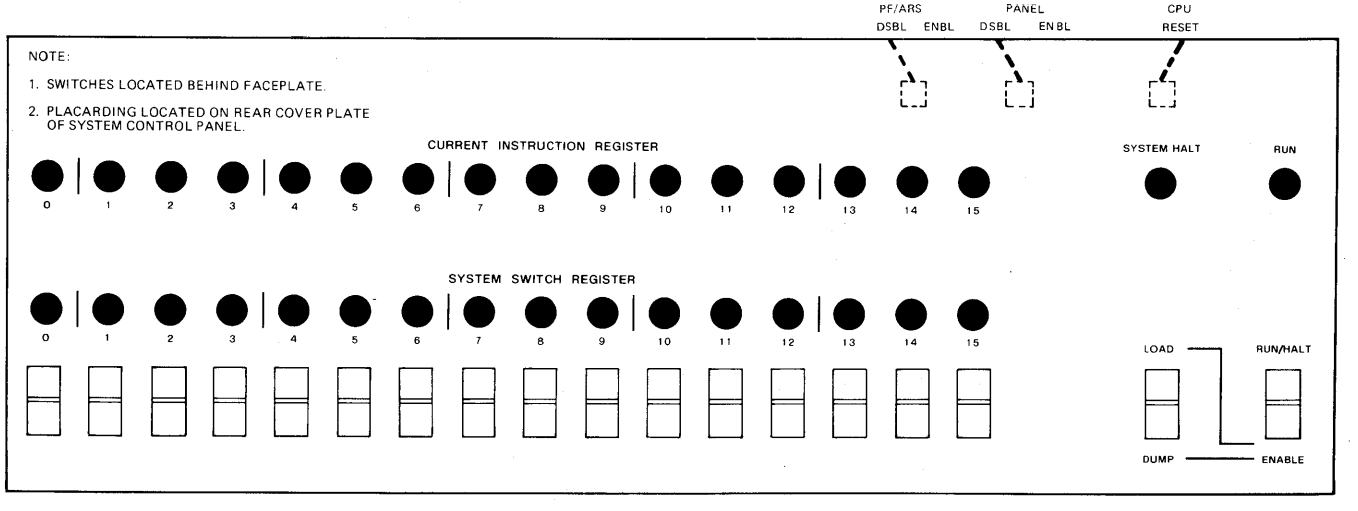

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Figure 1-1. System Control Panel

1-12. COLD LOAD (DIAGNOSTIC)

Perform the following steps to cold load a diagnostic tape.

NOTE

When the SYSTEM SWITCH REGISTER bit 8 is set to 0, all memory is initialized with a HALT %10 instruction (%030370) prior to executing the cold load. If bit 8 is set to 1, no initialization occurs prior to the cold load.

a. Load tape on tape unit 0.

b. Enter %003006 on SYSTEM SWITCH REGISTER. Simultaneously press LOAD and ENABLE switches.

c. Select the appropriate diagnostic file number from the tape and enter this octal number in the SYSTEM SWITCH REGISTER.

d. Press RUN. The diagnostic loads and the tape rewinds at the end of the load.

e. Set SYSTEM SWITCH REGISTER to 000000.

NOTE

The following verification procedures can only be used with tapes shipped with the system and listed in Table 1-2. Unless directed otherwise, all operator entries are made using the system console.

NOTE

Prior to performing any maintenance or shutdown procedures, have the System Operator verify that all jobs/sessions have been terminated before proceeding.

NOTE

Do not power-up or power-down any peripheral device when a diagnostic is running. Failure to observe this note could adversely effect the diagnostic that is executing.

1-13. HP 30129 CARTRIDGE DISC DIAGNOSTIC (D419)

The diagnostic verifies the input, output, and control functions of the HP 30129A Cartridge Disc subsystem. The following procedure is used to verify operation.

NOTE

A SYSDUMP should be performed prior to executing the diagnostic. A RELOAD must be performed after completing the diagnostic.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D419 from stand-alone diagnostic tape. Press RETURN	D99 01 CARTRIDGE DISC (HP 30129A) DIAGNOSTIC CONFIGURATION (D419X.YY.Z) Q99 02 DECIMAL DEVICE NUMBER?
X = Version YY = Update level Z = Fix level Enter the decimal device number of the disc controller. Press RETURN	
Enter in decimal the maximum number of error messages you wish to receive (4-6). Press RETURN	Q99 03 MAXIMUM ERROR PRINT COUNT
Set SYSTEM SWITCH REGISTER bit 0 off. Press RETURN	P99 55 UPDATE SWITCH REGISTER
On the disc unit, set the LOWER and UPPER DISC PROTECT switches down. Set the FORMAT switch to the right position. Set UNIT SELECT switch to position 0. Press RETURN	P99 05 RESET BOTH PROT. DATA SWITCHES, SET SWITCH FORMAT AND UNIT TO 0.
Enter NO Press RETURN	Q99 42 WISH TO EXECUTE INTERACTIVE PORTION IN SECTION 1 (YES/NO)
Program runs approximately one hour.	D99 07 CARTRIDGE DISC (HP 30129A) DIAGNOSTIC OFF-LINE (D419X.YY.Z)

1-14. HP 30008A/30009A FAULT CORRECTION MEMORY DIAGNOSTIC (D430)

The fault correction memory diagnostic performs the following functions:

- Verifies the Fault Logging Interface (FLI) PCA array and reads the previous history of both arrays (when present) and lists all errors.
- Clears and verifies both Memory Control and Logging (MCL) PCA arrays.
- Verifies all Semiconductor Memory Array (SMA) PCA arrays and lists any errors.
- Checks the capability to detect and correct single bit errors in both data and check bits, detects most multi-bit errors, and detects I/O failures in the Fault Correction Array (FCA) PCA.
- Executes the main diagnostic program for all SMA PCA's.
- Reads and lists the error history of both MCL logging arrays.

The following procedure is used to verify operation:

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D430 from stand-alone diagnostic tape.	
Set SYSTEM SWITCH REGISTER bit 0 off. Press RETURN.	HP 3000 SERIES II FAULT CORRECTING MEMORY TEST D430X.YY.ZZ (C) COPYRIGHT HEWLETT-PACKARD COMPANY 1976.
X = Version YY = Update level ZZ = Fix level	
NOTE The following message only appears if banks 2 and 3 are not present in the system.	E0.02 UPPER MCL, NOT RESPONDING
Enter in decimal the lowest memory bank number (0). Press RETURN.	LOW BANK ?
Enter in decimal the low memory address (1). (Do Not enter 0). Press RETURN.	LOW ADDRESS ?
Enter in decimal the highest memory bank number in the system (0,1,2, or 3). Press RETURN	HIGH BANK ?
Enter in octal the highest memory address that is addressable from the memory bank specified in the previous entry. Refer to the following list.	HIGH ADDRESS ?
Press RETURN	
Program executes and takes approximately 62 minutes to fully test each bank. (All banks specified above are tested during one pass of the diagnostic.)	D1.04 END OF SECTION 1 D2.10 END OF SECTION 2 D3.17 END OF SECTION 3 D4.25 END OF SECTION 4 P5.50 END OF STEP 50 P5.51 END OF STEP 51 P5.52 END OF STEP 52 P5.54 END OF STEP 54
NOTE Messages P5.55 through P5.65 will appear when addresses in the range of 10K to 40K in bank 0 are tested.	

Memory Word Size	Bank	Address
64K	0	%177777
96K	1	%077777
128K	1	%177777
160K	2	%077777
192K	2	%177777
224K	3	%077777
256K	3	%177777

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
	P5.55 END OF STEP 55 P5.60 END OF STEP 60 P5.61 END OF STEP 61 P5.62 END OF STEP 62 P5.64 END OF STEP 64 P5.65 END OF STEP 65 D5.25 END OF SECTION 5
NOTE The following message appears if the upper 128K MCL PCA is not present in the system.	E6.66 UPPER MCL, NOT RESPONDING D6.66 END OF SECTION 6 D6.66 01 PASS
Program restarts and continues to run until operator presses HALT.	

1-15. HP 30036A MULTIPLEXER CHANNEL DIAGNOSTIC (D422)

The multiplexer channel diagnostic verifies the functional operation of the Multiplexer PCA by testing order RAM, order register, address RAM, address register, state RAM, state register, and related SIO. Two Selector Channel Maintenance PCA's (SCMB) should be installed with the correct device numbers before executing the diagnostic. Refer to Section IV of this manual for installation information. The diagnostic may be run with none, or one SCMB installed, console messages will be different. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D422 from stand-alone diagnostic tape. Press RETURN X = Version YY = Update level Z = Fix level Set SYSTEM SWITCH REGISTER bit 0 off.	D01 30036A MPX CHANNEL TEST (HP D422X.YY.Z) Q01 SELECT OPTIONS
NOTE The SYSTEM SWITCH REGISTER may be set to %101000 (bits 0 and 6 set) when only one SCMB is installed in the multiplexer channel. This switch register setting will cause steps 75-78 of the diagnostic to be skipped. These steps are used only when a second SCMB is installed in the multiplexer channel.	

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Press RUN (Time for one pass is approximately two minutes.)	P02 END SECTION IORES P02 END SECTION ARADDR P02 END SECTION ARDATA P02 END SECTION ARCPP P02 END SECTION ORADDR P02 END SECTION ORDATA P02 END SECTION ORCP P02 END SECTION AREG P02 END SECTION OREG P02 END SECTION NSGP1 P02 END SECTION NSGP2 P02 END SECTION NSGP3 P02 END SECTION NSGP4 P02 END SECTION STPAR
NOTE The following console message appears if no SCMB's are installed in the multiplexer channel.	P18 1ST SCMB DRT# NOT ENTERED; STEPS 41-74 ABORTED P19 2ND SCMB DRT# NOT ENTERED; STEPS 75-78 ABORTED
With one SCMB installed, message P18 is not displayed. With both SCMB's installed, messages P18 and P19 are supressed, and the following messages appear.	P16 FAST SR READ MODE (2K XFER); TIME = 4 MSEC.; BANK 00; STEP 63 P16 FAST SR READ MODE (2K XFER); TIME = 4 MSEC.; BANK 01; STEP 63 P17 FAST SR WRITE MODE (2K XFER); TIME = 4 MSEC.; BANK 00; STEP 68 P17 FAST SR WRITE MODE (2K XFER); TIME = 4 MSEC.; BANK 01; STEP 68 P02 END SECTION SIOTST D02 END MPX CHAN TEST D03 END: PROGRAM CYCLE: PASS=1
Program restarts and continues to run until operator presses HALT switch.	

1-16. HP 30102A DISC FILE DIAGNOSTIC (D423)

The diagnostic verifies the input, output, and control functions of the HP 30102A Disc File. The following procedure is used to verify operation.

NOTE

Prior to running this diagnostic a SYS DUMP should be performed to save information stored on the disc pack. When answering the dialogue for the SYS DUMP, enter 0 for the date so that all the data is saved.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D423 from stand-alone diagnostic tape. Press RETURN	D99 01 DISC FILE (30102A) DIAG CONFG (D423X.YY.Z) Q99 02 DECIMAL DEVICE NUMBER
X = Version YY = Update level Z = Fix level Enter in decimal the DRT number of the disc controller. Press RETURN	Q99 03 INTERRUPTS ON OR OFF?
Enter ON Press RETURN	P99 61 PAUSE AFTER CONFIGURATION
(The message means the hardware has paused (%030040 in CIR) and is waiting for an update of the switch register.) Set SYSTEM SWITCH REGISTER bit 0 off. Press RETURN Program runs approximately one hour to completion.	

1-17. HP 30110A CARTRIDGE DISC DIAGNOSTIC (D424)

The diagnostic verifies the input, output, and control functions of the HP 30110A Cartridge Disc. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D424 from stand-alone diagnostic tape. Press RETURN	D99 01 CARTRIDGE DISC (30110A) DIAG CONFG (D424X.YY.Z) Q99 02 DECIMAL DEVICE NUMBER?
X = Version YY = Update level Z = Fix level Enter in decimal the DRT number of the disc controller. Press RETURN	Q99 03 INTERRUPTS ON OR OFF?
Enter OFF Press RETURN	P99 61 PAUSE AFTER CONFIGURATION
(The message means the program has paused and is waiting for an update of the switch register.) Set SYSTEM SWITCH REGISTER bit 0 off. Press RETURN Program runs approximately one hour.	

1-18. HP 30031A SYSTEM CLOCK CONSOLE INTERFACE DIAGNOSTIC (D425)

The system clock console interface diagnostic verifies the operation of system console interface with the system clock console interface PCA. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D425 from stand-alone diagnostic tape. Press RETURN	
	D01 HP 30031A SYSTEM TIMER DIAGNOSTIC (D425X.YY.Z) Q02 SELECT SWREG OPTIONS
X = Version YY = Update level Z = Fix level Set SYSTEM SWITCH REGISTER bit 0 off. Press RUN Program runs and messages appear on the console. Program runs approximately 2.5 minutes for a complete pass.	
	P01 SECTION I P03 END STEP 101 P03 END STEP 103 P03 END STEP 105 P02 END SECTION 1
	P01 SECTION 2 P03 END STEP 201 P03 END STEP 202 P03 END STEP 203 P03 END STEP 204 P03 END STEP 205 P03 END STEP 206 P03 END STEP 207 P03 END STEP 210 P02 END SECTION 2
	P01 SECTION 3 P03 END STEP 302 P03 END STEP 304 P03 END STEP 306 P03 END STEP 310 P03 END STEP 312 P03 END STEP 314 P03 END STEP 316 P02 END SECTION 3
	P01 SECTION 4 P03 END STEP 402 P03 END STEP 404 P03 END STEP 406 P03 END STEP 407 P03 END STEP 410 P03 END STEP 411 P03 END STEP 412 P03 END STEP 413 P03 END STEP 414 P03 END STEP 415 P03 END STEP 420 P03 END STEP 422 P03 END STEP 424 P03 END STEP 426 P02 END SECTION 4
	D02 END: PROGRAM CYCLE: PASS=1
Program restarts and continues to run until the operator presses HALT.	

1-19. HP 30032A TERMINAL DATA INTERFACE (TDI) PCA DIAGNOSTIC (D427)

The TDI diagnostic tests the 16 channels of the Terminal Data Interface PCA. Test cable 30062-60003 is required to execute the diagnostic. The test cable is initially connected between channels 0 and 1 on the HP 30062A Terminal Controller/Multiplexer Connector Panel and then connected to the next sequential pair of channels until all channels have been tested. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
NOTE Tag and identify all cable connectors on HP 30062A Connector Panel located at the rear of equipment bay 1 before proceeding.	NOTE No console messages are obtained during this diagnostic.
Disconnect all cable connectors from HP 30062A Connector Panel.	Each pair of channels takes approximately 20 seconds for the test to run.
Connect test cable 30062-60003 between channels 0 and 1 on the connector panel.	
Cold load diagnostic D427 from stand-alone diagnostic tape. Program loads and displays HALT %6 (%030366) in CIR.	
Select switch register options by setting bit 0 of SYSTEM SWITCH REGISTER off. Press RUN	
CIR displays HALT %7 (%030367).	
Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 0 and 1, enter %000001. Press RUN	
CIR displays HALT %6 (%030366). Press RUN	
Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR.	
Disconnect test cable from channels 0 and 1, and reconnect between channels 2 and 3.	
Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 2 and 3, enter %001003. Press RUN	
CIR displays HALT %6 (%030366). Press RUN	
Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR.	
Disconnect test cable from channels 2 and 3, and reconnect between channels 4 and 5.	
Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 4 and 5, enter %002005. Press RUN	

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable from channels 4 and 5, and reconnect between channels 6 and 7. Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 6 and 7, enter %003007. Press RUN CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable from channels 6 and 7, and reconnect between channels 8 and 9. Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 8 and 9, enter %004011. Press RUN CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable from channels 8 and 9, and reconnect between channels 10 and 11. Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 10 and 11, enter %005013. Press RUN CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable from channels 10 and 11, and reconnect between channels 12 and 13. Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 12 and 13, enter %006015. Press RUN CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable from channels 12 and 13, and reconnect between channels 14 and 15.	

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 14 and 15, enter %007017. Press RUN CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable and reconnect cables to connector panel for normal system operation.	

1-20. HP 2660A FIXED HEAD DIAGNOSTIC (D428)

The fixed head disc diagnostic verifies proper operation of the fixed head disc subsystem. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D428 from stand-alone diagnostic tape. Press RETURN X = Version YY = Update level Z = Fix level Enter in decimal the DRT number of the disc controller. Enter in decimal the first track to be tested, usually 0. Enter 255 for a 2Mbyte disc or 511 for a 4Mbyte disc. Set SYSTEM SWITCH REGISTER bits 0 and 15 on. (No tracks protected). Press RUN	D000 FIXED HEAD DISC DIAGNOSTIC (HP 428X.YY.Z) P008 ENTER DEVICE NUMBER P009 ENTER FIRST AVAILABLE TRACK P010 ENTER LAST AVAILABLE TRACK D14 SET SWITCH REGISTER E001 NSW 1000000000000001

1-21. HP 30033A SELECTOR CHANNEL DIAGNOSTIC (D429)

The selector channel diagnostic communicates with the selector channel maintenance PCA (SCMB) via the selector channel PCA and its associated port controller PCA. Checks are made on data pattern, response, control sequences, and I/O program orders.

The selector channel maintenance board (SCMB) PCA must be installed and configured prior to executing the diagnostic. Refer to Section IV of this manual for installation information. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D429 from stand-alone diagnostic tape. Press RETURN	NOTE The following console messages were obtained from a system having two memory banks, and 128K words of memory. D100 HP-30030B SELECTOR CHANNEL DIAG. (D429X.YY.Z) Q104 SELECT OPTIONS
X = Version YY = Update level Z = Fix level Set SYSTEM SWITCH REGISTER bit 0 off. Press RUN	
Enter in decimal the DRT number of the SCMB. Press RETURN	Q101 SET MAINT CARD DEV NUM?
Enter in decimal the DRT number of the system clock/ console interface PCA (usually 3). Press RETURN	Q102 SET TIMER/CONSOLE NUM?
Enter the highest memory bank number for the system (0 - 3). Refer to the following list. **Memory Word Size / Bank / Address** 64K / 0 / %177777 96K / 1 / %077777 128K / 1 / %177777 160K / 2 / %077777 192K / 2 / %177777 224K / 3 / %077777 256K / 3 / %177777	Q108 ENTER UPPER BANK #=
Press RETURN	
Enter in octal the last address for the highest bank number in the system (%077777 or %177777). See above list. Press RETURN	Q109 ENTER UPPER ADDRESS (OCTAL)=
Enter in decimal the maximum number of error messages you wish to receive. Press RETURN	Q105 ERR PRINT LIMIT ?
Program executes and displays the following messages.	D110 DIRECT I/O TEST D127 DIRECT I/O TEST COMPLETED D130 CONTROL ORDER TEST D217 CONTROL ORDER TEST COMPLETED D220 READ TEST D224 2K READ 2 MILLISEC; BANK 0 D224 2K READ 2 MILLISEC; BANK 1 D247 READ TEST COMPLETED D250 WRITE TEST D274 2K WRITE 2 MILLISEC; BANK 0 D274 2K WRITE 2 MILLISEC; BANK 1 D275 WRITE TEST COMPLETED D300 CHAINED READ TEST D317 CHAINED READ TEST COMPLETED D320 CHAINED WRITE TEST D337 CHAINED WRITE TEST COMPLETED

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Program restarts and continues to run until operator presses HALT.	D340 ERROR RESPONSE TEST D367 ERROR RESPONSE TEST COMPLETED D600 SELECTOR CHANNEL DIAG COMPLETED D601 END OF PASS 1

1-22. HP 30012A EXTENDED INSTRUCTION SET DIAGNOSTIC (D431)

The extended instruction set diagnostic is contained in two sections. Section 1 is the Floating Point diagnostic and Section 2 is the Decimal diagnostic. The diagnostic is designed to verify that both Floating Point and Decimal instructions execute properly, and any residues derived are verified for correctness. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D431 from stand-alone diagnostic tape. Press RETURN	D01 HP 30012A EXTENDED INSTRUCTION SET DIAGNOSTIC (D431.X.YY.ZZ) Q01 ENTER SWREG.SELECT OPTIONS
X = Version YY = Update level ZZ = Fix level Set SYSTEM SWITCH REGISTER bit 0 off. Press RUN	Q02 ENTER SECTION SELECT OPTIONS
Set SYSTEM SWITCH REGISTER bit 0 off. Press RUN	
Program execute and displays the following message. (Execution time for 200 passes is approximately 60 seconds.) Program halts after 200 passes.	D02 200 PASSES COMPLETED

1-23. HP 30115A NINE-TRACK MAGNETIC TAPE DIAGNOSTIC (D433)

The diagnostic verifies the input, output, and control functions of the HP 30115A nine-track magnetic tape unit. A blank reel of tape (80 - 100 feet) with a write ring must be available for test purposes. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D433 from stand-alone diagnostic tape. Press RETURN	HP 30115A 9-TRACK MAGNETIC TAPE (D433X.YY.Z) (STAND-ALONE DIAGNOSTIC PROGRAM) Q010 TAPE DEVICE NUMBER?
X = Version YY = Update level Z = Fix level Enter in decimal the DRT number of the tape controller. Press RETURN	Q011 TIMER DEVICE NUMBER?

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Enter in decimal the DRT number of the timer (usually 3). Press RETURN	
	Q012 MAXIMUM ERROR PRINT COUNT?
Enter in decimal the maximum number of error messages you wish to receive. Press RETURN	
	P005 TYPE FOLLOWING CONTROL A'CR'-AUTO E'CR'-EXIT R'CR'-RESTART M'CR'-MANU 'CR'-RESUME YOUR CODE?
Enter A Press RETURN	
	D015 PRESENT SECTION REGISTER: %077414 DO YOU WISH TO CHANGE? (YES/NO)
Enter NO Press RETURN	
	Q019 AUTO-PRCESS: ENTER TAPE UNIT (B,E,NO) AT Q020 DRIVE 0?
Enter tape model suffix designator B, or E, NO= no tape unit present. Press RETURN	
	Q020 DRIVE 1?
Enter tape model suffix designator. Press RETURN	
	Q020 DRIVE 2?
Enter tape model suffix designator. Press RETURN	
	Q020 DRIVE 3?
Enter tape model suffix designator. Press RETURN	
	P003 UNLOAD PROGRAM TAPE — LOAD TEST TAPE(S)
Remove the stand alone diagnostic tape and mount a scratch tape 80-100 feet long.	
	Q030 ALL DEFINITIONS CORRECT (YES/NO)?
(This message is asking if you are satisfied that all previous entries are correct before proceeding.) Enter YES Press RETURN	
	P011 UPDATE SWITCH REGISTER (CR)
Set all bits of the SYSTEM SWITCH REGISTER off. Press RETURN	
Program executes and message appears on the console after a complete pass (approximately 20 minutes for 100 feet of tape). Program will repeat until HALT is pressed.	
	P060 01 PASS 000000 TOTAL ERRORS

1-24. HP 30055A SYNCHRONOUS SINGLE LINE CONTROLLER (SSLC) PCA DIAGNOSTIC (D434)

Prior to executing the diagnostic, the SSLC PCA interconnecting cable must be terminated with test connector part number 30055-60005. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D434 from stand-alone diagnostic tape. Press RETURN. X = Version YY = Update level Z= Fix level Set SYSTEM SWITCH REGISTER bit 0 off. Press RUN Program restarts and continues to run until operator presses HALT.	30055A SYNC SINGLE LINE CTLR TEST (D434.X.YY.Z) P10 ENTER SWITCH REG. OPTIONS D345 END SECTION 1 D345 END SECTION 2 D345 END SECTION 3 D345 END SECTION 4 D345 END SECTION 5 D345 END SECTION 6 D350 END OF PASS 1

1-25. UNIVERSAL INTERFACE, CARD READER PUNCH INTERFACE PCA DIAGNOSTIC (D435)

This diagnostic can test the HP 30050A Universal Interface (TTL) PCA, HP 30051A Universal Interface (Differential) PCA, or the HP 30219A Card Reader Punch Interface PCA. The diagnostic requires the HP 30049C Diagnostic Hardware assembly to execute the diagnostic. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Set the SYSTEM DC POWER switch to STANDBY. Disconnect the cable for the peripheral device from the PCA to be tested. Remove the PCA to be tested from the card cage and note the position of the interrupt jumper. If a TTL PCA, also note the presence or absence of jumper W1 (present = positive true, absent = negative true). The interface PCA must have a jumper inserted near connector J3. If the jumper is missing, remove the two-pin jumper plug from the Diagnostic Hardware assembly and insert it near J3 on the interface PCA. This jumper provides power to the Diagnostic Hardware assembly. Insert the PCA to be tested into the card cage. Connect the Diagnostic Hardware Assembly to the interface PCA. Set the SYSTEM DC POWER switch to ON. The PWR ON indicator on the Diagnostic Hardware assembly should light. Cold load diagnostic D435 from stand-alone diagnostic tape. Press RETURN	D100 UNIV. INTERFACE TEST (D435X.YY.Z)

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
X = Version YY = Update level Z = Fix level	
Enter in decimal the DRT number of the PCA to be tested. Press RETURN	Q110 DEVICE NUMBER?
Check the interrupt mask jumper position on the PCA to be tested and use the following chart to determine the correct entry.	Q112 INTERRUPT MASK?
Press RETURN	Q113 NEGATIVE TRUE?
Enter YES for PCA's 30050-60001 and 30050-60008. Enter NO for PCA 30050-60003. Press RETURN	
Enter NO Press RUN	Q114 CHANGE INTERNAL SWITCH REGISTER
Enter 2,3,4,5,6,7,8,9,10 Include section 1 only when the test equipment referenced in the manual of diagnostics is available for use. Press RETURN	Q115 SECTION LIST?
Enter YES if the PCA is the interface for the card reader punch. Otherwise enter NO. Press RETURN	Q116 READER PUNCH INTERFACE?
	D102 END SECTION 0 D100 UNIV. INTERFACE TEST (D335X.YY.Z) D102 END SECTION 2 D102 END SECTION 3 D102 END SECTION 4 D102 END SECTION 5 D102 END SECTION 6 D102 END SECTION 7 D102 END SECTION 8 D102 END SECTION 9 D102 END SECTION 10 D103 END PASS 1
Time for one pass is approximately 50 seconds. Program restarts and continues to run until the operator presses HALT.	

Jumper Position	Entry
0	100000
1	40000
2	20000
3	10000
4	4000
5	2000
6	1000
7	400
8	200
9	100
10	40
11	20
12	10
13	4
14	2
15	1
ENABLE	0
DISABLE	177777

1-26. HP 30061A TERMINAL CONTROLLER INTERFACE (TCI) PCA DIAGNOSTIC (D438)

The TCI diagnostic tests the 16 channels of the terminal controller. Test cable 30062-60003 is required to execute the diagnostic. The test cable is initially connected between channels 0 and 1 on the the HP 30062A Terminal Controller/Multiplexer Connector Panel and then connected to the next sequential pair of channels until all channels have been tested. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
NOTE Tag and identify all cable connectors on HP 30062A Connector Panel, located at the rear of equipment bay 1 before proceeding.	
Disconnect all cable connectors from HP 30062A Connector Panel.	
Connect test cable 30062-60003 between channels 0 and 1 on the connector panel.	
Cold load diagnostic D438 from stand-alone diagnostic tape. Program loads and displays HALT %6 (%030366) in CIR.	
Select switch register options by setting all bits of SYSTEM SWITCH REGISTER off. Press RUN	
CIR displays HALT %7 (%030367) Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 0 and 1, enter %000001. Press RUN	
CIR displays HALT %6 (%030366). Press RUN	
Program executes and CIR displays HALT %16 (%030376) after successful completion of the test. An error condition will display a HALT %12 (%030372) in CIR.	NOTE No console messages are obtained during this diagnostic.
Disconnect test cable from channels 0 and 1, and reconnect between channels 2 and 3.	
Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 2 and 3, enter %001003. Press RUN	
CIR displays HALT %6 (%030366). Press RUN	
Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR.	
Disconnect test cable from channels 2 and 3, and reconnect between channels 4 and 5.	
Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 4 and 5, enter %1002005. Press RUN	
CIR displays HALT %6 (%030366). Press RUN	

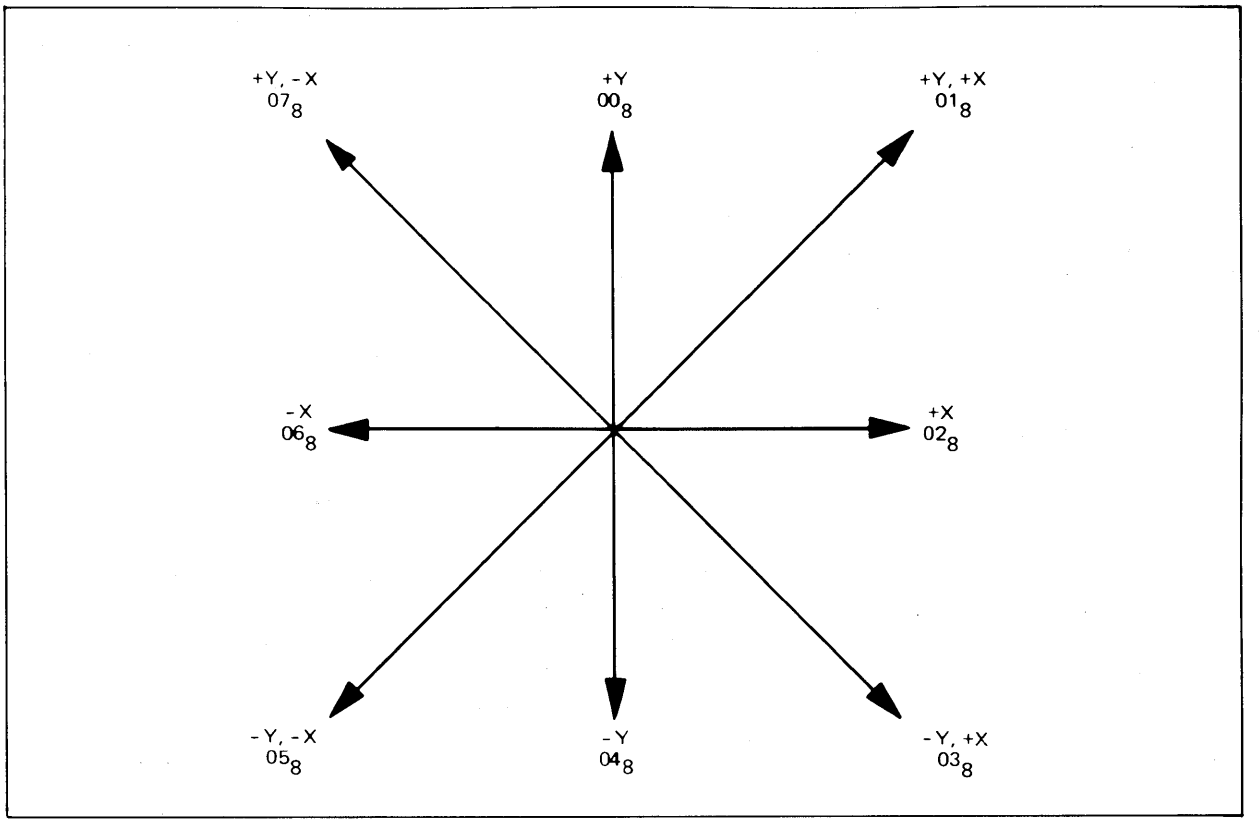
OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (030372) in CIR. Disconnect test cable from channels 4 and 5, and reconnect between channels 6 and 7. Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 6 and 7, enter %003007. Press RUN CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable from channels 6 and 7, and reconnect between channels 8 and 9. Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 8 and 9, enter %004011. Press RUN CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable from channels 8 and 9, and reconnect between channels 10 and 11. Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 10 and 11, enter %005013. Press RUN CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable from channels 10 and 11, and reconnect between channels 12 and 13. Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 12 and 13, enter %006015. Press RUN CIR displays HALT %6 (%030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable from channels 12 and 13, and reconnect between channels 14 and 15.	

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Enter channel numbers to be tested into SYSTEM SWITCH REGISTER. For channels 14 and 15, enter %007017. Press RUN CIR displays HALT %6 (030366). Press RUN Program executes and CIR displays HALT %16 (%030376) after successful completion of test. An error condition will display a HALT %12 (%030372) in CIR. Disconnect test cable and reconnect cables to connector panel for normal system operation.	

1-27. HP 30226A PLOTTER INTERFACE DIAGNOSTIC (D439)

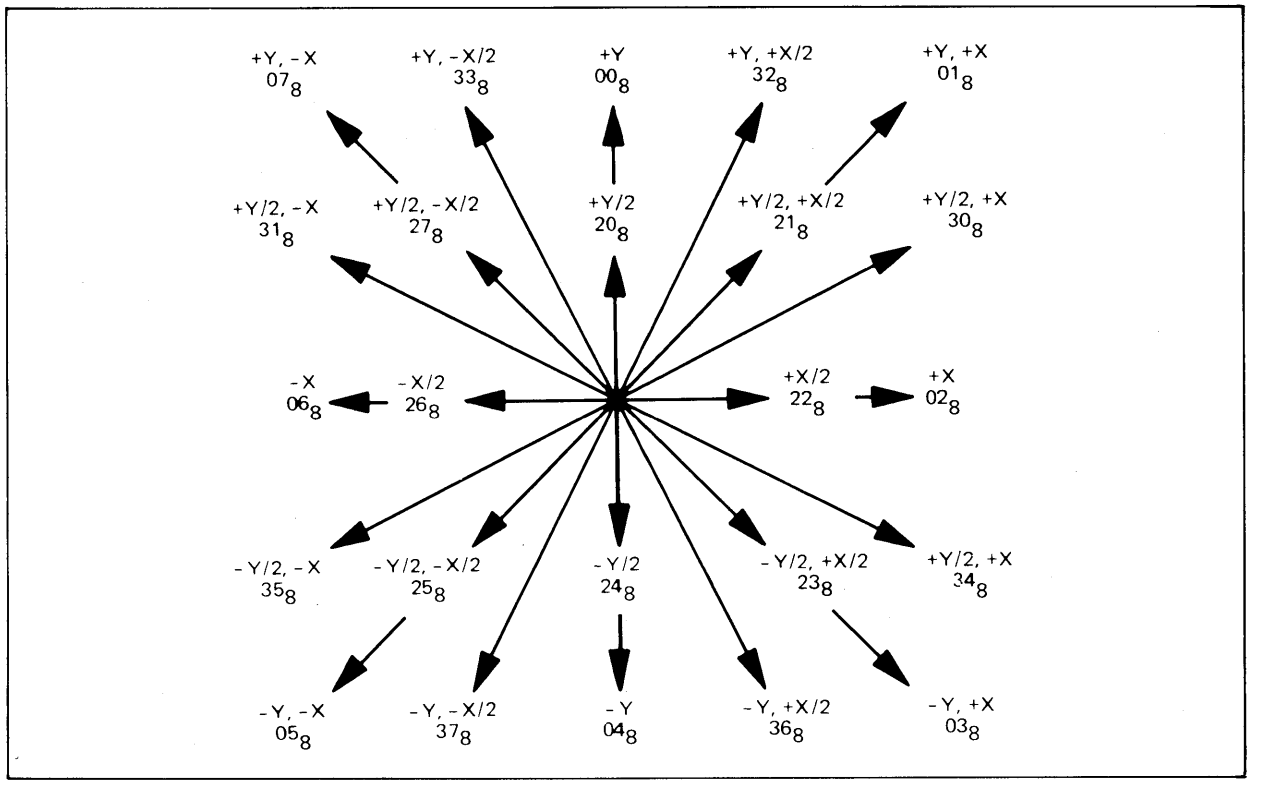
This diagnostic is divided into two sections. Section I is performed with a test connector (part number 30226-60003) connected in place of the plotter cable. This section tests the interface PCA. Section 2 tests the basic operation of the CalComp plotter when connected to the interface PCA. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Cold load diagnostic D439 from stand-alone diagnostic tape. Press RETURN	D326 PLOTTER INTERFACE DIAGNOSTIC (HP 32367X.YY.Z) ENTER SWITCH REGISTER OPTIONS
X = Version YY = Update level Z = Fix level Set SYSTEM SWITCH REGISTER bit 0 off. Press RUN Program stops and displays HALT 7 in CIR (%030367).	
After installing the connector, press RUN Program executes Section I. (HALT 7 in CIR, %030367)	PROPERLY INSTALL THE 30226-60003 TEST CONNECTOR
Connect plotter cable, place plotter power on. Press RUN	CONNECT PLOTTER TO INTERFACE PLACE PLOTTER POWER ON, INSURE UNIT IS NOT IN STANDBY WHAT IS THE INCREMENT/INCH RATIO OF YOUR PLOTTER ?
Step Size / **Operator Entry** .01 in. 100 .005 in. 200 .0025 in. 400 .002 in. 500 .10 mm 200 .05 mm 500	
Press RETURN after the entry.	TYPE 500 PLOTTER ?
Enter YES or NO Press RETURN (If YES, go to procedure B)	IS THE LIMIT SWITCH OPTION AVAILABLE?
Enter YES or NO Press RETURN	IS THE READY/NOT READY OPTION AVAILABLE ?



7522-18

Figure 1-2. Type 500 Plot



7522-19

Figure 1-3. Type 600/700 Plot

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Enter YES or NO Press RETURN (If the plotter is a type 600 or 700 and the Ready/Not Ready option is not installed, go to procedure A.)	
Place plotter power off and enter Y to continue.	PLACE PLOTTER POWER OFF
Turn plotter power on and enter Y to continue.	PLACE PLOTTER POWER ON, ENSURE UNIT ISN'T IN STANDBY
A If the plotter is a type 600 or 700 and the Limit Switch option is installed, the message is:	
Strike the limit switch with the pen and enter Y to continue.	STRIKE THE LIMIT SWITCH WITH THE PEN
B Place the pen in the center of plotter chart, enter Y to continue.	PLACE PEN IN CENTER OF PLOTTER CHART
Program runs until the following message is displayed: (Plot for a type 500 plotter is shown in figure 1-2, and for a type 600 or 700 plotter see figure 1-3).	D328 END OF PLOTTER INTERFACE DIAGNOSTIC

1-28. HP 3000 SERIES II COMPUTER SYSTEM CPU DIAGNOSTIC (D420)

The diagnostic tests all the instructions and most of the conditions that result in interrupts and traps by the CPU. The diagnostic is divided into 14 parts. Only the first five parts should be run when no HP 30354A Maintenance Panel is connected to the system. The remaining nine parts require the maintenance panel for observing data. Refer to the CPU stand-alone diagnostic manual (30003-90001) for details of how to execute the remaining nine parts of the diagnostic. The following procedure is used to verify operation.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Cold load CPU cold load diagnostic tape, part number 30000-10016/11016. (Leave the SYSTEM SWITCH REGISTER set to %003006.) This cold loads part 1 of the diagnostic. Press RUN CIR contains a PAUSE (%030020) Press HALT Computer should HALT. Press RUN (Program runs approximately 45 seconds. CIR displays HALT %15, %030375, indicating end of part 1.)	NOTE No console messages are obtained during this diagnostic.
Cold load part 2 by pressing LOAD and ENABLE. Press RUN (Program runs approximately 50 seconds. CIR displays HALT %15, %030375, indicating end of part 2.)	
Cold load part 3 by pressing LOAD and ENABLE. Press RUN (Program runs approximately 4 seconds. CIR displays HALT %15, %030375, indicating end of part 3.)	

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Cold load part 4 by pressing LOAD and ENABLE. Press RUN (Program runs approximately 4 seconds. CIR displays HALT %15, %030375, indicating end of part 4.) Cold load part 5 by pressing LOAD and ENABLE. Press RUN (Program runs approximately 50 seconds. CIR displays HALT %15, %030375, indicating end of part 5.)	

1-29. HP 30104A PAPER TAPE READER, HP 30105A PAPER TAPE PUNCH ON-LINE VERIFICATION PROGRAM

On-line verification of the paper tape punch is performed independently from the paper tape reader. Both subsystems may not always be present in the system configuration.

1-30. PAPER TAPE PUNCH VERIFICATION. To verify operation of the paper tape punch, perform the following steps:

1. Log onto the system.

   :HELLO FIELD.SUPPORT,HP32230

2. Set up the punch file command, where LDN = the logical device name of the tape punch.

   :FILE OUT;DEV=LDN;REC=-72,I,F,ASCII

3. Output the numerals, alphabet, and special characters from the terminal to tape punch using FCOPY.

   :RUN FCOPY.PUB.SYS

   HP32212A.XX.YY FILE COPIER (C) HEWLETT/PACKARD CO. 1976
   >FROM= ;TO=*OUT

4. The following message will be output by FCOPY if the terminal is not set up as a 72 byte device. The message can be ignored, enter a RETURN.

   200

5. Input each of the following lines at the terminal. Terminate each line with a RETURN.

   1234567890

   ABCDEFGHIJKLMNOPQRSTUVWXYZ

   !"# $%&'( )=-\@@+*;:<>?,./

6. Enter Y^c (control Y) to terminate the input phase.

7. The following message appears on the terminal.

   <CONTROL Y>
   4 RECORDS PROCESSED ***0 ERRORS

8. Terminate FCOPY by entering the following:

   >EXIT

9. Compare the tape just produced with figure 1-4, the two tapes should be identical. If the tapes differ, use SLEUTH to determine the problem with the paper tape punch.

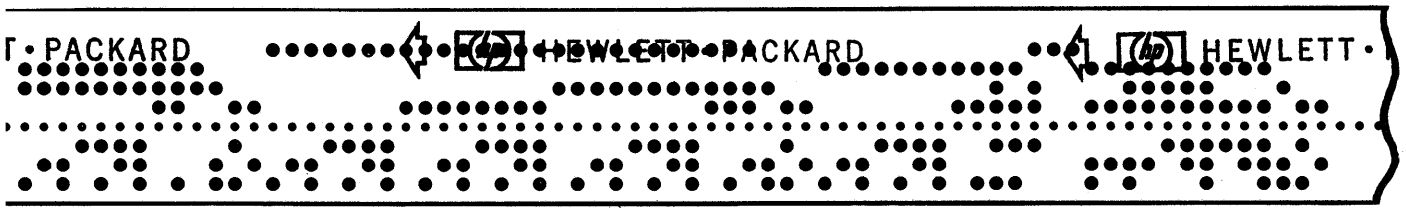


Figure 1-4. Master Tape

1-31. PAPER TAPE READER VERIFICATION. To verify operation of the paper tape reader, perform the following steps:

1. Log onto the system.

   :HELLO FIELD.SUPPORT,HP32230

2. Set up the reader file command, where LDN = the logical device name of the paper tape reader.

   :FILE IN;DEV=LDN;REC=-72,I,F,ASCII

3. If the reader is a job accepting device, the following entries are required at the system console to make the reader non-job accepting.

   =REFUSE LDN
   =ABORTIO LDN

4. Use FCOPY to read from the tape reader and write to the terminal.

   :RUN FCOPY.PUB.SYS

   HP32212A.XX.YY FILE COPIER (C) HEWLETT-PACKARD CO. 1976
   >FROM=IN;TO=

5. Place the paper tape (30204-80003) supplied with the reader into the read head leaving some leader behind the read head.

6. Answer the I/O request on the system console with the PIN and logical device number of the tape reader.

7. If the terminal is configured for anything greater than 72 byte records, FCOPY will output the following message. The message can be ignored by entering a RETURN.

   200

8. The following characters should be displayed at the terminal. Verify that all characters are correct. If the characters are incorrect, use SLEUTH to locate the problem.

   1234567890
   ABCDEFGHIJKLMNOPQRSTUVWXYZ
   !"# $%&'( )=-\@@+*;:<>?,./

9. The following message appears on the terminal:

   EOF FOUND IN FROM FILE AFTER RECORD 2
   3 RECORDS PROCESSED ***0 ERRORS

10. Terminate FCOPY by entering:

    >EXIT

1-32. HP 7920A DISC DRIVE VERIFIER, SLEUTH07

The SLEUTH07 program verifies the operation of an HP 7920A Disc Drive, formats disc packs, and checks packs for surface damage.

The program, which resides in the field support account, must be copied to magnetic tape for subsequent loading after the MPE Operating System is shut down.

Detailed instructions for loading and running SLEUTH07 can be found in the HP 7920A Disc Drive Verifier SLEUTH07 Manual (part number 32230-90002).

The following procedure summarizes disc verification.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES/COMMENTS
Program destroys data stored on customer's disc pack(s). Be sure customer has dumped MPE System using a 0 dump date.	
Cold load SLEUTH 3000 from I/O stand-alone diagnostic tape.	
Press RUN on System Control Panel. Press RETURN on Console.	
	>10 (a typical prompt for input)
Mount tape containing SLEUTH07 and enter: BA E	
	>670 (a typical prompt for input)
Type the SLEUTH RUN command.	
	7920 VERIFIER, ENTER DRT #

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES/COMMENTS
Enter DRT number of disc controller.	
	UNIT SELECT SWITCH TEST? (0=N, 1=Y)
Enter 1	
	ENTER UNIT #, SET SWITCH TO UNIT # ENTERED, PRESS RUN
Enter a unit number 0 through 7. Set Unit Select Switch on disc drive to the same number. Press RUN on the System Control Panel.	
	ENTER UNIT #, SET SWITCH TO UNIT # ENTERED, PRESS RUN.
Question is repeated until you test eight numbers. Then testing continues.	
	ENTER UNIT # TO BE TESTED
Respond with a logical unit number, 0 through 7.	
	FORMAT PACK? (0=N, 1=Y)
Type a one (1) to initialize the pack.	
	VERIFY PACK? (0=N, 1=Y)
Type a one (1) to check the disc pack for surface damage.	
	VERIFY LONG PASS? (0=N, 1=Y)
Type a zero (0) for a short pass. Type a one (1) for a long pass.	
	BEGIN FORMAT (Takes about 10 minutes) END FORMAT
	BEGIN VERIFY (For short and long pass; VERIFY PASS #1 takes about 7 minutes.)
	VERIFY PASS #2 (For long pass only; takes VERIFY PASS #3 about 14 minutes.)
	END VERIFY
	BEGIN MAIN (Main tests require END HEAD TEST about 5 minutes.) END TRACK SWITCH TEST END W/R TEST
	>670 (a typical prompt for input)
Type RUN to repeat SLEUTH07 execution or halt the system.	

1-33. HP 30360A HARDWIRED SERIAL INTERFACE (HSI) PCA DIAGNOSTIC (D432)

The diagnostic verifies the input, output, and control functions of the HP 30360A Hardwired Serial Interface (HSI) PCA. The following procedure is used to verify operation.

NOTE

Prior to running the diagnostic, set the TEST/NORMAL switch (on the HSI cable assembly, part no. 30360-60003) to TEST for the channel to be tested.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Cold load diagnostic D432 from stand-alone diagnostic tape. Press RETURN.	HP 30360A HARDWIRED SERIAL INTERFACE DIAGNOSTIC (D432X.YY.Z) ENTER SWITCH REG. OPTIONS
X = Version YY = Update level Z = Fix level Set SYSTEM SWITCH REGISTER bit 0 off. Press RUN	D400 END SECTION 1 D400 END SECTION 2 D400 END SECTION 3 D400 END SECTION 4 D400 END SECTION 5 D400 END SECTION 6 D500 END OF PASS 1
Program restarts and continues to run until operator presses HALT.	

SYSTEM TROUBLESHOOTING

SECTION II

2-1. INTRODUCTION

This section contains the system troubleshooting procedures and a list of materials required to support the procedures. The troubleshooting is performed on the CPU, memory, multiplexer channel, and selector channel.

2-2. PURPOSE

The system troubleshooting flowchart, figure 2-1, is designed to isolate a fault to a functional area of the system. References are provided in the flowchart to manuals and procedures that may be required to perform certain procedures.

Repair of a defective functional area is usually accomplished by replacement of the defective PCA. Only the Semiconductor Memory Array PCA (30008-60002) and the Fault Correcting Array PCA (30009-60001) are repaired to the component level. Replacement of the memory array chips can only be performed by those specifically trained in this procedure. Attempting replacement by non-trained personnel can ruin the PCA.

NOTE

Only IC memory chips marked with HP part number 5080-4560 can be used for replacements. Reliability of the PCA will be seriously degraded if this note is not observed.

2-3. FACILITIES REQUIRED

The specific items required to perform the troubleshooting on the system are listed in table 2-1.

Table 2-1. Facilities Required

HP 30345A Maintenance Panel
Stand-Alone Diagnostics
System Verification Tape and Listing
CPU Diagnostic Listings (Sections 1 through 5)
Known Good SYSDUMP Tape

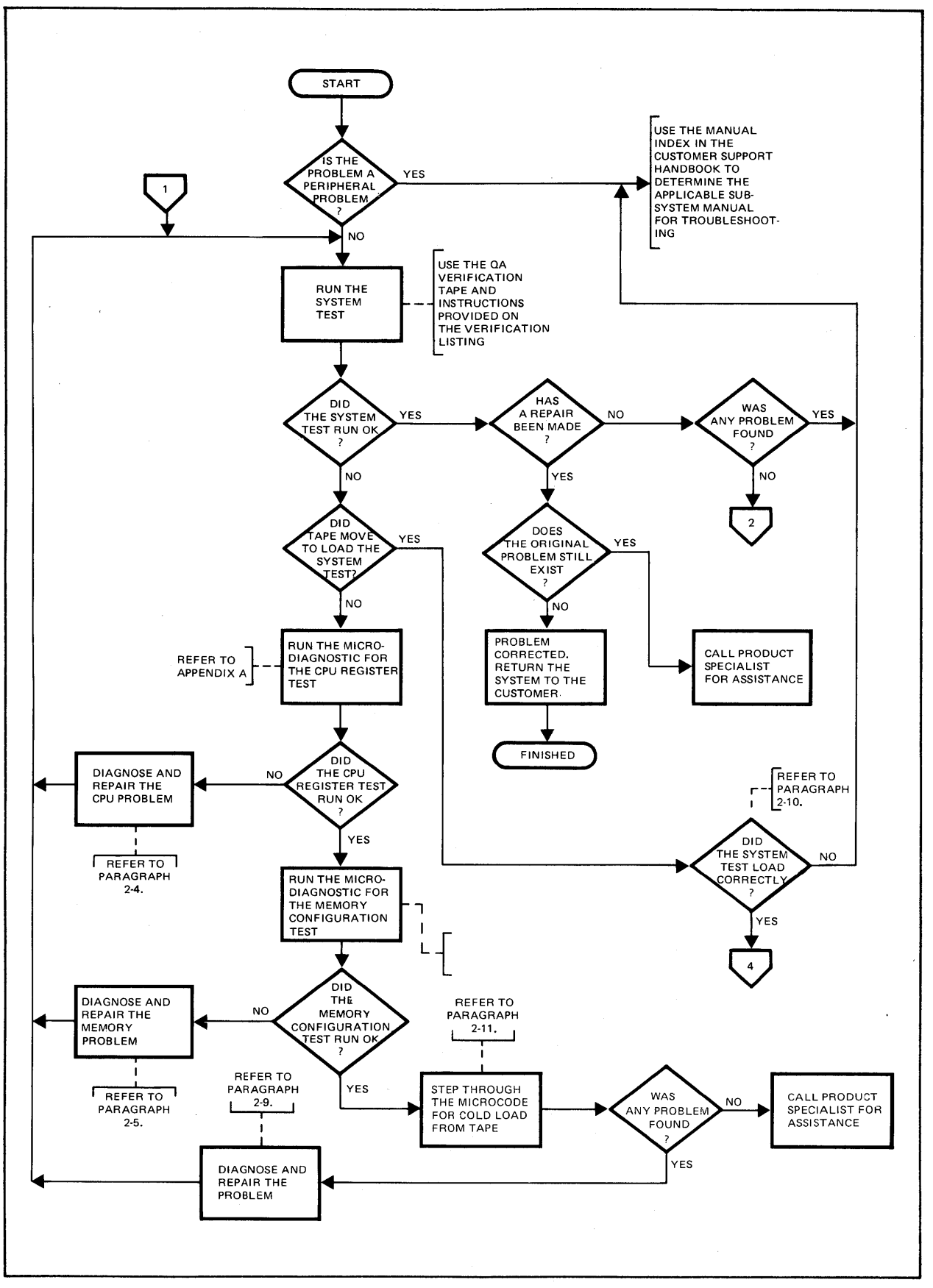


Figure 2-1. System Troubleshooting Flowchart

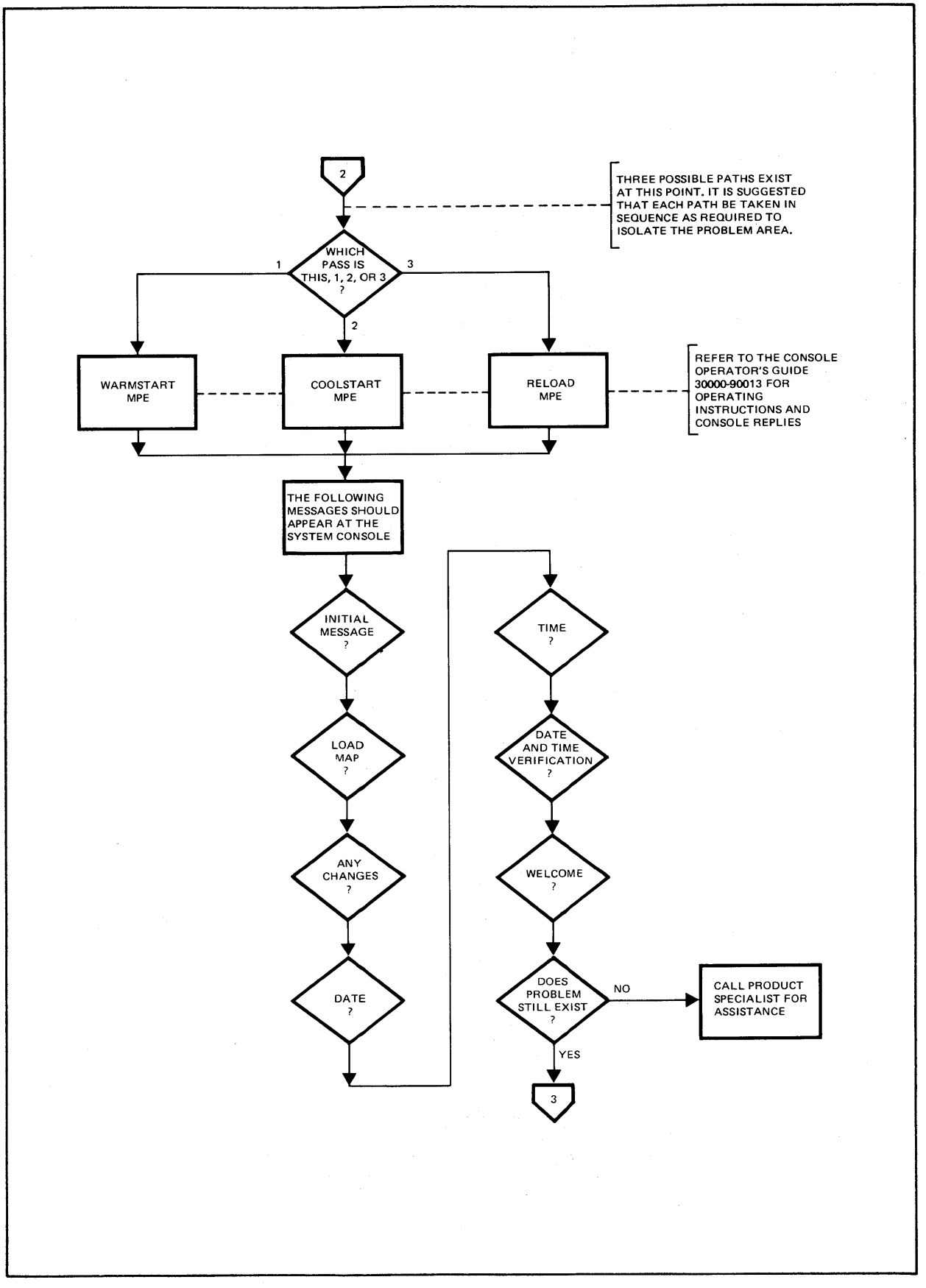


Figure 2-1. System Troubleshooting Flowchart (Continued)

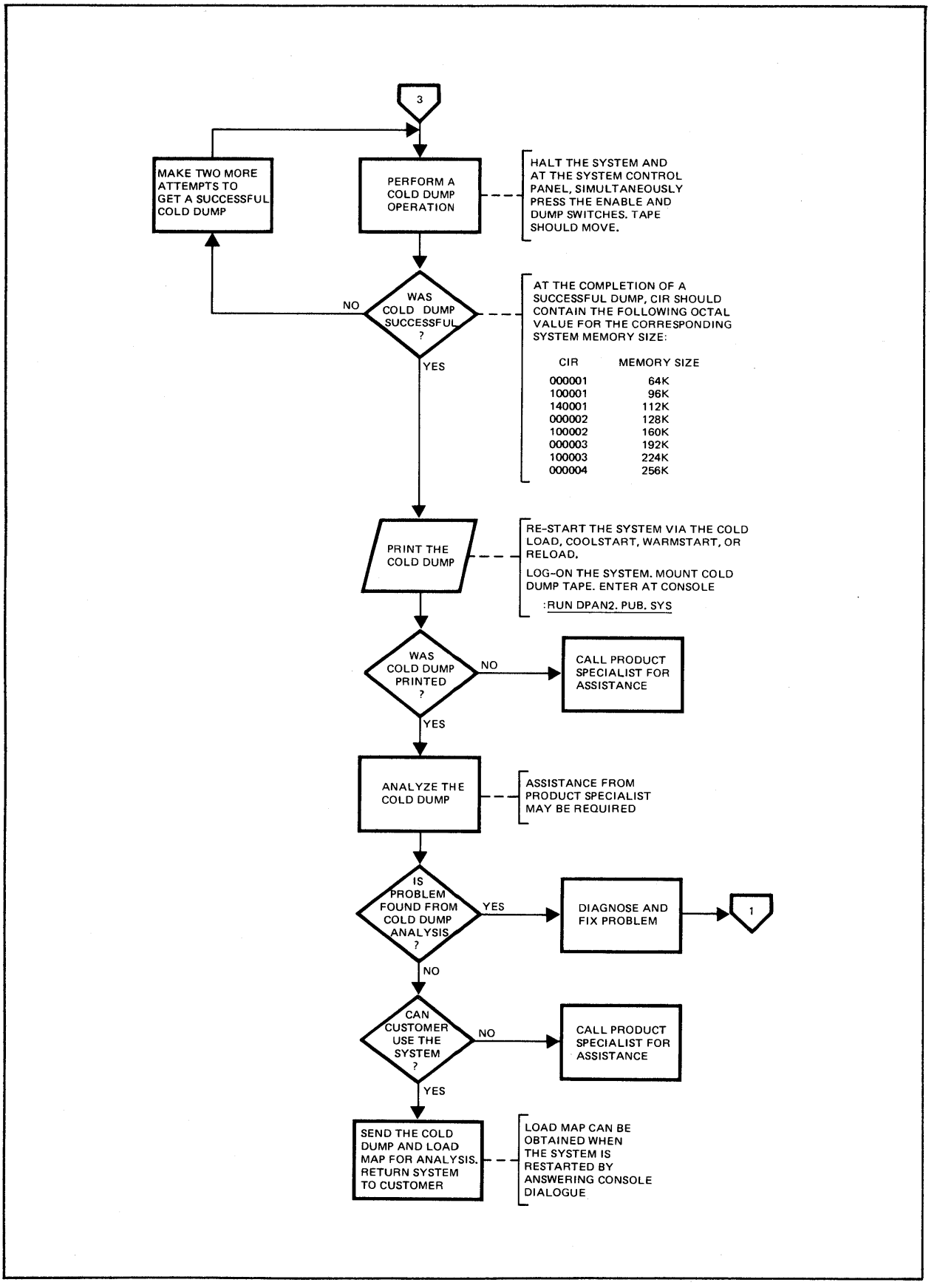


Figure 2-1. System Troubleshooting Flowchart (Continued)

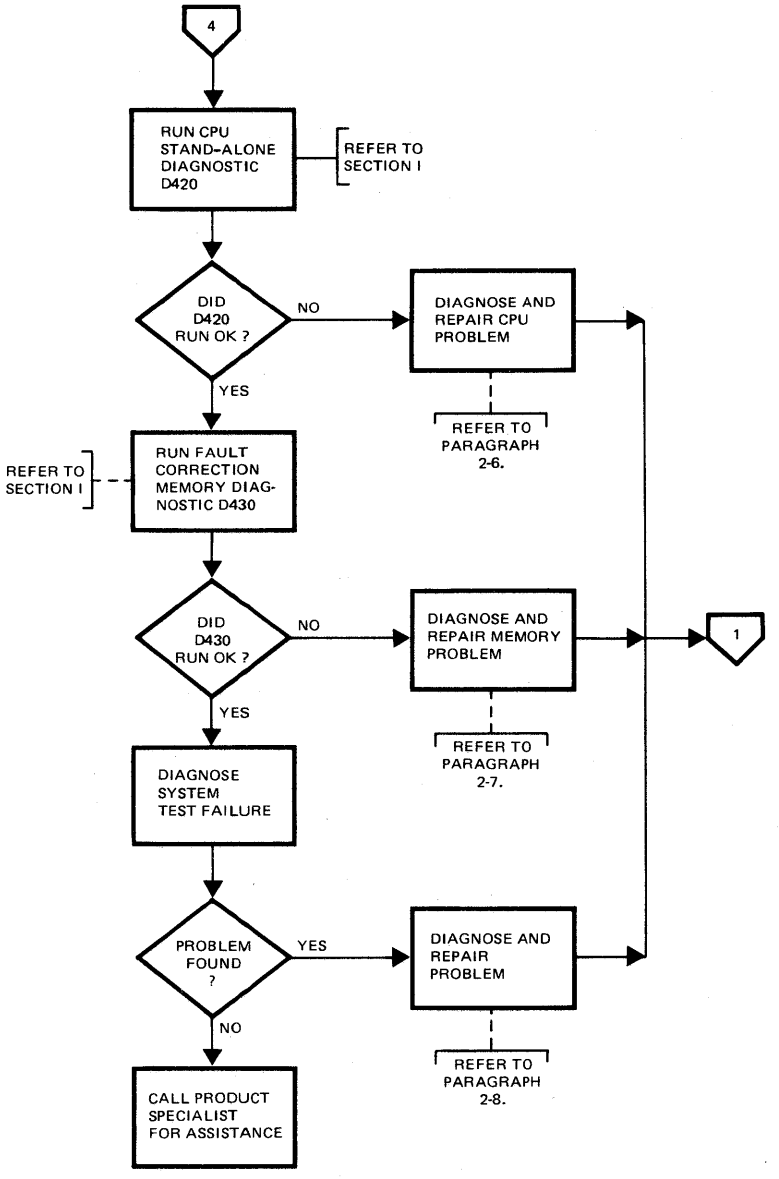


Figure 2-1. System Troubleshooting Flowchart (Continued)

2-4. CPU REGISTER TEST — DIAGNOSIS AND REPAIR

Instructions for running the CPU register test are contained in Appendix A of this manual. Table A-1 in the appendix identifies the PCA's that should be replaced if the diagnostic fails.

2-5. MEMORY CONFIGURATION TEST — DIAGNOSIS AND REPAIR

Appendix B of this manual contains the instructions for running the memory configuration test.

When problems exist with the memory, the following steps are recommended to be performed:

1. Check switch settings and jumper locations on the S-Bus, IOP, SMA, MCL, and Selector Channel Register PCA's.

2. Using the maintenance panel, store and display one location at an address on each SMA PCA.

3. Remove the FCA PCA and run the memory N Squared test as follows:

   a. Load %100200 into the SYSTEM SWITCH REGISTER.

   b. Press LOAD and ENABLE switches.

   c. Program runs until an error occurs. When an error occurs, the program pauses and the CIR contains the error data (lamp on = error bit). By pressing the RUN/HALT switch, the CIR then contains the address information shown in table A-2 in the appendix. The test should be continued by pressing RUN so all memory is tested before any repairs are made. The N Squared test runs approximately 10 minutes for each 32K words of memory.

2-6. CPU STAND-ALONE DIAGNOSTIC — DIAGNOSIS AND REPAIR

The following steps should be performed if the CPU stand-alone diagnostic fails.

1. If a HALT 12 (%030372) — analyze the halt using the diagnostic listing.

2. If other than a HALT 12 — perform the cold load of the diagnostic again but leave switch 8 off.

   a. Check address %10000 after the cold load. If it does not equal a PAUSE, the diagnostic did not load properly.

   b. If address %10000 contains a HALT 10 (%030370), the diagnostic did not load at all.

   c. If address %10000 contains anything other than a HALT 10 or a PAUSE (%030040), the diagnostic was loaded in the wrong locations. Check to see if the initialization program was loaded (refer to SDUPII manual appendix A). If the initialization program loaded incorrectly, there could possibly be a mag tape controller PCA problem or a bad SIO Multiplexer.

   d. If the initialization program loaded correctly but will not execute properly, the LOAD, SETR, or EXIT instructions could cause the problem. Set up the environment specified in Appendix A of the diagnostic manual and use the program listing to determine the fault.

2-7. ERROR CORRECTING MEMORY DIAGNOSTIC — DIAGNOSIS AND REPAIR

The following steps should be performed if the fault correction memory diagnostic fails.

1. Swap the suspected bad PCA into a high memory address location and repeat the diagnostic.

2. Remove the FCA PCA and run the memory N Squared test described in paragraph 2-5.

2-8. SYSTEM TEST — DIAGNOSIS AND REPAIR

Information not available at this time.

2-9. COLD LOAD PROCEDURE — DIAGNOSIS AND REPAIR

Information not available at this time.

2-10. SYSTEM TEST (LOAD)

Information not available at this time.

2-11. COLD LOAD PROCEDURE (TAPE)

This cold load procedure is only valid for ROM PCA's having a date code of 1630.

The following is the SIO program built by the microcode for a cold load from tape:

30=000031
31=014000
32=000000
33=040000
34=000006
35=077740
36=000037
37=034000

Maintenance Panel Set-Up

1. Place all switches down.
2. Set TIMERS switch to INHIBIT.
3. Press SYSTEM RESET switch.
4. Set CLOCK switch to INHIBIT.
5. Press and hold down LOAD switch.
6. Press and count clocks using the CLOCK SINGLE CYCLE switch until the CPU LORQ lamp comes on (60 clocks).
7. Release the LOAD switch.

The SINGLE CYCLE REGISTER DISPLAY switch must be in the REGISTER position (up) to display the Selected Registers given in the following listing.

The following conventions are used throughout the listing:

– = don't care
0 = zero in display

Clocks are counted in decimal, all other numbers are in octal.

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
14	RUN	—	—	—	—	—	—	
60	CPU LORQ	—	—	—	—	—	—	
93	DIRECT ACTIVE FREEZE	1726	1206	—	—	0	—	
94	DIRECT ACTIVE SERVICE OUT FREEZE	1726	1206	—	—	0	—	
95	DIRECT ACTIVE SERVICE OUT FREEZE	1726	1206	—	—	0	—	
96	DIRECT ACTIVE SERVICE OUT FREEZE	1726	1206	—	—	0	—	
97	DIRECT ACTIVE SERVICE IN FREEZE	1726	1206	—	—	0	—	
98	(DROP CPU FRZ)	1726	0	—	—	0	—	
99		1727	0	—	—	0	—	
100	DATA POLL	1730	0	—	—	0	—	<RESULTS OF HSREQ
101	DATA POLL	3273	0	—	—	30	—	
102	DATA POLL	3274	1000	—	—	30	—	

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
103	SERVICE IN SIO ACTIVE DRT REQ I/O LOW REQ	3275	1000	30	—	0	—	<STATE C>
104	SIO ACTIVE DRT REQ I/O SELECT I/O WAIT	3276	1000	30	—	0	30	
105	SIO ACTIVE DRT REQ I/O WAIT	3277	1000	30	—	0	—	
106	SIO ACTIVE DRT REQ I/O WAIT	3275	1000	30	—	0	—	
107	SIO ACTIVE DRT REQ	3276	1000	30	—	0	31	
108	SIO ACTIVE DRT REQ IOB ENABLE DRT STORE	3277	1000	30	—	31	—	<NO DRT STORE, BAD IOP
109	SERVICE OUT SIO ACTIVE DRT REQ IOB ENABLE DRT STORE I/O LOW REQ	3275	1000	30	31	31	—	

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
110	SERVICE IN SIO ACTIVE DRT REQ IOB ENABLE DRT STORE I/O HIRQ I/O SELECT	3276	0	30	33	31	30	<IOP NOT 33, BAD IOP
111	SIO ACTIVE DRT REQ IOB ENABLE DRT STORE I/O SELECT	3277	0	30	33	31	33	<DRT DOESN'T SET, BAD IOP
112		3275	0	30	33	0	—	
113	DATA POLL	3276	0	30	33	0	—	
114	DATA POLL	3277	0	30	33	0	—	
115	DATA POLL	3275	0	30	33	31	—	
116	SERVICE IN SIO ACTIVE I/O LORQ	3276	0	31	33	0	—	
117	SIO ACTIVE I/O WAIT I/O SELECT	3277	0	31	33	0	31	
118	SIO ACTIVE I/O WAIT	3275	0	31	33	0	—	

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
119	SIO ACTIVE I/O WAIT	3276	0	31	33	0	—	
120	SIO ACTIVE I/O WAIT	3277	0	31	33	0	14000	
121	SIO ACTIVE IOB ENABLE	3275	0	31	33	14000	—	
122	SERVICE OUT SIO ACTIVE IOB ENABLE	3276	0	31	33	14000	—	
123	SERVICE IN SIO ACTIVE IOB ENABLE	3277	0	31	33	14000	—	
124		3275	0	31	33	0	—	
125	DATA POLL	3276	0	31	33	0	—	
126	DATA POLL	3277	0	31	33	0	—	
127	DATA POLL	3275	0	31	33	32	—	
128	SERVICE IN SIO ACTIVE I/O LORQ	3276	0	32	33	0	—	
129	SIO ACTIVE I/O WAIT I/O SELECT	3277	0	32	33	0	32	

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
130	SIO ACTIVE I/O WAIT	3275	0	32	33	0	—	
131	SIO ACTIVE I/O WAIT	3276	0	32	33	0	—	
132	SIO ACTIVE I/O WAIT	3277	0	32	33	0	0	
133	IOB ENABLE SIO ACTIVE	3275	0	32	33	0	—	
134	SERVICE OUT SIO ACTIVE IOB ENABLE	3276	0	32	33	0	—	
135	SERVICE IN SIO ACTIVE IOB ENABLE	3277	0	32	33	0	—	
136		3275	0	32	33	0	—	
137	DATA POLL	3276	0	32	33	0	—	
138	DATA POLL	3277	0	32	33	30	—	
139	DATA POLL	3275	1000	32	33	30	—	
140	SERVICE IN SIO ACTIVE DRT REQ I/O LORQ	3276	1000	30	33	0	—	

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
141	SIO ACTIVE DRT REQ I/O WAIT I/O SELECT	3277	1000	30	33	0	30	
142	SIO ACTIVE DRT REQ I/O WAIT	3275	1000	30	33	0	—	
143	SIO ACTIVE DRT REQ I/O WAIT	3276	1000	30	33	0	—	
144	SIO ACTIVE DRT REQ I/O WAIT	3277	1000	30	33	0	33	
145	SIO ACTIVE DRT REQ IOB ENABLE DRT STORE	3275	1000	30	33	33	—	
146	SERVICE OUT SIO ACTIVE DRT REQ IOB ENABLE DRT STORE I/O LORQ	3276	1000	30	33	33	—	

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
147	SERVICE IN SIO ACTIVE DRT REQ IOB ENABLE DRT STORE I/O HIRQ I/O SELECT	3277	0	30	35	33	30	
148	SIO ACTIVE DRT REQ IOB ENABLE DRT STORE I/O SELECT	3275	0	30	35	33	35	
149		3276	0	30	35	0	—	
150	DATA POLL	3277	0	30	35	0	—	<STATE A>
151	DATA POLL	3275	0	30	35	0	—	
152	DATA POLL	3276	0	30	35	33	—	
153	SERVICE IN SIO ACTIVE I/O LORQ	3277	0	33	35	0		
154	SIO ACTIVE I/O WAIT I/O SELECT	3275	0	33	35	0	—	
155	SIO ACTIVE I/O WAIT	3276	0	33	35	0	—	

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
156	SIO ACTIVE I/O WAIT	3277	0	33	35	0	—	
157	SIO ACTIVE I/O WAIT	3275	0	33	35	0	40000	
158	SIO ACTIVE IOB ENABLE	3276	0	33	35	40000	—	
159	SERVICE OUT SIO ACTIVE IOB ENABLE	3277	0	33	35	40000	—	
160	SERVICE IN SIO ACTIVE IOB ENABLE	3275	0	33	35	40000	—	
161		3276	0	33	35	0	—	
162	DATA POLL	3277	0	33	35	0	—	<STATE B>
163	DATA POLL	3275	0	33	35	0	—	
164	DATA POLL	3276	0	33	35	34	—	
165	SERVICE IN SIO ACTIVE I/O LORQ	3277	0	34	35	0	—	
166	SIO ACTIVE I/O WAIT I/O SELECT	3275	0	34	35	0	34	

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
167	SIO ACTIVE I/O WAIT	3276	0	34	35	0	—	
168	SIO ACTIVE I/O WAIT	3277	0	34	35	0	—	
169	SIO ACTIVE I/O WAIT	3275	0	34	35	0	6	
170	SIO ACTIVE IOB ENABLE	3276	0	34	35	6	—	
171	SERVICE OUT SIO ACTIVE IOB ENABLE	3277	0	34	35	6	—	
172	SERVICE IN SIO ACTIVE IOB ENABLE	3275	0	34	35	6	—	
173		3276	0	34	35	0	—	
174	DATA POLL	3277	0	34	35	0	—	
175	DATA POLL	3275	0	34	35	30	—	
176	DATA POLL	3276	1000	34	35	30	—	
177	SERVICE IN SIO ACTIVE DRT REQ I/O LORQ	3277	1000	30	35	0	—	

CLK	LAMPS ON	SELECTED REGISTERS						COMMENTS
		V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	
178	SIO ACTIVE DRT REQ I/O WAIT I/O SELECT	3275	1000	30	35	0	30	
179	SIO ACTIVE DRT REQ I/O WAIT	3276	1000	30	35	0	—	
180	SIO ACTIVE DRT REQ I/O WAIT	3277	1000	30	35	0	—	
181	SIO ACTIVE DRT REQ I/O WAIT	3275	1000	30	35	0	35	
182	SIO ACTIVE DRT REQ IOB ENABLE DRT STORE	3276	1000	30	35	35	—	
183	SERVICE OUT SIO ACTIVE DRT REQ IOB ENABLE DRT STORE I/O LORQ	3277	1000	30	35	35	—	

CLK	LAMPS ON	SELECTED REGISTERS						COMMENTS
		V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	
184	SERVICE IN SIO ACTIVE DRT REQ IOB ENABLE DRT STORE I/O HIRQ I/O SELECT	3275	0	30	37	35	30	
185	SIO ACTIVE DRT REQ IOB ENABLE DRT STORE I/O SELECT	3276	0	30	37	35	—	
186		3277	0	30	37	0	—	
187	DATA POLL	3275	0	30	37	0	—	
188	SERVICE OUT DATA POLL	3276	0	30	37	0	—	
189	DATA POLL	3277	0	30	37	35	—	
190	SERVICE IN SIO ACTIVE I/O LORQ	3275	0	35	37	0	—	
191	SIO ACTIVE I/O WAIT I/O SELECT	3276	0	35	37	0	—	
192	SIO ACTIVE I/O WAIT	3277	0	35	37	0	—	

SELECTED REGISTERS

CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
193	SIO ACTIVE I/O WAIT	3275	0	35	37	0	—	
194	SIO ACTIVE I/O WAIT	3276	0	35	37	0	077740	
195	SIO ACTIVE IOB ENABLE	3277	0	35	37	77740	—	
196	SERVICE OUT SIO ACTIVE IOB ENABLE	3275	0	35	37	77740	—	
197	SERVICE IN SIO ACTIVE IOB ENABLE	3276	0	35	37	77740	—	
198		3277	0	35	37	0	—	
199	DATA POLL	3275	0	35	37	0	—	
200	DATA POLL	3276	0	35	37	0	—	
201	DATA POLL	3277	0	35	37	36	—	
202	SERVICE IN SIO ACTIVE I/O LORQ	3275	0	36	37	0	—	
203	SIO ACTIVE I/O WAIT I/O SELECT	3276	0	36	37	0	36	

		SELECTED REGISTERS						
CLK	LAMPS ON	V-BUS ADDRESS	CMD DEV NO.	IOD	IOP	I/O DATA	CTL	COMMENTS
204	SIO ACTIVE I/O WAIT	3277	0	36	37	0	—	
205	SIO ACTIVE I/O WAIT	3275	0	36	37	0	—	
206	SIO ACTIVE I/O WAIT	3276	0	36	37	0	37	
207	SIO ACTIVE IOB ENABLE	3277	0	36	37	37	—	
208	SIO ACTIVE SERVICE OUT IOB ENABLE	3275	0	36	37	37	—	
209	SERVICE IN SIO ACTIVE IOB ENABLE INTRPT REQ	3276	0	36	37	37	—	
		(TAPE SHOULD MOVE)						
210	INTRPT POLL	3277	6	36	37	0	—	
211	INTRPT POLL INTRPT ACK	3275	6	36	37	0	—	
212	INTRPT ACK EXT INTRPT	3276	0	36	37	0	—	
213	EXT INTRPT	3277	0	36	37	0	—	
214	EXT INTRPT	3300	0	36	37	0	—	
215	EXT INTRPT	3301	0	36	37	0	—	

OPERATION SHOULD BE COMPLETE

MAINTENANCE PANEL OPERATING PROCEDURES

SECTION III

3-1. PURPOSE OF MAINTENANCE PANEL

The HP 30354A Maintenance Panel (figure 3-1) is a troubleshooting aid for the HP 3000 Series II Computer System. When the Maintenance Panel is connected to the system, switches on the panel are used to select specific registers whose content may be observed or changed to assist in localizing system faults. Additionally, lamps on the Maintenance Panel show the contents of many computer registers and the state of principal signals, allowing analysis of system functioning. (For the most part, the visual displays are used only when the computer is halted.) Operating power is provided by the computer system. An interface PCA, installed in the CPU card cage, is required for the Maintenance Panel.

The names of switches and indicators on the Maintenance Panel are marked on an overlay which installs on the face of the unit. A smaller overlay (the I/O overlay) can be placed over a certain row of lamp names on the main overlay to extend the display function of those lamps. A switch permits display of the signals named on the small overlay; other displays remain unchanged. The small overlay can be turned over to provide another set of names; these signals are displayed by making an additional cable connection to the computer system.

As well as being used for equipment fault finding, the Maintenance Panel can be employed for debugging computer programs. However, the Maintenance Panel is not intended for programmers. (A software debug package is available for programmers' use.)

The Maintenance Panel has a self-test capability which allows the operability of most circuits in the Maintenance Panel to be verified without the use of test equipment.

3-2. ITEMS SUPPLIED

The items making up the HP 30354A Maintenance Panel are the following:

- Maintenance panel assembly (mounted on carrying case), no part number.
- Overlay, part no. 30354-80010 — date code 1552, or 30354-80015 — date code 1632
- I/O overlay, part no. 30354-80012
- Maintenance panel interface PCA, part no. 30354-60003 — date code 1552, or 30354-60003 — date code 1632
- Power cable, part no. 30354-60005
- Interface cable, part no. 30354-60007
- Flat cable, part no. 30354-60013

(Overlay part number 30354-80015 — date code 1632 is modified to include shock mounts. Maintenance panel interface PCA, part number 30354-60003 — date code 1632 is modified to include U115 to eliminate a timing problem that prevented cold loading from the maintenance panel when certain ALU PCA's are installed in the system.)

3-3. ADDITIONAL EQUIPMENT

A switch on the Maintenance Panel allows use of an external pulse generator as the source of system clock pulses for the CPU. This permits the CPU to be run at a rate slower or faster than normal, and allows the pulse width to be varied. The change in operating speed and pulse width makes certain types of intermittent failure become steady faults, simplifying troubleshooting.

The pulse generator may be of the general purpose type. The required pulse characteristics are described in table 3-1 (CLOCK EXT/INT entry, row 11 group in the table).

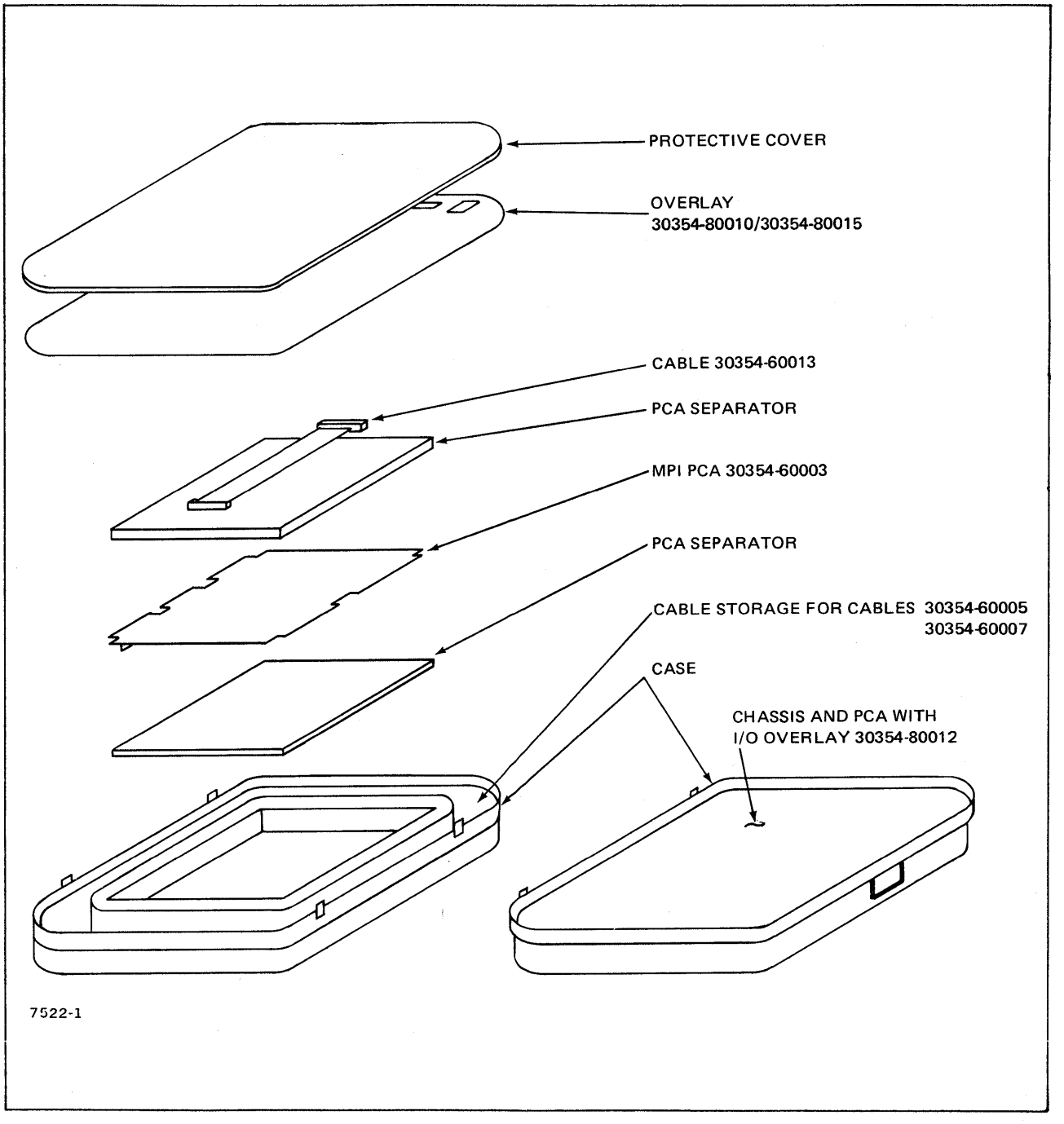


Figure 3-1. HP 30354 Maintenance Panel

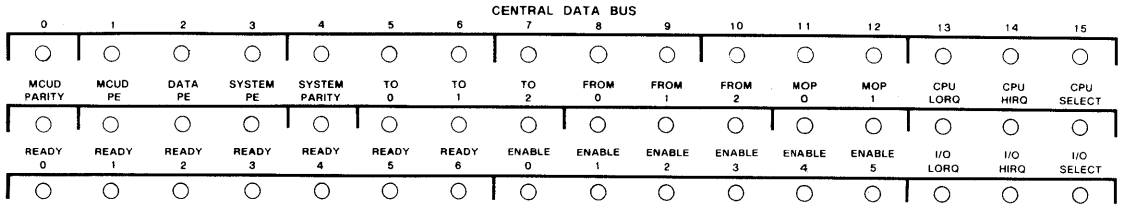


Table 3-1. Maintenance Panel Controls and Indicators

PANEL ROW	PANEL MARKING	USE
1	CENTRAL DATA BUS 0 through 15 (lamps)	These lamps display the data word which is on the central data bus (MCUD 0:15).
2	MCUD PARITY (lamp)	Indicates the state of the CTL bus parity bit.
2	MCUP PE (lamp)	Indicates a parity error has been detected on the CTL bus.
2	DATA PE (lamp)	Indicates there was a parity error detected in the data received by the CPU from memory.
2	SYSTEM PE (lamp)	Indicates a parity error was detected in the information transferred on the TO, FROM, MOP, and SYSTEM PARITY lines.
2	SYSTEM PARITY (lamp)	Indicates the state of the parity bit generated from the TO, FROM, and MOP codes.
2	TO 0, TO 1, TO 2 (lamps)	Display the address for which the word on the CTL bus is intended.
2	FROM 0, FROM 1 FROM 2 (lamps)	Display the address of the module from which the word on the CTL bus is being sent.
2	MOP 0, MOP 1 (lamps)	Display the memory operation code. This code is used by the addressed memory module.
2	CPU LORQ (lamp)	Indicates the CPU is issuing a low priority request for a transfer to a module.
2	CPU HIRQ (lamp)	Indicates the CPU is issuing a high priority request for use of the CTL bus.
2	CPU SELECT (lamp)	Indicates the CPU is currently selected to use the CTL bus.
3	READY 0 through 6 (lamps)	Display the module ready lines. Each line is associated with a like numbered module, and when true, indicates the module is ready to receive a transfer.
3	ENABLE 0 through 5 (lamps)	Display the module enable lines. Each line is associated with a like numbered module, and when true, indicates a module is transferring data. The enable lines are monitored by the modules to resolve priorities.
3	I/O LORQ (lamp)	Indicates the IOP is issuing a low priority request for use of the CTL bus.

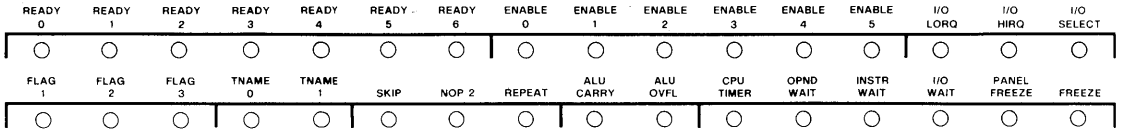


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
3	I/O HIRQ (lamp)	Indicates the IOP is issuing a high priority request for use of the CTL bus.
3	I/O SELECT (lamp)	Indicates the IOP is selected to use the CTL bus.
4	FLAG 1, FLAG 2, FLAG 3 (lamps)	Indicate the states of the three Flag flip-flops controlled primarily by the special field microinstructions.
4	TNAME 0, TNAME 1 (lamps)	Indicate the states of the Top Of Stack namer bits. These bits specify the mapping between the Top Of Stack registers RA, RB, RC, RD, and the associated physical registers.
4	SKIP (lamp)	Indicates a skip condition is met during the current clock cycle.
4	NOP 2 (lamp)	Indicates the state of the NOP 2 bit. When true causes a "no operation" by Rank 2 of the ROM Output Register.
4	REPEAT (lamp)	Indicates the Repeat bit is true, causing the microprocessor to repeat the current microinstruction until the skip condition is met.
4	ALU CARRY (lamp)	Indicates the carry signal from the microprocessor ALU is true.
4	ALU OVFL (lamp)	Indicates the overflow signal from the microprocessor is true.
4	CPU TIMER (lamp)	Indicates that a module did not respond to the CPU within a specified time.
4	OPND WAIT (lamp)	Indicates the CPU is waiting for an operand from memory.
4	INSTR WAIT (lamp)	Indicates the CPU is waiting for an instruction from memory.
4	I/O WAIT (lamp)	Indicates a multiplexed I/O operation is fetching a word from memory.
4	PANEL FREEZE (lamp)	Lighted when a microprogram halt is in effect, or when the V bus carries the same number as the V BUS COMPARE REGISTER switches.
4	FREEZE (lamp)	Indicates the CPU freezable clock has stopped.

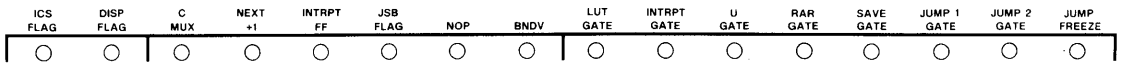


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
5	ICS FLAG (lamp)	Indicates the interrupt stack flag FF is set.
5	DISP FLAG (lamp)	Indicates the dispatcher is executing.
5	C MUX (lamp)	Indicates which instruction is being decoded. Lighted = current instruction, off = next instruction.
5	NEXT + 1 (lamp)	Indicates the sequence is in the "next sequence" state.
5	INTRPT FF (lamp)	Indicates the state of the interrupt FF. When lighted, an external or internal interrupt is pending.
5	JSB FLAG (lamp)	Indicates the microcode is executing a subroutine.
5	NOP (lamp)	Indicates one of the normal inputs of the V Bus are turned off caused by any one of the following: • CPU Reset • PWR ON • UGATE on (RAR in the Store Field) • INTG on (A CPU interrupt is forcing the V Bus to address 3). • The execution of a V Bus jump with panel switches
5	BNDV (lamp)	Indicates a memory instruction references an address outside the limit registers.
5	LUT GATE (lamp)	Indicates an instruction target address is being sent to the V Bus.
5	INTRPT GATE (lamp)	Indicates when doing a NEXT + 1 cycle and a microcode interrupt is pending or when a bounds violation has been detected.
5	U GATE (lamp)	Indicates the U Bus is gated onto the V Bus.
5	RAR GATE (lamp)	Indicates the current address + 1 is put on the V Bus.
5	SAVE GATE (lamp)	Indicates the microcode return address is being gated onto the V Bus.
5	JUMP 1 GATE (lamp)	Indicates the jump target from Rank 1 is being gated onto the V Bus.
5	JUMP 2 GATE (lamp)	Indicates the jump target from Rank 2 is being gated onto the V Bus.
5	JUMP FREEZE (lamp)	Indicates a one cycle freeze is taking place to allow a new V Bus address.

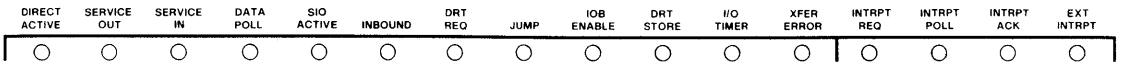


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
6	DIRECT ACTIVE (lamp)	Indicates the IOP is sending out a direct I/O command.
6	SERVICE OUT (lamp)	Indicates to device controller: • For direct commands, the command code, device address, and data on the bus are valid. • For SIO transfers inbound, data on the bus is anticipated. • For SIO transfers outbound, data on the bus is valid.
6	SERVICE IN (lamp)	Indicates a response to an IOP Service Out or Data Poll.
6	DATA POLL (lamp)	Indicates the IOP has received a request for a transfer to or from memory.
6	SIO ACTIVE (lamp)	Indicates a multiplexed I/O operation is in progress.
6	INBOUND (lamp)	Indicates the IOP is executing an inbound memory transfer.
6	DRT REQ (lamp)	Indicates the IOP has received a request from an SIO multiplexer to fetch a DRT entry.
6	JUMP (lamp)	Indicates the IOP is currently updating the DRT pointer during the execution of a jump order.
6	IOB ENABLE (lamp)	Indicates the outbound data is on the IOP Bus.
6	DRT STORE (lamp)	Indicates the IOP is updating the DRT pointer.
6	I/O TIMER (lamp)	Indicates the Service In signal has failed to occur within a period of time after a Service Out signal.
6	XFER ERROR (lamp)	Indicates an I/O data parity exists.
6	INTRPT REQ (lamp)	Indicates the state of the Int Req line from the devices.
6	INTRPT POLL (lamp)	Indicates the state of the Int Poll signal from the IOP to the devices.
6	INTRPT ACK (lamp)	Indicates that an Interrupt Acknowledge signal has been received in response to an interrupt poll.
6	EXT INTRPT (lamp)	Indicates an external interrupt has been acknowledged by the IOP.

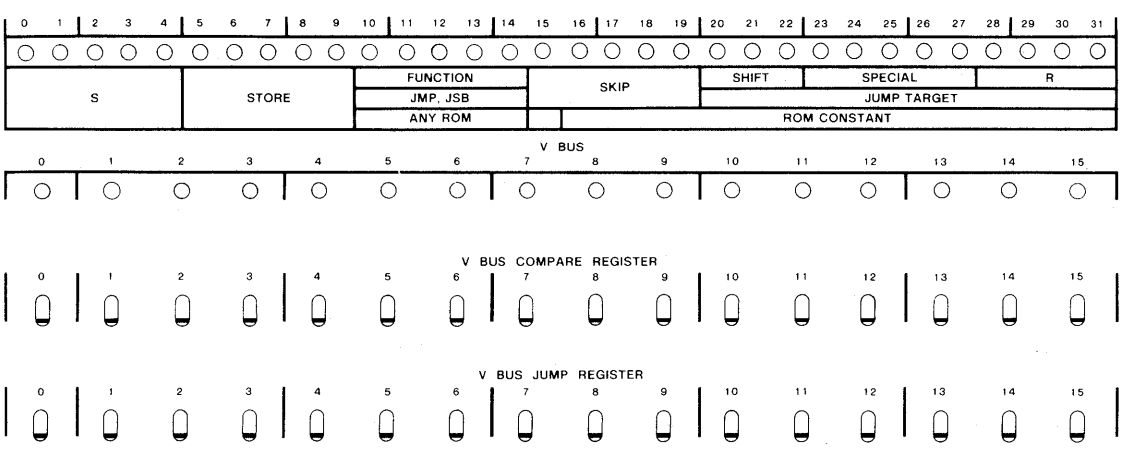


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Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
7	ROM 0 through 31 (lamps)	Displays the contents of the ROM output registers. Lamps (0:4) and (28:31) display ROR1. Lamps (5:27) display ROR2.
8	V BUS 0 through 15 (lamps)	Displays the address of the ROM data currently being accessed, since the ROM is two levels removed from the actual microinstruction being executed out of ROR2, the address is normally two ahead of the address being executed.
9	V BUS COMPARE REGISTER 0 through 15 (bistable switches)	These switches specify the microprogram address at which a V TRIG pulse will be supplied. (The pulse is available at test point E3 at the front of the MPI PCA. It is also available at pin 3, J3, on the MPI PCA.) These switches also specify a microprogram jump address or halt address when the V BUS COMPARE ENABLE/INHIBIT switch is at ENABLE. The V TRIG pulse or breakpoint halt takes place at the completion of a particular clock cycle. To bring about the effect at the desired clock cycle, the microinstruction address set into the V BUS COMPARE REGISTER switches should be as follows: • Address +1 for completion of execution of the R bus and S bus fields. • Address +2 for completion of execution of the remaining microinstruction fields.
10	V BUS JUMP REGISTER 0 through 15 (bistable switches)	These switches specify the jump target for: • Jump resulting from the V bus contents being equal to the contents of the V BUS COMPARE REGISTER switches. • Jump resulting from the V BUS EXECUTE JUMP switch being pressed.

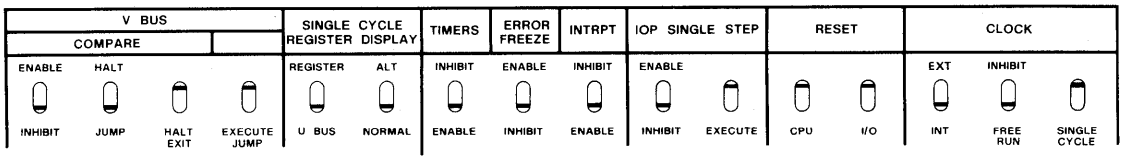


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
11	V BUS COMPARE ENABLE/INHIBIT (bistable switch)	Enables the V BUS COMPARE HALT/JUMP switch.
11	V BUS COMPARE HALT/JUMP (bistable switch)	When enabled by the switch listed above, selects halt or jump when the V bus contents are the same as the V BUS COMPARE REGISTER switches.
11	V BUS COMPARE HALT EXIT (spring-return switch)	When pressed, starts the microprogram after: • A halt brought about by the V BUS COMPARE REGISTER switches. • A freeze brought about a CCPX-14 special field micro-instruction.
11	V BUS EXECUTE JUMP (spring-return switch)	When this switch is pressed, the microprogram jumps to the address in the V BUS JUMP REGISTER switches. **This function should be used only when the computer is halted.**
11	SINGLE CYCLE REGISTER DISPLAY, REGISTER/U BUS (bistable switch)	Selects the REGISTER DISPLAY lamp readout as follows: • With the switch at the REGISTER position, the display is identified by the lighted REGISTER SELECTION lamp. • With the switch at the U BUS position, the U bus is displayed. For this function, the CLOCK INHIBIT/FREE RUN switch (panel row 11) must be at INHIBIT (single cycle operation).
11	SINGLE CYCLE REGISTER DISPLAY ALT/NORMAL (bistable switch)	With this switch at the NORMAL position, RA, RB, RC, and RD on the S bus PCA can be displayed by the REGISTER DISPLAY lamps. With the switch at ALT, RA, RB, RC, and RD on the R bus PCA can be displayed. Also, with the switch at NORMAL, SP1 and pre-adder are displayed from the S bus; with the switch at ALT, SP1 and the pre-adder are displayed from the R bus. This switch must be at NORMAL to store into RA, RB, RC, RD, or SP1 from the Maintenance Panel.
11	TIMERS (bistable switch)	Enables or disables the CPU, memory, IOP, and selector channel timers.

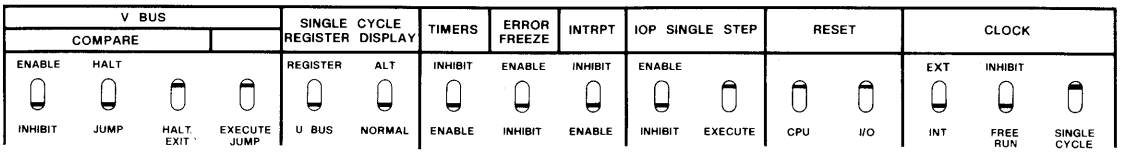


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
11	ERROR FREEZE (bistable switch)	In the ENABLE position, this switch causes a freeze when any of the following occurs: • Illegal memory address • Memory address parity error • MCUD parity error • System parity error • I/O data parity error • I/O address parity error To end the freeze, the ERROR FREEZE switch is set to the down position.
11	INTRPT (bistable switch)	When the computer is running, setting this switch to INHIBIT causes all internal and external interrupts to be ignored, with the exception of the power failure interrupt. When the switch is returned to the ENABLE position, the previously ignored interrupts are processed. The switch performs no function when the computer is halted.
11	IOP SINGLE STEP ENABLE/INHIBIT (bistable switch)	Enables or disables the IOP SINGLE STEP EXECUTE switch.
11	IOP SINGLE STEP EXECUTE (spring-return switch)	When enabled by the switch listed above, the IOP executes one step each time the switch is pressed.
11	RESET CPU (spring-return switch)	The CPU and MCU are reset when this switch is pressed. To avoid improperly changing the contents of registers, the switch should be pressed only when the computer is halted.
11	RESET I/O (spring-return switch)	All I/O subsystems are reset when this switch is pressed.
11	CLOCK EXT/INT (bistable switch)	At the INT position, this switch allows the CPU to use the clock pulse generated within the CPU. At the EXT position, the switch selects a clock pulse produced by an external pulse generator. The external clock-pulse must have the following characteristics: • Source impedance: 50 ohms or less. • Source must sink up to 60 ma. • High level: +2.5V to 5.0V. • Low level: 0.0V to 0.4V. • Maximum rise time: 10 nsec. • Maximum fall time: 10 nsec. • High time: 20 nsec to infinite time. • Low time: 20 nsec to infinite time. • Maximum frequency: 25.0 MHz. • Minimum frequency: 0 Hz.

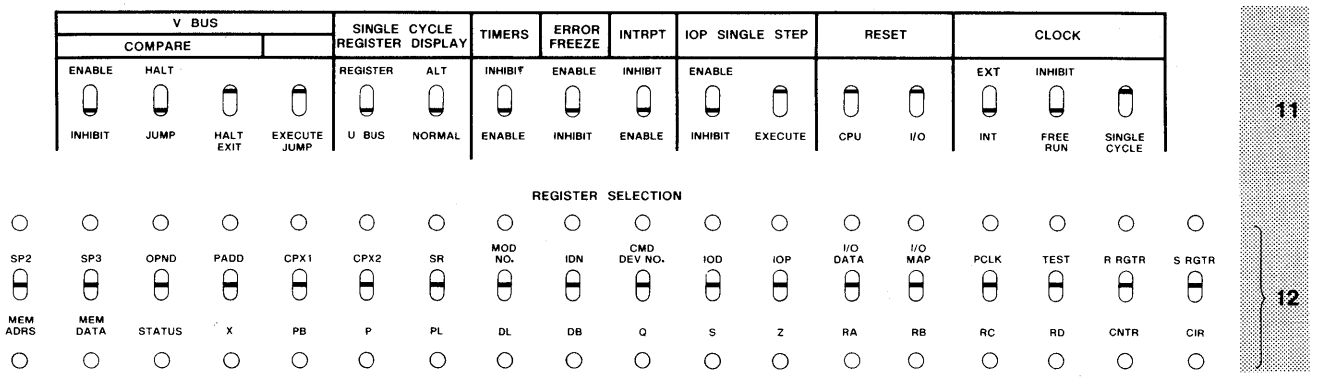


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
		To equal the internal clock-pulse rate, the external clock-pulse frequency must be 22.8571 MHz. This corresponds to a period of 43.75 nsec, which, because of a divide-by-four action in the CPU, provides a 175-nsec computer clock cycle. The external clock-pulse is supplied to a BNC-type connector on the CPU backplane. The connector is labelled EXT — CLOCK. A 50-ohm termination impedance is provided in the CPU.
11	CLOCK INHIBIT/FREE RUN (bistable switch)	In the INHIBIT position, this switch permits the CPU to execute one machine cycle each time the CLOCK SINGLE CYCLE switch is pressed. In the FREE RUN position of the switch, the CPU operates continuously using either internal or external clock pulses.
11	CLOCK SINGLE CYCLE (spring-return switch)	When enabled by the CLOCK INHIBIT/FREE RUN switch, pressing this switch causes execution of one CPU machine cycle.
12	REGISTER SELECTION (lamps and center off spring-return switches)	When pressed up or down, each switch lights the lamp above or below it, and turns off any other lighted lamp in the group. The lighted lamp identifies the register displayed by the REGISTER DISPLAY lamps. The B14 and B15 lamps remain extinguished except as stated below. The lighted REGISTER SELECTION lamp also identifies the register which will be loaded by either of the LOAD REGISTER switches. The following registers cannot be loaded by the LOAD REGISTER FROM SW RGTR switch; these are identified below as "display only" registers.

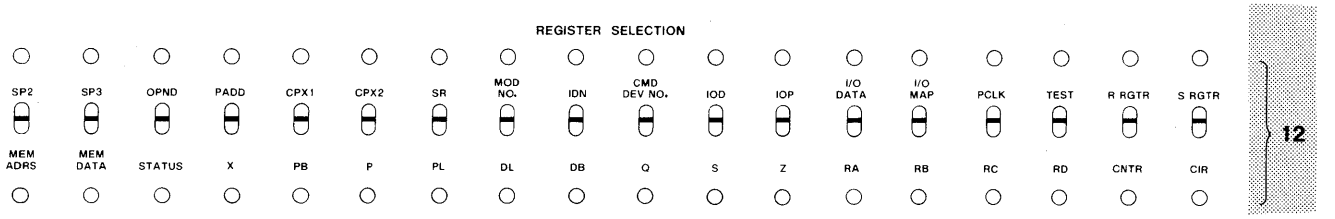


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
		Special comments are as follows: • OPND, display only. • PADD, display only. • CPX1, display only. • CPX2, display only. • SR, display only. • MOD NO., display only. The module number appears in positions 5, 6, and 7 of the REGISTER DISPLAY lamps. If the computer is CPU no. 1, position 13 of the REGISTER DISPLAY lamps is lighted. If the computer is CPU no. 2, position 12 is lighted. • IDN, display only. • CMD DEV NO., display only. The I/O command is displayed in positions 5 through 7; the device number is in positions 8 through 15. Positions 0 through 4 of the display do not light. • IOD, display only. Displays (via the S bus) the contents of the IOD-input register. • IOP, display only. Displays the contents of the data-in register. • I/O DATA, display only. Displays the data on the IOD (0:15) bits. On the IOP bus, these bits are in "not" form; however, the "not" bits are inverted before display. Thus there is no overbar over the mnemonic. • I/O MAP, display only. To identify the I/O Map bits, the I/O overlay (part no. 30354-80012) is placed over the REGISTER DISPLAY lamps. • PCLK, display only. • TEST, display only. Displays any 16 bits applied to J3 on the maintenance panel interface PCA. • R RGTR, display only. • S RGTR, display only. • MEM ADRS displays the memory address (SP0) in REGISTER DISPLAY (0:15), and the ABS bank register in B14 and B15. This lamp is called MEM ADRS because SP0 contains the address when memory is accessed by means of the MEMORY STORE or MEMORY DISPLAY switches.

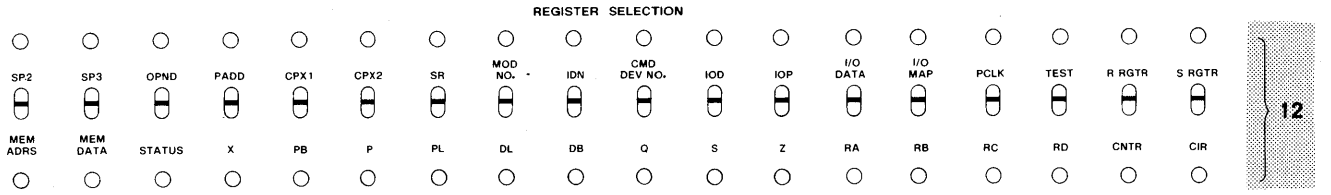


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
		• MEM DATA displays the memory data (SP1) in REGISTER DISPLAY (0:15). B14 and B15 will be zero. This lamp is called MEM DATA because SP1 receives the data when memory is displayed by means of the MEMORY DISPLAY switch. • SP2 displays the contents of the scratch pad 2 register, used by the microcode. B14 and B15 will be zero. • SP3 displays the contents of the scratch pad 3 register, used by the microcode. B14 and B15 will be zero. • RA displays the contents of the top of stack register. B14 and B15 will be zero. • RB displays the contents of the second stack register. B14 and B15 will be zero. • RC displays the contents of the third stack register. B14 and B15 will be zero. • RD displays the contents of the fourth stack register. B14 and B15 will be zero. • STATUS displays the CPU status register. • PB displays the PB status register in REGISTER DISPLAY (0:15). B14 and B15 display the PB bank register. • P displays the P register in REGISTER DISPLAY (0:15). B14 and B15 display the PB bank register. • PL displays the PL register in REGISTER DISPLAY (0:15). B14 and B15 display the PB bank register; these two bits are display only. • DL displays the contents of the DL register in REGISTER DISPLAY (0:15). B14 and B15 display the stack register; these two bits are display only. • DB displays the data base register in REGISTER DISPLAY (0:15). B14 and B15 display the DB bank register. • Q displays the Q register in REGISTER DISPLAY (0:15). B14 and B15 display the stack bank register; these two bits are display only. • S displays the S register in REGISTER DISPLAY (0:15). B14 and B15 display the stack bank register; these two bits are display only. • Z displays the Z register in REGISTER DISPLAY (0:15). B14 and B15 display the stack bank register.

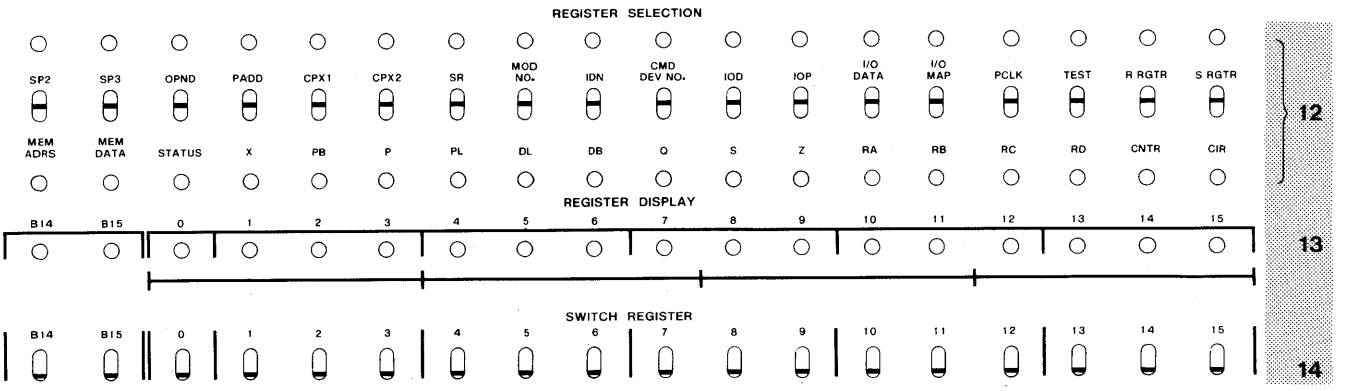


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
		• CNTR, display bits 10:15. • CIR, display only. Display valid only when the CLOCK IN HIBIT/FREE RUN switch is at INHIBIT position (single cycle operation).
13	REGISTER DISPLAY 0 through 15, B15, and B14 (lamps)	Display the register identified by the lighted REGISTER SELECTION lamp. The REGISTER DISPLAY lamps also indicate the data which will be loaded by the LOAD REGISTER, MEM ADDRS FROM DISPL switch.
14	SWITCH REGISTER 0 through 15, B15 and B14 (bistable switches)	Switches 0 through 15 provide a 16-bit word to: • Load in a selected register by means of the LOAD REGISTER FROM SWITCH RGTR switch. • Store in memory by means of the MEMORY STORE switch. • Use as an instruction word when the EXECUTE SW RGTR switch is pressed. • Match with a word read from memory to cause a read breakpoint halt (using the BREAKPOINT READ ENABLE switch). • Match with a word stored in a memory storage operation to cause a store breakpoint halt (using the BREAKPOINT STORE ENABLE switch). Switches B15 and B15 are used to change the contents of the following two-bit bank registers by means of the LOAD REGISTER FROM SW RGTR switch: • ABS bank register (MEM ADRS register selected). • PB bank register (PB register selected). • Stack bank register (Z register selected). • DB bank register (DB register selected).

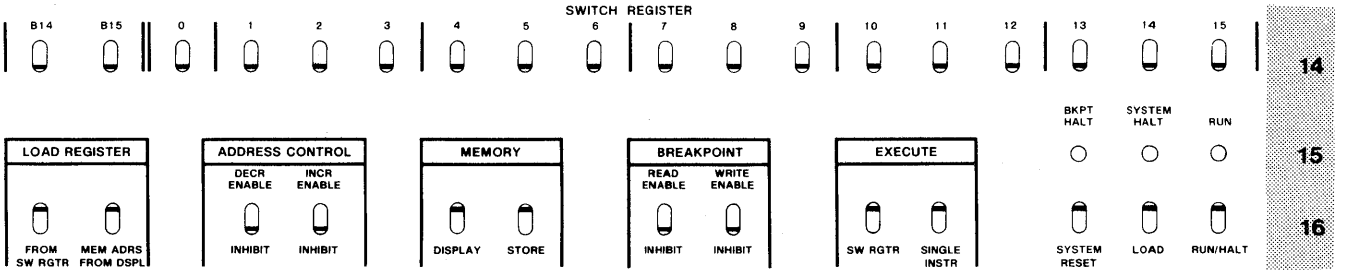


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
		Except as listed above, switches B14 and B15 produce no effect when registers are manually loaded. A further use of switches B14 and B15 is to specify the memory module number for breakpoint halts (using the BREAKPOINT STORE ENABLE/INHIBIT switch).
15	BKPT HALT (lamp)	Lighted during a breakpoint halt caused by either of the following switches: • BREAKPOINT READ ENABLE/INHIBIT • BREAKPOINT STORE ENABLE/INHIBIT
15	SYSTEM HALT (lamp)	Lighted during a system halt (caused by an irrecoverable error).
15	RUN (lamp)	Lighted when the CPU is running.
16	LOAD REGISTER FROM SW RGTR (spring-return switch)	When pressed, the register indicated by the lighted REGISTER SELECTION lamp is loaded with the contents of the SWITCH REGISTER switches. The bank registers may also be loaded, as explained in the SWITCH REGISTER description above.
16	LOAD REGISTER, MEM ADDRS FROM DISPL (spring-return switch)	When pressed, the memory address register (SP0) is loaded with the bits displayed by the REGISTER DISPLAY (0:15) lamps. Also, the ABS bank register is loaded with the bits displayed by the REGISTER DISPLAY B14 and B15 lamps. The MEMORY DISPLAY or MEMORY STORE switch can then display or store at the 18-bit address.
16	ADDRESS CONTROL, DECR ENABLE/INHIBIT (bistable switch)	When this switch is at ENABLE, the memory address register (SP0) is decremented by 1 each time the MEMORY DISPLAY or MEMORY STORE switch is pressed. (The ADDRESS CONTROL INCR ENABLE/INHIBIT switch should be at INHIBIT.)
16	ADDRESS CONTROL INCR ENABLE/INHIBIT (bistable switch)	When this switch is at ENABLE, the memory address register (SP0) is incremented by 1 each time the MEMORY DISPLAY or MEMORY STORE switch is pressed. (The ADDRESS CONTROL DECR ENABLE/INHIBIT switch should be at INHIBIT.)

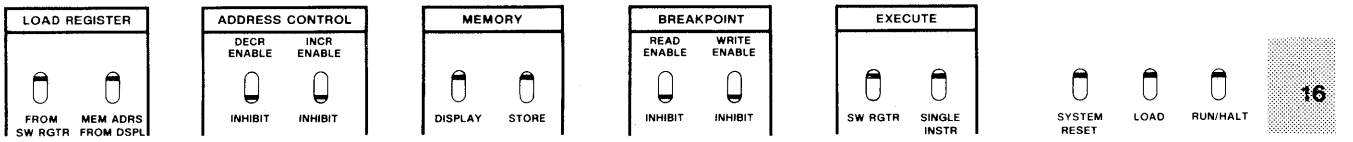


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
16	MEMORY DISPLAY (spring-return switch)	When this switch is pressed, the following takes place: • The REGISTER SELECTION MEM DATA lamp lights. Any other lighted lamp in this group goes out. • The REGISTER DISPLAY (0:15) lamps show the contents of the memory address specified by the ABS bank register and the memory address register (SP0). Lamps B14 and B15 remain extinguished. • The memory address register (SP0) is incremented or decremented by 1 if one of the ADDRESS CONTROL switches is at ENABLE. A carry from SP0 does not enter the ABS bank register.
16	MEMORY STORE (spring-return switch)	When this switch is pressed, the following takes place: • The contents of the SWITCH REGISTER (0:15) switches are stored in memory at the address indicated by the ABS bank register and the memory address register (SP0). • The memory address register (SP0) is incremented or decremented by 1 if one of the ADDRESS CONTROL switches is at ENABLE. A carry from SP0 does not enter the ABS bank register.
16	BREAKPOINT READ ENABLE/INHIBIT (bistable switch)	In the ENABLE position, this switch halts the CPU when a 16-bit word read from memory is the same as the word in the SWITCH REGISTER (0:15) switches.
16	BREAKPOINT WRITE ENABLE/INHIBIT (bistable switch)	In the ENABLE position, this switch halts the CPU when memory storage takes place at an address which is in the SWITCH REGISTER B14, B15, and (0:15) switches.
16	EXECUTE SW RGTR (spring-return switch)	When this switch is pressed, the CPU executes the instruction in the SWITCH REGISTER (0:15) switches. The P-register contents do not change when the instruction is performed unless the instruction of the branch type; in this case the P-register receives the target address if the branch condition is met. If a stack operation is performed, stack operation B should be NOP. (That is, positions 10 through 15 of the SWITCH REGISTER must contain 0's.)
16	EXECUTE SINGLE INSTR (spring-return switch)	When this switch is pressed, the instruction indicated by the P-register is executed. The P-register is incremented by 1, or it is loaded with a target address if the instruction is of the branch type and the branch condition is met.

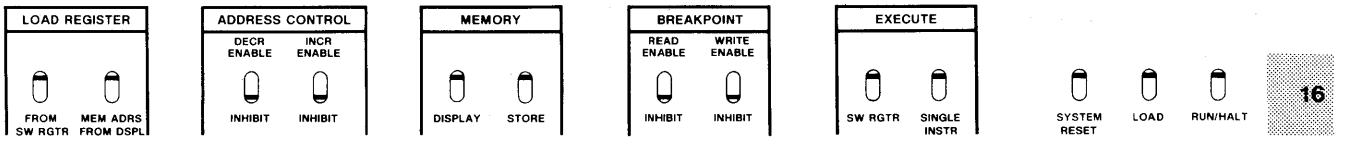


Table 3-1. Maintenance Panel Controls and Indicators (Continued)

PANEL ROW	PANEL MARKING	USE
		If the instruction is of the double stack type, the switch must be pressed twice to execute both halves of the instruction. The first depression causes execution of stack operation A. The second depression causes execution of stack operation B. If operation B is other than NOP, bit 3 of the CPU status register is set to 1 during stack operation A. This bit is cleared at the start of stack operation B. The P-register is incremented during stack operation B unless B is NOP, in which case it is incremented during A.
16	SYSTEM RESET (spring-return switch)	When pressed, this switch resets the CPU and the I/O system.
16	LOAD (spring-return switch)	Stores in memory from an I/O device specified in the SWITCH REGISTER switches.
16	RUN HALT (spring-return switch)	Pressing this switch halts the CPU if it is running, or starts the computer if it is halted. Both halves of a stack op instruction are always completed before the halt takes place. If the CPU halts while an SIO operation is in progress, the SIO operation continues to its normal completion.

3-4. OPTIONS

An option 001 is available for the Maintenance Panel. The option allows use of the Maintenance Panel with other HP 3000 Computer Systems. An instruction manual, part number 30354-90005 is furnished with the option.

3-5. SWITCHES AND LAMPS

Figure 3-2 illustrates Maintenance Panel switches and lamps. The shaded numbers on the right side of figure 3-2 identify the row number of lamps or switches and are used in table 3-1 as an aid to locating the switch or lamp. The I/O overlay is shown in figure 3-3. When referring to a switch or lamp, this manual uses the name physically marked on the equipment. The name is quoted in capital letters to indicate it is an equipment marking.

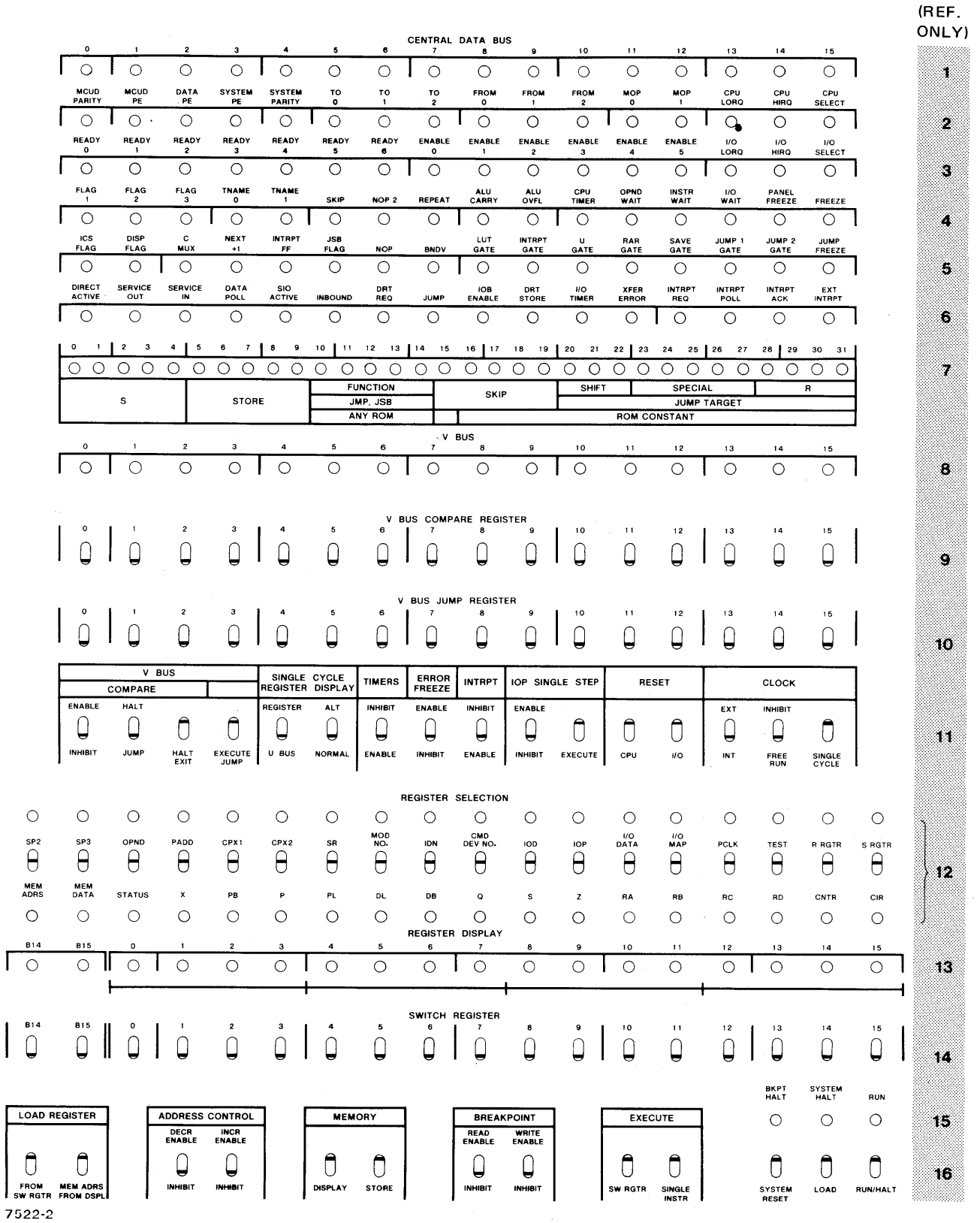


Figure 3-2. Maintenance Panel Switches and Lamps

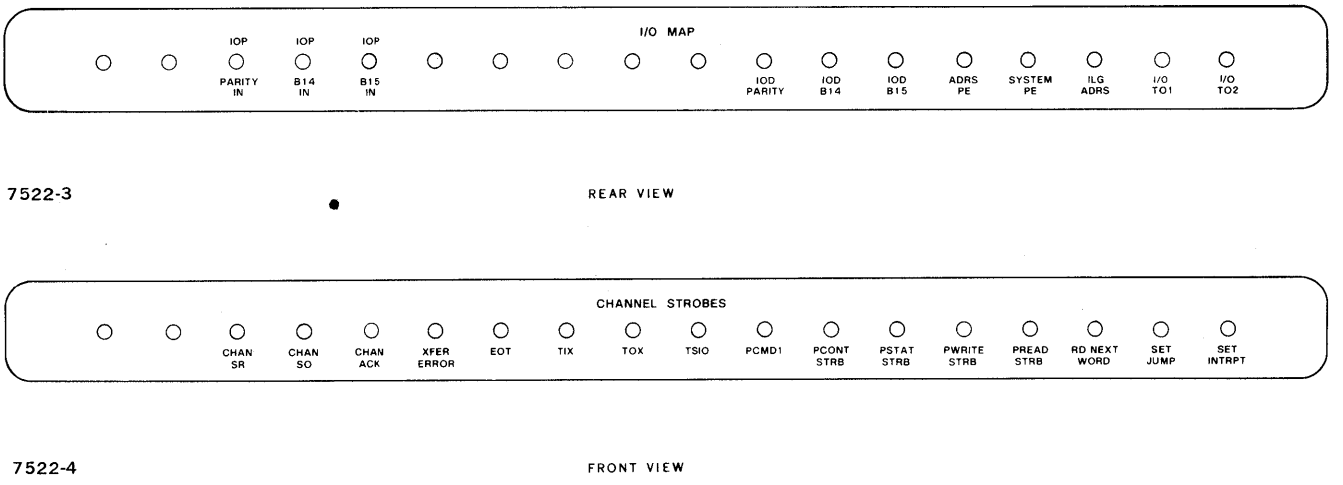


Figure 3-3. I/O Overlay

Switches on the Maintenance Panel are of three types:

- Bistable switches. These switches have two positions, and can remain in either the up or the down position. In the down position they have no effect on normal computer functioning, and they are left in this position except when their particular functions is required. In figure 3-2, the bistable switches can be identified by the fact that they are in the down position.
- Two-position spring-return switches. These switches are pressed down when their function is required. When released, they return to the up position.
- Three-position spring-return switches. These switches have a center-off position. They are pressed up or down to produce the desired function. When released, they return to the center position. All switches of this type are in row 12 of figure 3-2.

Lamps which display register contents are lighted when the particular position of the register contains a binary 1.

Lamps which display the state of a signal are lighted when the signal is in the asserted state. That is, a lamp is lighted when a "not" signal is low; for other signals, a lamp is lighted when the signal is high.

Table 3-1 explains the function of each switch and lamp on the Maintenance Panel.

3-6. OPERATING METHODS

3-7. PRECAUTIONS

The operating system, if in use, may cause unexpected changes in computer functioning when Maintenance Panel switches are actuated. These unexpected changes result from such factors as stack overflow, etc. The Maintenance Panel operator therefore should be familiar with the operating system.

3-8. PREPARATION FOR USE

To use the Maintenance Panel, make preparation as follows:

- Ascertain that the computer system is not in use.
- Inform potential users that the system is unavailable until further notice.
- Set the SYSTEM DC POWER switch (at the top of bay 1) to the STANDBY position.
- Install maintenance panel interface (MPI) PCA 30354-60003 in slot 1 of the CPU card cage.
- At the front of the MPI PCA, set switch S1 to the NORMAL position. (This switch is labelled NORMAL/LAMP TEST/SWITCH TEST.)
- Make the connections shown in figure 3-4.
- If required, install the 30354-80012 I/O overlay over the REGISTER DISPLAY lamps. If using the CHANNEL STROBES side of this overlay, connect jack J3 on the MPI PCA to J1 on the selector channel maintenance PCA.
- Set to the down position all bistable switches on the Maintenance Panel.
- Apply power to the computer system.

3-9. GENERAL OPERATING METHOD

When using the Maintenance Panel, operate switches to achieve the desired results, observing indications shown by the lamps. Refer as necessary to table 3-1 and the applicable program documentation.

To prevent unauthorized use of the Maintenance Panel, set switch S1 on the MPI PCA to the SWITCH TEST position. This prevents Maintenance Panel switch information from entering the computer system. Note that if a power failure occurs with S1 at SWITCH TEST, the switch must be returned to the NORMAL position to permit initialization of the computer system for restart after power is restored.

3-10. SWITCHES AND INDICATORS ON BAY 1 CONTROL PANEL

When the Maintenance Panel is in use, switches and indicators on the bay 1 control panel function in the normal manner. The following points apply:

- The CPU can be started or halted either by the RUN-HALT on the Maintenance Panel or by the RUN/HALT switch on the bay 1 control panel.
- If the LOAD switch on the bay 1 control panel is used, the appropriate information must be set into the SWITCH REGISTER on the bay 1 control panel. Similarly, use of the LOAD switch on the Maintenance Panel requires that the SWITCH REGISTER on the Maintenance Panel be used.
- The RSW instruction acquires the 16-bit word which is in the SWITCH REGISTER on the bay 1 control panel, as in normal operation.

3-11. STACK REGISTER LOADING

Because of the queue-down function which occurs when the CPU halts, stack registers must be loaded at their location in memory. For test purposes it is possible to load the stack registers which are on the S bus PCA and R bus PCA; however, when queue-up takes place after the CPU is started, the register contents will be destroyed.

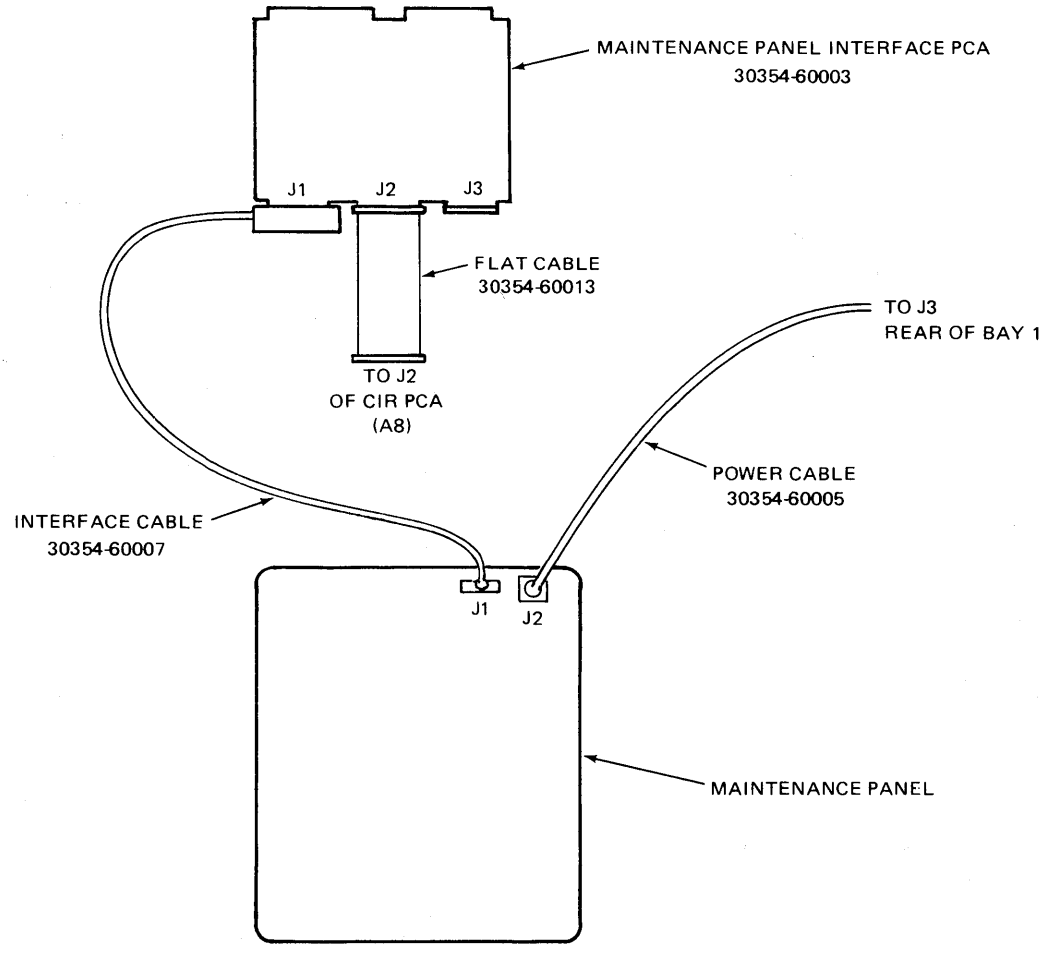


Figure 3-4. Connections for Use

3-12. CPU REGISTER DISPLAYS

When CPU registers are displayed, the register contents are acquired either from the computer S bus or R bus, dependingnon the bus to which the register is gated in the computer. In the case of the stack registers, SP1, and the preadder, a switch on the Maintenance Panel permits display from either the S bus or the R bus; this switch is titled SINGLE CYCLE REGISTER DISPLAY, ALT/NORMAL (panel row 11).

3-13. GENERAL-USE DISPLAY

When the REGISTER SELECTION TEST lamp is lighted, any 16 bits or 16 binary signals can be applied for display to jack J3 of the MPI PCA (figure 3-4). The bits or signals must have TTL silicon logic levels. They are displayed in the REGISTER DISPLAY (0:15) lamps on the Maintenance Panel. The pins in J3 to which connection is made are listed in table 3-2. The table also shows two trigger pulses and a + 5 volt source; these are supplied by the MPI PCA. The $\overline{MR}$ signal is an input to the PCA, used for factory test purposes.

For any particular application of the general-use display, a cardboard overlay can be made for the REGISTER DISPLAY lamps, with appropriate signal names marked on the overlay. (A ticket punch is a suitable device for making the holes in the cardboard.)

3-14. MAINTENANCE PANEL TEST

The following test checks the operability of most circuits in the Maintenance Panel. Most circuits in the MPI PCA are not checked. If performed as described, and if step *a* below has previously been completed, the test can be executed without interfering with normal computer functioning. (Switch information from the Maintenance Panel does not enter the computer system when switch S1 on the MPI PCA is at the SWITCH TEST position.)

3-15. LAMP TEST

To exercise the lamp test function, perform the following steps:

a. Connect the Maintenance Panel to the computer system in the normal manner (figure 3-4). Before making connection, be sure + 5 volts has been removed from the system, and make sure all bistable switches on the Maintenance Panel are down.

b. At the MPI PCA, set switch S1 to the LAMP TEST position. Every lamp on the Maintenance Panel should light.

c. Set S1 to the SWITCH TEST position. Some lamps should go out.

CAUTION

Before performing step *d* below, be sure S1 has been set to the SWITCH TEST position, otherwise switch information may enter the computer system. The switch information is the result of voltage spikes produced when the plug is removed from J1.

d. Remove the plug from receptacle J1 on the Maintenance Panel. All lamps should go out. Replace the plug.

Table 3-2. Pin Connections, J3 of MPI PCA*

PIN	SIGNAL
1	MCU TRIG
3	V TRIG
5	$\overline{MR}$
7	+5 volts (100Ω source)
19	REGISTER DISPLAY 0
21	REGISTER DISPLAY 1
23	REGISTER DISPLAY 2
25	REGISTER DISPLAY 3
27	REGISTER DISPLAY 4
29	REGISTER DISPLAY 5
31	REGISTER DISPLAY 6
33	REGISTER DISPLAY 7
35	REGISTER DISPLAY 8
37	REGISTER DISPLAY 9
39	REGISTER DISPLAY 10
41	REGISTER DISPLAY 11
43	REGISTER DISPLAY 12
45	REGISTER DISPLAY 13
47	REGISTER DISPLAY 14
49	REGISTER DISPLAY 15
*All even-numbered pins are ground.	

3-16. SWITCH TEST

The switches on the maintenance panel can be tested by placing the switch on the MPI PCA to the SWITCH TEST position. This routes the switch information back to the maintenance panel to be displayed by lighting or extinguishing one or more lamps for each switch. The data from the switches will be displayed by nine groups of lamps. See figure 3-5.

The information for the REGISTER SELECTION switches is coded into six binary bits. These bits are displayed twice by the lamps in group five. Figure 3-5 illustrates the individual groups of lamps and also indicates by each switch which lamp/lamps will illuminate or extinguish when the switch is exercised.

Note: Although twelve groups of lamps are designated in figure 3-5, not all of the groups of lamps will be exercised during the switch test.

The bistable switches, shown in the down position, will illuminate the lamp/lamps indicated by the numbers above the switch when the switch is placed up. The two-position spring return switches, shown in the up position, will extinguish the lamps indicated by the numbers below the switch when the switch is held down. The three-position spring return switches (REGISTER SELECTION switches) have a code above and below the switch that will be displayed when the switch is held in that position. Stenciling on the panel has not been shown for clarity. Where two pairs of numbers are present, two lamps will be illuminated. For example, 1,8 and 9,8 signify that group 1 lamp 8 and group 9 lamp 8 will be illuminated when the switch is exercised, the lamps will extinguish when the switch is off. The reverse condition applies to the two-position spring return switches, extinguishing the lamps when the switch is exercised.

When exercising the REGISTER SELECTION switches, a binary coded value is presented by the lamps in group five. The coded value appears twice, in bits 0-5 and bits 8-13. The indications presented by bits 8-13 should be ignored.

CAUTION

After the switch test is complete, be sure all bistable switches on the Maintenance Panel are in the down position before restoring S1 on the MPI PCA to the NORMAL position. This will prevent information from entering the computer when the switch is returned to NORMAL.

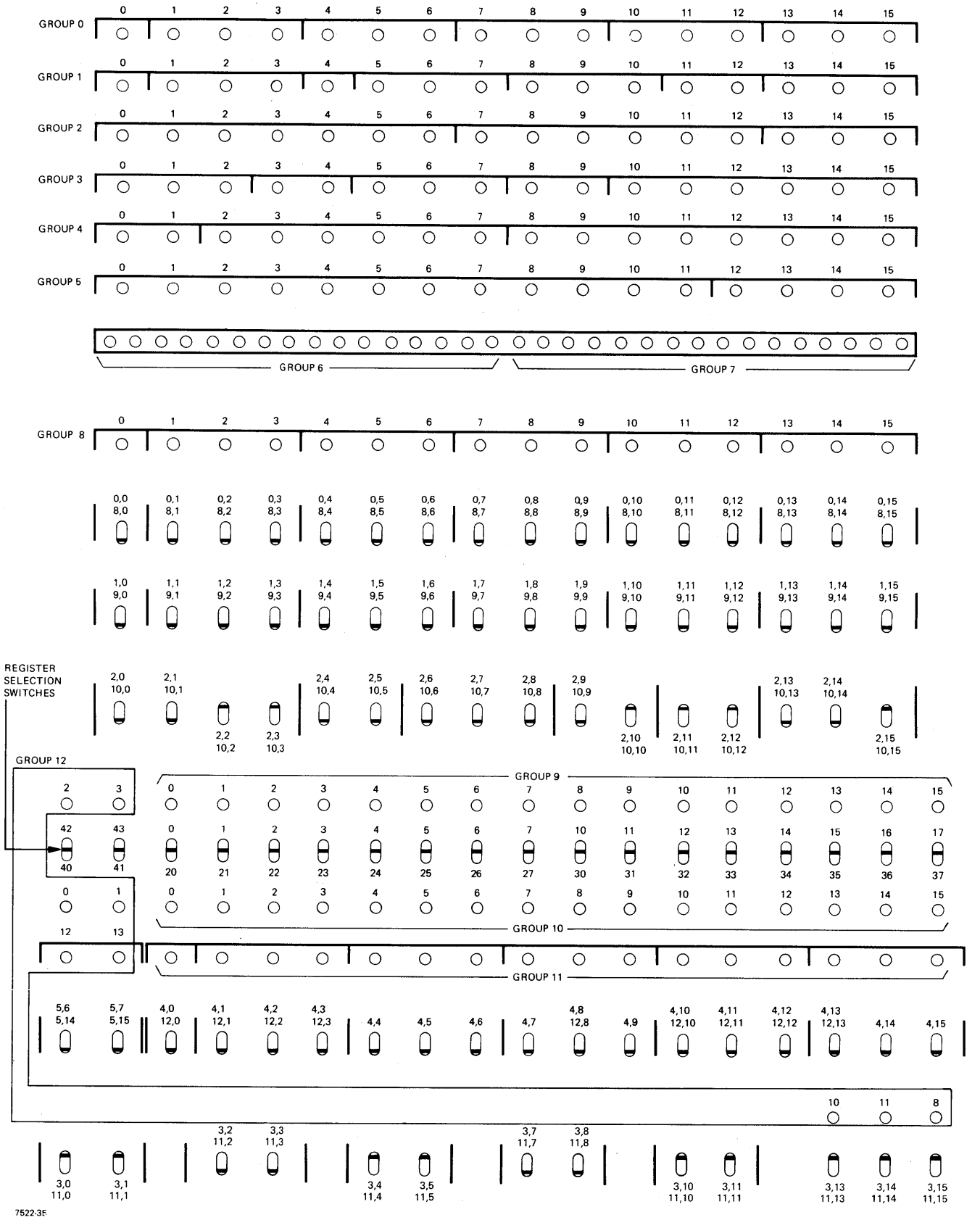


Figure 3-5. Switch Test Lamp Indications

MAINTENANCE PROCEDURES

SECTION IV

4-1. INTRODUCTION

This section includes general servicing information, safety precautions, repair philosophy, memory chip replacement information, and PCA jumper information. Principles of operation and principal servicing points of the memory module are also presented in this section.

4-2. SAFETY PRECAUTIONS

When performing maintenance on the system, observe all cautions and warnings placarded in the cabinet and included in this manual. Failure to observe the warnings could result in injury or death.

WARNING

Dangerous voltages are present in the HP 3000 Computer System power control module and cabinet ac power distribution. Exercise extreme caution when working in these areas when covers and panels have been opened for troubleshooting convenience.

WARNING

Two men are required to remove the HP 30310A Power Supply from its mounting hinge in an equipment cabinet. This power supply weighs 50 pounds (22.7 kilograms).

4-3. REPAIR PHILOSOPHY

The repair philosophy for the system is to replace a defective PCA, and not troubleshoot to the defective component. The exceptions are the Semiconductor Memory Array PCA (30008-60002) and the Fault Correction Array PCA (30009-60001). These PCA's are repaired to the component level. Repair of these PCA's should only be performed by CE's specifically trained for this task.

The repair philosophy for the three power supplies (HP 30310A, HP 30311A, and HP 30312A) limits field repair to replacing open fuses. If any other problem arises with a power supply, the entire unit should be replaced. Power supplies are non-repairable items maintained on an exchange basis.

4-4. GENERAL SERVICING INFORMATION

A prime consideration to be remembered when servicing the HP 3000 Series II Computer System is the power requirement of the memory module. Unlike core memory, data will be lost or altered when power is removed from this dynamic solid state memory. A battery back-up power supply (HP 30311A) is installed in the system to provide power to the memory module when the system is turned off for maintenance, for PCA replacement, or when system AC input power is interrupted. A full description of this power supply, its function, operation, adjustment procedures, and associated lamp indications, is contained in Appendix B.

The following is a brief summary of the switch settings on the DC Control Panel (located behind the front door of equipment bay 1) used when performing maintenance functions:

- Memory module PCA replacement:
  MEMORY DC POWER - STANDBY

- Non-memory module PCA replacement:
  SYSTEM DC POWER - STANDBY

- Extended shutdown (memory data lost)
  SYSTEM DC POWER - STANDBY
  MEMORY DC POWER - STANDBY
  HP 30311A Power Supply - off

When any PCA is replaced, ensure that it sits in the slots with the extractor handles locked. All cable connectors should be firmly seated on the PCA's.

NOTE

Prior to performing any maintenance or shutdown procedures, have the System Operator verify that all jobs/sessions have been terminated before proceeding.

4-5. I/O ERROR LOGGING

I/O error logging capability (log files) exists within the system software but must be enabled for use. Discuss the use of this feature with the system manager/supervisor. Refer to the System Manager/ Supervisor Reference Manual (30000-90014) for a description and use of log files.

4-6. MEMORY ERROR LOGGING

Memory logging is always activated when MPE is initialized. The logging process is automatic and requires no operator intervention. To examine the log file, a user with system manager capabilities need only enter the following:

```
:FILE OUT;DEV=LP
:RUN MEMLOGAN.PUB.SYS
(.PUB.SYS required if the user is not signed on the SYS account)
```

The line printer will then reproduce the contents of the log file. Refer to paragraph 4-99 for a complete description of the error logging facility.

4-7. ADJUSTING SYSTEM VOLTAGES

Voltage measurements to be made in the following procedures must reference the appropriate common circuit. The common circuits are labelled COM and common symbol, and are specified in the following instructions. Use an HP 3439A Digital Voltmeter with an HP 3441A Range Selector (or their equivalent).

1. Allow at least 15 minutes warm-up time, preferably with the CPU in the RUN state (RUN lamp lit).

2. Check the control panel at the top front of the full length door on the CPU bay. If the RUN lamp is lit, press the top of the RUN/HALT switch to turn-off the RUN lamp.

3. Behind the front door of equipment bays, look for the small panel of an HP 30312A Power Supply. For each HP 30312A Power Supply in the system, perform these steps:

   a. Set the ADJ R32 potentiometer fully clockwise.

   b. Press and hold toggle switch S2 and turn ADJ R32 counterclockwise until the LED in the upper-right corner of the HP 30312A panel lights to indicate "over-current".

   c. Release toggle switch S2 and check that the over-current LED goes out and a 5V LED lights.

4. Open the rear door of equipment bay number 1, remove the screw(s) at the left edge of the HP 30310A Power Supply and swing that Power Supply out of the bay.

5. At the top of the HP 30310A Power Supply, turn R12 fully clockwise.

6. Connect the digital voltmeter between the +5VDC connector (BNC type) center conductor and a COM terminal lug on the backplane of the CPU card cage.

NOTE

DO NOT connect the digital voltmeter common lead to chassis ground. Failure to heed this note will produce erroneous and possibly destructive results.

7. Use a small tip screwdriver to reach through the top of the HP 30310A Power Supply to adjust A1R1 until the digital voltmeter displays +5.17 volts.

8. Leave the digital voltmeter common lead where it is now but move input lead to the +15, −5, and −15 test jacks on the HP 30310A rear panel. The voltmeter should display a value between 14.7 and 16.5 for either the +15 or −15 test jacks, and between 4.5 and 5.3 for the −5 test jack.

9. Move the voltmeter input lead to the +20 test jack on the HP 30310A panel, then use a small tip screwdriver to reach through the top of the HP 30310A Power Supply to set A3R2 fully clockwise and leave at this setting. The voltmeter should display a value between 16.9 and 17.7 volts.

10. Move the voltmeter input lead to the −20 test jack; the same value (but opposite polarity) noted in step 9 should be displayed.

11. Repeat steps 4 through 10 for each HP 30310A Power Supply in the system.

12. Move the voltmeter to the front of the equipment bays.

13. Connect the voltmeter common or return lead to the common symbol jack on the front panel of the HP 30311A Power Supply in the CPU bay.

14. Connect the input lead of the voltmeter to each of the test jacks on the HP 30311A Power Supply front panel and compare the value displayed against table 4-1.

15. If all the values displayed are out of tolerance, proceed no further until the +5.00V Internal Reference Adjustment procedure described in Appendix B, have been performed on the HP 30311A Power Supply.

16. Repeat steps 13 through 15 for each HP 30311A Power Supply in the system.

Table 4-1. HP 30311A Test Jack Voltages

TEST JACK	VALUE REQUIRED
+5	+5.0; +−0.125
+12	+12.0; +−0.12
+12.7	value of +12 test jack, +0.9, −0.5
−3	−3.0; +−0.15
−5	−5.0; +−0.05

4-8. SELECTOR CHANNEL MAINTENANCE PCA (SCMB) 30033-60001

The selector channel maintenance board PCA (SCMB) was designed to aid in the maintenance of the selector channel and multiplexer channel. Under solftware control (usually the selector channel diagnostic) the SCMB can exercise all selector channel data paths and control circuitry. All I/O program orders can be executed and device dependent sequences such as conditional jump, device end, and clear interface can be exercised selectively. Also, device timeout conditions can be simulated causing a timeout error in the selector channel. The following paragraphs contain information for installing and using the SCMB.

4-9. JUMPERS

Three jumpers must be configured on the SCMB. (See figure 4-20.) They are:

- XW1 — This jumper selects whether the SCMB is to be used on the selector channel or the multiplexer channel. A plug-in socket containing two jumper wires is installed in XW1. If the jumper wires are aligned with SC on the PCA, the PCA is enabled for use with the selector channel. If the jumper wires are aligned with MX, the PCA is enabled for use with the multiplexer channel.

NOTE

When jumper XW1 is in the MX position and the SCMB is installed in the multiplexer channel, the selector channel diagnostic verifies the operation of the SCMB.

- MUX SR — This jumper selects a service request number used when the SCMB is used with a multiplexer channel. This 16-position jumper should be installed to provide a service request number not used by any other device controller in the system.

- XW2 — These jumpers select the SCMB device number. A jumper wire installed selects a "0" in that position. Use a device number not already assigned.

4-10. SELECTOR CHANNEL INSTALLATION

To install the SCMB in a selector channel, perform the following steps:

a. Set the SYSTEM DC POWER switch to STANDBY.

b. Ensure that jumper XW1 is properly installed.

c. Refer to the System Support Log and ensure that the SCMB device number is not used by any other device in the system.

d. Install the SCMB in an empty slot on the selector channel bus for the channel to be used.

e. Install the interrupt poll for the SCMB.

f. Set the SYSTEM DC POWER switch to ON.

4-11. MULTIPLEXER CHANNEL INSTALLATION

To install the SCMB in the multiplexer channel, perform the following steps:

a. Set the SYSTEM DC POWER switch to STANDBY.

b. Ensure that jumper XW1 is properly installed.

c. Refer to the System Support Log and ensure that the SCMB device number is not used by any other device in the system.

d. Install the SCMB in an empty slot on the multiplexer channel bus.

e. Install the interrupt poll for the SCMB.

f. If a second SCMB is to be installed, repeat steps a through e.

g. Set the SYSTEM DC POWER switch to ON.

4-12. SCMB VERIFICATION

The operation of the SCMB can be verified by installing the SCMB in the multiplexer channel and running the selector channel diagnostic. The SCMB can be verified by performing the following procedure.

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGES
Verify that all jumpers are properly installed in the SCMB. Jumper XW1 must be in the MX position during this verification procedure. Ensure that the DRT number and interrupt poll are wired correctly. Install the SCMB in the multiplexer channel.	

OPERATOR ACTION/COMMENTS	CONSOLE MESSAGE
Cold load the selector channel diagnostic (D429) from the stand-alone diagnostic tape. Press RETURN	D100 HP30030B SELECTOR CHANNEL DIAG (D429X.YY.Z) Q104 SELECT OPTIONS
X = Version YY = Update level Z = Fix level Set SYSTEM SWITCH REGISTER bit 0 off. Press RETURN	Q110 SELECT SECTION OPTIONS
Press RETURN	Q101 SET MAINT CARD DEV NUM?
Enter in decimal the DRT number of the SCMB. Press RETURN	Q102 SET TIMER/CONSOLE DEV NUM?
Enter in decimal the DRT number of the system timer (usually 3). Press RETURN	Q108 ENTER UPPER BANK # =
Enter in decimal the number of the highest memory bank in the system. Press RETURN	Q109 ENTER UPPER ADDRESS (OCTAL) =
Enter in octal the highest memory address in the system. Press RETURN	Q105 ERR PRINT LIMIT ?
Enter in decimal the maximum number of error messages you wish to receive. Press RETURN	D110 DIRECT I/O TEST D127 DIRECT I/O TEST COMPLETED D130 CONTROL ORDER TEST

4-13. SCMB STATE DISPLAY

The state of pertinent signals associated with the SCMB can be displayed on the maintenance panel as follows (see figure 4-1).

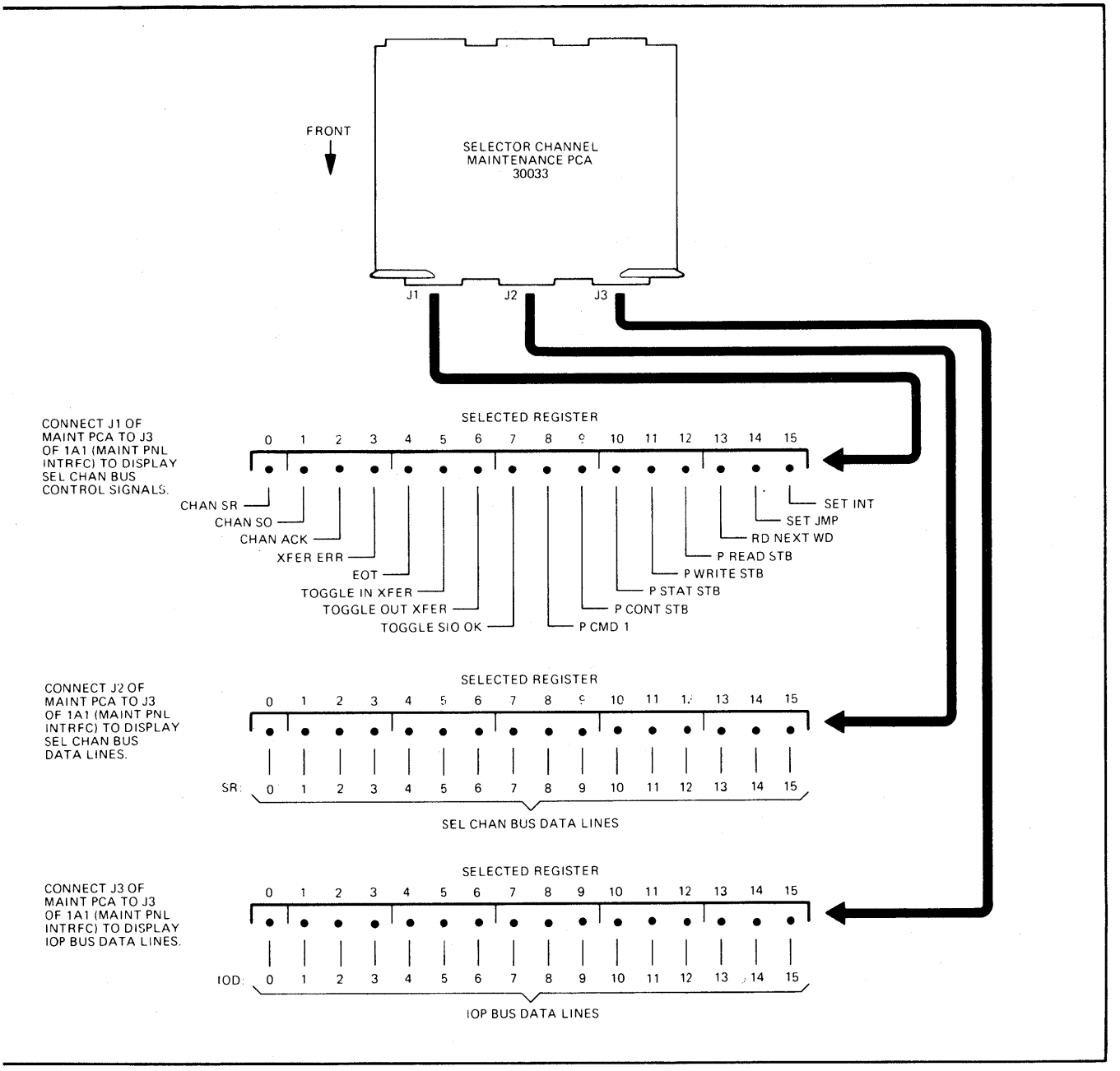
a. Connect with a flat cable, connector J3 of 1A1 (the maintenance panel interface PCA) to either J1 (to display SEL CHAN BUS control signals), J2 (to display SEL CHAN BUS data signals), or J3 (to display IOP BUS data signals) of the SCMB.

b. Set the maintenance panel CLOCK switch to INHIBIT.

c. Refer to figure 4-1 for the meaning of the information displayed on the REGISTER DISPLAY indicators.

NOTE

The system can be permitted to run in the free run mode with this setup. However, the display is valid only in the single cycle mode.



522-34

Figure 4-1. SCMB State Display

4-14. PROGRAMMING

The principal components illustrated in figure 4-2 comprise the SCMB. Like any device controller, the SCMB is programmed through the use of direct I/O instructions issued by the CPU/IOP and through I/O program orders executed by the selector channel. SCMB operation is initially configured when a control word is issued by a direct Control I/O instruction. To initiate execution of an I/O program (and therefore channel operation) an SIO instruction is issued to the SCMB. The SCMB also provides a 16-bit status word to report on various maintenance PCA and selector channel operating conditions.

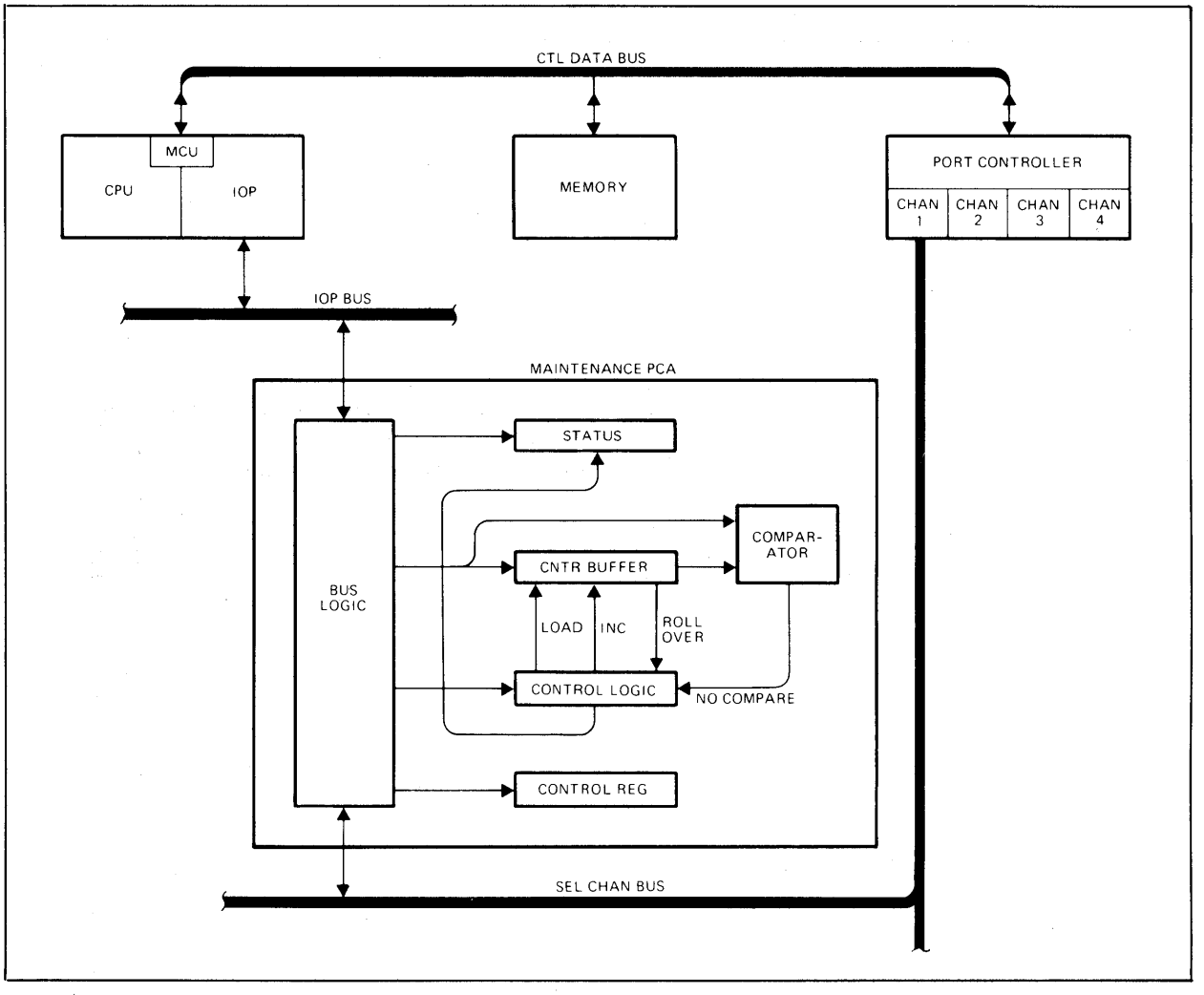


Figure 4-2. SCMB Block Diagram

4-15. I/O INSTRUCTIONS. The following is a list of applicable I/O instructions and their effect upon the SCMB.

a. SIN Instruction — Sets the SCMB interrupt request flip-flop.

b. CIO Instruction — Loads a control word from the TOS into the SCMB control register.

c. SIO Instruction — Initiates I/O program execution if the channel is inactive. The SIO instruction is rejected if the channel is currently active.

d. WIO Instruction — Loads a data word from the TOS into the counter/buffer.

e. RIO Instruction — Sends the contents of the counter/buffer to the TOS.

f. TIO Instruction — Returns the SCMB status word to the TOS.

g. SMSK Instruction — This instruction is ignored because the SCMB has no mask flip-flop.

4-16. I/O PROGRAM ORDERS. The following is a list of applicable I/O program orders and their effect on the SCMB.

a. Control — Refer to paragraph 4-16 below.

b. Write — Loads a data word from memory into the counter/buffer if IOCW bit 11 is a "0", compares the data word from memory to the counter/buffer contents if control word bit 11 is a "1".

c. Read — Sends the contents of the counter/buffer to memory.

d. End — Returns the SCMB status word to the End order IOAW location and terminates I/O program execution. An interrupt occurs if bit 4 is set.

e. Interrupt — Sets the SCMB interrupt request flip-flop.

f. Sense — Returns the SCMB status word to the Sense order IOAW location in memory.

g. Jump — Causes an I/O program jump to occur if bit 4 of the order is set and bit 2 of the current IOCW is a "1" or if bit 4 of the current control word is not set (ie, set jump met).

h. Return Residue — Causes the residue of the count to be returned to the IOAW if bit 4 of the IOCW is a "0".

i. Set Bank — Loads the bank register for that device with the IOAW bits 14 and 15 when bit 4 of the IOCW is a "1".

4-17. CONTROL WORD. The control word is used to select the various operational states and test modes of the SCMB. A control word can be issued to the SCMB through a direct Control I/O instruction or through an I/O program Control order. If a Control order is used, the control word is located in the Control order IOAW location (the Control order IOCW is ignored by the SCMB). The control word is stored in the SCMB control register. Refer to figure 4-3 during the following description of the control word format.

4-18. Bit 0 — Master Reset. This bit, if a "1", issues a reset to the SCMB logic, clearing control logic, control register, and the counter/buffer. If the channel is active (ie, SIO ENABLE = 0), then a clear interface (ie, REQ) is issued to the channel. This feature can be used to stop a runaway channel or another device controller's I/O program execution.

4-19. Bit 1 — Reset Interrupt. This bit, if a "1", clears the SCMB Interrupt Request FF.

4-20. Bit 2 — Set Jump Met. This bit, if a "1", sets the SCMB Jump FF. Then if the selector channel executes a conditional Jump order, the SCMB returns the Jump Met signal to the channel, causing an I/O program jump to occur.

4-21. Bit 3 — Device End. This bit, if a "1", causes the SCMB to issue the Device End signal to the channel at the beginning of any data transfer. This results in no data being transferred between the channel and the SCMB.

4-22. Bit 4 — Inhibit Channel Acknowledge. This bit, if a "1", causes the SCMB to inhibit the Channel Acknowledge signal to the channel, following the current Control order. This results in an SO Timeout error in the channel (if the channel timers are enabled).

4-23. Bit 5 — Inhibit Service Request. This bit, if a "1", causes the SCMB to inhibit the Channel Service Request signal to the channel. This results in an SR timeout error in the channel if a subsequent Control, Read, or Write order is executed.

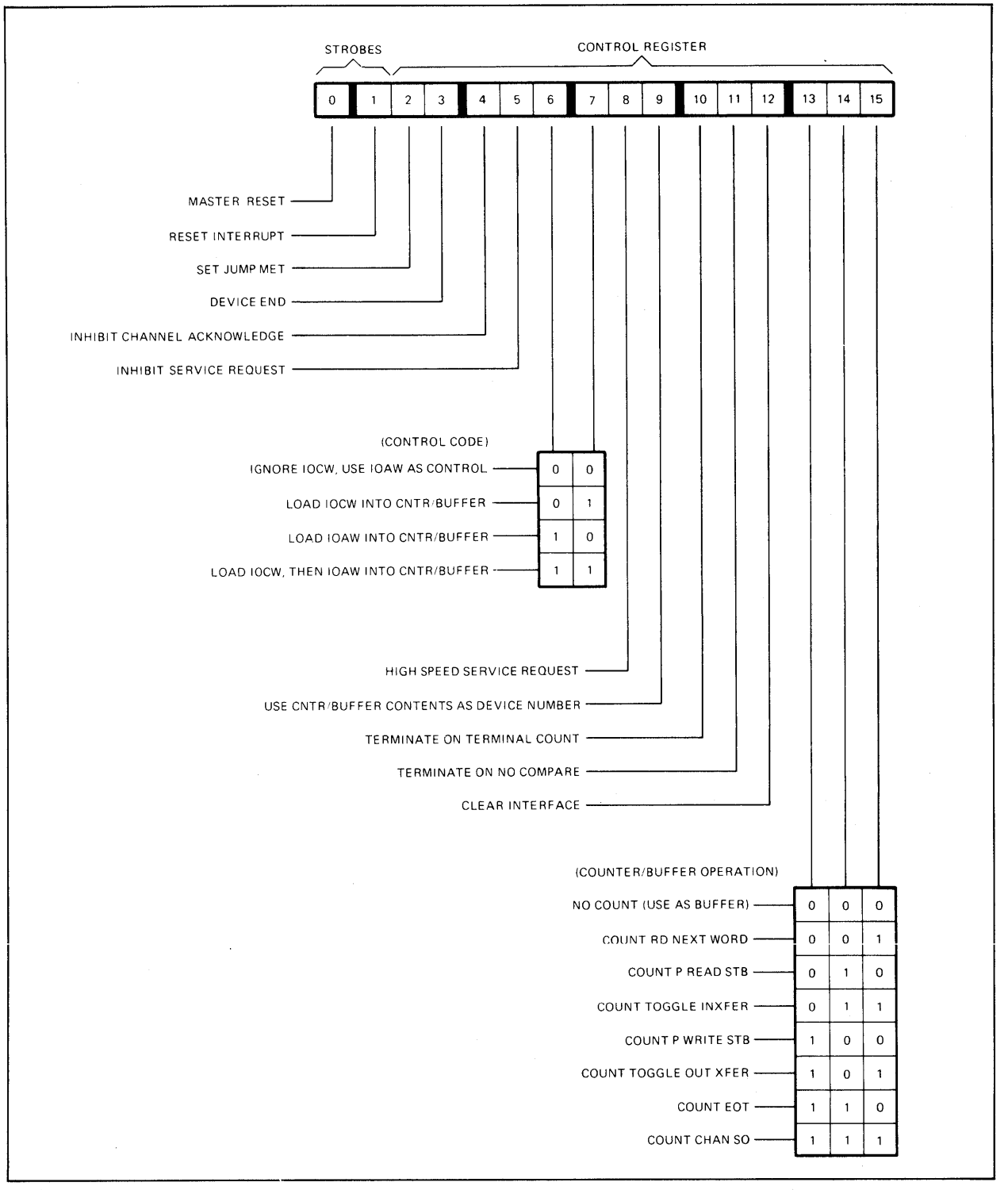


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Figure 4-3. SCMB Control Word Format

4-24. Bits 6 and 7 — Control Code. These bits define how the two control words sent during channel execution of a Control order are used. The normal mode loads the Control order IOAW into the control register to be used as a control word. The other modes load either or both the IOCW and IOAW into the counter/buffer leaving the control register contents unchanged.

4-25. Bit 8 — High Speed Service Request. This bit, if a "1", overrides the SCMB service request delay (normally 200kHz) to force continuous CHAN SR signals (when required) to the channel. The resulting transfer rate will be approximately 950 kHz outbound and 1140 kHz inbound.

4-26. Bit 9 — Device Number. This bit, if a "1", supplies the contents of the counter/buffer as the device number at I/O program initiatioin instead of the hardwired device number. By preloading the counter/buffer using a direct WIO instruction, an I/O program can be executed to any device number.

4-27. Bit 10 — Terminate on Terminal Count. This bit, if a "1", causes a Device End or clear interface (ie, REQ) to be issued to the channel if the counter/buffer contents "rollover" (ie, past count capacity). Whether device end or clear interface is issued is determined by the state of bit 12.

4-28. Bit 11 — Terminate on NO Compare. This bit, if a "1", causes the contents of the counter/buffer to be compared to data words issued to the maintenance PCA during channel execution of a Write order. (Normally, data received during execution of a Write order is loaded into the counter/buffer. If bit 11 is a "1", the counter/buffer contents remain unchanged.) If a compare failure occurs, the SCMB issues either a Device End signal or a clear interface (ie, REQ) to the channel. Whether device end or clear interface is issued is determined by the state of bit 12.

4-29. Bit 12 — Clear Interface. This bit, if a "1", causes a clear interface (ie, REQ) to be issued to the channel if either conditions controlled by bits 10 or 11 occur. If a "1", a Device End signal is issued if the bit 10 or 11 condition occurs.

4-30. Bit 13 - 15 — Counter/Buffer Operation. These bits control the operation of the counter/buffer. When used as a buffer, the counter/buffer is loaded with data words received during channel execution of a Write order (unless bit 11 is a "1"). The buffer contents are sent to the channel as data during channel execution of a Read order.

NOTE

Upon receipt of an I/O Reset signal, the SCMB counter/buffer and control word storage registers are cleared Therefore, the initial operating state of the SCMB is as follows:

1) the counter/buffer contents = "0"

2) if a Control order is executed, the Control order IOAW will be used as a Control word

3) the SCMB wired device number will be sent if an SIO instruction is executed to the SCMB

4) the counter/buffer will be used as a buffer.

4-31. STATUS WORD. The status word results from various signals and flip-flops on the SCMB. The conditions reported by the status word are reset each time I/O program execution is initiated by an SIO instruction. Transfer related functions (eg, no compare) are reset at the beginning of data transfers. Refer to figure 4-4 during the following description of the status word format.

4-32. Bit 0 — SIO OK. This bit is a "1" if the SCMB is not currently executing an I/O program and the channel is inactive.

4-33. Bit 1 — RIO/WIO OK. Always a "1".

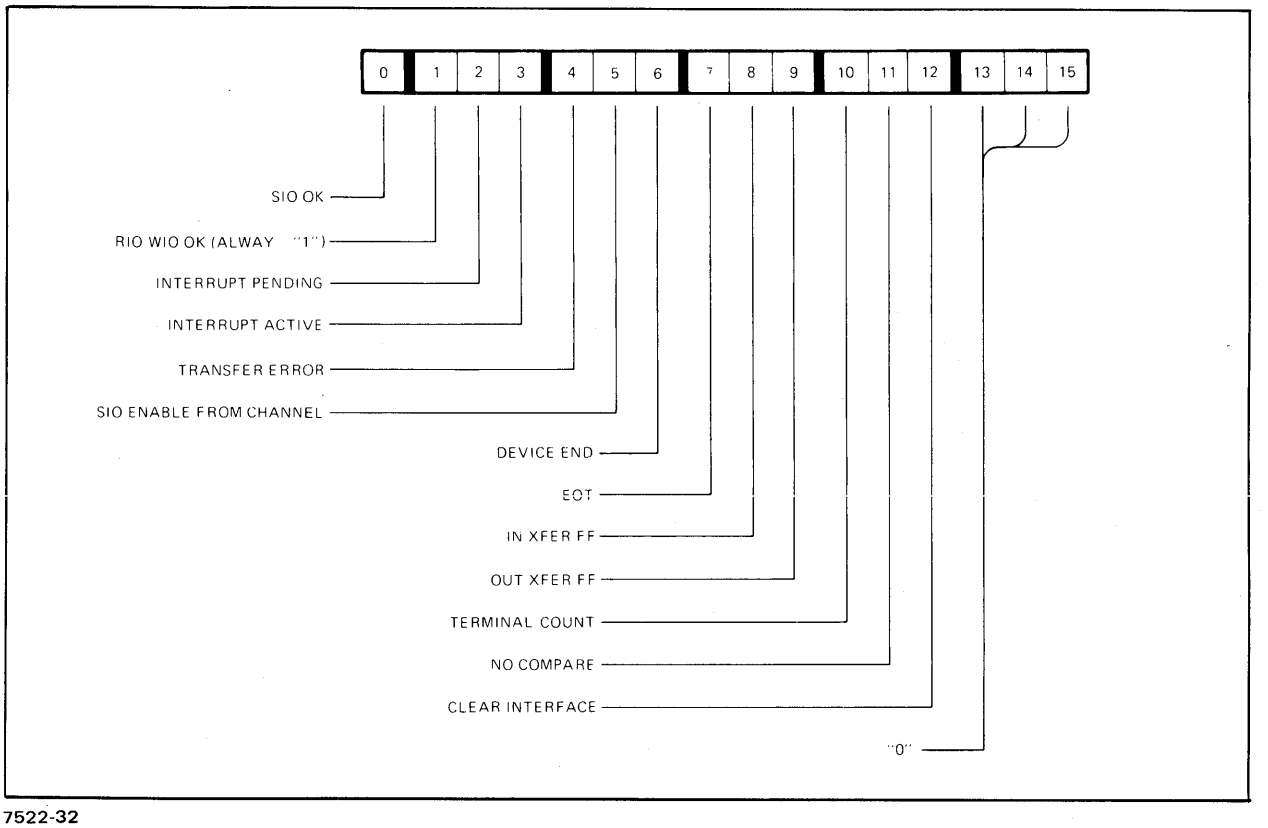
4-34. Bit 2 — Interrupt Pending. This bit is a "1" if the SCMB is attempting to interrupt the CPU.

4-35. Bit 3 — Interrupt Active. This bit is a "1" if the SCMB interrupt circuitry is currently in the active state.

4-36. Bit 4 — Transfer Error. This bit is a "1" if the channel has sent the XFER ERR (transfer error) signal. Bit 4 is cleared by the next SIO instruction or I/O Reset.

4-37. Bit 5 — SIO Enable. This bit is a "1" if the channel is asserting the SIO ENABLE signal (ie, channel inactive).

4-38. Bit 6 — Device End. This bit is a "1" if the SCMB has asserted the device end signal to the channel. Bit 6 is cleared at the beginning of a new data transfer, by the next SIO instruction, or by an I/O Reset.



7522-32

Figure 4-4. SCMB Status Word Format

4-39. Bit 7 — EOT. This bit is a "1" if the channel has asserted the EOT (ie, end of transfer) signal to the SCMB. Bit 7 is cleared at the beginning of a new data transfer, by the next SIO instruction, or by an I/O Reset.

4-40. Bit 8 — IN XFER FF. This bit if a "1", indicates that the most current data transfer operation was a Read order.

4-41. Bit 9 — OUT XFER FF. This bit if a "1", indicates that the most current data transfer operation was a Write order.

4-42. Bit 10 — Terminal Count. This bit, if a "1", indicates that a condition counted by the counter/buffer caused a rollover (refer to paragraph 4-22). Bit 10 is cleared at the beginning of a new data transfer, by the next SIO instruction to the SCMB, and by an I/O Reset.

4-43. Bit 11 — No Compare. This bit is enabled if control word bit 10 is a "1". If a "1", this bit indicates that a data word received from the channel during Write order execution did not match the word contained in the counter/buffer. Bit 11 is cleared at the beginning of a data transfer by the next SIO instruction to the SCMB, or by an I/O Reset.

4-44. Bit 12 — Clear Interface. This bit is a "1" if the SCMB has asserted the clear interface (ie, REQ) signal to the channel. Bit 12 is cleared at the beginning of the next SIO instruction or by an I/O Reset.

4-45. PROGRAM EXECUTION

See figure 4-5. A simple way to initiate I/O program execution with the SCMB is to use the CPU cold load feature.

Because the SCMB counter/buffer is cleared by an I/O Reset, cold loading from the SCMB causes an unconditional jump to memory location %000000. A service engineer designed I/O program, starting at location %000000, is then executed.

To use this method of I/O program initiation, perform the following steps:

a. Using the maintenance panel, enter the desired I/O program starting at memory location %000000.

b. Refer to paragraph 4-12 and enter any desired control option (bits 0:7) into the left byte of the SYSTEM SWITCH REGISTER.

c. Enter the SCMB device number into the right 6 bits of the SYSTEM SWITCH REGISTER, bit 8 must be set and bit 9 cleared (A cold load cannot occur from a device number greater than %77.)

NOTE

If bit 9 is set to a "1", this indicates a cold load will occur from a direct I/O device (HP 2644A).

d. If the selectable freeze capability is to be used, the condition should be selected and the two-position switch on the channel control PCA should be set to the FRZ position at this time. (Refer to paragraph 4-65.)

e. Press the LOAD switch (this causes the I/O program at location %000000 to begin execution).

f. If the selectable freeze capability is being used, the CLOCK INHIBIT/FREE RUN switch on the maintenance panel should be set to the INHIBIT position and the two-position switch on the control PCA should be set opposite the FRZ position. The selector channel and SCMB can now be single-cycled through the I/O program.

g. With the CPU in the halt state, the I/O program can be altered (while running) and the panel indicators can be observed.

h. To stop the I/O program execution, press RESET I/O.

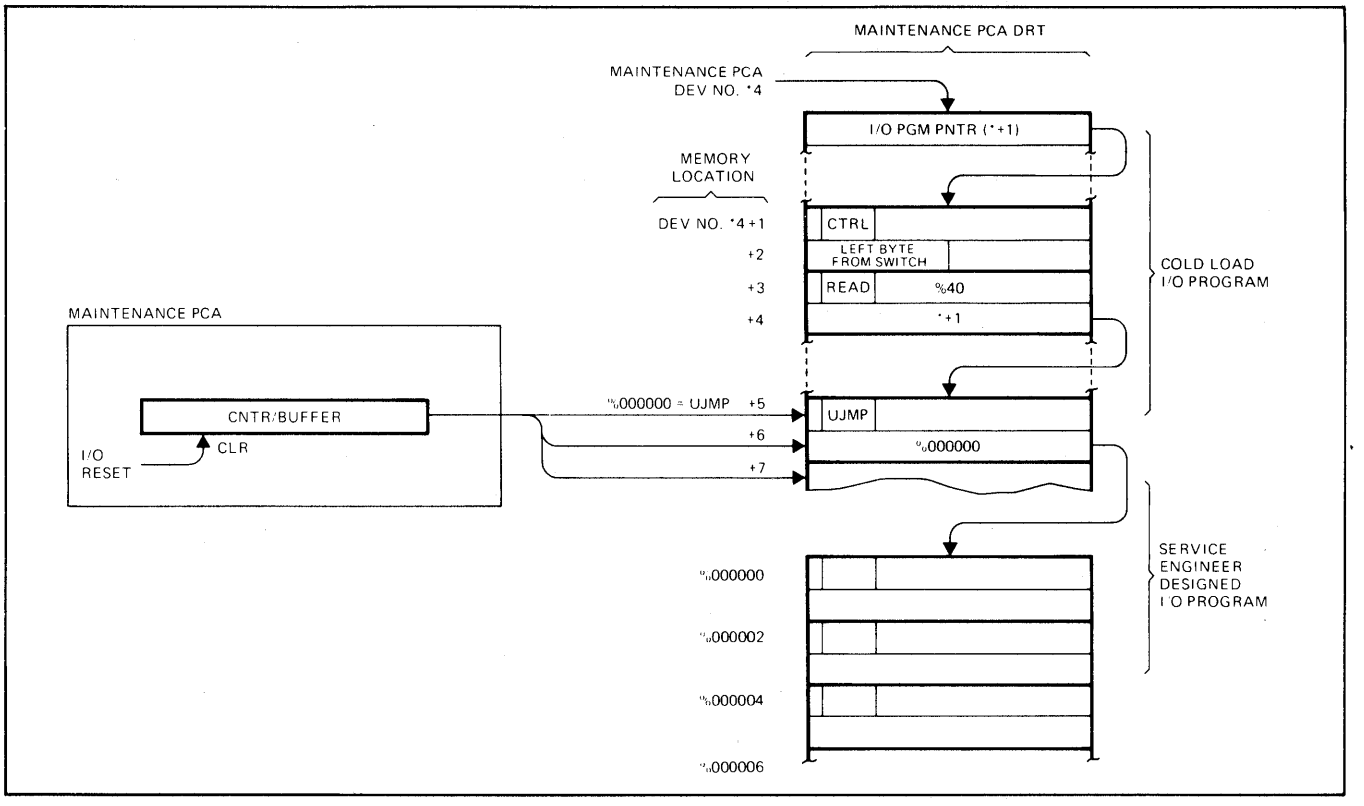


Figure 4-5. Cold Load Method of I/O Program Initiation

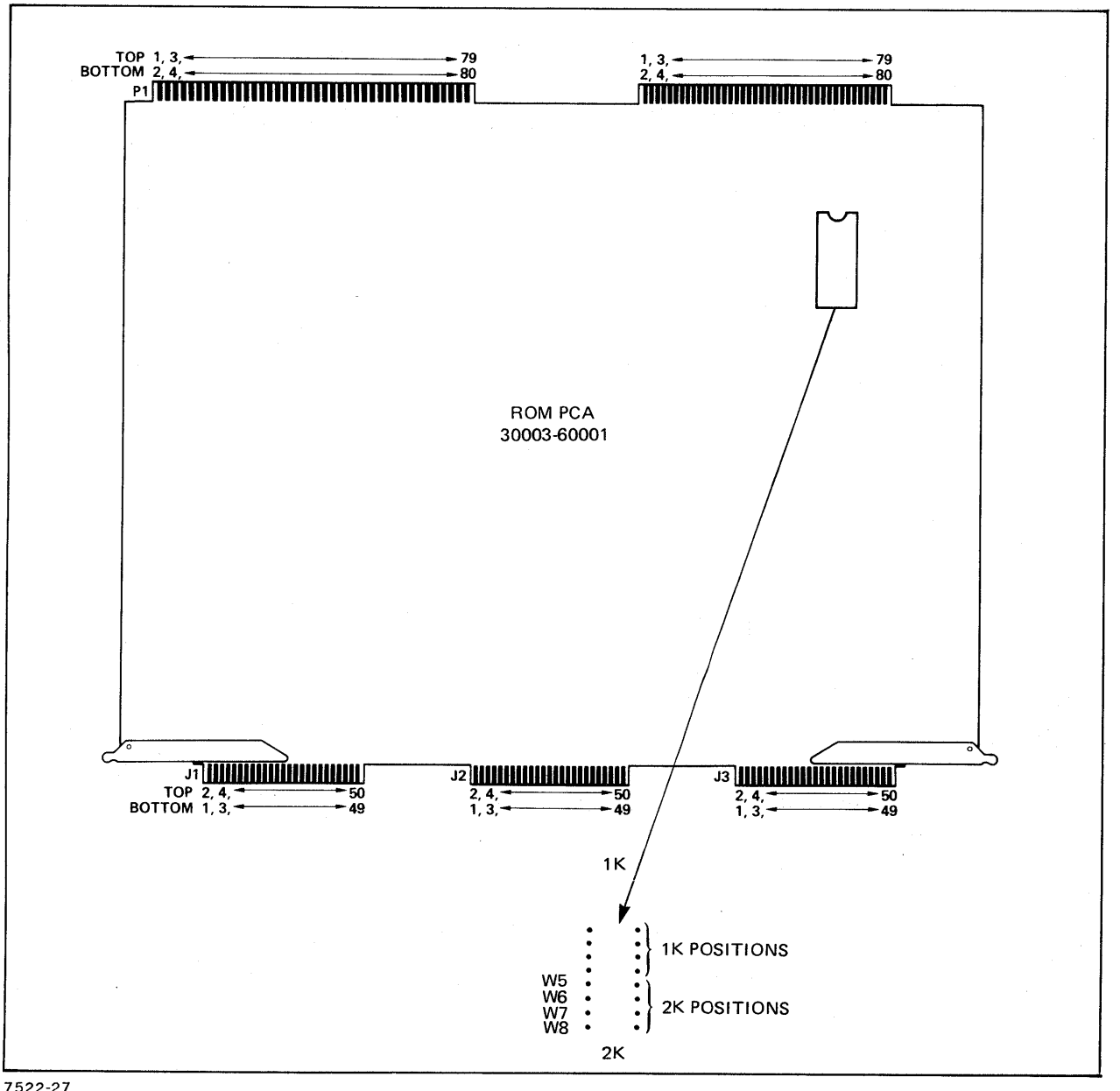
4-46. PCA JUMPERS AND SWITCHES

The following paragraphs and the asociated illustrations locate and explain the use of the switches and jumpers located on the system processor PCA's.

The actual switch position and jumpers inserted on a PCA can be determined by referring to the Configuration Guide of the System Support Log.

4-47. ROM PCA 30003-60001

4-48. ROM LOADING. Jumpers W5 through W8 (figure 4-6) are inserted in the four positions nearest the 1K marking when the PCA is loaded with ROM's having a capacity of 1K words. The four positions nearest the 2K marking have the jumpers inserted when the PCA is loaded with ROM's having a capacity of 2K words.



7522-27

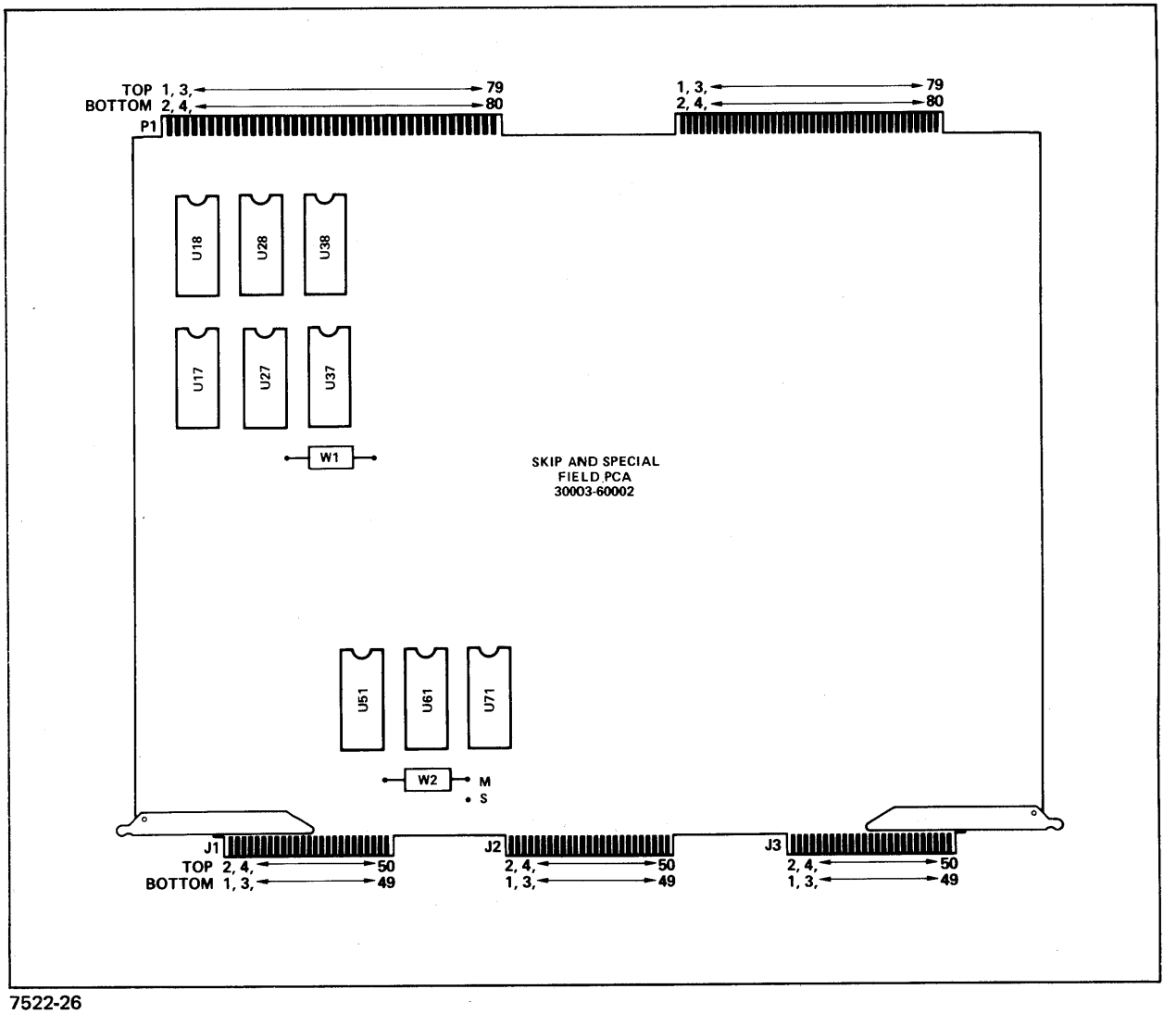
Figure 4-6. ROM PCA Jumper Locations

4-49. SKIP AND SPECIAL FIELD PCA 30003-60002

4-50. SYNC JUMPERS. When two CPU's are used in a system, CPU number 2 (slave) must be in sync with the master CPU. Jumpers W1 and W2 are used to configure each CPU accordingly. See figure 4-7.

With one CPU in a system, W1 is inserted and W2 in in position M.

W1 is inserted if it is the master CPU (CPU number 1) and W2 is placed in position M. The second CPU will have W1 removed and W2 in position S, putting CPU number 2 in sync with CPU number 1.



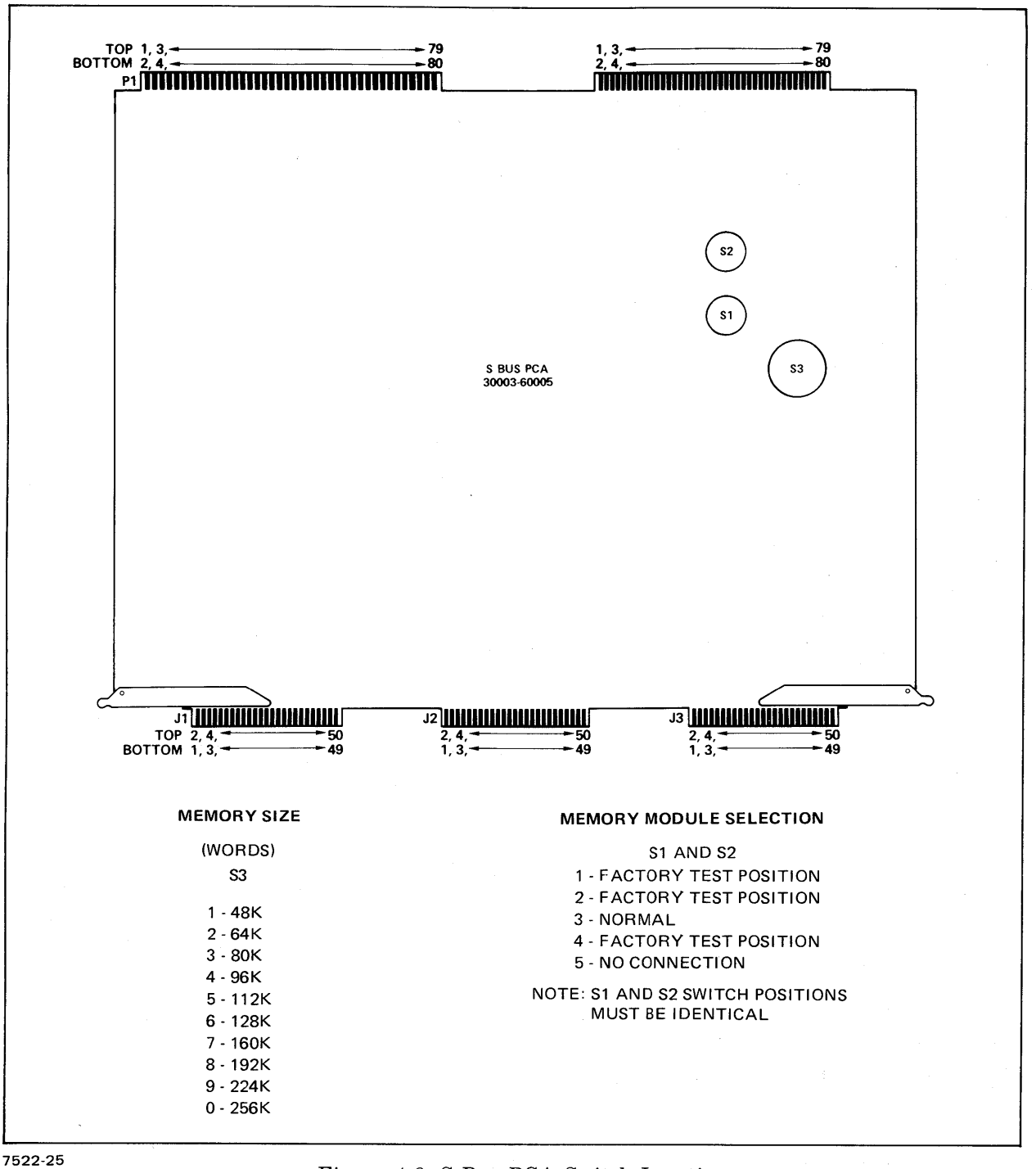
7522-26

Figure 4-7. Skip and Special Field PCA Jumper Locations

4-51. S BUS PCA 30003-60005

4-52. MEMORY SIZE. Selection of the memory size is accomplished by setting a ten position switch on the S Bus PCA. position switch on the S Bus PCA. See figure 4-8.

4-53. MEMORY MODULE SELECTION. Two five-position switches S1 and S2, are used to select the memory module. See figure 4-8. S1 and S2 switch positions must always be identical, and set to the NORMAL position. The remaining switch positions are used for factory test purposes. Inadvertantly using a position other than NORMAL could cause the wrong memory module to be selected.



7522-25

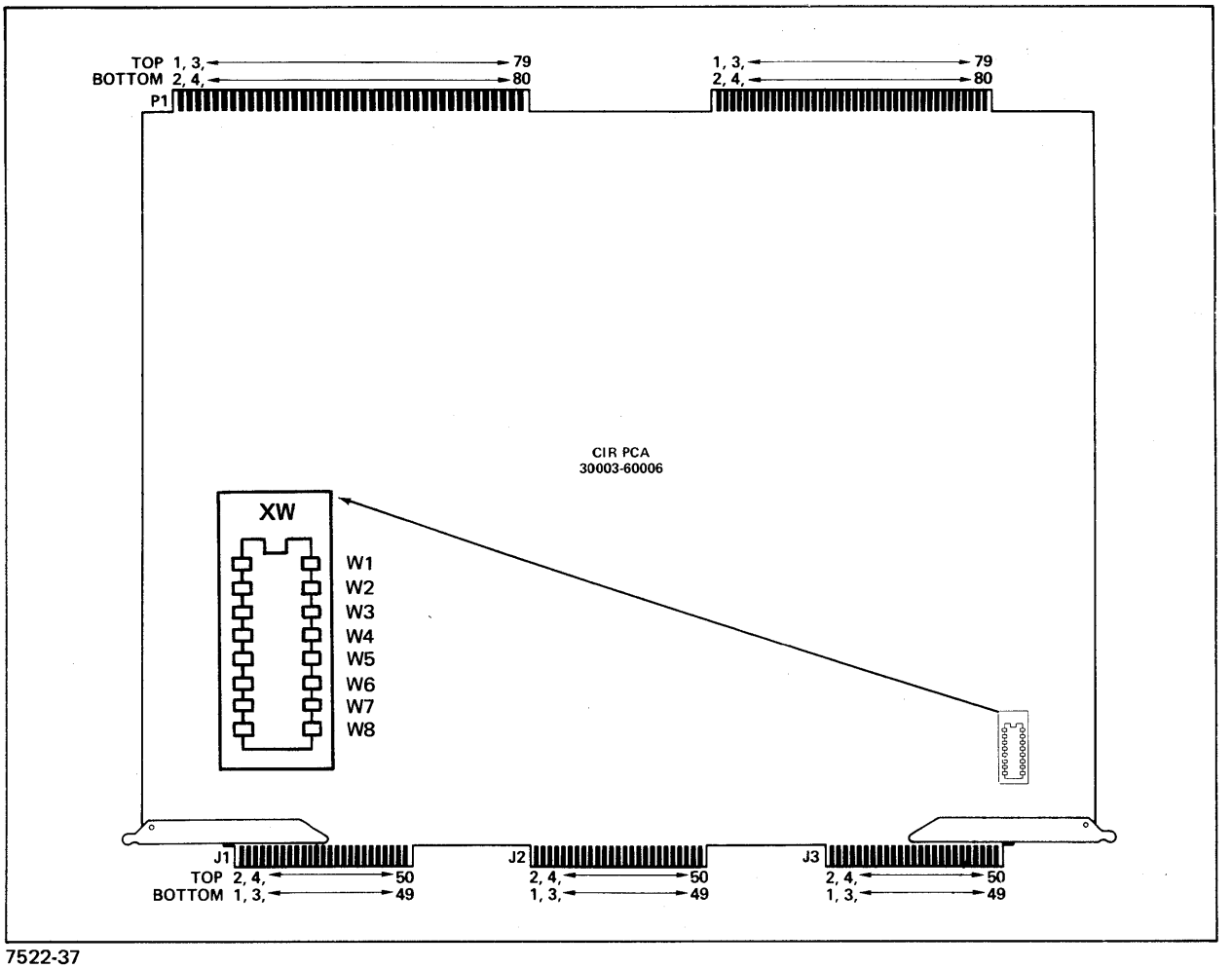
Figure 4-8. S Bus PCA Switch Locations

4-54. CURRENT INSTRUCTION REGISTER (CIR) PCA 30003-60006, EXTENDED INSTRUCTION SET (EIS) PCA 30012-60001

4-55. JUMPERS. Jumpers W1 through W8 on the CIR PCA are used to configure the CIR when the EIS PCA is installed in the system.

When the EIS PCA is installed in the system, jumpers W1 and W8 are removed from CIR PCA. Removing W1 enables the floating point instructions, and removing W8 enables the decimal instruction set.

When APL (A Programming Language), product number HP 32105A, is installed in the system, jumper W2 on the CIR PCA must be removed to enable the APL instructions.



7522-37

Figure 4-9. CIR PCA Jumper Locations

Jumpers W1 through W8 are all installed on the CIR PCA when the EIS PCA is not present in the system.

The EIS PCA has jumpers W1 through W8 installed in socket XW2 when the PCA is loaded with 2K ROM's. Socket XW1 would then have no jumpers installed.

If the EIS PCA is loaded with 1K ROM's, jumpers W1 through W8 are installed in socket XW1 and socket XW2 has no jumpers installed.

4-56. MCU PCA 30003-60007

4-57. ENABLE. The ENABLE signal is used to establish priority for accessing the CTL bus. The insertion of jumpers W1 through W4 establish the priority of the MCU PCA.

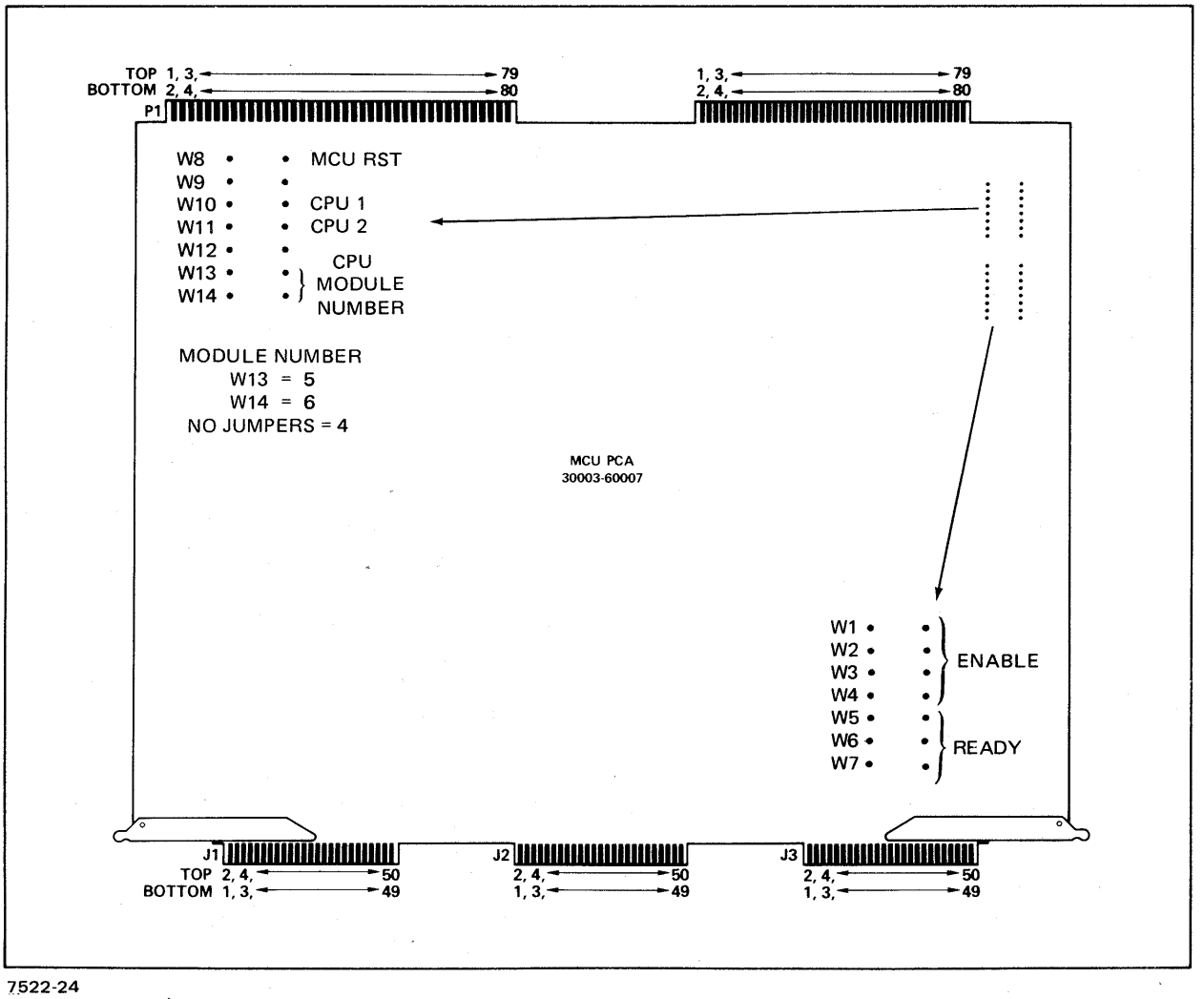
4-58. READY. The READY signal is used to signify that a module is ready to communicate with memory. The insertion of jumpers W5 (READY 4) through W7 (READY 6) determine which READY line is assigned to the MCU PCA.

4-59. CPU NUMBER. The system has the future capability of having two CPU's installed. When two CPU's are installed, each is assigned a number determined by inserting jumpers W10 or W11. In a one CPU configuration, the CPU is designated as number 1.

4-60. CPU MODULE NUMBER. The CPU connected to the CTL bus is assigned a module number between 4 and 6 by insertion of jumpers W13 and W14. The module number 5 normally will be assigned to the CPU.

4-61. MCU RESET. In a single CPU configuration, jumper W8 is removed, see figure 4-10.

In a dual CPU configuration, the capability of having one CPU reset the other CPU is obtained by inserting jumper W8.



7522-24

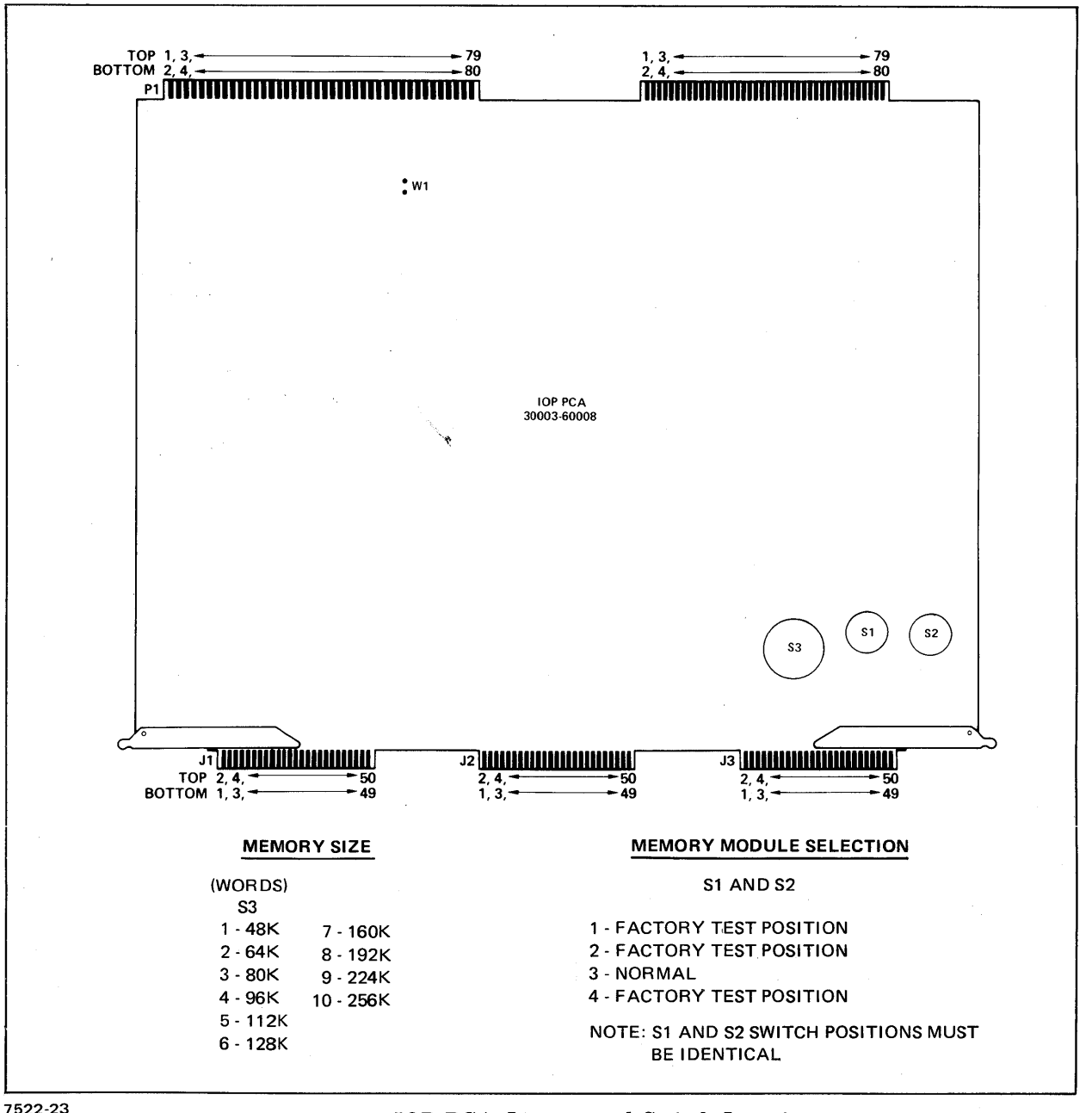
Figure 4-10. MCU PCA Jumper Locations

4-62. IOP PCA 30003-60008

4-63. ENABLE/DISABLE. Jumper W1 is not installed, enabling the IOP PCA. Installation of this jumper disables the IOP PCA.

4-64. MEMORY SIZE. Selection of the memory word size is accomplished by setting a ten position switch, S3, on the IOP PCA. See figure 4-11.

4-65. MEMORY MODULE SELECTION. Two four-position switches, S1 and S2, are used to select the memory module. S1 and S2 switch positions must always be identical, and set to the NORMAL position. The remaining switch positions are used only for factory test purposes. Inadvertently using a position other than NORMAL could cause the wrong memory module to be selected.



7522-23

Figure 4-11. IOP PCA Jumper and Switch Locations

4-66. SEMICONDUCTOR MEMORY ARRAY (SMA) PCA 30008-60002

4-67. MEMORY MODULE CONFIGURATION. To configure the memory module according to its designated board number in the module, insert jumpers in socket XW1 (figure 4-12) according to table 4-2 noting the revision level of the PCA.

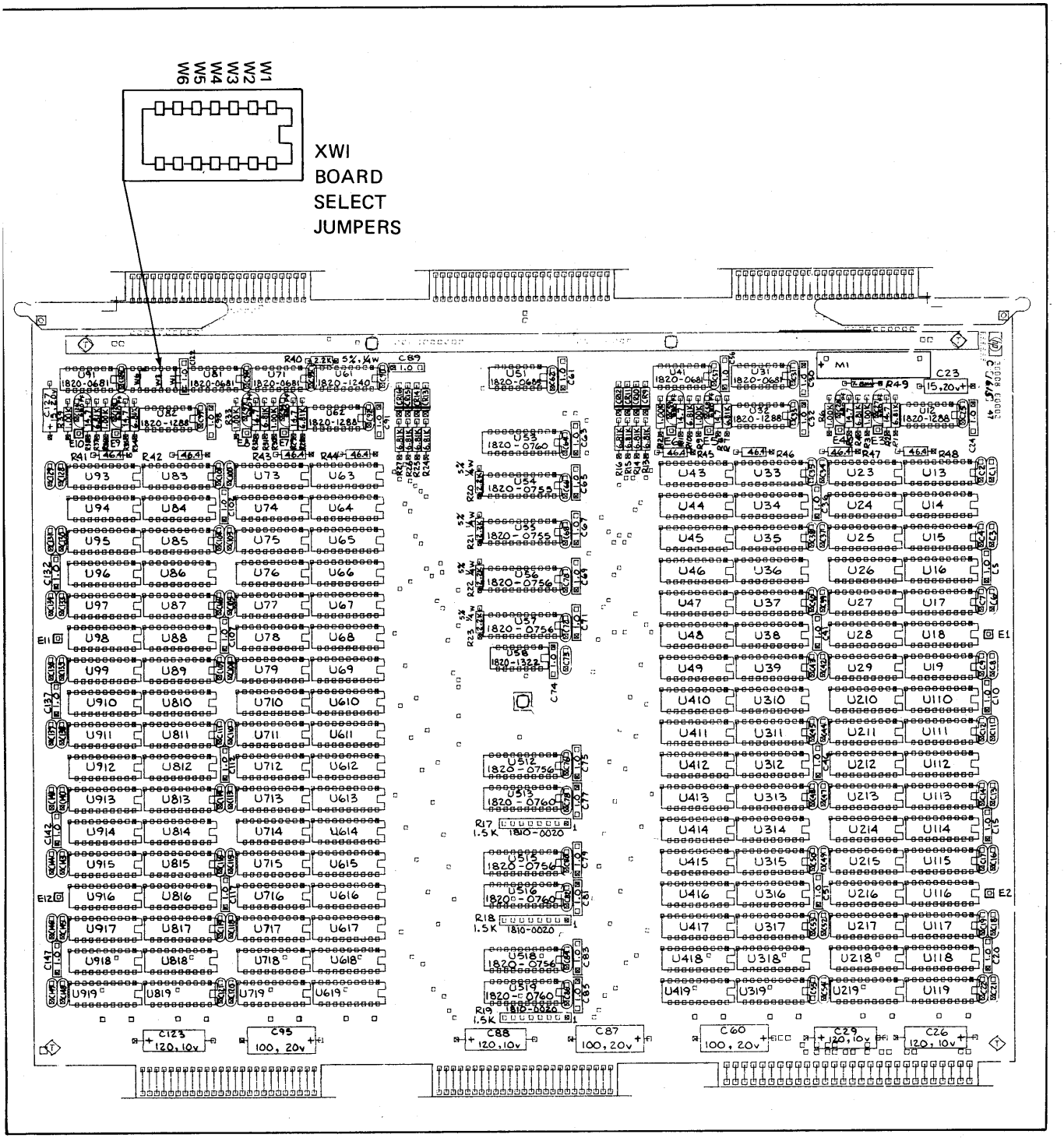


Figure 4-12. SMA PCA Jumper Locations

Table 4-2. SMA PCA Board Select Jumpers

Rev A	Jumpers Inserted					
Board Select	**W1**	**W2**	**W3**	**W4**	**W5**	**W6**
1st 32K	X			X	X	
2nd 32K	X		X		X	
3rd 32K		X		X	X	
4th 32K		X	X		X	
Rev B and Later	**W1**	**W2**	**W3**	**W4**	**W5**	**W6**
1st 32K		X	X		X	
2nd 32K	X		X		X	
3rd 32K		X		X	X	
4th 32K	X			X	X	

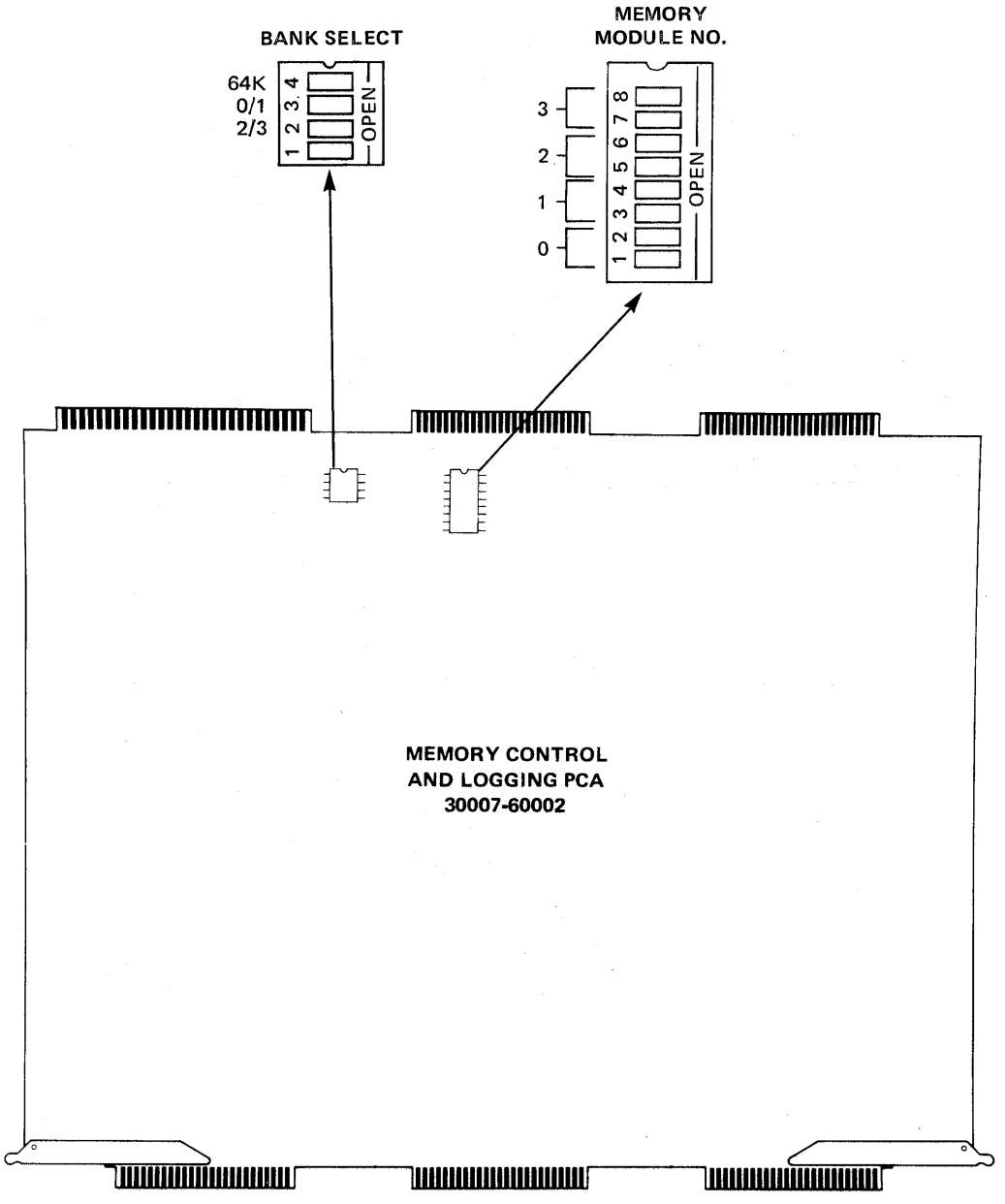
4-68. MEMORY CONTROL AND LOGGING (MCL) PCA 30007-60002

4-69. MEMORY MODULE CONFIGURATION. To configure the MCL PCA to the memory module size, position the individual switches on each switch assembly as shown in table 4-3. Refer to figure 4-13 for the location and designations of switches.

Table 4-3. MCL PCA Switch Positions

Module Size	Bank Number	0	1	2	3	0/1	2/3	64K
64K	0	C	O	O	O	O	O	C
64K	1	O	C	O	O	O	O	C
64K	2	O	O	C	O	O	O	C
64K	3	O	O	O	C	O	O	C
0K to 128K	0 & 1	C	C	O	O	C	O	O
128K to 256K	2 & 3	O	O	C	C	O	C	O

O= OPEN
C= CLOSED



7522-39

Figure 4-13. MCL PCA Switch Locations

4-70. FAULT LOGGING INTERFACE (FLI) PCA 30009-60002

4-71. DRT NUMBER. The FLI PCA is always configured with a DRT number of 2. Switches S1 and S3 through S7 are always closed. S2 is always open. See figure 4-14.

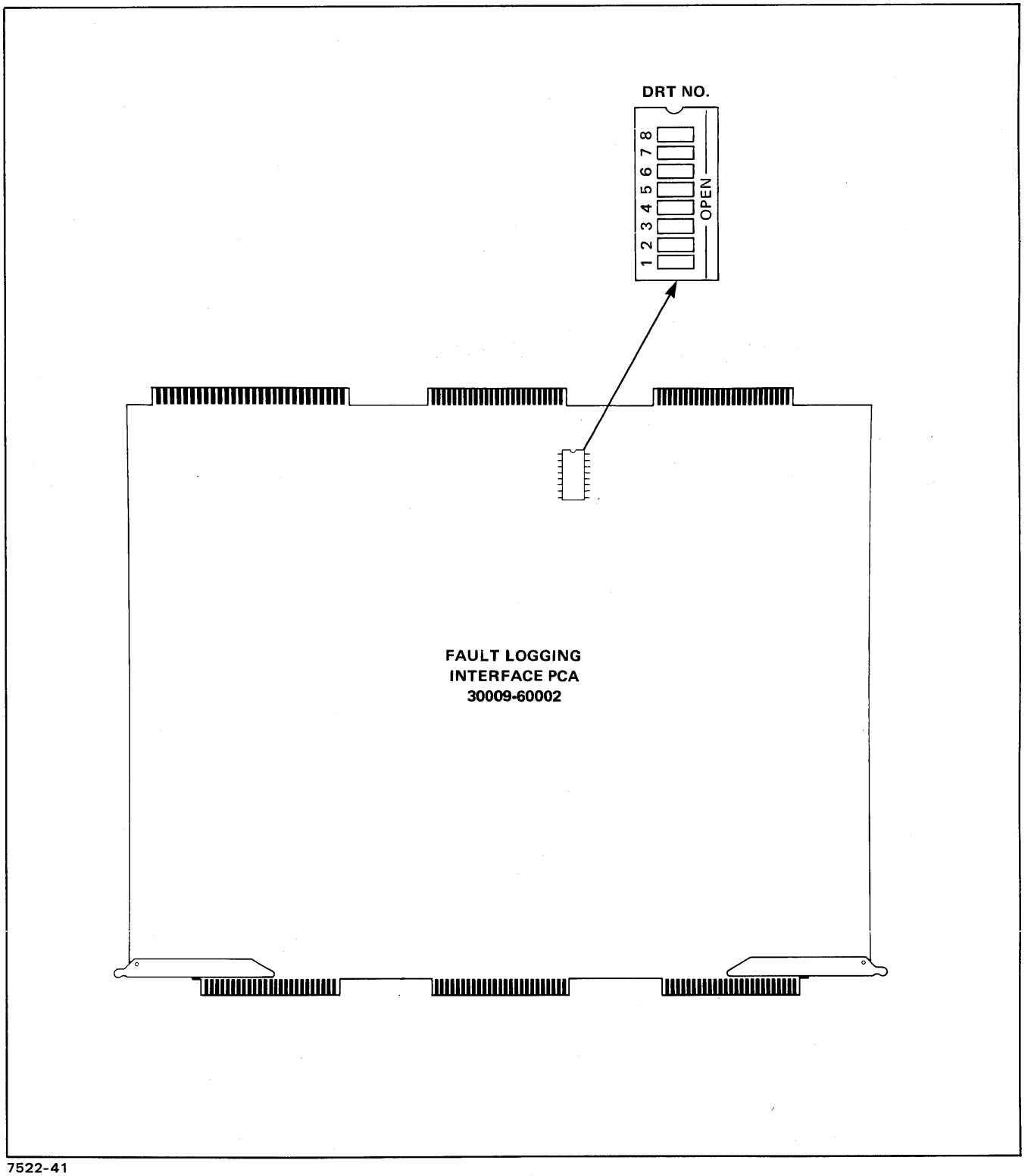


Figure 4-14. FLI PCA Switch Location

4-72. FAULT CORRECTION ARRAY (FCA) PCA 30009-60001

No switches or jumpers exist on this PCA. Figure 4-15 is presented as an aid to physically locate components on the PCA.

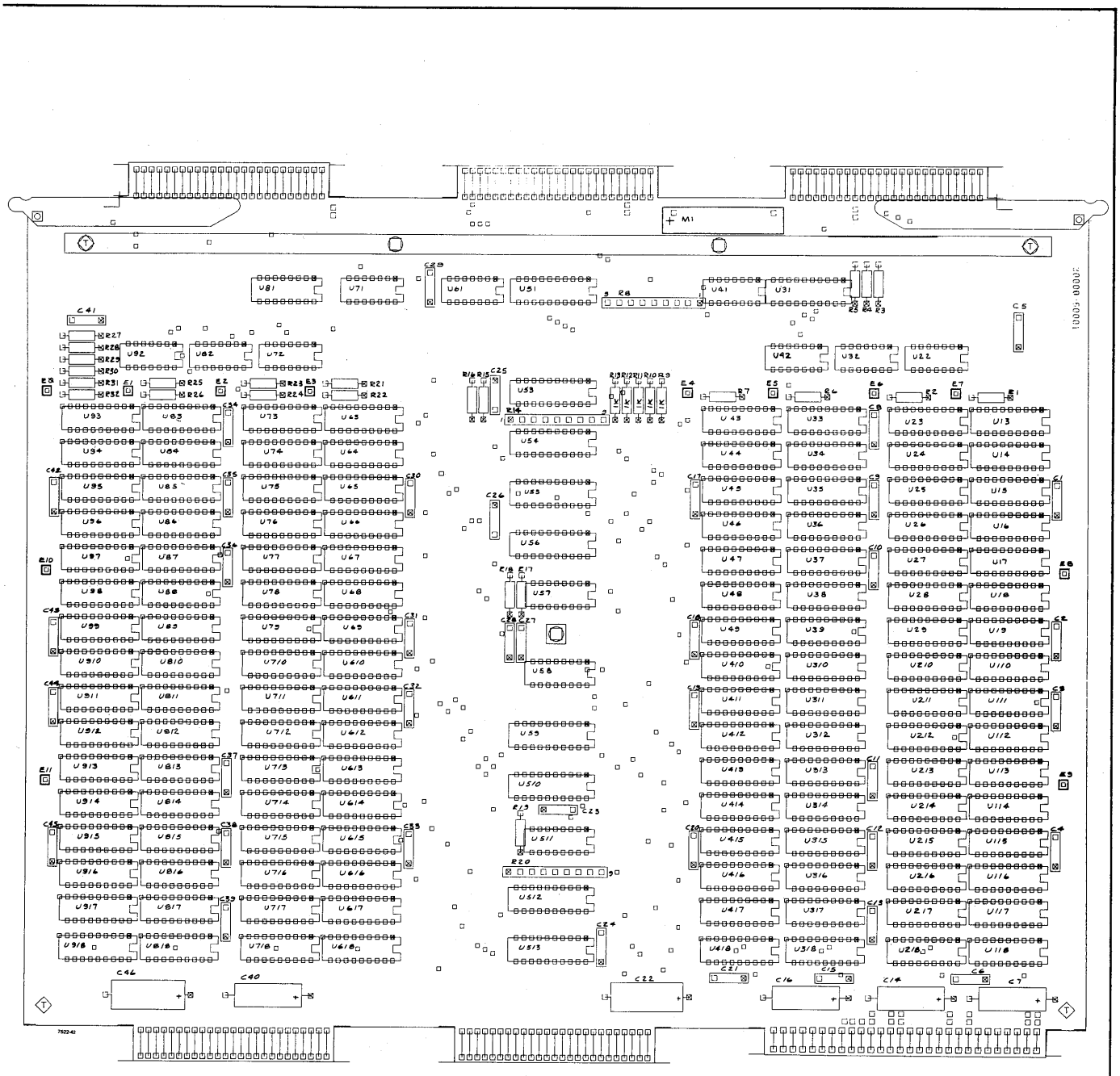
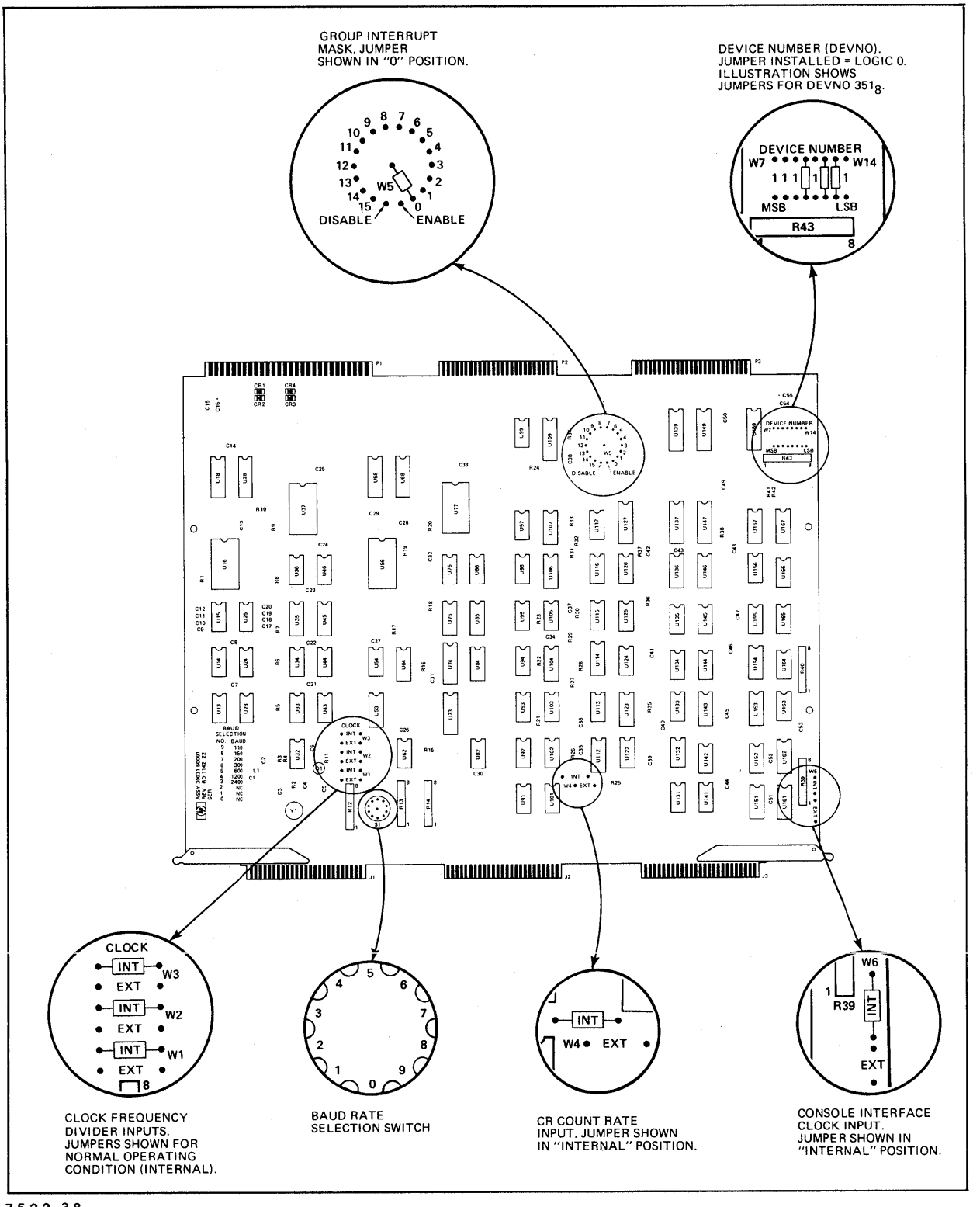


Figure 4-15. FCA PCA Component Location

4-73. SYSTEM CLOCK/CONSOLE INTERFACE PCA 30031-60001

The system clock/console interface PCA contains locations for 14 jumpers and one ten-position switch that select operating parameters for the PCA. Physical locations of the jumper wires and switch are shown in figure 4-16.



7522-38

Figure 4-16. System Clock/Console Interface PCA Jumper and Switch Locations

4-74. FREQUENCY DIVIDER INPUT SELECTION W1, W2, AND W3. These three jumpers connect all or part of the clock frequency divider input to either the 10 MHz internal clock or to an external input. The normal operating configuration for the PCA is with these three jumpers installed in the INT position.

4-75. CR COUNT RATE INPUT W4. Jumper W4 determines the source of the PCA count register (CR) clock input. The INT (normal operation) position of W4 connects the CR clock input to the PCA circuits that are controlled by bits 0, 1, and 2 of the control word. The EXT position of W4 connects the CR clock input to an external source (J2-30).

4-76. GROUP INTERRUPT MASK W5. Jumper W5 selects the interrupt mask group for the PCA. In addition to one of the 16 interrupt mask groups, the jumper can be connected to permanently enable or disable interrupts from the PCA.

4-77. SERIAL INTERFACE CLOCK INPUT W6. Jumper W6 selects the source of the clock signal that determines the baud rate for the console interface logic. With W6 in the INT position, the clock signal is obtained from the baud rate selection logic on the PCA. With W6 in the EXT position, the clock signal is obtained externally (J2-28) and is 16 times greater than the baud rate.

4-78. DEVICE NUMBER W7 THRU W14. The configuration of these eight jumpers determines the DRT number (usually 3) of the PCA. A jumper installed corresponds to a logic 0, and the absence of a jumper corresponds to a logic 1 in the device number.

4-79. BAUD RATE SELECTION S1. The PCA can transmit and receive serial data at seven baud rates from 110 to 2400 baud. The rate selected for the PCA must correspond to the baud rate of the external I/O device. The switch position and corresponding baud rates are shown in table 4-4.

Table 4-4. S1 Baud Rate Selection

S1 POSITION	BAUD RATE
1	110
2	150
3	220
4	300
5	600
6	1200
7	2400
8	NC
9	NC
0	NC

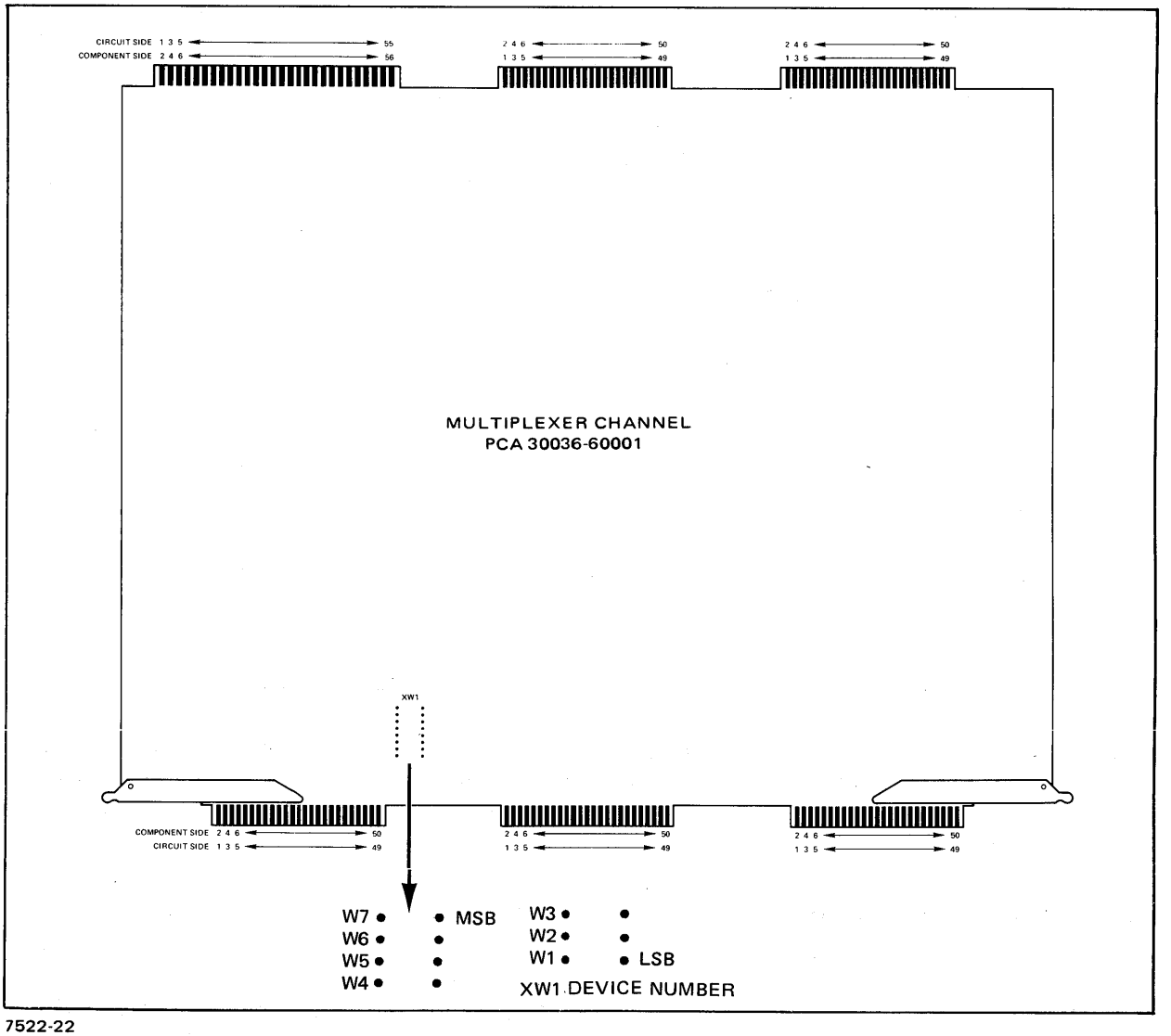
Baud rate can also be selected by conecting jumpers externally to connector J1. Switch S1 must be in position 0 (no connection) when an external jumper is installed. Only one jumper may be installed at a time. Table 4-5 shows the jumper connection required for the selected baud rate.

4-80. MULTIPLEXER CHANNEL PCA 30036-60001

4-81. DEVICE NUMBER. The configuration of jumpers W1 through W7 determine the device number and therefore the DRT address associated with the multiplexer channel PCA. A logic "1" is represented by the absence of a jumper wire and conversely, a logic "0" is represented by the presence of a jumper wire. See figure 4-17.

Table 4-5. External Baud Rate Selection

SYSTEM CLOCK/CONSOLE INTERFACE PCA J1	JUMPER CONNECTED BETWEEN PINS ON P1	BAUD RATE SELECTED
35	18A	2400
36	18B	
37	19A	1200
38	19B	
39	20A	600
40	20B	
41	21A	300
42	21B	
43	22A	220
44	22B	
45	23A	150
46	23B	
47	24A	110
48	24B	

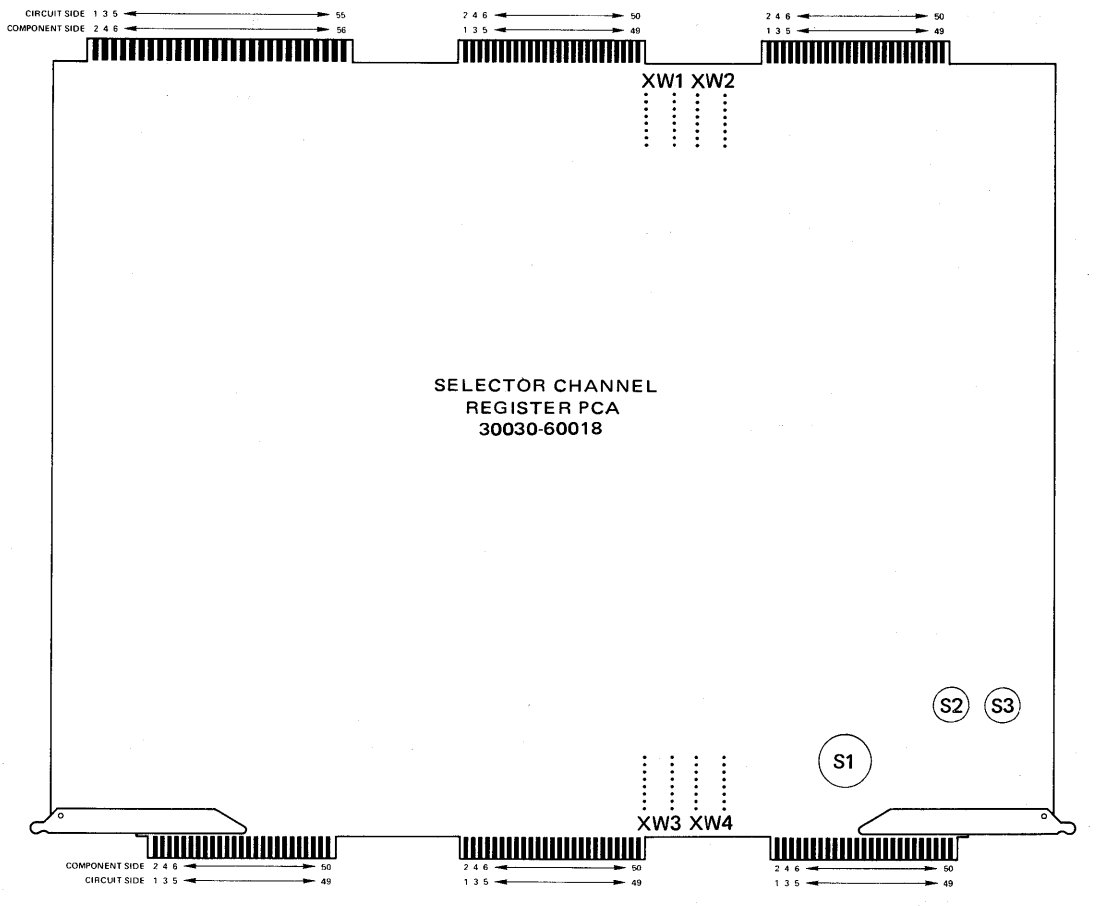


7522-22

Figure 4-17. Multiplexer Channel PCA Jumper Locations

4-82. SELECTOR CHANNEL REGISTER PCA 30030-60018

4-83. CHANNEL NUMBER. The port controller contains four ports so that up to four channels can be multiplexed to the central data bus through a single module number. A jumper plug and four dual inline sockets are used to designate to which channel the selector channel register PCA is connected. The channel number can be changed by moving the jumper plug from one socket to another. See figure 4-18.



CHANNEL NUMBER

XW1 = CHANNEL 1
XW2 = CHANNEL 2
XW3 = CHANNEL 3
XW4 = CHANNEL 4

MEMORY SIZE

(WORDS)
S1

1 - 48K
2 - 64K
3 - 80K
4 - 96K
5 - 112K
6 - 128K
7 - 160K
8 - 192K
9 - 224K
0 - 256K

MEMORY MODULE SELECTION

S2 AND S3

1 - FACTORY TEST POSITION
2 - FACTORY TEST POSITION
3 - NORMAL
4 - FACTORY TEST POSITION
5 - FACTORY TEST POSITION

NOTE: S2 AND S3 SWITCH POSITIONS MUST BE IDENTICAL.

7522-21

Figure 4-18. Selector Channel Register PCA Jumper and Switch Locations

4-84. MEMORY SIZE. Selection of the memory word size is accomplished by setting a ten position switch S1 on the register PCA. See figure 4-18.

4-85. MEMORY MODULE SELECTION. Two five-position switches, S2 and S3 are used to select the memory module. See figure 4-18. S2 and S3 switch positions must always be identical, and set to the NORMAL position. The remaining switch positions are used only for factory test purposes. Inadvertently using a position other than NORMAL could cause the wrong memory module to be selected.

4-86. SELECTOR CHANNEL CONTROL PCA 30030-60003

4-87. SELECTABLE TRIGGER/FREEZE. A ten-position rotary switch S1, and a stand-off terminal E2 (TRIG) on the control PCA provide the capability of triggering an oscilloscope each time a pre-selected condition occurs. The switch can select one of eight orders or an error condition. In the case of an order, the trigger occurs when the order begins executing. A typical use of the selectable trigger is to loop on an I/O program by means of a Jump order while triggering on an order of interest. See figure 4-19 for switch settings and terminal location.

NOTE

The trigger/freeze feature can only be used when the HP 30354A Maintenance Panel is connected to the system.

To use the trigger/freeze feature, do the following:

a. Set the ten-position rotary switch (figure 4-19) to the position corresponding to the desired condition.

b. Set the two-position switch S2 (figure 4-19) to the FRZ position.

c. Initiate program execution.

d. The selector channel operation "freezes" when the selected condition is decoded by the control PCA.

e. Set the maintenance panel for single-cycle operation.

f. Set S2 on the control panel PCA opposite the FRZ position.

g. Single-cycle the system through the execution sequence for the desired order while various indicators are observed.

4-88. ERROR LOGGING REGISTER. The error logging register (figure 4-19) provides a means for determining the type of error that prematurely terminates the the execution of an I/O program. When an error occurs, the error type sets a corresponding bit in the error logging register.

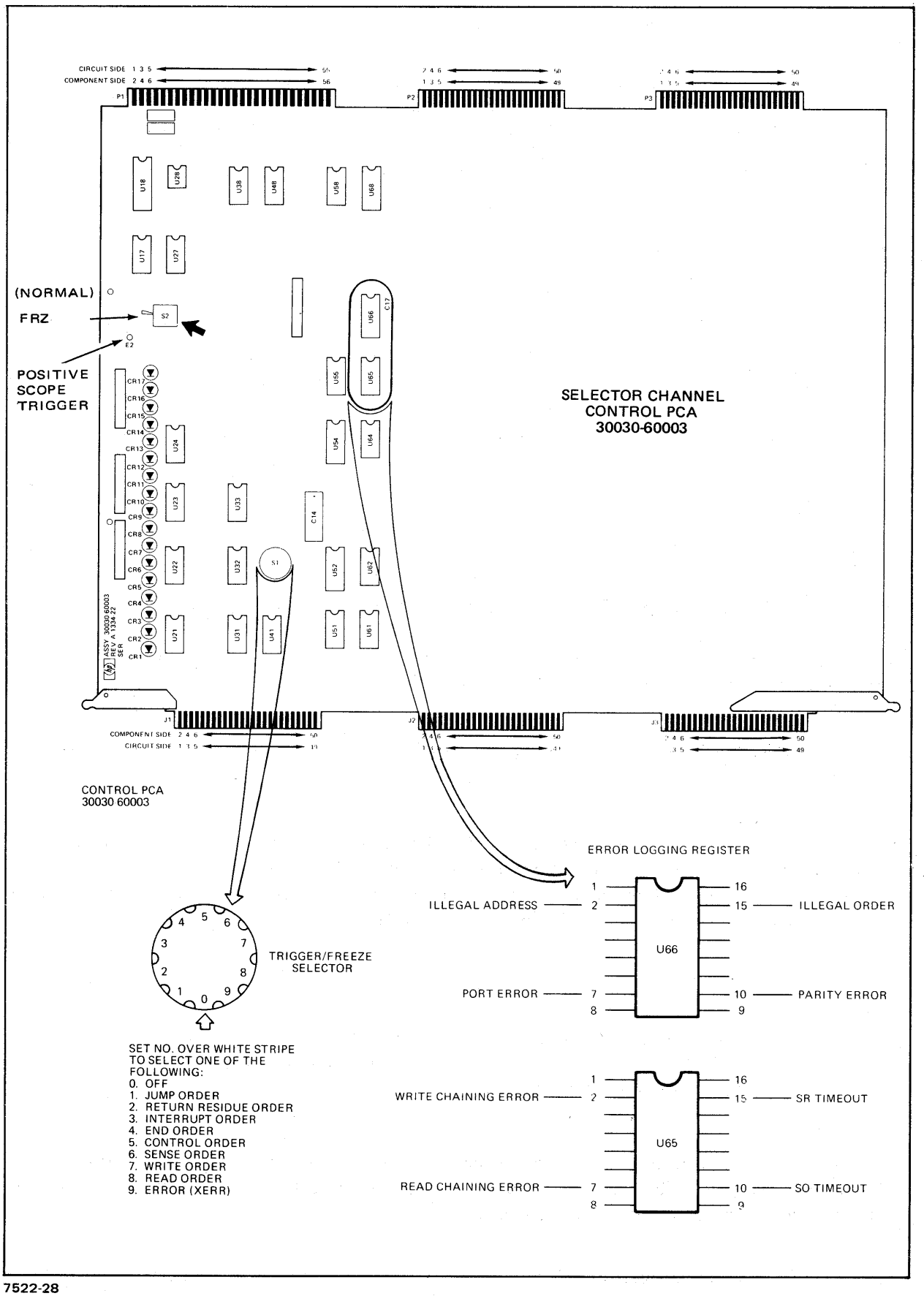
To observe the error logging register contents, do the following:

a. Observe the error register contents on the control PCA with a logic probe or a logic clip.

b. Set the trigger/freeze selector S1 to position 9

c. Set the two-position switch S2 to the FRZ position.

Because the error logging register contents are cleared immediately after an error occurs (during the clear sequence), the contents are valid when the error occurs causing the "freeze".



7522-28

Figure 4-19. Selector Channel Control PCA Switch and Register Locations

4-89. INDICATORS. A number of indicators have been designed into the control PCA to display the state of various signals. Refer to table 4-6 for a list of identifying signals.

Table 4-6. Selector Channel Control PCA Indicators

SIGNAL	INDICATOR	DESCRIPTION
CR1 thru CR5	IOCW4 thru IOCW0	Order code from register PCA
CR6	ACTIVE	An order is currently executing
CR7	WCRO	Word count roll over
CR8	DEVEND	Device end from device controller
CR9	XERR	An error occurred
CR10	RR	State of the RR (return residue) FF
CR11	END	State of the END FF
CR12	JUMP	State of the JUMP FF
CR13	CTRL	State of the CTRLR FF
CR14	CHAN SR	Service request from device controller
CR15	CHAN SO	Service out from channel
CR16	CHAN ACK	Channel acknowledge from device controller
CR17	FREEZE	Clock is frozen by a selected condition

4-90. SELECTOR CHANNEL MAINTENANCE PCA (SCMB) 30033-60001

The selector channel maintenance board PCA (SCMB) was designed to aid the maintenance of the selector channel and multiplexer channel.

4-91. CONFIGURATION. Three jumpers must be configured on the SCMB. See figure 4-20. They are:

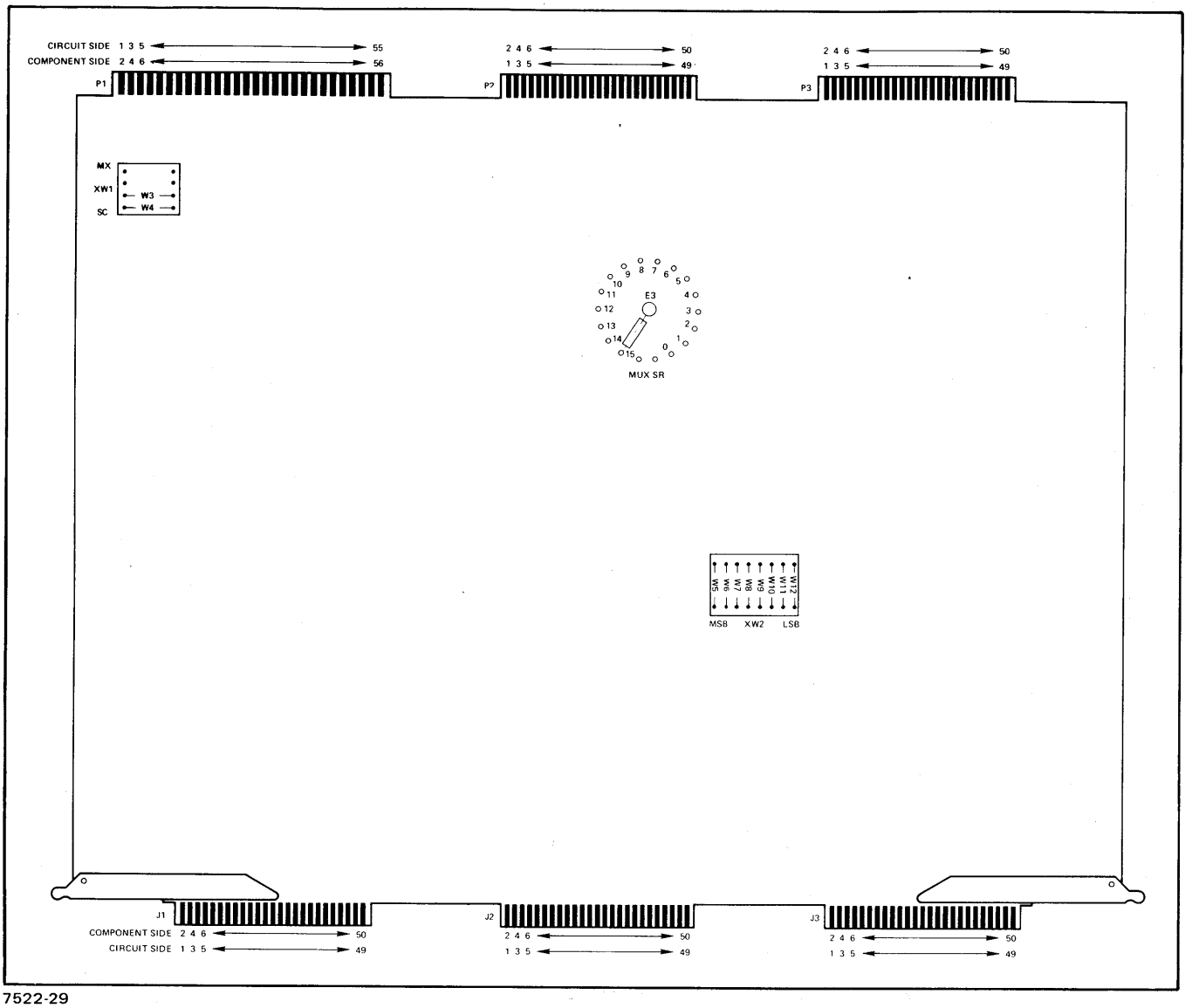
- XW1 — This jumper selects whether the SCMB is to be used on the selector channel or the multiplexer channel. A plug-in containing two jumper wires is installed in XW1. If the jumper wires are aligned with SC on the PCA, the PCA is enabled for use with the selector channel. If the jumper wires are aligned with MX, the PCA is enabled for use with the multiplexer channel.

NOTE

When jumper XW1 is in the MX position and the SCMB is installed in the multiplexer channel, the selector channel diagnostic verifies the operation of the SCMB.

- MUX SR — This jumper selects a service request number used when the SCMB is used with a multiplexer channel. This 16-position jumper should be installed to provide a service request number not used by any other device controller in the system.

- XW2 — These jumpers select SCMB the device number. A jumper wire installed selects a "0" in that position. Use a device number not already assigned.



7522-29

Figure 4-20. SCMB Jumper Locations

4-92. SYSTEM CONTROL PANEL 30003-60012

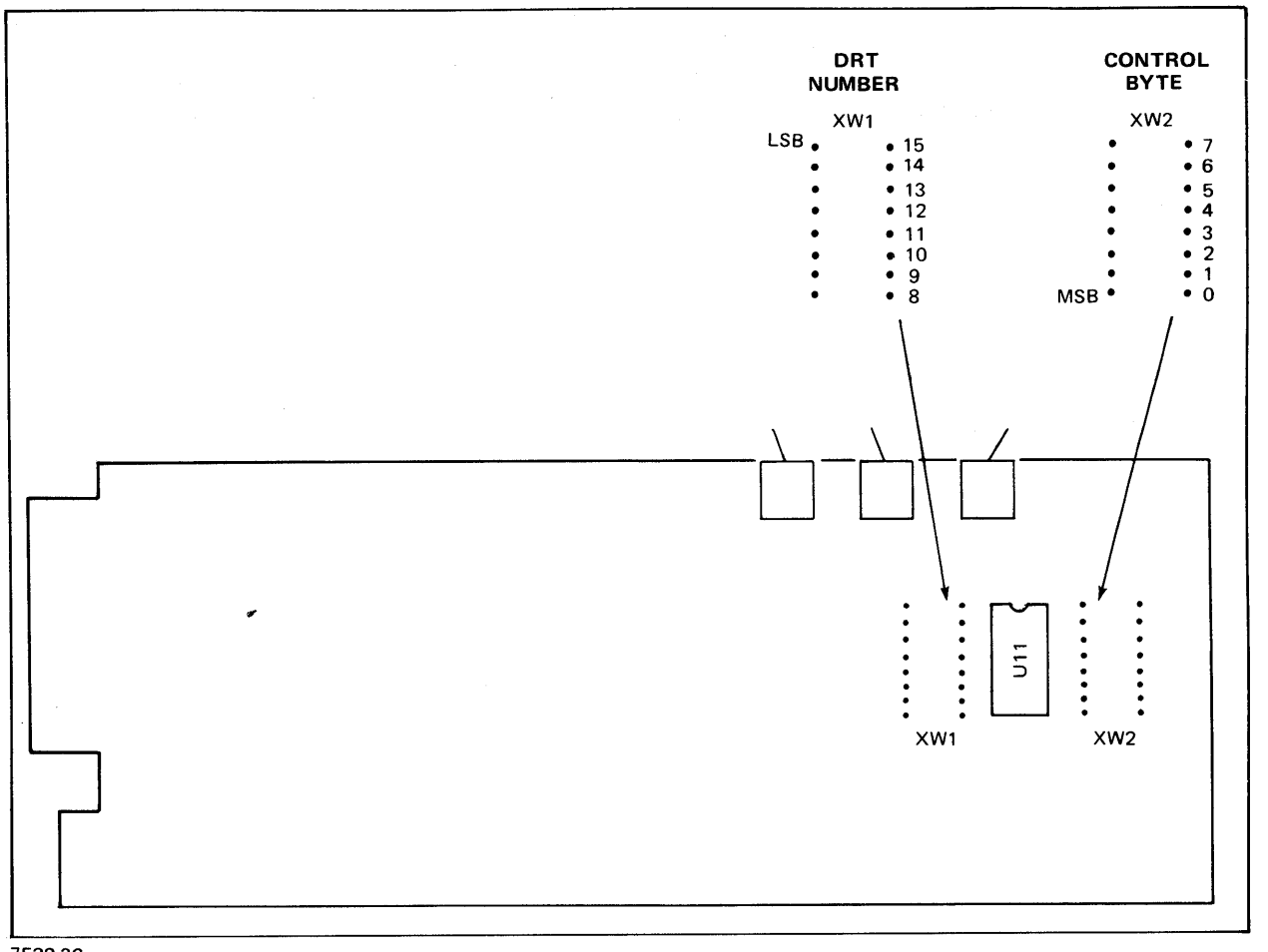
4-93. DRT NUMBER. Jumpers are inserted in socket XW1 to configure a DRT number and and into socket XW2 to configure a control byte. The presence a of jumper signifies a logical "1". By preconfiguring the DRT number and control byte, nothing need be entered in the SYSTEM SWITCH REGISTER switches when a system dump is performed. See figure 4-21 for the location of the sockets.

4-94. MEMORY IC REPLACEMENT

Replacement of the memory array chips can only be performed by those specifically trained in the procedure. Attempting replacement by non-trained personnel can ruin the PCA.

NOTE

Only IC memory chips marked with HP part number 5080-4560 can be used for replacements. Reliability of the PCA will be seriously degraded if this note is not observed.



7522-36

Figure 4-21. System Control Panel Jumper Locations

4-95. PREVENTIVE MAINTENANCE

Refer to the HP 3000 Computer System Support Log, part number 03000-90117 for the preventive maintenance intervals and routines.

4-96. (Deleted)

4-97. MEMORY MODULE

The memory module provides high-speed storage for the HP 3000 Series II Computer System. Memory operates as an error correcting memory with one bit error correction. Memory can be made to operate as a non-error correcting memory with a parity bit by removal of one PCA. However, this is not the normal operating mode. There are four PCA's basic to any memory module:

- Memory Control and Logging (MCL) PCA 30007-60002. This PCA contains the read/write control circuits, address and data registers, refresh circuits, error logging array (ELA), and error correction logic.

- Semiconductor Memory Array (SMA) PCA 30008-60002. This PCA contains the 32K word dynamic MOS semiconductor memory, I/O receivers and drivers, and one of the check bits.

- Fault Correction Array (FCA) PCA 30009-60001. This PCA contains the check bit parity generators and check bit storage array. Removal of this PCA from the memory module causes memory to operate as a non-error correcting memory. The check bit storage array on this PCA is also a dynamic MOS semiconductor memory, the same type used on the SMA PCA.

- Fault Logging Interface (FLI) PCA 30009-60002. This PCA contains the control circuits and I/O logging array for interrogating the error logging array in the MCL PCA.

A memory module may be from 32K to 128K words in 32K increments. Up to four memory modules are permitted in a system but the maximum word capacity of a system is limited to 256K words. One MCL PCA can support up to four SMA PCA's (128K words). One FCA PCA can support up to 128K words of memory. One FLI PCA can support up to 256K words of memory. A bank therefore can contain a maximum of 64K words. Table 4-7 shows the possible memory configurations available and the total number of PCA's required.

Table 4-7. Memory Configurations

Bank	System Word Capacity	PCA's Required				
		MCL	SMA	FCA	FLI	Total
0	32K	1	1	1	1	4
0	64K	1	2	1	1	5
1	96K	1	3	1	1	6
1	128K	1	4	1	1	7
2	160K	2	5	2	1	10
2	192K	2	6	2	1	11
3	224K	2	7	2	1	12
3	256K	2	8	2	1	13

Memory has the following operating modes and specifications:

- WRITE 700 nsec minimum cycle time

- READ 350 nsec access, 700 nsec cycle time

- READ WRITE ONES (RW1) 350 nsec access, 1050 nsec cycle time

- NO OPERATION (NOP) 700 nsec cycle time

Operating power for the FCA and SMA PCA's and for the refresh and power fail circuits of the MCL PCA is supplied by a rechargable battery pack in the HP 30311A Semiconductor Memory Power Supply. The power supply can support 128K words of memory. Two power supplies are required to support a memory greater than 128K words. When ac line power is removed or lost, and when the system is placed in the standby condition, power is obtained from the battery. When the power supply

input voltage is removed, battery power is available for up to 90 minutes (depending on memory size and battery condition) to maintain memory data and check bits. The volatile characteristics of a dynamic MOS semiconductor memory dictates this back-up power requirement.

The memory module interfaces with other modules in the system through the Central Data Bus (CTL). Other modules on this bus may request transfers of data to or from the memory modules. Operation of the memory with other modules on the CTL bus is controlled by the MCU logic (module control unit) on the MCL PCA. The MCL PCA checks all data on the CTL bus for correct parity during a write operation and provides correct parity to the CTL bus during a read operation.

4-98. ERROR CORRECTION

Error correction detects and corrects all single bit errors. Some multiple bit errors are detected, but not corrected. Error checking and correcting occurs during the normal memory cycle of READ and RW1 operations only.

The FCA PCA adds a five bit check field (A,B,C,D,E) to each 16 bit memory word. The check bits are actually parity bits calculated over specific bits of the data word. See figure 4-22 for the check bit assignments.

DATA BITS																CHECK BITS
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
X	X	X	X	X	X	X	X									A even parity
X	X	X	X					X	X	X	X					B odd parity
X				X	X			X	X			X	X	X		C even parity
	X			X		X		X		X		X	X		X	D odd parity
		X			X		X			X	X	X		X	X	E even parity

7522-52

Figure 4-22. Check Bit Assignments

During the WRITE operation, check bit A is stored in the SMA PCA 17th bit position where the data parity bit would normally be stored in a non-error correcting memory system. Check bits B,C,D, and E are stored on the FCA PCA.

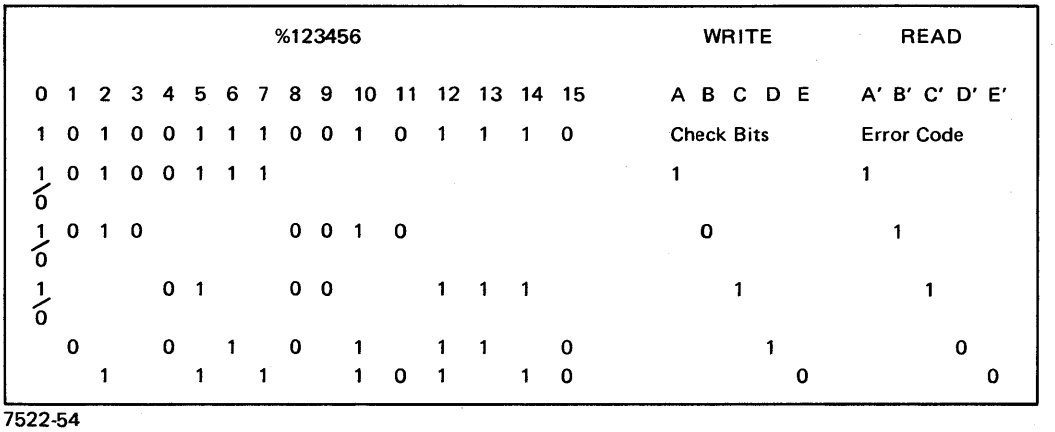
During the READ operation, parity is checked on the same data bits, and the check bits. If the resulting error code (A',B',C',D' and E') calculation is zero, no error occurred in memory. If the error code is other than zero, the appropriate error bit is toggled. Figure 4-23 shows the bit pattern and check bits generated for a data word of %123456 during a WRITE and a READ operation. The figure illustrates the check bits produced when no error occurs, the error code is equal to zero.

%123456																WRITE					READ				
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	A	B	C	D	E	A'	B'	C'	D'	E'
1	0	1	0	0	1	1	1	0	0	1	0	1	1	1	0	Check Bits					Error Code				
1	0	1	0	0	1	1	1									1					0				
1	0	1	0					0	0	1	0						0					0			
1				0	1			0	0			1	1	1				1					0		
	0			0		1		0		1		1	1		0				1					0	
		1			1		1			1	0	1		1	0					0					0

7522-53

Figure 4-23. Check Bits and Error Code (No Error)

Using the same data word (%123456), figure 4-24 illustrates the error code produced during a READ operation when an error in memory drops bit 0. The resulting error code (11100) is interpreted by table 4-8 as a fault in bit 0. Before the data is presented on the CTL bus, bit 0 would be toggled, thereby correcting the error. Note that the check bits generated in both figures are identical, this is because the check bits are generated on the data bits before data is entered in memory.



7522-54

Figure 4-24. Check Bits and Error Code (Error Condition)

To maintain system integrity, parity is checked on each word written into memory. If parity is wrong on the CTL bus, it is indicated on the SYS PE line. In the error correcting memory, parity is generated by the FCA PCA. When data is read from memory, parity is calculated from the field of data bits (0 - 15). If an error is made on any data bit, parity is toggled along with the particular error bit. Referring again to figure 4-24, the data read (0 010 011 100 101 110) would be modified to produce a data word of 1 010 011 100 101 110 and a parity bit of 0.

If memory is operating as non-error correcting, parity is checked and written as received on the CTL bus and the same value is placed on the bus during a read operation.

When errors are corrected, a logic "1" is stored in a Error Logging Array (ELA) static 1K RAM located on the MCL PCA. The RAM is organized in a 1024 X 1 bit array requiring 10 bits for addressing. The five most significant bits of the address correspond to the bank bit 0 and four most significant bits of the memory address that had an error bit. The five least significant bits of the error logging array address correspond to the error code A' thru E'. Any error logging array location containing a "1" signifies an error was detected. The error logging array is read under program control by the FLI PCA.

Figure 4-25 illustrates the structure of the error logging array address for an error in bit 0 of memory address 10000.

Figure 4-25 shows the formation of a 10-bit error logging address 0047. This address contains a logic "1" if bit 0 of system address 010000 through 017777 had been corrected. Address 010000 is located on SMA PCA board 1, the memory chip is on row 1 (chip select line 1), the error bit 0 will identify the specific chip. The error logging array can record errors occurring on up to four SMA PCA'sand one FCA PCA. An additional MCL PCA containing the error logging array and a FCA PCA must be installed whenever memory size exceeds 128K words.

The FLI PCA under program control interrogates the error logging array in the MCL PCA approximately once each hour, however, this can be changed by running the program MEMTIMER (refer to paragraph 4-99). If a logic "1" is detected in the array, the error address is read and decoded. An error file is updated that can be accessed by the CE during PM intervals. The file will display information pertaining to memory errors.

Table 4-8. Error Code Definitions

Error Code					Fault Conditions
A'	B'	C'	D'	E'	
0	0	0	0	0	No Error
1	0	0	0	0	Check bit A
0	1	0	0	0	Check bit B
1	1	0	0	0	Bit 3
0	0	1	0	0	Check bit C
1	0	1	0	0	Multiple bit *
0	1	1	0	0	Bit 9
1	1	1	0	0	Bit 0
0	0	0	1	0	Check bit D
1	0	0	1	0	Bit 6
0	1	0	1	0	Read CLK failure **
1	1	0	1	0	Bit 1
0	0	1	1	0	Bit 13
1	0	1	1	0	Bit 4
0	1	1	1	0	Bit 8
1	1	1	1	0	Multiple bit *
0	0	0	0	1	Check bit E
1	0	0	0	1	Bit 7
0	1	0	0	1	Bit 11
1	0	0	0	1	Bit 2
0	0	1	0	1	Bit 14
1	0	1	0	1	Bit 5
0	1	1	0	1	Multiple bit *
1	1	1	0	1	Multiple bit *
0	0	0	1	1	Bit 15
1	0	0	1	1	Multiple bit *
0	1	0	1	1	Bit 10
1	1	0	1	1	Multiple bit *
0	0	1	1	1	Bit 12
1	0	1	1	1	Multiple bit *
0	1	1	1	1	Check bit I/O driver fault **
1	1	1	1	1	Check bit I/O driver fault **

* Any two or more bit failures in the same address
** Fault occurred in peripheral circuit

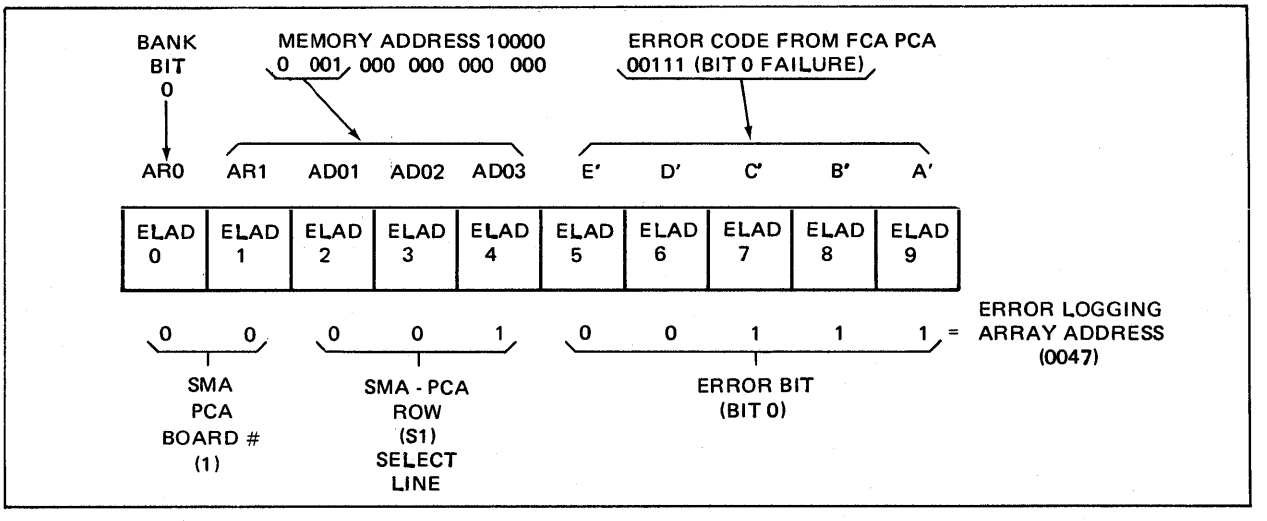


Figure 4-25. Error Logging Array Address Structure

4-99. MEMORY ERROR LOGGING FACILITY

The memory error logging facility allows the CE or system manager to examine the error history of memory. The error logging facility consists of the following elements:

- Error correcting memory and the FLI PCA
- Memory error logging system process (MEMLOGP)
- Memory error log analysis program (MEMLOGAN)
- Memory error logging internal update program (MEMTIMER)

Memory error logging is in no way connected to or related to standard system logging, both function independently. None of the operator interfaces to system logging have an effect on memory logging. Memory error logging will always be invoked if error correcting memory is present in the system.

MEMLOGP is a system process that runs under MPE. Once initiated, MEMLOGP automatically and periodically interrogates the FLI PCA to obtain the latest error information.

MEMLOGP is activated during the initialization phase of MPE (coolstart, warmstart, coldstart, reload, update). MEMLOGP cannot be activated at any other time. If MEMLOGP cannot be initiated successfully during initialization, another attempt cannot be made until the system is brought up again.

MEMLOGP determines if error correcting memory is present by attempting to obtain the status of the FLI PCA (DRT 2). If the PCA does not respond, error correcting memory is absent from the system and MEMLOGP immediately terminates and no message relating to error logging will appear at the system console. If error correcting memory is present, the following message appears at the system console:

ST/<TIME>/MEMORY ERROR LOGGING INITIATED

If the message appears, it occurs after the DATE/TIME messages and before the WELCOME message.

MEMLOGP attempts to open the system memory error disc file MEMLOG (MEMLOG.PUB.SYS). If no such file exists on the system, a new file will be created. If MEMLOG already exists, the file will be opened without altering the information contained in the file. The file remains open as long as the system is up. During those periods when MEMLOGP is accessing the file, it will lock and unlock the file as necessary to insure no other access to it. The log analysis program (MEMLOGAN) similarly locks and unlocks the file when it is accessing it.

If an operational error is encountered by MEMLOGP, the process will display an error message and terminate. The message displayed is:

ST/<TIME>/MEMORY LOGGING ERROR#<ERRNUM>.LOGGING STOPPED

The range and definitions for <ERRNUM> are:

1-10	Internal MEMLOGP errors
1	FLOCK error on MEMLOG file
2	FUNLOCK error on MEMLOG file
3	TIO error. Error logging hardware not ready.
4	CIO error during copy operation from logging array
5	RIO error during scan of logging array (Errors 6-10 reserved for future use.)
20-500	File system errors involving MEMLOG file. All file errors encountered by MEMLOGP are fatal to the process and cause it to terminate. Refer to the MPE Intrinsics Reference Manual (30000-90010) for definitions of the file system error numbers.

Once the MEMLOG file has been opened, MEMLOGP periodically interrogates the error logging array in the MCL PCA via the FLI PCA. If errors have occurred, the MEMLOG file is updated. The error logging array is interrogated via the FLI PCA when MEMLOG is first activated and thereafter once approximately every hour. If one or more errors have occurred in the hour interval since the last log update, MEMLOGP will perform the following operations:

1. Read the appropriate MEMLOG record from disc

2. Scan the error logging array for errors

3. Update the error counter in the MEMLOG record for each location where an error occurred.

4. Reset the error logging array to a no-error condition

5. Write the updated MEMLOG record to disc.

MEMLOGAN (MEMLOGAN.PUB.SYS) is the utility that reads and interprets the error information logged and kept in the MEMLOG file. Because of the security placed on the MEMLOG file by the system, MEMLOGAN can successfully run from an account other than PUB.SYS if:

1. The RELEASE command was entered for MEMLOG by the system manager,or

2. The logon account has system manager capability.

MEMLOGAN will read MEMLOG and output its contents in a meaningful manner. The formal designator of the output device is "OUT". To direct output to the line printer, the following file equation must be entered:

```
:FILE OUT;DEV=LP
```

There is no user dialogue with MEMLOGAN. However, certain MEMLOG file handling operations are available through the PARM parameter of the RUN command. The following PARM values are recognized by MEMLOGAN:

PARM=0 Causes the current contents of MEMLOG to be printed on the output device. The contents of the file will not be changed. This is the default PARM value.

PARM=1 Causes the current contents of MEMLOG to be printed on the output device after which the file is reset to a no-error state. All previously logged errors are deleted from the log file.

NOTE

When a system with error correcting memory is initialized for the first time or the memory size is changed to cross the 128K boundary, MEMLOGAN should be run with PARM=1 as soon as the system is up and running. This will ensure a clean MEMLOG file and that subsequent error counts are valid.

PARM=2 Causes the current contents of MEMLOG to be printed on the output device after which the file is deleted from the system. (This is the only way to remove the MEMLOG file from the system and normally only the system manager would use this PARM value.)

MEMTIMER (MEMTIMER.PUB.SYS) is the utility program which allows the user to modify the interval of time between successive memory log updates. The normal default interval is 60 minutes. This interval provides the average installation with an adequate log of the memory system. For other reasons, it may be desirable to modify the interval to allow increased monitoring of the memory performance. It is the function of MEMTIMER to modify the time interval.

MEMTIMER alters the current timing interval to a new value and terminates the current interval. This causes MEMLOGP to update the memory log file immediately and periodically thereafter according to the new interval specified.

A new timing interval is specified through the PARM parameter of the RUN command. There is no user dialogue with MEMTIMER. The PARM value is given as a positive integer greater than zero which represents the number of seconds between log file updates. To begin memory logging at 10 second intervals, the following RUN command would be entered:

```
:RUN MEMTIMER;PARM=10
```

To return logging to the default interval (60 minutes), the following RUN command would be entered:

```
:RUN MEMTIMER;PARM=3600
```

Three error conditions are detected by MEMTIMER. If the PARM parameter of the RUN command is equal to or less than zero, then MEMTIMER will terminate after printing the following message:

```
** INVALID PARM (DELAY) VALUE **
```

The current time interval remains unchanged.

If MEMLOGP has been terminated, then MEMTIMER will terminate itself after printing:

```
** MEMORY LOGGING PROCESS NOT ACTIVE **
```

In this case there is no timing interval update.

If either the memory logging hardware is not present on the system or MEMLOGP is currently updating the memory log file, the following message will appear:

```
** MEMLOGP TIMER ENTRY NOT FOUND **
```

In this case, the timing interval will be updated. If the memory logging hardware exists on the system, MEMTIMER should be run again to insure that MEMLOGP will recognize the updated interval immediately.

Note that the default timing interval will become the current timing interval each time the system is brought up. Therefore, if a non-default timing interval is desired, MEMTIMER must be run after each initialization of the system.

4-100. OUTPUT. MEMLOGAN output will vary according to whether the MEMLOG file is null or updated, and if updated, whether errors have occurred.

If the MEMLOG file is null (after running MEMLOGAN with PARM= 1) MEMLOGAN will terminate after displaying the message:

```
*NO ENTRIES IN MEMLOG FILE*
```

If the MEMLOG file is not empty, MEMLOGAN will print the date and time of the first and last log updates. If errors have been logged, the date and time of the first and last error logged will also be printed. If no errors have been logged, MEMLOGAN will terminate after displaying the message:

```
LOGGING STARTED -DATE:
LAST LOG UPDATE -DATE:
***NO ERRORS LOGGED***
```

If errors have been logged, MEMLOGAN will continue by printing a tabular interpretation of the information in the MEMLOG file. The format of the printout is shown in figure 4-26.

ADDRESS			ERROR TYPE				ERROR COUNT
MEMORY	LOC	ROW	TYPE	BIT	BOARD	CHIP	
<MEM>	<LOC>	<ROW>	<TYPE>	<BIT>	<BOARD>	<CHIP>	<CNT>

WHERE:

<MEM> = BANK <N> WITH <N> = 0,1,2,3. BANK0 AND BANK1 REFER TO THE LOWER 128K OF MEMORY; BANK2 AND BANK3 REFER TO THE UPPER 128K OF MEMORY

<LOC> = L32K, U32K. L32K REFERS TO THE LOWER 32K WORDS OF <MEM>; U32K REFERS TO THE UPPER 32K WORDS OF <MEM>.

<ROW> = 0-7. <ROW> IS AN INTEGER WHICH CORRESPONDS TO THE ROW DESIGNATION ON THE BOARD IN WHICH THE FAILING CHIP IS LOCATED.

<TYPE> = CHECK. CHECK BIT ERROR OCCURRED;

<BIT> = A,B,C,D,E. <BIT> REFERS TO THE FAILING CHECK BIT

<BOARD> = SMA. SEMICONDUCTOR MEMORY ARRAY BOARD. CHECK BIT A ONLY.
FCA. FAULT CORRECTION ARRAY BOARD. CHECK BITS B,C,D,E.

<CHIP> = U<N> WITH <N> = CHIP NUMBER

= DATA. DATA BIT ERROR OCCURRED:

<BIT> = 0-15. <BIT> REFERS TO THE FAILING DATA BIT.

<BOARD> = SMA. SEMICONDUCTOR MEMORY ARRAY BOARD.

<CHIP> = U<N> WITH <N> = CHIP NUMBER.

= LOGGING SYSTEM ERROR. THIS IS AN ERROR WHICH SHOULD NEVER OCCUR UNLESS THE ERROR LOGGING HARDWARE ITSELF FAILED. THIS ERROR REPRESENTS AN ERROR ON THE FAULT LOGGING INTERFACE PCA RATHER THAN A MEMORY ERROR.

= MULTIPLE BIT ERROR.

= I/O DRIVER FAULT. CHECK BIT I/O DRIVER FAULT.

= READ CLOCK FAILURE.

<CNT> = AN INTEGER REPRESENTING THE NUMBER OF TIMES THIS ERROR WAS DETECTED AND LOGGED.

Figure 4-26. Error Printout Format

Figure 4-27 shows a typical error message.

ERROR CORRECTING MEMORY LOG ANALYSIS

LOGGING STARTED — DATE: 3/31/76 TIME: 13:35
FIRST ERROR LOGGED — DATE: 3/31/76 TIME: 17:45
LAST ERROR LOGGED — DATE: 4/ 1/76 TIME: 8:29
LAST LOG UPDATE — DATE: 4/ 1/76 TIME: 8:54

ADDRESS			ERROR TYPE				ERROR COUNT
MEMORY	LOC	ROW	TYPE	BIT	BOARD	CHIP	
BANK 0	U32K	2	DATA	7	SMA	U710	8
		5	DATA	9	SMA	U312	1
BANK 1	L32K	7	CHECK	A	SMA	U119	8
		7	CHECK	C	FCA	U112	3

Figure 4-27. Typical Error Message

4-101. ERRORS. If an operational error is encountered by MEMLOGAN, the program will print the appropriate error information and then terminate. A non-file system error causes the following message to be displayed:

*MEMLOGAN ERROR: <ERRNUM>:

Where

<ERRNUM> 1= FLOCK ERROR ON MEMLOG FILE
2= FUNLOCK ERROR ON MEMLOG FILE

The occurrence of a file system error will cause an error tombstone to be displayed followed by either *OUT FILE ERROR* or, *LOG FILE ERROR*.

4-102. CE OPERATING PROCEDURES

The following commands are suggested for the CE to use to obtain hard copy output of memory errors.

```
:HELLO FIELD.SUPPORT,HP32230
:FILE OUT;DEV=LP
:RUN MEMLOGAN.PUB.SYS
```

The line printer will then reproduce a copy of the log file.

4-103. FLI PCA PROGRAMMING

The FLI PCA only accepts direct I/O commands. These commands cause the FLI PCA to copy the contents of the MCL error logging array into the FLI I/O logging array (CIO-Read Copy), determine if

an error log (1) was transferred (TIO-Read Copy Error), search the I/O logging array for the presence of a "1" (CIO-Read Scan) and send the address of where the "1" was stored to the IOP bus (RIO-Address). Direct commands clear the I/O logging array (WIO-Load Block) and then transfer these zeros into the error logging array (WIO-Write Copy). The error logging array would then be cleared and able to start a new fault logging sequence. Interrogating and writing into the error logging array can only occur during refresh time. The following paragraphs explain in detail the control word formats.

4-104. TIO COMMAND. Figure 4-28 shows the word format for a TIO instruction. This instruction can be executed any time.

Bit 0,1, and 2 — These bits have the standard I/O significance.

Bit 3 — Read Scan-This bit is set when a Read Scan is in process and remains set until the completion or termination of the scan.

Bit 4 — DISWEC-This bit is set if the disable error correction FF (DISWEC) is set.

Bit 5 — L/NU 128K-If bit 5 = 1, then the upper 128K ELA has been selected. If bit 5 = 0, then the lower 128K ELA has been selected.

Bit 7 — Read Copy Error-This bit is set if there are one or more errors (1's stored in ELA) during a Read Copy. This bit is cleared by any CIO or WIO Instruction.

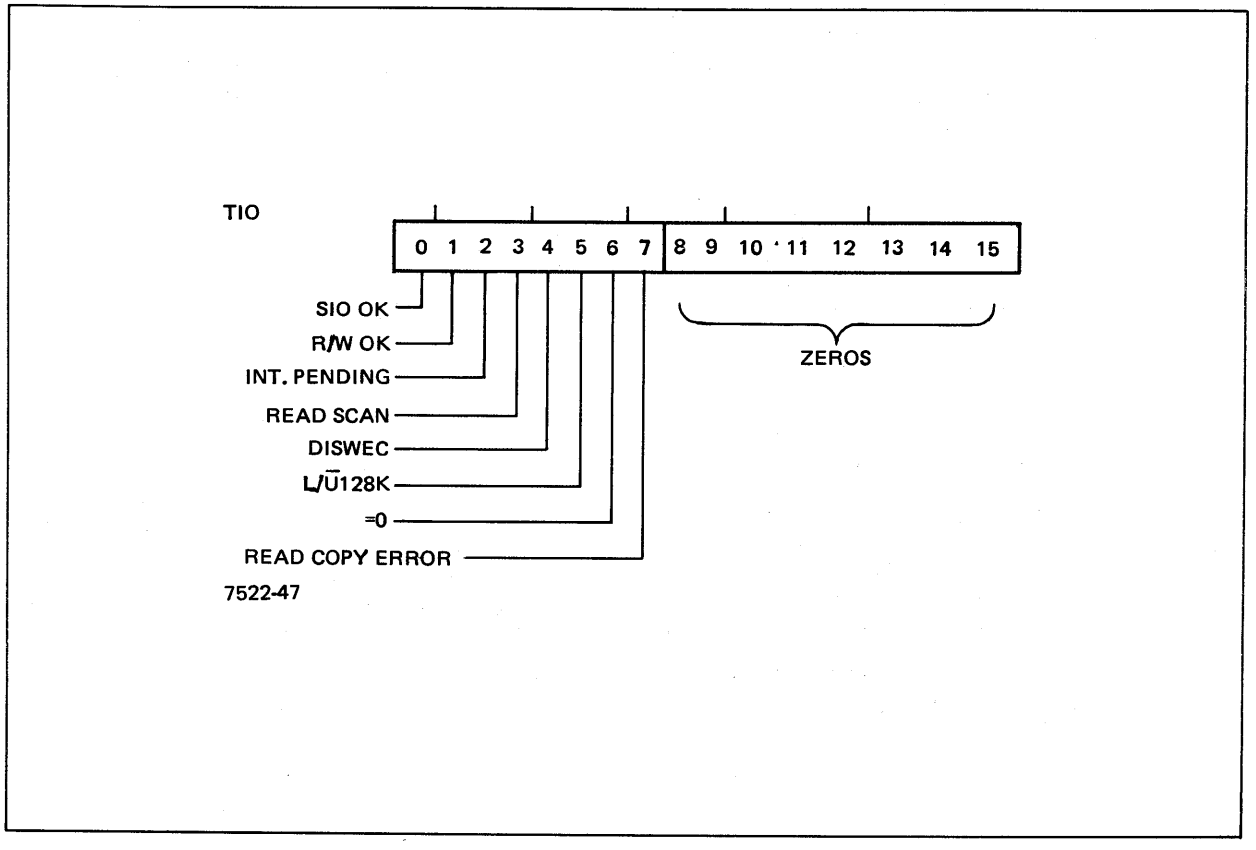


Figure 4-28. TIO Word Format

4-105. CIO COMMAND. CIO instructions may be executed only if TIO bit 1 = 1 (R/W OK) except for a CIO master clear which can be executed at any time. Figure 4-29 shows the word format of the CIO instruction.

Bit 0 Master Clear-When set, causes the FLI PCA to reset and inhibits simultaneous Read Copy, Read Scan and/or DISWEC CIO instructions, or aborts any of these operations.

Bit 2 Read Copy-Causes the contents of the lower or upper 128K ELA transferred to the I/O logging array starting at the address location specified by bits 6 through 15 and ending at %1777. The Read Copy is completed when the Address Counter rolls over to %0000. The total time for a Read Copy is less than or equal to 0.25 seconds. During a transfer TIO bit 1 = 0 (R/W not OK) and goes to a 1 within 100 usec after completion of a copy. A Read Copy will be terminated by the occurrence of a PFW, PON, I/O Reset or CIO Master Clear. Read Copy will inhibit a simultaneous Read Scan and is aborted by a Master Clear.

Bit 3 Read Scan-The I/O logging array contents are interrogated starting at the address specified by bits 6 through 15 and finishing at address %1777. The scan is completed when the Address Counter rolls over to %0000. The scan will halt at any I/O logging array location containing an error. An RIO instruction may be executed to retrieve the address of that error location. After the RIO completion the scan will resume. During a scan, TIO bit 1 = 0 (R/W not OK) and goes to a 1 two usec after a halt on error or a scan completion. A read scan can be aborted by a Master Clear.

Bit 4 DISWEC-The disable write error correction FF is set on the FLI PCA resulting in a memory operation with the error correction logic disabled. During a write operation, the data bits and check bit A can be changed without modifying the check bits B through E. Note that error correction is disabled on all MCL PCA's. Bit 4 can be cleared by I/O Reset, PFW, PON, completion of a Read Copy or Write Copy (WIO instruction), CIO Master Clear, or setting bit 4 to a 0.

Bit 5 L/NU 128K-If bit 5 = 1, then the upper 128K ELA is selected. If bit 5 = 0, then the lower 128K ELA is selected. The upper or lower 128K ELA is selected after one CPU clock cycle.

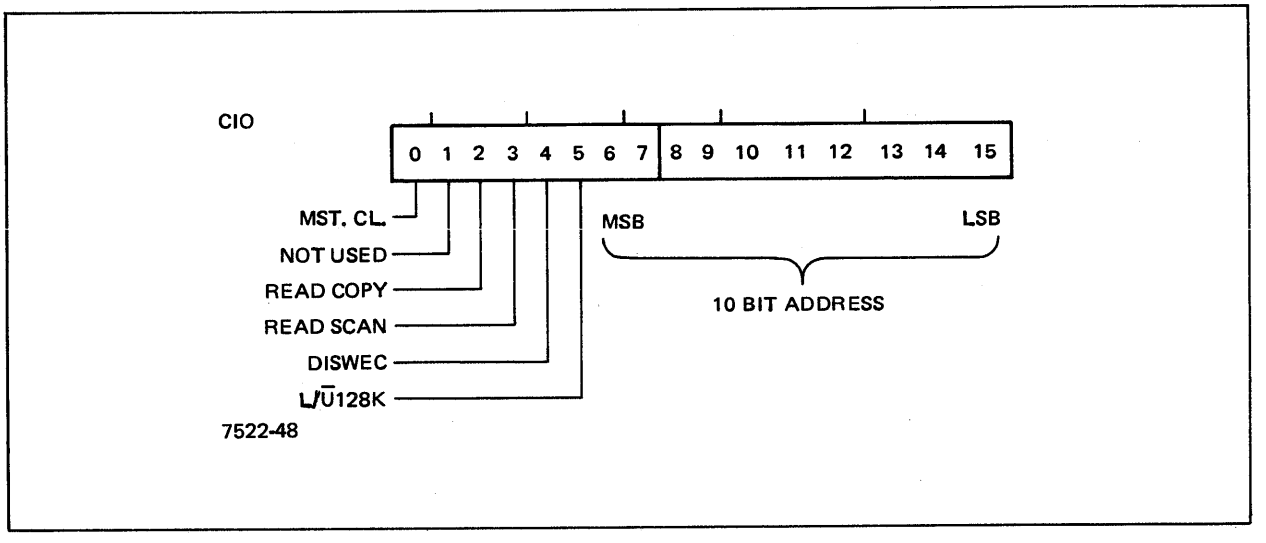


Figure 4-29. CIO Word Format

Bits 6-15 Address-The 10 bit address (1024 locations) is the starting address for a Read Copy of the ELA to the I/O logging array or a Read Scan of the I/O logging array. The address is loaded on all CIO instructions and is not affected by master clear.

4-106. WIO COMMAND. WIO instructions may be executed only if TIO bit 1 = 1 (R/W OK). Figure 4-30 is the word format for a WIO instruction.

Bit 0 Data-This bit is used as the data in a WIO Load Block and Load Single instruction.

Bit 2 Write Copy-The contents of the I/O logging array is transferred into the upper 128K ELA or the lower 128K ELA starting at the address specified by bits 6 through 15, and ending at address %1777. At the completion of the transfer, the Address Counter is set to %0000. During a transfer, TIO bit 1 = 0 (R/W not OK) and goes to a 1 at 100 usec after a transfer. A CIO Master Clear will abort a Write Copy.

Bit Load Block-The data in bit 0 (Data) is transferred to the I/O logging array in all locations starting at the location specified by bits 6 through 15 and ending at %1777. Upon completion of the transfer the Address Counter is set to %0000. During the transfer, TIO bit 1 = 0 and goes to a 1 two usec after a transfer. A Load Block will override simultaneous Write Copy and/or Load Single.

Bit 4 Load Single-The data in bit 0 (Data) is transferred to the I/O logging array at the address location specified by bits 6 through 15. The Address Counter is not changed after the completion of the transfer.

Bit 5 L/NU 128K-If bit 5 = 1, then the upper 128K ELA is selected and if bit 5 = 0, then the lower 128K ELA is selected during a Write Copy execution. The upper or lower 128K ELA is selected after one CPU clock cycle.

Bits 6-15 Address-The 10 bit address (1024) locations is the starting address for a Write Copy of the I/O logging array to the ELA, a Load Block of the I/O logging array, or the address for a Load Single of the I/O logging array.

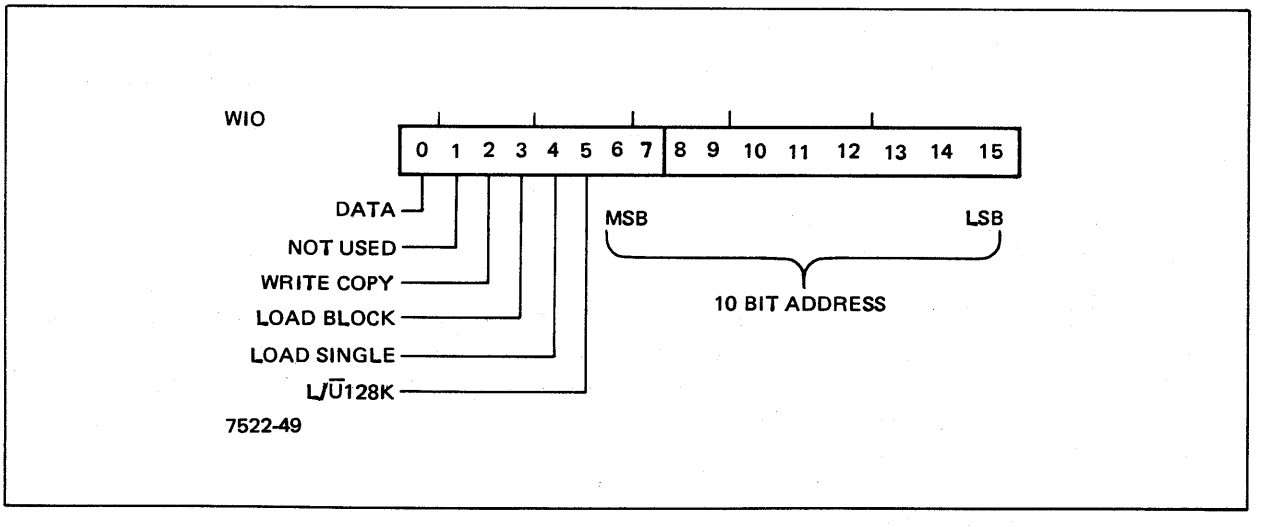


Figure 4-30. WIO Word Format

4-107. RIO COMMAND. Figure 4-31 shows the word format for the RIO command.

Bit 0 This bit is set if there was an error logged in the I/O logging array during a Read Scan and the address of that error is specified by bits 6 through 15.

Bit 1 R/W OK-This bit contains the same information as R/W OK on a TIO.

Bit 3 Read Scan-This bit is set when a Read Scan is in process and remains set until the completion or termination of a scan.

Bit 4 DISWEC-This bit is set if the disable error correction FF is set.

Bit 5 L/NU 128K-If bit 5 = 1, the upper 128K ELA has been selected and if bit 5 = 0, the lower 128K ELA has been selected.

Bits 6-15 Address-This is the I/O logging array address of a logged error during a Read Scan.

NOTE

The following discussion uses the convention of placing the character N before a mnemonic or functional name to signify the "not" condition.

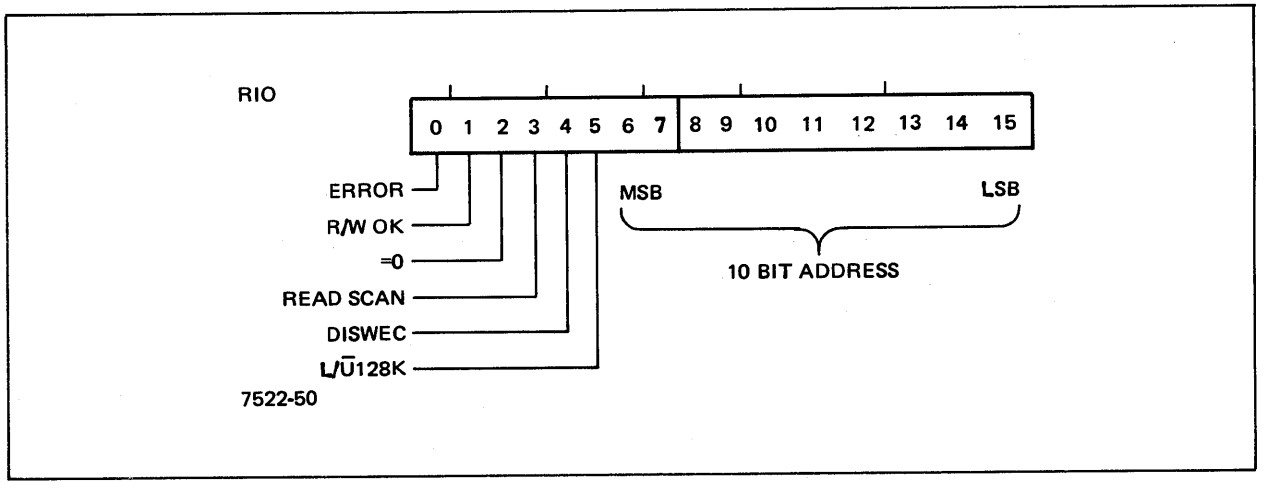


Figure 4-31. RIO Word Format

4-108. INTERFACING

4-109. CTL DATA BUS. The CTL data bus provides for the transfer of data between the memory module and the other modules on the bus via the MCUD (00-15) lines. Data parity is provided by the MCUD PRTY line. Addressing information used to select a specific address of a word in memory is transferred via the data lines. See figure 4-32. Control information is provided for the following functions:

- To select a module, TO (00-02)
- To designate the requesting module, FROM (00-02)

- To indicate whether the module is ready or not, READY (00-03)
- To resolve priority considerations, ENABLE (00-03)
- To select a specific memory operation, MOP(00-01)
- To indicate a parity error on transfer of control information and data parity error during a write cycle, NSYS PE.
- To indicate parity for the control lines, SYSPRTY
- The "not" master reset (NMCU RST) pulse initializes the MCL PCA during initial power turn-on and during power failure. Control can be reset during a refresh cycle without loss of stored data.
- To indicate an address parity error, NMCUD PE

4-110. IOP BUS. The FLI PCA interfaces with the IOP bus to execute direct I/O commands. The FLI PCA interrogates the MCL fault logging array and stores the contents into the FLI I/O logging array. Commands on the IOP bus then cause a read of the I/O logging array and transfer the contents into a disc file for future analysis.

4-111. FAULT LOGGING INTERFACE BUS. The fault logging interface bus is a flat cable connected between P3 on the MCL PCA and P2 on the FLI PCA. All communication between these two PCA's occurs on this bus. When a memory is configured above 128K words, this bus extends to P3 of the upper 128K MCL PCA. A single FLI PCA can communicate independently over the bus to the selected (upper or lower 128K) MCL PCA.

4-112. POWER BUS. The CPU applies an ENTIMER signal to the MCL PCA via the power bus to enable a timer during every write cycle. If the data is not received within 6.4 msec during a write operation, the timer resets the control circuits to prevent memory from waiting for data. No loss of memory data occurs during an incomplete write cycle.

System clock (NMCUCLK) is a 175 nsec square wave from the CPU that provides timing to the MCU circuits. The NMCUCLK can be halted and pulsed for maintenance purposes with the single cycle switch on the HP 30354A Maintenance Panel. For maintenance purposes, NMCUCLK can be disconnected and replaced with an external timing signal.

Refresh clock timing is automatically selected from an oscillator internal to the MCL PCA, or from the NFRUNCLK signal input. NFRUNCLK is in sync with NMCUCLK, but cannot be halted with the single-cycle switch.

Power failures are sensed in the HP 30310A Power Supply and initiate the NPF WARN (power fail warning) to the CPU and memory. The MCL PCA guarantees 3.5 msec for the CPU to execute its power fail routine and store the necessary information into memory. After this 3.5 msec interval, clock timing to memory is disabled to prevent any further read or write operations until power is restored.

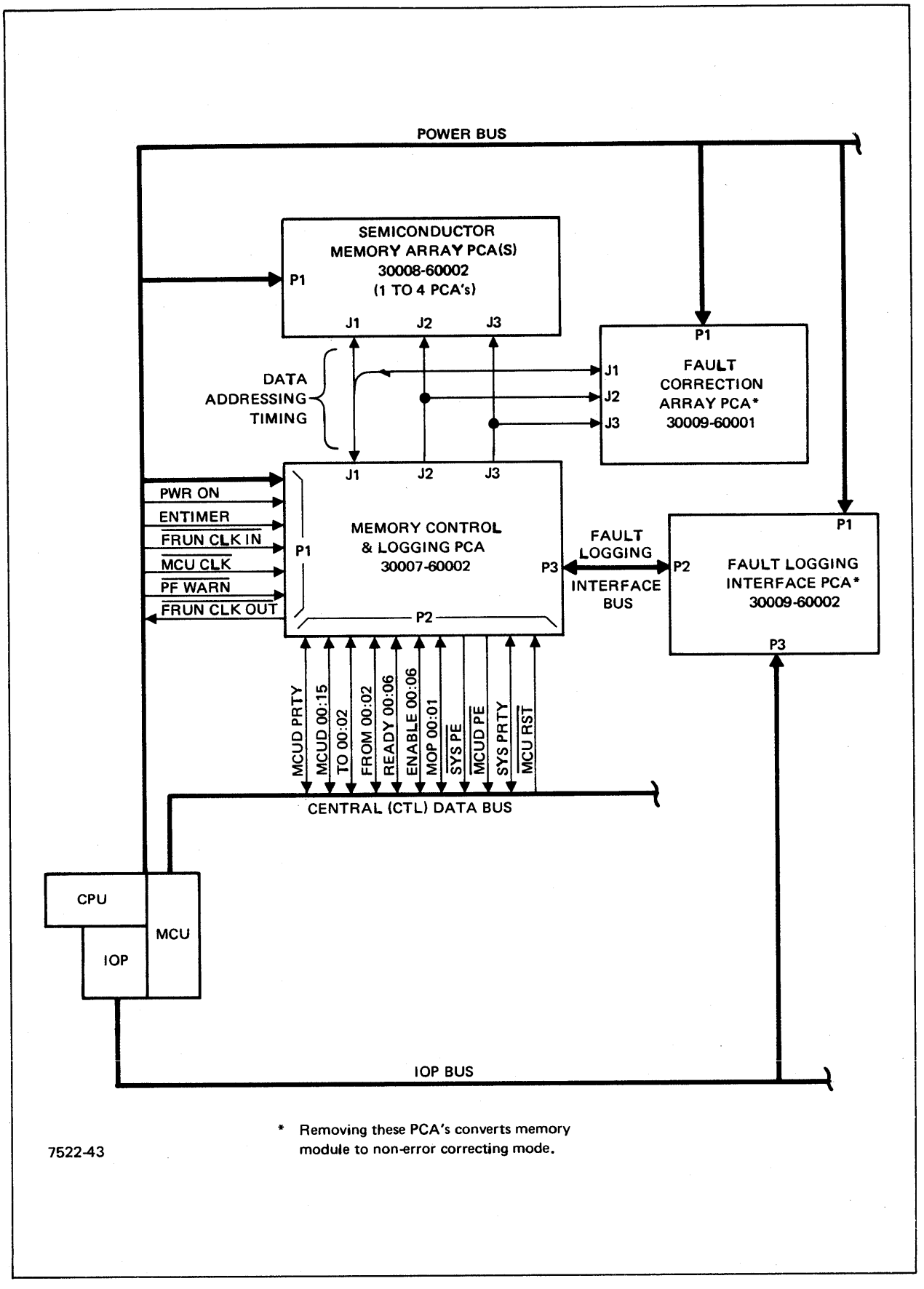


Figure 4-32. Memory Module Interface Diagram

4-113. ERROR CORRECTING MEMORY MODULE.

A typical error correcting memory module is shown in figure 4-33. The figure shows the major data and signal paths between PCA's in the module.

During a write operation the addressed memory location is latched in the MCL Address Register and is presented to the SMA and FCA Memory Arrays. The memory location in the SMA is therefore accessed and the corresponding section in the FCA Memory Array is also accessed for storing the check bits. Address parity is checked by the MCL Parity Generator/Checker and a parity error is sent on the CTL bus if parity is incorrect. Data parity is also checked during a write operation and indicated on the NSYS PE line.

Data is latched in the MCL Data Register and stored in the SMA Memory Array. The data is also sent to the FCA Check Bit/Error Code Generator to generate the check bits that are then stored in the FCA Memory Array. Four of the check bits are stored in the FCA Memory Array and check bit A is stored in the 17th bit position of the SMA Memory Array.

When a memory location is read, the data from the SMA Memory Array is latched in the MCL Data Register and presented to the FCA Check Bit/Error Code Generator. The check bits that are simultaneously read out with the data are sent to the FCA Check Bit/Error Code Generator, and together with the data bits form a five bit error code (A' - E').

The MCL Error Code Register stores this error code and presents it to the MCL Error Detector and the Multiplexer. If the error code is equal to zero, data from the MCL Data Register is unchanged by the MCL Error Corrector and gated to the CTL bus with parity which is calculated on the data bits.

When the error code is not equal to zero, the MCL Error Detector activates the appropriate output line to the MCL Error Corrector and complements the bit in error. Parity is then calculated on the corrected data bits and sent to the CTL bus with the data. When an error has been detected, the error code along with the bank bit and four most significant bits (A0 - A3) of the address containing the error are formed into a ten-bit address by the MCL Multiplexer. With the error signal present, a "1" is written into the MCL Error Logging Array at the address specified by the Multiplexer. The "1" written into the array signifies that an error actually occurred. The bits of the address where that "1" is stored actually contain the information such as location, type of error, row and chip number where the error occurred.

Under software control, direct I/O commands cause the FLI PCA to interrogate the MCL Error Logging Array approximately once each hour to find out if an error has occurred. The Error Logging Array is then copied into the FLI I/O Logging Array where it is then available to be sent on the IOP bus. The starting address of the interrogation is loaded into the FLI Address Counter. This same address is then applied to the I/O Logging Array and Address Comparator. When the MCL Refresh Counter reaches the starting interrogating address, the FLI Address Comparator signals the R/W Control circuit to read into the I/O Logging Array the contents of the Error Logging Array. The FLI Address Counter increments along with the Refresh Counter to keep both addresses in sync.

When the interrogation is finished, the MCL Error Logging Array should be cleared to all zero's so that repetitive errors can be logged. The I/O Logging Array is read by software and the data is stored in a disc file. The I/O Logging Array can be written into the MCL Error Logging Array. Reading the MCL Error Logging Array can only occur during refresh time. This prevents interference with a normal memory operation, and does not extend the cycle time.

4-114. SMA PCA

The SMA PCA (figure 4-34) contains the 32K word memory array and the circuits that provide address decoding, clock selection, and memory data transfers. All communication with the SMA PCA is governed by the MCL PCA.

The individual semiconductor memory chip is a 4K by 1 storage device (four thousand one bit words). On the SMA PCA the chips are physically arranged in eight lines with 17 chips on a line. This arrangement provides 32K words (8x4K) of storage, each word containing 16 bits and a check bit. Table 1 on figure 4-34 shows the chip enable lines (S0 thru S7), the specific memory chip associated with each bit of the word, and the range of addresses that can be accessed in that line.

Since a maximum of four SMA PCA's can be contained in a memory module (128K), each SMA PCA contains jumpers that identify the portion of memory represented by that SMA PCA. Refer to paragraph 4-66 for the various jumper assignments.

NOTE

Different revisions of the SMA PCA exist in the field. Jumpers for Rev A PCA's are positioned differently than those for PCA's of a later revision.

Memory locations are addressed by a 16 bit word that provides access to 64K word locations. The three bits of the address word (01-03) cause one of eight chip enable lines (S0 thru S7) on the proper SMA PCA to be activated by the Chip Enable Line Decoder, enabling one line of 4K addresses. Bit 00 of the address word (AR1) and the bank bit (AR0) will enable the Chip Enable Line Decoder if the SMA PCA is correctly jumpered; the address selects the upper or lower 32K words of memory. The remaining 12 bits (04-15) of the address word are applied by the Address Drivers to all of the chips in the memory array. However, only those chips that have the Chip Enable line active will permit reading out of or writing into that address.

The polarity of the NR/W signal applied to the memory array determines whether the operation is a read or a write, and whether the data path is from the Data Receivers or to the Data Drvers. The NR/W signal causes multiplexing internally in the memory chip and allows the input and output data to share a common terminal (I/O).

4-115. MCL PCA

4-116. REFRESH. The storage mechanism of a dynamic random access semiconductor memory is charge retention on a capacitor. Because internal leakage paths exist, these capacitors must be periodically recharged or "refreshed" to prevent a loss of memory data. Leakage rate is directly proportional to temperature, therefore, refresh rate must be a direct function of temperature. Refresh consists of a read without the transfer of any data.

A programmed read operation causes 64 cells in each memory chip of the enabled chip select line to be refreshed. However, programmed read operations will not access enough sequential addreses fast enough to recharge all the capacitor elements of the array and prevent loss of data. The refresh circuits on the MCL PCA do provide the refresh clock to the SMA and FCA PCA's at the correct rate and addressing sequence to prevent this data loss.

A refresh cycle restores a block of 64 cells in every memory chip located on each SMA and FCA PCA associated with the MCL PCA. Sixty-four refresh cycles are required to refresh the entire PCA (64 x 64

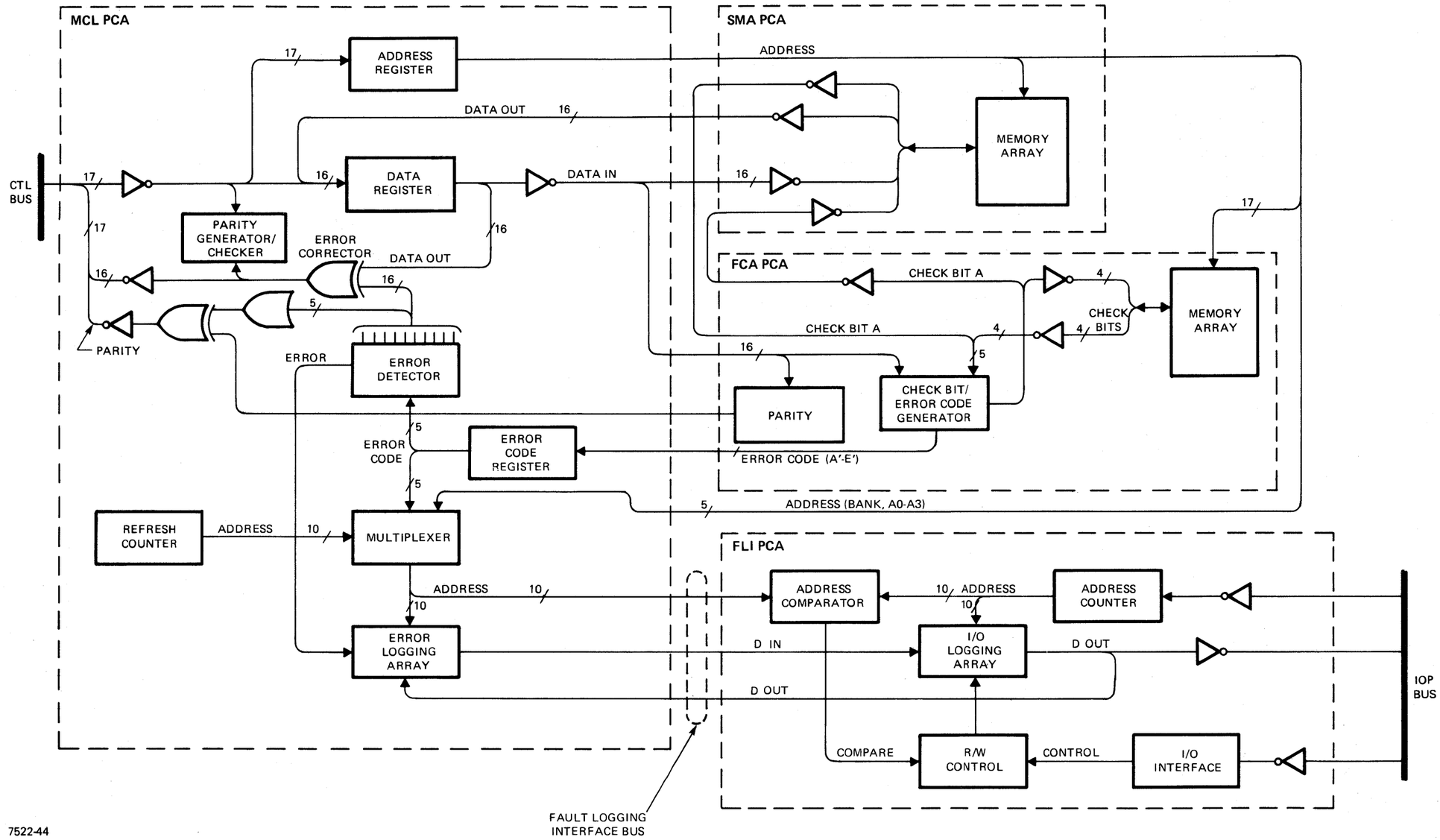
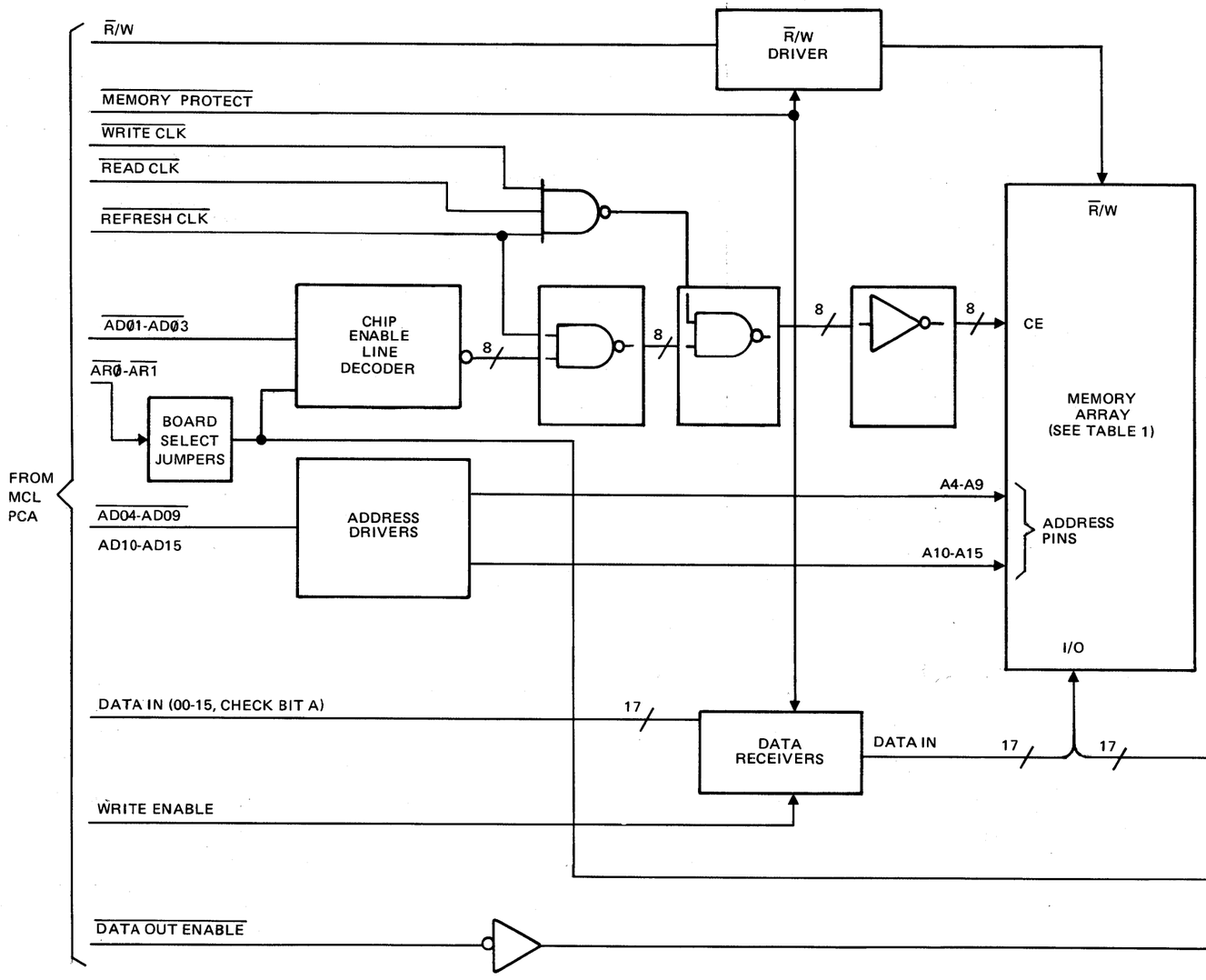


Figure 4-33. Error Correcting Memory Functional Block Diagram



		BIT POSITION		ADDRESS
		B0-B6	B7-B16	
CHIP ENABLE LINE	S0	U93-99	910-919	0-7777
	S1	U83-89	810-819	10,000-17,777
	S2	U73-79	710-719	20,000-27,777
	S3	U63-69	610-619	30,000-37,777
	S4	U43-49	410-419	40,000-47,777
	S5	U33-39	310-319	50,000-57,777
	S6	U23-29	210-219	60,000-67,777
	S7	U13-19	110-119	70,000-77,777

TABLE 1. MEMORY ARRAY CHIP CONFIGURATION

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Figure 4-34. SMA PCA Functional Block Diagram

= 4096, the number of bits in each memory chip). A refresh cycle occurs once every 62 usec at 25 degrees C and every 31 usec at 70 degrees C. The period to refresh the entire PCA will therefore require from 2 msec to 4 msec depending on ambient temperature.

Refresh cycles occur between memory operations (read, write) and when the memory is not being accessed by program control. The SMA and FCA PCA's and refresh circuits on the MCL PCA are battery powered and refresh is continued when the system DC power has been set to standby or when ac power is interrupted to the system. Neither memory operations nor refresh operations interrupt each other, the operation in progress is allowed to complete before the next operation starts.

Figure 4-35 is a functional block diagram of the refresh circuitry. The FRUNCLK signal from the CPU is examined by the Frequency Discriminator to determine if the frequency is within tolerance for refresh circuit operation. FRUNCLK is normally produced internally by the CPU, but for maintenance purposes, the FRUNCLK can be generated from an external source. When FRUNCLK is absent or too slow, the Frequency Discriminator directs the Internal/External Clock Selector to select the free running Refresh Control Oscillator output (approximately 400kHz) as the REFRESH CLOCK. When the FRUNCLK is present and within tolerance, it is selected by the Internal/External Clock Selector as the REFRESH CLOCK.

The rate at which the refresh cycles occur is determined by the thermistor controlled Refresh Rate Oscillator. The frequency range of this oscillator is approximately 16kHz (one refresh cycle every 62.5 usec) to 32kHz (one refresh cycle every 31.2 usec), this corresponds to a 25 degree C to 70 degree C temperature range. The oscillator output is used to clock the Refresh Request FF set, and to increment the Address Counter. The Address Counter is a six-bit counter that counts from 0 to 63 to provide 64 refresh addresses (A10 - A15). With the Refresh Request FF set, and the memory has finished its previous operation, the Memory Busy Latch will be clear and the Memory Free FF sets with the REFRESH CLOCK signal. Under these conditions, the Refresh Override Control circuits enable the Address Multiplexer to pass the A10 to A15 address lines to the SMA and FCA PCA's, and the Read/Write Lockout circuit is disabled to prevent a read or write operation from activating the delay line until the refresh is completed. The Read/Write Clock Gate is also disabled, blocking the READ CLK and WRITE CLK signals to the SMA and FCA PCA's, to exclude all timing signals except REFRESH CLOCK.

The Refresh Start Controller is enabled by the Refresh Override Control circuits to send the REFRESH CLOCK to the SMA PCA. The Refresh Start Controller also sets the Memory Busy Latch which clears the Memory Free FF and prevents another refresh cycle from starting until the current cycle is finished. Activating the Delay Line Driver by the Refresh Start Controller starts a pulse down the delay line to develop the timing signals that reset the circuits previously activated to start the refresh cycle, and to release gates blocked out for the refresh cycle.

During a read or write operation, the SMA Chip Select Line Decoder decodes the address bits (AD01 thru AD03) if the board is selected by AR0 and AR1, to enable one of eight chip select lines where the memory is located. During a refresh operation, the REFRESH CLOCK enables all eight Chip Select Decoder Gates forcing their outputs high. REFRESH CLOCK also provides an ENABLE to the Chip Select Enable Gates whose outputs are inverted by the Chip Select Drivers and enables each of the eight chip enable lines S0 thru S7 simultaneously. Every memory chip is thus enabled and decodes the output of the Address Drivers. Internally in the memory chip, the combination of the chip enable and address cause 64 locations in every memory chip to be refreshed.

During a refresh operation, the FCA PCA Upper and Lower 16K CE Drivers are enabled by the RC (Refresh Clock). Every memory chip is thus enabled and decodes the output of the Address Drivers. Internally in the memory chip, the combination of the chip enable and address cause 64 locations in every memory chip to be refreshed.

4-117. MEMORY OPERATIONS

The following discussion of memory operations are referenced to the MCU (Module Control Unit) functional block diagram, figure 4-36. The four possible memory operations are READ (10), Write (01), RW1 (Read Write one's 11) and NOP (No Operation 00). The MCU, located on the MCL PCA, controls communications between the CTL bus and the memory array.

4-118. READ. A read operation (MOP 10) will output 16 data bits and a parity bit from the addressed location to the requesting module via the CTL bus. The requesting module checks the READY line to see if the module is ready to receive information, the READY line will be high if the module is free. The requesting module then pulls its ENABLE line low, disabling all lower priority modules. The requesting module will also pull the READY line down for one clock cycle to prevent any other module from accessing memory. The requesting module then initiates a read operation by sending over the CTL bus the address to be read and the following codes on their respective lines; TO, FROM, MOP (memory operation), MCUD PRTY (address parity), and SYS PRTY (control signal parity).

When the TO code compares with the Memory Module Number, the TO Comparator outputs a COMPARE signal and the following events occur:

- The requesting module pulls the memory module's READY line low to inform any other requesting module that memory is busy.
- The Address Latch FF is set and locks the address on the MCUD lines into the Address Register.
- The Data Address Parity Checker is enabled and checks the address bits with the MCUD PRTY bit for odd parity. If a parity error is detected, the NMCUD PE line is enabled and the Error Latch is reset forcing a NOP code out of the MOP Decoder.
- The System Parity Checker is enabled and checks the nine control bits (TO, FROM, MOP) with the SYS PRTY bit for odd parity. A parity error will be indicated on the NSYS PE line and also reset the Error Latch to force a NOP out of the MOP Decoder.
- The NREADY FF sets, enabling the Memory Module Number to pull the READY line low, signifying a memory operation is in progress for that module. The READY line pulled low corresponds to the module number.

NOTE

Because one MCL PCA services two memory modules, the READY lines for modules 0 and 1 are simultaneously pulled low if either module is active. Similarly, the READY lines for modules 2 and 3 are simultaneously pulled low if either module is active.

The combination of the NREADY FF and the NW' signal from the MOP Decoder start the timing sequence and data transfer from memory to the CTL bus. The Read Delay Start and Read Clock FF's are set, sending a pulse down the tapped delay line to produce the required D times. As long as the refresh circuits do not have priority, NREAD CLOCK is passed to the SMA PCA to enable memory for the read function. NR/W Control output normally remains in the read state (low). During the time the Clock Counter counts four MCU CLK signals, the memory will have completed the read operation and data will be presented on the MCUD lines if the bus is not busy, the read cycle is extended until the bus is free and then data is presented on the MCUD lines.

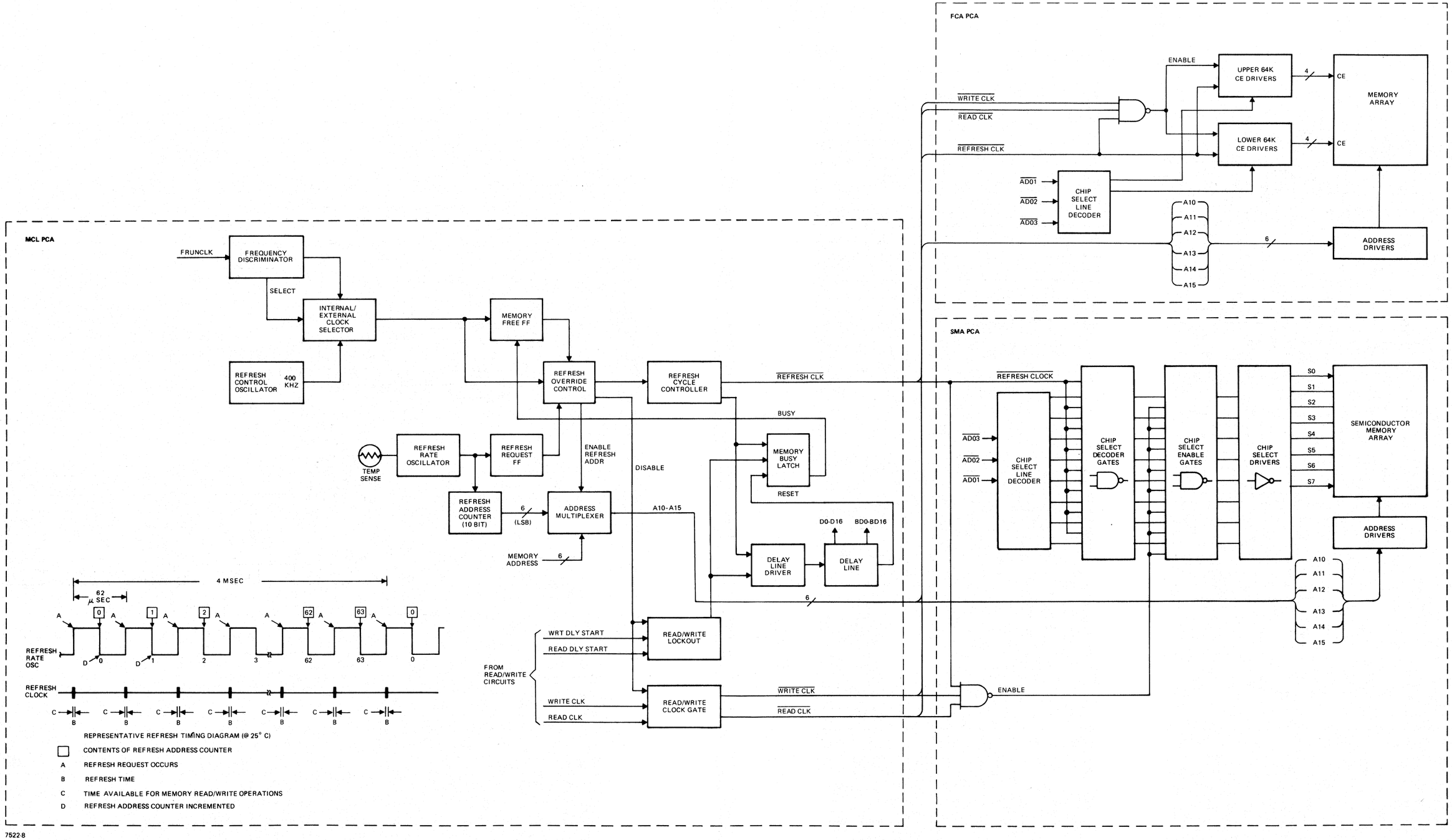

Figure 4-35. Refresh Circuit Functional Block Diagram

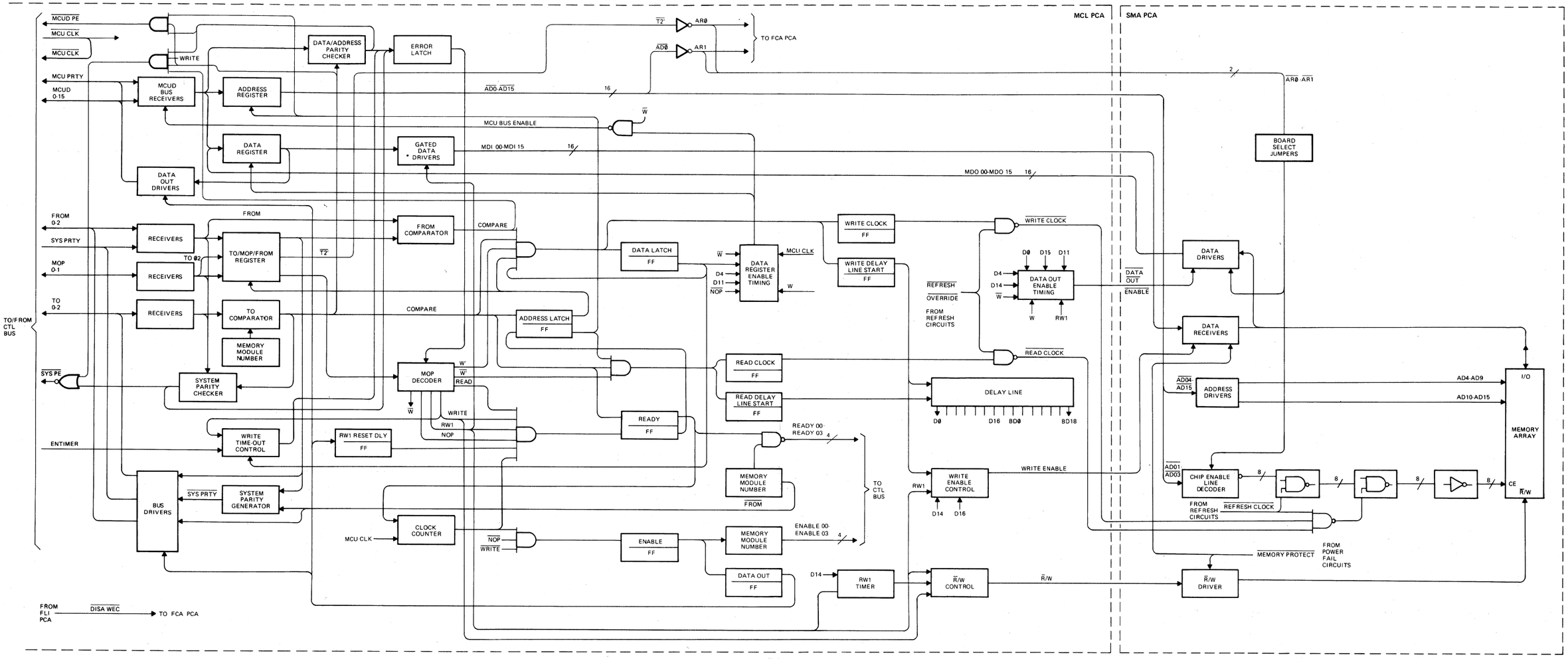

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Figure 4-36. Memory MCU Functional Block Diagram

Address bits NAD01 thru NAD03 from the Address Register are decoded by the Chip Enable Line Decoder and activate one of eight CE lines in the Memory Array. The Chip Enable Line Decoder is enabled by bit zero of the address word (AR1) and the bank register bit translated as NT2' (AR0) provided the board select jumpers are properly inserted. A partial enable is also sent to the Data Drivers. Address bits NAD4 thru NAD15 from the Address Drivers are presented to the Memory Array, and, in conjunction with the enabled CE line, the memory address is accessed. Providing a power fail condition has not occurred, NMEMORY PROTECT allows the NR/W Driver to route the read signal to the array. The read operation then occurs in the array and the output data is sent by the Data Drivers, enabled by the Data Out Timing Enable circuit between times D4 and D14 to the Data Register. Data is trapped in the Data Register by the Data Register Timing circuit between times D4 and D11 of a read operation. To prevent any destruction of memory output data by the signals present on the MCUD lines, the MCUD Bus Receivers are inhibited by removing the MCU BUS ENABLE signal during the same time interval data is trapped in the Data Register.

The Clock Counter counts MCU CLK signals while the memory performs the read operation. When the first clock is counted, the Ready FF resets if this module has priority for the CTL bus and the bus is available. The module is not busy, and the Enable FF sets enabling modules of lower priority. The Data Out FF sets on the next MCU CLK enabling the Data Out Drivers to output on the MCUD lines the contents of the Data Register. The Data Out FF also enables the Bus Drivers to place on the CTL bus the TO, FROM, SYS PRTY signals and a NOP function. Parity is generated using the TO, FROM, and MOP codes. The module originally requesting the read operation will be receiving the data and is designated on the TO lines. The memory module that received the read request (TO) sends the data as the FROM module on the bus.

4-119. WRITE. A write operation (MOP 01) will load 16 data bits and a check bit into a given address location. Two transmissions to the memory module are required to initiate a write operation. On the first transmission, the requesting module sends over the CTL bus the address to be written into and the following codes on their respective lines: TO, FROM, MOP, MCU PRTY, and SYS PRTY. This is identical to the transmission received by the MCU for a read operation, and is referred to as the addressing phase. The second transmission required for a write operation is the data phase, containing the TO, FROM, MOP code, MCU PRTY, SYS PRTY, and the data to be written into memory.

For a write operation, the events that occur during the addressing phase are nearly identical to those of the read operation. The TO code compares with the Memory Module Number storing the address, checking parity, setting the NReady FF, starting the Clock Counter, decoding the memory enable and address lines, etc. The following discussion explains the actions unique to a write operation.

When the MOP Decoder decodes the WRITE signal, the NR/W Control circuit switches to the write mode, and the Write Time-Out Control is activated when the ENTIMER signal is present. With the Write Time-Out Control activated, the data must be received within 6.4 msec or the Error Latch will be reset and force a NOP signal out of the MOP Decoder, suspending the write operation.

When the second transmission to the MCU occurs, the TO code is compared with the original TO code, the FROM code is compared with the FROM code of the address phase and a NOP (00) is sent on the MOP lines. A compare signal will be produced by the FROM comparator that sets the Data Latch, Write Delay Start, and Write Clock FFs. Write Time-Out Control is de-energized by the Data Latch FF, suspending the 6.4 msec time restriction. The Data Register Enable Timing circuit is enabled by the MCU CLK locking the write data in the Data Register. Memory therefore has applied to it the address and the write signal. The Data Receivers, enabled by the Write Enable Control circuit, present to memory the data trapped in the Data Register that is to be written into memory.

During the data phase, the control signals (TO, FROM, MOP) are checked for parity error and if an error exists, the SYS PE signal goes to a logis 0. A NOP is not produced for a system parity error, and parity is checked on the data. A parity error on data is indicated on the NSYS PE line.

4-120. RW1. The RW1 (Read Write ones) memory operation (MOP 11) reads and transfers the data from the addressed location, and writes all ones back into the same location. The function is similar to the read operation, however, more time is required to complete the operation and the Delay Line is effectively extended by the RW1 Timer.

A decoded RW1 signal from the MOP Decoder starts the normal read operation and transfer of data. At D14 time of the Delay Line the RW1 Timer is turned on, switching the condition of the R/NW Control circuit from read to write. Write Enable Control activates the Data Receivers at D16 time to pass all ones as the input to memory because the Gated Data Drivers outputs have been forced to ones by the RW1 signal.

4-121. NOP. A NOP (no operation) is similar to a read operation, however, no data is transferred to the originating module. The NOP (MOP 00) can occur during an address phase when there is a system address parity error.

During a write operation, the MOP code sent with the data is a NOP.

When a system or address parity error occurs during the address phase, the Error Latch resets and forces a NOP out of the MOP Decoder. The Read Delay Start and Read Clock FFs are set because the TO Comparator output is true. The Delay Line is therefore activated and the NREAD CLOCK signal is applied to the SMA PCA. However, the output data is not gated to the MCUD lines because the Data Out Drivers are not enabled. The set input of the Enable FF is disabled by NNOP preventing the Data Out FF from setting, preventing the enable from being applied to the Data Out Drivers.

4-122. FAULT CORRECTION AND ERROR LOGGING.

Fault correction and error logging occurs on the MCL PCA. Generation and storage of the check bits and generation of the error code occurs on the FCA PCA. The FCA PCA effectively operates in parallel with the SMA PCA. See figure 4-35 which shows the interface between the MCL, SMA, and FCA PCA's. With the exception of NDISWEC, and MDO lines, all remaining signals from the MCL MCU Timing and Control Circuits shown in figure 4-36 are also applied to the SMA PCA. Whenever a read, write, or refresh operation occurs on the SMA PCA, the same operation occurs on the FCA PCA. The same address is accessed on each array PCA, however, the data being read or written is not the same.

4-123. FAULT CORRECTION. During a Write operation, the same sixteen data bits being written into the SMA PCA are presented to the FCA PCA Check Bit/Error Code Generator where the CHECK BITS (A-E) are formed on the data word. CHECK BIT A is sent to the SMA PCA where it is stored in the 17th bit position of the data word. The remaining four check bits (B,C,D,E) are stored in the FCA PCA Memory Array.

The FCA Memory Array physically contains eight rows of 4K RAM chips, with 16 chips in a row. Each row is divided into four groups, corresponding to the four possible SMA PCA's that could exist in a memory module. Therefore, each FCA PCA contains 128K-4 bit storage locations. Figure 4-37 shows the relationship between the FCA chips, SMA PCA's, and check bits.

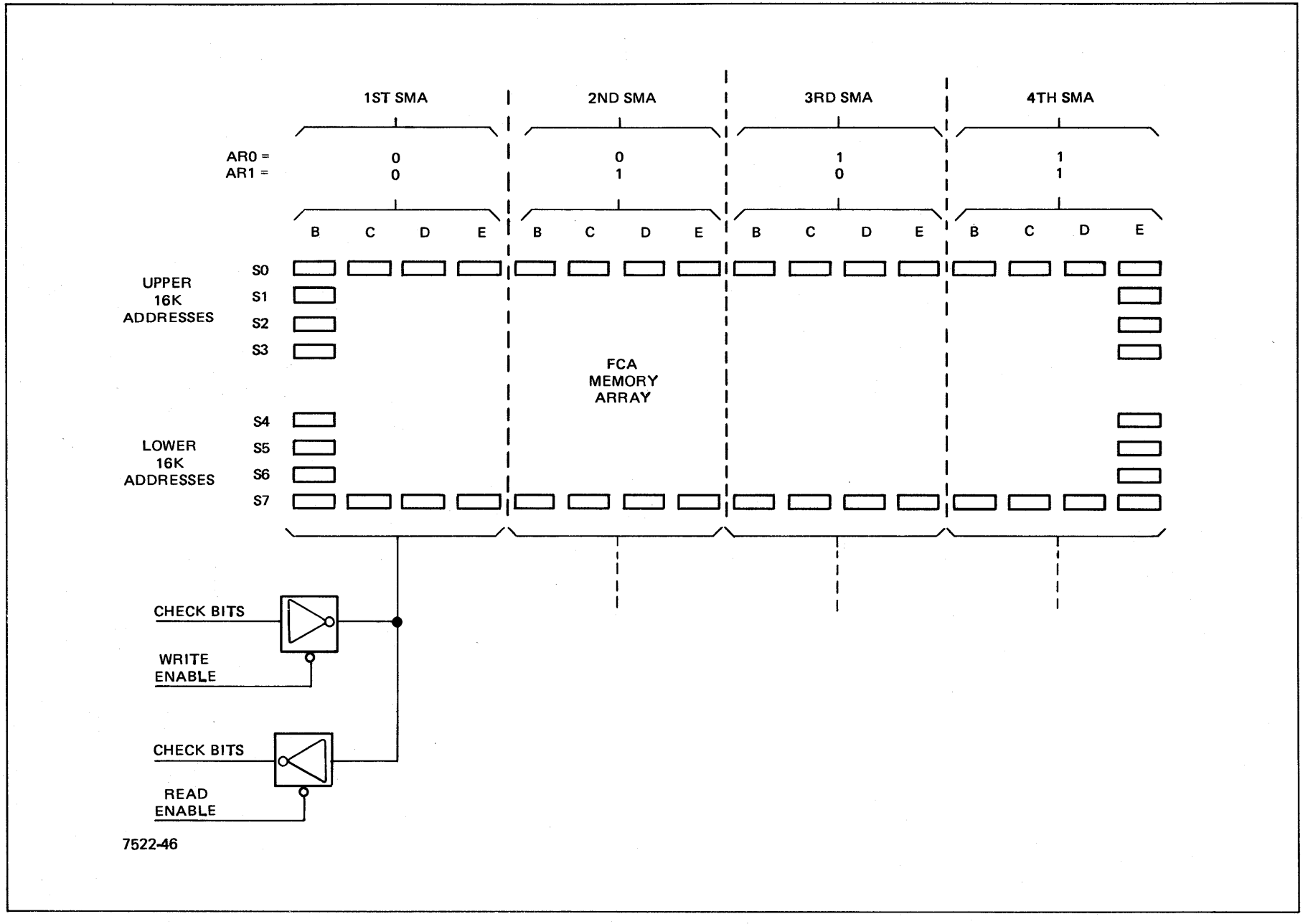


Figure 4-37. FCA PCA Memory Array

The Read/Write Selector on the FCA PCA, figure 4-38, selects one of four drivers for reading or writing, depending on the bit configuration of the AR0 and AR1 signals. AR0 and AR1 are formed in the MCL Timing and Control Circuits and actually relate to the most significant bit of the address word (AR1) and the bank register bit (AR0). This combination selects which sector of the FCA Memory Array the check bits are written into or read from.

During a Read or RW1 operation, the 16 bits read from the SMA PCA are stored in the MCL Data Register. The same 16 bit data word is also presented to the FCA Check Bit/Error Code Generator. In addition, the 17th bit (CHECK BIT A) read from the SMA PCA is directly presented to the Check Bit/Error Code Generator, not via the MCL Data Register. Simultanously, the four CHECK BITS (B,C,D,E) are read from the same address in the FCA Memory Array and sent to the Check Bit/Error Code Generator. A 5-bit Error Code is then generated from the 21 bits presented to the generator. This ERROR CODE will be equal to zero if none of the 21 bits has changed, compared to the original bits when the word was written and check bits were generated.

The ERROR CODE is then latched into the MCL Error Code Register and presented to the Error Detector where the ERROR CODE is checked to see if it is equal to zero (00000). When it is equal to zero, the Error Corrector does not modify the data bits from the MCL Data Register, and the data is sent to the CTL Bus.

When the Error Detector checks the ERROR CODE and it is not equal to zero, the Error Corrector will complement the bit in error which was determined by the ERROR CODE, and then send the data to the CTL Bus. Only one error bit can be corrected in a data word. An ERROR signal is produced by the Error Detector that activates the Read/Write Control Circuit and causes a "1" to be written into the Error Logging Array. Errors are only logged during Read and RW1 operations.

The address where the flag ("1") is written is determined by a 10-bit address that consists of the 5-bit ERROR CODE, three bits of the address read (AD01-AD03) and the signals AR0 and AR1. The fact that an error occurred is represented by the "1" stored in the Error Logging Array. The actual bits of the address where that "1" is stored represents information about the error.

The Error Logging Array is read by the FLI PCA only during Refresh time so as not to interfere or extend the normal memory cycle.

4-124. FAULT LOGGING INTERFACE PCA

The FLI PCA under software control reads from and writes into the MCL Error Logging Array (ELA). The FLI PCA only operates with direct I/O commands received on the IOP Bus. All communication between the MCL and FLI PCA's occurs on the Fault Logging Interface Bus. See figure 4-39.

Although the FLI PCA reads and writes the ELA, all logging information must pass through the FLI I/O Logging Array. Data is copied from the ELA into the I/O Logging Array, and then the I/O Logging Array is read onto the IOP Bus. To write into the ELA, the I/O Logging Array is written into from the IOP Bus, then the I/O Logging Array is read into the ELA. Writing into the ELA is normally done with all zeros to clear the entry in the ELA.

Direct I/O instructions are decoded by the Command Decoder to the Timing Control Circuits and set the R/NW Control Circuit to the appropriate condition for reading or writing. To perform a read of the MCL ELA, that particular MCL PCA must be selected since the FLI PCA can service two independent MCL PCA's. A starting address is loaded into the FLI Address Counter and is applied to the Address Comparator and I/O Logging Array. The other input to the Address Comparator is the address of the

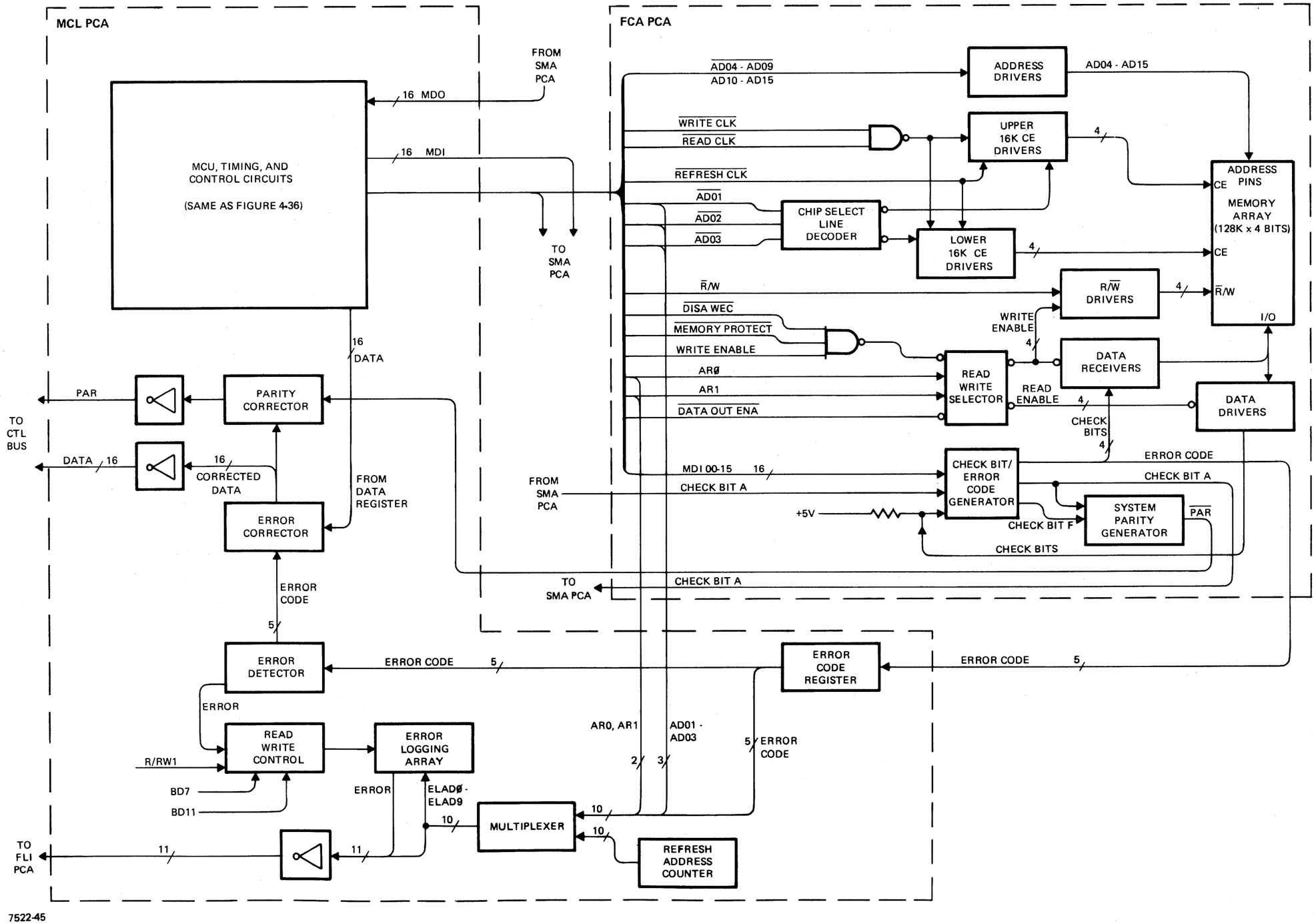
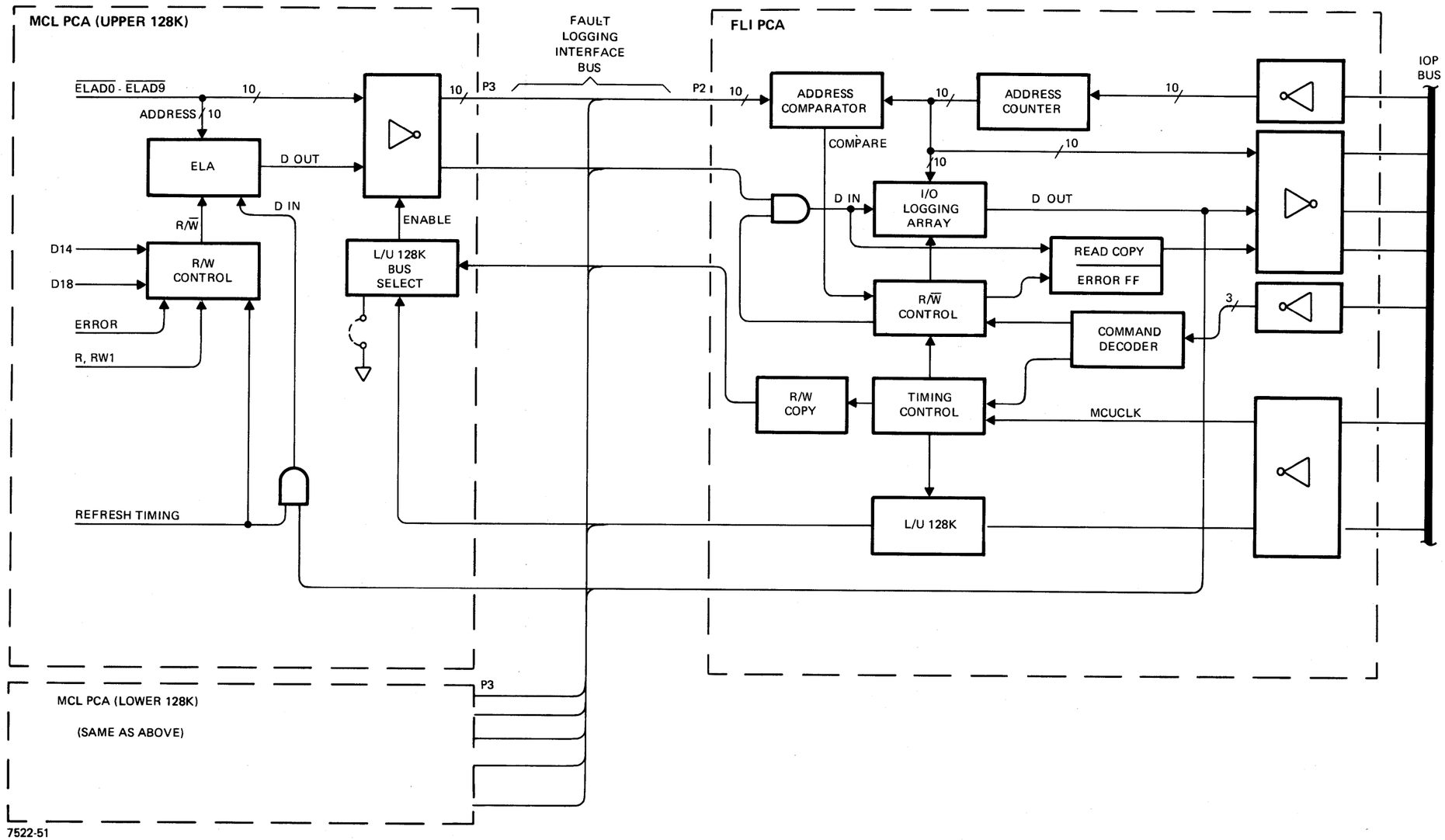


Figure 4-38. Fault Correction and Error Logging Functional Block Diagram



4-39. FLI PCA Functional Block Diagram

ELA refresh counter. When the two addresses compare, the content of the ELA is read into the I/O Logging Array. The Address Counter increments and the addresses stay in sync with each other.

To write into the ELA, the MCL must be selected, timing initiated, and addresses compared. The output of the I/O Logging Array is then routed as the input to the ELA.

At regular intervals the software commands the FLI to read the ELA. If a "1" has been logged in the ELA, it is recorded in the I/O Logging Array and sets the Read Copy Error FF. Setting this flip-flop indicates that an error has been logged in the ELA. The software can then interrogate the I/O Logging Array to find the address where the "1" was copied. Software then examines the address bits to determine the type of error and chip location. A disc file is then updated with this information for analysis at a later time.

4-125. POWER FAIL

The MCL PCA contains the power fail circuits that guarantee the CPU enough time to execute a power fail routine before memory becomes protected when power failures occur, and also contains the circuits that clear out the ELA when power is first applied to the system. The power fail circuits and timing waveforms are shown in figure 4-40. All the power fail circuits are operated on battery backup voltages.

From the time a power failure is sensed until the loss of usable power, the CPU executes a power fail routine. The power fail circuits allow 3.5 msec ± 20% for the CPU to complete the routine. After the 3.5 msec interval, the power fail circuits generate the NMEM PROTECT signal that disables the read and write clocks to the SMA and FCA PCA's. Erroneous data could be entered into memory if the clocks were not disabled because TTL circuits oscillate when power to them decays.

Power failures may be considered as short duration (transient line conditions) or long duration (loss of ac line power). A line transient causes the HP 30310A Power Supply to produce the NPFW signal that fires the 3.5 MSEC One-Shot. The CPU power fail routine is executed and completed before the one-shot times out. After 3.5 msec, the 300 MSEC One-Shot starts timing and memory is protected. When the 300 MSEC One-Shot times out, the protect signal is removed if the NPFW signal has gone high and PON is high.

When ac line power is removed from the system, NPFW again activates the 3.5 MSEC One-Shot, and then the 300 MSEC One-Shot starts timing out protecting memory. Since ac line power was lost, PON will go low and keep memory protected until power is restored. When power is returned to the system, NPFW goes high and 0.6 sec later, PON and NMEM PROTECT go high removing the protect from memory. The contents of the ELA will remain unchanged provided the length of the power failure did not allow the battery backup to discharge below a useful level.

When ac power is first applied to the system or when power is applied after a power failure where the battery was allowed to discharge below a useful level, the ELA will be cleared to all zero's. The + 5VB Threshold Detector monitors the + 5VB line, and when this voltage reaches + 4.1V, the ELA will be reset. If the ELA were not cleared when power is applied, it would contain meaningless random data.

NOTE

Whenever a PCA in the memory module is changed, the ELA contents is reset when the LOWER 128K MEMORY or UPPER 128K MEMORY DC POWER switch is placed ON.

NOTE

A complete description on care of batteries is contained in Appendix D of the Signal and Power Distribution Manual (03000-90021).

4-126. PCA JUMPERS

Refer to paragraphs 4-66 through 4-72 for details of jumper installations and switch positions on the SMA, FCA, FLI and MCL PCA's.

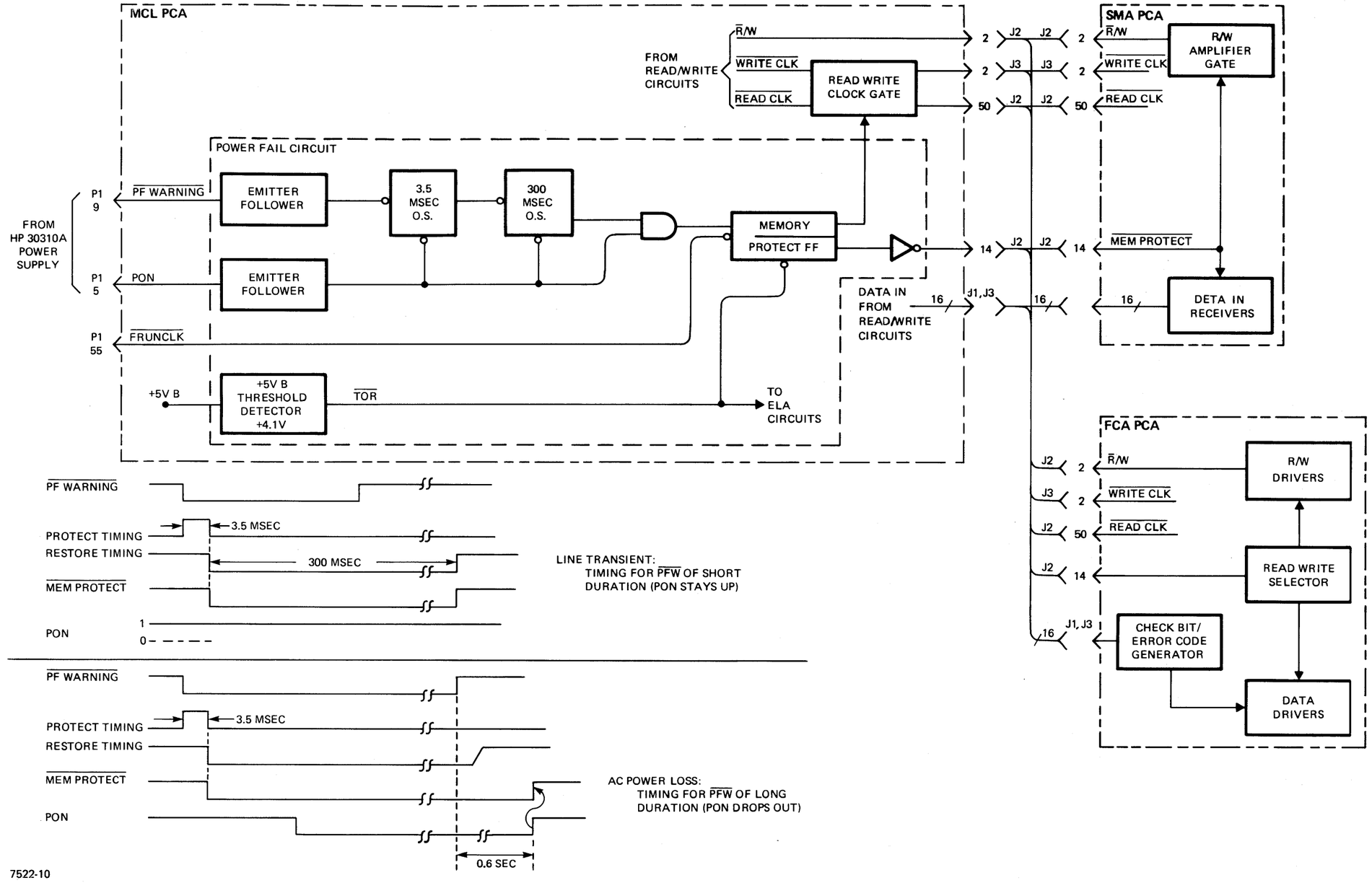


Figure 4-40. Power Fail Circuit Functional Block Diagram

REPLACEABLE PARTS

SECTION V

5-1. INTRODUCTION

This section contains a list of replaceable items in the HP 3000 Computer System.

5-2. REPLACEABLE PARTS

Table 5-1 is a list of replaceable assemblies contained in the HP 3000 Computer System. When additional assemblies are listed for a major item, field personnel have the option of replacing the major item or any of the subassemblies listed for that item.

Table 5-1 lists only the system processor assemblies. For repair and replacement information for subsystems, controllers, and I/O interface PCA's, refer to the applicable service manual.

Table 5-1. Replaceable Assemblies

Description	Part Number
Extended Instruction Set PCA	30012-60001
Read Only Memory PCA	30003-60001
Skip and Special Field PCA	30003-60002
Arithmetic and Logic Unit PCA	30003-60003
R-Bus PCA	30003-60004
S-Bus PCA	30003-60005
Current Instruction Register PCA	30003-60006
Module Control Unit	30003-60007
Input Output Processor	30003-60008
Multiplexer Channel PCA	30036-60001
Port Controller PCA	30030-60016
Selector Channel Register PCA	30030-60018
Selector Channel Sequencer PCA	30030-60011
Selector Channel Control PCA	30030-60003
Memory Control and Logging PCA	30007-60002
Fault Correction Array PCA	30009-60001
Fault Logging Interface PCA	30009-60002
Semiconductor Memory Array PCA	30008-60002
HP 30310A Power Supply	30310-60024
A1 Pre-regulator Control PCA	30310-60002
A2 Inverter Driver PCA	30310-60003
A3 20 Volt Supply PCA	30310-60004
A4 Current Limit PCA	30310-60005
A5 Voltage Protect PCA	30310-60006
A6 5V/30V Rectifier Assembly	30310-60011
A7 Inverter PCA	30310-60007
A8 Deck Assembly	30310-60014
A8A1 Capacitor PCA	30310-60008
A9 Pre-regulator Assembly	30310-60010
A10 Connector Panel Assembly	30310-60012
A12 Front Panel Assembly	30310-60013
A12A1 Test Point PCA	30310-60001
A13 Output Crowbar Assembly	30310-60015
HP 30311A Power Supply	30311A
Control Board Assembly	30311-60003
Mother Board Assembly	30311-60002
Heat Sink Assembly	30311-60005
Battery Pack	30311-60006

Table 5-1. Replaceable Assemblies (Continued)

DESCRIPTION	PART NUMBER
HP 30312A Power Supply	30312A
Model 62605M Power Supply	62605M
Interface Board Assembly	30312-60002
System Control Panel	30003-60012
Control Panel Board	30003-60011
System Clock/Console Interface PCA	30031-60001

Table 5-2. Replaceable Cables

(to be supplied)

Table 5-3. Miscellaneous Items

DESCRIPTION	PART NUMBER
Diagnostic Hardware Assembly	30049-60003
SCMB	30033-60001
HP 30354A Maintenance Panel	30354-60001
	30354-60002
Maintenance Panel Interface PCA	30354-60003
Card cage fan	3160-0257

5-3. CARD CAGES

Two models of card cages are used in the HP 3000 System, HP 30002B and HP 30002C.

5-4. HP 30002B CARD CAGE

When a fan fails in this card cage, both fans must be replaced. This requires removal and replacement of the card cage from the equipment bay, a time consuming procedure that can take as long as four hours.

5-5. HP 30002C CARD CAGE

When a fan fails in this card cage, only the defective fan needs replacement. The HP 30002C card cage need not be removed from the equipment bay. The fans are secured to a removable panel and fan replacement takes about fifteen minutes.

5-6. HP 30002B CARD CAGE — FAN REPLACEMENT

The following procedure is used to replace a defective fan in a HP 30002B card cage. Figure 5-1 is used with this procedure.

1. Have the console operator terminate all jobs and sessions. Have the console operator back-up the system files since the system must be shut-down.

2. Shut-down the system.

   a. Set the SYSTEM DC POWER switch OFF.

   b. Set the LOWER and UPPER 128K MEMORY ON/STANDBY switches to STANDBY.

   c. Set the POWER switch on each HP 30312 power supply in the system to the OFF position.

   d. Set the PCM MAIN SYSTEM POWER circuit breaker OFF.

   e. Set the Computer Mainframe Power Panel circuit breaker OFF.

3. Remove all PCA's from the card cage.

4. Remove the card cage door.

5. Disconnect the fan power plug from the service strip inside the equipment bay.

5. Disconnect the fan power plug from the service strip inside the equipment bay.

6. Label the connection point of each cable and wire that connects to the card cage, then disconnect these cables and wires.

7. Disconnect the ground cable and ground plate from the right rear side of the card cage. There are two cables and two ground plates if the card cage is not the top or bottom card cage in the equipment bay.

8. Remove the angle brace from the left rear of the card cage that connects to the adjacent card cage.

9. Remove the four screws from the front of the card cage that secures it to the equipment bay and remove the card cage from the cabinet.

10. Remove the four screws securing the fan plate to the side of the card cage.

11. Disconnect the power plug from each fan and remove the four self tapping screws that secure each fan to the cage frame.

12. Replace the two fans (3160-0257) and secure them to the cage frame with the original hardware. Make sure the fans are mounted so the direction of air flow is into the card cage and that the fan is positioned with the power receptacle facing the bottom of the fan plate. Reconnect the power plugs to the fans.

13. Install the card cage into the equipment bay and secure it with the original hardware removed in step 9.

14. Reconnect the ground plate and ground cable to the card cage.

15. Replace the angle brace at the left rear of the card cage.

16. Reconnect all cables and wires, identified in step 7, to the card cage.

17. Connect the fan power plug to the service strip.

18. Replace all PCA's removed from the card cage.

19. Replace and secure the card cage door.

20. Power-up the system.

    a. Set the Computer Mainframe Power Panel circuit breaker ON.

    b. Set the PCM MAIN SYSTEM POWER circuit breaker ON. Check that the new fans installed are operating properly.

    c. Set the POWER switch on each HP 30312 power supply in the system to the ON position.

    d. Set the LOWER and UPPER 128K MEMORY ON/STANDBY switch to ON.

    e. Set the SYSTEM DC POWER switch ON.

21. Ask the console operator to reload the system.

5-7. HP 30002C CARD CAGE — FAN REPLACEMENT

The following procedure is used to replace a defective fan in a HP 30002C card cage. Figure 5-2 is used with this procedure.

1. Have the console operator terminate all jobs and sessions. Have the console operator back-up the system files since the system must be shut-down.

2. Shut-down the system.

    a. Set the SYSTEM DC POWER switch to OFF.

    b. Set the LOWER and UPPER 128K MEMORY ON/STANDBY switches to STANDBY.

    c. Set the POWER switch on each HP 30312 power supply in the system to the OFF position.

    d. Set the PCM MAIN SYSTEM POWER circuit breaker OFF.

    e. Set the Computer Mainframe Power Panel circuit breaker OFF.

3. Remove the card cage door and the hardware that secures the door hinges to the cabinet frame.

4. Disconnect the fan power plug from the service strip inside the equipment bay.

5. Remove the cable tie that secures the power cord to the upper corner of the card cage inside the equipment bay.

6. Remove the screw and cap washer that secures the fan chassis to the card cage.

7. Pull the fan chassis and the fan power cable out of the card cage.

8. Disconnect the power plug from the defective fan and remove the four screws that secure the fan to the chassis.

9. Replace the defective fan and secure it to the fan chassis with the original hardware. Make sure the fan is mounted so the direction of air flow is into the card cage and that the fan is positioned with the power receptacle facing the bottom of the fan chassis. Reconnect the power plug to the fan.

10. Insert the fan power cable and fan chassis into the card cable. The fan chassis should rest on the plastic guides located on the bottom left side and be guided by the single plastic guide located on the upper left edge of the card cage.

CAUTION

When inserting the fan chassis into the card cage, make certain that none of the fan wires are pinched or otherwise damaged.

11. Hold the fan chassis to the left of the card cage and secure it to the card cage with the screw and cap washer removed in step 6.

12. Replace the two card cage door hinges and the card cage door.

13. Secure the power cord to the card cage with a new cable tie.

14. Insert the fan power plug into the service strip.

15. Power-up the system.

    a. Set the Computer Mainframe Power Panel circuit breaker ON.

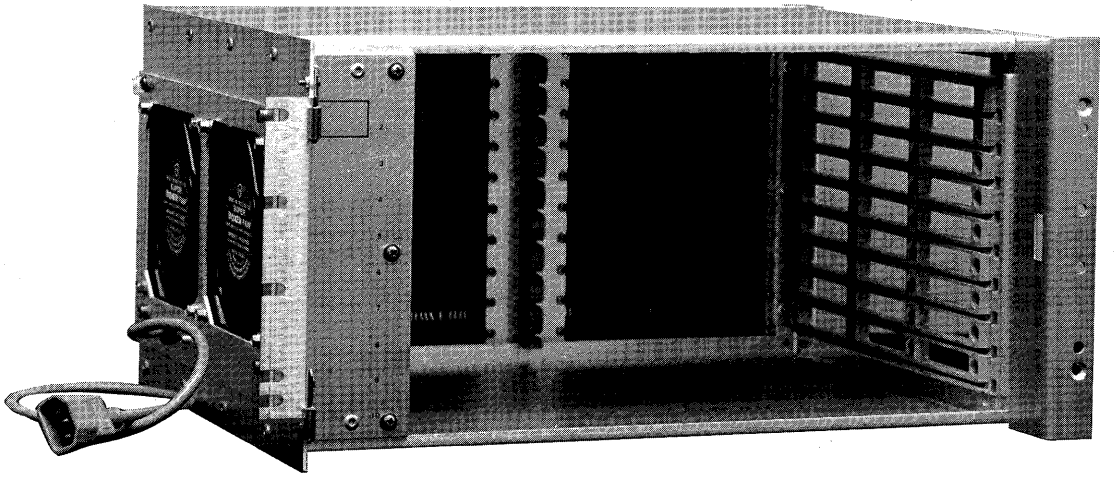
    b. Set the PCM MAIN SYSTEM POWER circuit breaker ON. Check that the new fan just installed is operating properly.

    c. Set the POWER switch on each HP 30312 power supply in the system to the ON position.

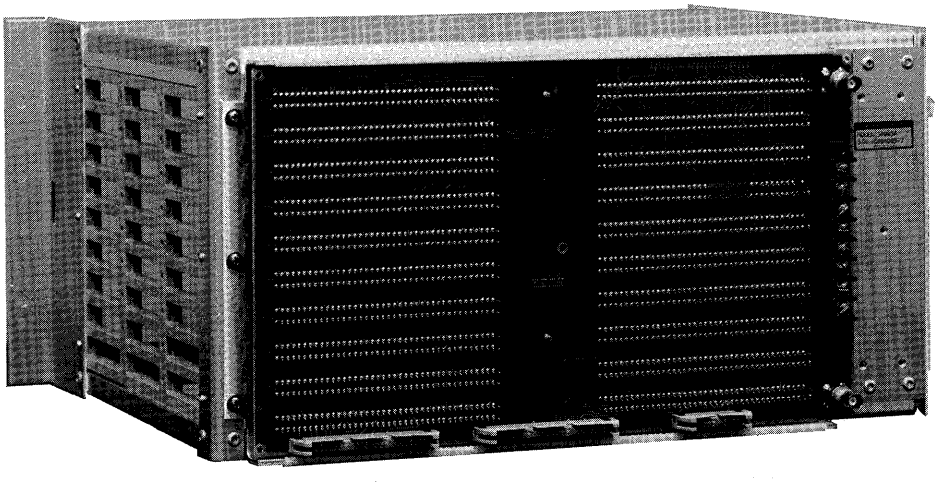
    d. Set the LOWER and UPPER 128K MEMORY ON/STANDBY switches to ON.

    e. Set the SYSTEM DC POWER switch ON.

16. Ask the console operator to reload the system.

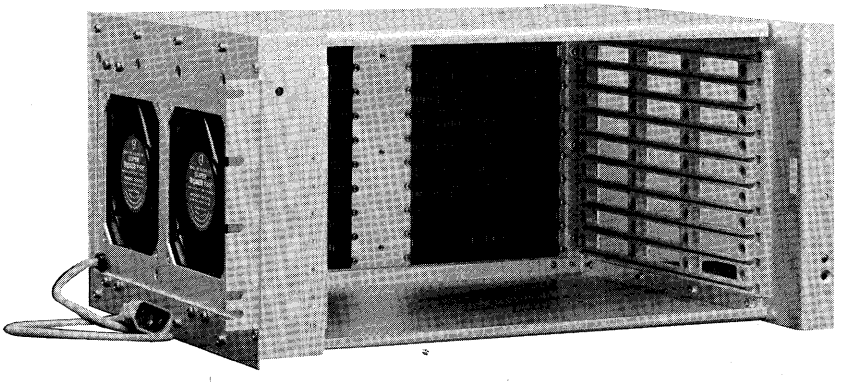


(Front View)

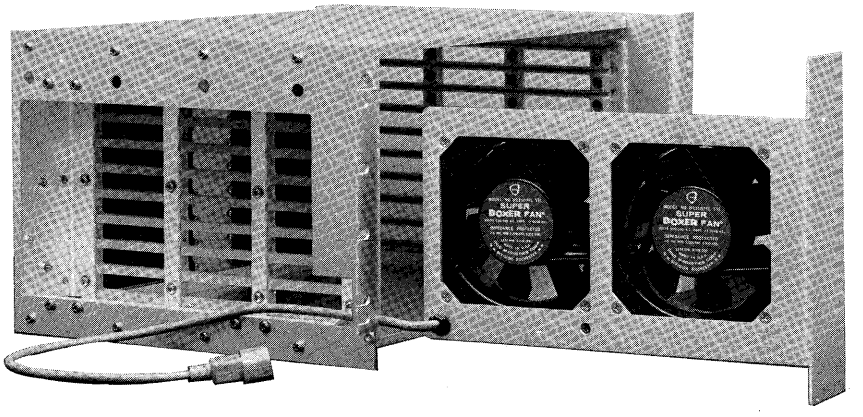


(Rear View)

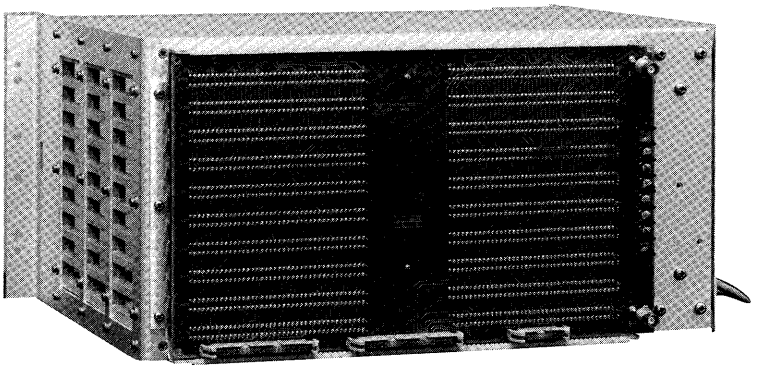
Figure 5-1. HP 30002B Card Cage



(Front View)



(Front View) Fans Removed



(Rear View)

Figure 5-2. HP 30002C Card Cage

A-1 MICRODIAGNOSTICS

Stored in the microcode are diagnostics to test the CPU registers, memory, and the I/O channels. The diagnostics are accessed by a cold load procedure from the System Control Panel.

If an error occurs when running a diagnostic, the maintenance panel can be connected to the system to facilitate stepping through the microcode, or, the stand-alone diagnostic in the Manual of Diagnostics can be run to determine the malfunction.

A-2. CPU REGISTER TEST

This diagnostic tests the various CPU registers. Normal running time for the diagnostic is approximately one second. To run the test, perform the following steps:

a. Set the SYSTEM SWITCH REGISTER to %000201.

b. Press the ENABLE and LOAD switches.

c. The program runs continuously until the HALT switch is pressed or until an error occurs.

Normally, when an error occurs, the computer halts with the RUN light off and a coded register number in the CIR display. The coded number can be interpreted by referring to table A-1.

Occasionally, an error causes the computer to halt with the RUN light on and all lights in the CIR display off. If this happens, press HALT and then use table A-1 to interpret the resulting coded register number.

NOTE

If the SYSTEM SWITCH REGISTER bit 8 is clear (0), all memory is initialized with HALT %10 instructions (%030370) prior to executing the cold load. Because untested registers must be used while writing the instructions, it is possible for test results to display misleading symptoms. If bit 8 is set (1), no initialization occurs.

Table A-1. CPU Register Codes

CIR	REGISTER	CIR	REGISTER
00	SP1 (1) SEE NOTE	20	OPND (5)
01	PL (1)	21	DL (2)
02	Z (1)	22	SP2 (2)
03	X (1)	23	PB (2)
04	RD (R BUS) (1)	24	PCLK (2)
05	RC (R BUS) (1)	25	RD (R BUS) (2)
06	RB (R BUS))1)	26	RC (S BUS) (2)
07	RA (R BUS) (1)	27	RB (S BUS) (2)
10	SP0 (1)	30	RA (S BUS) (2)
11	CRTL (2)	31	CTRH (2)
12	P (2)	32	ABS (BANK) (3)
13	Q (2)	33	PB (BANK) (3)
14	DB (2)	34	DB (BANK) (3)
15	SM (2)	35	S (BANK) (3)
16	STA (4)		
17	SP3 (2)		

(1) Located on R-Bus PCA
(2) Located on S-Bus PCA
(3) Located on Skip and Special Field PCA
(4) Located on Skip and Special Field PCA and S-Bus PCA
(5) Located on Current Instruction Register PCA

NOTE

SP1 is the first register tested and the problem may not necessarily be in SP1 but somewhere previous in the data path (Store logic, Shifter, ALU, etc.).

A-3. MEMORY TEST

A memory configuration test is available from the microprogram for testing memory. Memory configuration test diagnostic time is approximately ten seconds.

To run the memory diagnostics, perform the following steps:

a. Set the SYSTEM SWITCH REGISTER to %000200.

b. Press the ENABLE and LOAD switches.

c. Program runs until an error occurs.

When an error occurs the program pauses and the CIR contains the error data (lamp on = error bit). By pressing the RUN/HALT switch, the CIR then contains the address information shown in table A-2. The test should be continued so all memory is tested before any repairs are made. The test is terminated by pressing the HALT switch.

Table A-2. CIR Address Information

CIR BIT	FUNCTION
0:3	Address bits 0:3
6,7	Bank number
10:14	CPX1 register bits 2:6
10	(2) Illegal address
11	(3) CPU timer
12	(4) System Parity Error
13	(5) Address Parity Error
14	(6) Data Parity Error
15	Address bit 15

A-4. I/O TEST

A Test Input/Output (TIO) instruction is executed on each I/O device number (3 through %177) in sequence. Only those device numbers with a device connected will respond; empty device numbers are skipped. To run the I/O test, perform the following steps:

NOTE

If the HP 30354A Maintenance Panel is connected to the system, the TIMERS switch must be set to ENABLE.

a. Set the SYSTEM SWITCH REGISTER to %000202.

b. Press the ENABLE and LOAD switches. (When an existing device number is encountered, the program pauses with the device number in CIR. The RUN lamp will be illuminated.)

c. Press the RUN/HALT switch. CIR then displays the device status, the RUN lamp will be extinguished.

d. Press the RUN/HALT switch. Steps b and c are repeated until all device numbers have been interrogated. Diagnostic is finished when CIR displays %000200. The RUN indicator will be extinguished.

SYSTEM POWER SUPPLIES

APPENDIX B

This appendix presents detailed information about system power supply units. Additional information about power distribution is given in the Engineering Diagrams Manual.

B-1. INTRODUCTION

An HP 3000 Series II Computer System with up to 128K words of memory has three power supplies:

- HP 30310A Power Supply
- HP 30311A Power Supply
- HP 30312A Power Supply

HP 3000 Series II Computer Systems containing more than 128K words of memory have one additional HP 30310A and one additional HP 30311A.

The power supplies require preventive maintenance, voltage adjustments, and an occasional troubleshooting. The following items are required to perform these tasks:

- A vacuum cleaner for removing dust.
- One digital voltmeter with at least a 4-digit readout and a minimum input resistance of 10 megohms. The device should have full-scale ranges of 9.999 and 99.99 and accuracy of better than one percent.
- One oscilloscope.
- One multimeter.
- One autotransformer.

All power supplies are non-repairable items maintained on an exchange basis. Only open fuses should be replaced in the field.

B-2. HP 30310A POWER SUPPLY

This power supply provides +20, +15, +5, -20, -15, and -5 volt DC outputs. Main assemblies within the power supply are:

A1	Preregulator Control PCA	30310-60002
A2	Inverter Driver PCA	30310-60003
A3	20-Volt Supply PCA	30310-60004

A4	Current Limit PCA	30310-60005
A5	Voltage Protect PCA	30310-60006
A6	5V/30V Rectifier Assembly	30310-60011
A7	Inverter PCA	30310-60007
A8	Deck Assembly	30310-60014
A9	Preregulator Assembly	30310-60010
A10	Connector Panel Assembly	30310-60012
A12	Front Panel Assembly	30310-60013
A12A1	Test Point PCA	30310-60001
A13	Output Crowbar Assembly	30310-60015

The power supply is a modular unit mounted in the cabinet by means of hinges. The unit swings out on the hinges for service and is removable from the hinges for replacement.

WARNING

Two men are required to remove the HP 30310A Power Supply from its mounting hinge. This power supply weighs 50 pounds (22.7 kilograms).

A POWER switch which is on the front panel of the power supply (see figure B-6) turns the unit on. (Note however, that a DC Enable (DCE) signal is required at terminal 1 of terminal board TB3 to enable the output voltages.) Circuits within the power supply provide normal operation and failure warning signals to the CPU. The status and control signal connections at terminal board TB3 and the output DC voltages at TB1 are cabled to their destinations at the factory. The output voltages and the Power On (PON) signal are accessible on the front panel for measurement. In addition, an indicator lamp is mounted on the front panel near the test points to monitor the +5 volt output.

Refer to table B-1 for HP 30310A Power Supply specifications.

B-3. THEORY OF OPERATION

The theory of operation is divided into two sections. A general description at the block diagram level is presented first, followed by a functional description at the simplified schematic level.

The power supply converts a 208/240-volt, single-phase, 50- or 60-Hertz power source to regulated DC supply voltages for system operation. An HP 30312A Power Supply augments the +5 volt output of this supply.

A POWER switch, mounted on the front panel of the supply, controls the AC input to this unit. The DC output voltages can be controlled by the SYSTEM switch which is mounted on the DC Control Panel (see figure B-6). The output voltages provide status signals for protection of software (information stored in CPU memory). Computer system hardware is protected by circuits that sense overvoltage, overcurrent, or overtemperature conditions. Circuits within the power supply are protected by various overvoltage and overtemperature circuits, current limit circuits, and fuses. The general concept in the power supply design is to immediately turn the power off when an overvoltage condition occurs. For undervoltage or over temperature conditions, a short delay is generated before the power supply is turned off. This delay permits the CPU to store data which, in turn, makes power on and restart much easier.

Table B-1. HP 30310A Power Supply Specifications

POWER REQUIREMENTS	
LINE VOLTAGE:	208V ac ±10%, 3-phase, 5A, or 230V to 240V ac ±10%, 1-phase, 5A
LINE FREQUENCY:	47.5 to 66 Hertz
POWER CONSUMPTION:	830 watts (1000 volt-amperes), maximum
POWER CABLE (CONNECTED TO AC LINE)	
LENGTH:	5 feet (152.4 centimeters)
CONNECTOR:	CEE 22 Type VI (for ac line) CEE 22 Type V (for power supply)
DC SUPPLY VOLTAGES AND CURRENTS	
+20V ±1%, 7.5A*	
+15V ±5%, 2.5A	
+5V ±5%, 55.0A	
-5V ±5%, 6.0A	
-15V ±5%, 2.5A	
-20V ±1%, 1.0A*	
ENVIRONMENTAL LIMITS	
AMBIENT TEMPERATURE RANGE:	Operating: 0° to 55°C (32° to 131°F) Non-operating: -40° to 75°C (-40° to 167°F)
RELATIVE HUMIDITY:	50 to 95% at 25°C to 40°C (77° to 104°F) without condensation
ALTITUDE:	Operating: 15,000 feet (4572 meters) Non-operating: 25,000 feet (7620 meters)
VENTILATION	
AIR FLOW:	100 cubic feet (2.8317 cubic meters) per minute
HEAT DISSIPATION:	2550 BTU's (642.549 kilocalories) per hour, maximum
WEIGHT AND DIMENSIONS (See figure 1-2.)	
WEIGHT:	50 pounds (22.7 kilograms)
HEIGHT:	8.875 inches (225.4 millimeters)
WIDTH:	19.0 inches (482.6 millimeters)
DEPTH:	10.22 inches (259.5 millimeters)
REPLACEABLE FUSES	
F1	5A, 250 VAC
F2	1A, 250 VAC

*Temperature compensation resistor provides negative regulation of -0.26%/°C.

B-4. BLOCK DIAGRAM DESCRIPTION. Figure B-1 is a block diagram of the power supply. The following paragraphs describe the operation of each of the blocks shown in the figure.

B-5 Primary Power Circuit. The AC line voltage enters the power supply through a connector and passes through a 5-ampere fuse and radio frequency interference (RFI) filter to the POWER switch. The POWER switch is located on the front panel of the power supply. With the POWER switch in the ON position, line voltage is applied to the preregulator, cooling fan, and a step-down transformer. The fan and transformer circuit are protected by a 1-ampere fuse.

B-6. Preregulator A9. The preregulator contains a silicon controlled rectifier (SCR) bridge that converts the AC line voltage to a unidirectional, pulsed voltage. The pulsating voltage is filtered to become the regulated +130 volt rail voltage. The rail voltage is applied to the inverters and is used as a basis for all DC output voltages. The SCR bridge is controlled by the preregulator control circuit through an isolating transformer.

B-7. Preregulator Control A1. The stepped-down line voltage is applied to full-wave rectifiers which supply unregulated +22, -22, and +9 volts DC for the bias voltage regulagors. The regulators provide internal power supply bias voltages. The preregulator control circuit uses the AC line frequency, -30 volt DC feedback, and status of the current limiter and voltage protect circuits. The preregulator control circuit supplies trigger pulses to the preregulator that determine the "on" time of the SCR bridge circuit to maintain proper control of the 130 volt DC rail.

B-8. Inverter A7. The inverter circuits convert the 130 volt DC output of the preregulator to a square-wave AC voltage which is transformer-coupled to the rectifiers. The transformer coupling provides isolation for stages following the inverter. The 800-Hertz operating frequency of the inverter is determined by the inverter driver. There are two inverter circuits within the inverter that operate 90 degrees out of phase with each other. Each circuit is fused for 3 amperes.

B-9. Inverter Driver A2. The inverter driver generates an 800-Hertz, two-phase clock which is timed to develop phase 1 and phase 2 drive signals. The two inverter driver circuits are transformer-coupled to the two inverter circuits.

B-10. Full-Wave Rectifiers and Filters. The transformer-coupled inverter output is rectified and filtered to provide DC outputs of +15, +5, -5, and -15 volts DC. Additionally, +30 and -30 volts DC are supplied to the +20 and -20 volt regulators.

An independent -30 volt output is fed back to the preregulator control circuit to maintain output voltage regulation.

B-11. 20-Volt Regulators. The 20-volt regulators consist of a +20 and a -20 volt regulator. The +20 volt regulator is a switching regulator which converts the +30 volt rectifier output to a regulated +20 volt DC output. The -20 volt regulator is a series regulator which converts the -30 volt rectifier output to a regulated -20 volt DC output. The +20 and -20 volts DC are used by a power supply for the semi-conductor memory. An analog signal from the memory power supply is used by the +20 volt regulator to control the output voltage. The -20 volt regulator is designed to track the +20 volt regulator so that the two outputs are equal and opposite in polarity.

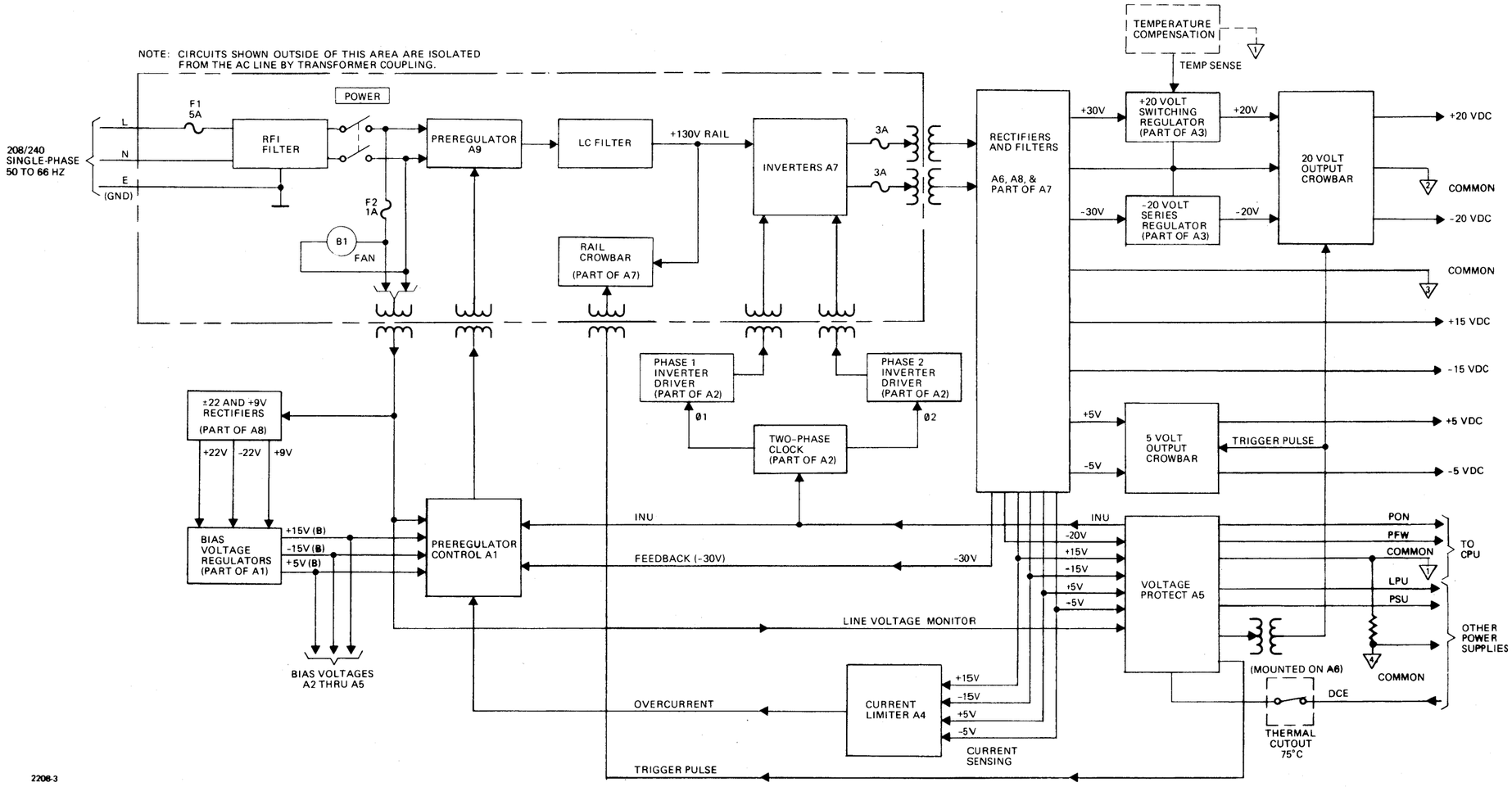


Figure B-1. HP 30310A Power Supply Block Diagram

B-12. Current Limiter A4. The current limiter circuits monitor the individual DC voltage drops across the output filter chokes for the +15, +5, –5, and –15 volt outputs. Any excessive current drawn from these outputs results in the immediate generation of an OVERCURRENT signal. The OVERCURRENT signal is used by the preregulator control circuit to limit the preregulator output voltage to protect the power supply.

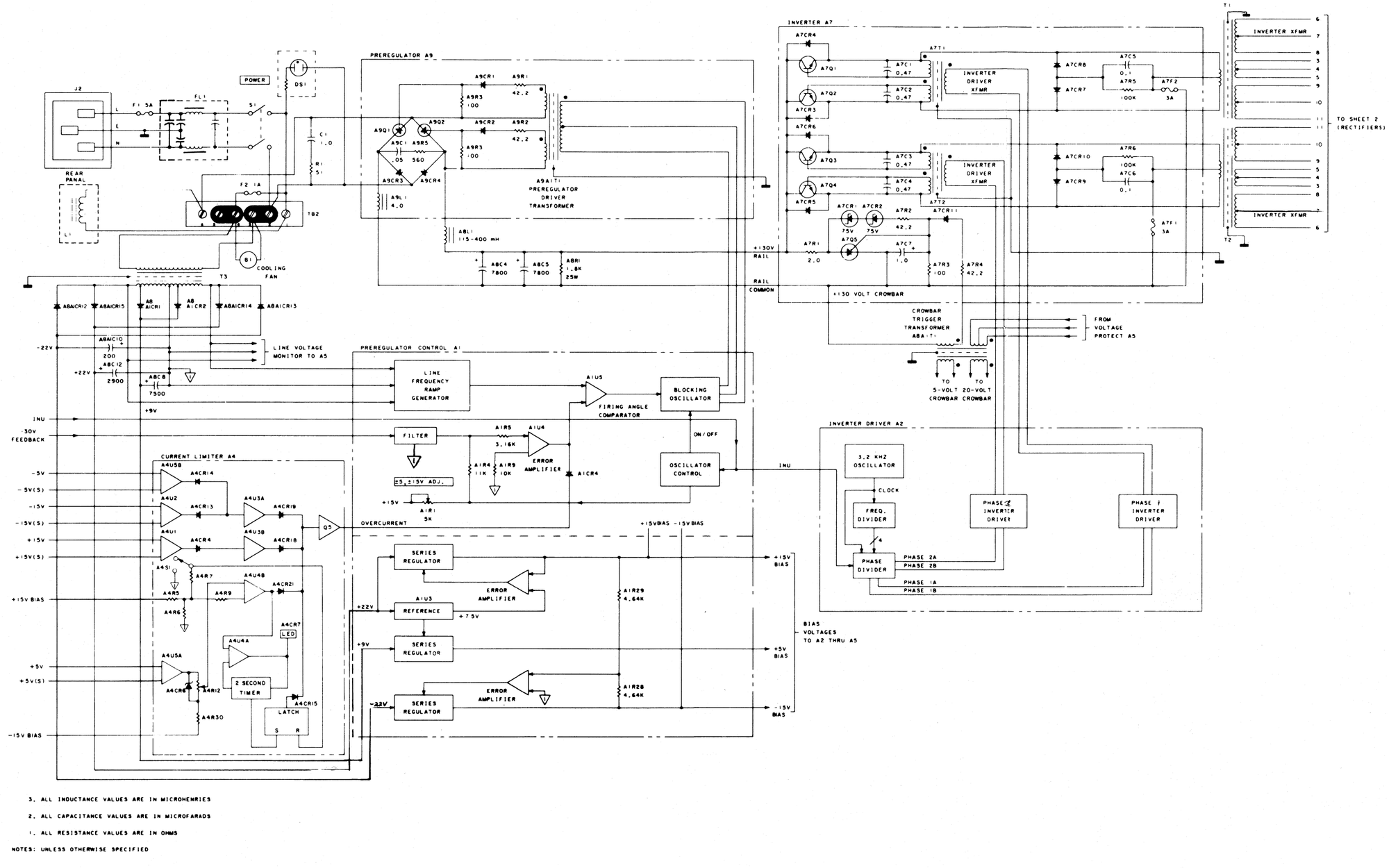
B-13. Voltage Protection and Control A5. The voltage protection and control circuits contain overvoltage sensing circuits to protect the Computer System hardware and undervoltage sensing circuits to protect system software. The overvoltage comparator circuits monitor all DC output voltages, with the exception of the +20 volt output. Whan an overvoltage condition is sensed, an overvoltage latch is set. Transformer-coupled crowbar trigger pulses are generated, which crowbar the +130V RAIL, +20, –20, +5, and –5 volt DC outputs. Also, when the latch is set, the Inverter Up (INU) goes low and disables the inverters and preregulator. Circuits also monitor the internal thermal cutout switch (overtemperature sense) and the external DC Enable (DCE) signal. If the internal power supply temperature exceeds its fixed limit or an external DCE signal is removed, the Power Fail Warning (PFW) signal goes low after a 70 ms delay. After another delay of 12 ms, the INU signal goes low, turning the preregulator and inverter off. Since the output voltages go down, the Power Supply On (PON) signal goes low. (See following paragraph for further description of undervoltage.) The SYSTEM switch controls the power supply outputs with the DCE signal. This signal appears as an overtemperature condition to the power supply and initiates the overtemperature sequence.

The undervoltage comparator circuits monitor all DC output voltages with the exception of the +20 volt output. If any of these DC output voltages drop below specified limits, the PON signal goes low. An excessive current overload causes the output DC voltages to drop. The undervoltage sequence is initiated due to this condition. Circuits also monitor the input AC line voltage. If it drops below a preset limit, the PFW signal goes low and after a minimum delay of 5 ms, the PON signal also goes low. When the DC output voltages and AC line voltage are above the specified low limits, and the thermal switch is closed, a high PON signal is provided for the system within 0.6 second.

The undervoltage sensing circuits also provide power supply control signals for use when multiple supplies are "control paralleled" in a Computer System. These signals are Power Supply Up (PSU), Line Power Up (LPU), and control common ▽4▽ . PSU indicates that the DC output voltages are above specified limits. LPU indicates that the AC line voltage is above a specified limit, the thermal switch is closed and DCE enabled. When the PSU, LPU, DCE, and control common ▽4▽ signals of multiple supplies are wired in parallel, any supply can provide the PON and PFW signals to the system, and all multiple supply outputs can be controlled by a single DCE signal.

B-14. FUNCTIONAL DESCRIPTION. As shown in the functional diagram (Figure B-2), the AC input line is connected through fuse F1, RFI filter FL1, POWER switch S1, and terminal board TB2 to the phase-controlled, bridge rectifier preregulator. The preregulator bridge circuit contains two diodes and two SCRs that rectify and control the preregulator DC output voltage. The SCRs are turned on by trigger pulses from the preregulator control circuit and turned off when the AC input voltage passes through zero. This action sends a portion of the AC input voltage (during each half-cycle) into the LC filter to provide the controlled 130 volt rail voltage.

The crowbar circuit across the 130 volt rail is driven by the crowbar trigger transformer, which is initiated by the overvoltage latch circuit in voltage protect PCA A5. If an overvoltage condition is sensed by A5, trigger pulses are produced to fire the crowbar. The crowbar shorts the 130 volt rail



3. ALL INDUCTANCE VALUES ARE IN MICROHENRIES
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS
1. ALL RESISTANCE VALUES ARE IN OHMS

NOTES: UNLESS OTHERWISE SPECIFIED

Figure B-2. HP 30310A Power Supply Functional Block Diagram (Sheet 1 of 2)

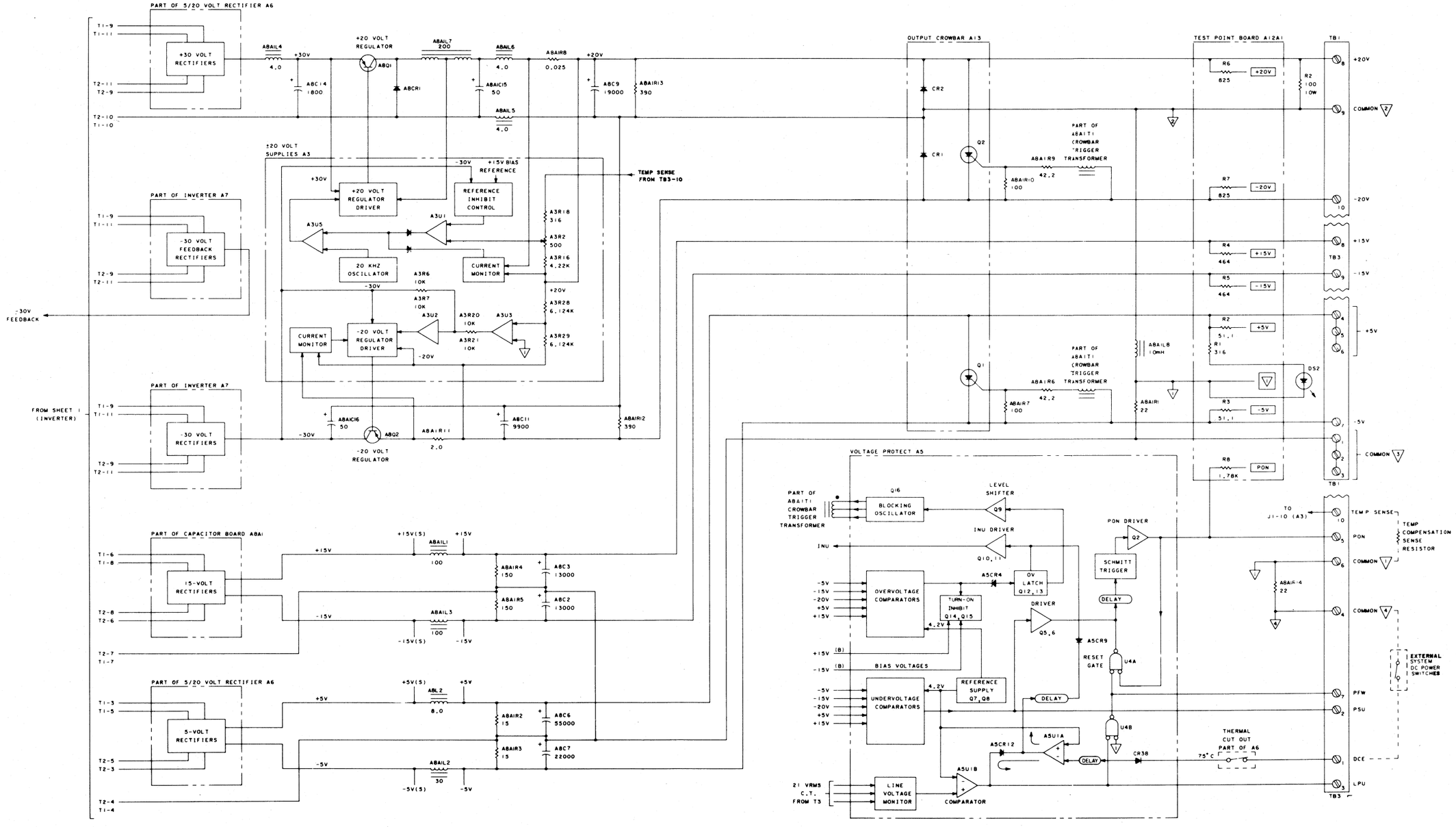


Figure B-2. HP 30310A Power Supply Functional Block Diagram (Sheet 2 of 2)

(through a low resistance) to protect the load circuit. The crowbar circuit is also triggered directly (by zener diodes) whenever the rail voltage exceeds +150 volts.

The AC input is also connected through fuse F2 and terminal board TB2 to transformer T3 and cooling fan B1. The secondary winding of T3 supplies voltages to a group of rectifiers which provide the unregulated +22, -22, and +9 volt inputs to the bias voltage regulators in PCA A1. The regulators furnish the +15, -15, and +5 volt internal bias voltages for PCAs A1 through A5. The secondary of T3 also drives the line frequency ramp generator in PCA A1. The output of this circuit is a sawtooth signal whose period is determined by the frequency of the AC line voltage. The sawtooth signal is applied to one input of the firing angle comparator. The other input to the comparator is connected to the output of error amplifier A1U4. The error amplifier monitors the -30 volt feedback voltage which is proportional to the inverter output transformers flux. The firing angle comparator determines the starting point of the blocking oscillator pulse train. The blocking oscillator provides the preregulator SCR trigger pulses. If the line voltage of -30 volt feedback voltage decreases, the blocking oscillator starting point occurs sooner, which increases the "on" time of the preregulator SCRs. In this manner, the preregulator is phase-controlled to compensate for variations in line voltage or DC voltage while it maintains a closely-controlled, -30 volt secondary voltage.

The 130-volt rail voltage is connected to the two inverter circuits. Each of the circuits consists of two transistor switches that are controlled by transformer-coupled square-waves from inverter driver A2. Switching action develops AC square-waves at the inverter transformer primaries which are coupled to the rectifier circuits to supply the DC output voltages. Fuses A7F1 and A7F2 protect the inverter transistors from short circuit loads.

The 3200-Hertz inverter driver clock signal is divided to obtain two different 800-Hertz phases (phase 1 and phase 2) that are 90 degrees apart. Therefore, one inverter driver and inverter circuit operates 90 degrees out of phase from the other. This results in AC square-waves from the inverters which overlap. When the inverter transformer outputs are combined in the full-wave rectifiers, low-ripple DC outputs are obtained. This permits the use of smaller output filter components.

The +30 and -30 volt rectified outputs are used as supply voltages by the +20 and -20 volt series regulators. The additional regulation is required for the 20-volt supplies because the load has large fluctuations in current and requires a high degree of regulation. The 20-volt supplies are temperature controlled by external temperature sensing to provide optimum voltage. The two different types of supplies are described in the following paragraphs.

The +20 volt supply with transistor A8Q1 comprise a switching-type series regulator, with the output voltage determined by the duty cycle of A8Q1. The duty cycle is controlled by a feedback signal from the regulator output, connected through a resistive divider to one input of error amplifier A3U1. This input is also connected to the temperature sensing resistor from the memory power supply. The other input to the error amplifier is derived from the +15 volt bias. The error amplifier provides a DC error signal to one input of comparator A3U5. The other input to the comparator is from a 20k Hertz oscillator, which provides a triangle-wave signal. The comparator output is a series of rectangular pulses whose duty cycle is determined by the amplitude of the error signal. The pulses are supplied to the regulator driver which controls the duty cycle of switching transistor A8Q1 and thereby regulates the +20 volt output. If the +20 volt load current is excessive, a current monitor circuit takes over the comparator, which inhibits the output voltage from making further change in the regulator driver duty cycle, protecting A8Q1.

The –20 volt supply and transistor A8Q2 comprise a series-type regulator, with the output voltage determined by +20 volt output. Divider A3R28 and A3R29, and comparator A3U3 function as an error signal generator and detector which causes the –20 volt output to equal and track the +20 volt output. The error signal level is shifted by A3R7 and A3R21 and applied to A3U2. The output of amplifier A3U2 is at the proper level to control the driver, which directly controls the current through A8Q2. If the +20 and –20 volt outputs are not equal and opposite in polarity, error amplifier A3U3 provides an error signal to correct the –20 volt output. If the –20 volt load current is excessive, a current monitor circuit holds back the driver to protect A8Q2.

The DC voltage drops across the output filter chokes for +15, +5, –5, and –15 volt outputs are monitored by current limiter PCA A4. Any excessive current (typically 15 percent above rated value) results in the generation of an OVERCURRENT signal, which delays the firing angle comparator circuit in PCA A1. This limits the blocking oscillator, which decreases the preregulator output voltage, to protect the power supply. Thus, a current overload is reflected in lowered output voltages on the ±5 and ±15 volt. The +5 volt current limit circuitry has the added capability of an adjustable limit threshold. This circuitry protects external subsystems where overloads greater than 10 amperes may occur which do not exceed the rated capability of the power supply. The overcurrent threshold for the +5 output is set by A4R1. An overcurrent condition must exist for at least 2 seconds to set an overcurrent latch which activates the OVERCURRENT signal. Switch A4S1 and light-emitting diode (led) A4CR7 are used by the operator to set the overcurrent threshold 10 amperes above the operating current level. The switch is also used to reset the latch. Instructions for this adjustment are printed on the power supply cover. Because of the abrupt action of the overcurrent latch, all of the output voltages go to zero, whereas, the ±15 and –5 overcurrent circuits (described at the beginning of the paragraph) are protected by "foldback current limiter" action only. The +20 and –20 volt outputs are individually protected by current monitor circuits in the ±20 volt supply PCA A3.

All supply output voltages, except for the +20 volts, are monitored by overvoltage and undervoltage comparators in voltage protect PCA A5. If an overvoltage condition is sensed, a latch is set via A5CR4. When this occurs, the INU driver is enabled, and the INU signal goes low. With INU low, the blocking oscillator in PCA A1 and the phase divider circuit in A2 are disabled. This action disables the preregulator and inverter, thus protecting the power supply when the crowbars are fired. The latch output is also level-shifted and applied to a blocking oscillator which provides three transformer-coupled crowbar trigger pulse outputs. The trigger pulses fire the 130-volt rail crowbar and both output crowbars: the 130-volt rail, the +20 and –20 volt outputs, and the +5 and –5 volt outputs are shorted. To reset the latch, the power supply must be turned off. A level detector monitors the internal +15 and –15 volt biases and acts as a turn-on inhibit to the overvoltage latch to prevent premature operation of the crowbars any time power is applied.

The Functional Timing Diagram in figure B-3 illustrates turn-on sequencing of the power supply. When the power supply is turned on, the DC output voltages rise until the undervoltage comparators provide an enable signal (PSU) to the PON circuit. Assuming PFW is up, a 0.6 second delay is provided between PSU and PON. A comparator circuit monitors the secondary winding voltage of T3. If the line voltage falls below a preset limit, comparator A5U1B provides a low LPU signal. LPU is connected through a driver (A5U4B) to provide the PFW signal. If PFW should occur before the 0.6 second delay in the PON circuit has elapsed, gate A5U4A resets the PON delay. A high PFW signal has no effect once the PON signal is high. When the DCE signal goes high (open) or an overtemperature condition in A6 is sensed, comparator A5U1A provides a low PFW signal through A5CR12 and A5U4B. LPU goes low at the same time. After a delay of 12 ms, the INU driver is enabled through A5CR9. The INU signal disables the preregulator and inverter. When DCE

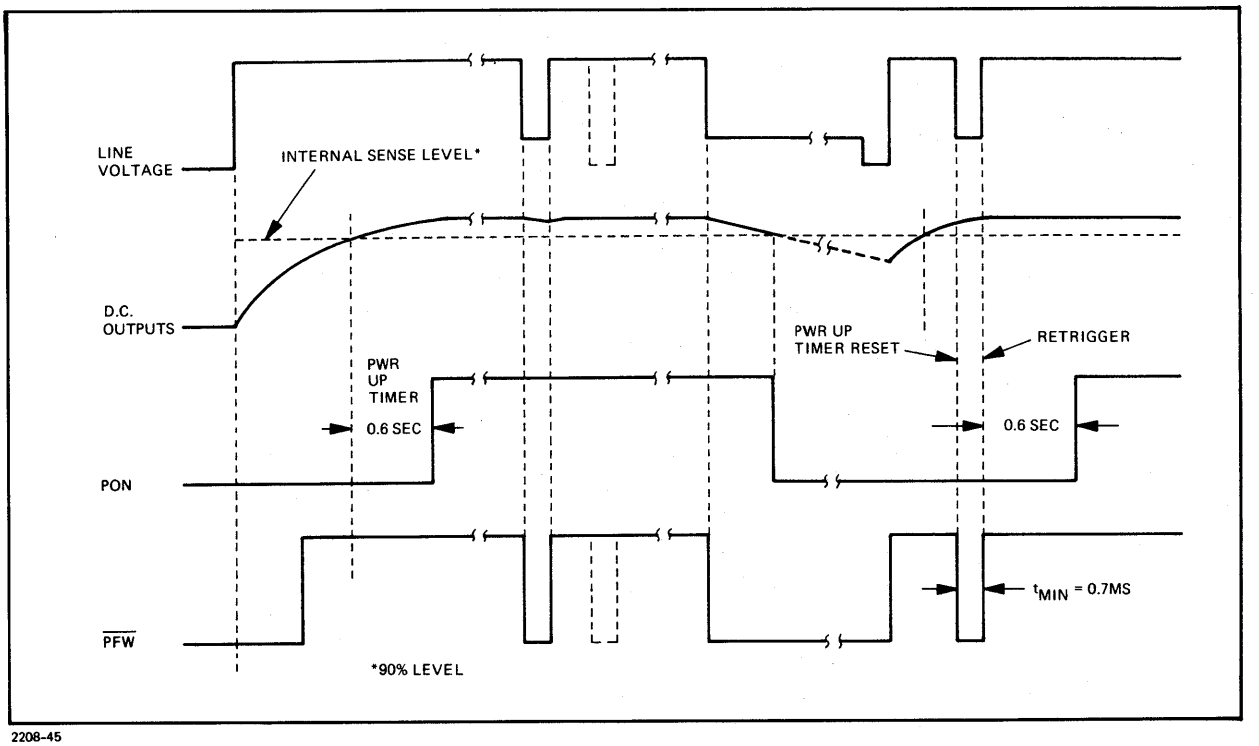


Figure B-3. HP 30310A Functional Timing Diagram

goes low PFW and LPU go high. After a 4 ms delay, INU goes high and the preregulator and inverter are enabled. The DC output voltages rise to their proper values and PSU goes high. After a delay of 0.6 second, PON goes high.

The overvoltage, undervoltage, line voltage, and DCE comparators are referenced to +4.22 volts. The PON and PFW signals are supplied to the CPU. The TEMP SENSE signal is provided by a thermistor in the CPU core. PON, PFW, and TEMP SENSE use common ⑦ as a return. PSU, LPU, and DCE are provided for use with multiple power supplies. They use control common ④ as a return. The +20 and -20 volt outputs use common ② as a return, and the other DC outputs use common ③. All four commons are isolated from each other by resistors or an inductor. The DC output voltages and the PON signal are brought out through isolation resistors to front panel test jacks for maintenance purposes.

B-15. HP 30310A MAINTENANCE

Preventive maintenance is performed at scheduled intervals to prevent or minimize equipment deterioration. Included in the preventive maintenance procedures are voltage tests which check power supply operation.

Adjustments and test procedures are performed when required to isolate trouble and ensure normal operation after a trouble has been corrected.

WARNING

Death or serious injury may occur if the following precautions are not observed.

While the input power is connected, use caution when working inside the power supply. Many exposed conductors carry low DC voltages which are capable of supplying heavy currents if short-circuited, resulting in high heat and the possibility of painful burns. Use caution when manipulating metal tools or probes. A wrist watch, or a metal necklace, bracelet, or ring must not be worn. Avoid dropping tools, screws, or other metal objects onto conductors. Remove power and recover dropped objects at once; if forgotten, damage could result later.

AC powerline voltage and 130 volts DC are exposed when covers are removed. Exercise extreme caution when working in the power supply with covers removed, and never work under this condition unless another person is nearby and within sight. Also, remember that the test equipment is floating with respect to earth ground, so the cases can be at the same line voltage as the point being measured in the power supply. Thus test equipment must be temporarily enclosed and marked dangerous to alert all personnel of unsafe conditions.

If feasible, before performing any work inside the power supply, unplug the AC power cable and wait 3 minutes for filter capacitors to discharge. To prevent explosion resulting from internal heating, always be sure to replace filter capacitors properly with respect to polarity.

B-16. HIGH-VOLTAGE POINTS. The highest AC voltage in the power supply is the AC line voltage (250 volts rms, 350 volts peak). The highest DC voltage in the power supply is 130 volts. The AC line voltage is exposed at the input circuits of the power supply and at filter choke L1. The 130 volts DC is exposed at the preregulator filter circuit and the inverter assembly A7. Additionally, AC voltages of 240 volts peak are exposed at transformers T1 and T2.

B-17. TEST EQUIPMENT GROUND. If the test equipment has a metal case, the negative test lead should not be connected to the case. Also, the negative lead should not be connected to digital voltmeters that have floating (guarded) inputs, to multimeters, nor to power supply chassis. Instead, the test equipment chassis should be connected to the computer system cabinet earth ground through the test equipment power cable. For the oscilloscope, a three-prong to two-prong conversion plug must be used on the power cable. Consequently, the oscilloscope case will "float.' with respect to earth ground. All test equipment should be plugged into the AC power convenience outlets provided in the computer system bay cabinets.

B-18. TEST EQUIPMENT COMMON. All measurements and connections to the power supply must be referenced to the appropriate common circuit. There are four such circuits within the HP 30310A Power Supply: common ▽1▽ , common ▽2▽ , common ▽3▽ , and common ▽4▽ . In subsequent paragraphs, all test and adjustment procedures specify the particular common circuit to be used.

CAUTION

Do not connect test equipment to power supply chassis ground. All common circuits within the power supply "float" with respect to chassis ground. Damage to test equipment or power supply components, and erroneous measurements may result if this caution is ignored.

B-19. PREVENTIVE MAINTENANCE

The following preventive maintenance procedures are performed at monthly or semi-monthly intervals, the frequency depending upon the physical conditions prevailing at a particular site. Routine maintenance once per month is adequate for most power supplies that operate 24 hours per day, seven days per week. The interval can be reduced in accordance with the amount of time the power supply is turned off. The power supply is not removed from the computer to perform preventive maintenance.

Preventive maintenance for the power supply consists of the following:

a. Remove dust.

b. Check PCAs for proper seating.

c. Check cooling fan operation.

d. Check the DC operating voltages at the power supply front panel.

e. Check the AC voltages for ripple at the PCA cage backplane.

To gain access to the power supplies, open the rear door of the CPU cabinet bay. The power supplies are hinge-mounted and may be swung-out by removing the screws that attach the left side of the front panel to the CPU cabinet bay. In this position, the power supply top and bottom covers can be removed for maintenance and test.

If required, use a vacuum cleaner to remove dust and other light debris from the power supply. Loosen encrusted dust with a soft-bristled brush, paying particular attention to heat dissipating areas.

With the top cover of the power supply removed, check all PCAs for proper seating. Adjust where necessary.

Position the POWER switch to ON and check the cooling fan for proper operation. Ensure that no object interferes with fan blade rotation.

Before making voltage checks, the voltmeter must be allowed time to warm up as prescribed by the manufacturer of the instrument. Also, the computer must run, with any type of program, for at least 15 minutes before making the voltage measurement.

Make the voltage checks as described below:

a. Stop the computer program.

b. Measure the six DC voltages listed in table B-2. These voltages are available for cursory measurement only at test jacks mounted on the power supply front panel. (See figure B-6.)

c. Set the oscilloscope for reading AC voltage. On the PCA cage backplane, check each of the six voltages listed in table B-2 for ripple. For each voltage, the indicated ripple should be less than that listed in table B-2.

If any voltage is not within specified limits, make the necessary adjustments as described in paragraphs B-20 through B-23.

Table B-2. DC Output Voltages for the HP 30310A

VOLTAGE TEST POINT	MINIMUM READING	MAXIMUM READING	RIPPLE VOLTAGE TOLERANCE
+20	(See paragraph B-22)		
+15	+14.7	+16.5	0.4 volt peak-to-peak
+5	Set at +5.17		0.3 volt peak-to-peak
-5	-4.5	-5.3	0.3 volt peak-to-peak
-15	-14.7	-16.5	0.4 volt peak-to-peak
-20	(See paragraph B-22)		

B-20. HP 30310A ADJUSTMENTS

Three adjustments should be made to the power supply after it is installed in the computer. These adjustments are accessible through the top cover of the power supply.

B-21. PREREGULATOR ADJUSTMENT. The +15, +5, -15 volt supply outputs are controlled by preregulator adjustment resistor A1R1 (+5, +15V ADJ) on the preregulator control PCA. If one or more of these voltages are not within tolerance when the voltage check is made, the preregulator should be adjusted as described in the following paragraphs.

a. Set the power supply POWER switch to the ON position.

b. Connect the voltmeter between the center conductor of the +5VDC connector and COM on the PCA cage backplane. While observing the voltmeter, adjust the +5, +15V ADJ resistor (A1R1) until the +5 volt output is 5.17 volts as specified in table B-2.

c. Using the same COM as a return, connect the voltmeter, in turn, to the +15V, -5V, and -15V test jacks and verify that each output voltage is within the limits specified in table B-2.

d. Set the power supply POWER switch to OFF and disconnect voltmeter.

B-22. **20-VOLT ADJUSTMENT.** The +20 and -20 volt supply outputs are adjusted by setting resistor A3R2 (+20V ADJ) fully clockwise. These voltages are used by the HP 30311A Power Supply which regulates the voltages by applying an analog signal to the HP 30310A Power Supply's TEMP SENSE input terminal. The value is approximately 17.3 volts when the battery is fully charged and stabilized at room temperature.

B-23. **VOLTAGE PROTECT PCA ADJUSTMENT.** The purpose of this procedure is to check and, if necessary, adjust the +4.22 volt reference supply and line voltage monitor circuits on the A5 voltage protect PCA.

Use the following procedure for adjusting the reference voltage and line voltage monitor circuits.

a. Plug power supply AC line cord into autotransformer.

b. Set POWER switch to ON position. Increase AC input voltage to 208 volts AC.

c. Connect a voltmeter to terminal E1(+) and E2(-,COMMON $\triangledown$1$\triangle$) on A5. Adjust A5R2 until voltmeter reads +4.22 +0.01 volts DC.

d. Connect multimeter between TB3, pin 5(+) and TB3, pin 6(-, COMMON $\triangledown$1$\triangle$). Set multimeter controls to +10 VOLTS DC. This monitors the PON signal.

e. Connect digital voltmeter between TB3, pin 7(+) and TB3, pin 6(-, COMMON $\triangledown$1$\triangle$). This monitors the PFW signal.

f. Both PON and PFW should be at a high level (+4 volts DC, minimum).

g. Slowly reduce the AC input voltage to 160 volts while watching the PFW voltage. The PFW voltage should drop to approximately zero volts when the AC input voltage is between 170 and 160 volts. If the PFW voltage fails to drop to zero as the AC input voltage is reduced below 170 volts, adjust A4R1.

NOTE

Each time PFW goes low, the circuit must be reset by increasing the AC input voltage to 208 volts.

h. Set the AC input voltage to 160 volts. PFW and PON voltages should be low. Increase AC input voltage to 180 volts. PFW should go high, followed by PON after a 1-second maximum delay.

i. Reduce AC input voltage to zero. Set POWER switch to OFF position.

j. Unplug AC line cord from autotransformer. Plug into AC power receptacle.

B-24. TROUBLESHOOTING AN HP 30310A

Troubleshooting in the field is limited to visual checkout, voltage checks, alignment, and power supply replacement if necessary. Proceed as follows:

a. Open rear door of cabinet and observe that the POWER switch is set to ON and that the indicator light is lit. If the switch is ON but the indicator is out, the indicator is bad or AC input power is not available to the power supply. Check the fuse.

b. With the power on, observe that the +5 volt red indicator is lighted. If it is not lighted, check that the DCE signal at terminal of TB3 is low and that the indicator is good.

c. Use the procedure given in paragraph B-19 to check the output voltages of the power supply at the test points furnished on the front panel. If the voltages are not correct, follow the appropriate adjustment procedure from paragraphs B-20 through B-23.

d. Replace the power supply if it remains inoperative or does not respond to alignment.

B-25. HP 30311A POWER SUPPLY

This power supply provides the semiconductor memory of an HP 3000 Computer with backup battery power during the absence of AC input power. The volatile nature of dynamic MOS semiconductor memory requires this backup power to prevent data loss.

The HP 30311A receives its input power from an HP 30310A Power Supply and, in turn, provides backup battery power for 128K words of memory. HP 3000 Computer Systems containing more than 128K words of memory have two HP 30310A Power Supplies and two HP 30311A Power Supplies.

The HP 30311A is a self-contained modular unit. It occupies one-half of a standard 19-inch rack mounting. If only one power supply is mounted in the system, a filler panel is supplied. The filler panel extends the full width of the cabinet and has a 4 by 2-5/8 inch opening used for accessing power supply controls. When an HP 30312A Power Supply is mounted next to this power supply (such as in the I/O bay of a Model 7 system), a half panel covers only the HP 30311A Power Supply.

The principal parts of an HP 30311A Power Supply are:

- A seven-cell sealed lead-acid battery pack (30311-60006)
- A Control PCA (30311-60003)
- A Motherboard PCA (30311-60002)
- A heat sink (30311-60005) for the Motherboard
- Controls and indicators, which are mounted on the front panel, for monitoring the system (refer to figure B-6).
- A test switch, which is mounted on the rear panel, for testing the battery (refer to figure B-6).

An HP 30311A provides voltages of +12.7 VB, +12.0 VB, +5.0 VB, -3.0 VB, and -5.0 VB. The Semiconductor Memory Array PCA (30008-60002) uses all of the voltages except -3.0 VB; the Semiconductor Memory Control PCA (30007-60001) uses only the +5 VB output.

Refer to table B-3 for HP 30311A Power Supply specifications.

B-26. THEORY OF OPERATION

The theory of operation is divided into two sections; a simplified block diagram discussion and a detailed block diagram discussion.

The power supply normally operates from +20, -20, and +15 volt outputs of the HP 30310A Power Supply and supplies +12.7, +12.0, +5, and -5 volts to the memory system. When AC input power to the HP 30310A Power Supply is interrupted, a seven-cell lead-acid battery pack in the HP 30311A

Table B-3. HP 30311A Power Supply Specifications

POWER REQUIREMENTS

+17.3 and −17.3 +15 ± 5%	These are nominal voltages. They are the +20V and −20V outputs of the HP 30310A Power Supply. The actual voltage value is controlled by a signal from the HP 30311A Power Supply as a function of load and temperature. The ±20V ADJ potentiometer on the HP 30310A Power Supply must be set fully clockwise.

OUTPUT VOLTAGES AND CURRENTS

Volts	Amperes
+12.7 (2)	0.8 (3)
+12.0 ± 1% (1)	1.85 (3)
+5.0 ± 2.5%	3.6
−5.0 ± 1%	0.2
−3.0 ± 5%	0.2

DIMENSIONS	Centimeters	Inches
Height	17.8	7
Width	21.3	8.375
Depth	36.8	15.2

NOTES

(1) The +12.0 volt output is adjustable with a +12V ADJ potentiometer on the rear panel.

(2) The +12.7 volt output tracks the +12.0 volt output under normal loads and remains 0.7 ± 0.2 volts higher.

(3) Amperes stated are for expected usage in semiconductor memory applications.

Power Supply furnishes the input power and maintains the voltages to the memory system. The amount of time the battery continues to furnish power depends on the condition of the battery and the size of memory requiring power. Normally, the battery will furnish power for 40 to 90 minutes before it discharges to a level that activates the undervoltage circuits and removes all power from memory.

The power supply can be operated without the battery. However, no power will be available to the memory system if AC power is removed from the HP 30310A Power Supply. When operating in this mode, the battery status lights are disabled. A battery mode switch on the 30311-60003 Control PCA must be set to operate without a battery.

B-27. BLOCK DIAGRAM DESCRIPTION. Figure B-4 is a block diagram of the HP 30311A Power Supply. The figure shows the relationship with the HP 30310A Power Supply.

The +20 volt output of the HP 30310A Power Supply provides the charging power for the battery pack and the input power for the +12.7, +12.0, and +5 volt regulators. The TEMP SENSE input to the HP 30310A controls the output of the +20 volt line. The +20 volt output also supplies input power to the +5 volt regulator and the control circuits.

Outputs of −3 and −5 volts are derived from a source voltage obtained from the +5 volt switching regulator. Load current from the −3 volt line adds to the −5 volt load current so that a single current limit on the −5 volt line protects both outputs. The maximum combined current for the −3 and −5 volt loads may be divided between the loads in any combination.

Over/under voltage detectors can disable the PSU (Power Supply Up) system DC power line, and shut down the power supply by sensing the +12.0, +5, and −5 volt outputs for undervoltage. The −3 volt output is sensed for undervoltage to disable the +12.0 and +12.7 volt outputs, thus protecting the memory array chips from lack of either −3 or −5 volt substrate bias. Overvoltage conditions sensed on the +5 and +12.0 volt outputs cause the power supply to crowbar to protect the TTL elements and memory array chips.

Indicators and controls that monitor and control HP 30311A operation are located on the System's DC Control Panel and on the front panel of the HP 30311A.

B-28. DETAILED BLOCK DIAGRAM DESCRIPTION. The +20 volt output of the HP 30310A Power Supply provides the power required for HP 30311A operation and the current to charge the seven-cell lead-acid battery pack. The +20 volt output of the HP 30310A Power Supply is regulated by the HP 30311A Power Supply controlling the DC input to its TEMP SENSE input terminal. These connections may be seen in the detailed block diagram of the HP 30311A, figure B-5.

B-29. Battery Pack. When the power switch is ON, the battery pack is connected to the +20 volt line through Fuse F1. While the switch is ON, the battery is kept at the proper float voltage. Float voltage is defined as the voltage applied to keep the battery fully charged. The battery charge voltage is temperature dependent and the float voltage is nominally +16.45 volts at room temperature. A temperature sensitive resistor located in the battery pack senses the temperature variations and varies the potentials of the battery charge voltage divider. This change in potential controls the battery voltage regulator output that is connected to the TEMP SENSE terminal of the HP 30310A Power Supply. A decrease in battery temperature produces a control voltage from the battery voltage regulator that causes the +20 volt line to increase to the correct float voltage for

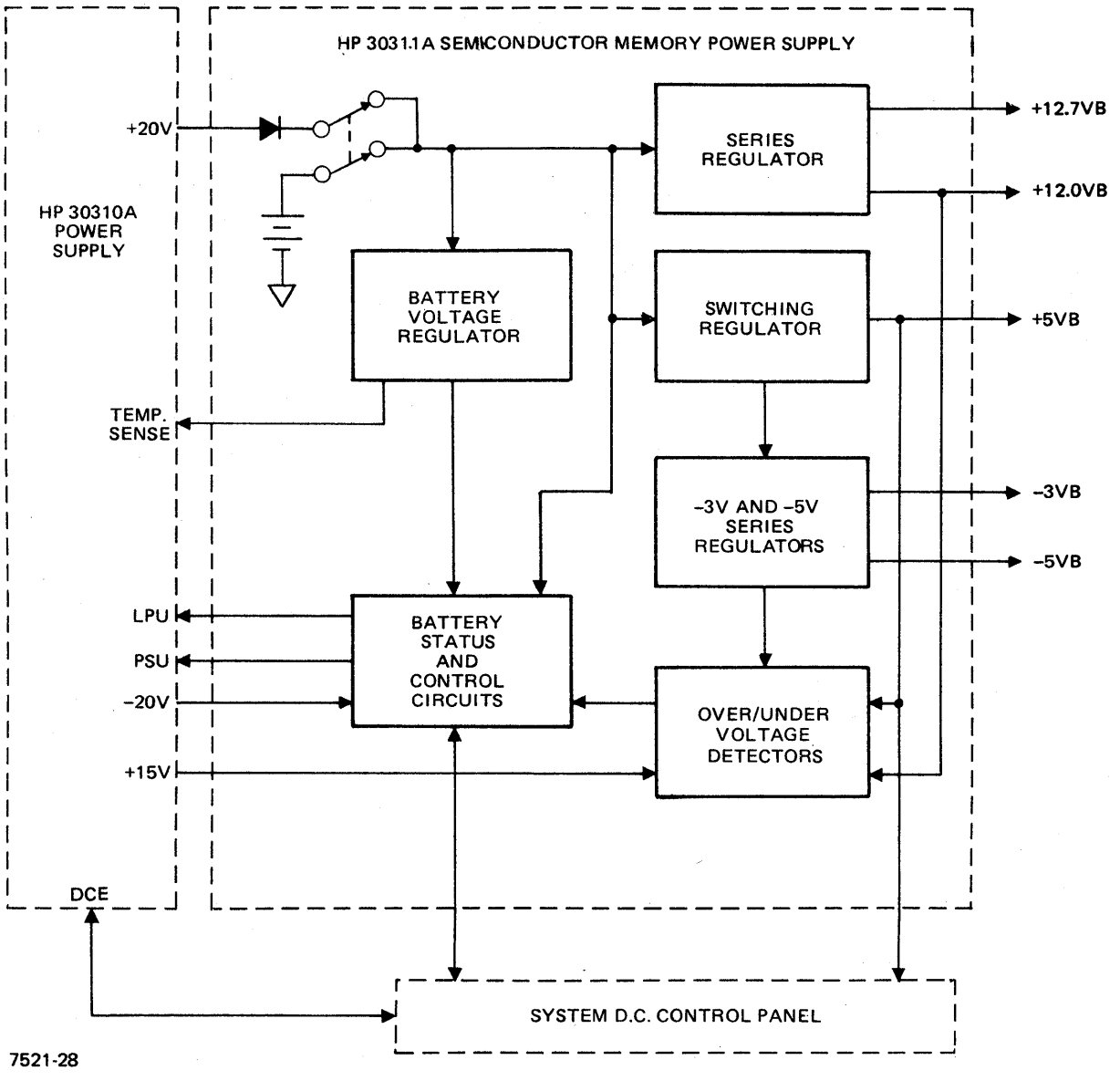


Figure B-4. HP 30311A Power Supply Simplified Block Diagram

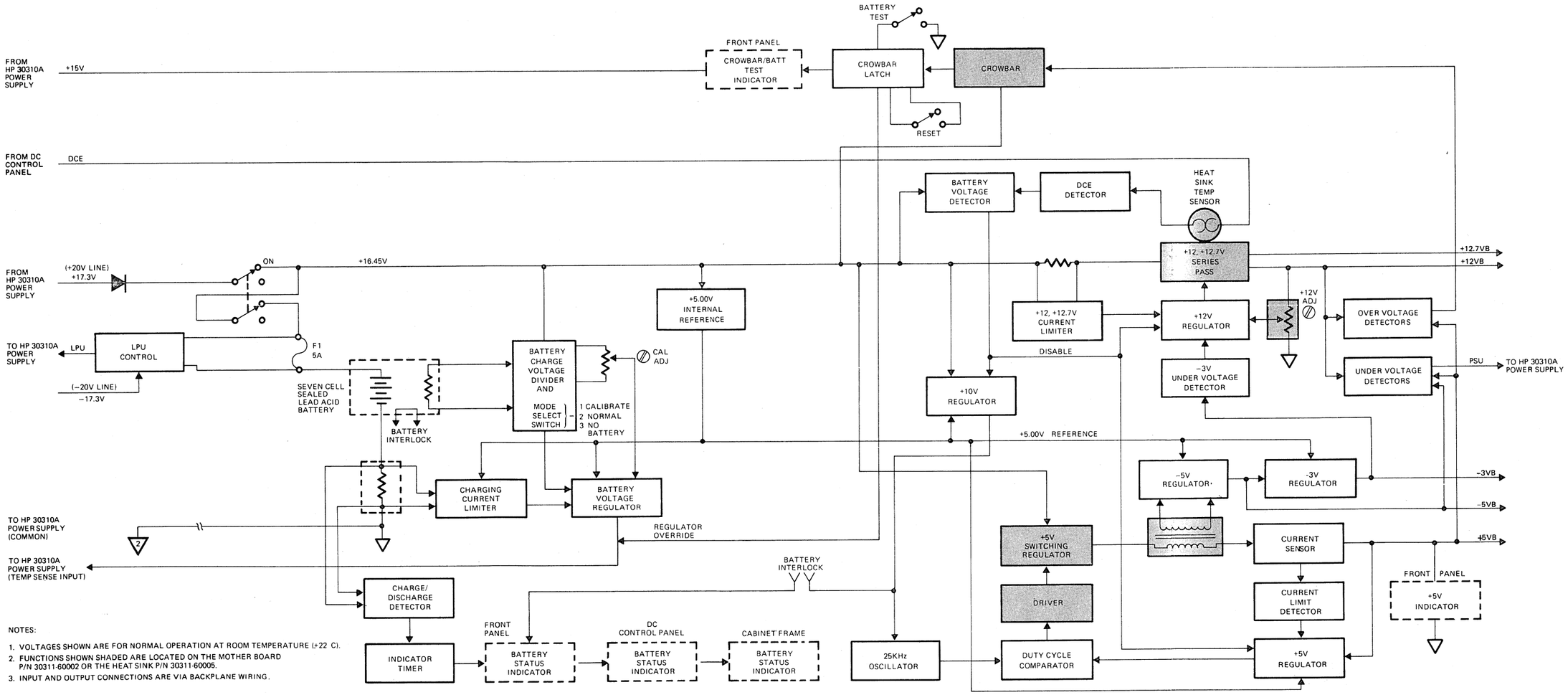


Figure B-5. HP 30311A Power Supply Detailed Block Diagram

battery charge. A 1-degree C temperature change produces approximately a 0.03 volt change on the +20 volt line. The temperature-voltage relationship has a negative coefficient. The +20 volt line is approximately +17.3 volts for a battery pack at 22 degrees C (room temperature). The –20 volt line will be at the same voltage as the +20 volt line because they track each other in the HP 30310A Power Supply.

B-30. Battery Charge/Discharge. The charging current limiter overrides the battery voltage regulator to limit the current drawn by the battery pack. This prevents damage to a fully discharged or very low battery during any portion of the charging period. The charge/discharge detector signals the indicator timer to select a 0.5-Hertz flashing rate for the LED detectors if the battery pack is charging; or a 2-Hertz rate (one ON to three OFF ratio) if the battery pack is discharging. When the battery is fully charged during normal operation, the BATTERY STATUS indicator is continually lit. If the HP 30311A is operated without a battery or the battery is discharged below a usable level with input power to the HP 30310A Power Supply removed, the BATTERY STATUS indicator remains off. The status indicators are disabled by the battery interlock jumper when no battery is installed.

B-31. Line Power Up. As long as the HP 30311A Power Supply fuse F1 is good, with or without a battery, LPU (Line Power Up) is returned to the HP 30310A Power Supply to indicate that the HP 30311A is capable of battery backup operation.

B-32. DC Enable. The DCE (DC Enable) signal from the DC Control Panel is present when its particular control switch is in the ON position, and is applied ground true to the DCE detector through the temperature sensor on the motherboard heat sink. The state of the DCE signal is sensed by the DCE detector which controls the battery voltage detector. Absence of the DCE signal shuts down the power supply.

B-33. Internal Supplies. A +5.00 volt internal reference voltage is developed from the +16.45 volt level and is distributed to various functional circuits in the power supply. This voltage is primarily used for comparison purposes in circuit operations. A +10 volt regulator, also operating from the +16.45 volt line, provides additional operating potentials for the power supply and disables the power supply upon command from the battery voltage detector.

B-34. Battery Voltage Protection. When the supply is operating from the battery pack, the battery voltage is monitored by the battery voltage detector. When the battery discharges to a preset +12.6 volt level, the battery voltage detector disables the +10, +12, and +5 volt regulators causing the output voltages to shut off. The battery voltage detector also prevents the battery from discharging down to 0 volts. When AC power to the HP 30310A Power Supply is resumed, the battery pack starts charging, but the output voltages remain turned off until the battery voltage rises to a preset +14.9 volt level. The battery voltage detector also disables the power supply output voltages when the DCE signal is removed.

B-35. Regulators. The +5 volt output is obtained from a duty-cycle controlled switching regulator. The +5 volt switching regulator output passes through a transformer to develop approximately –7.5 volts as the source for the –5 volt regulator which in turn provides the source for the –3 volt regulator. The +12 volt output is obtained from a precision regulated series pass transistor with the +12.7 volt output referenced to the +12 volt line. The +12 ADJ permits the +12 volt output to be set between 10 and 12.9 volts for memory operation. The +12.7 volt output tracks the +12 volt output and remains a nominal +0.7 volt above it for any setting of the adjustment.

B-36. Over/Under Voltage Protection. The +5 and +12 volt outputs are sensed for overvoltage to protect the TTL circuits on the Semiconductor Memory Control PCA and the memory chips on the Semiconductor Memory Array PCA. An overvoltage condition causes the crowbar to fire and sets the crowbar latch. Firing the crowbar pulls the +16.45 volt line to ground and opens fuse F1. The crowbar latch produces a regulator override signal which is sent to the TEMP SENSE input of the HP 30310A Power Supply. The regulator override signal also causes the +20 volt line to drop to approximately +0.2 volt. The +15 volt line from the HP 30310A Power Supply is maintained to keep the crowbar latch energized. The HP 30311A Power Supply is then completely shut down (fuse F1 opens and there is approximately 0 volts on the +20 volt line).

The +12, +5, and –5 volt outputs are sensed for undervoltage to disable the PSU (Power Supply Up) power control lines at turn on (when all the output signals are above their undervoltage levels). Enabling PSU to the HP 30310A Power Supply enables the start of the 0.6-second delay to the system PON line.

B-37. Battery Test. Located on the rear panel of the power supply is a momentary toggle switch labeled BATTERY TEST. This switch places the power supply in the battery discharge mode. When the switch is depressed, the crowbar latch is set providing a REGULATOR OVERRIDE signal that effectively forces the +20 volt line to approximately 0 volts. Fuse F1 is not opened and the power supply operates from the battery pack as evidenced by the BATTERY STATUS indicator flashing at a 2-Hertz rate and the CROWBAR/BATT TEST indicator turning on. The computer should be halted before this simulated power fail verification is attempted. The power supply is returned to normal operation by momentarily pressing the RESET switch which is located on the power supply front panel.

B-38. CONTROLS AND INDICATORS

Controls and indicators mounted on the front panel of the HP 30311A Power Supply and on the DC Control Panel are provided to monitor and control power supply status and operation. In addition, test points on the power supply front panel are provided as an aid in troubleshooting. An internal three-position slide-switch permits power supply operation with a battery or without a battery, and in the calibrate position allows setting of the battery float voltage level.

Figure B-6 shows the locations of the controls and indicators on the power supply panels and on the DC Control panel. Table B-4 lists the function of each control and indicator. The BATTERY STATUS indicator is duplicated on the power supply, on the DC Control Panel, and on the top of the cabinet door of the main bay. The power supply +5 indicator is also duplicated on the DC Control Panel as the SYSTEM DC POWER indicator.

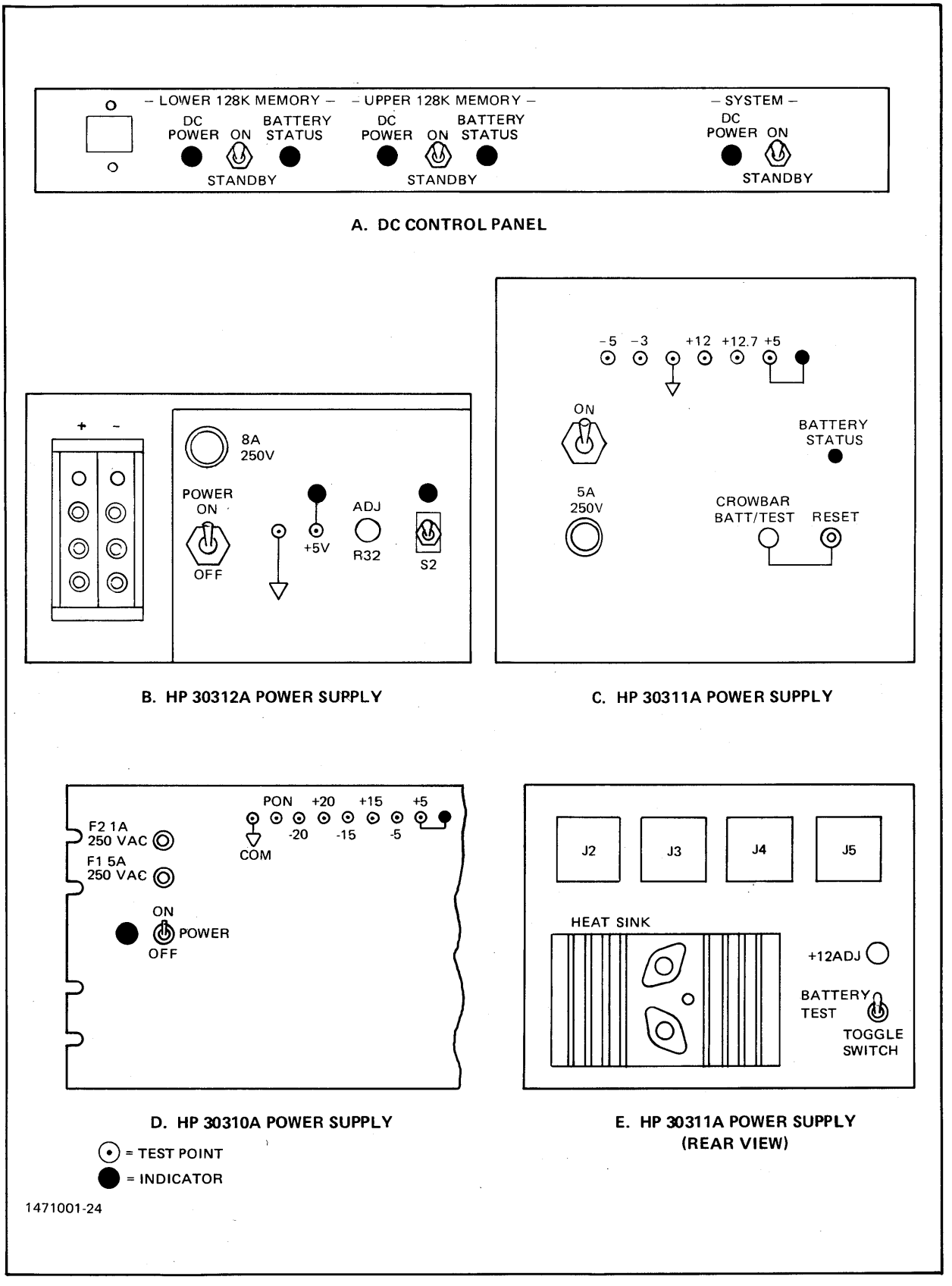


Figure B-6. Power Controls and Indicators

Table B-4. HP 30311A Power Supply Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
Power ON/OFF Toggle Switch	In the ON position, connects +20 volts from the HP 30310A Power Supply to the HP 30311A to maintain the charge on the battery and to develop required memory voltages. In the OFF (down) position, disables the HP 30311A.
BATTERY TEST Momentary Toggle Switch (mounted on rear of unit)	Places power supply in a battery discharge mode for test purposes. (Simulates a power failure condition.)
RESET Pushbutton Switch	Resets the battery discharge mode returning the power supply to normal operation.
+5 LED Indicator	When lit, indicates that +5 volts is being produced by the HP 30311A Power Supply.
CROWBAR/BATT TEST LED Indicator	Used in conjunction with the BATTERY STATUS indicator to determine if the crowbar circuit has fired and shut down the power supply.
BATTERY STATUS LED Indicator	Indicates battery condition as follows: a. Remains continually lit for a fully-charged battery. b. Flashes at a 2-Hertz rate when the battery is discharging. c. Flashes at a 0.5-Hertz rate when the battery is charging. d. Remains off if battery is low or not present.

B-39. HP 30311A MAINTENANCE

No high voltage points exist within this power supply. However, the supply is capable of supplying low voltage at moderate current levels. Use caution when manipulating metal tools or probes near exposed conductors and terminals. Extra care should be exercised to prevent the possibility of shorting the output lines of the battery pack.

CAUTION

When cables are connected to or disconnected from the power supply, the corresponding UPPER or LOWER 128K MEMORY DC POWER switch on the System DC Control Panel must be placed in STANDBY and the corresponding HP 30311A power switch must be in the off (down) position to prevent equipment damage.

B-40. WIRING INFORMATION. Interconnecting wiring between the HP 30311A Power Supply and other units of the system is presented in the Engineering Diagrams Manual. The information can be used as an aid to troubleshooting procedures.

B-41. PRINCIPAL SERVICING POINTS. The principal servicing points for the HP 30311A Power Supply are the test points on the front panel and wired connection points on the card cage backplane of the memory.

B-42. TROUBLESHOOTING AN HP 30311A

When a malfunction occurs in the memory DC power system, the available voltage and status indicators should be analyzed with the aid of Figure B-5 to determine if the problem exists in the HP 30311A Power Supply.

B-43. PREVENTIVE MAINTENANCE

Preventive maintenance is performed at monthly or bi-monthly intervals depending on the physical environment prevailing at the site. Preventive maintenance consists of measuring the DC voltages at the test jacks on the power supply front panel and performing the battery test procedure described in paragraph B-45.

B-44. VOLTAGE CHECKS. Measure the five voltages listed in Table B-5 using the digital voltmeter. Allow the recommended warm-up period for the voltmeter before taking any measurements. If any voltage is out of tolerance, make the necessary adjustments as described in paragraphs B-46 through B-49.

Table B-5. DC Output Voltages

VOLTAGE TEST JACK	INDICATION
+5B	5.0 ± 0.125V
+12.7B	+12B + 0.7, ± 0.2V
+12B	12.0 ± 0.12V
−3B	−3.0 ± 0.15V
−5B	−5.0 ± 0.05V

NOTE

If all voltages are out of tolerance, perform the +5.00 volt internal reference adjustment first. (Refer to paragraph B-49.) Also, the +12.7 test jack voltage is equal to whatever voltage is measured at the +12 test jack plus 0.7 ± 0.2 volts.

B-45. **BATTERY TEST.** The battery test certifies that the backup capability of the power supply is functioning normally. The system must be halted before performing this test. Proceed as follows:

a. On the rear panel of the power supply, momentarily press the BATTERY TEST toggle switch.

b. The CROWBAR/BATT TEST indicator should light and the BATTERY STATUS indicator should flash at a 2-Hertz rate. Allow the battery to discharge for 3 to 5 minutes.

c. Return the power supply to normal operation by pressing the RESET pushbutton on the power supply front panel.

d. The BATTERY STATUS indicator flashes at a 0.5-Hertz rate until the battery is fully charged. Then the indicator remains continually lit.

B-46. HP 30311A ADJUSTMENTS

The following adjustments should be performed after replacing a power supply or after replacing a circuit board or battery pack within the power supply.

B-47. **BATTERY (FLOAT) VOLTAGE ADJUSTMENT.** Float voltage must be adjusted whenever a battery pack is replaced.

CAUTION

The replacement battery pack must be at a stable known ambient temperature before the adjustment is performed. For a change in ambient temperature, the settling time for the pack is 4 to 6 hours. Failure to observe this precaution may considerably degrade the backup time and/or shorten the life of the battery pack.

Adjust the float voltage as follows:

a. Power down the system by placing the corresponding UPPER or LOWER 128K MEMORY DC POWER switch on the System DC Control Panel to STANDBY and place the corresponding HP 30311A Power Supply power switch off (down).

b. Remove the power supply from the cabinet and place on a suitable support.

c. Remove the top cover from the power supply.

d. Connect the digital voltmeter between the +16.45V test point on the control board (figure B-7) and a common ground point on the edge of the control board.

NOTE

Allow the digital voltmeter to warm-up before taking any measurements.

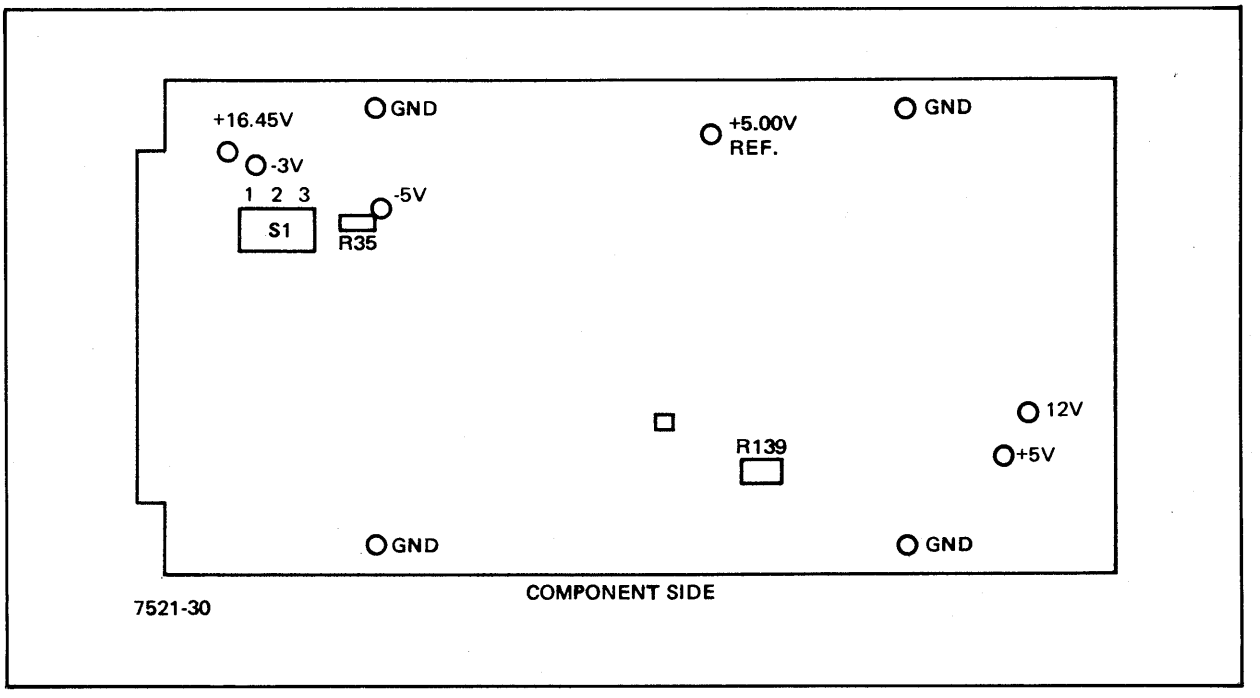


Figure B-7. Control Board Adjustment Locations

e. Place control board switch S1 in position 1 (calibrate).

f. Power up the system and allow five minutes for power supply circuits to stabilize.

g. Refer to table B-6 and determine the float voltage setting.

h. Adjust potentiometer R35 on the control board (figure B-7) for the voltmeter indication determined in the previous step. This assumes that the battery is almost fully charged. If it is not, the voltmeter indication will be low and gradually increase as the battery charges. A stable indication must exist before R35 can be satisfactorily adjusted.

i. Set switch S1 to position 2 (normal).

j. Power down the system and disconnect the digital voltmeter.

k. Replace power supply top cover.

l. Install the power supply into the cabinet.

Table B-6. Float Voltage Versus Temperature*

TEMPERATURE (0°C)	FLOAT VOLTAGE	TEMPERATURE (0°C)	FLOAT VOLTAGE
0	17.10	28	16.26
1	17.07	29	16.23
2	17.04	30	16.20
3	17.01	31	16.17
4	16.98	32	16.14
5	16.95	33	16.11
6	16.92	34	16.08
7	16.89	35	16.05
8	16.86	36	16.02
9	16.83	37	16.09
10	16.80	38	15.96
11	16.77	39	15.93
12	16.74	40	15.90
13	16.71	41	15.87
14	16.68	42	15.84
15	16.65	43	15.81
16	16.62	44	15.78
17	16.59	45	15.75
18	16.56	46	15.72
19	16.53	47	15.69
20	16.50	48	15.66
21	16.47	49	15.63
22	16.44	50	15.60
23	16.41	51	15.57
24	16.38	52	15.54
25	16.35	53	15.51
26	16.32	54	15.48
27	16.29	55	15.45

*For 7-cell sealed lead-acid battery

B-48. +12 VOLT ADJUSTMENT. The +12 volt output of the power supply is adjusted as follows:

a. Connect the digital voltmeter between the +12 and (common) test jacks on the power supply front panel.

NOTE

Allow the digital voltmeter to warm-up before taking any measurements.

b. Adjust the +12ADJ control located on the rear panel of the power supply for a 12.0 + 0.12 volt indication on the digital voltmeter.

B-49. +5.00 VOLT INTERNAL REFERENCE ADJUSTMENT. The +5.00 volt internal reference is adjusted as follows:

a. Power down the system by placing the corresponding UPPER or LOWER 128K MEMORY DC POWER switch on the DC Control Panel to STANDBY and place the corresponding HP 30311A Power Supply power switch off (down).

b. Remove the power supply from the cabinet and place on a suitable support.

c. Remove the top cover from the power supply.

d. Connect the digital voltmeter between the +5.00 volt internal reference test point on the control board (figure B-7) and a common ground point on the control board.

NOTE

Allow the digital voltmeter to warm-up for the recommended warm-up period before taking any measurements.

e. Power up the system and allow five minutes for power supply circuits to stabilize. Measure the +5.00 volt internal reference voltage (+5.00 + 0.005 volts).

f. If necessary, adjust R139 on the control board for a 5.00 + 0.005 volt indication on the digital voltmeter.

NOTE

If an adjustment was necessary, the BATTERY (FLOAT) VOLTAGE adjustment procedure must also be performed.

g. Power down the system and disconnect the digital voltmeter.

h. Replace power supply top cover.

i. Install the power supply into the cabinet.

B-50. REPLACEMENT PROCEDURES

B-51. POWER SUPPLY REPLACEMENT. The power supply is replaced by performing the following steps:

a. Power down the system by placing the corresponding UPPER or LOWER 128K MEMORY DC POWER switch on the System DC Control Panel to STANDBY and place the corresponding HP 30311A Power Supply power switch off (down).

b. Disconnect plugs P2, P3, and P4 on the rear panel of the power supply.

c. Remove four screws on the front of the cabinet securing the power supply to the cabinet frame and the two screws on the right rear of the power supply and remove the power supply by sliding it forward.

d. The power supply is installed using the reverse order of the above procedure.

B-52. BATTERY PACK REPLACEMENT. To replace a battery pack in the power supply, perform the following steps:

a. Remove the power supply from the cabinet by performing steps a through c of paragraph B-51.

b. Remove the top cover from the power supply.

c. Disconnect jack J7 coming from the battery pack.

d. Remove the battery pack cover plate.

e. Remove the battery pack by lifting it out.

Install a new battery pack by using the reverse order of the above procedure. The battery float voltage adjustment which is described in paragraph B-47 must be performed anytime a battery pack is replaced.

B-53. CONTROL PCA REPLACEMENT. The control board is replaced by performing the following steps:

a. Remove the power supply from the cabinet by performing steps a through c of paragraph B-51.

b. Remove two screws holding the control board to the metal spacers on the top right side of the frame.

c. Disconnect plug P2 on the control board and disconnect the control board from the motherboard. Lift out the control board.

NOTE

The +5.00 volt internal reference voltage must be checked and the battery float voltage must be adjusted after replacing a control board.

The control board is reassembled by using the reverse order of the above procedure.

B-54. MOTHERBOARD PCA REPLACEMENT. To replace the motherboard with its associated heat sink, perform the following steps:

a. Power down the system by placing the corresponding UPPER or LOWER 128K MEMORY DC POWER switch on the DC Control Panel to STANDBY and place the corresponding HP 30311A Power Supply power switch off (down).

b. Disconnect plugs P2, P3, P4, and P5 on the rear panel of the power supply.

c. Remove the power supply from the cabinet.

d. Remove top and bottom covers from the power supply.

e. Free the motherboard by removing four screws, two from the top and two from the bottom edges of the rear panel frame.

f. Disconnect plug P6 on the motherboard.

g. Slide the two boards out of the rear of the power supply frame.

h. Remove the control board from J1 on the motherboard.

NOTE

Steps i and j should be performed when the motherboard and heat sink are to be replaced.

i. Remove four screws holding the motherboard to the rear panel.

j. Remove four screws securing the heat sink to the rear panel.

The motherboard and heat sink are replaced by using the reverse order of the above procedure. Power supply output voltages should be checked after replacing the motherboard.

B-55. HP 30312A POWER SUPPLY

The HP 30312A Power Supply delivers up to 100 amperes of five-volt power for operation of the interface PCAs in the I/O area of the computer. The power supply is an HP 62605M Power Supply modified by adding a power switch, fuse, AC receptacle, and a threshold adjustment circuit. The threshold adjustment circuit is adjusted when the system is configured to provide overcurrent shutdown of the HP 62605M Power Supply when the drain on the power supply exceeds a predetermined amount by ten amperes.

The information to follow covers only the items and circuit added to the HP 62605M Power Supply. The HP 62605M Power Supply is described in Modular Power Supplies, L and M Series, Models 62605L, 62605M, and 62615M, manual (part number 5950-1756). The Model 62605M is equipped with Option 106 which enables the power supply to operate on 187 to 250 volts AC input power.

The HP 30312A Power Supply provides five-volt power over a current range nominally 15 to 100 amperes. It augments the approximate 55-ampere, five-volt output of the HP 30310A Power Supply which powers the CPU/IOP, the HP 30311A Power Supply, and portions of the computer I/O area.

B-56. THEORY OF OPERATION

The following paragraphs contain the theory of operation for the HP 30312A Power Supply Interface Board (part number 30312-60002). Principles of operation for the model 62605M Power Supply are contained in its associated Operating and Service Manual, HP part number 5950-1756.

Figure B-8 is a simplified block diagram of the HP 30312A Power Supply showing the major functional areas of the interface board. The model 62605M Power Supply is also shown to illustrate the relationship between the power supply and the interface board. The interface logic is required to properly sense and control the 62605M Power Supply with the existing HP 30310A Power Supply system DC control lines (DCE and PSU). Input power of 208/230 VAC is applied to the power supply and interface board by POWER switch S3 through the eight-ampere fuse. An internal power supply provides the operating potentials for the circuits including the reference voltage (adjusted to 4.75 volts by potentiometer R51) used by several functional circuits on the interface board.

B-57. OVERCURRENT PROTECTION. The operating current configurator monitors the +5 volt load on the 62605M Power Supply and is activated whenever the load increases 10 amperes above the normal load. When S2 is pressed, ADJ potentiometer R32 is adjusted at the normal steady state current level. When S2 is released, the threshold is automatically incremented to sense a current 10 amperes above the nominal value set with R32.

Transient overcurrents exceeding the 10-ampere margin cause the over current indicator (located above switch S2) to light for the transient time interval. The two-second timer prevents the power supply from shutting down when overloads are less than two seconds long. When such overloads last longer than two seconds, the two-second timer sets the latch (causing the over current indicator to light continually) and shuts down the 62605M Power Supply output by pulling the A1 terminal control voltage below its turnon value.

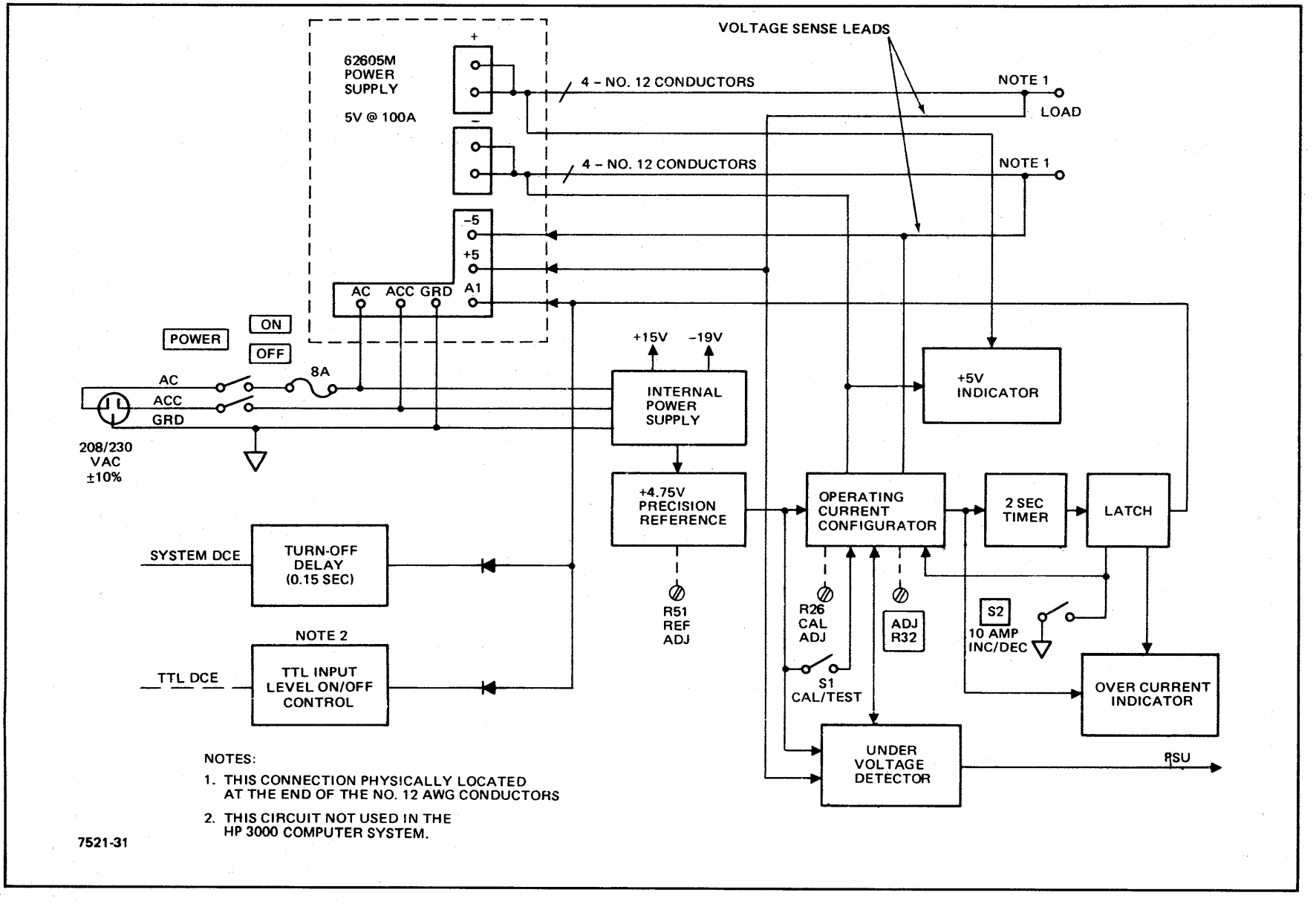


Figure B-8. HP 30312A Power Supply Simplified Block Diagram

The Cal/Test switch S1 and Cal Adj potentiometer R26 are used by factory personnel to calibrate the operating current configurator to the resistance of the high current wires connected to the power supply. These controls are normally not used in the field and should be left as they are.

B-58. UNDER VOLTAGE PROTECTION. The under voltage detector, connected to the +S (+sense) terminal of the power supply, sets the Power Supply Up (PSU) signal low (1V) to the system whenever the output voltage at the load drops below 4.61 volts. The PSU signal is restored to the open circuit condition whenever the output voltage at the load rises above 4.81 volts.

B-59. POWER FAILURES. An AC power failure sensed by the HP 30310A Power Supply causes Power Fail Warning (PFW) signal to be sent to the CPU, therefore the HP 30312A does not require a power failure detector. Maximum utilization of this detection capability can only be obtained when the 30310A and 30312A are supplied from the same AC power source.

B-60. DC ENABLE. The DCE is the same control line connected to the HP 30310A DCE terminal. It turns on (DCE at gnd) and turns off (DCE approximately +10 volts) the +5 volt output of the HP 30312A. The interface board receives the DCE signal and generates the appropriate signal to the A1 control terminal on the 62605M Power Supply. The interface board circuits delay the turnoff of the +5 volt line after release of the DCE signal by about 0.15 seconds to allow ample time for the HP 30310A Power Supply to generate its PFW signal for the CPU. This delay guarantees the +5 volt output will be present for at least 1 msec after the CPU receives the PFW signal.

B-61. HP 30312A MAINTENANCE

WARNING

While the input power is connected, use caution when working inside the power supply. Many exposed conductors carry low DC voltages which are capable of supplying heavy currents if short-circuited, resulting in high heat and the possibility of painful burns. Use caution when manipulating metal tools or probes. A wrist watch, or a metal necklace, bracelet, or ring must not be worn. Avoid dropping tools, screws, or other metal objects onto conductors. Remove power and recover dropped objects at once; if forgotten, damage could result later.

AC power-line voltage is exposed when covers are removed. Exercise extreme caution when working in the power supply with covers removed, and never work under this condition unless another person is nearby and within sight.

B-62. WIRING INFORMATION. Interconnecting wiring between the HP 30312A Power Supply and other units of the system is shown in the Engineering Diagrams Manual.

B-63. TROUBLESHOOTING AN HP 30312A

If the computer system is down because the 5-volt output of this power supply is absent, disconnect the wire at terminal A1 of the HP 62605M Power Supply. If power is restored, the interface board (30312-60002) is defective. If power is not restored, the HP 62605M unit is bad.

BATTERY CARE

APPENDIX C

C-1. INTRODUCTION

This appendix provides information on the care of the lead-acid cell used in an HP 30311A Power Supply. The part number of the battery is 30311-60006.

C-2. ENVIRONMENT

The useful life of a lead-acid cell is shortened if the cell is exposed to prolonged excessive heat or prolonged cold. Deterioration is greatest at temperatures over 60 degrees C and under −20 degrees C. In addition, while a cell is charging, cold temperatures hinder recovery and warm temperatures (about 35 to 40 degrees C) speed it.

C-3. SHELF LIFE

Shelf life is defined as the storage life of a battery whether it is installed in the power supply or stored on a shelf.

A fully charged battery stored on a shelf at room temperature will typically lose 50 percent of its charge in six months.

A discharged battery has an extremely short shelf life. Leaving a battery in a discharged state is by far the most serious cause of cell damage. The surfaces of the plates gradually become sulfated with the result that the charge acceptance capability of the cell approaches zero with increases in sulfation.

Some degrees of cell damage follow:

- A cell left in the discharged state for one or two days will probably begin to accept a charge within a few seconds or minutes.
- A cell left in the discharged state for several weeks may take from several hours to several days to begin accepting a charge. Although it will charge more slowly than normal, such a battery will eventually recover fully in one or two days of continual charging.
- A cell left in the discharged state for six months may never recover charge acceptance capability. If it does recover, recovery will occur after the cell has been on a charger for weeks.

C-4. RESTORING DAMAGED CELLS

When a fully discharged cell is left a week or two in the discharged state, it appears as an open circuit to a source of charge. This is why a neglected battery pack appears to be fully charged when an HP 30311A Power Supply is first turned on. The charging current detector sees no charging current and immediately indicates a fully charged condition. The battery backup capability in this case is actually non-existent.

Such a cell or battery can be restored if put on a constant-current-limited power supply (0.15 to 0.25 amperes) with the charging voltage set to 150 percent of the normal float voltage. Once the cell or battery starts accepting a charge, apply 130 to 150 percent of its ampere-hour capacity. Note that the cells used in the battery for the HP 30311A are rated at 5 ampere-hours.

C-5. SHIPPING BATTERIES

We recommend that the 5-ampere fuse of the HP 30311A Power Supply be removed when the power supply is shipped or stored. This prevents the battery from discharging if the front panel power switch is accidentally tripped during handling. (A tripped switch causes the battery to discharge fully in three or four days.)

C-6. SUMMARY

The HP 30311A Power Supply is designed to power memory and, with its battery backup capability, to carry the system through AC line power failures and brief maintenance procedures. If AC power is interrupted, the HP 30311A can provide backup power for approximately 15 minutes.

A few practical suggestions for improving battery life follow:

- Avoid exposing batteries to excessive heat or cold for prolonged periods.
- Never leave a lead-acid cell or battery in a discharged state for longer than absolutely necessary.
- Disable the power supplies and battery output by setting the LOWER 128K MEMORY and, if appropriate, the UPPER 128K MEMORY switches to STANDBY if system shutdown will exceed 15 minutes.
- Turn off the HP 30311A Power Supplies at their front panel if system shutdown will exceed four hours.