$8.00

Optoelectronics Designer's Catalog 1986

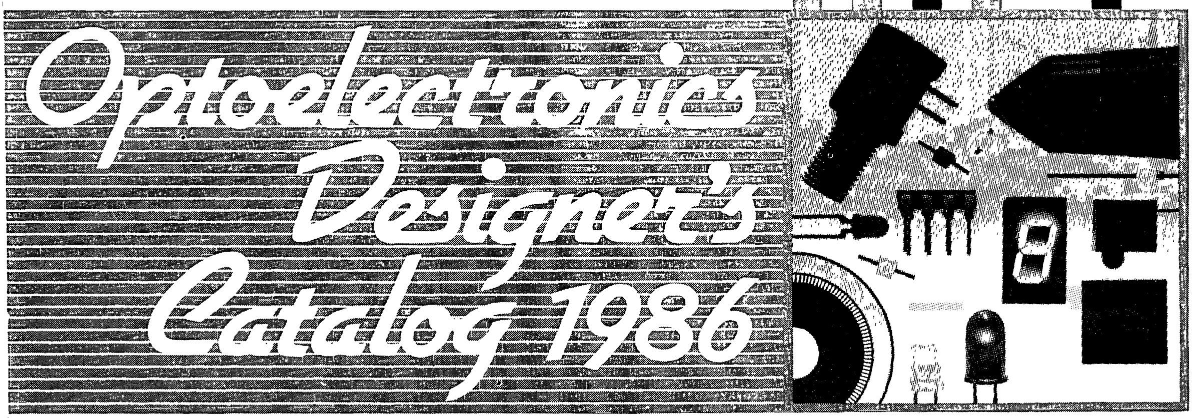
HEWLETT PACKARD

To help you in choosing and designing with HP optoelectronic components, detailed specifications for HP bar code components, motion sensing and encoder products, LED displays, lamps, light bars and bar graphs, fiber optics, optocouplers and high reliability products are included in this catalog.

How to Find the Right Information
To help you locate the product needed for your application, there is a table of contents which indicates each section by thumb-tab, an alphanumeric index following the table of contents, and product selection guides in the opening of each product line section. There are ten sections, one for each of the product lines listed above plus a section containing a complete listing of application bulletins and notes. Section 10 is an appendix containing HP sales and service as well as authorized distributor locations.

How to Order
To order complete applications information, use the business reply card in the back of this book, or call your nearest HP sales office. Ask for the Components office. There is a listing of HP Component sales and service offices for the U.S. on Pages 10-13 and 10-14. In Europe and the rest of the world, look on pages 10-6 through 10-12 in the appendix for the worldwide listing of HP sales and service offices.

Also in the appendix is a worldwide listing of HP authorized distributors. These distributors offer off-the-shelf delivery for most HP components.



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New Products in **BOLD** Type.

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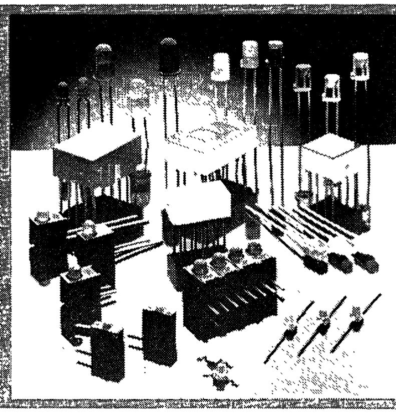
Hewlett-Packard Components: A Brief Sketch



In 1964, Hewlett-Packard established a new division having the charter of developing and producing state-of-the-art electronic components for internal use. By 1975, both microwave and optoelectronic devices contributed to the growing business of Hewlett-Packard and the Components Group was formed. Today there are three divisions: the Optoelectronics division, Optical Communications division and Microwave Semiconductor division. In addition to these three divisions there is a specialized team of people to develop, manufacture and market bar code components.

The products of the Components Group are vertically integrated, from the growing of LED crystals to the development of the various on-board integrated circuits to package design. Vertical integration insures that HP quality is maintained throughout product development and manufacturing.

Over 5200 employees are dedicated to HP Components, including manufacturing facilities in Malasia and Singapore, factory and marketing support in San Jose, California and a world-wide sales force. Marketing operations for Europe are located in Boeblingen, Germany.

Each field sales office is staffed with engineers trained to provide technical assistance. An extensive communications network links field with factory to assure that each customer can quickly attain the information and help needed.

Quality and reliability are two very important concepts to Hewlett-Packard in maintaining the commitment to product performance.

At Hewlett-Packard, quality is integral to product development, manufacturing and final introduction. "Parts per million" (PPM) as a measure of quality is used in HP's definition of product assurance. And HP's commitment to quality means that there is a continuous process of improvement and tightening of quality standards. Manufacturing quality circles and quality testing programs are important ingredients in HP products.

Reliability testing is also required for the introduction of new HP components. Lifespan calculations in "mean-time-between-failure" (MTBF) terms are published and available as reliability data sheets. HP's stringent reliability testing assures long component lifetimes and consistent product performance.

Warranty

HP's Components are warranted against defects in material and workmanship for a period of one year from the date of shipment (in the case of designated Fiber Optics and Bar Code products 90 days from the date of shipment). If HP receives notice of such defects during the warranty period, HP will repair or, at its option, replace components that prove to be defective in material or workmanship under proper use during the warranty period. This warranty extends only to HP customers.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE.

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL THEORY.

The foregoing limitation of liability shall not apply in the event that any HP product sold hereunder is determined by a court of compentent jurisdiction to be defective and to have directly caused bodily injury, death or property damage; provided, that in no event shall HP's liability for property damage exceed the greater of $50,000 or the purchase price of the specific product that caused such damage.

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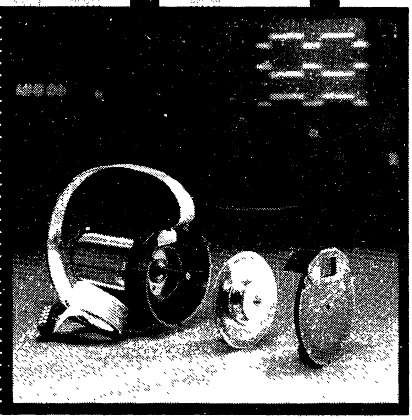
1. Motion Sensing and Control



Motion Sensing and Control

Motion Sensing

As an extension of our emitter/detector systems capability, Hewlett-Packard has developed a family of motion sensing products. These products include optical shaft encoders for closed loop servo applications and digital potentiometers for manual input applications. HP's Optical products provide a digital link converting mechanical shaft rotation into TTL logic level signals.

Our HEDS-5000 and HEDS-6000 series encoders may be used in a wide variety of closed loop servo applications varying from computer peripherals and professional audio-video systems to automated production equipment. Encoders also find wide-spread use in industrial and instrument applications in which digital information is needed to monitor rotary motion.

With three easy to assemble components, the HP encoder system takes advantage of a specialized optical design and a custom integrated circuit to deliver superior performance in a compact package. The design also minimizes the mechanical tolerances required of the shaft and mounting surface. The HEDS-5000 and HEDS-6000 encoders are available with a range of options including resolution and shaft sizes.

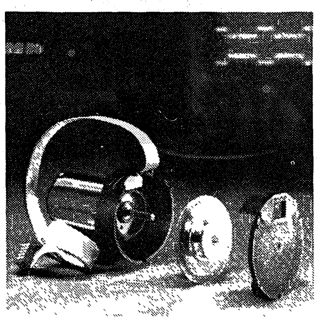
The HEDS-7000 series digital potentiometer is a 28 mm diameter encoder completely assembled with a shaft and bushing, making it suitable for panel mounting. The device converts manual rotary inputs into digital outputs using the same high performance emitter/detector technology used in our encoders. A digital potentiometer can be used as an input mechanism in a variety of applications including: test and measurement equipment, CAD-CAM systems, and positioning tables.

Motion Control

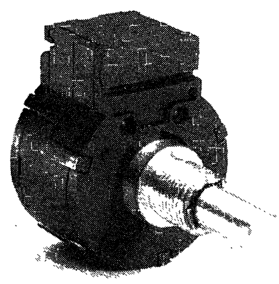
To complement the motion sensing products, HP has recently released two new motion control ICs. The HCTL-1000 general purpose motion control IC greatly simplifies the task of designing digital motion control systems. The HCTL-1000 compares the command position or velocity from a host processor to the actual position or velocity from an incremental encoder, and outputs an appropriate motor command using one of four programmable position and velocity control modes. Some of its other features include a programmable digital filter, an electronic commutator, and a quadrature decoder/counter.

The HCTL-2000 Quadrature Decoder Counter IC provides a one chip, easy to implement solution to interfacing the quadrature output of an encoder or digital potentiometer to a microprocessor. It includes a quadrature decoder, a 12 bit up/down state counter, and an 8 bit bus interface. The use of Schmitt triggered inputs and a digital noise filter allows reliable operation in noisy environments.

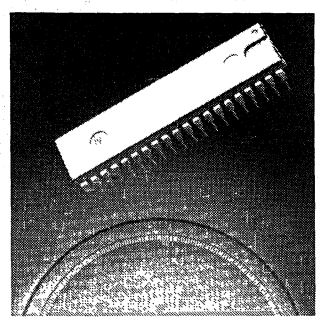
For more information on these new product developments, contact your local Hewlett-Packard Components Field Engineer, or write Hewlett-Packard Optoelectronics Division, 640 Page Mill Road, Palo Alto, California 94304.



Optical Shaft Encoder



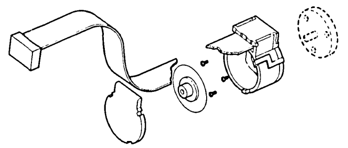
Digital Potentiometer



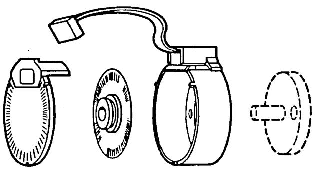
Motion Control IC

Motion Sensing and Control

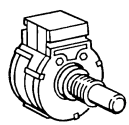
28 mm Diameter Encoders — HEDS-5000 Series

Package Outline Drawing	Part No.	Channels	Option Code		Page No.
			Resolution	Shaft Size	
			□	□□	
	HEDS-5000	A, B	C 100 CPR	01 2 mm	1-5
	OPT □ □□		D 192 CPR	02 3 mm	
			E 200 CPR	03 1/8 in.	
			F 256 CPR	04 5/32 in.	
			G 360 CPR	05 3/16 in.	
	HEDS-5010	A, B, I	H 400 CPR	06 1/4 in.	
	OPT □ □□		A 500 CPR	11 4 mm	
			I 512 CPR	14 5 mm	

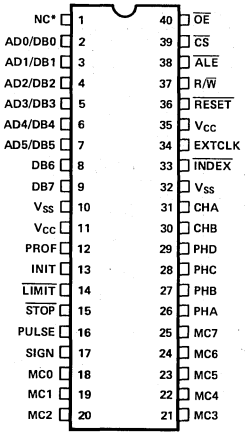
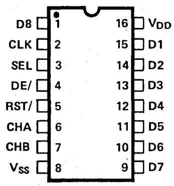
56 mm Diameter Encoders — HEDS-6000 Series

Package Outline Drawing	Part No.	Channels	Option Code		Page No.
			Resolution	Shaft Size	
			□	□□	
	HEDS-6000	A, B	E 200 CPR	05 3/16 in.	1-13
	OPT □ □□		H 400 CPR	06 1/4 in.	
			A 500 CPR	07 5/16 in.	
			I 512 CPR	08 3/8 in.	
			B 1000 CPR	09 1/2 in.	
			J 1024 CPR	10 5/8 in.	
	HEDS-6010	A, B, I		11 4 mm	
	OPT □ □□			12 6 mm	
				13 8 mm	

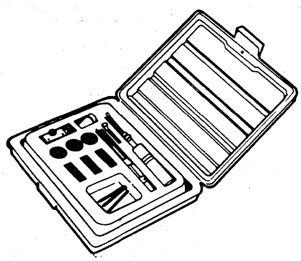
Digital Potentiometer — HEDS-7500 Series

Package Outline Drawing	Part No.	Resolution	Termination	Page No.
	HEDS-7500	256 CPR	Color Coded Wire	1-21
	HEDS-7501	256 CPR	Ribbon Cable	

Motion Control ICs — HCTL-XXXX Series

Package Outline	Part No.	Description	Page No.
 * SHOULD BE LEFT FLOATING.	HCTL-1000	General Purpose Motion Control IC	1-23
	HCTL-2000	Quadrature Decoder/Counter IC	1-43

Convenience Assembly Tools for 28 mm Diameter Encoders — Not Required

Package Outline Drawing	Part No.	Description		Page No.
	HEDS-8930	HEDS-5000 Series Tool Kit	• Holding Screwdriver • Torque Limiting Screwdriver • HEDS-8920 Hub Puller • HEDS-8922 Gap Setter	1-5
	HEDS-892X	Centering Cones	• Aid in High Volume Assembly • Order in Appropriate Shaft Size	

HEWLETT PACKARD

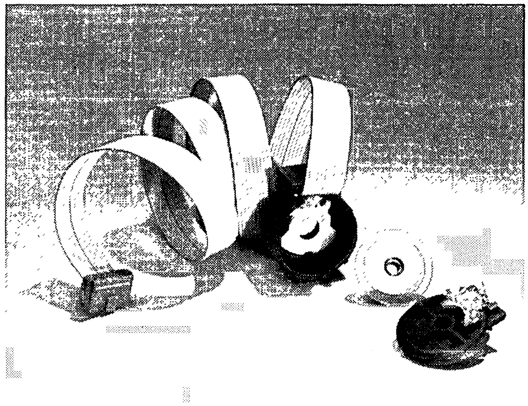
28 mm DIAMETER TWO AND THREE CHANNEL INCREMENTAL OPTICAL ENCODER KIT

HEDS-5000 SERIES

TECHNICAL DATA JANUARY 1986

Features

- SMALL SIZE — 28 mm DIAMETER
- 100-512 CYCLES/REVOLUTION AVAILABLE
- MANY RESOLUTIONS STANDARD
- LOW INERTIA
- QUICK ASSEMBLY
- 0.25 mm (.010 INCHES) END PLAY ALLOWANCE
- TTL COMPATIBLE DIGITAL OUTPUT
- SINGLE 5V SUPPLY
- WIDE TEMPERATURE RANGE
- INDEX PULSE AVAILABLE



Description

The HEDS-5000 series is a high resolution incremental optical encoder kit emphasizing reliability and ease of assembly. The 28 mm diameter package consists of 3 parts: the encoder body, a metal code wheel, and an emitter end plate. An LED source and lens transmit collimated light from the emitter module through a precision metal code wheel and phase plate into a bifurcated detector lens.

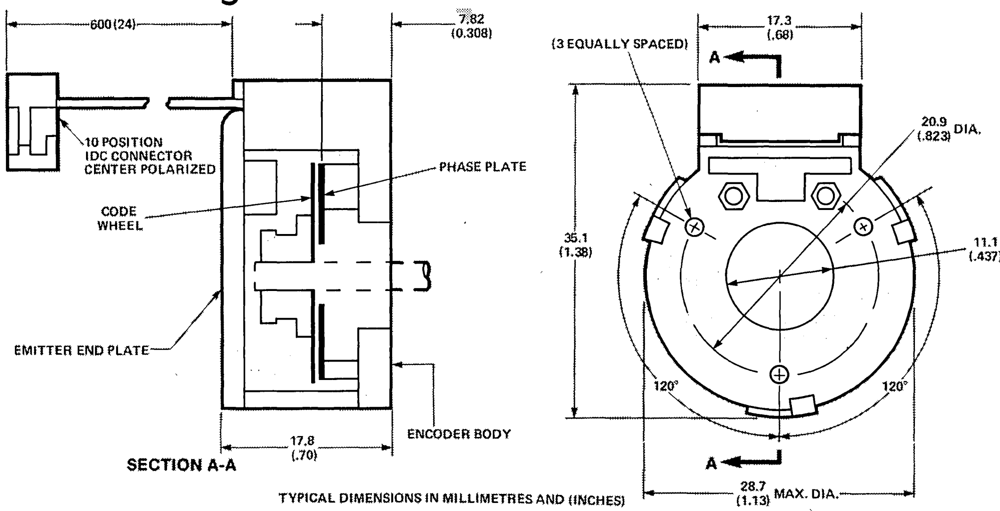
The light is focused onto pairs of closely spaced integrated detectors which output two square wave signals in quadrature and an optional index pulse. Collimated light and a custom photodetector configuration increase long life reliability by reducing sensitivity to shaft end play, shaft eccentricity and LED degradation. The outputs and the 5V supply input of the HEDS-5000 are accessed through a 10 pin connector mounted on a .6 metre ribbon cable.

A standard selection of shaft sizes and resolutions between 100 and 512 cycles per revolution are available. Consult the factory for custom resolutions. The part number for the standard 2 channel kit is HEDS-5000, while that for the 3 channel device, with index pulse, is HEDS-5010. See Ordering Information for more details. For additional design information, see Application Note 1011.

Applications

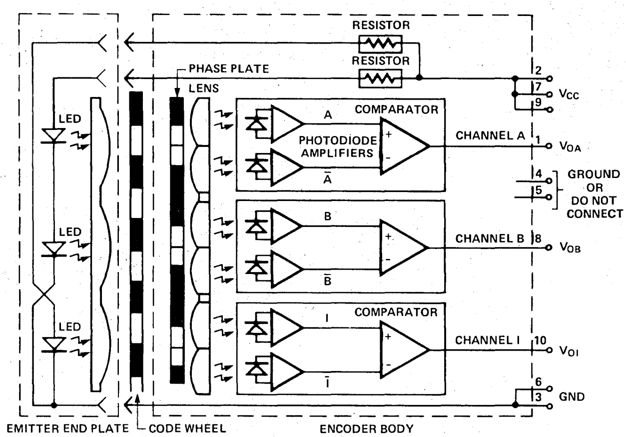
Printers, Plotters, Tape Drives, Positioning Tables, Automatic Handlers, Robots, and any other servo loop where a small high performance encoder is required.

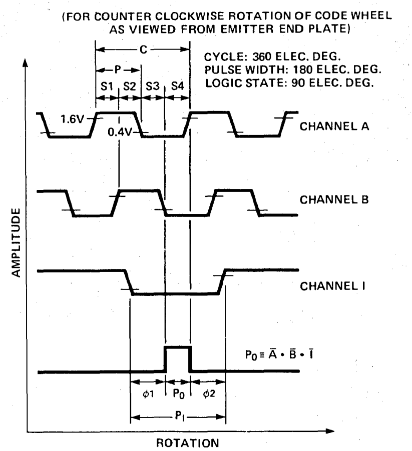
Outline Drawing



TYPICAL DIMENSIONS IN MILLIMETRES AND (INCHES)

Block Diagram and Output Waveforms





Theory of Operation

The incremental shaft encoder operates by translating the rotation of a shaft into interruptions of a light beam which are then output as electrical pulses.

In the HEDS-5XXX the light source is a Light Emitting Diode collimated by a molded lens into a parallel beam of light. The Emitter End Plate contains two or three similar light sources, one for each channel.

The standard Code Wheel is a metal disc which has N equally spaced apertures around its circumference. A matching pattern of apertures is positioned on the stationary phase plate. The light beam is transmitted only when the apertures in the code wheel and the apertures in the phase plate line up; therefore, during a complete shaft revolution, there will be N alternating light and dark periods. A molded lens beneath the phase plate aperture collects the modulated light into a silicon detector.

The Encoder Body contains the phase plate and the detection elements for two or three channels. Each channel consists of an integrated circuit with two photodiodes and amplifiers, a comparator, and output circuitry.

The apertures for the two photodiodes are positioned so that a light period on one detector corresponds to a dark period on the other ("push-pull"). The photodiode signals are amplified and fed to the comparator whose output changes state when the difference of the two photocurrents changes sign. The second channel has a similar configuration but the location of its aperture pair provides an output which is in quadrature to the first channel (phase difference of 90°). Direction of rotation is determined by observing which of the channels is the leading waveform. The outputs are TTL logic level signals.

The optional index channel is similar in optical and electrical configuration to the A and B channels previously described. An index pulse of typically 1 cycle width is generated for each rotation of the code wheel. Using the recommended logic interface, a unique logic state (P_0) can be identified if such accuracy is required.

The three part kit is assembled by attaching the Encoder Body to the mounting surface using three screws. The Code Wheel is set to the correct gap and secured to the shaft. Snapping the cover (Emitter End Plate) on the body completes the assembly. The only adjustment necessary is the encoder centering relative to the shaft. This optimizes quadrature and the optional index pulse outputs.

Index Pulse Considerations

The motion sensing application and encoder interface circuitry will determine the necessary phase relationship of the index pulse to the main data tracks. A unique shaft position can be identified by using the index pulse output only or by logically relating the index pulse to the A and B data channels. The HEDS-5010 allows some adjustment of the index pulse position with respect to the main data channels. The position is easily adjusted during the assembly process as illustrated in the assembly procedures.

Definitions

Electrical degrees:
1 shaft rotation = 360 angular degrees
= N electrical cycles

1 cycle = 360 electrical degrees

Position Error:

The angular difference between the actual shaft position and its position as calculated by counting the encoder's cycles.

Cycle Error:

An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Phase:

The angle between the center of Pulse A and the center of Pulse B.

Index Phase:

For counter clockwise rotation as illustrated above, the Index Phase is defined as:

$$\Phi_I = \frac{(\phi_1 - \phi_2)}{2}.$$

ϕ_1 is the angle, in electrical degrees between the falling edge of I and falling edge of B. ϕ_2 is the angle, in electrical degrees, between the rising edge of A and the rising edge of I.

Index Phase Error:

The Index Phase Error ($\Delta\Phi_I$) describes the change in the Index Pulse position after assembly with respect to the A and B channels over the recommended operating conditions.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-55	100	°Celsius	
Operating Temperature	T_A	-55	100	°Celsius	See Note 1
Vibration			20	g	See Note 1
Shaft Axial Play			.50 (20)	mm(1inch/1000) TIR	
Shaft Eccentricity Plus Radial Play			.1 (4)	mm(1inch/1000) TIR	Movement should be limited even under shock conditions.
Supply Voltage	V_{CC}	-0.5	7	Volts	
Output Voltage	V_O	-0.5	V_{CC}	Volts	
Output Current per Channel	I_O	-1	5	mA	
Velocity			30,000	R.P.M.	
Acceleration	α		250,000	Rad. Sec^{-2}	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	-20	85	°Celsius	Non-condensing atmos.
Supply Voltage	Vcc	4.5	5.5	Volt	Ripple < $100mV_{p-p}$
Code Wheel Gap			1.1 (45)	mm (inch/1000)	Nominal gap = 0.63 mm (.025 in.) when shaft is at minimum gap position.
Shaft Perpendicularity Plus Axial Play			0.25 (10)	mm (inch/1000) TIR	
Shaft Eccentricity Plus Radial Play			0.04 (1.5)	mm (inch/1000) TIR	10 mm (0.4 inch) from mounting surface.
Load Capacitance	C_L		100	pF	

Encoding Characteristics

The specifications below apply within the recommended operating conditions and reflect performance at 500 cycles per revolution (N = 500). Some encoding characteristics improve with decreasing cycles (N). Consult Application Note 1011 or factory for additional details.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes (See Definitions)
Position Error - Worst Error Full Rotation	$\Delta\Theta$		10	40	Minutes of Arc	1 Cycle = 43.2 Minutes See Figure 5.
Cycle Error - Worst Error Full Rotation	ΔC		3	5.5	Electrical deg.	
Max. Count Frequency	f_{MAX}	130,000	200,000		Hertz	f = Velocity (RPM) x N/60
Pulse Width Error - Worst Error Full Rotation	ΔP		16		Electrical deg.	T = 25° C, f = 8 KHz See Note 2
Phase Sensitivity to Eccentricity			520 (13)		Elec. deg./mm (Elec. deg./mil)	mil = inch/1000
Phase Sensitivity to Axial Play			20 (.5)		Elec. deg./mm (Elec. deg./mil)	mil = inch/1000
Logic State Width Error - Worst Error Full Rotation	ΔS		25		Electrical deg.	T = 25° C, f = 8 KHz See Note 2
Index Pulse Width	P_I		360		Electrical deg.	T = 25° C, f = 8 KHz See Note 3
Index Phase Error	$\Delta\Phi_I$		0	17	Electrical deg.	See Notes 4, 5
Index Pulse Phase Adjustment Range		±70	±130		Electrical deg.	See Note 5

Mechanical Characteristics

Parameter	Symbol	Dimension	Tolerance	Units	Notes
Outline Dimensions		See Mech. Dwg.			
Code Wheel Available to Fit the Following Standard Shaft Diameters		2 4 3 5	+.000 −.015	mm	
		5/32	+.0002 −.0005	inches	
		1/8 3/16 1/4	+.0000 −.0007	inches	
Moment of Inertia	J	$0.4\ (6 \times 10^{-6})$		gcm^2 ($oz\text{-}in\text{-}s^2$)	
Required Shaft Length		12.8 (.50)	±0.5 (±0.02)	mm (inches)	See Figure 10. Shaft in minimum length position.
Bolt Circle		20.9 (.823)	±0.13 (±.005)	mm (inches)	See Figure 10.
Mounting Screw Size		1.6 x 0.35 x 5 mm DIN 84 or 0-80 x 3/16 Binding Head		mm inches	

Electrical Characteristics When operating within the recommended operating range.

Electrical Characteristics over Recommended Operating Range (Typical at 25° C).

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		21	40	mA	HEDS-5000 (2 Channel)
			36	60		HEDS-5010 (3 Channel)
High Level Output Voltage	V_{OH}	2.4			V	$I_{OH} = -40\mu A$ Max.
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} = 3.2$ mA
Rise Time	t_r		0.5		μs	$C_L = 25$ pF, $R_L = 11K$ Pull-up
Fall Time	t_f		0.2			See Note 6
Cable Capacitance	C_{CO}		12		pF/metres	Output Lead to Ground

NOTES:

1. The structural parts of the HEDS-5000 have been tested to 20g and up to 500 Hz. For use outside this range, operation may be limited at low frequencies (high displacement) by cable fatigue and at high frequencies by code wheel resonances. Resonant frequency depends on code wheel material and number of counts per revolution. For temperatures below -20° C the ribbon cable becomes brittle and sensitive to displacements. Maximum operating and storage temperature includes the surface area of the encoder mounting. Consult factory for further information. See Application Note 1011.
2. In a properly assembled lot 99% of the units, when run at 25° C and 8 KHz, should exhibit a pulse width error less than 35 electrical degrees, and a state width error less than 45 electrical degrees. To calculate errors at other speeds and temperatures add the values specified in Figures 1 or 2 to the typical values specified under encoding characteristics or to the maximum 99% values specified in this note.
3. In a properly assembled lot, 99% of the units when run at 25° C and 8 KHz should exhibit an index pulse width greater than 260 electrical degrees and less than 460 electrical degrees. To calculate index pulse widths at other speeds and temperatures add the values specified in Figures 3 or 4 to the typical 360° pulse width or to the maximum 99% values specified in this note.
4. After adjusting index phase at assembly, the index phase error specification ($\Delta\Phi_I$) indicates the expected shift in index pulse position with respect to channels A and B over the range of recommended operating conditions and up to 50 KHz.
5. When the index pulse is centered on the low-low states of channels A and B as shown on page 2, a unique P_O can be defined once per revolution within the recommended operating conditions and up to 25 KHz. Figure 6 shows how P_O can be derived from A, B, and I outputs. The adjustment range indicates how far from the center of the low-low state that the center of the index pulse may be adjusted.
6. The rise time is primarily a function of the RC time constant of R_L and C_L. A faster rise time can be achieved with either a lower value of R_L or C_L. Care must be observed not to exceed the recommended value of I_{OL} under the worst case conditions.

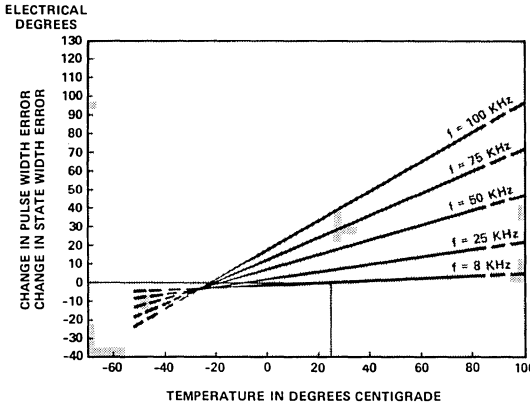


Figure 1. Typical Change in Pulse Width Error or in State Width Error due to Speed and Temperature

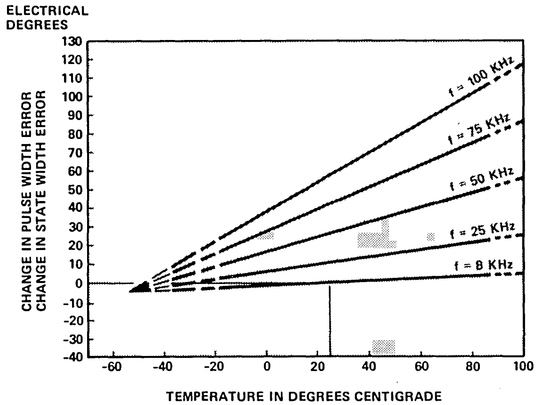


Figure 2. Maximum Change in Pulse Width Error or in State Width Error Due to Speed and Temperature

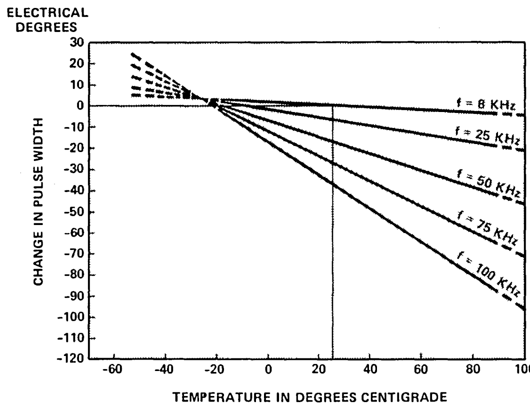


Figure 3. Typical Change in Index Pulse Width Due to Speed and Temperature

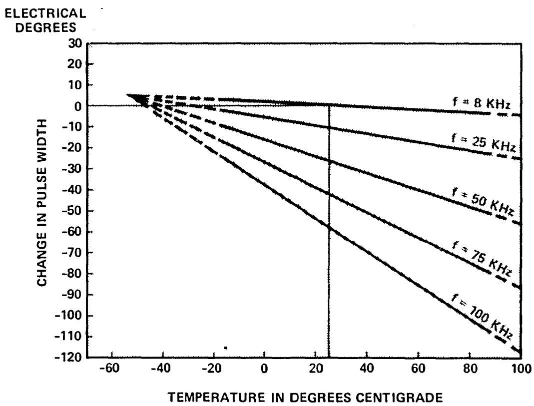


Figure 4. Maximum Change in Index Pulse Width Due to Speed and Temperature

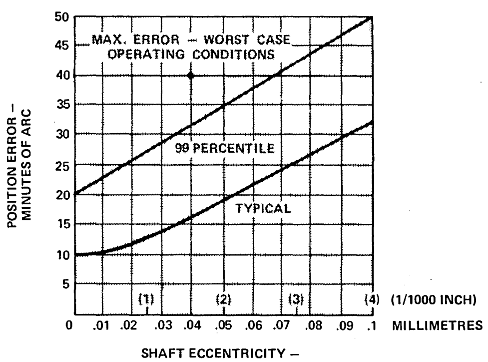
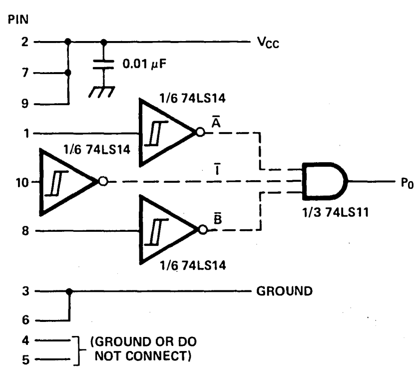
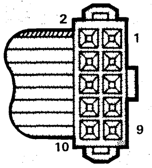


Figure 5. Position Error vs. Shaft Eccentricity



DASHED LINES REPRESENT AN OPTIONAL INDEX SUMMING CIRCUIT.
STANDARD 74 SERIES COULD ALSO BE USED TO IMPLEMENT THIS CIRCUIT.

Figure 6. Recommended Interface Circuit



BOTTOM VIEW

PINOUT

PIN #	FUNCTION
1	CHANNEL A
2	V_{CC}
3	GROUND
4	N.C. OR GROUND
5	N.C. OR GROUND
6	GROUND
7	V_{CC}
8	CHANNEL B
9	V_{CC}
10	CHANNEL I

NOTE: REVERSE INSERTION OF THE CONNECTOR WILL PERMANENTLY DAMAGE THE DETECTOR IC.

MATING CONNECTOR
BERG 65-692-001 OR EQUIVALENT

Figure 7. Connector Specifications

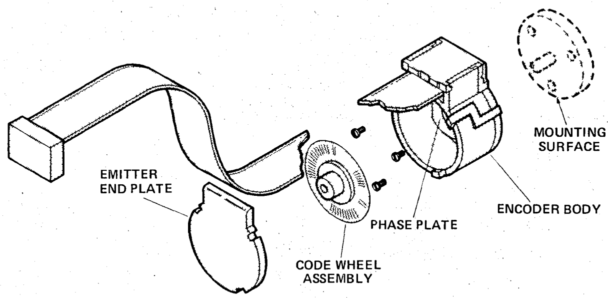


Figure 8. HEDS-5000 Series Encoder Kit

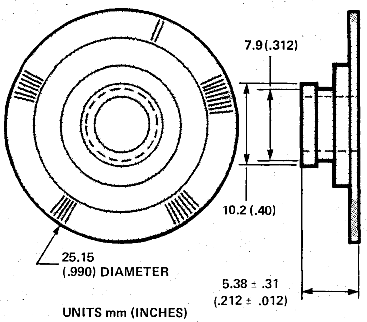
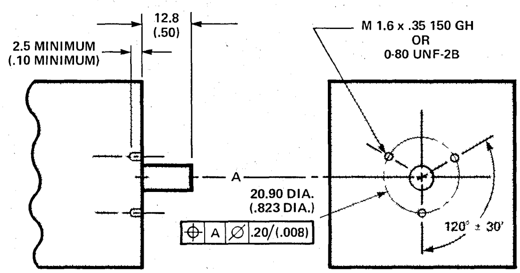


Figure 9. Code Wheel



MILLIMETRE .X ± .5 .XX ± .10
(INCHES) (.XX ± .02 .XXX ± .005)

Figure 10. Mounting Requirements

Ordering Information

HEDS-5 ☐ ☐ ☐

OPTION* ☐ ☐

RESOLUTION (CYCLES PER REVOLUTION)	
C – 100 CPR	G – 360 CPR
D – 192 CPR	H – 400 CPR
E – 200 CPR	A – 500 CPR
F – 256 CPR	I – 512 CPR

NOTE: OTHER RESOLUTIONS AVAILABLE ON SPECIAL REQUEST.

SHAFT DIAMETER
01 – 2 mm
02 – 3 mm
03 – 1/8 in.
04 – 5/32 in.
05 – 3/16 in.
06 – 1/4 in.
11 – 4 mm
14 – 5 mm
00 – USE WHEN ORDERING ENCODER BODIES

PRODUCT TYPE
0 – 28 mm COMPLETE KIT
1 – 28 mm CODE WHEEL
2 – 28 mm ENCODER BODY
3 – 28 mm EMITTER END PLATE*

OUTPUTS
0 – 2 CHANNEL DIGITAL
1 – 3 CHANNEL DIGITAL

MECHANICAL CONFIGURATION
0 – 0.6 m (24 in.) CABLE

*NO OPTION IS SPECIFIED WHEN ORDERING EMITTER END PLATES ONLY.

Shaft Encoder Kit Assembly See Application Note 1011 for further discussion.

The following assembly procedure represents a simple and reliable method for prototype encoder assembly. High volume assembly may suggest modifications to this procedure using custom designed tooling. In certain high volume applications encoder assembly can be accomplished in less than 30 seconds. Consult factory for further details. Note: The code wheel to phase plate gap should be set between 0.015 in. and 0.045 in.

WARNING: THE ADHESIVES USED MAY BE HARMFUL. CONSULT THE MANUFACTURER'S RECOMMENDATIONS.

READ THE INSTRUCTIONS TO THE END BEFORE STARTING ASSEMBLY.

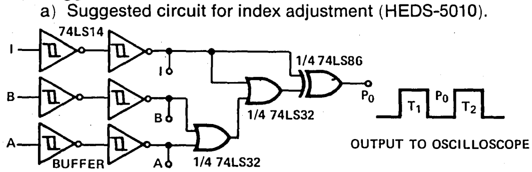
1.0 SUGGESTED MATERIALS

1.1 Encoder Parts
Encoder Body
Emitter End Plate
Code Wheel

1.2 Assembly Materials
RTV — General Electric 162
— Dow Corning 3145
Epoxy—Hysol 1C
Acetone
Mounting Screws (3)
RTV and Epoxy Applicators

1.3 Suggested Assembly Tools
a) Holding Screwdriver.
b) Torque Limiting Screwdriver, 0.36 cm kg (5.0 in. oz.).
c) Depth Micrometer or HEDS-8922 Gap Setter.
d) Oscilloscope or Phase Meter (Described in AN 1011). Either may be used for two channel phase adjustment. An oscilloscope is required for index pulse phase adjustment.

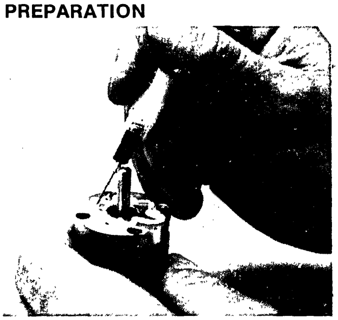
1.4 Suggested Circuits
a) Suggested circuit for index adjustment (HEDS-5010).



For optimal index phase, adjust encoder position to equalize T_1 and T_2 pulse widths.

b) Phase Meter Circuit
Recommended for volume assembly. Please see Application Note 1011 for details.

2.0 SURFACE PREPARATION



THE ELAPSED TIME BETWEEN THIS STEP AND THE COMPLETION OF STEP 8 SHOULD NOT EXCEED 1/2 HOUR.

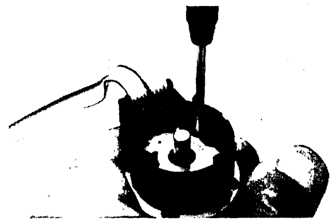
2.1 Clean and degrease with acetone the mounting surface and shaft making sure to keep the acetone away from the motor bearings.

2.2 Load the syringe with RTV.

2.3 Apply RTV into screw threads on mounting surface. Apply more RTV on the surface by forming a daisy ring pattern connecting the screw holes as shown above.

CAUTION: KEEP RTV AWAY FROM THE SHAFT BEARING.

3.0 ENCODER BODY ATTACHMENT



3.1 Place the encoder body on the mounting surface and slowly rotate the body to spread the adhesive. Align the mounting screw holes with the holes in the body base.

3.2 Place the screws in the holding screwdriver and thread them into the mounting holes. Tighten to approximately 0.36 cm kg (5.0 in. oz.) using a torque limiting screwdriver if available (See notes a and b below). Remove centering cone if used.

Notes:
a) At this torque value, the encoder body should slide on the mounting surface only with considerable thumb pressure.
b) The torque limiting screwdriver should be periodically calibrated for proper torque.

4.0 EPOXY APPLICATION

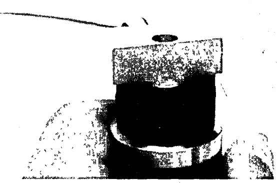
CAUTION: HANDLE THE CODE WHEEL WITH CARE.

4.1 Collect a small dab of epoxy on an applicator.

4.2 Spread the epoxy inside the lower part of the hub bore.

4.3 Holding the code wheel by its hub, slide it down the shaft just enough to sit it squarely. About 3 mm (1/8").

5.0 CODE WHEEL POSITIONING



5.1 Take up any loose play by lightly pulling down on the shaft's load end.

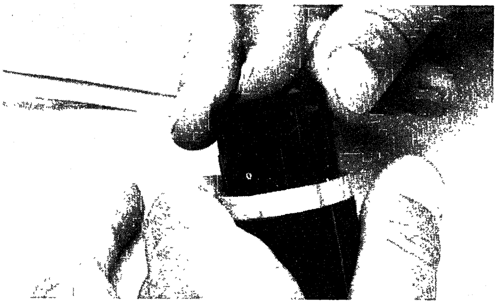
5.2 Using the gap setter or a depth micrometer, push the code wheel hub down to a depth of 1.65 mm (.065 in.) below the rim of the encoder body. The registration holes in the gap setter will align with the snaps protruding from the encoder body near the cable.

5.3 Check that the gap setter or micrometer is seated squarely on the body rim and maintains contact with the code wheel hub.

5.4 No epoxy should extrude through the shaft hole.

DO NOT TOUCH THE CODE WHEEL AFTER ASSEMBLY.

6.0 EMITTER END PLATE

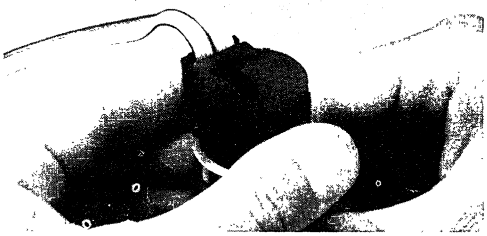


6.1 Visually check that the wire pins in the encoder body are straight and straighten if necessary.

6.2 Hold the end plate parallel to the encoder body rim. Align the guiding pin on the end plate with the hole in the encoder body and press the end plate straight down until it is locked into place.

6.3 Visually check to see if the end plate is properly seated.

7.0 PHASE ADJUSTMENT



7.1 The following procedure should be followed when phase adjusting channels A and B.

7.2 Connect the encoder cable.

7.3 Run the motor. Phase corresponds to motor direction. See output waveforms and definitions. Using either an oscilloscope or a phase meter, adjust the encoder for minimum phase error by sliding the encoder forward or backward on the mounting surface as shown above. See Application Note 1011 for the phase meter circuit.

7.4 No stress should be applied to the encoder package until the RTV cures. Cure time is 2 hours @ 70° C or 24 hrs. at room temperature.

Note: After mounting, the encoder should be free from mechanical forces that could cause a shift in the encoder's position relative to its mounting surface.

CODE WHEEL REMOVAL

In the event that the code wheel has to be removed after the epoxy has set, use the code wheel extractor as follows:

1 Remove the emitter end plate by prying a screwdriver in the slots provided around the encoder body rim. Avoid bending the wire leads.

2 Turn the screw on the extractor counter-clockwise until the screw tip is no longer visible.

3 Slide the extractor's horseshoe shaped lip all the way into the groove on the code wheel's hub.

4 While holding the extractor body stationary, turn the thumb screw clockwise until the screw tip pushes against the shaft.

5 Applying more turning pressure will pull the hub upwards breaking the epoxy bond.

6 Clean the shaft before reassembly.

8.0 INDEX PULSE ADJUSTMENT (HEDS-5010)

8.1 Some applications require that the index pulse be aligned with the main data channels. The index pulse position and the phase must be adjusted simultaneously. This procedure sets index phase to zero.

8.2 Connect the encoder cable.

8.3 Run the motor. Adjust for minimum phase error using an oscilloscope or phase meter (see 7.3).

8.4 Using an oscilloscope and the circuit shown in 1.4, set the trigger for the falling edge of the I output. Adjust the index pulse so that T_1 and T_2 are equal in width. The physical adjustment is a side to side motion as shown by the arrow.

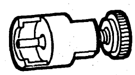
8.5 Recheck the phase adjustment.

8.6 Repeat steps 8.3-8.5 until both phase and index pulse position are as desired.

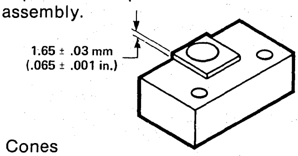
8.7 No stress should be applied to the encoder package until the RTV has cured. Cure time: 2 hours @ 70° C or 24 hrs. at room temperature.

SPECIALITY TOOLS — Available from Hewlett-Packard

a) HEDS-8920 Hub Puller
This tool may be used to remove code wheels from shafts after the epoxy has cured.

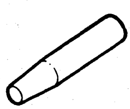


b) HEDS-8922 Gap Setter
This tool may be used in place of a depth micrometer as an aid in large volume assembly.

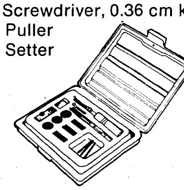


c) HEDS-892X Centering Cones
For easier volume assembly this tool in its appropriate shaft size may be used in step 3.0 to initially center the encoder body with respect to the shaft and aid in locating the mounting screw holes. Depending on the resolution and accuracy required this centering may eliminate the need for phase adjustment steps 7 and 8.

Part Number	Shaft Size
HEDS-8923	2 mm
HEDS-8924	3 mm
HEDS-8925	1/8 in.
HEDS-8926	5/32 in.
HEDS-8927	3/16 in.
HEDS-8928	1/4 in.
HEDS-8929	4 mm
HEDS-8931	5 mm



d) HEDS-8930 HEDS-5000 Tool Kit
1 Holding Screwdriver
1 Torque Limiting Screwdriver, 0.36 cm kg (5.0 in. oz.)
1 HEDS-8920 Hub Puller
1 HEDS-8922 Gap Setter
1 Carrying Case



HEWLETT PACKARD

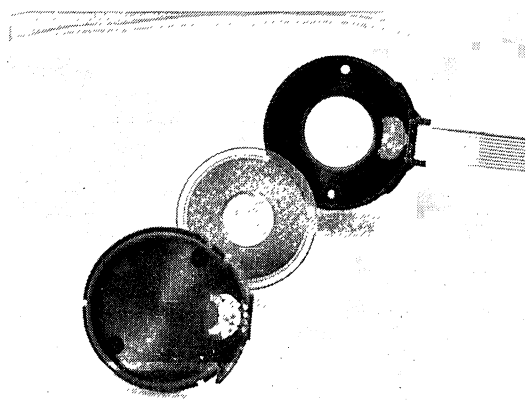
56 mm DIAMETER TWO AND THREE CHANNEL INCREMENTAL OPTICAL ENCODER KIT

HEDS-6000 SERIES

TECHNICAL DATA JANUARY 1986

Features

- 192-1024 CYCLES/REVOLUTION AVAILABLE
- MANY RESOLUTIONS STANDARD
- QUICK ASSEMBLY
- 0.25 mm (.010 INCHES) END PLAY ALLOWANCE
- TTL COMPATIBLE DIGITAL OUTPUT
- SINGLE 5V SUPPLY
- WIDE TEMPERATURE RANGE
- SOLID STATE RELIABILITY
- INDEX PULSE AVAILABLE



Description

The HEDS-6000 series is a high resolution incremental optical encoder kit emphasizing ease of assembly and reliability. The 56 mm diameter package consists of 3 parts: the encoder body, a metal code wheel, and emitter end plate. An LED source and lens transmit collimated light from the emitter module through a precision metal code wheel and phase plate into a bifurcated detector lens.

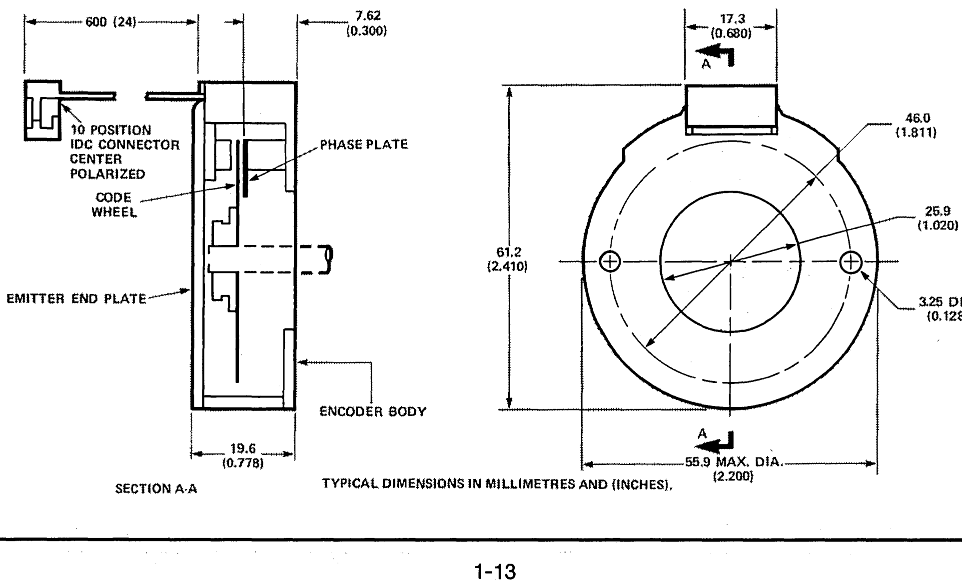
The light is focused onto pairs of closely spaced integrated detectors which output two square wave signals in quadrature and an optional index pulse. Collimated light and a custom photodetector configuration increase long life reliability by reducing sensitivity to shaft end play, shaft eccentricity and LED degradation. The outputs and the 5V supply input of the HEDS-6000 are accessed through a 10 pin connector mounted on a .6 metre ribbon cable.

A standard selection of shaft sizes and resolutions between 192 and 1024 cycles per revolution are available. Consult the factory for custom resolutions. The part number for the standard 2 channel bit is HEDS-6000, while that for the 3 channel device, with index pulse, is HEDS-6010. See Ordering Information for more details. For additional design information, see Application Note 1011.

Applications

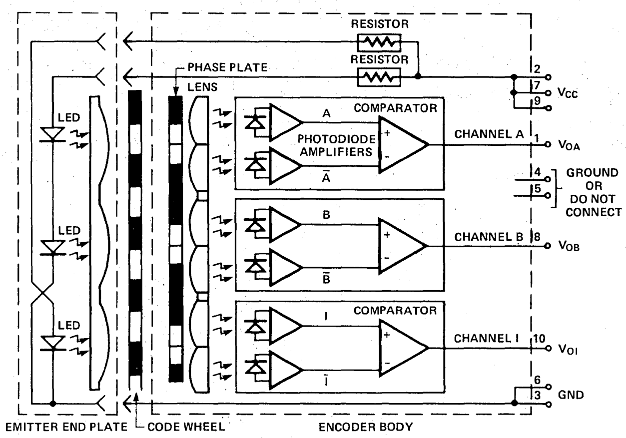
Printers, Plotters, Tape Drives, Positioning Tables, Automatic Handlers, Robots, and any other servo loop where a small high performance encoder is required.

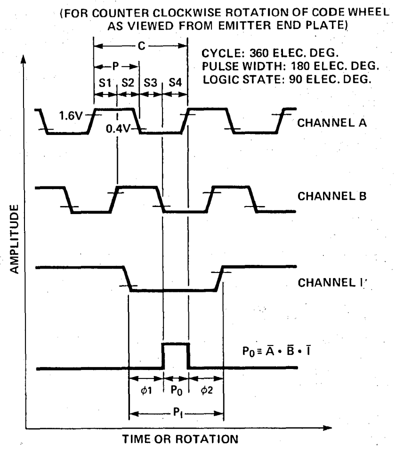
Outline Drawing



TYPICAL DIMENSIONS IN MILLIMETRES AND (INCHES).

Block Diagram and Output Waveforms





Theory of Operation

The incremental shaft encoder operates by translating the rotation of a shaft into interruptions of a light beam which are then output as electrical pulses.

In the HEDS-6XXX the light source is a Light Emitting Diode collimated by a molded lens into a parallel beam of light. The Emitter End Plate contains two or three similar light sources, one for each channel.

The standard Code Wheel is a metal disc which has N equally spaced slits around its circumference. An aperture with a matching pattern is positioned on the stationary phase plate. The light beam is transmitted only when the slits in the code wheel and the aperture line up; therefore, during a complete shaft revolution, there will be N alternating light and dark periods. A molded lens beneath the phase plate aperture collects the modulated light into a silicon detector.

The Encoder Body contains the phase plate and the detection elements for two or three channels. Each channel consists of an integrated circuit with two photodiodes and amplifiers, a comparator, and output circuitry.

The apertures for the two photodiodes are positioned so that a light period on one detector corresponds to a dark period on the other. The photodiode signals are amplified and fed to the comparator whose output changes state when the difference of the two photo currents changes sign ("Push-Pull"). The second channel has a similar configuration but the location of its aperture pair provides an output which is in quadrature to the first channel (phase difference of 90°). Direction of rotation is determined by observing which of the channels is the leading waveform. The outputs are TTL logic level signals.

The optional index channel is similar in optical and electrical configuration to the A,B channels previously described. An index pulse of typically 1 cycle width is generated for each rotation of the code wheel. Using the recommended logic interface, a unique logic state (P_0) can be identified if such accuracy is required.

The three part kit is assembled by attaching the Encoder Body to the mounting surface using two screws. The Code Wheel is set to the correct gap and secured to the shaft. Snapping the cover (Emitter End Plate) on the body completes the assembly. The only adjustment necessary is the encoder centering relative to the shaft, to optimize quadrature and optional index pulse output.

Index Pulse Considerations

The motion sensing application and encoder interface circuitry will determine the need for relating the index pulse to the main data tracks. A unique shaft position is identified by using the index pulse output only or by logically relating the index pulse to the A and B data channels. The HEDS-6010 index pulse can be uniquely related with the A and B data tracks in a variety of ways providing maximum flexibility. Statewidth, pulse width or edge transitions can be used. The index pulse position, with respect to the main data channels, is easily adjusted during the assembly process and is illustrated in the assembly procedures.

Definitions

Electrical degrees:
1 shaft rotation = 360 angular degrees
= N electrical cycles
1 cycle = 360 electrical degrees

Position Error:
The angular difference between the actual shaft position and its position as calculated by counting the encoder's cycles.

Cycle Error:
An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Phase:
The angle between the center of Pulse A and the center of Pulse B.

Index Phase:
For counter clockwise rotation as illustrated above, the Index Phase is defined as:

$$\Phi_I = \frac{(\phi_1 - \phi_2)}{2}.$$

ϕ_1 is the angle, in electrical degrees, between the falling edge of I and falling edge of B. ϕ_2 is the angle, in electrical degrees, between the rising edge of A and the rising edge of I.

Index Phase Error:
The Index Phase Error ($\Delta\Phi_I$) describes the change in the Index Pulse position after assembly with respect to the A and B channels over the recommended operating conditions.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-55	100	°Celsius	
Operating Temperature	T_A	-55	100	°Celsius	See Note 1
Vibration			20	g	See Note 1
Shaft Axial Play			.58 (23)	mm (inch/1000) TIR	
Shaft Eccentricity Plus Radial Play			.25 (10)	mm (inch/1000) TIR	Movement should be limited even under shock conditions.
Supply Voltage	V_{CC}	-0.5	7	Volts	
Output Voltage	V_O	-0.5	V_{CC}	Volts	
Output Current	I_O	-1	5	mA	
Velocity			12,000	R.P.M.	
Acceleration	α		250,000	Rad. Sec^{-2}	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	-20	85	°Celsius	Non-condensing atmos.
Supply Voltage	V_{CC}	4.5	5.5	Volt	Ripple < $100mV_{p-p}$
Code Wheel Gap			1.1 (45)	mm (inch/1000)	Nominal gap = 0.76 mm (.030 in.) when shaft is at minimum gap position.
Shaft Perpendicularity Plus Axial Play			0.25 (10)	mm (inch/1000) TIR	
Shaft Eccentricity Plus Radial Play			0.04 (1.5)	mm (inch/1000) TIR	10 mm (0.4 inch) from mounting surface.
Load Capacitance	C_L		100	pF	

Encoding Characteristics

The specifications below apply within the recommended operating conditions and reflect performance at 1000 cycles per revolution (N = 1000). Some encoding characteristics improve with decreasing cycles (N). Consult Application Note 1011 or factory for additional details.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes (See Definitions)
Position Error	$\Delta\Theta$		7	18	Minutes of Arc	1 Cycle = 21.6 Minutes See Figure 5.
Cycle Error	ΔC		3	5.5	Electrical deg.	
Max. Count Frequency	f_{MAX}	130,000	200,000		Hertz	f = Velocity (RPM) x N/60
Pulse Width Error	ΔP		12		Electrical deg.	T = 25°C, f = 8 KHz See Note 2
Phase Sensitivity to Eccentricity			227 (5.8)		Elec. deg./mm (Elec. deg./mil)	mil = inch/1000
Phase Sensitivity to Axial Play			20 (.5)		Elec. deg./mm (Elec. deg./mil)	mil = inch/1000
Logic State Width Error	ΔS		25		Electrical deg.	T = 25°C, f = 8 KHz See Note 2
Index Pulse Width	P_I		360		Electrical deg.	T = 25°C, f = 8 KHz See Note 3
Index Phase Error	$\Delta\Phi_I$		0	17	Electrical deg.	See Notes 4, 5
Index Pulse Adjustment Range			±165		Electrical deg.	

Mechanical Characteristics

Parameter	Symbol	Dimension	Tolerance	Units	Notes
Outline Dimensions		See Mech. Dwg.			
Code Wheel Available to Fit the Following Standard Shaft Diameters		4 6 8	+.000 −.015	mm	
		3/16 3/8 1/4 1/2 5/16 5/8	+.0000 −.0007	inches	
Moment of Inertia	J	7.7 (110 x 10^{-6})		gcm^2 ($oz\text{-}in\text{-}s^2$)	
Required Shaft Length		15.9 (0.625)	±0.6 (±.024)	mm (inches)	See Figure 10. Shaft at minimum length position.
Bolt Circle		46.0 (1.811)	±0.13 (±.005)	mm (inches)	See Figure 10.
Mounting Screw Size		2.5 x 0.45 x 5 OR #2-56 x 3/16 Pan Head		mm inches	

Electrical Characteristics When operating within the recommended operating range.

Electrical Characteristics over Recommended Operating Range (Typical at 25° C).

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		21	40	mA	HEDS-6000 (2 Channel)
			36	60		HEDS-6010 (3 Channel)
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA Max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Rise Time	t_r		0.5		μs	C_L = 25 pF, R_L = 11K Pull-up
Fall Time	t_f		0.2			See Note 6
Cable Capacitance	C_{CO}		12		pF/meter	Output Lead to Ground

NOTES:

1. The structural parts of the HEDS-6000 have been successfully tested to 20g. In a high vibration environment use is limited at low frequencies (high displacement) by cable fatigue and at high frequencies by code wheel resonances. Resonant frequency depends on code wheel material and number of counts per revolution. For temperatures below -20° C the ribbon cable becomes brittle and sensitive to displacements. Maximum operating and storage temperature includes the surface area of the encoder mounting. Consult factory for further information. See Application Note 1011.
2. In a properly assembled lot 99% of the units, when run at 25° C and 8 KHz, should exhibit a pulse width error less than 32 electrical degrees, and a state width error less than 40 electrical degrees. To calculate errors at other speeds and temperatures add the values specified in Figures 1 or 2 to the typical values specified under encoding characteristics or to the maximum 99% values specified in this note.
3. In a properly assembled lot, 99% of the units when run at 25° C and 8 KHz should exhibit an index pulse width greater than 260 electrical degrees and less than 460 electrical degrees. To calculate index pulse widths at other speeds and temperatures add the values specified in Figures 3 or 4 to the typical 360° pulse width or to the maximum 99% values specified in this note.
4. Index phase is adjusted at assembly. Index phase error is the maximum change in index phase expected over the full temperature range and up to 50 KHz, after assembly adjustment of the index pulse position has been made.
5. When the index pulse is centered on the low-low states of channels A and B as shown on page 2, a unique P_O can be defined once per revolution within the recommended operating conditions and up to 25 KHz. Figure 6 shows how P_O can be derived from A, B, and I outputs. The adjustment range indicates how far from the center of the low-low state that the center of the index pulse may be adjusted.
6. The rise time is primarily a function of the RC time constant of R_L and C_L. A faster rise time can be achieved with either a lower value of R_L or C_L. Care must be observed not to exceed the recommended value of I_{OL} under worst case conditions.

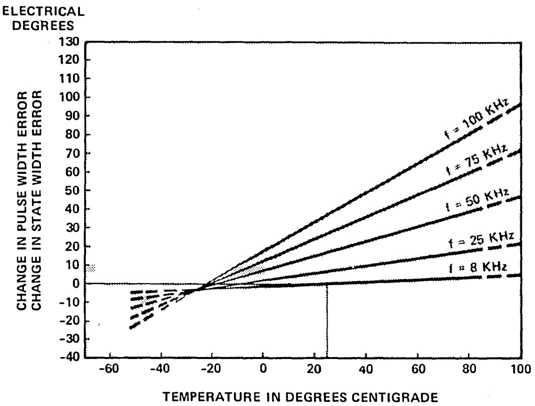


Figure 1. Typical Change in Pulse Width Error or in State Width Error due to Speed and Temperature

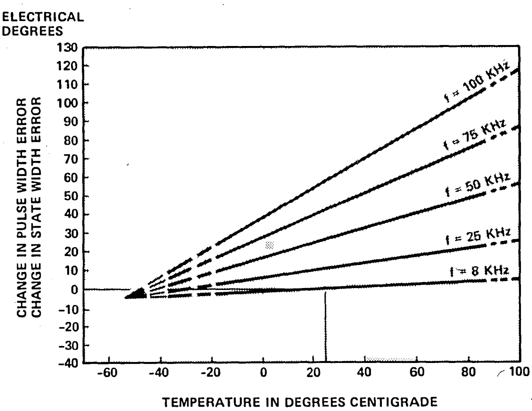


Figure 2. Maximum Change in Pulse Width Error or in State Width Error Due to Speed and Temperature

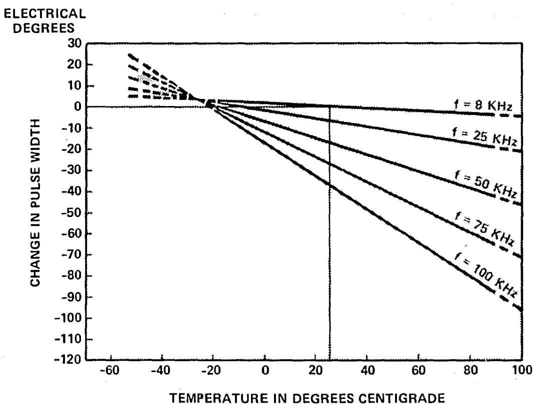


Figure 3. Typical Change in Index Pulse Width Due to Speed and Temperature

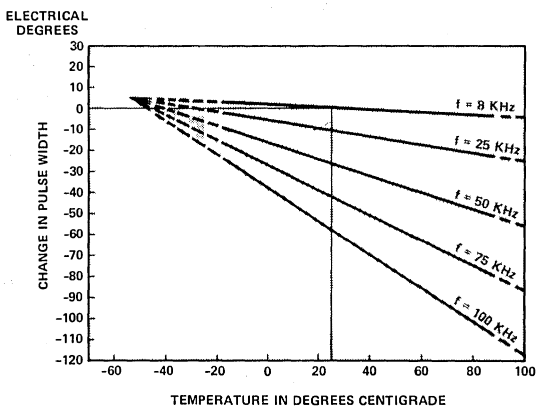


Figure 4. Maximum Change in Index Pulse Width Due to Speed and Temperature

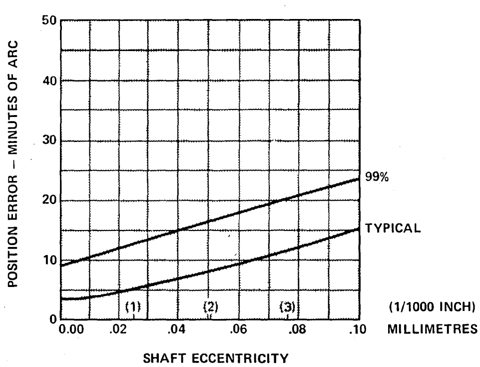
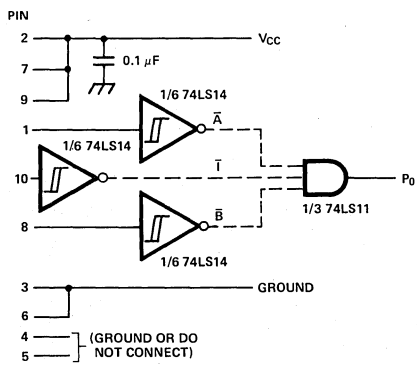


Figure 5. Position Error vs. Shaft Eccentricity

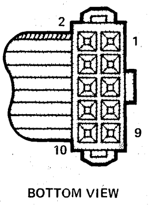


DASHED LINES REPRESENT AN OPTIONAL INDEX SUMMING CIRCUIT.
STANDARD 74 SERIES COULD ALSO BE USED TO IMPLEMENT THIS CIRCUIT.

Figure 6. Recommended Interface Circuit

PINOUT

PIN #	FUNCTION
1	CHANNEL A
2	V_{CC}
3	GROUND
4	N.C. OR GROUND
5	N.C. OR GROUND
6	GROUND
7	V_{CC}
8	CHANNEL B
9	V_{CC}
10	CHANNEL I



MATING CONNECTOR
BERG 65-692-001 OR EQUIVALENT

Figure 7. Connector Specifications

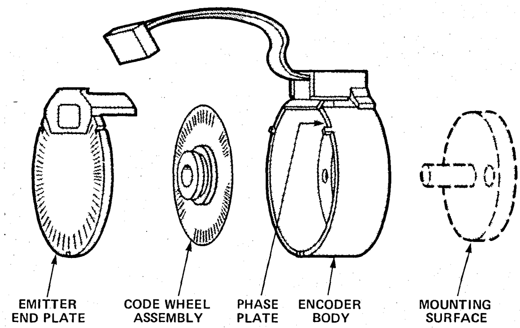


Figure 8. HEDS-6000 Series Encoder Kit

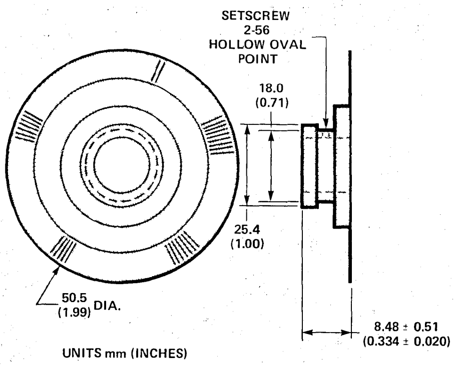


Figure 9. Code Wheel

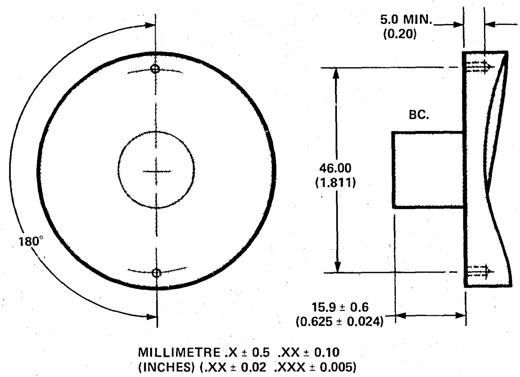


Figure 10. Mounting Requirements

Ordering Information

HEDS-6 ☐ ☐ ☐

OPTION* ☐ ☐

RESOLUTION (CYCLES PER REVOLUTION)

D – 192 CPR	I – 512 CPR
E – 200 CPR	B – 1000 CPR
H – 400 CPR	J – 1024 CPR
A – 500 CPR	

NOTE: OTHER RESOLUTIONS AVAILABLE ON SPECIAL REQUEST

SHAFT DIAMETER

05 – 3/16 IN.
06 – 1/4 IN.
07 – 5/16 IN.
08 – 3/8 IN.
09 – 1/2 IN.
10 – 5/8 IN.
11 – 4 mm
12 – 6 mm
13 – 8 mm
00 – USE WHEN ORDERING ENCODER BODIES

PRODUCT TYPE

0 – 56 mm COMPLETE KIT
1 – 56 mm CODE WHEEL
2 – 56 mm ENCODER BODY
3 – 56 mm EMITTER END PLATE*

OUTPUTS

0 – 2 CHANNEL DIGITAL
1 – 3 CHANNEL DIGITAL

MECHANICAL CONFIGURATION

0 – 0.6 m (24 IN.) CABLE

*NO OPTION IS SPECIFIED WHEN ORDERING EMITTER END PLATES ONLY.

Shaft Encoder Kit Assembly See Application Note 1011 for further discussion.

The following assembly procedure represents a simple and reliable method for prototype encoder assembly. High volume assembly may suggest modifications to this procedure using custom designed tooling. In certain high volume applications encoder assembly can be accomplished in less than 30 seconds. Consult factory for further details. Note — the code wheel to phase plate gap should be set between 0.015 in. and 0.045 in.

WARNING: THE ADHESIVES USED MAY BE HARMFUL. CONSULT THE MANUFACTURER'S RECOMMENDATIONS.

READ THE INSTRUCTIONS TO THE END BEFORE STARTING ASSEMBLY.

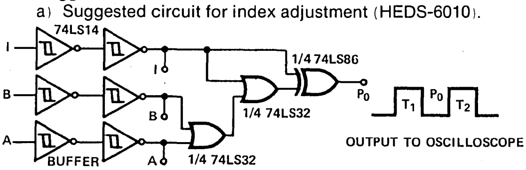
1.0 SUGGESTED MATERIALS

1.1 Encoder Parts
Encoder Body
Emitter End Plate
Code Wheel

1.2 Assembly Materials
RTV-General Electric 162
-Dow Corning 3145
Acetone
Mounting Screws (2)

1.3 Assembly Tools
a) Torque limiting screwdriver, 0.5 cm kg. (7.0 in. oz.).
b) Straight edge. Straight within 0.1 mm (0.004 in.)
c) Oscilloscope. (Phase meter may be optionally used for two channel calibration).
d) Hub puller. Grip-O-Matic-OTC #1000 2-jaw or equivalent. Optional tool for removing code wheels.
e) Syringe applicator for RTV.
f) Torque limiting Allen wrench. 0.5 cm kg (7.0 in. oz.) 0.035 in. hex.

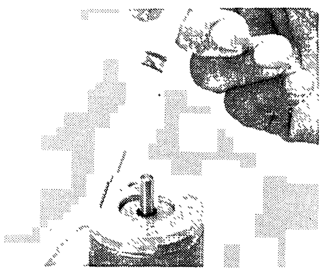
1.4 Suggested Circuits
a) Suggested circuit for index adjustment (HEDS-6010).



For optimal index phase adjust encoder position to equalize T_1 and T_2 pulse widths.

b) Phase Meter Circuit
Recommended for volume assembly. Please see Application Note 1011 for details.

2.0 SURFACE PREPARATION



THE ELAPSED TIME BETWEEN THIS STEP AND THE COMPLETION OF STEP 8 SHOULD NOT EXCEED 1/2 HOUR.

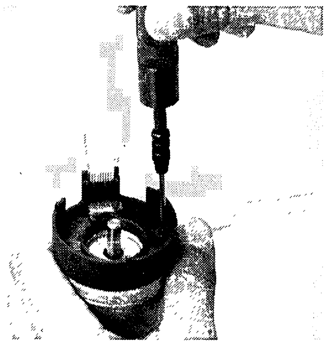
2.1 Clean and degrease with acetone the mounting surface and shaft making sure to keep the acetone away from the motor bearings.

2.2 Load the syringe with RTV.

2.3 Apply RTV into screw threads on mounting surface. Apply more RTV on the surface by forming a daisy ring pattern connecting the screw holes as shown above.

CAUTION: KEEP RTV AWAY FROM THE SHAFT BEARING.

3.0 ENCODER BODY ATTACHMENT



3.1 Place the encoder body on the mounting surface and slowly rotate the body to spread the adhesive. Align the mounting screw holes with the holes in the body base.

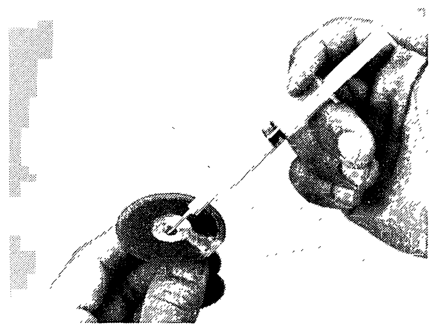
3.2 Place the two mounting screws into the holding bosses in the body base, as shown.

3.3 Thread the screws into the mounting holes and tighten both to 0.5 cm kg (7.0 in. oz.) using the torque limiting screwdriver. (See notes A and B).

3.4 It is not necessary to center the encoder body at this time.

Notes:
a) At this torque value, the encoder body should slide on the mounting surface only with considerable thumb pressure.
b) The torque limiting screwdriver should be periodically calibrated for proper torque.

4.0 APPLICATION OF RTV TO THE HUB



CAUTION: HANDLE THE CODE WHEEL WITH CARE.

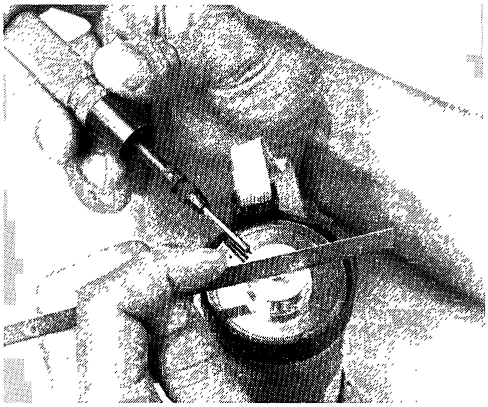
4.1 Make sure that the hex screw on the hub does not enter into the hub bore.

4.2 Apply a small amount of RTV onto the inner surface of the hub bore.

4.3 Spread the RTV evenly inside the entire hub bore.

4.4 Holding the code wheel by its hub, slide it down onto the shaft until the shaft extends at least halfway into the bore.

5.0 CODE WHEEL POSITIONING



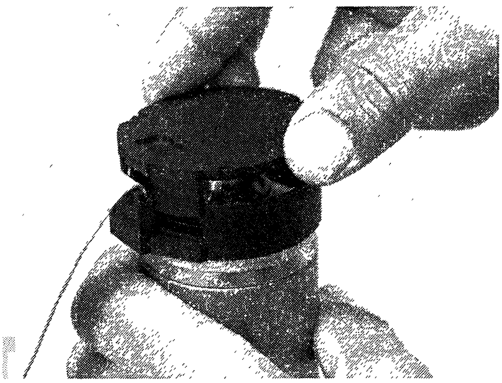
5.1 Position the Allen torque wrench into the hex set screw in the hub, as shown.

5.2 Pull the shaft end down to bottom out axial shaft play. Using the straight edge, push the top of the hub even with the top of the encoder body. The Allen wrench should be used during this movement to apply a slight upward force to the hub, insuring continuous contact between the straight edge and the hub.

5.3 Tighten the hex set screw to approximately 0.5 cm. kg. (7.0 in. oz.) and remove the straight edge.

5.4 The code wheel gap may now be visually inspected to check against gross errors. A nominal gap of 0.8 mm (0.030 in.) should be maintained.

6.0 EMITTER END PLATE

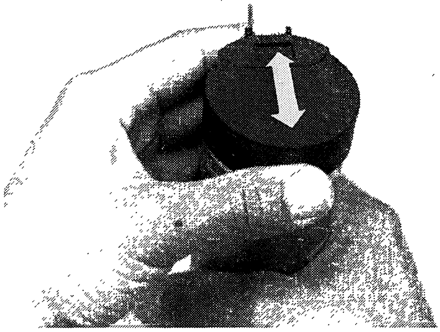


6.1 Visually check that the wire pins in the encoder body are straight and straighten if necessary.

6.2 Align the emitter end plate so that the two flanges straddle the track of the encoder body where the wire pins are located. Press the end plate until it snaps into place.

6.3 Visually check to see if the end plate is properly seated.

7.0 PHASE ADJUSTMENT



7.1 The following procedure should be followed when phase adjusting channels A and B.

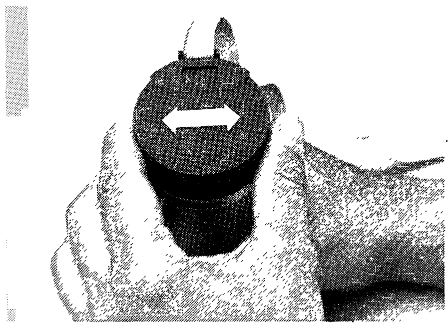
7.2 Connect the encoder cable.

7.3 Run the motor. Phase corresponds to motor direction. See output waveforms and definitions. Using either an oscilloscope or a phase meter, adjust the encoder for minimum phase error by sliding the encoder forward or backward on the mounting surface as shown above. See Application Note 1011 for the phase meter circuit.

7.4 No stress should be applied to the encoder package until the RTV cures. Curve time is 2 hours @ 70° C or 24 hours at room temperature.

Note: After mounting, the encoder should be free from mechanical forces that could cause a shift in the encoder's position relative to its mounting surface.

8.0 INDEX PULSE ADJUSTMENT (HEDS-6010)



8.1 Some applications require that the index pulse be aligned with the main data channels. The index pulse position and the phase must be adjusted simultaneously. This procedure sets index phase to zero.

8.2 Connect the encoder cable.

8.3 Run the motor. Adjust for minimum phase error using an oscilloscope or phase meter. (See 7.3).

8.4 Using an oscilloscope and the circuit shown in 1.4, set the trigger for the falling edge of the P_I output. Adjust the index pulse so that T_1 and T_2 are equal in width. The physical adjustment is a side to side motion as shown by the arrow.

8.5 Recheck the phase adjustment.

8.6 Repeat steps 8.3-8.5 until both phase and index pulse position are as desired.

8.7 No stress should be applied to the encoder package until the RTV has cured. Cure time: 2 hours @ 70° C or 24 hours at room temperature.

HEWLETT PACKARD

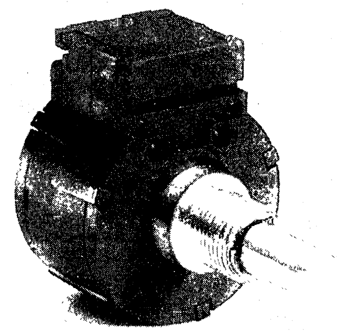
PANEL MOUNT DIGITAL POTENTIOMETER

HEDS-7500 SERIES

TECHNICAL DATA JANUARY 1986

Features

- **DESIGNED FOR MANUAL OPERATION**
- **SMALL SIZE**
- **RELIABLE OPTICAL TECHNOLOGY**
- **256 PULSES PER REVOLUTION STANDARD Other Resolutions Available**
- **TTL COMPATIBLE DIGITAL OUTPUT**
- **SINGLE 5 V SUPPLY**
- **—20° TO +85° C OPERATING RANGE**
- **0.1 OZ.-IN. NOMINAL SHAFT TORQUE**



Description

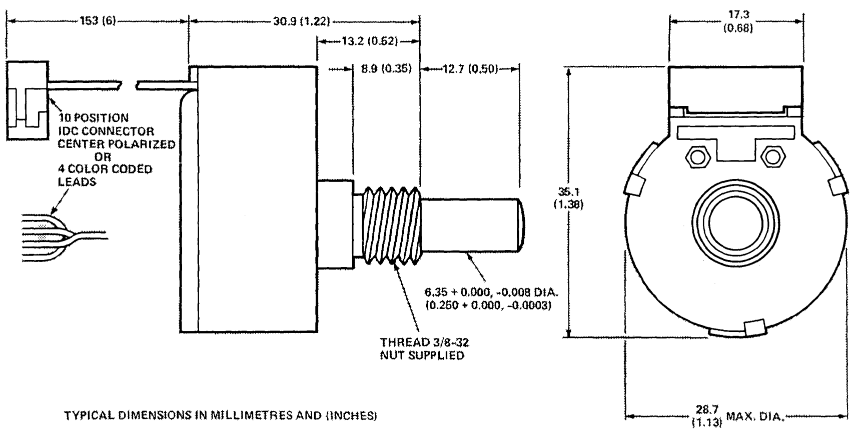
The HEDS-7500 series is a family of digital potentiometers designed for applications where a hand operated panel mounted encoder is required. The unit outputs two digital waveforms which are 90 degrees out of phase to provide resolution and direction information. 256 pulses per revolution is available as a standard resolution. The digital outputs and the 5 V supply input of the HEDS-7500 are accessed through color coded wire or through a 10 pin connector mounted on a 6 inch ribbon cable. Each digital output is capable of driving two standard TTL loads.

The HEDS-7500 emphasizes reliability by using solid state LEDs and photodiode detectors. A non-contacting slotted code wheel rotates between the LED and detector to provide digital pulses without wipers or noise. The HEDS-7500 is configured to provide standard potentiometer type panel mounting. Additional design information is available in Application Note 1025.

Applications

The HEDS-7500 series digital potentiometer may be used in applications where a manually operated knob is required to convert angular position into digital information.

Outline Drawing



TYPICAL DIMENSIONS IN MILLIMETRES AND (INCHES)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+85	°C	
Operating Temperature	T_A	-40	+85	°C	
Vibration			20	g	20 Hz - 2 kHz
Shock			30	g	11 msec
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current per Channel	I_O	-1	5	mA	
Shaft Load — Radial Axial			1 1	lbs. lbs.	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	-20	85	°C	Non-condensing atmosphere
Supply Voltage	V_{CC}	4.5	5.5	V	Ripple < 100 mV_{p-p}
Rotation Speed			300	RPM	

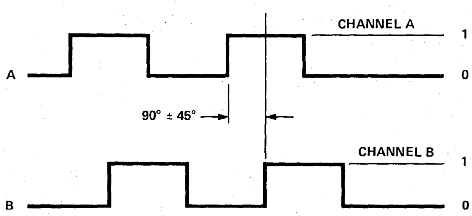
Electrical Characteristics When operating within the recommended operating range.

Electrical Characteristics Over Recommended Operating Range Typical at 25° C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		21	40	mA	
High Level Output Voltage	V_{OH}	2.4			V	$I_{OH} = -40\ \mu A$ Max.
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} = 3.2$ mA

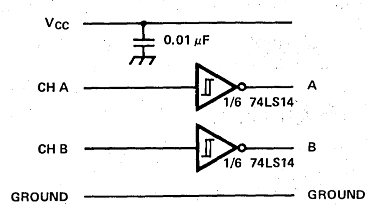
CAUTION: Device not intended for applications where coupling to a motor is required.

WAVEFORMS



CH B LEADS CH A FOR COUNTERCLOCKWISE ROTATION.
CH A LEADS CH B FOR CLOCKWISE ROTATION.

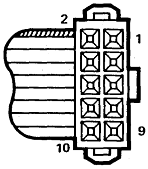
RECOMMENDED INTERFACE CIRCUIT



STANDARD 74 SERIES COULD ALSO BE USED TO IMPLEMENT THIS CIRCUIT.

TERMINATION

Ribbon Cable Termination



BOTTOM VIEW

PINOUT

PIN #	FUNCTION
1	CHANNEL A
2	V_{CC}
3	GROUND
4	N.C. OR GROUND
5	N.C. OR GROUND
6	GROUND
7	V_{CC}
8	CHANNEL B
9	V_{CC}
10	N.C.

NOTE: REVERSE INSERTION OF THE CONNECTOR WILL PERMANENTLY DAMAGE THE DETECTOR IC.

MATING CONNECTOR
BERG 65-692-001 OR EQUIVALENT

Color Coded Wire Termination

COLOR	DESIGNATION
WHITE/BLACK/RED	CHANNEL A
WHITE/BLACK/BROWN	CHANNEL B
WHITE/RED	V_{CC}
BLACK	GROUND

Ordering Information

Part Number	Description	
	PPR	Termination
HEDS-7500	256	Wire
HEDS-7501	256	Cable

HEWLETT PACKARD

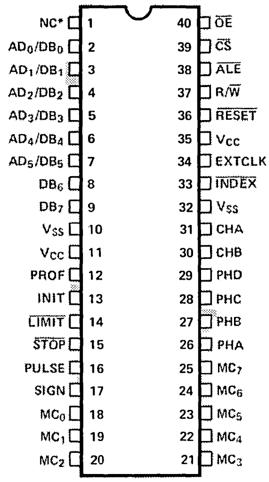
GENERAL PURPOSE MOTION CONTROL IC

HCTL-1000

TECHNICAL DATA JANUARY 1986

Features

- DC, DC BRUSHLESS AND STEPPER MOTOR CONTROL
- POSITION CONTROL
- VELOCITY CONTROL
- PROGRAMMABLE VELOCITY PROFILING
- PROGRAMMABLE DIGITAL FILTER
- PROGRAMMABLE COMMUTATOR
- PROGRAMMABLE PHASE OVERLAP
- PROGRAMMABLE PHASE ADVANCE
- GENERAL 8 BIT PARALLEL I/O PORT
- 8 BIT PARALLEL MOTOR COMMAND PORT
- PWM MOTOR COMMAND PORT
- QUADRATURE DECODER FOR ENCODER SIGNALS
- 24 BIT POSITION COUNTER
- SINGLE 5V POWER SUPPLY
- TTL COMPATIBLE
- 1 OR 2 MHz CLOCK OPERATION



*Should be left floating

PINOUT

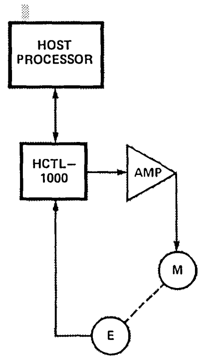
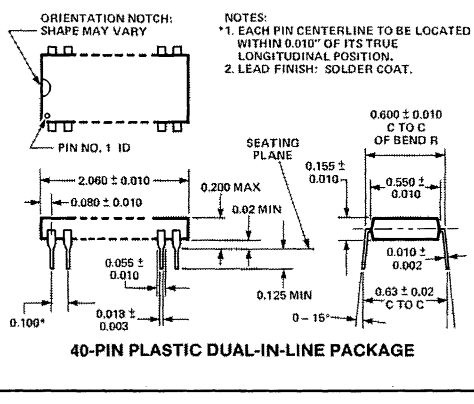


Figure 1. System Block Diagram

General Description

The HCTL-1000 is a high performance, general purpose motion control IC fabricated in Hewlett-Packard NMOS technology. It performs all the time-intensive tasks of digital motion control, thereby freeing the host processor for other tasks. The simple programmability of all control parameters provides the user with maximum flexibility and quick design of control systems with a minimum number of components. All that is needed for a complete servo system is a host processor to specify commands, an amplifier and motor with an incremental encoder. No analog compensation or velocity feedback is necessary (see Figure 1).

Package Dimensions



40-PIN PLASTIC DUAL-IN-LINE PACKAGE

Table of Contents

ESD WARNING: Since this is an NMOS device, normal precautions should be taken to avoid static damage.

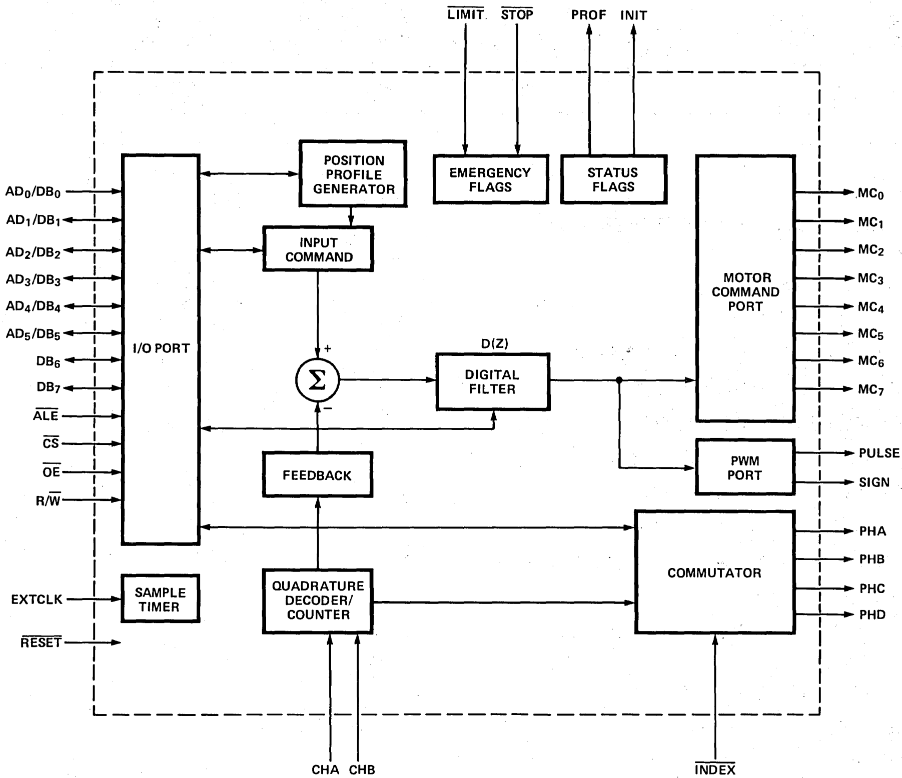


Figure 2. Internal Block Diagram

Introduction

The purpose of this section is to describe the organization of this data sheet. The front page includes the key features of the HCTL-1000, a general description of the part, the mechanical drawing and pin-out, and a Table of Contents. Following this section is the Theory of Operation, which gives the user a brief overview of how the HCTL-1000 operates by describing the internal block diagram shown in Figure 2. The following five sections give the specifications of the HCTL-1000, including Absolute Maximum Ratings, DC Characteristics, AC Characteristics, Timing Diagrams, and Functional Pin Descriptions. The final two sections include the detailed information on how to operate and interface to the HCTL-1000. The How to Operate section discusses the function and address of each software register, and describes how to use the four position and velocity control modes and the electronic commutator. The How to Interface section describes how to interface the HCTL-1000 to a microprocessor, an encoder, and an amplfier.

Theory of Operation

The HCTL-1000 is a general purpose motor controller which provides position and velocity control for dc, dc brushless and stepper motors. The internal block diagram of the HCTL-1000 is shown in Figure 2. The HCTL-1000 receives its input commands from a host processor and position feedback from an incremental encoder with quadrature output. An 8-bit bidirectional multiplexed address/data bus interfaces the HCTL-1000 to the host processor. The encoder feedback is decoded into quadrature counts and a 24-bit counter keeps track of position. The HCTL-1000 executes any one of four control algorithms selected by the user. The four control modes are:

- Position Control
- Proportional Velocity Control
- Trapezoidal Profile Control for point to point moves
- Integral Velocity Control with continuous velocity profiling using linear acceleration

The resident Position Profile Generator calculates the necessary profiles for Trapezoidal Profile Control and Integral Velocity Contol. The HCTL-1000 compares the desired position (or velocity) to the actual position (or velocity) to compute compensated motor commands using a programmable digital filter D(z). The motor command is externally available at the Motor Command Port as an 8-bit byte and at the PWM Port as a Pulse Width Modulated (PWM) signal.

The HCTL-1000 has the capability of providing electronic commutation for dc brushless and stepper motors. Using the encoder position information, the motor phases are enabled in the correct sequence. The commutator is fully programmable to encompass most motor encoder combinations. In addition, phase overlap and phase advance can be programmed to improve torque ripple and high speed performance. The HCTL-1000 contains a number of flags including two externally available flags, Profile and Initialization, which allow the user to see or check the status of the controller. It also has two emergency flags, Limit and Stop, which allow operation of the HCTL-1000 to be interrupted under emergency conditions.

The HCTL-1000 controller is a digitally sampled data system. While information from the host processor is accepted asynchronously with respect to the control functions, the motor command is computed on a discrete sample time basis. The sample timer is programmable.

Absolute Maximum Ratings

Operating Temperature .... 0°C to 70°C
Storage Temperature .... −40°C to +125°C
Supply Voltage .... −0.3 V to 7 V
Input Voltage .... −0.3 V to 7 V
Maximum Power Dissipation .... 0.95 W
Maximum Clock Frequency .... 2 MHz

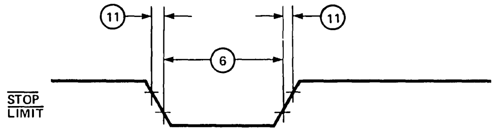
D.C. Characteristics $T_a = 0°C$ to $+70°C$; $V_{CC} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$

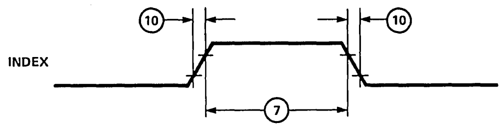
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Power Supply	V_{CC}	4.75	5.00	5.25	V	
Supply Current	I_{CC}		80	180	mA	
Input Leakage Current	I_{il}			10	μA	$V_{in} = 5.25$ V
Tristate Output Leakage Current	I_{loh}			±10	μA	$V_{out} = -0.3$ to 5.25 V
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}	−0.3		0.4	V	$I_{OL} = 2.2$ mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -200$ μA
Power Dissipation	P_D		400	950	mW	
Input Capacitance	C_{in}			20	pF	$T_a = 25°$ C, f = 1 MHz unmeasured pins returned to ground
Output Capacitance Load	C_{out}		100		pF	Same as above

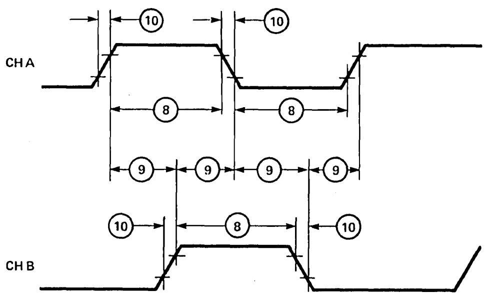
A.C. Electrical Specifications $T_a = 0$ to 70°C; $V_{CC} = 5.0$ V ± 5%; Units = nsec

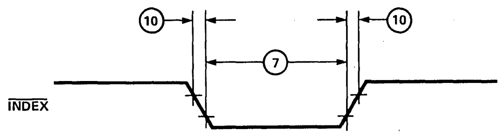
			Clock Frequency			
			2 MHz		1 MHz	
ID#	Signal	Symbol	Min.	Max.	Min.	Max.
1	Clock Period	t_{CPER}	500		1000	
2	Pulse Width, Clock High	t_{CPWH}	230		300	
3	Pulse Width, Clock Low	t_{CPWL}	200		200	
4	Clock Rise and Fall Time	t_{CR}		50		50
5	Input Pulse Width $\overline{\text{Reset}}$	t_{IRST}	2500		5000	
6	Input Pulse Width $\overline{\text{Stop}}$, $\overline{\text{Limit}}$	t_{IP}	600		1100	
7	Input Pulse Width $\overline{\text{Index}}$, Index	t_{IX}	1600		3100	
8	Input Pulse Width CHA, CHB	t_{IAB}	1600		3100	
9	Delay CHA to CHB Transition	t_{AB}	600		1100	
10	Input Rise/Fall Time CHA, CHB, Index	t_{IABR}		450		900
11	Input Rise/Fall Time $\overline{\text{Reset}}$, $\overline{\text{ALE}}$, $\overline{\text{CS}}$, $\overline{\text{OE}}$, $\overline{\text{Stop}}$, $\overline{\text{Limit}}$	t_{IR}		50		50
12	Input Pulse Width $\overline{\text{ALE}}$, $\overline{\text{CS}}$	t_{IPW}	80		80	
13	Delay Time, $\overline{\text{ALE}}$ Fall to $\overline{\text{CS}}$ Fall	t_{AC}	50		50	
14	Delay Time, $\overline{\text{ALE}}$ Rise to $\overline{\text{CS}}$ Rise	t_{CA}	50		50	
15	Address Set Up Time Before $\overline{\text{ALE}}$ Rise	t_{ASR1}	20		20	
16	Address Set Up Time Before $\overline{\text{CS}}$ Fall	t_{ASR}	20		20	
17	Write Data Set Up Time Before $\overline{\text{CS}}$ Rise	t_{DSR}	20		20	
18	Address/Data Hold Time	t_H	20		20	
19	Set Up Time, R/$\overline{\text{W}}$ Before $\overline{\text{CS}}$ Rise	t_{WCS}	20		20	
20	Hold Time, R/$\overline{\text{W}}$ After $\overline{\text{CS}}$ Rise	t_{WH}	20		20	
21	Delay Time, Write Cycle, $\overline{\text{CS}}$ Rise to $\overline{\text{ALE}}$ Fall	t_{CSAL}	1700		3400	
22	Delay Time, Read/Write, $\overline{\text{CS}}$ Rise to $\overline{\text{CS}}$ Fall	t_{CSCS}	1500		3000	
23	Write Cycle, $\overline{\text{ALE}}$ Fall to $\overline{\text{ALE}}$ Fall	t_{WC}	1830		3530	
24	Delay time, $\overline{\text{CS}}$ Rise to $\overline{\text{OE}}$ Fall	t_{CSOE}	1700		3200	
25	Delay Time, $\overline{\text{OE}}$ Fall to Data Bus Valid	t_{OEDB}	100		100	
26	Delay Time, $\overline{\text{CS}}$ Rise to Data Bus Valid	t_{CSDB}	1800		3300	
27	Input Pulse Width $\overline{\text{OE}}$	t_{IPWOE}	100		100	
28	Hold Time, Data Held After $\overline{\text{OE}}$ Rise	t_{DOEH}	20		20	
29	Delay Time, Read Cycle, $\overline{\text{CS}}$ Rise to $\overline{\text{ALE}}$ Fall	t_{CSALR}	1820		3320	
30	Read Cycle, $\overline{\text{ALE}}$ Fall to $\overline{\text{ALE}}$ Fall	t_{RC}	1950		3450	
31	Output Pulse Width, PROF, INIT, Pulse, Sign, PHA-PHD, MC Port	t_{OF}	500		1000	
32	Output Rise/Fall Time, PROF, INIT, Pulse, Sign, PHA-PHD, MC Port	t_{OR}	20	150	20	150
33	Delay Time, Clock Rise to Output Rise	t_{EP}	20	300	20	300
34	Delay Time, $\overline{\text{CS}}$ Rising to MC Port Valid	t_{CSMC}		1600		3200

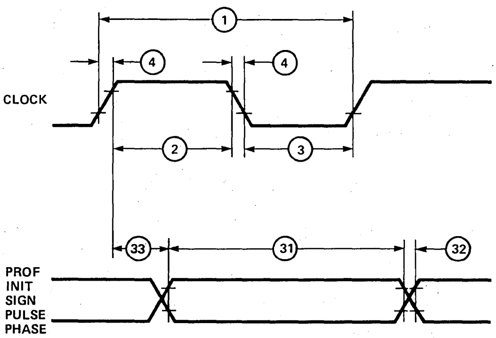
HCTL-1000 I/O Timing Diagrams

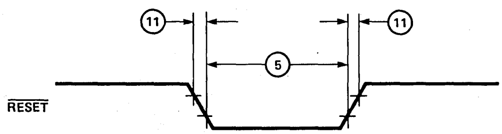










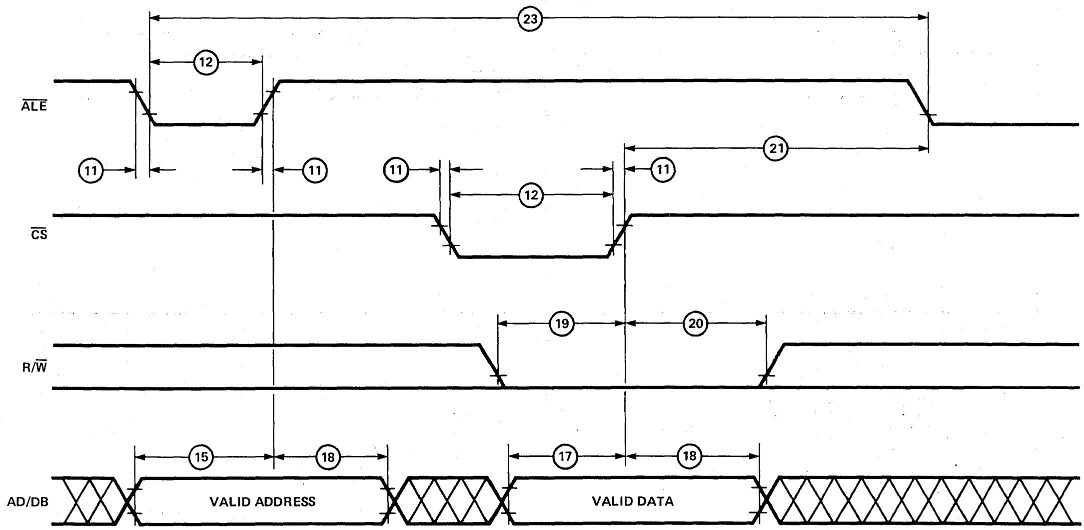


HCTL-1000 I/O Timing Diagrams

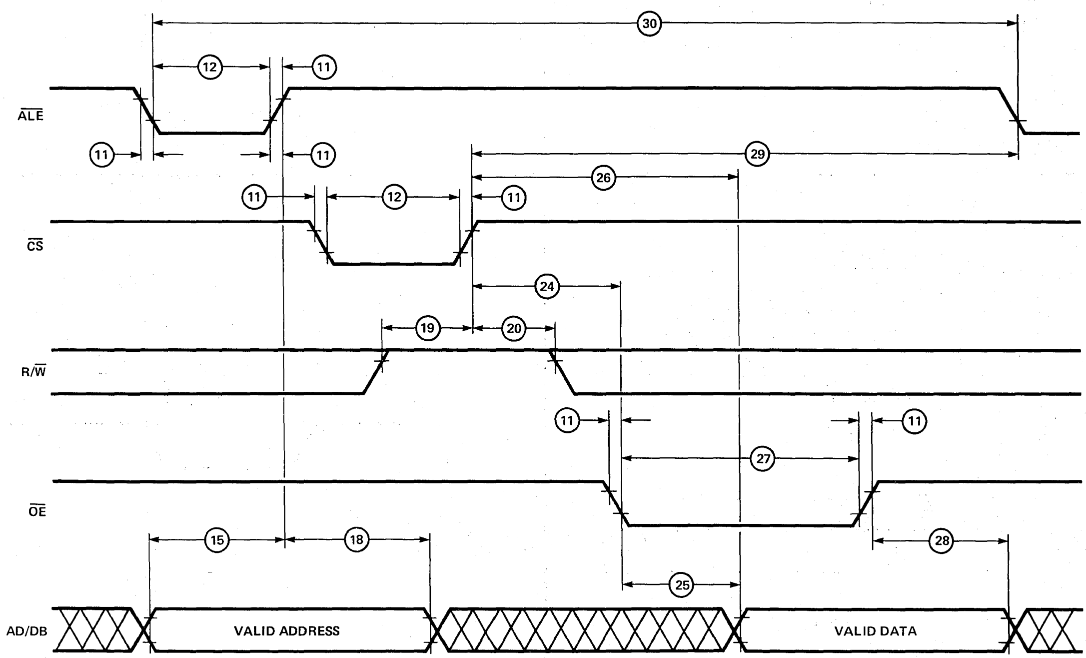
There are three different timing configurations which can be used to give the user flexibility to interface the HCTL-1000 to most microprocesors. See the I/O interface section for more details.

I. $\overline{ALE}/\overline{CS}$ NON OVERLAPPED

A. Write Cycle



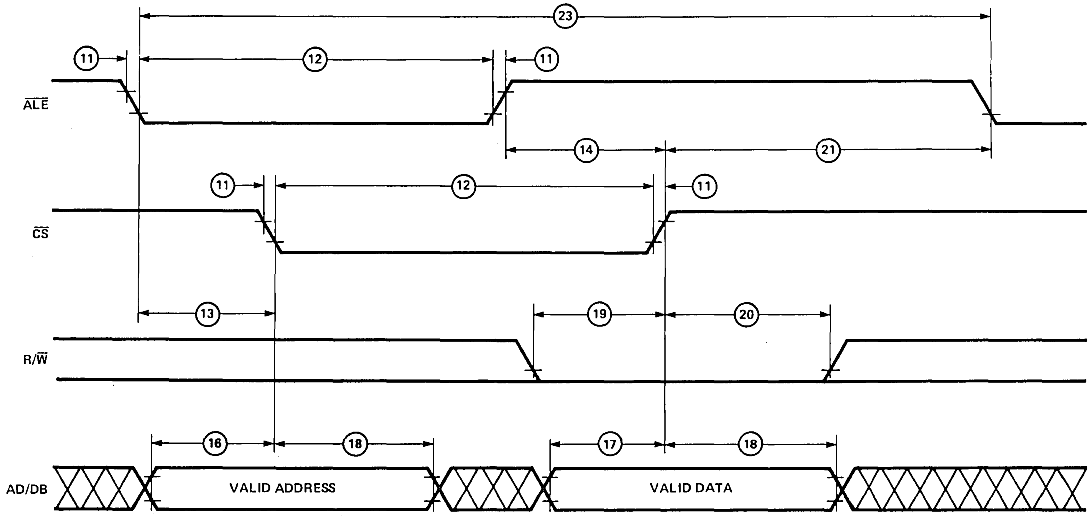
B. Read Cycle



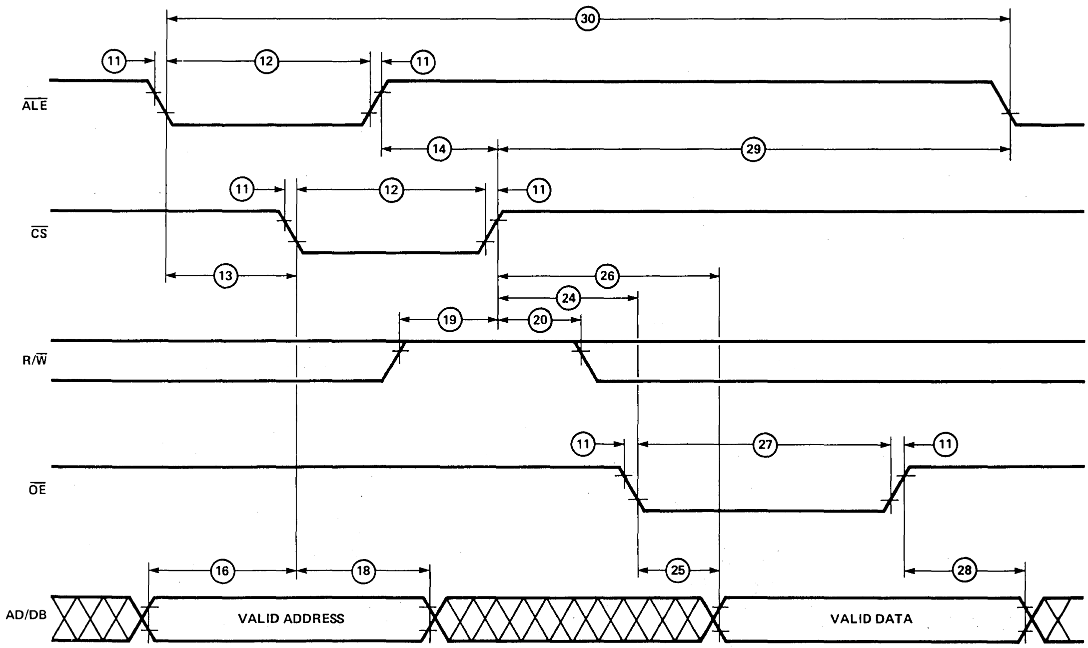
HCTL-1000 I/O Timing Diagrams

II. $\overline{ALE}$/$\overline{CS}$ OVERLAPPED

A. Write Cycle



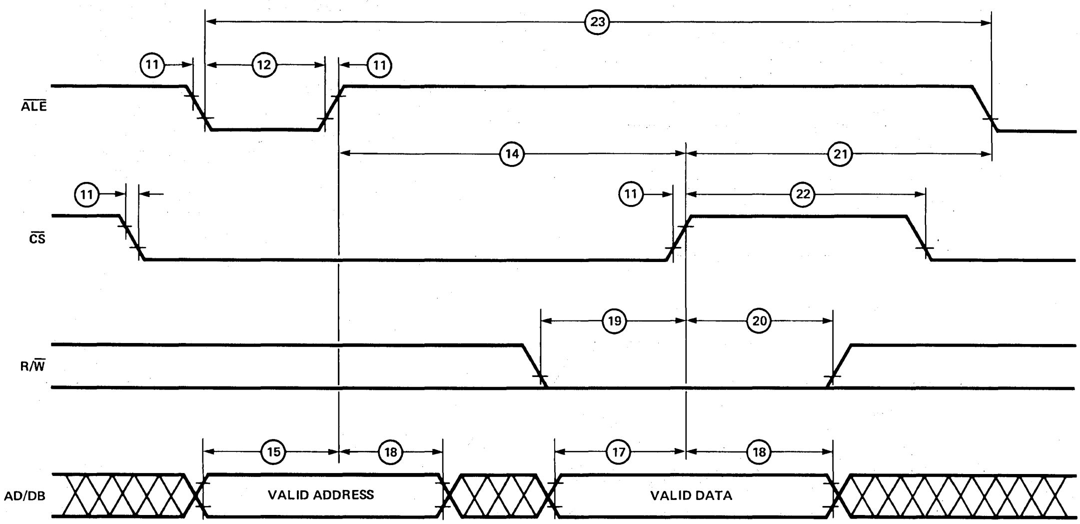
B. Read Cycle



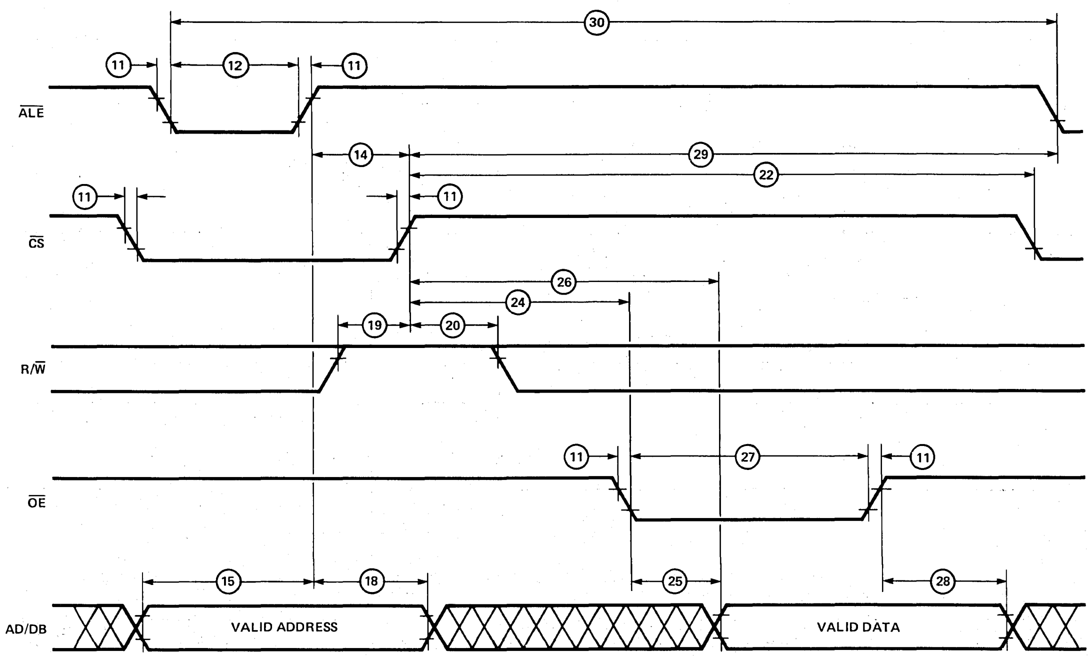
HCTL-1000 I/O Timing Diagrams

III. $\overline{ALE}$ WITHIN $\overline{CS}$

A. Write Cycle



B. Read Cycle



Functional Pin Description

INPUT/OUTPUT SIGNALS

Symbol	Pin Number	Description
AD0/DB0 — AD5/DB5	2 - 7	Address/Data bus — Low 6 bits of 8 bit I/O port which are multiplexed between address and data.
D6,D7	8, 9	Data bus — Upper 2 bits of 8 bit I/O port used for data only.

INPUT SIGNALS

Symbol	Pin Number	Description
CHA/CHB	31, 30	Channel A,B — input pins for position feedback from an incremental shaft encoder. Two channels, A and B, 90 degrees out of phase are required.
$\overline{\text{Index}}$	33	Index Pulse — input from the reference or index pulse of an incremental encoder. Used only in conjunction with the Commutator. Either a low or high true signal can be used with the Index pin. See Timing Diagrams and Encoder Interface section for more detail.
R/$\overline{\text{W}}$	37	Read/Write — determines direction of data exchange for the I/O port.
$\overline{\text{ALE}}$	38	Address Latch Enable — enables low 6 bits of external data bus into internal address latch.
$\overline{\text{CS}}$	39	Chip Select — performs I/O operation dependent on status of R/W line. For a Write, the external bus data is written into the internal addressed location. For Read, data is read from an internal location into an internal output latch.
$\overline{\text{OE}}$	40	Output Enable — enables the data in the internal output latch onto the external data bus to complete a Read operation.
$\overline{\text{Limit}}$	14	Limit Switch — an internal flag which when externally set, triggers an unconditional branch to the Initialization/Idle mode before the next control sample is executed. Motor Command is set to zero. Status of the Limit Flag is monitored in the Status Register.
$\overline{\text{Stop}}$	15	Stop Flag — an internal flag that is externally set. When flag is set during Integral Velocity control mode, the Motor Command is decelerated to a stop.
$\overline{\text{Reset}}$	36	Reset — a hard reset of internal circuitry and a branch to Reset mode.
ExtClk	34	External Clock
V_{CC}	11, 35	Voltage Supply — Both V_{CC} pins must be connected to a 5.0 volt supply.
V_{SS}	10, 32	Circuit Ground
NC	1	Not Connected — this pin should be left floating.

OUTPUT SIGNALS

Symbol	Pin Number	Description
MC0-MC7	18 - 25	Motor Command Port — 8 bit output port which contains the digital motor command adjusted for easy bipolar DAC interfacing. MC7 is the most significant bit (MSB).
Pulse	16	Pulse — Pulse Width Modulated signal whose duty cycle is proportional to the Motor Command magnitude. The frequency of the signal is External Clock/100 and pulse width is resolved into 100 external clocks.
Sign	17	Sign — gives the sign/direction of the pulse signal.
PHA-PHD	26 - 29	Phase A, B, C, D — phase enable outputs of the commutator.
Prof	12	Profile Flag — status flag which indicates that the controller is executing a profiled position move in the Trapezoidal Profile Control Mode.
Init	13	Initialization/Idle Flag — status flag which indicates that the controller is in the Initialization/Idle mode.

How to Operate the HCTL-1000 User Accessible Registers

The HCTL-1000 operation is controlled by a bank of 64 8-bit registers, 32 of which are user accessible. These registers contain command and configuration information necessary to properly run the controller chip. The 32 user accessible registers are listed in Table I. The register number is also the address. A functional block diagram of the HCTL-1000 which shows the role of the user accessible registers is also included in Figure 3. The other 32 registers are used by the internal CPU as scratch registers and should not be accessed by the user.

There are several registers which the user must configure to his application. These configuration registers are discussed in more detail below.

PROGRAM COUNTER (R05H)

The program counter, which is a write only register, executes the preprogrammed functions of the controller. The program counter is used along with the control flags F0, F3, and F5 in the Flag Register (R00H) to change control modes. The user can write any of the following four commands to the program counter.

00H — Software Reset
01H — Initialization/Idle mode
02H — Align mode
03H — Control modes; flags F0, F3, and F5 in the Flag Register (R00H) specify which control mode will be executed.

The commands written to the program counter are discussed in more detail in the section called Operating Modes and are shown in flowchart form in Figure 4.

FLAG REGISTER (R00H)

The flag register contains flags F0 thru F5. This register is also a *write only register*. Each flag is set and cleared by writing an 8-bit data word to R00H. The upper four bits are ignored by the HCTL-1000. The bottom three bits specify the flag address and the fourth bit specifies whether to set (bit=1) or clear (bit=0) the addressed flag.

Bit number	7-4	3	2	1	0
Function	Don't care	set/clear	AD2	AD1	AD0

F0 — Trapezoidal Profile Flag — set by the user to execute trapezoidal profile control. The flag is reset by the controller when the move is completed. The status of F0 can be monitored at the Profile pin (12) and in status register R07H bit 4.

F1 — Initialization/Idle Flag — set/cleared by the HCTL-1000 to indicate execution of the Initialization/Idle mode. The status of F1 can be monitored at the Initialization/Idle pin (13) and in bit 5 of the Status register (R07H). The user should never attempt to set or clear F1.

F2 — Unipolar flag — set/cleared by the user to specify bipolar (clear) or unipolar (set) mode for the Motor Command Port.

F3 — Proportional Velocity Control Flag — set by the user to specify proportional velocity control.

F4 — Hold Commutator Flag — set/cleared by the user or automatically by the Align mode. When set, this flag inhibits the internal commutator counters to allow open loop stepping of a motor by using the commutator.

F5 — Integral Velocity Control — set by the user to specify integral velocity control.

STATUS REGISTER (R07H)

The Status Register indicates the status of the HCTL-1000. Each bit decodes into one signal. All 8 bits are user readable and are decoded as shown below. Only the lower 4 bits can be written to by the user to configure the HCTL-1000. To set or clear any of the lower 4 bits, the user writes an 8-bit word to R07H. The upper 4 bits are ignored. Each of the lower 4 bits directly sets/clears the corresponding bit of the status register as shown below. For example, writing XXXX0101 to R07H sets the PWM Sign Reversal Inhibit, sets the Commutator Phase Configuration to "3 Phase", and sets the Commutator Count Configuration to "full".

Status Bit	Function	Note
0	PWM Sign Reversal Inhibit 0 = off 1 = on	Discussed in Amplifier Interface section under PWM Port.
1	Commutator Phase Configuration 0 = 3 phase 1 = 4 phase	Discussed in Commutator section
2	Commutator Count Configuration 0 = quadrature 1 = full	Discussed in Commutator section
3	Should always be set to 0	
4	Trapezoidal Profile Flag F0 1 = in Profile Control	Discussed in Operating Mode section under Trapezoidal Profile Control
5	Initialization/Idle Flag F1 1 = in Initialization/Idle Mode	Discussed in Operating Mode section under Initialization/Idle Mode
6	Stop Flag 0 = set (Stop triggered) 1 = cleared (no Stop)	Discussed in Emergency Flags Section
7	Limit Flag 0 = set (Limit triggered) 1 = cleared (no Limit)	Discussed in Emergency Flags Section

TABLE I: REGISTER REFERENCE TABLE

Register (Hex)	Function	Mode Used	Data Type	User Access
R00H	Flag Register	All	-----	w
R05H	Program Counter	All	scalar	w
R07H	Status Register	All	-----	r/w[1]
R08H	8 bit Motor Command Port	All	2's complement+80H	r/w
R09H	PWM Motor Command Port	All	2's complement	r/w
R0CH	Command Position (MSB)	Position Control	2's complement	r/w[2]
R0DH	Command Position	Position Control	2's complement	r/w[2]
R0EH	Command Position (LSB)	Position Control	2's complement	r/w[2]
R0FH	Sample Timer	All	scalar	w
R12H	Actual Position (MSB)	Position Control	2's complement	r[3]
R13H	Actual Position	Position Control	2's complement	r[3]/w[4]
R14H	Actual Position (LSB)	Position Control	2's complement	r[3]
R18H	Commutator Ring	All	scalar[5]	r/w[6]
R19H	Commutator Velocity Timer	All	scalar	w
R1AH	X	All	scalar[5]	r/w
R1BH	Y Phase Overlap	All	scalar[5]	r/w
R1CH	Offset	All	2's complement	r/w[6]
R1FH	Maximum Phase Advance	All	scalar[5]	r/w[6]
R20H	Filter Zero, A	All except Proportional Velocity	scalar	r/w
R21H	Filter Pole, B	All except Proportional Velocity	scalar	r/w
R22H	Gain, K	All	scalar	r/w
R23H	Command Velocity (LSB)	Proportional Velocity	2's complement	r/w
R24H	Command Velocity (MSB)	Proportional Velocity	2's complement	r/w
R26H	Acceleration (LSB)	Integral Velocity and Trapezoidal Profile	scalar[5]	r/w
R27H	Acceleration (MSB)	Integral Velocity and Trapezoidal Profile	scalar[5]	r/w
R28H	Maximum Velocity	Trapezoidal Profile	scalar[5]	r/w
R29H	Final Position (LSB)	Trapezoidal Profile	2's complement	r/w
R2AH	Final Position	Trapezoidal Profile	2's complement	r/w
R2BH	Final Position (MSB)	Trapezoidal Profile	2's complement	r/w
R34H	Actual Velocity (LSB)	Proportional Velocity	2's complement	r
R35H	Actual Velocity (MSB)	Proportional Velocity	2's complement	r
R3CH	Command Velocity	Integral Velocity	2's complement	r/w

Notes:
1. Upper 4 bits are read only.
2. Writing to R0EH (LSB) latches all 24 bits.
3. Reading R14H (LSB) latches data into R12H and R13H.
4. Writing to R13H clears Actual Position Counter to zero.
5. The scalar data is limited to positive numbers (00H to 7FH).
6. The commutator registers (R18H, R1CH, R1FH) have further limits which are discussed in the Commutator section of this data sheet.

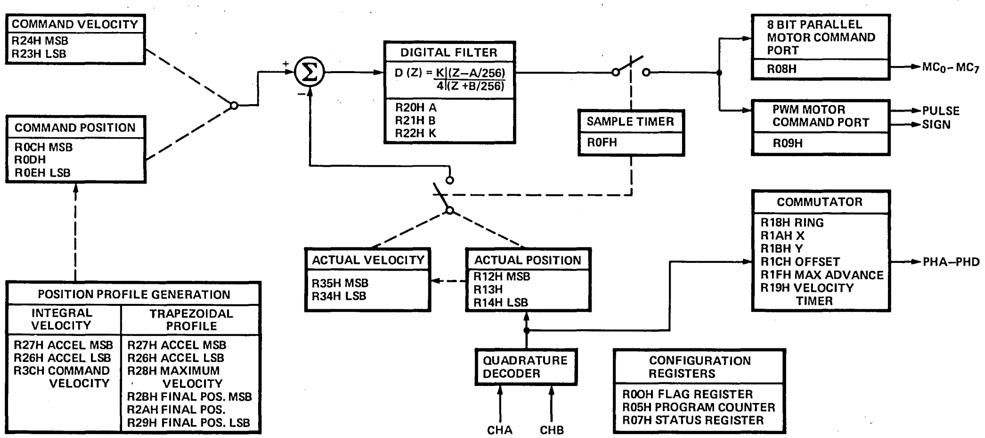


Figure 3. Register Block Diagram

EMERGENCY FLAGS — STOP AND LIMIT

Stop and Limit Flags are hardware set flags that signify the occurrence of an emergency condition and cause the controller to immediately take special action.

The Stop Flag affects the HCTL-1000 only in the Integral Velocity Mode. When the Stop Flag is set, the system will come to a decelerated stop and stay in this mode with a command velocity of zero until the Stop Flag is cleared and a new command velocity is specified.

The Limit Flag, when set in any control mode, causes the HCTL-1000 to go into the Initialization/Idle Mode, clearing the Motor Command and causing an immediate motor shutdown.

Stop and Limit Flags are set by a low level input at their respective pins (15, 14). The flags can only be cleared when the input to the corresponding pin goes high, signifying that the emergency condition has been corrected, AND a write to the Status Register (R07H) is executed. That is, after the emergency pin has been set and cleared, the flag also must be cleared by writing to R07H. Any word that is written to R07H after the emergency pin is set and cleared will clear the emergency flag, but the lower 4 bits of that word will also reconfigure the Status Register.

DIGITAL FILTER (R22H, R20H, R21H)

All control modes use some part of the programmable digital filter D(z) to compensate for closed loop system stability. The compensation D(z) has the form:

$$D(z) = \frac{K\ (z - A/256)}{4\ (z + B/256)}$$

where z = the digital domain operator

K = gain (R22H)
A = zero (R20H)
B = pole (R21H)

The compensation is a first order lead filter which in combination with the sample timer T (R0FH) affects the dynamic step response and stability of the control system. The sample timer, T, determines the rate at which the control algorithm gets executed. All parameters, A, B, K, and T, are 8-bit scalars that can be changed by the user any time.

The digital filter uses previously sampled data to calculate D(z). This old internally sampled data is cleared when the Initialization/Idle Mode is executed.

SAMPLE TIMER REGISTER (R0FH)

The contents of this register set the sampling period of the HCTL-1000. The sampling period is

$$t = 16\ (\text{R0FH} + 1)\ (1/\text{frequency of the external clock})$$

The sample timer has a limit on the minimum allowable sample time depending on the control mode being executed. The limits are given below:

	R0FH Contents Minimum Limit
Position Control	7
Proportional Velocity Control	7
Trapezoidal Profile Control	15
Integral Velocity Control	15

The maximum value of R0FH is FFH (255 decimal). For example, with a 2MHz clock, the sample time can vary from 64 μsec to 2048 μsec.

Operating Modes

The HCTL-1000 executes any one of 3 set up routines or 4 control modes selected by the user. The 3 set up routines include:

— Reset
— Initialization/Idle
— Align.

The four control modes available to the user include:

— Position Control
— Proportional Velocity Control
— Trapezoidal Profile Control
— Integral Velocity Control

The HCTL-1000 switches from one mode to another as a result of one of the following three mechanisms:

1. The user writes to the Program Counter.
2. The user sets/clears flags F0, F3, or F5 by writing to the Flag Register (R00H).
3. The controller switches automatically when certain initial conditions are provided by the user.

This section describes the function of each set up routine and control mode and the initial conditions which must be provided by the user to switch from one mode to another. Figure 4 shows a flowchart of the set up routines and control modes, and shows the commands required to switch from one mode to another.

SET UP ROUTINES

1. Reset

The Reset mode is entered under all conditions by either executing a hard reset (Reset Pin goes low) or a soft reset (write 00H to the Program Counter, R05H).

When a hard reset is executed, the following conditions occur:

— All output signal pins are held low except Sign (17), Databus (2-9), and Motor Command (18-25).

— All flags (F0 to F5) are cleared.

— The PWM port (R09H) is preset to FFH.

— The Motor Command Port (R08H) is preset to 80H.

— The Commutator logic is cleared.

— The I/O control logic is cleared.

— A soft reset is automatically executed.

When a soft reset is executed, the following conditions occur:

— The digital filter parameters are preset to

A (R20H) = E5H
B (R21H) = K (R22H) = 40H

— The sample timer (R0FH) is preset to 40H.

— The status register (R07H) is cleared.

— The Position counters (R12H, R13H and R14H) are cleared to 0.

From Reset mode, the HCTL-1000 goes automatically to Initialization/Idle mode.

2. Initialization/Idle

The Initialization/Idle mode is entered either automatically from Reset or by writing 01H to the Program Counter (R05H) under any conditions.

In the Initialization/Idle mode, the following conditions occur:

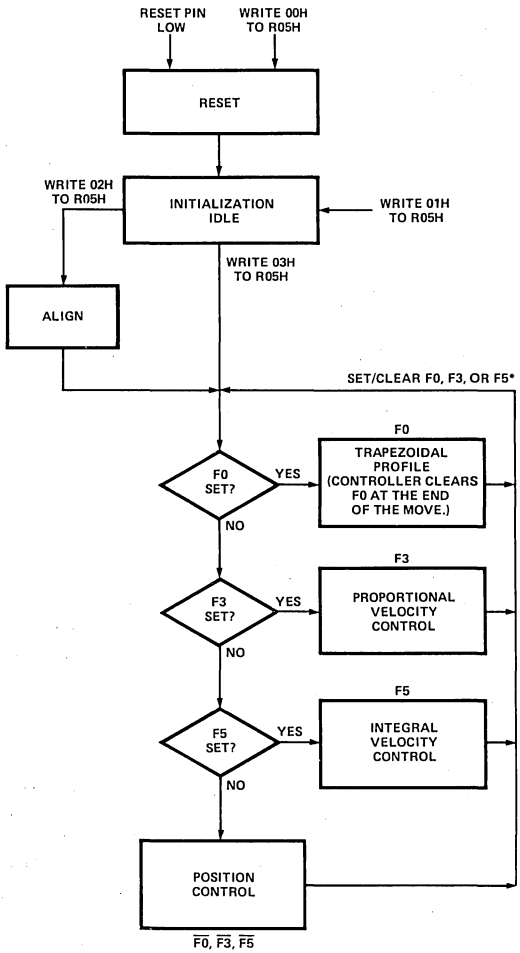
— The Initialization/Idle Flag (F1) is set.

— The PWM port (R09H) is set to 00H.

— The Motor Command port (R08H) is set to 80H.

— Previously sampled data stored in the digital filter is cleared.

It is at this point that the user should pre-program all the necessary registers needed to execute the desired control mode. The HCTL-1000 stays in this mode (idling) until a new mode command is given.



*Only one flag can be set at a time.

Figure 4. Operating Mode Flowchart

3. **Align**

The Align mode can be entered only from the Initialization/Idle mode by writing 02H to the Program Counter (R05H). This mode automatically aligns multiphase motors to the Commutator. Align mode is executed only when using the commutator feature of the HCTL-1000 and before any control modes are used.

The Align mode assumes that, during encoder/motor assembly, the encoder index pulse has been physically aligned to the last motor phase, the Commutator parameters have been correctly preprogrammed (see the section called *The Commutator* for details), and a hard reset has been executed while the motor is stationary.

The Align mode first disables the commutator and with open loop control enables the first phase (PHA) and then the last phase (PHC or PHD) to orient the motor on the last phase torque detent. Each phase is energized for 2048 system sampling periods. For proper operation, the motor must come to a complete stop during the last phase enable. Once the last phase torque detent is found, the Commutator is enabled and commutation is closed loop.

The HCTL-1000 then switches automatically from Align to the Control Modes.

CONTROL MODES

Control flags F0, F3, and F5 in the Flag Register (R00H) determine which control mode is executed. *Only one control flag can be set at a time.* After one of these control flags is set, the control modes are entered either automatically from Align or from the Initialization/Idle mode by writing 03H to the Program Counter (R05H).

1. **Position Control**
F0, F3, F5 cleared

Position Control performs point to point position moves with no velocity profiling. The user specifies a 24-bit position command, which the controller compares to the 24-bit actual position. The position error is calculated, the full digital lead compensation is applied and the motor command is output.

The controller will remain position locked at a destination until a new position command is given.

The actual and command position data is 24-bit two's complement data stored in six 8-bit registers. Position is measured in encoder quadrature counts.

The command position resides in R0CH (MSB), R0DH, R0EH (LSB). Writing to R0EH latches all 24-bits at once for the control algorithm. Therefore, the command position is written in the sequence R0CH, R0DH and R0EH. The command registers can be read in any desired order.

The actual position resides in R12H (MSB), R13H, and R14H (LSB). Reading R14H latches the upper two bytes into an internal buffer. Therefore, actual position registers are read in the order of R14H, R13H, and R12H for correct instantaneous position data. The position registers cannot be written to, but they can all be cleared to 0 by a write to R13H.

2. **Proportional Velocity Control**
F3 set

Proportional Velocity Control performs control of motor speed using only the gain factor, K, for compensation. The dynamic pole and zero lead compensation are not used.

The algorithm takes a user command velocity, calculates the actual velocity, and computes the velocity error. The velocity error is multiplied by K/4 and output as motor command.

The command and actual velocity are 16-bit two's complement words. The units of velocity are encoder quadrature counts/sample time. In addition, the command velocity is internally divided by 16 to produce fractional resolution. The 16-bit command is interpreted as 12-bits of integer and 4-bits of fraction.

R24H	R23H
IIII IIII	IIII.FFFF

COMMAND VELOCITY FORMAT

The command velocity resides in unlatched R24H (MSB) and R23H (LSB). The registers can be read or written to in any order.

The actual velocity is computed only in this algorithm and stored in scratch registers R35H (MSB) and R34H (LSB). There is no fractional component in the actual velocity registers and they can be read in any order.

The controller tracks the command velocity continuously until new mode command is given. The system behavior after a new velocity command is governed only by the system dynamics, until a steady state velocity is reached.

3. **Integral Velocity Control**
F5 set

Integral Velocity Control performs continuous velocity profiling which is specified by a command velocity and command acceleration. Figure 5 shows the capability of this control algorithm.

The user can change velocity and acceleration any time to continuously profile velocity in time. Once the specified velocity is reached, the HCTL-1000 will maintain that velocity until a new command is specified. Changes between actual velocities occur at the presently specified linear acceleration.

The command velocity is an 8-bit two's complement word stored in R3CH. The units of velocity are quadrature counts/sample time.

While the overall range of the velocity command is 8-bits, two's complement, the difference between any two sequential commands cannot be greater than 7-bits in magnitude (i.e., 127 decimal). For example, when the HCTL-1000 is executing a command velocity of 40H (+64D), the next velocity command must fall in the range of 7FH (+127D), the maximum command range, to C1H (−63D).

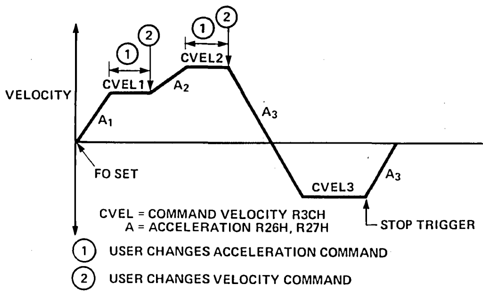


Figure 5. Integral Velocity Mode

The command acceleration is a 16-bit scalar word stored in R27H and R26H. The upper byte (R27H) is the integer part and the lower byte (R26H) is the fractional part provided for resolution. The integer part has a range of 00H to 7FH. The contents of R26H are internally divided by 256 to produce the fractional resolution.

R27H	R26H
0IIIIIII	FFFFFFFF/256
COMMAND ACCELERATION FORMAT	

The units of acceleration are quadrature counts/sample time squared.

Internally, the controller performs velocity profiling through position control. From the user specified command velocity and acceleration, the controller internally generates position profiles. In control theory terms, integral compensation has been added and therefore, this system has zero steady state velocity error.

The advantage that this mode has over Proportional Velocity modes is that the system has zero steady state velocity error. However, the drawback which comes along with this advantage is that loop stability compensation is more difficult to achieve. In the Integral Velocity Mode, the system is actually a position control system and therefore the complete dynamic compensation D(z) is used in this control mode.

If the external STOP flag F6 is set during this mode signaling an emergency situation, the controller automatically decelerates to zero velocity at the presently specified acceleration factor and stays in this condition until the flag is cleared. The user then can specify new velocity profiling data.

4. Trapezoidal Profile Control
F0 set

Trapezoidal Profile Control performs point to point position moves and profiles the velocity trajectory to a trapezoid or triangle. The user specifies only the desired final position, acceleration and maximum velocity. The controller computes the necessary profile to conform to the command data. If maximum velocity is reached before the distance halfway point, the profile will be trapezoidal, otherwise the profile will be triangular. Figure 6 shows the possible trajectories with Trapezoidal Profile control.

The command data for this control mode is a 24-bit two's complement final position written to R2BH (MSB), R2AH, and R29H (LSB). The acceleration resides in R27H (MSB) and R26H (LSB). It is the same integer and fraction

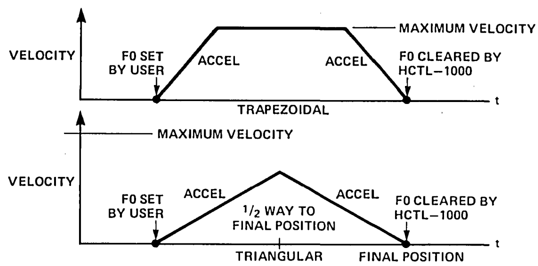


Figure 6. Trapezoidal Profile Mode

format as discussed under Integral Velocity Control. The maximum velocity is a 7-bit scalar (range is 00H to 7FH) written to R28H with units of quadrature counts/sample. The command data registers can be written/read in any order.

Once desired data is entered, flag F0 is set in the Flag Register (R00H) to commence motion (if already in Position Control). When the Trapezoidal Profile move is finished, the controller clears F0 and Position Control locks on the final position. The status of the Profile flag can be monitored in the Status Register (R07H) and at the external Profile pin. During Trapezoidal Profile move no new command data should be sent to the controller.

The internal profile generator produces a position profile using the present command position (R0CH-R0EH) as the starting point and the final position (R29H-R2BH) as the end point. The controller actually performs position control while the profile generator loads profile data into the Command Position registers. The full digital filter is applied for compensation.

Commutator

The commutator is a digital state machine that is configured by the user to properly select the phase sequence for electronic commutation of multiphase motors. The Commutator is designed to work with 2, 3, and 4 phase motors of various winding configurations and with various encoder counts.

Besides the correct phase enable sequence, the Commutator provides programmable phase overlap and phase advance. Phase overlap is used for better torque ripple control. It can also be used to generate unique state sequences which can be further decoded externally to drive more complex amplifiers and motors.

Phase advance allows the user to compensate for the frequency characteristics of the motor/amplifier combination. By advancing the phase enable command (in position), the delay in reaction of the motor/amplifier combination can be offset and higher performance can be achieved.

The ouput of the Commutator is on PHA (26) to PHD (29). The inputs to the Commutator are the three encoder signals, Channel A, Channel B, and Index, and the configuration data stored in registers.

The Commutator uses both channels and the index pulse of an incremental encoder. The index pulse of the encoder must be physically aligned to a known torque curve location because it is used as the reference point of the rotor position with respect to the Commutator phase enables.

The index pulse should be permanently aligned during motor encoder assembly to the last motor phase. This is done by energizing the last phase of the motor during assembly and permanently attaching the encoder codewheel to the motor shaft such that the index pulse is active. Fine tuning of alignment for commutation purposes is done electronically by the Offset Register (R1CH) once the complete control system is set up.

1. Commutator Configuration Registers

The Commutator is programmed by the data in the following registers. Figure 7 shows an example of the relationship between all the parameters.

Status Register (R07H)

Bit #1 — 0 = 3 phase configuration, PHA, PHB, and PHC are active outputs.
1 = 4 phase configuration, PHA - PHD are active outputs.

Bit #2 — 0 = rotor position measured in quadrature counts.
1 = rotor position measured in full counts.

RING REGISTER (R18H)

The ring register is scalar and determines the length of the electrical cycle measured in full or quadrature counts as set by bit #1 in R07H. The magnitude of Ring is limited to 7FH.

X REGISTER (R1AH)

Scalar data which sets the interval during which a phase is the only one active.

Y REGISTER (R1BH)

Scalar data which sets the interval during which two sequential phases are both active. Y is phase overlap.

X and Y must be such that:

X + Y = Ring/(# of phases)

These three parameters define the basic electrical commutation cycle.

OFFSET REGISTER (R1CH)

The offset is two's complement data which determines the relative start of the electrical cycle with respect to the index pulse. Since the index pulse must be physically referenced to the rotor, offset performs fine alignment between the electrical and mechanical torque cycles.

PHASE ADVANCE REGISTERS (R19H, R1FH)

The phase advance feature performs the function of linearly incrementing the phase advance according to measured speed of rotation up to a set maximum.

VELOCITY TIMER REGISTER (R19H)

This register contains scalar data which determines the amount of phase advance at a given velocity. The phase advance is interpreted in the units set for the Ring counter by bit #1 in R07H. The velocity is measured in revolutions/second.

$$\text{Advance} = Nv\Delta t$$

$$\text{where } \Delta t = \frac{16\,(\text{R19H}+1)}{f \text{ external clk}}$$

N = encoder counts/revolution

v = velocity (revolutions/second)

3 PHASE
FULL COUNTS
RING: 9

ENCODER: 90 COUNTS/REVOLUTION

CASE	1	2	3	4
X	3	2	2	2
Y	0	1	1	1
OFFSET	0	0	2	2
ADVANCE	0	0	0	1

INDEX PULSE OCCURS AT THE ORIGIN

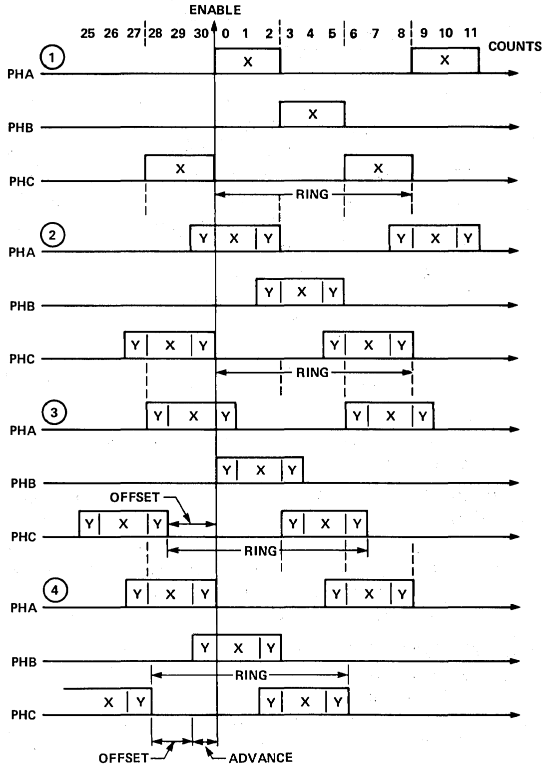


Figure 7. Commutator Configuration

MAXIMUM ADVANCE REGISTER (R1FH)

The scalar data sets the upper limit for phase advance regardless of rotor speed.

Figure 8 shows the relationship between the phase advance registers. Note: If the phase advance feature is not used, set both R19H and R1FH to 0.

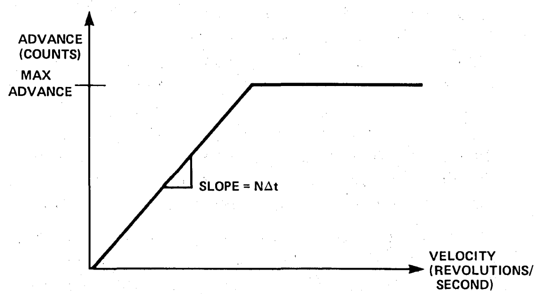


Figure 8. Phase Advance vs. Motor Velocity.

COMMUTATOR CONSTRAINTS

There are several numerical constraints the user should be aware of to use the Commutator.

The parameters of *Ring, X, Y,* and *Max Advance* must be positive numbers (00H to 7FH). Additionally, the following equation must be satisfied:

$$80H \le \frac{3}{2}\text{Ring} + \text{Offset} \pm \text{Max Advance} \le 7FH \quad (1)$$

In order to utilize the greatest flexibility of the Commutator, it must be realized that the Commutator works on a circular ring counter principle, whose range is defined by the Ring Register (R18H). This means that for a ring of 96 counts and a needed offset of 10D, numerically the Offset Register can be programmed as 0AH (10D) or D0H (−80D), the latter satisfying Equation 1.

Example: Suppose you want to commutate a 3 phase 15 deg/step Variable Reluctance Motor attached to a 192 count encoder.

1. Select 3 phase and quadrature mode for commutator by writing 0 to R07H.
2. With a 3 phase 15 degree/step Variable Reluctance Motor the torque cycle repeats every 45 degrees or 360 deg/45 deg/revolution.
3. $\text{Ring Register} = \dfrac{(4)\,(192)\ \text{counts/revolution}}{8/\text{revolution}}$

   $= 96$ quadrature counts
4. By measuring the motor torque curve in both directions, it is determined that an offset of 3 degrees, and a phase overlap of 2 degrees is needed.

   $$\text{Offset} = 3° \ \frac{(4)\,(192)}{360°} \simeq 6 \text{ quadrature counts}$$

   To numerically satisfy the commutator write A6H (−90D) to Offset Register (R1CH).

   $$y = \text{overlap} = \frac{(2°)\,(4)\,(192)}{360°} \simeq 4$$

   $$\frac{x + y}{3} = 96$$

   Therefore, $x = 28$
   $y = 4$

   For the purposes of this example, the Velocity Timer and Maximum Advance are set to 0.

How to Interface to the HCTL-1000

I/O INTERFACE

The HCTL-1000 looks to the user like a bank of 8-bit registers which the user can read/write. The data in these registers control the operation of the HCTL-1000. The user communicates with these registers over an 8-bit address/data multiplexed bidirectional bus. The four I/O control lines, $\overline{\text{ALE}}$, $\overline{\text{CS}}$, $\overline{\text{OE}}$ and R/$\overline{\text{W}}$, execute the data transfers.

There are three different timing configurations which can be used to give the user greater flexibility to interface the HCTL-1000 to most microprocessors (see Timing diagrams). They are differentiated from one another by the arrangement of the $\overline{\text{ALE}}$ signal with respect to the $\overline{\text{CS}}$ signal. The three timing configurations are listed below.

1. $\overline{\text{ALE}}$, $\overline{\text{CS}}$ non-overlapped
2. $\overline{\text{ALE}}$, $\overline{\text{CS}}$ overlapped
3. $\overline{\text{ALE}}$ within $\overline{\text{CS}}$

Any I/O operation starts by asserting the $\overline{\text{ALE}}$ signal which starts sampling the external bus into an internal address latch. Rising $\overline{\text{ALE}}$ or falling $\overline{\text{CS}}$ during $\overline{\text{ALE}}$ stops the sampling into the address latch.

$\overline{\text{CS}}$ low after rising $\overline{\text{ALE}}$ samples the external bus into the data latch. Rising $\overline{\text{CS}}$ stops the sampling into the data latch, and starts the internal synchronous process.

In the case of a write, the data in the data latch is written into the addressed location. In the case of a read, the addressed location is written into an internal output latch. $\overline{\text{OE}}$ low enables the internal output latch onto the external bus. The $\overline{\text{OE}}$ signal and the internal output latch allow the I/O port to be flexible and avoid bus conflicts during read operations.

The I/O Port is designed to work with most microprocessor systems and is easily fitted in as part of addressable RAM.

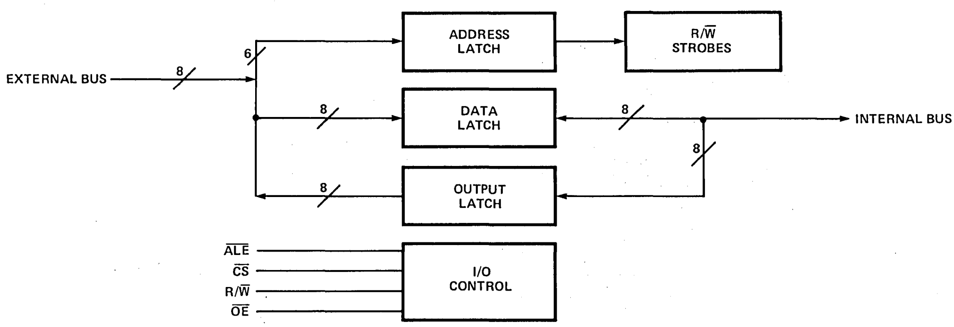


Figure 9. I/O Port Block Diagram

ENCODER INTERFACE

The HCTL-1000 accepts TTL compatible outputs from 2 or 3 channel incremental shaft encoders such as the HEDS-5000 and 6000 series. Channels A and B are internally decoded into quadrature counts which increment or decrement the 24-bit position counter. For example, a 500 count encoder is decoded into 2000 quadrature counts per revolution. The position counter will be incremented when Channel B leads Channel A. The Index channel is used only for the Commutator and its function is to serve as a reference point for the internal Ring Counter.

The inputs to the quadrature decoder from Channel A and B, have a 3-bit state delay filter to filter out unwanted noise spikes on the encoder input lines. Any transition on the input pins must be stable during 3 consecutive external clock edges before it is qualified internally as a legitimate transition. This 3-bit state delay filter, together with the quadrature decoder, impose a limit on the encoder frequency.

The AC specifications give the delay requirements between encoder signal edges. When calculating the encoder frequency limit, the user must take into consideration the external clock frequency and the encoder state width error.

The index signal of an encoder is used in conjunction with the Commutator. It resets the internal ring counter which keeps track of the rotor position so that no cumulative errors are generated.

The Index pin of the HCTL-1000 also has a 3-bit filter on its input. The Index pin is *active low and level transition sensitive.* It detects a valid high to low transition and qualifies the low input level through the 3-bit filter. At this point, the Index signal is internally detected by the commutator logic. This type of configuration allows an Index or $\overline{\text{Index}}$ signal to be used to generate the reference mark for commutator operation as long as the AC specifications for the Index signal are met.

AMPLIFIER INTERFACE

The HCTL-1000 outputs a motor command in two forms: an 8-bit Motor Command which can be connected to a DAC to drive a linear amplifier and PULSE and SIGN output to drive a PWM amplifier.

All control algorithms internally compute an error between the desired command and actual feedback which is processed through the digital filter. The result is an internal 8-bit 2's complement motor command. Before the internal motor command is made externally available, it is additionally adjusted for different output formats and ease of interfacing to external hardware. The sections below discuss the externally available amplifier interfaces and their formats. Tables II and III summarize the amplifier interface outputs.

8-Bit Parallel Motor Command Port

The 8-bit Motor Command Port consists of register R08H whose data goes directly to external pins MC0-MC7. MC7 is the most significant bit. R08H can be read and written to, however, it should be written to only during Initialization/Idle mode. During any of the four Control Modes, the controller writes the motor command into R08H.

The Motor Command Port is the ideal interface to an 8-bit DAC, configured for bipolar output. The data written to the 8-bit Motor Command Port by the control algorithms is the internally computed 2's complement motor command with an 80H offset added. This allows direct interfacing to a DAC. Figure 10 shows a typical DAC interface to the HCTL-1000. An inexpensive DAC, such as MC1408 or equivalent, has its digital inputs directly connected to the Motor Command Port. The DAC produces an output current which is converted to a voltage by an operational amplifier. R_O and R_G control the analog offset and gain. The circuit is easily adjusted for +5V to −5V operation by first writing 80H to R08H and adjusting R_O for 0V output. Then FFH is written to R08H and R_G is adjusted until the output is 5V. Note that 00H in R08H corresponds to −5V out.

The above interface is suitable to drive linear amplifiers and DC motors because of the bipolar output. When using commutated motors, the direction of rotation of the motor is governed by the order of firing the motor phases which is under commutator control. In this case, it is desirable to have the Motor Command be unipolar to specify magnitude only, not direction. The HCTL-1000 has the feature of digitally configuring the 8-bit Motor Command Port into unipolar mode. Flag F2 in the Flag Register R00H controls this function.

F2 clear — Bipolar mode
F2 set — Unipolar mode

This mode functions such that, with the same circuit in Figure 10 (or any DAC configured for similar bipolar operation) setting F2 will cause the DAC to output from 0V to 5V only and to digital data on pins MC0 to MC7 to be restricted in the control modes from 80H to FFH. Internally the commutator keeps track of the sign of the motor command for proper commutation of the motor.

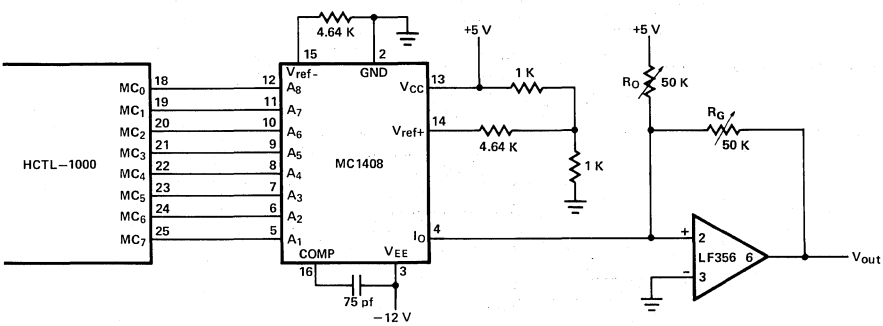


Figure 10. Linear Amplifier Interface

Internally, the HCTL-1000 operates on data of 24, 16 and 8-bit lengths to produce the 8-bit motor command, available externally. Many times the computed motor command will be greater than 8-bits. At this point, the motor command is saturated by the controller. The saturated value output by the controller is not the full scale value 00H, or FFH. The saturated value is adjusted to 0FH (negative saturation) and F0H (positive saturation). Saturation levels for the Motor Command Port are also included in Table II.

PWM Port

The PWM port outputs the motor command as a pulse width modulated signal with the correct sign of polarity. The PWM Port consists of the Pulse and Sign pins (pins 16 and 17) and R09H.

The PWM signal at the Pulse pin has a frequency of External Clock/100 and the duty cycle is resolved into the 100 clocks.

The Sign pin gives the polarity of the command. Low output on Sign pin is positive polarity.

The 2's complement contents of R09H determine the duty cycle and polarity of the PWM command. For example, D8H (−40D) gives a 40% duty cycle signal at the Pulse pin and forces the Sign pin high. Data outside the 64H (+100D) to 9CH (−100D) linear range gives 100% duty cycle. R09H can be read and written to. However, the user should only write to R09H when the controller is in the Initialization/Idle mode. Table II gives the PWM output vs the internal motor command.

When any Control Mode is being executed, the unadjusted internal 2's complement motor command is written to R09H. Because of the hardware limit on the linear range (64H to 9CH; ±100D), the PWM port saturates sooner than the 8-bit Motor Command Port (00H to FFH; +127D to −128D). When the internal Motor Command saturates above 8 bits, the PWM Port is saturated to the full ±100% duty cycle level. Table III gives the actual values inside the PWM port. Note that the unipolar Flag, F2, does *not* affect the PWM port.

TABLE II. MOTOR COMMAND PORT OUTPUTS

Functional Condition During Control Modes	Internal Motor Command 2's Complement	Motor Command Port R08H, MC0-MC7		DAC Output	
		Bipolar F2 = 0	Unipolar F2 = 1	Biploar F2 = 0	Unipolar F2 = 1
Minimum Motor Command	80H	00H	FFH	−5.0 V	5.0 V
Negative Internal Motor Command Saturation	< 80H	0FH	F0H	−4.4 V	4.4 V
Zero Motor Command	00H	80H	80H	0 V	0 V
Position Internal Motor Command Saturation	> 7FH	F0H	F0H	4.4 V	4.4 V
Maximum Motor Command	7FH	FFH	FFH	5.0 V	5.0 V

TABLE III. PWM PORT OUTPUTS

Functional Condition During Control Modes	Internal Motor Command	PWM Port		
		R09H	Pulse Duty Cycle	Sign
Minimum Motor Command	80H	80H	100%	High
Negative Internal Motor Command Saturation	< 80H	8FH	100%	High
Minimum PWM Linear Range	9CH	9CH	100%	High
Zero Motor Command	00H	00H	0%	Low
Positive Internal Motor Command Saturation	> 7FH	70H	100%	Low
Maximum PWM Linear Range	64H	64H	100%	Low
Maximum Motor Command	7FH	7FH	100%	Low

The PWM port has an option that can be used with H bridge type amplifiers. The option is Sign Reversal Inhibit, which inhibits the Pulse output for one PWM period after a sign polarity reversal. This allows one pair of transistors to turn off before others are turned on and thereby avoids a short across the power supply. Bit 0 in the Status Register (R07H) controls the sign reversal inhibit option. Figure 11 shows the output of the PWM port when Bit 0 is set.

Figure 12 shows an example of how to interface the HCTL-1000 to an H bridge amplifier (amplifier schematic is simplified). An H bridge amplifier works such that either Q1 and Q4 conduct or Q2 and Q3 conduct. This allows for bipolar motor operation with a unipolar power supply. The Sign Reversal Inhibit feature prevents all transistors from being on at the same time when the direction of motion is reversed.

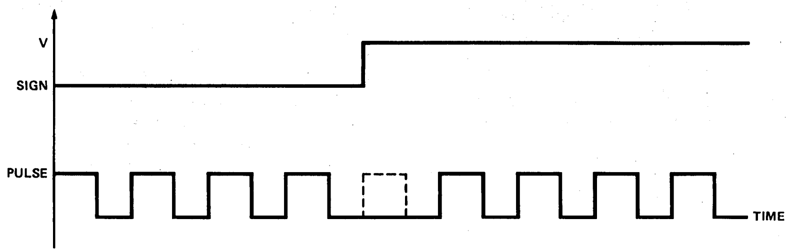


Figure 11. Sign Reversal Inhibit

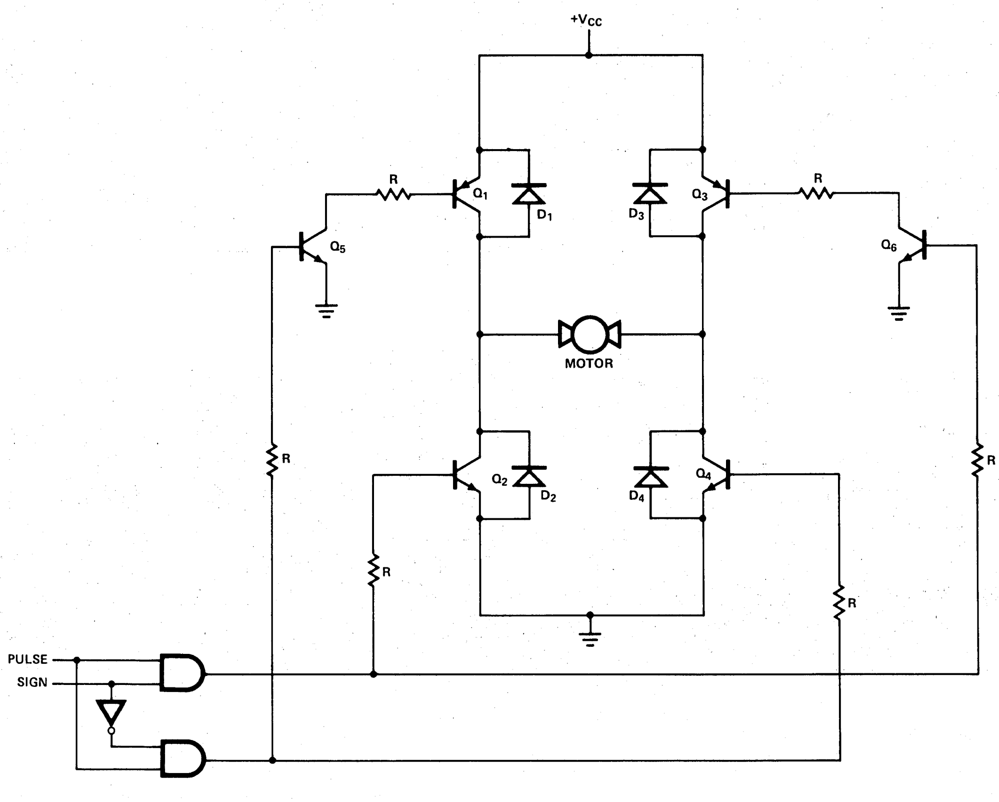


Figure 12. H-Bridge Amplifier Interface

HEWLETT PACKARD

QUADRATURE DECODER/ COUNTER INTERFACE IC

HCTL-2000

TECHNICAL DATA JANUARY 1986

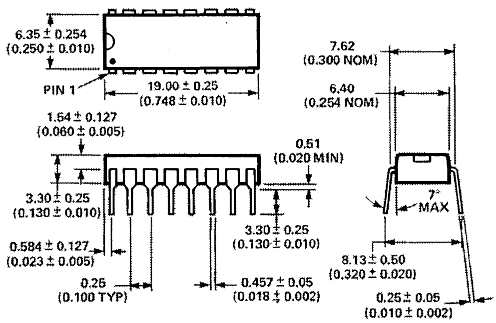
Features

- FULL FUNCTION IN A SPACE SAVING PACKAGE
- SUBSTANTIALLY REDUCED SYSTEM SOFTWARE
- FULL 4X DECODE
- HIGH NOISE IMMUNITY:
  SCHMITT TRIGGER INPUTS
  DIGITAL NOISE FILTER
- 8 BIT TRISTATE INTERFACE
- 12 BIT BINARY UP/DOWN COUNTER TO BUFFER THE CONTROL PROCESSOR
- 12 BIT LATCH AND INHIBIT LOGIC PROVIDE A STABLE, 2 BYTE READ OPERATION
- 8 AND 12 BIT OPERATING MODES

Description

The HCTL-2000 is an HCMOS IC that performs the quadrature decoder, counter, and bus interface function. The HCTL-2000 is designed to improve system performance in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The HCTL-2000 consists of a 4x quadrature decoder, 12 bit binary up/down state counter, and 8 bit bus interface. The use of Schmitt triggered CMOS inputs and a 3 bit state delay filter allows reliable operation in noisy environments. The HCTL-2000 provides LSTTL compatible tri-state output buffers. Operation is specified for a temperature range from -40 to +85° C at clock frequencies up to 3.9 mHz.

Package Dimensions



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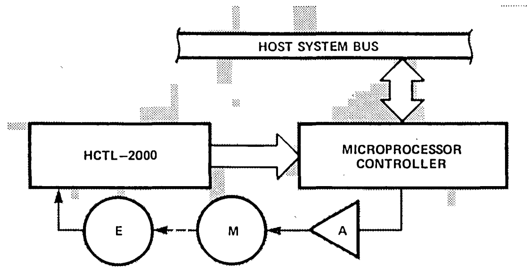
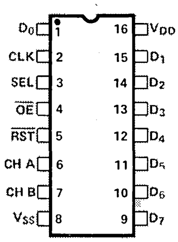
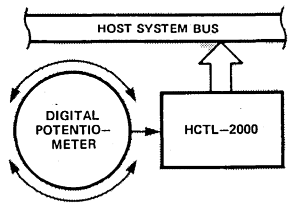


DIGITAL MOTION CONTROL



PINOUT



DIGITAL DATA ENTRY

Applications

- INTERFACE QUADRATURE INCREMENTAL ENCODERS TO MICROPROCESSORS
- INTERFACE DIGITAL POTENTIOMETERS TO DIGITAL DATA INPUT BUSSES

Table of Contents

ESD WARNING: HCTL-2000 is implemented in a standard HCMOS process with diode protection of all I/O pads. Standard precautions for handling HCMOS devices should be observed.

Operating Characteristics

Table 1. Absolute Maximum Ratings (all voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{dd}	–0.3 to +7	V
Input Voltage	V_{in}	–0.3 to V_{dd} +0.3	V
Storage Temperature	T_s	–40 to +125	°C
Operating Temperature	T_a[1]	–40 to +85	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{dd}	+3 to +6	V
Ambient Temperature	T_a[1]	–40 to +85	°C

Table 3. DC Characteristics V_{dd} = 5V ± 5%; T_a = –40 to +85° C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{il}[2]	Low-Level Input Voltage				1.5	V
V_{ih}[2]	High-Level Input Voltage		3.5			V
V_{t+}[2]	Schmitt-Trigger Positive-Going Threshold			3.0	4.0	V
V_{t-}[2]	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
V_h	Schmitt-Trigger Hysteresis		1.0	1.5		V
I_{in}	Input Current	$V_{in} = V_{dd}$ $V_{in} = V_{ss}$	–10 –10	1 1	+10 +10	μA μA
V_{oh}[2]	High-Level Output Voltage	I_{oh} = –1.6mA	2.4	4.5		V
V_{ol}[2]	Low-Level Output Voltage	I_{ol} = +1.6mA		0.2	0.4	V
I_{oz}	High-Z Output Leakage Current	$V_o = V_{ss}$ or V_{dd}	–10	1	+10	μA
I_{dd}	Quiescent Supply Current	$V_{in} = V_{ss}$ or V_{dd} V_d = HiZ		60		μA
C_{in}	Input Capacitance	Any Input[3]		5		pF
C_{out}	Output Capacitance	Any Output[3]		7		pF

NOTES:
1. Free Air.
2. In general, for any V_{dd} between the allowable limits (+3V to +6V), $V_{il} = 0.3V_{dd}$ and $V_{ih} = 0.7V_{dd}$; V_t+ and V_t– vary as Fig 1; $V_{oh} = V_{dd}$ – 0.5V and $V_{ol} = V_{ss}$ + 0.2V @ (±) 1.6 ma respectively.
3. Excluding package capacitance.

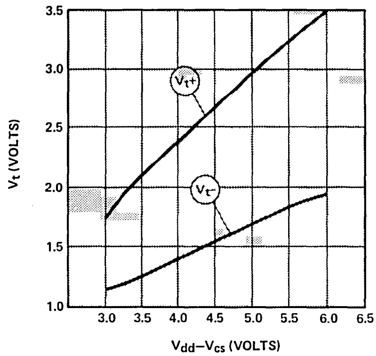


Figure 1. Typical Schmitt Trigger Input Threshholds

Functional Pin Descriptions

Table 4. Functional Pin Descriptions

Symbol	Pin	Description
V_{dd}	16	Power Supply
V_{ss}	8	Ground
CLK	2	The rising edge of this Schmitt trigger input controls the sampling of the CHA and CHB inputs, and the clocking of the input of the noise filters, decoder, counter and internal data latch. The falling edge of the CLK input controls the sampling of the OE and SEL inputs to control the inhibit logic.
CHA	6	CHA and CHB are Schmitt trigger inputs which accept the output from a quadrature encoded source, such as an incremental optical shaft encoder. The 4x decoding into states produces count and direction information where the number of states is 4 times the number of pulses on CHA or CHB (See Figure 8). Non-ideal state width affects the relationship between the clock frequency and the maximum encoder line frequency: See "Digital Filter" and "Quadrature Decoder" section.
CHB	7	
$\overline{RST}$	5	This active low Schmitt trigger input clears the internal 12 bit up/down position counter and the position latch. It also resets the inhibit logic. $\overline{RST}$ is asynchronous with respect to any other input signals. $\overline{RST}$ does not clear the input filter state machine nor the decoder state machine.
$\overline{OE}$	4	This HCMOS active low input directly controls the tri-state output buffers. In addition, the $\overline{OE}$ and SEL inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch. The above operation constrains the timing of $\overline{OE}$ and SEL to be synchronous with the falling clock edge during two byte read operations. See "Inhibit Logic".
SEL	3	This HCMOS input directly controls which data byte from the position latch is enabled into the 8 bit tri-state output buffer. As in $\overline{OE}$ above, SEL also controls the internal inhibit logic. SEL / BYTE SELECTED: 0 / high 1 / low
D0	1	These LSTTL compatible tri-state outputs form an 8 bit output port through which the contents of the 12 bit position latch may be read in 2 sequential bytes. Inhibit logic disables the position data latch inputs at the start of the read operation to hold the data stable throughout the 2 byte read operation. Once commenced, this sequence must be completed, or $\overline{RST}$ must be used to reset the inhibit logic, with resulting data loss. The high byte, containing bits 8-11, is read first. The most significant 4 bits of this byte are set to 0 internally. The lower byte, bits 0-7, is read second.
D1	15	
D2	14	
D3	13	
D4	12	
D5	11	
D6	10	
D7	9	

Switching Characteristics

Table 5. Switching Characteristics Min/Max specifications at V_{dd} = 5.0 ± 5%, T_a = −40 to +85° C; Typicals are representative of V_{dd} = 5.0V, T_{case} = 25° C

		Symbol Description	Min.[1]	Typ.[2]	Max.[1]	Units
1	T_{clk}	Rising edge to rising edge of clock period	255	136	—	ns
2	T_{chh}	Minimum clock high hold time	125	70	—	ns
3	T_{cd}[3]	Delay from rising edge of clock to valid, updated count information on D0-7	—	126	230	ns
4	T_{ode}[5]	OE to valid data on D0-7	—	47	86	ns
5	T_{odz}	OE delay to Hi-Z state on D0-7	—	30	55	ns
6	T_{sdv}[4]	SEL valid to stable, selected data byte, delay to High Byte=delay to Low Byte	—	71	129	ns
7	T_{clh}	Minimum clock low hold time	35	20	—	ns
8	T_{ss}[6]	SEL setup time prior to falling clock edge	36	20	—	ns
9	T_{os}[6]	OE setup time prior to falling clock edge	31	17	—	ns
10	T_{sh}[6]	Hold time of SEL after falling clock edge	0	—	—	ns
11	T_{oh}[6]	Hold time of OE after falling clock edge	0	—	—	ns
12	T_{rst}	RST active low hold time	50	27	—	ns
13	T_{dcd}	Output Delay Time: Last Position Count Stable on D0-7 after Rising Clock Edge.	5	36	—	ns
14	T_{dsd}	Output Delay Time: Last Data Byte Stable after next SEL state change.	4	31	—	ns
15	T_{dod}	Output Delay Time: Data Byte Stable after $\overline{OE}$ Rising Edge	3	25	—	ns

NOTES:

1. All times specified from valid logic level to valid logic level of relevant I/O pins. Conformance to these limits is necesary to insure proper operation over T_a = −40 to +85° C.
2. Typical times are for reference only.
3. T_{cd} specification and waveform assume valid stable SEL and $\overline{OE}$ from T = −∞
4. T_{sdv} specification and waveform assume data stable and valid on internal multiplexer inputs prior to the SEL transition.
5. T_{ode} specification and waveform assume data stable on buffer inputs.
6. T_{ss}, T_{os}, T_{sh}, T_{oh} only pertain to proper operation of the inhibit logic. In other cases, such as 8 bit read operations, these setup and hold times do not need to be observed.

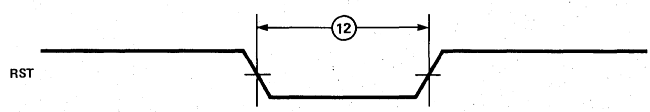


Figure 2. Reset Waveform

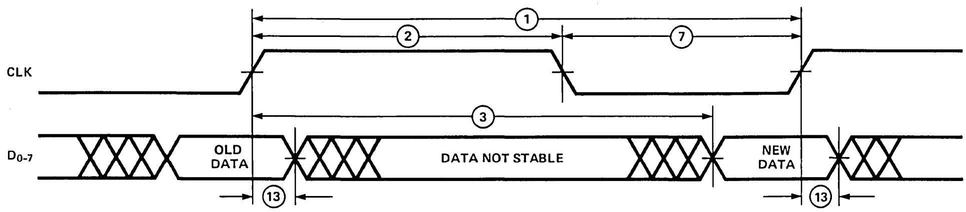


Figure 3. Waveforms for Positive Clock Edge Related Delays

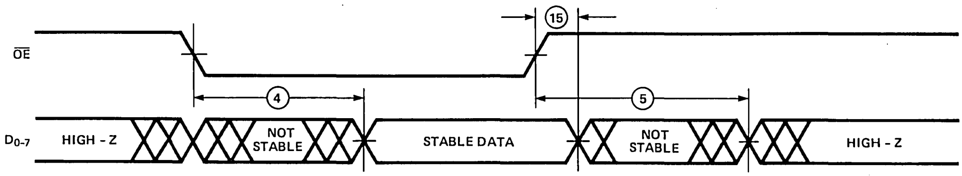


Figure 4. Tri-State Output Timing

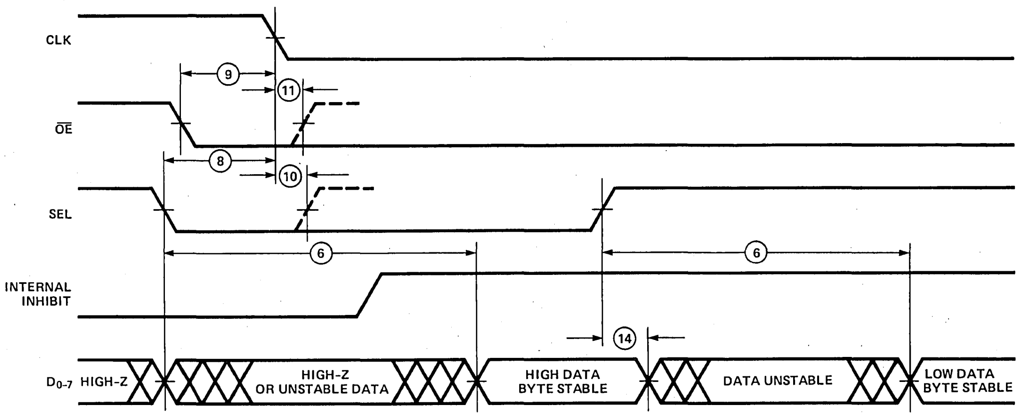


Figure 5. Bus Control Timing

Operation

A detailed block diagram of the HCTL-2000 is shown in Figure 6. The operation of each major function is described in the following sections.

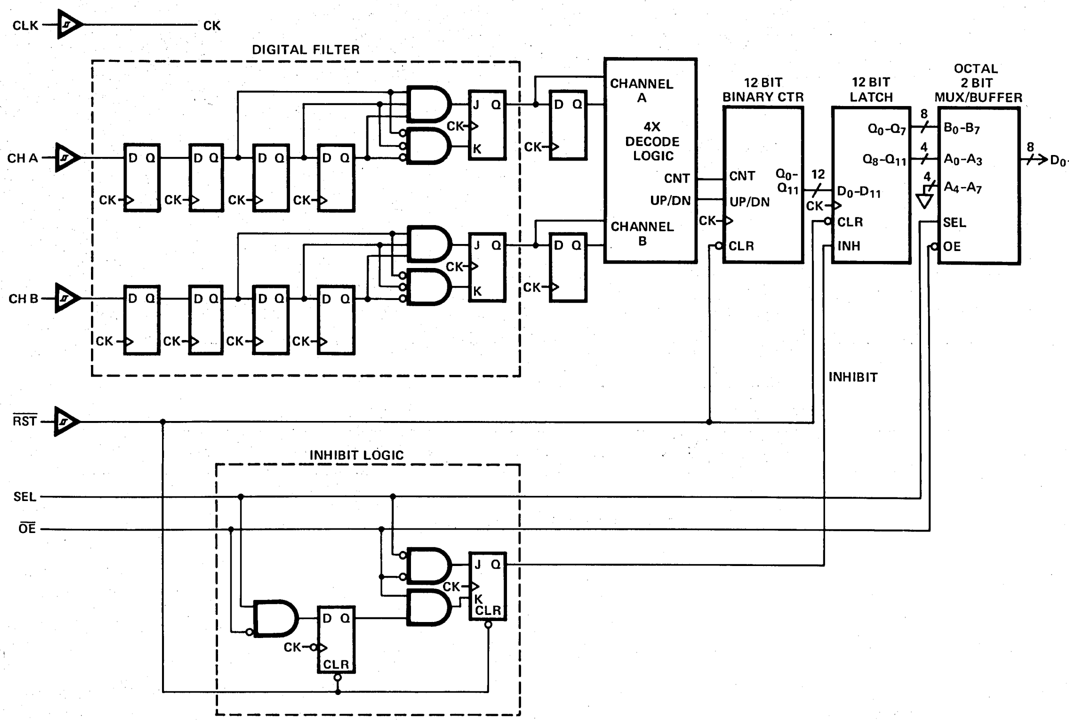


Figure 6. Simplified Logic Diagram

DIGITAL FILTER

The digital filter section is responsible for rejecting noise on incoming quadrature signals. Schmitt-trigger conditioning addresses the problems of slow rise and fall times and low level noise. The major task of the filter is to deal with short-duration noise pulses that cause the input logic level to momentarily change. Due to the nature of quadrature decoding, noise pulses on one channel will not cause a count error, but the coincidence of two overlapping noise pulses, one on each input, can cause illegal state transitions. False counts of undetermined direction will result from the decoding of these illegal transitions (see Fig. 8).

A pair of filters rejects these noise pulses by sampling the CHA and CHB logic levels and storing a time history in a pair of shift registers. For each channel, if the input level has had the same value on three consecutive rising clock edges, that value becomes the new output of the filter; otherwise the output is unchanged. This means that the CHA filter output cannot change from high to low until the CHA input has been low for three consecutive rising clock edges. CHB is treated the same as CHA.

The operation of this digital filter section places one of two timing constraints on the minimum clock frequency in relationship to the encoder count frequency. The first constraint derives from the operation of the input filters. It relates the maximum clock period to the minimum encoder pulse width. The second constraint derives from the decoder operation and is covered in the "Quadrature Decoder" section. It relates the maximum clock period to the minimum encoder state width (T_{es}).

The explanation of constraint one above is as follows: It takes a minimum of four positive clock transitions for a new logic level on either CHA or CHB to propagate through their respective filters, but the signal only needs to be stable for three consecutive rising clock edges (See Figure 7). This means that the minimum encoder pulse width (T_e) on each channel must be $\geq 3T_{CLK}$, where T_{CLK} is the period of the clock.

In the presence of noise, the filter will require that $3T_{CLK}$ be less than T_e, since noise pulses will interrupt the required three consecutive constant level samples necessary for the filter to accept a new input level. In general, the types of noise that this filter will deal with will derive from the rotating system, i.e., motor noise, capacitively coupled level changes from other encoder channels, etc. As such, these noise sources will be periodic in nature and proportional to the encoder frequency. Design for noise of this type is discussed later in the "Filter Optimization" section.

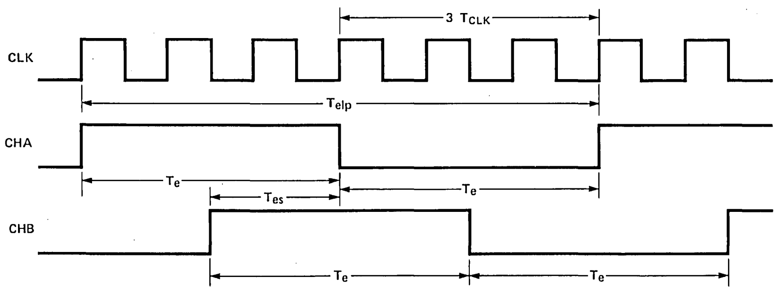


Figure 7. Minimum Encoder Pulse Width with Respect to T_{CLK}

In addition to problems with noise, other common signal problems enter into the determination of the maximum T_{CLK} for each application. The following quadrature signal aberrations can all be accounted for by designing with short enough T_{CLK} to accommodate the reduction of the effective encoder pulse width:

1) non-ideal encoder rise and fall times,
2) asymmetric pulses,
3) short (< 180 electrical degrees) pulses.

Designing for these non-ideal signals is discussed later in the "Filter Optimization" section.

QUADRATURE DECODER

The Quadrature Decoder section samples the outputs from the CHA and CHB filters. Sampling occurs on the rising clock edge. The Decoder Section observes changes in these outputs, and, on the rising clock edge, it outputs two signals to the position counter. These signals specify when to count and in which direction (up or down).

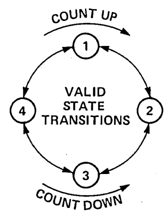
Encoder state changes are detected by comparing the previous sampled state to the current sampled state. If the two are different, the counter section is signaled to count on the next rising clock edge. Count direction (up or down) is also determined by observing the previous and current states, as shown in the quadrature state transition diagram (figure 8). An illegal state transition, caused by a faulty encoder or noises severe enough to pass the filter, will produce a count but in an undefined direction.

The second constraint on the relationship between T_{CLK} and the input quadrature signal, as previously mentioned in the "Digital Filter" section, is the requirement by the 4x decoder for at least one positive clock transition to occur during each quadrature state to detect the state. This constraint is satisfied if: $T_{es} > T_{CLK}$, where T_{es} is the time interval corresponding to the shortest state width at the maximum system velocity.

The combination of the following two errors must be examined in light of the minimum state width constraint to ensure proper operation of the decoder section:

1) Phase shift deviations from 90 electrical degrees between the CHA and CHB signals;
2) Pulse width errors resulting in T_e shorter than 180 electrical degrees in either or both CHA and CHB.

Design for these conditions is discussed in the "Filter Optimization" section.



CHA	CHB	STATE
1	0	1
1	1	2
0	1	3
0	0	4

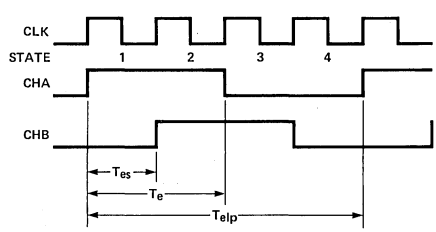


Figure 8. Elements of 4x Quadrature Decoding

POSITION COUNTER

This section consists of a 12-bit binary up/down counter which counts on rising clock edges as specified by the Quadrature Decode Section. All twelve bits of data are passed to the position data latch. The system can use this count data in three ways:

A. System total range is ≤12 bits, so the count represents "absolute" position.

B. The system is cyclic with ≤12 bits of count per cycle, $\overline{RST}$ is used to reset the counter every cycle, and the system uses the data to interpolate within the cycle.

C. System count is >12 bits, so the count data is used as a relative or incremental position input for a system computation of absolute position.

In case C above, counter rollover occurs. In order to prevent loss of position information, the processor must read the outputs of the HCTL-2000 at intervals shorter than 512 times the minimum encoder line period. This minimum line period (T_{elp}) corresponds to the maximum encoder velocity of the design. Two's complement arithmetic is normally used to compute position from these periodic position updates.

POSITION DATA LATCH

This section is a 12-bit latch which captures the position counter output data on each rising clock edge, except when its inputs are disabled by the inhibit logic section during two-byte read operations. The output data is passed to the bus interface section. The latch is cleared asynchronously by the $\overline{RST}$ signal. When active, a signal from the inhibit logic section prevents new data from being captured by the latch, keeping the data stable while successive byte-reads are made through the bus interface section.

BUS INTERFACE

The bus interface section consists of a 16 to 8 line multiplexer and an 8 bit, three-state output buffer. The multiplexer allows independent access to the low and high bytes of the position data latch output. Since the latch is only twelve bits wide, the upper four bits of the high byte are internally set to zero. The SEL and $\overline{OE}$ signals determine which byte is output and whether or not the output bus is in the high-Z state, respectively.

INHIBIT LOGIC

The Inhibit Logic Section samples the $\overline{OE}$ and SEL signals on the falling edge of the clock and, in response to certain conditions (see Figure 9 below), inhibits the position data latch. The $\overline{RST}$ signal asynchronously clears the inhibit logic, enabling the latch.

STEP	SEL	$\overline{OE}$	CLK	INHIBIT SIGNAL	ACTION
1	L	L	⌐	1	SET INHIBIT; READ HIGH BYTE
2	H	L	⌐	1	READ LOW BYTE; STARTS RESET
3	X	H	⌐	0	COMPLETES INHIBIT LOGIC RESET

Figure 9. Two Byte Read Sequence

While the HCTL-2000 can be used with any microprocessor, the Bus Interface and Inhibit Logic sections have been optimized for use with microprocessors similar to the Motorola 6801. The 6801 has a double-byte fetch instruction (LDD) which produces two consecutive fetch cycles on the bus. In the correct interface configuration, the first cycle inhibits the position data latch and reads the high data byte, and the second cycle reads the low byte and resets the inhibit logic. A version of this configuration is illustrated in Figure 14.

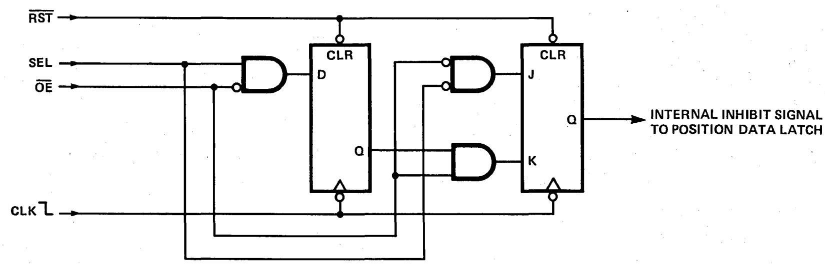


Figure 10. Simplified Inhibit Logic

Filter Optimization

System design with the HCTL-2000 will require the user to optimize its clock period for encoding errors and line noise on the CHA and CHB inputs. In the absence of noise this optimization is simplified. The critical encoding errors, minimum pulse width and minimum state width, occur at the maximum designed system operating velocity. Input noise can be caused by motor electromagnetic interference, channel cross coupling, etc. The HCTL-2000 input filter interacts with encoding errors and noise to form the major system design constraints. This section will illustrate system design techniques and will present guidelines useful in implementing the HCTL-2000.

The discussion that follows will make use of the definitions listed below:

T_{nf} = The fundamental period characteristic of a periodic noise source

T_{CLK} = Period of HCTL-2000 clock input signal

T_{mn} = Maximum pulse duration of encoder noise

$T_{emin} = T_{e(min)}$ = Minimum encoder line pulse width including encoder errors

$T_{esmin} = T_{es(min)}$ = Minimum encoder statewidth including encoder errors

T_{elpmin} = Period of maximum designed encoder line frequency

RPM = Maximum designed operating speed of the encoder in revolutions per minute

N = Encoder line count = Number of encoder counts per revolution

K1 = 60 sec./min.

ENCODING ERRORS

Design for quadrature signal errors proceeds as follows for an ideal quadrature signal, i.e. all errors = 0:

$T_{elp} = 360°e$ = defined as one electrical cycle in electrical degrees (1)

$T_e = 1/2T_{elp} = 180°e$ ideal pulse width (2)

$T_{es} = 1/4T_{elp} = 1/2\ T_e = 90°e$, ideal state width (3)

In a real system there are quadrature signal errors, where these errors are:

ΔP = Maximum encoder pulse width error in °e, as a deviation from the ideal pulse width of 180°e

ΔS = Maximum state width error in °e, as a deviation from the ideal state width of 90°e

The worst cases for pulse width and state width errors in terms of time intervals will occur at the maximum designed system operating velocity. These errors are typically available from encoder manufacturer's data sheets.

$$T_{elpmin} = \frac{K1}{(RPM)\ (N)} \tag{4}$$

$$T_{emin} = \left(\frac{180-|\Delta P|}{360}\right) T_{elpmin} \tag{5}$$

$$T_{esmin} = \left(\frac{90-|\Delta S|}{360}\right) T_{elpmin} \tag{6}$$

NOISE

In the absence of noise, the system design reduces to case A in Table 6. In the presence of noise, cases B through E describe the types of noise for which the above filters are effective. Normal techniques for reducing noise on CHA and CHB inputs may be required to reduce this noise to a level that can be handled by the input filters.

Noise that can be filtered by the HCTL-2000 input filters is noise where $T_{nf} > T_{esmin}$ and $T_{mn} < 2T_{CLK}$. This noise can be subdivided into four categories, each having different design constraints. These categories are differentiated by the pulse width of noise on the individual encoder channels.

Dependant channel noise, as below in case B and C in Table 6, is noise where the superposition of noise from both encoder channels does not display a period shorter than the minimum state width:

$$T_{nf} > T_{esmin}.$$

The graphic analysis of the effect of this type of noise upon the filter operation is illustrated in Figure 11.

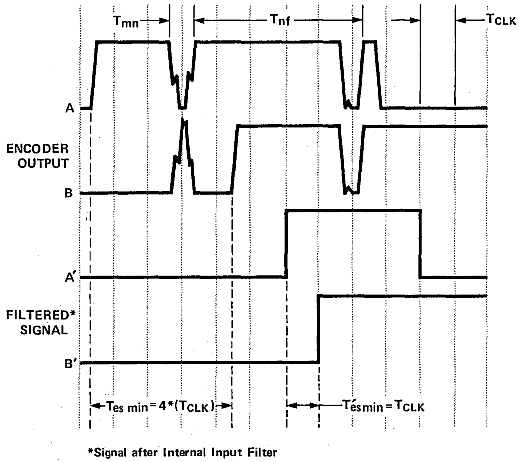


Figure 11. Noise is Encoder Channel Dependent

Independant channel noise, as in case D and E in Table 6, is such that the noise on each channel is independant of the noise on the other channel. The period of the noise on each channel must satisfy the condition:

$$T_{nf} > T_{esmin}$$

independantly. The graphic analysis of the effect of this type of noise on the filter operation is illustrated in Figure 12.

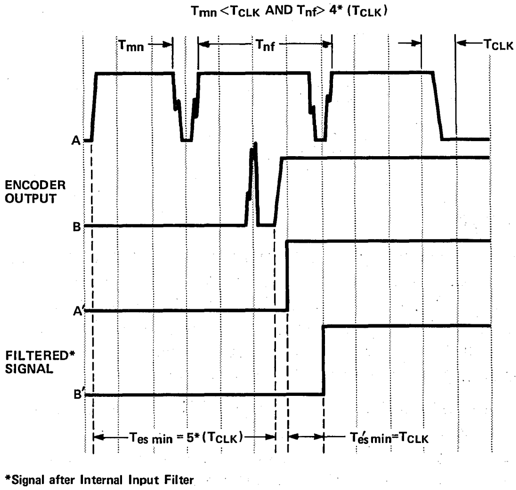


Figure 12. Noise is Encoder Channel Independent

The set of design rules that are presented in Table 6 can be derived by examination of Figures 11 and 12, and the following constraints:

a) The encoder output signals must stay at a logic level for a minimum of three consecutive clock pulses before the HCTL-2000 recognizes the logic level change: $T_{emin} > 3T_{CLK}$.

b) After acceptance by the HCTL-2000 input filtering section, a state must exist for a minimum of T_{CLK} to be recognized by the internal logic.

c) The minimum encoded pulse width must be greater than twice the minimum state width: $T_{emin} > 2T_{esmin}$.

d) The minimum clock period must be greater than 255 ns, which is the minimum clock period for which the HCTL-2000 is guaranteed to operate over the entire specified operating temperature range.

FILTER DESIGN EXAMPLES

Given the above rules, we can calculate the design parameters for a typical high performance motor loop as follows:

Where RPM = 3600 rev/min.
N = 1000 counts/rev.
$\Delta P = \pm 48°e$
$\Delta S = \pm 60°e$
at 60° C, $1/T_{elpmin} = 60kHz$

Then the following calculation accounts for signal errors:

$$T_{elpmin} = \left(\frac{K1}{(RPM)(N)}\right) = \frac{60}{(3600)(1000)} \quad \text{from eq. 4}$$

$$= 16667 \text{ ns}$$

$$T_{emin} = \left(\frac{180-|\Delta P|}{360}\right) T_{elpmin}$$

$$= \left(\frac{180-48}{360}\right)(16667 \text{ ns}) \quad \text{from eq. 5}$$

$$= 6111 \text{ ns}$$

$$T_{esmin} = \left(\frac{90-|\Delta S|}{360}\right) T_{elpmin}$$

$$= \left(\frac{90-60}{360}\right)(16667 \text{ ns}) \quad \text{from eq. 6}$$

$$= 1389 \text{ ns}$$

If the noise is as in case B of Table 6, we can use the above to evaluate the system.

For the condition of noise such that $T_{mn} < 260$ ns:

$$T_{CLK} > 260 \text{ ns}$$

$$255 \text{ ns} \leq T_{CLK} < \frac{T_{esmin}}{4}$$

$$\frac{T_{esmin}}{4} = \frac{1389}{4} = 347 \text{ ns}$$

Thus,

$$255 \text{ ns} \leq T_{CLK} < 347 \text{ ns}$$

Similar calculations can be performed to design the filter for the specifics of each system.

Table 6. Summary of Filter Design Rules for the HCTL-2000

Case	Noise Relationship	General Conditions	Pulse Width Constraint	Clock Period Design Criteria
A	No noise on CHA or CHB	$T_{emin} > 2T_{esmin}$	$T_{clk} < T_{esmin}$	$255ns \leq T_{clk} < (1/3)T_{emin}$
B	Superposition of noise on CHA or CHB	$T_{esmin} > T_{nf}$ $T_{emin} > 2T_{esmin}$	$T_{clk} > T_{mn} > 0$	$255ns \leq T_{clk} < (1/4)T_{esmin}$
C	Superposition of noise on CHA or CHB	$T_{esmin} > T_{nf}$ $T_{emin} > 2T_{esmin}$	$2T_{clk} > T_{mn} \geq T_{clk}$	$255ns \leq T_{clk} < (1/5)T_{esmin}$
D	Noise on CHA or on CHB Independent of each other	$T_{esmin} > T_{nf}$ $T_{emin} > 2T_{esmin}$	$T_{clk} > T_{mn} > 0$	$255ns \leq T_{clk} < (1/5)T_{esmin}$
E	Noise on CHA or on CHB Independent of each other	$T_{esmin} > T_{nf}$ $T_{emin} > 2T_{esmin}$	$2T_{clk} > T_{mn} \geq T_{clk}$	$255ns \leq T_{clk} < (1/7)T_{esmin}$

Interfacing the HCTL-2000: General

The 12 bit latch and inhibit logic on the HCTL-2000 allows access to 12 bits of count with an 8 bit bus. When only 8 bits of count are required, a simple 8 bit (1 byte) mode is available by holding SEL high continously. This disables the inhibit logic. $\overline{OE}$ provides control of the tri-state bus, and read timing is per Figures 3 and 4.

For proper operation of the inhibit logic during a two-byte read, $\overline{OE}$ and SEL must be synchronous with CLK due to the falling edge sampling of $\overline{OE}$ and SEL.

The internal inhibit logic on HCTL-2000 inhibits the transfer of data from the counter to the position data latch during the time that the latch outputs are being read. The inhibit logic allows the microprocessor to first read the high order 4 bits from the latch and then read the low order 8 bits from the latch. Meanwhile, the counter can continue to keep track of the quadrature states from the CHA and CHB input signals.

Figure 10 shows a logic diagram of the inhibit logic circuit. The operation of the circuitry is illustrated in the read timing shown in Figure 13.

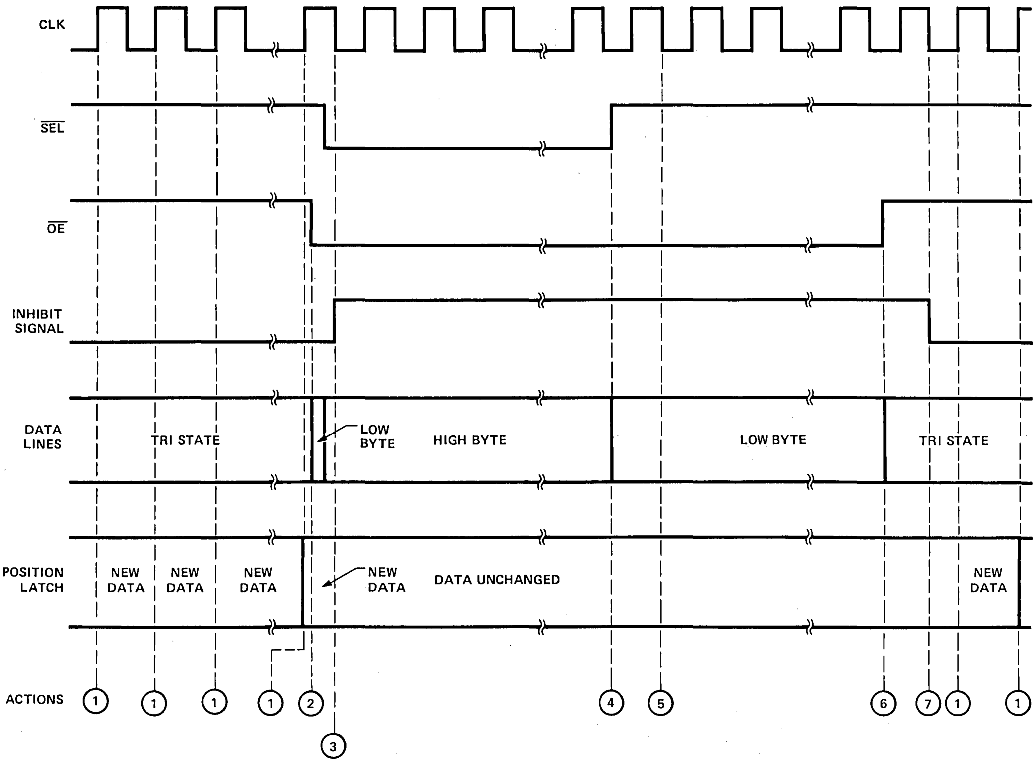


Figure 13. Internal Inhibit Logic Timing

ACTIONS

1. On the rising edge of the clock, counter data is transferred to the position data latch, provided the inhibit signal is low.
2. When $\overline{OE}$ goes low, the outputs of the multiplexer are enabled onto the data lines. If SEL is low, then the high order data bytes are enabled onto the data lines. If SEL is high, then the low order data bytes are enabled onto the data lines.
3. When the HCTL-2000 detects a low on $\overline{OE}$ and SEL during a falling clock edge, the internal inhibit signal is activated. This blocks new data from being transferred from the counter to the position data latch.
4. When SEL goes high, the data outputs change from high byte to low byte.
5. The first reset condition for the inhibit logic is met when the HCTL-2000 detects a logic high on SEL and a logic low on $\overline{OE}$ during a falling clock edge.
6. When $\overline{OE}$ goes high, the data lines change to a high impedance state.
7. To complete the reset of the inhibit logic, after the first reset condition has been met, the HCTL-2000 needs to detect a logic high on $\overline{OE}$ during a falling clock edge.

Interfacing the HCTL-2000 to a Motorola 6801

This interface method provides the minimum part count when the 6801 is operated in "MODE 5". A typical 6801 circuit is shown in Figure 14. In Figure 14, the 74LS138 address decoder can be eliminated if the HCTL-2000 is the only occupant of Port 4.

The processor clock output (E) is used to clock the HCTL-2000 as well as the address decoder. One of the address decoder outputs drives the $\overline{OE}$ input. This results in HCTL-2000 counter data being enabled onto the bus whenever an external memory access is made to the HCTL-2000. This example assumes the address assigned to the HCTL-2000 high byte is an even address. The least significant address bit is connected to the SEL input. It determines which data byte is output. When A0 on the decoder equals 0 the chip selects the high byte, and when A0 equals 1, the chip selects the low byte. This configuration allows the 6801 to read both data bytes with a single double-byte fetch instruction (LDD E, 01XX). The LDD instruction is a five cycle instruction which reads external memory location 01XX and stores the high order byte in accumulator A and reads external memory location 01XX +1 and stores the low order byte in accumulator B during the last two cycles. Figure 15 illustrates the sequence of events during all five cycles.

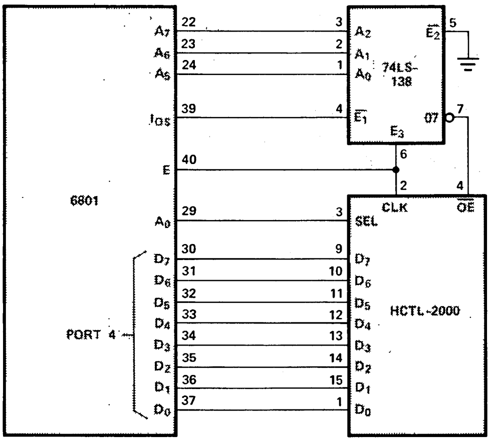


Figure 14. A Circuit to Interface to the 6801

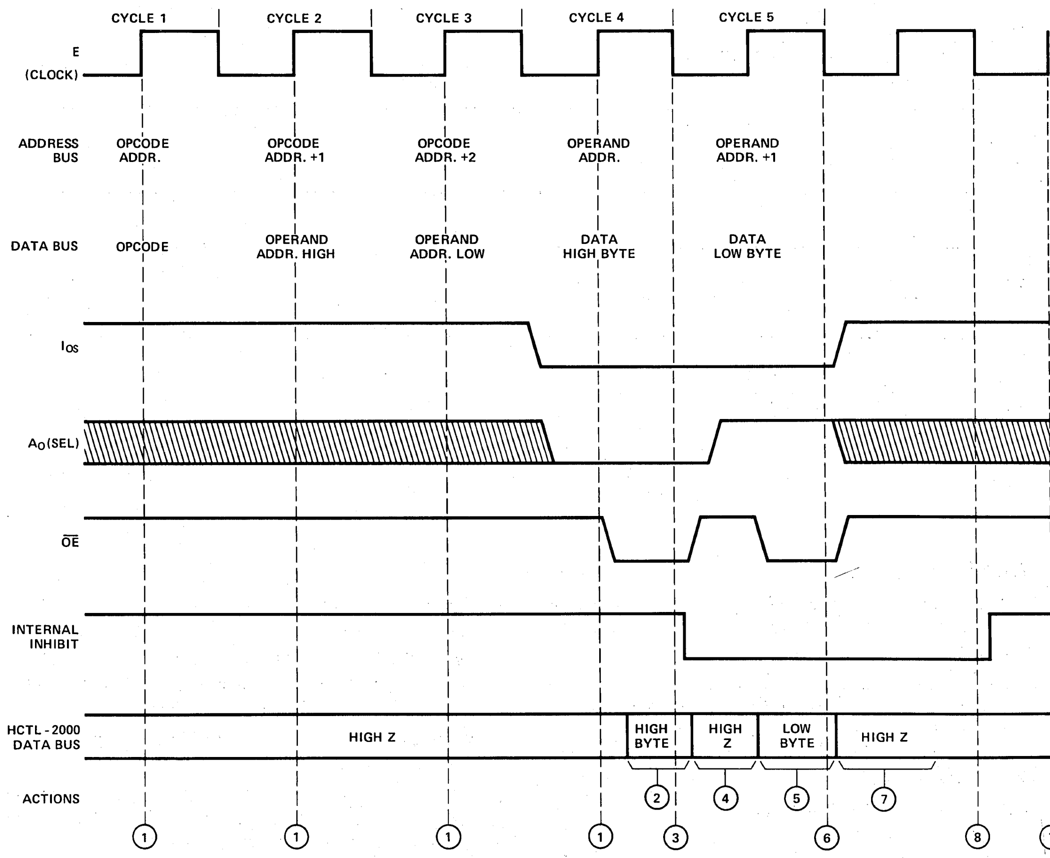


Figure 15. Interface Timing for the 6801 LDD E

ACTIONS

1. E is the microprocessor clock output. On the rising edge of E, if the internal inhibit is not active, then new data is transferred from the internal counter to the position data latch.
2. An even address output from the 6801 has caused SEL to go low. E goes high which causes the address decoder output for the HCTL-2000 $\overline{OE}$ input to go low. This causes the HCTL-2000 to output the high byte of the position data latch.
3. The 6801 reads the data bus on the falling edge of E, storing the high order data byte in accumulator A. The chip detects that $\overline{OE}$ and SEL are low on the falling edge of E and activates the internal inhibit signal. The position data latch is inhibited and data cannot be transferred from the internal counter to the latch.
4. E is now low, so the address decoder output is disabled and $\overline{OE}$ goes high. The 6801 increments the address, so SEL goes high. The position data latch is still inhibited.
5. The address decoder is enabled after E goes high, so $\overline{OE}$ goes low and the low data byte is enabled onto the bus.
6. The 6801 reads the data bus on the falling edge of E, storing the low order data byte in accumulator B. The chip detects that $\overline{OE}$ is low and SEL is high on the falling edge of E, so the first inhibit-reset condition is met.
7. E is now low, so the address decoder is disabled, causing $\overline{OE}$ to go high and the data lines to go to the high impedence state. The 6801 continues its instruction execution, and the state of SEL is indeterminate.
8. The HCTL-2000 detects $\overline{OE}$ is high on the next falling edge of E. This satisfies the second inhibit reset condition so the inhibit signal is reset.

Interfacing the HCTL-2000 to an Intel 8748

The circuit in Figure 15 shows the connections between an HCTL-2000 and an 8748. Data lines D0-D7 are connected to the 8748 bus port. Bits 0 and 1 of port 1 are used to control the SEL and $\overline{OE}$ inputs of the HCTL-2000 respectively. T0 is used to provide a clock signal to the HCTL-2000. The frequency of T0 is the crystal frequency divided by 3. T0 must be enabled by executing the ENT0 CLK instruction after each system reset, but prior to the first encoder position change. An 8748 program which interfaces to the circuit in Figure 16 is given in Figure 17. The resulting interface timing is shown in Figure 18.

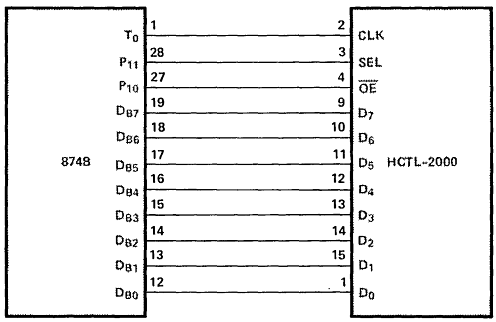


Figure 16. An HCTL-2000 to Intel 8748 Interface

LOC	OBJECT CODE	SOURCE STATEMENTS	
000	99 00	ANL P1, 00H	ENABLE OUTPUT AND OUTPUT HIGHER ORDER BITS
002	08	INS A, BUS	LOAD HIGHER ORDER BITS INTO ACC
003	A8	MOVE R0 A	MOVE DATA TO REGISTER 0
004	89 03	ORL P1, 01H	CHANGE DATA FROM HIGH ORDER TO LOW ORDER BITS
006	08	INS A, BUS	LOAD ORDER BITS INTO AC
008	A9	MOV R1, A	MOVE DATA TO REGISTER 1
009	89 03	ORL P1, 03H	DISABLE OUTPUTS
00B	93	RETR	RETURN

Figure 17. A Typical Program for Reading HCTL-2000 with an 8748

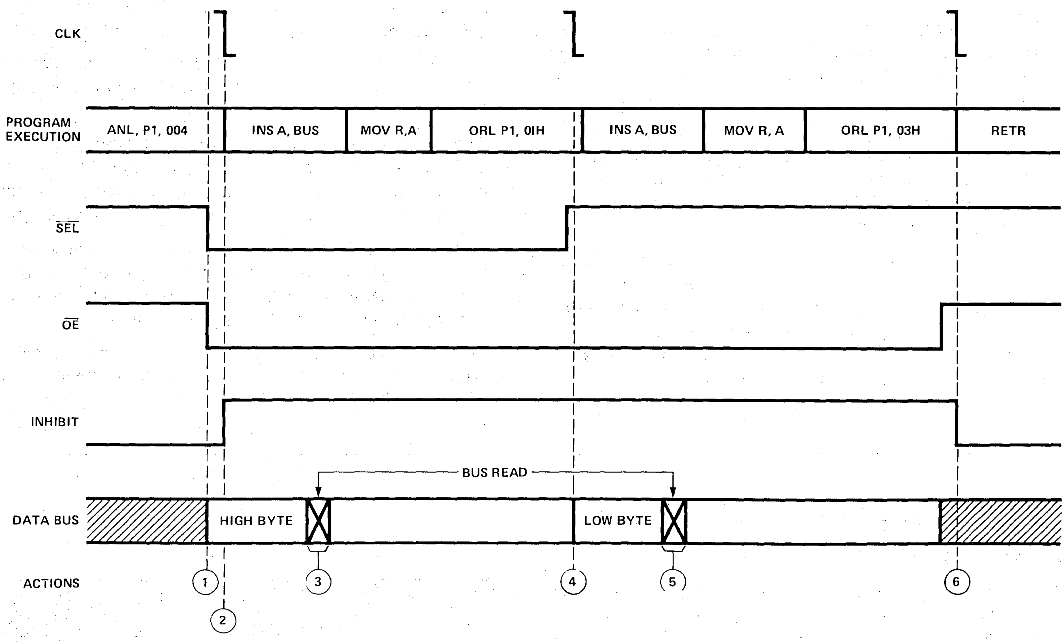


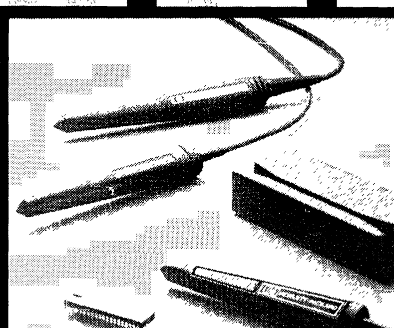
Figure 18. 8748 READ Cycle from Figure 14.

ACTIONS

1. ANL P1, 00H has just been executed. The output of bits 0 and 1 of Port 1 cause SEL and $\overline{OE}$ to be logic low. The data lines output the higher order byte.
2. The HCTL-2000 detects that $\overline{OE}$ and SEL are low on the next falling edge of the CLK and asserts the internal inhibit signal. Data can be read without regard for the phase of the CLK.
3. INS A, BUS has just been executed. Data is read into the 8748.
4. ORL PORT 1, 01H has just been executed. The program sets SEL high and leaves $\overline{OE}$ low by writing the correct values to port 1. The HCTL-2000 responds by outputting the lower byte. The HCTL-2000 detects $\overline{OE}$ is low and SEL is high on the next falling edge of the CLK, and thus, the first inhibit-reset condition is met.
5. INS A, BUS has just been executed. Lower order data bits are read into the 8748.
6. ORL P1, 03H has just been executed. The HCTL-2000 detects $\overline{OE}$ high on the next falling edge of CLK. The program sets $\overline{OE}$ and SEL high by writing the correct values to port 1. This causes the data lines to be tri-stated. This satisfies the second inhibit-reset condition. On the next rising CLK edge new data is transferred from the counter to the position data latch.

[redacted]

2. Bar Code Components

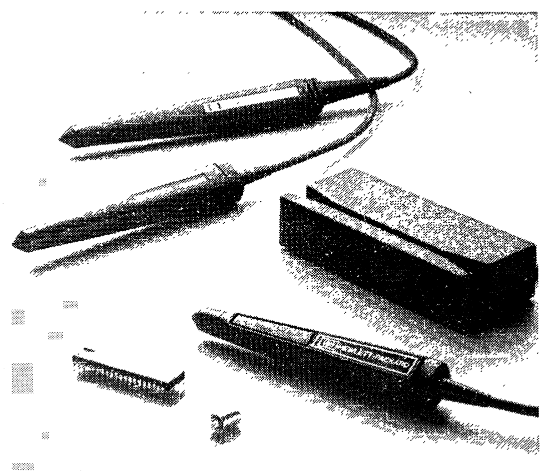


Bar Code Products

1986 brings with it a further expansion of Hewlett-Packard's bar code line in three widely diversified areas.

We have expanded our line of digital bar code wands again this year with the introduction of the HBCS-5XXX and HBCS-6XXX families of wands. These Low Current Digital Bar Code Wands are the latest technological advance from a company that invented the Digital Wand. Through sophisticated circuitry, these wands are able to provide superior performance while drawing less than 5 mA of current at 5 volts. Performance improvements include high ambient light rejection, including direct sunlight; a wider range of resolution choices; and a new sensor design specifically for reading thermally printed bar codes.

Of course, these wands continue to offer the other features you've come to expect from Hewlett-Packard wands: sealed, sapphire tips, wide scan angles, choice of case designs, and fully compatible digital outputs.



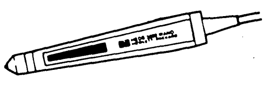
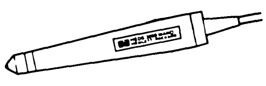
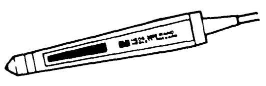
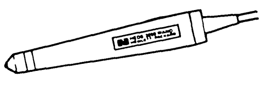
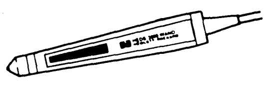
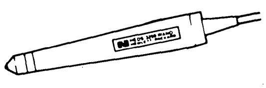
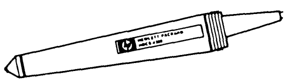
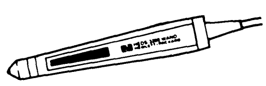
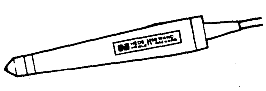
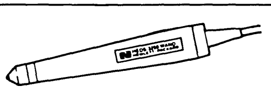
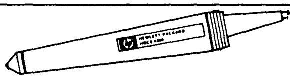
A totally new product for 1986 is Hewlett-Packard's Industrial Digital Slot Reader. This rugged scanner is designed specifically for reading bar codes printed on I.D. cards, badges, heavy paper stock, or traveller forms. It features a large slot width for handling even multiple laminated cards, a wide scan speed range, and a digital output that is compatible with wand decoding software.

Available in both an infrared (880 nm) version and a visible red (660 nm) version, the unit is housed in a black epoxy finished, metal case. The unique rear mounting system and tamper-proof design makes it ideal for use in security or industrial applications.

Finally, adding to our successful line of decoder IC's, is the new Multi-Purpose Decoder IC. This extraordinary device is designed specifically for the OEM who would rather not tie up valuable resources developing bar code decoding software. Packaged in a standard 40 pin DIP, the Multi-Purpose Decoder IC accepts inputs from virtually all hand-held scanning devices, including hand-held lasers and other solid state non-contact scanners. Now you have a way to simply and inexpensively add quality bar code decoding to your products and still retain the flexibility your customers require.

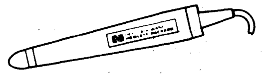
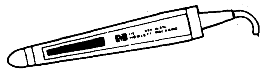
Look to Hewlett-Packard for performance products designed to meet the OEM's bar code needs!

Bar Code Wands

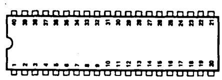
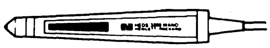
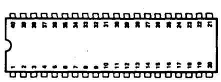
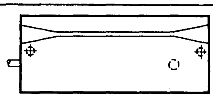
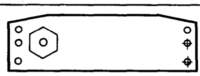
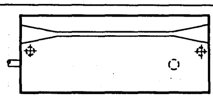
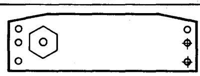
Package Outline Drawing	Part No.	Description	Features	Page No.
	HBCS-5000	Low Current Digital Bar Code Wand (with Switch) Resolution 0.33mm	• Low Continuous Current Draw (Less Than 5mA) • High Ambient Light Rejection • 0 to 45° Scan Angle • Push to Read Switch for Ultra Low Power Consumption • Rugged Polycarbonate Case • Sealed Sapphire Tip • Full Line of Options Available	2-6
	HBCS-5100	Low Current Digital Bar Code Wand (without Switch) Resolution 0.33mm		
	HBCS-5200	Low Current Digital Bar Code Wand (with Switch) Resolution 0.19mm		
	HBCS-5300	Low Current Digital Bar Code Wand (without Switch) Resolution 0.19mm		
	HBCS-5400	Low Current Digital Bar Code Wand (with Switch) Resolution 0.13mm		
	HBCS-5500	Low Current Digital Bar Code Wand (without Switch) Resolution 0.13mm		
	HBCS-6100	Low Current Digital Bar Code Wand Resolution 0.33mm	• Low Continuous Current Draw (Less Than 5mA) • High Ambient Light Rejection • 0 to 45° Scan Angle • Sealed Sapphire Tip • Metal Case • Full Line of Options Available	2-6
	HBCS-6300	Low Current Digital Bar Code Wand Resolution 0.19mm		
	HBCS-6500	Low Current Digital Bar Code Wand Resolution 0.13mm		
	HBCS-2200	Sapphire Tip Digital Bar Code Wand (with Switch) Resolution 0.19mm	• Digital Output • 0–45° scan angle • Replaceable Sapphire Tip • Internal Shielding • Push-to-read switch available for low power applications • Rugged Polycarbonate Case • Full line of options available	2-26
	HBCS-2300	Sapphire Tip Digital Bar Code Wand (without Switch) Resolution 0.19mm		
	HBCS-2400	Sapphire Tip Digital Bar Code Wand (with Switch) Resolution 0.13mm		
	HBCS-2500	Sapphire Tip Digital Bar Code Wand (without Switch) Resolution 0.13mm		
	HBCS-4300	Industrial Digital Bar Code Wand Resolution 0.19mm	• Digital Output • 0–45° scan angle • Replaceable Sapphire Tip • Metal case • Full line of options available	2-32
	HBCS-4500	Industrial Digital Bar Code Wand Resolution 0.13mm		

Package outline drawings not drawn to scale.

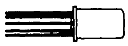
Bar Code Wands

Package Outline Drawing	Part No.	Description	Features	Page No.
	HEDS-3000	Digital Bar Code Wand (with Switch) Resolution 0.3mm	• Digital Output • 0–30° scan angle • Replaceable Tip • Internal Shielding available for improved electrical noise rejection • Push-to-read switch available for low power applications • Full line of options available	2-38
	HEDS-3050	Digital Bar Code Wand (Shielded) Resolution 0.3mm		
	HEDS-3200	Digital Bar Code Wand (with Switch) Resolution 0.19mm		2-44
	HEDS-3250	Digital Bar Code Wand (Shielded) Resolution 0.19mm		

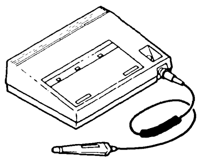
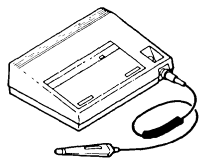
Component Level Bar Code Readers

Package Outline Drawing	Part No.	Description	Features	Page No.
   	HBCR-1000 HBCR-1022 HBCR-1024 HBCR-1025 HBCR-1043 HBCR-1045	Component Level Bar Code Reader with Sapphire Tip Wand Component Level Bar Code Reader with Industrial Metal Wand	• Industry Standard Bar Codes • Automatic Code Recognition • Full Duplex Serial or Parallel ASCII Output • Choice of High Performance Wands • Single 5 Volt Supply	2-18
	HBCR-2000	Multi-Purpose Decoder IC	• Accepts Inputs from All Hand-Held Scanners, Including Lasers • Largest Selection of Codes Available • Automatic Code Recognition • Serial ASCII Output • Standard 40 Pin Package	2-12
	HBCS-7000	Industrial Digital Slot Reader, Visible Red, Resolution 0.19mm	• 125 Mil Slot Width • Epoxy Finished Metal Housing • Wide Scan Speed Range • Tamper Proof Design • Digital Output	2-68
	HBCS-7001	Optics/Electornics Module, Visible Red, Resolution 0.19mm		
	HBCS-7100	Industrial Digital Slot Reader, Infra-Red, Resolution 0.19mm		
	HBCS-7101	Optics/Electronics Module, Infra-Red, Resolution 0.19mm		

Optical Reflective Sensors

Package Outline Drawing	Part No.	Description	Features	Page No.
	HBCS-1100	High Resolution Optical Reflective Sensor	• 0.19mm spot size • Fully Specified and Guaranteed for Assured Performance • Visible Light Source can Detect Most Colors • Photo IC Detector Optimizes Speed and Response • Standard To-5 Header	2-52

Bar Code Readers

Package Outline Drawing	Part No.	Description	Features	Page No.
	16800A	Programmable Bar Code Reader	• Flexible Configuration • All Standard Industrial and Commercial Bar Codes Supported • Choice of High Performance, Rugged Wands • Computer Control and Simple Operator Feedback (16800A only) • Internal Power Supply • Meet UL, CSA, FCC Class B, VDE Level B	2-58
	16801A	Non-Programmable Bar Code Reader		

HEWLETT PACKARD

LOW CURRENT DIGITAL BAR CODE WANDS

METAL, LOW RESOLUTION	HBCS-6100
METAL, GENERAL PURPOSE RESOLUTION	HBCS-6300
METAL, HIGH RESOLUTION	HBCS-6500
POLYCARBONATE, LOW RESOLUTION	HBCS-5000/5100
POLYCARBONATE, GENERAL PURPOSE RESOLUTION	HBCS-5200/5300
POLYCARBONATE, HIGH RESOLUTION	HBCS-5400/5500

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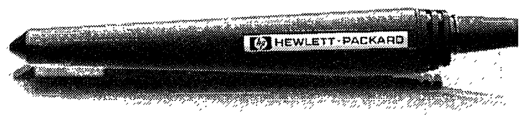
Features

- ULTRA LOW CONTINUOUS CURRENT DRAIN
  — Less Than 5 mA
- HIGH AMBIENT LIGHT REJECTION
  — Operates in Direct Sunlight
- AVAILABLE IN THREE RESOLUTIONS TO MEET A VARIETY OF SCANNING NEEDS
- VISIBLE RED (655 nm) AND INFRARED (820 nm) VERSIONS FOR READING A WIDE RANGE OF PRINTING TYPES AND COLORS
- SCAN ANGLE 0 to 45 DEGREES
- AVAILABLE IN EITHER HIGH IMPACT POLYCARBONATE OR INDUSTRIAL METAL HOUSINGS
- OPERATING TEMPERATURE −20°C to +65°C
- SEALED REPLACEABLE SAPPHIRE TIP
  — Provides Protection from Contamination Due to Dirt and Debris
- DIGITAL OUTPUT
  — Open Collector Output Compatible with TTL and CMOS Logic
- SINGLE 5 VOLT SUPPLY



Description

Hewlett-Packard's Low Current Digital Bar Code Wands are hand-held scanners optimized to provide excellent reading of all common bar code formats. The wands contain an optical sensor with a 655 nm visible red or an 820 nm infrared LED; a photodetector IC; and precision aspheric optics. The internal signal conditioning circuitry converts the optical information into a logic level pulse width representation of the bars and spaces.

Available in a choice of three resolutions, these wands have been designed to cover a wide range of bar code printing. The general purpose resolution wands, with their 0.19 mm (0.0075 in.) spot size, are excellent choices for reading a wide range of bar code symbols. For reading very high density symbols, the high resolution wands with a 0.13 mm (0.005 in.) spot size, are the appropriate choice. For lower resolution or poorly printed dot matrix symbols, the low resolution wands have a spot size of 0.38 mm (0.13 in.) to help reject extraneous spots and voids.

All of the wands have a special circuit design that provides for extremely low current drain (less than 5 mA) with continuous operation. This makes them ideal for use on battery powered systems where low power drain will extend battery life. These wands also have excellent ambient light rejection, allowing full operation in direct sunlight.

All of HP's Low Current Digital Bar Code Wands are FCC and VDE approved. They feature a shield for maximizing immunity to electrostatic discharge (ESD), electromagnetic interference (EMI) and ground loops. The shield is also designed to eliminate noise from capacitively coupled inputs.

The standard wand configuration includes a strain relieved coiled cord, which has a comfortable extended length of 190 cm (75 in.). Maximum length is 250 cm (100 in.). The standard connector on the polycarbonate wands is a 5 pin, 240 degree DIN connector. On the metal wands the standard connector is a 5 pin, 240 degree DIN connector with metal locking ring.

Applications

The digital bar code wand is a highly effective alternative to keyboard data entry. Bar code scanning is faster and more accurate than key entry and provides far greater throughput. In addition, bar code scanning typically has a higher first read rate and greater data accuracy than optical character recognition. When compared to magnetic stripe encoding, bar code offers significant advantages in flexibility of media, symbol placement, and immunity to electromagnetic fields.

Hewlett-Packard's Low Current Digital Bar Code Wands are especially designed for battery powered applications where low power drain is a primary concern. With continuous current draws of less than 5 mA, these wands can be used on battery powered systems without sacrificing battery life or requiring special "strobing" circuits. They are also ideal for AC powered systems where conventional wand current drains may require an increased power supply design.

In addition to their low current drain, these wands are also designed to work in high ambient light, such as outdoors or near large windows. This feature is extremely useful in applications such as inventory control on receiving docks, automobile tracking outdoors and check-out stands outdoors or near large store front windows.

Because the low resolution and the general purpose resolution wands use an emitter wavelength of 655 nm, they are extremely versatile in the range of printing type and colors that they will read, including thermal printing and dot matrix printing.

Available in either a light weight polycarbonate case or a rugged metal case, these wands are excellent choices for both light industrial and commercial applications, or heavy industrial and LOGMARS applications.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Nominal Narrow Element Width HBCS-5000/5100/6100		0.33 (0.013)		mm (in.)	
HBCS-5200/5300/6300		0.19 (0.0075)		mm (in.)	
HBCS-5400/5500/6500		0.13 (0.005)		mm (in.)	
Scan Velocity	V_{SCAN}	7.6 (3)	127 (50)	cm/sec (in/sec)	
Contrast	R_W-R_B	45		%	1
Supply Voltage	V_S	4.5	5.5	Volts	2
Temperature	T_A	−20	+65	°C	
Ambient Light	E_V		100,000	lux	3
Tilt Angle	(See Figure 2)				
Orientation	(See Figure 3)				

NOTES:

1. Contrast is defined as R_W-R_B where R_W is the reflectance of the white spaces and R_B is the reflectance of the black bars, measured at the emitter wavelength (655 nm or 820 nm). Contrast is related to print contrast signal (PCS) by PCS = (R_W-R_B)/R_W or R_W-R_B = PCS*R_W.
2. Power supply ripple and noise should be less than 100 mV peak to peak.
3. Ambient light sources can be diffuse tungsten, sodium, mercury, fluorescent, sunlight, or a combination thereof.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	−40	+75	°C	
Operating Temperature	T_A	−20	+65	°C	
Supply Voltage	V_S	−0.5	+6.00	V	
Output Transistor Power	P_T		150	mW	
Output Collector Voltage	V_O	−0.5	+20	V	

Electrical Operation

The HBCS-5XXX/6XXX family of digital bar code wands consists of a precision optical sensor and an electronic circuit that creates a digital output of the bar code pattern. The open collector transistor requires only a pull-up resistor to provide a TTL compatible output from a single 4.5V to 5.5V DC power supply.

A non-reflecting black bar results in a logic high (1) level output, while a reflecting white space will cause a logic low (0) level output (see Figure 1). The initial state will be indeterminate. However, if no bar code is scanned, after a short period (typically less than 1 second), the wand will assume a logic low state. This feature insures that the first bar will not be missed in a normal scan.

The wands provide a case, cable and connector shield which must be terminated to logic ground or, preferably, to both logic ground and earth ground. The shield is connected to the metal housing of the 5 pin DIN connector.

All standard HP Low Current Digital Bar Code wands are certified to meet FCC Class B and VDE Level B standards. The shield must be properly terminated in order to maintain these approvals and to keep the cable from acting as an antenna, injecting electrical noise into the wand circuitry. Grounding the shield will also provide a substantial improvement in EMI/ESD immunity.

The recommended logic interface for the wands is shown in Figure 5. This interconnection provides the maximum ESD protection for both the wand and the user's electronics.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Notes
Supply Current	I_S		3.5	5.0	mA	$V_S = 5.0$ V	4, 5
High Level Output Current	I_{OH}			1.0	μA	$V_{OH} = 2.4$ V	
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} = 16$ mA	
Output Rise Time	t_r		3.4	20	μs	10%-90% Transition $R_L = 1$ K	6
Output Fall Time	t_f		1.2	20	μs		6
Switch Bounce HBCS-5000/5200/5400	t_{sb}		0.5	5.0	ms		7
Electrostatic Discharge Immunity	ESD		25		kV		8
Wake-Up Time	t_W		50	200	ms		9

NOTES:

4. Push-to-read switch (if applicable) is depressed.
5. Not including pull-up resistor current.
6. See Figure 1.
7. Switch bounce causes a series of sub-millisecond pulses to appear at the output (V_O).
8. Shield must be properly terminated (see Figure 9). The human body is modeled by discharging a 300 pF capacitor through a 500 Ω resistor. No damage to the wand will occur at the specified discharge level.
9. After this time, the wand is operational.

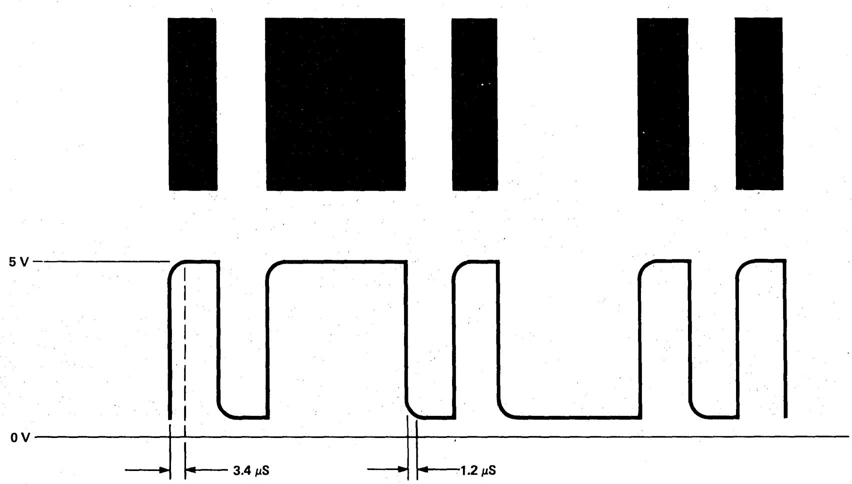


Figure 1. Typical Output Waveform

Depth of Field

Hewlett-Packard Digital Bar Code Wands are designed for contact scanning. However, it is possible to read through some overlay or covering material depending on the thickness of the material and the angle at which the wand is held. Figure 2 shows the relationship between tilt angle and depth of field.

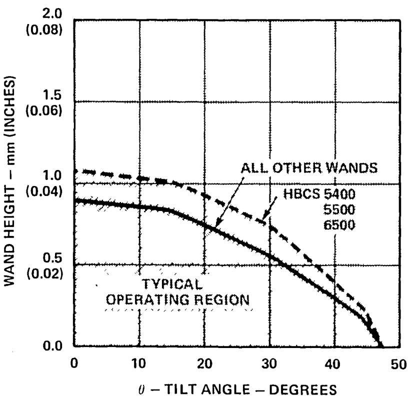


Figure 2. Wand Height vs. Tilt Angle

Testing

All Hewlett-Packard Digital Bar Code Wands are 100% tested for performance and digitizing accuracy after manufacture. This insures you of the consistent quality product you expect from HP. More information about our test procedures, test set-up, and test limits are available upon request.

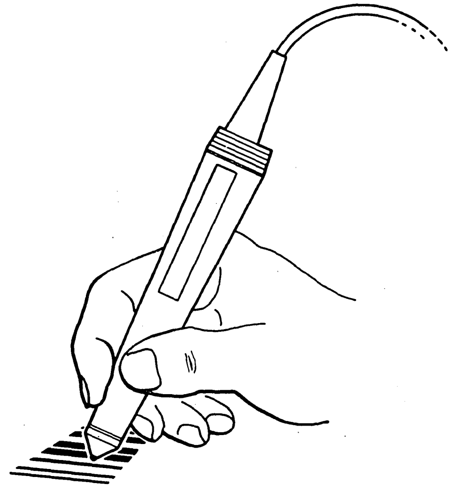


Figure 3. Preferred Orientation

Selection and Application Guide

	HBCS 5000	HBCS 5100	HBCS 5200	HBCS 5300	HBCS 5400	HBCS 5500	HBCS 6100	HBCS 6300	HBCS 6500
Wavelength (nm)	655	655	655	655	820	820	655	655	820
Nominal Narrow Element Width									
(mm)	0.33	0.33	0.19	0.19	0.13	0.13	0.33	0.19	0.13
(inch)	0.013	0.013	0.0075	0.0075	0.005	0.005	0.013	0.0075	0.005
Case Material									
Polycarbonate	X	X	X	X	X	X			
Metal							X	X	X
Switch	Yes	No	Yes	No	Yes	No	No	No	No
Will Read Bar Codes Printed Using:									
Regular Thermal Paper	Yes	Yes	Yes	Yes	No	No	Yes	Yes	No
Dye-Based Inks	Yes	Yes	Yes	Yes	No	No	Yes	Yes	No
Carbon Based Inks (Note 10)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Colors (Note 11)	Yes	Yes	Yes	Yes	No	No	Yes	Yes	No
Best Choice For:									
Widest Range of Bar Code Printing			X	X				X	
Highest Resolution Printing					X	X			X
Low Resolution or Poor Quality Printing	X	X					X		

NOTES:

10. For "black-on-black" bar codes, use the infrared (820 nm) wands only.
11. For color bar codes the background (spaces) should reflect red light, and the bars should absorb red light.

Certification

FCC Certification (USA Only)

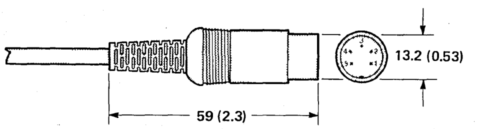
Model	FCC Identification
HBCS-6100 through -61XX	FCC ID: CUP6Z9HBCS-6100 HEWLETT—PACKARD
HBCS-6300 through -63XX	FCC ID: CUP6Z9HBCS-6300 HEWLETT—PACKARD
HBCS-6500 through -65XX	FCC ID: CUP6Z9HBCS-6500 HEWLETT—PACKARD
HBCS-5000 through -5XXX	FCC ID: CUP6Z9HBCS-5000 HEWLETT—PACKARD
HBCS-5100 through -51XX	FCC ID: CUP6Z9HBCS-5100 HEWLETT—PACKARD
HBCS-5200 through -52XX	FCC ID: CUP6Z9HBCS-5200 HEWLETT—PACKARD
HBCS-5300 through -53XX	FCC ID: CUP6Z9HBCS-5300 HEWLETT—PACKARD
HBCS-5400 through -54XX	FCC ID: CUP6Z9HBCS-5400 HEWLETT—PACKARD
HBCS-5500 through -55XX	FCC ID: CUP6Z9HBCS-5500 HEWLETT—PACKARD

This equipment generates radio frequency energy and if not installed and used properly, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference, However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

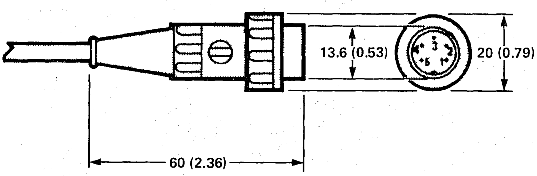
- Reorient the receiving antenna
- Relocate the wand with respect to the receiver
- Move the wand away from the receiver

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20422, Stock No. 004-00345-4.

Interface



HBCS-5XXX



HBCS-6XXX

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).

PIN	WIRE COLOR	FUNCTION
1	RED	V_S SUPPLY VOLTAGE
2	WHITE	V_O OUTPUT
3	BLACK	GROUND
4	N/A	N/C
5	N/A	N/C
CASE	-	SHIELD (MUST BE CONNECTED)

Figure 4. Connector Specifications.

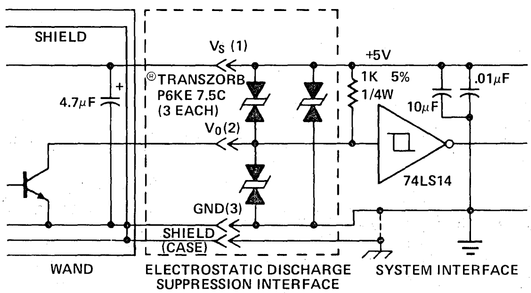


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Figure 5. Recommended Logic Interface (When earth ground is not available, connect shield to logic ground, as shown by dotted line).

The wands include a standard 5 pin, 240° DIN connector. The detailed specifications and pin-outs are shown in Figure 4. Mating connectors are available from RYE Industries and SWITCHCRAFT in both 5 pin and 6 pin configurations. These connectors are listed below.

Connector	Configuration
RYE MAB-5*	5 Pin
SWITCHCRAFT 61GA5F*	5 Pin
SWITCHCRAFT 61HA5F	5 Pin
RYE MAB-6*	6 Pin
SWITCHCRAFT 61HA6F	6 Pin

*Suitable for non-locking connector only.

Maintenance Considerations

There are no user serviceable parts inside the wand. The tip is designed to be easily replaceable, and if damaged it should be replaced. Before unscrewing the tip, disconnect the wand from the system power source. The part number for the wand tip is HBCS-2999 for the HBCS-5XXX family and HBCS-4999 for the HBCS-6XXX family. The tips can be ordered from any Hewlett-Packard authorized distributor.

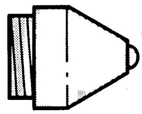


Figure 6A. HBCS-2999 Sapphire Tip

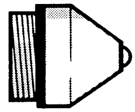
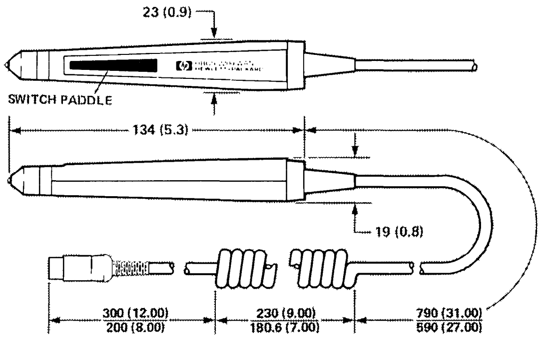


Figure 6B. HBCS-4999 Sapphire Tip

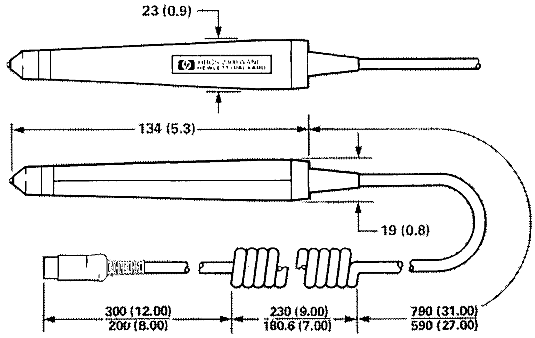
Optional Features

For options such as special cords, connectors or labels, contact your nearest Hewlett-Packard sales office or authorized representative.

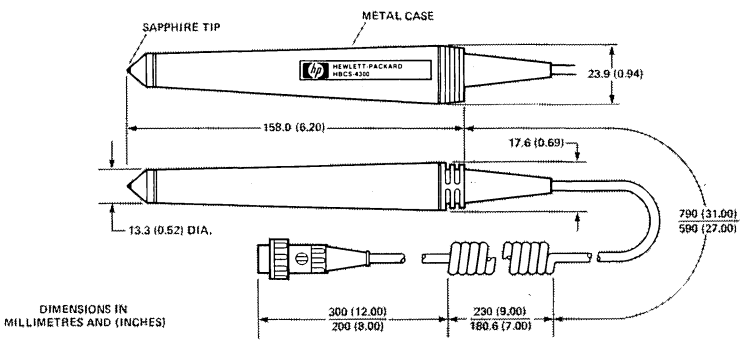
Wand Dimensions



HBCS-50/52/5400



HBCS-51/53/5500



HBCS-6XXX

Figure 7.

HEWLETT PACKARD

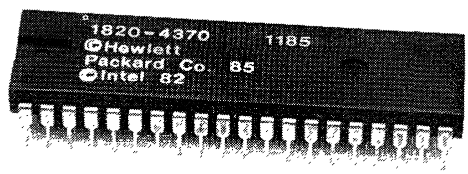
MULTI-PURPOSE BAR CODE DECODER IC

HBCR-2000

TECHNICAL DATA JANUARY 1986

Features

- IDEAL FOR HAND SCANNING APPLICATIONS AND MANY AUTOMATED SCANNING APPLICATIONS
- COMPATIBLE WITH THE SCANNERS NEEDED FOR VIRTUALLY ALL HAND-HELD SCANNING APPLICATIONS
  - — Laser Scanners
  - — Wands
  - — Slot Readers
- WIDE SELECTION OF INDUSTRY STANDARD BAR CODES SUPPORTED
  - — Code 39 (3 of 9 Code)
  - — Extended Code 39
  - — Interleaved 2 of 5 Code
  - — UPC/EAN/JAN Codes
  - — Codabar (NW7 Code)
  - — Code 128
- AUTOMATIC CODE RECOGNITION
- FULL DUPLEX SERIAL ASCII INTERFACE
- EXTENSIVE CONFIGURATION CONTROL THROUGH SOFTWARE COMMANDS
- STANDARD 40 PIN DIP PACKAGE
- AUDIO AND VISUAL FEEDBACK CONTROL
- SINGLE 5 VOLT SUPPLY



Description

Hewlett-Packard's HBCR-2000 Multipurpose Bar Code Decoder IC offers a flexible bar code decoding capability designed to give OEMs the ability to address a large number of industry segments and applications. The decoder IC's flexibility is made possible through sophisticated software which allows the IC to accept data input from a wide variety of digital scanners and to decode the most popular bar code symbologies with full automatic code recognition. Implementation of the decoder IC is easy since it requires only a few supporting chips and provides a standard interface to the host.

The HBCR-2000 is compatible with the scanners needed for virtually all hand scanning applications. Specifically, it is compatible with moving-beam laser scanners such as the Symbol Technologies' LS7000, Symbol Technologies' LS7000 II, and Spectra Physics' SP2001; fixed-beam non-contact scanners; Hewlett-Packard digital wands; and Hewlett-Packard digital slot readers.

The decoder IC is also an excellent decoding solution for a number of the stationary scanning applications found in automated systems. In this case, the scan rates for moving-beam applications must be similar to the scan rates for most hand-held laser scanners (35-45 scans/second) and the scan speeds for fixed-beam applications must be similar to the scan speeds for wands and slot readers. For moving beam applications, it is also important for the scanner to utilize the three laser control lines on the IC.

The standard decoder IC supports the bar code symbologies now being used for most applications in the industrial, retail, commercial, government, and medical markets. The bar codes supported are: Code 39 (3 of 9 Code), Extended Code 39, Interleaved 2 of 5 Code, UPC/EAN/JAN Codes, Codabar (NW7 Code) and Code 128. If more than one code is enabled, the decoder IC will automatically recognize and decode the code being scanned. Bi-directional scanning is allowed for all codes except UPC/EAN/JAN codes with supplemental digits.

The HBCR-2000 communicates with the host through a flexible, full duplex serial ASCII interface. OEMs may choose either to convert this interface to a standard data communications protocol such as RS-232-C/V.24 or to connect the decoder IC directly to another microprocessor for data processing or data re-formatting. Operator feedback is supported through pins that allow for external LED drive and beeper drive circuits. In addition, there are 21 programmable functions covering items from laser redundancy check to the tone of the beeper.

Applications

Bar codes are rapidly becoming a preferred alternative to other forms of data entry. Bar coding has proven faster and more accurate than keyboard data entry. In addition, bar code scanning typically has a higher first read rate and greater data accuracy than optical character recognition. When compared to magnetic stripe encoding, bar code offers significant advantages in flexibility of media, symbol placement and immunity to electromagnetic fields.

Manufacturers of data collection terminals, point-of-sale terminals, keyboards, weighing scales, automated test equipment and other data collection or material handling equipment are finding a growing demand for bar code reading capability in their products. The HBCR-2000 Multipurpose Bar Code Decoder IC makes it easy to add bar code reading capability for a wide variety of applications without the need to invest in the development of bar code decoding software.

Decoder IC Specifications

GENERAL INFORMATION

The HBCR-2000 is an NMOS decoding IC in a 40 pin Dual In-Line package. When configured in a system, the HBCR-2000 requires a crystal and an external 1K byte RAM. The external RAM may be implemented using either a multiplexed RAM chip (Intel 8185 or equivalent) or a non-multiplexed RAM chip and a latch chip (Mostek MK4801 or equivalent and 74LS373). The recommended crystal frequency is 11.059 MHz (CTS Knights R1032-6BA.11.059 or equivalent).

The decoder IC is designed to interface with most standard microprocessors or other host systems through a full duplex serial asynchronous ASCII port. It offers complete compatibility with Hewlett-Packard digital wands and digital slot readers as well as hand-held laser scanners from both Spectra Physics, Inc. and Symbol Technologies, Inc. Other scanners, such as hand-held fixed-beam non-contact scanners and the scanners used in some stationary scanning applications, may also be used with the IC.

Performance Features

BAR CODES SUPPORTED

The HBCR-2000 decoder IC is capable of reading six popular bar code symbologies: Code 39 (3 of 9 Code), Extended Code 39, Interleaved 2 of 5 Code, UPC/EAN/JAN Codes, Codabar (NW7 Code), and Code 128.

Code 39, an alphanumeric code, and Extended Code 39, a full 128 character ASCII version of Code 39, may be read bi-directionally for message lengths up to a maximum of 32 characters. An optional check character may be used with these codes, and the decoder IC may be configured to verify this character prior to data transmission. Enabling Extended Code 39 will disable standard Code 39 as the two are mutually exclusive.

The Interleaved 2 of 5 Code, a compact numeric only bar code, may also be read bi-directionally for message lengths from 4 to 32 characters. To enhance data accuracy, optional check character verification and/or label length checking may be enabled.

All popular versions of the UPC, EAN, and JAN bar codes may be read bi-directionally, including UPC-A, UPC-E, EAN-8, EAN-13, JAN-8, and JAN-13. All codes may be enabled simultaneously or only the UPC codes may be enabled. UPC, EAN, and JAN symbols with complementary two digit or five digit supplemental encodations, or "add-ons", may also be read.

Codabar, a numeric only bar code with special characters, may be read bi-directionally for message lengths up to a maximum of 32 characters. The start and stop characters in the symbol are normally transmitted, but transmission of these characters may be disabled through a software command.

Code 128, a compact full ASCII bar code, may also be scanned bi-directionally for message lengths up to a maximum of 32 characters.

Automatic code recognition is provided for the Interleaved 2 of 5 Code, UPC/EAN/JAN Codes, Codabar, Code 128, and either Code 39 or Extended Code 39. Any subset of these codes may be selected for decoding. The decoder IC's default setting is for simultaneous reading of Code 39, Interleaved 2 of 5 Code with variable lengths, UPC/EAN/JAN Codes without supplements, Codabar, and Code 128.

SCANNER INPUT

The HBCR-2000 is designed to accept a digital input signal either from a fixed-beam scanner, such as a wand, slot reader, or fixed-beam non-contact scanner, or from a moving-beam scanner such as a hand-held laser scanner. The state of pin 7 must be set prior to power-up to reflect the type of scanner connected to the decoder IC.

The decoding software has been specially designed to operate with any of Hewlett-Packard's digital bar code wands. Sapphire-tip digital wands feature a scan angle of 0 to 45 degrees, a variety of resolutions, and a TTL compatible digital output. A complete wand selection guide is presented in Table 2.

The decoder IC is also designed specifically for operation with Hewlett-Packard's digital slot readers. These slot readers feature a sealed case with a slot width of 3.2 mm (0.125 in.) and either an infrared (880 mm) or visible red (660 mm) LED light source. A separate module which contains the slot reader optics and electronics is available for stationary scanning applications or for configuration in applications requiring a different slot width.

The decoding software for moving-beam scanners has been designed to work with hand-held laser scanners manufactured by Spectra Physics, Inc. and Symbol Technologies, Inc. The delay time for automatic laser shutoff is adjustable through a software command to the IC. A redundancy check feature is available for applications which require extreme accuracy. Applications which require and ability to sense motor failure in a laser scanner or to calculate the ratio of laser on-time to laser off-time must support these requirements through external hardware.

The digital input signal from the scanner is connected to pin 12. When the decoder IC is used with a hand-held laser scanner, the laser enable, laser trigger, and scanner synchronization signal lines are connected to pins 6, 8, and 13, respectively. Scanner input can be disabled by the host system though a software command. This allows the application program to enable bar code data entry only when expecting the operator to enter data which has been encoded in bar code. The decoder IC also offers a single read mode which can; be enabled through a software command. The single read mode allows the application program to prevent bar code data entry until a "Next Read" command is sent, thereby allowing the host to process transmissions and verify each scan before enabling subsequent decodes.

DATA COMMUNICATIONS

The decoder IC can communicate with the host system through a full-duplex, asynchronous, serial ASCII port. A wide range of baud rate, parity, stop bits, and terminator characters may be selected, as described in Table 1. In addition, both request-to-send/clear-to-send hardware handshake and X_{ON}/X_{OFF} (DC1/DC3) character pacing are available for control of the decoder IC's data transmission.

OPERATOR FEEDBACK

The decoder IC has several provisions for signalling operator feedback. Pin 14 provides a signal for an LED driver and pin 15 provides a signal for a beeper driver. An LED or beeper driver connected to the decoder IC may either be connected to the decoder IC may either be controlled directly by the IC, with a signal generated after a good read, or may be controlled by the host system. In addition, the tone of the beeper can be varied by a software command to be one of 16 tones or the beeper may be silenced.

POWER REQUIREMENTS

The decoder IC operates from a single SV DC power supply. The maximum current draw is 175 mA. The maximum ripple voltage for the power supply should be less than 100 mV peak-to-peak.

CONFIGURATION CONTROL

Configuration of the decoder IC may be determined through hardwire connections and/or through software commands. Hardwire selection is limited to key operating parameters. A much greater range of configuration control is available through software commands. A summary of the decoder IC features and the configuration control available for these features is presented in Table 1. A users manual which provides detailed configuration information and example schematics is suplied with the HBCR-2000.

Handling Precautions

The decoder IC is extremely sensitive to electrostatic discharge (ESD). It is important that good anti-static procedures be observed when handling the IC. The package should not be opened except in a static free environment.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{CC}	4.5		5.5	V	1
Ambient Temperature	T_A	0		70	°C	
Crystal Frequency	XTAL		11.059		MHz	2
Element Time Interval (Moving-Beam)	ETI_M	22		555	µsec	2, 3, 4, 5
Element Time Interval (Fixed-Beam)	ETI_F	150		70,000	µsec	2, 3, 5, 6, 7

NOTES:

1. Maximum power supply ripple of 100 mV peak-to-peak.
2. Crystal frequencies from 3.5 Mhz to 12 MHz may be used. For frequencies other than 11.059 Mhz, multiply the specified baud rates, beeper frequencies, and element time interval ranges by $\frac{\text{XTAL}}{\text{11.059 MHz}}$. The ETI ranges specified assume a crystal frequency of 11.059 MHz.
3. An element time interval (ETI) is the time period in the digital signal from the scanner that corresponds to the physical width of a printed element bar (bar or space) in the bar code symbol ETI_M applies when pin 7 is tied low and ETI_F applies when pin 7 is tied high.
4. Corresponds to a scan rate of 35 to 45 scans per second, a scan rate which is common for hand-held laser scanners.
5. Element time intervals which are smaller than the minimum ETI's specified will still be processed, but with additional width errors that may cause the input signal to be undecodable.
6. The maximum scan speed may be calculated by dividing the smallest narrow element width by 150 µsec. For example, for 0.19 mm (0.0075 in.) narrow elements, the maximum scan speed is 127 cm/sec (50 in./sec).
7. The minimum scan speed may be calculated by dividing the largest wide element width by 70,000 µsec. For example, for 1.52 mm (0.060 in.) wide elements, the minimum scan speed is 2.2 cm/sec (0.9 in./sec).

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	−65	+150	°C	
Pin Voltage	V_{IN}	−0.5	+7.0	V	8
Power Dissipation	P_D		1.5	Watts	

Note:

8. Voltage on any pin with respect to ground.

BAR CODE COMPONENTS

TABLE 1. SUMMARY OF FEATURES AND CONFIGURATION CONTROL

	Feature	Function or Value	Hardwire/ Software Control[9]	Default Setting[10]
Scanner Selection/Control	Scanner Type	Wand/Slot Reader or Moving Beam Laser Scanner	Hardwire	Moving Beam Laser Scanner
	Laser Shutoff Delay	Defines Laser On-Time prior to Automatic Shutoff from 0 to 10 seconds in 100 ms steps	Software	3 seconds
	Laser Redundancy Check	Enables Requirement for Two Consecutive, Identical Decodes for a Good Read	Software	Not Enabled
	Scanner Input Enable	Enables Data Acquisition from Scanner	Software	Enabled
	Single Read Mode	Enables Requirement for a 'Next Read' Command before Processing the next Scanner Input Signal	Software	Not Enabled
Code Selection	Code Select	Extended Code 39	Both	Code 39 Interleaved 2 of 5 Code UPC/EAN/JAN Codes Codabar Code 128
		Code 39 Interleaved 2 of 5 Code UPC/EAN/JAN Codes Codabar Code 128	Software	
	UPC/EAN/JAN Decoding Options	UPC/EAN/JAN together; or UPC Only	Software	UPC/EAN/JAN together
		Enable 2 or 5 Digit Supplements	Software	Supplements Not Enabled
	Check Character Verification Enable	Code 39 Check Character	Both	No Check Character Verification
		Interleaved 2 of 5 Code Check Character	Software	
	Codabar Data Transmission Option	Transmit or Suppress Start/Stop Characters	Software	Transmit
	Interleaved 2 of 5 Label Length Check	User Defined from 4 to 32 Characters or Variable Length	Software	Variable Length
Data Communications	Baud Rate	1200, 2400, 4800, 9600	Hardwire	1200
	Parity	0's, 1's, Odd, Even	Hardwire	0's
	Stop Bits	1 or 2	Hardwire	1
	Terminator Character	CR, CR/LF, ETX, None	Hardwire	CR
		User Defined (10 Characters Max.)	Software	
	Header Character	User Defined (10 Characters Max.)	Software	No Header Character
	Data Output Pacing	RTS/CTS	Hardwire	No Pacing
		X_{ON}/X_{OFF}	Software	
Operator Feedback	Good Read Beep Select	Enables Good Read Beep and sets 1 of 16 tones	Software	Beep Enabled; Tone 12
	Sound Tone	External Command to Initiate Beep Signal in 1 of 16 tones	Software	N/A
	LED Control	Defines LED Control to be Internal, External, or both	Software	LED to Flash Automatically Upon Good Read
System Control	Status Request	Gives Status of Decoder IC Configuration	Software	N/A
	Hard Reset	Resets Decoder IC to Hardwire Configuration and Default Software Settings	Software	N/A

NOTES:

9. Hardwire control is accomplished by tying the appropriate input pins high or low. Software commands are sent by means of escape sequences.
10. Default settings are those settings which result when the relevant input pins have been tied to Ground and no software commands have been sent to the decoder IC.

Pinout

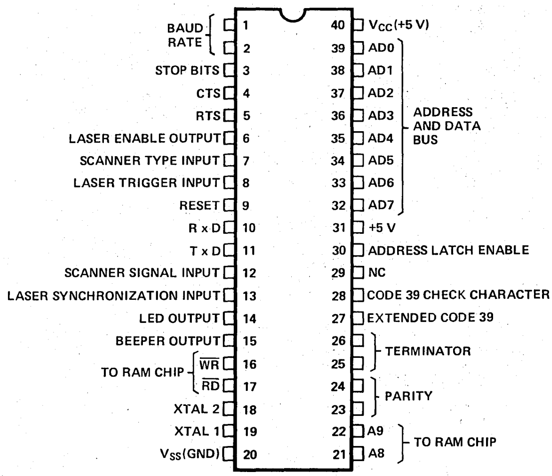


Figure 1.

Block Diagrams

DECODER IC TO MEMORY

1K x 8 RAM WITH ADDRESS LATCH CHIP

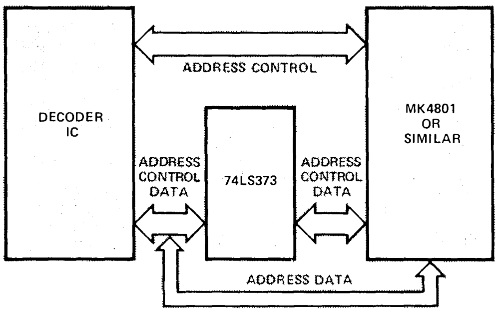


Figure 2.

8185 MULTIPLEXED 1K x 8 RAM

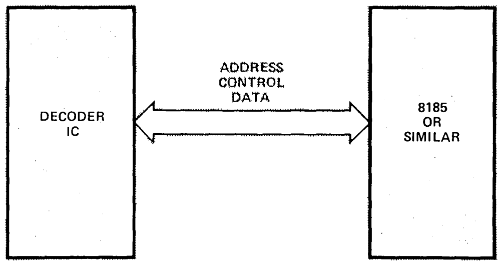


Figure 3.

Scanner Compatibility

The HBCR-2000 is compatible with the complete line of Hewlett-Packard digital wands, Hewlett-Packard digital slot readers, and hand-held laser scanners manufactured by both Symbol Technologies, Inc. and Spectra Physics, Inc.

The selection of Hewlett-Packard digital wands available for use with the HBCR-2000 is presented in Table 2. For the two families of sapphire-tip digital wands, the most widely used wands are those which specify a recommended nominal narrow element width of 0.19 mm (0.0075 in.). These wands are capable of reading bar codes printed with a variety of different printers and over a wide range of printed resolutions (as specified by narrow element widths) and are, therefore, considered to be general-purpose wands. The higher resolution wands, with a recommended nominal narrow element of 0.13 mm (0.005 in.), are recommended for applications in which only high resolution bar codes are being read. For applications which require a scanner to read medium or low resolution bar codes, particularly those with edge roughness, ink smearing, spots and voids, or other minor print flaws, the wands which specify a recommended nominal narrow element width of 0.3 mm (0.012 in.) or 0.33 mm (0.013 in.) are recommended.

The Hewlett-Packard slot readers and slot reader modules which are available for use with the HBCR-2000 are presented in Table 3. The standard slot readers have a slot width of 3.2 mm (0.125 in.) and are, therefore, capable of reading bar codes on anything from paper to double-laminated badges. For applications which require a different slot width or which require a fixed-beam scanner in an automated system, a module which contains the slot reader optics and electronics assembly is also available.

The hand-held laser scanners compatible with the HBCR-2000 include the Symbol Technologies' LS7000, Symbol Technologies' LS7000 II, and Spectra Physics' SP2001. For detailed information on these scanners, please contact these companies directly.

TABLE 2. HEWLETT-PACKARD DIGITAL BAR CODE WANDS

	Part Number	Recommended[11, 12] Nominal Narrow Element Width	Emitter[13] Wavelength	Tilt Angle	Typical Current	Case Material	Switch	Tip
Low Cost	HEDS-3000	0.3 mm (0.012 in.)	700 nm	0-30°	42 ma	ABS Plastic	Yes	Open
	HEDS-3050	|	|	|	|	|	No	|
	HEDS-3200	0.19 mm (0.0075 in.)	820 nm	|	35 ma	|	Yes	|
	HEDS-3250	|	|	|	|	|	No	|
Sapphire-Tip	HBCS-2200	0.19 mm (0.0075 in.)	700 nm	0-45°	42 ma	Polycarbonate	Yes	Sapphire Ball
	HBCS-2300	|	|	|	|	|	No	|
	HBCS-4300	|	|	|	|	Metal	|	|
	HBCS-2400	0.13 mm (0.005 in.)	820 mm	|	|	Polycarbonate	Yes	|
	HBCS-2500	|	|	|	|	|	No	|
	HBCS-4500	|	|	|	|	Metal	|	|
Low Current Sapphire-Tip[14]	HBCS-5000	0.33 mm (0.013 in.)	655 nm	0-45°	3.5 ma	Polycarbonate	Yes	Sapphire Ball
	HBCS-5100	|	|	|	|	|	No	|
	HBCS-6100	|	|	|	|	Metal	|	|
	HBCS-5200	0.19 mm (0.0075 in.)	|	|	|	Polycarbonate	Yes	|
	HBCS-5300	|	|	|	|	|	No	|
	HBCS-6300	|	|	|	|	Metal	|	|
	HBCS-5400	0.13 mm (0.005 in.)	820 mm	|	|	Polycarbonate	Yes	|
	HBCS-5500	|	|	|	|	|	No	|
	HBCS-6500	|	|	|	|	Metal	|	|

NOTES:

11. The nominal narrow element width of a symbol may also be referred to as the resolution of the symbol or as the 'x' dimension of the symbol.
12. Nominal narrow element (bar/space) width, a term which applies to the symbol and not to the scanner itself, is specified to facilitate selecting the best scanner for the symbol being read. The scanners are designed to accomodate printing tolerances around the nominal dimension specified. Bar codes having larger nominal narrow element widths (ie. lower resolution) than specified may also be read as long as print quality is good.
13. Wands with an emitter wavelength of 655 mm are recommended for reading bar codes printed on regular (white) thermal paper or printed with Hewlett-Packard's Thinkjet printer. Either 655 mm or 700 mm wands are recommended for bar codes printed with dye-based ink or in color.
14. Low current sapphire-tip wands are designed to operate in all ambient light environments including in direct sunlight and under high intensity lamps.

TABLE 3. HEWLETT-PACKARD DIGITAL SLOT READERS

Part Number	Configuration	Recommended[15] Nominal Narrow Element Width	Emitter[16] Wavelength	Temperature Range	Case Material
HBCS-7000	Complete Slot Reader	0.19 mm (0.0075 in.)	660 nm	-20 to +55°C	Metal
HBCS-7001	Slot Reader Module	|	660 nm	|	|
HBCS-7100	Complete Slot Reader	0.19 mm (0.0075 in.)	880 nm	-40 to +70°C	|
HBCS-7101	Slot Reader	|	880 nm	|	|

NOTES:

15. The aperture design of the slot reader optical system allows reading both high resolution bar code symbols and poorly printed medium or low resolution bar code symbols with the same scanner.
16. The 880 nm slot reader is recommended for bar code symbols printed with carbon-based inks or for "black-on-black" bar code symbols. The 660 nm slot reader is recommended for bar code symbols printed with dye-based inks or printed on regular thermal paper.

HEWLETT PACKARD

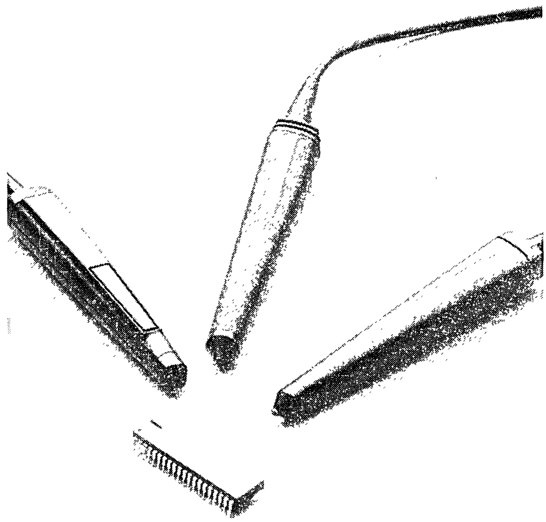
COMPONENT BAR CODE READERS

HBCR-1000
HBCR-1022
HBCR-1024
HBCR-1025
HBCR-1043
HBCR-1045

TECHNICAL DATA JANUARY 1986

Features

- **INDUSTRY STANDARD BAR CODES**
  - **3 of 9 Code**
  - **Extended 3 of 9 Code**
  - **Interleaved 2 of 5 Code**
  - **UPC/EAN/JAN Codes**
- **AUTOMATIC CODE RECOGNITION**
- **FULL DUPLEX SERIAL OR PARALLEL ASCII OUTPUT**
- **EXTENSIVE CONFIGURATION CONTROL THROUGH SOFTWARE COMMANDS**
- **DECODER IC IN A STANDARD 40 PIN DIP PACKAGE**
- **HIGH PERFORMANCE DIGITAL WANDS**
  - **45 Degree Scan Angle**
  - **Sealed Sapphire Tip**
  - **Polycarbonate or Metal Case**
  - **Wide Operating Temperature Range**
- **AUDIO AND VISUAL FEEDBACK CONTROL**
- **SINGLE 5 VOLT SUPPLY**



Description

Hewlett-Packard's HBCR-1000 series Component Bar Code Readers are high performance product sets designed to simplify the implementation of bar code reading capability in any OEM system. The standard 40 pin decoder IC has been specially designed to work with any of several Hewlett-Packard sapphire tip, digital wands. When combined with an external RAM chip, the result is a component-level reader that allows a manufacturer to easily add bar code reading to his equipment.

The standard decoding chip supports four of the most popular codes: 3 of 9 Code, Extended 3 of 9 Code, Interleaved 2 of 5 Code, and UPC/EAN/JAN Codes. If more than one standard code is enabled, the reader will automatically recognize and decode the code being scanned. Bi-directional scanning is allowed for all codes except UPC/EAN/JAN with supplemental digits. For 3 of 9 Codes and Interleaved 2 of 5 Code, a maximum of 32 characters (not including start and stop characters) are allowed.

The decoder IC may be set to communicate in either serial or parallel ASCII. Operator feedback is supported through pins that allow for external LED drive and a beeper drive circuits. In addition, there are thirteen programmable functions covering items from terminator character selection to the tone of the beeper.

The readers are standard with your choice of sapphire tip wands (see Reader Selection Guide, page 8). These wands feature scan angles from 0 to 45 degrees, advanced H-P optics, and are available in a wide choice of resolutions and constructions to suit a variety of needs.

Applications

Bar codes are rapidly becoming a preferred alternative to other forms of data entry. Bar coding has proven faster and more accurate than keyboard entry. In addition, bar code scanning typically has a higher first read rate and greater data accuracy than Optical Character Recognition. When compared to magnetic stripe encoding, bar code offers significant advantages in flexibility of media, symbol placement and immunity to electromagnetic fields.

Manufacturers of data collection terminals, point-of-sale terminals, keyboards, weighing scales, and other data collection and material handling equipment are finding a growing demand for bar code reading capability in their products. The HBCR-1000 series Component Bar Code Readers make it easy to add this capability without the need to invest in the development of bar code decoding software.

The 40 pin decoder IC may be easily configured with most common microprocessors using either a parallel ASCII or serial ASCII interface. The IC may be added to an existing board, designed into an add-on board, or designed into an entirely new system. Using the decoder IC as an integral part of the host system will eliminate the need for the external bar code readers which are often used to perform the same function.

Decoder IC Specifications

General Information

The HBCR-1000 series of Component Bar Code Readers consists of an NMOS decoding IC in a 40 pin Dual In-Line package, and a high performance digital bar code wand with a sapphire tip. The readers require an external 1K x 8 bit multiplexed RAM chip (Intel 8185 or similar) or a 1K by 8 bit RAM and an address latch chip (Mostek MK4801 or similar and a 74LS373). To complete the reader, a 12 MHz crystal must also be added.

The decoding IC is designed to interface with most standard microprocessors, and can communicate in either serial or parallel ASCII. It provides complete compatibility with the output from Hewlett-Packard digital bar code wands.

Performance Features

Bar Codes Supported

The decoder IC in the HBCR-1000 series of Component Bar Code Readers is capable of reading four popular bar code symbologies: 3 of 9 Code, Extended 3 of 9 Code, Interleaved 2 of 5 Code and UPC/EAN/JAN Codes.

The 3 of 9 Code, an alphanumeric code, and the Extended 3 of 9 Code, a full 128 character ASCII version of the 3 of 9 Code, may be read bi-directionally for message lengths up to a maximum of 32 characters. An optional checksum character may be used with these codes, and the decoder IC may be configured to verify this character prior to data transmission. Enabling the Extended 3 of 9 Code will disable the standard 3 of 9 Code as the two are mutually exclusive.

The Interleaved 2 of 5 Code, a compact numeric only bar code, may also be read bi-directionally for message lengths up to a maximum of 32 characters. To enhance data accuracy, an optional checksum character verification and/or label length checking may be enabled.

All popular versions of the UPC, EAN, and JAN bar codes may be read bi-directionally, including UPC-A, UPC-E, EAN-8, EAN-13, JAN-8, and JAN-13. All codes may be enabled simultaneously or only the UPC codes may be enabled.

UPC, EAN and JAN codes with complementary two digit or five digit supplemental encodations, or "add-ons", may also be read in one of two ways. If UPC, EAN and JAN codes are enabled but neither two digit nor five digit supplemental encodations are enabled, then only the main part of the symbols printed with supplemental encodations will be read. If the two digit or the five digit supplemental encodations are enabled, then only symbols with these supplementals will be read. In this case, the symbols may only be read in the direction which results in the supplement being scanned last.

Automatic code recognition is provided for the Interleaved 2 of 5 Code, UPC/EAN/JAN Codes, and either the 3 of 9 Code or the Extended 3 of 9 Code. The decoder IC's default setting is for simultaneous reading of the 3 of 9 Code, Interleaved 2 of 5 Code and UPC/EAN/JAN Codes.

Wand Input

The decoder IC has been specially designed to operate with any of several Hewlett-Packard sapphire tip, digital bar code wands. All of these wands feature scan angles from 0 to 45 degrees, TTL compatible digital output, and single 5 volt supply. Scanning speeds range from 7.6 cm/sec (3 in./sec) to 127 cm/sec (50 in./sec).

Wand input can be disabled by the host system through a software command. This allows the application program to control the operator's ability to enter bar code data, thereby preventing inadvertant data entry and allowing the host to verify each scan before enabling subsequent scans.

The wand is connected to pin 12 of the decoder IC (see Figures 1 and 2).

Data Communications

The decoder IC can communicate with the host system through either a serial ASCII or parallel ASCII port. The parallel port allows for faster data communication between the two devices. Both parallel and serial ports are bi-directional.

The serial port may also be connected directly to RS-232-C level shifters to produce an RS-232-C compatible output. A wide range of baud rate, parity, stop bits and terminator characters may be selected, as described in Table 1. In addition, XON/XOFF pacing for the decoder IC's data transmission is available.

The parallel port utilizes both a send and receive handshake for data transfer between the decoder IC and the host system. Timing diagrams for these handshakes are shown on page 5.

The decoder IC has a 255 character output buffer which will store data if transmission to the host is prevented. A buffer overflow will actuate a signal on the beeper line for the beeper to sound three times in rapid succession.

Feedback Features

The decoder IC has several provisions for signalling operator feedback. Pin 14 provides a signal for an LED driver and pin 15 provides a signal for a beeper driver. An LED or beeper driver connected to the decoder IC may be controlled directly by the IC, with a signal generated after a good read; or may be controlled by the host system. In addition, the tone of the beeper can be varied by a software command to be one of 16 different tones.

Power Requirements

Both the decoder IC and the wands operate from a single +5 V DC power supply. The maximum current draw for the decoder IC is 175 mA. The maximum current draw for the wands is 50 mA. For both the IC and the wand power supplies, the maximum ripple voltage should be less than 100 mV peak-to-peak.

Configuration Control

Configuration of the decoder IC may be determined through hardwire connections and/or through software commands. Hardwire selection is limited to key operating parameters. A much greater range of configuration control is available through software commands. A summary of the decoder IC features and configuration control these features is presented in the following table.

Table 1. Summary of Features and Configuration Control

Feature	Function of Value	Hardwire/ Software Control[1]	Default Setting[2]	Mode[3]	Notes
Mode of Operation	Parallel or Serial Mode	Hardwire	Parallel	N/A	
Baud Rate	300, 1200, 2400, 9600	Hardwire	300 Baud	Serial	
Parity	0's, 1's, Odd, Even	Hardwire	0's	Serial	4
Stop Bits	1 or 2	Hardwire	2	Serial	
Terminator Character	CR, CR/LF, HT, None	Hardwire	CR	Serial	
	User Defined (10 Characters Max.)	Software	CR	Both	5
Header Character	User Defined (10 Characters Max.)	Software	No Header Character	Both	
Data Output Pacing	XON/XOFF	Software	No Pacing	Both	
Industrial Code Select	3 of 9 Code Interleaved 2 of 5 Code	Software	3 of 9 Code Interleaved 2 of 5 Code	Both	
	Extended 3 of 9 Code	Both			
UPC/EAN/JAN Code Select	UPC/EAN/JAN together; or UPC Only	Software	UPC/EAN/JAN Codes		
	Enable 2 or 5 Digit Supplements	Software	Supplements Not Enabled		
	Suppress Zeros UPC-E	Software	Zeros Included		
Checksum Verification Enable	3 of 9 Code Checksum	Both	No Checksum Verification	Both	
	Interleaved 2 of 5 Checksum	Software			
Interleaved 2 of 5 Label Length Check	User Defined up to 32 Characters or Variable Length	Software	Variable Length	Both	
Scanner Disable	Disables Wand Input	Software	Wand Input Enabled	Both	
Good Read Beep Select	Enables Good Read Beep in one of 16 Tones	Software	Beep Signal Enabled; Tone = 15	Both	
Sound Tone	External Command to Sound Tones Defines 1 of 16 Tones	Software	N/A	Both	
LED Control	Controls LED Driver Circuit	Software	LED to Flash Upon Good Read	Both	
Status Request	Gives Status of Decoder IC Configuration	Software	N/A	Both	
Hard Reset	Resets Decoder IC to Hardwire Configuration and Default Software Settings	Software	N/A	Both	

Notes:
1. Software commands are sent by means of escape sequence.
2. Default settings are those settings which result when the relevant pins have been tied to +5V and no software commands have been sent to the decoder IC.
3. Some functions apply only when the decoder IC is operating in the serial mode. Others apply in both the parallel and serial modes.
4. In the parallel mode, the parity is always odd.
5. In the parallel mode the terminator character is "CR" unless changed through software commands.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{CC}	4.5		5.5	V	7
Ambient Temperature	T_A	0		70	°C	
Crystal Frequency	XTAL		12		MHz	8

Note:
7. Maximum power supply ripple of 100 mV peak-to-peak.
8. 12 MHz crystal is recommended.

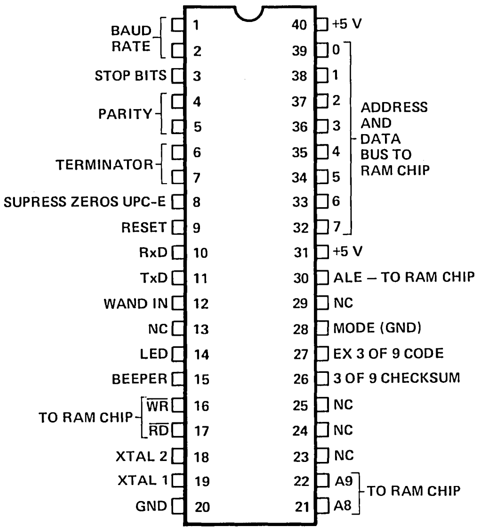
Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	−65	+150	°C	
Pin Voltage	V_{IN}	−0.5	+7.0	V	9
Power Dissipation	P_D		2.0	Watts	

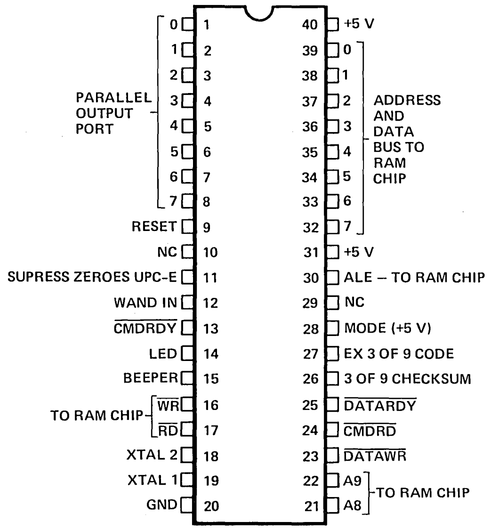
Note:
9. Voltage on any pin with respect to ground.

Block Diagrams

SERIAL PINOUT



PARALLEL PINOUT



NC — Pins should be left floating

Figure 1.

Figure 2.

DECODER IC TO MEMORY

8185 MULTIPLEXED 1K x 8 RAM

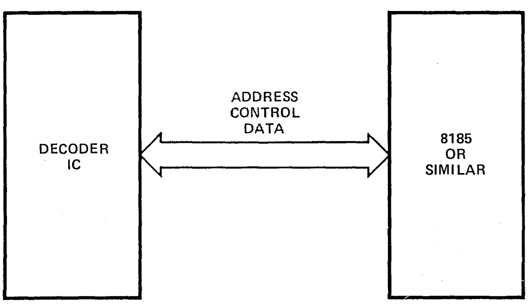


Figure 3.

1K x 8 RAM WITH ADDRESS LATCH CHIP

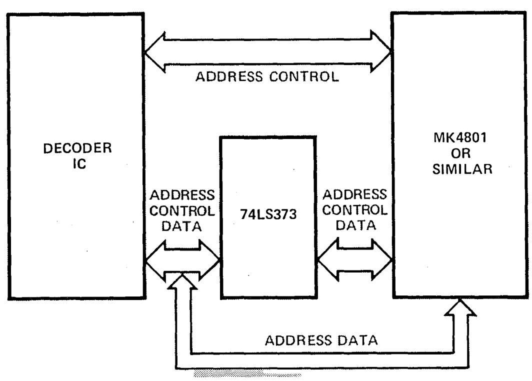
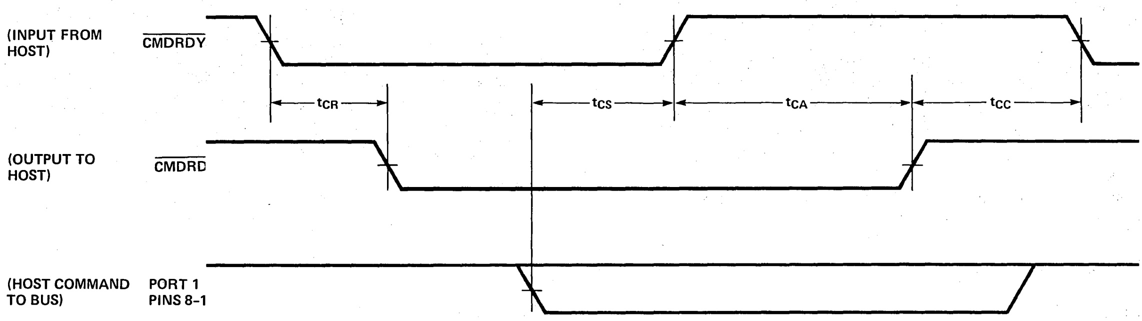


Figure 4.

Parallel Mode Handshake Timing

HOST COMMANDS RECEIVED BY DECODER IC



*t_{CR} = Falling edge of $\overline{\text{COMMAND READY}}$ to falling edge of $\overline{\text{COMMAND READ}}$. Max. = 22 μs (MICRO SECONDS).

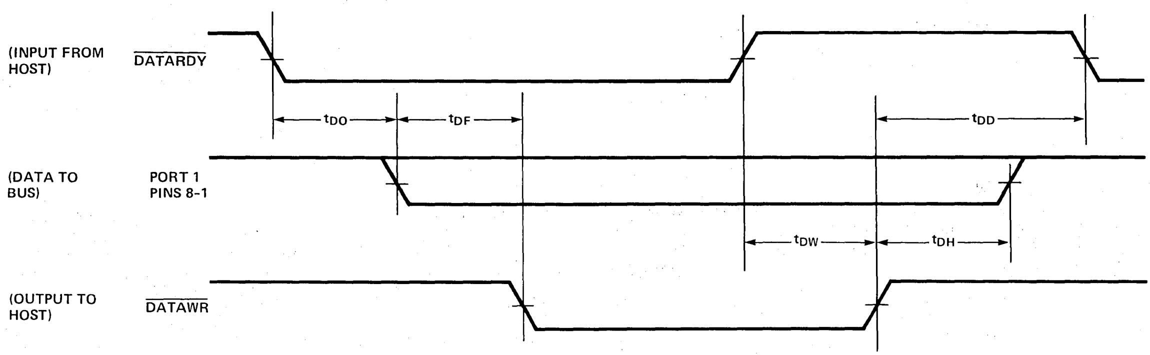
t_{CS} = Command setup to rising edge of $\overline{\text{COMMAND READY}}$. Min. = 0 μs.

*t_{CA} = Rising edge of $\overline{\text{COMMAND READY}}$ to rising edge of $\overline{\text{COMMAND READ}}$. Typical = 6 μs.

t_{CC} = Rising edge of $\overline{\text{COMMAND READ}}$ to falling edge of $\overline{\text{COMMAND READY}}$. Min. = 0 μs.

***Note:** These timing specifications given are based on the assumptions that the wand is not active at the time. Since the wand input to the microprocessor is interrupt driven, the timing might be stretched if the wand is active during that time. All the timings assume the microprocessor runs at 12 MHz.

DECODER IC DATA SENT TO HOST



*t_{DO} = Falling edge of $\overline{\text{DATA READY}}$ to data output to bus. Max. = 140μs.

This number reflects that there is no decoding in progress, no status, terminal ID, header or terminator change command is being executed at the time.

*t_{DF} = Data output to bus to falling edge of $\overline{\text{DATA WRITE}}$. Max. = 2 μs

*t_{DW} = Rising edge of $\overline{\text{DATA READY}}$ to rising edge of $\overline{\text{DATA WRITE}}$. Max. = 5 μs.

*t_{DH} = Data hold after rising edge of $\overline{\text{DATA WRITE}}$. Max. = 2 μs.

t_{DD} = Rising edge of $\overline{\text{DATA WRITE}}$ to falling edge of $\overline{\text{DATA READY}}$. Min. = 0 μs.

DC Characteristics ($T_A = 0°C$ to $70°C$, $V_{CC} = 4.5V$ to $5.5V$, $V_{SS} = 0V$)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (except Pins 9 and 18)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (Pins 9 and 18)	2.5	V_{CC} + 0.5	V	Pin 19 to V_{SS}
V_{OL}	Output Low Voltage (Pins 1-8, 10-17, 21-28)		0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage (Pins 30 and 32-39)		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage (Pins 1-8, 10-17 and 21-28)	2.4		V	I_{OH} = −80 μA
V_{OH1}	Output High Voltage (Pins 30 and 32-39)	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Low Current (Pins 1-8, 10-17 and 21-28)		−800	μA	V_{IN} = 0.45V
I_{IL2}	Input Low Current (Pin 18)		−2.5	mA	Pin 19 to V_{SS}; V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Pins 32-39)		±10	μA	0.45 < V_{IN} < V_{CC}
I_{IH1}	Input High Current to Pin 9 for Reset		500	μA	V_{IN} = V_{CC} −1.5
I_{CC}	Power Supply Current		175	mA	All Outputs Disconnected

BAR CODE COMPONENTS

Handling Precautions

The decoder IC is extremely sensitive to electrostatic discharge (ESD). It is important that good anti-static procedures be observed when handling the IC. It is recommended that the package not be opened except in a static free environment.

Wand Specifications

General Information

Hewlett-Packard's Sapphire Tip Digital Bar Code Wands are hand-held scanners optimized to provide excellent reading of all common bar code formats. These wands contain an optical sensor with a 700 nm visible red LED (HBCS-2200/-2300/-4300) or an 820 nm infrared LED (HBCS-2400/-2500/-4500), a photo detector IC, and precision aspheric optics. The internal conditioning circuitry converts the optical information into a logic level pulse width representation of the bars and spaces.

The HBCS-2200/-2300/-4300 with their nominal 0.19 mm (0.0075 in.) spot size, are excellent choices for reading a general range of bar code. The HBCS-2400/-2500/-4500 wands have a nominal spot size of 0.13 mm (0.005 in.) and are ideal for reading very high density bar code.

The HBCS-2XXX series of wands feature a durable, polycarbonate case. They are the ideal choices for general purpose commercial and light industrial applications. The HBCS-4XXX series of wands feature a rugged metal case and are recommended for heavy industrial and LOGMARS applications.

The standard wand configuration includes a strain-relieved coiled cord which has a comfortable extended length of 190 cm (75 in.). Maximum length is 250 cm (100 in.). The standard connector on the HBCS-2XXX family of wands is a 5 pin, 240 degree DIN connector. The connector on the HBCS-4XXX family is a metal, 5 pin, 240 degree DIN connector with a locking ring. Mating sockets for both connectors are listed under the Mechanical Considerations section.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Nominal Narrow Element Width HBCS-2200/2300/4300		0.19 (0.0075)		mm (in.)	
HBCS-2400/2500/4500		0.13 (0.005)		mm (in.)	
Scan Velocity	V_{SCAN}	7.6 (3)	127 (50)	cm/sec (in./sec)	
Contrast	R_W-R_B	45		%	10
Supply Voltage	V_S	4.5	5.5	Volts	11
Temperature	T_A	−20	+65	°C	
Tilt Angle	(See Figure 5)				12
Orientation	(See Figure 6)				

Notes:

10. Contrast is defined as R_W-R_B, where R_W is the reflectance of the white spaces and R_B is the reflectance of the black bars measured at the emitter wavelength (700 nm or 820 nm). Contrast is related to print contrast signal (PCS) by PCS = R_W-R_B/R_W or R_W-R_B = PCS*R_W).
11. Power supply ripple and noise should be less than 100 mV peak to peak.
12. Performance in sunlight will vary depending on shading at wand tip.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	−40	+75	°C	
Operating Temperature	T_A	−20	+65	°C	
Supply Voltage HBCS-2200/2300/4300	V_S	−0.5	+6.00	V	
HBCS-2400/2500/4500	V_S	−0.5	+5.75	V	
Output Transistor Power	P_T		200	mW	
Output Collector Voltage	V_O	−0.5	+20	V	

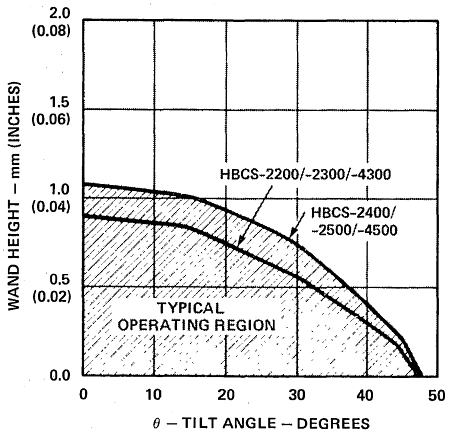


Figure 5. Wand Height vs. Tilt Angle

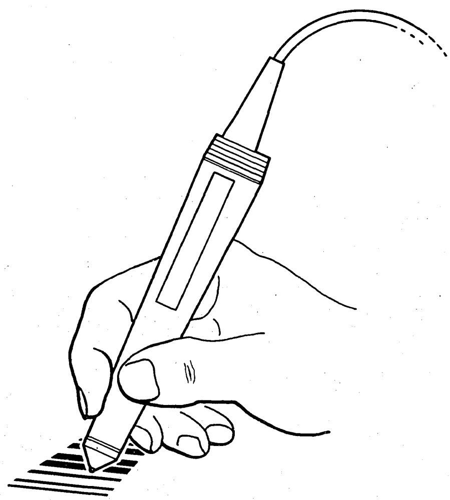


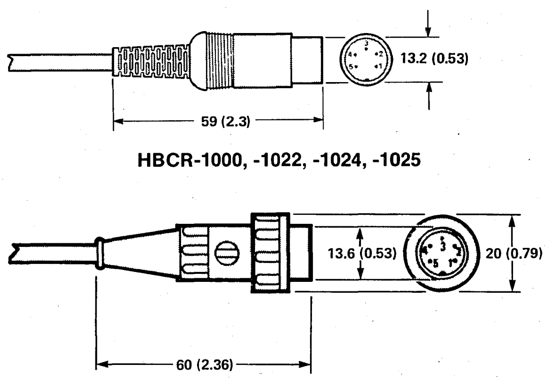
Figure 6. Preferred Orientation

Mechanical Considerations

The wands include a standard 5 pin, 240° DIN connector. The detailed specifications and pin-outs are shown in Figure 7. Mating connectors are available from RYE industries and SWITCHCRAFT in both 5 pin and 6 pin configurations. These connectors are listed below.

Connector	Configuration
RYE MAB-5*	5 Pin
SWITCHCRAFT 61GA5F*	5 Pin
SWITCHCRAFT 61HA5F	5 Pin
RYE MAB-6*	6 Pin
SWITCHCRAFT 61HA6F	6 Pin

*Suitable for non-locking connector only.

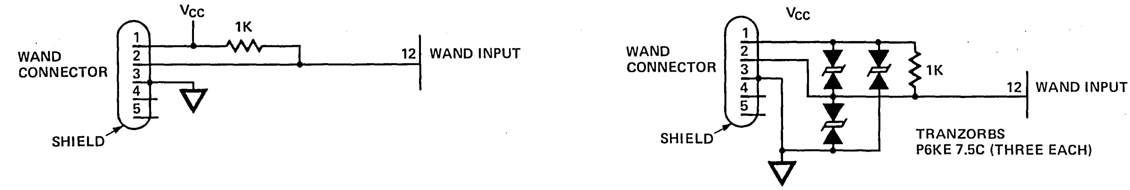


NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).

PIN	WIRE COLOR	FUNCTION
1	RED	V_S SUPPLY VOLTAGE
2	WHITE	V_O OUTPUT
3	BLACK	GROUND
4	N/A	N/C
5	N/A	N/C
CASE	-	SHIELD (MUST BE CONNECTED)

Figure 7. Connector Specifications

Wand I/O Interfaces



MINIMAL **RECOMMENDED**

Note:
The shield must be connected to ground for proper wand operation.

Figure 8. Wand Interfaces

Reader Selection Guide

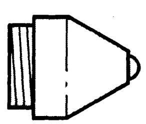
The following table will help in selecting the proper Component Bar Code Reader part number for a given application. To use the table, first determine the minimum size of the narrow elements in the bar codes to be read. Next, determine the type of environment in which the reader's wand will be used. Finally, determine whether a switched wand is required for the application.

Type of Bar Code	Type of Environment	
	Commercial or Light Industrial	Heavy Industrial
High, Medium or Low Resolution (7.5 mil or Larger)	HBCR-1000 (Non-Switched) HBCR-1022 (Switched)	HBCR-1043 (Non-Switched)
Very High Resolution (Less than 7.5 mil)	HBCR-1025 (Non-Switched) HBCR-1024 (Switched)	HBCR-1045 (Non-Switched)
Security (Black-on-Black) Bar Code	HBCR-1025 (Non-Switched) HBCR-1024 (Switched)	HBCR-1045 (Non-Switched)
Colored (UPC/EAN/JAN) Bar Code	HBCR-1000 (Non-Switched) HBCR-1022 (Switched)	HBCR-1043 (Non-Switched)

Maintenance Considerations

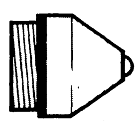
There are no user serviceable parts inside the wands. The tip is designed to be easily replaceable, and if damaged should be replaced. The table below will help determine the correct replacement tip part number. Before attempting to replace the wand tip, be sure that the wand is disconnected from any power source.

The wands or decoder IC are also available as replacement parts. Should either become damaged, the correct replacement part numbers can be determined from the table below.These parts can be ordered from any Hewlett-Packard authorized distributor.



HBCS-2999

Figure 9a. Sapphire Tip



HBCS-4999

Figure 9b. Sapphire Tip

Reader Part No.	Replacement Part Numbers		
	Wand	Wand Tip	Decoder IC
HBCR-1000	HBCS-2300	HBCS-2999	HBCR-1900
HBCR-1022	HBCS-2200	HBCS-2999	HBCR-1900
HBCR-1024	HBCS-2400	HBCS-2999	HBCR-1900
HBCR-1025	HBCS-2500	HBCS-2999	HBCR-1900
HBCR-1043	HBCS-4300	HBCS-4999	HBCR-1900
HBCR-1045	HBCS-4500	HBCS-4999	HBCR-1900

HEWLETT PACKARD

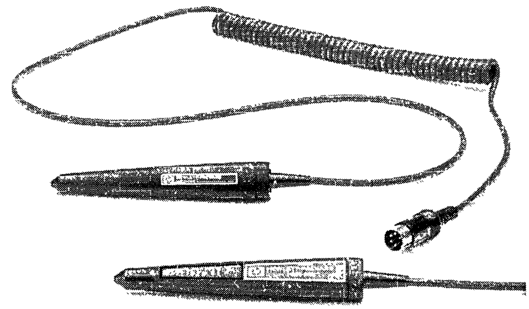
SAPPHIRE TIP DIGITAL BAR CODE WANDS

HBCS-2200
HBCS-2300
HBCS-2400
HBCS-2500

TECHNICAL DATA JANUARY 1986

Features

- **SCAN ANGLE 0 TO 45 DEGREES**
- **OPERATING TEMPERATURE −20° C TO +65° C**
- **AVAILABLE IN EITHER 0.19 mm (0.0075 IN.) OR 0.13 0.13 mm (0.005 IN.) RESOLUTION**
- **SEALED REPLACEABLE SAPPHIRE TIP**
  Provides Protection from Contamination Due to Dirt and Debris
- **DIGITAL OUTPUT**
  Open Collector Output Compatible with TTL and CMOS
- **DECODABILITY SPECIFIED FOR GUARANTEED PERFORMANCE**
- **SINGLE 5 VOLT SUPPLY**
- **PUSH-TO-READ SWITCH (HBCS-2200/2400)**
  Minimizes Power Consumption in Battery Operated Systems
- **SOLID STATE RELIABILITY**
- **POLYCARBONATE CASE**
  Durable, yet Lightweight



Description

Hewlett-Packard's Sapphire Tip Digital Bar Code Wands are hand-held scanners optimized to provide excellent reading of all common bar code formats. These wands contain an optical sensor with a 700 nm visible red LED (HBCS-2200/2300) or an 820 nm infrared LED (HBCS-2400/2500); a photo IC detector; and precision aspheric optics. The internal signal conditioning circuitry converts the optical information into a logic level pulse width representation of the bars and spaces.

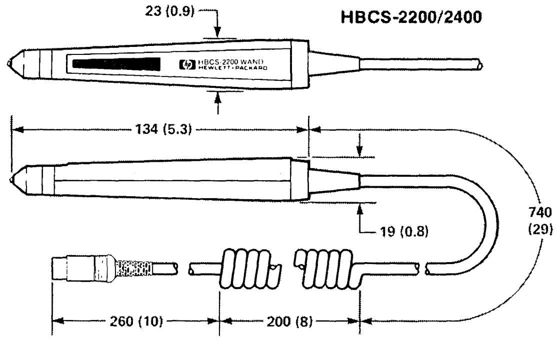
The HBCS-2200/2300 wands, with their nominal 0.19 mm spot size, are excellent choices for reading a general range of bar codes. The HBCS-2400/2500 wands have a nominal spot size of 0.13 mm and are ideal for reading very high density bar code.

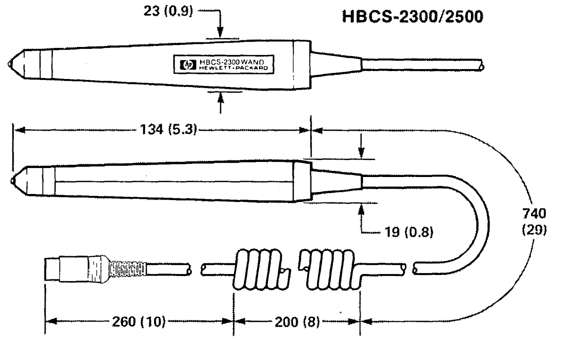
All of the wands feature an internal shield for maximizing immunity to electromagnetic interference (EMI), electrostatic discharge (ESD), and ground loops. The shield is also designed to eliminate noise from capacitively coupled inputs.

The HBCS-2200 and HBCS-2400, with their push-to-read switch, are recommended for use in battery powered applications requiring low power consumption. The HBCS-2300 and HBCS-2500 (without switch) are the usual choices for AC powered systems.

The standard wand configuration includes a strain relieved coiled cord, which has a comfortable extended length of 190 cm (75 in.). Maximum length is 250 cm (100 in.). The standard connector is a 5 pin, 240 degree DIN connector.

Wand Dimensions





NOTE: DIMENSIONS IN MILLIMETRES AND (INCHES).

Applications

The digital bar code wand is a highly effective alternative to keyboard data entry. Bar code scanning is faster and more accurate than key entry and provides far greater throughput. In addition, bar code scanning typically has a higher first read rate and greater data accuracy than optical character recognition. When compared to magnetic stripe encoding, bar code offers significant advantages in flexibility of media, symbol placement and immunity to electromagnetic fields.

Hewlett-Packard's sapphire tip wands are designed for use in applications where dirt and debris are a common occurrence and could cause clogging in a conventional open-tip wand. In addition, the sapphire ball provides superior wear resistance and improves scanning ease. The rugged yet lightweight polycarbonate case makes these wands ideal for use in commercial or light industrial applications.

Applications include remote data collection, work-in-process tracking, point-of-sale data entry, inventory control, library circulation control, medical records tracking, and repair/service work.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Nominal Narrow Element Width HBCS-2200/2300		0.19 (0.0075)		mm (in.)	
HBCS-2400/2500		0.13 (0.005)		mm (in.)	
Scan Velocity	V_{SCAN}	7.6 (3)	127 (50)	cm/sec (in/sec)	
Contrast	R_W-R_B	45		%	1
Supply Voltage	V_S	4.5	5.5	Volts	2
Temperature	T_A	−20	+65	°C	
Tilt Angle	(See Figure 8)				3
Orientation	(See Figure 1)				

Notes:
1. Contrast is defined as R_W-R_B, where R_W is the reflectance of the white spaces and R_B is the reflectance of the black bars, measured at the emitter wavelength (700 nm or 820 nm). Contrast is related to print contrast signal (PCS) by PCS = (R_W-R_B)/R_W or R_W-R_B = PCS*R_W.
2. Power supply ripple and noise should be less than 100 mV peak to peak.
3. Performance in sunlight will vary depending on shading at wand tip.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	−40	+75	°C	
Operating Temperature	T_A	−20	+65	°C	
Supply Voltage HBCS-2200/2300	V_S	−0.5	+6.00	V	
HBCS-2400/2500	V_S	−0.5	+5.75	V	
Output Transistor Power	P_T		200	mW	
Output Collector Voltage	V_O	−0.5	+20	V	

Electrical Operation

The HBCS-2XXX family of digital bar code wands consists of a precision optical sensor, an analog amplifier, a digitizing circuit, and an output transistor. These elements provide a TTL compatible output from a single 4.5V to 5.5V power supply. The open collector transistor requires an external pull-up resistor for proper operation.

A non-reflecting black bar results in a logic high (1) level output, while a reflecting white space will cause a logic low (0) level output. The initial or "wake-up" state will be indeterminate. However, after a short period (typically less than 1 second), the wand will assume a logic low state if no bar code is scanned. This feature insures that the first bar will not be missed in a normal scan.

The wands provide a case, cable, and connector shield which must be terminated to logic ground or, preferably, to both logic ground and earth ground. The shield is connected to the metal housing of the 5 pin DIN connector.

Grounding the shield will provide a substantial improvement in EMI/ESD immunity in AC powered systems. However, it is essential that the shield be properly terminated even when EMI and ESD are not a concern, otherwise the shield will act as an antenna, injecting electrical noise into the wand circuitry.

The HBCS-2200/2400 wands incorporate a push-to-read switch which is used to energize the LED emitter and electronic circuitry. When the switch is initially depressed, contact bounce may cause a series of random pulses to appear at the output (V_O). This pulse train will typically settle to a final value within 5 ms.

The recommended logic interface for the wands is shown in Figure 9. This interconnection provides the maximum ESD protection for both the wand and the user's electronics.

Electrical Characteristics

(V_S = 4.5V to 5.5V, T_A = 25° C, R_L = 1KΩ to 10KΩ, unless otherwise noted)

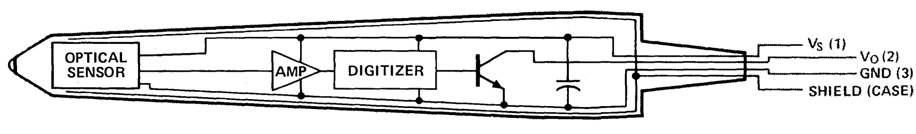
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Notes
Supply Current	I_S		42	50	mA	V_S = 5.0V	4
High Level Output Current	I_{OH}			400	μA	V_{OH} = 2.4V	
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA	
Output Rise Time	t_r		3.4	20	μs	10%-90% Transition R_L = 1K	
Output Fall Time	t_f		1.2	20	μs		
Switch Bounce HBCS-2200/2400	t_{sb}		0.5	5.0	ms		5
Electrostatic Discharge Immunity	ESD		25		kV		6

Notes:

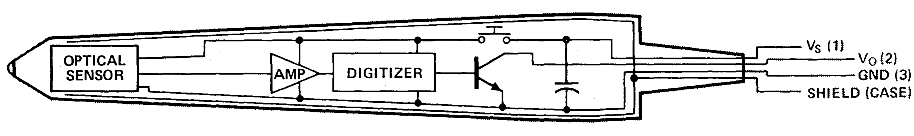
4. Push-to-read switch (if applicable) is depressed.
5. Switch bounce causes a series of sub-millisecond pulses to appear at the output (V_O).
6. Shield must be properly terminated (see Figure 9). The human body is modeled by discharging a 300 pF capacitor through a 500 Ω resistor. No damage to the wand will occur at the specified discharge level.

Block Diagram

HBCS-2300/2500 (without Switch)



HBCS-2200/2400 (with Switch)



Scanning Performance

(V_S = 5.0 V, R_L = 1.0 to 10 KΩ, T_A = 25° C, Scan Velocity = 50 cm/sec)

Parameter	Symbol	HBCS-	Typ.	Max.	Units	Condition	Fig.	Note
Decodability Index	DI	2200/2300	9	22	%		1,2,3 4,7,9	7,8
		2400/2500	12	22	%			
Average Width Error (Narrow Bars)	OS_{bn}	2200/2300	0.005 (0.0002)		mm (in.)		1,2,9	7
		2400/2500	0.024 (0.0009)		mm (in.)	Tilt Angle 0° to 40° Preferred Orientation Standard Test Tag		
Average Width Error (Wide Bars)	OS_{bw}	2200/2300	0.003 (0.0001)		mm (in.)			
		2400/2500	0.023 (0.009)		mm (in.)			
Average Width Error (Narrow Spaces)	OS_{sn}	2200/2300	−0.011 (−0.0004)		mm (in.)			
		2400/2500	−0.027 (−0.0106)		mm (in.)			
Average Width Error (Wide Spaces)	OS_{sw}	2200/2300	−0.002 (−0.0001)		mm (in.)			
		2400/2500	−0.026 (−0.0010)		mm (in.)			
Deviation from Average (Internal)	d_e	2200/2300	0.018 (0.0007)	0.048 (0.0019)	mm (in.)		1,2,5 6,9	7
		2400/2500	0.019 (0.0007)	0.052 (0.0020)	mm (in.)			
Deviation from Average (First Bar)	d_{b1}	2200/2300	0.090 (0.0035)	0.152 (0.0060)	mm (in.)			
		2400/2500	0.060 (0.0024)	0.100 (0.0039)	mm (in.)			

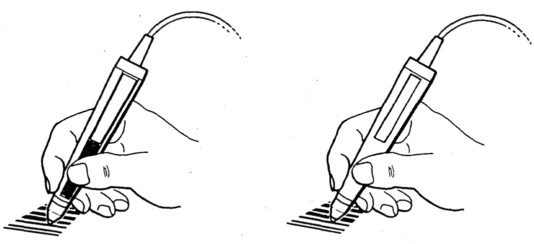
Notes:

7. The test tag for the HBCS-2200/2300 Wands (Figure 2a) consists of black bars and white spaces with a narrow element width of 0.19 mm (0.0075 in.) and a wide element width of 0.42 mm (0.0165 in.). This equates to a wide-to-narrow ratio of 2.2:1. A margin, or white reflecting area, of at least 5 mm in width precedes the first bar.

   The test tag for the HBCS-2400/2500 wands (Figure 2b) consists of black bars with a narrow element width of 0.13 mm (0.005 in.) and wide element width of 0.43 mm (0.017 in.) giving a ratio of 3.4:1. The white spaces have a narrow element width of 0.28 mm (0.011 in.) and wide element width of 0.64 mm (0.025 in.) yielding a ratio of 2.3:1. Both tags are photographically reproduced on diffuse reflecting paper with a PCS greater than 90%.

8. Decodability index is a measure of the errors produced by the wand when scanning a standard test symbol at a constant velocity. It is expressed as a percentage of the narrow element width.

   For a more detailed discussion of the terms used here, see Hewlett-Packard Application Note 1013 "Elements of a Bar Code System" (publication number 5953-9387).



HBCS-22/2400 **HBCS-23/2500**

Figure 1. Preferred Wand Orientation

a. HBCS-22/2300 Test Tag **b. HCBS-24/2500 Test Tag**

Figure 2. Standard Test Tag Formats (Test Tags Enlarged to Show Detail)

Typical Performance Curves

(VS = 5 V, RL = 1 KΩ, TA = 25° C, Tilt = 15°, VSCAN = 50 cm/sec unless otherwise specified)

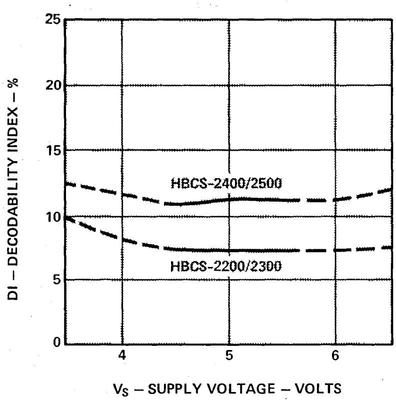


Figure 3. Decodability Index vs. Supply Voltage.

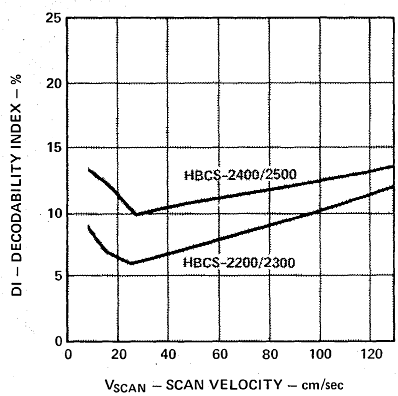


Figure 4. Decodability Index vs. Scan Velocity.

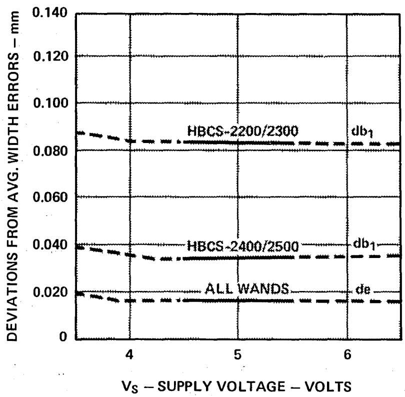


Figure 5. Deviation from Average Width Error vs. Supply Voltage.

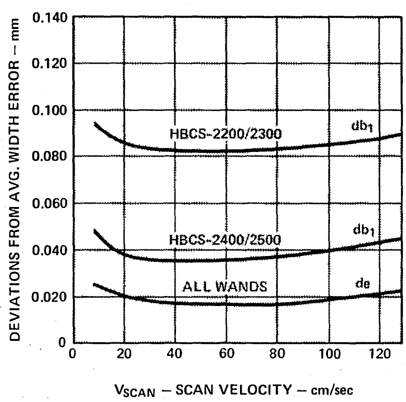


Figure 6. Deviation from Average Width Error vs. Scan Velocity.

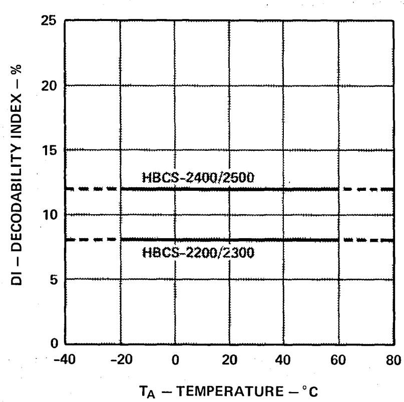


Figure 7. Decodability Index vs. Temperature.

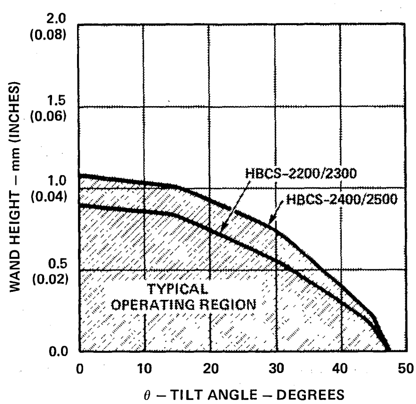
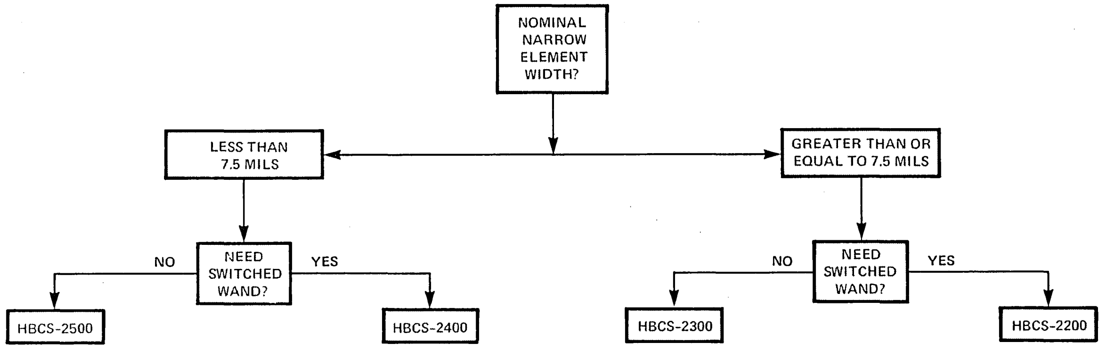


Figure 8. Wand Height vs. Tilt Angle.

Selection Guide



NOTES:
IF IT IS NECESSARY TO READ BAR CODE PRINTED IN COLORS OTHER THAN BLACK AND WHITE IT IS RECOMMENDED THAT EITHER THE HBCS-2200 OR HBCS-2300 WANDS BE SELECTED.
IF IT IS NECESSARY TO READ SECURITY "BLACK-ON-BLACK" BAR CODE (CARBON-BASED BLACK AND WHITE BAR CODE WITH A BLACK OVERLAY), IT IS RECOMMENDED THAT EITHER THE HBCS-2400 OR THE HBCS-2500 WANDS BE SELECTED.

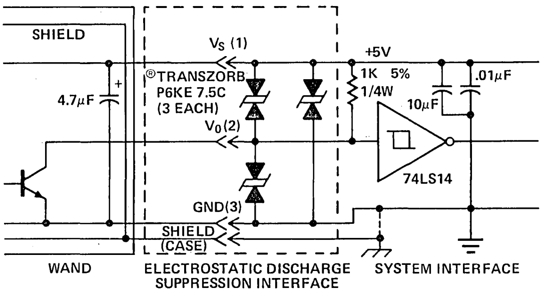


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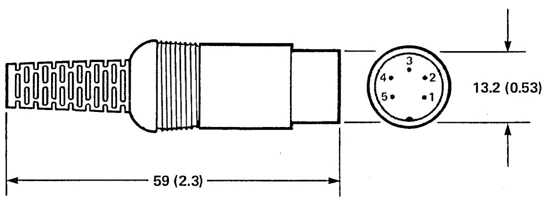
Figure 9. Recommended Logic Interface (When earth ground is not available, connect shield to logic ground, as shown by dotted line).



NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).

PIN	WIRE COLOR	FUNCTION
1	RED	V_S SUPPLY VOLTAGE
2	WHITE	V_O OUTPUT
3	BLACK	GROUND
4	N/A	N/C
5	N/A	N/C
CASE	-	SHIELD (MUST BE CONNECTED)

Figure 10. Connector Specifications.

Mechanical Considerations

The wands include a standard 5 pin, 240° DIN connector. The detailed specifications and pin-outs are shown in Figure 10. Mating connectors are available from RYE Industries and SWITCHCRAFT in both 5 pin and 6 pin configurations. These connecors are listed below.

Connector	Configuration
RYE MAB-5	5 Pin
SWITCHCRAFT 61GA5F	5 Pin
SWITCHCRAFT 61HA5F	5 Pin
RYE MAB-6	6 Pin
SWITCHCRAFT 61GA6F	6 Pin

Maintenance Considerations

There are no user serviceable parts inside the wand. The tip is designed to be easily replaceable, and if damaged it should be replaced. Before unscrewing the tip, disconnect the wand from the system power source. The part number for the wand tip is HBCS-2999. The tip can be ordered from any Hewlett-Packard franchised distributor.

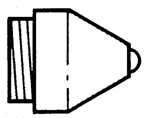


Figure 11. Sapphire Tip.

Optional Features

For options such as special cords, connectors or labels, contact your nearest Hewlett-Packard sales office or franchised Hewlett-Packard distributor.

HEWLETT PACKARD

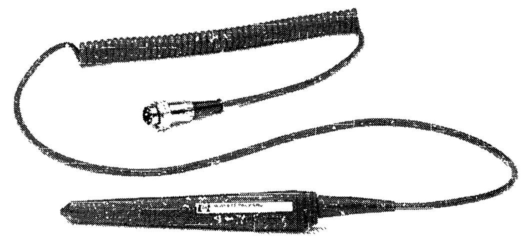
INDUSTRIAL DIGITAL BAR CODE WANDS

HBCS-4300
HBCS-4500

TECHNICAL DATA JANUARY 1986

Features

- **SEALED METAL CASE FOR HEAVY INDUSTRIAL ENVIRONMENTS AND LOGMARS APPLICATIONS**
- **SCAN ANGLE 0 TO 45 DEGREES**
- **OPERATING TEMPERATURE −20° C TO +65° C**
- **AVAILABLE IN EITHER 0.19 mm (0.0075 IN.) OR 0.13 mm (0.005 IN.) RESOLUTION**
- **SEALED REPLACEABLE SAPPHIRE TIP**
  Provides Protection from Contamination Due to Dirt and Debris
- **DIGITAL OUTPUT**
  Open Collector Output Compatible with TTL and CMOS
- **DECODABILITY SPECIFIED FOR GUARANTEED PERFORMANCE**
- **SINGLE 5 VOLT SUPPLY**
- **SOLID STATE RELIABILITY**



Description

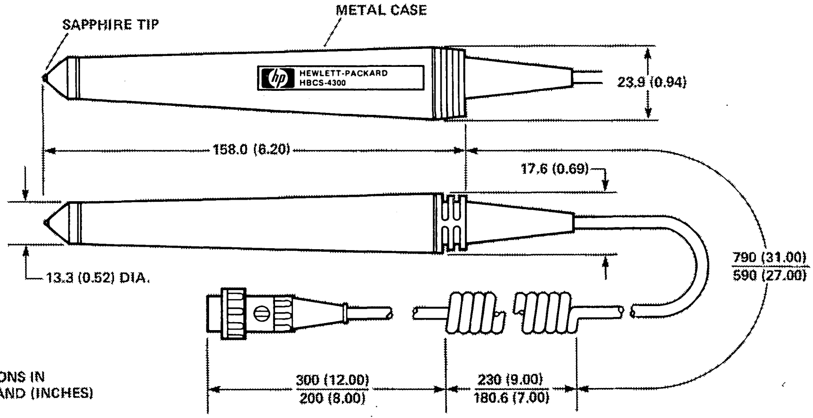
Hewlett-Packard's Industrial Digital Bar Code Wands are hand-held scanners optimized to provide excellent reading of all common bar code formats. These wands contain an optical sensor with a 700 nm visible red LED (HBCS-4300) or an 820 nm infrared LED (HBCS-4500); a photodetector IC; and precision aspheric optics. The internal signal conditioning circuitry converts the optical information into a logic level pulse width representation of the bars and spaces.

The HBCS-4300 wand, with its nominal 0.19 mm spot size, is an excellent choice for reading a general range of bar codes. The HBCS-4500 wand has a nominal spot size of 0.13 mm and is ideal for reading very high density bar code.

Both wands feature an integral shield for maximizing immunity to electromagnetic interference (EMI), electrostatic discharge (ESD), and ground loops. The shield is also designed to eliminate noise from capacitively coupled inputs.

The standard configuration includes a strain relieved coiled cord, which has a comfortable extended length of 190 cm (75 in.) [maximum length is 250 cm (100 in.)]. The standard connector is a 5 pin, 240 degree, metal, locking DIN connector.

Wand Dimensions



DIMENSIONS IN MILLIMETRES AND (INCHES)

Applications

The digital bar code wand is a highly effective alternative to keyboard data entry. Bar code scanning is faster and more accurate than key entry and provides far greater throughput. In addition, bar code scanning typically has a higher first read rate and greater data accuracy than optical character recognition. When compared to magnetic stripe encoding, bar code offers significant advantages in flexibility of media, symbol placement and immunity to electromagnetic fields.

Hewlett-Packard's industrial bar code wands are designed for use in applications which require the added ruggedness and durability that a metal wand can provide. In addition, the sapphire ball provides superior wear resistance and improves scanning ease. The rugged yet lightweight aluminum case makes these wands ideal for use in heavy industrial and LOGMARS applications such as: shop floor data collection, work-in process tracking, material tracking, and repair/service work.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Nominal Narrow Element Width HBCS-4300		0.19 (0.0075)		mm (in.)	
HBCS-4500		0.13 (0.005)		mm (in.)	
Scan Velocity	V_{SCAN}	7.6 (3)	127 (50)	cm/sec (in/sec)	
Contrast	R_W-R_B	45		%	1
Supply Voltage	V_S	4.5	5.5	Volts	2
Temperature	T_A	−20	+65	°C	
Tilt Angle	(See Figure 8)				3
Orientation	(See Figure 1)				

Notes:

1. Contrast is defined as R_W-R_B where R_W is the reflectance of the white spaces and R_B is the reflectance of the black bars, measured at the emitter wavelength (700 nm or 820 nm). Contrast is related to print contrast signal (PCS) by PCS = (R_W-R_B)/R_W or R_W-R_B = PCS*R_W.
2. Power supply ripple and noise should be less than 100 mV peak to peak.
3. Performance in direct sunlight will vary depending on shading at the wand tip.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	−40	+75	°C	
Operating Temperature	T_A	−20	+65	°C	
Supply Voltage HBCS-4300	V_S	−0.5	+6.00	V	
HBCS-4500	V_S	−0.5	+5.75	V	
Output Transistor Power	P_T		200	mW	
Output Collector Voltage	V_O	−0.5	+20	V	

Electrical Operation

The HBCS-4XXX family of digital bar code wands consists of a precision optical sensor, an analog amplifier, a digitizing circuit, and an output transistor. These elements provide a TTL compatible output from a single 4.5V to 5.5V power supply. The open collector transistor requires a pull-up resistor for proper operation.

A non-reflecting black bar results in a logic high (1) level output, while a reflecting white space will cause a logic low (0) level output. The initial or "wake-up" state will be indeterminate. However, after a short period (typically less than 1 second), the wand will assume a logic low state if no bar code is scanned. This feature insures that the first bar will not be missed in a normal scan.

The wands provide a case, cable, and connector shield which must be terminated to logic ground or, preferably, to both logic ground and earth ground. The shield is connected to the metal housing of the 5 pin DIN connector.

The shield must be properly terminated otherwise it will act as an antenna, injecting electrical noise into the wand circuitry. Grounding the shield will also provide a substantial improvement in EMI/ESD immunity.

The recommended logic interface for the wands is shown in Figure 9. This interconnection provides the maximum ESD protection for both the wand and the user's electronics.

Electrical Characteristics

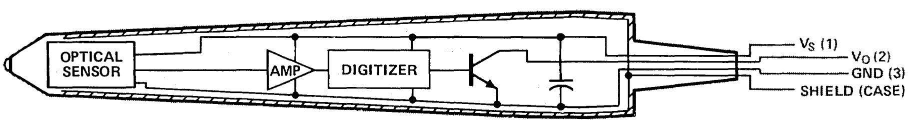
(V_S = 4.5V to 5.5V, T_A = 25° C, R_L = 1KΩ to 10KΩ, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Notes
Supply Current	I_S		42	50	mA	V_S = 5.0V	
High Level Output Current	I_{OH}			400	μA	V_{OH} = 2.4V	
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA	
Output Rise Time	t_r		3.4	20	μs	10%-90% Transition R_L = 1K	
Output Fall Time	t_f		1.2	20	μs		
Electrostatic Discharge Immunity	ESD		25		kV		4

Notes:

4. Shield must be properly terminated (see Figure 3). The human body is modeled by discharging a 300 pF capacitor through a 500 Ω resistor. No damage to the wand will occur at the specified discharge level.

Block Diagram



Scanning Performance

(V_S = 5.0 V, R_L = 1.0 to 10 KΩ, T_A = 25° C, Scan Velocity = 50 cm/sec).

Parameter	Symbol	HBCS-	Typ.	Max.	Units	Condition	Fig.	Note
Decodability Index	DI	4300	9	22	%	Tilt Angle 0° to 40° Preferred Orientation Standard Test Tag	1,2,3	5,6
		4500	12	22	%		4,5,8	
Average Width Error (Narrow Bars)	OS_{bn}	4500	0.005 (0.0002)		mm (in.)		1,2,3	5
		4500	0.024 (0.0009)		mm (in.)			
Average Width Error (Wide Bars)	OS_{bw}	4300	0.003 (0.0001)		mm (in.)			
		4500	0.023 (0.0009)		mm (in.)			
Average Width Error (Narrow Spaces)	OS_{sn}	4300	−0.011 (−0.0004)		mm (in.)			
		4500	−0.027 (−0.0106)		mm (in.)			
Average Width Error (Wide Spaces)	OS_{sw}	4300	−0.002 (−0.0001)		mm (in.)			
		4500	−0.026 (−0.0010)		mm (in.)			
Deviation from Average (Internal)	d_e	4300	0.018 (0.0007)	0.048 (0.0019)	mm (in.)		1,2,3 6,7	5
		4500	0.019 (0.0007)	0.052 (0.0020)	mm (in.)			
Deviation from Average (First Bar)	d_{b1}	4300	0.090 (0.0035)	0.152 (0.0060)	mm (in.)			
		4500	0.060 (0.0024)	0.100 (0.0039)	mm (in.)			

Notes:

5. The test tag for the HBCS-4300 Wands (Figure 2a) consists of black bars and white spaces with a narrow element width of 0.19 mm (0.0075 in.) and a wide element width of 0.42 mm (0.0165 in.). This equates to a wide-to-narrow ratio of 2.2:1. A margin, or white reflecting area, of at least 5 mm in width precedes the first bar.

   The test tag for the HBCS-4500 wands (Figure 2b) consists of black bars with a narrow element width of 0.13 mm (0.005 in.) and wide element width of 0.43 mm (0.017 in.) giving a ratio of 3.4:1. The white spaces have a narrow element width of 0.28 mm (0.011 in.) and wide element width of 0.64 mm (0.025 in.) yielding a ratio of 2.3:1. Both tags are photographically reproduced on diffuse reflecting paper with a PCS greater than 90%.

6. Decodability index is a measure of the errors produced by the wand when scanning a standard test symbol at a constant velocity. It is expressed as a percentage of the narrow element width.

   For a more detailed discussion of the terms used here, see Hewlett-Packard Application Note 1013, "Elements of a Bar Code System" (publication number 5953-9387).

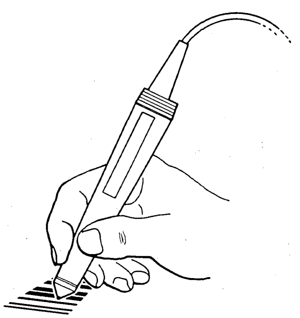


Figure 1. Preferred Wand Orientation

a. HBCS-4300 Test Tag **b. HBCS-4500 Test Tag**

Figure 2. Standard Test Tag Formats (Test Tags enlarged to show detail)

Typical Performance Curves

(Vs = 5.0 V, RL = 1.0 to 10 KΩ, TA = 25° C, Tilt = 15° C, VSCAN = 50 cm/sec, unless otherwise specified).

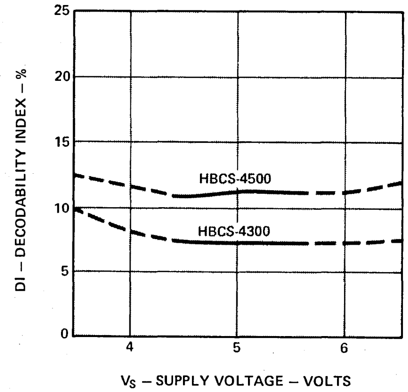


Figure 3. Decodability Index vs. Supply Voltage

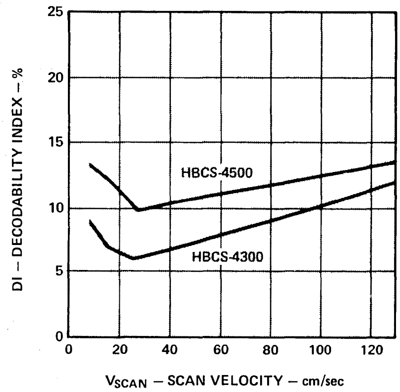


Figure 4. Decodability Index vs. Scan Velocity

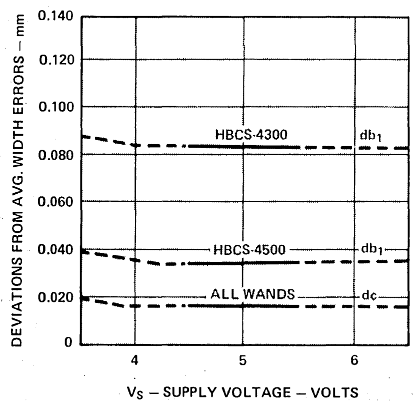


Figure 5. Deviation from Average Width Error vs. Supply Voltage

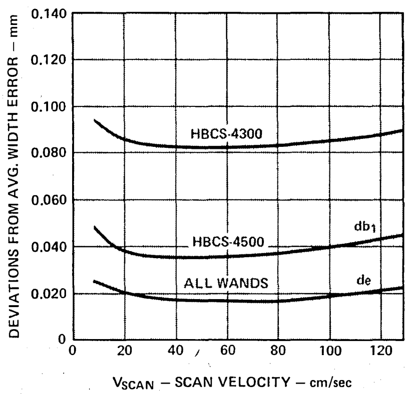


Figure 6. Deviation from Average Width Error vs. Scan Velocity

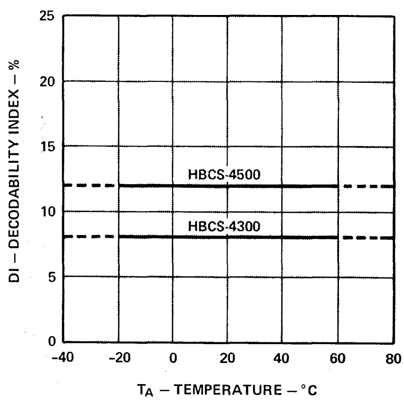


Figure 7. Decodability Index vs. Temperature

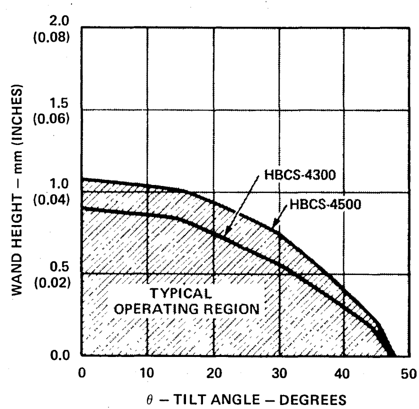
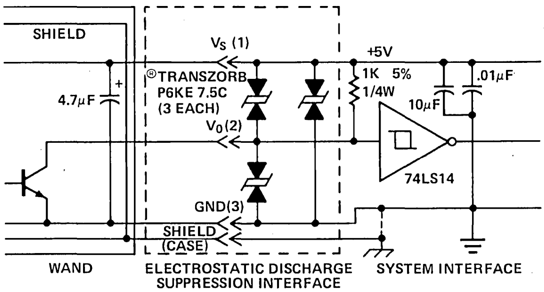
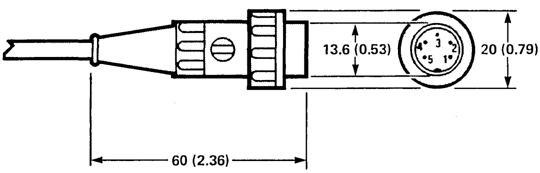


Figure 8. Wand Height vs. Tilt Angle



®TRANSZORB IS A REGISTERED TRADEMARK OF GENERAL SEMICONDUCTOR INDUSTRIES, TEMPE AZ.

Figure 9. Recommended Logic Interface (When earth ground is not available, connect shield to logic ground, as shown by dotted line).



NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).

PIN	WIRE COLOR	FUNCTION
1	RED	V_S SUPPLY VOLTAGE
2	WHITE	V_O OUTPUT
3	BLACK	GROUND
4	N/A	N/C
5	N/A	N/C
CASE	-	SHIELD (MUST BE CONNECTED)

Figure 10. Connector Specifications.

Mechanical Considerations

The wands include a standard 5 pin, 240°, metal, locking DIN connector. The detailed specifications and pin-outs are shown in Figure 10. Mating connectors are available from SWITCHCRAFT in both 5 pin and 6 pin configurations. These connectors are listed below.

Connector	Configuration
SWITCHCRAFT 61HA5F	5 Pin
SWITCHCRAFT 13EL5F	5 Pin
SWITCHCRAFT 61HA6F	6 Pin

Maintenance Considerations

There are no user serviceable parts inside the wand. The tip is designed to be easily replaceable, and if damaged it should be replaced. Before unscrewing the tip, disconnect the wand from the system power source. The part number for the wand tip is HBCS-4999. The tip can be ordered from any Hewlett-Packard authorized distributor.

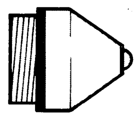


Figure 11. Sapphire Tip.

Optional Features

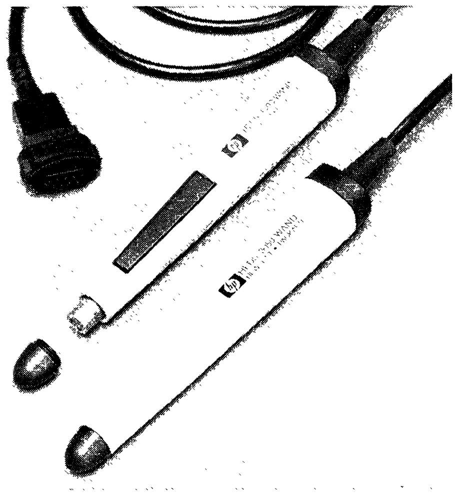
For options such as special cords, connectors or labels, contact your nearest Hewlett-Packard sales office or authorized Hewlett-Packard distributor.

![HP logo] HEWLETT PACKARD

DIGITAL BAR CODE WAND

HEDS-3000
HEDS-3050

TECHNICAL DATA JANUARY 1986



Features

- **0.3 mm RESOLUTION**
  Enhances the Readability of dot matrix printed bar codes
- **DIGITAL OUTPUT**
  Open Collector Output Compatible with TTL and CMOS
- **PUSH-TO-READ SWITCH (HEDS-3000)**
  Minimizes Power in Battery Operated Systems
- **SINGLE 5V SUPPLY OPERATION**
- **ATTRACTIVE, HUMAN ENGINEERED CASE**
- **DURABLE LOW FRICTION TIP**
- **SOLID STATE RELIABILITY**
  Uses LED and IC Technology
- **SHIELDED CASE AND CABLE (HEDS-3050)**
  Maximizes EMI/ESD Immunity in AC Powered Systems

Description

The HEDS-3000 and HEDS-3050 Digital Bar Code Wands are hand held scanners designed to read all common bar code formats that have the narrowest bars printed with a nominal width of 0.3 mm (0.012 in.). The wands contain an optical sensor with a 700 nm visible light source, photo IC detector, and precision aspheric optics. Internal signal conditioning circuitry converts the optical information into a logic level pulse width representation of the bars and spaces.

The HEDS-3000 comes equipped with a push-to-read switch which is used to activate the electronics in battery powered applications requiring lowest power consumption. The HEDS-3050 does not have a switch, and features internal metal shielding that maximizes immunity to electromagnetic interference, electrostatic discharge, and ground loops in AC powered systems. Both wands feature a strain relieved 104 cm (41 in.) cord with a nine-pin subminiature D-style connector.

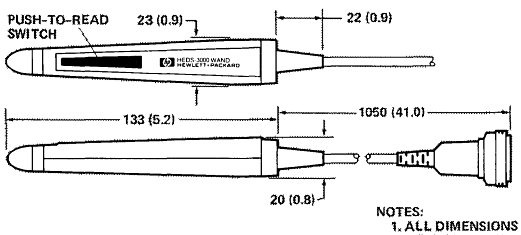
Applications

The Digital Bar Code Wand is an effective alternative to the keyboard when used to collect information in self-contained blocks. Bar code scanning is faster than key entry and also more accurate since most codes have check-sums built-in to prevent incorrect reads from being entered.

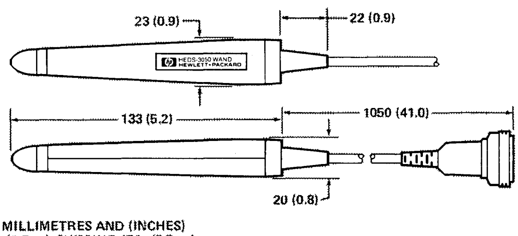
Applications include remote data collection, ticket identification systems, security checkpoint verification, file folder tracking, inventory control, identifying assemblies in service, repair, and manufacturing environments, and programming appliances, intelligent instruments and personal computers.

Wand Dimensions

HEDS-3000



HEDS-3050



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES)
2. WEIGHT: NET 46.5g (1.5oz.) SHIPPING 171g (5.5oz.)

Electrical Operation

The HEDS-3000 and HEDS-3050 consist of a precision optical sensor, an analog amplifier, a digitizing circuit, and an output transistor. These elements provide a TTL compatible output from a single voltage supply range of 3.6V to 5.75V. A non-reflecting black bar results in a logic high (1) level, while a reflecting white space will cause a logic low (0) at the V_O connection (pin 2). The output of the wands is an open collector transistor.

The HEDS-3050 provides a case and cable shield (pin 5) which must be connected to logic ground and preferably also to earth ground. This will provide a substantial improvement in EMI/ESD immunity for the wand in AC powered systems.

The recommended logic interface for the wands is shown in Figure 3. This interconnection provides maximum ESD protection for both the wand and the user's electronics.

The HEDS-3000 incorporates a push-to-read switch which is used to energize the 700nm LED emitter and electronic circuitry. When the switch is initially depressed, its contact bounce may cause a series of random pulses to appear at the output, V_O. This pulse train will typically settle to a final value within 0.5 ms. This initial pulse train is eliminated when a switchless HEDS-3050 is used.

BAR CODE COMPONENTS

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Bar Width	s, b	0.3		mm
Scan Velocity	V_{scan}	7.6	76	cm/s
Contrast	PCS	70		%
Supply Voltage	V_S	3.6	5.75	V
Temperature	T_A	0	55	°C
Orientation	See Figure 1			

Absolute Maximum Ratings

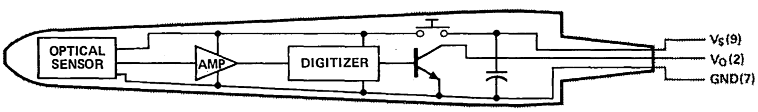
Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-20	55	°C	1
Operating Temperature	T_A	0	55	°C	
Supply Voltage	V_S	-0.5	6.0	V	2
Output Transistor Power	P_T		200	mW	
Output Collector Voltage	V_O		20	V	

Electrical Characteristics (V_S = 3.6V to 5.75V at T_A = 25°C, R_L = 2.2kΩ, unless otherwise noted)

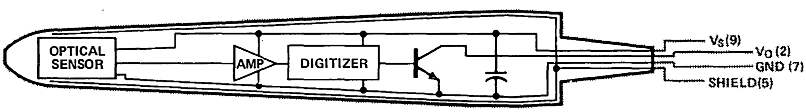
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Switch Bounce (HEDS-3000)	t_{sb}		0.5	5	ms			3
High Level Output Current	I_{OH}			400	μA	V_{OH} = 2.4V, Bar Condition (Black)	3	
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 16mA, Space Condition (White)	3	
Output Rise Time	t_r		2		μs	10%-90% Transition	3	
Output Fall Time	t_f		100		ns	90%-10% Transition	3	
Supply Current	I_S		42	50	mA	V_S = 5V, Bar Condition (Black)		2,4

Block Diagram

HEDS-3000 (WITH SWITCH)



HEDS-3050 (SHIELDED)



GUARANTEED WIDTH ERROR PERFORMANCE

(V_S = 5V, T_A = 0°C to 55°C, R_L = 2.2kΩ, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions		Fig.	Notes
Bar Width Error	1st	Δb_1		0.08 (3.2)	0.13 (5.2)	mm (in.x10^{-3})	T_A=25°C	Margin ≥ 5mm Height = 0.25mm Tilt = 0° v_{scan} = 50 cm/s Standard Test Tag Preferred Orientation b=s=0.3mm (0.012 in.) 2b=2s=0.6mm (0.024 in.)	1 2,6 11	5 7,8 9,10 11
				0.10 (3.8)	0.15 (5.7)		T_A = 0° to 55°C			
	Interior	Δb	-0.04 (-1.4)	0.05 (1.8)	0.10 (3.9)	mm (in.x10^{-3})	T_A=25°C		1,2 6,11	6,7 8,9 10,11
			-0.05 (-2.0)	0.05 (2.0)	0.11 (4.3)		T_A = 0° to 55°C			
Space Width Error	Interior	Δs	0.04 (1.4)	-0.05 (-1.8)	-0.10 (-3.9)	mm (in.x10^{-3})	T_A=25°C		1,2 6,11	6,7 8,10 11
			0.05 (2.0)	-0.05 (-2.0)	-0.11 (-4.3)		T_A = 0° to 55°C			
Tag Scan Velocity		v_{scan}	7.6		76	cm/s			9	7
Emitter Peak Wavelength		λ		700		nm	T_A=25°C			

TYPICAL WIDTH ERROR PERFORMANCE

(V_S = 5V, T_A = 25°C, R_L = 2.2kΩ, unless otherwise noted)

Parameter	From	To	Symbol	Typical WE Tilt = 0° Height = 0.25mm	Typical WE Tilt = 30° Height = 0.0mm	Units	Conditions	Fig.	Notes
Bar Width Error	Margin	1st	Δb_1	0.08 (3.2)	0.11 (4.2)	mm (in.x10^{-3})	Margin ≥ 5mm 1b=1s=0.3mm 2b=2s=0.6mm T_A=25°C V_S=5V v_{scan}=50cm/s Preferred Orientation Standard Test Tag	1,2	5,7,8
	1s	1b	Δb_{1-1}	0.03 (1.2)	0.04 (1.6)	mm (in.x10^{-3})		1,2	6,7,8
	2s	1b	Δb_{2-1}	0.06 (2.5)	0.07 (2.9)	mm (in.x10^{-3})		1,2	6,7,8
	1s	2b	Δb_{1-2}	0.02 (0.9)	0.02 (0.7)	mm (in.x10^{-3})		1,2	6,7,8
	2s	2b	Δb_{2-2}	0.05 (1.9)	0.05 (2.1)	mm (in.x10^{-3})		1,2	6,7,8
Space Width Error	1b	1s	Δs_{1-1}	-0.04 (-1.4)	-0.04 (-1.4)	mm (in.x10^{-3})		1,2	6,7,8
	2b	1s	Δs_{2-1}	-0.03 (-1.0)	-0.03 (-1.1)	mm (in.x10^{-3})		1,2	6,7,8
	1b	2s	Δs_{1-2}	-0.07 (-2.7)	-0.08 (-3.3)	mm (in.x10^{-3})		1,2	6,7,8
	2b	2s	Δs_{2-2}	-0.06 (-2.4)	-0.06 (-2.4)	mm (in.x10^{-3})		1,2	6,7,8

Notes:
1. Storage Temperature is dictated by Wand case.
2. Power supply ripple and noise should be less than 100 mV.
3. Switch bounce causes a series of sub-millisecond pulses to appear at the output, V_O. (HEDS-3000 only)
4. Push-to-Read switch is depressed, and the Wand is placed on a non-reflecting (black) surface. (HEDS-3000 only)
5. The margin refers to the reflecting (white) space that preceeds the first bar of the bar code.
6. The interior bars and spaces are those which follow the first bar of bar code tag.
7. The standard test tag consists of black bars, white spaces (0.3 mm, 0.012 in. min.) photographed on Kodagraph Transtar TC5® paper with a print contrast signal greater than 0.9.
8. The print contrast signal (PCS) is defined as: PCS = $(R_w - R_b)/R_w$, where R_w is the reflectance at 700 nm from the white spaces, and R_b is the reflectance at 700 nm for the bars.
9. 1.0 in. = 25.4 mm, 1 mm = 0.0394 in.
10. The Wand is in the preferred orientation when the surface of the label is parallel to the height dimension of the bar code.

OPERATION CONSIDERATIONS

The Wand resolution is specified in terms of a bar and space Width Error, WE. The width error is defined as the difference between the calculated bar (space) width, B, (S), and the optically measured bar (space) widths, b (s). When a constant scan velocity is used, the width error can be calculated from the following.

$B = t_b \cdot v_{scan}$

$S = t_s \cdot v_{scan}$

$\Delta b = B - b$

$\Delta s = S - s$

Where

Δb, Δs = bar, space Width Error (mm)

b, s = optical bar, space width (mm)

B, S = calculated bar, space width (mm)

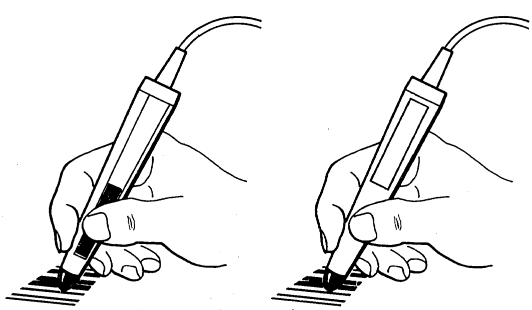
v_{scan} = scan velocity (mm/s)

t_b, t_s = wand pulse width output(s)

The magnitude of the width error is dependent upon the width of the bar (space) preceeding the space (bar) being measured. The Guaranteed Width Errors are specified as a maximum for the margin to first bar transition, as well as, maximums and minimums for the bar and space width errors resulting from transitions internal to the body of the bar code character. The Typical Width Error Performance specifies all possible transitions in a two level code (e.g. 2 of 5). For example, the Δb_{2-1} Width Error specifies the width error of a single bar module (0.3 mm) when preceeded by a double space module (0.6 mm).

The Bar Width Error Δb, typically has a positive polarity which causes the calculated bar, B, to appear wider than its printed counterpart. The typical negative polarity of the Space Width Error Δs, causes the measured spaces to appear narrower. The consistency of the polarity of the bar and space Width Errors suggest decoding schemes which average the measured bars and measured spaces within a character. These techniques will produce a higher percentage of good reads.

The Wand will respond to a bar code with a nominal module width of 0.3 mm when it is scanned at tilt angles between 0° and 30°. The optimum performance will be obtained when the Wand is held in the preferred orientation (Figure 1), tilted at an angle of 10° to 20°, and the Wand tip is in contact with the tag. The Wand height, when held normal to the tag, is measured from the tip's aperture, and when it is tilted it is measured from the tip's surface closest to the tag. The Width Error is specified for the preferred orientation, and using a Standard Test Tag consisting of black bars and white spaces. Figure 2 illustrates the random two level bar code tag. The Standard Test Tag is photographed on Kodagraph Transtar TC5® paper with a nominal module width of 0.3 mm (0.012 in.) and a Print Contrast Signal (PCS) of greater than 90%.



HEDS-3000 HEDS-3050

Figure 1. Preferred Wand Orientation.

BAR WIDTH 0.3 mm (0.012 in.) BLACK & WHITE

$R_{WHITE} \geq 75\%$, PCS $\geq$ 0.9 KODAGRAPH TRANSTAR TC5® PAPER

Figure 2. Standard Test Tag Format.

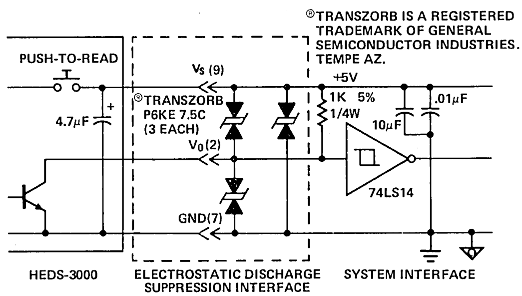


Figure 3a. Recommended Logic Interface for HEDS-3000

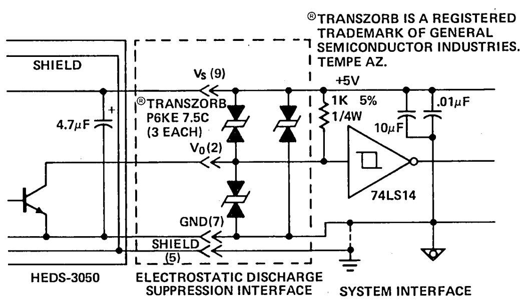


Figure 3b. Recommended Logic Interface for HEDS-3050. (When earth ground is not available, connect shield to logic ground, as shown by dotted line)

Typical Performance Curves ($R_L = 2.2k\Omega$)

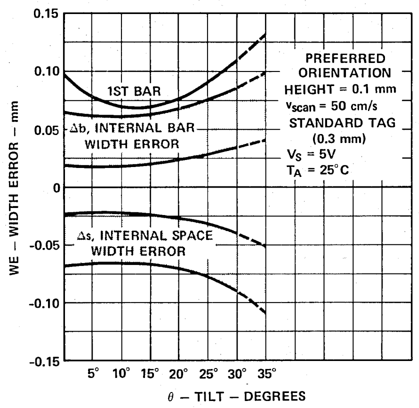


Figure 4. Width Error vs. Tilt (Preferred Orientation).

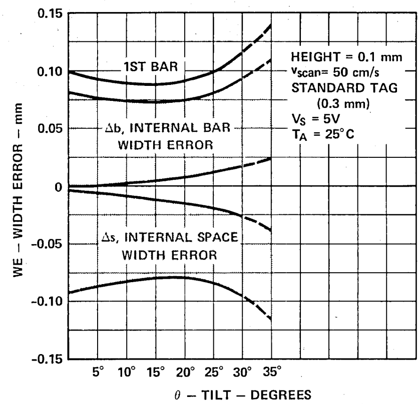


Figure 5. Width Error vs. Tilt (Any Orientation).

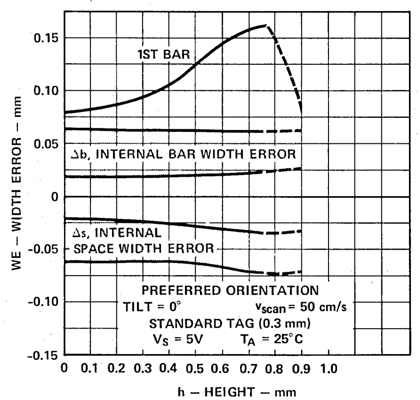


Figure 6. Width Error vs. Height (Preferred Orientation).

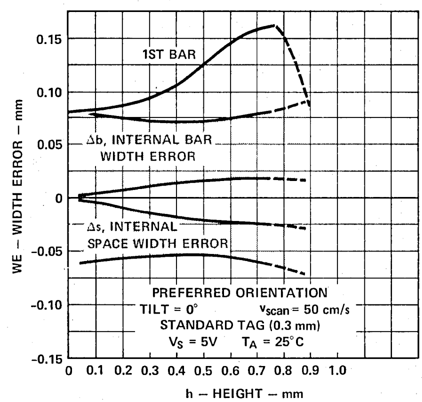


Figure 7. Width Error vs. Height (Any Orientation).

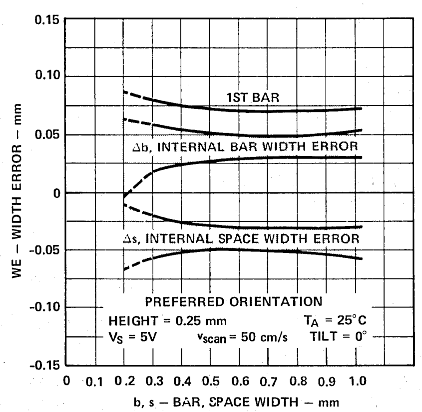


Figure 8. Width Error vs. Bar Width.

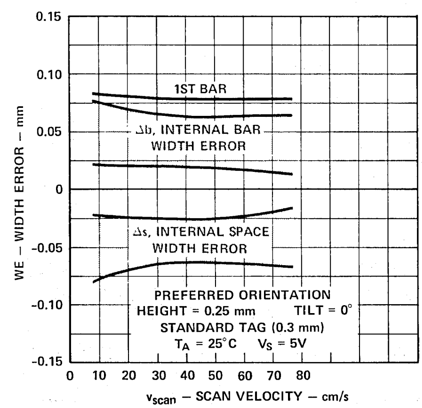


Figure 9. Width Error vs. Scan Velocity.

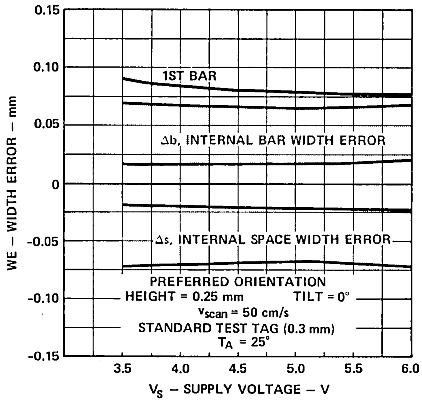


Figure 10. Width Error vs. Supply Voltage.

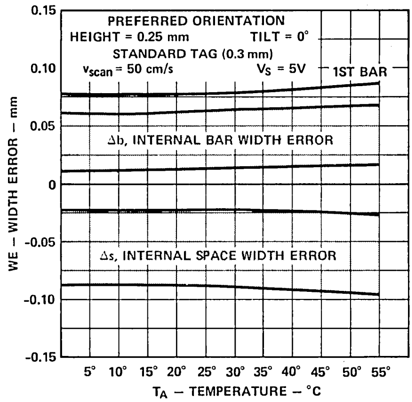


Figure 11. Width Error vs. Temperature.

MECHANICAL CONSIDERATIONS

The HEDS-3000/-3050 include a standard nine pin D-style connector with integral squeeze-to-release retention mechanism. Two types of receptacles with the retention mechanism are available from AMP Corp. (Printed circuit header: 745001-2 Panel mount: 745018, body; 66570-3, pins). Panel mount connectors that are compatible with the Wand connector, but do not include the retention mechanism, are the Molex A7224, and AMP 2074-56-2.

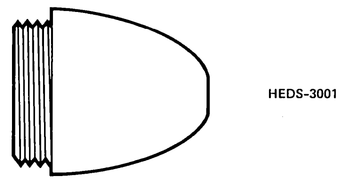


Figure 12. Wand Tip.

MAINTENANCE CONSIDERATIONS

While there are no user serviceable parts inside the Wand, the tip should be checked periodically for wear and dirt, or obstructions in the aperture. The tip aperture is designed to reject particles and dirt but a gradual degradation in performance will occur as the tip wears down, or becomes obstructed by foreign materials.

Before unscrewing the tip, disconnect the Wand from the system power source. The aperture can be cleaned with a cotton swab or similar device and a liquid cleaner.

The glass window on the sensor should be inspected and cleaned if dust, dirt, or fingerprints are visible. To clean the sensor window dampen a lint free cloth with a liquid cleaner, then clean the window with the cloth taking care not to disturb the orientation of the sensor. DO NOT SPRAY CLEANER DIRECTLY ON THE SENSOR OR WAND.

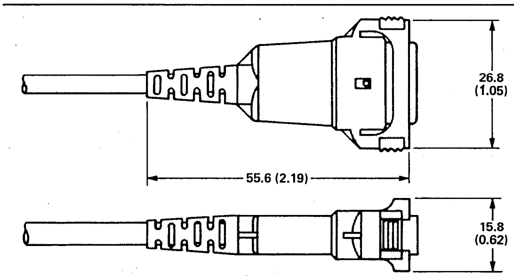
After cleaning the tip aperture and sensor window, the tip should be gently and securely screwed back into the Wand assembly. The tip should be replaced if there are visible indications of wear such as a disfigured, or distorted aperture. The part number for the Wand tip is HEDS-3001. It can be ordered from any franchised Hewlett-Packard distributor.

OPTIONAL FEATURES

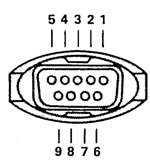
The wand may also be ordered with the following special features:

- Special colors
- Customer specified label
- No label
- Heavy duty retractable coiled cord
- No connector
- With/without switch button

For more information, call your local Hewlett-Packard sales office or franchised distributor.



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).



Pin	Wire Color	HEDS-3000 Function	HEDS-3050 Function
1	NC	NC	NC
2	White	V_O Output	V_O Output
3	NC	NC	NC
4	NC	NC	NC
5	—	NC	Shield
6	NC	NC	NC
7	Black	Ground	Ground
8	NC	NC	NC
9	Red	V_S Supply Voltage	V_S Supply Voltage

Figure 13. Connector Specifications.

HEWLETT PACKARD

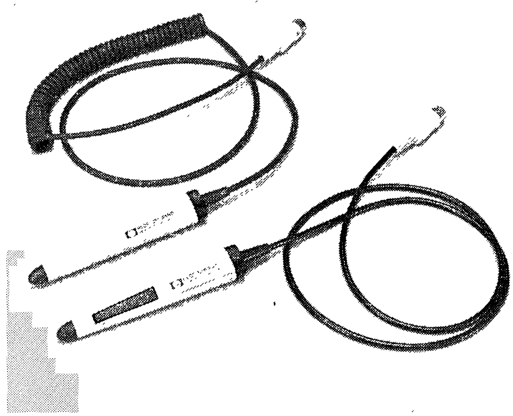
HIGH-RESOLUTION DIGITAL BAR CODE WAND

HEDS-3200
HEDS-3201
HEDS-3250
HEDS-3251

TECHNICAL DATA JANUARY 1986

Features

- **0.13 mm (0.005 in.) SPOT SIZE**
  Enhances Readability of High-Resolution Bar Codes
- **DECODABILITY SPECIFIED FOR BAR CODES WITH 0.19 mm (0.0075 in.) NARROW BAR WIDTH**
- **PUSH-TO-READ SWITCH (HEDS-3200/3201)**
  Minimizes Power Consumption in Battery Operated Systems
- **SHIELDED CASE, CABLE, AND CONNECTOR (HEDS-3250/3251)**
  Maximizes EMI/ESD Immunity in AC Powered Systems
- **DIGITAL OUTPUT**
  Open Collector Output Compatible with TTL and CMOS
- **SINGLE 5V SUPPLY OPERATION**
- **ATTRACTIVE, HUMAN ENGINEERED CASE**
- **DURABLE, LOW FRICTION TIP**
- **SOLID STATE RELIABILITY**
  Uses LED and IC Technology



Description

Hewlett-Packard's High-Resolution Digital Bar Code Wands are hand-held scanners optimized to read all common bar code formats that have the narrowest bars (spaces) printed with a nominal width of 0.19 mm (0.0075 in.). The wands contain an optical sensor with an 820 nm infrared LED, photo IC detector, and precision aspheric optics. Internal signal conditioning circuitry converts the optical information into a logic level pulse width representation of the bars and spaces. The output signal is specified to be decodable when scanning a 2-level bar code which has a narrow bar (space) width of 0.19 mm (0.0075 in.) and a minimum wide bar (space) to narrow bar (space) ratio of 2.2:1. The 3 of 9 Alphanumeric Code is an example of such a bar code.

The HEDS-3200/01, with a push-to-read switch, are recommended for use in battery powered applications requiring low power consumption. The HEDS-3250/51 feature an internal shield which maximizes immunity to electromagnetic interference (EMI), electrostatic discharge (ESD), and ground loops. These wands are recommended for use in AC powered systems.

Both standard wand configurations are available with either a strain relieved 104 cm (41 in.) straight cord or a strain relieved coiled cord. The coiled cord has a maximum extended length of 250 cm. (100 in.) and a comfortably extended length of 190 cm. (75 in.). The standard connector for all models is a 5 pin, 240 degree DIN connector.

Applications

The High-Resolution Digital Bar Code Wand is an effective alternative to the keyboard when used to collect information in compact, self-contained blocks. Bar code scanning is faster than key entry and is also more accurate since most codes have built-in checksums which prevent incorrect data from being entered.

High-resolution bar codes are typically used in applications where the number of characters to be represented and the physical space available together require a bar code symbol with high information density. The primary code characteristics which influence information density are the code structure and the narrow bar (space) width. Once the bar code type has been selected, a high-resolution symbol is used to achieve the highest information density for that code structure.

Applications for high-resolution bar codes include: material handling and inventory control; remote data collection; item identification for assemblies in service, repair, manufacturing, or testing; ticket identification; security checkpoint verification; file folder tracking; book, magazine, or general publication distribution; fixed asset accounting; and the programming of microprocessor-based systems such as consumer products (appliances, video recorders, games, etc.), intelligent instrumentation and control equipment, personal computers, and calculators.

BAR CODE COMPONENTS

Selection Guide

Part Number	Case Configuration	Cord Configuration	Note
HEDS-3200	Switched	Straight	1
HEDS-3201	Switched	Coiled	2
HEDS-3250	Shielded, Non-Switched	Straight	1
HEDS-3251	Shielded, Non-Switched	Coiled	2

NOTES:
1. Straight Cord Dimensions are 41 in. wand-to-connector.
2. Coiled Cord Dimensions are 29 in. wand-to-coil, 8 in. coil (collapsed), 10 in. coil-to-connector.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-20	55	°C	3
Operating Temperature	T_A	-20	55	°C	
Supply Voltage	V_S	-0.5	6.0	V	
Output Transistor Power	P_t		200	mW	
Output Collector Voltage	V_O		20	V	

NOTE:
3. Maximum Storage Temperature is dictated by the wand case.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Bar/Space Width	b, s	0.150 (0.006)		mm (in.)	
Scan Velocity	V_{SCAN}	5	100	cm/sec	
Contrast	R_w-R_b	65		%	4
Temperature	T_A	-20	55	°C	
Relative Humidity	RH		95	%	5
Ambient Light	E_V		2000	lux	6
Supply Voltage	V_S	4.5	5.5	V	7
Tilt Angle	Θ	0	30	degrees	
Height	See Figure 7				
Orientation	See Figure 1				8

NOTES:
4. Contrast is defined as R_w-R_b where R_w is the reflectance at 820 nm from the white spaces and R_b is the reflectance at 820 nm from the black bars. Contrast is directly related to Print Contrast Signal (PCS = (R_w-R_b /R_w) as it is equivalent to R_wxPCS.
5. Non-Condensing.
6. Ambient Light sources can be diffuse tungsten, fluorescent, sunlight, or a combination thereof. Performance in ambient light levels above 2000 lux will vary depending on the light source and shading at the wand tip.
7. Power Supply ripple and noise should be less than 100 mV.
8. The wand is in the preferred orientation when the surface of the wand label is parallel to the bars and spaces in the bar code symbol as shown in Figure 1.

Electrical Operation

The High-Resolution Digital Bar Code Wands consist of a precision optical sensor, an analog amplifier, a digitizing circuit, and an output transistor. These elements provide a TTL compatible output from a single 4.5V to 5.5V power supply. The open collector transistor used at the output requires an external pull-up resistor for proper operation.

A non-reflecting black bar results in a logic high (1) level while a reflecting white space will cause a logic low (0) level. The initial or "wake-up" state will always be the correct (logic low) state when the wand is placed on reflecting white surface. The initial state is indeterminate if the wand is placed on a black surface or is pointed into free space.

The HEDS-3250/51 provide a case, cable, and connector shield which must be terminated to logic ground or, preferably, to both logic ground and earth ground. This will provide a substantial improvement in EMI/ESD immunity in AC powered systems. It is recommended that the shield be properly terminated even when EMI and ESD are not of concern because the shield will otherwise act as an antenna, injecting electrical noise into the wand circuitry.

The HEDS-3200/01 incorporate a push-to-read switch which is used to energize the LED emitter and electronic circuitry. When the switch is initially depressed, contact bounce may cause a series of random pulses to appear at the output V_O. This pulse train will typically settle to a final value within 5 ms. The final value will be the initial or "wake-up" state.

The recommended logic interface for the wands is shown in Figure 3. This interconnection provides maximum ESD protection for both the wand and the user's electronics.

Electrical Characteristics (V_S = 4.5V to 5.5V, T_A = 25°C, R_L = 1.0-10 kΩ, unless otherwise noted)

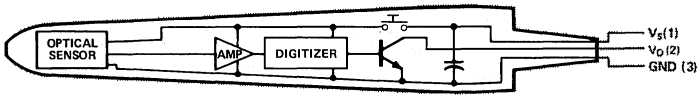
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Switch Bounce (HEDS-3200/3201)	t_{sb}		0.5	5	ms			9
High Level Output Current	I_{OH}			400	μA	V_{OH} = 2.4V Bar condition (Black)	3	
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA Space Condition (White)	3	
Output Rise Time	t_r		2		μs	10%-90% Transition R_L = 1.0 kΩ	3	
Output Fall Time	t_f		100		ns	90%-10% Transition	3	
Supply Current	I_s		35	50	mA	V_S = 5V, Bar Condition (Black)		10

NOTES:

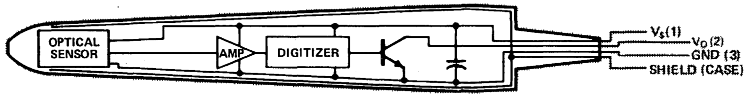
9. Switch bounce causes a series of sub-millisecond pulses to appear at the output, V_O (HEDS-3200/3201 only).
10. Push-to-Read switch is depressed (if applicable) and the wand is scanning on a non-reflecting (black) surface.

Block Diagram

HEDS-3200/3201 (with switch)



HEDS-3250/3251 (shielded)

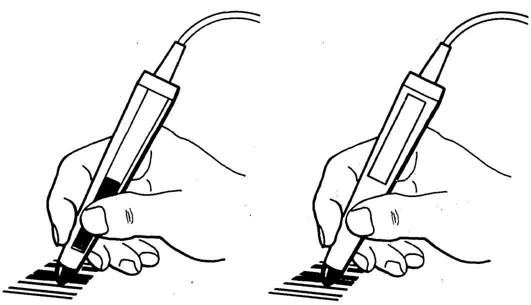


Scanning Performance (V_S = 5V, R_L = 1.0-10 kΩ, T_A = 25°C, V_{SCAN} = 50 cm/sec)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Decodability Index	DI		14	22	%	Tilt = 0 to 30° Preferred Orientation	1,2 4,5 6,7 8	11,13 14
Average Width Error (Narrow Bars)	OS_{bn}		0.030 (0.0012)		mm (in.)	Standard Test Tag	1,2 9	12
Average Width Error (Wide Bars)	OS_{bw}		0.021 (0.0008)		mm (in.)			
Average Width Error (Narrow Spaces)	OS_{sn}		-0.015 (-0.0006)		mm (in.)			
Average Width Error (Wide Spaces)	OS_{sw}		-0.044 (-0.0017)		mm (in.)			
Deviation from Average (Internal Elements)	de		0.023 (0.0009)	0.038 (0.0015)	mm (in.)		1,2 4,5 6,7 8	15
Deviation from Average (First Bar)	db_1		0.054 (0.0021)	0.110 (0.0043)	mm (in.)			

NOTES:

11. The standard test tag is designed to include all possible combinations of wide or narrow bars and spaces. The tag, shown in Figure 2, consists of black bars and white spaces with a narrow element width of 0.19 mm (0.0075 in.) and a wide element width of 0.42 mm (0.0165 in.). This equates to a wide-to-narrow ratio of 2.2:1. A margin, or white reflecting area, of at least 5 mm in width precedes the first bar. The test tag is photographically reproduced on KODAGRAPH TRANSTAR TC5® paper with R_W = 0.9 and PCS greater than 0.9, yielding a contrast greater than 0.81.
12. The difference between the calculated bar (space) width derived from the digital output and the optically measured bar (space) width defines width error (WE). The Average Width Error for the narrow or wide bars (spaces) specifies the systematic error in the output signal. This systematic error is largely due to paper bleed and is thus very dependent on the symbol media.
13. $DI = \frac{de + \Delta OS/4}{m} \times 100$, expressed as a percentage of the module width. "de" is the deviation from the average width error for the internal bars (spaces), "ΔOS" is the difference in average width error between the wide and narrow bars (spaces), and "m" is the optically measured narrow bar (space) or "module" width. The first bar is not included due to its unique characteristics.
14. DI is calculated independently for bars and spaces and the worst-case, largest DI is used. This results in a DI specification which applies only to the bars since the DI for the bars is characteristically larger than the DI for the spaces.
15. Deviation from the Average Width Error (de, db_1) specifies the random errors in the output signal which are largely due to digitizing noise. The first bar, which generally appears larger than the interior bars, has a deviation significantly larger than the deviation for the interior bars (spaces).



HEDS-3200/01 HEDS-3250/51

Figure 1. Preferred Wand Orientation

BAR WIDTH 0.19 mm (0.0075 in.) BLACK & WHITE

CONTRAST ≥ 65% KODAGRAPH TRANSTAR TC5® PAPER

Figure 2. Standard Test Tag Format

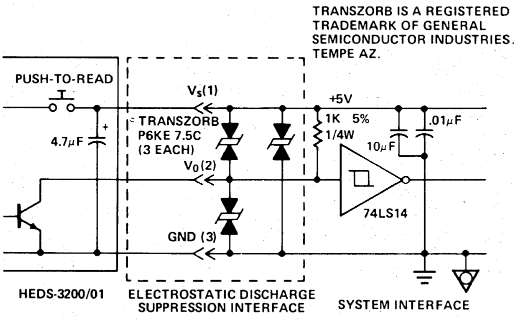


Figure 3a. Recommended Logic Interface for HEDS-3200/01

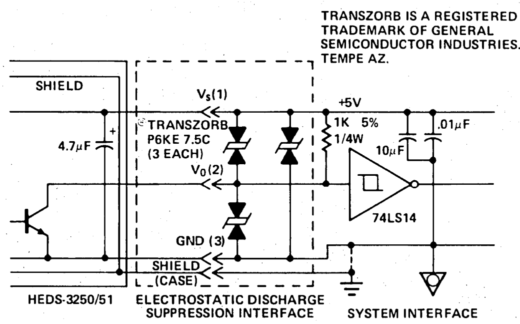


Figure 3b. Recommended Logic Interface for HEDS-3250/51. (When earth ground is not available, connect shield to logic ground, as shown by dotted line)

Typical Performance Curves

(V_S = 5V, R_L = 1.0 kΩ, T_A = 25°C, Tilt = 15°, unless otherwise specified)

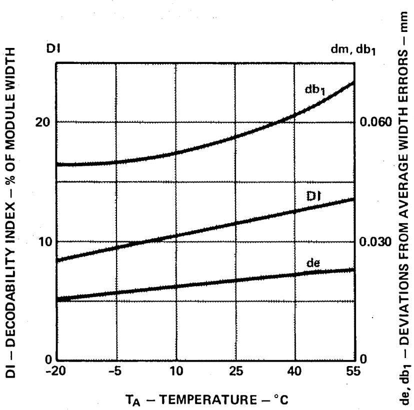


Figure 4. Decodability Index and Deviation from Average Width Error vs. Temperature

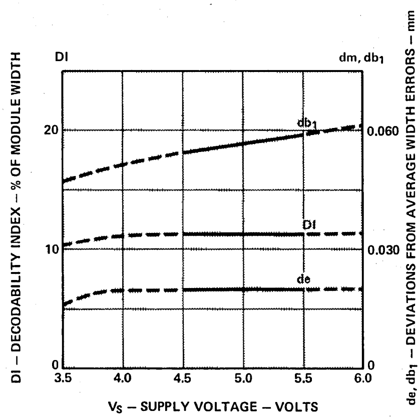


Figure 5. Decodability Index and Deviation from Average Width Error vs. Supply Voltage

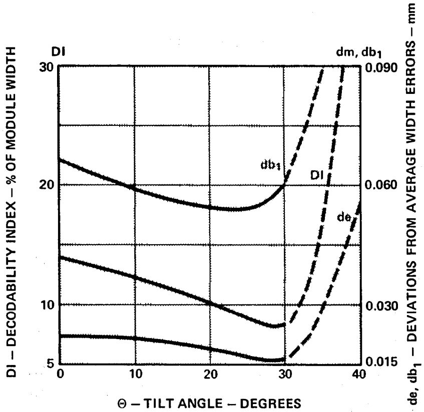


Figure 6. Decodability Index and Deviation from Average Width Error vs. Tilt Angle

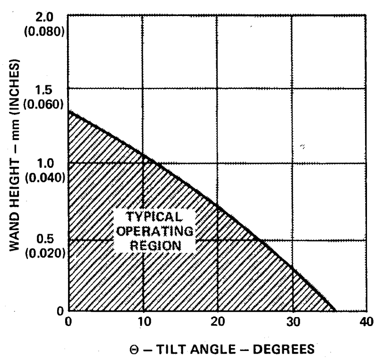


Figure 7. Wand Height vs. Tilt Angle Operating Region

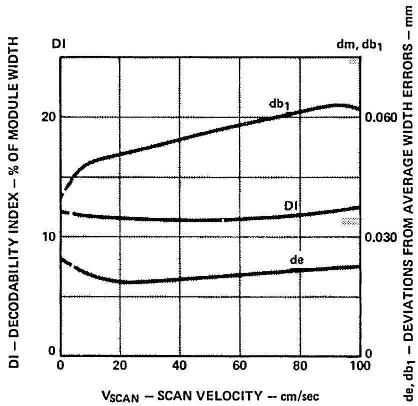


Figure 8. Decodability Index and Deviation from Average Width Error vs. Scan Velocity

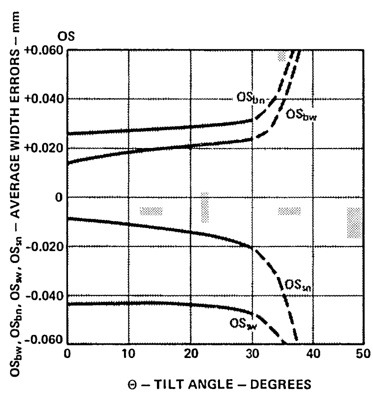


Figure 9. Average Width Errors vs. Tilt Angle

Operation Considerations

The HEDS-32XX series of wands provide TTL compatible pulse widths whose widths are determined by the printed bar (space) width and the scan velocity (V_{SCAN}). When scanning a black and white printed bar code, the wand will output a logic high (1) for a non-reflecting black bar and a logic low (0) for a reflecting white space.

The serial time data from the wand represents the bar code symbol's binary data in a width modulated format. When scanning a 3 of 9 Code symbol at a constant velocity, for example, the longer (wide) time intervals encode binary ones (1) and the shorter (narrow) time intervals encode binary zeros (0). The wide (1) and narrow (0) time intervals may represent either bars or spaces.

The wand's serial data is supplied to a decoder which translates the time width data into binary character bit images. The decoding algorithm sets a decision threshold which is compared to the pulse width data supplied by the wand. Those time intervals which are larger than the threshold are decoded as ones (1), and those smaller as logic zeros (0). The accuracy of this decision is dependent upon the ability of the algorithm to compensate for systematic and random errors introduced by the wand and the printer.

Printers and wands can be characterized as having both Offset (systematic) and Noise (random) errors. The printer Offset (OS_P) results from ink bleeding or ink shrinkage. Ink bleeding causes the bars to be printed wider and the spaces narrower. Conversely, ink shrinkage causes bars to be narrower and spaces wider. The random component for the printer is the variation of the printed bar (space) widths centered around the Offset (OS_P).

For the wands, Offset (OS_W) causes bars to be wider and spaces narrower than they are actually printed. The random component (dm) for the wand is the variation of the width error centered around the wand Offset (OS_W).

An algorithm that creates a separate decision threshold (T) for bars and spaces compensates for the offset errors of both the printer and the wand. When this is done, the dominant errors become the random components of the printer and the wand. The optimal algorithm to calculate a decision threshold (T) selects the time mid-point between the time intervals for the wide and narrow bars, or spaces, within a single character. This threshold, in the worst case, can be expressed by:

$$T = \frac{N(min) + W(min)}{2},$$

where

T = decision threshold
N(min) = minimum narrow width
W(min) = minimum wide width

When evaluating a population of bars and spaces, the threshold (T) should always be greater than the widest narrow bar (space) and smaller than the narrowest wide bar (space). The condition shown below describes the worst-case condition:

$$N(max) < \frac{N(min) + W(min)}{2}$$

Each of these three components — N(max), N(min), and W(min) — can be represented as a nominal element width plus offset and random components.

When the offset and random errors are combined to represent the narrowest narrow, and the narrowest wide bar (space), they can be inserted into the previous equations. With a little algebraic manipulation, the equation can be segmented to describe a decodability limit (DL) for the bar code as it compares to a decodability index of the printer (DI_P) and the wand (DI_W). This analysis leads to the two error sensitivity equations shown below:

Bar Error Sensitivity

Decodability Limit (DL_b) > Printer (DI_{bp}) + Wand (DI_{bw})

$$\frac{(WB{:}NB - 1)}{4} > \frac{(OS_{bpN} - OS_{bpW}) + (3\delta_{bpN} + \delta_{bpW})}{4m} + \frac{(OS_{bwN} - OS_{bwW}) + 4de_{bw}}{4m}$$

Space Error Sensitivity

Decodability Limit (DL_S) > Printer (DI_{sp}) + Wand (DI_{sw})

$$\frac{(WS:NS - 1)}{4} > \frac{(OS_{spN} - OS_{spW}) + (3\delta_{spN} + \delta_{spW})}{4m} + \frac{(OS_{swN} - OS_{swN}) + 4de_{sw}}{4m}$$

The first term of the equation estimates the offset and random errors of the printer (DI_p) while the second term describes the offset and random errors of the wand (DI_W). The random errors of the wand (de_{bw}, de_{sw}) are the combination of the wide (δ_{wW}) and narrow (δ_{wN}) random components. The individual random components are summed because, in the case of the wand, they are approximately equal.

These two equations allow a system designer to predict, given the wide to narrow ratio (W:N), module width (m), and errors (OS, δ), whether the decoder will correctly recognize the narrow time interval as a narrow bar (space) and the wide time interval as a wide bar (space). The (W:N — 1)/4 factor in the equation is defined as the decodability limit (DL) of the symbology. To ensure decodability, this number should be greater than the sum of the errors introduced by the printer and wand. The wand may, however, render a decodable signal even if the combination of printer and wand errors exceed the decodability limit (DL). This results from the introduction of other random variables such as the operator scan velocity, acceleration and deceleration profiles, and the sampling times of the decoder time interval counter. These factors can bias the printer and wand errors, thus permitting the decoder to make the correct decision.

When using the prescribed decoding algorithm and the concept of decodability presented above, the system designer should independently evaluate the decodability of the bars and the spaces. The decodability index for the wand (DI_W) is typically larger for bars than for spaces while the decodability index for the printer is typically larger for the spaces. If an algorithm which does not separate bars and spaces is used, the designer must evaluate the offset differences between the bars and spaces in addition to the analysis presented above. This introduces another variable into the system as the wand offset is dependent on the characteristics of the paper media.

The best first read rate can be achieved when good quality printed bar code symbols are used. Good quality high-resolution bar codes can be pre-printed or printed on-demand with "drummer" label printers using OCR ribbons and good quality label stock. Bar code symbols which are printed on very translucent media, as are some photolithographic symbols, can cause the wand offset to be excessive due to paper bleed. This will degrade system performance, particularly for algorithms which compare bars and spaces.

The high resolution wand is not recommended for use with bar codes printed on dot matrix printers because of the print flaws (spots and voids) which are characteristic of this printing process. These flaws may be large enough to be recognized as bars (spaces) by a high resolution wand, leading to a mis-read.

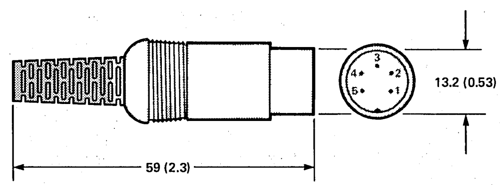
Table 1. Definition of Terms

Bars	Spaces	Definition
DL_b	DL_s	decodability limit
DI_{bp}	DI_{sp}	printer decodability index
DI_{bw}	DI_{sw}	wand decodability index
WB:NB	WS:NS	wide to narrow ratio
OS_{bpN}	OS_{spN}	printer offset, narrow element
OS_{bpW}	OS_{spW}	printer offset, wide element
OS_{bwN}	OS_{swN}	wand offset, narrow element
OS_{bwW}	OS_{swW}	wand offset, wide element
δ_{bpN}	δ_{spN}	printer random error, narrow element
δ_{bpW}	δ_{spW}	printer random error, wide element
de_{bw}	de_{sw}	wand random error
m	m	module width (narrow element width)

Mechanical Considerations

The HEDS-32XX wands include a standard 5 pin, 240 degree DIN connector. The detailed specifications and pin-outs are shown in Figure 10. Mating connectors are available from RYE Industries and Switch Craft in both 5 pin and 6 pin configurations. These connectors are listed below:

Connector	Configuration
RYE MAB-5	5 Pin
Switch Craft 61GA5F	5 Pin
Switch Craft 61HA5F	5 Pin
RYE MAB-6	6 Pin
Switch Craft 61GA6F	6 Pin



NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).

PIN	WIRE COLOR	HEDS-3200/01	HEDS-3250/51
1	RED	V_S SUPPLY VOLTAGE	V_S SUPPLY VOLTAGE
2	WHITE	V_O OUTPUT	V_O OUTPUT
3	BLACK	GROUND	GROUND
4	N/A	N/C	N/C
5	N/A	N/C	N/C
CASE	-	N/C	SHIELD

Figure 10. Connector Specifications

Maintenance Considerations

While there are no user serviceable parts inside the Wand, the tip should be checked periodically for wear and dirt, or obstructions in the aperture. The tip aperture is designed to reject particles and dirt but a gradual degradation in performance will occur as the tip wears down, or becomes obstructed by foreign materials.

Before unscrewing the tip, disconnect the Wand from the system power source. The aperture can be cleaned with a cotton swab or similar device and a liquid cleaner.

The glass window on the sensor should be inspected and cleaned if dust, dirt, or fingerprints are visible. To clean the sensor window dampen a lint free cloth with a liquid cleaner, then clean the window with the cloth taking care not to disturb the orientation of the sensor. DO NOT SPRAY CLEANER DIRECTLY ON THE SENSOR OR WAND.

After cleaning the tip aperture and sensor window, the tip should be gently and securely screwed back into the Wand assembly. The tip should be replaced if there are visible indications of wear such as a disfigured, or distorted aperture. The part number for the Wand tip is HEDS-3001. It can be ordered from any franchised Hewlett-Packard distributor.

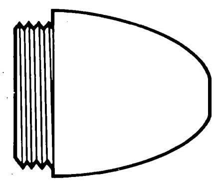


Figure 11. Wand Tip

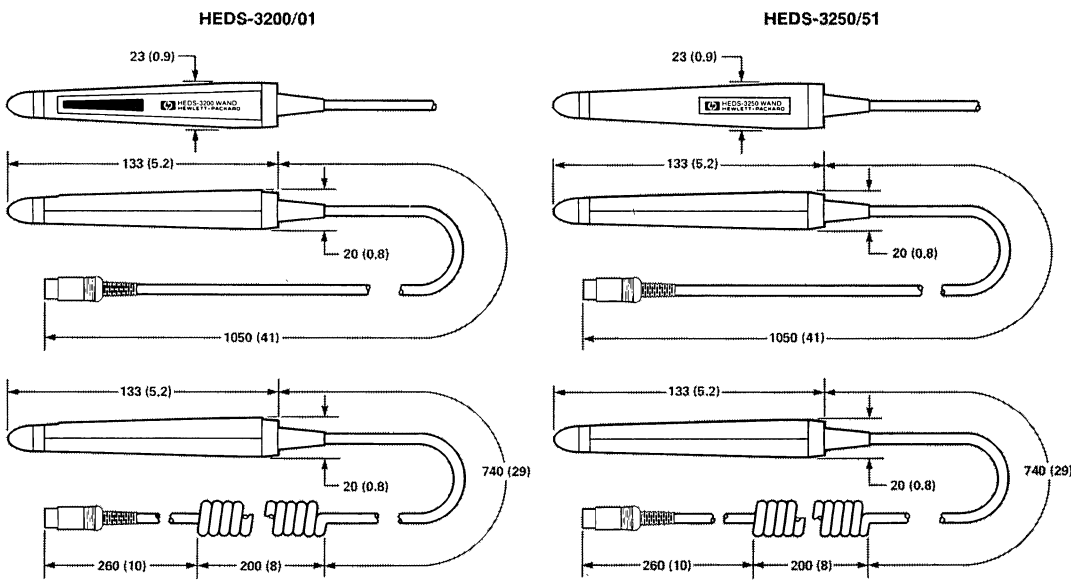
Optional Features

The wand may also be ordered with the following special features:

- Special colors
- Customer specified label
- No label
- Special Retractable Coiled Cords
- 9 Pin subminiature D-style plastic connector (same as HEDS-3000/3050)
- No connector (stripped and tinned leads)

For more information, call your local Hewlett-Packard sales office or franchised distributor.

Wand Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

BAR CODE COMPONENTS

HEWLETT PACKARD

HIGH RESOLUTION OPTICAL REFLECTIVE SENSOR

HBCS-1100

TECHNICAL DATA JANUARY 1986

Features

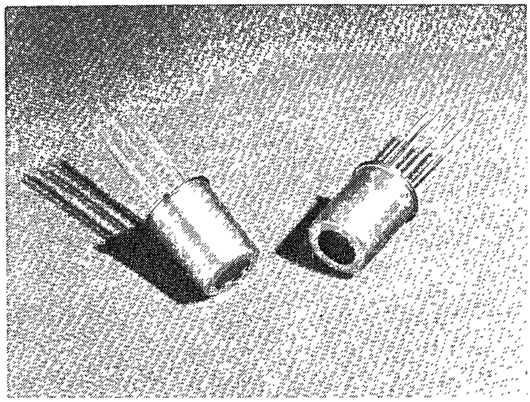
- **FOCUSED EMITTER AND DETECTOR IN A SINGLE PACKAGE**
- **HIGH RESOLUTION — .190mm SPOT SIZE**
- **700nm VISIBLE EMITTER**
- **LENS FILTERED TO REJECT AMBIENT LIGHT**
- **TO-5 MINIATURE SEALED PACKAGE**
- **PHOTODIODE AND TRANSISTOR OUTPUT**
- **SOLID STATE RELIABILITY**

Description

The HBCS-1100 is a fully integrated module designed for optical reflective sensing. The module contains a .178mm (.007 in.) diameter 700nm visible LED emitter and a matched I.C. photodetector. A bifurcated aspheric lens is used to image the active areas of the emitter and the detector to a single spot 4.27mm (0.168 in.) in front of the package. The reflected signal can be sensed directly from the photodiode or through an internal transistor that can be configured as a high gain amplifier.

Applications

Applications include pattern recognition and verification, object sizing, optical limit switching, tachometry, textile thread counting and defect detection, dimensional monitoring, line locating, mark, and bar code scanning, and paper edge detection.

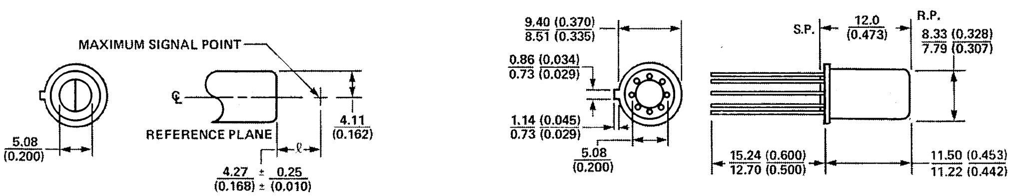


Mechanical Considerations

The HBCS-1100 is packaged in a high profile 8 pin TO-5 metal can with a glass window. The emitter and photodetector chips are mounted on the header at the base of the package. Positioned above these active elements is a bifurcated aspheric acrylic lens that focuses them to the same point.

The sensor can be rigidly secured by commercially available two piece TO-5 style heat sinks, such as Thermalloy 2205, or Aavid Engineering 3215. These fixtures provide a stable reference platform and their tapped mounting holes allow for ease of affixing this assembly to the circuit board.

Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. THE REFERENCE PLANE IS THE TOP SURFACE OF THE PACKAGE.
4. NICKEL CAN AND GOLD PLATED LEADS.
5. S.P. SEATING PLANE.
6. THE LEAD DIAMETER IS 0.45mm (0.018in.) TYP.

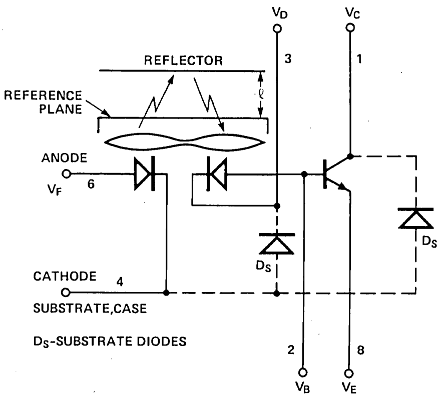
Electrical Operation

The detector section of the sensor can be connected as a single photodiode, or as a photodiode transistor amplifier. When photodiode operation is desired, it is recommended that the substrate diodes be defeated by connecting the collector of the transistor to the positive potential of the power supply and shorting the base-emitter junction of the transistor. Figure 15 shows photocurrent being supplied from the anode of the photodiode to an inverting input of the operational amplifier. The circuit is recommended to improve the reflected photocurrent to stray photocurrent ratio by keeping the substrate diodes from acting as photodiodes.

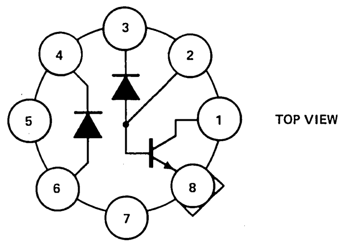
The cathode of the 700nm emitter is physically and electrically connected to the case-substrate of the device. Applications that require modulation or switching of the LED should be designed to have the cathode connected to the electrical ground of the system. This insures minimum capacitive coupling of the switching transients through the substrate diodes to the detector amplifier section.

The HBCS-1100 detector also includes an NPN transistor which can be used to increase the output current of the sensor. A current feedback amplifier as shown in Figure 6 provides moderate current gain and bias point stability.

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



PIN	FUNCTION
1	TRANSISTOR COLLECTOR
2	TRANSISTOR BASE, PHOTODIODE ANODE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
5	NC
6	LED ANODE
7	NC
8	TRANSISTOR EMITTER

Absolute Maximum Ratings at T_A=25°C

Parameter	Symbol	Min.	Max.	Units	Fig.	Notes
Storage Temperature	T_S	-40	+75	°C		
Operating Temperature	T_A	-20	+70	°C		
Lead Soldering Temperature 1.6mm from Seating Plane			260 for 10 sec.	°C		11
Average LED Forward Current	I_F		50	mA		2
Peak LED Forward Current	I_{FPK}		75	mA	1	1
Reverse LED Input Voltage	V_R		5	V		
Package Power Dissipation	P_P		120	mW		3
Collector Output Current	I_O		8	mA		
Supply and Output Voltage	V_D,V_C,V_E	-0.5	20	V		10
Transistor Base Current	I_B		5	mA		
Transistor Emitter Base Voltage	V_{EB}		.5	V		

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be introduced by ESD.

System Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Total Photocurrent ($I_{PR}+I_{PS}$)	I_P			575		T_A=-20°C		
		150	250	375	nA	T_A=25°C, I_F=35mA, V_D=V_C=5V	2,3	4
		80				T_A=70°C	15	
Reflected Photocurrent (I_{PR}) to Internal Stray Photocurrent (I_{PS})	$\frac{I_{PR}}{I_{PS}}$	4	8.5			I_F=35mA, V_C=V_D=5V	3	
Transistor DC Static Current Transfer Ratio	h_{FE}	50				T_A=-20°C, V_{CE}=5V, I_C=10μA	4,5	
		100	200			T_A=25°C		
Slew Rate			.08		V/μs	R_L=100K I_{PK}=50mA R_F= 10M t_{ON}=100μs, Rate = 1kHz	6	
Image Diameter	d		.17		mm	I_F=35mA, ℓ=4.27mm (0.168in.)	8,10	8,9
Maximum Signal Point	ℓ	4.01	4.27	4.52	mm	Measured from Reference Plane	9	
50% Modulation Transfer Function	MTF		2.5		lnpr/mm	I_F=35mA, ℓ =4.27mm	10,11	5,7
Depth of Focus	$\Delta\ell$ FWHM		1.2		mm	50% of I_P at ℓ=4.27mm	9	5
Effective Numerical Aperature	N.A.		.3					
Image Location	D		.51		mm	Diameter Reference to Centerline ℓ=4.27mm		6
Thermal Resistance	Θ_{JC}		85		°C/W			

Detector Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Dark Current	I_{PD}		5	200	pA	T_A=25°C, I_F=0, V_D=5V;		
				10	nA	T_A=70°C, Reflection=0%		
Capacitance	C_D		45		pF	V_D=0V, I_P=0, f=1MHz		
Flux Responsivity	$R\phi$		.22		$\frac{A}{W}$	λ=700nm, V_D=5V	12	
Detector Area	A_D		.160		mm^2	Square, with Length=.4mm/Side		

Emitter Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Forward Voltage	V_F		1.6	1.8	V	I_F=35mA	13	
Reverse Breakdown Voltage	BV_R	5			V	I_R=100μA		
Radiant Flux	ϕ_E	5	9.0		μW	I_F=35mA, λ=700nm	14	
Peak Wavelength	λ_p	680	700	720	nm	I_F=35mA	14	
Thermal Resistance	Θ_{JC}		150		°C/W			
Temperature Coefficient of V_F	$\Delta V_F/\Delta T$		-1.2		mV/°C	I_F=35mA		

Transistor Electrical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Collector-Emitter Leakage	I_{CEO}		1		nA	V_{CE}=5V		
Base-Emitter Voltage	V_{BE}		.6		V	I_C=10μA, I_B=70nA		
Collector-Emitter Saturation Voltage	V_{CE}(SAT)		.4		V	I_B=1μA, I_E=10μA		
Collector-Base Capacitance	C_{CB}		.3		pF	f=1MHz, V_{CB}=5V		
Base-Emitter Capacitance	C_{BE}		.4		pF	f=1MHz, V_{BE}=0V		
Thermal Resistance	Θ_{JC}		200		°C/W			

NOTES:
1. 300μs pulse width, 1 kHz pulse rate.
2. Derate Maximum Average Current linearly from 65°C by 6mA/°C.
3. Without heat sinking from T_A = 65°C, derate Maximum Average Power linearly by 12mW/°C.
4. Measured from a reflector coated with a 99% reflective white paint (Kodak 6080) positioned 4.27mm (0.168 in.) from the reference plane.
5. Peak-to-Peak response to black and white bar patterns.
6. Center of maximum signal point image lies within a circle of diameter D relative to the center line of the package. A second emitter image (through the detector lens) is also visible. This image does not affect normal operation.
7. This measurement is made with the lens cusp parallel to the black-white transition.
8. Image size is defined as the distance for the 10%-90% response as the sensor moves over an abrupt black-white edge.
9. (+) indicates an increase in the distance from the reflector to the reference plane.
10. All voltages referenced to Pin 4.
11. CAUTION: The thermal constraints of the acrylic lens will not permit the use of conventional wave soldering procedures. The typical preheat and post cleaning temperatures and dwell times can subject the lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.

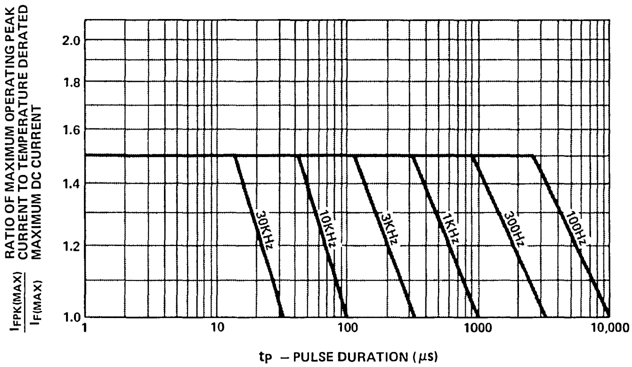


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

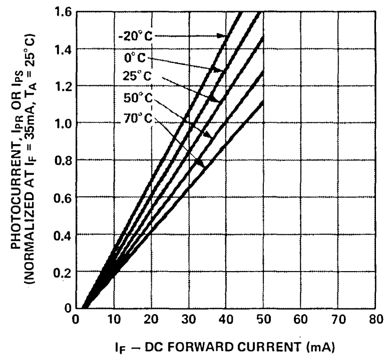
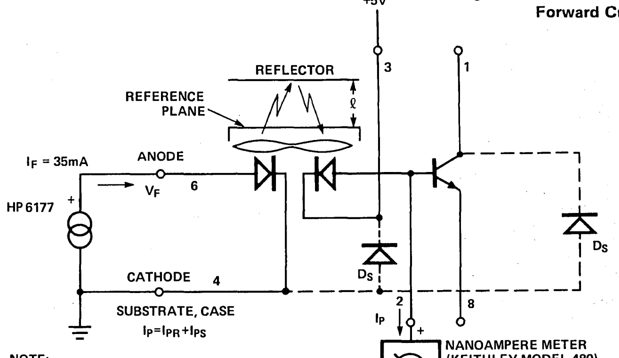


Figure 2. Relative Total Photocurrent vs. LED DC Forward Current



NOTE:
1. I_P MEASUREMENT CONDITIONS ARE; ℓ = 4.34mm, KODAK 6080 PAINT REFLECTOR.
2. I_{PS} MEASUREMENT CONDITIONS ARE; ℓ = ∞ A CAVITY WHOSE DEPTH IS MUCH GREATER THAN THE HBCS-1100 DEPTH OF FIELD.

Figure 3. Ip Test Circuit

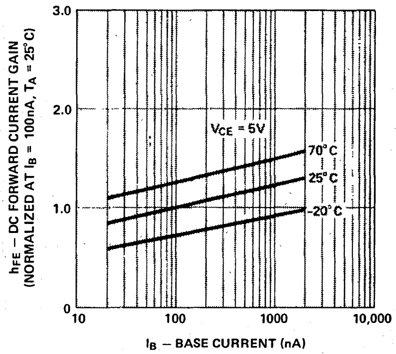


Figure 4. Normalized Transistor DC Forward Current Gain vs. Base Current at Temperature

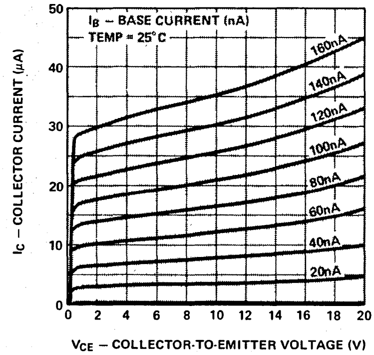


Figure 5. Common Emitter Collector Characteristics

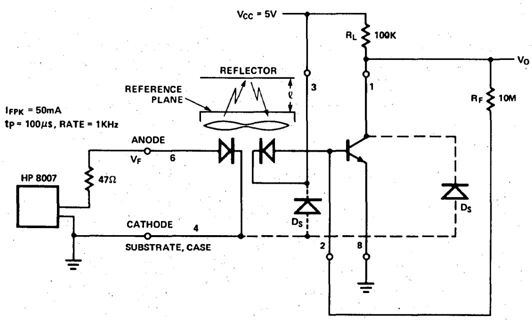


Figure 6. Slew Rate Measurement Circuit

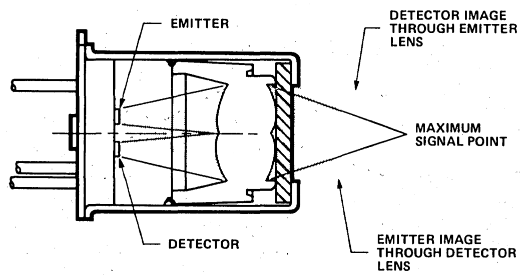


Figure 7. Image Location

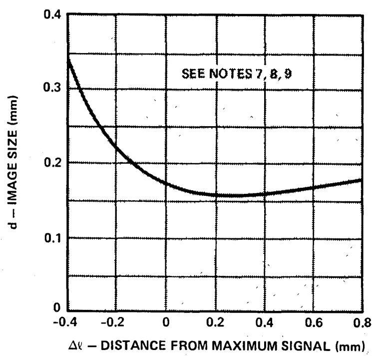


Figure 8. Image Size vs. Maximum Signal Point

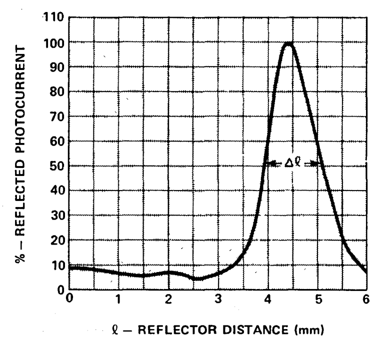


Figure 9. Reflector Distance vs. % Reflected Photocurrent

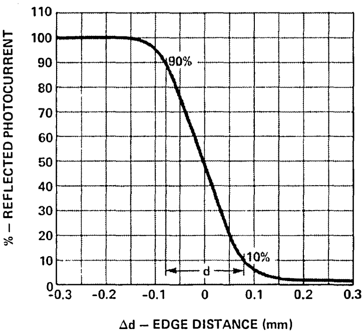


Figure 10. Step Edge Response

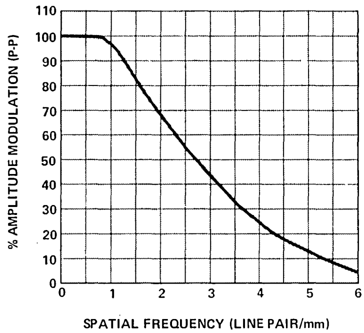


Figure 11. Modulation Transfer Function

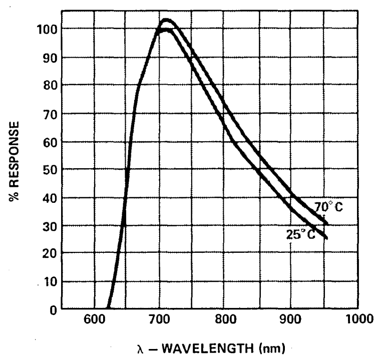


Figure 12. Detector Spectral Response

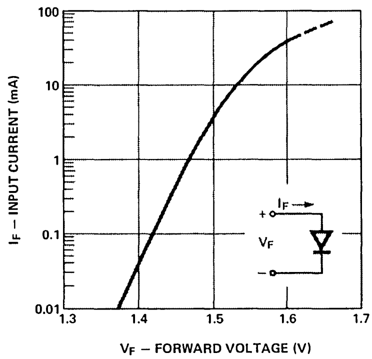


Figure 13. LED Forward Current vs. Forward Voltage Characteristics

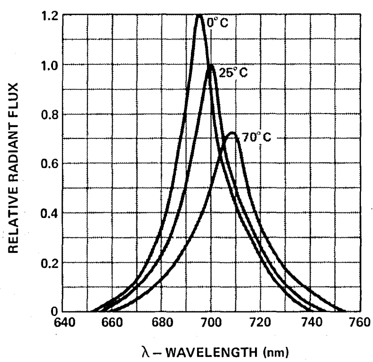


Figure 14. Relative Radiant Flux vs. Wavelength

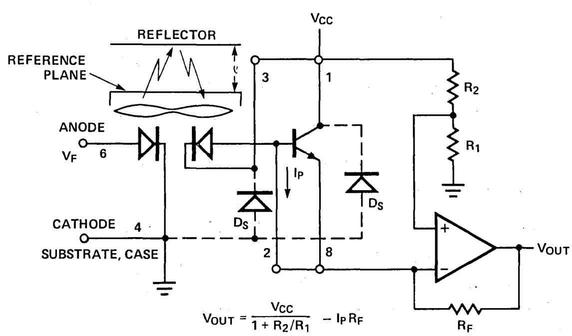


Figure 15. Photodiode Interconnection

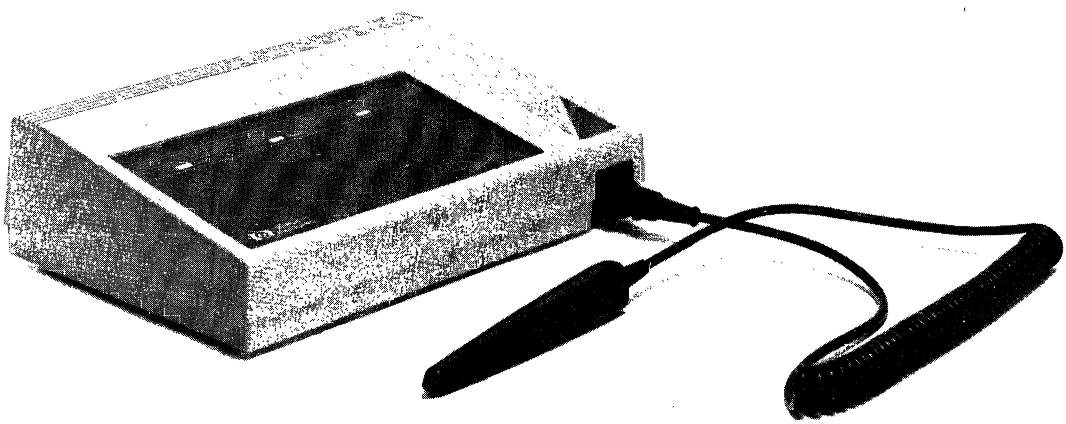
BAR CODE COMPONENTS

HEWLETT PACKARD

BAR CODE READERS

16800A
16801A

TECHNICAL DATA JANUARY 1986



Features

- **THREE INDUSTRIAL BAR CODES STANDARD:**
  - **— 3 of 9 Code**
  - **— Interleaved 2 of 5 Code**
  - **— Industrial 2 of 5 Code**
- **AUTOMATIC CODE RECOGNITION**
- **OPTIONAL BAR CODES AVAILABLE**
  - **— UPC/EAN/JAN**
  - **— Codabar**
  - **— Others**
- **FLEXIBLE DUAL RS-232-C (V.24) DATA COMMUNICATIONS**
  - **— Facilitates a Wide Variety of Configurations**
- **PROGRAMMABLE OPERATION (16800A only):**
  - **— Two LED Status Indicators**
  - **— Beeper Control**
  - **— Code Selection**
  - **— Data Communication Configuration**
  - **— Reader Operational Status**
- **HIGH PERFORMANCE DIGITAL WANDS:**
  - **— 45 Degree Scan Angle**
  - **— Sealed Sapphire Tip**
  - **— Polycarbonate or Metal Case**
- **INTEGRAL POWER SUPPLY**
- **TABLETOP OR WALL MOUNTABLE**
- **BUILT-IN SELF TEST**
- **WORLDWIDE HP SERVICE**

Description

The 16800A and 16801A are high performance bar code readers. The 16800A includes a wide range of programmable features which allow the reader to be fully integrated into sophisticated data entry systems. The 16801A is non-programmable, providing a more cost-effective solution for applications which do not require programmability.

The standard reader supports three popular industrial bar codes: 3 of 9 code, Interleaved 2 of 5 code, and Industrial 2 of 5 code. If more than one standard code is enabled, the reader will automatically recognize which code is being read. Options are available for reading UPC/EAN/JAN codes, Codabar code, and other bar codes. Bidirectional scanning is provided for all bar codes supported.

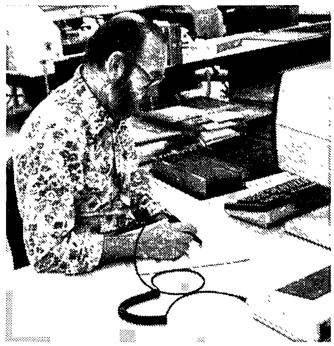
The 16800A and 16801A may be configured with a wide range of computer systems; including minicomputers, desktop computers, and personal computers. Dual RS-232-C (V.24) ports facilitate operation in both stand-alone and eavesdrop configurations. In an eavesdrop configuration, the reader will generally be operated in conjunction with an RS-232-C terminal.

Interactive systems design is supported in the 16800A through programmable operator feedback and reader control features. A multi-tone beeper and two LED indicators are provided to allow simple, yet flexible audio and visual programmable feedback. Local operator feedback is provided in the 16801A through a beeper which sounds to signify a good read.

Reader performance can be optimized by selecting the wand appropriate for the environment and the type of symbol being read. The wands offer a 45 degree scan angle, a rugged case, and a sealed sapphire tip. The sapphire tip may be replaced by the user if it is damaged.

Applications

Bar codes offer a method of entering data into computers which is fast, accurate, reliable, and which requires little operator training. Implementation of a bar code system can lead to increased productivity, reduced inventory costs, improved accountability, increased asset visibility, and reduced paperwork. Customer satisfaction will also improve as a result of improved quality control, reduced shipping errors, and reduced order and ship times. On-line, real-time interactive systems will allow the user to take full advantage of the contributions offered by bar code systems. The 16800A and 16801A provide a high performance solution for applications which require on-line bar code data entry.



The most common type of data stored in bar code is item identification information used in a wide range of applications such as:

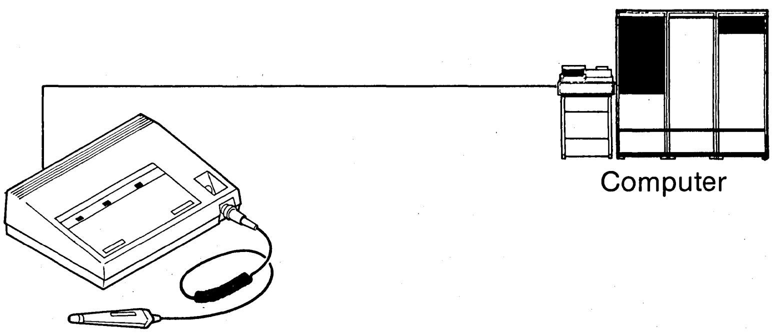
— Inventory Control
— Work-in-Process Tracking
— Distribution Tracking
— Order Processing
— Records Management
— Point-of-Sale
— Government Packaging and Shipping

Bar codes can also be used in applications where information about an item or a transaction must be accurately entered into the host computer. Item location, employee identification, work steps, equipment settings, equipment status, and inspection results are some of the types of information which can be entered using bar codes.

Typical Configuration

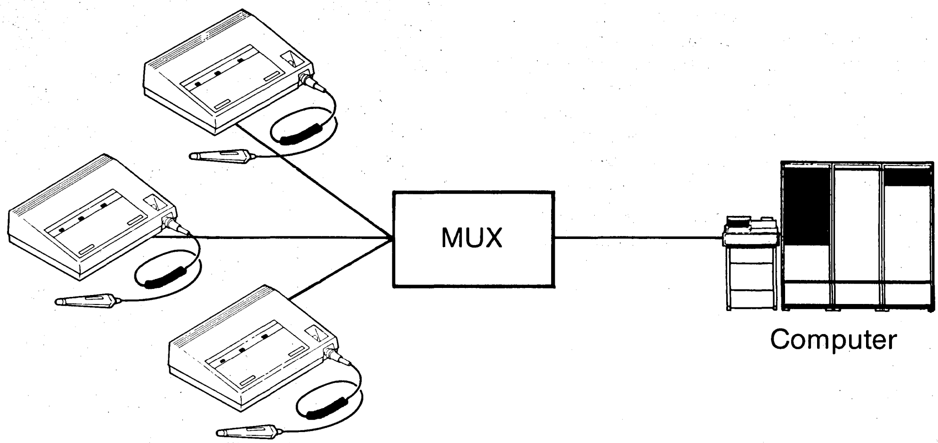
The dual RS-232-C (V.24) output provided by the 16800A and 16801A allows a single reader to be configured in a wide range of on-line applications. Three typical system configurations are outlined below:

- **Stand-Alone Reader** — The 16800A/16801A is in direct communication with the host minicomputer, desktop computer, or personal computer.

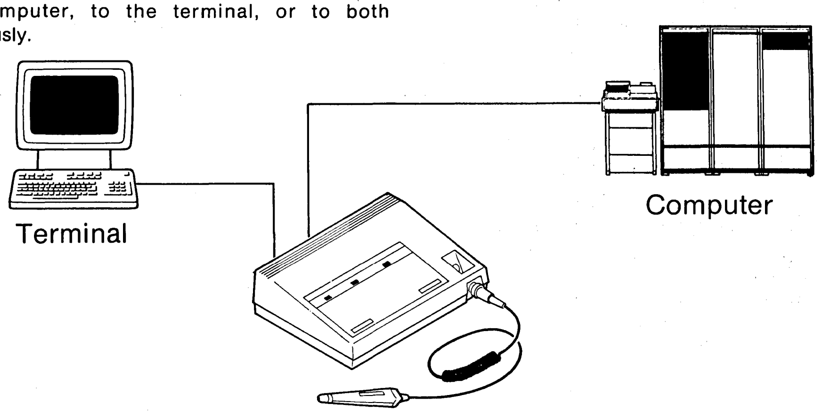


BAR CODE COMPONENTS

- **Multiplexed** — A cluster of 16800A/16801As communicates with the host computer through a multiplexer. Where the advantages of fiber optic data communications are desired, the Hewlett-Packard 39301A Fiber Optic Multiplexer can be used.



- **Eavesdrop** — The 16800A/16801A is in an eavesdrop configuration between an RS-232-C terminal and the host computer. The reader can be configured to transmit to the computer, to the terminal, or to both simultaneously.



Wand Selection

The 16800A and 16801A bar code readers include a 16830A digital bar code wand which is capable of reading bar code symbols which have nominal narrow bar/space widths of 0.19 mm (0.0075 in.) or greater. This includes a wide range of high, medium, and low resolution bar codes including standard 3 of 9 code [0.19 mm (0.0075 in.)].

An optional 16832A digital bar code wand is available for very high resolution codes with nominal narrow bar/space widths of 0.13 mm (0.005 in.) to 0.20 mm (0.008 in.). The 820 nm near-infrared emitter in the 16832A wand also enables it to read the black-on-black bar codes used in some security systems. This wand is not recommended for dot matrix printed bar codes or colored bar codes.

The 16830A and 16832A wands feature a rugged polycarbonate case designed for light industrial and commercial applications. Applications which require an industrial wand are supported by the optional 16840A and 16842A digital bar code wands. These wands feature a solid metal case and internal construction designed for abusive environments. The 16840A and 16842A have the same bar code reading characteristics as the 16830A and 16832A, respectively.

All wands are also available under accessory product numbers.

Code Selection

The 16800A and 16801A offer user flexibility in the implementation of the three standard bar codes:

- Single Code Selection or Automatic Code Recognition (any combination of the three standard codes)
- Checksum Verification Selectable
- Variable Message Length up to 32 characters

- Selectable Message Length Check (Interleaved 2 of 5 code and Industrial 2 of 5 code)
- Any specified code resolution

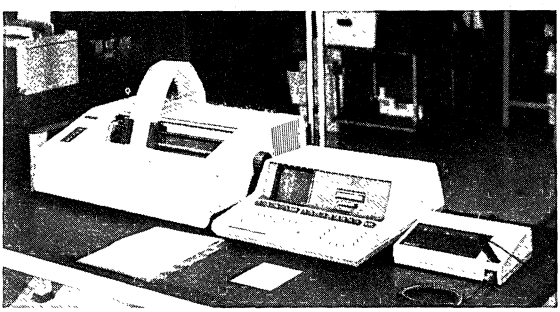
Optional bar codes will also provide a high degree of user flexibility. The code reading configuration is switch selectable. Additional information on bar code symbologies is available in the Operating and Installation Manual and in Application Note 1013 — "Elements of a Bar Code System".

16800A Additional Capabilities
The 16800A offers the advantage of programmable control over all aspects of the code reading configuration. This capability enables the applications software to determine what code can be read depending on the type of data to be entered. For example, the 3 of 9 code could be enabled for entering item identification information and then the 3 of 9 code disabled and Interleaved 2 of 5 code enabled for entering a different type of data such as employee identification or job status. This allows different bar codes to be used in the system while at the same time preventing the operator from entering the wrong type of data into the data base.

Data Communications

The 16800A and 16801A provide a flexible dual RS-232-C (V.24) serial ASCII data communications capability which can support a wide range of system configurations. The reader offers the user the choice of full or half duplex transmission when in character mode and, if in an eavesdrop configuration with a terminal, the reader can also be operated in block mode. The user can tailor the reader's data communication configuration to the application by selecting the appropriate transmission mode (full/half duplex), operating mode (character/block mode), data rate, parity, terminator, stop bits, and inter-character delay on the readily accessible DIP switches. Request to Send/Clear to Send and DC1/DC3 (XON/XOFF) traffic control is available.

16800A Additional Capabilities
The 16800A offers expanded data communications capabilities with the added benefit of programmable control. In addition to programmable control of the transmission mode (full/half duplex) and the operating mode (character/block mode), the 16800A provides the following programmable features:
- User-definable header (up to 10 characters)
- User-definable terminator (up to 10 characters)
- DC1/DC3 (XON/XOFF) traffic control enable/disable



Operator Feedback

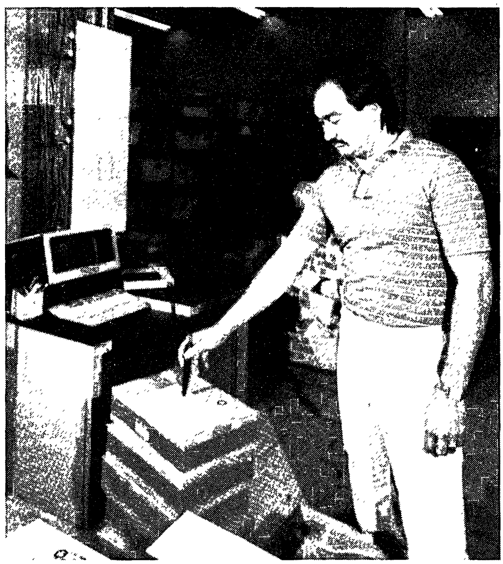
The 16800A and 16801A provide good read feedback to the operator by sounding an integral beeper. Beeper volume can be adjusted as appropriate for the application.

16800A Additional Capabilities
Interactive operator feedback is provided in the 16800A through two programmable LED indicators and programmable beeper control. The user has programmable control over operator feedback as follows:
- Local good read beep enable/disable
- Local good read beep tone (16 tones available)
- Computer commanded beep (16 tones available)
- Red LED Indicator on/off
- Green LED Indicator on/off

Programmable operator feedback can be used to prompt the operator, to signify that data has been validated by the computer, to differentiate between different workstations in close proximity, to provide additional LED feedback in extremely noisy environments, or for a variety of other reasons.

Reader Control and Status (16800A only)

The 16800A provides the user with added programmable control over the reader's operation and also enables the user to obtain on-line status information regarding the reader's configuration and functionality. The programmable control and status features are described below:
Scanner Enable/Disable — When disabled, further bar code scans are ignored.
Single Read Enable/Disable — When enabled, a single bar code scan can be entered between "Next Read" commands.
Hard Reset — Commands the reader to return to the operating configuration prescribed by the DIP switch settings. An automatic self-test is also executed.
Status Request — Commands the reader to send the status of its operating configuration to the computer.



BAR CODE COMPONENTS

Specifications

General

Typical Wand Reading Characteristics:

Parameter	Units	16830A or 16840A	16832A or 16842A
Minimum Recommended Nominal Narrow Element Width	mm in.	0.190 0.0075	0.127 0.005
Tilt Angle	degrees	0-45	0-45
Scan Speed	cm/sec in./sec	7.6-127 3-50	7.6-127 3-50
Wavelength	nm	700	820

Bar Codes Supported:

Standard: 3 of 9 Code (ANSI MH10.8M-1983; MIL-STD-1189)
Interleaved 2 of 5 Code (ANSI MH10.8M-1983)
Industrial 2 of 5 Code

Optional: UPC/EAN/JAN (Option 001)
Codabar (Option 002)
Others (contact factory)

Data Communications

Data Rate:	110, 300, 600, 1200, 2400, 4800, 9600 baud. Switch Selectable.
Parity:	0's, 1's, Odd, Even. Switch Selectable.
Terminator:	CR, CR/LF, Horizontal Tab (HT), None. Switch Selectable.
Programmable Header/ Terminator (16800A only):	User defined. Maximum of 10 characters each.
Stop Bits:	1 or 2. Switch Selectable.
Inter-Character Delay:	30 ms or None. Switch Selectable.
Standard Asynchronous Communications Interface:	EIA Standard RS-232-C (CCITT V.24)
Transmission Modes:	Full or half duplex, asynchronous. Switch selectable. Programmable in 16800A.
Operating Modes:	Character or Block Mode. Switch selectable. Programmable in 16800A.
Traffic Control:	Request to Send/Clear to Send. DC1/DC3 (XON/XOFF). Switch Selectable. Programmable in 16800A.
Output Buffer:	255 Characters

Environmental Conditions

Temperature, Free Space Ambient:

Non-Operating:	-40 to 75° C (-40 to +167° F)
Operating:	0 to +55° C (+32 to 131° F)
Humidity:	5 to 95% (non-condensing)
Altitude: Non-Operating:	Sea level to 15300 metres (50,000 feet)
Operating:	Sea level to 4600 metres (15,000 feet)
Vibration:	0.38 mm (0.015 in.) p-p, 5 to 55 to 5 Hz, 3 axis
Shock:	30g, 11 ms, 1/2 sine

Physical Specifications

Weight, including wand:	2.0 kg (4.4 pounds)
Weight, polycarbonate wand only: (including coiled cord)	0.13 kg (0.3 pounds)
Weight, industrial wand only: (including coiled cord)	0.16 kg (0.4 pounds)
Reader Dimensions:	260 mmW x 189 mmD X 71 mmH (10.25 in.W x 7.4 in.D x 2.8 in.H)
Polycarbonate Wand Dimensions:	134 mmW x 23 mmD x 20 mmH (5.3 in.W x 0.9 in.D x 0.8 in.H)
Industrial Wand Dimensions:	158 mmW x 24 mmD x 18 mmH (6.2 in.W x 0.9 in.D x 0.7 in.H)
Wand Cord Length:	94 cm (37 in.) — retracted 206 cm (81 in.) — extended

Power Requirements

Input Voltage:	100V (+5%, -10%) at 48-66 Hz (Opt. 210) 120V (+5%, -10%) at 48-66 Hz (Standard) 220V (+5%, -10%) at 48-66 Hz (Opt. 222) 240V (+5%, -10%) at 48-66 Hz (Opt. 224)
Power Consumption:	20 VA maximum

Regulatory Agency Approvals

RFI/EMI:
— VDE 0871 level B
— FCC Class B

Safety Approvals:
— UL478, UL114 for EDP and office equipment
— CSA C22.2-154 for EDP equipment
— VDE 0730 part 2P for EDP and office equipment
— Complies with IEC standard #380 and #435 for EDP and office equipment

Installation

All product preparation and installation can be performed by the owner/user. Refer to the Operating and Installation Manual supplied with the unit for detailed instructions.

Supporting Literature

For further information refer to:

16800A/16801A Option 001 Data Sheet, Publication Number 5954-2156 (Available through local sales office)

16800A/16801A Option 002 Data Sheet, Publication Number 5954-2157 (Available through local sales office)

16800A/16801A Operating and Installation Manual, P/N: 16800-90001

16800A/16801A Option 001 Operating and Installation Manual Addendum, P/N: 16800-90004

16800A/16801A Option 002 Operating and Installation Manual Addendum, P/N: 16800-90006

Application Note 1013, "Elements of a Bar Code System", Publication Number: 5953-7732 (Available through local sales office)

Application Bulletin 59, "HP 16800A/16801A Bar Code Reader Configuration Guide for a DEC VT-100 or Lear Siegler ADM-31 to a DEC PDP-11 Computer", Publication Number: 5953-9365 (Available through local sales office)

Application Bulletin 61, "HP 16800A/16801A Bar Code Reader Configuration Guide for an IBM 3276/3278 Terminal", Publication Number: 5953-9361 (Available through local sales office)

Application Bulletin 62, "HP 16800A/16801A Bar Code Reader Configuration Guide for an IBM 4955F Series 1 Process Control CPU/Protocol Converter and an IBM 3101 Terminal", Publication Number: 5953-9362 (Available through local sales office)

Application Bulletin 63, "HP 16800A/16801A Bar Code Reader Configuration Guide for an IBM 5101 Personal Computer", Publication Number: 5953-9363 (Available through local sales office)

Application Bulletin 68, "HP 16800A/16801A Bar Code Reader Configuration Guide for a MICOM Micro 280 Message Concentrator", Publication Number: 5953-9382 (Available through local sales office)

BAR CODE COMPONENTS

Ordering Information

PRODUCT NO.	DESCRIPTION
16800A	PROGRAMMABLE BAR CODE READER — Includes 16830A digital wand, internal power supply for 120V line voltage, power cord, and Operating and Installation Manual. Reader supports 3 of 9 Code, Interleaved 2 of 5 Code, and Industrial 2 of 5 Code.
16801A	BAR CODE READER — Includes 16830A digital wand, internal power supply for 120V line voltage, power cord, and Operating and Installation Manual. Reader supports 3 of 9 Code, Interleaved 2 of 5 Code, and Industrial 2 of 5 Code.
-001	Add UPC/EAN/JAN code reading capability; Delete Industrial 2 of 5 code
-002	Add Codabar code reading capability; Delete Industrial 2 of 5 code
-210	100V power supply
-222	220V power supply
-224	240V power supply
-320	Delete 16830A digital wand; Add 16832A digital wand
-400	Delete 16830A digital wand; Add 16840A industrial digital wand
-420	Delete 16830A digital wand; Add 16842A industrial digital wand
-610	Add Wall Mounting Kit
-910	Additional Operating and Installation Manual
ACCESSORIES	
16830A	General Purpose Digital Bar Code Wand
16832A	High Resolution Digital Bar Code Wand
16840A	Industrial (Metal) General Purpose Bar Code Wand
16842A	Industrial (Metal) High Resolution Bar Code Wand
HBCS-2999	16830A/16832A Replacement Sapphire Tip
HBCS-4999	16840A/16842A Replacement Sapphire Tip
16800-61000	Wall Mount Kit
HEDS-0200	20 foot Wand Extension Cord
03075-40006	External Wand Holder
17355A	2.7 metres (9 feet) Male-Male RS-232-C cable. Shielded.
LITERATURE	
16800-90001	Operating and Installation Manual
16800-90004	Option 001 Operating and Installation Manual Addendum
16800-90006	Option 002 Operating and Installation Manual Addendum

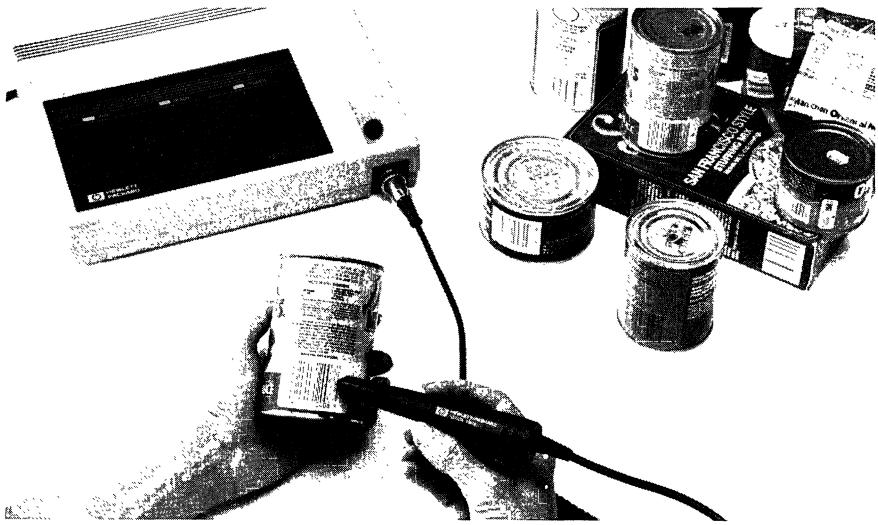
HEWLETT PACKARD

UPC/EAN/JAN BAR CODE READERS

16800A OPTION 001

16801A OPTION 001

TECHNICAL DATA JANUARY 1986



Features

- FLEXIBLE COMMERCIAL CODE READING CAPABILITY
  - UPC-A, UPC-E
  - EAN-8, EAN-13
  - JAN-8, JAN-13
  - 2-Digit Supplemental Encodation
  - 5-Digit Supplemental Encodation
- TWO STANDARD INDUSTRIAL BAR CODES
  - 3 of 9 Code
  - Interleaved 2 of 5 Code
- AUTOMATIC CODE RECOGNITION
- COMPATIBLE WITH UPC SHIPPING CONTAINER SYMBOL SPECIFICATION
- HIGH PERFORMANCE DIGITAL WANDS
  - 45 Degree Scan Angle
  - Replaceable, Sealed, Sapphire Tip
  - Polycarbonate or Metal Case

Description

Option 001 adds bar code reading capability for the Universal Product Code (UPC), European Article Numbering Code (EAN), and Japanese Article Numbering Code (JAN) to the HP 16800A Programmable Bar Code Reader and HP 16801A Non-Programmable Bar Code Reader.

All popular versions of the UPC, EAN and JAN bar codes may be enabled, including UPC-A, UPC-E, EAN-8, EAN-13, JAN-8 and JAN-13. All codes may be read simultaneously, or only UPC-A and UPC-E may be enabled.

UPC, EAN, and JAN codes with complementary 2-digit or 5-digit supplemental encodations, or "add-ons", may be read in one of two ways. If UPC, EAN, and JAN codes are enabled but neither 2-digit nor 5-digit supplemental encodations are enabled, then symbols printed with, or without, supplements can be read and only the main symbol will be output. If 2-digit (or 5-digit) supplemental encodations are enabled, then only symbols with 2-digit (or 5-digit) supplements can be read and both the main symbol and the supplement are output. 2-digit and 5-digit supplemental encodations may be enabled simultaneously.

Two standard industrial codes, the 3 of 9 code and Interleaved 2 of 5 code, may also be read with Option 001. These two codes may be enabled individually, simultaneously, and/or in conjunction with the UPC, EAN, and JAN codes. The implementation of the Interleaved 2 of 5 code is compatible with the UPC Shipping Container Symbol Specification.

Industrial 2 of 5 code reading capability, available with the standard HP 16800A and HP 16801A, is not provided with Option 001.

Applications

Option 001 to the HP 16800A and HP 16801A Bar Code Readers provides an excellent solution for both commercial and industrial applications by supporting the popular UPC, EAN, and JAN codes as well as the industry standard 3 of 9 and Interleaved 2 of 5 codes.

Typical applications for UPC, EAN, and JAN codes include:

- Point-of-sale
- Inventory control in retail stores
- Order entry for retail products
- Tracking periodical and/or book returns
- Tracking coupon receipts
- Production line tracking in consumer products manufacturing plants

The 3 of 9 code and Interleaved 2 of 5 code are commonly used for work-in-process tracking and inventory control applications. Some applications may require that the 3 of 9 code or Interleaved 2 of 5 code be read interchangeably with the UPC, EAN, and/or JAN codes. For example, products which are marked with a UPC code may be shipped in a container marked with the Interleaved 2 of 5 code. The automatic code recognition capability of the HP 16800A and HP 16801A allows these codes to be read interchangeably.

Typical applications for 3 of 9 code and Interleaved 2 of 5 code include:

- Inventory control
- Work-in-process tracking
- Distribution tracking
- Records management
- Government packaging and shipping
- Labor reporting
- Asset management

Wand Selection

The HP 16800A and HP 16801A Bar Code Readers include an HP 16830A digital bar code wand which is capable of reading bar code symbols which have nominal narrow bar/space widths of 0.19 mm (0.0075 in.) or greater. A 700 nm visible red emitter enables the HP 16830A to read a wide variety of colored bar codes. This wand is recommended for reading the UPC, EAN, and JAN bar codes.

An optional HP 16832A digital bar code wand is available for very high resolution codes having nominal narrow bar/space widths of 0.13 mm (0.005 in.) to 0.20 mm (0.008 in.). An 820 nm near-infrared emitter enables the HP 16832A to read black-and-white bar codes and the black-on-black bar codes used in some security systems. It cannot read colored bar codes and, therefore, is not recommended for reading the UPC, EAN, and JAN bar codes.

Applications which require an industrial wand are supported by the optional 16840A and 16842A digital bar code wands. These wands feature a solid metal case and internal construction designed for abusive environments. The 16840A and 16842A have the same bar code reading characteristics as the 16830A and 16832A, respectively.

BAR CODE COMPONENTS

Supporting Literature

For further information, refer to:

16800A/16801A Option 001 Operating and Installation Manual Addendum, P/N: 16800-90004

16800A/16801A Operating and Installation Manual, P/N: 16800-90001

16800A/16801A Data Sheet, Publication No.: 5954-2155

Ordering Information

Product Number	Description
16800A -001	PROGRAMMABLE BAR CODE READER Includes 16830A digital wand, internal power supply for 120 V line voltage, power cord, and Operating and Installation Manuals. Reader supports UPC, EAN, JAN, 3 of 9, and Interleaved 2 of 5 codes.
16801A -001	NON-PROGRAMMABLE BAR CODE READER Includes 16830A digital wand, internal power supply for 120 V line voltage, power cord, and Operating and Installation Manuals. Reader supports UPC, EAN, JAN, 3 of 9, and Interleaved 2 of 5 codes.
-210	100 V power supply
-222	220 V power supply
-224	240 V power supply
-320	Delete 16830A digital wand; add 16832A digital wand
-400	Delete 16830A digital wand; add 16840A industrial digital wand
-420	Delete 16830A digital wand; add 16842A industrial digital wand
-610	Add Wall Mounting Kit
-910	Additional Operating and Installation Manuals

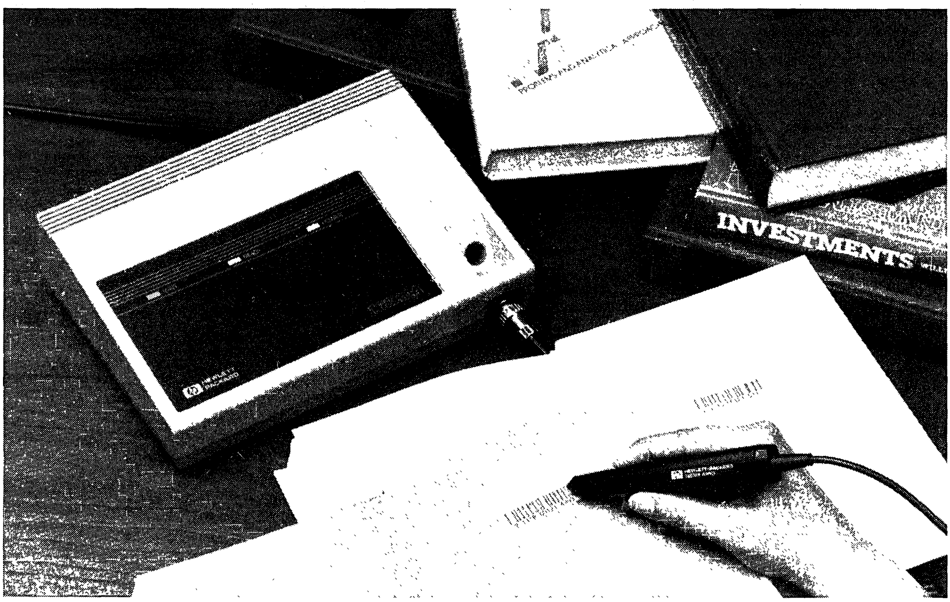
HEWLETT PACKARD

CODABAR BAR CODE READERS

16800A OPTION 002

16801A OPTION 002

TECHNICAL DATA JANUARY 1986



Features

- **CODABAR CODE READING CAPABILITY**
- **TWO STANDARD INDUSTRIAL BAR CODES**
  - **— 3 of 9 Code**
  - **— Interleaved 2 of 5 Code**
- **AUTOMATIC CODE RECOGNITION**
- **HIGH PERFORMANCE DIGITAL WANDS**
  - **— 45 Degree Scan Angle**
  - **— Replaceable, Sealed, Sapphire Tip**
  - **— Polycarbonate or Metal Case**

Description

Option 002 adds bar code reading capability for Codabar to the HP16800A Programmable Bar Code Reader and HP16801A Non-Programmable Bar Code Reader. Transmission of the start and stop characters which are part of each Codabar symbol is user-selectable.

Two standard industrial codes, the 3 of 9 code and Interleaved 2 of 5 code, may also be read with Option 002. These two codes may be enabled individually, simultaneously, and/or in conjunction with the Codabar code.

Industrial 2 of 5 code reading capability, available with the standard HP16800A and HP16801A, is not provided with Option 002.

Applications

Codabar code is commonly used for material tracking, customer identification, and traceability in four specific application areas:

— Libraries
— Hospitals
— Film Processing
— Package Tracking

The 3 of 9 code is also popular in these applications, especially where an alphanumeric code is preferred. In some circumstances, both the 3 of 9 code and Codabar code may need to be read interchangeably. This capability is provided by the automatic code recognition feature of the HP16800A and HP16801A.

The 3 of 9 code and Interleaved 2 of 5 code are generally preferred in industrial applications and in applications which involve interfacility or intercompany movement of goods. These applications include:

— Inventory control
— Work-in-process tracking
— Distribution tracking
— Records management
— Government packaging and shipping
— Labor reporting
— Asset management

Wand Selection

The HP16800A and HP16801A Bar Code Readers include an HP16830A digital bar code wand which is capable of reading bar code symbols which have nominal narrow bar/space widths of 0.19 mm (0.0075 in.) or greater. This wand is recommended for reading all low resolution bar codes, such as those produced with dot matrix printers, and for reading high resolution 3 of 9 and Interleaved 2 of 5 bar codes. It may also be used to read most high resolution Codabar symbols.

An optional HP16832A digital bar code wand is available for very high resolution codes having nominal narrow bar/space widths of 0.13 mm (0.005 in.) to 0.20 mm (0.008 in.). This wand may provide superior performance when reading high resolution Codabar symbols since this code has a nominal narrow bar width of 0.17 mm (0.0065 in.). An 820 nm near-infrared emitter enables the HP 16832A to read black-and-white bar codes and the black-on-black bar codes used in some security systems.

Applications which require an industrial wand are supported by the optional 16840A and 16842A digital bar code wands. These wands feature a solid metal case and internal construction designed for abusive environments. The 16840A and 16842A have the same bar code reading characteristics of the 16830A and 16832A, respectively.

Supporting Literature

For further information refer to:

16800A/16801A Option 002 Operating and Installation Manual Addendum, P/N: 16800-90006

16800A/16801A Operating and Installation Manual, P/N: 16800-90001

16800A/16801A Data Sheet, Publication No: 5954-2155

Ordering Information

Product Number	Description
16800A	Programmable Bar Code Reader
-002	Includes 16830A digital wand, internal power supply for 120V line voltage, power cord, and Operating and Installation Manuals. Reader supports Codabar, 3 of 9, and Interleaved 2 of 5 codes.
16801A	Non-Programmable Bar Code Reader
-002	Includes 16830A digital wand, internal power supply for 120V line voltage, power cord, and Operating and Installation Manuals. Reader supports Codabar, 3 of 9, and Interleaved 2 of 5 codes.
-210	100V Power Supply
-222	220V Power Supply
-224	240V Power Supply
-320	Delete 16830A Digital Wand; add 16832A Digital Wand
-400	Delete 16830A Digital Wand; add 16840A Industrial Digital Wand
-420	Delete 16830A Digital Wand; add 16842A Industrial Digital Wand
-610	Add Wall Mounting Kit
-910	Additional Operating and Installation Manuals

HEWLETT PACKARD

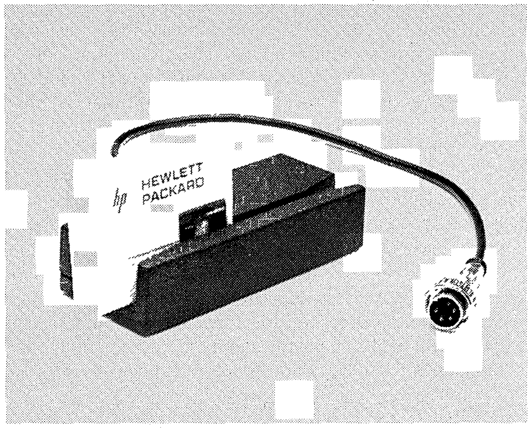
INDUSTRIAL DIGITAL BAR CODE SLOT READERS

HBCS-7000
HBCS-7001
HBCS-7100
HBCS-7101

TECHNICAL DATA JANUARY 1986

Features

- **MINIMAL FIRST BAR DISTORTION**
  — Compatible with Most Decoding Software
- **LARGE SLOT WIDTH**
  — Allows Reading Multiple Laminated Cards
- **SEALED METAL CASE**
  — Can Be Installed Outdoors or in Wet Environments
- **TAMPER PROOF DESIGN**
  — Ideal for Security Applications
- **AVAILABLE IN EITHER VISIBLE 660 nm OR INFRARED 880 nm VERSIONS**
- **WIDE TEMPERATURE RANGE**
  — −40 to 70°C (HBCS-7100)
  — −20 to 55°C (HBCS-7000)
- **WIDE SCAN SPEED RANGE**
- **BLACK TEXTURED EPOXY FINISH**
- **SINGLE 5 VOLT SUPPLY**



Description

Hewlett-Packard's Industrial Digital Slot Readers are designed to provide excellent scanning performance on a wide variety of bar coded cards and badges. They contain a unique optical/electrical system that integrates over a large area of the bar/space pattern, providing a greatly improved first read rate even on poorly printed bar codes.

The HBCS-7000 has a visible red (660 nm) optical system with a resolution of 0.19 mm (0.0075 in.). The HBCS-7100 model has an infrared (880 nm) optical system with a resolution of 0.19 mm (0.0075 in.).

The extra large depth of field allows these slot readers to have a slot width of 3.175 mm (.125 in.), thus making it possible to read even multiple laminated cards and badges. When used as a stand alone optics module, the maximum depth of field is dependent on resolution.

The optics and electronics are housed in a rugged metal case. The cases are fully gasketed and sealed, making them suitable for use in outdoor or wet environments. The black epoxy coating adds a durable, finished look to these Digital Slot Readers. When installed using the rear screw holes, the units become tamper-proof, making them excellent choices for security access control.

The optical system is centered in the slot track, allowing the user to easily scan from either direction. The wide slot width makes it easy to insert and slide the cards. The optical system is covered with a recessed window to prevent contamination and reduce the wear on the cards.

The standard slot reader comes with the optical/electrical assembly mounted on a base plate with an opposite rail. A 104 cm (41 in.) straight cord and a 5 pin, 240 degree, locking DIN connector are also standard.

The optical/electrical system is also available as a separate unit which can be integrated into other equipment or used as a stand alone sensor assembly.

Applications

The digital bar code slot reader is a highly effective alternative to keyboard data entry. Bar code scanning is faster and more accurate than key entry and provides far greater throughput. In addition, bar code scanning typically has a higher first read rate and greater data accuracy than optical character recognition. When compared to magnetic stripe encoding, bar code offers significant advantages in flexibility of media, symbol placement and immunity to electromagnetic fields.

Hewlett-Packard's Industrial Digital Slot Readers are designed for applications where high first read rate and durability are important factors. The epoxy coated metal case, with its tamper-proof mounting system, makes these slot readers ideal choices for security access control, time and attendance recording and other bar coded badge and card reading applications.

Specifications

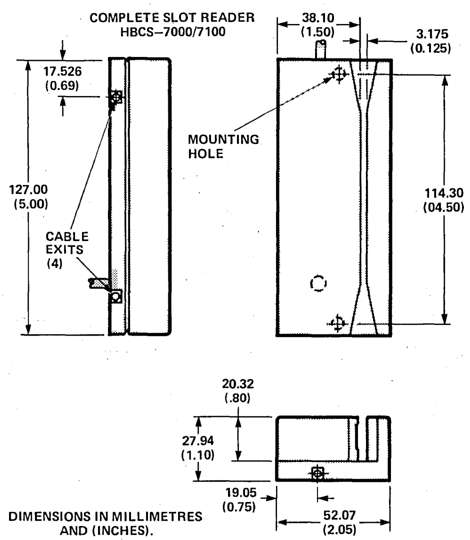
Parameter	Symbol	Min.	Max.	Units	Notes
Nominal Narrow Element Width HBCS-7000/7001		0.19 (0.0075)		mm (in.)	
HBCS-7100/7101		0.19 (0.0075)		mm (in.)	
Scan Velocity	V_{SCAN}		305 (120)	cm/sec (in/sec)	
Contrast	R_W-R_B	45		%	1
Supply Voltage	V_S	4.5	5.5	Volts	2
Temperature HBCS-7000/7001	T_A	−20	+55	°C	3
HBCS-7100/7101	T_A	−40	+70	°C	3
Supply Current	I_S		100	mA	

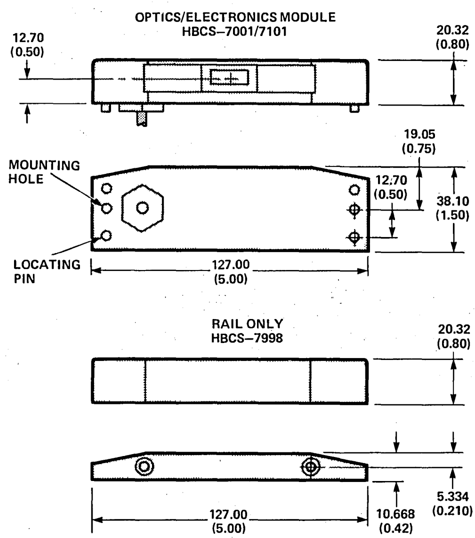
Notes:
1. Contrast is defined as R_W-R_B where R_W is the reflectance of the white spaces and R_B is the reflectance of the black bars, measured at the emitter wavelength (660 nm or 880 nm). Contrast is related to print contrast signal (PCS) by PCS = $(R_W\text{-}R_B)/R_W$ or R_W-R_B = PCS x R_W.
2. Power supply ripple and noise should be less than 100 mV peak to peak.
3. Non-condensing. If there is a frost or dew covering over the optics window, it should be removed for optimal scanning performance.

Selection Guide

Part Number	Description
HBCS-7000	Complete Slot Reader assembly with 660 nM visible red light source and 0.19 mm (0.0075 in.) nominal resolution.
HBCS-7100	Complete Slot Reader assembly with 880 nM infrared light source and 0.19 mm (0.0075 in.) nominal resolution.
HBCS-7001	Optics/electronics module only with 660 nM visible red light source and 0.19 mm (0.0075 in.) nominal resolution.
HBCS-7101	Optics/electonics module only with 880 nM infrared light source and 0.19 mm (0.0075 in.) nominal resolution.
HBCS-7998	Optional side rail assembly for use with HBCS-7001/7101.

Dimensions





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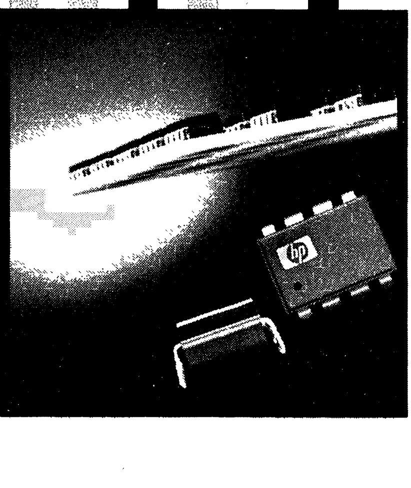
3. Optocouplers



Optocouplers

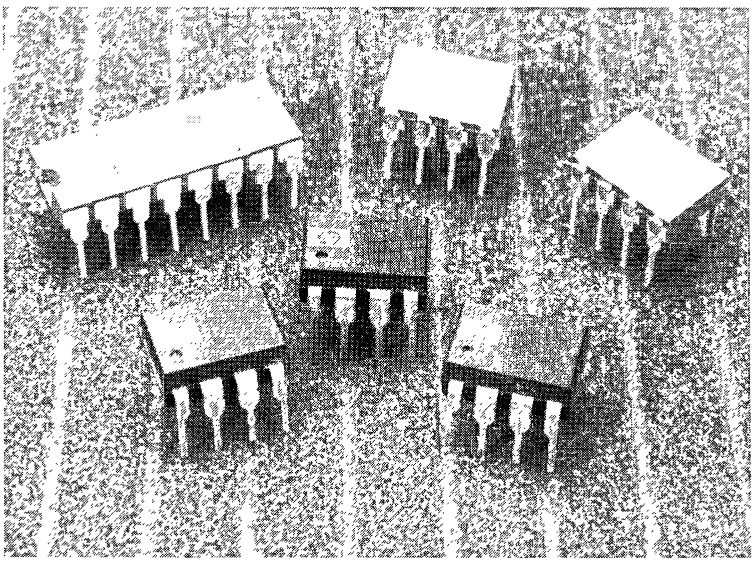
Hewlett-Packard's original approach toward integrated output detectors provides performance not found in conventional phototransistor output devices. A family of optocouplers has been established to provide reliable, economical, high performance solutions to problems caused by ground loops and induced common mode noise for both analog and digital applications in commercial, industrial and military products.

The capabilities of this family span a wide range. Device selections include: programmable AC/DC power sensing input with logic output; speeds up to 40M bits/s; CTR gains as high as 2000% and input currents as low as 0.5 mA. HP's HCPL-2200 features guaranteed propagation delay of 300 ns max. from 0 to 85 degrees C with a wide V_{CC} range from 4.5 V to 20 V and I_{CC} of only 6 mA. Additionally, the high CMR of 1000 V/μs and built-in hysteresis help assure reliable circuit design.

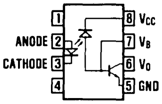
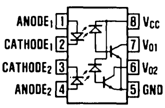
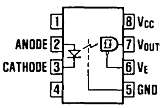
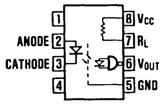
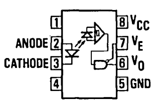
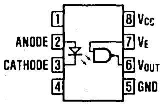
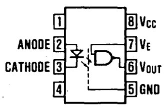
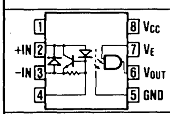
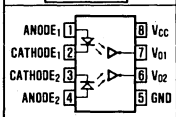
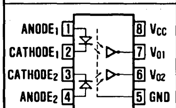
Hewlett-Packard also has available highly linear optocouplers that are useful in analog applications, a unique integrated-input optically coupled line receiver that can be connected directly to twisted pair wires without additional circuitry, and optocouplers that provide complete isolated transmit and receive functions for a 20 mA current loop. Commercial burn-in and screening programs are available for Hewlett-Packard's plastic optocouplers upon special request. See the High Reliability section (page 8-1) for additional details.

Many of these devices are available in dual channel versions as well as in hermetic DIP packages. For military users, Hewlett-Packard's established, and DESC recognized hi-rel capability facilitates economical, hi-rel purchases.

Hewlett-Packard plastic optocouplers are now available for surface mount (see Option 100) applications, and higher insulation voltage (see Option 010) applications. Our newest optocoupler, the HCPL-2400, features a guaranteed data rate of 20 MBaud over temperature. Additionally the HCPL-2400 simplifies high speed design with specifications for pulse width and channel distortion, and power supply noise immunity.



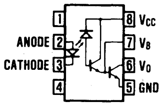
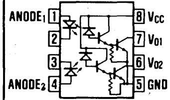
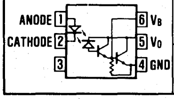
High Speed Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage		Page No.
							Standard*	Option 010**	
	6N135	Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 M bit/s	7% Min.	16 mA	3000 V dc	2500 V ac	3-9
	6N136				19% Min.				
	HCPL-4502	Pin 7 Not Connected							
	HCPL-2502				15-22%				
	SL5505		Telephone circuits, Approved by CNET	1 M bit/s	15% Min. 40% Max.	16 mA	1500 V dc		3-13
	HCPL-2530	Dual Channel Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 M bit/s	7% Min.	16 mA	3000 V dc	2500 V ac	3-15
	HCPL-2531				19% Min.				
	HCPL-2200	Low Input Current Optically Coupled Logic Gate 3 State Output V_{CC} = 20 V Max.	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface	5 M bit/s	4 TTL Loads	1.6 mA	3000 V dc	2500 V ac	3-19
	HCPL-2300	Low Input Current, High Speed Opto-Coupler	High Speed, Long Distance Line Receiver, Computer Peripheral Interfaces, CMOS Logic Interface	8 M bit/s	5 TTL Loads	0.5 mA	3000 V dc	2500 V ac	3-23
	HCPL-2400	20 MBaud, High Common Mode Rejection, Optically Coupled Logic Gate 3 State Output	High Speed Logic Isolation, A/D and Parallel/Serial Conversion, Communications, Networks, Computers	40 M bit/s	5 TTL Loads	5.0 mA	3000 V dc	2500 V ac	3-29
	6N137	Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation	10 M bit/s	8 TTL Loads	5.0 mA	3000 V dc	2500 V ac	3-35
	HCPL-2601	High Common Mode Rejection, Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation in High Ground or Induced Noise Environments	10 M bit/s	8 TTL Loads	5.0 mA	3000 V dc	2500 V ac	3-39
	HCPL-2602	Optically Coupled Line Receiver	Replace Conventional Line Receivers in High Ground or Induced Noise Environments	10 M bit/s	8 TTL Loads	5.0 mA	3000 V dc	2500 V ac	3-43
	HCPL-2630	Dual Channel Optically Coupled Gate	Line Receiver, High Speed Logic Ground Isolation	10 M bit/s	8 TTL Loads	5.0 mA	3000 V dc	2500 V ac	3-49
	HCPL-2631	Dual Channel, High Common Mode Rejection, Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation in High Ground or Induced Noise Environments	10 M bit/s	8 TTL Loads	5.0 mA	3000 V dc	2500 V ac	3-53

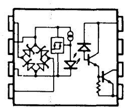
*Standard Parts meet the UL1440 V ac test for 1 minute.

**Option 010 parts meet the UL 2500 V ac test for 1 minute.

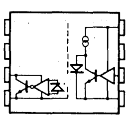
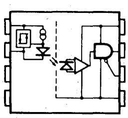
High Gain Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage		Page No.
							Standard*	Option 010**	
	6N138	Low Saturation Voltage, High Gain Output, V_{CC} = 7 V Max.	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	100k bit/s	300% Min.	1.6 mA	3000 V dc	2500 V ac	3-57
	6N139	Low Saturation Voltage, High Gain Output, V_{CC} = 18 V Max.	Line Receiver, Ultra Low Current Ground Isolation, CMOS/LSTTL, CMOS/TTL, CMOS/CMOS		400% Min.	0.5 mA			
	HCPL-2730	Dual Channel, High Gain, V_{CC} = 7 V Max.	Line Receiver, Polarity Sensing, Low Current Ground Isolation	100k bit/s	300% Min.	1.6 mA	3000 V dc	2500 V ac	3-61
	HCPL-2731	Dual Channel, High Gain, V_{CC} = 18 V Max.			400% Min.	0.5 mA			
	4N45	Darlington Output V_{CC} = 7 V Max.	AC Isolation, Relay-Logic Isolation	3k bit/s	250% Min.	1.0 mA	3000 V dc	2500 V ac	3-65
	4N46	Darlington Output V_{CC} = 20 V Max.			350% Min.	0.5 mA			

AC/DC to Logic Interface Optocoupler

Device		Description	Application[1]	Typical Data Rates	Input Threshold Current	Output Current	Withstand Test Voltage		Page No.
							Standard*	Option 010**	
	HCPL-3700	AC/DC to Logic Threshold Sensing Interface Optocoupler	Limit Switch Sensing, Low Voltage Detector, Relay Contact Monitor	4 KHz	2.5 mA TH+ 1.3 mA TH−	4.2 mA	3000 V dc		3-69

20 mA Current Loop Optocouplers

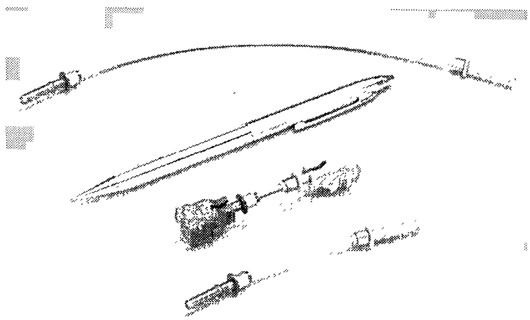
Device		Description	Application[1]	Typical Data Rates	Input Char-acteristics	Output Char-acteristics	Withstand Test Voltage		Page No.
							Standard*	Option 010**	
	HCPL-4100	Optically Coupled 20 mA Current Loop Transmitter	Isolated 20 mA Current Loop in: • Computer Peripherals • Industrial Control Equipment • Data Communication Equipment	20 kBd (at 400 metres)	TTL/CMOS	27 V Max. Compliance Voltage	3000 V dc	2500 V ac	3-75
	HCPL-4200	Optically Coupled 20 mA Current Loop Receiver			6.5 mA Typ. Threshold Current	3 State Output			3-83

*Standard Parts meet the UL1440 V ac test for 1 minute.
**Option 010 parts meet the UL 2500 V ac test for 1 minute.

Optocoupler Options (Do not apply to Hermetic Optocouplers)

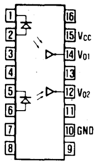
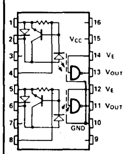
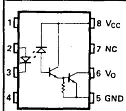
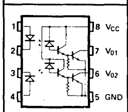
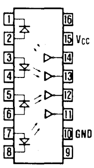
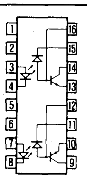
Option	Description
010	Special construction and testing to ensure the capability to withstand 2500 V ac input to output for one minute. Testing is recognized by Underwriters Laboratories, Inc. (File No. E55361). This specification is required by U.L. in some applications where working voltages can exceed 220 V ac.
100	Surface mountable optocoupler in a standard sized dual-in-line package with leads trimmed (butt joint). Provides an optocoupler which is compatible with surface mounting processes.

Very High Voltage Isolation



Hewlett-Packard Low Cost Fiber Optic links provide cost effective isolation of voltages from 10KV to hundreds of KV. TTL compatibility with data rates up to 5 MBd can be attained using the HFBR-1510/2501/3510. See page 6-5, 1986 Catalog for more details or contact your Hewlett-Packard Field Representative.

Hermetic Optocouplers

Device		Description	Application	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N134	Dual Channel Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems	10M bit/s	400% Typ.	10 mA	1500 V dc	8-66
	8102801EC	DESC Approved 6N134	Military/High Reliability					8-69
	6N134TXV	TXV — Screened	Use 8102801EC in New Designs					8-66
	6N134TXVB	TXVB — Screened with Group B Data						
	HCPL-1930	Dual Channel Hermetically sealed High CMR Line Receiver Optocoupler	Line receiver, High Speed Logic Ground Isolation in High Ground or Induced Noise Environments	10M bit/s	400% Typ.	10 mA	1500 Vdc	8-73
	HCPL-1931	MIL-STD-883 Class B Part	Military/High Reliability					
	HCPL-5700	Single Channel Hermetically Sealed High Gain Optocoupler	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	60k bit/s	200% Min.	0.5 mA	500 V dc	8-79
	HCPL-5701	MIL-STD-883 Class B Part	Military/High Reliability					
	HCPL-5730	Dual Channel Hermetically Sealed High Gain Optocoupler	Line Receiver, Polarity Sensing, Low Current Ground Isolation					8-83
	HCPL-5731	MIL-STD-883 Class B Part	Military/High Reliability					
	6N140A (6N140)	Hermetically Sealed Package Containing 4 Low Input Current, High Gain Optocouplers	Line Receiver, Low Power Ground Isolation for High Reliability Systems	100k bit/s	300% Min.	0.5 mA	1500 V dc	8-87
	8302401EC	DESC Approved 6N140A	Military/High Reliability					8-91
	6N140A/883B (6N140/883B)	MIL-STD-883 Class B Part	Use 8302401EC in New Designs					8-87
	6N140TXV	TXV — Hi-Rel Screened						
	6N140TXVB	TXVB — Hi-Rel Screened with Group B Data						
	4N55	Dual Channel Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element	700k bit/s	9% Min.	16 mA	1500 V dc	8-96
	4N55/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	4N55TXV	TXV — Hi-Rel Screened	Use 4N55/883B in New Designs					
	4N55TXVB	TXVB — Hi-Rel Screened with Group B Data						

HEWLETT PACKARD

OPTOCOUPLER OPTION FOR 2500 Vac/ 1 MINUTE REQUIREMENT

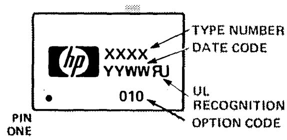
OPTION 010

TECHNICAL DATA JANUARY 1986

Features

- **SPECIAL CONSTRUCTION AND TESTING**
- **UL RECOGNITION FOR 2500 V ac/1 MINUTE REQUIREMENT (FILE NO. E55361)**
- **AVAILABLE FOR ALL PLASTIC OPTOCOUPLERS**
- **480 V ac LINE VOLTAGE RATING**

DEVICE MARKING



Description

Option 010 consists of special construction on a wide range of Hewlett-Packard plastic optocouplers. After assembly, each unit is subjected to an equivalent electrical performance test to insure its capability to withstand 2500 Vac input to output for 1 minute. This test is recognized by Underwriters Laboratory as proof that these components may be used in many high voltage applications.

Applications

The 2500 Vac/1 Minute dielectric withstand voltage is required by Underwriters Laboratory when components are used in certain types of electronic equipment. This requirement also depends on the specific application within the equipment. Some applicable UL documents are listed below.

UL Spec. Number	Specification Title
1577	Standard for Optical Isolators Applications
114	Appliance and Business Equipment
347	High Voltage Industrial Control Equipment
478	Information Processing and Business Equipment
508	Industrial Control Equipment
544	Medical and Dental Equipment
698	Industrial Control Equipment for Use in Hazardous Locations
773	Plug-in, Locking Type Photocontrols
913	Intrinsically Safe Apparatus and Associated Apparatus
916	Standard for Energy Management Equipment
1012	Power Supplies
1244	Electrical and Electronic Measuring and Testing Equipment
1410	Television and Video Products

Specifications

All specifications for optocouplers remain unchanged when this option is ordered. The 2500 Vac/1 Minute capability is validated by a factory 3200 Vac/1 Second dielectric voltage withstand test.

Ordering Information

To obtain this high voltage capability on plastic optocouplers order the standard part number and Option 010.

Examples:

6N135	HCPL-3700
Option 010	Option 010

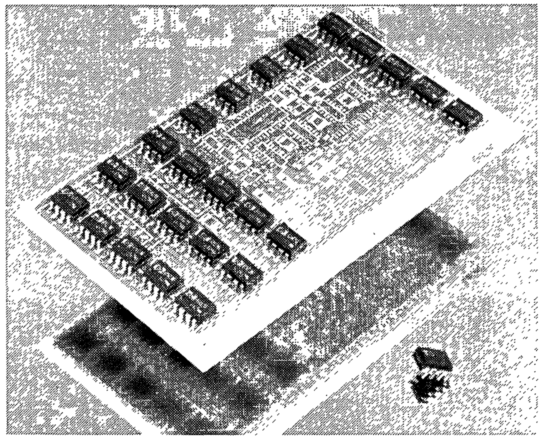
This option is currently available on all standard catalog plastic optocouplers except SL5505.

HEWLETT PACKARD

SURFACE MOUNT OPTION FOR OPTOCOUPLERS

OPTION 100

TECHNICAL DATA JANUARY 1986



Features

- SURFACE MOUNTABLE
  Leads Trimmed for a Butt Joint Connection
- COMPATIBLE WITH VAPOR PHASE REFLOW AND WAVE SOLDERING PROCESSES
- MEETS ALL ELECTRICAL SPECIFICATIONS OF CORRESPONDING STANDARD PART NUMBERS
- LEAD COPLANARITY WITHIN 0.004 INCHES
- AVAILABLE FOR ALL OPTOCOUPLERS IN PLASTIC PACKAGES
- AVAILABLE IN STANDARD SHIPPING TUBES

Description

Option 100 is an optocoupler in a standard sized dual-in-line package, with trimmed leads (butt joint). The distance from the printed circuit board (PCB), to the bottom of the optocoupler package, will be typically 0.035 inches. The height of the optocoupler package is typically 0.150 inches, leaving a distance of 0.185 inches from PCB to the top of the optocoupler package.

Applications

Option 100 enables electronic component assemblers to include HP optocouplers on a PCB that utilizes surface-mount assembly processes. Option 100 does not require "through holes" in a PCB. This reduces board costs, while potentially increasing assembly rates and increasing component density per board.

Specifications

All electrical specifications for optocouplers remain unchanged when this option is ordered. In addition, the device will withstand typical vapor phase reflow soldering conditions of 215°C for 30 seconds, and wave solder immersion for 5 seconds, @ 260°C.

Ordering Information

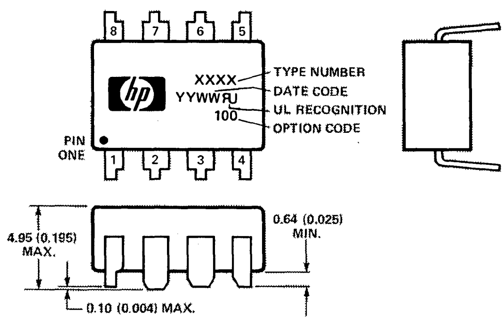
Option 100 is available for all optocouplers in plastic packages.

To obtain surface-mountable optocouplers, order the standard part number and Option 100.

Examples:

6N136	HCPL-2200
Option 100	Option 100

OPTION 100 DRAWING



DIMENSIONS IN MILLIMETRES (INCHES)

Note: For complete dimensions, refer to outline drawing of corresponding catalog part number.

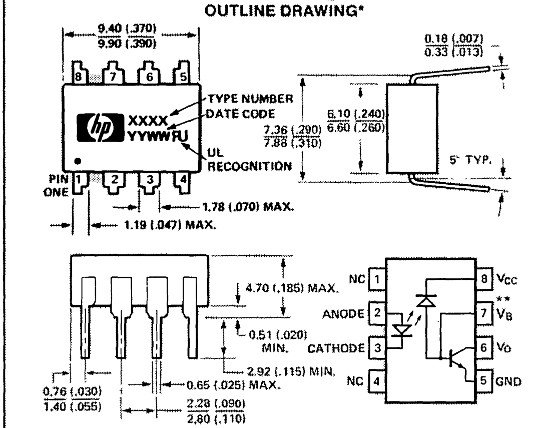
HEWLETT PACKARD

HIGH SPEED OPTOCOUPLERS

6N135
6N136
HCPL-2502
HCPL-4502

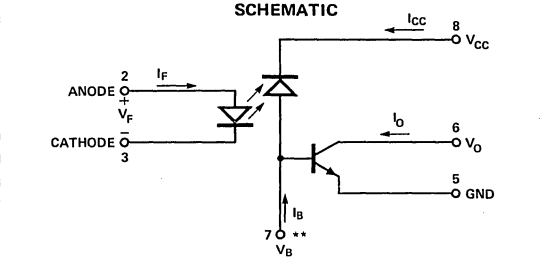
TECHNICAL DATA JANUARY 1986

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

SCHEMATIC



**Note: For HCPL-4502, pin 7 is not connected.

Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: >1000V/μs TYPICAL**
- **2 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUT**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).**

Description

These diode-transistor optocouplers use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collector increases the speed up to a hundred times that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The 6N135 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the 6N135 is 7% minimum at $I_F = 16$ mA.

The 6N136 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the 6N136 is 19% minimum at $I_F = 16$ mA.

The HCPL-2502 is suitable for use in applications where matched or known CTR is desired. CTR is 15 to 22% at $I_F = 16$ mA.

The HCPL-4502 provides the electrical and switching performance of the 6N136 and increased ESD protection.

*JEDEC Registered Data (The HCPL-2502 and HCPL-4502 are not registered.)

Applications

- **Line Receivers** — High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** — TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** — Pins 2-7 of the 6N135/6 series conform to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5V to 30V for high speed operation.
- **Replace Pulse Transformers** — Save board space and weight.
- **Analog Signal Ground Isolation** — Integrated photon detector provides improved linearity over phototransistor type.

Absolute Maximum Ratings

Storage Temperature*	−55°C to +125°C
Operating Temperature*	−55°C to 100°C
Lead Solder Temperature*	260°C for 10s (1.6mm below seating plane)
Average Input Current — I_F*	25mA[1]
Peak Input Current — I_F*	50mA[2] (50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F*	1.0A (≤1μs pulse width, 300pps)
Reverse Input Voltage — V_R* (Pin 3-2)	5V
Input Power Dissipation*	45mW[3]
Average Output Current — I_O* (Pin 6)	8mA
Peak Output Current*	16mA
Emitter-Base Reverse Voltage* (Pin 5-7, except −4502)	5V
Output Voltage* — V_O (Pin 6-5)	−0.5V to 15V
Supply Voltage* — V_O (Pin 6-5)	−0.5V to 15V
Output Voltage — V_O (Pin 6-5)	−0.5V to 20V
Supply Voltage — V_{CC} (Pin 8-5)	−0.5V to 30V
Base Current — I_B* (Pin 7, except HCPL-4502)	5mA
Output Power Dissipation*	100mW[4]

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

See notes, following page.

Electrical Specifications Over recommended temperature (T_A = 0° C to 70° C) unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N135	7	18		%	I_F = 16mA, V_O = 0.4V, V_{CC} = 4.5V T_A = 25° C	1,2,4	5,12
		6N136 HCPL-4502	19	24		%			
		HCPL-2502	15	18	22	%			
	CTR	6N135	5	19		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		5
		6N136 HCPL-4502	15	25		%			
Logic Low Output Voltage	V_{OL}	6N135		0.1	0.4	V	I_F = 16 mA, I_O = 1.1mA, V_{CC} = 4.5V, T_A = 25° C		
		6N136 HCPL-2502 HCPL-4502		0.1	0.4	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V, T_A = 25° C		
Logic High Output Current	I_{OH}*			3	500	nA	I_F = 0mA, V_O = V_{CC} = 5.5V T_A = 25° C	6	
				0.01	1	μA	I_F = 0mA, V_O = V_{CC} = 15V T_A = 25° C		
	I_{OH}				50	μA	I_F = 0mA, V_O = V_{CC} = 15V		
Logic Low Supply Current	I_{CCL}			50		μA	I_F = 16mA, V_O = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}*			0.02	1	μA	I_F = 0mA, V_O = Open, V_{CC} = 15V T_A = 25° C		
	I_{CCH}				2	μA	I_F = 0mA, V_O = Open, V_{CC} = 15V		
Input Forward Voltage	V_F*			1.5	1.7	V	I_F = 16mA, T_A = 25° C	3	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10μA, T_A = 25° C		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation	I_{I-O}*				1	μA	45% RH, t = 5s, V_{I-O} = 3kV dc, T_A = 25° C		6, 11
OPT. 010	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min.		13
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		6
Transistor DC Current Gain	h_{FE}			150		—	V_O = 5V, I_O = 3mA		

*For JEDEC registered parts. **All typicals at T_A = 25° C

Switching Specifications at $T_A = 25°C$ V_{CC} = 5V, I_F = 16mA, unless otherwise specified

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}*	6N135		0.2	1.5	μs	R_L = 4.1kΩ	5,9	8,9
		6N136 HCPL-2502 HCPL-4502		0.2	0.8	μs	R_L = 1.9kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}*	6N135		1.3	1.5	μs	R_L = 4.1kΩ	5,9	8,9
		6N136 HCPL-2502 HCPL-4502		0.3	0.8	μs	R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	6N135		1000		V/μs	I_F = 0mA, V_{CM} = 10 V_{p-p}, R_L = 4.1kΩ	10	7,8,9
		6N136 HCPL-2502 HCPL-4502		1000		V/μs	I_F = 0 m, V_{CM} = 10 V_{p-p}, R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	6N135		1000		V/μs	V_{CM} = 10V_{p-p}, R_L = 4.1kΩ	10	7,8,9
		6N136 HCPL-2502 HCPL-4502		1000		V/μs	V_{CM} = 10V_{p-p}, R_L = 1.9kΩ		
Bandwidth	BW			2		MHz	R_L = 100Ω	8	10

NOTES:
1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70° C free-air temperature at a rate of 2.0mW/°C.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
8. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and the 5.6kΩ pull-up resistor.
9. The 4.1kΩ load represents 1 LSTTL unit load of 0.36mA and 6.1kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3dB below the low frequency asymptote.
11. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
12. The JEDEC registration for the 6N136 specifies a minimum CTR of 15%. HP guarantees a minimum CTR of 19%.
13. See Option 010 data sheet for more information.

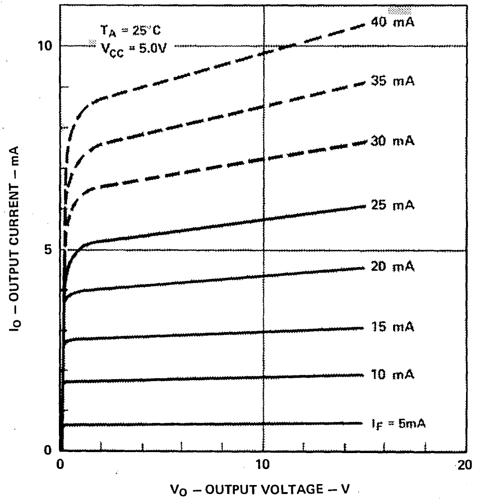


Figure 1. DC and Pulsed Transfer Characteristics.

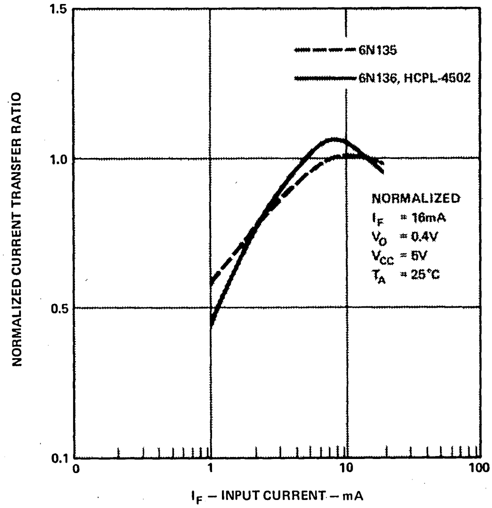


Figure 2. Current Transfer Ratio vs. Input Current.

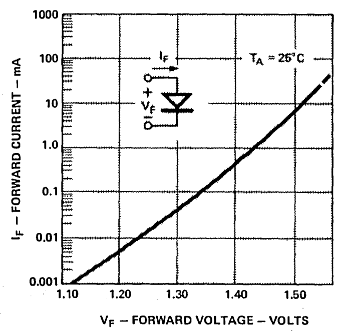


Figure 3. Input Current vs. Forward Voltage.

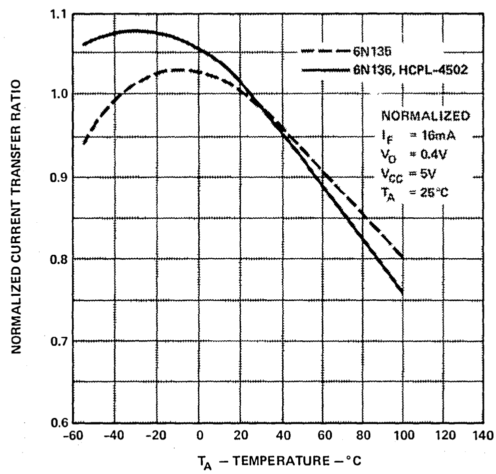


Figure 4. Current Transfer Ratio vs. Temperature.

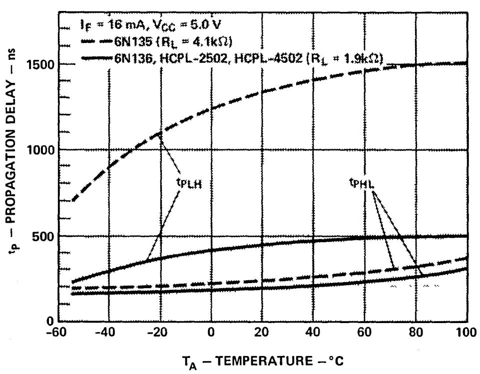


Figure 5. Propagation Delay vs. Temperature.

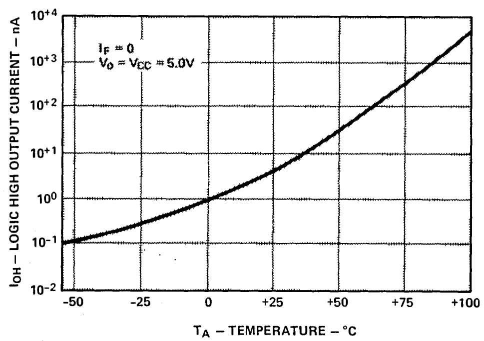


Figure 6. Logic High Output Current vs. Temperature.

OPTOCOUPLERS

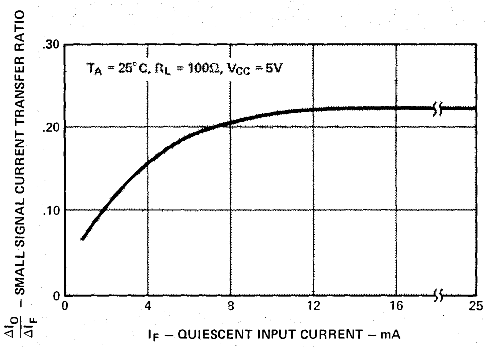


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

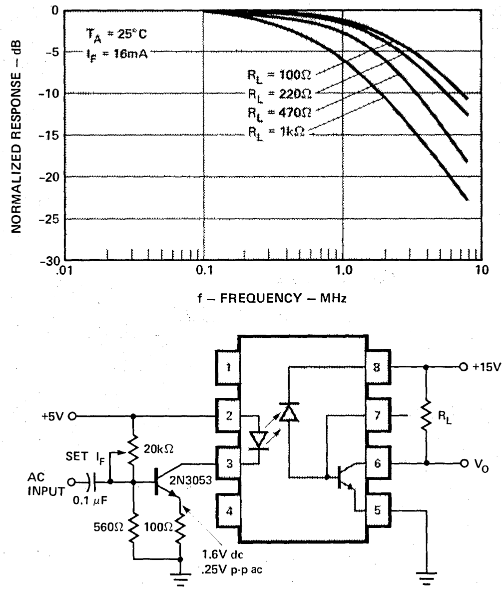


Figure 8. Frequency Response.

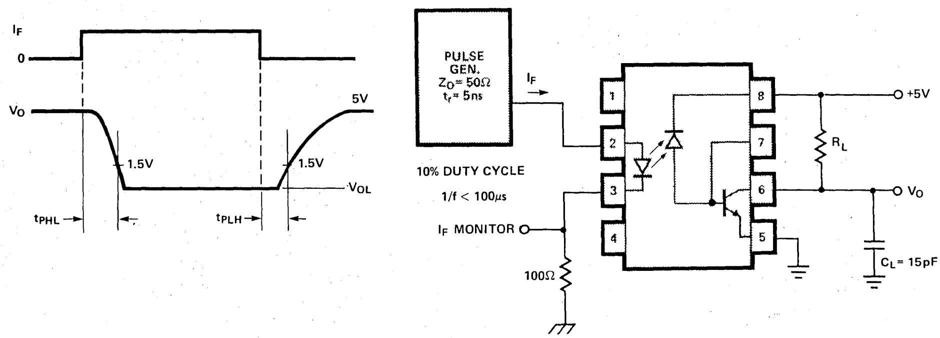
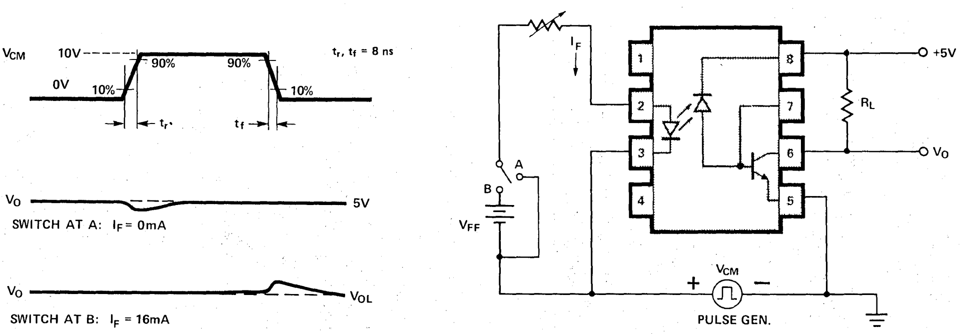


Figure 9. Switching Test Circuit. *



*JEDEC Registered Data

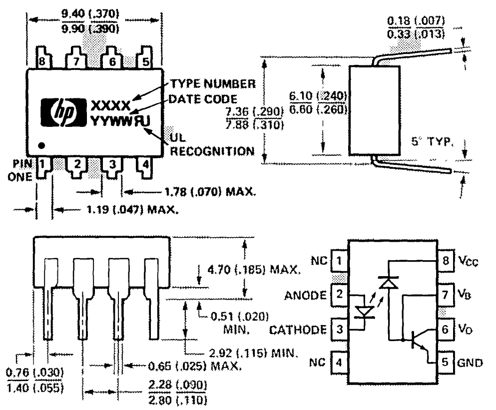
Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

HIGH SPEED OPTOCOUPLER

SL5505

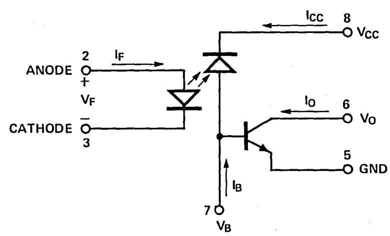
TECHNICAL DATA JANUARY 1986

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

SCHEMATIC



Absolute Maximum Ratings

Storage Temperature .... -55°C to +125°C
Operating Temperature .... -55°C to 100°C
Lead Solder Temperature .... 260°C for 10s (1.6mm below seating plane)
Average Input Current — I_F .... 25mA[1]
Peak Input Current — I_F .... 50mA[2] (50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F .... 1.0A ($\leq 1\mu s$ pulse width, 300pps)
Reverse Input Voltage — V_R (Pin 3-2) 3V
Input Power Dissipation .... 45mW[3]
Average Output Current — I_O (Pin 6) 8mA
Peak Output Current 16mA
Emitter-Base Reverse Voltage (Pin 5-7) 5V
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 6-5) .... -0.5V to 15V
Base Current — I_B (Pin 7) 5mA
Output Power Dissipation .... 100mW[4]

Electrical Specifications ($T_A = 25°C$) unless otherwise specified.

Parameter	Symbol	Min.	Max.	Units	Test Conditions	Note
Current Transfer Ratio	CTR	15	40	%	$I_F = 16mA$, $V_O = 0.4V$, $V_{CC} = 4.5V$	5
	CTR	8		%	$I_F = 2mA$, $V_O = 5.0V$, $V_{CC} = 4.5V$	
Logic Low Output Voltage	V_{OL}		0.4	V	$I_F = 16mA$, $I_O = 2.4mA$, $V_{CC} = 4.5V$	
Logic High Output Current	I_{OH}		50	nA	$I_F = 0mA$, $V_O = V_{CC} = 10V$	
	I_{OH}		25	μA	$I_F = 0mA$, $V_O = V_{CC} = 10V$, $T_A = 70°C$	
Input Forward Voltage	V_F		1.8	V	$I_F = 20mA$	
Input Reverse Current	I_R		50	μA	$V_R = 3V$	
Input-Output Insulation Leakage Current	I_{I-O}		1.0	μA	45% Relative Humidity, t = 5s $V_{I-O} = 1500Vdc$	6
Resistance (Input-Output)	R_{I-O}	10^9		Ω	$V_{I-O} = 100Vdc$	6
Transistor DC Current Gain	h_{FE}	100	400	—	$V_O = 5V$, $I_O = 3mA$	
Capacitance	C_{I-O}		1.3	pF	f = 1 MHz	6

Switching Specifications at T_A=25°C

V_{CC} = 5V, I_F = 16mA, unless otherwise specified

Parameter	Symbol	Min.	Max.	Units	Test Conditions	Note
Propagation Delay Time to Logic Low at Output (Fig. 1)	t_{PHL}		0.8	μs	R_L = 1.9kΩ	7
Propagation Delay Time to Logic High at Output (Fig. 1)	t_{PLH}		0.8	μs	R_L = 1.9kΩ	7
Breakdown Voltage Collector/Emitter	$V_{(BR)}$ CEO	22		V	I_C = 10mA	8
Breakdown Voltage Collector/Base	$V_{(BR)}$ CBO	40		V	I_C = 10μA	
Breakdown Voltage Emitter/Base	$V_{(BR)}$ EBO	3		V	I_E = 10μA	
Collector/Base Current	I_{CBO}		50	nA	V_{CB} = 22V	

Notes:
1. Derate linearly above 70° C free-air temperature at a rate of 0.8mA/ °C.
2. Derate linearly above 70° C free-air temperature at a rate of 1.6mA/ °C.
3. Derate linearly above 70° C free-air temperature at a rate of 0.9mW/° C.
4. Derate linearly above 70° C free-air temperature at a rate of 2.0mW/° C.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. The 1.9 KΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 KΩ pull-up resistor.
8. Duty Cycle ≤ 2%, Pulse Width ≤ 300 μs.

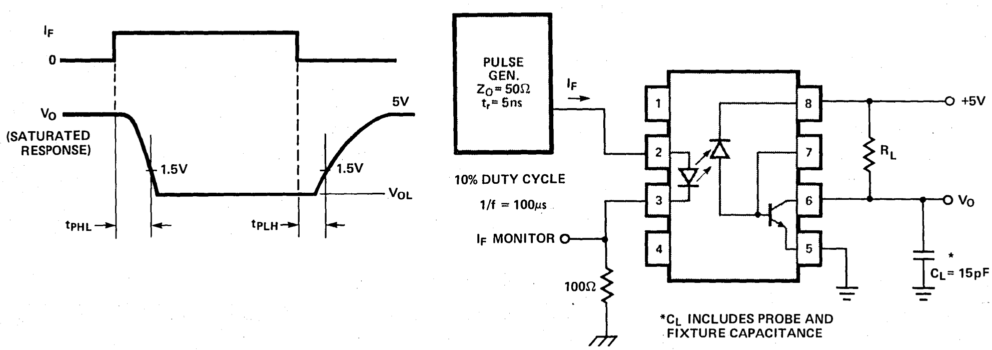


Figure 1. Switching Test Circuit.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

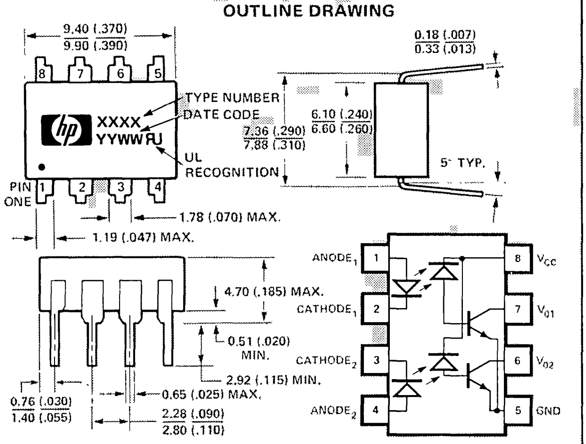
HEWLETT PACKARD

DUAL HIGH SPEED OPTOCOUPLER

HCPL-2530
HCPL-2531

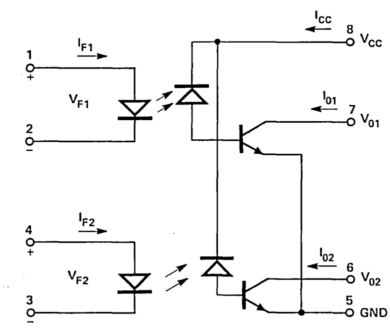
TECHNICAL DATA JANUARY 1986

OUTLINE DRAWING



DIMENSIONS IN MILLIMETERS AND (INCHES)

SCHEMATIC



Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: > 1000V/μs TYPICAL**
- **HIGH DENSITY PACKAGING**
- **3 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUTS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).**

Description

The HCPL-2530/31 dual couplers contain a pair of light emitting diodes and integrated photon detectors with electical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

The HCPL-2530 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the -2530 is 7% minimum at $I_F = 16$ mA.

The HCPL-2531 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output curent for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the -2531 is 19% minimum at $I_F = 16$ mA.

Applications

- **Line Receivers** — High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** — TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Pulse Transformers** — Save board space and weight.
- **Analog Signal Ground Isolation** — Integrated photon detector provides improved linearity over phototransistor type.
- **Polarity Sensing.**
- **Isolated Analog Amplifier** — Dual channel packaging enhances thermal tracking.

Absolute Maximum Ratings

Storage Temperature . . . . -55°C to +125°C
Operating Temperature . . . . -55°C to +100°C
Lead Solder Temperature . . . . 260°C for 10s
(1.6mm below seating plane)
Average Input Current — I_F (each channel) . . . . . . 25mA[1]
Peak Input Current — I_F (each channel) . . . . 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F (each channel) . . . . 1.0 A
(≤1μs pulse width, 300pps)
Reverse Input Voltage — V_R (each channel) 5V
Input Power Dissipation (each channel) . . . . 45mW[3]
Average Output Current — I_O (each channel) 8mA
Peak Output Current — I_O (each channel) 16mA
Supply Voltage - V_{CC} (Pin 8-5) . . . . - 0.5V to 30V
Output Voltage - V_O (Pin 7,6-5) . . . . - 0.5V to 20V
Output Power Dissipation (each channel) . . . . . . 35mW[4]

See notes, following page.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device HCPL-	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2530	7	18		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V T_A = 25°C	1,2	5,6
		2531	19	24		%			
		2530	5			%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
		2531	15			%			
Logic Low Output Voltage	V_{OL}	2530		0.1	0.5	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V, T_A = 25°C		5
		2531		0.1	0.5	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V, T_A = 25°C		
Logic High Output Current	I_{OH}			3	500	nA	T_A = 25°C, I_{F1} = I_{F2} = 0, V_{O1} = V_{O2} = V_{CC} = 5.5V	6	5
					50	µA	I_{F1} = I_{F2} = 0, V_{O1} = V_{O2} = V_{CC} = 15V		5
Logic Low Supply Current	I_{CCL}			100		µA	I_{F1} = I_{F2} = 16mA V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_{F1} = I_{F2} = 0mA V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Input Forward Voltage	V_F			1.5	1.7	V	I_F = 16mA, T_A = 25°C	3	5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16mA		5
Input Reverse Breakdown Voltage	V_R		5			V	I_F = 10µA, T_A = 25°C		5
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		5
Input-Output Insulation	$I_{I\text{-}O}$*				1	µA	45% RH, t = 5s, $V_{I\text{-}O}$ = 3kV dc, T_A = 25°C		7, 13
OPT. 010	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min.		14
Resistance (Input-Output)	$R_{I\text{-}O}$			10^{12}		Ω	$V_{I\text{-}O}$ = 500Vdc		7
Capacitance (Input-Output)	$C_{I\text{-}O}$			0.6		pF	f = 1MHz		7
Input-Input Insulation Leakage Current	$I_{I\text{-}I}$			0.005		µA	45% Relative Humidity, t = 5 s $V_{I\text{-}I}$ = 500Vdc		8
Resistance (Input-Input)	$R_{I\text{-}I}$			10^{11}		Ω	$V_{I\text{-}I}$ = 500Vdc		8
Capacitance (Input-Input)	$C_{I\text{-}I}$			0.25		pF	f = 1MHz		8

*For JEDEC registered parts.

**All typicals at 25°C.

Switching Specifications at T_A=25°C V_{CC} = 5V, I_F = 16mA, unless otherwise specified

Parameter	Sym.	Device HCPL-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	2530		0.2	1.5	µs	R_L = 4.1kΩ	5,9	10,11
		2531		0.2	0.8	µs	R_L = 1.9kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}	2530		1.3	1.5	µs	R_L = 4.1kΩ	5,9	10,11
		2531		0.3	0.8	µs	R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	2530		1000		V/µs	I_F = 0mA, R_L = 4.1kΩ, V_{CM} = 10$V_{p\text{-}p}$	10	9,10,11
		2531		1000		V/µs	I_F = 0mA, R_L = 1.9kΩ, V_{CM} = 10$V_{p\text{-}p}$		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	2530		1000		V/µs	V_{CM} = 10$V_{p\text{-}p}$, R_L = 4.1kΩ	10	9,10,11
		2531		1000		V/µs	V_{CM} = 10$V_{p\text{-}p}$, R_L = 1.9kΩ		
Bandwidth	BW			3		MHz	R_L = 100Ω	8	12

NOTES:
1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 1.0mW/°C.
5. Each channel.
6. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
10. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and the 5.6kΩ pull-up resistor.
11. The 4.1kΩ load represents 1 LSTTL unit load of 0.36mA and 6.1kΩ pull-up resistor.
12. The frequency at which the ac output voltage is 3dB below the low frequency asymptote.
13. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
14. See Option 010 data sheet for more information.

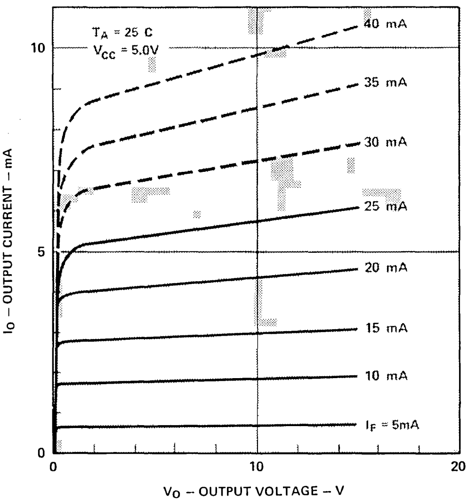


Figure 1. DC and Pulsed Transfer Characteristics.

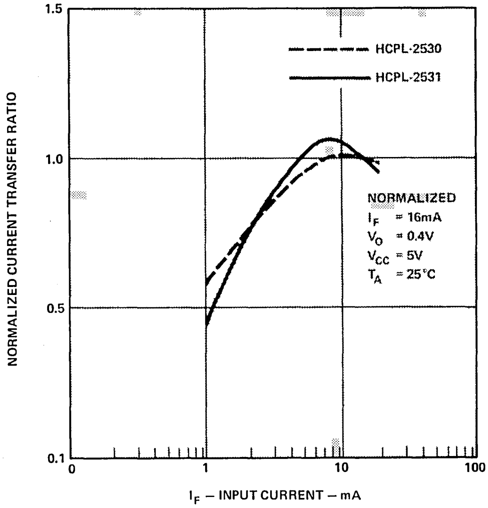


Figure 2. Current Transfer Ratio vs. Input Current.

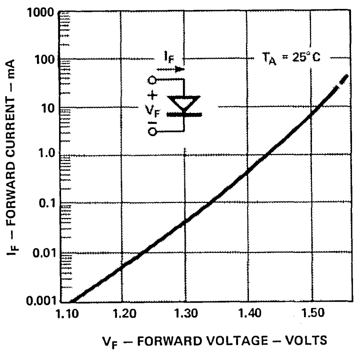
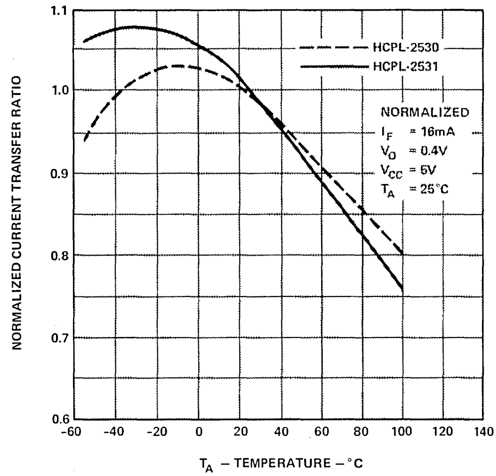


Figure 3. Input Current vs. Forward Voltage.



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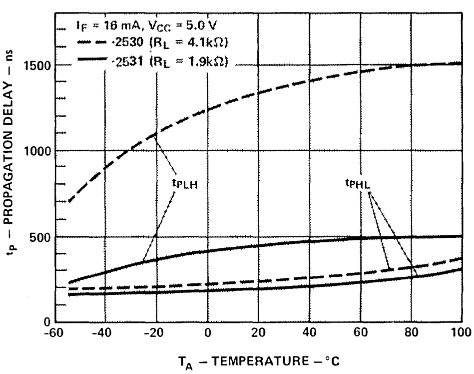


Figure 5. Propagation Delay vs. Temperature.

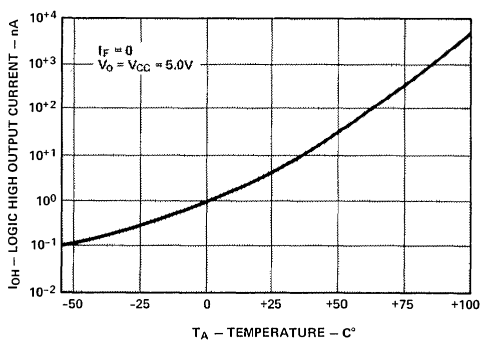


Figure 6. Logic High Output Current vs. Temperature.

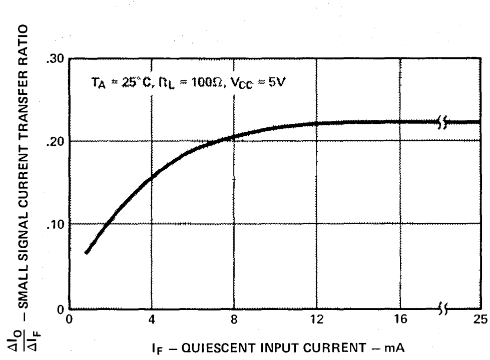


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

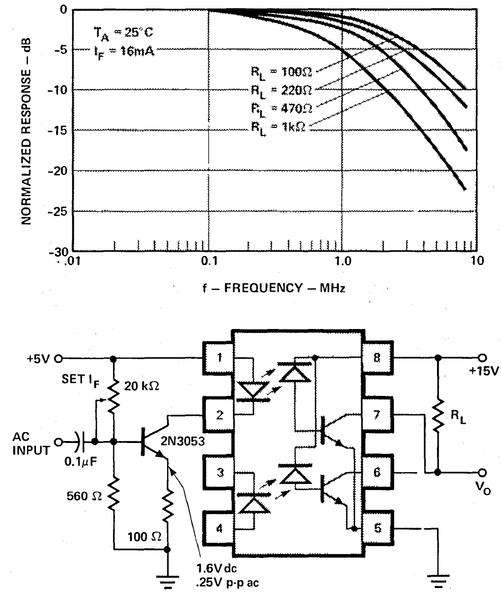


Figure 8. Frequency Response.

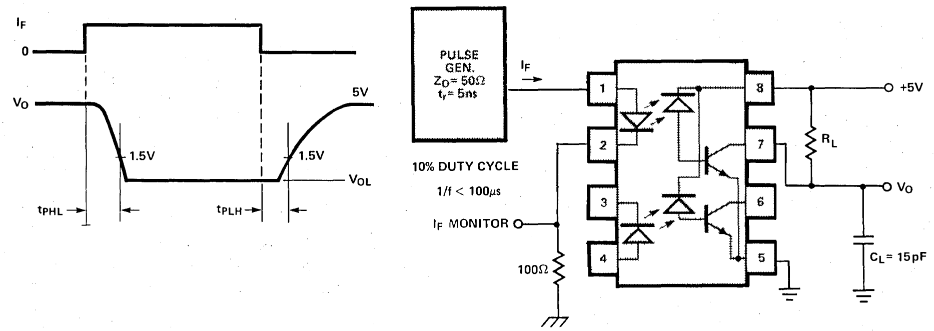


Figure 9. Switching Test Circuit.

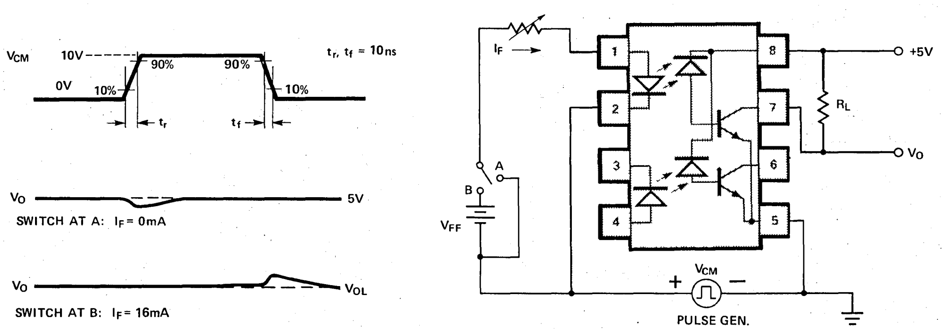


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

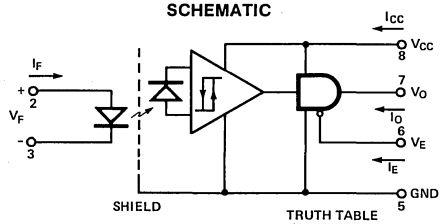
HEWLETT PACKARD

LOW INPUT CURRENT LOGIC GATE OPTOCOUPLER

HCPL-2200

TECHNICAL DATA JANUARY 1986

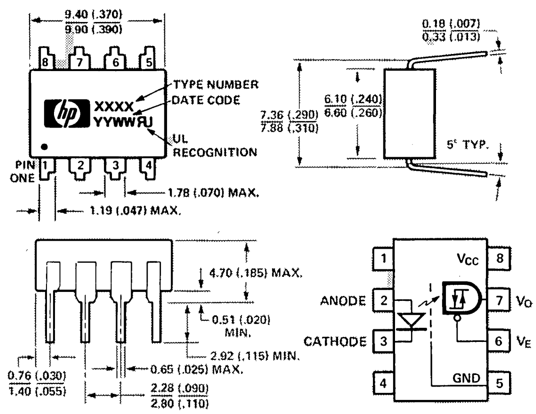
SCHEMATIC



TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	Z
L	H	Z
H	L	H
L	L	L

OUTLINE DRAWING



DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- COMPATIBLE WITH LSTTL, TTL, AND CMOS LOGIC
- 2.5 MBAUD GUARANTEED OVER TEMPERATURE
- LOW INPUT CURRENT (1.6 mA)
- WIDE V_{CC} RANGE (4.5 TO 20 VOLTS)
- THREE STATE OUTPUT (NO PULLUP RESISTOR REQUIRED)
- GUARANTEED PERFORMANCE FROM 0° C TO +85° C
- INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Applications

- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Microprocessor System Interfaces
- Ground Loop Elimination
- Pulse Transformer Replacement
- Isolated Buss Driver
- High Speed Line Receiver

Description

The HCPL-2200 is an optically coupled logic gate that combines a GaAsP LED and an integrated high gain photon detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides typically 0.1 mA of differential mode noise immunity and eliminates the potential for output signal chatter. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1,000 volts/μsec. Higher CMR specifications are available upon request. Improved power supply rejection eliminates the need for special power supply bypassing precautions.

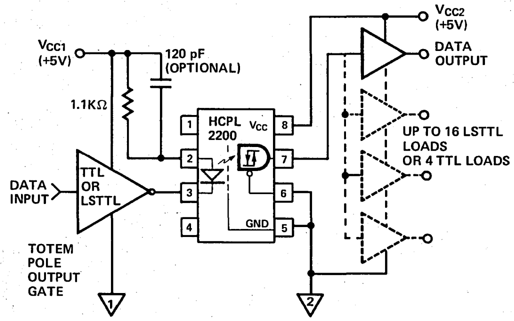
The Electrical and Switching Characteristics of the HCPL-2200 are guaranteed over the temperature range of 0° C to 85° C. The HCPL-2200 is guaranteed to operate over a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic. Low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 160 nsec when a 120 pF peaking capacitor is used in parallel with the 1.1KΩ current limiting resistor.

The HCPL-2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Enable Voltage High	V_{EH}	2.0	20	Volts
Enable Voltage Low	V_{EL}	0	0.8	Volts
Forward Input Current	$I_{F(ON)}$	1.6	5	mA
Forward Input Current	$I_{F(OFF)}$	—	0.1	mA
Operating Temperature	T_A	0	85[1]	°C
Fan Out	N		4	TTL Loads

Recommended Circuit Design



The 120 pF capacitor may be omitted in applications where 500 ns propagation delay is sufficient.

Figure 1. Recommended LSTTL to LSTTL Circuit

Absolute Maximum Ratings

(No Derating Required up to 70° C)

Storage Temperature .... -55° C to +125° C
Operating Temperature .... -40° C to +85° C[1]
Lead Solder Temperature .... 260° C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current — I_F .... 10 mA
Peak Transient Input Current — I_F 1A
(≤1 µs Pulse Width, 300 pps)
Reverse Input Voltage 5V
Supply Voltage — V_{CC} .... 0.0V min., 20V max.
Three State Enable Voltage
— V_E .... -0.5V min., 20V max.
Output Voltage — V_O .... -0.5V min., 20V max.
Total Package Power
Dissipation — P .... 210 mW[1]
Average Output Current — I_O .... 25 mA

Electrical Characteristics

For 0° C ≤ T_A[1] ≤ 85° C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 2.0 V ≤ V_{EH} ≤ 20 V, 0.0 V ≤ V_{EL} ≤ 0.8 V, 0 mA ≤ $I_{F(OFF)}$ ≤ 0.1 mA. All Typicals at T_A = 25° C, V_{CC} = 5V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2	
Logic High Output Voltage	V_{OH}	2.4	*		Volts	I_{OH} = -2.6 mA	*$V_{OH} = V_{CC} - 2.1V$	3	
Output Leakage Current ($V_{OUT} > V_{CC}$)	I_{OHH}			100	µA	V_O = 5.5V	I_F = 5 mA		
				500	µA	V_O = 20V	V_{CC} = 4.5V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	µA	V_{EN} = 2.7V			
				100	µA	V_{EN} = 5.5V			
			.004	250	µA	V_{EN} = 20V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_{EN} = 0.4V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5V	I_F = 0 mA		
			5.25	7.5	mA	V_{CC} = 20V	V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5V	I_F = 5 mA,		
			3.1	6.0	mA	V_{CC} = 20V	V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			-20	µA	V_O = 0.4V	V_{EN} = 2V, I_F = 5 mA		
	I_{OZH}			20	µA	V_O = 2.4V	V_{EN} = 2V, I_F = 0		
				100	µA	V_O = 5.5V			
				500	µA	V_O = 20V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	$V_O = V_{CC}$ = 5.5V	I_F = 0 mA		2
		40			mA	$V_O = V_{CC}$ = 20V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5V	I_F = 5 mA, V_O = GND		2
		-25			mA	V_{CC} = 20V			
Input Current Hysteresis	I_{HYS}		0.12		mA	V_{CC} = 5V		4	
Input Forward Voltage	V_F		1.5	1.70	Volts	I_F = 5 mA, T_A = 25° C		5	
Input Reverse Breakdown Voltage	V_R	5			Volts	I_R = 10 µA at T_A = 25° C			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/° C	I_F = 5 mA			
Input-Output Insulation	I_{I-O}*			1	µA	45% RH, t = 5s, V_{I-O}=3kV dc, T_A=25° C			3, 7
OPT. 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min.			8
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		90		pF	f = 1 MHz, V_F = 0V, Pins 2 and 3			

*For JEDEC registered parts.

Switching Characteristics

For 0°C ≤ T_A[1] ≤ 85°C, 4.5V ≤ V_{CC} ≤ 20V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 0.0 mA ≤ $I_{F(OFF)}$ ≤ 0.1 mA. All Typicals at T_A = 25°C, V_{CC} = 5V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		210		ns	Without Peaking Capacitor	6,7	4,5
			160	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		170		ns	Without Peaking Capacitor	6,7	4,5
			115	300		With Peaking Capacitor		
Output Enable Time to Logic High	t_{PZH}		25		ns		8,10	
Output Enable Time to Logic Low	t_{PZL}		28		ns		8,9	
Output Disable Time from Logic High	t_{PHZ}		105		ns		8,10	
Output Disable Time from Logic Low	t_{PLZ}		60		ns		8,9	
Output Rise Time (10-90%)	t_r		55		ns		6,11	
Output Fall Time (90-10%)	t_f		15		ns		6,11	
Logic High Common Mode Transient Immunity	$\|CM_H\|$	1000	10,000		V/µs	T_A = 25°C, I_F = 1.6 mA, V_{CM} = 50 V	12,13	6
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	1000	10,000		V/µs	T_A = 25°C, I_F = 0, V_{CM} = 50 V	12,13	6

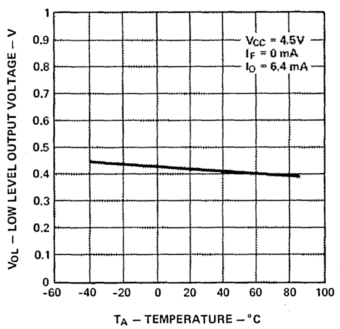


Figure 2. Typical Logic Low Output Voltage vs. Temperature

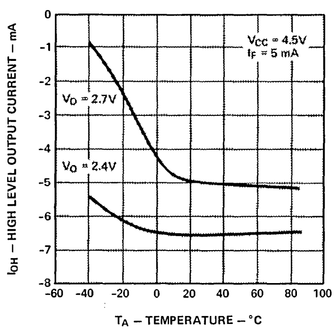


Figure 3. Typical Logic High Output Current vs. Temperature

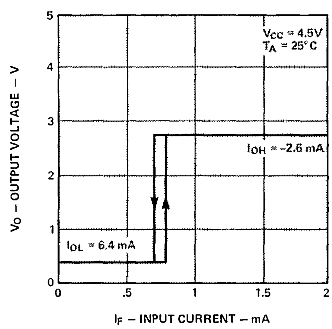


Figure 4. Output Voltage vs. Forward Input Current

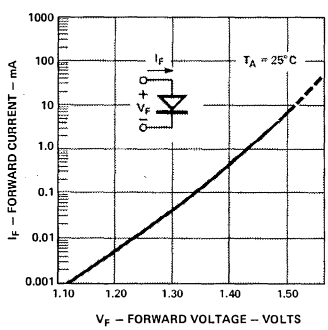


Figure 5. Typical Input Diode Forward Characteristic

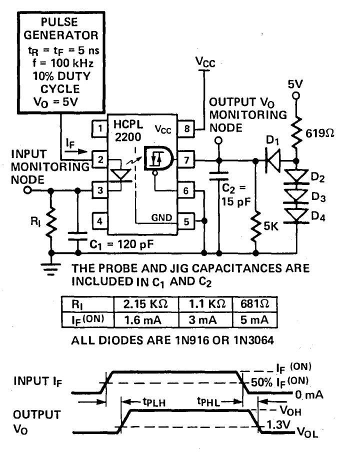


Figure 6. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

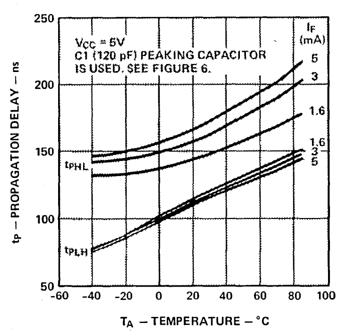


Figure 7. Typical Propagation Delays vs. Temperature

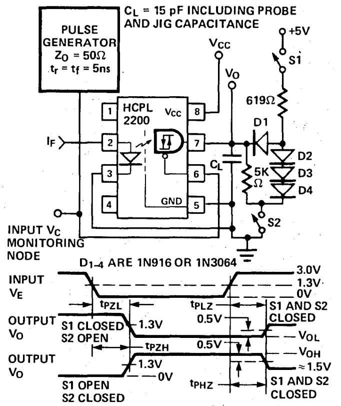


Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

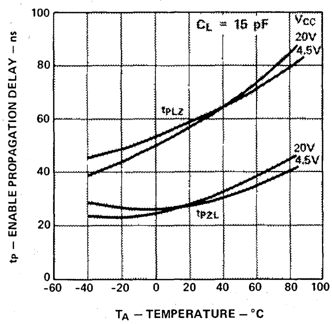


Figure 9. Typical Logic Low Enable Propagation Delay vs. Temperature

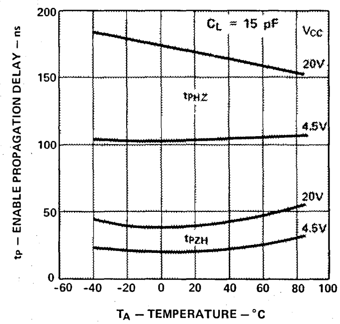


Figure 10. Typical Logic High Enable Propagation Delay vs. Temperature

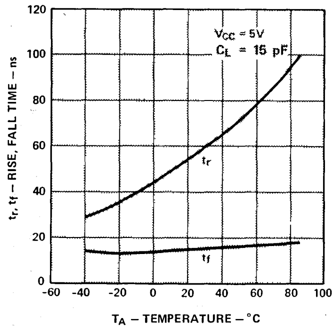


Figure 11. Typical Rise, Fall Time vs. Temperature

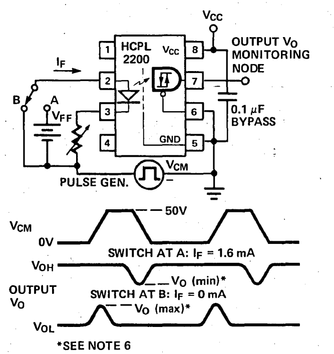


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

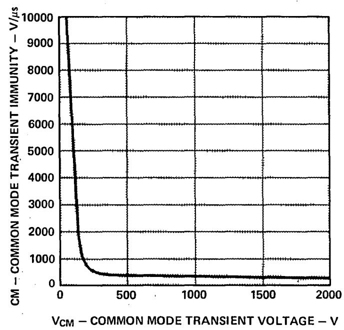


Figure 13. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude

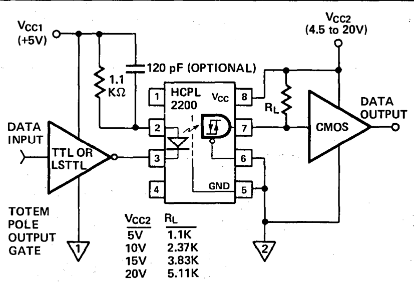


Figure 14. LSTTL to CMOS Interface Circuit

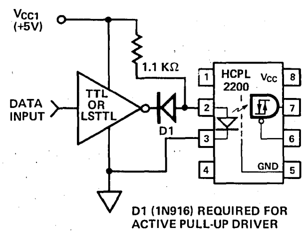


Figure 15. Recommended LED Drive Circuit

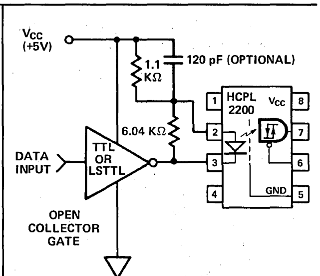


Figure 16. Series LED Drive with Open Collector Gate (6.04 KΩ Resistor Shunts I_{OH} from the LED)

The 120 pF capacitor may be omitted in applications where 500 ns propagation delay is sufficient.

Notes:

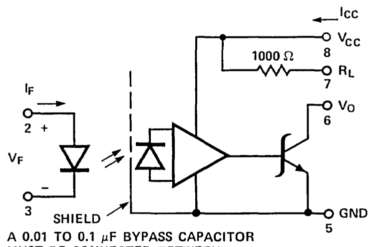
1. Derate total package power dissipation, P, linearly above 70°C free air temperature at a rate of 4.5 mW/°C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.
5. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8V$). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0V$).
7. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
8. See Option 010 data sheet for more information.

HEWLETT PACKARD

LOW INPUT CURRENT HIGH SPEED OPTOCOUPLER

HCPL-2300

TECHNICAL DATA JANUARY 1986



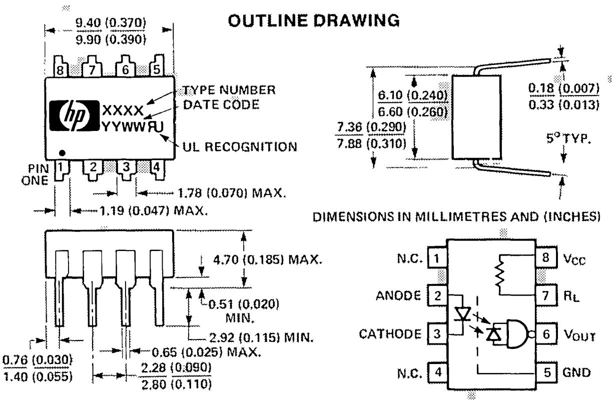
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5. (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

INPUT	OUTPUT
H	L
L	H

Figure 1. Schematic

OUTLINE DRAWING



DIMENSIONS IN MILLIMETRES AND (INCHES)

Features

- GUARANTEED LOW THRESHOLDS: $I_F = 0.5$ mA, $V_F \leq 1.5$ V
- HIGH SPEED: GUARANTEED 5 MBd OVER TEMPERATURE
- VERSATILE: COMPATIBLE WITH TTL, LSTTL AND CMOS
- MORE EFFICIENT 820 nm AlGaAs IRED
- INTERNAL SHIELD FOR GUARANTEED COMMON MODE REJECTION
- SCHOTTKY CLAMPED, OPEN COLLECTOR OUTPUT WITH OPTIONAL INTEGRATED PULL-UP RESISTOR
- STATIC AND DYNAMIC PERFORMANCE GUARANTEED FROM -40°C to 85°C
- SPECIAL SELECTION FOR LOW FORWARD CURRENT APPLICATIONS ($I_F \geq 150$ μA)
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Applications

- GROUND LOOP ELIMINATION
- COMPUTER-PERIPHERAL INTERFACES
- LEVEL SHIFTING
- MICROPROCESSOR SYSTEM INTERFACES
- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- RS-232-C INTERFACE
- HIGH SPEED, LONG DISTANCE ISOLATED LINE RECEIVER

Description

The HCPL-2300 optocoupler combines an 820 nm AlGaAs photon emitting diode with an integrated high gain photon detector. This combination of Hewlett-Packard designed and manufactured semiconductor devices brings high performance capabilities to designers of isloted logic and data communication circuits.

The low current, high speed AlGaAs emitter manufactured with a unique diffused junction, has the virtue of fast rise and fall ties at low drive currents. The HCPL-2300 has a typical propagation delay of 120 ns at 0.5 mA forward current. With special selection, the device can achieve 80 ns propagation delay at 150 μA. Figure 6 illustrates the propagation delay vs. input current characteristic. These unique characteristics enable this device to be used in an RS-232-C interface with ground loop isolation and improved common mode rejection. As a line receiver, the HCPL-2300 will operate over longer line lengths for a given data rate because of lower I_F and V_F specifications.

The output of the shielded integrated detector circuit is an open collector Schottky clamped transistor. The shield, which shunts capacitively coupled common mode noise to ground, provides a guaranteed transient immunity specification of 100 V/μs. The output circuit includes an optional integrated 1000 Ohm pull-up resistor for the open collector. This gives designers the flexibility to use the internal resistor for pull-up to five volt logic or to use an external resistor for 18 volt CMOS logic.

The Electrical and Switching Characteristics of the HCPL-2300 are guaranteed over a temperature range of -40°C to 85°C. This data sheet will allow users of the HCPL-2300 to confidently implement all necessary static and dynamic performance requirements which may be subjected to a broad range of operating environments.

Recommended Operating Conditions

		Sym.	Min.	Max.	Units
Input Voltage, Low Level		V_{FL}	-2.5	0.8	V
Input Current High Level	0° C to 85° C	I_{FH}	0.5	1.0	mA
	-40° C to 85° C		0.5	0.75	
Supply Voltage, Output		V_{CC}	4.75	5.25	V
Fan Out (TTL Load)		N		5	
Operating Temperature		T_A	-40	85	°C

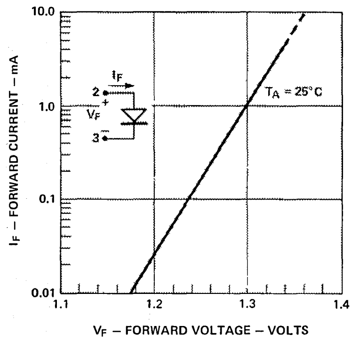


Figure 2. Typical Input Diode Forward Characteristic.

Absolute Maximum Ratings

(No derating required)

Parameter	Symbol	Min.	Max.	Units	Reference
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Solder Temperature	260° C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		5	mA	See Note 2
Reverse Input Voltage	V_R		4.5	V	
Supply Voltage	V_{CC}	0.0	7.0	V	
Pull-up Resistor Voltage	V_{RL}	-0.5	V_{CC}	V	
Output Collector Current	I_O	-25	25	mA	
Input Power Dissipation	P_I		10	mW	
Output Collector Power Dissipation	P_O		40	mW	
Output Collector Voltage	V_O	-0.5	18	V	

Electrical Characteristics

For -40° C ≤ T_A ≤ 85° C, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified.
All typicals at T_A = 25° C, V_{CC} = 5 V, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		0.05	250	μA	V_F = 0.8 V, V_O = 18 V	4	
				10		V_F = 0.8 V, V_O = 18 V, T_A = 25° C		
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_F = 0.5 mA I_{OL} (Sinking) = 8 mA	3	
High Level Supply Current	I_{CCH}		4.0	6.3	mA	I_F = 0 mA, V_{CC} = 5.25 V		
Low Level Supply Current	I_{CCL}		6.2	10.0	mA	I_F = 1.0 mA, V_{CC} = 5.25 V		
Input Forward Voltage	V_F	1.0	1.3	1.5	V	I_F = 1.0 mA, T_A = 25° C	2	
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 1.0 mA		
Input Reverse Breakdown Voltage	BV_R	4.5			V	I_R = 10 μA, T_A = 25° C		
Input Capacitance	C_{IN}		18		pF	V_F = 0 V, f = 1 MHz		
Input-Output Insulation	I_{I-O}*			1	μA	45% RH, t = 5s, V_{I-O} = 3 kV dc, T_A = 25° C		3, 9
OPT 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50% t = 1 MIN		10
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3
Internal Pull-up Resistor	R_L	680	1000	1700	Ohms			

*For JEDEC registered parts.

Switching Characteristics

For -40° C ≤ T_A ≤ 85° C, 0.5 mA ≤ I_{FH} ≤ 0.75 mA;
For 0° C ≤ T_A ≤ 85° C, 0.5 mA ≤ I_{FH} ≤ 1.0 mA; With 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified.
All typicals at T_A = 25° C, V_{CC} = 5 V, I_{FH} = 0.625 mA, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		95		ns	C_P = 0 pF	5, 6, 8	4, 8
			85	160		C_P = 20 pF	5, 8	
Propagation Delay Time to Logic Low Output Level	t_{PHL}		110		ns	C_P = 0 pF	5, 6, 8	5, 8
			35	200		C_P = 20 pF	5, 8	
Output Rise Time (10-90%)	t_r		40		ns	C_P = 20 pF	7, 8	8
Output Fall Time (90-10%)	t_f		20		ns			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	100	400		V/μs	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 560Ω, I_F = 0 mA	9, 10	6
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	100	400		V/μs	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 560Ω, I_F = 0.5 mA	9, 10	7

(See page 5-35 for Notes)

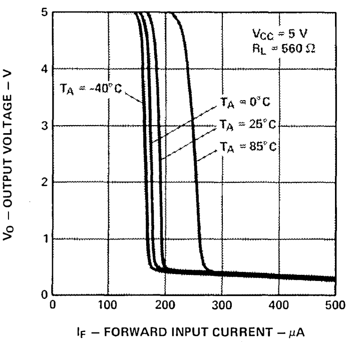


Figure 3. Typical Output Voltage vs. Forward Input Current vs. Temperature.

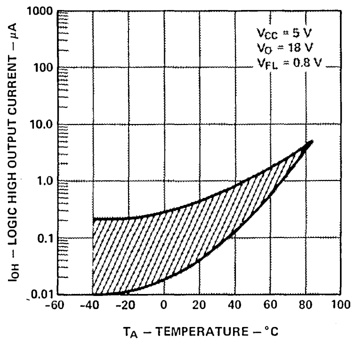


Figure 4. Typical Logic High Output Current vs. Temperature.

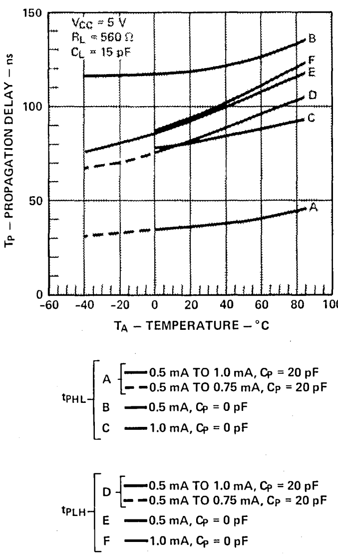


Figure 5. Typical Propagation Delay vs. Temperature and Forward Current With and Without Application of a Peaking Capacitor.

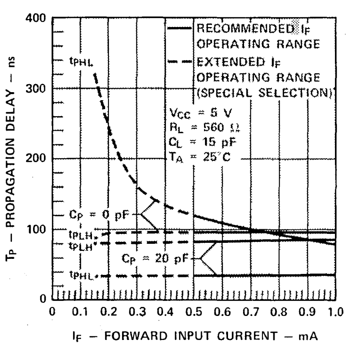


Figure 6. Typical Propagation Delay vs. Forward Current.

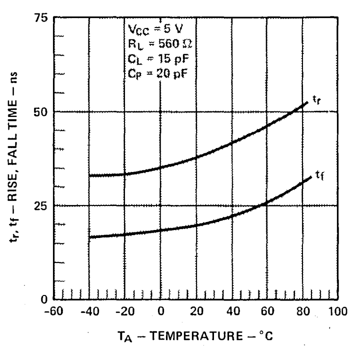


Figure 7. Typical Rise, Fall Time vs. Temperature.

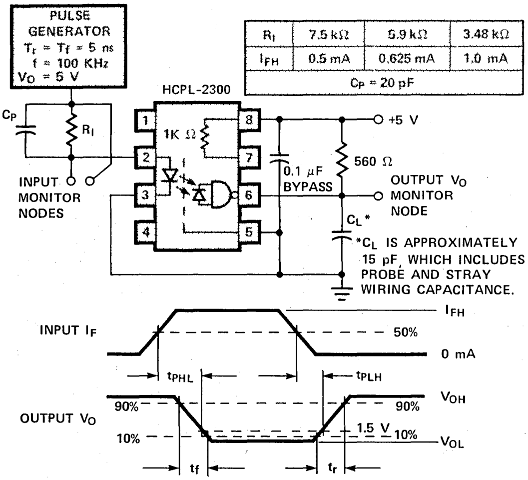


Figure 8. Test Circuit for t_{PHL}, t_{PLH}, t_r and t_f.

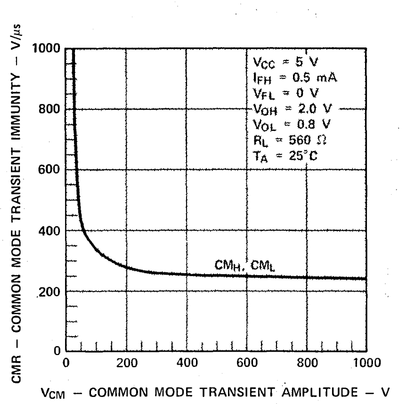


Figure 9. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

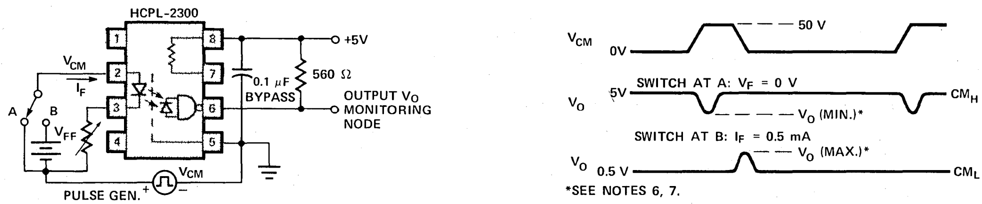


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

Applications

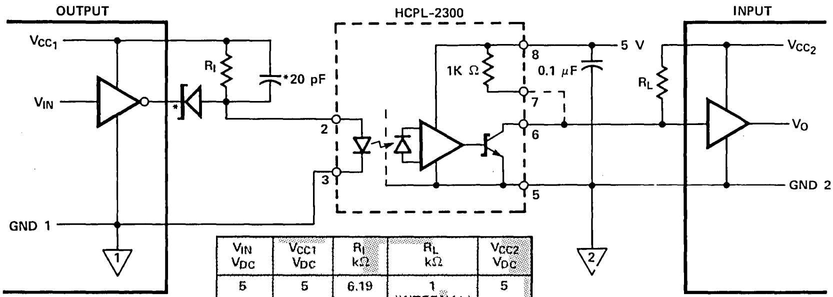
The HCPL-2300 optocoupler has the unique combination of low 0.5 mA LED operating drive current at a 5 MBd speed performance. Low power supply current requirement of 10 mA maximum and the ability to provide isolation between logic systems fulfills numerous applications ranging from logic level translations, line receiver and party line receiver applications, microprocessor I/O port isolation, etc. The open collector output allows for wired-OR arrangement. Specific interface circuits are illustrated in Figures 11 through 18 with corresponding component values, performance data and recommended layout.

For -40° C to 85° C operating temperature range, a mid range LED forward current (I_F) of 0.625 mA is recommended in order to prevent overdriving the integrated circuit detector due to increased LED efficiency at temperatures between 0° C and -40° C. For narrower temperature range of 0° C to 85° C, a suggested operating LED current of 0.75 mA is recommended for the mid range operating point and for minimal propagation delay skew. A peaking capacitance of 20 pF in parallel with the current limiting resistor for the LED shortens t_{PHL} by approximately 33% and t_{PLH} by 13%. Maintaining LED forward voltage (V_F) below 0.8 V will guarantee that the HCPL-2300 output is off.

The recommended shunt drive technique for TTL/LSTTL/CMOS of Figure 11 provides for optimal speed performance, no leakage current path through the LED, and reduced common mode influences associated with series switching of a "floating" LED. Alternate series drive techniques with either an active CMOS inverter or an open collector TTL/LSTTL inverter are illustrated in Figures 12 and 13 respectively. Open collector leakage current of 250 µA has been compensated by the 3.16K Ohms resistor (Figure 13) at the expense of twice the operating forward current.

An application of the HCPL-2300 as an unbalanced line receiver for use in long line twisted wire pair communication links is shown in Figure 14. Low LED I_F and V_F allow longer line length, higher speed and multiple stations on the line in comparison to higher I_F, V_F optocouplers. Greater speed performance along with nearly infinite common mode immunity are achieved via the balanced split phase circuit of Figure 15. Basic balanced (differential) line receiver can be accomplished with one HCPL-2300 in Figure 15, but with a typical 400 V/µs common mode immunity. Data rate versus distance for both the above unbalanced and balanced line receiver applications are compared in Figure 16. The RS-232-C interface circuit of Figure 17 provides guaranteed minimum common mode immunity of 100 V/µs while maintaining the 2:1 dynamic range of I_F.

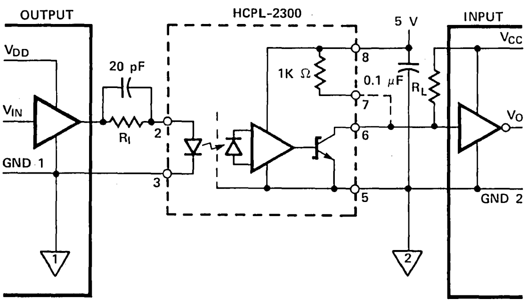
A recommended layout for use with an internal 1000 Ohms resistor or an external pull-up resistor and required V_{CC} bypass capacitor is given in Figure 18. V_{CC1} is used with an external pull-up resistor for output voltage levels (V0) greater than or equal to 5 V. As illustrated in Figure 18, an optional V_{CC} and GND trace can be located between the input and the output leads of the HCPL-2300 to provide additional noise immunity at the compromise of insulation capability (VI-0).



V_{IN} V_{DC}	V_{CC1} V_{DC}	R_I kΩ	R_L kΩ	V_{CC2} V_{DC}
5	5	6.19	1 (INTERNAL)	5
10	10	14.7	2.37	10
15	15	21.5	3.16	15

*SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT) AND 20 pF CAPACITOR ARE NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 11. Recommended Shunt Drive Circuit for Interfacing Between TTL/LSTTL/CMOS Logic Systems.



V_{IN} V_{DC}	V_{DD} V_{DC}	R_I kΩ	R_L kΩ	V_{CC} V_{DC}
5	5	5.11	1 (INTERNAL)	5
10	10	13.3	2.37	10
15	15	19.6	3.16	15

Figure 12. Active CMOS Series Drive Circuit.

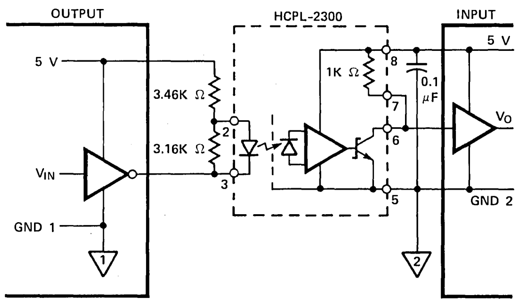
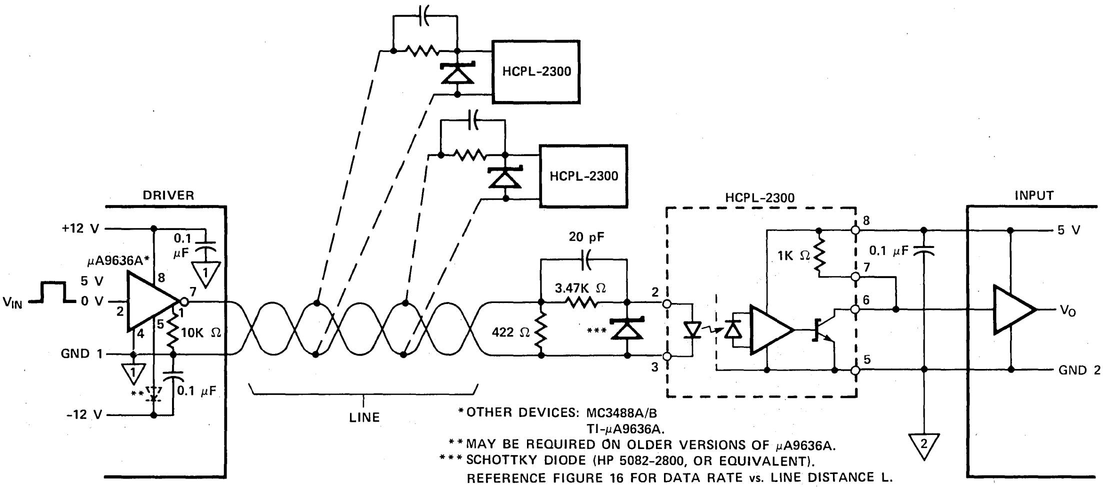


Figure 13. Series Drive from Open Collector TTL/LSTTL Units.



*OTHER DEVICES: MC3488A/B
TI-μA9636A.
**MAY BE REQUIRED ON OLDER VERSIONS OF μA9636A.
***SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT).
REFERENCE FIGURE 16 FOR DATA RATE vs. LINE DISTANCE L.

Figure 14. Application of HCPL-2300 as Isolated, Unbalanced Line Receiver(s).

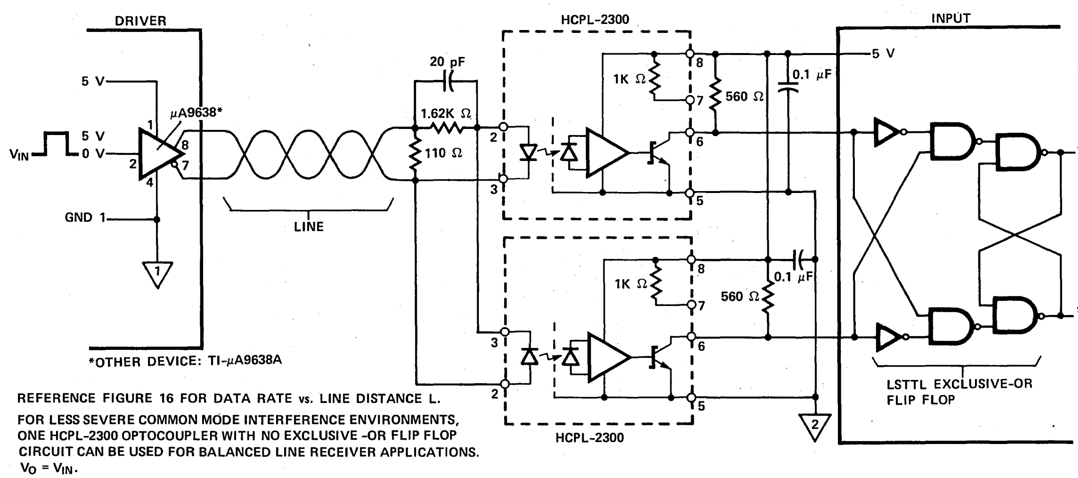


Figure 15. Application of Two HCPL-2300 Units Operating as an Isolated, High Speed, Balanced, Split Phase Line Receiver with Significantly Enhanced Common Mode Immunity.

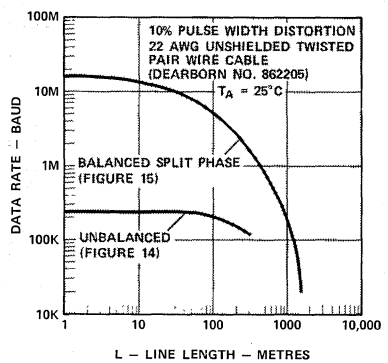


Figure 16. Typical Point to Point Data Rate vs. Length of Line for Unbalanced (Figure 14) and Balanced (Figure 15) Line Receivers using HCPL-2300 Optocouplers.

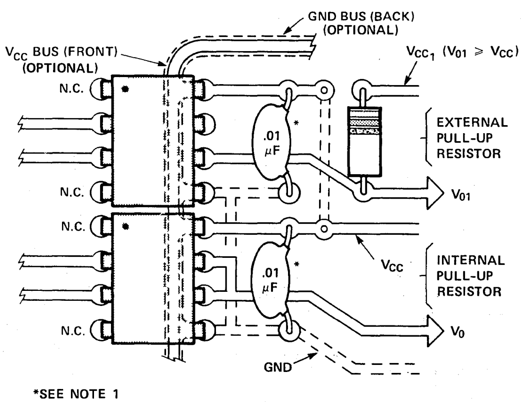


Figure 18. Recommended Printed Circuit Board Layout.

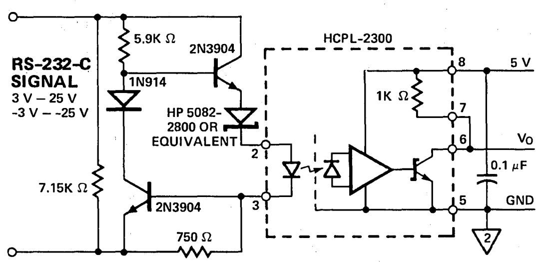


Figure 17. RS-232-C Interface Circuit with HCPL-2300. $0°C = T_A = 85°C$.

NOTES:

1. Bypassing of the power supply line is required with a 0.01 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 18. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 100 mA, 500 ns maximum pulse width, provided average current does not exceed 5 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., $V_{OUT} > 2.0$ V).
7. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., $V_{OUT} < 0.8$ V).
8. C_P is the peaking capacitance. Refer to test circuit in Figure 8.
9. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
10. See Option 010 data sheet for more information

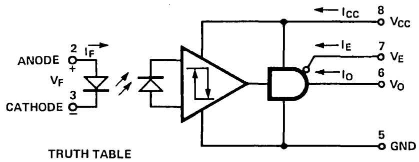
HEWLETT PACKARD

20 M BAUD HIGH CMR LOGIC GATE OPTOCOUPLER

HCPL-2400

TECHNICAL DATA JANUARY 1986

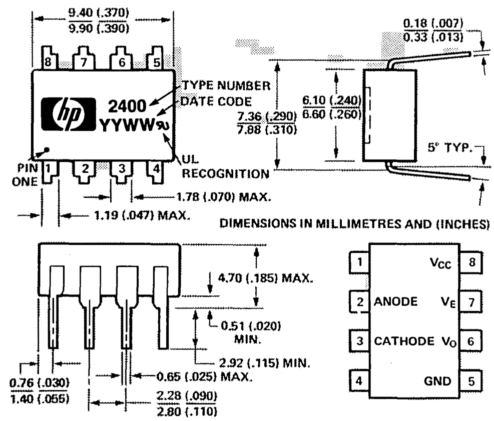
SCHEMATIC



TRUTH TABLE (POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H	L	L
L	L	H
H	H	Z
L	H	Z

OUTLINE DRAWING



Features

- HIGH SPEED: 40 MBd TYPICAL DATA RATE
- HIGH COMMON MODE REJECTION — 1000 V/μs GUARANTEED MINIMUM COMMON MODE TRANSIENT IMMUNITY
- AC PERFORMANCE GUARANTEED OVER TEMPERATURE
- COMPATIBLE WITH TTL, STTL, LSTTL, AND HCMOS LOGIC FAMILIES
- NEW, HIGH SPEED AlGaAs EMITTER
- THREE STATE OUTPUT (NO PULL-UP RESISTOR REQUIRED)
- HIGH POWER SUPPLY NOISE IMMUNITY
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Applications

- ISOLATION OF HIGH SPEED LOGIC SYSTEMS
- COMPUTER-PERIPHERAL INTERFACES
- ISOLATED BUS DRIVER (NETWORKING APPLICATIONS)
- SWITCHING POWER SUPPLIES
- GROUND LOOP ELIMINATION
- HIGH SPEED DISK DRIVE I/O
- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- PULSE TRANSFORMER REPLACEMENT

Description

The HCPL-2400 high speed optocoupler combines an 820 nm AlGaAs photon emitting diode with a high speed photon detector. This combination results in very high data rate capability and low input current. The three state output eliminates the need for a pull-up resistor and allows for direct drive of data buses. The hysteresis provides typically 0.25 mA of differential mode noise immunity and minimizes the potential for output signal chatter. Improved power supply rejection minimizes the need for special power supply bypassing precautions.

The electrical and switching characteristics of the HCPL-2400 are guaranteed over the temperature range of 0° C to 70° C.

The HCPL-2400 is compatible with TTL, STTL, LSTTL and HCMOS logic families. When Schottky type TTL devices (STTL) are used, a data rate performance of 20 MBd over temperature is guaranteed when using the application circuit of Figure 13. Typical data rates are 40 MBd.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Input Current (High)	$I_{F\,(ON)}$	4	8	mA
Input Voltage (Low)	$V_{F\,(OFF)}$	—	0.8	Volts
Enable Voltage (Low)	V_{EL}	0	0.8	Volts
Enable Voltage (High)	V_{EH}	2.0	V_{CC}	Volts
Operating Temperature	T_A	0	70°	°C
Fan Out	N		5	TTL Loads

Absolute Maximum Ratings

(No derating required up to 85° C)

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature	T_A	0	85	°C	
Lead Solder Temperature	260° C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		10.0	mA	
Peak Forward Input Current	I_{FPK}		20.0	mA	9
Reverse Input Voltage	V_R		3.0	V	
Supply Voltage	V_{CC}	0	7.0	V	
Three State Enable Voltage	V_E	–0.5	10.0	V	
Average Output Collector Current	I_O	–25.0	25.0	mA	
Output Collector Voltage	V_O	–0.5	10.0	V	
Output Collector Power Dissipation	P_O		40.0	mW	

Electrical Characteristics

For $0°C \leq T_A \leq 70°C$, $4.75\ V \leq V_{CC} \leq 5.25\ V$, $4\ mA \leq I_{F(ON)} \leq 8\ mA$, $2.0\ V \leq V_{EH} \leq 5.25$, $0\ V \leq V_{EL} \leq 0.8\ V$, $0\ V \leq V_{F(OFF)} \leq 0.8\ V$ except where noted. All Typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 5.0\ mA$, $V_{F(OFF)} = 0\ V$ except where noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	$I_{OL} = 8.0$ mA (5 TTL Loads)		1	
Logic High Output Voltage	V_{OH}	2.4			Volts	$I_{OH} = -4.0$ mA		2	
Output Leakage Current	I_{OHH}			100	μA	$V_O = 5.25$ V	$V_F = 0.8$ V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	μA	$V_E = 2.4$ V			
				100	μA	$V_E = 5.25$ V			
Logic Low Enable Current	I_{EL}		–0.28	–0.4	mA	$V_E = 0.4V$			
Logic Low Supply Current	I_{CCL}		19	26	mA	$V_{CC} = 5.25$ V			
Logic High Supply Current	I_{CCH}		17	26	mA	$V_E = 0$ V			
High Impedance State Supply Current	I_{CCZ}		22	28	mA	$V_{CC} = 5.25$ V $V_E = 5.25$ V			
High Impedance State Output Current	I_{OZL}			20	μA	$V_O = 0.4V$	$V_E = 2$ V		
	I_{OZH}			20	μA	$V_O = 2.4$ V	$V_E = 2$ V		
	I_{OZH}			100	μA	$V_O = 5.25$ V			
Logic Low Short Circuit Output Current	I_{OSL}		52		mA	$V_O = V_{CC} = 5.25$ V	$I_F = 8$ mA		1
Logic High Short Circuit Output Current	I_{OSH}		–45		mA	$V_{CC} = 5.25$ V	$I_F = 0$ mA, V_O = GND		1
Input Current Hysteresis	I_{HYS}		0.25		mA	$V_{CC} = 5$ V		3	
Input Forward Voltage	V_F	1.1	1.3	1.5	Volts	$I_F = 5$ mA, $T_A = 25°C$		4	
Input Reverse Breakdown Voltage	V_R	3.0	5.0		Volts	$I_R = 10\ \mu A$, $T_A = 25°C$			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		–1.44		mV/°C	$I_F = 5$ mA		4	
Input-Output Insulation	I_{I-O}			1	μA	45% RH, t = 5s, V_{I-O} = 3kVdc, $T_A = 25°C$			2, 8
Option 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min.			10
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			2
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 V dc			2
Input Capacitance	C_{IN}		20		pF	f = 1 MHz, V_F = 0V, Pins 2 and 3			

Switching Characteristics

$0°C \leq T_A \leq 70°C$, $4.75\ V \leq V_{CC} \leq 5.25\ V$, $0.0\ V \leq V_{EN} \leq 0.8\ V$, $4\ mA \leq I_F \leq 8.0\ mA$. All Typicals $V_{CC} = 5\ V$, $T_A = 25°C$, $I_F = 5.0\ mA$ except where noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}			55	ns	$I_{F(ON)} = 7.0$ mA	5,6,7	4
		15	33	60	ns		5,6,7	3
Propagation Delay Time to Logic High Output Level	t_{PLH}			55	ns	$I_{F(ON)} = 7.0$ mA	5,6,7	4
		15	30	60	ns		5,6,7	3
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH}\rvert$		2	15	ns	$I_{F(ON)} = 7.0$ mA	5,8	4
			3	25	ns		5,8	
Channel Distortion	Δt_{PHL}		8	25	ns		5	5
	Δt_{PLH}		8	25	ns		5	5
Output Rise Time	t_r		20		ns		5	
Output Fall Time	t_f		10		ns		5	
Output Enable Time to Logic High	t_{PZH}		15		ns		9,10	
Output Enable Time to Logic Low	t_{PZL}		30		ns		9,10	
Output Disable Time from Logic High	t_{PHZ}		20		ns		9,10	
Output Disable Time from Logic Low	t_{PLZ}		15		ns		9,10	
Logic High Common Mode Transient Immunity	$\lvert CM_H\rvert$	1000	10,000		V/µs	$T_A = 25°C$, $I_F = 0$	11,12	6
Logic Low Common Mode Transient Immunity	$\lvert CM_L\rvert$	1000	10,000		V/µs	$T_A = 25°C$, $I_F = 4$ mA	11,12	6
Power Supply Noise Immunity	PSNI		0.5		V_{p-p}	$V_{CC} = 5.0$ V, 48 Hz $\leq F_{AC} \leq$ 50 MHz		7

Notes:

1. Duration of output short circuit time not to exceed 10 ms.
2. Device considered a two terminal device: pins 1–4 shorted together, and pins 5–8 shorted together.
3. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input current pulse to the 1.5 V level on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input current pulse to the 1.5 V level on the rising edge of the output pulse.
4. This specification simulates the worst case operating conditions of the HCPL-2400 over the recommended operating temperature and V_{CC} range with the suggested applications circuit of Figure 13.
5. Channel distortion describes the worst case variation of propagation delay from one part to another at identical operating conditions.
6. CM_H is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)} > 2.0$ V). CM_L is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)} < 0.8$ V).
7. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)} > 2.0$ V, and for desired logic low state, $V_{OL(MAX)} < 0.8$ volts.
8. This is a proof test. This rating is equally validated by a 2500 V ac, 1 second test per UL E55 361.
9. Peak Forward Input Current pulse width < 50 µs at 1 KHz maximum repetition rate.
10. See Option 010 data sheet for more information.

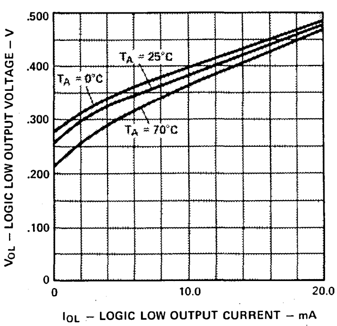


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current

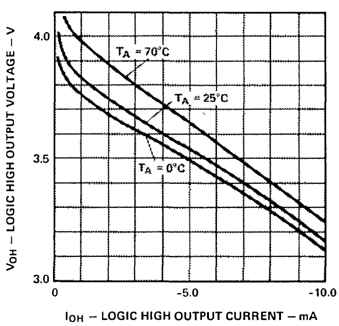


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current

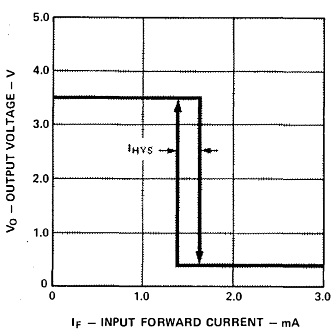


Figure 3. Typical Output Voltage vs. Input Forward Current

OPTOCOUPLERS

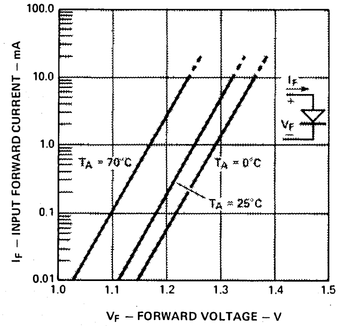


Figure 4. Typical Diode Input Forward Current Characteristic

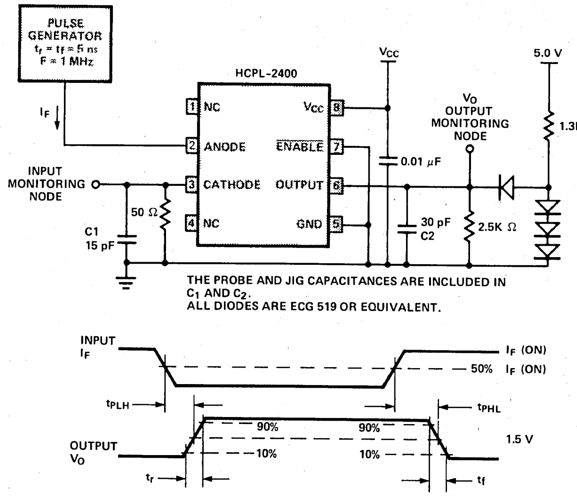


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

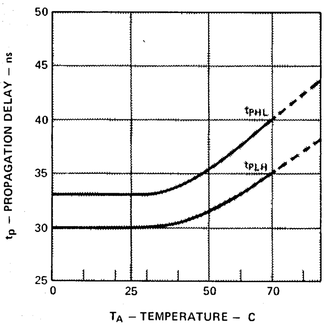


Figure 6. Typical Propagation Delay vs. Ambient Temperature

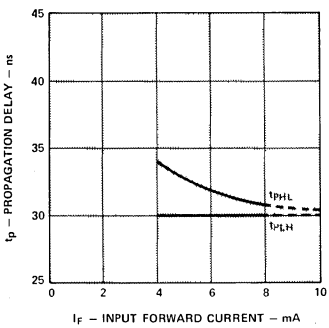


Figure 7. Typical Propagation Delay vs. Input Forward Current

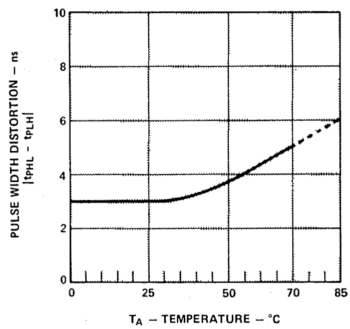
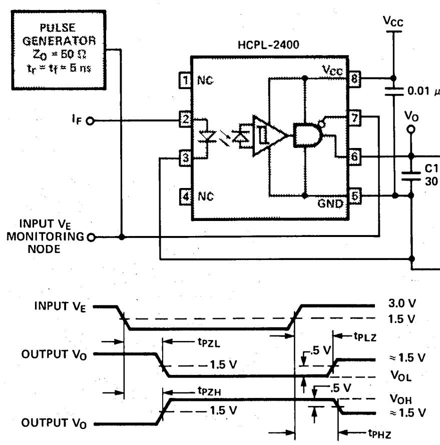


Figure 8. Typical Pulse Width Distortion vs. Ambient Temperature



SWITCH MATRIX

	S_1	S_2
t_{PHZ}	CLOSED	CLOSED
t_{PZH}	OPEN	CLOSED
t_{PLZ}	CLOSED	CLOSED
t_{PZL}	CLOSED	OPEN

ALL DIODES ARE EC6 519 OR EQUIVALENT
C1 = 30 pF INCLUDING PROBE AND JIG CAPACITANCE.

Figure 9. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ} and t_{PZL}.

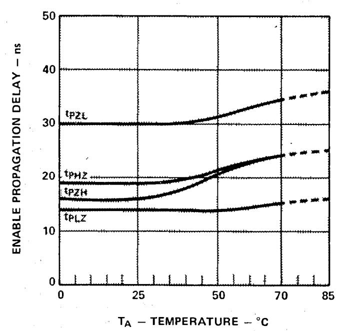
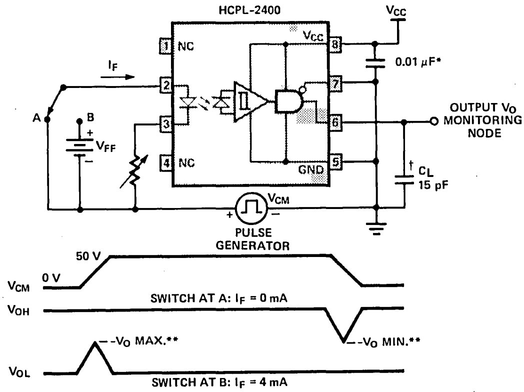


Figure 10. Typical Enable Propagation Delay vs. Ambient Temperature



*MUST BE LOCATED < 1 cm FROM DEVICE UNDER TEST.
**SEE NOTE 6.
† C_L IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms

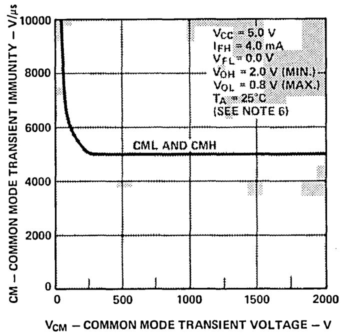


Figure 12. Typical Common Mode Transient Immunity vs. Common Mode Transient Voltage

Applications

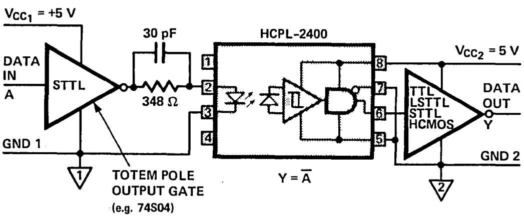


Figure 13. Recommended 20 MBd HCPL-2400 Interface Circuit

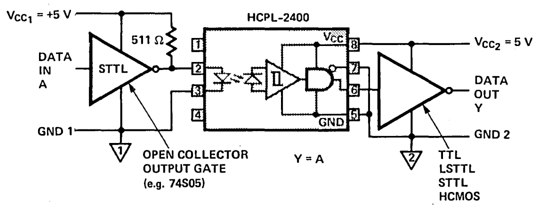


Figure 14. Alternative HCPL-2400 Interface Circuit

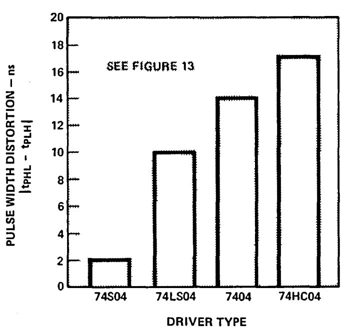


Figure 15. Typical Pulse Width Distortion vs. Input Driver Logic Family

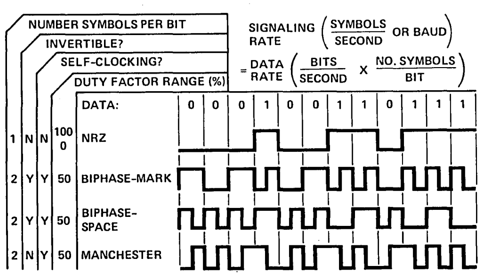


Figure 16. Modulation Code Selections

Data Rate, Pulse-Width Distortion, and Channel Distortion Definitions

In the world of data communications, a bit is defined as the smallest unit of information a computer operates with. A bit is either a Logic 1 or Logic 0, and is interpreted by a number of coding schemes. For example, a bit can be represented by one symbol through the use of NRZ code, or can contain two symbols in codes such as Biphase or Manchester (see Figure 16). The bit rate capability of a system is expressed in terms of bits/second (b/s) and the symbol rate is expressed in terms of Baud (symbols/second). For NRZ code, the bit rate capability equals the Baud capability because the code contains one symbol per bit of information. For Biphase and Manchester codes, the bit rate capability is equal to one half of the Baud capability, because there are two symbols per bit.

Propagation delay is a figure of merit which describes the finite amount of time required for a system to translate information from input to output when shifting logic levels. Propagation delay from low to high (t_{PLH}) specifies the amount of time required for a system's output to change from a Logic 0 to a Logic 1, when given a stimulus at the input. Propagation delay from high to low (t_{PHL}) specifies the amount of time required for a system's output to change from a Logic 1 to a Logic 0, when given a stimulus at the input (see Figure 5).

When t_{PLH} and t_{PHL} differ in value, pulse width distortion results. Pulse width distortion is defined as $|t_{PHL}-t_{PLH}|$ and determines the maximum data rate capability of a distortion-limited system. Maximum pulse width distortion on the order of 20–30% is typically used when specifying the maximum data rate capabilities of systems. The exact figure depends on the particular application (RS-232, PCM, T-1, etc.).

Channel distortion, (Δt_{PHL}, Δt_{PLH}), describes the worst case variation of propagation delay from device to device at identical operating conditions. Propagation delays tend to shift as operating conditions change, and channel distortion specifies the uniformity of that shift. Specifying a maximum value for channel distortion is helpful in parallel data transmission applications where the synchronization of signals on the parallel lines is important.

The HCPL-2400 optocoupler offers the advantages of specified propagation delay (t_{PLH}, t_{PHL}), pulse-width distortion ($|t_{PLH}-t_{PHL}|$), and channel distortion (Δt_{PLH}, Δt_{PHL}) over temperature, input forward current, and power supply voltage ranges.

Applications Circuits

A recommended application circuit for high speed operation is shown in Figure 13. Due to the fast current switching capabilities of Schottky family TTL logic (74STTL), data rates of 20 MBd are achievable from 0 to 70°C. The 74S04 totem-pole driver sources current to series-drive the input of the HCPL-2400 optocoupler. The 348Ω resistor limits the LED forward current. The 30 pF speed-up capacitor assists in the turn-on and turn-off of the LED, increasing the data rate capability of the circuit. On the output side, the following logic can be directly driven by the output of the HCPL-2400, since a pull-up resistor is not required. If desired, a non-inverting buffer may be substituted on either the input or the output side to change the circuit function from $Y = \overline{A}$ to $Y = A$. This circuit satisfies all recommended operating conditions.

An alternative circuit is shown in Figure 14, which utilizes a 74S05 open-collector inverter to shunt-drive the HCPL-2400 optocoupler. This circuit also satisfies all recommended operating conditions.

The HCPL-2400 optocoupler is compatible with other logic families, such as TTL, LSTTL, and HCMOS. However, the output drive capabilities of Schottky family devices greatly exceed those associated with TTL, LSTTL, and HCMOS logic families, and are recommended in high data rate (20 MBd) applications where fast drive current transitions are required to operate the HCPL-2400 with minimum pulse-width distortion.

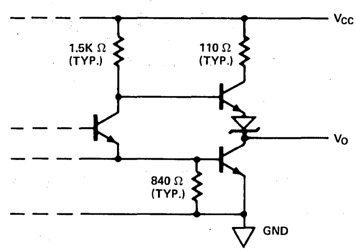


Figure 17. Typical HCPL-2400 Output Schematic

HEWLETT PACKARD

LSTTL/TTL COMPATIBLE OPTOCOUPLER

6N137

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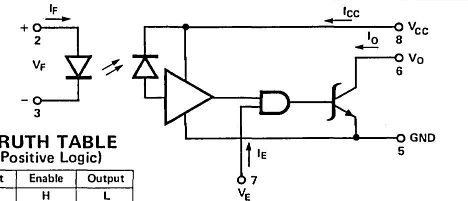
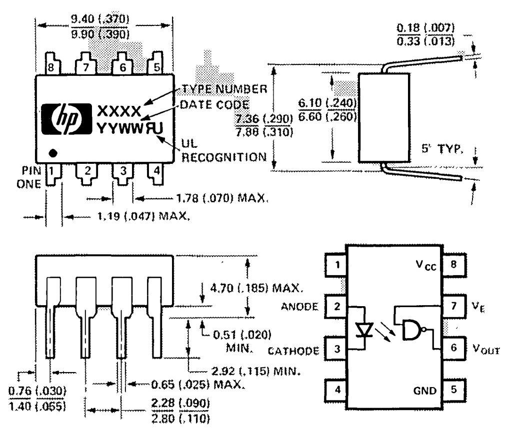


TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

Figure 1.

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- LSTTL/TTL COMPATIBLE: 5 V SUPPLY
- HIGH SPEED: 10 MBd TYPICAL
- LOW INPUT CURRENT REQUIRED: 5 mA
- HIGH COMMON MODE REJECTION: >1000 V/μs TYPICAL
- GUARANTEED PERFORMANCE OVER TEMPERATURE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Description/Applications

The 6N137 consists of a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing.

The 6N137 can be used in high speed digital interfacing applications where common mode signals must be rejected, such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, OR'ing and strobing.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3**	15	mA
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage (Output High)	V_{EL}	0	0.8	V
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings*

(No derating required up to 70°C)

Storage Temperature .... −55°C to +125°C
Operating Temperature .... 0°C to +70°C
Lead Solder Temperature .... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current .... 40mA (t ≤ 1msec Duration)
Average Forward Input Current 20mA
Reverse Input Voltage 5V
Enable Input Voltage .... 5.5V (Not to exceed V_{CC} by more than 500mV)
Supply Voltage - V_{CC} .... 7V (1 Minute Maximum)
Output Current - I_O 50mA
Output Collector Power Dissipation 85mW
Output Voltage - V_O 7V

**6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

*JEDEC Registered Data.

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}*		2	250	μA	V_{CC}=5.5V, V_O=5.5V, I_F=250μA, V_E=2.0V	6	
Low Level Output Voltage	V_{OL}*		0.4	0.6	V	V_{CC}=5.5V, I_F=5mA, V_{EH}=2.0V I_{OL} (Sinking) =13mA	3,5	
High Level Enable Current	I_{EH}		-1.0		mA	V_{CC}=5.5V, V_E=2.0V		
Low Level Enable Current	I_{EL}*		-1.4	-2.0	mA	V_{CC}=5.5V, V_E=0.5V		
High Level Supply Current	I_{CCH}*		7	15	mA	V_{CC}=5.5V, I_F=0 V_E=0.5V		
Low Level Supply	I_{CCL}*		14	18	mA	V_{CC}=5.5V, I_F=10mA V_E=0.5V		
Input-Output Insulation	I_{I-O}*			1	μA	45% RH, t = 5s, V_{I-O}= 3 kV dc, T_A= 25°C		5, 9
OPT 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50% t = 1 MIN		10
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500V, T_A=25°C		5
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f=1MHz, T_A=25°C		5
Input Forward Voltage	V_F*		1.5	1.75	V	I_F=10mA, T_A=25°C	4	8
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R=10μA, T_A=25°C		
Input Capacitance	C_{IN}		60		pF	V_F=0, f=1MHz		
Current Transfer Ratio	CTR		700		%	I_F=5.0mA, R_L=100Ω	2	7

*For JEDEC registered parts.

**All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics at T_A=25°C, V_{CC}=5V

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}*		55	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	1
Propagation Delay Time to Low Output Level	t_{PHL}*		55	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	2
Output Rise-Fall Time (10-90%)	t_r, t_f		50, 20		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA		
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		65		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA, V_{EH}=3.0V, V_{EL}=0.5V	8	3
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		20		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA V_{EH}=3.0V, V_{EL}=0.5V	8	4
Common Mode Transient Immunity at Logic High Output Level	$\|CM_H\|$		100		v/μs	V_{CM}=10V R_L=350Ω, V_O(min.)=2V, I_F=0mA	11	6
Common Mode Transient Immunity at Logic Low Output Level	$\|CM_L\|$		-300		v/μs	V_{CM}=10V R_L=350Ω, V_O(max.)=0.8V, I_F=5mA	11	6

*JEDEC Registered Data.

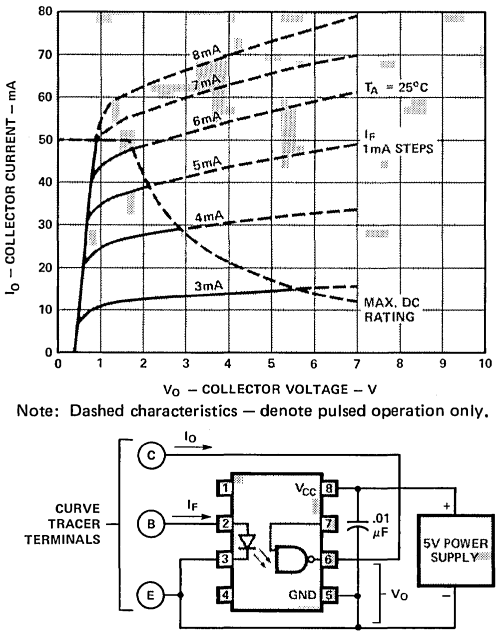
Operating Procedures and Definitions

Logic Convention. The 6N137 is defined in terms of positive logic.

Bypassing. A ceramic capacitor (.01 to 0.1μF) should be connected from pin 8 to pin 5 (Figure 12). Its purpose is to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 20mm.

Polarities. All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Enable Input. No external pull-up required for a logic (1), i.e., can be open circuit.



Note: Dashed characteristics – denote pulsed operation only.

Figure 2. Optocoupler Collector Characteristics.

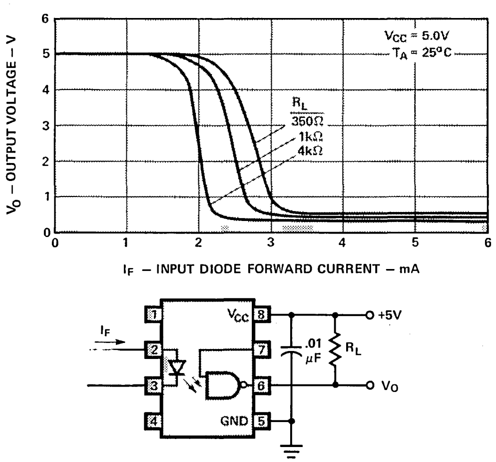


Figure 3. Input-Output Characteristics.

NOTES:

1. The t_{PLH} propagation delay is measured from the 3.75mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The t_{PHL} propagation delay is measured from the 3.75mA point on the leading edge of the input pulse to 1.5V point on the leading edge of the output pulse.
3. The t_{ELH} enable propagation delay is measured from the 1.5V point of the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
4. The t_{EHL} enable propagation delay is measured from the 1.5V point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
5. Device considered a two terminal device: pins 2 and 3 shorted together, and pins 5, 6, 7, and 8 shorted together.
6. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O>2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O<0.8V).
7. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
8. At 10mA V_F decreases with increasing temperature at the rate of 1.6mV/°C.
9. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
10. See Option 010 data sheet for more information.

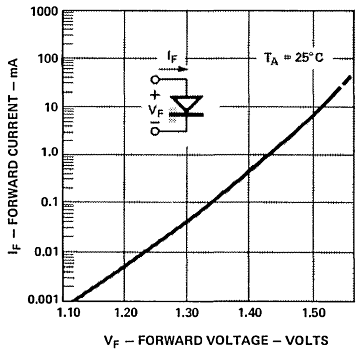


Figure 4. Input Diode Forward Characteristic.

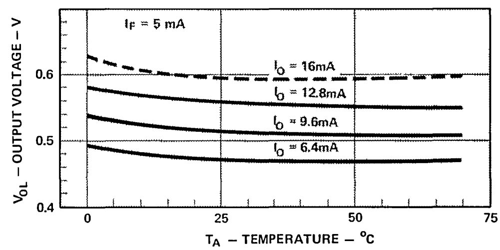


Figure 5. Output Voltage, V_{OL} vs. Temperature and Fan-Out.

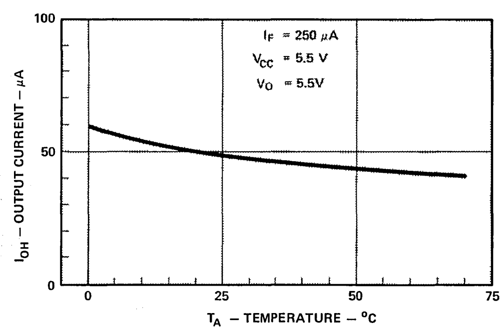


Figure 6. Output Current, I_{OH} vs. Temperature (I_F=250μA).

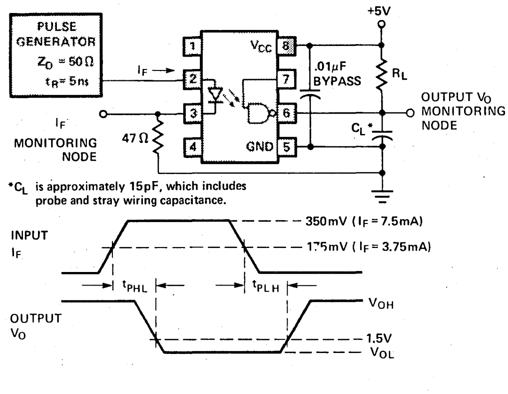


Figure 7. Test Circuit for t_{PHL} and t_{PLH}.**

**JEDEC Registered Data.

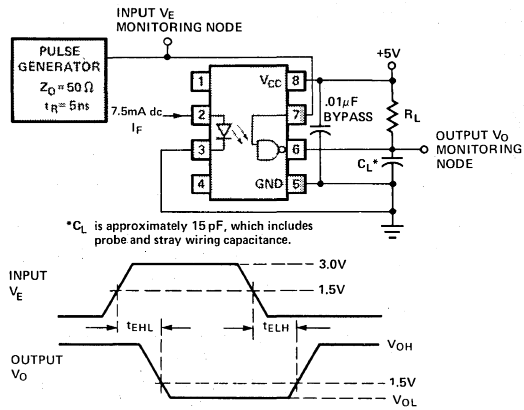


Figure 8. Test Circuit for t_{ELH} and t_{EHL}.

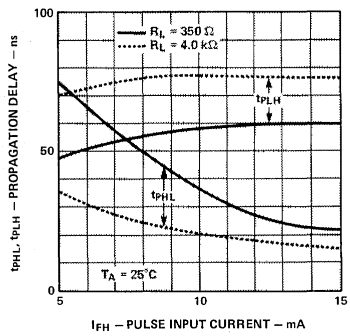


Figure 9. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

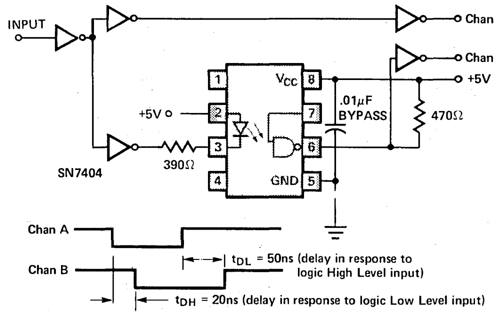
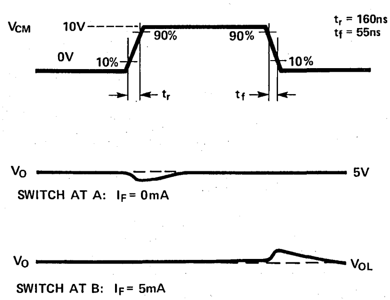


Figure 10. Response Delay Between TTL Gates.



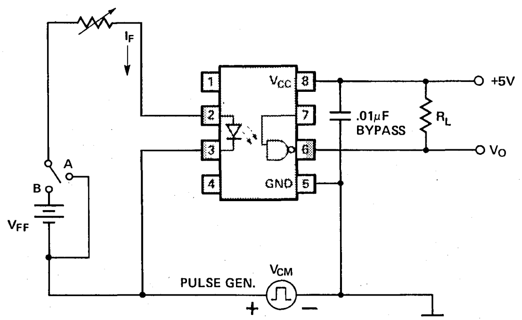


Figure 11. Test Circuit for Transient Immunity and Typical Waveforms.

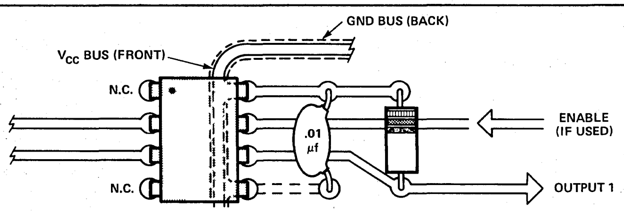


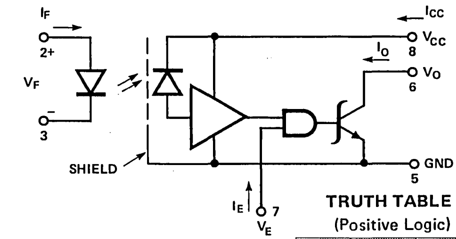
Figure 12. Recommended Printed Circuit Board Layout.

HEWLETT PACKARD

HIGH CMR, HIGH SPEED OPTOCOUPLER

HCPL-2601

TECHNICAL DATA JANUARY 1986



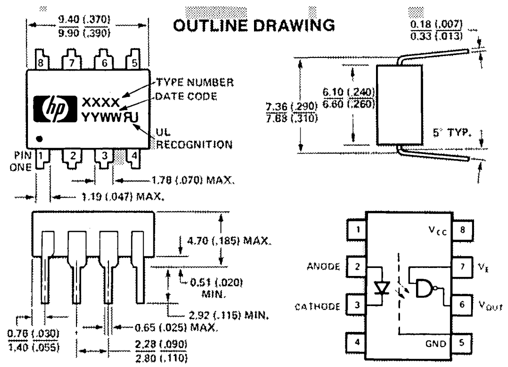
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

Figure 1. Schematic.

OUTLINE DRAWING



DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION (CMR)**
- **HIGH SPEED: 10 MBd TYPICAL**
- **GUARANTEED MINIMUM COMMON MODE TRANSIENT IMMUNITY: 1000V/μs**
- **LSTTL/TTL COMPATIBLE**
- **LOW INPUT CURRENT REQUIRED: 5mA**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE: 0°C to 70°C**
- **STROBABLE OUTPUT**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).**

Description

The HCPL-2601 optically coupled gate combines a GaAsP light emitting diode and an integrated high gain photon detector. An enable input allows the detector to be strobed. The output of the detector I.C. is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 1000 volts/μsec.

This unique design provides maximum D.C. and A.C. circuit isolation while achieving TTL compatibility. The isolator D.C. operational parameters are guaranteed from 0°C to 70°C allowing troublefree system performance. This isolation is achieved with a typical propagation delay of 40 nsec.

The HCPL-2601's are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Applications

- Isolated Line Receiver
- Simplex/Multiplex Data Transmission
- Computer-Peripheral Interface
- Microprocessor System Interface
- Digital Isolation for A/D, D/A Conversion
- Switching Power Supply
- Instrument Input/Output Isolation
- Ground Loop Elimination
- Pulse Transformer Replacement

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level	I_{FL}	0	250	μA
Input Current, High Level	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Storage Temperature .... −55°C to +125°C
Operating Temperature .... 0°C to +70°C
Lead Solder Temperature .... 260°C for 10 s
(1.6mm below seating plane)
Forward Input Current − I_F (see Note 2) .... 20 mA
Reverse Input Voltage .... 5 V
Supply Voltage − V_{CC} .... 7V (1 Minute Maximum)
Enable Input Voltage − V_E .... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current − I_O .... 25 mA
Output Collector Power Dissipation .... 40 mW
Output Collector Voltage − V_O .... 7 V

*6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

(Over Recommended Temperature, $T_A = 0°C$ to $+70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		20	250	μA	$V_{CC} = 5.5V$, $V_O = 5.5V$, $I_F = 250\ \mu A$, $V_E = 2.0\ V$	2	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	$V_{CC} = 5.5V$, $I_F = 5\ mA$ $V_E = 2.0\ V$, I_{OL} (Sinking) = 13 mA	3,5	
High Level Supply Current	I_{CCH}		10	15	mA	$V_{CC} = 5.5V$, $I_F = 0$, $V_E = 0.5\ V$		
Low Level Supply Current	I_{CCL}		15	19	mA	$V_{CC} = 5.5V$, $I_F = 10\ mA$, $V_E = 0.5\ V$		
Low Level Enable Current	I_{EL}		-1.4	-2.0	mA	$V_{CC} = 5.5\ V$, $V_E = 0.5\ V$		
High Level Enable Current	I_{EH}		-1.0		mA	$V_{CC} = 5.5\ V$, $V_E = 2.0V$		
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voltage	V_F		1.5	1.75	V	$I_F = 10\ mA$, $T_A = 25°C$	4	
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10\ \mu A$, $T_A = 25°C$		
Input Capacitance	C_{IN}		60		pF	$V_F = 0$, f = 1 MHz		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	$I_F = 10\ mA$		
Input-Output Insulation	I_{I-O}*			1	μA	45% RH, t = 5s, $V_{I-O} = 3$ kV dc, $T_A = 25°C$		3, 12
OPT 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50% t = 1 MIN		13
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	$V_{I-O} = 500\ V$		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*For JEDEC registered parts.

*All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

Switching Characteristics ($T_A = 25°C$, $V_{CC} = 5V$)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output level	t_{PLH}		40	75	ns	$R_L = 350\ \Omega$, $C_L = 15\ pF$, $I_F = 7.5\ mA$	6	4
Propagation Delay Time to Low Output Level	t_{PHL}		40	75	ns		6	5
Output Rise Time (10–90%)	t_r		20		ns			
Output Fall Time (90–10%)	t_f		30		ns			
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	$R_L = 350\ \Omega$, $C_L = 15\ pF$, $I_F = 7.5\ mA$, $V_{EH} = 3\ V$, $V_{EL} = 0\ V$	9	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		25		ns	$R_L = 350\ \Omega$, $C_L = 15\ pF$, $I_F = 7.5\ mA$, $V_{EH} = 3\ V$, $V_{EL} = 0\ V$	9	7
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	1000	10,000		V/μs	$V_{CM} = 50$ V (peak), V_O (min.) = 2 V, $R_L = 350\ \Omega$, $I_F = 0\ mA$	12	8,10
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	1000	10,000		V/μs	$V_{CM} = 50$ V (peak), V_O (max.) = 0.8 V, $R_L = 350\ \Omega$, $I_F = 7.5\ mA$	12	9,10

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 15. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
6. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} >2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT}<0.8 V).
10. For sinusoidal voltages, $\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM}$ (p-p)
11. No external pull up is required for a high logic state on the enable input.
12. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
13. See Option 010 data sheet for more information.

OPTOCOUPLERS

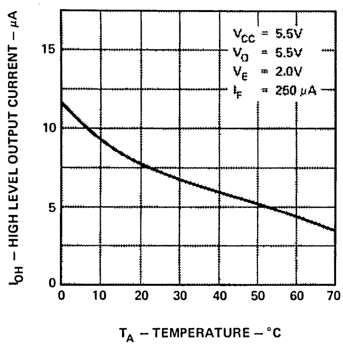


Figure 2. High Level Output Current vs. Temperature.

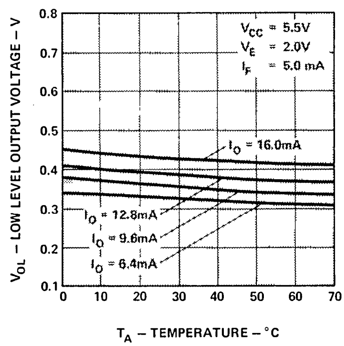


Figure 3. Low Level Output Voltage vs. Temperature.

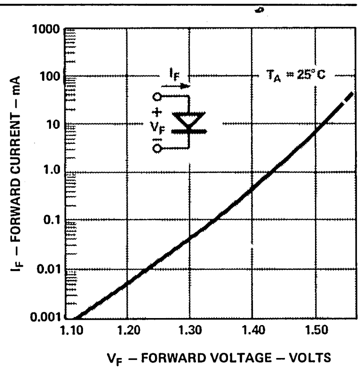


Figure 4. Input Diode Forward Characteristic.

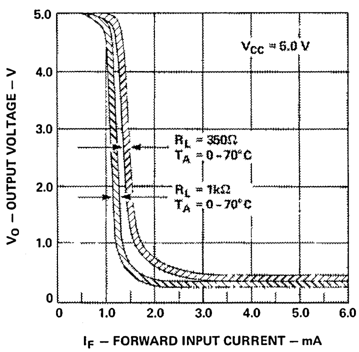


Figure 5. Output Voltage vs. Forward Input Current.

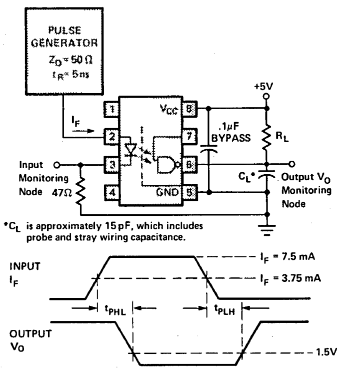


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

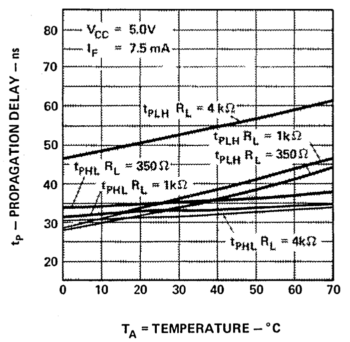


Figure 7. Propagation Delay vs. Temperature.

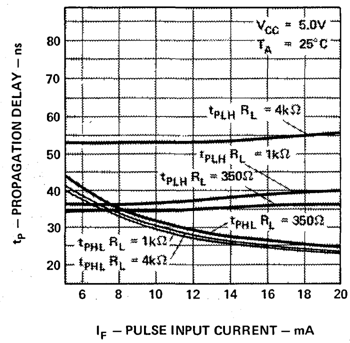


Figure 8. Propagation Delay vs. Pulse Input Current.

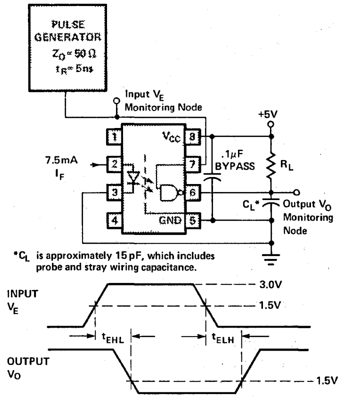


Figure 9. Test Circuit for t_{EHL} and t_{ELH}.

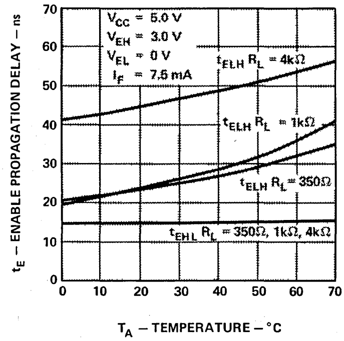


Figure 10. Enable Propagation Delay vs. Temperature.

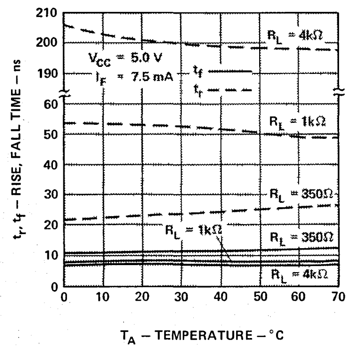


Figure 11. Rise, Fall Time vs. Temperature.

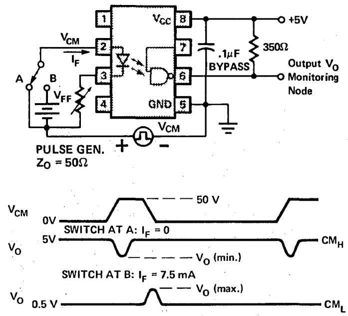


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

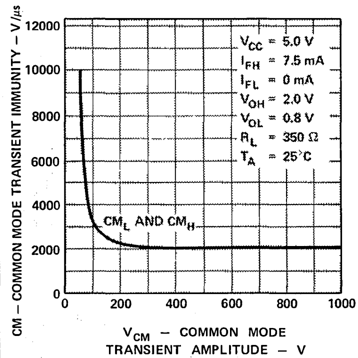


Figure 13. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

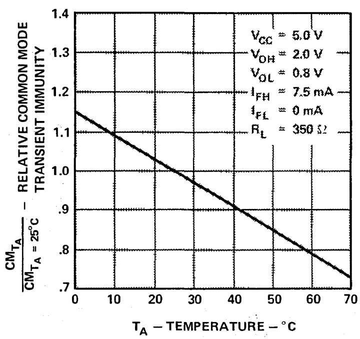


Figure 14. Relative Common Mode Transient Immunity vs. Temperature.

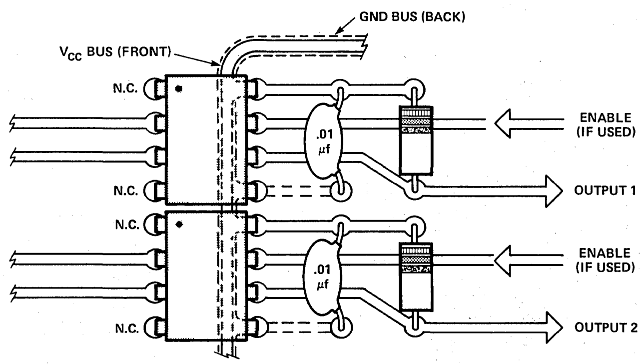


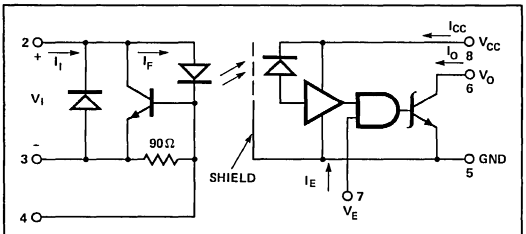
Figure 15. Recommended Printed Circuit Board Layout.

HEWLETT PACKARD

HIGH CMR LINE RECEIVER OPTOCOUPLER

HCPL-2602

TECHNICAL DATA JANUARY 1986

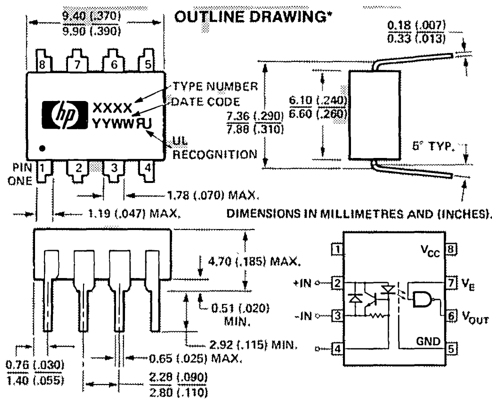


A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

Figure 1. Schematic.

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H



Features

- LINE TERMINATION INCLUDED — NO EXTRA CIRCUITRY REQUIRED
- ACCEPTS A BROAD RANGE OF DRIVE CONDITIONS
- GUARDBANDED FOR LED DEGRADATION
- LED PROTECTION MINIMIZES LED EFFICIENCY DEGRADATION
- HIGH SPEED — 10MBd (LIMITED BY TRANSMISSION LINE IN MANY APPLICATIONS)
- INTERNAL SHIELD PROVIDES EXCELLENT COMMON MODE REJECTION
- EXTERNAL BASE LEAD ALLOWS "LED PEAKING" AND LED CURRENT ADJUSTMENT
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Description

The HCPL-2602 optically coupled line receiver combines a GaAsP light emitting diode, an input current regulator and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance.

The regulator allows a typical LED current of 8.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of 1000 V/μsec.

Applications

- Isolated Line Receiver
- Simplex/Multiplex Data Transmission
- Computer-Peripheral Interface
- Microprocessor System Interface
- Digital Isolation for A/D, D/A Conversion
- Current Sensing
- Instrument Input/Output Isolation
- Ground Loop Elimination
- Pulse Transformer Replacement

DC specifications are defined similar to TTL logic and are guaranteed from 0°C to 70°C allowing trouble free interfacing with digital logic circuits. An input current of 5 mA will sink an eight gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45 nsec.

The HCPL-2602's are useful as line receivers in high noise environments that conventional line receivers cannot tolerate. The higher LED threshold voltage provides improved immunity to differential noise and the internally shielded detector provides orders of magnitude improvement in common mode rejection with little or no sacrifice in speed.

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damange from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	μA
Input Current, High Level	I_{IH}	6.3*	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

*6.3 mA condition permits at least 20% degradation guardband. Initial switching threshold is 5 mA or less.

Absolute Maximum Ratings

Storage Temperature .... −55° C to +125° C
Operating Temperature .... 0° C to +70° C
Lead Solder Temperature .... 260°C for 10 s (1.6mm below seating plane)
Forward Input Current — I_I .... 60 mA
Reverse Input Current .... 60 mA
Supply Voltage — V_{CC} .... 7V (1 Minute Maximum)
Enable Input Voltage — V_E .... 5.5 V (Not to exceed V_{CC} by more than 500 mV)
Output Collector Current — I_O .... 25 mA
Output Collector Power Dissipation .... 40 mW
Output Collector Voltage — V_O .... 7 V
Input Current, Pin 4 .... ±10 mA

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 15. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
3. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
4. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
5. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} >2.0 V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT}<0.8 V).
9. For sinusoidal voltages, $\left(\frac{|dV_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM}$ (p-p)
10. No external pull up is required for a high logic state on the enable input.
11. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
12. See Option 010 data sheet for more information.

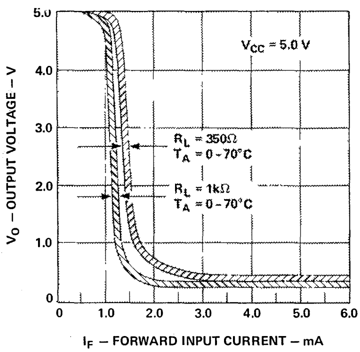


Figure 2. Output Voltage vs. Forward Input Current.

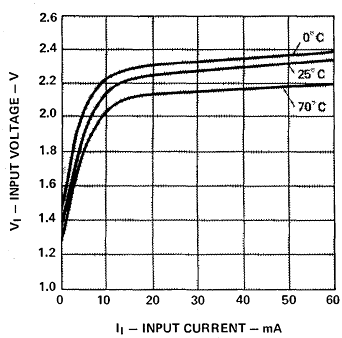


Figure 3. Input Characteristics.

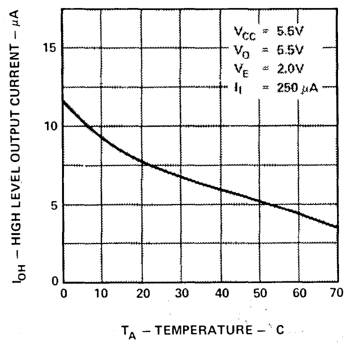


Figure 4. High Level Output Current vs. Temperature.

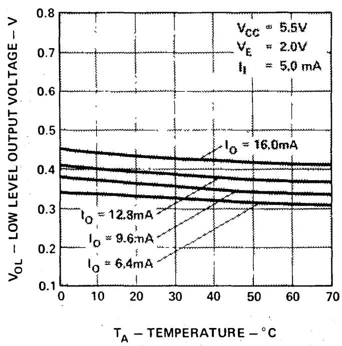


Figure 5. Low Level Output Voltage vs. Temperature.

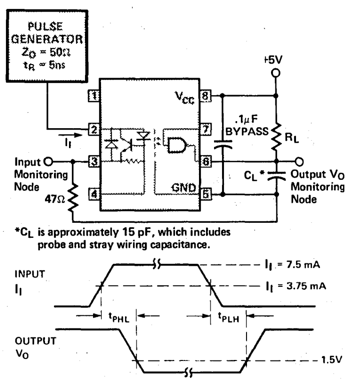


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

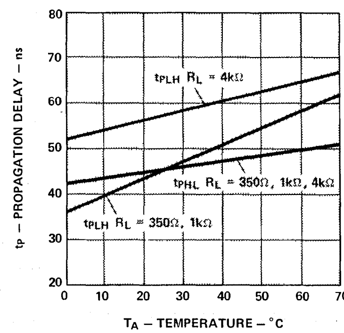


Figure 7. Propagation Delay vs. Temperature.

Electrical Characteristics

(Over Recommended Temperature, $T_A = 0°C$ to $+70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		20	250	μA	$V_{CC} = 5.5V$, $V_O = 5.5V$ I_I=250 μA, V_E=2.0V	4	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC}=5.5V, I_I=5 mA V_E=2.0V, I_{OL} (Sinking)=13 mA	2,5	
Input Voltage	V_I		2.0	2.4	V	I_I=5 mA	3	
			2.3	2.7		I_I=60 mA	3	
Input Reverse Voltage	V_R		0.75	0.95	V	I_R=5 mA		
Low Level Enable Current	I_{EL}		-1.4	-2.0	mA	V_{CC}=5.5V, V_E=0.5V		
High Level Enable Current	I_{EH}		-1.0		mA	V_{CC}=5.5V, V_E=2.0V		
High Level Enable Voltage	V_{EH}	2.0			V			10
Low Level Enable Voltage	V_{EL}			0.8	V			
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC}=5.5V, I_I=0, V_E=0.5V		
Low Level Supply Current	I_{CCL}		16	19	mA	V_{CC}=5.5V, I_I=60 mA V_E=0.5V		
Input Capacitance	C_{IN}		90		pF	V_I=0, f=1 MHz, (PIN 2-3)		
Input-Output Insulation	I_{I-O}*			1	μA	45% RH, t = 5s, V_{I-O}= 3 kV dc, T_A= 25°C		2, 11
OPT 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50% t = 1 MIN		12
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500V		2
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		2

*For JEDEC registered parts.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics

(T_A = 25°C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		45	75	ns	R_L = 350 Ω, C_L = 15 pF, I_I = 7.5 mA	6	3
Propagation Delay Time to Low Output Level	t_{PHL}		45	75	ns		6	4
Output Rise Time (10-90%)	t_r		25		ns			
Output Fall Time (90-10%)	t_f		25		ns			
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L=350Ω, C_L=15 pF, I_I=7.5 mA, V_{EH}=3 V, V_{EL}=0 V	10	5
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		15		ns		10	6
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	1000	10,000		V/μs	V_{CM}=50 V (peak), V_O (min.)=2 V, R_L=350Ω, I_I=0 mA	12	7, 9
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	1000	10,000		V/μs	V_{CM}=50 V (peak), V_O (max.)=0.8 V, R_L=350Ω, I_I=7.5 mA	12	8, 9

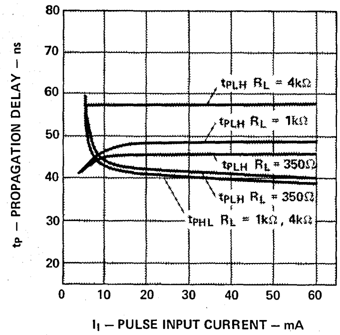


Figure 8. Propagation Delay vs. Pulse Input Current.

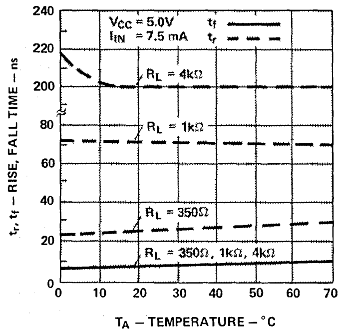


Figure 9. Rise, Fall Time vs. Temperature.

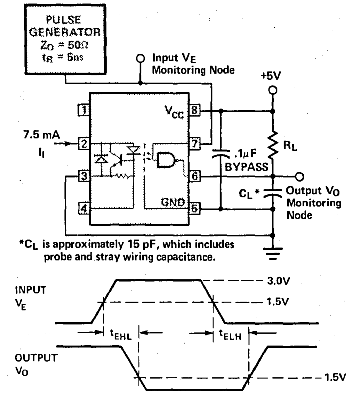


Figure 10. Test Circuit for t_{EHL} and t_{ELH}.

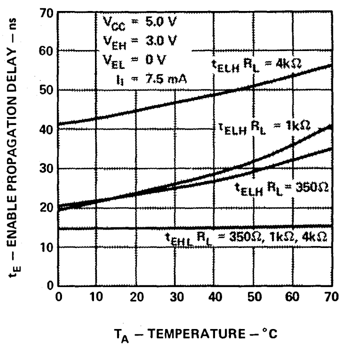


Figure 11. Enable Propagation Delay vs. Temperature.

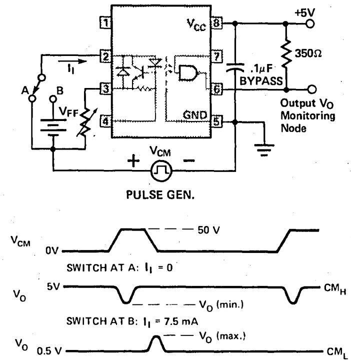


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

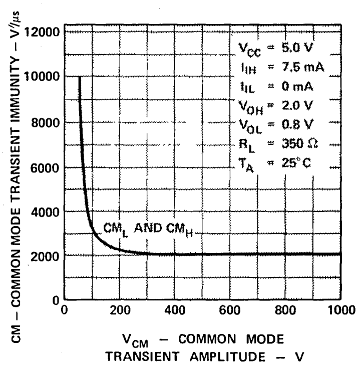


Figure 13. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

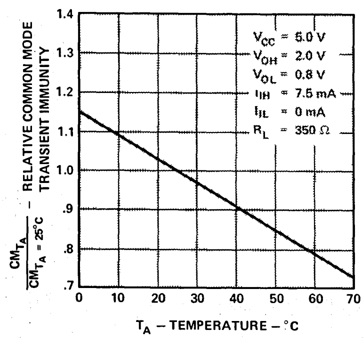


Figure 14. Relative Common Mode Transient Immunity vs. Temperature.

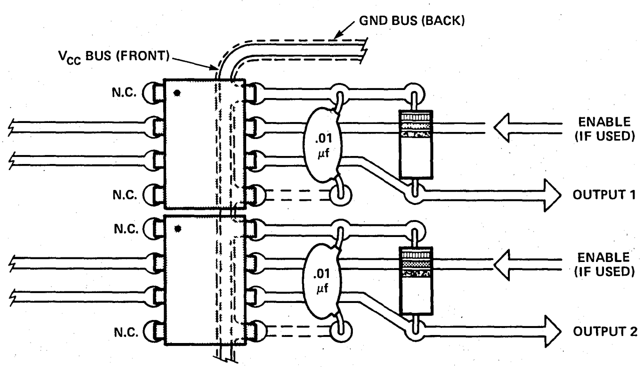


Figure 15. Recommended Printed Circuit Board Layout.

Using the HCPL-2602 Line Receiver Optocoupler

The primary objectives to fulfill when connecting an optocoupler to a transmission line are to provide a minimum, but not excessive, LED current and to properly terminate the line. The internal regulator in the HCPL-2602 simplifies this task. Excess current from variable drive conditions such as line length variations, line driver differences and power supply fluctuations are shunted by the regulator. In fact, with the LED current regulated, the line current can be increased to improve the immunity of the system to differential-mode-noise and to enhance the data rate capability. The designer must keep in mind the 60 mA input current maximum rating of the HCPL-2602, in such cases, and may need to use series limiting or shunting to prevent overstress.

Design of the termination circuit is also simplified; in most cases the transmission line can simply be connected directly to the input terminals of the HCPL-2602 without the need for additional series or shunt resistors. If reversing line drive is used it may be desirable to use two HCPL-2602's, or an external Schottky diode to optimize data rate.

Polarity Non-Reversing Drive

High data rates can be obtained with the HCPL-2602 with polarity non-reversing drive. Figure (a) illustrates how a 74S140 line driver can be used with the HCPL-2602 and shielded, twisted pair or coax cable without any additional components. There are some reflections due to the "active termination" but they do not interfere with circuit performance because the regulator clamps the line voltage. At longer line lengths t_{PLH} increases faster than t_{PHL} since the switching threshold is not exactly halfway between asymptotic line conditions. If optimum data rate is desired, a series resistor and peaking capacitor can be used to equalize t_{PLH} and t_{PHL}. In general, the peaking capacitance should be as large as possible; however, if it is too large it may keep the regulator from achieving turn-off during the negative (or zero) excursions of the input signal. A safe rule:

make $C \leqslant 16t$
where C = peaking capacitance in picofarads
t = data bit interval in nanoseconds

Polarity Reversing Drive

A single HCPL-2602 can also be used with polarity reversing drive (Figure b). Current reversal is obtained by way of the substrate isolation diode (substrate to collector). Some reduction of data rate occurs, however, because the substrate diode stores charge, which must be removed when the current changes to the forward direction. The effect of this is a longer t_{PHL}. This effect can be eliminated and data rate improved considerably by use of a Schottky diode on the input of the HCPL-2602.

For optimum noise rejection as well as balanced delays a split-phase termination should be used along with a flip-flop at the output (Figure c). The result of current reversal in split-phase operation is seen in Figure (c) with switches A and B both OPEN. The coupler inputs are then connected in ANTI-SERIES; however, because of the higher steady-state termination voltage, in comparison to the single HCPL-2602 termination, the forward current in the substrate diode is lower and consequently there is less junction charge to deal with when switching.

Closing switch B with A open is done mainly to enhance common mode rejection, but also reduces propagation delay slightly because line-to-line capacitance offers a slight peaking effect. With switches A and B both CLOSED, the shield acts as a current return path which prevents either input substrate diode from becoming reversed biased. Thus the data rate is optimized as shown in Figure (c).

Improved Noise Rejection

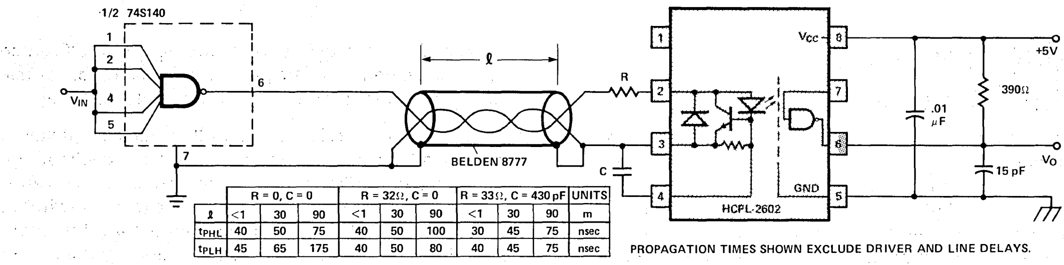
Use of additional logic at the output of two HCPL-2602's operated in the split phase termination, will greatly improve system noise rejection in addition to balancing propagation delays as discussed earlier.

A NAND flip-flop offers infinite common mode rejection (CMR) for NEGATIVELY sloped common mode transients but requires $t_{PHL} > t_{PLH}$ for proper operation. A NOR flip-flop has infinite CMR for POSITIVELY sloped transients but requires $t_{PHL} < t_{PLH}$ for proper operation. An exclusive-OR flip-flop has infinite CMR for common mode transients of EITHER polarity and operates with either $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$.

With the line driver and transmission line shown in Figure (c), $t_{PHL} > t_{PLH}$, so NAND gates are preferred in the R-S flip-flop. A higher drive amplitude or different circuit configuration could make $t_{PHL} < t_{PLH}$, in which case NOR gates would be preferred. If it is not known whether $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$, or if the drive conditions may vary over the boundary for these conditions, the exclusive-OR flip-flop of Figure (d) should be used.

RS-422 and RS-423

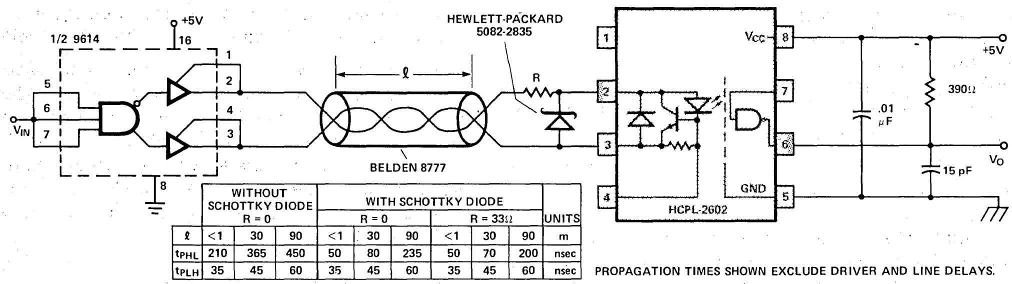
Line drivers designed for RS-422 and RS-423 generally provide adequate voltage and current for operating the HCPL-2602. Most drivers also have characteristics allowing the HCPL-2602 to be connected directly to the driver terminals. Worst case drive conditions, however, would require current shunting to prevent overstress of the HCPL-2602.



	R = 0, C = 0			R = 32Ω, C = 0			R = 33Ω, C = 430 pF			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	40	50	75	40	50	100	30	45	75	nsec
t_{PLH}	45	65	175	40	50	80	40	45	75	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

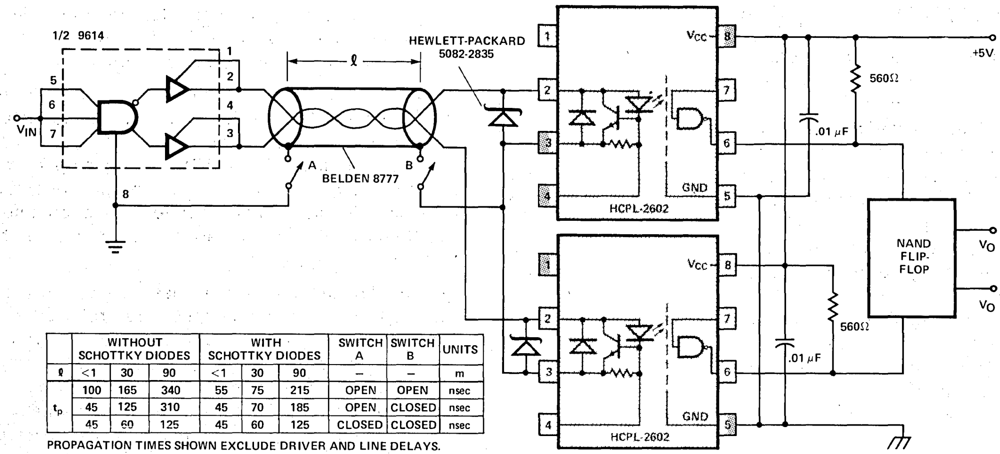
Figure a. Polarity Non-Reversing.



	WITHOUT SCHOTTKY DIODE			WITH SCHOTTKY DIODE						UNITS
	R = 0			R = 0			R = 33Ω			
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	210	365	450	50	80	235	50	70	200	nsec
t_{PLH}	35	45	60	35	45	60	35	45	60	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

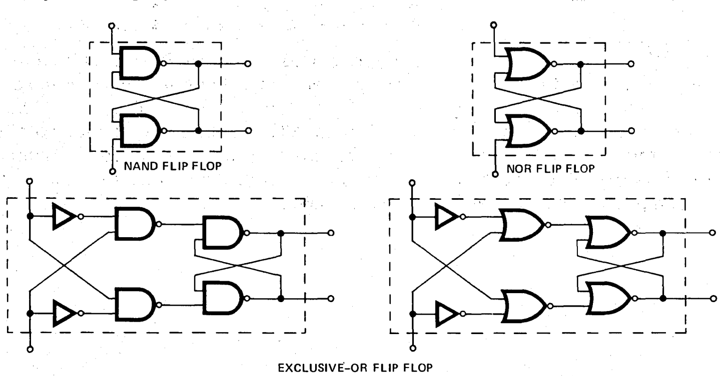
Figure b. Polarity Reversing, Single Ended.



	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	<1	30	90	<1	30	90	–	–	m
t_p	100	165	340	55	75	215	OPEN	OPEN	nsec
	45	125	310	45	70	185	OPEN	CLOSED	nsec
	45	60	125	45	60	125	CLOSED	CLOSED	nsec

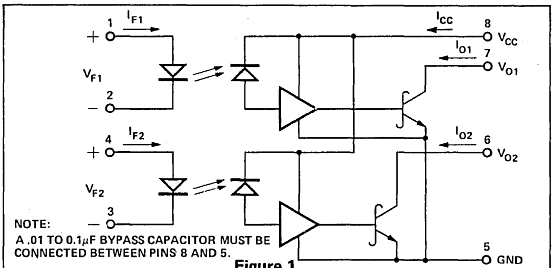
PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure c. Polarity Reversing, Split Phase.



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

Figure d. Flip Flop Configurations.



NOTE: A .01 TO 0.1μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5.

Figure 1.

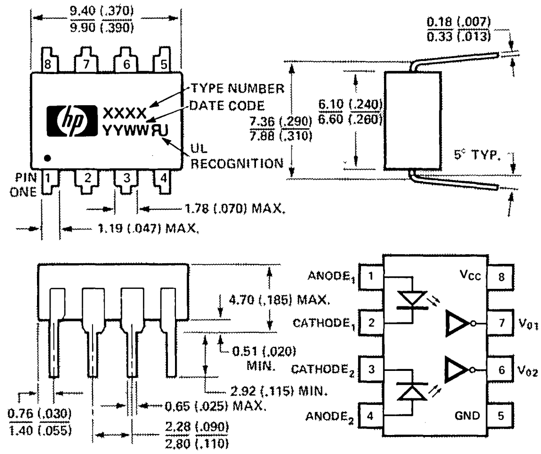
DUAL TTL COMPATIBLE OPTOCOUPLER

HCPL-2630

TECHNICAL DATA JANUARY 1986

OPTOCOUPLERS

OUTLINE DRAWING



DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- HIGH DENSITY PACKAGING
- LSTTL/TTL COMPATIBLE: 5V SUPPLY
- HIGH SPEED: 10 MBd TYPICAL
- LOW INPUT CURRENT REQUIRED: 5 mA
- GUARANTEED PERFORMANCE OVER TEMPERATURE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Description/Applications

The HCPL-2630 consists of a pair of inverting optically coupled gates each with a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving LSTTL/TTL circuit compability. The coupler operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5 mA in each channel will sink an eight gate fan-out (13 mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

The HCPL-2630 can be used in high speed digital interface applications where common mode signals must be rejected such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished between system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, strobing and "WIRED-OR" connection. In all applications, the dual channel configuration allows for high density packaging, increased convenience and more usable board space.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

(No derating required up to 70°C)

Storage Temperature .... -55°C to +125°C
Operating Temperature .... 0°C to +70°C
Lead Solder Temperature .... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current (each channel) ..... 30 mA (≤ 1 msec Duration)
Average Forward Input Current (each channel) ..... 15 mA
Reverse Input Voltage (each channel) 5V
Supply Voltage – V_{CC} .... 7V (1 Minute Maximum)
Output Current – I_O (each channel) .... 16 mA
Output Voltage – V_O (each channel) 7V
Output Collector Power Dissipation .... 60 mW

*6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		2	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250μA		3
Low Level Output Voltage	V_{OL}		0.5	0.6	V	V_{CC} = 5.5V, I_F = 5mA I_{OL} (Sinking) = 13mA	3	3
High Level Supply Current	I_{CCH}		14	30	mA	V_{CC} = 5.5V, I_F = 0 (Both Channels)		
Low Level Supply	I_{CCL}		28	36	mA	V_{CC} = 5.5V, I_F = 10mA (Both Channels)		
Input-Output Insulation	$I_{I\text{-}O}$*			1	μA	45% RH, t = 5s, $V_{I\text{-}O}$ = 3 kV dc, T_A = 25°C		4,9
OPT 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50% t = 1 MIN		10
Resistance (Input-Output)	$R_{I\text{-}O}$		10^{12}		Ω	$V_{I\text{-}O}$ = 500V, T_A = 25°C		4
Capacitance (Input-Output)	$C_{I\text{-}O}$		0.6		pF	f = 1MHz, T_A = 25°C		4
Input Forward Voltage	V_F		1.5	1.75	V	I_F = 10mA, T_A = 25°C	4	7,3
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10μA, T_A = 25°C		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1MHz		3
Input-Input Insulation Leakage Current	$I_{I\text{-}I}$		0.005		μA	Relative Humidity = 45%, t=5s, $V_{I\text{-}I}$=500V		8
Resistance (Input-Input)	$R_{I\text{-}I}$		10^{11}		Ω	$V_{I\text{-}I}$ = 500V		8
Capacitance (Input-Input)	$C_{I\text{-}I}$		0.25		pF	f = 1MHz		8
Current Transfer Ratio	CTR		700		%	I_F = 5.0mA, R_L = 100Ω	2	6

*For JEDEC registered parts.

**All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics at T_A=25°C, V_{CC}=5V

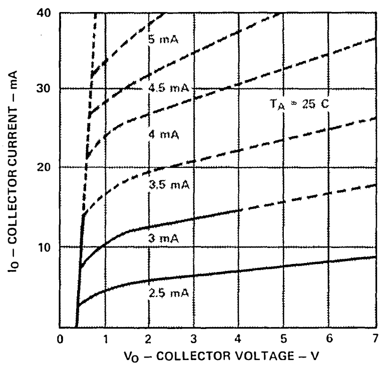
EACH CHANNEL

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		55	75	ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA	6,7	1
Propagation Delay Time to Low Output Level	t_{PHL}		55	75	ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA	6,7	2
Output Rise Time (10-90%)	t_r		50		ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA		
Output Fall Time (90-10%)	t_f		20		ns			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$		100		V/μs	V_{CM} = 10$V_{p\text{-}p}$, R_L = 350 Ω, V_O (min.) = 2V, I_F = 0mA	9	5
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$		300		V/μs	V_{CM} = 10$V_{p\text{-}p}$, R_L = 350 Ω, V_O (max.) = 0.8V I_F = 7.5mA	9	5

NOTE: It is essential that a bypass capacitor (.01μF to 0.1μF, ceramic) be connected from pin 8 to pin 5. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm. Failure to provide the bypass may impair the switching properties (Figure 5).

NOTES:

1. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
6. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
7. At 10mA VF decreases with increasing temperature at the rate of 1.6mV/°C.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
10. See Option 010 data sheet for more information.



NOTE: Dashed characteristics indicate pulsed operation.

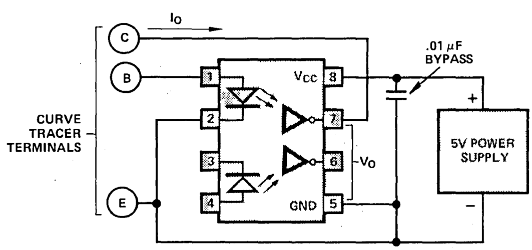
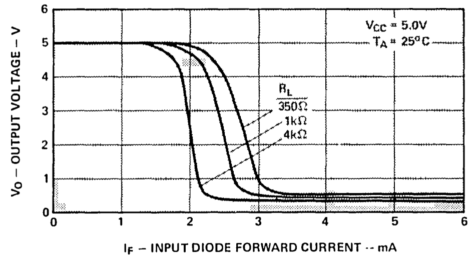


Figure 2. Optocoupler Transfer Characteristics.



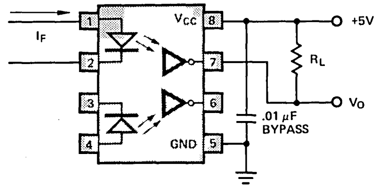


Figure 3. Input-Output Characteristics.

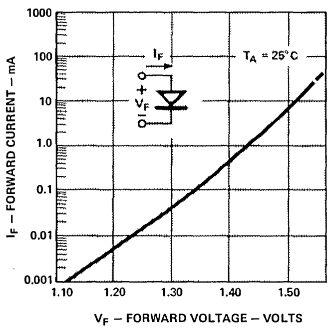


Figure 4. Input Diode Forward Characteristic

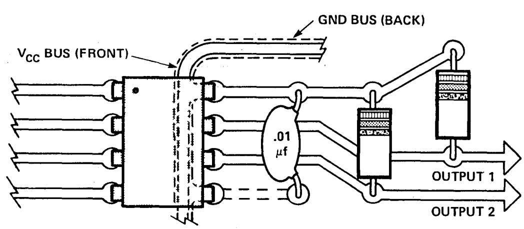


Figure 5. Recommended Printed Circuit Board Layout.

OPTOCOUPLERS

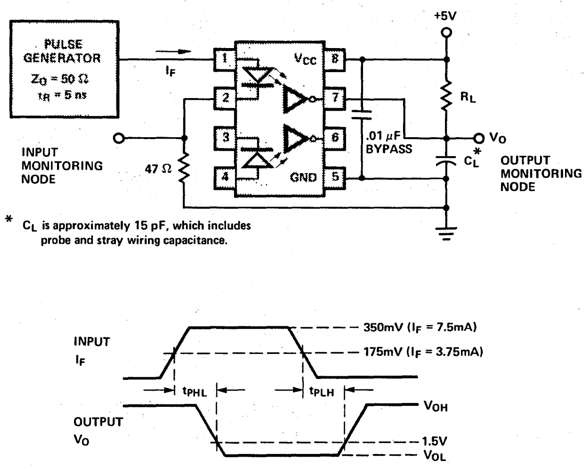


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

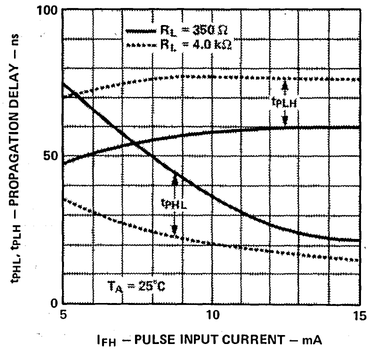


Figure 7. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

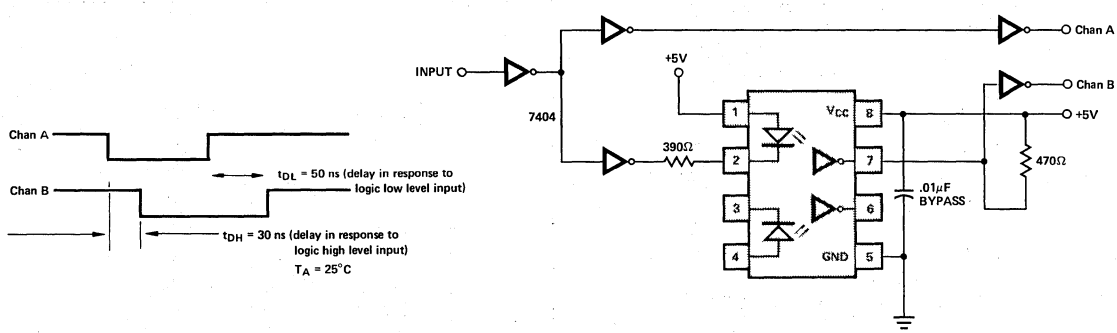


Figure 8. Response Delay Between TTL Gates.

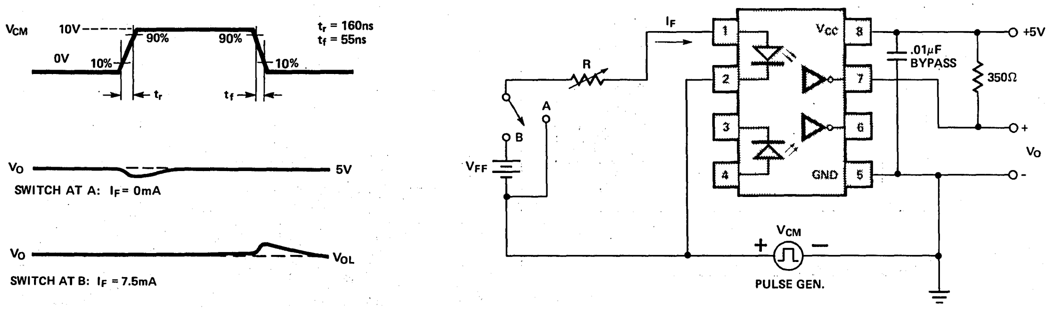


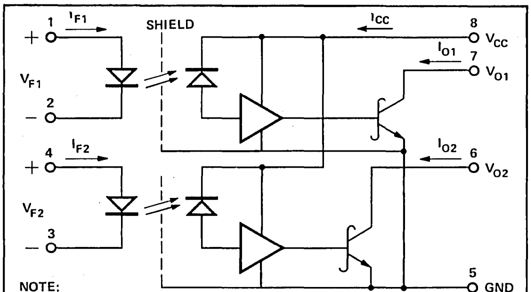
Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

DUAL CHANNEL HIGH CMR HIGH SPEED OPTOCOUPLER

HCPL-2631

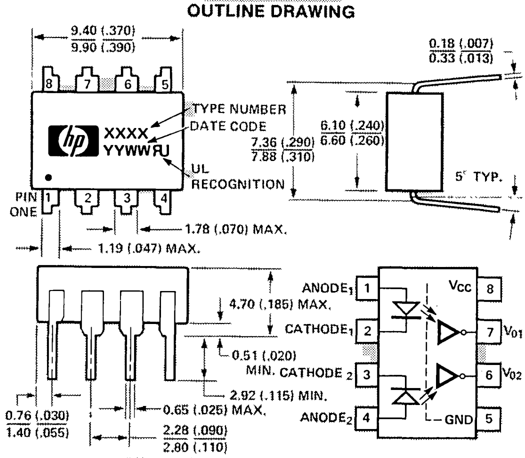
TECHNICAL DATA JANUARY 1986



NOTE:
A .01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5. SEE NOTE 1.

Figure 1. Schematic

OUTLINE DRAWING



DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION (CMR)
- HIGH DENSITY PACKAGING
- HIGH SPEED: 10 MBd TYPICAL
- LSTTL AND TTL COMPATIBLE
- GUARANTEED MINIMUM COMMON MODE TRANSIENT IMMUNITY: 1000 V/μs
- GUARANTEED PERFORMANCE OVER TEMPERATURE 0° C to 70° C
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Applications

- ISOLATION OF HIGH SPEED LOGIC SYSTEMS
- MICROPROCESSOR SYSTEM INTERFACES
- ISOLATED LINE RECEIVER
- COMPUTER-PERIPHERAL INTERFACES
- GROUND LOOP ELIMINATION

Description

The HCPL-2631 is a dual channel optically coupled logic gate that combines GaAsP light emitting diodes and integrated high gain photodetectors. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/μs. The unique design provides maximum DC and AC circuit isolation while achieving LSTTL and TTL logic compatibility. The logic isolation is achieved with a typical propagation delay of 40 nsec. The dual channel design saves space and results in increased convenience.

The HCPL-2631 is recommended for high speed logic interfacing, input/output buffering and for use as line receivers in environments that conventional line receivers cannot tolerate. The HCPL-2631 can be used for the digital programming of machine control systems, motors, and floating power supplies. The internal shield makes the HCPL-2631 ideal for use in extremely high ground or induced noise environments.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		8	
Operating Temperature	T_A	0	70	°C

*6.3 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5 mA or less.

Absolute Maximum Ratings

(No derating required up to 70° C)

Storage Temperature .... −55° C to +125° C
Operating Temperature .... 0° C to +70° C
Lead Solder Temperature .... 260° C for 10s
(1.6 mm below seating plane)
Average Forward
Input Current (each channel) ...... 15 mA (See Note 2)
Reverse Input Voltage (each channel) .... 5 V
Supply Voltage — V_{CC} .... 7 V (1 Minute Maximum)
Output Current — I_O (each channel) .... 16 mA
Output Voltage — V_O (each channel) .... 7 V
Output Collector Power Dissipation
(each channel) .... 40 mW

Electrical Characteristics

(Over Recommended Temperature, $T_A = 0°C$ to $+70°C$, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
Low Level Output Voltage	V_{OL}		0.4	0.6	V	$V_{CC} = 5.5V$, $I_F = 5$ mA I_{OL} (Sinking) = 13 mA	2, 3	3
High Level Output Current	I_{OH}		20	250	μA	$V_{CC} = 5.5V$, $V_O = 5.5$ V, $I_F = 250$ μA	4	3
High Level Supply Current	I_{CCH}		20	30	mA	$V_{CC} = 5.5V$, $I_F = 0$, (Both Channels)		
Low Level Supply Current	I_{CCL}		30	38	mA	$V_{CC} = 5.5V$, $I_F = 10$ mA, (Both Channels)		
Input Forward Voltage	V_F		1.5	1.75	V	$I_F = 10$ mA, $T_A = 25°C$	5	3
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10$ μA, $T_A = 25°C$		3
Input Capacitance	C_{IN}		60		pF	$V_F = 0$, f = 1 MHz		3
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.6		mV/°C	$I_F = 10$ mA		
Input-Output Insulation	$I_{I\text{-}O}$*			1	μA	45% RH, t = 5s, $V_{I\text{-}O} = 3$ kV dc, $T_A = 25°C$		4, 5
OPT 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50% t = 1 MIN		13
Input-Input Leakage Current	$I_{I\text{-}I}$		0.005		μA	Relative Humidity = 45% t = 5 s, $V_{I\text{-}I} = 500$ V		6
Resistance (Input-Input)	$R_{I\text{-}I}$		10^{11}		Ω	$V_{I\text{-}I} = 500$ V		6
Capacitance (Input-Input)	$C_{I\text{-}I}$		0.25		pF	f = 1 MHz		
Resistance (Input-Output)	$R_{I\text{-}O}$		10^{12}		Ω	$V_{I\text{-}O} = 500$ V		4
Capacitance (Input-Output)	$C_{I\text{-}O}$		0.6		pF	f = 1 MHz		

*For JEDEC registered parts. ** All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

Switching Characteristics ($T_A = 25°C$, $V_{CC} = 5$ V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		40	75	ns	$R_L = 350Ω$ $C_L = 15$ pF $I_F = 7.5$ mA	6	3, 7
Propagation Delay Time to Low Output Level	t_{PHL}		40	75	ns		6	3, 8
Output Rise Time (10-90%)	t_r		20		ns			3
Output Fall Time (90-10%)	t_f		30		ns			3
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	1000	10,000		V/μs	$V_{CM} = 50$ V (peak), V_O (min.) = 2 V, $R_L = 350$ Ω, $I_F = 0$ mA	10	3, 9, 11
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L \rvert$	1000	10,000		V/μs	$V_{CM} = 50$ V (peak), V_O (max.) = 0.8 V, $R_L = 350$ Ω, $I_F = 7.5$ mA	10	3, 10, 11

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 14. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply. Failure to provide the bypass may impair the switching properties.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
6. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
7. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., $V_{OUT} > 2.0$ V).
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., $V_{OUT} > 0.8$ V).
11. For sinusoidal voltages, $\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM}$ (p-p)
12. As illustrated in Figure 14, the V_{CC} and GND traces can be located between the input and the output leads of the HCPL-2631 to provide additional noise immunity at the compromise of insulation capability.
13. See Option 010 data sheet for more information.

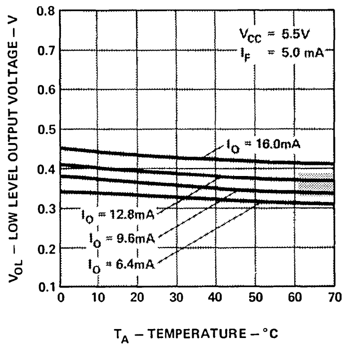


Figure 2. Low Level Output Voltage vs. Temperature

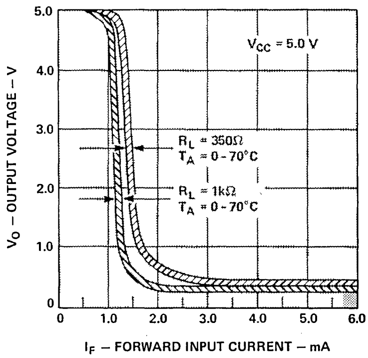


Figure 3. Output Voltage vs. Forward Input Current

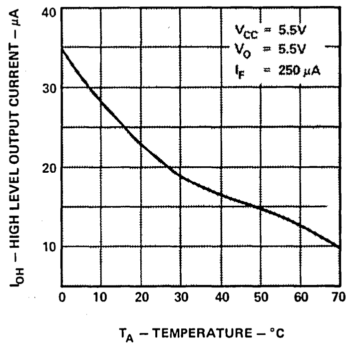


Figure 4. High Level Output Current vs. Temperature

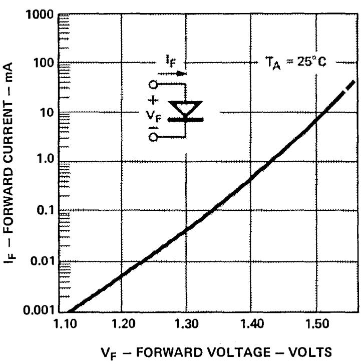


Figure 5. Input Diode Forward Characteristic

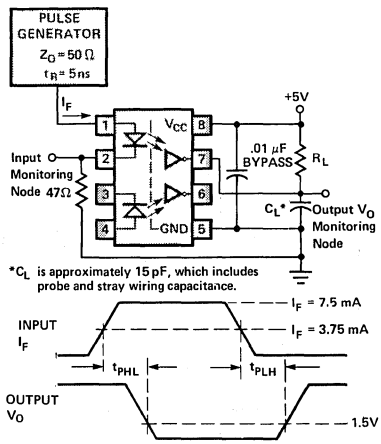


Figure 6. Test Circuit for t_{PHL} and t_{PLH}. Note 3

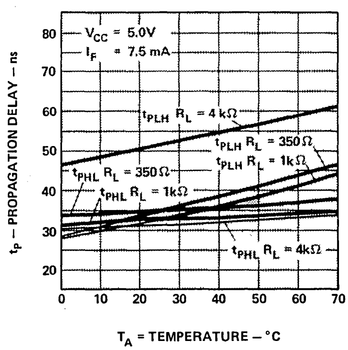


Figure 7. Propagation Delay vs. Temperature

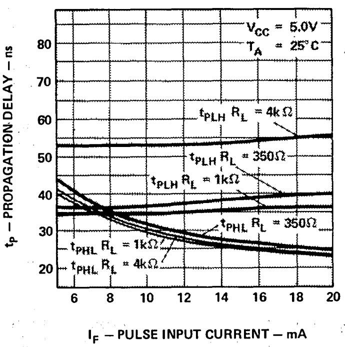


Figure 8. Propagation Delay vs. Pulse Input Current

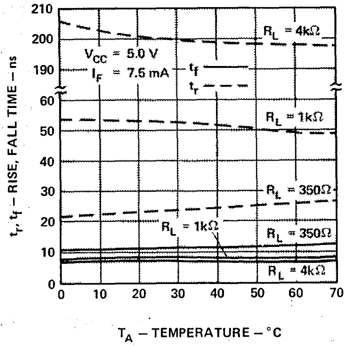


Figure 9. Rise, Fall Time vs. Temperature

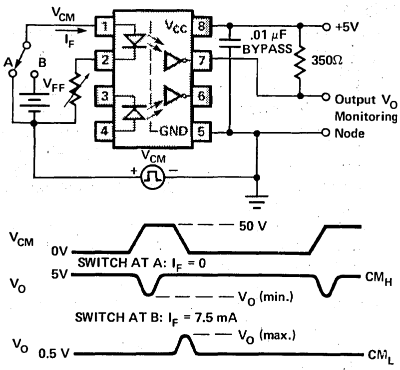


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms. Note 3

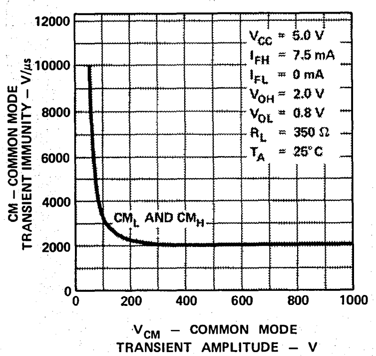
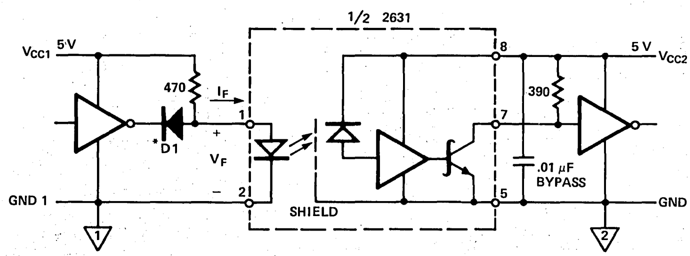


Figure 11. Common Mode Transient Immunity vs. Common Mode Transient Amplitude



*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 12. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit

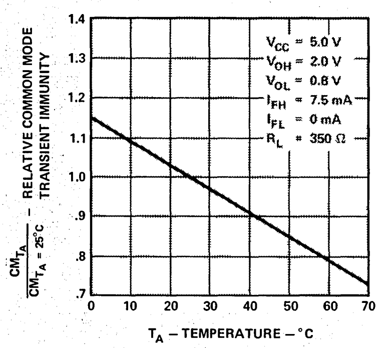
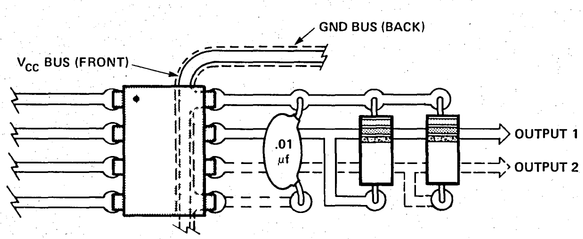


Figure 13. Relative Common Mode Transient Immunity vs. Temperature



NOTES 1, 12

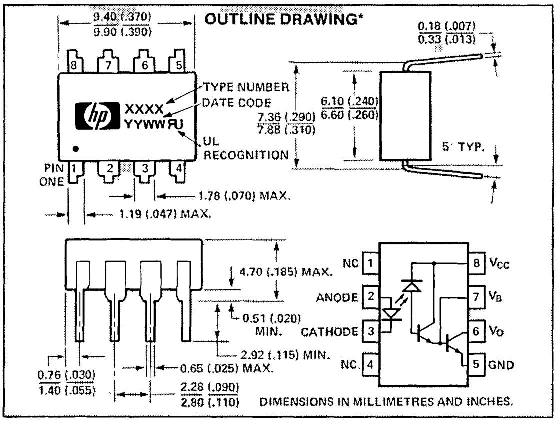
Figure 14. Recommended Printed Circuit Board Layout

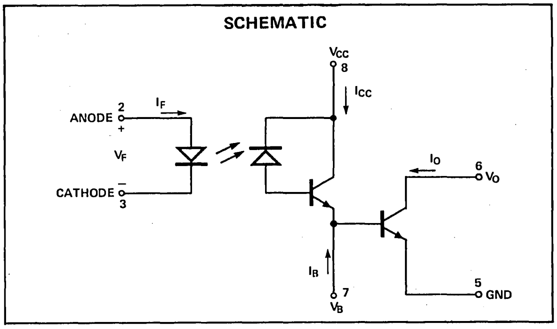
HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

6N138
6N139

TECHNICAL DATA JANUARY 1986





Features

- HIGH CURRENT TRANSFER RATIO—2000% TYPICAL
- LOW INPUT CURRENT REQUIREMENT — 0.5 mA
- TTL COMPATIBLE OUTPUT — 0.1 V V_{OL} TYPICAL
- HIGH COMMON MODE REJECTION — 500 V/μs
- PERFORMANCE GUARANTEED OVER TEMPERATURE 0° C to 70° C
- BASE ACCESS ALLOWS GAIN BANDWIDTH ADJUSTMENT
- HIGH OUTPUT CURRENT — 60 mA
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photon detector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70° C operating range for only 0.5 mA of LED current.

The 6N138 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70° C for an LED current of 1.6 mA [1 TTL Unit load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. out with a 2.2 kμ pull-up resistor.

Applications

- Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL
- Low Input Current Line Receiver – Long Line or Party line
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator – Low Input Power Dissipation
- Low Power Systems – Ground Isolation

Absolute Maximum Ratings *

Storage Temperature	−55°C to +125°C
Operating Temperature	0°C to +70°C
Lead Solder Temperature	260°C for 10s (1.6mm below seating plane)
Average Input Current – I_F	20mA [1]
Peak Input Current – I_F	40mA (50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F	1.0A (≤ 1μs pulse width, 300 pps)
Reverse Input Voltage – V_R	5V
Input Power Dissipation	35mW [2]
Output Current – I_O (Pin 6)	60mA [3]
Emitter-Base Reverse Voltage (Pin 5-7)	0.5V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)	
6N138	−0.5 to 7V
6N139	−0.5 to 18V
Output Power Dissipation	100mW [4]

See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

*JEDEC Registered Data.

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C to 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N139	400	2000		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V	3	5,6
			500	1600			I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
		6N138	300	1600		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}	6N139		0.1	0.4	V	I_F = 1.6mA, I_O = 6.4mA, V_{CC} = 4.5V	1,2	6
				0.1	0.4		I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V		
				0.2	0.4		I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V		
		6N138		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}*	6N139		0.05	100	μA	I_F = 0mA, V_O = V_{CC} = 18V		6
		6N138		0.1	250	μA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}			0.4		mA	I_F = 1.6mA, V_O = Open, V_{CC} = 5V		6
Logic High Supply Current	I_{CCH}			10		nA	I_F = 0mA, V_O = Open, V_{CC} = 5V		6
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	4	
Input Reverse Breakdown Voltage	BV_R*		5		V		I_R = 10μA, T_A=25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			−1.8		mV/°C	I_F = 1.6mA		
Input Capacitance	C_{IN}			60		pF	f=1MHz, V_F = 0		
Input-Output Insulation	I_{I-O}*				1	μA	45% RH, t = 5s, V_{I-O} = 3kV dc, T_A = 25°C		7,11
OPT. 010	V_{ISO}	2500				V_{RMS}	RH ≤ 50%, t = 1 min.		12
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7

*For JEDEC registered parts. **All typicals at T_A = 25°C and V_{CC} = 5V, unless otherwise noted.

Switching Specifications

AT T_A = 25° C, V_{CC} = 5V

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}*	6N139		5	25	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	6,8
				0.2	1		I_F = 12mA, R_L = 270Ω		
		6N138		1.6	10	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}*	6N139		18	60	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	6,8
				2	7		I_F = 12mA, R_L = 270Ω		
		6N138		10	35	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Common Mode Transient Immunity at Logic High Level Output	$\lvert CM_H \rvert$			500		V/μs	I_F = 0mA, R_L = 2.2kΩ, R_{CC} = 0, $\lvert V_{cm} \rvert$ = $10V_{p-p}$	10	9,10
Common Mode Transient Immunity at Logic Low Level Output	$\lvert CM_L \rvert$			500		V/μs	I_F = 1.6mA, R_L = 2.2kΩ, R_{CC} = 0, $\lvert V_{cm} \rvert$ = $10V_{p-p}$	10	9,10

NOTES:

1. Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 7 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
10. In applications where dV/dt may exceed 50,000V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.15\ I_F\ (mA)}$ kΩ.
11. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
12. See Option 010 data sheet for more information.

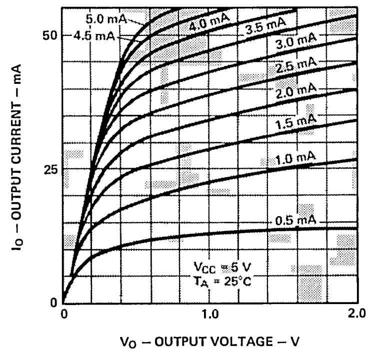


Figure 1. 6N138/6N139 DC Transfer Characteristics

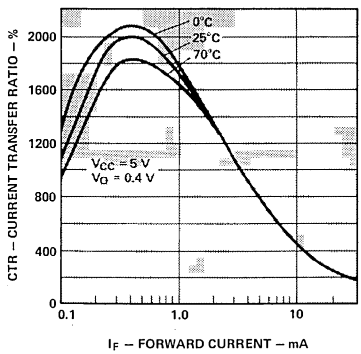


Figure 2. Current Transfer Ratio vs Forward Current 6N138/6N139

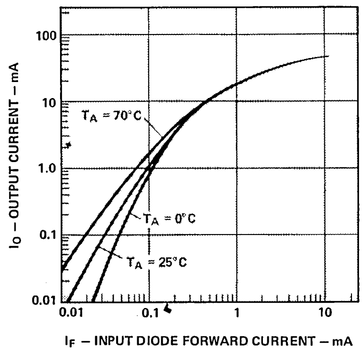


Figure 3. 6N138/6N139 Output Current vs Input Diode Forward Current

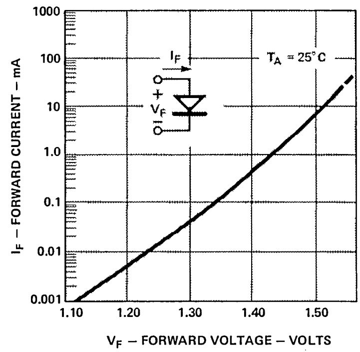


Figure 4. Input Diode Forward Current vs. Forward Voltage.

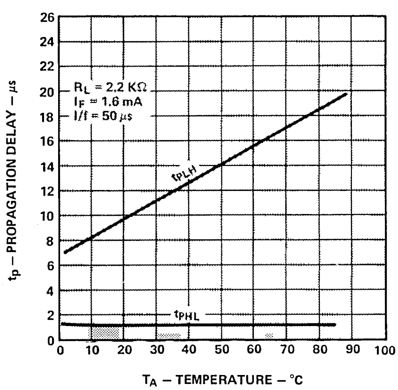


Figure 5. Propagation Delay vs. Temperature.

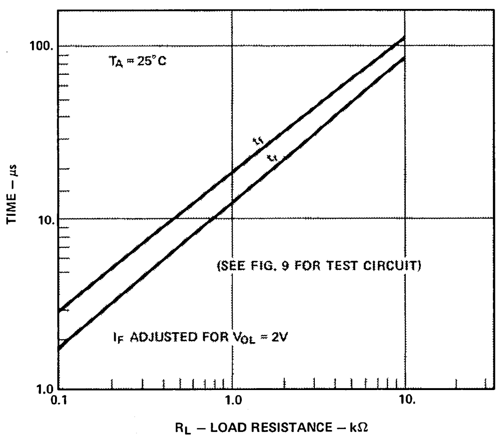


Figure 6. Non Saturated Rise and Fall Times vs. Load Resistance.

OPTOCOUPLERS

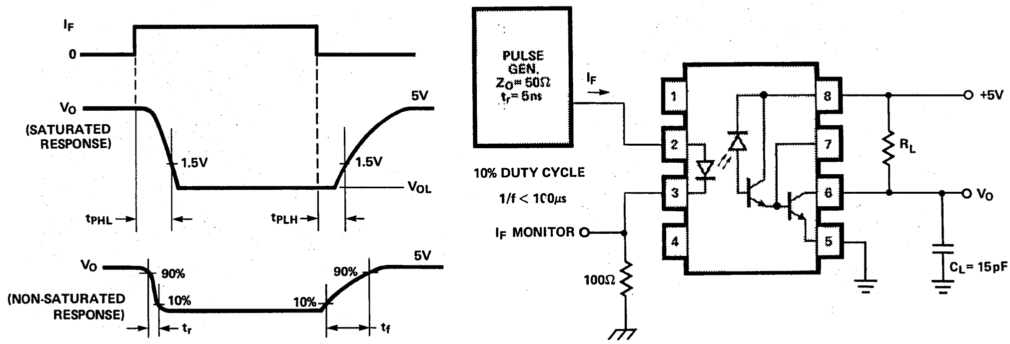


Figure 7. Switching Test Circuit.*

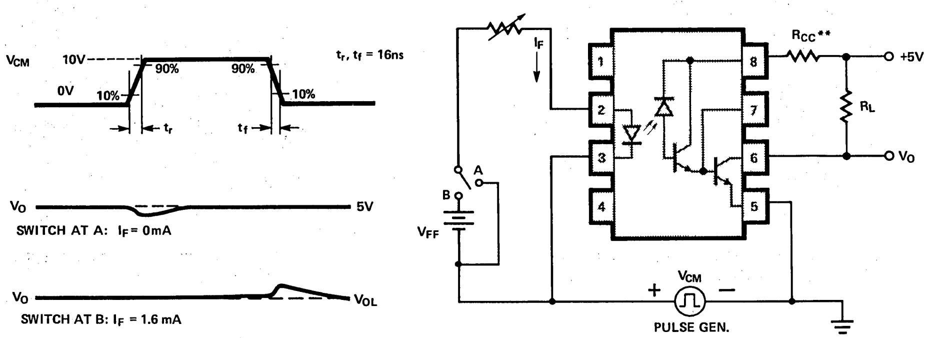


Figure 8. Test Circuit for Transient Immunity and Typical Waveforms.

*JEDEC Registered Data.

**See Note 10

HEWLETT PACKARD

DUAL LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

HCPL-2730 HCPL-2731

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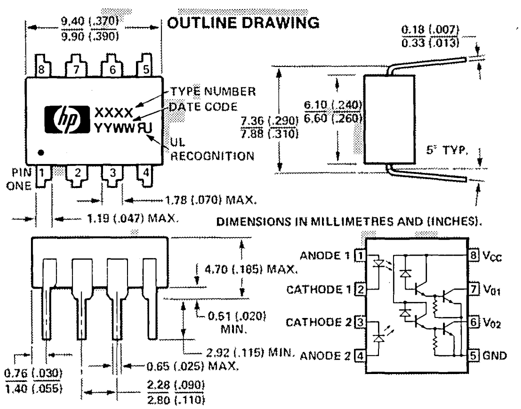
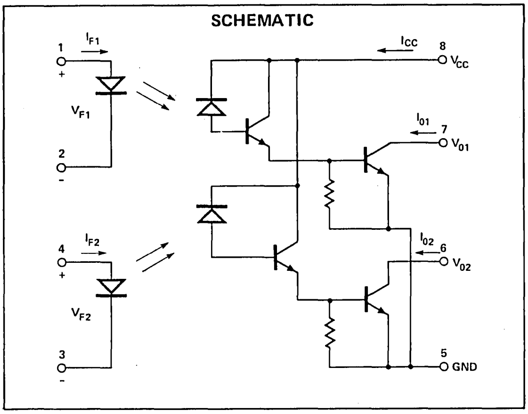




Features

- HIGH CURRENT TRANSFER RATIO — 1800% TYPICAL
- LOW INPUT CURRENT REQUIREMENT — 0.5 mA
- LOW OUTPUT SATURATION VOLTAGE — 0.1V TYPICAL
- HIGH DENSITY PACKAGING
- PERFORMANCE GUARANTEED OVER 0°C TO 70°C TEMPERATURE RANGE
- HIGH COMMON MODE REJECTION — 500 V/μS
- LSTTL COMPATIBLE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Applications

- Digital Logic Ground Isolation
- Telephone Ring Detector
- EIA RS-232C Line Receiver
- Low Input Current Line Receiver — Long Line or Party Line
- Microprocessor Bus Isolation
- Current Loop Receiver
- Polarity Sensing
- Level Shifting
- Line Voltage Status Indicator — Low input Power Dissipation

Description

The HCPL-2730/31 dual channel couplers contain a separated pair of GaAsP light emitting diodes optically coupled to a pair of integrated high gain photon detectors. They provide extremely high current transfer ratio, 3000V dc withstand test voltage and excellent input-output common mode transient immunity. A separate pin for the photodiodes and first gain stages (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photodarlington type isolators. In addition V_{CC} may be as low as 1.6V without adversely affecting the parametric performance.

Guaranted operation at low input currents and the high current transfer ratio (CTR) reduce the magnitude and effects of CTR degradation.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The HCPL-2731 has a 400% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current application such as MOS, CMOS and low power logic interfacing or RS232C data transmission systems. In addition, the high CTR and high output current capability make this device extremely useful in applications where a high fanout is required. Compatibility with high voltage CMOS logic systems is guaranteed by the 18V V_{CC} and V_O specifications and by testing output high leakage (I_{OH}) at 18V.

The HCPL-2730 is specified at an input current of 16 mA and has a 7V V_{CC} and V_O rating. The 300% mimimum CTR allows TTL to TTL interfacing with an input current of only 1.6 mA.

Important specifications such as CTR, leakage current and output saturation voltage are guaranteed over the 0°C to 70°C temperature range to allow trouble-free system operation.

Electrical Specifications

(Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2731	400	1800		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V	2	6,7
			500	1600			I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
		2730	300	1600		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	2	
Logic Low Output Voltage	V_{OL}	2731		0.1	0.4	V	I_F = 1.6mA, I_O = 8mA, V_{CC} = 4.5V	1	6
				0.1	0.4		I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V		
				0.2	0.4		I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V		
		2730		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}	2731		0.005	100	µA	I_F = 0 mA, V_O = V_{CC} = 18V		6
		2730		0.01	250	µA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}	2731		1.2		mA	I_{F1} = I_{F2} = 1.6mA; V_{CC} = 18V		
		2730		0.9			V_{01} = V_{02} = Open; V_{CC} = 7V		
Logic High Supply Current	I_{CCH}	2731		5		nA	I_{F1} = I_{F2} = 0mA; V_{CC} = 18V		
		2730		4			V_{01} = V_{02} = Open; V_{CC} = 7V		
Input Forward Voltage	V_F			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	4	6
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA, T_A = 25°C		6
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6mA		6
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		6
Input-Output Insulation	$I_{I\text{-}O}$*				1	µA	45% RH, t = 5s, $V_{I\text{-}O}$ = 3kV dc, T_A = 25°C		8,12
OPT. 010	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min.		13
Resistance (Input-Output)	$R_{I\text{-}O}$			10^{12}		Ω	$V_{I\text{-}O}$ = 500Vdc		8
Capacitance (Input-Output)	$C_{I\text{-}O}$			0.6		pF	f = 1 MHz		8
Input-Input Insulation Leakage Current	$I_{I\text{-}I}$			0.005		µA	45% Relative Humidity, t=5s, $V_{I\text{-}I}$ = 500Vdc		9
Resistance (Input-Input)	$R_{I\text{-}I}$			10^{11}		Ω	$V_{I\text{-}I}$ = 500Vdc		9
Capacitance (Input-Input)	$C_{I\text{-}I}$			0.25		pF	f = 1 MHz		9

*For JEDEC registered parts.

*All typicals at T_A = 25°C

Switching Specifications AT T_A = 25°C, V_{CC} = 5V

Parameter	Sym.	Device HCPL-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	2731		25	100	µs	I_F = 0.5mA, R_L = 4.7kΩ	9	6
		2730/1		5	20	µs	I_F = 1.6mA, R_L = 2.2kΩ		
				0.5	2		I_F = 12mA, R_L = 270Ω		
Propagation Delay Time To Logic High at Output	t_{PLH}	2731		10	60	µs	I_F = 0.5mA, R_L = 4.7kΩ	9	6
		2730/1		10	35	µs	I_F = 1.6mA, R_L = 2.2kΩ		
				1	10		I_F = 12mA, R_L = 270Ω		
Common Mode Transient Immunity at Logic High Level Output	$\lvert CM_H \rvert$			500		V/µs	I_F = 0mA, R_L = 2.2kΩ, $\lvert V_{CM} \rvert$ = $10V_{p\text{-}p}$	10	6, 10, 11
Common Mode Transient Immunity at Logic Low Level Output	$\lvert CM_L \rvert$			500		V/µs	I_F = 1.6mA, R_L = 2.2kΩ, $\lvert V_{CM} \rvert$ = $10V_{p\text{-}p}$	10	6, 10, 11

NOTES:
1. Derate linearly above 50°C free-air temperature at a rate of 0.5mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.9mW/°C.
3. Derate linearly above 35°C free-air temperature at a rate of 0.6mA/°C.
4. Pin 5 should be the most negative voltage at the detector side.
5. Derate linearly above 35°C free-air temperature at a rate of 1.7mW/°C. Output power is collector output power plus supply power.
6. Each channel.
7. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
8. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
9. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
10. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
11. In applications where dV/dt may exceed 50,000 V/µs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.3\, I_F\ (mA)}$ kΩ.
12. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
13. See Option 010 data sheet for more information.

Absolute Maximum Ratings

Storage Temperature .... -55°C to +125°C
Operating Temperature .... -40°C to +85°C
Lead Solder Temperature .... 260°C for 10 sec (1.6mm below seating plane)
Average Input Current — I_F (each channel) .... 20 mA [1]
Peak Input Current — I_F (each channel) .... 40 mA (50% duty cycle, 1 ms pulse width)
Reverse Input Voltage — V_R (each channel) 5V

Input Power Dissipation (each channel) .... 35 mW [2]
Output Current — I_O (each channel) .... 60 mA [3]
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 7,6-5) [4]
HCPL-2730 .... -0.5 to 7V
HCPL-2731 .... -0.5 to 18V
Output Power Dissipation (each channel) .... 100 mW [5]

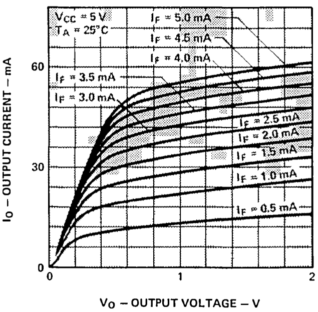


Figure 1. DC Transfer Characteristics (HCPL-2730/HCPL-2731)

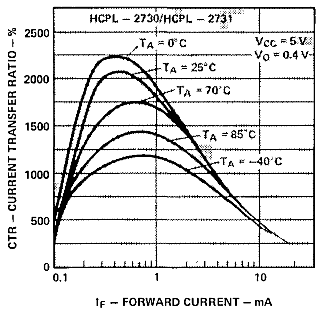


Figure 2. Current Transfer Ratio vs Forward Current

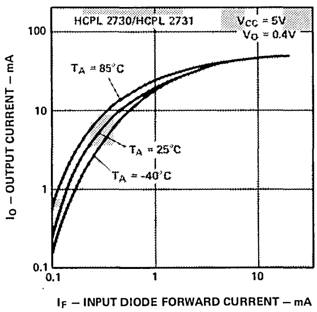


Figure 3. Output Current vs Input Diode Forward Current

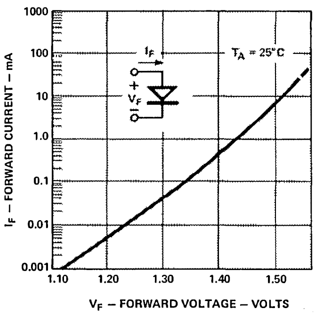


Figure 4. Input Diode Forward Current vs. Forward Voltage.

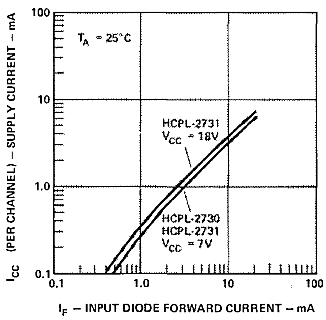


Figure 5. Supply Current Per Channel vs. Input Diode Forward Current.

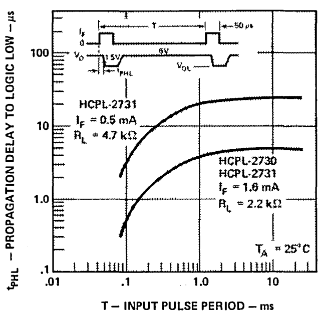


Figure 6. Propagation Delay To Logic Low vs. Pulse Period.

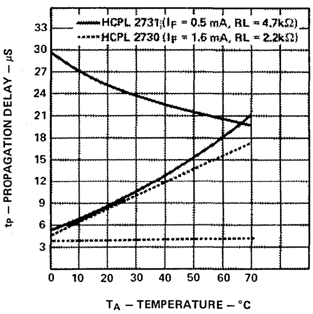


Figure 7. Propagation Delay vs. Temperature.

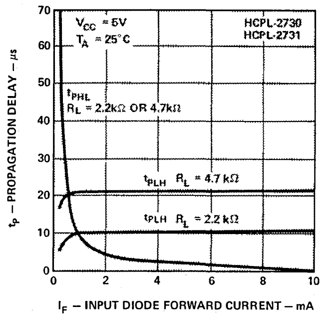


Figure 8. Propagation Delay vs. Input Diode Forward Current.

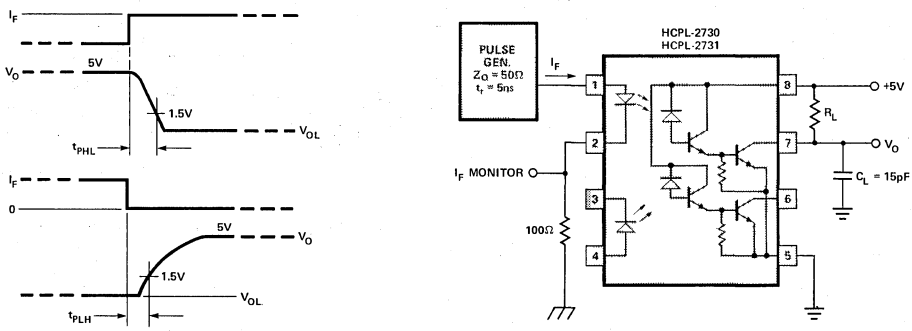
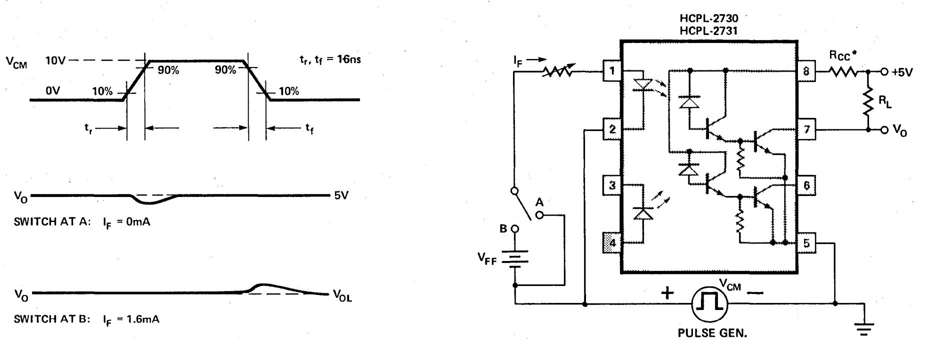


Figure 9. Switching Test Circuit.



*See Note 11.

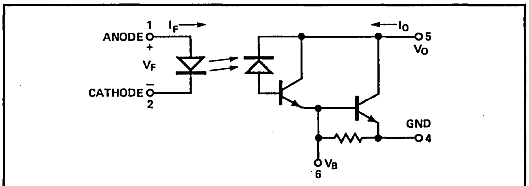
Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLER

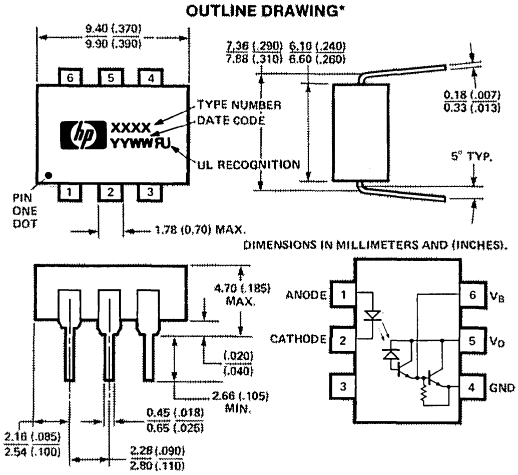
4N45
4N46

TECHNICAL DATA JANUARY 1986



Schematic

OUTLINE DRAWING*



Features

- **HIGH CURRENT TRANSFER RATIO — 1500% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **PERFORMANCE GUARANTEED OVER 0°C TO 70°C TEMPERATURE RANGE**
- **INTERNAL BASE-EMITTER RESISTOR MINIMIZES OUTPUT LEAKAGE**
- **GAIN-BANDWIDTH ADJUSTMENT PIN**
- **HIGH COMMON MODE REJECTION**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).**

Description

The 4N45/46 optocouplers contain a GaAsP light emitting diode optically coupled to a high gain photodetector IC.

The excellent performance over temperature results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground. External access to the second stage base provides better noise rejection than a conventional photodarlington detector. An external resistor or capacitor at the base can be added to make a gain-bandwidth or input current threshold adjustment. The base lead can also be used for feedback.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

The 4N46 has a 350% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing. Compatibility with high voltage CMOS logic systems is assured by the 20V minimum breakdown voltage of the output transistor and by the guaranteed maximum output leakage (I_{OH}) at 18V.

The 4N45 has a 250% minimum CTR at 1.0mA input current and a 7V minimum breakdown voltage rating.

*JEDEC Registered Data.

Applications

- **Telephone Ring Detector**
- **Digital Logic Ground Isolation**
- **Low Input Current Line Receiver**
- **Line Voltage Status Indicator — Low Input Power Dissipation**
- **Logic to Reed Relay Interface**
- **Level Shifting**
- **Interface Between Logic Families**

Absolute Maximum Ratings*

Storage Temperature	-55°C to +125°C
Operating Temperature	-40°C to +70°C
Lead Solder Temperature	260°C for 10 s. (1.6mm below seating plane)
Average Input Current — I_F	20 mA[1]
Peak Input Current — I_F	40 mA (50% duty cycle, 1ms pulse width)
Peak Transient Input Current — I_F	1.0A ($\leqslant$1 µs pulse width, 300pps)
Reverse Input Voltage — V_R	5V
Input Power Dissipation	35mW[2]
Output Current — I_O (Pin 5)	60 mA[3]
Emitter-Base Reverse Voltage (Pins 4-6)	0.5V
Output Voltage — V_O (Pin 5-4)	
4N45	-0.5 to 7V
4N46	-0.5 to 20V
Output Power Dissipation	100mW[4]

See notes, following page

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	4N46	350 500 200	1500 1500 600		%	I_F = 0.5mA, V_O = 1.0V I_F = 1.0mA, V_O = 1.0V I_F = 10mA, V_O = 1.2V	4	5,6
		4N45	250 200	1200 500		%	I_F = 1.0mA, V_O = 1.0V I_F = 10mA, V_O = 1.2V		
Logic Low Output Voltage	V_{OL}	4N46		.90 .92 .95	1.0 1.0 1.2	V	I_F = 0.5mA, I_{OL} = 1.75mA I_F = 1.0mA, I_{OL} = 5.0mA I_F = 10mA, I_{OL} = 20mA	2	6
		4N45		.90 .95	1.0 1.2	V	I_F = 1.0mA, I_{OL} = 2.5mA I_F = 10mA, I_{OL} = 20mA		
Logic High Output Current	I_{OH}*	4N46		.001	100	μA	I_F = 0mA, V_O = 18V		6
		4N45		.001	250	μA	I_F = 0mA, V_O = 5V		
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.0mA, T_A = 25°C	1	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.0mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10μA, T_A = 25°C		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation	I_{I-O}*				1.0	μA	45% RH, t = 5s, V_{I-O} = 3kV dc, T_A = 25°C		7,10
OPT. 010	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min.		11
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500VDC		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7

Switching Specifications

AT T_A = 25° C, V_{CC} = 5.0V

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}		80		μs	I_F = 1.0mA, R_L = 10kΩ	8	6,8
	t_{PHL}*		5	50	μs	I_F = 10mA, R_L = 220Ω		
Propagation Delay Time To Logic High at Output	t_{PLH}		1500		μs	I_F = 1.0mA, R_L = 10kΩ	8	6,8
	t_{PLH}*		150	500	μs	I_F = 10mA, R_L = 220Ω		
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$		500		V/μs	I_F = 0mA, R_L = 10kΩ $\|V_{cm}\|$ = $10V_{p-p}$	9	9
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$		500		V/μs	I_F = 1.0mA, R_L = 10kΩ $\|V_{cm}\|$ = $10V_{p-p}$	9	9

*JEDEC Registered Data.

**All typicals at T_A = 25°C, unless otherwise noted.

NOTES:

1. Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.8mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 1.5mW/°C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 6 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3 shorted together and Pins 4, 5, and 6 shorted together.
8. Use of a resistor between pin 4 and 6 will decrease gain and delay time. (See Figures 10 and 12).
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.5V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., V_O < 2.5V).
10. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
11. See Option 010 data sheet for more information.

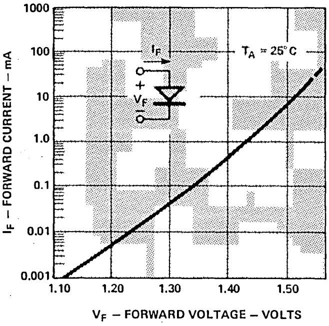


Figure 1. Input Diode Forward Current vs. Forward Voltage.

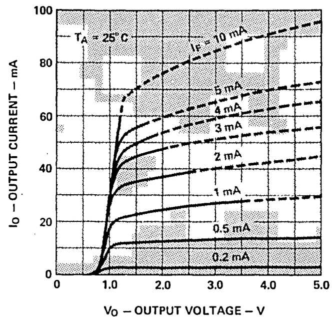


Figure 2. Typical DC Transfer Characteristics.

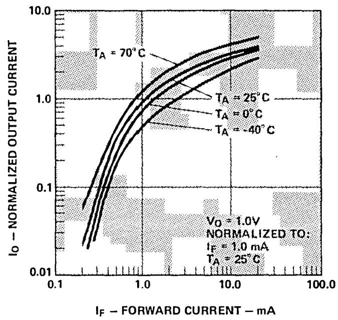


Figure 3. Output Current vs. Input Current.

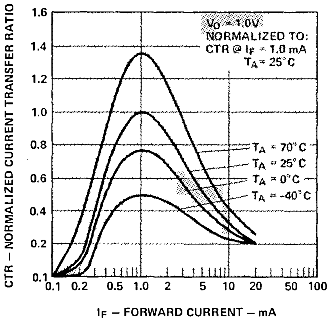


Figure 4. Current Transfer Ratio vs. Input Current.

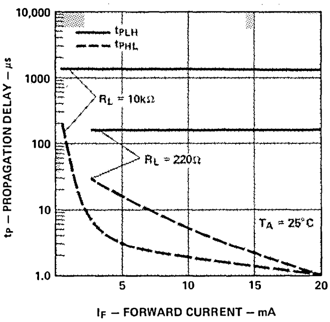


Figure 5. Propagation Delay vs. Forward Current.

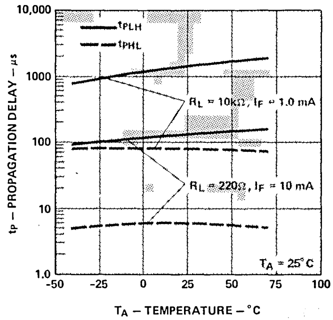


Figure 6. Propagation Delay vs. Temperature.

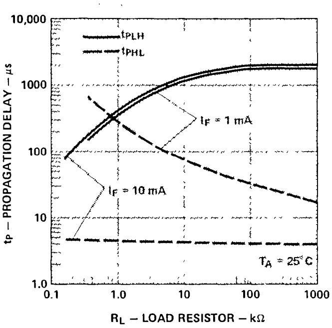


Figure 7. Propagation Delay vs Load Resistor.

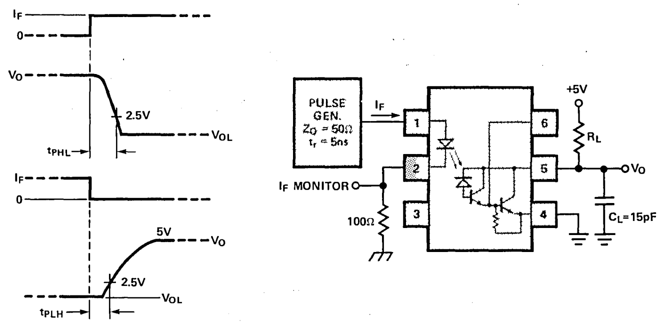


Figure 8. Switching Test Circuit

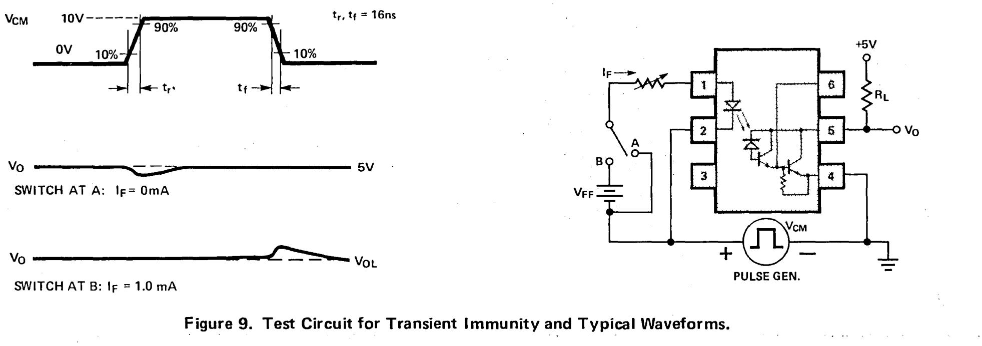


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

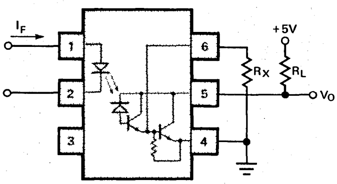


Figure 10. External Base Resistor, R_X

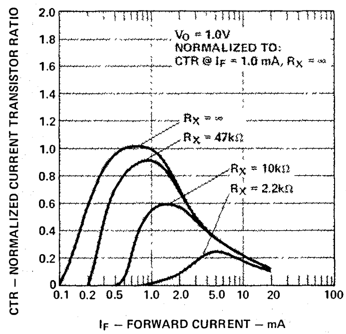


Figure 11. Effect of R_X On Current Transfer Ratio

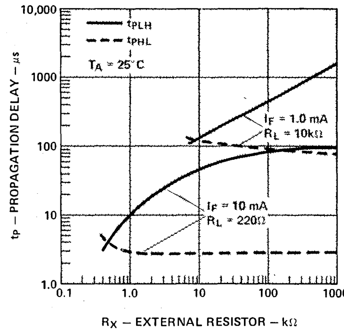
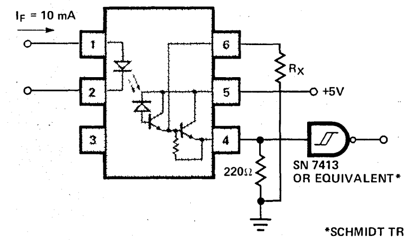


Figure 12. Effect of R_X On Propagation Delay

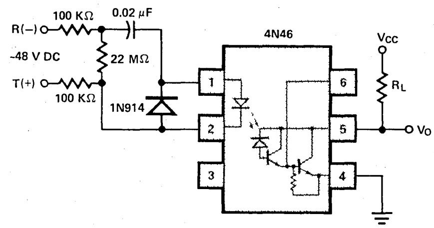
Applications



R_X (kΩ)	t_{PHL} (µs)	t_{PLH} (µs)
∞	5	320
100	5	200
47	5	140
20	6	80
10	6	45

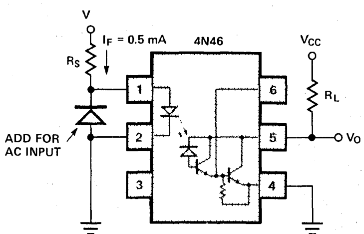
*SCHMIDT TRIGGER RECOMMENDED BECAUSE OF LONG t_r, t_f.

TTL Interface



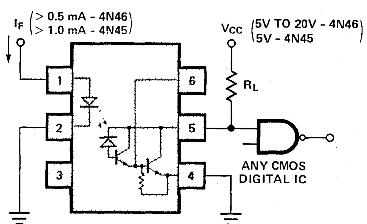
NOTE: AN INTEGRATOR MAY BE REQUIRED AT THE OUTPUT TO ELIMINATE DIALING PULSES AND LINE TRANSIENTS.

Telephone Ring Detector

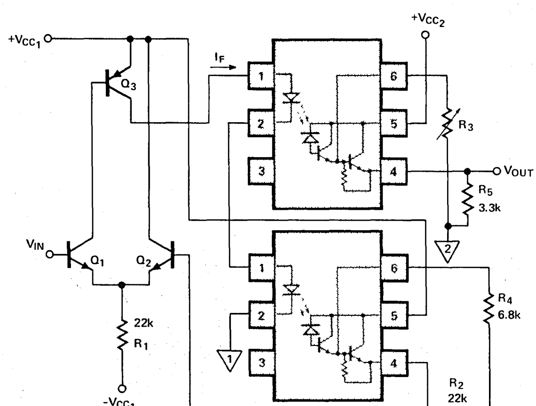


V (Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
115	220kΩ	62
230	470kΩ	113

Line Voltage Monitor



CMOS Interface



Q_1, Q_2 - 2N3904
Q_3 - 2N3906

CHARACTERISTICS

$R_{IN} \approx 30M\Omega$, $R_{OUT} \approx 50\Omega$
$V_{IN(MAX.)} = V_{CC_1} - 1V$, LINEARITY BETTER THAN 5%

DESIGN COMMENTS

R_1 - NOT CRITICAL $\left(<< \frac{V_{IN\ (MAX.)} - (-V_{CC_1}) - V_{BE}}{I_{F\ (MAX.)}}\right) h_{FE}\ Q_3$

R_2 - NOT CRITICAL (OMIT IF 0.2 TO 0.3V OFFSET IS TOLERABLE)

$R_4 > \frac{V_{IN\ (MAX.)} + V_{BE}}{1\ mA}$

$R_5 > \frac{V_{IN\ (MAX.)}}{2.5\ mA}$

NOTE: ADJUST R_3 SO $V_{OUT} = V_{IN}$ AT $V_{IN} = \frac{V_{IN\ (MAX.)}}{2}$

Analog Signal Isolation

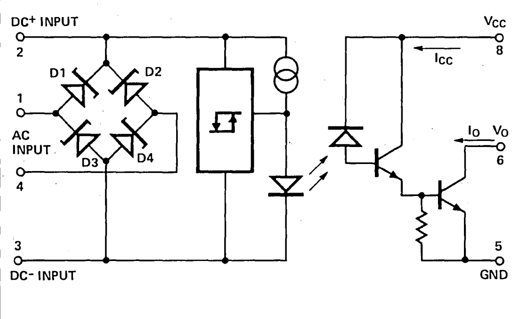
HEWLETT PACKARD

AC/DC TO LOGIC INTERFACE OPTOCOUPLER

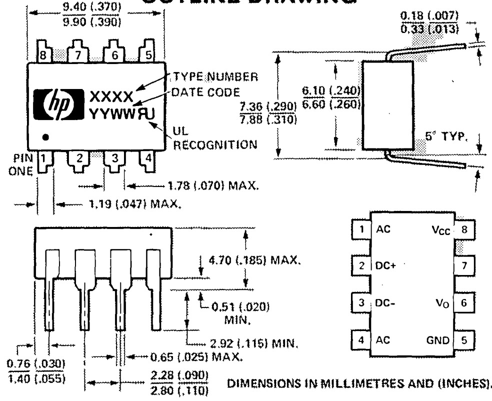
HCPL-3700

TECHNICAL DATA JANUARY 1986

SCHEMATIC



OUTLINE DRAWING



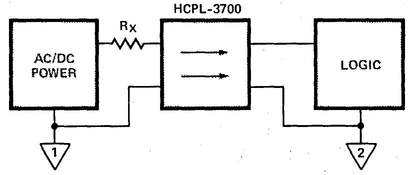
DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- AC OR DC INPUT
- PROGRAMMABLE SENSE VOLTAGE
- HYSTERESIS
- LOGIC COMPATIBLE OUTPUT
- SMALL SIZE: STANDARD 8 PIN DIP
- THRESHOLDS GUARANTEED OVER TEMPERATURE
- THRESHOLDS INDEPENDENT OF LED DEGRADATION
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Applications

- LIMIT SWITCH SENSING
- LOW VOLTAGE DETECTOR
- AC/DC VOLTAGE SENSING
- RELAY CONTACT MONITOR
- RELAY COIL VOLTAGE MONITOR
- CURRENT SENSING
- MICROPROCESSOR INTERFACING
- TELEPHONE RING DETECTION



Description

The HCPL-3700 is a voltage/current threshold detection optocoupler. This optocoupler uses an internal Light Emitting Diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.8 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes effects of different optical gain and LED variations over operating life (CTR degradation). Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with ac voltage input.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

The HCPL-3700, by combining several unique functions in a single package, provides the user with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

Absolute Maximum Ratings (No derating required up to 70°C)

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	°C	
Operating Temperature		T_A	-40	85	°C	
Lead Soldering Cycle	Temperature			260	°C	1
	Time			10	sec	
Input Current	Average	I_{IN}		50	mA	2
	Surge			140		2,3
	Transient			500		
Input Voltage (Pins 2-3)		V_{IN}	-0.5		V	
Input Power Dissipation		P_{IN}		230	mW	4
Total Package Power Dissipation		P		305	mW	5
Output Power Dissipation		P_O		210	mW	6
Output Current	Average	I_O		30	mA	7
Supply Voltage (Pins 8-5)		V_{CC}	-0.5	20	V	
Output Voltage (Pins 6-5)		V_O	-0.5	20	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{CC}	4.5	18	V	
Operating Temperature	T_A	0	70	°C	
Operating Frequency	f	0	4	KHz	8

Switching Characteristics at $T_A = 25°C$, $V_{CC} = 5.0V$

Parameter	Symbol	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		4.0	15	μs	$R_L = 4.7\ k\Omega$, $C_L = 30\ pF$	6,9	10
Propagation Delay Time to Logic High Output Level	t_{PLH}		10.0	40	μs	$R_L = 4.7\ k\Omega$, $C_L = 30\ pF$		11
Common Mode Transient Immunity at Logic Low Output Level	$\|CM_L\|$		600		V/μs	$I_{IN} = 3.11\ mA$, $R_L = 4.7\ k\Omega$ $V_{O\ max.} = 0.8V$, $V_{CM_L} = 140V$	8,10	12,13
Common Mode Transient Immunity at Logic High Output Level	$\|CM_H\|$		4000		V/μs	$I_{IN} = 0\ mA$, $R_L = 4.7\ k\Omega$ $V_{O\ min.} = 2.0V$, $V_{CM_H} = 1400V$		
Output Rise Time (10-90%)	t_r		20		μs	$R_L = 4.7\ k\Omega$, $C_L = 30\ pF$	7	
Output Fall Time (90-10%)	t_f		0.3		μs	$R_L = 4.7\ k\Omega$, $C_L = 30\ pF$		

Electrical Characteristics

Over Recommended Temperature (0°C ≤ T_A ≤ 70°C) Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Input Threshold Current		I_{TH+}	1.96	2.5	3.11	mA	$V_{IN}=V_{TH+}$; V_{CC} = 4.5V; V_O = 0.4V; $I_O \geq$ 4.2 mA	2,3	14
		I_{TH-}	1.00	1.3	1.62	mA	$V_{IN} = V_{TH-}$; V_{CC} = 4.5V; V_O = 2.4V; $I_{OH} \leq$ 100 μA		
Input Threshold Voltage	DC (Pins 2, 3)	V_{TH+}	3.35	3.8	4.05	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5V; V_O = 0.4V; $I_O \geq$ 4.2 mA		
		V_{TH-}	2.01	2.6	2.86	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5V; V_O = 2.4V; $I_O \leq$ 100 μA		
	AC (Pins 1, 4)	V_{TH+}	4.23	5.1	5.50	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5V; V_O = 0.4V; $I_O \geq$ 4.2 mA		14,15
		V_{TH-}	2.87	3.8	4.24	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5V; V_O = 2.4V; $I_O \leq$ 100 μA		
Hysteresis		I_{HYS}		1.2		mA	$I_{HYS} = I_{TH+} - I_{TH-}$	2	
		V_{HYS}		1.2		V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage		V_{IHC1}	5.4	5.9	6.6	V	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1	
		V_{IHC2}	6.1	6.6	7.3	V	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open		
		V_{IHC3}		12.0	13.4	V	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15 mA; Pins 1 & 4 Open		
		V_{ILC}		-0.76		V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Input Current		I_{IN}	3.0	3.7	4.4	mA	$V_{IN} = V_2 - V_3$ = 5.0V; Pins 1 & 4 Open	5	
Bridge Diode Forward Voltage		$V_{D1,2}$		0.59			I_{IN} = 3 mA (see schematic)		
		$V_{D3,4}$		0.74					
Logic Low Output Voltage		V_{OL}		0.1	0.4	V	V_{CC} = 4.5V; I_{OL} = 4.2 mA	5	14
Logic High Output Current		I_{OH}			100	μA	$V_{OH} = V_{CC}$ = 18V		
Logic Low Supply Current		I_{CCL}		1.2	4	mA	$V_2 - V_3$ = 5.0V; V_O = Open V_{CC} = 5.0V		
Logic High Supply Current		I_{CCH}		0.002	4	μA	V_{CC} = 18V; V_O = Open	4	14
Input-Output Insulation		$I_{I\text{-}O}$*			1	μA	45% RH, t = 5s, $V_{I\text{-}O}$ = 3 kV dc, T_A = 25°C		16, 17
	OPT 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50% t = 1 MIN		18
Input-Output Resistance		$R_{I\text{-}O}$		10^{12}		Ω	$V_{I\text{-}O}$ = 500 Vdc		16
Input-Output Capacitance		$C_{I\text{-}O}$		0.6		pF	f = 1 MHz, $V_{I\text{-}O}$ = 0 Vdc		
Input Capacitance		C_{IN}		50		pF	f=1 MHz; V_{IN}=0V, Pins 2 & 3, Pins 1 & 4 Open		

*For JEDEC registered parts.

Notes:

1. Measured at a point 1.6 mm below seating plane.
2. Current into/out of any single lead.
3. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 μs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
4. Derate linearly above 70°C free-air temperature at a rate of 4.1 mW/°C. Maximum input power dissipation of 230 mW allows an input IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA_i} = 240°C/W. Excessive P_{IN} and T_J may result in IC chip degradation.
5. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C.
6. Derate linearly above 70°C free-air temperature at a rate of 3.9 mW/°C. Maximum output power dissipation of 210 mW allows an output IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA_O} = 265°C/W.
7. Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
8. Maximum operating frequency is defined when output waveform (Pin 6) obtains only 90% of V_{CC} with R_L = 4.7 kΩ, C_L = 30 pF using a 5V square wave input signal.

9. All typical values are at $T_A = 25°C$, $V_{CC} = 5.0V$ unless otherwise stated.
10. The t_{PHL} propagation delay is measured from the 2.5V level of the leading edge of a 5.0V input pulse (1 μs rise time) to the 1.5V level on the leading edge of the output pulse (see Figure 9).
11. The t_{PLH} propagation delay is measured from the 2.5V level of the trailing edge of a 5.0V input pulse (1 μs fall time) to the 1.5V level on the trailing edge of the output pulse (see Figure 9).
12. Common mode transient immunity in Logic High level is the maximum tolerable (positive) $dV_{CM/dt}$ on the leading edge of the common mode pulse, V_{CM}, to insure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) $dV_{CM/dt}$ on the trailing edge of the common mode pulse signal, V_{CM}, to insure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$). See Figure 10.
13. In applications where $dV_{CM/dt}$ may exceed 50,000 V/μs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240Ω.
14. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH-}$ once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
15. AC voltage is instantaneous voltage.
16. Device considered a two terminal device: pins 1, 2, 3, 4 connected together, and Pins 5, 6, 7, 8 connected together.
17. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
18. See Option 010 data sheet for more information.

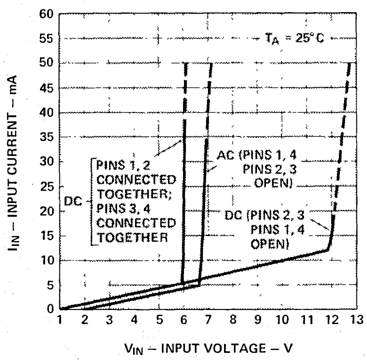


Figure 1. Typical Input Characteristics, I_{IN} vs. V_{IN}. (AC voltage is instantaneous value.)

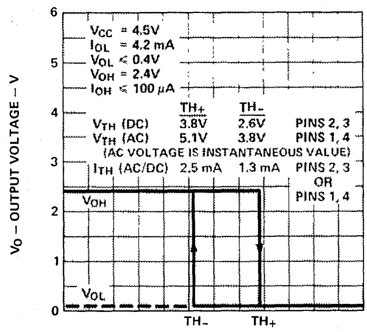


Figure 2. Typical Transfer Characteristics. (AC voltage is instantaneous value.)

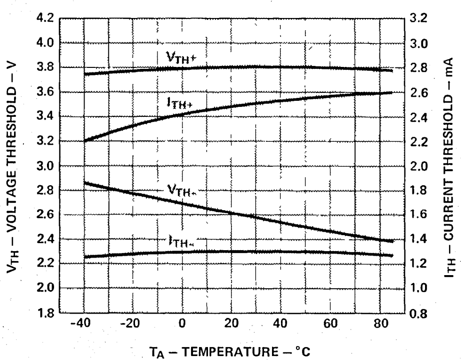


Figure 3. Typical DC Threshold Levels vs. Temperature.

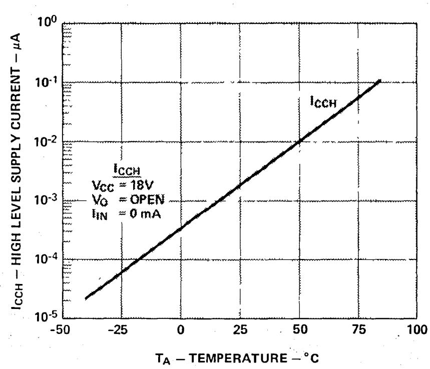


Figure 4. Typical High Level Supply Current, I_{CCH} vs. Temperature.

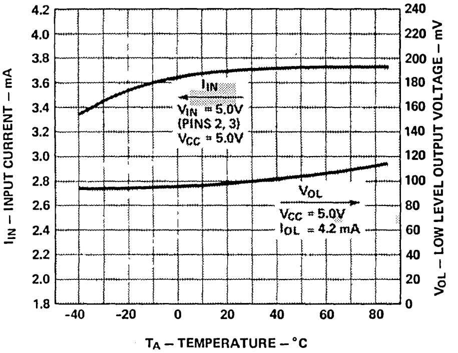


Figure 5. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

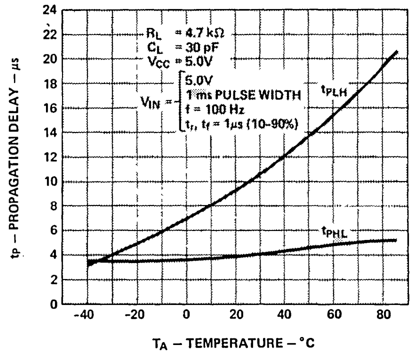


Figure 6. Typical Propagation Delay vs. Temperature.

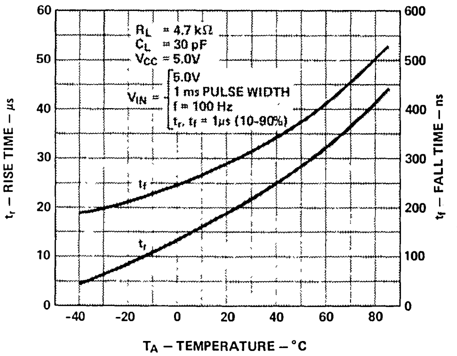


Figure 7. Typical Rise, Fall Times vs. Temperature.

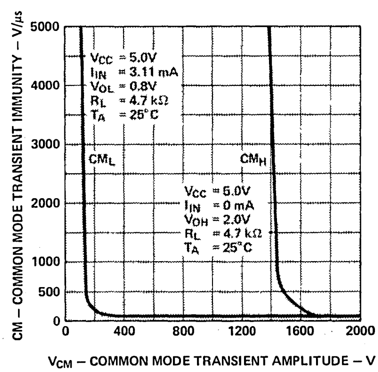


Figure 8. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

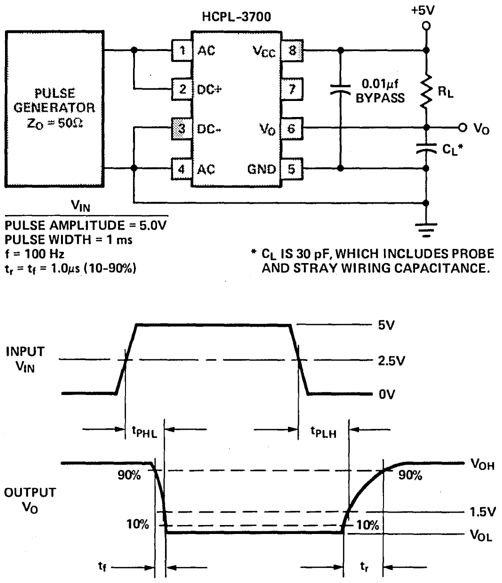


Figure 9. Switching Test Circuit.

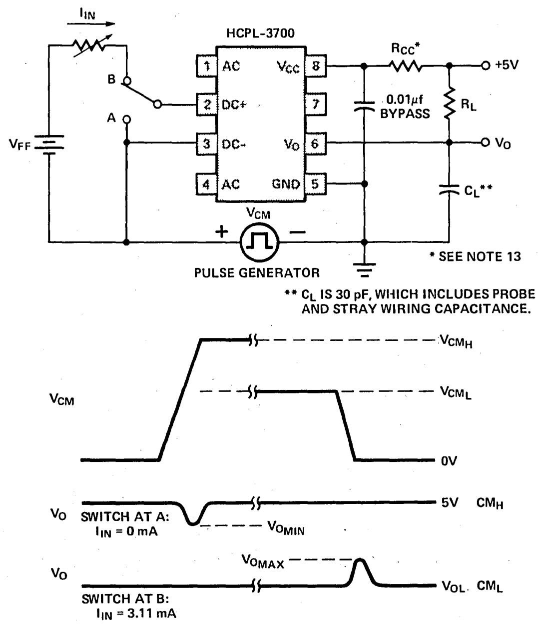


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

Electrical Considerations

The HCPL-3700 optocoupler has internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_X, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_X can be obtained from Figure 11. Specific calculation of R_X can be obtained from Equation (1) of Figure 12. Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_X and R_P as shown in Figure 12 and determined by Equations (2) and (3).

R_X can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts of a relay or switch, the HCPL-3700 in combination with R_X and R_P can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 1). It is recommended that the low clamp condition be used when possible to lower the input power dissipation as well as the LED current, which minimizes LED degradation over time.

In applications where $dV_{CM/dt}$ may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See note 13 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 μf be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing AC signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 μf capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For AC input applications, a filter capacitor can be placed across the DC input terminals for either signal or transient filtering.

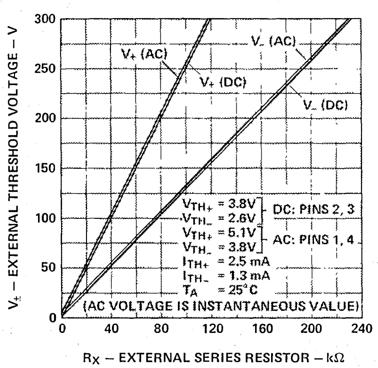


Figure 11. Typical External Threshold Characteristic, $V_{\pm}$ vs. R_X.

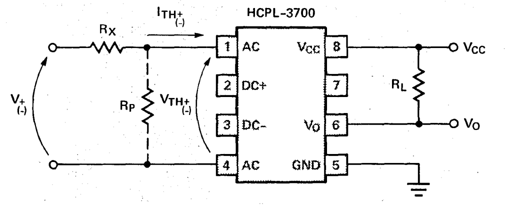


Figure 12. External Threshold Voltage Level Selection.

Either AC (Pins 1, 4) or DC (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_X can be determined without use of R_P via

$$R_X = \frac{V_{+(-)} - V_{TH+(-)}}{I_{TH+(-)}} \tag{1}$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_X and R_P will permit this selection via equations (2), (3) provided the following conditions are met. If the denominator of equation (2) is positive, then

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \quad \text{and} \quad \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

Conversely, if the denominator of equation (2) is negative, then

$$\frac{V_+}{V_-} \leq \frac{V_{TH+}}{V_{TH-}} \quad \text{and} \quad \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}}$$

$$R_X = \frac{V_{TH-}\,(V_+) - V_{TH+}\,(V_-)}{I_{TH+}\,(V_{TH-}) - I_{TH-}\,(V_{TH+})} \tag{2}$$

$$R_P = \frac{V_{TH-}\,(V_+) - V_{TH+}\,(V_-)}{I_{TH+}\,(V_- - V_{TH-}) + I_{TH-}\,(V_{TH+} - V_+)} \tag{3}$$

See Application Note 1004 for more information.

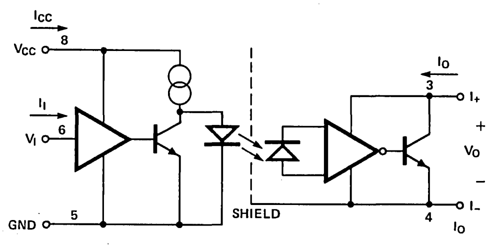
HEWLETT PACKARD

OPTICALLY COUPLED 20 mA CURRENT LOOP TRANSMITTER

HCPL-4100

TECHNICAL DATA JANUARY 1986

SCHEMATIC

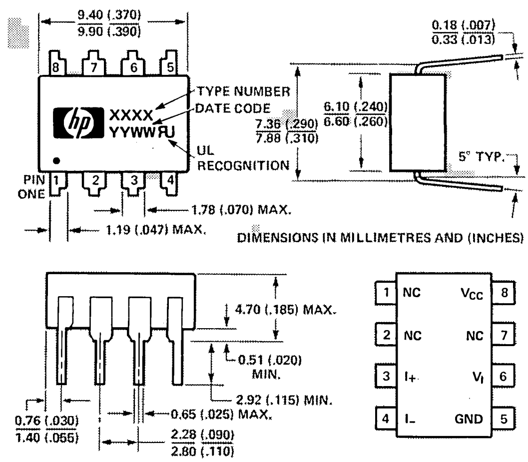


TRUTH TABLE
(POSITIVE LOGIC)*

V_I	V_{CC}	I_O
H	ON	H
L	ON	L
H	OFF	H
L	OFF	H

*CURRENT LOOP CONVENTION – H = MARK: $I_O \geq 12$ mA, L = SPACE: $I_O \leq 2$ mA.

OUTLINE DRAWING*



Features

- GUARANTEED 20 mA LOOP PARAMETERS
- DATA INPUT COMPATIBLE WITH LSTTL, TTL AND CMOS LOGIC
- GUARANTEED PERFORMANCE OVER TEMPERATURE (0° C to 70° C)
- INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION
- 20 KBaud DATA RATE AT 400 METRES LINE LENGTH
- GUARANTEED ON AND OFF OUTPUT CURRENT LEVELS
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).
- OPTICALLY COUPLED 20 mA CURRENT LOOP RECEIVER, HCPL-4200, ALSO AVAILABLE

Applications

- IMPLEMENT AN ISOLATED 20 mA CURRENT LOOP TRANSMITTER IN:
  - Computer Peripherals
  - Industrial Control Equipment
  - Data Communications Equipment

Description

The HCPL-4100 optocoupler is designed to operate as a transmitter in equipment using the 20 mA current loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the logic input to the 20 mA current loop breaks ground loops and provides very high immunity to common mode interference.

The HCPL-4100 data input is compatible with LSTTL, TTL, and CMOS logic gates. The input integrated circuit drives a GaAsP LED. The light emitted by the LED is sensed by a second integrated circuit that allows 20 mA to pass with a voltage drop of less than 2.7 volts when no light is emitted and allows less than 2 mA to pass when light is emitted. The transmitter output is capable of withstanding 27 volts. The input integrated circuit provides a controlled amount of LED drive current and takes into account LED light output degradation. The internal shield allows a guaranteed 1000 V/μs common mode transient immunity.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Voltage Low	V_{IL}	0	0.8	Volts
Input Voltage High	V_{IH}	2.0	20	Volts
Operating Temperature	T_A	0	70	°C
Output Voltage	V_O	0	27	Volts
Output Current	I_O	0	24	mA

Absolute Maximum Ratings

(No Derating Required up to 55° C)

Storage Temperature .... -55° C to 125° C
Operating Temperature .... -40° C to 85° C
Lead Solder Temperature .... 260° C for 10 sec. (1.6 mm below seating plane)
Supply Voltage — V_{CC} .... 0 to 20 V
Average Output Current — I_O .... -30 mA to 30 mA
Peak Output Current — I_O .... internally limited
Output Voltage — V_O .... -0.4 V to 27 V
Input Voltage — V_I .... -0.5 V to 20 V
Input Power Dissipation — P_I .... 265 mW[1]
Output Power Dissipation — P_O .... 125 mW[2]
Total Power Dissipation — P .... 360 mW[3]

Electrical Characteristics

for 0° C ≤ T_A ≤ 70° C, 4.5 V ≤ V_{CC} ≤ 20 V, all typicals at T_A = 25° C and V_{CC} = 5 V unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Mark State Output Voltage	V_{MO}		1.8 2.2 2.35	2.25 2.7	Volts Volts Volts	I_O = 2 mA I_O = 12 mA I_O = 20 mA	V_I = 2.0 V	1, 2	
Mark State Short Circuit Output Current	I_{SC}	30	85		mA	V_I = 2 V, V_O = 5 V to 27 V			4
Space State Output Current	I_{SO}	0.5	1.1	2.0	mA	V_I = 0.8 V, V_O = 27 V		3	
Low Level Input Current	I_{IL}		-0.12	-0.32	mA	V_{CC} = 20 V, V_I = 0.4 V			
Low Level Input Voltage	V_{IL}			0.8	Volts				
High Level Input Voltage	V_{IH}	2.0			Volts				
High Level Input Current	I_{IH}		 0.005	20 100 250	μA μA μA	V_I = 2.7 V V_I = 5.5 V V_I = 20 V			
Supply Current	I_{CC}		7.0 7.8	11.5 13	mA mA	V_{CC} = 5.5 V V_{CC} = 20 V	0 V ≤ V_I ≤ 20 V		
Input-Output Insulation	I_{I-O}*			1	μA	45% RH, t = 5s, V_{I-O} = 3 kV dc, T_A = 25° C			5, 6
OPT 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50% t = 1 MIN			13
Resistance (input-output)	R_{I-O}		10^{12}		Ohms	V_{I-O} = 500 V dc			5
Capacitance (input-output)	C_{I-O}		1		pF	f = 1 MHz, V_{I-O} = 0 V dc			5

*For JEDEC registered parts.

Notes:

1. Derate linearly above 55° C free air temperature at a rate of 3.8 mW/° C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125° C for ambient temperatures up to 85° C.
2. Derate linearly above a free-air temperature of 70° C at a rate of 2.3 mW/° C. A significant amount of power may be dissipated in the HCPL-4100 output circuit during the transition from the SPACE state to the MARK state when driving a data line or capacitive load (C_{OUT}). The average power dissipation during the transition can be estimated from the following equation which assumes a linear discharge of a capacitive load: $P = I_{SC} (V_{SO} + V_{MO})/2$, where V_{SO} is the output voltage in the SPACE state. The duration of this transition can be estimated as $t = C_{OUT} (V_{SO} - V_{MO})/I_{SC}$. For typical applications driving twisted pair data lines with NRZ data as shown in Figure 11, the transition time will be less than 10% of one bit time.
3. Derate linearly above 55° C free-air temperature at a rate of 5.1 mW/° C.
4. The maximum current that will flow into the output in the mark state (I_{SC}) is internally limited to protect the device. The duration of the output short circuit shall not exceed 10 ms.
5. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together, and pins 5, 6, 7, and 8 are connected together.
6. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.

Switching Characteristics

for $0 \leq T_A \leq 70°C$, $4.5\ V \leq V_{CC} \leq 20\ V$, all typicals at $T_A = 25°C$ and $V_{CC} = 5\ V$ unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Testing Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.3	1.6	μs	$C_O = 1000$ pF, $C_L = 15$ pF, $I_O = 20$ mA	4, 5, 6	7
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.2	1.0	μs	$C_O = 1000$ pF, $C_L = 15$ pF, $I_O = 20$ mA	4, 5, 6	8
Propagation Delay Time Skew	t_{PLH}-t_{PHL}		0.1		μs	$I_O = 20$ mA		
Output Rise Time (10-90%)	t_r		16		ns	$I_O = 20$ mA, $C_O = 1000$ pF, $C_L = 15$ pF.	5, 7	9
Output Fall Time (90-10%)	t_f		23		ns	$I_O = 20$ mA, $C_O = 1000$ pF, $C_L = 15$ pF.	5, 7	10
Common Mode Transient Immunity at Logic High Output Level	$\lvert CM_H \rvert$	1,000	10,000		V/μs	$V_I = 2$ V, $T_A = 25°C$ $V_{CM} = 50$ V (peak), $V_{CC} = 5$ V I_O (min.) = 12 mA	8, 9, 10	11
Common Mode Transient Immunity at Logic Low Output Level	$\lvert CM_L \rvert$	1,000	10,000		V/μs	$V_I = 0.8$ V, $T_A = 25°C$ $V_{CM} = 50$ V (peak), $V_{CC} = 5$ V I_O (max.) = 3 mA	8, 9, 10	12

Notes:

7. The t_{PLH} propagation delay is measured from the 1.3 volt level on the leading edge of the input pulse to the 10 mA level on the leading edge of the output pulse.
8. The t_{PHL} propagation delay is measured from the 1.3 volt level on the trailing edge of the input pulse to the 10 mA level on the trailing edge of the output pulse.
9. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output current pulse.
10. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output current pulse.
11. The common mode transient immunity in the logic high level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Mark ("H") state (i.e., $I_O > 12$ mA).
12. The common mode transient immunity in the logic low level is the maximum (negative) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Space ("L") state (i.e., $I_O > 3$ mA).
13. See Option 010 data sheet for more information.

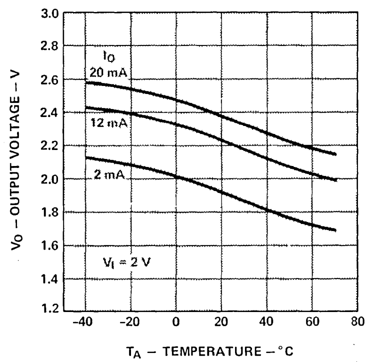


Figure 1. Typical Mark State Output Voltage vs. Temperature

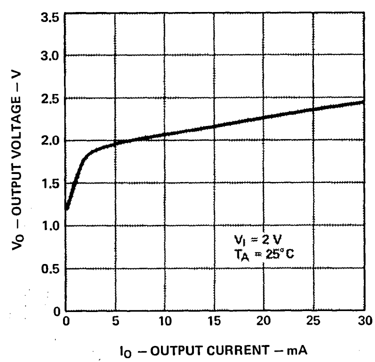


Figure 2. Typical Output Voltage vs. Output Current in Mark State

OPTOCOUPLERS

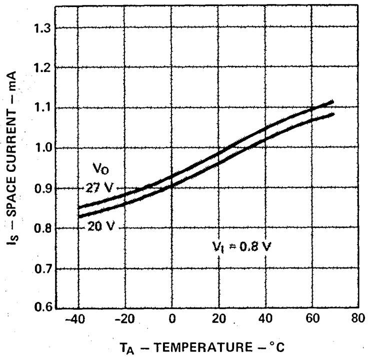


Figure 3. Typical Space State Output Current vs. Temperature

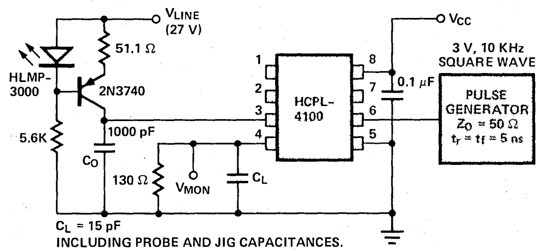


Figure 4. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

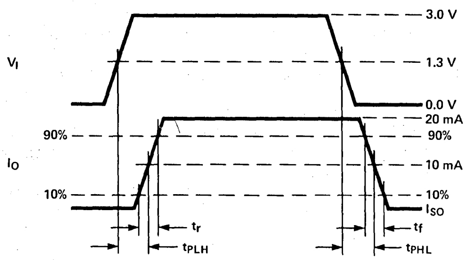


Figure 5. Waveforms for t_{PLH}, t_{PHL}, t_r, and t_f

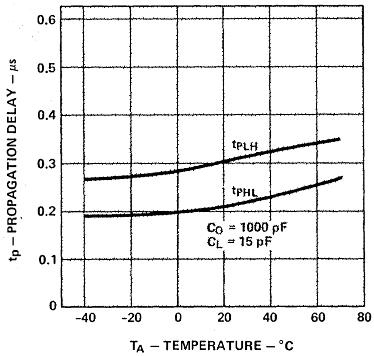


Figure 6. Typical Propagation Delay vs. Temperature

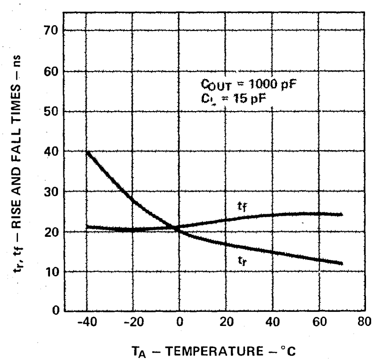


Figure 7. Typical Rise, Fall Times vs. Temperature

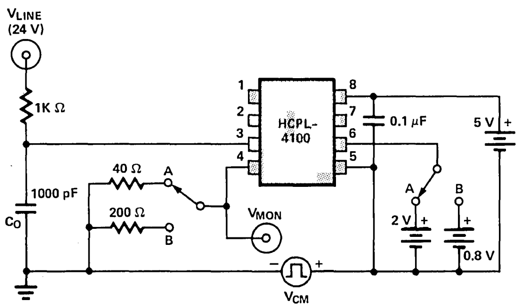


Figure 8. Test Circuit for Common Mode Transient Immunity

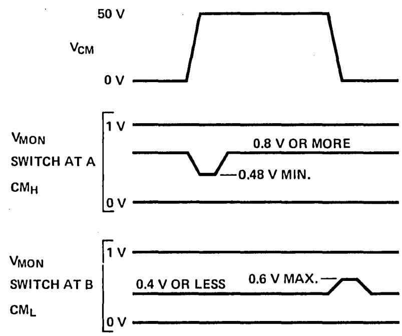


Figure 9. Typical Waveforms for Common Mode Transient Immunity

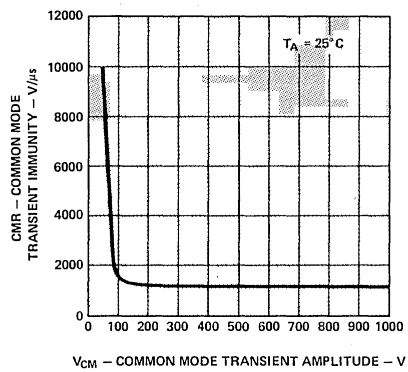


Figure 10. Common Mode Transient Immunity vs. Common Mode Transient Amplitude

Applications

Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point to point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

SIMPLEX

The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter(s) to receiver. This is the simplest configuration for use in long line length (two wire), moderate data rate, and low current source compliance level applications. A block diagram of simplex point to point arrangement is given in Figure 11 for the HCPL-4100 transmitter optocoupler.

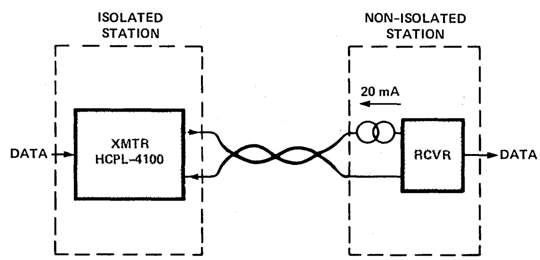


Figure 11. Simplex Point to Point Current Loop System Configuration

Major factors which limit maximum data rate performance for a simplex loop are the location and compliance voltage of the loop current source as well as the total line capacitance. Application of the HCPL-4100 transmitter in a simplex loop necessitates that a non-isolated active receiver (containing current source) be used at the opposite end of the current loop. With long line length, large line capacitance will need to be charged to the compliance voltage level of the current source before the receiver loop current decreases to zero. This effect limits upper data rate performance. Slower data rates will occur with larger compliance voltage levels. The maximum compliance level is determined by the transmitter breakdown characteristic. In addition, adequate compliance of the current source must be available for voltage drops across station(s) during the MARK state in multidrop applications for long line lengths.

In a simplex multidrop application with multiple HCPL-4100 transmitters and one non-isolated active receiver, priority of transmitters must be established.

A recommended non-isolated active receiver circuit which can be used with the HCPL-4100 in point to point or in multidrop 20 mA current loop applications is given in Figure 12. This non-isolated active receiver current threshold must be chosen properly in order to provide adequate noise immunity as well as not to detect SPACE state current (bias current) of the HCPL-4100 transmitter. The receiver input threshold current is Vth/Rth ≈ 10 mA. A simple transistor current source provides a nominal 20 mA loop current over a V_{CC} compliance range of 6 V dc to 27 V dc. A resistor can be used in place of the constant current source for simple applications where the wire loop distance and number of stations on the loop are fixed. A minimum transmitter output load capacitance of 1000 pF is required between pins 3 and 4 to ensure absolute stability.

Length of the current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 12 is graphically illustrated in Figure 13. Multidrop configurations will require larger V_{CC} than Figure 13 predicts in order to account for additional station terminal voltage drops.

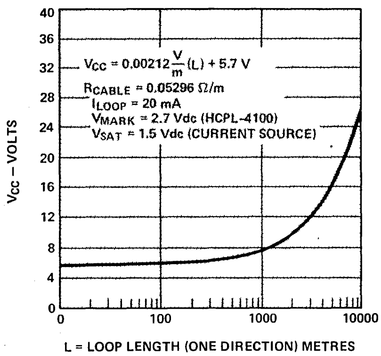


Figure 13. Minimum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 12

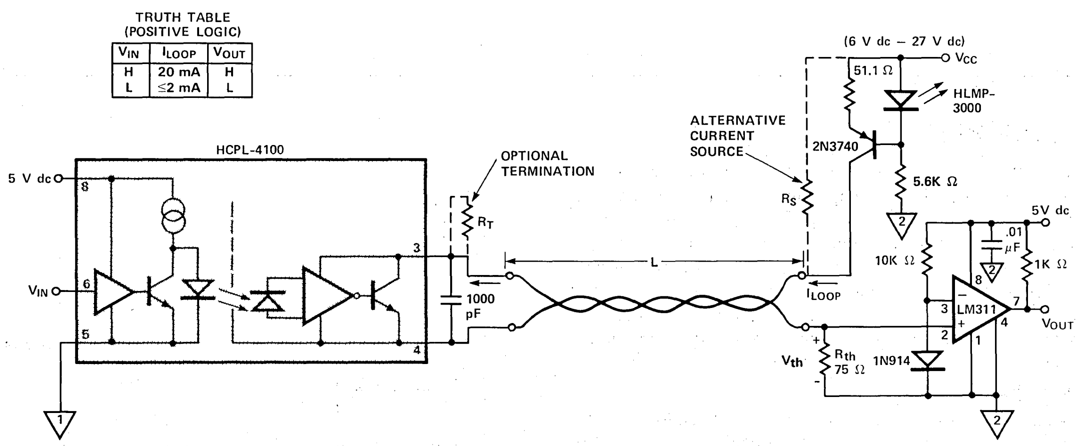


Figure 12. Recommended Non-Isolated Active Receiver with HCPL-4100 Isolated Transmitter for Simplex Point to Point 20 mA Current Loop

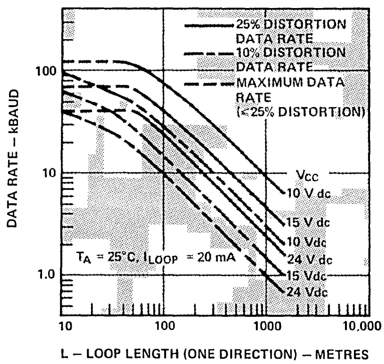


Figure 14. Typical Data Rate vs. Distance and Supply Voltage

Typical data rate performance versus distance is illustrated in Figure 14 for the combination of a non-isolated active receiver and HCPL-4100 optically coupled current loop transmitter shown in Figure 12. Curves are shown for 25% distortion data rate at different V_{CC} values. 25% distortion data rate is defined as that rate at which 25% distortion occurs to output bit interval with respect to the input bit interval. Maximum data rate (dotted line) is restricted by device characteristics. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Enhanced speed performance of the loop system can be obtained with lower V_{CC} supply levels, as illustrated in Figure 14. In addition, when loop current is supplied through a resistor instead of by a current source, an additional series termination resistance equal to the characteristic line impedance can be used at the HCPL-4100 transmitter end to enhance speed of response by approximately 20%.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

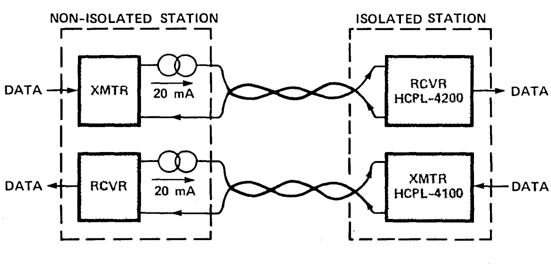


Figure 15. Full Duplex Point to Point Current Loop System Configuration

FULL DUPLEX

Full duplex point to point communication of Figure 15 uses a four wire system to provide simultaneous, bi-directional data communication between local and remote equipment. Basic application uses two simplex point to point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 15 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. Full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

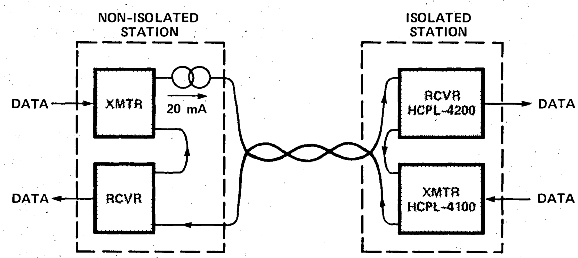
HALF DUPLEX

The half duplex configuration, whether point to point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 16a and 16b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

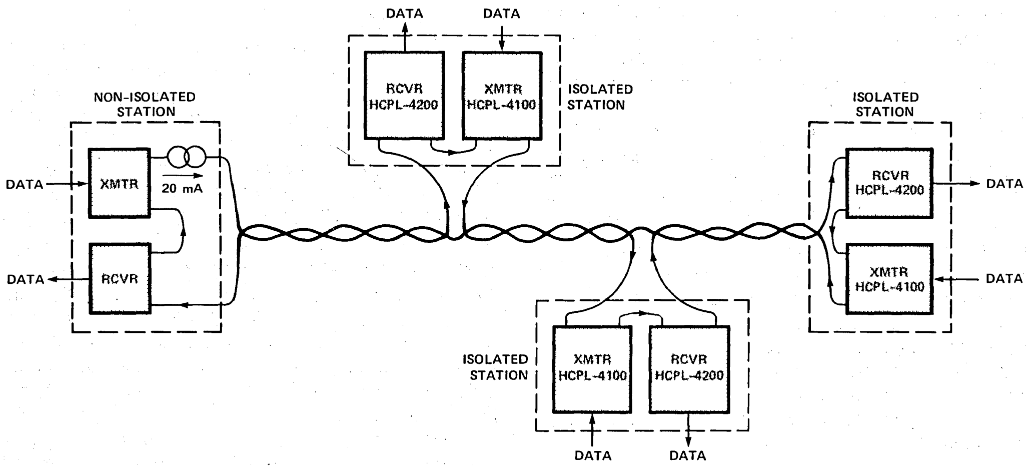
Figures 16a and 16b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow output loop current to conduct when input V_{CC} power is off. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

For more informaton about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.



(a) POINT TO POINT



(b) MULTIDROP

Figure 16. Half Duplex Current Loop System Configurations for (a) Point to Point, (b) Multidrop

HEWLETT PACKARD

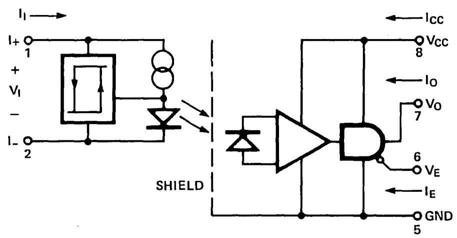
OPTICALLY COUPLED 20 mA CURRENT LOOP RECEIVER

HCPL-4200

TECHNICAL DATA JANUARY 1986

OPTOCOUPLERS

SCHEMATIC

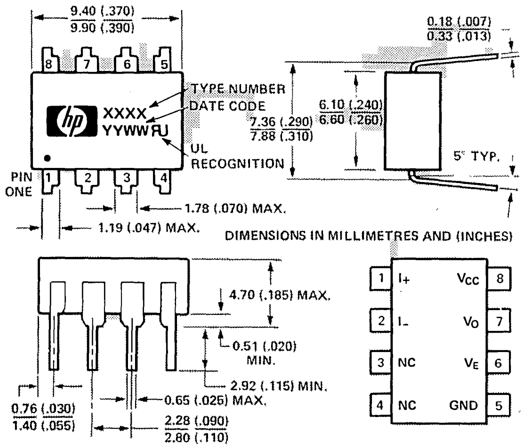


TRUTH TABLE (POSITIVE LOGIC)*

I_I	V_E	V_O
H	H	Z
L	H	Z
H	L	H
L	L	L

*CURRENT LOOP CONVENTION – H = MARK: $I_I \geq 12$ mA, L = SPACE: $I_I \leq 3$ mA, Z = OFF (HIGH IMPEDANCE) STATE.

OUTLINE DRAWING*



Features

- **DATA OUTPUT COMPATIBLE WITH LSTTL, TTL, AND CMOS**
- **20K BAUD DATA RATE AT 1400 METRES LINE LENGTH**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE (0° C TO 70° C)**
- **GUARANTEED ON AND OFF THRESHOLDS**
- **LED IS PROTECTED FROM EXCESS CURRENT**
- **INPUT THRESHOLD HYSTERESIS**
- **THREE-STATE OUTPUT COMPATIBLE WITH DATA BUSES**
- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).**
- **OPTICALLY COUPLED 20 mA CURRENT LOOP TRANSMITTER, HCPL-4100, ALSO AVAILABLE**

Applications

- **IMPLEMENT AN ISOLATED 20 mA CURRENT LOOP RECEIVER IN:**
  Computer Peripherals
  Industrial Control Equipment
  Data Communications Equipment

Description

The HCPL-4200 optocoupler is designed to operate as a receiver in equipment using the 20 mA Current Loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the 20 mA current loop to the logic output breaks ground loops and provides for a very high common mode rejection. The HCPL-4200 aids in the design process by providing guaranteed thresholds for logic high state and logic low state for the current loop, providing an LSTTL, TTL, or CMOS compatible logic interface, and providing guaranteed common mode rejection. The buffer circuit on the current loop side of the HCPL-4200 provides typically 0.8 mA of hysteresis which increases the immunity to common mode and differential mode noise. The buffer also provides a controlled amount of LED drive current which takes into account LED light output degradation. The internal shield allows a guaranteed 1000 V/μs common mode transient immunity.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Forward Input Current (SPACE)	I_{SI}	0	2.0	mA
Forward Input Current (MARK)	I_{MI}	14	24	mA
Operating Temperature	T_A	0	70	°C
Fan Out	N	0	4	TTL Loads
Logic Low Enable Voltage	V_{EL}	0	0.8	Volts
Logic High Enable Voltage	V_{EH}	2.0	20	Volts

Absolute Maximum Ratings

(No Derating Required up to 70° C)

Storage Temperature .... —55° C to 125° C
Operating Temperature .... —40° C to 85° C
Lead Solder Temperature .... 260° C for 10 sec.
(1.6 mm below the seating plane)
Supply Voltage — V_{CC} .... 0 V to 20 V
Average Input Current — I_I .... —30 mA to 30 mA
Peak Transient Input Current — I_I .... 0.5 A[1]
Enable Input Voltage — V_E .... —0.5 V to 20 V
Output Voltage — V_O .... —0.5 V to 20 V
Average Output Current — I_O .... 25 mA
Input Power Dissipation — P_I .... 90 mW[2]
Output Power Dissipation — P_O .... 210 mW[3]
Total Power Dissipation — P .... 255 mW[4]

Electrical Characteristics

For 0° C ≤ T_A ≤ 70° C, 4.5 V ≤ V_{CC} ≤ 20 V, V_E = 0.8 V, all typicals at T_A = 25° C and V_{CC} = 5 V unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Mark State Input Current	I_{MI}	12			mA			1, 2, 3	
Mark State Input Voltage	V_{MI}		2.52	2.75	Volts	I_I = 20 mA	V_E = Don't Care	3, 4	
Space State Input Current	I_{SI}			3	mA			1, 2, 3	
Space State Input Voltage	V_{SI}		1.6	2.2	Volts	I_I = 0.5 to 2.0mA	V_E = Don't Care	1, 3	
Input Hysteresis Current	I_{HYS}	0.3	0.8		mA			1	
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)	I_I = 3 mA	5	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -2.6 mA,	I_I = 12 mA	6	
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	µA	V_O = 5.5 V	I_I = 20 mA		
				500	µA	V_O = 20 V	V_{CC} = 4.5 V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	µA	V_E = 2.7 V			
				100	µA	V_E = 5.5 V			
			.004	250	µA	V_E = 20 V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_E = 0.4 V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5 V	I_I = 0 mA		
			5.25	7.5	mA	V_{CC} = 20 V	V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5 V	I_I = 20 mA		
			3.1	6.0	mA	V_{CC} = 20 V	V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			-20	µA	V_O = 0.4 V	V_E = 2.0 V, I_I = 20 mA		
	I_{OZH}			20	µA	V_O = 2.4 V	V_E = 2 V, I_I = 0 mA		
				100	µA	V_O = 5.5 V			
				500	µA	V_O = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5 V	I_I = 0 mA		5
		40			mA	V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_I = 20 mA		5
		-25			mA	V_{CC} = 20 V	V_O = GND		
Input-Output Insulation	$I_{I\text{-}O}$*			1	µA	45% RH, t = 5s, $V_{I\text{-}O}$ = 3kV dc, T_A = 25°C			6, 7
OPT. 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min.			14
Input-Output Resistance	$R_{I\text{-}O}$		10^{12}		ohms	$V_{I\text{-}O}$ = 500 V dc			6
Input-Output Capacitance	$C_{I\text{-}O}$		1.0		pF	f = 1 MHz, $V_{I\text{-}O}$ = 0 V dc			6
Input Capacitance	C_{IN}		120		pF	f = 1 MHz, V_I = 0 V dc, Pins 1 and 2			

*For JEDEC registered parts.

Switching Characteristics

For $0°C \leq T_A \leq 70°C$, $4.5\ V \leq V_{CC} \leq 20\ V$, $V_E = 0.8\ V$, all typicals at $T_A = 25°C$ and $V_{CC} = 5\ V$ unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.23	1.6	μs	$V_E = 0$ V, $C_L = 15$ pF	7, 8, 9	8
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.17	1.0	μs	$V_E = 0$ V, $C_L = 15$ pF	7, 8, 9	9
Propagation Delay Time Skew	t_{PLH}-t_{PHL}		60		ns	$I_I = 20$ mA, $C_L = 15$ pF	7, 8, 9	
Output Enable Time to Logic Low Level	t_{PZL}		25		ns	$I_I = 0$ mA, $C_L = 15$ pF	11, 12, 14	
Output Enable Time to Logic High Level	t_{PZH}		28		ns	$I_I = 20$ mA, $C_L = 15$ pF	11, 12, 13	
Output Disable Time from Logic Low Level	t_{PLZ}		60		ns	$I_I = 0$ mA, $C_L = 15$ pF	11, 12, 14	
Output Disable Time from Logic High Level	t_{PHZ}		105		ns	$I_I = 20$ mA, $C_L = 15$ pF	11, 12, 13	
Output Rise Time (10-90%)	t_r		55		ns	$V_{CC} = 5$ V, $C_L = 15$ pF	7, 8, 10	10
Output Fall Time (90-10%)	t_f		15		ns	$V_{CC} = 5$ V, $C_L = 15$ pF	7, 8, 10	11
Common Mode Transient Immunity at Logic High Output Level	$\|CM_H\|$	1,000	10,000		V/μs	$V_{CM} = 50$ V (peak) $I_I = 12$ mA, $T_A = 25°C$	15, 16	12
Common Mode Transient Immunity at Logic Low Output Level	$\|CM_L\|$	1,000	10,000		V/μs	$V_{CM} = 50$ V (peak) $I_I = 3$ mA, $T_A = 25°C$	15, 16	13

NOTES:
1. ≤ 1 μs pulse width, 300 pps.
2. Derate linearly above 70° C free air temperature at a rate of 1.6 mW/° C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125° C for ambient temperatures up to 85° C.
3. Derate linearly above 70° C free air temperature at a rate of 3.8 mW/° C.
4. Derate linearly above 70° C free air temperature at a rate of 4.6 mW/° C.
5. Duration of output short circuit time shall not exceed 10 ms.
6. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together and pins 5, 6, 7, and 8 are connected together.
7. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
8. The t_{PLH} propagation delay is measured from the 10 mA level on the leading edge of the input pulse to the 1.3 V level on the leading edge of the output pulse.
9. The t_{PHL} propagation delay is measured from the 10 mA level on the trailing edge of the input pulse to the 1.3 V level on the trailing edge of the output pulse.
10. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output logic pulse.
11. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output logic pulse.
12. Common mode transient immunity in the logic high level is the maximum (negative) dV_{CM}/dt on the trailing edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic high state (i.e., $V_O \geq 2$ V).
13. Common mode transient immunity in the logic low level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic low state (i.e., $V_O \leq 0.8$ V).
14. See Option 010 data sheet for more information.

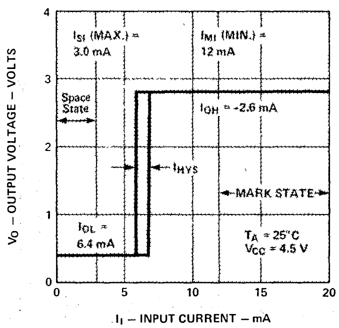


Figure 1. Typical Output Voltage vs. Loop Current

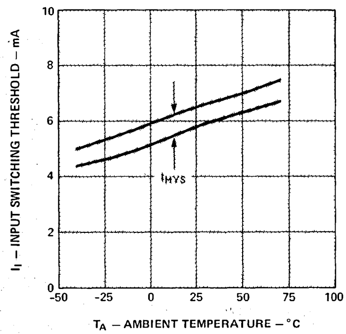


Figure 2. Typical Current Switching Threshold vs. Temperature

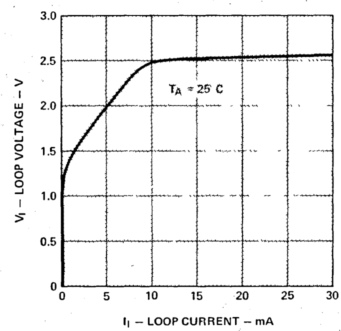


Figure 3. Typical Input Loop Voltage vs. Input Current

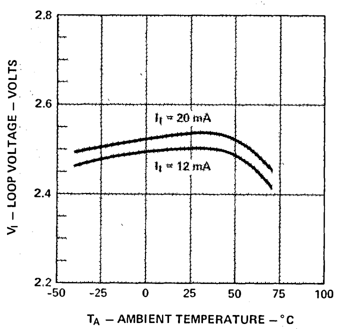


Figure 4. Typical Input Voltage vs. Temperature

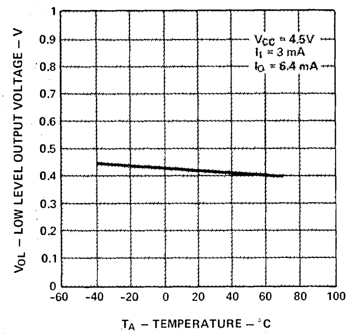


Figure 5. Typical Logic Low Output Voltage vs. Temperature

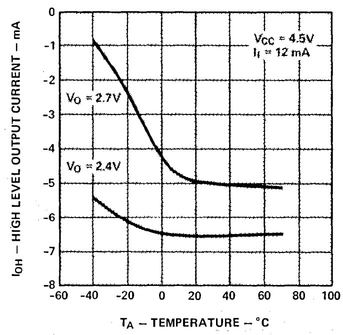
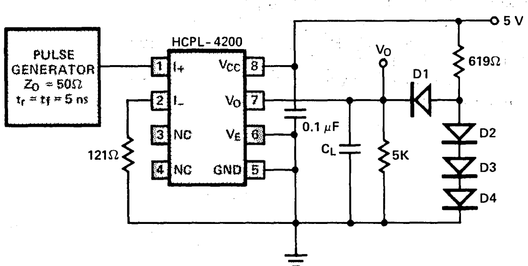


Figure 6. Typical Logic High Output Current vs. Temperature



V_{IN} = 5 VOLT, 100 KHz 10% DUTY CYCLE
D1 - D4 ARE 1N916 OR 1N3064

C_L = 15 pF INCLUDING PROBE AND JIG CAPACITANCE

Figure 7. Test Circuit for t_{PHL}, t_{PLH}, t_r, and t_f

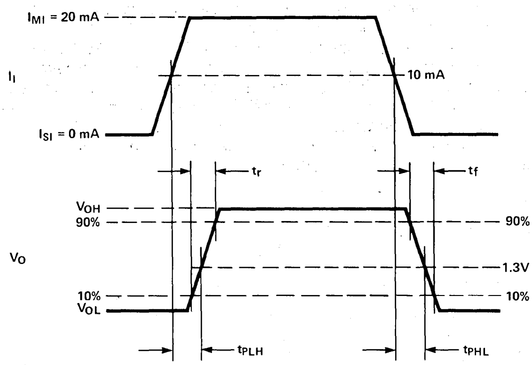


Figure 8. Waveforms for t_{PHL}, t_{PLH}, t_r, and t_f

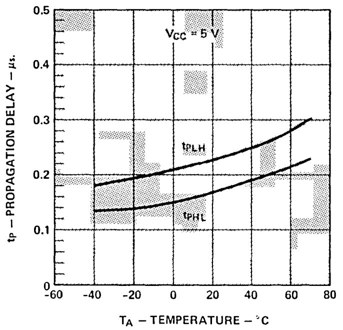


Figure 9. Typical Propagation Delay vs. Temperature

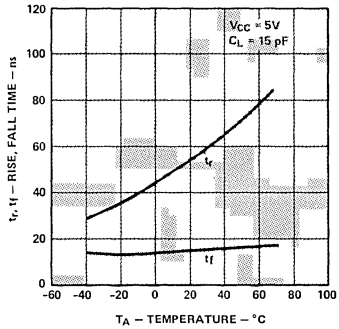


Figure 10. Typical Rise, Fall Time vs. Temperature

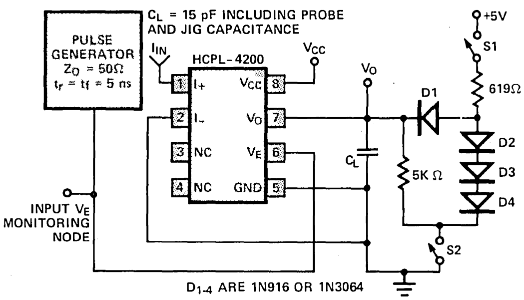


Figure 11. Test Circuit for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}

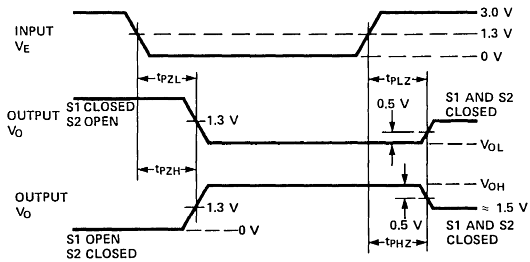


Figure 12. Waveforms for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}

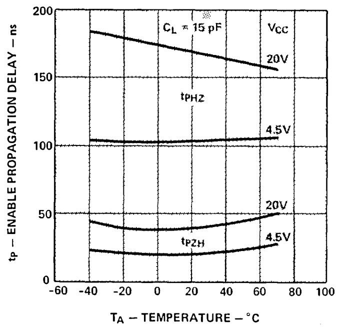


Figure 13. Typical Logic High Enable Propagation Delay vs. Temperature

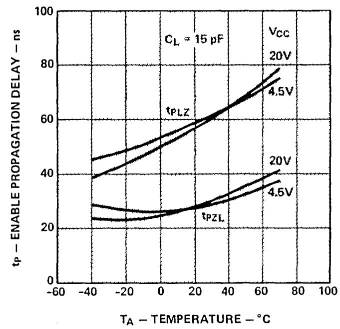


Figure 14. Typical Logic Low Enable Propagation Delay vs. Temperature

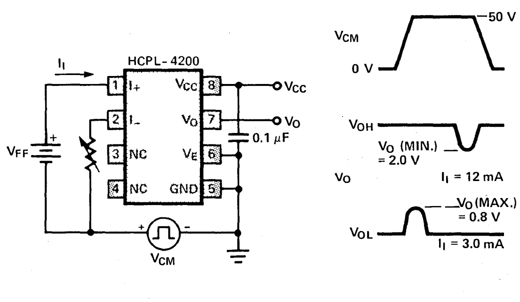


Figure 15. Test Circuit for Common Mode Transient Immunity

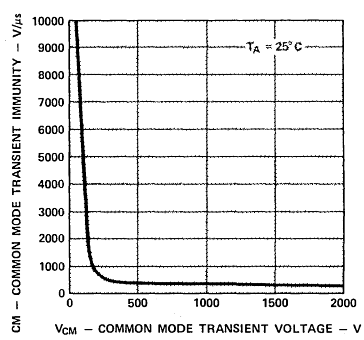


Figure 16. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude

Applications

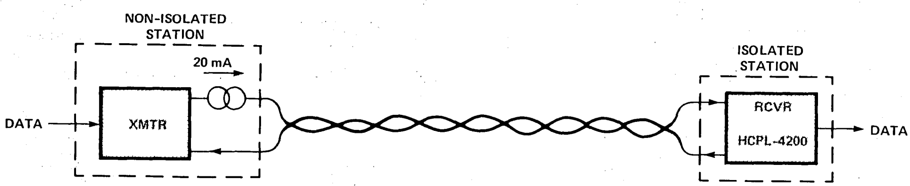
Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point-to-point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

SIMPLEX

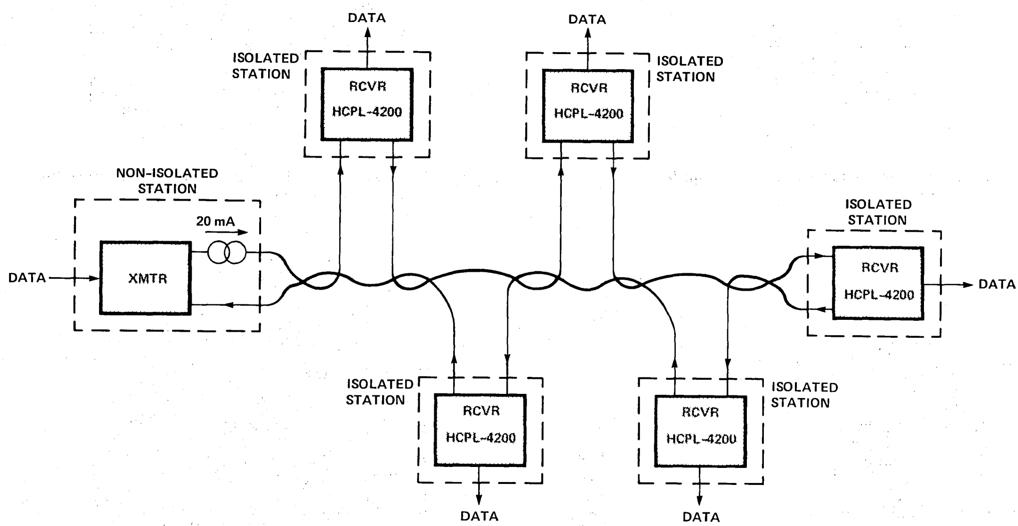
The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter to receiver(s). This is the simplest configuration for use in long line length (two wire), for high data rate, and low current source compliance level applications. Block diagrams of simplex point-to-point and multidrop arrangements are given in Figures 17a and 17b respectively for the HCPL-4200 receiver optocoupler.

For the highest data rate performance in a current loop, the configuration of a non-isolated active transmitter (containing current source) transmitting data to a remote isolated receiver(s) should be used. When the current source is located at the transmitter end, the loop is charged approximately to V_{MI} (2.5 V). Alternatively, when the current source is located at the receiver end, the loop is charged to the full compliance voltage level. The lower the charged voltage level the faster the data rate will be. In the configurations of Figures 17a and 17b, data rate is independent of the current source voltage compliance level. An adequate compliance level of current source must be available for voltage drops across station(s) during the MARK state in multidrop applications or for long line length. The maximum compliance level is determined by the transmitter breakdown characteristic.

A recommended non-isolated active transmitter circuit which can be used with the HCPL-4200 in point-to-point or in multidrop 20 mA current loop applications is given in Figure 18. The current source is controlled via a standard TTL 7407 buffer to provide high output impedance of current source in both the ON and OFF states. This non-isolated active transmitter provides a nominal 20 mA loop current for the listed values of V_{CC}, R2 and R3 in Figure 18.

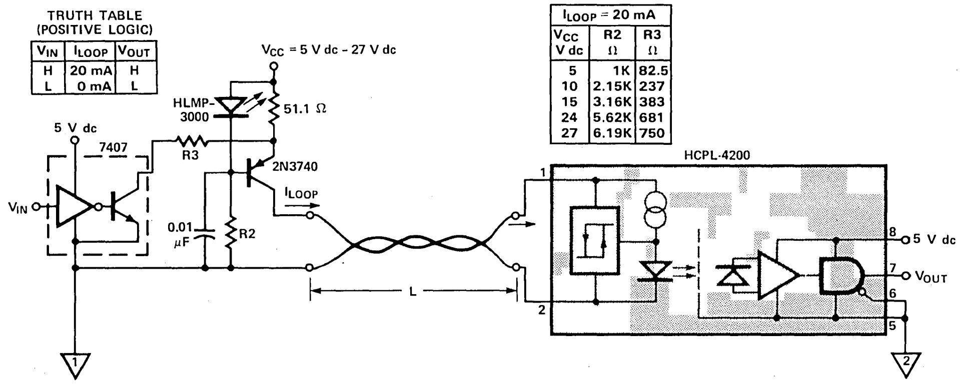


(a) POINT-TO-POINT



(b) MULTIDROP

Figure 17. Simplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop



V_{IN}	I_{LOOP}	V_{OUT}
H	20 mA	H
L	0 mA	L

I_{LOOP} = 20 mA		
V_{CC} V dc	R2 Ω	R3 Ω
5	1K	82.5
10	2.15K	237
15	3.16K	383
24	5.62K	681
27	6.19K	750

Figure 18. Recommended Non-Isolated Active Transmitter with HCPL-4200 Isolated Receiver for Simplex Point-to-Point 20 mA Current Loop

Length of current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 18 is graphically illustrated in Figure 19. Multidrop configurations will require larger V_{CC} than Figure 19 predicts in order to account for additional station terminal voltage drops.

Typical data rate performance versus distance is illustrated in Figure 20 for the combination of a non-isolated active transmitter and HCPL-4200 optically coupled current loop receiver shown in Figure 18. Curves are shown for 10% and 25% distortion data rate. 10% (25%) distortion data rate is defined as that rate at which 10% (25%) distortion occurs to output bit interval with respect to input bit interval. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Data rate is independent of current source supply voltage, V_{CC}.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

FULL DUPLEX

The full duplex point-to-point communication of Figure 21 uses a four wire system to provide simultaneous, bidirectional data communication between local and remote equipment. The basic application uses two simplex point-to-point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 21 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. The full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

HALF DUPLEX

The half duplex configuration, whether point-to-point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 22a and 22b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

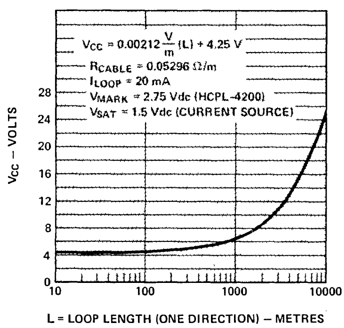


Figure 19. Minimum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 18

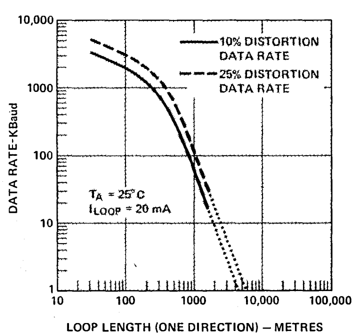


Figure 20. Typical Data Rate vs. Distance

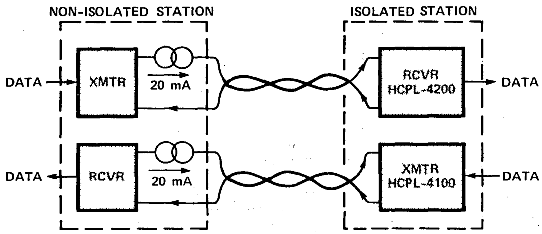
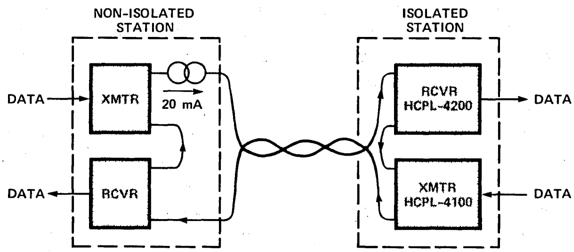


Figure 21. Full Duplex Point-to-Point Current Loop System Configuration

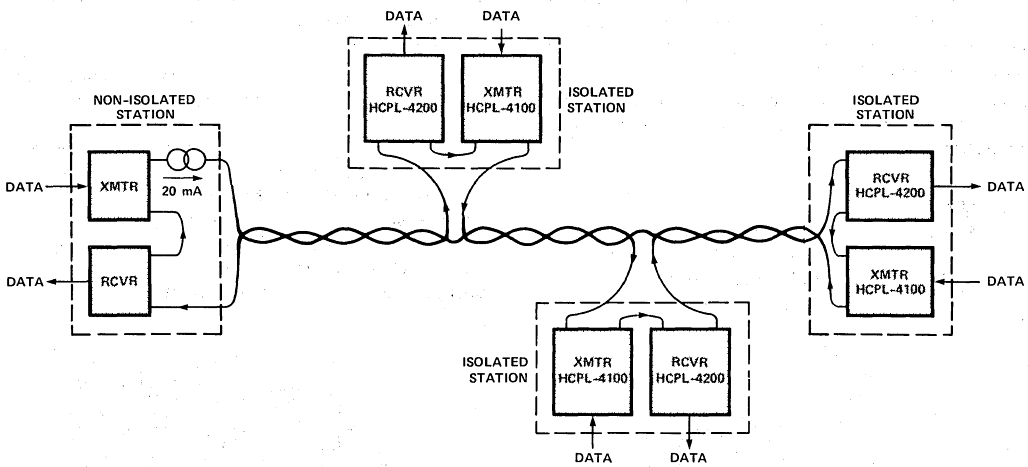
Figures 22a and 22b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow loop current to conduct when input V_{CC} power is off. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

For more information about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.



(a) POINT-TO-POINT

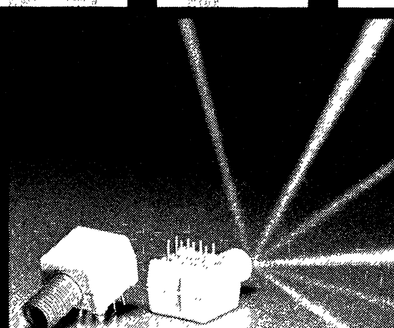


(b) MULTIDROP

Figure 22. Half Duplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop

[redacted]

4. Fiber Optics



Fiber Optics

Three major families of fiber optic components offer a wide range of application solutions. The design and specification of each of these three families allow easy design-in and provide guaranteed end-to-end performance.

Hewlett-Packard's method of specification assures guaranteed link performance and easy design-in. The transmitter optical output power and receiver sensitivity are specified at the end of a length of test cable. These specifications take into account variations over temperature and connector tolerances. All families of components incorporate the fiber optic connector receptacle in the transmitter and receiver packages. Factory alignment of the emitter inside the connector receptacle minimizes the variation of optical output power, resulting in smaller dynamic range requirements for the receiver. The guaranteed distance and data rates for various transmitter/receiver pairs are shown in the following selection guide.

Hewlett-Packard offers a choice of fiber optic cable, either glass fiber or plastic, simplex or duplex, factory-connectored or bulk. Connector attachment in each case has been designed for your production-line economy.

Plastic Snap-In Link Components

Low-cost and ease of use make this family of link components well-suited for applications connecting computers to terminals, printers, plotters and industrial-control equipment. These links are rugged, 1 millimetre diameter plastic fiber cable. Assembling the plastic snap-in connectors onto the cable is extremely easy. The HFBR-0500 evaluation kit contains a complete working link including transmitter, receiver, 5 metres of connectored cable, extra connectors, polishing kit and technical literature.

Miniature Link Components

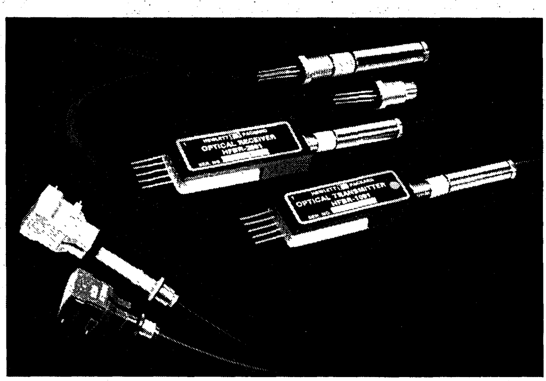
This family offers a wide range of price/performance choices for computer, industrial-control and military applications. The unique design of the lensed optical coupling system makes this family of components very reliable. The low cost miniature line (HFBR-0400 series) features a Dual-in-line package which requires no mounting hardware or receptacle for use with SMA-style connectors. It is also specified for use with five fiber sizes: 100/140 μm, 85/125 μm, 62.5/125 μm, 50/125 μm, and 200 μm Plastic Coated Silica (PCS) cable. The standard miniature line (HFBR-0200 series) features a precision metal package for rugged applications. Both HP-style and SMA-style connectors are available for this line. An evaluation kit is available for sampling purposes. The HFBR-0200 kit contains transmitter, receiver, 10 metres of cable and technical literature.

High Performance Modules

Transparent TTL-TTL link capability and independence from data format restrictions make this family of modules easy to use in a variety of applications. A link monitor on the receiver provides a digital indication of link continuity, independent of the presence of data. The modules are compatible with HP-style connectors and small-diameter glass fiber cable. A transmitter, receiver, 10 metres of connectored cable and technical literature are contained in the HFBR-0010 evaluation kit.

RS-232/V.24 to Fiber Optic Multiplexer

The 39301A 16-channel RS-232C/V.24 to fiber optic multiplexer allows the extension of up to 16 independent 19.2 Kbps full duplex channels to distance up to 1250m.



Fiber Optic Selection Guide

Snap-In Link Family: Features — Plastic fiber (1 mm dia.), Plastic Snap-in connectors, TTL compatible output.

Products/Part Nos.		Description		Page No.
Evaluation Kit				4-6
HFBR-0500		HFBR-1510 Transmitter, HFBR-2501 Receiver, 5 metre connectored cable, connectors, bulkhead feedthrough polishing kit; literature		
Transmitter/Receiver Pairs		Guaranteed Distance*	Guaranteed Data-Rate*	
5 MBd Link	HFBR-1510/-2501	17 metre	5 MBd	4-8
1 MBd Link	HFBR-1502/-2502	36 metre	1 MBd	4-10
Extended Distance Link	HFBR-1512/-2503	65 metre	40 kBd	4-12
Low Current Link	HFBR-1512/-2503	14 metre	40 kBd	4-12
Photo Interrupter Link	HFBR-1512/-2503	N/A	20 kHz	4-14
	HFBR-1502/-2502	N/A	500 kHz	4-14
Cables				
Simplex	Duplex	Cable Length		4-20
HFBR-3511	—	0.1 metre		
HFBR-3512	HFBR-3612	0.5 metre		
HFBR-3513	HFBR-3613	1.0 metre		
HFBR-3514	HFBR-3614	5.0 metre	connectored	
HFBR-3515	HFBR-3615	10.0 metre		
HFBR-3516	HFBR-3616	20.0 metre		
HFBR-3517	HFBR-3617	30.0 metre		
HFBR-3518	HFBR-3618	45.0 metre		
HFBR-3519	HFBR-3619	60.0 metre		
HFBR-3579	HFBR-3679	25.0 metre		
HFBR-3580	HFBR-3680	100.0 metre	unconnectored	
HFBR-3581	HFBR-3681	500.0 metre		
Connectors				
HFBR-4501		Gray Connector/Crimp Ring		4-22
HFBR-4511		Blue Connector/Crimp Ring		
Polishing Kit				
HFBR-4595		Plastic polishing fixture, abrasive paper		4-22
HFBR-4596		Metal polishing fixture		
Bulkhead Feedthrough/in-line Splice				
HFBR-4505		Gray Bulkhead Feedthrough		4-22
HFBR-4515		Blue Bulkhead Feedthrough		

Low Cost Miniature Link Family: Features — Dual-in-line package interfaces directly with SMA-style connectors specified for use with 50/125 μm, 62.5/125 μm 85/125 μm, 100/140 μm, and 200 μm Plastic Coated Silica (PCS) cable. No mounting hardware required.

Products/Part Nos.	Description		Page No.
Transmitter/Receiver Pairs	Guaranteed Optical Power Budget*	Guaranteed Data-Rate*	
HFBR-1402/2402	14 dB (200 μm PCS)	5 MBd	4-31
	9 dB (HFBR-3000 100/140 μm cable)	5 MBd	4-31
	6 dB (85/125 μm cable)	5 MBd	4-31
HFBR-1404/2402	9 dB (62.5/125 μm cable)	5 MBd	4-31
	4 dB (50/125 μm cable)	5 MBd	4-31
HFBR-1402/2404 (HFBR-0422 Tranceiver Board)	12 dB (HFBR-3000 100/140 μm cable)	50 MBd	4-41
HFBR-1402 Standard Transmitter	Optimized for large size fiber such as 85/125 μm, 100/140 μm, or 200 μm PCS cable		4-27
HFBR-1404 High-Performance Transmitter	Optimized for small size fiber such as 50/125 μm or 62.5/125 μm cable		4-27
HFBR-2402 5 MB Receiver	TTL/CMOS Compatible receiver with –25.4 dBm sensitivity		4-31
HFBR-2404 25 MHz Receiver	PIN-preamp receiver for data rates up to 50 MBd		4-33

Miniature Link Family: Features — Glass fiber (100/400 μm). Precision metal connectors.

Products/Part Nos.		Description		Page No.
Evaluation Kit HFBR-0200		HFBR-1201 Transmitter, HFBR-2201 Receiver, 10 metre connectored cable Mounting Hardware		4-46
Transmitter/Receiver Pairs				4-46
HP Style Connectors	SMA Style Connectors	Guaranteed Distance*	Guaranteed Data Rate*	4-54
HFBR-1201/-2201	HFBR-1202/-2202	800 metre	5 MBd	4-58
HFBR-1201/-2203	HFBR-1202/-2204	1200 metre	40 MBd	4-74
HFBR-1203/-2201	HFBR-1204/-2202	1800 metre	5 MBd	
HFBR-1203/-2203	HFBR-1204/-2204	2100 metre	40 MBd	
HFBR-1203/-2207	HFBR-1204/-2208	500 mètre (typical)	125 MBd (typical)	
Transceivers, 20 MBd (to 40 MBd)				
HP Style Connectors	SMA Style Connectors	Guaranteed Distance	Data Format	4-66
HFBR-0221	HFBR-0222	1100 metre	33 to 67% duty factor (for use with code schemes such as Manchester)	
HFBR-0223	HFBR-0224	625 metre	STD 95% duty factor (for use with code schemes such as NRZ)	
Cables				
Simplex	Duplex			
HFBR-3000 (OPT001)	HFBR-3100 (OPT001)	Customer specified length, connectored (HFBR-4000 connector)		4-92
HFBR-3000 (OPT002)	HFBR-3100 (OPT002)	Customer specified length, connectored (SMA style connector)		
HFBR-3200	HFBR-3300	Customer specified length, unconnectored		4-94
HFBR-3001		10 metres connectored (HFBR-4000 connector)		
HFBR-3021		10 metres connectored (SMA style connector)		
Connectors				
HFBR-4000		Metal body, metal ferrule		4-96
HFBR-3099		Connector-connector junction, bulkhead feedthrough for HFBR-4000 connector		
Connector Assembly Tools				
HFBR-0100		Field installation kit for HFBR-4000 connectors (includes case, tools, consumables)		4-98
HFBR-0101		Replacement consumables for HFBR-0100 Kit		
HFBR-0102		Custom tool set only		
Mounting Hardware				
HFBR-4201		PCB mounting bracket, EMI shield, misc. hardware for HFBR-1201/-1203/-2201/-2203		4-46
HFBR-4202		PCB mounting bracket, EMI shield, misc. hardware for HFBR-1202/-1204/-2202/-2204		

*Link performance at 25° C.

High Performance Module Family: Glass fiber (100/140 μm), Precision metal connectors, TTL compatible output, Link monitor, Transparent 3-level code

Products/Part Nos.		Description			Page No.
Evaluation Kit					
HFBR-0010		HFBR-1001 Transmitter, HFBR-2001 Receiver, 10 metre connectored cable, literature			
Transmitter/Receiver Pairs		Guaranteed Distance*	Guaranteed Data Rate*	Connector Style	
HFBR-1001/-2001		180 metre	10 MBd	HFBR-4000	4-80
HFBR-1002/-2001		1500 metre	10 MBd	HFBR-4000	4-84
Cables					
Simplex	Duplex				
HFBR-3000 (OPT001)	HFBR-3100 (OPT001)	Customer specified length, connectored (HFBR-4000 connector)			4-92
HFBR-3200	HFBR-3300	Customer specified length, unconnectored			4-94
HFBR-3001		10 metres connectored (HFBR-4000 connector)			
HFBR-3021		10 metres connectored (SMA style connector)			
Connectors					
HFBR-4000		Metal body, metal ferrule			4-96
HFBR-3099		Connector-connector junction, bulkhead feedthrough for HFBR-4000 connector			
Connector Assembly Tools					
HFBR-0100		Field installation kit for HFBR-4000 connectors (includes case, tools, consumables)			4-98
HFBR-0101		Replacement consumables for HFBR-0100 Kit			
HFBR-0102		Custom tool set only			

Data Communications Equipment

Products/Part Nos.	Description	Page No.
RS-232-C/V.24 to Fiber Optic Multiplexer		
39301A Multiplexer	1250 metres length, 19.2 kbps/channel data rate, 16 channels RS-232-C Input/Output	4-100

PIN Photodiodes: Variety of packages, high speed, low capacitance, low noise.

Products/Part Nos.	Description	Page No.
5082-4200 Series	High Speed PIN Photodiodes for use in Fiber Optic Applications	4-106

*Link performance at 25° C.

FIBER OPTICS

HEWLETT PACKARD

SNAP-IN FIBER OPTIC LINKS TRANSMITTERS, RECEIVERS, CABLE AND CONNECTORS

HFBR-0500 SERIES

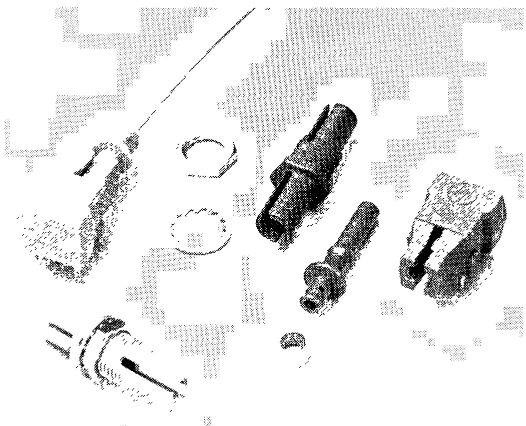
TECHNICAL DATA JANUARY 1986

Features

- GUARANTEED LINK PERFORMANCE OVER TEMPERATURE
  High Speed Links: dc to 5 MBd
  Extended Distance Links up to 82 m
  Low Current Links: 6 mA Peak Supply Current for an 8 m Link
  Photo Interrupters
- LOW COST PLASTIC DUAL-IN-LINE PACKAGE
- EASY FIELD CONNECTORING
- EASY TO USE RECEIVERS:
  Logic Compatible Output Level
  Single +5 V Receiver Power Supply
  High Noise Immunity
- LOW LOSS PLASTIC CABLE:
  Selected Super Low Loss Simplex Cable
  Simplex and Zip Cord Style Duplex Cable

Applications

- HIGH VOLTAGE ISOLATION
- SECURE DATA COMMUNICATIONS
- REMOTE PHOTO INTERRUPTER
- LOW CURRENT LINKS
- INTER/INTRA-SYSTEM LINKS
- STATIC PROTECTION
- EMC REGULATED SYSTEMS (FCC, VDE)



Description

The HFBR-0500 series is a complete family of fiber optic link components for configuring low-cost control, data transmission, and photo interrupter links. These components are designed to mate with plastic snap-in connectors and low-cost plastic cable.* Link design is simplified by the logic compatible receivers and the ease of connectoring the plastic fiber cable. The key parameters of links configured with the HFBR-0500 family are fully guaranteed. The HFBR-0500 Evaluation Kit contains all the components and literature necessary to evaluate a working link.

* Cable is available in standard low loss and selected super low lost varieties.

Link Selection Guide

GUARANTEED LINKS

	Data Rate	Guaranteed Link Length 0-70° C HFBR-351X /361X Series Cable	Guaranteed Link Length 0-70° C HFBR-3530 Cable	Typical Link Lengths HFBR-351X /361X Series Cable	Typical Link Lengths HFBR-3530 Cable	Transmitter	Receiver	Page
5 MBd Link	5 MBd	12	17	35 m	48 m	HFBR-1510	HFBR-2501	4-8
1 MBd Link	1 MBd	24	34	55 m	76 m	HFBR-1502	HFBR-2502	4-10
Low Current Link	40 kBd	8	11	50 m	69 m	HFBR-1512	HFBR-2503	4-12
Extended Distance Link	40 kBd	60	82	110 m	152.5 m	HFBR-1512	HFBR-2503	4-12
Photo Interrupter Link	20 kHz	N/A	N/A	N/A	N/A	HFBR-1512	HFBR-2503	4-14
	500 kHz	N/A	N/A	N/A	N/A	HFBR-1502	HFBR-2502	4-14
Evaluation Kit, HFBR-0500	HFBR-1510 Transmitter, HFBR-2501 Receiver, 5 metre Connectored Cable, Bulkhead Feed-through, Connectors, Polishing Kit, Literature							

Component Selection Guide

TRANSMITTERS

	Minimum Output Optical Power 0 to 70° C	Peak Emission Wavelength	Page
HFBR-1510	–16.5 dBm	665 nm	11
HFBR-1502	–13.6 dBm	665 nm	11
HFBR-1512	–13.6 dBm	665 nm	11

RECEIVERS

	Sensitivity 0 to 70° C	Data Rate	Page
HFBR-2501	–21.6 dBm	5 MBd	12
HFBR-2502	–24 dBm	1 MBd	12
HFBR-2503	–39 dBm	40 kBd	14

CABLES

Page 15

Connectored Plastic Fiber Optic Cable

Single Channel	Dual Channel	Length* (metres)
HFBR-3510**	HFBR-3610**	Customer
HFBR-3530**	—	Specified
HFBR-3511	—	0.1
HFBR-3512	HFBR-3612	0.5
HFBR-3513	HFBR-3613	1
HFBR-3514	HFBR-3614	5
HFBR-3517	HFBR-3617	30
HFBR-3518	HFBR-3618	45
HFBR-3519	HFBR-3619	60

Unconnectored Plastic Fiber Optic Cable

Single Channel	Dual Channel	Length* (metres)
HFBR-3579	HFBR-3679	25
HFBR-3580	HFBR-3680	100
HFBR-3581	HFBR-3681	500
HFBR-3582 Selected (Low Loss)	—	500

*All cable lengths are +10%, –0% tolerance.

**HFBR-3510, HFBR-3530, HFBR-3610 Ordering Information. These cable assemblies of customer specified length have factory installed connectors. The length must be specified in 1 metre increments. The mandatory OPT 001 specifies the number of assemblies of equal length ordered.

EXAMPLE: To order 3 duplex cable assemblies, 21 metres each, specify:

HFBR-3610	Quantity 63
OPT 001	Quantity 3

CONNECTORS

Page 17

HFBR-4501 Gray Connector/Crimp Ring
HFBR-4511 Blue Connector/Crimp Ring
HFBR-4595 Polishing Kit
Polishing Fixture — Abrasive Paper
HFBR-4596 Polishing Fixture
Bulkhead Feedthrough/In-Line Splice
HFBR-4505 Gray
HFBR-4515 Blue

Mechanical Dimensions

Page 19

5 MBd Link

HFBR-1510 AND HFBR-2501

The dc to 5 MBd link is guaranteed over temperature to operate up to 17 m with a transmitter drive current of 60 mA. This link uses the 665 nm HFBR-1510 Transmitter, the HFBR-2501 Receiver, and HFBR-3530 Cable. The receiver compatible with LSTTL/TTL/CMOS logic levels offers a choice of an internal pull-up or open collector output.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Ref.
Ambient Temperature	T_A	0	70	°C	
Transmitter Peak Forward Current	$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	V_{CC}	4.75	5.25	V	Note 2
Fan-Out (TTL)	N		5		

SYSTEM PERFORMANCE Using HFBR-3510/3610 series cable under recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Data Rate		dc		5	MBd	BER $\leq 10^{-9}$	
Transmission Distance HFBR-351X/361X series cable	ℓ	12			m	$I_{FPK} = 60$ mA, 0–70° C	
		18	35		m	$I_{FPK} = 60$ mA, 25° C	
Transmission Distance HFBR-3530 cable		17			m	$I_{FPK} = 60$ mA, 0–70° C	
		24	48		m	$I_{FPK} = 60$ mA, 25° C	
Propagation Delay	t_{PLH}		80	140	ns	$R_L = 560\ \Omega$, $C_L = 30$ pF	Fig. 4, 5
	t_{PHL}		50	140	ns	$P_R = -21.6 \leq P_R \leq -9.5$ dBm	Note 3
Pulse Width Distortion	t_D		30		ns	$P_R = -15$ dBm $R_L = 560\ \Omega$, $C_L = 30$ pF	Fig. 4, 6 Note 4
EMI Immunity			8000		V/m	BER $\leq 10^{-9}$	

Notes: 1. For $I_{FPK} > 80$ mA, the duty factor must be such as to keep $I_{FAV} \leq 80$ mA. In addition, for $I_{FPK} > 80$ mA, the following rules for pulse width apply: $I_{FPK} \leq 160$ mA: Pulse width ≤ 1 ms $I_{FPK} > 160$ mA: Pulse width $\leq 1\ \mu s$

2. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. The propagation delay of 1 m of cable (5 ns) is included.
4. $T_D = t_{PLH} - t_{PHL}$.
5. Typical data is at 25° C, $V_{CC} = 5$ V.

Link Design Considerations

The HFBR-1510/2501 Transmitter/Receiver pair is guaranteed for operation at data rates up to 5 MBd over link distances from 0 to 12 metres with HFBR-351X/361X series cable and from 0 to 17 metres with HFBR-3530 cable. The value of transmitter drive current, I_F, depends on the link distance as shown in Figures 2 and 3. Note that there is an upper as well as a lower limit on the value of I_F for any given distance. The dotted lines in Figures 2 and 3 represent pulsed operation. When operating in the pulsed mode, the conditions in Note 1 must be met. After selecting a value of the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F}{I_F}$$

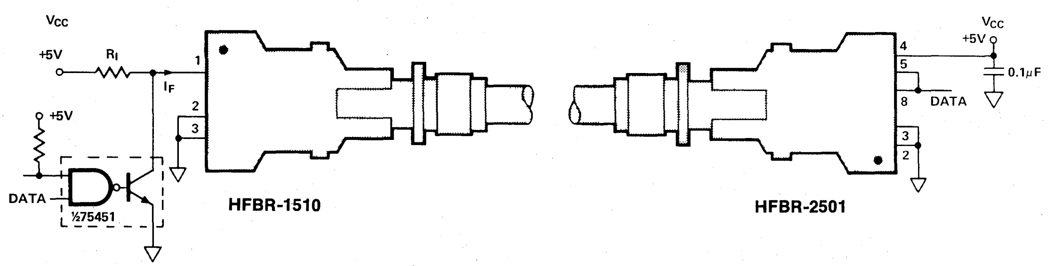


Figure 1. Typical Circuit Operation (5 MBd ≤ 12 m)

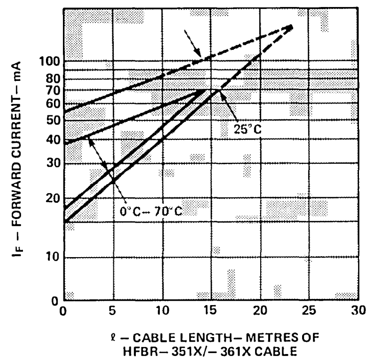


Figure 2. Guaranteed System Performance with HFBR-1510 and HFBR-2501

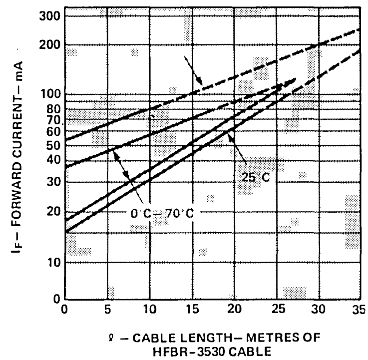


Figure 3. Guaranteed System Performance with HFBR-1510, HFBR-2501 and HFBR-3530 cable.

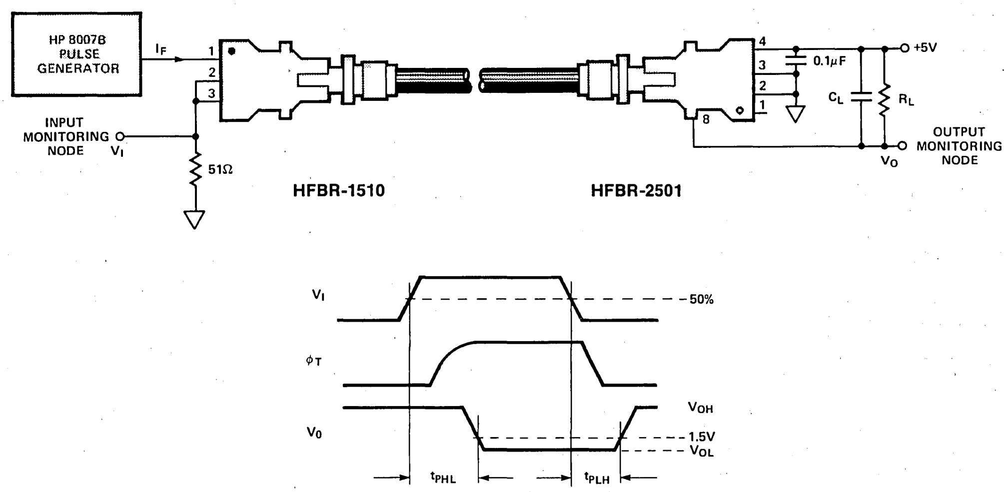


Figure 4. A.C. Test Circuit

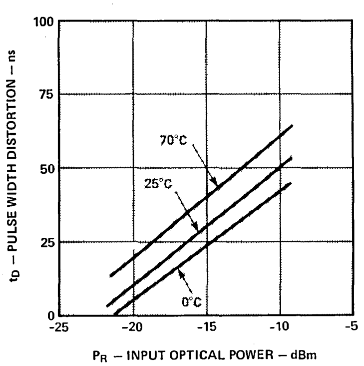


Figure 5. HFBR-1510/2501 Link Pulse Width Distortion vs. Optical Power

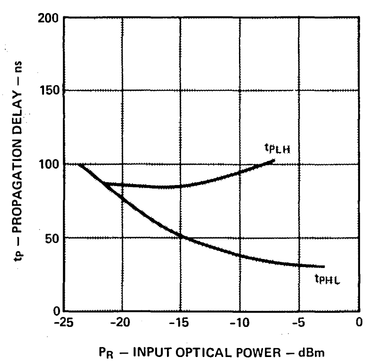


Figure 6. HFBR-1510/2501 Link Propagation Delay vs. Optical Power

FIBER OPTICS

1 MBd Link HFBR-1502 AND HFBR-2502

The dc to 1 MBd link is guaranteed over temperature to operate from 0 to 34 m with a transmitter drive current of 60 mA. This link uses the 665 nm HFBR-1502 Transmitter, the HFBR-2502 Receiver, and HFBR-3530 Cable. The receiver is compatible with LSTTL/TTL/CMOS logic levels and offers a choice of an internal pull-up or open collector output.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Ref.
Ambient Temperature	T_A	0	70	°C	
Transmitter Peak Forward Current	$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	V_{CC}	4.75	5.25	V	Note 2
Fan-Out (TTL)	N		5		

SYSTEM PERFORMANCE Using HFBR-3510/3610 series cable under recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Data Rate		dc		1	MBd	BER $\leq 10^{-9}$	
Transmission Distance HFBR-351X/361X series cable	ℓ	24			m	I_{FPK} = 60 mA, 0–70°C	
		30	55		m	I_{FPK} = 60 mA, 25°C	
Transmission Distance HFBR-3530 Cable	ℓ	34			m	I_{FPK} = 60 mA, 0–70°C	
		41	76		m	I_{FPK} = 60 mA, 25°C	
Transmission Distance 50% Duty Cycle - 351X/361X Series Cable	ℓ	30				I_{FPK} = 120 mA, 0–70°C	
		36	65			I_{FPK} = 120 mA, 25°C	
Transmission Distance 50% Duty Cycle - 3530 Cable	ℓ	41				I_{FPK} = 120 mA, 0–70°C	
		50	90			I_{FPK} = 120 mA, 25°C	
Propagation Delay	t_{PLH}		180	250	ns	R_L = 560 Ω, C_L = 30 pF	Fig. 4, 5
	t_{PHL}		100	140	ns	P_R = −24 dBm	Note 3
Pulse Width Distortion	t_D		80		ns	P_R = −24 dBm, R_L = 560 Ω, C_L = 30 pF	Fig. 4, 6 Note 4
EMI Immunity			8000		V/m	BER $\leq 10^{-9}$	

Notes: 1. For I_{FPK} > 80 mA, the duty factor must be such as to keep $I_{FAV} \leq$ 80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply: $I_{FPK} \leq$ 160 mA: Pulse width $\leq$ 1 ms I_{FPK} > 160 mA: Pulse width $\leq$ 1 μs
2. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. The propagation delay of 1 m of cable (5 ns) is included. 4. $T_D = t_{PLH} - t_{PHL}$. 5. Typical data is at 25°C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1502/2502 Transmitter/Receiver pair is guaranteed for operation at data rates up to 1 MBd over link distances from 0 to 24 metres with HFBR-351X/361X series cable and from 0 to 34 metres with HFBR-3530 cable. The value of transmitter drive current, I_F, depends on the link distance as shown in Figures 2 and 3. Note that there is a lower limit on the value of I_F for any given distance. The dotted lines in Figures 2 and 3 represent pulsed operation.

When Operating in the pulsed mode, the conditions in Note 1 must be met. After selecting a value of the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F - V_{OL}\ (75451)}{I_F}$$

For the HFBR-1502/2502 pair, the value of the capacitor, C_1 (Figure 1) must be chosen such that $R_1 C_1 \leq$ 75 ns.

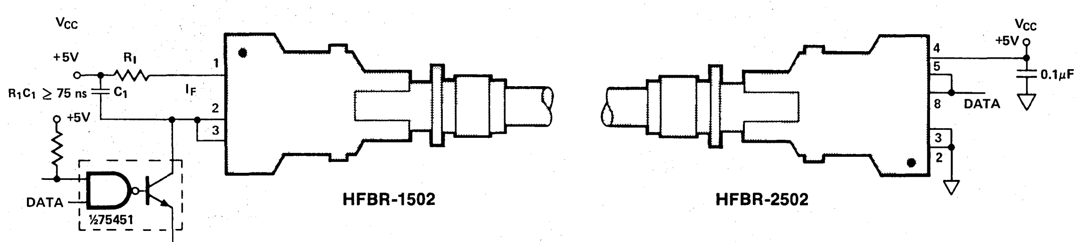


Figure 1. Typical Circuit Operation (1 MBd ≤ 24 m)

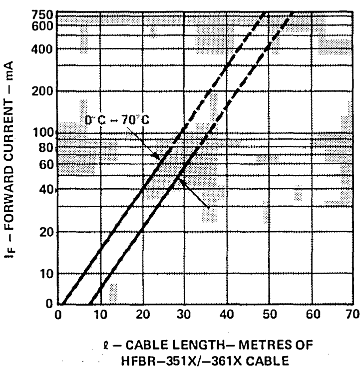


Figure 2. Guaranteed System Performance with HFBR-1502 and HFBR-2502

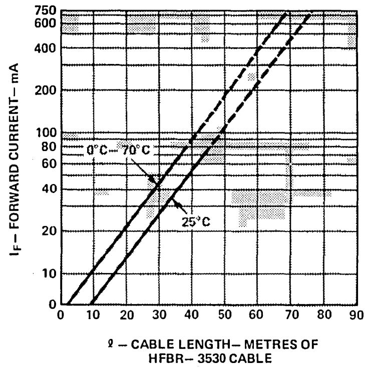


Figure 3. Guaranteed System Performance with HFBR-1502, HFBR-2502 and HFBR-3530 cable.

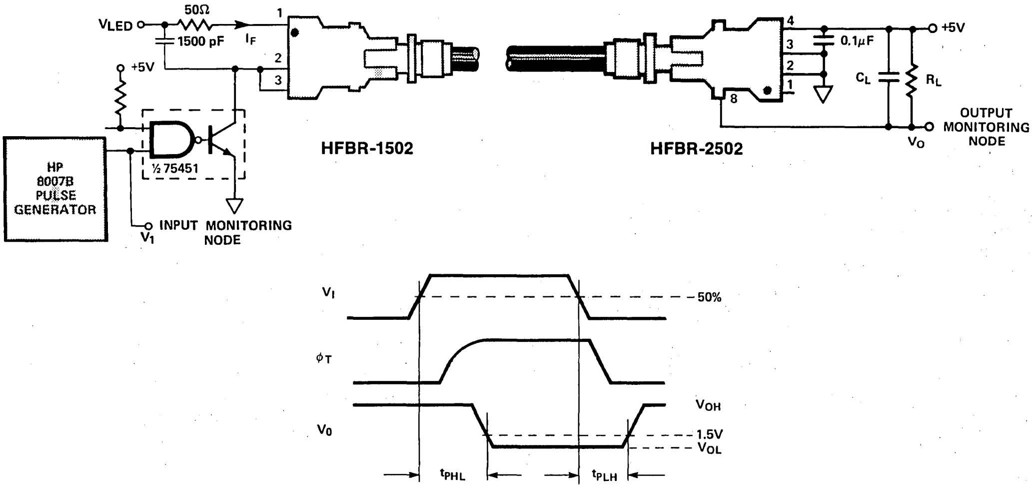


Figure 4. A.C. Test Circuit

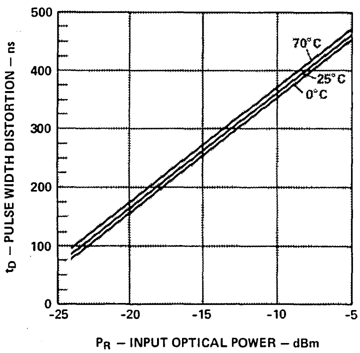


Figure 5. HFBR-1502/2502 Link Pulse Width Distortion vs. Optical Power

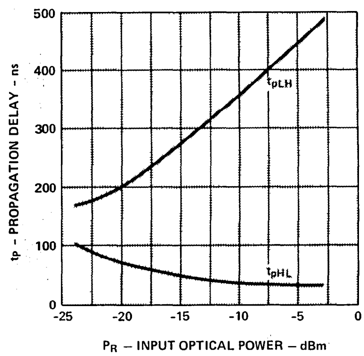


Figure 6. HFBR-1502/2502 Link Propagation Delay vs. Optical Power

Low Current/Extended Distance Link

HFBR-1512 AND HFBR-2503

The low current link requires only 6 mA peak supply current for the transmitter and receiver combined to achieve an 11 m link. Extended distances up to 82 m can be achieved at a maximum transmitter drive current of 60 mA peak. This link can be driven with TTL/LSTTL and most CMOS logic gates.

The black plastic housing of the HFBR-1512 Transmitter is designed to prevent the penetration of ambient light into the cable through the transmitter. This prevents the sensitive receiver from being triggered by ambient light pulses.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Ref.
Ambient Temperature	T_A	0	70	°C	
Transmitter Peak Forward Current	$I_{F\,PK}$	2	120	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	V_{CC}	4.5	5.5	V	Note 2
Output Voltage	V_O		V_{CC}	V	
Fan-Out (TTL)	N		1		

SYSTEM PERFORMANCE Using HFBR-3510/3610 series cable under recommended operating conditions unless otherwise otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Data Rate		dc		40	kBd	$t_D \leq 7.0\ \mu s$	
Transmission Distance HFBR-351X/361X series cable	ℓ	8	50		m	$I_{FPK} = 2$ mA, 0–70°C	
		60	110		m	$I_{FPK} = 60$ mA, 0–70°C	
Transmission Distance HFBR-3530 cable	ℓ	11	69		m	$I_{FPK} = 2$ mA, 0–70°C	
		82	152		m	$I_{FPK} = 60$ mA, 0–70°C	
Propagation Delay	t_{PLH}		4		μs	$R_L = 3.3K\ \Omega$, $C_L = 30$ pF	Fig. 4, 5
	t_{PHL}		2.5		μs	$P_R = -25$ dBm	Note 3
Pulse Width Distortion	t_D			7.0	μs	$-39 \leq P_R \leq -14$ dBm $R_L = 3.3\ K\Omega$, $C_L = 30$ pF	Fig. 4, 6 Note 4
Bit Error Rate	BER		10^{-9}			$P_R = -30$ dBm	
EMI Immunity			5000		V/m	$P_R = 0$ mW	

Notes:

1. For $I_{FPK} > 80$ mA, the duty factor must be such as to keep $I_{FAV} \leq 80$ mA. In addition, if $I_{FAV} > 80$ mA, then the pulse width must be equal to or less than 1 ms.
2. It is recommended that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver.
3. The propagation delay of 1 m of cable (5 ns) is included.
4. $t_D = t_{PLH} - t_{PHL}$.
5. Typical data is at 25°C, $V_{CC} = 5$ V.

Link Design Considerations

The HFBR-1512/2503 Transmitter/Receiver pair is guaranteed for operation at data rates up to 40 kBd for transmitter drives as low as 2 mA. The value of transmitter drive current, I_F, depends on the link distance as shown in Figures 2 and 3. Note that there is an upper as well as a lower limit on the value of I_F for any given distance. After selecting a value of the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F}{I_F}$$

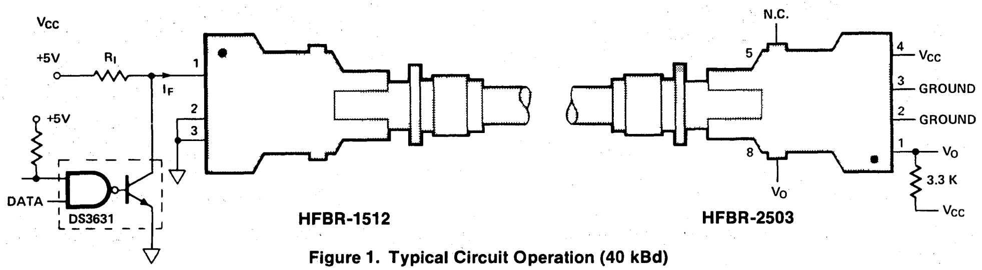


Figure 1. Typical Circuit Operation (40 kBd)

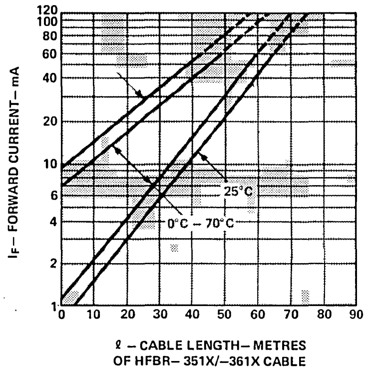


Figure 2. Typical Circuit Operation (40 kBd)

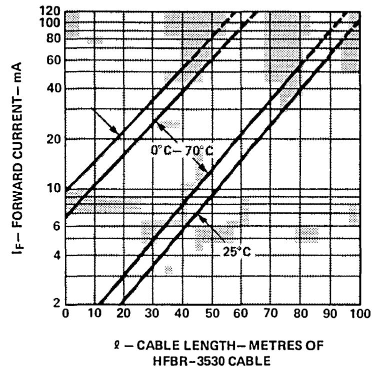


Figure 3. Guaranteed System Performance with HFBR-1512 and HFBR-2503

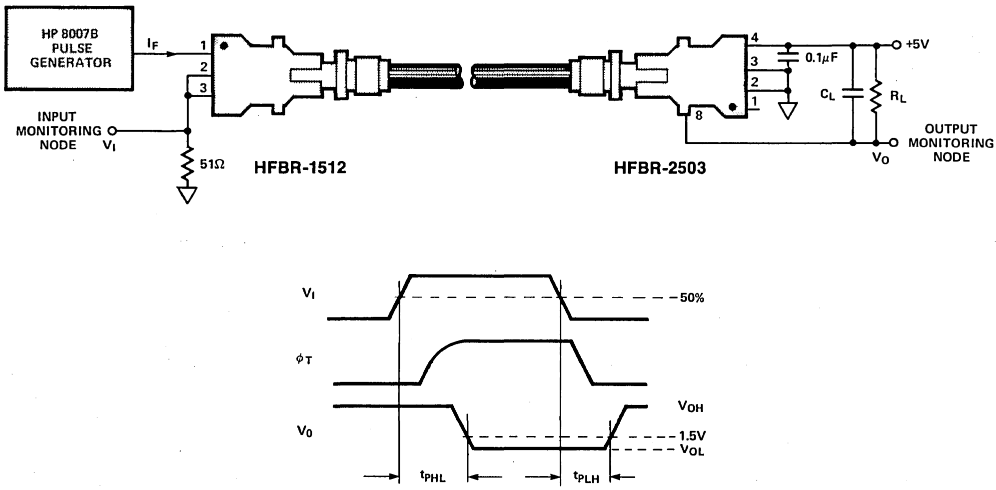


Figure 4. A.C. Test Circuit

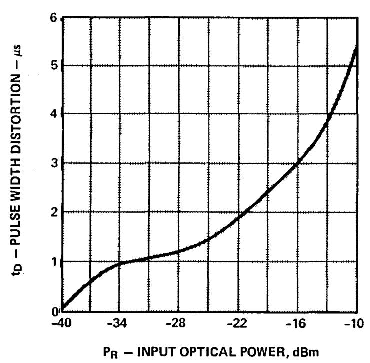


Figure 5. HFBR-1512/2503 Link Pulse Width Distortion vs. Optical Power

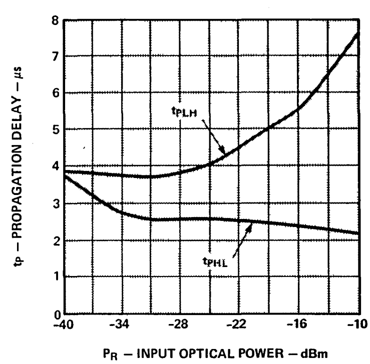


Figure 6. HFBR-1512/2503 Link Propagation Delay vs. Optical Power

Photo Interrupter Links

HFBR-1502/2502
HFBR-1512/2503

These links may be used in optical switches, shaft position sensors, and velocity sensors. They are particularly useful where high voltage, electrical noise, or explosive environments prohibit the use of electromechanical or optoelectronic sensors.

The HFBR-1512/2503 link (20 kHz) has an optical power budget of 24 dB, and the HFBR-1502/2502 link (500 kHz) budget is 10 dB. Total system losses (cable attenuation, air-gap loss, etc) must not exceed the link optical power budget.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min.	Max.	Units	Ref.
Ambient Temperature		T_A	0	70	°C	
Transmitter Peak Forward Current		$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current		$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	HFBR-2503	V_{CC}	4.50	5.50	V	Note 2
	HFBR-2502		4.75	5.25		
Output Voltage	HFBR-2503	V_O		V_{CC}	V	
	HFBR-2502			18		
Fanout (TTL)	HFBR-2503			1		
	HFBR-2502			5		

SYSTEM PERFORMANCE

See HFBR-1502/2502 link data sheet (page 4-10) and HFBR-1512/2503 link data sheet (page 4-12) for more design information. These specifications apply when using HFBR-3510/3610 series cable and, unless otherwise specified, under recommended operating conditions.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
HFBR-1512/HFBR-2503							
Max. Count Frequency		dc		20	kHz		
Optical Power Budget		25.4			dB	I_{FPK} = 60 mA, 0–70° C	Note 3, 4
		27.8	34		dB	I_{FPK} = 60 mA, 25° C	
HFBR-1502, HFBR-2502							
Max. Count Frequency		dc		500	kHz		
Optical Power Budget		10.4			dB	I_{FPK} = 60 mA, 0–70° C	Note 3
		12.8	15.6		dB	I_{FPK} = 60 mA, 25° C	

Notes:

1. For $I_{FPK} > 80$ mA, the duty factor must be such as to keep $I_{FAV} \leq 80$ mA. In addition, for $I_{FPK} > 80$ mA, the following rules for pulse width apply:
   $I_{FPK} \leq 160$ mA: Pulse width ≤ 1 ms
   $I_{FPK} > 160$ mA: Pulse width ≤ 1 μs
2. A bypass capacitor (0.01 μF to 0.1 μF ceramic) connected from pin 3 to pin 4 of the receiver is recommended for the HFBR-2503 and essential for the HFBR-2502. For the HFBR-2502, the total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. Optical Power Budget = P_T Min. – $P_{R(L)}$ Min. Refer to HFBR-1502/1512 data sheet, page 4-16; HFBR-2502 data sheet, page 4-17; and HFBR-2503 data sheet, page 4-19 for additional design information.
4. In addition to a minimum power budget, care should be taken to avoid overdriving the HFBR-2503 receiver with too much optical power. For this reason power levels into the receiver should be kept less than –13.7 dBm to eliminate any overdrive with the recommended operating conditions.
5. Typical data is at 25°C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1512/2503 and HFBR-1502/2502 Transmitter/Receiver pairs are intended for applications where the photo interrupter must be physically separate from the optoelectronic emitter and detector. This separation would be useful where high voltage, electrical noise or explosive environments prohibit the use of electronic devices. To ensure reliable long term operation, links designed for this application should operate with an ample optical power margin $\alpha_M \geq 3$ dB, since the exposed fiber ends are subject to environmental contamination that will increase the optical attenuation of the slot with time. A graph of air gap separation versus attenuation for clean fiber ends with minimum radial error ≤ 0.005 inches (0.127 mm) and angular error ($\leq 3.0°$) is provided in Figure 2. The following equations can now be used to determine the transmitter output power, P_T, for both the overdrive and minimum drive cases. Overdrive is defined as a condition where excessive optical power is delivered to the receiver. The first equation enables the maximum P_T that will not result in receiver overdrive to be calculated for a predetermined link length and slot attenuation. The second equation defines the minimum P_T allowed for link operation.

$$P_T\,(MAX) - P_R\,(MAX) \leq \alpha_{O\ MIN}\,\ell + \alpha_{SLOT} \qquad \text{Eq. 1}$$

$$P_T\,(MIN) - P_{RL}\,(MIN) \geq \alpha_{O\ MAX}\,\ell + \alpha_{SLOT} + \alpha_M \qquad \text{Eq. 2}$$

Once P_T (MIN) has been determined in the second equation for a specific link length (ℓ), slot attenuation (α_{SLOT}) and margin (α_M), Figure 3 can then be used to find I_F.

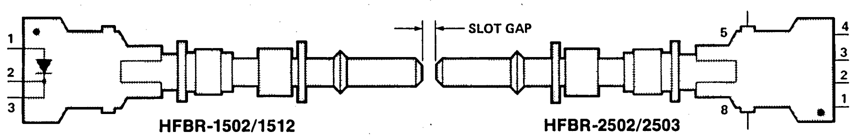


Figure 1. Typical Slot Interrupter Configuration. Refer to 1 MBd or Low Current Links for Schematic Diagrams

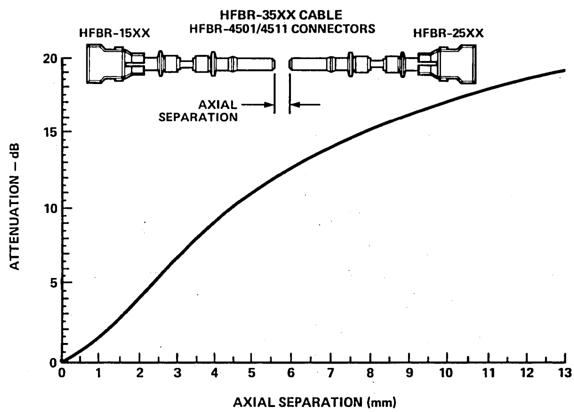


Figure 2. Typical Attenuation vs. Axial Separation

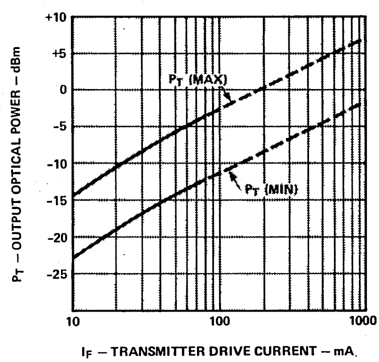


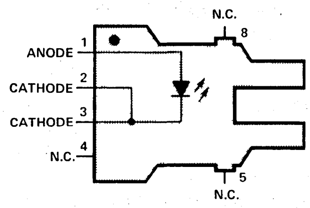
Figure 3. Typical HFBR-1502/1512 Optical Output Power vs. Transmitter I_F (0—70° C)

665 nm Transmitters

HFBR-1502/HFBR-1510 and HFBR-1512

The HFBR-1510/1502/1512 Transmitter modules incorporate a 665 nm LED emitting at a low attenuation wavelength for the HFBR-3510/3610 plastic fiber optic cable. The transmitters can be easily interfaced to standard TTL logic. The optical power output of the HFBR-1510/1512/1502 is specified at the end of 0.5 m of cable. The HFBR-1512 output optical power is tested and guaranteed at low drive currents.

HFBR-1510/1512/1502 Transmitter



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	−40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec.	
Peak Forward Input Current		$I_{F\ PK}$		1000	mA	Note 2
Average Forward Input Current		$I_{F\ AV}$		80	mA	
Reverse Input Current		V_R		5	V	

Electrical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	HFBR-1510	P_T	−16.5		−7.6	dBm	I_F = 60 mA, 0–70°C	
			−14.1		−8.4	dBm	I_F = 60 mA, 25°C	
	HFBR-1502 and HFBR-1512	P_T	−13.6		−4.5	dBm	I_F = 60 mA, 0–70°C	Fig. 2
			−11.2		−5.4	dBm	I_F = 60 mA, 25°C	Note 4
	HFBR-1512	P_T	−35.5			dBm	I_F = 2 mA, 0–70°C	Note 3
Output Optical Power Temperature Coefficient		$\frac{\Delta P_T}{\Delta T}$		−0.026		dB/°C		
Peak Emission Wavelength		λ_{PK}		665		nm		
Forward Voltage		V_F	1.45	1.67	2.02	V	I_F = 60 mA	
Forward Voltage Temperature Coefficient		$\frac{\Delta V_F}{\Delta T}$		−1.37		mV/°C		Fig. 1
Effective Diameter		D_T		1		mm		
Numerical Aperture		N.A.		0.5				
Reverse Input Breakdown Voltage		V_{BR}	5.0	12.4		V	I_F = −10 μA, T_A = 25°C	
Diode Capacitance		C_O		86		pF	V_F = 0, f = 1 MHz	
Rise and Fall Time		t_R, t_F		50		ns	10% to 90%	

Notes:
1. 1.6 mm below seating plane.
2. 1 μs pulse, 20 μs period.
3. Measured at the end of 0.5 m HFBR-3512 Fiber Optic Cable with large area detector.
4. Optical power, P (dBm) = 10 Log P (μW)/1000 μW.
5. Typical data is at 25°C.

WARNING. When viewed under some conditions, the optical port of the Transmitter may expose the eye beyond the Maximum Permissible Exposure recommended in ANSI Z-136-1, 1981. Under most viewing conditions there is no eye hazard.

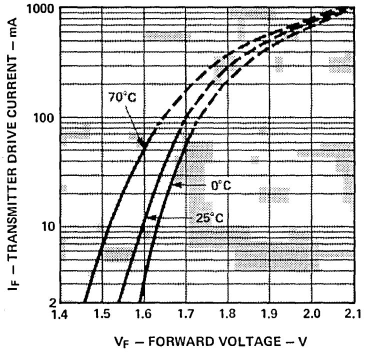


Figure 1. Typical Forward Voltage vs. Drive Current for HFBR-1510/1502/1512

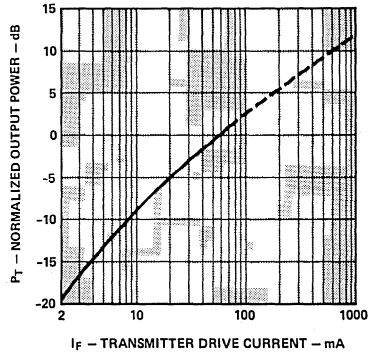


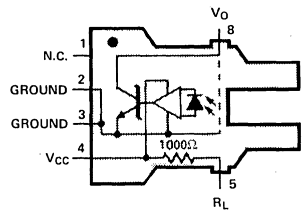
Figure 2. Normalized HFBR-1510/1502/1512 Typical Output Optical Power vs. Drive Current

Receivers

HFBR-2501 (5 MBd) and HFBR-2502 (1 MBd)

The HFBR-2501/2502 Receiver modules feature a shielded integrated photodetector and wide bandwidth DC amplifier for high EMI immunity. A Schottky clamped open-collector output transistor allows interfacing to common logic families and enables "wired-OR" circuit designs. The open collector output is specified up to 18V. An integrated 1000 ohm resistor internally connected to V_{CC} may be externally jumpered to provide a pull-up for ease-of-use with +5V logic. The combination of high optical power levels and fast transitions falling edge could result in distortion of the output signal (HFBR-2502 only), that could lead to multiple triggering of following circuitry.

HFBR-2501/2502 Receiver



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7	V	Note 6
Output Collector Current		I_O		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	-0.5	18	V	
Pullup Voltage		V_{RL}	-0.5	V_{CC}	V	

FIBER OPTICS

Electrical/Optical Characteristics 0° C to +70° C, 4.75 ≤ V_{CC} ≤ 5.25 Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2501	$P_{R\,(L)}$	−21.6		−9.5	dBm	0-70° C, V_{OL} = 0.5 V, I_{OL} = 8 mA	Note 2, 3
			−21.6		−8.7	dBm	25° C, V_{OL} = 0.5 V, I_{OL} = 8 mA	
	HFBR-2502	$P_{R\,(L)}$	−24			dBm	0-70° C, V_{OL} = 0.5 V, I_{OL} = 8 mA	
			−24			dBm	25° C, V_{OL} = 0.5 V, I_{OL} = 8 mA	
Input Optical Power Level for Logic "1"		P_R (H)			−43	dBm	V_{OH} = 5.25 V, I_{OH} ≤ 250 μA	Note 2
High Level Output Current		I_{OH}		5	250	μA	V_O = 18 V, P_R = 0	Note 4
Low Level Output Voltage		V_{OL}		0.4	0.5	V	I_{OL} = 8 mA, P_R = $P_{RL\ MIN}$	Note 4
High Level Supply Current		I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V, P_R = 0 μW	Note 4
Low Level Supply Current		I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V, P_R = −12.5 dBm	Note 4
Effective Diameter		D_R		1		mm		
Numerical Aperture		$N.A._R$		0.5				
Internal Pull-Up Resistor		R_L		1000		Ohms		

Notes:

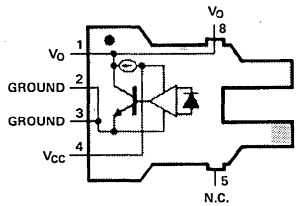
1. 1.6 mm below seating plane.
2. Optical flux, P (dBm) = 10 Log P (μW)/1000 μW.
3. Measured at the end of HFBR-3510 Fiber Optic Cable with large area detector.
4. R_L is open.
5. Typical data is at 25° C, V_{CC} = 5 V.
6. It is essential that a bypass capacitor 0.01 μF to 0.1 μF be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.

High Sensitivity Receiver

HFBR-2503

The blue plastic HFBR-2503 Receiver module has a sensitivity of –39 dBm. It features an integrated photodetector and DC amplifier for high EMI immunity. The output is an open collector with a 150 μA internal current source pull-up and is compatible with TTL/LSTTL and most CMOS logic families. For minimum rise time add an external pull-up resistor of at least 3.3K ohms. V_{CC} must be greater than or equal to the supply voltage for the pull-up resistor.

HFBR-2503 Receiver



FIBER OPTICS

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	–40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	–0.5	7	V	Note 7
Output Collector Current (Average)		I_O	–1	5	mA	
Output Collector Power Dissipation		P_{OD}		25	mW	
Output Voltage		V_O	–0.5	V_{CC}	V	

Electrical/Optical Characteristics 0° C to +70° C, $4.5 \leq V_{CC} \leq 5.5$ Unless Otherwise Specified

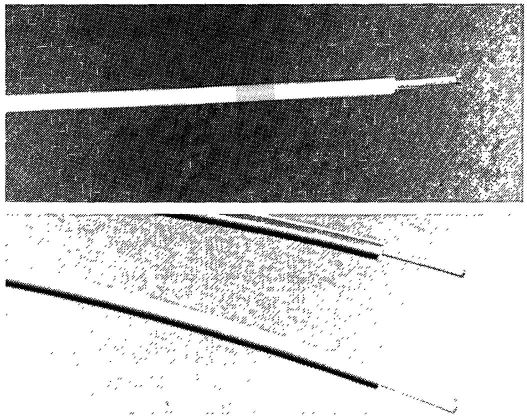
Parameter		Symbol	Min.	Typ. (5)	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2503	$P_{R(L)}$	–39		–13.7	dBm	0-70° C, $V_O = V_{OL}$, $I_{OL} = 3.2$ mA	Note 2, 3, 4
			–39		–13.3	dBm	25° C, $V_O = V_{OL}$, $I_{OL} = 3.2$ mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			–53	dBm	$V_{OH} = 5.5V$, $I_{OH} \leq 40\ \mu A$	Note 2
High Level Output Voltage		V_{OH}	2.4			V	$I_{OH} = -40\ \mu A$, $P_R = 0\ \mu W$	
Low Level Output Voltage		V_{OL}			0.4	V	$I_{OL} = 3.2$ mA, $P_R = P_{RL\ MIN}$	Note 6
High Level Supply Current		I_{CCH}		1.2	1.9	mA	$V_{CC} = 5.5V$, $P_R = 0\ \mu W$	
Low Level Supply Current		I_{CCL}		2.9	3.7	mA	$V_{CC} = 5.5V$, $P_R \geq P_{RL}$ (MIN)	Note 6
Effective Diameter		D_R		1		mm		
Numerical Aperture		$N.A._R$		0.5				

Notes:

1. 1.6 mm below seating plane.
2. Optical flux, P (dBm) = 10 Log P (μW)/1000 μW.
3. Measured at the end of the HFBR-3510 Fiber Optic Cable with large area detector.
4. Because of the very high sensitivity of the HFBR-2503, the digital output may switch in response to ambient light levels when a cable is not occupying the receiver optical port. The designer should take care to filter out signals from this source if they pose a hazard to the system.
5. Typical data is at 25° C, $V_{CC} = 5$ V.
6. Including current in 3.3K pull-up resistor.
7. It is recommended that a bypass capacitor 0.01 μF to 0.1 μF ceramic be connected from pin 3 to pin 4 of the receiver.

Plastic Fiber Optic Cable

HFBR-3510/HFBR-3530



High performance plastic fiber optic cable is available in two varieties: standard low loss cable (HFBR-351X and HFBR-361X) and selected super low loss simplex cable (HFBR-3530). The HFBR-3510/3530 Simplex Fiber Optic Cable is constructed of a single step index plastic fiber sheathed in a PVC jacket. The HFBR-3610 Duplex Fiber Optic Cable has two plastic fibers, each in a cable of construction similar to the Simplex Cable, joined with a web. The individual channels are identified by a marking on one channel of the cable.

These cables are UL recognized components and pass UL VW-1 flame retardancy specification. The cable's safety in flammable environments, and non-conductive electrical properties may make the use of conduit unnecessary.

The HFBR-3510/3610 Connectored Fiber Optic Cables are available in fixed lengths ranging from 0.1 m to 60 m. Connectored cables may also be ordered in customer specified lengths of metre increments. HFBR-3530 Connectored Fiber Optic cable may be ordered in customer specified lengths of one metre increments.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Installation Temperature		T_I	-20	+70	°C	
Short Term	(Single Channel)	F_T		50	N	
Tensile Force	(Dual Channel)	F_T		100	N	Note 1
Short Term Bend Radius		r	10		mm	Note 2
Long Term Bend Radius		r	35		mm	
Long Term Tensile Load		F_T		1	N	
Flexing				1000	Cycles	Note 3
Impact		m		0.5	Kg	Note 4
		h		150	mm	

Electrical/Optical Characteristics 0° C to +70° C Unless Otherwise Specified

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Cable Attenuation HFBR-351X/HFBR-361X	α_o	0.19	0.31	0.43	dB/m	Source is HFBR-1502/1510/1512 (665 nm), $\ell = 20$ m	[6]
HFBR-3530	α_o	0.19	0.25	0.31	dB/m		
Numerical Aperture	N.A.		0.5			$\ell > 2$ m	
Diameter, Core	D_C		1.0		mm		
Diameter, Jacket	D_J		2.2		mm	Simplex Cable	
Travel Time Constant	W		5.0		nsec/m		
Mass per Unit Length/ Channel	m/ℓ		4.6		g/m	Without Connectors	
Cable Leakage Current	I_L		12		nA	50 kV, $\ell = 0.3$m	

Notes:
1. Less than 30 minutes.
2. Less than 1 hour, non-operating.
3. 90° bend on 10 mm radius mandrel.
4. Tested at 1 impact according to MIL-STD-1678, Method 2030, Procedure 1.
5. Typical data is at 25° C.
6. In addition to standard Hewlett-Packard 100% product testing, HP provides additional margin to ensure link performance. Under certain conditions, cable installation and improper connectoring may reduce performance. Contact Hewlett-Packard for recommendations.

Ordering Guide

HFBR-3510/3610 FIBER CABLE

Connectored Plastic Fiber Optic Cable

Single Channel	Dual Channel	Length* (metres)
HFBR-3510** HFBR-3530**	HFBR-3610** —	Customer Specified
HFBR-3511	—	0.1
HFBR-3512	HFBR-3612	0.5
HFBR-3513	HFBR-3613	1
HFBR-3514	HFBR-3614	5
HFBR-3515	HFBR-3615	10
HFBR-3516	HFBR-3616	20
HFBR-3517	HFBR-3617	30
HFBR-3518	HFBR-3618	45
HFBR-3519	HFBR-3619	60

Unconnectored Plastic Fiber Optic Cable

Single Channel	Dual Channel	Length* (metres)
HFBR-3579	HFBR-3679	25
HFBR-3580	HFBR-3680	100
HFBR-3581	HFBR-3681	500
HFBR-3582 Selected (Low Loss)	—	500

*All Cable Lengths are +10%, −0% tolerance.

**HFBR-3510, HFBR-3530 and HFBR-3610 ordering information. These cable assemblies of customer specified length have installed connectors. The length must be specified in 1 metre increments. The mandatory OPT 001 specifies the number of assemblies of equal length ordered.

EXAMPLE: To order 2 duplex cable assemblies, 21 metres each, specify:

HFBR-3610 Quantity 63
OPT 001 Quantity 3

HFBR-3500/3600 FIBER CABLE (Not recommended for new designs.)

Electrical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Cable Attenuation	α_0	0.3	0.45	0.63	dB/m	at 665 nm Source NA = 0.5	
Numerical Aperture	N.A.		0.5			$\ell > 2$m	
Diameter, Core	D_C		1.0		mm		
Diameter, Jacket	D_J		2.3		mm	Simplex Cable	
Travel Time Constant	l/V		5.0		nsec/m		
Mass per Unit Length/Cable	m/ℓ		4.6		g/m	Without Connectors	
Cable Leakage Current	I_L		1		nA	50 kV, $\ell = 0.3$m	

Ordering Guide

HFBR-3500/3600

The cables listed below are still available from Hewlett-Packard. However, the newer HFBR-3510/3610 series shown above offers higher performance.

Connectored Plastic Fiber Optic Cable

Single Channel	Dual Channel	Length (metres)
HFBR-3500	HFBR-3600	Customer Specified
HFBR-3501	—	0.1
HFBR-3502	HFBR-3602	0.5
HFBR-3503	HFBR-3603	1
HFBR-3504	HFBR-3604	5
HFBR-3505	HFBR-3605	10
HFBR-3506	HFBR-3606	15
HFBR-3507	HFBR-3607	20
HFBR-3508	HFBR-3608	25

Unconnectored Plastic Fiber Optic Cable

Single Channel	Dual Channel	Length (metres)
HFBR-3589	HFBR-3689	25
HFBR-3590	HFBR-3690	100
HFBR-3591	HFBR-3691	500

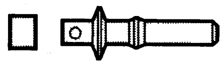
Snap-in Fiber Optic Connector, Bulkhead Feedthrough/Splice and Polishing Tools

HFBR-4501/4511 CONNECTORS
HFBR-4505/4515 BULKHEAD FEEDTHROUGHS

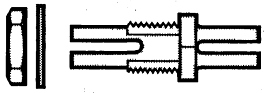
The HFBR-4501 and HFBR-4511 snap-in connectors terminate low cost plastic fiber cable and mate with the Hewlett-Packard HFBR-0500 family of fiber optic transmitters and receivers. They are quick and easy to install. The metal crimp ring provides strong and stable cable retention and the polishing technique ensures a smooth optical finish which results in consistently high optical coupling efficiency.

The HFBR-4505 and HFBR-4515 bulkhead feedthroughs mate two snap-in connectors and can be used either as an in-line splice or as a panel feedthrough for plastic fiber cable. The connector to connector loss is low and repeatable.

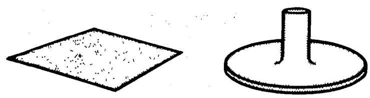
HFBR-4501 (GRAY)/4511 (BLUE) CONNECTOR



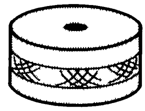
HFBR-4505 (GRAY)/4515 (BLUE) BULKHEAD FEEDTHROUGH



HFBR-4595 POLISHING KIT

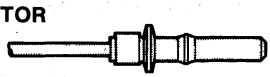


HFBR-4596 HARDENED STEEL POLISHING FIXTURE

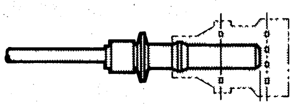


Applications

- **CONNECTOR**

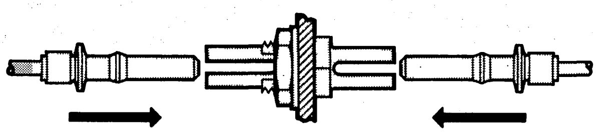


TERMINATION FOR HEWLETT-PACKARD HFBR-35XX/36XX FIBER OPTIC CABLE

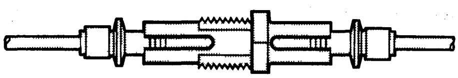


INTERFACE TO HEWLETT-PACKARD HFBR-15XX/25XX SNAP-IN FIBER OPTIC LINK COMPONENTS

- **BULKHEAD FEEDTHROUGH**



BULKHEAD FEEDTHROUGH OR PANEL MOUNTING OF HFBR-45XX CONNECTORS



IN-LINE SPLICE FOR HFBR-35XX/36XX FIBER OPTIC CABLE

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+75	°C	
Operating Temperature	T_A	0	+70	°C	
Nut Torque HFBR-4505/4515	T_N		$\frac{0.7}{100}$	$\frac{\text{N-m}}{\text{OzF-IN}}$	1

Notes:
1. Recommended nut torque is $\frac{0.57}{80}$ $\frac{\text{N-m}}{\text{OzF-IN}}$

Mechanical/Optical Characteristics 0° to 70° C Unless Otherwise Specified.

Typical Data at 25° C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Retention Force Connector/Module HFBR-4501/4511 to HFBR-15XX/25XX	F_{RC}		6.8		N	
Tensile Force Connector/Cable	F_T		22		N	
HFBR-4505/4515 Conn. to Conn. Loss	α_{CC}	0.7	1.5	2.8	dB	2, 3
Retention Force Connector/ Bulkhead HFBR-4501/4511 to HFBR-4505/4515	F_{RB}		7.8		N	

Notes:
2. Factory polish or field polish per recommended procedure.
3. Module to connector insertion loss is factored into the transmitter output optical power and the receiver input optical power level specifications.

Note:
For applications where frequent temperature cycling over extremes is expected please contact Hewlett-Packard for alternate connectoring techniques.

Cable Terminations

The following easy procedure describes how to make cable terminations. It is ideal for both field and factory installaiton. If a high volume connectoring technique is required please contact your Hewlett-Packard sales engineer for the recommended procedure and equipment.

Connectoring the cable is accomplished with the Hewlett-Packard HFBR-4595 Polishing Kit consisting of a Polishing Fixture and 600 grit abrasive paper and 3 micron pink lapping film (3M Company, OC3-14). No adhesive material is needed to secure the cable in the connector, and the connector can be used immediately after polishing.

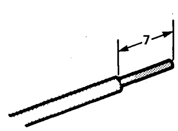
Connectors may be easily installed on the cable ends with readily available tools. Materials needed for the terminating procedure are:

1) HFBR-35XX/36XX Fiber Optic Cable
2) HFBR-4595 Polishing Kit
3) HFBR-4501 Gray Connector and Crimp Ring
4) HFBR-4511 Blue Connector and Crimp Ring
5) Industrial razor blade or wire cutters
6) 16 gauge latching wire strippers
7) Crimp Tool, AMP 90364-2

Step 1

The zip cord structure of the HFBR-36XX duplex cable permits easy separation of the channels. The channels should be separated approximately 50 mm (2.0 in.) back from the ends to permit connectoring and polishing.

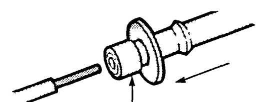
After cutting the cable to the desired length, strip off approximately 7 mm (0.3 in) of the outer jacket with the 16 gauge wire strippers. Excess webbing on duplex cable may have to be trimmed to allow the connector to slide over the cable.



Step 2

Place the crimp ring and connector over the end of the cable; the fiber should protrude about 3 mm (0.12 in.) through the end of the connector. Carefully position the ring so that it is entirely on the connector and then crimp the ring in place with the crimping tool.

Note: *Place the gray connector on the cable end to be connected to the transmitter and the blue connector on the cable end to be connected to the receiver to maintain the color coding (both connectors are the same mechanically).*



Step 3

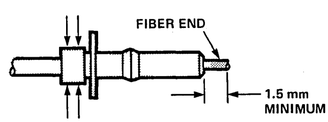
Any excess fiber protruding from the connector end may be cut off; however, the trimmed fiber should extend at least 1.5 mm (0.06 in.) from the connector end.

Insert the connector fully into the polishing fixture with the connector end protruding from the bottom of the fixture.

For high volume connectoring use the hardened steel HFBR-4596 polishing fixture.

Note: *The four dots on the bottom of the polishing fixture are wear indicators. Replace the polishing fixture when any dot is no longer visible.*

Place the 600 grit abrasive paper on a flat smooth surface. Pressing down on the connector, polish the fiber and the connector until the connector is flush with the end of the polishing fixture. Wipe the connector and fixture with a clean cloth or tissue.

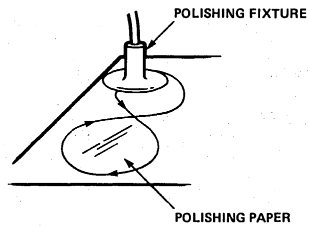


Step 4

Place the flush connector and polishing fixture on the dull side of the 3 micron pink lapping film and continue to polish the fiber and connector for approximately 25 strokes. The fiber end should be flat, smooth and clean.

The cable can now be used.

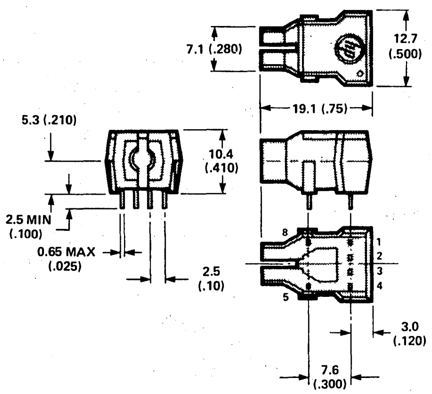
Note: *Use of the pink lapping film fine polishing step results in approximately a 2 dB improvement in coupling performance of either a transmitter-receiver link or a bulkhead/splice over 600 grit polish alone. This polish is comparable to Hewlett-Packard's factory polish. The fine polishing step may be omitted where an extra 2 dB of optical power is not essential as with short link lengths.*



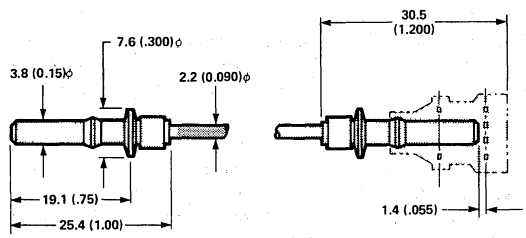
Mechanical Dimensions

All dimensions in mm (inches).
All dimensions ±0.25 mm unless otherwise specified.

HFBR-15XX (GRAY OR BLACK)/250X (BLUE) MODULE

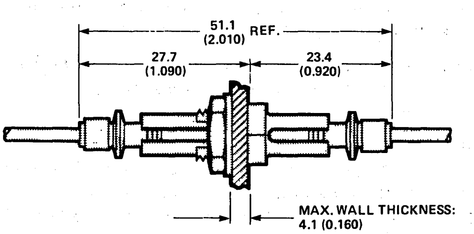


HFBR-4501 (GRAY)/4511 (BLUE) CONNECTOR

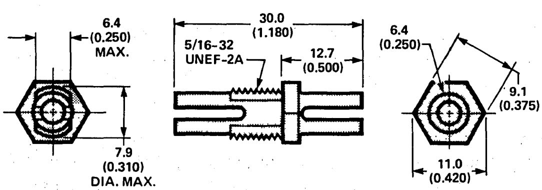


CONNECTORS DIFFER ONLY IN COLOR

BULKHEAD FEEDTHROUGH WITH TWO HFBR-4501/4511 CONNECTORS

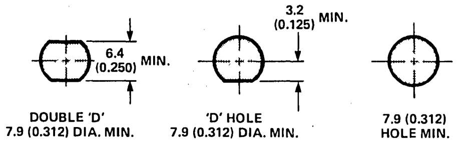


HFBR-4505 (GRAY)/4515 (BLUE) BULKHEAD FEEDTHROUGH



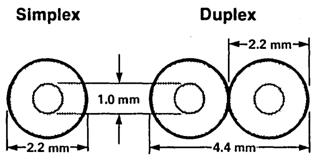
BULKHEAD FEEDTHROUGHS DIFFER ONLY IN COLOR

PANEL MOUNTING

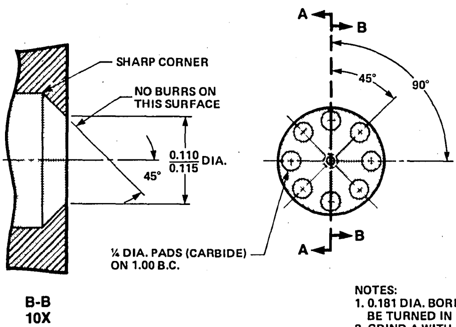


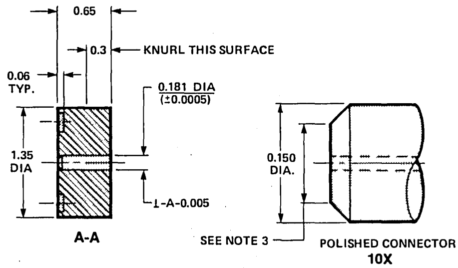
DIMENSIONS IN mm (INCHES)
ALL DIMENSIONS ±0.2 mm UNLESS NOTED.

FIBER OPTIC CABLE CONSTRUCTION



HFBR-4596 HARDENED STEEL POLISHING FIXTURE





NOTES:
1. 0.181 DIA. BORE AND 45° TAPER TO BE TURNED IN SAME OPERATION.
2. GRIND A WITH PADS ⊥ TO 0.181 DIA. BORE, AND HOLD 0.110/0.115 DIA.
3. POLISHED CONNECTOR FACE MUST BE 0.110 MIN., 0.125 MAX.

HEWLETT PACKARD

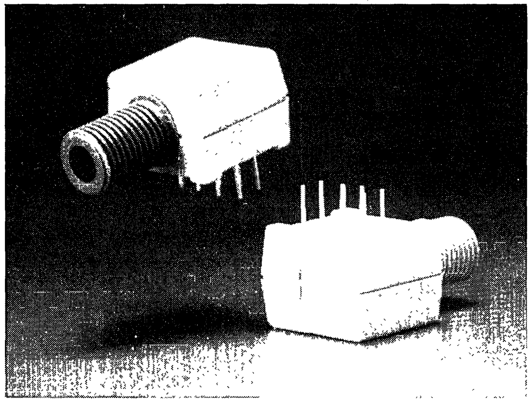
LOW COST MINIATURE FIBER OPTIC COMPONENTS (TRANSMITTERS, RECEIVERS, AND LINK DESIGNS)

HFBR-0400 SERIES

TECHNICAL DATA JANUARY 1986

Features

- LOW COST TRANSMITTERS AND RECEIVERS
- HIGH SPEED TRANSMITTERS:
  Typical Rise/Fall Time of 4.0 ns
- CHOICE OF TWO RECEIVERS:
  5 MBd TTL/CMOS Compatible Output
  25 MHz Analog Output (50 MBd Data Rate)
- GUARANTEE WITH ANY OF THE FOLLOWING FIVE FIBER SIZES: 100/140μm, 85/125μm, 62.5/125μm, 50/125μm, or 200μm PCS
- AUTO-INSERTABLE DUAL-IN-LINE PACKAGE
  No Mounting Hardware Required
  Wavesolderable and Corrosion Resistant
- OPTICAL PORT INTERFACES DIRECTLY WITH STANDARD SMA CONNECTOR
  No Receptacle Required
- COLOR CODED PACKAGE
- WIDE OPERATING TEMPERATURE RANGE:
  -40°C TO +85°C



Applications

- COMPUTER TO PERIPHERAL LINKS
- LOCAL AREA NETWORKS
- PBX LINKS
- COMPUTER MONITOR LINKS
- VIDEO LINKS
- PROCESS AND NUMERICAL CONTROL LINKS
- FACTORY DATA HIGHWAYS
- SUITABLE FOR TEMPEST DATA

Selection Guide

Description

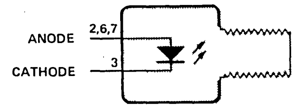
The HFBR-0400 series of components is designed to provide cost effective, high performance fiber optic communication links for computer and industrial applications. Their intended use is primarily on printed circuit boards for inter/intra system links using glass core or Plastic Coated Silica (PCS) fiber with standard SMA style connectors. There are currently four components in the HFBR-0400 family: HFBR-1402 Standard Transmitter, HFBR-1404 High Performance Transmitter, HFBR-2402 5 MBd TTL Receiver, and HFBR-2404 25 MHz Analog Receiver. Distances to 2.5 kilometres at data rates up to 5 MBd are achievable using the HFBR-1402/1404 Transmitter and the HFBR-2402 receiver. For data rates above 5 MBd, the HFBR-2404 Receiver should be used. Although the HFBR-2404 is an analog receiver, it is easily made compatible with digital systems for operations up to 50 MBd using the support circuit described inside the datasheet.

HIGH SPEED LOW COST FIBER OPTIC TRANSMITTER

HFBR-1402
HFBR-1404

The HFBR-1402/1404 Fiber Optic Transmitter contains a planar 820 nm GaAlAs emitter capable of efficiently launching optical power into five different optical fiber sizes: 100/140 μm, 50/125 μm, 62.5/125 μm, 85/125 μm and 200 μm PCS. This allows the designer flexibility in choosing the fiber size. The HFBR-1402/1404 is designed to operate with the Hewlett-Packard HFBR-2402 and HFBR-2404 Fiber Optic Receivers.

The HFBR-1402/1404 transmitter's high coupling efficiency allows the emitter to be driven at low current levels resulting in low power consumption and increased reliability of the transmitter. The HFBR-1402 Standard Transmitter typically can couple −11.5 dBm of optical power into 100/140 μm HFBR-3000 series fiber cable. It is ideal for large size fiber such as 85/125 μm, 100/140 μm, and 200 μm PCS. The HFBR-1404 High Performance Transmitter is optimized for small size fiber and typically can launch −17.5 dBm optical power into 50/125 μm fiber and −12 dBm into 62.5/125 μm fiber. The high power level is also useful for systems where star couplers, taps, or in-line connectors create large fixed losses.



Consistent coupling efficiency is assured by the double-lens optical system (Figure 1). Power coupled into any of the five fiber types varies less than 5 dB from part to part at a given drive current and temperature. The benefit of this is reduced dynamic range requirements on the receiver.

The HFBR-1402/1404 transmitter is housed in a low cost dual-in-line package that is made of high strength, heat resistant, chemical resistant, and UL V-0 flame retardant plastic. The optical port is color coded to distinguish transmitters and receivers.

The package is designed for auto-insertion and wave soldering so it is ideal for high volume production applications.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Notes
Storage Temperature		T_S	−55	+85	°C	
Operating Temperature		T_A	−40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	
	Time			10	sec	
Forward Input Current	Peak	I_{FPK}		70	mA	
	DC	I_{FDC}		70	mA	
Reverse Input Voltage		V_{BR}		1.8	V	

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Unit	Notes
Forward Input Current	Peak	I_{FPK}		60	mA	Note 1
	DC	I_{FDC}		60	mA	

HFBR-1402/1404 TRANSMITTER

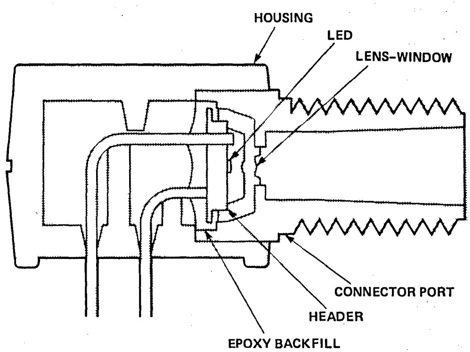
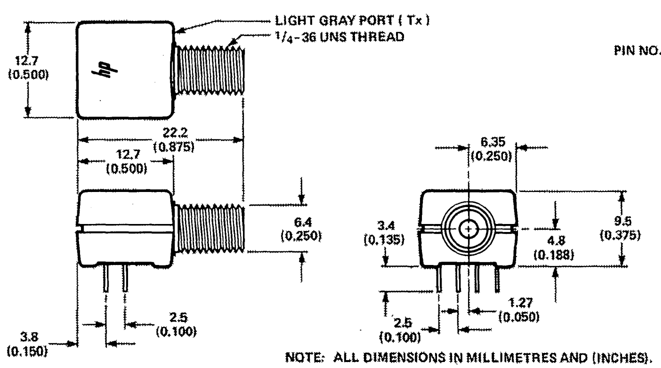
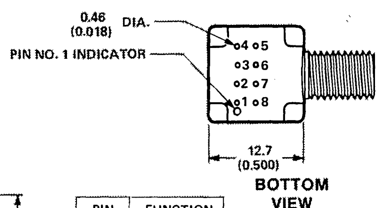


Figure 1.

Mechanical Dimensions





PIN	FUNCTION
1	N.C.
2*	ANODE
3	CATHODE
4	N.C.
5	N.C.
6*	ANODE
7*	ANODE
8	N.C.

* PINS 2, 6 AND 7 ARE BUTT-WELDED TO HEADER

NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

Electrical/Optical Characteristics -40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Notes
Forward Voltage	V_F	1.58	1.80	2.19	V	$I_F = 60$ mA	Fig. 2
Forward Voltage Temperature Coefficient	V_F/T		-0.86		mV/°C	$I_F = 60$ mA	Fig. 2
Reverse Input Voltage	V_{BR}	1.8	3.8		V	$I_R = 100\ \mu A$	
Peak Emission Wavelength	λ_P		820		nm		Fig.5
Diode Capacitance	C_T		145		pF	V = 0, f = 1 MHz	
Optical Power	$\Delta P_T/\Delta T$		-0.016		dB/°C	$I_F = 60$ mA	
Thermal Resistance	Θ_{JA}		240		°C/W		Note 3
Numerical Apecture (HFBR-1402)	NA_{1402}		.49				
Numerical Apecture (HFBR-1404)	NA_{1404}		.31				
Optical Port Diameter (HFBR-1402)	D_{T1402}		290		μm		Note 4
Optical Port Diameter (HFBR-1404)	D_{T1402}		150		μm		Note 4

HFBR-1402 Peak Output Optical Power Measured Out of 1m of Cable

HFBR-3000 Series 100/140μm Fiber Cable	P_{T100}	-15.0	-11.5	-10	dBm	$T_A = 25°C$	I_F=60mA	Notes 5,6
		-16		-9	dBm	$T_A = -40°C$ to $+85°C$		
Siecor 100/140 μm or Equivalent NA = 0.29	P_{T100}	-17	-13.5	-12	dBm	$T_A = 25°C$		Notes 5,6,7
		-18		-11	dBm	-40°C to +85°C		
85/125 μm Cable, NA = 0.26	P_{T85}	-18.5	-15.0	-13.5	dBm	$T_A = 25°C$		Notes 5,6
		-19.5		-12.5	dBm	$T_A = -40°C$ to $+85°C$		
62.5/125 μm Cable, NA = 0.28	P_{T62}	-20.5	-16.5	-15.5	dBm	$T_A = -25°C$		
		-21.5		-14.5	dBm	$T_A = -40°C$ to $+85°C$		
50/125 μm Cable, NA = 0.20	P_{T50}	-25.4	-21.9	-20.4	dBm	$T_A = 25°C$		
		-26.4		-19.4	dBm	$T_A = -40°C$ to $+85°C$		
200 μm PCS, NA = 0.40	P_{T200}	-10	-6.5	-4	dBm	$T_A = 25°C$		
		-11		-3	dBm	$T_A = -40°C$ to $+85°C$		

HFBR-1404 Peak Output Optical Power Measured Out of 1m of Cable

50/125 μm Cable, NA = 0.20	P_{T50}	-20	-17.5	-15	dBm	$T_A = 25°C$	I_F=60mA	Notes 5,6
		-21		-14	dBm	$T_F = -40°C$ to $+85°C$		
62.5/125 μm Cable, NA = 0.28	P_{T62}	-15.1	-12.2	-10.1	dBm	$T_A = 25°C$		
		-16.1		-9.1	dBm	$T_A = -40°C$ to $+85°C$		
85/125 μm Cable, NA = 0.26	P_{T85}	-13.1	-10.6	-8.1	dBm	$T_A = 25°C$		
		-14.1		-7.1	dBm	$T_A = -40°C$ to $+85°C$		
Siecor 100/140 μm or Equivalent NA = 0.29	P_{T100}	-11.6	-9.1	-6.6	dBm	$T_A = 25°C$		Notes 5,6,7
		-12.6		-5.6	dBm	$T_A = -40°C$ to $+85°C$		
HFBR-3000 100/140 μm Cable	P_{T100}	-9.6	-7.1	-4.6	dBm	$T_A = 25°C$		Notes 5,6
		-10.6		-3.6	dBm	$T_A = -40°C$ to $+85°C$		
200 μm PCS, NA = 0.40	P_{T200}	-4.6	-3.1	1.4	dBm	$T_A = 25°C$		
		-5.6		2.4	dBm	$T_A = -40°C$ to $+85°C$		

WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe: however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Notes
Rise Time, Fall Time (10 to 90%)	t_r, t_f		4.0	6.5	nsec	$I_F = 60$ mA No pre-bias	Note 1 Fig. 6
Propagation Delay LOW to HIGH	t_{PLH}		10		nsec	$I_{FPK} = 60$ mA	
Propagation Delay HIGH to LOW	t_{PHL}		8		nsec	$I_{FPK} = 60$ mA	

Notes:
1. Pre-bias is recommended if $I_F < 30$ mA, see recommended drive circuit in Figure 4.
2. Typical data at $T_A = 25°C$.
3. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board.
4. D_T is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of the maximum.
5. Measured with a large area detector at the end of 1 metre cable, with an OFTI series NOFC precision ceramic ferrule. This approximates a standard test connector.
6. When changing μW to dBm, the optical power is referenced to 1 mW (1000 μW). Optical Power P (dBm) = 10 log P (μW)/1000 μW.
7. The fiber N/A is 0.29 measured at the end of a 2.0 metre length, the N/A being defined as the sine of the half angle determined by the 6.5% of peak intensity point.

FIBER OPTICS

Recommended Drive Circuit

Rise and fall times can be improved by using a pre-bias current and "speed-up" capacitor. A pre-bias current will significantly reduce the junction capacitance and will not change the extinction ratio appreciably. The recommended TTL compatible drive circuit in Figure 4 using a speed-up capacitor will provide typical rise and fall times of 4 ns. The following set of equations will give the component values for the circuit for different transmitter drive current:

$$R_y = \frac{(V_{CC} - V_F) + 3.2\,(V_{CC} - V_F - 1.4V)}{I_{FON}}$$

$$R_x = \left(\frac{R_y}{3.2} - 10\,\Omega\right)$$

$$R_{x_1} = \frac{R_x + 10\Omega}{2}$$

$$R_{x_2} = R_{x_1} - 10\Omega$$

$$C = \frac{2.0\text{ nsec}}{R_{x_1}}$$

Example: For $I_{FON} = 27$ mA, V_F can be obtained from Figure 2 (= 1.7 V).

$$R_y = \frac{(5V - 1.7V) + 3.2\,(5\text{ V} - 1.7\text{ V} - 1.4\text{ V})}{27\text{ mA}}$$

$$= \frac{3.3\text{ V} + 6.1\text{ V}}{27\text{ mA}} = 348\,\Omega$$

$$R_x = \left(\frac{348\,\Omega}{3.2}\right) - 10\,\Omega = 98.8\,\Omega$$

$$R_{x_1} = \frac{98.8\,\Omega + 10\,\Omega}{2} = 54.4\,\Omega$$

$$R_{x_2} = 54.4 - 10 = 44.4\,\Omega$$

$$C = \frac{2\text{ nsec}}{R_{x_1}} = 36.8\text{ pF}$$

Selected the following standard value components:

$R_y = 330\,\Omega$ $R_{x_1} = 56\,\Omega$ $R_{x_2} = 47\,\Omega$ $C = 39$ pF

Handling and Design Information

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.

Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon on a cotton swab also works well.

Three pins have been welded to the anode header connection to minimize the thermal resistance from junction to ambient. To further reduce the thermal resistance, the anode trace should be made as large as is consistent with good RF circuit design.

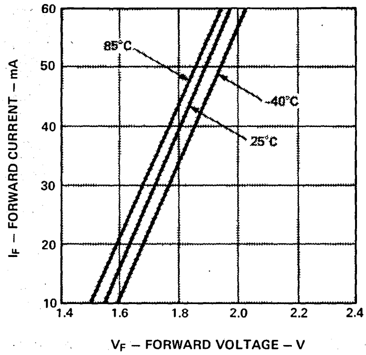


Figure 2. Forward Voltage and Current Characteristics

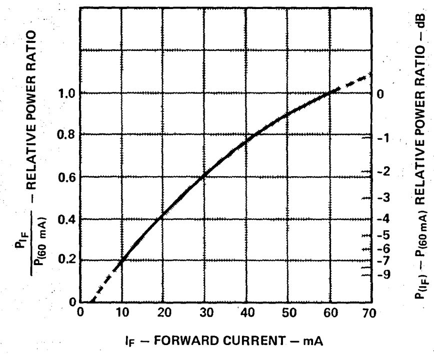


Figure 3. Normalized Transmitter Output vs. Forward Current

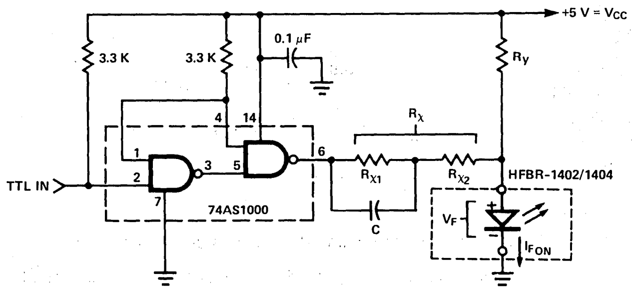


Figure 4. Recommended Drive Circuit

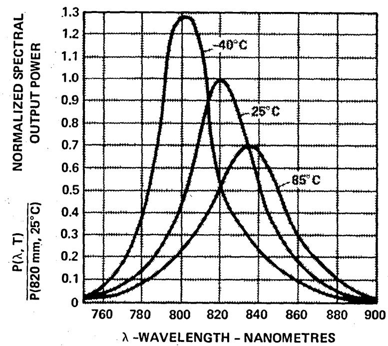


Figure 5. Transmitter Spectrum Normalized to the Peak at 25°C

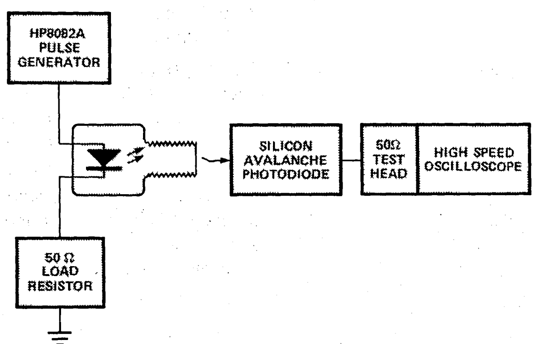
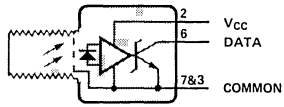


Figure 6. Test Circuit for Measuring t_r, t_f

5 MBd LOW COST FIBER OPTIC RECEIVER

HFBR-2402



The HFBR-2402 Fiber Optic Receiver incorporates a monolithic photo-IC which contains a photodetector and a dc amplifier. An open collector Schottky transistor on the IC provides compatibility with TTL and CMOS logic. This receiver is designed to operate with the Hewlett-Packard HFBR-1402/1404 Fiber Optic Transmitter and 100/140 μm, 50/125 μm, 62.5/125 μm, 85/125 μm and 200 μm PCS fiber optic cable terminated with SMA connectors.

Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size.

The HFBR-2402 receiver is housed in a low cost dual-in-line package that is made of high strength, heat resistant, chemically resistant, and UL V-0 flame retardant plastic. The optical port is color coded to distinguish transmitters and receivers. EMI immunity is equivalent to the HFBR-2202 metal packaged receiver.

The package is designed for auto-insertion and wave soldering so it is ideal for high volume production applications.

FIBER OPTICS

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	
Lead Soldering Cycle	Temp			+260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7.0	V	
Output Current		I_O		25	mA	
Output Voltage		V_O	-0.5	18.0	V	
Output Collector Power Dissipation		$P_{O\ AV}$		40	mW	

HFBR-2402 RECEIVER

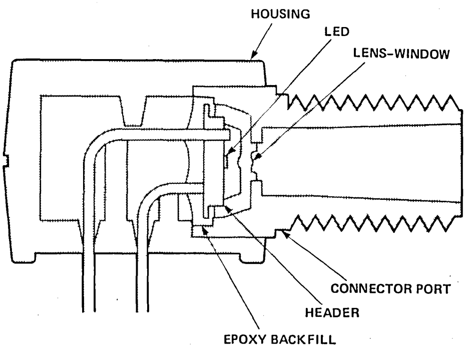
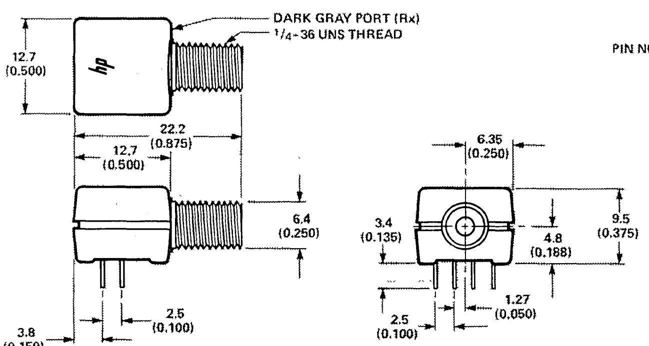
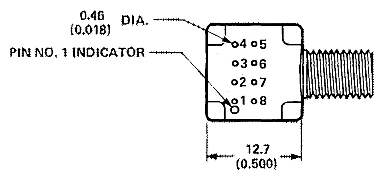


Figure 1.

Mechanical Dimensions





BOTTOM VIEW

PIN	FUNCTION
1	N.C.
2	V_{CC} (5 V)
3*	COMMON
4	N.C.
5	N.C.
6	DATA
7*	COMMON
8	N.C.

* PINS 3 AND 7 BUTT-WELDED TO HEADER

NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

Electrical/Optical Characteristics -40° C to +85° C unless otherwise specified

Fiber sizes with core diameter ≤ 200 μm and NA ≤ 0.4, 4.75 ≤ V_{CC} ≤ 5.25 V

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
High Level Output Current	I_{OH}		5	250	μA	V_O = 18V P_R < -40 dBm	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_O = 8 mA P_R > -24 dBm	
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V P_R < -40 dBm	
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R > -24 dBm	
Equivalent N.A.	NA		.50				
Optical Port Diameter	D_R		400		μm		Note 3

Dynamic Characteristics -40° C to +85° C unless otherwise specified; 4.75 ≤ V_{CC} ≤ 5.25 V

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Notes
Peak Input Power Level Logic HIGH	P_{RH}			-40	dBm	λ_P = 820 nm	Note 4
				0.1	μW		
Peak Input Power Level Logic LOW	P_{RL}	-25.4		-11.2	dBm	T_A = +25° C, V_{OL} = 0.5 V I_{OL} = 8 mA	Note 4
		2.9		76	μW		
		-24.0		-12.0	dBm	-40 < T_A < 85° C, V_{OL} = 0.5 V I_{OL} = 8 mA	
		4.0		63	μW		
Propagation Delay LOW to HIGH	t_{PLHR}		65		nsec	T_A = 25° C, P_R = -21 dBm Data Rate = 5 MBd BER = 10^{-9}	Note 5
Propagation Delay HIGH to LOW	t_{PHLR}		49		nsec		

Notes:

1. 2.0 mm from where leads enter case.
2. Typical data at T_A = 25°C, V_{CC} = 5.0V dc.
3. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
4. Measured at the end of HFBR-3000 Fiber Optic Cable with large area detector.
5. Propagation delay through the system is the result of several sequentially-occurring phemonena. Consequently it is a combination of data-rate-limiting effects and of transmission-time effects. Because of this, the data-rate limit of the system must be described in terms of time differentials between delays imposed on falling and rising edges.
   As the cable length is increased, the propagation delays increase at 5 ns per metre of length. Data rate, as limited by pulse width distortion, is not affected by increasing cable length if the optical power level at the Receiver is maintained.

Electrical Description

The HFBR-2402 Receiver incorporates an integrated photo IC containing a photodetector and dc amplifier driving an open-collector Schottky output transistor. The HFBR-2402 is designed for direct interfacing to popular logic families. The absence of an internal pull-up resistor allows the open-collector output to be used with logic families such as CMOS requiring voltage excursions much higher than V_{CC}. Both the open-collector "Data" output (Pin 6) and V_{CC} (Pin 2) are referenced to "Com" (Pin 3, 7). The "Data" output allows busing, strobing and wired "OR" circuit configurations. The transmitter is designed to operate from a single +5V supply. It is essential that a bypass capacitor (0.01μF to 0.1 μF ceramic) be connected from Pin 2 (V_{CC}) to Pin 3 (circuit common) of the receiver.

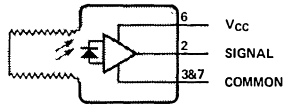
Handling and Design Information

When soldering, it is advisable to leave the protective cap of the unit to keep the optics clean.

Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon on a cotton swab also works well.

25 MHz LOW COST FIBER OPTIC RECEIVER

HFBR-2404



The HFBR-2404 Fiber Optic Receiver contains a discrete PIN photodiode and a preamplifier IC. It is designed to operate with the Hewlett-Packard HFBR-1402/1404 Fiber Optic Transmitters and 100/140 μm, 50/125 μm, 62.5/125 μm, 85/125 μm and 200 μm PCS fiber optic cable terminated with SMA connectors. Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size.

The receiver output is an analog signal that can be optimized for a variety of distance/data rate requirements. Low-cost external components can be used to convert the analog output to logic compatible signal levels for various data formats and data rates up to 50 MBaud. This distance/data rate tradeoff results in increased optical power budget at lower data rates which can be used for additional distance or splices.

The HFBR-2404 receiver is housed in a low cost dual-in-line package that is made of high strength, heat resistant, chemically resistant, and UL V-0 flame retardant plastic. The optical port is color coded to distinguish transmitters and receivers. EMI immunity is equivalent to the HFBR-2204 metal packaged receiver.

The package is designed for auto-insertion and wave soldering so it is ideal for high volume production applications.

HFBR-2404 RECEIVER

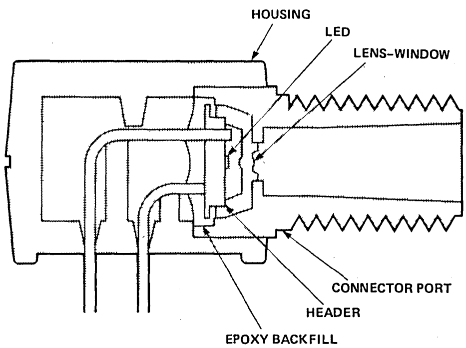


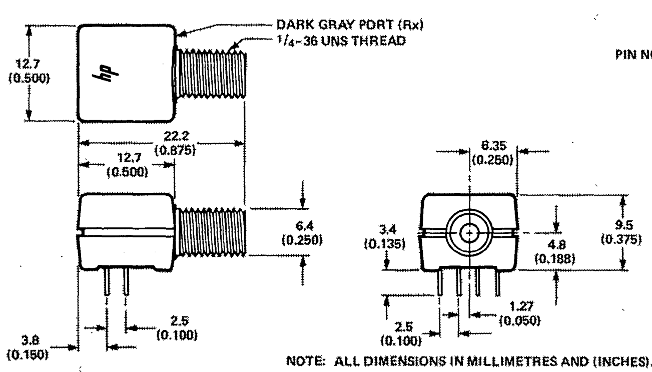
Figure 1.

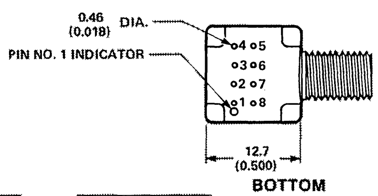
HFBR-2404 RECEIVER

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Signal Pin Voltage		V_{SIGNAL}	-0.5	1	V	
Supply Voltage		V_{CC}	-0.5	7.0	V	

Mechanical Dimensions





BOTTOM VIEW

PIN	FUNCTION
1	N.C.
2	V_{CC} (5 V)
3*	COMMON
4	N.C.
5	N.C.
6	DATA
7*	COMMON
8	N.C.

* PINS 3 AND 7 BUTT-WELDED TO HEADER

NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

Electrical/Optical Characteristics -40° C to +85° C; $4.75 \le V_{CC} \le 5.25$; $R_{LOAD} = 511\Omega$

Fiber sizes with core dia. ≤ 200 microns, and N.A. ≤ 0.4 unless otherwise specified.

Parameter	Symbol	Min.	Typ[5]	Max.	Unit	Conditions	Reference
Responsivitity	R_P	5.1	7	10.9	mV/μW	$T_A = 25°C$ at 820 nm	
		4.6		12.3	mV/μW	$-40 \le T_A \le +85°C$	
RMS Output Noise Voltage	V_{NO}		.30	.36	mV	$T_A = 25°C$, $P_R = 0\mu W$	
				.43	mV	$-40 \le T_A \le 85°C$, $P_R = 0\mu W$	
Input Power	P_R			-12.6	dBm	$T_A = 25°C$	Note 2
				55	μW		
				-14	dBm	$-40 \le T_A \le 85°C$	
				40	μW		
Output Impedance	Z_O		20		Ω	Test Frequency = 20 MHz	
DC Output Voltage	V_{odc}		.7		V	$P_R = 0\mu W$	Note 3
Power Supply Current	I_{CC}		3.4	6.0	mA	$R_{LOAD} = \infty$	
Equivalent N.A.	NA		.35				
Equivalent Diameter	D_R		250		μm		Note 4
Equivalent Optical Noise Input Power	P_N		-43.7	-40.3	dBm		
			.042	.094	μW		

Dynamic Characteristics

-40° C to +85° C; $4.75 \le V_{CC} \le 5.25$; $R_{LOAD} = 511\Omega$, $C_{LOAD} = 13$ pF unless otherwise specified

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Reference
Rise/Fall Time, 10% to 90%	t_r, t_f		14	19.5	ns	$T_A = 25°C$ $P_R = 10\ \mu W$ Peak	Note 6
				26	ns	$-40 \le T_A \le 85°C$	
Pulse Width Distortion	$t_{phl} - t_{plh}$			2	ns	$P_R = 40\ \mu W$ Peak	
Overshoot			4		%	$T_A = 25°C$	Note 7
Bandwidth			25		MHz		
Power Supply Rejection Ratio (Referred to Output)	PSRR		50		dB	at 2 MHz	Note 8

Notes:

1. 2.0 mm from where leads enter case.
2. If $P_R > 40\mu W$, then pulse width distortion may increase. At Pin = 80μW and $T_A = 85°C$, some units have exhibited as much as 100 ns pulse width distortion.
3. $V_{OUT} = V_{ODC} - (R_P \times P_R)$.
4. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
5. Typical specifications are for operation at $T_A = 25°C$ and $V_{CC} = 5.0V$.
6. Input optical signal is assumed to have 10% - 90% rise and fall times of less than 6 ns.
7. Percent overshoot is defined as: $\frac{V_{PK} - V_{100\%}}{V_{100\%}} \times 100\%$
8. Output referred P.S.R.R. is defined as 20 log $\left(\frac{V_{POWER\ SUPPLY\ RIPPLE}}{V_{OUT\ RIPPLE}}\right)$

Electrical Description

The HFBR-2404 Fiber Optic Receiver contains a PIN photodiode and low noise transimpedance pre-amplifier hybrid circuit with an inverting output (see note 3). The HFBR-2404 receives an optical signal and converts it to an analog voltage. The output is a buffered emitter-follower. Because the signal amplitude from the HFBR-2404 Receiver is much larger than from a simple PIN photodiode, it is less susceptible to EMI, especially at high signal rates.

The frequency response is typically dc to 25 MHz. Although the HFBR-2404 is an analog receiver, it is easily made compatible with digital systems (see 50 MBaud Logic Link Design for more information).

It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from Pin 6 (V_{CC}) to Pin 3, 7 (circuit common) of the receiver. Total lead length between both ends of the capacitor and the pins should be less than 20 mm.

Handling and Design Information

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.

Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressd air often is sufficient to remove particles of dirt; methanol or Freon on a cotton swab also works well.

5 MBaud Logic Link Design

The HFBR-1402/1404 Transmitter and the HFBR-2402 Receiver can be used to design fiber optic data link for distances to 2.5 Kilometers at rates up to 5 MBaud. The components are compatible with standard SMA style connector and can operate with 100/140 μm fiber cable (such as HFBR-3000/3100 series), or other fiber sizes such as 50/125 μm, 62.5/125 μm, or 200 μm PCS. The HFBR-1402/1404 Transmitter contains a high speed GaAlAs emitter operating at a wavelength of 820 nm. It is easily identified by the light grey color optical port. The HFBR-2402 Receiver incorporates a photo IC containing a photodetector and dc amplifier. An open collector Schottky transistor on the IC provides TTL/CMOS compatible output. The receiver is also easily identified by the dark grey color optical port.

System Design Considerations

The HFBR-1402/2402 Logic Link is guaranteed to work with HFBR-3000 100/140μm fiber optic cable over the entire range of 0 to 625 metres at a data rate of dc to 5MBd, with arbitrary data format and typically less than 25% pulse width distortion, if the Transmitter is driven with $I_F = 30$ mA, $R_1 = 89\Omega$. If it is desired to economize on power or achieve lower pulse distortion, then a lower drive current (I_F) may be used. The following example will illustrate the technique for optimizing I_F.

EXAMPLE: Maximum distance required = 400 metres. From Figure 2 the worst case drive current = 20 mA. From the Transmitter data $V_F = 2.33$V (max.).

$$R_1 = \frac{V_{CC} - V_F}{I_F} = \frac{5 - 2.33\text{V}}{20\text{ mA}} = 134\Omega$$

The optical power margin between the typical and worst case curves (Figure 2) at 400 metres is 6.6 dB. To calculate the worst case pulse width distortion at 400 metres, see Figure 5. The power into the Receiver is P_{RL} + 6.6 dB = −17.4 dBm. Therefore, the typical distortion is 40 ns or 20% at 5 MBd.

CABLE SELECTION

The link performance specifications on the above example are based on using the HFBR-3000/HFBR-3100 cable/ connector assemblies. These cables contain glass-clad silica fibers with a 100 μm core diameter and 140 μm cladding diameter. This fiber type is now a user accepted standard for local data communications links (RS-458, Class I, Type B). The HFBR-1402/4 Transmitter and HFBR-2402 Receiver can be used with HP's 100/140 μm fiber, or other fiber sizes such as 50/125 μm, 62.5/125 μm, 85/125 μm, or 200 μm PCS. Before selecting an alternate fiber type, several parameters need to be carefully evaluated.

The attenuation (dB/km) of the selected fiber, in conjunction with the amount of optical power coupled into it will determine the achievable link length. The parameters that will significantly affect the optical power coupled into the fiber are as follows:

a. **Fiber Core Diameter.** As the core diameter is increased, the optical power coupled increases, leveling off at about 250 μm diameter.
b. **Numerical Aperture (NA).** as the NA is increased, the optical power coupled increases, leveling off at an NA of about 0.34.
c. **Index Profile (α).** The index profile parameter of fibers varies from 2 (fully graded index) to infinite (step index). Some gains in coupled optical power can be achieved at the expense of bandwidth, when α is increased.

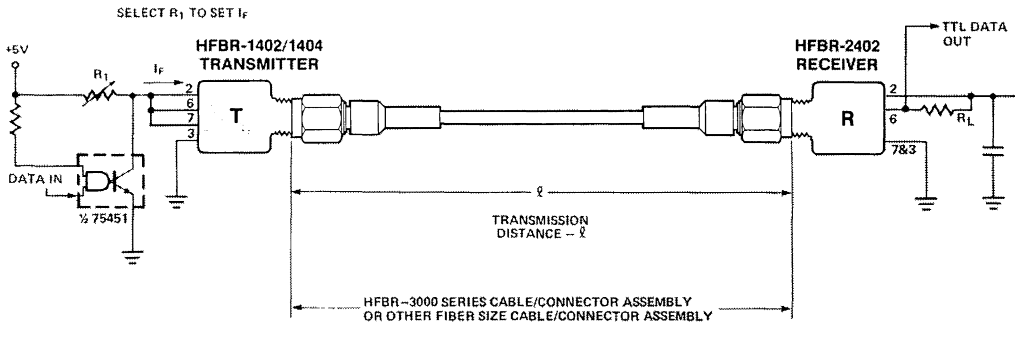
In addition to the optical parameters, the environmental performance of the selected fiber/cable must be evaluated. Finally, the ease of installing connectors on the selected fiber/cable must be considered.

SMA STYLE CONNECTORS

The HFBR-1402/4 Transmitter with HFBR-2402 Receiver are compatible with either the Type A or Type B SMA style fiber optic connector (see Figure 7). The basic difference between the two connectors is the plastic half-sleeve on the stepped ferrule tip of the Type B connector. This step provides the capability to use a full length plastic sleeve to ensure good alignment of two connectors for an inline splice. The HFBR-300/HFBR-3100, OPT 002 series connectored cable utilizes the Type A connector system.

Typical Circuit Configuration

NOTE:
IT IS ESSENTIAL THAT A BYPASS CAPACITOR (0.01 μF TO 0.1 μF CERAMIC) BE CONNECTED FROM PIN 2 TO PIN 7 OF THE RECIEVER. TOTAL LEAD LENGTH BETWEEN BOTH ENDS OF THE CAPACITOR AND THE PINS SHOULD NOT EXCEED 20 mm.



Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Reference
TRANSMITTER					
Ambient Temperature	T_A	-40	+85	°C	
Peak Forward Input Current	$I_{F,PK}$		60	mA	
DC Forward Input Current	I_{FDC}		60	mA	
RECEIVER					
Ambient Temperature	T_A	-40	+85	°C	
Supply Voltage	V_{CC}		5.25	V	
Fan Out (TTL)	N		5		Note 1, Fig.1
CABLE (see HFBR-3000/HFBR-3100 data sheet)					

System Performance –40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Optical Power Budget w/50/125μm Fiber	OPB_{50}	3	8.5		dB	HFBR - 1404 Transmitter w/50/125μm, NA = 0.20	
Optical Power Budget w/62.5/125μm Fiber	$OPB_{62.5}$	8	13.8		dB	HFBR - 1404 Transmitter w/62.5/125μm, NA = 0.28	
Optical Power Budget w/85/125μm Fiber	OPB_{85}	4.5	11		dB	HFBR - 1402 Transmitter w/85/125μm, NA = 0.26	
Optical Power Budget w/100/140μm Fiber	OPB_{100}	8	14.5		dB	HFBR - 1402 Transmitter w/HFBR-3000 Cable	
Optical Power Budget w/200μm PCS	OPB_{200}	13	19		dB	HFBR - 1402 Transmitter w/200μm PCS, NA = 0.40	
Data Rate Synchronous		dc		5	MBaud		Note 3
Asynchronous		dc		2.5	MBaud		Note 3, Fig. 5
Propagation Delay LOW to HIGH	t_{PLH}		72		nsec	$T_A = 25°C$, $P_R = -21$ dBm	Fig. 4,5,6
Propagation Delay HIGH to LOW	t_{PHL}		46		nsec		
System Pulse Width Distortion	$t_{PLH} - t_{PHL}$		25		nsec	$\ell = 1.5$ metre	
Bit Error Rate	BER			10^{-9}		Data Rate ≤ 5 MBaud $P_R > -24$ dBm (4μW)	

Notes:

1. 8 mA load (5 x 1.6 mA), $R_L = 560\Omega$.
2. Typical data at T = 25°C, V_{CC} = 5.0V dc.
3. Synchronous data rate limit is based on these assumptions: (a) 50% duty factor modulation. e.q. Manchester I or BiPhase (Manchester II); (b) continous data; (c) PLL (Phase Lock Loop) demodulation; (d) TTL threshold.

   Asynchronous data rate limit is based on these assumptions: (a) NRZ data; (b) arbitrary timing — no duty factor restriction; c) TTL threshold.

   The EYE pattern describes the timing range within which there is no uncertainty of the logic state, relative to a specific threshold, due to either noise or intersymbol (prop. delay) effects.

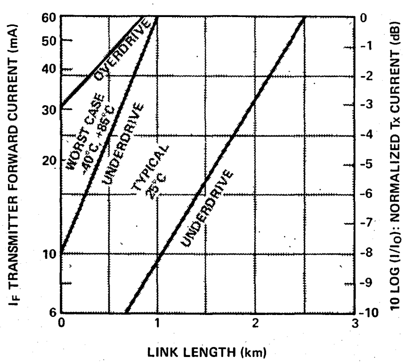


Figure 2. HFBR-1402/HFBR-2402 Link Design Limits with 100/140 μm Cable (HFBR-3000 Series)

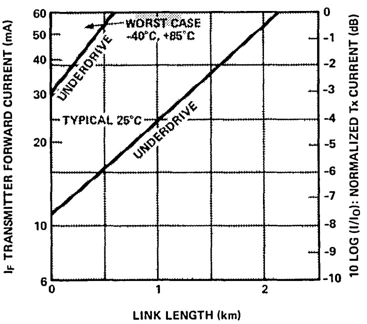


Figure 3. HFBR-1404/HFBR-2402 Link Design Limits with 50/125 μm Cable

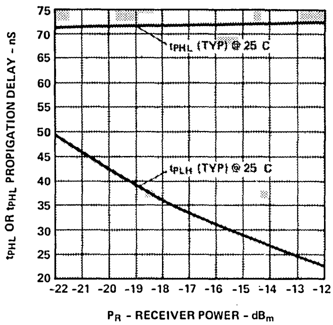


Figure 4. Propagation Delay through System with One Metre of Cable

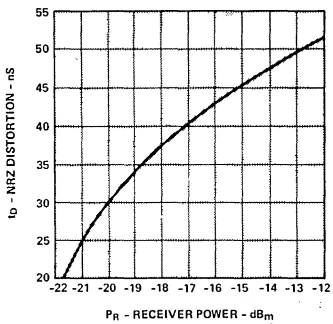


Figure 5. Worst-Case Distortion of NRZ EYE-pattern with Pseudo Random Data at 5 Mb/s. (see note 10).

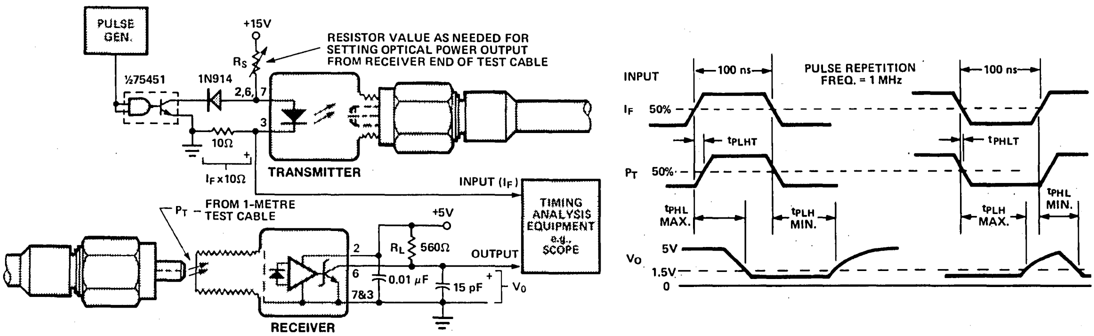


Figure 6. System Propagation Delay Test Circuit and Wave form Timing Definitions

SMA STYLE CONNECTORS

TYPE A
(Used in HFBR-3000/3100, Option 002 Cable Assemblies).

TYPE B
(Not Available from Hewlett-Packard)

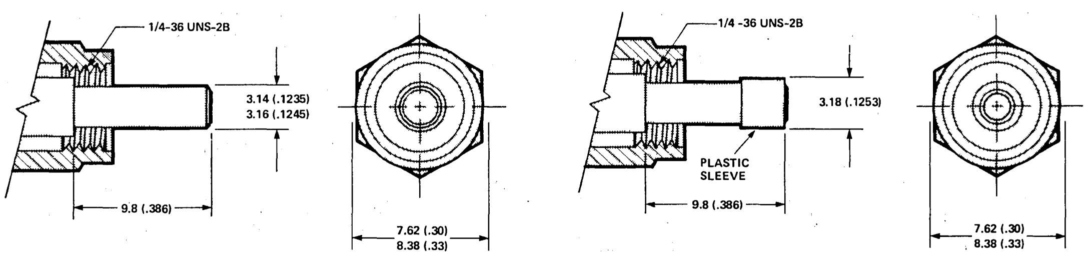


Figure 7.

30/50 MBaud Logic Link Design

The HFBR-1402/1404 Transmitter and the HFBR-2404 Receiver can be used to design fiber optic data link for distances to 2 kilometers at rates up to 50 MBaud. The components are compatible with standard SMA style connector and can operate with 100/140 μm fiber cable (such as HP's HFBR-3000/3100 series), or other fiber sizes such as 50/125 μm, 62.5/125 μm, 85/125 μm, or 200 μm PCS.

The HFBR-1402/1404 Transmitter contains a high speed GaAlAs emitter operating at a wavelength of 820 nm. It is easily identified by the light grey color optical port. The HFBR-2404 Receiver contains a discrete PIN photodiode and a preamplifier IC. It is also easily identified by the dark grey color optical port.

Logic compatible signal levels are achieved by addition of low-cost external components. For speed below 30 MBaud, a simple circuit as shown in Figure 1 can be used (for detail of that design, please see the product data sheet for the HFBR-0221/2/3/4 Fiber Optic Transceivers).

For speed beyond 30 MBaud, recommended driver and amplifier circuits are presented in Figure 2. Details of the design are described in the 50 MBaud Transciever Board section. These circuits provide TTL input and complementary TTL ouputs and are available as printed circuit board assembly (the HFBR-0422 Transceiver Board) for evaluation purpose. Figure 4 gives the performance of the HFBR-0422 at 50MBd characterized over 0°C to 70°C.

System Design Considerations

OPTICAL POWER BUDGETING

The HFBR-2404 Fiber Optic Receivers when used with the HFBR-1402/1404 Fiber Optic Transmitters can be operated at a signalling rate of more than 50 MBd over a distance greater than 2000 metres (assuming 6 dB/km cable attenuation). For shorter transmission distances, power consumption can be reduced by decreasing Transmitter drive current. At a lower data rate, the transmission distance may be increased by applying bandwidth-filtering at the output of the HFBR-2404 Receiver; since noise is reduced as the square root of the bandwidth, the sensitivity of the circuit is proportionately improved provided these two conditions are met:

a. input-referred noise of the follow-on circuit is well below the filtered noise of the Receiver
b. logic comparator threshold is reduced in the same proportion as the noise reduction

As an example, consider a link with a maximum data rate of 10 MBd (e.g., 5 Mb/s Manchester); this requires a 3 dB bandwidth of only 5 MHz. For this example (See Figure 1) the input-referred rms noise voltage of the follow-on circuit is 0.03 mV. The equivalent optical noise power of the complete receiver (P_{NO}) is given by:

$$P_{NO} = [(V_{NO})^2 (B/Bo) + (V_{NI})^2]^{0.5} / R_P$$

V_{NO} = rms output noise voltage of the HFBR-2404 with no bandwidth filtering
V_{NI} = input-referred rms noise voltage of the follow-circuit
B = filtered 3 dB bandwidth
V = filtered 3 dB bandwidth
B_O = unfiltered 3dB bandwidth of the HFBR-2404 (25 MHz)
R_P = optical-to-electrical responsivity (mV/μW) of the HFBR-2404.

Note that noise adds in an rms fashion, and that the square of the rms noise voltage of the HFBR-2404 is reduced by the bandwidth ratio, B/Bo.

From the receiver data (Electrical/Optical Characteristics) taking worst-case values, and applying NO bandwidth filtering (B/Bo = 1):

$$P_{NO} = \frac{[(0.43)^2+(0.03)^2]^{0.5}\ \text{mV}}{4.6\ \text{mV}/\mu\text{W}} = 0.094\,\mu\text{W or } -40.3\ \text{dBm}$$

To ensure a bit error rate less than 10^{-9} requires the signal power to be 12 times larger (+11 dB) than the rms noise as referred to the Receiver input. The minimum Receiver input power is then:

$$P_{RMIN} = P_{NO} + 11\ \text{dB} = -29.3\ \text{dBm}$$

With the application of a 5 MHz low-pass filter, the band width ratio becomes:

$$B/B_O = 5\text{MHz}/25\text{MHz} = 0.2$$

Note that 25 MHz should be used for the total noise bandwidth of the HFBR-2404. Inserting this value of the bandwidth ratio in the expressions for P_{NO} and P_{RMIN} above yields the results:

$$P_{NO} = 0.042\ \mu\text{W or -43.8 dBm and } P_{RMIN} = -32.8\ \text{dBm}$$

Given the HFBR-1402 Transmitter optical power $P_T = -16$ dBm at $I_F = 60$ mA, and allowing a 3 dB margin, a minimum optical power budget of 13.8 dB is obtained:

$$[-16\ \text{dBm} -3\text{dB} -(-32.8\ \text{dBm})] = 13.8\ \text{dB}$$

Using 8 dB/km optical fiber, this translates into a minimum link length of 1725 metres (typical link power budget for this configuration is approximately 17.2 dB or 3130 metres with 5.5 dB/km fiber).

BANDWIDTH

The bandwidth of the HFBR-2404 is typically 25 MHz. Over the entire temperature range of −40°C to +85°C, the rise and fall times vary in an approximately linear fashion with temperature. Under worst case conditions, t_r and t_f may reach a maximum of 26 ns, which translates to a 3 dB bandwidth of:

$$f_{3dB} \simeq \frac{350}{t_r} = \frac{350}{26\ \text{ns}} = 13.5\ \text{MHz}$$

The receiver response is essentially that of a single-pole system, rolling off at 6 dB/octave. In order for the receiver to operate up to 50 MBd even though its worst case 3 dB bandwidth is 13.5 MHz, the received optical power must be increased by 3 dB to compensate for the restricted receiver transmission bandwidth.

PRINTED CIRCUIT BOARD LAYOUT

When operating at data rates above 10 MBd, standard PC board precautions should be taken. Lead lengths greater than 20 mm should be avoided whenever possible and a ground plane should be used. Although transmission line techniques are not required, wire wrap and plug boards are not recommended.

30 MBaud Transceiver Circuit

Figure 1 shows the circuit diagram for a 30 MBaud link designed for 50% duty cycle operation. The transmitter circuit uses 1/2 75451 positive AND driver operating operating in conjunction with an HFBR-1402 fiber optic transmitter. The transmitter drive current is determined by R2 and R3. CR1, R3 and C3 are used to speed up the edges of the optical waveform.

Th receiver circuit uses the HFBR-2404 fiber optic receiver, followed by an LM-733 video amplifier and an LM-360 high-speed comparator. The resistors R8, R9, R10, R11 provide 200mV of hysteresis. The gain of the post amplifier LM-733 is adjusted by resistor R7 to provide a minimum of 400mV output, which corresponds to the minimum receiver optical power input.

For additional application information, see the product data sheet for the HFBR-0221/2/3/4 Fiber Optic Transceivers product.

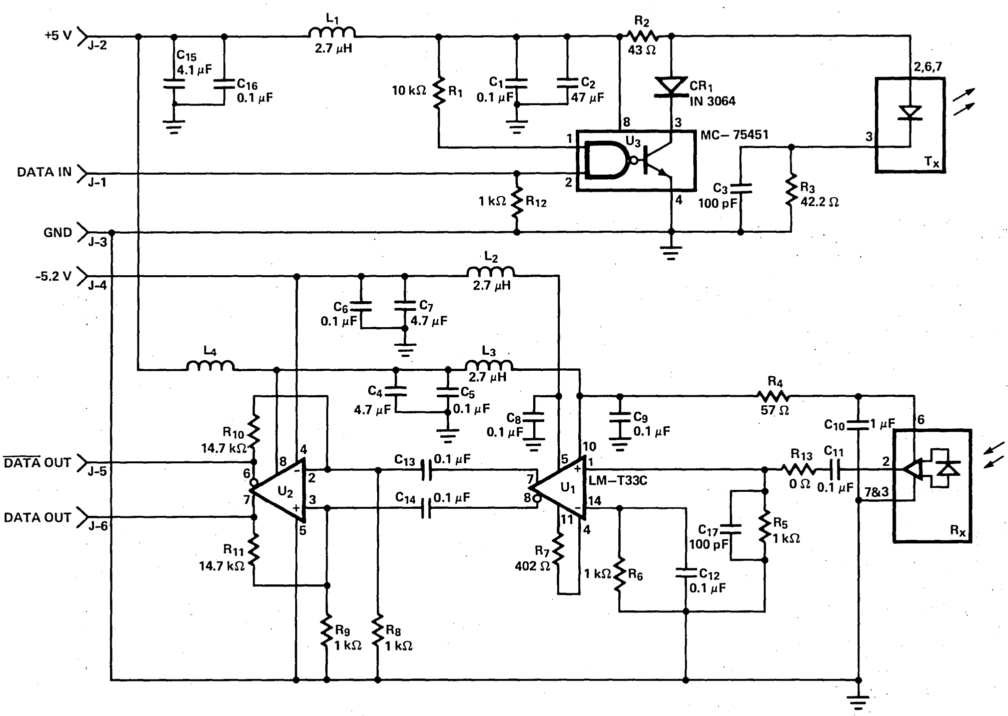
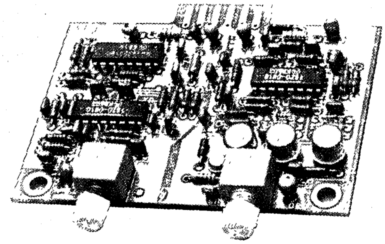


Figure 1. 30 MBaud Transceiver Circuit

FIBER OPTICS

50 MBd Transceiver Evaluation Board

HFBR-0422



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Applied Voltage Data, $\overline{Data}$ +V_{CC}, Data In		−0.5	5.25	V
Storage Temperature[1]	Ts	−55	85	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	+V_{CC}	4.75	5.25	V
Operating[6] Temperature	T_A	0	70	°C
Duty Factor	DF	33	67	%
Data Rate Range		0.05	50	MBd

Electrical/Optical Characteristics 0°C to 70°C unless otherwise specified

(Recommended operating conditions for transceiver for 50 MBd apply, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Optical Power Budget	OPB	When used with HFBR-3000 Fiber Cable/Connectors, Data Rate = 50 MBd BER = 10^{-9}	12.0	18		dB
Pulse Distortion	$t_{PLH} - t_{PHL}$			7	12.5	ns
Data Output Response Time[2]	t_r			3		ns
	t_f			2		
Transceiver Propagation Delay[3]	t_{PLH}, t_{PHL}			40		ns
Supply Current	I_{CC}			210		mA
Transmitter Output Optical Power[4] into HFBR-3000 Fiber Cable/ Connector Assembly	$P_{T_{AV}}$	50% Data	−18.8	−16		dBm
Receiver Optical Input Power	$P_{R_{AV}}$	50% Data Data Rate = 50 MBd	−30.8	−34	−14	dBm
TTL Gate Fanout					4	

WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe: however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Notes:

1. Operating temperature of HFBR-3000 Fiber Cable/Connector is −20°C to +70°C.
2. Data Output Response Time is the 10% to 90% electrical rise and fall time on PIN 6 (DATA) and PIN 5 ($\overline{DATA}$).
3. Transceiver propagation delay is measured by looping the transmitter back on the receiver with one metre of fiber cable. Transceiver propagation delay is the time interval between a signal applied to the DATA IN pad and the signal received at the DATA OUT pad.
4. Measured at the end of one metre of HFBR-3000 Fiber Optic Connector/Cable Assembly with a large area detector and cladding modes stripped (NA = 0.28) This represents a standard test fiber.
5. Typical specifications are at 25°C and V_{CC} = 5 V.
6. Operating temperature limited by support circuit.

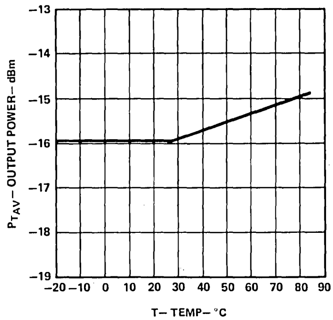


Figure 4. HFBR-0422 Transceiver Power vs. Temperature at 50MB

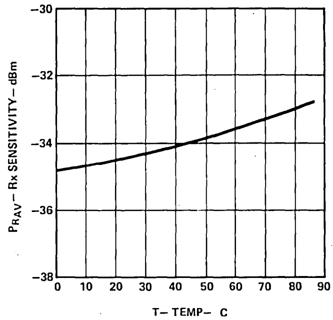


Figure 5. HFBR-0422 Receiver Sensitivity

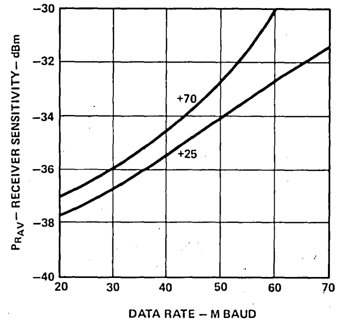


Figure 6. HFBR-0422 Receiver Sensitivity vs. Bit Rate at 10-9) BER)

Test Set-Up

Equipment Needed

1. Dual power supply (HP 623613)
2. 100 MHz oscilloscope (HP 1725A)
3. Active oscilloscope probe and probe tip (HP 1120A/1122A)
4. 10:1 divider for oscilloscope probe (HP 10241A)
5. 50 MHz pulse generator (HP 8082A)
6. Miscellaneous cables and connectors

Procedure

1. Connect fiber cable and edge card connector to the transceiver board.
2. Adjust the power supply to +5V. Then connect to the transceiver board as shown below. Take care not to exceed the recommended operating voltage.
3. Adjust the pulse generator for TTL level square wave (+3 V) with 5 nsec, edge transition time and then connect to the transceiver board.
4. Use the oscilloscope with the active probe and 10:1 divider to observe the input and output waveforms.

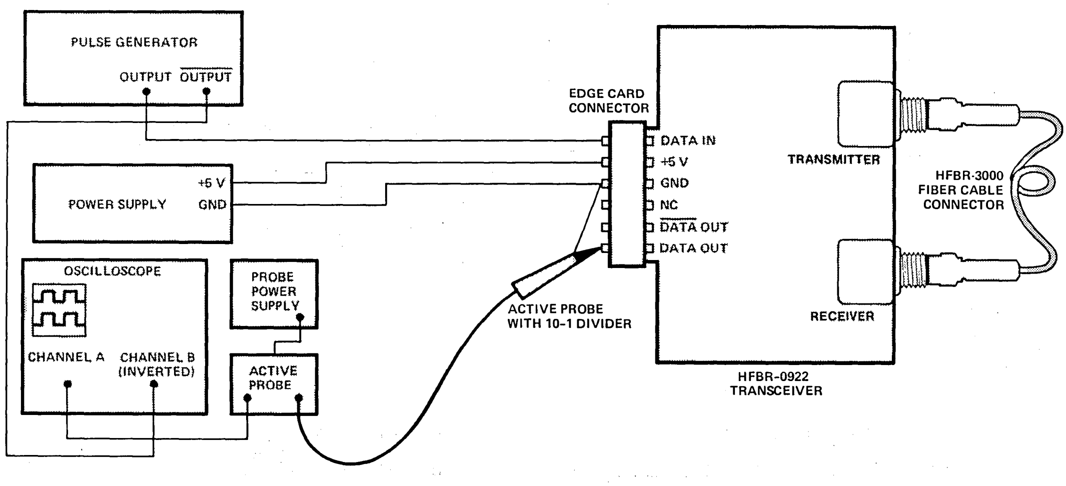


Figure 7.

Notes:
1. The data out observed through the active probe exhibits overshoot at the rising edge. This overshoot will disappear if the output is loaded to drive a TTL input.
2. Oscilloscope inputs should be terminated into 50 ohms.
3. The active probe should be set on DC for observation of lower data rates. The offset on the active probe should be off.
4. The active probe is used to avoid reflection in the observed signal through impedance matching.
5. If necessary clean the optical port of the fiber connectors with Acetone before connecting them to the transceivers.

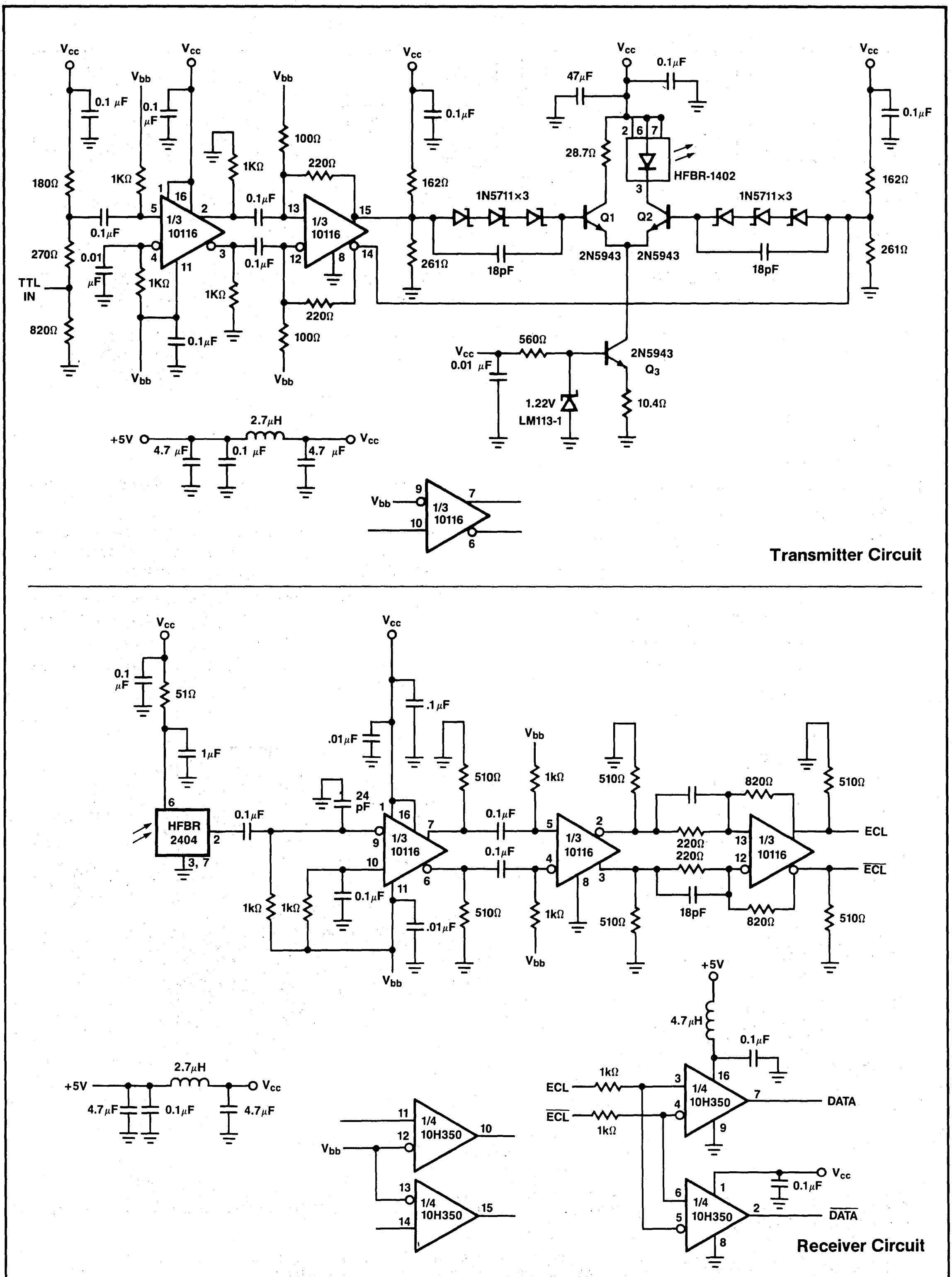


Figure 2. 50 MBaud Transceiver Circuit

50 MBaud Transceiver Circuit

Figure 3 shows the circuit diagram for a 50 MBaud link (the HFBR-0422 Transceiver Board). The transmitter side utilizes a 10116 ECL line receiver as an amplifier with hysteresis driving a differential transistor pair, Q1 and Q2. The HFBR-1042 LED is switched on and off by the pair with current source Q3 controlling the LED forward current. The shunt switch arrangement demands equal amount of supply currents while switching the HFBR-1402 LED, thus minimizing supply noise generated. The input resistor network (180Ω/270Ω/810Ω) can be deleted for ECL applications and -5.2V substituted for +5V operation.

The receiver circuit cascades two 10116 stages to form a post amplifier. The output of the HFBR-2404 is amplified and fed to the 10116 third stage amplifier with hysteresis. The 820 and 220 resistors provide about 75mV of hysteresis.The setting of the hysteresis affects the overall sensitivity of the receiver. Excessively high hysteresis translates to "wasted" input optical power. Low hysteresis threshold allows noise in the circuit to randomly switch the output logic state when there is no light input. The hysteresis in the circuit is set on the low side to maximize receiver sensitivity. Increasing the 220 resistances will raise the hysteresis.

The 10H350 is an ECL to TTL converter. It can be eliminated for ECL applications and –5.2V substitued for +5V operation. Throughout the receiver circuit, proper power supply filtering is critical in order to achieve ultimate performance. The 10116 ECL line receiver used in the +5V and ground configuration is especially susceptable to noise on the +5V line.

Figure 3 gives the link configuration and the performance of the HFBR-0422 Transceiver Board and is specified on the next page. Figure 4 shows the transmitter output power versus temperature, Figure 5 shows the receiver sensitivity versus temperature, and Figure 6 gives the receiver sensitivity for different data rates. The test set-up for the transceiver board is shown in Figure 7, and Figure 8 gives the mechanical dimensions of the board. Component list and the circuit board layout for the 50 MBd Transceiver Board are shown in Figure 9 and Figure 10 respectively.

FIBER OPTICS

LINK CONFIGURATION

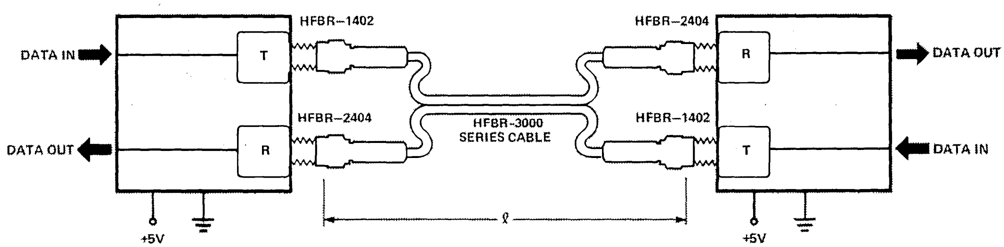


Figure 3. 50 MBaud TTL Duplex Link

Mechanical Dimensions

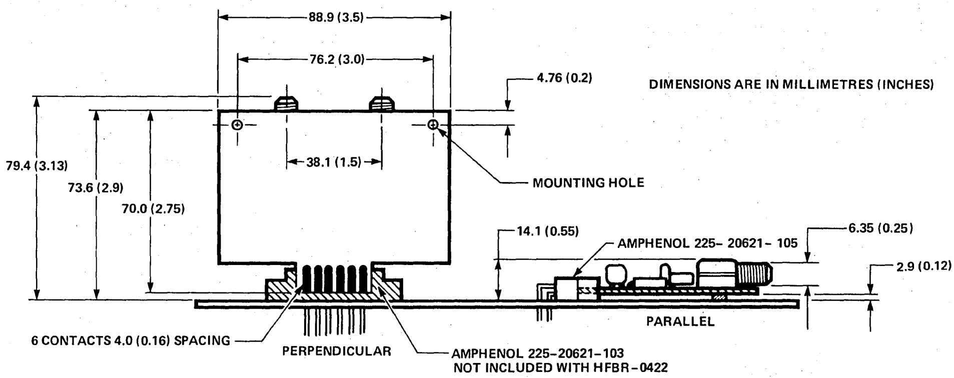


Figure 8.

Components List

Resistors	Part Description
R1	Resistor 51.1 Ohm; 1%; 1/8W
R2	Resistor 0 Ohm; Jumper Wire
R3,4,7,8,17,18,22,23	Resistor 1K Ohm; 1%; 1/8W
R5,6,9,10,15,16,24,25	Resistor 510 Ohm; 5%; 1/8W
R11, 12, 28, 29	Resistor 220 Ohm; 5%; 1/8W
R13, 14, 21	Resistor 820 Ohm; 5%; 1/8W
R19	Resistor 180 Ohm; 5%; 1/8W
R20	Resistor 270 Ohm; 5%; 1/8W
R26, 27	Resistor 100 Ohm; 5%; 1/8W
R30, 35	Resistor 162 Ohm; 1%; 1/8W
R31, 26	Resistor 261 Ohm; 1%; 1/8W
R32	Resistor 560 Ohm; 5%; 1/8W
R33	Resistor 28.7 Ohm; 1%; 1/8W
R34	Resistor 10.5 Ohm; 1%; 1/8W

Capacitor	Part Description
C1, 3, 5, 7 9, 10, 14, 16-19	Capacitor 0.1μf; 20%; 50V; ceramic
C24-28,31,32,34,36	Capacitor 0.1μf; 20%; 50V; ceramic
C4	Capacitor 25pf; 5%; 200V; ceramic
C6, 8, 20	Capacitor .01μf; 20%; 100V ceramic
C11, 12, 29, 33	Capacitor 18pf; 5%; 200V; ceramic
C2, 13, 15, 35, 37	Capacitor 4.7μf; 20%; 35V; tantalum
C30	Capacitor 47μf; 20%; 8V; tantalum

Inductor	Part Description
L1, 2	Inductor 2.7μH
L3	Inductor 4.7 μH

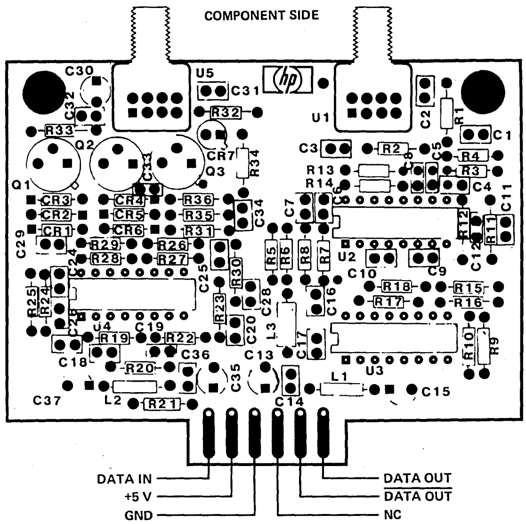
Diode	Part Description
CR1-6	Diode 1N5711
CR7	Diode LM113-1

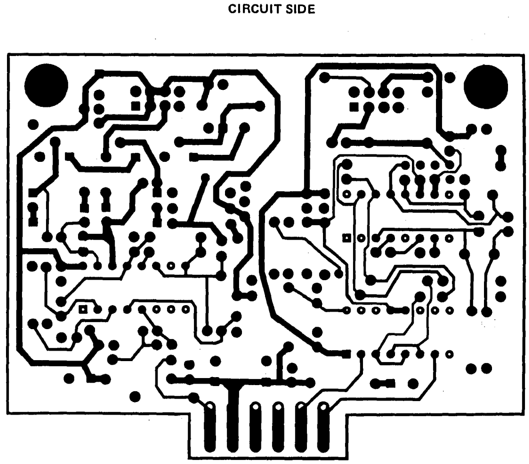
Transistor	Part Description
Q1-3	Transistor 2N5943

Integrated Circuit	Part Description
U1	IC HFBR-2404
U2, 4	IC 10116
U3	IC 10H350
U5	IC HFBR-1402

Figure 9.

PRINTED CIRCUIT BOARD LAYOUT





For more information on the printed circuit board layout, please contact your HP component sales representative.

Figure 10.

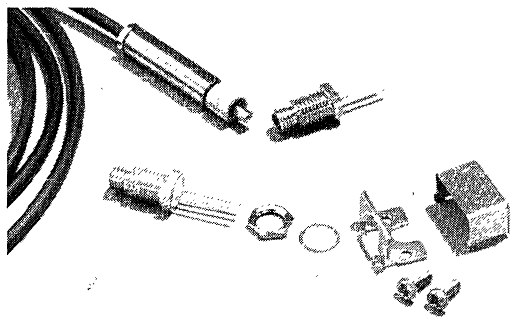
MINIATURE FIBER OPTIC LOGIC LINK

HFBR-0200
HFBR-1201/2
HFBR-2201/2
HFBR-4201/2

TECHNICAL DATA JANUARY 1986

Features

- **DC TO 5 MBAUD DATA RATE**
- **MAXIMUM LINK LENGTH**
  625 Metres (Guaranteed)
  1600 Metres (Typical)
- **TTL/CMOS COMPATIBLE OUTPUT**
- **MINIATURE, RUGGED METAL PACKAGE**
- **SINGLE +5V RECEIVER POWER SUPPLY**
- **INTERNALLY SHIELDED RECEIVER FOR EMI/RFI IMMUNITY**
- **PCB AND PANEL MOUNTABLE**
- **LOW POWER CONSUMPTION**



Applications

- **EMC REGULATED SYSTEMS (FCC, VDE)**
- **EXPLOSION PROOF SYSTEMS IN OIL INDUSTRY/CHEMICAL PROCESS CONTROL INDUSTRY**
- **SECURE DATA COMMUNICATIONS**
- **WEIGHT SENSITIVE SYSTEMS (e.g. Avionics, Mobile Stations)**
- **HIGH VOLTAGE ISOLATION IN POWER GENERATION**

Description

The HFBR-1201/2 Transmitter and HFBR-2201/2 Receiver are HFBR-4000/SMA style connector compatible fiber optic link components. Distances to 1600 metres at data rates up to 5 MBaud are achievable with these components and the HFBR-3000/3100 series fiber optic cable assemblies.

A complete evaluation kit is available (HFBR-0200) containing an HFBR-1201 transmitter, HFBR-2201 receiver, HFBR-4201 mounting hardware, 10m of HFBR-3000 option 001 cable/connector assembly and technical literature.

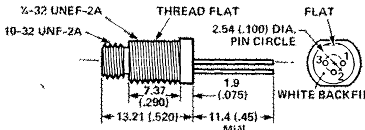
The HFBR-1201/2 Transmitter contains a high efficiency GaAlAs emitter operating at 820 nm. Consistent coupling efficiency is assured by factory alignment of the LED with the optical axis of the package. Power coupled into the fiber varies less than 4 dB from part to part at a given temperature and drive current. The benefit of this is reduced dynamic range requirements on the receiver.

The HFBR-2201/2 Receiver incorporates a photo IC containing a photodetector and dc amplifier. An open collector Schottky transistor on the IC provides logic compatibility. The combination of an internal EMI shield, the metal package and an isolated case ground provides excellent immunity to EMI/RFI. For unusually severe EMI/ESD environments, a snap-on metal shield is available. The receiver is easily identified by the black epoxy backfill.

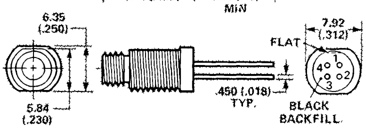
The HFBR-1201 Transmitter and the HFBR-2201 Receiver are compatible with the HFBR-4000 Connector and HFBR-3000 series, Option 001 connectored cable. The HFBR-1202 Transmitter and HFBR-2202 Receiver are compatible with SMA style connectors, types A and B (see Figure 12), and HFBR-3000 series, Option 002 connectored cable. HFBR-3000 series cable can be ordered with or without connectors. The HFBR-0100 connector assembly kit is available if field installation of HFBR-4000 connectors is desired.

Mechanical Dimensions

HFBR-1201 TRANSMITTER



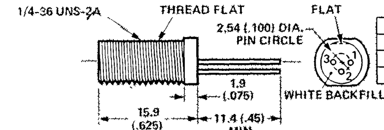
PIN	FUNCTION
1	ANODE
2	CATHODE
3	CASE



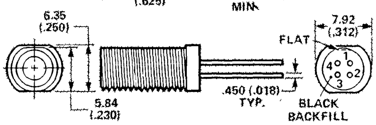
PIN	FUNCTION
1	CASE
2	V_{CC}
3	DATA
4	COMMON

HFBR-2201 RECEIVER

HFBR-1202 TRANSMITTER



PIN	FUNCTION
1	ANODE
2	CATHODE
3	CASE



PIN	FUNCTION
1	CASE
2	V_{CC}
3	DATA
4	COMMON

HFBR-2202 RECEIVER

DIMENSIONS IN MILLIMETRES (INCHES)
UNLESS OTHERWISE SPECIFIED, THE TOLERANCES ARE:
.X ± .51 mm (.XX ± .02 IN)
.XX ± .13 mm (.XXX ± .005 IN)

System Design Considerations

The Miniature Fiber Optic Logic Link is guaranteed to work over the entire range of 0 to 625 metres at a data rate of dc -5 MBd, with arbitrary data format and typically less than 25% pulse width distortion, if the Transmitter is driven with I_F = 40 mA, R_1 = 82Ω. If it is desired to economize on power or achieve lower pulse distortion, then a lower drive current (I_F) may be used. The following example will illustrate the technique for optimizing I_F.

EXAMPLE: Maximum distance required = 250 metres. From Figure 2 the worst case drive current = 20 mA. From the Transmitter data — V_F = 1.8V (max.).

$$R_1 = \frac{V_{CC} - V_F}{I_F} = \frac{5 - 1.8V}{20\ mA} = 160\Omega$$

The optical power margin between the typical and worst case curves (Figure 2) at 250 metres is 4 dB. To calculate the worst case pulse width distortion at 250 metres, see Figure 8. The power into the Receiver is P_{RL} + 4 dB = -20 dBm. Therefore, the typical distortion is 40 ns or 20% at 5 MBd.

CABLE SELECTION

The link performance specifications on the following page are based on using the HFBR-3000/HFBR-3100 cable/connector assemblies. These cables contain glass-clad silica fibers with a 100 μm core diameter and 140 μm cladding diameter. This fiber type is now a user accepted standard for local data communications links (RS-458, Class I, Type B). The HFBR-1201/2 Transmitter and HFBR-2201/2 Receiver are optimized for use with the 100/140 μm fiber. There is, however, no fundamental restriction against using other fiber types. Before selecting an alternate fiber type, several parameters need to be carefully evaluated.

The attenuation (dB/km) of the selected fiber, in conjunction with the amount of optical power coupled into it will determine the achievable link length. The parameters that will significantly affect the optical power coupled into the fiber are as follows:

a. **Fiber Core Diameter.** As the core diameter is increased, the optical power coupled increases, leveling off at about 250 μm diameter.
b. **Numerical Aperture (NA).** As the NA is increased, the optical power coupled increases, leveling off at an NA of about 0.34.
c. **Index Profile (α).** The Index profile parameter of fibers varies from 2 (fully graded index) to infinite (step index). Some gains in coupled optical power can be achieved at the expense of bandwidth, when α is increased.

In addition to the optical parameters, the environmental performance of the selected fiber/cable must be evaluated. Finally, the ease of installing connectors on the selected fiber/cable must be considered. Given the large number of parameters that must be evaluated when using a non-standard fiber, it is recommended that the 100/140 μm fiber be used unless unusual circumstances warrant the use of an alternate fiber/cable type.

SMA STYLE CONNECTORS

The HFBR-1202/2202 is compatible with either the Type A or Type B SMA style fiber optic conector (see Figure 12). The basic difference between the two connectors is the plastic half-sleeve on the stepped ferrule tip of the Type B connector. This step provides the capability to use a full length plastic sleeve to ensure good alignment of two connectors for an inline splice. The HFBR-3000/HFBR-3100, OPT 002 series connectored cable utilizes the Type A connector system because of the inherent environmental advantages of metal-to-metal interfaces.

The HFBR-1201/2201 is compatible with HFBR-4000 connectors and HFBR-3000/HFBR-3000 Option 001 series connectored cable

Typical Circuit Configuration

NOTE:
IT IS ESSENTIAL THAT A BYPASS CAPACITOR (0.01 μF to 0.1 μF CERAMIC) BE CONNECTED FROM PIN 2 TO PIN 4 OF THE RECEIVER. TOTAL LEAD LENGTH BETWEEN BOTH ENDS OF THE CAPACITOR AND THE PINS SHOULD NOT EXCEED 20 mm.

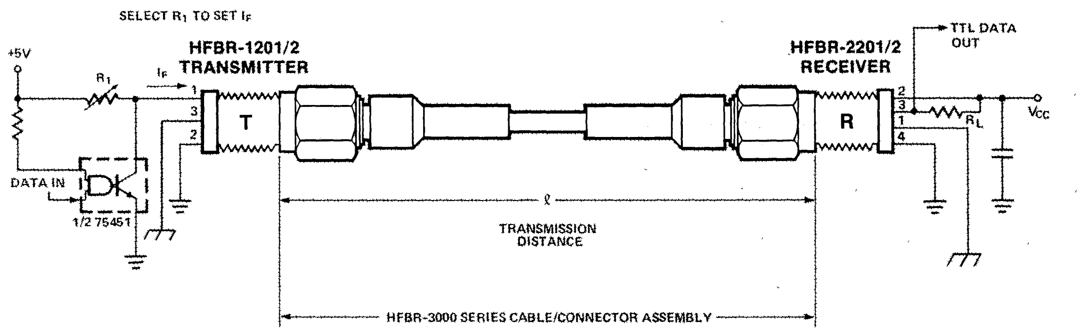


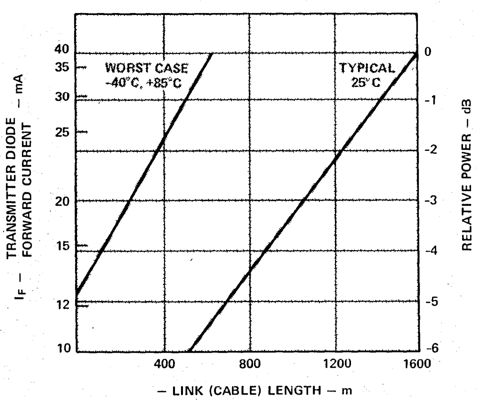
Figure 1.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Reference
TRANSMITTER					
Ambient Temperature	T_A	-40	+85	°C	
Peak Forward Input Current	$I_{F,PK}$		40	mA	Note 7
Average Forward Input Current	I_{FAV}		40	mA	Note 7
RECEIVER					
Ambient Temperature	T_A	-40	+85	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	
Fan Out (TTL)	N		5		Note 3, Fig. 1
CABLE (see HFBR-3000/HFBR-3100 data sheet)					

System Performance -40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.[1]	Typ.	Max.	Units	Conditions	Reference
Transmission Distance	ℓ	625	1600		Metres		Fig. 2, Note 9
Data Rate Synchronous		dc		5	MBaud		Note 10
Asynchronous		dc		2.5	MBaud		Note 10, Fig. 8
Propagation Delay LOW to HIGH	t_{PLH}		82		nsec	$T_A = 25°C$, $P_R = -21$ dBm $I_{F,PK} = 15$ mA ℓ = 1 metre	Fig. 7, 8, 9
Propagation Delay HIGH to LOW	t_{PHL}		55		nsec		
System Pulse Width Distortion	t_D		27		nsec		
Bit Error Rate	BER			10^{-9}		Data Rate ≤5 MBaud $P_R > -24$ dBm (4μW)	



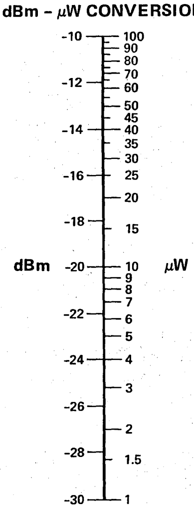


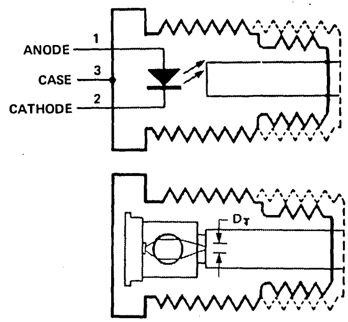
Figure 2. System Performance: HFBR-1201/2/HFBR-2201/2 with HFBR-3000/3100 Cable Assembly

HFBR-1201/1202 TRANSMITTER

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	Note 13
Lead Soldering Cycle	Temp.			+260	°C	Note 2
	Time			10	sec	
Forward Input Current	Peak	$I_{F,\ PK}$		40	mA	Note 7
	Average	$I_{F,\ AV}$		40	mA	
Reverse Input Voltage		V_R		2.5	V	

HFBR-1201/1202 TRANSMITTER



Electrical/Optical Characteristics -40°C to +85°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Forward Voltage	V_F		1.5	1.8	V	$I_F = 40$ mA	Figure 5
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-0.91		mV/°C	$I_F = 40$ mA	Figure 5
Reverse Breakdown Voltage	V_{BR}	2.5	4.0		V	$I_R = 100\ \mu A$	
Numerical Aperture	NA		.34				
Optical Port Diameter	D_T		250		μm		Note 11
Peak Emission Wavelength	λ_P		820		nm		Figure 6
Output Optical Power Coupled into HFBR-3000 Fiber Cable/Connector Assembly, 100/140 μm	P_T	-17	-16	-13	dBm	$I_F = 40$ mA	Figure 3
		20	25	50	μW	$T_A = 25°C$	Notes 4, 15
		-18		-12.3	dBm	$I_F = 40$ mA	
		15.8		59	μW	$-40°C < T_A < 85°C$	
Output Optical Power Coupled into 50/125 μm Fiber	P_T		-24		dBm	$I_F = 40$ mA	Figure 3
			4		μW	$T_A = 25°C$	Notes 14, 15
Output Optical Power Coupled into Siecor 100/140 μm Fiber Cable or Equivalent	P_T		-18		dBm	$I_F = 40$ mA $T_A = 25°C$	Figure 3 Notes 15, 16
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-.017		dB/°C		Figure 4

Dynamic Characteristics -40°C to +85°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Propagation Delay LOW to HIGH	t_{PLH}		17		nsec	$I_{F\ PK} = 10$ mA	Note 8 Figure 7
Propagation Delay HIGH to LOW	t_{PHL}		6		nsec		

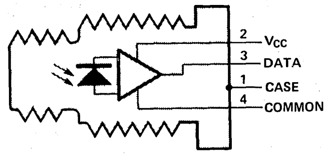
Notes:
1. Typical data at $T_A = 25°C$, $V_{CC} = 5.0V$ dc.
2. 2.0 mm from where leads enter case.
3. 8 mA load (5 x 1.6 mA). $R_L = 560\Omega$.
4. Measured at the end of 1.0 metre HFBR-3000 Fiber Optic Cable with large area detector and cladding modes stripped, terminated with the appropriate type of connector. This assembly approximates a Standard Test Fiber. The fiber NA is 0.28, measured at the end of greater than 300 metres length of fiber, the NA being defined as the sine of the half angle determined by the 10% intensity points.
5. Measured at the end of HFBR-3000 Fiber Optic Cable with large area detector.
6. When changing microwatts to dBm, the optical flux is referenced to one milliwatt (1000 μW).
$$\text{Optical Flux, P (dBm)} = 10 \log \frac{P\ (\mu W)}{1000\ \mu W}$$
7. I_{FPK} should not be less than 10 mA in the "ON" state. This is to avoid the long turn-on time that occurs at low input current. I_{FAV} may be arbitrarily low, as there is no duty factor restriction.

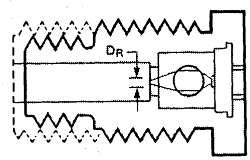
WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe; however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 2
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	+7.0	V	
Output Current		I_O		25	mA	
Output Voltage		V_O	-0.5	+18.0	V	
Output Collector Power Dissipation		$P_{O,\,AV}$		40	mW	

HFBR-2201/2202 RECEIVER





Electrical/Optical Characteristics

−40° C to +85° C and 4.75 ≤ V_{CC} ≤ 5.25 V unless otherwise specified.

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
High Level Output Current	I_{OH}		5	250	μA	V_O = 18V P_R < -40 dBm	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_O = 8 mA P_R > -24 dBm	
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V P_R < -40 dBm	
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R > -24 dBm	
Optical Port Diameter	D_R		700		μm		Note 12
Numerical Aperture	NA		.32				

Dynamic Characteristics

−40° C to +85° C and 4.75 ≤ V_{CC} ≤ 5.25 V unless otherwise specified.

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Input Power Level Logic HIGH	P_{RH}			-40	dBm	λ_P = 820 nm	Note 5
				0.1	μW		
Input Power Level Logic LOW	P_{RL}	-25.4		-11.2	dBm	T_A= +25° C	Fig. 4, Note 5
		2.9		76	μW		
		-24		-12.0	dBm	-40 < T_A < 85° C	
		4.0		63	μW		
Propagation Delay LOW to HIGH	t_{PLHR}		65		nsec	T_A = 25° C, P_R = -21 dBm	Note 8, Fig. 7
Propagation Delay HIGH to LOW	t_{PHLR}		49		nsec		

Notes:

8. Propagation delay through the system is the result of several sequentially-occurring phenomena. Consequently it is a combination of data-rate-limiting effects and of transmission-time effects. Because of this, the data-rate limit of the system must be described in terms of time differentials between delays imposed on falling and rising edges.

   As the cable length is increased, the propagation delays increase at 5 ns per metre of length increase. Data rate, as limited by pulse width distortion, is not affected by increasing cable length if the optical power level at the Receiver is maintained.
9. Worst case system performance is based on worst case performance of individual components: transmitter at +85° C, receiver at -40° C and cable at- 20° C.
10. Synchronous data rate limit is based on these assumptions: (a) 50% duty factor modulation, e.g. Manchester I or BiPhase (Manchester II); (b) continuous data; (c) PLL (Phase Lock Loop) demodulation; (d) TTL threshold.

    Asynchronous data rate limit is based on these assumptions: (a) NRZ data; (b) arbitrary timing — no duty factor restriction; (c) TTL threshold.

    The EYE pattern describes the timing range within which there is no uncertainty of the logic state, relative to a specific threshold, due to either noise or intersymbol (prop. delay) effects.
11. D_T is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of its maximum.
12. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
13. HFBR-3000 series Fiber Cable is specified at a narrower temperature range, −20° C to 85° C.
14. Measured at the end of 1.0 metre 50/125 μm fiber with large area detector and cladding modes stripped, approximating a Standard Test Fiber. The fiber NA is 0.21, measured at the end of a 2.0 metre length, the NA being defined as the sine of the half angle determined by the 5% of peak intensity points. Measured by the method of Note 4, the corresponding NA is 0.185.
15. Output Optical Power into connectored fiber cable other than HFBR-3000 Fiber Optic Cable/Connector Assemblies may be different than specified because of mechanical tolerances of the connector, quality of the fiber surface, and other variables.
16. Measured at the end of 1.0 metre Siecor 100/140 μm fiber cable or equivalent, with large area detector and cladding modes stripped, terminated with the appropriate type of connector. This assembly approximates a Standard Test Fiber. The fiber NA is 0.275, measured at the end of a 2.0 metre length, the NA being defined as the sine of the half angle determined by the 5% of peak intensity points. Measured by the method of Note 4, the corresponding NA value is 0.232.

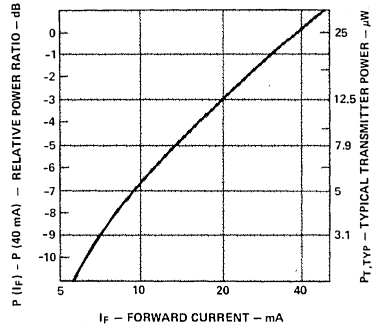


Figure 3. Normalized Transmitter Output vs. Forward Current

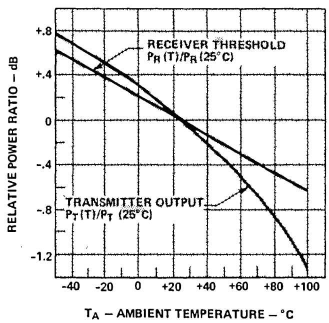


Figure 4. Normalized Thermal Effects in Transmitter Output, Receiver Threshold, and Link Performance (Relative Threshold)

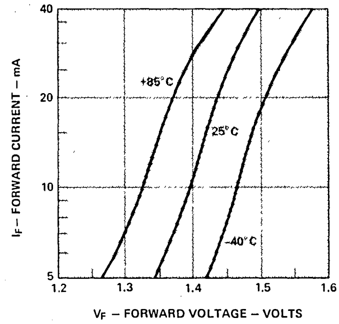


Figure 5. Forward Voltage and Current Characteristics for the Transmitter LED.

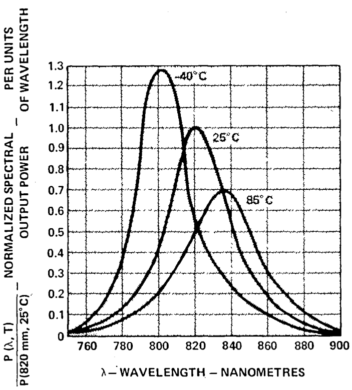


Figure 6. Transmitter Spectrum Normalized to the Peak at 25°C

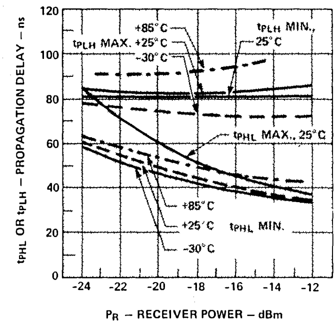


Figure 7. Propagation Delay through System with One Metre of Cable

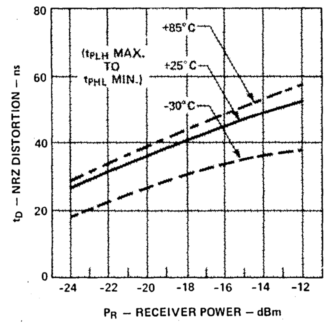


Figure 8. Worst-Case Distortion of NRZ EYE-pattern with Pseudo Random Data at 10 Mb/s. (see note 10).

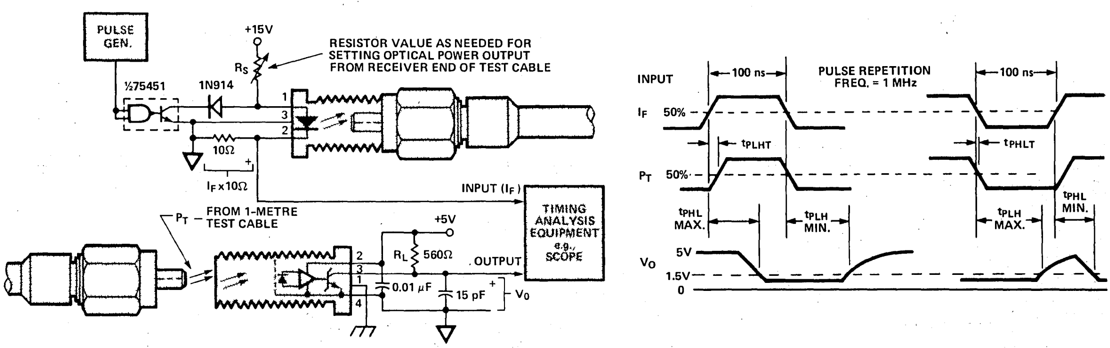


Figure 9. System Propagation Delay Test Circuit and Waveform Timing Definitions

Electrical Description

The HFBR-1201/2 Transmitter contains a GaAlAs infrared emitter. Both the anode and cathode of the emitter are insulated from the case. This configuration permits the use of a variety of drive circuitry such as series switching, shunt-switching and high frequency peaking. There is no internal drive circuit or current limiter.

The HFBR-2201/2 Receiver incorporates an integrated photo IC containing a photodetector and dc amplifier driving an open-collector Schottky output transistor. The HFBR-2201/2 is designed for direct interfacing to popular logic families. The absence of an internal pull-up resistor allows the open-collector output to be used with logic families such as CMOS requiring voltage excursions much higher than V_{CC}. Both the open-collector "Data" output (Pin 3) and V_{CC} (Pin 2) are referenced to "Com" (Pin 4). The "Data" output allows busing, strobing and wired "OR" circuit configurations. Both the transmitter and receiver are designed to operate from a single +5V supply. Note that the "Com" and "Case" pins are not connected internally.

The HFBR-1201/2 and HFBR-2201/2 optical receptacles contain a lens to optimize the coupling between the fiber and the active optical device.

Horizontal PCB Mounting

Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

When bending the leads, avoid sharp bends right where the lead enters the backfill. Use needle nose pliers to support the leads at the base of the package and bend the leads as desired.

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.

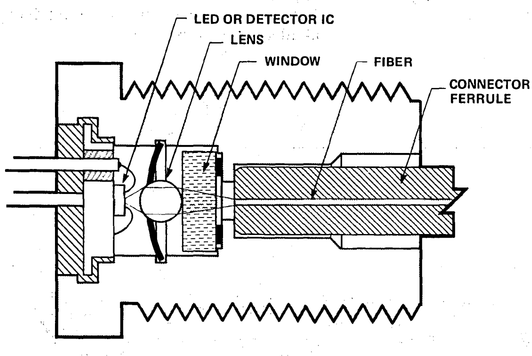


Figure 10. Cross Sectional View

Mechanical Description

The HFBR-1201/2 fiber optic transmitter and HFBR-2201/2 receiver are housed in rugged metal packages intended for use with the HFBR-3000/HFBR-3100 cable assemblies. The low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking. A flat on the mounting threads of the device is provided to prevent rotation in all mounting configurations and to provide an orientation reference for the pin-out. Hardware is available for horizontal mounting applications on printed circuit boards. The hardware consists of a stainless steel mounting bracket fastened directly to the printed circuit board with two stainless steel self-tapping screws and a nut and washer for fastening the device in the bracket. A metal shield which snaps directly on the mounting bracket is also available for unusually severe EMI/ESD environments. When mounted in the horizontal configuration, the overall height of the component conforms with guidelines allowing printed circuit board spacing on 12.7 mm (.500) centers. A thorough environmental characterization has been performed on these products. The test data as well as information regarding operation beyond the specified limits is available from any Hewlett-Packard sales office.

Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well.

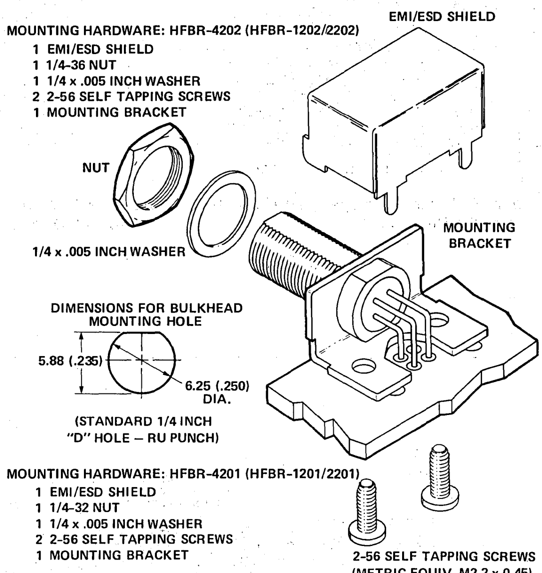
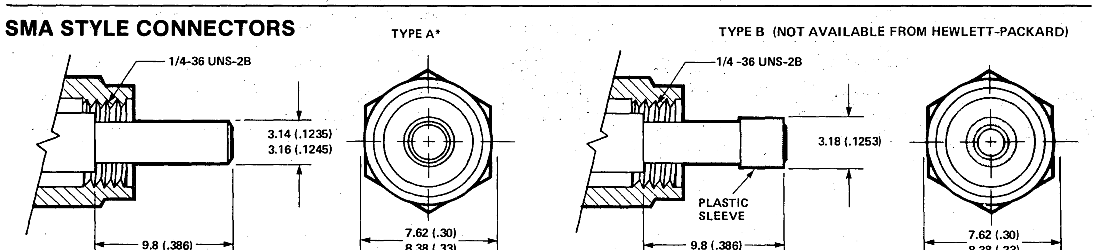


Figure 11.



*USED IN HFBR-3000/3100 OPT 002 CABLE ASSEMBLIES.

Figure 12.

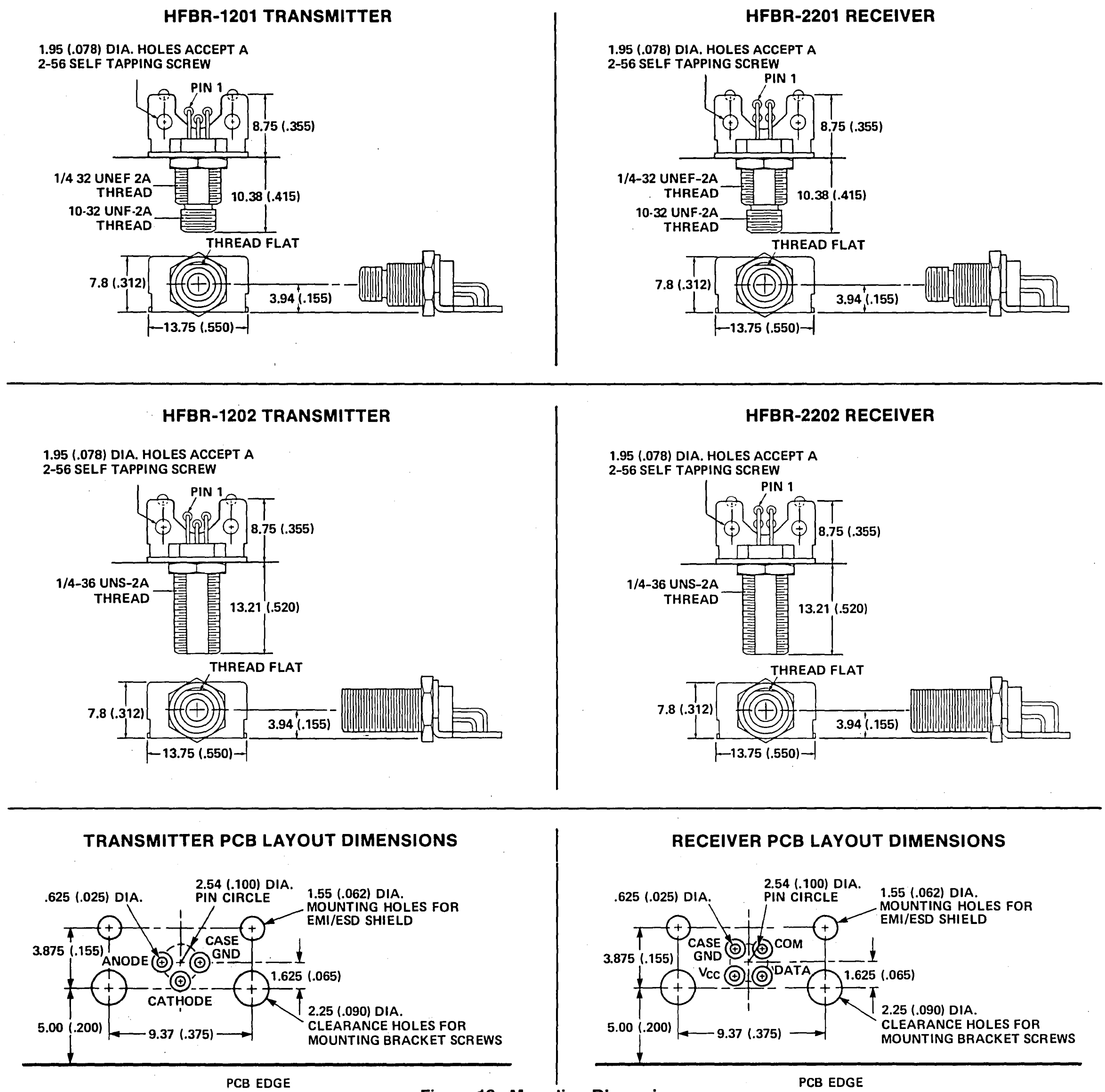


Figure 13. Mounting Dimensions
DIMENSIONS IN MILLIMETRES (INCHES).

Ordering Guide

Transmitter: HFBR-1201 (HP Connector Compatible)
HFBR-1202 (SMA Connector Compatible)

Receiver: HFBR-2201 (HP Connector Compatible)
HFBR-2202 (SMA Connector Compatible)

Mounting Hardware: HFBR-4201 (HP Connector Compatible)
HFBR-4202 (SMA Connector Compatible)

HFBR-0200 Kit:

HFBR-1201 Transmitter
HFBR-2201 Receiver
HFBR-4201 Mounting Hardware (2 sets)
HFBR-3000 10 Metre Cable/Connector Assembly
Technical Literature

Fiber Optic Cable — see data sheets

HFBR-3000 Single Channel Connectored — Custom Lengths
HFBR-3100 Dual Channel Connectored — Custom Lengths
Note: Option 001 specifies HFBR-4000 connector and Option 002 specifies SMA connectors.
HFBR-3001 Single Channel Connectored — 10 metres (HFBR-4000 connectors)
HFBR-3021 Single Channel Connectored — 10 metres (SMA connectors)
HFBR-3200 Unconnectored Single Channel — Custom Lengths
HFBR-3300 Unconnectored Dual Channel — Custom Lengths

HEWLETT PACKARD

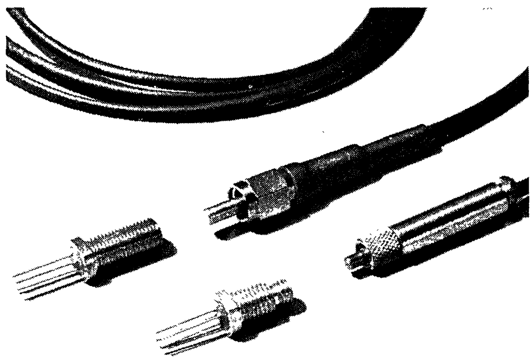
HIGH EFFICIENCY FIBER OPTIC TRANSMITTER

HFBR-1203
HFBR-1204

TECHNICAL DATA JANUARY 1986

Features

- **OPTICAL POWER COUPLED INTO 100/140 μm FIBER CABLE**
  —9.8 dBm Guaranteed at 25° C
  —7.4 dBm Typical
- **FACTORY ALIGNED OPTICS**
- **RUGGED MINIATURE PACKAGE**
- **COMPATIBLE WITH HP OR SMA STYLE CONNECTORS**



Description

The HFBR-1203/-1204 Fiber Optic Transmitter contains an etched-well 820 nm GaAlAs emitter capable of coupling greater than −10 dBm of optical power into 100/140 μm HFBR-3000 Fiber Cable/Connector Assemblies. This high power level is useful for fiber lengths greater than 1 km, or systems where star couplers, taps, or in-line connectors create large fixed losses.

Consistent coupling efficiency is assured by factory alignment of the LED with the mechanical axis of the package connector port. Power coupled into the fiber varies less than 5 dB from part to part at a given drive current and temperature. The benefit of this is reduced dynamic range requirements on the receiver.

High coupling efficiency allows the emitters to be driven at low current levels resulting in low power consumption and increased reliability of the transmitter. Another advantage of the high coupling efficiency is that a significant amount of power can still be launched into smaller fiber such as 50/125 μm (−19.1 dBm typ.).

The HFBR-1203/-1204 transmitter is housed in a rugged miniature package. The lens is suspended to avoid mechanical contact with the active devices. This assures improved reliability by eliminating mechanical stress on the die due to the lens. For increased ESD protection and design flexibility, both the anode and cathode are insulated from the case.

HFBR-1203 is compatible with HFBR-4000 connectors, and HFBR-1204 is compatible with SMA style connectors. The low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking. A complete mounting hardware package (HFBR-4201/-4202) is available for horizontal mounting on PCBs, including a snap-on metal shield for harsh EMI/ESD environments.

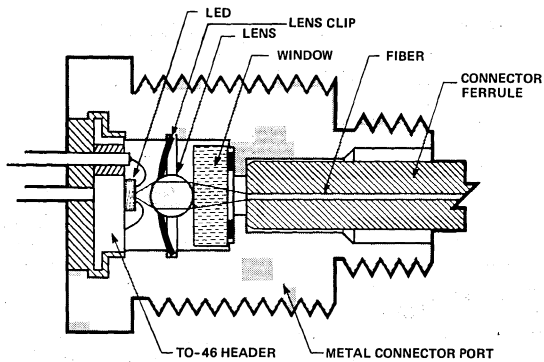
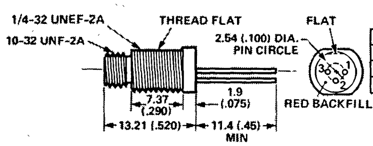


Figure 1. Cross Sectional View

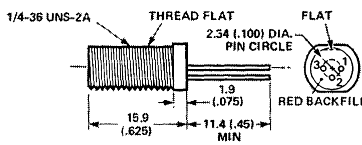
Mechanical Dimensions

HFBR-1203



PIN	FUNCTION
1	ANODE
2	CATHODE
3	CASE

HFBR-1204



PIN	FUNCTION
1	ANODE
2	CATHODE
3	CASE

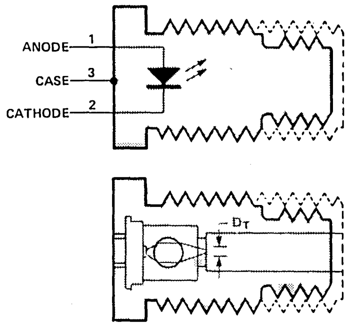
DIMENSIONS IN MILLIMETRES (INCHES)

HFBR-1203/-1204 TRANSMITTER

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	Note 4
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Forward Input Current	Peak	$I_{F,PK}$		100	mA	
	Average	$I_{F,AV}$		100	mA	
Reverse Input Voltage		V_R		1.0	V	
Voltage, Case-to-Junction		V_C		25	V	

HFBR-1203/1204 TRANSMITTER



Electrical/Optical Characteristics

−40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Forward Voltage	V_F	1.44	1.72	1.94	V	$I_F = 100$ mA	Figure 2
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-0.54		mV/°C	$I_F = 100$ mA	Figure 2
Reverse Breakdown Voltage	V_{BR}	1.0	3.1		V	$I_R = 100\ \mu A$	
Numerical Aperture	NA		0.38				
Optical Port Diameter	D_T		250		μm		Note 3
Peak Emission Wavelength	λ_P		820		nm		Figure 5
Output Optical Power Coupled into HFBR-3000 Fiber Cable/Connector Assembly, 100/140 μm Fiber	P_T	-9.8	-7.4	-5.0	dBm	$I_F = 100$ mA	Figure 3, 4
		105	182	316	μW	$T_A = 25°C$	Notes 4, 5, 6, 8
		-11.2		-4.2	dBm	$I_F = 100$ mA	
		76		380	μW	$-40°C < T_A < 85°C$	
Output Optical Power Coupled into 50/125 μm Fiber	P_T		-19.1		dBm	$I_F = 100$ mA	Figure 3, 4
			12		μW	$T_A = 25°C$	Notes 5, 7
Output Optical Power Coupled into Siecor 100/140 μm Fiber Cable or Equivalent	P_T		-9.4		dBm	$I_F = 100$ mA $T_A = 25°C$	Figure 3, 4 Notes 5, 11
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-.014		dB/°C	$I_F = 100$ mA	Figure 3
Case Isolation Resistance (Case to Pins 1 or 2)	R_{CASE}	1			MΩ	$V_{CASE} = 25$ V	
Thermal Resistance	Θ_{JC}		90		°C/W		Note 9
Rise Time, Fall Time (10 to 90%)	t_r, t_f		11		nsec		Figure 6 Note 10

WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe; however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Notes:

1. 2.0 mm from where leads enter case.
2. Typical data at $T_A = 25°C$.
3. D_T is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of the maximum.
4. HFBR-3000 series Fiber Cable is specified at a narrower temperature range, −20° C to 85° C.
5. Output Optical Power into connectored fiber cable other than HFBR-3000 Fiber Optic Cable/Connector Assemblies may be different than specified because of mechanical tolerances of the connector, quality of the fiber surface, and other variables.
6. Measured at the end of 1.0 metre HFBR-3000 Fiber Optic Cable with large area detector and cladding modes stripped, terminated with the appropriate type of connector. This assembly approximates a Standard Test Fiber. The fiber NA is 0.28, measured at the end of greater than 300 metres length of fiber, the NA being defined as the sine of the half angle determined by the 10% intensity points.

7. Measured at the end of 1.0 metre 50/125 μm fiber with large area detector and cladding modes stripped, approximating a Standard Test Fiber. The fiber NA is 0.21, measured at the end of a 2.0 metre length, the NA being defined as the sine of the half angle determined by the 5% of peak intensity points. Measured by the method of Note 6, the corresponding NA is 0.185.
8. When changing microwatts to dBm, the optical power is referenced to 1 milliwatt (1000 μW).
   Optical Power, P (dBm) = 10 log P (μW)/1000 μW
9. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board with the HFBR-4201 mounting hardware.
10. Measured with a 1 mA pre-bias current and terminated into a 50 ohm load.
11. Measured at the end of 1.0 metre Siecor 100/140 μm fiber cable or equivalent, with large area detector and cladding modes stripped, terminated with the appropriate type of connector. This assembly approximates a Standard Test Fiber. The fiber NA is 0.275, measured at the end of a 2.0 metre length, the NA being defined as the sine of the half angle determined by the 5% of peak intensity points. Measured by the method of Note 6, the corresponding NA value is 0.232.

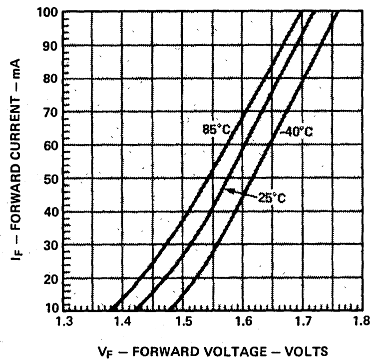


Figure 2. Forward Voltage and Current Characteristics

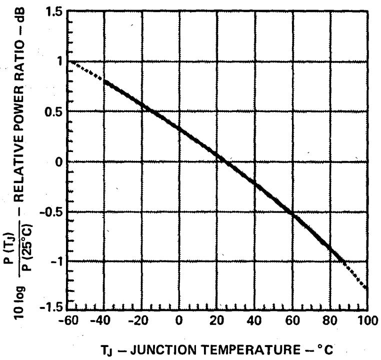


Figure 3. Normalized Thermal Effects in Transmitter Output

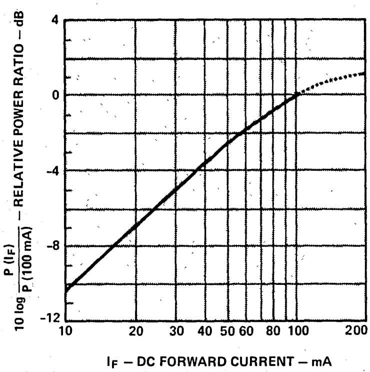


Figure 4. Normalized Transmitter Output vs. DC Forward Current

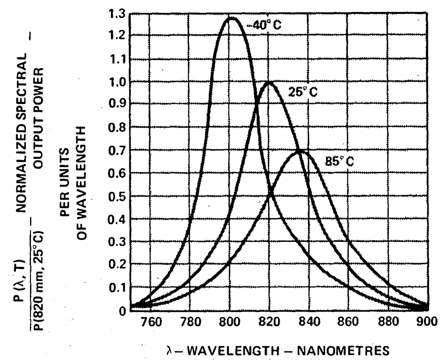


Figure 5. Transmitter Spectrum Normalized to the Peak at 25°C

Ordering Guide

Transmitter: HFBR-1203 (HP Connector Compatible)
HFBR-1204 (SMA Connector Compatible)

Receiver: HFBR-2201 (5 MBaud, HP Connector)
HFBR-2202 (5 MBaud, SMA Connector)
HFBR-2203 (40 MBaud, HP Connector Compatible)
HFBR-2204 (40 Mbaud, SMA Connector Compatible)

Mounting Hardware: HFBR-4201 (HP Connector Compatible)
HFBR-4202 (SMA Connector Compatible)

Fiber Optic Cable — see data sheets

HFBR-3000 Single Channel Connectored — Custom Lengths

HFBR-3100 Dual Channel Connectored — Custom Lengths

Note: Option 001 specifies HFBR-4000 HP connector and Option 002 specifies SMA connectors.

HFBR-3001 Single Channel Connectored — 10 metres (HFBR-4000 connectors)

HFBR-3021 Single Channel Connectored — 10 metres (SMA connectors)

HFBR-3200 Unconnectored Single Channel — Custom Lengths

HFBR-3300 Unconnectored Dual Channel — Custom Lengths

High Speed Operation

Rise and fall times can be improved by using a pre-bias current and "speed-up" capacitor. A 1 mA pre-bias current will significantly reduce the junction capacitance and will couple less than –34 dBm of optical power into the fiber cable. The TTL compatible circuit in Figure 7 using a speed-up capacitor will provide typical rise and fall times of 10 ns.

$$I_{PEAK} = 100\ \text{mA} = \frac{V_{CC} - V_F}{34.9\Omega}$$

$$I_{AVG} = 78\ \text{mA} = \frac{V_{CC} - V_F}{34.9 + 10\Omega}$$

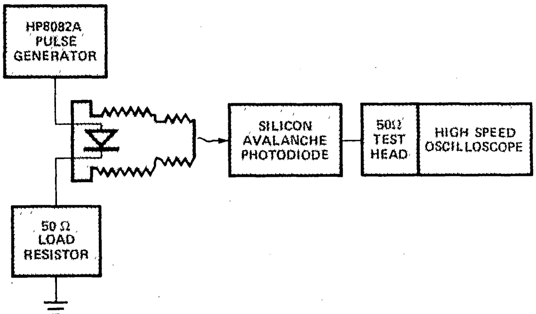


Figure 6. Test Circuit for Measuring t_r, t_f

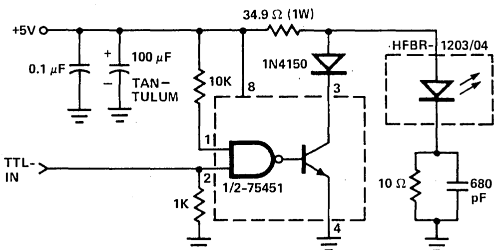


Figure 7. High Speed TTL Circuit

Link Design

With transmitter performance specified as power in dBm into a fiber of particular properties (core size, NA, and index profile), and receiver performance given in terms of the power in dBm radiated from the same kind of fiber, then the link design equation is simply:

(1) $P_T - \ell \cdot \alpha_O = P_R$

where

P_T = transmitter power into fiber (dBm)
ℓ = fiber (cable) length (km)
α_O = fiber attenuation (dB/km)
P_R = receiver power, from fiber, (dBm)

For transmitter input current in the range from 10 to 100 mA, the power varies approximately linearly:

(2) $P_T = P_O + 10 \log (I/I_O)$

where

P_O = transmitter power specification (dBm) at I_O
I_O = specified transmitter current (100 mA)
I = selected transmitter current (mA)

To allow for the dynamic range limits of proper receiver performance, it is necessary that a link with maximum transmitter power and minimum attenuation does not OVERDRIVE the receiver and that minimum transmitter power with maximum attenuation does not UNDERDRIVE it. These limits can be expressed in a combination of the two equations above:

(3) $P_{O\,MAX} + 10 \log (I_{MAX}/I_O) - \ell \cdot \alpha_{OMIN} < P_{R\,MAX}$

(4) $P_{O\,MIN} + 10 \log (I_{MIN}/I_O) - \ell \cdot \alpha_{OMAX} > P_{R\,MIN}$

where

$P_{O\,MAX}$, $P_{O\,MIN}$ = max., min. specified power from transmitter (dBm) at $I = I_O$
I_{MAX}, I_{MIN} = max., min. selected transmitter operating current (mA)
$P_{R\,MAX}$, $P_{R\,MIN}$ = max., min. specified power at receiver (dBm)
α_{OMAX}, α_{OMIN} = max., min. attenuation (dB/km)

A more useful form of these equations comes from solving them for the current ratio, expressed in dB:

(5) $10 \log (I_{MAX}/I_O) < P_{R\,MAX} - P_{O\,MAX} + \ell \cdot \alpha_{OMIN}$

(6) $10 \log (I_{MIN}/I_O) > P_{R\,MIN} - P_{O\,MIN} + \ell \cdot \alpha_{OMAX}$

These are plotted in Figure 8 as the OVERDRIVE LINE, and UNDERDRIVE LINE, respectively for the following components:

HFBR-1203/4 Transmitter $-11.2 < P_T < -4$ dBm
HFBR-2203/4 Receiver (25 MHz) $-28.5 < P_R < -12.6$ dBm
HFBR-2203/4 Receiver (2.5 MHz) $-35.5 < P_R < -12.6$ dBm
HFBR-3000 Series Fiber Cable $4 < \alpha_O < 8$ dB/km

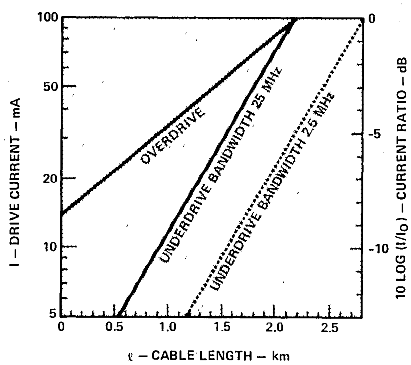


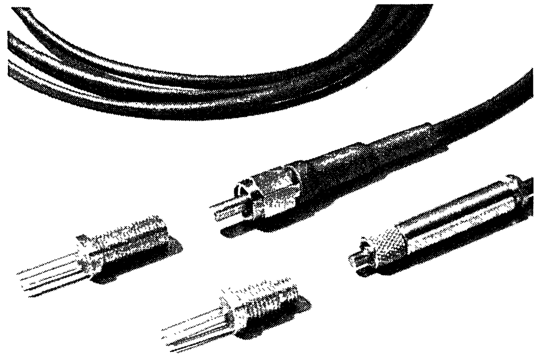
Figure 8. Link Design Limits.

These design equations take account only of the power loss due to attenuation. The specifications for the receiver and transmitter include loss effects in end connectors. If the system has other fixed losses, such as from directional couplers or additional in-line connectors, the effect is to shift both OVERDRIVE and UNDERDRIVE lines upward by the amount of the additional loss ratio.

40 MBd MINIATURE FIBER OPTIC RECEIVERS

HFBR-2203
HFBR-2204

TECHNICAL DATA JANUARY 1986



Features

- DATA RATES UP TO 40 MBd
- HIGH OPTICAL COUPLING EFFICIENCY
- RUGGED, MINIATURE METAL PACKAGE
- COMPATIBLE WITH HP OR SMA STYLE CONNECTORS
- VERSATILE ANALOG RECEIVER OUTPUT
- 25 MHz ANALOG BANDWIDTH

Applications

- DATA ACQUISITION AND PROCESS CONTROL
- SECURE DATA COMMUNICATION
- EMC REGULATED SYSTEMS (FCC/VDE)
- EXPLOSION PROOF SYSTEMS
- WEIGHT SENSITIVE SYSTEMS (e.g., AVIONICS, MOBILE STATIONS)
- VIDEO TRANSMISSION

Description

The HFBR-2203/04 Receiver is capable of data rates up to 40 MBd at distances greater than 1 km when used with HFBR-3000 series cable and HFBR-1201/2/3/4 Transmitters. The HFBR-2203/04 Receivers contain a discrete PIN photodiode and preamplifier IC.

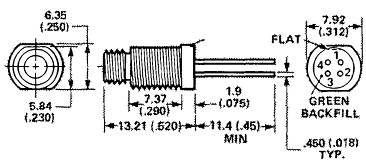
The signal from this simple analog receiver can be optimized for a variety of transmission requirements. For example the HFBR-0221/02/03/04 transceivers add low-cost external components to achieve logic compatible signal levels optimized for various data formats and data rates.

Each of these fiber optic components uses the same rugged, lensed, miniature package. This package assures a consistent, efficient optical coupling between the active devices and the optical fiber.

The HFBR-2203 Receiver is compatible with the HFBR-4000 Connector and HFBR-3000 series, Option 001 connectored cable. The HFBR-2204 Receiver is compatible with SMA style connectors, types A and B (see Figure 11), and HFBR-3000 series, Option 002 connectored cable. HFBR-3000 series cable can be ordered with or without connectors. The HFBR-0100 connector assembly kit is available if field installation of HFBR-4000 connectors is desired.

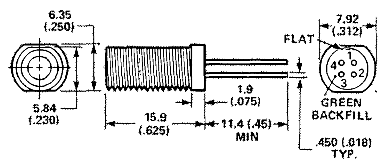
Mechanical Dimensions

HFBR-2203 RECEIVER



PIN	FUNCTION
1	CASE
2	SIGNAL
3	COMMON
4	V_{CC}

HFBR-2204 RECEIVER



PIN	FUNCTION
1	CASE
2	SIGNAL
3	COMMON
4	V_{CC}

DIMENSIONS IN MILLIMETRES (INCHES)
UNLESS OTHERWISE SPECIFIED, THE TOLERANCES ARE:
.X ± .51 mm (.XX ± .02 IN)
.XX ± .13 mm (.XXX ± .005 IN)

Electrical Description

The HFBR-2203/04 Fiber Optic Receiver contains a PIN photodiode and low noise transimpedance pre-amplifier hybrid circuit with an inverting output (see note 10). The HFBR-2203/04 receives an optical signal and converts it to an analog voltage. The output is a buffered emitter-follower. Because the signal amplitude from the HFBR-2203/04 Receiver is much larger than from a simple PIN photodiode, it is less susceptible to EMI, especially at high signal rates.

The frequency response is typically dc to 25 MHz. Although the HFBR-2203/04 is an analog receiver, it is easily made compatible with digital systems (see HFBR-0221/2/3/4 Transceiver data sheet). Separate case and signal ground leads are provided for maximum design flexibility.

It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from Pin 4 (V_{CC}) to Pin 3 (circuit common) of the receiver. Total lead length between both ends of the capacitor and the pins should be less than 20 mm.

Mechanical Description

The HFBR-2203/04 Fiber Optic Receiver is housed in a miniature package intended for use with HFBR-3000 Fiber Optic Cable/Connector Assemblies. This package has important performance advantages:

1. Precision mechanical design and assembly procedures assure the user of consistent high efficiency optical coupling.
2. The lens is suspended to avoid contact with the active devices, thereby assuring improved reliability.
3. The versatile miniature package is easy to mount. This low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking.

   A complete mounting hardware package is available for horizontal PCB applications, including a snap-on metal shield for harsh EMI/ESD environments.

   Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; Methanol or Freon on a cotton swab also works well.

   Note:
   When installing connectored cable on the optical port, do not use excessive force to tighten the nut. Finger tightening is sufficient to ensure connectoring integrity, while use of a wrench may cause damage to the connector or the optics.

System Design Considerations

For additional information, see the product data sheet for the HFBR-0221/2/3/4 Fiber Optic Transceivers.

OPTICAL POWER BUDGETING

The HFBR-2203/04 Fiber Optic Receivers when used with the HFBR-1201/02 Fiber Optic Transmitters can be operated at a signalling rate of more than 40 MBd over a distance greater than 1000 metres (assuming 8 dB/km cable attenuation). For shorter transmission distances, power consumption can be reduced by decreasing Transmitter drive current. At a lower data rate, the transmission distance may be increased by applying bandwidth-filtering at the

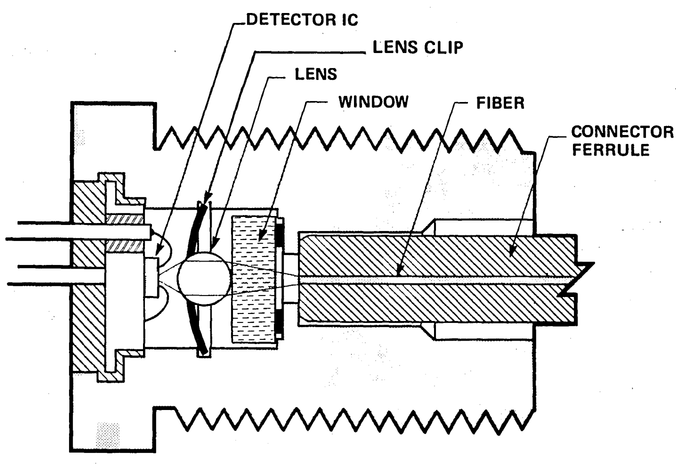


Figure 1. Cross Sectional View

FIBER OPTICS

output of the HFBR-2203/04 Receiver; since noise is reduced as the square root of the bandwidth, the sensitivity of the circuit is proportionately improved provided these two conditions are met:

a. input-referred noise of the follow on circuit is well below the filtered noise of the Receiver
b. logic comparator threshold is reduced in the same proportion as the noise reduction

As an example, consider a link with a maximum data rate of 10 MBd (e.g., 5 Mb/s Manchester); this requires a 3 dB bandwidth of only 5 MHz. For this example, the input-referred rms noise voltage of the follow-on circuit is 0.03 mV. The equivalent optical noise power of the complete receiver (P_{NO}) is given by:

$$P_{NO} = [(V_{NO})^2 (B/B_O) + (V_{NI})^2]^{0.5} / R_P$$

V_{NO} = rms output noise voltage of the HFBR-2203/04 with no bandwidth filtering
V_{NI} = input-referred rms noise voltage of the follow-on circuit
B = filtered 3 dB bandwidth
B_O = Unfiltered 3dB bandwidth of the HFBR-2203/04 (25 MHz)
R_P = optical-to-electrical responsivity (mV/μW) of the HFBR-2203/04

Note that noise adds in an rms fashion, and that the square of the rms noise voltage of the HFBR-2203/04 is reduced by the bandwidth ratio, B/Bo.

From the receiver data (Electrical/Optical Characteristics) taking worst-case values, and applying NO bandwidth filtering (B/Bo = 1):

$$P_{NO} = \frac{[(0.43)^2+(0.03)^2]^{0.5}\ \text{mV}}{4.6\ \text{mV}/\mu\text{W}} = 0.094\,\mu\text{W or } -40.3\ \text{dBm}$$

To ensure a bit error rate less than 10^{-9} requires the signal power to be 12 times larger (+11 dB) than the rms noise as referred to the Receiver input. The minimum Receiver input power is then:

$$P_{RMIN} = P_{NO} + 11\ \text{dB} = -29.3\ \text{dBm}$$

With the application of a 5 MHz low-pass filter, the bandwidth ratio becomes:

$$B/B_O = 5\ \text{MHz}/25\ \text{MHz} = 0.2$$

Note that 25 MHz should be used for the total noise bandwidth of the HFBR-2203/04. Inserting this value of the bandwidth ratio in the expressions for P_{NO} and P_{RMIN} above yields the results:

$$P_{NO} = 0.042\ \mu\text{W or } -43.8\ \text{dBm and } P_{RMIN} = -32.8\ \text{dBm}$$

Given the HFBR-1201/2 Transmitter optical power P_T = −18 dBm at I_F = 40 mA, and allowing a 3 dB margin, a minimum optical power budget of 11.8 dB is obtained:

$$|-18\ \text{dBm} -3\ \text{dB} -(-32.8\ \text{dBm})| = 11.8\ \text{dB}$$

Using 8 dB/km optical fiber, this translates into a minimum link length of 1475 metres (typical link power budget for this configuration is approximately 17.2 dB or 3130 metres with 5.5 dB/km fiber).

BANDWIDTH

The bandwidth of the HFBR-2203/04 is typically 25 MHz. Over the entire temperature range of -40° C to +85° C, the rise and fall times vary in an approximately linear fashion with temperature. Under worst case conditions, t_r and t_f may reach a maximum of 26 ns, which translates to a 3 dB bandwidth of:

$$f_{3dB} \simeq \frac{350}{t_r} = \frac{350}{26\ \text{ns}} = 13.5\ \text{MHz}$$

The receiver response is essentially that of a single-pole system, rolling off at 6 dB/octave. In order for the receiver to operate up to 40 MBd even though its worst case 3 dB bandwidth is 13.5 MHz, the received optical power must be increased by 3 dB to compensate for the restricted receiver transmission bandwidth.

PRINTED CIRCUIT BOARD LAYOUT

When operating at data rates above 10 MBd, standard PC board precautions should be taken. Lead lengths greater than 20 mm should be avoided whenever possible and a ground plane should be used. Although transmission line techniques are not required, wire wrap and plug boards are not recommended.

OPERATION WITH HEWLETT-PACKARD TRANSMITTERS

Hewlett-Packard offers two transmitters compatible with the HFBR-2203/4. Link performance with each transmitter is shown below for 25° C operation with HFBR-3000 series glass fiber cable. See product data sheets for further information.

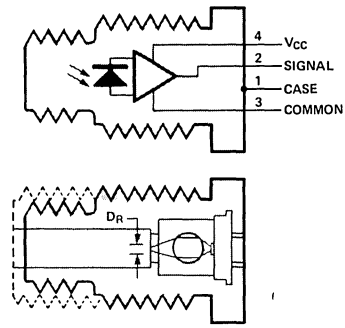
	HFBR-1201/2 -17 dBm Coupled Optical Power	**HFBR-1203/4 -9.8 dBm Coupled Optical Power**
HFBR-2203/4 -27 dBm Sensitivity	1200 m 40 MBd	2100 m 40 MBd
HFBR-2203/4 -32 dBm Sensitivity	1800 M 10 MBd	2800 M 10 MBd

HFBR-2203/2204 RECEIVER

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	-40	85	°C	Note 9
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Case Voltage		V_{CASE}		25	V	
Signal Pin Voltage		V_{SIGNAL}	-0.5	1	V	
Supply Voltage		V_{CC}	-0.5	7.0	V	

HFBR-2203/2204 RECEIVER



Electrical/Optical Characteristics

-40° C to +85° C; $4.75 \le V_{CC} \le 5.25$; $R_{LOAD} = 511\Omega$ unless otherwise specified

Parameter	Symbol	Min.	Typ[4]	Max.	Unit	Conditions	Reference
Responsivitity	R_P	5.1	7	10.9	mV/μW	$T_A = 25°C$ at 820 nm	Note 10 Figure 3
		4.6		12.3	mV/μW	$-40 \le T_A \le +85°C$	
RMS Output Noise Voltage	V_{NO}		.30	.36	mV	$T_A = 25°C$, $P_{IN} = 0\mu W$	Figures 4, 7
				.43	mV	$-40 \le T_A \le 85°C$, $P_{IN} = 0\ \mu W$	
Input Power	P_R			-12.6	dBm	$T_A = 25°C$	Note 2
				55	μW		
				-14	dBm	$-40 \le T_A \le 85°C$	
				40	μW		
Output Impedance	Z_O		20		Ω	Test Frequency = 20 MHz	
DC Output Voltage	V_{odc}		.7		V	$P_{IN} = 0\ \mu w$	
Power Supply Current	I_{CC}		3.4	6.0	mA	$R_{LOAD} = \infty$	
Equivalent N.A.	NA		.35				
Equivalent Diameter	D_R		250		μm		Note 3
Equivalent Optical Noise Input Power	P_N		-43.7	-40.3	dBm		
			.042	.094	μW		

Dynamic Characteristics

-40° C to +85° C; $4.75 \le V_{CC} \le 5.25$; $R_{LOAD} = 511\Omega$, $C_{LOAD} = 13$ pF unless otherwise specified

Parameter	Symbol	Min.	Typ.[7]	Max.	Units	Conditions	Reference
Rise/Fall Time, 10% to 90%	t_r, t_f		14	19.5	ns	$T_A = 25°C$ $P_{IN} = 10\ \mu W$ Peak	Note 5
				26	ns	$-40 \le T_A \le 85°C$	Figures 8, 9
Pulse Width Distortion	$t_{phl} - t_{plh}$			2	ns	$P_{IN} = 40\ \mu W$ Peak	Figure 9
Overshoot			4		%	$T_A = 25°C$	Note 6 Figures 8, 9
Bandwidth			25		MHz		
Power Supply Rejection Ratio (Referred to Output)	PSRR		50		dB	at 2 MHz	Note 7 Figures 5, 6

Notes:
1. 2.0 mm from where leads enter case.
2. If Pin < 40 μW, then pulse width distortion may increase. At Pin = 80 μW and $T_A = 80°C$, some units have exhibited as much as 100 ns pulse width distortion.

Notes (cont.):

3. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
4. Typical specifications are for operation at $T_A = 25°C$ and $V_{CC} = 5.0V$.
5. Input optical signal is assumed to have 10% — 90% rise and fall times of less than 6 ns.
6. Percent overshoot is defined as:

$$\frac{V_{PK} - V_{100\%}}{V_{100\%}} \times 100\% \quad \text{See Figure 16.}$$

7. Output referred P.S.R.R. is defined as

$$20 \log \left(\frac{V_{POWER\ SUPPLY\ RIPPLE}}{V_{OUT\ RIPPLE}}\right)$$

8. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 4 (V_{CC}) to pin 3 (circuit common) of the receiver. Total lead length between both ends of the capacitor and the pins should be less than 20 mm.
9. HFBR-3000 series Fiber Cable is specified at a narrower temperature range, -20° C to 85° C.
10. $V_{OUT} = V_{ODC} - (R_P \times P_{IN})$.

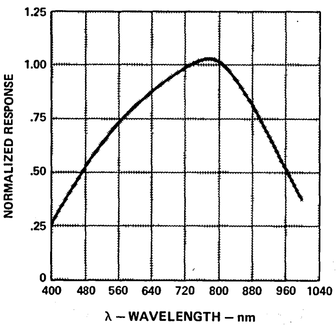


Figure 3. Receiver Spectral Response Normalized to 820 nm

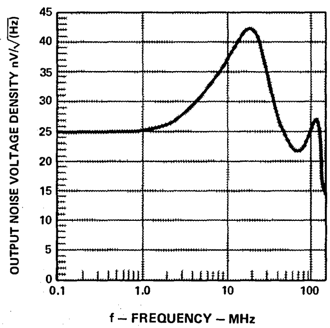


Figure 4. Receiver Noise Spectral Density

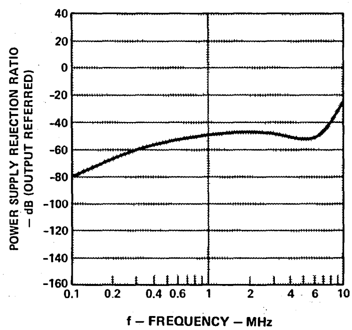


Figure 5. Receiver Power Supply Rej. vs. Freq.

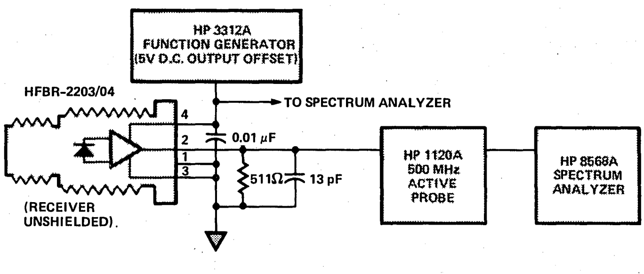


Figure 6. Power Supply Rejection Test Circuit

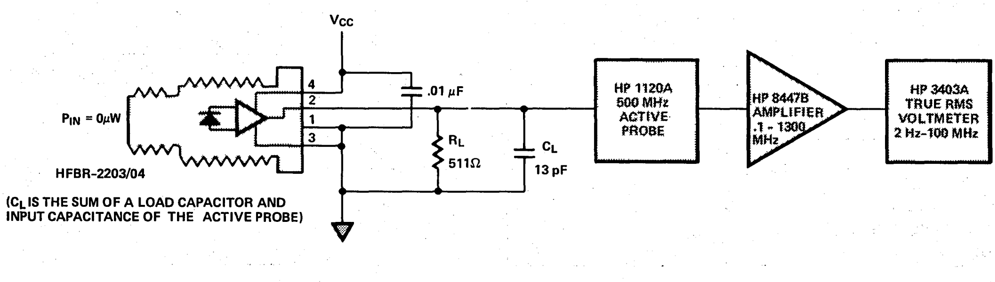


Figure 7. RMS Output Noise Voltage Test Circuit

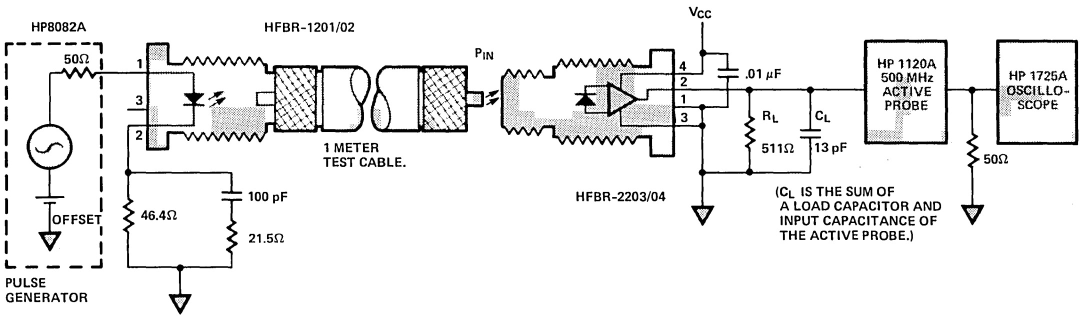


Figure 8. Rise and Fall Time Test Circuit

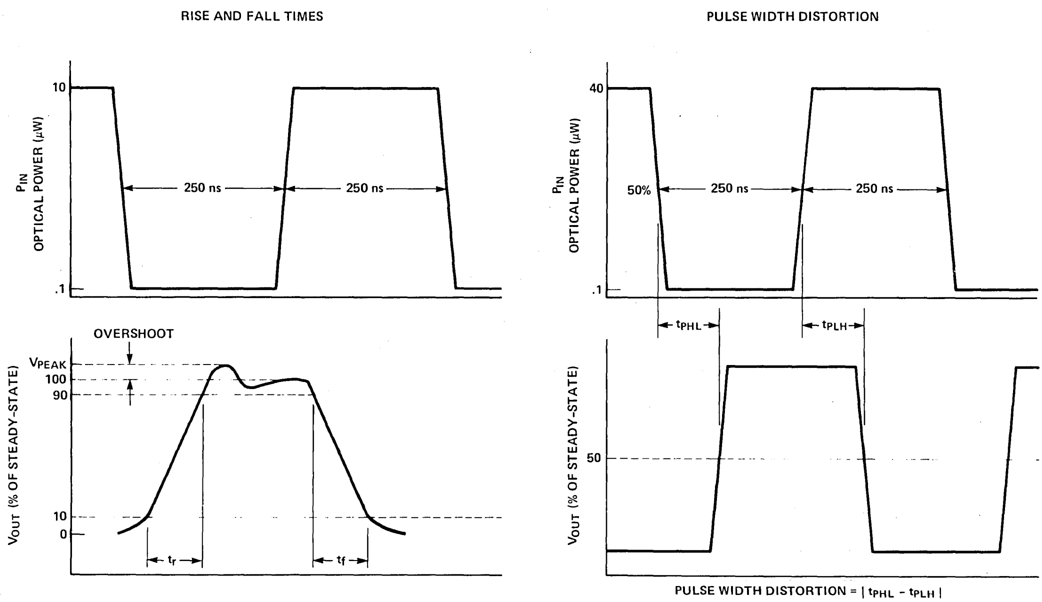
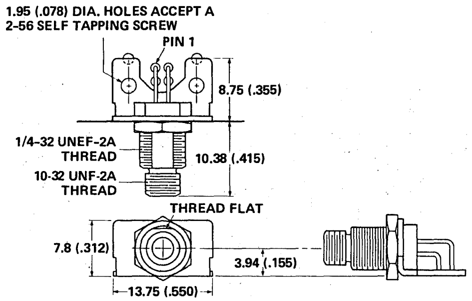
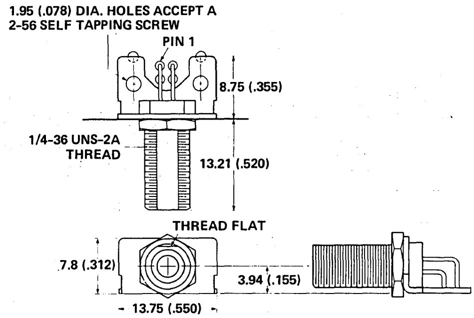


Figure 9. Waveform Timing Definitions

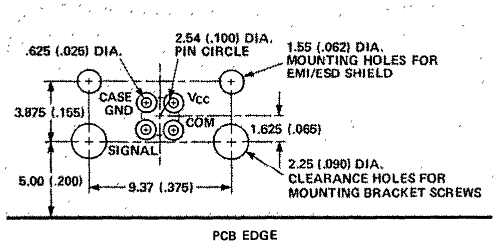
HFBR-2203 RECEIVER



HFBR-2204 RECEIVER



RECEIVER PCB LAYOUT DIMENSIONS

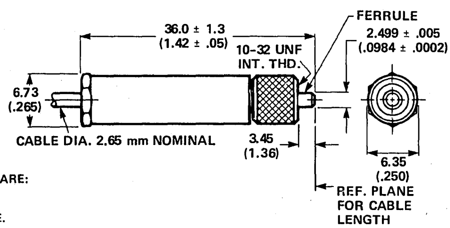


DIMENSIONS IN MILLIMETRES (INCHES).

Figure 10. Mounting Dimensions

HEWLETT-PACKARD STYLE CONNECTOR (Used in HFBR-3000/3100, Option 001 Cable Assemblies).

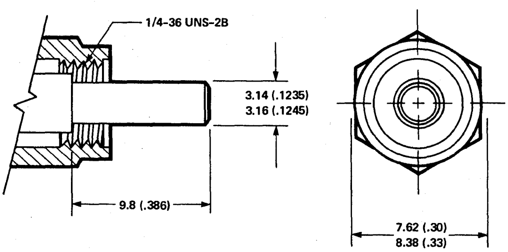
HFBR-4000 CONNECTOR



NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCES ARE:
   .X ± .51 mm, (.XX ± .02 in.)
   .XX ± .13 mm (.XXX ± .005 in.)
3. FIBER END IS LOCKED FLUSH WITH FERRULE FACE.

SMA STYLE CONNECTORS

TYPE A
(Used in HFBR-3000/3100, Option 002 Cable Assemblies).



TYPE B
(Not Available from Hewlett-Packard)

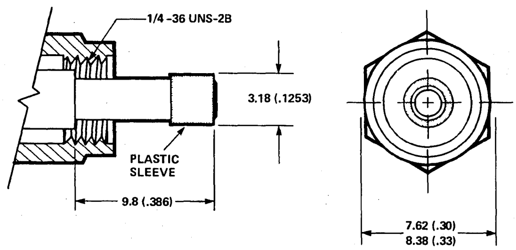


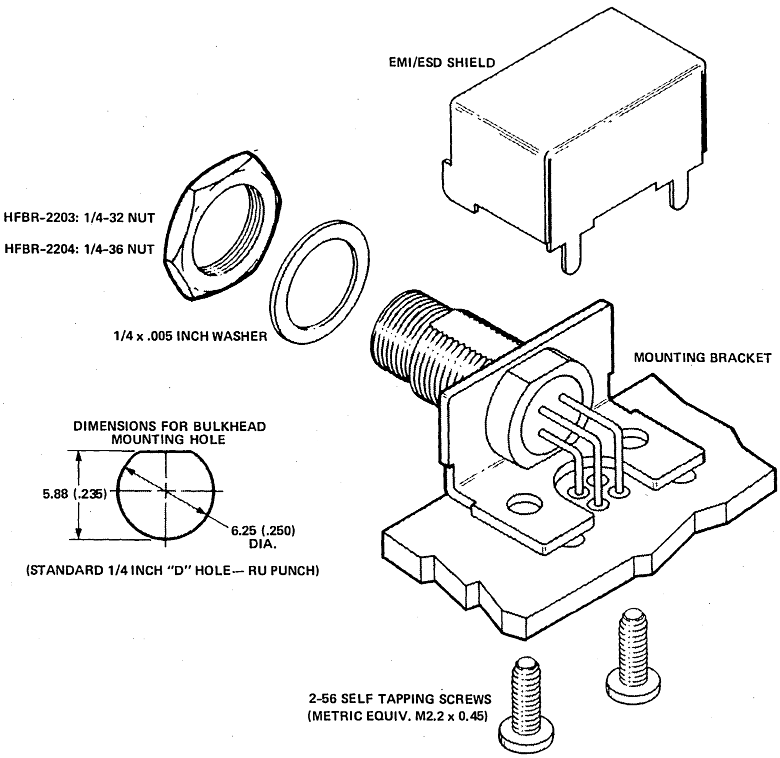
Figure 11. Fiber Optic Connector Styles

Horizontal PCB Mounting

Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

When bending the leads, avoid sharp bends right where the lead enters the backfill. Use needle nose pliers to support the leads at the base of the package and bend the leads as desired.

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.



MOUNTING HARDWARE: HFBR-4201 (HFBR-2203)
1 EMI/ESD SHIELD
1 1/4-32 NUT
1 1/4 x .005 INCH WASHER
2 2-56 SELF TAPPING SCREWS
1 MOUNTING BRACKET

MOUNTING HARDWARE: HFBR-4202 (HFBR-2204)
1 EMI/ESD SHIELD
1 1/4-36 NUT
1 1/4 x .005 INCH WASHER
2 2-56 SELF TAPPING SCREWS
1 MOUNTING BRACKET

Ordering Guide

Transmitter:	HFBR-1201 (HP Connector Compatible) HFBR-1202 (SMA Connector Compatible) HFBR-1203 (HP Connector Compatible) HFBR-1204 (SMA Connector Compatible)
Receiver:	HFBR-2203 (HP Connector Compatible) HFBR-2204 (SMA Connector Compatible)
Mounting Hardware:	HFBR-4201 (HP Connector Compatible) HFBR-4202 (SMA Connector Compatible)

Fiber Optic Cable — see data sheets

HFBR-3000 Single Channel Connectored — Custom Lengths

HFBR-3100 Dual Channel Connectored — Custom Lengths

Note: Option 001 specifies HFBR-4000 connector and Option 002 specifies SMA connectors.

HFBR-3001 Single Channel Connectored — 10 metres (HFBR-4000 connectors)

HFBR-3021 Single Channel Connectored — 10 metres (SMA connectors)

HFBR-3200 Unconnectored Single Channel — Custom Lengths

HFBR-3300 Unconnectored Dual Channel — Custom Lengths

HEWLETT PACKARD

HIGH SPEED FIBER OPTIC TRANSCEIVERS

HFBR-0221
HFBR-0222
HFBR-0223
HFBR-0224

TECHNICAL DATA JANUARY 1986

Features

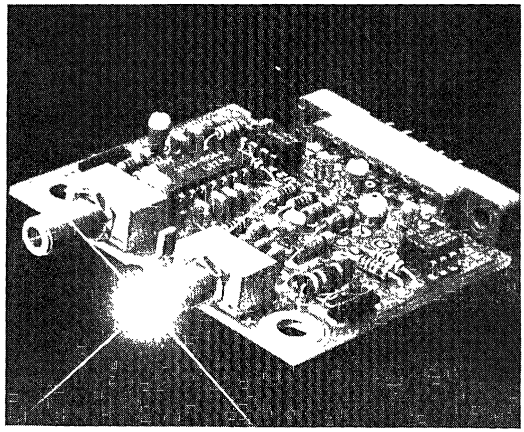
- GUARANTEED LINK PERFORMANCE
- DISTANCE/DATA RATE TRADEOFF ALLOWS INCREASED OPTICAL POWER BUDGET AT LOWER DATA RATES
- TTL I/O
- 20 MBAUD DATA RATE (CAN BE MODIFIED FOR 40 MBd OPERATION)
- COMPATIBLE WITH MOST DATA FORMATS
- AVAILABLE WITH HP OR SMA STYLE CONNECTORS
- LINK LENGTHS TYPICALLY GREATER THAN 1 km AT 20 MBd

Applications

- DESIGN AID FOR HIGH SPEED FIBER OPTIC COMPONENTS
- DATA ACQUISITION AND PROCESS CONTROL
- SECURE DATA COMMUNICATION
- EMC REGULATED SYSTEMS (FCC/VDE)
- EXPLOSION PROOF SYSTEMS
- WEIGHT SENSITIVE SYSTEMS (e.g. AVIONICS, MOBILE STATIONS)

Description

The HFBR-0221/2/3/4 High Speed Fiber Optic Transceivers are printed circuit board assemblies containing HFBR-1201/-1202 Transmitters, HFBR-2203/-2204 Receivers and support circuitry to provide TTL input and complementary TTL outputs. The performance of these transceivers at 20 MBd has been characterized over 0° C to 70° C and total link performance with HFBR-3000 Fiber Cable/Connector Assembly is guaranteed.

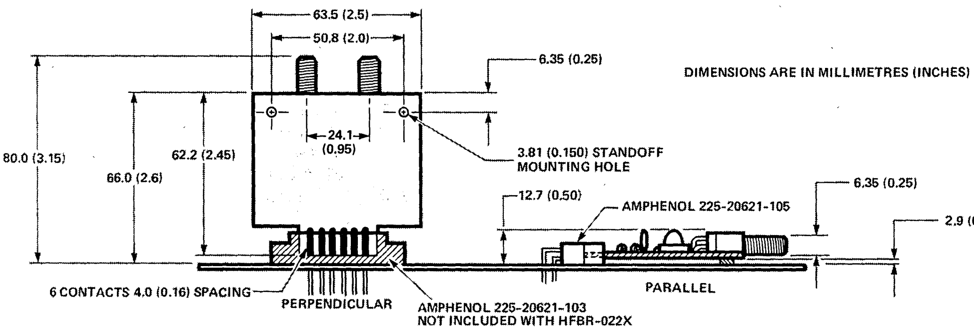


These transceivers are optimized for 20 MBd operation. However, the support circuitry on the printed circuit board can be optimized for other data rates. Recommendations for component values and anticipated performance for operation at 1 MBd, 5 MBd and 40 MBd are included in the "Application Information" section.

There are two transceiver designs (available with HP or SMA style connector ports) which accommodate various data formats. The HFBR-0221/0222 transceivers are optimized for data formats which have 50 percent duty factors such as Manchester and biphase. The HFBR-0223/-0224 transceivers are designed for arbitrary data formats including most NRZ schemes (see "Circuit Description" for details).

The transceivers can be mounted via an edge card connector, either parallel or perpendicular to a reference printed circuit board. A right angle edge card connector is included with each transceiver for parallel mounting.

Mechanical Dimensions



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Applied Voltage Data, $\overline{Data}$ $+V_{CC}$, Data In		−0.5	5.25	V
$-V_{CC}$		−6.5	+0.5	V
Storage Temperature[1]	T_S	−55	85	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	$+V_{CC}$	4.75	5.25	V
	$-V_{CC}$	−4.5	−6.5	V
Operating Temperature	T_A	0	70	°C
Duty Factor HFBR-0221/22	DF	33	67	%
HFBR-0223/24		5	95	%
Data Rate Range		0.01	20	MBd

Electrical/Optical Characteristics

(Recommended operating conditions for transceiver optimized for 20 MBd apply, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Optical Power Budget HFBR-0221/2	OPB	When used with HFBR-3000 Fiber Cable/Connectors, Data Rate = 20 MBd BER = 10^{-9}	9	15.5		dB
HFBR-0223/4			5	11		dB
Pulse Distortion HFBR-0221/2	$t_{PLH} - t_{PHL}$			7	12.5	ns
HFBR-0223/4				2	12.5	ns
Data Output Response Time[2]	t_r			7		ns
	t_f			5		ns
Transceiver Propagation Delay[3]	t_{PLH}, t_{PHL}			70		ns
Power Consumption $+V_{CC}$				750		mW
$-V_{CC}$				125		mW
Transmitter Output Optical Power Power coupled into HFBR-3000 Fiber Cable/ Connector Assembly[4] Data In is high, $T_A = 25°C$	P_T	Data In is high, $T_A = 25°C$	−18	−16.5		dBm
			15.8	22.4		μW
		$0 < T_A < 70°C$ Data in is high	−19			dBm
			12.6			μW
Power Coupled into Siecor 100/140 μm Fiber Cable or Equivalent[6]		Data In is High, $T_A = 25°C$		−18.5		dBm
Optical Rise and Fall Times	$t_{r,o}$ $t_{f,o}$	10% to 90%		10		ns
Receiver Optical Sensitivity HFBR-0221/2	P_R		−28	−32		dBm
			1.6	0.6		μW
HFBR-0223/4			−24	−27.5		dBm
			4	1.8		μW
TTL Gate Fanout					4	

WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe: however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

(See notes on page 6-40)

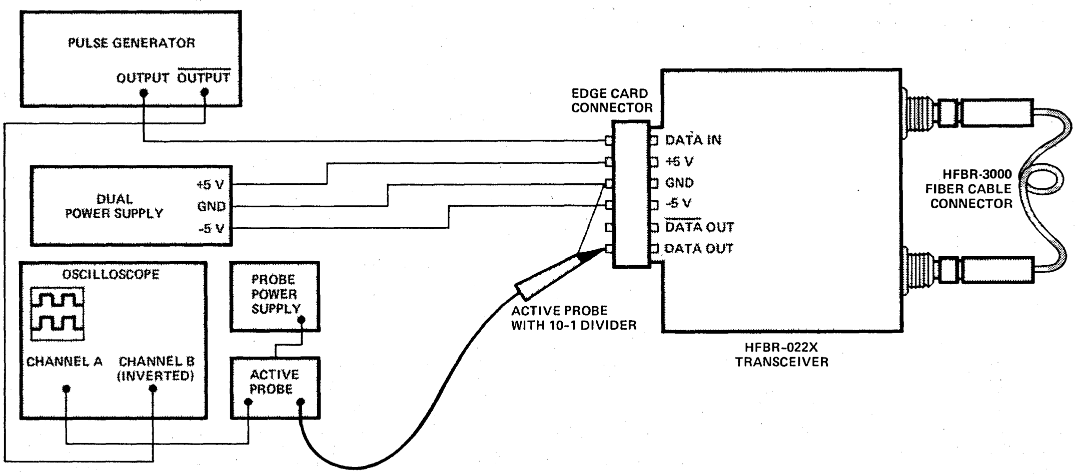
Test Set-Up

Equipment Needed

1. Dual power supply (HP 623613)
2. 100 MHz oscilloscope (HP 1725A)
3. Active oscilloscope probe and probe tip (HP 1120A/ 1122A)
4. 10:1 divider for oscilloscope probe (HP 10241A)
5. 50 MHz pulse generator (HP 8082A)
6. Miscellaneous cables and connectors

Procedure

1. Connect fiber cable and edge card conector to the transceiver board.
2. Adjust the power supply to +5 V and –5 V. Then connect to the transceiver board as shown below. Take care not to exceed the recommended operating voltage.
3. Adjust the pulse generator for TTL level square wave (+3 V) with a 5 nsec, edge transition time and then connect to the transceiver board.
4. Use the oscilloscope with the active probe and 10:1 divider to observe the input and output waveforms.



Notes:
1. The data out observed through the active probe exhibits overshoot at the rising edge. This overshoot will disappear if the output is loaded to drive a TTL input.
2. Oscilloscope inputs should be terminated into 50 ohms.
3. The active probe should be set on DC for observation of lower data rates. The offset on the active probe should be off.
4. The active probe is used to avoid reflection in the observed signal through impedance matching.
5. If necessary clean the optical port of the fiber connectors with Acetone before connecting them to the transceivers.

Ordering Information

	Connector Style	Data Format
HFBR-0221	HP	33 to 67% Duty Factor (For use with code schemes such as Manchester and Biphase)
HFBR-0222	SMA	
HFBR-0223	HP	5 to 95% Duty Factor (For use with code schemes such as NRZ and NRZI)
HFBR-0224	SMA	

Fiber Optic Cable (See Data Sheets)

HFBR-3000 Single Channel Connectored — Custom Lengths

HFBR-3100 Dual Channel Connectored — Custom Lengths

NOTE: Option 001 specifies HFBR-4000 (HP) connector and Option 002 specifies SMA style connectors.

HFBR-3001 Single Channel Connectored — 10 metres (HFBR-4000 connectors)

HFBR-3021 Single Channel Connectored — 10 metres (SMA connectors)

HFBR-3200 Unconnectored Single Channel — Custom Lengths

HFBR-3300 Unconnectored Dual Channel — Custom Lengths

Application Information

TRANSCEIVER CIRCUIT DESCRIPTION

There are separate transmitting and receiving circuits that function independently so data may be simultaneously sent and received without mutual interference.

Transmitting Circuit

On the transmitter side, the DATA IN terminal operates from TTL-level signals; the HFBR-1201/2 Transmitter is off ($P_T = 0$) with DATA IN low, and is on with DATA IN high. R_{12} holds the input low in the absence of anything connected. In this condition, the output transistor of U3 is on, and the current from R_2 is taken to ground through CR_1, making the voltage at the anode of the HFBR-1201/2 transmitter low enough to hold the LED off, yet allow it to be slightly forward biased (by the forward voltage on CR_1) so it can be turned on with little delay. With insignificant forward current in the LED, C_3 is discharged. When DATA IN is raised, the output transistor of U3 is turned off, allowing the current from R2 to enter the LED; there is an initial rush of current as C3 charges, thus peaking the LED turn-on. In steady state "on", LED current is limited by the sum of R_2 and R_3, but during turn-on current is limited by R_2 only, so the peak-to-dc current ratio is approximately $(R_2 + R_3)/R_2$. During turn-off, until C_3 is partly discharged, the voltage on C_3 will apply a small reverse voltage to the LED, thus peaking its turn-off as long as the voltage on C_3 remains higher than the voltage at the anode of CR_1.

Receiving Circuit

On the receiving side there is a similar relationship between the optical power and the TTL-level signals; that is, a rising input optical power excursion will normally cause a logic high DATA OUT.

Under steady-state conditions of optical input, both the positive and negative inputs of U1 are at ground potential, so the output of U1 is near zero and therefore capable of excursions either up or down in response to changes at its input. U2 is a comparator; when connected as shown it has positive feedback from DATA OUT when DATA OUT is high, and from $\overline{\text{DATA}}$ OUT when DATA OUT is low. This positive feedback makes it operate as a Schmitt circuit, the hysteresis thresholds being established by the voltage division ratios in R_{11}, R_9 when DATA OUT is high and in R_{10}, R_8 when DATA OUT is low.

Under dynamic conditions, a rise in optical input power causes the voltage at pin 2 of the HFBR-2203/-2204 to fall. This fall is ac-coupled by C_{11} to the input, pin 1, of U1, where it is amplified and converted to a balanced output signal, rising at pin 8 and falling at pin 7. The falling signal coupled by C_{13} to U2 will, if the amplitude exceeds the hysteresis threshold, cause U2 to latch a logic high at DATA OUT. Similarly, a drop in optical input power will cause U2 to latch a logic high at $\overline{\text{DATA}}$ OUT (low at DATA OUT).

After a change in optical input power, the U1 amplifier circuit may return to steady-state conditions, but U2 holds the logic state until an opposite excursion occurs unless there is a noise-voltage excursion that causes logic reversal. Consequently, the threshold set at U2 must be high enough that neither electromagnetic interference coupled from elsewhere on the circuit board, nor Receiver noise amplified through U1 can cause a false change. On the other hand, if the threshold is set too high, the Receiver would require inappropriately large changes in optical input power in order to make U2 change state properly.

Within the limits of its dynamic range, U1 operates linearly, so the threshold at U2 can be referred to the input of U1 as an equivalent threshold voltage (i.e., divided by the gain of U1). Similarly, the HFBR-2203/-2204 Receiver makes a linear conversion of optical input to voltage output (typically 7 mV per μW), so the U2 threshold can be referred to the optical input as an equivalent optical power level. Consequently, changes of either the gain of U1 or the threshold at U2 affect the threshold-equivalent input power.

Likewise, the rms noise voltage at the input of U1 can be referred to the optical input as noise-equivalent input power.

Sensitivity is defined relative to noise and threshold, as the optical input power excursion needed to obtain reliable operation. It can be improved by applying bandwidth filtering to reduce the noise amplitude. Since the HFBR-2203/-2204 Receiver is well shielded, its output noise is due only to shot and thermal noise, for which the amplitude varies as the square root of the bandwidth. Consequently, applying bandwidth filtering at the output of the Receiver reduces the noise in the rest of the circuit. How this is done and with what benefit is discussed in the section on "Sensitivity Improvement with Data Rate Reduction".

Bandwidth filtering is useless unless interference (EMI) is less than the filter-reduced noise. For this reason the impedances to ground at the inputs of U1 must be balanced, even though the input signal from the HFBR-2203/-2204 Receiver is single-ended. This is done by making R_5 the same value as R_6, and C_{11} the same as C_{12}. This makes the impedances balanced because the internal impedance of the Receiver's output is very low, and only low values of R_{13} are used for bandwidth filtering. Further neutralization of EMI is achieved by making the traces connecting to the inputs of U1 of approximately the same length and located as close together as possible.

DESIGN DIFFERENCES

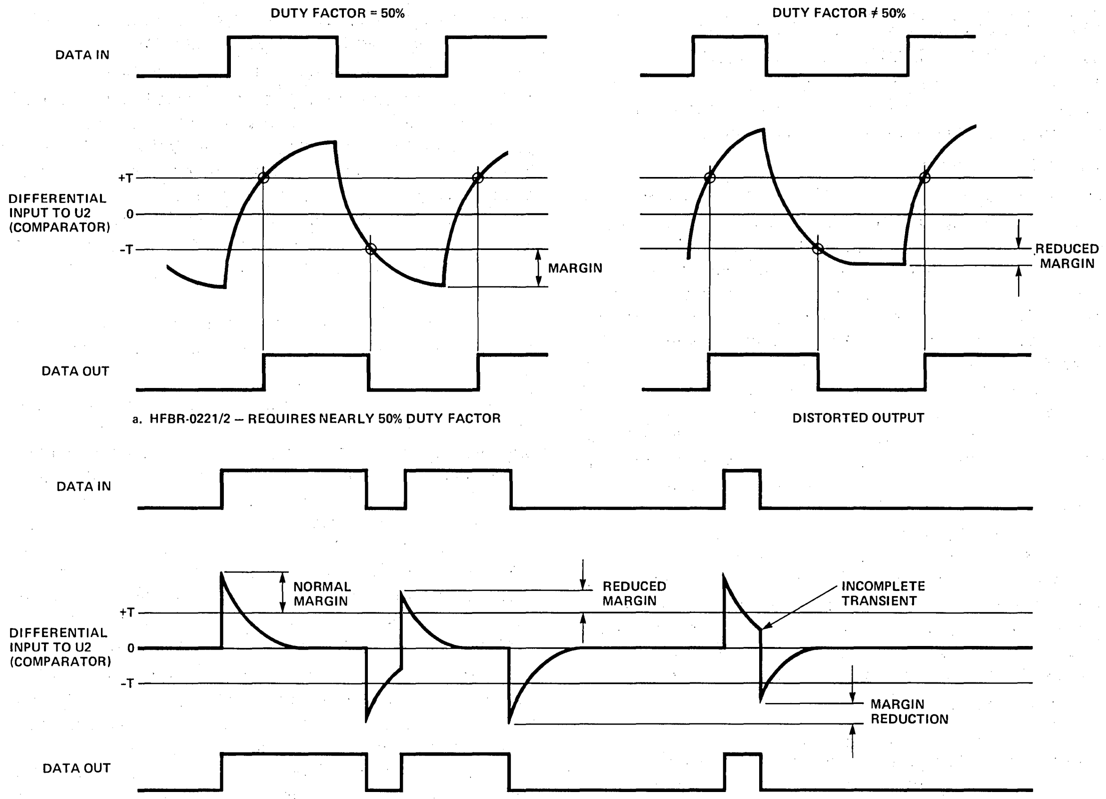
(HFBR-0221/-0222 and HFBR-0223/-0224)

The two versions of the Transceiver are designed with different data-handling objectives. The HFBR-0221/-0222 is intended for use with signals having a nearly 50% duty factor (such as Biphase or Manchester coded signals). The HFBR-0223/-0224 is intended for use as an edge detector (differentiator); with a very short time constant at C_{13} and C_{14}, the voltage levels are restored so rapidly that response time is virtually unaffected by the time differences between transitions in optical power, and for this reason it is capable of dealing with an arbitrary data format, such as NRZ and NRZI coded signals.

The difference in response modes is shown in Figure 1. It is clear that for the HFBR-0223/-0224 version, the edge timing is restricted only at the low end (minimum edge spacing or maximum signalling rate), where encroachment of one pulse might affect the next. For the HFBR-0221/-0222 version, a duty factor much more or much less than 50% would reduce the signal-to-noise ratio and also add propagation delay distortion.

Circuit adjustments to realize these differences in performance are mainly in the receiving side. Obviously, for the

FIBER OPTICS



a. HFBR-0221/2 – REQUIRES NEARLY 50% DUTY FACTOR

b. HFBR-0223/4 ARBITRARY EDGE TIMING UNDISTORTED BUT MAY HAVE REDUCED MARGIN FROM ENCROACHMENT OF NEXT TRANSITION.

Figure 1. Transceiver Response Waveforms

HFBR-0221/-0222 version it is necessary only to make the time constants of C_{13} and C_{14} long enough to couple a rectangular waveform to the inputs of U2, then set U1 for high gain and make the thresholds at U2 the value which provides a threshold-to-noise ratio greater than six. For the HFBR-0223/-0224 version the time constant of C_{13}, C_{14} must be less than a third of the shortest time desired between successive edges. The peak amplitude of pulses reaching U2 will be limited by the short time constant, a situation which can be remedied somewhat by lowering the gain of U1 (thus raising its bandwidth). This, in turn will require reduction of the threshold at U2.

There is a limit to how far the U2 threshold can be reduced without making it too vulnerable to EMI from the transmitting side. Because of these design constraints, the accommodation of arbitrary data format is obtained at the expense of sensitivity; that is, the HFBR-0223/-0224 version requires excursions of optical input power slightly higher than the excursions required by the HFBR-0221/-0222 version.

There is also a limit to how much gain adjustment is possible at U1. The maximum possible gain is 400 with $R_7 = 0$, so the gain increase that is available is approximately 6 dB (i.e. x4 because of the linear relationship to input power). Raising the gain by a factor of four permits sensitivity improvement by the same ratio if the noise bandwidth is reduced by sixteen times.

On the transmitting side the difference is very small. Both versions are operated at the same steady-state input current to the HFBR-1201/-1202 Transmitter LED, but they have different peak-to-dc current ratios. The purpose of the peaking is mainly to charge the LED and stray capacitances, so the 2:1 peak-to-dc current ratio in the HFBR-0221/-0222 version does not overstress the LED even though the 80 mA peak exceeds the 40 mA data sheet specification for that part. In the HFBR-0223/-0224 version, the peaking is slightly reduced to make sure the trailing edge of the peak will not be sensed by the receiving circuit as a negative data transition.

CIRCUIT LAYOUT CONSIDERATIONS

In so far as possible, given the limited space, the sensitive portions of the receiving circuit are spaced away from the parts of the transmitting circuit that have large excursions of current and voltage. Components that have no signal function (power supply decoupling elements) are placed in the space between the receiving and transmitting circuits to further enhance the shielding. Traces connecting to balanced inputs are made as nearly as possible the same length and closely spaced. Of course, a ground-plane style of PC board layout is used, and the EMI/ESD Shields in the HFBR-4201/-4202 Mounting Hardware are installed.

The transmitting side requires only a single +5 V power supply. Because of the large excursion currents in the

LED, shunt drive is used to minimize reaction on the power supply, which is shared by the receiving circuit. There is also decoupling by L_1, C_1, C_2 in addition to the +5 V supply input bypass, C_{15}, C_{16}.

On the receiving side, the −5 V supply has only the input bypass C_6, C_7 and single decoupling for U1 by L_2, C_8. Since the +5 V supply is shared with the transmitting circuit, considerable decoupling is needed to reduce interference. For U2 there is the first stage, L_4, C_4, C_5; for U1 a second stage, L_3, C_9; and for the HFBR-2203/-2204 Receiver a third stage, R_4, C_{10}.

SENSITIVITY IMPROVEMENT WITH DATA RATE REDUCTION

In a well-shielded receiver circuit, sensitivity is not limited by electro magnetic interference (EMI), but rather by random (Gaussian) noise for which the amplitude varies as the square root of the bandwidth. Sensitivity is defined as the amplitude of signal power needed to obtain sufficiently low Bit-Error Rate (BER), also known as Probability of Error, P_e. Obtaining $P_e < 10^{-9}$ in an ac-coupled circuit with hysteresis, such as used in HFBR-0221/-0222 and HFBR-0223/-0224, requires

a) $T > 6N$ to prevent false transition of output

b) $P > (T + 6N)$ to assure desired transition,

where

N = noise-equivalent input power (μW)
T = threshold-equivalent input power (μW)
P = excursion amplitude of input power (μW)

Noise reduction by filtering allows sensitivity improvement by reducing the noise amplitude. The filtered noise has amplitude, N in a bandwidth, B and the filtered/unfiltered noise ratio is:

$N/N_O = [B/B_O]^{0.5}$ as described above,

where

N_O = reference noise in a bandwidth, B_O

B_O = 25 MHz, the unfiltered 3-dB bandwidth of the HFBR-2203/4 Receiver

With noise reduced by the factor N/N_O, the threshold may be reduced by the same factor, and this allows the input excursion power to be reduced by N/N_O, while still obtaining $P_e < 10^{-9}$. If the noise is reduced by filtering, but no threshold adjustment is made, there is still some sensitivity improvement, but the improvement factor may be considerably less:

$P/P_O = N/N_O$ for threshold adjustment: $T/T_O = N/N_O$

$P/P_O = (1 + N/N_O)/2$ for no threshold adjustment

Bandwidth reduction is accomplished by lengthening the time constant at the output of the HFBR-2203/-2204 Receiver. The bandwidth, B, obtained by doing this is:

$B = 1/[(2 \pi)(Req)(C_{17})]$

where

Req = equivalent resistance of R_5 and R_{13} in parallel = $1/(1/R_5 + 1/R_{13})$

C_{17} = capacitance added in parallel with R_5

Threshold reduction can be done either by raising the gain of U1 or lowering the hysteresis set at U2, or by a combination. The simpler of the two is raising the gain of U1, since that requires changing the value of only one resistor, R_7; lowering R_7 raises the gain. The hysteresis setting at U2 should be kept balanced, so its reduction requires lowering R_8 and R_9 or raising R_{10} and R_{11}. It may even be necessary to change all four, since their values affect the time constant with C_{13} and C_{14}. The HFBR-0221/-0222 requires a long time constant, while the HFBR-0223/-0224 requires the time constant be kept short.

Bandwidth reduction will, or course, reduce the speed of response, and therefore the signalling rate will be reduced. A good rule for relating signalling rate to bandwidth is the ratio: two baud per hertz; that is, a 2 MHz bandwidth allows 4 MBd signalling.

A set of recommended component values and the anticipated result of such selection is listed in Table 1.

Table 1. Recommended Component Values and Typical Transceiver Performance (0° C to 70° C)

For HFBR-0221/-0222: (0.33 < Duty Factor < 0.67)

	1 MBd	5 MBd	20 MBd	30 MBd
R_{13} (ohms)	100	100	zero	zero
C_{17} (pF)	3300	680	100	100
R_7 (ohms)	zero	20	110	402
R_8 and R_9 (ohms)	1.0 k	1.0 k	1.0 k	1.0 k
R_{10} and R_{11} (ohms)	26.1 k	14.7 k	14.7 k	14.7 k

Minimum Power Budget (dB)

For Cabling Loss	17.5	14.0	9.0	6.0

Cable Length (metres)

@ 5.5 dB/km	3100	2500	1600	1000

Table 1. Recommended Component Values and Typical Transceiver Performance (0° C to 70° C) (cont.)

For HFBR-0223/-0224: (0.05 < Duty Factor < 0.95)

	1 MBd	5 MBd	20 MBd
R_{13} (ohms)	100	100	zero
C_{17} (pF)	3300	680	100
R_7 (ohms)	82.5	402	1620
C_{13} and C_{14} (pF)	1000	220	68
R_8 and R_9 (ohms)	0.215k	0.215k	0.215k
R_{10} and R_{11} (ohms)	8.25 k	8.25 k	8.25 k

Minimum Power Budget (dB)

For Cabling Loss	13.5	10.0	5.0

Cable Length (metres)

@ 5.5 dB/km	2400	1800	900

Schematic

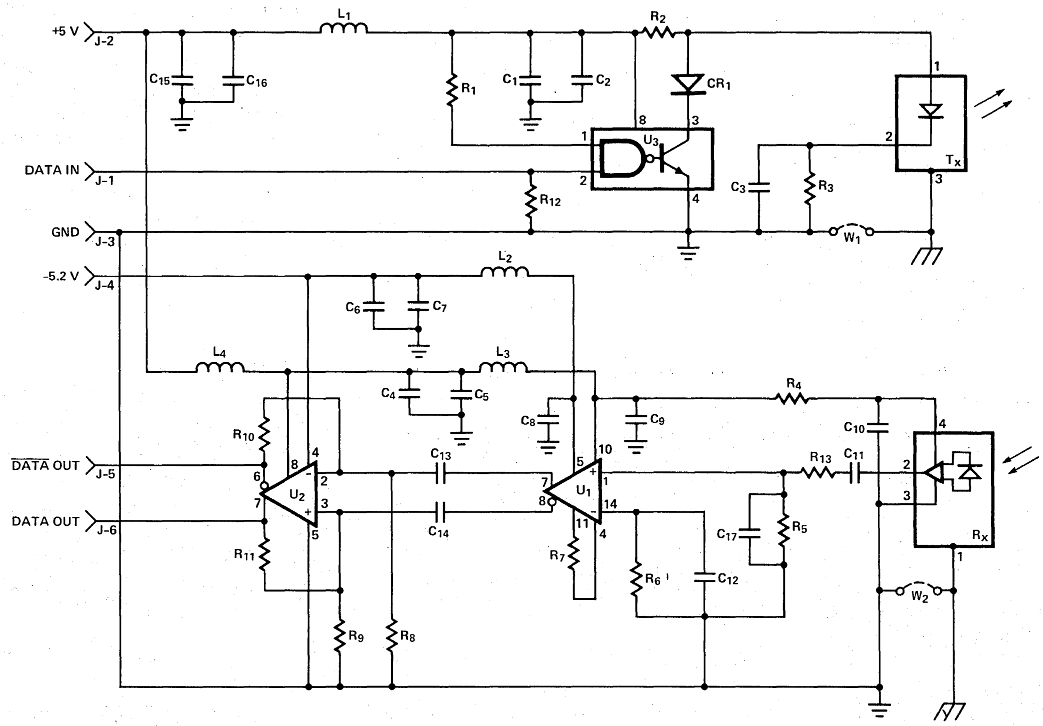


Figure 2.

COMPONENTS LIST

Common Components

Resistors	Part Description
R_1	10K Ω; 1%; 1/8W
R_4	51.1 Ω; 1%; 1/8W
$R_{5,6,12}$	1K Ω; 1% 1/8W
R_{13}	0 Ω (same as W_3)
Capacitors	
$C_{1,5,6,8,9,11,12,16}$	0.1 μF ceramic
C_2	47 μF tantalum
$C_{3,17}$	100 pF
$C_{4,7,15}$	4.7 μF tantalum
C_{10}	1 μF ceramic
Inductors	
$L_{1,2,3,4}$	2.7 μH ± 10%; Q = 40 @ 7.9 MHz dc res. = 0.55 ohms
Diode	
CR_1	1N3064
Integrated Circuits	
U1	LM-733C
U2	LM-360N
U3	MC-75451
Optional Jumpers	
$W_{1,2,3}$ ($W_3 = R_{13}$)	

PRODUCT SPECIFIC COMPONENTS

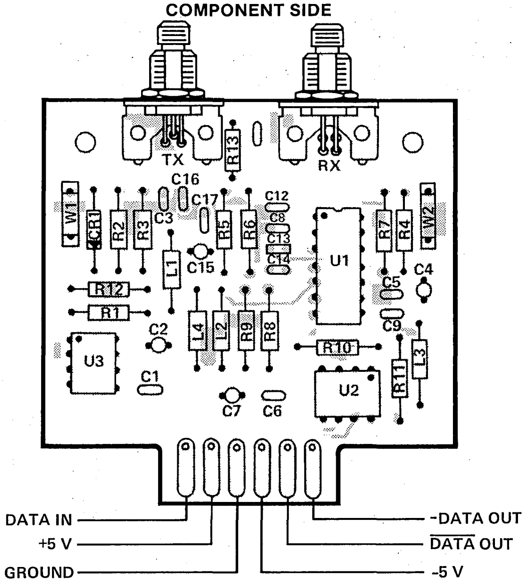
	HFBR-0221/-0222	HFBR-0223/-0224
Resistors		
R_2	43.0 Ω; 1%; 1/2W	51.0 Ω; 5%; 1/2W
R_3	42.2 Ω; 1%; 1/8W	31.6 Ω; 1%; 1/8W
R_7	110 Ω; 1%; 1/8W	1.62K Ω; 1%; 1/8W
$R_{8,9}$	1K Ω; 1%; 1/8W	215 Ω; 1%; 1/8W
$R_{10,11}$	14.7K Ω; 1%; 1/8W	8.25K Ω; 1%; 1/8W
Capacitors		
$C_{13,14}$	0.1 μF ceramic	68 pF

FIBER OPTIC COMPONENTS

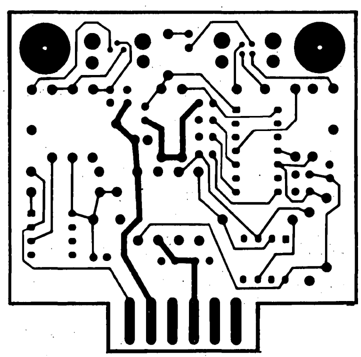
	HFBR-0221/-0223	HFBR-0222/-0224
T_X	HFBR-1201	HFBR-1202
R_X	HFBR-2203	HFBR-2204
Mounting Hardware	HFBR-4201	HFBR-4202

PRINTED CIRCUIT BOARD LAYOUT

COMPONENT SIDE



CIRCUIT SIDE



HEWLETT PACKARD

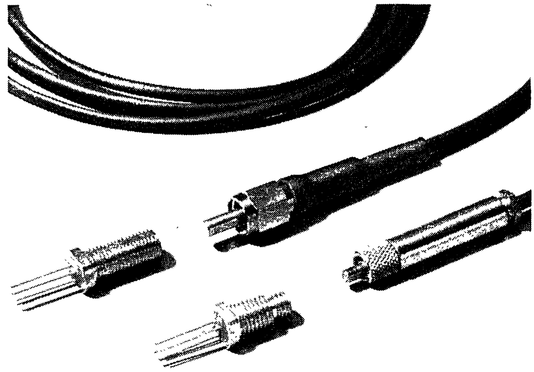
PIN PHOTODIODE FIBER OPTIC RECEIVER

HFBR-2207 HFBR-2208

TECHNICAL DATA JANUARY 1986

Features

- **GUARANTEED PERFORMANCE:**
  60 MHz Bandwidth at 5 V Reverse Bias
  Low Capacitance: Less than 1.6 pF
  0.29 A/W Minimum Responsivity
  Low Dark Current: Less than 300 pA
- **MATES DIRECTLY WITH HP AND SMA STYLE CONNECTORS**
- **RUGGED, ISOLATED MINIATURE METAL PACKAGE WITH FACTORY ALIGNED OPTICS**



Applications

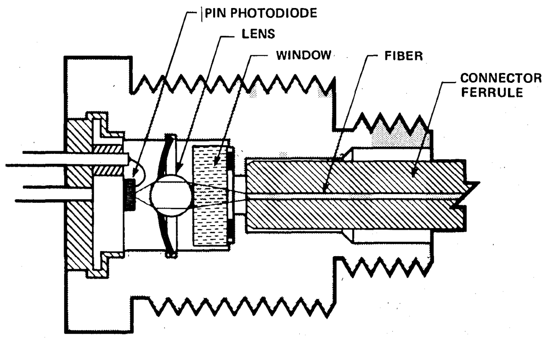
- **HIGH SPEED FIBER OPTIC LINKS**
- **WIDE BANDWIDTH ANALOG FIBER OPTIC LINKS**
- **HIGH SENSITIVITY, LOW BANDWIDTH LINKS**
- **OPTICAL POWER SENSOR**

Description

The HFBR-2207/8 Fiber Optic Receiver is a silicon PIN photodiode mounted in a rugged metal package. Well suited for high speed applications, the HFBR-2207/8 Fiber Optic Receiver has low capacitance and low noise. The high coupling efficiency of the miniature package provides a minimum of 0.29 A/W responsivity. Receiver responsivity includes the optical power lost in coupling light from the fiber onto the PIN photodiode as well as the responsivity of the PIN photodiode itself.

The HFBR-2207 mates with HFBR-4000 Connectors and the HFBR-2208 mates with SMA style connectors.

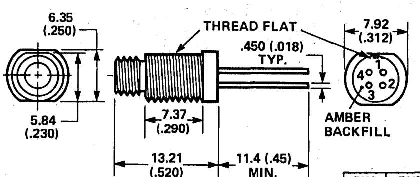
The HFBR-2207/8 is a member of the family of transmitters and receivers which use the miniature package. HP also offers connectored and unconnectored 100/140 μm fiber cable in simplex and duplex configurations.



Cross Sectional View

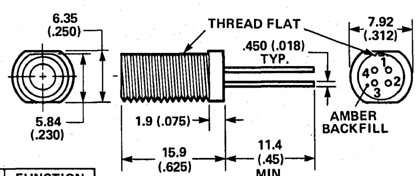
Mechanical Dimensions

HFBR-2207 HP CONNECTOR COMPATIBLE



PIN	FUNCTION
1	CASE
2	ANODE
3	CATHODE
4	NC

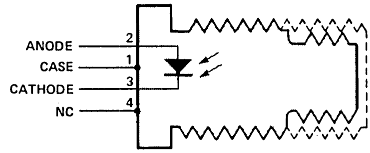
HFBR-2208 SMA STYLE COMPATIBLE

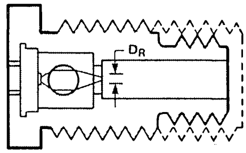


PIN	FUNCTION
1	CASE
2	ANODE
3	CATHODE
4	NC

DIMENSIONS IN MILLIMETRES (INCHES)

HFBR-2207/2208 PIN PHOTODIODE





Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–55	85	°C	
Operating Temperature		T_A	–55	85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Reverse Bias Voltage		V_R	–0.5	50	V	
Voltage, Case-to-Junction		V_C		100	V	Note 2

Electrical/Optical Characteristics

–55° C to +85° C; V_R = 5 V; P_R = –20 dBm at 820 nm unless otherwise specified. Typical data at T_A = 25° C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions		Reference
Effective Optical Port DC Responsivity	R_P	0.29	0.38	0.40	A/W	HFBR-3000/3100 100/140 μm Fiber N.A. = 0.28, g = 2		Fig. 1, 2, 3, 8
Dark Current	I_D		50	300	pA	T_A = 25° C	P_R = 0 μW V_R = 20 V	Fig. 4, 9
Noise Equivalent Power	NEP			3.4 x 10^{-14}	$\frac{W}{\sqrt{Hz}}$			Note 5
Total Capacitance	C_T		1.3	1.6	pF			Fig. 5
Series Resistance	R_S		5	10	Ω			
Equivalent N.A.	NA		0.4					
Equivalent Diameter	D_R		250		μm			Note 3
Case Isolation Resistance	R_{CASE}	1			MΩ	V_C = 100 V		Note 2, Fig. 9

Dynamic Characteristics

T_A = 25° C, R_{LOAD} = 50 Ω, P_R = –20 dBm at 820 nm unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Reference
3 dB Bandwidth	BW	60	100		MHz	V_R = 5 V	Fig. 6, 7
		150	250			V_R = 20 V	Fig. 10
Rise/Fall Time (10–90%)	t_r, t_f		3.5		ns	V_R = 5 V	Note 4
Relative Incremental Response	$\Delta R_P/R_P$		0.5		%	$P_R \leq -20$ dBm V_R = 5 V	Fig. 8 Note 6

Notes:

1. 2.0 mm from where leads enter case.
2. V_C (100 V) is applied simultaneously to Pin 2 and Pin 3 with respect to Pin 1.
3. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
4. Rise/Fall time is calculated from the equation:

$$t_r, t_f = \frac{350}{3 \text{ dB BW (MHz)}} \text{ns}$$

5. For (λ, f, Δf) = (820 nm, 100 Hz, 6 Hz) where f is the frequency for a spot noise measurement and Δf is the noise bandwidth, NEP is the optical flux required for unity signal/-noise ratio normalized for bandwidth.

Thus:

$$NEP = \frac{I_N/\sqrt{\Delta f}}{R_P}$$

where $I_N/\sqrt{\Delta f}$ is the bandwidth — normalized noise current computed from the shot noise formula:
$I_N/\sqrt{\Delta f} = \sqrt{2qI_D} = 17.9 \times 10^{-15} \sqrt{I_D}\ (A/\sqrt{Hz})$ where I_D is nA.

6. Relative incremental response is defined as:

$$\frac{\Delta R_P}{R_P} \times 100\% = \frac{R_{AC}(P_R) - R_{AC}(-25 \text{ dBm})}{R_{AC}(-25 \text{ dBm})} \times 100\%$$

where:
R_{AC} = Small signal AC (20 MHz, –30 dBm) response
P_R = DC optical power incident on port.

V_R = 5 V; P_R = −20 dBm at 820 nm; T_A = 25°C unless otherwise specified.

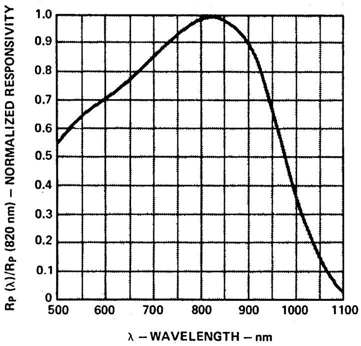


Figure 1. Normalized Responsivity vs. Wavelength

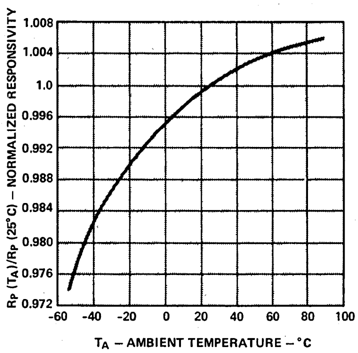


Figure 2. Normalized Responsivity vs. Ambient Temperature

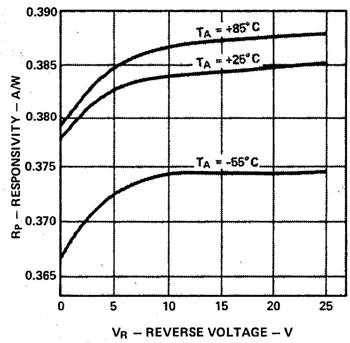


Figure 3. Responsivity vs. Reverse Voltage

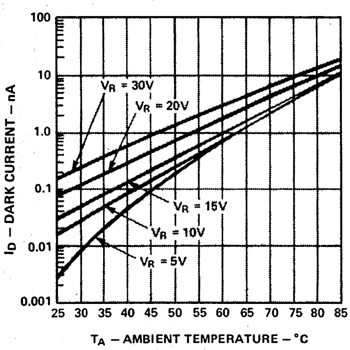


Figure 4. Dark Current vs. Ambient Temperature

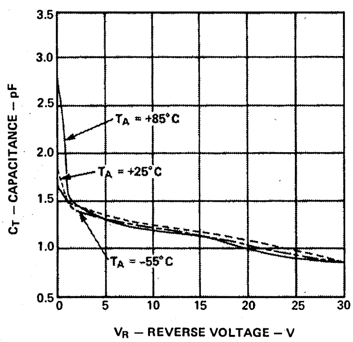


Figure 5. Capacitance vs. Reverse Voltage

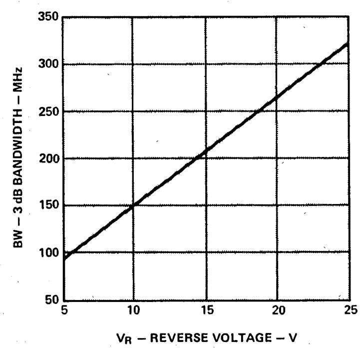


Figure 6. 3 dB Bandwidth vs. Reverse Voltage

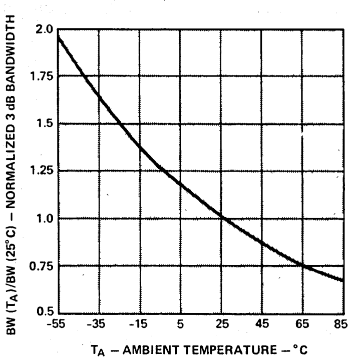


Figure 7. Normalized Bandwidth vs. Ambient Temperature

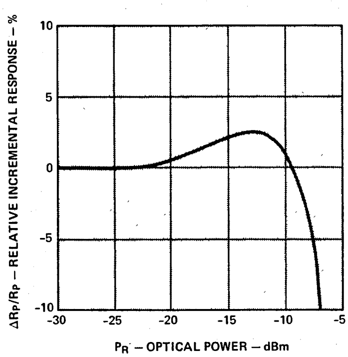


Figure 8. Linearity Characteristic vs. Optical Power

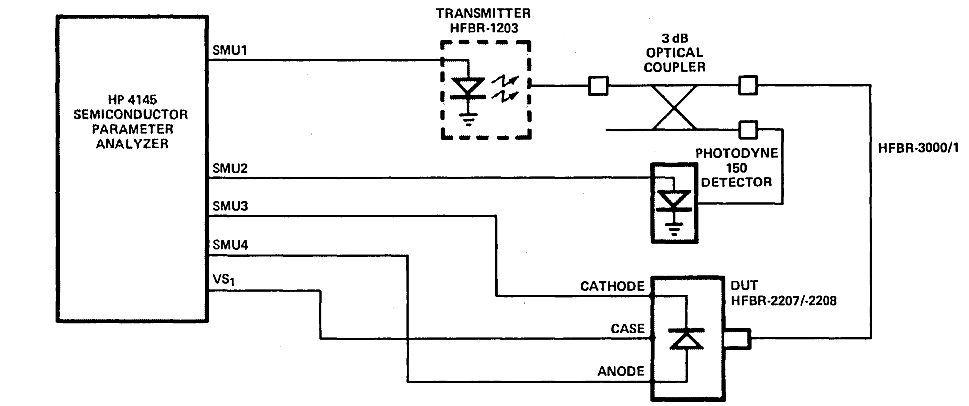


Figure 9. Test Set-up

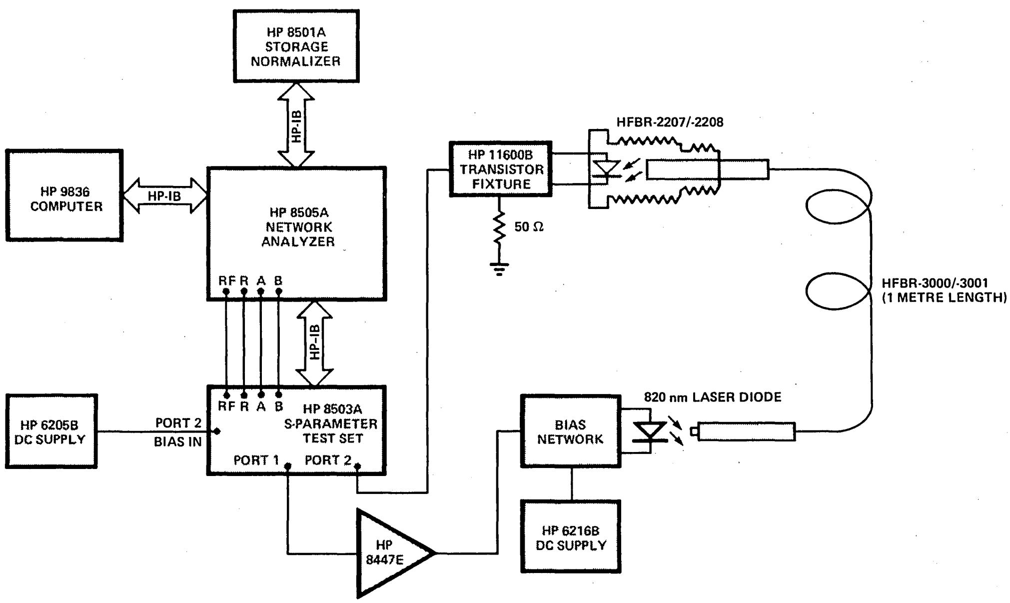
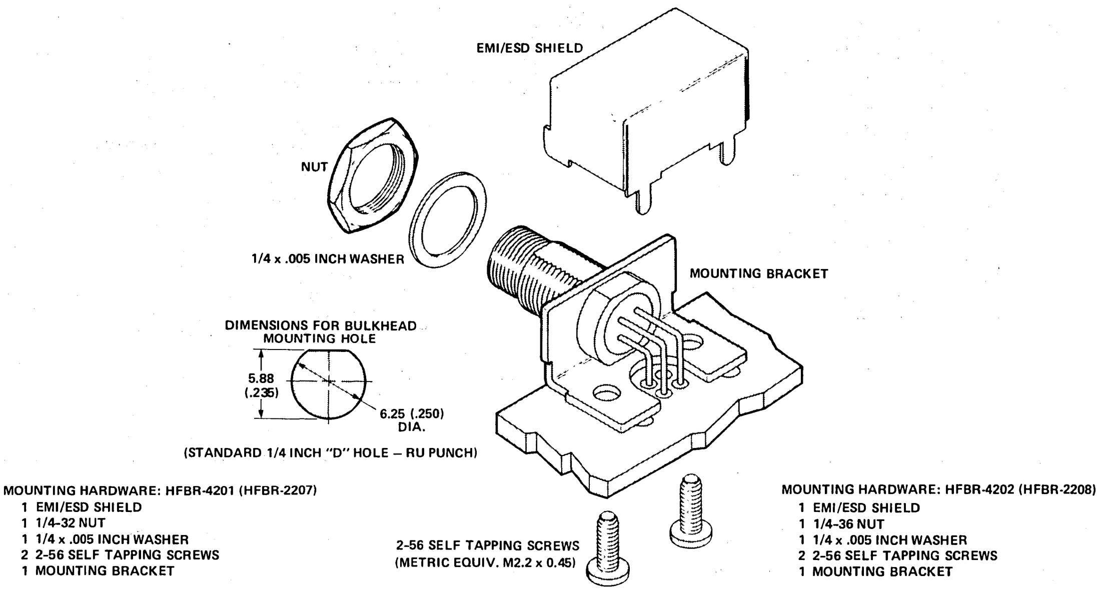


Figure 10. Bandwidth Measurement Set-up

Mechanical Description

The HFBR-2207 and 2208 fiber optic receivers are housed in rugged metal packages intended for use with the HP or SMA style connectored fiber cables. The low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking. A flat on the mounting threads of the device is provided to prevent rotation in all mounting configurations and to provide an orientation reference for the pin-out. Hardware is available for horizontal mounting applications on printed circuit boards. The hardware consists of a stainless steel mounting bracket fastened directly to the printed circuit board with two stainless steel self-tapping screws and a nut and washer for fastening the device in the bracket. A metal shield which snaps directly on the mounting bracket is also available for unusually severe EMI/ESD environments. When mounted in the horizontal configuration, the overall height of the component conforms with guidelines allowing printed circuit board spacing on 12.7 mm (0.500) centers. A thorough environmental characterization has been performed on these products. The test data as well as information regarding operation beyond the specified limits is available from any Hewlett-Packard sales office.

Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well.



Horizontal PCB Mounting

Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

When bending the leads, avoid sharp bends right where the lead enters the backfill. Use needle nose pliers to support the leads at the base of the package and bend the leads as desired.

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.

Application Information

NOISE FREE PROPERTIES

The noise current of the HFBR-2207/8 is negligible. This is a direct result of the exceptionally low leakage current, in accordance with the shot noise formula $I_N = (2qI_D\Delta f)^{1/2}$. Since the leakage current does not exceed 300 picoamps at a reverse bias of 20 volts, shot noise current is less than 9.8×10^{-15} amp $Hz^{-1/2}$ at this voltage.

Excess noise is also very low, appearing only at frequencies below 10 Hz, and varying approximately as 1/f. When the output of the diode is observed in a load, thermal noise of the load resistance (R_L) is $1.28 \times 10^{-10} (R_L)^{-1/2} \times (\Delta f)^{1/2}$ at 25° C, and far exceeds the diode shot noise for load resistance less than 100 megohms. Thus in high frequency operation where low values of load resistance are required for high cut-off frequency, the HFBR-2207/8 contributes virtually no noise to the system.

HIGH SPEED PROPERTIES

High speed operation is possible since the HFBR-2207/8 has low capacitance and wide bandwidth at a low reverse bias.

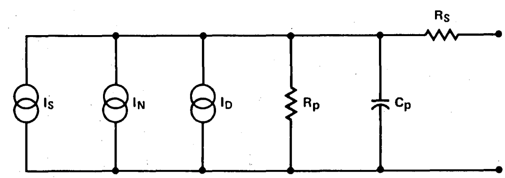


Figure 11. Photodiode Equivalent Circuit

I_S = Signal current ≈ 0.38 μA/μW x P_R
I_N = Shot noise current
< 9.8×10^{-15} amps/$Hz^{1/2}$

I_D = Dark current
< 300×10^{-12} amps at 20 V dc bias

$R_P = 10^{11}\ \Omega$
$R_S = 10\ \Omega$

LINEAR OPERATION

Operation of the photodiode is most linear when operated with a current amplifier as shown in Figure 12.

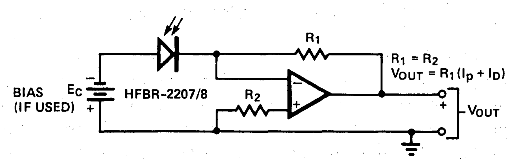
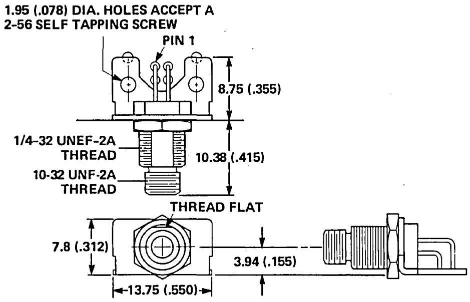


Figure 12. Linear Operation

Lowest noise is obtained with $E_C = 0$, but higher speed and wider dynamic range are obtained if $5 < E_C < 20$ volts. The amplifier should have as high an input resistance as possible to permit high loop gain. If the photodiode is reversed, bias should also be reversed.

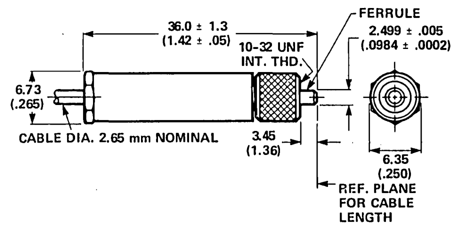
HFBR-2207 RECEIVER



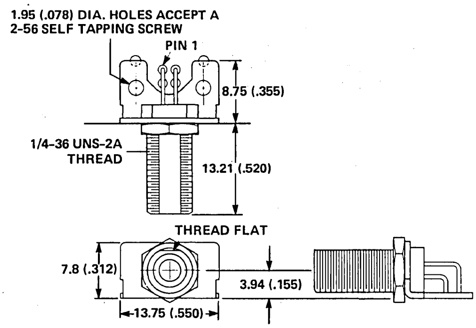
HEWLETT-PACKARD STYLE CONNECTOR

(Used in HFBR-3000/3100, Option 001 Cable Assemblies).

HFBR-4000 CONNECTOR

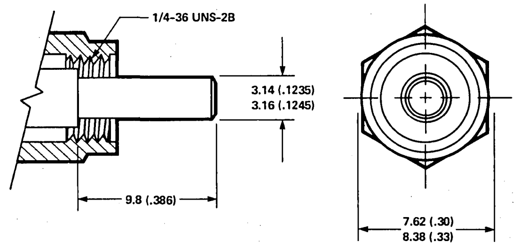


HFBR-2208 RECEIVER



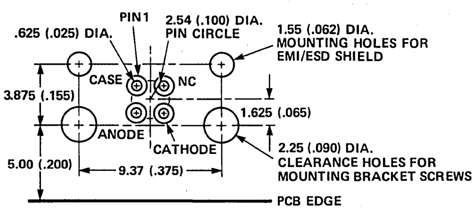
SMA STYLE CONNECTORS TYPE A

(Used in HFBR-3000/3100, Option 002 Cable Assemblies).



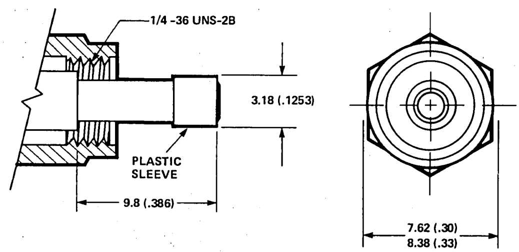
RECEIVER PCB LAYOUT DIMENSIONS

Top View



SMA STYLE CONNECTORS TYPE B

(Type B is not available from HP)



DIMENSIONS IN MILLIMETRES (INCHES).

Ordering Guide

Receivers: HFBR-2207 (HP Connector Compatible)
HFBR-2208 (SMA Connector Compatible)

Transmitters: HFBR-1201
HFBR-1202
HFBR-1203
HFBR-1204
(see data sheets)

Mounting Hardware: HFBR-4201 (HP Connector Compatible)
HFBR-4202 (SMA Connector Compatible)

Fiber Optic Cable

Hewlett-Packard offers connectored or unconnectored 100/140 μm fiber cables in simplex or duplex configurations. See data sheets for details.

FIBER OPTIC 100m HIGH PERFORMANCE TRANSMITTER MODULE

HEWLETT PACKARD

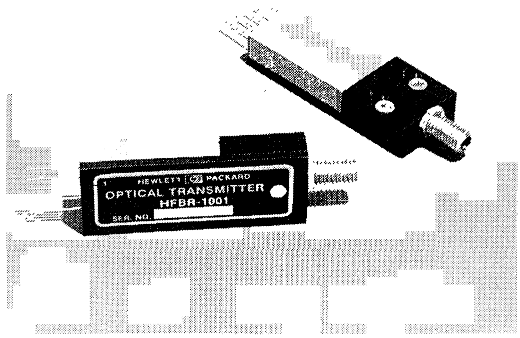
HFBR-1001

TECHNICAL DATA JANUARY 1986

Features

- **TRANSMISSION LENGTH: 100 METRES***
- **DATA RATE: DC TO 10 Mbaud***
- **NO DATA ENCODING REQUIRED***
- **TTL INPUT LEVELS**
- **FUNCTIONAL LINK MONITORING***
- **SINGLE +5V SUPPLY**
- **PCB MOUNTABLE, LOW PROFILE**
- **INTEGRAL, HIGH QUALITY OPTICAL CONNECTOR**
- **LOW POWER CONSUMPTION**

*When used with HFBR-2001 Receiver and any Hewlett Packard HFBR-3000/-3100 Series Cable/Connector Assembly.

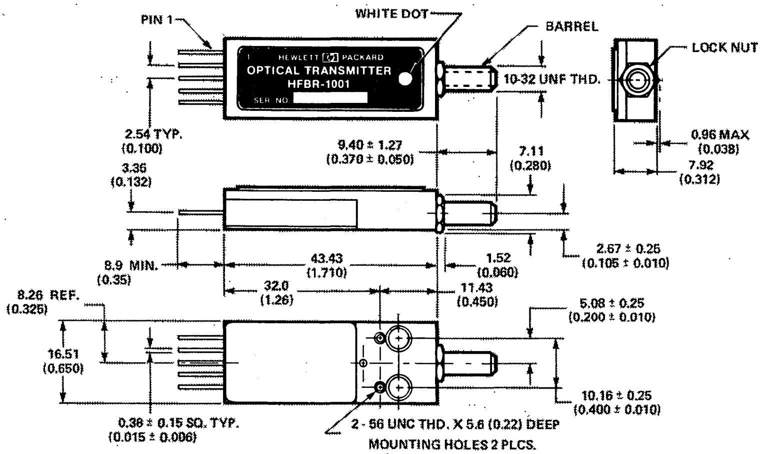


Description

The HFBR-1001 fiber optic transmitter is an integrated electrical to optical transducer designed for digital data transmission over single fiber channels. A bipolar integrated circuit and a GaAsP LED convert TTL level inputs to optical pulses at data rates from dc to 10Mb/s NRZ. An integral optical connector on the module allows easy interfacing without problems of source/fiber alignment. The low profile package is designed for direct printed circuit board mounting without additional heat sinking.

The HFBR-1001 is intended for use with HFBR-3000 fiber optic cable/connector assemblies, and the HFBR-2001 fiber optic receiver for transmission distances up to 100 metres. The HFBR-1001 generates optical signals in either of two externally selectable modes. The internally-coded mode produces a 3-level coded optical signal for reception and decoding by the HFBR-2001 receiver. This feature provides data format independence over the data rate range of dc to 10Mb/s NRZ while allowing for wide dynamic range and high sensitivity at the receiver. The externally-coded mode produces a 2-level optical signal which is a digital replica of the data input waveform. Used in this mode with the HFBR-2001 receiver, the user must provide proper data formatting (explained in the HFBR-2001 data sheet) to insure proper receiver operation. In either mode, the radiant output is radiologically safe (per ANSI Z136.1-1981).

Package Dimensions



CAUTION:
1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HEWLETT-PACKARD CABLE/CONNECTOR DATA SHEET (FINGER TIGHT).

PIN	FUNCTION
1	MODE SELECT
2	N.C.
3	GROUND
4	V_{CC}
5	DATA INPUT

NOTES:
1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ± 0.38mm (±0.015")

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	0	70	°C	
Lead Soldering	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6	V	
Mode Select or Data Input Voltage		V_I	-0.5	5.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Note
Ambient Temperature	T_A	0	70	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	4
High Level Input Voltage, Mode Select or Data Input	V_{IH}	2.0	V_{CC}	V	
Low Level Input Voltage, Mode Select or Data Input	V_{IL}	0	0.8	V	
Data Input Voltage Pulse Duration (high or low)	t_H, t_L	100		ns.	

Electrical/Optical Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ[6]	Max	Units	Conditions		Fig.	Note
High Level Input Current	Mode Select	I_{IH}			100	µA	V_{CC} = 5.25V, V_I = 2.4V		2	
	Data Input				20					
Low Level Input Current	Mode Select	I_{IL}			-1.6	mA	V_{CC} = 5.25V, V_I = 0.4V			
	Data Input				-0.6					
Supply Current	Externally-Coded Mode	I_{CC}			170	mA	Mode Select High	Data Input High V_{CC} = 5.25V	1, 2	5
			40					Data Input Low V_{CC} = 4.75V		
	Internally-Coded Mode		68	95	125		Mode Select Low	Data Input High or Low V_{CC} = 5.25V		
Optical Power	High Level	P_H		67		µW	Mode Select High	Data Input High	1, 2, 3	
	Low Level	P_L		3				Data Input Low		
	Mid Level (average)	P_M		35			Mode Select Low	Data Input Square Wave at 500 kHz		
	Excursion $\left(\frac{\text{peak-to-peak}}{2}\right)$	ΔP	22	32			Mode Select High			9
Amplitude Symmetry, Flux Excursion Ratio		k	0.8		1.2	—	Mode Select Low		1	7
Exit Numerical Aperture		N.A.		0.5		—			3	
Optical Port (fiber optic core) Diam.		D_C		200		µm				
Coupling Loss	from area mismatch	α_A		6.0		dB	with HFBR-3000 Cable/Connector Assembly			
	from numerical aperture mismatch	$\alpha_{N.A.}$		4.0						
Peak Emission Wavelength		λp		700		nm			4	

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ[6]	Max	Units	Conditions	Fig.	Note
Propagation Delay	High-to-Low Data Input Voltage Step	t_{PHL}		31		ns	V_{CC} = 4.75 V	1	8
	Low-to-High Data Input Voltage Step	t_{PLH}		35		ns			
Refresh Pulse Internally-Coded Mode	Duration	t_p		60		ns	V_{CC} = 5.00 V, Mode Select Low	1	8
	Repetition Rate	f_R		400		kHz			

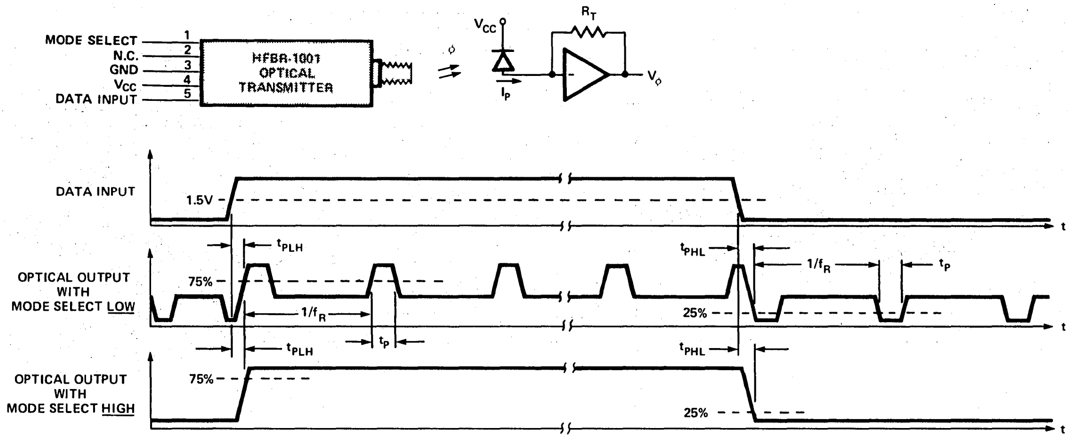


Figure 1. Optical Power Coding and Timing Diagram.

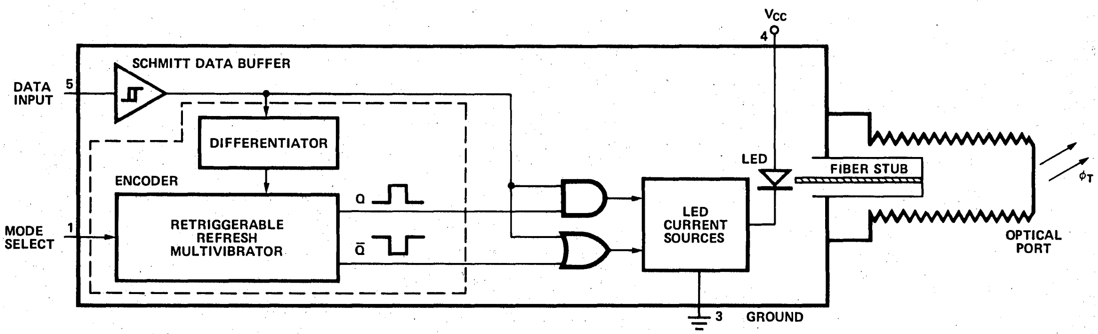


Figure 2. Schematic Diagram.

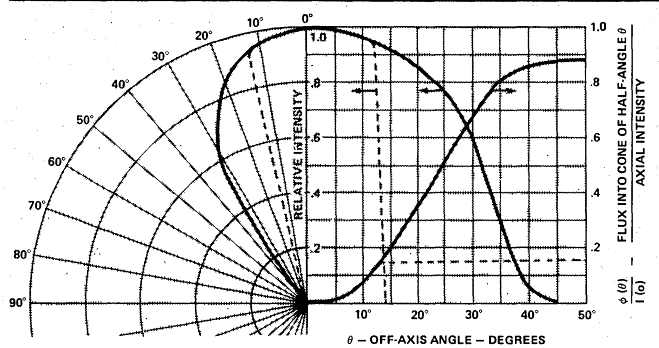


Figure 3. Radiation Pattern.*

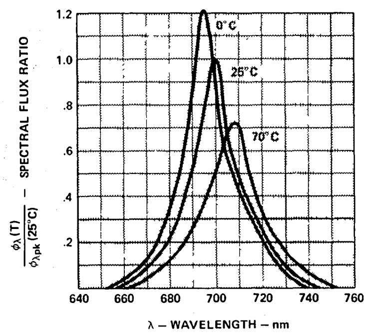


Figure 4. Emission Spectrum.

*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents radiation pattern from fiber stub without obscuration by connector barrel. Dashed line represents radiation pattern as seen from outside of connector.

Notes (cont'd):

3. Measured at a point 2mm (.079 in.) from where lead enters package.
4. A supply decoupling network of 2.2μH with 60μF is recommended.
5. Average currents for steady-state conditions at Data Input.
6. For typical values, V_{CC} = 5.00V and T_A = 25°C.
7. Optical power excursion ratio, k, is the ratio of optical power excursion above mid level to optical power excursion below mid level. $k = \frac{P_H - P_M}{P_M - P_L}$
8. The refresh pulse is interrupted (abbreviated) if Data Input changes state during the refresh pulse. MAX propagation delay is for Data Input changing state during the maximum excursion of the refresh pulse.
9. Optical power excursion
   $\Delta P = 0.5\,(P_H - P_L)$, or $\Delta P = 0.5\,(P_M - P_L) \bullet (1+k)$.

Notice that under the conditions specified for ΔP, the **average** flux is ($\Delta P + P_L$).

Electrical Description

The HFBR-1001 has two modes of operation: Internally-Coded mode and Externally-Coded mode. These are selected by making the Mode Select input "low" for Internally-Coded mode and "high" for Externally-Coded mode. With Mode Select "low," the optical signal generator in the HFBR-1001 produces a "mid-level" optical power which has positive or negative excursions, depending on whether Data Input is "high" or "low." In this Internally-Coded mode, a train of positive excursions is initiated when Data Input goes "high;" when Data Input goes "low," a train of negative excursions is initiated. These excursions are pulses of approximately 60ns duration with a 400 kHz repetition rate. Each initiation of a pulse train starts with a full-duration pulse, but when Data Input changes state, the train is terminated — even at mid-pulse — as a new train of opposite-polarity pulses is initiated. With this coding scheme and the low duty factor, the average optical power is always near the mid-level, regardless of the data rate or duration in either state. This coding scheme is designed to operate the HFBR 2001 Fiber Optic Receiver most effectively; the mid-level flux operates the Receiver's dc-restorer and the "refresh" pulses of either polarity keep the Receiver's ALC voltage at the proper level, allowing low propagation delay for any change of state at Data Input. The Internally-Coded mode permits transmission of analog information, e.g., by means of Pulse Width Modulation. Another advantage of the 3-level Internally-Coded mode is that supply current is nearly the same for either logic state, this reducing transients on the power supply line.

With Mode Select "high," the optical signal is at full maximum (~2 X mid level) when Data Input is "high," and nearly zero when Data Input is "low." This mode provides for these three applications:

1. Steady state turn-on of the photo-emitter at maximum flux level (e.g., for system diagnosis).
2. Stand-by mode (e.g., when the system is not in use).
3. Transmission of 2-level optical signals from externally generated code (e.g., Manchester) for receivers not configured for the 3-level code. With Mode Select "high," the output is either P_H, or P_L. Direct analog operation is not possible due to hysteresis in the response of the optical signal to the Data Input signal.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the transmitter can be mounted without consideration for external heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Transmitter with the ferrule in the HFBR-3000 Fiber Optic Cable/Connector. The connection procedure is to FIRST start the Connector ferrule into the sleeve; THEN screw the coupling ring on the barrel. The barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened as specified in the HFBR-3000 Fiber Optic Cable/Connector data sheet.

The HFBR-1001 should be mounted so that the lock nut at the optical port is not disturbed. Moving the lock nut can cause misalignment of the optical fiber stub inside the module resulting in a reduction of power output. Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

Good system performance requires clean ferrule faces to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well. If it is absolutely necessary to remove the threaded barrel and lock nut to clean the transmitter ferrule face, refer to the section "Installation Measurement and Maintenance" in Hewlett-Packard Application Note 1000.

FIBER OPTIC 1250m HIGH PERFORMANCE TRANSMITTER MODULE

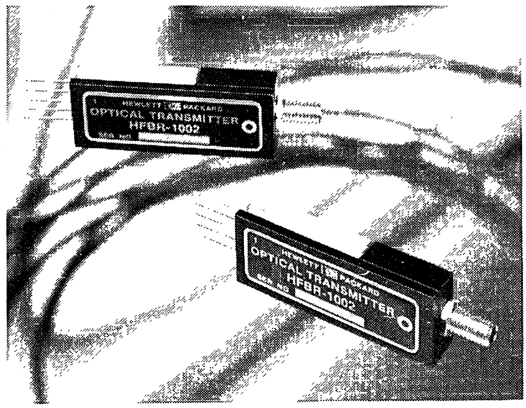
HFBR-1002

TECHNICAL DATA JANUARY 1986

Features

- PIN COMPATIBLE WITH HFBR-1001 TRANSMITTER
- TRANSMISSION LENGTH: 1250 METRES*
- DATA RATE: DC TO 10 Mbaud*
- NO DATA ENCODING REQUIRED*
- TTL INPUT LEVELS
- FUNCTIONAL LINK MONITORING*
- SINGLE +5V SUPPLY
- PCB MOUNTABLE, LOW PROFILE
- INTEGRAL, HIGH QUALITY OPTICAL CONNECTOR
- LOW POWER CONSUMPTION

*When used with HFBR-2001 Receiver and any Hewlett Packard HFBR-3000/-3100 Series Cable/Connector Assembly.



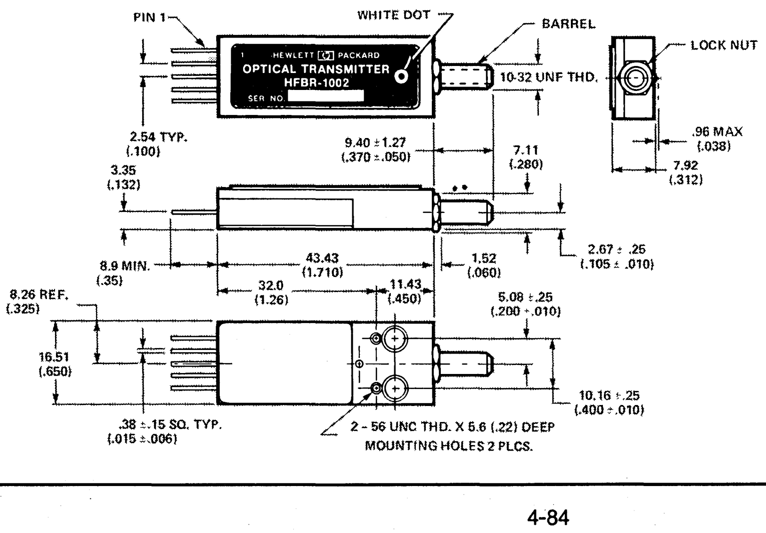
Description

The HFBR-1002 fiber optic transmitter is an integrated electrical to optical transducer designed for digital data transmission over single optical fiber channels. A bipolar integrated circuit and a high efficiency GaAlAs LED convert TTL level inputs to optical pulses at data rates from dc to 10 Mbaud (see note 5). An integral optical connector on the module allows easy interfacing without problems of fiber alignment. The low profile rugged industrial package is designed for direct circuit board mounting without additional heat sinking on printed circuit boards with 12.7 mm (0.5") card rack spacing.

The HFBR-1002 is intended for use with Hewlett-Packard fiber optic cable/connector assemblies, and the HFBR-2001 fiber optic receiver for transmission distances to 1250 metres. It is a direct replacement for extending links currently using the HFBR-1001 (100 metre) transmitter to give 1250 metre capability. The HFBR-1002 generates optical signals in either of two externally selectable modes. True dc response (data high or low for arbitrary time interval) is available when using the Internally-Coded mode.

WARNING: OBSERVING THE TRANSMITTER OUTPUT FLUX UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the near IR output flux is radiologically safe; however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Package Dimensions



CAUTION:
1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HEWLETT-PACKARD CABLE/ CONNECTOR DATA SHEET (FINGER TIGHT).

PIN	FUNCTION
1	MODE SELECT
2	N.C.
3	GROUND
4	V_{CC}
5	DATA INPUT

NOTES:
1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38mm (±.015")

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6	V	
Mode Select or Data Input Voltage		V_I	-0.5	5.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Note
Ambient Temperature	T_A	0	+70	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	4
High Level Input Voltage, Mode Select or Data Input	V_{IH}	2.0	V_{CC}	V	
Low Level Input Voltage, Mode Select or Data Input	V_{IL}	0	0.8	V	
Data Input Voltage Pulse Duration (high or low)	t_H, t_L	100		ns	5
Transmission Distance	ℓ		1250	m	6

Electrical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[7]	Max.	Units	Conditions		Fig.	Note
Optical Power	Transmitter Output $\frac{\text{peak-to-peak}}{2}$	P_O	-13 50	-11 80		dBm μW	Mode Select High	Data Input Square Wave at 500 kHz	1, 2, 3, 5	8
	High Level	P_H		165		μW	Mode Select High	Data Input High		
	Low Level	P_L		5		μW		Data Input Low		
	Mid Level	P_M		85		μW	Mode Select Low	Data Input Square Wave at 500 kHz		
Fixed Coupling Loss		α_F		1.5	5.4	dB	with HFBR-3000/3100 >300m			12
Output Optical Power Coupled into HFBR-3000 Fiber Cable/Connector Assembly, 100/140 μm		P_T		-12.5		dBm	Mode Select High	Data Input Square Wave at 500 kHz		13
Output Optical Power Coupled into 50/125 μm Fiber		P_T		-21		dBm	Mode Select High	Data Input Square Wave at 500 kHz		14
Output Optical Power Coupled into Siecor 100/140 μm Fiber Cable or equivalent		P_T		-14.5		dBm	Mode Select High	Data Input Square Wave at 500 kHz		15
Amplitude Symmetry, Flux Excursion Ratio		k	0.8		1.2	—	Mode Select Low		1	9
Exit Numerical Aperture		N.A.		0.3		—			3	
Optical Port (fiber optic core) Diam.		D_C	c	100		μm				
Peak Emission Wavelength		λ_{PK}		820		nm			4	
High Level Input Current	Mode Select	I_{IH}			100	μA	$V_{CC} = 5.25$ V, $V_I = 2.4$ V		2	
	Data Input				20					
Low Level Input Current	Mode Select	I_{IL}			-1.6	mA	$V_{CC} = 5.25$ V, $V_I = 0.4$ V			
	Data Input				-0.6					
Supply Current	Externally-Coded Mode	I_{CC}			170	mA	Mode Select High	Data Input High $V_{CC} = 5.25$ V	1, 2	10
			40					Data Input Low $V_{CC} = 4.75$ V		
	Internally-Coded Mode		68	95	125		Mode Select Low	Data Input High or Low, $V_{CC} = 5.25$ V		

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ[7]	Max	Units	Conditions	Fig.	Note
Propagation Delay	High-to-Low Data Input Voltage Step	t_{PHL}		34		ns	$V_{CC} = 4.75$ V Data Input Square Wave at 500 kHz	1	11
	Low-to-High Data Input Voltage Step	t_{PLH}		32		ns			
Refresh Pulse Internally-Coded Mode	Duration	t_p		40		ns	$V_{CC} = 5.00$ V, Mode Select Low	1	11
	Repetition Rate	f_R		400		kHz			

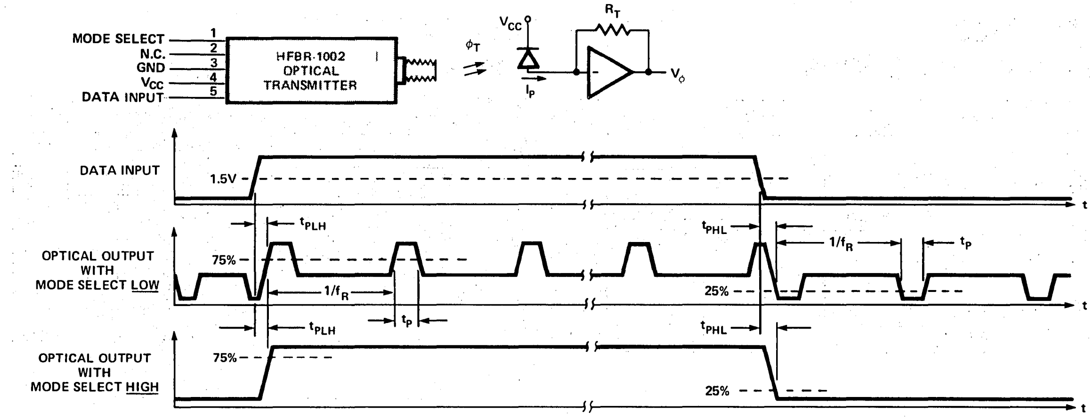


Figure 1. Flux Coding and Timing Diagram.

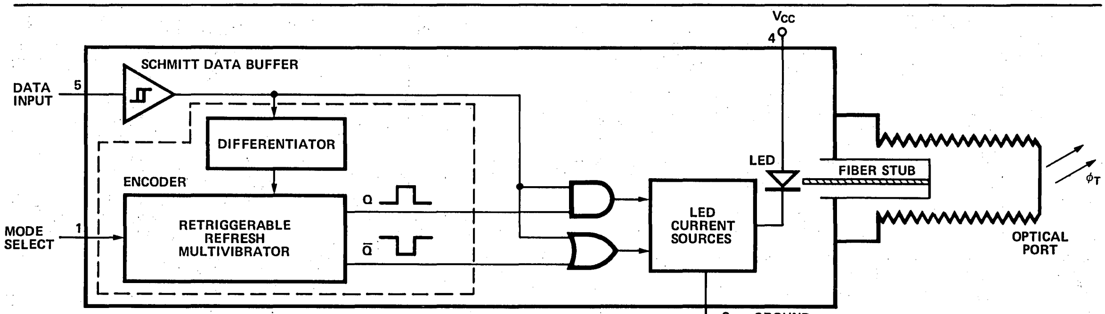


Figure 2. Schematic Diagram.

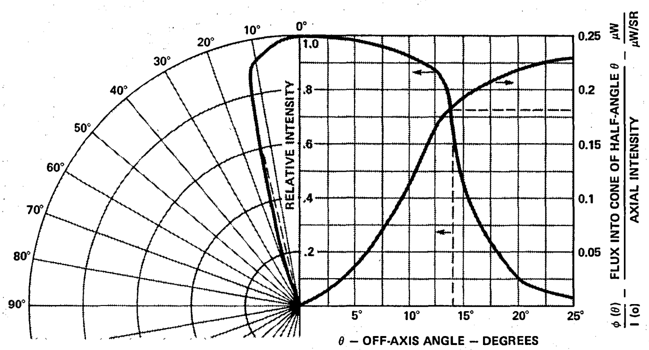


Figure 3. Radiation Pattern.*

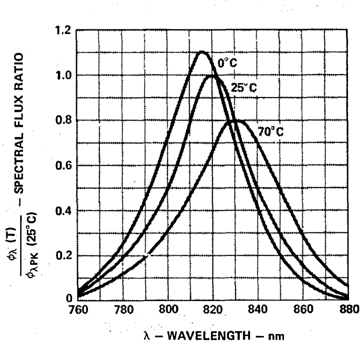


Figure 4. Emission Spectrum.

*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents radiation pattern from fiber stub without obscuration by connector barrel. Dashed line represents radiation pattern as seen from outside of connector.

Notes (cont'd):

3. Measured at a point 2mm (.079 in.) from where lead enters package.
4. A supply decoupling network of 2.2μH with 60μF is recommended.
5. With NRZ data, 10 Mbaud corresponds to a data rate of 10 Mbits/second. With other codes, the data rate is the baud rate divided by the number of code intervals per bit interval. Self-clocking code (e.g., Manchester) usually has two code intervals per bit interval giving 5 Mbits/second at 10 Mbaud.
6. With Hewlett-Packard HFBR-2001 and HFBR-3000 Series Cable/Connector Assembly.
7. For typical values, V_{CC} = 5.00V and T_A = 25° C.
8. The transmitter output, P_T, equals the optical power excursion, $\Delta P = (P_H - P_L)/2$. Notice that under the conditions specified for ΔP, the average optical power is $(P_H + P_L)/2$.
9. Optical power excursion ratio, k, is the ratio of optical power excursion above mid level to optical power excursion below mid level.

$$k = \frac{P_H - P_M}{P_M - P_L}$$

10. Average currents for steady-state conditions at Data Input.
11. The refresh pulse is interrupted (abbreviated) if Data Input changes state during the refresh pulse. MAX propagation delay is for Data Input changing state during the maximum excursion of the refresh pulse.
12. When used with the HFBR-3000/3100 cable assemblies, the total insertion loss (α_T) is calculated as follows:
   α_T = 8.4 dB; $\ell \leq$ 300m
   $\alpha_T = \alpha_F + \alpha_O \cdot \ell/1000$; $\ell >$ 300m
   Where α_O = Cable attenuation at 820 nm; ℓ = cable length (metres).
13. Measured at the end of 1.0 metre HFBR-3000 Fiber Optic Cable with large area detector and cladding modes stripped.

Electrical Description

The HFBR-1002 has two modes of operation: Internally-Coded mode and Externally-Coded mode. These are selected by making the Mode Select input "low" for Internally-Coded mode and "high" for Externally-Coded mode. With Mode Select "low," the optical signal generator in the HFBR-1002 produces a "mid-level" optical power which has positive or negative excursions, depending on whether Data Input is "high" or "low". In this Internally-Coded mode, a train of positive excursions is initiated when Data Input goes "high," when Data Input goes "low", a train of negative excursions is initiated. These excursions are pulses of approximately 40ns duration with a 400kHz repetition rate. Each initiation of a pulse train starts with a full-duration pulse, but when Data Input changes state, the train is terminated — even at mid-pulse — as a new train of opposite-polarity pulses is initiated. With this coding scheme and the low duty factor, the average optical power is always near the mid-level, regardless of the data rate or duration in either state. This coding scheme, which is transparent to the user, is designed to operate the HFBR-2001 Fiber Optic Receiver most effectively; the mid-level flux operates the Receiver's dc-restorer and the "refresh" pulses of either polarity keep the Receiver's ALC voltage at the proper level, providing data format independence (no data encoding required) over the data rate range of dc to 10Mbaud. The Internally-Coded mode permits transmission of analog information, e.g., by means of Pulse Width Modulation. Another advantage of the 3-level Internally-Coded mode is that supply current is nearly the same for either logic state, thus reducing transients on the power supply line.

With Mode Select "high," the optical signal is at full maximum (~2 X mid-level) when Data Input is "high," and nearly zero when Data Input is "low." Used in this mode with the HFBR-2001 Receiver, the user must provide proper data formatting (e.g., Manchester or Bi-Phase coding, explained in HFBR-2001 data sheet) to ensure proper receiver operation. This mode provides for these three applications:

1. Steady state turn-on of the photo-emitter at maximum flux level (e.g., for system diagnosis).
2. Stand-by mode (e.g., when the system is not in use).
3. Transmission of 2-level optical signals from externally generated code (e.g., Manchester) for receivers not configured for the 3-level code. With Mode Select "high," the output is either P_H, or P_L. Direct analog operation is not possible due to hysteresis in the response of the optical signal to the Data Input signal.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the transmitter can be mounted without consideration for external heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Transmitter with the ferrule in the Hewlett-Packard Fiber Optic Cable/Connector Assembly. The threaded barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened finger-tight as specified in the Hewlett-Packard Fiber Optic Cable/Connector data sheet.

The HFBR-1002 should be mounted so that the lock nut at the optical port is not disturbed. Moving the lock nut can cause misalignment of the optical fiber stub inside the module resulting in a reduction of power output. Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

Good system performance requires clean ferrule faces to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well. If it is absolutely necessary to remove the threaded barrel and lock nut to clean the transmitter ferrule face, refer to the section "Installation Measurement and Maintenance" in Hewlett-Packard Application Note 1000.

FIBER OPTICS

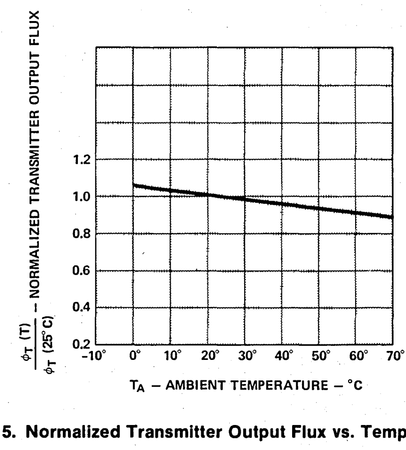


Figure 5. Normalized Transmitter Output Flux vs. Temperature.

HEWLETT PACKARD

FIBER OPTIC HIGH PERFORMANCE RECEIVER MODULE

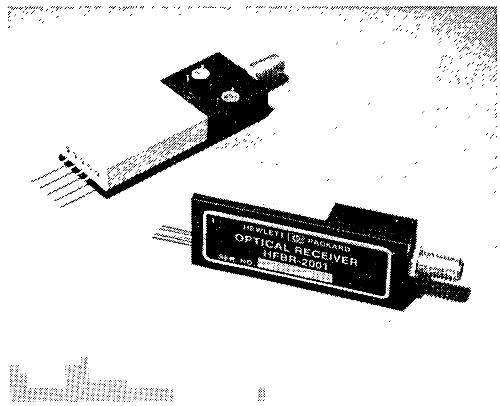
HFBR-2001

TECHNICAL DATA JANUARY 1986

Features

- **DATA RATE: DC TO 10 Mbaud***
- **LOW NOISE: 10^{-9} BER WITH 0.8 μW INPUT***
- **NO DATA ENCODING REQUIRED***
- **TTL OUTPUT LEVELS**
- **FUNCTIONAL LINK MONITORING***
- **OPTICAL POWER INPUT INDICATION**
- **SINGLE +5V SUPPLY**
- **PCB MOUNTABLE, LOW PROFILE**
- **INTEGRAL, HIGH QUALITY OPTICAL CONNECTOR.**

*When used with HFBR-1001/-1002 Transmitters and any Hewlett Packard HFBR-3000/-3100 Series Cable/Connector Assembly.



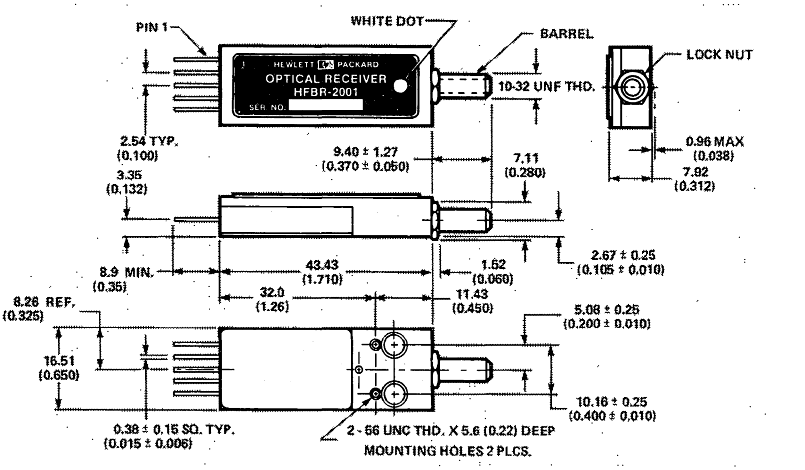
Description

HFBR-2001 fiber optic receiver is an integrated optical to electrical transducer designed for reception of digital data over single fiber channels. A silicon PIN photodetector and a bipolar integrated circuit convert optical pulses to TTL level outputs with an optical sensitivity of .8 μW, and data rates to 10 Mb/s NRZ. An integral optical connector on the module allows easy interfacing without problems of fiber/detector alignment. The low profile package is designed for direct printed circuit board mounting without additional heat sinking.

The HFBR-2001 is intended for use with HFBR-3000 fiber optic cable/connector assemblies and the HFBR-1001/1002 fiber optic transmitters. In order to provide wide dynamic range, dc response, and high sensitivity, the receiver must periodically extract information from the optical waveform. When operating with a transmitter in the internally-coded mode, this information is automatically provided by the transmitter. When operating in the externally-coded mode, or with another transmission source, the user must provide proper data formatting to insure proper receiver operation.

An additional TTL output called Link Monitor (LM), provides a digital indication of link continuity independent of the presence of data. Link continuity is indicated by a logical high output state.

Package Dimensions



CAUTION:
1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HEWLETT-PACKARD CABLE/ CONNECTOR DATA SHEET (FINGER TIGHT).

PIN	FUNCTION
1	TEST POINT
2	LINK MONITOR
3	GROUND
4	V_{CC}
5	DATA OUTPUT

NOTES:
1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ± 0.38mm (± 0.015")

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	0	70	°C	
Lead Soldering Cycle	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6.0	V	
Output Voltage (High State)		V_{OH}		6.0	V	

Recommended Operating Conditions

Parameter			Symbol	Min	Max	Units	Note
Ambient Temperature			T_A	0	70	°C	
Supply Voltage			V_{CC}	4.75	5.25	V	
Supply Ripple (Peak-to-Peak)			ΔV_{CC}		250	mV	4
High Level Output Current	Link Monitor		I_{OH}		-100	µA	
	Data Output				-400		
Low Level Output Current			I_{OL}		8	mA	
Average Input Optical Power			P_M	0.8	70	µW	6
Peak-to-Peak Input Optical Power			$P_H - P_L$	1.6	140	µW	
Optical Input Pulse Duration and Timing	2-Level Code	High Level	t_H	100	5000	ns	
		Low Level	t_L				
	Flux Excursion Ratio		k	0.75	1.25		7
	3-Level Code	High Level	t_H	50		ns	
		Low Level	t_L				
		Mid Level	t_M	0.05	6.7	µs	8
	Refresh Repetition Rate		f_R	150		kHz	
	Refresh Duty Factor		$f_R t_H, f_R t_L$		0.04		

Electrical/Optical Characteristics 0° C to 70° C Unless Otherwise Specified

Parameter			Symbol	Min	Typ[5]	Max	Units	Conditions	Fig.	Note
Output Voltage	High State	Data Output	V_{OH}	2.4	2.85		V	$P = (P_M + 0.8\ \mu W)$, $I_o = -400\ \mu A$; $V_{CC} = 4.75$ V	1, 2	7, 9
		Link Monitor						$\Delta P = 0.8\ \mu W$, $I_o = -100\ \mu A$		
	Low State	Data Output	V_{OL}		0.35	0.5	V	$P = (P_M - 0.8\ \mu W)$; $I_o = 8$ mA		
		Link Monitor			0.2	0.4		$\Delta P = 0$; $V_{CC} = 4.75$ V		
Test Point Voltage			V_T		0		V	$P_M = 100\ \mu W$		10
					1.3			$P_M = 0$		
Supply Current			I_{CC}		77	100	mA	$V_{CC} = 5.25$ V		
				60	77			$V_{CC} = 4.75$ V		
Optical Port (fiber optic core) Diameter			D_C		200		µm			
Numerical Aperture			N.A.		0.5				3	
Peak Responsivity Wavelength			λ_P		770		nm		4	

Dynamic Characteristics 0° C to 70° C Unless Otherwise Specified

Parameter			Symbol	Min	Typ[5]	Max	Units	Conditions	Fig.	Note
Propagation Delay	High to Low	3-Level Code	t_{PHL}		29		ns	$V_{CC} = 4.75$ V, k = 1, Link Monitor High	1	11
		2-Level Code			37					
	Low to High	3-Level Code	t_{PLH}		37		ns			12
		2-Level Code			45					
Link Monitor Response Time	Low-to-High		t_{MH}		20		ms	$V_{CC} = 4.75$ V $\Delta p = 0.8\ \mu W$		13
	High-to-Low		t_{ML}		1000			$I_{OL} = 8$ mA Peak-to-Peak		14
Bit Error Rate at 10 M baud			BER			10^{-9}		$k = 1, \Delta p \geqslant 0.8\ \mu W$		15

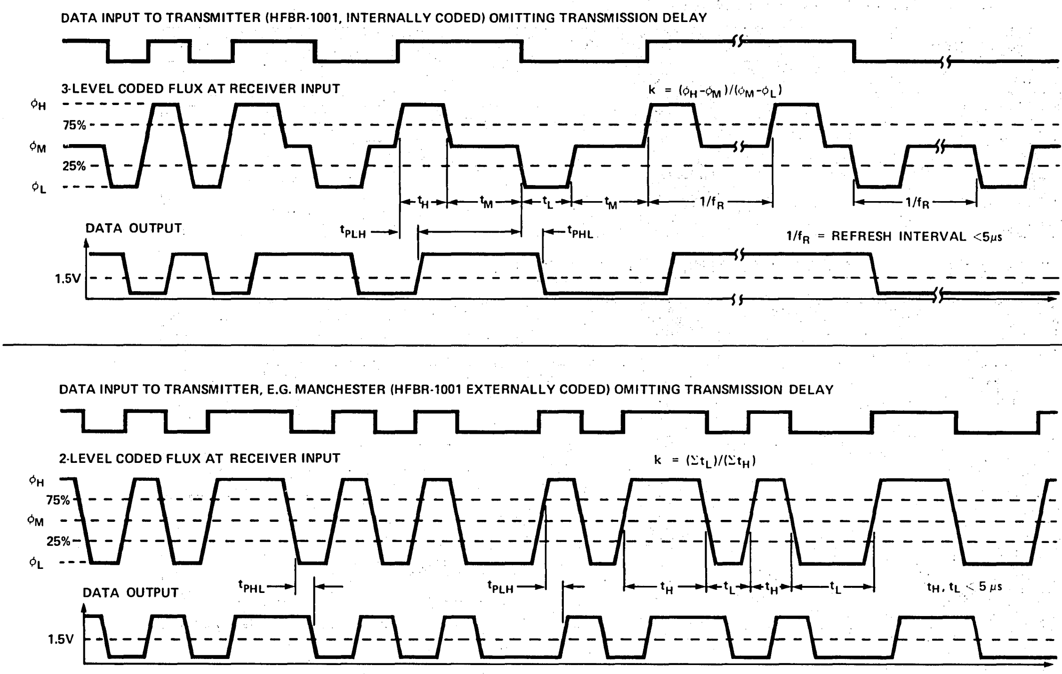


Figure 1. Optical Input Timing Requirements.

Notes (cont'd):

3. Measured at a point 2mm (.079″) from where the lead enters the package.
4. If ripple exceeds the specified limit, the regulator shown in Figure 5 should be used. The LC filter shown in Figure 5 is recommended whether the regulator is used or not.
5. For typical values, V_{CC} = 5.00V and T_A = 25°C.
6. Optical power is average over an interval of at least 50 μs. Optical power values specified are for the equivalent of a monochromatic source between 700nm and 820nm.
7. For either 2-level or 3-level code, $k = (P_H - P_M)/(P_M - P_L)$.
8. For the HFBR-2001, a *3-Level Code* is defined as having a mid-level, with equal-amplitude and pulse width excursions to high-level or to low-level.
9. Link Monitor provides a check of link continuity. A low Link Monitor output indicates that the optical signal path has been interrupted. For example, it might indicate a broken cable or a loose, dirty, or damaged connector. The link may still be operational with Link Monitor low, but it should be checked to determine the cause of the low indication. When the source of optical power is an Internally-Coded HFBR-1001/1002 Fiber Optic Transmitter, Link Monitor high will be a valid indication of link continuity whether or not data is being transmitted. An optical input with excursions (ΔP) greater than or equal to 0.8μW is sufficient to hold Link Monitor high.
10. When observing V_T, use a voltmeter with at least 10MΩ input resistance. With zero input optical power, V_T is at its maximum value, $V_{T,MAX}$. Then when flux is being received, whether modulated or not:

    $(V_{T,MAX} - V_T) = (25k\Omega)(I_P) = (25k\Omega)(R_P P_M)$

    where I_P = average photodiode photocurrent

    $R_P \approx 0.4A/W$ = photodiode responsivity

    P_M = average flux being received
11. Measured from the time at which optical input crosses the 25% level until DATA OUTPUT = 1.5V in HL transition.
12. Measured from the time at which optical input crosses the 75% level until DATA OUTPUT = 1.5V in LH transition.

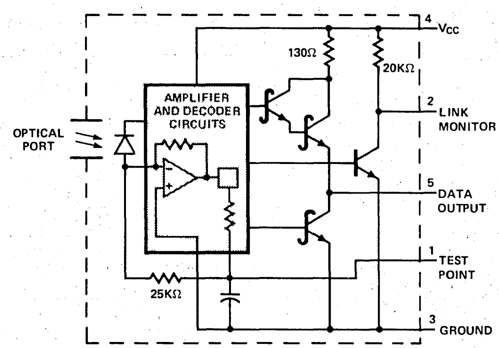


Figure 2. Schematic Diagram.

13. Measured from the time at which optical input fluctuation begins until LINK MONITOR rises to 1.5V.
14. Measured from the time at which optical input fluctuation ceases until LINK MONITOR falls to 1.5V.
15. With NRZ data, 10Mbaud corresponds to a data rate of 10Mb/s. With other codes, the data rate is the baud rate divided by the number of code intervals per bit interval—self-clocking code (e.g., Manchester) usually has two code intervals per bit interval giving 5Mb/s at 10Mbaud.

Electrical Description

Flux enters the HFBR-2001 via an optical fiber stub where a PIN photodiode converts it to a photocurrent. This photocurrent goes to an I-V (current-to-voltage) amplifier which utilizes both dc feedback and ALC (automatic level control).

The function of dc feedback is to keep the average value of the signal centered in the linear range of the amplifier. The dc feedback amplifier has a high impedance output to establish a long time constant on a capacitor at its output. (The voltage on the capacitor is observable at the test point). As seen in the schematic diagram, the voltage on this capacitor extracts the *average* component of photocurrent from the input of the I-V amplifier so its *average* output is at a *fixed level.* Optical flux excursions above and below the average cause voltage excursion above and below the fixed level at the output of the I-V amplifier.

The voltage excursions operate a flip-flop whose output drives the Data Output amplifier; an excursion above the average level sets the data output high, where it remains until an excursion below the average level resets the flip-flop.

To prevent overdrive, an ALC circuit, responding to excursions *either above or below* the average level, controls the gain of the I-V amplifier. Gain is then determined by *whichever polarity* of excursion is the *greater*. If these excursions are too far from being balanced, the gain limitation imposed by the larger excursion may cause the smaller (opposite polarity) excursion to be too small to operate the flip-flop.

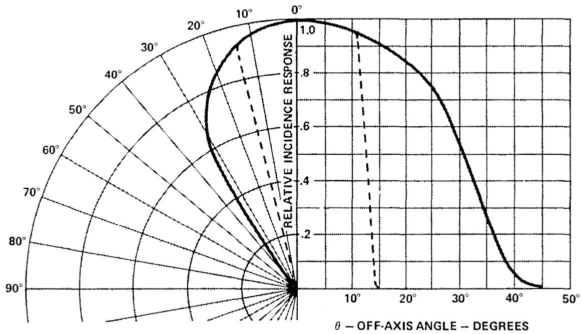
The Link Monitor output is driven by an amplifier which responds to the ALC voltage. The Link Monitor is high when the flux excursions are greater than or equal to 0.8μW.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the Receiver can be mounted without consideration for additional heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Receiver with the ferrule in the HFBR-3000 Fiber Optic Cable/Connector. The connection procedure is to FIRST start the Connector ferrule into the sleeve, THEN screw the coupling ring on the barrel. The barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened as specified in the HFBR-3000 Fiber Optic Cable/Connector data sheet.

Good system performance requires clean ferrule faces to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well. If it is absolutely necessary to remove the threaded barrel and lock nut to clean the Receiver ferrule face, refer to the section "Installation Measurement and Maintenance" in Hewlett-Packard Application Note 1000.

FIBER OPTICS 6



*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents reception pattern at fiber stub without obscuration by connector barrel. Dashed line represents reception pattern as seen from outside of connector.

Figure 3. Reception Pattern.*

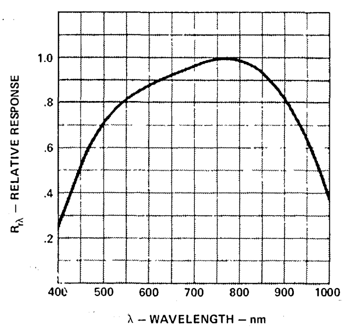


Figure 4. Spectral Response.

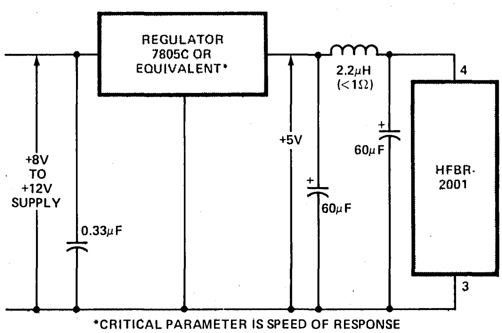


Figure 5. Power Supply Transient Filter Recommendation.

HEWLETT PACKARD

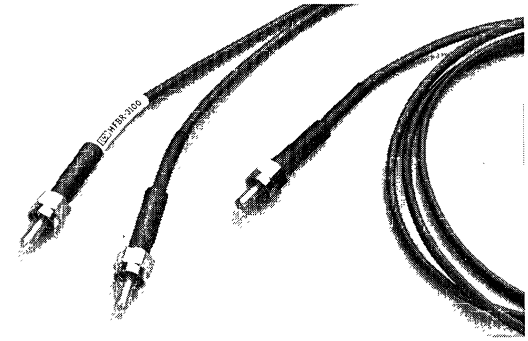
FIBER OPTIC CABLE/CONNECTOR ASSEMBLIES

HFBR-3000
HFBR-3100
HFBR-3001
HFBR-3021

TECHNICAL DATA JANUARY 1986

Features

- HFBR-4000 OR SMA STYLE CONNECTORS
- CONNECTORS FACTORY INSTALLED AND TESTED
- SIMPLEX OR DUPLEX CABLE
- USER SPECIFIED CABLE LENGTHS
- UL RECOGNIZED COMPONENT PASSES UL VW-1 FLAME RETARDANCY SPECIFICATION*
- STANDARD 100/140 μm GLASS FIBER
- RUGGED TIGHT JACKET CONSTRUCTION
- PARAMETERS OPTIMIZED FOR LOCAL DATA COMMUNICATIONS
- BANDWIDTH: 40 MHz AT 1 km



Description

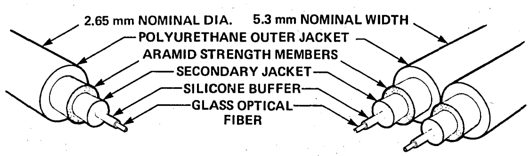
The HFBR-3000 Simplex Fiber Optic Cable/Connector assemblies and HFBR-3100 Duplex Fiber Optic Cable/Connector assemblies are intended for use with HP's High Performance Modules (HFBR-1001/2, HFBR-2001) and the Miniature Link series of transmitters and receivers (HFBR-12XX, HFBR-22XX) and 39301A RS-232 to Fiber Optic Multiplexer. These cable assemblies are available with either HFBR-4000 connectors (OPT 001) or SMA style connectors (OPT 002).

The HFBR-3000 Simplex cable is constructed of a single graded index glass fiber surrounded by a silicone buffer, secondary jacket, and aramid strength members. The combination is covered with a scuff resistant polyurethane outer jacket.

The HFBR-3100 Duplex cable has two glass fibers each in a cable of construction similar to the simplex cable, joined with a web. The individual channels are identified by a marking on one channel of the cable.

*UL File Number E84364

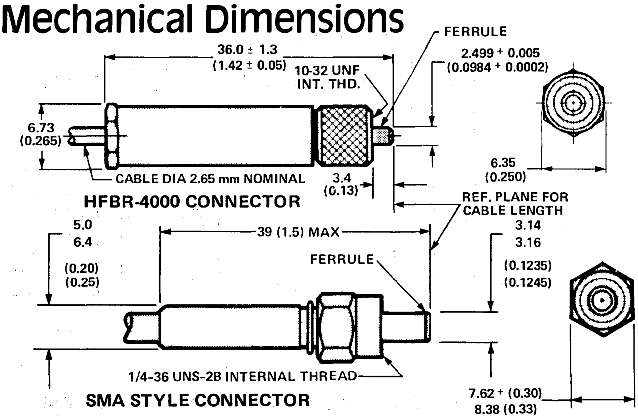
Fiber Optic Cable Construction



The HFBR-3001 is a ten metre Simplex Cable assembly terminated with HFBR-4000 connectors. The HFBR-3021 is a ten metre Simplex Cable assembly terminated with SMA style connectors.

The cable's resistance to mechanical abuse, safety in flammable environments, and absence of electromagnetic interference effects may make the use of conduit unnecessary. However, the light weight and high strength of the cables allows them to be drawn through most electrical conduits. The connectors must be protected during installation by a pulling grip such as Kellems 033-29-003.

Mechanical Dimensions



CABLE LENGTH TOLERANCE

Cable Length (Metres)	Tolerance
1-10	+10/-0 %
11-100	+1/-0 Metre
> 100	+1/-0 %

NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. FIBER END IS LOCKED FLUSH WITH FERRULE FACE.

CAUTION:
1. COUPLING NUT SHOULD NOT BE OVERTIGHTENED: TORQUE 0.05 TO 0.1 UNITS N·m OVER TIGHTENING MAY CAUSE EXCESSIVE FIBER MISALIGNMENT OR PERMANENT DAMAGE.
2. GOOD SYSTEM PERFORMANCE REQUIRES CLEAN FERRULE FACES TO AVOID OBSTRUCTING THE OPTICAL PATH. CLEAN COMPRESSED AIR OFTEN IS SUFFICIENT TO REMOVE PARTICLES. A COTTON SWAB SOAKED IN METHANOL OR FREON™ MAY ALSO BE USED.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Relative Humidity at $T_A = 70°C$			95	%	13
Storage Temp.	T_S	-40	+85	°C	
Operating Temp.	T_A	-20	+85	°C	
Bend Radius, No Load	r	20		mm	9, 10
Flexing		50K		Cycles	1

Parameter		Symbol	Min.	Max.	Units	Note
Crush Load		F_C		200	N	2, 8
Impact		m		1.5	kg	3
		h		0.15	m	
Tensile Force	on Cable	F_T		300	N	9, 8
	on Connector/Cable			100		

Mechanical/Optical Characteristics −20°C to +85°C Unless Otherwise Specified.

Parameter		Symbol	Min.	Typ.[6]	Max.	Units	Conditions	Fig.	Note
Exit Numerical Aperture		N.A.		0.3		—	$\lambda = 820$ nm, $\ell \geq 300$m		4
Attenuation		α_o	3.5	5.5	8	dB/Km	$\lambda = 820$ nm	1	7, 12
Bandwidth @ 1 km		BW		40		MHz	$\lambda = 820$ nm (LED)		5
Travel Time Constant		l/V		5		ns/m	$\lambda = 820$ nm		11
Optical Fiber Core Diameter		D_C		100		μm			
Cladding Outside Diameter		D_{CL}		140		μm			
Index Grading Coefficient		g		2		—			
Cable Structural Strength		F_C		1800		N			8
Mass per Unit Length	Single Channel	m/ℓ		6		kg/km			
	Dual Channel			12					
Cable Leakage Current		I_L		30		nA	50KV, $\ell = 0.3$m		

Notes:

1. 180° bending at minimum bend radius, with 10N tensile load.
2. Force applied on 2.5 mm diameter mandrel laid across the cable on a flat surface, for 100 hours, followed by flexure test.
3. Tested at 1 impact according to DOD-STD-1678, Method 2030, Procedure 1.
4. Exit N.A. is defined as the sine of the angle at which the off-axis radiant intensity is 10% of the axial radiant intensity.
5. Bandwidth is measured with a pulsed LED source ($\lambda = 820$ nm), and varies as $\ell^{-0.85}$, where ℓ is the length of the fiber (km). Pulse dispersion and bandwidth are approximately inversely related.
6. Typical values are at $T_A = 25°C$.
7. Fixed losses (length independent) are included in Transmitter/Receiver optical specifications.
8. One Newton equals approximately 0.225 pounds force.
9. Short term, ≤ 1 hr.
10. The probability of a fiber weak point occurring at a point of maximum bend is small, consequently the risk of fiber breakage from exceeding the maximum curvature is extremely low.
11. Travel time constant is the reciprocal of the group velocity for propagation of optical power. Group velocity, $V = \lambda/n$ where λ = velocity of light in space = 3×10^8m/s and n = effective core index of refraction.
12. For lower attenuation cable consult local sales office.
13. This applies to cable only.

Cable Assembly-Ordering Guide

HFBR-3000/HFBR-3100 defines fiber optic cables with factory installed connectors of user specified length. The cable length must be specified in metres and can be any length in one metre increments from 1 to 1500 metres (longer cables available upon request). Option 001 specifies that the cable is terminated with HFBR-4000 connectors and Option 002 specifies that the cable is terminated with SMA style connectors. Either OPT 001 or OPT 002 must be specified.

Examples:

A. To order one Duplex Cable assembly 125 metres long, with SMA style connectors, specify:

HFBR-3100	Quantity 125
OPT 002	Quantity 1

B. To order four Simplex Cable assemblies, 150 metres each, with HFBR-4000 connectors, specify:

HFBR-3000	Quantity 600
OPT 001	Quantity 4

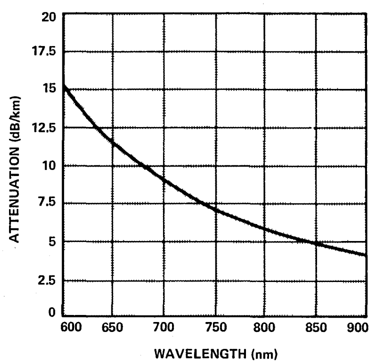


Figure 1. Attenuation vs. Wavelength

HEWLETT PACKARD

FIBER OPTIC CABLE

HFBR-3200
HFBR-3300

TECHNICAL DATA JANUARY 1986

Features

- **SIMPLEX OR DUPLEX CABLE**
- **USER SPECIFIED CABLE LENGTHS**
- **UL RECOGNIZED COMPONENT, PASSES UL VW-1 FLAME RETARDANCY SPECIFICATION***
- **STANDARD 100/140 μm GLASS FIBER**
- **RUGGED TIGHT JACKET CONSTRUCTION**
- **PARAMETERS OPTIMIZED FOR LOCAL DATA COMMUNICATION**
- **BANDWIDTH: 40 MHz AT 1 km**

Description

The HFBR-3200 Simplex Fiber Optic Cables and HFBR-3300 Duplex Fiber Optic Cables are intended for use with HP's High Performance Modules (HFBR-1001/2, HFBR-2001) and the Miniature Link series of transmitters and receivers (HFBR-12XX, HFBR-22XX).

The HFBR-3200 Simplex Fiber Optic Cable is constructed of a single graded index glass fiber surrounded by a silicone buffer, secondary jacket, and aramid strength members. The combination is covered with a scuff resistant polyurethane outer jacket.

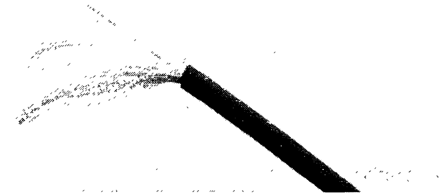
The HFBR-3300 Duplex Fiber Optic cable has two glass fibers, each in a cable of construction similar to the Simplex cable, joined with a web. The individual channels are identified by a marking on one channel of the cable.

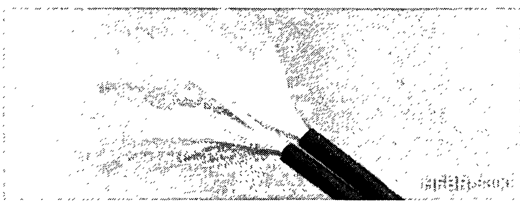
The optical waveguide is a fused silica glass, graded index fiber, which gives low attenuation and wide bandwidth. The silicone buffer and secondary jacket protect the fiber from being scratched and provide a base for the helically wrapped aramid strength members.

The HFBR-3200 and HFBR-3300 cables can be terminated with HFBR-4000 connectors using the HFBR-0100 Connector Assembly Tooling Kit. Information on cables with factory installed connectors is available in the HFBR-3000/HFBR-3100 data sheet.

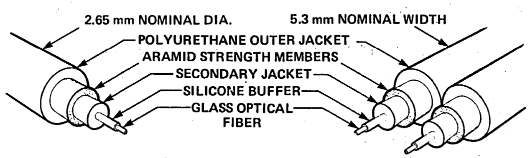
The cable's resistance to mechanical abuse, safety in flammable environments, and immunity from electromagnetic interference effects may make the use of conduit unnecessary. However, the light weight and high strength of the cables allows them to be drawn through most electrical conduits.

*UL File Number E84364





Fiber Optic Cable Construction



SIMPLEX DUPLEX

CABLE LENGTH TOLERANCE

Cable Length (Metres)	Tolerance
1-10	+10/-0 %
11-100	+1/-0 Metre
> 100	+1/-0 %

Installation

Hewlett-Packard Fiber Optic cable is designed so that when pulled through conduit, accepted wire pulling methods and tools, such as a cable grip, can be used. However, a few precautions for optical cable are necessary: the cable must not be bent tighter than its minimum bend radius; the tensile strength of the cable should not be exceeded (a cable lubricant can be used to minimize the drawing force); tensile load should be applied only to the cable and not the connector.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Relative Humidity at $T_A = 70°C$			95	%	
Storage Temp.	T_S	-40	+85	°C	
Operating Temp.	T_A	-20	+85	°C	
Bend Radius, No Load	r	20		mm	8, 9
Flexing		50K		Cycles	1

Parameter	Symbol	Min.	Max.	Units	Note
Crush Load	F_C		200	N	2, 7
Impact	m		1.5	kg	3
	h		0.15	m	
Tensile Force Per Cable Channel	F_T		300	N	7, 8

Mechanical/Optical Characteristics -20° C to +85° C Unless Otherwise Specified.

Parameter		Symbol	Min.	Typ.[6]	Max.	Units	Conditions	Fig.	Note
Exit Numerical Aperture		N.A.		0.3		—	$\lambda = 820$ nm, $\ell \geq 300$m		4
Attenuation		α_O	3.5	5.5	8	dB/km	$\lambda = 820$ nm	1	11
Bandwidth @ 1 km		BW		40		MHz	$\lambda = 820$ nm (LED)		5
Travel Time Constant		l/V		5		ns/m	$\lambda = 820$ nm		10
Optical Fiber Core Diameter		D_C		100		μm			
Cladding Outside Diameter		D_{CL}		140		μm			
Index Grading Coefficient		g		2		—			
Cable Structural Strength		F_C		1800		N			7
Mass per Unit Length	Single Channel	m/ℓ		6		kg/km			
	Dual Channel			12					
Cable Leakage Current		I_L		30		nA	50 kV, $\ell = 0.3$m		

Notes:
1. 180° bending at minimum bend radius, with 10N tensile load.
2. Force applied on 2.5 mm diameter mandrel laid across the cable on a flat surface, for 100 hours, followed by flexure test.
3. Tested at 1 impact according to DOD-STD-1678, Method 2030, Procedure 1.
4. Exit N.A. is defined as the sine of the angle at which the off-axis radiant intensity is 10% of the axial radiant intensity.
5. Bandwidth is measured with a pulsed LED source ($\lambda = 820$ nm), and varies as $\ell^{-0.85}$, where ℓ is the length of the fiber (km). Pulse dispersion and bandwidth are approximately inversely related.
6. Typical values are at $T_A = 25°C$.
7. One Newton equals approximately 0.225 pounds force.
8. Short term, ≤ 1 hr.
9. The probability of a fiber weak point occurring at a point of maximum bend is small, consequently the risk of fiber breakage from exceeding the maximum curvature is extremely low.
10. Travel time constant is the reciprocal of the group velocity for propagation of optical power. Group velocity, $V = \lambda/n$ where λ = velocity of light in space = 3×10^8 m/s, n = effective core index of refraction.
11. For lower attenuation cable consult your local sales office.

Cable Ordering Guide

HFBR-3200/HFBR-3300 defines fiber optic cables of user specified length. The cable length must be specified in metres and can be any length in one metre increments from 1 to 1000 metres (longer cables available upon request). Option 001 specifies the number of equal length cables ordered.

Examples:

A. To order one Duplex Cable 150 metres long specify:

HFBR-3300	Quantity 150
OPT 001	Quantity 1

B. To order five Simplex Cables, 100 metres each, specify:

HFBR-3200	Quantity 500
OPT 001	Quantity 5

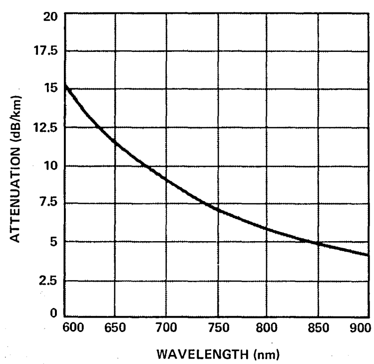


Figure 1. Typical Cable Attenuation vs. Wavelength

FIBER OPTICS

HEWLETT PACKARD

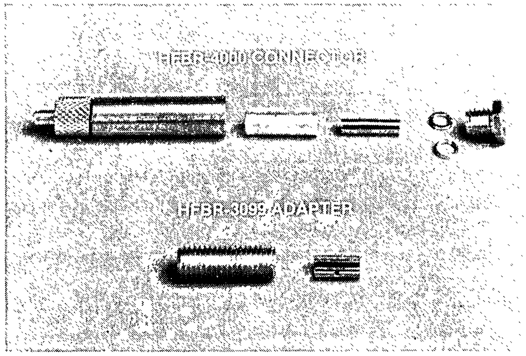
FIBER OPTIC CONNECTOR

HFBR-4000 CONNECTOR
HFBR-3099 ADAPTER

TECHNICAL DATA JANUARY 1986

Features

- **TERMINATES HEWLETT-PACKARD 100/140 μm FIBER OPTIC CABLE**
- **TYPICAL INSERTION LOSS 1.5 dB**
- **ALL METAL PIECE-PARTS**
- **SIMPLE, RAPID ASSEMBLY**
- **STANDARD 2.50 mm FERRULE**
- **WIDE OPERATING TEMPERATURE RANGE**
- **SMALL DIAMETER**



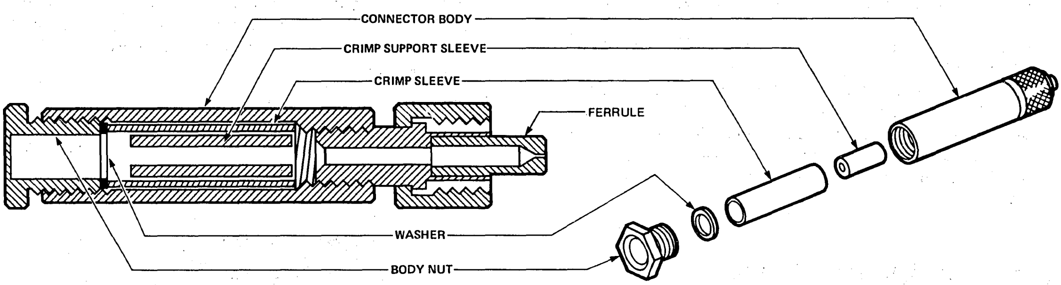
Description

The HFBR-4000 Fiber Optic Connector is constructed of all metal piece-parts and has been designed to use a high performance epoxy to stake the optical fiber. The standard, 2.50 mm connector ferrule is prepared with a polished optical surface giving the assembly a uniformly repeatable low insertion-loss of typically 1.5 dB.

The connector can be assembled in less than 20 minutes by an experienced user with suitable tooling, such as provided in the Hewlett-Packard HFBR-0100 Connector Assembly Tooling Kit. When properly assembled, the connector has excellent strength and repeatable performance over a wide temperature range.

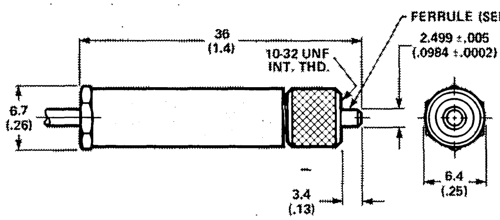
The connector is compatible with Hewlett-Packard HFBR-3200/3300 Fiber Optic Cables.

The HFBR-3099 adapter is used for making an aligned, easily disassembled, connector-to-connector junction.



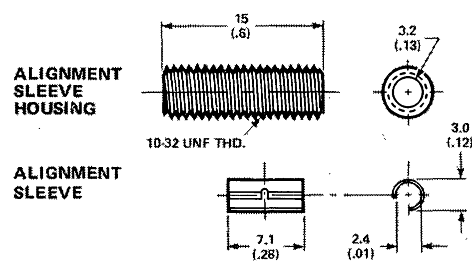
CONNECTOR ASSEMBLY

Mechanical Details



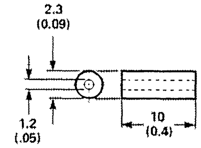
NOTES: 1. Dimensions are in mm (inches).
2. Unless otherwise specified. The tolerances are:
.X ± .51mm, (.XX ± .02in.)
.XX ± .13mm, (.XXX ± .005in.)
3. Ferrule hole accomodates 140μm O.D. fiber.

ASSEMBLED HFBR-4000 CONNECTOR

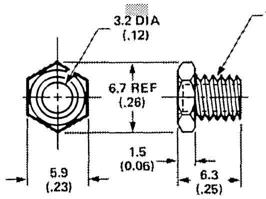


HFBR-3099 ADAPTER

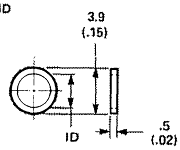
Connector Piece-Parts



CRIMP SUPPORT SLEEVE

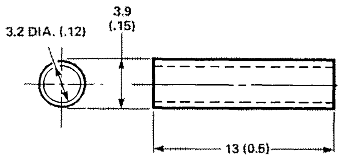


BODY NUT

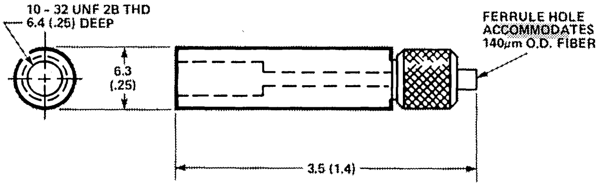


ID:
GOLD COLORED: 3.2 (.12) SILVERED COLORED: 2.8 (.10)

WASHER



CRIMP SLEEVE



CONNECTOR BODY

NOTES: 4. DIMENSIONS IN mm (in.)
5. TOLERANCES ARE:
.x .51mm .xx .12mm
(.xx .02in.) (.xxx .005in.)

Absolute Maximum Ratings

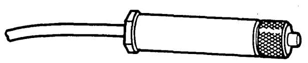
Parameter	Symbol	Min.	Max.	Units	Note
Storage Temp.	T_S	-40	+85	°C	7
Operating Temp.	T_A	-20	+70	°C	7
Tensile Force	F_T		100	N	7

6. α_{CC}, connector-to-connector loss; measured steady state.
7. When assembled with Hewlett-Packard HFBR-0100 procedure and HFBR-3000 series glass fiber cable.
8. 100 connection cycles.

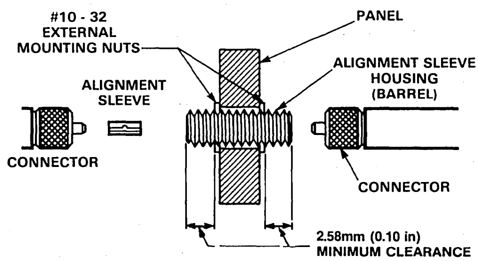
Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Insertion Loss	α_{CC}		1.5		dB	6,7
Insertion Loss Repeatability	$\Delta\alpha_{CC}$		0.2		dB	8

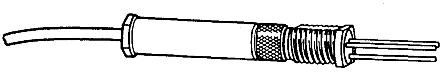
Applications



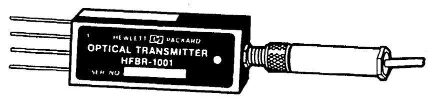
- **TERMINATION FOR HEWLETT-PACKARD HFBR-3200/3300 FIBER OPTIC CABLE**



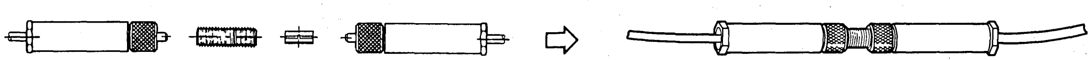
- **BULKHEAD OR PANEL MOUNTING OF HFBR-4000 CONNECTORS**



- **INTERFACE TO HEWLETT-PACKARD HFBR-12XX/22XX MINIATURE FIBER OPTIC LINK COMPONENTS**



- **INTERFACE TO HEWLETT-PACKARD HFBR-1001/1002/2001 FIBER OPTIC MODULES**



- **CONNECTOR-TO-CONNECTOR INTERFACE**

FIBER OPTICS

HEWLETT PACKARD

FIBER OPTIC CONNECTOR ASSEMBLY TOOLING KIT

HFBR-0100 TOOLING KIT

HFBR-0101 CONSUMABLES KIT

HFBR-0102 CUSTOM TOOLS

TECHNICAL DATA JANUARY 1986

Features

- **AIDS IN THE ASSEMBLY AND REPAIR OF HEWLETT-PACKARD 100/140 μm FIBER OPTIC CABLE WITH HEWLETT-PACKARD CONNECTORS**
- **INCLUDES AN ILLUSTRATED, STEP-BY-STEP TUTORIAL USER'S MANUAL**
- **PRODUCES FACTORY-QUALITY CONNECTIONS; 1.5 dB Typical Insertion Loss**
- **COMPLETE — INCLUDES ALL TOOLS, MATERIALS AND CONNECTOR PARTS REQUIRED TO ASSEMBLE 10 CONNECTORS**
- **RAPID, LESS THAN 20 MINUTE CONNECTOR ASSEMBLY TIME WITH EXPERIENCE**
- **PACKAGED IN A RUGGED CASE**

Description

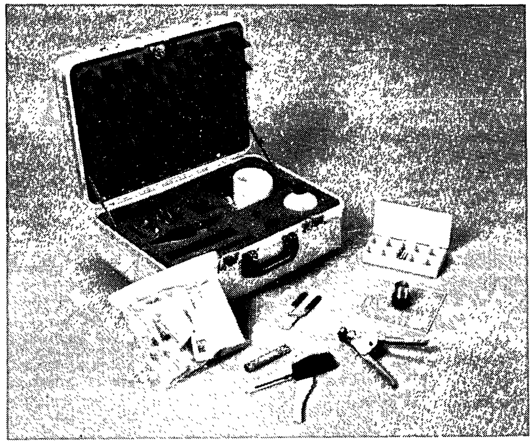
The HFBR-0100 Fiber Optic Connector Assembly Tooling Kit is a complete kit designed for quick field installation of Hewlett-Packard HFBR-4000 connectors onto Hewlett-Packard HFBR-3200/3000 Fiber Optic Cable. The kit is packaged in a rugged case, supplying the user with everything required for terminating the fiber optic cable. The contents are:

1. A set of common connectoring tools
2. A consumables kit containing sufficient material to assemble ten fiber optic connectors (available separately as HFBR-0101).
3. A set of custom tools (available separately as HFBR-0102).
4. A set of connector piece-parts for terminating ten connector ends, and adapters for making connector-to-connector junctions (the individual unassembled connectors are available as HFBR-4000; the adapter is available as HFBR-3099).
5. An illustrated user's manual presenting the procedure in a step by step, tutorial fashion.

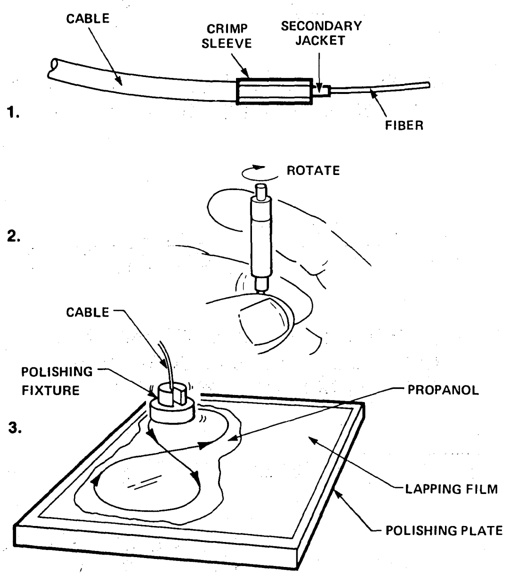
User's Manual Outline

The User's Manual details the connectoring procedure for the first time user, allowing an inexperienced technician to construct factory-quality fiber optic connectors. Numerous photographs and diagrams simplify the assembly process.

The User's Manual is composed of three major sections, described as follows:



1. CABLE PREPARATION: The fiber optic cable is stripped of its jackets, and the strength members are terminated by the installation of crimp hardware.
2. CONNECTOR ASSEMBLY: The prepared cable end is assembled into the connector body using a high performance epoxy to stake the optical fiber. The epoxy is cured in ten minutes using the supplied heater.
3. CONNECTOR POLISHING: The fiber end is ground to an optically flat finish and inspected with a microscope comparing the finish with the detailed photomicrographs in the User's Manual.



HFBR-0100 Materials List

1. COMMON CONNECTORING TOOLS WITH CASE
   - Sapphire Ribbon Cleave Tool
   - No-Nik™ Strippers
   - Scissors
   - 50X Microscope
   - Safety Glasses
   - 16 AWG Wire Strippers
   - Crimping Tool
   - Polishing Plate
   - Heater:
     (option 001) 100-120 VAC 50/60 Hz
     (option 2XX) 200-240 VAC 50/60 Hz
2. TEN HFBR-4000 CONNECTORS WITH SIX HFBR-3099 ADAPTERS
3. HFBR-0101 CONSUMABLES KIT
   - Hysol™ 1C Epoxy
   - Propanol/Acetone swabs
   - Loctite™ 495 Adhesive
   - Stirring Sticks
   - Syringes with Flat-tipped Needles
   - Hand Towels
   - Propanol
   - Lapping Film:
     — Coarse grit, 12 micron
     — Medium grit, 3 micron
     — Fine grit, 0.5 micron
   - Bottle Spout
   - Mixing Pads
4. HFBR-0102 CUSTOM TOOLS
   - Slotted Vise
   - Polishing Weight
   - Polishing Assembly
5. USER'S MANUAL

Specifications

Parameter		Value	Units
Weight	Net	7.3 (16)	kg (lbs)
	Shipping	8.2 (18)	
Size	Height	356 (14)	mm (in.)
	Width	457 (18)	
	Depth	229 (9)	
Heater Wattage	Opt 001	600	W
	Opt 2XX	80	

Ordering Guide

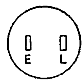
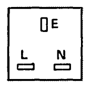
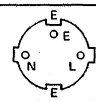
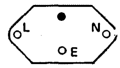
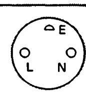
The HFBR-0100 Connector Assembly Tooling Kit is designed to be sold as a complete unit, ready for use. Common connectoring tools, consumables, custom tools, connector piece-parts, and the user's manual are included.

The kit is ordered by specifying both the base product number (HFBR-0100) and a heater option. The heater option specifies either a 110 VAC (option 001) or a 220 VAC (option 2XX) heater with the appropriate power cord.

Both the Consumables Kit (HFBR-0101) and the Custom Tools (HFBR-0102) are available separately for restocking the kit. The unassembled connectors (HFBR-4000), adapters (HFBR-3099) and fiber optic cable (HFBR-3200/3300) are also available.

Order Examples:
1. Three Connector Assembly Tooling Kits — specify;
   HFBR-0100 Fiber Optic Connector Assembly Tooling Kit — Quantity 3
   Option 202: European Continent Plug, 220 VAC
2. One Consumables Kit replacement — specify;
   HFBR-0101 Consumables Kit — Quantity 1

POWER CORD (MALE PLUG) OPTIONS

OPTION NO.	PLUG* CONFIGURATION	COUNTRY
001		USA, CANADA (120V) JAPAN
200		U.K.
201		AUSTRALIA, NEW ZEALAND
202		EUROPEAN CONTINENT
206		SWITZERLAND
212		DENMARK

*VIEW OF PLUG FACE

E – EARTH OR SAFETY GROUND
N – NEUTRAL OR IDENTIFIED CONDUCTOR
L – LINE OR ACTIVE CONDUCTOR

HEWLETT PACKARD

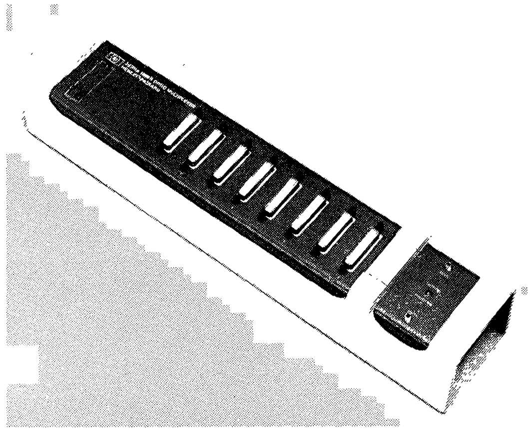
RS-232-C/ V.24 TO FIBER OPTIC MULTIPLEXER

39301A

TECHNICAL DATA JANUARY 1986

Features

- EXTEND UP TO 16 RS-232-C/V.24 CHANNELS TO 1.25 km STANDARD, 2.5 km WITH SELECTED CABLE
- DATA UP TO 19.2 kbps ON EACH OF 16 CHANNELS SIMULTANEOUSLY
- SYSTEM IMMUNITY TO EMI SOURCES SUCH AS LIGHTNING STRIKES
- SECURE DATA TRANSMISSION
- ELIMINATION OF SPARK HAZARDS IN VOLATILE ATMOSPHERES
- BUILT-IN FAULT ISOLATION CAPABILITY
- LOW INSTALLATION COSTS DUE TO LIGHTWEIGHT FIBER OPTIC CABLE



Description

A pair of HP 39301A Multiplexers interconnected with Hewlett-Packard HFBR-3000 Series Fiber Optic Cable, may be used to extend up to 16 full duplex RS-232-C/V.24 channels up to 2.5 km (8200 ft.). Figure 1 shows a typical link configuration between a host CPU and a cluster of 16 terminal devices.

This link provides an easy way to incorporate the advantages of fiber optic links into local area terminal communications. These advantages include immunity to electromagnetic interference of all types, from lightning strikes to noisy electric motors, and freedom from static discharge and crosstalk. The fiber optic cable also provides security for data as it will not radiate electromagnetic signals. In volatile atmospheres, there is no need for special cable

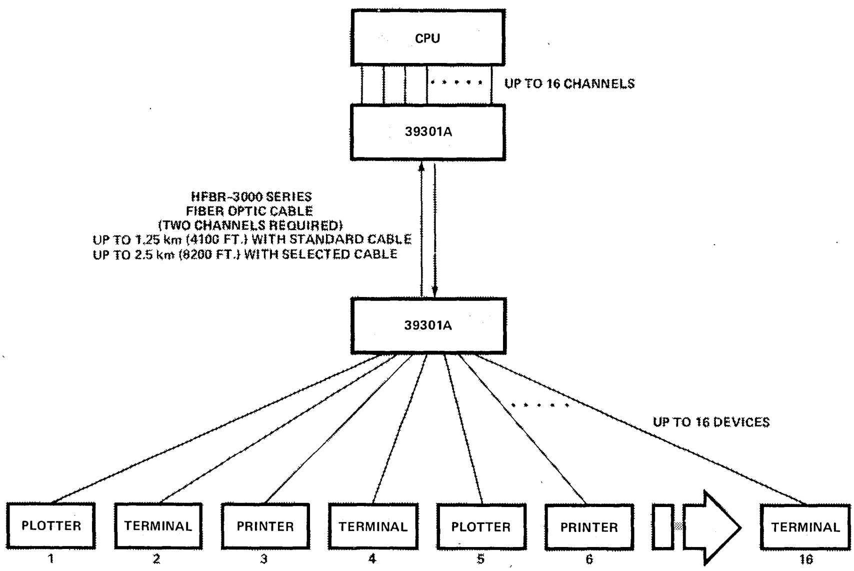


Figure 1. Typical Link Configuration

shielding because no sparks can be generated by this totally dielectric medium.

Each 39301A Multiplexer has eight RS-232-C/V.24 connectors. Each connector has both the Primary and Secondary Data channels available. This provides for a variety of possible configurations. These configurations include: sixteen independent asynchronous channels, eight independent asynchronous channels with handshake control lines, or eight independent synchronous channels with Data Terminal Equipment (DTE) supplied clock signals. The cables required to accomplish any combination of these connections are described in the Typical Configurations Section of this Data Sheet.

Each of the Primary and Secondary Data channels may operate any asynchronous protocol up to 19200 bps. Each channel may be used independently with different protocols and data rates without adjustments to the Multiplexer. This is possible because the 39301A operates as a time division multiplexer, sampling each of the 16 data channels at a 200 kHz rate. This sampled data is serialized and transmitted in real time at a rate of 7 Mbaud over the interconnecting HFBR-3000 Series Fiber Optic Cable to the companion 39301A. This serial data is then reconverted to 16 parallel channels and distributed to the respective Primary or Secondary Data channels.

Specifications

SYSTEM PERFORMANCE

A system consists of two or more 39301A's interconnected by fiber optic cable assemblies.

Transmission Distance: The usable distance between 39301A's is determined by the optical fiber and connectors used.

Typical Fiber Specifications Size, α_0, N.A.	Connector Mfr./Model	Distance Max.	Typ.
Local Communication Fiber 100/140 μm, 5.5 dB/km, 0.28	HP/HFBR-4000 Amphenol/ 906-120-5000	1.25 km Note 1, 2	2.5 km
Telecommunication Fiber 50/125 μm, 4 dB/km, 0.21	Amphenol/ 906-120-5001	Note 2	1.5 km

NOTES:
1. Guaranteed with HFBR-3000 Series cable assemblies.
2. Contact HP Sales Office for expected performance of specific fiber and connectors used.

System Bit Error Rate: One error in 10^9 bits typical.

ENVIRONMENTAL

Storage Temperature: -40° C to +75° C
Operating Temperature: 0° C to +55° C
Relative Humidity: 95%

PHYSICAL CHARACTERISTICS

Size: 42.5 x 8.9 x 7.2 cm
(16.75 x 3.5 x 2.85 inches)
Weight: 2.2 kg (4.75 lbs)
Shipping Weight: 3.4 kg (7.5 lbs)
Power Requirements: 18 VA Maximum
Power Cord Length: 2.3 m (7.5 ft.)

REGULATION COMPLIANCE

RFI/EMI:
- VDE 0871 level A
- FCC Class A

Safety Approvals:
- UL478, UL114 for EDP and office equipment
- CSA C22.2-154 for EDP equipment
- VDE 0730 part 2P for EDP and office equipment
- Complies with IEC standard #380 and #435 for EDP and office equipment

ELECTRICAL CHANNEL INTERFACE

Electrical: Conforms to EIA standard RS-232-C Section 2 (CCITT V.24) for the assigned pins.

Pulse Width Distortion: +/− 6 μs maximum at data rates to 19.2 kbps
(Operated with RS-232-C load of 3K ohms and 2500 pF).

Electrical Connector: Female 25 pin subminiature "D"

PIN ASSIGNMENTS

Pin No.	EIA RS-232-C		CCITT V.24		Notes
1	Protective Ground	AA	Earth Common	101	1
2	Transmitted Data (Primary)	BA	Transmitted Data	103	3
3	Received Data (Primary)	BB	Received Data	104	4
6	Data Set Ready	CC	Data Set Ready	107	2
7	Signal Ground	AB	Signal Ground	102	1
14	Secondary Transmitted Data	SBA	Transmitted Backward Channel Data	118	3
16	Secondary Received Data	SBB	Received Backward Channel Data	119	4

Notes:
1. Pins 1 and 7 are internally connected.
2. Pin 6 is internally hardwired "on" to +12V through a 316 ohm resistor.
3. Data to 39301A.
4. Data from 39301A.

OPTICAL CHANNEL INTERFACE

Transmitter Optical Output Flux: −13 dBm (50 μW) minimum at 820 nm

Receiver Optical Input Flux: -31 dBm (0.8 μW) minimum at 820 nm

Fiber Optic Port Connector: HFBR-4000 compatible. (HFBR-4000 installed on HFBR-3000 Series Fiber Optic Cables. Optional SMA style connector adapters are available from HP sales offices.)

INDICATORS AND SWITCHES

AC Line Indicator: When ON indicates that AC power is on.

Carrier Received Indicator: When ON, indicates that the 39301A is receiving a modulated signal from the remote transmitter.

Loopback Switch: In the TEST position, enables an electrical loopback at the interface between the multiplexer electronics and the fiber optic transceiver circuitry. The "Carrier Received Indicator" is disabled when this switch is in the TEST position.

DTE Interface Configurations

Each RS-232-C/V.24 connector on the 39301A Multiplexer can be interfaced to a variety of Data Terminal Equipment (DTE) by use of properly configured interconnecting RS-232-C/V.24 data cables. Each connector provides two independent full duplex asynchronous channels on the Primary and Secondary Data lines. Therefore, 16 total channels are available on any 39301A link. The following figures will describe the cable configurations for four typical DTE connections. Only one end of the full 39301A link is shown in each figure. The opposite end will be a mirror image in all cases, therefore, two of the illustrated RS-232-C/V.24 data cables will be required to complete each link. Shielded RS-232-C/V.24 cables are recommended in all cases to minimize radio frequency emissions. Any of the DTE configurations described may be intermixed and connected to a 39301A link simultaneously with the only limitation being that no more than 16 full duplex channels are available.

ASYNCHRONOUS DATA ONLY DTE

It is possible to connect one or two "Data Only" DTEs to each connector on the 39301A. Figure 2 shows the configuration for a single DTE connection utilizing the Primary Transmitted/Received Data pins on the 39301A connector. Figure 3 shows the configuration of HP's 8120-3569 Dual Channel RS-232-C/V.24 Adapter Cable. This 8120-3569 Cable can be used to separately access both the Primary and Secondary Data channels on each 39301A connector. Then two of the cables shown in Figure 2 can be used to extend these channels out to two separate "data only" DTEs. This 8120-3569 Cable will enable up to 16 "data only" DTEs to be connected to each 39301A link.

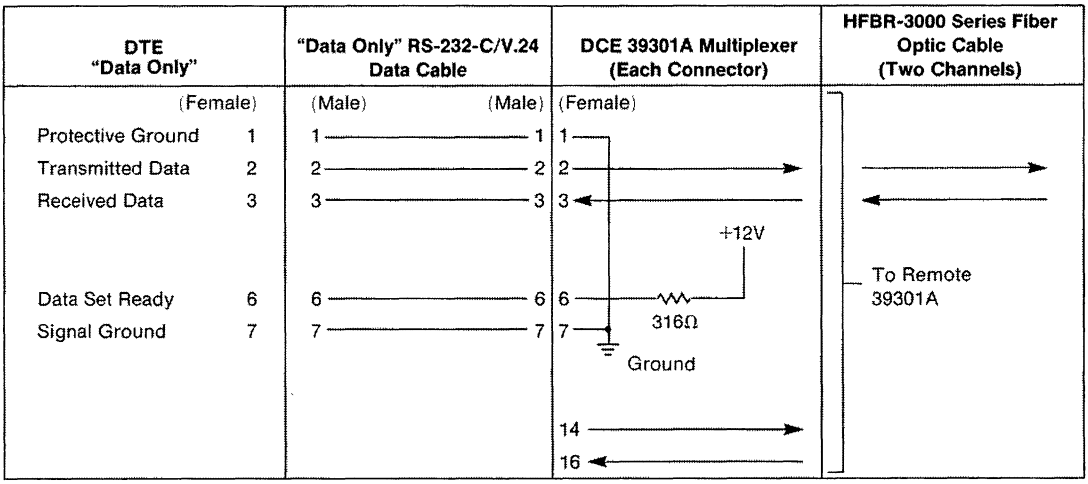
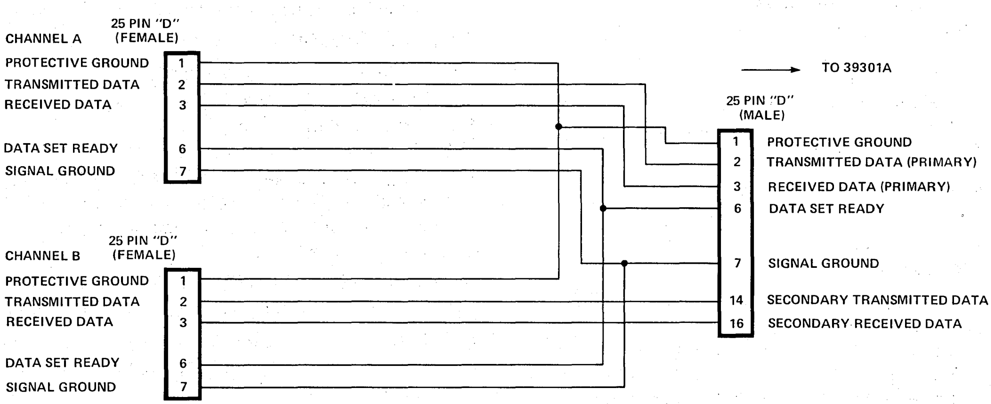


Figure 2. Asynchronous Data Only Configuration



NOTE: THE SEPARATION BETWEEN MALE AND FEMALE CONNECTORS IS 0.6m (2 ft).

Figure 3. 8120-3569: Dual Channel RS-232-C/V.24 Adapter Cable

ASYNCHRONOUS DATA PLUS HANDSHAKE DTE

If a DTE requires that normal modem handshake lines be active for control purposes, the Secondary Data channel on each 39301A connector can be used to establish this connection between the host CPU and the remote terminal. Figure 4 shows one possible cable configuration using the Secondary Data channel to interconnect the DTE's Request to Send/Clear to Send handshake lines. Up to eight DTEs with handshake lines may be connected to a 39301A link in this way.

Note that pin 6, Data Set Ready, on each 39301A connector is hardwired "on" to +12V through a 316 ohm resistor. If the connected DTE does not require this signal, it may be eliminated from the RS-232-C/V.24 data cable.

SYNCHRONOUS DATA WITH DTE SUPPLIED CLOCK

Although the 39301A does not provide a clock for synchronous data transmission, synchronous DTE may be interconnected by the 39301A link if the DTE can supply the necessary clock signal. Figure 5 illustrates the use of a 39301A connector's Secondary Data channel to accomplish this type of DTE connection. Up to eight synchronous data DTEs with their own clock lines may be connected to a 39301A link.

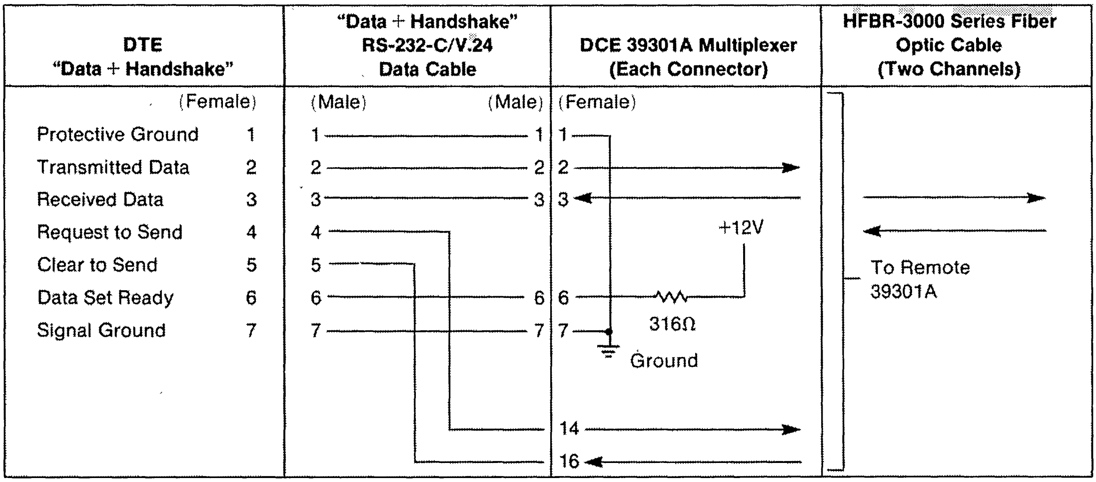


Figure 4. Asynchronous Data Plus Handshake Configuration

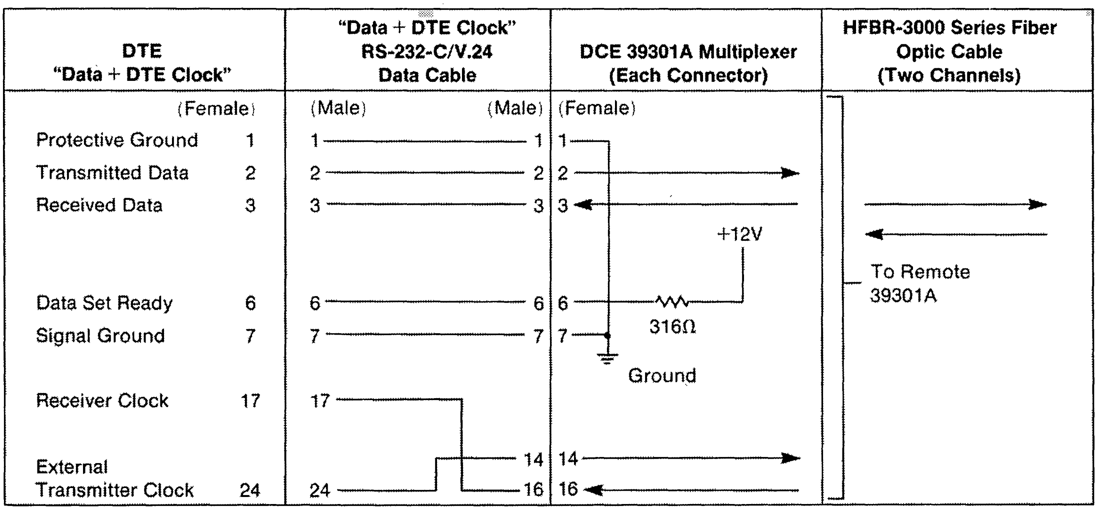


Figure 5. Synchronous Data with DTE Supplied Clock Configuration.

System Configurations

Point-to-Point: See Figure 1

The 39301A's can be configured in a normal point-to-point fashion utilizing a two channel fiber optic cable assembly to interconnect them.

Multiple Node Loop:

Several 39301A's can be interconnected in a simple closed loop configuration using single channel fiber optic cable assemblies to interconnect the transmitter of each 39301A to the receiver of the subsequent 39301A. This configuration allows one multiplexer at the computer center to address several different groups of terminals at different locations in a local facility. A maximum of 16 asynchronous "Data Only" DTE connections can be made around the loop. The unused channels at each multiplexer must be externally looped back on the 25 pin connectors, (i.e., tie pins 2 to 3 and 14 to 16). The maximum data rate of any channel in the loop is determined by the number of multiplexers in the loop and the amount of distortion that the interconnected DTE's can tolerate.

Number of 39301A's	Maximum Channel Data Rate
Up to 3	19.2 Kbps
Up to 6	9.6 Kbps
Up to 15	4.8 Kbps

This data rate limit is due to the accumulated distortion thru the loop. The accumulated distortion will be within the 25% limits of EIA Standard RS-404, Standard for Start-Stop Signal Quality Between Data Terminal Equipment and Non-Synchronous Data Communications Equipment.

Installation

The 39301A Multiplexer and the interconnecting HFBR-3000 Series Fiber Optic Cable is designed for easy installation. Complete details are provided in the Installation, Operating, and Service Manual supplied with each 39301A.

It is recommended that the 39301A Multiplexer be securely mounted to protect the attached data cables. The 39301A is designed for surface or EIA standard 19 inch width rack mounting. Standard Rack/Surface Mounting Hardware supplied with each 39301A allows installation in a standard open rack or flush mounting on any convenient flat surface. Optional Recessed Rack Mounting Hardware (Option 001) allows mounting inside standard racks with closed doors without damage to the attached cables.

The HFBR-3000 Series Fiber Optic Cable required to interconnect the 39301A Multiplexers is available in several configurations. These configurations are detailed in the Support Products Section of this Data Sheet. Two channels of this cable are required to operate the link. This cable is suitable for installation in cable trays, conduits and ducts. The cable will operate in environments from -20°C to +70°C and 95% Relative Humidity. Standard cable installation techniques and equipment may be used with the minor precautions stated in the 39301A Installation, Operating, and Service Manual. The precautions include maintaining the minimum bend radius of 25mm (1 in.) and maximum tensile load of 300N (67 lb) per channel during installation.

If junction box or bulkhead splices are required in a cable run, or a link is reconfigured to a longer distance requiring additional fiber optic cable to be added to the original installation, HFBR-3099 Cable Coupling Hardware may be used to splice these cables together. The HFBR-3099 is supplied with each factory connectored HFBR-3000 Series Cable or may be ordered separately. Each in-line HFBR-3099 Coupler produces a 2 dB optical power loss in the cable run. This loss will affect the maximum separation between 39301A's by the distance equal to 2 dB ÷ cable attenuation in dB/km. For example, if standard HFBR-3000 series cable is used the maximum link length will be reduced by 2 dB ÷ 8 dB/km = 250 m for each intermediate HFBR-3099 used.

The RS-232-C/V.24 data cables required for connection to various Data Terminal Equipment are detailed in the Typical Configurations Section of this Data Sheet. It is recommended that shielded cables are used for these connections for maximum suppression of radio frequency emissions. These cables should be no longer than 15m (50 ft.) for compliance with the EIA and CCITT Standards, unless low capacitance cable is used.

Service

The 39301A is designed with easy-to-use link fault isolation facilities. Loopback techniques utilizing the built-in loopback switch and fiber optic loopback cable supplied with each 39301A Multiplexer are used to quickly isolate link failures to either 39301A Multiplexer, the HFBR-3000 Series Fiber Optic Cable, or the interconnected Data Terminal Equipment. These procedures are described in the Installation, Operating, and Service Manual supplied with each 39301A. 39301A Multiplexers or HFBR-3000 Series Fiber Optic Cables may be self-serviced by the customer or returned to the nearest Hewlett-Packard Sales Office for service.

Customer self-service may be accomplished for the Multiplexer by following the procedures outlined in the Installation, Operating and Service Manual to identify the failed subassembly. Replacement subassemblies are available through HP Sales Offices. HFBR-3000 Series Fiber Optic Cables may be repaired by using the HP HFBR-0100 Connector Assembly Tool kit to splice or reconnector a damaged cable.

Hewlett-Packard service is available for the 39301A by returning the Multiplexer to the nearest HP Sales Office. This service is available either on Monthly Contract basis or for a Time and Materials charge. The HFBR-3000 Series Cable will be repaired on a Time and Materials basis upon return to the nearest HP Sales Office.

Support Products for the 39301A

39301A MOUNTING HARDWARE

Rack/Surface Mounting Hardware:
Supplied standard with each 39301A. Available separately as part 1600-1090.

Recessed Rack Mounting Hardware:
Supplied as Option 001 to the 39301A. Available separately as part 1600-1092.

39301A FIBER OPTIC LOOPBACK CABLE

Supplied standard with each 39301A. Available separately as part 5061-2694.

39301A INSTALLATION, OPERATING, AND SERVICE MANUAL

Supplied standard with each 39301A. Extra copies available as part 39301-90001.

8120-3569 DUAL CHANNEL RS-232-C/V.24 ADAPTER CABLE

Enables two Data Terminal Equipment devices to be connected to each 39301A RS-232-C/V.24 connector port. A wiring diagram is shown in Figure 3 of this Data Sheet. The length is 0.6m (2 ft.)

HFBR-3000* SERIES FIBER OPTIC CABLE

	Single Channel (Two Req.) OR	Dual Channel (One Req.)
With Factory Installed HFBR-4000 Fiber Optic Connectors	HFBR-3000* or 39200A*	HFBR-3100* or 39200B*
Without Factory Installed Connectors	HFBR-3200*	HFBR-3300*

Two channels of HFBR-3000 Series Fiber Optic Cable are required to interconnect the HP 39301A Multiplexers. This cable is available in several forms as shown in the table above. It may be ordered in any length in one metre increments up to 1000 metres (3280 ft.)

*Detailed specifications for these products are available from HP sales offices.

HFBR-0100* CONNECTOR ASSEMBLY TOOLING KIT

This kit allows the installation of HFBR-4000 Fiber Optic Connectors onto HFBR-3000 Series Fiber Optic Cables in the field. It is used for system installation purposes if HFBR-3200/3300 unconnectored cables are used. It may also be used for field repair of HFBR-3000 Series Fiber Optic Cables.

HFBR-4000* FIBER OPTIC CONNECTORS

These connectors are compatible with the HFBR-3000 Series Fiber Optic Cable and the fiber optic ports on the 39301A.

HFBR-3099* FIBER OPTIC CABLE COUPLING HARDWARE

This hardware enables two cables with HFBR-4000 connectors to be coupled together for link extension or repair splices. See Installation Section of this Data Sheet for limitations on use of the HFBR-3099.

Ordering Information

HP 39301A: RS-232-C/V.24 TO FIBER OPTIC MULTIPLEXER

Two are required per link. Each 39301A is supplied with standard Rack/Surface Mounting Hardware, a Fiber Optic Loopback Cable and an Installation, Operating, and Service Manual.

Option 001: Recessed Rack Mounting Hardware

Required Power Supply Option: One required per 39301A

Option 210: 100V 50/60Hz Operation
Option 212: 120V 50/60Hz Operation
Option 222: 220V 50/60Hz Operation
Option 224: 240V 50/60Hz Operation

8120-3569: DUAL CHANNEL RS-232-C/V.24 ADAPTER CABLE

This cable may be used to separately access both Primary and Secondary Data channels on each 39301A connector. Eight of these cables will enable up to 16 "data only" DTE to be connected to each 39301A.

HFBR-3000 SERIES FIBER OPTIC INTERCONNECTING CABLE

Two channels are required per link.

See Support Products Section of this Data Sheet for product choices.

HEWLETT PACKARD

PIN PHOTODIODES

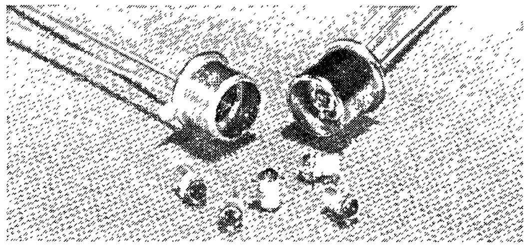
5082-4200 SERIES

TECHNICAL DATA JANUARY 1986

Features

- HIGH SENSITIVITY (NEP <-108 dBm)
- WIDE DYNAMIC RANGE (1% LINEARITY OVER 100 dB)
- BROAD SPECTRAL RESPONSE
- HIGH SPEED (T_r, T_f, EQUALS 1.5 ns TYP.)
- STABILITY SUITABLE FOR PHOTOMETRY/ RADIOMETRY
- HIGH RELIABILITY
- FLOATING, SHIELDED CONSTRUCTION
- LOW CAPACITANCE
- LOW NOISE
- HERMETIC PACKAGE

Active area: 1mm Diam 5082-4207 — Tall (TO-18)
0.5mm Diam 5082-4203, 5082-4204 — Tall (TO-18); 5082-4220 — Short (TO-46)
0.25mm Magnified 2.5x 5082-4205 — Subminiature



Description

The HP silicon planar PIN photodiodes are ultra-fast light detectors for visible and near infrared radiation. Their response to blue and violet is unusually good for low dark current silicon photodiodes.

These devices are suitable for applications such as high speed tachometry, optical distance measurement, star tracking, densitometry, radiometry, and fiber-optic termination.

The low dark current of these planar diodes enables detection of very low light levels. The quantum detection efficiency is constant over ten decades of light intensity, providing a wide dynamic range.

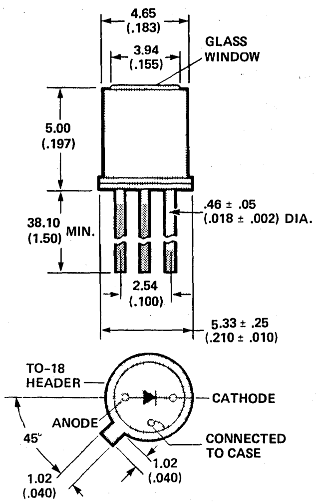
The 5082-4203, -4204, and -4207 are packaged on a standard TO-18 header with a flat glass window cap. For versatility of circuit connection, they are electrically insulated from the header. The light sensitive area of the 5082-4203 and -4204 is 0.508mm (0.020 inch) in diameter and is located 1.905mm (0.075 inch) behind the window. The light sensitive area of the 5082-4207 is 1.016mm (0.040 inch) in diameter and is also located 1.905mm (0.075 inch) behind the window.

The 5082-4205 is in a low capacitance Kovar and ceramic package of very small dimensions, with a hemispherical glass lens.

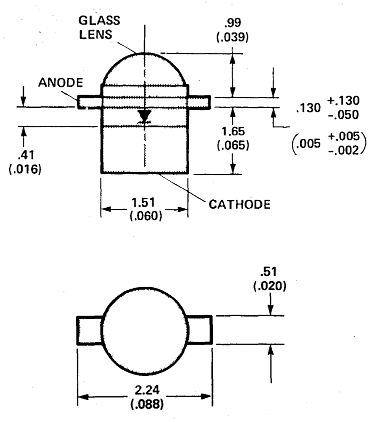
The 5082-4220 is packaged on a TO-46 header with the 0.508mm (0.020 inch) diameter sensitive area located 2.540mm (0.100 inch) behind a flat glass window.

Package Dimensions

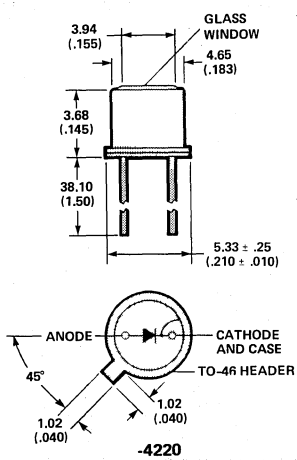
NOTES: 1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED.THE TOLERANCES ARE: .XX ± .13 mm (.XXX ± .005 IN.)



-4203, -4204, -4207



-4205



-4220

Absolute Maximum Ratings Operating and Storage Temperature –55° to 125°C

Parameter	-4203	-4204	-4205	-4207	-4220	Units
P_{MAX} Power Dissipation [1]	100	100	50	100	100	mW
Steady Reverse Voltage [2]	50	20	50	20	50	volts

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	-4203			-4204			-4205			-4207			-4220			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
$R_{E,0}$ = $R_\phi \cdot A$	Axial Incidance Response at 770nm [3]		0.86			0.86			1.1			3.4			.37		$\frac{\mu A}{mW/cm^2}$
A	Active Area [3]		2 x 10^{-3}			2 x 10^{-3}			3 x 10^{-3}*			8 x 10^{-3}			2 x 10^{-3}		cm^2
R_ϕ	Flux Responsivity 770 nm [4] (Fig. 1, 3)		0.43			0.43			.74			0.43			.37		$\frac{\mu A}{\mu W}$
I_D	Dark Current [5] (Fig. 4)			2.0			0.6			.15			2.5			5.0	nA
NEP	Noise Equivalent Power [6] (Fig. 8)		5.9 x 10^{-14}			3.2 x 10^{-14}			1.6 x 10^{-14}			6.6 x 10^{-14}			9.3 x 10^{-14}		$\frac{W}{\sqrt{Hz}}$
D*	Detectivity [7]		7.5 x 10^{11}			1.4 x 10^{12}			3.4 x 10^{12}			1.3 x 10^{12}			4.8 x 10^{11}		$\frac{cm\sqrt{Hz}}{W}$
C_j	Junction Capacitance [8] (Fig. 5)		1.5			2.0			0.7			5.5			2.0		pF
C_P	Package Capacitance [9]		2			2						2					pF
t_r, t_f	Zero Bias Speed (Rise, Fall Time) [10]		300			300			300			300			300		ns
t_r, t_f	Rev.-Bias Speed (Rise, Fall Time) [11]		1.5			1.5			1.5			1.5			1.5		ns
R_S	Series Resistance			50			50			50			50			50	Ω
V_{BR}	Breakdown Voltage	50			50			50			50			50			V

*see Note 4.

NOTES:

1. Peak Pulse Power

   When exposing the diode to high level incidance the following photocurrent limits must be observed:

   $$I_p \text{ (avg MAX.)} < \frac{P_{MAX} - P_\phi}{E_c}\text{; and in addition:}$$

   $$I_{p(PEAK)} < \frac{1000\ A}{t\ (\mu sec)} \text{ or } < 500mA \text{ or } < \frac{I_p \text{ (avg MAX.)}}{f \times t}$$

   whichever of the above three conditions is least.

   I_p - photocurrent (A) f - pulse repetion rate (MHz)
   E_c - supply voltage (V) P_ϕ - power input via photon flux
   t - pulse duration (μs) P_{MAX} - max dissipation (W)

   Power dissipation limits apply to the sum of both the optical power input to the device and the electrical power input from flow of photocurrent when reverse voltage is applied.
2. Exceeding the Steady Reverse Voltage may impair the low-noise properties of the photodiodes, an effect which is noticeable only if operation is diode-noise limited (see Figure 8).
3. The 5082-4205 has a lens with approximately 2.5x magnification; the actual junction area is 0.5 x 10^{-3} cm^2, corresponding to a diameter of 0.25mm (.010"). Specification includes lens effect.
4. At any particular wavelength and for the flux in a small spot falling entirely within the active area, responsivity is the ratio of incremental photodiode current to the incremental flux producing it. It is related to quantum efficiency, η_q in electrons per photon by:

   $$R_\phi = \eta_q \left(\frac{\lambda}{1240}\right)$$

   where λ is the wavelength in nanometers. Thus, at 820nm, a responsivity of 0.43 A/W corresponds to a quantum efficiency of 0.65 (or 65%) electrons per photon.
5. At –10V for the 5082-4204, –4205, and –4207; at –25V for the 5082-4203 and –4220.
6. For (λ, f, Δf) = 820nm, 100Hz, 6Hz) where f is the frequency for a spot noise measurement and Δf is the noise bandwidth, NEP is the optical flux required for unity signal/noise ratio normalized for bandwidth. Thus:

   $$NEP = \frac{I_N/\sqrt{\Delta f}}{R_\phi}$$

   where $I_N/\sqrt{\Delta f}$ is the bandwidth — normalized noise current computed from the shot noise formula:

   $I_N/\sqrt{\Delta f} = \sqrt{2qI_D} = 17.9 \times 10^{-15}\sqrt{I_D}$ $(A/\sqrt{Hz})$ where I_D is in nA.
7. Detectivity, D* is the active-area-normalized signal to noise ratio. It is computed: $D^* = \frac{\sqrt{A}}{NEP}\left(\frac{cm\sqrt{Hz}}{W}\right)$ for A in cm^2, for (λ, f, Δf) = (820nm, 100Hz, 6Hz).
8. At –10V for 5082-4204, –4205, –4207, –4220; at –25V for 5082-4203.
9. Between diode cathode lead and case — does not apply to 5082-4205, -4220.
10. With 50Ω load.
11. With 50Ω load and –20V bias.

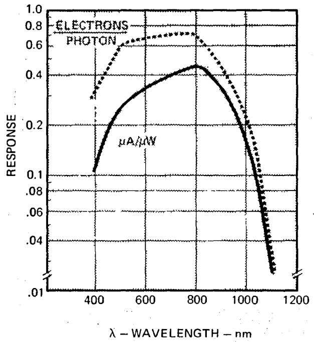


Figure 1. Spectral Response.

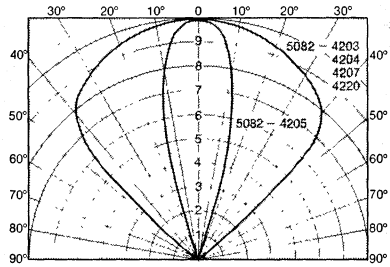


Figure 2. Relative Directional Sensitivity of the PIN Photodiodes.

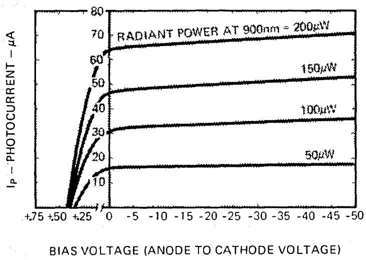


Figure 3. Typical Output Characteristics at λ = 900nm.

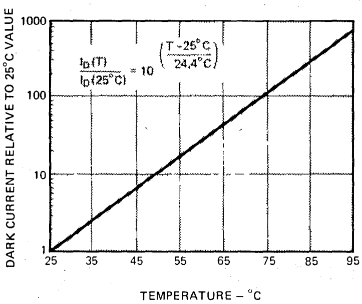


Figure 4. Dark Current at -10V Bias vs. Temperature.

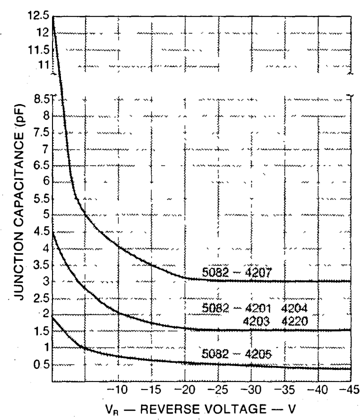


Figure 5. Typical Capacitance Variation With Applied Voltage.

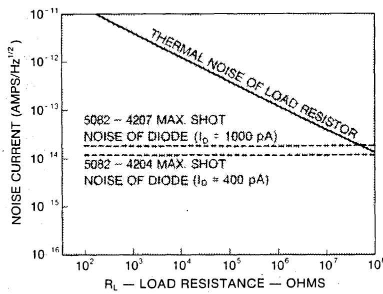


Figure 6. Noise vs. Load Resistance.

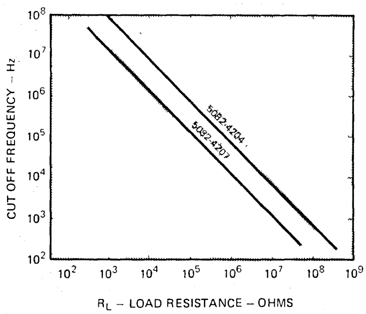


Figure 7. Photodiode Cut-Off Frequency vs. Load Resistance (C = 2pF).

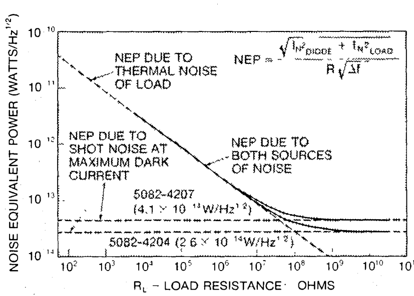


Figure 8. Noise Equivalent Power vs. Load Resistance.

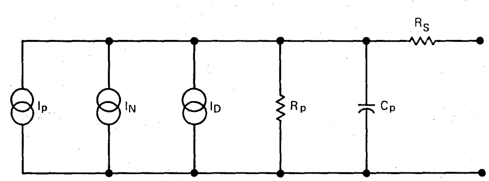


Figure 9. Photodiode Equivalent Circuit.

I_P = Signal current ≈ 0.43 μA/μW x flux input at 820 nm
I_N = Shot noise current
<1.2 x 10^{-14} amps/$Hz^{1/2}$(5082-4204)
<4 x 10^{-14} amps/$Hz^{1/2}$(5082-4207)
I_D = Dark current
<600 x 10^{-12} amps at -10 V dc (5082-4204)
<2500 x 10^{-12} amps at -10 V dc (5082-4207)
$R_P = 10^{11}\Omega$
R_S = <50Ω

Application Information

NOISE FREE PROPERTIES

The noise current of the PIN diodes is negligible. This is a direct result of the exceptionally low leakage current, in accordance with the shot noise formula $I_N = (2qI_R\Delta f)^{1/2}$. Since the leakage current does not exceed 600 picoamps for the 5082-4204 at a reverse bias of 10 volts, shot noise current is less than 1.4×10^{-14} amp $Hz^{-1/2}$ at this voltage.

Excess noise is also very low, appearing only at frequencies below 10 Hz, and varying approximately as 1/f. When the output of the diode is observed in a load, thermal noise of the load resistance (R_L) is $1.28 \times 10^{-10} (R_L)^{-1/2} \times (\Delta f)^{1/2}$ at 25° C, and far exceeds the diode shot noise for load resistance less than 100 megohms (see Figure 6). Thus in high frequency operation where low values of load resistance are required for high cut-off frequency, all PIN photodiodes contribute virtually no noise to the system (see Figures 6 and 7).

HIGH SPEED PROPERTIES

Ultra-fast operation is possible because the HP PIN photodiodes are capable of a response time of 1.5 nanoseconds. A significant advantage of this device is that the speed of response is exhibited at relatively low reverse bias (−10 to −20 volts).

OFF-AXIS INCIDANCE RESPONSE

Response of the photodiodes to a uniform field of radiant incidanceE_e, parallel to the polar axis is given by $I = (RA) \times E_e$ for 820nm. The response from a field not parallel to the axis can be found by multiplying (RA) by a normalizing factor obtained from the radiation pattern at the angle of operation. For example, the multiplying factor for the 5082-4207 with incidance E_e at an angle of 40° from the polar axis is 0.8. If $E_e = 1 mW/cm^2$, then $I_p = k \times (RA) \times E_e$; $I_p = 0.8 \times 4.0 \times 1 = 3.2$ μamps.

SPECTRAL RESPONSE

To obtain the response at a wavelength other than 820nm, the relative spectral response must be considered. Referring to the spectral response curve, Figure 1, obtain response, X, at the wavelength desired. Then the ratio of the response at the desired wavelength to response at 820nm is given by:

$$\text{RATIO} = \frac{X}{.43}$$

Multiplying this ratio by the incidance response at 820nm gives the incidance response at the desired wavelength.

ULTRAVIOLET RESPONSE

Under reverse bias, a region around the outside edge of the nominal active area becomes responsive. The width of this annular g is approximately 25μm (0.001 inch) at −20V, and expands with higher reverse voltage. Responsivity in this edge region is higher than in the interior, particularly at shorter wavelengths; at 400nm the interior, responsivity is 0.1 A/W while edge responsivity is 0.35 A/W. At wavelengths shorter than 400nm, attenuation by the glass window affects response adversely. Speed of response for edge incidance is t_r, $t_f \approx$ 300ns.

5082-4205 MOUNTING RECOMMENDATIONS

a. The 5082-4205 is intended to be soldered to a printed circuit board having a thickness of from 0.51 to 1.52mm (0.02 to 0.06 inch).

b. Soldering temperature should be controlled so that at no time does the case temperature approach 280° C. The lowest solder melting point in the device is 280° C (gold-tin eutectic). If this temperature is approached, the solder will soften, and the lens may fall off. Lead-tin solder is recommended for mounting the package, and should be applied with a small soldering iron, for the shortest possible time, to avoid the temperature approaching 280° C.

c. Contact to the lens end should be made by soldering to one or both of the tabs provided. Care should be exercised to prevent solder from coming in contact with the lens.

d. If printed circuit board mounting is not convenient, wire leads may be soldering or welded to the devices using the precautions noted above.

LINEAR OPERATION

Having an equivalent circuit as shown in Figure 9, operation of the photodiode is most linear when operated with a current amplifier as shown in Figure 10.

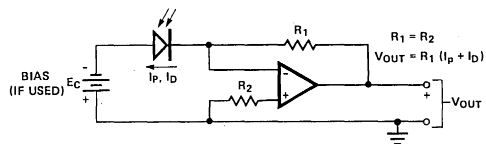


Figure 10. Linear Operation.

Lowest noise is obtained with $E_c = 0$, but higher speed and wider dynamic range are obtained if $5 < E_c < 20$ volts. The amplifier should have as high an input resistance as possible to permit high loop gain. If the photodiode is reversed, bias should also be reversed.

LOGARITHMIC OPERATION

If the photodiode is operated at zero bias with a very high impedance amplifier, the output voltage will be:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{kT}{q} \cdot \ln \left(1 + \frac{I_P}{I_S}\right)$$

where $I_S = I_F \left(e^{\frac{qV}{kT}} - 1\right)^{-1}$ at $0 < I_F < 0.1mA$

using a circuit as shown in Figure 11.

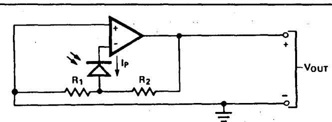
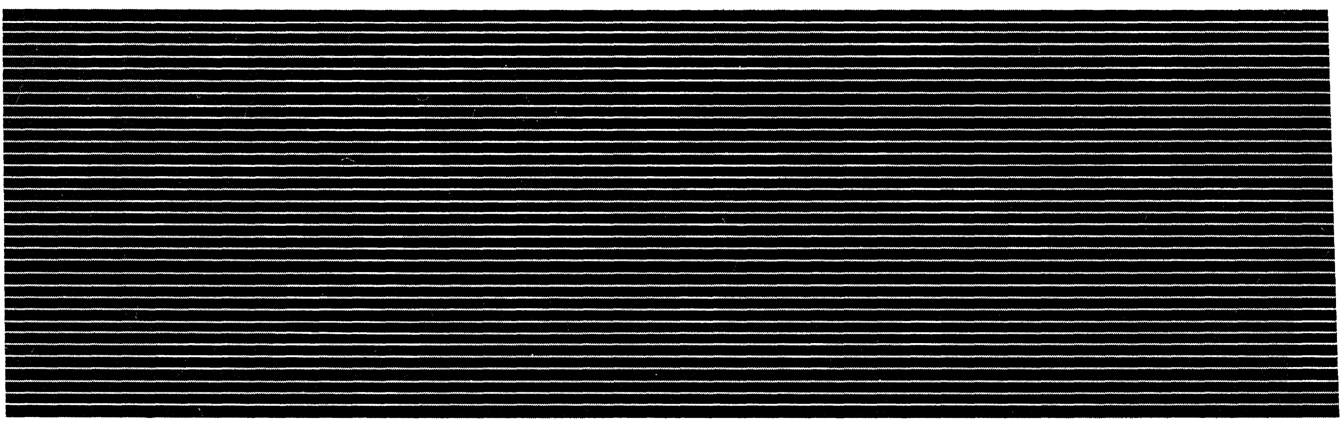


Figure 11. Logarithmic Operation.

Output voltage, V_{OUT}, is positive as the photocurrent, I_P, flows back through the photodiode making the anode positive.

FIBER OPTICS

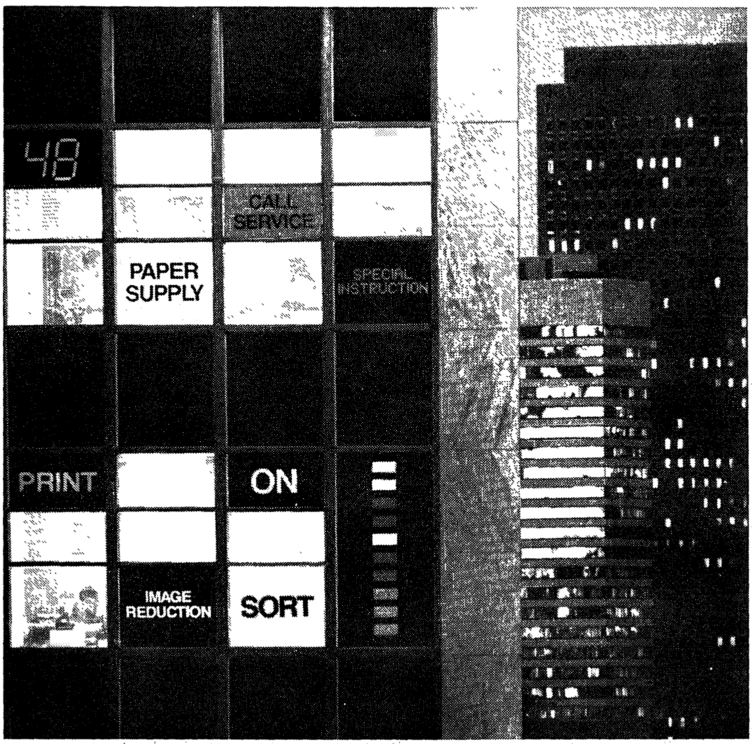


5. Light Bars and Bar Graph Arrays

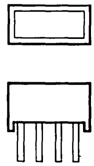
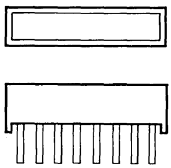
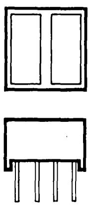
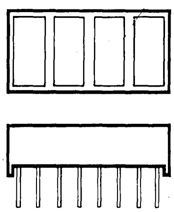
Light Bars and Bar Graph Arrays

LED Light Bars are Hewlett-Packard's innovative solution to fixed message annunciation. The large, uniformly illuminated light emitting surface may be used for backlighting legends or simple indicators. Four distinct colors are offered, high efficiency red, yellow, high performance green and emerald green, with three bicolor combinations (see page 5-14.) Each of the eight X-Y stackable package styles offers one, two, or four light emitting surfaces. Panel and Legend Mounts are also available for all devices.

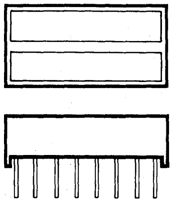
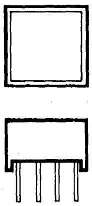
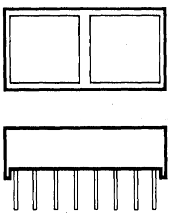
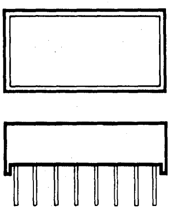
In addition to light bars, HP offers effective analog message annunciation with the new 10-element and 101-element LED Bar Graph Arrays. These bar graph arrays eliminate the matching and alignment problems commonly associated with arrays of discrete LED indicators. Each device offers easy to handle packages that are compatible with standard SIP and DIP sockets. The 10-element Bar Graph Array is available in standard red, high efficiency red, yellow, high performance green and emerald green. The new multicolor 10-element arrays have high efficiency red, yellow and green LEDs in one package. The package is X-Y stackable, with a unique interlock allowing easy end-to-end alignment. The 101-element Bar Graph Array is offered in standard red, high efficiency red and high performance green with 1% resolution.



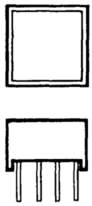
LED Light Bars

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2300	High Efficiency Red	4 Pin In-Line; .100" Centers; .400"L x .195"W x .240"H	Diffused	20 mcd	2.0 V	5-7
	HLMP-2400	Yellow		Diffused	20 mcd	2.1 V	
	HLMP-2500	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2000	Emerald		Diffused	9 mcd	2.2 V	
	HLMP-2350	High Efficiency Red	8 Pin In-Line; .100" Centers; .800"L x .195"W x .240"H	Diffused	35 mcd	2.0 V	
	HLMP-2450	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2550	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2050	Emerald		Diffused	18 mcd	2.2 V	
	HLMP-2600	High Efficiency Red	8 Pin DIP; .100" Centers; .400"L x .400"W x .240"H; Dual Arrangement	Diffused	20 mcd	2.0 V	
	HLMP-2700	Yellow		Diffused	18 mcd	2.1 V	
	HLMP-2800	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2100	Emerald		Diffused	9 mcd	2.2 V	
	HLMP-2620	High Efficiency Red	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H; Quad Arrangement	Diffused	20 mcd	2.0 V	
	HLMP-2720	Yellow		Diffused	18 mcd	2.1 V	
	HLMP-2820	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2120	Emerald		Diffused	9 mcd	2.2 V	

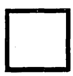
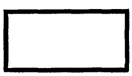
LED Light Bars (Continued)

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2635	High Efficiency Red	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H Dual Bar Arrangement	Diffused	35 mcd	2.0 V	5-7
	HLMP-2735	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2835	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2135	Emerald		Diffused	18 mcd	2.2 V	
	HLMP-2655	High Efficiency Red	8 Pin DIP; .100" Centers; .400"L x .400"W x .240"H Square Arrangement	Diffused	35 mcd	2.0 V	
	HLMP-2755	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2855	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2155	Emerald		Diffused	18 mcd	2.2 V	
	HLMP-2670	High Efficiency Red	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H Dual Square Arrangement	Diffused	35 mcd	2.0 V	
	HLMP-2770	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2870	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2170	Emerald		Diffused	18 mcd	2.2 V	
	HLMP-2685	High Efficiency Red	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H Single Bar Arrangement	Diffused	70 mcd	2.0 V	
	HLMP-2785	Yellow		Diffused	70 mcd	2.1 V	
	HLMP-2885	Green		Green Diffused	100 mcd	2.2 V	
	HLMP-2185	Emerald		Diffused	36 mcd	2.2 V	

LED Bicolor Light Bars

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2950	High Efficiency Red/ Yellow	8 Pin DIP; .100" Centers; .400"L x .400"W x .240"H Square Arrangment	Diffused	HER: 20 mcd Yellow: 12 mcd	HER: 2.0 V Yellow: 2.1 V	5-14
	HLMP-2965	High Efficiency Red/ Green		Diffused	HER: 20 mcd Green: 20 mcd	HER: 2.0 V Green: 2.2 V	
	HLMP-2980	High Efficiency Red/ Emerald		Diffused	HER: 20 mcd Emerald: 9 mcd	HER: 2.0 V Emerald: 2.2 V	

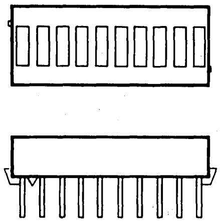
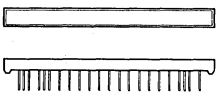
Panel and Legend Mounts for LED Light Bars

Device		Corresponding Light Bar Module Part Number HLMP-	Page No.
Package Outline Drawing	Part No.		
	HLMP-2598	2050, 2350, 2450, 2550, 2050	5-21
	HLMP-2599	2000, 2300, 2400, 2500, 2000	
	HLMP-2898	2100, 2600, 2700, 2800, 2100 2155, 2655, 2755, 2855, 2155 2950, 2965, 2980	
	HLMP-2899	2120, 2620, 2720, 2820, 2120 2135, 2635, 2735, 2835, 2135 2170, 2670, 2770, 2870, 2170 2185, 2685, 2785, 2885, 2185	

Special Options

Description	Option Code	Applicable Part Number HLMP-	Page No.
Legends	L00- L06	2300, 2400, 2500, 2000 2655, 2755, 2855, 2155 2685, 2785, 2885, 2185	5-23
Intensity Selected	S02	2300, 2400, 2500 2635, 2735, 2835 2350, 2450, 2550 2655, 2795, 2855 2600, 2700, 2800 2670, 2770, 2870 2620, 2720, 2820 2685, 2785, 2885	5-25

LED Bar Graph Arrays

Device		Description			Typical Luminous Intensity	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HDSP-4820	Standard Red	20 Pin DIP; .100" Centers; 1.0"L x .400"W x .240"H	Diffused	1250 μcd @ 20 mA DC	1.6 V @ 20 mA DC	5-26
	HDSP-4830	High Efficiency Red		Diffused	2280 μcd @ 10 mA DC	2.1 V @ 20 mA DC	
	HDSP-4840	Yellow		Diffused	1900 μcd @ 10 mA DC	2.2 V @ 20 mA DC	
	HDSP-4850	High Performance Green		Green Diffused	1900 μcd @ 10 mA DC	2.1 V @ 10 mA DC	
	HDSP-4890	Emerald		Diffused	1600 μcd @ 10 mA DC	2.2 V @ 10 mA DC	
	HDSP-4832	Multicolor		Diffused	1900 μcd @ 10 mA DC		
	HDSP-4836	Multicolor		Diffused	1900 μcd @ 10 mA DC		
	HDSP-8820	Standard Red	22 Pin SIP; .100" Centers; 4.16"L x .390"W x .236"H	Red, Non-Diffused	20 μcd @ 100 mA Pk: 1 of 110 D.F.	1.7 V @ 100 mA Pk: 1 of 110 D.F.	5-32
	HDSP-8825	High Efficiency Red		Clear	175 μcd @ 100 mA Pk: 1 of 110 D.F.	2.3 V @ 100 mA Pk: 1 of 110 D.F.	
	HDSP-8835	High Performance Green		Clear	175 μcd @ 100 mA Pk: 1 of 110 D.F.	2.3 V @ 100 mA Pk: 1 of 110 D.F.	

HEWLETT PACKARD

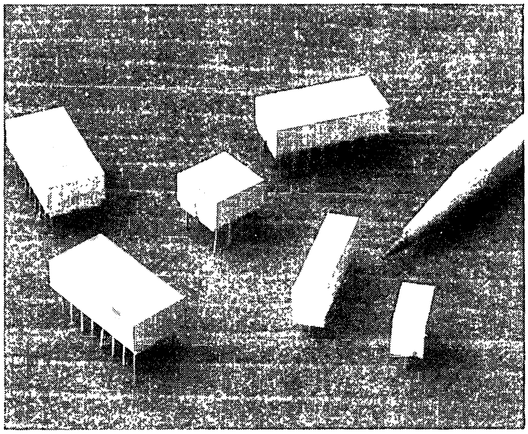
LED LIGHT BARS

HIGH EFFICIENCY RED HLMP-2300/-2600 SERIES
YELLOW HLMP-2400/-2700 SERIES
HIGH PERFORMANCE GREEN HLMP-2500/-2800 SERIES
EMERALD GREEN HLMP-2000/-2100 SERIES

TECHNICAL DATA JANUARY 1986

Features

- **LARGE, BRIGHT, UNIFORM LIGHT EMITTING AREAS**
  Approximately Lambertian Radiation Pattern
- **CHOICE OF THREE COLORS**
- **CATEGORIZED FOR LIGHT OUTPUT**
- **YELLOW, GREEN, AND EMERALD GREEN CATEGORIZED FOR DOMINANT WAVELENGTH**
- **EXCELLENT ON-OFF CONTRAST**
- **EASILY MOUNTED ON P.C. BOARDS OR INDUSTRY STANDARD SIP/DIP SOCKETS**
- **MECHANICALLY RUGGED**
- **X-Y STACKABLE**
- **FLUSH MOUNTABLE**
- **CAN BE USED WITH PANEL AND LEGEND MOUNTS**
- **LIGHT EMITTING SURFACE SUITABLE FOR LEGEND ATTACHMENT PER APPLICATION NOTE 1012**
- **SUITABLE FOR MULTIPLEX OPERATION**
- **I.C. COMPATIBLE**



Applications

- **BUSINESS MACHINE MESSAGE ANNUNCIATORS**
- **TELECOMMUNICATIONS INDICATORS**
- **FRONT PANEL PROCESS STATUS INDICATORS**
- **PC BOARD IDENTIFIERS**
- **BAR GRAPHS**

Description

The HLMP-2000/-2100/-2300/-2400/-2500/-2600/-2700/-2800 series light bars are rectangular light sources designed for a variety of applications where a large, bright source of light is required. These light bars are configured in a single-in-line and dual-in-line packages that contain either single or segmented light emitting areas. The -2300/-2400/-2600/-2700 series devices utilizes LED chips which are made from GaAsP on a transparent GaP substrate. The -2000/-2100/-2500/-2800 series devices utilize chips made from GaP on a transparent GaP substrate.

Selection Guide

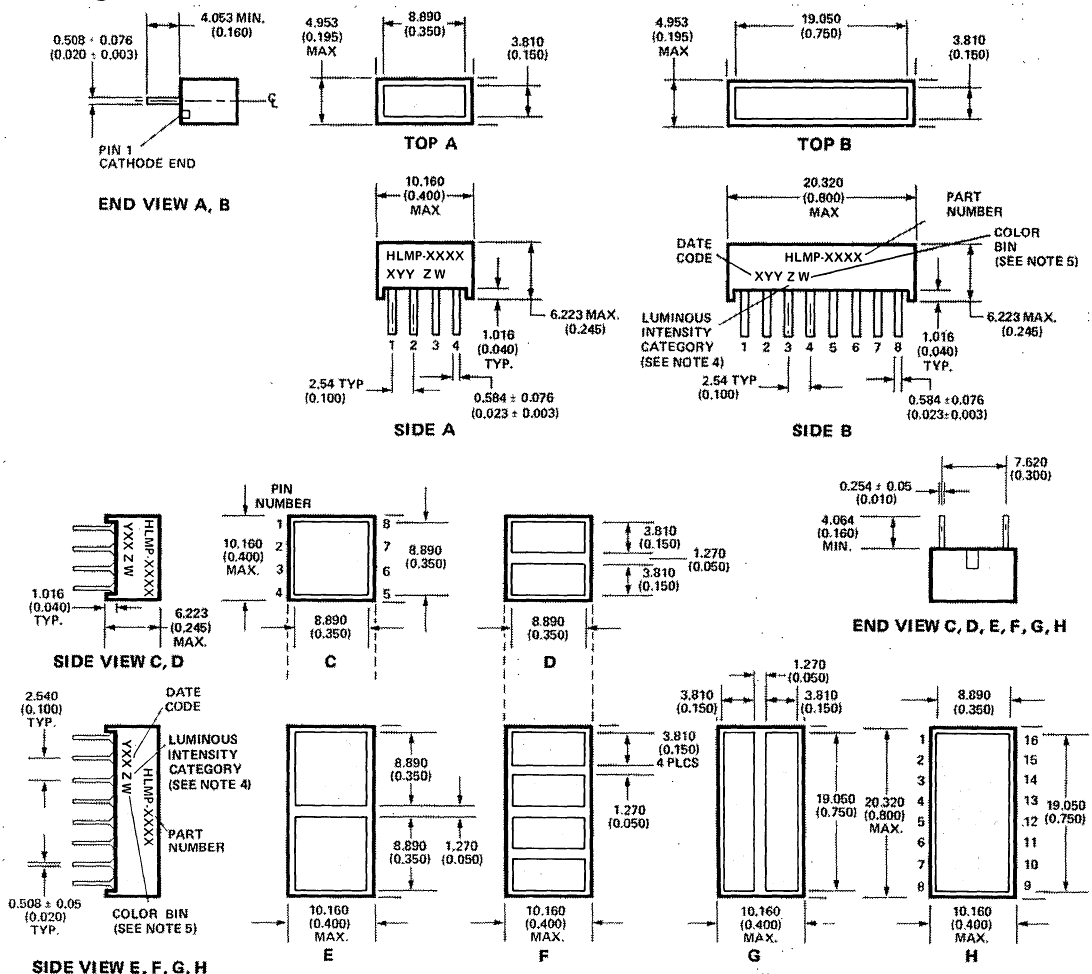
Light Bar Part Number HLMP-				Size of Light Emitting Areas	Number of Light Emitting Areas	Package Outline	Corresponding Panel and Legend Mount Part No. HLMP-
High Efficiency Red	Yellow	Green	Emerald Green				
2300	2400	2500	2000	8.89 mm x 3.81 mm (.350 in x .150 in.)	1	A	2599
2350	2450	2550	2050	19.05 mm x 3.81 mm (.750 in x .150 in.)	1	B	2598
2600	2700	2800	2100	8.89 mm x 3.81 mm (.350 in x .150 in.)	2	D	2698
2620	2720	2820	2120	8.89 mm x 3.81 mm (.350 in x .150 in.)	4	F	2899
2635	2735	2835	2135	8.89 mm x 19.05 mm (.150 in x .750 in.)	2	G	2899
2655	2755	2855	2155	8.89 mm x 8.89 mm (.350 in x .350 in.)	1	C	2898
2670	2770	2870	2170	8.89 mm x 8.89 mm (.350 in x .350 in.)	2	E	2899
2685	2785	2885	2185	8.89 mm x 19.05 mm (.350 in x .750 in.)	1	H	2899

Absolute Maximum Ratings

Parameter	HLMP-2300/ -2600 Series	HLMP-2400/ -2700 Series	HLMP-2500/ -2800 Series	HLMP-2000/ -2100 Series
Average Power Dissipation per LED Chip[1]	135 mW	85 mW	135 mW	135 mW
Peak Forward Current per LED Chip, $T_A = 50°C$ (Maximum Pulse Width = 2 ms[1,2])	90 mA	60 mA	90 mA	90 mA
Time Average Forward Current per LED Chip, Pulsed Conditions[2]	25 mA $T_A = 25°C$	20 mA $T_A = 50°C$	25 mA $T_A = 25°C$	25 mA $T_A = 25°C$
DC Forward Current per LED Chip, $T_A = 50°C$[3]	30 mA	25 mA	30 mA	30 mA
Reverse Voltage per LED Chip	6V			
Operating Temperature Range	−40°C to +85°C		−20°C to +85°C	
Storage Temperature Range	−40°C to +85°C			
Lead Soldering Temperature 1.6 mm (1/16 inch) Below Seating Plane	260°C for 3 seconds			

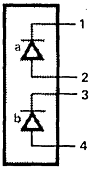
NOTES: 1. For HLMP-2000/-2100/-2300/-2500/-2600/-2800 series, derate above $T_A = 25°C$ at 1.8 mW/°C per LED chip. For HLMP-2400/-2700 series, derate above $T_A = 50°C$ at 1.8 mW/°C per LED chip. See Figure 2. 2. See Figure 1 to establish pulsed operating conditions.
3. For HLMP-2000/-2100/-2300/-2500/-2600/-2800 series, derate above $T_A = 50°C$ at 0.50 mA/°C per LED chip. For HLMP-2400/-2700 series, derate above $T_A = 60°C$ at 0.50 mA/°C per LED chip. See Figure 3.

Package Dimensions

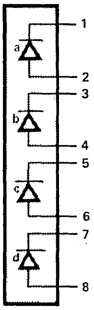


NOTE: DIMENSIONS IN MILLIMETRES (INCHES). TOLERANCES ±0.25 mm (±0.010 in) UNLESS OTHERWISE INDICATED.

Internal Circuit Diagrams

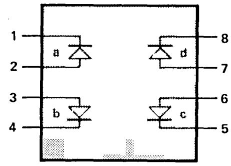


A

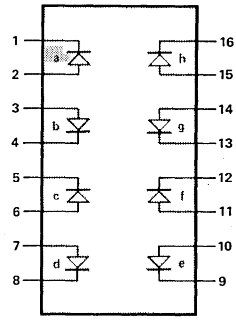


B

PIN FUNCTION		
PIN	A -2000/-2300/-2400 -2500	B -2100/-2350/-2450 -2550
1	Cathode — a	Cathode — a
2	Anode — a	Anode — a
3	Cathode — b	Cathode — b
4	Anode — b	Anode — b
5		Cathode — c
6		Anode — c
7		Cathode — d
8		Anode — d



C,D



E,F,G,H

PIN	PIN FUNCTION	
	C, D	E, F, G, H
1	CATHODE a	CATHODE a
2	ANODE a	ANODE a
3	ANODE b	ANODE b
4	CATHODE b	CATHODE b
5	CATHODE c	CATHODE c
6	ANODE c	ANODE c
7	ANODE d	ANODE d
8	CATHODE d	CATHODE d
9		CATHODE e
10		ANODE e
11		ANODE f
12		CATHODE f
13		CATHODE g
14		ANODE g
15		ANODE h
16		CATHODE h

Electrical/Optical Characteristics at $T_A = 25°C$

High Efficiency Red HLMP-2300/-2600 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[4] Per Light Emitting Area	2300	I_V	6	23		mcd	20 mA DC
				26		mcd	60 mA Pk: 1 of 3 DF
	2350	I_V	13	45		mcd	20 mA DC
				52		mcd	60 mA Pk: 1 of 3 DF
	2600	I_V	6	22		mcd	20 mA DC
				25		mcd	60 mA Pk: 1 of 3 DF
	2620	I_V	6	25		mcd	20 mA DC
				29		mcd	60 mA Pk: 1 of 3 DF
	2635	I_V	13	45		mcd	20 mA DC
				52		mcd	60 mA Pk: 1 of 3 DF
	2655	I_V	13	43		mcd	20 mA DC
				49		mcd	60 mA Pk: 1 of 3 DF
	2670	I_V	13	45		mcd	20 mA DC
				52		mcd	60 mA Pk: 1 of 3 DF
	2685	I_V	22	80		mcd	20 mA DC
				92		mcd	60 mA Pk: 1 of 3 DF
Peak Wavelength		λ_{peak}		635		nm	
Dominant Wavelength[5]		λ_d		626		nm	
Forward Voltage Per LED		V_F		2.0	2.6	V	$I_F = 20$ mA
Reverse Breakdown Voltage Per LED		V_{BR}	6	15		V	$I_R = 100\mu A$
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/ LED Chip	

Yellow HLMP-2400/-2700 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[4] Per Light Emitting Area	2400	Iv	6	20		mcd	20 mA DC
				24		mcd	60 mA Pk: 1 of 3 DF
	2450	Iv	13	38		mcd	20 mA DC
				46		mcd	60 mA Pk: 1 of 3 DF
	2700	Iv	6	18		mcd	20 mA DC
				22		mcd	60 mA Pk: 1 of 3 DF
	2720	Iv	6	18		mcd	20 mA DC
				22		mcd	60 mA Pk: 1 of 3 DF
	2735	Iv	13	35		mcd	20 mA DC
				43		mcd	60 mA Pk: 1 of 3 DF
	2755	Iv	13	35		mcd	20 mA DC
				43		mcd	60 mA Pk: 1 of 3 DF
	2770	Iv	13	35		mcd	20 mA DC
				43		mcd	60 mA Pk: 1 of 3 DF
	2785	Iv	26	70		mcd	20 mA DC
				85		mcd	60 mA Pk: 1 of 3 DF
Peak Wavelength		λ_{peak}		583		nm	
Dominant Wavelength[5]		λ_d		585		nm	
Forward Voltage Per LED		V_F		2.1	2.6	V	$I_F = 20$ mA
Reverse Breakdown Voltage Per LED		V_{BR}	6	15		V	$I_R = 100\ \mu A$
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/ LED Chip	

High Performance Green HLMP-2500/-2800 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[4] Per Light Emitting Area	2500	Iv	5	25		mcd	20 mA DC
				28		mcd	60 mA Pk: 1 of 3 DF
	2550	Iv	11	50		mcd	20 mA DC
				56		mcd	60 mA Pk: 1 of 3 DF
	2800	Iv	5	25		mcd	20 mA DC
				28		mcd	60 mA Pk: 1 of 3 DF
	2820	Iv	5	25		mcd	20 mA DC
				28		mcd	60 mA Pk: 1 of 3 DF
	2835	Iv	11	50		mcd	20 mA DC
				56		mcd	60 mA Pk: 1 of 3 DF
	2855	Iv	11	50		mcd	20 mA DC
				56		mcd	60 mA Pk: 1 of 3 DF
	2870	Iv	11	50		mcd	20 mA DC
				56		mcd	60 mA Pk: 1 of 3 DF
	2885	Iv	22	100		mcd	20 mA DC
				111		mcd	60 mA Pk: 1 of 3 DF
Peak Wavelength		λ_{peak}		565		nm	
Dominant Wavelength[5]		λ_d		572		nm	
Forward Voltage Per LED		V_F		2.2	2.6	V	$I_F = 20$ mA
Reverse Breakdown Voltage Per LED		V_{BR}	6	15		V	$I_R = 100\ \mu A$
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/ LED Chip	

Emerald Green HLMP-2000/-2100 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity [4] Per Light Emitting Area	2000	Iv	5	9		mcd	20 mA DC
				11		mcd	60 mA Pk: 1 of 3 DF
	2050	Iv	11	18		mcd	20 mA DC
				21		mcd	60 mA Pk: 1 of 3 DF
	2100	Iv	5	9		mcd	20 mA DC
				11		mcd	60 mA Pk: 1 of 3 DF
	2120	Iv	5	9		mcd	20 mA DC
				11		mcd	60 mA Pk: 1 of 3 DF
	2135	Iv	11	18		mcd	20 mA DC
				21		mcd	60 mA Pk: 1 of 3 DF
	2155	Iv	11	18		mcd	20 mA DC
				21		mcd	60 mA Pk: 1 of 3 DF
	2170	Iv	11	18		mcd	20 mA DC
				21		mcd	60 mA Pk: 1 of 3 DF
	2185	Iv	22	36		mcd	20 mA DC
				42		mcd	60 mA Pk: 1 of 3 DF
Peak Wavelength		λ_{PEAK}		556		nm	
Dominant Wavelength [5]		λ_d		558		nm	
Forward Voltage Per LED		λ_F		2.2	2.6	V	$I_F = 20$ mA
Reverse Breakdown Voltage Per LED		V_{BR}	6	15		V	$I_R = 100 \mu A$
Thermal Resistance LED Junction-to-Pin		$R_{\theta J\text{-}PIN}$		150		°C/W/ LED Chip	

NOTES
4. These devices are categorized for luminous intensity with the intensity category designated by a letter code on the side of the package.
5. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device. Yellow, green, and emerald, devies are categorized for dominant wavelength with the color bin designated by a number code on the side of the package.

Electrical

The HLMP-2000/-2100/-2300/-2400/-2500/-2600/-2700/-2800 series of light bar devices are composed of two, four or eight light emitting diodes, with the light from each LED optically scattered to form an evenly illuminated light emitting surface. The LED's have a P-N junction diffused into the epitaxial layer on a GaP transparent substrate.

The anode and cathode of each LED is brought out by separate pins. This universal pinout arrangement allows for the wiring of the LED's within a device in any of three possible configurations: parallel, series, or series/parallel.

The typical forward voltage values, scaled from Figure 5, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$$V_F = 1.8V + I_{PEAK} (40\Omega)$$
For $I_{PEAK} \geq 20mA$

$$V_F = 1.6V + I_{DC} (50\Omega)$$
For $5mA \leq I_{DC} \leq 20mA$

The maximum power dissipation can be calculated for any pulsed or DC drive condition. For DC operation, the maximum power dissipation is the product of the maximum forward voltage and the maximum forward current. For pulsed operation, the maximum power dissipation is the product of the maximum forward voltage at the peak forward current times the maximum average forward current. Maximum allowable power dissipation for any given ambient temperature and thermal resistance ($R\theta_{J-A}$) can be determined by using Figure 2. The solid line in Figure 2 ($R\theta_{J-A}$ of 538°C/W) represents a typical thermal resistance of a device socketed in a printed circuit board. The dashed lines represent achievable thermal resistances that can be obtained through improved thermal design. Once the maximum allowable power dissipation is determined, the maximum pulsed or DC forward current can be calculated.

Optical

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_V\ (cd/m^2) = \frac{I_V\ (cd)}{A\ (m^2)}$$

$$L_V\ (footlamberts) = \frac{\pi I_V\ (cd)}{A\ (ft^2)}$$

Size of Light Emitting Area	Surface Area	
	Sq. Metres	Sq. Feet
8.89 mm x 8.89 mm	67.74×10^{-6}	729.16×10^{-6}
8.89 mm x 3.81 mm	33.87×10^{-6}	364.58×10^{-6}
8.89 mm x 19.05 mm	135.48×10^{-6}	1458.32×10^{-6}
3.81 mm x 19.05 mm	72.58×10^{-6}	781.25×10^{-6}

Refresh rates of 1 kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 4, $\eta_{I_{PEAK}}$, and adjusted for operating ambient temperature. The time average luminous intensity at $T_A = 25°C$ is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{20mA}\right] (\eta_{I_{PEAK}})\ (I_V\ \text{Data Sheet})$$

Example: For HLMP-2735 series

$$\eta_{I_{PEAK}} = 1.18 \text{ at } I_{PEAK} = 48\ mA$$

$$I_{V\ TIME\ AVG} = \left[\frac{12mA}{20mA}\right] (1.18)\ (35\ mcd) = 25\ mcd$$

The time average luminous intensity may be adjusted for operating ambient temperature by the following exponential equation:

$$I_V\ (T_A) = I_V\ (25°C)\ e^{[K\ (T_A - 25°C)]}$$

Device	K
-2300/-2600 Series	-0.0131/°C
-2400/-2700 Series	-0.0112/°C
-2500/-2800 Series	-0.0104/°C
-2000/-2100 Series	-0.0104/°C

Example: $I_V\ (80°C) = (25\ mcd) e^{[-0.0112\ (80-25)]} = 14\ mcd$

Mechanical

These light bar devices may be operated in ambient temperatures above +60°C without derating when installed in a PC board configuration that provides a thermal resistance to ambient value less than 250°C/W/LED. See Figure 3 to determine the maximum allowed thermal resistance for the PC board, $R_{\theta PC-A}$, which will permit nonderated operation in a given ambient temperature.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

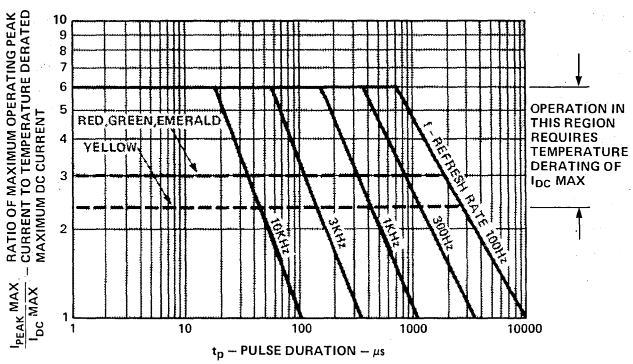


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration.

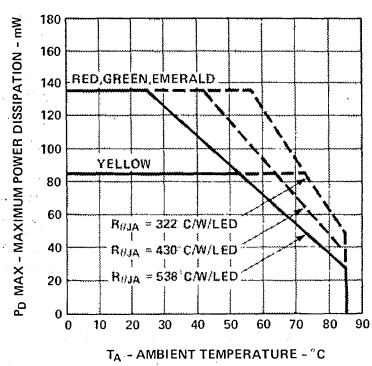


Figure 2. Maximum Allowable Power Dissipation per LED vs. Ambient Temperature Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction to Ambient on a per LED Basis, Tj MAX = 100° C.

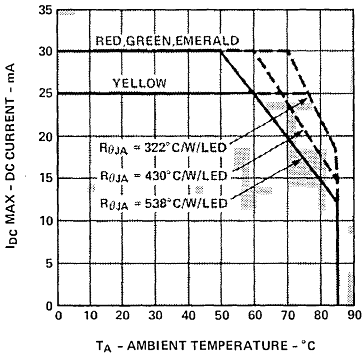


Figure 3. Maximum Allowable DC Current per LED vs. Ambient Temperature, Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED Basis, Tj MAX = 100° C.

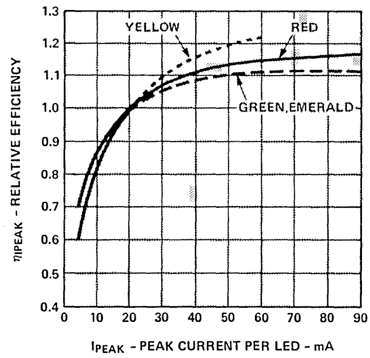


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

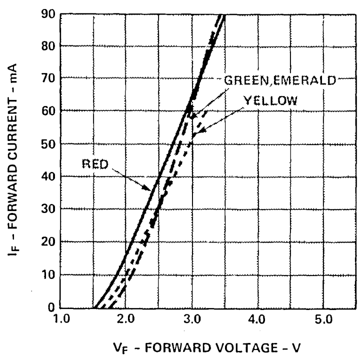


Figure 5. Forward Current vs. Forward Voltage Characteristics.

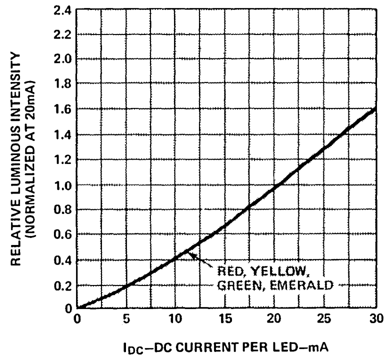


Figure 6. Relative Luminous Intensity vs. DC Forward Current.

LIGHT BARS AND BAR GRAPH ARRAYS

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

LED BICOLOR LIGHT BARS

DIP — Single Light Emitting Area

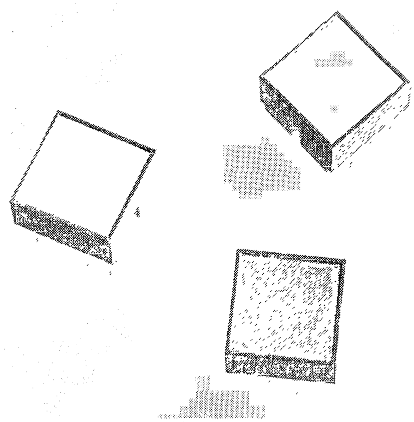
HEWLETT PACKARD

HIGH EFFICIENCY RED/YELLOW HLMP-2950
HIGH EFFICIENCY RED/HIGH PERFORMANCE GREEN HLMP-2965
HIGH EFFICIENCY RED/EMERALD GREEN HLMP-2980

TECHNICAL DATA JANUARY 1986

Features

- **LARGE, BRIGHT, UNIFORM LIGHT EMITTING AREA**
  8.89mm x 8.89mm (0.35 x 0.35 inch)
  Approximately Lambertian Radiation Pattern
- **CHOICE OF THREE BICOLOR COMBINATIONS**
- **CATEGORIZED FOR LIGHT OUTPUT**
- **YELLOW, GREEN, AND EMERALD CATEGORIZED FOR DOMINANT WAVELENGTH**
- **EXCELLENT ON-OFF CONTRAST**
- **EASILY MOUNTED ON P.C. BOARDS OR INDUSTRY STANDARD DIP SOCKETS**
- **MECHANICALLY RUGGED**
- **X-Y STACKABLE**
- **FLUSH MOUNTABLE**
- **CAN BE USED WITH HLMP-2898 PANEL AND LEGEND MOUNT**
- **LIGHT EMITTING SURFACE SUITABLE FOR LEGEND ATTACHMENT PER APPLICATION NOTE 1012**
- **I.C. COMPATIBLE**



Applications

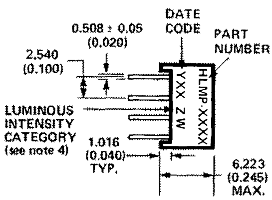
- **TRISTATE LEGEND ILLUMINATION**
- **SPACE-CONSCIOUS FRONT PANEL STATUS INDICATORS**
- **BUSINESS MACHINE MESSAGE ANNUNCIATORS**
- **TELECOMMUNICATIONS INDICATORS**
- **TWO FUNCTION LIGHTED SWITCHES**

Description

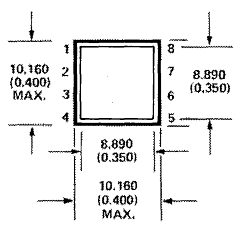
The HLMP-2950/-2965/-2980 light bars are bicolor light sources designed for a variety of applications where dual state or tristate illumination is required for the same annunciator function. In addition, both devices are capable of emitting a range of colors by pulse width modulation.

These light bars are configured in dual-in-line packages which contain a single light emitting area. The high efficiency red (HER) and yellow LED chips utilize GaAsP on a transparent Gap substrate. The green and emerald LED chips utilize GaP on a transparent substrate.

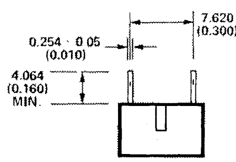
Package Dimensions



SIDE VIEW



TOP VIEW



END VIEW

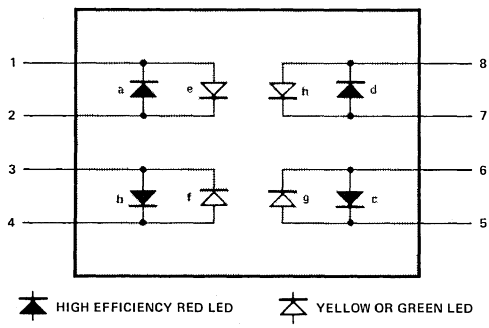
NOTES: DIMENSIONS IN MILLIMETRES (INCHES).
TOLERANCES ±0.25 mm (±0.010 in) UNLESS OTHERWISE INDICATED.

Absolute Maximum Ratings

Parameter	HLMP-2965	HLMP-2950	HLMP-2980
Average Power Dissipation per LED Chip[1]	135 mW	85 mW	135 mW
Peak Forward Current per LED Chip, $T_A = 50°C$ (Maximum Pulse Width = 2 ms)[1,2]	90 mA	60 mA	90 mA
Time Average Forward Current per LED Chip, Pulsed Conditions[2]	25 mA, $T_A = 25°C$	20 mA, $T_A = 50°C$	25 mA $T_A = 50°C$
DC Forward Current per LED Chip, $T_A = 50°C$[3]	30 mA	25 mA	30 mA
Operating Temperature Range	-20°C to +85°C	-40°C to +85°C	-20°C to +85°C
Storage Temperature Range	-40°C to +85°C		
Lead Soldering Temperature, 1.6 mm (1/16 inch) Below Seating Plane	260°C for 3 seconds		

NOTES:
1. For HLMP-2965, derate above $T_A = 25°C$ at 1.8 mW/°C per LED chip. For HLMP-2950 and -2980 derate above $T_A = 50°C$ at 1.8 mW/°C per LED chip. See Figure 2.
2. See Figure 1 to establish pulsed operating conditions.
3. For HLMP-2965, derate above $T_A = 50°C$ at 0.50 mA/°C per LED chip. For HLMP-2950 and -2980 derate above $T_A = 60°C$ at 0.50 mA/°C per LED chip. See Figure 3.

Internal Circuit Diagram



PIN	PIN FUNCTION HER	PIN FUNCTION YELLOW/ GREEN/ EMERALD
1	CATHODE a	ANODE e
2	ANODE a	CATHODE e
3	ANODE b	CATHODE f
4	CATHODE b	ANODE f
5	CATHODE c	ANODE g
6	ANODE c	CATHODE g
7	ANODE d	CATHODE h
8	CATHODE d	ANODE h

Electrical/Optical Characteristics at $T_A = 25°C$

HIGH EFFICIENCY RED/YELLOW HLMP-2950

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[4]	HER	I_V	9	43		mcd	20 mA DC
				49		mcd	60 mA Pk: 1 of 3 Duty Factor
	Yellow	I_V	8	35		mcd	20 mA DC
				43		mcd	60 mA Pk: 1 of 3 Duty Factor
Peak Wavelength	HER	λ_{PEAK}		635		nm	
	Yellow			583			
Dominant Wavelength[5]	HER	λ_d		626		nm	
	Yellow			585			
Forward Voltage	HER	V_F		2.1	2.6	V	$I_F = 20$ mA
	Yellow			2.2	2.6		
Thermal Resistance LED Junction-to-Pin		θ_{JC}		150		°C/W/LED	

Electrical/Optical Characteristics at $T_A = 25°C$

HIGH EFFICIENCY RED/GREEN HLMP-2965

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity [4]	HER	I_V	9	43		mcd	20 mA DC
				49		mcd	60 mA Pk: 1 of 3 Duty Factor
	Green	I_V	7.5	50		mcd	20 mA DC
				56		mcd	60 mA Pk: 1 of 3 Duty Factor
Peak Wavelength	HER	λ_{PEAK}		635		nm	
	Green			565			
Dominant Wavelength [5]	HER	λ_d		626		nm	
	Green			572			
Forward Voltage	HER	V_F		2.1	2.6	V	$I_F = 20$ mA
	Green			2.2	2.6		
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/LED	

HIGH EFFICIENCY RED/EMERALD GREEN HLMP-2980

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity	HER	I_V	9	43 49		mcd	20 mA DC 60 mA Pk: 1 of 3 Duty Factor
	Emerald	I_V	7.5	18 22		mcd	20 mA DC 60 mA Pk: 1 of 3 Duty Factor
Peak Wavelength	HER Emerald	λ_{PEAK}		635 556		nm	
Dominant Wavelength	HER Emerald	λ_d		626 558		nm	
Forward Voltage	HER Emerald	V_F		2.0 2.2	2.6 2.6	V	$I_F = 20$ mA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/LED	

NOTES:
4. These devices are categorized for luminous intensity with the intensity categorization designated by a two letter combination code located on the side of the package (Z = HER, W = Yellow, Green or Emerald).
5. The dominant wavelength, λ_d, is derived from the C.I.E. chromaticity diagram and is that single wavelength which defines the color of the device.

Electrical

The HLMP-2950/-2965/-2980 bicolor light bar devices are composed of eight light emitting diodes: four High Efficiency Red and four that either Yellow, Green, or Emerald. The light from each LED is optically scattered to form an evenly illuminated light emitting surface. The LED's are die attached and wire bonded in bicolor pairs, with the anode/cathode of each LED pair brought out by separate pins.

The typical forward voltage values, scaled from Figure 5, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be approximated using the following V_F models:

$$V_F = 1.8V + I_{PEAK}\,(40\Omega)$$
$$\text{For } I_{PEAK} \geq 20 \text{ mA}$$

$$V_F = 1.6V + I_{DC}\,(50\Omega)$$
$$\text{For } 5 \text{ mA} \leq I_{DC} \leq 20 \text{ mA}$$

The maximum power dissipation can be calculated for any pulsed or DC drive condition. For DC operation, the maximum power dissipation is the product of the maximum forward voltage and the maximum forward current. For pulsed operation, the maximum power dissipation is the product of the maximum forward voltage at the peak forward current times the maximum average forward current. Maximum allowable power dissipation for any given ambient temperature and thermal resistance ($R\theta_{J-A}$) can be determined by using Figure 2. The solid line in Figure 2 ($R\theta_{J-A}$ of 538° C/W) represents a typical thermal resistance of a device socketed in a printed circuit board. The dashed lines represent achievable thermal resistance that can be obtained through improved thermal design. Once the maximum allowable power dissipation is determined, the maximum pulsed or DC forward current can be calculated.

Optical

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_V\,(\text{cd/m}^2) = \frac{I_V\,(\text{cd})}{A\,(\text{m}^2)} \qquad L_V\,(\text{footlamberts}) = \frac{\pi I_V\,(\text{cd})}{A\,(\text{ft}^2)}$$

where the area (A) of the light emitting surface is 67.74 x 10^{-6} m^2 (729.16 x 10^{-6} ft.^2).

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, see Application Note 1005.

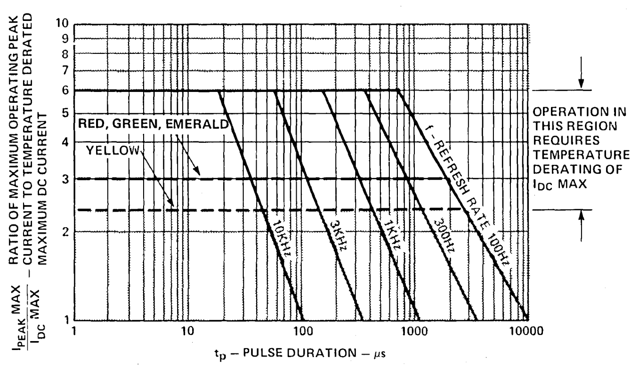


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration.

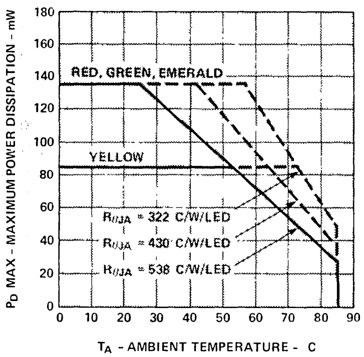


Figure 2. Maximum Allowable Power Dissipation per LED vs. Ambient Temperature. Deratings based on Maximum Allowable Thermal Resistance Values, LED Junction to Ambient on a per LED Basis, Tj MAX = 100° C.

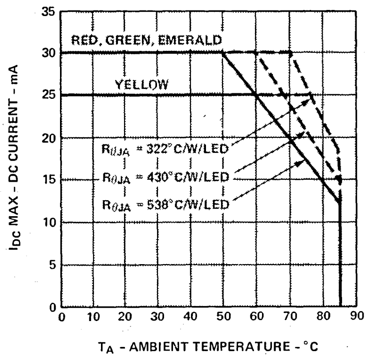


Figure 3. Maximum Allowable DC Current per LED vs. Ambient Temperature, Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED Basis, Tj MAX = 100° C.

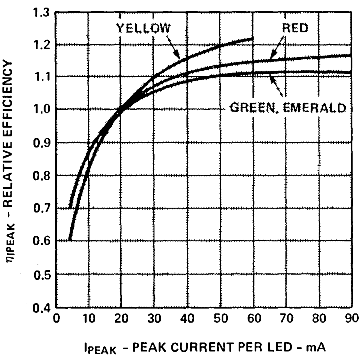


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

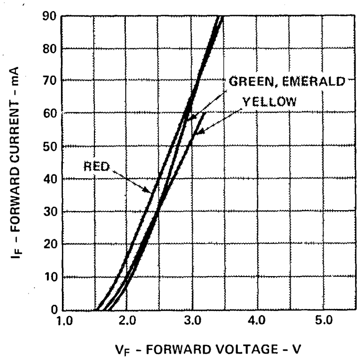


Figure 5. Forward Current vs. Forward Voltage Characteristics.

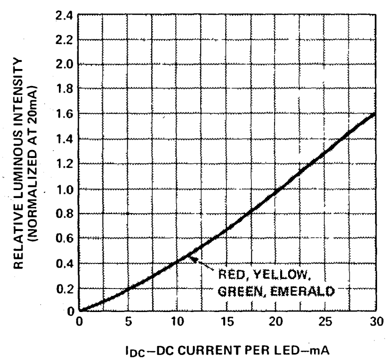


Figure 6. Relative Luminous Intensity vs. DC Forward Current.

Reversing Polarity LED Drivers

Bicolor LED light bar modules require a polarity reversing scheme to turn on the desired LED. Reversing line drivers, timers and memory drivers can be used to drive bicolor LED light bars.

The reversing line driver, which was originally designed to drive a data transmission line, can also be used as a polarity reversing driver for bicolor LED modules. The reversing line driver has a totem pole output structure that differs from most TTL circuits in that the output is designed to source as much current as it is capable of sinking.

Line drivers designed to operate from a single 5V supply are typically specified to source or sink 40 mA. Figure 7 shows the typical output characteristics of three different line drivers connected so that one output sources current across a load and the current is sunk by another output. This circuit is shown in Figure 8. At 40 mA output current, the output voltage typically varies from 2.4V (74128) to 2.9V (DM 8830, 9614) for $V_{CC} = 5.0V$. A basic bicolor LED circuit is shown in Figure 9. Since a line driver can supply 40 mA, it is capable of driving two LED pairs.

Some line drivers like the 9614 are constructed such that the sourcing output is brought out separately from the sinking output. With this type of line driver, the LED currents for each pair can be controlled separately. This technique is shown in Figure 10. Other line drivers provide a tri-state output control or provide other means for turning both LED's off. An example of this circuit technique is shown in Figure 11.

The NE556 dual timer, or two NE555 timers can also be used to drive bicolor light bars, as shown in Figure 12. The outputs at the NE555 timer are able to source or sink up to 200 mA. Connected as shown, each timer acts as an inverting buffer. This circuit has the advantage over the previous line driver circuits of being able to operate at a wide variety of power supply voltages ranging from 4.5 to 16 volts.

Memory drivers can also be used to drive bicolor light bars. Figure 13 shows a 75325 core memory driver being used to drive several pairs of bicolor LEDs. The 75325 is guaranteed to supply up to 600 mA of current with an output voltage considerably higher than 5V line drivers. The 75325 requires an additional 7.5V power supply at about 40 mA to properly bias the sourcing drivers. The 75325 allows tri-state (red, green, yellow, or emerald, off) operation.

By employing pulse width modulation techniques to any of these circuits a range of colors can be obtained. This technique is illustrated in Figure 14.

Hewlett-Packard cannot assume responsibility for use of any circuitry described other than the circuitry entirely embodied in an HP product.

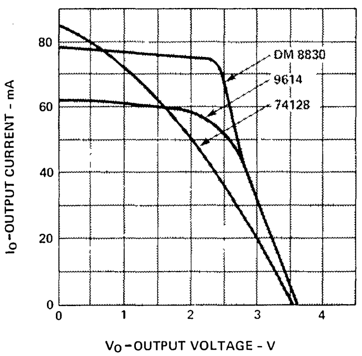


Figure 7. Typical Output Characteristics of Reversing Line Drivers.

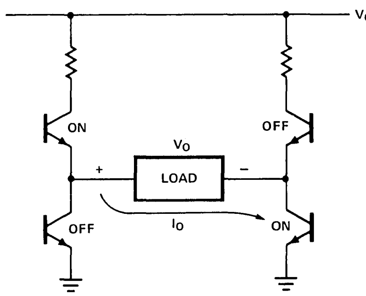


Figure 8. Line Driver Equivalent Circuit.

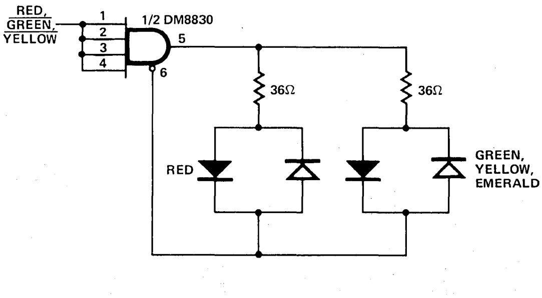
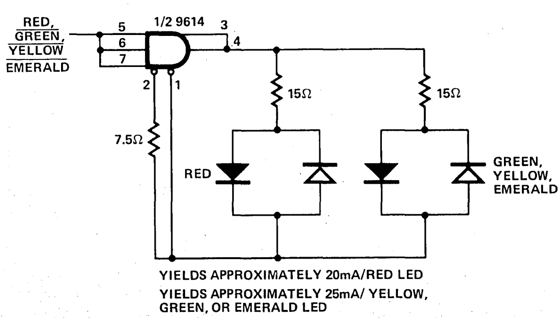


Figure 9. Typical Line Driver Circuit; Approximately 20mA/LED Pair.



YIELDS APPROXIMATELY 20mA/RED LED
YIELDS APPROXIMATELY 25mA/ YELLOW, GREEN, OR EMERALD LED

Figure 10. Techniques for Varying the Current of Each LED.

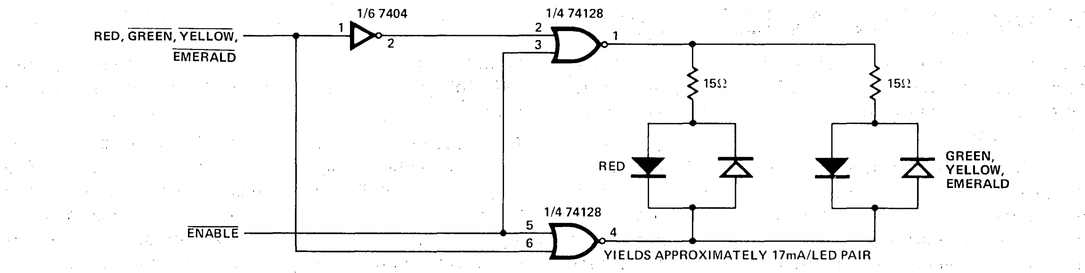


Figure 11. Tristate (Red, Green/Yellow/Emerald, Off) Bicolor LED Driver.

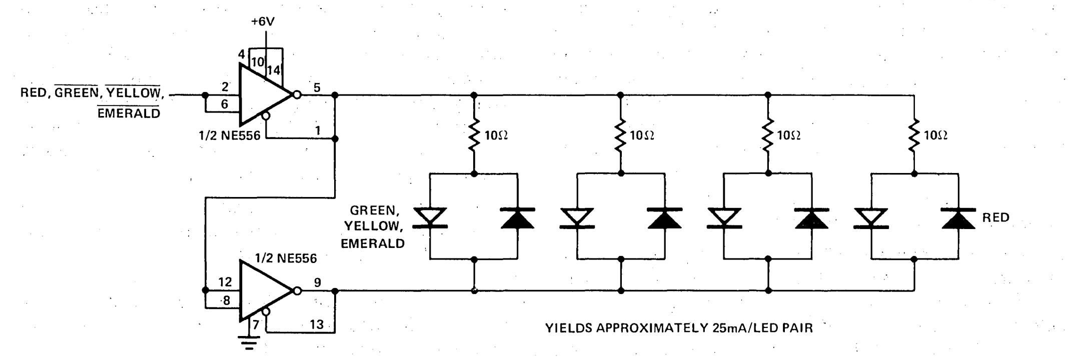


Figure 12. Use of Dual Timer to Drive Bicolor Light Bars

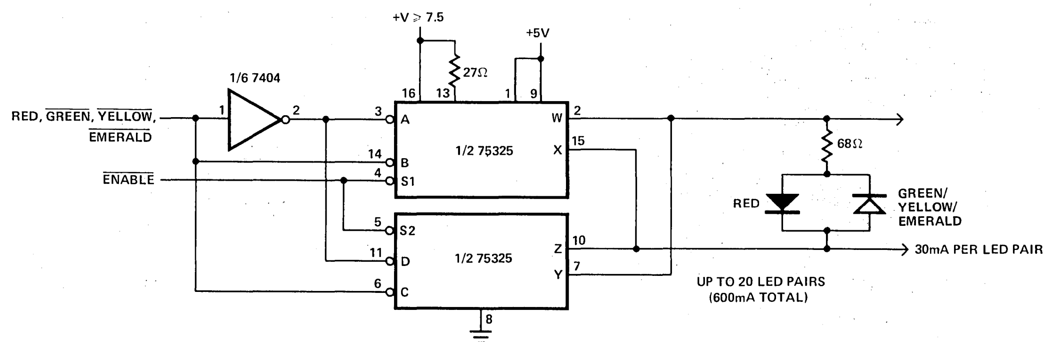


Figure 13. 75325 High Current Bicolor Driver

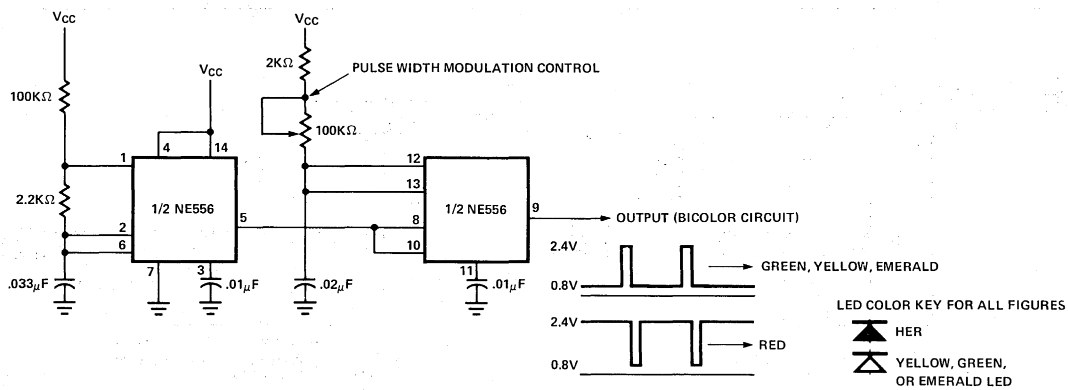


Figure 14. Pulse Width Modulation Technique

HEWLETT PACKARD

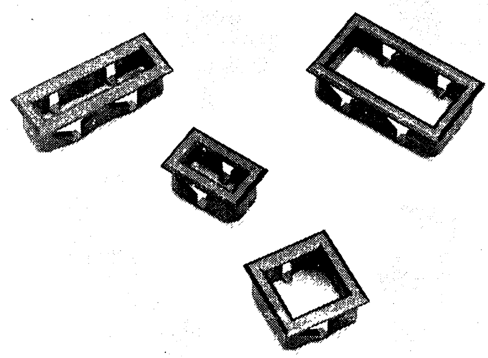
PANEL AND LEGEND MOUNTS FOR LED LIGHT BARS

HLMP-2598
HLMP-2599
HLMP-2898
HLMP-2899

TECHNICAL DATA JANUARY 1986

Features

- FIRMLY MOUNTS LIGHT BARS IN PANELS
- HOLDS LEGENDS FOR FRONT PANEL OR PC BOARD APPLICATIONS[1]
- ONE PIECE, SNAP-IN ASSEMBLY
- MATTE BLACK BEZEL DESIGN ENHANCES PANEL APPEARANCE
- FOUR SIZES AVAILABLE
- MAY BE INSTALLED IN A WIDE RANGE OF PANEL THICKNESSES
- PANEL HOLE EASILY PUNCHED OR MILLED



Description

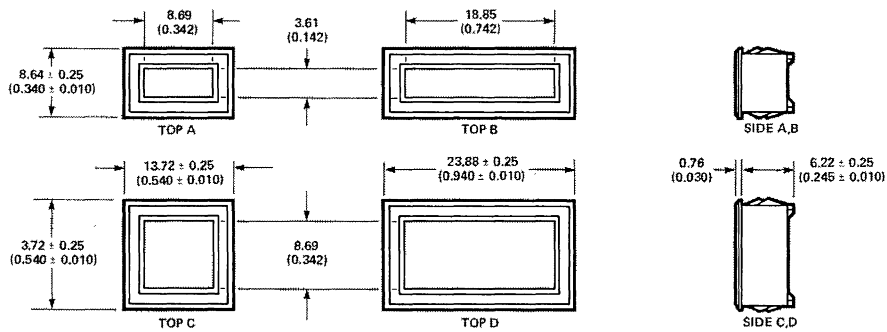
This series of black plastic bezel mounts is designed to install Hewlett-Packard Light Bars in instrument panels ranging in thickness from 1.52 mm (0.060 inch) to 3.18 mm (0.125 inch). A space has been provided for holding a 0.13 mm (0.005 inch) film legend over the light emitting surface of the light bar module.

Selection Guide

Panel and Legend Mount Part No. HLMP-	Corresponding Light Bar Module Part No. HLMP-	Panel Hole Installation Dimensions[2]	Package Outline
2598	2050, 2350, 2450, 2550	7.62 mm (0.300 inch) x 22.86 mm (0.900 inch)	B
2599	2000, 2300, 2400, 2500	7.62 mm (0.300 inch) x 12.70 mm (0.500 inch)	A
2898	2100, 2600, 2700, 2800 2155, 2655, 2755, 2855 2950, 2965, 2980	12.70 mm (0.500 inch) x 12.70 mm (0.500 inch)	C
2899	2120, 2620, 2720, 2820 2135, 2635, 2735, 2835 2170, 2670, 2770, 2870 2185, 2685, 2785, 2885	12.70 mm (0.500 inch) x 22.86 mm (0.900 inch)	D

Notes:
1. Application Note 1012 addresses legend fabrication options.
2. Allowed hole tolerance: +0.00 mm, -0.13 mm (+0.000 inch, -0.005 inch). Permitted radius: 1.60 mm (0.063 inch).

Package Dimensions



NOTES: 1. DIMENSIONS IN MILLIMETRES (INCHES)
2. UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.

Mounting Instructions

1. Mill[3] or punch a hole in the panel. Deburr, but do not chamfer, the edges of the hole.
2. Place the front of the mount against a solid, flat surface. A film legend with outside dimensions equal to the outside dimensions of the light bar may be placed in the mount or on the light bar light emitting surface. Press the light bar into the mount until the tabs snap over the back of the light bar. (When inserting the HLMP-2898, align the notched sides of the light bar with the mount sides which do not have the tabs). (See Figure 1)
3. Applying even pressure to the top of the mount, press the entire assembly into the hole from the front of the panel.[4] (See Figure 2)

NOTE: For thinner panels, the mount may be pressed into the panel first, then the light bar may be pressed into the mount from the back side of the panel.

Notes:
3. A 3.18 mm (0.125 inch) diameter mill may be used.
4. Repetitive insertion of the mount into the panel will degrade the retention force of the mount.

Suggested Punch Sources

Hole punches may be ordered from one of the following sources:

Danly Machine Corporation
Punchrite Division
15400 Brookpark Road
Cleveland, OH 44135
(216) 267-1444

Ring Division
The Producto Machine Company
Jamestown, NY 14701
(800) 828-2216

Porter Precision Products Company
12522 Lakeland Road
Santa Fe Springs, CA 90670
(213) 946-1531

Di-Acro Division
Houdaille Industries
800 Jefferson Street
Lake City, MN 55041
(612) 345-4571

Installation Sketches

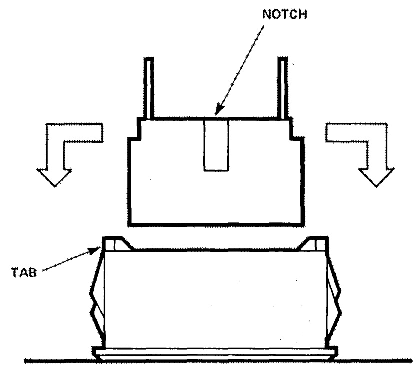


Figure 1. Installation of a Light Bar into a Panel Mount

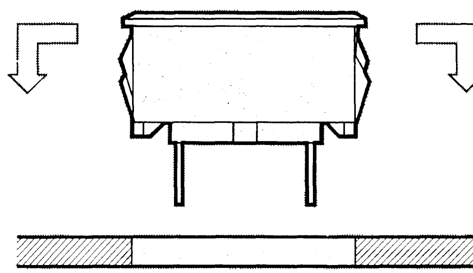


Figure 2. Installation of the Light Bar/Panel Mount Assembly into a Front Panel

HEWLETT PACKARD

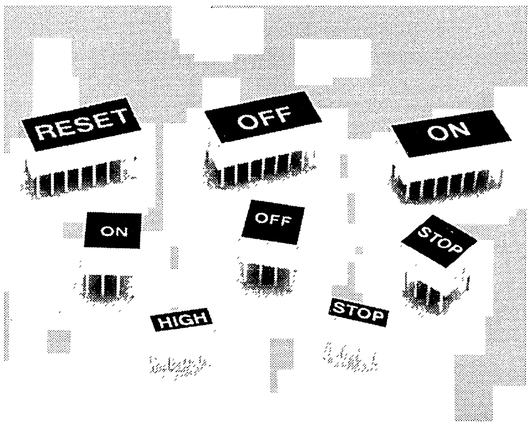
LIGHT BAR LEGENDS

STANDARD OPTIONS FOR:
HLMP-2300/-2400/-2500/-2000 SERIES
HLMP-2655/-2755/-2855/-2155 SERIES
HLMP-2685/-2785/-2885/-2185 SERIES

TECHNICAL DATA JANUARY 1986

Features

- **FACTORY INSTALLATION SAVES TIME IN MANUFACTURING, PURCHASING AND STOCKING**
- **LIGHT OR DARK FIELD FORMAT (DARK FIELD STANDARD)**
- **HIGH STRENGTH ADHESIVE BACKING**
- **CUSTOM LEGENDS AVAILABLE**



Description

Light bar legends are available with factory installation on all light bars, using either standard or custom legends. Options L00 through L06 address our standard legend formats and can be specified for various size light bars in accordance with the Device/Option Selection Matrix.

Ordering Information

To order light bar legends, include the appropriate option code along with the device catalog number. Example: to order the HLMP-2655 with the "OFF" legend, order as follows: HLMP-2655 Option L01. Minimum order quantities vary by part number.

For custom legends, please contact your local Hewlett-Packard sales office or franchised Hewlett-Packard distributor.

Option Guide

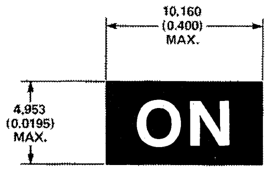
Option	Legend Title
L00	ON
L01	OFF
L02	READY
L03	HIGH
L04	LOW
L05	RESET
L06	STOP

Ratings and Characteristics

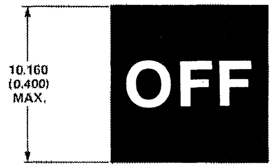
The absolute maximum ratings, mechanical dimensions and electrical characteristics for light bars with legends are the same as for the standard catalog devices. Refer to the basic data sheet for the specified values. For use in applications involving high humidity conditions, please contact your Hewlett-Packard representative.

As with the standard light bar devices, the radiation pattern is approximately Lambertion. The luminous sterance for a given device is the same as for the standard light bar products. To calculate this value, refer to the "Optical" section of the LED Light Bars data sheet in this catalog.

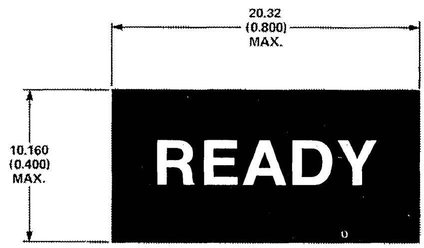
Dimensional Specifications for Legends



HLMP-2300 Series



HLMP-2655 Series



HLMP-2685 Series

Device/Option Selection Matrix

		Applicable Light Bar Series		
Option	**Legend**	**HLMP-2300/-2400/ -2500/-2000**	**HLMP-2655/-2755/ -2855/-2155**	**HLMP-2685/-2785/ -2885/-2185**
L00	ON	X	X	X
L01	OFF	X	X	X
L02	READY			X
L03	HIGH	X	X	X
L04	LOW	X	X	X
L05	RESET			X
L06	STOP		X	X

HEWLETT PACKARD

INTENSITY SELECTED LIGHT BARS

TECHNICAL DATA JANUARY 1986

Features

- **INTENSITY SELECTION IMPROVES UNIFORMITY OF LIGHT OUTPUT FROM UNIT TO UNIT. AVAILABLE IN HIGH EFFICIENCY RED, YELLOW, AND HIGH PERFORMANCE GREEN.**
- **TWO CATEGORY SELECTION SIMPLIFIES INVENTORY CONTROL AND ASSEMBLY.**

Description

Light bars are now available from Hewlett-Packard which are selected from two adjacent intensity categories. These select light bars are basic catalog devices which are pre-sorted for luminous intensity then selected from two predetermined adjacent categories and assigned to one convenient part number.

Example: Two luminous intensity categories are selected from the basic catalog HLMP-2300 production distribution and assigned to the part number HLMP-2300 option S02.

Selected light bars are ideal for applications which require two or more light bars per panel.

Luminous intensity selection is available for high efficiency red, yellow, and high performance green.

To ensure our customers a steady supply of product, HP must offer selected units from the center of our production distribution. If our production distribution shifts, we will need to change the intensity range of the selected units our customers receive. Typically, an intensity may have to be changed once every 1 to 3 years.

Current intensity selection information is available through a category reference chart which is available through your local field sales engineer or local franchised distributor.

Absolute Maximum Ratings and Electrical/Optical Characteristics

The absolute maximum ratings, mechanical dimensions, and electrical/optical characteristics are identical to the basic catalog device.

LIGHT BARS AND BAR GRAPH ARRAYS

Device Selection Guide

The following table summarizes which basic catalog devices are available with category selection.

Package	High Efficiency Red	Yellow	Green
4 Pin In-Line	HLMP-2300 Option S02	HLMP-2400 Option S02	HLMP-2500 Option S02
8 Pin In-Line	HLMP-2350 Option S02	HLMP-2450 Option S02	HLMP-2550 Option S02
8 Pin DIP Dual Arrangement	HLMP-2600 Option S02	HLMP-2700 Option S02	HLMP-2800 Option S02
16 Pin DIP Quad Arrangement	HLMP-2620 Option S02	HLMP-2720 Option S02	HLMP-2820 Option S02
16 Pin DIP Dual Bar Arrangement	HLMP-2635 Option S02	HLMP-2735 Option S02	HLMP-2835 Option S02
8 Pin DIP Square Arrangement	HLMP-2655 Option S02	HLMP-2755 Option S02	HLMP-2855 Option S02
16 Pin DIP Dual Square Arrangement	HLMP-2670 Option S02	HLMP-2770 Option S02	HLMP-2870 Option S02
16 Pin DIP Single Bar Arrangement	HLMP-2685 Option S02	HLMP-2785 Option S02	HLMP-2885 Option S02

Note: Option S02 designates a two intensity category selection. Option S02s of different part numbers may not have the same apparent brightness. Contact your HP Field Sales Office for design assistance.

HEWLETT PACKARD

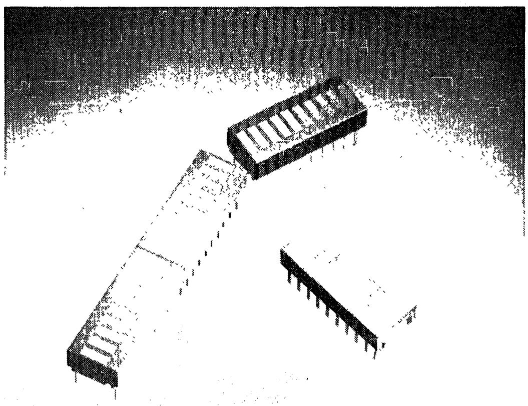
10-ELEMENT BAR GRAPH ARRAY

RED HDSP-4820
HIGH-EFFICIENCY RED HDSP-4830
YELLOW HDSP-4840
HIGH PERFORMANCE GREEN HDSP-4850
EMERALD GREEN HDSP-4890
MULTICOLOR HDSP-4832
MULTICOLOR HDSP-4836

TECHNICAL DATA JANUARY 1986

Features

- CUSTOM MULTICOLOR ARRAY CAPABILITY
- MATCHED LEDs FOR UNIFORM APPEARANCE
- END STACKABLE
- PACKAGE INTERLOCK ENSURES CORRECT ALIGNMENT
- LOW PROFILE PACKAGE
- RUGGED CONSTRUCTION— RELIABILITY DATA SHEETS AVAILABLE
- LARGE, EASILY RECOGNIZABLE SEGMENTS
- HIGH ON-OFF CONTRAST, SEGMENT TO SEGMENT
- WIDE VIEWING ANGLE
- CATEGORIZED FOR LUMINOUS INTENSITY
- HDSP-4832/-4836/-4840/-4850/-4890 CATEGORIZED FOR DOMINANT WAVELENGTH



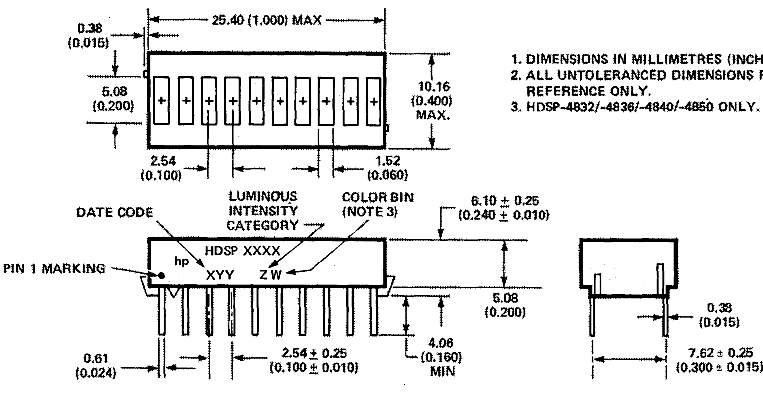
Description

These 10-element LED arrays are designed to display information in easily recognizable bar graph form. The packages are end stackable and therefore capable of displaying long strings of information. Use of these bar graph arrays eliminates the alignment, intensity, and color matching problems associated with discrete LEDs. The HDSP-4820/-4830/-4840/-4850/-4890 each contain LEDs of just one color. The HDSP-4832/-4836 are multicolor arrays with High-Efficiency Red, Yellow, and Green LEDs in a single package. CUSTOM MULTICOLOR ARRAYS ARE AVAILABLE WITH MINIMUM DELIVERY REQUIREMENTS. CONTACT YOUR LOCAL DISTRIBUTOR OR HP SALES OFFICE FOR DETAILS.

Applications

- INDUSTRIAL CONTROLS
- INSTRUMENTATION
- OFFICE EQUIPMENT
- COMPUTER PERIPHERALS
- CONSUMER PRODUCTS

Package Dimensions

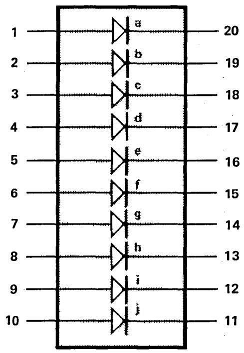


Absolute Maximum Ratings[9]

Parameter	HDSP-4820	HDSP-4830	HDSP-4840	HDSP-4850	HDSP-4890
Average Power Dissipation per LED (T = 25° C)[1]	125 mW	125 mW	125 mW	125 mW	125 mW
Peak Forward Current per LED	150 mA[2]	90 mA[3]	60 mA[3]	90 mA[3]	90 mA[3]
DC Forward Current per LED	30 mA[4]	30 mA[5]	30 mA[6]	30 mA[7]	30 mA[7]
Operating Temperature Range	-40° C to +85° C			-20° C to +85° C	
Storage Temperature Range	-40° C to +85° C				
Reverse Voltage per LED	3.0 V				
Lead Soldering Temperature (1.59 mm (1/16 inch) below seating plane[8]	260° C for 3 sec				

NOTES:
1. Derate maximum average power above $T_A = 25°$ C at 1.67 mW/° C. This derating assumes worst case $R\Theta_{J-A} = 600°$ C/W/LED.
2. See Figure 1 to establish pulsed operating conditions.
3. See Figure 6 to establish pulsed operating conditions.
4. Derate maximum DC current above $T_A = 63°$ C at 0.81 mA/° C per LED. This derating assumes worst case $R\Theta_{J-A} = 600°$ C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 2.
5. Derate maximum DC current above $T_A = 50°$ C at 0.6 mA/° C per LED. This derating assumes worst case $R\Theta_{J-A} = 600°$ C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 7.
6. Derate maximum DC current above $T_A = 70°$ C at 0.67 mA/° C per LED. This derating assumes worst case $R\Theta_{J-A} = 600°$ C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 8.
7. Derate maximum DC current above $T_A = 37°$ C at 0.48 mA/° C per LED. This derating assumes worst case $R\Theta_{J-A} = 600°$ C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 9.
8. Clean only in water, Isopropanol, Ethanol, Freon TF or TE (or equivalent) and Genesolve DI-15 (or equivalent).
9. Absolute maximum ratings for the HER, Yellow, and Green elements of the multicolor arrays are identical to the HDSP-4830/-4840/-4850 maximum ratings.

Internal Circuit Diagram



PIN	FUNCTION	PIN	FUNCTION
1	ANODE-a	11	CATHODE-j
2	ANODE-b	12	CATHODE-i
3	ANODE-c	13	CATHODE-h
4	ANODE-d	14	CATHODE-g
5	ANODE-e	15	CATHODE-f
6	ANODE-f	16	CATHODE-e
7	ANODE-g	17	CATHODE-d
8	ANODE-h	18	CATHODE-c
9	ANODE-i	19	CATHODE-b
10	ANODE-j	20	CATHODE-a

Multicolor Array Segment Colors

Segment	HDSP-4832 Segment Color	HDSP-4836 Segment Color
a	HER	HER
b	HER	HER
c	HER	Yellow
d	Yellow	Yellow
e	Yellow	Green
f	Yellow	Green
g	Yellow	Yellow
h	Green	Yellow
i	Green	HER
j	Green	HER

Electrical/Optical Characteristics at $T_A = 25°$ C[4]

RED HDSP-4820

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	$I_F = 20$ mA	610	1250		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[2]	λ_d			645		nm
Forward Voltage per LED	V_F	$I_F = 20$ mA		1.6	2.0	V
Reverse Voltage per LED	V_R	$I_R = 100\ \mu A$	3	12[5]		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\Theta_{J-PIN}$			300		°C/W/LED

HIGH-EFFICIENCY RED HDSP-4830

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	$I_F = 10$ mA	900	3500		μcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[2]	λ_d			626		nm
Forward Voltage per LED	V_F	$I_F = 20$ mA		2.1	2.5	V
Reverse Voltage per LED	V_R	$I_R = 100\ \mu A$	3	30[5]		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			300		°C/W/ LED

YELLOW HDSP-4840

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	$I_F = 10$ mA	600	1900		μcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[2,3]	λ_d		581	585	592	nm
Forward Voltage per LED	V_F	$I_F = 20$ mA		2.2	2.5	V
Reverse Voltage per LED	V_R	$I_R = 100\ \mu A$	3	40[5]		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			300		°C/W/ LED

GREEN HDSP-4850

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	$I_F = 10$ mA	600	1900		μcd
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[2,3]	λ_d			571	577	nm
Forward Voltage per LED	V_F	$I_F = 10$ mA		2.1	2.5	V
Reverse Voltage per LED	V_R	$I_R = 100\ \mu A$	3	50[5]		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			300		°C/W/ LED

EMERALD GREEN HDSP-4890

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity Per LED (Unit Average)[1]	I_V	$I_F = 10$ mA	250	1600		μcd
Peak Wavelength	λ_{PEAK}			556		nm
Dominant Wavelength[2,3]	λ_d			558		nm
Forward Voltage Per LED	V_F	$I_F = 10$ mA		2.2	2.5	V
Reverse Voltage Per LED	V_R	$I_R = 100\ \mu A$	3	50[5]		
Temperature Coefficient V_F Per LED	$\Delta V_F/°C$			–2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			300		°C/W/LED

NOTES:
1. The bar graph arrays are categorized for luminous intensity. The category is designated by a letter located on the side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
3. The HDSP-4832/-4836/-4840/-4850/-4890 bar graph arrays are categorized by dominant wavelength with the category designated by a number adjacent to the intensity category letter. Only the yellow elements of the HDSP-4832/-4836 are categorized for color.
4. Electrical/optical characteristics of the High-Efficiency Red elements of the HDSP-4832/-4836 are identical to the HDSP-4830 characteristics. Characteristics of Yellow elements of the HDSP-4832/-4836 are identical to the HDSP-4840. Characteristics of Green elements of the HDSP-4832/-4836 are identical to the HDSP-4850.
5. Reverse voltage per LED should be limited to 3.0 V Max.

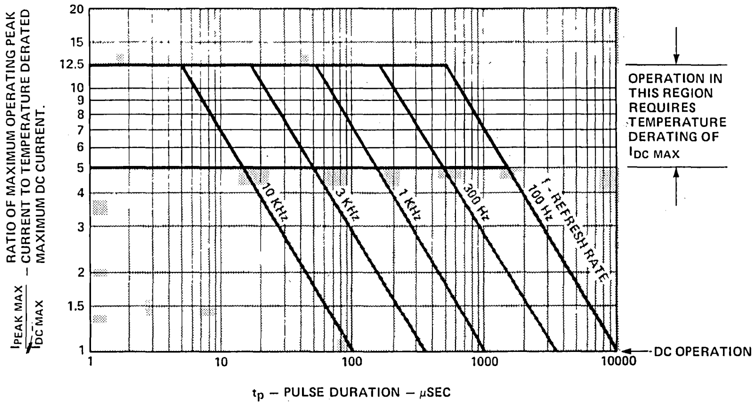


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

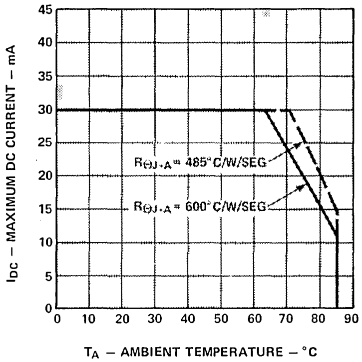


Figure 2. Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings based on Maximum Allowable Thermal Resistance, LED Junction-to-Ambient on a per LED basis. $T_{JMAX} = 100°C$

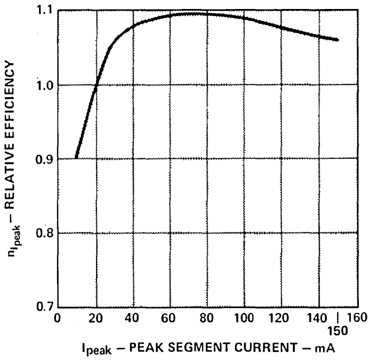


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

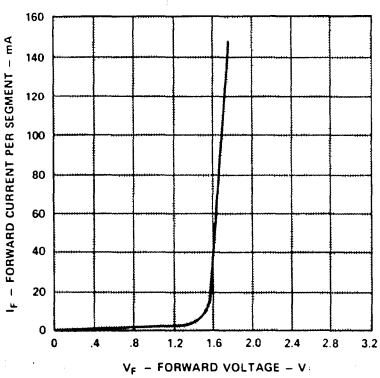


Figure 4. Forward Current vs. Forward Voltage

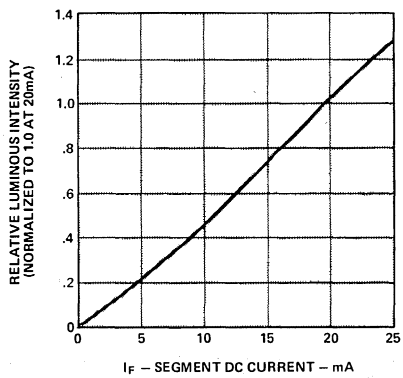


Figure 5. Relative Luminous Intensity vs. D.C. Forward Current

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

LIGHT BARS AND BAR GRAPH ARRAYS

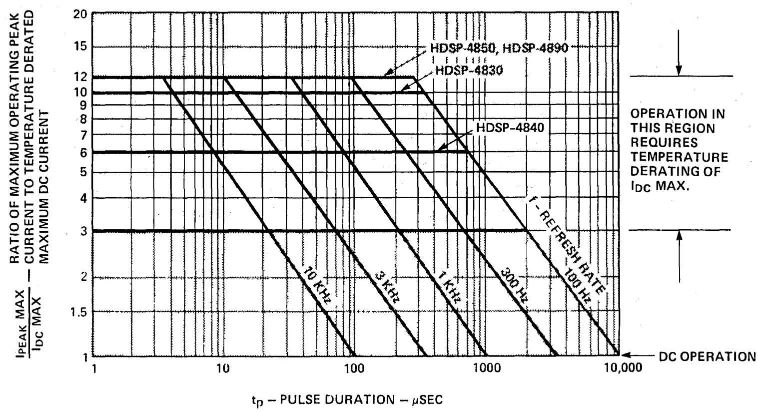


Figure 6. HDSP-4830/-4840/-4850/-4890 Maximum Tolerable Peak Current vs. Pulse Duration

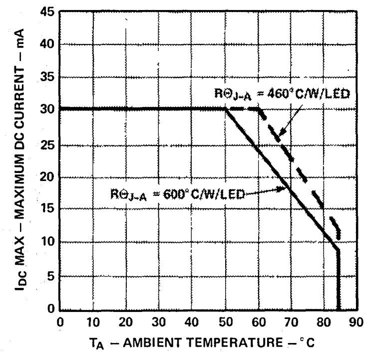


Figure 7. HDSP-4830 Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED basis. $T_{J\ MAX}$ = 100° C.

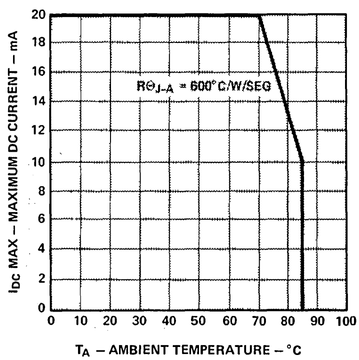


Figure 8. HDSP-4840 Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED basis. $T_{J\ MAX}$ = 100° C.

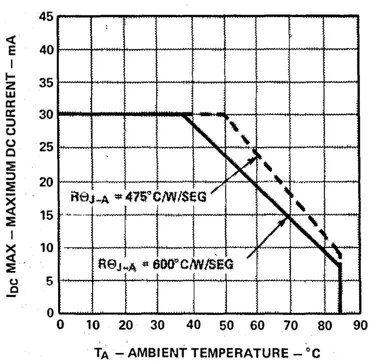


Figure 9. HDSP-4850/-4890 Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED basis. $T_{J\ MAX}$ = 100° C.

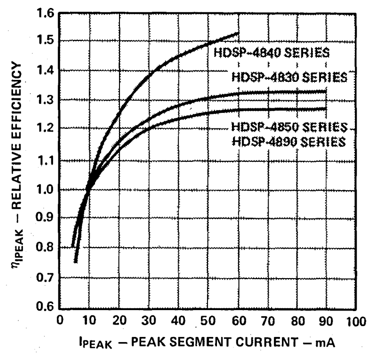


Figure 10. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

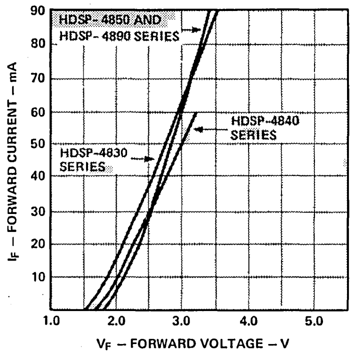


Figure 11. Forward Current vs. Forward Voltage

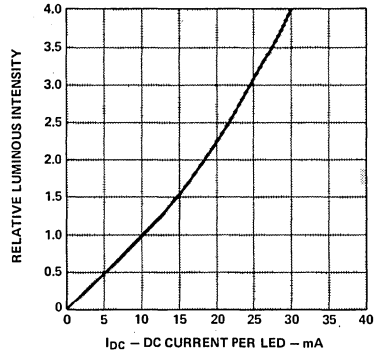


Figure 12. HDSP-4830/-4840/-4850/-4890 Relative Luminous Intensity vs. D.C. Forward Current

Electrical

These versatile bar graph arrays are composed of ten light emitting diodes. The light from each LED is optically stretched to form individual elements. The diodes in the HDSP-4820 bar graph utilize a Gallium Arsenide Phosphide (GaAsP) epitaxial layer on a Gallium Arsenide (GaAs) Substrate. The HDSP-4830/-4840 bar graphs utilize a GaAsP epitaxial layer on a GaP substrate to produce the brighter high-efficiency red and yellow displays. The HDSP-4850/-4890 bar graph arrays utilize a GaP epitaxial layer on a GaP substrate. The HDSP-4832/-4836 multicolor arrays have high efficiency red, yellow, and green LEDs in one package.

These display devices are designed to allow strobed operation. The typical forward voltage values, scaled from Figure 4 or 11, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following $V_{F\ MAX}$ models.

HDSP-4820 (Red)

$V_{F\ MAX} = 1.75\ V + I_{PEAK}\ (12.5\Omega)$
For: $I_{PEAK} \geq 5$ mA

HDSP-4830/-4840 (High Efficiency Red/Yellow)

$V_{F\ MAX} = 1.75V + I_{PEAK}\ (38\Omega)$
For $I_{PEAK} \geq 20$ mA

$V_{F\ MAX} = 1.6V + I_{DC}\ (45\Omega)$
For: $5\ \text{mA} \leq I_{DC} \leq 20$ mA

HDSP-4850/-4890 (Green/Emerald)

$V_{F\ MAX} = 2.0V + I_{PEAK}\ (50\Omega)$
For: $I_{PEAK} > 5$ mA

Refresh rates of 1 KHz or faster provide the most efficient operation resulting in the maximum possible time averaged luminous intensity.

The time averaged luminous intensity may be calculated using the relative efficiency characteristic shown in Figures 3 and 10. The time averaged luminous intensity at T_A = 25°C is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{F\ AVG}}{I_{F\ SPEC\ AVG}}\right](\eta I_{PEAK})\ (I_V\ SPEC)$$

Example: For HDSP-4830 operating at $I_{PEAK} = 50$ mA, 1 of 4 Duty Factor

$$\eta I_{PEAK} = 1.35\ (\text{at } I_{PEAK} = 50\ \text{mA})$$

$$I_{V\ TIME\ AVG} = \left[\frac{12.5\ \text{mA}}{10\ \text{mA}}\right](1.35)\ 2280\ \mu cd = 3847\ \mu cd$$

For Further Information Concerning Bar Graph Arrays and Suggested Drive Circuits, Consult HP Application Note 1007 Entitled "Bar Graph Array Applications".

HEWLETT PACKARD

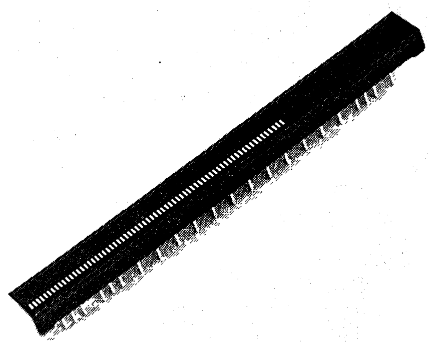
101 ELEMENT BAR GRAPH ARRAY

RED HDSP-8820
HIGH EFFICIENCY RED HDSP-8825
HIGH PERFORMANCE GREEN HDSP-8835

TECHNICAL DATA JANUARY 1986

Features

- **HIGH RESOLUTION (1%)**
- **EXCELLENT ELEMENT APPEARANCE**
  Wide, Recognizable Elements
  Matched LEDs for Uniformity
  Excellent Element Alignment
- **SINGLE-IN-LINE PACKAGE DESIGN**
  Sturdy Leads on Industry Standard 2.54 mm (0.100") Centers
  Environmentally Rugged Package
  Common Cathode Configuration
- **LOW POWER REQUIREMENTS**
  1.0 mA Average per Element at 1% Duty Cycle
- **SUPPORT ELECTRONICS**
  Easy Interface with Microprocessors



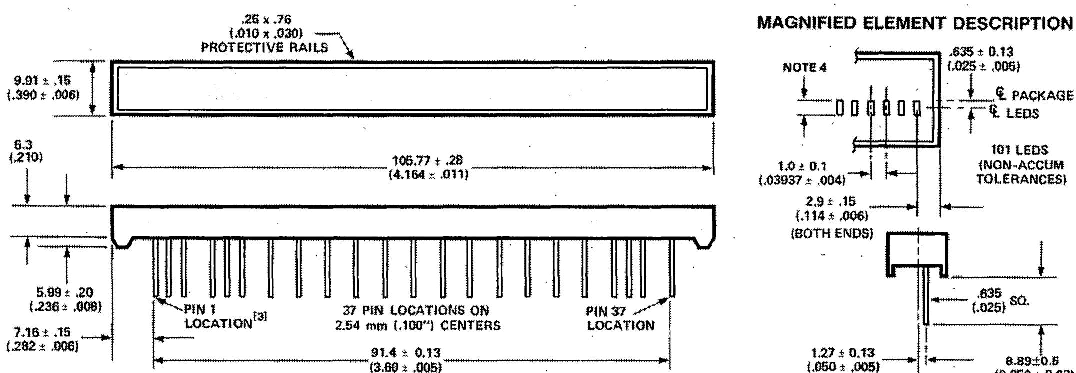
Description

The HDSP-88XX series is a family of 101-element LED linear arrays designed to display information in easily recognizable bar graph or position indicator form. The HDSP-8820, utilizing red GaAsP LED chips assembled on a PC board and enclosed in a red polycarbonate cover with an epoxy backfill seal, has 1.52 mm (0.060 inch) wide segments. The HDSP-8825 and HDSP-8835 are high efficiency red and high performance green respectively, each with a 1.02 mm (0.040 inch) segment width. The HDSP-8825 and HDSP-8835 have a clear polycarbonate lens. Mechanical considerations and pin-out are identical among all 3 devices. The common cathode chips are addressed via 22 single-in-line pins extending from the back side of the package.

Applications

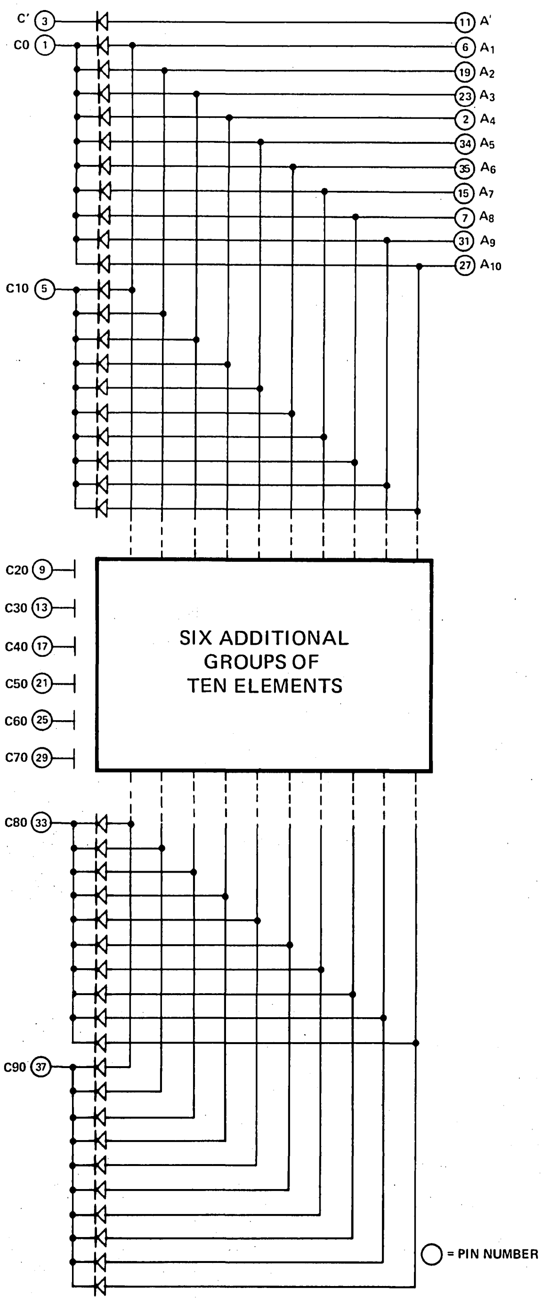
- **INDUSTRIAL PROCESS CONTROL SYSTEMS**
- **EDGEWISE PANEL METERS**
- **INSTRUMENTATION**
- **POSITION INDICATORS**
- **FLUID LEVEL INDICATORS**

Package Dimensions[1, 2]



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY INK DOT ADJACENT TO LEAD AND HP PART NUMBER ON BACK OF PACKAGE.
4. SEGMENT WIDTH DIMENSION IS 1.52 mm (.060) FOR HDSP-8820 AND 1.02 mm (.040) FOR HDSP-8825 AND HDSP-8835. ALL OTHER DIMENSIONS INCLUDING CENTERLINE OF LEDs AND PACKAGE ARE IDENTICAL ON ALL 3 DEVICES.

Internal Circuit Diagram (5, 6)



NOTES:
5. ELEMENT LOCATION NUMBER = COMMON CATHODE NUMBER + ANODE NUMBER. FOR EXAMPLE, ELEMENT 83 IS OBTAINES BY ADDRESSING C80 AND A3.
6. A' AND C' ARE ANODE AND CATHODE OF ELEMENT ZERO.

Device Pin Description

PIN LOCATION	FUNCTION
1	C0
2	A4
3	C'(6)
4	No Pin
5	C10
6	A1
7	A8
8	No Pin
9	C20
10	No Pin
11	A'(6)
12	No Pin
13	C30
14	No Pin
15	A7
16	No Pin
17	C40
18	No Pin
19	A2
20	No Pin
21	C50
22	No Pin
23	A3
24	No Pin
25	C60
26	No Pin
27	A10
28	No Pin
29	C70
30	No Pin
31	A9
32	No Pin
33	C80
34	A5
35	A6
36	No Pin
37	C90

Absolute Maximum Ratings

Parameter	HDSP-8820	HDSP-8825	HDSP-8835
Average Power per Element ($T_A = 25°C$)	15 mW	20 mW	20 mW
Peak Forward Current per Element ($T_A = 25°C$)[7] (Pulse Width $\leq 300\ \mu s$)	200 mA	150 mA	150 mA
Average Forward Current per Element ($T_A = 25°C$)[8]	7 mA	5 mA	5 mA
Operating Temperature Range	–40° to +85°C	–40° to +85°C	–40° to +85°C
Storage Temperature Range	–40° to +85°C	–40° to +85°C	–40° to +85°C
Reverse Voltage per Element or DP	5.0 V	5.0 V	5.0 V
Lead Solder Temperature 1.59 mm [1.16 inch] below seating plane[9]	260°C for 3 sec.	260°C for 3 sec.	260°C for 3 sec.

Notes:
7. See Figures 1 and 2 to establish pulsed operating conditions.
8. Derate maximum average forward current above $T_A = 70°C$ at 0.16 mA/°C/Element for the HDSP-8820 and 0.11 mA/°C/Element for the HDSP-8825 and HDSP-8835. See Figures 3 and 4.
9. Clean only in water, Isopropanol, Ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent). See mechanical section of this data sheet for information on wave soldering conditions.

Electrical/Optical Characteristics at $T_A = 25°C$

RED HDSP-8820

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Time averaged Luminous Intensity per Element (Unit average) [10]	I_V	100 mA Pk.: 1 of 110 Duty Factor	8	20		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength [11]	λ_d			640		nm
Forward Voltage per Element	V_F	$I_F = 100$ mA		1.7	2.1	V
Reverse Voltage per Element	V_R	$I_R = 100\ \mu A$	3.0			V
Temperature Coefficient V_F per Element	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\Theta_{J-PIN}$			700		°C/W/ LED

HIGH EFFICIENCY RED HDSP-8825

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Time averaged Luminous Intensity per Element (Unit average) [10]	I_V	100 mA Pk.: 1 of 110 Duty Factor	60	175		μcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength [11]	λ_d			626		nm
Forward Voltage per Element	V_F	$I_F = 100$ mA		2.3	3.1	V
Reverse Voltage per Element	V_R	$I_R = 100\ \mu A$	3.0			V
Temperature Coefficient V_F per Element	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\Theta_{J-PIN}$			1000		°C/W/ LED

Electrical/Optical Characteristics at $T_A = 25°C$ (continued)

HIGH PERFORMANCE GREEN HDSP-8835

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Time Averaged Luminous Intensity per Element (Unit average)[10]	I_V	100 mA Pk.: 1 of 110 Duty Factor	70	175		μcd
Peak Wavelength	λ_{PEAK}			568		nm
Dominant Wavelength[11]	λ_d			574		nm
Forward Voltage per Element	V_F	$I_F = 100$ mA		2.3	3.1	V
Reverse Voltage per Element	V_R	$I_F = 100\ \mu A$	3.0			V
Temperature Coefficient V_F per Element	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\Theta_{J-PIN}$			1000		°C/W/ LED

Notes:
10. Operation at peak currents of less than 100 mA may cause intensity mismatch. Consult factory for low current operation.
11. The dominant wavelength, λd, is derived from the CIE chromaticity diagram and is the single wavelength which defines the color of the device.

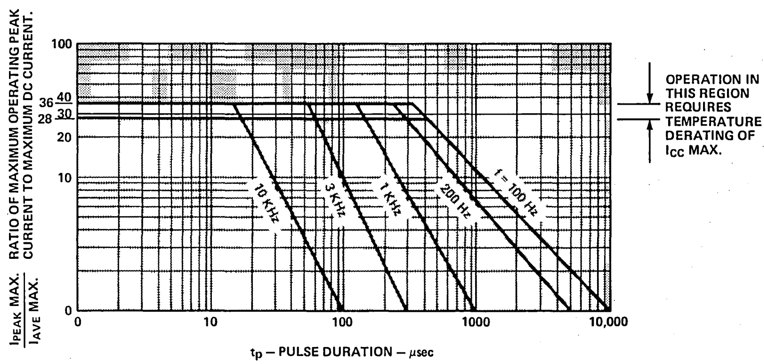


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration HDSP-8820

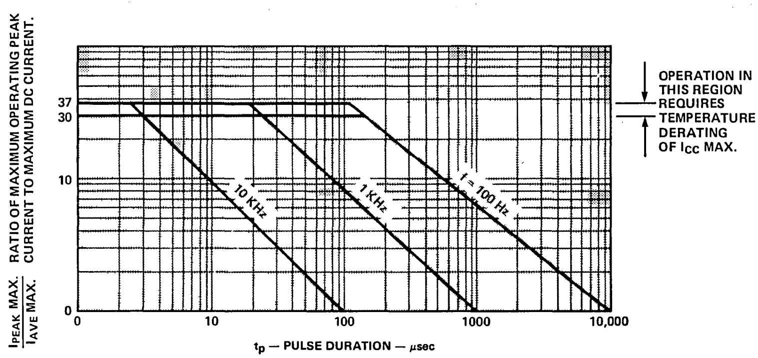


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration HDSP-8825 and HDSP-8835

LIGHT BARS AND BAR GRAPH ARRAYS

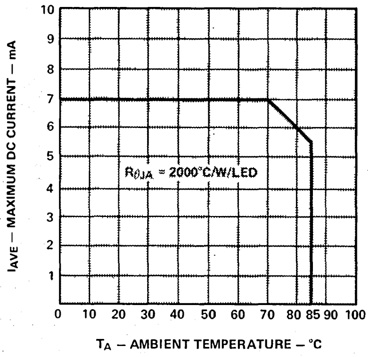


Figure 3. Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings based on Maximum Allowable Thermal Resistance, LED Junction-to-Ambient on a per LED basis. T_{JMAX} = 115° C HDSP-8820

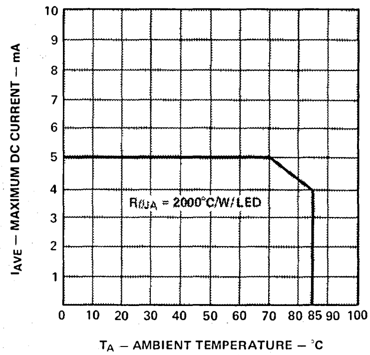


Figure 4. Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings based on Maximum Allowable Thermal Resistance, LED Junction-to-Ambient on a per LED basis. T_{JMAX} = 115° C HDSP-8825/HDSP-8835

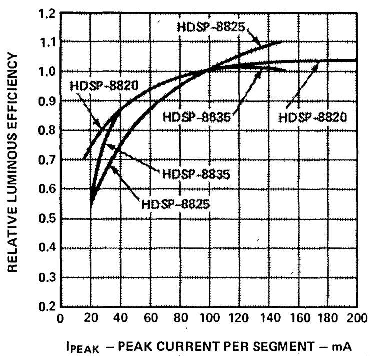


Figure 5. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

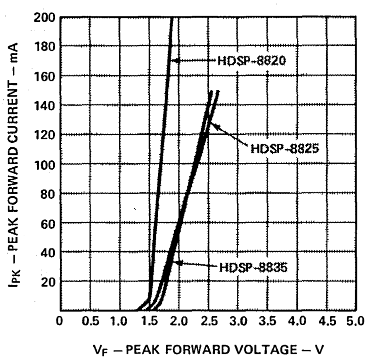


Figure 6. Forward Current vs. Forward Voltage

For A Detailed Explanation on the Use of Data Sheet Information, See Application Note 1005.

Operational Considerations

ELECTRICAL

The HDSP-88XX is a 101 element bar graph array. The linear array is arranged as ten groups of ten LED elements plus one additional element. The ten elements of each group have common cathodes. Like elements in the ten groups have common anodes. The device is addressed via 22 single-in-line pins extending from the back side of the display.

This display is designed specifically for strobed (multiplexed) operation. Minimum peak forward current at which all elements will be illuminated is 15 mA. Display aesthetics are specified at 100 mA, 1/110 DF, peak forward current. The typical forward voltage values, scaled from Figure 6 should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F model:

HDSP-8820

$V_{FMAX} = 2.02\ V + I_{PEAK}\ (0.8\ \Omega)$
For $I_{PEAK} > 40$ mA

HDSP-8825

$V_{FMAX} = 1.7\ V + I_{PEAK}\ (14\ \Omega)$
For $I_{PEAK} > 40$ mA

HDSP-8835

$V_{FMAX} = 1.7\ V + I_{PEAK}\ (14\ \Omega)$
For $I_{PEAK} > 40$ mA

The time averaged luminous intensity at $T_A = 25°C$ may be calculated using:

$$I_V\ \text{Time Avg.} = \left[\frac{I_{F-AVG}}{I_{F-SPEC-AVG}}\right] \cdot \eta I_{PEAK} \cdot I_{V-SPEC}$$

where η, relative efficiency, may be determined from Figure 5.

The circuit in Figure 7 displays an analog input voltage in bar graph form with 101 bit resolution. The 74390 dual decade counter has been configured to count from 0 to 99. The 1Q outputs correspond to "ones" and the 2Q outputs correspond to "tens". The "one" outputs from the counter drives the display element anodes through a 7442 1 of 10 BCD decoder. Sprague UDN 2585 drivers source the anodes with 80 mA peak/segment. The "ten" outputs from the counter drive the group cathodes through a 74145 BCD decoder. The circuit multiplexes segments 100 to 91 first, then segments 90 to 81, and so on with segments 10 to 1 last. During the time that the output from the T.I. TL507C A/D converter is low the corresponding display elements will be illuminated.

The TL507C is an economical A/D converter with 7 bit resolution. The single output is pulse-width-modulated to correspond to the analog input voltage magnitude. With $V_{CC} = 5$ V the analog input voltage range is 1.3 V to 3.9 V. The TL507C output is reset each time the 74390 resets. Duration of the high output pulse is shorter for larger analog input voltages. A high output from the TL507C disables the display by forcing the 7442 inputs to an invalid state. Hence, as the analog input voltage increases more elements of the bar graph display are illuminated. Display element zero is DC driven.

The circuit in Figure 8 uses the HDSP-88XX as a 100 bit position indicator. Two BCD input words define the position of the illuminated element. Display duty factor, 1/100, is controlled by the $\overline{\text{ENABLE}}$ signal.

MECHANICAL

Suitable conditions for wave soldering depend on the specific kind of equipment and procedure used. A cool down period after flow solder and before flux rinse is recommended. For more information, consult the local Hewlett-Packard Sales Office or Hewlett-Packard Optoelectronics, Palo Alto, California.

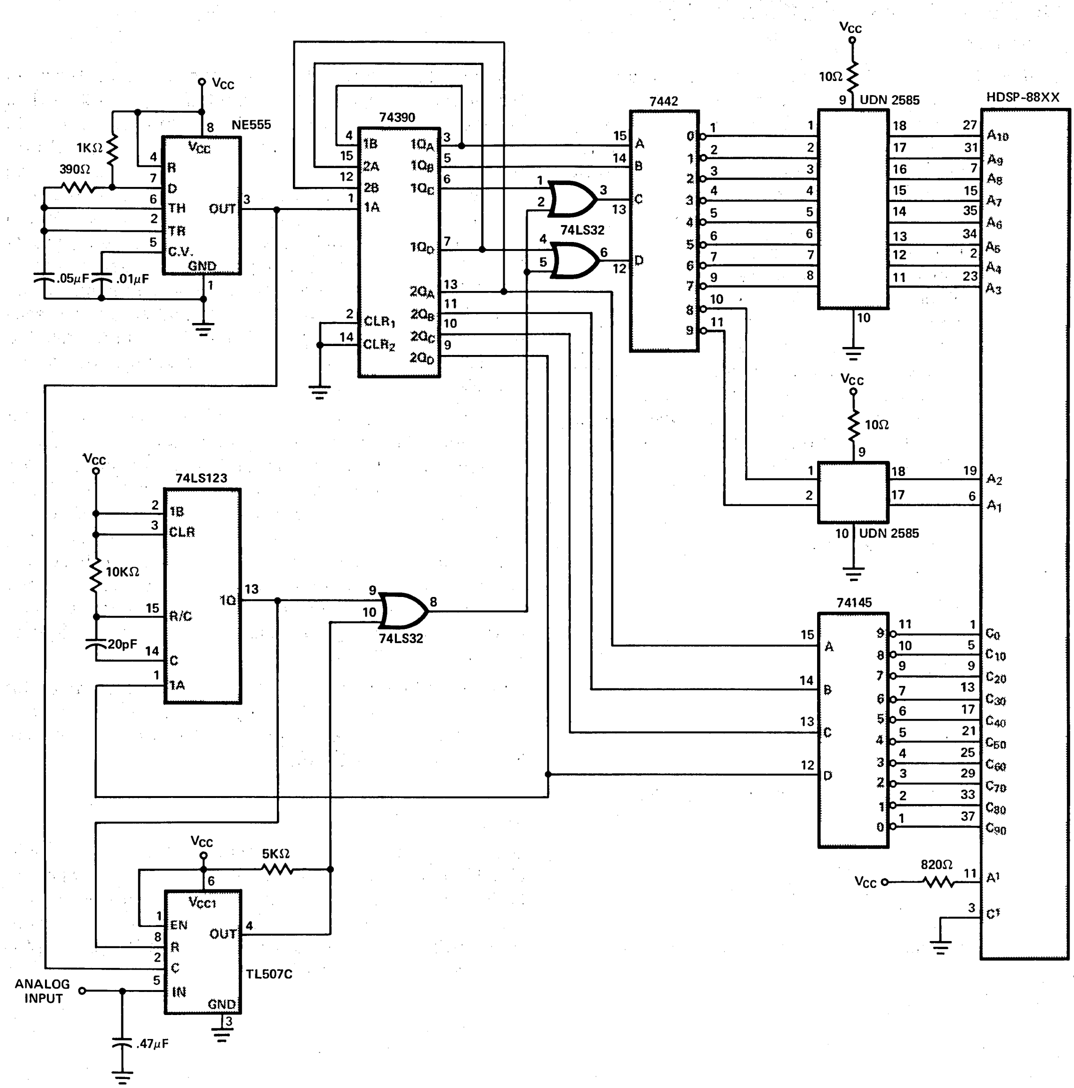


Figure 7. 101 Element Bar Graph

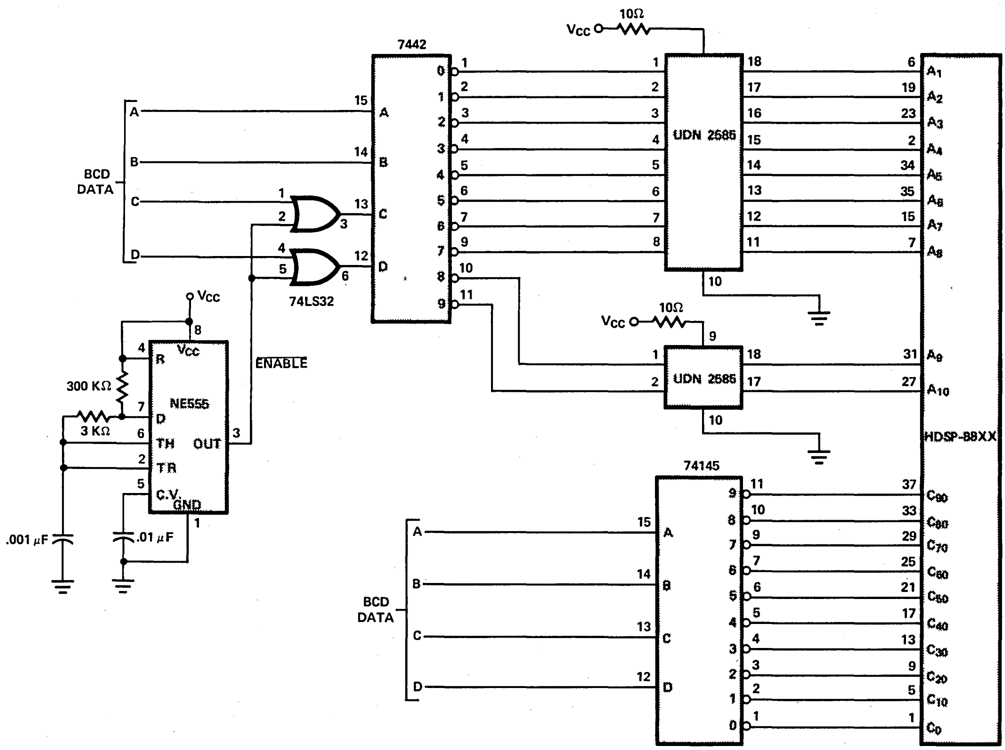
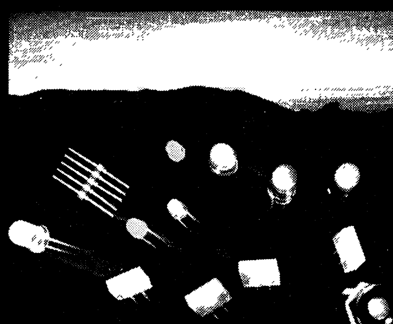


Figure 8. 100 Element Position Indicator

[redacted]

6. Solid State Lamps



Solid State Lamps

New products are the keystone of the Hewlett-Packard LED lamp products. This year the broad line of lamp products is growing by five new major product families.

Hewlett-Packard has two surface mount lamp families, one for front panel or status indication applications and the other for backlighting applications. Both families are compatible with automatic placement equipment and reflow solder processes.

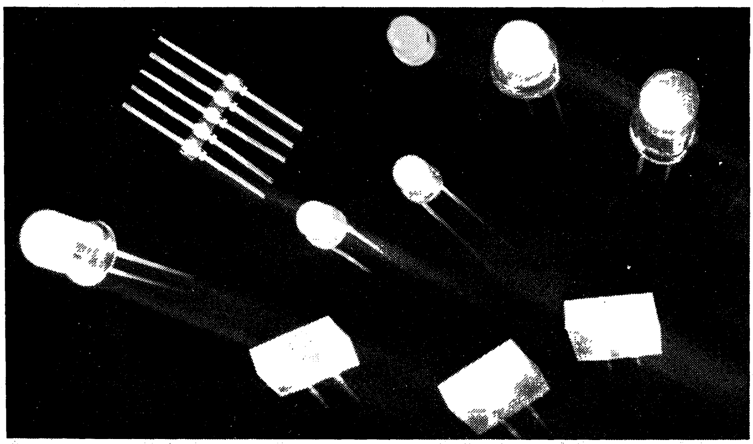
For the front panel designer the new 2mm and 4mm flat top lamps provide wide viewing angles and uniform light output to provide excellent flush mounting ability.

Aluminum Gallium Arsenide (AlGaAs) is an improved red LED technology which provides higher brightness and better efficiency in an LED lamp.

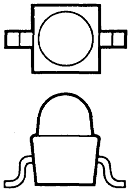
Orange (608nm) and Emerald Green (556nm) are additions to the broad range of colors available for Hewlett-Packard lamps.

Last year HP introduced a family of T-1 3/4 right angle status indicators, which provide a lamp with pre-formed leads inserted into a high contrast, flat seating molded plastic package. This year the right angle family is complete with the addition of T-1 and Subminiature package sizes.

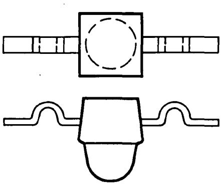
In addition to new products, Hewlett-Packard offers a broad selection of T-1, T-1 3/4, and Subminiature lamps.



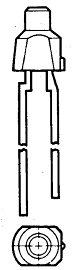
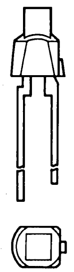
Surface Mount Lamps (Gull Wing Lead)

Device		Description			Typical Luminous Intensity	2θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-6000 Option 011	Red (640 nm)	Subminiature Gull Wing Lead Configuration	Tinted Diffused	1.2 mcd @ 10 mA	90°	1.6 V @ 10 mA	6-17
	HLMP-6300 Option 011	High Efficiency Red (626 nm)			3.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-6400 Option 011	Yellow (585 nm)					2.2 V @ 10 mA	
	HLMP-6500 Option 011	Green (569 nm)					2.3 V @ 10 mA	
	HLMP-7000 Option 011	Low Current High Efficiency Red (626 nm)			0.8 mcd @ 2 mA	70°	1.8 V @ 2 mA	
	HLMP-7019 Option 011	Low Current Yellow (585 nm)			0.6 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-7040 Option 011	Low Current Green (569 nm)						
	HLMP-6600 Option 011	Integrated Resistor High Efficiency Red (626 nm)			2.4 mcd @ 5 V	80°	9.6 mA @ 5 V	
	HLMP-6620 Option 011				0.6 mcd @ 5 V		3.5 mA @ 5 V	

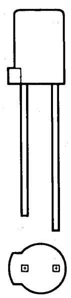
Surface Mount Lamps (Yoke Lead)

Device		Description			Typical Luminous Intensity	2θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-6000 Option 021	Red (640 nm)	Subminiature Yoke Lead Configuration	Tinted Diffused	1.2 mcd @ 10 mA	90°	1.6 V @ 10 mA	6-21
	HLMP-6300 Option 021	High Efficiency Red (626 nm)			3.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-6400 Option 021	Yellow (585 nm)					2.2 V @ 10 mA	
	HLMP-6500 Option 021	Green (569 nm)					2.3 V @ 10 mA	
	HLMP-7000 Option 021	Low Current High Efficiency Red (626 nm)			0.8 mcd @ 2 mA	70°	1.8 V @ 2 mA	
	HLMP-7019 Option 021	Low Current Yellow (585 nm)			0.6 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-7040 Option 021	Low Current Green (569 nm)						
	HLMP-6600 Option 021	Integrated Resistor High Efficiency Red (626 nm)			2.4 mcd @ 5 V	80°	9.6 mA @ 5 V	
	HLMP-6620 Option 021				0.6 mcd @ 5 V		3.5 mA @ 5 V	

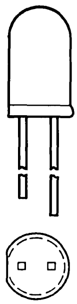
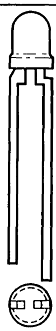
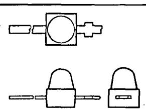
2mm Flat Top Lamps

Device		Description			Typical Luminous Intensity	$2\theta_{1/2}$[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-1800	High Efficiency Red (626 nm)	2mm Flat Top, Round Emitting Surface	Tinted Diffused	1.8 mcd @ 10 mA	140°	2.2 V @ 10 mA	6-25
	HLMP-1801				2.9 mcd @ 10 mA			
	HLMP-1819	Yellow (585 nm)			1.5 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-1820				2.5 mcd @ 10 mA			
	HLMP-1840	Green (569 nm)			2.0 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-1841				3.0 mcd @ 10 mA			
	HLMP-L250	High Efficiency Red (626 nm)	2mm Flat Top, Square Emitting Surface	Tinted Diffused	1.8 mcd @ 10 mA	140°	2.2 V @ 10 mA	
	HLMP-L251				2.9 mcd @ 10 mA			
	HLMP-L350	Yellow (585 nm)			1.5 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-L351				2.5 mcd @ 10 mA			
	HLMP-L550	Green (569 nm)			2.0 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-L551				3.0 mcd @ 10 mA			

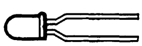
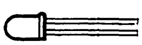
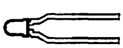
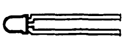
4mm Flat Top Lamps

Device		Description			Typical Luminous Intensity	$2\theta_{1/2}$[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-M200	High Efficiency Red (626 nm)	4mm Flat Top	Tinted Diffused	5.0 mcd @ 20 mA	150°	2.2 V @ 10 mA	6-35
	HLMP-M201				7.0 mcd @ 20 mA			
	HLMP-M250			Tinted Non-Diffused	5.0 mcd @ 10 mA			
	HLMP-M251				7.0 mcd @ 10 mA			
	HLMP-M300	Yellow (585 nm)		Tinted Diffused	5.0 mcd @ 20 mA		2.2 V @ 10 mA	
	HLMP-M301				7.0 mcd @ 20 mA			
	HLMP-M350			Tinted Non-Diffused	5.0 mcd @ 10 mA			
	HLMP-M351				7.0 mcd @ 10 mA			
	HLMP-M500	Green (569 nm)		Tinted Diffused	7.0 mcd @ 20 mA		2.3 V @ 10 mA	
	HLMP-M501				10.0 mcd @ 20 mA			
	HLMP-M550			Tinted Non-Diffused	10.0 mcd @ 10 mA			
	HLMP-M551				16.0 mcd @ 10 mA			

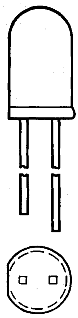
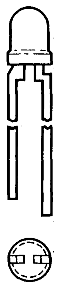
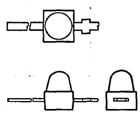
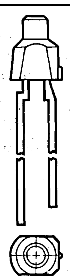
AlGaAs Lamps

Device		Description			Typical Luminous Intensity	2θ1/2[1]	Maximum Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-D100	AlGaAs Red (646 nm)	T-1 3/4	Tinted Diffused	30 mcd @ 20 mA	65°	3.0 V @ 20 mA	6-39
	HLMP-K100		T-1		20 mcd @ 20 mA	60°	3.0 V @ 20 mA	
	HLMP-Q100		Subminiature		5.5 mcd @ 20 mA	70°	3.0 V @ 20 mA	

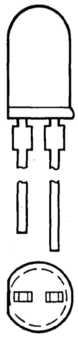
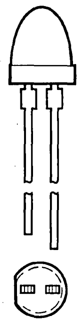
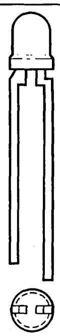
Tape and Reel: Solid State Lamps

Device		Description			Typical Luminous Intensity	2θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3300 Option 001	High Efficiency Red (626 nm)	T-1 3/4	Tinted Diffused	3.5 mcd @ 10 mA	65°	2.2 V @ 10 mA	6-43
	HLMP-3300 Option 002							
	HLMP-1301 Option 001		T-1		2.5 mcd @ 10 mA	60°		
	HLMP-1301 Option 002							

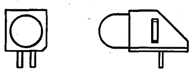
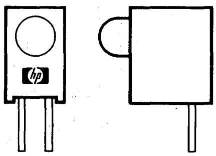
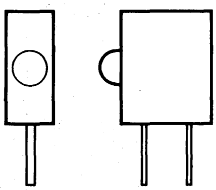
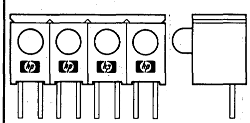
Low Current Lamps

Device		Description			Typical Luminous Intensity	2θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-4700	High Efficiency Red (626 nm)	T-1 3/4	Tinted Diffused	2.0 mcd @ 2 mA	50°	1.8 V @ 2 mA	6-47
	HLMP-4719	Yellow (585 nm)			1.8 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-4740	Green (569 nm)			1.8 mcd @ 2 mA		1.8 V @ 2 mA	
	HLMP-1700	High Efficiency Red (626 nm)	T-1	Tinted Diffused	1.8 mcd @ 2 mA	50°	1.8 V @ 2 mA	
	HLMP-1719	Yellow (585 nm)			1.6 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-1790	Green (569 nm)			1.6 mcd @ 2 mA		1.8 V @ 2 mA	
	HLMP-7000	High Efficiency Red (626 nm)	Subminiature	Tinted Diffused	0.8 mcd @ 2 mA	70°	1.8 V @ 2 mA	
	HLMP-7019	Yellow (585 nm)			0.6 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-7040	Green (569 nm)			0.6 mcd @ 2 mA		1.8 V @ 2 mA	
	HLMP-1740	High Efficiency Red (626 nm)	2 mm Flat Top, Round Emitting Surface	Tinted Diffused	0.5 mcd @ 2 mA	140°	1.8 V @ 2 mA	
	HLMP-1760	Yellow (585 nm)			0.4 mcd @ 2 mA		1.9 V @ 2 mA	

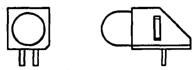
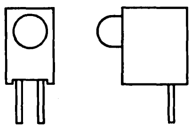
Ultrabright Lamps

Device		Description			Typical Luminous Intensity	$2\theta_{1/2}$[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3750	High Efficiency Red (626 nm)	T-1 3/4	Untinted Non-Diffused	125 mcd @ 20 mA	24°	2.2 V @ 20 mA	6-51
	HLMP-3850	Yellow (585 nm)			140 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-3950	Green (569 nm)			120 mcd @ 20 mA		2.3 V @ 20 mA	
	HLMP-3390	High Efficiency Red (626 nm)	T-1 3/4 Low Profile	Untinted Non-Diffused	55 mcd @ 20 mA	32°	2.2 V @ 20 mA	
	HLMP-3490	Yellow (585 nm)					2.2 V @ 20 mA	
	HLMP-3590	Green (569 nm)					2.3 V @ 20 mA	
	HLMP-1340	High Efficiency Red (626 nm)	T-1 Low Profile	Untinted Non-Diffused	35 mcd @ 20 mA	45°	2.2 V @ 20 mA	
	HLMP-1440	Yellow (585 nm)					2.2 V @ 20 mA	
	HLMP-1540	Green (569 nm)					2.3 V @ 20 mA	

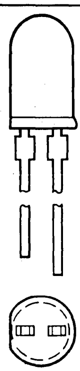
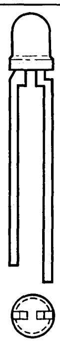
Right Angle Indicators without current limiting resistor

Device		Description			Typical Luminous Intensity	$2\theta_{1/2}$[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-5000	Red (640 nm)	T-1 3/4 Right Angle Indicator	Red Diffused	4.0 mcd @ 20 mA	75°	1.6 V @ 20 mA	6-55
	HLMP-5030	High Efficiency Red (626 nm)			6.0 mcd @ 10 mA	65°	2.2 V @ 10 mA	
	HLMP-5040	Yellow (585 nm)		Yellow Diffused	6.0 mcd @ 10 mA	75°	2.2 V @ 10 mA	
	HLMP-5050	Green (569 nm)		Green Diffused	2.4 mcd @ 10 mA	75°	2.3 V @ 10 mA	
	HLMP-1002 Option 010	Red (640 nm)	T-1 Right Angle Indicator	Red Diffused	2.5 mcd @ 20 mA	125°	1.6 V @ 20 mA	6-57
	HLMP-1301 Option 010	High Efficiency Red (626 nm)			2.5 mcd @ 10 mA	60°	2.2 V @ 10 mA	
	HLMP-1401 Option 010	Yellow (585 nm)		Yellow Diffused	3.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-1503 Option 010	Green (569 nm)		Green Diffused	2.0 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-6000 Option 010	Red (640 nm)	Subminiature Right Angle Indicator	Red Diffused	1.2 mcd @ 10 mA	90°	1.6 V @ 10 mA	6-59
	HLMP-6300 Option 010	High Efficiency Red (626 nm)			3.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-6400 Option 010	Yellow (585 nm)		Yellow Diffused			2.2 V @ 10 mA	
	HLMP-6500 Option 010	Green (569 nm)		Green Diffused			2.3 V @ 10 mA	
	HLMP-1301 Option 104	High Efficiency Red (626 nm)	T-1 Right Angle Indicator 4-Element Array	Tinted Diffused	2.5 mcd @ 10 mA	60°	2.2 V @ 10 mA	6-61
	HLMP-1401 Option 104	Yellow (585 nm)			3.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-1503 Option 104	Green (569 nm)			2.0 mcd @ 10 mA		2.2 V @ 10 mA	

Right Angle Indicators with current limiting resistor

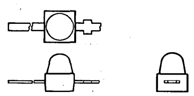
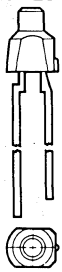
Device		Description			Typical Luminous Intensity	$2\theta 1/2$[1]	Typical Forward Current	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-5012	Red (640 nm)	T-1 3/4 Right Angle Indicator	Red Diffused	2 mcd @ 12V	75°	13 mA @ 12 V	6-55
	HLMP-5005				2 mcd @ 5 V		13 mA @ 5 V	
	HLMP-5060	High Efficiency Red (626 nm)			4 mcd @ 5 V	65°	10 mA @ 5 V	
	HLMP-5070	Yellow (585 nm)		Yellow Diffused		75°	10 mA @ 5 V	
	HLMP-5080	Green (569 nm)		Green Diffused			12 mA @ 5 V	
	HLMP-1100 Option 010	Red (640 nm)	T-1 Right Angle Indicator	Red Diffused	1.5 mcd @ 5 V	60°	13 mA @ 5 V	6-62
	HLMP-1600 Option 010	High Efficiency Red (626 nm)			4 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1620 Option 010	Yellow (585 nm)		Yellow Diffused			10 mA @ 5 V	
	HLMP-1640 Option 010	Green (569 nm)		Green Diffused			12 mA @ 5 V	

Integrated Resistor Lamps

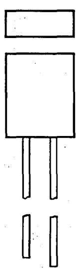
Device		Description			Typical Luminous Intensity	$2\theta 1/2$[1]	Typical Forward Current	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3105	Red (640 nm)	T-1 3/4	Tinted Diffused	2 mcd @ 5 V	75°	13 mA @ 5 V	6-62
	HLMP-3112				2 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3600	High Efficiency Red (626 nm)			4 mcd @ 5 V	65°	10 mA @ 5 V	
	HLMP-3601				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3650	Yellow (585 nm)			4 mcd @ 5 V	75°	10 mA @ 5 V	
	HLMP-3651				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3680	Green (569 nm)			4 mcd @ 5 V		12 mA @ 5 V	
	HLMP-3681				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1100	Red (640 nm)	T-1	Tinted Diffused	1.5 mcd @ 5 V	60°	13 mA @ 5 V	
	HLMP-1120			Untinted Diffused		50°		
	HLMP-1600	High Efficiency Red (626 nm)		Tinted Diffused	4 mcd @ 5 V	60°	10 mA @ 5 V	
	HLMP-1601				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1620	Yellow (585 nm)			4 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1621				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1640	Green (569 nm)			4 mcd @ 5 V		12 mA @ 5 V	
	HLMP-1641				4 mcd @ 12 V		13 mA @ 12 V	

SOLID STATE LAMPS

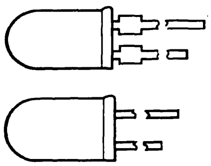
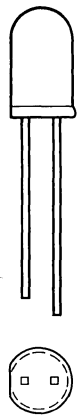
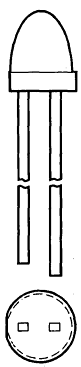
Integrated Resistor Lamps (cont.)

Device		Description			Typical Luminous Intensity	2Θ1/2[1]	Typical Forward Current	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-6600	High Efficiency	Subminiature	Tinted Diffused	5.0 mcd @ 5 V	90°	10 mA @ 5 V	6-66
	HLMP-6620	Red (626 nm)			2.0 mcd @ 5 V		3.5 mA @ 5 V	
	HLMP-6700	Yellow (585 nm)			5.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-6720				2.0 mcd @ 5 V		2.5 mcd @ 5 V	
	HLMP-6800	Green (569 nm)			5.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-6820				2.0 mcd @ 5 V		3.5 mA @ 5 V	
	HLMP-1660	High Efficiency	2mm Flat Top, Round Emitting Surface	Tinted Diffused	1.0 mcd @ 5V	140°	10 mA @ 5V	
	HLMP-1661	Red (626 nm)			1.0 mcd @ 12 V		13 mA @ 5 V	
	HLMP-1674	Yellow (585 nm)			1.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1675				1.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1687	Green (569 nm)			1.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1688				1.0 mcd @ 12 V		13 mA @ 12 V	

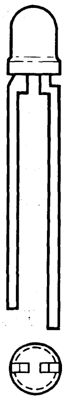
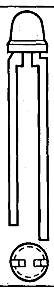
Rectangular Lamps

Device		Description			Typical Luminous Intensity	2Θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-0300	High Efficiency	Rectangular	Tinted Diffused	2.5 mcd @ 20 mA	100°	2.2 V @ 20 mA	6-69
	HLMP-0301	Red (626 nm)			5.0 mcd @ 20 mA			
	HLMP-0400	Yellow (585 nm)			2.5 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-0401				5.0 mcd @ 20 mA			
	HLMP-0503	Green (569 nm)			2.5 mcd @ 20 mA		2.3 V @ 20 mA	
	HLMP-0504				5.0 mcd @ 20 mA			

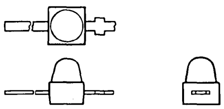
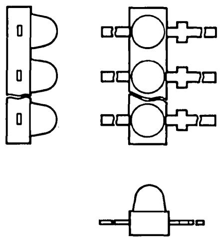
Diffused (Direct View) Lamps

Device		Description			Typical Luminous Intensity	2Θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3000	Red (640 nm)	T-1 3/4	Tinted Diffused	2.0 mcd @ 20 mA	75°	1.6 V @ 20 mA	6-72
	HLMP-3001				4.0 mcd @ 20 mA			
	HLMP-3002		Thin Leadframe		2.0 mcd @ 20 mA			
	HLMP-3003				4.0 mcd @ 20 mA			
	HLMP-3300	High Efficiency Red (626 nm)	T-1 3/4		3.5 mcd @ 10 mA	65°	2.2 V @ 10 mA	6-74
	HLMP-3301				7.0 mcd @ 10 mA			
	HLMP-3762				15.0 mcd @ 10 mA			
	HLMP-D400	Orange (608 nm)			3.5 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-D401				7.0 mcd @ 10 mA			
	HLMP-3400	Yellow (585 nm)			4.0 mcd @ 10 mA	75°	2.2 V @ 10 mA	
	HLMP-3401				8.0 mcd @ 10 mA			
	HLMP-3862				12.0 mcd @ 10 mA			
	HLMP-3502	Green (569 nm)			2.4 mcd @ 10 mA	75°	2.3 V @ 10 mA	
	HLMP-3507				5.2 mcd @ 10 mA			
	HLMP-3962				11.0 mcd @ 10 mA			
	HLMP-D600	Emerald Green (555 nm)			3.0 mcd @ 10 mA			
	HLMP-D601				6.0 mcd @ 10 mA			
	HLMP-3200	Red (640 nm)	T-1 3/4 Low Profile	Tinted Diffused	2.0 mcd @ 20 mA	60°	1.6 V @ 20 mA	6-78
	HLMP-3201				4.0 mcd @ 20 mA			
	HLMP-3350	High Efficiency Red (626 nm)			3.5 mcd @ 10 mA	50°	2.2 V @ 10 mA	
	HLMP-3351				9.0 mcd @ 10 mA			
	HLMP-3450	Yellow (585 nm)			4.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-3451				10.0 mcd @ 10 mA			
	HLMP-3553	Green (569 nm)			3.2 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-3554				10.0 mcd @ 10 mA			

Diffused (Direct View) Lamps (cont.)

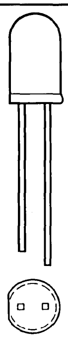
Device		Description			Typical Luminous Intensity	2θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-1000	Red (640 nm)	T-1	Tinted Diffused	1.0 mcd @ 20 mA	125°	1.6 V @ 20 mA	6-84
	HLMP-1002				2.5 mcd @ 20 mA			
	HLMP-1080			Untinted Diffused	1.5 mcd @ 20 mA			
	HLMP-1300	High Efficiency Red (626 nm)		Tinted Diffused	2.0 mcd @ 10 mA	60°	2.2 V @ 10 mA	
	HLMP-1301				2.5 mcd @ 10 mA			
	HLMP-1302				4.0 mcd @ 10 mA			
	HLMP-1385				10.0 mcd @ 10 mA			
	HLMP-K400	Orange (608 nm)			2.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-K401				2.5 mcd @ 10 mA			
	HLMP-K402				4.0 mcd @ 10 mA			
	HLMP-1400	Yellow (585 nm)			2.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-1401				3.0 mcd @ 10 mA			
	HLMP-1402				4.0 mcd @ 10 mA			
	HLMP-1485				10.0 mcd @ 10 mA			
	HLMP-1503	Green (569 nm)			2.0 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-1523				4.0 mcd @ 10 mA			
	HLMP-1585				6.0 mcd @ 10 mA			
	HLMP-K600	Emerald Green (555 nm)			2.0 mcd @ 10 mA			
	HLMP-K601				2.5 mcd @ 10 mA			
	HLMP-1200	Red (640 nm)	T-1 Low Profile	Untinted Non-Diffused	1.0 mcd @ 20 mA	120°	1.6 V @ 20 mA	6-90
	HLMP-1201				2.5 mcd @ 20 mA			
	HLMP-1350	High Efficiency Red (626 nm)		Tinted Diffused	2.0 mcd @ 10 mA	54°	2.2 V @ 10 mA	
	HLMP-1450	Yellow (585 nm)					2.2 V @ 10 mA	
	HLMP-1550	Green (569 nm)					2.3 V @ 10 mA	

Diffused (Direct View) Lamps (cont.)

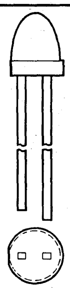
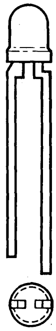
Device		Description				Typical Luminous Intensity	2Θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens	*				
	HLMP-6000	Red (640 nm)	Subminiature	Tinted Diffused		1.2 mcd @ 10 mA	90°	1.6 V @ 10 mA	6-91
	HLMP-6001					3.2 mcd @ 10 mA			
	HLMP-6300	High Efficiency Red (626 nm)				3.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-Q400	Orange (608 nm)							
	HLMP-6400	Yellow (585 nm)						2.2 V @ 10 mA	
	HLMP-6500	Green (569 nm)						2.3 V @ 10 mA	
	HLMP-Q600	Emerald Green (555 nm)							
	HLMP-6203	Red (640 nm)			3	1.2 mcd @ 10 mA		1.6 V @ 10 mA	
	HLMP-6204				4				
	HLMP-6205				5				
	HLMP-6206				6				
	HLMP-6208				8				
	HLMP-6653	High Efficiency Red (626 nm)			3	3.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-6654				4				
	HLMP-6655				5				
	HLMP-6656				6				
	HLMP-6658				8				
	HLMP-6753	Yellow (585 nm)			3			2.2 V @ 10 mA	
	HLMP-6754				4				
	HLMP-6755				5				
	HLMP-6756				6				
	HLMP-6758				8				
	HLMP-6853	Green (569 nm)			3			2.3 V @ 10 mA	
	HLMP-6854				4				
	HLMP-6855				5				
	HLMP-6856				6				
	HLMP-6858				8				

*Array Length

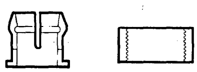
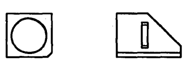
High Intensity Lamps

Device		Description			Typical Luminous Intensity	2Θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3050	Red (640 nm)	T-1 3/4	Tinted Non-Diffused	2.5 mcd @ 20 mA	24°	1.6 V @ 20 mA	6-72
	HLMP-3315	High Efficiency Red (626 nm)			18.0 mcd @ 10 mA	35°	2.2 V @ 10 mA	
	HLMP-3316				30.0 mcd @ 10 mA			
	HLMP-3415	Yellow (585 nm)			18.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-3416				30.0 mcd @ 10 mA			
	HLMP-3517	Green (569 nm)			10.0 mcd @ 10 mA	24°	2.3 V @ 10 mA	
	HLMP-3519				25.0 mcd @ 10 mA			

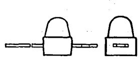
High Intensity Lamps (cont.)

Device		Description			Typical Luminous Intensity	2θ1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3365	High Efficiency Red (626 nm)	T-1 3/4 Low Profile	Tinted Non-Diffused	10.0 mcd @ 10 mA	45°	2.2 V @ 10 mA	6-78
	HLMP-3366				18.0 mcd @ 10 mA			
	HLMP-3465	Yellow (585 nm)			12.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-3466				18.0 mcd @ 10 mA			
	HLMP-3567	Green (569 nm)			7.0 mcd @ 10 mA	40°	2.3 V @ 10 mA	
	HLMP-3568				15.0 mcd @ 10 mA			
	HLMP-1071	Red (640 nm)	T-1	Untinted Non-Diffused	2.0 mcd @ 20 mA	80°	1.6 V @ 20 mA	6-84
	HLMP-1320	High Efficiency Red (626 nm)			12.0 mcd @ 10 mA	45°	2.2 V @ 10 mA	
	HLMP-1321			Tinted Non-Diffused				
	HLMP-1420	Yellow (585 nm)		Untinted Non-Diffused	12.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-1421			Tinted Non-Diffused				
	HLMP-1520	Green (569 nm)		Untinted Non-Diffused	12.0 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-1521			Tinted Diffused				

Mounting Hardware

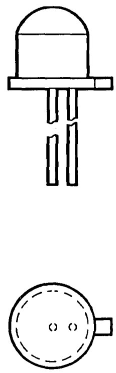
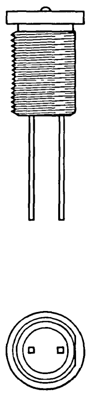
Device			Page No.
Package Outline Drawing	Part No.	Description	
	HLMP-0103	Mounting Clip and Ring for T-1 3/4 Lamps	6-109
	HLMP-5029	Right Angle Housing for T-1 3/4 Lamps	6-110

Emitter Components

Device				Page No.
Package Outline Drawing	Part No.	Description	Features	
	HEMT-6000	700 nm High Intensity Subminiature Emitter	• Visible (Near IR) emmision facilitates alignment. • Compatible with most silicon phototransistors and photodiodes.	6-111

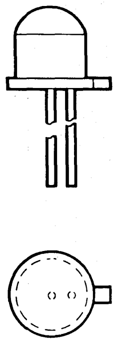
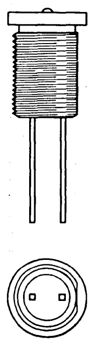
Notes: 1) 2θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2) Dominant wavelength

Hermetically Sealed and High Reliability LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	**Part No.**	**Color[2]**	**Package**	**Lens**				
	1N5765 JAN1N5765[4] JANTX1N5765[4]	Red (640 nm)	Hermetic/ TO-46[3]	Red Diffused	1.0 mcd @ 20 mA	70°	1.6 V @ 20 mA	8-18
	1N6092 JAN1N6092[4] JANTX1N6092[4]	High Efficiency Red (626 nm)			5.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6093 JAN1N6093[4] JANTX1N6093[4]	Yellow (585 nm)		Yellow Diffused				
	1N6094 JAN1N6094[4] JANTX1N6094[4]	Green (572 nm)		Green Diffused	3.0 mcd @ 25 mA		2.1 V @ 25 mA	
	HLMP-0904 HLMP-0930 HLMP-0931	Red (640 nm)	Panel Mount Version	Red Diffused	1.0 mcd @ 20 mA		1.6 V @ 20 mA	
	HLMP-0354 JANM19500/51901 JTXM19500/51902	High Efficiency Red (626 nm)			5.0 mcd @ 20 mA		2.0 V @ 20 mA	
	HLMP-0454 JANM19500/52001 JTXM19500/52002	Yellow (585 nm)		Yellow Diffused				
	HLMP-0554 JANM19500/52101 JTXM19500/52102	Green (572 nm)		Green Diffused	3.0 mcd @ 25 mA		2.1 V @ 25 mA	

NOTES:
1. Θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Dominant Wavelength.
3. PC Board Mountable.
4. Military Approved and qualified for High Reliability Applications.

Hermetically Sealed and High Reliability LED Lamps (cont.)

Device		Description			Typical Luminous Intensity	2Θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-0363 HLMP-0391 HLMP-0392	High Efficiency Red (626 nm)	Hermetic TO-18[3]	Clear Class	50 mcd @ 20 mA	18°	2.0 V @ 20 mA	8-24
	HLMP-0463 HLMP-0491 HLMP-0492	Yellow (585 nm)			50 mcd @ 20 mA		2.0 V @ 20 mA	
	HLMP-0563 HLMP-0591 HLMP-0592	Green (572 nm)			50 mcd @ 25 mA		2.1 V @ 25 mA	
	HLMP-0364 HLMP-0365 HLMP-0366	High Efficiency Red (626 nm)	Panel Mount Version	Clear Glass	50 mcd @ 20 mA		2.0 V @ 20 mA	
	HLMP-0464 HLMP-0465 HLMP-0466	Yellow (585 nm)			50 mcd @ 25 mA		2.0 V @ 20 mA	
	HLMP-0564 HLMP-0565 HLMP-0566	Green (572 nm)			50 mcd @ 25 mA		2.1 V @ 25 mA	

NOTES:
1. Θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Dominant Wavelength.
3. PC Board Mountable.

SURFACE MOUNT OPTION FOR SUBMINIATURE LAMPS — GULL WING LEAD CONFIGURATION

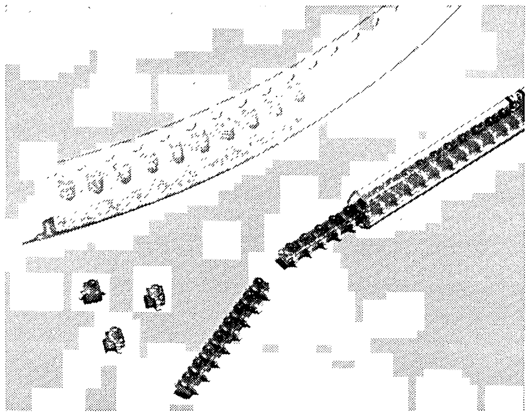
HEWLETT PACKARD

INDIVIDUAL SUBMINIATURE LAMP SUPPLIED IN 12mm TAPE — OPTION 011
SUBMINIATURE ARRAY SUPPLIED IN A SHIPPING TUBE — OPTION 013

TECHNICAL DATA JANUARY 1986

Features

- GULL WING LEAD CONFIGURATION, INDIVIDUAL SUBMINIATURE LAMPS AND ARRAYS
- COMPATIBLE WITH AUTOMATIC PLACEMENT EQUIPMENT
- COMPATIBLE WITH VAPOR PHASE REFLOW SOLDER PROCESSES
- LOW PACKAGE PROFILE
- WIDE VIEWING ANGLE
- LONG LIFE — SOLID STATE RELIABILITY
- INDIVIDUAL SUBMINIATURE LAMPS ARE SUPPLIED IN 12mm TAPE
- SUBMINIATURE ARRAYS ARE SUPPLIED IN TUBES



Description

These subminiature solid state lamps are encapsulated in an axial lead package of molded epoxy. They utilize a tinted, diffused lens providing high on-off contrast and wide angle viewing.

The leads of this device are bent in a gull wing configuration for surface mounting. The device can be mounted using automatic placement equipment.

The individual gull wing subminiature lamp is supplied in 12mm tape on seven inch reels per ANSI/EIA standard RS-481 specifications. Gull wing subminiature arrays are supplied in shipping tubes. The lamp can be mounted with either batch or in line vapor phase reflow solder processes.

Subminiature lamps for surface mount applications are available in standard red, high efficiency red, yellow, green, integrated resistor, and low current versions.

Ordering Information

To obtain gull wing surface mount subminiature lamps, order the basic catalog device with the appropriate option code. Note: Option 011 is available for individual subminiature lamps only. Option 013 is available for subminiature arrays only.

Device Selection Guide

Option	Description
Option 011	Individual subminiature lamps in gull wing configuration. Supplied in 12mm tape on seven inch reels; 1500 pieces per reel. Minimum order quantity and order increment are 1500 pieces.
Option 013	Subminiature array in gull wing configuration. Supplied in shipping tubes.

Examples:

HLMP-6300	HLMP-6658
Option 011	Option 013
High Efficiency Red	High Efficiency Red, 8 Element Array
Supplied on Tape	Supplied in Tubes

SOLID STATE LAMPS

Vapor Phase Reflow Solder Rating

Absolute Maximum Rating

Vapor Phase Soldering Temperature	215°C for 3 minutes Material FC-5311

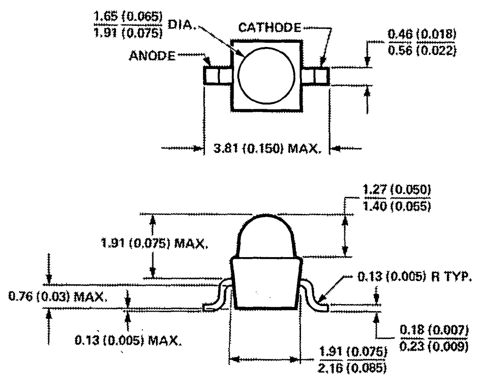
Note: Lead soldering maximum rating is 260°C for 3 seconds.

Absolute Maximum Ratings and Electrical/Optical Characteristics

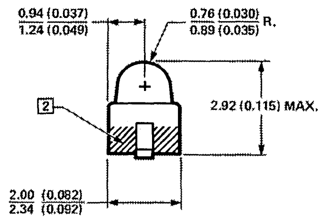
The absolute maximum ratings and electrical/optical specifications are identical to the basic catalog device, except for the vapor phase soldering rating as specified at left.

Package Dimensions

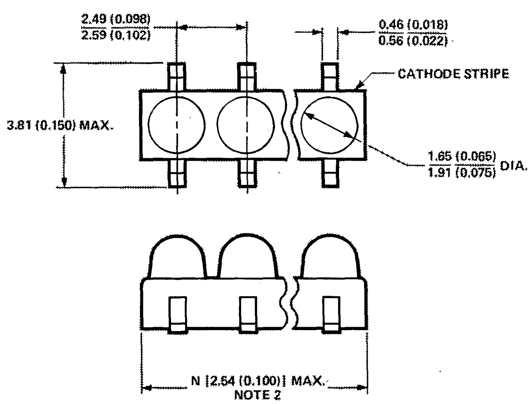
INDIVIDUAL SUBMINIATURE



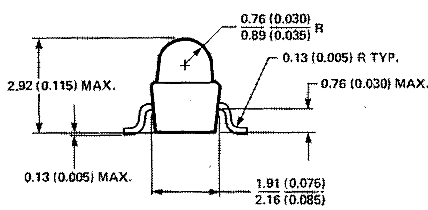
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. CATHODE LEAD IS IDENTIFIED BY THE SILVER STRIPE.



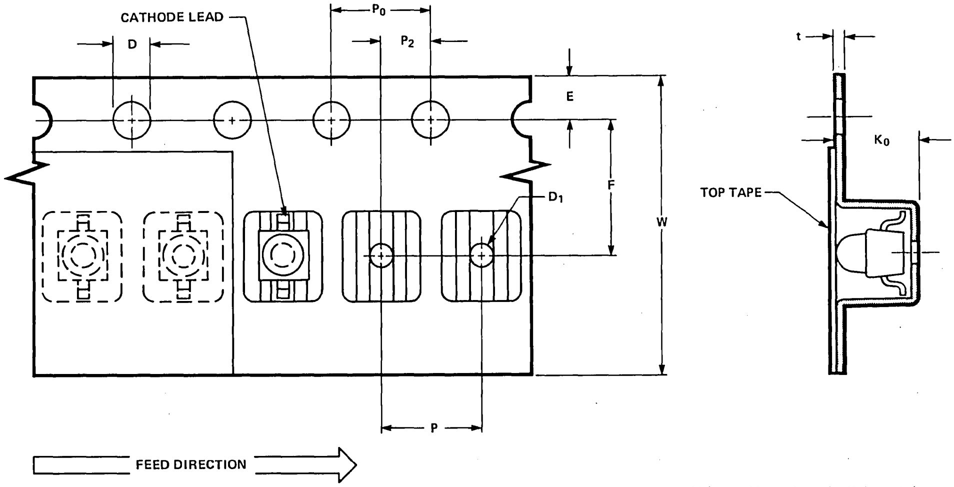
SUBMINIATURE ARRAY



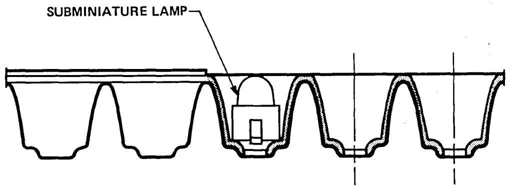
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. OVERALL LENGTH IS THE NUMBER OF ELEMENTS TIMES 2.54mm (0.100 in.).



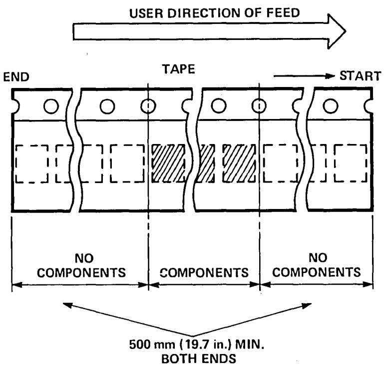
12 mm TAPE AND REEL



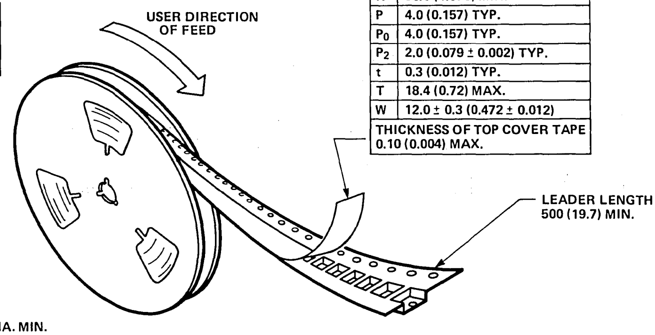
TOLERANCES (UNLESS OTHERWISE SPECIFIED):
.X ± .1; .XX ± .05 (.XXX ± .004)



NOTES:
1. EMPTY COMPONENT POCKETS SEALED WITH TOP COVER TAPE.
2. 7 INCH REEL - 1,500 PIECES PER REEL.
3. MINIMUM LEADER LENGTH AT EITHER END OF THE TAPE IS 500mm.
4. THE MAXIMUM NUMBER OF CONSECUTIVE MISSING LAMPS IS TWO.
5. IN ACCORDANCE WITH ANSI/EIA RS-481 SPECIFICATIONS, THE CATHODE IS ORIENTED TOWARDS THE TAPE SPROCKET HOLE.

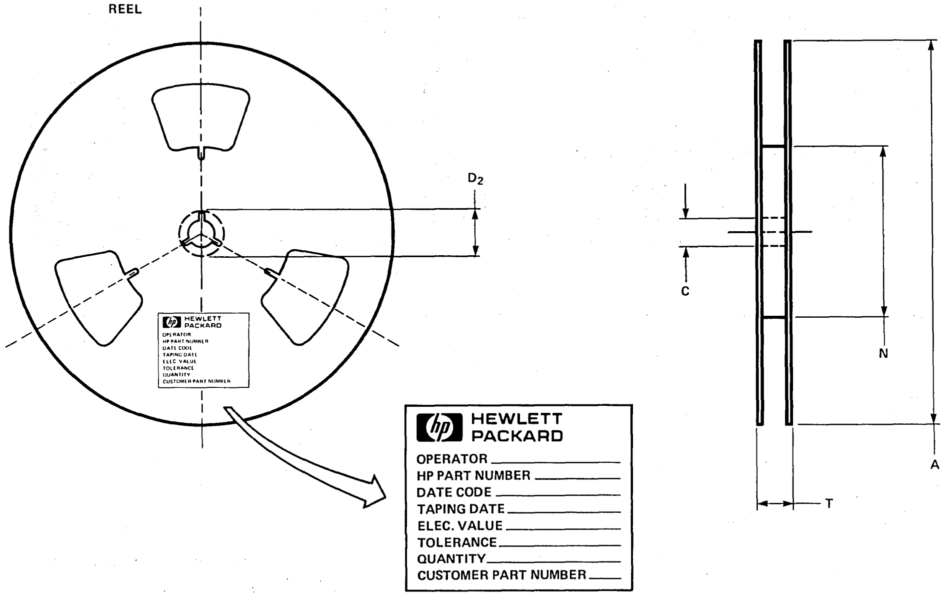


DIMENSIONS PER ANSI/EIA STANDARD RS-481* ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).	
A	178.0 ± 2.0 (7.0 ± 0.08) DIA.
C	13.0 (0.512) DIA. TYP.
D	$1.5\ ^{+0.1}_{-0.0}\left(0.059\ ^{+0.004}_{-0.000}\right)$ DIA.
D_1	1.0 (0.039) DIA. MIN.
D_2	20.2 (0.795) DIA. MIN.
E	1.75 ± 0.1 (0.069)
F	5.50 (0.127 ± 0.002)
K_0	3.05 (0.120) TYP.
N	50.0 (1.970) MIN.
P	4.0 (0.157) TYP.
P_0	4.0 (0.157) TYP.
P_2	2.0 (0.079 ± 0.002) TYP.
t	0.3 (0.012) TYP.
T	18.4 (0.72) MAX.
W	12.0 ± 0.3 (0.472 ± 0.012)
THICKNESS OF TOP COVER TAPE 0.10 (0.004) MAX.	

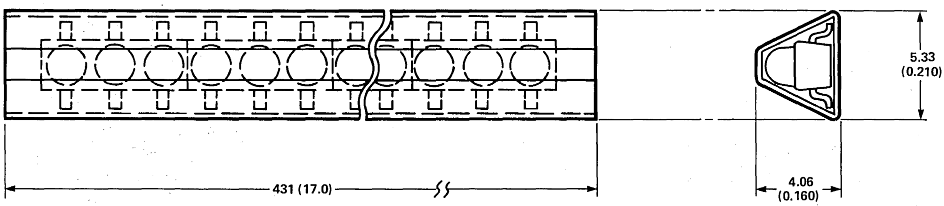


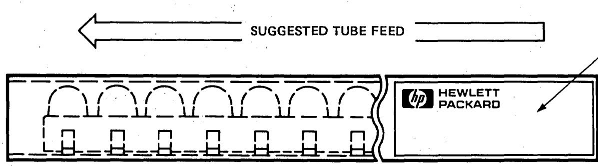
*EXCEPTION: THE EJECTOR-PIN HOLE (D_1) IS 1.0 (0.039) DIA. MIN.

REEL



ARRAY SHIPPING TUBE





TUBE LABEL IDENTIFIES
CATHODE SIDE OF ARRAYS.

HLMP-	NO. OF LAMP ELEMENTS PER ARRAY	QUANTITY OF ARRAYS PER TUBE
6XX3	3	53
6XX4	4	40
6XX5	5	32
6XX6	6	26
6XX8	8	20

HEWLETT PACKARD

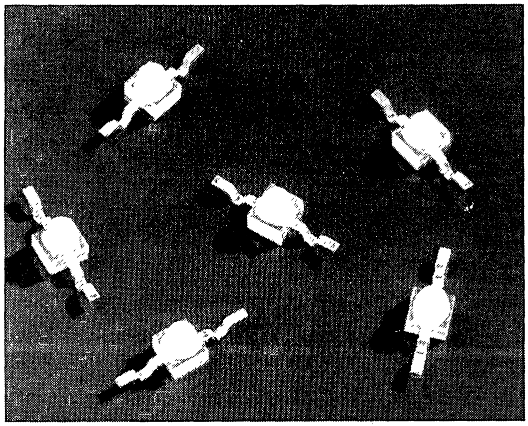
SURFACE MOUNT OPTION FOR SUBMINIATURE LAMPS — "YOKE" LEAD CONFIGURATION

INDIVIDUAL SUBMINIATURE LAMP SUPPLIED IN 12 mm TAPE —OPTION 021
INDIVIDUAL SUBMINIATURE LAMP SUPPLIED IN BULK —OPTION 022

TECHNICAL DATA JANUARY 1986

Features

- **"YOKE" LEAD CONFIGURATION FOR THROUGH HOLE MOUNTING ON PC BOARD**
- **COMPATIBLE WITH AUTOMATIC PLACEMENT EQUIPMENT**
- **COMPATIBLE WITH VAPOR PHASE REFLOW SOLDER PROCESSES**
- **LOW PACKAGE PROFILE**
- **WIDE VIEWING ANGLE**
- **LONG LIFE—SOLID STATE RELIABILITY**
- **SUPPLIED IN 12 mm TAPE OR BULK**



Description

These subminiature solid state lamps are encapsulated in an axial lead package of molded epoxy. The lens is diffused for even light dispersion.

The lamps are designed to be inserted through holes in the PC board to backlight switches, membrane panels, or appliques. Other backlighting applications are equally suitable. As shown in Figure 1, the leads are specially formed to give two features: mechanical strain relief and adequate solder pads.

Automatic placement equipment may be used to mount the LEDs on the PC board if the designer selects the 021 option. These lamps are supplied in 12mm tape on seven inch reels per ANSI/EIA standard RS-481 specifications. Bulk lamps are available under the 022 option code. The lamps can be mounted using either batch or in line vapor phase reflow solder processes.

Subminiature lamps for surface mount applications are available in standard red, high efficiency red, yellow, green, integrated resistor, and low current versions.

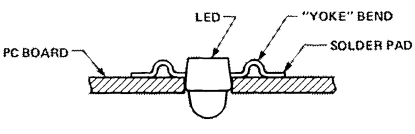


Figure 1.

Ordering Information

To obtain surface mount subminiature lamps with the "yoke" lead configuration, order the basic catalog device with the appropriate option code.

Device Selection Guide

Option	Description
Option 021	Individual subminiature lamps in "yoke" lead configuration. Supplied in 12 mm tape on seven inch reels; 1500 pieces per reel. Minimum order quantity and order increment is 1500 pieces.
Option 022	Individual subminiature lamps in "yoke" lead configuration. Supplied in bulk.

Examples:

HLMP-6300	HLMP-6400
Option 021	Option 022
High Efficiency Red	Yellow
Supplied on Tape	Supplied in Bulk

Vapor Phase Reflow Solder Rating

Absolute Maximum Rating

Vapor Phase Soldering Temperature	215°C for 3 minutes Material FC-5311

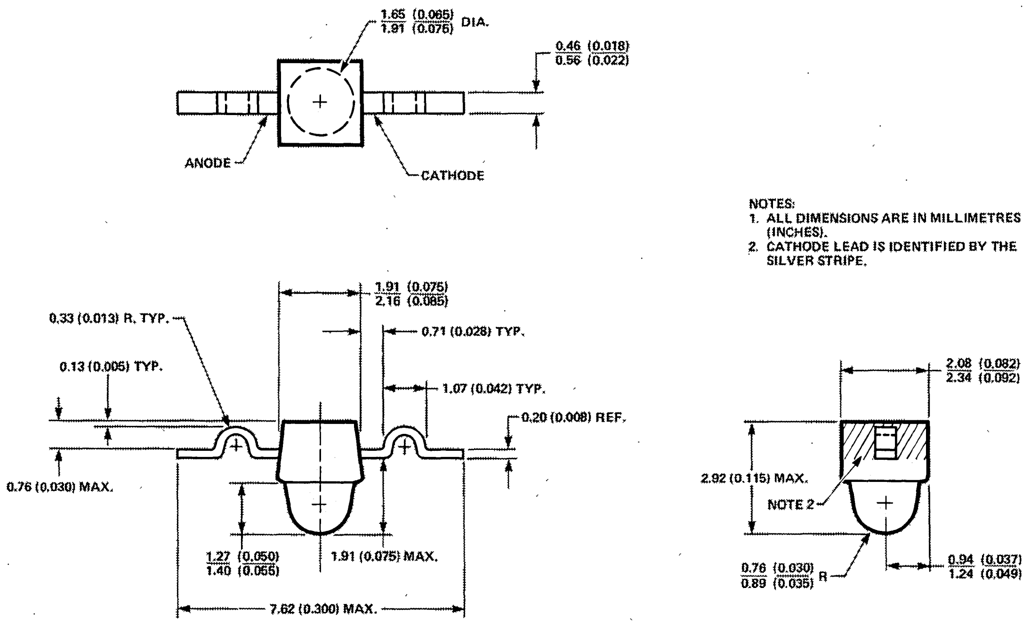
NOTE: Lead soldering maximum rating is 260°C for 3 seconds.

Absolute Maximum Ratings and Electrical/Optical Characteristics

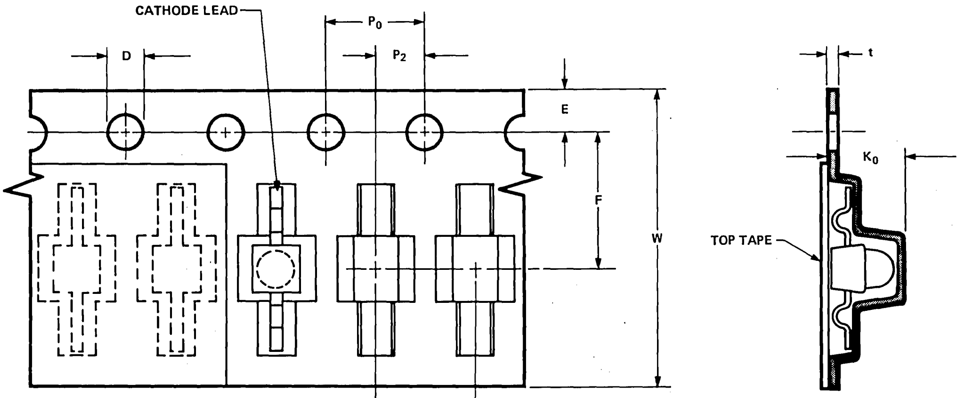
The absolute maximum ratings and electrical/optical specifications are identical to the basic catalog device, except for the vapor phase soldering rating as specified at left.

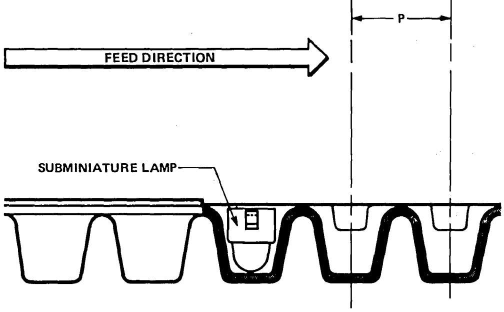
Package Dimensions

INDIVIDUAL SUBMINIATURE LAMP



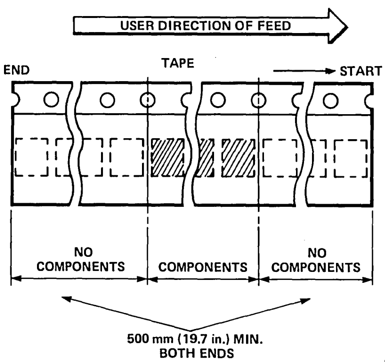
12mm TAPE AND REEL



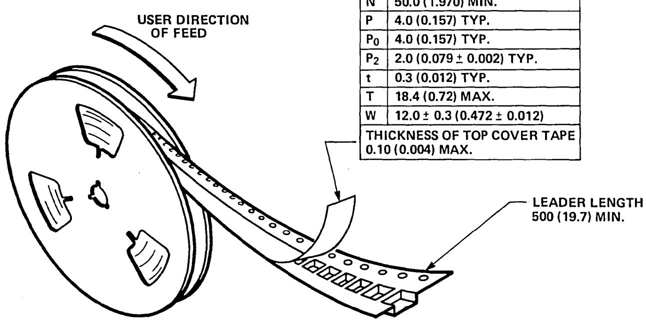


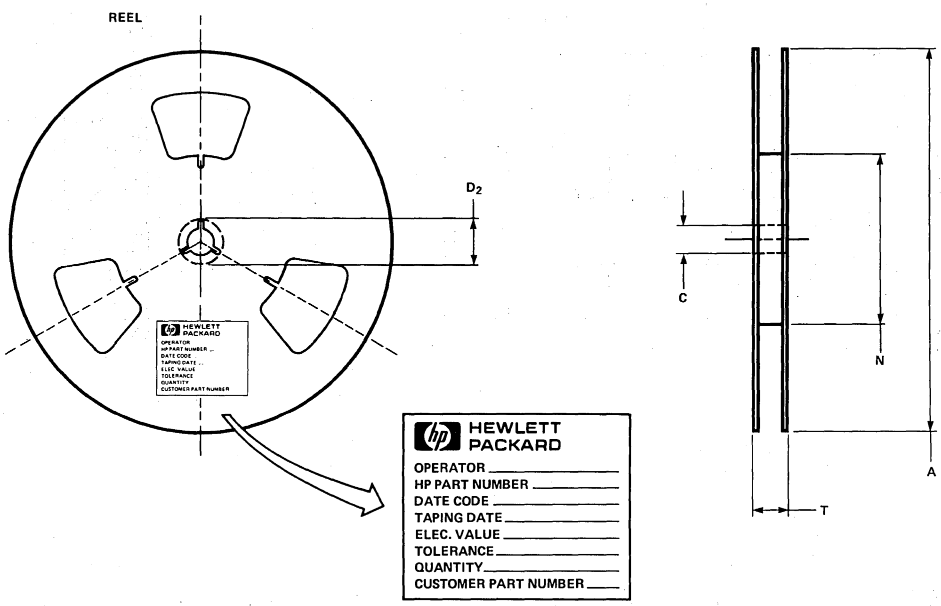
TOLERANCES (UNLESS OTHERWISE SPECIFIED):
.X ± 0.1; .XX ± 0.05 (.XXX ± 0.004)

NOTES:
1. EMPTY COMPONENT POCKETS SEALED WITH TOP COVER TAPE.
2. 7 INCH REEL - 1,500 PIECES PER REEL.
3. MINIMUM LEADER LENGTH AT EITHER END OF THE TAPE IS 500mm.
4. THE MAXIMUM NUMBER OF CONSECUTIVE MISSING LAMPS IS TWO.
5. IN ACCORDANCE WITH ANSI/EIA RS-481 SPECIFICATIONS, THE CATHODE IS ORIENTED TOWARDS THE TAPE SPROCKET HOLE.



DIMENSIONS PER ANSI/EIA STANDARD RS-481 ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).	
A	178.0 ± 2.0 (7.0 ± 0.08) DIA.
C	13.0 (0.512) DIA. TYP.
D	1.55 (0.061 ±0.002) DIA.
D_2	20.2 (0.795) DIA. MIN.
E	1.75 ± 0.1 (0.069)
F	5.50 (0.127 ± 0.002)
K_0	3.05 ± 0.1(0.120) TYP.
N	50.0 (1.970) MIN.
P	4.0 (0.157) TYP.
P_0	4.0 (0.157) TYP.
P_2	2.0 (0.079 ± 0.002) TYP.
t	0.3 (0.012) TYP.
T	18.4 (0.72) MAX.
W	12.0 ± 0.3 (0.472 ± 0.012)
THICKNESS OF TOP COVER TAPE 0.10 (0.004) MAX.	




REEL
D2
C
N
A
T
HEWLETT
PACKARD
OPERATOR
HP PART NUMBER
DATE CODE
TAPING DATE
ELEC. VALUE
TOLERANCE
QUANTITY
CUSTOMER PART NUMBER

HEWLETT PACKARD

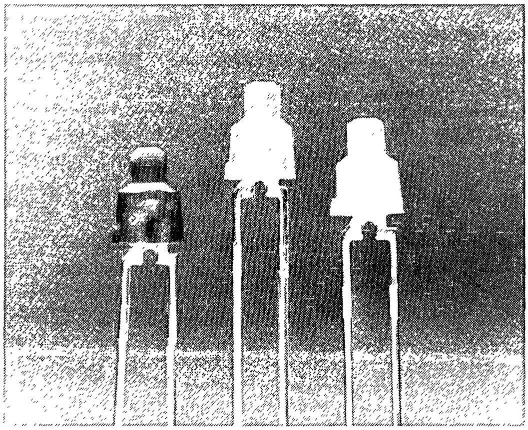
2mm FLAT TOP LED LAMPS

High Efficiency Red, Yellow, Green Lamps
Low Current Lamps
Integrated Resistor Lamps

TECHNICAL DATA JANUARY 1986

Features

- WIDE VIEWING ANGLE
- UNIFORM LIGHT OUTPUT
- MOUNTS FLUSH WITH PANEL
- CHOICE OF THREE BRIGHT COLORS
  - — High Efficiency Red
  - — Yellow
  - — High Performance Green
- LOW CURRENT VERSION AVAILABLE
  - — High Efficiency Red and Yellow
- INTEGRATED RESISTOR VERSION AVAILABLE
  - — Requires no External Current Limiter with 5 V — 12 V Supply



Description

These rugged solid state lamps are designed for applications requiring a bright, compact source of light. Uniform light output, wide viewing angle and flat top make the lamp ideal for flush mounting on a front panel.

The red and yellow devices use Gallium Arsenide Phosphide on Gallium Phosphide light emitting diodes, the green devices use a Gallium Phosphide light emitting diode.

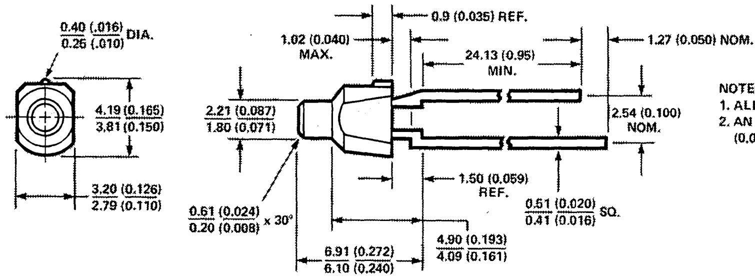
SOLID STATE LAMPS

Axial Luminous Intensity and Viewing Angle

Color	Part Number HLMP-	Description	I_V (mcd) Min.	Typ.	Test Condition	$2\Theta1/2$[1]
High Efficiency Red	-1800	Tinted, Diffused	0.8	1.8	10 mA	140
	-1801	Tinted, Diffused, High Brightness	2.1	2.9	10 mA	
	-1740	Tinted, Diffused, Low Current	0.2	0.5	2 mA	
	-1660	Tinted, Diffused, 5 V Integrated Resistor	0.5		5 V	
	-1661	Tinted, Diffused, 12 V Integrated Resistor	0.5		12 V	
Yellow	-1819	Tinted, Diffused	0.9	1.5	10 mA	140
	-1820	Tinted, Diffused, High Brightness	1.4	2.5	10 mA	
	-1760	Tinted, Diffused, Low Current	0.2	0.4	2 mA	
	-1674	Tinted, Diffused, 5 V Integrated Resistor	0.5		5 V	
	-1675	Tinted, Diffused, 12 V Integrated Resistor	0.5		12 V	
Green	-1840	Tinted, Diffused	1.0	2.0	10 mA	140
	-1841	Tinted, Diffused, High Brightness	1.6	3.0	10 mA	
	-1687	Tinted, Diffused, 5 V Integrated Resistor	0.5		5 V	
	-1688	Tinted, Diffused, 12 V Integrated Resistor	0.5		12 V	

NOTE:
1. $\Theta1/2$ is the off-axis angle at which the luminous intensity is half the axial intensity.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

Absolute Maximum Ratings at $T_A = 25°C$

HIGH EFFICIENCY RED, YELLOW AND GREEN LAMPS

Parameter	High Efficiency Red HLMP-1800/-1801	Yellow HLMP-1819/-1820	Green HLMP-1840/-1841	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	−55 to +100		−20 to +100	°C
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature (1.6 mm [0.063 in.] from body)	260° C for 5 seconds			

NOTES:
1. See Figure 3 to establish pulsed operating conditions.
2. For Red and Green Series derate linearly from 50° C at 0.5 mA/° C. For Yellow Series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green Series derate power linearly from 25° C at 1.8 mW/° C. For Yellow Series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

LOW CURRENT LAMPS

Parameter	High Efficiency Red HLMP-1740	Yellow HLMP-1760	Units
DC and Peak Forward Current[1]	7	7	mA
Transient Forward Current (10 msec Pulse)	500	500	mA
Power Dissipation	27	24	mW
Reverse Voltage (I_R = 50 μA)	5.0		V
Operating and Storage Temperature Range	−55 to +100		°C
Lead Soldering Temperature (1.6 mm [0.063 in.] from body)	260° C for 5 seconds		

NOTES:
1. Derate linearly from 92° C at 1.0 mA/° C.

INTEGRATED RESISTOR LAMPS

Parameter	5 V Lamps HER/Yellow HLMP-1660 HLMP-1674	12 V Lamps HER/Yellow HLMP-1661 HLMP-1675	5 V Lamps Green HLMP-1687	12 V Lamps Green HLMP-1688
Reverse Voltage (I_R = 100 μA)	5 V	5 V	5 V	5 V
DC Forward Voltage (T_A = 25°C)	7.5 V[1]	15 V[2]	7.5 V[1]	15 V[2]
Operating Temperature Range	−40° C to 85° C	−40° C to 85° C	−20° C to 85° C	−20° C to 85° C
Storage Temperature Range	−55° C to 100° C	−55° C to 100° C	−55° C to 100° C	−55° C to 100° C
Lead Soldering Temperature	260° C for 5 seconds			

NOTES:
1. Derate from T_A = 50° C at 0.071 V/° C, see Figure 3.
2. Derate from T_A = 50° C at 0.086 V/° C, see Figure 4.

Electrical/Optical Characteristics at $T_A = 25°C$

COMMON CHARACTERISTICS

Symbol	Parameter	High Efficiency Red			Yellow			Green			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
λ_{PEAK}	Peak Wavelength		635			583			565		nm	
λ_d	Dominant Wavelength		626			585			569		nm	Note 1
η_V	Luminous Efficacy		145			500			595		lumen /watt	Note 2
V_{BR}	Reverse Breakdown Voltage	5.0			5.0			5.0			V	$I_R = 100\ \mu A$

NOTES:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$. Where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

HIGH EFFICIENCY RED, YELLOW AND GREEN LAMPS

Symbol	Parameter	High Efficiency Red HLMP-1800/-1801			Yellow HLMP-1819/-1820			Green HLMP-1840/-1841			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_F	Forward Voltage	1.5	2.2	3.0	1.5	2.2	3.0	1.6	2.3	3.0	V	$I_F = 10$ mA
T_S	Speed of Response		90			90			500		ns	
C	Capacitance		20			15			18		pF	$V_F = 0$, f = 1 MHz
θ_{JC}	Thermal Resistance		95			95			95		°C/W	Junction to Cathode Lead at 0.79 mm (0.031 in.) from body

LOW CURRENT LAMPS

Symbol	Parameter	High Efficiency Red HLMP-1740			Yellow HLMP-1760			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V_F	Forward Voltage		1.8	2.2		1.9	2.7	V	2 mA
T_S	Speed of Response		100			200		ns	
C	Capacitance		4			4		pF	$V_F = 0$, f = 1 MHz
θ_{JC}	Thermal Resistance		190			190		°C/W	Junction to Cathode Lead at 0.79 mm from body

INTEGRATED RESISTOR LAMPS

Symbol	Parameter	5 V HLMP-1660/ -1674/-1687			12 V HLMP-1661/ 1675/-1688			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_F	Forward Current		10	15		13	20	mA	At rated voltage
θ_{JC}	Thermal Resistance		90			90		°C/W	Junction to Lead at 0.79 mm from body

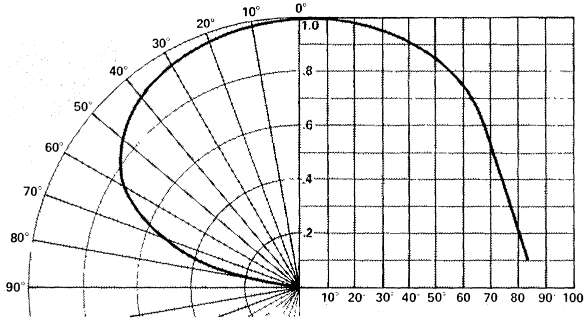


Figure 1. Relative Luminous Intensity vs. Angular Displacement

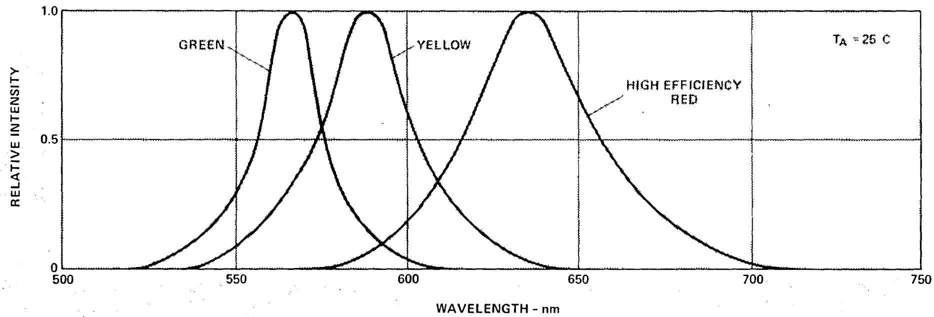


Figure 2. Relative Intensity vs. Wavelength

HIGH EFFICIENCY RED, YELLOW AND GREEN LAMPS

HER HLMP-1800,-1801
Yellow HLMP-1819,-1820
Green HLMP-1840,-1841

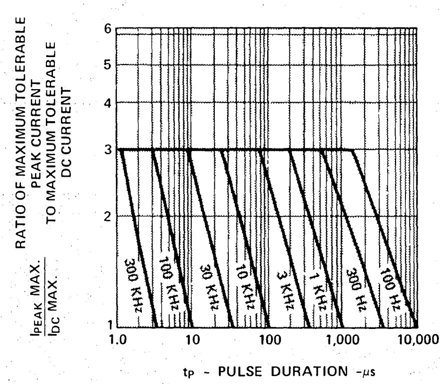


Figure 3. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

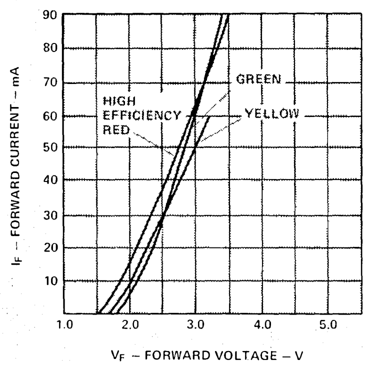


Figure 4. Forward Current vs. Forward Voltage

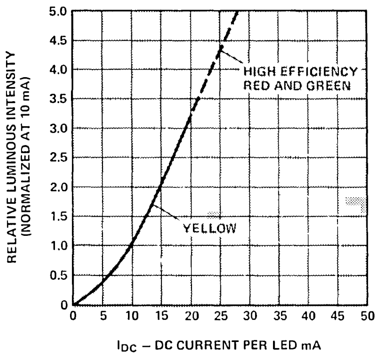


Figure 5. Relative Luminous Intensity vs. Forward Current

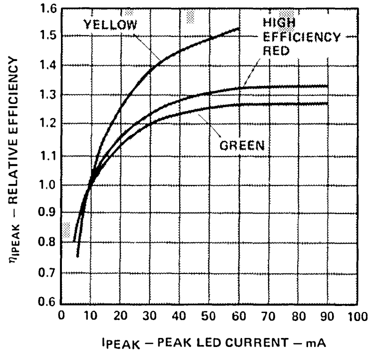


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

LOW CURRENT LAMPS

HER HLMP-1740
Yellow HLMP-1760

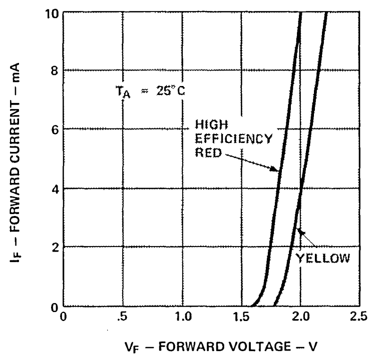


Figure 7. Forward Current vs. Forward Voltage

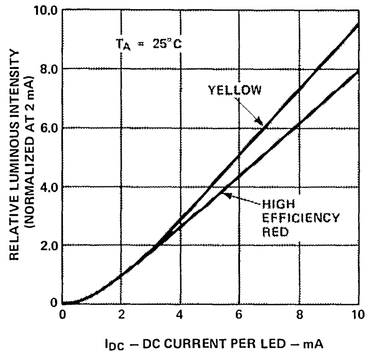


Figure 8. Relative Luminous Intensity vs. Forward Current

INTEGRATED RESISTOR LAMPS

5 Volt HLMP-1660, -1674, 1687
12 Volt HLMP-1661, -1675, -1688

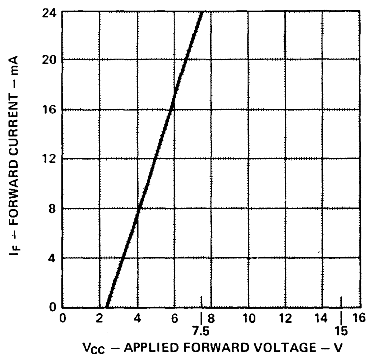


Figure 9. Forward Current vs. Applied Forward Voltage. 5 Volt Devices

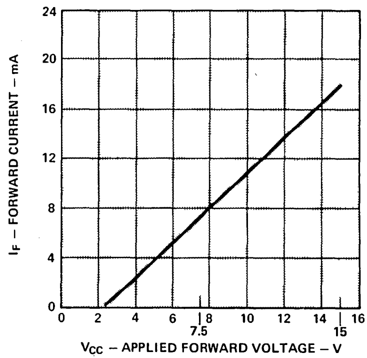


Figure 10. Forward Current vs. Applied Forward Voltage. 12 Volt Devices

SOLID STATE LAMPS

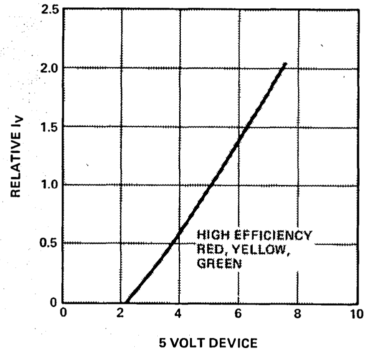


Figure 11. Relative Luminous Intensity vs. Applied Forward Voltage. 5 Volt Devices

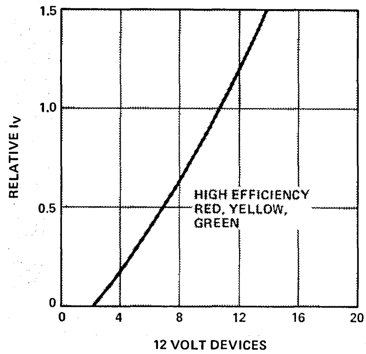


Figure 12. Relative Luminous Intensity vs. Applied Forward Voltage. 12 Volt Devices

HEWLETT PACKARD

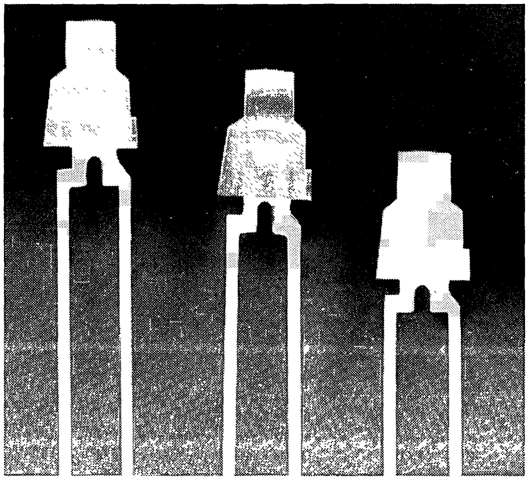
2mm SQUARE FLAT TOP LED LAMPS

High Efficiency Red HLMP-L250, -L251
Yellow HLMP-L350, -L351
Green HLMP-L550, -L551

TECHNICAL DATA JANUARY 1986

Features

- WIDE VIEWING ANGLE
- UNIFORM LIGHT OUTPUT
- SQUARE LIGHT EMITTING AREA
- MOUNTS FLUSH WITH PANEL
- CHOICE OF THREE BRIGHT COLORS
  - — High Efficiency Red
  - — Yellow
  - — High Performance Green



Description

These rugged solid state lamps are designed for applications requiring a bright, compact source of light. Uniform light output, wide viewing angle and flat top make the lamp ideal for flush mounting on a front panel.

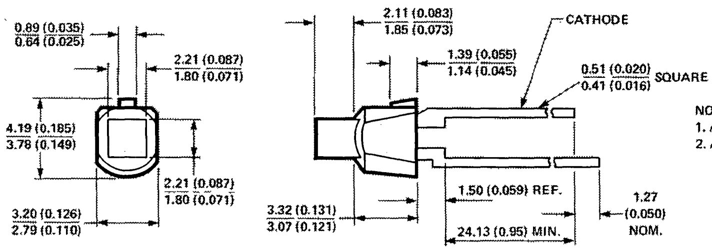
The red and yellow devices use Gallium Arsenide Phosphide on Gallium Phosphide light emitting diodes, the green devices use a Gallium Phosphide light emitting diode.

Axial Luminous Intensity and Viewing Angle

Color	Part Number HLMP-	Description	I_V (mcd) Min.	I_V (mcd) Typ.	Test Condition	$2\Theta 1/2$[1]
High Efficiency Red	-L250	Tinted, Diffused	0.8	1.8	10 mA	140
	-L251	Tinted, Diffused, High Brightness	2.1	2.9	10 mA	
Yellow	-L350	Tinted, Diffused	0.9	1.5	10 mA	140
	-L351	Tinted, Diffused, High Brightness	1.4	2.5	10 mA	
Green	-L550	Tinted, Diffused	1.0	2.0	10 mA	140
	-L551	Tinted, Diffused, High Brightness	1.6	3.0	10 mA	

NOTE:
1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial intensity.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

Electrical/Optical Characteristics at $T_A = 25°C$

COMMON CHARACTERISTICS

Symbol	Parameter	High Efficiency Red L250/L251			Yellow L350/L351			Green L550/L551			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
λ_{PEAK}	Peak Wavelength		635			583			565		nm	
λ_d	Dominant Wavelength		626			585			569		nm	Note 1
η_V	Luminous Efficacy		145			500			595		lumen /watt	Note 2
V_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	$I_R = 100\ \mu A$
V_F	Forward Voltage	1.5	2.2	3.0	1.5	2.2	3.0	1.6	2.3	3.0	V	$I_F = 10$ mA
T_S	Speed of Response		90			90			500		ns	
C	Capacitance		20			15			18		pF	$V_F = 0$, f = 1 MHz
θ_{JC}	Thermal Resistance		120			120			120		°C/W	Junction to Cathode Lead

NOTES:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavlength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$. Where Iv is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

HIGH EFFICIENCY RED, YELLOW AND GREEN LAMPS

Parameter	High Efficiency Red HLMP-L250/-L251	Yellow HLMP-L350/-L351	Green HLMP-L550/-L551	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage ($I_R = 100\ \mu A$)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	−55 to +100		−20 to +100	°C
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature (1.6 mm [0.063 in.] from body)	260° C for 5 seconds			

NOTES:

1. See Figure 3 to establish pulsed operating conditions.
2. For Red and Green Series derate linearly from 50° C at 0.5 mA/° C. For Yellow Series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green Series derate power linearly from 25° C at 1.8 mW/° C. For Yellow Series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

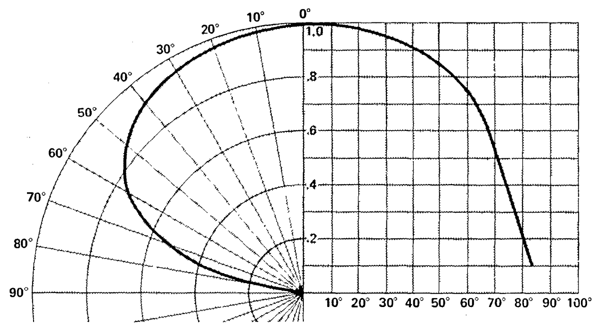


Figure 1. Relative Luminous Intensity vs. Angular Displacement

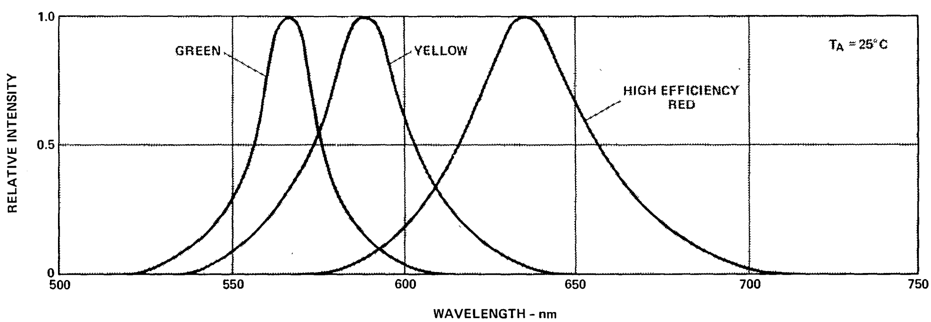


Figure 2. Relative Intensity vs. Wavelength

SOLID STATE LAMPS

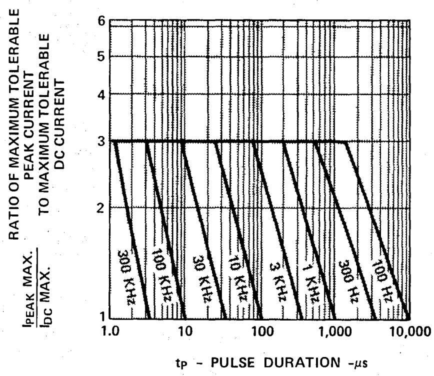


Figure 3. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

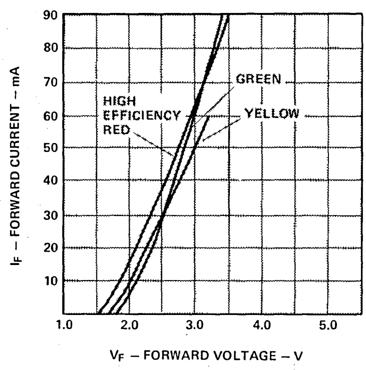


Figure 4. Forward Current vs. Forward Voltage

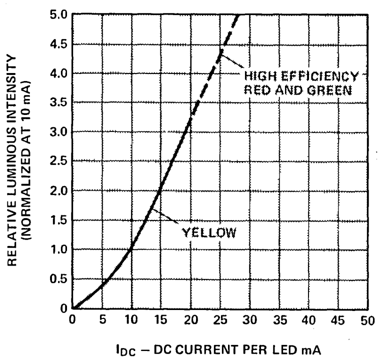


Figure 5. Relative Luminous Intensity vs. Forward Current

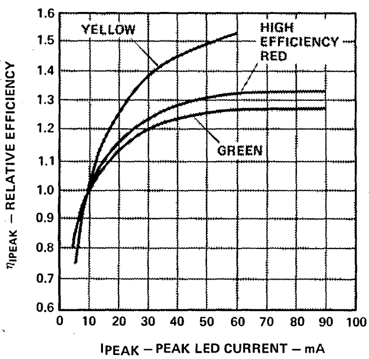


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

HEWLETT PACKARD

4mm FLAT TOP LED LAMPS

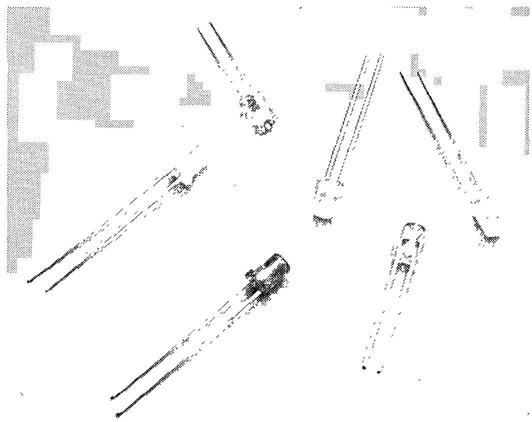
High Efficiency Red, Yellow, Green Lamps

HIGH EFFICIENCY RED HLMP-M200, -M201, -M250, -M251
YELLOW HLMP-M300, -M301, -M350, -M351
GREEN HLMP-M500, -M501, -M550, -M551

TECHNICAL DATA JANUARY 1986

Features

- WIDE VIEWING ANGLE
- FLAT TOP
- DIFFUSED AND NONDIFFUSED PACKAGES
- CHOICE OF BRIGHT COLORS
  - — High Efficiency Red
  - — Yellow
  - — High Performance Green



Description

This line of solid state lamps is designed for applications requiring lamps with a pleasing, flat, light emitting surface in combination with a 4mm cylindrical shape.

The red and yellow devices use Gallium Arsenide Phosphide on Gallium Phosphide light emitting diodes, the green devices use a Gallium Phosphide light emitting diode.

Select diffused or nondiffused lamps based on the radiation pattern or appearance desired. See Figure 1 for detailed radiation pattern differences.

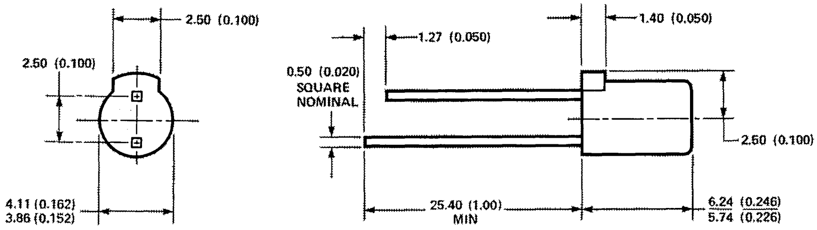
SOLID STATE LAMPS

Axial Luminous Intensity and Viewing Angle

Color (Material)	Part Number HLMP-	Description	I_V (mcd) Min.	I_V (mcd) Typ.	Test Condition (mA)	$2\Theta 1/2$[1]
High Efficiency Red (GaAsP on GaP)	M200	Tinted, Diffused	3.4	5.0	20	135
	M201	Tinted, Diffused, High Brightness	5.4	7.0	20	
	M250	Tinted, Nondiffused	3.4	5.0	10	80
	M251	Tinted, Nondiffused, High Brightness	5.4	7.0	10	
Yellow (GaAsP on GaP)	M300	Tinted, Diffused	3.6	5.0	20	135
	M301	Tinted, Diffused, High Brightness	5.7	7.0	20	
	M350	Tinted, Nondiffused	3.6	5.0	10	80
	M351	Tinted, Nondiffused, High Brightness	5.7	7.0	10	
Green (GaP)	M500	Tinted, Diffused	4.2	7.0	20	135
	M501	Tinted, Diffused, High Brightness	6.7	10.0	20	
	M550	Tinted, Nondiffused	4.2	10.0	10	80
	M551	Tinted, Nondiffused, High Brightness	6.7	16.0	10	

NOTE: 1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial intensity.

Package Dimensions



DIMENSIONS IN MILLIMETERS AND (INCHES)

Electrical/Optical Characteristics at $T_A = 25°C$

COMMON CHARACTERISTICS

Symbol	Parameter	High Efficiency Red HLMP-M2XX			Yellow HLMP-M3XX			Green HLMP-M5XX			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ	Max.	Min.	Typ.	Max.		
λ_{PEAK}	Peak Wavelength		635			583			565		nm	
λ_d	Dominant Wavelength		626			585			569		nm	Note 1
η_v	Luminous Efficacy		142			500			595		lumen /watt	Note 2
V_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	$I_R = 100\ \mu A$
V_F	Forward Voltage	1.5	2.2	3.0	1.5	2.2	3.0	1.6	2.3	3.0	V	$I_V = 10$ mA
T_S	Speed of Response		90			90			500		ns	
C	Capacitance		20			15			18		pF	$V_C = 0.1 = 1$ MHz
θ_{JC}	Thermal Resistance		120			120			120		°C/W	Junction to Cathode Lead

NOTES:

1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$. Where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

HIGH EFFICIENCY RED, YELLOW AND GREEN LAMPS

Parameter	High Efficiency Red HLMP-M2XX	Yellow HLMP-M3XX	Green HLMP-M5XX	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage ($I_R = 100\ \mu A$)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	-55 to +100		-20 to +100	°C
Storage Temperature Range			-55 to +100	
Lead Soldering Temperature (1.6 mm [0.063 in.] from body)	260° C for 5 seconds			

NOTES:

1. See Figure 3 to establish pulsed operating conditions.
2. For Red and Green Series derate linearly from 50° C at 0.5 mA/° C. For Yellow Series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green Series derate power linearly from 25° C at 1.8 mW/° C. For Yellow Series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

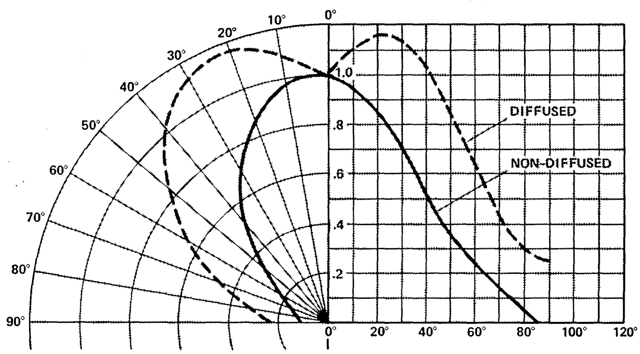


Figure 1. Relative Luminous Intensity vs. Angular Displacement

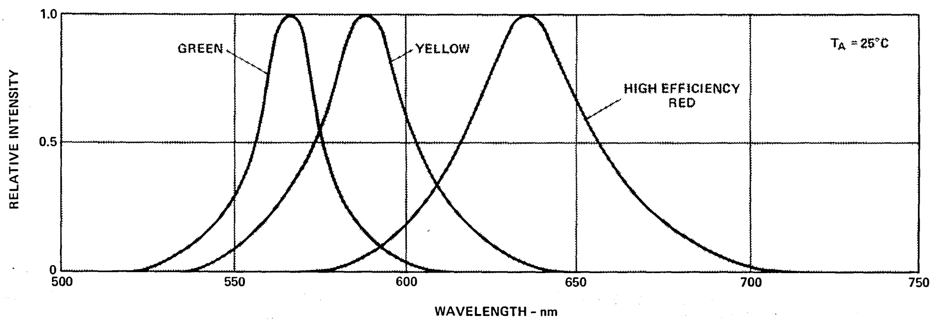


Figure 2. Relative Intensity vs. Wavelength

SOLID STATE LAMPS

HIGH EFFICIENCY RED, YELLOW AND GREEN LAMPS

HER HLMP-M2XX Series
Yellow HLMP-M3XX Series
Green HLMP-M5XX Series

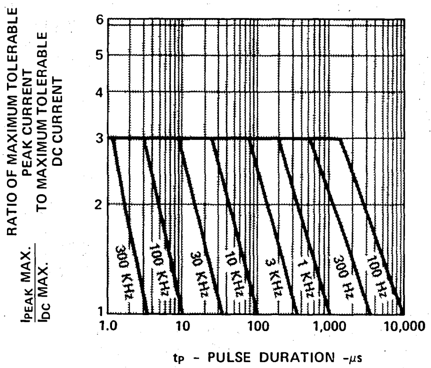


Figure 3. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

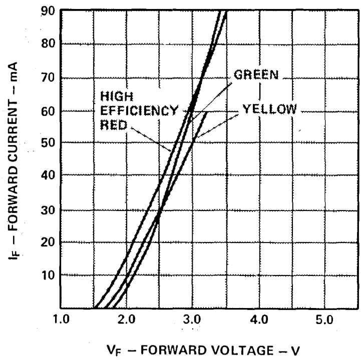


Figure 4. Forward Current vs. Forward Voltage

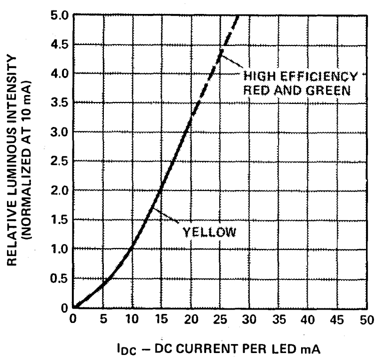


Figure 5. Relative Luminous Intensity vs. Forward Current. Nondiffused Devices.

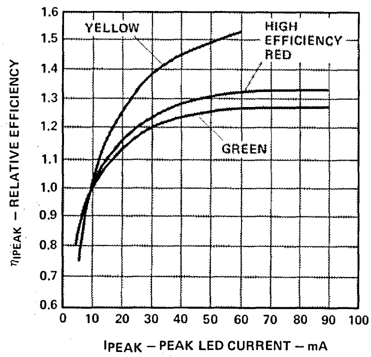


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current. Nondiffused Devices.

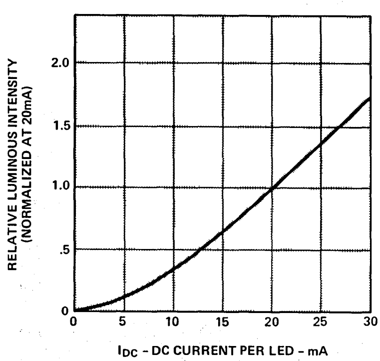


Figure 7. Relative Luminous Intensity vs. Forward Current. Diffused Devices.

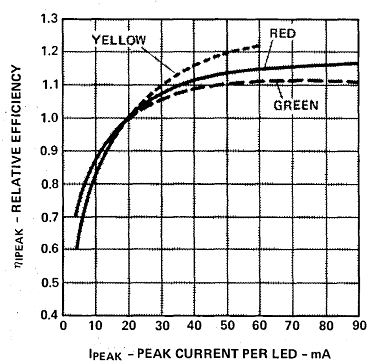


Figure 8. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current. Diffused Devices.

HEWLETT PACKARD

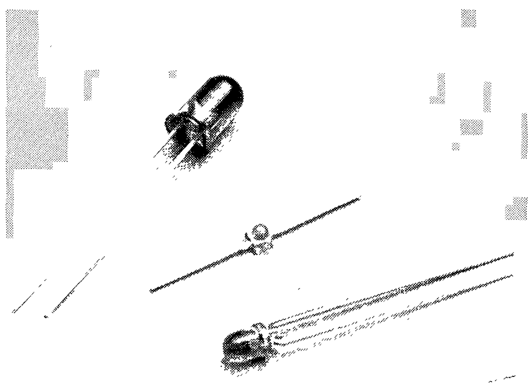
ALUMINUM GALLIUM ARSENIDE (AlGaAs) RED LED LAMPS

T-1 3/4 (5mm)	HLMP-D100
T-1 (3mm)	HLMP-K100
SUBMINIATURE	HLMP-Q100

TECHNICAL DATA JANUARY 1986

Features

- LOW POWER/LOW FORWARD VOLTAGE
- HIGH BRIGHTNESS
- HIGH EFFICIENCY MATERIAL
- CMOS/MOS COMPATIBLE
- TTL COMPATIBLE
- WIDE VIEWING ANGLE
- CHOICE OF PACKAGE STYLES
- DEEP RED COLOR



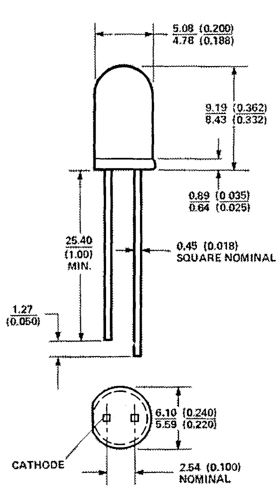
Applications

- LOW POWER CIRCUITS
- TELECOMMUNICATIONS INDICATORS
- PORTABLE EQUIPMENT
- GENERAL USE

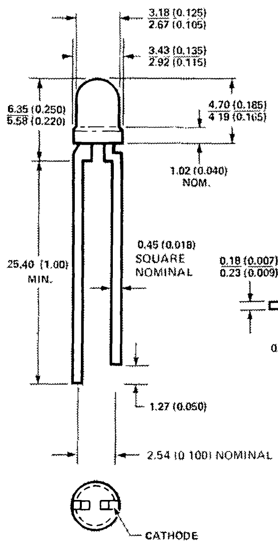
Description

This group of solid state lamps uses Aluminum Gallium Arsenide material to emit deep red light at a dominant wavelength of 646 nm. This material is highly efficient over a wide range of drive current levels, from 2 to 30 mA and can be either DC or pulse driven. This makes these lamps ideal for either low or high current applications.

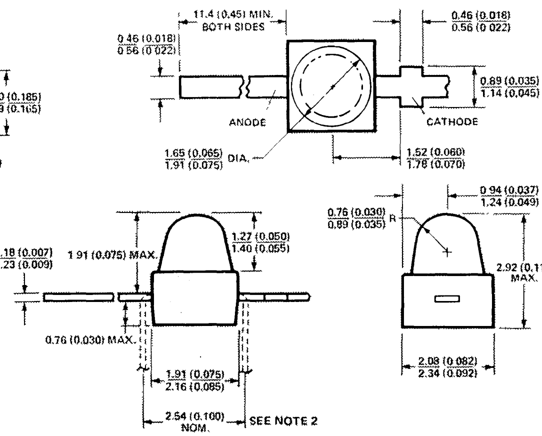
Package Dimensions



A
HLMP-D100



B
HLMP-K100



C
HLMP-Q100

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

AXIAL LUMINOUS INTENSITY AND VIEWING ANGLE @ 25°C

Part Number HLMP-	Package Description	I_V (mcd) @ 20 mA DC		2Θ 1/2[1]	Package Outline
		Min.	Typ.		
D100	T-1 3/4 Red Tinted Diffused	20	30	65°	A
K100	T-1 Red Tinted Diffused	14	20	60°	B
Q100	Subminiature Red Tinted Diffused	3	5.5	70°	C

NOTES:
1. Θ1/2 is the typical off-axis angle at which the luminous intensity is half the axial luminous intensity.

Absolute Maximum Ratings

Parameter		Units
Peak Forward Current	60	mA
Average Forward Current[1]	20	mA
DC Current[2]	20	mA
Power Dissipation[3]	85	mW
Reverse Voltage (I_R = 100μA)	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	mA
Operating Temperature Range	-20 to +100	°C
Storage Temperature Range	-55 to +100	

NOTES:
1. See Figure 7 to establish pulsed operating conditions.
2. Derate linearly from 50° C at 0.2 mA/° C.
3. Derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	Min.	Typ.	Max.	Units	Test Condition
V_F	Forward Voltage			3.0	V	20 mA
V_R	Reverse Breakdown Voltage	5.0			V	I_R = 100 μA
λ_P	Peak Wavelength		662		nm	Measurement at peak
λ_d	Dominant Wavelength		646		nm	Note 1
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		35		nm	
τ_S	Speed of Response		50		ns	
C	Capacitance		40		pF	$V_F = 0$ f = 1 MHz
Θ_{JC}	Thermal Resistance		120		°C/W	Junction to Cathode lead
η_V	Luminous Efficacy		48		$\frac{\text{Lumens}}{\text{Watt}}$	Note 2

NOTES:
1. The dominant wavelength, λ_D, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

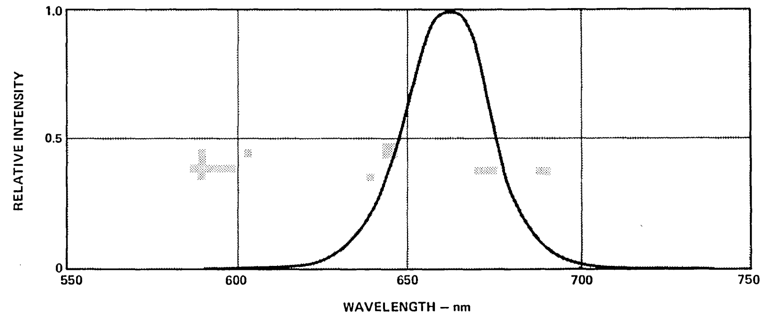


Figure 1. Relative Intensity vs. Wavelength

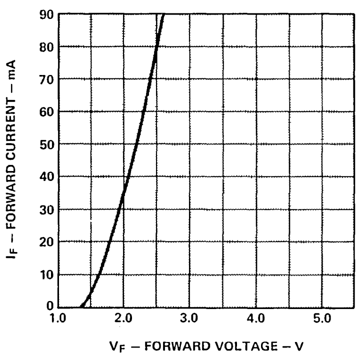


Figure 2. Forward Current vs. Forward Voltage.

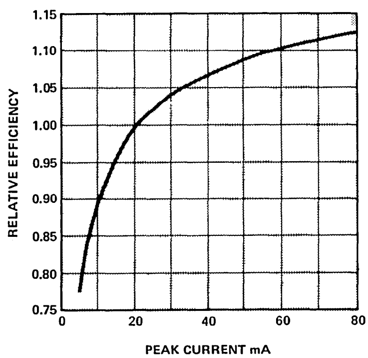


Figure 3. Relative Luminous Intensity vs. Forward Current

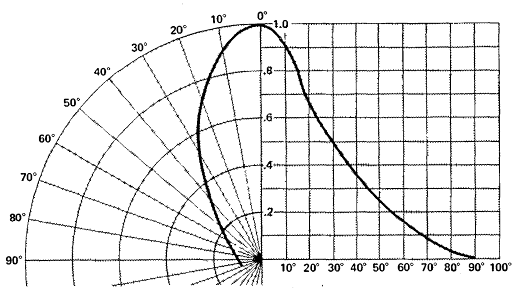


Figure 4. Relative Luminous Intensity vs. Angular Displacement for T-1 3/4 Lamp

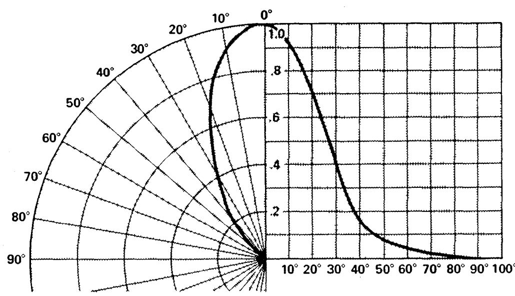


Figure 5. Relative Luminous Intensity vs. Angular Displacement for T-1 Lamp

SOLID STATE LAMPS

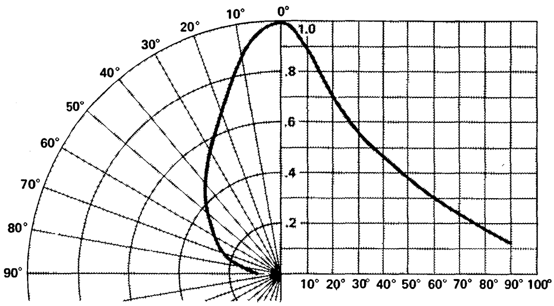


Figure 6. Relative Luminous Intensity vs. Angular Displacement for Subminiature Lamp

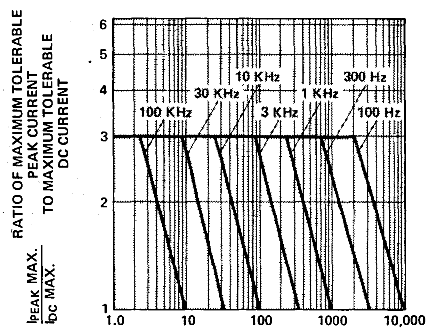


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

HEWLETT PACKARD

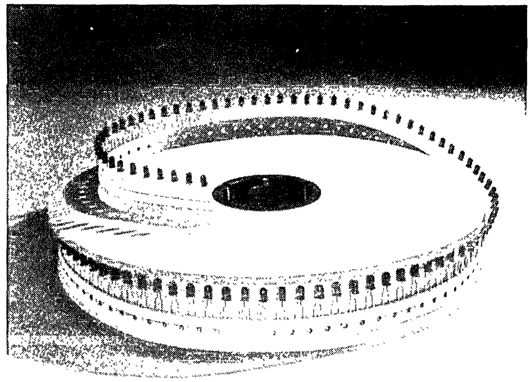
TAPE AND REEL SOLID STATE LAMPS

Leads: 5mm (0.197 inch) Formed Leads — OPTION 001
2.54mm (0.100 inch) Straight Leads — OPTION 002

TECHNICAL DATA JANUARY 1986

Features

- COMPATIBLE WITH RADIAL LEAD AUTOMATIC INSERTION EQUIPMENT
- MEETS DIMENSIONAL SPECIFICATIONS OF IEC PUBLICATION 286 AND ANSI/EIA STANDARD RS-468 FOR TAPE AND REEL
- REEL PACKAGING SIMPLIFIES HANDLING AND TESTING
- T-1 AND T-1 3/4 LED LAMPS AVAILABLE PACKAGED ON TAPE AND REEL
- 5 mm (0.197 INCH) FORMED LEAD AND 2.54 mm (0.100 INCH) STRAIGHT LEAD SPACING AVAILABLE



Description

T-1 and T-1 3/4 LED lamps are available on tape and reel as specified by the IEC Publication 286 and ANSI/EIA Standard RS-468. The Option 001 lamp devices have formed leads with 5 mm (0.197 inch) spacing for automatic insertion into PC boards by radial lead insertion equipment. The Option 002 lamp devices have straight leads with 2.54 mm (0.100 inch) spacing, packaged on tape and reel for ease of handling. T-1 lamps are packaged 1800/reel. T-1 3/4 lamps are packaged 1300/reel.

Ordering Information

To order LED lamps packaged on tape and reel, include the appropriate option code along with the device catalog part number. Example: to order the HLMP-3300 on tape and reel with formed leads (5 mm lead spacing) order as follows: HLMP-3300 Option 001. Minimum order quantities vary by part number. Orders must be placed in reel increments. Please contact your local Hewlett-Packard sales office or franchised Hewlett-Packard distributor for a complete list of lamps available on tape and reel.

LED lamps with 0.46 mm (0.018 inch) square leads with 5 mm (0.197 inch) lead spacing are recommended for use with automatic insertion equipment. It is suggested that insertion machine compatibility be confirmed.

Device Selection Guide

Option	Description
001	Tape and reel, 5 mm (0.197 inch) formed leads.
002	Tape and reel, 2.54 mm (0.100 inch) straight leads.

Package	Quantity/Reel	Order Increments
T-1	1800	1800
T-1 3/4	1300	1300

Absolute Maximum Ratings and Electrical/Optical Characteristics

The absolute maximum ratings, mechanical dimension tolerances and electrical/optical characteristics for lamps packaged on tape and reel are identical to the basic catalog device. Refer to the basic data sheet for the specified values.

Notes:
1. Minimum leader length at either end of tape is 3 blank part spaces.
2. Silver saver paper is used as the interlayer for silver plated lead devices.
3. The maximum number of consecutive missing lamps is 3.
4. In accordance with EIA and IEC specs, the anode lead leaves the reel first.
5. Drawings apply to devices with 0.46 mm (0.018 inch) square leads only. Contact Hewlett-Packard Sales Office for dimensions of 0.635 mm (0.025 inch) square lead devices.

Tape and Reel LED Configurations

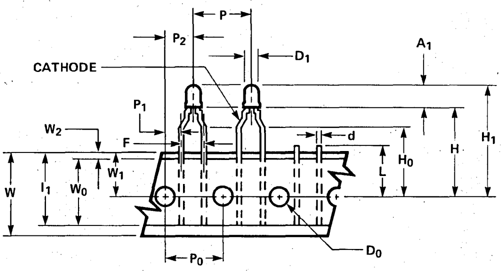


Figure 1. T-1 High Profile Lamps, Option 001

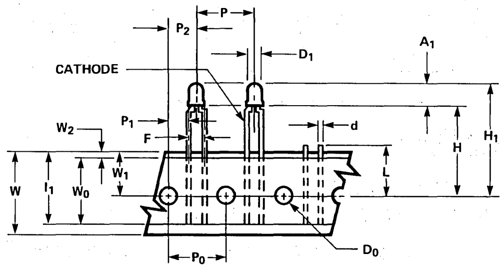


Figure 2. T-1 High Profile Lamps, Option 002

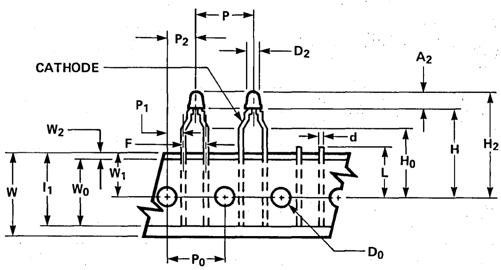


Figure 3. T-1 Low Profile Lamps, Option 001

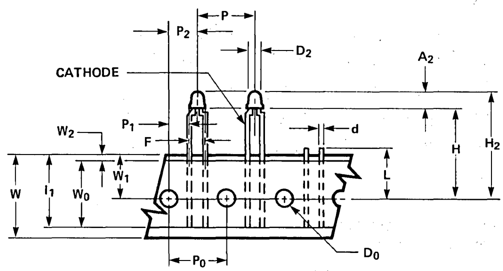


Figure 4. T-1 Low Profile Lamps, Option 002

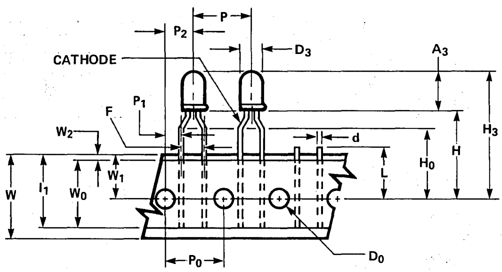


Figure 5. T-1 3/4 High Profile Lamps, Option 001

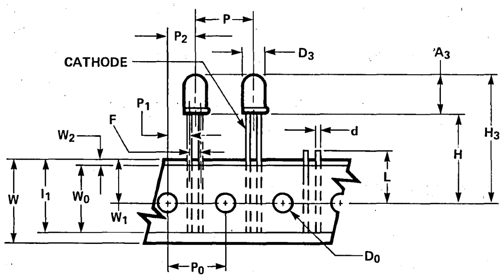


Figure 6. T-1 3/4 High Profile Lamps, Option 002

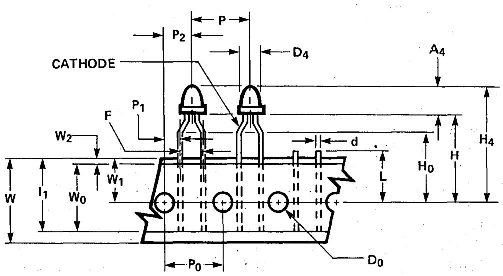


Figure 7. T-1 3/4 Low Profile Lamps, Option 001

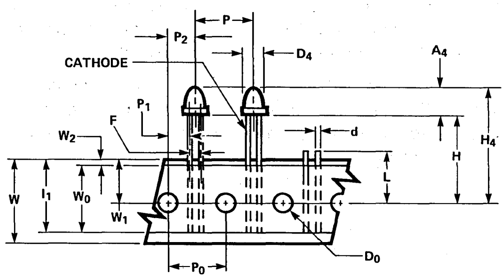
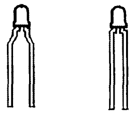
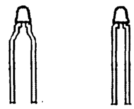
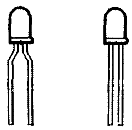
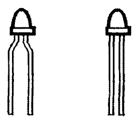


Figure 8. T-1 3/4 Low Profile Lamps, Option 002

Dimensional Specifications for Tape and Reel

Item Option 001 002	Symbol	Specification	Notes
T1 High Profile Body Height 	A1	4.70 (0.185) / 4.19 (0.165)	
Body Diameter	D1	3.18 (0.125) / 2.67 (0.105)	
Component Height	H1	25.7 (1.012) Max.	
T1 Low Profile Body Height 	A2	3.73 (0.147) / 3.23 (0.127)	
Body Diameter	D2	3.05 (0.120) / 2.79 (0.110)	
Component Height	H2	24.7 (0.974) Max.	
T1-3/4 High Profile Body Height 	A3	9.19 (0.362) / 8.43 (0.332)	
Body Diameter	D3	5.08 (0.200) / 4.32 (0.170)	
Component Height	H3	30.2 (1.189) Max.	
T1-3/4 Low Profile Body Height 	A4	6.35 (0.250) / 5.33 (0.210)	
Body Diameter	D4	5.08 (0.200) / 4.32 (0.170)	
Component Height	H4	27.4 (1.079) Max.	
Lead wire thickness	d	0.45 (0.018)	Square Leads
Pitch of component	P	13.7 (0.539) / 11.7 (0.461)	
Feed hole pitch	Po	12.9 (0.508) / 12.5 (0.492)	Cumulative error: 1.0 mm/20 pitches.
Feed hole center to lead center	P1	4.55 (0.179) / 3.15 (0.124)	Measure at crimp bottom. 5.78/3.68 (0.227/0.1448) for straight leads
Hole center to component center	P2	7.35 (0.289) / 5.35 (0.211)	
Lead to lead distance	F	5.40 (0.213) / 4.90 (0.193)	2.54 (0.100) nominal for straight leads.
Component alignment, front-rear	Δh	0 ± 1.0 (0.039)	Figure 9
Tape width	W	18.5 (0.728) / 17.5 (0.689)	
Hold down tape width	Wo	15.3 (0.602) / 14.7 (0.579)	
Hole position	W1	9.75 (0.384) / 8.50 (0.335)	
Hold down tape position	W2	0.5 (0.020) Max.	
Height of component from hole center	H	21.0 (0.827) / 20.0 (0.787)	
Lead clinch height	Ho	16.5 (0.650) / 15.5 (0.610)	
Feed hole diameter	Do	4.20 (0.165) / 3.80 (0.150)	
Total tape thickness	t	0.90 (0.035) / 0.50 (0.020)	Paper thickness: 0.55 (0.022) / 0.45 (0.018) Figure 9
Length of snipped lead	L	11.0 (0.433) Max.	
Lead length under hold down tape	l1	14.5 (0.571) Min.	

Note:

1. Dimensions in millimetres (inches), maximum/minimum.

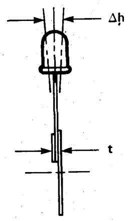
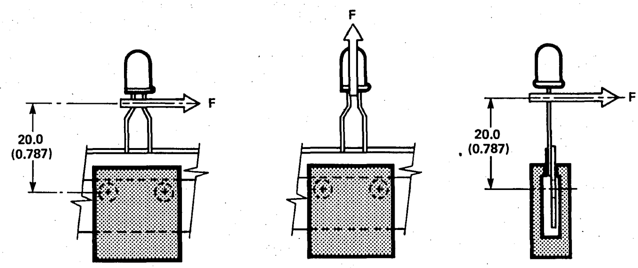


Figure 9. Front to Rear Alignment and Tape Thickness, Typical All Device Types



F = 100g MIN. APPLIED FOR 3 ± 1 SEC.

F = 500g MIN. APPLIED FOR 3 ± 1 SEC.

F = 70g MIN. APPLIED FOR 3 ± 1 SEC.

Figure 10. Device Retention Tests and Specifications

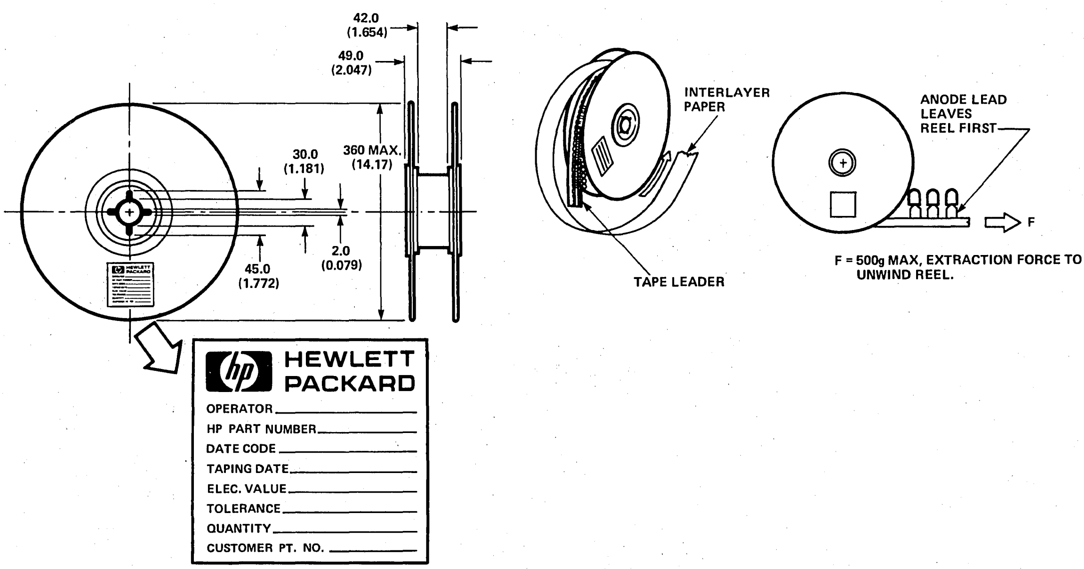


Figure 11. Reel Configuration and Labeling

HEWLETT PACKARD

LOW CURRENT LED LAMP SERIES

T-1 3/4 (5mm) HLMP-4700, -4719, -4740
T-1 (3mm) HLMP-1700, -1719, -1790
SUBMINIATURE HLMP-7000, -7019, -7040

TECHNICAL DATA JANUARY 1986

Features

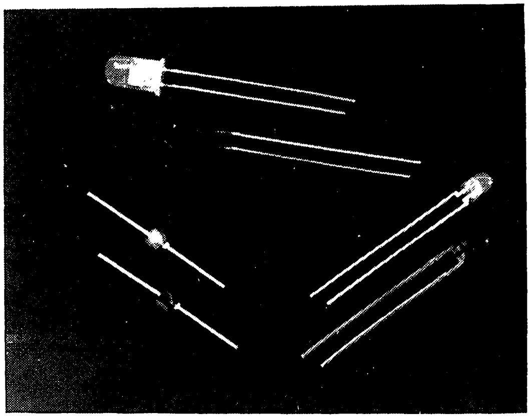
- LOW POWER
- HIGH EFFICIENCY
- CMOS/MOS COMPATIBLE
- TTL COMPATIBLE
- WIDE VIEWING ANGLE
- CHOICE OF PACKAGE STYLES
- CHOICE OF COLORS

Applications

- LOW POWER DC CIRCUITS
- TELECOMMUNICATIONS INDICATORS
- PORTABLE EQUIPMENT
- KEYBOARD INDICATORS

Description

These tinted diffused LED lamps were designed and optimized specifically for low DC current operation. Luminous intensity and forward voltage are tested at 2 mA to assure consistent brightness at TTL output current levels.

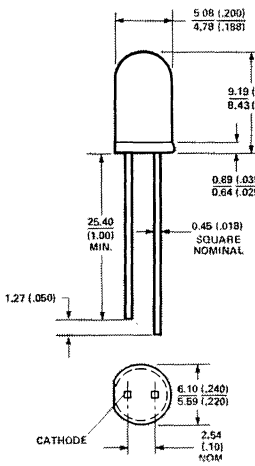


LOW CURRENT LAMP SELECTION GUIDE

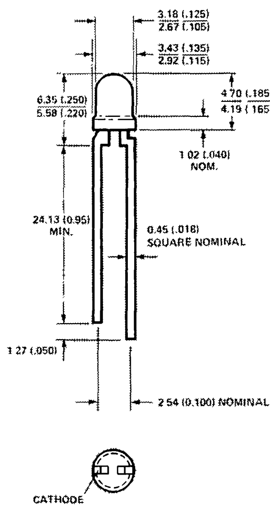
Size	Color		
	Red HLMP-	Yellow HLMP-	Green HLMP-
T-1 3/4	4700	4719	4740
T-1	1700	1719	1790
Subminiature	7000	7019	7040

SOLID STATE LAMPS

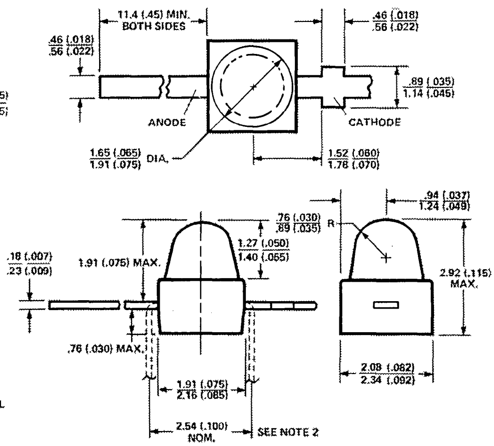
Package Dimensions



HLMP-4700, -4719, -4740



HLMP-1700, -1719, -1790



HLMP-7000, -7019, -7040

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

AXIAL LUMINOUS INTENSITY AND VIEWING ANGLE @ 25°C

Part Number HLMP-	Package Description	Color	I_V (mcd) @ 2 mA DC Min.	Typ.	2Θ 1/2[1]	Package Outline
-4700 -4719 -4740	T-1 3/4 Tinted Diffused	Red Yellow Green	1.2 1.2 1.2	2.0 1.8 1.8	50°	A
-1700 -1719 -1790	T-1 Tinted Diffused	Red Yellow Green	1.0 1.0 1.0	1.8 1.6 1.6	50°	B
-7000 -7019 -7040	Subminiature Tinted Diffused	Red Yellow Green	0.4 0.4 0.4	0.8 0.6 0.6	70°	C

Notes:
1. Θ1/2 is the typical off-axis angle at which the luminous intensity is half the axial luminous intensity.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	T-1 3/4	T-1	Subminiature	Min.	Typ.	Max.	Units	Test Condition
V_F	Forward Voltage	4700 4719 4740	1700 1719 1790	7000 7019 7040		1.8 1.9 1.8	2.2 2.7 2.2	V	2 mA
V_R	Reverse Breakdown Voltage	4700 4719 4740	1700 1719 1790	7000 7019 7040	5.0 5.0 5.0	30 40 30		V	$I_R = 50\ \mu A$
λ_D	Dominant Wavelength	4700 4719 4740	1700 1719 1790	7000 7019 7040		629 585 569		nm	Note 1
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	4700 4719 4740	1700 1719 1790	7000 7019 7040		40 35 28		nm	
τ_S	Speed of Response	4700 4719 4740	1700 1719 1790	7000 7019 7040		100 200 500		ns	
C	Capacitance	4700 4719 4740	1700 1719 1790	7000 7019 7040		4 4 18		pF	$V_F = 0$ f = 1 MHz
Θ_{JC}	Thermal Resistance	4700 4719 4740	1700 1719 1790	7000 7019 7040		135 120 120		°C/W	Junction to Cathode lead
λ_P	Peak Wavelength	4700 4719 4740	1700 1719 1790	7000 7019 7040		635 583 565		nm	Measurement at peak
η_V	Luminous Efficacy	4700 4719 4740	1700 1719 1790	7000 7019 7040		145 500 595		$\frac{\text{Lumens}}{\text{Watt}}$	Note 2

Notes:
1. The dominant wavelength, λ_D, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings

Parameter	Maximum Rating		Units
Power Dissipation (Derate linearly from 92°C at 1.0 mA/°C)	Red Yellow Green	24 36 24	mW
DC and Peak Forward Current	7		mA
Transient Forward Current (10 μsec pulse)[1]	500		mA
Reverse Voltage (I_R = 50 μA)	5.0		V
Operating and Storage Temperature Range	-55°C to 100°C		
Lead Soldering Temperature (1.6 mm [0.063 in] from body)	260°C for 5 Seconds (T-1, T-1 3/4) 260°C for 3 Seconds (Subminiature)		

Notes:

1. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

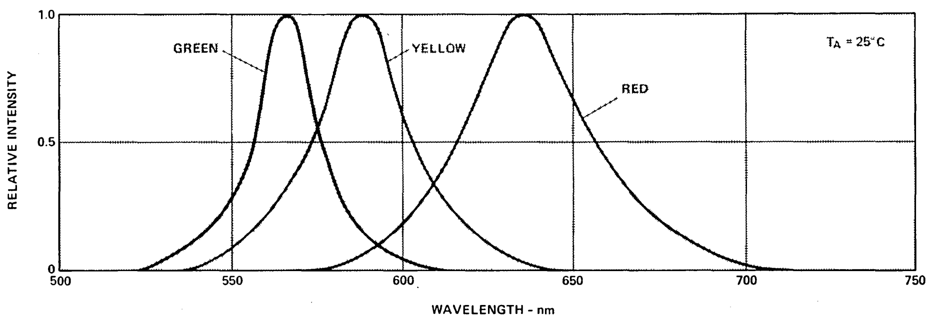


Figure 1. Relative Intensity vs. Wavelength

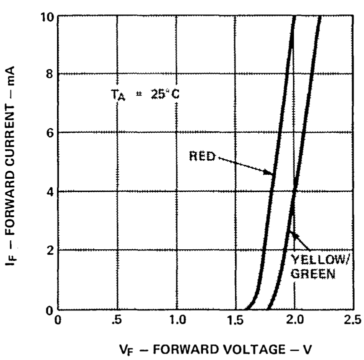


Figure 2. Forward Current vs. Forward Voltage

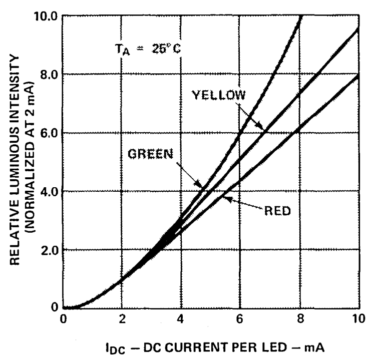


Figure 3. Relative Luminous Intensity vs. Forward Current

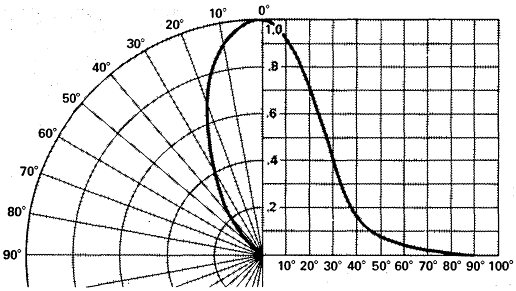


Figure 4. Relative Luminous Intensity vs. Angular Displacement for T-1 3/4 Lamp

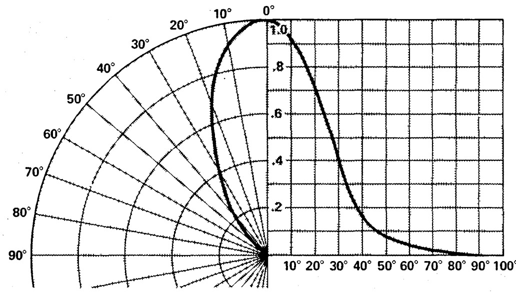


Figure 5. Relative Luminous Intensity vs. Angular Displacement for T-1 Lamp

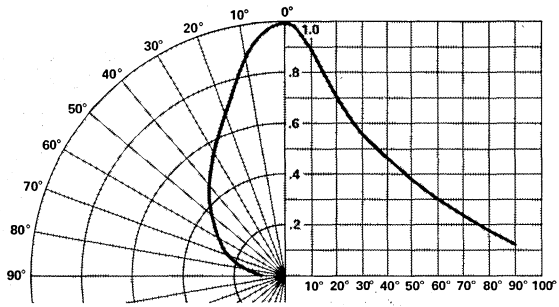


Figure 6. Relative Luminous Intensity vs. Angular Displacement for Subminiature Lamp

HEWLETT PACKARD

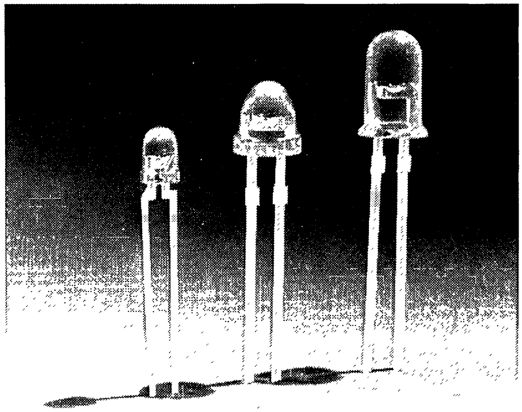
ULTRA-BRIGHT LED LAMP SERIES

T-1 3/4 HLMP-3750,-3850,-3950
T-1 3/4 LOW PROFILE HLMP-3390,-3490,-3590
T-1 HLMP-1340,-1440,-1540

TECHNICAL DATA JANUARY 1986

Features

- IMPROVED BRIGHTNESS
- IMPROVED COLOR PERFORMANCE
- AVAILABLE IN POPULAR T-1 and T-1 3/4 PACKAGES
- NEW STURDY LEADS
- IC COMPATIBLE/LOW CURRENT CAPABILITY
- RELIABLE AND RUGGED
- CHOICE OF 3 BRIGHT COLORS
  High Efficiency Red
  High Brightness Yellow
  High Performance Green



Description

These clear, non-diffused lamps out perform conventional LED lamps. By utilizing new higher intensity material, we achieve superior product performance.

The HLMP-3750/-3390/-1340 Series Lamps are Gallium Arsenide Phosphide on Gallium Phosphide red light emitting diodes. The HLMP-3850/-3490/-1440 Series are Gallium Arsenide Phosphide on Gallium Phosphide yellow light emitting diodes. The HLMP-3950/-3590/-1540 Series lamps are Gallium Phosphide green light emitting diodes.

Applications

- LIGHTED SWITCHES
- BACKLIGHTING FRONT PANELS
- LIGHT PIPE SOURCES
- KEYBOARD INDICATORS

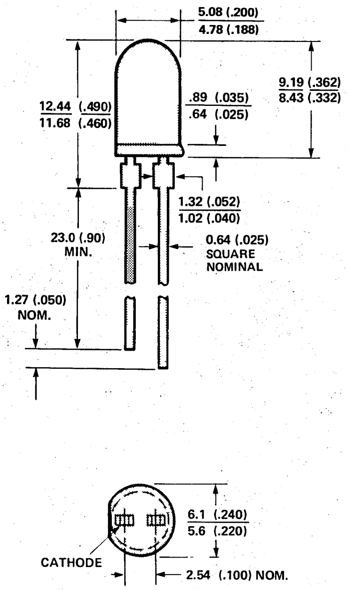
SOLID STATE LAMPS

Axial Luminous Intensity and Viewing Angle @ 25°C

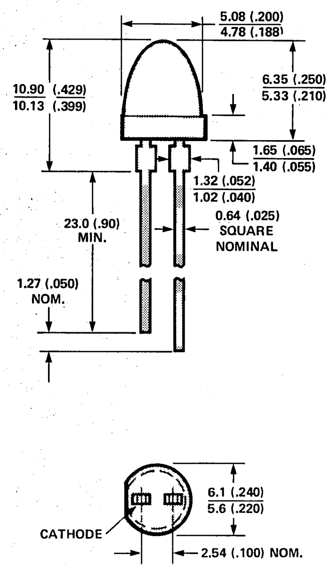
Part Number HLMP-	Package Description	Color	I_V (mcd) @ 20 mA DC Min.	Typ.	2Θ 1/2 Note 1.	Package Outline
3750	T-1 3/4	HER	80	125	24°	A
3850		Yellow	80	140	24°	A
3950		Green	80	120	24°	A
3390	T-1 3/4 Low Profile	HER	35	55	32°	B
3490		Yellow	35	55	32°	B
3590		Green	35	55	32°	B
1340	T-1	HER	24	35	45°	C
1440		Yellow	24	35	45°	C
1540		Green	24	35	45°	C

NOTE:
1. Θ1/2 is the typical off-axis angle at which the luminous intensity is half the axial luminous intensity.

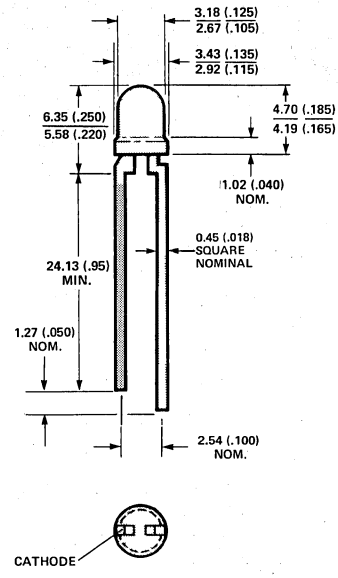
Package Dimensions



PACKAGE OUTLINE "A"
HLMP-3750, 3850, 3950



PACKAGE OUTLINE "B"
HLMP-3390, 3490, 3590



PACKAGE OUTLINE "C"
HLMP-1340, 1440, 1540

NOTES:
1. All dimensions are in millimeters (inches).
2. An epoxy meniscus may extend about 1mm (0.40") down the leads.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Red	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Transient Forward Current[4] (10 μsec pulse)	500	500	500	mA
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Operating Temperature Range	−55 to +100	−55 to +100	−20 to +100	°C
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:
1. See Figure 2 to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	T-1 3/4	T-1 3/4 Low Dome	T-1	Min.	Typ.	Max.	Units	Test Conditions
λ_p	Peak Wavelength	3750 3850 3950	3390 3490 3590	1340 1440 1540		635 583 565		nm	Measurement at peak
λ_d	Dominant Wavelength	3750 3850 3950	3390 3490 3590	1340 1440 1540		626 585 571		nm	Note 1
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	3750 3850 3950	3390 3490 3590	1340 1440 1540		40 36 28		nm	
τ_s	Speed of Response	3750 3850 3950	3390 3490 3590	1340 1440 1540		90 90 500		ns	
C	Capacitance	3750 3850 3950	3390 3490 3590	1340 1440 1540		16 18 18		pF	$V_F = 0$; f = 1 MHz
Θ_{JC}	Thermal Resistance	3750 3850 3950	3390 3490 3590			95 95 95		°C/W	Junction to Cathode Lead
				1340 1440 1540		120 120 120			
V_F	Forward Voltage	3750 3850 3950	3390 3490 3590	1340 1440 1540	1.6 1.6 1.6	2.2 2.2 2.3	3.0 3.0 3.0	V	$I_F = 20$ mA (Figure 3)
V_R	Reverse Breakdown Voltage	3750 3850 3950	3390 3490 3590	1340 1440 1540	5.0			V	$I_F = 100\ \mu A$
η_V	Luminous Efficacy	3750 3850 3950	3390 3490 3590	1340 1440 1540		145 500 595		$\frac{\text{lumens}}{\text{watt}}$	Note 2

NOTES:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

Red, Yellow and Green

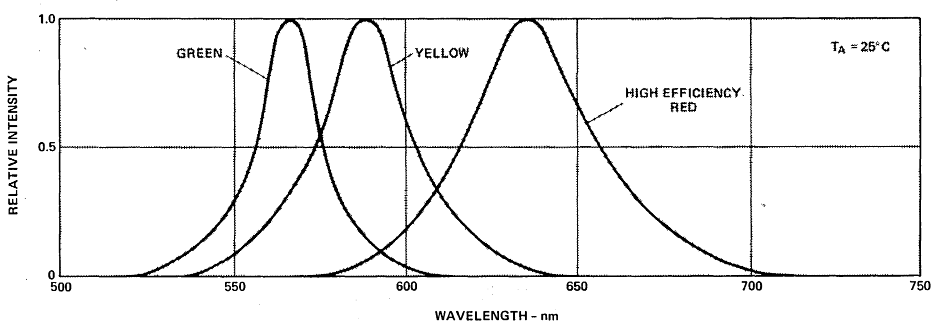


Figure 1. Relative Intensity vs. Wavelength.

SOLID STATE LAMPS

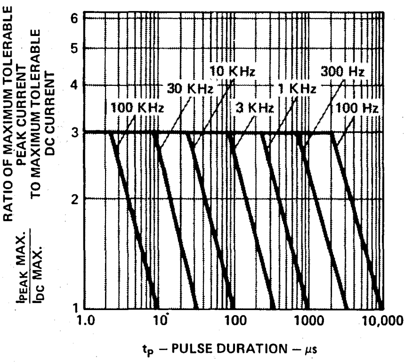


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

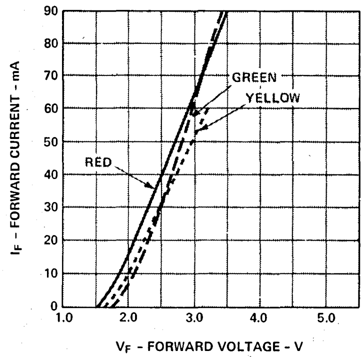


Figure 3. Forward Current vs. Forward Voltage.

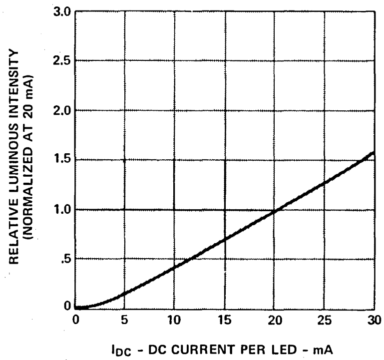


Figure 4. Relative Luminous Intensity vs. Forward Current.

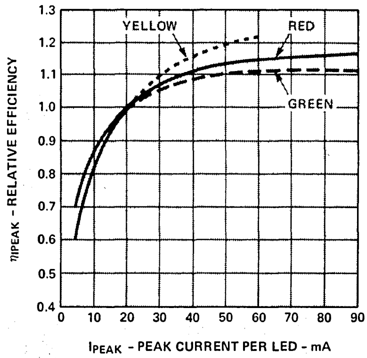


Figure 5. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

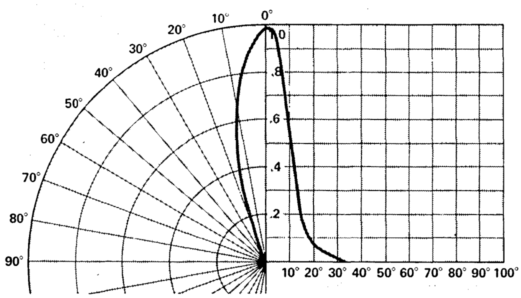


Figure 6. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Lamp.

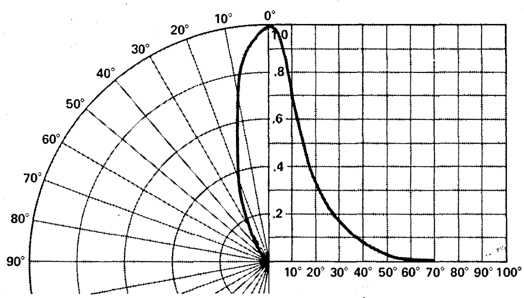


Figure 7. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Low Profile Lamp.

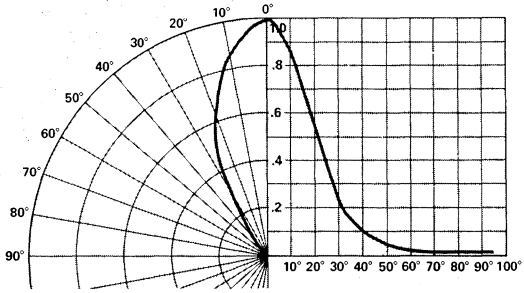


Figure 8. Relative Luminous Intensity vs. Angular Displacement. T-1 Lamp.

HEWLETT PACKARD

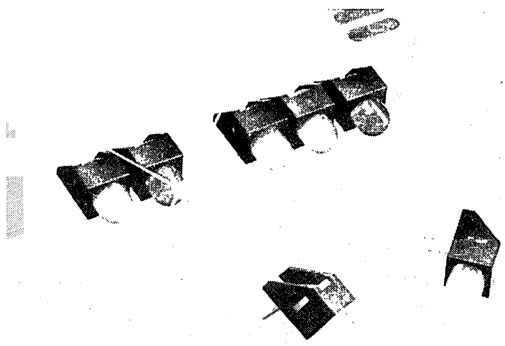
LED RIGHT ANGLE INDICATORS T-1 3/4 (5mm)

RED	HLMP-5000	HER	HLMP-5030	HER 5 V	HLMP-5060
RED 5 V	HLMP-5005	YELLOW	HLMP-5040	YELLOW 5 V	HLMP-5070
RED 12 V	HLMP-5012	GREEN	HLMP-5050	GREEN 5 V	HLMP-5080

TECHNICAL DATA JANUARY 1986

Features

- IDEAL FOR CARD EDGE STATUS INDICATION
- PACKAGE DESIGN ALLOWS FLUSH SEATING ON A PC BOARD
- MAY BE SIDE STACKED ON 6.35 mm (0.25") CENTERS
- LEDs AVAILABLE IN FOUR COLORS, WITH OR WITHOUT INTEGRATED CURRENT LIMITING RESISTOR IN T-1 3/4 TINTED DIFFUSED PACKAGES
- ADDITIONAL CATALOG LAMPS AVAILABLE AS OPTIONS

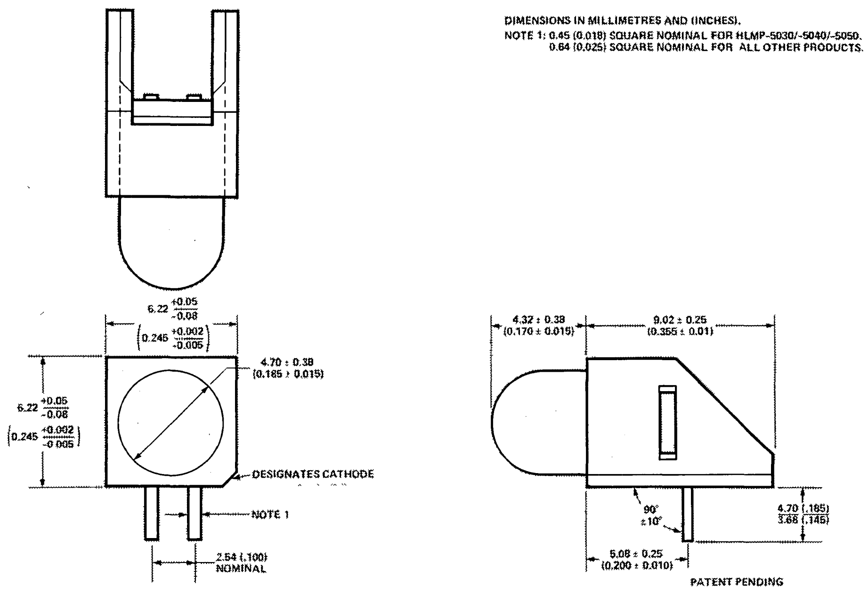


Description

The HLMP-5000 series of Right Angle Indicators are industry standard status indicators that incorporate a tinted diffused T-1 3/4 LED lamp in a black plastic housing. The indicators are available in standard Red, High Efficiency Red, Yellow, or High Performance Green with or without an integrated current limiting resistor. These products are designed to be used as back panel diagnostic indicators and card edge logic status indicators.

SOLID STATE LAMPS

Package Dimensions



PATENT PENDING

Electrical/Optical Characteristics at $T_A = 25°C$

RIGHT ANGLE INDICATORS WITHOUT INTEGRATED CURRENT LIMITING RESISTOR							
Part Number	Color	Luminous Intensity (I_V) mcd		Forward Voltage (V_F)		Test Condition for I_V and V_F	Minimum Reverse Breakdown Voltage at (V_{BR}) $I_R = 100\ \mu A$
		Min.	Typ.	Typ.	Max.		
HLMP-5000	Red	2.0	4.0	1.6	2.0	$I_F = 20$ mA	3.0
HLMP-5030	High Efficiency Red	3.0	6.0	2.2	3.0	$I_F = 10$ mA	5.0
HLMP-5040	Yellow	3.0	6.0	2.2	3.0	$I_F = 10$ mA	5.0
HLMP-5050	Green	3.0	6.0	2.3	3.0	$I_F = 10$ mA	5.0

RIGHT ANGLE INDICATORS WITH CURRENT LIMITING RESISTOR							
Part Number	Color	Luminous Intensity (I_V) mcd		Forward Current (I_F) mA		Test Condition for I_V and I_F	Minimum Reverse Breakdown Voltage at (V_{BR}) $I_R = 100\ \mu A$
		Min.	Typ.	Typ.	Max.		
HLMP-5012	Red	1.0	2.0	13	20	$V_F = 12$ V	3.0
HLMP-5005	Red	1.0	2.0	13	20	$V_F = 5$ V	3.0
HLMP-5060	High Efficiency Red	1.5	4.0	10	15	$V_F = 5$ V	5.0
HLMP-5070	Yellow	1.5	4.0	10	15	$V_F = 5$ V	5.0
HLMP-5080	Green	1.5	4.0	12	15	$V_F = 5$ V	5.0

Ordering Information

To order T-1 3/4 high dome lamps in addition to the parts indicated above, select the base part number and add the option code 010. For example: HLMP-3750-010.

All Hewlett-Packard T-1 3/4 high-dome lamps, except ferrules, are available in right angle housing. Contact your local Hewlett-Packard Sales Office or authorized components distributor for additional ordering information.

Right Angle Indicator (Part Number)	Equivalent T-1 3/4 LED Lamp (Part Number)
HLMP-5000	HLMP-3001
HLMP-5005	HLMP-3105
HLMP-5012	HLMP-3112
HLMP-5030	HLMP-3300
HLMP-5040	HLMP-3400
HLMP-5050	HLMP-3502
HLMP-5060	HLMP-3600
HLMP-5070	HLMP-3650
HLMP-5080	HLMP-3680

Absolute Maximum Ratings and Other Electrical/Optical Characteristics

The absolute maximum ratings and typical device characteristics are identical to those of the T-1 3/4 LED lamps listed here. For information about these characteristics, see the data sheets of the equivalent T-1 3/4 LED lamp.

HEWLETT PACKARD

T-1 (3mm) RIGHT ANGLE LED INDICATORS

RED HLMP-1002-010	HER HLMP-1301-010	HER 5V HLMP-1600-010
RED 5V HLMP-1100-010	YELLOW HLMP-1401-010	YELLOW 5V HLMP-1620-010
	GREEN HLMP-1503-010	GREEN 5V HLMP-1640-010

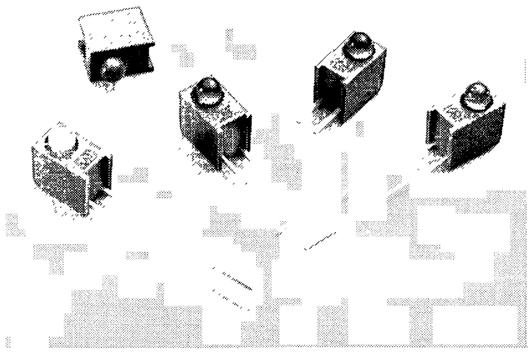
TECHNICAL DATA JANUARY 1986

Features

- IDEAL FOR CARD EDGE STATUS INDICATION
- PACKAGE DESIGN ALLOWS FLUSH SEATING ON A PC BOARD
- MAY BE SIDE STACKED ON 4.57 mm (0.18 in) CENTERS
- UP TO 8 UNITS MAY BE COUPLED FOR A HORIZONTAL ARRAY CONFIGURATION WITH A COMMON COUPLING BAR (SEE T-1 RIGHT ANGLE ARRAY DATA SHEET)
- LEDs AVAILABLE IN ALL LED COLORS, WITH OR WITHOUT INTEGRATED CURRENT LIMITING RESISTOR IN T-1 PACKAGES
- EASY FLUX REMOVAL DESIGN
- HOUSING MATERIAL MEETS UL 94V-0 RATING
- ADDITIONAL CATALOG LAMPS AVAILABLE AS OPTIONS

Description

Hewlett-Packard T-1 Right Angle Indicators are industry standard status indicators that incorporate a tinted diffused T-1 LED lamp in a black plastic housing. The indicators are available in Standard Red, High Efficiency Red, Orange, Yellow, High Performance Green, and Emerald Green, with or without an integrated current limiting resistor. These products are designed to be used as back panel diagnostic indicators and card edge logic status indicators.



Ordering Information

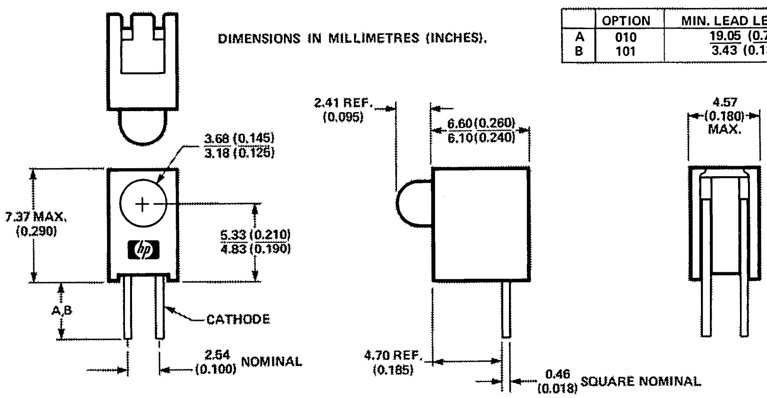
To order other T-1 High Dome Lamps in Right Angle Housings in addition to the parts indicated above, select the base part number and add the option code 010 or 101, depending on the lead length desired (see drawing below). For example, by ordering HLMP-1302-010, you would receive the long lead option. By ordering HLMP-1302-101, you would receive the short lead option.

Arrays made by connecting two to eight single Right Angle Indicators with a Common Coupling Bar are available. Ordering information for arrays may be found on the T-1 Right Angle Array data sheet.

The above data sheet information is for the most commonly ordered part numbers. Refer to other T-1 base part number specifications in this catalog for other lamp types that may be ordered with the right angle option.

Package Dimensions

	OPTION	MIN. LEAD LENGTH
A	010	19.05 (0.750)
B	101	3.43 (0.135)



Electrical/Optical Characteristics at $T_A = 25°C$

RIGHT ANGLE INDICATORS WITHOUT INTEGRATED CURRENT LIMITING RESISTOR

Part Number	Color	Luminous Intensity (I_V) mcd		Forward Voltage (V_F)		Test Condition for I_V and V_F	Minimum Reverse Breakdown V at (V_{BR}) IR = 100μA	Replaces Dialight Part Number
		Min.	Typ.	Typ.	Max.			
HLMP-1002-010	Red	1.5	2.5	1.6	2.0	$I_F = 20$ mA	3.0	551-0405
HLMP-1301-010	High Efficiency Red	2.0	2.5	2.2	3.0	$I_F = 10$ mA	5.0	N/A
HLMP-1401-010	Yellow	2.0	3.0	2.2	3.0	$I_F = 10$ mA	5.0	551-0305
HLMP-1503-010	Green	1.0	2.0	2.3	3.0	$I_F = 10$ mA	5.0	551-0205

RIGHT ANGLE INDICATORS WITH CURRENT LIMITING RESISTOR

Part Number	Color	Luminous Intensity (I_V) mcd		Forward Current (I_F)		Test Condition for I_V and I_F	Minimum Reverse Breakdown V at (V_{BR}) IR = 100μA	Replaces Dialight Part Number
		Min.	Typ.	Typ.	Max.			
HLMP-1100-010	Red	0.8	1.5	13.0	20.0	$V_F = 5$ V	3.0	555-0505
HLMP-1600-010	High Efficiency Red	1.5	4.0	10.0	15.0	$V_F = 5$ V	5.0	N/A
HLMP-1620-010	Yellow	1.5	4.0	10.0	15.0	$V_F = 5$ V	5.0	N/A
HLMP-1640-010	Green	1.5	4.0	12.0	15.0	$V_F = 5$ V	5.0	N/A

Absolute Maximum Ratings and Other Electrical/Optical Characteristics

The absolute maximum ratings and typical device characteristics are identical to those of the T-1 LED lamps listed here. For information about these characteristics, see the data sheets of the equivalent T-1 LED lamp.

HEWLETT PACKARD

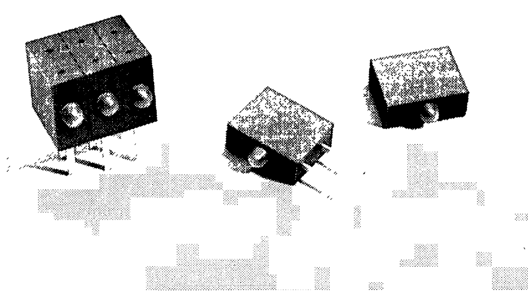
SUBMINIATURE LED RIGHT ANGLE INDICATORS

RED HLMP-6000-010
HIGH EFFICIENCY RED HLMP-6300-010
YELLOW HLMP-6400-010
GREEN HLMP-6500-010

TECHNICAL DATA JANUARY 1986

Features

- IDEAL FOR PC BOARD STATUS INDICATION
- SIDE STACKABLE ON 2.54 mm (0.100 in) CENTERS
- AVAILABLE IN FOUR COLORS
- HOUSING MEETS UL 94V-O FLAMMABILITY SPECIFICATIONS
- ADDITIONAL CATALOG LAMPS AVAILABLE AS OPTIONS



Description

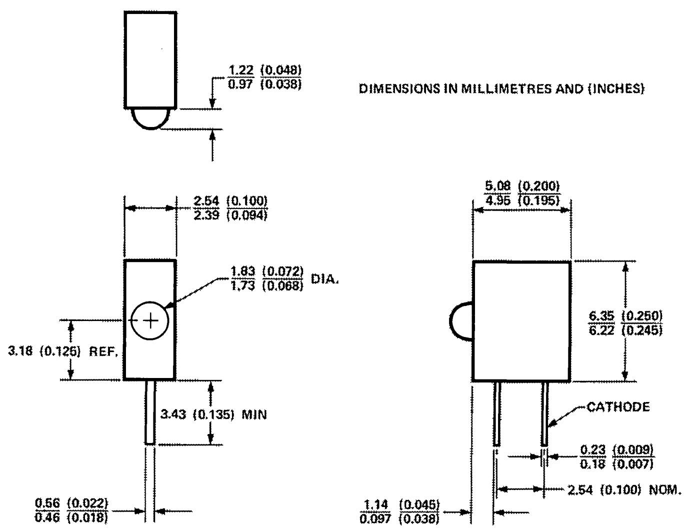
The Hewlett-Packard series of Subminiature Right Angle Indicators are industry standard status indicators that incorporate tinted diffused LED lamps in black plastic housings. The 2.54mm (0.100 in) wide packages may be side stacked for maximum board space savings. The silver plated leads are in line on 2.54mm (0.100 in) centers, a standard spacing that makes the PC board layout straightforward. These products are designed to be used as back panel diagnostic indicators and logic status indicators on PC boards.

Ordering Information

To order Subminiature Right Angle indicators, order the base part number and add the option code 010. For price and delivery on Resistor Subminiature Right Angle Indicators and other subminiature LEDs not indicated above, please contact your nearest H.P. Components representative. A cross reference to Dialight part numbers appears on the next page.

SOLID STATE LAMPS

Package Dimensions



Electrical/Optical Characteristics at $T_A = 25°C$

RIGHT ANGLE INDICATORS WITHOUT INTEGRATED CURRENT LIMITING RESISTOR

Part Number	Color	Luminous Intensity (Iv) mcd		Forward Voltage (V_F)		Test Condition for Iv and V_F	Minimum Reverse Breakdown Voltage at (V_{BR}) IR = 100 microA
		Min.	Typ.	Typ.	Max.		
HLMP-6000-010	Red	0.5	1.2	1.6	2.0	$I_F = 10$ mA	3.0
HLMP-6300-010	High Efficiency Red	1.0	3.0	2.2	3.0	$I_F = 10$ mA	5.0
HLMP-6400-010	Yellow	1.0	3.0	2.2	3.0	$I_F = 10$ mA	5.0
HLMP 6500-010	Green	1.0	3.0	2.3	3.0	$I_F = 10$ mA	5.0

Cross Reference

The following list crosses Hewlett-Packard Subminiature Right Angle Indicators to the closest Dialight part number. The H.P. product will meet or exceed the cross referenced part in electrical and optical performance.

Dialight Part No.	Hewlett-Packard Part No.	Color/Description
555-2001	HLMP-6000-010	Standard Red
555-2007	HLMP-6620-010*	Red/5V Resistor lamp
555-2004	HLMP-6600-010*	Red/5V Resistor lamp
555-2301	HLMP-6500-010	Green
555-2303	HLMP-6820-010*	Green/5V Resistor lamp
555-2401	HLMP-6400-010*	Yellow
555-2403	HLMP-6720-010*	Yellow/5V Resistor lamp

*Please contact your nearest H.P. Components representative for pricing and delivery.

Absolute Maximum Ratings and Other Electrical/Optical Characteristics

The absolute maximum ratings and typical device characteristics are identical to those of the Subminiature lamps listed here. For information about these characteristics, see the data sheets of the equivalent Subminiature lamp.

HEWLETT PACKARD

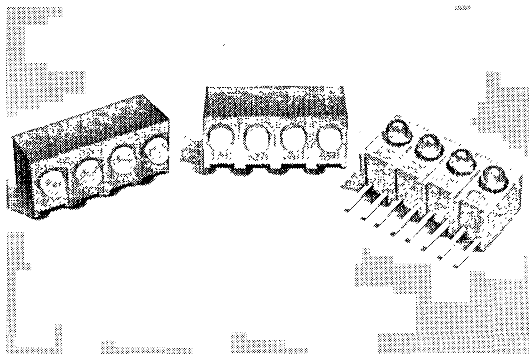
T-1 (3 mm) RIGHT ANGLE ARRAYS

HIGH EFFICIENCY RED HLMP-1301 Option 104
YELLOW HLMP-1401 Option 104
GREEN HLMP-1503 Option 104

TECHNICAL DATA JANUARY 1986

Features

- IDEAL FOR PC BOARD STATUS INDICATION
- STANDARD 4 ELEMENT CONFIGURATION
- EASY HANDLING
- EASY FLUX REMOVAL
- HOUSING MEETS UL 94V-O FLAMMABILITY SPECIFICATIONS
- OTHER CATALOG LAMPS AVAILABLE



Description

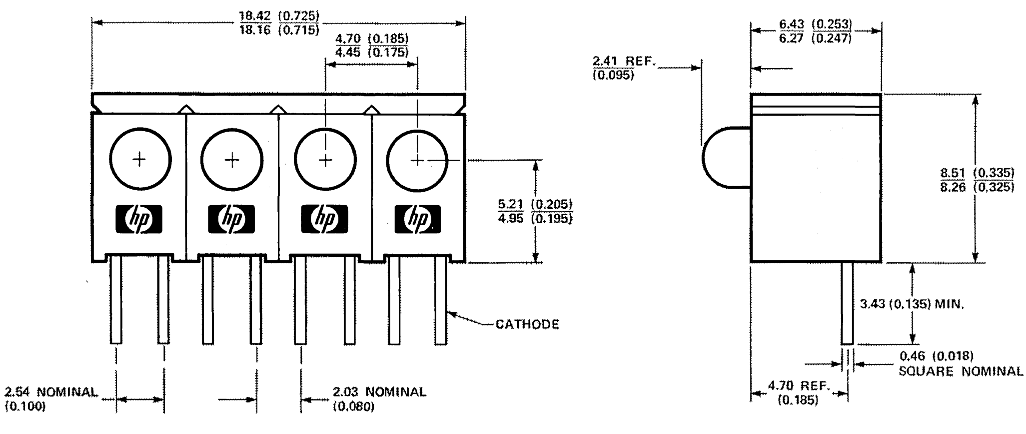
These 4 element right angle arrays incorporate tinted diffused standard lamps for a good balance of viewing angle and intensity. Single units are held together by a plastic tie bar. The leads of each member of the array are spaced on 2.54 mm (0.100 in) centers. Lead spacing between adjacent lamps in the array is on 2.03 mm (0.080 in) centers. These products are designed to be used as back panel diagnostic indicators and logic status indicators on PC boards.

Ordering Information

Use the option code 104 in addition to the base part number to order these arrays. Arrays from 2 to 8 elements in length and special lamp color combinations within an array are also available. Please contact your nearest Hewlett-Packard Components representative for ordering information on these special items.

SOLID STATE LAMPS

Package Dimensions



DIMENSIONS IN MILLIMETRES AND INCHES.

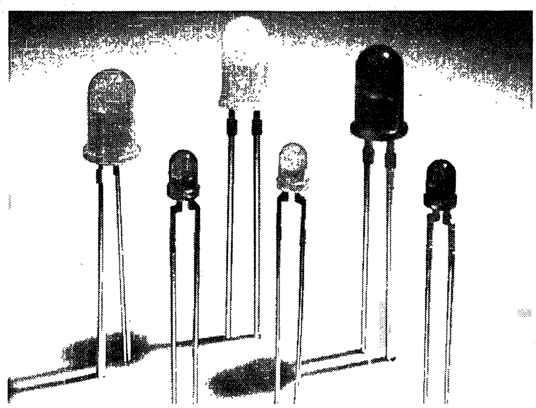
HEWLETT PACKARD

INTEGRATED RESISTOR LAMPS
5 Volt and 12 Volt Series in T-1 and T-1 3/4 Packages

TECHNICAL DATA JANUARY 1986

Features

- **INTEGRAL CURRENT LIMITING RESISTOR**
- **TTL COMPATIBLE**
  Requires no External Current Limiter with 5 Volt/12 Volt Supply
- **COST EFFECTIVE**
  Saves Space and Resistor Cost
- **WIDE VIEWING ANGLE**
- **AVAILABLE IN ALL COLORS**
  Red, High Efficiency Red, Yellow and High Performance Green in T-1 and T-1 3/4 Packages



Description

The 5 volt and 12 volt series lamps contain an integral current limiting resistor in series with the LED. This allows the lamp to be driven from a 5 volt/12 volt source without an external current limiter. The red LEDs are made from GaAsP on a GaAs substrate. The High Efficiency Red and Yellow devices use GaAsP on a GaP substrate.

The green devices use GaP on a GaP substrate. The diffused lamps provide a wide off-axis viewing angle.

The T-1 3/4 lamps are provided with sturdy leads suitable for wire wrap applications. The T-1 3/4 lamps may be front panel mounted by using the HLMP-0103 clip and ring.

Color	P/N HLMP-	Package	Operating Voltage	I_V mcd Min.	I_V mcd Typ.	2Θ 1/2[1]	Package Outline
Red	1100	T-1 Tinted Diffused	5	0.8	1.5	60°	A
	1120	T-1 Untinted Diffused	5	0.8	1.5	60°	A
	3105	T-1 3/4 Tinted Diffused	5	1.0	2.0	75°	B
	3112		12	1.0	2.0	75°	B
High Efficiency Red	1600	T-1 Tinted Diffused	5	1.5	4.0	60°	A
	1601		12				
	3600	T-1 3/4 Tinted Diffused	5			65°	B
	3601		12				
Yellow	1620	T-1 Tinted Diffused	5	1.5	4.0	60°	A
	1621		12				
	3650	T-1 3/4 Tinted Diffused	5			75°	B
	3651		12				
High Performance Green	1640	T-1 Tinted Diffused	5	1.5	4.0	60°	A
	1641		12				
	3680	T-1 3/4 Tinted Diffused	5			75°	B
	3681		12				

Notes:
1. Θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.

Absolute Maximum Ratings at $T_A = 25°C$

	Red/HER/Yellow 5 Volt Lamps		Red/HER/Yellow 12 Volt Lamps		Green 5 Volt Lamps		Green 12 Volt Lamps	
DC Forward Voltage ($T_A = 25°C$)	7.5 Volts[2]		15 Volts[3]		7.5 Volts[2]		15 Volts[3]	
Reverse Voltage ($I_R = 100\ \mu A$)	GaAsP	3 Volts	GaAsP	3 Volts	GaAsP	3 Volts	GaAsP	3 Volts
	GaP	5 Volts	GaP	5 Volts	GaP	5 Volts	GaP	5 Volts
Operating Temperature Range	−40° C to 85° C		−40° C to 85° C		−20° C to 85° C		−20° C to 85° C	
Storage Temperature Range	−55° C to 100° C		−55° C to 100° C		−55° C to 100° C		−55° C to 100° C	
Lead Soldering Temperature	260° C for 5 seconds							

Notes:
2. Derate from $T_A = 50°C$ at 0.071V/° C, see Figure 3.
3. Derate from $T_A = 50°C$ at 0.086V/° C, see Figure 4.

Electrical/Optical Characteristics at $T_A = 25°C$

		Red			High Efficiency Red			Yellow			Green				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Test Conditions
λ_p	Peak Wavelength		655			635			583			565		nm	
λ_d	Dominant Wavelength		648			626			585			569		nm	Note 4
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		24			40			36			28		nm	
Θ_{JC}	Thermal Resistance		120			120			120			120		° C/W	Junction to Cathode Lead (Note 6)
Θ_{JC}	Thermal Resistance		95			95			95			95		° C/W	Junction to Cathode Lead (Note 7)
I_F	Forward Current 12 V Devices		13	20		13	20		13	20		13	20	mA	$V_F = 12\ V$
I_F	Forward Current 5 V Devices		13	20		10	15		10	15		12	15	mA	$V_F = 5\ V$
η_V	Luminous Efficacy		65			145			500			595		lumen /watt	Note 5
V_R	Reverse Breakdown Voltage	3.0			5.0			5.0			5.0			V	$I_R = 100\ \mu A$

Notes:
4. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
5. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$. Where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.
6. For Figure A package type.
7. For Figure B package type.

Package Dimensions

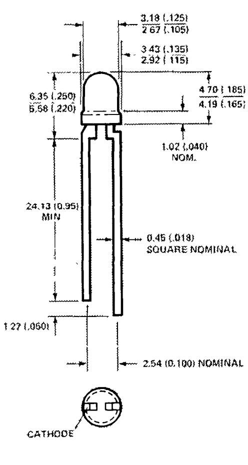


Figure A. T-1 Package

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

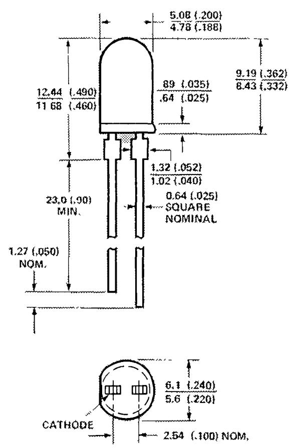


Figure B. T-1 3/4 Package

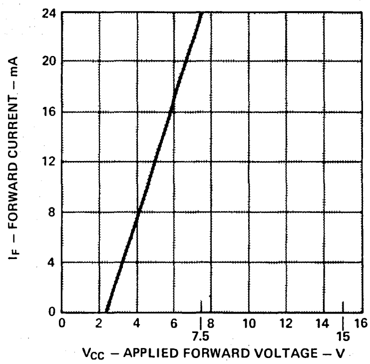


Figure 1. Forward Current vs. Applied Forward Voltage. 5 Volt Devices

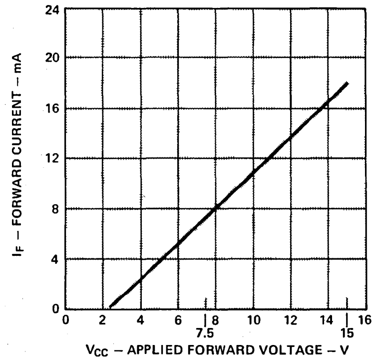


Figure 2. Forward Current vs. Applied Forward Voltage. 12 Volt Devices

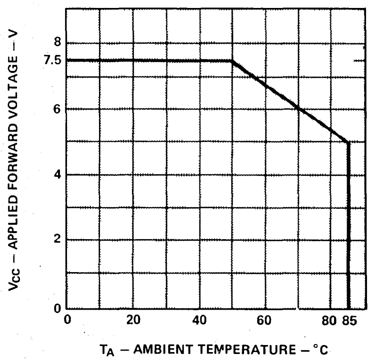


Figure 3. Maximum Allowed Applied Forward Voltage vs. Ambient Temperature $R\theta_{JA}$ = 175° C/W. 5 Volt Devices

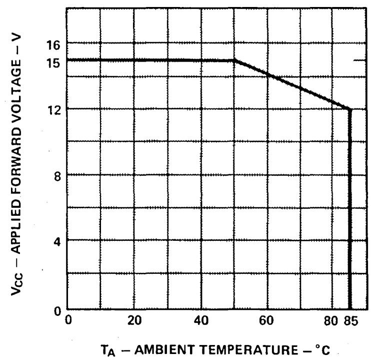


Figure 4. Maximum Allowed Applied Forward Voltage vs. Ambient Temperature $R\theta_{JA}$ = 175° C/W. 12 Volt Devices

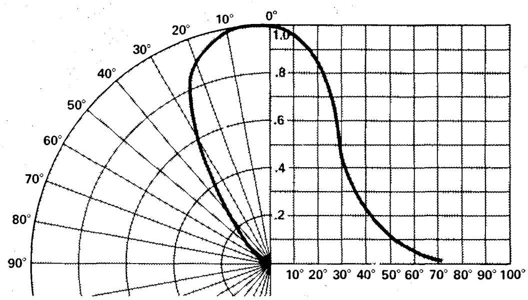


Figure 5. Relative Luminous Intensity vs. Angular Displacement for T-1 Package

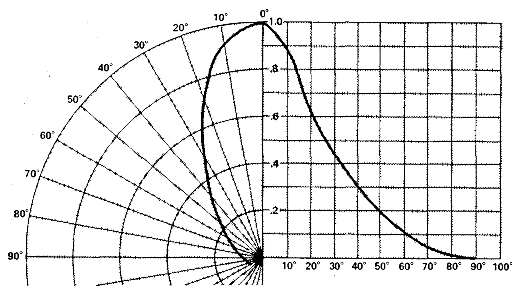


Figure 6. Relative Luminous Intensity vs. Angular Displacement for T-1 3/4 Package

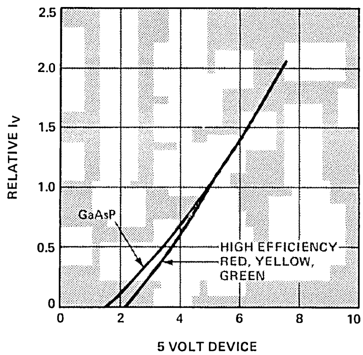


Figure 7. Relative Luminous Intensity vs. Applied Forward Voltage. 5 Volt Devices

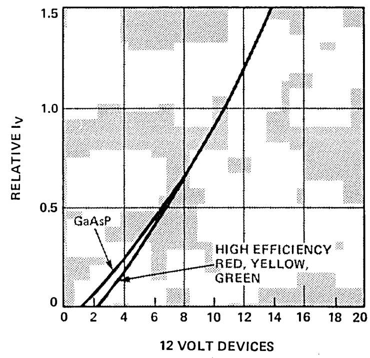


Figure 8. Relative Luminous Intensity vs. Applied Forward Voltage. 12 Volt Devices

SOLID STATE LAMPS

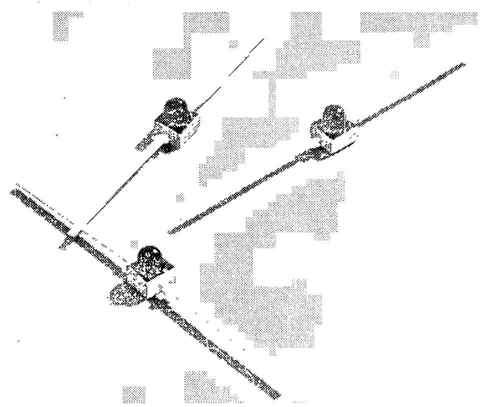
HEWLETT PACKARD

SUBMINIATURE RESISTOR LAMPS 5 VOLT 4 mA AND 5 VOLT 10 mA SERIES

TECHNICAL DATA JANUARY 1986

Features

- INTEGRAL CURRENT LIMITING RESISTOR
- TTL AND LSTTL COMPATIBLE
- REQUIRES NO EXTERNAL RESISTOR WITH 5 VOLT SUPPLY
- SPACE SAVING SUBMINIATURE PACKAGE
- WIDE VIEWING ANGLE
- CHOICE OF CURRENT LEVEL, 4 mA or 10 mA
- AVAILABLE IN HIGH EFFICIENCY RED, YELLOW, AND GREEN
- IDEALLY SUITED FOR PORTABLE OR SPACE CONSTRAINED APPLICATIONS



Description

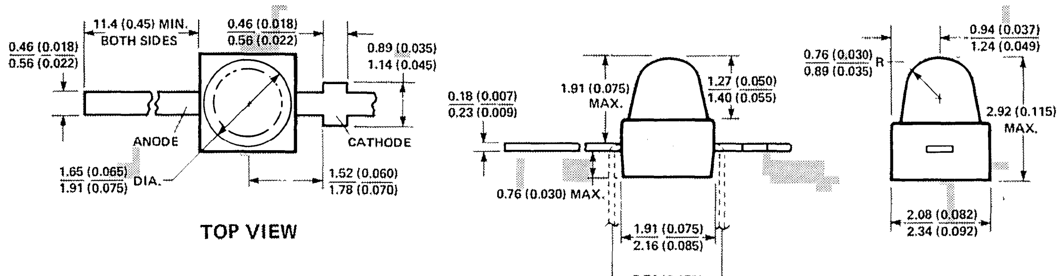
The subminiature resistor lamps contain an integral current limiting resistor in series with the LED. This allows the lamp to be driven from a 5 volt source without an external current limiter. The high efficiency red and yellow devices use GaAsP on a GaP substrate. The green devices use GaP on a GaP substrate. The tinted, diffused epoxy lens provides high on-off contrast and a wide viewing angle. The following special configurations are available on request:

1. Surface Mount Gull Wing Bend — Refer to the Surface Mount Gull Wing Data Sheet.
2. Tape and Reel Packaging
3. Special Lead Bending on 2.54 mm (0.100 in.) and 5.08 mm (0.200) in Centers

Device Selection Guide

	High Efficiency Red	Yellow	Green
5 Volt, 10 mA	HLMP-6600	HLMP-6700	HLMP-6800
5 Volt, 4 mA	HLMP-6620	HLMP-6720	HLMP-6820

Package Dimensions



NOTES
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)
2. OPTIONAL LEAD FORM AVAILABLE.

Absolute Maximum Ratings at $T_A = 25°C$

	HLMP-6600/6620 6700/6720 High Efficiency Red/Yellow	HLMP-6800/6820 Green
DC Forward Voltage	6 Volts	6 Volts
Reverse Voltage ($I_R = 100 \mu A$)	5 Volts	5 Volts
Operating Temperature Range	−40° C to 85° C	−20° C to 85° C
Storage Temperature Range	−55° C to 100° C	
Lead Soldering Temperature 1.6 mm (0.063 in.) From Body	260° C for 3 Seconds	

Electrical/Optical Characteristics at $T_A = 25°C$

		High Efficiency Red						Yellow						Green							
		HLMP-6600			HLMP-6620			HLMP-6700			HLMP-6720			HLMP-6800			HLMP-6820				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	1.3	5.0		0.8	2.0		1.4	5.0		0.9	2.0		1.6	5.0		0.8	2.0		mcd	$V_F = 5$ Volts (See Figure 2)
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		90°			90°			90°			90°			90°			90°			Note 1 (See Figure 3
λ_P	Peak Wavelength		635			635			583			583			565			565		nm	
λ_D	Dominant Wavelength		624			624			586			586			572			572		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		40			40			36			36			28			28		nm	
Θ_{JC}	Thermal Resistance		120			120			120			120			120			120		°C/W	Junction to Cathode Lead
I_F	Forward Current		9.6	13		3.5	5		9.6	13		3.5	5		9.6	13		3.5	5	mA	$V_F = 5$ Volts (See Figure 1)
V_R	Reverse Breakdown Voltage	5.0			5.0			5.0			5.0			5.0			5.0			V	$I_R = 100 \mu A$
η_V	Luminous Efficacy		145			145			500			500			595			595		lm/w	Note 3

Notes:
1. $2\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity in watts/steradion, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

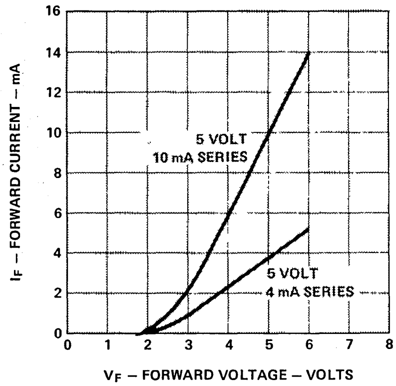


Figure 1. Forward Current vs. Forward Voltage.

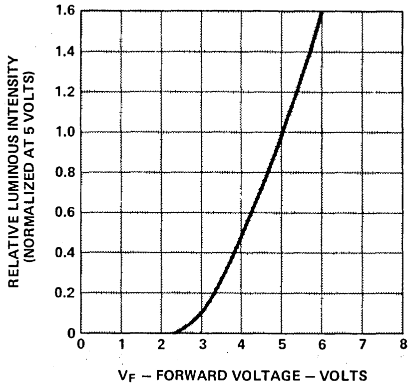


Figure 2. Relative Luminous Intensity vs. Forward Voltage.

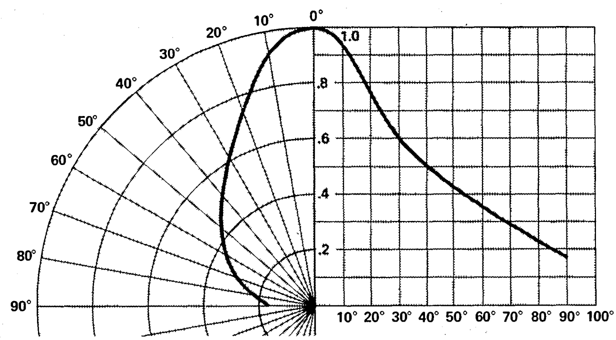


Figure 3. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

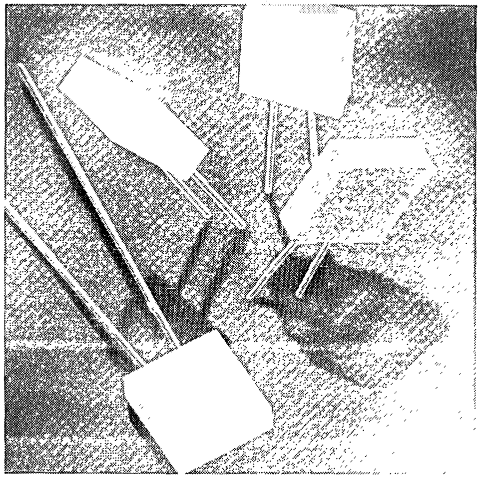
RECTANGULAR SOLID STATE LAMPS

HIGH EFFICIENCY RED HLMP-0300/0301
YELLOW HLMP-0400/0401
HIGH PERFORMANCE GREEN HLMP-0503/0504

TECHNICAL DATA JANUARY 1986

Features

- RECTANGULAR LIGHT EMITTING SURFACE
- FLAT HIGH STERANCE EMITTING SURFACE
- STACKABLE ON 2.54 MM (0.100 INCH) CENTERS
- IDEAL AS FLUSH MOUNTED PANEL INDICATORS
- IDEAL FOR BACKLIGHTING LEGENDS
- LONG LIFE: SOLID STATE RELIABILITY
- CHOICE OF 3 BRIGHT COLORS
  HIGH EFFICIENCY RED
  YELLOW
  HIGH PERFORMANCE GREEN
- IC COMPATIBLE/LOW CURRENT REQUIREMENTS



Description

The HLMP-030X, -040X, -050X are solid state lamps encapsulated in an axial lead rectangular epoxy package. They utilize a tinted, diffused epoxy to provide high on-off contrast and a flat high intensity emitting surface. Borderless package design allows creation of uninterrupted light emitting areas.

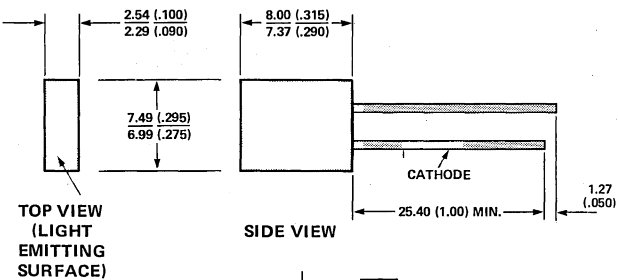
The HLMP-0300 and -0301 have a high efficiency red GaAsP on GaP LED chip in a light red epoxy package. This lamp's efficiency is comparable to that of the GaP red, but extends to higher current levels.

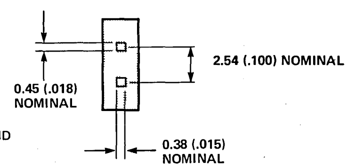
The HLMP-0400 and -0401 provide a yellow GaAsP on GaP LED chip in a yellow epoxy package.

The HLMP-0503 and -0504 provide a green GaP LED chip in a green epoxy package.

SOLID STATE LAMPS

Package Dimensions





BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Axial Luminous Intensity

Color	Part Number	I_V (mcd) @ 20 mA DC Min.	Typ.
High Efficiency Red	HLMP-0300	1.0	2.5
	HLMP-0301	2.5	5.0
Yellow	HLMP-0400	1.5	2.5
	HLMP-0401	3.0	5.0
High Performance Green	HLMP-0503	1.5	2.5
	HLMP-0504	3.0	5.0

Absolute Maximum Ratings at T_A = 25°C

Parameter	HLMP-0300/-0301	HLMP-0400/0401	HLMP-0503/-0504	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Transient Forward Current[4] (10 μs Pulse)	500	500	500	mA
Operating Temperature Range	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range	-55 to +100	-55 to +100	-55 to +100	°C
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:
1. See Figure 5 to establish pulsed operating conditions.
2. For Red and Green Series derate linearly from 50° C at 0.5 mA/° C. For Yellow Series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommedned that the device be operated at peak current beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical/Optical Characteristics at T_A=25°C

		HLMP-0300/-0301			HLMP-0400/-0401			HLMP-0503/-0504				
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		100			100			100		Deg.	Note 1. Figure 6.
λ_P	Peak Wavelength		635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		626			585			569		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		40			36			28		nm	
τ_S	Speed of Response		90			90			500		ns	
C	Capacitance		16			18			18		pF	V_F = 0; f = 1 MHz
Θ_{JC}	Thermal Resistance		120			120			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	1.6	2.2	3.0	1.6	2.2	3.0	1.6	2.3	3.0	V	I_F = 20 mA Figure 2.
V_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	I_R = 100 μA
η_V	Luminous Efficacy		145			500			595		lm/W	Note 3

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

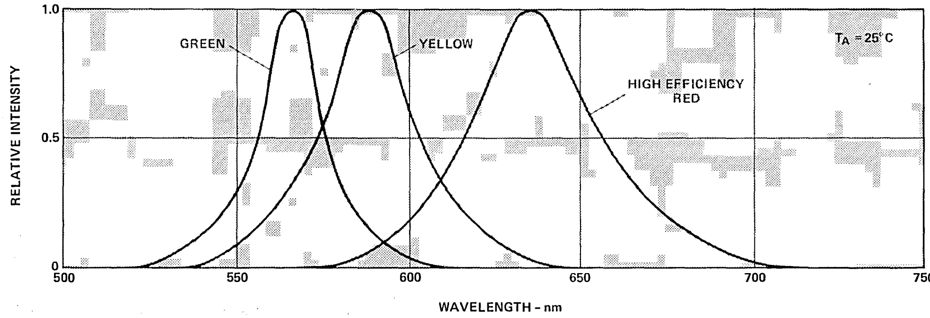


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red, Yellow and Green Rectangular Lamps

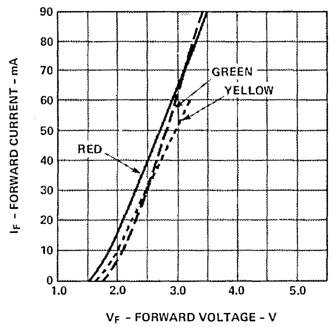


Figure 2. Forward Current vs. Forward Voltage.

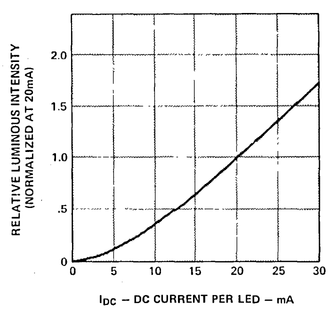


Figure 3. Relative Luminous Intensity vs. Forward Current.

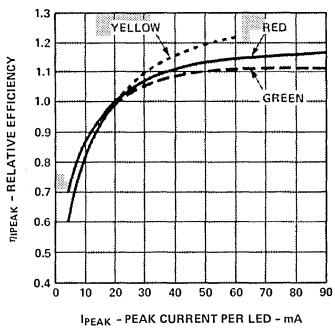


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

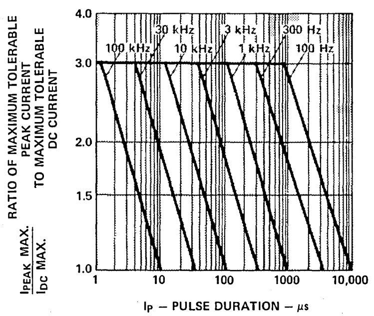


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

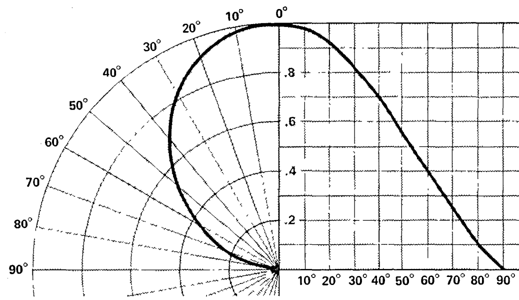


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

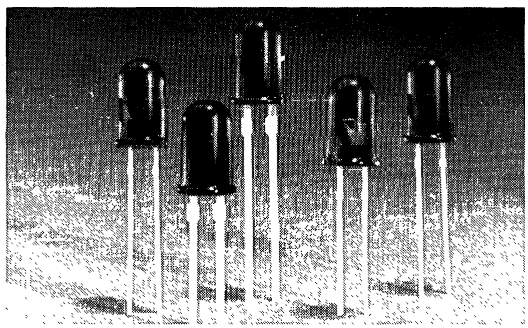
T-1 3/4 (5mm) RED SOLID STATE LAMPS

HLMP-3000
HLMP-3001
HLMP-3002
HLMP-3003
HLMP-3050

TECHNICAL DATA JANUARY 1986

Features

- LOW COST, BROAD APPLICATIONS
- LONG LIFE, SOLID STATE RELIABILITY
- LOW POWER REQUIREMENTS: 20 mA @ 1.6V
- HIGH LIGHT OUTPUT:
  2.0 mcd Typical for HLMP-3000
  4.0 mcd Typical for HLMP-3001
- WIDE AND NARROW VIEWING ANGLE TYPES
- RED DIFFUSED AND NON-DIFFUSED VERSIONS



Description

The HLMP-3000 series lamps are Gallium Arsenide Phosphide light emitting diodes intended for High Volume/ Low Cost applications such as indicators for appliances, smoke detectors, automobile instrument panels and many other commercial uses.

The HLMP-3000/-3001/-3002/-3003 have red diffused lenses where as the HLMP-3050 has a red non-diffused lens. These lamps can be panel mounted using mounting clip HLMP-0103. The HLMP-3000/-3001 lamps have .025" leads and the HLMP-3002/-3003/-3050 have .018" leads.

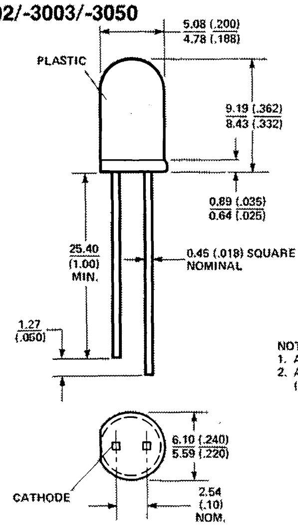
NOTES:
1. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Absolute Maximum Ratings at $T_A = 25°C$

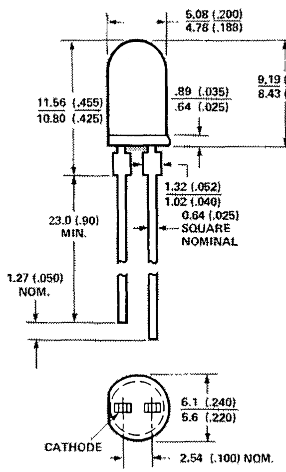
Parameter	3000 Series	Units
Power Dissipation	100	mW
DC Forward Current (Derate linearly from 50° C at 0.2 mA/° C)	50	mA
Average Forward Current	50	mA
Peak Operating Forward Current	1000	mA
Reverse Voltage (I_R = 100 μA)	3	V
Transient Forward Current[1] (10 μsec Pulse)	2000	mA
Operating and Storage Temperature Range	−55° C to +100° C	
Lead Solder Temperature (1.6 mm [0.063 inch] below package base)	260° C for 5 seconds	

Package Dimensions

HLMP-3002/-3003/-3050



HLMP-3000/-3001



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Electrical Characteristics at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	3000/3002	1.0	2.0		mcd	I_F = 20 mA
		3001/3003	2.0	4.0		mcd	I_F = 20 mA
		3050	1.0	2.5		mcd	I_F = 20 mA
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3000/3002 3001/3003 3050		75 75 24		Deg.	I_F = 20 mA
λ_P	Peak Wavelength	3000/3002 3001/3003 3050		655 655 655		nm	Measurement at Peak
λ_d	Dominant Wavelength	3000/3002 3001/3003 3050		648		nm	
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	3000/3002 3001/3003 3050		24		nm	
τ_S	Speed of Response	3000/3002 3001/3003 3050		10		ns	
C	Capacitance	3000/3002 3001/3003 3050		100		pF	V_F = 0, f = 1 MHz
Θ_{JC}	Thermal Resistance	3000/3001 3002/3003 3050		95 120 120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	3000/3002 3001/3003 3050	1.4	1.6	2.0	V	I_F = 20 mA (Fig. 2)
V_R	Reverse Breakdown Voltage	3000/3002 3001/3003 3050	3.0	10		V	I_R = 100 μA

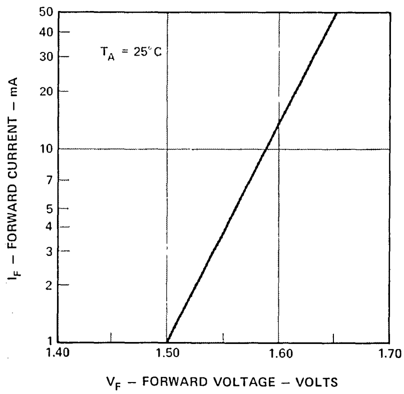


Figure 1. Forward Current Versus Forward Voltage

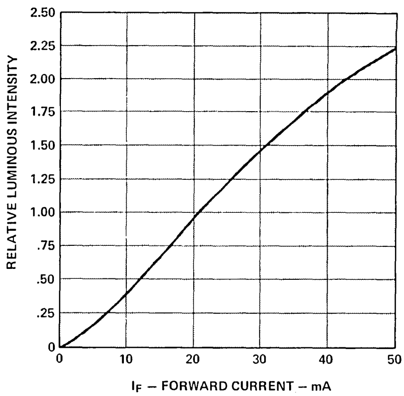


Figure 2. Relative Luminous Intensity Versus Forward Current

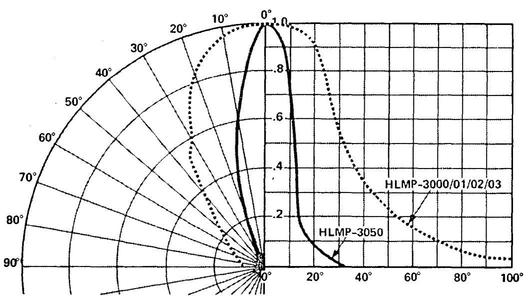


Figure 3. Relative Luminous Intensity Versus Angular Displacement.

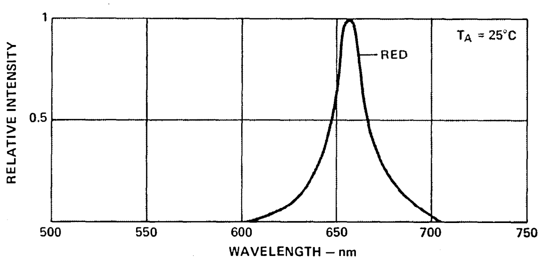


Figure 4. Relative Luminous Intensity Versus Wavelength.

SOLID STATE LAMPS

HEWLETT PACKARD

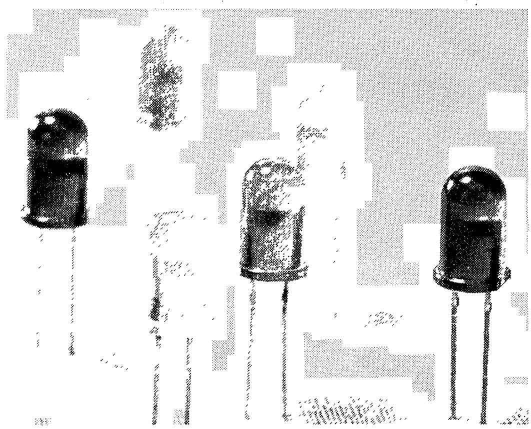
T-1 3/4 (5mm) DIFFUSED SOLID STATE LAMPS

HIGH EFFICIENCY RED • HLMP-3300 SERIES
ORANGE • HLMP-D400 SERIES
YELLOW • HLMP-3400 SERIES
HIGH PERFORMANCE GREEN • HLMP-3500 SERIES
EMERALD GREEN • HLMP-D600 SERIES

TECHNICAL DATA JANUARY 1986

Features

- HIGH INTENSITY
- CHOICE OF 5 BRIGHT COLORS
  - High Efficiency Red
  - Orange
  - Yellow
  - High Performance Green
  - Emerald Green
- POPULAR T-1¾ DIAMETER PACKAGE
- SELECTED MINIMUM INTENSITIES
- WIDE VIEWING ANGLE
- GENERAL PURPOSE LEADS
- RELIABLE AND RUGGED
- AVAILABLE ON TAPE AND REEL

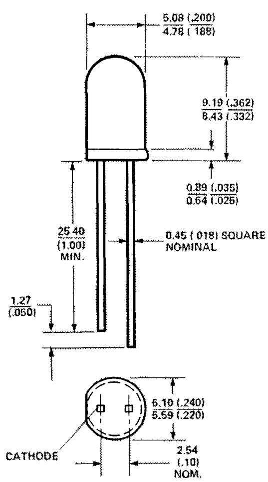


Description

This family of T-1¾ lamps is widely used in general purpose indicator applications. Diffusants, tints, and optical design are balanced to yield superior light output and wide viewing angles. Several intensity choices are available in each color for increased design flexibility.

Part Number HLMP-	Application	Minimum Intensity (mcd) at 10mA	Color (Material)
3300	General Purpose	2.1	High Efficiency Red (GaAsP on GaP)
3301	High Ambient	4.0	
3762	Premium Lamp	8.0	
D400	General Purpose	2.1	Orange (GaAsP on GaP)
D401	High Ambient	4.0	
3400	General Purpose	2.2	Yellow (GaAsP on GaP)
3401	High Ambient	4.0	
3862	Premium Lamp	8.0	
3502	General Purpose	1.6	Green (GaP) 565 nm
3507	High Ambient	4.2	
3962	Premium Lamp	8.0	
D600	General Purpose	1.6	Emerald Green (GaP) 555 nm
D601	High Ambient	4.2	

Package Dimensions



NOTES.
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	High Efficiency Red					
		3300	2.1	3.5			
		3301	4.0	7.0			
		3762	8.0	15.0			
		Orange					
		D400	2.1	3.5			
		D401	4.0	7.0			
		Yellow					
		3400	2.2	4.0			
		3401	4.0	8.0		mcd	$I_F = 10$ mA
		3862	8.0	12.0			
		Green					
		3502	1.6	2.4			
		3507	4.2	5.2			
		3962	8.0	11.0			
		Emerald Green					
		D600	1.6	3.0			
		D601	4.2	6.0			
2Θ1/2	Including Angle Between Half Luminous Intensity Points	High Efficiency Red		65			
		Orange					
		Yellow		75		Deg.	$I_F = 10$ mA See Note 1
		Green					
		Emerald Green					
λ_{PEAK}	Peak Wavelength	High Efficiency Red		635			
		Orange		612			
		Yellow		583		nm	Measurement at Peak
		Green		565			
		Emerald Green		555			
λd	Dominant Wavelength	High Efficiency Red		626			
		Orange		608			
		Yellow		585		nm	See Note 2
		Green		569			
		Emerald Green		556			
τ_S	Speed of Response	High Efficiency Red		90			
		Orange		280			
		Yellow		90		ns	
		Green		500			
		Emerald Green		4000			
C	Capacitance	High Efficiency Red		16			
		Orange		4			
		Yellow		18		pF	$V_F = 0$; f = 1 MHz
		Green		18			
		Emerald Green		35			
θ_{JC}	Thermal Resistance	All		140		°C/W	Junction to Cathode Lead at Seating Plane
V_F	Forward Voltage	HER/Orange	1.5	2.2	3.0		
		Yellow	1.5	2.2	3.0	V	$I_F = 10$ mA
		Grn/Emerald Grn	1.6	2.3	3.0		
V_R	Reverse Breakdown Volt.	All	5.0			V	$I_R = 100\ \mu A$
η_V	Luminous Efficacy	High Efficiency Red		145			
		Orange		262			
		Yellow		500		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3
		Green		595			
		Emerald Green		656			

NOTES:
1. Θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	HER/Orange	Yellow	Grn/Emerald Grn	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage ($I_R = 100\ \mu A$)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	−55 to +100	−55 to +100	−20 to +100	°C
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:

1. See Figure 5 (Red/Orange), 10 (Yellow) or 15 (Green/Emerald Green) to establish pulsed operating conditions.
2. For Red, Orange, Emerald Green, and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C.
3. For Red, Orange, Emerald Green, and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

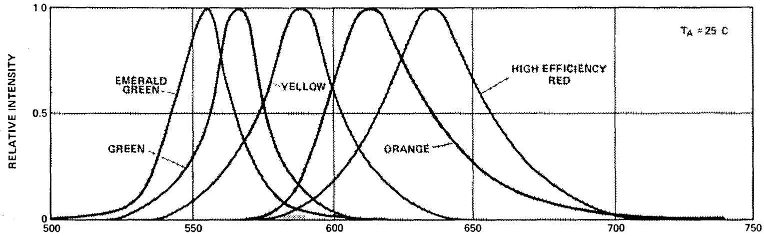


Figure 1. Relative Intensity vs. Wavelength

T-1¾ High Efficiency Red, Orange Diffused Lamps

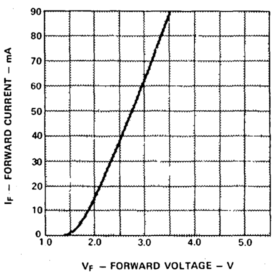


Figure 2. Forward Current vs. Forward Voltage Characteristics.

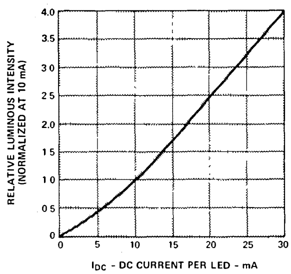


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

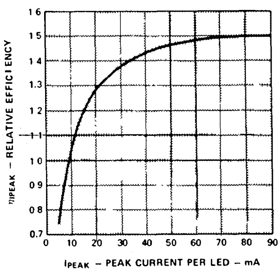


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. LED Peak Current.

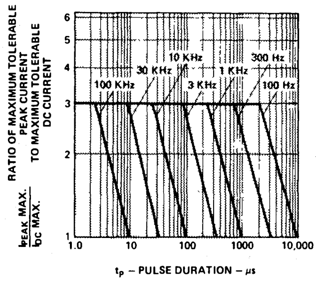


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings

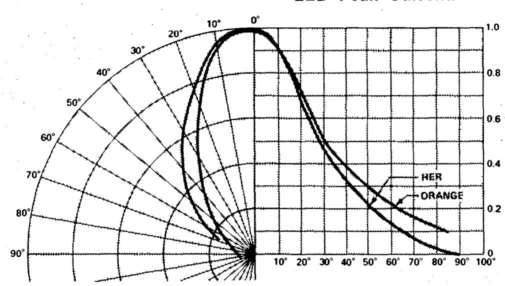


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

T-1¾ Yellow Diffused Lamps

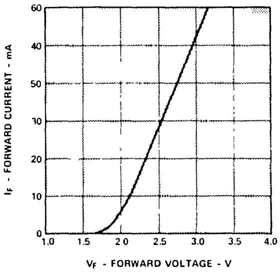


Figure 7. Forward Current vs. Forward Voltage Characteristics.

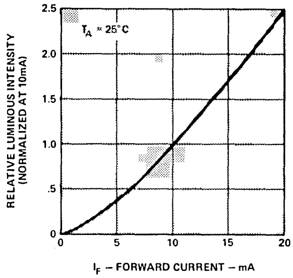


Figure 8. Relative Luminous Intensity vs. Forward Current.

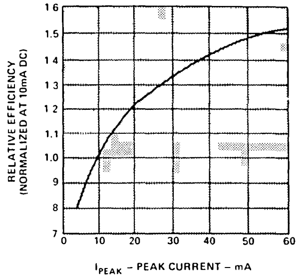


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

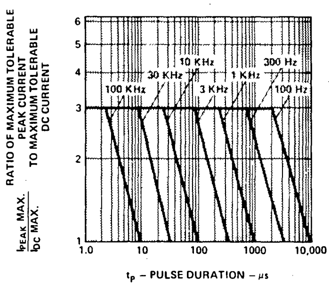


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

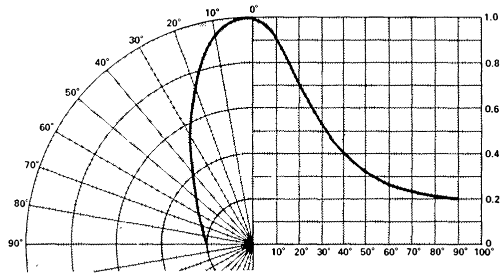


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

T-1¾ Green, Emerald Green Diffused Lamps

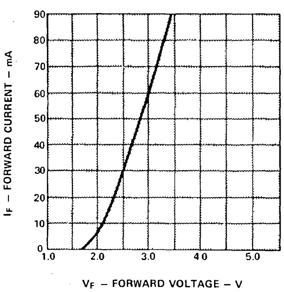


Figure 12. Forward Current vs. Forward Voltage Characteristics.

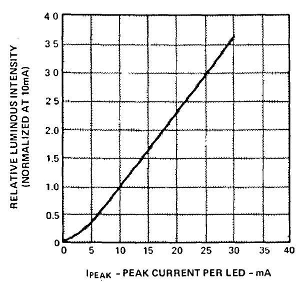


Figure 13. Relative Luminous Intensity vs. DC Forward Current.

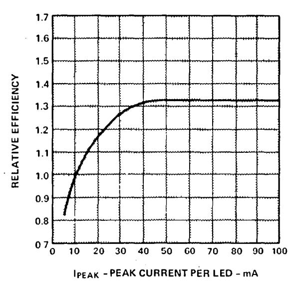


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

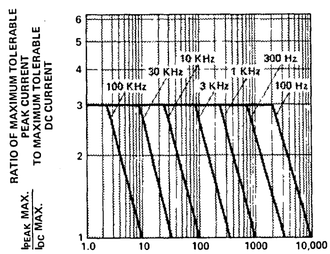


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

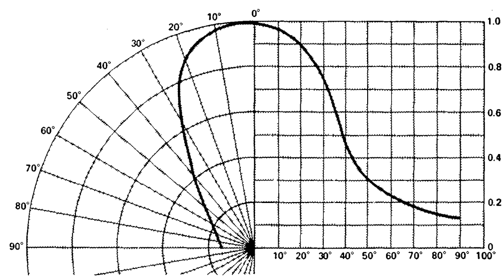


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

T-1 3/4 (5mm) LOW PROFILE SOLID STATE LAMPS

RED • HLMP-3200 SERIES
HIGH EFFICIENCY RED • HLMP-3350 SERIES
YELLOW • HLMP-3450 SERIES
HIGH PERFORMANCE GREEN • HLMP-3550 SERIES

TECHNICAL DATA JANUARY 1986

Features

- HIGH INTENSITY
- LOW PROFILE: 5.8mm (0.23 in) NOMINAL
- T-1¾ DIAMETER PACKAGE
- DIFFUSED AND NON-DIFFUSED TYPES
- GENERAL PURPOSE LEADS
- IC COMPATIBLE/LOW CURRENT REQUIREMENTS
- RELIABLE AND RUGGED

Description

The HLMP-3200 Series are Gallium Arsenide Phosphide Red Light Emitting Diodes with a red diffused lens.

The HLMP-3350 Series are Gallium Arsenide Phosphide on Gallium Phosphide High Efficiency Red Light Emitting Diodes.

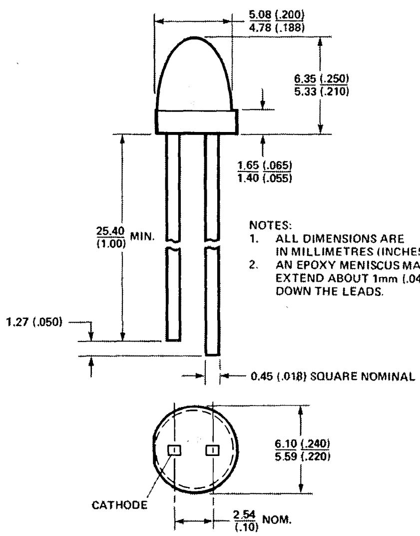
The HLMP-3450 Series are Gallium Arsenide Phosphide on Gallium Phosphide Yellow Light Emitting Diodes.

The HLMP-3550 Series are Gallium Phosphide Green Light Emitting Diodes.

The Low Profile T-1¾ package provides space savings and is excellent for backlighting applications.

Part Number HLMP-	Application	Lens	Color
3200	Indicator — General Purpose	Tinted Diffused Wide Angle	Red
3201	Indicator — High Brightness		
3350	Indicator — General Purpose	Tinted Diffused Wide Angle	High Efficiency Red
3351	Indicator — High Brightness		
3365	General Purpose Point Source	Tinted Non-diffused Narrow Angle	
3366	High Brightness Annunciator		
3450	Indicator — General Purpose	Tinted Diffused Wide Angle	Yellow
3451	Indicator — High Brightness		
3465	General Purpose Point Source	Tinted Non-diffused Narrow Angle	
3466	High Brightness Annunciator		
3553	Indicator — General Purpose	Tinted Diffused Wide Angle	Green
3554	Indicator — High Brightness		
3567	General Purpose Point Source	Tinted Non-diffused Narrow Angle	
3568	High Brightness Annunciator		

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	3200 Series	3350 Series	3450 Series	3550 Series	Units
Peak Forward Current	1000	90	60	90	mA
Average Forward Current[1]	50	25	20	25	mA
DC Current[2]	50	30	20	30	mA
Power Dissipation[3]	100	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	3	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	2000	500	500	500	mA
Operating Temperature Range Storage Temperature Range	−55 to +100	−55 to +100	−55 to +100	−20 to +100 −55 to +100	°C
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds				

NOTES:

1. See Figure 5 (Red), 10 (High Efficiency Red), 15 (Yellow) or 20 (Green) to establish pulsed operating conditions.
2. For High Efficiency Red and Green Series derate linearly from 50° C at 0.5 mA/° C. For Red and Yellow Series derate linearly from 50° C at 0.2 mA/° C.
3. For High Efficiency Red and Green Series derate power linearly from 25° C at 1.8 mW/° C. For Red and Yellow Series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak current beyond the peak forward current listed in the Absolute Maximum Ratings.

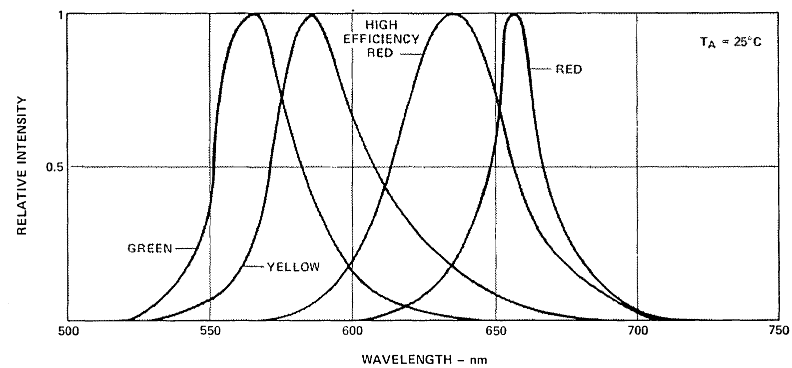


Figure 1. Relative Intensity versus Wavelength.

SOLID STATE LAMPS

RED HLMP-3200 SERIES

Electrical Specifications at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3200	1.0	2.0		mcd	$I_F = 20$ mA (Figure 3)
		3201	2.0	4.0			
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points			60		deg.	Note 1 (Figure 6)
λ_P	Peak Wavelength			655		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength			648		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			24		nm	
τ_s	Speed of Response			10		ns	
C	Capacitance			100		pF	$V_F = 0$; f = 1 MHz
θ_{JC}	Thermal Resistance			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.4	1.6	2.0	V	$I_F = 20$ mA (Fig. 2)
V_R	Reverse Breakdown Voltage		3	10		V	$I_R = 100\ \mu A$
η_V	Luminous Efficacy			65		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

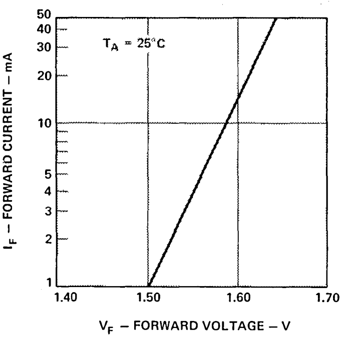


Figure 2. Forward Current versus Forward Voltage.

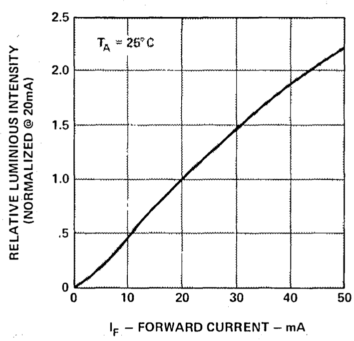


Figure 3. Relative Luminous Intensity versus Forward Current.

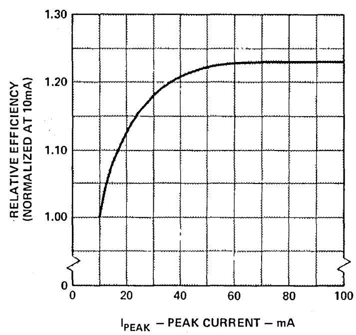


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

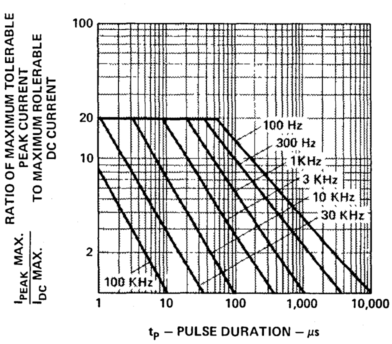


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

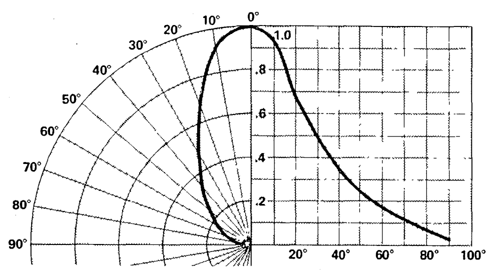


Figure 6. Relative Luminous Intensity versus Angular Displacement.

HIGH EFFICIENCY RED HLMP-3350 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3350 3351 3365 3366	2.0 5.0 7.0 12.0	3.5 7.0 10.0 18.0		mcd	I_F = 10 mA (Fig. 8)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3350 3351 3365 3366		50 50 45 45		Deg.	Note 1 (Fig. 11)
λ_P	Peak Wavelength			635		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength			626		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			40		nm	
τ_S	Speed of Response			90		ns	
C	Capacitance			16		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.5	2.2	3.0	V	I_F = 10 mA (Fig. 7)
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			145		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

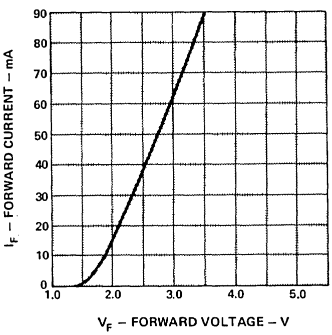


Figure 7. Forward Current versus Forward Voltage.

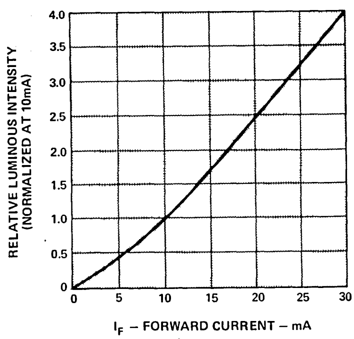


Figure 8. Relative Luminous Intensity versus Forward Current.

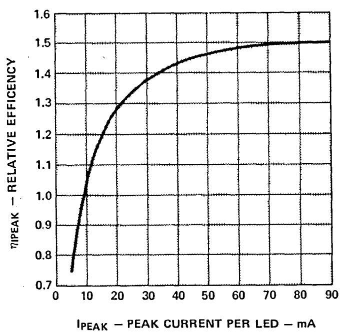


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

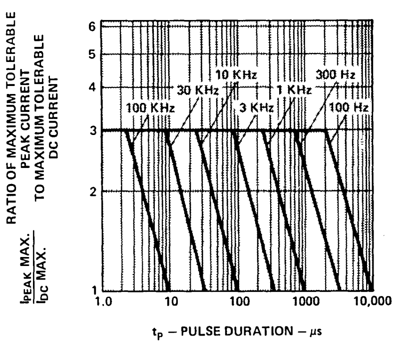


Figure 10. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

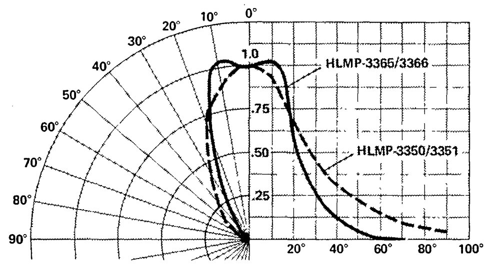


Figure 11. Relative Luminous Intensity versus Angular Displacement.

YELLOW HLMP-3450 SERIES

Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3450 3451 3465 3466	2.5 6.0 6.0 12.0	4.0 10.0 12.0 18.0		mcd	I_F = 10 mA (Fig. 13)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3450 3451 3465 3466		50 50 45 45		Deg.	Note 1 (Fig. 16)
λ_P	Peak Wavelength			583		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength			585		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			36		nm	
τ_S	Speed of Response			90		ns	
C	Capacitance			18		pF	$V_F = 0$; f = 1 MHz
θ_{JC}	Thermal Resistance			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.5	2.2	3.0	V	I_F = 10 mA (Fig. 12)
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			500		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

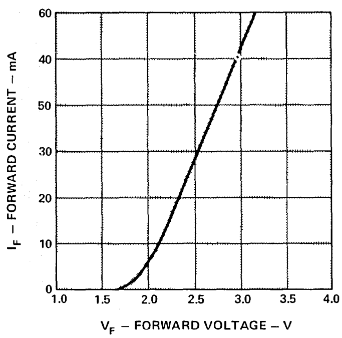


Figure 12. Forward Current versus Forward Voltage.

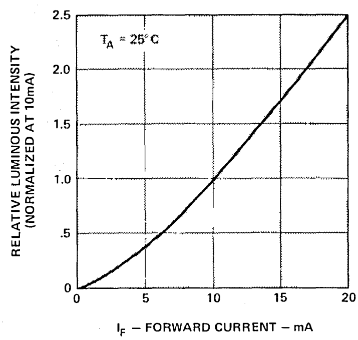


Figure 13. Relative Luminous Intensity versus Forward Current.

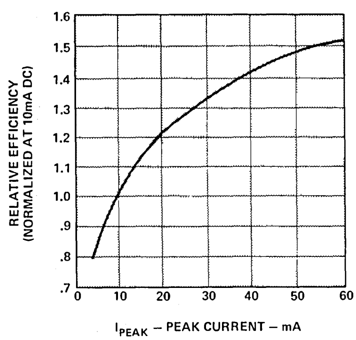


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

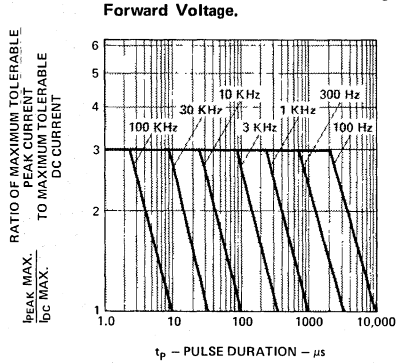


Figure 15. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings).

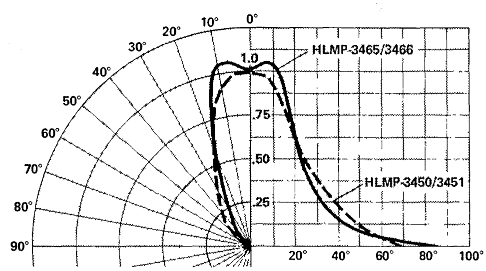


Figure 16. Relative Luminous Intensity versus Angular Displacement

GREEN HLMP-3550 SERIES

Electrical Specifications at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3553 3554 3567 3568	1.6 6.7 4.2 10.6	3.2 10.0 7.0 15.0		mcd	$I_F = 10$ mA (Fig. 18)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3553 3554 3567 3568		50 50 40 40		Deg.	Note 1 (Figure 21)
λ_P	Peak Wavelength			565		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength			569		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			28		nm	
τ_S	Speed of Response			500		ns	
C	Capacitance			18		pF	$V_F = 0$; f = 1 MHz
θ_{JC}	Thermal Resistance			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.6	2.3	3.0	V	$I_F = 10$ mA (Fig. 17)
V_R	Reverse Breakdown Voltage		5.0			V	$I_R = 100\ \mu A$
η_V	Luminous Efficacy			595		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

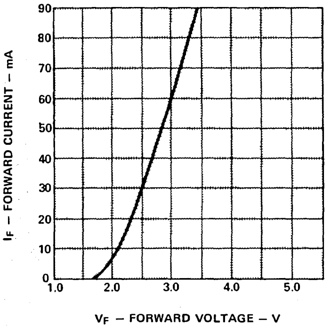


Figure 17. Forward Current versus Forward Voltage.

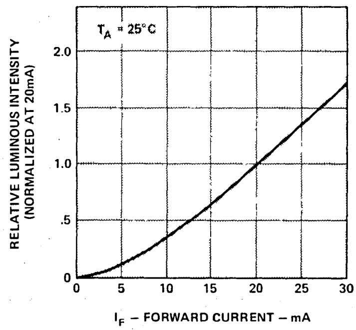


Figure 18. Relative Luminous Intensity versus Forward Current.

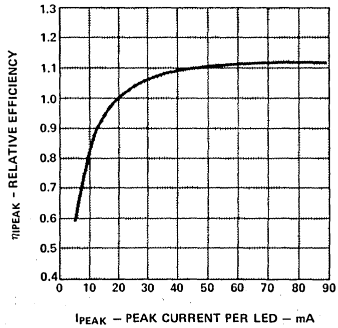


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

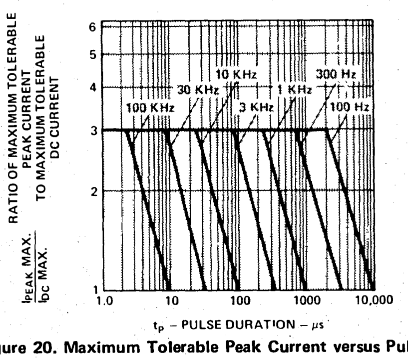


Figure 20. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX ratings).

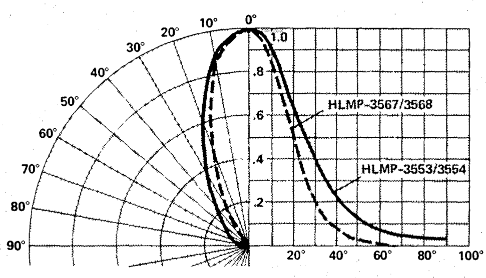


Figure 21. Relative Luminous Intensity versus Angular Displacement.

SOLID STATE LAMPS

T-1 (3mm) RED SOLID STATE LAMPS

HEWLETT PACKARD

HLMP-1000 Series
HLMP-1200 Series

TECHNICAL DATA JANUARY 1986

Features

- WIDE VIEWING ANGLE
- SMALL SIZE T-1 DIAMETER 3.18mm (0.125")
- IC COMPATIBLE
- RELIABLE AND RUGGED

Description

The HLMP-1000 is a series of Gallium Arsenide Phosphide Light Emitting Diodes designed for applications where space is at a premium, such as in high density arrays.

The HLMP-1000 series is available in three lens configurations.

HLMP-1000 — Red Diffused lens provides excellent on-off contrast ratio, high axial luminous intensity, and wide viewing angle.

HLMP-1080 — Same as HLMP-1000, but untinted diffused to mask red color in the "off" condition.

HLMP-1071/-1201 — Untinted non-diffused plastic lens provides a point source. Useful when illuminating external lens, annunciators, or photo-detectors.

Part Number HLMP-	Package & Lens Type	Iv (mcd) @ 20 mA		Typ. Viewing Angle 2Θ 1/2
		Min.	Typ.	
-1000	A-Tinted Diffused	.5	1.0	125°
-1002	A-Tinted Diffused	1.5	2.5	125°
-1080	A-Untinted Diffused	.5	1.5	125°
-1071	A-Untinted Non-Diffused	1.0	2.0	80°
-1200	B-Untinted Non-Diffused	.5	1.0	120°
-1201	B-Untinted Non-Diffused	1.5	2.5	120°

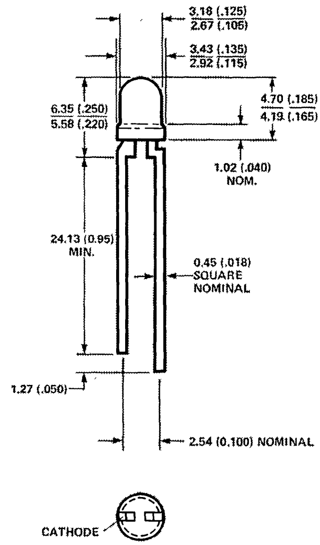


Figure A.

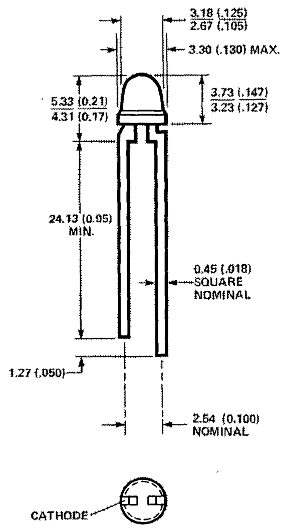


Figure B.

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

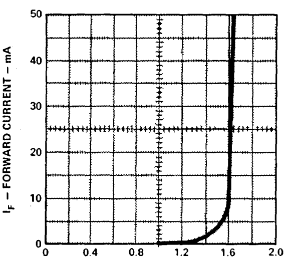
Absolute Maximum Ratings at $T_A = 25°C$

Parameter	1000 Series	Units
Power Dissipation	100	mW
DC Forward Current [1]	50	mA
Average Forward Current	50	mA
Peak Operating Forward Current	1000	mA
Reverse Voltage ($I_R = 100\ \mu A$)	3	V
Transient Forward Current[1] (10 μsec Pulse)	2000	mA
Operating and Storage Temperature Range	–55° C to +100° C	
Lead Solder Temperature (1.6 mm [0.063 inch] below package base)	260° C for 5 seconds	

Note:
1. Derate linerarly from 50°C at 0.2 mA/°C.

Electrical Characteristics at $T_A = 25°C$

Symbol	Parameters	Min.	Typ.	Max.	Units	Test Conditions
λ_P	Peak Wavelength		655		nm	Measurement at Peak
λ_d	Dominant Wavelength		648		nm	
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		24		nm	
τ_s	Speed of Response		10		ns	
C	Capacitance		100		pF	$V_F = 0$, f = 1 MHz
θ_{JC}	Thermal Resistance		120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	1.4	1.6	2.0	V	$I_F = 20$ mA
V_R	Reverse Breakdown Voltage	3	10		V	$I_R = 100\ \mu A$



FORWARD CURRENT – VOLTAGE CHARACTERISTICS

Figure 1. Forward Current vs. Voltage Characteristic.

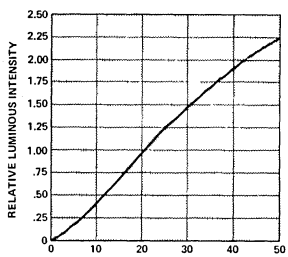


Figure 2. Luminous Intensity vs. Forward Current (IF).

HLMP-1200/-1201

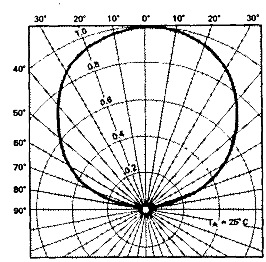


Figure 3. Typical Relative Luminous Intensity vs. Angular Displacement.

HLMP-1000/-1002/-1080

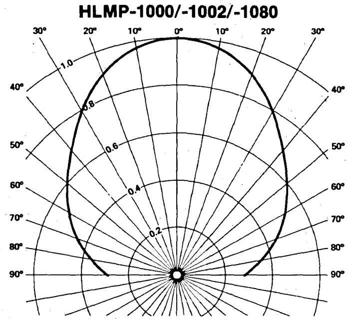


Figure 4. Relative Luminous Intensity vs. Angular Displacement.

HLMP-1071

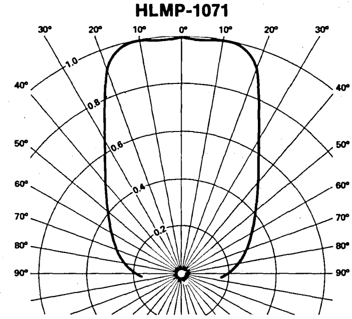


Figure 5. Relative Luminous Intensity vs. Angular Displacement.

T-1 (3mm) DIFFUSED SOLID STATE LAMPS

HIGH EFFICIENCY RED • HLMP-1300 SERIES
ORANGE • HLMP-K400 SERIES
YELLOW • HLMP-1400 SERIES
HIGH PERFORMANCE GREEN • HLMP-1500 SERIES
EMERALD GREEN • HLMP-K600 SERIES

HEWLETT PACKARD

TECHNICAL DATA JANUARY 1986

Features

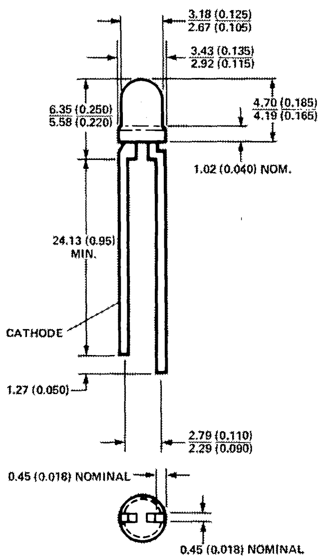
- **HIGH INTENSITY**
- **CHOICE OF 5 BRIGHT COLORS**
  - **High Efficiency Red**
  - **Orange**
  - **Yellow**
  - **High Performance Green**
  - **Emerald Green**
- **POPULAR T-1 DIAMETER PACKAGE**
- **SELECTED MINIMUM INTENSITIES**
- **WIDE VIEWING ANGLE**
- **GENERAL PURPOSE LEADS**
- **RELIABLE AND RUGGED**
- **AVAILABLE ON TAPE AND REEL**

Description

This family of T-1 lamps is widely used in general purpose indicator applications. Diffusants, tints, and optical design are balanced to yield superior light output and wide viewing angles. Several intensity choices are available in each color for increased design flexibility.

Part Number HLMP-	Application	Minimum Intensity (mcd) at 10mA	Color (Material)
1300	General Purpose	1.0	High Efficiency Red (GaAsP on GaP)
1301	General Purpose	2.0	
1302	High Ambient	3.0	
1385	Premium Lamp	6.0	
K400	General Purpose	1.0	Orange (GaAsP on GaP)
K401	High Ambient	2.0	
K402	Premium Lamp	3.0	
1400	General Purpose	1.0	Yellow (GaAsP on GaP)
1401	General Purpose	2.0	
1402	High Ambient	3.0	
1485	Premium Lamp	6.0	
1503	General Purpose	1.0	Green (GaP) 565 nm
1523	High Ambient	2.6	
1585	Premium Lamp	4.0	
K600	General Purpose	1.0	Emerald Green (GaP) 555 nm
K601	High Ambient	2.0	

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (0.040") DOWN THE LEADS.

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	High Efficiency Red				mcd	$I_F = 10$ mA
		1300	1.0	2.0			
		1301	2.0	2.5			
		1302	3.0	4.0			
		1385	6.0	10.0			
		Orange					
		K400	1.0	2.0			
		K401	2.0	2.5			
		K402	3.0	4.0			
		Yellow					
		1400	1.0	2.0			
		1401	2.0	3.0			
		1402	3.0	4.0			
		1485	6.0	10.0			
		Green					
		1503	1.0	2.0			
		1523	2.5	4.0			
		1585	4.0	6.0			
		Emerald Green					
		K600	1.0	2.0			
		K601	2.0	2.5			
$2\Theta 1/2$	Including Angle Between Half Luminous Intensity Points	All		60		Deg.	$I_F = 10$ mA See Note 1
λ_{PEAK}	Peak Wavelength	High Efficiency Red Orange Yellow Green Emerald Green		635 612 583 565 555		nm	Measurement at Peak
λ_d	Dominant Wavelength	High Efficiency Red Orange Yellow Green Emerald Green		626 608 585 569 556		nm	See Note 2
τ_S	Speed of Response	High Efficiency Red Orange Yellow Green Emerald Green		90 280 90 500 4000		ns	
C	Capacitance	High Efficiency Red Orange Yellow Green Emerald Green		16 4 18 18 35		pF	$V_F = 0$; f = 1 MHz
θ_{JC}	Thermal Resistance	All		120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	HER/Orange Yellow Grn/Emerald Grn	1.5 1.5 1.6	2.2 2.2 2.3	3.0 3.0 3.0	V	$I_F = 10$ mA
V_R	Reverse Breakdown Volt.	All	5.0			V	$I_R = 100\ \mu A$
η_V	Luminous Efficacy	High Efficiency Red Orange Yellow Green Emerald Green		145 262 500 595 656		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3

NOTES:
1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

SOLID STATE LAMPS

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	HER/Orange	Yellow	Grn/Emerald Grn	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range			-55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:

1. See Figure 5 (Red/Orange), 10 (Yellow) or 15 (Green/Emerald Green) to establish pulsed operating conditions.
2. For Red, Orange, Emerald Green, and Green series derate linearly from 50°C at 0.5 mA/°C. For Yellow series derate linearly from 50°C at 0.2 mA/°C.
3. For Red, Orange, Emerald Green, and Green series derate power linearly from 25°C at 1.8 mW/°C. For Yellow series derate power linearly from 50°C at 1.6 mW/°C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

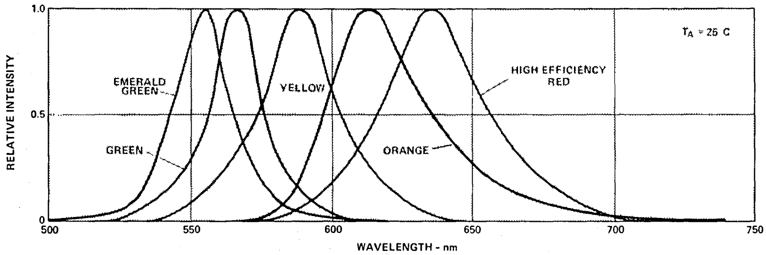


Figure 1. Relative Intensity vs. Wavelength

T-1 High Efficiency Red, Orange Diffused Lamps

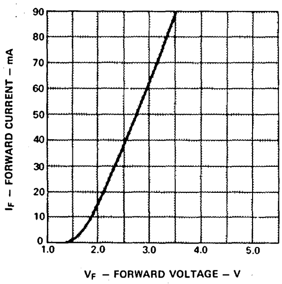


Figure 2. Forward Current vs. Forward Voltage Characteristics.

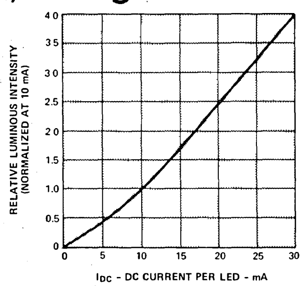


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

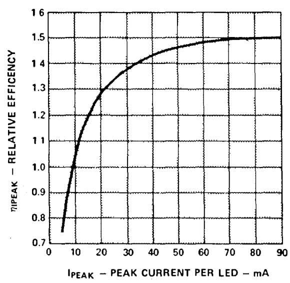


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

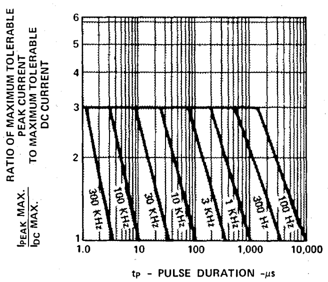


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

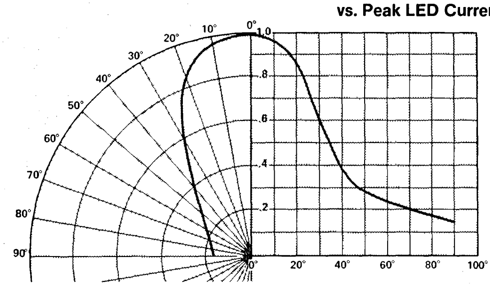


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

T-1 Yellow Diffused Lamps

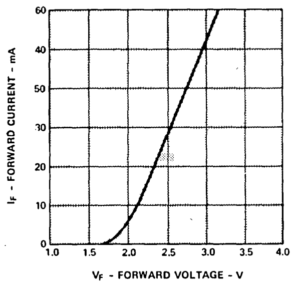


Figure 7. Forward Current vs. Forward Voltage Characteristics.

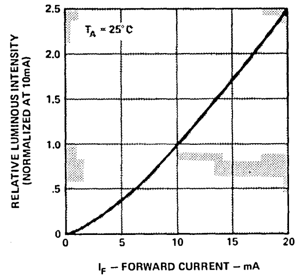


Figure 8. Relative Luminous Intensity vs. Forward Current.

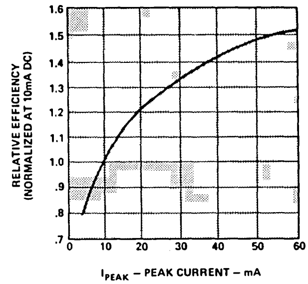


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

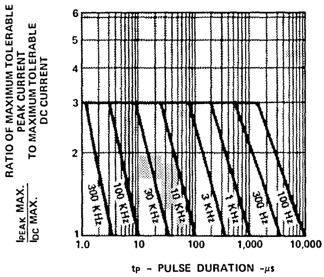


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

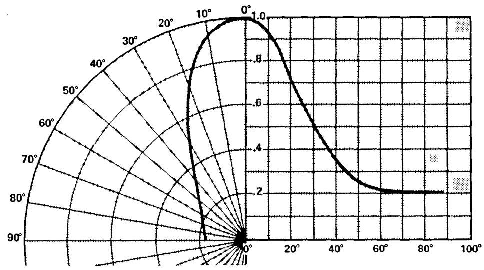


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

T-1 Green, Emerald Green Diffused Lamps

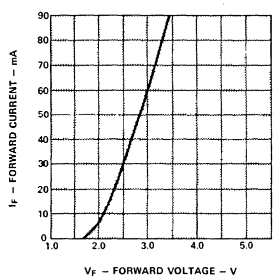


Figure 12. Forward Current vs. Forward Voltage Characteristics.

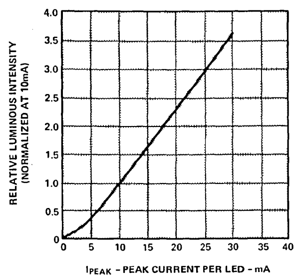


Figure 13. Relative Luminous Intensity vs. Forward Current.

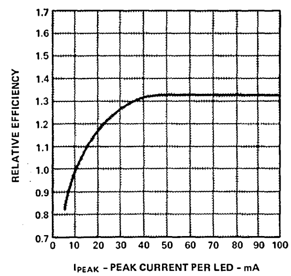


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

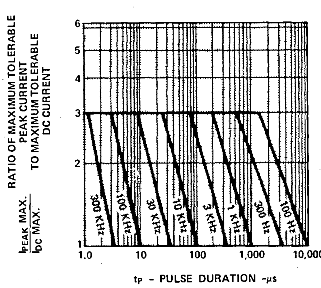


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

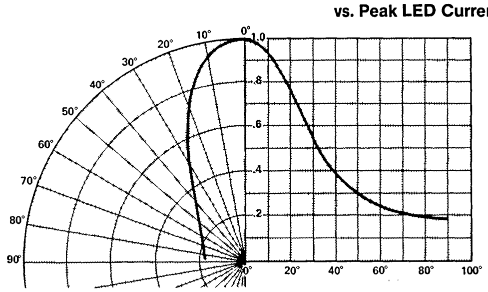


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

LOW PROFILE T-1 (3mm) LED LAMPS

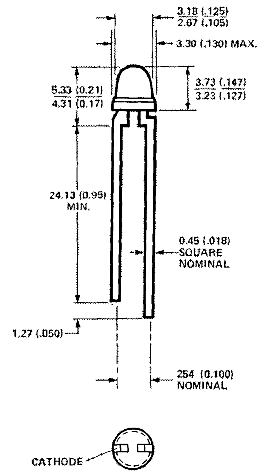
High Efficiency Red HLMP-1350
Yellow HLMP-1450
High Performance Green HLMP-1550

TECHNICAL DATA JANUARY 1986

Features

- LOW PROFILE HEIGHT
- SMALL T-1 SIZE DIAMETER 3.18 mm (.125 inch)
- HIGH INTENSITY
- IC COMPATIBLE
- CHOICE OF 3 BRIGHT COLORS
  High Efficiency Red
  Yellow
  High Performance Green

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Description

This family of solid state lamps is especially suited for applications where small package size is required without sacrificing luminous intensity. The HLMP-1350 is a red tinted, diffused lamp providing a wide viewing angle. The HLMP-1450 and HLMP-1550 are similar products in yellow and green respectively.

Axial Luminous Intensity and Viewing Angle @ 25°C

Part Number HLMP-	Description	I_V (mcd)		Test Condition mA	$2\Theta_{1/2}$ (Typ.) [1]	λ_d (nm-Typ.) [2]	Color
		Min.	Typ.				
1350	Tinted, Wide Angle	1.0	2.0	10	55°	626	High Efficiency Red
1450	Tinted, Wide Angle	1.0	2.0	10	55°	585	Yellow
1550	Tinted, Wide Angle	1.0	2.0	10	55°	569	Green

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

For Maximum Ratings and Electrical/Optical Characteristics (including figures) see HLMP-1300/-1400/-1500 data sheet, publication number 5953-7735, except for Figure A shown here.

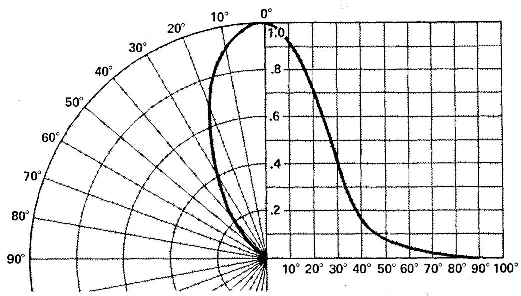


Figure A. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

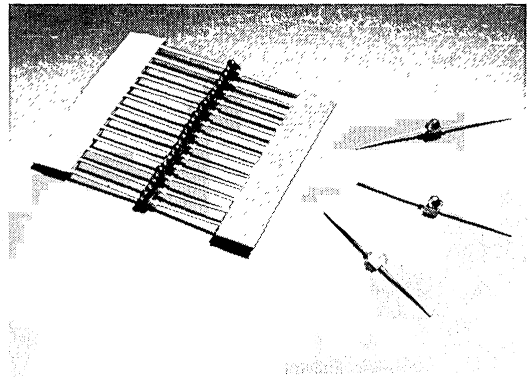
SUBMINIATURE SOLID STATE LAMPS

RED • HLMP-6000/6001
HIGH EFFICIENCY RED • HLMP-6300
ORANGE • HLMP-Q400
YELLOW • HLMP-6400
HIGH PERFORMANCE GREEN • HLMP-6500
EMERALD GREEN • HLMP-Q600

TECHNICAL DATA JANUARY 1986

Features

- SUBMINIATURE PACKAGE STYLE
- END STACKABLE
- LOW PACKAGE PROFILE
- AXIAL LEADS
- WIDE VIEWING ANGLE
- LONG LIFE — SOLID STATE RELIABILITY
- AVAILABLE IN BULK OR ON TAPE AND REEL



Description

Lamps in this series of solid state indicators are encapsulated in an axial lead subminiature package of molded epoxy. They utilize a tinted, diffused lens providing high on-off contrast and wide angle viewing. Small size makes these lamps suitable for PC board mounting in space sensitive applications.

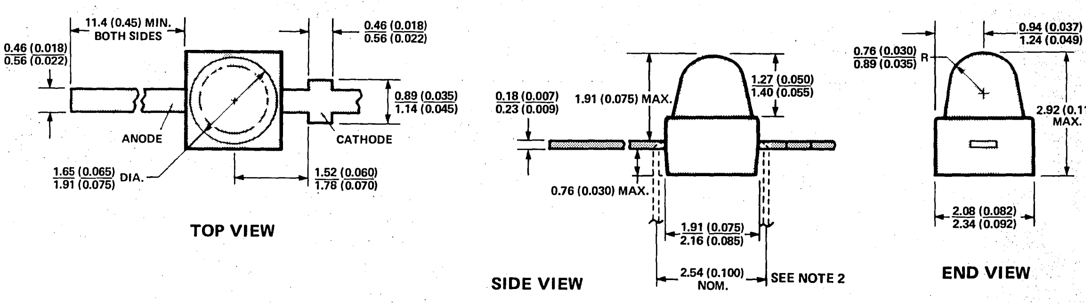
Special lead bending, packaging and assembly methods can be used with these devices. For example, lead bending on 2.54mm (0.100 in) and 5.08mm (0.200 in) centers is available. Two special surface mount lead configurations are also available. See the data sheets for "gull wing" and "yoke lead" options for more detailed information.

Tape and reel packaging for the standard product is described in this data sheet. Similar packaging for the surface mountable "gull wing" and "yoke lead" versions is described in the respective surface mount data sheets.

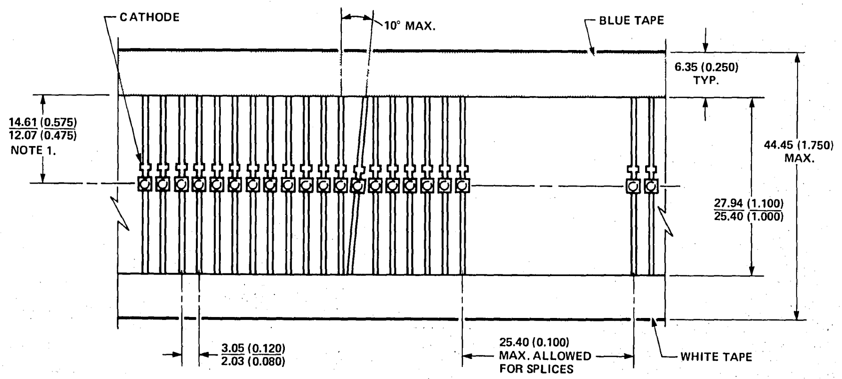
Part Number HLMP-	Tape and Reel Part Number HLMP-	Minimum Intensity (mcd) at 10mA	Color (Material)
6000	6020	0.5	Standard Red (GaAsP)
6001	6021	1.3	Standard Red (GaAsP)
6300	6320	1.0	High Efficiency Red (GaP on GaAsP)
Q400	Q420	1.0	Orange (GaP on GaAsP)
6400	6420	1.0	Yellow (GaP on GaAsP)
6500	6520	1.0	Green (GaP)
Q600	Q620	1.0	Emerald Green (GaP) 555 nm

Package Dimensions

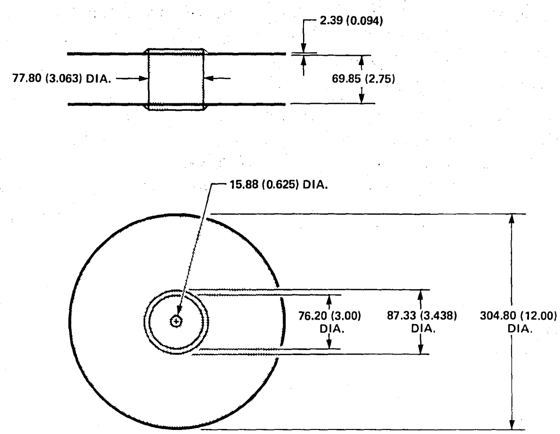
OUTLINE A (SINGLE LED)



OUTLINE B (TAPE AND REEL)



NOTES:
1. LED'S MUST FALL WITHIN ± 0.031" OF A COMMON CENTER.
2. OPTIONAL LEAD FORM IS AVAILABLE.



ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).
ALL DIMENSIONS ARE TYPICAL VALUES.

Electrical Characteristics at $T_A = 25°C$

Symbol	Parameter	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	Standard Red 6000 6001	 0.5 1.3	 1.2 3.2		mcd	$I_F = 10$ mA (Figures 3, 8, 13, 18)
		High Efficiency Red 6300	1.0	3.0			
		Orange Q400	1.0	3.0			
		Yellow 6400	1.0	3.0			
		Green 6500	1.0	3.0			
		Emerald Green Q600	1.0	2.5			
$2\Theta 1/2$	Including Angle Between Half Luminous Intensity Points	All		90		Deg.	See Note 1 (Figures 6, 11, 16, 21)
λ_{PEAK}	Peak Wavelength	Standard Red High Efficiency Red Orange Yellow Green Emerald Green		655 635 612 583 565 555		nm	Measurement at Peak
λd	Dominant Wavelength	Standard Red High Efficiency Red Orange Yellow Green Emerald Green		640 626 608 585 569 556		nm	See Note 2
τ_S	Speed of Response	Standard Red High Efficiency Red Orange Yellow Green Emerald Green		15 90 260 90 500 4000		ns	
C	Capacitance	Standard Red High Efficiency Red Orange Yellow Green Emerald Green		100 11 4 15 18 35		pF	$V_F = 0$; f = 1 MHz
θ_{JC}	Thermal Resistance	All		120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	Standard Red High Efficiency Red Orange Yellow Green Emerald Green	1.4 1.5 1.5 1.5 1.5 1.5	1.6 2.2 2.2 2.2 2.3 2.2	2.0 3.0 3.0 3.0 3.0 3.0	V	$I_F = 10$ mA (Figures 2, 7, 12, 17)
V_R	Reverse Breakdown Voltage	All	5.0			V	$I_R = 100\ \mu A$
η_V	Luminous Efficacy	Standard Red High Efficiency Red Orange Yellow Green Emerald Green		65 145 262 500 595 656		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3

Notes on following page.

SOLID STATE LAMPS

NOTES:

1. Θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$. Where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Red HLMP-6000/1	High Eff. Red HLMP-6300	Orange HLMP-Q400	Yellow HLMP-6400	Green HLMP-6500	Emerald Green HLMP-Q600	Units
Power Dissipation	100	135	135	85	135	135	mW
DC Forward Current	50[1]	30[2]	30[2]	20[1]	30[2]	30[2]	mA
Peak Forward Current	1000 See Fig. 5	90 See Fig. 10	90 See Fig. 10	60 See Fig. 15	90 See Fig. 20	90 See Fig. 20	mA
Reverse Voltage (I_R = 100 μA)	3	5	5	5	5	5	V
Transient Forward Current[3] (10 μsec Pulse)	2000	500	500	500	500	500	mA
Operating Temperature Range	–55 to +100	–55 to +100	–55 to +100	–55 to +100	–20 to +100	–20 to +100	°C
Storage Temperature Range					–55 to +100	–55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 3 seconds						

NOTES:

1. Derate from 50° C at 0.2 mA/° C.
2. Derate from 50° C at 0.5 mA/° C.
3. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak current beyond the peak forward current listed in the Absolute Maximum Ratings.

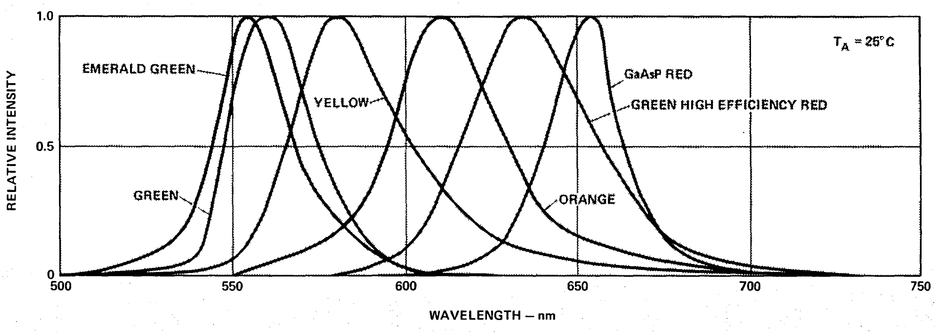


Figure 1. Relative Intensity vs. Wavelength

Standard Red HLMP-6000/6001

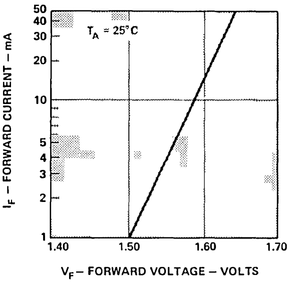


Figure 2. Forward Current vs. Forward Voltage.

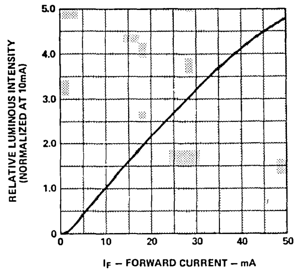


Figure 3. Relative Luminous Intensity vs. Forward Current.

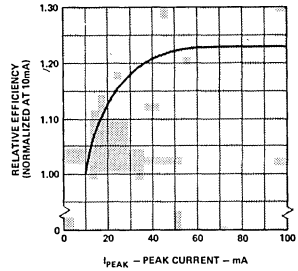


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

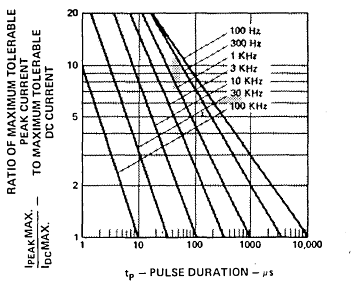


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

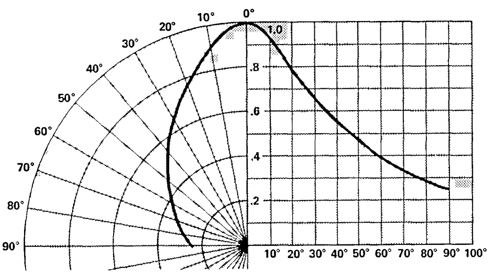


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

High Efficiency Red HLMP-6300, Orange HLMP-Q400

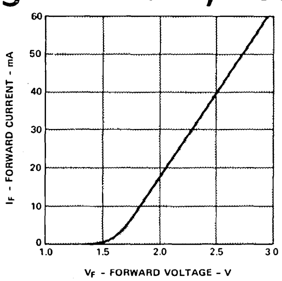


Figure 7. Forward Current vs. Forward Voltage Characteristics

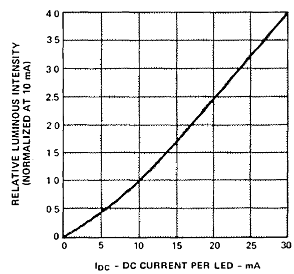


Figure 8. Relative Luminous Intensity vs. Forward Current.

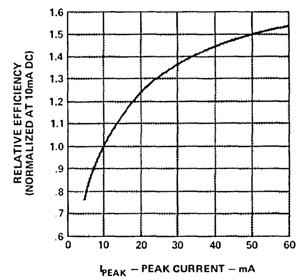


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

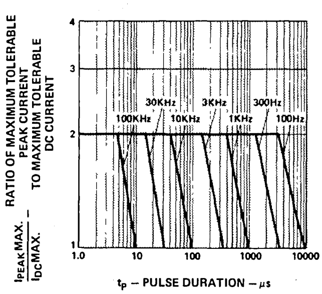


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

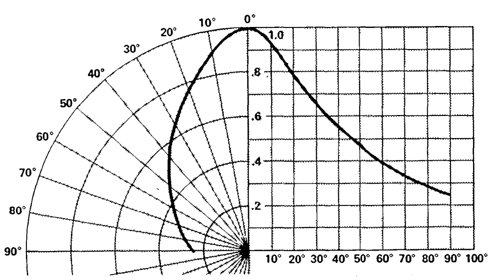


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Yellow HLMP-6400

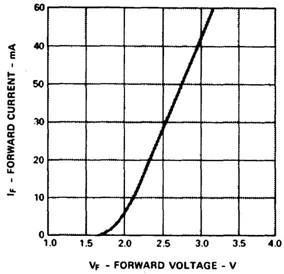


Figure 12. Forward Current vs. Forward Voltage Characteristics

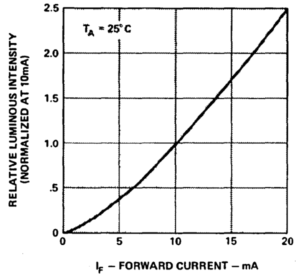


Figure 13. Relative Luminous Intensity vs. Forward Current.

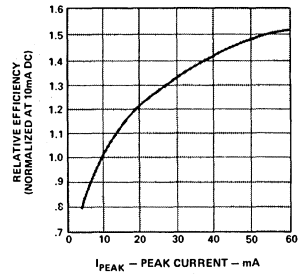


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

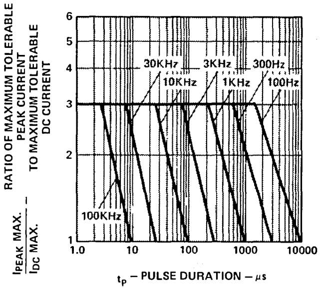


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

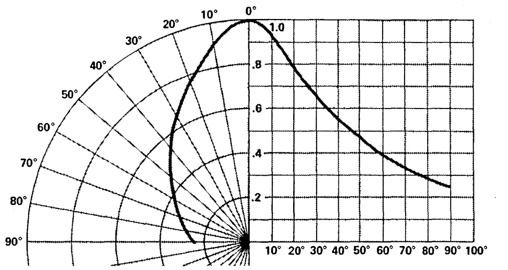


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Green HLMP-6500, Emerald Green HLMP-Q600

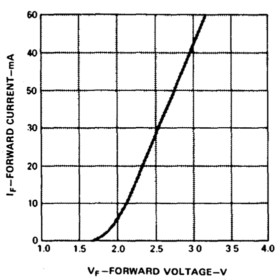


Figure 17. Forward Current vs. Forward Voltage.

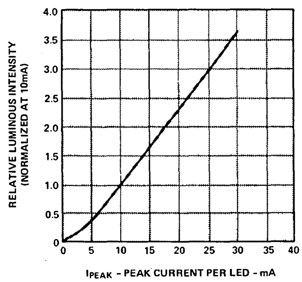


Figure 18. Relative Luminous Intensity vs. DC Forward Current

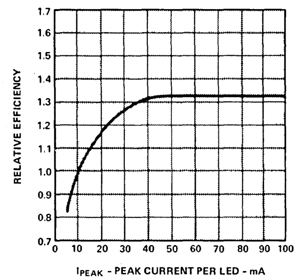


Figure 19. Relatiave Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

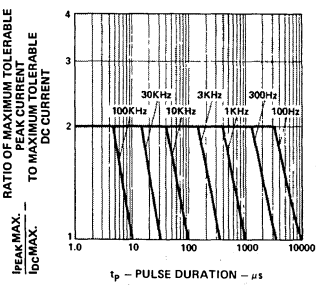


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

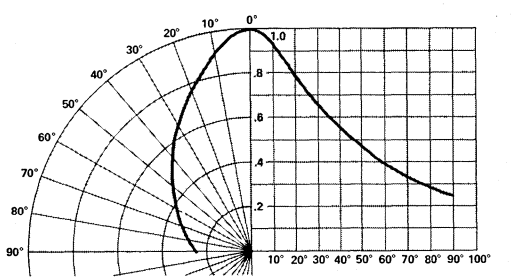


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

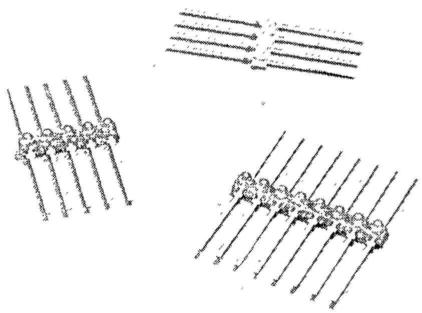
MATCHED ARRAYS OF SUBMINIATURE LAMPS

RED HLMP-6200 SERIES
HIGH EFFICIENCY RED HLMP-6650 SERIES
YELLOW HLMP-6750 SERIES
GREEN HLMP-6850 SERIES

TECHNICAL DATA JANUARY 1986

Features

- IMPROVED BRIGHTNESS
- AVAILABLE IN 4 BRIGHT COLORS
  Red
  High Efficiency Red
  Yellow
  High Performance Green
- EXCELLENT UNIFORMITY BETWEEN ELEMENTS
- END STACKABLE FOR LONGER ARRAYS
- SELECTION OF VARIOUS LENGTHS
- COMPACT SUBMINIATURE PACKAGE STYLE
- NO CROSSTALK BETWEEN ELEMENTS



Description

The HLMP-6XXX Series Arrays are comprised of several subminiature lamps molded as a single bar. Arrays are tested to assure 2.1 to 1 matching between elements and intensity binned for matching between arrays.

The HLMP-620X Series Arrays are Gallium Arsenide Phosphide red light emitting diodes. The HLMP-665X, HLMP-675X series arrays are Gallium Arsenide Phosphide on Gallium Phosphide red and yellow light emitting diodes. The HLMP-685X series arrays are Gallium Phosphide green light emitting diodes.

Each element has separately accessible leads and a diffused lens which provides a wide viewing angle and a high on/off contrast ratio. The center-to-center spacing is 2.54 mm (.100 in.) between elements. Special lead bending is available on 2.54 mm (.100 in.) and 5.08 mm (.200 in.) centers.

Array Length	Red	High Efficiency Red	Yellow	High Performance Green
3-Element HLMP-	6203	6653	6753	6853
4-Element HLMP-	6204	6654	6754	6854
5-Element HLMP-	6205	6655	6755	6855
6-Element HLMP-	6206	6656	6756	6856
8-Element HLMP-	6208	6658	6758	6858

Applications

- INDUSTRIAL CONTROLS
- POSITION INDICATORS
- OFFICE EQUIPMENT
- INSTRUMENTATION LOGIC INDICATORS
- CONSUMER PRODUCTS

Axial Luminous Intensity and Viewing Angle at 25°C

Part Number	Number of Elements	Color	I_V per Element (mcd) @ 10 mA DC Min.	Typ.	$2\Theta 1/2$ Note 1.
HLMP-620X	X = 3,4, 5,6,8	Red	.5	1.2	90°
HLMP-665X	X = 3,4 5,6,8	High Efficiency Red	1.0	3.0	90°
HLMP-675X	X = 3,4 5,6,8	Yellow	1.0	3.0	90°
HLMP-685X	X = 3,4 5,6,8	Green	1.0	3.0	90°

NOTE:

1. $\Theta 1/2$ is the off-axis angle at which the Luminous Intensity is half the axial luminous intensity.

SOLID STATE LAMPS

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Red	High Efficiency Red	Yellow	Green	Units
Peak Forward Current	1000	90	60	90	mA
DC Current	50[1]	30[2]	20[1]	30[2]	mA
Power Dissipation	100	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	3	5	5	5	V
Transient Forward Voltage (10 μsec Pulse)	2000[3]	500[3]	500[3]	500[3]	mA
Operating Temperature Range	–55 to +100	–55 to +100	–55 to +100	–20 to +100	°C
Storage Temperature Range				–55 to +100	
Lead Soldering Temperature 1.6 mm [(0.063 in.) from body]	260° C for 3 seconds				

NOTES: 1. Derate from 50° C at 0.2 mA/° C. 2. Derate from 50° C at 0.5 mA/° C.
3. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

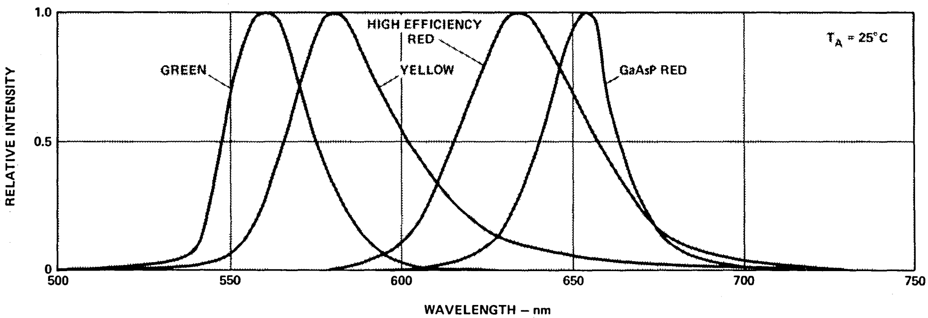


Figure 1. Relative Intensity vs. Wavelength.

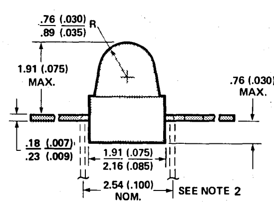
Electrical/Optical Characteristics at T_A=25°C

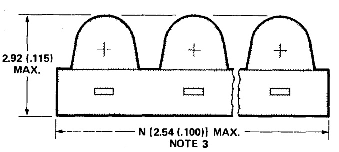
Symbol	Description	HLMP-62XX			HLMP-665X			HLMP-675X			HLMP-685X			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
λ_P	Peak Wavelength		655			635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		648			626			585			569		nm	Note 1
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		24			40			36			28		nm	
τ_s	Speed of Response		10			90			90			500		ns	
C	Capacitance		100			16			18			18		pF	V_F = 0; f = 1 MHz
Θ_{JC}	Thermal Resistance		120			120			120			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	1.4	1.6	2.0	1.5	2.2	3.0	1.5	2.2	3.0	1.5	2.3	3.0	V	I_F = 10 mA, Figures 2, 7, 12, 17
V_R	Reverse Breakdown Voltage	3.0	10		5.0			5.0			5.0			V	I_R = 100 μA
η_V	Luminous Efficacy		65			145			500			595		lm/W	Note 2

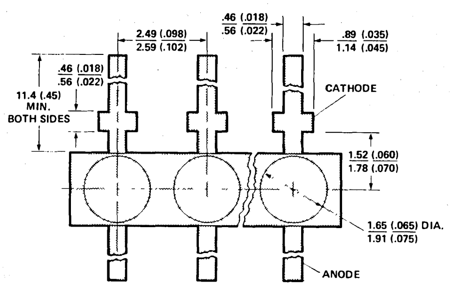
NOTES:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

Package Dimensions

Notes:
1. All dimensions are in millimetres (inches).
2. Optional lead form available.
3. Overall length is the number of elements times 2.54mm (.100 in.).







Red HLMP-62XX Series

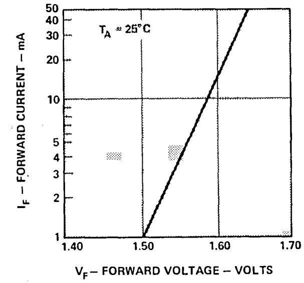


Figure 2. Forward Current vs. Forward Voltage.

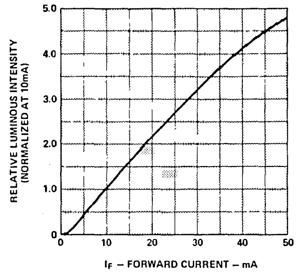


Figure 3. Relative Luminous Intensity vs. Forward Current.

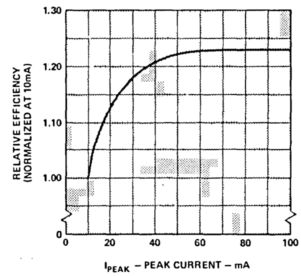


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

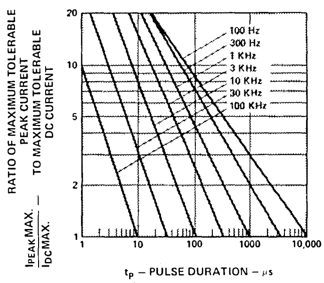


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

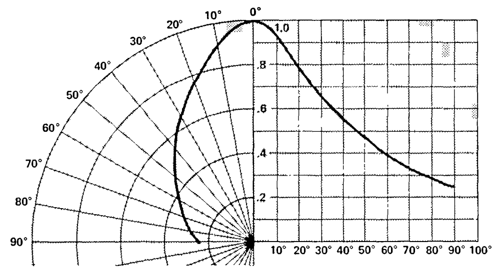


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

High Efficiency Red HLMP-665X Series

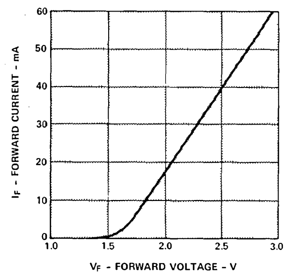


Figure 7. Forward Current vs. Forward Voltage.

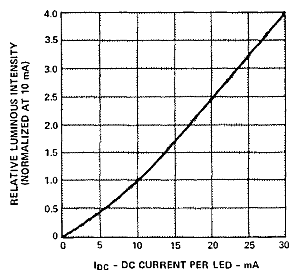


Figure 8. Relative Luminous Intensity vs. DC Forward Current.

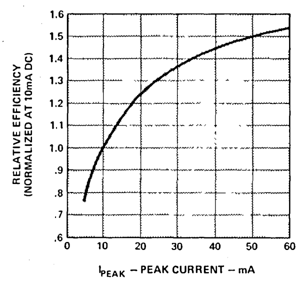


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

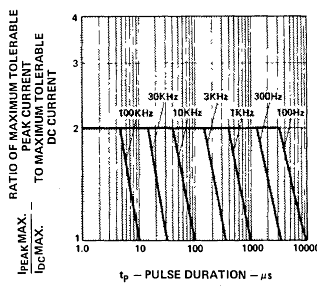


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

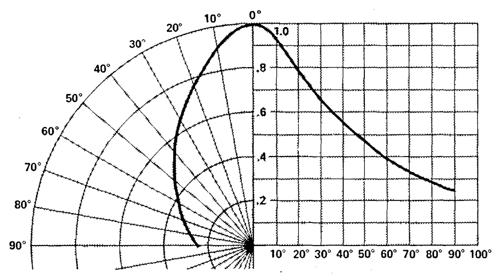


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

SOLID STATE LAMPS

Yellow HLMP-675X Series

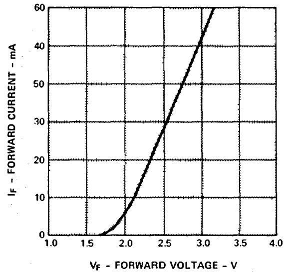


Figure 12. Forward Current vs. Forward Voltage.

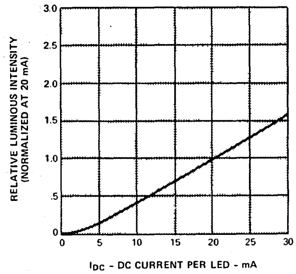


Figure 13. Relative Luminous Intensity vs. DC Forward Current.

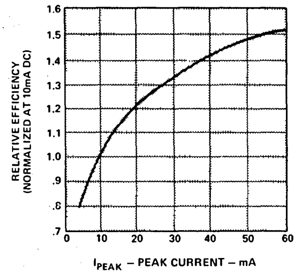


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

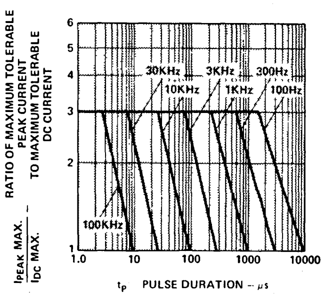


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

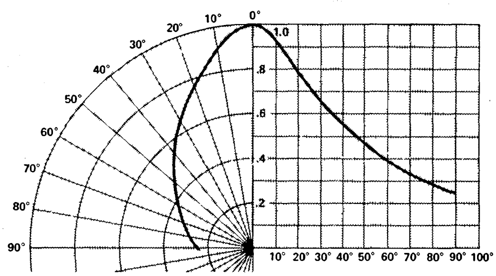


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Green HLMP-685X Series

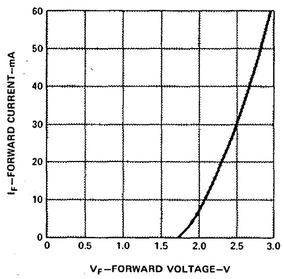


Figure 17. Forward Current vs. Forward Voltage.

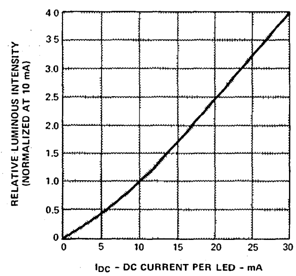


Figure 18. Relative Luminous Intensity vs. DC Forward Current.

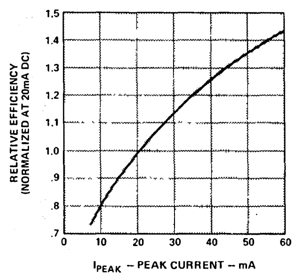


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

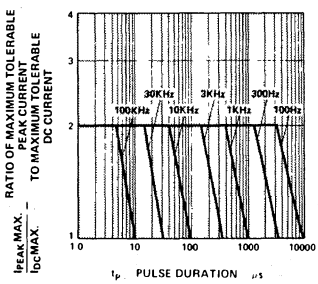


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

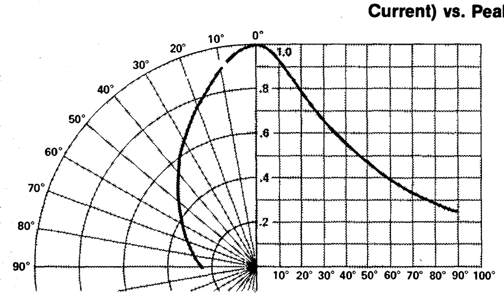


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

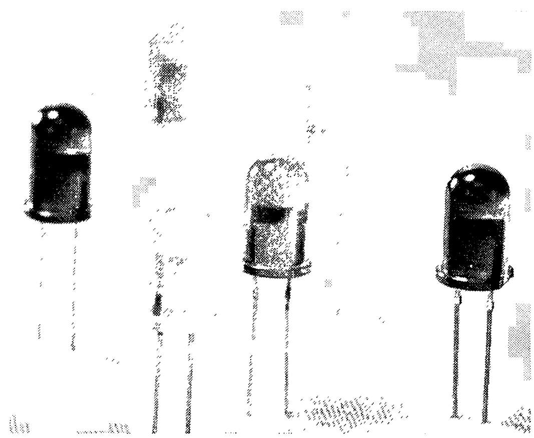
T-1 3/4 (5 mm) HIGH INTENSITY SOLID STATE LAMPS

HIGH EFFICIENCY RED • HLMP-331X SERIES
YELLOW • HLMP-341X SERIES
HIGH PERFORMANCE GREEN • HLMP-351X SERIES

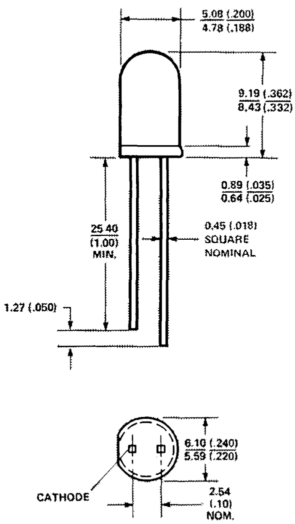
TECHNICAL DATA JANUARY 1986

Features

- **HIGH INTENSITY**
- **CHOICE OF 3 BRIGHT COLORS**
  - **High Efficiency Red**
  - **Yellow**
  - **High Performance Green**
- **POPULAR T-1 3/4 DIAMETER PACKAGE**
- **SELECTED MINIMUM INTENSITIES**
- **NARROW VIEWING ANGLE**
- **GENERAL PURPOSE LEADS**
- **RELIABLE AND RUGGED**
- **AVAILABLE ON TAPE AND REEL**



Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Description

This family of T-1 3/4 lamps is specially designed for applications requiring higher on-axis intensity than is achievable with a standard lamp. The light generated is focused to a narrow beam to achieve this effect.

Part Number HLMP-	Description	Minimum Intensity (mcd) at 10 mA	Color (Material)
3315	Illuminator/Point Source	12	High Efficiency Red (GaAsP on GaP)
3316	Illuminator/High Brightness	20	
3415	Illuminator/Point Source	10	Yellow (GaAsP on GaP)
3416	Illuminator/High Brightness	20	
3517	Illuminator/Point Source	6.7	Green (GaP)
3519	Illuminator/High Brightness	10.6	

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	3315 3316	12.0 20.0	18.0 30.0		mcd	I_F = 10 mA (Figure 3)
		3415 3416	10.0 20.0	18.0 30.0		mcd	I_F = 10 mA (Figure 8)
		3517 3519	6.7 10.6	10.0 25.0		mcd	I_F = 10 mA (Figure 3)
$2\Theta 1/2$	Including Angle Between Half Luminous Intensity Points	3315 3316		35 35		Deg.	I_F = 10 mA See Note 1 (Figure 6)
		3415 3416		35 35		Deg.	I_F = 10 mA See Note 1 (Figure 11)
		3517 3519		24 24		Deg.	I_F = 10 mA See Note 1 (Figure 16)
λ_{PEAK}	Peak Wavelength	331X 341X 351X		635 583 565		nm	Measurement at Peak (Figure 1)
λ_d	Dominant Wavelength	331X 341X 351X		626 585 569		nm	See Note 2 (Figure 1)
τ_S	Speed of Response	331X 341X 351X		90 90 500		ns	
C	Capacitance	331X 341X 351X		16 18 18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance	331X 341X 351X		120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	331X 341X 351X	1.5 1.5 1.6	2.2 2.2 2.3	3.0 3.0 3.0	V	I_F = 10 mA (Figure 2) I_F = 10 mA (Figure 7) I_F = 10 mA (Figure 12)
V_{BR}	Reverse Breakdown Volt.	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	331X 341X 351X		145 500 595		lumens Watt	See Note 3

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	331X Series	341X Series	351X Series	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	–55 to +100	–55 to +100	–20 to +100	°C
Storage Temperature Range			–55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:

1. See Figure 5 (Red), 10 (Yellow), or 15 (Green) to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

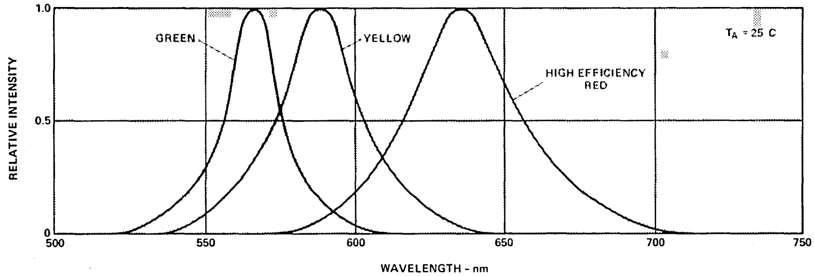


Figure 1. Relative Intensity vs. Wavelength

High Efficiency Red HLMP-331X Series

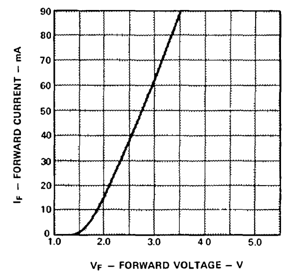


Figure 2. Forward Current vs. Forward Voltage Characteristics

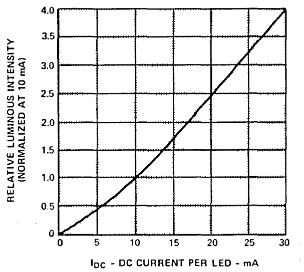


Figure 3. Relative Luminous Intensity vs. DC Forward Current

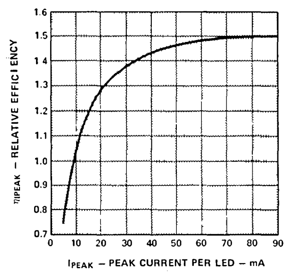


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

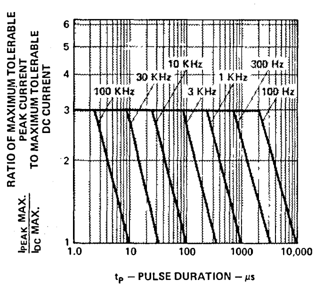


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings)

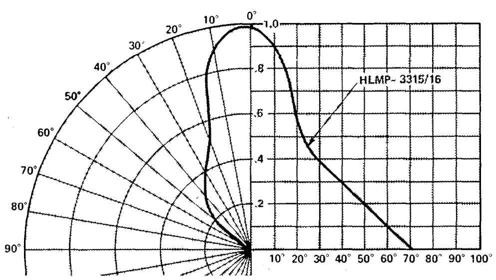


Figure 6. Relative Luminous Intensity vs. Angular Displacement

Yellow HLMP-341X Series

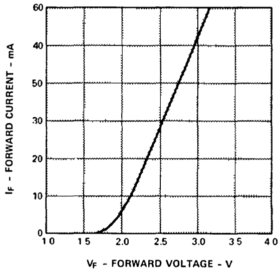


Figure 7. Forward Current vs. Forward Voltage Characteristics

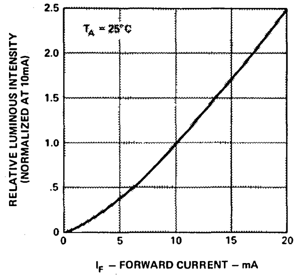


Figure 8. Relative Luminous Intensity vs. Forward Current

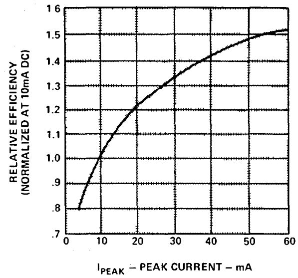


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current

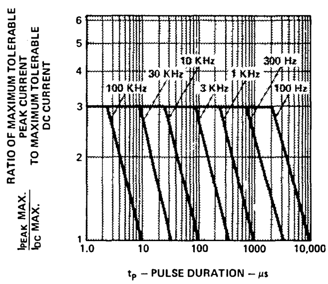


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings)

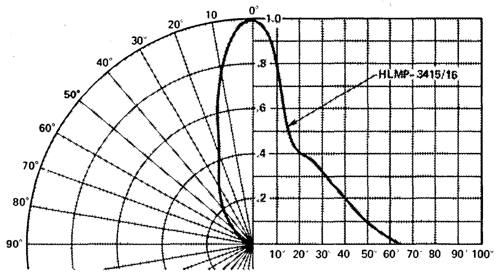


Figure 11. Relative Luminous Intensity vs. Angular Displacement

Green HLMP-351X Series

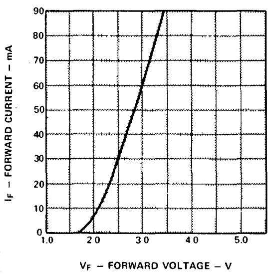


Figure 12. Forward Current vs. Forward Voltage Characteristics

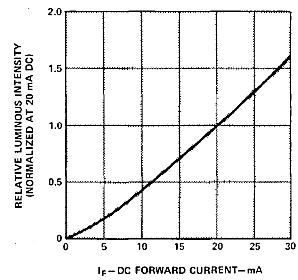


Figure 13. Relative Luminous Intensity vs. DC Forward Current

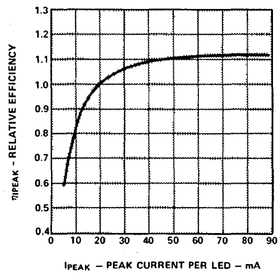


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

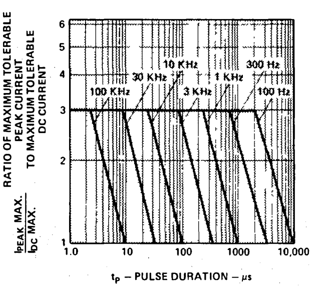


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings)

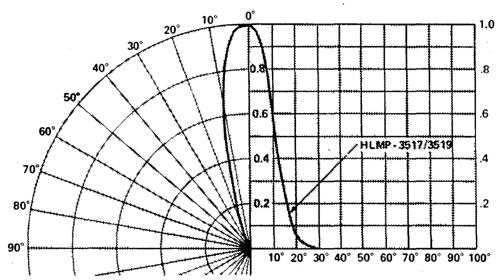


Figure 16. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Lamp

HEWLETT PACKARD

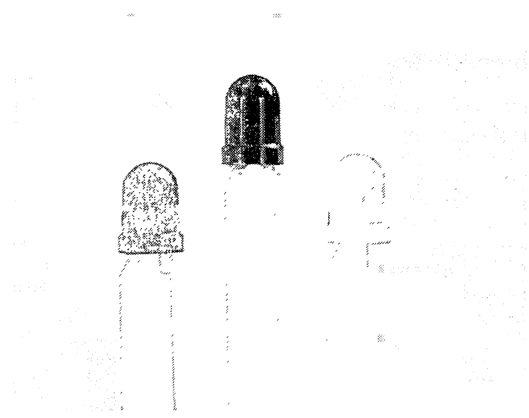
T-1 (3 mm) HIGH INTENSITY SOLID STATE LAMPS

HIGH EFFICIENCY RED • HLMP-132X SERIES
YELLOW • HLMP-142X SERIES
HIGH PERFORMANCE GREEN • HLMP-152X SERIES

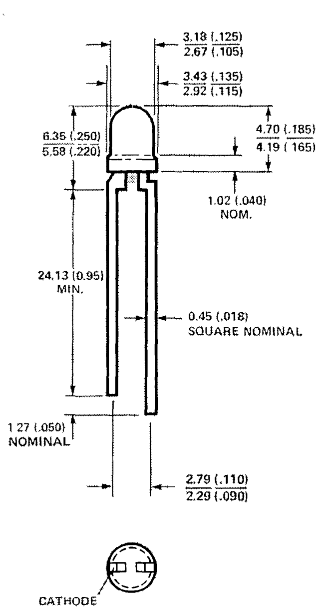
TECHNICAL DATA JANUARY 1986

Features

- HIGH INTENSITY
- CHOICE OF 3 BRIGHT COLORS
  - High Efficiency Red
  - Yellow
  - High Performance Green
- POPULAR T-1 DIAMETER PACKAGE
- SELECTED MINIMUM INTENSITIES
- NARROW VIEWING ANGLE
- GENERAL PURPOSE LEADS
- RELIABLE AND RUGGED
- AVAILABLE ON TAPE AND REEL



Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Description

This family of T-1 lamps is specially designed for applications requiring higher on-axis intensity than is achievable with a standard lamp. The light generated is focused to a narrow beam to achieve this effect.

Part Number HLMP-	Description	Minimum Intensity (mcd) at 10 mA	Color (Material)
1320 1321	Untinted Non-Diffused Tinted Non-Diffused	6	High Efficiency Red (GaAsP on GaP)
1420 1421	Untinted Non-Diffused Tinted Non-Diffused	6	Yellow (GaAsP on GaP)
1520 1521	Untinted Non-Diffused Tinted Non-Diffused	4.2	Green (GaP)

SOLID STATE LAMPS

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	1320 1321	6.0 6.0	12.0 12.0		mcd	$I_F = 10$ mA (Figure 3)
		1420 1421	6.0 6.0	12.0 12.0		mcd	$I_F = 10$ mA (Figure 8)
		1520 1521	4.2 4.2	5.0 5.0		mcd	$I_F = 10$ mA (Figure 3)
$2\Theta 1/2$	Including Angle Between Half Luminous Intensity Points	All		45		Deg.	$I_F = 10$ mA See Note 1 (Figure 6, 11, 16)
λ_{PEAK}	Peak Wavelength	132X 142X 152X		635 583 565		nm	Measurement at Peak (Figure 1)
λ_d	Dominant Wavelength	132X 142X 152X		626 585 569		nm	See Note 2 (Figure 1)
τ_S	Speed of Response	132X 142X 152X		90 90 500		ns	
C	Capacitance	132X 142X 152X		16 18 18		pF	$V_F = 0$; f = 1 MHz
θ_{JC}	Thermal Resistance	All		120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	131X 142X 152X	1.5 1.5 1.6	2.2 2.2 2.3	3.0 3.0 3.0	V	$I_F = 10$ mA
V_{BR}	Reverse Breakdown Volt.	All	5.0			V	$I_R = 100\ \mu A$
η_V	Luminous Efficacy	132X 142X 152X		145 500 595		lumens Watt	See Note 3

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Red	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage ($I_R = 100\ \mu A$)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	−55 to +100	−55 to +100	−20 to +100	°C
Storage Temperature Range	−55 to +100	−55 to +100	−55 to +100	°C
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:

1. See Figure 5 (Red), 10 (Yellow), or 15 (Green) to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50°C at 0.5 mA/°C. For Yellow series derate linearly from 50°C at 0.2 mA/°C.
3. For Red and Green series derate power linearly from 25°C at 1.8 mW/°C. For Yellow series derate power linearly from 50°C at 1.6 mW/°C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

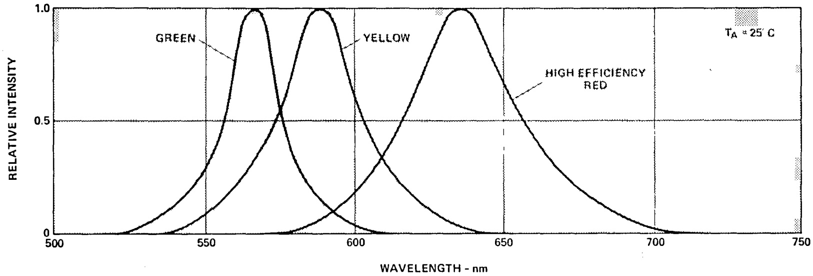


Figure 1. Relative Intensity vs. Wavelength

T-1 High Efficiency Red Non-Diffused

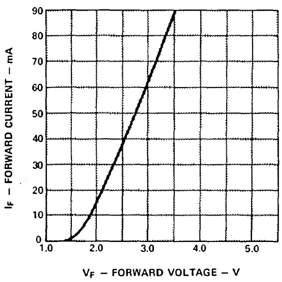


Figure 2. Forward Current vs. Forward Voltage Characteristics

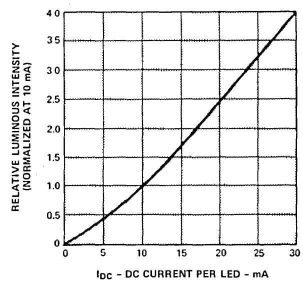


Figure 3. Relative Luminous Intensity vs. DC Forward Current

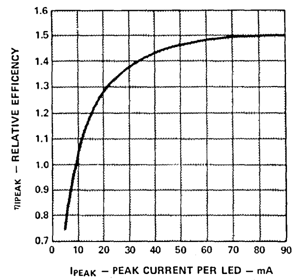


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

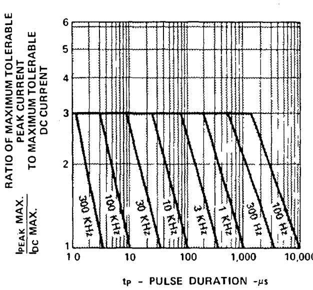


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings)

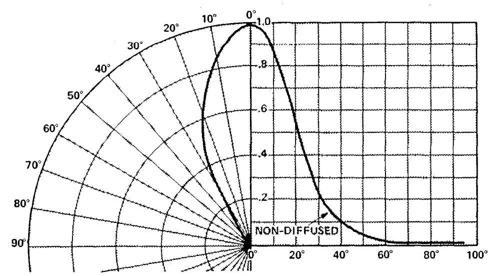


Figure 6. Relative Luminous Intensity vs. Angular Displacement

T-1 Yellow Non-Diffused

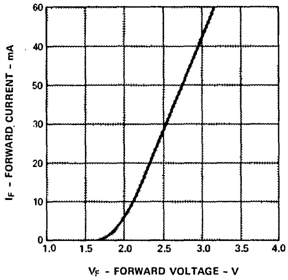


Figure 7. Forward Current vs. Forward Voltage Characteristics

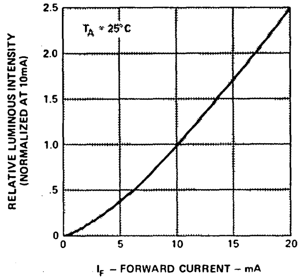


Figure 8. Relative Luminous Intensity vs. Forward Current

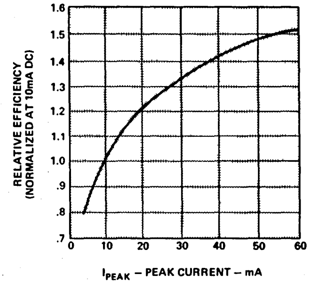


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current

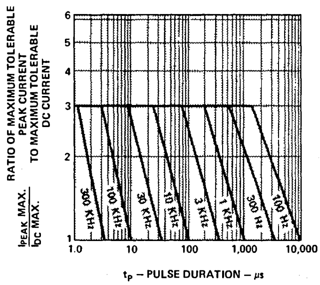


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings)

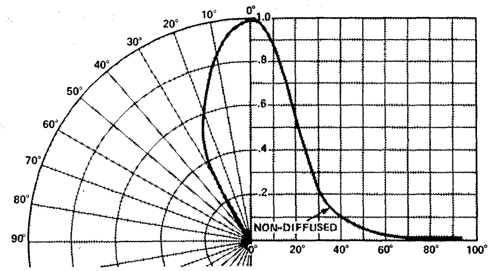


Figure 11. Relative Luminous Intensity vs. Angular Displacement

T-1 Green Non-Diffused

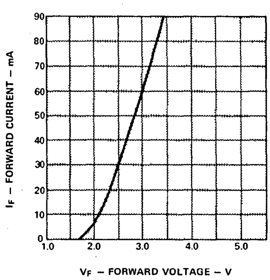


Figure 12. Forward Current vs. Forward Voltage Characteristics

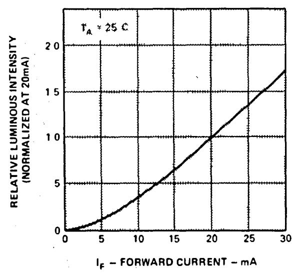


Figure 13. Relative Luminous Intensity vs. Forward Current

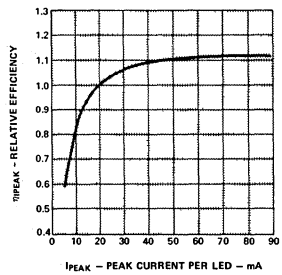


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

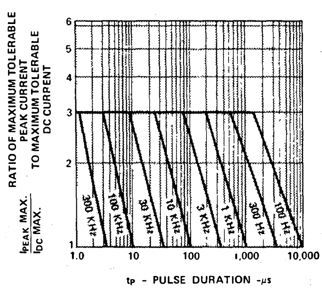


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings)

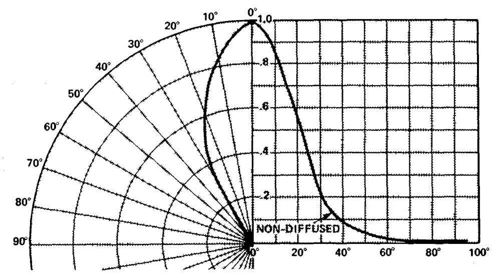


Figure 16. Relative Luminous Intensity vs. Angular Displacement

HEWLETT PACKARD

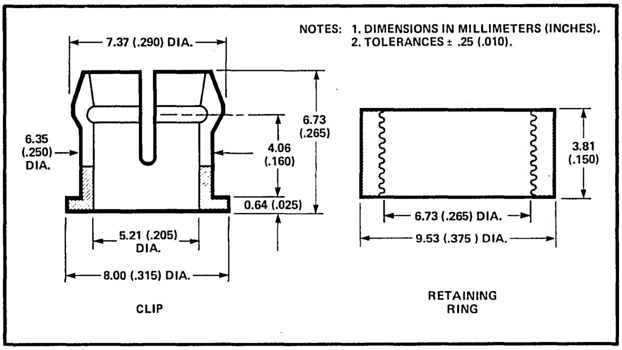
CLIP AND RETAINING RING FOR PANEL MOUNTED T1 3/4 LEDs

OPTION 009 (HLMP-0103)

TECHNICAL DATA JANUARY 1986

Description

The Option 009 (HLMP-0103) is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett-Packard Solid State high profile T-1 3/4 size lamps. This clip and ring combination is intended for installation in instrument panels from 1.52mm (.060") to 3.18mm (.125") thick. For panels greater than 3.18mm (.125") counterboring is required to the 3.18mm (.125") thickness.



Mounting Instructions

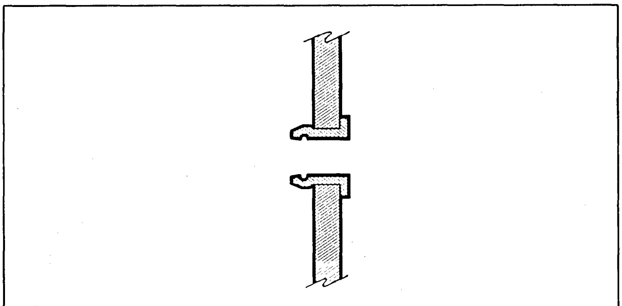
1. Drill an ASA C size 6.15mm (.242") dia. hole in the panel. Deburr but do not chamfer the edges of the hole.

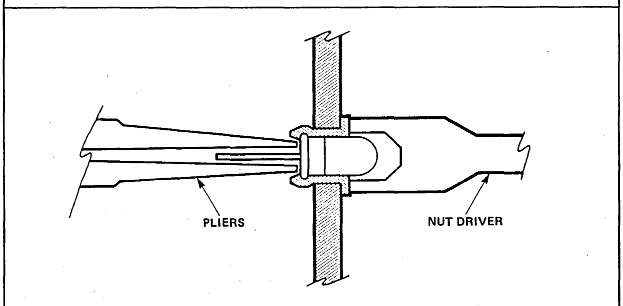
2. Press the panel clip into the hole from the front of the panel.

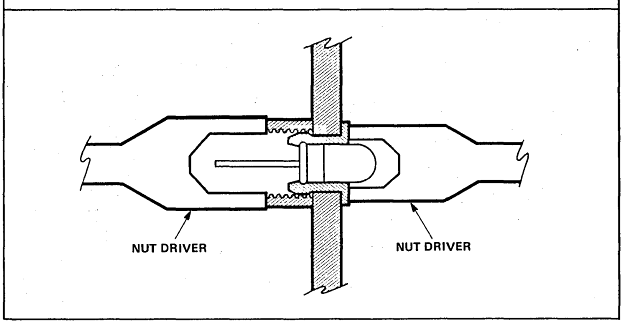
3. Press the LED into the clip from the back. Use blunt long nose pliers to push on the LED. Do not use force on the LED leads. A tool such as a nut driver may be used to press on the clip.

Note: Clip and retaining ring are also available for T-1 package, from a non-HP source. Please contact Interconsal Association, 991 Commercial St., Palo Alto, CA 94303 for additional information.

4. Slip a plastic retaining ring onto the back of the clip and press tight using tools such as two nut drivers.







Ordering Information

T-1 3/4 High Dome LED Lamps can be purchased to include clip and ring by adding Option Code 009 to the device catalog part number.

Example:

To order the HLMP-3300 including clip and ring, order as follows: HLMP-3300 Option 009.

HEWLETT PACKARD

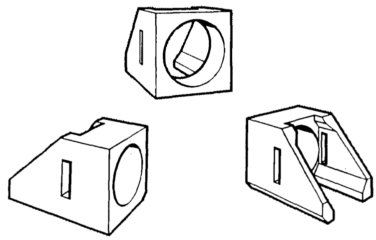
T-1 3/4 LED LAMP RIGHT ANGLE HOUSING

HLMP-5029

TECHNICAL DATA JANUARY 1986

Features

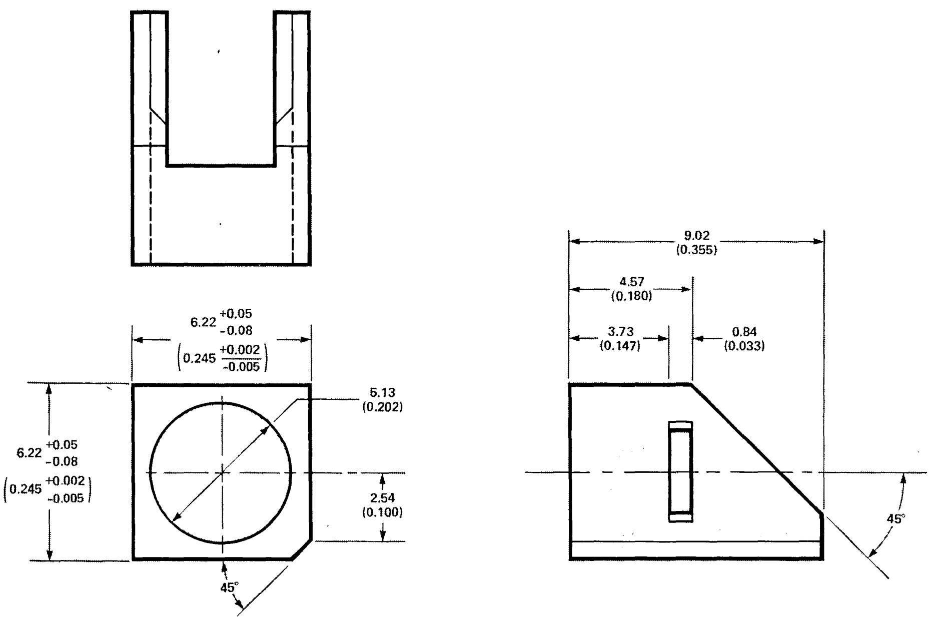
- FITS ANY HP HIGH DOME T-1 3/4 LED LAMP
- SNAP-IN FIT MAKES MOUNTING SIMPLE
- HIGH CONTRAST BLACK PLASTIC



Description

The HLMP-5029 is a black plastic right angle housing which mates with any Hewlett-Packard High Dome T-1 3/4 lamp. The lamp snaps into place. The material is fully compatible with environmental specifications of all Hewlett-Packard T-1 3/4 lamps.

Physical Dimensions



ALL TOLERANCES ±0.254 (±0.010) UNLESS OTHERWISE SPECIFIED.
DIMENSIONS IN MILLIMETRES AND (INCHES).

PATENT PENDING

HEWLETT PACKARD

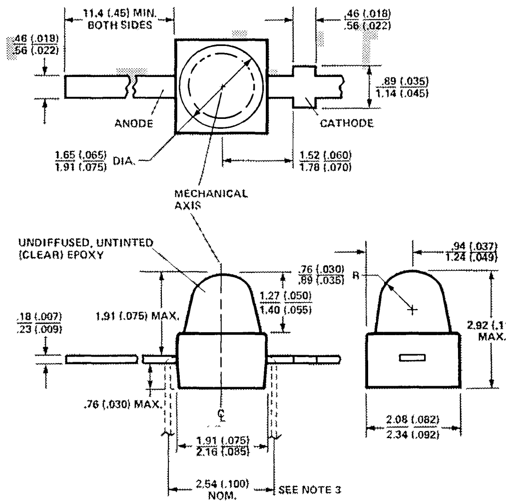
700nm HIGH INTENSITY SUBMINIATURE EMITTER

HEMT-6000

TECHNICAL DATA JANUARY 1986

Features

- HIGH RADIANT INTENSITY
- NARROW BEAM ANGLE
- NONSATURATING OUTPUT
- BANDWIDTH: DC TO 5 MHz
- IC COMPATIBLE/LOW CURRENT REQUIREMENT
- VISIBLE FLUX AIDS ALIGNMENT



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. USER MAY BEND LEADS AS SHOWN.
4. EPOXY ENCAPSULANT HAS A REFRACTIVE INDEX OF 1.53.
5. CHIP CENTERING WITHIN THE PACKAGE IS CONSISTENT WITH FOOTNOTE 3.

Description

The HEMT-6000 uses a GaAsP chip designed for optimum tradeoff between speed and quantum efficiency. This optimization allows a flat modulation bandwidth of 5 MHz without peaking, yet provides a radiant flux level comparable to that of 900nm IREDs. The subminiature package allows operation of multiple closely-spaced channels, while the narrow beam angle minimizes crosstalk. The nominal 700nm wavelength can offer spectral performance advantages over 900nm IREDs, and is sufficiently visible to aid optical alignment. Applications include paper-tape readers, punch-card readers, bar code scanners, optical encoders or transducers, interrupt modules, safety interlocks, tape loop stabilizers and fiber optic drivers.

Maximum Ratings at $T_A = 25°C$

Power Dissipation .... 50 mW
(derate linearly from 70°C @ 1.0mW/°C)

Average Forward Current .... 20 mA
(derate linearly from 70°C @ 0.4mA/°C)

Peak Forward Current .... See Figure 5

Operating and Storage
Temperature Range .... -55° to +100°C

Lead Soldering
Temperature .... 260°C for 3 sec.
[1.6 mm (0.063 in.) from body]

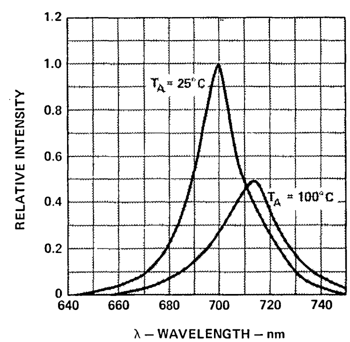


Figure 1. Relative Intensity versus Wavelength.

SOLID STATE LAMPS

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions	Fig.
I_e	Radiant Intensity along Mechanical Axis	100	250		$\mu W/sr$	$I_F = 10$ mA	3,4
K_e	Temperature Coefficient of Intensity		-0.005		$°C^{-1}$	Note 1	
η_v	Luminous Efficacy		2.5		lm/W	Note 2	
$2\Theta_{1/2}$	Optical Axis Half Intensity Total Angle		16		deg.	Note 3, $I_F = 10$ mA	6
λ_{PEAK}	Peak Wavelength (Range)		690-715		nm	Measured @ Peak	1
$\Delta\lambda_{PEAK}/\Delta T$	Spectral Shift Temperature Coefficient		.193		nm/°C	Measured @ Peak, Note 4	
t_r	Output Rise Time (10%-90%)		70		ns	$I_{PEAK} = 10$ mA	
t_f	Output Fall Time (90%-10%)		40		ns	$I_{PEAK} = 10$ mA	
C_o	Capacitance		65		pF	$V_F = 0$; f = 1 MHz	
BV_R	Reverse Breakdown Voltage	5	12		V	$I_R = 100\ \mu A$	
V_F	Forward Voltage		1.5	1.8	V	$I_F = 10$ mA	2
$\Delta V_F/\Delta T$	Temperature Coefficient of V_F		-2.1		mV/°C	$I_F = 100\ \mu A$	
Θ_{JC}	Thermal Resistance		140		°C/W	Junction to cathode lead	

NOTES:
1. $I_e(T) = I_e(25°C) \exp[K_e(T - 25°C)]$.
2. $I_v = \eta_v I_e$ where I_v is in candela, I_e in watts/steradian, and η_v in lumen/watt.
3. $\Theta_{1/2}$ is the off-axis angle at which the radiant intensity is half the intensity along the optical axis. The deviation between the mechanical and the optical axis is typically within a conical half-angle of three degrees.
4. $\lambda_{PEAK}(T) = \lambda_{PEAK}(25°C) + (\Delta\lambda_{PEAK}/\Delta T)(T - 25°C)$

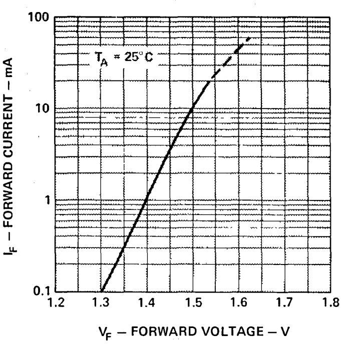


Figure 2. Forward Current versus Forward Voltage.

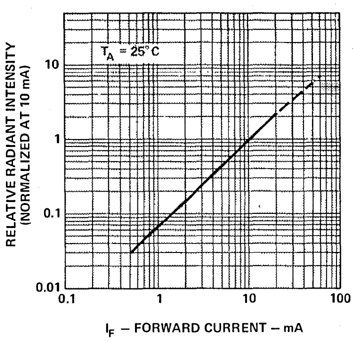


Figure 3. Relative Radiant Intensity versus Forward Current.

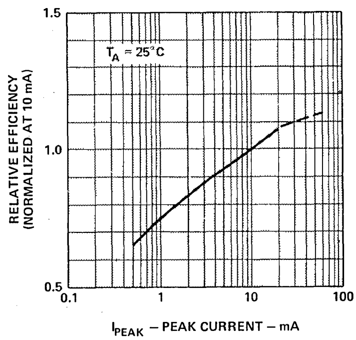


Figure 4. Relative Efficiency (Radiant Intensity per Unit Current) versus Peak Current.

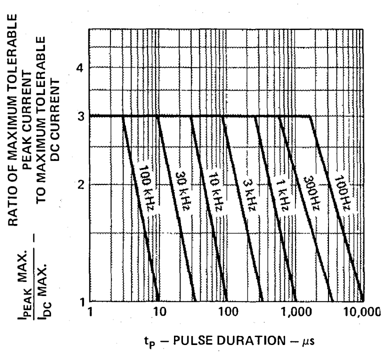


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

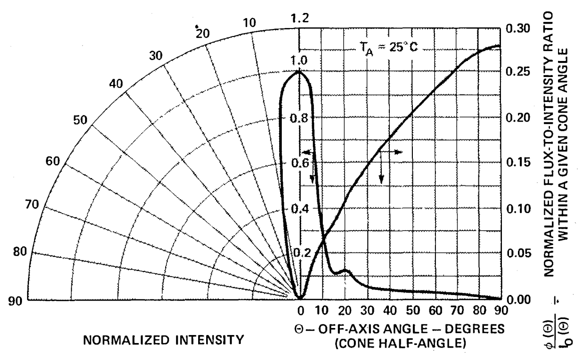
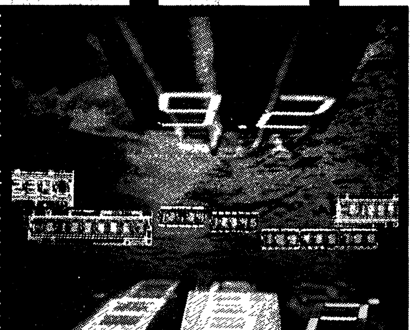


Figure 6. Far-Field Radiation Pattern.

7. Solid State Displays

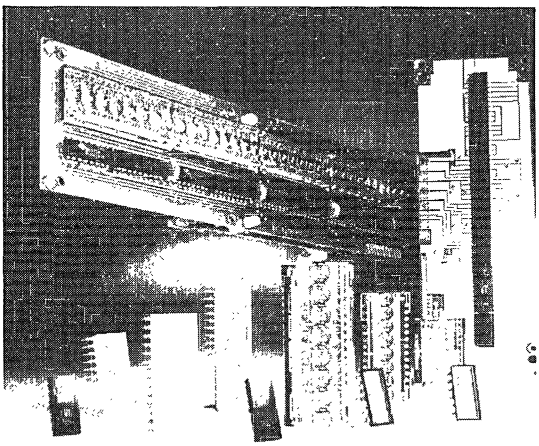


Solid State Displays

Hewlett-Packard's line of Solid State Displays answers all the needs of the designer. From smart alphanumeric displays to low cost numeric displays in sizes from 3 mm (.15 in.) to 20 mm (.8 in) and colors of red, high efficiency red, yellow, and high performance green, the selection is complete.

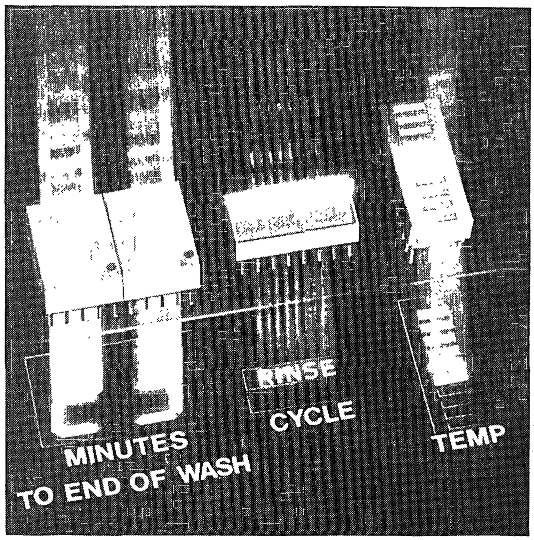
Hewlett-Packard's 5 x 7 dot matrix alphanumeric display line comes in 3 character sizes: 3.8 mm (.15 in), 5 mm (.2 in), and 6.9 mm (.27 in). In addition, there are now 4 colors available for each size: standard red, yellow, high efficiency red, and green. This wide selection of package sizes and colors makes these products ideal for a variety of applications in avionics, industrial control, and instrumentation.

The newest additions to HP's alphanumeric display line are two fully-supported monolithic sixteen segment displays. Both displays have an on-board CMOS IC containing memory, ASCII decoder, multiplexing circuitry, and drivers. Two character heights are available to fit your needs — 4.1 mm (.16 in) and 2.9 mm (.112 in). These displays incorporate many improvements over competitive products and are ideal for industrial, business and telecommunication applications.

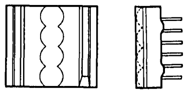
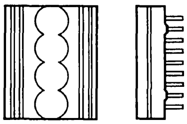
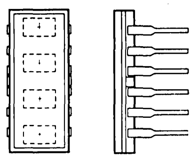
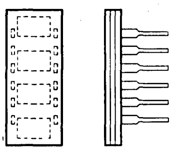
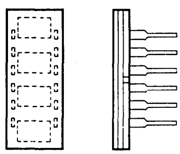
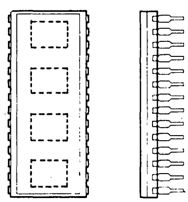
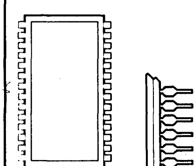


Hewlett-Packard's line of numeric seven segment displays is one of the broadest. From low cost, standard red displays to high light ambient displays producing 7.5 mcd/segment, HP's 0.3 in., 0.43 in., 0.56 in., and 0.8 in. characters can provide a solution to every display need. HP's latest product offering include 0.56 in. dual digit displays and a new line of small package, bright 0.3 in. displays — the 0.3 in. Microbright. These are ideal for displaying numeric information in electronic instrumentation, point-of-sale equipment, appliances and automotive instrumentation.

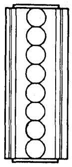
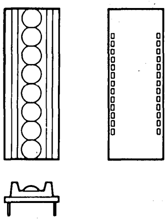
Integrated numeric and hexadecimal displays (with on-board IC's) solve the designer's decoding/driving problems. They are available in plastic packages for general purpose usage, ceramic/glass packages for industrial applications, and hermetic packages for high reliability applications. This family of displays has been designed for ease of use in a wide range of environments.



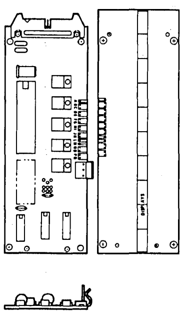
Alphanumeric LED Displays

Device		Description	Color	Application	Page No.
	HPDL-1414	2.85 mm (.112") Four Character Monolithic Smart Alphanumeric Display Operating Temperature Range: -40°C to +85°C	Red	• Portable Data Entry Devices • Industrial Instrumentation • Computer Perpherals • Telecommunication Equipment	7-15
	HPDL-2416	2.1 mm (.16") Four Character Monolithic Smart Alphanumeric Display Operating Temperature Range: -40°C to +85°C	Red	• Portable Data Entry Devices • Medical Equipment • Industrial Instrumentation • Computer Peripherals • Telecommunication Equipment	7-23
	HDSP-2000 HDSP-2001 HDSP-2002 HDSP-2003	3.7 mm (.15") 5 x 7 Four Character Alphanumeric 12 Pin Ceramic 7.62 mm (.3") DIP with untinted glass lens. Operating Temperature Range: -20°C to +85°C	Red Yellow High Efficiency Red High Performance Green	• Computer Terminals • Business Machines • Portable, Hand-held or mobile data entry, read-out or communications For further information see Application Note 1016.	7-31
	HDSP-2300 HDSP-2301 HDSP-2302 HDSP-2303	4.87 mm (.19") 5 x 7 Four Character Alphanumeric 12 Pin Ceramic 6.35 mm (.25") DIP with untinted glass lens Operating temperature Range: -20°C to +85°C	Red Yellow High Efficiency Red High Performance Green	• Avionics • Grounds Support, Cockpit, Shipboard Systems • Medical Equipment • Industrial and Process control • Computer Peripherals and Terminals For further information see Application Note 1016.	7-35
	HDSP-2381 HDSP-2382 HDSP-2393	4.87 mm (.19") 5 x 7 Four Character Alphanumeric Sunlight Viewable Display	Yellow High Efficiency Red High Performance Green	• Avionics • Cockpit • Ground Support Systems • Industrial	7-41
	HDSP-2490 HDSP-2491 HDSP-2492 HDSP-2493	6.9 mm (.27") 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (.6") DIP with untinted glass lens Operating Temperature Range: -20°C to +85°C	Red Yellow High Efficiency Red High Performance Green	• High Brightness Ambient Systems • Industrial and Process Control • Computer Peripherals • Ground Support Systems For further information see Application Note 1016.	7-52
	5082-7100 5082-7101 5082-7102	6.9 mm (.27") 5 x 7 Three Character Alphanumeric 22 Pin Ceramic 15.2 mm (.6") DIP 6.9 mm (.27") 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.2 mm (.6") DIP 6.9 mm (.27") 5 x 7 Five Character Alphnumeric 36 Pin Ceramic 15.2 mm (.6") DIP	Red Untinted Glass Lens	General Purpose Market • Business Machines • Calculators • Solid State CRT • Industrial Equipment	7-68

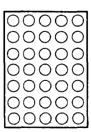
Alphanumeric LED Displays (cont.)

Device		Description	Color	Application	Page No.
	HDSP-6504	3.8 mm (.15") Sixteen Segment Four Character Alphanumeric 22 Pin 15.2 mm (.6") DIP	Red	• Computer Terminals • Hand Held Instruments • In-Plant Control Equipment • Diagnostic Equipment	7-72
	HDSP-6508	3.8 mm (.15") Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (.6") DIP			
	HDSP-6300	3.56 mm (.14") Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (.6") DIP		• Computer Peripherals and Terminals • Computer Base Emergency Mobile Units • Automotive Instrument Panels • Desk Top Calculators • Hand-Held Instruments For further information ask for Application Note 931.	7-78

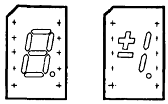
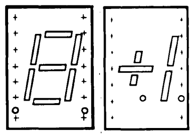
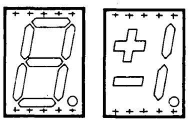
Alphanumeric Display Systems

Device		Description	Package	Application	Page No.
	HDSP-2416	Single-Line 16 Character Display Panel Utilizing the HDSP-2000	162.56 mm (6.4") L x 58.42 mm (2.3") H x 7.11 mm (28") D	• Data Entry Terminals • Instrumentation	7-56
	HDSP-2424	Single-Line 24 Character Display Panel Utilizing the HDSP-2000			
	HDSP-2432	Single-Line 32 Character Display Panel Utilizing the HDSP-2000			
	HDSP-2440	Single-Line 40 Character Display Panel Utilizing the HDSP-2000 Display	177.80 mm (7.0") L x 58.42 mm (2.3") H x 7.11 mm (.28") D		
	HDSP-2470	HDSP-2000 Display Interface Incorporating a 64 Character ASCII Decoder	171.22 mm (6.74") L x 58.42 mm (2.3") H x 16.51 mm (.65") D		
	HDSP-2471	HDSP-2000 Display Interface Incorporating a 128 Character ASCII Decoder			
	HDSP-2472	HDSP-2000 Display Interface without ASCII Decoder. Instead, a 24 Pin Socket is Provided to Accept a Custom 128 Character Set from a User Programmed 1K x 8 PROM			

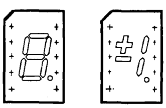
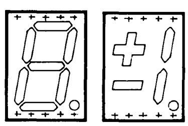
Alphanumeric Displays

Device		Description	Package	Typical Iv @20 mA DC	Page No.
	HDSP-4501	High Efficiency Red, Common Anode Row	26.5 mm (1.05") Dual-in-Line 1.09" H x .77" W x .24" D		7-83
	HDSP-4503	High Efficiency Red, Common Cathode Row			

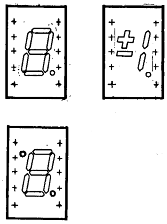
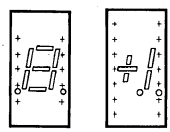
High Efficiency Red Low Current Seven Segment LED Displays

Package	Device	Description	Typical I_V @ 2 mA DC	Page No.
 7.62 mm (.3") Microbright Dual-in-Line .5" H x .3" W x .24" D	HDSP-7511 HDSP-7513 HDSP-7517 HDSP-7518	High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red, Overflow, ±1, Common Anode High Efficiency Red, Overflow, ±1, Common Cathode	270μcd/seg.	7-85
 10.92 mm (.43") Dual-in-line .75" H x .5" W x .25" D	HDSP-3350 HDSP-3351 HDSP-3353 HDSP-3356	High Efficiency Red, Common Anode, LHDP High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red, Universal Polarity and Overflow Indicator, RHDP	300μcd/seg.	7-85
 14.2 mm (.56") Dual-in-Line (Single Digit) .67" H x .49" W x .31" D	HDSP-5551 HDSP-5553 HDSP-5557 HDSP-5558	High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red, Overflow, ±1, Common Anode High Efficiency Red, Overflow, ±1, Common Cathode	370μcd/seg.	7-85

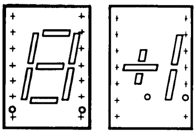
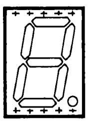
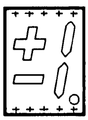
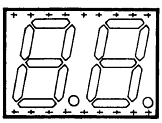
Emerald Green Seven Segment LED Displays

Package	Device	Description	Typical I_V @ 20 mA DC	Page No.
 7.62 mm (.3") Microbright Dual-in-Line .5" H x .3" W x .24" D	HDSP-7901 HDSP-7903 HDSP-7907 HDSP-7908	Emerald Green, Common Anode, RHDP Emerald Green, Common Cathode, RHDP Emerald Green, Overflow, ±1, Common Anode Emerald Green, Overflow, ±1, Common Cathode	1475μcd/seg.	7-91
 14.2 mm (.56") Dual-in-Line (Single Digit) .67" H x .49" W x .31" D	HDSP-5901 HDSP-5903 HDSP-5907 HDSP-5908	Emerald Green, Common Anode, RHDP Emerald Green, Common Cathode, RHDP Emerald Green, Overflow, ±1, Common Anode Emerald Green, Overflow, ±1, Common Cathode	1550μcd/seg.	7-91

Red, High Efficiency Red, Yellow, and High Performance Green Seven Segment LED Displays

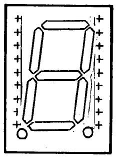
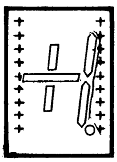
Package	Device	Description	Typical I_V @ 20 mA DC	Page No.
 7.62 mm (.3") Microbright Dual-in-Line .5" H x .3" W x .24" D	HDSP-7301	Red, Common Anode, RHDP	1100 μcd/seg	7-97
	HDSP-7302	Red, Common Anode, RHDP, Colon		
	HDSP-7303	Red, Common Cathode, RHDP		
	HDSP-7304	Red, Common Cathode, RHDP, Colon		
	HDSP-7307	Red, Overflow, ±1, Common Anode, RHDP		
	HDSP-7308	Red, Overflow, ±1, Common Cathode, RHDP		
	HDSP-7311	Bright Red, Common Anode, RHDP	1355 μcd/seg	
	HDSP-7313	Bright Red, Common Cathode, RHDP		
	HDSP-7317	Bright Red, Overflow, ±1, Common Anode		
	HDSP-7318	Bright Red, Overflow, ±1, Common Cathode		
	HDSP-7401	Yellow, Common Anode, RHDP	2750 μcd/seg	
	HDSP-7402	Yellow, Common Anode, RHDP, Colon		
	HDSP-7403	Yellow, Common Cathode, RHDP		
	HDSP-7404	Yellow, Common Cathode, RHDP, Colon		
	HDSP-7407	Yellow, Overflow, ±1, Common Anode		
	HDSP-7408	Yellow, Overflow, ±1, Common Cathode		
	HDSP-7501	High Efficiency Red, Common Anode, RHDP	5400 μcd/seg	
	HDSP-7502	High Efficiency Red, Common Anode, RHDP, Colon		
	HDSP-7503	High Efficiency Red, Common Cathode, RHDP		
	HDSP-7504	High Efficiency Red, Common Cathode, RHDP, Colon		
	HDSP-7507	High Efficiency Red, Overflow, ±1, Common Anode		
	HDSP-7508	High Efficiency Red, Overflow, ±1, Common Cathode		
	HDSP-7801	High Performance Green, Common Anode, RHDP	3700 μcd/seg	
	HDSP-7802	High Performance Green, Common Anode, RHDP, Colon		
	HDSP-7803	High Performance Green, Common Cathode, RHDP		
	HDSP-7804	High Performance Green, Common Cathode, RHDP, Colon		
	HDSP-7807	High Performance Green, Overflow, ±1, Common Anode		
	HDSP-7808	High Performance Green, Overflow, ±1, Common Cathode		
 7.62 mm (.3") Dual-in-line .75" H x .4" W x .18" D	5082-7730	Red, Common Anode, LHDP	770 μcd/seg	7-103
	5082-7731	Red, Common Anode, RHDP		
	5082-7736	Red, Common Anode, Polarity and Overflow Indicator, RHDP		
	5082-7740	Red, Common Cathode, RHDP		
	5082-7610	High Efficiency Red, Common Anode, LHDP	4400 μcd/seg	
	5082-7611	High Efficiency Red, Common Anode, RHDP		
	5082-7613	High Efficiency Red, Common Cathode, RHDP		
	5082-7616	High Efficiency Red, Universal Polarity Overflow Indicator, RHDP		
	5082-7620	Yellow, Common Anode, LHDP	3400 μcd/seg	
	5082-7621	Yellow, Common Anode, RHDP		
	5082-7623	Yellow, Common Cathode, RHDP		
	5082-7626	Yellow, Universal Polarity and Overflow Indicator, RHDP		
	HDSP-3600	High Performance Green, Common Anode, LHDP	3950 μcd/seg	
	HDSP-3601	High Performance Green, Common Anode, RHDP		
	HDSP-3603	High Performance Green, Common Cathode, RHDP		
	HDSP-3606	High Performance Green, Universal Overflow Indicator, RHDP		

Red, High Efficiency Red, Yellow, and High Performance Green Seven Segment LED Displays (continued)

Package	Device	Description	Typical I_V @ 20 mA DC	Page No.
 10.92 mm (.43") Dual-in-line .75" H x .5" W x .25" D	5082-7750	Red, Common Anode, LHDP	1100 μcd/seg	7-103
	5082-7751	Red, Common Anode, RHDP		
	5082-7756	Red, Universal Polarity and Overflow Indicator, RHDP		
	5082-7760	Red, Common Cathode, RHDP		
	5082-7650	High Efficiency Red, Common Anode, LHDP	6100 μcd/seg	
	5082-7651	High Efficiency Red, Common Anode, RHDP		
	5082-7653	High Efficiency Red, Common Cathode, RHDP		
	5082-7656	High Efficiency Red, Universal Polarity and Overflow Indicator, RHDP		
	5082-7660	Yellow, Common Anode, LHDP	4600 μcd/seg	
	5082-7661	Yellow, Common Anode, RHDP		
	5082-7663	Yellow, Common Cathode, RHDP		
	5082-7666	Yellow, Universal Polarity and Overflow Indicator, RHDP		
	HDSP-4600	High Performance Green, Common Anode, LHDP	3850 μcd/seg	
	HDSP-4601	High Performance Green, Common Anode, RHDP		
	HDSP-4603	High Performance Green, Common Cathode, RHDP		
	HDSP-4606	High Performance Green, Universal Overflow Indicator, RHDP		
  14.2 mm (.56") Dual-in-Line (Single Digit) .67" H x .49" W x .31" D	HDSP-5301	Red, Common Anode, RHDP	1300 μcd/seg	7-112
	HDSP-5303	Red, Common Cathode, RHDP		
	HDSP-5307	Red ±1, Common Anode, RHDP		
	HDSP-5308	Red ±1, Common Cathode, RHDP		
	HDSP-5321	Red, Common Anode, Dual Digit, RHDP		
	HDSP-5323	Red, Common Cathode, Dual Digit, RHDP		
	HDSP-5501	High Efficiency Red, Common Anode, RHDP	6300 μcd/seg	
	HDSP-5503	High Efficiency Red, Common Cathode, RHDP		
	HDSP-5507	High Efficiency Red ±1, Common Anode, RHDP		
	HDSP-5508	High Efficiency Red ±1, Common Cathode, RHDP		
	HDSP-5521	High Efficiency Red, Common Anode, Dual Digit, RHDP		
	HDSP-5523	High Efficiency Red, Common Cathode, Dual Digit, RHDP		
	HDSP-5601	High Performance Green, Common Anode, RHDP	5600 μcd/seg	
	HDSP-5603	High Performance Green, Common Cathode, RHDP		
	HDSP-5607	High Performance Green, Common Anode Overflow Indicator, RHDP		
	HDSP-5608	High Performance Green, Common Cathode Overflow Indicator, RHDP		
	HDSP-5621	High Performance Green, Common Anode, Dual Digit, RHDP		
	HDSP-5623	High Performance Green, Common Cathode, Dual Digit, RHDP		
14.2 mm (.56") Dual-in-Line (Dual Digit) .67" H x 1.0" W x .31" D	HDSP-5701	Yellow, Common Anode, RHDP	4200 μcd/seg	
	HDSP-5703	Yellow, Common Cathode, RHDP		
	HDSP-5707	Yellow ±1, Common Anode, RHDP		
	HDSP-5708	Yellow ±1, Common Cathode, RHDP		
	HDSP-5721	Yellow, Common Anode, Dual Digit, RHDP		
	HDSP-5723	Yellow, Common Cathode, Dual Digit, RHDP		

SOLID STATE DISPLAYS

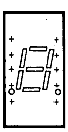
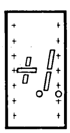
Red, High Efficiency Red, Yellow, and High Performance Green Seven Segment LED Displays (continued)

Package	Device	Description	Typical I_V @ 20 mA DC	Page No.
 	HDSP-3400	Red, Common Anode, LHDP	1200 μcd/seg	7-120
	HDSP-3401	Red, Common Anode, RHDP		
	HDSP-3403	Red, Common Cathode, RHDP		
	HDSP-3405	Red, Common Cathode, LHDP		
	HDSP-3406	Red, Universal Polarity Overflow Indicator, RHDP		
	HDSP-3900	High Efficiency Red, Common Anode, LHDP	4800 μcd/seg	
	HDSP-3901	High Efficiency Red, Common Anode, RHDP		
	HDSP-3903	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3905	High Efficiency Red, Common Cathode, LHDP		
	HDSP-3906	High Efficiency Red, Universal Polarity Overflow Indicator, RHDP		
	HDSP-4200	Yellow, Common Anode, LHDP	3400 μcd/seg	
	HDSP-4201	Yellow, Common Anode, RHDP		
	HDSP-4203	Yellow, Common Cathode, RHDP		
	HDSP-4205	Yellow, Common Cathode, LHDP		
	HDSP-4206	Yellow, Universal Polarity Overflow Indicator, RHDP		
	HDSP-8600	High Performance Green, Common Anode, LHDP	3600 μcd/seg	
20 mm (.8") Dual-in-Line 1.09" H x .78" W x .33" D	HDSP-8601	High Performance Green, Common Anode, RHDP		
	HDSP-8603	High Performance Green, Common Cathode, RHDP		
	HDSP-8605	High Performance Green, Common Cathode, LHDP		
	HDSP-8606	High Performance Green, Universal Overflow Indicator, RHDP		

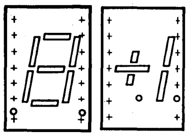
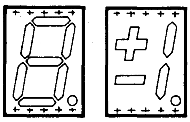
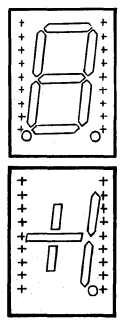
Solid State Display Options

Option	Description	Page No.
Option S02 Option S20	Intensity and Color Selected Displays	7-135

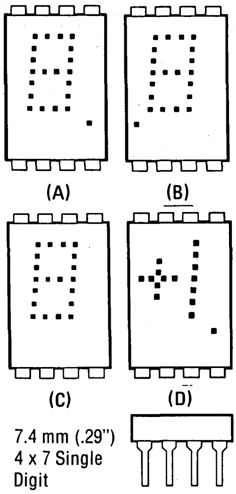
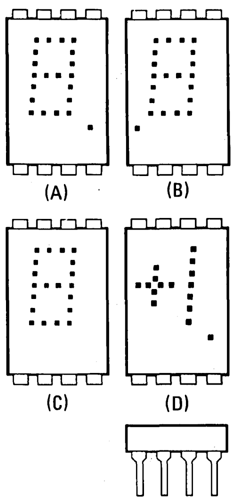
High Ambient Light, High Efficiency Red, Yellow, and High Performance Green Seven Segment Displays

Package	Device	Description	Typical I_V @ 100 mA Peak 1/5 Duty Factor	Page No.
 	HDSP-3530	High Efficiency Red, Common Anode, LHDP	7100 μcd/seg	7-127
	HDSP-3531	High Efficiency Red, Common Anode, RHDP		
	HDSP-3533	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3536	High Efficiency Red, Universal Polarity Overflow Indicator, RHDP		
	HDSP-4030	Yellow, Common Anode, LHDP	4500μcd/seg	
7.62 mm (.3") Dual-in-Line .75" H x .4" W x .18" D	HDSP-4031	Yellow, Common Anode, RHDP		
	HDSP-4033	Yellow, Common Cathode, RHDP		
	HDSP-4036	Yellow, Universal Polarity Overflow Indicator, RHDP		
	HDSP-3600	High Performance Green, Common Anode, LHDP	7000 μcd/seg (90 mA Peak 1/3 Duty Factor)	
	HDSP-3601	High Performance Green, Common Anode, RHDP		
	HDSP-3603	High Performance Green, Common Cathode, RHDP		
	HDSP-3606	High Performance Green, Universal Overflow Indicator, RHDP		

High Ambient Light, High Efficiency Red, Yellow, and High Performance Green Seven Segment Displays (continued)

Package	Device	Description	Typical I_V @ 100 mA Peak 1/5 Duty Factor	Page No.
	HDSP-3730	High Efficiency Red, Common Anode, LHDP	10900 μcd/seg	7-127
	HDSP-3731	High Efficiency Red, Common Anode, RHDP		
	HDSP-3733	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3736	High Efficiency Red, Universal Polarity Overflow Indicator, RHDP		
	HDSP-4130	Yellow, Common Anode, LHDP	5000 μcd/seg	
	HDSP-4131	Yellow, Common Anode, RHDP		
10.92 mm (.43")	HDSP-4133	Yellow, Common Cathode, RHDP		
Dual-in-Line	HDSP-4136	Yellow, Universal Polarity Overflow Indicator, RHDP		
.75" H x .5" W x .25" D	HDSP-4600	High Performance Green, Common Anode, LHDP	6800μcd/seg	
	HDSP-4601	High Performance Green, Common Anode, RHDP	(90 mA Peak	
	HDSP-4603	High Performance Green, Common Cathode, RHDP	1/3 Duty Factor)	
	HDSP-4606	High Performance Green, Universal Overflow Indicator, RHDP		
	HDSP-5531	High Efficiency Red, Common Anode, RHDP	6000 μcd/seg	7-112
	HDSP-5533	High Efficiency Red, Common Cathode, RHDP		
	HDSP-5537	High Efficiency Red ±1, Common Anode		
	HDSP-5538	High Efficiency Red ±1, Common Cathode		
	HDSP-5731	Yellow, Common Anode, RHDP	5500 μcd/seg	
14.2 mm (.56")	HDSP-5733	Yellow, Common Cathode, RHDP		
Dual-in-Line	HDSP-5737	Yellow, ±1, Common Anode		
.67" H x .49" W x .31" D	HDSP-5738	Yellow, ±1, Common Cathode		
	HDSP-5601	High Performance Green, Common Anode, RHDP	9400 μcd/seg	
	HDSP-5603	High Performance Green, Common Cathode, RHDP	(90 mA Peak	
	HDSP-5607	High Performance Green, Common Anode Overflow Indicator	1/3 Duty Factor)	
	HDSP-5608	High Performance Green, Common Cathode Overflow Indicator		
	HDSP-3900	High Efficiency Red, Common Anode, LHDP	7000 μcd/seg	7-120
	HDSP-3901	High Efficiency Red, Common Anode, RHDP		
	HDSP-3903	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3905	High Efficiency Red, Common Cathode, LHDP		
	HDSP-3906	High Efficiency Red, Universal Overflow Indicator, RHDP		
	HDSP-4200	Yellow, Common Anode, LHDP	7000 μcd/seg	
	HDSP-4201	Yellow, Common Anode, RHDP		
	HDSP-4203	Yellow, Common Cathode, RHDP		
	HDSP-4205	Yellow, Common Cathode, LHDP		
	HDSP-4206	Yellow, Universal Polarity Overflow Indicator, RHDP		
	HDSP-8600	High Performance Green, Common Anode, LHDP	5800 μcd/seg	
	HDSP-8601	High Performance Green, Common Anode, RHDP	(90 mA Peak	
20 mm (.8")	HDSP-8603	High Performance Green, Common Cathode, RHDP	1/3 Duty Factor)	
Dual-in-Line	HDSP-8605	High Performance Green, Common Cathode, LHDP		
1.09" H x .78" W x .33" D	HDSP-8606	High Performance Green, Universal Overflow Indicator, RHDP		

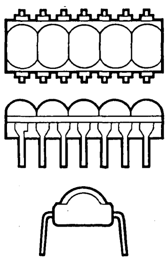
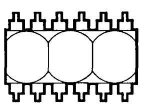
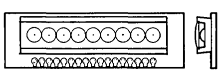
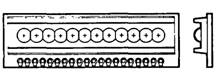
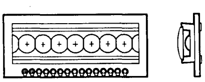
Hexadecimal and Dot Matrix Displays

Device		Description	Package	Application	Page No.
 (A) (B) (C) (D) 7.4 mm (.29") 4 x 7 Single Digit	5082-7300 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	8 Pin Epoxy 15.2 mm (.6") DIP	General Purpose Market • Test Equipment • Business Machines • Computer Peripherals • Avionics	7-136
	5082-7302 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	5082-7340 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	5082-7304 (D)	Over Range ±1			
	5082-7356 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	8 Pin Glass Ceramic 15.2 mm (.6") DIP	• Medical Equipment • Industrial and Process Control Equipment • Computers • Where Ceramic Package IC's are required • High Reliability Applications	7-140
	5082-7357 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	5082-7359 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	5082-7358 (D)	Over Range ±1			
 (A) (B) (C) (D) 7.4 mm (.29") 4 x 7 Single Digit Package: 8 Pin Glass Ceramic 15.2 mm (.6") DIP	HDSP-0760 (A)	Numeric RHDP Built in Decoder/Driver/Memory	High Efficiency Red Low Power	• Military Equipment • Ground Support Equipment • Avionics • High Reliability Applications	7-145
	HDSP-0761 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0762 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0763 (D)	Over Range ± 1			
	HDSP-0770 (A)	Numeric RHDP Built in Decoder/Driver/Memory	High Efficiency Red High Brightness	• High Brightness Ambient Systems • Cockpit, Shipboard Equipment • High Reliability Applications	
	HDSP-0771 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0772 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0763 (D)	Over Range ± 1			
	HDSP-0860 (A)	Numeric RHDP Built in Decoder/Driver/Memory	Yellow	• Business Machines • Fire Control Systems • Military Equipment • High Reliability Applications	
	HDSP-0861 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0862 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0863 (D)	Over Range ± 1			

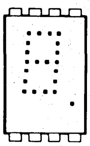
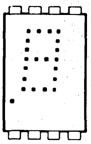
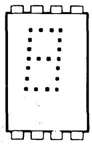
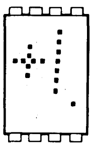
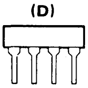
Hexadecimal and Dot Matrix Displays (continued)

Device and Package		Description	Color	Application	Page No.
(See previous page)	HDSP-0960 (A)	Numeric RHDP Built in Decoder/Driver/Memory	High Performance Green	• Business Machines • Fire Control Systems • Military Equipment • High Reliability Applications	7-145
	HDSP-0961 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0962 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0963 (D)	Over Range ± 1			

Monolithic Numeric Displays

Device		Description	Package	Application	Page No.
	5082-7404	2.79 mm (.11") Red, 4 Digits Centered D.P.	12 Pin Epoxy, 7.62 mm (.3") DIP	Small Display Market • Portable/Battery Power Instruments • Portable Calculators • Digital Counters • Digital Thermometers • Digital Micrometers • Stopwatches • Cameras • Copiers • Digital Telephone Peripherals • Data Entry Terminals • Taxi Meters For further information ask for Application Note 937.	7-151
	5082-7405	2.79 mm (.11") Red, 5 Digits, Centered D.P.	14 Pin Epoxy, 7.62 mm (.3") DIP		
	5082-7414	2.79 mm (.11") Red, 4 Digits, RHDP	12 Pin Epoxy, 7.62 mm (.3") DIP		
	5082-7415	2.79 mm (.11") Red, 5 Digits, RHDP	14 Pin Epoxy, 7.62 mm (.3") DIP		
	5082-7432	2.79 mm (.11") Red, 2 Digits, Right, RHDP	12 Pin Epoxy, 7.62 mm (.3") DIP		
	5082-7433	2.79 mm (.11") Red, 3 Digits, RHDP			
	5082-7441	2.67 mm (.105") Red, 9 Digits, Mounted on P.C. Board	50.8 mm (2") PC Bd., 17 Term. Edge Con.		7-156
	5082-7446	2.92 mm (.115") Red, 16 Digits, Mounted on P.C. Board	69.85 mm (2.750") PC Bd., 24 Term. Edge Con.		
	5082-7285	4.45 mm (.175") Red, 5 Digits, Mounted on P.C. Board. RHDP	50.8 mm (2") PC Bd., 15 Term. Edge Con.		
	5082-7295	4.45 mm (.175") Red, 15 Digits, Mounted on P.C. Board. RHDP	91.2 mm (3.59") PC Bd., 23 Term. Edge Con.		

Hermetic Hexadecimal and Numeric Dot Matrix Displays

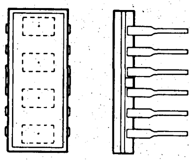
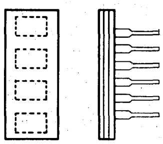
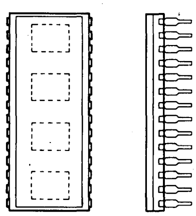
Device		Description	Package	Application	Page No.
 (A)  (B)  (C)  (D)  7.4 mm (.29") 4 x 7 Single Digit Package: 8 Pin Glass Ceramic 15.2mm (.6") DIP Truly Hermetic	4N51 4N51TXV M87157/00101ACX[1] (4N51TXVB) (A)	Numeric RHDP Decoder/Driver/Memory TXV — Hi Rel Screened	8 Pin Hermetic Built-in 15.2 mm (.6") DIP with gold plated leads	• Military High Reliability Applications • Avionics/Space Flight Systems • Fire Control Systems • Ground Support, Shipboard Equipment	8-30
	4N52 4N52TXV M87157/00102ACX[1] (4N52TXVB) (B)	Numeric LHDP Built-in Decoder/Driver/Memory TXV — Hi Rel Screened			
	4N54 4N54TXV M87157/00103ACX[1] (4N54TXVB) (C)	Hexadecimal Built-in Decoder/Driver/Memory TXV — Hi Rel Screened			
	4N53 4N53TXV 104ACX[1] (4N53TXVB) (D)	Character Plus/Minus Sign TXV — Hi Rel Screened			
	HDSP-0781 (A) HDSP-0781 TXV HDSP-0781 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	High Efficiency Red, Low Power	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	8-38
	HDSP-0782 (B) HDSP-0782 TXV HDSP-0782 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0783 (D) HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0784 (C) HDSP-0784 TXV HDSP-0784 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0791 (A) HDSP-0791 TXV HDSP-0791 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	High Efficiency Red, High Brightness	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	
	HDSP-0792 (B) HDSP-0792 TXV HDSP-0792 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			

[1] Military Approved and Qualified for High Reliability Applications.

Hermetic Hexadecimal and Numeric Dot Matrix Displays (cont.)

Device		Description	Color	Application	Page No.
(See previous page)	HDSP-0783 (D) HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	High Efficiency Red, High Brightness	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	8-38
	HDSP-0794 (C) HDSP-0794 TXV HDSP-0794 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0881 (A) HDSP-0881 TXV HDSP-0881 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	Yellow		
	HDSP-0882 (B) HDSP-0882 TXV HDSP-0882 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0883 (D) HDSP-0883 TXV HDSP-0883 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0884 (C) HDSP-0884 TXV HDSP-0884 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			

Hermetic Alphanumeric Displays

Device		Description	Color	Application	Page No.
	HDSP-2010 HDSP-2010 TXV HDSP-2010 TXVB	3.7 mm (.15") 5 x 7 Four Character Alphanumeric Operating Temperature Range: -40°C to +85°C TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	Red, Red Glass Contrast Filter	• Extended temperature applications requiring high reliability. • I/O Terminals • Avionics For further information see Application Note 1016.	8-46
	HDSP-2310 HDSP-2310 TXV HDSP-2310 TXVB	5.0 mm (.20") 5 x 7 Four Character Alphanumeric 12 Pin Ceramic 6.35 mm (.25") DIP with untinted glass lens Operating Temperature Range: -55°C to +85°C True Hermetic Seal TXV — Hi Rel Screened TXVB — Hi Rel Screened to Level A MIL-D-87157	Standard Red	• Military Equipment • Avionics • High Rel Industrial Equipment	8-52
	HDSP-2311 HDSP-2311 TXV HDSP-2311 TXVB		Yellow		
	HDSP-2312 HDSP-2312 TXV HDSP-2312 TXVB		High Eff. Red		
	HDSP-2450 HDSP-2450 TXV HDSP-2450 TXVB	Operating Temperature Range: -55°C to +85°C 6.9 mm (.27") 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (.6") DIP True Hermetic Seal TXV — Hi Rel Screened TXVB — Hi Rel Screened to Level A MIL-D-87157	Red	• Military Equipment • High Reliability Applications • Avionics • Ground Support, Cockpit, Shipboard Systems	8-59
	HDSP-2451 HDSP-2451 TXV HDSP-2451 TXVB		Yellow		
	HDSP-2452 HDSP-2452 TXV HDSP-2452 TXVB		High Efficiency Red		

HEWLETT PACKARD

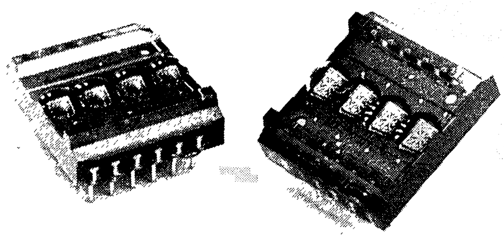
FOUR CHARACTER 2.85mm (0.112 in.) SMART ALPHANUMERIC DISPLAY

HPDL-1414

TECHNICAL DATA JANUARY 1986

Features

- **SMART ALPHANUMERIC DISPLAY**
  Built-in RAM, ASCII Decoder and LED Drive Circuitry
- **WIDE OPERATING TEMPERATURE RANGE**
  −40° C to +85° C
- **FAST ACCESS TIME**
  160 ns
- **EXCELLENT ESD PROTECTION**
  Built-in Input Protection Diodes
- **CMOS IC FOR LOW POWER CONSUMPTION**
- **FULL TTL COMPATIBILITY OVER OPERATING TEMPERATURE RANGE**
  $V_{IL} = 0.8$ V
  $V_{IH} = 2.0$ V
- **WAVE SOLDERABLE**
- **RUGGED PACKAGE CONSTRUCTION**
- **END-STACKABLE**
- **WIDE VIEWING ANGLE**



Description

The HPDL-1414 is a smart 2.85 mm (0.112") four character, sixteen-segment, red GaAsP display. The on-board CMOS IC contains memory, ASCII decoder, multiplexing circuitry and drivers. The monolithic LED characters are magnified by an immersion lens which increases both character size and luminous intensity. The encapsulated dual-in-line package provides a rugged, environmentally sealed unit.

The HPDL-1414 incorporates many improvements over competitive products. It has a wide operating temperature range, very fast IC access time and improved ESD protection. The display is also fully TTL compatible, wave solderable and highly reliable. This display is ideally suited for industrial and commercial applications where a good-looking, easy-to-use alphanumeric display is required.

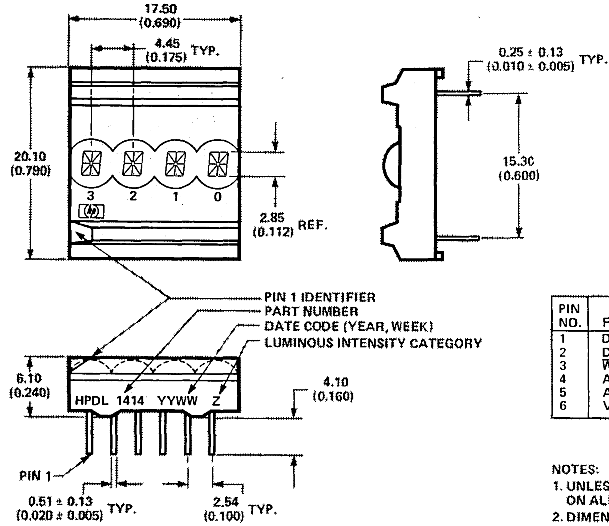
Typical Applications

- **PORTABLE DATA ENTRY DEVICES**
- **MEDICAL EQUIPMENT**
- **PROCESS CONTROL EQUIPMENT**
- **TEST EQUIPMENT**
- **INDUSTRIAL INSTRUMENTATION**
- **COMPUTER PERIPHERALS**
- **TELECOMMUNICATION INSTRUMENTATION**

Absolute Maximum Ratings

Supply Voltage, V_{CC} to Ground .... −0.5 V to 7.0 V
Input Voltage, Any Pin to Ground .... −0.5 V to V_{CC}+0.5 V
Free Air Operating
Temperature Range, T_A .... −40° C to +85° C
Relative Humidity (non-condensing) at 65° C 90%
Storage Temperature, T_S .... −40° C to +85° C
Maximum Solder Temperature, 1.59 mm (0.063 in.)
below Seating Plane, t<5 sec. .... 260° C

Package Dimensions



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	D_5 DATA INPUT	7	GND
2	D_4 DATA INPUT	8	D_0 DATA INPUT
3	$\overline{WR}$ WRITE	9	D_1 DATA INPUT
4	A_1 ADDRESS INPUTS	10	D_2 DATA INPUT
5	A_0 ADDRESS INPUTS	11	D_3 DATA INPUT
6	V_{CC}	12	D_6 DATA INPUT

NOTES:
1. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS 0.25 mm (0.010 in.).
2. DIMENSIONS IN mm (inches).

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage High	V_{IH}	2.0			V
Input Voltage Low	V_{IL}			0.8	V

DC Electrical Characteristics Over Operating Temperature Range

TYPICAL VALUES

Parameter	Symbol	Units	–40°C	–20°C	25°C	85°C	Test Condition
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	90	85	70	60	$V_{CC} = 5.0$ V
I_{CC} Blank	I_{CC} ($\overline{BL}$)	mA	1.8	1.5	1.2	1.1	$V_{CC} = 5.0$ V $\overline{BL} = 0.8$ V
Input Current, Max.	I_{IL}	μA	23	20	17	12	$V_{CC} = 5.0$ V $V_{IN} = 0.8$ V

GUARANTEED MAXIMUM VALUES

Parameter	Symbol	Units	25°C $V_{CC} = 5.0$ V	Maximum Over Operating Temperature Range $V_{CC} = 5.5$ V
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	90	130
I_{CC} Blank	I_{CC} ($\overline{BL}$)	mA	2.3	4.0
Input Current, Max.	I_{IL}	μA	30	50
Power Dissipation[3]	P_D	mW	450	715

Notes:
1. "%" illuminated in all four characters.
2. Measured at five seconds.
3. Power dissipation = $V_{CC} \cdot I_{CC}$ (10 seg.).

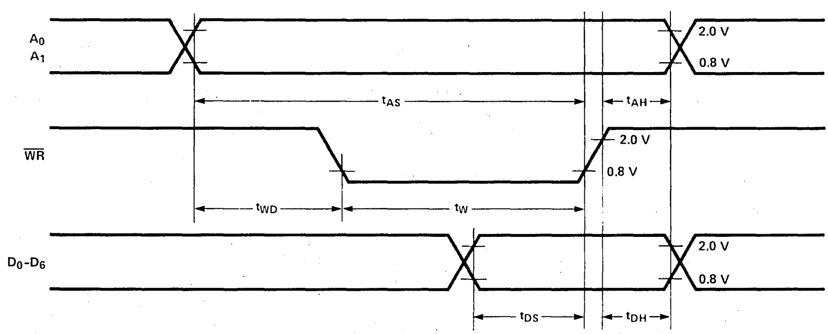
AC Timing Characteristics Over Operating Temperature Range at $V_{CC} = 4.5\ V$

Parameter	Symbol	−20°C t_{MIN}	25°C t_{MIN}	70°C t_{MIN}	Units
Address Setup Time	t_{AS}	90	115	150	ns
Write Delay Time	t_{WD}	10	15	20	ns
Write Time	t_W	80	100	130	ns
Data Setup Time	t_{DS}	40	60	80	ns
Data Hold Time	t_{DH}	40	45	50	ns
Address Hold Time	t_{AH}	40	45	50	ns
Access Time		130	160	200	ns
Refresh Rate		420-790	310-630	270-550	Hz

Optical Characteristics

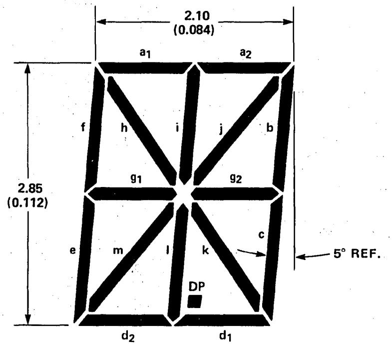
Parameter	Symbol	Test Condition	Min.	Typ.	Units
Peak Luminous Intensity per digit, 8 segments on (character average)	I_V Peak	$V_{CC} = 5.0\ V$ "✱" illuminated in all 4 digits.	0.4	1.0	mcd
Peak Wavelength	$\lambda peak$			655	nm
Dominant Wavelength	λ_d			640	nm
Off Axis Viewing Angle				±40	degrees
Digit Size				2.85	mm

Timing Diagram

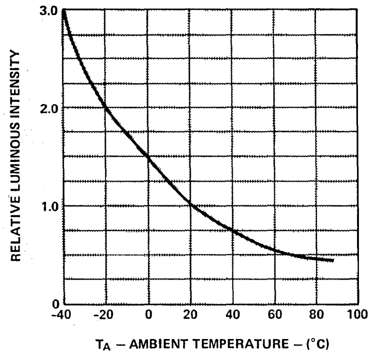


SOLID STATE DISPLAYS

Magnified Character Font Description



Relative Luminous Intensity vs. Temperature



Electrical Description

Figure 1 shows the internal block diagram of the HPDL-1414. It consists of two parts: the display LEDs and the CMOS IC. The CMOS IC consists of a four-word ASCII memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. Seven-bit ASCII data is stored in RAM. Since the display uses a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where D5=D6 in the ASCII RAM, the display character is blanked.

Data is loaded into the display through the DATA inputs (D_6-D_0), ADDRESS inputs (A_1-A_0), and WRITE ($\overline{WR}$). After a character has been written to memory, the IC decodes the ASCII data, drives the display and refreshes it without any external hardware or software.

The HPDL-1414 uses 12 pins to control the CMOS IC. Figure 1 shows the effect these inputs have on the display.

DATA INPUTS (D_0-D_6, pins 1, 2, 8-12)	Seven bit ASCII data is entered into memory via the DATA inputs.
ADDRESS INPUTS (A_1-A_0, pins 4 and 5)	Each location in memory has a distinct address. ADDRESS inputs enable the designer to select a specific location in memory to store data. Address 00 accesses the far right display location. Address 11 accesses the far left location.
WRITE ($\overline{WR}$, pin 3)	Data is written into the display when the $\overline{WR}$ input is low.
V_{CC} and GND (pins 6 and 7)	These pins supply power to the display.

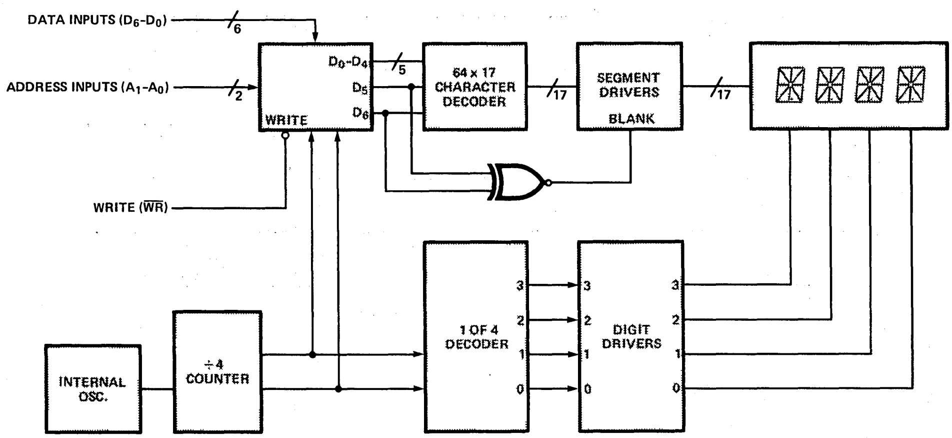


Figure 1. HPDL-1414 Internal Block Diagram

$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
L	L	H	b	b	b	b	b	b	b	NC	NC	B	NC
L	H	L	c	c	c	c	c	c	c	NC	C	NC	NC
L	H	H	d	d	d	d	d	d	d	D	NC	NC	NC
H	X	X	X	X	X	X	X	X	X	Previously Written Data			

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE

"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE

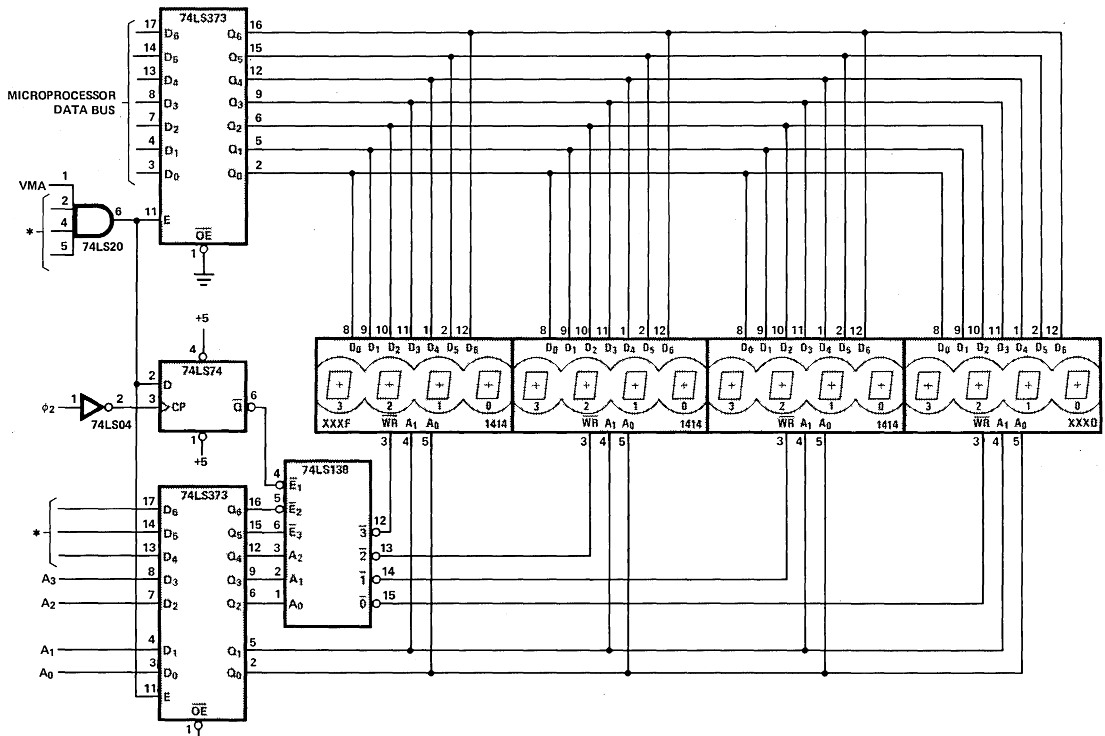
Figure 2. Write Truth Table

Using the HPDL-1414 with Microprocessors

Figures 3 and 4 show how to connect the HPDL-1414 to a Motorola 6800 or an Intel 8085. The major differences between the two circuits are:

1. The 6800 requires two latches to store the ADDRESS and ASCII DATA information to increase the address and data input hold times.
2. The 6800 requires a flip-flop to delay the display WRITE signal to increase the address input setup time.

ADDRESS inputs (A_1 and A_0) are connected to microprocessor addresses A_1 and A_0. A 74LS138 may be used to generate individual display WRITE signals. Higher order microprocessor address lines are connected to the 74LS138. The microprocessor write line must be wired to one of the active low enable inputs of the 74LS138. Both figures are formatted with address 0 being the far right display character.



*USED FOR HIGHER ORDER ADDRESS DECODING

Figure 3: Memory Mapped Interface for the 6800

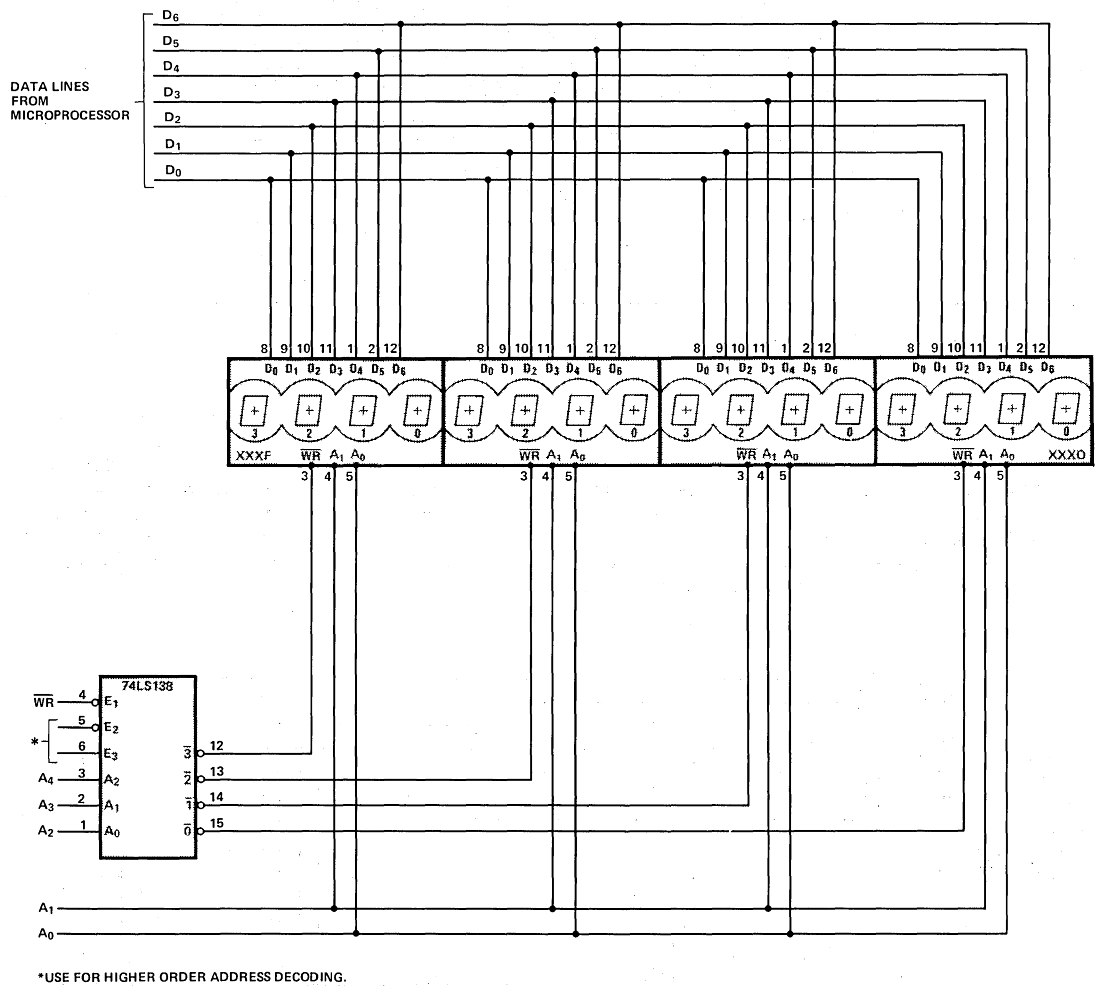


Figure 4. Memory Mapped Interface for the 8085

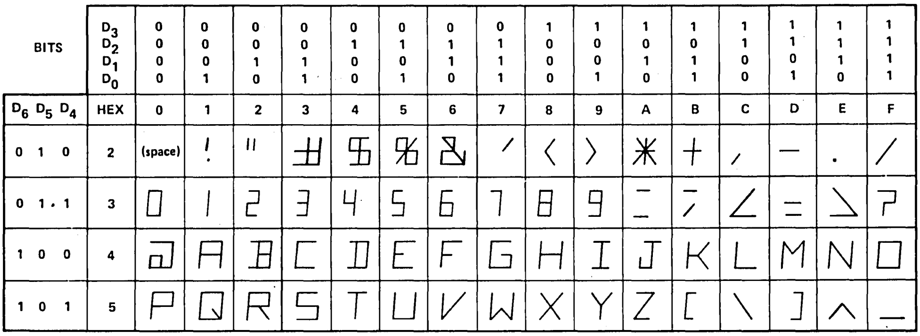


Figure 5. HPDL-1414 ASCII Character Set

Mechanical and Electrical Considerations

The HPDL-1414 is a 12 pin dual-in-line package which can be stacked horizontally and vertically to create arrays of any size. The HPDL-1414 is designed to operate continuously from −40°C to +85°C for all possible input conditions.

The HPDL-1414 is assembled by die attaching and wire bonding the four GaAsP/GaAs monolithic LED chips and the CMOS IC to a high temperature printed circuit board. An immersion lens is formed by placing the PC board assembly into a nylon lens filled with epoxy. A plastic cap creates an air gap to protect the CMOS IC. Backfill epoxy environmentally seals the display package. This package construction gives the display a high tolerance to temperature cycling.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results, standard CMOS handling precautions should be used. Prior to use, the HPDL-1414 should be stored in anti-static tubes or conductive material. A grounded conductive assembly area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic materials should be avoided since they may collect a static charge. Input current latchup is caused when the CMOS inputs are subjected either to a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{CC} ($V_{IN} > V_{CC}$), and when a high current is forced into the input.

Soldering and Post Solder Cleaning Instructions for the HPDL-1414

The HPDL-1414 may be hand soldered or wave soldered with SN63 solder. Hand soldering may be safely performed only with an electronically temperature-controlled and securely grounded soldering iron. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux or a water soluble organic acid (OA) flux can be used. The solder wave temperature should be 245°C ±5°C (473°F ±9°F), and the dwell in the wave should be set at 1 1/2 to 3 seconds for optimum soldering. Preheat temperature should not exceed 93°C (200°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical Genesolv DES, Baron Blakeslee Blaco-Tron TES or DuPont Freon TE can only be used. These solvents are azeotropes of trichlorotrifluoroethane FC-113 with low concentrations of ethanol (5%). The maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Solvents containing high concentrations of alcohols, pure alcohols, isopropanol or acetone should not be used as they will chemically attack the nylon lens. Solvents containing trichloroethane FC-111 or FC-112 and trichloroethylene (TCE) are not recommended.

An aqueous cleaning process is highly recommended. A saponifier, such as Kester Bio-kleen Formula 5799 or equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperature is 60°C (140°F). The maximum cumulative exposure of the HPDL-1414 to wash and rinse cycles should not exceed 15 minutes.

Optical Considerations/ Contrast Enhancement

The HPDL-1414 display uses a precision aspheric immersion lens to provide excellent readability and low off-axis distortion. The aspheric lens produces a magnified character height of 2.85 mm (0.112 in.) and a viewing angle of ±40 degrees. These features provide excellent readability at distances of up to 1.5 meters (4 feet).

Each HPDL-1414 display is tested for luminous intensity and marked with an intensity category on the side of the display package. To ensure intensity matching for multiple package applications, mixing intensity categories for a given panel is not recommended.

The HPDL-1414 display is designed to provide maximum contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60, Panelgraphic Dark Red 63, SGL Homalite H100-1650, Rohm and Haas 2423, Chequers Engraving 118, and 3M R6510. For further information on contrast enhancement, see Hewlett-Packard Application Note 1015.

HEWLETT PACKARD

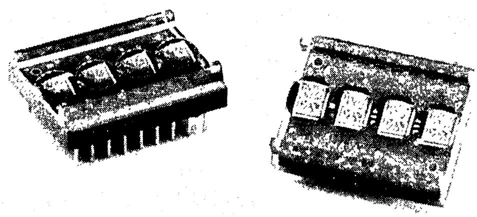
FOUR CHARACTER 4.1 mm (0.16 in.) SMART ALPHANUMERIC DISPLAY

HPDL-2416

TECHNICAL DATA JANUARY 1986

Features

- **SMART ALPHANUMERIC DISPLAY**
  Built-in RAM, ASCII Decoder, and LED Drive Circuitry
- **WIDE OPERATING TEMPERATURE RANGE**
  −40° C to +85° C
- **VERY FAST ACCESS TIME**
  160 ns
- **EXCELLENT ESD PROTECTION**
  Built-in Input Protection Diodes
- **CMOS IC FOR LOW POWER CONSUMPTION**
- **FULL TTL COMPATIBILITY OVER OPERATING TEMPERATURE RANGE**
  $V_{IL} = 0.8$ V
  $V_{IH} = 2.0$ V
- **WAVE SOLDERABLE**
- **RUGGED PACKAGE CONSTRUCTION**
- **END-STACKABLE**
- **WIDE VIEWING ANGLE**



Description

The HPDL-2416 has been designed to incorporate several improvements over competitive products. It has a wide operating temperature range, fast IC access time and improved ESD protection. The HPDL-2416 is fully TTL compatible, wave solderable, and highly reliable. This display is ideally suited for industrial and commercial applications where a good looking, easy-to-use alphanumeric display is required.

The HPDL-2416 is a smart 4.1 mm (0.16 in) four character, sixteen-segment red GaAsP display. The on-board CMOS IC contains memory, ASCII decoder, multiplexing circuitry, and drivers. The monolithic LED characters are magnified by an immersion lens which increases both character size and luminous intensity. The encapsulated dual-in-line package construction provides a rugged, environmentally sealed unit.

Typical Applications

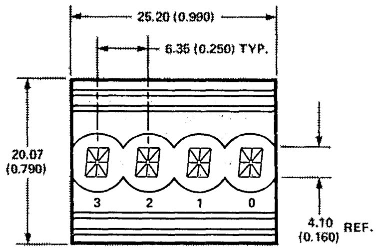
- **PORTABLE DATA ENTRY DEVICES**
- **MEDICAL EQUIPMENT**
- **PROCESS CONTROL EQUIPMENT**
- **TEST EQUIPMENT**
- **INDUSTRIAL INSTRUMENTATION**
- **COMPUTER PERIPHERALS**
- **TELECOMMUNICATION EQUIPMENT**

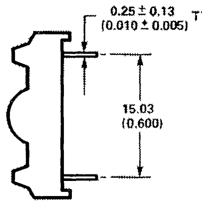
Absolute Maximum Ratings

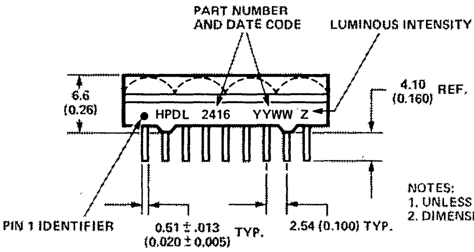
Supply Voltage, V_{CC} to Ground .... −0.5 V to 7.0 V
Input Voltage, Any Pin to Ground ... −0.5 V to V_{CC}+0.5 V
Free Air Operating
Temperature Range, T_A .... −40° C to +85° C
Relative Humidity (non-condensing) at 65° C 90%
Storage Temperature, T_S .... −40° C to +85° C
Maximum Solder Temperature, 1.59 mm (0.063 in.)
below Seating Plane, t < 5 sec. .... 260° C

SOLID STATE DISPLAYS

Package Dimensions







PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	$\overline{CE_1}$ CHIP ENABLE	10	GND
2	$\overline{CE_2}$ CHIP ENABLE	11	D_0 DATA INPUT
3	$\overline{CLR}$ CLEAR	12	D_1 DATA INPUT
4	CUE CURSOR ENABLE	13	D_2 DATA INPUT
5	$\overline{CU}$ CURSOR SELECT	14	D_3 DATA INPUT
6	$\overline{WR}$ WRITE	15	D_6 DATA INPUT
7	ADDRESS INPUT	16	D_5 DATA INPUT
8	ADDRESS INPUT	17	D_4 DATA INPUT
9	V_{CC}	18	$\overline{BL}$ DISPLAY BLANK

NOTES:
1. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS 0.254 mm (0.010 IN.)
2. DIMENSIONS IN mm (INCHES).

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage High	V_{IH}	2.0			V
Input Voltage Low	V_{IL}			0.8	V

DC Electrical Characteristics Over Operating Temperature Range

TYPICAL VALUES

Parameter	Symbol	Units	-40°C	-20°C	25°C	70°C	85°C	Test Condition
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	100	95	85	75	72	$V_{CC} = 5.0$ V
I_{CC} Cusor[2,3,4]	I_{CC} (CU)	mA	147	140	125	110	105	$V_{CC} = 5.0$ V
I_{CC} Blank	I_{CC} (BL)	mA	1.85		1.5		1.15	$V_{CC} = 5.0$ V, BL = 0.8 V
Input Current, Max.	I_{IL}	μA	20		17		14	$V_{CC} = 5.0$ V, $V_{IN} = 0.8$ V

GUARANTEED VALUES

Parameter	Symbol	Units	25° C $V_{CC} = 5.0$ V	Maximum Over Operating Temperature Range $V_{CC} = 5.5$ V
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	115	170
I_{CC} Cursor[2,3,4]	I_{CC} ($\overline{CU}$)	mA	165	232
I_{CC} Blank	I_{CC} ($\overline{BL}$)	mA	3.5	8.0
Input Current, Max.	I_{IL}	μA	30	40
Power Dissipation[5]	P_D	mW	575	910

Notes:
1. "%" illuminated in all four characters.
2. Measured at five seconds.
3. Cursor character is sixteen segments and DP on.
4. Cursor operates continuously over operating temperature range.
5. Power dissipation = $V_{CC} \cdot I_{CC}$ (10 seg.).

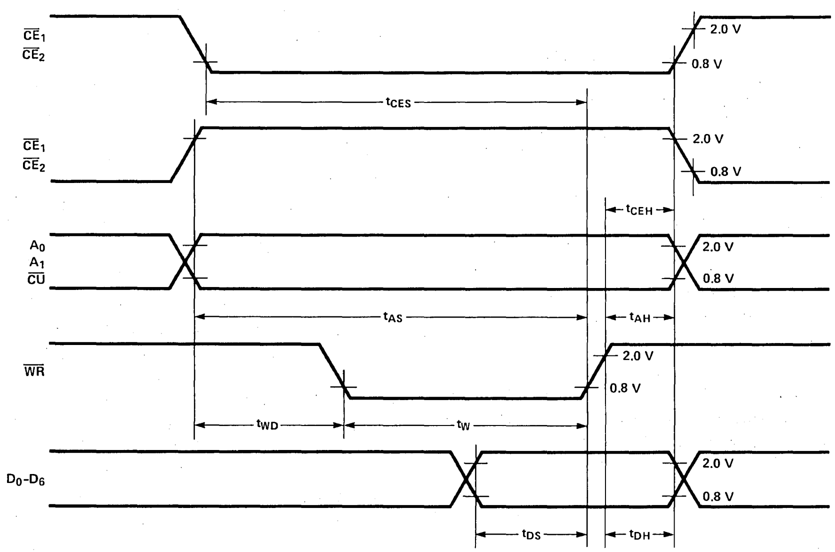
AC Timing Characteristics Over Operating Temperature Range at $V_{CC} = 4.5$ V

Parameter	Symbol	−20° C t_{MIN}	25° C t_{MIN}	70° C t_{MIN}	Units
Address Setup Time	t_{AS}	90	115	150	ns
Write Delay Time	t_{WD}	10	15	20	ns
Write Time	t_W	80	100	130	ns
Data Setup Time	t_{DS}	40	60	80	ns
Data Hold Time	t_{DH}	40	45	50	ns
Address Hold Time	t_{AH}	40	45	50	ns
Chip Enable Hold Time	t_{CEH}	40	45	50	ns
Chip Enable Setup Time	t_{CES}	90	115	150	ns
Clear Time	t_{CLR}	2.4	3.5	4.0	ms
Access Time		130	160	200	ns
Refresh Rate		420-790	310-630	270-550	Hz

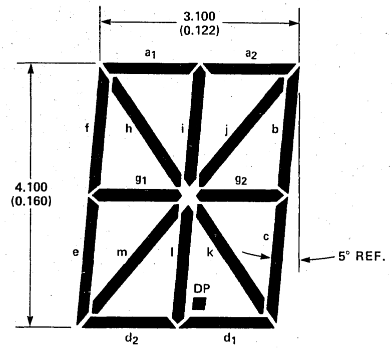
Optical Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Units
Peak Luminous Intensity per digit, 8 segments on (character average)	I_V Peak	$V_{CC} = 5.0$ V "✱" illuminated in all 4 digits.	0.5	1.25	mcd
Peak Wavelength	λpeak			655	nm
Dominant Wavelength	λ_d			640	nm
Off Axis Viewing Angle				±50	degrees
Digit Size				4.1	mm

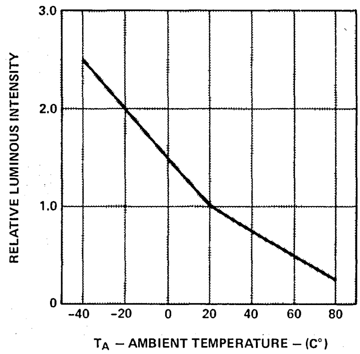
Timing Diagram



Magnified Character Font Description



Relative Luminous Intensity vs. Temperature



Electrical Description

Display Internal Block Diagram

Figure 1 shows the internal block diagram for the HPDL-2416 display. The CMOS IC consists of a four-word ASCII memory, a four-word cursor memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. For each display location, the cursor enable (CUE) selects whether the data from the ASCII RAM (CUE = 0) or the stored cursor (CUE = 1) is to be displayed. The cursor character is denoted by all sixteen segments and the DP ON. Seven-bit ASCII data is stored in RAM. Since the display utilizes a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where $D_5 = D_6$ in the ASCII RAM, the display character is blanked. The entire display is blanked when $\overline{BL} = 0$.

Data is loaded into the display through the data inputs (D_6-D_0), address inputs (A_1, A_0), chip enables ($\overline{CE}_1$, $\overline{CE}_2$), cursor select ($\overline{CU}$), and write ($\overline{WR}$). The cursor select ($\overline{CU}$) determines whether data is stored in the ASCII RAM ($\overline{CU}$ = 1) or cursor memory ($\overline{CU}$ = 0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 1$, the information on the data inputs is stored in the ASCII RAM at the location specified by the address inputs (A_1, A_0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 0$, information on the data input, D_0, is stored in the cursor at the location specified by the address inputs (A_1, A_0). If $D_0 = 1$, a cursor character is stored in the cursor memory. If $D_0 = 0$, a previously stored cursor character will be removed from the cursor memory.

If the clear input ($\overline{CLR}$) equals zero for one internal display cycle (4 ms minimum), the data in the ASCII RAM will be rewritten with zeroes and the display will be blanked. Note that the blanking input ($\overline{BL}$) must be equal to logical one during this time.

Data Entry

Figure 2 shows a truth table for the HPDL-2416 display. Setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its high state will enable data loading. The desired data inputs (D_6-D_0) and address inputs (A_1, A_0) as well as the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored into the display. Valid ASCII data codes are shown in Figure 3. The display accepts standard seven-bit ASCII data. Note that $D_6 = D_5$ for the codes shown in Figure 2. If $D_6 = D_5$ during the write cycle, then a blank will be stored in the display. Data can be loaded into the display in any order. Note that when $A_1 = A_0 = 0$, data is stored in the furthest right-hand display location.

Cursor Entry

As shown in Figure 2, setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its low state will enable cursor loading. The cursor character is indicated by the display symbol having all 16 segments and the DP ON. The least significant data input (D_0), the address inputs (A_1, A_0), the chip enables ($\overline{CE}_1$, $\overline{CE}_2$), and the cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored in the display. If D_0 is in a low state during the write cycle, then a cursor character will be removed at the indicated location. If D_0 is in a high state euring the write cycle, then a cursor character will be stored at the indicated location. The presence or absence of a cursor character does not affect the ASCII data stored at that location. Again, when $A_1 = A_0 = 0$, the cursor character is stored in the furthest right-hand display location.

All stored cursor characters are displayed if the cursor enable (CUE) is high. Similarly, the stored ASCII data words are displayed, regardless of the cursor characters, if the cursor enable (CUE) is low. The cursor enable (CUE) has no effect on the storage or removal of the cursor characters within the display. A flashing cursor is displayed by pulsing the cursor enable (CUE). For applications not requiring a cursor, the cursor enable (CUE) can be connected to ground and the cursor select ($\overline{CU}$) can be connected to V_{CC}. This inhibits the cursor function and allows only ASCII data to be loaded into the display.

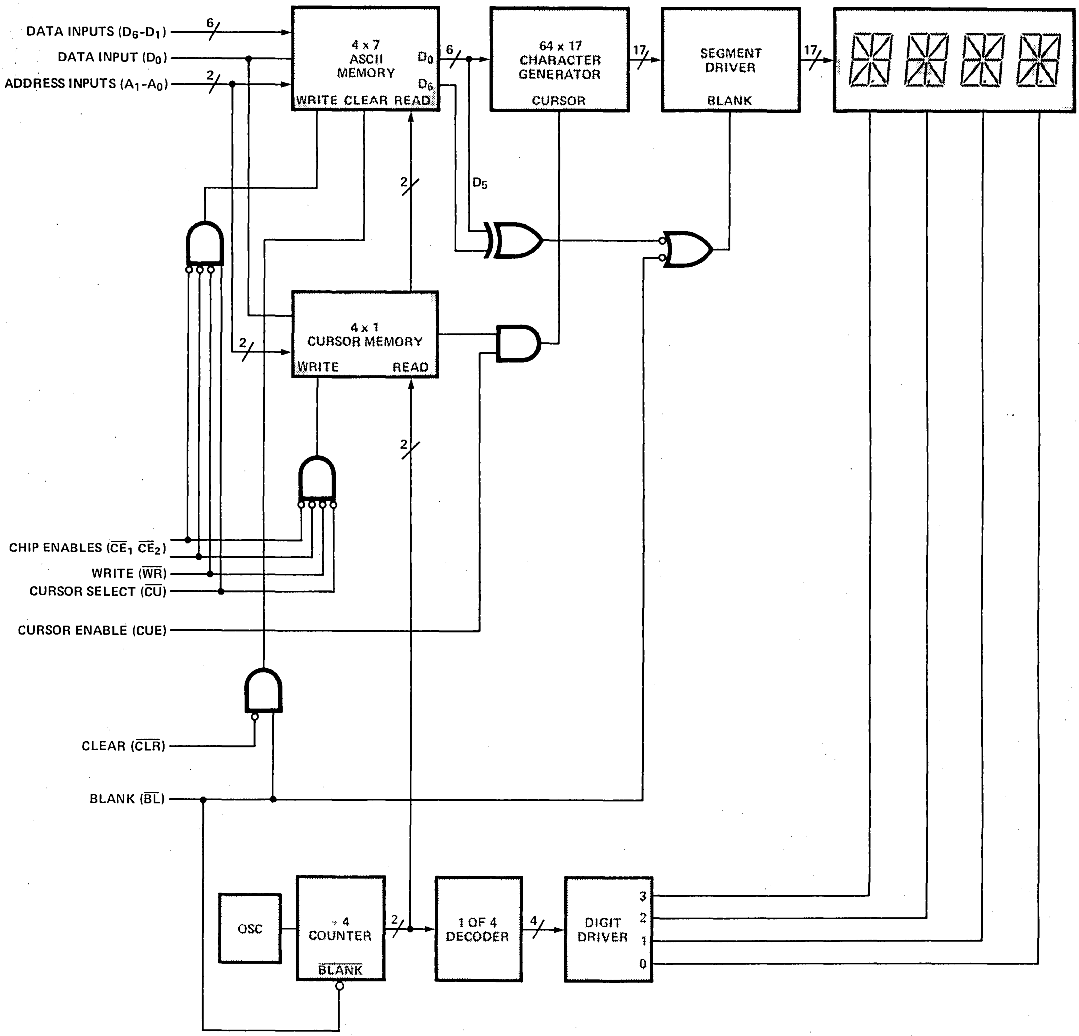


Figure 1. HPDL-2416 Internal Block Diagram

SOLID STATE DISPLAYS

Display Clear

As shown in Figure 2, the ASCII data stored in the display will be cleared if the clear ($\overline{CLR}$) is held low and the blanking input ($\overline{BL}$) is held high for 4 ms minimum. The cursor memory is not affected by the clear ($\overline{CLR}$) input. Cursor characters can be stored or removed even while the clear ($\overline{CLR}$) is low. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$). However, to ensure that all four display characters are cleared, $\overline{CLR}$ should be held low for 4 ms following the last write cycle.

Display Blank

As shown in Figure 2, the display will be blanked if the blanking input ($\overline{BL}$) is held low. Note that the display will be blanked regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) or write ($\overline{WR}$) inputs. The ASCII data stored in the display and the cursor memory are not affected by the blanking input. ASCII data and cursor data can be stored even while the blanking input ($\overline{BL}$) is low. Note that while the blanking input ($\overline{BL}$) is low, the clear ($\overline{CLR}$) function is inhibited. A flashing display can be obtained by applying a low frequency square wave to the blanking input ($\overline{BL}$). Because the blanking input ($\overline{BL}$) also resets the internal display multiplex counter, the frequency applied to the blanking input ($\overline{BL}$) should be much slower than the display multiplex rate. Finally, dimming of the display through the blanking input ($\overline{BL}$) is not recommended.

For further application information please consult Application Note 1026.

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
Write	L	X	X	H	L	L	L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
Data				-OR-				L	H	b	b	b	b	b	b	b	NC	NC	B	NC
Memory	X	H	X	H	L	L	L	H	L	c	c	c	c	c	c	c	NC	C	NC	NC
								H	H	d	d	d	d	d	d	d	D	NC	NC	NC
Disable	X	X	X	H	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written			
Data	X	X	X	H	X	H	X										Data			
Memory	X	X	X	H	H	X	X													
Write																				
Write	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	H	NC	NC	NC	⊠
Cursor								L	H	X	X	X	X	X	X	H	NC	NC	⊠	NC
								H	L	X	X	X	X	X	X	H	NC	⊠	NC	NC
								H	H	X	X	X	X	X	X	H	⊠	NC	NC	NC
Clear	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	L	NC	NC	NC	□
Cursor								L	H	X	X	X	X	X	X	L	NC	NC	□	NC
								H	L	X	X	X	X	X	X	L	NC	□	NC	NC
								H	H	X	X	X	X	X	X	L	□	NC	NC	NC
Disable	X	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written			
Cursor	X	X	X	L	X	H	X										Cursor			
Memory	X	X	X	L	H	X	X													

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE

"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE
⊠ = CURSOR CHARACTER (ALL SEGMENTS ON)

Figure 2a. Cursor/Data Memory Write Truth Table

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	DIG_3	DIG_2	DIG_1	DIG_0	
CUE	H	H	L	X	X	X	X	A	B	C	D	Display previously written data
	H	H	H	X	X	X	X	⊠	⊠	⊠	⊠	Display previously written cursor
Clear	H	L	X	X	X	X	X*	□	□	□	□	Clear data memory, cursor memory unchanged
	*NOTE: CLR should be held low for 4 ms following the last WRITE cycle to ensure all data is cleared.											
Blanking	L	X	X	X	X	X	X	□	□	□	□	Blank display, data and cursor memories unchanged.

Figure 2b. Displayed Data Truth Table

BITS	D_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	D_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	D_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	D_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
D_6 D_5 D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0	2	(space)	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
0 1 1	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

Figure 3. HPDL-2416 ASCII Character Set

Mechanical and Electrical Considerations

The HDPL-2416 is an 18 pin dual-in-line package that can be stacked horizontally and vertically to create arrays of any size. The HPDL-2416 is designed to operate continuously from −40° C to +85° C all possible input conditions including the illuminated cursor in all four character locations.

The HPDL-2416 is assembled by die attaching and wire bonding the four GaAsP/GaAs monolithic LED chips and the CMOS IC to a high temperature printed circuit board. An immersion lens is formed by placing the PC board assembly into a nylon lens filled with epoxy. A plastic cap creates an air gap to protect the CMOS IC. Backfill epoxy environmentally seals the display package. This package construction provides the display with a high tolerance to temperature cycling.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HPDL-2416 should be stored in anti-static tubes or conductive material. During assembly a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge build-up. Input current latchup is caused when the CMOS inputs are subjected either to a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{CC} ($V_{IN} > V_{CC}$) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{CC}. Voltages should not be applied to the inputs until V_{CC} has been applied to the display. Transient input voltages should be eliminated.

Soldering and Post Solder Cleaning Instructions for the HPDL-2416

The HPDL-2416 may be hand soldered or wave soldered with SN63 solder. Hand soldering may be safely performed only with an electronically temperature-controlled and securely grounded soldering iron. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be 245°C ±5°C (473°F ±9°F), and the dwell in the wave should be set at 1½ to 3 seconds for optimum soldering. Preheat temperature should not exceed 93°C (200°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical Genesolv DES, Baron Blakeslee Blaco-Tron TES or DuPont Freon TE can only be used. These solvents are azeotropes of trichlorotrifluoroethane FC-113 with low concentrations of ethanol (5%). The maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Solvents containing high concentrations of alcohols, pure alcohols, isopropanol or acetone should not be used as they will chemically attack the nylons lens. Solvents containing trichloroethane FC-111 or FC-112 and trichloroethylene (TCE) are not recommended.

An aqueous cleaning process is highly recommended. A saponifier, such as Kester-Bio-kleen Formula 5799 or equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperature is 60°C (140°F). The maximum cumulative exposure of the HPDL-2416 to wash and rinse cycles should not exceed 15 minutes.

Optical Considerations/ Contrast Enhancement

The HPDL-2416 display uses a precision aspheric immersion lens to provide excellent readability and low off-axis distortion. The aspheric lens produces a magnified character height of 4.1 mm (0.160 in.) and a viewing angle of $\pm 50°$. These features provide excellent readability at distances up to 2 metres (6 feet).

Each HPDL-2416 display is tested for luminous intensity and marked with an intensity category on the side of the display package. To ensure intensity matching for multiple package applications, mixing intensity categories for a given panel is not recommended.

The HPDL-2416 display is designed to provide maximum contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60, Panelgraphic Dark Red 63, SGL Homalite H100-1650, Rohm and Haas 2423, Chequers Engraving 118, and 3M R6510. For further information on contrast enhancement, see Hewlett-Packard Application Note 1015.

FOUR CHARACTER 3.8 mm (0.15 INCH) 5x7 ALPHANUMERIC DISPLAYS

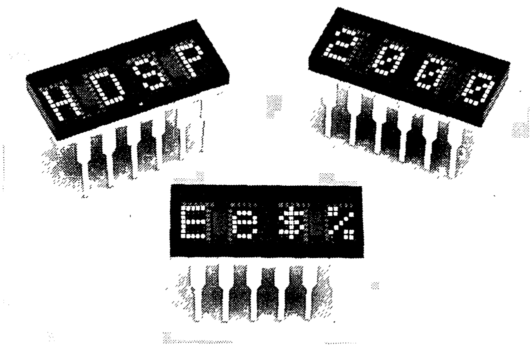
HEWLETT PACKARD

STANDARD RED HDSP-2000
YELLOW HDSP-2001
HIGH EFFICIENCY RED HDSP-2002
HIGH PERFORMANCE GREEN HDSP-2003

TECHNICAL DATA JANUARY 1986

Features

- FOUR COLORS
  Standard Red
  Yellow
  High Efficiency Red
  High Performance Green
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- COMPACT CERAMIC PACKAGE
- WIDE VIEWING ANGLE
- END STACKABLE FOUR CHARACTER PACKAGE
- TTL COMPATIBLE
- 5 x 7 LED MATRIX DISPLAYS FULL ASCII SET
- CATEGORIZED FOR LUMINOUS INTENSITY
- HDSP-2001/2003 CATEGORIZED FOR COLOR



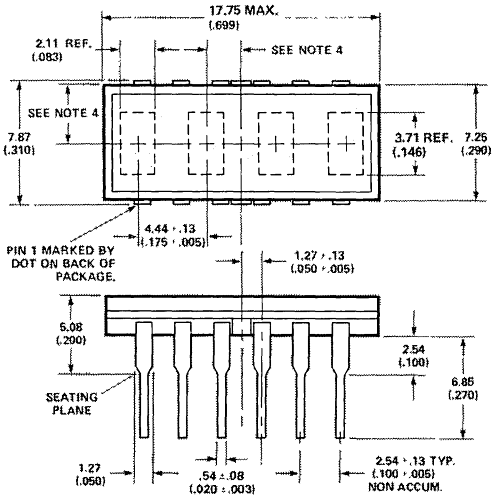
Typical Applications

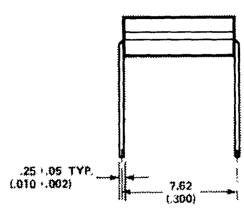
- INDUSTRIAL PROCESS CONTROL EQUIPMENT
- BUSINESS MACHINES
- PROGRAMMABLE LEGEND SWITCHES
- MEDICAL INSTRUMENTS
- MILITARY GROUND SUPPORT EQUIPMENT
- COMPUTER PERIPHERALS

Description

The HDSP-2000/-2001/-2002/-2003 series of displays are 3.8 mm (0.15 inch) 5 x 7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow, high efficiency red, and high performance green. Each four character cluster is contained in a 12 pin dual-in-line package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions





PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015")
3. LEAD MATERIAL IS COPPER ALLOY.
4. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

Absolute Maximum Ratings (HDSP-2000/-2001/-2002/-2003)

Supply Voltage V_{CC} to Ground .... —0.5V to 6.0V
Inputs, Data Out and V_B .... —0.5V to V_{CC}
Column Input Voltage, V_{COL} .... —0.5V to +6.0V
Free Air Operating
Temperature Range, T_A[1,2] .... —20° C to +85° C
Storage Temperature Range, T_S ..... —55° C to +100° C
Maximum Allowable Power Dissipation
at T_A = 25° C[1,2,3] .... 1.24 Watts
Maximum Solder Temperature 1.59 mm (0.063 in)
Below Seating Plane t < 5 sec .... 260° C

Recommended Operating Conditions (HDSP-2000/-2001/-2002/-2003)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2000	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On, HDSP-2001/-2002/-2003	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range[1,2]	T_A	-20		85	°C	2

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V, V_{COL} = 3.5V, All SR Stages = Logical 1	V_B = 0.4V			500	μA	4
Column Current at any Column Input		I_{COL}		V_B = 2.4V		335	410	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V	
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	μA	
	Data In	I_{IH}				10	40	μA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	μA	
	Data In	I_{IL}				-250	-400	μA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF 15 LEDs on per character, V_B = 2.4V			0.72		W	2
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				25		°C/W/ Device	2

*All typical values specified at V_{CC} = 5.0V and T_A = 25° C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85° C ambient is possible provided the following conditions are met. The junction should not exceed 125° C T_J and the case temperature (as measured at pin 1 or the back of the display) should not exceed 100° C T_C.
2. The device should be derated linearly above 50°C at 16.7 mW/° C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 35° C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

Optical Characteristics

STANDARD RED HDSP-2000

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_i = 25° C[6], V_B = 2.4V	105	200		μcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2001

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_i = 25° C[6], V_B = 2.4V	400	750		μcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2002

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_i = 25° C[6], V_B = 2.4V	400	1430		μcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

HIGH PERFORMANCE GREEN HDSP-2003

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_i = 25° C[6], V_B = 2.4V	850	1550		μcd	3
Peak Wavelength	λ_{PEAK}			568		nm	
Dominant Wavelength[5,7]	λ_d			574		nm	

*All typical values specified at V_{CC} = 5.0V and T_A = 25° C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2001/-2003 are categorized for color with the color category designated by a number code on the bottom of the package.
6. T_i refers to the initial case temperature of the device immediately prior to the light measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:
   L_v (cd/m2) = I_v (Candela)/A (Metre)2
   L_v (Footlamberts) = πI_v (Candela)/A (Foot)2
   A = 5.3 x 10^{-8} M2 = 5.8 x 10^{-7} (Foot)2

Electrical Description

The HDSP-200X series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features DATA IN and DATA OUT terminals arrayed for easy PC board interconnection. DATA OUT represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5 x 7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

In the normal mode of operation, input data for digit 4 column 1 is loaded into the 7 on-board shift register locations 1 through 7. Column 1 data for digits 3, 2 and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5\,(t+T)}$$

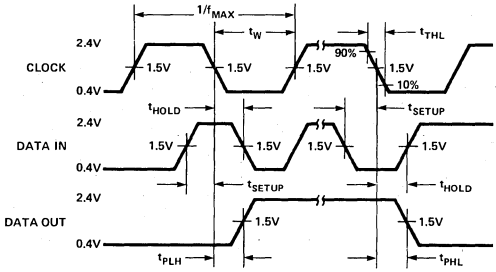
The time frame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time t + T of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain t << T. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics HDSP-2000/-2001/-2002/-2003 (T_A = -20° C to +85° C)

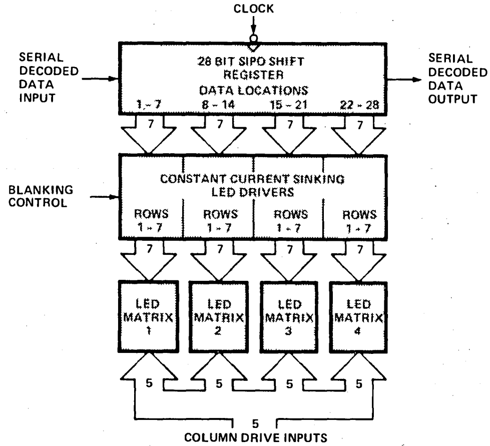


Figure 5. Block Diagram of HDSP-2000/-2001/-2002/-2003

Mechanical and Thermal Considerations

The HDSP-2000/-2001/-2002/-2003 are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 60° C/watt/device is possible up to ambient temperature of 50° C. For operation above 50° C, the maximum device dissipation should be derated linearly at 16.7 mW/° C (see Figure 2). With an improved thermal design, operation at higher ambient temperatures without derating is possible.

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.4V for the HDSP-2000 and 2.75V for the HDSP-2001/-2002/-2003. Also, the average drive current can be decreased through pulse width modulation of V_B. Please refer to HP Application Note 1016 for further information.

The HDSP-2000/-2001/-2002/-2003 displays have glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 6. Additional information on filtering and constrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

Display Color	Ambient Lighting Dim	Moderate	Bright
HDSP-2000 Std. Red	Panelgraphic Dark Red 63, Ruby Red 60, Chequers Red 118, Plexiglass 2423		
HDSP-2001 (Yellow)	Panelgraphic Yellow 27, Chequers Amber 107	Polaroid HNCP37, 3M Light Control Film, Panelgraphic Gray 10	Polaroid HNCP10-Glass, Marks Polarized MPC-0301-8-10, Note 1
HDSP-2002 (HER)	Panelgraphic Ruby Red 60, Chequers Red 112	Chequers Grey 105	Polaroid HNCP10-Glass, Marks Polarized MPC-0201-2-22
HDSP-2003 (HP Green)	Panelgraphic Green 48, Chequers Green 107		Polaroid HNCP10-Glass, Marks Polarized MPC-0101-5-12

Note: 1. Optically coated circular polarized filters, such as Polaroid HNCP10.

Figure 6. Contrast Enhancement Filters

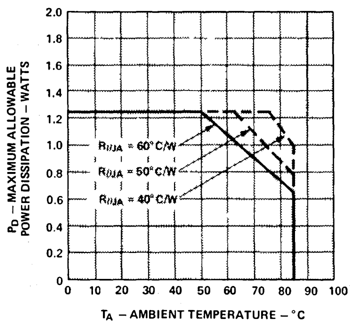


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

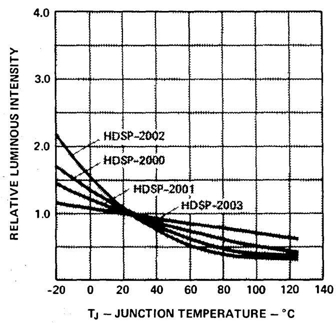


Figure 3. Relative Luminous Intensity vs. Temperature

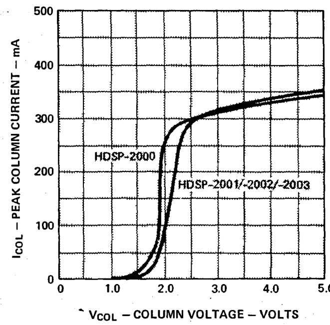


Figure 4. Peak Column Current vs. Column Voltage

HEWLETT PACKARD

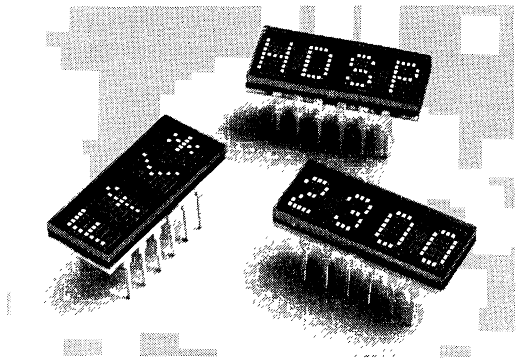
FOUR CHARACTER 5.0 mm (0.20 INCH) 5x7 ALPHANUMERIC DISPLAYS

STANDARD RED HDSP-2300
YELLOW HDSP-2301
HIGH EFFICIENCY RED HDSP-2302
HIGH PERFORMANCE GREEN HDSP-2303

TECHNICAL DATA JANUARY 1986

Features

- FOUR COLORS
  Standard Red
  Yellow
  High Efficiency Red
  High Performance Green
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- COMPACT CERAMIC PACKAGE
- WIDE VIEWING ANGLE
- END STACKABLE FOUR CHARACTER PACKAGE
- TTL COMPATIBLE
- 5 x 7 LED MATRIX DISPLAYS FULL ASCII SET
- CATEGORIZED FOR LUMINOUS INTENSITY
- HDSP-2301/2303 CATEGORIZED FOR COLOR



Typical Applications

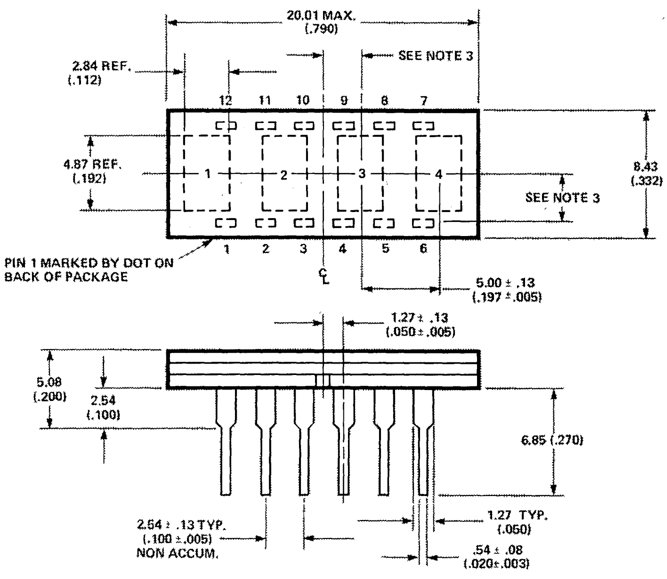
- AVIONICS
- BUSINESS MACHINES
- MEDICAL INSTRUMENTS
- INDUSTRIAL PROCESS CONTROL EQUIPMENT
- COMPUTER PERPHERALS

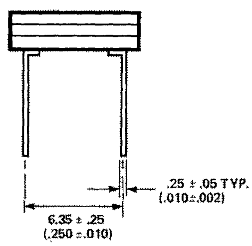
Description

The HDSP-2300/-2301/-2302/-2303 series of displays are 5.0 mm (0.20 inch) 5 x 7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow, high efficiency red, and high performance green.

Each four character cluster is contained in a 12 pin dual-in-line package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions





PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015")
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

Absolute Maximum Ratings (HDSP-2300/-2301/-2302/-2303)

Supply Voltage V_{CC} to Ground .... —0.5V to 6.0V
Inputs, Data Out and V_B .... —0.5V to V_{CC}
Column Input Voltage, V_{COL} .... —0.5V to +6.0V
Free Air Operating
Temperature Range, T_A[1,2] .... —20° C to +85° C
Storage Temperature Range, T_S ..... —55° C to +100° C

Maximum Allowable Power Dissipation
at T_A = 25° C[1,2,3]
HDSP-2300 .... 1.24 Watts
HDSP-2301/-2302/-2303 .... 1.46 Watts
Maximum Solder Temperature is 1.59 mm (0.063 in)
Below Seating Plane t < 5 sec .... 260° C

Recommended Operating Conditions (HDSP-2300/-2301/-2302/-2303)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2300	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On HDSP-2301/-2302/-2303	V_{COL}	2.75		3.5	V	7
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range[1,2]	T_A	-20		85	°C	3, 5

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

STANDARD RED HDSP-2300

Description	Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current	I_{CC}	V_{CC} = 5.25V V_{CLOCK} = V_{DATA} = 2.4V All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
			V_B = 2.4V		73	95	mA	
Column Current at any Column Input	I_{COL}	V_{CC} = 5.25 V V_{COL} = 3.5V	V_B = 0.4V			500	µA	4
Column Current at any Column Input	I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		335	410	mA	
V_B, Clock or Data Input Threshold High	V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V	
V_B, Clock or Data Input Threshold Low	V_{IL}					0.8	V	
Input Current Logical 1 — V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA	
Input Current Logical 1 — Data In	I_{IH}				10	40	µA	
Input Current Logical 0 — V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA	
Input Current Logical 0 — Data In	I_{IL}				-250	-400	µA	
Data Out Voltage	V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
	V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**	P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF 15 LEDs on per character, V_B = 2.4V			0.72		W	2
Thermal Resistance IC Junction-to-Case	$R\theta_{J-C}$				25		°C/W/ Device	2

*All typical values specified at V_{CC} = 5.0V and T_A = 25° C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85°C ambient is possible provided the following conditions are met. The junction temperature should not exceed 125° C T_J and the case temperature (as measureed at pin 1 or the back of the display) should not exceed 100° C T_C.
2. The HDSP-2300 should be derated linearly above 50° C at 16.7 mW/° C. The HDSP-2301/-2302/-2303 should be derated linearly above 37° C at 16.7 mW/° C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 35°** C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

YELLOW HDSP-2301/HIGH EFFICIENCY RED HDSP-2302/HIGH PERFORMANCE GREEN HDSP-2303

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	$V_{CC} = 5.25V$ $V_{CLOCK} = V_{DATA} = 2.4V$ All SR Stages = Logical 1	$V_B = 0.4V$		45	60	mA	
				$V_B = 2.4V$		73	95	mA	
Column Current at any Column Input		I_{COL}	$V_{CC} = 5.25V$ $V_{COL} = 3.5V$	$V_B = 0.4V$			500	μA	7
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	$V_B = 2.4V$		380	520	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	$V_{CC} = V_{COL} = 4.75V$		2.0			V	
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V	
Input Current Logical 1	V_B, Clock	I_{IH}	$V_{CC} = 5.25V$, $V_{IH} = 2.4V$			20	80	μA	
	Data In	I_{IH}				10	40	μA	
Input Current Logical 0	V_B, Clock	I_{IL}	$V_{CC} = 5.25V$, $V_{IL} = 0.4V$			-500	-800	μA	
	Data In	I_{IL}				-250	-400	μA	
Data Out Voltage		V_{OH}	$V_{CC} = 4.75V$, $I_{OH} = -0.5$ mA, $I_{COL} = 0$ mA		2.4	3.4		V	
		V_{OL}	$V_{CC} = 4.75V$, $I_{OL} = 1.6$ mA, $I_{COL} = 0$ mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$, 17.5% DF 15 LEDs on per character, $V_B = 2.4V$			0.78		W	5
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				25		°C/W/ Device	5

Optical Characteristics

STANDARD RED HDSP-2300

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	130	300		μcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2301

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	650	1140		μcd	6
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2302

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	650	1430		μcd	6
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

HIGH PERFORMANCE GREEN HDSP-2303

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	1280	2410		μcd	6
Peak Wavelength	λ_{PEAK}			568		nm	
Dominant Wavelength[5,7]	λ_d			574		nm	

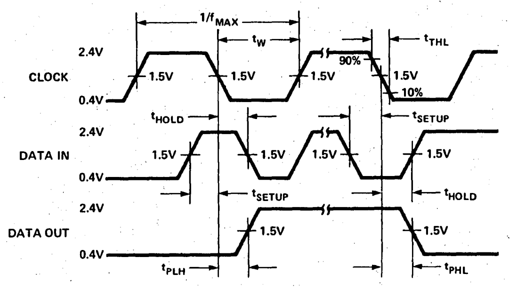
*All typical values specified at $V_{CC} = 5.0V$ and $T_A = 25°C$ unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2301/-2303 are categorized for color with the color category designated by a number code on the bottom of the package.
6. T_i refers to the initial case temperature of the device immediately prior to the light measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:
   L_v (cd/m^2) = I_v (Candela)/A (Metre)^2
   L_v (Footlamberts) = πI_v (Candela)/A (Foot)^2
   $A = 5.3 \times 10^{-8}$ M^2 = 5.8×10^{-7} (Foot)^2

SOLID STATE DISPLAYS



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics HDSP-2300/-2301/-2302/-2303 (T_A = -20° C to +85° C)

HDSP-2300

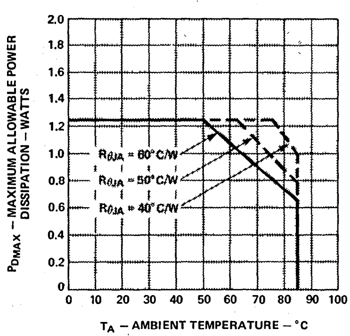


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

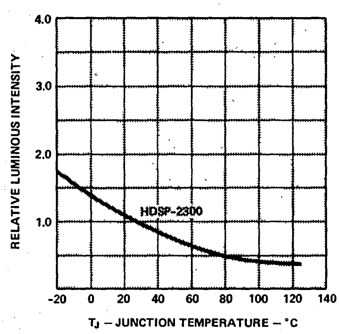


Figure 3. Relative Luminous Intensity vs. Temperature

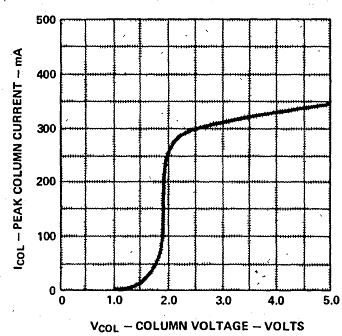


Figure 4. Peak Column Current vs. Column Voltage

HDSP-2301/-2302/-2303

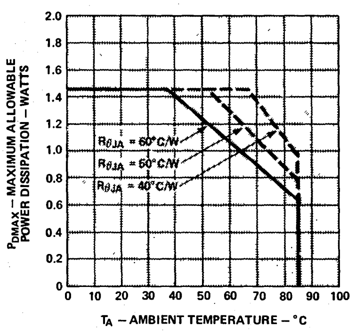


Figure 5. Maximum Allowable Power Dissipation vs. Temperature

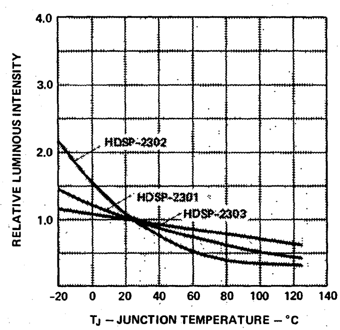


Figure 6. Relative Luminous Intensity vs. Temperature

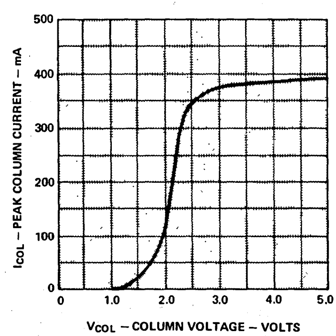


Figure 7. Peak Column Current vs. Column Voltage

Electrical Description

The HDSP-230X series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electonics design. Each four character display module features DATA IN and DATA OUT terminals arrayed for easy PC board interconnection. DATA OUT represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5 x 7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

In the normal mode of operation, input data for digit 4 column 1 is loaded into the 7 on-board shift register locations 1 through 7. Column data for digits 3, 2, and 1 is similiarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode the load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5\,(t+T)}$$

The time frame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time t + T of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain t << T. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.

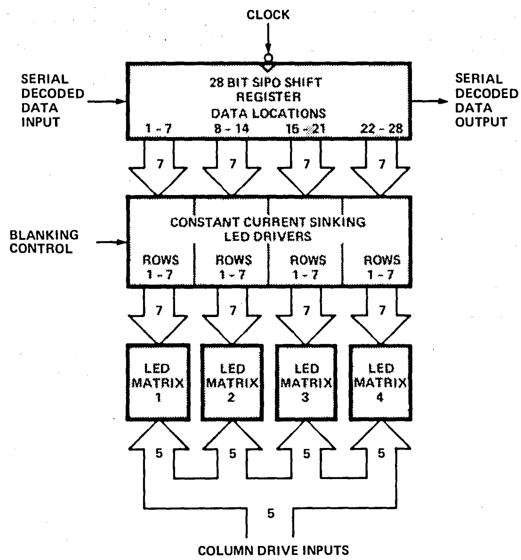


Figure 8. Block Diagram of HDSP-2300/-2301/-2302/-2303

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2000 Std. Red	Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Plexiglass 2423		
HDSP-2001 (Yellow)	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10	Polaroid HNCP10-Glass Marks Polarized MPC-0301-8-10 Note 1
HDSP-2002 (HER)	Panelgraphic Ruby Red 60 Chequers Red 112	Chequers Grey 105	Polaroid HNCP10-Glass Marks Polarized MPC-0201-2-22
HDSP-2003 (HP Green)	Panelgraphic Green 48 Chequers Green 107		Polaroid HNCP10-Glass Marks Polarized MPC-0101-5-12

Note: 1. Optically coated circular polarized filters, such as Polaroid HNCP10.

Figure 9. Contrast Enhancement Filters

Mechanical and Thermal Considerations

The HDSP-2300/-2301/-2302/-2303 are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. The HDSP-2301/-2302/-2303 utilize a high output current IC to provide excellent readability in bright ambient lighting. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 60° C/watt/device is possible up to ambient temperature of 37° C. For operation above 37° C, the maximum device dissipation should be derated linearly at 16.7 mW/° C (see Figure 5). With an improved thermal design, operation at higher ambient temperatures without derating is possible. Please refer to HP Application Note 1016 for further information.

The HDSP-2300 uses a lower power IC, yet achieves excellent readabilty in indoor ambient lighting. Full power operation up to T_A = 50° C (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) is possible by providing a total thermal resistance from IC junction to ambient of 60° C/watt/device maximum. For operation above 50° C, the maximum device dissipation should be derated at 16.7 mW/° C/device (see Figure 2).

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.6V for the HDSP-2300 and 2.75V for the HDSP-2301/-2302/-2303. Also, the average drive current can be decreased through pulse width modulation of V_B.

The HDSP-2300/-2301/-2302/-2303 displays have glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 9. Additional information on filtering and constrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

NOTE:
The HDSP-2301/-2302/-2303 are available in high intensity categories suitable for some applications where direct sunlight viewing is required. For information on displays and filters for sunlight viewable applications, contact your field salesman.

HEWLETT PACKARD

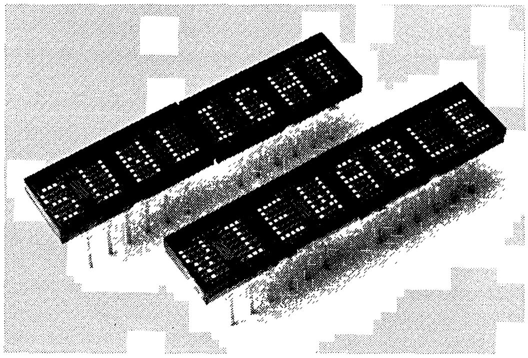
FOUR CHARACTER 5.0 mm (0.20 INCH) 5X7 ALPHANUMERIC DISPLAY FOR SUNLIGHT VIEWABLE APPLICATIONS

YELLOW HDSP-2381
HIGH EFFICIENCY RED HDSP-2382
HIGH PERFORMANCE GREEN HDSP-2383

TECHNICAL DATA JANUARY 1986

Features

- **SUNLIGHT VIEWABLE UP TO 10,000 FOOTCANDLES**
- **THREE COLORS**
  Yellow
  High Efficiency Red
  High Performance Green
- **COMPACT CERAMIC PACKAGE**
- **WIDE VIEWING ANGLE**
- **END AND ROW STACKABLE**
- **5X7 LED MATRIX DISPLAYS FULL ASCII SET**
- **INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS**
- **TTL COMPATIBLE**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
- **HDSP-2381/-2383 CATEGORIZED FOR COLOR**



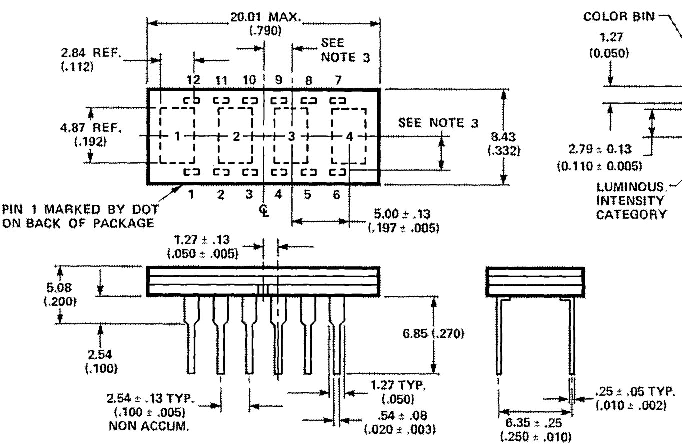
Typical Applications

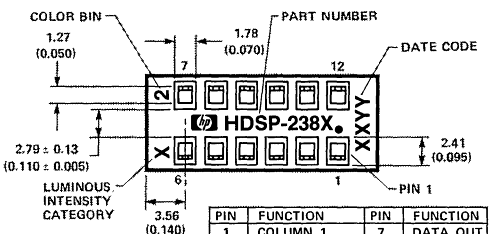
- **COMMERCIAL AVIONICS — Cockpit displays, fuel management and airborne navigational radio systems**
- **TEST AND GROUND SUPPORT FIELD EQUIPMENT**
- **INDUSTRIAL VEHICLES AND EQUIPMENT**
- **OTHER APPLICATIONS REQUIRING READABILITY IN DIRECT SUNLIGHT**

Description

The HDSP-2381/-2382/-2383 displays are designed for use in applications requiring readability in bright sunlight. With a proper contrast enhancement filter and heat sinking, these displays are readable in sunlight ambients up to 10,000 foot-candles. The character font is a 5.0 mm (0.20 inch) 5X7 LED array for displaying alphanumeric information. These devices are available in yellow, high efficiency red, and high performance green. Each four character cluster is packaged in a 12-pin dual-in-line package. An on-board serial-in-parallel-out 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions





PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	CLOUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ± .38 mm (± .015").
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ± .13 mm (± .005").

SOLID STATE DISPLAYS

Absolute Maximum Ratings (HDSP-2381/-2382/-2383)

Supply Voltage V_{CC} to Ground .... −0.5 V to +6.0 V
Inputs, Data Out and V_B .... −0.5 V to V_{CC}
Column Input Voltage, V_{COL} .... −0.5 V to +6.0 V
Free Air Operating Temperature
Range, T_A[1,2] .... −20° C to +85° C
Storage Temperature Range, T_S ...... −55° C to +100° C

Maximum Allowable Package Dissipation
at T_A = 25° C[1,2,3]
HDSP-2381/-2382/-2383 .... 1.74 Watts
Maximum Solder Temperature 1.59 mm (0.063 in)
Below Seating Plane t<5 sec .... 260° C

Recommended Operating Conditions Over Operating Temperature Range (−20° C to +85° C) (HDSP-2381/-2382/-2383)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2381/-2382/-2383	V_{COL}	2.75		3.5	V	4
Setup Time	t_{SETUP}	70	45		ns	1
Hold Time	t_{HOLD}	30	0		ns	1
Width of Clock	$t_{W(CLOCK)}$	75			ns	1
Clock Frequency	f_{CLOCK}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range[1,2]	T_A	-20		85	°C	3

Electrical Characteristics Over Operating Temperature Range (−20° C to +85° C)

YELLOW HDSP-2381/HIGH EFFICIENCY RED HDSP-2382/HIGH PERFORMANCE GREEN HDSP-2383

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		50	60	mA	
				V_B = 2.4V		90	100	mA	
Column Input Current (any Column Pin)		I_{COL}	V_{CC} = 5.25 V, V_{COL} = 3.5V	V_B = 0.4V			500	μA	4
Column Input Current (any Column Pin)		I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		550	653	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V	
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	μA	
	Data In	I_{IH}				10	40	μA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	μA	
	Data In	I_{IL}				-250	-400	μA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF 15 LEDs on per character, V_B = 2.4V			1.05		W	2
Thermal Resistance IC Junction-to-Pin		$R\theta_{J-PIN}$				10		°C/W/ Device	2

*All typical values specified at V_{CC} = 5.0V and T_A = 25° C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:
1. The HDSP-2381/-2382/-2383 should be derated linearly above 50° C at 24.3 mW/° C, based on a device mounted such that the thermal resistance from IC junction to ambient is 45° C/W (10° C/W $R\theta_{J-PIN}$ and 35° C/W$_{PIN-A}$). See Figure 2 for power deratings based on lower thermal resistance mounting.
2. Operation above 50° C ambient is possible provided the following conditions are met. The junction temperature should not exceed 125° C (T_J) and the temperature at the pins should not exceed 100° C (T_C).
3. Maximum allowable dissipation is derived from V_{CC} = 5.25 V, V_B = 2.4 V, V_{COL} = 3.5 V, 20 LEDs on per character, 20% DF.

Optical Characteristics

YELLOW HDSP-2381

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPEAK}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	2400	3400		μcd	3
Dominant Wavelength[5,7]	λ_d			585		nm	
Peak Wavelength	λ_{PEAK}			583		nm	

HIGH EFFICIENCY RED HDSP-2382

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPEAK}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	1920	2850		μcd	3
Dominant Wavelength[7]	λ_d			626		nm	
Peak Wavelength	λ_{PEAK}			635		nm	

HIGH PERFORMANCE GREEN HDSP-2383

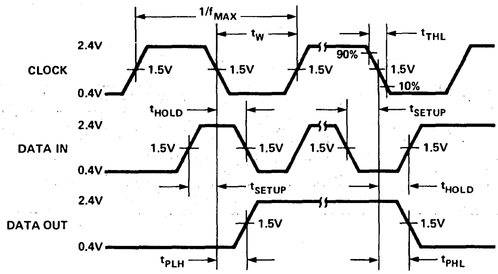
Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPEAK}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	2400	3000		μcd	3
Dominant Wavelength[5,7]	λ_d			574		nm	
Peak Wavelength	λ_{PEAK}			568		nm	

*All typical values specified at $V_{CC} = 5.0V$ and $T_A = 25°C$ unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. These LED displays are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2381/-2383 are categorized for color with the color category designated by a number code on the bottom of the package.
6. T_I refers to the initial case temperature of the device immediately prior to the light measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:
   L_v (cd/m^2) = I_v (Candela)/A (Metre)^2
   L_v (Footlamberts) = πI_v (Candela)/A (Foot)^2
   $A = 5.3 \times 10^{-8}\ M^2 = 5.8 \times 10^{-7}$ (Foot)^2



Parameter	Condition	Min.	Typ.	Max.	Units
f_{CLOCK} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	$C_L = 15pF$ $R_L = 2.4K\Omega$			125	ns

Figure 1. Switching Characteristics HDSP-2381/-2381/-2383 ($T_A = -20°$ C to +85° C).

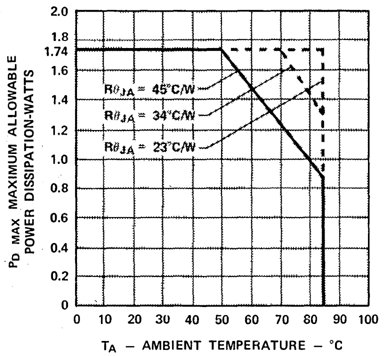


Figure 2. Maximum Allowable Power Dissipation vs. Ambient Temperature as a Function of Thermal Resistance IC Junction to Ambient Air. $R\theta_{JA}$.

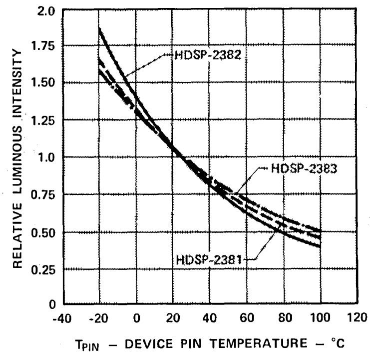


Figure 3. Relative Luminous Intensity vs. Device Substrate (PIN) Temperature.

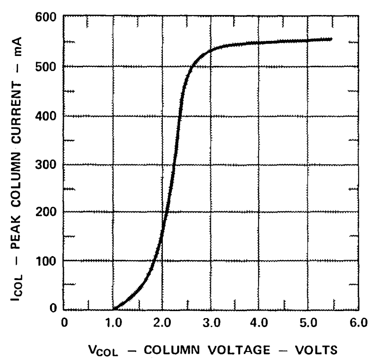


Figure 4. Peak Column Current vs. Column Voltage.

Electrical Description

The electrical configuration of the HDSP-238X series alphanumeric displays allows for an effective interface to a microprocessor data source. Each display device contains four 5x7 LED dot matrix characters and two integrated circuits, as diagrammed in Figure 5. The two integrated circuits, with TTL compatible inputs, form a 28 bit serial-in-parallel-out column data shift register. The data input is connected to shift register bit position 1 and the data output is connected to bit position 28. The shift register parallel outputs are connected to constant current sinking LED row drivers that sink a nominal 19.6 mA. A logic 1 stored in the shift register enables the corresponding LED row driver and a logic 0 stored in the shift register disables the corresponding LED row driver.

Column data is loaded into an on-board shift register with high to low transitions of the Clock input. To load character information into the display, column data for the character 4 is loaded first and the column data for character 1 is loaded last in the following manner: The 7 data bits for column 1, character 4 are loaded into the on-board shift register. Next, the 7 data bits for column 1, character 3 are loaded into the on-board shift register, shifting the character 4 data over one character position. This process is repeated until all 28 bits of column data are loaded into the on-board shift register. Then, the column 1 input is energized to illuminate column 1's in all four characters. The procedure is repeated for columns 2, 3, 4 and 5.

The light output of the display may be dimmed by pulse width modulating (PWM) the blanking input V_B, with the brightness being in direct proportion to the LED on-time. When the blanking input is at logic high the display is illuminated and when the blanking input is at logic low the display is blanked. These displays may be dimmed by PWM on the order of a 2000:1 change in brightness while maintaining light output and color uniformity between characters.

The LED on-time duty factor, DF, may be determined when the time to load the on-board shift register, t, the column on-time without blanking, T, and the time display is blanked, TB, are known:

$$DF = \frac{T}{5(t + T + TB)}$$

Where: $5(t + T + TB)$ is 1/column refresh rate

The column driver inputs should be strobed at a refresh rate of 100 Hz or faster to achieve a flicker free display. The value of DF approaches 20% when TB = 0 and t is very small compared to T.

For information on interfacing these displays to microprocessor data sources and techniques for intensity control, see Application Note 1016.

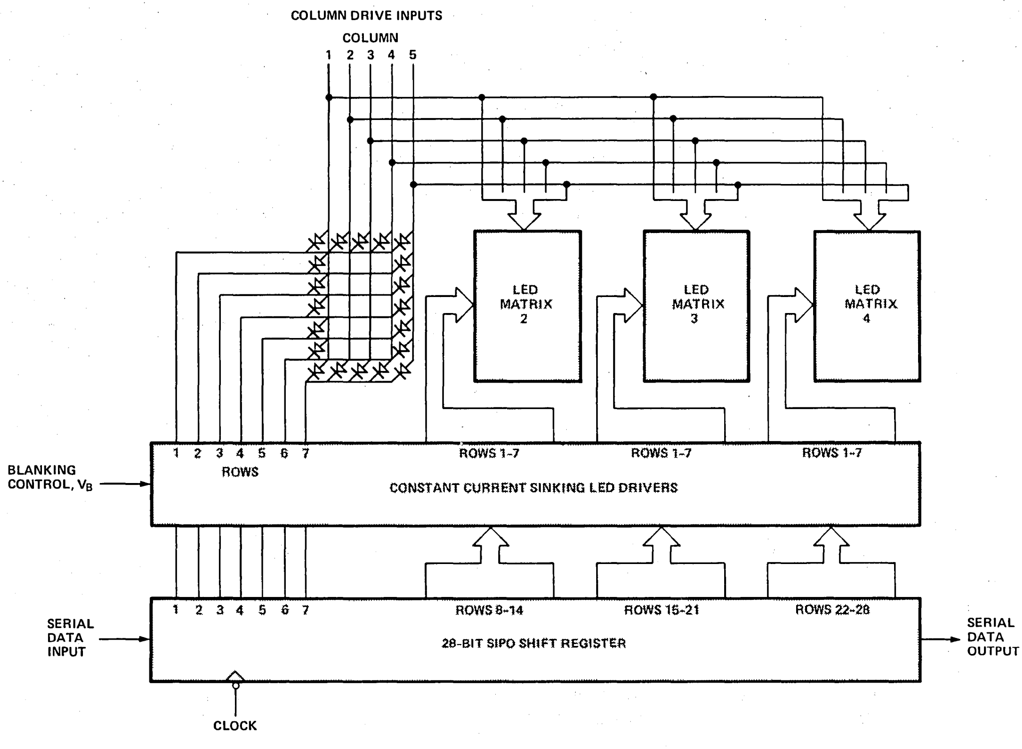


Figure 5. Block Diagram of an HDSP-238X Series LED Alphanumeric Display.

SOLID STATE DISPLAYS

Power Dissipation and Low Thermal Resistance Design Considerations

The light output of the HDSP-238X devices is a function of temperature, decreasing 1.5% for each 1° C increase in junction temperature. Therefore, it is desirable to maintain as low device junction temperature as possible to insure sufficient light output for sunlight readability. This is preferably achieved by designing for a low junction to ambient thermal resistance, or alternatively by controlling total display power dissipation by derating, see data sheet Figure 2.

Power Dissipation Calculation:

Power dissipation may be calculated using the equations of Figure 6a. For typical applications, the average pixel count per character is 15. The maximum power dissipation is calculated with a pixel count of 20 per character. As demonstrated in Figure 6c, the maximum power dissipation is 1.741 W with DF = 20%, V_{CC} = 5.25 V and V_{COL} = 3.5 V. The average power dissipation is 1.161 W per device with DF = 20%, V_{CC} = 5.0 V and V_{COL} = 3.5 V.

As shown in Figure 4 on the data sheet, the column current, I_{COL}, is constant when the column input voltage, V_{COL}, is at 2.75 V or greater. Setting V_{COL} substantially greater than 2.75 V does not increase light output, but does add to device total power dissipation. For optimum performance, it is recommended that V_{COL} be set between 2.75 V and 3.5 V.

Junction Temperature and Device Thermal Resistance:

It is necessary to control the IC junction temperature, T_J(IC), to insure proper operation of the display:

$$T_J(IC)MAX = 125° C$$

The equations to calculate T_J(IC) are given in Figure 6b. T_J(IC) will be higher than the device substrate temperature where as the individual LED pixel junction temperatures, T_J(LED), will be nearly the same as the substrate temperature. A sample calculation is presented in Figure 6c.

An easy design rule is to obtain a IC junction to ambient thermal resistance, $R_{\theta J-A}$, that establishes the device pin temperature less than 100° C. The value of $R_{\theta J-A}$ = 23° C/W will permit device operation in an ambient temperature of 85° C, without derating. Figure 7 gives the maximum values for $R\theta_{J-A}$ for reliable device operation in ambient temperatures from 25° C to 85° C.

To achieve a low value of $R_{\theta PIN-A}$, the following designs may be incorporated into the display system:

1. Mount the displays on a double sided maximum metalized PC board, as illustrated in Figure 8.

For single line display assemblies, a double sided maximum metalized PC board is a cost effective way to achieve a low thermal resistance to ambient. "Lands" are used instead of "traces" as the current carrying elements. Each "land" is made as wide as possible, consistent with circuit layout restrictions, to achieve metalized surface area to radiate thermal energy. Isolation strips, 0,64 mm (0.025 inch) wide, are etched from the board to electrically isolate the lands. PC board thermal resistance values in the range of 35° C/W per device are achievable for single line display assemblies. Air flow across the display PC board assembly dissipates the heat.

2. Install a metal plate, or bar, between the display packages and the PC board, with the bar mechanically fastened to the chassis, as illustrated in Figure 9a.

For multiple display lines, a metal plate may be placed between the display packages and the PC board to conduct the heat to the chassis housing assembly. The metal plate may be electrically insulated from the PC board by a thermally conductive insulator. Heat sink bars are formed in the metal plate by milling out lead clearance slots. The ceramic package of a display rests on one of the heat sink bars with the device leads passing through the slots to make electrical contact with the PC board. The heat is transferred from the display ceramic package into the metal plate. The chassis housing acts as the thermal radiator to dissipate the heat into the surrounding environment. The metal plate must be mechanically fastened to the housing assembly, otherwise it will act only as a thermal capacitor and will not dissipate the heat.

3. Install a heat pipe between the display packages and the PC board, with the heat pipe mechanically fastened to the chassis housing, as shown in Figure 9b.

The heat pipe is a low mass alternative to the metal plate described above. A heat pipe is a small tube, filled with a chemical, that transfers heat from the source to a heat sink with minimal thermal impedance. It is not a heat sink. The heat pipe transfers the heat directly from the display ceramic package to the chassis housing which dissipates the heat into the surrounding air.

4. Utilize a heat pipe to transfer the heat from a maximum metalized PC board to a finned heat sink mounted on the back of the assembly housing, as shown in Figure 10.

The heat pipe is placed against the back side of a maximum metalized PC board, electrically isolated by a thermally conductive insulator. When the heat pipe is connected to a finned heat sink on the back of the chassis housing, PC board to external ambient thermal resistance values in the range of 10 to 15° C/W per device can be achieved. The heat generated by the displays is directly dissipated into the external ambient surrounding the chassis housing by the finned heat sink.

Contact the following manufacturers for information on:

Heat Pipe Technology:

Noren Products
3545 Haven Avenue
Menlo Park, CA 94025
(415) 365-0632

Thermally Conductive Insulators; "Sil-Pad":

Bergquist Company
5300 Edina Indl Blvd.
Minneapolis, MN 55435
(612) 835-2322

$PD = P(I_{CC}) + P(I_{REF}) + P(I_{COL})$; Total power dissipation per device.

Where: $P(I_{CC}) = I_{CC}\ (V_B = 0.4\ V) \cdot V_{CC}$; Power dissipated by the two ICs when the display is blanked.

$P(I_{REF}) = 5 \cdot [I_{CC}\ (V_B = 2.4\ V) - I_{CC}\ (V_B = 0.4\ V)] \cdot V_{CC} \cdot (n/35) \cdot DF$; Additional power dissipated by the two ICs with characters illuminated.

$P(I_{COL}) = 5 \cdot I_{COL} \cdot V_{COL}(n/35) \cdot DF$; Power dissipated by the LED pixels when the characters are illuminated.

n = 15 pixels per character for average power.

n = 20 pixels per character for maximum power.

Figure 6a. Equations for Calculating Device Power Dissipation.

Delta T_J (IC) = $R\theta_{J\text{-}PIN} \cdot PD$; IC junction temperature rise above device pin temperature.

Where: $R\theta_{J\text{-}PIN}$ = 10° C/W; The thermal resistance IC junction to device pin 1.

Delta T_{PIN} = $R\theta_{PIN\text{-}A} \cdot PD$; Device pin temperature rise above the ambient temperature, T_A.

Where: $R\theta_{PIN\text{-}A}$ = The thermal resistance, device pin to ambient through the PC board, on a per device basis.

T_J (IC) = T_A + [Delta T_J (IC) + Delta T_{PIN}]; IC junction temperature, the sum of the ambient temperature and the temperature rise above ambient.

Figure 6b. Equations for Calculating IC Junction

Device Maximum Power Dissipation:

IC Maximum Power Dissipation:

$P(I_{CC}) = (0.060A)\ (5.25\ V) = 0.315\ W$

$P(I_{REF}) = 5(0.100A - 0.060A)\ (5.25\ V)\ (20/35)\ (1/5) = 0.120W$

I_{COL} Power Dissipation:

$P(I_{COL}) = 5(0.653A)\ (3.5\ V)\ (20/35)\ (1/5) = 1.306\ W$

Device Maximum Power Dissipation:

$PD(MAX) = 0.315\ W + 0.120\ W + 1.306\ W = 1.741\ W$

IC Junction Temperature, T_A = 85° C:

IC Junction Temperature Rise Above Substrate Pin:

Delta T_J(IC) = (10° C/W) (1.741 W) = 17.4° C Rise

Device Pin Temperature Rise Above Ambient:

Delta T(PIN) = (13° C/W) (1.741 W) = 22.6° C Rise

IC Junction Temperature:

T_J(IC) = 85° C + (17.4° C + 22.6° C) = 125.0° C

Note:
I_{CC} and I_{COL} values taken from the data sheet Electrical Characteristics. $R\theta_{J\text{-}PIN}$ = 10° C/W and $R\theta_{PIN\text{-}A}$ = 13° C/W.

Figure 6c. Sample Calculation of Device Maximum Power Dissipation and IC Junction Temperature for an HDSP-238X Series Device Operating in an Ambient of T_A = 85° C.

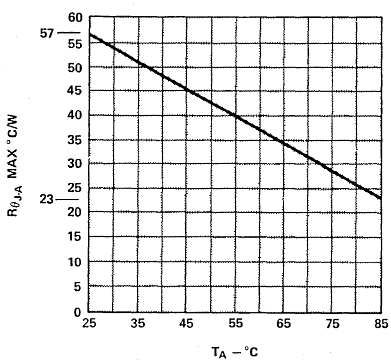


Figure 7. Maximum Thermal Resistance IC Junction to Ambient, $R\theta_{J\text{-}A}$, vs. Ambient Temperature. Based on: P_D MAX. = 1.741 W, T_J (IC) MAX. = 125° C.

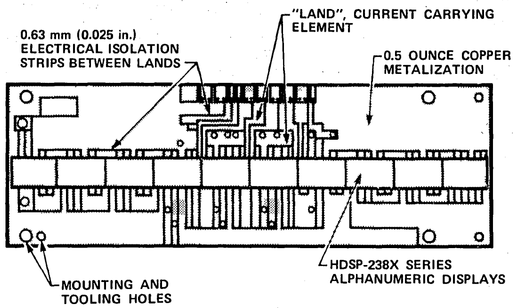


Figure 8. Maximum Metalized PC Board, Double Sided, for Mounting HDSP-238X Series Displays.

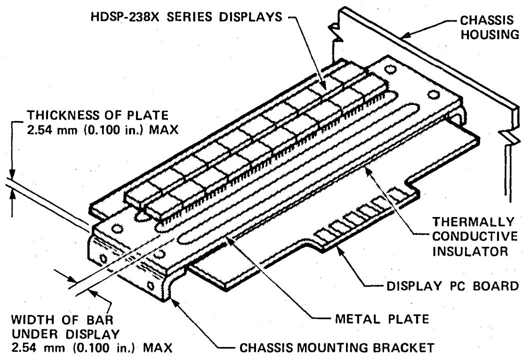


Figure 9a. Metal Plate Mounted Between Display Devices and PC Board, Mechanically Fastened to Chassis Housing.

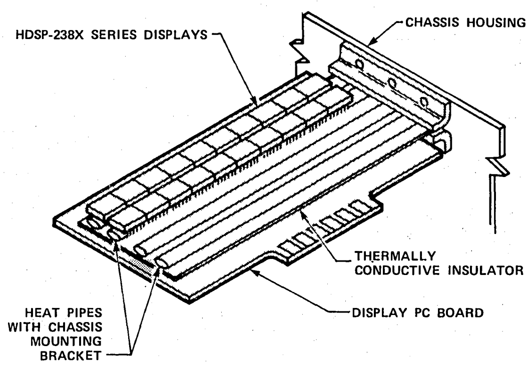


Figure 9b. Heat Pipes Mounted Between Display Devices and PC Board, Mechanically Fastened to Chassis Housing.

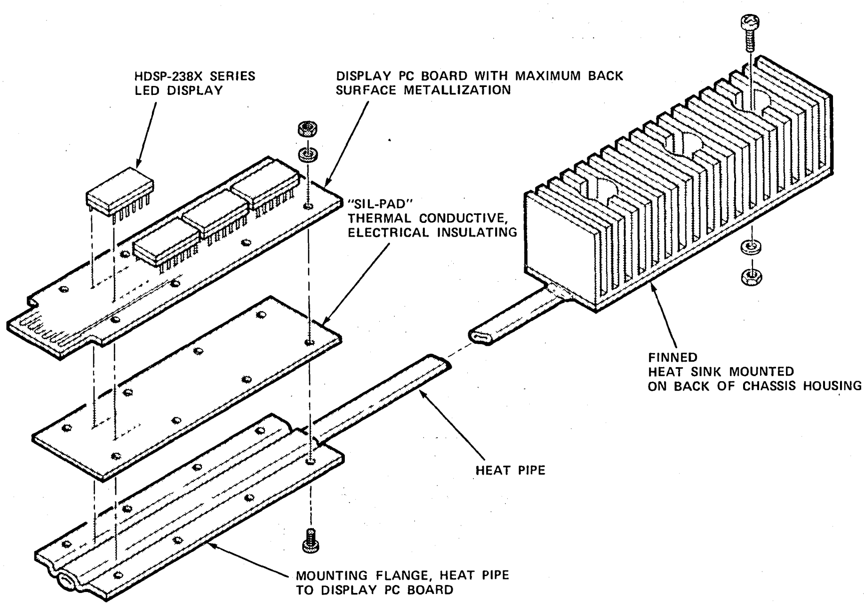


Figure 10. Using a Heat Pipe to Transfer Display Generated Heat to an Externally Mounted Finned Heat Sink.

Contrast Enhancement

The high light output of the HDSP-238X series displays in combination with improved contrast enhancement techniques, such as a new filter for the green HDSP-2383 display, make it possible to achieve readability in sunlight. Readability of the HDSP-238X series displays in sunlight is achieved by placing an antireflection coated, AR, circular polarized, CP, optically tinted glass filter in front of the display. The AR/CP optically tinted glass filter provides luminous contrast between the on-LED pixels and the display background, establishes a recognizable color difference between the on-LED pixels and the display background and reduces the level of ambient light reflected off the front surface of the filter. This technology and the concept of Discrimination Index, as a measure of readability, are discussed in Application Note 1015.

An AR/CP optically tinted glass filter should have a single pass relative transmission between 11% and 17% at the peak wavelength of the LED radiated spectrum, provided by the optical tinting. The double pass relative transmission should be less than 1%, provided by the circular polarizer. The filter can be either neutral density or bandpass, depending upon the properties of the optical tinting. The appropriate bandpass filter, with a peak relative transmission positioned at the peak wavelength of the LED radiated spectrum, will typically have a higher luminous contrast ratio than a neutral density filter, as it absorbs ambient light in the blue and blue-green regions. The AR coating reduces reflections off the front surface of the glass filter to a nominal 0.25%.

Luminous contrast values greater than 4.0 can be achieved in 107,000lm/m^2 (10,000fc) sunlight, excluding the condition of a reflected image of the sun off the front surface of the filter. The luminous contrast, which includes both diffuse and specular reflectance components off the front surface of the glass filter, is the predominant factor in the determination of the Discrimination Index. The luminous contrast combined with the color difference between illuminated LED pixels and the display background, as viewed through the AR/CP filter, produce Discrimination Index values in the neighborhood of 5.0. Values of Discrimination Index greater than 4.0 have been demonstrated to correlate with acceptable readability in sunlight.

A theoretical relative transmission characteristic for an optimal bandpass filter for the HDSP-2383 is presented in Figure 11. Diffuse and specular reflectance values are given in Figure 12. Two AR/CP glass filters that approach the theoretical characteristic are the 12% GREEN passband manufactured by Marks Polarized Corporation and the HOYA HLF-608-1G. Figures 13a, b and c present the Luminous Index, Chrominance Index and Discrimination Index calculations for the HDSP-2383/Marks 12% GREEN filter combination. The Luminous contrast ratio of 5.22 gives a Luminance Index of 4.79, combined with a Chrominance Index of 1.07 produces a Discrimination Index of 4.91.

The HDSP-2383 combined with a 14% neutral density AR/CP glass filter can achieve a luminous contrast of 4.66, providing a Discrimination Index of 4.60 which is an 16% improvement over the value of 3.97 calculated for the standard green HDSP-2303 display in Application Note 1015.

Table 1 lists calculated values for luminous contrast, Luminous Index, Chrominance Index and Discrimination Index for the three HDSP-238X series devices in combination with a 14% transmission neutral density AR/CP glass filter in sunlight.

At present, the following two filter manufacturers provide AR/CP optically tinted glass filters for use with the HDSP-238X series displays in sunlight:

Marks Polarized Corporation 25B Jefryn Blvd. West Deer Park, NY 11729 (516) 242-1300	Polaroid Corporation Polarizer Division 1 Upland Road Norwood, MA 02062 (617) 769-6800	Hoya Optics, Inc. 3400 Edison Way Fremont, CA 94538 (415) 490-1880
AR/CP Glass Filter: 12% Green Bandpass Display: HDSP-2383 10% Neutral Density Displays: HDSP-2381/ -2382	AR/CP Glass Filter: HNCP10 10% Neutral Density Displays: HDSP-2381/ -2382/-2383	AR/CP Glass Filter: HLF-608-1G Display:HDSP-2383 HLF-608-34 Display: HDSP-2381 HLF-608-5-12 Displays: HDSP-2382

Hewlett-Packard has contacted various filter manufacturers, requesting development of bandpass AR/CP glass filters for all three HDSP-238X series displays. As these filters become available, Hewlett-Packard will publish application information on their luminous/color contrasts and Discrimination Index performances.

SOLID STATE DISPLAYS

Table 1. Discrimination Index Values for the HDSP-238X Series Displays

Display Device	Time Average Luminous Intensity	Luminous Contrast	Luminance Index	Chrominance Index	Discrimination Index
HDSP-2381	680 μcd	4.66	4.46	1.94	4.86
HDSP-2382	570 μcd	4.09	4.08	6.86	7.98
HDSP-2383	680 μcd	4.66	4.46	1.14	4.60

Ambient: 107,000 lm/m^2 (10,000 fc) Sunlight
Filter Type: 14% Transmission, AR/CP, Neutral Density

Filter Surface Reflectance: 0.25% Specular and 0.02% Diffuse
Luminous Intensity: Data Sheet Typical × 20% Duty Factor

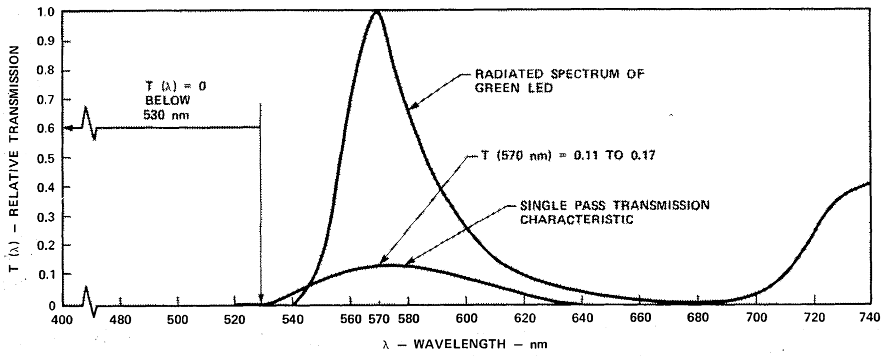


Figure 11. Relative Transmission Characteristics for a Yellow-Green Bandpass Antireflection Coated, Circular Polarized Glass Filter for use with the HDSP-2383 Green LED Alphanumeric Display.

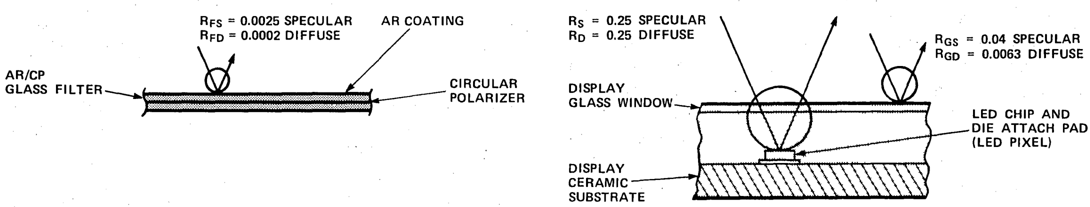
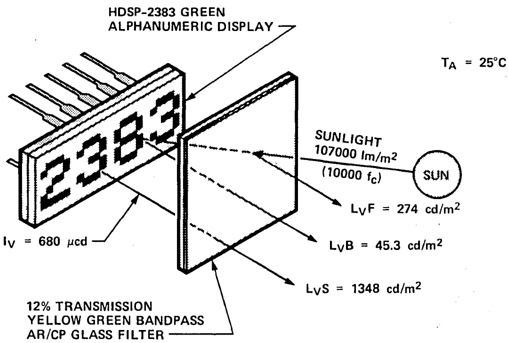


Figure 12. Reflectances off Surfaces of an HDSP-238X Series Display and an AR/CP Glass Filter.

$$ID = \sqrt{IDL^2 + IDC^2}$$
$$ID = \sqrt{(4.79)^2 + (1.07)^2}$$
$$ID = 4.91$$

$$IDL = 4.79$$
$$IDC = 1.07$$

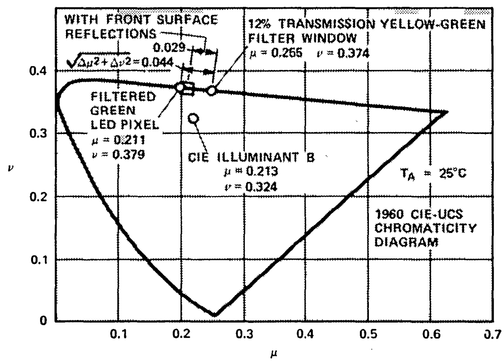
Figure 13a. Discrimination Index for the HDSP-2383 Green LED Alphanumeric Display Combined with a 12% Transmission Yellow-Green Bandpass AR/CP Glass Filter in Indirect 107000 lm/m² (10,000 fc) sunlight.



$$CR = \frac{L_VS + L_VB + L_VF}{L_VB + L_VF}$$
$$CR = \frac{1348 + 45.3 + 274}{45.3 + 274}$$
$$CR = 5.22$$

$$IDL = \frac{LOG_{10}\ CR}{0.15}$$
$$IDL = \frac{LOG_{10}\ (5.22)}{0.15}$$
$$IDL = 4.79$$

Figure 13b. Contrast Ratio and Luminance Index.



$$IDC = \frac{\sqrt{\Delta\mu^2 + \Delta\mu^2}}{0.027} = \frac{0.029}{0.027} = 1.07$$

Figure 13c. Color Difference and Chrominance Index

SOLID STATE DISPLAYS

HEWLETT PACKARD

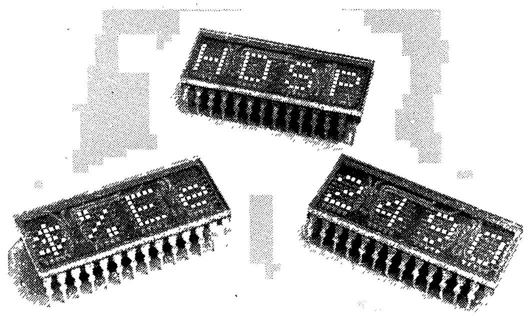
FOUR CHARACTER 6.9 mm (0.27 INCH) 5X7 ALPHANUMERIC DISPLAYS

STANDARD RED HDSP-2490
YELLOW HDSP-2491
HIGH EFFICIENCY RED HDSP-2492
HIGH PERFORMANCE GREEN HDSP-2493

TECHNICAL DATA JANUARY 1986

Features

- **FOUR COLORS**
  Standard Red
  Yellow
  High Efficiency Red
  High Performance Green
- **INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS**
- **COMPACT CERAMIC PACKAGE**
- **WIDE VIEWING ANGLE**
- **END STACKABLE FOUR CHARACTER PACKAGE**
- **TTL COMPATIBLE**
- **5 x 7 LED MATRIX DISPLAYS FULL ASCII SET**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
- **HDSP-2491/2493 ALSO CATEGORIZED FOR COLOR**



Typical Applications

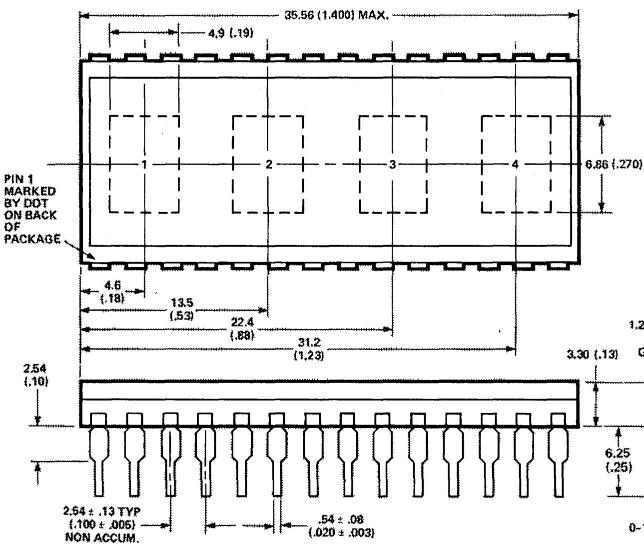
- **INSTRUMENTS**
- **BUSINESS MACHINES**
- **INDUSTRIAL PROCESS CONTROL EQUIPMENT**
- **MEDICAL INSTRUMENTS**
- **COMPUTER PERIPHERALS**
- **MILITARY GROUND SUPPORT EQUIPMENT**

Description

The HDSP-2490/-2491/-2492/-2493 series of displays are 6.9 mm (0.27 inch) 5 x 7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow, high efficiency red, and high performance green.

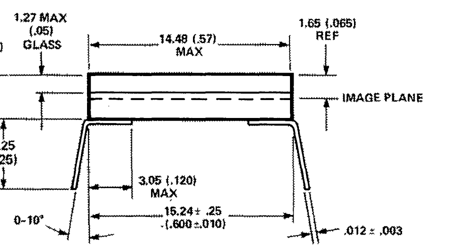
Each four character cluster is contained in a 28 pin dual-in-line package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions



PIN	FUNCTION[1]	PIN	FUNCTION
1	NO CONNECT	15	NO CONNECT
2	COLUMN 1	16	DATA OUT
3	COLUMN 1	17	DATA OUT
4	COLUMN 2	18	V_B
5	COLUMN 2	19	V_B
6	COLUMN 3	20	V_{CC}
7	COLUMN 3	21	V_{CC}
8	COLUMN 4	22	CLOCK
9	COLUMN 4	23	CLOCK
10	COLUMN 5	24	GROUND
11	COLUMN 5	25	GROUND
12	INT. CONNECT[2]	26	DATA IN
13	INT. CONNECT[2]	27	DATA IN
14	NO CONNECT	28	NO CONNECT

NOTES:
1. ALL USEABLE FUNCTION PINS ARE REDUNDANT. ELECTRICAL CONNECTION CAN BE MADE TO EITHER PIN OR BOTH.
2. DO NOT CONNECT OR USE.
3. DIMENSIONS IN mm (INCHES).
4. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ± .38 mm (±.015 INCHES).



Absolute Maximum Ratings (HDSP-2490/-2491/-2492/-2493)

Supply Voltage V_{CC} to Ground .... —0.5V to 6.0V
Inputs, Data Out and V_B .... —0.5V to V_{CC}
Column Input Voltage, V_{COL} .... —0.5V to +6.0V
Free Air Operating
Temperature Range, T_A [1,2] .... —20° C to +85° C
Storage Temperature Range, T_S ..... —55° C to +100° C
Maximum Allowable Power Dissipation
at T_A = 25° C [1,2,3] .... 1.46 Watts
Maximum Solder Temperature 1.59 mm (0.063 in.)
Below Seating Plane t < 5 sec .... 260° C

Recommended Operating Conditions (HDSP-2490/-2491/-2492/-2493)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2490	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On HDSP-2491/-2492/-2493	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range [1,2]	T_A	-20		85	°C	2

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V, V_{COL} = 3.5V	V_B = 0.4V			500	μA	4
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		380	520	mA	4
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V	
V_B, Clock or Data Input Threshold Low		V_{IL}	V_{CC} = V_{COL} = 4.75V				0.8	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	μA	
	Data In	I_{IH}				10	40	μA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	μA	
	Data In	I_{IL}				-250	-400	μA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF 15 LEDs on per character, V_B = 2.4V			0.78		W	2
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				20		°C/W/ Device	2

*All typical values specified at V_{CC} = 5.0V and T_A = 25° C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85° C ambient is possible provided the following conditions are met. The junction should not exceed 125° C T_J and the case temperature (as measured at pin 1 or the back of the display) should not exceed 100° C T_C.
2. The device should be derated linearly above 60° C at 22.2 mW/° C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 25° C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

Optical Characteristics

STANDARD RED HDSP-2490

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	220	370		μcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2491

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	850	1400		μcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2492

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	850	1530		μcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

HIGH PERFORMANCE GREEN HDSP-2493

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_i = 25°C$[6], $V_B = 2.4V$	1280	2410		μcd	3
Peak Wavelength	λ_{PEAK}			568		nm	
Dominant Wavelength[5,7]	λ_d			574		nm	

*All typical values specified at $V_{CC} = 5.0V$ and $T_A = 25°C$ unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2491/-2493 are categorized for color with the color category designated by a number code on the bottom of the package.
6. T_i refers to the initial case temperature of the device immediately prior to the light measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:
   L_v (cd/m^2) = I_v (Candela)/A (Metre)^2
   L_v (Footlamberts) = πI_v (Candela)/A (Foot)^2
   $A = 5.3 \times 10^{-8}$ M^2 = 5.8×10^{-7} (Foot)^2

Electrical Description

The HDSP-249X series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features DATA IN and DATA OUT terminals arrayed for easy PC board interconnection. DATA OUT represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5 x 7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

In the normal mode of operation, input data for digit 4 column 1 is loaded into the 7 on-board shift register locations 1 through 7. Column 1 data for digits 3, 2 and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5\,(t + T)}$$

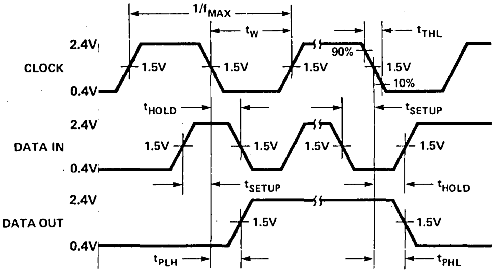
The time frame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time t + T of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain t << T. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics HDSP-2490/-2491/-2492/-2493 (T_A = -20° C to +85° C)

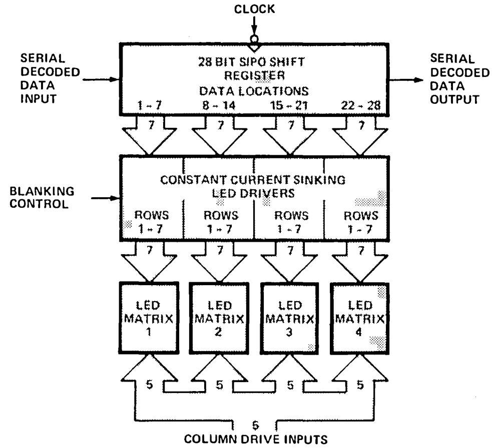


Figure 5. Block Diagram of HDSP-2490/-2491/-2492/-2493

Mechanical and Thermal Considerations

The HDSP-2490/-2491/-2492/-2493 are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. The HDSP-2490/-2491/-2492/-2493 utilize a high output current IC to provide excellent readability in bright ambient lighting. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 45° C/watt/device is possible up to ambient temperature of 60° C. For operation above 60° C, the maximum device dissipation should be derated linearly at 22.2 mW/°C (see Figure 2). With an improved thermal design, operation at higher ambient temperatures without derating is possible. Please refer to Application Note 1016 for further information.

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.4V for the HDSP-2490 and 2.75V for the HDSP-2491/-2492/-2493. Also, the average drive current can be decreased through pulse width modulation of V_B.

The HDSP-2490/-2491/-2492/-2493 displays have glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 6. Additional information on filtering and contrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2000 Std. Red	Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Plexiglass 2423		
HDSP-2001 (Yellow)	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10 Chequers Grey 105	Polaroid HNCP10-Glass Marks Polarized MPC-0301-8-10 Note 1
HDSP-2002 (HER)	Panelgraphic Ruby Red 60 Chequers Red 112		Polaroid HNCP10-Glass Marks Polarized MPC-0201-2-22
HDSP-2003 (HP Green)	Panelgraphic Green 48 Chequers Green 107		Polaroid HNCP10-Glass Marks Polarized MPC-0101-5-12

Note: 1. Optically coated circular polarized filters, such as Polaroid HNCP10.

Figure 6. Contrast Enhancement Filters

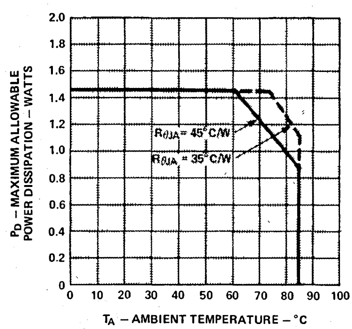


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

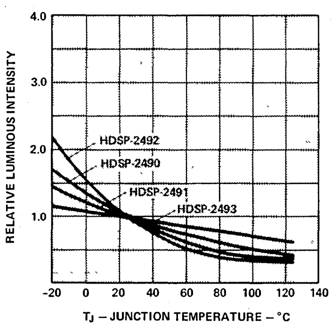


Figure 3. Relative Luminous Intensity vs. Temperature

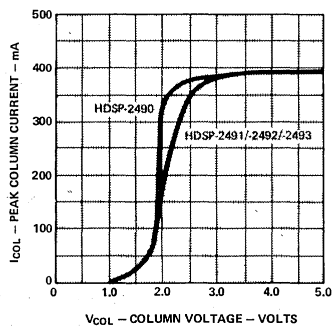


Figure 4. Peak Column Current vs. Column Voltage

HEWLETT PACKARD

5 x 7 DOT MATRIX ALPHANUMERIC DISPLAY SYSTEM

HDSP-2416
HDSP-2424
HDSP-2432
HDSP-2440
HDSP-2470
HDSP-2471
HDSP-2472

TECHNICAL DATA JANUARY 1986

Features

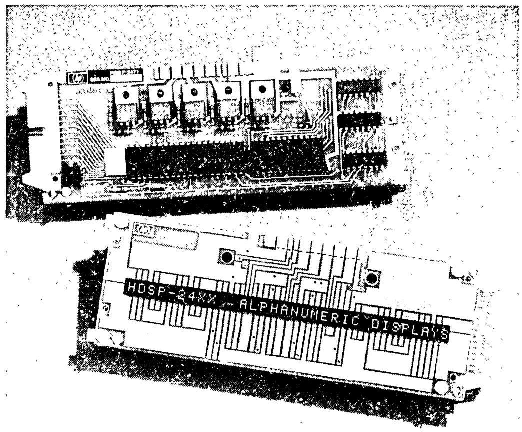
- COMPLETE ALPHANUMERIC DISPLAY SYSTEM UTILIZING THE HDSP-2000 DISPLAY
- CHOICE OF 64, 128, OR USER DEFINED ASCII CHARACTER SET
- CHOICE OF 16, 24, 32, or 40 ELEMENT DISPLAY PANEL
- MULTIPLE DATA ENTRY FORMATS — Left, Right, RAM, or Block Entry
- EDITING FEATURES THAT INCLUDE CURSOR, BACKSPACE, FORWARDSPACE, INSERT, DELETE, AND CLEAR
- DATA OUTPUT CAPABILITY
- SINGLE 5.0 VOLT POWER SUPPLY
- TTL COMPATIBLE
- EASILY INTERFACED TO A KEYBOARD OR A MICROPROCESSOR

Description

The HDSP-24XX series of alphanumeric display systems provides the user with a completely supported 5 x 7 dot matrix display panel. These products free the user's system from display maintenance and minimize the interaction normally required for alphanumeric displays. Each alphanumeric display system is composed of two component parts:

1. An alphanumeric display controller which consists of a preprogrammed microprocessor plus associated logic, which provides decode, memory, and drive signals necessary to properly interface a user's system to an HDSP-2000 display. In addition to these basic display support operations, the controller accepts data in any of four data entry formats and incorporates several powerful editing routines.
2. A display panel which consists of HDSP-2000 displays matched for luminous intensity and mounted on a P.C. board designed to have low thermal resistance.

These alphanumeric display systems are also available in high efficiency red, yellow, and green. In addition, they are available using the HDSP-2300 or HDSP-2490 series displays to form display systems with larger characters (5.0 mm and 6.9 mm, respectively). Contact your local HP sales office for more information.



Typical Applications

- DATA ENTRY TERMINALS
- INSTRUMENTATION
- BUSINESS EQUIPMENT
- COMPUTER PERIPHERALS

PART NUMBER	DESCRIPTION
Display Boards	
HDSP-2416	Single-line 16 character display panel utilizing the HDSP-2000 display
HDSP-2424	Single-line 24 character display panel utilizing the HDSP-2000 display
HDSP-2432	Single-line 32 character display panel utilizing the HDSP-2000 display
HDSP-2440	Single-line 40 character display panel utilizing the HDSP-2000 display
Controller Boards	
HDSP-2470	HDSP-2000 display interface incorporating a 64 character ASCII decoder
HDSP-2471	HDSP-2000 display interface incorporating a 128 character ASCII decoder
HDSP-2472	HDSP-2000 display interface without ASCII decoder. Instead, a 24 pin socket is provided to accept a custom 128 character set from a user programmed 1K x 8 PROM.

When ordering, specify one each of the Controller Board and the Display Board for each complete system.

HDSP-2470/-2471/-2472

Absolute Maximum Ratings

V_{CC} .... -0.5V to 6.0V
Operating Temperature Range,
Ambient (T_A) .... 0°C to 70°C
Storage Temperature Range (T_S) .... -55°C to 100°C
Voltage Applied to any Input or Output ..-0.5V to 6.0V
I_{SOURCE} Continuous for any Column
Driver .... 5.0 Amps (60 sec. max. duration)

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units
Supply Voltage		V_{CC}	4.75	5.25	V
Data Out		I_{OL}		0.4	mA
		I_{OH}		-20	μA
Ready, Data Valid, Column On, Display Data		I_{OL}		1.6	mA
		I_{OH}		-40	μA
Clock		I_{OL}		10.0	mA
		I_{OH}		-1.0	mA
$Column_{1-5}$		I_{SOURCE}		-5.0	A

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	
Supply Current[1]	I_{CC}			400	mA	V_{CC} = 5.25V Column On and All Outputs Open	
Input Threshold High (except Reset)	V_{IH}	2.0			V	V_{CC} = 5.0V ± .25V	
Input Threshold High — Reset[2]	V_{IH}	3.0			V	V_{CC} = 5.0V ± .25V	
Input Threshold Low — All Inputs	V_{IL}			0.8	V	V_{CC} = 5.0V ± .25V	
Data Out Voltage	V_{OH}Data	2.4			V	I_{OH} = -20μA	V_{CC} = 4.75V
	V_{OL}Data			0.5	V	I_{OL} = 0.4mA	V_{CC} = 4.75V
Clock Output Voltage	V_{OH}Clk	2.4			V	I_{OH} = -1000μA	V_{CC} = 4.75V
	V_{OL}Clk			0.5	V	I_{OL} = 10.0mA	V_{CC} = 4.75V
Ready, Display Data, Data Valid, Column on Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA	V_{CC} = 4.75V
	V_{OL}			0.5	V	I_{OL} = 1.6mA	V_{CC} = 4.75V
Input Current,[3] All Inputs Except Reset, Chip Select, D_7	I_{IH}			-0.3	mA	V_{IH} = 2.4V	V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V	V_{CC} = 5.25V
$\overline{\text{Reset}}$ Input Current	I_{IH}			-0.3	mA	V_{IH} = 3.0V	V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V	V_{CC} = 5.25V
Chip Select, D_7 Input Current	I_I	-10		+10	μA	$0 < V_I < V_{CC}$	
Column Output Voltage	V_{OL}COL	2.6	3.2		V	I_{OUT} = -5.0A	V_{CC} = 5.00V

NOTES:
1. See Figure 11 for total system supply current.
2. External reset may be initiated by grounding Reset with either a switch or open collector TTL gate for a minimum time of 50ms. For Power On Reset to function properly, V_{CC} power supply should turn on at a rate > 100V/s.
3. Momentary peak surge currents may exist on these lines. However, these momentary currents will not interfere with proper operation of the HDSP-2470/1/2.

SOLID STATE DISPLAYS

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground .... -0.5V to 6.0V

Inputs, Data Out and V_B .... -0.5V to V_{CC}

Column Input Voltage, V_{COL} .... -0.5V to +6.0V

Free Air Operating Temperature
Range, T_A[1] .... 0°C to +55°C

Storage Temperature Range, T_S .... -55°C to +100°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Norm.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Column Input Voltage, Column On	V_{COL}	2.6			V
Setup Time	t_{SETUP}	70	45		ns
Hold Time	t_{HOLD}	30	0		ns
Width of Clock	$t_{W(CLOCK)}$	75			ns
Clock Frequency	f_{CLOCK}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating[1] Temperature Range	T_A	0		55	°C

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter		Symbol	Min.	Typ.*	Max.	Units	Conditions	
Supply Current		I_{CC}		45n	60n[2]	mA	V_{CC} = 5.25V V_{CLOCK}=V_{DATA}=2.4V All SR Stages = Logical 1	V_B = 0.4V
				73n	95n	mA		V_B = 2.4V
Column Current at any Column Input		I_{COL}			1.5n	mA	V_{CC} = V_{COL} = 5.25V All SR Stages = Logical 1	V_B = 0.4V
		I_{COL}		335n	410n	mA		V_B = 2.4V
Peak Luminous Intensity per LED (Character Average)		$I_{V\ PEAK}$	105	200		μcd	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25°C[3], V_B = 2.4V	
V_B, Clock or Data Input Threshold High		V_{IH}	2.0			V	V_{CC} = V_{COL} = 4.75V	
V_B, Clock or Data Input Threshold Low		V_{IL}			0.8	V		
Input Current Logical 1	V_B, Clock	I_{IH}			80	μA	V_{CC} = 5.25V, V_{IH} = 2.4V	
	Data In	I_{IH}			40	μA		
Input Current Logical 0	V_B, Clock	I_{IL}		-500	-800	μA	V_{CC} = 5.25V, V_{IL} = 0.4V	
	Data In	I_{IL}		-250	-400	μA		
Power Dissipation Per Board[4]		P_D		0.66n		W	V_{CC} = 5.0V, V_{COL} = 2.6V 15 LED's on per Character, V_B = 2.4V	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

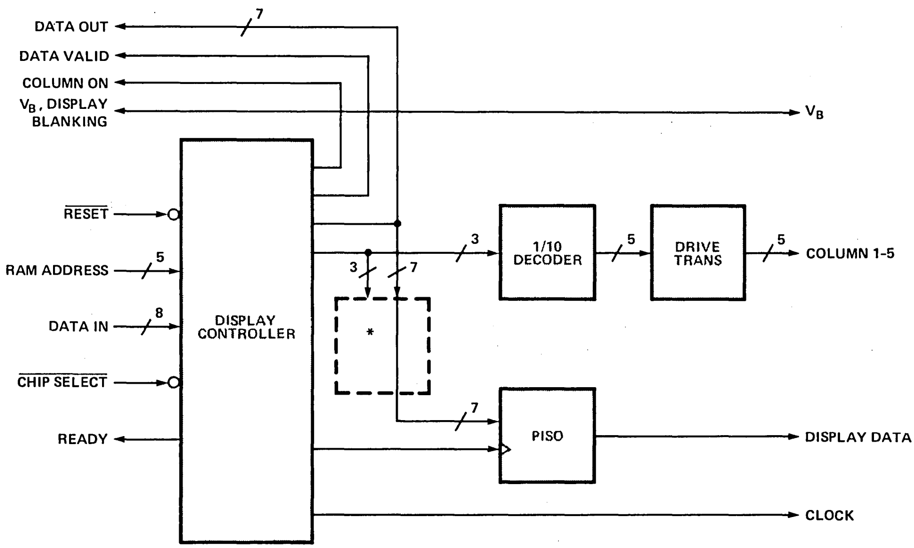
NOTES:

1. Operation above 55° C (70° C MAX) may be achieved by the use of forced air (150 fpm normal to component side of HDSP-247X controller board at sea level). Operation down to -20° C is possible in applications that do not require the use of HDSP-2470/-2471/-2472 controller boards.
2. n = number of HDSP-2000 packages
   HDSP-2416 n = 4
   HDSP-2424 n = 6
   HDSP-2432 n = 8
   HDSP-2440 n = 10
3. Tj refers to initial case temperature immediately prior to the light measurement.
4. Power dissipation with all characters illuminated.

System Overview

The HDSP-2470/-2471/-2472 Alphanumeric Display Controllers provide the interface between any ASCII based Alphanumeric System and the HDSP-2000 Alphanumeric Display. ASCII data is loaded into the system by means of any one of four data entry modes — Left, Right, RAM or Block Entry. This ASCII data is stored in the internal RAM memory of the system. The system refreshes HDSP-2000 displays from 4 to 48 characters with the decoded data.

The user interfaces to any of the systems through eight DATA IN inputs, five ADDRESS inputs (RAM mode), a CHIP SELECT input, RESET input, seven DATA OUT outputs, a READY output, DATA VALID output, and a COLUMN ON output. A low level on the RESET input clears the display and initializes the system. A low level on the CHIP SELECT input causes the system to load data from the DATA IN and ADDRESS inputs into the system. The controller outputs a status word, cursor address and 32 ASCII data characters through the DATA OUT outputs and DATA VALID output during the time the system is waiting to refresh the next column of the display. The COLUMN ON output can be used to synchronize the DATA OUT function. A block diagram for the HDSP-2470/-2471/-2472 systems is shown in Figure 1.



* CHARACTER GENERATOR FOR HDSP-2471, SOCKET FOR 1K X 8 PROM FOR HDSP-2472.

Figure 1. Block Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

The system interfaces to the HDSP-2000 display through five COLUMN outputs, a CLOCK output, DISPLAY DATA output, and the COLUMN ON output. The user should connect DISPLAY DATA to DATA IN of the leftmost HDSP-2000 cluster and cascade DATA OUT to DATA IN of all HDSP-2000 clusters. COLUMN outputs from the system are connected to the COLUMN inputs of all HDSP-2000 clusters. The HDSP-24XX Series display boards are designed to interconnect directly with the HDSP-247X Series display controllers. The COLUMN outputs can source enough current to drive up to 48 characters of the HDSP-2000 display. Pulse width modulation of display luminous intensity can be provided by connecting COLUMN ON to the input of a monostable multivibrator and the output of the monostable multivibrator to the V_B inputs of the HDSP-2000 displays. The system is designed to refresh the display at a fixed refresh rate of 100 Hz. COLUMN ON time is optimized for each display length in order to maximize light output as shown in Figure 2.

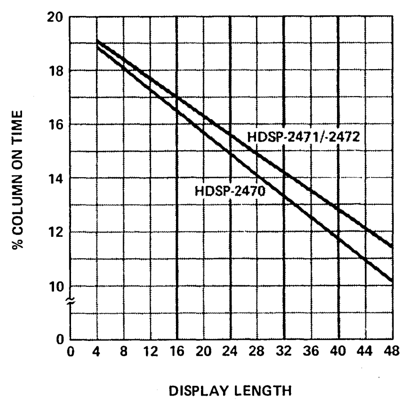


Figure 2. Column on Time vs. Display Length for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

SOLID STATE DISPLAYS

Control Mode/Data Entry

User interface to the HDSP-247X Series controller is via an 8 bit word which provides to the controller either a control word or standard ASCII data input. In addition to this user provided 8 bit word, two additional control lines, CHIP SELECT and READY, allow easily generated "handshake" signals for interface purposes.

A logic low applied to the CHIP SELECT input (minimum six microseconds) causes the controller to read the 8 DATA IN lines and determine whether a control word or ASCII data word is present, as determined by the logic state of the most significant bit (D_7). If the controller detects a logic high at D_7, the state of D_6-D_0 will define the data entry mode and the number of alphanumeric characters to be displayed.

The 8 bit control data word format is outlined in Figure 3. For the control word (D_7 high), bits D_6 and D_5 define the selected data entry mode (Left entry, Right entry, etc.) and bits D_3 to D_0 define display length. Bit D_4 is ignored.

Control word inputs are first checked to verify that the control word is valid. The system ignores display lengths greater than 1011 for left block or right, or 0111 for RAM. If the word is valid, the present state—next state table shown in Figure 4 is utilized to determine whether or not to clear the display. For display lengths of up to 32 characters, RAM entry can be used as a powerful editing tool, or can be used to preload the cursor. With other transitions, the internal data memory is cleared.

CONTROL
WORD: $D_7D_6D_5D_4D_3D_2D_1D_0$

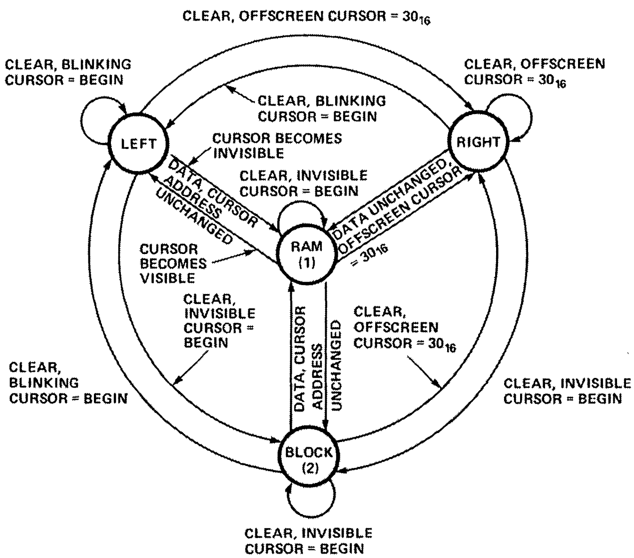
1	X	X	–	Y	Y	Y	Y

Y Y Y Y	DISPLAY LENGTH:
0 0 0 0	4 DIGITS
0 0 0 1	8 "
0 0 1 0	12 "
0 0 1 1	16 "
0 1 0 0	20 "
0 1 0 1	24 "
0 1 1 0	28 "
0 1 1 1	32* "
1 0 0 0	36 "
1 0 0 1	40 "
1 0 1 0	44 "
1 0 1 1	48 "

*maximum for RAM data entry mode

X X	DATA ENTRY MODES
0 0	RAM DATA ENTRY
0 1	LEFT DATA ENTRY
1 0	RIGHT DATA ENTRY
1 1	BLOCK DATA ENTRY

Figure 3. Control Word Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.



(1) RAM ENTRY MODE IS VALID FOR DISPLAYS OF 32 CHARACTERS OR LESS IN LENGTH.
(2) FOLLOWING A TRANSITION FROM RAM TO BLOCK, WHEN THE CURSOR ADDRESS IS 48 (30_{16}) DURING THE TRANSITION, THE FIRST VALID ASCII CHARACTER WILL BE IGNORED AND THE SECOND VALID ASCII CHARACTER WILL BE LOADED IN THE LEFT-MOST DISPLAY LOCATION.

WHERE BEGIN IS DEFINED AS FOLLOWS:

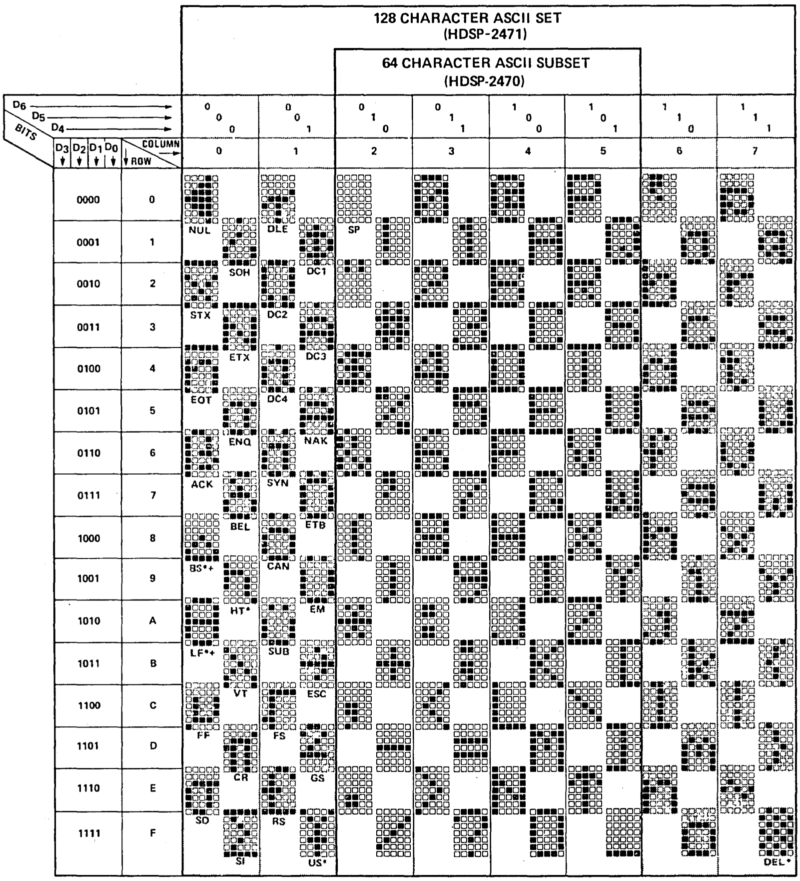
DISPLAY LENGTH	CURSOR ADDRESS OF BEGIN
4	$2C_{16}$, 44_{10}
8	28_{16}, 40_{10}
12	24_{16}, 36_{10}
16	20_{16}, 32_{10}
20	$1C_{16}$, 28_{10}
24	18_{16}, 24_{10}
28	14_{16}, 20_{10}
32	10_{16}, 16_{10}
36	$0C_{16}$, 12_{10}
40	08_{16}, 8_{10}
44	04_{16}, 4_{10}
48	00_{16}

Figure 4. Present State-Next State Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

If D_7 is a logic low when the DATA IN lines are read, the controller will interpret D_6-D_0 as standard ASCII data to be stored, decoded and displayed. The system accepts seven bit ASCII for all three versions. However, the HDSP-2470 system displays only the 64 character subset [20_{16} (space) to $5F_{16}$ (_)] and ignores all ASCII characters outside this subset with the exception of those characters defined as display commands. These display commands are shown in Figure 5. Displayed character sets for the HDSP-2470/-2471 systems are shown in Figure 6.

DATA WORD:	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
ASCII ASSIGNMENT	0	A	A	A	A	A	A	A	DISPLAY COMMAND	
LF		0	0	0	1	0	1	0	CLEAR	Valid in Right Entry Mode; Valid in Left Entry Mode
BS		0	0	0	1	0	0	0	BACKSPACE CURSOR	Valid in Right Entry Mode; Valid in Left Entry Mode
HT		0	0	0	1	0	0	1	FORWARDSPACE CURSOR	Valid in Left Entry Mode
US		0	0	1	1	1	1	1	INSERT CHARACTER	Valid in Left Entry Mode
DEL		1	1	1	1	1	1	1	DELETE CHARACTER	Valid in Left Entry Mode

Figure 5. Display Commands for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

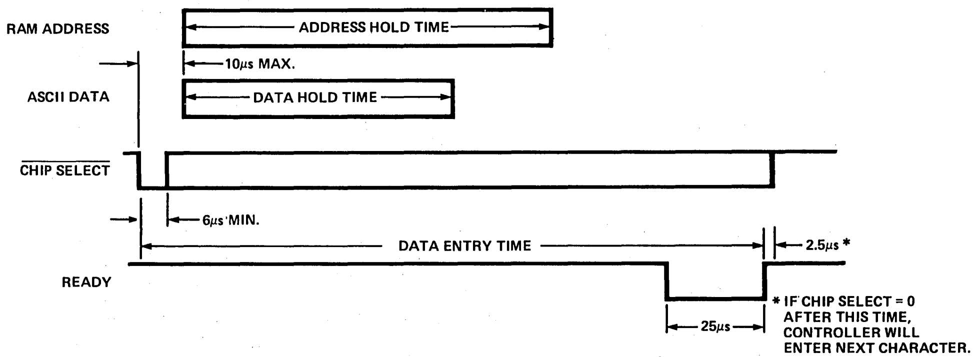


*DISPLAY COMMANDS WHEN USED IN LEFT ENTRY
+DISPLAY COMMANDS WHEN USED IN RIGHT ENTRY

Figure 6. Display Font for the HDSP-2470 (64 Character ASCII Subset), and HDSP-2471 (128 Character ASCII Set) Alphanumeric Display Controller.

Regardless of whether a control word or ASCII data word is presented by the user, a READY signal is generated by the controller after the input word is processed. This READY signal goes low for 25µs and upon a positive transition, a new CHIP SELECT may be accepted by the controller. Data Entry Timing is shown in Figure 7.

DATA ENTRY TIMING



MAXIMUM DATA ENTRY TIMES OVER OPERATING TEMPERATURE RANGE

DATA ENTRY MODE			FUNCTION					
HDSP-	DATA HOLD TIME*		DATA ENTRY	BACK SPACE	CLEAR	FORWARD SPACE	DELETE	INSERT
LEFT (2471/2)	135µs		235µs	195µs	505µs	205µs	725µs	725µs
LEFT (2470)	150µs		245µs	215µs	530µs	225µs	745µs	735µs
RIGHT (2471/2)	85µs		480µs	470µs	465µs			
RIGHT (2470)	105µs		490µs	490µs	485µs			
RAM (2471/2)	55µs	120µs**	190µs					
RAM (2470)	55µs	130µs**	200µs					
BLOCK (2471/2)	55µs		120µs	(155µs FOR RIGHTMOST CHARACTER)				
BLOCK (2470)	55µs		130µs	(165µs FOR RIGHTMOST CHARACTER)				
LOAD CONTROL (2471/2)	50µs		505µs					
LOAD CONTROL (2470)	50µs		505µs					

*Minimum time that data inputs must remain valid after Chip Select goes low.
**Minimum time that RAM address inputs must remain valid after Chip Select goes low.

Figure 7. Data Entry Timing and Data Entry Times for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Left Entry Mode

With Left entry, characters are entered in typewriter fashion, i.e., to the right of all previous characters. Left entry uses a blinking cursor to indicate the location where the next character is to be entered. CLEAR loads the display with spaces and resets the cursor to the leftmost display location. BACKSPACE and FORWARDSPACE move the cursor without changing the character string. Thus, the user can backspace to the character to be edited, enter a character and then forward space the cursor. The DELETE function deletes the displayed character at the cursor location and then shifts the character string following the cursor one location to the left to fill the void of the deleted character. The INSERT CHARACTER sets a flag inside the system that causes subsequent ASCII characters to be inserted to the left of the character at the cursor location. As new characters are entered, the cursor, the character at the cursor, and all characters to the right of the cursor are shifted one location to the right. The INSERT function is terminated by a second INSERT CHARACTER, or by BACKSPACE, FORWARDSPACE, CLEAR or DELETE. In Left entry mode, after the display is filled, the system ignores all characters except BACKSPACE and CLEAR. The system allows the cursor to be positioned only in the region between the leftmost display character and immediately to the right (offscreen) of the rightmost display character.

Right Entry Mode

In Right entry mode, characters are entered at the right hand side of the display and shifted to the left as new characters are entered. In this mode, the system stores 48 ASCII characters, although only the last characters entered are displayed. CLEAR loads the display with spaces. BACKSPACE shifts the display one location to the right, deleting the last character entered and displaying the next character in the 48 character buffer. Right entry mode is a simple means to implement the walking or "Times-Square" display. FORWARDSPACE, INSERT, and DELETE have character assignments in this mode since they are not treated as editing characters. In this mode, the cursor is located immediately to the right (offscreen) of the rightmost displayed character.

Block Entry Mode

Block entry allows the fastest data entry rate of all four modes. In this mode, characters are loaded from left to right as with Left entry. However, with Block entry, after the display is completely loaded, the next ASCII character is loaded in the leftmost display location, replacing the previous displayed character. While Block entry has a nonvisible cursor, the cursor is always loaded with the address of the next character to be entered. In this entry mode, the system can display the complete 128 character ASCII set. The display can be cleared and the cursor reset to the leftmost display location by loading in a new BLOCK control word.

RAM Entry Mode

In RAM entry, ASCII characters are loaded at the address specified by the five bit RAM address. Due to the limitation of only five address lines, RAM data entry is allowed only for displays less than or equal to 32 characters. Regardless of display length, address 00 is the leftmost display character. Out of range RAM addresses are ignored. While RAM entry has a non-visible cursor, the cursor is always preloaded with the address to the right of the last character entered. This allows the cursor to be preloaded with an address prior to going into any other entry mode. In RAM entry, the system can display the complete 128 character ASCII set because it does not interpret any of the characters as control functions. The display can be cleared by loading in a new RAM control word.

Data Out

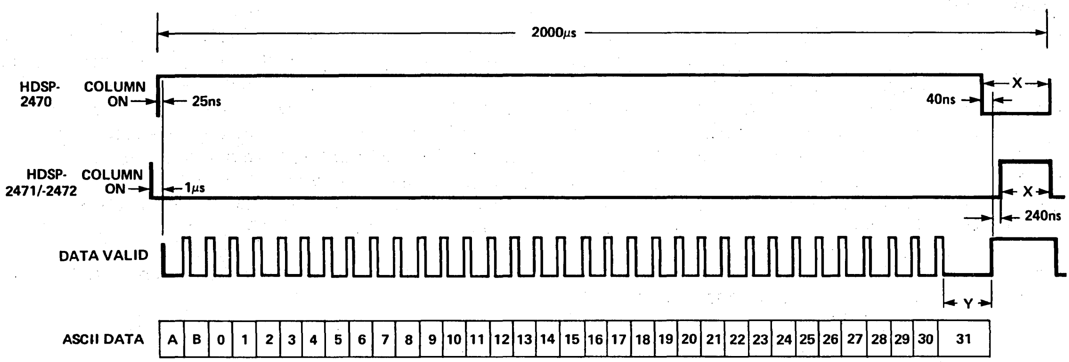
For display lengths of 32 characters or less, the data stored in the internal RAM is available to the user during the time between display refresh cycles. The system outputs a STATUS WORD, CURSOR ADDRESS, and 32 ASCII data characters. The STATUS WORD specifies the data entry mode and the display length of the system. The STATUS WORD output differs slightly from the CONTROL WORD input. This difference is depicted in Figure 8. Regardless of display length, the CURSOR ADDRESS of the rightmost character location is address 47 ($2F_{16}$) and the offscreen address of the cursor is address 48 (30_{16}). The CURSOR ADDRESS of the leftmost location is defined as address 48 minus the display length. A general formula for CURSOR ADDRESS is:

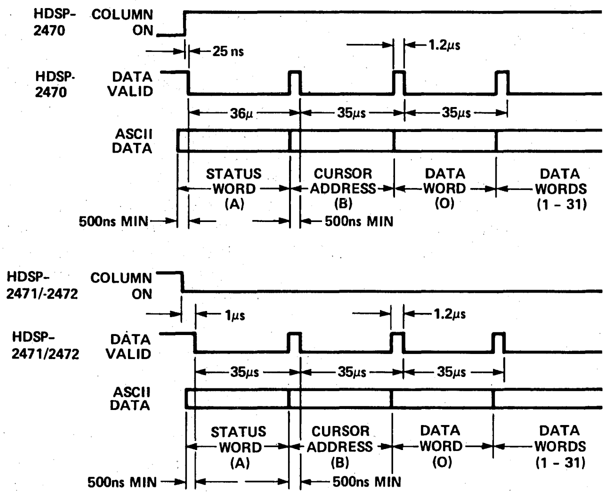
$$\text{CURSOR ADDRESS} = (47 - \text{Display Length}) + \text{Number of Characters from Left.}$$

For example, suppose the alphanumeric display is 16 characters long and the cursor was blinking at the third digit from the left. Then the CURSOR ADDRESS would be 47 - 16 + 3 or 34 (22_{16}) and the 18th ASCII data word would correspond to the ASCII character at the location of the display cursor. In Left and Block entry, the CURSOR ADDRESS specifies the location where the next ASCII data character is to be entered. In RAM entry, the CURSOR ADDRESS specifies the location to the right of the last character entered. In Right entry, the CURSOR ADDRESS is always 48 (30_{16}). The negative edge of the DATA VALID output can be used to load the 34 DATA OUT words into the user's system. The DATA OUT timing for the HDSP-247X systems are summarized in Figure 8. For displays longer than 32 characters, the system only outputs the STATUS WORD between refresh cycles.

Master/Power On Reset

When power is first applied to the system, the system clears the display and tests the state of the DATA INPUT, D_7. If $D_7 > 2.0V$, the systems loads the control word on the DATA INPUTS into the system. If $D_7 \leq .8V$ or the system sees an invalid control word, the system initializes as Left entry for a 32 character display with a flashing cursor in the leftmost location. For POWER ON RESET to function properly, the power supply must turn on at a rate > 100 V/s. In addition, the system can be reset by pulling the RESET input low for a minimum of 50 milliseconds. POWER ON/MASTER RESET timing is shown in Figure 9.





X, COLUMN OFF TIME

(HDSP-2470) = 30.5μs + 20μs X Display Length

(HDSP-2471/-2472) = 17.5μs + 17.5μs X Display Length

Y, DATA VALID TO COLUMN OFF TIME

(Display Length ≤32 Characters)

(HDSP-2470) = 813.5μs - 20μs X Display Length

(HDSP-2471/-2472) = 826.2μs - 17.5μs X Display Length

STATUS WORD FORMAT (WORD A)

D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	Y	Y	Y	Y	RAM ENTRY
0	0	1	Y	Y	Y	Y	BLOCK ENTRY
0	1	0	Y	Y	Y	Y	LEFT ENTRY
1	0	0	Y	Y	Y	Y	RIGHT ENTRY

YYYY = DISPLAY LENGTH

CURSOR ADDRESS FORMAT (WORD B)

CURSOR ADDRESS = (47 - Display Length) + No. of Characters from Left

DATA WORD FORMAT (WORDS 0-31)

STANDARD ASCII DATA Where Word (31) is Rightmost Displayed ASCII Character

Figure 8. Data Out Timing and Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

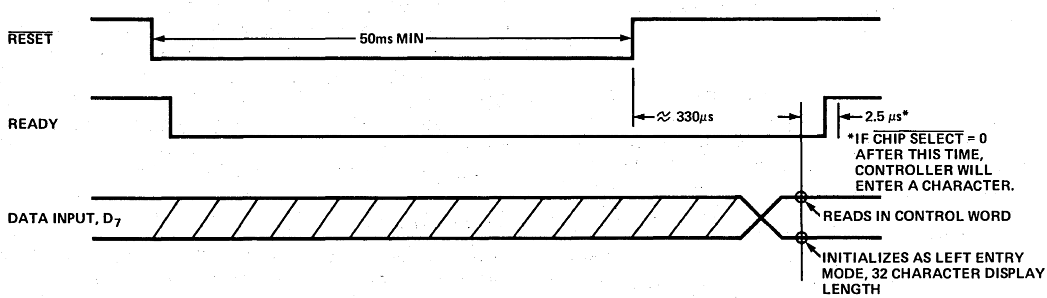


Figure 9. Power-On/Master Reset Timing for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Custom Character Sets

The HDSP-2472 system has been specifically designed to permit the user to insert a custom 128 ASCII character set. This system features a 24 pin socket that is designed to accept a custom programmed 1K X 8 PROM, EPROM, or ROM. The read only memory should have an access time $\leq$ 500ns, $I_{IL} \leq |-.4mA|$ and $I_{IH} \leq 40\mu A$. A list of pin compatible read only memories is shown in Figure 10. Jumper locations are provided on the HDSP-2472 P.C. board which allow the use of ROM's requiring chip enables tied either to 0 or 5V. For further information on ROM programming, please contact the factory.

Power Supply Requirements

The HDSP-247X Alphanumeric Display System is designed to operate from a single 5 volt supply. Total I_{CC} requirements for the HDSP-247X Alphanumeric Display Controller and HDSP-24XX Display Panel are shown in Figure 11. Peak I_{CC} is the instantaneous current required for the system. Maximum Peak I_{CC} occurs for V_{CC} = 5.25V with 7 dots ON in the same Column in all display characters. This current must be supplied by a combination of the power supply and supply filter capacitor. Maximum Average I_{CC} occurs for V_{CC} = 5.25V with 21 dots ON per character in all display characters. The inclusion of a 375 X microfarad capacitor (where X is the number of characters in the display) adjacent to the HDSP-247X Alphanumeric Display System will permit the use of a power supply capable of supplying the maximum average I_{CC}.

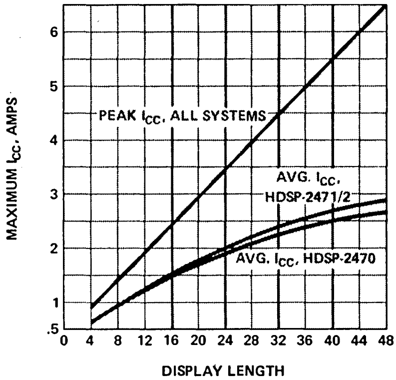


Figure 11. Maximum Peak and Average I_{CC} for the HDSP-2470/71/72 Alphanumeric Display Controller and HDSP-2000 Display.

CONNECTORS

FUNCTION	TYPE OF CONNECTOR	SUGGESTED MANUFACTURER
CONTROL/DATA ENTRY	26 Pin Ribbon Cable	3M P/N 3399-X000 Series
POWER(1)	3 Pin With Locking Ramp	Molex P/N 09-50-3031 with 08-50-0106 Terminals
DISPLAY DRIVE(2,3)	17 Pin Board to Board Pin/Socket	Pin: BERG p/n 75409-041 Socket: BERG p/n 65780-017

NOTES:
(1) Power leads should be 18-20 gauge stranded wire.
(2) The maximum lead length from the controller board to the display should not exceed 1 metre.

PART NUMBER	MANUFACTURER	TYPE	CONSTRUCTION	EXTERNAL CONNECTION* X	Y	Z
2758	Intel	EPROM	NMOS	GND	GND	+5
7608	Harris	PROM	BIPOLAR-NiCr	NC	NC	NC
3628-4	Intel	PROM	BIPOLAR-Si	+5	+5	GND
82S2708	Signetics	PROM	BIPOLAR-NiCr	NC	NC	NC
6381	Monolithic Mem.	PROM	BIPOLAR-NiCr	+5	+5	GND
6385	Monolithic Mem.	PROM	BIPOLAR-NiCr	NC	NC	NC
87S228	National	PROM	BIPOLAR-TiW	+5	+5	GND
93451	Fairchild	PROM	BIPOLAR-NiCr	+5	+5	GND
68308	Motorola	ROM	NMOS	**	NC	NC
2607	Signetics	ROM	NMOS	**	NC	NC
30000	Mostek	ROM	NMOS	**	+5	NC

*Board jumpers correspond to pins 18, 19 & 21 of ROM.
**As defined by customer

Figure 10. Pin Compatible 1K x 8 Read Only Memories for the HDSP-2472 Alphanumeric Display Controller.

Display Boards/Hardware

The mechanical layout of the HDSP-247X Series allows direct mating of the controller P.C. board to a compatible series of display boards available from Hewlett-Packard. These display boards consist of matched and tested HDSP-2000 clusters soldered to a P.C. board.

Included with the controller board are four locking circuit board support nylon standoffs (Richco LCBS-4). This hardware allows the controller board to interconnect with any of the standard display boards. Figure 12 depicts correct assembly technique.

Assembly Steps

1. Insert the standoffs into .151 diameter holes (noted as "S" on Figure 12. The long end of the standoffs should protrude through the controller board side.
2. Position the controller board and display board with the components and displays facing out. The HP logo should be in the upper left corner when viewed facing the boards. Insert the standoffs through the mating holes on the display board and press the boards together so that the standoffs lock in place.
3. Insert the pins from the display board into the socket on the controller board.

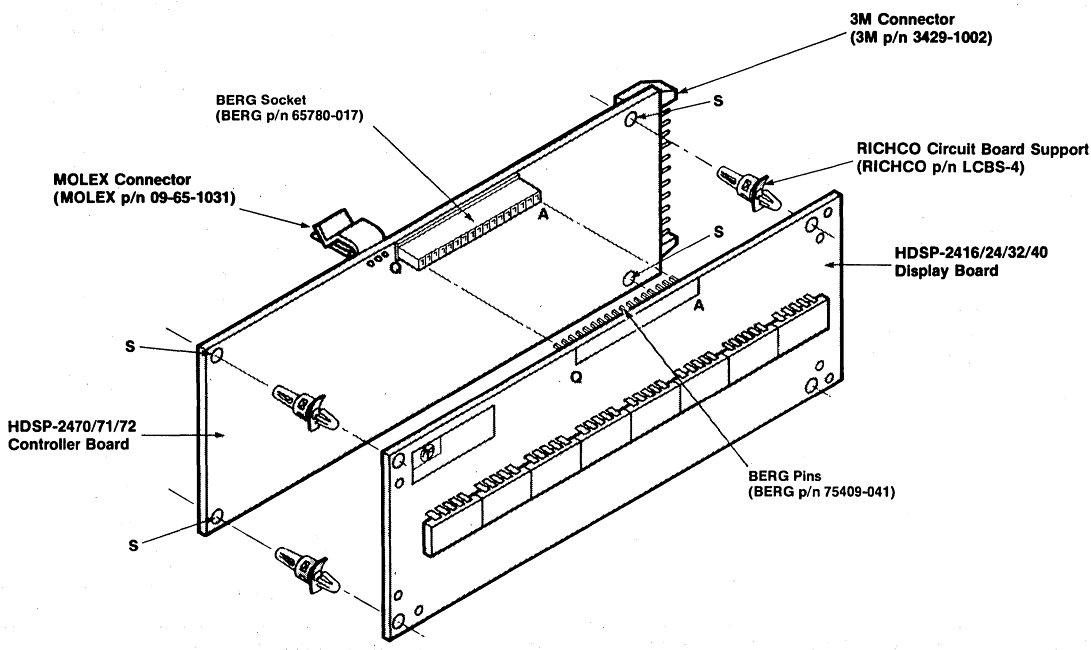


Figure 12. Assembly Drawing.

Package Dimensions

UNLESS OTHERWISE SPECIFIED,,DIMENSIONS ARE IN mm AND (INCHES)

HDSP-2470/-2471/-2472

PIN	DESCRIPTION
1	$\overline{\text{CHIP SELECT}}$
2	DATA VALID
3	RAM ADDRESS, A_0
4	DATA IN, D_7
5	RAM ADDRESS, A_1
6	$\overline{\text{RESET}}$
7	RAM ADDRESS, A_2
8	DATA OUT, DO_6
9	RAM ADDRESS, A_3
10	DATA OUT, DO_5
11	DATA IN, D_0
12	DATA OUT' DO_4
13	DATA IN, D_1
14	DATA OUT, DO_3
15	DATA IN, D_2
16	DATA OUT, DO_2
17	DATA IN, D_3
18	DATA OUT, DO_1
19	DATA IN, D_4
20	DATA OUT, DO_0
21	DATA IN, D_5
22	READY
23	DATA IN, D_6
24	COLUMN ON
25	RAM ADDRESS, A_4
26	DISPLAY BLANK, V_B

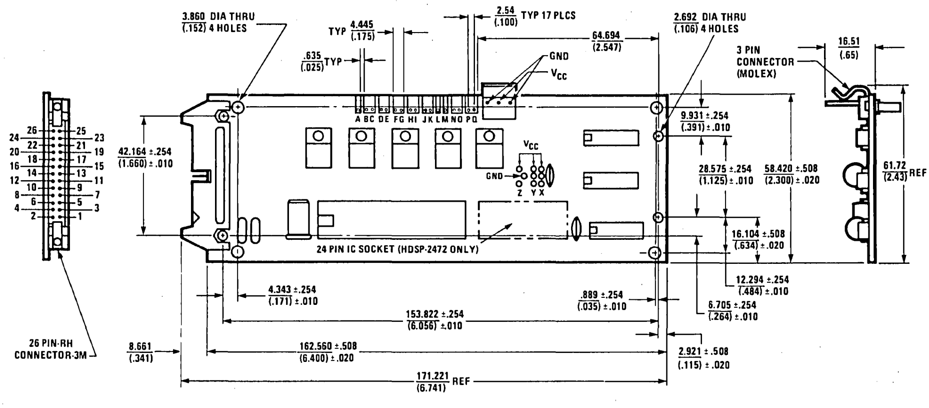
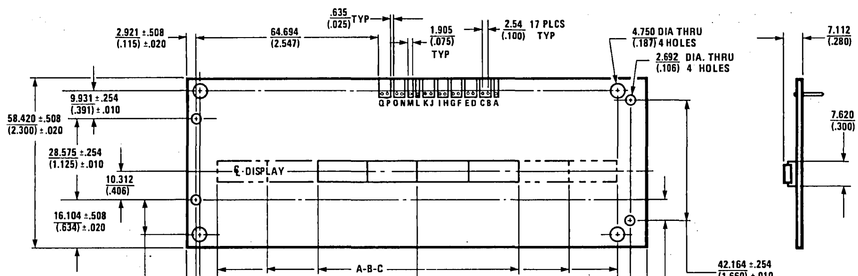


Figure 13. HDSP-2470/-2471/-2472

HDSP-2416/-2424/-2432/-2440
HDSP-2470/-2471/-2472

PIN	DESCRIPTION
A	DISPLAY BLANK, V_B
B,C	$COLUMN_1$
D,E	$COLUMN_2$
F,G	$COLUMN_3$
H,I	$COLUMN_4$
J,K	$COLUMN_5$
L	CLOCK
M	DISPLAY DATA
N,O	V_{CC}
P,Q	GND



A	HDSP-2416	71.120 (2.800)
B	HDSP-2424	106.680 (4.200)
C	HDSP-2432	142.240 (5.600)

Figure 14. HDSP-2416/-2424/-2432

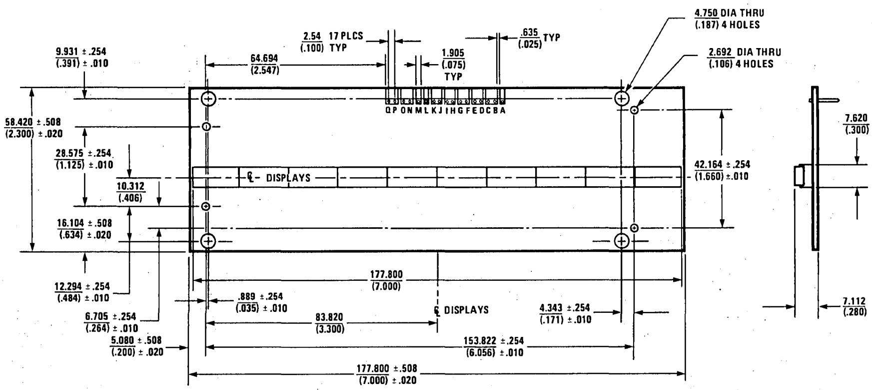


Figure 15. HDSP-2440

SOLID STATE DISPLAYS

HEWLETT PACKARD

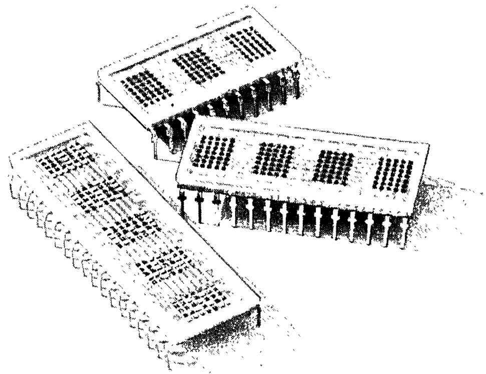
LED SOLID STATE ALPHANUMERIC INDICATOR

5082-7100
5082-7101
5082-7102

TECHNICAL DATA JANUARY 1986

Features

- 5 x 7 LED MATRIX CHARACTER
- LARGE 6.9 mm (.27 INCH) CHARACTER HEIGHT
- EXTREMELY WIDE TEMP. RANGE
- COMPACT 15.2 mm (.600 INCH) GLASS/CERAMIC DIP
- WIDE VIEWING ANGLE
- RUGGED, SHOCK RESISTANT



Typical Applications

- COMPUTER PERIPHERALS
- MILITARY EQUIPMENT
- INDUSTRIAL EQUIPMENT
- AVIONICS

Description

The Hewlett-Packard 5082-7100 Series is an X-Y addressable, 5 x 7 LED Matrix capable of displaying the full alphanumeric character set. This alphanumeric indicator series is available in 3, 4, or 5 character end-stackable clusters. The clusters permit compact presentation of information, ease of character alignment, minimum number of interconnections, and compatibility with multiplexing driving schemes.

The **5082-7100** is a three character cluster.
The **5082-7101** is a four character cluster.
The **5082-7102** is a five character cluster.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current Per LED (Duration < 1 ms)	I_{PEAK}		100	mA
Average Current Per LED	I_{AVG}		10	mA
Power Dissipation Per Character (All diodes lit)[1]	P_D		700	mW
Operating Temperature, Case	T_C	–55	95	°C
Storage Temperature	T_S	–55	100	°C
Reverse Voltage Per LED	V_R		4	V

Note 1: At 25°C Case Temperature; derate 8.5 mW/°C above 25°C.

Electrical / Optical Characteristics at $T_C = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units
Peak Luminous Intensity Per LED (Character Average) @ Pulse Current of 100mA/LED	I_V (PEAK)	1.0	2.2		mcd
Reverse Current Per LED @ $V_R = 4V$	I_R		10		µA
Peak Forward Voltage @ Pulse Current of 50mA/LED	V_F		1.7	2.0	V
Peak Wavelength	λ_{PEAK}		655		nm
Spectral Line Halfwidth	$\Delta\lambda_{1/2}$		30		nm
Rise and Fall Times [1]	t_r, t_f		10		ns

Note 1. Time for a 10% - 90% change of light intensity for step change in current.

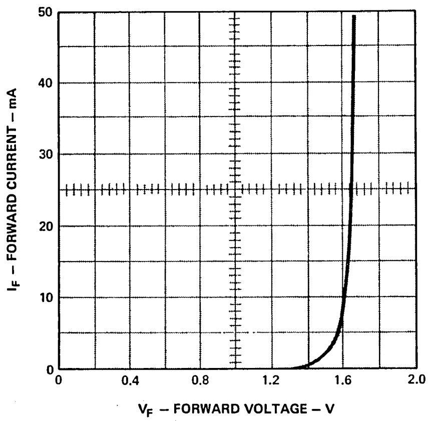


Figure 1. Forward Current-Voltage Characteristic.

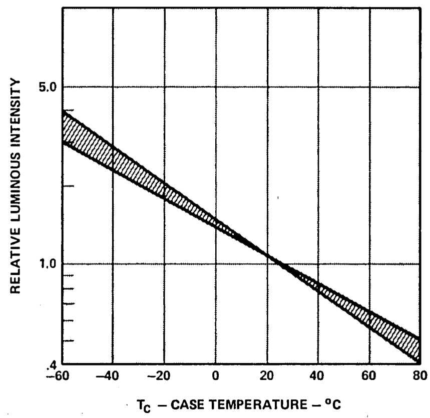


Figure 2. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

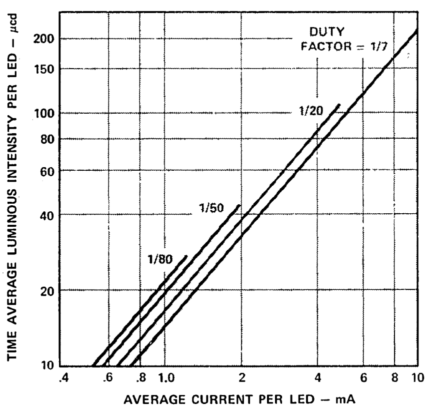


Figure 3. Typical Time Average Luminous Intensity per LED vs. Average Current per LED.

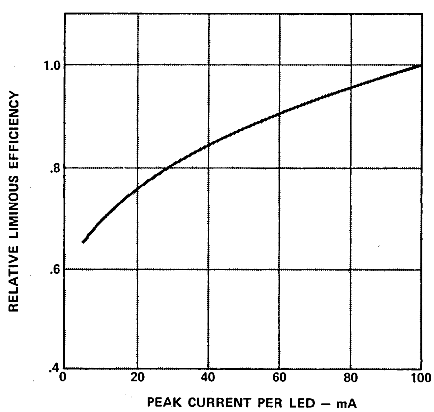
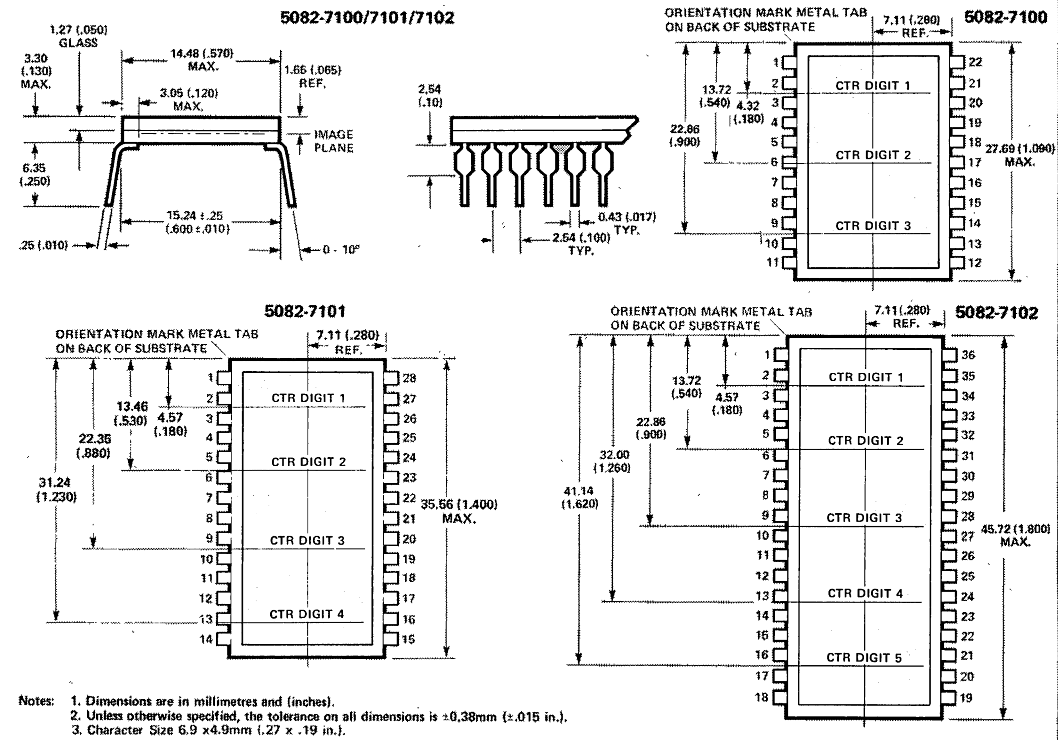


Figure 4. Typical Relative Luminous Efficiency vs. Peak Current per LED.

SOLID STATE DISPLAYS

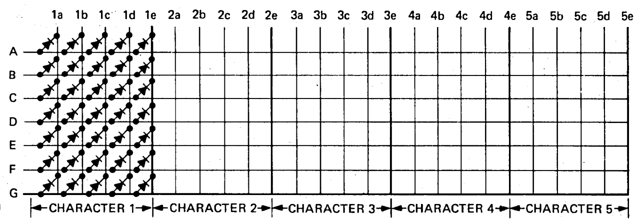
Package Dimensions and Pin Configurations



Notes:
1. Dimensions are in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±0.38mm (±.015 in.).
3. Character Size 6.9 x4.9mm (.27 x .19 in.).

Device Pin Description

5082-7100				5082-7101				5082-7102			
Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Anode G	12	Anode B	1	N/C	15	Anode C	1	N/C	19	5e
2	1c	13	3d	2	1c	16	4c	2	1c	20	5c
3	1d	14	3b	3	1e	17	4a	3	1e	21	5a
4	Anode F	15	Anode A	4	Anode G	18	Anode B	4	Anode F	22	Anode D
5	Anode E	16	2e	5	2b	19	3e	5	2b	23	4e
6	2b	17	2c	6	2d	20	3b	6	2d	24	4c
7	2d	18	2a	7	Anode D	21	3a	7	2e	25	N/C
8	Anode C	19	Anode D	8	Anode E	22	2e	8	Anode E	26	Anode C
9	3a	20	1e	9	3c	23	2c	9	3c	27	3d
10	3c	21	1b	10	3d	24	2a	10	3e	28	3b
11	3e	22	1a	11	Anode F	25	Anode A	11	Anode G	29	3a
				12	4b	26	1d	12	4a	30	Anode B
				13	4d	27	1b	13	4b	31	2c
				14	4e	28	1a	14	4d	32	2a
								15	N/C	33	Anode A
								16	5b	34	1d
								17	5d	35	1b
								18	N/C	36	1a



5082-7100/7101/7102
Schematic Wiring Diagram

Operating Considerations

ELECTRICAL

The 5 x 7 matrix of LED's, which make up each character, are X-Y addressable. This allows for a simple addressing, decoding and driving scheme between the display module and customer furnished logic.

There are three main advantages to the use of this type of X-Y addressable array:

1. It is an elementary addressing scheme and provides the least number of interconnection pins for the number of diodes addressed. Thus, it offers maximum flexibility toward integrating the display into particular applications.
2. This method of addressing offers the advantage of sharing the Read-Only-Memory character generator among several display elements. One character generating ROM can be shared over 25 or more 5 x 7 dot matrix characters with substantial cost savings.
3. In many cases equipment will already have a portion of the required decoder/driver (timing and clock circuitry plus buffer storage) logic circuitry available for the display.

To form alphanumeric characters a method called "scanning" or "strobing" is used. Information is addressed to the display by selecting one row of diodes at a time, energizing the appropriate diodes in that row and then proceeding to the next row. After all rows have been excited one at a time, the process is repeated. By scanning through all rows at least 100 times a second, a flicker free character can be produced. When information moves sequentially from row to row of the display (top to bottom) this is row scanning, as illustrated in Figure 5. Information can also be moved from column to column (left to right across the display) in a column scanning mode. For most applications (5 or more characters to share the same ROM) it is more economical to use row scanning.

MECHANICAL/THERMAL MOUNTING

The solid state display typically operates with 200 mW power dissipation per character. However, if the operating conditions are such that the power dissipation exceeds the derated maximum allowable value, the device should be heat sunk. The usual mounting technique combines mechanical support and thermal heat sinking in a common structure. A metal strap or bar can be mounted behind the display using silicone grease to insure good thermal control. A well-designed heat sink can limit the case temperature to within 10°C of ambient.

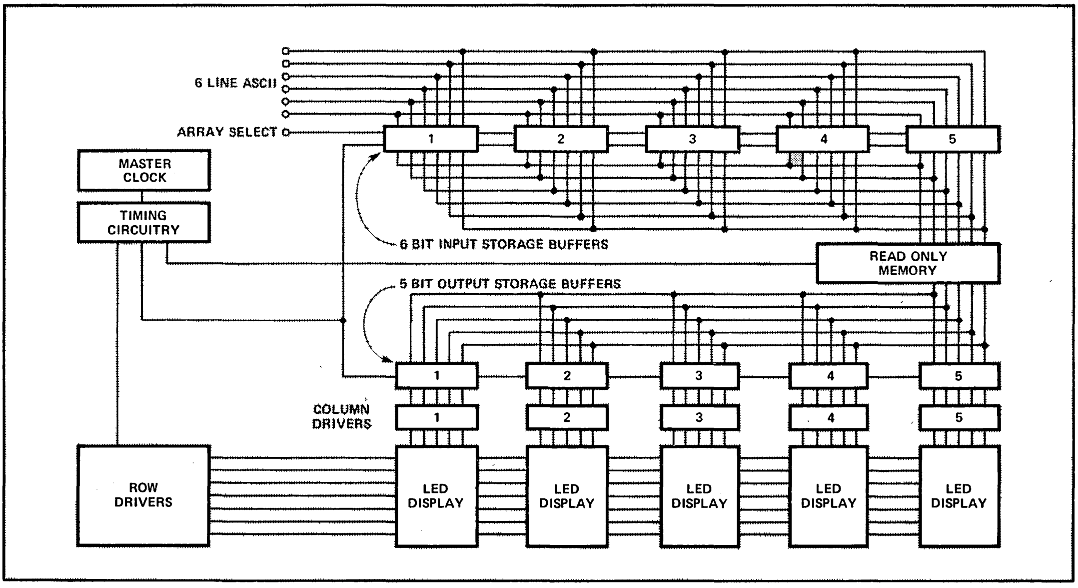


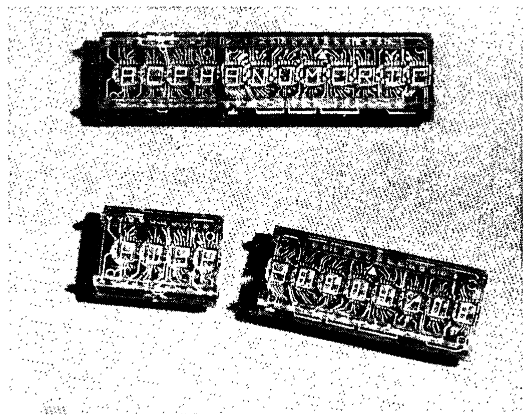
Figure 5. Row Scanning Block Diagram.

HEWLETT PACKARD

16 SEGMENT SOLID STATE ALPHANUMERIC DISPLAY

HDSP-6504
HDSP-6508

TECHNICAL DATA JANUARY 1986



Features

- **ALPHANUMERIC**
  Displays 64 Character ASCII Set and Special Characters
- **16 SEGMENT FONT PLUS CENTERED D.P. AND COLON**
- **3.81mm (0.150") CHARACTER HEIGHT**
- **APPLICATION FLEXIBILITY WITH PACKAGE DESIGN**
  4 and 8 Character Dual-In-Line Packages
  End Stackable-On Both Ends for 8 Character and On One End for 4 Character
  Sturdy Gold-Plated Leads on 2.54mm (0.100") Centers
  Environmentally Rugged Package
  Common Cathode Configuration
- **LOW POWER**
  As Low as 1.0-1.5mA Average Per Segment Depending on Peak Current Levels
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Segment Font
  High On/Off Contrast
  6.35mm (0.250") Character Spacing
  Excellent Character Alignment
  Excellent Readability at 2 Metres
- **SECONDARY BARREL MAGNIFIER AVAILABLE**
  Increases Character Height to 4.45 mm (0.175")
- **SUPPORT ELECTRONICS**
  Can Be Driven With ROM Decoders and Drivers
  Easy Interfacing With Microprocessors and LSI Circuitry
- **CATEGORIZED FOR LUMINOUS INTENSITY**

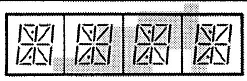
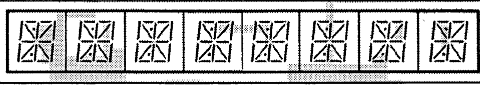
Description

The HDSP-6504 and HDSP-6508 are 3.81mm (0.150") sixteen segment GaAsP red alphanumeric displays mounted in 4 character and 8 character dual-in-line package configurations that permit mounting on PC boards or in standard IC sockets. The monolithic light emitting diode character is magnified by the integral lens which increases both character size and luminous intensity, thereby making low power consumption possible. The rugged package construction, enhanced by the backfill design, offers extended environmental capabilities compared to the standard PC board/lens type of display package. Its good temperature cycling capability is the result of the air gap which exists between the semiconductor chip/wire bond assembly and the lens. In addition to the sixteen segments, a centered D.P. and colon are included. Character spacing yields 4 characters per inch.

Applications

These alphanumeric displays are attractive for applications such as computer peripherals and terminals, computer base emergency mobile units, automotive instrument panels, desk top calculators, in-plant control equipment, hand-held instruments and other products requiring low power, display compactness and alphanumeric display capability.

Device Selection Guide

Characters Per Display	Configuration: Device	Configuration: Package	Part No. HDSP-
4		(Figure 6)	6504
8		(Figure 7)	6508

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
I_{PEAK}	Peak Forward Current Per Segment or DP (Duration ≤ 312μs)		200	mA
I_{AVG}	Average Current Per Segment or DP[1]		7	mA
P_D	Average Power Dissipation Per Character[1,2]		138	mW
T_A	Operating Temperature, Ambient	-40	85	°C
T_S	Storage Temperature	-40	100	°C
V_R	Reverse Voltage		5	V
	Solder Temperature at 1.59mm (1/16 inch) below seating plane, t ≤ 3 Seconds		260	°C

NOTES:
1. Maximum allowed drive conditions for strobed operation are derived from Figures 1 and 2. See electrical section of operational considerations.
2. Derate linearly above T_A = 50°C at 2.17mW/°C. P_D Max. (T_A = 85°C) = 62mW.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_V	Luminous Intensity, Time Average, Character Total with 16 Segments Illuminated [3,4]	I_{PEAK} = 30mA 1/16 Duty Factor	0.40	1.65		mcd
V_F	Forward Voltage Per Segment or DP	I_F = 30mA (One Segment On)		1.6	1.9	V
λ_{PEAK}	Peak Wavelength			655		nm
λ_d	Dominant Wavelength [5]			640		nm
I_R	Reverse Current Per Segment or DP	V_R = 5V		10		μA
$\Delta V_F/\Delta°C$	Temperature Coefficient of Forward Voltage			-2		mV/°C
$R\theta_{J-PIN}$	Thermal Resistance LED Junction-to-Pin			232		°C/W/ Seg

NOTES:
3. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus each segment will appear with equal brightness to the eye.
4. Each character of the display is matched for luminous intensity at the test conditions shown. Operation of the display at lower peak currents may cause intensity mismatch within the display. Operation at peak currents less than 7 mA will cause objectionable display segment matching.
5. The dominant wavelength, λd, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.

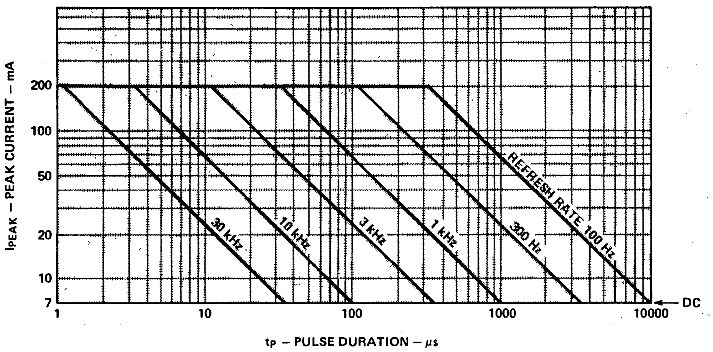


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration. Derate derived operating conditions above $T_A = 50°C$ using Figure 2.

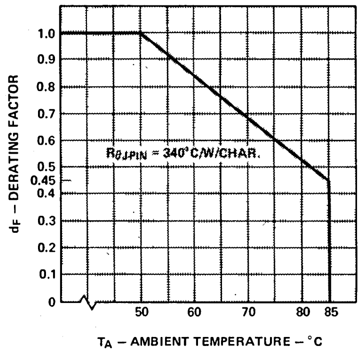


Figure 2. Temperature Derating Factor For Peak Current per Segment vs. Ambient Temperature. $T_JMAX = 110°C$

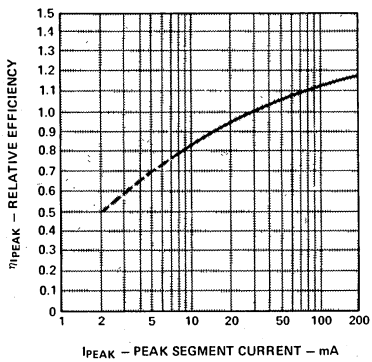


Figure 3. Relative Luminous Efficiency (Luminous Intensity Per Unit Current) vs. Peak Segment Current.

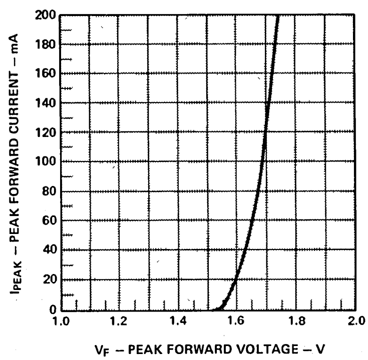
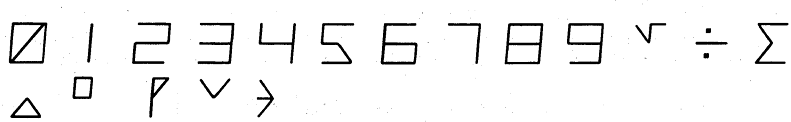


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

Figure 5. Typical 64 Character ASCII Set.



Additional Character Font

Package Dimensions

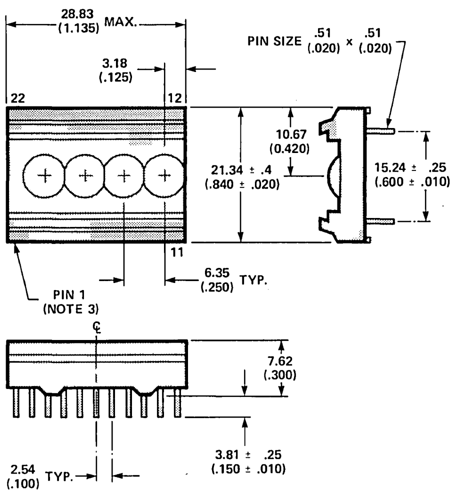


Figure 6. HDSP-6504

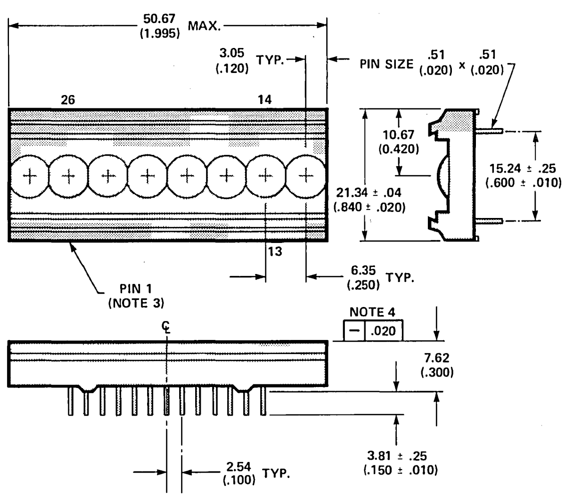


Figure 7. HDSP-6508

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY INK DOT ADJACENT TO LEAD.

Magnified Character Font Description

DEVICES
HDSP-6504
HDSP-6508

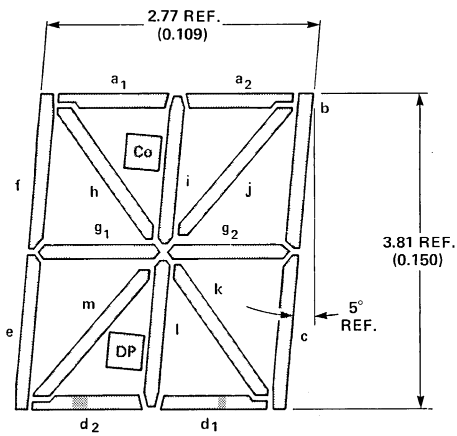


Figure 8.

Device Pin Description

Pin No.	Function HDSP-6504		HDSP-6508	
1	Anode	Segment g_1	Anode	Segment g_1
2	Anode	Segment DP	Anode	Segment DP
3	Cathode	Digit 1	Cathode	Digit 1
4	Anode	Segment d_2	Anode	Segment d_2
5	Anode	Segment l	Anode	Segment l
6	Cathode	Digit 3	Cathode	Digit 3
7	Anode	Segment e	Anode	Segment e
8	Anode	Segment m	Anode	Segment m
9	Anode	Segment k	Anode	Segment k
10	Cathode	Digit 4	Cathode	Digit 4
11	Anode	Segment d_1	Anode	Segment d_1
12	Anode	Segment j	Cathode	Digit 6
13	Anode	Segment C_O	Cathode	Digit 8
14	Anode	Segment g_2	Cathode	Digit 7
15	Anode	Segment a_2	Cathode	Digit 5
16	Anode	Segment i	Anode	Segment j
17	Cathode	Digit 2	Anode	Segment C_O
18	Anode	Segment b	Anode	Segment g_2
19	Anode	Segment a_1	Anode	Segment a_2
20	Anode	Segment c	Anode	Segment i
21	Anode	Segment h	Cathode	Digit 2
22	Anode	Segment f	Anode	Segment b
23			Anode	Segment a_1
24			Anode	Segment c
25			Anode	Segment h
26			Anode	Segment f

Operational Considerations

ELECTRICAL

The HDSP-6504 and -6508 devices utilize large monolithic 16 segment GaAsP LED chips with centered decimal point and colon. Like segments of each digit are electrically interconnected to form an 18 by N array, where N is the quantity of characters in the display. In the driving scheme the decimal point or colon is treated as a separate character with its own time frame.

These displays are designed specifically for strobed (multiplexed) operation. Under normal operating situations the maximum number of illuminated segments needed to represent a given character is 10. Therefore, except where noted, the information presented in this data sheet is for a maximum of 10 segments illuminated per character.*

The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.85V + I_{PEAK}\ (1.8\Omega)$
For: $30mA \leq I_{PEAK} \leq 200mA$
$V_F = 1.58V + I_{PEAK}\ (10.7\Omega)$
For: $10mA \leq I_{PEAK} \leq 30mA$

OPTICAL AND CONTRAST ENHANCEMENT

Each large monolithic chip is positioned under a separate element of a plastic aspheric magnifying lens, producing a magnified character height of 3.81 mm (.150 inch). The aspheric lens provides wide included viewing angles of typically 75 degrees horizontal and 75 degrees vertical with low off-axis distortion. These two features, coupled with the very high segment luminous sterance, provide to the user a display with excellent readability in bright ambient light for viewing distances in the range of 2 meters. Effective contrast enhancement can be obtained by employing any of the following optical filter products: Panelgraphic: Ruby Red 60, Dark Red 63 or Purple 90; SGL Homalite: H100-1605 Red or H100-1804 Purple, Plexiglas 2423. For very bright ambients, such as indirect sunlight, the 3M Light Control Film is recommended: Red 655, Violet, Purple or Neutral Density.

For those applications requiring only 4 or 8 characters, a secondary barrel magnifier, HP part number HDSP-6505 (four character) and -6509 (eight character), may be inserted into support grooves on the primary magnifier. This secondary magnifier increases the character height to 4.45mm (.175 inch) without loss of horizontal viewing angle.

MECHANICAL

These devices are constructed by LED die attaching and wire bonding to a high temperature PC board substrate. A precision molded plastic lens is attached to the PC board and the resulting assembly is backfilled with a sealing epoxy to form an environmentally sealed unit.

The four character and eight character devices can be end stacked to form a character string which is a multiple of a basic four character grouping. As an example, one -6504 and two -6508 devices will form a 20 character string. These devices may be soldered onto a printed circuit board or inserted into 24 and 28 pin DIP LSI sockets. The socket spacing must allow for device end stacking.

Suitable conditions for wave soldering depend upon the specific kind of equipment and procedure used. For more information, consult the local HP Sales Office or Hewlett-Package Components, Palo Alto, California.

*More than 10 segments may be illuminated in a given character, provided the maximum allowed character power dissipation, temperature derated, is not exceeded.

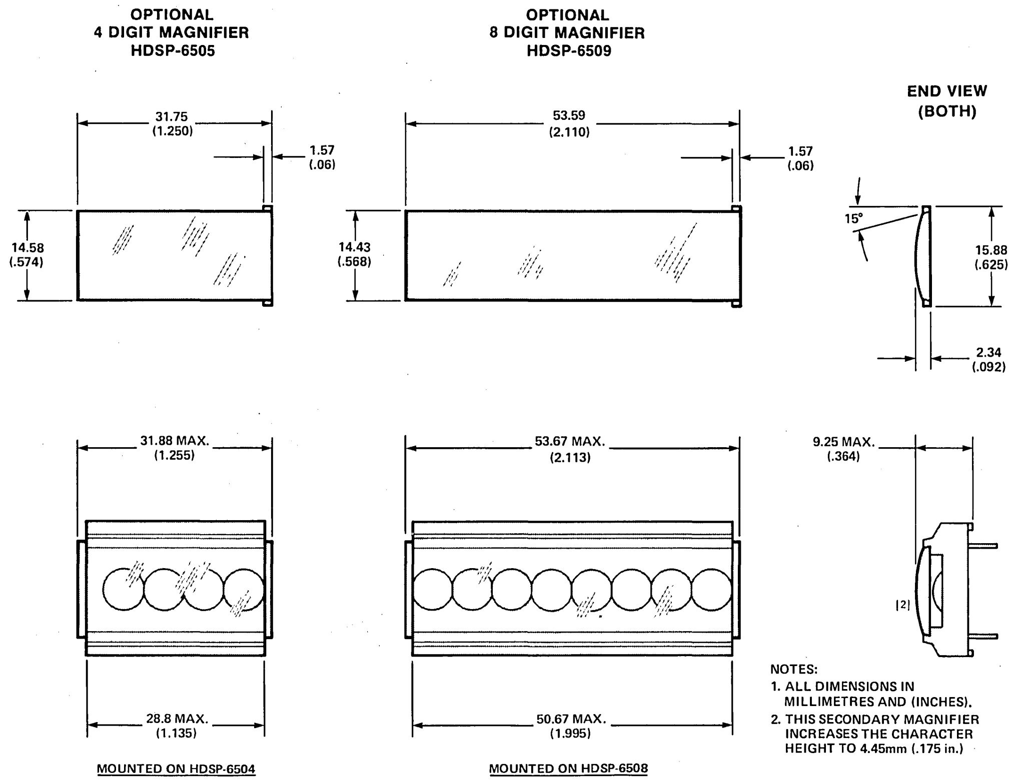


Figure 9. Design Data for Optional Barrel Magnifier in Single Display Applications.

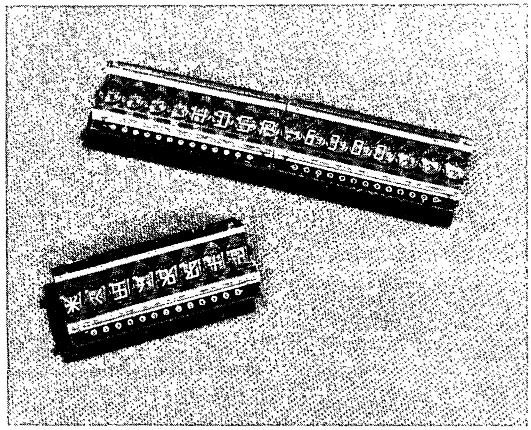
SOLID STATE DISPLAYS

HEWLETT PACKARD

16 SEGMENT SOLID STATE ALPHANUMERIC DISPLAY

HDSP-6300

TECHNICAL DATA JANUARY 1986



Features

- **ALPHANUMERIC**
  Displays 64 Character ASCII Set and Special Characters
- **16 SEGMENT FONT PLUS CENTERED D.P. AND COLON**
- **3.56mm (0.140") CHARACTER HEIGHT**
- **APPLICATION FLEXIBILITY WITH PACKAGE DESIGN**
  8 Character Dual-In-Line Package
  End Stackable
  Sturdy Leads on 2.54mm (0.100") Centers
  Common Cathode Configuration
- **LOW POWER**
  As Low as 1.0-1.5mA Average Per Segment Depending on Peak Current Levels
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Segment Font
  High On/Off Contrast
  5.08mm (0.200") Character Spacing
  Excellent Character Alignment
  Excellent Readability at 1.5 Metres
- **SUPPORT ELECTRONICS**
  Can Be Driven With ROM Decoders and Drivers
  Easy Interfacing With Microprocessors and LSI Circuitry
- **CATEGORIZED FOR LUMINOUS INTENSITY**

Description

The HDSP-6300 is a sixteen segment GaAsP red alphanumeric display mounted in an 8 character dual-in-line package configuration that permits mounting on PC boards or in standard IC sockets. The monolithic light emitting diode character is magnified by the integral lens which increases both character size and luminous intensity, thereby making low power consumption possible. The sixteen elements consist of sixteen segments for alphanumeric and special characters plus centered decimal point and colon for good visual aesthetics. Character spacing yields 5 characters per inch.

Applications

These alphanumeric displays are attractive for applications such as computer peripherals and mobile terminals, desk top calculators, in-plant control equipment, hand-held instruments and other products requiring low power, display compactness and alphanumeric display capability.

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
I_{PEAK}	Peak Forward Current Per Segment or DP (Duration ≤ 417μs)		150	mA
I_{AVG}	Average Current Per Segment or DP[1]		6.25	mA
P_D	Average Power Dissipation Per Character[1,2]		133	mW
T_A	Operating Temperature, Ambient	-40	85	°C
T_S	Storage Temperature	-40	100	°C
V_R	Reverse Voltage		5	V
	Solder Temperature at 1.59mm (1/16 inch) below seating plane, t ≤ 5 Seconds		260	°C

NOTES:
1. Maximum allowed drive conditions for strobed operation are derived from Figures 1 and 2. See electrical section of operational considerations.
2. Derate linearly above T_A = 50°C at 2.47 mW/°C. P_D Max. (T_A = 85°C) = 47 mW.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_V	Luminous Intensity, Time Average, Character Total with 16 Segments Illuminated [3,4]	I_{PEAK} = 24mA 1/16 Duty Factor	400	1200		μcd
V_F	Forward Voltage Per Segment or DP	I_F = 24mA (One Segment On)		1.6	1.9	V
λ_{PEAK}	Peak Wavelength			655		nm
λ_d	Dominant Wavelength [5]			640		nm
I_R	Reverse Current Per Segment or DP	V_R = 5V		10		μA
$R\theta_{J-PIN}$	Thermal Resistance LED Junction-to-Pin per Character			250		°C/W/ Char.

NOTES:
3. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus each segment will appear with equal brightness to the eye.
4. Each character of the display is matched for luminous intensity at the test conditions shown. Operation of the display at lower peak currents may cause intensity mismatch within the display. Operation at peak currents less than 7 mA will cause objectionable display segment matching.
5. The dominant wavelength, λd, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.

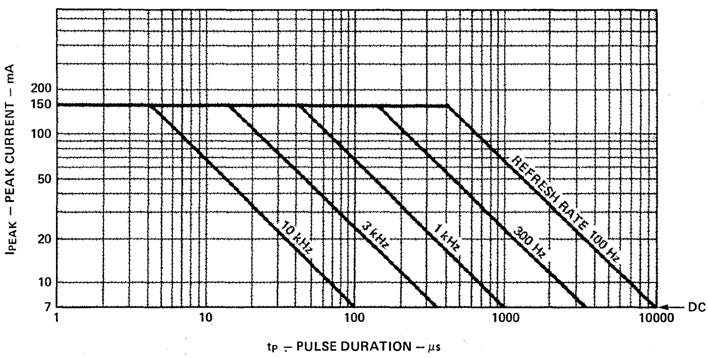


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration. Derate derived operating conditions above T_A = 50°C using Figure 2.

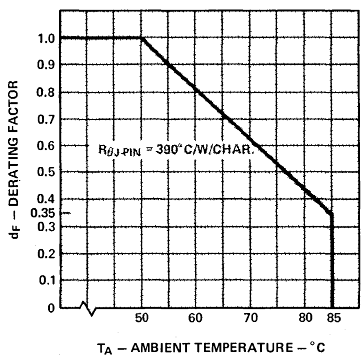


Figure 2. Temperature Derating Factor For Peak Current per Segment vs. Ambient Temperature. T_JMAX = 110°C

SOLID STATE DISPLAYS

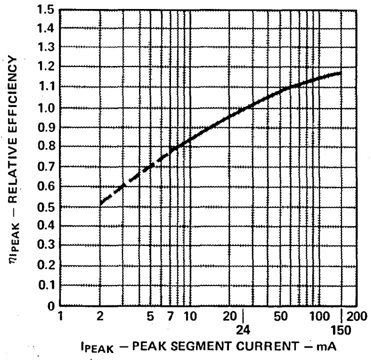


Figure 3. Relative Luminous Efficiency (Luminous Intensity Per Unit Current) vs. Peak Segment Current.

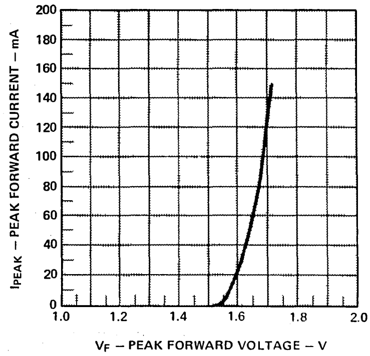


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

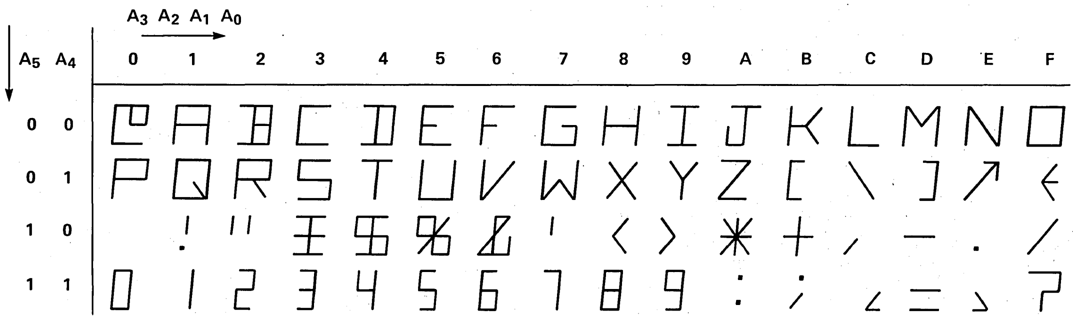
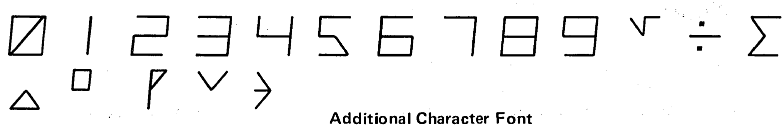
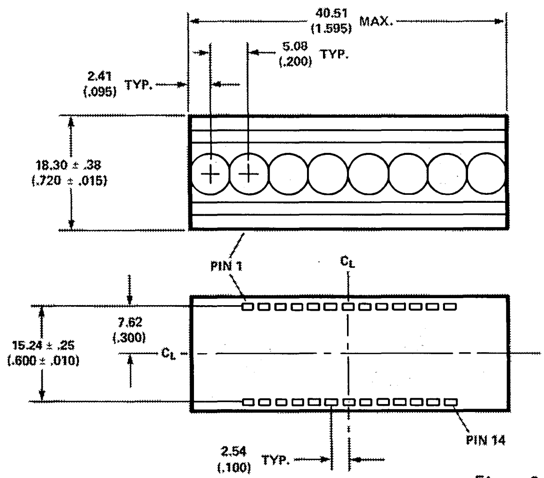
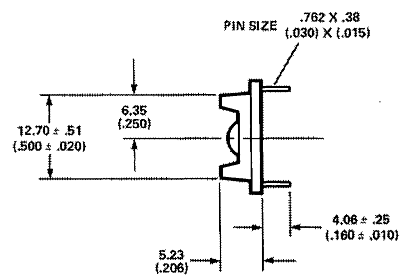


Figure 5. Typical 64 Character ASCII Set.



Additional Character Font





NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY DOT ADJACENT TO LEAD.

Figure 6.

Magnified Character Font Description

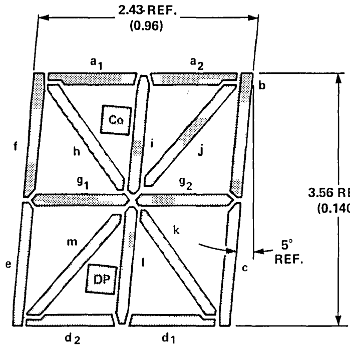


Figure 7.

Device Pin Description

Pin No.	Function	
1	Anode	Segment K
2	Anode	Segment D_1
3	Anode	Segment C
4	Cathode	Digit 1
5	Cathode	Digit 2
6	Cathode	Digit 3
7	Cathode	Digit 4
8	Anode	Segment L
9	Anode	Segment G_2
10	Anode	Segment E
11	Anode	Segment M
12	Anode	Segment D_2
13	Anode	Segment DP
14	Anode	Segment A_2
15	Anode	Segment I
16	Anode	Segment J
17	Cathode	Digit 8
18	Cathode	Digit 7
19	Cathode	Digit 6
20	Cathode	Digit 5
21	Anode	Segment C_O
22	Anode	Segment G_1
23	Anode	Segment B
24	Anode	Segment F
25	Anode	Segment H
26	Anode	Segment A_1

Operational Considerations

ELECTRICAL

The HDSP-6300 device utilizes large monolithic 16 segment plus centered decimal point and colon GaAsP LED chips. Like segments of each digit are electrically interconnected to form an 18 by N array, where N is the quantity of characters in the display. In the driving scheme the decimal point or colon is treated as a separate character with its own time frame.

This display is designed specifically for strobed (multiplexed) operation. Under normal operating situations the maximum number of illuminated segments needed to represent a given character is 10. Therefore, except where noted, the information presented in this data sheet is for a maximum of 10 segments illuminated per character.*

The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.85V + I_{PEAK}\ (1.8\Omega)$
For $30mA \leq I_{PEAK} \leq 150mA$
$V_F = 1.58V + I_{PEAK}\ (10.7\Omega)$
For $10mA \leq I_{PEAK} \leq 30mA$

*More than 10 segments may be illuminated in a given character, provided the maximum allowed character power dissipation, temperature derated, is not exceeded.

SOLID STATE DISPLAYS

OPTICAL AND CONTRAST ENHANCEMENT

Each large monolithic chip is positioned under a separate element of a plastic aspheric magnifying lens producing a magnified character height of 3.56mm (0.140 inch). The aspheric lens provides wide included viewing angles of 60 degrees horizontal and 55 degrees vertical with low off axis distortion. These two features, coupled with the very high segment luminous sterance, provide to the user a display with excellent readability in bright ambient light for viewing distances in the range of 1.5 metres. Effective contrast enhancement can be obtained by employing an optical filter product such as Panelgraphic Ruby Red 60, Dark Red 63 or Purple 90; SGL Homalite H100-1605 Red or H100-1804 Purple; or Plexiglas 2423. For very bright ambients, such as indirect sunlight, the 3M Red 655 or Neutral Density Light Control Film is recommended.

MECHANICAL

This device is constructed by LED die attaching and wire bonding to a high temperature PC board substrate. A precision molded plastic lens is attached to the PC board.

The HDSP-6300 can be end stacked to form a character string which is a multiple of a basic eight character grouping. These devices may be soldered onto a printed circuit board or inserted into 28 pin DIP LSI sockets. The socket spacing must allow for device end stacking.

Suitable conditions for wave soldering depend upon the specific kind of equipment and procedure used. It is recommended that a non-activated rosin core wire solder or a low temperature deactivating flux and solid wire solder be used in soldering operations. For more information, consult the local HP Sales Office or Hewlett-Packard Components, Palo Alto, California.

HEWLETT PACKARD

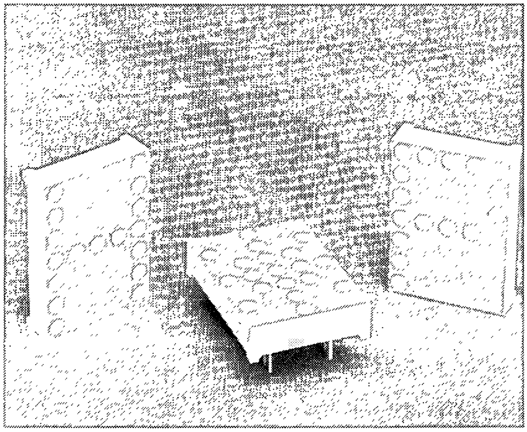
26.67mm (1.05 inch) 5x7 DOT MATRIX ALPHANUMERIC DISPLAY

HIGH EFFICIENCY RED HDSP-4501/4503

TECHNICAL DATA JANUARY 1986

Features

- LARGE 1 INCH CHARACTER HEIGHT
- 5 x 7 DOT MATRIX FONT
- VIEWABLE UP TO 18 METERS (60 FEET)
- END AND SIDE STACKABLE
- IDEAL FOR GRAPHICS PANELS
- EXCELLENT CHARACTER APPEARANCE
- AVAILABLE IN COMMON ANODE ROW AND COMMON CATHODE ROW CONFIGURATIONS
- CATEGORIZED FOR INTENSITY
- MECHANICALLY RUGGED



Description

The HDSP-4501/4503 are high efficiency red alphanumeric displays. These displays have a one inch tall 5 x 7 dot matrix character font which provides readability up to 18 meters. Each LED element is mounted at the base of a diffusing cavity which provides uniform dot size, spacing and appearance.

These devices utilize a standard 10.16 mm (0.4 in) dual-in-lead configuration that permits mounting on PC boards or in IC sockets.

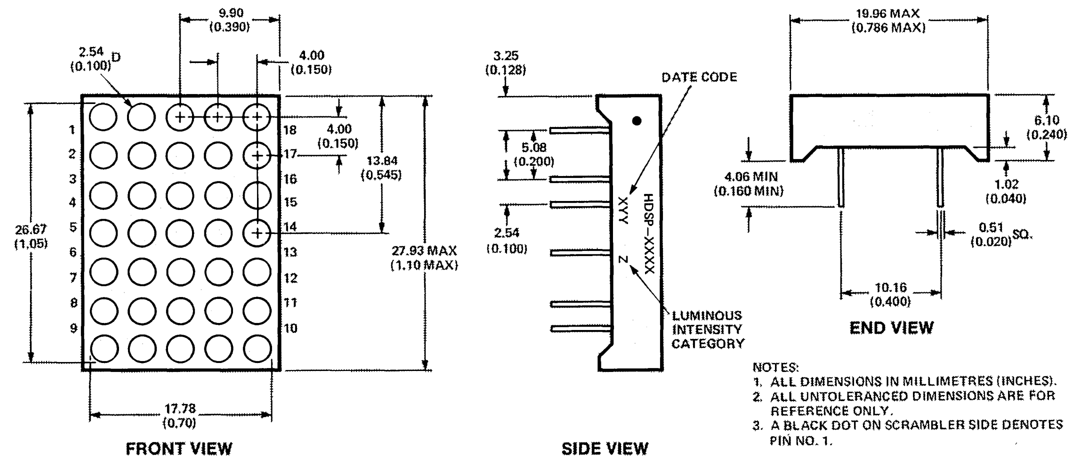
Applications include electronic instrumentation, computer peripherals, point of sale terminals, weighing scales, and industrial electronics.

Devices

Part Number	Color	Description
HDSP-4501 HDSP-4503	High Efficiency Red	Common Anode Row Common Cathode Row

SOLID STATE DISPLAYS

Package Dimensions

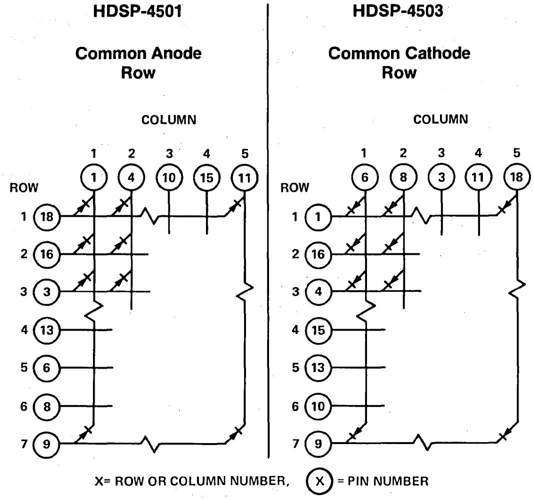


NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. A BLACK DOT ON SCRAMBLER SIDE DENOTES PIN NO. 1.

Pin Function

PIN	HDSP-4501	HDSP-4503
1	COLUMN 1 CATHODE	ROW 1 CATHODE
2	NO PIN	NO PIN
3	ROW 3 ANODE	COLUMN 3 ANODE
4	COLUMN 2 CATHODE	ROW 3 CATHODE
5	NO PIN	NO PIN
6	ROW 5 ANODE	COLUMN 1 ANODE
7	NO PIN	NO PIN
8	ROW 6 ANODE	COLUMN 2 ANODE
9	ROW 7 ANODE	ROW 7 CATHODE
10	COLUMN 3 CATHODE	ROW 6 CATHODE
11	COLUMN 5 CATHODE	COLUMN 4 ANODE
12	NO PIN	NO PIN
13	ROW 4 ANODE	ROW 5 CATHODE
14	NO PIN	NO PIN
15	COLUMN 4 CATHODE	ROW 4 CATHODE
16	ROW 2 ANODE	ROW 2 CATHODE
17	NO PIN	NO PIN
18	ROW 1 ANODE	COLUMN 5 ANODE

Internal Circuit Diagram



Absolute Maximum Ratings (All Products)

Average Power per Segment
($T_A = 25°C$)[1] .... 60 mW

Peak Forward Current per Segment
($T_A = 25°C$)[2] .... 90 mA

Average Forward Current per Segment
($T_A = 25°C$)[3] .... 15 mA

Operating Temperature Range .... −40° C to +85° C

Storage Temperature Range .... −40° C to +85° C

Reverse Voltage per Segment .... 3.0 V

Lead Solder Temperature
(1.59 mm [1/16 inch] below
seating plane) .... 260° C for 3 sec.

NOTES:
1. Average power/segment based on 20 segments 'on' per character. Total package power dissipation should not exceed 1.2 W.
2. Do not exceed maximum average current per segment.
3. Derate maximum average current above $T_A = 55°C$ at 0.25 mA/° C per segment. This derating is based on a device mounted in a socket having a thermal resistance for pin to ambient of 615° C/W per segment.

Electrical/Optical Characteristics at $T_A = 25°C$

HIGH EFFICIENCY RED HDSP-4500 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[4] (Digit Average)	I_V	50 mA Pk: 1 of 5 Duty Factor (10 mA Avg.)	1400	3500		µcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[5]	λ_D			626		nm
Forward Voltage/Segment	V_F	$I_F = 20$ mA		2.1	2.5	V
Reverse Voltage/Segment or DP[6]	V_R	$I_R = 100$ µA	3.0	25.0		V
Temperature Coefficient of V_F/Segment	$\Delta V_F/°C$			−2.0		mV/° C
Thermal Resistance LED Junction-to-Pin per Segment	$R\theta_{J-PIN}$			380		° C/W/ Seg

NOTES:
4. The displays are categorized for luminous intensity with the intensity category designated by a letter on the right hand side of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual segment intensities.
5. The dominant wavelength is derived from the C.I.E. Chromaticity diagram and is that single wavelength which defines the color of the device.
6. Typical specification for reference only. Do not exceed absolute maximum ratings.

HEWLETT PACKARD

LOW CURRENT SEVEN SEGMENT DISPLAYS

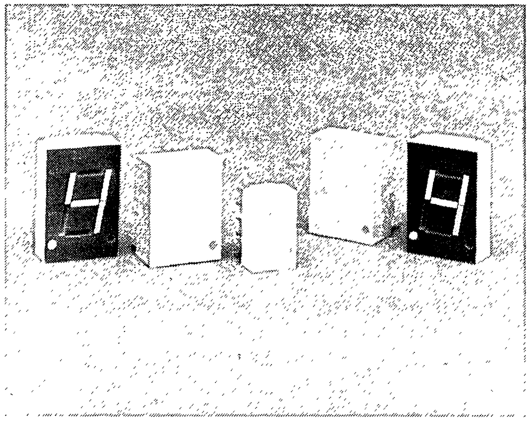
HIGH EFFICIENCY RED

7.6 mm (0.3 in) HDSP-7510 SERIES
10.9 mm (0.43 in) HDSP-3350 SERIES
14.2 mm (0.56 in) HDSP-5550 SERIES

TECHNICAL DATA JANUARY 1986

Features

- **LOW POWER CONSUMPTION**
  Typical Power Consumption is 3 mW/Seg at 2 mA Drive
- **TYPICAL INTENSITY OF 300 μcd/Seg AT 2 mA DRIVE**
- **CAPABLE OF HIGH CURRENT DRIVE**
  Excellent for Long Digit String Multiplexing
- **COMPATIBLE WITH MONOLITHIC LED DISPLAY DRIVERS**
- **THREE CHARACTER SIZES**
  7.6 mm (0.3 in), 10.9 mm (0.43 in), 14.2 mm (0.56 in)
- **COMMON ANODE OR COMMON CATHODE**
  Right Hand Decimal Point
  Overflow ± Character
- **EXCELLENT CHARACTER APPEARANCE**
  Wide Viewing Angle
  Grey Body for Optimum Contrast
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Use of Like Categories Yields a Uniform Display



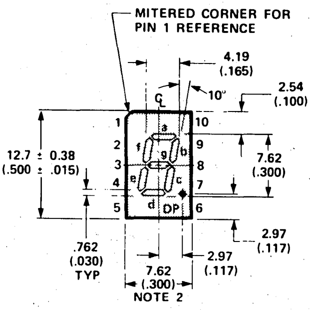
Description

The HDSP-7510, HDSP-3350, HDSP-5550 series are 7.6 mm (0.3 in), 10.9 mm (0.43 in) and 14.2 mm (0.56 in) high efficiency red displays featuring low power consumption. The HDSP-7510 series are designed for viewing distances up to 2 meters, the HDSP-3350 series for viewing distances up to 5 meters, and the HDSP-5550 series for viewing distances up to 7 meters. Typical applications include instruments, scales, point-of-sale terminals and meters.

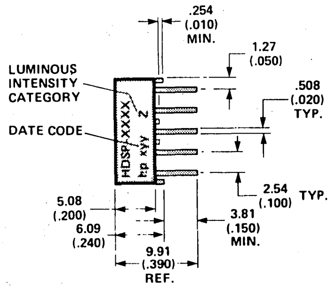
Devices

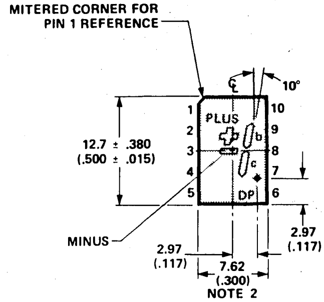
Part Number	Color	Description	Package Drawing
HDSP-7511 HDSP-7513 HDSP-7517 HDSP-7518	High Efficiency Red	7.6 mm Common Anode Right Hand Decimal 7.6 mm Common Cathode Right Hand Decimal 7.6 mm Overflow ±1 Common Anode 7.6 mm Overflow ±1 Common Cathode	A B C D
HDSP-3350 HDSP-3351 HDSP-3353 HDSP-3356	High Efficiency Red	10.9 mm Common Anode Left Hand Decimal 10.9 mm Common Anode Right Hand Decimal 10.9 mm Common Cathode Right Hand Decimal 10.9 mm Universal Overflow ±1 Right Hand Dec.	E F G H
HDSP-5551 HDSP-5553 HDSP-5557 HDSP-5558	High Efficiency Red	14.2 mm Common Anode Right Hand Decimal 14.2 mm Common Cathode Right Hand Decimal 14.2 mm Overflow ±1 Common Anode 14.2 mm Overflow ±1 Common Cathode	I J K L

Package Dimensions (HDSP-7510 Series)

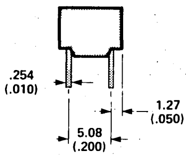


A, B





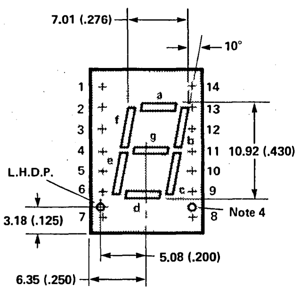
C, D



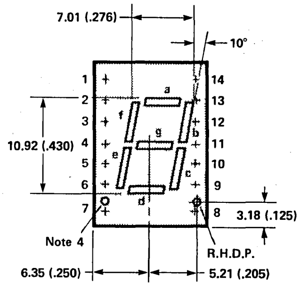
Notes:
1. All dimensions in millimetres (inches).
2. Maximum.
3. All untoleranced dimensions are for reference only.
4. Redundant anodes.
5. Redundant cathodes.

PIN	FUNCTION			
	A	B	C	D
1	ANODE [4]	CATHODE [5]	ANODE [4]	CATHODE [5]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE [4]	CATHODE [5]	ANODE [4]	CATHODE [5]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC

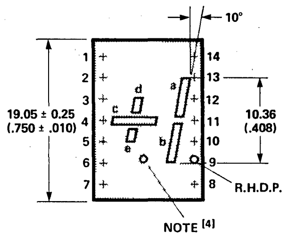
Package Dimensions (HDSP-3350 Series)



E

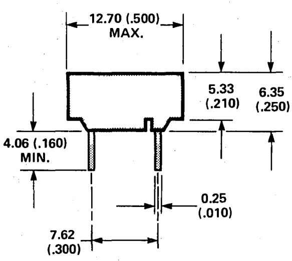


F,H

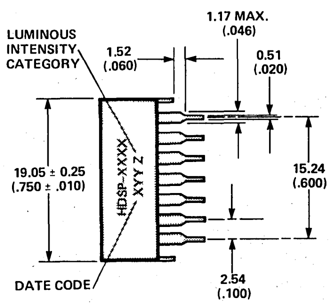


G

FRONT VIEW



END VIEW

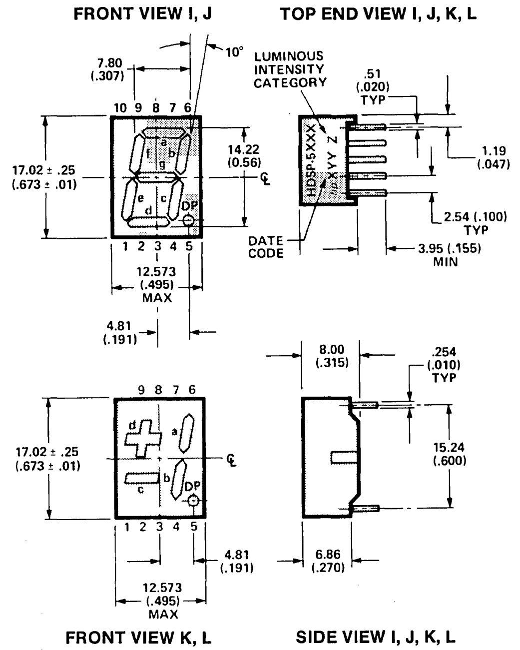


SIDE VIEW

PIN	FUNCTION			
	E	F	G	H
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE [3]	ANODE [3]	CATHODE [6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN. [5]	NO CONN. [5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN. [5]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE [3]	ANODE [3]	CATHODE [6]	ANODE-b

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.
7. See part number table for L.H.D.P. and R.H.D.P. designation.

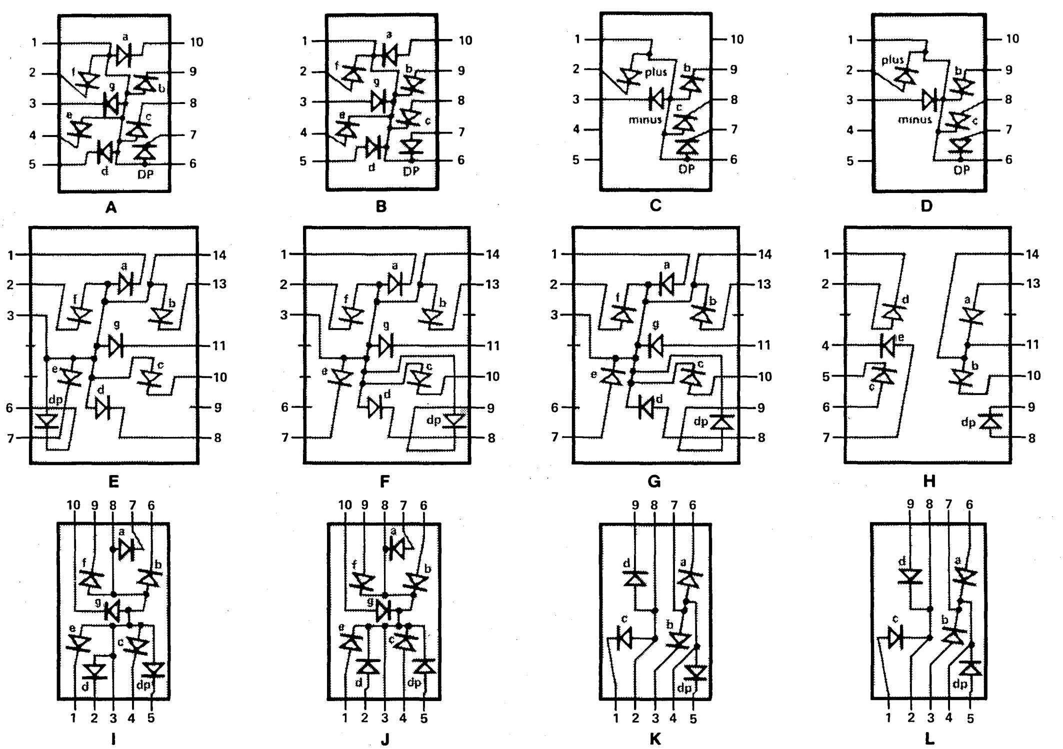
Package Dimensions (HDSP-5550 Series)



PIN	FUNCTION I	J	K	L
1	CATHODE e	ANODE e	CATHODE c	ANODE c
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d
3	ANODE[4]	CATHODE[5]	CATHODE b	ANODE b
4	CATHODE c	ANODE c	ANODE a, b, DP	CATHODE a, b, DP
5	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
6	CATHODE b	ANODE b	CATHODE a	ANODE a
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP
8	ANODE[4]	CATHODE[5]	ANODE c, d	CATHODE c, d
9	CATHODE f	ANODE f	CATHODE d	ANODE d
10	CATHODE g	ANODE g	NO PIN	NO PIN

Notes:
1. All dimensions in millimetres (inches).
2. Maximum.
3. All untoleranced dimensions are for reference only.
4. Redundant anodes.
5. Redundant cathodes.

Internal Circuit Diagram



SOLID STATE DISPLAYS

Absolute Maximum Ratings (All Products)

Average Power per Segment or DP (T_A = 25° C)	52 mW
Peak Forward Current per Segment or DP (T_A = 25° C)[1]	45 mA
Average or DC Forward Current per Segment[2] or DP (T_A == 25° C)	15 mA
Operating Temperature Range	−40° C to +85° C
Storage Temperature Range	−55° C to +100° C
Reverse Voltage per Segment or DP	3.0 V
Lead Solder Temperature (1.59 mm [1/16 inch] below seating plane)	260° C for 3 sec.

Notes:
1. Do not exceed maximum average current per segment.
2. Derate maximum average current above T_A = 65° C at 0.4 mA/° C per segment, see Figure 1. Derate maximum DC current above T_A = 78° C at 0.6 mA/° C per segment.

Electrical/Optical Characteristics at T_A = 25° C

HIGH EFFICIENCY RED HDSP-7510 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[3] (Digit Average)	I_V	2 mA DC	160	270		μcd
		5 mA DC		1050		
		40 mA Pk: 1 of 4 Duty Factor		3500		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[4]	λ_d			626		nm
Forward Voltage/Segment or DP	V_F	I_F = 2 mA		1.6		V
		I_F = 5 mA		1.7		
		I_F = 20 mA Pk		2.1	2.5	
Reverse Voltage/Segment or DP[5]	V_R	I_R = 100 μA	3.0	30.0		V
Temperature Coefficient of V_F/Segment or DP	ΔV_F/° C			−2.0		mV/° C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			200		° C/W/ Seg

HIGH EFFICIENCY RED HDSP-3350 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[3] (Digit Average)	I_V	2 mA DC	200	300		μcd
		5 mA DC		1200		
		40 mA Pk: 1 of 4 Duty Factor		3900		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[4]	λ_d			626		nm
Forward Voltage/Segment or DP	V_F	I_F = 2 mA		1.6		V
		I_F = 5 mA		1.7		
		I_F = 20 mA Pk		2.1	2.5	
Reverse Voltage/Segment or DP[5]	V_R	I_R = 100 μA	3.0	30.0		V
Temperature Coefficient of V_F/Segment or DP	ΔV_F/° C			−2.0		mV/° C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			282		° C/W/ Seg

HIGH EFFICIENCY RED HDSP-5550 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[3] (Digit Average)	I_V	2 mA DC	270	370		μcd
		10 mA DC		3400		
		40 mA Pk: 1 of 4 Duty Factor		4800		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[4]	λ_d			626		nm
Forward Voltage/Segment or DP	V_F	$I_F = 2$ mA		1.6		V
		$I_F = 5$ mA		1.7		
		$I_F = 20$ mA Pk		2.1	2.5	
Reverse Voltage/Segment or DP[5]	V_R	$I_R = 100\ \mu A$	3.0	30.0		V
Temperature Coefficient of V_F/Segment or DP	$\Delta V_F/°C$			−2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			345		°C/W/ Seg

3. The digits are categorized for luminous intensity with the intensity category designated by a letter on the right hand side of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual segment intensities, decimal point not included. Operation at less than 2 mA DC or peak current per segment may cause objectionable display segment matching and is not recommended.
4. The dominant wavelength is derived from the C.I.E. Chromaticity diagram and is that single wavelength which defines the color of the device.
5. Typical specification for reference only. Do not exceed absolute maximum ratings.

HDSP-7510/-3350/-5550 SERIES

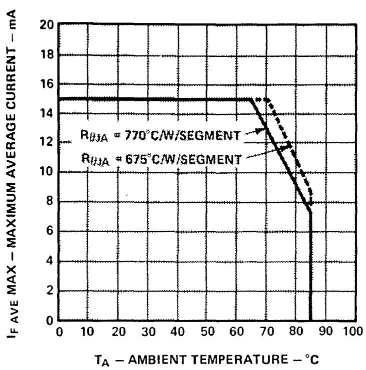


Figure 1. Maximum Allowable Average Current per Segment as a Function of Ambient Temperature

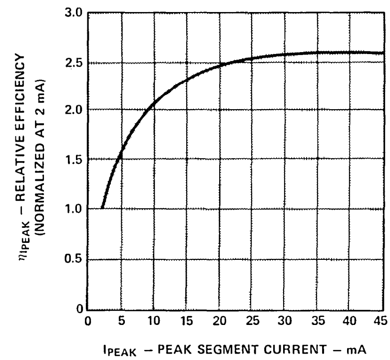


Figure 2. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current per Segment

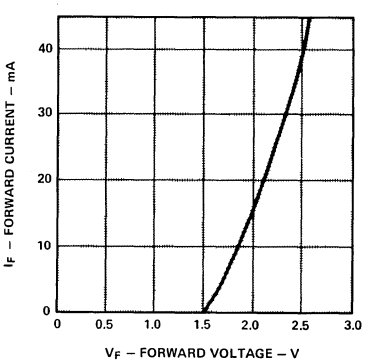


Figure 3. Forward Current vs. Forward Voltage

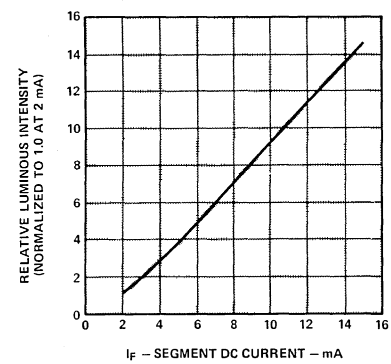


Figure 4. Relative Luminous Intensity vs. DC Forward Current

Electrical

THe HDSP-7510/-3350/-5550 series of display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. These displays have their p-n junctions diffused into GaAsP epitaxial layer on a GaP substrate.

These display devices are well suited for strobed operation. The typical forward voltage values, scaled from Figure 3, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX model:

V_F MAX = 1.75 V + I_{PEAK} (38Ω)
For: $I_{PEAK} \geq 20$ mA
V_F MAX = 1.6 V + I_{DC} (45Ω)
For: 2 mA $\leq I_{DC} \leq$ 20 mA

These displays are compatible with monolithic LED display drivers. See Application Note 1006 for more information.

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance readability by having the OFF-segments blend into the display background and the ON-segments stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the segments.

Contrast enhancement may be achieved by using one of the following suggested filters:

Panelgraphic SCARLET RED 65 or GRAY 10
SGL Homalite H100-1670 RED or -1266 GRAY
3M Louvered Filter R6310 RED or N0210 GRAY

Mechanical

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolve DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Such cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the packages of plastic LED devices.

HEWLETT PACKARD

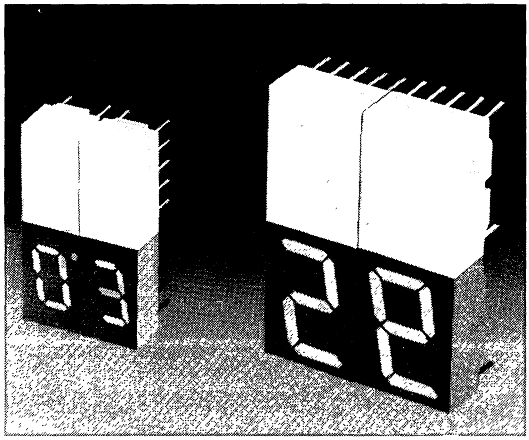
EMERALD GREEN SEVEN SEGMENT DISPLAYS

7.6 mm (0.30 in) HDSP-7900 SERIES
14.2 mm (0.56 in) HDSP-5900 SERIES

TECHNICAL DATA JANUARY 1986

Features

- TRUE GREEN COLOR
- TYPICAL DOMINANT WAVELENGTH OF 557 nm
- AVAILABLE IN TWO SIZES
- INDUSTRY STANDARD PINOUTS
- CATEGORIZED FOR LUMINOUS INTENSITY AND COLOR
- EXCELLENT CHARACTER APPEARANCE
  Mitered Segments
  Wide Viewing Angle
  Grey Body for Optimum Contrast
- COMMON ANODE OR COMMON CATHODE
  Right Hand Decimal Point
  Overflow ± Character



Description

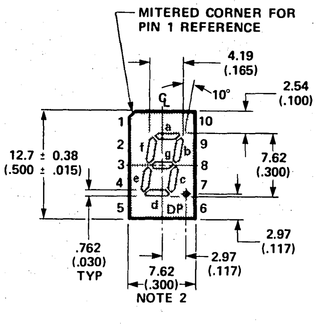
The HDSP-7900 and HDSP-5900 series are 7.6 mm (0.30 in) and 14.2 mm (0.56 in) emerald green displays. Emerald green displays feature a shorter wavelength, true green color. The HDSP-7900 series are designed for viewing distances up to 3 meters and the HDSP-5900 series are designed for viewing distances up to 7 meters. Typical applications include instruments, scales, point of sale terminals, and meters.

SOLID STATE DISPLAYS

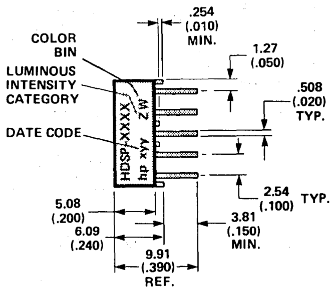
Devices

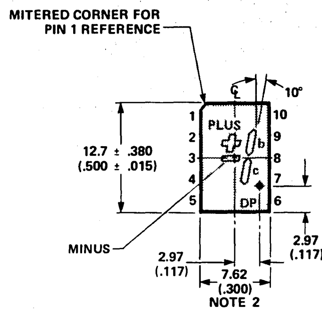
Part Number	Color	Description	Package Drawing
HDSP-7901	Emerald	7.6 mm Common Anode Right Hand Decimal	A
HDSP-7903	Green	7.6 mm Common Cathode Right Hand Decimal	B
HDSP-7907		7.6 mm Overflow ±1 Common Anode	C
HDSP-7908		7.6 mm Overflow ±1 Common Cathode	D
HDSP-5901	Emerald	14.2 mm Common Anode Right Hand Decimal	E
HDSP-5903	Green	14.2 mm Common Cathode Right Hand Decimal	F
HDSP-5907		14.2 mm Overflow ±1 Common Anode	G
HDSP-5908		14.2 mm Overflow ±1 Common Cathode	H

Package Dimensions (HDSP-7900 Series)

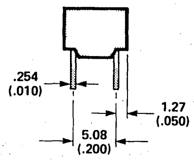


A, B





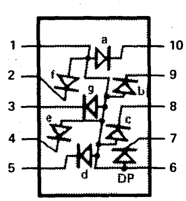
C, D



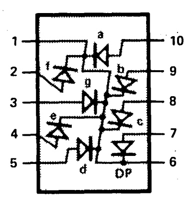
Notes:
1. All dimensions in millimetres (inches).
2. Maximum.
3. All untoleranced dimensions are for reference only.
4. Redundant anodes.
5. Redundant cathodes.

PIN	FUNCTION A	B	C	D
1	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC

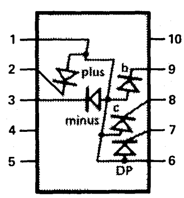
Internal Circuit Diagram



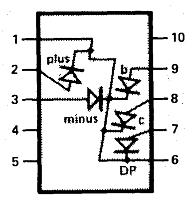
A



B

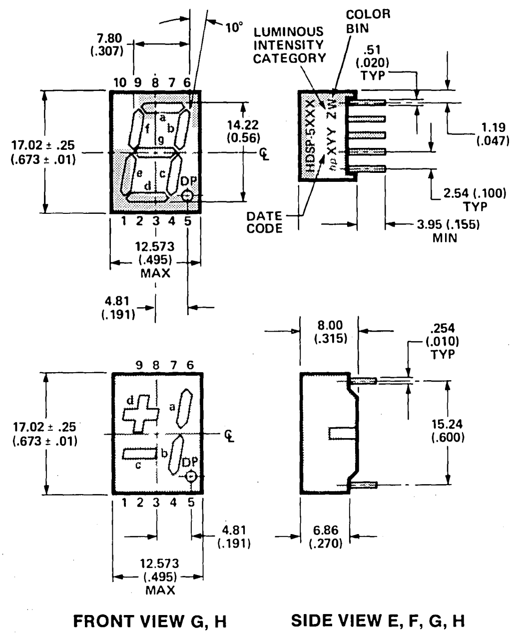


C



D

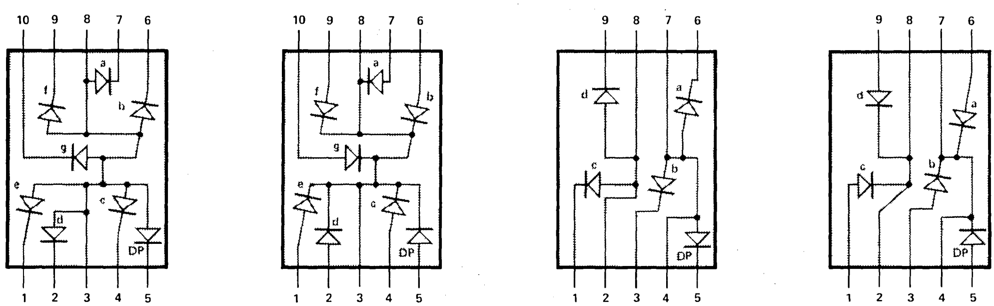
Package Dimensions (HDSP-5900 Series)



PIN	FUNCTION E	F	G	H
1	CATHODE e	ANODE e	CATHODE c	ANODE c
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d
3	ANODE[4]	CATHODE[5]	CATHODE b	ANODE b
4	CATHODE c	ANODE c	ANODE a, b, DP	CATHODE a, b, DP
5	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
6	CATHODE b	ANODE b	CATHODE a	ANODE a
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP
8	ANODE[4]	CATHODE[5]	ANODE c, d	CATHODE c, d
9	CATHODE f	ANODE f	CATHODE d	ANODE d
10	CATHODE g	ANODE g	NO PIN	NO PIN

Notes:
1. All dimensions in millimetres (inches).
2. Maximum.
3. All untoleranced dimensions are for reference only.
4. Redundant anodes.
5. Redundant cathodes.

Internal Circuit Diagram



E F G H

Absolute Maximum Ratings (All Products)

Average Power per Segment or DP ($T_A = 25°C$) .... 105 mW

Peak Forward Current per Segment or DP ($T_A = 25°C$)[1] .... 90 mA

Average or DC Forward Current per Segment[2] or DP ($T_A = 25°C$) .... 30 mA

Operating Temperature Range .... −20° C to +85° C

Storage Temperature Range .... −55° C to +100° C

Reverse Voltage per Segment or DP .... 3.0 V

Lead Solder Temperature (1.59 mm [1/16 inch] below seating plane) .... 260° C for 3 sec.

NOTES:

1. Do not exceed maximum average current per segment.
2. Derate maximum average current above $T_A = 25°C$ at 0.38 mA/° C per segment, see Figure 1.

Electrical/Optical Characteristics at $T_A = 25°C$

EMERALD GREEN HDSP–7900 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[3] (Digit Average)	I_V	10 mA DC	220	590		μcd
		20 mA DC		1475		
		60 mA Pk: 1 of 6		750		
Peak Wavelength	λ_{PEAK}			555		nm
Dominant Wavelength[4]	λ_d			557	565	nm
Forward Voltage/Segment or DP	V_F	$I_F = 10$ mA		2.1	2.5	V
Reverse Voltage/Segment or DP[5]	V_R	$I_F = 100\mu A$	3.0	30.0		V
Temperature Coefficient of V_F/Segment or DP	$\Delta V_F/°C$			-2.0		mV/° C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			200		° C/W/ Seg

EMERALD GREEN HDSP–5900 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[3] (Digit Average)	I_V	10 mA DC	270	620		μcd
		20 mA DC		1550		
		60 mA Pk: 1 of 6		800		
Peak Wavelength	λ_{PEAK}			555		nm
Dominant Wavelength[4]	λ_d			557	565	nm
Forward Voltage/Segment or DP	V_F	$I_F = 10$ mA		2.1	2.5	V
Reverse Voltage/Segment or DP[5]	V_R	$I_F = 100\mu A$	3.0	30.0		V
Temperature Coefficient of V_F/Segment or DP	$\Delta V_F/°C$			-2.0		mV/° C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			345		° C/W/ Seg

3. The digits are categorized for luminous intensity with the intensity category designated by a letter on the right hand side of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual segment intensities, decimal point not included.
4. The dominant wavelength is derived from the C.I.E. Chromaticity diagram and is that single wavelength which defines the color of the device. These displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
5. Typical specification for reference only. Do not exceed absolute maximum ratings.

HDSP-7900/-5900 SERIES

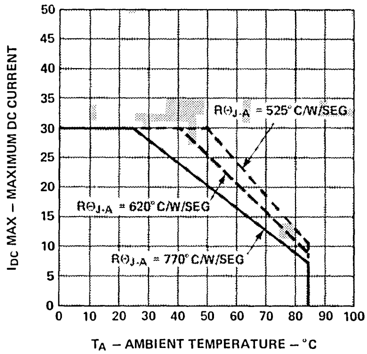


Figure 1. Maximum Allowable Average Current per Segment as a Function of Ambient Temperature

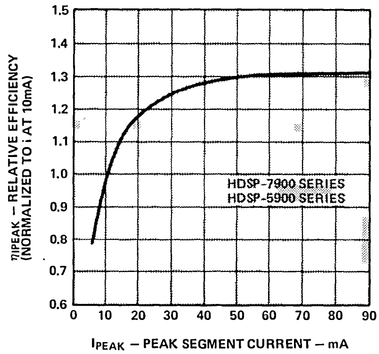


Figure 2. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current per Segment

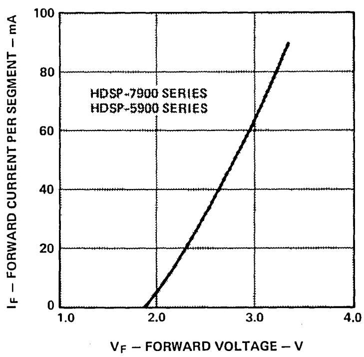


Figure 3. Forward Current vs. Forward Voltage

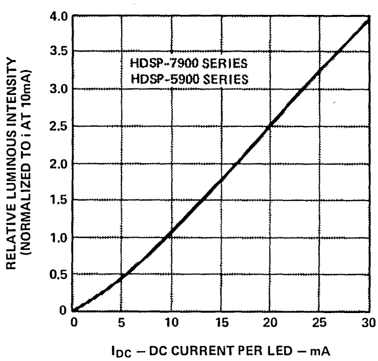


Figure 4. Relative Luminous Intensity vs. DC Forward Current

Electrical

The HDSP-7900/5900 series of display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The -7900 and -5900 series have their p-n junctions diffused into a GaP epitaxial layer on a GaP substrate.

These display devices are well suited for strobed operation. The typical forward voltage values, scaled from Figure 3, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX model:

V_F MAX = 2.0 V + I_{PEAK} (50Ω)
For: $I_{PEAK} \geq$ 5mA

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance readability by having the OFF-segments blend into the display background and the ON-segments stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the segments.

Contrast enhancement may be achieved by using one of the following suggested filters:

Panelgraphic GREEN 48
SGL Homalite H100-1440 GREEN
3M Louvered Filter G5610 GREEN or N0210 GRAY

Mechanical

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolve DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Such cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the packages of plastic LED devices.

See Applicaton Note 1027 for additional information on soldering and cleaning LED displays.

HEWLETT PACKARD

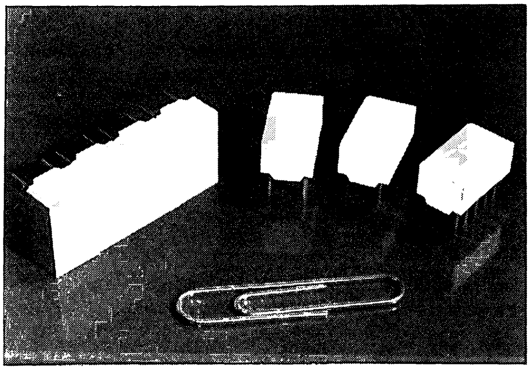
7.6 mm (.3 inch) MICRO BRIGHT 7 SEGMENT DISPLAYS

RED HDSP-7300
HIGH EFFICIENCY RED HDSP-7500
YELLOW HDSP-7400
HIGH PERFORMANCE GREEN HDSP-7800

TECHNICAL DATA JANUARY 1986

Features

- **HIGH BRIGHTNESS**
  Package Optimized for High Ambient Conditions
- **COMPACT PACKAGE**
  0.300 x 0.500 inches
- **CHOICE OF FOUR COLORS:**
  Red, High Efficiency Red, Yellow, High Performance Green
- **EXCELLENT CHARACTER APPEARANCE:**
  Evenly Lighted Segments
  Mitered Segments
  Wide Viewing Angle
  Grey Package Provides Optimum On-Off Contrast
- **EASY MOUNTING ON PC BOARDS OR SOCKETS**
  5.08 mm (0.2 inch) DIP Leads on 2.54 mm (0.1 inch) Centers
- **AVAILABLE WITH COLON FOR CLOCK DISPLAY**
- **COMMON ANODE OR COMMON CATHODE**
  Right Hand Decimal Point
  Overflow ± Character
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW AND GREEN ALSO CATEGORIZED FOR COLOR**
  Use of Like Category Yields a Uniform Display



Description

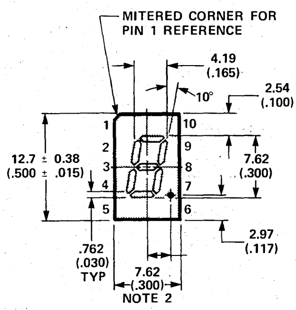
The HDSP-7300/-7500/-7400/-7800 Series are 7.6 mm (0.3 inch) character LED seven segment displays in a compact package. Designed for viewing distances up to 3 metres (10 feet), these displays are ideal for high ambient applications where space is at a premium. Typical applications include instruments, aircraft and marine equipment, point-of-sale terminals, clocks, and appliances.

Devices

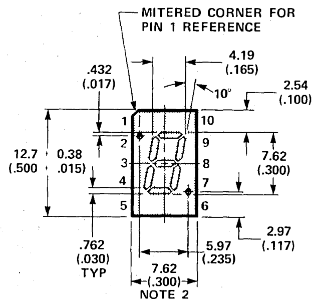
Part Number	Color	Description	Package Drawing
HDSP-7301	Red	Common Anode Right Hand Decimal	A
HDSP-7311	Bright Red	Common Anode Right Hand Decimal	A
HDSP-7302	Red	Common Anode Right Hand Decimal, Colon	B
HDSP-7303	Red	Common Cathode Right Hand Decimal	C
HDSP-7313	Bright Red	Common Cathode Right Hand Decimal	C
HDSP-7304	Red	Common Cathode Right Hand Decimal, Colon	D
HDSP-7307	Red	Overflow ±1 Common Anode	E
HDSP-7317	Bright Red	Overflow ±1 Common Anode	E
HDSP-7308	Red	Overflow ±1 Common Cathode	F
HDSP-7318	Bright Red	Overflow ±1 Common Cathode	F
HDSP-7501	HER	Common Anode Right Hand Decimal	A
HDSP-7502		Common Anode Right Hand Decimal, Colon	B
HDSP-7503		Common Cathode Right Hand Decimal	C
HDSP-7504		Common Cathode Right Hand Decimal, Colon	D
HDSP-7507		Overflow ±1 Common Anode	E
HDSP-7508		Overflow ±1 Common Cathode	F
HDSP-7401	Yellow	Common Anode Right Hand Decimal	A
HDSP-7402		Common Anode Right Hand Decimal, Colon	B
HDSP-7403		Common Cathode Right Hand Decimal	C
HDSP-7404		Common Cathode Right Hand Decimal, Colon	D
HDSP-7407		Overflow ±1 Common Anode	E
HDSP-7408		Overflow ±1 Common Cathode	F
HDSP-7801	Green	Common Anode Right Hand Decimal	A
HDSP-7802		Common Anode Right Hand Decimal, Colon	B
HDSP-7803		Common Cathode Right Hand Decimal	C
HDSP-7804		Common Cathode Right Hand Decimal, Colon	D
HDSP-7807		Overflow ±1 Common Anode	E
HDSP-7808		Overflow ±1 Common Cathode	F

SOLID STATE DISPLAYS

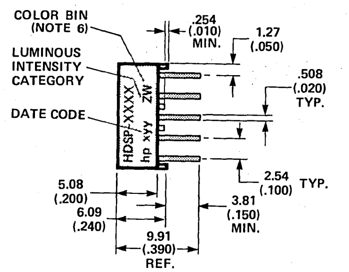
Package Dimensions

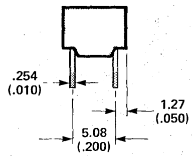


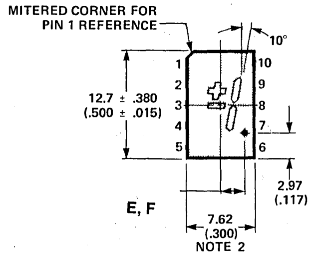
A, C



B, D





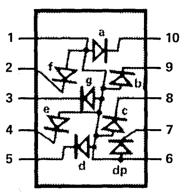


E, F

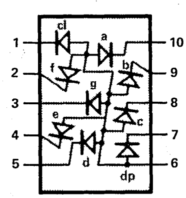
Notes:
1. All dimensions in millimetres (inches).
2. Maximum.
3. All untoleranced dimensions are for reference only.
4. Redundant anodes.
5. Redundant cathodes.
6. For HDSP-7400/-7800 series product only.

PIN	FUNCTION A	B	C	D	E	F
1	ANODE[4]	CATHODE COLON	CATHODE[5]	ANODE COLON	ANODE[4]	CATHODE[5]
2	CATHODE f	CATHODE f	ANODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	CATHODE g	ANODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	CATHODE e	ANODE e	ANODE e	NC	NC
5	CATHODE d	CATHODE d	ANODE d	ANODE d	NC	NC
6	ANODE[4]	ANODE	CATHODE[5]	CATHODE	ANODE[4]	CATHODE[5]
7	CATHODE DP	CATHODE DP	ANODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	CATHODE c	ANODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	CATHODE b	ANODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	CATHODE a	ANODE a	ANODE a	NC	NC

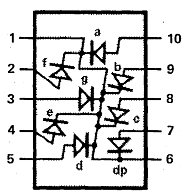
Internal Circuit Diagram



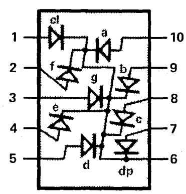
A



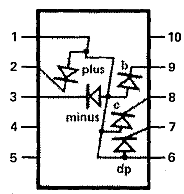
B



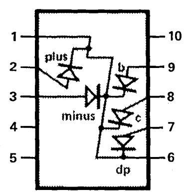
C



D



E



F

Absolute Maximum Ratings

	HDSP-7300/ -7310 Series	HDSP-7500 Series	HDSP-7400 Series	HDSP-7800 Series
Average Power Dissipation per Segment or D.P.	73 mW	105 mW	81 mW	105 mW
Operating Temperature Range[7]	-40°C to +85°C			-20°C to +85°C
Storage Temperature Range	-55°C to +100°C			
Peak Forward Current per Segment or D.P.[8]	150 mA	90 mA	60 mA	90 mA
DC Forward Current per Segment or D.P.[9]	25 mA	30 mA	20 mA	30 mA
Reverse Voltage per Segment or D.P.	3 V	3 V	3 V	3 V
Lead Soldering Temperature 1.59 mm (1/16 inch) below seating plane	260°C for 3 sec.			

7. For operation of HDSP-7800 series to -40°C consult Optoelectronics division.
8. See Figures 1, 6, 7, and 8 to establish pulsed operating conditions. (Figure 1, HDSP-7300 Series; Figure 6, HDSP-7500 Series; Figure 7, HDSP-7400 Series; Figure 8, HDSP-7800 Series)
9. See Figures 2, 9, 10, and 11 to derate maximum DC current. (Figure 2, HDSP-7300 Series; Figure 9, HDSP-7500 Series; Figure 10, HDSP-7400 Series; Figure 11, HDSP-7800 Series)

Electrical/Optical Characteristics at $T_A = 25°C$

STANDARD RED HDSP-7300 SERIES

Description	Device HDSP-	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[10] (Digit Average)	7300	I_V	10 mA DC		500		μcd
			20 mA DC	600	1100		
	7310		10 mA DC		610		
			20 mA DC	770	1355		
Peak Wavelength		λ_{PEAK}			655		nm
Dominant Wavelength[11]		λ_d			640		nm
Forward Voltage, any Segment or D.P.		V_F	$I_F = 20$ mA		1.6	2.0	V
Reverse Voltage, any Segment or D.P.[13]		V_R	$I_R = 100\ \mu A$	3.0	12.0		V
Temperature Coefficient of Forward Voltage		$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$			200		°C/W/ Seg

HIGH EFFICIENCY RED HDSP-7500 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[10] (Digit Average)	I_V	5 mA D.C.	360	980		μcd
		20 mA D.C.		5390		
		60 mA Pk: 1 of 6 Duty Factor		3430		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[11]	λ_d			626		nm
Forward Voltage/Segment or D.P.	V_F	$I_F = 5$ mA		1.7		V
		$I_F = 20$ mA		2.0	2.5	
		$I_F = 60$ mA		2.8		
Reverse Voltage/Segment or D.P.[13]	V_R	$I_R = 100\ \mu A$	3.0	30.0		V
Temperature Coefficient of V_F/Segment or D.P.	$\Delta V_F/°C$			—2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			200		°C/W/ Seg

YELLOW HDSP-7400 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[10] (Digit Average)	I_V	5 mA D.C.	225	480		μcd
		20 mA D.C.		2740		
		60 mA Pk: 1 of 6 Duty Factor		1700		
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[11,12]	λ_d		581.5	586	592.5	nm
Forward Voltage/Segment or D.P.	V_F	$I_F = 5$ mA		1.8		V
		$I_F = 20$ mA		2.2	2.5	
		$I_F = 60$ mA		3.1		
Reverse Voltage/Segment or D.P.[13]	V_R	$I_R = 100\ \mu A$	3.0	50.0		V
Temperature Coefficient of V_F/Segment or D.P.	$\Delta V_F/°C$			—2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			200		°C/W/ Seg

10. The digits are categorized for luminous intensity with the intensity category designated by a letter on the right hand side of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual segment intensities, decimal point not included.
11. The dominant wavelength is derived from the C.I.E. Chromaticity diagram and is that single wavelength which defines the color of the device.
12. The HDSP-7400/-7800 series are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
13. Typical specification for reference only. Do not exceed absolute maximum ratings.

HIGH PERFORMANCE GREEN HDSP-7800 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[9] (Digit Average)	Iv	5 mA D.C.		545		μcd
		10 mA D.C.	570	1480		
		60 mA Pk: 1 of 6 Duty Factor		1935		
Peak Wavelength	λPEAK			566		nm
Dominant Wavelength[10, 11] (Digit Average)	λd			571	577	nm
Forward Voltage/Segment or D.P.	V_F	I_F = 10 mA		2.1	2.5	V
Reverse Voltage/Segment or D.P.[12]	V_R	I_R = 100 μA	3.0	50.0		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			200		°C/W/ Seg

HDSP-7300 SERIES

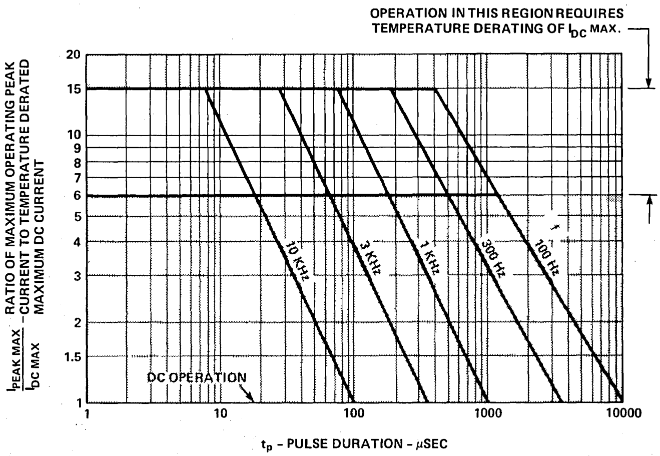


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

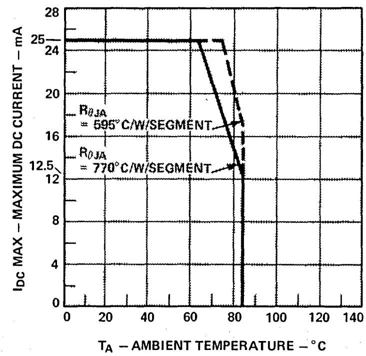


Figure 2. Maximum Allowable DC Current Dissipation per Segment as a Function of Ambient Temperature

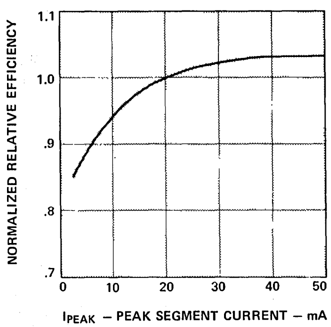


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current per Segment

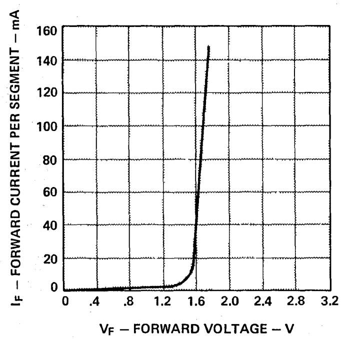


Figure 4. Forward Current vs. Forward Voltage

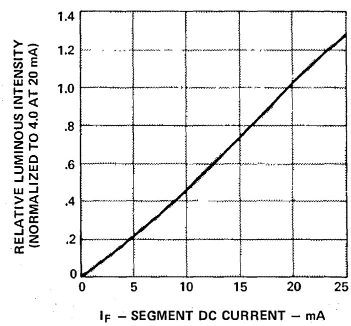


Figure 5. Relative Luminous Intensity vs. DC Forward Current

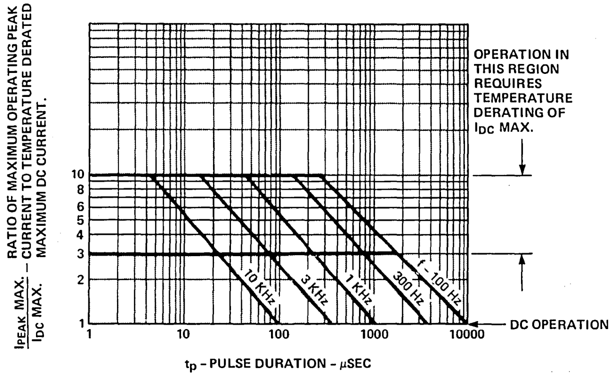


Figure 6. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-7500 Series

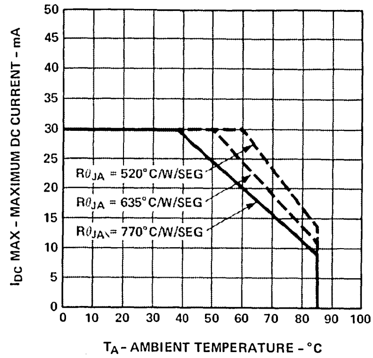


Figure 9. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature — HDSP-7500 Series

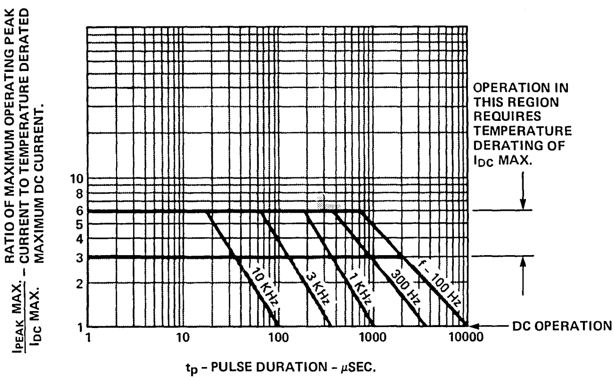


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-7400 Series

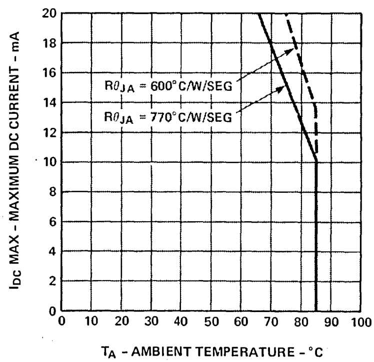


Figure 10. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature — HDSP-7400 Series

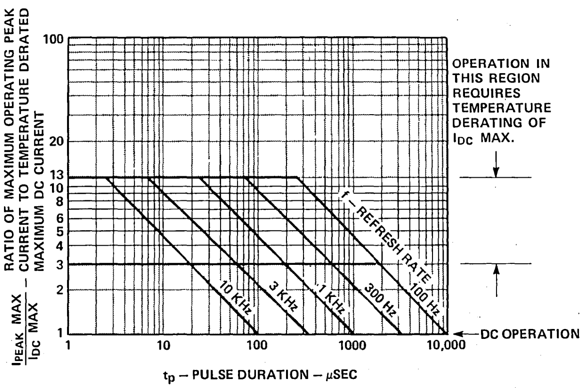


Figure 8. Allowed Peak Current vs. Pulse Duration — HDSP-7800 Series

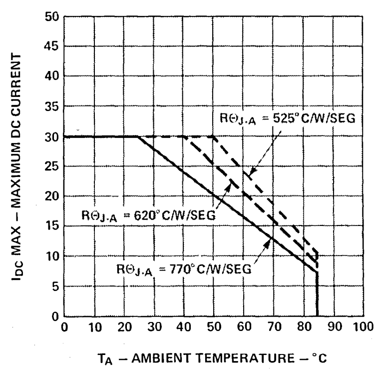


Figure 11. Maximum Allowable DC Current per Segment vs. Ambient Temperature — HDSP-7800 Series

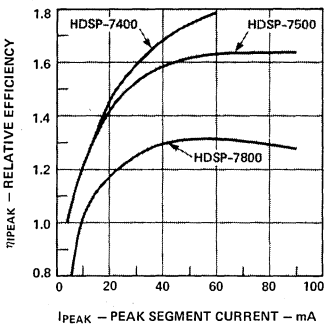


Figure 12. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

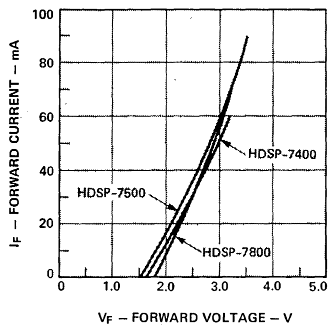


Figure 13. Forward Current vs. Forward Voltage Characteristics

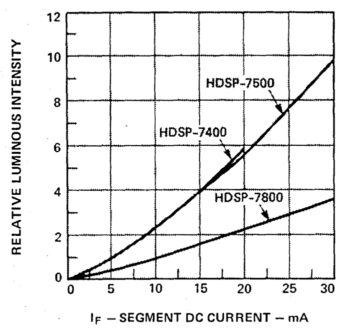


Figure 14. Relative Luminous Intensity vs. DC Forward Current

Electrical

The HDSP-7300/-7400/-7500/-7800 series of display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The -7300 series uses a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The -7400 and-7500 series have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The -7800 series use a GaP epitaxial layer on GaP.

These display devices are well suited for strobed operation. The typical forward voltage values, scaled from Figure 4 or 13, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

HDSP-7300 Series:

V_F MAX = 1.85 V + I_{PEAK} (7Ω)
For: $I_{PEAK} \geq 5$ mA

HDSP-7400/-7500 Series:

V_F MAX = 1.75 V + I_{PEAK} (38Ω)
For: $I_{PEAK} \geq 20$ mA
V_F MAX = 1.6 V + I_{DC} (45Ω)
For: 5 mA $\leq I_{DC} \leq$ 20 mA

HDSP-7800 Series:

V_F MAX = 2.0 V + I_{PEAK} (50Ω)
For: $I_{PEAK} \geq 5$ mA

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance readability by having the OFF-segments blend into the display background and the ON-segments stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the segments.

Contrast enhancement may be achieved by using one of the following suggested filters:

HDSP-7300: Panelgraphic RUBY RED 60
SGL Homalite H100-1605 RED
3M Louvered Filter R6610 RED or N0210 GRAY

HDSP-7400: Panelgraphic YELLOW 27 or GRAY 10
SGL Homalite H100-1720 AMBER or -1266 GRAY
3M Louvered Filter A5910 AMBER or N0210 GRAY

HDSP-7500: Panelgraphic SCARLET RED 65 or GRAY 10
SGL Homalite H100-1670 RED or -1266 GRAY
3M Louvered Filter R6310 RED or N0210 GRAY

HDSP-7800: Panelgraphic GREEN 48
SGL Homalite H100-1440 GREEN
3M Louvered Filter G5610 GREEN or N0210 GRAY

Mechanical

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes. with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolve DI-15 or DE-15, Arklone A or K. A 60° C (140° F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Such cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the packages of plastic LED devices.

HEWLETT PACKARD

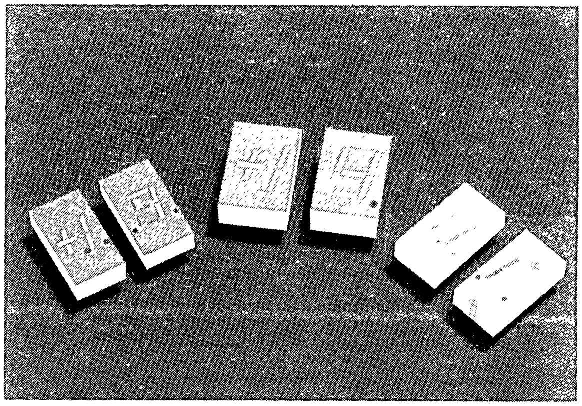
7.6/10.9 mm (0.3/0.43 INCH) SEVEN SEGMENT DISPLAYS

RED • 5082-7730/-7750 SERIES
HIGH EFFICIENCY RED • 5082-7610/-7650 SERIES
YELLOW • 5082-7620/-7660 SERIES
HIGH PERFORMANCE GREEN • HDSP-3600/-4600 SERIES

TECHNICAL DATA JANUARY 1986

Features

- **COMPACT SIZE**
- **CHOICE OF 4 BRIGHT COLORS**
  - **Red**
  - **High Efficiency Red**
  - **Yellow**
  - **High Performance Green**
- **LOW CURRENT OPERATION**
  - **As Low as 3mA per Segment**
  - **Designed for Multiplex Operation**
- **EXCELLENT CHARACTER APPEARANCE**
  - **Evenly Lighted Segments**
  - **Wide Viewing Angle**
  - **Body Color Improves "Off" Segment Contrast**
- **EASY MOUNTING ON PC BOARD OR SOCKETS**
  - **Industry Standard 7.62mm (0.3 in.) DIP Leads on 2.54mm (0.1 in.) Centers**
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW AND GREEN CATEGORIZED FOR COLOR**
  - **Use of Like Categories Yields a Uniform Display**
- **MECHANICALLY RUGGED**



Description

The -7730/-7610/-7620/-3600 and -7750/-7650/-7660/-4600 series are 7.62/10.92 mm (0.3/.43 in.) red, high efficiency red, yellow, and green displays. The -7730/-7610/-7620/-3600 series displays are designed for viewing distances of up to three metres and the -7750/-7650/-7660/-4600 series displays are designed for viewing distances of up to six metres. These displays are designed for use in instruments, point of sale terminals, clocks and appliances.

Devices

Part Number	Color	Description	Package Drawing
5082-7730	Red	7.6 mm Common Anode Left Hand Decimal	A
5082-7731		7.6 mm Common Anode Right Hand Decimal	B
5082-7736		7.6 mm Common Cathode Right Hand Decimal	C
5082-7740		7.6 mm Universal Overflow ±1 Right Hand Decimal	D
5082-7610	High Efficiency Red	7.6 mm Common Anode Left Hand Decimal	A
5082-7611		7.6 mm Common Anode Right Hand Decimal	B
5082-7613		7.6 mm Common Cathode Right Hand Decimal	C
5082-7616		7.6 mm Universal Overflow ±1 Right Hand Decimal	D
5082-7620	Yellow	7.6 mm Common Anode Left Hand Decimal	A
5082-7621		7.6 mm Common Anode Right Hand Decimal	B
5082-7623		7.6 mm Common Cathode Right Hand Decimal	C
5082-7626		7.6 mm Universal Overflow ±1 Right Hand Decimal	D
HDSP-3600	High Performance Green	7.6 mm Common Anode Left Hand Decimal	A
HDSP-3601		7.6 mm Common Anode Right Hand Decimal	B
HDSP-3603		7.6 mm Common Cathode Right Hand Decimal	C
HDSP-3606		7.6 mm Universal Overflow ±1 Right Hand Decimal	D

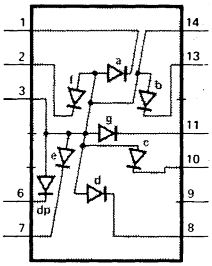
NOTE: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram D.

Devices

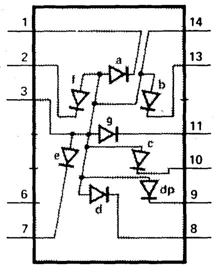
Part Number	Color	Description	Package Drawing
5082-7750 5082-7751 5082-7756 5082-7760	Red	10.9 mm Common Anode Left Hand Decimal 10.9 mm Common Anode Right Hand Decimal 10.9 mm Common Cathode Right Hand Decimal 10.9 mm Universal Overflow ±1 Right Hand Decimal	E F G H
5082-7650 5082-7651 5082-7653 5082-7656	High Efficiency Red	10.9 mm Common Anode Left Hand Decimal 10.9 mm Common Anode Right Hand Decimal 10.9 mm Common Cathode Right Hand Decimal 10.9 mm Universal Overflow ±1 Right Hand Decimal	E F G H
5082-7660 5082-7661 5082-7663 5082-7666	Yellow	10.9 mm Common Anode Left Hand Decimal 10.9 mm Common Anode Right Hand Decimal 10.9 mm Common Cathode Right Hand Decimal 10.9 mm Universal Overflow ±1 Right Hand Decimal	E F G H
HDSP-4600 HDSP-4601 HDSP-4603 HDSP-4606	High Performance Green	10.9 mm Common Anode Left Hand Decimal 10.9 mm Common Anode Right Hand Decimal 10.9 mm Common Cathode Right Hand Decimal 10.9 mm Universal Overflow ±1 Right Hand Decimal	E F G H

NOTE: Universal pinout brings the anode and the cathode of each segment's LED out to separate pins, see internal diagram H.

Internal Circuit Diagram



A



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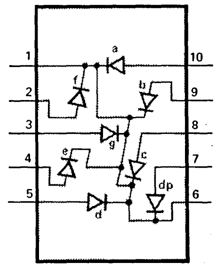

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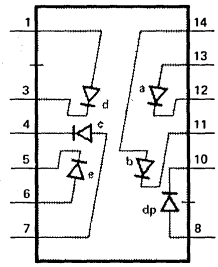

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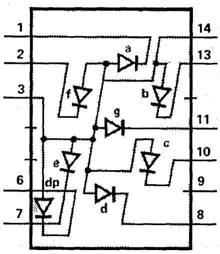
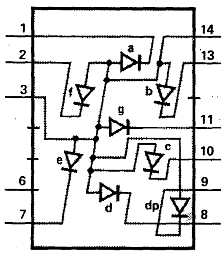


E



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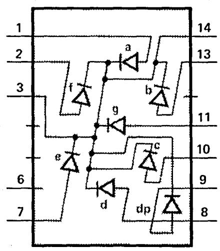

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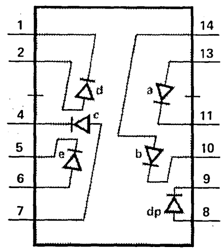


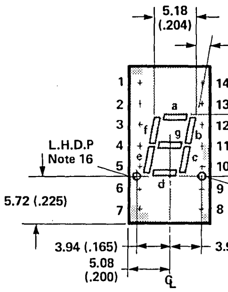
H

Absolute Maximum Ratings

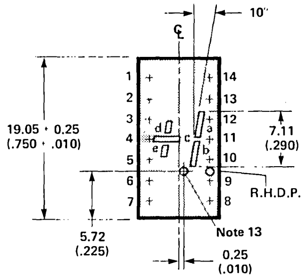
	-7730/-7750 Series	-7610/-7650 Series	-7620/-7660 Series	-3600/-4600 Series
Average Power Dissipation per Segment or DP	65 mW[1]	105 mW[2]	81 mW[3]	105 mW[4]
Operating Temperature Range	−40° C to +85° C	−40° C to +85° C	−40° C to +85° C	−20° C to +85° C[5]
Storage Temperature	−55° C to +100° C	−55° C to +100° C	−55° C to +100° C	−55° C to +100° C
Peak Forward Current per Segment or DP	150 mA[6]	90 mA[7]	60 mA[8]	90 mA[9]
DC Forward Current per Segment of DP	25 mA[1]	30 mA[2]	20 mA[3]	30 mA[4]
Reverse Voltage per Segment or DP	3.0 V	3.0 V	3.0 V	3.0 V
Lead Soldering Temperature 1.59 mm (1/16 in.) below seating plane	260° C for 3 sec.	260° C for 3 sec.	260° C for 3 sec.	260° C for 3 sec.

Notes:
1. See power derating curve (Figure 5).
2. See power derating curve (Figure 6).
3. See power derating curve (Figure 7).
4. See power derating curve (Figure 8).
5. For operation to −40° C consult optoelectronics division.
6. See Figure 1 to establish pulsed operating conditions.
7. See Figure 2 to establish pulsed operating conditions.
8. See Figure 3 to establish pulsed operating conditions.
9. See Figure 4 to establish pulsed operating conditions.

Package Dimensions (5082-7730/-7610/-7620/-3600)

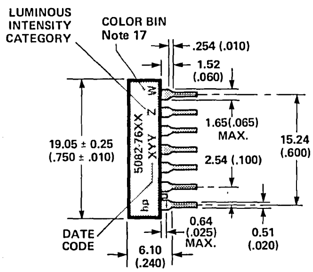


A,B,C

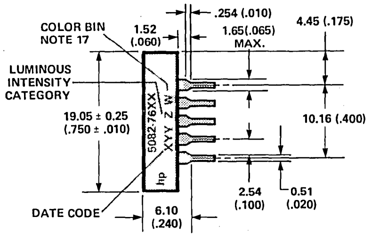


D

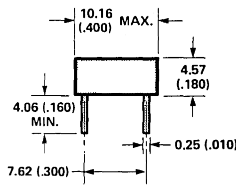
PIN	FUNCTION A	B	C	D
1	CATHODE - a	CATHODE - a	NO PIN	ANODE - d
2	CATHODE - f	CATHODE - f	CATHODE[15]	NO PIN
3	ANODE[12]	ANODE[12]	ANODE - f	CATHODE - d
4	NO PIN	NO PIN	ANODE - g	CATHODE - c
5	NO PIN	NO PIN	ANODE - e	CATHODE - e
6	CATHODE - dp	NO CONN.[14]	ANODE - d	ANODE - e
7	CATHODE - e	CATHODE - e	NO PIN	ANODE - c
8	CATHODE - d	CATHODE - d	NO PIN	ANODE - dp
9	NO CONN.[14]	CATHODE - dp	CATHODE[15]	NO PIN
10	CATHODE - c	CATHODE - c	ANODE - dp	CATHODE - dp
11	CATHODE - g	CATHODE - g	ANODE - c	CATHODE - b
12	NO PIN	NO PIN	ANODE - b	CATHODE - a
13	CATHODE - b	CATHODE - b	ANODE - a	ANODE - a
14	ANODE[12]	ANODE[12]	NO PIN	ANODE - b



A,B,D
SIDE

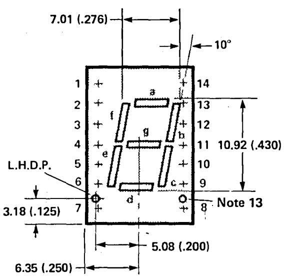


C
SIDE

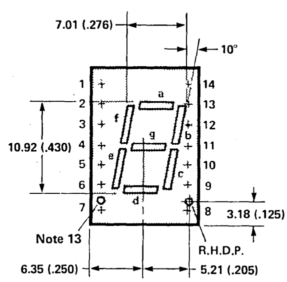


A,B,C,D
END

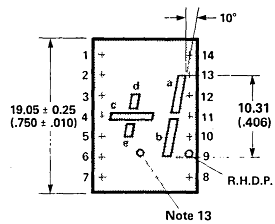
(5082-7750/-7650/-7660/-4600)



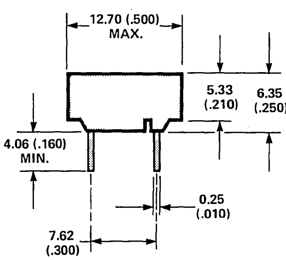
E



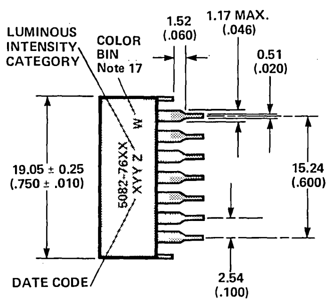
F,G
FRONT VIEW



H



END VIEW



SIDE VIEW

PIN	FUNCTION E	F	G	H
1	CATHODE - a	CATHODE - a	ANODE - a	CATHODE - d
2	CATHODE - f	CATHODE - f	ANODE - f	ANODE - d
3	ANODE[12]	ANODE[12]	CATHODE[15]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE - c
5	NO PIN	NO PIN	NO PIN	CATHODE - e
6	CATHODE - dp	NO CONN.[14]	NO CONN.[14]	ANODE - e
7	CATHODE - e	CATHODE - e	ANODE - e	ANODE - c
8	CATHODE - d	CATHODE - d	ANODE - d	ANODE - dp
9	NO CONN.[14]	CATHODE - dp	ANODE - dp	CATHODE - dp
10	CATHODE - c	CATHODE - c	ANODE - c	CATHODE - b
11	CATHODE - g	CATHODE - g	ANODE - g	CATHODE - a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE - b	CATHODE - b	ANODE - b	ANODE - a
14	ANODE[12]	ANODE[12]	CATHODE[15]	ANODE - b

NOTES:
10. Dimensions in millimetres and (inches).
11. All untoleranced dimensions are for reference only.
12. Redundant anodes.
13. Unused dp position.
14. See Internal Circuit Diagram.
15. Redundant cathode.
16. See part number table for L.H.D.P. and R.H.D.P. designation.
17. For yellow and green devices only.

SOLID STATE DISPLAYS

Electrical/Optical Characteristics at T_A=25°C

RED 5082-7730/-7750 SERIES

Parameter	Device HDSP-	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/ Segment[18] (Digit Average)	-7730 Series	I_V	20 mA DC	360	770		μcd
			100 mA Pk 1:10 Duty Factor		400		
	-7750 Series		20 mA DC	360	1100		
			100 mA Pk 1:10 Duty Factor		570		
Peak Wavelength		λ_{PEAK}			655		nm
Dominant Wavelength[19]		λ_d			640		nm
Forward Voltage/Segment or D.P.[21]		V_F	$I_F = 20$ mA		1.6	2.0	V
Reverse Voltage/Segment or D.P.[21,22]		V_R	$I_R = 100\ \mu A$	3.0	30.0		V
Temperature Coefficient of V_F/Segment or D.P.		$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$			282		°C/W/ Seg

HIGH EFFICIENCY RED 5082-7610/-7650 SERIES

Parameter	Device HDSP-	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/ Segment[18] (Digit Average)	-7610 Series	I_V	5 mA DC	340	800		μcd
			60 mA Pk 1:6 Duty Factor		2800		
	-7650 Series		5 mA DC	340	1115		
			60 mA Pk 1:10 Duty Factor		3900		
Peak Wavelength		λ_{PEAK}			635		nm
Dominant Wavelength[19]		λ_d			626		nm
Forward Voltage/Segment or D.P.[21]		V_F	$I_F = 5$ mA		1.7		
			$I_F = 20$ mA		2.0	2.5	V
			$I_F = 60$ mA		2.8		
Reverse Voltage/Segment or D.P.[21,22]		V_R	$I_R = 100\ \mu A$	3.0	30.0		V
Temperature Coefficient of V_F/Segment or D.P.		$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$			282		°C/W/ Seg

YELLOW 5082-7620/-7660 SERIES (continued)

Parameter	Device HDSP-	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/ Segment[18] (Digit Average)	-7620 Series	I_V	5 mA DC	205	620		μcd
			60 mA Pk 1:6 Duty Factor		2414		
	-7660 Series		5 mA DC	290	835		
			60 mA Pk 1:6 Duty Factor		3250		
Peak Wavelength		λ_{PEAK}			583		nm
Dominant Wavelength[19,20]		λ_d		581.5	586	592.5	nm
Forward Voltage/Segment or D.P.[21]		V_F	$I_F = 5$ mA		1.8		
			$I_F = 20$ mA		2.2	2.5	V
			$I_F = 60$ mA		3.1		
Reverse Voltage/Segment or D.P.[21,22]		V_R	$I_R = 100$ μA	3.0	50.0		V
Temperature Coefficient of V_F/Segment or D.P.		$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$			282		°C/W/ Seg

HIGH PERFORMANCE GREEN HDSP-3600/-4600 SERIES

Parameter	Device HDSP-	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/ Segment[18] (Digit Average)	-3600 Series	I_V	10 mA DC	570	1800		μcd
			60 mA Pk 1:6 Duty Factor		2350		
	-7750 Series		10 mA DC	460	1750		
			60 mA Pk 1:6 Duty Factor		2280		
Peak Wavelength		λ_{PEAK}			566		nm
Dominant Wavelength[19,20] (Digit Average)		λ_d			571	577	nm
Forward Voltage/Segment or D.P.[21]		V_F	$I_F = 10$ mA		2.1	2.5	V
Reverse Voltage/Segment or D.P.[21,22]		V_R	$I_R = 100$ μA	3.0	50.0		V
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$			282		°C/W/ Seg

NOTES:

18. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
19. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is that single wavelength which defines the color of the device.
20. The displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
21. Quality level for electrical characteristics is 1000 parts per million.
22. Typical specification is for reference only. Do not exceed absolute maximum ratings.

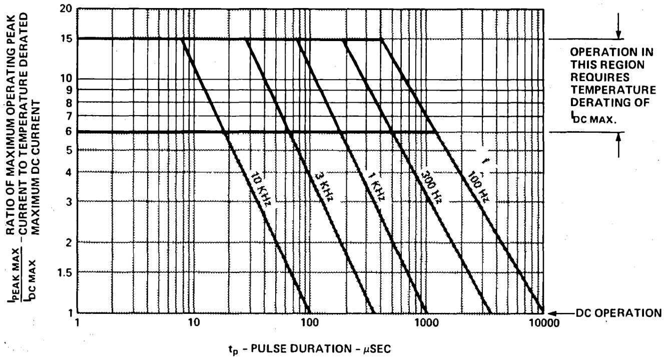


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration) 5082-7730/-7750 Series

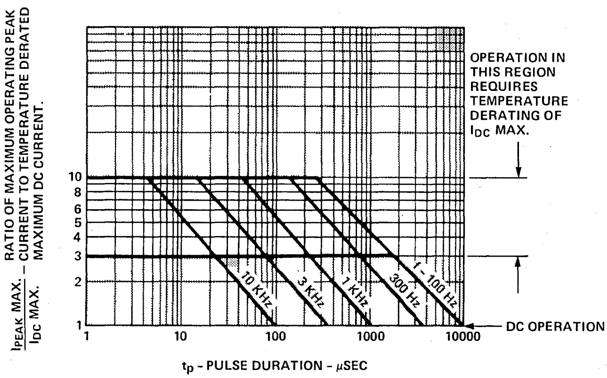


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration — 5082-7610/-7650 Series

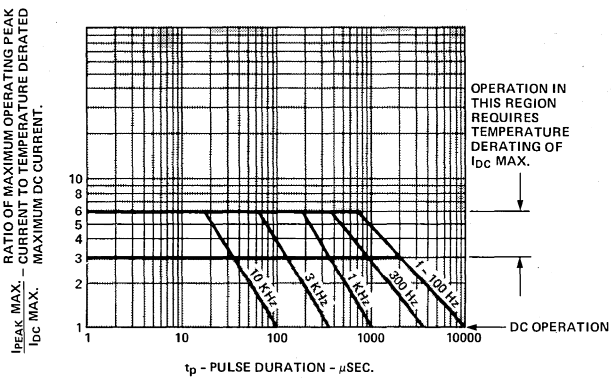


Figure 3. Maximum Tolerable Peak Current vs. Pulse Duration — 5082-7620/-7660 Series

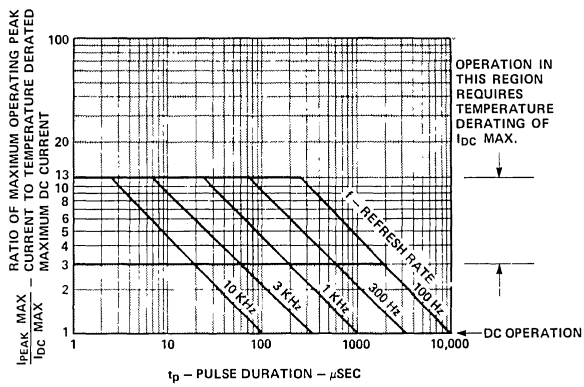


Figure 4. Allowed Peak Current vs. Pulse Duration — HDSP-3600/-4600 Series

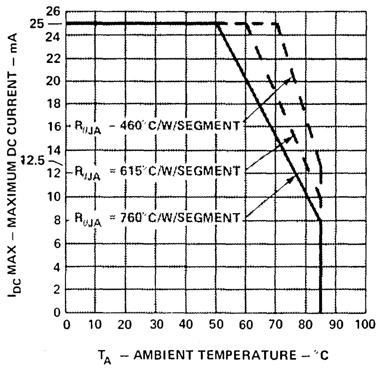


Figure 5. Maximum Allowable DC Current Dissipation per Segment as a Function of Ambient Temperature- 5082-7730/-7750 Series

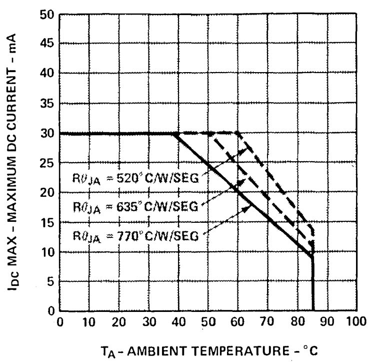


Figure 6. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature — 5082-7610/-7650 Series

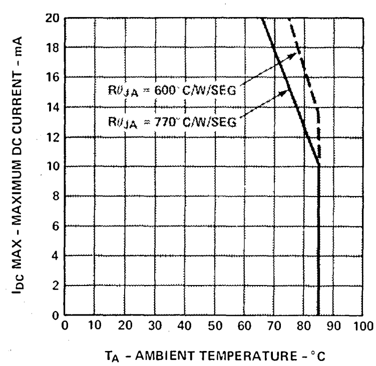


Figure 7. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature — 5082-7620/-7660 Series

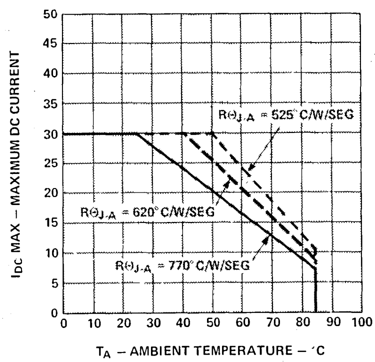


Figure 8. Maximum Allowable DC Current per Segment vs. Ambient Temperature — HDSP-3600/-4600 Series

SOLID STATE DISPLAYS

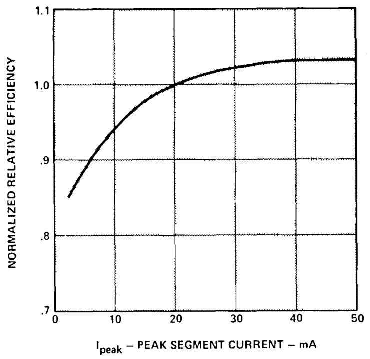


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment- 5082-7730/-7750 Series

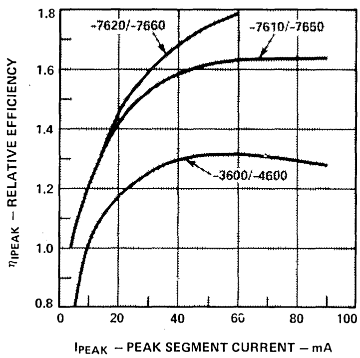


Figure 10. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

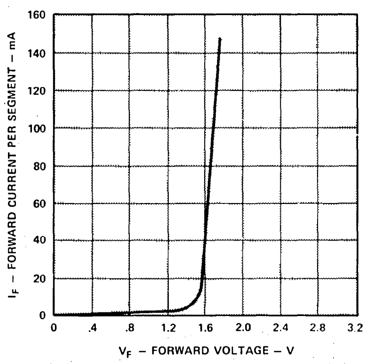


Figure 11. Forward Current vs. Forward Voltage- 5082-7730/-7750 Series.

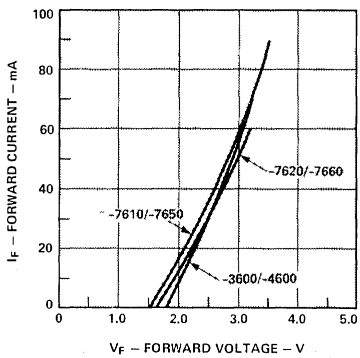


Figure 12. Forward Current vs. Forward Voltage Characteristics

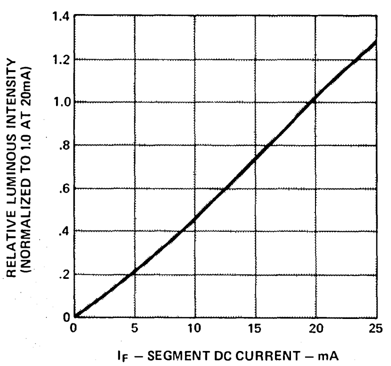


Figure 13. Relative Luminous Intensity vs. DC Forward Current- 5082-7730/-7750 Series

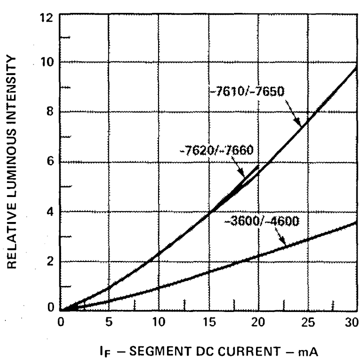


Figure 14. Relative Luminous Intensity vs. DC Forward Current

Electrical

These display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points.

These display devices are well suited for strobed operation. The typical forward voltage values, scaled from Figure 8, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

5082-7730/-7750 Series:
$V_F = 1.55V + I_{PEAK} (7\Omega)$
For $5\ mA \leq I_{PEAK} \leq 150\ mA$

5082-7610/-7620/-7650/-7660 Series:
$V_F\ MAX = 1.75\ V + I_{PEAK} (38\Omega)$
For: $I_{PEAK} \geq 20\ mA$
$V_F MAX = 1.6\ V + I_{DC} (45\Omega)$
For: $5\ mA \leq I_{DC} \leq 20\ mA$

HDSP-3600/-4600 Series:
$V_F\ MAX = 2.0\ V + I_{PEAK} (50\Omega)$
For: $I_{PEAK} \geq 5\ mA$

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance readability by having the OFF-segments blend into the display background and the ON-segments stand out vividly against this same background. Therefore, these display devices are assembled with a package color which matches the encapsulating epoxy in the segments.

Contrast enhancement may be achieved by using one of the following suggested filters:

5082-7730/ -7750	Panelgraphic RUBY RED 60 or GRAY 10 SGL Homalite H100-1605 RED or -1266 GRAY 3M Louvered Filter R6510 RED or N0210 GRAY
5082-7610/ -7650	Panelgraphic SCARLET RED 65 or GRAY 10 SGL Homalite H100-1670 RED or -1266 GRAY 3M Louvered Filter R6310 RED or N0210 GRAY
5082-7620/ -7660	Panelgraphic YELLOW 27 or GRAY 10 SGL Homalite H100-1720 AMBER or -1266 GRAY 3M Louvered Filter A5910 AMBER or N0210 GRAY
HDSP-3600/ -4600	Panelgraphic GREEN 48 SGL Homalite H100-1440 GREEN 3M Louvered Filter G5610 GREEN or N0210 GRAY

Mechanical

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes. with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolve DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Such cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the packages of plastic LED devices.

HEWLETT PACKARD

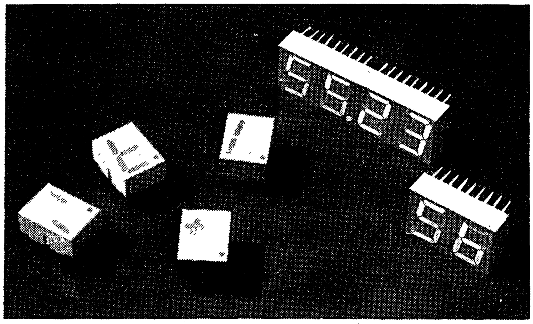
14.2mm (.56 INCH) SEVEN SEGMENT DISPLAYS

RED HDSP-5300 SERIES
HIGH EFFICIENCY RED HDSP-5500 SERIES
HIGH PERFORMANCE GREEN HDSP-5600 SERIES
YELLOW HDSP-5700 SERIES

TECHNICAL DATA JANUARY 1986

Features

- **INDUSTRY STANDARD SIZE**
- **INDUSTRY STANDARD PINOUT**
  15.24mm (.6 inch) DIP Leads on 2.54mm (.1 inch) Centers
- **CHOICE OF FOUR COLORS**
  Red Yellow
  High-Efficiency Red High Performance Green
- **EXCELLENT CHARACTER APPEARANCE**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray Package Gives Optimum Contrast
- **COMMON ANODE OR COMMON CATHODE**
  Right Hand Decimal Point
  Overflow ±1 Character
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW AND GREEN CATEGORIZED FOR COLOR**
  Use of Like Categories Yields a Uniform Display



Description

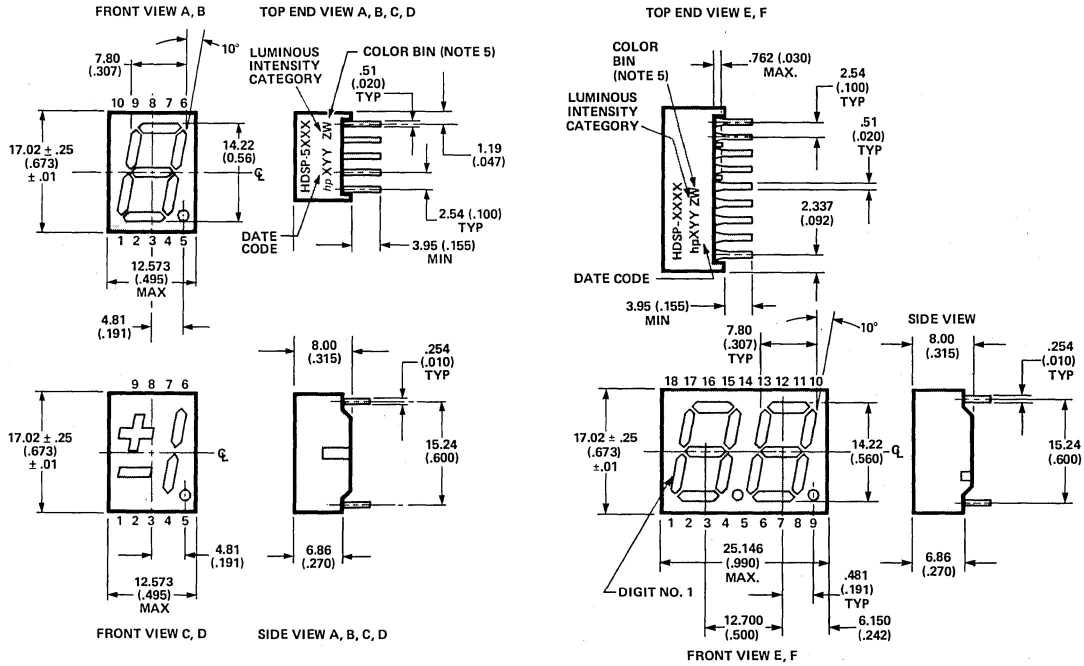
The HDSP-5300/-5500/-5600/-5700 Series are large 14.22 mm (.56 inch) LED seven segment displays. Designed for viewing distances up to 7 metres (23 feet), these displays provide excellent readability in bright ambients.

These devices utilize an industry standard size package and pin function configuration. Both the numeric and ±1 overflow devices feature a right hand decimal point and are available as either common anode or common cathode.

Devices

Part No. HDSP-	Color	Description	Package Drawing
5301	Red	Common Anode Right Hand Decimal	A
5303		Common Cathode Right Hand Decimal	B
5307		Overflow ± Common Anode	C
5308		Overflow ± Common Cathode	D
5321		Two Digit Common Anode Right Hand Decimal	E
5323		Two Digit Common Cathode Right Hand Decimal	F
5501	High Efficiency Red	Common Anode Right Hand Decimal	A
5503		Common Cathode Right Hand Decimal	B
5507		Overflow ± Common Anode	C
5508		Overflow ± Common Cathode	D
5521		Two Digit Common Anode Right Hand Decimal	E
5523		Two Digit Common Cathode Right Hand Decimal	F
5601	High Performance Green	Common Anode Right Hand Decimal	A
5603		Common Cathode Right Hand Decimal	B
5607		Overflow ± Common Anode	C
5608		Overflow ± Common Cathode	D
5621		Two Digit Common Anode Right Hand Decimal	E
5623		Two Digit Common Cathode Right Hand Decimal	F
5701	Yellow	Common Anode Right Hand Decimal	A
5703		Common Cathode Right Hand Decimal	B
5707		Overflow ± Common Anode	C
5708		Overflow ± Common Cathode	D
5721		Two Digit Common Anode Right Hand Decimal	E
5723		Two Digit Common Cathode Right Hand Decimal	F

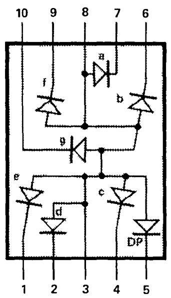
Package Dimensions



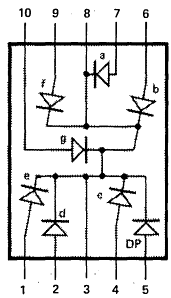
PIN	FUNCTION					
	A	B	C	D	E	F
1	CATHODE e	ANODE e	CATHODE c	ANODE c	E CATHODE NO. 1	E ANODE NO. 1
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d	D CATHODE NO. 1	D ANODE NO. 1
3	ANODE[3]	CATHODE[4]	CATHODE b	ANODE b	C CATHODE NO. 1	C ANODE NO. 1
4	CATHODE c	ANODE c	ANODE a, b, DP	CATHODE a, b, DP	DP CATHODE NO. 1	DP ANODE NO. 1
5	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP	E CATHODE NO. 2	E ANODE NO. 2
6	CATHODE b	ANODE b	CATHODE a	ANODE a	D CATHODE NO. 2	D ANODE NO. 2
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP	G CATHODE NO. 2	G ANODE NO. 2
8	ANODE[3]	CATHODE[4]	ANODE c, d	CATHODE c, d	C CATHODE NO. 2	C ANODE NO. 2
9	CATHODE f	ANODE f	CATHODE d	ANODE d	DP CATHODE NO. 2	DP ANODE NO. 2
10	CATHODE g	ANODE g	NO PIN	NO PIN	B CATHODE NO. 2	B ANODE NO. 2
11					A CATHODE NO. 2	A ANODE NO. 2
12					F CATHODE NO. 2	F ANODE NO. 2
13					DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14					DIGIT NO. 1 ANODE	DIGIT NO. 1 CATHODE
15					B CATHODE NO. 1	B ANODE NO. 1
16					A CATHODE NO. 1	A ANODE NO. 1
17					G CATHODE NO. 1	G ANODE NO. 1
18					F CATHODE NO. 1	F ANODE NO. 1

Notes:
1. All dimensions in millimetres (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Redundant cathodes.
5. For HDSP-5600/-5700 series product only.

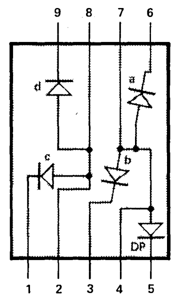
Internal Circuit Diagram



A



B



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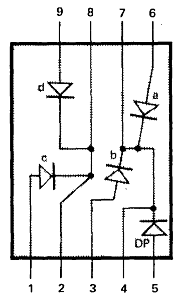
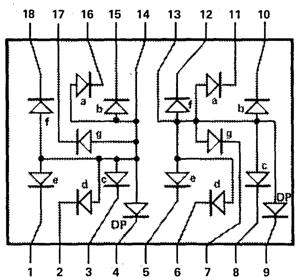
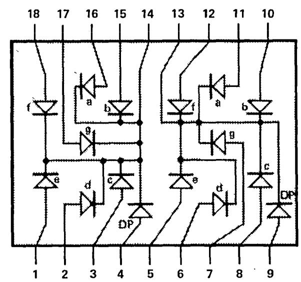


D



E



F

Absolute Maximum Ratings

	-5300 Series	-5500 Series	-5600 Series	-5700 Series
Average Power per Segment or DP	60 mW	105 mW	105 mW	80 mW
Peak Forward Current per Segment or DP	150 mA[6] (Pulse Width ≤ .2 ms)	90 mA[7] (Pulse Width ≤ 1 ms)	90 mA[7] (Pulse Width ≤ 1 ms)	60 mA[8] (Pulse Width ≤ 1 ms)
DC Forward Current per Segment[9] or DP	25 mA	30 mA	30 mA	20 mA
Operating Temperature Range [10]	−40° C to +85° C	−40° C to +85° C	−20° C to +85° C	−40° C to +85° C
Storage Temperature Range	−55° C to +100° C	−55° C to +100° C	−55° C to +100° C	−55° C to +100° C
Reverse Voltage per Segment or DP	3.0V	3.0V	3.0V	3.0V
Lead Solder Temperature	260° C for 3 sec.	260° C for 3 sec.	260° for 3 sec.	260° for 3 sec.

(1.59 mm [1/16 in.] below seating plane)

Notes:

6. See Figure 1 to establish pulsed operating conditions.
7. See Figure 6 to establish pulsed operating conditions. HDSP-5500. See Figure 7 to establish pulsed operating conditions. HDSP-5600.
8. See Figure 8 to establish pulsed operating conditions.
9. Derate Maximum DC current: See Figure 2 for -5300 Series. See Figure 9 for -5500 Series. See Figure 10 for -5600 Series. See Figure 11 for -5700 Series.
10. For Operation of HDSP-5600 Series to −40°C consult optoelectronics division.

Electrical/Optical Characteristics at $T_A = 25°C$

RED HDSP-5300 Series

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[11] (Digit Average)	I_v	$I_F = 20$ mA	600	1300		μcd
		100 mA Peak: 1 of 5 Duty Factor		1400		
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[12]	λ_d			640		nm
Forward Voltage/Segment or DP[13]	V_F	$I_F = 20$ mA		1.6	2.0	V
Reverse Voltage/Segment or DP[13,18]	V_R	$I_R = 100$ μA	3	12		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			345		°C/W/ Seg.

Notes:

11. The digits are categorized for luminous intensity with category designated by a letter located on the right hand side of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual segment intensities, decimal point not included.
12. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is that single wavelength which defines the color of the device.
13. Quality level for Electrical Characteristics is 1000 parts per million.

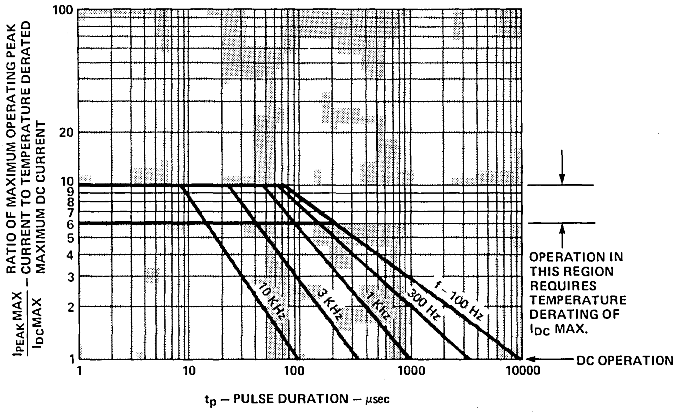


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

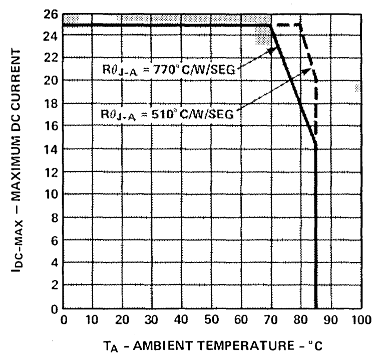


Figure 2. Maximum Allowable Average Forward Current Per Segment vs. Ambient Temperature. Deratings Based on Maximum Allowed Thermal Resistance Values, LED Junction to Ambient on a per Segment Basis. T_J MAX = 105° C.

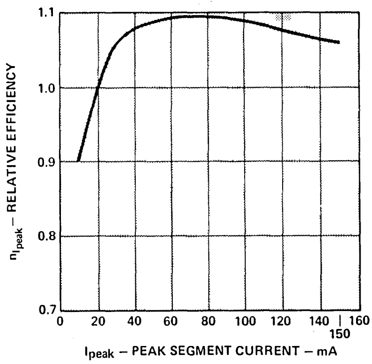


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

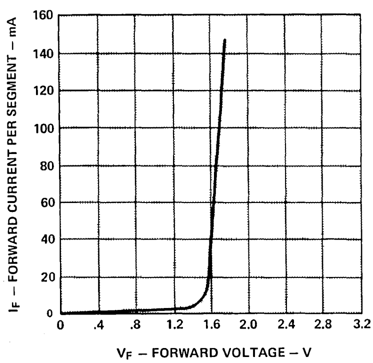


Figure 4. Forward Current vs. Forward Voltage.

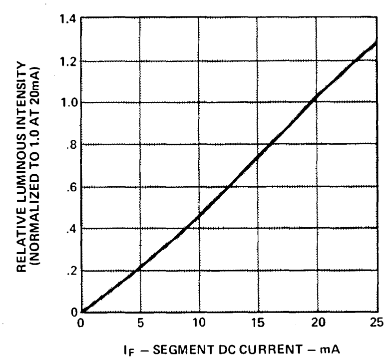


Figure 5. Relative Luminous Intensity vs. D.C. Forward Current.

For a Detailed Explanation of the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

HIGH EFFICIENCY RED HDSP-5500 SERIES

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[14] (Digit Average)	I_V	10 mA DC	900	2800		μcd
		60 mA Peak: 1 of 6 Duty Factor		3700		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[15]	λ_d			626		nm
Forward Voltage/Segment or DP[17]	V_F	$I_F = 20$ mA		2.1	2.5	V
Reverse Voltage/Segment or DP[18]	V_R	$I_R = 100\ \mu$A	3	30		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			345		°C/W/Seg.

HIGH PERFORMANCE GREEN HDSP-5600 SERIES

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[14] (Digit Average)	I_V	10 mA DC	900	2500		μcd
		60 mA Peak: 1 of 6 Duty Factor		3100		
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[15,16]	λ_d			571	577	nm
Forward Voltage/Segment or DP[17]	V_F	$I_F = 10$ mA		2.1	2.5	V
Reverse Voltage/Segment or DP[17,18]	V_R	$I_R = 100\ \mu$A	3	50		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			345		°C/W/Seg.

YELLOW HDSP-5700 SERIES

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[14] (Digit Average)	I_V	10 mA DC	600	1800		μcd
		60 mA Peak: 1 of 6 Duty Factor		2700		
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[15,16]	λ_d		581.5	586	592.5	nm
Forward Voltage/Segment or DP[17]	V_F	$I_F = 20$ mA		2.2	2.5	V
Reverse Voltage/Segment or DP[17,18]	V_R	$I_R = 100\ \mu$A	3	40		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			345		°C/W/Seg.

Notes:

14. The digits are categorized for luminous intensity with category designated by a letter located on top of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual segment intensities, decimal point not included.
15. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is that single wavelength which defines the color of the device.
16. The HDSP-5600 and HDSP-5700 series displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
17. Quality level for Electrical Characteristics is 1000 parts per million.
18. Typical specification for reference only. Do not exceed absolute maximum ratings.

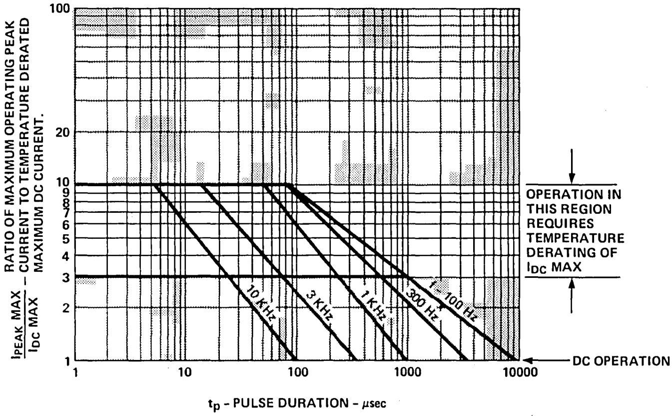


Figure 6. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-5500 Series.

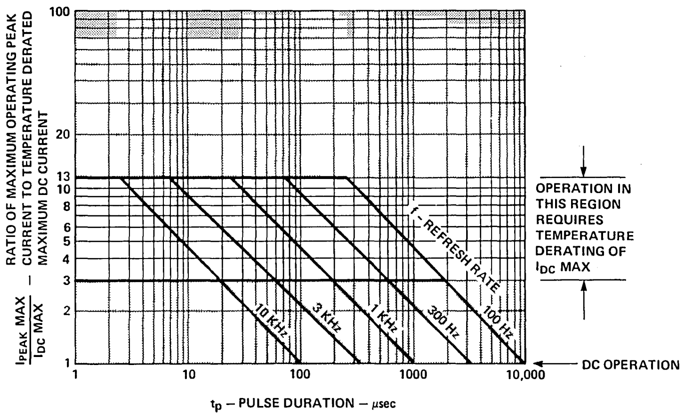


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-5600 Series.

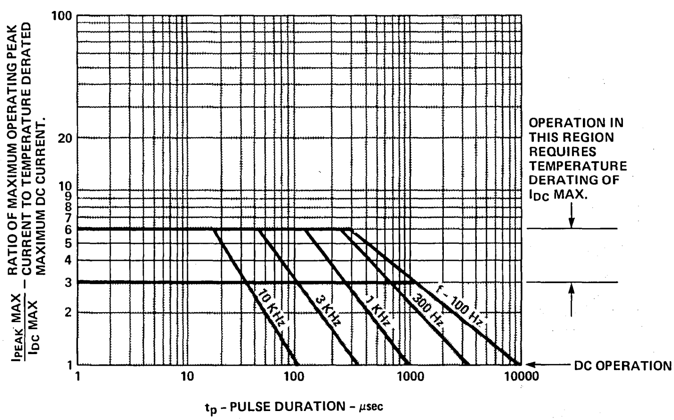


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-5700 Series.

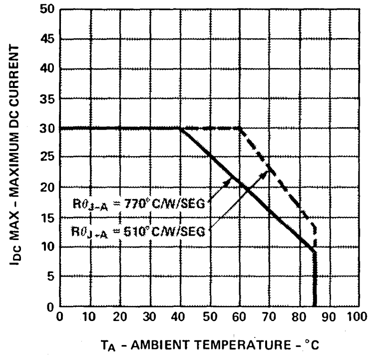


Figure 9. Maximum Allowable Average Current per Segment vs. Ambient Temperature. Derating Based on Maximum Allowed Thermal Resistance Values. LED Junction to Ambient on a per Segment Basis. T_J LED MAX = 105° C — HDSP-5500 Series.

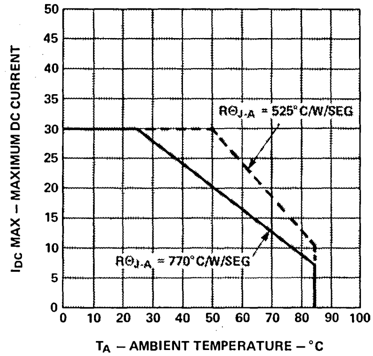


Figure 10. Maximum Allowable Average Current per Segment vs. Ambient Temperature. Derating Based on Maximum Allowed Thermal Resistance Values, LED Junction to Ambient on a per Segment Basis. T_J LED MAX = 105° C. — HDSP-5600 Series.

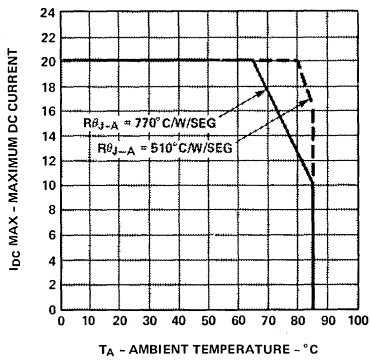


Figure 11. Maximum Allowable Average Current per Segment vs. Ambient Temperature. Derating Based on Maximum Allowed Thermal Resistance Values, LED Junction to Ambient on a per Segment Basis. T_J LED MAX = 105° C — HDSP-5700 Series.

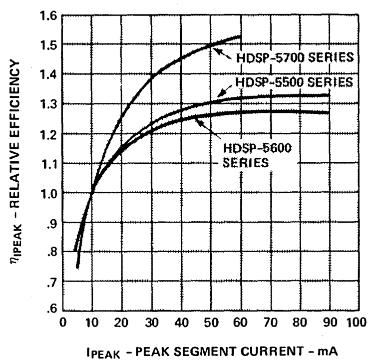


Figure 12. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

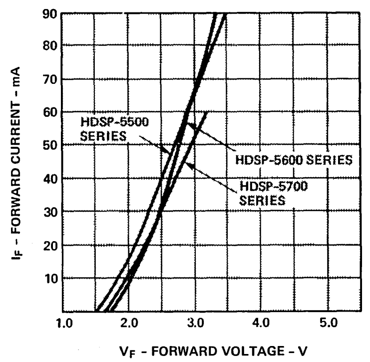


Figure 13. Forward Current vs. Forward Voltage Characteristics.

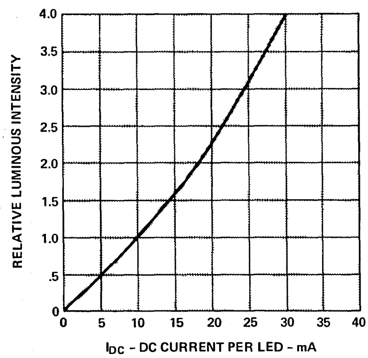


Figure 14. Relative Luminous Intensity vs. DC Forward Current. HDSP-5500/-5600/-5700

Electrical

The HDSP-5300/-5500/-5600/-5700 series of display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The -5300 series uses a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The -5500 and -5700 series have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The -5600 series use a GaP epitaxial layer on GaP.

These display devices are designed for strobed operation. The typical forward voltage values, scaled from Figure 4 or 13, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

HDSP-5300 Series:

V_F MAX $= 1.55V + I_{PEAK}$ (7Ω)
For: $I_{PEAK} \geq 5$ mA

HDSP-5500/-5700 Series:

V_F MAX $= 1.75V + I_{PEAK}$ (38Ω)
For: $I_{PEAK} \geq 20$ mA
V_F MAX $= 1.5V + I_{DC}$ (45Ω)
For: 5 mA $\leq I_{DC} \leq$ 20 mA

HDSP-5600 Series:

V_F MAX $= 2.0V + I_{PEAK}$ (50Ω)
For: $I_{PEAK} \geq 5$ mA

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance readibility by having the OFF-segments blend into the display background and the ON-segments stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the segments.

Contrast enhancement may be achieved by using one of the following suggested filters:

HDSP-5300: Panelgraphic RUBY RED 60
SGL Homalite H100-1605 RED
3M Louvered Filter R6610 RED or N0210 GRAY

HDSP-5500: Panelgrahpic SCARLET RED 65 or GRAY 10
SGL Homalite H100-1670 RED or -1266 GRAY
3M Louvered Filter R6310 RED or N0210 GRAY

HDSP-5600: Panelgraphic GREEN 48
SGL Homalite H100-1440 GREEN
3M Louvered Filter G5610 GREEN or N0210 GRAY

HDSP-5700: Panelgraphic YELLOW 27 or GRAY 10
SGL Homalite H100-1720 AMBER or -1266 GRAY
3M Louvered Filter A5910 AMBER or N0210 GRAY

Mechanical

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolve DI-15 or DE-15. Arklone A or K. A 60° C (140° F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Such cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the packages of plastic LED devices.

HEWLETT PACKARD

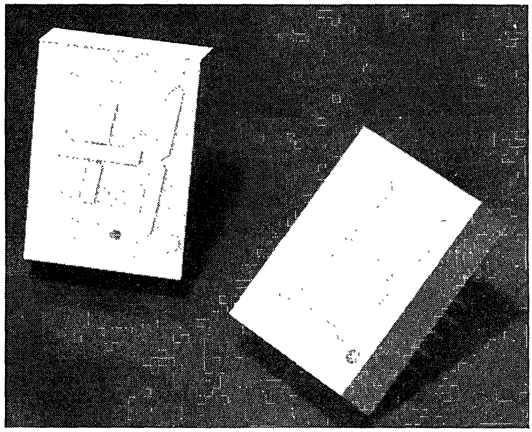
LARGE 20 mm (0.8") SEVEN SEGMENT DISPLAYS

RED HDSP-3400 Series
HIGH EFFICIENCY RED HDSP-3900 Series
YELLOW HDSP-4200 Series
HIGH PERFORMANCE GREEN HDSP-8600 Series

TECHNICAL DATA JANUARY 1986

Features

- **20 mm (0.8") DIGIT HEIGHT**
  Viewable Up to 10 Metres (33 Feet)
- **CHOICE OF FOUR COLORS**
  Red Yellow
  High Efficiency Red Green
- **EXCELLENT CHARACTER APPEARANCE**
  Evenly Lighted Segments
  Wide Viewing Angle
  Mitered Corners on Segments
  Grey Package Provides Optimum Contrast
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW AND GREEN CATEGORIZED FOR COLOR**
  Use of Like Categories Yields a Uniform Display
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

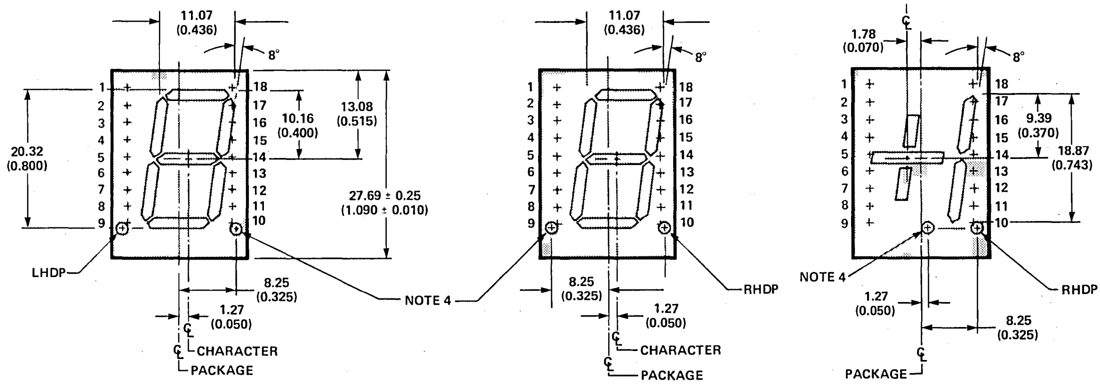
The HDSP-3400/-3900/-4200/-8600 Series are very large 20 mm (0.8 in.) LED seven segment displays. Designed for viewing distances up to 10 metres (33 feet), these single digit displays provide excellent readability.

These devices utilize a standard 15.24 mm (0.6 in.) dual in line package configuration that permits mounting on PC boards or in standard IC sockets. Requiring a low forward voltage, these displays are inherently IC compatible, allowing for easy integration into electronic instrumentation, point-of-sale terminals, TVs, weighing scales, and digital clocks.

Devices

Part Number	Color	Description	Package Drawing
HDSP-3400	Red	Common Anode Left Hand Decimal	A
HDSP-3401		Common Anode Right Hand Decimal	B
HDSP-3403		Common Cathode Right Hand Decimal	C
HDSP-3405		Common Cathode Left Hand Decimal	D
HDSP-3406		Universal Overflow ±1 Right Hand Decimal	E
HDSP-3900	High Efficiency Red	Common Anode Left Hand Decimal	A
HDSP-3901		Common Anode Right Hand Decimal	B
HDSP-3903		Common Cathode Right Hand Decimal	C
HDSP-3905		Common Cathode Left Hand Decimal	D
HDSP-3906		Universal Overflow ±1 Right Hand Decimal	E
HDSP-4200	Yellow	Common Anode Left Hand Decimal	A
HDSP-4201		Common Anode Right Hand Decimal	B
HDSP-4203		Common Cathode Right Hand Decimal	C
HDSP-4205		Common Cathode Left Hand Decimal	D
HDSP-4206		Universal Overflow ±1 Right Hand Decimal	E
HDSP-8600	High Performance Green	Common Anode Left Hand Decimal	A
HDSP-8601		Common Anode Right Hand Decimal	B
HDSP-8603		Common Cathode Right Hand Decimal	C
HDSP-8605		Common Cathode Left Hand Decimal	D
HDSP-8606		Universal Overflow ±1	E

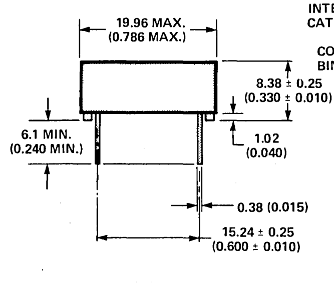
Package Dimensions (3900/4200 Series)



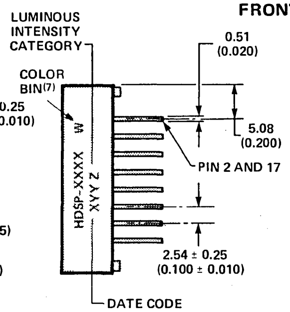
FRONT VIEW A, D

FRONT VIEW B, C

FRONT VIEW E



END VIEW

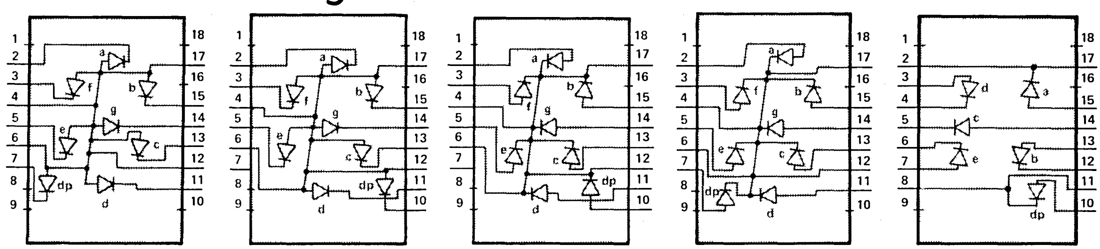


SIDE VIEW

Pin	Function: A 3400/3900/ 4200/8600	B 3401/3901/ 4201/8601	C 3403/3903/ 4203/8603	D 3405/3905/ 4205/8605	E 3406/3906/ 4206/8606
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE e
7	CATHODE dp	NO. CONNEC.	NO. CONNEC.	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant Cathodes.
7. For HDSP-4200/-8600 Series product only.
8. See part number table for LHDP and RHDP designation.

Internal Circuit Diagram



A B C D E

Absolute Maximum Ratings

	-3400 Series	-3900/-4200 Series	-8600 Series
Average Power per Segment or DP ($T_A = 25°C$)[9]	120 mW	105 mW	105 mW
Operating Temperature Range[10]	−40° C to +85° C	−40° C to +85° C	−20° C to +85° C
Storage Temperature Range	−55° C to +100° C	−55° C to +100° C	−55° C to +100° C
Peak Forward Current per Segment or DP ($T_A = 25°C$, Pulse Width = 1.2 ms)[11]	200 mA	135 mA	90 mA
DC Forward Current per Segment or DP ($T_A = 25°C$)[9]	50 mA	40 mA	30 mA
Reverse Voltage per Segment or DP	3.0 V	3.0 V	3.0 V
Lead Soldering Temperature (1.6 mm [1/6 in.] Below Seating Plane)	260° C for 3 sec.	260° C for 3 sec.	260° C for 3 sec.

Notes:

9. See Power Derating Curves (see Figure 2 for -3400 Series, Figure 7 for -3900/-4200 Series, and Figure 12 for -8600 Series).
10. For operation of -8600 series to -40°C consult Optoelectronics division.
11. See appropriate curves to establish pulsed operating conditions (see Figure 1 for -3400 Series, Figure 6 for -3900/-4200 Series, Figure 11 for -8600 Series).

SOLID STATE DISPLAYS

Electrical/Optical Characteristics at $T_A = 25°C$

RED HDSP-3400 SERIES

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[12,13]	I_V	$I_F = 20$ mA	500	1200		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[14]	λ_d			640		nm
Forward Voltage, any Segment or DP[16]	V_F	$I_F = 20$ mA		1.6	2.0	V
Reverse Voltage, any Segment or DP[15,16]	V_R	$I_R = 100\ \mu$A	3.0	20.0		V
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$	$I_F = 20$ mA		−1.5		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			375		°C/W/ Seg

HIGH EFFICIENCY RED HDSP-3900 SERIES

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[12,13]	I_V	100 mA Pk; 1 of 5 Duty Factor	3350	7000		μcd
		20 mA DC		4800		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[14] (Digit Average)	λ_d			626		nm
Forward Voltage, any Segment or DP[16]	V_F	$I_F = 100$ mA		2.6	3.5	V
Reverse Voltage, any Segment or DP[16,17]	V_R	$I_R = 100\ \mu$A	3.0	25.0		V
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$	$I_F = 100$ mA		−1.1		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			375		°C/W/ Seg

YELLOW HDSP-4200 SERIES

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[12,13]	I_V	100 mA Pk; 1 of 5 Duty Factor	2200	7000		μcd
		20 mA DC		3400		
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[14,15] (Digit Average)	λ_d		581.5	586	592.5	nm
Forward Voltage, any Segment or DP[16]	V_F	$I_F = 100$ mA		2.6	3.5	V
Reverse Voltage, any Segment or DP[16,17]	V_R	$I_R = 100\ \mu$A	3.0	25.0		V
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$	$I_F = 100$ mA		−1.1		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			375		°C/W/ Seg

HIGH PERFORMANCE GREEN HDSP-8600 SERIES

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[12,13]	Iv	60 mA Pk; 1 of 5 Duty Factor		1960		μcd
		10 mA DC	700	1500		
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[14,15] (Digit Average)	λ_d			571	577	nm
Forward Voltage, any Segment or DP[16]	V_F	$I_F = 10$ mA		2.1	2.5	V
Reverse Voltage, any Segment or DP[16,17]	V_R	$I_R = 100\ \mu A$	3.0	50.0		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			375		°C/W/ Seg

Notes:

12. Case temperature of the device immediately prior to the intensity measurement is 25° C.
13. The digits are categorized for luminous intensity with the intensity category designated by a letter on the side of the package.
14. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
15. The yellow and green displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
16. Quality level for electrical characteristics is 1000 parts per million.
17. Typical specification for reference only. Do not exceed absolute maximum ratings.

HDSP-3400 SERIES

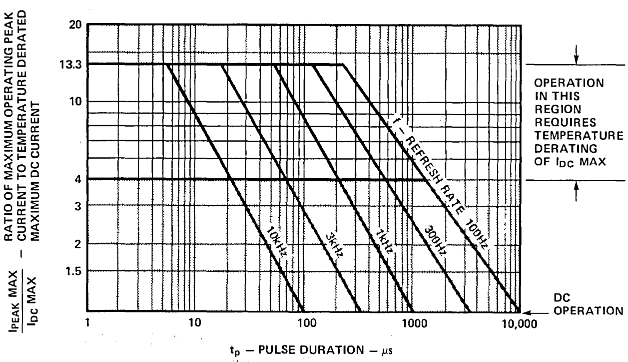


Figure 1. Maximum Allowable Peak Current vs. Pulse Duration

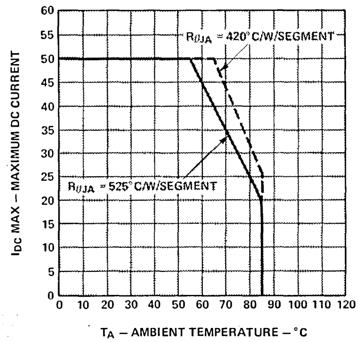


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature

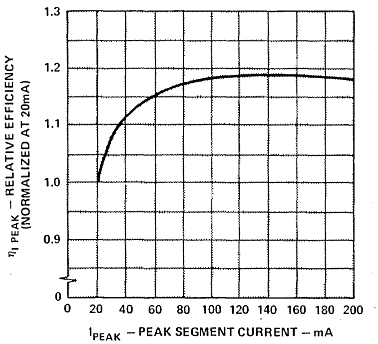


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

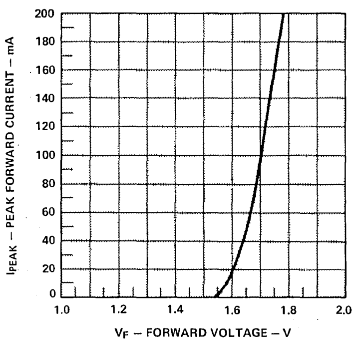


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage

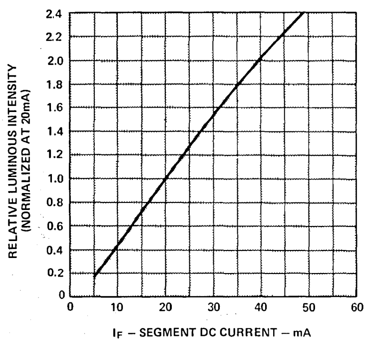


Figure 5. Relative Luminous Intensity vs. DC Forward Current

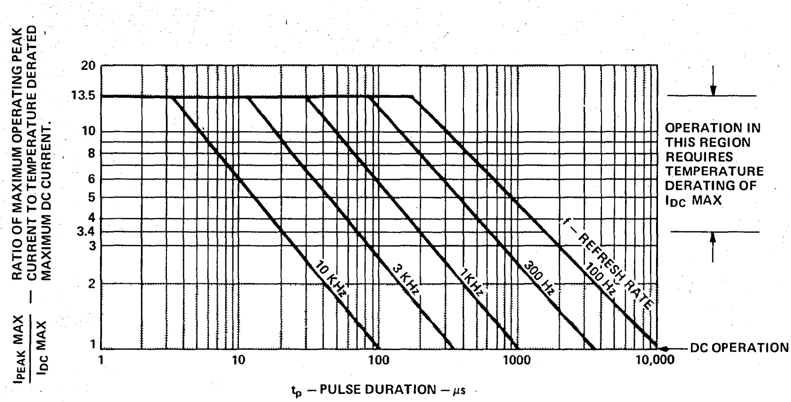


Figure 6. Maximum Allowed Peak Current vs. Pulse Duration

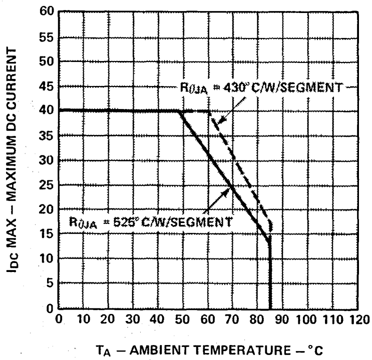


Figure 7. Maximum Allowable DC Current per Segment vs. Ambient Temperature

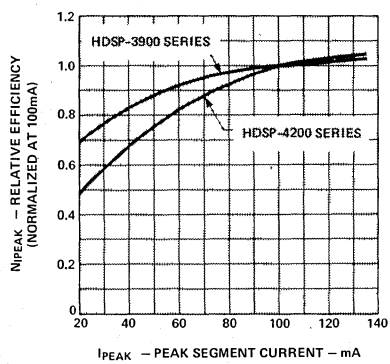


Figure 8. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

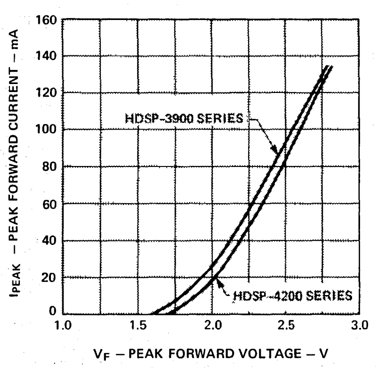


Figure 9. Peak Forward Segment Current vs. Peak Forward Voltage

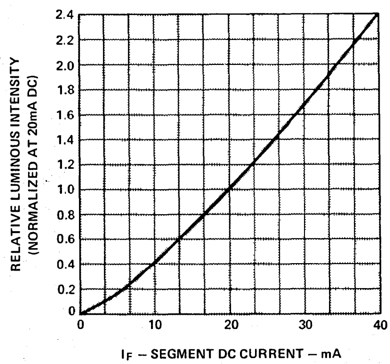


Figure 10. Relative Luminous Intensity vs. DC Forward Current

HDSP-8600 SERIES

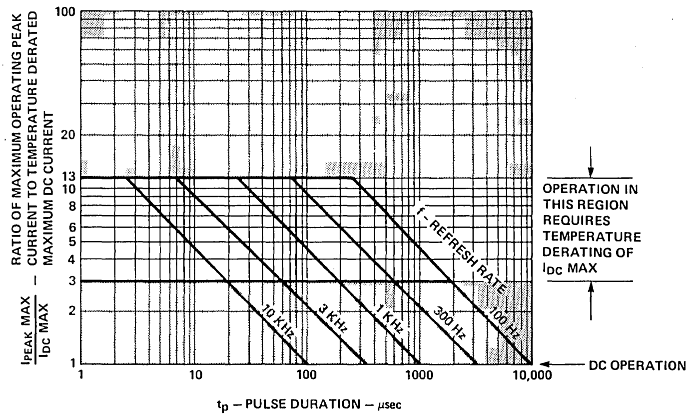


Figure 11. Maximum Allowed Peak Current vs. Pulse Duration

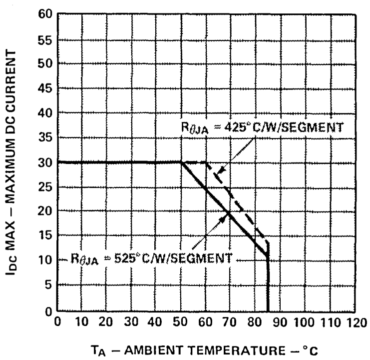


Figure 12. Maximum Allowable DC Current per Segment vs. Ambient Temperature

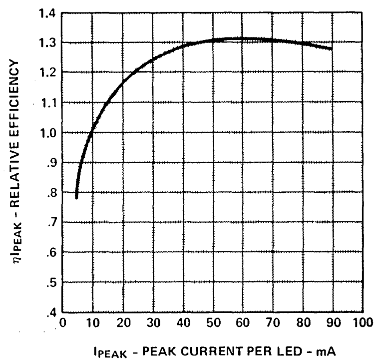


Figure 13. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

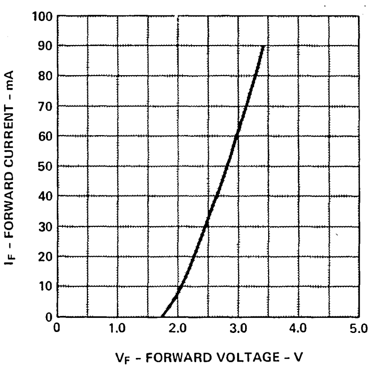


Figure 14. Peak Forward Segment Current vs. Peak Forward Voltage

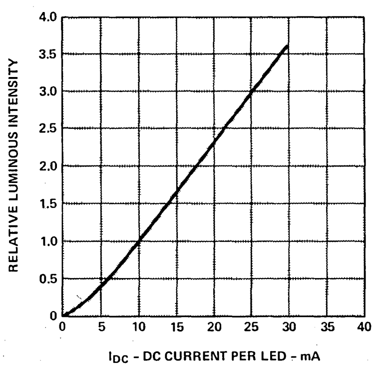


Figure 15. Relative Luminous Intensity vs. DC Forward Current

SOLID STATE DISPLAYS

Electrical

These display devices are composed of eight light emitting diodes, with light from each LED optically stretched to form individual segments and a decimal point.

These display devices are designed for strobed operation. The typical forward voltage values, scaled from Figure 4, 9, or 14 should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

HDSP-3400 Series	V_F MAX = 1.55 V + I_{PEAK} (7Ω) For: $I_{PEAK} \geq 5$ mA
HDSP-3900/-4200 Series	V_F MAX = 2.15 V + I_{PEAK} (13.5Ω) For: $I_F \geq 30$ mA
	V_F MAX = 1.9 V + I_{DC} (21.8Ω) For: 10 mA $\leq I_F \leq$ 30 mA
HDSP-8600 Series	V_F MAX = 2.0 V + I_{PEAK} (50Ω) For: $I_{PEAK} \geq 5$ mA

Temperature derated strobed operating conditions are obtained from Figures 1, 6, or 11 and 2, 7, or 12. Figures 1, 6, and 11 relate pulse duration (t_p), refresh rate (f), and the ratio of maximum peak current to maximum dc current (I_{PEAK} MAX/I_{DC} MAX). Figures 2, 7, and 12 present the maximum allowed dc current vs. ambient temperature. Figures 1, 6, and 11 are based on the principle that the peak junction temperature for pulsed operation at a specified peak current, pulse duration and refresh rate should be the same as the junction temperature at maximum DC operation. Refresh rates of 1 kHz or faster minimize the pulsed junction heating effect of the device resulting in the maximum possible time average luminous intensity.

The time average luminous intensity can be calculated knowing the average forward current and relative efficiency characteristic, η_{IPEAK}, of Figures 3, 8, or 13. Time average luminous intensity for a device case temperature of 25° C, I_V (25° C), is calculated as follows:

$$I_V\ (25°\,C) = \left[\frac{I_{AVG}}{I_{AVG}\ \text{Test Condition}}\right]\left[\eta_{IPEAK}\right]\left[I_V\ \text{DATA SHEET}\right]$$

Example: For HDSP-4200 series

η_{IPEAK} = 1.00 at I_{PEAK} = 100 mA. For DF = 1/5:

$$I_V\ (25°\,C) = \left[\frac{20\ \text{mA}}{20\ \text{mA}}\right]\left[1.00\right]\left[7.0\ \text{mcd}\right] = 7.0\ \text{mcd/segment}$$

The time average luminous intensity may be adjusted for operating junction temperature by the following exponential equation:

$$I_V\ (T_J) = I_V\ (25°\,C)\ e^{[k(T_J + 25°\,C)]}$$

where $T_J = T_A + P_D \cdot R\theta_{J\text{-}A}$

Device	K
-3400	-0.0188/° C
-3900	-0.0131/° C
-4200	-0.0112/° C
-8600	-0.0044/° C

Mechanical

These devices are constructed utilizing a lead frame in a standard DIP package. The LED dice are attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, T_J MAX, is 105° C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit.

Worst case thermal resistance pin-to-ambient is 400° C/W/Seg when these devices are soldered into minimum trace width PC boards. When installed in a PC board that provides $R\theta_{PIN\text{-}A}$ less than 400° C/W/Seg these displays may be operated at higher average currents as shown in Figure 2.

Optical

The radiation pattern for these devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas.

$$L_V(\text{cd/m}^2) = \frac{I_V(\text{cd})}{A(\text{m}^2)}$$

$$L_V(\text{footlamberts}) = \frac{\pi I_V(\text{cd})}{A(\text{ft}^2)}$$

Area/Seg. mm²	Area/Seg. in.²
14.9	0.0231

Contrast Enhancement

The objective of contrast enhancement is to optimize display readability. Adequate contrast enhancement can be achieved in indoor applications through luminous contrast techniques. Luminous contrast is the observed brightness of the illuminated segment compared to the brightness of the surround. Appropriate wavelength filters maximize luminous contrast by reducing the amount of light reflected from the area around the display while transmitting most of the light emitted by the segment. These filters are described further in Application Note 1015.

Chrominance contrast can further improve display readability. Chrominance contrast refers to the color difference between the illuminated segment and the surrounding area. These displays are assembled with a gray package and untinted encapsulating epoxy in the segments to improve chrominance contrast of the ON segments. Additional contrast enhancement in bright ambients may be achieved by using a neutral density gray filter such as Panelgraphic Chromafilter Gray 10, or 3M Light Control Film (louvered film).

SEVEN SEGMENT DISPLAYS FOR HIGH LIGHT AMBIENT CONDITIONS

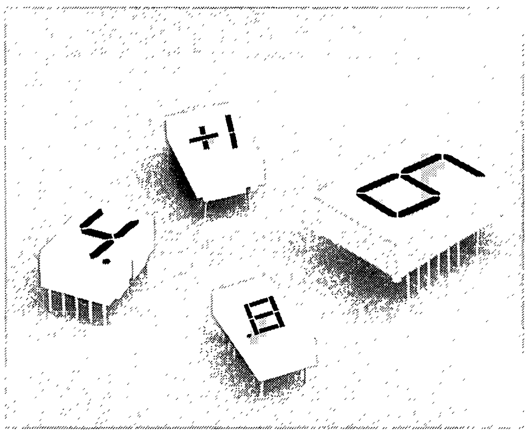
HEWLETT PACKARD

HIGH EFFICIENCY RED HDSP-3530/-3730/-5530/-3900 SERIES
YELLOW HDSP-4030/-4130/-5730/-4200 SERIES

TECHNICAL DATA JANUARY 1986

Features

- **HIGH LIGHT OUTPUT**
  Typical Intensities of up to 7.0 mcd/seg at 100 mA pk 1 of 5 duty factor.
- **CAPABLE OF HIGH CURRENT DRIVE**
  Excellent for Long Digit String Multiplexing
- **FOUR CHARACTER SIZES**
  7.6 mm, 10.9 mm, 14.2 mm, and 20.3 mm
- **CHOICE OF TWO COLORS**
  High Efficiency Red
  Yellow
- **EXCELLENT CHARACTER APPEARANCE**
  Evenly Lighted Segments
  Wide Viewing Angle
  Grey Body for Optimum Contrast
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW CATEGORIZED FOR COLOR**
  Use of Like Categories Yields a Uniform Display
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

The HDSP-3530/-3730/-5530/-3900 and HDSP-4030/-4130/-5730/-4200 are 7.6 mm, 10.9 mm/14.2 mm/20.3 mm high efficiency red and yellow displays designed for use in high light ambient condition. The four sizes of displays allow for viewing distances at 3, 6, 7, and 10 meters. These seven segment displays utilize large junction high efficiency LED chips made from GaAsP on a transparent GaP substrate. Due to the large junction area, these displays can be driven at high peak current levels needed for high ambient conditions or many character multiplexed operation.

These displays have industry standard packages, and pin configurations and ±1 overflow display are available in all four sizes. These numeric displays are ideal for applications such as Automotive and Avionic Instrumentation, Point of Sale Terminals, and Gas Pump.

Devices

Part No. HDSP-	Color	Description	Package Drawing
3530	High Efficiency Red	7.6 mm Common Anode Left Hand Decimal	A
3531		7.6 mm Common Anode Right Hand Decimal	B
3533		7.6 mm Common Cathode Right Hand Decimal	C
3536		7.6 mm Universal Overflow ±1 Right Hand Decimal	D
4030	Yellow	7.6 mm Common Anode Left Hand Decimal	A
4031		7.6 mm Common Anode Right Hand Decimal	B
4033		7.6 mm Common Cathode Right Hand Decimal	C
4036		7.6 mm Universal Overflow ±1 Right Hand Decimal	D

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagrams D and H.

Devices

Part No. HDSP	Color	Description	Package Drawing
3730	High Efficiency Red	10.9 mm Common Anode Left Hand Decimal	E
3731		10.9 mm Common Anode Right Hand Decimal	F
3733		10.9 mm Common Cathode Right Hand Decimal	G
3736		10.9 mm Universal Overflow ±1 Right Hand Dec.	H
4130	Yellow	10.9 mm Common Anode Left Hand Decimal	E
4131		10.9 mm Common Anode Right Hand Decimal	F
4133		10.9 mm Common Cathode Right Hand Decimal	G
4136		10.9 mm Universal Overflow ±1 Right Hand Dec.	H
5531	High Efficiency Red	14.2 mm Common Anode Right Hand Decimal	I
5533		14.2 mm Common Cathode Right Hand Decimal	J
5537		14.2 mm Overflow ±1 Common Anode	K
5538		14.2 mm Overflow ±1 Common Cathode	L
5731	Yellow	14.2 mm Common Anode Right Hand Decimal	I
5733		14.2 mm Common Cathode Right Hand Decimal	J
5737		14.2 mm Overflow ±1 Common Anode	K
5738		14.2 mm Overflow ±1 Common Cathode	L
3900	High Efficiency Red	20.3 mm Common Anode Left Hand Decimal	M
3901		20.3 mm Common Anode Right Hand Decimal	N
3903		20.3 mm Common Cathode Right Hand Decimal	O
3905		20.3 mm Common Cathode Left Hand Decimal	P
3906		20.3 mm Universal Overflow ±1 Right Hand Decimal	Q
4200	Yellow	20.3 mm Common Anode Left Hand Decimal	M
4201		20.3 mm Common Anode Right Hand Decimal	N
4203		20.3 mm Common Cathode Right Hand Decimal	O
4205		20.3 mm Common Cathode Left Hand Decimal	P
4206		20.3 mm Universal Overflow ±1 Right Hand Decimal	Q

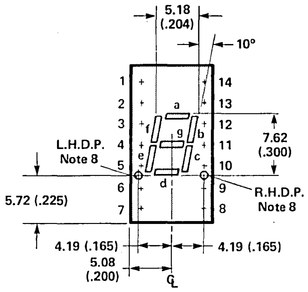
Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram Q.

Absolute Maximum Ratings (All Products)

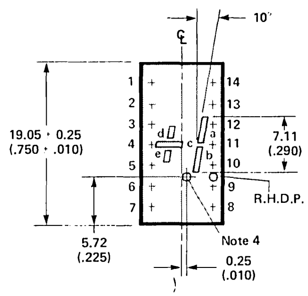
Average Power per Segment or DP ($T_A = 25°C$)	105 mW
Peak Forward Current per Segment or DP ($T_A = 25°C$)[1]	135 mA (Pulse Width = 0.16 ms)
DC Forward Current per Segment[2] or DP ($T_A = 25°C$)	40 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +100°C
Reverse Voltage per Segment or DP	3.0V
Lead Solder Temperature (1.59 mm [1/16 inch] below seating plane)	260°C for 3 sec.

Notes:
1. See Figure 1 to establish pulsed operating conditions.
2. Derate maximum DC current above $T_A = 25°C$ at .50 mA/°C per segment, see Figure 2.

Package Dimensions (HDSP-3530/4030 Series)

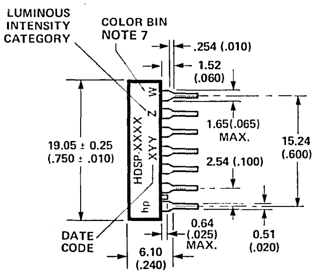


A,B,C

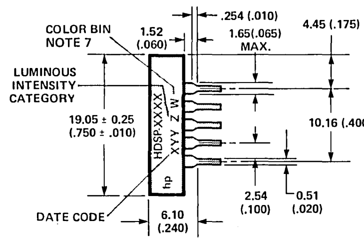


D

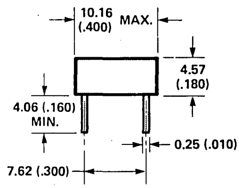
PIN	FUNCTION A -3530/-4030	B -3531/-4031	C -3533/-4033	D -3536/-4036
1	CATHODE-a	CATHODE-a	NO PIN	ANODE-d
2	CATHODE-f	CATHODE-f	CATHODE [6]	NO PIN
3	ANODE[3]	ANODE[3]	ANODE-f	CATHODE-d
4	NO PIN	NO PIN	ANODE-g	CATHODE-c
5	NO PIN	NO PIN	ANODE-e	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	ANODE-d	ANODE-e
7	CATHODE-e	CATHODE-e	NO PIN	ANODE-c
8	CATHODE-d	CATHODE-d	NO PIN	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	CATHODE[6]	NO PIN
10	CATHODE-c	CATHODE-c	ANODE-dp	CATHODE-dp
11	CATHODE-g	CATHODE-g	ANODE-c	CATHODE-b
12	NO PIN	NO PIN	ANODE-b	CATHODE-a
13	CATHODE-b	CATHODE-b	ANODE-a	ANODE-a
14	ANODE[3]	ANODE[3]	NO PIN	ANODE-b



A,B,D
SIDE

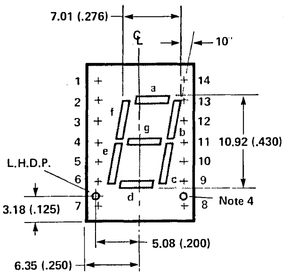


C
SIDE

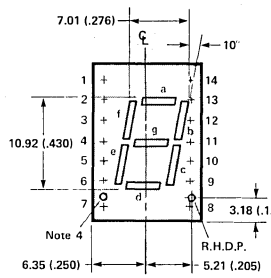


A,B,C,D
END

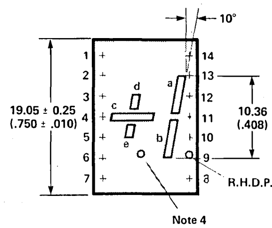
Package Dimensions (HDSP-3730/4130 Series)



E

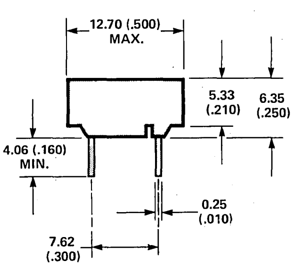


F,G

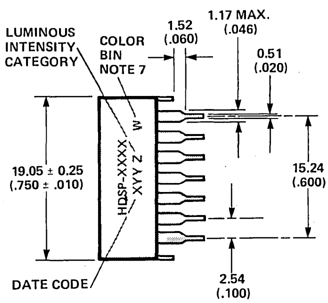


H

FRONT VIEW



END VIEW



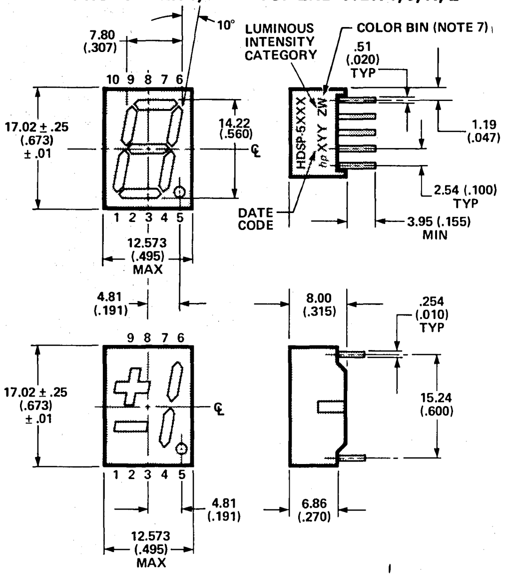
SIDE VIEW

PIN	FUNCTION E -3730/-4130	F -3731/-4131	G -3733/-4133	H -3736/-4136
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE-b

SOLID STATE DISPLAYS

Package Dimensions (5530/5730 Series)

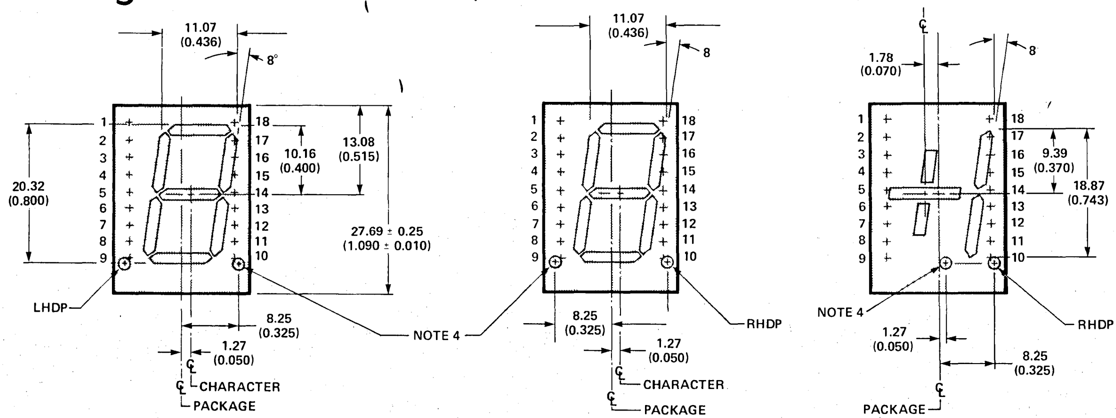
FRONT VIEW I, J   TOP END VIEW I, J, K, L



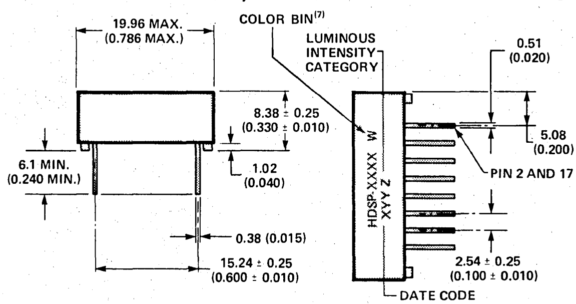
FRONT VIEW K, L   SIDE VIEW I, J, K, L

PIN	FUNCTION			
	I 5531	J 5533	K 5537	L 5538
1	CATHODE e	ANODE e	CATHODE c	ANODE c
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d
3	ANODE(3)	CATHODE(6)	CATHODE b	ANODE b
4	CATHODE c	ANODE c	ANODE a, b DP	CATHODE a, b, DP
5	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
6	CATHODE b	ANODE b	CATHODE a	ANODE a
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP
8	ANODE(3)	CATHODE(6)	ANODE c, d	CATHODE c, d
9	CATHODE f	ANODE f	CATHODE d	ANODE d
10	CATHODE g	ANODE g	NO PIN(5)	NO PIN(5)

Package Dimensions (3900/4200 Series)



FRONT VIEW M, P   FRONT VIEW N, O   FRONT VIEW Q



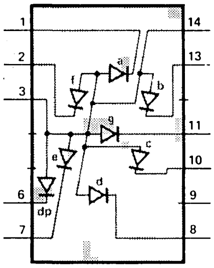
END VIEW M, N, O, P, Q   SIDE VIEW M, N, O, P, Q

Pin	Function				
	M 3900/4200	N 3901/4201	O 3903/4203	P 3905/4205	Q 3906/4206
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE(3)	ANODE(3)	CATHODE(6)	CATHODE(6)	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE(3)	ANODE(3)	CATHODE(6)	CATHODE(6)	CATHODE e
7	CATHODE dp	NO. CONNEC.	NO. CONNEC.	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE(3)	ANODE(3)	CATHODE(6)	CATHODE(6)	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE(3)	ANODE(3)	CATHODE(6)	CATHODE(6)	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

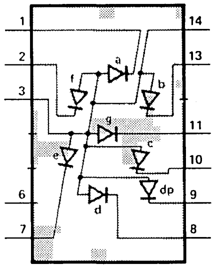
NOTES:

1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant Cathodes.
7. For HDSP-4030/-4130/-5730/-4200 Series product only.
8. See part number table for LHDP and RHDP designation.

Internal Circuit Diagram (HDSP-3530/4030 Series)



A



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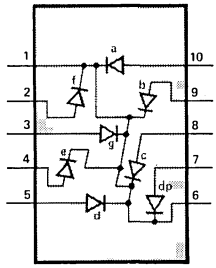

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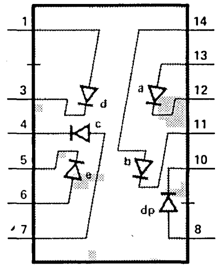
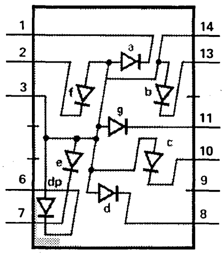


D

Internal Circuit Diagram (HDSP-3730/4130 Series)



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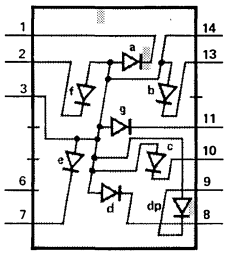

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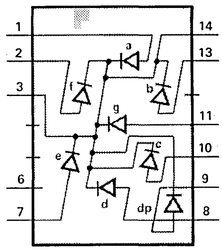
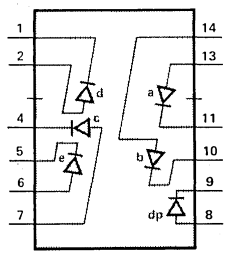
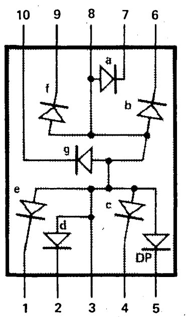


G

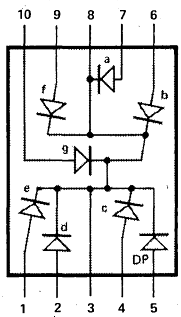


H

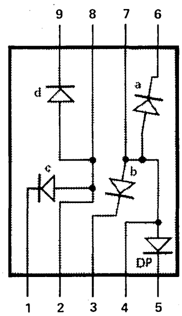
Internal Circuit Diagram (HDSP-5530/5730 Series)



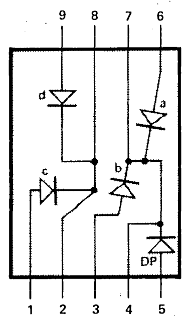
I



J



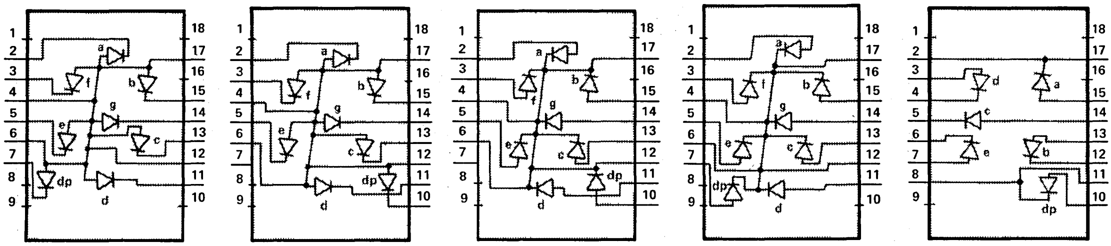
K



L

SOLID STATE DISPLAYS

Internal Circuit Diagram (HDSP-3900/4200 Series)



M N O P Q

Electrical/Optical Characteristics at $T_A = 25°C$

Parameter	Symbol	Device HDSP-	Test Condition	Min	Typ	Max	Units
Luminous Intensity/ Segment[9,10] (Digit Average)	I_V	3530 3730 5530 3900	100 mA Pk; 1 of 5 Duty Factor	2200 3350 2200 2200	7100 10860 6000 7000		μcd
		3530 3730 5530 3900	20 mA DC		4970 7600 5000 4800		μcd
		4030 4130 5730 4200	100 mA Pk; 1 of 5 Duty Factor	1500 1500 2200 2200	4500 5000 5500 7000		μcd
		4030 4130 5730 4200	20 mA DC		2200 2500 2800 3400		μcd
Peak Wavelength	λ_{PEAK}	3530/3730/ 5530/3900			635		nm
		4030/4130/ 5730/4200			583		nm
Dominant Wavelength[11, 12] (Digit Average)	λ_d	3530/3730/ 5530/3900			626		
		4030/4130/ 5730/4200		581.5	586	592.5	nm
Forward Voltage/Segment or D.P.[13]	V_F	All Devices	$I_F = 100$ mA		2.6	3.5	V
Reverse Voltage/Segment or D.P.[13, 14]	V_R	All Devices	$I_R = 100$ μA	3.0	25.0		V
Temp. Coeff. of V_F/Seg or D.P.	$\Delta V_F/°C$	All Devices	$I_F = 100$ mA		-1.1		mV/°C
Thermal Resistance LED Junction-to-pin	$R\theta_{J-PIN}$	3530/4030/ 3730/4130			282		°C/W/Seg
		5530/5730			345		°C/W/Seg
		3900/4200			375		°C/W/Seg

Notes:

9. Case temperature of the device immediately prior to the intensity measurement is 25°C.
10. The digits are categorized for luminous intensity with the intensity category designated by a letter on the side of the package.
11. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
12. The yellow displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
13. Quality level for electrical characteristics is 1000 parts per million.
14. Typical specification for reference only. Do not exceed absolute maximum ratings.

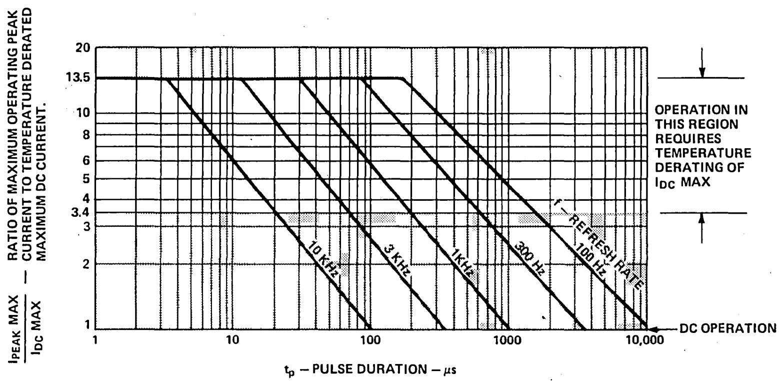


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration

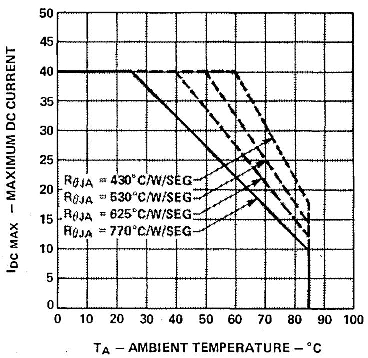


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature

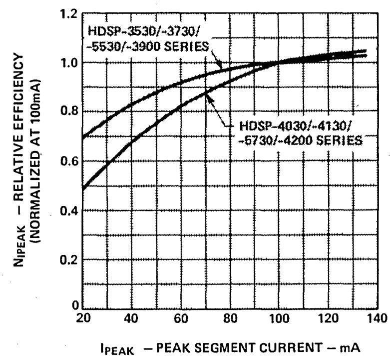


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

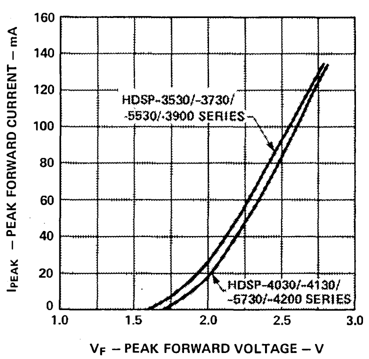


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage

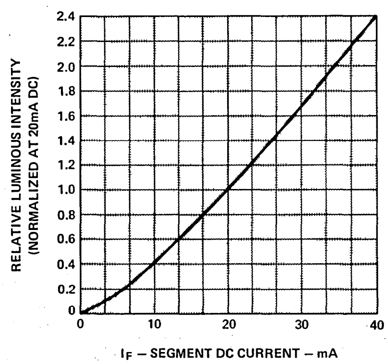


Figure 5. Relative Luminous Intensity vs. DC Forward Current

Electrical

These display devices are composed of eight light emitting diodes, with light from each LED optically stretched to form individual segments and a decimal point.

The devices utilize LED chips which are made from GaAsP on a transparent GaP substrate.

These display devices are designed for strobed operation. The typical forward voltage values, scaled from Figure 4 should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

$$V_F \text{ MAX} = 2.15\text{V} + I_{PEAK}\,(13.5\Omega)$$
For: $I_F \geq 30$ mA

$$V_F \text{ MAX} = 1.9\text{V} + I_{DC}\,(21.8\Omega)$$
For: $10 \text{ mA} \leq I_F \leq 30$ mA

Temperature derated strobed operating conditions are obtained from Figures 1 and 2. Figure 1 relates pulse duration (t_p), refresh rate (f), and the ratio of maximum peak current to maximum dc current (I_{PEAK} MAX/I_{DC} MAX). Figure 2 presents the maximum allowed dc current vs. ambient temperature. Figure 1 is based on the principle that the peak junction temperature for pulsed operation at a specified peak current, pulse duration and refresh rate should be the same as the junction temperature at maximum DC operation. Refresh rates of 1 kHz or faster minimize the pulsed junction heating effect of the device resulting in the maximum possible time average luminous intensity.

The time average luminous intensity can be calculated knowing the average forward current and relative efficiency characteristic, η_{IPEAK}, of Figure 3. Time average luminous intensity for a device case temperature of 25° C, I_V (25° C), is calculated as follows:

$$I_V\,(25°\,C) = \left[\frac{I_{AVG}}{20 \text{ mA}}\right] \left[\eta_{IPEAK}\right] \left[I_{V \text{ DATA SHEET}}\right]$$

Example: For HDSP-4030 series

$\eta_{IPEAK} = 1.00$ at $I_{PEAK} = 100$ mA. For DF = 1/5:

$$I_V\,(25°\,C) = \left[\frac{20 \text{ mA}}{20 \text{ mA}}\right] \left[1.00\right] \left[4.5 \text{ mcd}\right] = 4.5 \text{ mcd/segment}$$

The time average luminous intensity may be adjusted for operating junction temperature by the following exponential equation:

$$I_V\,(T_J) = I_V\,(25°\,C)\; e^{[k(T_J + 25°C)]}$$

where $T_J = T_A + P_D \cdot R\theta_{J-A}$

DEVICE	K
-3530/-3730/-5530/-3900	-0.0131/° C
-4030/-4130/-5730/-4200	-0.0112/° C

Mechanical

These devices are constructed utilizing a lead frame in a standard DIP package. The LED dice are attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, T_J MAX, is 105° C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit.

Worst case thermal resistance pin-to-ambient is 400° C/W/Seg when these devices are soldered into minimum trace width PC boards. When installed in a PC board that provides $R\theta_{PIN-A}$ less than 400° C/W/Seg these displays may be operated at higher average currents as shown in Figure 2.

Optical

The radiation pattern for these devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas.

$$L_V(\text{cd/m}^2) = \frac{I_V(\text{cd})}{A(\text{m}^2)}$$

$$L_V(\text{footlamberts}) = \frac{\pi I_V(\text{cd})}{A(\text{ft}^2)}$$

DEVICE	AREA/SEG. mm^2	AREA/SEG. $IN.^2$
-3530/-4030	2.5	.0039
-3730/-4130	4.4	.0068
-5530/-5730	8.8	.0137
-3900/-4200	14.9	.0231

Contrast Enhancement

The objective of contrast enhancement is to optimize display readability. Adequate contrast enhancement can be achieved in indoor applications through luminous contrast techniques. Luminous contrast is the observed brightness of the illuminated segment compared to the brightness of the surround. Appropriate wavelength filters maximize luminous contrast by reducing the amount of light reflected from the area around the display while transmitting most of the light emitted by the segment. These filters are described further in Application Note 1015.

Chrominance contrast can further improve display readability. Chrominance contrast refers to the color difference between the illuminated segment and the surrounding area. These displays are assembled with a gray package and untinted encapsulating epoxy in the segments to improve chrominance contrast of the ON segments. Additional contrast enhancement in bright ambients may be achieved by using a neutral density gray filter such as Panelgraphic Chromafilter Gray 10, or 3M Light Control Film (louvered film).

HEWLETT PACKARD

INTENSITY AND COLOR SELECTED DISPLAYS

TECHNICAL DATA JANUARY 1986

Features

- **INTENSITY SELECTION IMPROVES UNIFORMITY OF LIGHT OUTPUT FROM UNIT TO UNIT. AVAILABLE IN RED, HIGH EFFICIENCY RED, AND HIGH PERFORMANCE GREEN.**
- **COLOR SELECTION IMPROVES UNIFORMITY OF COLOR FROM UNIT TO UNIT. AVAILABLE IN YELLOW.**
- **TWO CATEGORY SELECTION SIMPLIFIES INVENTORY CONTROL AND ASSEMBLY.**

Description

Seven segment displays are now available from Hewlett-Packard which are selected from two categories. These select displays are basic catalog devices which are pre-sorted for luminous intensity and color then selected from two predetermined adjacent categories and assigned one convenient part number.

Example: Two luminous intensity categories are selected from the basic catalog 5082-7750 production distribution and assigned to the part number 5082-7750 option S02.

Luminous intensity selection is available for red, high efficiency red, and high performance green. Color selection is available for yellow.

To ensure our customers a steady supply of product, HP must offer selected units from the center of our distribution. If our production distribution shifts, we will need to change the intensity or color range of the selected units our customers receive. Typically, an intensity may have to be changed once every 1 to 3 years.

Current intensity and color selection information is available through a category reference chart which is available through your local field sales engineer or local franchised distributor.

Absolute Maximum Ratings and Electrical/Optical Characteristics

The absolute maximum ratings, mechanical dimensions, and electrical/optical characteristics are identical to the basic catalog device.

Device Selection Guide

The following table summarizes which basic catalog devices are available with category selection.

	COLOR					
Character Height	Red	High Efficiency Red	High Ambient High Efficiency Red	Yellow	High Ambient High Efficiency Yellow	High Performance Green
7.62 mm (0.3") Microbright	HDSP-7301 Option S02 HDSP-7303 Option S02 HDSP-7307 Option S02 HDSP-7308 Option S02	HDSP-7501 Option S02 HDSP-7503 Option S02 HDSP-7507 Option S02 HDSP-7508 Option S02	Basic Family Not Applicable	Selected Version Not Available	Basic Family Not Applicable	HDSP-7801 Option S02 HDSP-7803 Option S02 HDSP-7807 Option S02 HDSP-7808 Option S02
7.62 mm (0.3")	5082-7730 Option S02 5082-7731 Option S02 5082-7736 Option S02 5082-7740 Option S02	5082-7610 Option S02 5082-7611 Option S02 5082-7613 Option S02 5082-7616 Option S02	HDSP-3530 Option S02 HDSP-3531 Option S02 HDSP-3533 Option S02 HDSP-3536 Option S02	Selected Version Not Available	Selected Version Not Available	HDSP-3600 Option S02 HDSP-3603 Option S02 HDSP-3606 Option S02
10.92 mm (0.43")	5082-7750 Option S02 5082-7751 Option S02 5082-7756 Option S02 5082-7760 Option S02	5082-7650 Option S02 5082-7651 Option S02 5082-7653 Option S02 5082-7656 Option S02	HDSP-3730 Option S02 HDSP-3731 Option S02 HDSP-3733 Option S02 HDSP-3736 Option S02	5082-7663 Option S20 5082-7666 Option S20	HDSP-4133 Option S20 HDSP-4136 Option S20	Selected Version Not Available
14.2 mm (0.56") Single Digit	HDSP-5301 Option S02 HDSP-5303 Option S02 HDSP-5307 Option S02 HDSP-5308 Option S02	HDSP-5501 Option S02 HDSP-5503 Option S02 HDSP-5507 Option S02 HDSP-5508 Option S02	HDSP-5531 Option S02 HDSP-5533 Option S02 HDSP-5537 Option S02 HDSP-5538 Option S02	Selected Version Not Available	Selected Version Not Available	HDSP-5601 Option S02 HDSP-5607 Option S02
14.2 mm (0.56") Dual Digit	Selected Version Not Available	HDSP-5521 Option S02 HDSP-5523 Option S02	Basic Family Not Applicable	Selected Version Not Available	Basic Family Not Applicable	Selected Version Not Available
20 mm (0.8")	HDSP-3400 Option S02 HDSP-3403 Option S02 HDSP-3406 Option S02	Basic Family Not Applicable	HDSP-3900 Option S02 HDSP-3901 Option S02 HDSP-3903 Option S02 HDSP-3906 Option S02	Basic Family Not Applicable	Selected Version Not Available	Selected Version Not Available

Notes:
1. Option S02 designates a two intensity category selection.
2. Option S20 designates a two color category selection.
3. Option S02s of different part numbers may not have the same apparent brightness. Contact your HP Field Sales Office for design assistance.

SOLID STATE DISPLAYS

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC INDICATORS

5082-7300
5082-7302
5082-7304
5082-7340

TECHNICAL DATA JANUARY 1986

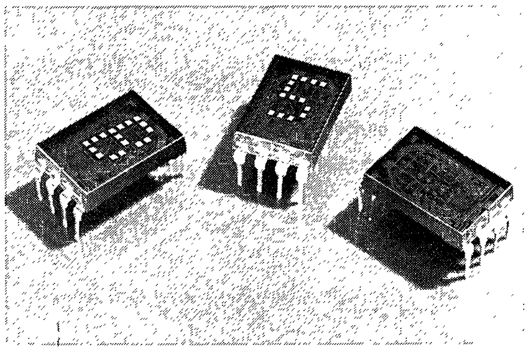
Features

- **NUMERIC 5082-7300/-7302**
  0-9, Test State, Minus Sign, Blank States
  Decimal Point
  7300 Right Hand D.P.
  7302 Left Hand D.P.
- **HEXADECIMAL 5082-7340**
  0-9, A-F, Base 16 Operation
  Blanking Control, Conserves Power
  No Decimal Point
- **DTL/TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH 5-BIT MEMORY**
  8421 Positive Logic Input
- **4 x 7 DOT MATRIX ARRAY**
  Shaped Character, Excellent Readibility
- **STANDARD DUAL-IN-LINE PACKAGE INCLUDING CONTRAST FILTER**
  15.2 mm x 10.2 mm (0.6 inch x 0.4 inch)
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category

Description

The HP 5082-7300 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide 7.4 mm (0.29 inch) displays for reliable, low-cost methods of displaying digital information.

The 5082-7300 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.



The 5082-7302 is the same as the 5082-7300, except that the decimal point is located on the left-hand side of the digit.

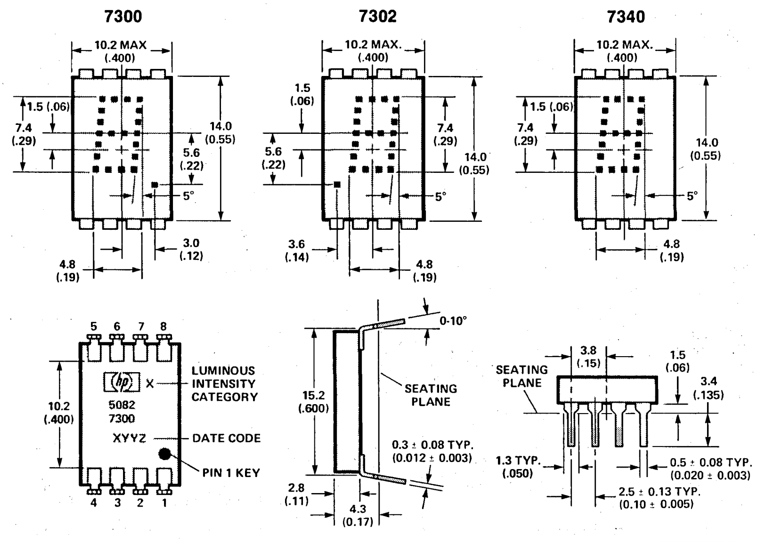
The 5082-7340 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7304 is a (±1) overrange display including a right-hand decimal point.

Applications

Typical applications include point-of-sale terminals, instrumentation, and computer system.

Package Dimensions



Pin	Function: 5082-7300 and 7302 Numeric	Function: 5082-7340 Hexadecimal
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal Point	Blanking Control
5	Latch Enable	Latch Enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

Notes:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±0.38 mm (± 0.015 inch).
3. Digit center line is ±0.25 mm (±0.01 inch) from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−40	+100	°C
Operating temperature, case (1,2)	T_C	−20	+85	°C
Supply voltage (3)	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input (7)	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; $t \leqslant 5$ seconds			230	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, case	T_C	-20		+85	°C
Enable Pulse Width	t_W	120			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_C = -20° C to +85° C, unless otherwise specified).

Description	Symbol	Test Conditions	Min.	Typ.(4)	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral 5 and dp lighted)		112	170	mA
Power dissipation	P_T			560	935	mW
Luminous intensity per LED (Digit average) (5,6)	I_v	V_{CC}=5.0V, T_C=25° C	32	70		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked (7)	V_{BL}				0.8	V
Blanking high-voltage; display blanked (7)	V_{BH}		3.5			V
Blanking low-level input current (7)	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			20	μA
Blanking high-level input current (7)	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			2.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+250	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+250	μA
Peak wavelength	λ_{PEAK}	T_C=25° C		655		nm
Dominant Wavelength (8)	λ_d	T_C=25° C		640		nm
Weight				0.8		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50° C/W; Θ_{JC}=15° C/W; 2. Θ_{CA} of a mounted display should not exceed 35° C/W for operation up to T_C = +85° C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_C=25° C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific case temperature, $I_V(T_C)$ may be calculated from this relationship: $I_V(T_C)=I_V\,(25° C)\,e^{[-.0188/°C\,(T_C-25°C)]}$ 7. Applies only to 7340. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

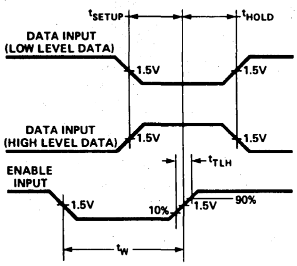


Figure 1. Timing Diagram of 5082-7300 Series Logic.

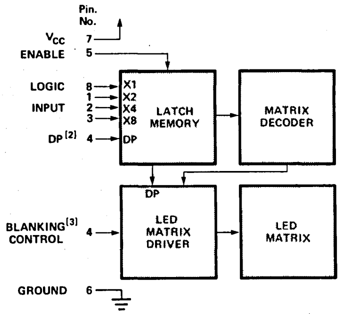


Figure 2. Block Diagram of 5082-7300 Series Logic.

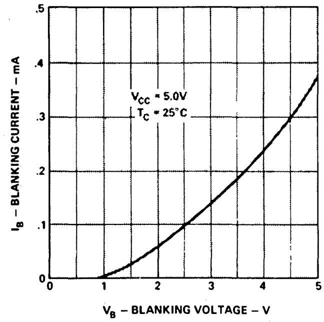


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7340.

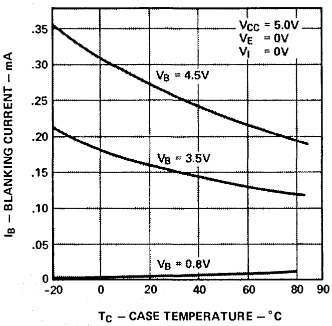


Figure 4. Typical Blanking Control Input Current vs. Temperature 5082-7340.

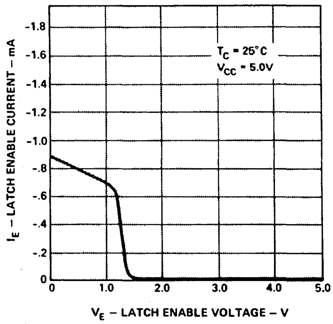


Figure 5. Typical Latch Enable Input Current vs. Voltage for the 5082-7300 Series Devices.

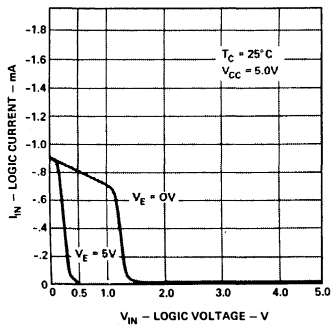


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage for the 5082-7300 Series Devices. Decimal Point Applies to 5082-7300 and -7302 Only.

TRUTH TABLE

BCD DATA[1]				5082-7300/7302	5082-7340
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	[illegible]	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	····	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

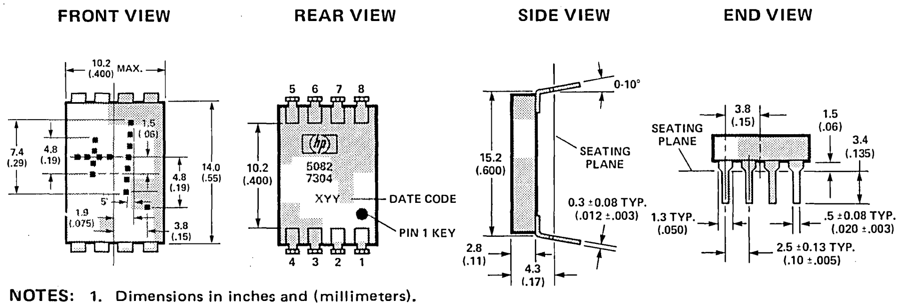
Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7300 and 5082-7302 displays.
3. The blanking control input, B, pertains only to the 5082-7340 hexadecimal display. Blanking input has no effect upon display memory.

Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7304 over range character is available. This display module comes in the same package as the 5082-7300 series numeric indicator and is completely compatible with it.

Package Dimensions



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

NOTES: 1. Dimensions in inches and (millimeters).
2. Unless otherwise specified, the tolerance on all dimensions is ±.015 inches. (± .38mm)

5082–7304

TRUTH TABLE FOR 5082-7304

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Fig. 7 cutoff.
H: Line switching transistor in Fig. 7 saturated.
X: 'don't care'

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Storage temperature, ambient	T_S	-40	+100	°C
Operating temperature, case	T_C	-20	+85	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to figure 7 for recommended resistor values.

TYPICAL DRIVING CIRCUIT FOR 5082-7304.

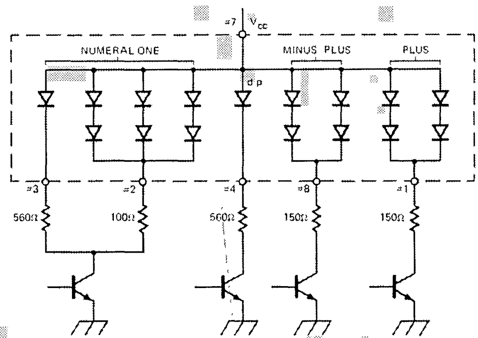


Figure 7.

Electrical/Optical Characteristics (T_C = -20°C TO +85°C, UNLESS OTHERWISE SPECIFIED)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		250	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	32	70		μcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λd	T_C = 25°C		640		nm
Weight				0.8		gm

SOLID STATE DISPLAYS

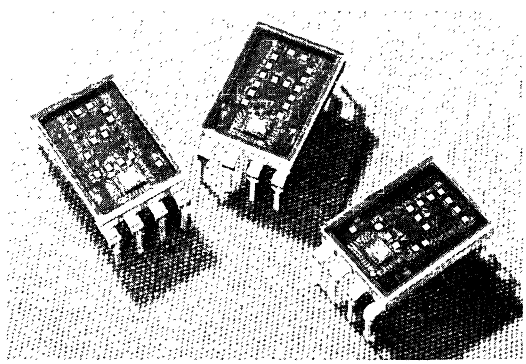
HEXADECIMAL AND NUMERIC DISPLAYS FOR INDUSTRIAL APPLICATIONS

5082-7356
5082-7357
5082-7358
5082-7359

TECHNICAL DATA JANUARY 1986

Features

- **CERAMIC/GLASS PACKAGE**
- **ADDED RELIABILITY**
- **NUMERIC 5082-7356/-7357**
  - **0-9, Test State, Minus Sign, Blank States**
  - **Decimal Point**
    - **7356 Right Hand D.P.**
    - **7357 Left Hand D.P.**
- **HEXADECIMAL 5082-7359**
  - **0-9, A-F, Base 16 Operation**
  - **Blanking Control, Conserves Power**
  - **No Decimal Point**
- **TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH 5 BIT MEMORY**
  - **8421 Positive Logic Input and Decimal Point**
- **4 x 7 DOT MATRIX ARRAY**
  - **Shaped Character, Excellent Readability**
- **STANDARD DUAL-IN-LINE PACKAGE**
  - **15.2mm x 10.2mm (.6 inch x .4 inch)**
- **CATEGORIZED FOR LUMINOUS INTENSITY**



Description

The HP 5082-7350 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide 7.4mm (0.29 inch) displays for use in adverse industrial environments.

The 5082-7356 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a " –" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.

The 5082-7357 is the same as the 5082-7356 except that the decimal point is located on the left-hand side of the digit.

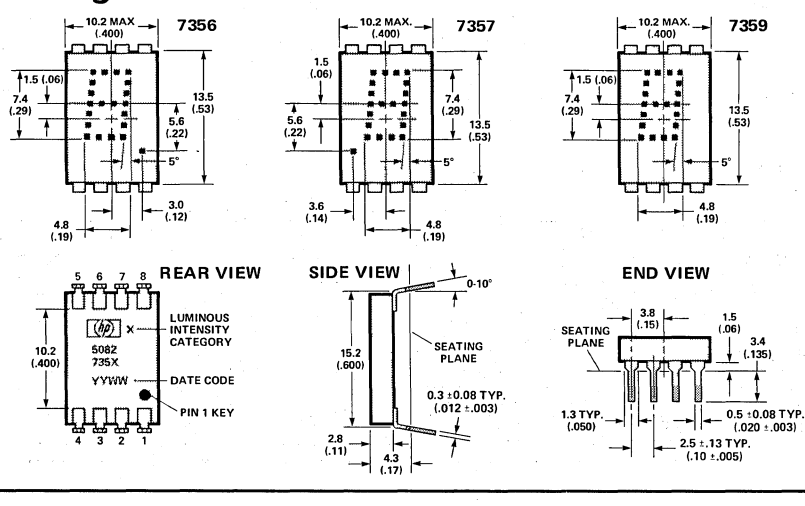
The 5082-7359 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7358 is a (±1) over range display including a right hand decimal point.

Applications

Typical applications include control systems, instrumentation, communication systems, and transportation equipment.

Package Dimensions



PIN	FUNCTION: 5082-7356 AND 7357 NUMERIC	FUNCTION: 5082-7359 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient	T_A	-20		+70	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_A = -20°C to +70°C, Unless Otherwise Specified)

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral 5 and dp lighted)		112	170	mA
Power dissipation	P_T			560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight				1.0		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50°C/W; Θ_{JC}=15°C/W; 2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 7359. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

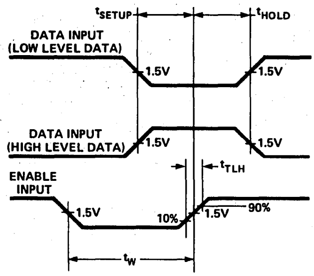


Figure 1. Timing Diagram of 5082-735X Series Logic.

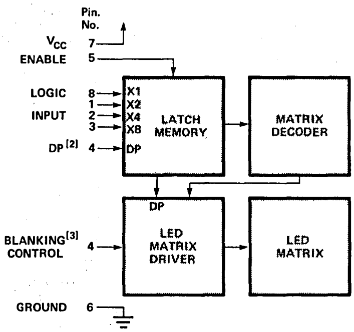


Figure 2. Block Diagram of 5082-735X Series Logic.

TRUTH TABLE					
BCD DATA[1]				5082-7356/7357	5082-7359
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	[illegible]	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	-	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7356 and 5082-7357 displays.
3. The blanking control input, B, pertains only to the 5082-7359 hexadecimal display. Blanking input has no effect upon display memory.

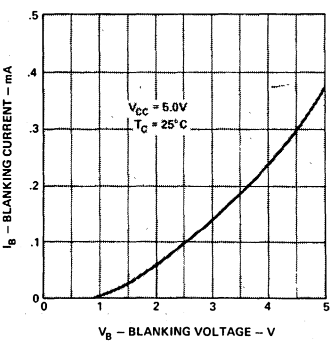


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7359.

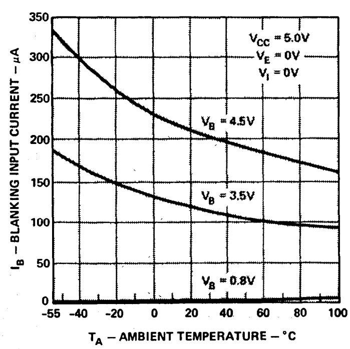


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 5082-7359.

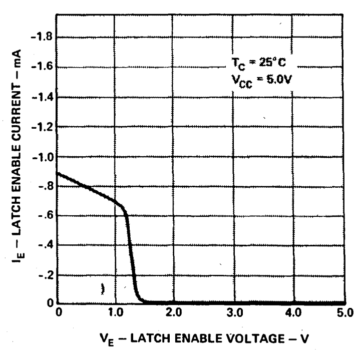


Figure 5. Typical Latch Enable Input Current vs. Voltage.

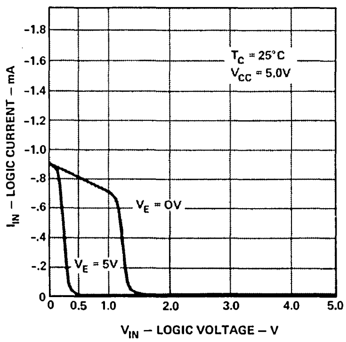


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

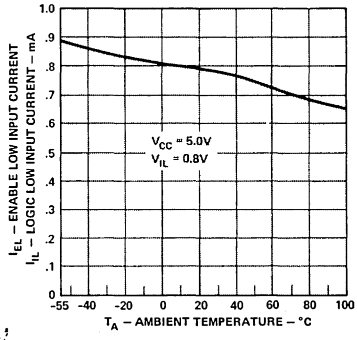


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

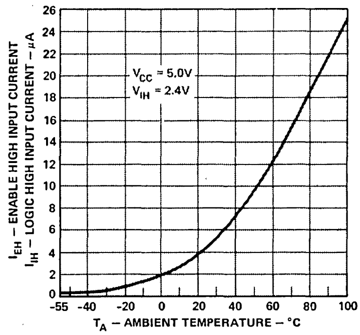


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 5082-735X series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 5082-7395 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as is the BCD data. The decimal point LED is driven by the on-board IC.

MECHANICAL

These displays are designed for use in adverse industrial environments.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

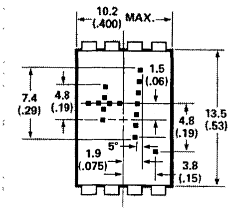
CONTRAST ENHANCEMENT

The 5082-735X displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

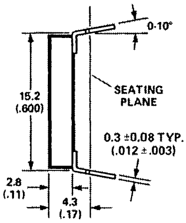
Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7358 over range character is available. This display module comes in the same package as the 5082-735X series numeric indicator and is completely compatible with it.

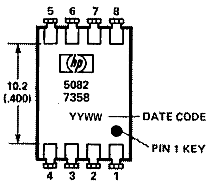
Package Dimensions



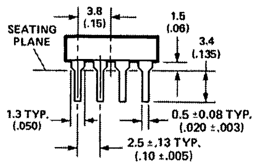
FRONT



SIDE



REAR



END

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

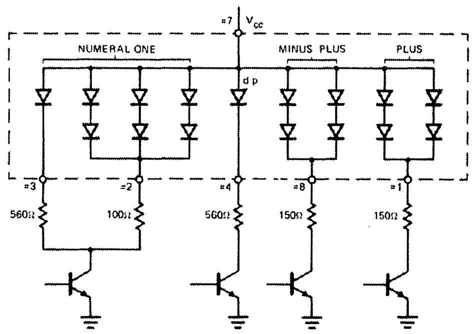


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics

5082-7358 (T_A = -20°C to 70°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		μcd
Peak wavelength	λpeak	T_C = 25°C		655		nm
Dominant Wavelength	λd	T_C = 25°C		640		nm
Weight				1.0		gm

Recommended Operating Conditions

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC DISPLAYS FOR INDUSTRIAL APPLICATIONS

HIGH EFFICIENCY RED

Low Power	HDSP-0760/0761/0762/0763
High Brightness	HDSP-0770/0771/0772/0763
YELLOW	HDSP-0860/0861/0862/0863
GREEN	HDSP-0960/0961/0962/0963

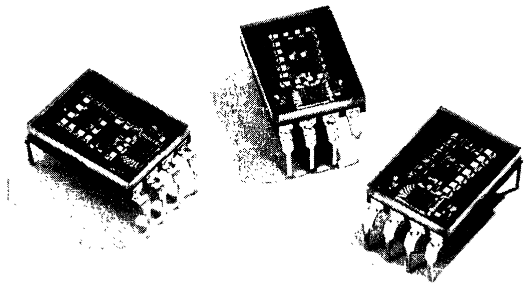
TECHNICAL DATA JANUARY 1986

Features

- **THREE COLORS**
  High-Efficiency Red
  Yellow
  High Performance Green
- **THREE CHARACTER OPTIONS**
  Numeric
  Hexadecimal
  Over Range
- **TWO HIGH-EFFICIENCY RED OPTIONS**
  Low Power
  High Brightness
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **MEMORY LATCH/DECODER/DRIVER**
  TTL Compatible
- **4x7 DOT MATRIX CHARACTER**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
- **YELLOW AND GREEN CATEGORIZED FOR COLOR**

Typical Applications

- **INDUSTRIAL EQUIPMENT**
- **COMPUTER PERIPHERALS**
- **INSTRUMENTATION**
- **TELECOMMUNICATION EQUIPMENT**



Description

These solid state display devices are designed and tested for use in adverse industrial environments. The character height is 7.4mm (0.29 inch). The numeric and hexadecimal devices incorporate an on-board IC that contains the data memory, decoder and display driver functions.

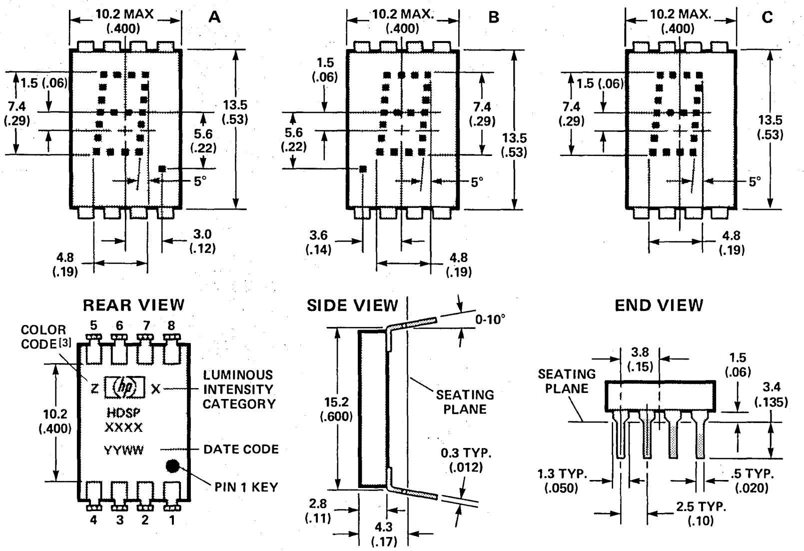
The numeric devices decode positive BCD logic into characters "0-9", a "—" sign, decimal point, and a test pattern. The hexadecimal devices decode positive BCD logic into 16 characters, "0-9, A-F". An input is provided on the hexadecimal devices to blank the display (all LED's off) without losing the contents of the memory.

The over range device displays "±1" and right hand decimal point and is typically driven via external switching transistors.

Devices

Part Number HDSP-	Color	Description	Front View
0760	High-Efficiency Red Low Power	Numeric, Right Hand DP	A
0761		Numeric, Left Hand DP	B
0762		Hexadecimal	C
0763		Over Range ±1	D
0770	High-Efficiency Red High Brightness	Numeric, Right Hand DP	A
0771		Numeric, Left Hand DP	B
0772		Hexadecimal	C
0763		Over Range ±1	D
0860	Yellow	Numeric, Right Hand DP	A
0861		Numeric, Left Hand DP	B
0862		Hexadecimal	C
0863		Over Range ±1	D
0960	Green	Numeric, Right Hand DP	A
0961		Numeric, Left Hand DP	B
0962		Hexadecimal	C
0963		Over Range ±1	D

Package Dimensions



PIN	FUNCTION: NUMERIC	FUNCTION: HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Vertical digit center line is ± .51mm (± .02") from vertical package center line.
3. HDSP-0860 and HDSP-0960 Series.

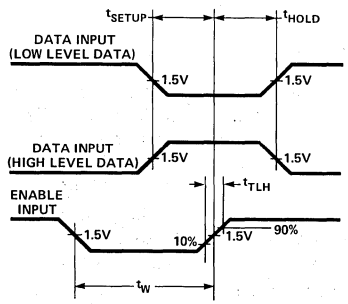


Figure 1. Timing Diagram

TRUTH TABLE					
BCD DATA[1] X_8	X_4	X_2	X_1	NUMERIC	HEXA-DECIMAL
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	[illegible]	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	····	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]		ON			V_{DP} = L
		OFF			V_{DP} = H
ENABLE[1]		LOAD DATA			V_E = L
		LATCH DATA			V_E = H
BLANKING[3]		DISPLAY-ON			V_B = L
		DISPLAY-OFF			V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels have no effect upon display memory, displayed character, or DP.
2. The decimal point input, DP, pertains only to the numeric displays.
3. The blanking control input, B, pertains only to the hexadecimal displays. Blanking input has no effect upon display memory.

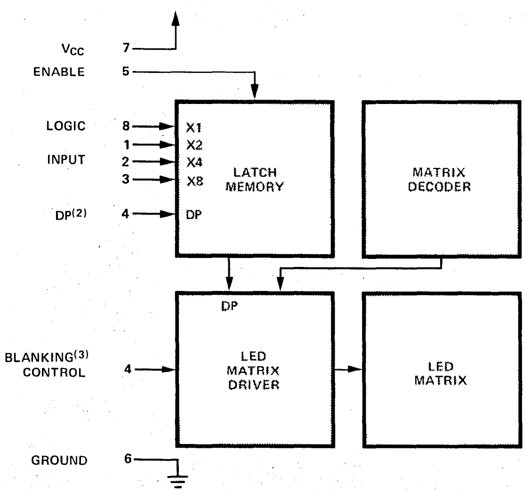


Figure 2. Logic Block Diagram

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+100	°C
Operating temperature, ambient [1]	T_A	−55	+70	°C
Supply voltage [2]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [2]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage [2]	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1]	T_A	-55		+70	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			1.0	msec

Optical Characteristics at $T_A = 25°C$, $V_{CC} = 5.0V$

Device	Description	Symbol	Min.	Typ.	Max.	Unit
HDSP-0760 Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	65	140		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength[5]	λ_d		626		nm
HDSP-0770 Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	260	620		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength[5]	λ_d		626		nm
HDSP-0860 Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	215	490		μcd
	Peak Wavelength	λ_{PEAK}		583		nm
	Dominant Wavelength[5,6]	λ_d		585		nm
HDSP-0960 Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	298	1100		μcd
	Peak Wavelength	λ_{PEAK}		568		nm
	Dominant Wavelength[5,6]	λ_d		574		nm

Notes:
1. The nominal thermal resistance of a display mounted in a socket that is soldered onto a printed circuit board is $R\theta_{JA} = 50°C/W$/device. The device package thermal resistance is $R\theta_{J\text{-}PIN} = 15°C/W$/device. The thermal resistance device pin-to-ambient through the PC board should not exceed 35° C/W/device for operation at $T_A = +70°C$.
2. Voltage values are with respect to device ground, pin 6.
3. These displays are categorized for luminous intensity with the intensity category designated by a letter code located on the back of the display package. Case temperature of the device immediately prior to the light measurement is equal to 25° C.

SOLID STATE DISPLAYS

Electrical Characteristics; $T_A = 0°C$ to $+70°C$

Description		Symbol	Test Conditions	Min.	Typ.[7]	Max.	Unit
Supply Current	HDSP-0760 Series	I_{CC}	$V_{CC} = 5.5V$ (Numeral 5 and DP Illuminated)		78	105	mA
	HDSP-0770 Series HDSP-0860 Series HDSP-0960 Series				120	175	
Power Dissipation	HDSP-0760 Series	P_T	$V_{CC} = 5.5V$ (Numeral 5 and DP Illuminated)		390	573	mW
	HDSP-0770 Series HDSP-0860 Series HDSP-0960 Series				690	963	
Logic, Enable and Blanking Low-Level Input Voltage		V_{IL}	$V_{CC} = 4.5V$			0.8	V
Logic, Enable and Blanking High-Level Input Voltage		V_{IH}		2.0			V
Logic and Enable Low-Level Input Current		I_{IL}	$V_{CC} = 5.5V$			-1.6	mA
Blanking Low-Level Input Current		I_{BL}	$V_{IL} = 0.4V$			-10	μA
Logic, Enable and Blanking High-Level Input Current		I_{IH}	$V_{CC} = 5.5V$ $V_{IH} = 2.4V$			+40	μA
Weight					1.0		gm
Leak Rate						$5x10^{-8}$	cc/sec

Notes:

4. The luminous intensity at a specific operating ambient temperature, $I_V(T_A)$ may be approximated from the following expotential equation: $I_V(T_A = I_V(25°C)\ e^{[k(T_A - 25°C)]}$.

Device	K
HDSP-0760 Series HDSP-0770 Series	-0.0131/° C
HDSP-0860 Series	-0.0112/° C
HDSP-0960 Series	-0.0104/° C

5. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
6. The HDSP-0860 and HDSP-0960 series devices are categorized as to dominant wavelength with the category designated by a number on the back side of the display package.
7. All typical values at $V_{CC} = 5.0V$ and $T_A = 25°C$.

Operational Considerations

ELECTRICAL

These devices use a modified 4 x 7 dot matrix of light emitting diode to display decimal/hexadecimal numeric information. The high efficiency red and yellow LED's are GaAsP epitaxial layer on a GaP transparent substrate. The green LED's are GaP epitaxial layer on a GaP transparent substrate. The LED's are driven by constant current drivers, BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7 MHz rate.

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The blanking control input on the hexadecimal displays blanks (turns off) the displayed information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 2.0 volts. When blanked, the display standby power is nominally 250 mW at $T_A = 25°C$.

MECHANICAL

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +70° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C watt/device as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixutres formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

CONTRAST ENHANCEMENT

These display devices are designed to provide an optimum ON/OFF contrast when placed behind an appropriate contrast enhancement filter. The following filters are suggested:

HIGH EFFICIENCY RED

Panelgraphic Ruby Red 60
Chequers Red 112
3M Light Control Film

YELLOW

Panelgraphic Yellow 27
Chequers Amber 107
3M Light Control Film

GREEN

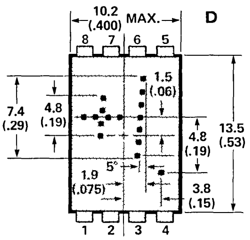
Panelgraphic Green 48
Chequers Green 107
3M Light Control Film

For many applications a neutral density gray filter in either plastic, circular polarizer or optically coated glass will provide the needed contrast enhancement. Suggested plastic neutral density gray filters are Panelgraphic Gray 10, Chequers Gray 105, or Polaroid HNCP37. The optically coated glass/circular polarized HNCP10 filter by Polaroid provides superior contrast enhancement for very bright ambients.

Over Range Character

The over range devices display "±1" and decimal point. The character height and package configuration are the same as the numeric and hexadecimal devices. Character selection is obtained via external switching transistors and current limiting resistors.

Package Dimensions



FRONT VIEW

Pin	Function
1	Plus
2	Numeral One
3	Numeral One
4	DP.
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

Note:
1. Dimensions in millimetres and (inches).

Character	Pin			
	1	2,3	4	8
+	1	X	X	1
—	0	X	X	1
1	X	1	X	X
Decimal Point	X	X	1	X
Blank	0	0	0	0

Notes:
0: Line switching transistor in Figure 7 cutoff.
1: Line switching transistor in Figure 7 saturated.
X: 'don't care'

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	-65	+100	°C
Operating Temperature Ambient	T_A	-55	+70	°C
Forward Current, Each LED	I_F		10	mA
Reverse Voltage, Each LED	V_R		5	V

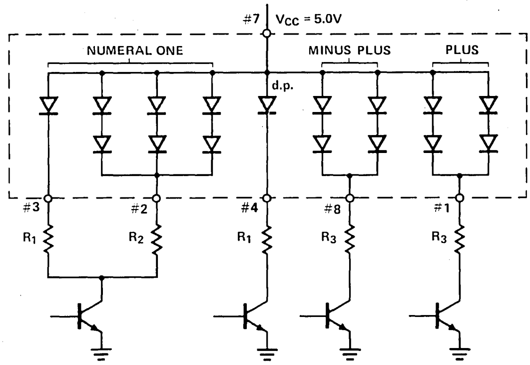


Figure 3. Typical Driving Circuit

Recommended Operating Conditions $V_{CC} = 5.0V$

Device		Forward Current Per LED, mA	Resistor Value		
			R_1	R_2	R_3
HDSP-0763	Low Power	2.3	1300	200	300
HDSP-0763	High Brightness	8	360	47	68
HDSP-0863		8	360	36	56
HDSP-0963		8	360	30	43

Luminous Intensity Per LED

(Digit Average)[3,4] at $T_A = 25°C$

Device	Test Conditions	Min.	Typ.	Units
HDSP-0763	$I_F = 2.3$ mA	65	140	μcd
	$I_F = 8$ mA		620	μcd
HDSP-0863	$I_F = 8$ mA	215	490	μcd
HDSP-0963	$I_F = 8$ mA	298	1100	μcd

Electrical Characteristics; $T_A = 0°C$ to $+70°C$

Device	Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
HDSP-0763	Power Dissipation (all LED's Illuminated)	P_T	$I_F = 2.8$ mA		72		mW
			$I_F = 8$ mA		224	282	
	Forward Voltage per LED	V_F	$I_F = 2.8$ mA		1.6		V
			$I_F = 8$ mA		1.75	2.2	
HDSP-0863	Power Dissipation (all LED's Illuminated)	P_T	$I_F = 8$ mA		237	282	mW
	Forward Voltage per LED	V_F			1.90	2.2	V
HDSP-0963	Power Dissipation (all LED's Illuminated)	P_T	$I_F = 8$ mA		243	282	mW
	Forward Voltage per LED	V_F			1.85	2.2	V

HEWLETT PACKARD

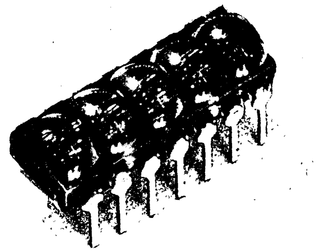
LEADFRAME MOUNTED SEVEN SEGMENT MONOLITHIC NUMERIC INDICATORS

5082-7400/7430 SERIES

TECHNICAL DATA JANUARY 1986

Features

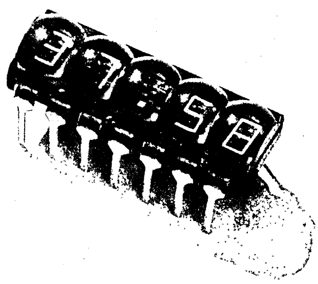
- **COMPACT PACKAGE SIZES**
  .25" Package Width
  .150" and .200" Digit Spacing
- **STROBED OPERATION**
  Minimizes Lead Connections
- **FULLY ENCAPSULATED STANDARD DIP PACKAGES**
  End Stackable
  Integral Red Filter
  Extremely Rugged Construction
- **I.C. COMPATIBLE**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures uniformity of light output from unit to unit within single category.



Description

The HP 5082-7400/-7430 series are 2.79 mm (.11"), seven segment GaAsP numeric indicators packaged in 2, 3, 4 and 5 digit clusters. An integral magnification technique increases the luminous intensity, thereby making low power consumption possible. Options include either the standard lower right hand decimal point or a centered decimal point.

Applications include mobile telephones, hand held calculators, portable instruments and many other products requiring compact, rugged, long lifetime active indicators.



Device Selection Guide

Digits per Cluster	Configuration Device	Inter-Digit Spacing mm (inches)	Part Number Center Decimal Point	Part Number Right Decimal Point
2 (right)		5.08 (.200)		5082-7432
3		5.08 (.200)		5082-7433
4		3.81 (.150)	5082-7404	5082-7414
5		3.81 (.150)	5082-7405	5082-7415

SOLID STATE DISPLAYS

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500 μs) 5082-7432/7433	I_{PEAK}		50	mA
Peak Forward Current per Segment or dp (Duration < 1 msec) 5082-7404/7405/7414/7415	I_{PEAK}		110	mA
Average Current per Segment or dp	I_{AVG}		5	mA
Power Dissipation per Digit[1]	P_D		80	mW
Operating Temperature, Ambient	T_A	-40	75	°C
Storage Temperature	T_S	-40	100	°C
Reverse Voltage	V_R		5	V
Solder Temperature 1/16" below seating plane (t ≤ 3 sec)[2]			230	°C

Notes: 1. Derate linearly @ 1 mW/°C above 25°C ambient.
2. See Mechanical section for recommended flux removal solvents.

Electrical/Optical Characteristics at T_A = 25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp[3,4] 5082-7432/7433	I_V	I_{AVG} = 500 μA (I_{PK} = 5 mA duty cycle = 10%)	10	40		μcd
Luminous Intensity/Segment or dp[3,4] (Time Averaged) 5082-7404/7405/7414/7415	I_V	I_{AVG} = 1 mA I_{PK} = 10 mA duty cycle = 10%)	5	20		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Forward Voltage/Segment or dp 5082-7432/-7433	V_F	I_F = 5 mA		1.55	2.0	V
Forward Voltage/Segment or dp 5082-7404/7405/7414/7415	V_F	I_F = 10 mA		1.55	2.0	V
Reverse Voltage/Segment or dp	V_R	I_R = 200 μA	5			V
Rise and Fall Time[5]	t_r, t_f			10		ns

NOTES:
3. The digits are categorized for luminous intensity. Intensity categories are designated by a letter located on the back side of the package.
4. Each character of the display is matched for luminous intensity at the test conditions shown. Operation of the display at lower peak currents may cause intensity mismatch within the display. Operation at peak currents less than 5.0 mA may cause objectionable display segment matching.
5. Time for a 10%-90% change of light intensity for step change in current.

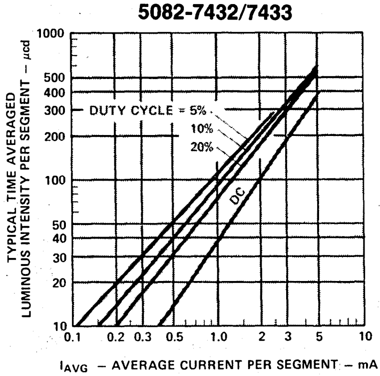


Figure 1. Typical Time Averaged Luminous Intensity per Segment (Digit Average) vs. Current per Segment.

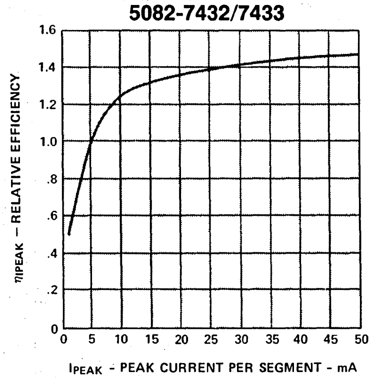


Figure 2. Relative Luminous Efficiency vs. Peak Current per Segment.

5082-7404/7405/7414/7415

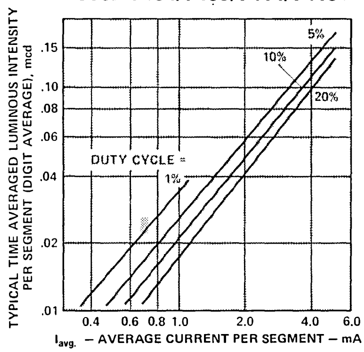


Figure 3. Typical Time Averaged Luminous Intensity per Segment (Digit Average) vs. Average Current per Segment.

5082-7404/7405/7414/7415

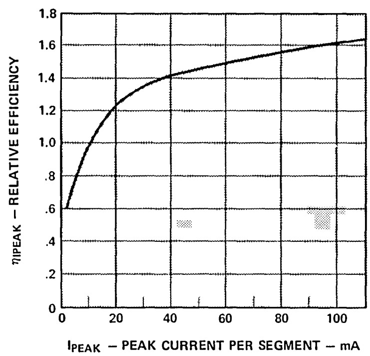


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment.

5082-7400/7430 SERIES

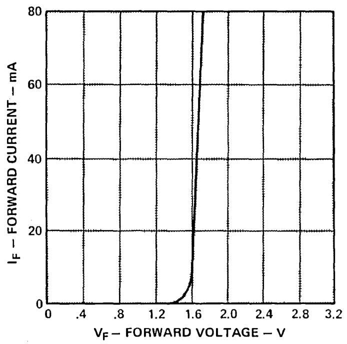


Figure 5. Forward Current vs. Forward Voltage.

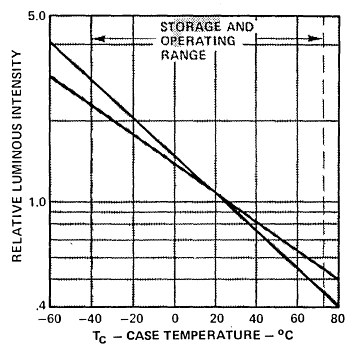


Figure 6. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

Electrical/Optical

The 5082-7400/7430 series devices utilize a monolithic GaAsP chip of 8 common cathode segments for each display digit. The segment anodes of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under an integrally molded lens giving a magnified character height of 2.79mm (0.11) inches. Satisfactory viewing will be realized within an angle of ±30° for the 7404/7405/7414/7415 and ±20° for the 7432/7433, measured from the center line of the digit.

The decimal point in the 7432, 7433, 7414, and 7415 displays is located at the lower right of the digit for conventional driving schemes.

The 5082-7404 and 7405 displays contain a centrally located decimal point which is activated in place of a digit. In long registers, this technique of setting off the decimal point significantly improves the display's readability. With respect to timing, the decimal point is treated as a separate character with its own unique time frame.

To improve display contrast, the plastic incorporates a red dye that absorbs strongly at all visible wavelengths except the 655 nm emitted by the LED. An additional filter, such as Plexiglass 2423, Panelgraphic 60 or 63, and SGL Homalite 100-1605, will further lower the ambient reflectance and improve display contrast.

Mechanical

The 5082-7400/7430 series package is a standard 12 or 14 Pin DIP consisting of a plastic encapsulated lead frame with integral molded lenses. It is designed for plugging into DIP sockets or soldering into PC boards. The lead frame construction allows use of standard DIP insertion tools and techniques. Alignment problems are simplified due to the clustering of digits in a single package. The shoulders of the lead frame pins are intentionally raised above the bottom of the package to allow tilt mounting of up to 20° from the PC board.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°C) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

SOLID STATE DISPLAYS

Package Description 5082-7404, -7405, -7414, -7415

Notes: 6. Dimensions in millimeters and (inches).
7. Tolerances on all dimension are ±.38 mm (±.015 in.) unless otherwise noted.

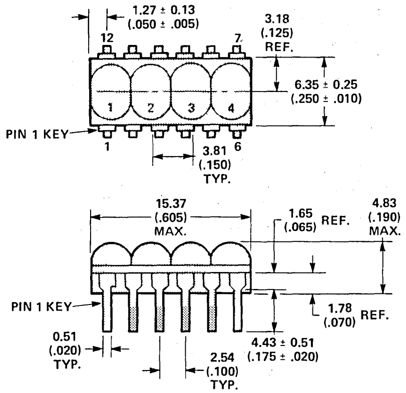


Figure 7. 5082-7404/7414

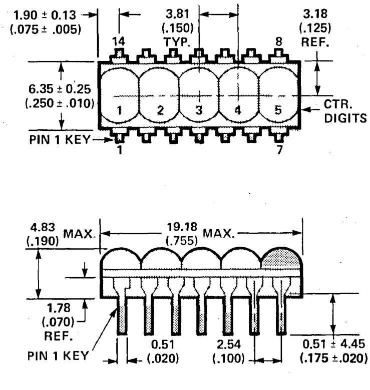


Figure 8. 5082-7405/7415.

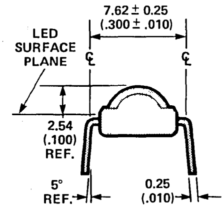


Figure 9. 5082-7404/7405/7414/7415

Magnified Character Font Description

DIMENSIONS IN MILLIMETERS AND (INCHES).

DEVICES
5082-7404
5082-7405

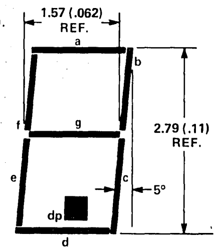


Figure 10. Center Decimal Point Configuration

DIMENSIONS IN MILLIMETERS AND (INCHES).

DEVICES
5082-7414
5082-7415

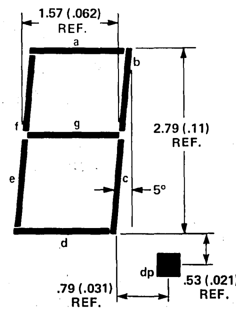


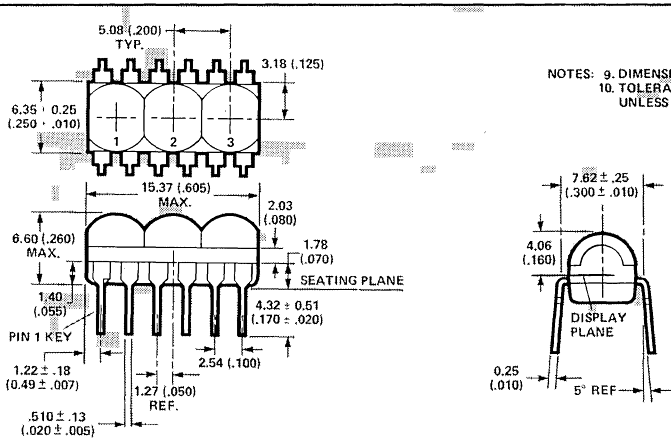
Figure 11. Right Decimal Point Configuration

Device Pin Description

PIN NO.	5082-7404/7414 FUNCTION	5082-7405/7415 FUNCTION
1	CATHODE 1	CATHODE 1
2	ANODE e	ANODE e
3	ANODE c	ANODE c
4	CATHODE 3	CATHODE 3
5	ANODE dp	ANODE dp
6	CATHODE 4	ANODE d
7	ANODE g	CATHODE 5
8	ANODE d	ANODE g
9	ANODE f	CATHODE 4
10	CATHODE 2	ANODE f
11	ANODE b	SEE NOTE 8
12	ANODE a	ANODE b
13	—	CATHODE 2
14	—	ANODE a

Note 8: Leave Pin Unconnected.

Package Description 5082-7432, -7433

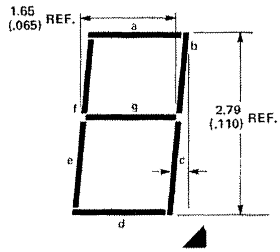


NOTES: 9. DIMENSIONS IN MILLIMETERS AND (INCHES).
10. TOLERANCES ON ALL DIMENSIONS ARE 0.038 ±(.015) UNLESS OTHERWISE SPECIFIED.

Figure 11.

Magnified Character Font Description

DEVICES
5082-7432
5082-7433



DIMENSIONS IN MILLIMETERS AND (INCHES).

Figure 12.

Device Pin Description

PIN NUMBER	5082-7432 FUNCTION	5082-7433 FUNCTION
1	SEE NOTE 11.	CATHODE 1
2	ANODE e	ANODE e
3	ANODE d	ANODE d
4	CATHODE 2	CATHODE 2
5	ANODE c	ANODE c
6	ANODE dp	ANODE dp
7	CATHODE 3	CATHODE 3
8	ANODE b	ANODE b
9	ANODE g	ANODE g
10	ANODE a	ANODE a
11	ANODE f	ANODE f
12	SEE NOTE 11.	SEE NOTE 11.

NOTE 11. Leave Pin unconnected.

SOLID STATE DISPLAYS

HEWLETT PACKARD

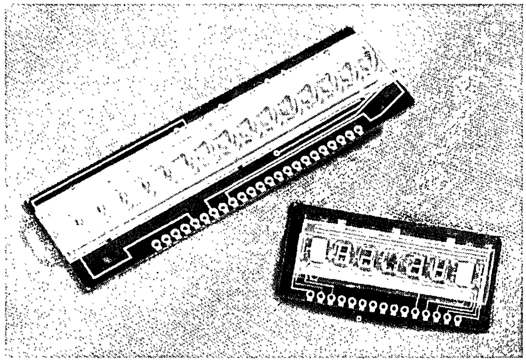
PRINTED CIRCUIT BOARD MOUNTED SEVEN SEGMENT NUMERIC INDICATORS

5082-7200/7440 SERIES

TECHNICAL DATA JANUARY 1986

Features

- MOS COMPATIBLE
- AVAILABLE IN 9 TO 16 DIGIT CONFIGURATIONS
- CHARACTER HEIGHTS OF .105", .115" AND .175"
- LOW POWER
- CATEGORIZED FOR LUMINOUS INTENSITY



Description

The HP-5082-7200/7440 series of displays are seven segment GaAsP Numeric Indicators mounted on printed circuit boards. A plastic lens magnifies the digits and includes an integral protective bezel. Character heights of .105" (2.67 mm), .115" (2.92 mm) and .175" (4.45 mm) are available. For large quantity applications, digit string lengths of 8, 12 and 14 digits are available by special order.

Applications are hand held calculators and portable equipment requiring compact, low power, long life time, active displays.

Device Selection Guide

Part Number	Digits Per PC Board	Decimal Point	Package	Character Height (mm) in.	Inter-Digit Spacing (mm) in.
5082-7441	9	Right Hand	Fig. 9	(2.67) .105"	(5.08) .200"
5082-7446	16	Right Hand	Fig. 11	(2.92) .115"	(3.81) .150"
5082-7285	5	Right Hand	Fig. 14	(4.45) .175"	(5.84) .230"
5082-7295	15	Right Hand	Fig. 13	(4.45) .175"	(5.84) .230"

Maximum Ratings 5082-7441/7446

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp[1]	I_{AVG}		3	mA
Power Dissipation per Digit [2]	P_D		50	mW
Operating Temperature, Ambient	T_A	-20	+85	°C
Storage Temperature	T_S	-20	+85	°C
Reverse Voltage	V_R		3	V
Solder Temperature at connector edge (t≤3 sec.)[3]			230	°C

NOTES: 1. Derate linearly at 0.1mA/°C above 60°C ambient.
2. Derate linearly at 1.7mW/°C above 60°C ambient.
3. See Mechanical section for recommended soldering techniques and flux removal solvents.

Maximum Ratings 5082-7285/7295

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or DP (Duration <35μs)	I_{PEAK}		200	mA
Average Current per Segment or DP (4)	I_{AVG}		7	mA
Power Dissipation per Digit (5)	P_D		125	mW
Operating Temperature, Ambient	T_A	-20	+70	°C
Storage Temperature	T_S	-20	+80	°C
Reverse Voltage	V_R		3	V
Solder Temperature at connector edge (t≤3 sec.) (6)			230	°C

NOTES: 4. Derate linearly at 0.12mA/°C above 25°C ambient.
5. Derate linearly at 2.3mW/°C above 25°C ambient.
6. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A = 25°C 5082-7441/7446

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp[7] 5082-7441	I_V	I_{AVG} = 500μA (I_{PK} = 5mA duty cycle = 10%)	9	40		μcd
5082-7446		5mA Peak 1/16 Duty Cycle	7	35		μcd
Peak Wavelength	λ_{peak}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 5mA		1.55		V

NOTES:
7. Each character of the display is matched for luminous intensity at the test conditions shown. Operation of the display at lower peak currents may cause intensity mismatch within the display. Operation at peak currents less than 3.5 mA may cause objectionable display segment matching.

SOLID STATE DISPLAYS

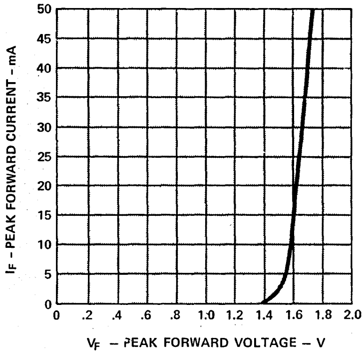


Figure 1. Peak Forward Current vs. Peak Forward Voltage.

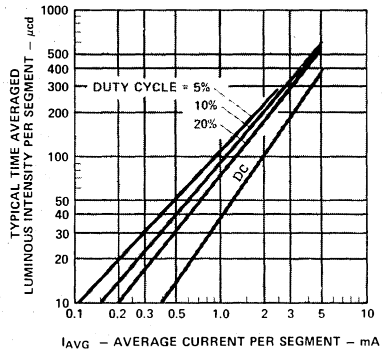


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment.

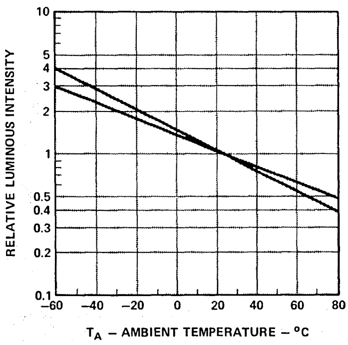


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level.

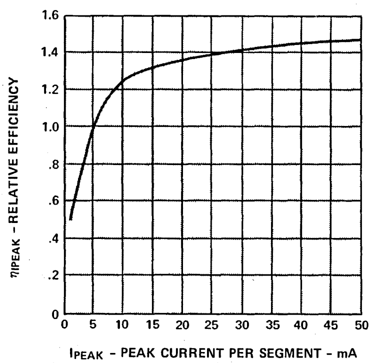


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment.

Electrical/Optical Characteristics at T_A=25°C 5082-7285/7295

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp (Time Averaged) 15 digit display 5082-7295[8,10]	I_v	$I_{avg.}$ = 2 mA (30 mA Peak 1/15 duty cycle)	30	90		μcd
Luminous Intensity/Segment or dp (Time Averaged) 5 digit display 5082-7285[8,10]	I_v	$I_{avg.}$ = 2 mA (10 mA Peak 1/5 duty cycle)	30	70		μcd
Forward Voltage per Segment or dp 5082-7295 15 digit display	V_F	I_F = 30 mA		1.60	2.3	V
Forward Voltage per Segment or dp 5082-7285 5 digit display	V_F	I_F = 10 mA		1.55	2.0	V
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[9]	λ_d			640		nm
Reverse Current per Segment or dp	I_R	V_R = 5V		10		μA
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$			-2.0		mV/°C

NOTES:

8. The luminous intensity at a specific ambient temperature, $I_V (T_A)$, may be calculated from this relationship: $I_V(T_A) = I_{V(25°C)} (.985)^{(T_A - 25°C)}$.
9. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and represents the single wavelength which defines the color of the device.
10. Each character of the display is matched for luminous intensity at the test conditions shown. Operation of the display at lower peak currents may cause intensity mismatch within the display. Operation at peak currents less than 6.0 mA may cause objectionable display segment matching.

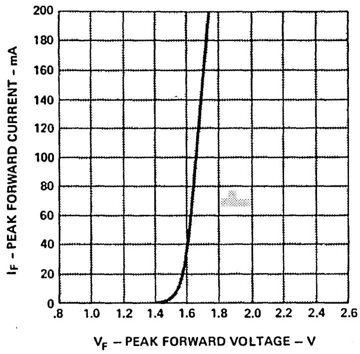


Figure 5. Peak Forward Current vs. Peak Forward Voltage.

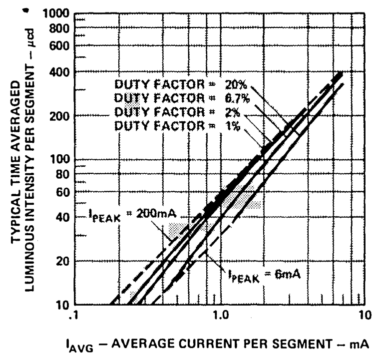


Figure 6. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment.

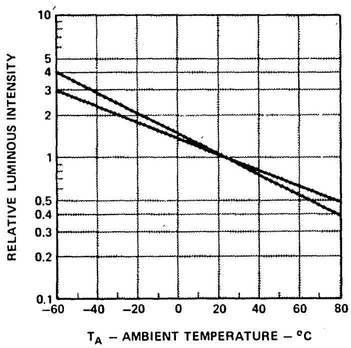


Figure 7. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level.

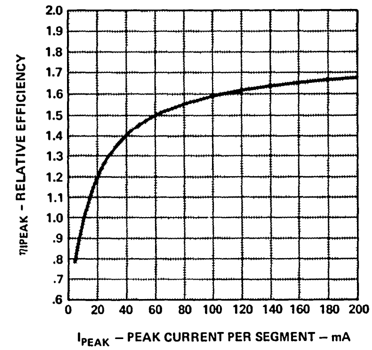


Figure 8. Relative Luminous Efficiency vs. Peak Current per Segment.

SOLID STATE DISPLAYS

Mechanical

These devices are constructed on a standard printed circuit board substrate. A separately molded plastic lens is attached to the PC board over the digits. The lens is an acrylic styrene material that gives good optical lens performance, but is subject to scratching so care should be exercised in handling.

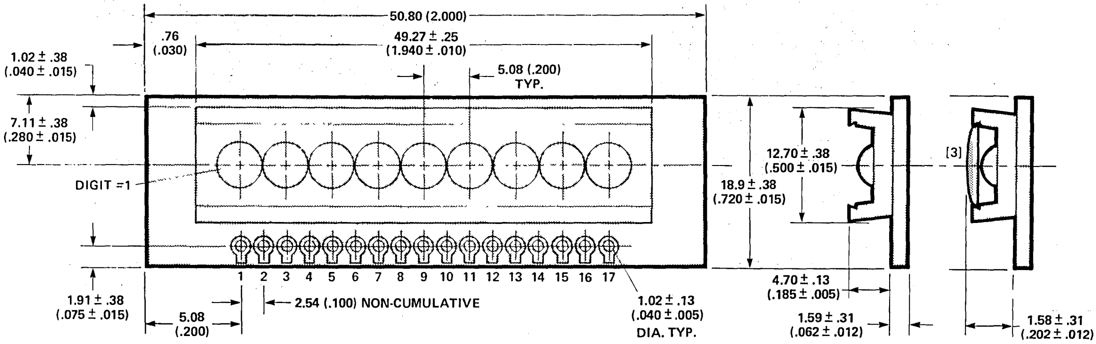
The device may be mounted either by use of pins which may be hand soldered into the plated through holes at the connector edge of the PC board or by insertion into a standard PC board connector. The devices may be hand soldered for up to 3 seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the display. It is recommended that a non-activated rosin core wire solder or a low temperature deactivating flux and solid wire solder be used in soldering operations.

The PC board is silver plated. To prevent the formation of a tarnish (Ag_2S) which could impair solderability the displays should be stored in the unopened shipping packages until they are used. Further information on the storage, handling, and cleaning of silver plated components is contained in Hewlett-Packard Application Bulletin No. 3.

Electrical/Optical

The HP 5082-7441, -7446, -7285 and 7295 devices utilize a monolithic GaAsP chip containing 7 segments and a decimal point for each display digit. The segments of each digit are interconnected, forming an 8 by N line array, where N is the number of digits in the display. Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character. Satisfactory viewing will be realized within an angle of approximately ±20° from the centerline of the digit. A filter, such as plexiglass 2423, Panelgraphic 60 or 63, and Homalite 100-1600, will lower the ambient reflectance and improve display contrast. Digit encoding of these devices is performed by standard 7 segment decoder driver circuits.

Package Dimensions

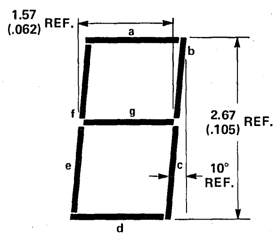


NOTES: 1. Dimensions in millimeters and (inches).
2. Logo and part number are on back of package.
3. Secondary 1.25X magnifier that slides into primary lens and increases character height to 3.33 (.131) available as special product.
4. Tolerances: ±.88 (.015)

Figure 9. 5082-7441

Magnified Character Font Description

5082-7441



Note: All dimensions in millimeters and (inches).

Figure 10.

Device Pin Description

Pin No.	5082-7441 Function	Pin No.	5082-7441 Function
1	Dig. 1 Cathode	10	Seg. d Anode
2	Seg. c Anode	11	Dig. 6 Cathode
3	Dig. 2 Cathode	12	Seg. g Anode
4	d.p. Anode	13	Dig. 7 Cathode
5	Dig. 3 Cathode	14	Seg. b Anode
6	Seg. a Anode	15	Dig. 8 Cathode
7	Dig. 4 Cathode	16	Seg. f Anode
8	Seg. e Anode	17	Dig. 9 Cathode
9	Dig. 5 Cathode		

Package Dimensions

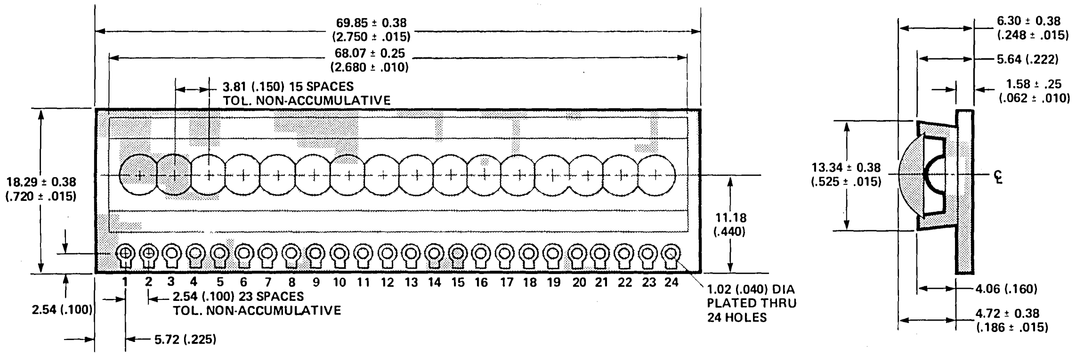
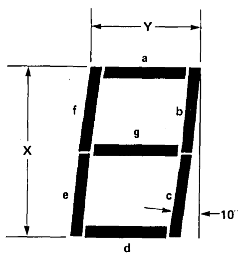


Figure 11. 5082-7446

Magnified Character Font Description



DEVICE	X	Y
5082-7446	2.92 (.115)	1.40 (.055)

NOTES: 1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. TOLERANCES ON ALL DIMENSIONS ARE ±0.38 (.015) UNLESS OTHERWISE SPECIFIED.

Figure 12.

Device Pin Description

Pin No.	5082-7446 Function
1	Cathode-Digit 1
2	Cathode-Digit 2
3	Cathode-Digit 3
4	Cathode-Digit 4
5	Cathode-Digit 5
6	Anode-Segment e
7	Cathode-Digit 6
8	Anode-Segment d
9	Cathode-Digit 7
10	Anode-Segment a
11	Cathode-Digit 8
12	Anode-Segment DP
13	Cathode-Digit 9
14	Anode-Segment c
15	Cathode-Digit 10
16	Anode-Segment g
17	Cathode-Digit 11
18	Anode-Segment b
19	Cathode-Digit 12
20	Anode-Segment f
21	Cathode-Digit 13
22	Cathode-Digit 14
23	Cathode-Digit 15
24	Cathode-Digit 16

Package Dimensions

ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

TOLERANCES ARE ±0.20 (±.008) UNLESS OTHERWISE NOTED

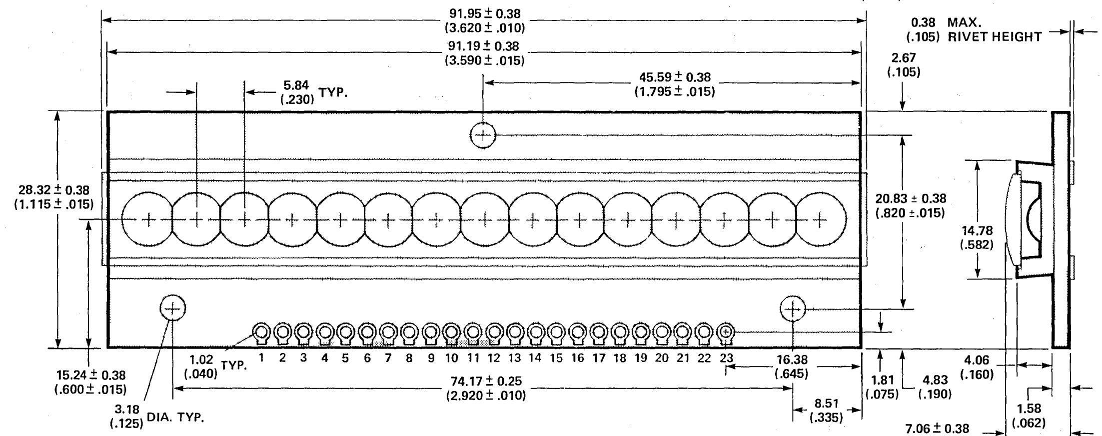
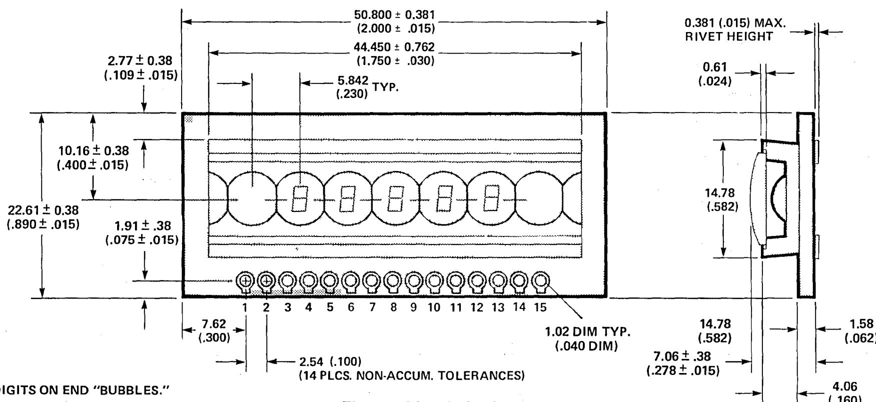


Figure 13. 5082-7295



NOTE: NO DIGITS ON END "BUBBLES."

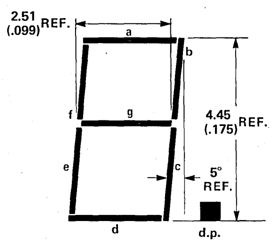
Figure 14. 5082-7285

Magnified Character Font Description

DEVICES

5082-7285

5082-7295



ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

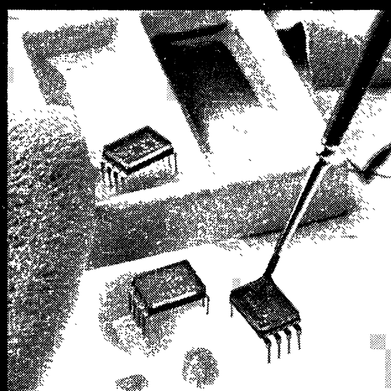
Figure 15.

Device Pin Description

Pin No.	5082-7285 Function	5082-7295 Function
1	Anode Segment b	Cathode Digit 1
2	Anode Segment g	Cathode Digit 2
3	Anode Segment e	Cathode Digit 3
4	No Connection	Cathode Digit 4
5	Cathode Digit 2	Anode Segment dp
6	Cathode Digit 3	Cathode Digit 5
7	Cathode Digit 4	Anode Segment c
8	Cathode Digit 5	Cathode Digit 6
9	Cathode Digit 6	Anode Segment e
10	No Connection	Cathode Digit 7
11	Anode Segment dp	Anode Segment a
12	Anode Segment d	Cathode Digit 8
13	Anode Segment c	Anode Segment g
14	Anode Segment a	Cathode Digit 9
15	Anode Segment f	Anode Segment d
16		Cathode Digit 10
17		Anode Segment f
18		Cathode Digit 11
19		Anode Segment b
20		Cathode Digit 12
21		Cathode Digit 13
22		Cathode Digit 14
23		Cathode Digit 15

[redacted]

8. High Reliability/ Hermetic Components



High Reliability

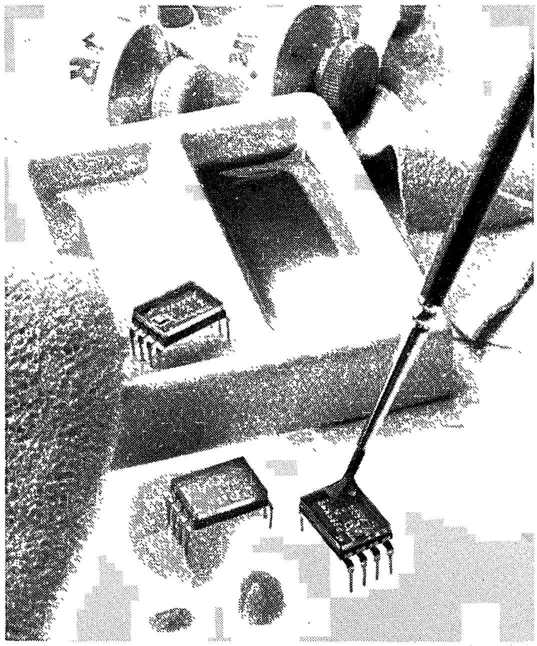
Hewlett-Packard has supplied specially tested high reliability optoelectronic products since 1968 for use in state-of-the-art commercial, military, and aerospace applications. To meet the requirements of high reliability, products must be designed with rugged capabilities to withstand severe levels of environmental stress and exposure without failure. We have accomplished this objective by designing a unique family of hermetic products including lamps, displays, and optocouplers which have proven their merits in numerous advanced space and defense programs in the international marketplace.

These products receive reliability screening and qualification tests in accordance with appropriate reliability programs similar to those of MIL-S-19500, MIL-D-87157 and MIL-STD-883. HP supplies JAN and JANTX LED indicators and optocouplers in compliance with DESC selected item drawings and parts with HP standard military equipment screening programs for optocouplers and displays.

Reliability programs are also performed to individual customer control drawings and specifications when needed. Some of these special testing programs are very complex and may include Class S requirements for microcircuits.

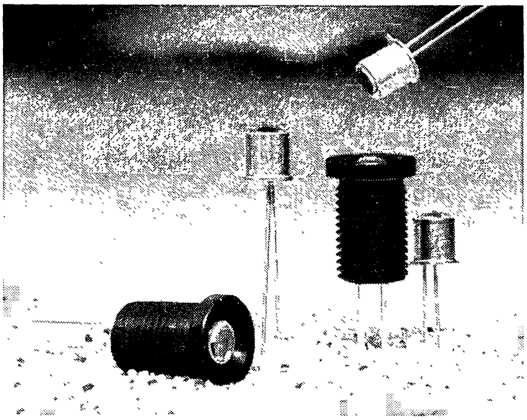
HP's optoelectronic epoxy encapsulated products are designed for long life applications where non-man rated or ground support requirements allow their use. As with hermetic products, the capabilities of epoxy parts can be enhanced by 100% screening and conditioning tests. Lot capabilities can be confirmed by acceptance qualification test programs. MIL-D-87157 is used to define the military requirements for plastic LED indicators and displays.

All testing is done by experienced Hewlett-Packard employees using facilities which are approved by DESC for JAN products and by customer inspection for special programs. Environmental equipment capabilities and operating methods of the test laboratory meet MIL-STD-750 or MIL-STD-883 procedures.



High Reliability Optoelectronic Products

Hewlett-Packard offers the broadest line of high reliability, solid state display products. They are specially designed to withstand severe environmental stress and exposure without failure. This unique product group includes lamps, integrated numeric and hexadecimal displays, and 5 x 7 dot matrix alphanumeric displays.



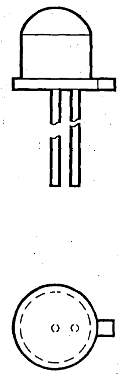
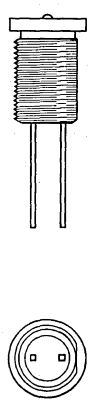
The hermetically sealed, solid state lamps are listed on the Qualified Parts List (QPL) of MIL-S-19500, and are supplied as either standard JAN or JANTX devices. There are four colors: standard red, high efficiency red, yellow, and green; and each color is also available in a panel mountable fixture.

Products meeting the hermeticity requirement of MIL-D-87157 include the integrated numeric and hexadecimal displays and 5 x 7 dot matrix alphanumeric displays. Hewlett-Packard offers two in-house high reliability testing programs, TXV and TXVB. The TXVB program is in conformance with Quality Level A of MIL-D-87157 with qualification and with 100% screening test. The TXV program is a modification of Quality Level A of MIL-D-87157 with 100% screening only. Detailed testing programs for TXV and TXVB are given in the individual data sheets.

The integrated numeric and hexadecimal displays with on-board decoder/driver and memory, are hermetically sealed, and have a character height of 7.4 mm (0.29 inch). They are available in standard red; low power, high efficiency red; high brightness, high efficiency red; and yellow. These displays are designed and tested for use in military and aerospace applications.

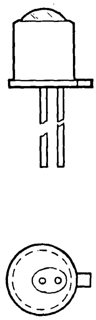
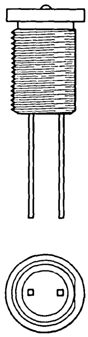
The 5 x 7 dot matrix alphanumeric displays with extended temperature range capabilities are available in three character heights: 3.8 mm (0.15 inch), 5 mm (0.2 inch), and 6.9 mm (0.27 inch). In addition, these displays are available in several colors: standard red, high efficiency red, and yellow. The 5 mm (0.2 inch) and 6.9 mm (0.27 inch) versions have the additional features of having a solder-glass seal and an even wider operating temperature range than the 3.8 mm (0.15 inch) package. This wide variety of character heights and colors makes these products ideal for a variety of applications in avionics, industrial controls, and instrumentation.

Hermetically Sealed and High Reliability LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	1N5765 JAN1N5765[4] JANTX1N5765[4]	Red (640 nm)	Hermetic/ TO-46[3]	Red Diffused	1.0 mcd @ 20 mA	70°	1.6 V @ 20 mA	8-18
	1N6092 JAN1N6092[4] JANTX1N6092[4]	High Efficiency Red (626 nm)			5.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6093 JAN1N6093[4] JANTX1N6093[4]	Yellow (585 nm)		Yellow Diffused				
	1N6094 JAN1N6094[4] JANTX1N6094[4]	Green (572 nm)		Green Diffused	3.0 mcd @ 25 mA		2.1 V @ 25 mA	
	HLMP-0904 HLMP-0930 HLMP-0931	Red (640 nm)	Panel Mount Version	Red Diffused	1.0 mcd @ 20 mA		1.6 V @ 20 mA	
	HLMP-0354 JANM19500/51901 JTXM19500/51902	High Efficiency Red (626 nm)			5.0 mcd @ 20 mA		2.0 V @ 20 mA	
	HLMP-0454 JANM19500/52001 JTXM19500/52002	Yellow (585 nm)		Yellow Diffused				
	HLMP-0554 JANM19500/52101 JTXM19500/52102	Green (572 nm)		Green Diffused	3.0 mcd @ 25 mA		2.1 V @ 25 mA	

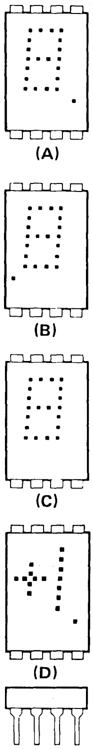
NOTES:
1. Θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Dominant Wavelength.
3. PC Board Mountable.
4. Military Approved and qualified for High Reliability Applications.

Hermetically Sealed and High Reliability LED Lamps (cont.)

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-0363 HLMP-0391 HLMP-0392	High Efficiency Red (626 nm)	Hermetic TO-18[3]	Clear Class	50 mcd @ 20 mA	18	2.0 V @ 20 mA	8-24
	HLMP-0463 HLMP-0491 HLMP-0492	Yellow (585 nm)			50 mcd @ 20 mA		2.0 V @ 20 mA	
	HLMP-0563 HLMP-0591 HLMP-0592	Green (572 nm)			50 mcd @ 25 mA		2.1 V @ 25 mA	
	HLMP-0364 HLMP-0365 HLMP-0366	High Efficiency Red (626 nm)	Panel Mount Version	Clear Glass	50 mcd @ 20 mA		2.0 V @ 20 mA	
	HLMP-0464 HLMP-0465 HLMP-0466	Yellow (585 nm)			50 mcd @ 25 mA		2.0 V @ 20 mA	
	HLMP-0564 HLMP-0565 HLMP-0566	Green (572 nm)			50 mcd @ 25 mA		2.1 V @ 25 mA	

NOTES:
1. Θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Dominant Wavelength.
3. PC Board Mountable.
4. Military Approved and qualified for High Reliability Applications.

Hermetic Hexadecimal and Numeric Dot Matrix Displays



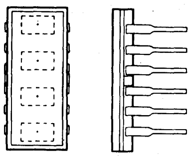
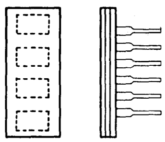
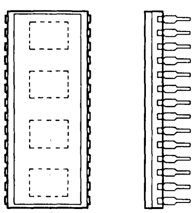
Device		Description	Package	Application	Page No.
7.4 mm (.29") 4 x 7 Single Digit Package: 8 Pin Glass Ceramic 15.2mm (.6") DIP Truly Hermetic	4N51 4N51TXV M87157/00101ACX[1] (4N51TXVB) (A)	Numeric RHDP Decoder/Driver/Memory TXV — Hi Rel Screened	8 Pin Hermetic Built-in 15.2 mm (.6") DIP with gold plated leads	• Military High Reliability Applications • Avionics/Space Flight Systems • Fire Control Systems • Ground Support, Shipboard Equipment	8-30
	4N52 4N52TXV M87157/00102ACX[1] (4N52TXVB) (B)	Numeric LHDP Built-in Decoder/Driver/Memory TXV — Hi Rel Screened			
	4N54 4N54TXV M87157/00103ACX[1] (4N54TXVB) (C)	Hexadecimal Built-in Decoder/Driver/Memory TXV — Hi Rel Screened			
	4N53 4N53TXV M87157/00103ACX[1] (4N53TXVB) (D)	Character Plus/Minus Sign TXV — Hi Rel Screened			
	HDSP-0781 (A) HDSP-0781 TXV HDSP-0781 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	High Efficiency Red, Low Power	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	8-38
	HDSP-0782 (B) HDSP-0782 TXV HDSP-0782 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0783 (D) HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0784 (C) HDSP-0784 TXV HDSP-0784 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0791 (A) HDSP-0791 TXV HDSP-0791 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	High Efficiency Red, High Brightness	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	
	HDSP-0792 (B) HDSP-0792 TXV HDSP-0792 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			

[1] Military Approved and Qualified for High Reliability Applications.

Hermetic Hexadecimal and Numeric Dot Matrix Displays (cont.)

Device		Description	Color	Application	Page No.
(See previous page)	HDSP-0783 (D) HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	High Efficiency Red, High Brightness	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	8-38
	HDSP-0794 (C) HDSP-0794 TXV HDSP-0794 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0881 (A) HDSP-0881 TXV HDSP-0881 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	Yellow		
	HDSP-0882 (B) HDSP-0882 TXV HDSP-0882 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0883 (D) HDSP-0883 TXV HDSP-0883 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			
	HDSP-0884 (C) HDSP-0884 TXV HDSP-0884 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157			

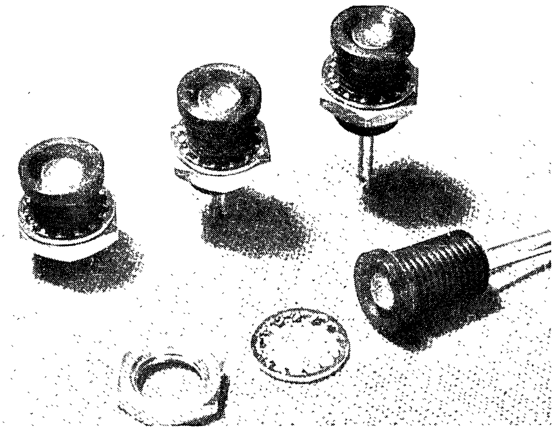
Hermetic Alphanumeric Displays

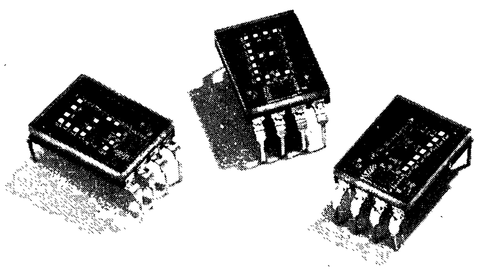
Device		Description	Color	Application	Page No.
	HDSP-2010 HDSP-2010 TXV HDSP-2010 TXVB	3.7 mm (.15") 5 x 7 Four Character Alphanumeric Operating Temperature Range: -40°C to +85°C TXV Hi Rel Screened TXVB Hi Rel Screened to Level A MIL-D-87157	Red, Red Glass Contrast Filter	• Extended temperature applications requiring high reliability. • I/O Terminals • Avionics For further information see Application Note 1016.	8-46
	HDSP-2310 HDSP-2310 TXV HDSP-2310 TXVB	5.0 mm (.20") 5 x 7 Four Character Alphanumeric 12 Pin Ceramic 6.35 mm (.25") DIP with untinted glass lens Operating Temperature Range: -55°C to +85°C True Hermetic Seal TXV — Hi Rel Screened TXVB — Hi Rel Screened to Level A MIL-D-87157	Standard Red	• Military Equipment • Avionics • High Rel Industrial Equipment	8-52
	HDSP-2311 HDSP-2311 TXV HDSP-2311 TXVB		Yellow		
	HDSP-2312 HDSP-2312 TXV HDSP-2312 TXVB		High Eff. Red		
	HDSP-2450 HDSP-2450 TXV HDSP-2450 TXVB	Operating Temperature Range: -55°C to +85°C 6.9 mm (.27") 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (.6") DIP True Hermetic Seal TXV — Hi Rel Screened TXVB — Hi Rel Screened to Level A MIL-D-87157	Red	• Military Equipment • High Reliability Applications • Avionics • Ground Support, Cockpit, Shipboard Systems	8-59
	HDSP-2451 HDSP-2451 TXV HDSP-2451 TXVB		Yellow		
	HDSP-2452 HDSP-2452 TXV HDSP-2452 TXVB		High Efficiency Red		

Optoelectronic Product Qualification

Two military documents are presently in use to qualify visible products. MIL-S-19500 establishes the standard JAN and JANTX test programs for hermetic lamps. Four hermetic lamps are listed on the Qualified Parts List (QPL) of MIL-S-19500. Descriptions of the individual devices are given in detail specifications called slash sheets.

The second military document governing the qualification of visible products is MIL-D-87157. This general specification is dated August 26, 1981, and covers solid state, light emitting diode displays. This specification may be used to cover all display products including lamps not covered in MIL-S-19500. This specification has provisions for four different quality levels as follows:





Level A Hermetically sealed displays with 100% screening tests

Level B Hermetically sealed displays without 100% screening tests

Level C Non-hermetic displays with 100% screening tests

Level D Non-hermetic displays without 100% screening tests

Hewlett-Packard devices meeting the hermeticity requirements of MIL-D-87157 include the hermetic hexadecimal, numeric, and alphanumeric displays described in this section of the catalog. If the suffix TXVB is added to the part number, the display is tested to Level A with 100% screening tests and qualification. If only the 100% tests are required, the suffix TXV is added.

Detailed testing programs which follow the general program for quality Level A are given in the individual data sheets.

The general program from MIL-D-87157 for quality Level C non-hermetic displays is given on the following pages.

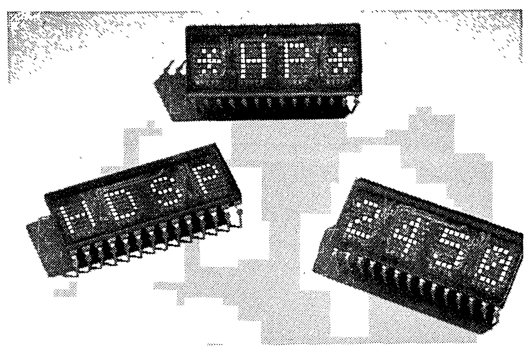


TABLE I. 100% SCREEN FORMAT FOR QUALITY LEVEL C

Test Screen	MIL-STD-750 Method	Level C
1. Precap Visual[1]	2072	When specified
2. High Temperature Storage[1]	1032	100%
3. Temperature Cycling[1]	1051	100%
4. Constant Acceleration[1,2]	2006	When specified
5. Fine Leak[1]	1071	N/A
6. Gross Leak[1]	1071	N/A
7. Interim Electrical/Optical Tests[1]	—	When specified
8. Burn-In[1,3]	1015	100%
9. Final Electrical/Optical Tests	—	100%
10. Delta Determinations[1]	—	When specified
11. External Visual[3]	2009	100%

Notes:
1. These tests are design dependent. The conditions and limits shall be specified in the detail specification when these tests are applicable.
2. Applicable to cavity type displays only.
3. MIL-STD-883 test method applies.

TABLE II. GROUP A ELECTRICAL TESTS[1]

Subgroups	LTPD
Subgroup 1 DC Electrical Tests at 25°C	5
Subgroup 2 Selected DC Electrical Tests at High Temperatures	7
Subgroup 3 Selected DC Electrical Tests at Low Temperatures	7
Subgroup 4 Dynamic Electrical Tests at $T_A = 25°C$	5
Subgroup 5 Dynamic Electrical Tests at High Temperatures	7
Subgroup 6 Dynamic Electrical Tests at Low Temperatures	7
Subgroup 7 Optical and Functional Tests at 25°C	5
Subgroup 8 External Visual	7

Notes:
1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail specification.

TABLE IIIb. GROUP B ENVIRONMENTAL TESTS (CLASS C AND D DISPLAYS ONLY)

Test	MIL-STD-750 Method	Sampling Plan
Subgroup 1		
Resistance to Solvents[1]	1022	4 Devices/ 0 Failures
Internal Visual and Mechanical[2,5]	2014	1 Device/ 0 Failures
Subgroup 2[3,4]		
Solderability[1]	2026	LTPD = 15
Electrical/Optical Endpoints[1]		
Subgroup 3		
Thermal Shock[1] (Temperature Cycling)	1051	LTPD = 15
Moisture Resistance[1]	1021	
Electrical/Optical Endpoints[1]		
Subgroup 4		
Operating Life Test (340 Hours)[1]	1027	LTPD = 10
Electrical/Optical Endpoints[1]		
Subgroup 5		
Non-Operating (Storage) Life Test (340 Hours)[1]	1032	LTPD = 10
Electrical/Optical Endpoints[1]		

Notes:
1. Test method or conditions in accordance with detail specification.
2. Not required for solid encapsulated displays.
3. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
4. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
5. MIL-STD-883 test method applies.

TABLE IVb. GROUP C PERIODIC TESTS (CLASS C AND D DISPLAYS ONLY)

Test	MIL-STD-750 Method	Sampling Plan
Subgroup 1[1]		
Physical Dimensions	2066	2 Devices/ 0 Failures
Subgroup 2[1]		
Lead Integrity[6]	2004	LTPD = 15
Subgroup 3		
Shock[2]	2016	LTPD = 15
Vibration, Variable Frequency[2]	2056	
Constant Acceleration[2]	2006	
External Visual[3]	1001 or 1011	
Electrical/Optical Endpoints[4]		
Subgroup 4		
Operating Life Test[4,5]	1026	$\lambda = 10$
Electrical/Optical Endpoints[4]		
Subgroup 5		
Temperature Cycling (25 cycles min.)[4]	1051	LTPD = 20
Electrical/Optical Endpoints[4]		

Notes
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. Not required for solid encapsulated displays.
3. Visual requirements shall be as specified in MIL-STD-883, method 1010 or 1011.
4. Test method or conditions in accordance with detail specification.
5. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made as a basis for Group B lot acceptance or the 1000 hours endpoint measurements shall be used as the basis for both Group B and C acceptance.
6. MIL-STD-883 test method applies.

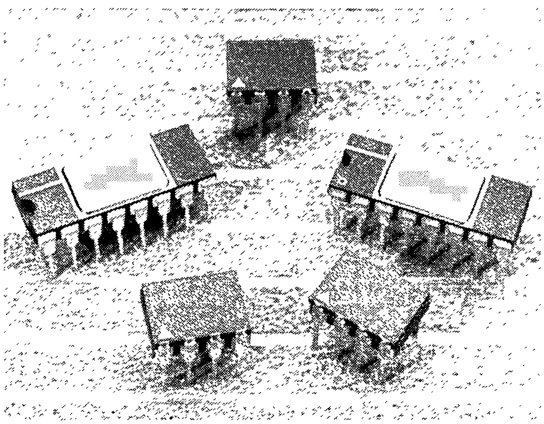
Hermetic Optocouplers

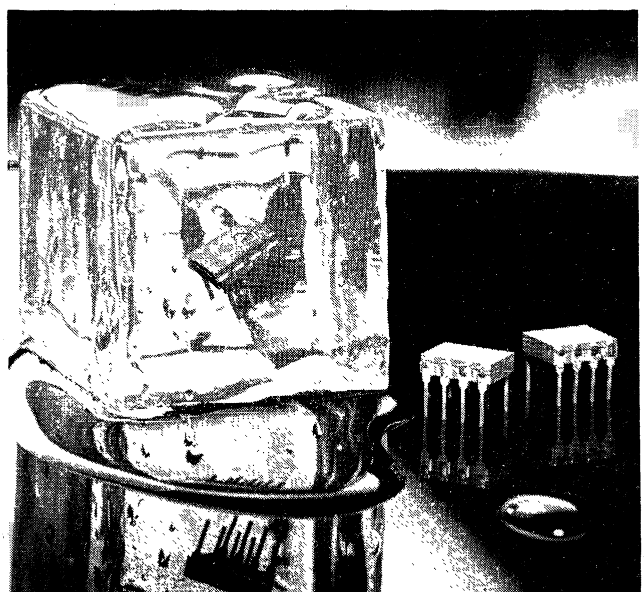
Hewlett-Packard has selected several very popular optocoupler types for assembly in our militarized hermetic 8 and 16 pin dual in-line packages. These devices offer a wide variety of LED input current levels, speed and current transfer ratio. High performance optocouplers are used in many U.S. and international military, aerospace and high reliability applications.

HP's 8102801EC and 8302401EC products are DESC* recognized devices which conform to MIL-STD-883 Class B testing. The 8102801EC is a 6N134 consisting of dual channel high speed logic gates compatible with TTL inputs and outputs. A second family of dual channel high speed logic gates, the HCPL-1930/1, were recently introduced and feature high common mode and input current regulation. The 8302401EC is a quad channel low power Darlington ideal for MOS, CMOS, or RS232-C data transmission systems. Our commercial quad optocoupler was re-registered as 6N140A featuring its new capability of full military temperature range from −55° C to +125° C. HP recently introduced a new family of 8 pin hermetic dual in-line packaged devices consisting of both single and dual channel Darlington units, the HCPL-5700/1 and HCPL-5730/1 respectively. The military types are fully compliant to MIL-STD-883 Class B, revision level C. The 4N55 product is a dual channel coupler having low gain transistor output useful for isolating circuits in power supply applications, logic interfacing, and wide bandwidth analog applications.

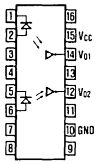
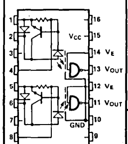
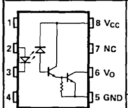
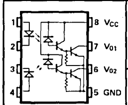
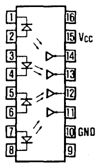
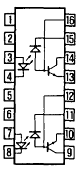
Special testing of hermetic optocouplers for advanced commercial, military, and aerospace applications has been performed since 1975. This testing is in accordance with the latest revisions of appropriate military and customers' specifications and drawings.

*Defense Electronic Supply Center(DESC) is an agency of the United States Department of Defense (DOD).





Hermetic Optocouplers

Device		Description	Application	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N134	Dual Channel Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems	10M bit/s	400% Typ.	10 mA	1500 V dc	8-66
	8102801EC	DESC Approved 6N134	Military/High Reliability					8-69
	6N134TXV	TXV — Screened						8-66
	6N134TXVB	TXVB — Screened with Group B Data	Use 8102801EC in New Designs					
	HCPL-1930	Dual Channel Hermetically sealed High CMR Line Receiver Optocoupler	Line receiver, High Speed Logic Ground Isolation in High Ground or Induced Noise Environments	10M bit/s	400% Typ.	10 mA	1500 Vdc	8-73
	HCPL-1931	MIL-STD-883 Class B Part	Military/High Reliability					
	HCPL-5700	Single Channel Hermetically Sealed High Gain Optocoupler	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	60k bit/s	200% Min.	0.5 mA	500 V dc	8-79
	HCPL-5701	MIL-STD-883 Class B Part	Military/High Reliability					
	HCPL-5730	Dual Channel Hermetically Sealed High Gain Optocoupler	Line Receiver, Polarity Sensing, Low Current Ground Isolation					8-83
	HCPL-5731	MIL-STD-883 Class B Part	Military/High Reliability					
	6N140A (6N140)	Hermetically Sealed Package Containing 4 Low Input Current, High Gain Optocouplers	Line Receiver, Low Power Ground Isolation for High Reliability Systems	100k bit/s	300% Min.	0.5 mA	1500 V dc	8-87
	8302401EC	DESC Approved 6N140A	Military/High Reliability					8-91
	6N140A/883B (6N140/883B)	MIL-STD-883 Class B Part	Use 8302401EC in New Designs					8-87
	6N140TXV	TXV — Hi-Rel Screened						
	6N140TXVB	TXVB — Hi-Rel Screened with Group B Data						
	4N55	Dual Channel Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element	700k bit/s	9% Min.	16 mA	1500 V dc	8-96
	4N55/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	4N55TXV	TXV — Hi-Rel Screened	Use 4N55/883B in New Designs					
	4N55TXVB	TXVB — Hi-Rel Screened with Group B Data						

Hermetic Optocoupler Product Qualification MIL-STD-883 Class B Test Program

The following 100% Screening and Quality Conformance Inspection programs show in detail the capabilities of our 4N55, 6N134, 6N140A, HCPL-5701, and 5731 optocouplers. This program will help customers understand the tests included in Methods 5004 and 5005 of MIL-STD-883 and to help in the design of special product drawings where this testing is required. The 4N55/883B, 5701/883B, 5731/883B, 8102801EC and 8302401EC (DESC Selected Item Drawings for the 6N134 and 6N140A respectively) have standardized test programs suitable for product use in military, high reliability applications and are the preferred devices by military contractors.

100% Screening

MIL-STD-883, METHOD 5004 (CLASS B DEVICES)

Test Screen	Method	Conditions
1. Precap Internal Visual	2010	Condition B, DESC Parts
2. High Temperature Storage	1008	Condition C, $T_A = 150°C$, Time = 24 Hours minimum
3. Temperature Cycling	1010	Condition C, −65° C to +150° C, 10 cycles
4. Constant Acceleration	2001	Condition A, 5K Gs, Y_1 axis only, 16 pin DIP, Condition E, 30K Gs, Y_1 axis only, 8 pin DIP
5. Fine Leak	1014	Condition A
6. Gross Leak	1014	Condition C
7. Interim Electrical Test	—	Group A, Subgroup 1, except $I_{I/O}$ (optional)
8. Burn-In	1015	Condition B, Time = 160 Hours minimum, $T_A = 125°C$ Burn-in conditions are product dependent and are given in the individual data sheets.
9. Final Electrical Test Electrical Test Electrical Test Electrical Test	—	Group A, Subgroup 1, 5% PDA applies Group A, Subgroup 2 Group A, Subgroup 3 Group A, Subgroup 9
10. External Visual	2009	

Quality Conformance Inspection

Group A electrical tests are product dependent and are given in the individual device data sheets. Group A and B testing is performed on each inspection lot.

GROUP A TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

	LTPD
Subgroup 1 Static tests at $T_A = 25°C$	2
Subgroup 2 Static tests at $T_A = +125°C$	3
Subgroup 3 Static tests at $T_A = -55°C$	5
Subgroups 4, 5, 6, 7 and 8 These subgroups are non-applicable to this device type	
Subgroup 9 Switching tests at $T_A = 25°C$	2
Subgroup 10 Switching tests at $T_A = +125°C$	3
Subgroup 11 Switching tests at $T_A = -55°C$	5

GROUP B TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1 Physical Dimensions (Not required if Group D is to be performed)	2016		2 Devices/ 0 Failures
Subgroup 2 Resistance to Solvents	2015		4 Devices/ 0 Failures
Subgroup 3 Solderability (LTPD applies to number of leads inspected — no fewer than 3 devices shall be used.)	2003	Soldering Temperature of 245 ± 5°C for 10 seconds	15 (3 Devices)
Subgroup 4 Internal Visual and Mechanical	2014		1 Device/ 0 Failures
Subgroup 5 Bond Strength (1) Thermocompression (performed at precap, prior to seal. LTPD applies to number of bond pulls from a minimum of 4 devices).	2011	(1) Test Condition D	15 (4 Devices)
Subgroup 6 Internal water vapor content (Not applicable — per footnote of MIL-STD)	—		—
Subgroup 7 Fine Leak Gross Leak	1014	Test Condition A Test Condition C	5
Subgroup 8* Electrical Test Electrostatic Discharge Sensitivity Electrical Test	 3015	Group A, Subgroup 1, except I_{I-O} Group A, Subgroup 1	15

*(To be performed at initial qualification only)

Group C testing is performed on a periodic basis from current manufacturing every 3 months.

GROUP C TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1 Steady State Life Test	1005	Condition B, Time = 1000 Hours Total $T_A = +125°C$ Burn-in conditions are product dependent and are given in the individual device data sheeets.	5
Endpoint Electricals at 168 hours and 504 hours		Group A, Subgroup 1, except I_{I-O}	
Endpoint Electricals at 1000 hours		Group A, Subgroup 1	
Subgroup 2 Temperature Cycling	1010	Condition C, -65°C to +150°C, 10 cycles	15
Constant Acceleration	2001	Condition A, 5KG's, Y_1 axis only	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per visual criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1	

OPTOCOUPLERS

HI REL/HERMETIC COMPONENTS

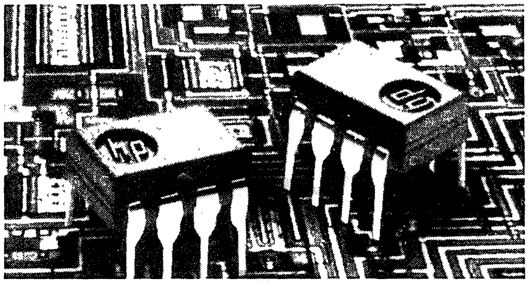
Group D testing is performed on a periodic basis from current manufacturing every 6 months.

GROUP D TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Test Condition B2 (lead fatigue)	15
Subgroup 3			
Thermal Shock	1011	Condition B, (−55°C to +125°C) 15 cycles min.	15
Temperature Cycling	1010	Condition C, (−65°C to +150°C) 100 cycles min.	
Moisture Resistance	1004		
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination		Per visual criteria of Method 1004 and 1010	
Endpoint Electricals		Group A, Subgroup 1	
Subgroup 4			
Mechanical Shock	2002	Condition B, 1500G, t = 0.5 ms, 5 blows in each orientation	15
Vibration Variable Frequency	2007	Condition A min.	
Constant Acceleration	2001	Condition A, 5KGs, Y_1 axis only, 16 pin DIP, Condition E, 30 KGs, Y_1 axis only, 8 pin DIP	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per visual criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1	
Subgroup 5			
Salt Atmosphere	1009	Condition A min.	15
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1009	Per visual criteria of Method 1009	
Suogroup 6			
Internal Water Vapor Content	1018	5,000 ppm maximum water content at 100°C	3 Devices (0 failures) 5 Devices (1 failure)
Subgroup 7			
Adhesion of lead finish	2025		15
Subgroup 8			
Lid Torque (Applicable to 8 pin DIP only)	2024		5 Devices (0 failures)

Plastic Optocouplers

Hewlett-Packard supplies plastic optocouplers with high reliability testing for commercial/industrial applications requiring prolonged operational life. Two of the most frequently requested 100% preconditioning and screening programs are given. The first program has burn-in and electrical test only, the second program adds temperature storage and temperature cycling. Either program is available for HP's plastic optocouplers. Electrical testing is to catalog conditions and limits and will include 100% DC parameters, sample testing of input-output insulation leakage current and appropriate AC parameters. Contact your local field representative for pricing and availability of these programs.



PLASTIC OPTOCOUPLERS
PRECONDITIONING AND SCREENING 100%

COMMERCIAL BURN-IN**

Examinations or Tests	MIL-STD-883 Methods	Conditions
1. Commercial Burn-in	1015	$T_A = 70°C$, 160 hours per designated circuit.
2. Electrical Test		Per specified conditions and min./max. limits at $T_A = 25°C$

SCREENING PROGRAM**

Examinations or Tests	MIL-STD-883 Methods	Conditions
1. High Temperature Storage	1008	24 hours at 125°C
2. Temperature Cycling	1010	10 cycles, -55°C to +125°C
3. Burn-in	1015	$T_A = 70°C$, 160 hours per designated circuit
4. Electrical Test		Per specified conditions and min./max. limits at $T_A = 25°C$
5. External Visual	2009	

**Contact your field salesman for details.

HEWLETT PACKARD

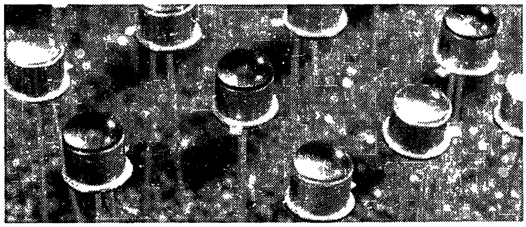
JAN QUALIFIED HERMETIC SOLID STATE LAMPS*

1N5765 JAN1N5765 JANTX1N5765	1N6093 JAN1N6093 JANTX1N6093
1N6092 JAN1N6092 JANTX1N6092	1N6094 JAN1N6094 JANTX1N6094

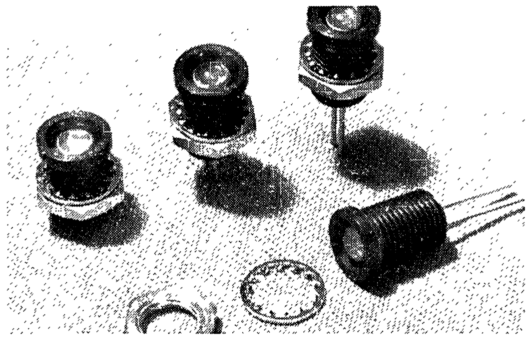
TECHNICAL DATA JANUARY 1986

Features

- **MILITARY QUALIFICATION**
- **CHOICE OF 4 COLORS**
  Red
  High Efficiency Red
  Yellow
  Green
- **DESIGNED FOR HIGH-RELIABILITY APPLICATIONS**
- **HERMETICALLY SEALED**
- **WIDE VIEWING ANGLE**
- **LOW POWER OPERATION**
- **IC COMPATIBLE**
- **LONG LIFE**
- **PANEL MOUNT OPTION HAS WIRE WRAPPABLE LEADS AND AN ELECTRICALLY ISOLATED CASE**



HERMETIC TO-46 LAMP



LAMP ASSEMBLY AS PANEL MOUNT

Description

The 1N5765, 1N6092, 1N6093, and 1N6094 are hermetically sealed solid state lamps encapsulated in a TO-46 package with a tinted diffused plastic lens over a glass window. These hermetic lamps provide good on-off contrast, high axial luminous intensity and a wide viewing angle.

All of these devices are available in a panel mountable fixture. The semiconductor chips are packaged in a hermetically sealed TO-46 package with a tinted diffused plastic lens over glass window. This TO-46 package is then encapsulated in a panel mountable fixture designed for high reliability applications. The encapsulated LED lamp assembly provides a high on-off contrast, a high axial luminous intensity and a wide viewing angle.

The 1N5765 utilizes a GaAsP LED chip with a red diffused plastic lens over glass window.

The 1N6092 has a high efficiency red GaAsP on GaP LED chip with a red diffused plastic lens over glass window. This lamp's efficiency is comparable to that of a GaP red but extends to higher current levels.

The 1N6093 provides a yellow GaAsP on GaP LED chip with a yellow diffused plastic lens over glass window.

The 1N6094 provides a green GaP LED chip with a green diffused plastic lens over glass window.

Part marking includes: part number from matrix below. CAQI designating code and YYWWX lot identification code including year, week and assembly plant if required. A maximum of 18 spaces can be accommodated.

COLOR — PART NUMBER — LAMP AND PANEL MOUNT MATRIX

Description	Standard Product	With JAN Qualification[1]	JAN Plus TX Testing[2]	Controlling MIL-S-19500 Document[4]
TABLE I HERMETIC TO-46 PART NUMBER SYSTEM				
Standard Red	1N5765	JAN1N5765	JANTX1N5765	/467
High Efficiency Red	1N6092	JAN1N6092	JANTX1N6092	/519
Yellow	1N6093	JAN1N6093	JANTX1N6093	/520
Green	1N6094	JAN1N6094	JANTX1N6094	/521
TABLE II PANEL MOUNTABLE PART NUMBER SYSTEM[3]				
Standard Red	HLMP-0904	HLMP-0930 (—)	HLMP-0931 (—)	NONE
High Efficiency Red	HLMP-0354	HLMP-0380 (JANM19500/51901)	HLMP-0381 (JTXM19500/51902)	/519
Yellow	HLMP-0454	HLMP-0480 (JANM19500/52001)	HLMP-0481 (JTXM19500/52002)	/520
Green	HLMP-0554	HLMP-0580 (JANM19500/52101)	HLMP-0581 (JTXM19500/52102)	/521

Notes:
1. Parts are marked J1NXXXX or as indicated.
2. Parts are marked JTX INXXXX or as indicated.
3. Panel mountable packaging incorporates additional assembly of the equivalent Table I TO-46 part into the panel mount enclosure. The resulting part is then marked per Table II.
4. JAN and JANTX parts only.

*Panel mount versions of all of the above are available per the selection matrix on this page.

JAN PART: Samples of each lot are subjected to Group A, B and C tests listed below. All tests are to the conditions and limits specified by the appropriate MIL-S-19500 slash sheet for the device under test. A summary of the data gathered in Groups A, B and C lot acceptance testing is supplied with each shipment.

Examination or Test	MIL-STD-750 Method
GROUP A INSPECTION	
Subgroup 1	
Visual and mechanical examination	2071
Subgroup 2	
Luminous intensity ($\theta = 0°$)	—
Luminous intensity ($\theta = 30°$)	—
Reverse current	4016
Forward voltage	4011
Subgroup 3	
Capacitance	4001
GROUP B INSPECTION	
Subgroup 1	
Physical dimensions	2066
Subgroup 2	
Solderability	2026
Thermal shock (temperature cycling)	1051
Thermal shock (glass strain)	1056
Hermetic seal	1071
Moisture resistance	1021
End points: Luminous intensity ($\theta = 0°$)	—
Subgroup 3	
Shock	2016
Vibration, variable frequency	2056
Constant acceleration	2006
End points: (same as subgroup 2)	
Subgroup 4	
Terminal strength	2036
End points: Hermetic seal	1071
Subgroup 5	
Salt atmosphere (corrosion)	1041
Subgroup 6	
High-temperature life (nonoperating)	1032
End points: Luminous intensity ($\theta = 0°$)	—
Subgroup 7	
Steady-state operation life	1027
End points: (same as subgroup 6)	

JANTX PART: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500 slash sheet. The JANTX lot has also been subjected to Group A, B and C tests as for the JAN PART above. A summary of the data gathered in Groups A, B and C acceptance testing is supplied with each shipment.

Examination or Test	MIL-STD-750 Method
GROUP C INSPECTION	
Subgroup 1	
Thermal shock (temperature cycling)	1051
End points: (same as subgroup 2 of group B)	
Subgroup 2	
Resistance to solvents	—
Subgroup 3	
High-temperature life (nonoperating)	1031
End points: Luminous intensity ($\theta = 0°$)	—
Subgroup 4	
Steady-state operation life	1026
End points: (same as subgroup 3)	
Subgroup 5	
Peak forward pulse current (transient)	—
End points: (same as subgroup 6 of group B)	
Subgroup 6	
Peak forward pulse current (operating)	—
End points: (same as subgroup 6 of group B)	
PROCESS AND POWER CONDITION ("TX" types only)	
High temperature storage (nonoperating)	—
Thermal shock (temperature cycling)	1051
Constant acceleration	2006
Hermetic seal	1071
Luminous intensity ($\theta = 0°$)	—
Forward voltage	4011
Reverse current	4016
Burn-in (Forward bias)	—
End points (within 72 hours of burn-in):	
Δ Luminous intensity ($\theta = 0°$)	—
Δ Forward voltage	4011

Absolute Maximum Ratings at T_A=25°C

Parameter	Red HLMP-0904	High Eff. Red HLMP-0354	Yellow HLMP-0454	Green HLMP-0554	Units
Power Dissipation (derate linearly from 50°C at 1.6mW/°C)	100	120	120	120	mW
DC Forward Current	50[1]	35[2]	35[2]	35[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-65°C to 100°C				
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	260°C for 7 seconds.				

Notes: 1. Derate from 50°C at 0.2mA/°C   2. Derate from 50°C at 0.5mA/°C

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	HLMP-0904			HLMP-0354			HLMP-0454			HLMP-0554			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{V1}	Axial Luminous Intensity	0.5	1.0		1.0	5		1.0	6		0.8	3 At I_F = 25mA		mcd	I_F = 20mA Figs. 3,8,13,18 $\theta = 0°$
I_{V2}	Luminous Intensity at $\theta = 30°$[5]	0.3			0.5			0.5			0.4			mcd	I_F = 20 mA $\theta = 30°$
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		60			70			70			70		deg.	[1] Figures 6, 11, 16, 21
λ_{PEAK}	Peak Wavelength[5]	630	655	700	590	635	695	550	583	660	525	565	600	nm	Measurement at Peak
λ_d	Dominant Wavelength		640			626			585			570		nm	[2]
τ_S	Speed of Response		10			200			200			200		ns	
C	Capacitance[5]		200	300		35	100		35	100		35	100	pF	V_F=0; f=1 MHz
θ_{JC}	Thermal Resistance*		425			425			425			425		°C/W	[3]
θ_{JC}	Thermal Resistance**		550			550			550			550		°C/W	[3]
V_F	Forward Voltage		1.6	2.0		2.0	3.0		2.0	3.0		2.1 At I_F = 25mA	3.0	V	I_F = 20mA Figures 2, 7, 12, 17
I_R	Reverse Current[5]			1.0			1.0			1.0			1.0	μA	V_R = 3V
BV_R	Reverse Breakdown Voltage	4	5		5.0			5.0			5.0			V	I_R = 100μA
η_V	Luminous Efficacy		56			140			455			600		lm/W	[4]

NOTES:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Junction to Cathode Lead with 3.18mm (0.125 inch) of leads exposed between base of flange and heat sink.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.
5. Limits do not apply to non JAN parts.

*Panel mount.
**T0-46

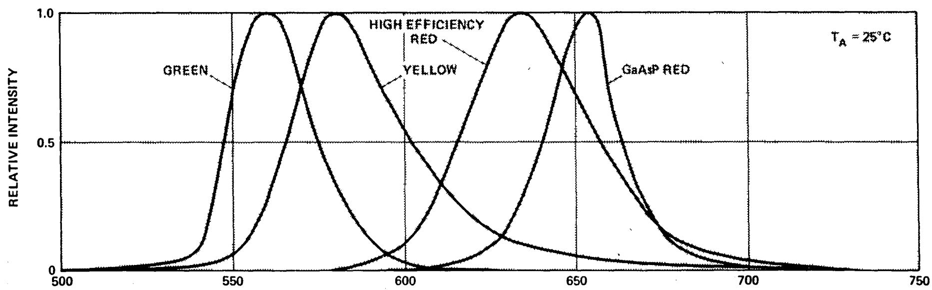
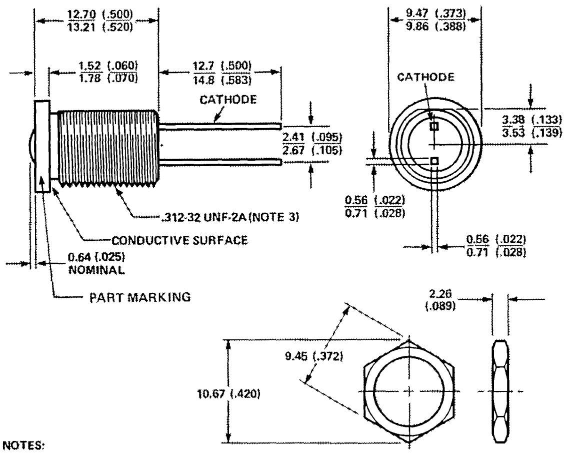
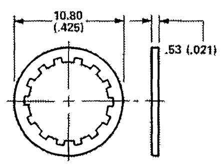


Figure 1. Relative Intensity vs. Wavelength.

Package Dimensions

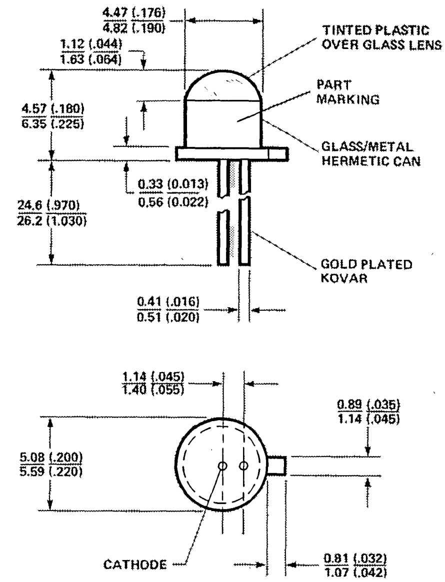
HLMP-0904, 0354, 0454, 0554





NOTES:
1. ALL EXTERNAL METAL SURFACES OF THE PACKAGE ARE BLACK ANODIZED EXCEPT FOR THE ALODINE AREA OF THE FLANGE AND THE GOLD PLATED LEADS.
2. MOUNTING HARDWARE WHICH INCLUDES ONE LOCK WASHER AND ONE HEX-NUT IS INCLUDED WITH EACH PANEL MOUNTABLE HERMETIC SOLID STATE LAMP.
3. USE OF METRIC DRILL SIZE 8.20 MILLIMETRES OR ENGLISH DRILL SIZE P (0.323 INCH) IS RECOMMENDED FOR PRODUCING HOLE IN THE PANEL FOR PANEL MOUNTING.
4. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
5. PACKAGE WEIGHT INCLUDING LAMP AND PANEL MOUNT IS 1.2 - 1.8 GRAMS. NUT AND WASHER IS AN EXTRA .6 - 1.0 GRAM.

1N5765, 1N6092, 1N6093, 1N6094



OUTLINE TO-46

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. GOLD-PLATED LEADS.
3. PACKAGE WEIGHT OF LAMP ALONE IS .25 - .35 GRAMS.

Family of Red 1N5765/HLMP-0904

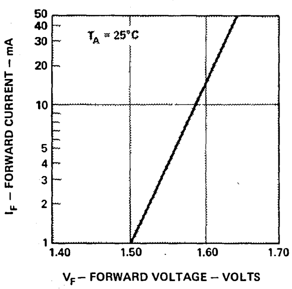


Figure 2. Forward Current vs. Forward Voltage.

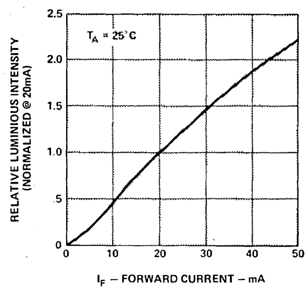


Figure 3. Relative Luminous Intensity vs. Forward Current.

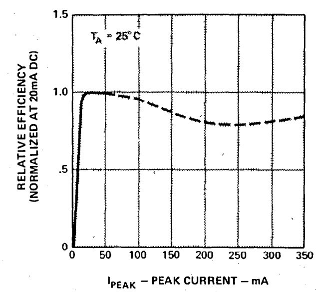


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

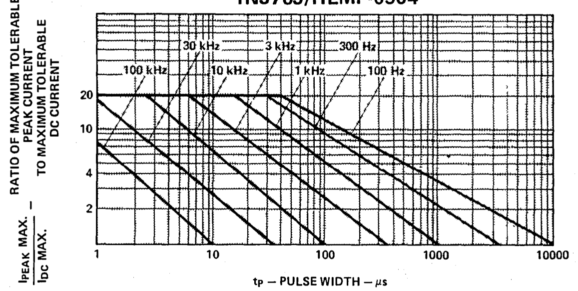


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

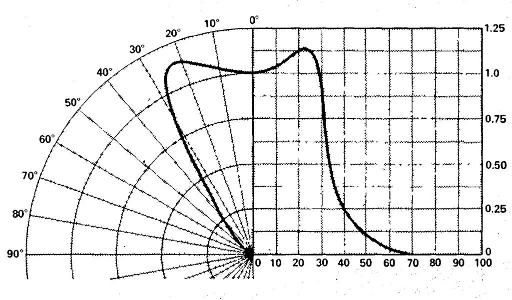


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

SOLID STATE LAMPS

HI REL/HERMETIC COMPONENTS

Family of High Efficiency Red 1N6092/HLMP-0354

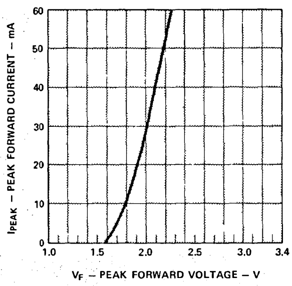


Figure 7. Forward Current vs. Forward Voltage.

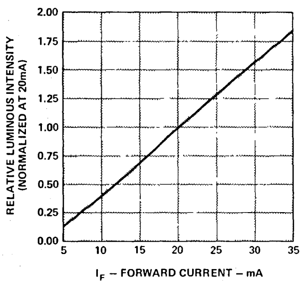


Figure 8. Relative Luminous Intensity vs. Forward Current.

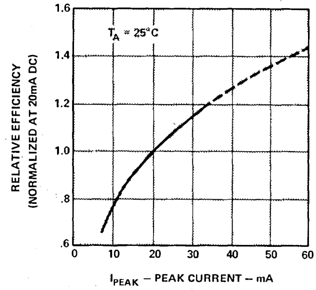


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

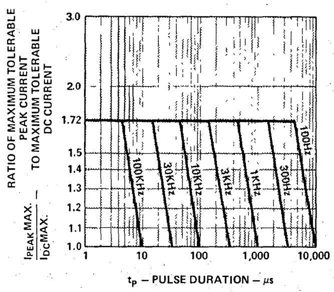


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

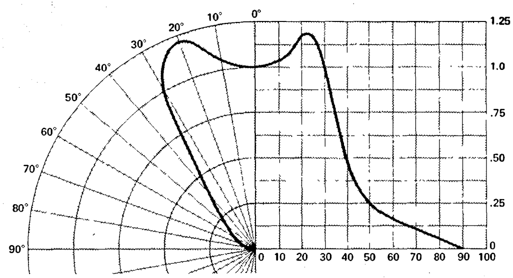


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Family of Yellow 1N6093/HLMP-0454

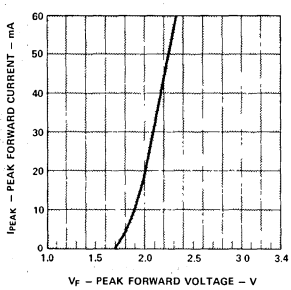


Figure 12. Forward Current vs. Forward Voltage.

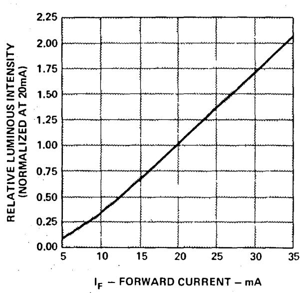


Figure 13. Relative Luminous Intensity vs. Forward Current.

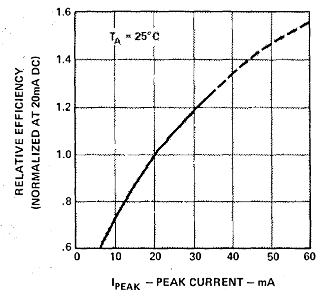


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

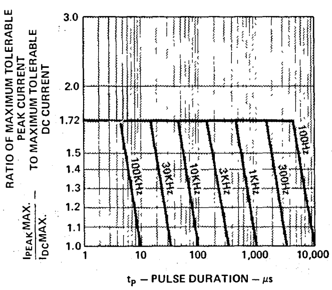


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

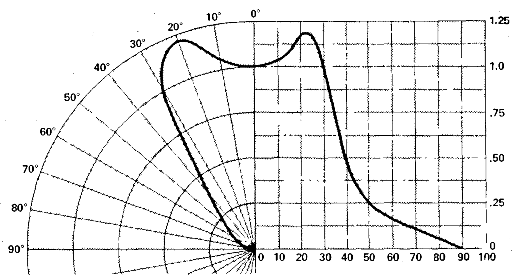


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Family of Green 1N6094/HLMP-0554

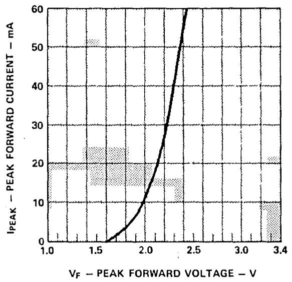


Figure 17. Forward Current vs. Forward Voltage.

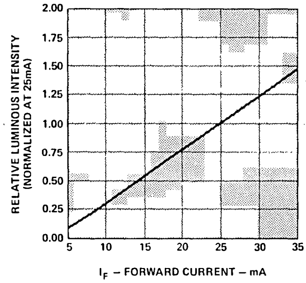


Figure 18. Relative Luminous Intensity vs. Forward Current.

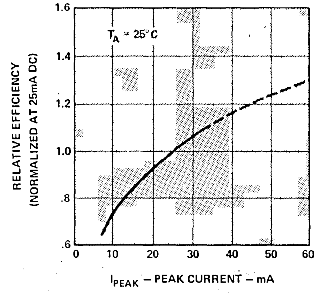


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

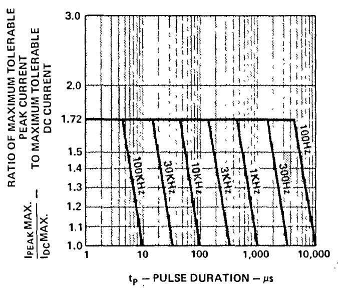


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

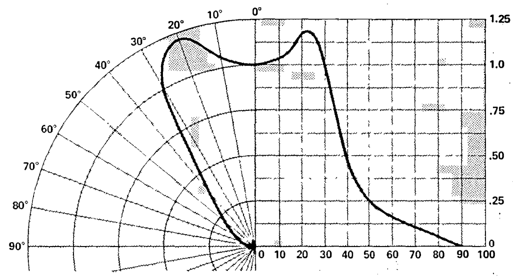


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

SOLID STATE LAMPS

HI REL/HERMETIC COMPONENTS

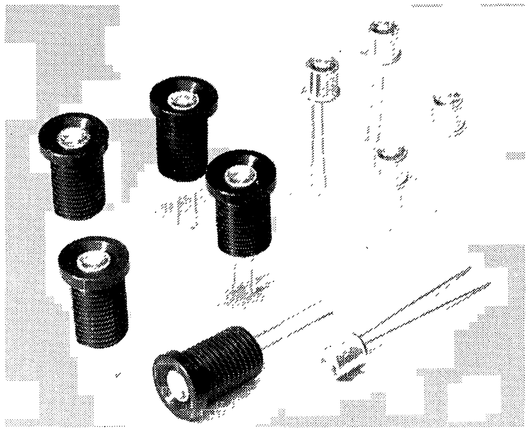
ULTRA-BRIGHT HERMETIC SOLID STATE LAMPS*

HLMP-0363 HLMP-0463 HLMP-0563
HLMP-0391 HLMP-0491 HLMP-0591
HLMP-0392 HLMP-0492 HLMP-0592

TECHNICAL DATA JANUARY 1986

Features

- **SUNLIGHT VIEWABLE WITH PROPER CONTRAST ENHANCEMENT FILTER**
- **HERMETICALLY SEALED**
- **CHOICE OF 3 COLORS**
  High Efficiency Red
  Yellow
  High Performance Green
- **LOW POWER OPERATION**
- **IC COMPATIBLE**
- **LONG LIFE/RELIABLE/RUGGED**
- **PANEL MOUNT OPTION with**
  Wire Wrappable leads
  Electrically isolated case



Description

The HLMP-0363, HLMP-0463, and HLMP-0563 are hermetically sealed solid state lamps in a TO-18 package with a clear glass lens. These hermetic lamps provide improved brightness over conventional hermetic LED lamps, good on-off contrast, and high axial luminous intensity. These LED indicators are designed for use in applications requiring readability in bright sunlight. With a proper contrast enhancement filter, these LED indicators are readable in sunlight ambients. All of these devices are available in a panel mountable fixture.

The HLMP-0363 utilizes a high efficiency red GaAsP on GaP LED chip. The HLMP-0463 uses a yellow GaAsP on a GaP LED chip. The HLMP-0563 uses a green GaP LED chip.

These devices are offered with JAN equivalent quality conformance inspection (QCI) and JANTX equivalent screenings similar to MIL-S-19500/519/520/521.

*Panel Mount version of all of the above are available per the selection matrix on this page.

COLOR — PART NUMBER — LAMP AND PANEL MOUNT MATRIX

Description	Standard Product	JAN QCI	JANTX Equivalent
TABLE I HERMETIC TO-18 PART NUMBER SYSTEM			
High Efficiency Red	HLMP-0363	HLMP-0391	HLMP-0392
Yellow	HLMP-0463	HLMP-0491	HLMP-0492
Green	HLMP-0563	HLMP-0591	HLMP-0592
TABLE II PANEL MOUNTABLE PART NUMBER SYSTEM[1]			
High Efficiency Red	HLMP-0364	HLMP-0365	HLMP-0366
Yellow	HLMP-0464	HLMP-0465	HLMP-0466
Green	HLMP-0564	HLMP-0565	HLMP-0566

NOTE:
1. Panel mountable packaging incorporates additional assembly of the equivalent Table I TO-18 part into the panel mount enclosure. The resulting part is then marked per Table II.

JAN QCI: Samples of each lot are subjected to Group A, B and C tests listed below. All tests are to the conditions and limits specified by the appropriate MIL-S-19500 slash sheet for the device under test. A summary of the data gathered in Groups A, B and C lot acceptance testing is supplied with each shipment.

Examination or Test	MIL-STD-750 Method
GROUP A INSPECTION	
Subgroup 1	
Visual and mechanical examination	2071
Subgroup 2	
Luminous intensity ($\theta = 0°$)	—
Reverse current	4016
Forward voltage	4011
Subgroup 3	
Capacitance	4001
GROUP B INSPECTION	
Subgroup 1	
Physical dimensions	2066
Subgroup 2	
Solderability	2026
Thermal shock (temperature cycling)	1051
Thermal shock (glass strain)	1056
Hermetic seal	1071
Moisture resistance	1021
End points: Luminous intensity ($\theta = 0°$)	—
Subgroup 3	
Shock	2016
Vibration, variable frequency	2056
Constant acceleration	2006
End points: (same as subgroup 2)	
Subgroup 4	
Terminal strength	2036
End points: Hermetic seal	1071
Subgroup 5	
Salt atmosphere (corrosion)	1041
Subgroup 6	
High-temperature life (nonoperating)	1032
End points: Luminous intensity ($\theta = 0°$)	—
Subgroup 7	
Steady-state operation life	1027
End points: (same as subgroup 6)	

JANTX Equivalent: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500 slash sheet. The JANTX lot has also been subjected to Group A, B and C tests as for the JAN QCI PART above. A summary of the data gathered in Groups A, B and C acceptance testing is supplied with each shipment.

Examination or Test	MIL-STD-750 Method
GROUP C INSPECTION	
Subgroup 1	
Thermal shock (temperature cycling)	1051
End points: (same as subgroup 2 of group B)	
Subgroup 2	
Resistance to solvents	—
Subgroup 3	
High-temperature life (nonoperating)	1031
End points: Luminous intensity ($\theta = 0°$)	—
Subgroup 4	
Steady-state operation life	1026
End points: (same as subgroup 3)	
Subgroup 5	
Peak forward pulse current (transient)	—
End points: (same as subgroup 6 of group B)	
Subgroup 6	
Peak forward pulse current (operating)	—
End points: (same as subgroup 6 of group B)	
PROCESS AND POWER CONDITION ("TX" types only)	
High temperature storage (nonoperating)	—
Thermal shock (temperature cycling)	1051
Constant acceleration	2006
Hermetic seal	1071
Luminous intensity ($\theta = 0°$)	—
Forward voltage	4011
Reverse current	4016
Burn-in (Forward bias)	—
End points (within 72 hours of burn-in):	
Δ Luminous intensity ($\theta = 0°$)	—
Δ Forward voltage	4011

Absolute Maximum Ratings at T_A=25° C

Parameter	High Eff. Red HLMP-0363	Yellow HLMP-0463	Green HLMP-0563	Units
Power Dissipation (derate linearly from 50° C at 1.6mW/° C)	120	120	120	mW
DC Forward Current	35[1]	35[1]	35[1]	mA
Peak Forward Current	60 See Fig. 5	60 See Fig. 10	60 See Fig. 15	mA
Operating and Storage Temperature Range	-65° C to 100° C			
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	260° C for 7 seconds.			

NOTES: 1. Derate from 50° C at 0.5mA/° C

Electrical/Optical Characteristics at T_A=25° C

Symbol	Description	HLMP-0363			HLMP-0463			HLMP-0563			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{V1}	Axial Luminous Intensity	20	50		20	50		20	50 At I_F = 25mA		mcd	I_F = 20mA Figs. 3,8,13 θ = 0°
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		18			18			18		deg.	[1] Figures 6,11,16
λ_{PEAK}	Peak Wavelength	590	635	695	550	583	660	525	565	600	nm	Measurement at Peak
λ_d	Dominant Wavelength		626			585			570		nm	[2]
τ_s	Speed of Response		200			200			200		ns	
C	Capacitance[5]		35	100		35	100		35	100	pF	V_1=0; f=1 MHz
Θ_{JC}	Thermal Resistance*		425			425			425		° C/W	[3]
Θ_{JC}	Thermal Resistance**		550			550			550		° C/W	[3]
V_F	Forward Voltage		2.0	3.0		2.0	3.0		2.1 At I_F = 25mA	3.0	V	I_F = 20mA Figures 2,7,12
I_R	Reverse Current			1.0			1.0			1.0	μA	V_R = 3V
BV_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	I_R = 100μA
η_v	Luminous Efficacy		140			455			600		lm/W	[4]

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Junction to Cathode Lead with 3.18mm (0.125 inch) of leads exposed between base of flange and heat sink.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.
5. Limits do not apply to non screened parts.

*Panel mount. **TO-18.

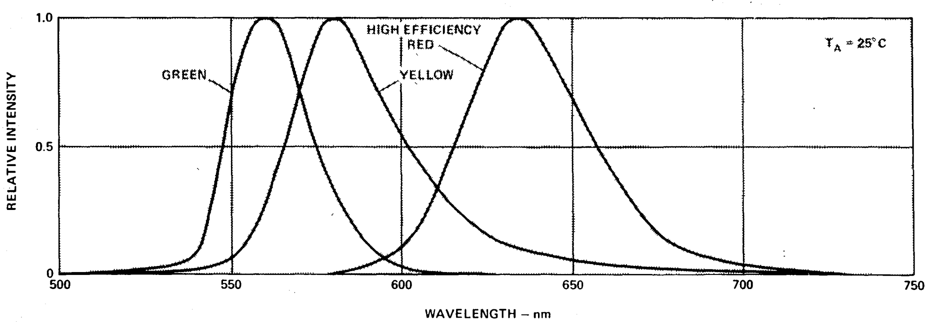
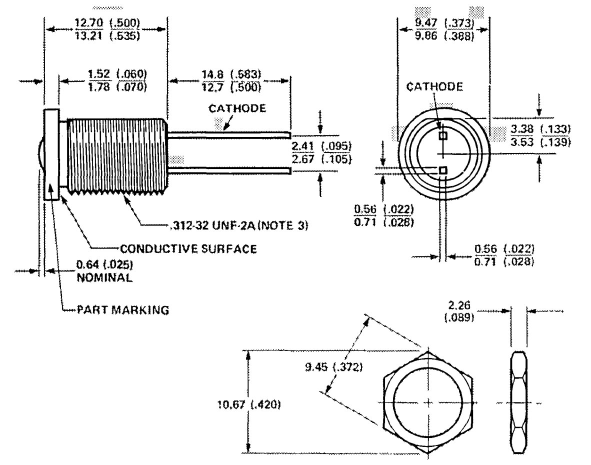


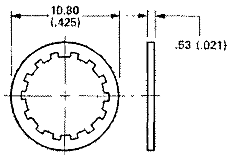
Figure 1. Relative Intensity vs. Wavelength.

Package Dimensions

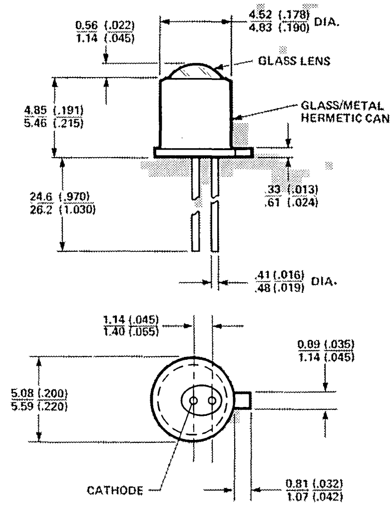
HLMP-0364, 0464, 0564



NOTES:
1. BLACK PANEL MOUNT SLEEVE
2. MOUNTING HARDWARE WHICH INCLUDES ONE LOCK WASHER AND ONE HEX-NUT IS INCLUDED WITH EACH PANEL MOUNTABLE HERMETIC SOLID STATE LAMP.
3. USE OF METRIC DRILL SIZE 8.20 MILLIMETRES OR ENGLISH DRILL SIZE P (0.323 INCH) IS RECOMMENDED FOR PRODUCING HOLE IN THE PANEL FOR PANEL MOUNTING.
4. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
5. PACKAGE WEIGHT INCLUDING LAMP AND PANEL MOUNT IS 1.2 - 1.8 GRAMS. NUT AND WASHER IS AN EXTRA .6 - 1.0 GRAM.



HLMP-0363, 0463, 0563



DIMENSIONS IN MILLIMETERS AND (INCHES).

OUTLINE TO-18

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. GOLD-PLATED LEADS.
3. PACKAGE WEIGHT OF LAMP ALONE IS .25 - .40 GRAMS.

Family of High Efficiency Red HLMP-0363/HLMP-0364

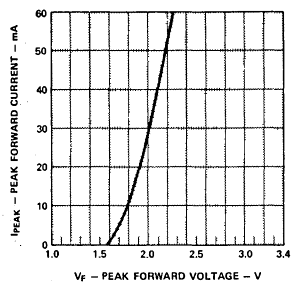


Figure 2. Forward Current vs. Forward Voltage.

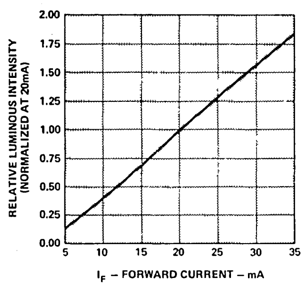


Figure 3. Relative Luminous Intensity vs. Forward Current.

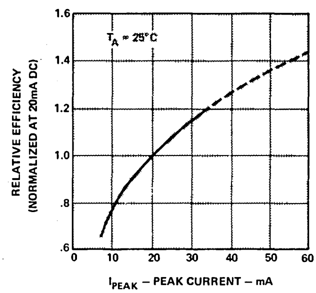


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

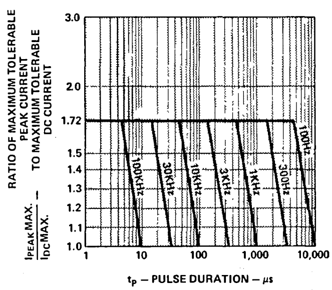


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

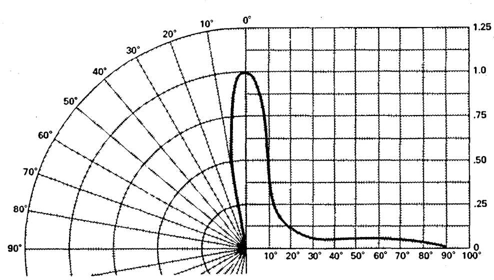


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Family of Yellow HLMP-0463/HLMP-0464

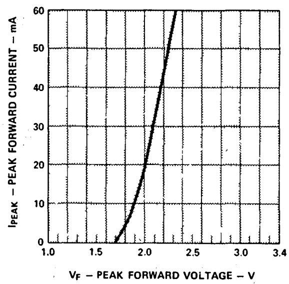


Figure 7. Forward Current vs. Forward Voltage.

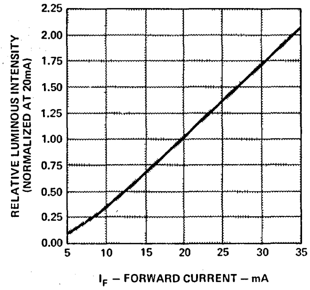


Figure 8. Relative Luminous Intensity vs. Forward Current.

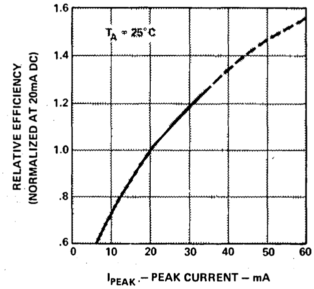


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

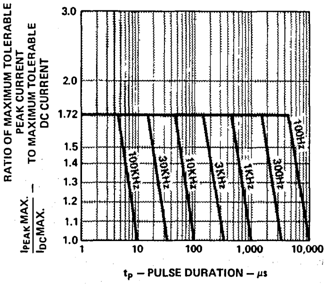


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

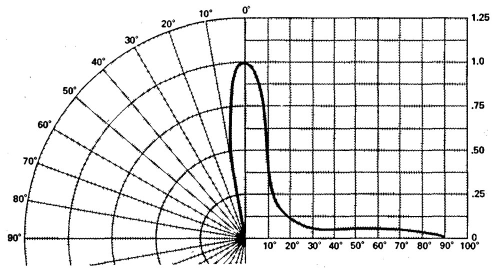


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Family of Green HLMP-0563/HLMP-0564

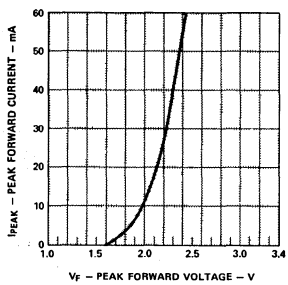


Figure 12. Forward Current vs. Forward Voltage.

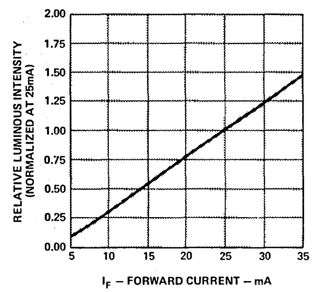


Figure 13. Relative Luminous Intensity vs. Forward Current.

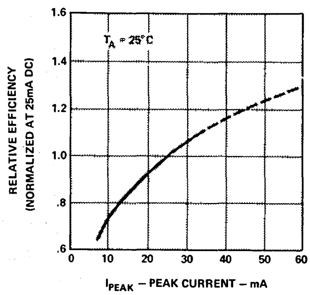


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

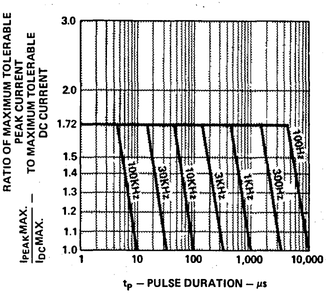


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

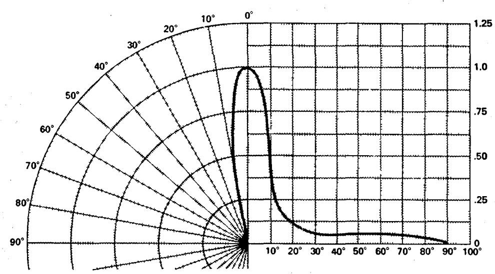


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Contrast Enhancement

The objective of contrast enhancement is to optimize display readability. Adequate contrast enhancement can be achieved in indoor applications through luminous contrast techniques. Luminous contrast is the observed brightness of the illuminated indicator compared to the brightness of the surround. Appropriate wavelength filters maximize luminous contrast by reducing the amount of light reflected from the area around the indicator while transmitting most of the light emitted by the indicator. These filters are described further in Application Note 1015.

SOLID STATE LAMPS

HI REL/HERMETIC COMPONENTS

HEWLETT PACKARD

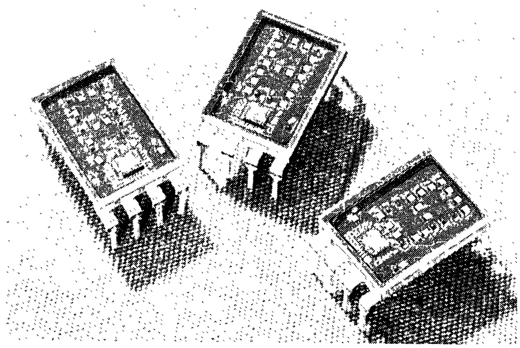
HERMETIC, HEXADECIMAL AND NUMERIC DISPLAYS FOR HIGH RELIABILITY APPLICATIONS

4N51 (5082-7391)/4N51TXV/M87157/00101ACX
4N52 (5082-7392)/4N52TXV/M87157/00102ACX
4N53 (5082-7393)/4N53TXV/M87157/00103ACX
4N54 (5082-7395)/4N54TXV/M87157/00104ACX

TECHNICAL DATA JANUARY 1986

Features

- HERMETICALLY SEALED
- TXV VERSION AVAILABLE
- THREE CHARACTER OPTIONS
  Numeric
  Hexadecimal
  Over Range
- 4 x 7 DOT MATRIX CHARACTER
- PERFORMANCE GUARANTEED OVER TEMPERATURE
- HIGH TEMPERATURE STABILIZED
- GOLD PLATED LEADS
- MEMORY LATCH/DECODER/DRIVER
  TTL Compatible
- CATEGORIZED FOR LUMINOUS INTENSITY



Description

The 4N51-4N54 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory are hermetically sealed 7.4mm (0.29 inch) displays for use in military and aerospace applications.

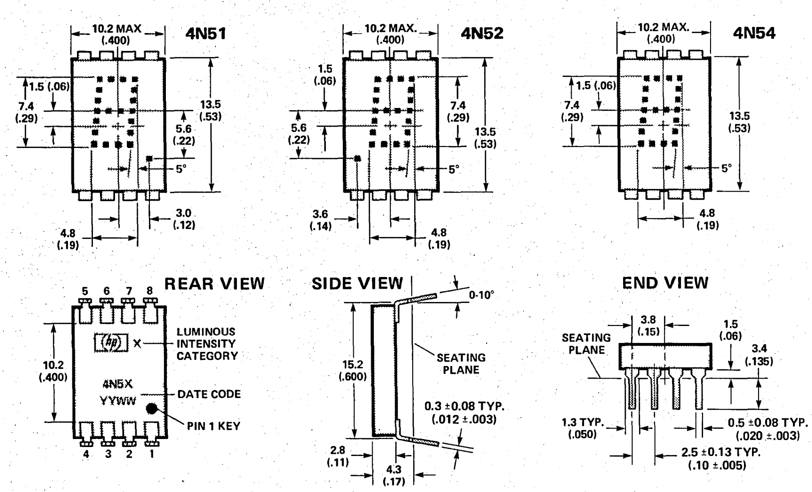
The 4N51 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.

The 4N52 is the same as the 4N51 except that the decimal point is located on the left-hand side of the digit.

The 4N54 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory.

The 4N53 is a "±1." overrange display, including a right-hand decimal point.

Package Dimensions*



PIN	FUNCTION 4N51 4N52 NUMERIC	FUNCTION 4N54 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.
4. Lead material is gold plated copper alloy.

*JEDEC Registered Data.

Absolute Maximum Ratings*

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions*

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1,2]	T_A	−55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics *(T_A = −55°C to +100°C, unless otherwise specified)

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}				0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}	V_{CC}=4.5V			0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight **				1.0		gm
Leak Rate					5×10^{-8}	cc/sec

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50°C/W; Θ_{JC}=15°C/W. 2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 4N54. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

*JEDEC Registered Data. **Non Registered Data.

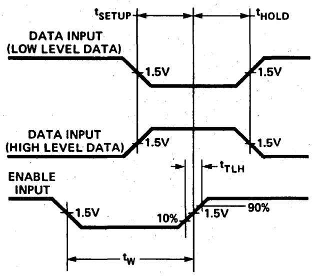


Figure 1. Timing Diagram of 4N51-4N54 Series Logic.

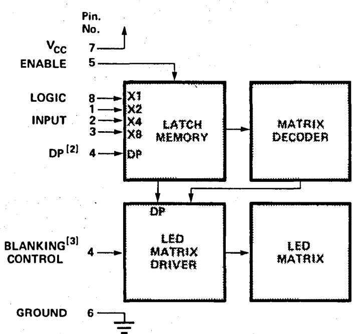


Figure 2. Block Diagram of 4N51-4N54 Series Logic.

TRUTH TABLE					
BCD DATA[1]				4N51 AND 4N52	4N54
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	[illegible]	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	....	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 4N51 and 4N52 displays.
3. The blanking control input, B, pertains only to the 4N54 hexadecimal display. Blanking input has no effect upon display memory.

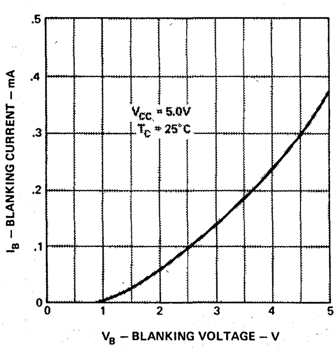


Figure 3. Typical Blanking Control Current vs. Voltage for 4N54.

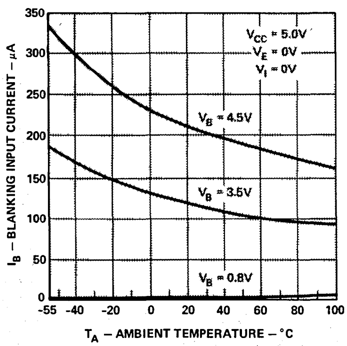


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 4N54.

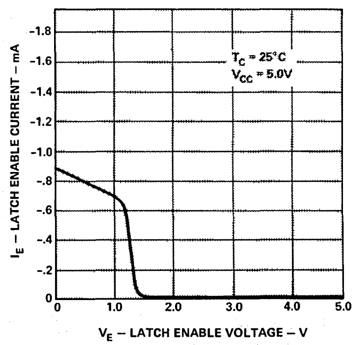


Figure 5. Typical Latch Enable Input Current vs. Voltage.

*JEDEC Registered Data.

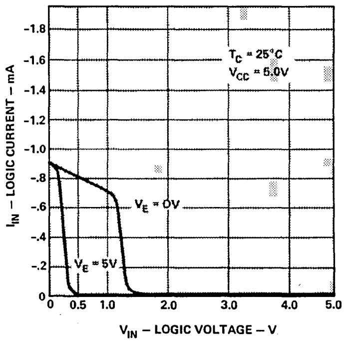


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

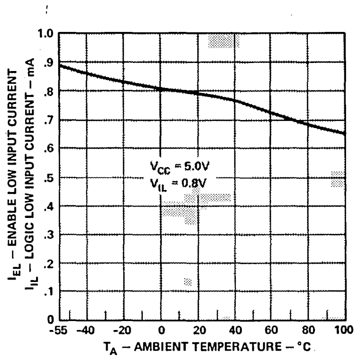


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

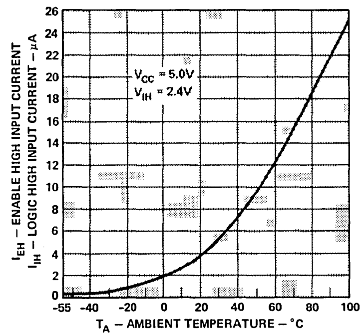


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 4N51-4N54 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 4N54 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

MECHANICAL

4N51-4N54 series displays are hermetically tested for use in environments which require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5 x 10^{-8} CC/SEC and a standard dye penetrant gross leak test.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100°C, it is important to maintain a case-to-ambient thermal resistance of less than 35°C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

4N51-4N54 series displays are 100% preconditioned by 24 hour storage at 125°C.

CONTRAST ENHANCEMENT

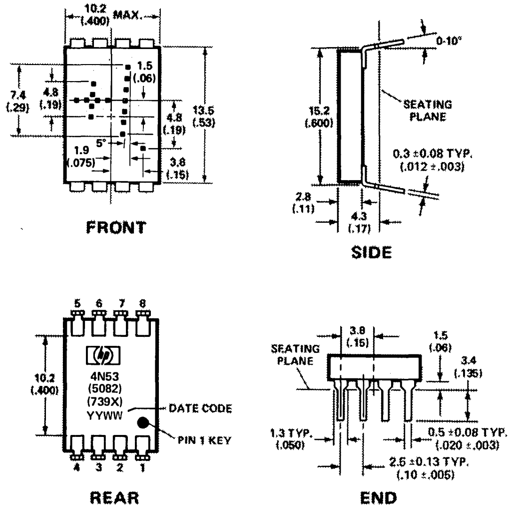
The 4N51-4N54 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

*JEDEC Registered Data.

Solid State Over Range Character

For display applications requiring a +, 1, or decimal point designation, the 4N53 over range character is available. This display module comes in the same package as the 4N51-4N54 series numeric indicator and is completely compatible with it.

Package Dimensions*



NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

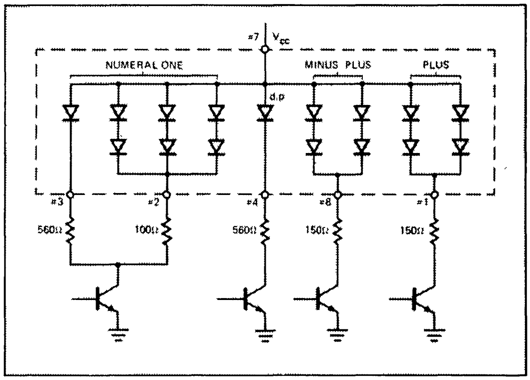


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics*

4N53 (T_A = –55°C to +100°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_ν	I_F = 6 mA T_C = 25°C	40	85		μcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λd	T_C = 25°C		640		nm
Weight * *				1.0		gm

Recommended Operating Conditions*

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

*JEDEC Registered Data. **Non Registered Data.

Absolute Maximum Ratings*

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa and IVa
PREFERRED PART NUMBER SYSTEM		
4N51	4N51TXV	M87157/00101ACX
4N52	4N52TXV	M87157/00102ACX
4N54	4N54TXV	M87157/00103ACX
4N53	4N53TXV	M87157/00104ACX

100% Screening

TABLE I.
QUALITY LEVEL A OF MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7572-52
2. High Temperature Storage	1032	$T_A = 125°C$, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 Cycles, 15 Min. Dwell
4. Constant Acceleration	2006	10,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C
7. Interim Electrical/Optical Tests[2]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} $T_A = 25°C$
8. Burn-In[1, 3]	1015	Condition B at $V_{CC} = 5V$ and cycle through logic at 1 character per second. $T_A = 100°C$, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	$\Delta I_V = -20\%$, $\Delta I_{CC} = \pm 10$ mA, $\Delta I_{IH} = \pm 10 \mu A$ and $\Delta I_{EH} = \pm 13 \mu A$
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. Burn-in for the over range shall use Condition B at a nominal $I_F = 8$ mA with '+1' illuminated for t = 160 hours.

TABLE II
GROUP A ELECTRICAL TESTS — MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function, $T_A = 25°C$	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. $T_A = +100°C$	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. $T_A = -55°C$	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

1. Limits and conditions are per the electrical/optical characteristics.

SOLID STATE DISPLAYS

HI REL/HERMETIC COMPONENTS

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical	2075		1 Device/ 0 Failures
Subgroup 2[1,2]			
Solderability	2026	$T_A = 245°C$ for 5 seconds	LTPD = 15
Subgroup 3			
Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 Min. Dwell	LTPD = 15
Moisture Resistance[3]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Electrical/Optical Endpoints[4]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual function. $T_A = 25°C$	
Subgroup 4			
Operating Life Test (340 hrs.)[5]	1027	$T_A = +100°C$ at $V_{CC} = 5.0V$ and cycling through logic at 1 character per second.	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3.	
Subgroup 5			
Non-operating (Storage) Life Test (340 hrs.)	1032	$T_A = +125°C$	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Initial conditioning should be a 15° bent inward one cycle.
4. Limits and conditions are per the electrical/optical characteristics.
5. Burn-in for the over range shall use Condition B at a nominal $I_F = 8$ mA with '+1' illuminated for t = 160 hours.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual Function, $T_A = 25°C$	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			$\lambda = 10$
Operating Life Test[6]	1026	$T_A = +100°C$	
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C Life Test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.

HEWLETT PACKARD

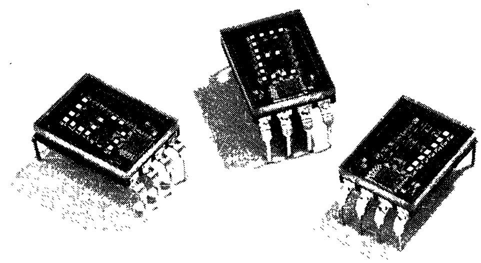
HERMETIC, HEXADECIMAL AND NUMERIC DISPLAYS FOR MILITARY APPLICATIONS

HIGH EFFICIENCY RED
Low Power HDSP-078X/078XTXV/078XTXVB
High Brightness HDSP-079X/079XTXV/079XTXVB
YELLOW HDSP-088X/088XTXV/088XTXVB

TECHNICAL DATA JANUARY 1986

Features

- **CONFORM TO MIL-D-87157, QUALITY LEVEL A**
- **HERMETICALLY SEALED**
- **TXV AND TXVB VERSIONS AVAILABLE**
- **THREE CHARACTER OPTIONS**
  Numeric
  Hexadecimal
  Over Range
- **4 x 7 DOT MATRIX CHARACTER**
- **HIGH EFFICIENCY RED AND YELLOW**
- **TWO HIGH EFFICIENCY RED OPTIONS**
  Low Power
  High Brightness
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **HIGH TEMPERATURE STABILIZED**
- **GOLD PLATED LEADS**
- **MEMORY LATCH/DECODER/DRIVER**
  TTL Compatible
- **CATEGORIZED FOR LUMINOUS INTENSITY**



Description

These displays are hermetic, solid state numeric and hexadecimal indicators with on-board decoder/drivers and memory. They are designed and tested for use in military and aero-space applications. The character height is 7.4 mm (0.29 inch). The TXVB versions of these products conform to Quality Level A of MIL-D-87157, the general specification for light emitting diode displays.

The numeric devices decode positive BCD logic into characters "0-9", a "—" sign, decimal point, and a test pattern. The hexadecimal devices decode positive BCD logic into 16 characters, "0-9, A-F". An input is provided on the hexadecimal devices to blank the display (all LEDs off) without losing the contents of the memory.

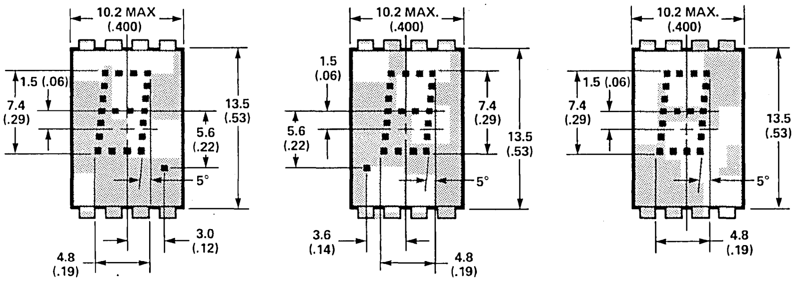
The over range device displays "±1" and right hand decimal point and is typically driven via external switching transistors.

Devices

Part Number HDSP-	Color	Description	Front View
0781/0781TXV/0781TXVB	High-Efficiency Red Low Power	Numeric, Right Hand DP	A
0782/0782TXV/0782TXVB		Numeric, Left Hand DP	B
0783/0783TXV/0783TXVB		Over Range ±1	C
0784/0784TXV/0784TXVB		Hexadecimal	D
0791/0791TXV/0791TXVB	High-Efficiency Red High Brightness	Numeric, Right Hand DP	A
0792/0792TXV/0792TXVB		Numeric, Left Hand DP	B
0783/0783TXV/0783TXVB		Over Range ±1	C
0794/0794TXV/0794TXVB		Hexadecimal	D
0881/0881TXV/0881TXVB	Yellow	Numeric, Right Hand DP	A
0882/0882TXV/0882TXVB		Numeric, Left Hand DP	B
0883/0883TXV/0883TXVB		Over Range ±1	C
0884/0884TXV/0884TXVB		Hexadecimal	D

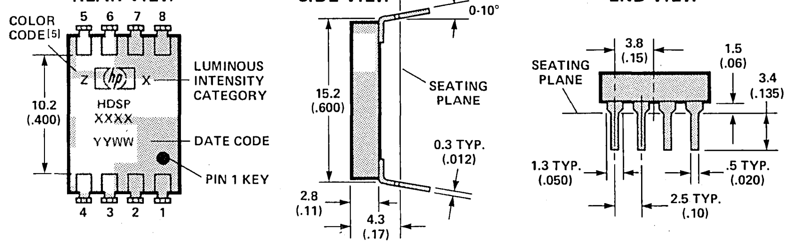
Package Dimensions

FRONT VIEW A · FRONT VIEW B · FRONT VIEW D



PIN	FUNCTION NUMERIC	FUNCTION HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

REAR VIEW · SIDE VIEW · END VIEW



Notes:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38 mm (±.015").
3. Digit center line is ±.25 mm (±.01") from package center line.
4. Lead material is gold plated copper alloy.
5. Color code for HDSP-088X series.

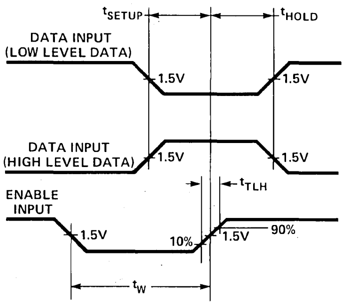


Figure 1. Timing Diagram

TRUTH TABLE					
BCD DATA[1]				NUMERIC	HEXA-DECIMAL
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	[illegible]	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	-	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

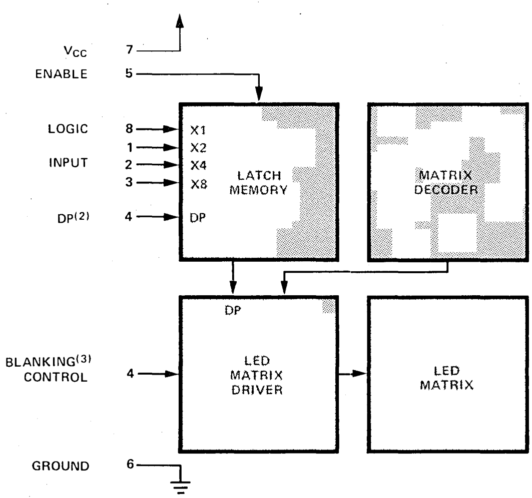


Figure 2. Logic Block Diagram

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels have no effect upon display memory, displayed character, or DP.
2. The decimal point input, DP, pertains only to the numeric displays.
3. The blanking control input, B, pertains only to the hexadecimal displays. Blanking input has no effect upon display memory.

SOLID STATE DISPLAYS

HI REL/HERMETIC COMPONENTS

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1]	T_A	−55	+100	°C
Supply voltage [2]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [2]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage [2]	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1]	T_A	-55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			1.0	msec

Optical Characteristics at $T_A = 25°C$, $V_{CC} = 5.0V$

Device	Description	Symbol	Min.	Typ.	Max.	Unit
HDSP-078X Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	65	140		µcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-079X Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	260	620		µcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-088X Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	215	490		µcd
	Peak Wavelength	λ_{PEAK}		583		nm
	Dominant Wavelength [5,6]	λ_d		585		nm

Notes:
1. The nominal thermal resistance of a display mounted in a socket that is soldered onto a printed circuit board is $R\theta_{JA} = 50°C/W$/device. The device package thermal resistance is $R\theta_{J-PIN} = 15°C/W$/device. The thermal resistance device pin-to-ambient through the PC board should not exceed 35° C/W/device for operation at $T_A = +100°C$.
2. Voltage values are with respect to device ground, pin 6.
3. These displays are categorized for luminous intensity with the intensity category designated by a letter code located on the back of the display package. Case temperature of the device immediately prior to the light measurement is equal to 25° C.

Electrical Characteristics; (T_A = -55° C to +100° C, unless otherwise specified)

Description		Symbol	Test Conditions	Min.	Typ.[7]	Max.	Unit
Supply Current	HDSP-078X Series	I_{CC}	V_{CC} = 5.5 V (Numeral 5 and DP Illuminated)		78	105	mA
	HDSP-079X Series HDSP-088X Series				120	175	
Power Dissipation	HDSP-078X Series	P_T	V_{CC} = 5.5 V (Numeral 5 and DP Illuminated)		390	573	mW
	HDSP-079X Series HDSP-088X Series				690	963	
Logic, Enable and Blanking Low-Level Input Voltage		V_{IL}	V_{CC} = 4.5 V			0.8	V
Logic, Enable High-Level Input Voltage		V_{IH}		2.0			V
Blanking High Voltage; Display Blanked		V_{BH}		2.3			V
Logic and Enable Low-Level Input Current		I_{IL}	V_{CC} = 5.5 V			-1.6	mA
Blanking Low-Level Input Current		I_{BL}	V_{IL} = 0.4 V			-10	μA
Logic, Enable and Blanking High-Level Input Current		I_{IH}	V_{CC} = 5.5 V V_{IH} = 2.4 V			+40	μA
Weight					1.0		gm
Leak Rate						5 x 10^{-8}	cc/sec.

Notes:

4. The luminous intensity at a specific operating ambient temperature, $I_V(T_A)$ may be approximated from the following expotential equation: $I_V(T_A) = I_V(25°C)\, e^{[K(T_A - 25°C)]}$

Device	K
HDSP-078X Series HDSP-079X Series	-0.0131/° C
HDSP-088X Series	-0.0112/° C

5. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
6. The HDSP-088X series devices are categorized as to dominant wavelength with the category designated by a number on the back side of the display package.
7. All typical values at V_{CC} = 5.0V and T_A = 25° C.

Operational Considerations

ELECTRICAL

These devices use a modified 4 x 7 dot matrix of light emitting diodes to display decimal/hexadecimal numeric information. The high efficiency red and yellow LEDs are GaAsP epitaxial layer on a GaP transparent substrate. The LEDs are driven by constant current drivers, BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7 MHz rate.

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The blanking control input on the hexadecimal displays blanks (turns off) the displayed information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 2.0 volts. When blanked, the display standby power is nominally 250 mW at T_A = 25° C.

MECHANICAL

These displays are hermetically sealed for use in environments that require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5 x 10^{-8} cc/sec.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54 mm (0.100 inch) and the lead row spacing is 15.24 mm (0.600 inch). These displays may be end stacked with 2.54 mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +70° C, it is important to maintain a base-to-ambient thermal resistance of less than 35° C watt/device as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or

Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

These displays are 100% preconditioned by 24 hour storage at 125°C.

CONTRAST ENHANCEMENT

These display devices are designed to provide an optimum ON/OFF contrast when placed behind an appropriate contrast enhancement filter. The following filters are suggested:

HIGH EFFICIENCY RED

Panelgraphic Scarlet Red 65
SGL Homalite H100-1670
3M Louvered Filter R6310

YELLOW

Panelgraphic Yellow 27
SGL Homalite H100-1720
3M Louvered Filter A5910

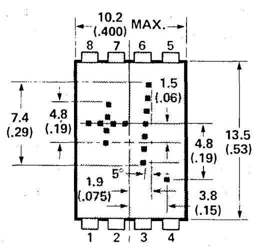
For many applications a neutral density gray filter in either plastic, circular polarizer or optically coated glass will provide the needed contrast enhancement. Suggested plastic neutral density gray filters are Panelgraphic Gray 10, SGL Homalite H100-1266 or 3M N0220. The optically coated glass/circular polarized SUNGARD filter by Optical Coating Laboratory, Inc., or the HNCP10 filter by Polaroid, provides superior contrast enhancement for very bright ambients.

Over Range Character

The over range devices display "±1" and decimal point. The character height and package configuration are the same as the numeric and hexadecimal devices. Character selection is obtained via external switching transistors and current limiting resistors.

Package Dimensions

FRONT VIEW C



Pin	Function
1	Plus
2	Numeral One
3	Numeral One
4	DP.
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

Note:
1. Dimensions in millimetres and (inches).

Character	Pin 1	Pin 2,3	Pin 4	Pin 8
+	1	X	X	1
—	0	X	X	1
1	X	1	X	X
Decimal Point	X	X	1	X
Blank	0	0	0	0

Notes:
0: Line switching transistor in Figure 7 cutoff.
1: Line switching transistor in Figure 7 saturated.
X: 'don't care'

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	-65	+125	°C
Operating Temperature Ambient	T_A	-55	+100	°C
Forward Current, Each LED	I_F		10	mA
Reverse Voltage, Each LED	V_R		5	V

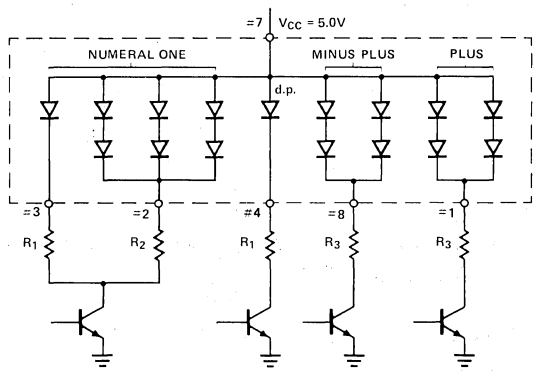


Figure 3. Typical Driving Circuit

Recommended Operating Conditions $V_{CC} = 5.0V$

Device		Forward Current Per LED, mA	Resistor Value R_1	R_2	R_3
HDSP-0783	Low Power	2.3	1300	200	300
	High Brightness	8	360	47	68
HDSP-0883		8	360	36	56

Luminous Intensity Per LED

(Digit Average) at $T_A = 25°C$

Device	Test Conditions	Min.	Typ.	Units
HDSP-0783	$I_F = 2.3$ mA	65	140	μcd
	$I_F = 8$ mA		620	μcd
HDSP-0883	$I_F = 8$ mA	215	490	μcd

Electrical Characteristics; (T_A = –55° C to +100° C, unless otherwise specified)

Device	Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
HDSP-0783	Power Dissipation (all LEDs Illuminated)	P_T	I_F = 2.8 mA		72		mW
			I_F = 8 mA		224	282	
	Forward Voltage per LED	V_F	I_F = 2.8 mA		1.6		V
			I_F = 8 mA		1.75	2.2	
HDSP-0883	Power Dissipation (all LEDs Illuminated)	P_T	I_F = 8 mA		237	282	mW
	Forward Voltage per LED	V_F			1.90	2.2	V

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa and IVa
HDSP-078X	HDSP-078XTXV	HDSP-078XTXVB
HDSP-079X	HDSP-079XTXV	HDSP-079XTXVB
HDSP-088X	HDSP-088XTXV	HDSP-088XTXVB

100% Screening

TABLE I.
QUALITY LEVEL A OF MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7572-52
2. High Temperature Storage	1032	T_A = 125° C, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 Cycles, 15 Min. Dwell
4. Constant Acceleration	2006	10,000 G at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C
7. Interim Electrical/Optical Tests[2]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} T_A = 25° C
8. Burn-In[1, 3]	1015	Condition B at V_{CC} = 5V and cycle through logic at 1 character per second. T_A = 100° C, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_V = -20%, ΔI_{CC} = ± 10 mA, ΔI_{IH} = ±10μA and ΔI_{EH} = ±13 μA
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. Burn-in for the over range display shall use Condition B at a nominal I_F = 8 mA with '+1' illuminated for t = 160 hours.

TABLE II
GROUP A ELECTRICAL TESTS — MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25° C[1]	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function, $T_A = 25°C$	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. $T_A = +100°C$	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. $T_A = -55°C$	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25° C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

1. Limits and conditions are per the electrical/optical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical[3]	2075		1 Device/ 0 Failures
Subgroup 2[1,2] Solderability	2026	$T_A = 245°C$ for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 min. Dwell	LTPD = 15
Moisture Resistance[3]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Electrical/Optical Endpoints[4]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual function. $T_A = 25°C$	
Subgroup 4 Operating Life Test (340 hrs.)[5]	1027	$T_A = +100°C$ at $V_{CC} = 5.0V$ and cycling through logic at 1 character per second.	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3.	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	$T_A = +125°C$	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Initial conditioning should be a 15° bent inward one cycle.
4. Limits and conditions are per the electrical/optical characteristics.
5. Burn-in for the over range display shall use Condition B at a nominal $I_F \pm 8$ mA with '+' illuminated for t = 160 hours.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual Function, $T_A = 25°C$	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			$\lambda = 10$
Operating Life Test[6]	1026	$T_A = +100°C$	
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C Life Test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.

HEWLETT PACKARD

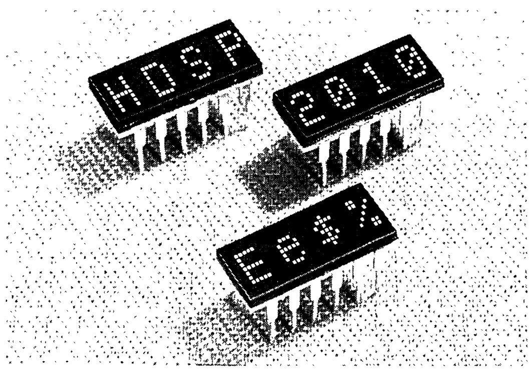
FOUR CHARACTER RED ALPHANUMERIC DISPLAY FOR EXTENDED TEMPERATURE APPLICATIONS

HDSP-2010
HDSP-2010TXV
HDSP-2010TXVB

TECHNICAL DATA JANUARY 1985

Features

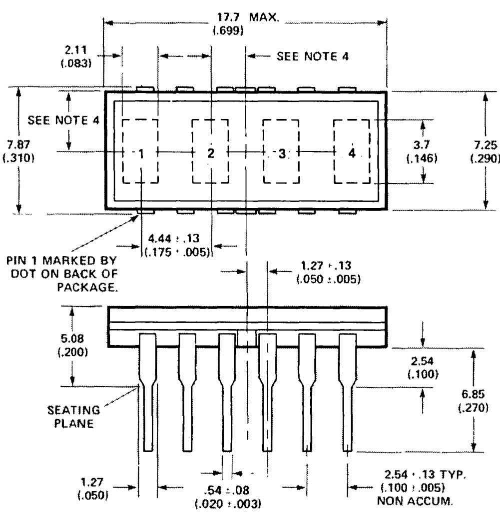
- OPERATION GUARANTEED TO T_A = -40°C
- LEAK RATE GUARANTEED
- TXVB VERSION CONFORMS TO QUALITY LEVEL A OF MIL-D-87157
- GOLD PLATED LEADS
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- CERAMIC 7.62mm (.3 in.) DIP
  Integral Red Glass Contrast Filter
- WIDE VIEWING ANGLE
- END STACKABLE 4 CHARACTER PACKAGE
- PIN ECONOMY
  12 Pins for 4 Characters
- TTL COMPATIBLE
- 5 x 7 LED MATRIX DISPLAYS FULL ASCII CODE
- RUGGED, LONG OPERATING LIFE
- CATEGORIZED FOR LUMINOUS INTENSITY
  Assures Ease of Package to Package Brightness Matching



Description

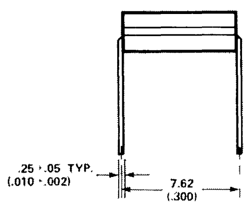
The HDSP-2010 display is designed for use in applications requiring high reliability. The character font is a 3.8mm (0.15 inch) 5 x 7 red LED array for displaying alphanumeric information. The device is available in 4 character clusters and is packaged in a 12-pin dual-in-line type package. An on-board SIPO (serial-in-parallel-out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing. The constant current LED drivers are externally programmable and typically capable of sinking 13.5mA peak per diode. Applications include interactive I/O terminals, avionics, portable telecommunications gear, and hand held equipment requiring alphanumeric displays.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE



NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015")
3. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.
4. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground .... −0.5V to 6.0V
Inputs, Data Out and V_B .... −0.5V to V_{CC}
Column Input Voltage, V_{COL} .... −0.5V to +6.0V
Free Air Operating Temperature
Range, T_A[2] .... −40° C to +85° C

Storage Temperature Range, T_S ..... -55° C to +100° C
Maximum Allowable Power Dissipation
at $T_A = 25°$ C[1,2,6] .... 1.29 Watts
Maximum Solder Temperature 1.59mm (.063")
Below Seating Plane t<5 secs .... 260° C

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, HighState	I_{OH}			−0.5	mA
Column Input Voltage, Column On	V_{COL}	2.6		3.5	V
Setup Time	t_{setup}	70	45		ns
Hold Time	t_{hold}	30	0		ns
Width of Clock	$t_{w(Clock)}$	75			ns
Clock Frequency	f_{clock}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating Temperature Range	T_A	-40		85	°C

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified.)

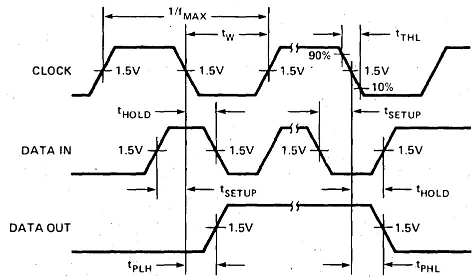
Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units
Supply Current		ICC	VCC = 5.25V VCLOCK = VDATA = 2.4V All SR Stages = Logical 1	VB = 0.4V		45	60	mA
				VB = 2.4V		73	95	mA
Column Current at any Column Input		ICOL	VCC = 5.25V VCOL = 3.5V All SR Stages = Logical 1	VB = 0.4V			500	μA
Column Current at any Column Input		ICOL		VB = 2.4V		350	435	mA
Peak Luminous Intensity per LED[3,7] (Character Average)		IvPEAK	VCC = 5.0V, VCOL = 3.5V Ti = 25° C[4] VB = 2.4V		105	200		μcd
VB, Clock or Data Input Threshold High		VIH	VCC = VCOL = 4.75V		2.0			V
VB, Data Input Threshold Low		VIL					0.8	V
Clock Threshold Low		VIL					0.6	V
Input Current Logical 1	VB, Clock	IIH	VCC = 5.25V, VIH = 2.4V			20	80	μA
	Data In	IIH				10	40	μA
Input Current Logical 0	VB, Clock	IIL	VCC = 5.25V, VIL = 0.4V			-500	-800	μA
	Data In	IIL				-250	-400	μA
Data Out Voltage		VOH	VCC = 4.75V, IOH = -0.5mA, VCOL = 0V		2.4	3.4		V
		VOL	VCC = 4.75V, IOL = 1.6mA, VCOL = 0V			0.2	0.4	V
Power Dissipation Per Package**		PD	VCC = 5.0V, VCOL = 3.5V 17.5% DF 15 LEDs on per character, VB = 2.4V			.74		W
Peak Wavelength		λPEAK				655		nm
Dominant Wavelength[5]		λd				640		nm
Thermal Resistance IC Junction-to-Case		RθJ-C				25		°C/W/ Device
Leak Rate							5x10⁻⁷	cc/s

***All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.**
****Power dissipation per package with 4 characters illuminated.**

1. Operation above 85° C ambient is possible provided the following conditions are met. The junction temperature should not exceed 125° C T_J and the case temperature as measured at pin 1 or the back of the display should not exceed 100° C T_C.
2. The device should be derated linearly above 50° C at 16.7 mW/° C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 35° C/W per device. See Figure 2 for power deratings based on a lower thermal resistances.
3. The characters are categorized for Luminous Intensity with the category designated by a letter code on the bottom of the package.
4. T_i refers to the initial case temperature of the device immediately prior to the light measurement.
5. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
6. Maximum allowable dissipation is derived from $V_{CC} = V_B$ = 5.25 Volts, V_{COL} = 3.5V, 20 LEDs on per character, 20% DF.
7. The luminous stearance of the LED may be calculated using the following relationships:
L_v (cd/m2) = I_v (Candela/A (Metre)2
L_v (Footlamberts) = πI_v (Candela)/A (Foot)2
A = 5.3×10^{-8} M2 = 5.8×10^{-7} (Foot)2

SOLID STATE DISPLAYS

HI REL/HERMETIC COMPONENTS



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics. (V_{CC} = 5V, T_A = -40°C to +70°C)

Mechanical and Thermal Considerations

The HDSP-2010 is available in a standard 12 lead ceramic-glass dual in-line package. It is designed for plugging into DIP sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size.

The HDSP-2010 can be operated over a wide range of temperature and supply voltages. Power reduction can be achieved by either decreasing V_{COL} or decreasing the average drive current through pulse width modulation of V_B.

The HDSP-2010 display has a glass lens. A front panel contrast filter is desirable in most actual display applications. Some suggested filters are Panelgraphic Ruby Red 60, SGL Homalite H100-1605 Red and 3M Light Control Film (louvered filters). OCLI Sungard optically coated glass filters offer superior contrast enhancement.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

Electrical Description

The HDSP-2010 display provides on-board storage of decoded column data and constant current sinking row drivers for each of 28 rows in the 4 character display. The device consists of four LED matrices and two integrated circuits that form a 28-bit serial input-parallel output (SIPO) shift register, see Figure 5. Each character is a 5 x 7 diode array arranged with the cathodes of each row connected to one constant current sinking output of the SIPO shift register. The anodes of each column are connected together, with the same column of each of the 4 characters connected together (i.e. column 1 of all four characters are connected to pin 1). Any LED within any character may be addressed by shifting data to the appropriate shift register location and applying a voltage to the appropriate column.

Associated with each shift register location is a constant current sinking LED driver, capable of sinking a nominal 13.5 mA. A logical 1 loaded into a shift register location enables the current source at that location. A voltage applied to the appropriate column input turns on the desired LED.

The display is column strobed on a 1 of 5 basis by loading 7 bits of row data per character for a selected column. The data is shifted through the SIPO shift register, one bit location for each high-to-low transition of the clock. When the HDSP-2010 display is operated with pin 1 in the lower left hand corner, the first bit that is loaded into the SIPO shift register will be the information for row 7 of the right most character. The 28th bit loaded into the SIPO shift register will be the information for row 1 of the left most character. When the 28 bits of row data for column 1 have been loaded into the SIPO shift register, the first column is energized for a time period, T, illuminating column 1 in all four characters. Column 1 is turned off and the process is repeated for columns 2 through 5.

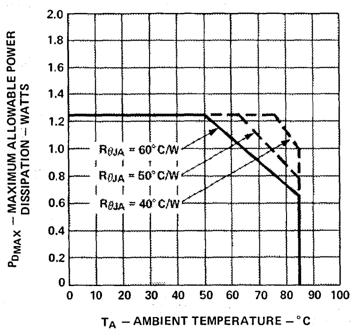


Figure 2. Maximum Allowable Power Dissipation vs. Temperature.

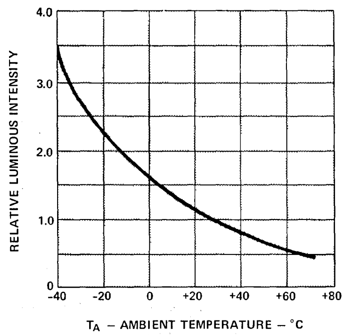


Figure 3. Relative Luminous Intensity vs. Temperature.

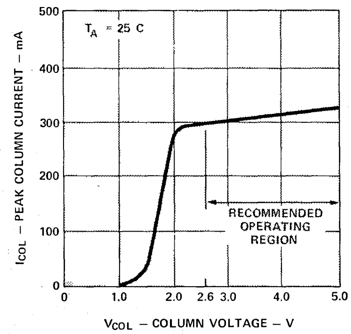


Figure 4. Peak Column Current vs. Column Voltage.

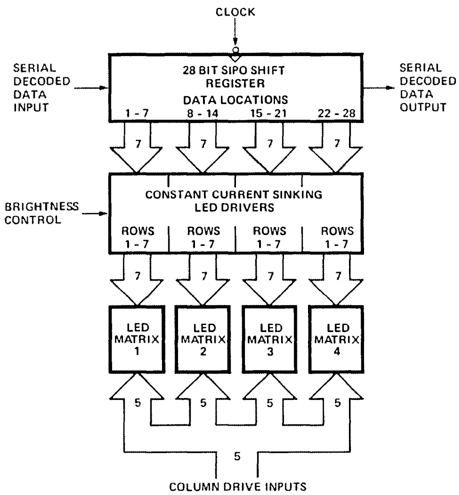


Figure 5. Block Diagram of the HDSP-2010 Display

The time frame allotted per column is (t + T) and the minimum recommended refresh rate for a flicker free display is 100 Hz, so that $(t + T) \leq 2$ ms. If the display is operated at the 3 MHz maximum clock rate, it is possible to maintain $t << T$. For display strings of 24 characters or less, the LED on time DF will be approximately 19.4%. For longer display strings, operation of the display with DF approximately 10% will provide adequate light output for indoor applications.

The 28th stage of the SIPO shift register is connected to the Data Output, which is designed to interface directly to the Data Input of the next HDSP-2010 in the display string.

The V_B input may be used to control the apparent brightness of the display. A logic high applied to the V_B input enables the display to be turned ON, and a logic low blanks the display by disabling the constant current LED drivers. Therefore, the time average luminous intensity of the display can be varied by pulse width modulation of V_B. For application and drive circuit information refer to HP Application Note 1016.

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa, and IVa
HDSP-2010	HDSP-2010 TXV	HDSP-2010 TXVB

100% Screening

TABLE I. QUALITY LEVEL A OF MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7512-52
2. High Temperature Storage	1032	$T_A = 100°C$, Time = 24 hours
3. Temperature Cycling	1051	$T_A = -55°C$ to $+100°C$, 10 cycles, 15 min. dwell
4. Constant Acceleration	2006	10,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H, Leak Rate $\leq 5 \times 10^{-7}$ cc/s
6. Gross Leak	1071	Condition C, except fluid temperature shall be $+100°C$
7. Interim Electrical/Optical Tests[2]	—	I_{CC} (at $V_B = 0.4V$ and $2.4V$), I_{COL} (at $V_B = 0.4V$ and $2.4V$) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} and I_V Peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. $T_A = 25°C$
8. Burn-In[1]	1015	Condition B at $V_{CC} = V_B = 5.25V$, $V_{COL} = 3.5V$, $T_A = +85°C$ LED ON-Time Duty Factor = 5%, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	$\Delta I_{CC} = \pm 6$ mA, ΔI_{IH} (clock) $= \pm 10\ \mu A$ ΔI_{IH} (Data In) $= \pm 10\ \mu A$ $\Delta I_{OH} = \pm 10\%$ of initial value and $\Delta I_V = -20\%$
11. External Visual	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

TABLE II
GROUP A ELECTRICAL TESTS MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1],	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test.	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = +85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = -40°C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

1. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical	2075		1 Device/ 0 Failures
Subgroup 2[1,2] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	T_A = -55°C to +100°C 15 min. dwell	LTPD = 15
Moisture Resistance[3]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C, except fluid temperature shall be +100°C	
Electrical/Optical Endpoints[4]	—	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, LED ON-Time Duty Factor = 5%	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +100°C	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Initial conditioning should be a 15° bent inward one cycle.
4. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1[1]			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C, except fluid temperature shall be +100° C	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{CC} (at V_B = 0.4V and 2.4V) I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In) I_{IL} (V_B, Clock and Data In) I_{OH}, I_{OL}, Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25° C.	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			
Operating Life Test[6]	1026	T_A = +85° C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

HEWLETT PACKARD

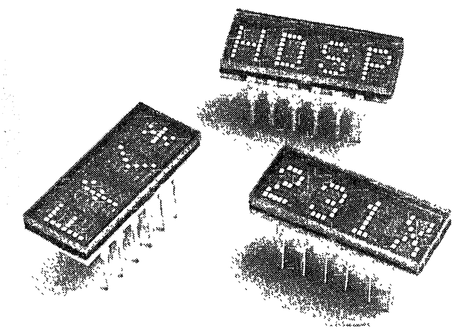
HERMETIC, EXTENDED TEMPERATURE RANGE 5.0mm (.20") 5x7 ALPHANUMERIC DISPLAYS

STANDARD RED HDSP-2310/2310TXV/2310TXVB
YELLOW HDSP-2311/2311TXV/2311TXVB
HIGH EFFICIENCY RED HDSP-2312/2312TXV/2312TXVB

TECHNICAL DATA JANUARY 1986

Features

- WIDE OPERATING TEMPERATURE RANGE -55°C TO +85°C
- TRUE HERMETIC PACKAGE
- TXVB VERSION CONFORMS TO QUALITY LEVEL A OF MIL-D-87157
- THREE COLORS
  Standard Red
  High Efficiency Red
  Yellow
- CATEGORIZED FOR LUMINOUS INTENSITY
- YELLOW DISPLAYS CATEGORIZED FOR COLOR
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- 5x7 LED MATRIX DISPLAYS FULL ASCII CHARACTER SET
- WIDE VIEWING ANGLE
- END STACKABLE
- TTL COMPATIBLE



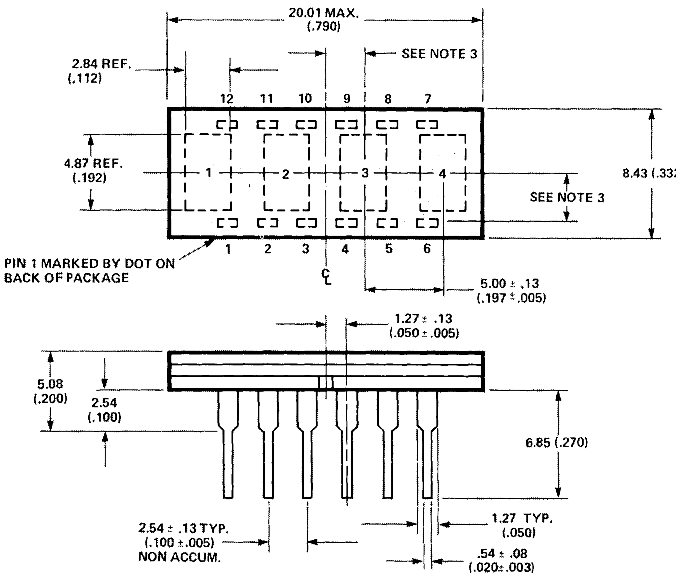
Typical Applications

- MILITARY EQUIPMENT
- AVIONICS
- HIGH RELIABILITY INDUSTRIAL EQUIPMENT

Description

The HDSP-2310 series displays are 5.0mm (0.20 in.) 5x7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow and high efficiency red. Each four character cluster is contained in a hermetic 12 pin dual-in-line, solder glass sealed ceramic package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

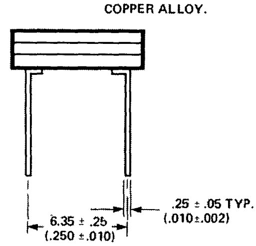
Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015")
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").
4. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.



Absolute Maximum Ratings (HDSP-2310/-2311/-2312)

Supply Voltage V_{CC} to Ground .... —0.5V to 6.0V
Inputs, Data Out and V_B .... —0.5V to V_{CC}
Column Input Voltage, V_{COL} .... —0.5V to +6.0V
Free Air Operating
Temperature Range, T_A[1,2] .... —55° C to +85° C
Storage Temperature Range, T_S ..... —65° C to +125° C
Maximum Allowable Power Dissipation
at T_A = 25° C[1,2,3] .... 1.46 Watts
Maximum Solder Temperature 1.59 mm (.063")
Below Seating Plane t < 5 secs .... 260° C

Recommended Operating Conditions (HDSP-2310/-2311/-2312)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1 6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2310	V_{COL}	2 4		3.5	V	4
Column Input Voltage, Column On HDSP-2311/-2312/-2313	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range [1,2]	T_A	-55		85	°C	

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V V_{CLOCK} = V_{DATA} = 2.4V All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V V_{COL} = 3.5V All SR Stages = Logical 1	V_B = 0.4V			500	µA	4
Column Current at any Column Input		I_{COL}		V_B = 2.4V		380	520	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = 4.75V		2.0			V	
V_B, Data Input Threshold Low		V_{IL}					0.8	V	
Clock Input Threshold Low		V_{IL}					0.6	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA	
	Data In	I_{IH}				10	40	µA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA	
	Data In	I_{IL}				-250	-400	µA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF 15 LEDs on per character, V_B = 2.4V			0.78		W	2
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				25		°C/W/ Device	2
Leak Rate							5×10^{-8}	cc/sec	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85°C ambient is possible provided the IC junction temperature, T_J, does not exceed 125°C.
2. The device should be derated linearly above 37°C at 16.7 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 35° C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

Optical Characteristics

STANDARD RED HDSP-2310

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25° C[6], V_B = 2.4V	220	370		μcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2311

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25° C[6], V_B = 2.4V	650	1140		μcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2312

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25° C[6], V_B = 2.4V	650	1430		μcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

*All typical values specified at V_{CC} = 5.0V and T_A = 25° C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2311 is categorized for color with the color category designated by a number code on the bottom of the package.
6. The luminous intensity is measured at $T_A = T_j$ = 25° C. No time is allowed for the device to warm-up prior to measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:
   L_V (cd/m2) = I_V (Candela)/A (Metre)2
   L_V (Footlamberts) = πI_V = (Candela)/A (Foot)2
   A = 5.3 x 10^{-8} M2 = 5.8 x 10^{-7} (Foot)2

Electrical Description

The HDSP-2310 series of four charater alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character module is arranged as a 28 bit serial in parallel out shift register as is shown in Figure 5. The display module features Data In and Data Out terminals arrayed for easy PC board interconnection. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5x7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

In the normal mode of operation, input data for digit 4, column 1 is loaded into the 7 on-board shift register locations 1 through 7. Column 1 data for digits 3, 2, and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5\,(t+T)}$$

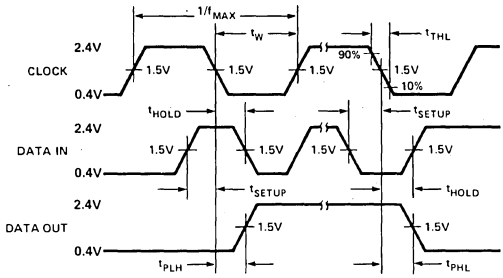
The time frame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With five columns to be addressed, this refresh rate then gives a value for the time t + T of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain t<<T. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics HDSP-2310/2311/-2312 (T_A = -55° C to +85° C)

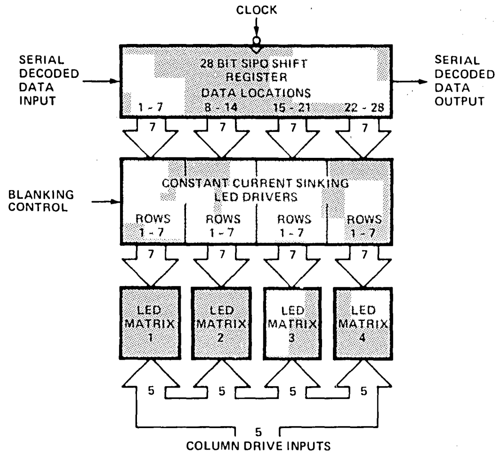


Figure 5. Block Diagram of HDSP-2310/-2311/-2312

Mechanical and Thermal Considerations

The HDSP-2310 series displays are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. HDSP-2310 series displays utilize a high output current IC to provide excellent readability in bright ambient lighting. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 60° C/watt/device is possible up to ambient temperature of 37° C. For operation above 37° C, the maximum device dissipation should be derated linearly at 16.7 mW/° C (see Figure 2). With an improved thermal design, operation at higher ambient temperatures without derating is possible.

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.4V for the HDSP-2310 and 2.75V for the HDSP-2311/-2312. Also, the average drive current can be decreased through pulse width modulation of V_B.

The HDSP-2310 series displays have integral glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 6. Additional information on filtering and contrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2310 Std. Red	Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Plexiglass 2423	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10	
HDSP-2311 (Yellow)	Panelgraphic Yellow 27 Chequers Amber 107	Chequers Grey 105	Polaroid HNCP10
HDSP-2312 (HER)	Panelgraphic Ruby Red 60 Chequers Red 112		

Figure 6. Contrast Enhancement Filters

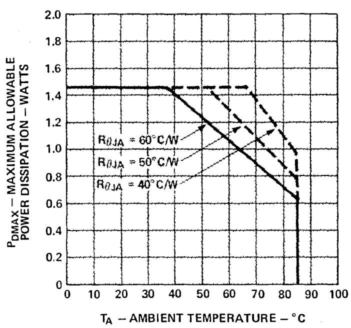


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

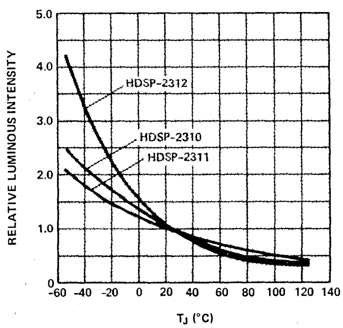


Figure 3. Relative Luminous Intensity vs. Temperature

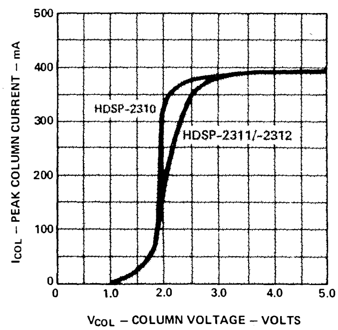


Figure 4. Peak Column Current vs. Column Voltage

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed LED displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Part Marking System

Standard Product	With Table I and II	With Tables I, II, IIIa, IVa
HDSP-2310 HDSP-2311 HDSP-2312	HDSP-2310 TXV HDSP-2311 TXV HDSP-2312 TXV	HDSP-2310 TXVB HDSP-2311 TXVB HDSP-2312 TXVB

100% Screening

Table I. Quality Level A of MIL-D-87157

Test Screen	Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7512-52, based on MIL-STD-883B
2. High Temperature Storage	MIL-STD-750 Method 1032	$T_A = 125°C$, Time = 24 hours
3. Temperature Cycling	MIL-STD-750 Method 1051	Condition B, 10 cycles, 15 min. dwell
4. Constant Acceleration	MIL-STD-750 Method 2006	10,000 G's at Y_1 orientation
5. Fine Leak	MIL-STD-750 Method 1071	Condition H
6. Gross Leak	MIL-STD-750 Method 1071	Condition C
7. Interim Electrical/Optical Tests[2]	—	I_{CC} (at $V_B = 0.4V$ and 2.4V), I_{COL} (at $V_B =$ 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} and I_V Peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. $T_A = 25°C$
8. Burn-In[1]	MIL-STD-883 Method 1015	Condition B at $V_{CC} = V_B = 5.25V$, $V_{COL} =$ 3.5V, $T_A = +85°C$, LED ON-Time Duty Factor = 5%, 35 Dots On; t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	$\Delta I_{CC} = \pm 6$ mA, ΔI_{IH} (clock) $= \pm 10\ \mu A$, ΔI_{IH} (Data In) $= \pm 10\ \mu A$ $\Delta I_{OH} = \pm 10\%$ of initial value, and $\Delta I_V = -20\%$, $T_A = 25°C$
11. External Visual	MIL-STD-883 Method 2009	

Notes:
1. MIL-STD-883 Test Method Applies
2. Limits and conditions are per the electrical optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table II. Group A Electrical Tests — MIL-D-87157

Subgroup/Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test.	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = +85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

Note:
1. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical	2075		1 Device/ 0 Failures
Subgroup 2[1,2]			
Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3			
Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 min. Dwell	LTPD = 15
Moisture Resistance[3]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Electrical/Optical Endpoints[4]	—	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C	
Subgroup 4			
Operating Life Test (340 hrs.)	1027	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, LED ON-Time Duty Factor = 5%, 35 Dots On	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	
Subgroup 5			
Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Initial conditioning should be a 15° bent inward one cycle.
4. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			
Lead Integrity	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{CC} (at V_B = 0.4V and 2.4V) I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In) I_{IL} (V_B, Clock and Data In) I_{OH}, I_{OL}, Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C.	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			
Operating Life Test[6]	1026	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, 35 Dots On	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

HEWLETT PACKARD

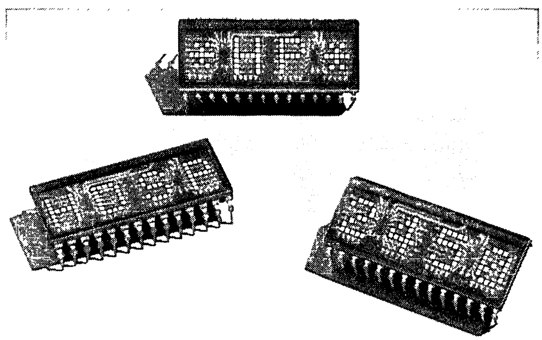
HERMETIC, EXTENDED TEMPERATURE RANGE 6.9mm (.27") 5x7 ALPHANUMERIC DISPLAYS

STANDARD RED HDSP-2450/2450TXV/2450TXVB
YELLOW HDSP-2451/2451TXV/2451TXVB
HIGH EFFICIENCY RED HDSP-2452/2452TXV/2452TXVB

TECHNICAL DATA JANUARY 1986

Features

- WIDE OPERATING TEMPERATURE RANGE -55° C TO +85° C
- TRUE HERMETIC PACKAGE
- TXVB VERSIONS CONFORM TO QUALITY LEVEL A OF MIL-D-87157
- THREE COLORS
  - Standard Red
  - High Efficiency Red
  - Yellow
- CATEGORIZED FOR LUMINOUS INTENSITY
- YELLOW DISPLAYS CATEGORIZED FOR COLOR
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- 5x7 LED MATRIX DISPLAYS FULL ASCII CHARACTER SET
- WIDE VIEWING ANGLE
- END STACKABLE
- TTL COMPATIBLE



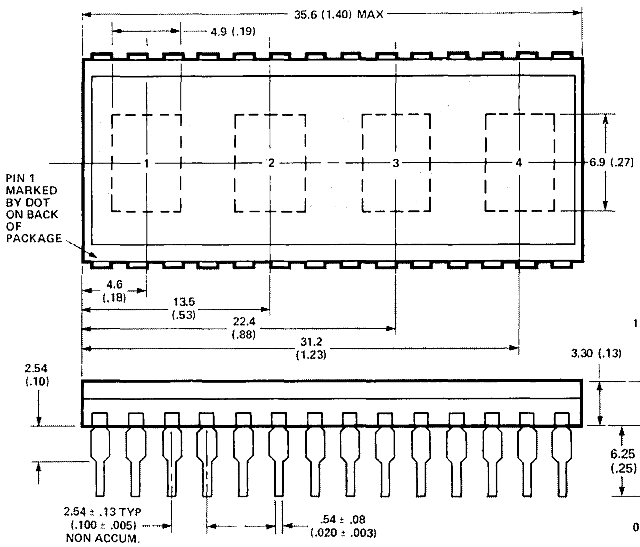
Typical Applications

- MILITARY EQUIPMENT
- AVIONICS
- HIGH RELIABILITY INDUSTRIAL EQUIPMENT

Description

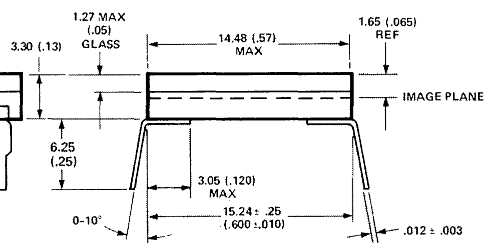
The HDSP-2450 series displays are 6.9mm (0.27 in.) 5x7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow, high efficiency red and high performance green. Each four character cluster is contained in a hermetic 28 pin dual-in-line, solder glass sealed ceramic package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions



PIN	FUNCTION[1]	PIN	FUNCTION
1	NO CONNECT	15	NO CONNECT
2	COLUMN 1	16	DATA OUT
3	COLUMN 1	17	DATA OUT
4	COLUMN 2	18	V_B
5	COLUMN 2	19	V_B
6	COLUMN 3	20	V_{CC}
7	COLUMN 3	21	V_{CC}
8	COLUMN 4	22	CLOCK
9	COLUMN 4	23	CLOCK
10	COLUMN 5	24	GROUND
11	COLUMN 5	25	GROUND
12	INT. CONNECT[2]	26	DATA IN
13	INT. CONNECT[2]	27	DATA IN
14	NO CONNECT	28	NO CONNECT

NOTES:
1. ALL USEABLE FUNCTION PINS ARE REDUNDANT ELECTRICAL CONNECTION CAN BE MADE TO EITHER PIN OR BOTH
2. DO NOT CONNECT OR USE.
3. DIMENSIONS IN mm (INCHES).
4. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ± .38 mm (± .015 INCHES).
5. LEAD MATERIAL IS GOLD PLATED IRON ALLOY.



SOLID STATE DISPLAYS

HI REL/HERMETIC COMPONENTS

Absolute Maximum Ratings (HDSP-2450/-2451/-2452)

Supply Voltage V_{CC} to Ground .... —0.5V to 6.0V
Inputs, Data Out and V_B .... —0.5V to V_{CC}
Column Input Voltage, V_{COL} .... —0.5V to +6.0V
Free Air Operating
Temperature Range, T_A[1,2] .... —55°C to +85°C

Storage Temperature Range, T_S ..... —65°C to +125°C
Maximum Allowable Package Dissipation
at T_A = 25°C[1,2,3] .... 1.46 Watts
Maximum Solder Temperature 1.59 mm (0.063")
Below Seating Plane t < 5 secs .... 260°C

Recommended Operating Conditions (HDSP-2450/-2451/-2452)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2450	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On HDSP-2451/2452/2453	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range[1,2]	T_A	-55		85	°C	

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V V_{CLOCK} = V_{DATA} = 2.4V All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V V_{COL} = 3.5V	V_B = 0.4V			500	µA	4
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		380	520	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = 4.75V		2.0			V	
V_B, Data Input Threshold Low		V_{IL}					0.8	V	
Clock Input Threshold Low		V_{IL}					0.6	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA	
	Data In	I_{IH}				10	40	µA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA	
	Data In	I_{IL}				-250	-400	µA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF 15 LEDs on per character, V_B = 2.4V			0.78		W	2
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				20		°C/W/ Device	2
Leak Rate							5×10^{-8}	cc/sec	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85°C ambient is possible provided the IC junction temperature, T_J, does not exceed 125°C.
2. The device should be derated linearly above 60°C at 22.2 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 25°C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

Optical Characteristics (continued)

STANDARD RED HDSP-2450

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_j = 25°C$[6], $V_B = 2.4V$	220	370		μcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2451

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_j = 25°C$[6], $V_B = 2.4V$	850	1400		μcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2452

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_j = 25°C$[6], $V_B = 2.4V$	850	1530		μcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

*All typical values specified at $V_{CC} = 5.0V$ and $T_A = 25°C$ unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2451 is categorized for color with the color category designated by a number code on the bottom of the package.
6. The luminous intensity is measured at $T_A = T_j = 25°C$. No time is allowed for the device to warm-up prior to measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:
   L_v (cd/m²) = I_v (Candela)/A (Metre)²
   L_v (Footlamberts) = πI_v (Candela)/A (Foot)²
   $A = 5.3 \times 10^{-8}$ M² = 5.8×10^{-7} Foot²

Electrical Description

The HDSP-2450 series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5x7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation input data for digit 4, column 1 is loaded into the 7 on-board shift register locations 1 through 7. Column 1 data for digits 3, 2, and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5(t+T)}$$

The time frame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time t + T of:

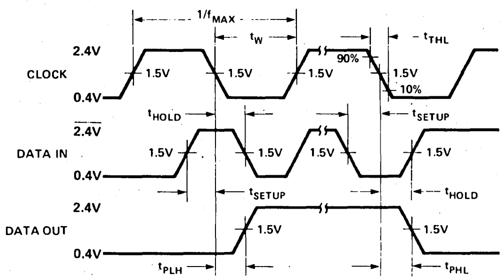
$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain t<<T. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.

SOLID STATE DISPLAYS

HI REL/HERMETIC COMPONENTS



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics HDSP-2450/-2451/-2452 (T_A = -55°C to +85°C)

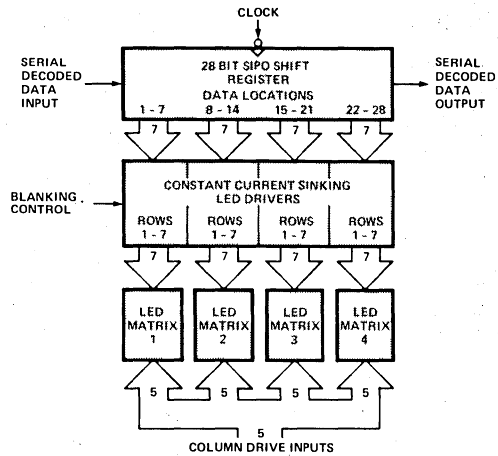


Figure 5. Block Diagram of HDSP-2450/-2451/-2452

Mechanical and Thermal Considerations

The HDSP-2450 series displays are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. HDSP-2450 series displays utilize a high output current IC to provide excellent readability in bright ambient lighting. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 45° C/watt/device is possible up to ambient temperature of 60° C. For operation above 60° C, the maximum device dissipation should be derated linearly at 22.2 mW/°C (see Figure 2). With an improved thermal design, operation at higher ambient temperatures without derating is possible.

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.4V for the HDSP-2450 and 2.75V for the HDSP-2451/-2452. Also, the average drive current can be decreased through pulse width modulation of V_B.

The HDSP-2450 series displays have glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 6. Additional information on filtering and contrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2450 Std. Red	Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Plexiglass 2423	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10	
HDSP-2451 (Yellow)	Panelgraphic Yellow 27 Chequers Amber 107	Chequers Grey 105	Polaroid HNCP10
HDSP-2452 (HER)	Panelgraphic Ruby Red 60 Chequers Red 112		

Figure 6. Contrast Enhancement Filters

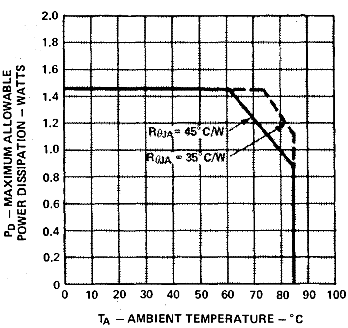


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

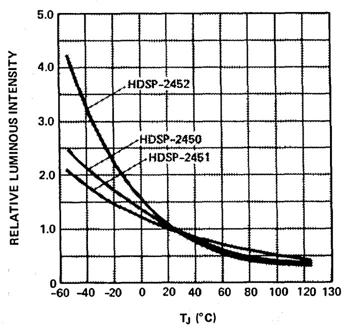


Figure 3. Relative Luminous Intensity vs. Temperature

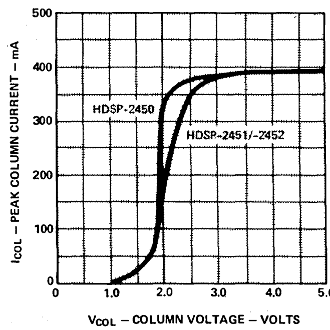


Figure 4. Peak Column Current vs. Column Voltage

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed LED displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Part Marking System

Standard Product	With Table I and II	With Tables I, II, IIIa, IVa
HDSP-2450 HDSP-2451 HDSP-2452	HDSP-2450 TXV HDSP-2451 TXV HDSP-2452 TXV	HDSP-2450 TXVB HDSP-2451 TXVB HDSP-2452 TXVB

100% Screening

Table I. Quality Level A of MIL-D-87157

Test Screen	Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7512-52, based on MIL-STD-883B
2. High Temperature Storage	MIL-STD-750 Method 1032	$T_A = 125°C$, Time = 24 hours
3. Temperature Cycling	MIL-STD-750 Method 1051	Condition B, 10 cycles
4. Constant Acceleration	MIL-STD-750 Method 2006	10,000 G's at Y_1 orientation
5. Fine Leak	MIL-STD-750 Method 1071	Condition H
6. Gross Leak	MIL-STD-750 Method 1071	Condition C
7. Interim Electrical/Optical Tests[2]	—	I_{CC} (at $V_B = 0.4V$ and 2.4V), I_{COL} (at $V_B =$ 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} and I_V Peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. $T_A = 25°C$
8. Burn-In	MIL-STD-883 Method 1015	Condition B at $V_{CC} = V_B = 5.25V$, $V_{COL} =$ 3.5V, $T_A = +85°C$, LED ON-Time Duty Factor = 5%, 35 dots On; t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	$\Delta I_{CC} = \pm 6$ mA, ΔI_{IH} (clock) $= \pm 8\ \mu A$, ΔI_{IH} (Data In) $= \pm 5\ \mu A$ $\Delta I_{OH} = \pm 50\ \mu A$, and $\Delta I_V = -20\%$, $T_A = 25°C$
11. External Visual	MIL-STD-883 Method 2009	

Notes:
1. MIL-STD-883 Test Method Applies
2. Limits and conditions are per the electrical optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table II. Group A Electrical Tests — MIL-D-87157

Subgroup/Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test.	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = +85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

Note:
1. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical	2075		1 Device/ 0 Failures
Subgroup 2[1,2] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 Min. Dwell	LTPD = 15
Moisture Resistance[3]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Electrical/Optical Endpoints[4]	—	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, LED ON-Time Duty Factor = 5%, 35 Dots On	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Initial conditioning should be a 15° bent inward one cycle.
4. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IVa. Group C, Class A and B of MIL-D-87157

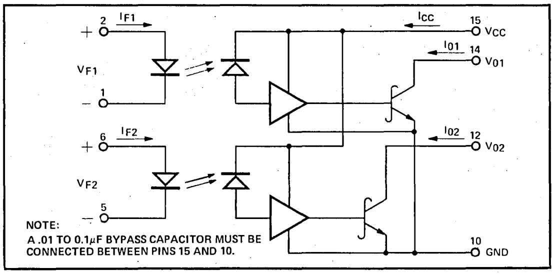
Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			
Lead Integrity	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{CC} (at V_B = 0.4V and 2.4V) I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In) I_{IL} (V_B, Clock and Data In) I_{OH}, I_{OL}, Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C.	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			
Operating Life Test[6]	1026	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, 35 Dots On	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

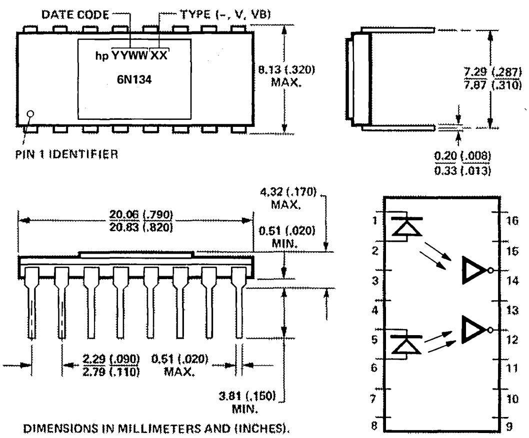
DUAL CHANNEL HERMETICALLY SEALED OPTOCOUPLER

6N134

TECHNICAL DATA JANUARY 1986



OUTLINE DRAWING*



DIMENSIONS IN MILLIMETERS AND (INCHES).

Features

- PERFORMANCE GUARANTEED OVER -55° C TO +125° C AMBIENT TEMPERATURE RANGE
- HERMETICALLY SEALED
- HIGH SPEED
- TTL COMPATIBLE INPUT AND OUTPUT
- HIGH COMMON MODE REJECTION
- DUAL-IN-LINE PACKAGE
- 1500 VDC WITHSTAND TEST VOLTAGE
- EIA REGISTRATION
- HIGH RADIATION IMMUNITY

Applications

- Logic Ground Isolation
- Line Receiver
- Computer — Peripheral Interface
- Vehicle Command/Control Isolation
- Harsh Industrial Environments
- System Test Equipment Isolation

Description

The 6N134 consists of a pair of inverting optically coupled gates, each with a light emitting diode and a unique high gain integrated photon detector in a hermetically sealed ceramic package. The output of the detector is an open collector Schottky clamped transistor.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving TTL circuit compatibility. The isolator operational parameters are guaranteed from –55° C to +125° C, such that a minimum input current of 10 mA in each channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

Hewlett-Packard's high reliability part type 8102801EC meets Class B testing requirements of MIL-STD-883. This part is the recommended and preferred device from the 6N134 product family for use in high reliability applications. Details of the 8102801EC test program may be seen in the data sheet for this part.

See the selection guide at the front of this section for other devices in this family.

Recommended Operating Conditions

TABLE I

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	12.5†	20	mA
Supply Voltage	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		6	
Operating Temperature	T_A	–55	125	°C

Absolute Maximum Ratings*

(No derating required up to 125°C)

Storage Temperature .... -65°C to +150°C
Operating Temperature .... -55°C to +125°C
Lead Solder Temperature .... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current (each channel) .... 40 mA (≤ 1 ms Duration)
Average Input Forward Current (each channel) ..... 20 mA
Input Power Dissipation (each channel) .... 35 mW
Reverse Input Voltage (each channel) 5V
Supply Voltage - V_{CC} .... 7V (1 minute maximum)
Output Current - I_O (each channel) .... 25 mA
Output Power Dissipation (each channel) .... 40 mW
Output Voltage - V_O (each channel) 7V
Total Power Dissipation (both channels) .... 350 mW

†12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10mA or less.

*JEDEC Registered Data

TABLE II

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = –55°C TO +125°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}*		5	250	µA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250µA		1
Low Level Output Voltage	V_{OL}*		0.4	0.6	V	V_{CC} = 5.5V, I_F = 10mA I_{OL} (Sinking) = 10mA	4	1, 9
High Level Supply Current	I_{CCH}*		18	28	mA	V_{CC} = 5.5V, I_F = 0 (Both Channels)		
Low Level Supply Current	I_{CCL}*		26	36	mA	V_{CC} = 5.5V, I_F = 20mA (Both Channels)		
Input Forward Voltage	V_F*		1.5	1.75	V	I_F = 20 mA, T_A = 25°C	1	1
	V_F			1.85	V	I_F = 20 mA	1	1
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10µA, T_A = 25°C		1
Input-Output Insulation Leakage Current	$I_{I\text{-}O}$*			1.0	µA	$V_{I\text{-}O}$ = 1500Vdc, Relative Humidity = 45% T_A = 25°C, t = 5s		2, 10
Propagation Delay Time to High Output Level	t_{PLH}*		60	90	ns	C_L=15pF; R_L=510Ω	2,3	1, 5
	t_{PLH}			100		C_L=50pF; I_F=13mA, T_A=25°C		
Propagation Delay Time to Low Output Level	t_{PHL}*		55	90	ns	C_L=15pF; R_L=510Ω	2,3	1, 6
	t_{PHL}			100		C_L=50pF; I_F=13mA, T_A=25°C		

**All typical values are at V_{CC} = 5V, T_A = 25°C

TABLE III

Typical Characteristics AT T_A = 25°C, V_{CC} = 5V EACH CHANNEL

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.5		mV/°C	I_F = 20mA		1
Resistance (Input-Output)	$R_{I\text{-}O}$		10^{12}		Ω	$V_{I\text{-}O}$ = 500V		3
Capacitance (Input-Output)	$C_{I\text{-}O}$		1.7		pF	f = 1MHz		3
Input-Input Leakage Current	$I_{I\text{-}I}$		0.5		nA	Relative Humidity = 45% $V_{I\text{-}I}$ = 500V, t = 5s		4
Resistance (Input-Input)	$R_{I\text{-}I}$		10^{12}		Ω	$V_{I\text{-}I}$ = 500V		4
Capacitance (Input-Input)	$C_{I\text{-}I}$		0.55		pF	f = 1MHz		4
Output Rise Time (10-90%)	t_r		35		ns	R_L = 510Ω, C_L = 15pF I_F = 13mA		1
Output Fall Time (90-10%)	t_f		35		ns			
Common Mode Transient Immunity at High Output Level	CM_H		100		V/µs	V_{CM} = 10V (peak), V_O (min.) = 2V, R_L = 510Ω, I_F = 0mA	6	1, 7
Common Mode Transient Immunity at Low Output Level	CM_L		-400		V/µs	V_{CM} = 10V (peak), V_O (max.) = 0.8V R_L = 510Ω, I_F = 10mA	6	1, 8

NOTES:
1. Each channel.
2. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
3. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 10, 12, 14 and 15 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 5 and 6 shorted together.
5. The t_{PLH} propagation delay is measured from the 6.5 mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
7. CM_H is the max. tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_O > 2.0V).
8. CM_L is the max. tolerable common mode transient to assure that the output will remain in a low logic state (i.e., V_O < 0.8V).
9. It is essential that a byass capacitor (.01 to 0.1 µF, ceramic) be connected from pin 10 to pin 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm.
10. This is a momentary withstand test, not an operating condition.

*JEDEC Registered Data

OPTOCOUPLERS

HI REL/HERMETIC COMPONENTS

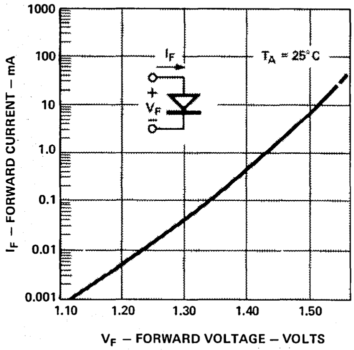


Figure 1. Input Diode Forward Characteristic

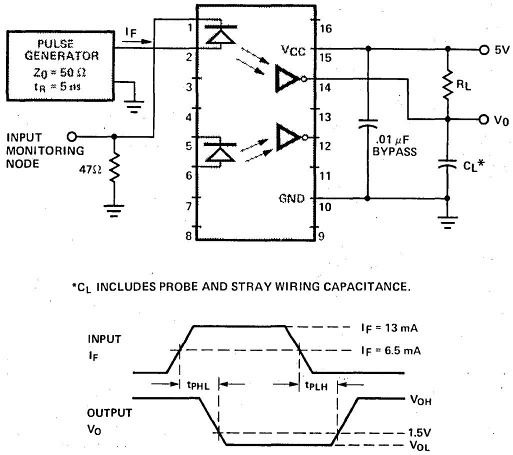


Figure 2. Test Circuit for t_{PHL} and t_{PLH}*

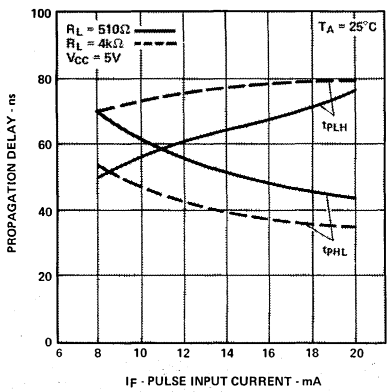


Figure 3. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}

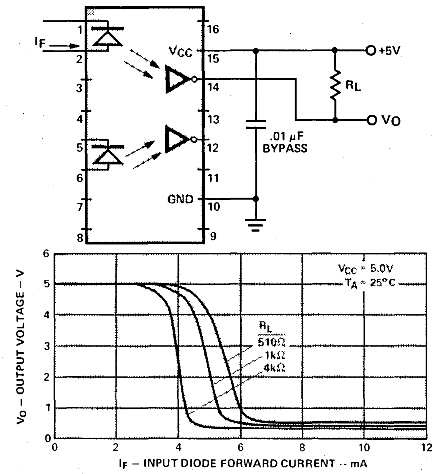


Figure 4. Input-Output Characteristics

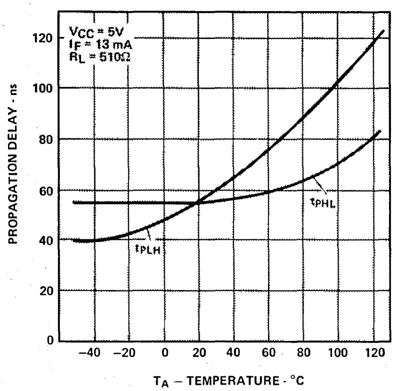


Figure 5. Propagation Delay vs. Temperature

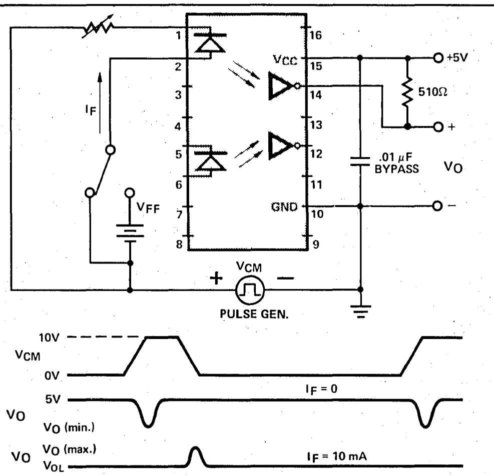


Figure 6. Typical Common Mode Rejection Characteristics/Circuit

*JEDEC Registered Data

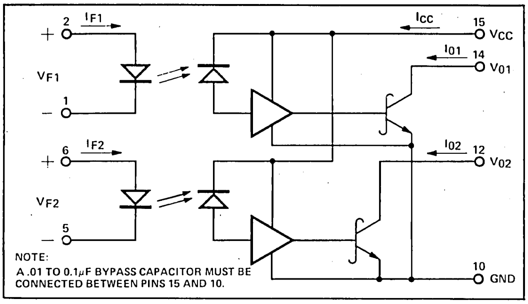
HEWLETT PACKARD

DUAL CHANNEL HERMETICALLY SEALED OPTOCOUPLER

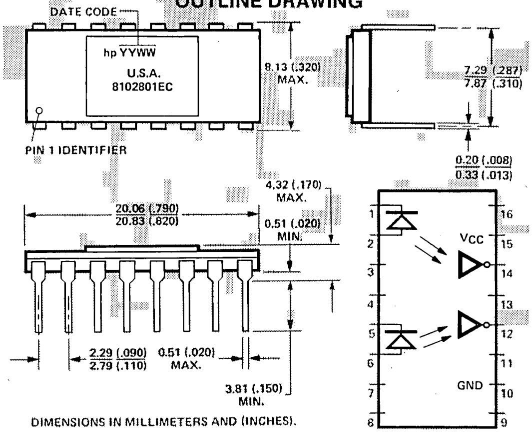
DESC APPROVED

8102801EC

TECHNICAL DATA JANUARY 1986



OUTLINE DRAWING



DIMENSIONS IN MILLIMETERS AND (INCHES).

Features

- RECOGNIZED BY DESC*
- HERMETICALLY SEALED
- MIL-STD-883 CLASS B TESTING
- HIGH SPEED
- PERFORMANCE GUARANTEED OVER -55° C TO +125° C AMBIENT TEMPERATURE RANGE
- TTL COMPATIBLE INPUT AND OUTPUT
- DUAL-IN-LINE PACKAGE
- 1500 VDC WITHSTAND TEST VOLTAGE
- HIGH RADIATION IMMUNITY

Applications

- MILITARY/HIGH RELIABILITY SYSTEMS
- LOGIC GROUND ISOLATION
- LINE RECEIVER
- COMPUTER — PERIPHERAL INTERFACE
- VEHICLE COMMAND/CONTROL ISOLATION
- SYSTEM TEST EQUIPMENT ISOLATION

Description

The 8102801EC is the DESC selected item drawing assigned by DOD for the 6N134 optocoupler which is in accordance with MIL-STD-883 class B testing. Operating characteristic curves for this part can be seen in the 6N134 data sheet.

The 8102801EC consists of a pair of inverting optically coupled gates, each with a light emitting diode and a unique high gain integrated photon detector in a hermetically sealed ceramic package. The output of the detector is an open collector Schottky clamped transistor.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving TTL circuit compatibility. The isolator operational parameters are guaranteed from -55° C to +125° C, such that a minimum input current of 10 mA in each channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

The photo ICs used in this device are less susceptible to radiation damage than PIN photo diodes or photo transistors due to their relatively thinner photo region.

The test program performed on the 8102801EC is in compliance with DESC drawing 81028 and the provisions of Method 5008, Class B of MIL-STD-883.

Recommended Operating Conditions

Supply Voltage	4.5 V dc minimum to 5.5 V dc maximum
High Level Input Current[1]	12.5 mA dc minimum (each channel)
Low Level Input Current	250 μA dc maximum (each channel)
Normalized Fanout (TTL Load)	6 maximum (each channel)
Operating Temperature Range	-55° C to +125° C

1. This condition permits at least 20 percent h_F (CTR) degradation. The initial switching threshold is 10 mA dc or less.

Absolute Maximum Ratings

Supply Voltage Range	7 V (1 minute maximum)
Input Current (each channel)	20 mA dc
Storage Temperature Range	-65° C to +150° C
Maximum Power Dissipation (both channels)	350 mW
Lead Temperature (soldering 10 seconds)	300° C for 10 seconds (1.6 mm below seating plane)
Junction Temperature (T_J)	175° C

*Defense Electronic Supply Center (DESC) is an agency of the Department of Defense (DOD).

100% Screening

MIL-STD-883, METHOD 5004 (CLASS B DEVICES)

Test Screen	Method	Conditions
1. Precap Internal Visual	2017	
2. High Temperature Storage	1008	Condition C, $T_A = 150°C$, Time = 24 hours minimum
3. Temperature Cycling	1010	Condition C, -65°C to +150°C, 10 cycles
4. Constant Acceleration	2001	Condition A, 5KG's, Y_1 axis only
5. Fine Leak	1014	Condition A
6. Gross Leak	1014	Condition C
7. Interim Electrical Test	—	Optional
8. Burn-In	1015	Condition B, Time = 160 hours minimum $T_A = +125°C$, $V_{CC} = 5.5V$, $I_F = 20$ mA, $I_O = 25$ mA (Figure 1)
9. Final Electrical Test Electrical Test Electrical Test	—	Group A, Subgroup 1, 5% PDA applies Group A, Subgroup 2 Group A, Subgroup 3
10. External Visual	2009	

Quality Conformance Inspection

GROUP A ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions	Group A Subgroups[6]	Limits Min.	Limits Max.	Unit
Low Level Output Voltage	V_{OL}	$V_{CC} = 5.5$ V; $I_F = 10$ mA[1]; $I_{OL} = 10$ mA	1, 2, 3	—	0.6	V
Current Transfer Ratio	h_F (CTR)	$V_O = 0.6$ V; $I_F = 10$ mA;[1] $V_{CC} = 5.5$ V	1, 2, 3	100	—	%
High Level Output Current	I_{OH}	$V_{CC} = 5.5$ V; $V_O = 5.5$ V[1]; $I_F = 250$ μA	1, 2, 3	—	250	μA dc
High Level Supply Current	I_{CCH}	$V_{CC} = 5.5$ V; $I_{F1} = I_{F2} = 0$ mA	1, 2, 3	—	28	mA dc
Low Level Supply Current	I_{CCL}	$V_{CC} = 5.5$ V; $I_{F1} = I_{F2} = 20$ mA	1, 2, 3	—	36	mA dc
Input Forward Voltage	V_F	$I_F = 20$ mA[1]	1, 2	—	1.75	V dc
			3	—	1.85	
Input Reverse Breakdown Voltage	V_{BR}	$I_R = 10$ μA[1]	1, 2, 3	5.0	—	V dc
Input to Output Insulation Leakage Current	I_{I-O}	$V_{IO} = 1500$ V dc[2]; Relative Humidity = 45 percent t = 5 seconds	1	—	1.0	μA dc
Capacitance Between Input/Output	C_{I-O}	f = 1 MHz; $T_C = 25°C$[3]	4	—	4.0	pF
Propagation Delay Time, Low to High Output Level	t_{PLH}	$R_L = 510$ Ω; $C_L = 50$ pF[1, 4]; $I_F = 13$ mA	9	—	100	ns
			10, 11	—	140	
Propagation Delay Time, High to Low Output Level	t_{PHL}	$R_L = 510$ Ω; $C_L = 50$ pF[1, 5]; $I_F = 13$ mA	9	—	100	ns
			10, 11	—	120	
Output Rise Time	t_{LH}	$R_L = 510$ Ω[1]; $C_L = 50$ pF; $I_F = 13$ mA	9, 10, 11	—	90	ns
Output Fall Time	t_{HL}			—	40	
Common Mode Transient Immunity at High Output Level	CM_H	$V_{CM} = 10$ V (peak);[1] $V_O = 2$ V (minimum); $R_L = 510$ Ω; $I_F = 0$ mA	9, 10, 11	40	—	V/μs
Common Mode Transient Immunity at Low Output Level	CM_L	$V_{CM} = 10$ V (peak);[1] $V_O = 0.8$ V (maximum); $R_L = 510$ Ω; $I_F = 10$ mA	9, 10, 11	-60	—	V/μs

See notes on following page.

Notes: 1. Each channel.
2. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
3. Measured between input pins 1 and 2, or 5 and 6 shorted together and output pins 10, 12, 14 and 15 shorted together.
4. The t_{PLH} propagation delay is measured from the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. Conditions of Group A subgroups may be seen in the High Reliability section of this catalog.
7. This is a momentary withstand test, not an operating condition.

GROUP B TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1 Physical Dimensions (Not required if Group D is to be performed)	2016		2 Devices (0 failures)
Subgroup 2 Resistance to Solvents	2015		4 Devices (0 failures)
Subgroup 3 Solderability (LTPD applies to number of leads inspected — no fewer than 3 devices shall be used).	2003	Soldering Temperature of 245 ± 5° C for 10 seconds	15 (3 Devices)
Subgroup 4 Internal Visual and Mechanical	2014		1 Device (0 failures)
Subgroup 5 Bond Strength Thermocompression: (Performed at precap, prior to seal LTPD applies to number of bond pulls from a minimum of 4 devices).	2011	Test Condition D	15 (4 Devices)
Subgroup 6 Internal Water Vapor Content (Not applicable — does not contain desiccant)	—		—
Subgroup 7 Fine Leak Gross Leak	1014	Condition A Condition C	5
Subgroup 8* Electrical Test		Group A, Subgroup 1, except I_{I-O}	15
Electrostatic Discharge Sensitivity	3015		
Electrical Test *(To be performed at initial qualification only)		Group A, Subgroup 1	

GROUP C TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1 Steady State Life Test	1005	Condition B, Time = 1000 hours total $T_A = +125°C$, $V_{CC} = 5.5$ V, $I_F = 20$ mA, $I_O = 25$ mA (Figure 1)	5
Endpoint Electricals at 1000 hours		Group A, Subgroup 1, 2, 3	
Subgroup 2 Temperature Cycling	1010	Condition C, -65° C to +150° C, 10 cycles	15
Constant Acceleration	2001	Condition A, 5KGs, Y_1 axis only	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per Visual Criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	

OPTOCOUPLERS

HI REL/HERMETIC COMPONENTS

GROUP D TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Test Condition B2 (lead fatigue)	15
Subgroup 3			
Thermal Shock	1011	Condition B, (-55°C to +125°C) 15 cycles min.	15
Temperature Cycling	1010	Condition C, (-65°C to +150°C) 100 cycles min.	
Moisture Resistance	1004		
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination		Per Visual Criteria of Method 1004	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	
Subgroup 4			
Mechanical Shock	2002	Condition B, 1500G, t = 0.5 ms, 5 blows in each orientation	15
Vibration Variable Frequency	2007	Condition A	
Constant Acceleration	2001	Condition A, 5KGs, Y_1 axis only	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per Visual Criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	
Subgroup 5			
Salt Atmosphere	1009	Condition A min.	15
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1009	Per Visual Criteria of Method 1009	
Subgroup 6			
Internal Water Vapor Content	1018	5000 ppm maximum water content at 100°C.	3 Devices (0 failures) 5 Devices (1 failure)
Subgroup 7			
Adhesion of Lead Finish	2025		15
Subgroup 8			
Lid Torque (not applicable — solder seal)	2024		5 Devices (0 failures)

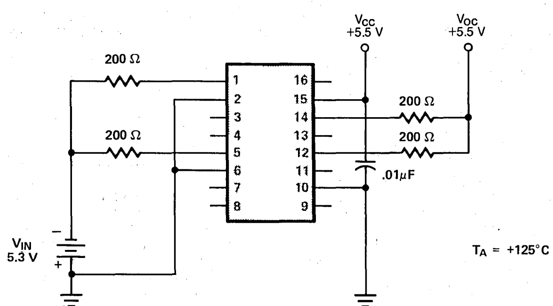


Figure 1. Operating Circuit for Burn-in and Steady State Life Tests.

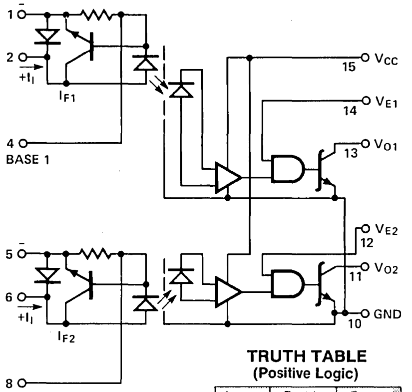
HEWLETT PACKARD

DUAL CHANNEL LINE RECEIVER HERMETIC OPTOCOUPLER

HCPL-1930
HCPL-1931
(883B)

TECHNICAL DATA JANUARY 1986

SCHEMATIC

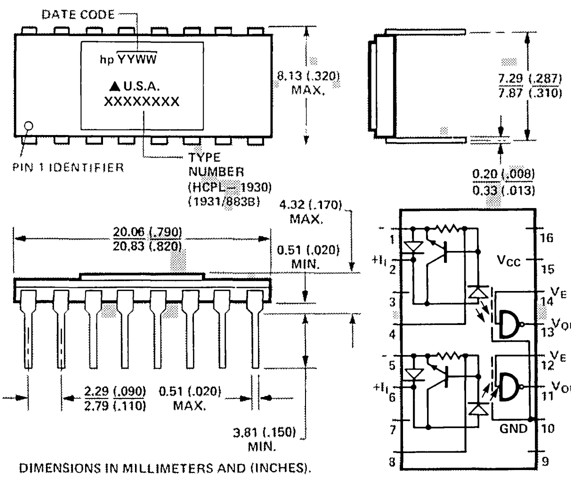


A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 10 AND 15 (See Note 1).

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

OUTLINE DRAWING



DIMENSIONS IN MILLIMETERS AND (INCHES).

Features

- HERMETICALLY SEALED
- MIL-STD-883 CLASS B TESTING
- HIGH SPEED — 10Mb/s
- PERFORMANCE GUARANTEED OVER -55° C TO +125° C AMBIENT TEMPERATURE RANGE
- ACCEPTS A BROAD RANGE OF DRIVE CONDITIONS
- LINE TERMINATION INCLUDED
- INTERNAL SHIELD PROVIDES EXCELLENT COMMON MODE REJECTION
- EXTERNAL BASE LEAD ALLOWS "LED PEAKING" AND LED CURRENT ADJUSTMENT
- 1500 Vdc WITHSTAND TEST VOLTAGE
- HIGH RADIATION IMMUNITY

Applications

- MILITARY/HIGH RELIABILITY SYSTEMS
- ISOLATED LINE RECEIVER
- SIMPLEX/MULTIPLEX DATA TRANSMISSION
- COMPUTER-PERIPHERAL INTERFACE
- MICROPROCESSOR SYSTEM INTERFACE
- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- CURRENT SENSING
- INSTRUMENT INPUT/OUTPUT ISOLATION
- GROUND LOOP ELIMINATION
- PULSE TRANSFORMER REPLACEMENT

Description

The HCPL-1930 and HCPL-1931 units are dual channel, hermetically sealed, high CMR, line receiver optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product (HCPL-1930) or with full MIL-STD-883 Class Level B testing (HCPL-1931). Both products are in sixteen pin hermetic dual in-line packages.

Each unit contains two independent channels, consisting of a GaAsP light emitting diode, an input current regulator, and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance.

(Continued on next page)

The regulator allows a typical LED current of 12.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of ±1000 V/μsec.

DC specifications are compatible with TTL logic and are guaranteed from -55°C to +125°C allowing trouble free interfacing with digital logic circuits. An input current of 10 mA will sink a six gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45nsec.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Recommended Operating Conditions (EACH CHANNEL)

	Sym.	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	μA
Input Current, High Level*	I_{IH}	12.5	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	3.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		6	
Operating Temperature	T_A	–55	125	°C

*12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10mA or less.

Absolute Maximum Ratings

Storage Temperature .... -65°C to +150°C
Operating Temperature .... -55°C to +125°C
Lead Solder Temperature .... 260°C for 10 s (1.6mm below seating plane)
Forward Input Current—I_I (Each Channel) ...... 60 mA[2]
Reverse Input Current .... 60 mA
Supply Voltage — V_{CC} .... 7V (1 Minute Maximum)
Enable Input Voltage — V_E (Each Channel) .... 5.5 V (Not to exceed V_{CC} by more than 500 mV)
Output Collector Current — I_O (Each Channel) .... 25 mA
Output Collector Power Dissipation (Each Channel). 40 mW
Output Collector Voltage — V_O (Each Channel) ...... 7 V
Total Package Power Dissipation .... 564 mW
Total Input Power Dissipation (Each Channel) ... 168 mW

Electrical Characteristics T_A = -55°C to +125°C, unless otherwise specified

Parameter	Symbol	Min.	Typ*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		20	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_I = 250μA, V_E = 3.0V	3	3
Low Level Output Voltage	V_{OL}		0.3	0.6	V	V_{CC} = 5.5V, I_I = 10mA, V_E = 3.0V, I_{OL} (Sinking) = 10 mA	1	3
Input Voltage	V_I		2.2	2.6	V	I_I = 10 mA	2	3
			2.35	2.75		I_I = 60mA	2	3
Input Reverse Voltage	V_R		0.8	1.10	V	I_R = 10mA		3
Low Level Enable Current	I_{EL}		-1.45	-2.0	mA	V_{CC} = 5.5V, V_E = 0.5V		3
High Level Enable Voltage	V_{EH}	2.0			V			3, 12
Low level Enable Voltage	V_{EL}			0.8	V			3
High Level Supply Current	I_{CCH}		21	28	mA	V_{CC} = 5.5V, I_I = 0, V_E = 0.5V both channels		
Low Level Supply Current	I_{CCL}		27	36	mA	V_{CC} = 5.5V, I_I = 60 mA, V_E = 0.5V both channels		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	Relative Humidity=45%, T_A = 25°C, t = 5 s, V_{I-O} = 1500 Vdc		4
Propagation Delay Time to High Output Level	t_{PLH}		45		ns	C_L = 15pF; R_L = 510Ω, I_I=13mA, T_A = 25°C	5	3, 5
			55	100		C_L = 50pF		
Propagation Delay Time to Low Output Level	t_{PHL}		55		ns	C_L = 15pF; R_L = 510Ω, I_I=13mA, T_A = 25°C	5	3, 6
			60	100		C_L = 50pF		
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	1000	10,000		V/μs	V_{CM} = 50 V (peak), V_O (min.)=2 V, T_A=25°C, R_L = 510Ω, I_I = 0 mA	7	3, 9
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	1000	10,000		V/μs	V_{CM} = 50 V (peak) V_O (max.) = 0.8 V, T_A=25°C, R_L = 510Ω, I_I = 10 mA	7	3, 10

*All typical values are at V_{CC} = 5V, T_A = 25°C.

Typical Characteristics $T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500$ Vdc		3, 13
Capacitance (Input-Output)	C_{I-O}	1.7	pF	f = 1 MHz		3, 13
Input-Input Insulation Leakage Current	I_{I-I}	0.5	nA	45% Relative Humidity, V_{I-I}=500 Vdc t = 5s.		11
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	$V_{I-I} = 500$ Vdc		11
Capacitance (Input-Input)	C_{I-I}	.55	pF	f = 1 MHz		11
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	35	ns	$R_L = 510Ω$, $C_L = 15pF$, $I_I = 13$ mA, $V_{EH} = 3$ V, $V_{EL} = 0$ V	6	3, 7
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	35	ns		6	3, 8
Output Rise Time (10-90%)	t_r	30	ns	$R_L = 510Ω$, $C_L = 15pF$,		3
Output Fall Time (90-10%)	t_f	24	ns	$I_I = 13$ mA		3
Input Capacitance	C_I	60	pF	f=1 MHz, V_I=0, PINS 1 to 2 or 5 to 6		3

NOTES:
1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Derate linearly at 1.2 mA/°C above $T_A = 100°C$.
3. Each channel.
4. Device considered a two terminal device: pins 1 through 8 are shorted together, and pins 9 through 16 are shorted together.
5. The t_{PLH} propagation delay is measured from the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{PLH} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
7. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e. V_{OUT}>2.0 V).
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e. V_{OUT}<0.8 V).
11. Measured between adjacent input leads shorted together, i.e. between 1, 2 and 4 shorted together and pins 5, 6 and 8 shorted together.
12. No external pull up is required for a high logic state on the enable input.
13. Measured between pins 1 and 2 or 5 and 6 shorted together, with pins 10 through 15 shorted together.

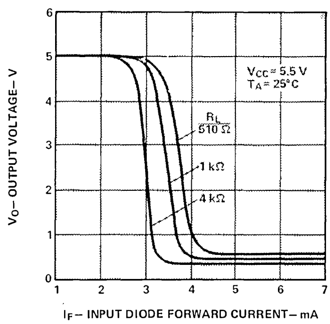


Figure 1. Input-Output Characteristics

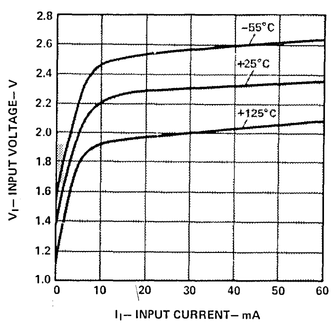


Figure 2. Input Characteristics.

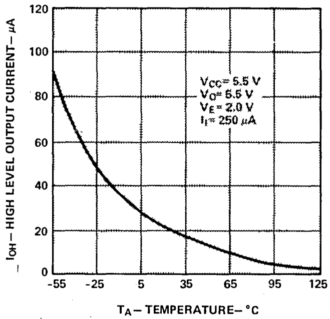


Figure 3. High Level Output Current vs. Temperature.

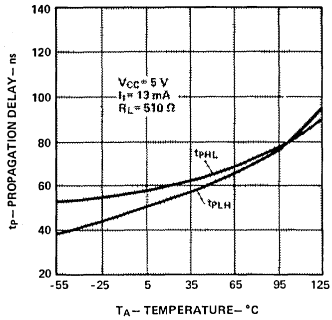


Figure 4. Propagation Delay vs. Temperature.

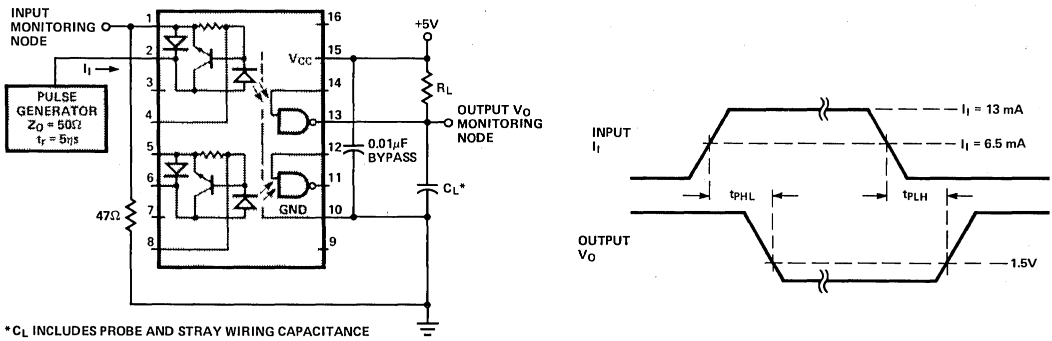


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.

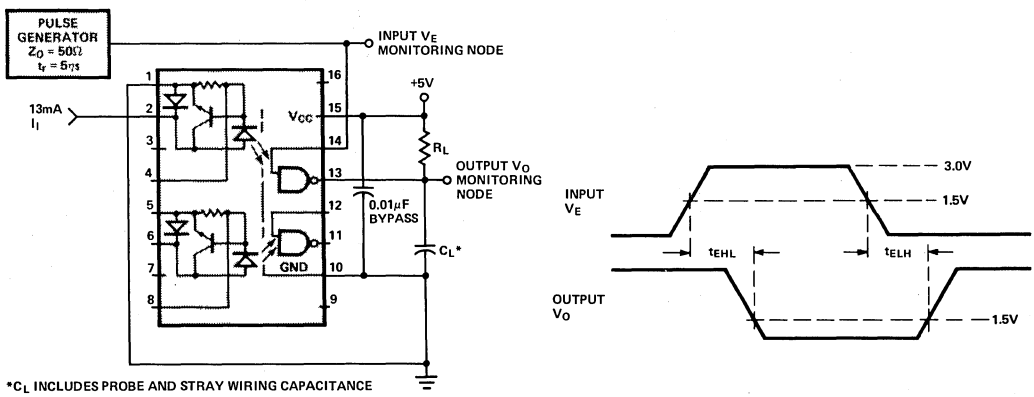


Figure 6. Test Circuit for t_{EHL} and t_{ELH}.

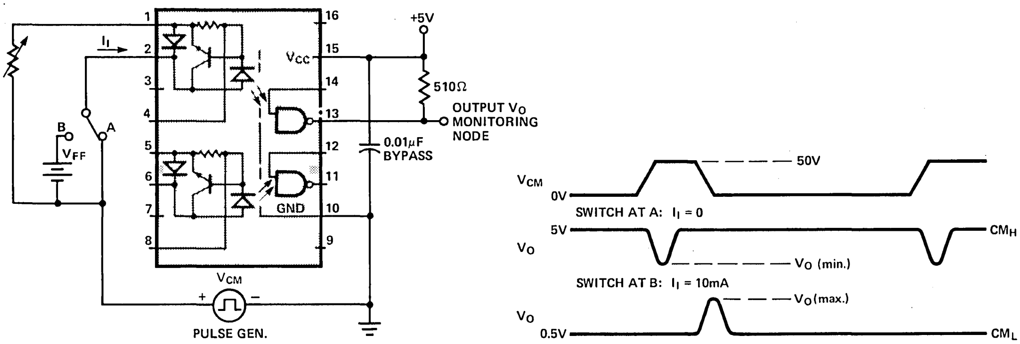


Figure 7. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

PART NUMBERING SYSTEM

Commercial Product	Class B Product
HCPL-1930	HCPL-1931

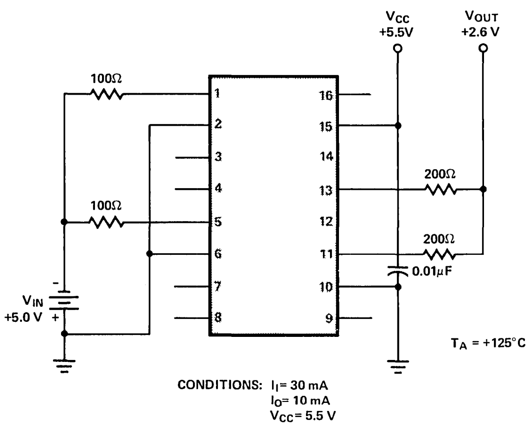


Figure 8. Burn In Circuit

MIL-STD-883 CLASS B TEST PROGRAM

Hewlett Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC drawing 81028 for an H.P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883. See the pages of this section entitled Hermetic Optocoupler MIL-STD-883 Class B Test Program for details of this test program.

HCPL-1931 Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration — Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.
   Group A — See table on next page for specific electrical tests.
   Group B — No change.
   Group C — Constant Acceleration — Condition A not E.
   Group D — Constant Acceleration — Condition A not E.

GROUP A

	LTPD
Subgroup 1 *Static tests at $T_A = 25°C$ — I_{OH}, V_{OL}, V_I, I_{CCH}, I_{CCL}, I_{EL}, V_{EH}, V_{EL}, V_R, $I_{I\text{-}O}$	2
Subgroup 2 *Static tests at $T_A = +125°C$ — I_{OH}, V_{OL}, V_I, I_{CCH}, I_{CCL}, I_{EL}, V_{EH}, V_{EL}, V_R	3
Subgroup 3 *Static tests at $T_A = -55°C$ — I_{OH}, V_{OL}, V_I, I_{CCH}, I_{CCL}, I_{EL}, V_{EH}, V_{EL}, V_R	5
Subgroup 4, 5, 6, 7 & 8 — These subgroups are non-applicable to this device type.	
Subgroup 9 *Switching tests at $T_A = 25°C$ — t_{PLH}, t_{PHL}, CM_H and CM_L	2
Subgroup 10 Switching tests at $T_A = +125°C$	3

Symbol	Max.	Units	Test Conditions
t_{PLH}	140	ns	$I_I = 13mAdc$, $R_L = 510\Omega$, $C_L = 50pF$
t_{PHL}	120	ns	$I_I = 13mAdc$, $R_L = 510\Omega$, $C_L = 50pF$

	LTPD
Subgroup 11 Switching tests at $T_A = -55°C$	5

Symbol	Max.	Units	Test Conditions
t_{PLH}	140	ns	$I_I = 13mAdc$, $R_L = 510\Omega$, $C_L = 50pF$
t_{PHL}	120	ns	$I_I = 13mAdc$, $R_L = 510\Omega$, $C_L = 50pF$

*Limits and conditions per Electrical Characteristics Table.

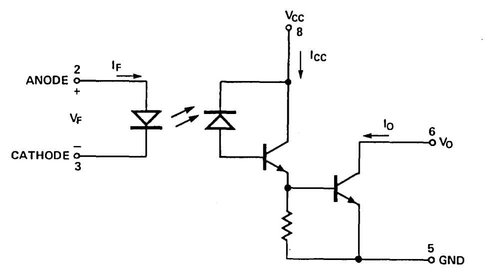
HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN, HERMETICALLY SEALED OPTOCOUPLER

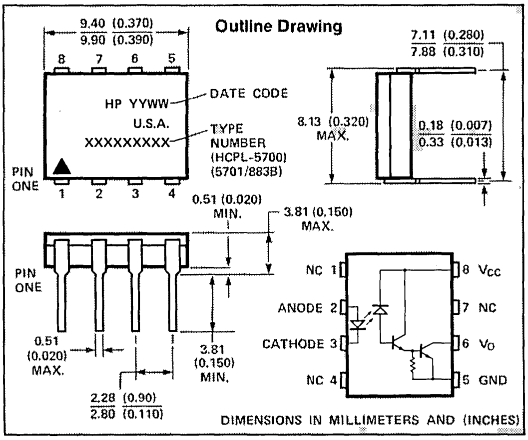
HCPL-5700
HCPL-5701
(883B)

TECHNICAL DATA JANUARY 1986

Schematic



Outline Drawing



Features

- HERMETICALLY SEALED 8 PIN DUAL IN-LINE PACKAGE
- PERFORMANCE GUARANTEED OVER −55° C TO +125° C AMBIENT TEMPERATURE RANGE
- MIL-STD-883 CLASS B TESTING
- 6N138, 6N139 AND 6N140A OPERATING COMPATIBILITY
- LOW INPUT CURRENT REQUIREMENT — 0.5 mA
- HIGH CURRENT TRANSFER RATIO — 1500% TYPICAL
- LOW OUTPUT SATURATION VOLTAGE — 0.11 V TYPICAL
- 500 Vdc WITHSTAND TEST VOLTAGE
- HIGH COMMON MODE REJECTION
- LOW POWER CONSUMPTION
- HIGH RADIATION IMMUNITY

Description

The HCPL-5700 and 5701 units are hermetically sealed, low input current, high gain optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product (HCPL-5700) or with full MIL-STD-883 Class Level B testing (HCPL-5701). Both products are in eight pin hermetic dual in-line packages.

Each unit contains an AlGaAs light emitting diode which is optically coupled to an integrated high gain photon detector. The high gain output stage features an open collector output providing both lower output saturation voltage and higher signaling speed than possible with conventional photo-darlington optocouplers.

The supply voltage can be operated as low as 2.0 V without adversely affecting the parametric performance.

The HCPL-5700 and HCPL-5701 have a 200% minimum CTR at an input current of only 0.5 mA making them ideal for use in low input current applications such as MOS, CMOS, low power logic interfaces or line receivers. Compatibility with high voltage CMOS logic systems is assured by the 18 V V_{CC}, V_{OH} current and the guaranteed maximum output leakage current at 18 V. The shallow depth and small junctions offered by the IC process provides better radiation immunity than conventional phototransistor optocouplers.

Upon special request, the following device selections can be made: CTR minimum of 300% to 600% at 0.5 mA, lower drive currents to 0.1 mA, and lower output leakage current levels to 100 μA.

Applications

- MILITARY/HIGH RELIABILITY SYSTEMS
- TELEPHONE RING DETECTION
- MICROPROCESSOR SYSTEM INTERFACE
- EIA RS-232-C LINE RECEIVER
- LEVEL SHIFTING
- DIGITAL LOGIC GROUND ISOLATION
- CURRENT LOOP RECEIVER
- ISOLATED INPUT LINE RECEIVER
- SYSTEM TEST EQUIPMENT ISOLATION
- PROCESS CONTROL INPUT/OUTPUT ISOLATION

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level	V_{FL}		0.7	V
Average Input Current High Level	I_{FH}	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings

Storage Temperature .... –65° C to +150° C
Operating Temperature .... –55° C to +125° C
Lead Solder Temperature .... 260° C for 10 sec. (1.6 mm below the seating plane)
Output Current I_O .... 40 mA
Output Voltage V_O .... –0.5 V to 20 V[1]
Supply Voltage V_{CC} .... –0.5 to 20 V[1]
Output Power Dissipation .... 50 mW[2]
Peak Input Current .... 8 mA
Reverse Input Voltage, V_R .... 5 V

Electrical Characteristics $T_A = -55°C$ to $125°C$, unless otherwise specified

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	200	1500		%	$I_F = 0.5$ mA, $V_O = 0.4$ V, $V_{CC} = 4.5$ V	3	3
		200	1000		%	$I_F = 1.6$ mA, $V_O = 0.4$ V, $V_{CC} = 4.5$ V		
		200	500		%	$I_F = 5$ mA, $V_O = 0.4$ V, $V_{CC} = 4.5$ V		
Logic Low Output Voltage	V_{OL}		0.11	0.4	V	$I_F = 0.5$ mA, $I_O = 1.0$ mA, $V_{CC} = 4.5$ V	2	
			0.13	0.4	V	$I_F = 1.6$ mA, $I_O = 3.2$ mA, $V_{CC} = 4.5$ V		
			0.16	0.4	V	$I_F = 5.0$ mA, $I_O = 10$ mA, $V_{CC} = 4.5$ V		
Logic High Output Current	I_{OH}		0.001	250	μA	$V_F = 0.7$ V, $V_O = V_{CC} = 18$ V		
Logic Low Supply Current	I_{CCL}		1.0	2.0	mA	$I_F = 1.6$ mA, $V_{CC} = 18$ V	4	
Logic High Supply Current	I_{CCH}		0.001	7.5	μA	$I_{F1} = 0$, $V_{CC} = 18$ V		
Input Forward Voltage	V_F	1.0	1.3	1.6	V	$I_F = 1.6$ mA, $T_A = 25°C$	1	
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10$ μA		
Input-Output Insulation Leakage Current	I_{I-O}			1.0	μA	45% Relative Humidity, $T_A = 25°C$ t = 5 sec, $V_{I-O} = 500$ Vdc		4, 5
Propagation Delay Time to Logic High At Output	t_{PLH}		17	185	μs	$I_F = 0.5$ mA, $R_L = 4.7$ kΩ, $V_{CC} = 5$ V	7,8	
			14	115	μs	$I_F = 1.6$ mA, $R_L = 2.2$ kΩ, $V_{CC} = 5$ V	7,8	
			8	60	μs	$I_F = 5.0$ mA, $R_L = 680$ Ω, $V_{CC} = 5$ V	7,8	
Propagation Delay Time to Logic Low At Output	t_{PHL}		10	185	μs	$I_F = 0.5$ mA, $R_L = 4.7$ kΩ, $V_{CC} = 5$ V	7,8	
			5	30	μs	$I_F = 1.6$ mA, $R_L = 2.2$ kΩ, $V_{CC} = 5$ V	7,8	
			2	12	μs	$I_F = 5.0$ mA, $R_L = 680$ Ω, $V_{CC} = 5$ V	7,8	
Common Mode Transient Immunity At Logic High Level Output	$\|CM_H\|$	500	≥2000		V/μs	$I_F = 0$, $R_L = 2.2$ kΩ $\|V_{CM}\| = 50\ V_{p-p}$, $V_{CC} = 5.0$ V, $T_A = 25°C$	9,10	6, 8
Common Mode Transient Immunity At Logic Low Level Output	$\|CM_L\|$	500	≥1000		V/μs	$I_F = 1.6$ mA, $R_L = 2.2$ kΩ $\|V_{CM}\| = 50\ V_{p-p}$, $V_{CC} = 5.0$ V, $T_A = 25°C$	9,10	7, 8

*All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

Typical Characteristics $T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500$ Vdc		9
Capacitance (Input-Output)	C_{I-O}	2.0	pF	f = 1 MHz		9
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	–1.5	mV/°C	$I_F = 1.6$ mA		
Input Capacitance	C_{IN}	15	pF	f = 1 MHz, $V_F = 0$		

NOTES:

1. GND Pin should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 V, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus one half of total supply power.
3. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
4. Device considered a two-terminal device. Pins 1 through 4 are shorted together and pins 5 through 8 are shorted together.
5. This is a momentary withstand test, not an operating condition.
6. CM_H is the maximum tolerable common mode transient such that the output will remain in a high logic state (i.e. $V_O > 2.0$ V).
7. CM_L is the maximum tolerable common mode transient such that the output will remain in a low logic state (i.e. $V_O < 0.8$ V).
8. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, is recommended to protect the detector IC from destructively high surge currents. The recommended maximum value is

$$R_{CC} \approx \frac{1V}{0.15\ I_F\ (mA)}\ k\Omega.$$

9. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.

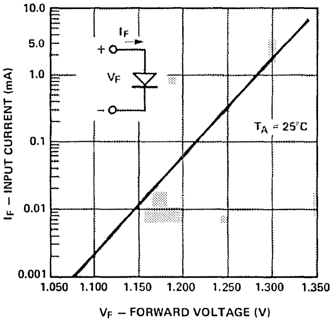


Figure 1. Input Current vs. Forward Voltage.

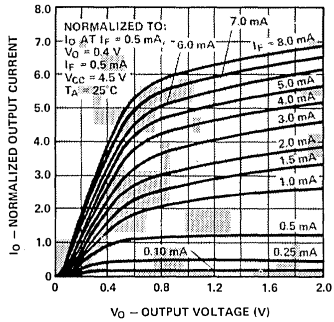


Figure 2. Normalized DC Transfer Characteristics.

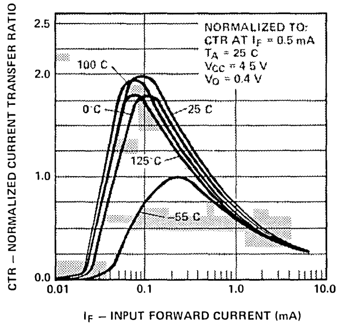


Figure 3. Normalized Current Transfer Ratio vs. Input Forward Current.

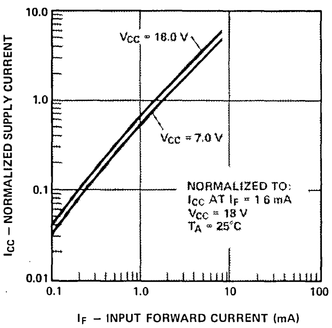


Figure 4. Normalized Supply Current vs. Input Forward Current.

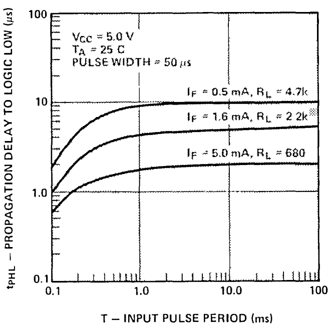


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

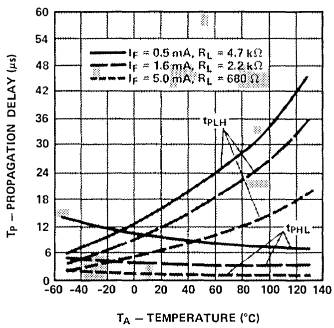


Figure 6. Propagation Delay vs. Temperature.

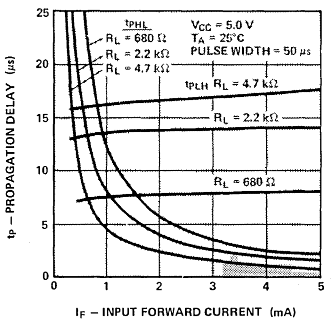


Figure 7. Propagation Delay vs. Input Forward Current.

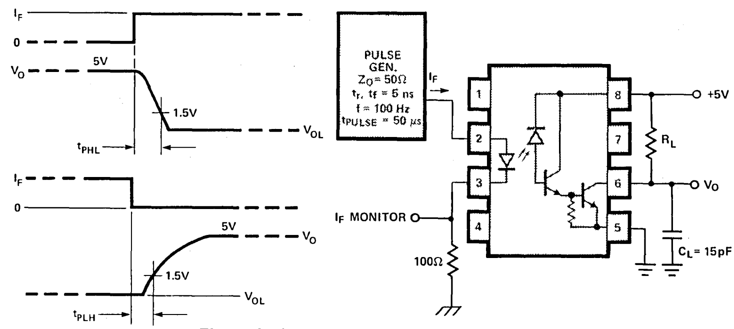


Figure 8. Switching Test Circuit

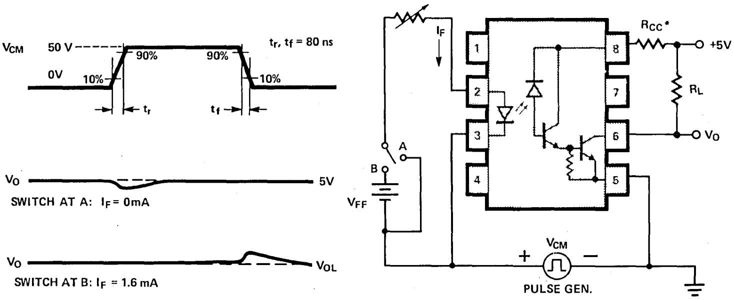


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms

*See Note 8

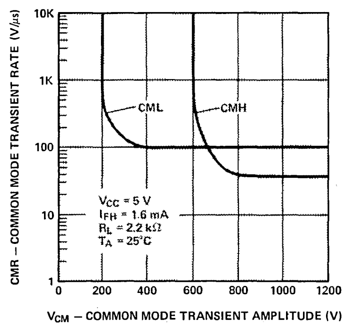


Figure 10. Common Mode Transient Immunity vs. Common Mode Transient Amplitude

MIL-STD-883 CLASS B TEST PROGRAM

Hewlett-Packard's HCPL-5701 optocoupler is in compliance with MIL-STD-883, Revision C. Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005. Details of these test programs may be found in the hermetic optocoupler product qualification section of Hewlett-Packard's Optoelectronics Designer's Catalog 1985.

See table below for specific electrical tests.

PART NUMBERING SYSTEM

Commercial Product	Class B Product
HCPL-5700	HCPL-5701

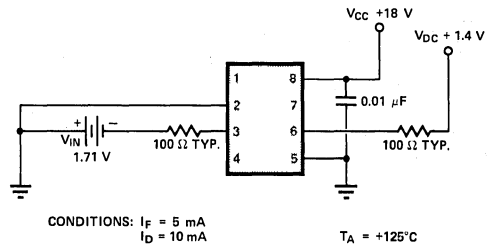


Figure 11. Operating Circuit for Burn-In and Steady State Life Tests

GROUP A — ELECTRICAL TESTS

Test					LTPD
Subgroup 1 *Static tests at $T_A = 25°C$ — I_{OH}, V_{OL}, I_{CCL}, I_{CCH}, CTR, V_F, BV_R and I_{I-O}					2
Subgroup 2 *Static tests at $T_A = +125°C$ — I_{OH}, V_{OL}, I_{CCL}, I_{CCH}, BV_R and CTR					3
Symbol	**Min.**	**Max.**	**Units**	**Test Conditions**	
V_F		1.8	V	$I_F = 1.6$ mA	
Subgroup 3 *Static tests at $T_A = -55°C$ — I_{OH}, V_{OL}, I_{CCL}, I_{CCH}, BV_R and CTR					5
Symbol	**Min.**	**Max.**	**Units**	**Test Conditions**	
V_F		1.8	V	$I_F = 1.6$ mA	
Subgroup 4, 5, 6, 7 and 8 These subgroups are not applicable to this device type.					
Subgroup 9 *Switching tests at $T_A = 25°C$ – t_{PLH1}, t_{PHL1}, t_{PLH2}, t_{PHL2}, t_{PLH3}, t_{PHL3}, CM_H and CM_L					2
Subgroup 10 *Switching tests at $T_A = +125°C$ – t_{PLH1}, t_{PHL1}, t_{PLH2}, t_{PHL2}, t_{PLH3}, t_{PHL3}					3
Subgroup 11 *Switching tests at $T_A = -55°C$ – t_{PLH1}, t_{PHL1}, t_{PLH2}, t_{PHL2}, t_{PLH3}, t_{PHL3}					5

*Limits and conditions per Table II.

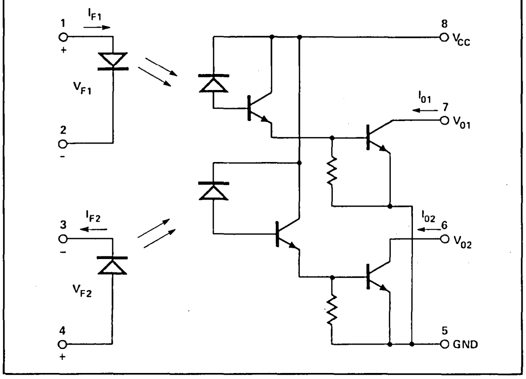
HEWLETT PACKARD

DUAL CHANNEL LOW INPUT CURRENT, HIGH GAIN, HERMETICALLY SEALED OPTOCOUPLER

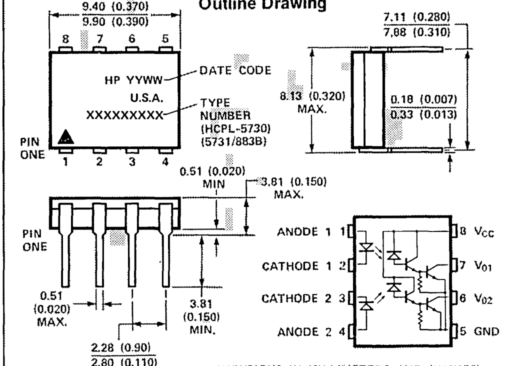
HCPL-5730
HCPL-5731
(883B)

TECHNICAL DATA JANUARY 1986

Schematic



Outline Drawing



Features

- **HERMETICALLY SEALED 8 PIN DUAL IN-LINE PACKAGE**
- **PERFORMANCE GUARANTEED OVER −55°C TO +125°C AMBIENT TEMPERATURE RANGE**
- **MIL-STD-883 CLASS B TESTING**
- **HCPL-2730/2731 AND 6N140A OPERATING COMPATIBILITY**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **HIGH CURRENT TRANSFER RATIO — 1500% TYPICAL**
- **LOW OUTPUT SATURATION VOLTAGE — 0.11 V TYPICAL**
- **500 Vdc WITHSTAND TEST VOLTAGE**
- **HIGH COMMON MODE REJECTION**
- **LOW POWER CONSUMPTION**
- **HIGH RADIATION IMMUNITY**

Applications

- **MILITARY/HIGH RELIABILITY SYSTEMS**
- **TELEPHONE RING DETECTION**
- **MICROPROCESSOR SYSTEM INTERFACE**
- **EIA RS-232-C LINE RECEIVER**
- **LEVEL SHIFTING**
- **DIGITAL LOGIC GROUND ISOLATION**
- **CURRENT LOOP RECEIVER**
- **ISOLATED INPUT LINE RECEIVER**
- **SYSTEM TEST EQUIPMENT ISOLATION**
- **PROCESS CONTROL INPUT/OUTPUT ISOLATION**

Description

The HCPL-5730 and HCPL-5731 units are dual channel, hermetically sealed, low input current, high gain optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product (HCPL-5730) or with full MIL-STD-883 Class Level B testing (HCPL-5731). Both products are in eight pin hermetic dual in-line packages.

Each unit contains two independent channels, consisting of an AlGaAs light emitting diode optically coupled to an integrated high gain photon detector. The high gain output stage features an open collector output providing both lower output saturation voltage and higher signaling speed than possible with conventional photo-darlington optocouplers.

The supply voltage can be operated as low as 2.0 V without adversely affecting the parametric performance.

The HCPL-5730 and HCPL-5731 have a 200% minimum CTR at an input current of only 0.5 mA making them ideal for use in low input current applications such as MOS, CMOS, low power logic interfaces or line receivers. Compatibility with high voltage CMOS logic systems is assured by the 18 V V_{CC}, V_{OH} current and the guaranteed maximum output leakage current at 18 V. The shallow depth and small junctions offered by the IC process provides better radiation immunity than conventional phototransistor optocouplers.

Upon special request, the following device selections can be made: CTR minimum of 300% to 600% at 0.5 mA, lower drive currents to 0.1 mA, and lower output leakage current levels to 100 μA.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level (Each Channel)	V_{FL}		0.7	V
Average Input Current High Level (Each Channel)	I_{FH}	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings

Storage Temperature .... −65° C to +150° C
Operating Temperature .... −55° C to +125° C
Lead Solder Temperature .... 260° C for 10 sec. (1.6 mm below the seating plane)
Output Current I_O (Each Channel) .... 40 mA
Output Voltage V_O (Each Channel) ..... −0.5 V to 20 V[1]
Supply Voltage V_{CC} .... −0.5 to 20 V[1]
Output Power Dissipation (Each Channel) .... 50 mW[2]
Peak Input Current (Each Channel) .... 8 mA
Reverse Input Voltage, V_R (Each Channel) .... 5 V

Electrical Characteristics $T_A = -55°C$ to $125°C$, unless otherwise specified

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	200 200 200	1500 1000 500		% % %	$I_F = 0.5$ mA, $V_O = 0.4$ V, $V_{CC} = 4.5$ V $I_F = 1.6$ mA, $V_O = 0.4$ V, $V_{CC} = 4.5$ V $I_F = 5$ mA, $V_O = 0.4$ V, $V_{CC} = 4.5$ V	3	3, 4
Logic Low Output Voltage	V_{OL}		0.11 0.13 0.16	0.4 0.4 0.4	V V V	$I_F = 0.5$ mA, $I_O = 1.0$ mA, $V_{CC} = 4.5$ V $I_F = 1.6$ mA, $I_O = 3.2$ mA, $V_{CC} = 4.5$ V $I_F = 5.0$ mA, $I_O = 10$ mA, $V_{CC} = 4.5$ V	2	3
Logic High Output Current	I_{OHX} I_{OH}		0.001	250	μA	$V_F = 0.7$ V (Channel Under Test) $I_F = 8$ mA (Other Channel) $V_O = V_{CC} = 18$ V		3, 5
Logic Low Supply Current	I_{CCL}		1.0	4	mA	$I_{F1} = I_{F2} = 1.6$ mA $V_{CC} = 18$ V	4	
Logic High Supply Current	I_{CCH}		0.001	15	μA	$I_{F1} = I_{F2} = 0$ $V_{CC} = 18$ V		
Input Forward Voltage	V_F	1.0	1.3	1.6	V	$I_F = 1.6$ mA, $T_A = 25°C$	1	3
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10$ μA		3
Input-Output Insulation Leakage Current	I_{I-O}			1.0	μA	45% Relative Humidity, $T_A = 25°C$ t = 5 sec, $V_{I-O} = 500$ Vdc		6, 12
Propagation Delay Time to Logic High At Output	t_{PLH}		17	185	μs	$I_F = 0.5$ mA, $R_L = 4.7$ kΩ, $V_{CC} = 5$ V	7,8	3
			14	115	μs	$I_F = 1.6$ mA, $R_L = 2.2$ kΩ, $V_{CC} = 5$ V	7,8	3
			8	60	μs	$I_F = 5.0$ mA, $R_L = 680$ Ω, $V_{CC} = 5$ V	7,8	3
Propagation Delay Time to Logic Low At Output	t_{PHL}		10	185	μs	$I_F = 0.5$ mA, $R_L = 4.7$ kΩ, $V_{CC} = 5$ V	7,8	3
			5	30	μs	$I_F = 1.6$ mA, $R_L = 2.2$ kΩ, $V_{CC} = 5$ V	7,8	3
			2	12	μs	$I_F = 5.0$ mA, $R_L = 680$ Ω, $V_{CC} = 5$ V	7,8	3
Common Mode Transient Immunity At Logic High Level Output	$\|CM_H\|$	500	≥2000		V/μs	$I_F = 0$, $R_L = 2.2$ kΩ $\|V_{CM}\| = 50\ V_{p-p}$, $V_{CC} = 5.0$ V, $T_A = 25°C$	9,10	3 9, 11
Common Mode Transient Immunity At Logic Low Level Output	$\|CM_L\|$	500	≥1000		V/μs	$I_F = 1.6$ mA, $R_L = 2.2$ kΩ $\|V_{CM}\| = 50\ V_{p-p}$, $V_{CC} = 5.0$ V, $T_A = 25°C$	9,10	3 10, 11

*All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

Typical Characteristics $T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500$ Vdc		3, 7
Capacitance (Input-Output)	C_{I-O}	2.0	pF	f = 1 MHz		3,7
Input-Input Insulation Leakage Current	I_{I-I}	0.5	nA	45% Relative Humidity, $V_{I-I} = 500$ Vdc $T_A = 25°C$, t = 5s.		8
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	$V_{I-I} = 500$ Vdc		8
Capacitance (Input-Input)	C_{I-I}	1.3	pF	f = 1 MHz		8
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	−1.5	mV/°C	$I_F = 1.6$ mA		3
Input Capacitance	C_{IN}	15	pF	f = 1 MHz, $V_F = 0$		3

NOTES:

1. GND Pin should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 V, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus one half of total supply power.
3. Each channel
4. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
5. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. V_F = 0.7 V for channel under test.
6. Device considered a two-terminal device: Pins 1 through 4 are shorted together and pins 5 through 8 are shorted together.
7. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
8. Measured between adjacent input pairs shorted together, i.e. between pins 1 and 2 shorted together and pins 3 and 4 shorted together.
9. CM_H is the maximum tolerable common mode transient such that the output will remain in a high logic state (i.e. $V_O > 2.0$ V).
10. CM_L is the maximum tolerable common mode transient such that the output will remain in a low logic state (i.e. $V_O < 0.8$ V).
11. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, is recommended to protect the detector IC's from destructively high surge currents. The recommended maximum value is

$$R_{CC} \approx \frac{1V}{0.3\, I_F\,(mA)}\ k\Omega.$$

12. This is a momentary withstand test, not an operating condition.

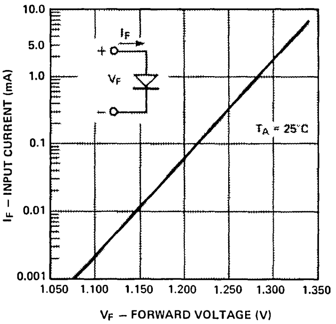


Figure 1. Input Current vs. Forward Voltage.

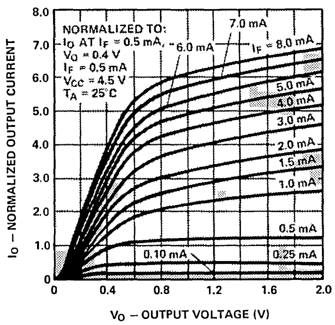


Figure 2. Normalized DC Transfer Characteristics.

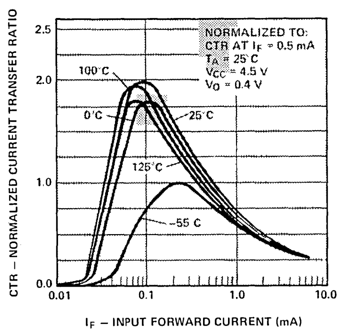


Figure 3. Normalized Current Transfer Ratio vs. Input Forward Current.

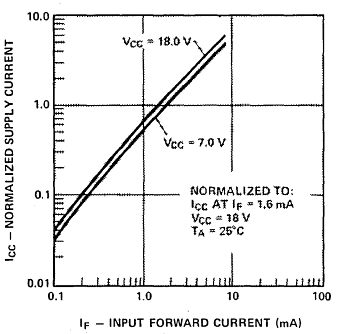


Figure 4. Normalized Supply Current vs. Input Forward Current.

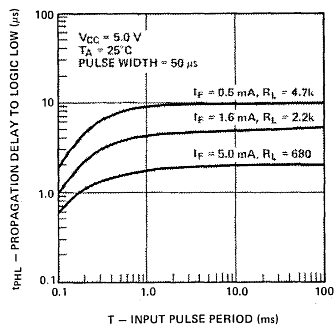


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

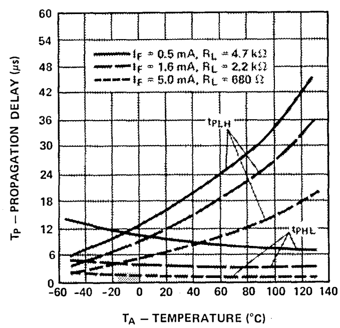


Figure 6. Propagation Delay vs. Temperature.

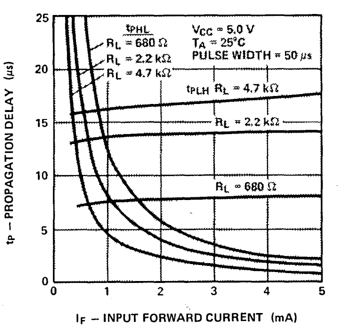


Figure 7. Propagation Delay vs. Input Forward Current.

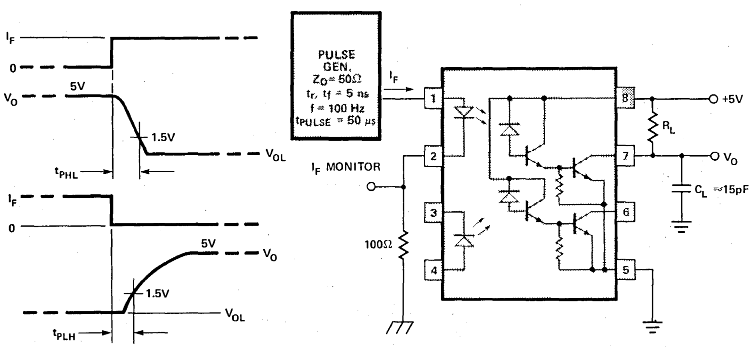


Figure 8. Switching Test Circuit.

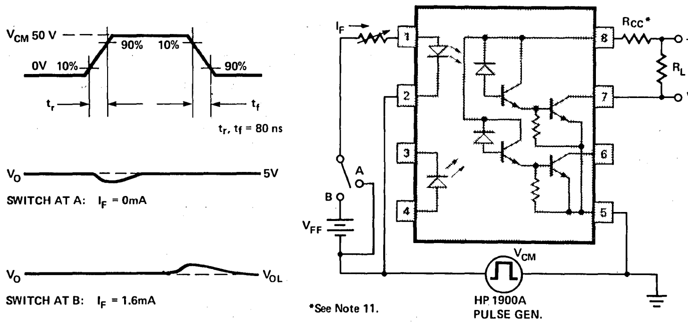


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

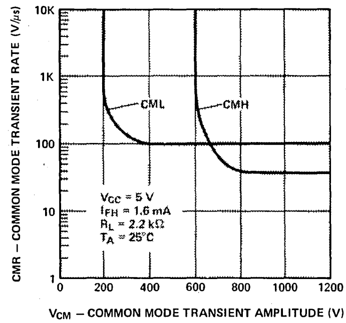


Figure 10. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

MIL-STD-883 CLASS B TEST PROGRAM

Hewlett-Packard's HCPL-5731 optocoupler is in compliance with MIL-STD-883, Revision C. Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005. Details of these test programs may be found in the hermetic optocoupler product qualification section of Hewlett-Packard's Optoelectronics Designer's Catalog 1985.

See table below for specific electrical tests.

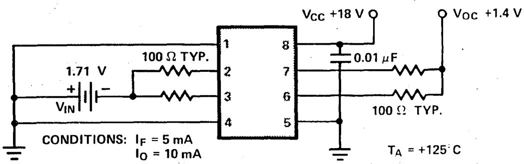


Figure 11. Operating Circuit for Burn-In and Steady State Life Tests.

PART NUMBERING SYSTEM

Commercial Product	Class B Product
HCPL-5730	HCPL-5731

GROUP A — ELECTRICAL TESTS

<table>
<tr><th colspan="5"></th><th>LTPD</th></tr>
<tr><td colspan="5">Subgroup 1
*Static tests at $T_A = 25°C$ – I_{OH}, I_{OHX}, V_{OL}, I_{CCL}, I_{CCH}, CTR, V_F, BV_R and I_{I-O}</td><td>2</td></tr>
<tr><td colspan="5">Subgroup 2
*Static tests at $T_A = +125°C$ — I_{OH}, I_{OHX}, V_{OL}, I_{CCL}, I_{CCH}, BV_R and CTR</td><td rowspan="3">3</td></tr>
<tr><td>Symbol</td><td>Min.</td><td>Max.</td><td>Units</td><td>Test Conditions</td></tr>
<tr><td>V_F</td><td></td><td>1.8</td><td>V</td><td>$I_F = 1.6$ mA</td></tr>
<tr><td colspan="5">Subgroup 3
*Static tests at $T_A = -55°C$ — I_{OH}, I_{OHX}, V_{OL}, I_{CCL}, I_{CCH}, BV_R and CTR</td><td rowspan="3">5</td></tr>
<tr><td>Symbol</td><td>Min.</td><td>Max.</td><td>Units</td><td>Test Conditions</td></tr>
<tr><td>V_F</td><td></td><td>1.8</td><td>V</td><td>$I_F = 1.6$ mA</td></tr>
<tr><td colspan="5">Subgroup 4, 5, 6, 7 and 8
These subgroups are not applicable to this device type.</td><td></td></tr>
<tr><td colspan="5">Subgroup 9
*Switching tests at $T_A = 25°C$ – t_{PLH1}, t_{PHL1}, t_{PLH2}, t_{PHL2}, t_{PLH3}, t_{PHL3}, CM_H and CM_L</td><td>2</td></tr>
<tr><td colspan="5">Subgroup 10
*Switching tests at $T_A = +125°C$ – t_{PLH1}, t_{PHL1}, t_{PLH2}, t_{PHL2}, t_{PLH3}, t_{PHL3}</td><td>3</td></tr>
<tr><td colspan="5">Subgroup 11
*Switching tests at $T_A = -55°C$ – t_{PLH1}, t_{PHL1}, t_{PLH2}, t_{PHL2}, t_{PLH3}, t_{PHL3}</td><td>5</td></tr>
</table>

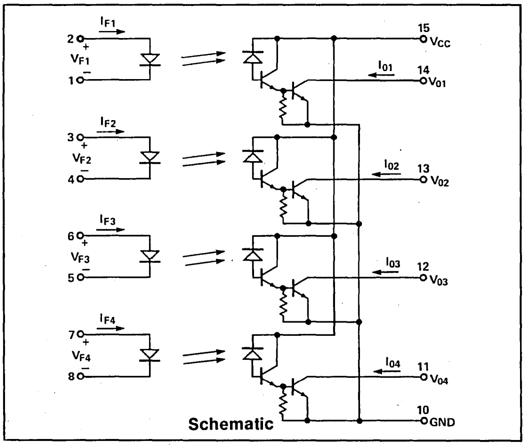
*Limits and conditions per Table II.

HEWLETT PACKARD

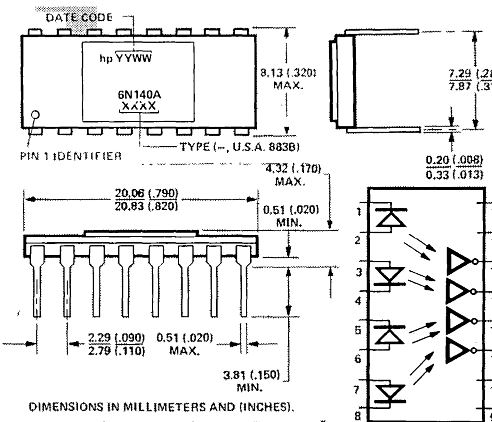
HERMETICALLY SEALED FOUR CHANNEL LOW INPUT CURRENT OPTOCOUPLER

6N140A
6N140A/883B

TECHNICAL DATA JANUARY 1986



Schematic



Outline Drawing*

Features

- PERFORMANCE GUARANTEED OVER −55° C TO +125° C AMBIENT TEMPERATURE RANGE
- MIL-STD-883 CLASS B TESTING
- HIGH DENSITY PACKAGING
- HERMETICALLY SEALED
- LOW INPUT CURRENT REQUIREMENT: 0.5 mA
- HIGH CURRENT TRANSFER RATIO: 1500% TYPICAL
- LOW OUTPUT SATURATION VOLTAGE: 0.1 V TYPICAL
- LOW POWER CONSUMPTION
- 1500 Vdc WITHSTAND TEST VOLTAGE
- HIGH RADIATION IMMUNITY

Applications

- MILITARY/HIGH RELIABILITY SYSTEMS
- ISOLATED INPUT LINE RECEIVER
- SYSTEM TEST EQUIPMENT ISOLATION
- DIGITAL LOGIC GROUND ISOLATION
- EIA RS-232C LINE RECEIVER
- MICROPROCESSOR SYSTEM INTERFACE
- CURRENT LOOP RECEIVER
- LEVEL SHIFTING
- PROCESS CONTROL INPUT/OUTPUT ISOLATION

Description

The 6N140A is an EIA registered hybrid microcircuit which is capable of operation over the full military temperature range from −55° C to +125° C and is electrically and functionally identical to the 6N140 part. It is an advanced replacement unit for the 6N140. Performance of the 6N140A over the full military temperature range results from an improved integrated bypass resistor which shunts photodiode and first stage leakage currents.

The 6N140A contains four GaAsP light emitting diodes, each of which is optically coupled to a corresponding integrated high gain photon detector. The high gain output stage features an open collector output providing both lower output saturation voltage and higher speed operation than possible with conventional photo-darlington type optocouplers. Also, the separate V_{CC} pin can be strobed low as an output disable or operated with supply voltages as low as 2.0V without adversely affecting the parametric performance.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

The 6N140A has a 300% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS-232C data transmission systems. Compatibility with high voltage CMOS logic systems is assured by the 18V V_{CC} and by the guaranteed maximum output leakage (I_{OH}) at 18V. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

See the selection guide at the front of this section for other devices in this family.

*JEDEC Registered Data

TABLE I

Recommended Operating Conditions

	Symbol	Min.	Max.	Units
Input Current, Low Level (Each Channel)	I_{FL}		2	μA
Input Current, High Level (Each Channel)	I_{FH}	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings*

Storage Temperature .... -65°C to +150°C
Operating Temperature .... -55°C to +125°C
Lead Solder Temperature .... 260°C for 10s.
(1.6mm below seating plane)
Output Current, I_O (each channel) .... 40 mA
Output Voltage, V_O (each channel) ...... -0.5 to 20 V[1]
Supply Voltage, V_{CC} .... -0.5 to 20 V[1]
Output Power Dissipation (each channel) ... 50 mW[2]
Peak Input Current (each channel, ≤1 ms duration, 500 pps) .... 20 mA
Average Input Current, I_F (each channel) ..... 10 mA[3]
Reverse Input Voltage, V_R (each channel) 5V

TABLE II

Electrical Characteristics $T_A = -55°C$ to 125°C, Unless Otherwise Specified

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	300 300 200	1500 1000 500		% % %	I_F=0.5mA, V_O=0.4V, V_{CC}=4.5V I_F=1.6mA, V_O=0.4V, V_{CC}=4.5V I_F=5mA, V_O=0.4V, V_{CC}=4.5V	3	4,5
Logic Low Output Voltage	V_{OL}		.1 .2	.4 .4	V V	I_F=0.5mA, I_{OL}=1.5mA, V_{CC}=4.5V I_F=5mA, I_{OL}=10mA, V_{CC}=4.5V	2	4
Logic High Output Current	I_{OHX} I_{OH}*		.001	250	μA	I_F=2μA (channel under test) V_O=V_{CC}=18V		4,6 4
Logic Low Supply Current	I_{CCL}*		1.7	4	mA	I_{F1}=I_{F2}=I_{F3}=I_{F4}=1.6mA V_{CC}=18V		
Logic High Supply Current	I_{CCH}*		.001	40	μA	I_{F1}=I_{F2}=I_{F3}=I_{F4}=0 V_{CC}=18V		
Input Forward Voltage	V_F*		1.44	1.7	V	I_F=1.6mA, T_A=25°C	1	4
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R=10μA, T_A=25°C		4
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	45% Relative Humidity, T_A=25°C, t=5s., V_{I-O}=1500 Vdc		7,13
Propagation Delay Time To Logic High At Output	t_{PLH}*		6	60	μs	I_F=0.5mA, R_L=4.7kΩ, V_{CC}=5.0V, T_A=25°C	8	4
			4	20	μs	I_F=5mA, R_L=680Ω, V_{CC}=5.0V, T_A=25°C	8	4
Propagation Delay Time To Logic Low At Output	t_{PHL}*		30	100	μs	I_F=0.5mA, R_L=4.7kΩ, V_{CC}=5.0V, T_A=25°C	8	4
			2	5	μs	I_F=5mA, R_L=680Ω, V_{CC}=5.0V, T_A=25°C	8	4
Common Mode Transient Immunity At Logic High Level Output	CM_H	500	1000		V/μs	I_F=0, R_L=1.5kΩ $\|V_{CM}\|$=50V_{p-p}, V_{CC}=5.0V, T_A=25°C	9	4 10,12
Common Mode Transient Immunity At Logic Low Level Output	CM_L	-500	-1000		V/μs	I_F=1.6mA, R_L=1.5kΩ $\|V_{CM}\|$=50V_{p-p}, V_{CC}=5.0V, T_A=25°C	9	4 11,12

*JEDEC Registered Data
**All typical values are at V_{CC} = 5V, T_A = 25°C.

TABLE III

Typical Characteristics T_A = 25°C, V_{CC} = 5V Each Channel

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500 Vdc, T_A=25°C		4,8
Capacitance (Input-Output)	C_{I-O}		1.5		pF	f=1MHz, T_A=25°C		4,8
Input-Input Insulation Leakage Current	I_{I-I}		0.5		nA	45% Relative Humidity, V_{I-I}=500 Vdc, T_A=25°C, t=5s.		9
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I}=500Vdc, T_A=25°C		9
Capacitance (Input-Input)	C_{I-I}		1		pF	f=1MHz, T_A=25°C		9
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.8		mV/°C	I_F=1.6mA		4
Input Capacitance	C_{IN}		60		pF	f=1MHz, V_F=0, T_A=25°C		4

NOTES:
1. Pin 10 should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 volts, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus one fourth of total supply power. Derate at 1.66mW/°C above 110°C.
3. Derate I_F at 0.33mA/°C above 110°C.
4. Each channel
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. I_F = 2μA for channel under test. For all other channels, I_F = 10mA.
7. Device considered a two-terminal device: Pins 1 through 8 are shorted together and pins 9 through 16 are shorted together.
8. Measured between the LED anode and cathode shorted together and pins 10 through 15 shorted together.
9. Measured between adjacent input pairs shorted together, i.e. between pins 1 and 2 shorted together and pins 3 and 4 shorted together, etc.
10. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e. V_O > 2.0V).
11. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e. V_O < 0.8V).
12. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC's from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.6\, I_F\, (mA)}$ kΩ.
13. This is a momentary withstand test, not an operating condition.

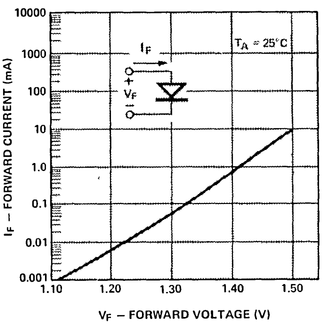


Figure 1. Input Diode Forward Current vs. Forward Voltage.

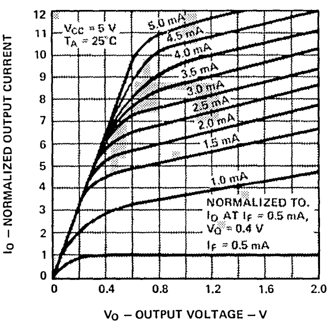


Figure 2. Normalized DC Transfer Characteristics

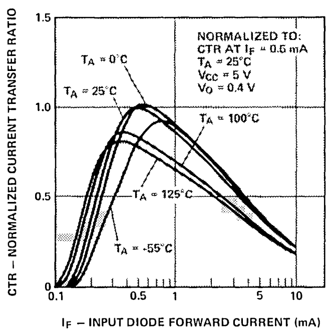


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

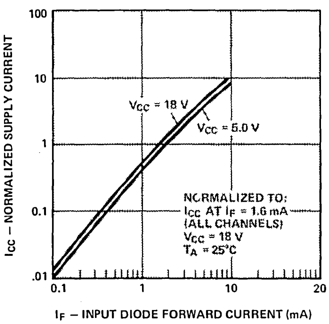


Figure 4. Normalized Supply Current vs. Input Diode Forward Current.

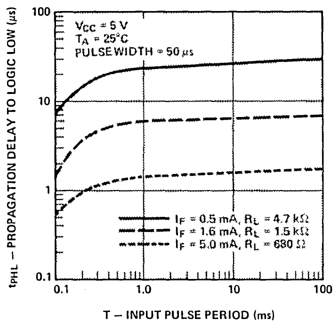


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

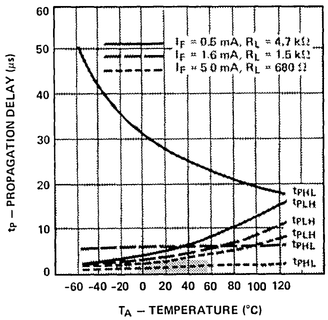


Figure 6. Propagation Delay vs. Temperature

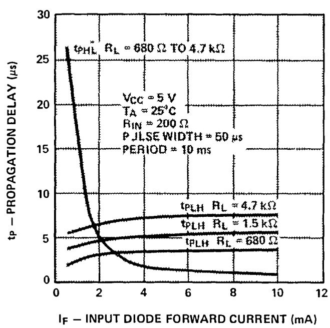


Figure 7. Propagation Delay vs. Input Diode Forward Current.

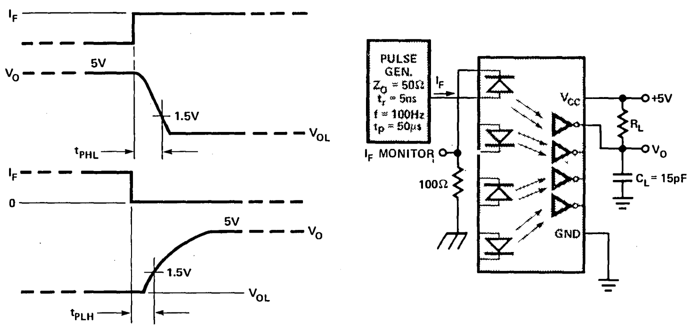


Figure 8. Switching Test Circuit.*
(f, t_P not JEDEC registered)

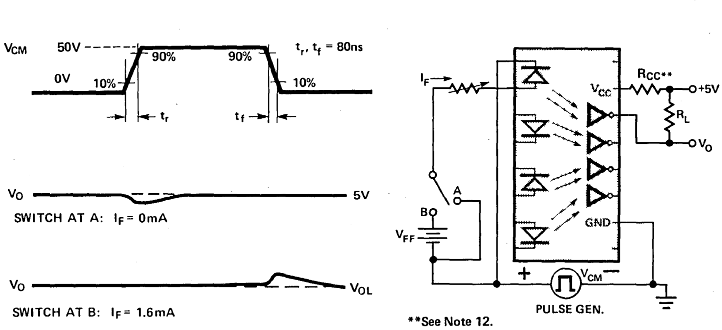


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

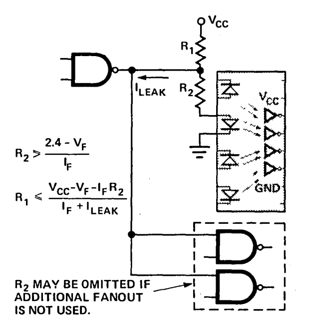


Figure 10. Recommended Drive Circuitry Using TTL Logic.

*JEDEC Registered Data

MIL-STD-883 CLASS B TEST PROGRAM

Hewlett Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC drawing 83024 for an H.P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883. See the pages of this section entitled Hermetic Optocoupler MIL-STD-883 Class B Test Program for details of this test program.

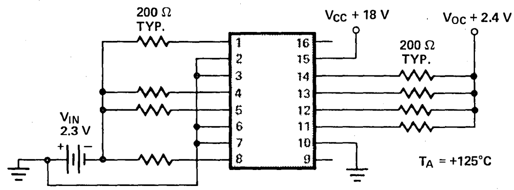
6N140A/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration — condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A,B,C and D.
Group A — See table below for specific electrical tests.
Group B — No change
Group C — Constant Acceleration — Condition A not E.
Group D — Constant Acceleration — Condition A not E.

PART NUMBERING SYSTEM

Commercial Product	Class B Product
6N140A	6N140A/883B



CONDITIONS: I_F = 5 mA
I_O = 10 mA
V_{CC} = 18 V

Figure 11. Operating Circuit for Burn-In and Steady State Life Tests.

GROUP A — ELECTRICAL TESTS

	LTPD
Subgroup 1 *Static tests at T_A = 25° C – I_{OH}, I_{OHX}, I_{CCL}, I_{CCH}, CTR, V_F, BV_R and I_{I-O}	2
Subgroup 2 *Static tests at T_A = +125° C – I_{OH}, I_{OHX}, I_{CCL}, I_{CCH}, CTR	3
Subgroup 3 *Static tests at T_A = –55° C – I_{OH}, I_{OHX}, I_{CCL}, I_{CCH}, CTR	5
Subgroup 4, 5, 6, 7 and 8 These subgroups are not applicable to this device type.	
Subgroup 9 *Switching tests at T_A = 25° C – t_{PLH1}, t_{PHL1}, t_{PLH2}, t_{PHL2}, CM_H and CM_L	2
Subgroup 10 Switching tests at T_A = +125° C	3
Subgroup 11 Switching tests at T_A = –55° C	5

Subgroup 2

Symbol	Min.	Max.	Units	Test Conditions
V_F		1.8	V	I_F = 1.6 mA
BV_R	5		V	I_R = 10 μA

Subgroup 3

Symbol	Min.	Max.	Units	Test Conditions
V_F		1.8	V	I_F = 1.6 mA
BV_R	5		V	I_R = 10 μA

Subgroup 10

Symbol	Max.	Units	Test Conditions	
t_{PLH1}	300	μs	I_F = 0.5 mA, R_L = 4.7 kΩ	V_{CC} = 5.0 V
t_{PLH2}	80	μs	I_F = 5 mA, R_L = 680 Ω	V_{CC} = 5.0 V
t_{PHL1}	200	μs	I_F = 0.5 mA, R_L = 4.7 kΩ	V_{CC} = 5.0 V
t_{PHL2}	10	μs	I_F = 5 mA, R_L = 680 Ω	V_{CC} = 5.0 V

Subgroup 11

Symbol	Max.	Units	Test Conditions	
t_{PLH1}	300	μs	I_F = 0.5 mA, R_L = 4.7 kΩ	V_{CC} = 5.0 V
t_{PLH2}	80	μs	I_F = 5 mA, R_L = 680 Ω	V_{CC} = 5.0 V
t_{PHL1}	200	μs	I_F = 0.5 mA, R_L = 4.7 kΩ	V_{CC} = 5.0 V
t_{PHL2}	10	μs	I_F = 5 mA, R_L = 680 Ω	V_{CC} = 5.0 V

*Limits and conditions per Table II.

HEWLETT PACKARD

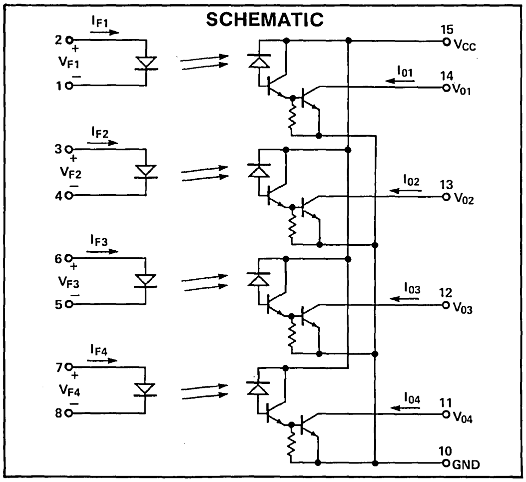
FOUR CHANNEL HERMETICALLY SEALED OPTOCOUPLER

DESC APPROVED

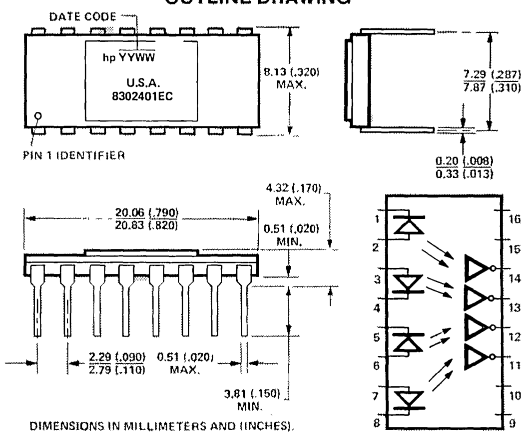
8302401EC

TECHNICAL DATA JANUARY 1986

SCHEMATIC



OUTLINE DRAWING



Features

- RECOGNIZED BY DESC*
- HERMETICALLY SEALED
- MIL-STD-883 CLASS B TESTING
- HIGH DENSITY PACKAGING
- PERFORMANCE GUARANTEED OVER −55° C TO +125° C AMBIENT TEMPERATURE RANGE
- 1500 V dc WITHSTAND TEST VOLTAGE
- LOW INPUT CURRENT REQUIREMENT: 0.5 mA
- HIGH CURRENT TRANSFER RATIO: 1500% TYPICAL
- LOW OUTPUT SATURATION VOLTAGE: 0.1 V TYPICAL
- LOW POWER CONSUMPTION
- HIGH RADIATION IMMUNITY

Applications

- MILITARY/HIGH RELIABILITY SYSTEMS
- ISOLATED INPUT LINE RECEIVER
- SYSTEM TEST EQUIPMENT ISOLATION
- DIGITAL LOGIC GROUND ISOLATION
- EIA RS-232C LINE RECEIVER
- MICROPROCESSOR SYSTEM INTERFACE
- CURRENT LOOP RECEIVER
- LEVEL SHIFTING
- PROCESS CONTROL INPUT/OUTPUT ISOLATION

Description

The 8302401EC is the DESC selected item drawing assigned by DOD for the 6N140A optocoupler which is in accordance with MIL-STD-883 class B testing. Operating characteristic curves for this part can be seen in the 6N140A data sheet. This hybrid microcircuit is capable of operation over the full military temperature range from −55° C to +125° C.

The 8302401EC contains four GaAsP light emitting diodes, each of which is optically coupled to a corresponding integrated high gain photon detector. The high gain output stage features an open collector output providing both lower output saturation voltage and higher speed operation than possible with conventional photo-darlington type optocouplers. Also, the separate V_{CC} pin can be strobed low as an output disable or operated with supply voltages as low as 2.0V without adversely affecting the parametric performance.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

The 8302401EC has a 300% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS-232C data transmission systems. Compatibility with high voltage CMOS logic systems is assured by the 18V V_{CC} and by the guaranteed maximum output leakage (I_{OH}) at 18V. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

The test program performed on the 8302401EC is in compliance with DESC drawing 83024 and the provisions of method 5008, Class B of MIL-STD-883.

*Defense Electronic Supply Center (DESC) is an agency of the Department of Defense (DOD).

Recommended Operating Conditions

	Symbol	Min.	Max.	Units
Input Current, Low Level (Each Channel)	I_{FL}		2	μA
Input Current, High Level (Each Channel)	I_{FH}	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings

Storage Temperature Range .... −65° C to +150° C
Operating Temperature .... −55° C to +125° C
Lead Solder Temperature .... 260° C for 10 s. (1.6mm below seating plane)
Output Current, I_O (each channel) .... 40 mA
Output Voltage, V_O (each channel) .... −0.5 to 20 V[1]
Supply Voltage, V_{CC} .... −0.5 to 20 V[1]
Output Power Dissipation (each channel) ...... 50 mW[2]
Peak Input Current (each channel, ≤ 1 ms duration) .... 20 mA
Average Input Current, I_F (each channel) .... 10 mA[3]
Reverse Input Voltage, V_R (each channel) 5V

100% Screening

MIL-STD-883, METHOD 5004 (CLASS B DEVICES)

Test Screen	Method	Conditions
1. Precap Internal Visual	2017	
2. High Temperature Storage	1008	Condition C, $T_A = 150°C$, Time = 24 hours minimum
3. Temperature Cycling	1010	Condition C, −65° C to +150° C, 10 cycles
4. Constant Acceleration	2001	Condition A, 5KG's, Y_1 axis only
5. Fine Leak	1014	Condition A
6. Gross Leak	1014	Condition C
7. Interim Electrical Test	—	Optional
8. Burn-In	1015	Condition B, Time = 160 hours minimum $T_A = +125°C$, $V_{CC} = 18V$, $I_F = 5$ mA, $I_O = 10$ mA (Figure 1)
9. Final Electrical Test Electrical Test Electrical Test	—	Group A, Subgroup 1, 5% PDA applies Group A, Subgroup 2 Group A, Subgroup 3
10. External Visual	2009	

Quality Conformance Inspection

GROUP A ELECTRICAL PERFORMANCE CHARACTERISTICS

Parameter	Symbol	Test Conditions	Group A Subgroups	Limits		Unit	Note
				Min.	Max.		
Current Transfer Ratio	$h_{F(CTR)}$	I_F=0.5mA, V_O=0.4V, V_{CC}=4.5V	1, 2, 3	300		%	4, 5
		I_F=1.6mA, V_O=0.4V, V_{CC}=4.5V	1, 2, 3	300		%	4, 5
		I_F=5mA, V_O=0.4V, V_{CC}=4.5V	1, 2, 3	200		%	4, 5
Logic Low Output Voltage	V_{OL}	I_F=0.5mA, I_{OL}=1.5mA, V_{CC}=4.5V	1, 2, 3		0.4	V	4
		I_F=5mA, I_{OL}=10mA, V_{CC}=4.5V	1, 2, 3		0.4	V	4
Logic High Output Current	I_{OH}	I_F=2μA	1, 2, 3		250	μA	4
	I_{OHX}	V_O=V_{CC}=18V	1, 2, 3		250	μA	4, 6
Logic Low Supply Current	I_{CCL}	I_{F1}=I_{F2}=I_{F3}=I_{F4}=1.6mA V_{CC}=18V	1, 2, 3		4	mA	
Logic High Supply Current	I_{CCH}	I_{F1}=I_{F2}=I_{F3}=I_{F4}=0mA V_{CC}=18V	1, 2, 3		40	μA	
Input Forward Voltage	V_F	I_F=1.6mA	1, 2		1.7	V	4
			3		1.8	V	4
Input Reverse Breakdown Voltage	BV_R	I_R=10μA	1, 2, 3	5		V	4
Input-Output Insulation Leakage Current	I_{I-O}	45% Relative Humidity, T=25°C, t=5s., V_{I-O}=1500 Vdc	1		1.0	μA	7, 12
Capacitance Between Input-Output	C_{I-O}	f=1MHz, T_C=25°C	4		4	pF	4, 8
Propagation Delay Time To Logic High At Output	t_{PLH}	I_F=0.5mA, R_L=4.7kΩ, V_{CC}=5.0V	9, 10, 11		60	μs	
		I_F=5mA, R_L=680Ω, V_{CC}=5.0V	9		20	μs	
			10, 11		30	μs	
Propagation Delay Time To Logic Low At Output	t_{PHL}	I_F=0.5mA, R_L=4.7kΩ, V_{CC}=5.0V	9, 10, 11		100	μs	
		I_F=5mA, R_L=680Ω, V_{CC}=5.0V	9		5	μs	
			10, 11		10	μs	
Common Mode Transient Immunity At Logic High Level Output	CM_H	I_F=0, R_L=1.5kΩ $\|V_{CM}\|$=25V_{p-p}, V_{CC}=5.0V, T_A=25°C	9, 10, 11	500		V/μs	9, 11
Common Mode Transient Immunity At Logic Low Level Output	CM_L	I_F=1.6mA, R_L=1.5kΩ $\|V_{CM}\|$=25V_{p-p}, V_{CC}=5.0V, T_A=25°C	9, 10, 11	−500		V/μs	10, 11

NOTES:

1. Pin 10 should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 volts, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus one fourth of total supply power. Derate at 1.66mW/°C above 110°C.
3. Derate I_F at 0.33mA/°C above 110°C.
4. Each channel
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. I_F = 2μA for channel under test. For all other channels, I_F = 10mA.
7. Device considered a two-terminal device: Pins 1 through 8 are shorted together and pins 9 through 16 are shorted together.
8. Measured between the LED anode and cathode shorted together and pins 10 through 15 shorted together.
9. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e. V_O > 2.0V).
10. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e. V_O < 0.8V).
11. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC's from destructively high surge currents. The recommended value is

$$R_{CC} \approx \frac{1V}{0.6\, I_F\,(mA)}\ k\Omega.$$

12. This is a momentary withstand test, not an operating condition.

GROUP B TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1 Physical Dimensions (Not required if Group D is to be performed)	2016		2 Devices (no failures)
Subgroup 2 Resistance to Solvents	2015		4 Devices (no failures)
Subgroup 3 Solderability (LTPD applies to number of leads inspected — no fewer than 3 devices shall be used).	2003	Soldering Temperature of 245 ± 5°C for 10 seconds	15 (3 Devices)
Subgroup 4 Internal Visual and Mechanical	2014		1 Device (no failures)
Subgroup 5 Bond Strength Thermocompression: (Performed at precap, prior to seal LTPD applies to number of bond pulls from a minimum of 4 devices).	2011	Test Condition D	15 (4 Devices)
Subgroup 6 Internal Water Vapor Content (Not applicable — does not contain desiccant)	—		—
Subgroup 7 Fine Leak Gross Leak	1014	Condition A Condition C	5
Subgroup 8* Electrical Test		Group A, Subgroup 1, except I_{I-O}	15
Electrostatic Discharge Sensitivity	3015		
Electrical Test		Group A, Subgroup 1	
*(To be performed at initial qualification only)			

GROUP C TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1 Steady State Life Test	1005	Condition B, Time = 1000 hours total $T_A = +125°C$, $V_{CC} = 18$ V, $I_F = 5$ mA, $I_O = 10$ mA (Figure 1)	5
Endpoint Electricals at 1000 hours		Group A, Subgroup 1, 2, 3	
Subgroup 2 Temperature Cycling	1010	Condition C, −65°C to +150°C, 10 cycles	15
Constant Acceleration	2001	Condition A, 5KGs, Y_1 axis only	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per Visual Criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	

GROUP D TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Test Condition B2 (lead fatigue)	15
Subgroup 3			
Thermal Shock	1011	Condition B, (−55° C to +125° C) 15 cycles min.	15
Temperature Cycling	1010	Condition C, (−65° C to +150° C) 100 cycles min.	
Moisture Resistance	1004		
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination		Per Visual Criteria of Method 1004	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	
Subgroup 4			
Mechanical Shock	2002	Condition B, 1500G, t = 0.5 ms, 5 blows in each orientation	15
Vibration Variable Frequency	2007	Condition A	
Constant Acceleration	2001	Condition A, 5KGs, Y_1 axis only	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per Visual Criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	
Subgroup 5			
Salt Atmosphere	1009	Condition A min.	15
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1009	Per Visual Criteria of Method 1009	
Subgroup 6			
Internal Water Vapor Content	1018	5,000 ppm Maximum Water content at 100° C	3 Devices (0 failures) 5 Devices (1 failure)
Subgroup 7			
Adhesion of Lead Finish	2025		15
Subgroup 8			
Lid Torque (not applicable—solder seal)	2024		5 Devices (0 failures)

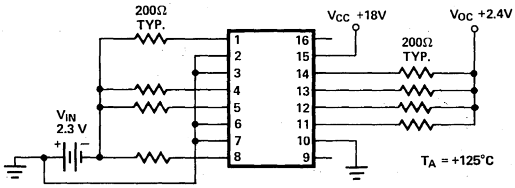


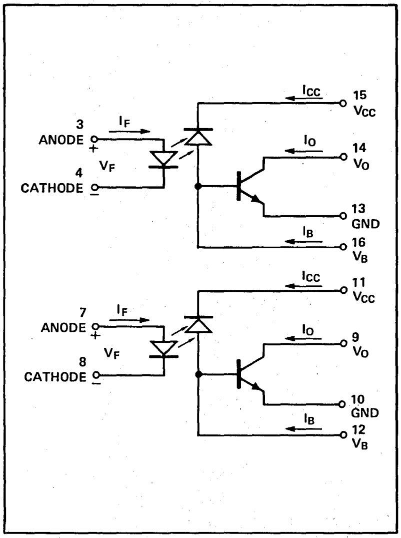
Figure 1. Operating Circuit for Burn-In and Steady State Life Tests.

HEWLETT PACKARD

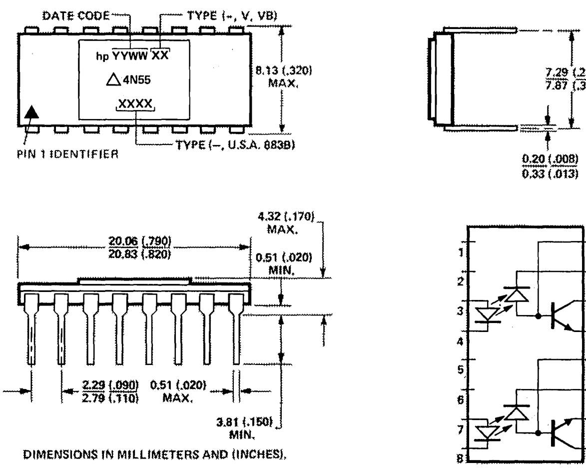
DUAL CHANNEL HERMETICALLY SEALED OPTOCOUPLER

4N55
4N55/883B

TECHNICAL DATA JANUARY 1986



Outline Drawing*



Features

- PERFORMANCE GUARANTEED OVER -55°C TO +125°C AMBIENT TEMPERATURE RANGE
- MIL-STD-883 CLASS B TESTING
- HERMETICALLY SEALED
- HIGH SPEED: TYPICALLY 400k BIT/S
- 2 MHz BANDWIDTH
- OPEN COLLECTOR OUTPUTS
- 18 VOLT V_{CC}
- DUAL-IN-LINE PACKAGE
- 1500 Vdc WITHSTAND TEST VOLTAGE
- HIGH RADIATION IMMUNITY

Applications

- HIGH RELIABILITY SYSTEMS
- LINE RECEIVERS
- DIGITAL LOGIC GROUND ISOLATION
- ANALOG SIGNAL GROUND ISOLATION
- SWITCHING POWER SUPPLY FEEDBACK ELEMENT
- VEHICLE COMMAND/CONTROL
- SYSTEM TEST EQUIPMENT
- LEVEL SHIFTING

Description

The 4N55 consists of two completely independent optocouplers in a hermetically sealed ceramic package. Each channel has a light emitting diode and an integrated photon detector. Separate connections for the photodiodes and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance.

The 4N55 is suitable for wide bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at I_F = 16mA over the full military operating temperature range, -55° C to +125° C. The 18V V_{CC} capability will enable the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

Hewlett-Packard's new high reliability part type 4N55/883B meets Class B testing requirements for MIL-STD-883. This part is the recommended and preferred device from the 4N55 product family for use in high reliability applications.

See the selection guide at the front of this section for other devices in this family.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

*JEDEC Registered Data

Absolute Maximum Ratings*

Storage Temperature .... -65° C to +150° C
Operating Temperature .... -55° C to +125° C
Lead Solder Temperature .... 260° C for 10 s (1.6mm below seating plane)
Average Input Current, I_F (each channel) 20mA
Peak Input Current, I_F (each channel, ≤ 1ms duration) 40mA
Reverse Input Voltage, V_R (each channel) 5V
Input Power Dissipation (each channel) 36mW
Average Output Current, I_O (each channel) 8mA
Peak Output Current, I_O (each channel) 16mA
Supply Voltage, V_{CC} (each channel) ..... -0.5V to 20V
Output Voltage, V_O (each channel) ...... -0.5V to 20V
Emitter Base Reverse Voltage, V_{EBO} 3.0V
Base Current, I_B (each channel) 5mA
Output Power Dissipation (each channel) 50mW
Derate linearly above 100° C free air temperature at a rate of 1.4mW/° C.

TABLE I.

Recommended Operating Conditions (EACH CHANNEL)

	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}		250	μA
Supply Voltage	V_{CC}	2	18	V

TABLE II.

Electrical Characteristics T_A = -55° C to +125° C, unless otherwise specified

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	9	20		%	I_F=16mA, V_O=0.4V, V_{CC}=4.5V	2,3	1,2
Logic High Output Current	I_{OH}		20	100	μA	I_F=0, I_F (other channel)=20mA V_O=V_{CC}=18V	4	1
Output Leakage Current	I_{OH1}*		70	250	μA	I_F=250μA, I_F (other channel)=20mA V_O=V_{CC}=18V	4	1
Logic Low Supply Current	I_{CCL}*		35	200	μA	I_{F1}=I_{F2}=20mA, V_{CC}=18V	5	1
Logic High Supply Current	I_{CCH}*		0.2	10	μA	I_F=0mA, I_F (other channel)=20mA V_{CC}=18V		1
Input Forward Voltage	V_F*		1.5	1.8	V	I_F=20mA	1	1
Input Reverse Breakdown Voltage	BV_R*	3			V	I_R=10μA		1
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	45% Relative Humidity, T_A=25° C, t=5s, V_{I-O}=1500Vdc		3,9
Propagation Delay Time to Logic High at Output	t_{PLH}*		2.0	6.0	μs	R_L=8.2KΩ, C_L=50pF I_F=16mA, V_{CC}=5V	6,9	1
Propagation Delay Time to Logic Low at Output	t_{PHL}*		0.4	2.0	μs	R_L=8.2KΩ, C_L=50pF I_F=16mA, V_{CC}=5V	6,9	1

*JEDEC Registered Data.
**All typical values are at V_{CC} = 5V, T_A = 25° C.

TABLE III.

Typical Characteristics at T_A=25°C

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/° C	I_F = 20 mA		1
Input Capacitance	C_{in}	120	pF	f=1 MHz, V_F=0		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O}=500 Vdc		1
Capacitance (Input-Output)	C_{I-O}	1.0	pF	f=1 MHz		1,4
Input-Input Insulation Leakage Current	I_{I-I}	1	pA	45% Relative Humidity, V_{I-I}=500Vdc, t=5s		5
Capacitance (Input-Input)	C_{I-I}	.55	pF	f=1 MHz		5
Transistor DC Current Gain	h_{FE}	150	—	V_O=5V, I_O=3mA		1
Small Signal Current Transfer Ratio	$\frac{\Delta I_O}{\Delta I_F}$	21	%	V_{CC}=5V, V_O=2V	7	1
Common Mode Transient Immunity at Logic High Level Output	CM_H	1000	V/μs	I_F=0, R_L=8.2kΩ V_{CM}=10V_{p-p} V_O (min.) = 2.0 V	10	1,6
Common Mode Transient Immunity at Logic Low Level Output	CM_L	-1000	V/μs	I_F=16mA, R_L=8.2kΩ V_{CM}=10V_{p-p} V_O (max.) = 0.8 V	10	1,7
Bandwidth	BW	2	MHz	R_L=100Ω	8	8

OPTOCOUPLERS

HI REL/HERMETIC COMPONENTS

Notes:

1. Each channel.
2. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle and system on time. Refer to Application Note 1002 for more detail. In short it is recommended that designers allow at least 20-25% guardband for CTR degradation.
3. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
4. Measured between each input pair shorted together and the output pins for that channel shorted together.
5. Measured between pins 3 and 4 shorted together and pins 7 and 8 shorted together.
6. CM_H is the steepest slope (dV/dt) on the leading edge of the common mode pulse, V_{CM}, for which the output will remain in the logic high state (i.e. $V_O > 2.0$ V).
7. CM_L is the steepest slope (dV/dt) on the trailing edge of the common mode pulse, V_{CM}, for which the output will remain in the logic low state (i.e. $V_O < 0.8$ V).
8. Bandwidth is the frequency at which the ac output voltage is 3dB below the low frequency asymptote.
9. This is a momentary withstand test, not an operating condition.

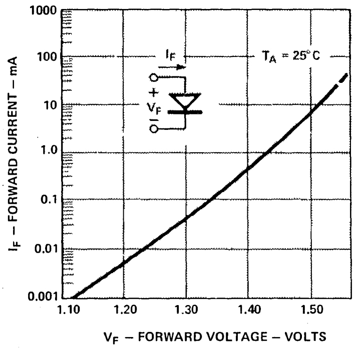


Figure 1. Input Diode Forward Characteristic.

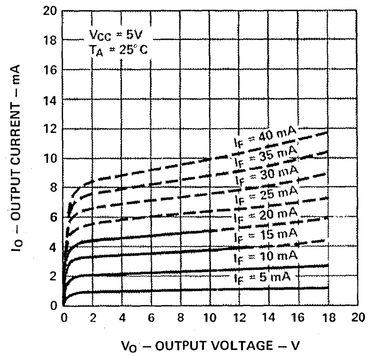


Figure 2. DC and Pulsed Transfer Characteristic

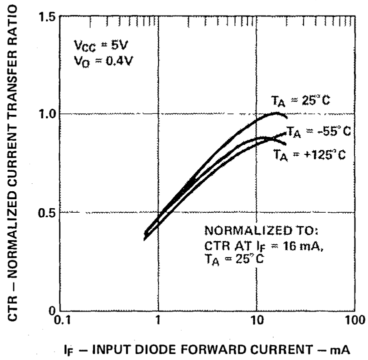


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

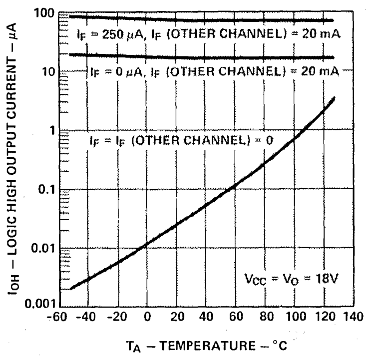


Figure 4. Logic High Output Current vs. Temperature.

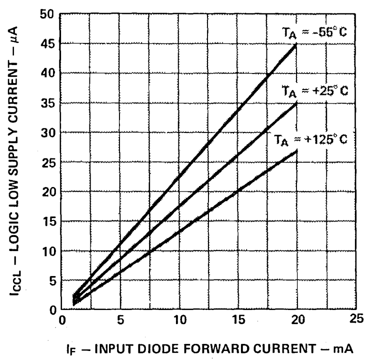


Figure 5. Logic Low Supply Current vs. Input Diode Forward Current.

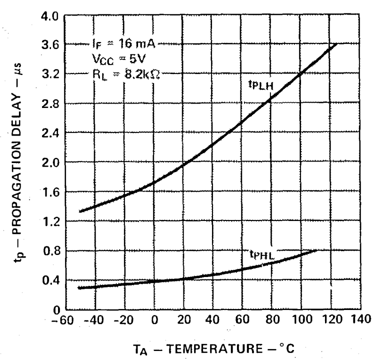


Figure 6. Propagation Delay vs. Temperature.

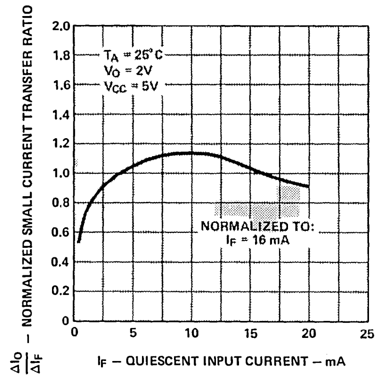


Figure 7. Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current.

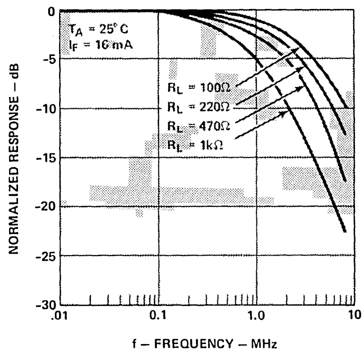


Figure 8a. Frequency Response

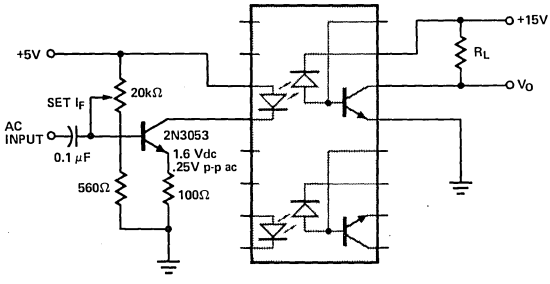


Figure 8b. Frequency Response

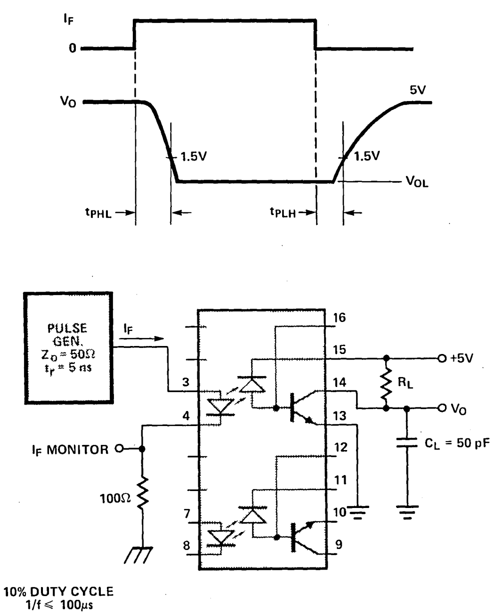


Figure 9. Switching Test Circuit*.

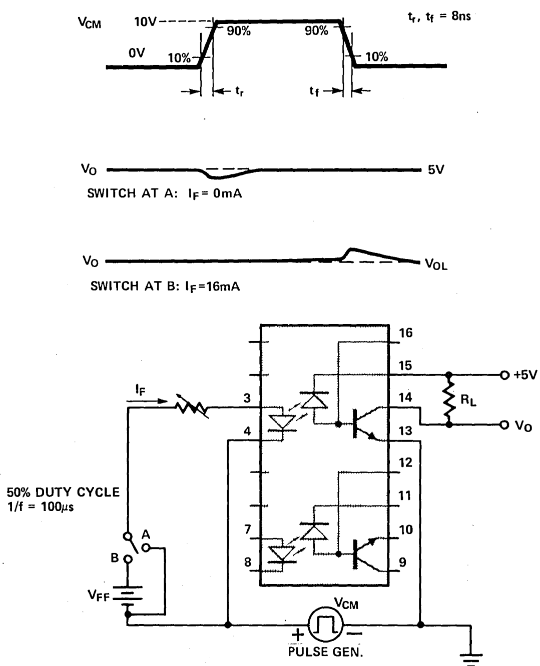
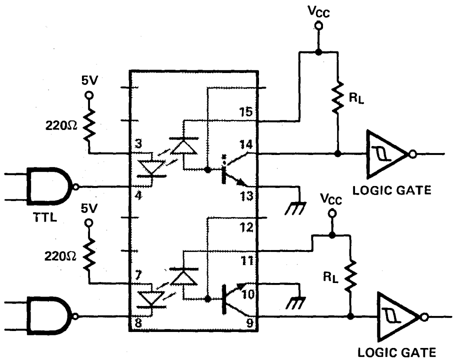


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

*JEDEC Registered Data



LOGIC FAMILY	LSTTL	CMOS	
DEVICE NO.	54LS14	CD40106BM	
V_{CC}	5V	5V	15V
R_L 5% TOLERANCE	*18kΩ	8.2kΩ	22kΩ

*THE EQUIVALENT OUTPUT LOAD RESISTANCE IS AFFECTED BY THE LSTTL INPUT CURRENT AND IS APPROXIMATELY 8.2kΩ.

This is a worst case design which takes into account 25% degradation of CTR. See App. Note 1002 to assess actual degradation and lifetime.

Figure 11. Recommended Logic Interface.

MIL-STD-883 CLASS B TEST PROGRAM

Hewlett-Packard's 883B optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC drawing 81028 for an H.P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883. See the pages of this section entitled Hermetic Optocoupler Product Qualification for details of this test program.

4N55/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration — condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C and D.

Group A — See table below for specific electrical tests.
Group B — No change
Group C — Constant Acceleration — Condition A not E.
Group D — Constant Acceleration — Condition A not E.

PART NUMBERING SYSTEM

Commercial Product	Class B Product
4N55	4N55/883B

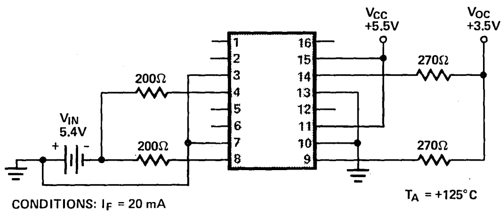


Figure 12. Operating Circuit for Burn-in and Steady State Life Tests

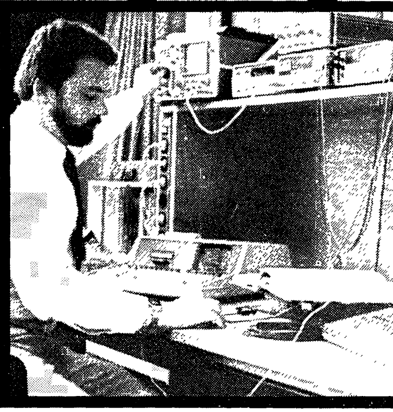
GROUP A — ELECTRICAL TESTS

	LTPD
Subgroup 1 * Static tests at $T_A = 25°C$, I_{OH}, BV_R, I_{CCL}, I_{CCH}, CTR, V_F, I_{OH1} and I_{I-O}.	2
Subgroup 2 * Static tests at $T_A = +125°C$, I_{OH}, BV_R I_{CCL}, I_{CCH}, CTR, V_F and I_{OH1}	3
Subgroup 3 * Static tests at $T_A = -55°C$, I_{OH}, BV_R I_{CCL}, I_{CCH}, CTR, V_F and I_{OH1}	5
Subgroups 4, 5, 6, 7 and 8 These subgroups are non-applicable to this device type	
Subgroup 9 * Switching tests at $T_A = 25°C$, t_{PLH} and t_{PHL}	2
Subgroup 10 * Switching tests at $T_A = +125°C$, t_{PLH} and t_{PHL}	3
Subgroup 11 * Switching tests at $T_A = -55°C$, t_{PLH} and t_{PHL}	5

* Limits and Conditions per Table II.

[redacted]

9. Applications



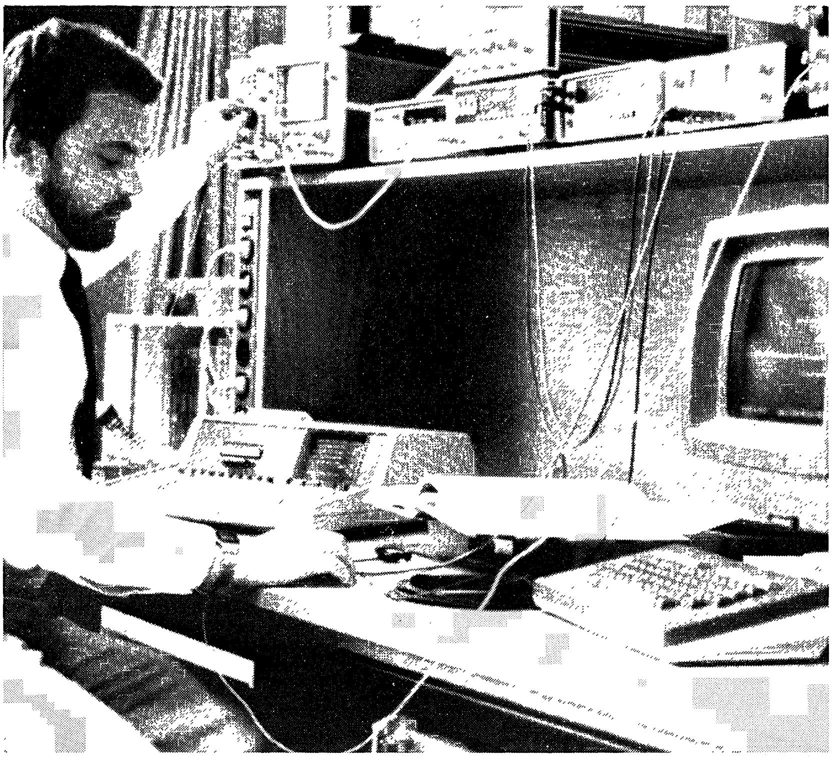
Applications

Because technology is growing and changing so rapidly, HP's commitment to customers includes an extensive applications department. In an effort to anticipate design needs and answer design questions, this team of engineers has published a complete library of applications literature available through HP sales and service offices, authorized distributors and direct from the factory. A listing of all application bulletins and application notes is on the facing page.

This year application handbooks which contain complete application notes bound together with additional product information are available. Now you can keep the design information you need from year-to-year.

These handbooks sell for $12 each, U.S. price. Look in the back of this catalog for a business reply card to order yours. For individual application notes either use the business reply card or call your nearest HP sales and service office. Ask for the Components department. A listing of these offices can be found in the appendix, section 10.

In 1981, the second edition of the Optoelectronics/Fiber Optics Applications Manual was published by McGraw-Hill. This hard-bound manual was prepared by HP's applications engineering staff and contains design information on LED's, displays, optocouplers and fiber optics. It can be purchased from an authorized distributor or directly from McGraw-Hill for $25.



Applications Listing

MOTION SENSING AND CONTROL

Model Pub. No. (Date)	Description
AN-1011 5953-9393 (12/83)	Design and Operational Considerations for the HEDS-5000 Incremental Shaft Encoder
AN-1025 5954-0920 (9/85)	Applications and Circuit Design for the HEDS-7500 series Digital Potentiometer

BAR CODE COMPONENTS

Model Pub. No. (Date)	Description
AB-59 5953-9365 (7/83)	HP 16800A/16801A Bar Code Reader Configuration Guide for a DEC VT-100 or Lear Siegler ADM-31 to a DEC PDP-11 Computer
AB-61 5953-9361 (8/83)	HP 16800A/16801A Bar Code Reader Configuration Guide for an IBM 3276/3278 Terminal
AB-62 5953-9362 (8/83)	HP 16800A/16801A Bar Code Reader Configuration Guide for an IBM 4955F Series 1 Process Control CPU/Protocol Converter and an IBM 3101 Terminal
AB-63 5953-9363 (8/83)	HP 16800A/16801A Bar Code Reader Configuration Guide for an IBM 5101 Personal Computer
AB-68 5953-9382 (11/83)	HP 16800A/16801A Bar Code Reader Configuration Guide for a MICOM Micro280 Message Concentrator
AB-1008 5953-0460 (1/81)	Optical Sensing with the HEDS-1000
AN-1013 5953-9387 (11/83)	Elements of a Bar Code System

OPTOCOUPLERS

Model Pub. No. (Date)	Description
TB-101 5954-1004 (4/85)	Fiber Optic SMA Connector Technology
TB-102 5954-1011 (5/85)	Fiber/Cable Selection for LED Based Local Communications Systems
TB-103 5954-1017 (7/85)	High Speed Optocouplers vs. Pulse Transformer
AB-60 5953-9347(4/83)	Applications Circuits for HCPL-3700 and HCPL-2601
AB-69 5953-9384 (10/83)	CMOS Circuit Design using Hewlett-Packard Optocouplers
AN-939 5953-9368 (10/73)	High Speed Optocouplers
AN-947 5953-7759 (6/82)	Digital Data Transmission Using Optically Coupled Isolators
AN-948 5953-7716 (12/81)	Performance of the 6N135, 6N136 and 6N137 Optocouplers in Short to Moderate Length Digital Data Transmission Systems
AN-951-1 5953-7794 (10/82)	Applications for Low Input Current, High Gain Optocouplers
AN-951-2 5963-7730 (4/82)	Linear Applications of Optocouplers
AN-1002 5953-7799 (10/82)	Consideration of CTR Variations in Optically Coupled Isolator Circuit Designs
AN-1004 5953-0406 (11/79)	Threshold Sensing for Industrial Control Systems with the HCPL-3700 Interface Optocoupler
AN-1018 5953-9359 (8/83)	Designing with HCPL-4100 and HCPL-4200 20 mA Optocouplers
AN-1023 5954-1003 (3/85)	Radiation Immunity of HP Optocouplers
AN-1024 5954-1006 (3/85)	Ring Detection with the HCPL-3700 Optocoupler

FIBER OPTICS

Model Pub. No. (Date)	Description
AB-65 5953-9370 (9/83)	Using 50/125 μm Optical Fiber with Hewlett-Packard Components
AB-71 5954-1021 (12/85)	Using 200 μm PCS Optical Fiber with HP Components
AN-915 5953-0431 (4/80)	Threshold Detection of Visible and Infrared Radiation with PIN Photodiodes
AN-1000 5953-0463 (1/82)	Digital Data Transmission with the HP Fiber Optic System
AN-1022 5954-0979 (1/85)	High Speed Fiber Optic Link Design with Discrete Components

LIGHT BARS AND BAR GRAPH ARRAYS

Model Pub. No. (Date)	Description
AN-1007 5953-0452 (1/81)	Bar Graph Array Applications
AN-1012 5953-0478 (2/81)	Methods of Legend Fabrication

SOLID STATE LAMPS

Model Pub. No. (Date)	Description
AB-1 5952-8378 (1/75)	Construction and Performance of High Efficiency Red, Yellow and Green LED Materials
AN-945 5952-0420 (10/73)	Photometry of Red LEDs
AN-1005 5953-0419 (3/80)	Operational Considerations for LED Lamps and Display Devices
AN-1017 5953-7784 (10/82)	LED Solid State Reliability
AN-1019 5954-0921 (1/86)	Using the HLMP-4700/-1700/-7000 Series Low Current Lamp
AN-1021 5953-0861 (5/84)	Utilizing LED Lamps Packaged on Tape and Reel
AN-1027 5954-0893 (7/85)	Soldering LED Components
AN-1028 5954-0902 (9/85)	Surface Mount Subminiature LED Lamps

SOLID STATE DISPLAYS

Model Pub. No. (Date)	Description
AB-4 5952-8381 (4/75)	Detection and Indication of Segment Failures in 7-Segment LED Displays
AB-64 5953-9366 (9/83)	Mechanical and Optical Considerations for the 0.3" Microbright Seven-Segment Display
AB-70 5954-0868 (11/84)	Green LED Displays and GEN III ANVIS Night Vision Goggle Compatibility
AN-934 5952-0337 (11/72)	5082-7300 Series Solid State Display Installation Techniques
AN-1006 5953-0439 (7/80)	Seven Segment LED Display Applications
AN-1015 5953-7788 (11/82)	Contrast Enhancement Techniques for LED Displays
AN-1016 5953-7787 (3/84)	Using the HDSP-2000 Alphanumeric Display Family
AN-1026 5954-0886 (6/85)	Designing with HP's Smart Display — the HPDL-2416

APPLICATIONS HANDBOOKS

Model Pub. No. (Date)	Description
HPBK-4000 (1986)	LED Indicators and Displays Applications Handbook $10
HPBK-5000 (1986)	Optocouplers and Fiber Optics Applications Handbook $10

APPLICATIONS MANUAL

Model Pub. No. (Date)	Description
HPBK-2000 McGraw-Hill (no. 93203815) (1981)	Optoelectronics/Fiber-Optics Applications Manual $25

Abstracts

APPLICATION BULLETIN 1
Construction and Performance of High Efficiency Red, Yellow and Green LED Materials

The high luminous efficiency of Hewlett-Packard's High Efficiency Red, Yellow and Green lamps and displays is made possible by a new kind of light emitting material utilizing a GaP transparent substrate. This application bulletin discusses the construction and performance of this material as compared to standard red GaAsP and red GaP materials.

APPLICATION BULLETIN 4
Detection and Indication of Segment Failures in Seven Segment LED Displays

The occurrence of a segment failure in certain applications of seven segment displays can have serious consequences if a resultant erroneous message is read by the viewer. This application bulletin discusses three techniques for detecting open segment lines and presenting this information to the viewer.

APPLICATION BULLETIN 59
HP16800A/16801A Bar Code Reader Configuration Guide for a DEC VT-100 or Lear Siegler ADM-31 to a DEC PDP-11 Computer

This application bulletin provides information to aid in configuring the HP 16800A/16801A bar code reader with a DEC-PDP-11 computer, and either a DEC-VT-100 terminal or a LEAR SIEGLER ADM-31 terminal.

APPLICATION BULLETIN 60
Applications Circuits for HCPL-3700 and HCPL-2601

Simple circuit illustrations are given for use of the HCPL-3700 threshold detection optocoupler for ac or dc sensing requirements. Programmable threshold levels are given for the HCPL-3700.

Also, a basic LSTTL to LSTTL isolation interface circuit for 10 MBd operation is given which uses the high common mode transient immunity HCPL-2601 optocoupler.

APPLICATION BULLETIN 61
HP 16800A/16801A Bar Code Reader Configuration Guide for an IBM 3276/3278 Terminal

This application bulletin provides information to aid in configuring the HP 16800A/16801A bar code reader with an IBM 3276/3278 terminal to an IBM 3272/3274 Remote Communications Controller. In this configuration the IBM 3272/3274 is connected to an IBM mainframe computer.

APPLICATION BULLETIN 62
HP 16800A/16801A Bar Code Reader Configuration Guide for an IBM 4955F Series 1 Process Control CPU/ Protocol Converter and an IBM 3101 Terminal

This application bulletin provides information to aid in configuring the HP 16800A/16801A bar code reader in an eavesdrop configuration with an IBM 3101 terminal and an IBM Series 1 Process Control CPU/Protocol Converter. In this configuration the IBM Series 1 is connected to an IBM mainframe computer.

APPLICATION BULLETIN 63
HP 16800A/16801A Bar Code Reader Configuration Guide for an IBM 5101 Personal Computer

This application bulletin provides information to aid in configuring the HP 16800A/16801A bar code reader with an IBM 5101 Personal Computer.

APPLICATION BULLETIN 64
Mechanical and Optical Considerations for the 0.3" Microbright Seven-Segment Display

The need to conserve space in electronic instruments has increased drastically in the drive to design more compact, more portable equipment. Hewlett-Packard has facilitated the saving of space in the design of front panels with the introduction of the Microbright, Hewlett-Packard's new HDSP-7300/-7400/-7500/-7800 series compact 0.3" seven segment displays. Smaller than the conventional 0.3" device, the Microbright requires less space without sacrificing display height and is also Hewlett-Packard's most sunlight viewable seven segment display.

This application bulletin deals with several issues in the use of the Microbright. Optical filtering is covered, with recommendations on filters to use over the devices. Adjusting the package height and recommended sockets are also presented, followed by a discussion on the brightness of the display.

APPLICATION BULLETIN 65
Using 50/125 μm Optical Fiber with Hewlett-Packard Components

Applications Bulletin 65 explains factors that influence the power coupled into various fiber diameters and numerical apertures. Test results showing coupled power from HP LED sources into 100/140 μ metre and 50/125 μ metre fiber are included.

APPLICATION BULLETIN 68
HP 16800A/16801A Bar Code Reader Configuration Guide for a MICOM Micro280 message concentrator

In some applications, multiple bar code readers may be required to input data to a logging terminal or a central processing unit. However, connecting each unit to a CPU may utilize more input/output ports than desired. A port concentrator will allow several devices to be connected using only one port to the CPU. This application bulletin provides information to aid in configuring the HP 16800A/16801A bar code reader with a MICOM Micro280 Message Concentrator.

Abstracts (cont.)

APPLICATION BULLETIN 69
CMOS Circuit Design Using Hewlett-Packard Optocouplers

Within this application bulletin are CMOS isolation interface circuits for use with the various, low input current, Hewlett-Packard optocouplers, specifically, the HCPL-2200/2300/2731 and 6N139 devices. Advantages of and recommendations for different input and output circuit configurations are given in tabular form for low power operation at various signalling rates.

APPLICATION BULLETIN 70
Green LED Displays and GEN III ANVIS Night Vision Goggle Compatibility

The military is incorporating GEN III Aviator's Night Vision Imaging System (ANVIS) night vision goggles (NVG) to provide vision capability during night operations. Aircraft instrument lighting and other equipment must be compatible with the GEN III ANVIS goggles so as not to interfere with their operation.

NVG compatibility can be achieved with Hewlett-Packard green LED displays when combined with the proper NVG filters. The topics discussed in this application bulletin include a description of the GEN III ANVIS night vision goggles, NVG compatibility problems, the military ANVIS Radiance requirement for NVG compatibility and technical data on NVG filters for use with green LED displays.

APPLICATION BULLETIN 71
200-μm PCS Fiber with Hewlett-Packard Fiber Optic Transmitters and Receivers

A description of the properties of 200-μm PCS fiber is given and the performance when used with Hewlett-Packard fiber optic components is described in the form of graphs and tables.

APPLICATION NOTE 915
Threshold Detection of Visible and Infrared Radiation with PIN Photodiodes

PIN photodiodes are compared with multiplier phototubes in an 11-point summary of their relative merits. This is followed by a description of PIN photodiode device structure, mode of operation, and analysis of the diode's equivalent circuit.

Four pre-amplifier circuits are presented. Two of these describe use of operational amplifiers — one for linear response, the other for logarithmic response. The other two circuits are designed for substantially higher speeds of response, using discrete components to obtain wide bandwidth as well as high sensitivity.

APPLICATION NOTE 934
5082-7300 Series Solid State Display Installation Techniques

The 4N5X, HDSP-07XX/08XX/09XX, and 5082-73XX series Numeric/Hexadecimal indicators are an excellent solution to most standard display problems in commercial, industrial and military applications. The unit integrates the display character and associated drive electronics in a single package. This advantage allows for space, pin and labor cost reductions, at the same time improving overall reliability.

The information presented in this note describes general methods of incorporating this series into varied applications.

APPLICATION NOTE 945
Photometry of Red LEDs

Nearly all LEDs are used either as discrete indicator lamps or as elements of a segmented or dot-matrix display. As such, they are viewed directly by human viewers, so the primary criteria for determining their performance is the judgment of a viewer. Equipment for measuring LED light output should, therefore, simulate human vision.

This application note will provide answers to these questions:

1. What to measure (definitions of terms)
2. How to measure it (apparatus arrangement)
3. Whose equipment to use (criteria for selection)

APPLICATION NOTE 947
Digital Data Transmission Using Optically Coupled Isolators

Optocouplers make ideal line receivers for digital data transmission applications. They are especially useful for elimination of common mode interference between two isolated data transmission systems. This application note describes design considerations and circuit techniques with special emphasis on selection of line drivers, transmission lines, and line receiver termination for optimum data rate and common mode rejection. Both resistive and active terminations are described in detail. Specific techniques are described for multiplexing applications, and for common mode rejection and data rate enhancement.

APPLICATION NOTE 948
Performance of the 6N135/6/7 Series of Optocouplers in Short to Moderate Length Digital Data Transmission Systems

Describes use of HP 6N135/6/7 optocouplers as line receivers in a TTL-TTL compatible NRZ (nonreturn-to-zero) data transmission link. It describes several useful total systems including line driver, cable, terminations, and TTL compatible connections.

APPLICATION NOTE 951-1
Applications for Low Input Current, High Gain Optocouplers

Optocouplers are useful in line receivers, logic isolation, power lines, medical equipment, and telephone lines. This note discusses use of the 6N138/9 series high CTR optocouplers in each of these areas.

Abstracts (cont.)

APPLICATION NOTE 951-2
Linear Applications of Optocouplers

Although optocouplers are not inherently linear, the separate photodiodes used in Hewlett-Packard optocouplers provide better linearity as well as higher speed of response than phototransistor detectors.

Linearity enhancement by use of paired optocouplers is described with specific circuit examples offering DC-to-25 KHz response. These examples illustrate the relative merits of differential and servo techniques.

A circuit with linear AC response to 10 MHz is also described for analog optocouplers having the photodiode terminals externally accessible.

Digital techniques of voltage-to-frequency conversion and pulse width modulation are discussed. Their linearity is quite independent of optocoupler linearity but require use of high speed optocouplers for low distortion.

APPLICATION NOTE 1000
Digital Data Transmission with the HP Fiber Optic System

Fiber optics can provide solutions to many data transmission system design problems. The purpose of this application note is to aid designers in obtaining optimal benefits from this relatively new technology. Following a brief review of the merits, as well as the limitations, of fiber optics relative to other media, there is a description of the optical, mechanical, and electrical fundamentals of fiber optic data transmission system design. How these fundamentals apply is seen in the detailed description of the Hewlett-Packard system. The remainder of the note deals with techniques recommended for operation and maintenance of the Hewlett-Packard system, with particular attention given to deriving maximum benefit from the unique features it provides.

APPLICATION NOTE 1002
Consideration of CTR Variations in Optocoupler Circuit Designs

A persistent, and sometimes crucial, concern of designers using optocouplers is that of the current transfer ratio, CTR, changing with time. The change, or CTR degradation, must be accounted for if long, functional lifetime of a system is to be guaranteed. This application note will discuss a number of different sources for this degradation.

APPLICATION NOTE 1004
Threshold Sensing for Industrial Control Systems with the HCPL-3700 Interface Optocoupler

Interfacing from industrial control systems to logic systems is a necessary operation in order to monitor system progress. This interfacing is found in process control systems, programmable controllers, microprocessor subsystems which monitor limit and proximity switches, environmental sensors and ac line status; in switching power supplies for detection of ac power loss; in power back up systems which need an early warning of power loss in order to save special microprocessor memory information or switch to battery operation, etc. Applications of the HCPL-3700 interface optocoupler are addressed in this note. The isolation and threshold detection capability of the HCPL-3700 allows it to provide unique features which no other optocoupler can provide. Addressed in this note are the advantages of using this optocoupler for isolating systems as well as the device characteristics, dc/ac operational performance with and without filtering, simple calculations for setting desired thresholds, and four typical application examples for the HCPL-3700. Additional coverage is given to protection considerations for the optocoupler from the standpoint of power transients, thermal conditions, and electrical safety requirements of the industrial control environment.

APPLICATION NOTE 1005
Operational Considerations for LED Lamps and Display Devices

In the design of a display system, which incorporates LED lamps and display devices, the objective is to achieve an optimum between light output, power dissipation, reliability, and operating life. The performance characteristics and capabilities of each LED device must be known and understood so that an optimum design can be achieved. The primary source for this information is the LED device data sheet. The data sheet typically contains Electrical/Optical Characteristics that list the performance of the device and Absolute Maximum Ratings in conjunction with characteristic curves and other data which describe the capabilities of the device. A thorough understanding of this information and its intended use provides the basis for achieving an optimum design. This application note presents an in-depth discussion of the theory and use of the electrical and optical information contained within a data sheet. Two designs using this information in the form of numerical examples are presented, one for dc operation and one for pulsed (strobed) operation.

APPLICATION NOTE 1006
Seven Segment LED Display Applications

This application note begins with a detailed explanation of the two basic product lines that Hewlett-Packard offers in the seven segment display market. This discussion includes mechanical construction techniques, character heights, and typical areas of application. The two major display drive techniques, dc and strobed, are covered. The resultant tradeoffs of cost, power, and ease of use are discussed. This is followed by several typical instrument applications including counters, digital voltmeters, and microprocessor interface applications. Several different microprocessor based drive techniques are presented incorporating both the monolithic and the large seven segment LED displays.

Abstracts (cont.)

The application note contains a discussion of intensity and color considerations made necessary if the devices are to be end stacked. Hewlett-Packard has made several advances in the area of sunlight viewability of LED displays. The basic theory is discussed and recommendations made for achieving viewability in direct sunlight. Information concerning display mounting, soldering, and cleaning is presented. Finally, an extensive set of tables has been compiled to aid the designer in choosing the correct hardware to match a particular application. These tables include seven segment decoder/drivers, digit drivers, LSI chips designed for use with LEDs, printed circuit board edge connectors, and filtering materials.

APPLICATION NOTE 1007
Bar Graph Array Applications

This application note begins with a description of the manufacturing process used to construct the 10 element array. Next is a discussion of the package design and basic electrical configuration and how they affect designing with the bar graph array. Mechanical information including pin spacing and wave soldering recommendations are made.

Display interface techniques of two basic types are thoroughly discussed. The first of these two drive schemes is applicable in systems requiring display of analog signals in a bar graph format. The second major drive technique interfaces bar graph arrays in systems where the data is of a digital nature. Examples of microprocessor controlled bar graph arrays are presented.

Summarized for the design engineer are tables of available integrated circuits for use with bar graph arrays. Finally, a list of recommended filters is included.

APPLICATION NOTE 1008
Optical Sensing with the HBCS-1100

This application note gives the basic optical flux coupling design for discrete emitters and detectors. Presents the concepts of modulation transfer function, depth of field, and reflective sensor design. It also discusses the optical and electrical operation of the HBCS-1100 High Resolution optical sensor. Finally, it presents electrical design techniques which allow the HBCS-1100 to interface with popular logic families.

APPLICATION NOTE 1011
Design and Operational Considerations for the HEDS-5000 Incremental Shaft Encoder

This application note is directed toward the system designer using the HEDS-5000 and HEDS-6000 modular incremental shaft encoders. First the note briefly analyzes the theory of design and operation of the HEDS-5000 and HEDS-6000. A practical approach to design considerations and an error analysis provide an indepth treatment of the relationship between motor mechanical parameters and encoding error accumulation. Several design examples demonstrate the analysis techniques presented. Operation considerations for assembly, test, trouble shooting and repair are presented. Finally some circuits and software concepts are introduced which will be useful in interfacing the shaft encoder to a digital or microprocessor based system. Appendix A summarizes the uses and advantages of various encoder technologies while Appendix B provides guidance for selecting DC motors suitable for use with the HEDS-5000 and HEDS-6000.

APPLICATION NOTE 1012
Methods of Legend Fabrication

Hewlett-Packard LED Light Bar Modules inscribed with fixed messages or symbols can be used as economical annunciators. Annunciators are often used in front panels to convey the status of a system, to indicate a selected mode of operation or to indicate the next step in a sequence. This application note discusses alternative ways the message or symbols (legends) can be designed. A selection matrix is provided to assist in the selection of the most appropriate method of legend fabrication. Each fabrication method is explained in detail along with mounting and attachment techniques. Finally, prevention of cross-talk is discussed for legend areas of a multi-segmented light bar.

APPLICATION NOTE 1013
Elements of a Bar Code System

This application note describes in detail the elements that make up most bar code systems. Included is a discussion of the fundamental system design, detailed discussion of 7 popular code symbologies, a section on symbol generation, and methods of data entry. A glossary of terms and a reference section are also included. This is an excellent publication for people who are just learning about bar code, or for those who need a more comprehensive understanding of the subject.

APPLICATION NOTE 1015
Contrast Enhancement Techniques for LED Displays

Contrast enhancement is essential to assure readability of LED displays in a variety of indoor and outdoor ambients. Plastic filters are typically used for contrast enhancement with indoor lighting and glass circular polarized filters are typically used to achieve readability in sunlight ambients.

This application note discusses contrast enhancement technology for both indoor and outdoor ambients, the theory of Discrimination Index and provides a list of tested contrast enhancement filters and filter manufacturers.

APPLICATION NOTE 1016
Using the HDSP-2000 Alphanumeric Display Family

The HDSP-2000 family of alphanumeric display products provides the designer with a variety of easy-to-use display modules with on board integrated circuit drivers. The HDSP-2000 family has been expanded to provide three display sizes with character heights ranging from 3.8 mm (0.15") to 6.9 mm (0.27"), four display colors, and both commercial and military versions. These displays can be arranged to create both single line and multiple line alphanumeric panels.

This note is intended to serve as a design and application guide for users of the HDSP-2000 family of alphanumeric display devices. It covers the theory of the device design and operation, considerations for specific circuit designs, thermal management, power derating and heat sinking, and intensity modulation techniques.

APPLICATION NOTE 1017
LED Solid State Reliability

Light emitting diode display technology offers many attractive features including multiple display colors, sunlight readability, and a continuously variable intensity adjustment. One of the most common reasons that LED displays are designed into an application, however, is the high level of reliability of the LED display. Hewlett-Packard has taken a leadership role in setting reliability standards for LED displays and documenting reliability performance.

This note explains how to use the reliability data sheets published for HP LED indicators and displays. It describes the LED indicator and display packages, defines device failures, and discusses parameters affecting useful life, failure rates and mechanical test performance.

APPLICATION NOTE 1018
Designing with the HCPL-4100 and HCPL-4200 Current Loop Optocoupler

Digital current loops provide unique advantages of large noise immunity and long distance communication at low cost. Applications are wide and varied for current loops, but one of the critical concerns of a loop system is to provide a predictable, reliable and isolated interface with the loop. The HCPL-4100 (transmitter) and HCPL-4200 (receiver) optocouplers provide for easy interfacing to and from a current loop with minimal design effort. Within this application note a complete description of the HCPL-4100/4200 devices is given along with applications for digital, 20 mA, simplex, half duplex and full duplex loops. These loops can be either point-to-point or multidrop configurations. Factors which affect data performance are discussed. Circuit arrangements with specific data performance are given in graphical and tabular form.

APPLICATION NOTE 1019
Using the HLMP-4700/-1700/-7000 Series Low Current Lamps

Hewlett-Packard manufactures a series of LED lamps that are designed for operation at 2 mA DC. These lamps are available in high efficiency red, yellow, and high performance green in a variety of package styles. These lamps allow the designer to reduce system power dissipation, and drive circuit costs.

This application note contrasts electrical characteristics of the low-current lamp with HP's conventional lamp. Costs of implementing lamp drive circuits are discussed, as in power conservation in TTL and circuits involving higher voltages. Finally, telecommunications and battery information are presented.

APPLICATION NOTE 1021
Utilizing LED Lamps Packaged on Tape and Reel

Hewlett-Packard offers many of its LED lamps packaged on tape and reel for radial insertion by automatic equipment during high volume production of PC board assemblies.

This application note is a guide to the use of tape and reel LED lamps in the automatic insertion process. Discussed are the LED lamp tape and reel configuration, the radial lead insertion process, PC board design considerations, a method to maintain LED lamp alignment during soldering and lamp stand-off height information.

APPLICATION NOTE 1022
High Speed Fiber Optic Link Design with Discrete Components

As the technology of fiber optic communication matures, design considerations for large volume applications focus as much on cost and reliability, as bandwidth and bit-error-rate. This application note describes a 100 MBd fiber optic communication link which was implemented with low-cost, non-exotic technology, including LED transmitter, PIN photodiode detector, off-the-shelf ICs and discrete components, laid out on epoxy-glass circuit boards.

APPLICATION NOTE 1023
Radiation Immunity of Hewlett-Packard Optocouplers

Opening with a quotation from MIL-HDBK-279 describing optocouplers containing photodiodes as superior to optocouplers containing phototransistors, the text describes the properties of ionizing radiation (particles and photons) and how it affects the performance of optocouplers. Graphs show degradation of CTR (Current Transfer Ratio) in the 6N140 as a function of gamma total dose (up to 1000 rad [Si] and as a function of total neutron fluence (up to 6×10^{12} n/cm^2). A table gives radiation hardness requirements for various military requirements.

APPLICATION NOTE 1024
Ring Detection with the HCPL-3700 Optocoupler

With the increased use of modems, automatic phone answering equipment, private automatic branch exchange (PABX) systems, etc., low-cost, reliable, isolated ring detection becomes important to many electronic equipment manufacturers. This application note addresses the definition of ringing requirements (U.S.A. and Europe), applications of the HCPL-3700 optocoupler as a simple, but effective, ring detector. A design example is shown with calculations to illustrate proper use of the HCPL-3700. Features which are integrated into the HCPL-3700 provide for predictable detection, protection and isolation when compared to other optocoupler techniques.

Abstracts (cont.)

APPLICATION NOTE 1025
Applications and Circuit Design for the HEDS-7500 series Digital Potentiometer

This application note demonstrates some of the uses for the Hewlett-Packard HEDS-7500 series digital potentiometer, explains how a digital potentiometer works, and explains some of the advantages of a digital potentiometer over a standard resistive potentiometer. In addition, this application note provides some examples of circuitry which will interface the digital potentiometer to a microprocessor, and provides mechanical design considerations and available options for the HEDS-7500 series digital potentiometer.

APPLICATION NOTE 1026
Designing with Hewlett-Packard's Smart Display — The HPDL-2416

The trend in LED Alphanumeric displays is to simplifiy a designer's job as much as possible by incorporating on board character storage, ASCII character generation, and multiplexing within the display. The HPDL-2416 is a four character alphanumeric display which incorporates a 64 character ASCII decoder and an on board CMOS IC to perform these functions. This application note is intended to serve as a design and application guide for users of the HPDL-2416. The information presented will cover: electrical description, electrical design considerations, interfacing to micro-processors, pre-programmed message systems, mechanical and electrical handling, and contrast enhancement.

APPLICATION NOTE 1027
Soldering LED Components

The modern printed circuit board is assembled with a wide variety of semiconductor components. These components may include LED lamps and displays in combination with other components. The quantity of solder connections will be many times the component count. Therefore, the solder connections must be good on the first pass through the soldering process. The effectiveness of the soldering process is a function of the care and attention paid to the details of the process. It is important for display system designers and PC board assembly engineers to understand the aspects of the soldering process and how they relate to LED components to assure high yields.

This application note provides an in depth discussion on the aspects of the soldering process and how they relate to LED lamps and display components, with the objective of being to serve as a guide towards achieving high yields for solder connections.

APPLICATION NOTE 1028
Surface Mount Subminiature LED Lamps

Modern printed circuit boards are being assembled with surface mounted components, replacing through hole mounted components in many traditional applications. Hewlett-Packard has surface mount options for its HLMP-6000/7000 series of subminiature LED lamps, Options 011 and 013 for "gull wing" leads and Option 021 for "yoke" leads for inverted mounting.

This application note provides information on how to surface mount and vapor phase reflow solder these surface mount subminiature LED lamps.

TECHNICAL BRIEF 101
Fiber Optic SMA Connector Technology

Technical Brief 101 discusses tradeoffs between various SMA connector techniques and provides a contact matrix of manufacturers versus SMA connector type.

TECHNICAL BRIEF 102
Fiber/Cable Selection for LED Based Local Communications Systems

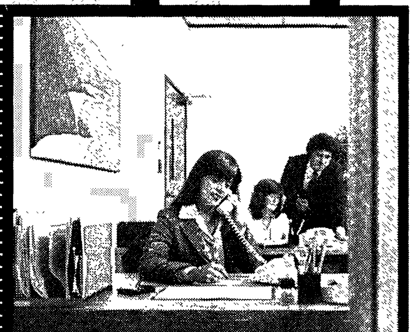
Technical Brief 102 is intended to assist the first time user of fiber optics with the selection of a fiber cable that best meets desired system requirements. Issues discussed in Technical Brief 102 include: Tradeoffs between various fiber types, the effect of LED emitters on fiber performance, coupled power versus numerical aperture and factors that influence cable selection. A contact matrix that lists fiber cable manufacturers versus cable type is also included.

TECHNICAL BRIEF 103
High Speed Optocouplers vs. Pulse Transformers

For high speed signaling with ground loop isolation, pulse transformers are often used. Here are summarized briefly the difficulties encountered in the use of pulse transformers, such as rise-time, sag, and interwinding capacitance. A table summarizes the parameters of Hewlett-Packard optocouplers designed for high speed signaling. A second table summarizes the advantages of using these optocouplers instead of pulse transformers.

[redacted]

10. Appendix



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ABOUT HEWLETT-PACKARD

David Packard and William Hewlett founded the company as a partnership in Palo Alto, California in 1939. Worldwide sales in fiscal year 1984 totalled U.S. $6.04 billion. International sales accounted for almost 43% of this figure.

PEOPLE

Worldwide employment is over 83,000 with 26,000 employees outside the United States.

PRODUCTS

The company designs, manufactures, and markets measurement and computation products and systems used in business, industry, science, engineering, education, and medicine.

FACILITIES

Hewlett-Packard has manufacturing facilities the United States, Canada, Latin America, Europe, and Asia. The company has established joint ventures in Japan, the People's Republic of China, Mexico, and South Korea. Hewlett-Packard has 330 sales and support activities in 76 countries. Intercontinental Operations headquarters and HP's corporate offices are located in Palo Alto, California. European Operations are headquartered in Geneva, Switzerland.

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HEWLETT PACKARD

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