HEWLETT PACKARD

ENGINEERING REFERENCE PACKAGE

7908 DISC/TAPE DRIVES

Manual part no. 07908-90907

Printed: JUN 1984 07908-90907
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PRINTING HISTORY

New editions incorporate all update material since the previous edition. Changes, when issued between editions, will contain additional and revised information to be incorporated into the document by the user. The date on the title page changes only when a new edition is published.

First Edition .... JUN 1984

NOTICE

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P/N 07908-60007

REGULATOR PCA-A1

Series Code F-2301

ER48 D/H: 50A

HEWLETT-PACKARD CO. / hp /

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting cutline). (L403)

LTR	REVISIONS	DATE	INIT	M F
A	AS ISSUED PER PCO 48-6021	10-20-82	sr/ML	M

LT	P.C. #	APPR	DATE		
A	48-6021	sr/ML	10-20-82	MODEL 7908	STK # 07908-60007
		/	- -	REGULATOR - IMS	
		/	- -	BY	DATE APR 30, 1984
LT	P.C. #	APPR	DA[illegible]	APPD	SHEET # 1 OF 15
REVISIONS				SUPERSEDES	DWG # A-07908-60007-5

IMS FOR THE REGULATOR BOARD
(07908-60007)

Note: The 7908 power supply is composed of two assemblies:
1) the rectifier assembly, 07908-60011, and
2) the regulator board, 07908-60007.

This document represents one-half of the IMS for the 7908 power supply.

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A. ELECTRICAL COMPONENTS

1. Zener Reference Diode: 1902-0692

The stability of the reference voltage over a wide range of operating conditions is vital for the proper regulation of the supply voltages. This 6.3v zener diode is temperature compensated and specified to be within one percent of the nominal value at its specified current.

2. Precision Resistor Network: 1810-0548

Precision 10k resistor networks are used to minimize errors due to component tolerances in the reference voltage circuit and the regulated voltage feedback to the controlling op-amps. The resistance between packs is specified to be within 0.5% of the nominal value. Within a given resistor network, the resistors will be within 0.5% of each other.

3. Controlling Op-Amp
   a. +5v supply (LM 307N): 1820-0493

The LM 307N op-amp is used to control the +5v regulator circuit because its input voltages can equal its positive supply voltage.

III. CRITICAL COMPONENTS AND MATERIALS (CONT)

b. +/-12v supplies (MC1458): 1826-0139

The MC1458 dual op-amp is preferable to the pin compatible MC4558 because it has a wider differential input voltage range and a single pole frequency response. Initially the MC4558 was used as the controlling op-amp in the +/-12v supplies until it was observed that op-amps were occasionally destroyed by input signals within their specified differential input voltage range. Tests conducted by Rick Wells showed that the MC4558 would break down for differential input voltage of +/-15v rather than for +/-30v as the device is specified.

4. Driver Transistor
   a. NPN (TIP 41A): 1854-0456
   b. PNP (TIP 42A): 1853-0234

These transistors are employed based upon their ready availability, TO-220 package type, maximum power dissipation of 65w at 25C, and a current gain of 15 to 75 at a collector current of three amps.

5. Pass Transistor
   a. NPN (2N5885): 1854-0679
   b. PNP (2N5883): 1853-0425

Selection of the pass transistors is based upon their extremely low collector to emitter saturation voltage of 1.0v max, current gain of 20 to 100 at a collector current of ten amps, a maximum junction temperature of 200C, and low cost.

6. Driver Emitter Resistor (10 ohm): 0698-3601

The choice of this resistor is based upon its power dissipation ability and potential as an auto-insertable part.

III. CRITICAL COMPONENTS AND MATERIALS (CONT)

7. Current Sense Resistor (0.01 ohm): 0811-3511

   An accurate, low resistance, power resistor is needed to sense the current drawn by the two pass transistors used in the +5v regulator circuit.

8. Op-amp Bypass Capacitors
   a. 100 pf: 0160-2204
   b. 470 pf: 0160-3533
   c. 1000 pf:0160-2218
   d. 0.01 uf: 0160-0161

   Fixed dip mica and mylar film capacitors are used to compensate the regulating op-amps and stabilize the circuit response to abrupt changes in the load current. The choices of these capacitors is due to their good frequency response characteristics and Ready availability.

9. Matched Diode Pack: 1906-0248

   It is preferrable to use matched diodes in the under-voltage detect circuit to eliminate measurement error due to unequal diode voltage drops. Important specifications used in choosing this device are its forward current specification of 400mA, total power dissipation ability of 600mW, and peak reverse voltage of 40V.

10. Power Rectifier Diodes
    a. General Purpose (1N4004): 1901-0743
    b. High Current (A15A): 1901-0673

    Selection of the power rectifier diodes for use in the overvoltage circuit is based upon their current ratings - average continuous rectified current and peak surge current. Their specifications are:

    a. 1N4004- 1A maximum, 30A maximum surge;
    B. A15A- 5A maximum, 125A maximum surge.

11. Silicon-Controlled Rectifier: 1884-0268

    Important characteristics of the SCR are its average rectified current (25A), peak surge current (300A), peak gate power rating (20W), and the TO-220 mechanical package type.

12. Thermal Switch: 3103-0093

    The thermal switch is designed to have contacts which are capable of switching current loads from 10mA to 2A. Some vital characterisics of the thermal switch are:
    a. close on temperature rise at 200F +/- 8F;
    b. open on temperature fall at 120F +/- 8F;
    c. gold flash on the contacts to allow switching at very low currents;
    d. mechanical package design affords easy assembly of the thermal switch onto the side of the heat sink.

III. CRITICAL COMPONENTS AND MATERIALS (CONT)

B. MECHANICAL COMPONENTS AND MATERIALS

1. Heat Sink: 07908-20002
   a. Mechanical Design

   The heat sink is an aluminum extrusion with multiple fins. Mounting holes for eight TO-3 transistors, eight TO-220 transistors, and two thermal switches are machined by the heat sink manufacturer. All of the mounting locations are not being used presently but were included for flexibility in future designs. The flatness specification for Thermalloy's standard extrusion is 0.004 inches per linear inch.

   b. Materials

   Aluminum is used because of its low thermal resistance, approximately one degree C per watt, and it is easily extruded and machined.

2. Transistor Insulators
   a. TO-3
   Hard anodized aluminum: 1200-0043

   Hard anodized aluminum insulators are used for the power transistors because of their low thermal resistance and ready availabilty. The necessity of coating the insulators with heat sink compound is a disadvantage of this type of insulator from a manufacturing point of view. The silicone rubber impregnated insulators were avoided due to tearing and cracking of the insulators which resulted in electrically shorting the transistors to the heat sink.

2. Transistor Insulators (cont)
   a. TO-3 (cont)
      Pre-coated Mica (INSUL-COTE): 0340-0978

      The mica insulators that are pre-coated with thermal compound are less expensive, easier to assemble, and more uniformly coated than their discrete counterparts mentioned above. An automatic dispensing machine, on loan from Thermalloy, is being used on the production line at present.

   b. TO-220
      Thermalfilm: 0340-0473

      A polyimide plastic insulator is used with each TO-220 package transistor. These insulators must be coated with thermally conductive compound.

      Pre-coated Thermalfilm: 0340-xxxx

      In the manual coating procedure, several insulators are placed between two sponges that are saturated with thermal compound. Dust, dirt, and metal leads can contaminate the sponges, stick to the insulators, and cause serious board failures. As a test case, pre-coated Thermalfilm transistor insulators and a dispensing machine are being examined by P.C. production for use in the assembly process.

3. Insulating Washers for Transistors
   a. TO-3 Insulating Flange Bushing: 1200-0081

      The screws used to attach the TO-3 transistors to the heat sink and the heat sink to the p.c. board also provide the electrically conductive path from the case (collector) of the transistor to the pad on the board. Nylon bushings are used to insulate the screws from the heat sink. Six additional nylon bushings are required to ensure that the heat sink is elevated a uniform distance above the p.c. board. The extra bushings limit wobble of the heat sink under vibration and prevent electrical/mechanical contact of the heat sink and the p.c. board.

   b. TO-220 Shoulder Washer: 3050-1021

      Shoulder washers, made of polyphenylene sulfide, are used to insulate the tab of the TO-220 transistors from the heat sink. The diameter of the mounting hole in the tab of the TO-220 packaged transistors has not been standardized among the various manufacturers. This shoulder washer is designed to mechanically fit any and all TO-220 packages.

4. Input Voltage Connector: 1251-5535

   Selection of this connector is based largely upon mechanical design constraints. The connector assembly can not extend past the edge of the p.c. board without interfering with the rear panel. This right-angle connector has ten pins and is capable of carrying seven amps per pin. The Fan-Rectifier cable, 07908-60024, connects the regulator board via this connector to the rectifier assembly.

IV. Electrical Function of the Regulator Board

A. Theory of Operation

1. Objectives and Constraints

The power dissipation of the regulator circuit, particularily the pass transistors, had to be minimized to allow the printed circuit board to be placed in the card cage and cooled adequately. A scheme of preregulating the voltages impressed upon the pass transistors is employed to curtail the power dissipation and increase the operating efficiency of the power supply. See the IMS for the Rectifier Assembly, 07908-60011, for the theory of operation of the pre-regulation circuit.

2. Regulator Board Input and Output Voltage and Current Specifications

Four voltages are impressed upon the regulator board from which six regulated voltages are derived. Table 7.1 on the following page lists all of the inputs and outputs for the regulator board and typical values. In addition two digital signals, Master Reset (MRST-L) and Possible Power Fail (PFAIL-L), are sent to the drive electronics from the regulator board. These signals are used under power on, power off, and power fail conditions. During normal operation of the drive, PFAIL-L and MRST-L are in the high state (+5V.)

Table 7.1

Output Voltage	Unregulated Input Voltage (average) at Rated Current	Rated Current	Purpose/Comments
+5V -2%,+5%	dc= 7.75V ripple= 1.5Vp-p	10A	+5v is used by all p.c. boards and tape drive. Turn-on of +5V occurs after +12L is up.
+12VS -5%,+5%	dc= 17.0V ripple= 2.0Vp-p	4A	+12VS powers the IMI spindle and voice coil. There is no delay at turn-on.
+12T -5%,+5%	dc= 17.0V ripple= 2.0Vp-p	1A/ 4A surge	+12T is used by the tape module alone. Turn-on is dependent upon +5V.
+12L -5%,+5%	dc= 17.0V ripple= 2.0Vp-p	1A	+12L is used to supply electronic components on all p.c. boards. This supply turns on immediately.
-12VS -5%,+5%	dc= -17.0V ripple= 2.0Vp-p	4A	The -12VS is used to operate the IMI spindle and voice coil. This supply turns on immediately.
-12L -5%,+5%	dc= -17.0V ripple= 2.0Vp-p	1A	-12L is used to supply the electronics on the pc bds. There is no delay in turn-on of the supply.
+12V UN	dc= 17.0V ripple= 2.0Vp-p	1A	+12V UN is sent to the motherboard, but is not presently used.
-12V UN	dc= 17.0V ripple= 2.0Vp-p	1A	-12V UN is sent to the motherboard, but is not presently used.

3. Sequencing of the Regulated Supply Voltages

a. Turn-on

The turn-on of the regulated voltages is coordinated and sequenced when powering up the drive. When power is applied to the regulator board the +12VS, +12L, -12VS, and -12L supplies begin immediately. The +5V supply is dependent upon +12L being within its specified voltage limits. The +12T supply, which operates the tape module, is required to be held off until the +5V supply is within its acceptable voltage range. There is no specified time delay between the turn-on of each supply; instead, the +12T supply is dependent upon the voltage level of the +5V supply. In powering up the drive MRST-L initiates assumption of microprocessor control of the disc drive first, followed by the tape drive.

b. Turn-off

When the power is shut off for any reason, PFAIL-L will fall low (0V) to warn the electronics of the impending loss of power. After a time delay of no less than 700 microseconds, MRST-L will assert (fall low) indicating that the power supplies are at their minimum acceptable voltage level. The time delay between PFAIL-L and MRST-L allows the microprocessor controlling the disc to complete its operations in an orderly fashion. The shut down of the tape drive will not be orderly because it would require about thirty milliseconds to finish writing a block! After MRST-L is set low, the drive electronics will not be operational.

4. Basic Circuit Configuration

a. Description

The circuit topology used is the "backwards" pass transistor in a linear, series regulation circuit, see Figure 7.1. The advantage of this circuit design is that the power transistors will continue to operate for input voltages only the transistor collector-to-emitter saturation voltage greater than the regulated output voltage. By choosing power transistors with an extremely low collector-to-emitter saturation voltage the circuit operating range is maximized and device power dissipation is minimized. The feedback capacitors around the op-amps stabilize the circuit response to step changes in the current load. The values of the capacitors chosen were based primarily on empirical evidence. Any resistive element introduced into the feedback was found to make the circuit unstable.

b. Generic Schematic Diagram

5. Re[illegible] [illegible]upply Description

a. [illegible] Supply

Based on calculations of junction temperature by Dan Michaud, it was determined that two transistors should share the 10A current. One supply consisting of U222, Q114, and Q136 is very similar to the +12VS, +12V and +12L supplies without the precision attenuation in the feedback. The master supply matches its reference voltage. The other SLAVE supply consisting of U148, Q196 and Q174 looks at the current through R162 and causes that current to pass through R144. Because of the low dissipation, low voltage drop requirements, R162 and R144 are 10 milliohm resistors. This puts the voltage across these resistors into the 10 to 50mv range where input offset voltages on U148 are quite important. Since the SLAVE circuit is a current matching arrangement, it will wrongly match a non-existent current due to an error in input offset voltage. Thus acting as a current source, the full unregulated voltage may be applied to a small load. To overcome this problem the SLAVE is held off by pulling approximately 1ma (more when the unregulated voltage is higher corresponding to smaller loads) through the parallel combination of R124 and R128. Typically, the current to the +5V load must be 1 amp before the SLAVE circuit starts to conduct current. R124 and R128 form an attenuator for the voltage drop across R144, so that the SLAVE gets an under estimate of its current. It therefore contributes more than half the incremental current once it gets rolling. At the 10 amp level, typically both circuits are carrying 5 amps.

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60007
07908-66007
07908-68007

DATE CODE : F-2300 and 2301

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C126	0180-0291	CAP 1UF 10%
C150	0160-2218	CAP 1000PF 5%
C160	0160-0161	CAP .01UF 10%
C210	0160-2218	CAP 1000PF 5%
C212	0160-2218	CAP 1000PF 5%
C214	0160-2218	CAP 1000PF 5%
C216	0160-2218	CAP 1000PF 5%
C224	0160-2218	CAP 1000PF 5%
C226	0160-2218	CAP 1000PF 5%
C232	0160-2204	CAP 100PF 5%
C238	0160-2204	CAP 100PF 5%
C252	0160-2204	CAP 100PF 5%
C256	0160-2204	CAP 100PF 5%
C258	0160-0127	CAP 1UF 20%
C306	0160-2204	CAP 100PF 5%
C310	0160-3879	CAP .01UF 20%
C312	0160-2218	CAP 1000PF 5%
C318	0160-3533	CAP 470PF 5%
C332	0180-0692	C-F 220UF 35V AL
C334	0180-0094	CAP 100UF-10+75%
C356	0180-0692	C-F 220UF 35V AL
C364	0180-0692	C-F 220UF 35V AL
C376	0180-0692	C-F 220UF 35V AL
C384	0180-0692	C-F 220UF 35V AL
C392	0180-0692	C-F 220UF 35V AL
CR106	1901-0040	DIODE-SWITCHING
CR108	1901-0040	DIODE-SWITCHING
CR112	1901-0040	DIODE-SWITCHING
CR166	1901-0040	DIODE-SWITCHING
CR193	1901-0040	DIODE-SWITCHING
CR195	1901-0040	DIODE-SWITCHING
CR202	1901-0040	DIODE-SWITCHING
CR264	1901-0743	DIO-1N4004
CR266	1901-0743	DIO-1N4004
CR276	1901-0743	DIO-1N4004
CR282	1901-0743	DIO-1N4004
CR288	1901-0743	DIO-1N4004
CR292	1901-0743	DIO-1N4004
CR354	1901-0743	DIO-1N4004
CR368	1901-0743	DIO-1N4004
CR370	1901-0743	DIO-1N4004
CR380	1901-0743	DIO-1N4004
CR390	1901-0743	DIO-1N4004
J138	1251-5535	CONN 10-PIN M
MP1	7120-6830	LABEL-INFO
MP10	1480-0116	PIN GRV .062X.25
MP12	2200-0600	SCREW-MACHINE

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60007
07908-66007
07908-68007

DATE CODE : F-2300 and 23

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
MP14	1200-0043	INSL-XSTR TO3 AL
MP15	1200-0081	INSUL-FLG-BSHG
MP16	0403-0451	EXTR-PC BD #1
MP2	07908-80007	BD-ETCHED
MP3	07908-20002	HEAT SINK-REG
MP4	0340-0473	INSUL-XSTR
MP5	3050-1021	WSHR-SHLDR
MP6	2200-0602	MS#4-40 .375 L
MP7	6040-0239	COMPOUND-THERMAL
MP8	2260-0009	NUT 4-40 W/LK
MP9	0624-0541	MS 6-20 .25L TX
Q105	1854-0456	TRANS TIP 41A
Q107	1854-0456	TRANS TIP 41A
Q110	1854-0456	TRANS TIP 41A
Q114	1854-0456	TRANS TIP 41A
Q130	1853-0425	XSTR PNP 2N5883
Q132	1853-0425	XSTR PNP 2N5883
Q134	1853-0425	XSTR PNP 2N5883
Q136	1853-0425	XSTR PNP 2N5883
Q170	1854-0679	XSTR NPN 2N5885
Q172	1854-0679	XSTR NPN 2N5885
Q174	1853-0425	XSTR PNP 2N5883
Q192	1853-0234	TRANSISTOR
Q194	1853-0234	TRANSISTOR
Q196	1854-0456	TRANS TIP 41A
Q358	1884-0268	THYR-2N6508 SCR
Q374	1884-0268	THYR-2N6508 SCR
Q388	1884-0268	THYR-2N6508 SCR
R116	0698-3601	RES 10 5% 2
R118	0698-3601	RES 10 5% 2
R120	0698-3601	RES 10 5% 2
R121	0698-3601	RES 10 5% 2
R122	0698-3403	RES 348 1% .5
R124	0698-3435	RES 38.3 1%.125
R128	0757-0346	RES 10 1%.125
R140	0757-0279	RES 3.16K 1%.125
R142	0757-0279	RES 3.16K 1%.125
R144	0811-3511	RES .01 1% 2W
R146	0757-0280	RES 1K 1%.125
R152	0757-0280	RES 1K 1%.125
R162	0811-3511	RES .01 1% 2W
R168	0757-0401	RES 100 1%.125
R178	0698-3601	RES 10 5% 2
R182	0698-3601	RES 10 5% 2
R186	0698-3601	RES 10 5% 2
R206	0757-0280	RES 1K 1%.125
R230	0757-0439	RES 6.81K 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60007
07908-66007
07908-68007

DATE CODE : F-2300 and 2301

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R246	0757-0439	RES 6.81K 1%.125
R250	0757-0470	RES 162K 1%.125
R254	0757-1094	RES 1.47K 1%.125
R262	0757-0466	RES 110K 1%.125
R302	0698-3439	RES 178 1% .125W
R308	0757-0442	RES 10K 1%.125
R314	0757-0438	RES 5.11K 1%.125
R320	0698-3152	RES 3.48K 1%.125
R322	0698-3161	RES 38.3K 1%.125
R324	0698-3155	RES 4.64K 1%.125
R326	0757-0464	RES 90.9K 1%.125
R328	0757-0278	RES 1.78K 1%.125
R336	0757-0398	RES 75 1%.125
R340	0757-0428	RES 1.62K 1%.125
R342	0757-0290	RES 6.19K 1%.125
R346	0698-3154	RES 4.22K 1%.125
R347	0757-0439	RES 6.81K 1%.125
R348	0757-0447	RES 16.2K 1%.125
R349	0757-0459	R:F 56.2K 1%.125
R350	0698-3155	RES 4.64K 1%.125
R352	0757-0274	RES 1.21K 1%.125
R360	0698-3444	RES 316 1%.125
R362	0698-3435	RES 38.3 1%.125
R372	0698-3435	RES 38.3 1%.125
R386	0698-3435	RES 38.3 1%.125
S190	3103-0093	SWITCH-THERMAL
TP101	0360-1682	TERM-PIN
TP102	0360-1682	TERM-PIN
TP154	0360-1682	TERM-PIN
TP156	0360-1682	TERM-PIN
TP158	0360-1682	TERM-PIN
TP164	0360-1682	TERM-PIN
TP176	0360-1682	TERM-PIN
TP180	0360-1682	TERM-PIN
TP184	0360-1682	TERM-PIN
TP188	0360-1682	TERM-PIN
TP192	0360-1682	TERM-PIN
U148	1820-0493	IC LM307N
U204	1810-0338	NETWORK-.1KX8
U218	1826-0139	IC MC1458 P1
U220	1826-0139	IC MC1458 P1
U222	1820-0493	IC LM307N
U228	1810-0455	NETWORK-RES DIP
U236	1810-0548	NETWOKRK-10KX8
U240	1826-0139	IC MC1458 P1
U242	1826-0138	IC LM339
U260	1810-0338	NETWORK-.1KX8

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60007
07908-66007
07908-68007

DATE CODE : F-2300 and 2301

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U304	1826-0138	IC LM339
U330	1810-0548	NETWOKRK-10KX8
U344	1906-0248	DIODE-ARRAY
VR123	1902-3046	DIODE ZNR 3.48V
VR208	1902-0692	DIO-ZNR 6.3V 1%
VR263	1902-3104	DIODE BD 5.62V
VR281	1902-3193	DIODE ZNR 13.3V
VR378	1902-3193	DIODE ZNR 13.3V

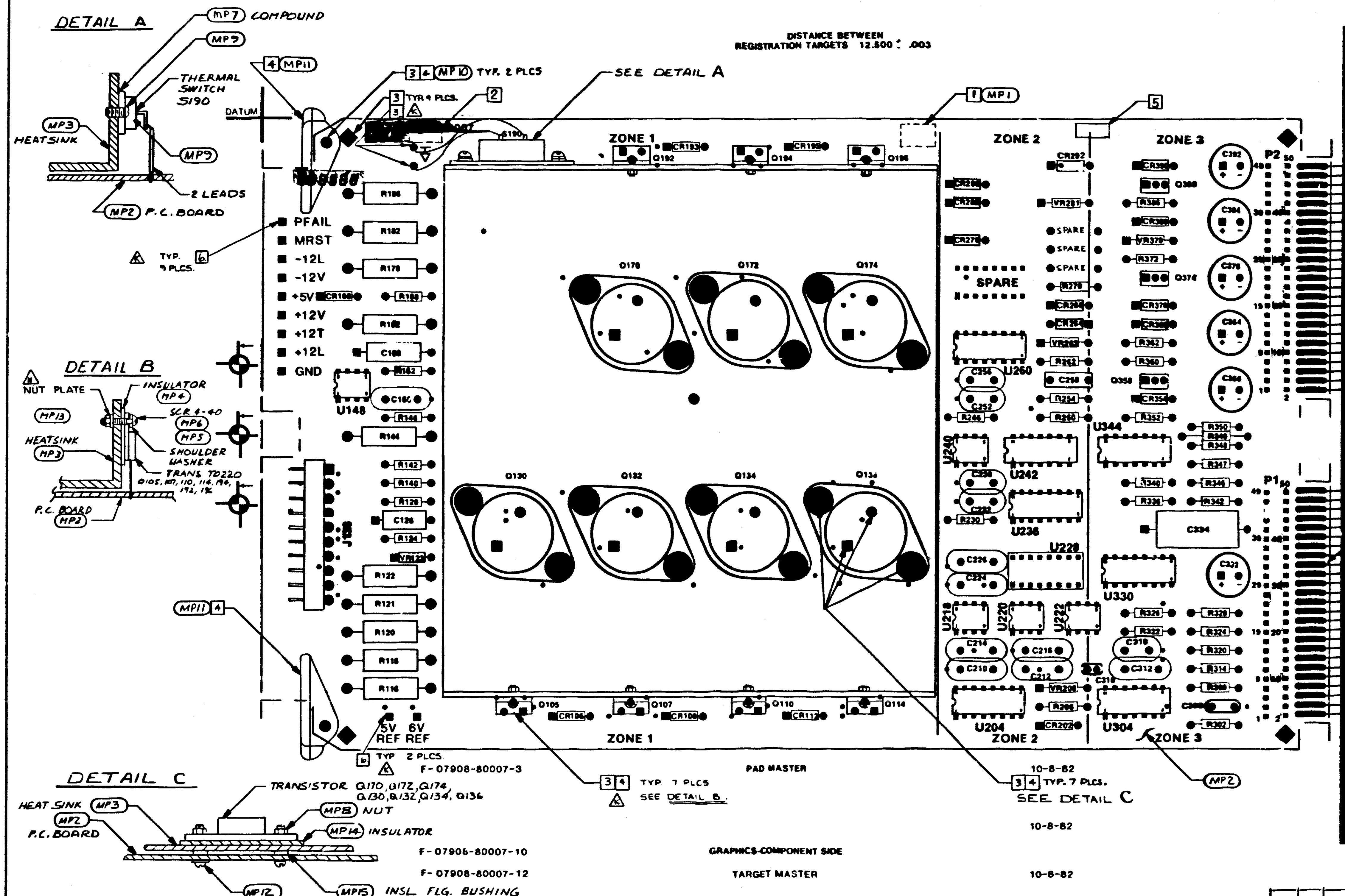
END OF MATERIAL LIST.

SYM	REVISIONS CONT	APPROVED	DATE
K	ADDED NOTE 6; DELETED HARDWARE DESCRIPTION PER PCO 48-4672	KT/ML	10/1/82
L	DATE CODE WAS E-2205; BD REV WAS E, PER PCO 48-4968	KT/ML	10/2/82
M	DATE CODE WAS 2232 PER PCO 48 0015	KT/ML	4/20/83
N	REV'D PER C0480792	ML	5/11/84

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		2-27-81
B	ENLARGE B; BD REV'D TO B / PC 48-4064		
C	BOARD REV TO C / PC48-4085		4-1-81
D	NOTE 2 WAS 2108; BD REV WAS C PER PC 48-4136		6/2/81
E	DATE CODE WAS D-2118 PER PC48-4191		
F	BD. REV. WAS D PER PC 48-4199		
G	ADDED SPARES & PLACEMENT OF NOTE 3 PER PPCO 48-4314	MTS/ML	
H	DATE CODE WAS 2126 PER PPCO 48-4359.	KT/ML	11/18/81
J	DATE CODE WAS E-2140 PCO 48-4624	KT/ML	/82

~ CONT. ~

DISTANCE BETWEEN REGISTRATION TARGETS 12.500 ± .003



REFERENCE DRAWINGS:

SCHEMATIC D-07908-60007 -50

UNLESS OTHERWISE SPECIFIED:

1. THIS BOARD CONFORMS TO CORPORATE AUTOMATIC INSERTION STANDARDS AS PER AXIAL LEAD MANUAL DATED 4-80.
2. THIS BOARD CONFORMS TO UNIVERSAL TEST FIXTURES. ALL COMPONENT HOLES ARE ON ONE-TENTH GRID CENTERS.

NOTES:

1. INSTALL MP1 AFTER LINE TEST.
2. OPR. 264: MARK ASSEMBLY DATE CODE F-2301.
3. OPR. 265: MASK PRIOR TO LOADING.
4. OPR. 266: TOUCH UP, INSTALL MP3 THRU MP15
5. P.C. PRODUCTION: MARK ASSEMBLY WORK ORDER NUMBER.
6. OPR. 265: INSTALL TEST PINS.

1-23-81	REGULATOR PCA ASSEMBLY
	HEWLETT PACKARD
2-27-81	SEE WHERE USED
	07908-60007
SCALE 2:1	F-07908-60007-1

F-07908-60007-1

ER48 D/H: 50A/50B

hp

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LTR	REVISIONS	DATE	INIT	M F
A	AS ISSUED	12-02-81	SB/ML	M
B	CORRECTED PG 2, ADDED APPENDIX A PER PPCO 48-4364	1-04-82	SR/ML	M
C	REVISED PER DATE CODE B,E-2203, PER PCO 48-4624	2-12-82	JMM/ML	M
D	REVISED PER DATE CODE F-2232 PER PCO 48-4968	10-13-82	SR/ML	M
E	CHANGED MRST TIMING PER PCO 48-6354	6-21-83	CR/ML	
F	ADDED DATE CODE 2301 PER C0480015	6-28-83	CR/ML	

D	48-4968	SR/ML	10-13-82	MODEL 7908	STK # 07908-69007
E	48-6354	CR/ML	6-21-83	UPDATE/REVISION PROC	
F	C0480015	CR/ML	6-28-83	BY	DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 6
REVISIONS				SUPERSEDES	DWG # A-07908-69007-1

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UPDATING AND REVISION PROCEDURE

07908-69007

This procedure contains instructions for modification of the regulator PCA, 07908-60007 to version 07908-69007.

REFERENCES:

SML:	07908-68007	Untested PCA
	07908-66007	Reel
Dwgs:	F-07908-60007-1	Assembly Dwg.
	D-07908-60007-50	Schematics
	A-07908-60007-2	Test procedures
	A-07908-60007-3	Debug procedures
	07908-80007	Tape masters

Production Changes:

48-4085	Fix shorted pins P2-43,44
48-4087	Change U344 from 1906-0249 to 1906-0248 (non-mandatory)
48-4092	Change R206 to 1K (0757-0280)
48-4100	Change VR281,VR378 to 1902-3193 (13.3V zener)
48-4136	Adds rework for MRST,output load, SCR's
48-4144	Change C318 to 470pf (0160-3533), adds 100 pF from U222-3 to ground
48-4191	Change R328 to 1.78K, change U228 to DIP resistor
48-4199	Implements Rev E board
48-4339	Implements change in Rev B rework
48-4624	Improves margins for triggering SCR crowbar circuits
48-4968	Implements Rev F Board
C0480015	Stopped using thermal compound (Non-mandatory Change)

D	48-4968	SR/ML	10-13-82	MODEL 7908	STK # 07908-69007
E	48-6354	CR/ML	6-21-83	UPDATE/REVISION PROC	
F	C0480015	CR/ML	6-28-83	BY	DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 2 OF 6
REVISIONS			SUPERSEDES		DWG # A-07908-69007-1

/ hp /

H E W L E T T - P A C K A R D C O.

INTRODUCTION:

This article will provide information concerning the eligibilty of the regulator board for revision and also concerning the revisions themselves.

REVISABLE ASSEMBLIES:

The first assembly which may be revised is B-2108. All prior assemblies are to be scrapped. Also scrap any C or D revision boards.

REVISIONS:

B-2108	48-4100,4092,4087,4085
B-2118	48-4136,4144
B-2126	48-4191
E-2126	48-4199
B,E-2140	48-4339
B,E-2203	48-4624
F-2232	48-4968
F-2300	48-6354

CURRENT ASSEMBLY:

B,E-2300; F-2300

F-2301

D	48-4968	SR/ML	10-13-82	MODEL 7908	STK # 07908-69007
E	48-6354	CR/ML	6-21-83	UPDATE/REVISION PROC	
F	C0480015	CR/ML	6-28-83	BY	DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 3 OF 6
REVISIONS				SUPERSEDES	DWG # A-07908-69007-1

HEWLETT-PACKARD CO. hp

1.0 Inspect all boards for general mechanical and cosmetic defects per A-5950-9205-1. Repair all component malfunctions.

2.0 Identify all boards with the following logo:

07908-69007

2300

To replace existing logo.

3.0 Affix, near the logo, a 7120-5480 label which has been stamped with the month and year of final inspection.

D	48-4968	SR/ML	10-13-82	MODEL 7908	STK # 07908-69007
E	48-6354	CR/ML	6-21-83	UPDATE/REVISION PROC	
F	C0480015	CR/ML	6-28-83	BY	DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 4 OF 6
REVISIONS			SUPERSEDES		DWG # A-07908-69007-1

4.0 On board revision: B-2108 (to get 2118)

A) Insure that the trace from P2-44 to nearest feedthru has been cut. Also that there is a wire from U242-14 to P2-44. See Mod. Dwg. F-07908-60007-20.

B) Note: U344 may be either 1906-0249 or 1906-0248

C) If R206 is not 1.0K ohms, replace with 0757-0280.

D) If VR281 and VR378 are not 13.3V replace with 1902-3193.

E) If U262 has a 1K network resistor loaded, replace with a 5.11K (0757-0438) in the location for pins 3,14. Refer to Mod. Dwg. F-20 and Assy Dwg. F-1.

F) Make other modifications per F-07908-60007-20

G) If C318 is 100 pf replace with 470 pf (0160-3533) add 100 pF (mod 10) 0160-2204 from U222-3 to ground. Refer to Mod. Dwg. F-07908-60007-20.

4.1 On board revision: B-2118 (to get 2126)

A) Replace R328 with 1.78K (0757-0278)

B) If the header at U228 is defective, remove and replace with 57K network resistor (1810-0455). If the header is good, do not replace it.

4.2 On board revision: B-2126 (to get 2140)

A) Move resistor and zener diode from connector area to spare DIP location and put on test pins.

B) Install eyelet on edge commector finger and install jumper. (Rework current jumper).

Refer to Mod. Dwg. F-07908-60007-20 Rev C.

4.3 On board revision B,E-2140 (to get 2203)

A) Remove resistors R362, R372, R386 and replace with 38.3 ohm resistor (0698-3435).

4.4 On board revision B, E- 2203; F-2232 (to get 2300)

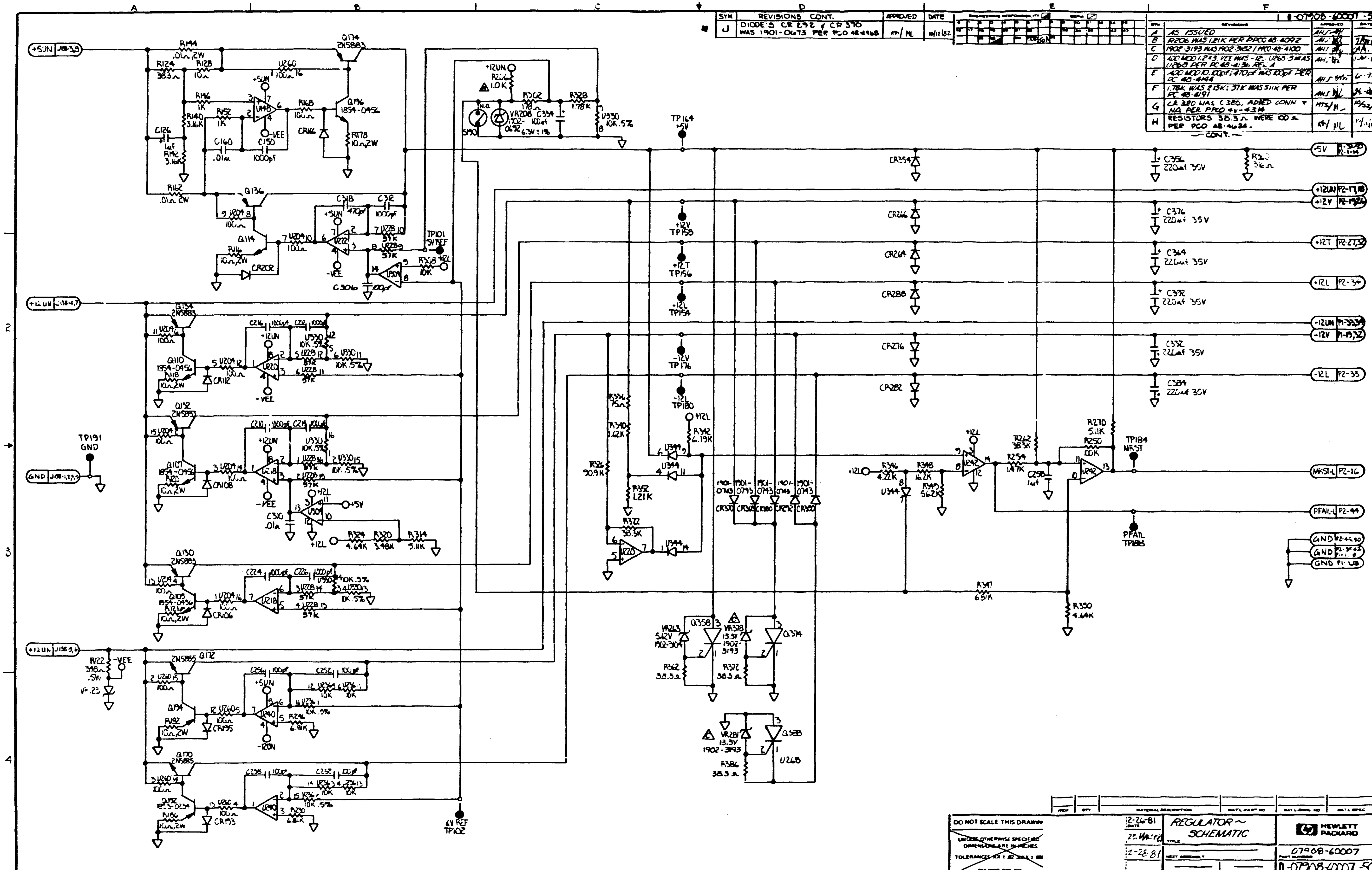
A) Replace R262 with a 110K (0757-0466). Replace R250 with a 162K (0757-0470).

4.5 On board revision B,E-2300; F-2300; 2301

A) Current Assembly

4.6 Test per

A-07908-60007-3


D-07908-60007-50
SYM | REVISIONS CONT. | APPROVED | DATE
J | DIODE'S CR 292 & CR 370 WAS 1901-0673 PER PCO 48-4968 | 10/11/82
A AS ISSUED
B R206 WAS 1.21K PER PPCO 48-4092
C 1902-3193 WAS 1902-3182 PRO 48-4100
D 400 MOD 1,2 & 3. VEE WAS -12. U268.5 WAS U268 PER PC 48-4136 REV. A
E 400 MOD 10. 100pf: 470pf WAS 100pf PER PC 48-4144
F 1.78K WAS 2.15K; 51K WAS 511K PER PC 48-4191
G CR 380 WAS C380, ADDED CONN + NA PER PPCO 48-4314
H RESISTORS 38.3Ω WERE 100Ω PER PCO 48-4624.
— CONT. —
+5UN
+12UN
GND
TP191 GND
+5V
+12UN
+12V
+12T
+12L
-12UN
-12V
-12L
MRST-L
PFAIL-L
6V REF TP102
5V REF TP101
TP164 +5V
+12V TP158
+12T TP156
+12L TP154
-12V TP176
-12L TP180
TP184 MRST
PFAIL TP188
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
12-26-81
REGULATOR ~ SCHEMATIC
HEWLETT PACKARD
07908-60007
D-07908-60007-50

P/N 07908-60006

SERVO PCA-A2

Series Code E-2338

ER48 D/H 50A

hp

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LTR	REVISIONS	DATE	INIT	MF
A	AS ISSUED PER PC048-4979	10-19-83	sr/CW	M
B	REVISED PER C0480296	09-28-83	db/ML	

A	ISSUED	sr/CW	10-07-82	MODEL 7908P/7908R	STK # 07908-60006
B	C0480296	db/ML	09-28-83	SERVO-IMS	
				BY	DATE 10-07-82
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 35
	REVISIONS			SUPERSEDES	DWG # A-07908-60006-7

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INTERNAL MAINTENANCE SPECIFIATION
7908 SERVO PCA

I. INTRODUCTION

- A. Purpose/Functions of Servo PCA
- B. Overview of how IMS is organized.

II. RELATED DOCUMENTS

III. FUNCTIONAL BLOCK DESCRIPTIONS

- A. Interface Block Diagram
- B. Signal List
- C. Servo Board Block Diagram
- D. Carrier Amplifier
- E. Peak Detection/Position Signal Generation
- F. Phase-locked Loop
- G. Position Comparators
- H. Track Following Loop
- I. Seek Electronics
- J. Power Amplifier
- K. Diagnostic Hardware
- L. Servo Calibration

IV. TECHNICAL DESCRIPTIONS

- A. Tri-bit Servo Recording Pattern
- B. Position Signal Generation
- C. Phase-locked Loop
- D. Servo Bit Pattern Detection
- E. Track Following Loop
- F. Track Seeking
- G. Power Amplifier
- H. Diagnostic Signal Injector

LIST OF FIGURES

I INTRODUCTION

I-A Purpose/Functions of Servo PCA

1. Obtain actuator position information by reading the tri-bit servo code from disc.
2. Derive clock from servo code for sector timing and write data clocking.
3. Generate index pulse, outer guardband, and inner guardband signals from servo code.
4. Provide electronics for track following loop.
5. Provide amplifier for actuator coil.
6. Provide uP interface for seeking.
7. Servo Specifications:

Average physical seek time:	36 msec.
Average latency:	8.3 msec.
Single track seek time:	5 msec.
379 track seek:	65 msec.
Seek soft error rate:	1 in 10^6

I-B Overview of how IMS is organized.

Section 3 presents a functional block diagram of the servo board and explains how it interfaces with the rest of the product. Each section in the block is then described in a general way to provide an understanding of how the board functions.

Section 4 provides more in-depth technical and design details on how the hardware functions.

II RELATED DOCUMENTS

A. ERS
B. Test Procedures
C. Diagnostics IMS
D. Seek IMS
E. Servo Adaptation IMS
F. Lab Notebooks
G. DMD Journal Articles

III FUNCTIONAL BLOCK DESCRIPTIONS

III-A Interface Block Diagram

Figure 1 illustrates how the servo PCA physically interacts with the power supply (regulator PCA), read/write board, microprocessor board, and the IMI disc mechanism.

III-B Signal List

INPUTS TO BOARD

uP:
SAL: Board Enable A
SBL: Board Enable B
RDL: Read Enable
WRL: Write Enable
MRSTL: Master Reset

DATA BUS: 2 input latches as follows
BOARD ENABLE A WITH WRL
2's complement 8 bits to DAC for current command
BOARD ENABLE B WITH WRL
D0: CVNL--Cylinder Even (odd or even track follow)
D1: PMDH--Position Mode (track follow enable)
D2: SKH---Seek High (enable current command)
D3: YFB---Yellow Function Button (secondary latch clock)
D4: TEH---Test Enable (enable signal injector)
D5: TFOH--Track Follow Offset (desensitize off-track comparison)
D6: unused
D7: RVDH--Reverse Direction

MECH:
SS1, SS2: Differential servo signals from head amplifier

POWER SUPPLY:
+12L: Low power--150ma
-12L: Low power--180ma
+12V: Servo actuator power--2 Amps peak
-12V: Servo actuator power--2 Amps peak
+5V : Logic power--700ma
DGND: Digital Ground
AGND: Servo actuator ground
LGND: Analog low power ground

OUTPUTS FROM BOARD

uP:
SERVO STATUS LINES
RB0: CYL---Cylinder addr LSB (CVNL fed back)
RB1: IDXL--Index pulse (3 uSEC)
RB2: ONH---On Track (+/-1V window)
RB3: TCH---Track Cross Pulse (pulse at zero crossing)
RB4: DIFH--Differentiator phase
RB5: IGBL--Inner Guard Band
RB6: OFH---Off Track (+/-2.5V window)
RB7: OGBL--Outer Guard Band

TKX: Track Cross pulse to CTC chip (same as TCH)

DATA BUS

BOARD ENABLE B WITH RDL

D0: PLL--Phase Lock (inverse of PLEL to F/latch)
D1: LMH--Linear Motor (>1 volt on motor coil)
D2: PLEH--Phase Lock Error (illegal servo pattern)

R/W:
P2L: Servo clock (648 KHZ)
P8L: Servo clock (2.59 MHZ)
PMDL: Position Mode
PLEL: Phase Lock Error to Fault Latch
ONH: On Track (also to Fault Latch)

MECH:
LMA, LMB: Linear Motor Drive lines
-8.2R: Servo head amplifier supply
GND: Servo head amplifier ground
SP, SM: Carriage lock solenoid power

III-C Servo Board Block Diagram

Figure 2 presents the functional block diagram of the servo board. The uP controller communicates to the servo PCA by sending comands across the data bus while activating the proper select lines (SAL or SBL) with WRL asserted, by reading the data bus with select line and RDL, or by reading the servo status word. Functional descriptions are included in the following paragraphs.

III-D Carrier Amplifier

The carrier amplifier's purposes are:

1. Amplify differential servo signals coming from the servo head preamplifier
2. Provide low pass filtering
3. Provide Automatic Gain Control with the amplification
4. Convert amplified differential signals to single ended signal for use by the peak detectors

The servo signals contain a tri-bit servo pattern (see Section IV for explanation) with a fundamental frequency of 324 KHZ.
The carrier amp output signal drives the peak detectors and also creates a sync pulse for the phase-locked loop.

III-E Peak Detection/Position Signal Generation

The two positive peaks of each cell of the carrier amp tri-bit signal are detected and held by active peak detectors. The voltage level of the two peaks is summed and forced to be a constant level via AGC feedback to the carrier amplifier. The difference of the two peaks is used to generate a signal proportional to servo head distance from track center (Position Signal or Position Error Signal).

III-F Phase-locked Loop

The negative swing of the CA output creates a sync pulse every 3 microseconds (324 KHZ). The servo phase-locked looped locks onto this sync pulse and multiplies its frequency by 16. The 8X frequency (P8L signal) is sent to the R/W board for use in in write data clock generation. The 2X frequency (P2L signal) is also sent to the R/W board for byte counting and sector timing. The 1X frequency (PCK) is used by the servo peak detectors to determine proper peak detection windows.

Some unique patterns of missing pulses in the servo signals are detected by the servo board to produce a once-around index pulse (for use in sector counting) and both inner- and outer-guardband detection. There are 30 outer-guardband tracks outside track 0 (the first valid data track) and up to 17 inner-guardband tracks inside track 389.

III-G Position Comparators

The position signal is used to create an "on track" indication (ONH), an "off track" indication (OFH), and a track cross pulse (TCH and TKX). The "on track" indicator is a narrow window around track center which remains active when the servo head is positioned within 12% of the track center. The "off track" indicator is used by the seek routine to indicate 30% off track. A track cross pulse is created each time the position signal crosses through zero volts (track center).
These comparator levels, or "windows", can be widened to twice their normal size by activating the TFOH command bit. This permits track following with offset to about 24% off track before triggering ONH low.

III-H Track Following Loop

For track following the position signal is filtered and passed on to the Linear Motor Current amplifier when the PMDH (Position Mode High) command bit is enabled. The two integrations (acceleration to position) through the Linear Motor Coil require lead compensation in the tracking loop filter for stability. The tracking loop will keep the position signal around zero volts when following a track center successfully.

Track following with offset is possible by enabling both PMDH and SKH (track follow and seek). The offset magnitude is then controlled by the DAC voltage injected into the loop.

III-I Seek Electronics

For seeking, the actuator is accelerated (or decelerated) across the disc on command of the uP controller. The controller sends an actuator coil current command through an 8-bit Digital/Analog converter (DAC) which is gated through to the Linear Motor Current amplifier when the seek bit is enabled. The current command direction is determined by the RVDH command bit. Current direction can also be manipulated by the 2's complement command word to the DAC. This 2's complement capability also facilitates current command offsets during track following and seeking.

While the servo head moves across the disc, the uP receives track crossing pulses and various level comparator outputs from the position signal. A desired actuator velocity profile as a function of distance to target track is resident in the uP. The uP counts track crossing pulses to determine distance-to-go information and measures the time between track crossing pulses to determine velocity information. The software seek algorithm then determines the actuator current command to bring the actuator velocity in line with the desired velocity profile.

III-J Linear Motor Current Amplifier

A voltage proportional to the Linear Motor Current command is gated to the power amplifier via the PMDH and/or SKH command bits. This power stage is a high gain amplifier with current sense feedback and high frequency roll off to prevent oscillations.

If the command bits PMDH and SKH are both low (by either controller command or master reset), the amplifier is disabled and a "retract" current of about 180ma pulls the actuator to the outside. This is to get the heads off of the data area and into the "park zone" or "landing area" on the outside diameter in case of power failure or other problems. On power down the 180ma retract current will be maintained for a few tenths of a second and a mechanical carriage lock will catch and hold the head assembly in the park zone.

III-K Diagnostic Hardware

The purpose of the diagnostic hardware is to isolate the cause of servo failures to either the IMI mechanism or the servo PCA. Considerable information can be obtained through "normal" hardware channels - Position Signal Comparators, DAC command, etc. The carrier amp, AGC, Peak Detectors, and phase-locked loop can be verified by injecting an on board generated test signal into the carrier amplifier (enabling TEH command bit will do this). The phase lock detect circuit and position signal comparators can then be checked for proper behavior to determine board integrity. A Linear Motor Coil voltage sensor can also report to the processor whether voltage is being applied to the coil.

III-L Servo Calibration

Three important measurements of drive servo parameters are made when power is applied to the unit. These measurements are:

1. DC actuator force (such as gravity).

2. Effective linear motor force constant.

3. Track center spacing.

These parameters directly affect track follow and seek performance. Instead of requiring manual offset measurements and adjustments the uP measures and nulls these effects. The DC force is nulled by an offset to the current command during both seeks and track following. The motor force constant is offset by adjusting the DAC gain via hardware on the servo board. The track center spacing can also be adjusted with position signal offsetting via board hardware.

IV. TECHNICAL DESCRIPTIONS

This section will provide technical and design details not presented in Section III.

IV-A Tri-bit Servo Recording Pattern

The underside of the lowest disc platter contains a dedicated servo surface for "continuous" servo feedback. Figure 3 illustrates how IMI encodes a tri-bit servo pattern onto the servo surface. The sync pulse magnitude will be constant since it is coincident on both "A" and "B" servo tracks. The sync pulse is used to set up timing windows to sample (peak detect) the A and B field magnitudes. A+B is forced to be a constant via the AGC circuit, A-B (or B-A, depending on even or odd cylinder) is used to produce a signal proportional to head position. A typical signal level coming from the servo head preamplifier (differential SS1 and SS2 signals) might be 60mV 0-to-peak for the sync pulse. The signal levels on tracks near the outside diameters may be up to 100% greater than on tracks near the inside. Figure 4 shows the servo track format. There is no servo code written in the "park" zone. The inner- and outer-guardband areas have unique patterns encoded on the servo surface so that they can be detected (See Section IV-D).

IV-B Position Signal Generation

The differential servo signals from the disc (SS1 and SS2) are gated through the analog switch (U111) when TEH is low (see Figure 5). TEH high gates the diagnostic signal through (see section IV-H). U112 is an IF amplifier with a voltage sensitive gain control input on pin 5. The output filter network on U112 provides three low pass poles at about 2 MHz. Typical differential signal amplitude at the opposite ends of R205/R206 is 1 volt 0-to-peak for the sync pulse. The transistor array network (U311) provides dual- to singleended signal conversion, amplification (about 5), and proper placement of the output around 0 volts. This output is called the carrier amp, or CA signal.

Figure 6 gives a block diagram showing the peak detectors and position signal generators. The CA signal is presented to the diode array (U231) for peak detection. When enabled, Q134 and Q135 are active sources for driving C226 and C231 to the positive peak voltage. Q134/135 are enabled in turn by the Phase-locked Loop to coincide with the A and B servo fields (see Figure 7). Q228 and Q229 with their respective emitter resistors cause a constant current (138 ua.) to ramp down the peak capacitor voltage at a constant rate (63mV/usec). U252 pins 1 and 7 are the buffered A and B peak detector outputs from which the sum and differences are taken for AGC and Position circuits, respectively.

The purpose of the AGC circuit is to force a constant A+B magnitude (about 6V.). This is important because the resulting volts/inch at the position signal (typically 2520 V/in or 8.4 v/track at PES1) needs to be held fairly constant. Otherwise tracking loop gain and position signal comparisons would vary from drive to drive and from track to track within a drive. U112 provides a range of 60dB of power gain as pin 5 goes from +5 to +7 volts. It normally operates around 6 V. so a filtered +12 V. is summed with the U122 output, which then operates around ground potential. This summation/attenuation gives added resolution and noise immunity at U122. U122 is a dual op amp used only in the AGC because I have previously had crosstalk into the sensitive AGC circuit from a shared quad device.

When an even cylinder is selected the B-A signal generates a voltage proportional to position at U252 pin 8 (PES1). This stage provides high frequency roll-off with a single low pass filter at 5.6KHz. A second order Butterworth low pass filter at 10.7KHz and unity gain produces PES2 from PES1. PES2 also allows for voltage offsetting through signal OFS by controller command (see section IV-F). The OFS signal through R373 causes a slight attenuation in the Position signal magnitude (2.5%) from PES1 to PES2.

IV-C Phase-locked Loop

The CA signal is run through a -2.5 V. comparison (U541 pin 2) to create the logic signal SNCH. SNCH is used to drive the Phase-locked Loop and plays a vital role in the pattern detect circuits (see section IV-D). The LM339 comparator (U541) has a specified typical large signal response time of 300 nsec., but no maximum specification is given. In this application the optimum response time is about 190 nsec. or less. Slower response times result in peak detector windows being delayed so that the "A" sample period may overlap the beginning of the "B" peak. Certain manufacturers and certain date code parts are, in fact, too slow for this application (Motorola, Texas Instr. 8109 date code). A new HP part number will likely be set up with the response time specified to fit our application.

An additional input (U571 pin 3) is provided for in the SNCH side of the phase detector. This is for the pattern detect circuitry to inject a pulse in the event SNCH is missing (see section IV-D).

A recent change was made to the charge pump in the PLL to compensate for the phase error induced by U541 and other components in the circuit. This includes changing CR247 to a Schottky diode and lowering R159 from 5.11K to 4.64K. The effect of this change is to speed up the response of the amplifier Q157/158 to SNCH and, as a result lessen the phase error between SNCH and PCK when the loop is locked. This also increases the gain of SNCH through the amplifier which makes noise more likely to disturb the PLL, but is necessary to adequately decrease the phase error. Lowering the gain of PCK was considered as a method of reducing the phase error, but it did not have enough affect to cure the seek problems that were occuring.

The object of the phase detector (U472) is to give an appropriate output if the falling edges of the compared input signals do not line up. The phase detector is comprised of a dual flip-flop with the Q outputs ANDed and fed back to the CLEAR inputs. This provides both phase and frequency detection. Figure 8 shows phase detector operation for various sequences of inputs.

Q157/158 and its network provides an inverting amplifier with the loop filter. R245 is a pull-up resistor for the amplifier. The PLL bandwidth is about 3KHz. This small bandwidth will not let the loop respond quickly to input disturbances (particlularly missing/delayed SNCH pulses) and provides a "jitter-free" clock to the R/W board for write data clocking. Acquisition parameters are not critical since the servo code is continuous.

U371 is a dual VCO with one half used in the PLL and the other half (normally disabled to prevent crosstalk) used for the diagnostic signal injector. Pin 2 is the voltage control input and pin 3 the range control (set to 2.5V. in this configuration). Pins 16 and 9 are the digital supply and pins 15 and 8 the analog supply. I have separated these and used a 5-Volt regulator (Q141) for the analog supply to provide for isolation and cross-stalk immunity. C348 was chosen to get the proper frequency range. Typical frequency output for a 2.5V control input is 5.7MHz with a 2MHz/V response.

The VCO output goes to a divide-by-16 counter (U361) to give various frequency outputs. U432 driving the CLEAR input on the counter provides capability for breaking the loop during board test. The PLL output frequencies for a nominal 324 KHz SNCH input frequency are:

VCO output	5.18MHz
P2H	648KHz
P8H	2.59MHz
PCK	324KHz

As shown in Figure 8 whenever PCK lags SNCH (PLL too slow) U472 pin 6 will go low. This pulls current through the Q157/158 feedback and raises the collector voltage, thus raising the VCO control voltage and increasing the frequency. Conversely, when PCK leads SNCH (PLL too fast) U472 pin 9 goes high and pushes current through the feedback to lower the control voltage and frequency. At equilibrium (SNCH and PCK negative edges lined up) pins 6 and 9 will go active simultaneously causing the clear pulse to "erase" themselves very quickly. With pins 6 and 9 both inactive (as is normally the case when phase locked) the diodes CR246/247 isolate them from the amplifier network and the status quo is maintained.

Detection of proper phase locking is implemented with U552 pins 12 and 13 monitoring the length of the "too slow" and "too fast" pulses out of U472. During proper phase lock U552 pin 11 will have a low duty cycle and U492 pin 1 will be low.

The frequency detection capability of the U472 phase detector is not desirable after proper phase lock has been achieved-stray crosstalk/noise or servo defects could knock the loop out of lock. Therefore, the circuit around U462 pin 6 was included to disable the frequency detection capability while in phase lock. Signal P2L causes pin 6 to go low and if PLL is high (no phase lock) pin 6 will stay low. When pin 6 goes high the phase detector is cleared. During phase lock pin 6 goes high once every servo bit (see Figure 9).

IV-D Servo Bit Pattern Detection

Normally, the servo sync, A, and B pulses are encountered every 3usec. Special patterns are encoded on the servo code, however, in the form of specific patterns of missing pulses. These special patterns define the inner/outer-guardband regions (see Figure 4) and a once-around index pulse for rotational registration. The index pulse (IDXL) is sent to the R/W board for sector timing and is also checked by the controller for proper disc spin velocity.

For future reference, a servo bit cell is the 3usec window in which a sync, A, and B pulse is normally found. If these pulses are present the servo bit is defined to be a "1". If they are missing the bit is a "0". Actually, only the sync pulse is used for bit determination but a given servo track will always omit both the sync pulse and the A or B pulse within the "0" bit cell. The special patterns are defined by the following sequences of servo bits:

```
Index            ...1111111010110101111111111...
Outer-guardband  ...0111011101110111011101110111...
Inner-guardband  ...0111101101111011011110111011...
```

Eight bits are required to detect each of these patterns so U452 serves as a serial shift register for storing the eight bits. U551 is a 256X4 PROM which serves as the pattern detect logic (the 8 address bits are the inputs and the 4 output bits respond to the patterns). U561 is a clocked "deglitcher"/buffer to prevent the shifting address lines on U551 from causing glitches on the signal lines.

The circuitry around the 4-bit counter (U361 pins 8-11) serves two functions--to decode the servo bits and to compensate the phase detector for missing sync pulses. Figure 9 shows that, until a sync pulse is missing, the U361 counter will not count past 7. About 200 nsec. after the front edge of a missing sync pulse the count of 8 is reached and U571 pin 13 sends a pulse to satisfy the phase detector. When the count of 12 is reached this phase detector pulse is terminated and the counter clock is disabled until the next sync pulse clears the counter. The delayed "substitute" sync pulse will cause a minor disturbance to the PLL. This has caused write clock disturbances and write data errors in the past but the PLL bandwidth has since been lowered solve this problem.

U452 is a serial 8-bit shift register which clocks in the decoded servo bit when the PCKH signal goes high. When a sync pulse is missing (see Figure 9) the U361 count is 11 when U452 shifts in a "0" bit. With regular sync pulses the U361 count won't exceed 7 and a "1" bit will always be shifted in.

There is only one PROM address (01011010) which will detect the index pulse--thus it becomes a 3usec pulse output. OGB and IGB, on the other hand, are continuous patterns so all "rotated" representations of their addresses must be detected. Valid OGB patterns, for instance, are 01110111, 11101110, 11011101, and 10111011. There are eight valid representations/rotations of IGB.

Two things should be pointed out at this time. The first is that the OGB pattern is not truly continuous completely around the disc. There is a string of 8 "1's" injected into the pattern coinciding with where the data tracks have the index pulse. Thus the OGB signal will go inactive for 40usec (13 servo bit times) once each rotation. The other thing is that track -1 is designated as an outer-guardband track but the OGB detection will be unreliable near the track center. The reason is the servo track towards the inside of track -1 will not have the missing pulses while the servo track towards the outside will. The servo head will pick up "half" of the sync pulse and "0" detection may or may not occur. For the same reason IGB detection at track 390 will be unreliable.

IV-E Track Following Loop

Figure 10 shows the tracking loop block diagram for use in analysis and simulation. From this model the following loop parameters can be calculated:

Loop bandwidth 240 Hz.
Gain margin 15 DB
Phas margin 50 deg.
Gain at runout 16 DB (60 Hz.)

Stiffness, measured as actuator force per unit offtrack, is 1.6 pounds per track (0.5 lb./.001 in. offtrack).

Unlike the seek operation, track following is accomplished entirely with hardware on the servo board. The PMDH signal going high will enable track following.

Schematically, there are three filter blocks in the track following loop. The first is a single pole low pass (5.57 KHz.) at the formation of the PES1 signal. The next is a two pole low pass (10.7 KHz.) to create PES2. The compensating filter, or tracking loop filter (U292 pin 14), has the lead corner at 76 Hz. for loop stability. It also has two low pass poles at 1.34 KHz. The reason for each of the low pass filters is for noise suppression.

There are two reasons, and two methods, for injecting position signal or track following offsets. Any non-zero signal added to the position signal in the tracking loop will result in a proportional track following offset. The seek calibration routine measures track syncopation (uneven spacing of track centers) across the disc. Track syncopation is a term used to describe alternately narrow and wide track center spacings--for example, when tracks 1 and 2 are closer together than 2 and 3, 3 and 4 closer together than 4 and 5, etc. The seek algorithm requires even track spacings for accurate velocity measurements. The OFS signal is the offset injected into the position signal to compensate for apparent track syncopation during seeks. The magnitude of OFS is governed by the result of the seek calibration routine for each area of the disc and can vary the apparent track center by up to +/-2.5%.

The other method for producing a track following offset is by enabling the SKH bit and injecting an offset value through the DAC (U531). In fact, the SKH and RVDH bits are always enabled during track following to allow compensation for "DC" force offsets (due to gravity, flex circuit, etc.) on the actuator. The seek calibration routine measures force offsets and these are compensated for during both seeking and track following by sending a current through the ..C. Each incremental DAC value results in 49mV. at DRV and about 0.8% track following offset. It should be

It should be noted that the OFS induced offset is injected before the position comparators and does not affect the offtrack indicator. The offset injected through the DAC is after the position comparators and adds to any other effects at the offtrack indicators. Therefore, an offset value of 15 at the DAC input will result in an outright "not on track" fault during a write operation (1 volt at PES2). Lesser values will reduce margins proportionately.

Finally, the signal TFOH desensitizes the off track comparators by a factor of two. This is to provide more margin during reads (2 volts for not on track fault) where off tracks are not fatal (won't destroy data).

IV-F Track Seeking

As mentioned in section III-I, the seek from one track to another involves much interaction between the hardware and the seek algorithm resident in the controller. The controller accepts DIFH, OFH, ONH, and TKX signals from the servo board and makes decisions based on them. The servo board then receives control signals SKH, RVDH, PMDH, and CVNL, as well as DAC values. The secondary port is set up at the beginning of the seek to adjust the DAC gain and the syncopation offset.

The actuator is moved by sending current through a voice coil in the IMI mechanism. The nominal acceleration/current is about 420,000 tracks per sec.**2 per amp. The rise time for current in the coil is about 1 msec. Each incremental DAC value results in 49 mV. at DRV, or about 12.3 ma. steady state current in the coil. The maximum current possible is nominally 12V./8 Ohms, or 1.5A. (630,000 tracks per sec.**2).

Figure 11 shows what several signals and commands might look like for a 5-track seek. The initial forward current command begins to move the heads, as seen in the position signal. Forward is considered as the direction of increasing track numbers, or towards the inside of the disc. After traveling one full track the current is reversed and the heads begin to slow down. The time between the track center crossings from track 1 to track 2 is measured by the controller and a decision is made as to the magnitude of reverse current to apply next (track 2 to track 3). At two tracks out (track 3 in this case) no current is commanded so that an accurate measurement of velocity can be made. A stop pulse of variable duration is then applied to bring the velocity into the track following capture range (about 400 tracks per sec.). The "final curve" (between tracks 4 and 5) is detected by the DIFH circuit. It is simply a differentiated position signal to indicate the slope of PES1. When the slope changes sign at the target track then the track follow (PMDH) command is given and the hardware loop takes over.

The DAC (U531) pulls between 0 and 2 ma. through pin 4, depending on the 8 input bits. The resulting DACV voltage at U292 pin 1 is made bipolar by the 1 ma. current drawn through R248. By inverting the most significant bit (U531 pin 5) at the DAC input the 8-bit command takes on a 2's complement format.

As mentioned earlier (sections III-L and IV-E) there is a servo calibration, or adaptation, routine which is executed at each drive power-on or self-test which measures DC forces, track spacing, and motor constant. The algorithms for these are discussed in other documents. The hardware implementation for adjusting for track syncopation and motor constant is made through the secondary port (U521). Data is entered into this port via the DAC port by activating YFB control bit. The lower three bits control the OFS signal magnitude. A value of 4 in these three bits is the nominal setting and one increment in either direction results in about 87mV. offset at PES2.

The upper two bits in this 8-bit port (U521) are unused but the middle three bits adjust the DAC gain in accordance with the motor constant measurement. Again, a value of 4 is the nominal setting.

An increment in either direction changes the DAC reference current by 0.041ma., a change of about 2% in DAC gain since the nominal reference current is about 2ma. A value of 7 will increase DAC gain, and motor current applied, by 6%--a value of 0 will reduce motor currents in a "hot" drive by about 8%.

IV-G Linear Motor Current Amplifier

The linear motor current amp (signal DRV to LMB, LMA) has the function of converting voltage commands at DRV into current in the voice coil. The first op amp (U491 pin 8) takes the DRV input and compares it with the feedback voltage from the current sense resistor (R152). The result is that, steady state, each volt at DRV commands 0.25 A. in the coil.

The current amp block itself is a rather complex circuit with several feedback paths. The voltage gain inside the loop is quite high so care must be taken to avoid instabilities. The purpose of the feedback section R177 and C264 is to shunt higher frequencies and reduce their gain. The coil current cannot respond reasonably (1 msec. rise time) to frequencies greater than 100 KHz. R193 feeds back the coil voltage which must be overcome by the feed forward voltage/current command. C191 serves to shunt higher frequencies.

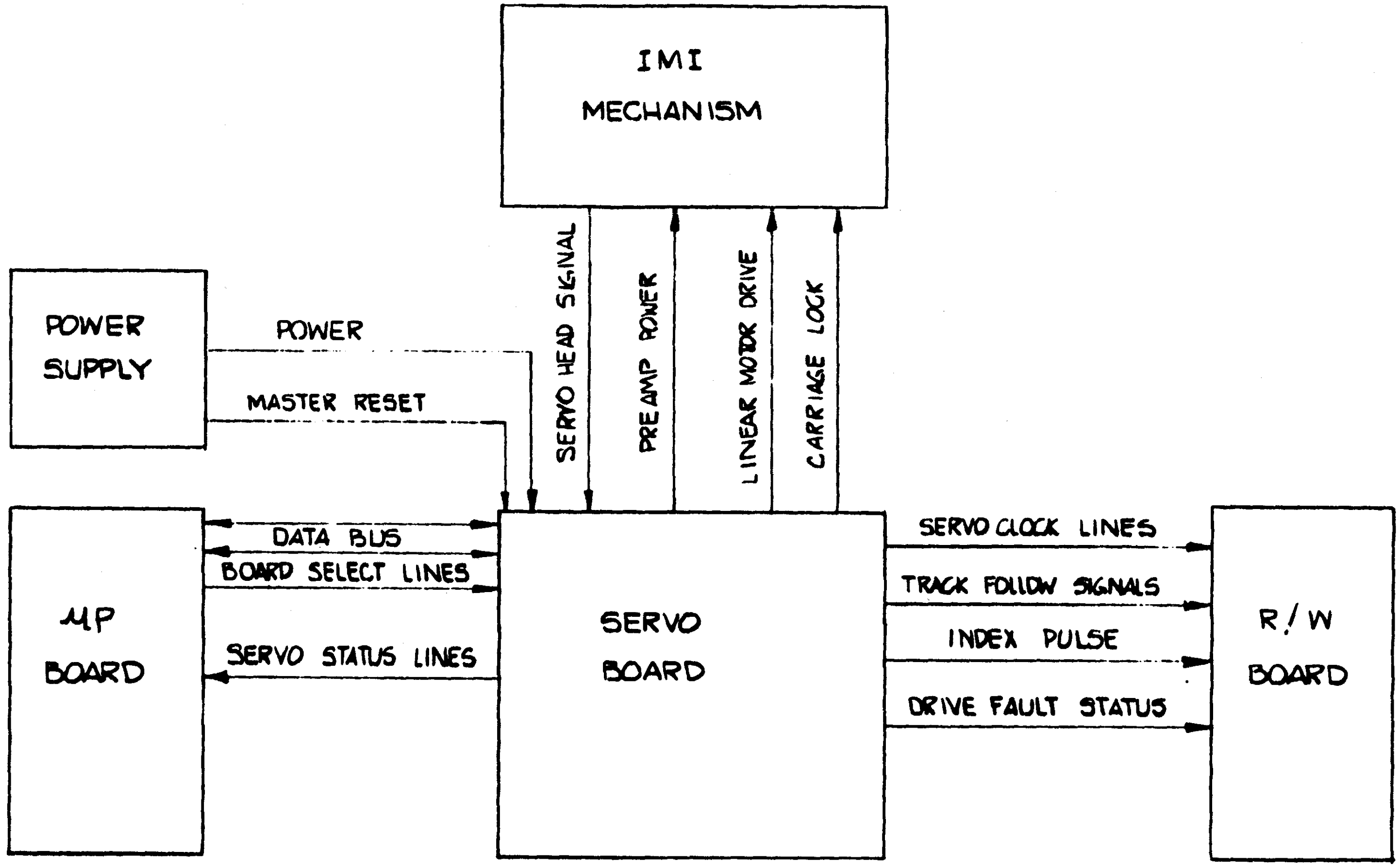
There is a problem involving switching times of the TO-66 transistors (Q183 and Q190)--they tend to turn on a few usec. faster than they turn off. When a current command is reversed, signal SD will slew at its maximum rate and attempt to turn one transistor off and the other on, in that order. The transistor switching time skews cause both transistors to conduct for 1 or 2 usec.--this results in large momentary currents from +12VP to -12VP and also causes crosstalk on the board. The severity of this problem was reduced by making R193 smaller (reducing internal voltage gain). This problem only occurs when maximum currents are commanded and achieved (Q183 or Q190 in saturation).

As part of the board self-test, there is a coil voltage sensing comparator (U492 pin 14) which gives feedback to the controller as to whether the coil voltage exceeds 1V. This helps isolate faults to board vs. IMI mechanism when the heads won't move.

The automatic retract current is presently set at about 180ma. The retract command (SDLL) is enabled whenever there is no track follow command (PMDH) or seek command (SKH), such as when MRSTL is active on a power-on or power-off. When retract is enabled then Q470 serves to disable the normal current amp driving path and Q471 then commands the 180ma. retract current. Coil voltage is monitored via R160/R249 to maintain the proper retract current. VR481 and VR462 serve to protect the transistors from excessive emitter-base voltages. Upon retract during power down Q111 will shut off current to the carriage locking solenoid and allow the retracted carriage to lock in the park zone.

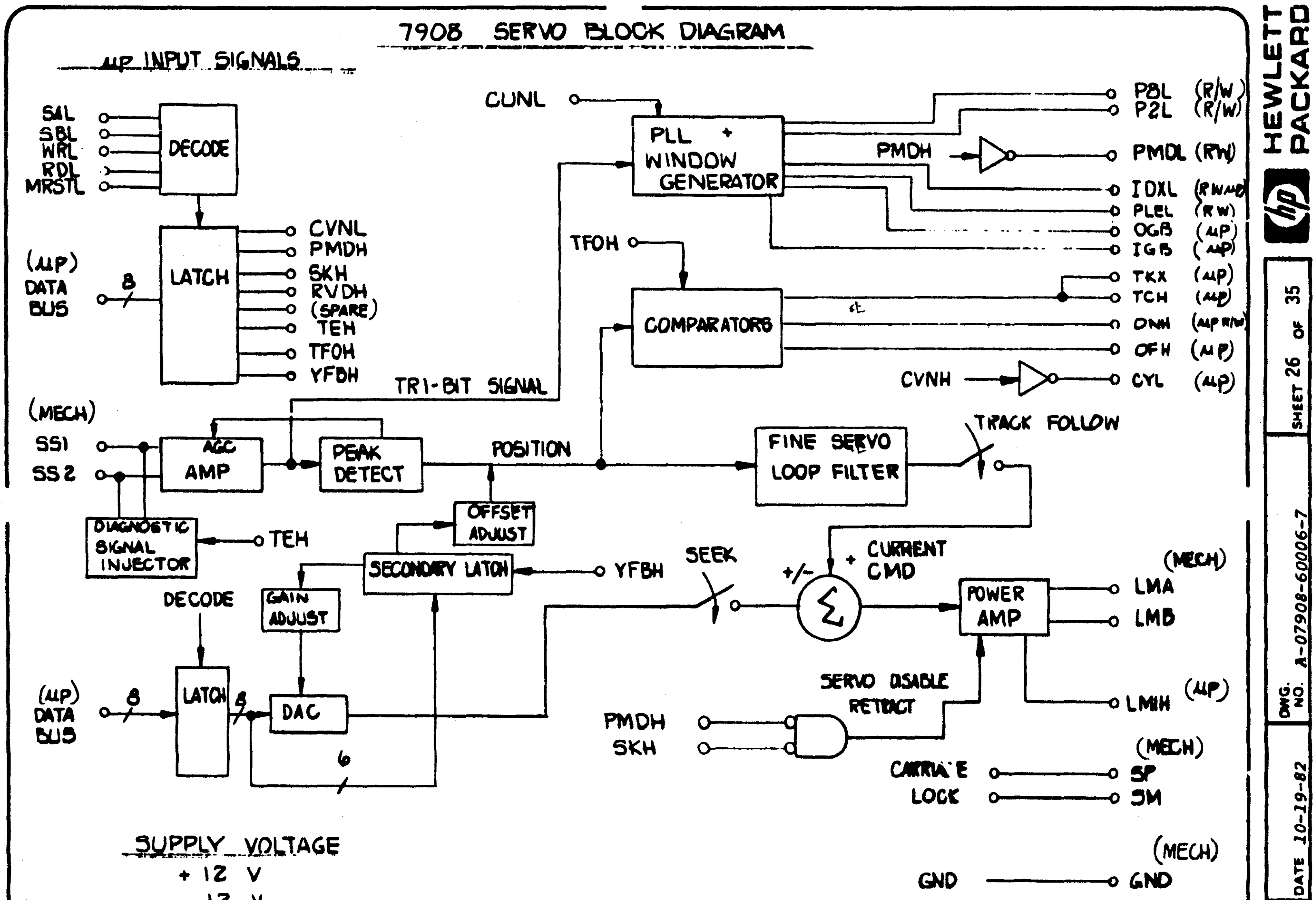
IV-H Diagnostic Signal Injector

The diagnostic signal injector circuitry synthesizes a substitute for the tri-bit signal from the disc servo code. To enable this diagnostic circuitry, the command bit TEH is activated. This enables the other half of the dual VCO (U371) to run at a frequency controlled by the DAC port value. A sawtooth wave is generated by an integrator (C169) following a 25% duty cyle TTL waveform (U471). This sawtooth wave, nominally 300 KHz. and 150mV. peak-peak, is then injected into the servo signal path with analog switch U111. Sync pulse detection and phase locking occur as normal but the asymmetry in the triangle wave will result in a non-zero position signal. The position signal magnitude should exceed 1V. and cause ONH to go low. In addition, proper phase lock is checked (PLE-L signal) and the CVNL signal is manipulated to create track crossings (TKX signal) to verify proper servo board operation independent of the IMI mechanism.



7908 SERVO BOARD INTERFACE BLOCK DIAGRAM

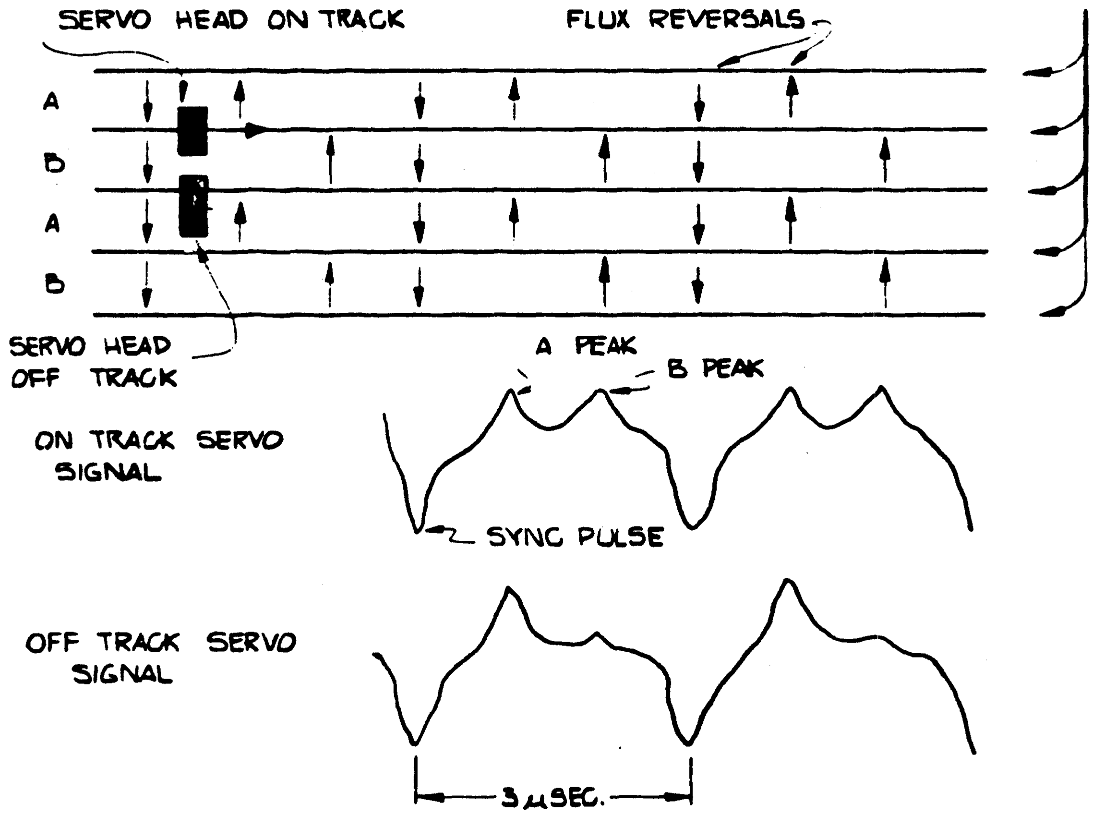
FIGURE 1



SERVO BLOCK DIAGRAM

FIGURE 2

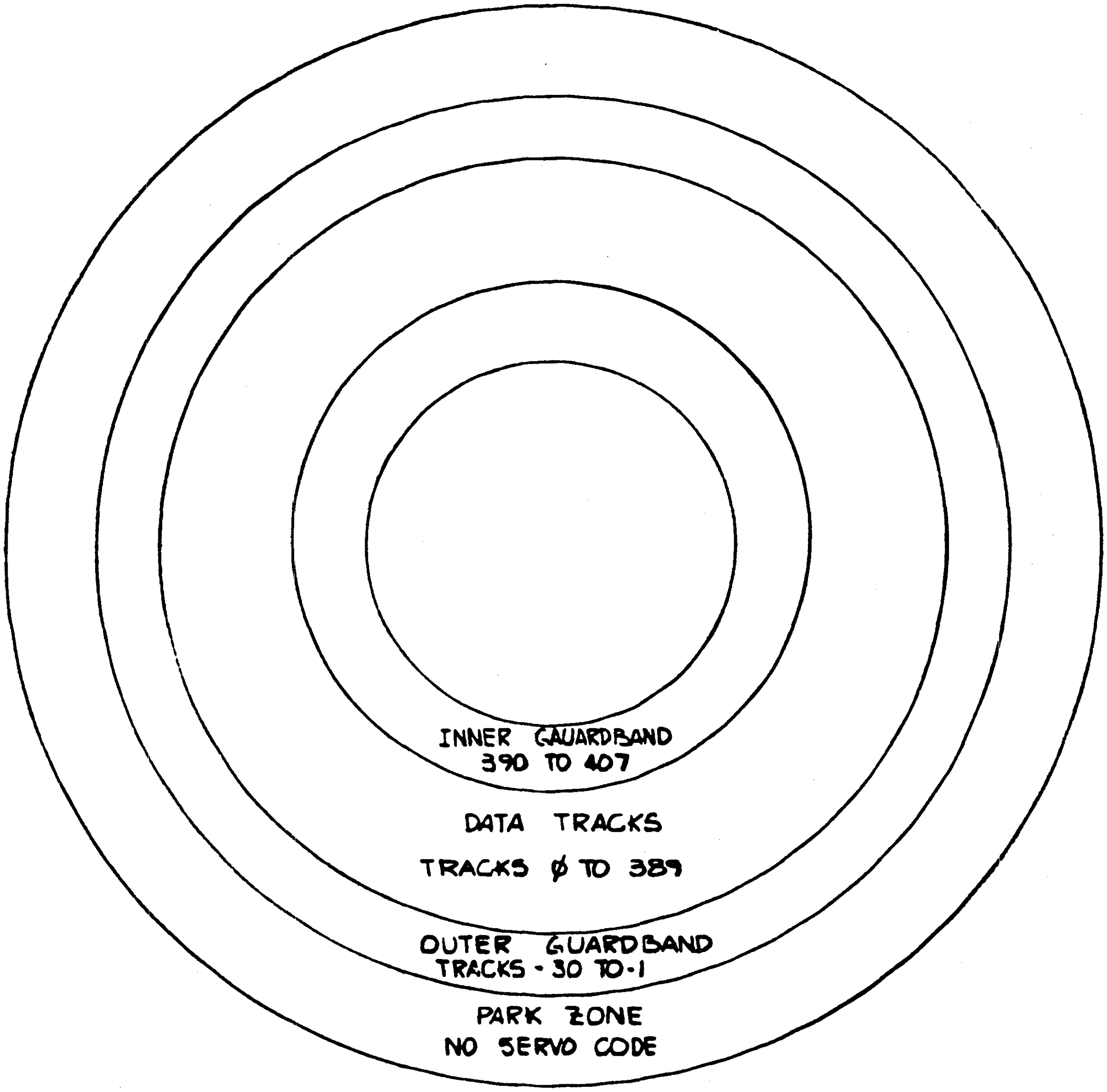
7908 TRI-BIT SERVO CODE



THE SYNC PULSE IS USED TO SET UP TIMING WINDOWS TO SAMPLE (PEAK DETECT) THE A AND B FIELD MAGNITUDES. A AND B IS FORCED TO BE A CONSTANT VIA THE AGC CIRCUIT, A-B (OR B-A, DEPENDING ON THE CYLINDER) IS USED TO PRODUCE A SIGNAL PROPORTIONAL TO HEAD POSITION.

TRI-BIT SERVO CODE

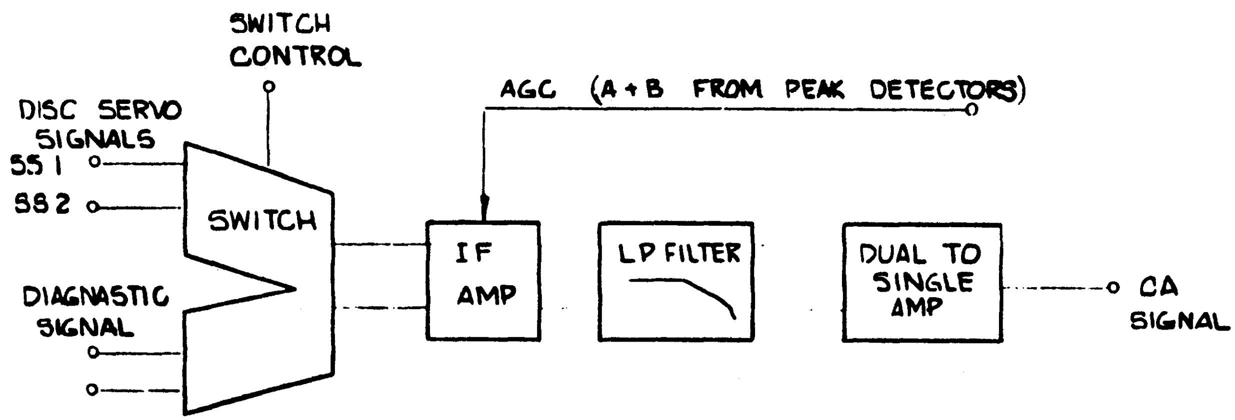
FIGURE 3



300 TRACKS PER INCH

* NOT DRAWN TO SCALE

FIGURE 4

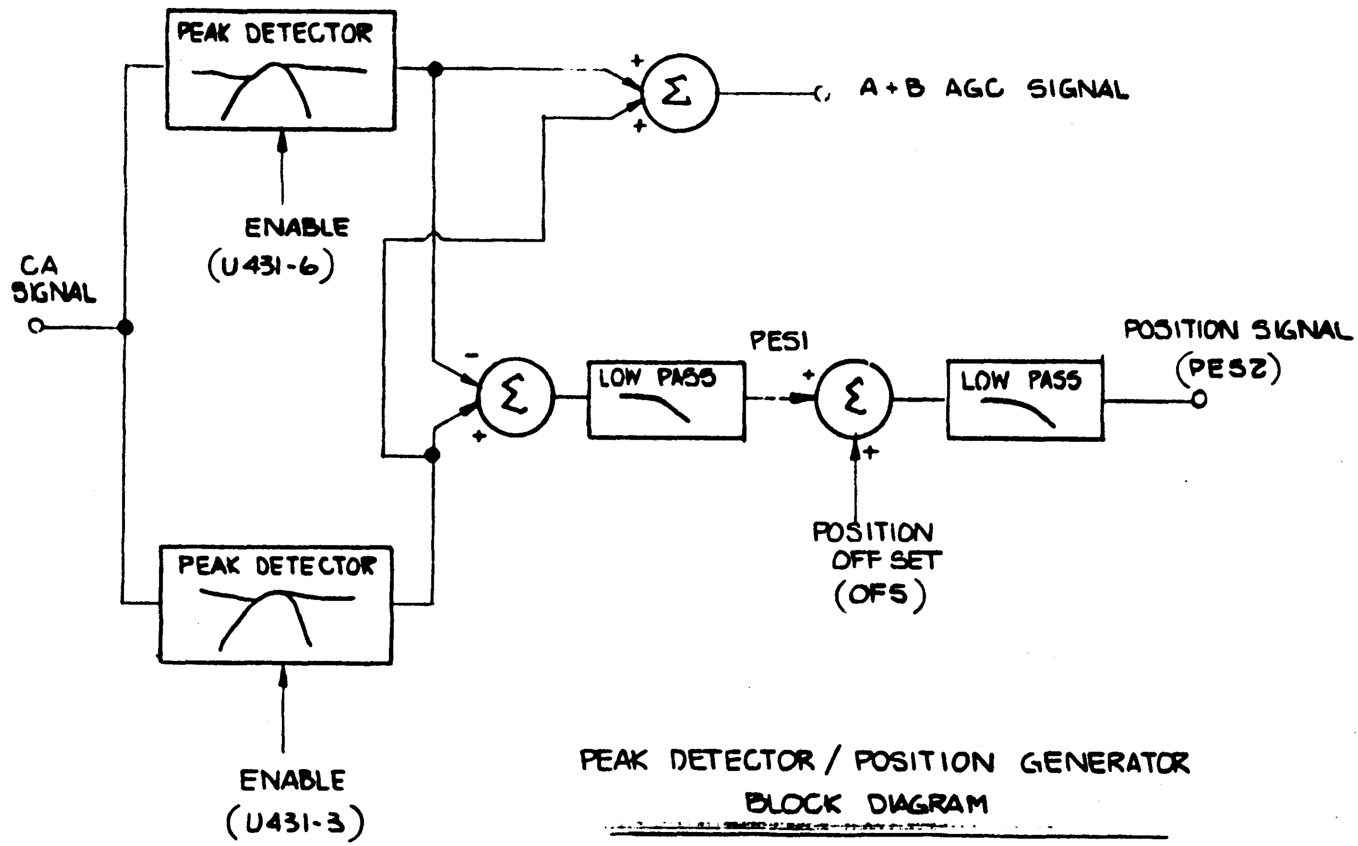


CARRIER AMP BLOCK DIAGRAM

FIGURE 5

REV. NO. A | DATE 10-19-82 | DWG. NO. A-07908-60006-7 | SHEET 29 OF 35

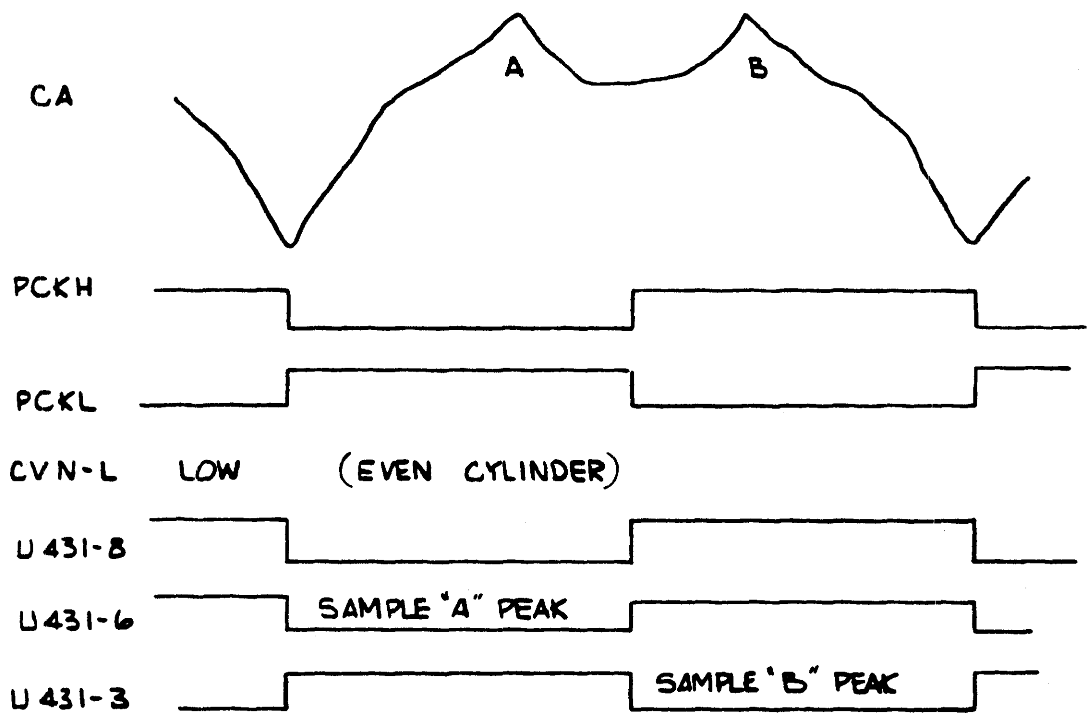
HEWLETT PACKARD



PEAK DETECTOR / POSITION GENERATOR
BLOCK DIAGRAM

FIGURE 6

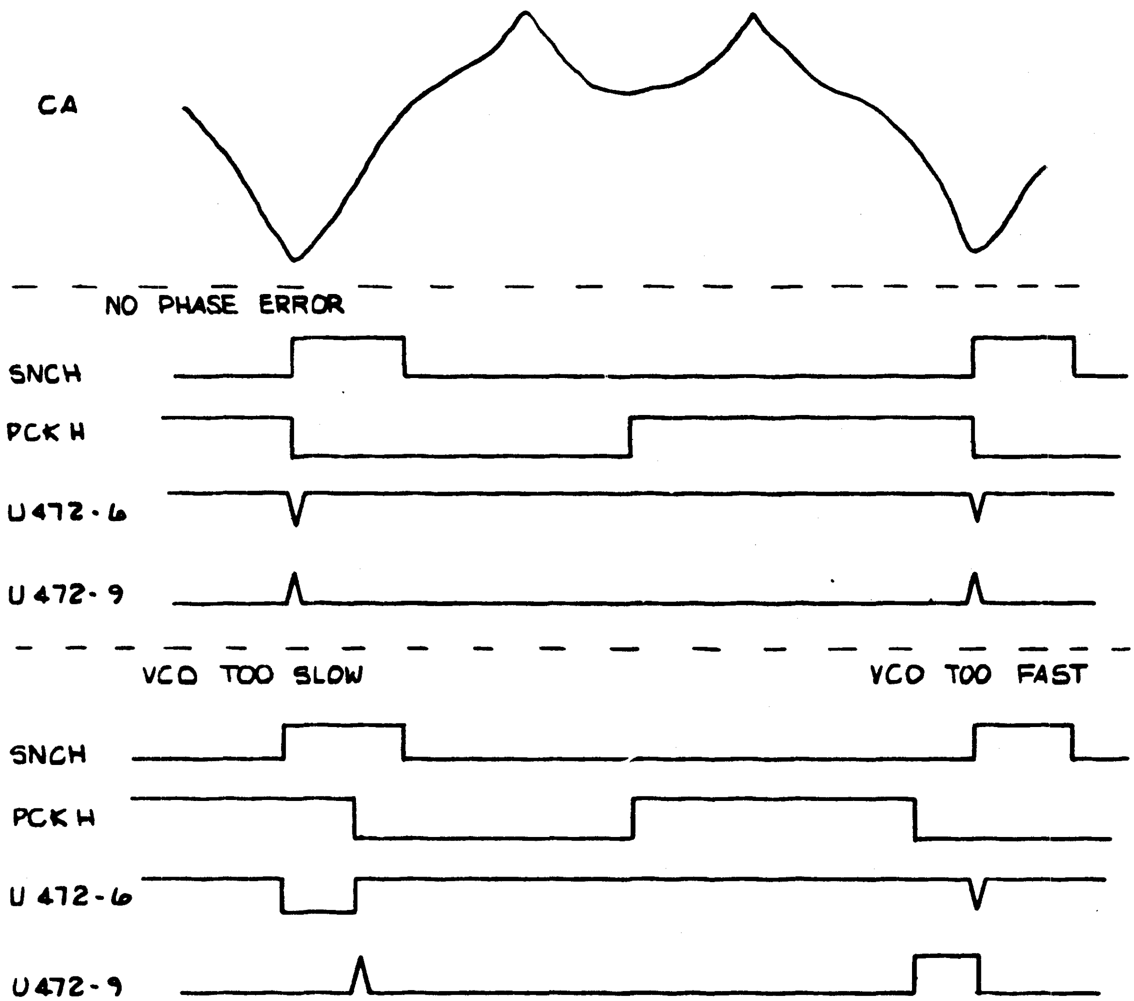
REV. NO. A
DATE 10-19-82
DWG. NO. A-07908-60006-7
SHEET 30 OF 35
HEWLETT PACKARD



B-A CREATES POSITION SIGNAL FOR EVEN CYLINDER
U431 OUTPUTS ALL BECOME INVERTED FOR CVN-L
HIGH TO GIVE A-B ON AN ODD CYLINDER.

PEAK DETECTOR TIMING

FIGURE 7

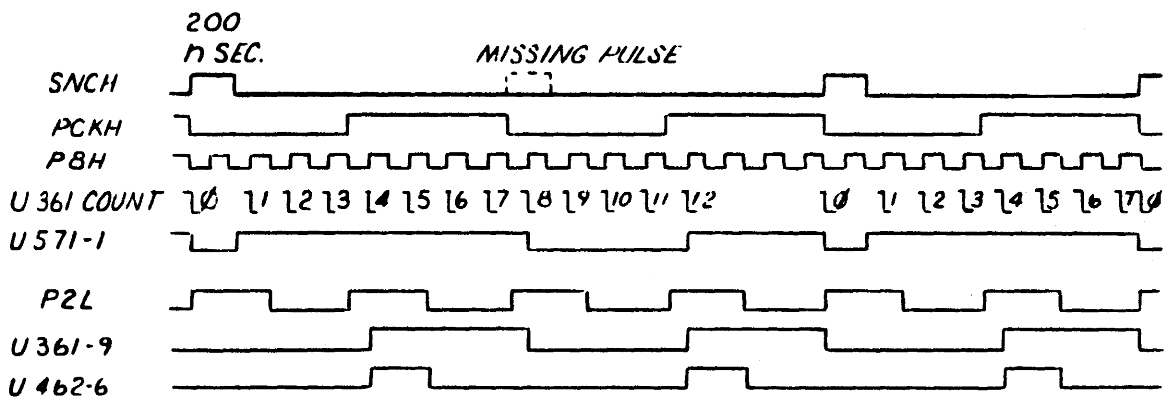


PLL PHASE DETECTION

FIGURE 8

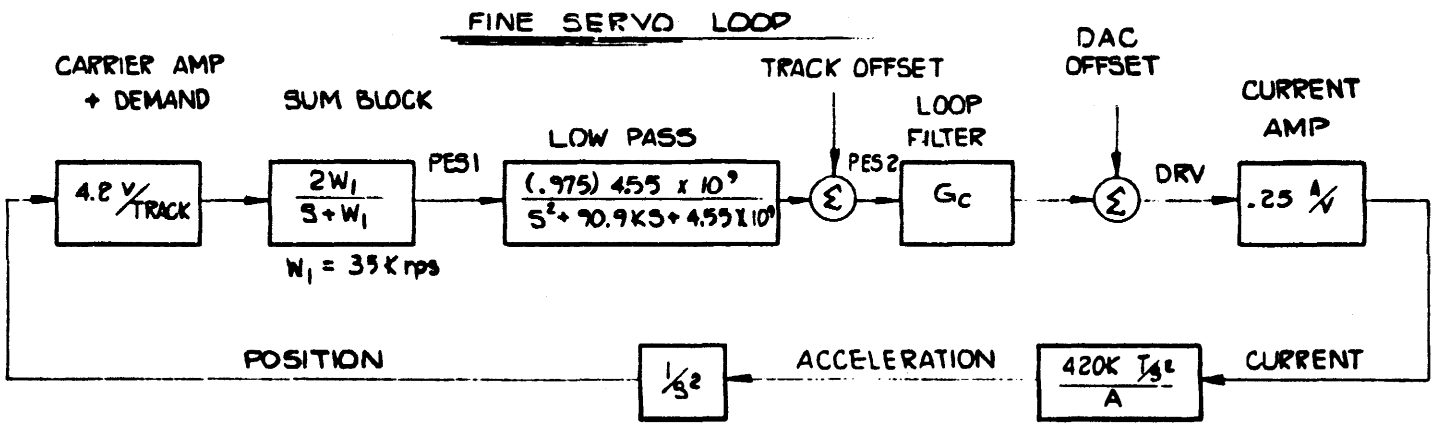
REV. NO. A | DATE 10-19-82 | DWG. NO. A-07908-60006-7 | SHEET 33 OF 35

HEWLETT PACKARD



SYNC BIT TIMING

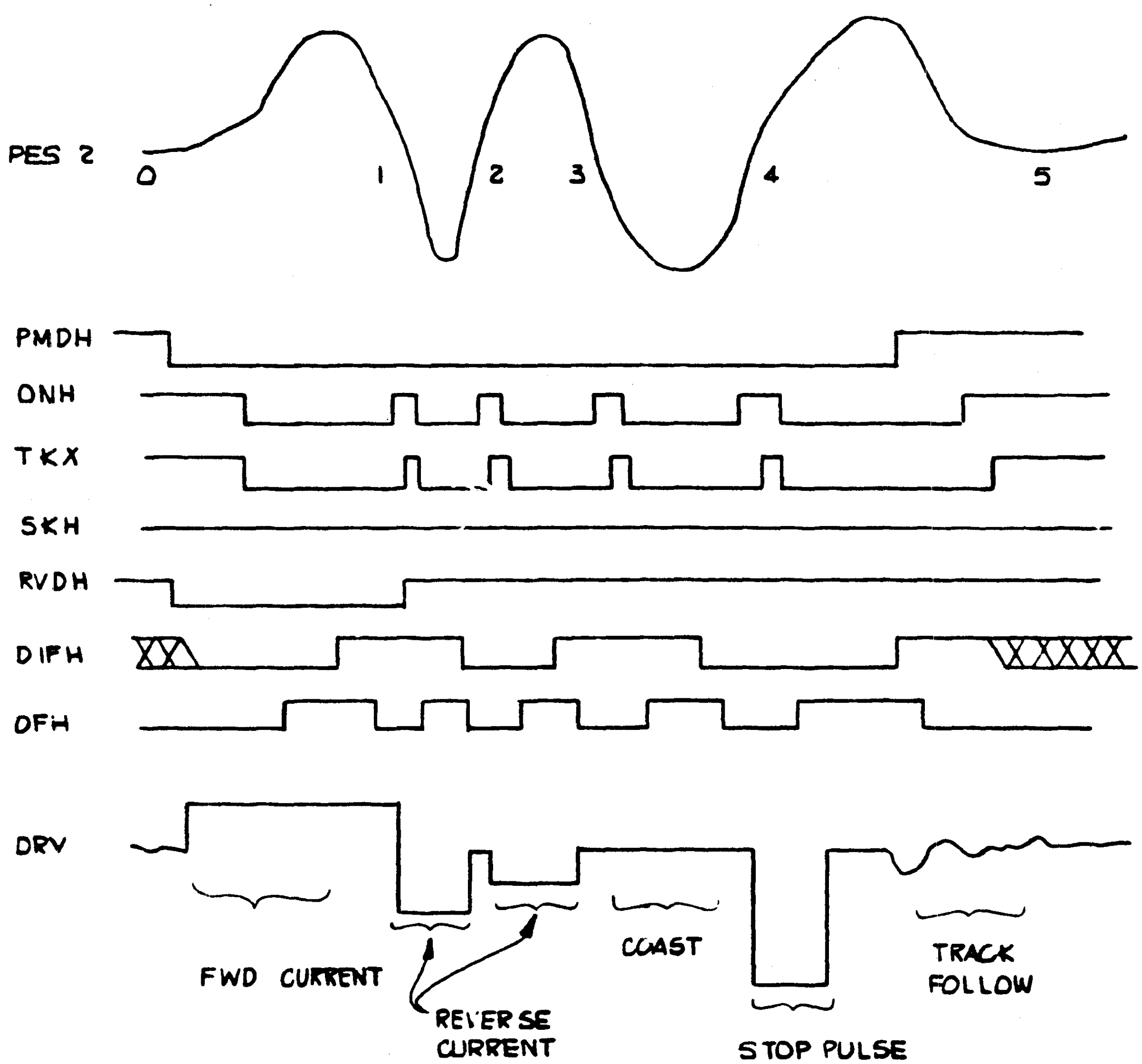
Figure 9



$$G_c = \frac{1.688 \times 10^{-3} S + .8045}{14.09 \times 10^{-9} S^2 + 214.1 \times 10^{-6} S + 1}$$

TRACKING LOOP BLOCK DIAGRAM

FIGURE 10



5 - TRACK SEEK

FIGURE 11

MATERIAL LIST FOR PC-BOARD COMPOSED OF MU'TIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60006
07908-66006
07908-68006

DATE CODE : E2338

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C104	0160-5332	CAP.1UF 20% 50V
C105	0160-5436	CAP- FXD 120 PF
C108	0160-5298	CAP .01UF 20%
C109	0160-5332	CAP.1UF 20% 50V
C110	0160-5332	CAP.1UF 20% 50V
C117	0160-5332	CAP 1UF 20% 50V
C123	0160-5354	CAP 2200PF 5%
C124	0160-5298	CAP .01UF 20%
C142	0160-5298	CAP .01UF 20%
C143	0160-5298	CAP .01UF 20%
C144	0160-5313	CAP 1000PF 5%
C145	0160-5354	CAP 2200PF 5%
C147	0160-5298	CAP .01UF 20%
C151	0160-5354	CAP 2200PF 5%
C161	0160-5298	CAP .01UF 20%
C168	0160-5332	CAP.1UF 20% 50V
C169	0160-5372	CAP .01UF 10%
C170	0160-5320	CAP 6800PF5%100V
C171	0160-5375	CAP .10UF 10%
C191	0160-5313	CAP 1000PF 5%
C196	0160-5364	CAP-FIXED .27UF
C204	0160-5326	CAP 27PF 5% 200V
C207	0160-5332	CAP.1UF 20% 50V
C208	0160-5332	CAP.1UF 20% 50V
C212	0160-5298	CAP .01UF 20%
C222	0160-5438	CAP -FXD 1UF
C226	0160-5354	CAP 2200PF 5%
C231	0160-5354	CAP 2200PF 5%
C235	0160-5354	CAP 2200PF 5%
C239	0160-5298	CAP .01UF 20%
C240	0160-5298	CAP .01UF 20%
C263	0160-5332	CAP.1UF 20% 50V
C264	0160-5319	CAP 5600PF5%100V
C274	0160-5371	CAP 1000PF 20%
C280	0160-5298	CAP .01UF 20%
C283	0160-5318	CAP 240PF 5%200V
C287	0160-5298	CAP .01UF 20%
C293	0160-5298	CAP .01UF 20%
C302	0160-5332	CAP.1UF 20% 50V
C303	0160-5298	CAP .01UF 20%
C304	0160-5332	CAP.1UF 20% 50V
C305	0160-5371	CAP 1000PF 20%
C321	0160-5298	CAP .01UF 20%
C328	0160-5298	CAP .01UF 20%
C329	0160-5298	CAP .01UF 20%
C331	0160-5298	CAP .01UF 20%
C332	0160-5298	CAP .01UF 20%

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60006
07908-66006
07908-68006

DATE CODE : E2338

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C337	0160-5298	CAP .01UF 20%
C338	0160-5298	CAP .01UF 20%
C342	0160-5298	CAP .01UF 20%
C343	0160-5298	CAP .01UF 20%
C347	0160-5298	CAP .01UF 20%
C348	0160-5329	CAP 47PF 5%
C353	0160-5298	CAP .01UF 20%
C354	0160-5298	CAP .01UF 20%
C355	0160-5310	CAP 220PF 5%
C367	0160-5298	CAP .01UF 20%
C378	0160-5371	CAP 1000PF 20%
C406	0160-5307	CAP 68PF 5%
C414	0160-5298	CAP .01UF 20%
C420	0160-5332	CAP.1UF 20% 50V
C421	0160-5298	CAP .01UF 20%
C422	0160-5298	CAP .01UF 20%
C423	0160-5298	CAP .01UF 20%
C424	0160-5307	CAP 68PF 5%
C425	0160-5298	CAP .01UF 20%
C432	0160-5298	CAP .01UF 20%
C433	0160-5298	CAP .01UF 20%
C434	0160-5298	CAP .01UF 20%
C435	0160-5298	CAP .01UF 20%
C436	0160-5298	CAP .01UF 20%
C440	0160-5298	CAP .01UF 20%
C441	0160-5298	CAP .01UF 20%
C451	0160-5298	CAP .01UF 20%
C452	0160-5298	CAP .01UF 20%
C461	0160-5298	CAP .01UF 20%
C473	0160-5354	CAP 2200PF 5%
C482	0160-5332	CAP.1UF 20% 50V
C501	0160-5298	CAP .01UF 20%
C502	0160-5298	CAP .01UF 20%
C503	0160-5298	CAP .01UF 20%
C504	0160-5298	CAP .01UF 20%
C505	0160-5298	CAP .01UF 20%
C506	0160-5298	CAP .01UF 20%
C507	0160-5298	CAP .01UF 20%
C511	0160-5298	CAP .01UF 20%
C512	0180-0374	CAP 10UF 10%
C516	0160-5298	CAP .01UF 20%
C517	0160-5298	CAP .01UF 20%
C518	0180-0374	CAP 10UF 10%
C519	0160-5298	CAP .01UF 20%
C525	0180-0374	CAP 10UF 10%
C526	0180-0374	CAP 10UF 10%
C527	0180-0374	CAP 10UF 10%

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60006
07908-66006
07908-68006

DATE CODE : E2338

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C534	0160-5332	CAP.1UF 20% 50V
C545	0160-5298	CAP .01UF 20%
C546	0160-5298	CAP .01UF 20%
C547	0160-5298	CAP .01UF 20%
C555	0160-5320	CAP 6800PF5%100V
C562	0160-5332	CAP.1UF 20% 50V
C564	0180-0100	CAP 4.7UF 10%
C565	0160-5298	CAP .01UF 20%
C566	0180-0291	CAP 1UF 10%
CR112	1901-0743	DIO-1N4004
CR172	1901-0743	DIO-1N4004
CR174	1901-0743	DIO-1N4004
CR246	1901-0040	DIODE-SWITCHING
CR247	1901-0518	DIODE-SCHOTTKY
CR253	1901-0040	DIODE-SWITCHING
CR258	1901-0040	DIODE-SWITCHING
CR269	1901-0040	DIODE-SWITCHING
CR273	1901-0040	DIODE-SWITCHING
CR427	1901-0040	DIODE-SWITCHING
CR463	1901-0040	DIODE-SWITCHING
CR480	1901-0040	DIODE-SWITCHING
CR485	1901-0040	DIODE-SWITCHING
CR486	1901-0040	DIODE-SWITCHING
CR530	1901-0040	DIODE-SWITCHING
L201	9100-1625	COIL 33UH 5%
L203	9100-1625	COIL 33UH 5%
MP1	07908-80006	BD-ETCHED
MP2	7120-6830	LABEL-INFO
MP3	2360-0464	MS#6-32X.37
MP4	2420-0003	NUT 6-32 .250AF
MP5	2190-0414	WSHR-LK EXT T
MP7	1480-0116	PIN GRV .062X.25
MP8	0403-0452	EXTR-PC BD #2
Q111	1854-0477	XSTR 2N2222ATO18
Q134	1853-0281	XSTR PNP 2N2907A
Q135	1853-0281	XSTR PNP 2N2907A
Q157	1854-0071	XSTR NPN SI PL5
Q158	1854-0071	XSTR NPN SI PL5
Q183	1854-0072	XSTR 2N3054 TO66
Q184	1853-0281	XSTR PNP 2N2907A
Q185	1854-0477	XSTR 2N2222ATO18
Q190	1853-0413	XSTR PNP 2N6049
Q228	1854-0477	XSTR 2N2222ATO18
Q229	1854-0477	XSTR 2N2222ATO18
Q319	1853-0281	XSTR PNP 2N2907A
Q320	1853-0281	XSTR PNP 2N2907A
Q464	1854-0477	XSTR 2N2222ATO18

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60006
07908-66006
07908-68006

DATE CODE : E2338

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
Q471	1854-0477	XSTR 2N2222AT018
R102	0698-3437	RES 133 1%.125
R103	0698-3437	RES 133 1%.125
R106	0757-0444	RES 12.1K 1%.125
R107	0698-3429	RES 19.6 1%.125
R115	0757-0280	RES 1K 1%.125
R116	0757-0438	RES 5.11K 1%.125
R118	0757-0346	RES 10 1%.125
R119	0757-0438	RES 5.11K 1%.125
R125	0698-3442	RES 237 1%.125
R126	0757-0317	RES 1.33K 1%.125
R127	0698-3153	RES 3.83K 1%.125
R128	0698-3156	RES 14.7K 1%.125
R129	0698-3156	RES 14.7K 1%.125
R136	0698-3153	RES 3.83K 1%.125
R137	0698-3442	RES 237 1%.125
R138	0757-0317	RES 1.33K 1%.125
R139	0757-0280	RES 1K 1%.125
R140	0698-0083	RES 1.96K 1%.125
R148	0757-0442	RES 10K 1%.125
R149	0757-0442	RES 10K 1%.125
R150	0757-0289	RES 13.3K 1%.125
R152	0811-3475	RES .4 1% 3W PW
R153	0757-0280	RES 1K 1%.125
R154	0757-0428	RES 1.62K 1%.125
R156	0698-0082	RES 464 1%.125
R159	0698-3155	RES 4.64K 1%.125
R160	0698-3132	RES 261 1%.125
R162	0757-0280	RES 1K 1%.125
R163	0757-0280	RES 1K 1%.125
R173	0757-0280	RES 1K 1%.125
R175	0757-0280	RES 1K 1%.125
R176	0757-1001	RES 56.2 1% .5
R177	0757-0199	RES 21.5K 1%.125
R192	0757-1001	RES 56.2 1% .5
R193	0698-3609	RES 22 5% 2
R194	0764-0033	RES 33 5% 2
R202	0698-3429	RES 19.6 1%.125
R205	0757-0416	RES 511 1%.125
R206	0757-0416	RES 511 1%.125
R209	0698-0083	RES 1.96K 1%.125
R213	0757-0462	RES 75K 1%.125
R214	0698-3153	RES 3.83K 1%.125
R215	0698-3157	RES 19.6K 1%.125
R216	0698-3157	RES 19.6K 1%.125
R221	0698-3159	RES 26.1K 1%.125
R223	0757-0438	RES 5.11K 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60006
07908-66006
07908-68006

DATE CODE : E2338

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R227	0757-0463	RES 82.5K 1%.125
R230	0757-0463	RES 82.5K 1%.125
R236	0757-0289	RES 13.3K 1%.125
R237	0757-0289	RES 13.3K 1%.125
R238	0757-0289	RES 13.3K 1%.125
R244	0757-0440	RES 7.5K 1%.125
R245	0757-0280	RES 1K 1%.125
R248	0698-3279	RES 4.99K 1%.125
R249	0757-0401	RES 100 1%.125
R254	0757-0280	RES 1K 1%.125
R255	0757-0280	RES 1K 1%.125
R256	0757-0280	RES 1K 1%.125
R257	0757-0280	RES 1K 1%.125
R259	0757-0280	RES 1K 1%.125
R262	0698-3162	RES 46.4K 1%.125
R265	0698-0082	RES 464 1%.125
R266	0757-0440	RES 7.5K 1%.125
R267	0757-0420	RES 750 1%.125
R268	0757-0280	RES 1K 1%.125
R271	0757-0280	RES 1K 1%.125
R272	0757-0280	RES 1K 1%.125
R276	0757-0280	RES 1K 1%.125
R277	0757-0438	RES 5.11K 1%.125
R278	0757-0424	RES 1.1K 1%.125
R279	0757-0279	RES 3.16K 1%.125
R281	0698-4479	RES 14K 1% .125W
R282	0698-4479	RES 14K 1% .125W
R284	0698-4462	RES 768 1% .125W
R285	0757-0447	RES 16.2K 1%.125
R286	0757-0280	RES 1K 1%.125
R288	0698-3161	RES 38.3K 1%.125
R289	0757-0443	RES 11K 1%.125
R294	0757-0463	RES 82.5K 1%.125
R301	0698-0083	RES 1.96K 1%.125
R308	0698-3157	RES 19.6K 1%.125
R309	0757-0417	RES 562 1%.125
R312	0757-0200	RES 5.62K 1%.125
R313	0757-0438	RES 5.11K 1%.125
R314	0698-3150	RES 2.37K 1%.125
R315	0757-0416	RES 511 1%.125
R316	0698-0083	RES 1.96K 1%.125
R317	0698-3438	RES 147 1%.125
R325	0757-0438	RES 5.11K 1%.125
R326	0698-4435	RES 2.49K 1%
R327	0757-0280	RES 1K 1%.125
R336	0757-0438	RES 5.11K 1%.125
R349	0757-0280	RES 1K 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60006
07908-66006
07908-68006

DATE CODE : E2338

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R357	0757-0280	RES 1K 1%.125
R358	0698-3279	RES 4.99K 1%.125
R359	0698-3279	RES 4.99K 1%.125
R360	0698-3279	RES 4.99K 1%.125
R365	0757-0442	RES 10K 1%.125
R366	0757-0442	RES 10K 1%.125
R373	0698-3459	RES 383K 1%.125
R374	0757-0442	RES 10K 1%.125
R375	0757-0280	RES 1K 1%.125
R376	0757-0420	RES 750 1%.125
R377	0757-0440	RES 7.5K 1%.125
R379	0757-0438	RES 5.11K 1%.125
R380	0757-0438	RES 5.11K 1%.125
R401	0757-0442	RES 10K 1%.125
R402	0757-0421	RES 825 1%.125
R403	0698-3157	RES 19.6K 1%.125
R404	0757-0442	RES 10K 1%.125
R405	0757-0417	RES 562 1%.125
R407	0698-3150	RES 2.37K 1%.125
R408	0698-3150	RES 2.37K 1%.125
R409	0757-0467	RES 121K 1%.125
R410	0698-3266	RES 237K 1%.125
R411	0698-3160	RES 31.6K 1%.125
R412	0757-0460	RES 61.9K 1%.125
R413	0757-0467	RES 121K 1%.125
R415	0757-0458	RES 51.1K 1%.125
R416	0757-0467	RES 121K 1%.125
R417	0757-0460	RES 61.9K 1%.125
R418	0757-0460	RES 61.9K 1%.125
R419	0698-3160	RES 31.6K 1%.125
R426	0757-0280	RES 1K 1%.125
R428	0757-0280	RES 1K 1%.125
R429	0757-0442	RES 10K 1%.125
R430	0757-0280	RES 1K 1%.125
R447	0757-0280	RES 1K 1%.125
R449	0757-0438	RES 5.11K 1%.125
R460	0757-0465	RES 100K 1%.125
R466	0757-0442	RES 10K 1%.125
R469	0698-0082	RES 464 1%.125
R472	0698-3159	RES 26.1K 1%.125
R474	0698-3159	RES 26.1K 1%.125
R475	0757-0438	RES 5.11K 1%.125
R483	0698-3157	RES 19.6K 1%.125
R484	0757-0438	RES 5.11K 1%.125
R531	0757-0280	RES 1K 1%.125
R532	0757-0280	RES 1K 1%.125
R541	0757-0419	RES 681 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60006
07908-66006
07908-68006

DATE CODE : E2338

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R542	0698-3447	RES 422 1% .125
R543	0698-3447	RES 422 1% .125
R544	0757-0419	RES 681 1%.125
R550	0698-3159	RES 26.1K 1%.125
R556	0757-0442	RES 10K 1%.125
R557	0698-3150	RES 2.37K 1%.125
R558	0698-0085	RES 2.61K 1%.125
R559	0698-4037	RES 46.4 1%.125
R560	0698-4037	RES 46.4 1%.125
R561	0757-0424	RES 1.1K 1%.125
R567	0757-0797	RES 90.9 1% .50
TP146	0360-1682	TERM-PIN
TP189	0360-1682	TERM-PIN
U111	1826-0502	IC 14066B
U112	1826-0159	IC 1350
U122	1826-0328	IC 4558
U231	1906-0248	DIODE-ARRAY
U252	1826-0323	IC OP AMP
U292	1826-0323	IC OP AMP
U311	1821-0001	XSTR ARY 14P-DIP
U351	1820-0471	IC SN7406N
U361	1820-2096	IC SN74LS393N
U371	1820-2369	IC SN74LS629N
U381	1820-1374	IC 7510DI
U422	1810-0083	NETWORK-RES DIP
U431	1820-1417	IC SN74LS26N
U432	1820-1199	IC SN74LS04N
U441	1820-1197	IC SN74LS00N
U451	1820-1197	IC SN74LS00N
U452	1820-1433	IC SN74LS164
U462	1820-1112	IC SN74LS74N
U471	1820-1112	IC SN74LS '4N
U472	1820-1212	IC SN74LS112N
U482	1826-0138	IC LM339
U491	1826-0323	IC OP AMP
U492	1826-0138	IC LM339
U511	1820-1641	IC SN74LS365N
U512	1820-1730	IC SN74LS273N
U521	1820-1730	IC SN74LS273N
U531	1826-0188	IC MC1408L-8
U532	1820-1730	IC SN74LS273N
U541	1826-1033	LINEAR IC
U542	1820-1416	IC SN74LS14N
U551	T101893	IC-PROM
U552	1820-1197	IC SN74LS00N
U561	1820-1195	IC SN74LS175N
U562	1820-1640	IC SN74LS366N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60006
07908-66006
07908-68006

DATE CODE : E2338

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U571	1820-1144	IC SN74LS02N
U572	1820-1640	IC SN74LS366N
U581	1820-1199	IC SN74LS04N
VR114	1902-0184	DIODE 16.2V
VR141	1826-0276	IC MC78L05ACP
VR275	1902-3082	DIO-ZNR 4.64V 5%
VR330	1826-0555	IC LM340LAZ-5
VR431	1902-3002	DIO-ZNR 2.37V 5%
VR450	1902-3082	DIO-ZNR 4.64V 5%
VR462	1902-0041	DIODE ZNR 5.11V
VR481	1902-0041	DIODE ZNR 5.11V
VR568	1902-3140	DIO-ZNR 8.25V 2%

END OF MATERIAL LIST.

ER48 D/H: 50A, ~~[illegible]~~ C2

HEWLETT-PACKARD CO. / hp /

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LTR	REVISIONS	DATE	INIT	M F
A	AS ISSUED	12-02-81	sb/ML	M
B	REVISED PER PC48-4666	06-02-82	sb/CW	M
C	REVISED PER PC48-4830	06-10-82	sr/CS	M
D	REVISED PER PC48-6025	12-20-82	clr/CW	M
E	PLL PHASE ERROR CHANGE PER C0480296	09-28-83	db/ML	M
F	REVISED TO INCLUDE NEW FIELD RETURN TEST C0480545	01-10-84	de/ML	M
G	REVISED 4.2 AND 4.3 PER C0480717	03-20-84	de/[illegible]	M

E	C0480296	db/ML	09-28-83	MODEL 7908	STK # 07908-60006/69006
F	C0480545	de/ML	01-10-84	UPDATE/REVISION PROC	
G	C0480717	de/ML	03-20-84		DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 4
REVISIONS				SUPERSEDES	DWG # A-07908-69006-1

HEWLETT-PACKARD CO. /hp/

UPDATING AND REVISION PROCEDURE

07908-69006

This procedure contains instructions for modification of the servo PCA, 07908-60006 to version 07908-69006.

REFERENCES:

SML:	07908-68006	Untested PCA
	07908-66006	Reel
Dwgs:	F-07908-60006-1	Assembly Dwg.
	D-07908-60006-50	Schematics
	A-07908-60006-2	Test procedures
	A-07908-60006-3	Debug procedures
	F-07908-60006-20	Mod Dwg.
	07908-80006	Tape masters

Production Changes:

48-4069	Change C171 to 0160-5375
48-4093	Add wire to Rev A bd
48-4108	Change U231 from 1906-0249 to-0248
48-4155	Adds test pins
48-4175	Crosstalk filter change
48-4208	Solves extra track cross problem
48-4285	Rev. C
48-4400	PLL bandwidth change
48-4666	Rev. D Servo Board.
48-4830	Retract current and current amp changes
48-6025	Rev E. Servo Board
C048-0296	PLL Phase Error Change

E	C0480296	db/ML	09-28-83	MODEL 7908	STK # 07908-60006/69006
F	C0480545	de/ML	01-10-84	UPDATE/REVISION PROC	
G	C0480717	de/ML	03-20-84	BY	DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 2 OF 4
REVISIONS				SUPERSEDES	DWG # A-07908-69006-1

HEWLETT-PACKARD CO. /hp/

INTRODUCTION:

This article will provide information concerning the eligibilty of the servo board for revision and also concerning the revisions themselves.

REVISABLE ASSEMBLIES:

The first assembly which may be revised is D-2207. All prior assemblies are to be scrapped.

REVISIONS:

A-2108	48-4093
C-2108	48-4069,4108,4155
C-2125	48-4175
C-2129	48-4208
C-2144	48-4400
D-2207	48-4285,4666
D-2214,C-2214	48-4830
E-2240,E-2241	48-6025
E-2338	C048-0296

CURRENT ASSEMBLY:

E-2338

LT	P.C. #	APPR	DATE		
E	C0480296	db/ML	09-28-83	MODEL 7908	STK # 07908-60006/69006
F	C0480545	de/ML	01-10-84	UPDATE/REVISION PROC	
G	C0480717	de/ML	03-20-84	BY	DATE 12-01-81
				APPD	SHEET # 3 OF 4
REVISIONS				SUPERSEDES -	DWG # A-07908-69006-1

HEWLETT-PACKARD CO. hp

PROCEDURE:

1.0 Inspect all boards for general mechanical and cosmetic defects per A-5950-9205-1. Repair all component malfunctions.

2.0 Identify all boards with the following logo:
07908-69006
Current Date Code
to replace existing logo for date codes 2207 or later.

3.0 Affix, near the logo, a 7120-5480 (made in USA) label which has been stamped with the month and year of final inspection.

4.0 On board revision: D-2207 (to get to D-2214)

a) Replace R160 with 0698-3132 (261)
b) Replace R193 with 0698-3609 (22)
c) Replace R249 with 0757-0401 (100)

4.1 On board revision: D-2214,E-2240,E-2241 (to get to D,E-2338)

a) Replace R159 with 0698-3155 (4.64K)

b) Replace CR247 with 1901-0518 (Schottky Diode)

4.2 On board revision: D-2338
E-2338
a) Current Assembly

4.3 On all Rev D boards manufactured at Loveland (88809L follows board number in upper left corner) be sure that insulator pads (0340-0140) have been installed under Q183 and Q190. This prevents collector shorts to base or emitter pads.

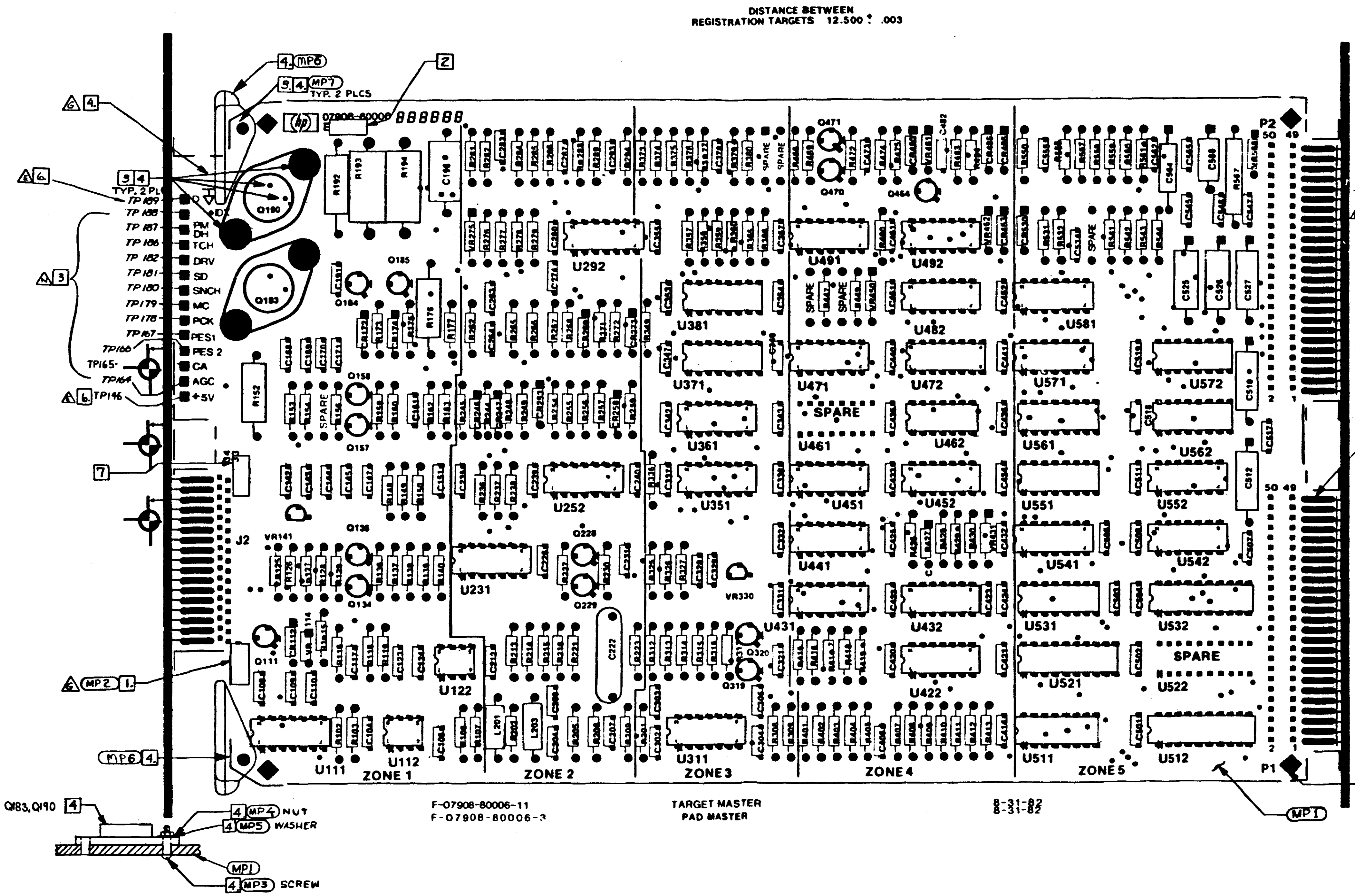
4.4 Test per A-5955-3476-1 3060 Test Procedure

and A-07908-69006-2 I/O Field Return Test Procedure

E	C0480296	db/ML	09-28-83	MODEL 7908	STK # 07908-60006/69006
F	C0480545	de/ML	01-10-84	UPDATE/REVISION PROC	
G	C0480717	de/ML	03-20-84	BY	DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 4 OF 4
	REVISIONS			SUPERSEDES	DWG # A-07908-69006-1

F-07908-60006-1

LTR	REVISIONS	APPROVED	DATE
A	AS ISSUED		[illegible]
B	ENLARGE Bs. BOARD REV D TC B / PC 48-4065		[illegible]
C	BD REV WAS "B". PHOTO DATE WAS 8-14-81 PER PC48-4073		3/24/81
D	ADD NOTE 5 PER PC 48-4093	AHJ / [illegible]	[illegible]
E	ADD NOTE 6 PER PC 48-4[illegible]	AHJ / [illegible]	[illegible]-4-81
F	NOTE 2 DATE CODE WAS 2[illegible] PC 48-4[illegible]	AHJ / [illegible]	[illegible]
G	NOTE 2 DATE CODE WAS 21[illegible] PC48-4[illegible]	[illegible]	[illegible]
H	NOTE 2 DATE CODE WAS 2129 PC 48-4[illegible]	[illegible] / CW	[illegible]-81
J	ADDED NOTE 8 PER PPCC 48-4372	HTS / CW	[illegible]-82
K	ADDED DATE CODE [illegible] PC 48-[illegible]	HTS / CW	[illegible]-82
L	REVISED NOTE 8; DATE CODE WAS C-2144 / D-2144, PER PC 48-[illegible]	[illegible] / CW	[illegible]
M	DATE CODE WAS D-2207 PER PC48-[illegible]	[illegible] CW	6-16-82
N	BD REV WAS [illegible] DATE CODE WAS D-2214 DELETED NOTE 8. PER PC 48-6025	[illegible] / RL	[illegible]/82
P	DATE CODE WAS E-2240 [illegible]	[illegible]	9-27-8[illegible]



F-07908-80006-9 GRAPHICS COMPONENT SIDE 8-31-82

REFERENCE DRAWINGS:
SCHEMATIC D-07908-60006-50, 3 SHTS

UNLESS OTHERWISE SPECIFIED:

THIS BOARD CONFORMS TO CORPORATE AUTOMATIC INSERTION STANDARDS AS PER AXIAL LEAD STANDARDS 4-11-80

NOTES:

1. INSTALL (MP2) AFTER LINE TEST. E-2338
2. MARK ASSEMBLY DATE CODE ____________
3. MASK PRIOR TO LOADING.
4. TOUCH UP, INSTALL (MP3-7)
5. CONNECT A WIRE FROM CR530 TO R531 WHERE IT CONNECTS TO R532. THIS APPLIES TO B REVISION ARTWORK ONLY.
6. INSTALL TEST PINS AS SHOWN.
7. PC PRODUCTION: MARK ASSEMBLY WORK ORDER NUMBER, COMPONENT SIDE ONLY.

NOTE:
THIS BOARD DOES NOT CONFORM TO UNIVERSAL TEST FIXTURES.

DATE 7-24-80 / 2/[illegible]/81 / [illegible]	TITLE SERVO ASSEMBLY
NEXT ASSEMBLY	SEE WHERE USED
PART NUMBER	07908-60006
FINISH —	SCALE 2:1
HEWLETT PACKARD	F-07908-60006-1
SHEET 1 OF 1	

ER48 D/H: 50A, ~~50B~~ C2

HEWLETT-PACKARD CO. / hp /

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LTR	REVISIONS	DATE	INIT	MF
A	AS ISSUED	12-02-81	sb/ML	M
B	REVISED PER PC48-4666	06-02-82	sb/CW	M
C	REVISED PER PC48-4830	06-10-82	sr/CS	M
D	REVISED PER PC48-6025	12-20-82	clr/CW	M
E	PLL PHASE ERROR CHANGE PER C0480296	09-28-83	db/ML	M
F	REVISED TO INCLUDE NEW FIELD RETURN TEST C0480545	01-10-84	de/ML	M
G	REVISED 4.2 AND 4.3 PER C0480717	03-20-84	de/[illegible]	M

E	C0480296	db/ML	09-28-83	MODEL 7908	STK # 07908-60006/69006
F	C0480545	de/ML	01-10-84	UPDATE/REVISION PROC	
G	C0480717	de/ML	03-20-84		DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 4
REVISIONS				SUPERSEDES	DWG # A-07908-69006-1

ER48 D/H: 50A, 50B

HEWLETT-PACKARD CO.   hp

UPDATING AND REVISION PROCEDURE

07908-69006

This procedure contains instructions for modification of the servo PCA, 07908-60006 to version 07908-69006.

REFERENCES:

SML:	07908-68006	Untested PCA
	07908-66006	Reel
Dwgs:	F-07908-60006-1	Assembly Dwg.
	D-07908-60006-50	Schematics
	A-07908-60006-2	Test procedures
	A-07908-60006-3	Debug procedures
	F-07908-60006-20	Mod Dwg.
	07908-80006	Tape masters

Production Changes:

48-4069	Change C171 to 0160-5375
48-4093	Add wire to Rev A bd
48-4108	Change U231 from 1906-0249 to-0248
48-4155	Adds test pins
48-4175	Crosstalk filter change
48-4208	Solves extra track cross problem
48-4285	Rev. C
48-4400	PLL bandwidth change
48-4666	Rev. D Servo Board.
48-4830	Retract current and current amp changes
48-6025	Rev E. Servo Board
C048-0296	PLL Phase Error Change

E	C0480296	db/ML	09-28-83	MODEL 7908	STK # 07908-60006/69006
F	C0480545	de/ML	01-10-84	UPDATE/REVISION PROC	
G	C0480717	de/ML	03-20-84	BY	DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 2 OF 4
REVISIONS				SUPERSEDES	DWG # A-07908-69006-1

INTRODUCTION:

This article will provide information concerning the eligibilty of the servo board for revision and also concerning the revisions themselves.

REVISABLE ASSEMBLIES:

The first assembly which may be revised is D-2207. All prior assemblies are to be scrapped.

REVISIONS:

A-2108	48-4093
C-2108	48-4069,4108,4155
C-2125	48-4175
C-2129	48-4208
C-2144	48-4400
D-2207	48-4285,4666
D-2214,C-2214	48-4830
E-2240,E-2241	48-6025
E-2338	C048-0296

CURRENT ASSEMBLY:

E-2338

PROCEDURE:

1.0 Inspect all boards for general mechanical and cosmetic defects per A-5950-9205-1. Repair all component malfunctions.

2.0 Identify all boards with the following logo:
07908-69006
Current Date Code
to replace existing logo for date codes 2207 or later.

3.0 Affix, near the logo, a 7120-5480 (made in USA) label which has been stamped with the month and year of final inspection.

4.0 On board revision: D-2207 (to get to D-2214)

a) Replace R160 with 0698-3132 (261)
b) Replace R193 with 0698-3609 (22)
c) Replace R249 with 0757-0401 (100)

4.1 On board revision: D-2214,E-2240,E-2241 (to get to D,E-2338)

a) Replace R159 with 0698-3155 (4.64K)

b) Replace CR247 with 1901-0518 (Schottky Diode)

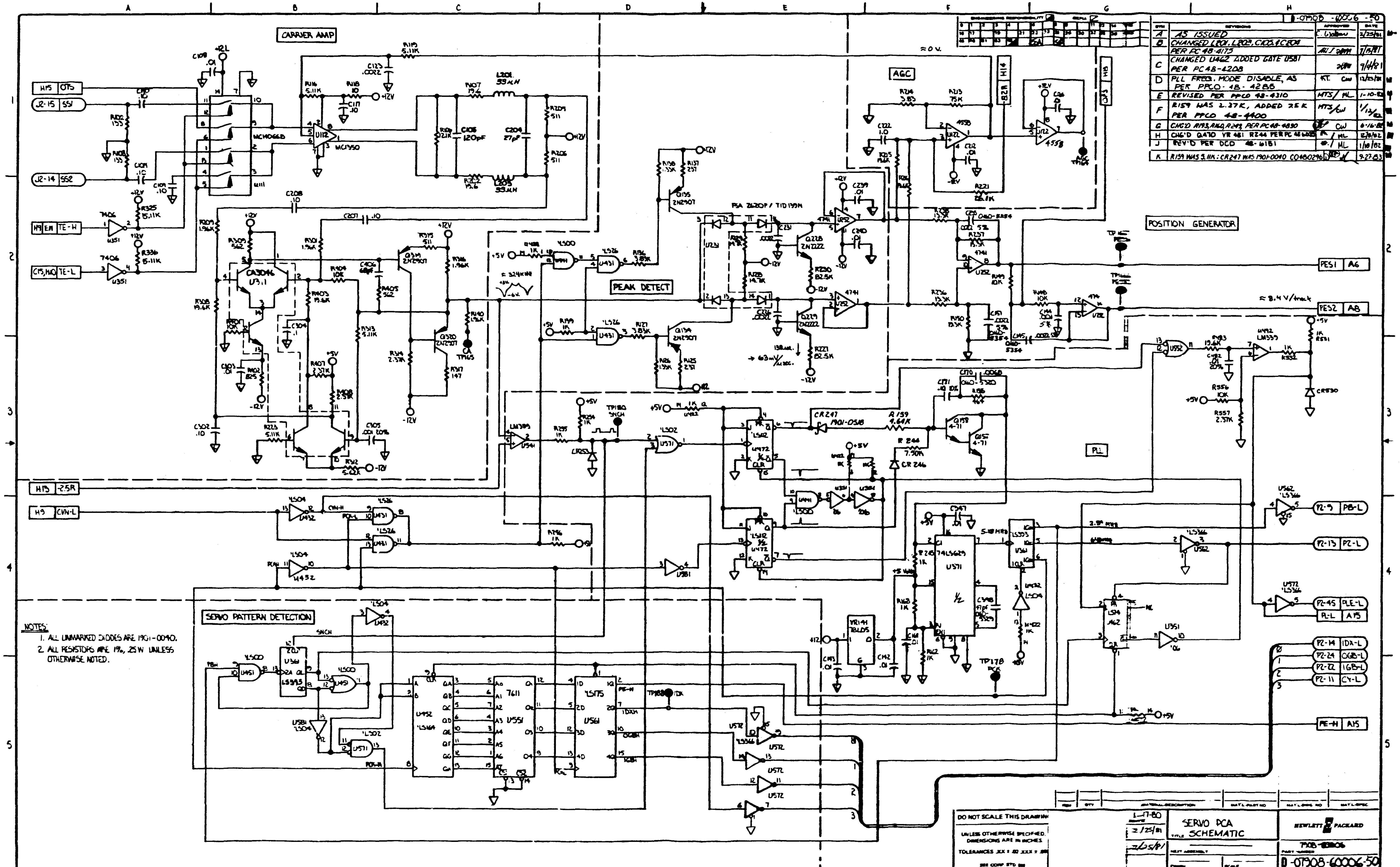
4.2 On board revision: D-2338
E-2338
a) Current Assembly

4.3 On all Rev D boards manufactured at Loveland (88809L follows board number in upper left corner) be sure that insulator pads (0340-0140) have been installed under Q183 and Q190. This prevents collector shorts to base or emitter pads.

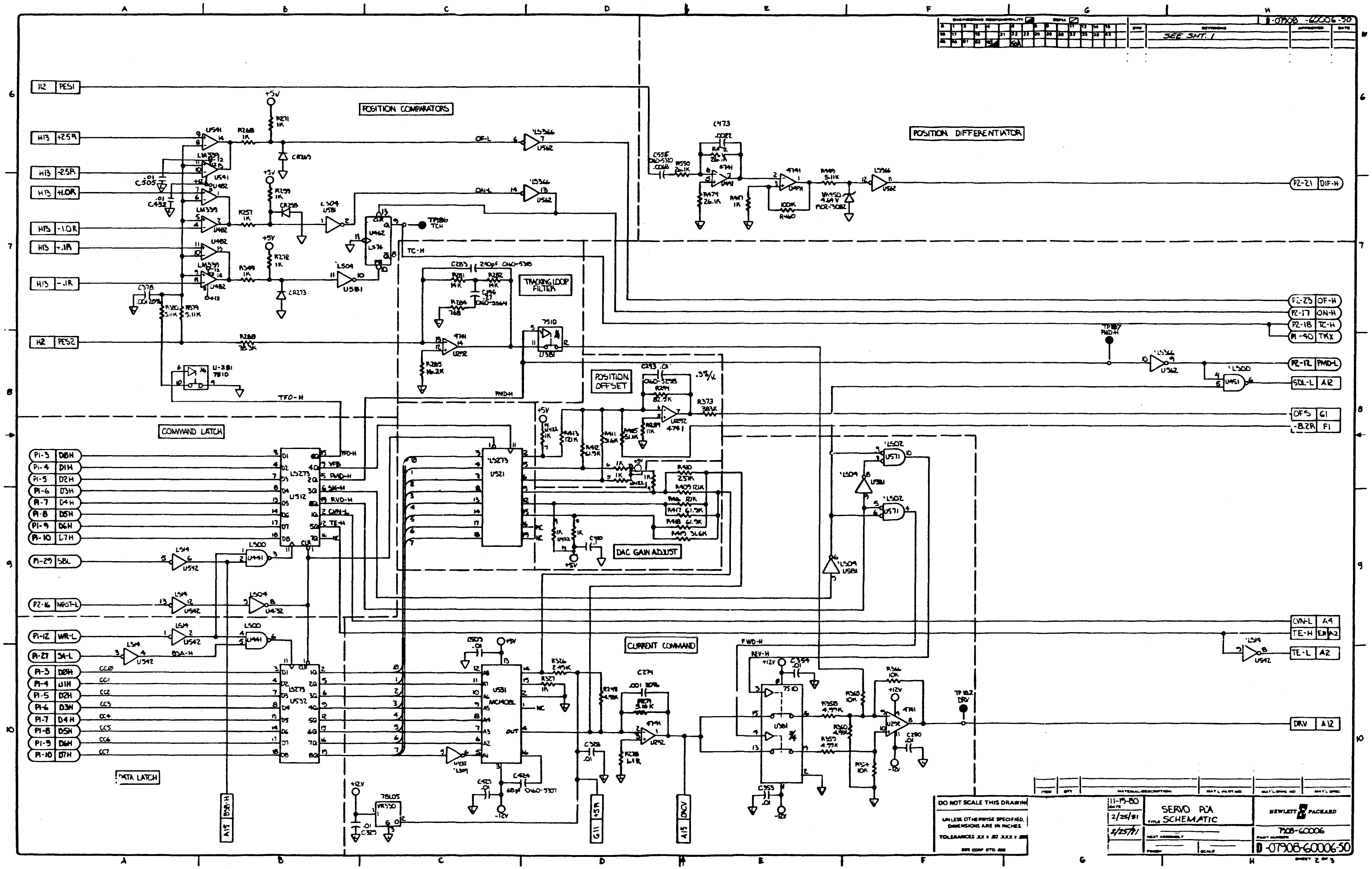
4.4 Test per A-5955-3476-1 3060 Test Procedure

and A-07908-69006-2 I/O Field Return Test Procedure

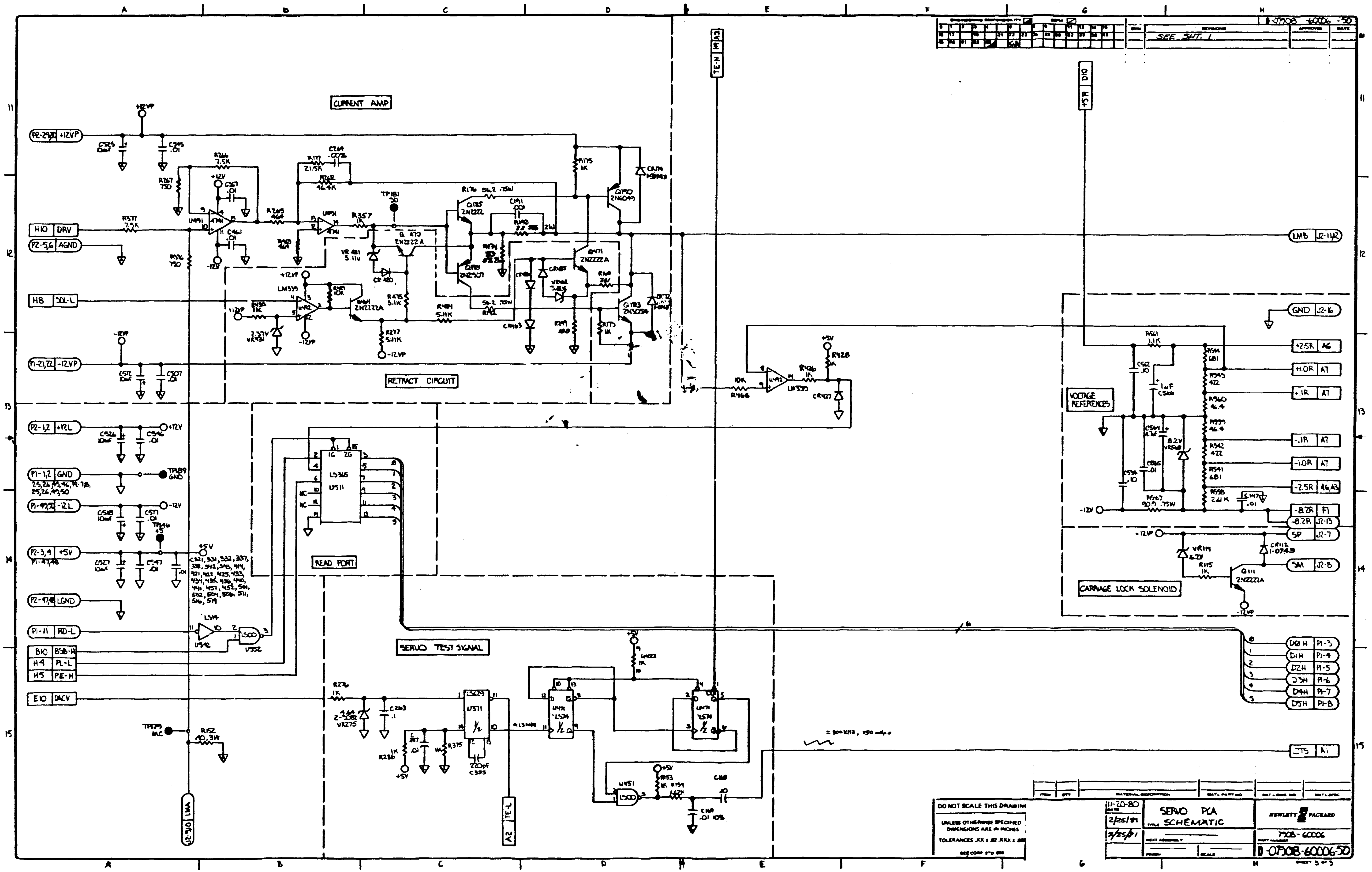
E	C0480296	db/ML	09-28-83	MODEL 7908	STK # 07908-60006/69006
F	C0480545	de/ML	01-10-84	UPDATE/REVISION PROC	
G	C0480717	de/ML	03-20-84	BY	DATE 12-01-81
LT	P.C. #	APPR	DATE	APPD	SHEET # 4 OF 4
	REVISIONS			SUPERSEDES	DWG # A-07908-69006-1



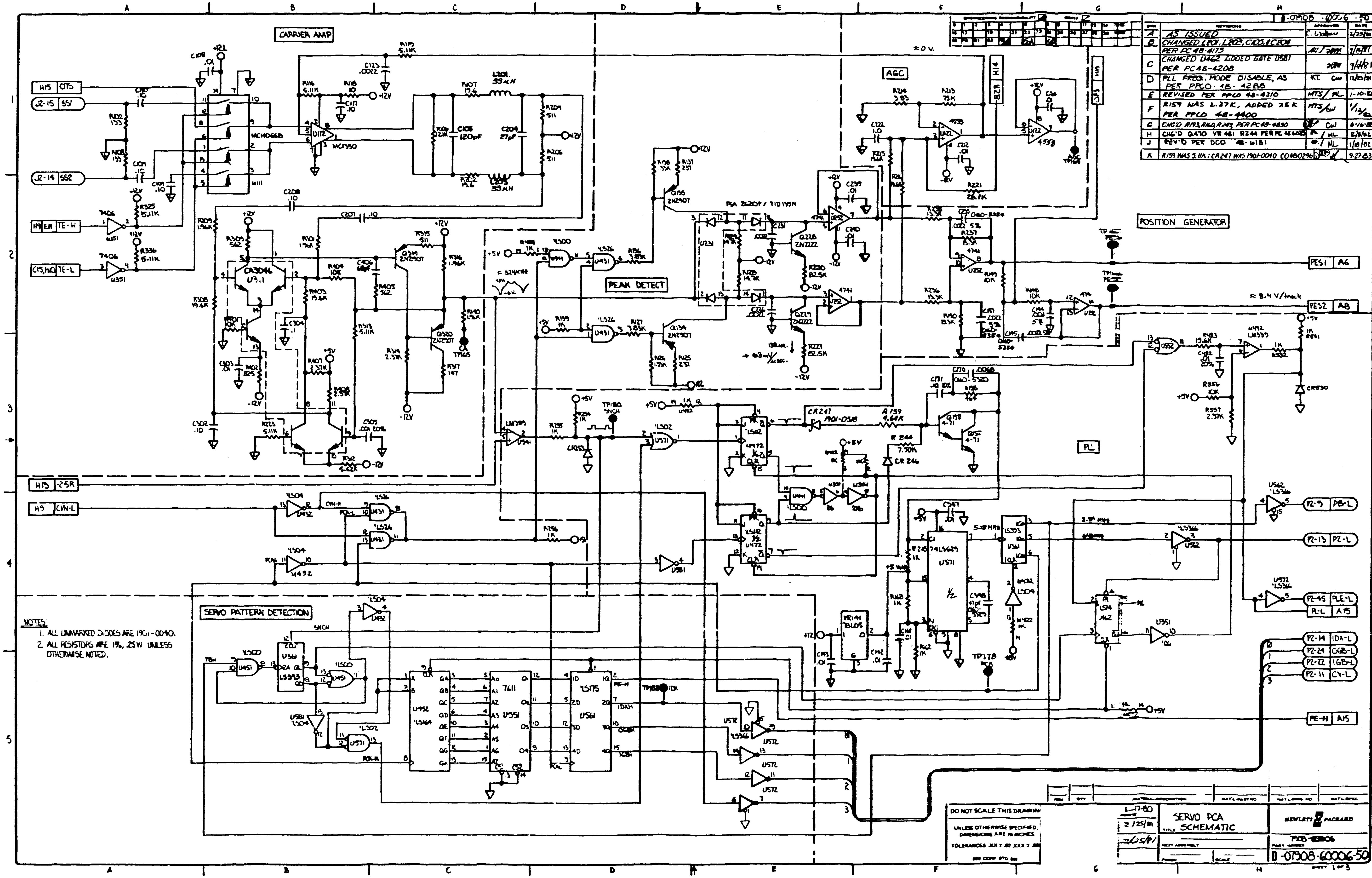
CARRIER AMP
PEAK DETECT
AGC
POSITION GENERATOR
PLL
SERVO PATTERN DETECTION
NOTES:
1. ALL UNMARKED DIODES ARE 1901-0040.
2. ALL RESISTORS ARE 1%, .25W UNLESS OTHERWISE NOTED.
A AS ISSUED
B CHANGED L201, L203, C105, & C204 PER PC 48-4175
C CHANGED U462 ADDED GATE U581 PER PC 48-4208
D PLL FREQ. MODE DISABLE, AS PER PPCO-48-4288
E REVISED PER PPCO 48-4310
F R159 WAS 2.37K, ADDED 25K PER PPCO 48-4400
J REV'D PER DCD 48-6181
DO NOT SCALE THIS DRAWING
SERVO PCA SCHEMATIC
HEWLETT PACKARD
D-07908-60006-50



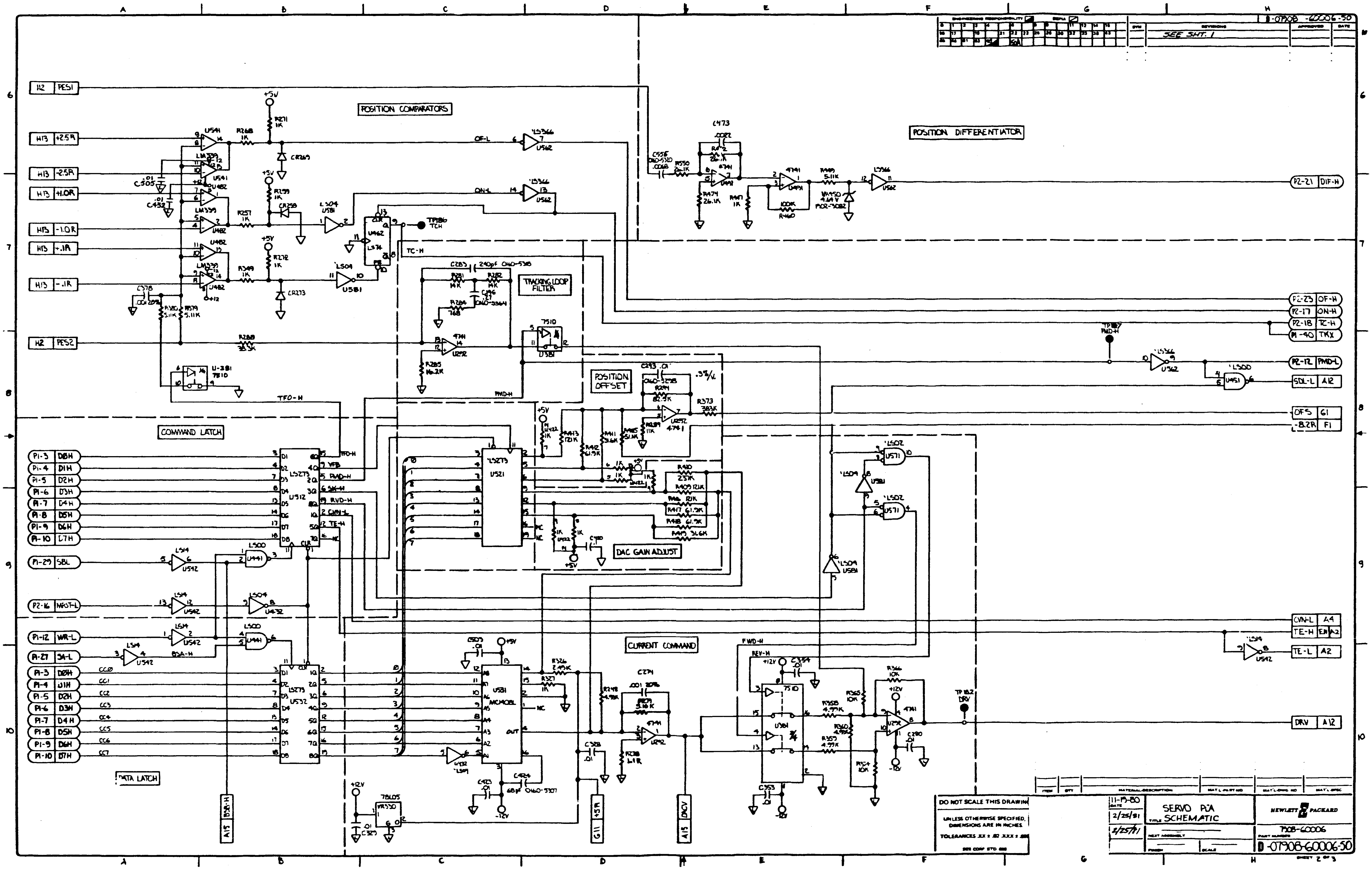
POSITION COMPARATORS
POSITION DIFFERENTIATOR
TRACKING LOOP FILTER
POSITION OFFSET
DAC GAIN ADJUST
COMMAND LATCH
DATA LATCH
CURRENT COMMAND
SEE SHT. 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
11-19-80
2/25/81
2/25/81
SERVO PCA
SCHEMATIC
HEWLETT PACKARD
7908-60006
D-07908-60006-50
SHEET 2 OF 3

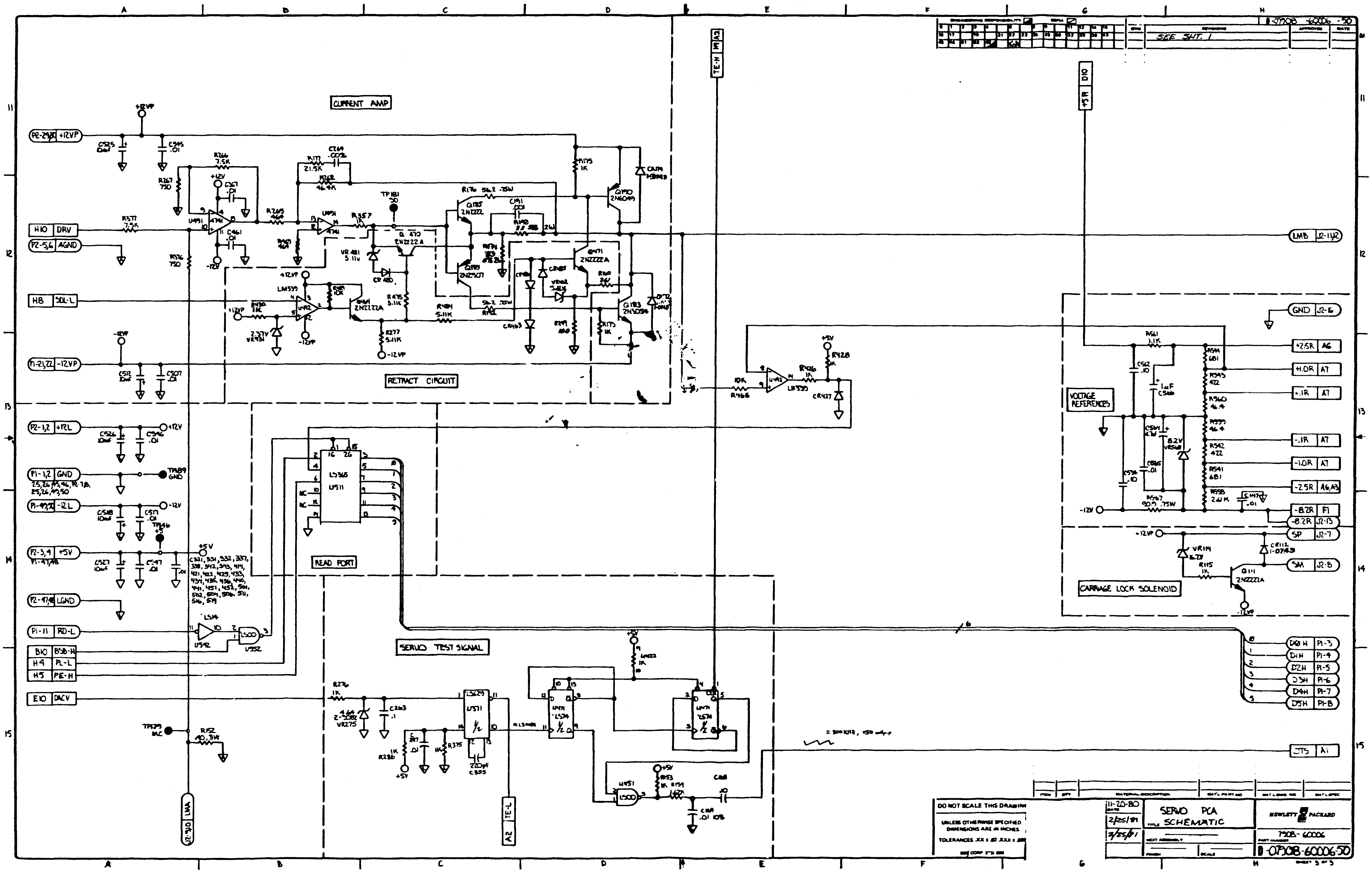


SEE SHT. 1
CURRENT AMP
RETRACT CIRCUIT
READ PORT
SERVO TEST SIGNAL
VOLTAGE REFERENCES
CARRIAGE LOCK SOLENOID
TE-H
+5R
D10
LMA
TE-L
P2-29,30 +12VP
H10 DRV
P2-5,6 AGND
H8 SDL-L
P1-21,22 -12VP
P2-1,2 +12L
P1-1,2 GND
P1-49,50 -12L
P2-3,4 +5V
P2-47,48 LGND
P1-11 RD-L
B10 BSB-H
H4 PL-L
H5 PE-H
E10 DACV
LMB J2-1,2
GND J2-16
+2.5R A6
H.OR A7
+.1R A7
-.1R A7
-1.0R A7
-2.5R A6,A3
-8.2R F1
-8.2R J2-13
SP J2-7
SM J2-8
D0H P1-3
D1H P1-4
D2H P1-5
D3H P1-6
D4H P1-7
D5H P1-8
JTS A1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
11-20-80
2/25/81
3/25/81
SERVO PCA
SCHEMATIC
HEWLETT PACKARD
7908-60006
D-07908-60006-50
SHEET 3 OF 3



CARRIER AMP
AGC
PEAK DETECT
POSITION GENERATOR
PLL
SERVO PATTERN DETECTION
NOTES:
1. ALL UNMARKED DIODES ARE 1901-0040.
2. ALL RESISTORS ARE 1%, .25W UNLESS OTHERWISE NOTED.
REVISIONS
A AS ISSUED C. Wolfe 2/25/81
B CHANGED L201, L203, C105 & C204 PER PC 48-4175 7/13/81
C CHANGED U462 ADDED GATE U581 PER PC48-4208 9/4/81
D PLL FREQ. MODE DISABLE, AS PER PPCO-48-4286 KT. CW 12/23/81
E REVISED PER PPCO 48-4310 MTS/ML 1-10-82
F R159 WAS 2.37K, ADDED 25K PER PPCO 48-4400 MTS/CW 1/13/82
G CHG'D R193, R160, R243 PER PC48-4830 CW 6-16-82
H CHG'D Q470 VR481 R244 PER PC 48-6025 ML 12/8/82
J REV'D PER DCO 48-6181 ML 1/10/83
K R159 WAS 5.11K: CR247 WAS 1901-0040 C0480296 9-27-83
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED. DIMENSIONS ARE IN INCHES.
1-17-80
2/25/81
2/25/81
SERVO PCA
TITLE SCHEMATIC
HEWLETT PACKARD
7908-60006
D-07908-60006-50
SHEET 1 OF 3


POSITION COMPARATORS
POSITION DIFFERENTIATOR
TRACKING LOOP FILTER
POSITION OFFSET
COMMAND LATCH
DAC GAIN ADJUST
CURRENT COMMAND
DATA LATCH
SEE SHT. 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
SERVO PCA SCHEMATIC
11-19-80
2/25/81
HEWLETT PACKARD
7908-60006
D-07908-60006-50


CURRENT AMP
RETRACT CIRCUIT
READ PORT
SERVO TEST SIGNAL
VOLTAGE REFERENCES
CARRIAGE LOCK SOLENOID
SEE SHT. 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
SERVO PCA
SCHEMATIC
HEWLETT PACKARD
7908-60006
D-07908-60006-50

P/N 07908-60205

READ/WRITE PCA-A3

Series Code E-2300

ER48 D/H: C2

HEWLETT-PACKARD CO. / hp /

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline) (L308)

LTR	REVISIONS	DATE	INIT	M F
A	AS ISSUED	07-20-82	jmm/LAC	M

A	ISSUED	jmm/LAC	07-20-82	MODEL 7908	STK # 07908-60205
		/	- -	INTERNAL MAINTENANCE SPECIFICATION	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 69
REVISIONS				SUPERSEDES	DWG # A-07908-60205-4

INTERNAL MAINTENANCE SPECIFICATION

7908 READ/WRITE

I. OVERVIEW

The 07908-60205 PCA performs physical data writes and data reads on the IMI disc drive.

A block diagram of the Read/Write board is given in Figure 1. There are nine principle blocks.

The control logic and fault latch block interfaces the Read/ Write circuitry to the micropocessor circuitry. The microprocessor is capable of controlling the operation of the Read/Write by setting control bits in the various registers in this block. The microprocessor can ascertain drive status by reading the status register (Fault Latch).

The sector timing logic takes servo clock information from the servo PCA and generates sector timing information which controls the operation of the rest of the Read/Write PCA. The sector timing logic is the state machine which determines when particular operations must be performed.

The timing recovery block generates data timing information which controls when individual data bits are written or read. During a write operation, the data is clocked from timing information supplied by the servo PCA. During a read operation, the Timing Recovery Block recovers clock information from the data bits as they are read from the disc.

I. OVERVIEW (Continued)

The Write Gate Generator block determines when data should be recorded on the disc and when data should not be recorded on the disc.

The Disc Mechanism Interface converts the TTL control signals from the control logic to logic levels required by the preamplifier chips in the sealed disc mechanism. This block also generates the power supplies required by these chips.

The Write Drivers are the devices which send data to the preamplifier chips during a write operation.

The signal processing block performs analog signal processing on the data signal which is read from the disc. This processing consists of a noise filter, a differentiator, a zero crossing detector, and an automatic level control (AGC) loop.

The Data Formatter accepts serial binary (NRZ format) data from the host interface PCA and encodes this data in MFM format. The data formatter also generates the VCO sync field and the data start bit information which is recorded on the disc during a write.

The data separator accepts MFM formatted information from the disc and decodes this information to NRZ format. This block strips out the VCO sync filed and data start bit information and transfers only data information to the host interface PCA.

II. DISC FORMAT

One data sector physically occupies 300 bytes on the disc. The sector format is shown in Figure 2. Also shown in Figure 2 is the relationship between the sector format and 4 timing signals used by various read/write circuits in generating the sector format.

The VCO sync field is 20 bytes long. The sync field is composed of an MFM encoded all zeroes pattern. The sync field is used by the timing recovery block on the read/write PCA to achieve phase lock. The VCO sync field ends with a 1 bit data start bit which is used to signal the beginning of the header field. This start bit is an MFM encoded "one" bit.

The 269 bytes recorded in the header, data, ECC, and CRC fields are presented in NRZ format to the read/write PCA by the DMA PCA. The read/write PCA merely records this information in MFM format on the disc. The header field consists of six bytes of status and address information. The data field contains the recorded user data. In the 7908, the ECC field is an MFM -encoded all "zeroes" pattern since the drive does not have an ECC option. The CRC field contains the cyclic redundancy check bits generated by the DMA PCA.

II. DISC FORMAT (Continued)

The final ten bytes of the sector comprise an "intersector gap" area filled with an MFM -encoded all "zeroes" pattern. This field supplies additional clocking to the DMA to clear the DMA's process pipeline. Not all of these bytes are required for this, so some future expansion of the 7908's capacity is possible.

Figure 3 shows the physical track format used by the 7908. There are 36 physical sectors per track. They are labeled 0 thru 35. The index pulse, also shown in Figure 3, is a once around timing pulse generated by the servo. This index pulse serves to identify sector 0. The index pulse occurs 40 bytes prior to the beginning of sector 0. This allows plenty of time for the controller to recognize that sector 0 is coming up. In fact, it probably allows more time than is needed. This is nice, in case we ever decide to expand the 7908 to 17 Mbytes by eliminating the gap fields in each sector to expand to 37 sectors per track [10 bytes x 36 = 360 bytes which is more than enough for one more sector].

III. CONTROL LOGIC AND FAULT LATCH BLOCK AND WRITE GATE GENERATOR BLOCK

This section is shown on sheet 1 of the schematics for the 7908 Read/Write PCA. U622 is a bus buffer through which data from the microprocessor PCA passes on the way to the control latches.

U621, U631, and part of U641 generates the various select signals used by the fault latch and the control latches.

U632 is the "Formatter-Separator" control latch. It is selected by inputs FSS-L and WR-L. These inputs are generated by the microprocessor PCA. Bit B7 of U632 is the Write Select bit. Its mnemonic is WRT-H. When asserted, this bit forces the timing recovery block to synchronize to the servo bit clock, P8-L.

Bit B6 of U632 is unused. However, this bit position does reflect the state of the target sector control bit, TGT-H. This control bit, when asserted, enables the PCA to write one sector of information on the disc.

TGT-H control information is actually processed by the write gate generator, U611 and U512 as shown in Figure 4. The microprocessor PCA asserts TGT-H by writing a logic "1" to bit B6 of the Formatter-Separator control latch. This bit is latched by U611 as shown in Figure 4 If WRT-H is also asserted, then TGT-H will be clocked thru the write gate generator on the next low to high transition of the start of sector control line, SOS-H. Unless TGT-H is reasserted after the SOS-H, the PCA will write one and only one sector of data if all other conditions permit. (See Figure 4 for the timing details of the Write Gate Generator.) If TGT-H is reasserted after SOS-H, multiple sector writes are possible.

III. CONTROL LOGIC AND FAULT LATCH BLOCK AND WRITE GATE GENERATOR BLOCK (Continued)

Bit B5 of U632 is the Device Select Bit, DEV-H. This bit enables data transfer between the R/W PCA and the DMA PCA to take place. It does this by controlling the access of the R/W PCA to the DMA-FORMATTER/SEPARATOR bus. When DEV-H is asserted, then U652 SIDE 2Y is enabled. This allows the R/W PCA to drive the Start Of Data (SOD-L), Start Of Sector (SOS-L), NRZ Read Data (Fout-H), and Read/Write Clock (RWCK-L) lines on the mother board. When DEV-H is de-asserted, these lines are tri-stated. U642 is the "READ/WRITE" control latch. It is selected by inputs SLG-L and WR-L. These inputs are generated by the microprocesor PCA. Bits B7 and B6 of U642 are the Head Select bits, H2-L and H1-L. Bits B1 and B0 of U642 are the chip enable bits, EN1-H and EN0-H. The combination of these 4 bits controls which head is selected in the disc mechanism. The selection code for the heads is given in Figure 5. Head 0 is the lowest data platter in the mechanism. Head 4 is the top data platter in the mechanism. The other heads are numbered in order from bottom to top.

Bits B5 and B4 of U642 are the write current control bits. WC2-H and WC1-H, when asserted, each of these bits causes a decrease in the level of write current applied to the drive.

U652 is a bus buffer. Side 1Y is always enabled. Side 2Y is controlled by DEV-H. Bit B3 is the input part for the Master Reset Control Line, MRST-L. This input is generated by the power supply. When asserted, it disables write operations and sets the Read/Write PCA to a known state.

III. CONTROL LOGIC AND FAULT LATCH BLOCK AND WRITE GATE GENERATOR BLOCK (Continued)

Bit B2 is the input part for On-Track qualifier, ONTH. ONT-H is generated by the Servo PCA. When asserted, it indicates that the heads are positioned over a track.

Bit B1 is the input part for the Write Data data input, WDA-H. WDA-H is the serial NRZ data orginating from the DMA PCA which the Read/Write PCA will encode and record on the disc.

Bit B0 is an output part for the Sector Timing Pulse, STP-L. This pulse is exactly the same as SOS-L. However, STP-L can not be tri-stated. Hence, it is always available to the microprocessor PCA for determining rotational position on the disc.

U681, U692, U682, and U672 comprise the Fault Latch. The fault latch is selected by the FLS-L input. When RD-L is asserted with FLS-L, the contents of the fault latch are returned to the deasserted state.

Bit B7 of U672 is the phase Lock Dropped Out bit, DPOL. This status bit is a latched indicator of the status of the Timing Recovery Block. When asserted, DPO-L indicates that loss of phase lock occurred in the Timing Recovery Block.

Bit B6 of U672 is the instantaneous state of the out of lock detector which monitors the Timing Recovery Block. This bit is called the Out Of Lock bit, OTL-L.

Bit B5 is the "speed okay" bit, SOK-H, which is not used in the 7908.

III. CONTROL LOGIC AND FAULT LATCH BLOCK AND WRITE GATE GENERATOR BLOCK (Continued)

Bit B4 is the "Off-Track While Writing" bit, WOT-L. This bit is asserted if ONT-H is de-asserted during a write.

Bit B3 of U672 is state of the ONT-H bit. When de-asserted, this indicates that we went off track. This is a latched signal.

Bit B2 of U672 is the "Power Fail" bit, PFAI-L. This bit is the latched output of the power supply's power fail detector. When asserted, it means that a power fail sequence has been initiated.

Bit B2 of U672 is the "Servo Timing Error" bit, PLE-L. This bit is a latched output of the servo PCA and, when asserted, means that timing information from the servo is invalid.

Bit B0 of U672 is the "Destructive Write Fault" bit, DWF-L. This bit is generated in the disc mechanism and is level converted by U161 on page 5 section F21 of the read/write PCA schematic. When asserted, it means a falt condition has arisen which caused the destruction of data on the most recently written sector. It does not imply physical damage to the disc mechanism. The most frequent causes of the DWF-L condition during a write include:

1. Selecting a non-existent head;
2. Failure of the write current circuitry (most frequently, Q225); or,
3. Failure of the write driver or formatter block.

IV. SECTOR TIMING LOGIC

Refer to page 3 of the READ/WRITE PCA schematic. U6111, U6112, U6101,U691, U572, U552, U641, U592, and U582 comprise the Sector Timing Logic. U6101, U6111, and U6112 are synchronous decade counters which count byte cells. The duration of one byte cell is determined by Servo Timing Signal P2-L. One byte cell is defined to be the time required to record eight NRZ bits on the disc mechanism. P2-L is derived by the Servo PCA from servo information recorded on the servo surface of the disc mechanism. The frequency of P2-L is nominally 648 KHZ.

The sector timing counter counts from 1 to 300. It then synchronously resets to 1 and begins the count again. The sector timing counter logic is depicted in simplified form in Figure 6. Note that LD and CLR are synchronous inputs to 74LS162 counters and cause changes in the counter's outputs to occur only on the positive-going edge of the clock.

There are four control outputs derived from the sector timing counter. AQM-L is the acquisition mode control signal. When AQM-L is asserted, the Timing Recovery Block acquires phase and frequency lock with the VCO sync field. MFM tracking operation is disabled during this time to allow the Timing Recovery Block to sync with the signal.

IV. SECTOR TIMING LOGIC (Continued)

SYN-H is the sync control bit. When SYN-H is asserted, the separator circuitry sync itself to properly decode MFM data.

DTP-H is the Data Timing Pulse. During a write operation, the data timing pulse signals the beginning of actual data recording. When DTP-H is asserted, the formatter causes the data start bit to be written and a start of data (SOD-L) to be sent to the DMA PCA.

SOS-L is the Start of Sector control bit. When asserted, SOS causes the sector timing counter to reset and forces the Formatter, Separator, and Write Gate Generator blocks to enter their initial states.

These four control signals are synchronously presented to the other Read/Write circuitry by the flipflops U592 and U582. This assures that all activity is synchronized at the bit level. This synchronization is accomplished by using the Read /Write clock, RWC-H, to qualify the outputs times of the bits. Flipflops U592 and U582 and gates U572 and U552 assure that the control bits are asserted and de-asserted at the proper time.

The Sector Timing Logic has one other input. That input is the once-around index pulse, IDX-L. When IDX-L is asserted, it means that only 40 bytes are left before the end of the last sector. IDX-L assures that the Sector Timing Counter gets initialized to its proper state by synchronously jamming a count of 260 (decimal) into the counter.

IV. SECTOR TIMING LOGIC (Continued)

Since 300 - 260 = 40, this assures that sector 0 always begins precisely 40 bytes after INDX-L is asserted. Flipflop U691 and NAND gate U641 serve to generate a one byte sync pulse, INDX-L, which is sent to the microprocessor PCA at the beginning of sector 0 to indicate the actual beginning of physical sector 0. IDX-L is not used for this purpose because IDX-L is two bytes in duration. [Note that one "byte duration" equals the time interval required to read eight bits of NRZ data from the disc].

Note that counters U6101, U6111, and U6112 have synchronous load and clear inputs. Note also that flipflops U582 and U592 have asynchronous clear inputs which override their asynchronous preset inputs.

V. FORMATTER

A detailed block diagram of the formatter is depicted in Figure 7. There are three blocks: The transition logic, the MFM Encoder, and the Sync Bit Generator.

The Sync Bit Generator determines when the Data Start Bit is to be recorded on the disc. The Sync Bit Generator is comprised of flipflops U522 and part of U532 and NAND gate U641. The circuit is shown in Figure 8.

Prior to the Start of Sector, the signals are as shown in Figure 8. When SOS-L is asserted, CLR-L is immediately asserted and is sent to the MFM encoder. This assures proper phasing of the VCO sync field which the Transition Logic will begin to record. Since SOS-L is asserted for one byte-time, and since RWC-H is the bit clock, SOS-L will be asserted for 8 cycles of RWC-H.

During the time between SOS-L going low and DTP-L going low, the Transition Logic is recording the VCO sync field on the disc. After DTP-L is asserted, CLR-L is de-asserted. The next bit to be recorded will be the Data Start Bit. When Start-L is asserted, the MFM Encoder will cause a "1" transition to be recorded on the disc.

The MFM Encoder is shown in Figure 9. The actual encoding is performed by NOR gates U562 and OR gates U681. The output CODE-L carries the MFM transition information in the falling edge of CODE-L.

V. FORMATTER (Continued)

In MFM coding, a transition occurs at the bit cell boundary between adjacent "0" bits or in the center of the bit cell of a "1" bit. Transistions between adjacent "0" cells are controlled by RWC-L being asserted. Transitions in the center of "1" cells are controlled by RWC-H being asserted.

The Data Start Bit is generated by START-L being asserted. Prior to START-L, the flipflops U542 are in the cleared state. (See Figure 8). When START-L is asserted, the first flipflop is preset to the "1" state. This "1" is then clocked through the encoder. Serial NRZ data line WDA-H follows this start bit with data from the DMA PCA.

The Transition Logic is shown in Figure 10. Flipflop U532 is a toggle flipflop which changes state with each negative-going edge of CODE-L. U532 is a schottky part, because its very close matching between output rise and fall times is required for minimizing write jitter. A Low Power Schottky part has too much mismatch to be used in this application.*

Level shifter U541 converts the TTL levels output from U532 to ECC compatible outlets as required by the write driver.

---

* Some Schottky parts sometimes have a temperature problem that slows their switching speed. If this happens to U532, the symptom will be a temperature dependent increase in hard errors. Changing U532 will cure this problem.

VI. WRITE DRIVERS

The Write Driver circuitry is shown in Figure 11. When the write gate, WRG-L, is de-asserted, the open collector outputs of U321 are high impedances. In this case, the voltage at the base of transistors Q157 is roughly zero volts. Q157 is therefore, in the cutoff state since RCD-H rand RCD-L are always voltages less then zero.

When WRG-L is asserted, both comparators U321 clamp their outputs to roughly -12 volts. This draws current through CR244 and acts to bias Q157. Q157 then, acts as a high gain differential amplifier to inputs RCD-H and RCD-L.
The outputs DX and DY go to the preamplifier ICs located in the disc mechanism which record DX and DY on the disc.

Two comparators U321 are used in this circuit to assure that sufficient current sink capability exists to bias Q157.

VII. SIGNAL PROCESSING BLOCK

The Signal Processing Circuitry is shown on page 4 of the R/W schematic. A detailed block diagram of this section is given in Figure 12. The differential input signal DX-DY is applied to an AGC amplifier which determines the output signal level. The level-controlled output is passed through a low pass filter to remove out of band noise. This signal is differentiated by a tuned amplifier to recover the zero crossings information. The signal is limited to convert it to TTL compatible levels at output RDA.

The analog signal at the output of the tuned amplifier is passed through a full wave average detector and applied to an integrator which sets the AGC control voltage such that the full wave average of SIGH-SIGL is equal to a reference voltage.

The AGC amplifier circuit is shown in Figure 13. The amplifier is a differential cascode amplifier whose gain is set by current rationing in the cascode transistors. Since Figure 13 looks a little intimidating, let's look at it a little at a time.

Capacitors C183 and C184 have very low impedance at the signal frequencies of interest. For the moment, let's consider them to be zero ohms at the signal frequencies. In this case, the bases of the cascode transistors, U181, are AC grounds. The small signal differential mode AC model of the amplifier then looks like Figure 14. In this figure, all capacitances are omitted since, at the frequencies of interest, their impedances are very low. Also, R154 is redrawn as a series connection of two B1 ohm resistors.

VII. SIGNAL PROCESSING BLOCK (Continued)

When DX-DY is a differential signal, we can use the symmetry of the circuit in Figure 14 to analyze the amplifier since we know that the small signal collector current ic1 is equal to

$$ic1 = -ic2$$

Furthermore,

$$ic1 = ic3 + ic4$$

and

$$ic1 \sim dVi/81 \text{ Ohms}$$

The output of the amplifier is

$$dVo = -(ic3)(237) \text{ Ohm}$$

Figure 15 shows the small signal model for determining ic3 and ic4 given ic1. The amount of collector current drawn by each of transistors Q3 and Q4 will be determined by the ratio of the base currents in each transistor. This ratio is given by

$$ib3 = (ic1/B)\ hie4/(hie3 + hie4), \text{ NOTE: } B = \text{Beta}$$

$$ib4 = (ic1/B)\ hie3/(hie3 + hie4)$$

so

$$ib3/ib4 = hie4/hie3$$

VII. SIGNAL PROCESSING BLOCK (Continued)

The parameter hie of a bipolar transistor is determined by the bias conditions. If I/b is the base bias current

then

$$hie = Vt/(B*Ib)$$

where Vt = 26 * 10E-3 at room temperature.

Therefore,

$$ib3/ib4 = [Vt /(B*Ib4)] * [(B*Ib3)/ Vt] = Ib3/Ib4$$

or

$$ib3 = [(ic1/B)] * [(Ib3/Ib3 + Ib4)]$$

so

$$\boxed{ic3 = B*ib3 = [Ib3/(Ib3 + Ib4)] * [ic1]}$$

The output of the AGC amplifier is then

$$
\begin{aligned}
dVo &= (ic3) * (237) \text{ ohms} \\
&= [Ib3/(Ib3 + Ib4)] * (ic1) * (237) \text{ ohms} \\
&= [Ib3/(Ib3 + Ib4)] * [(dVi)/81\text{ohms}] * (237\text{ohms})
\end{aligned}
$$

The amplifier gain is dVo/dVi, which is

$$Avs = (237/81) * (Ib3)/(Ib3 + Ib4)$$

VII. SIGNAL PROCESSING BLOCK (Continued)

Now, the base currents, Ib3 and Ib4, of the cascode transistors are DC bias conditions which depend upon the value of the AGC control voltage. As the AGC control voltage in Figure 13 changes, the ratio of Ib3 to Ib4 in each of the cascode transistor pairs will change.

For instance, if the AGC control voltage is 6 volts, then the base-emitter voltages of Q3 and Q4 are the same and to the degree allowed by the match of the transistors, Ib3 = Ib4. In this case, the gain becomes Av = [237/81] * (1/2) = 1.5

If the AGC control voltages increases, then the dc base-emitter voltage of Q4 becomes larger than that of Q3. Therefore, Ib4 > Ib3. In the limit where Ib4 >> Ib3, Av -> 0.

If the AGC control voltage drops below 6 volts, Ib3 > Ib4. In the limit where Ib3 >> Ib4, Av -> 0.

If the AGC control voltage drops below 6 volts, Ib3 > Ib3 > Ib4. In the limit where Ib3 >> Ib4, Av -> [237/81] = 2.9. Therefore, increasing the AGC control voltage decreases, the gain of the AGC amplifier, and decreasing the AGC control voltage increases the gain of the AGC amplifier.

VII. SIGNAL PROCESSING BLOCK (Continued)

C183 plays a very important role in the AGC amplifier since, without it, the AC ground assumption made in designing the amplifier is invalid. If C183 is bad, the effect will probably be that the amplifier circuit will oscillate at roughly 250 MHZ to 300 MHZ.

The low pass filter is shown in Figure 16. Also shown is the small signal model of the output stage of the AGC amplifier. Also shown is the tuned amplifier circuit.

The low pass filter is a simple ladder network applied to a differential input signal. It has a Bessel response with a 5 MHZ cutoff frequency. Notice that the filter response depends upon the output impedance of the AGC amplifier stage. If bypass capacitor C187 in the AGC amplifier is bad, the filter response will be upset.

The tuned amplifier stage has a gain at its resonant frequency of approximately 50. The resonant frequency is roughly 7 MHZ. The response of the tuned amplifier is a 2nd order Bessel response with a differentiator zero added.

The overall frequency response, in terms of a normalized input level, is given in Figure 17. In this figure, the magnitude scale is normalized, so only relative magnitudes are meaningful. The group delay scale is absolute.

VII. SIGNAL PROCESSING BLOCK (Continued)

The limiter circuit is shown in Figure 18. DC blocking capacitors C476 and C477 remove dc voltage levels established by other circuits. U4102 is a very fast comparator with TTL compatible outputs. Its main claim to fame is that the output skew a symmetry is guaranteed to be less than 2 nsec worst case. Since we are trying to locate the zero crossings of SIGH and SIGL as closely as possible, we need a very good zero crossing detector. The AM686 fits this need. It is superior to designs using the 8T20. It is a vast improvement over the LM361.

R479 and R483 supply a dc bias path for the input stage of U4102. R484 and R485 are chosen to minimize the slew rate of the device.

The full wave average detector and the reference voltage circuit are shown in Figure 19. When SIGH and SIGL are zero volts ac, the dc voltages in the circuit are as shown. The transistors are all part of U3101. The Q designators in Figure 19 are for discussion purposes only and do not correspond to Q designators on the PCA.

Q3 and Q5 are current sources which draw approximately 1 mA each. The matching of these bias currents improves the temperature tracking performance of Q1, Q2, and Q4.

Transistor Q4 is the voltage reference circuit. The output VREF is a dc voltage at roughly -1.5 volts. The voltage is determined by R353 and R349 and the base emitter drop across Q4. This base emitter drop matches and tracks the base emitter drops across Q1 and Q2.

VII. SIGNAL PROCESSING BLOCK (Continued)

Q1 and Q2 form a full wave rectifier, when SIGH > SIGL, Q1 turns on and Q2 turns off. The voltage at the emitter of Q1 is simply SIGH less one V/BE drop. When SIGH < SIGL, Q1 is off and Q2 turns on. The emitter voltage is then SIGL. Thus, at the emitters of Q1 and Q2 is developed a full wave rectified version of SIGH-SIGL. There is no "crossover distortion" because current source Q3 guarantees that either Q1 or Q2 will be on at all times.

The full wave rectified signal is filtered by R266 and C262 to detect the average value of this waveform. It is this average value that the AGC loop attempts to hold constant. Resistors R473 and R474 set a dc baseline for SIGH-SIGL which determines the peak to peak amplitude of SIGH-SIGL when the AGC is working properly.

The AGC loop integrator is shown in Figure 20. OpAmp U2101 is a standard integrator circuit. It is important that a low bandwidth opamp like the MC1458 be used because the signal V/AVG will contain small levels of high frequency ripple due to imperfect filtering by the F.W.A. detector. If a wider bandwidth op amp such as the Mc4558 is used, these high frequency elements will bleed through the device and appear on the AGC control voltage. This will cause distortion in the output of the AGC amplifier and will degrade the error rate.

Transistor Q199 and diode CR192 are voltage clamps which restrict the AGC control voltage range. CR192 limits AGC control to +7 volts maximum. Q199 limits AGC control to 5.5 volts minimum. This limiting is necessary to ensure that the AGC amplifier remains biased in the active region. Otherwise, during a seek, the AGC amplifier could be slammed on and off. This would create system noise and probably isn't good for the components.

VIII. TIMING RECOVERY BLOCK

The Timing Recovery and Separator circuits are shown on page 3 of the schematics. A detailed block diagram of the Timing Recovery Block is given in Figure 21.

During a write, the Data/Clock Mux selects the servo bit clock, P8-L. It also selects this clock during seeks or whenever an offtrack occurs. During a read operation, the Data/clock Mux selects the data signal, RDA.

The Edge Detector generates a pulse whenever it receives a change in the level of its input. This circuit is necessary because all information in an MFM-encoded signal is carried in the signal transitions. Therefore, we need to focus on the transitions to recover timing information.

The clock select logic determines which clocks will be applied to the phase lock loop's phase detector. The circuit has two operating modes, called Acquisition Mode and MFM mode.

Acquisition Mode is used during writes, seeks, and during the first 10 bytes of the VCO sync field during a read. The purpose of MFM mode is to process the VCO clock signal in such a way that the variations in the edges of the data signal caused by MFM encoding do not cause excessive jitter in the output of the VCO.

The phase/frequency detector puts out a voltage pulse whose width is proportional to the magnitude of the time difference between the negative-going edges of MFM-L and TRF-L. The polarity of this voltage pulse is positive if TRF-L leads MFM-L. The polarity is negative if TRF-L lags MFM-L.

VIII. TIMING RECOVERY BLOCK (Continued)

The loop filter provides compensation for the phase locked loop. Its characteristics set such loop parameters as acquisition time, noise bandwidth, and susceptibility to pattern-induced jitter.

The VCO is a square wave oscillator whose frequency of oscillation depends upon the magnitude of the control voltage output from the loop filter.

The R/W clock logic takes the basic timing information contained in the VCO output and uses it to generate the R/W bit clock.

The data/clock mux circuitry is shown in Figure 22. The select logic U552, U562, and U452 cause one of the two flipflops U581 to be preset. This will mask out the signal associated with that flop. The other flop will be in the cleared state and its associated signal passes through the mux. An example timing diagram is included in Figure 22.

This whole circuit is an overly fancy atavism which sprang from functions and capabilities we no longer include in the read/write board. The flipflops U581 no longer serve a real purpose. Yes, Virginia, it could be simplified. We just didn't catch it in time.

The Edge Detector is shown in Figure 23. This circuit is designed to generate a negative-going pulse each time input D/C has an edge. The width of the pulse is not important. The delay from positive edge to pulse out must equal the delay from negative edge to pulse out.

VIII. TIMING RECOVERY BLOCK (Continued)

On the rising edge of D/C, exclusive OR gate U561B clocks a 1 into flipflop U551. This propagates a one through U442, which in turn causes the output of U422 to fall. This falling signal is fed back through U452 and C429 to clear U551.

The falling edge of D/C causes the same behavior through the other flipflop. The exclusive-ORs U561 and flipflops U551 are closely matched so that no bias due to edge direction is introduced.

Inverters U452 and capacitor C429 serve to set the width of the output pulse by creating a short delay in the output feedback to U551. U422 is a 50-ohm line driver required for driving the load presented to the edge detector by the clock select logic.

A detailed block diagram of the Clock Select Logic is given in Figure 24. The mode is controlled by the 2-line-to-1-line mux, U511. When the mode control input is a "zero", the delayed signal MFMD and the output of the VCO Pulse Swallower are passed through. When the mode control is a "one", the delayed signal MFMD and the output of the divide by 2 counter are passed through.

The VCO divide by 2 counter sets the basic operating frequency of the VCO during acquisition mode. It is a simple toggle flipflop circuit.

VIII. TIMING RECOVERY BLOCK (Continued)

The VCO Pulse Swallower Circuit suppresses the timing reference output TRF-L when no data edge is present in MFMD. This is done to lessen the sensitivity of the phase locked loop's phase detector circuit to the modulation of MFMD caused by the data during a read. (Refer to Figure 9, CODE-L, for an example of how the edges of an MFM signal undergo pulse position modulation). The output DARM-H of the Pulse Swallower is a pulse which a high to low transition for each MFM data edge. This pulse is synchronized to the VCO clock, VCO-H, and is used to develop a phase reference by the R/W clock generator.

The 100 nsec. delay line, U521, is used to allow the VCO pulse swallower time to set up. In order for the timing recovery block to work properly, the amount of time delay used must be roughly 1/2 of a bit cell time. For the 7908, this is roughly 94 nsec. The additional 6 nsec allow some additional time for the Pulse Swallower to set up. The 100 nsec delay can <u>not</u> be shortened <u>or</u> lengthened by more than about +/- 6 nsec.

The VCO Pulse Swallower Circuit is shown in Figure 25. A negative-going edge on MFMD sets the first flipflop, U412A. Upon the next negative edge of VCO-H, VCOM is clocked thru to DARM. On the next rising edge of VCO-H, both flipflops U412 are reset. A timing diagram is shown in Figure 25. The phase locked loop circuitry establishes VCO-H such that the edges of DARM and VCOM line up with MFM-L as shown.

VIII. TIMING RECOVERY BLOCK (Continued)

If you should browse through the TTL data book sometime, you will find that the minimum pulse width applied to the clear input of a 74S112 is supposed to be 8 nsec. If the pulse applied to the clear input is less than this, the flipflop might oscillate.

If you browse further, you will see that the typical delay from clear to Q output of a 74S112 is 5 nsec. Furthermore, the typical delay through a 74S00 gate is 3 nsec. 3 + 5 = 8, so typically things will be just dandy with the Pulse Swallower circuit.

However, it is possible for a Schottky flipflop to clear in as little as 3 nsec. Further, it is possible for a 7400 to pass a signal in as little as 2 nsec. 2 + 3 is less than 8, so you might expect trouble. Sould you worry about it?

It turns out that if you examine the insides of a 74S112, you will find that feeding Q back to the clear input through a NAND gate is okay. The circuit is built in such a fashion that the flipflop will stabilize. Therefore, you don't have to worry about 3 + 2 < 8.

That would not be the case for a 74S112 circuit in which NOT Q is fed back to the CLEAR through an OR gate. That would be an unstable configuration and could oscillate even though the "logic" is apparently the same as our Pulse Swallower.

VIII. TIMING RECOVERY BLOCK (Continued)

By the way, the Pulse Swallower circuit is also used in the HP 13037 Formatter/Separator on the 13037-68028 board.

The Phase Detector circuit is shown in Figure 26. The phase detector triggers on the negative-going edges of MFM-L and TRF-L. The NOT Q outputs of flipflops U441 are applied to a difference amplifier to generate an output pulse whose width is proportional to the timing difference between MFM-L and TRF-L. When MFM-L leads TRF-L, a negative pulse is produced. This case is illustrated in the waveform diagrams on Figure 26. When TRF-L leads MFM-L, a positive pulse is produced.

Resistors R425, R427, R426, and R424 set the gain of the difference amplifier roughly Av = 0.1. This level of attenuation is required to prevent the op amp U351 from slew rate limiting. The 160 pf capacitors C438 and C442 are high frequency "snubs" which act to slow down the very fast pulses put out by the flipflops. This snubbing is necessary to prevent a non-linear behavior in op amps known as "rectification". Rectification is the phenomena whereby the base-emitter capacitance of the input differential amplifier conduct very high frequency pulses to the emitter of the differential amplifier. Since the input signal is differential mode, the positive-going pulse will cause one of the transistors to become cut off. [This is illustrated in Figure 27]. Cutting off these transistors cause the op amp's output to become amplitude modulated. A photo of this effect is also given in Figure 27.

VIII. TIMING RECOVERY BLOCK (Continued)

This amplitude modulation not only screws up the phase locked loop's frequency response, but also couples into the power supply and messes up the other circuits. It's a bad deal, and the capacitors prevent it.

Capacitor C318 is a compensation capacitor needed to stabilize the op amp so that it doesn't oscillate.

The phase detector gain from the input phase difference to phase error signal, 0e, is Kd = 0.05 volts/radian. The loop filter is shown in Figure 28. It is a standard active filter. The only things particularly noteworthy are the 5.6 pf capacitor C145, which stabilizes U261, and the compensation circuit composed of R327 and C420 which act as a snub for high frequency components which do appear at the output of the phase comparator.

The VCO circuit is a 74LS629 VCO chip. This chip has a very high gain, Kv = 21.10E6 rad/volt-sec. To desensitize the VCO to noise inputs, resistors R317, R236 and R325 and capacitor C433 are placed at the control input to scale down the effective sensitivity and filter out input noise. This network reduces the effective Kv to 7.1.10E6 rad/volt-sec. The 74LS629 can drive 12 schottky loads.

VIII. TIMING RECOVERY BLOCK (Continued)

The phase comparator, loop filter, and VCO form a phase locked loop. The loop is 2nd order with a cutoff frequency of 296 -10E3 rad/sec and a damping coefficient of 2.16.

The R/W clock logic is shown in Figure 29. This block is supposed to take the VCO output signal and use it to generate the read/write clocks, RWC-H and RWC-L. A timing diagram of this circuit's operation is shown in Figure 30.

During a read, DARM-H will initially clock on the MFM transitions caused by the all-zeroes pattern in the VCO synchronize field. Therefore, at the time when DECOD-H is asserted the DARM-H pulse is guaranteed to represent a "zero" bit to the separator.

As shown in Figure 30, when DECOD-H is asserted flipflops U432 begin to clock flipflop U482 such that the rising edge of RWC-H is coincident with the rising edge of DEDG-H. This guarantees that the RWC is properly phased in order for the separator to decode the MFM data properly.

IX. DATA SEPARATOR

To understand how to decode MFM data into NRZ data, refer to Figure 31. Figure 31 exhibits the relationship between NRZ data, MFM encoded data, and the derived edge pulse DEDG-H which is derived in the Timing Recovery Block.

As can be seen from Figure 31, transitions of DEDG-H which are due to "zero" data bits occur only at the boundaries between bit cells. Transitions of DEDG-H which are due to "one" data bits occur only in the center of the bit cells.

The VCO clock has one positive-going transition at each cell boundary. These transitions are given even numbers (0,2,4,6....) in Figure 31. The VCO clock also has one positive-going transition in the center of each bit cell. These transitions are given odd numbers (1,3,5,7,....) in Figure 31.

MFM decoding is very simple. If a positive-going edge of DEDG-H is coincident with an "odd" numbered VCO pulse, that edge was caused by a "one" data bit. Otherwise, the bit associated with that bit cell is a zero.

The R/W clock logic is constructed so that the falling edge of DTQ2 is caused only by even-numbered VCO pulses. The rising edge of DTQ2 occurs only during odd-numbered VCO pulses. Hence, DTQ2 makes the ideal clock for the separator.

IX. DATA SEPARATOR (Continued)

The separator is shown in Figure 32. If DEDG-H is high prior to an even-numbered VCO pulse, that means that DEDG-H went high during an odd-numbered VCO pulse. Therefore, on the next falling edge of DTQ2, DEDG-H will cause a "1" to clock into U492. Therefore, the "1" bits are properly decoded.

If DEDG-H is high prior to an odd-numbered VCO pulse, that means that DEDG-H must have gone high during an even-numbered VCO pulse. In this case, as can be seen in Figure 31, the next falling edge of DTQ2 will close a zero into U492.

Therefore, the Q output of U492A will be the desired NRZ data. Separation complete!

Well, then, what does the rest of that junk do? For starters, the separator needs to detect the Data Start Bit before it signals the DMA PCA that valid data is coming. That's what U492B does. Until the first "1" bit is detected, U492B has Q = 0 for its output. (That was caused when SOS-L went low). While in this state, it holds shift register U5101 to an all-all-zeroes state and disallows SOD-L, the start of data signal to the DMA, from being asserted.

After the first "1" bit is detected, U492B asserts SOD-L and allows the output data to pass through shift register U5101.

What does U5101 do? Well, for reasons best known to Peter Galen, the DMA PCA wants to see 3-zero bits clocked to it before it will be ready to receive data. U5101 just pads some garbage zeroes in front of the real data.

X. DISC MECHANISM INTERFACE

The last major block is the Disc Mechanism Interface. This section is shown on page 5 of the schematics.

The D.M.I. is really just a collection of different independent circuits. A "block diagram" is shown in Figure 33.

The Write Fault Comparator, U161, normally outputs +5 volts, when PSAF-H, from the disc mechanism, dips below 5.3 volts, that indicates that a write operation was bad and destroyed data on the disc. If PSAF-H dips below 5.3 volts, U161 asserts DWF-L.

The -4 volt supply is U341. It is just a high current dc amplifier. It's a straight-forward circuit except for one thing. C136 must be 0.01uf or so. If it's made too large (like 0.1 uf), Q233 will oscillate.

The +6 volts supply is Q627.

The Write Select Circuit is U421 and Q101. When reading, WSE-L is zero volts, then writing WSE-L is +3.5 volts.

The Head Select Circuitry is U421, U541, U552, and U512. U421 and U541 are level translators. U552 and U512 form an interlock which prevents CS0-L and CS1-L from being simultaneously asserted.

X. DISC MECHANISM INTERFACE (Continued)

The last circuit is the Write Current Circuit. This circuit is shown in Figure 34. Q221 and Q222, which are part of the write current circuit, are omitted from this drawing. Their role will be explained shortly.

U341 and Q226 form a constant current source that draws roughly 45 mA. Q225 is a current switch. When doing a write, open-collector comparators U321 have high impedance outputs. Resistor R113 then turns Q225 off, and all of Q226's current is drawn from the preamplifier chips located in the disc mechanism. This current is drawn through CR304.

When Master Resèt is asserted or when WRG-L is de-asserted (ie, when we are reading), one of comparators U321 clamps its output voltage to -12 volts. This saturates Q225, and all of the current required by Q226 is supplied thru Q225. No current is drawn through CR304.

If transistor Q225 is bad, this will sometimes appear as a drive fault when trying to write to the disc. What happens is that instead of a nice square wave pulse at J2-25 of about -3 volts, you will see a very short voltage pulse at WRMA which appears to have an oscillation riding in it. (See Figure 35). If this happens, Q225 is probably bad.

U421, Q222, and Q221 are current-level switches. When WC1-GH is asserted, U421 turns on Q222 which dumps roughly 8 mA of current into R223 and R224. U341 then acts to reduce the current drawn by Q226 by this amount. WC2-H causes similar action by Q221. By controlling WC1 and WC2, the microprocessor can change write current levels at different points on the disc.

ENGINEERING RESPONSIBILITY SEPIA

A - 07908 - 60205 - 4

0	1	2	3	4		6		8	9		11	12	14	15
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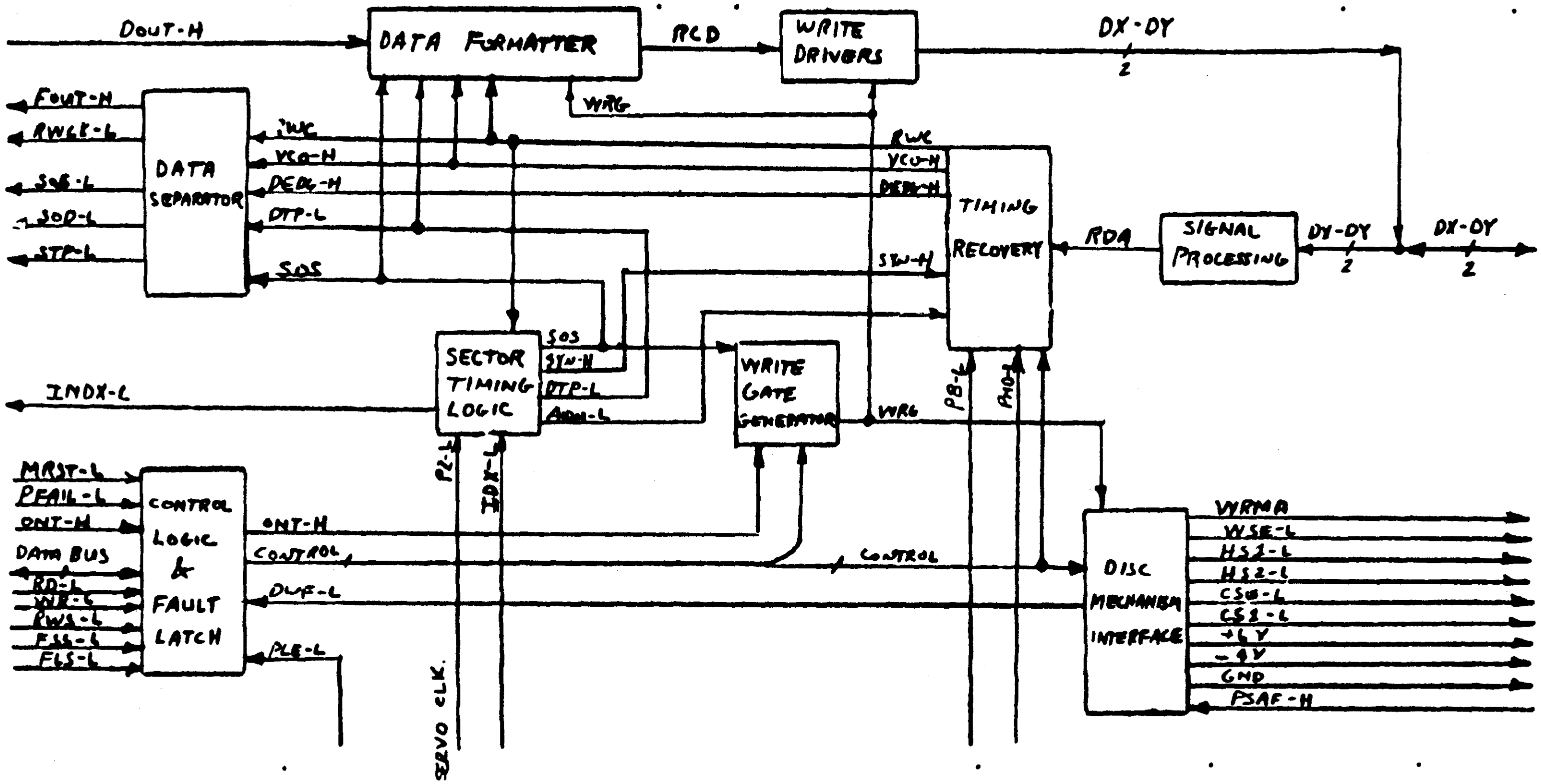
45	46	61	63											

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

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SUPERSEDES DWG.

TITLE: FIGURE 1
READ/WRITE PCA
BLOCK DIAGRAM

HEWLETT PACKARD

NEXT ASSEMBLY

FINISH | SCALE

PART NUMBER
A - 07908 - 60205 - 4

STOCK NO. 9280-0405 PRINTED ON DIEPO. NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

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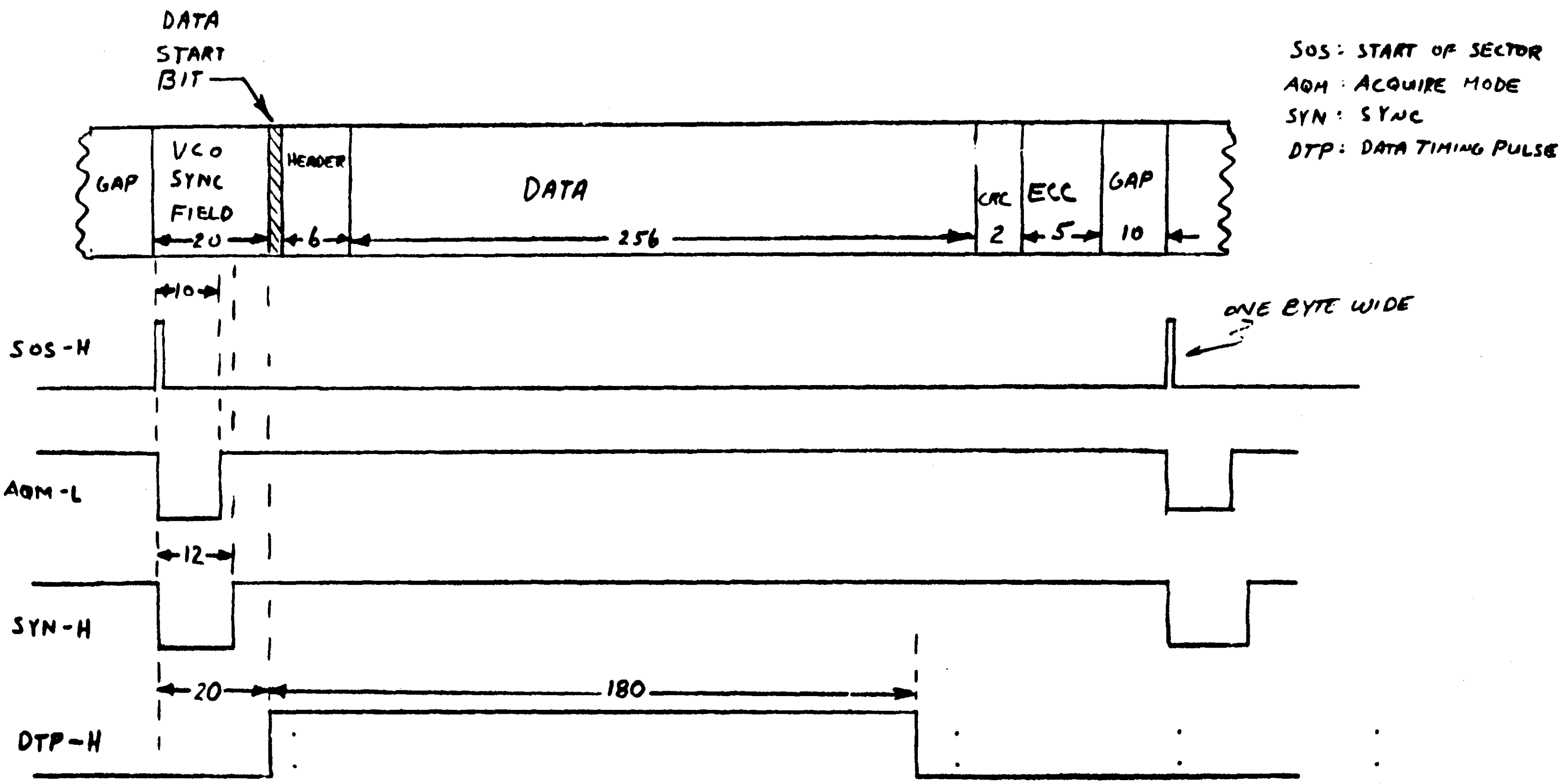
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A - 07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
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TITLE: FIGURE 2
7908 SECTOR FORMAT

NEXT ASSEMBLY

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PART NUMBER
A - 07908 - 60205 - 4

STOCK NO 9280-0405 PRINTED ON DIEPO NC 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY | SEPIA

A- 07908 - 60205 - 4

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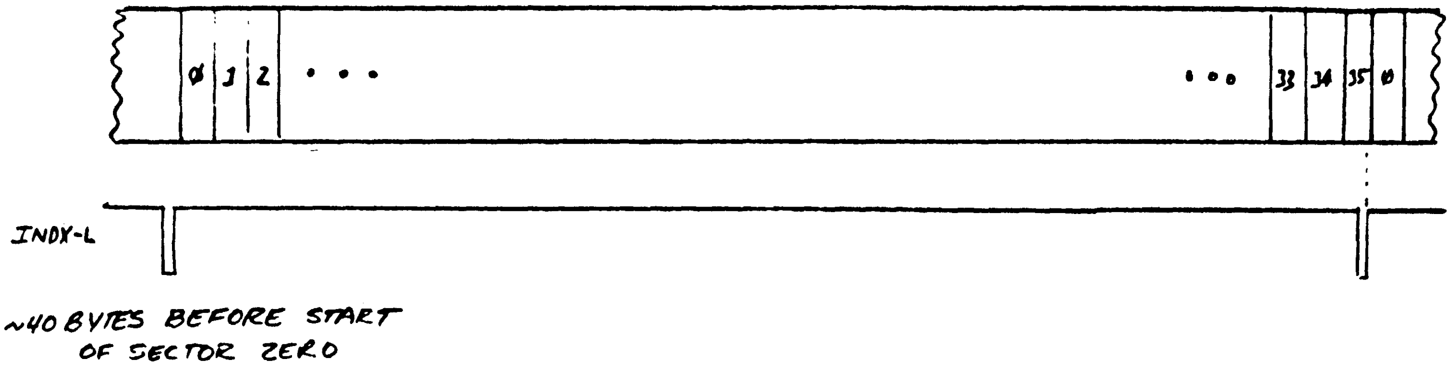
45	46	61	63											

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
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TITLE: FIGURE 3
7908 TRACK FORMAT

NEXT ASSEMBLY

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PART NUMBER
A - 07908 - 60205 - 4

STOCK NO 9280-0885 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

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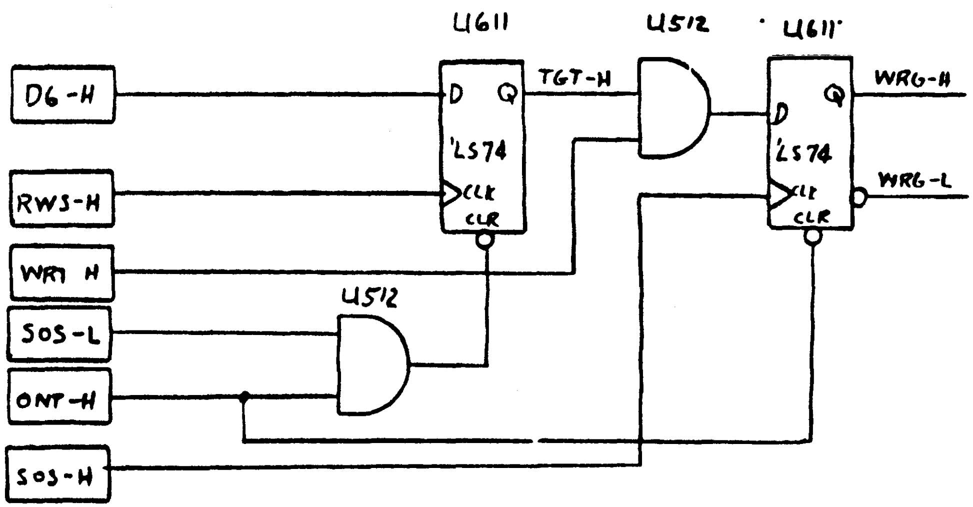
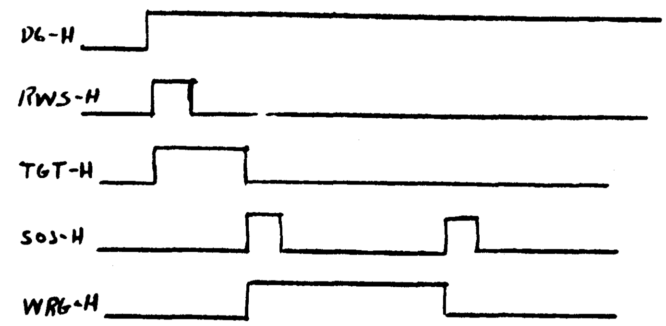
45	46	61	63								

A-07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE





ONT-H = "1" , WRT-H = "1"

IF ONT-H = "0" , WRG-H = "0"
ELSE WRG-H = TGT-H AND WRT-H AFTER SOS-H ↑

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

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SUPERSEDES DWG.

FIGURE 4
WRITE GATE GENERATOR
TITLE

NEXT ASSEMBLY
FINISH | SCALE

HEWLETT PACKARD

PART NUMBER
A - 07908 - 60205 - 4

STOCK NO 9280-0405 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

A - 07908 - 60205 - 4

H2-L	H1-L	EN1-H	ENØ-H	HEAD
1	1	Ø	1	Ø
1	Ø	Ø	1	1
1	1	1	Ø	2
1	Ø	1	Ø	3
Ø	1	1	Ø	4

ALL OTHER COMBINATIONS ARE ILLEGAL

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

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TITLE: FIGURE 5 HEAD SELECT TABLE

HEWLETT PACKARD

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ENGINEERING RESPONSIBILITY SEPIA

A-07908 60205 -4

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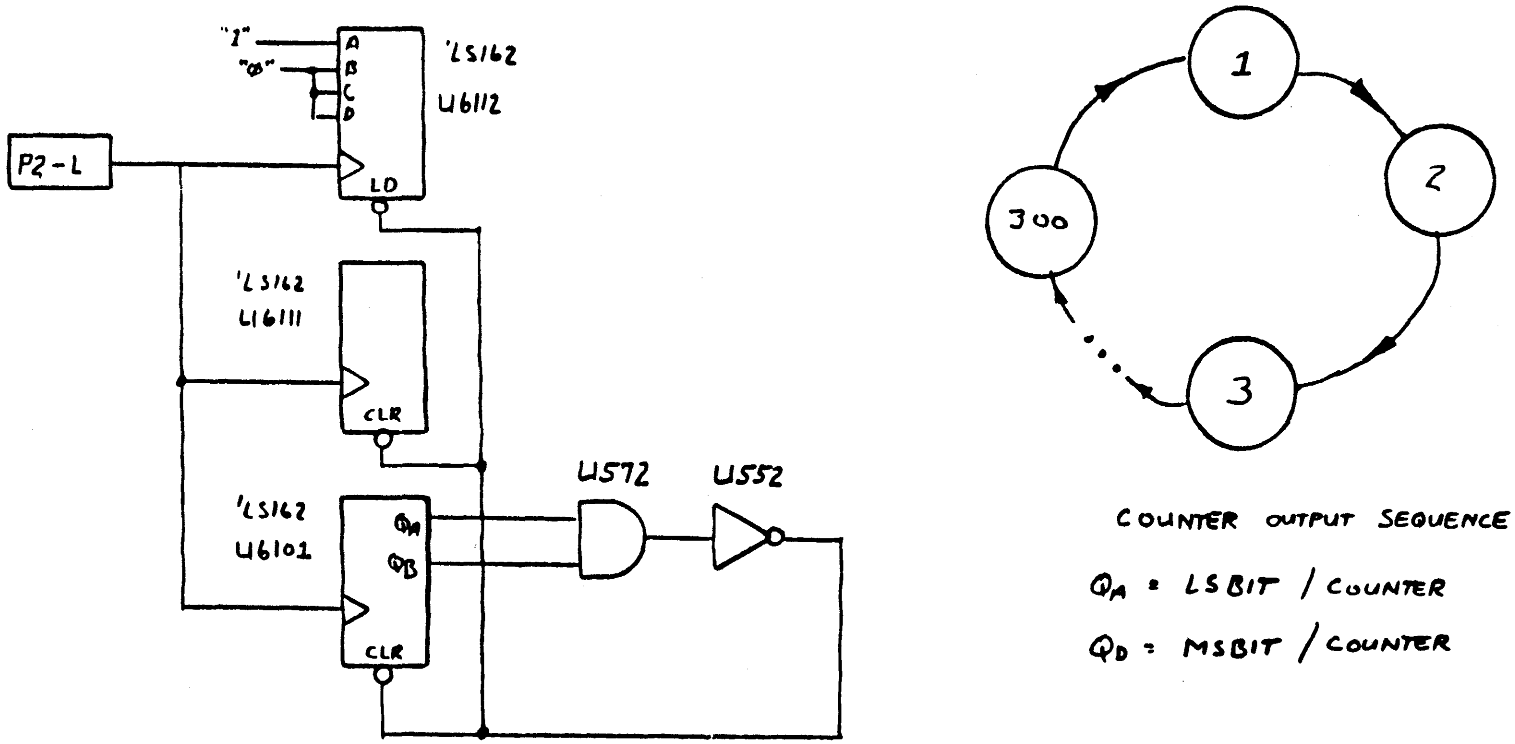
45	46	61	63											

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

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SUPERSEDES DWG.

TITLE: FIGURE 6
SIMPLIFIED SECTOR TIMING COUNTER

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

PART NUMBER
A - 07908 - 60205 - 4

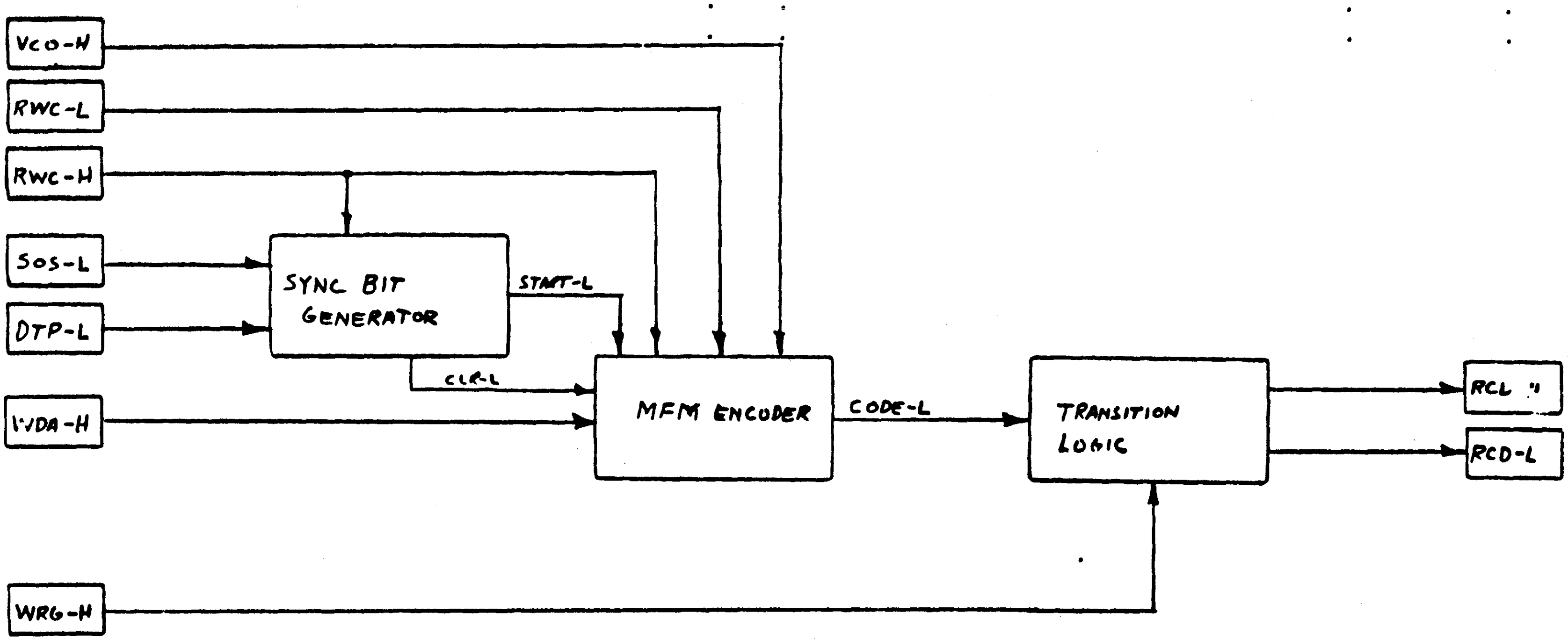
STOCK NO 9280-0485 PRINTED ON DIEPO NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A-07908 · 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY | DATE 810305

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

FIGURE 7

FORMATTER BLOCK DIAGRAM

TITLE

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

PART NUMBER

A - 07908 - 60205 -4

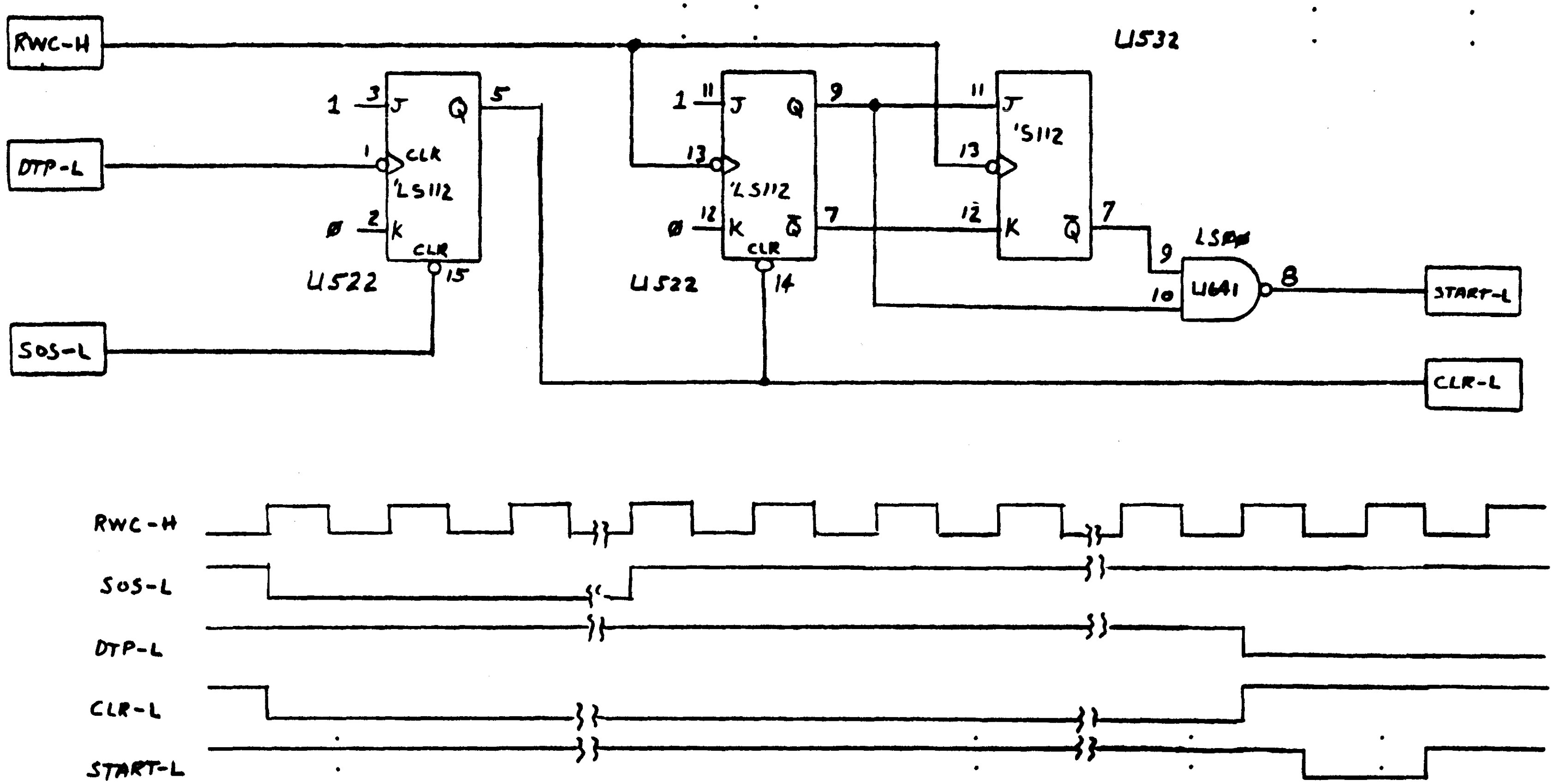
STOCK NO 9200-0405 PRINTED ON DIEPO. NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY   SEPIA

0	1	2	3	4	5	6	8	9	10	11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63										

A- 07908 - 60205

SYM	REVISIONS	APPROVED	DATE



UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L PART NO.	MAT'L DWG. NO.	MAT'L SPEC.

DRAWN BY — DATE 810305

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 8 SYNC BIT GENERATOR

NEXT ASSEMBLY

FINISH

SCALE

HEWLETT PACKARD

PART NUMBER A - 07908 - 60205 - 4

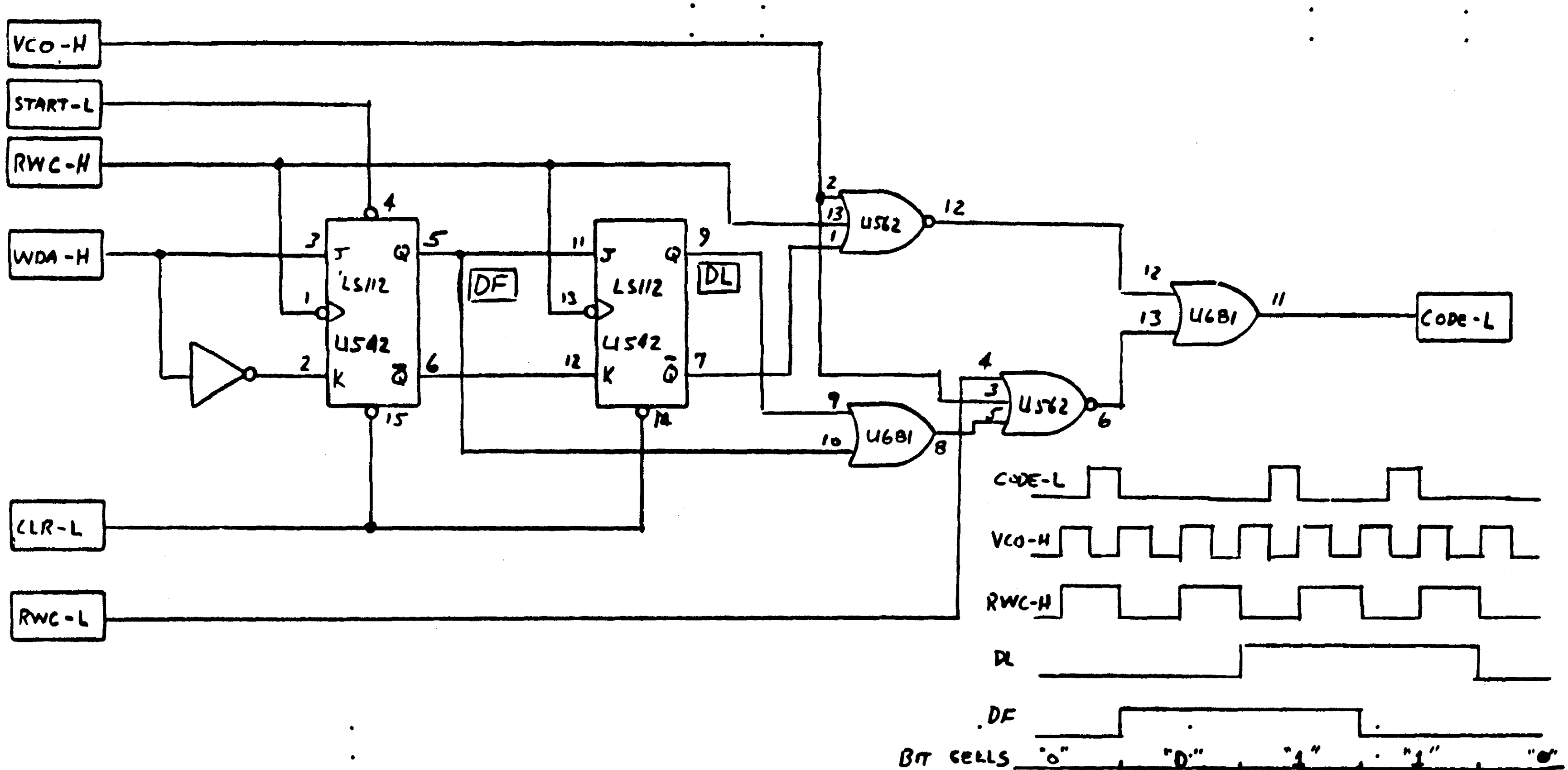
STOCK NO 9280-0685 PRINTED ON DIEPO NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A - 07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810313

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 9 MFM ENCODER

NEXT ASSEMBLY

FINISH — SCALE

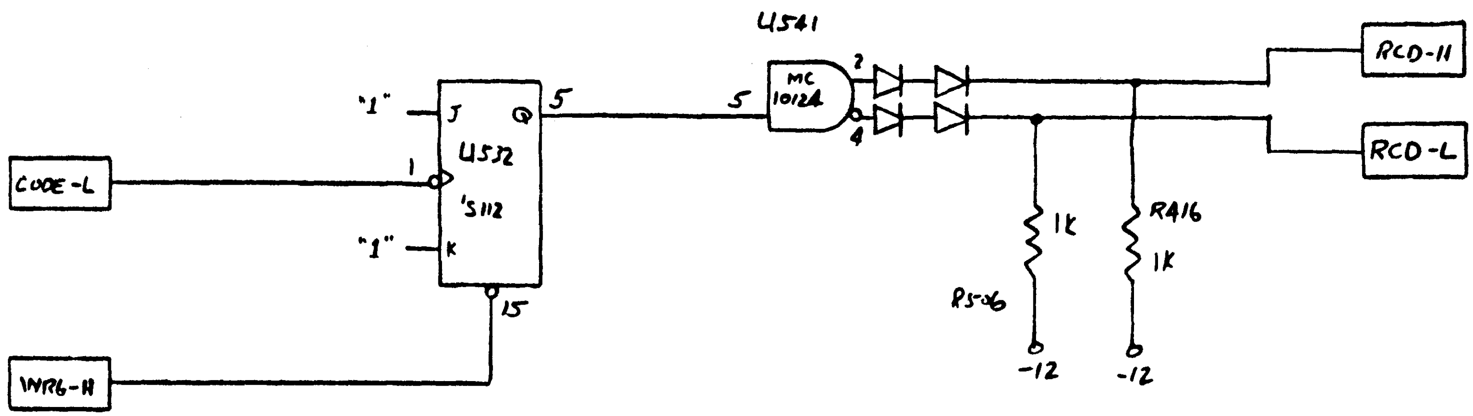
HEWLETT PACKARD

PART NUMBER A - 07908 - 60205 - 4

STOCK NO 9280-0485 PRINTED ON DIEPO. NO. 1020 MM CLEARPRINT FADEOUT

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

SYM	REVISIONS	APPROVED	DATE



NOTE : ① U532 MUST BE A SCHOTTKY PART FOR BEST ERROR RATE PERFORMANCE.

② SOME 74S112 DEVICES HAVE A TEMPERATURE SENSITIVE FAILURE MODE IN WHICH THE OUTPUT SWITCHING TIMES DROP OUT OF SPEC. IF THIS HAPPENS TO U532, THE SYMPTOM WILL BE THAT THE DRIVE WILL EXPERIENCE AN INCREASE IN THE NUMBER OF HARD ERRORS. THE ERRORS WILL BE MADE DURING WRITES. THE DRIVE WILL BE ABLE TO READ A TRACK BEFORE WRITING, BUT NOT AFTER.

ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810213

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 10 TRANSITION LOGIC

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

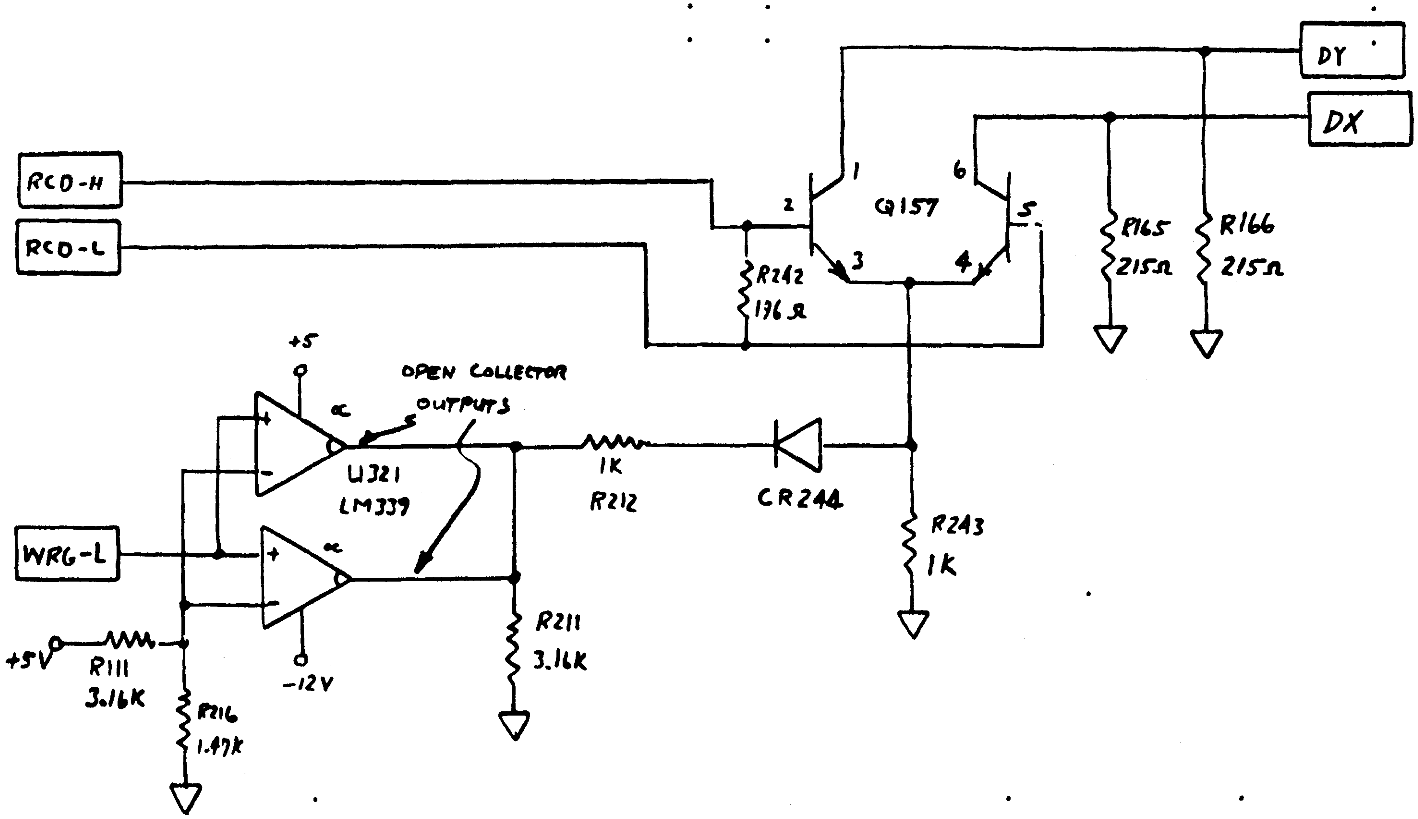
PART NUMBER A-07908 - 60205 -4

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	41
45	46	61	63											

A- 07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY | DATE 810316

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 11 WRITE DRIVERS

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

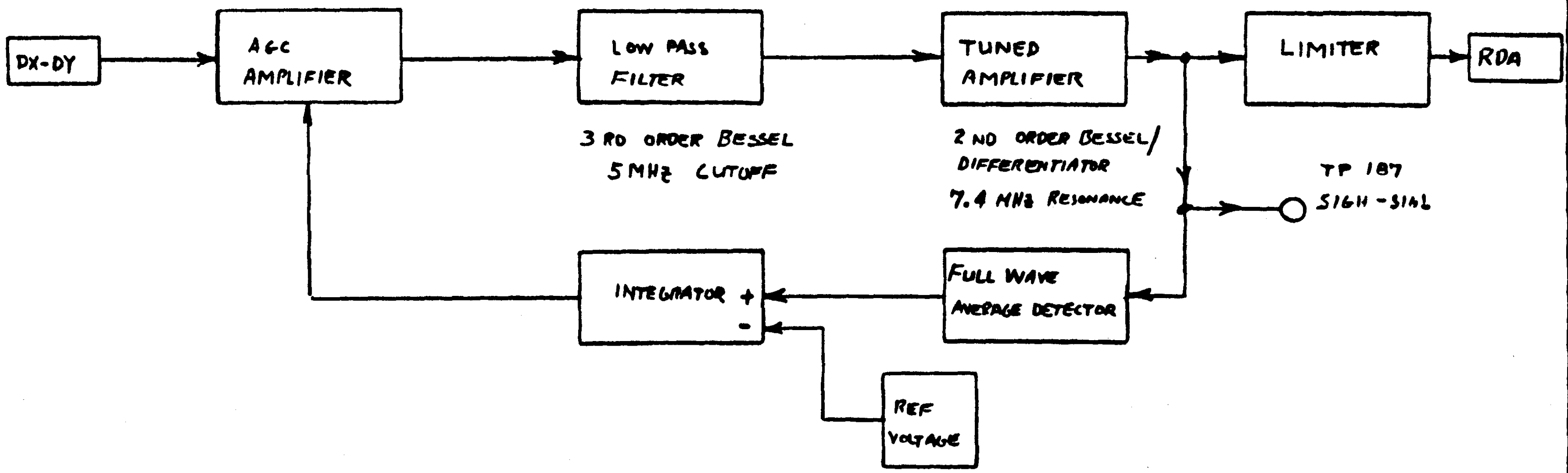
PART NUMBER A - 07908 - 60205 - 4

STOCK NO 9200-0603 PRINTED ON DIEPO. NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY | DATE 810316

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 12
DETAILED SIGNAL PROCESSING BLOCK DIAGRAM

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

PART NUMBER
A - 07908 - 60205 - 4

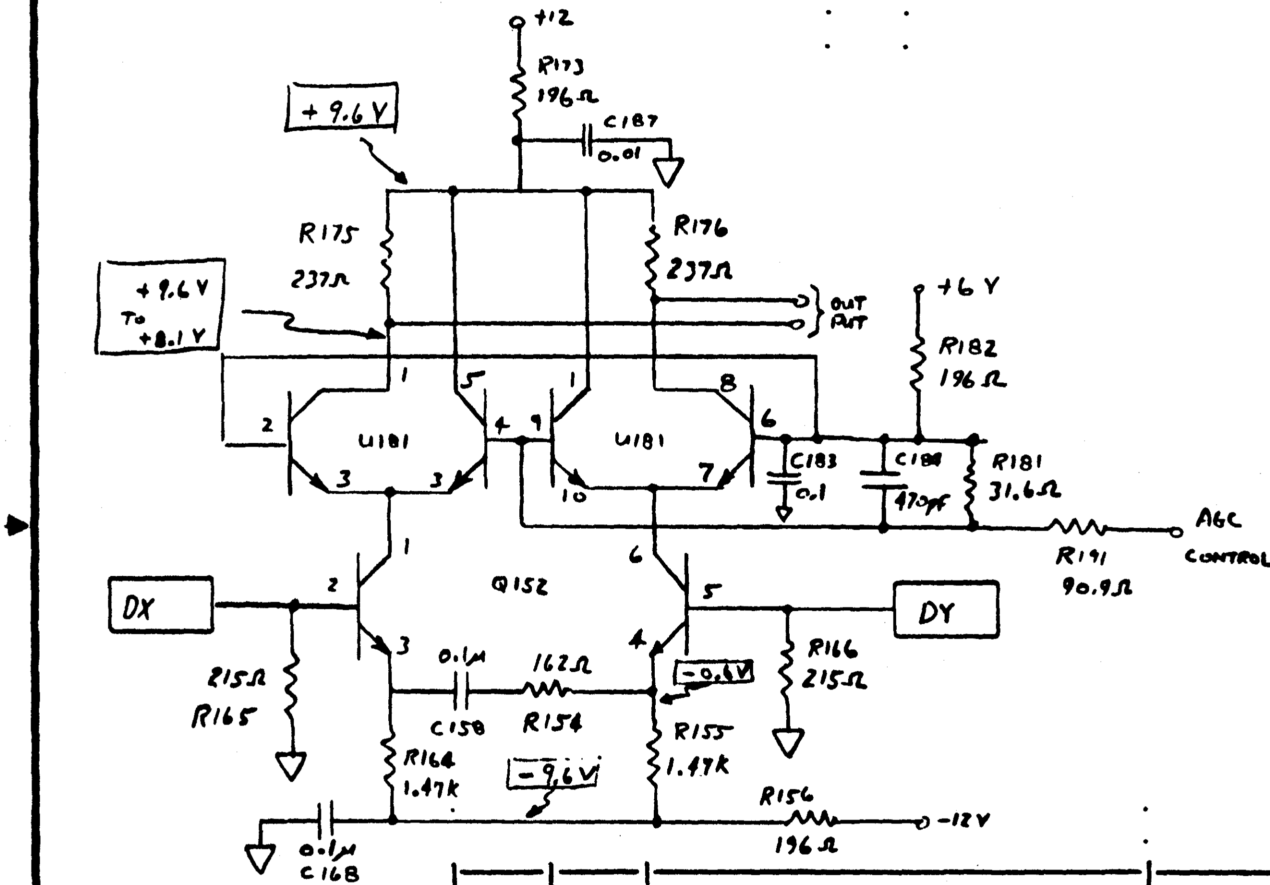
STOCK NO 9280-0405 PRINTED ON DIEPO. NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A-07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810316

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 13 AGC AMPLIFIER

NEXT ASSEMBLY

FINISH — SCALE

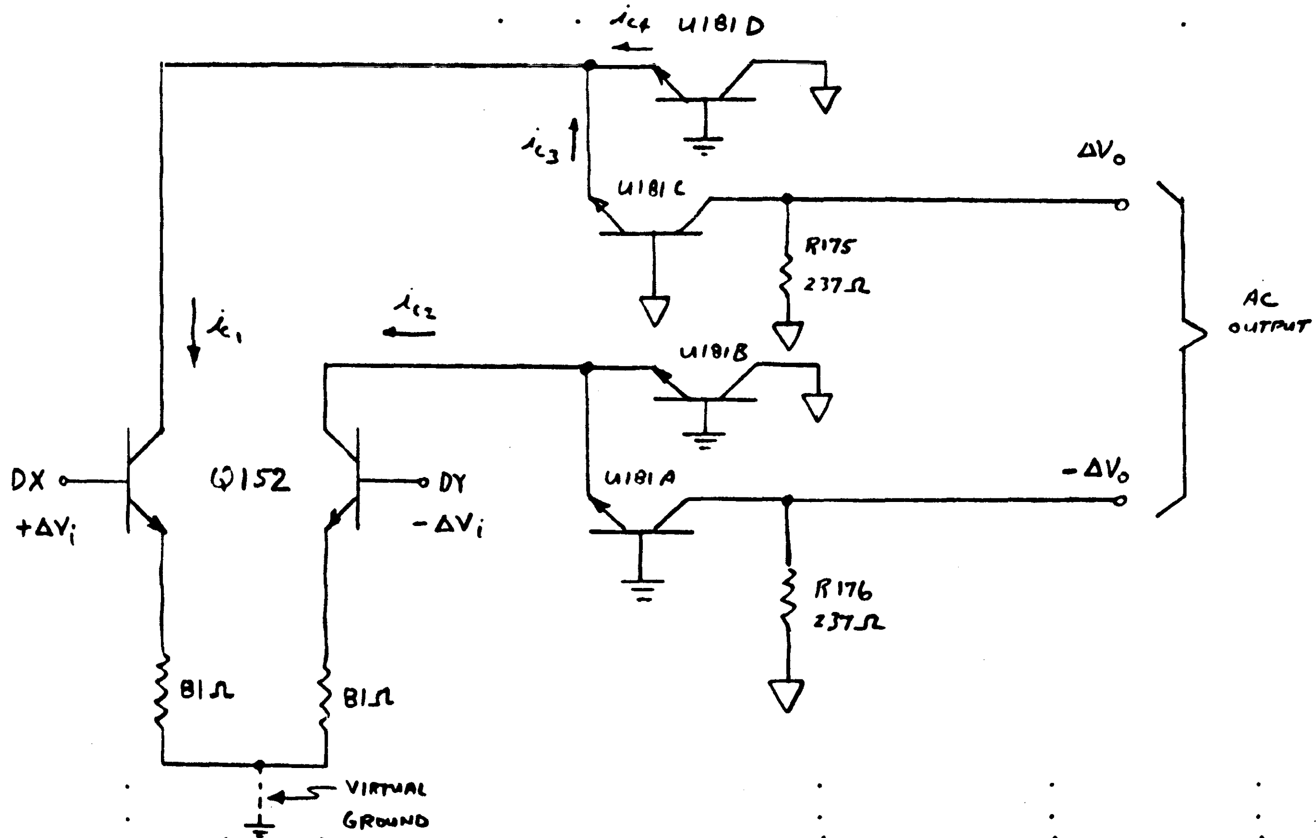
HEWLETT PACKARD

PART NUMBER: A - 07908 - 60205 - 4

STOCK NO. 9280-0405 PRINTED ON DIEPO NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY	SEPIA	A-07908-60205-4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810316

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 14 — AC MODEL OF AGC AMPLIFIER

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

PART NUMBER A-07908-60205-4

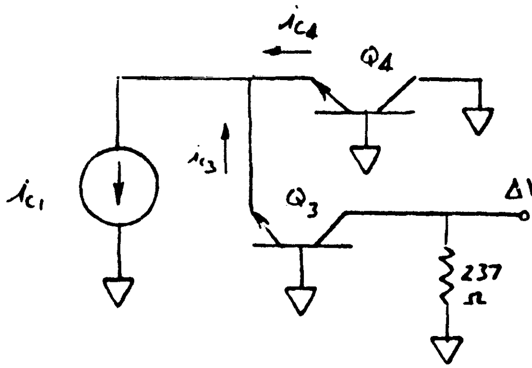
STOCK NO 9280-0485 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

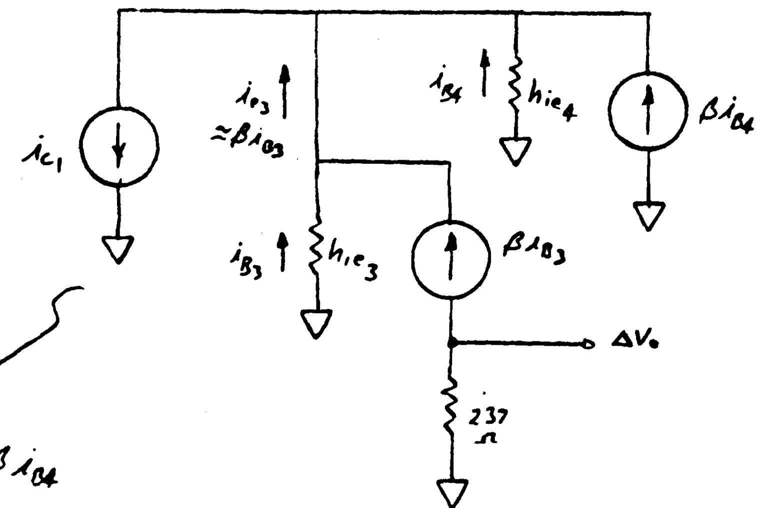
A-07908 - 60205 - 4

ENGINEERING RESPONSIBILITY | SEPIA

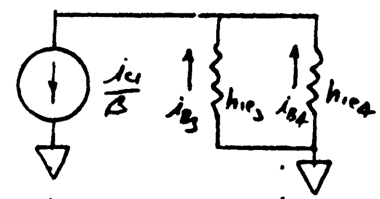
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

SYM	REVISIONS	APPROVED	DATE





$$i_{C_1} \approx \beta i_{B_3} + \beta i_{B_4}$$
$$= \beta (i_{B_3} + i_{B_4})$$



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY | 810316 DATE

ENGINEER | 810316

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 15 SMALL SIGNAL MODEL OF CASCODE AMPLIFIER

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

PART NUMBER A-07908 - 60205 -4

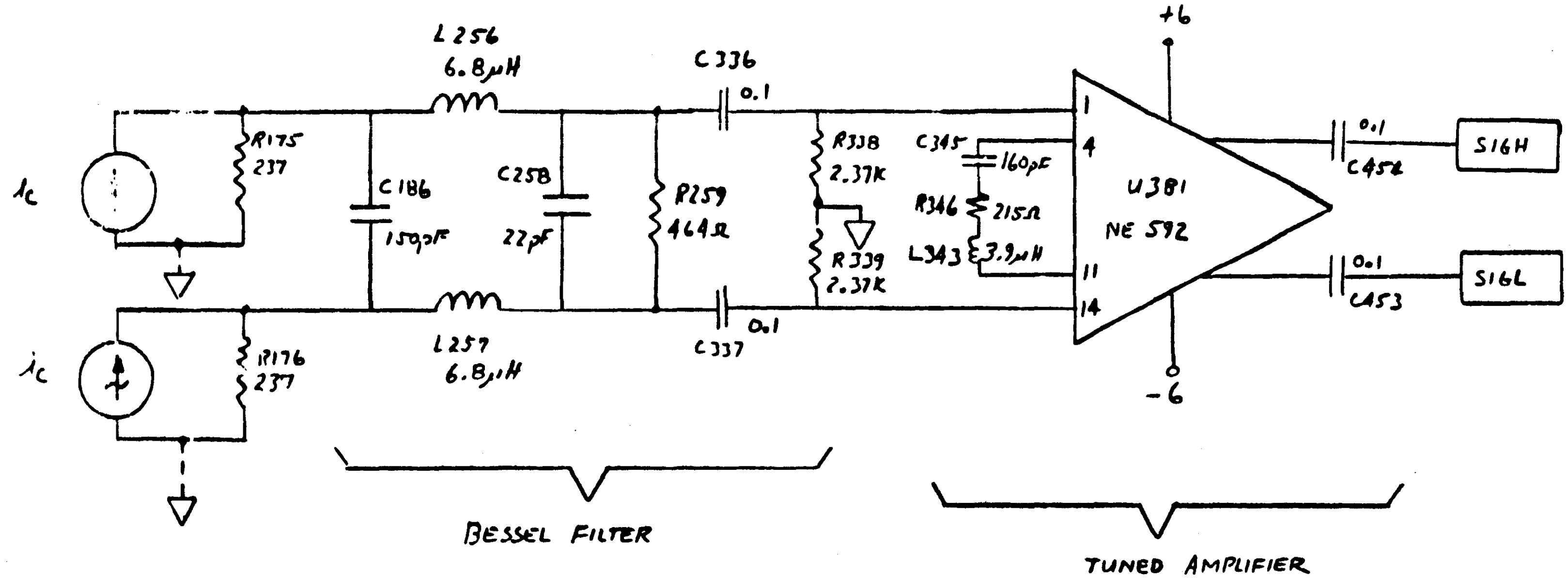
STOCK NO 9280-0485 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9	11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A-07908 - 60205 -4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810316

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 16
FILTER / DIFFERENTIATOR

NEXT ASSEMBLY

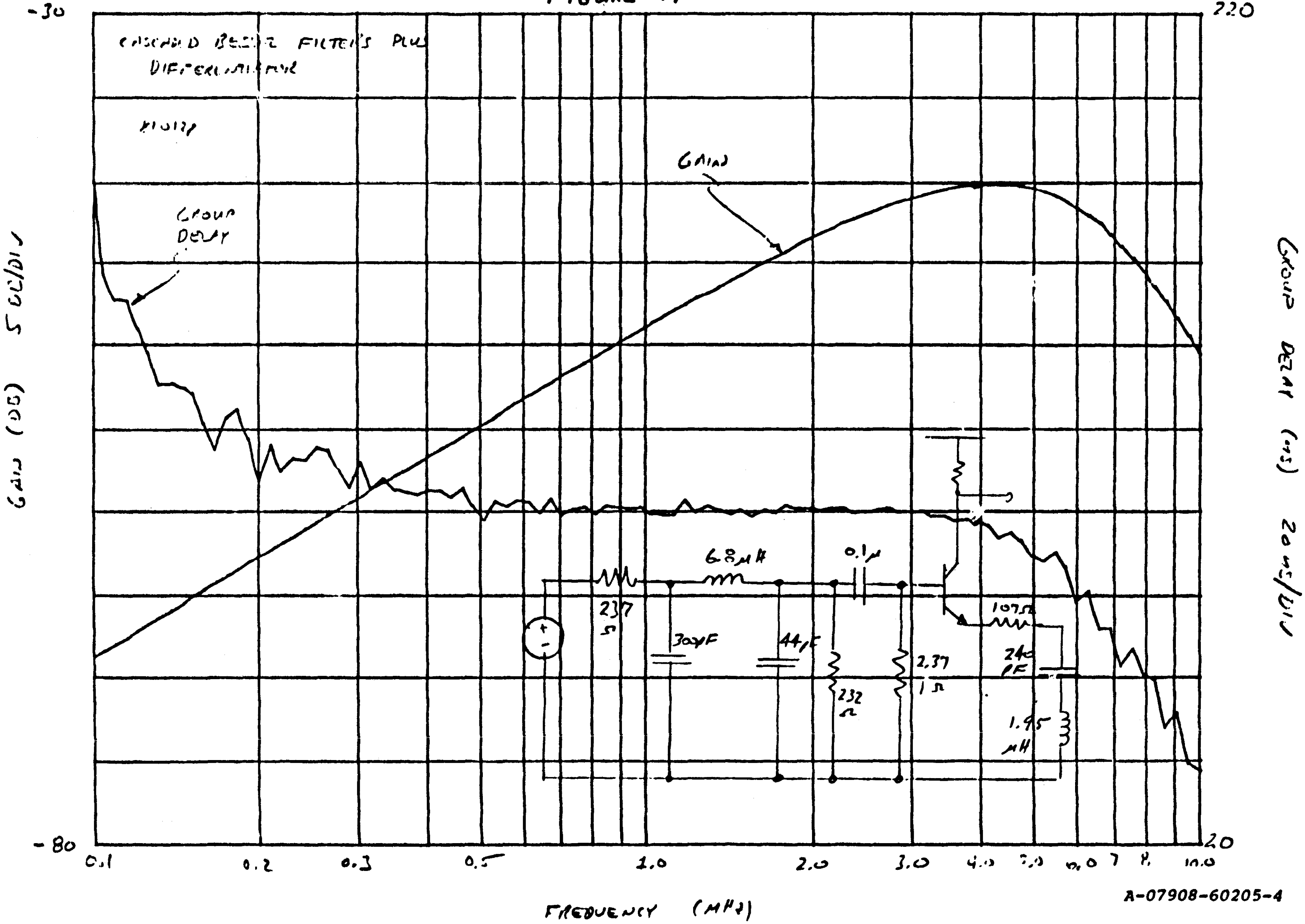
FINISH — SCALE

HEWLETT PACKARD

PART NUMBER
A - 07908 - 60205 -4

STOCK NO 9280-0605 PRINTED ON DIEPO. NO. 1020 MM CLEARPRINT FADEOUT

FIGURE 17

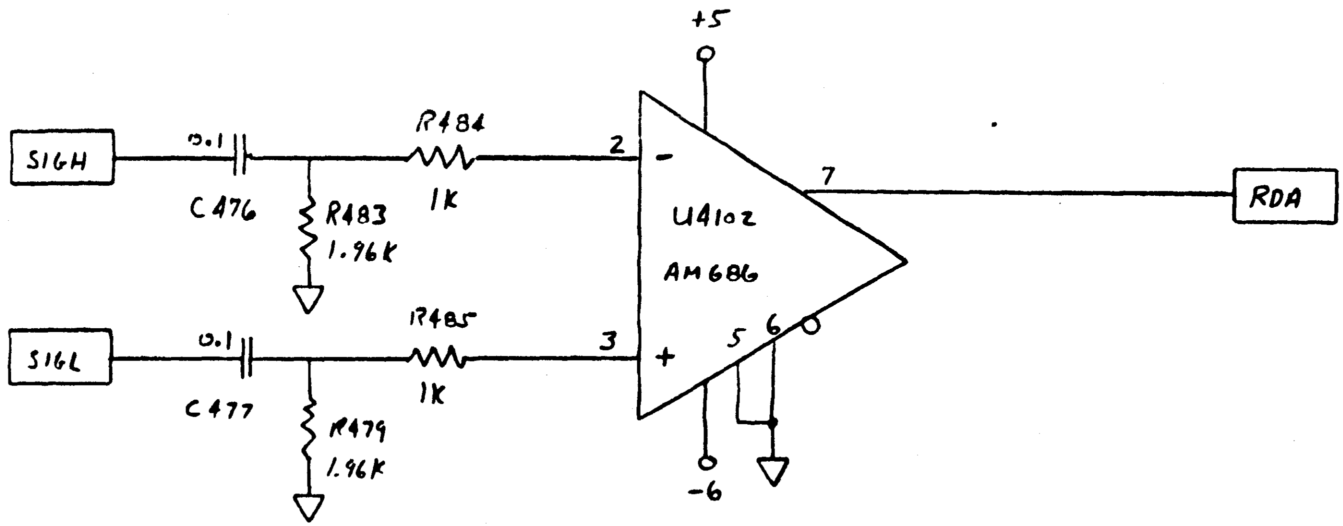

-30
220
CASCADED BESSEL FILTERS PLUS DIFFERENTIATOR
GAIN
GROUP DELAY
GAIN (DB) 5 DB/DIV
GROUP DELAY (NS) 20 NS/DIV
6.8 μH
0.1 μ
237 Ω
300 pF
44 pF
232 Ω
237 Ω
107 Ω
240 pF
1.95 μH
-80
20
0.1
0.2
0.3
0.5
1.0
2.0
3.0
4.0
5.0
6.0
7
8
10.0
FREQUENCY (MHz)

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A - 07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810316

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 18 LIMITER CIRCUIT

NEXT ASSEMBLY

FINISH

SCALE

HEWLETT PACKARD

PART NUMBER A - 07908 - 60205 - 4

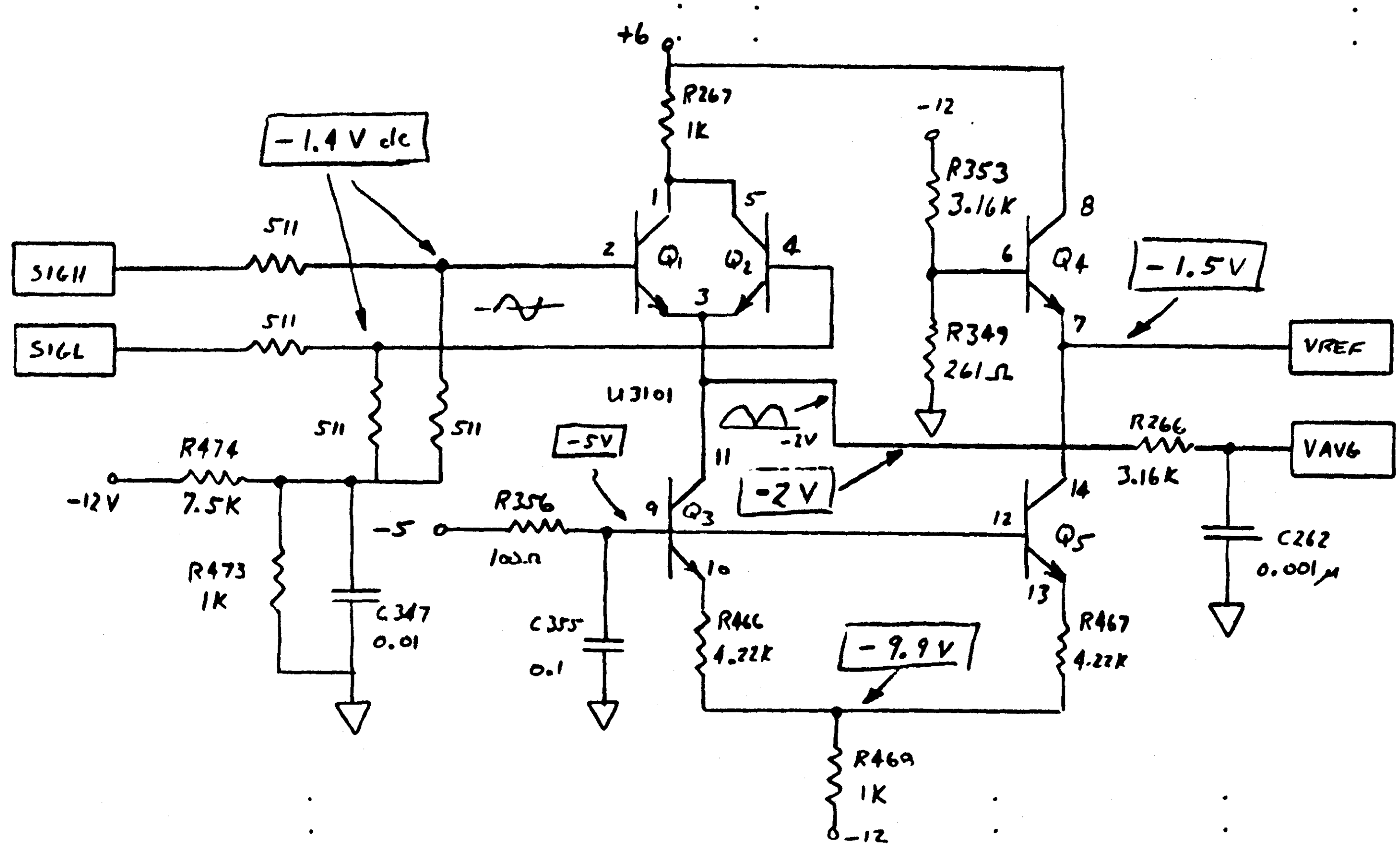
STOCK NO 9 00-0005 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY | SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A-07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD 608

DO NOT SCALE THIS DRAWING

DRAWN BY | DATE 810316

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 19
F.W.A. DETECTOR & VOLTAGE REFERENCE

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

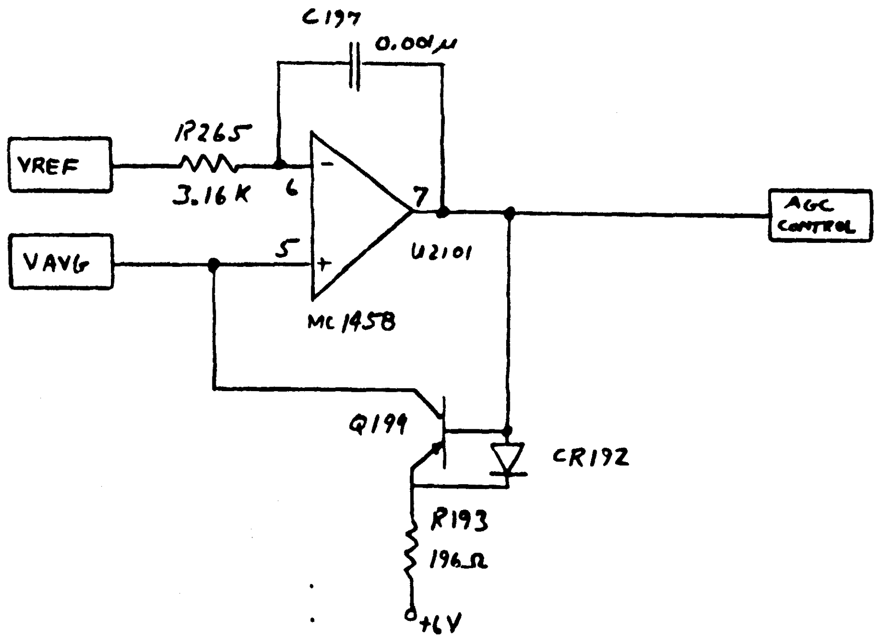
PART NUMBER
A - 07908 - 60205 - 4

STOCK NO. 9280-0405 PRINTED ON DIEPO NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	I	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810317

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 20 AGC LOOP INTEGRATOR

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

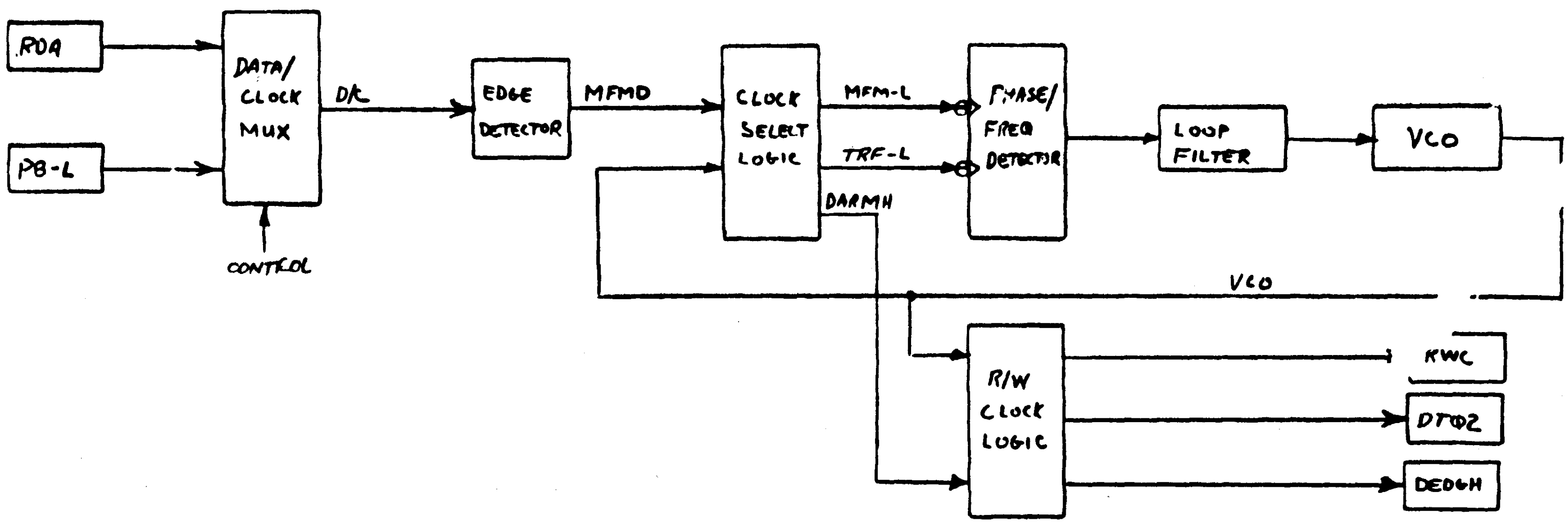
PART NUMBER A - 07908 - 60205 - 4

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A-07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY | DATE 810317

ENGINEERING

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 21 TIMING RECOVERY DETAILED BLOCK DIAGRAM

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

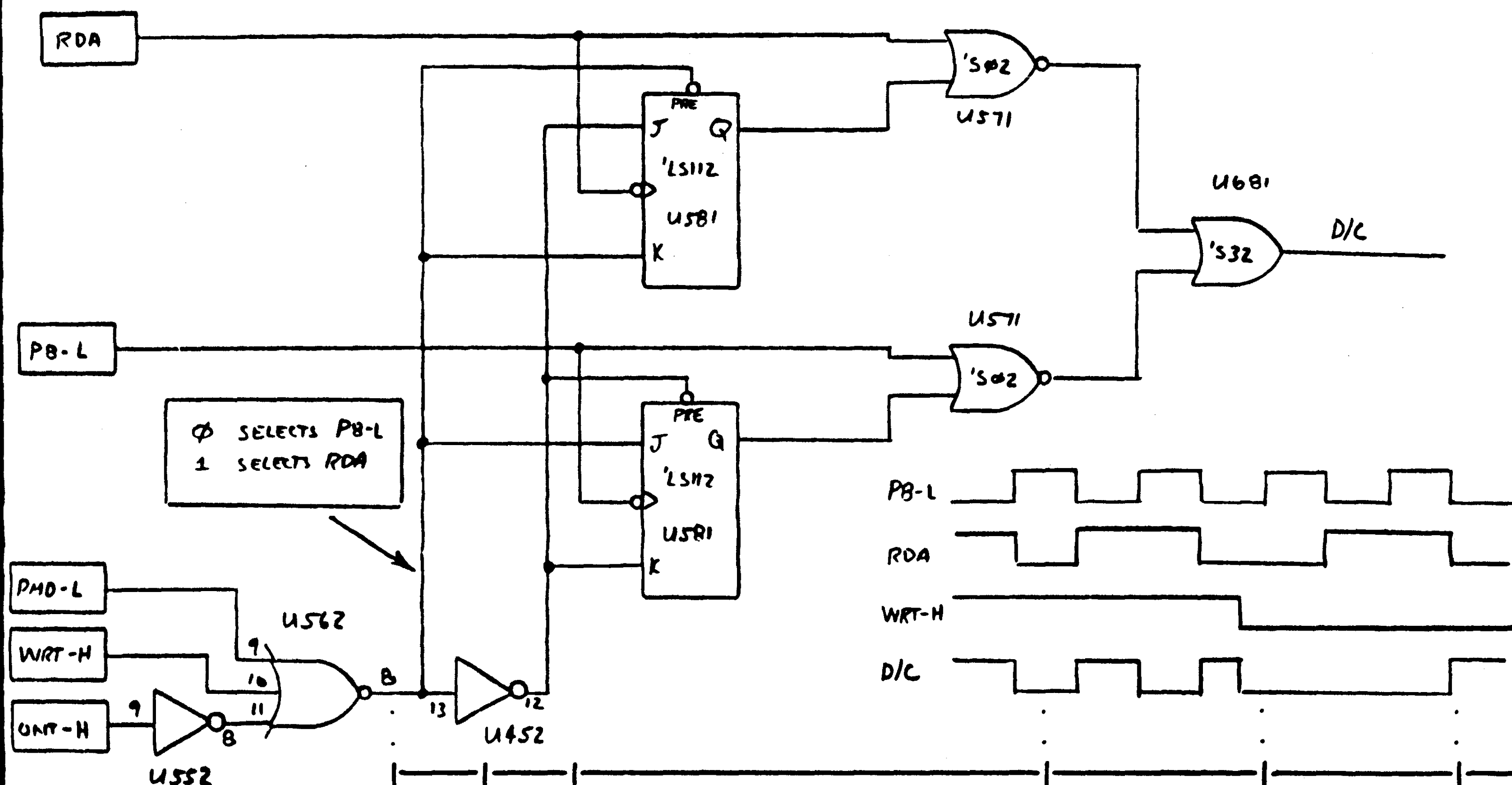
PART NUMBER A - 07908 - 60205 - 4

STOCK NO 9280-0495 PRINTED ON DIEPO. NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY	SEPIA	A - 07908 - 60205

0		2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810317

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 22 DATA / CLOCK MUX

NEXT ASSEMBLY

FINISH

SCALE

HEWLETT PACKARD

PART NUMBER: A - 07908 - 60205 - 4

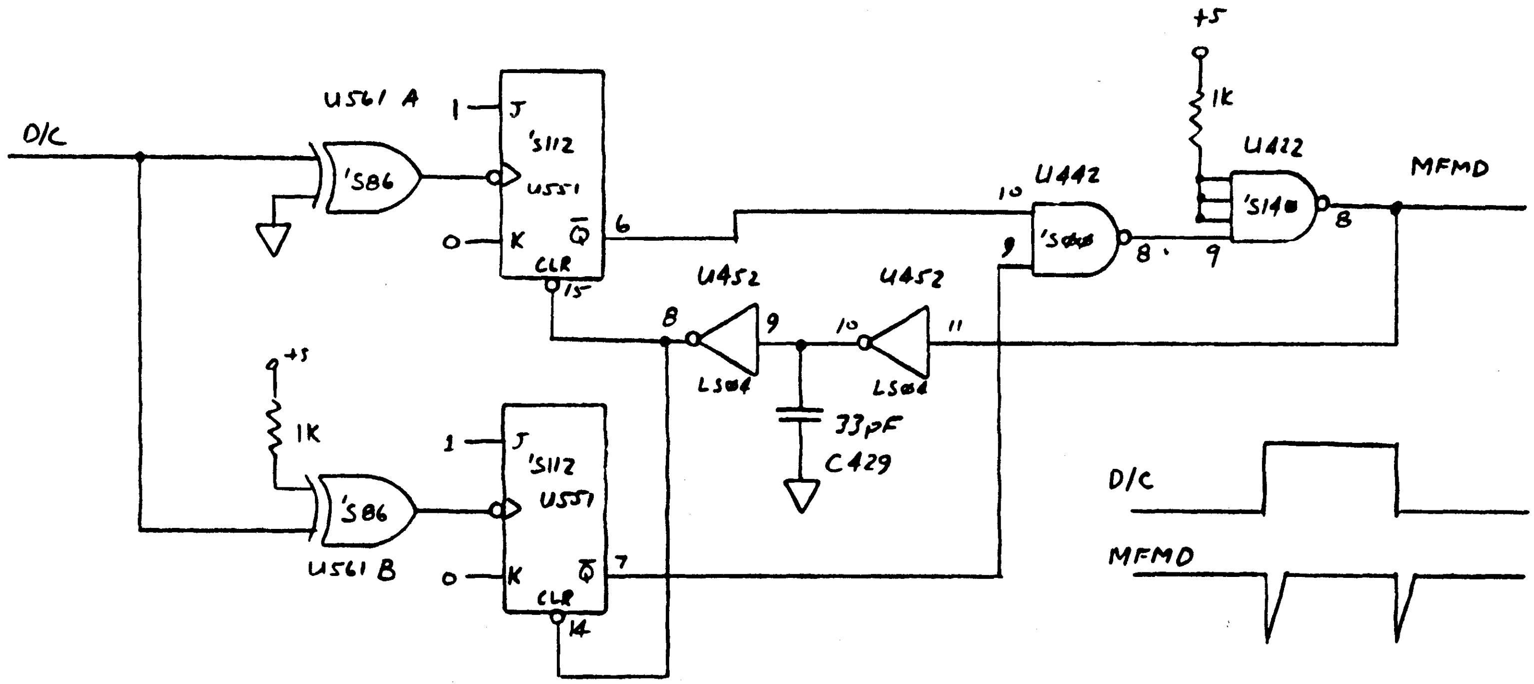
STOCK NO. 9280-0485 PRINTED ON DIEPO NO. 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A-07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY 810317 DATE

ENGINEER 810317

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE FIGURE 23 EDGE DETECTOR

NEXT ASSEMBLY

FINISH

SCALE

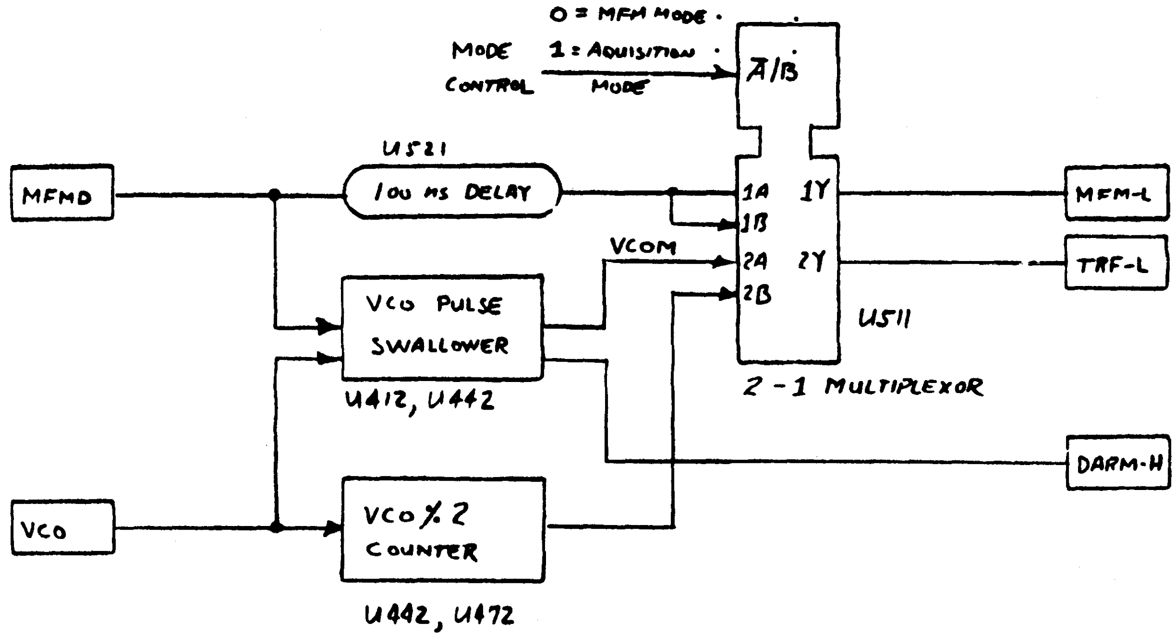
HEWLETT PACKARD

PART NUMBER A - 07908 - 60205 - 4

INEERING RESPONSIBILITY SEPIA

A- 07908 - 60205 -4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm · ± 0.4 mm
XX.X ± 0.2 mm · ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810317

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 24
CLOCK SELECT LOGIC
BLOCK DIAGRAM

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

PART NUMBER: A - 07908 - 60205- -4

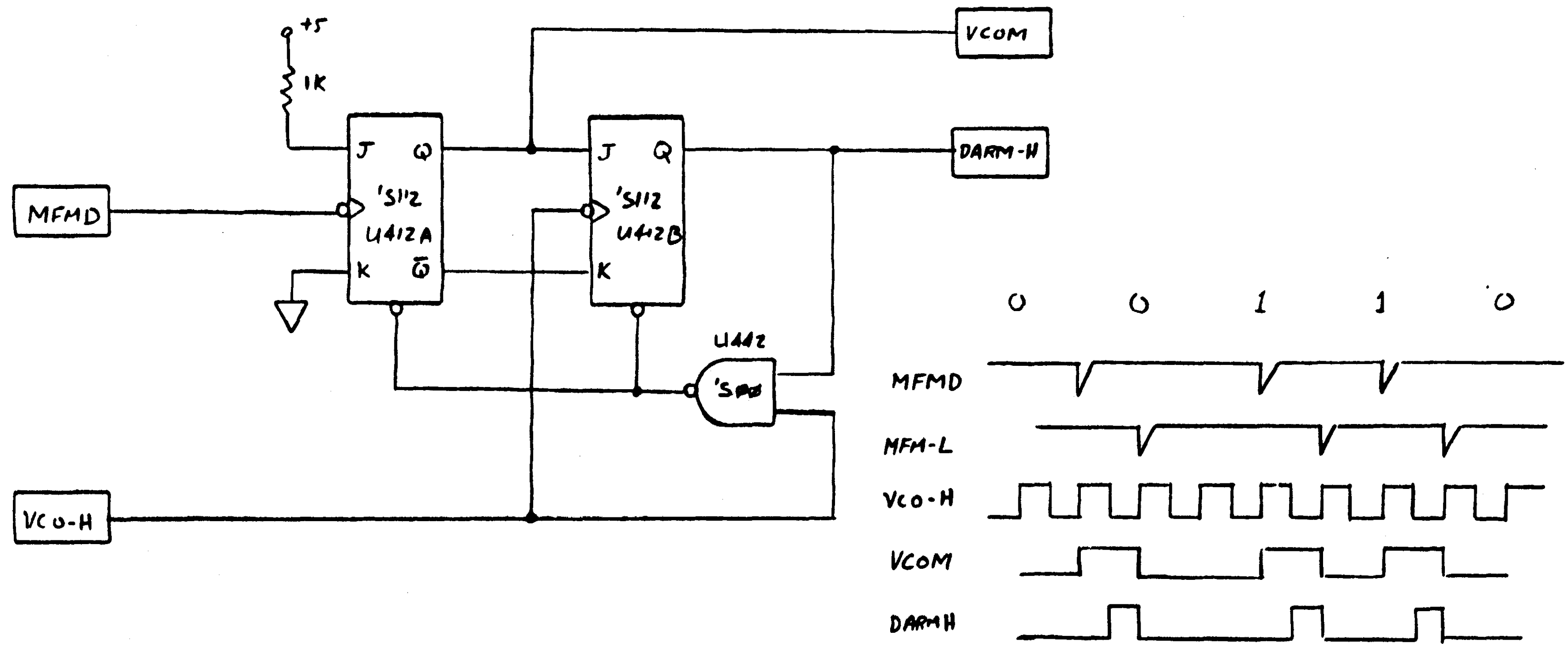
STOCK NO 9200-0405 PRINTED ON DIEPO NO. 10 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A - 07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY | DATE 810317

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

FIGURE 25
VCO PULSE SWALLOWER
TITLE

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

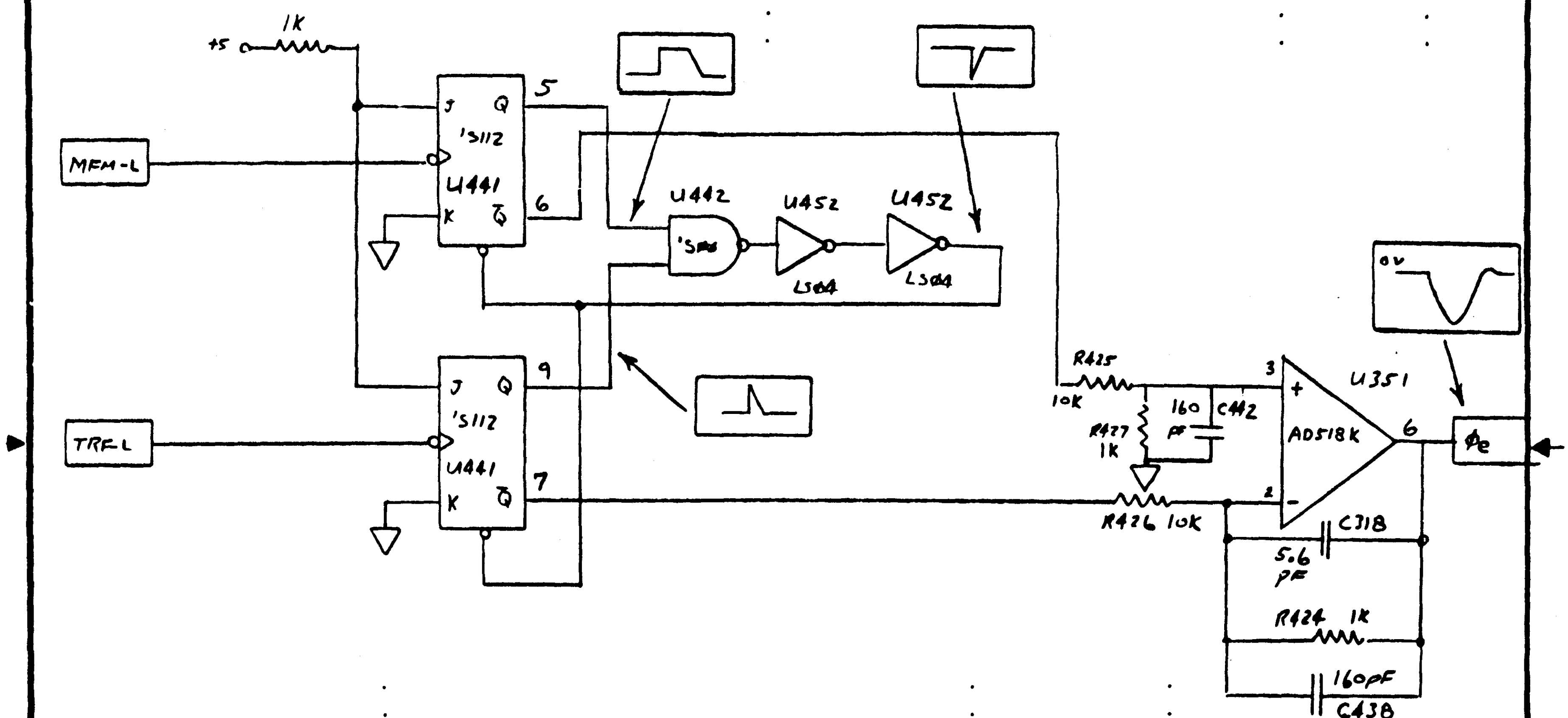
PART NUMBER
A - 07908 - 60205 - 4

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A-07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810318

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 26 PHASE DETECTOR

NEXT ASSEMBLY

FINISH

SCALE

HEWLETT PACKARD

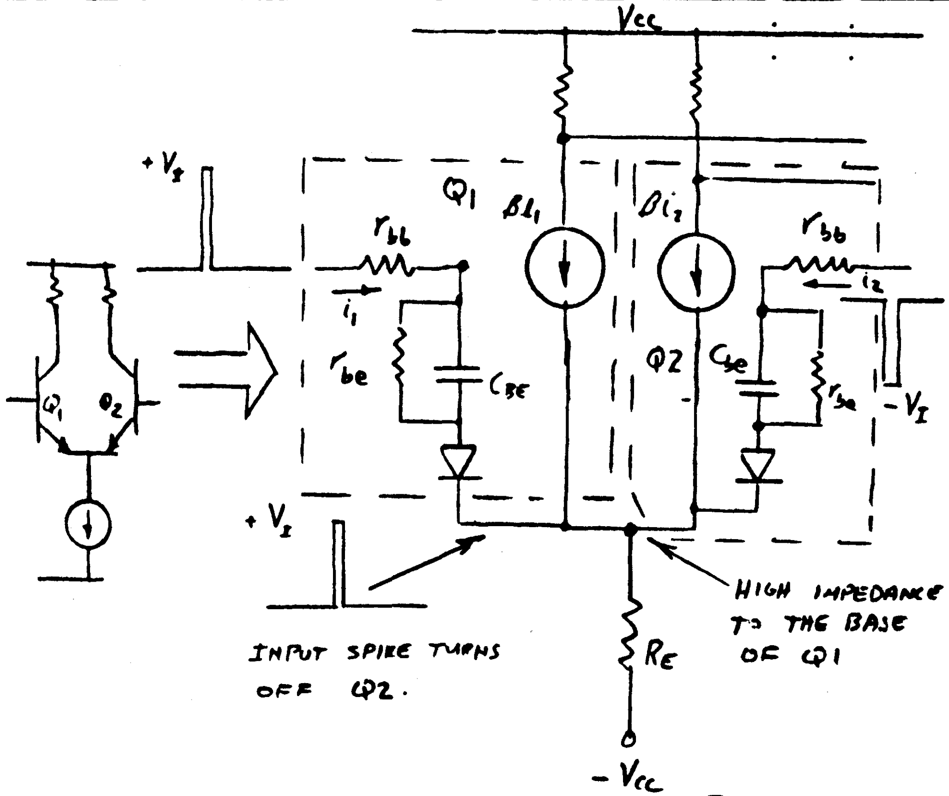
PART NUMBER A - 07908 - 60205 - 4

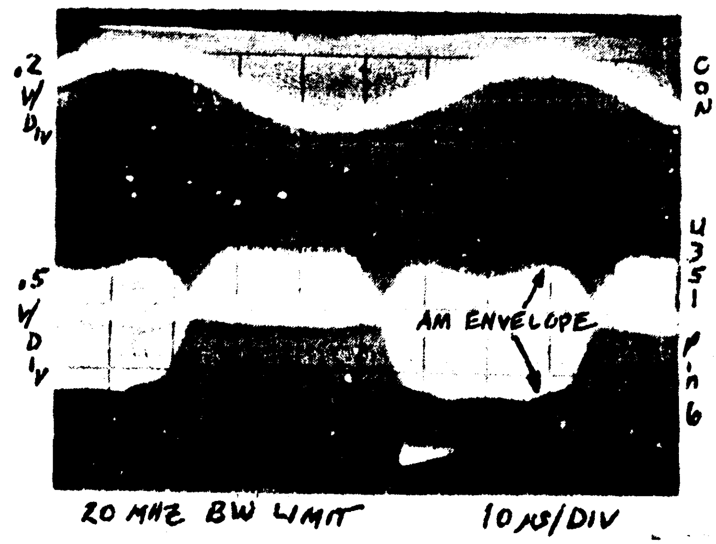
STOCK NO 9280-0485 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY																SEPIA
0	1	2	3	4		6		8	9		11	12	14	15		
16	17		19		21	22	23	25	29	30	32	33	38	43		
45	46	61	63													

A-07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE





ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

	DATE	
DRAWN BY	810318	
ENGINEER		TITLE: FIGURE 27 RECTIFICATION
RELEASE TO PROD.		NEXT ASSEMBLY
SUPERSEDES DWG.		FINISH / SCALE

HEWLETT PACKARD

PART NUMBER

A -07908 - 60205 - 4

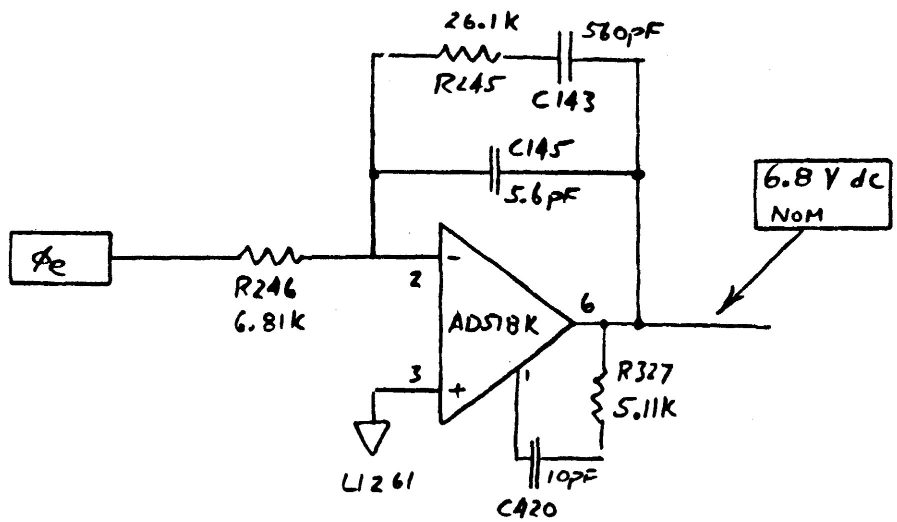
STOCK NO 9280-0403 PRINTED ON DIEPO. NO. 1020 MM CLEARPRINT FADEOUT

EERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9	11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A - 07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810317

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 28 LOOP FILTER

NEXT ASSEMBLY

FINISH

SCALE

HEWLETT PACKARD

PART NUMBER A - 07908 - 60205 - 4

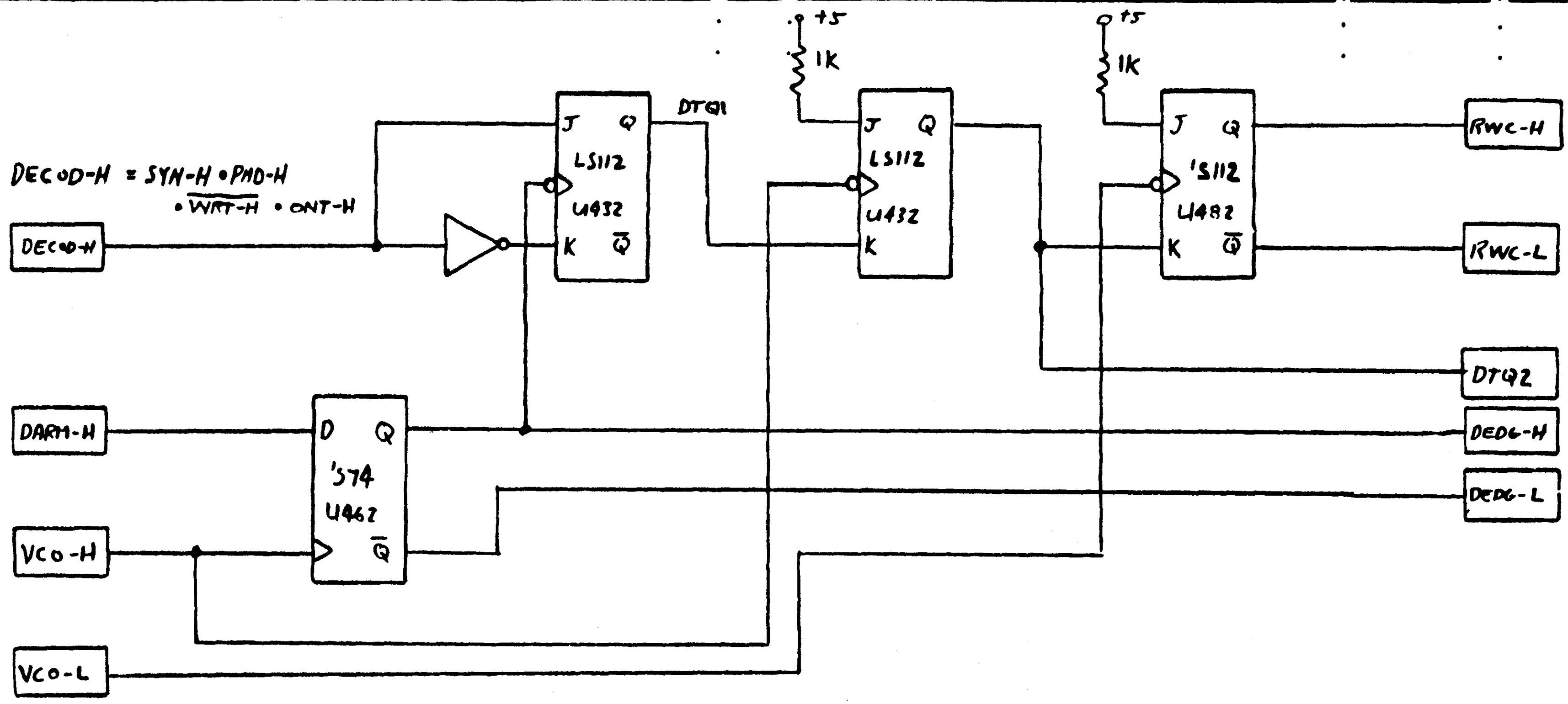
STOCK NO 9280-0405 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A-07908 - 60205 -4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810318

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 29 R/W CLOCK LOGIC

NEXT ASSEMBLY

FINISH

SCALE

HEWLETT PACKARD

PART NUMBER A - 07908 - 60205 - 4

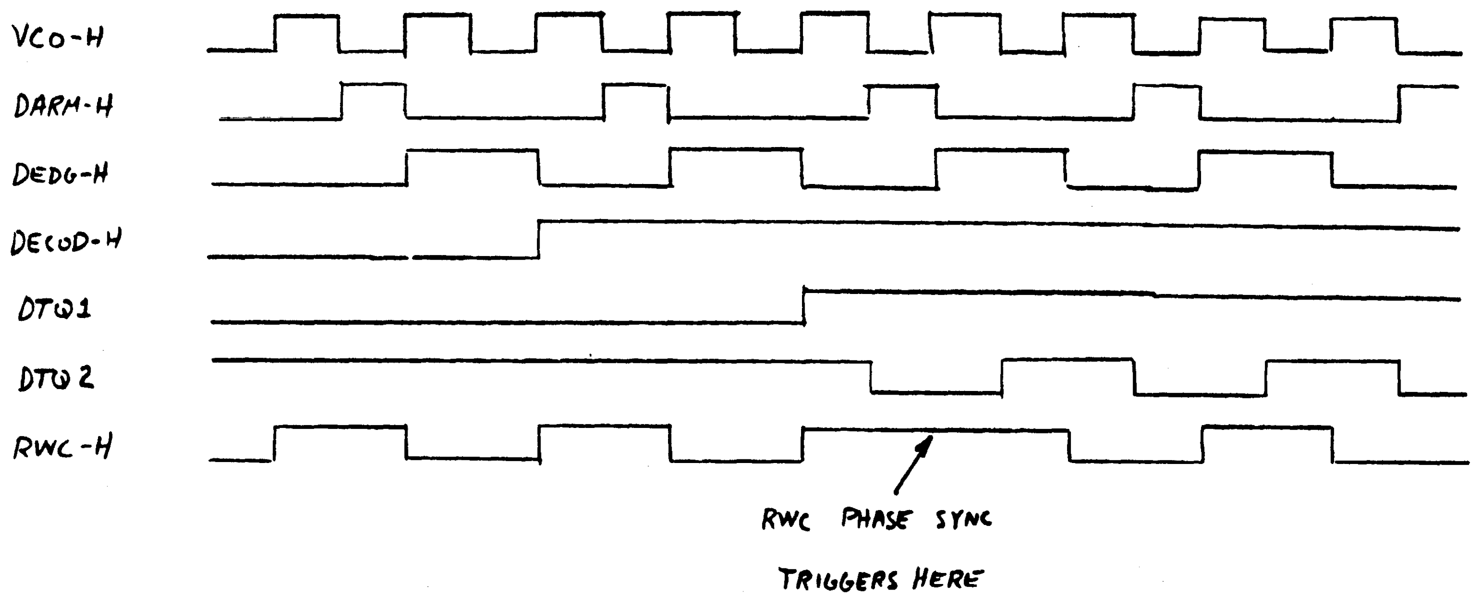
STOCK NO 9280-0405 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

A- 07908 - 60205 - 4

ENGINEERING RESPONSIBILITY | SEPIA

0	1	2	3	4		6		8	9		11	12	14	15	
18	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY | DATE 810318

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 30 R/W CLOCK LOGIC TIMING

HEWLETT PACKARD

NEXT ASSEMBLY

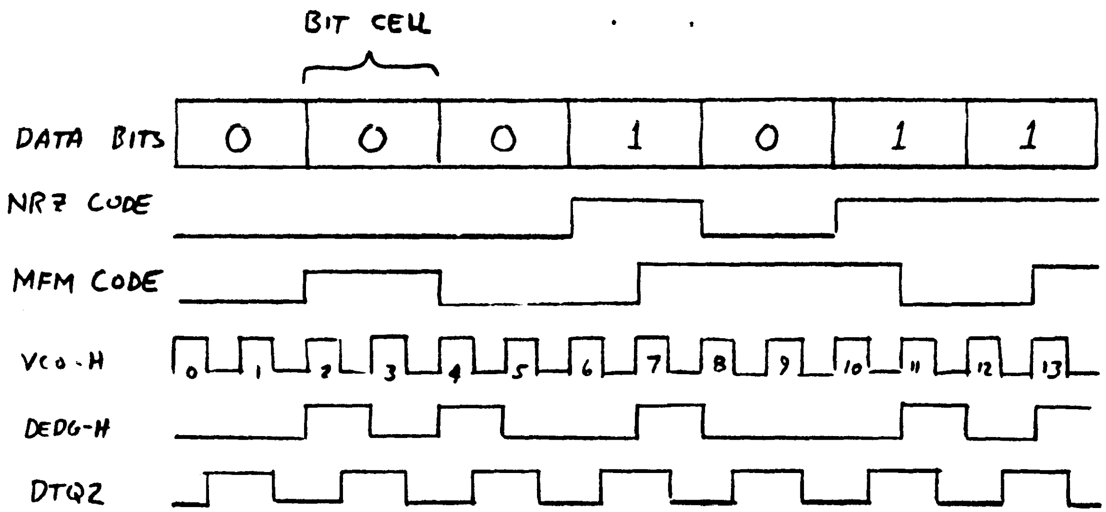
FINISH | SCALE

PART NUMBER A - 07908 - 60205 -4

ENGINEERING RESPONSIBILITY SEPIA

A- 07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810319

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 31 MFM CODE TIMING RELATIONSHIPS

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

PART NUMBER A - 07908 - 60205 - 4

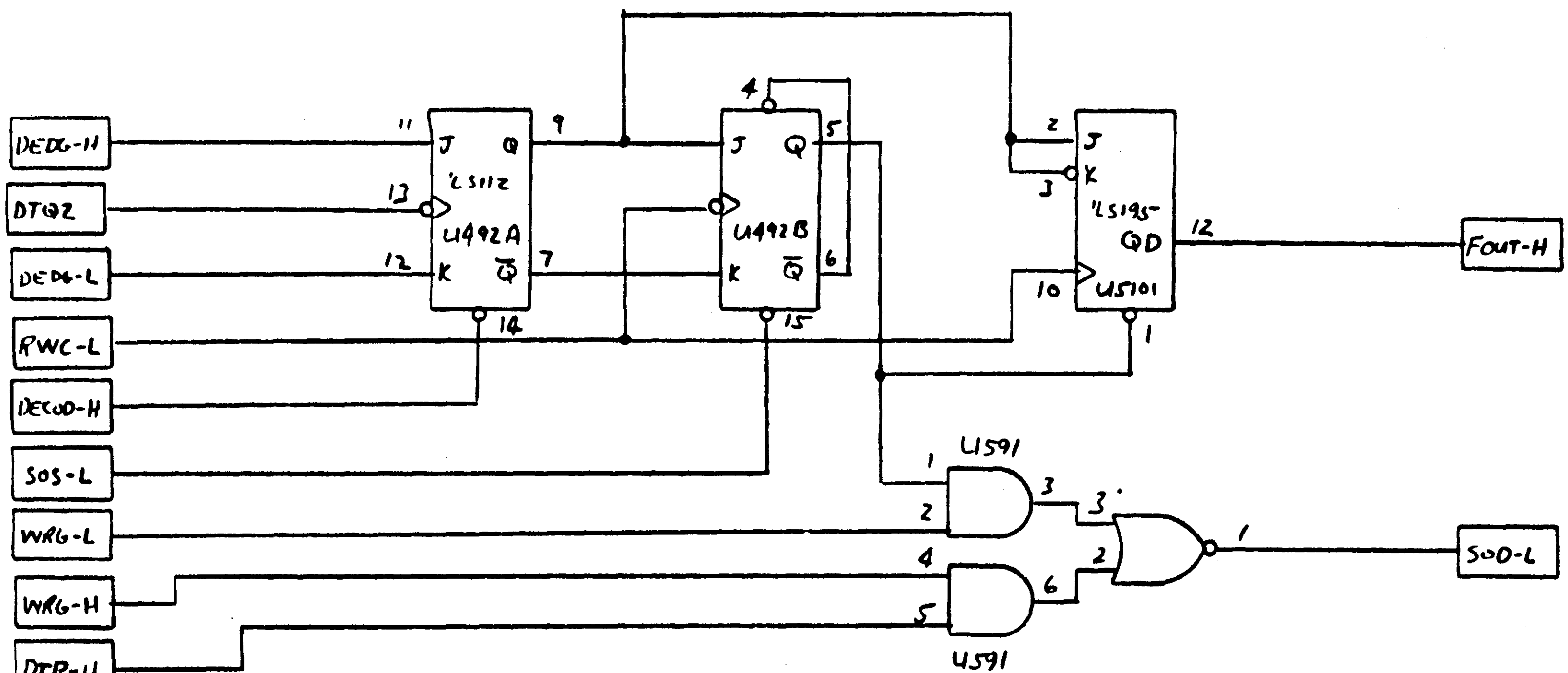
STOCK NO 9280-0405 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A- 07908 - 60205 -4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810319

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 32 THE SEPARATOR

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

PART NUMBER A- 07908 - 60205 -4

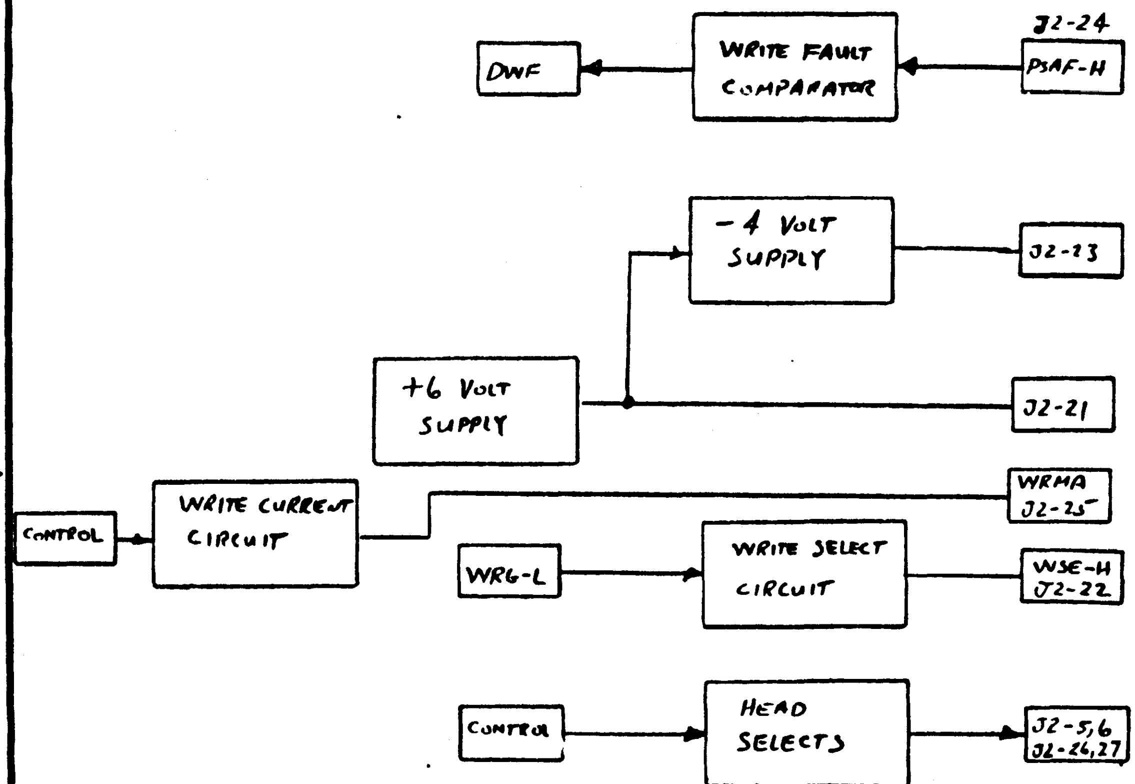
STOCK NO 9280-0405 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

A-07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810319

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 33 DISC MECHANISM INTERFACE

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

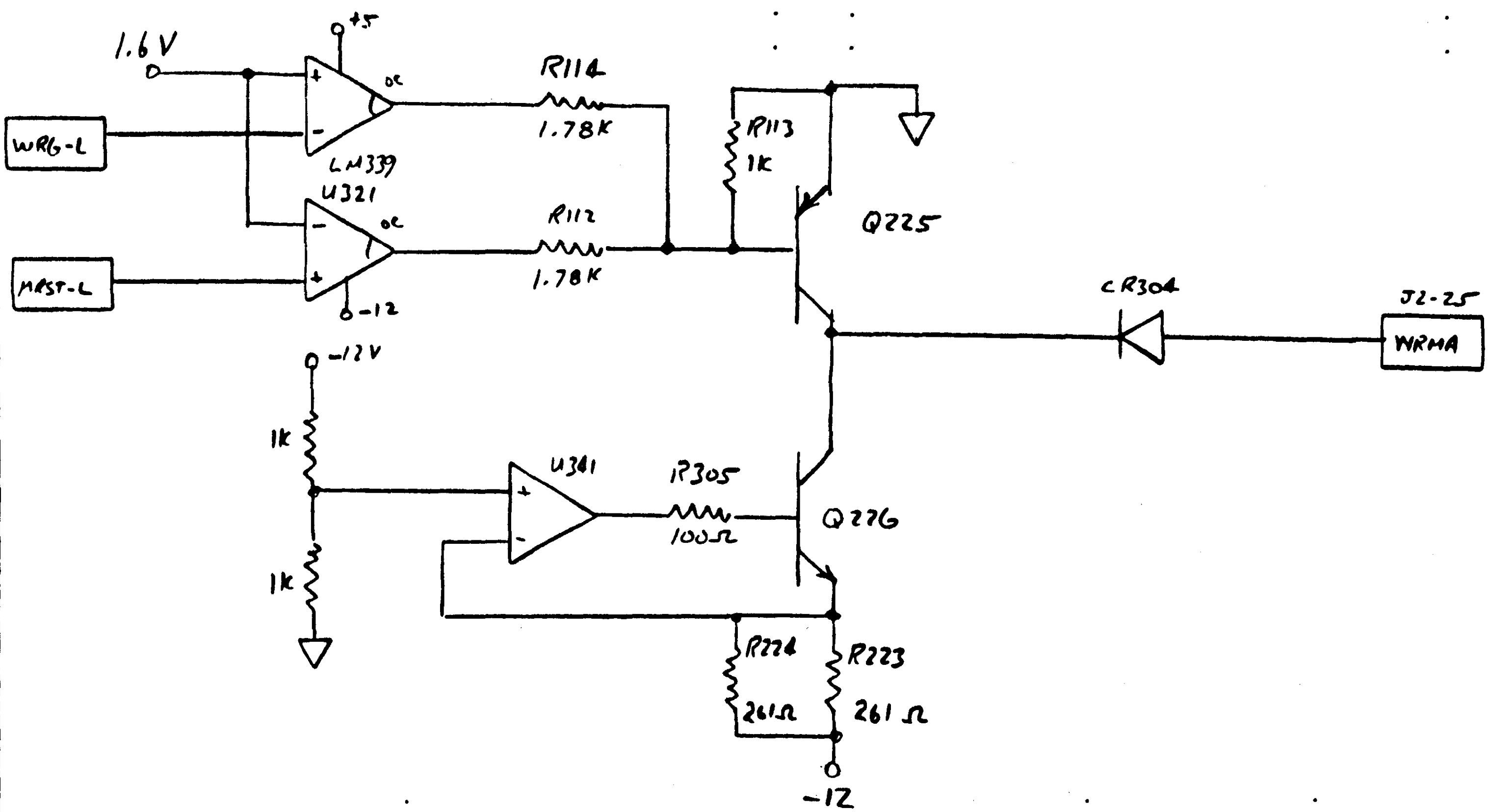
PART NUMBER A - 07908 - 60205 - 4

ENGINEERING RESPONSIBILITY SEPIA

A- 07908 - 60205 - 4

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810319

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FIGURE 34 WRITE CURRENT CIRCUIT

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

PART NUMBER: A - 07908 - 60205 - 4

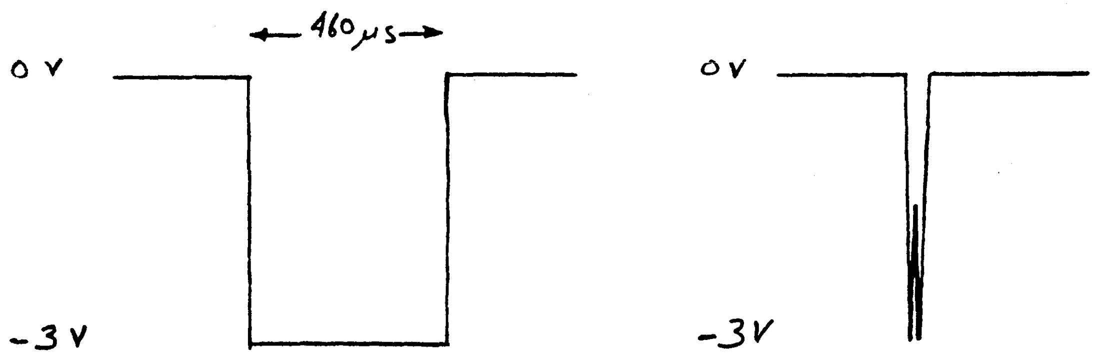
STOCK NO 9280-0405 PRINTED ON DIEPO NO 1020 MM CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY | SEPIA

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	36	43	
45	46	61	63												

A- 07908 - 60205 - 4

SYM	REVISIONS	APPROVED	DATE



GOOD WRMA SIGNAL
DURING A WRITE

BAD WRMA SIGNAL
WHEN Q225 is BAD

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY — DATE 810319

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE FIGURE 35
A STRANGE SYMPTOM OF A BAD Q225.

NEXT ASSEMBLY

FINISH — SCALE

HEWLETT PACKARD

PART NUMBER
A - 07908 - 60205 - 4

STOCK NO 9280-0405 PRINTED ON DIEPO NO. 1020 MM CLEARPRINT FADEOUT

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60205
07908-66205
07908-68205

DATE CODE : E-2300

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C102	0160-5298	CAP .01UF 20%
C133	0160-5332	CAP.1UF 20% 50V
C134	0160-5332	CAP.1UF 20% 50V
C136	0160-5298	CAP .01UF 20%
C140	0160-5332	CAP.1UF 20% 50V
C141	0160-5298	CAP .01UF 20%
C143	0160-3535	CAP 560PF 5%
C144	0160-5332	CAP.1UF 20% 50V
C145	0160-4498	CAP 5.6PF 5%
C153	0160-5298	CAP .01UF 20%
C158	0160-5332	CAP.1UF 20% 50V
C168	0160-5332	CAP.1UF 20% 50V
C174	0160-5332	CAP.1UF 20% 50V
C183	0160-5332	CAP.1UF 20% 50V
C184	0160-3533	CAP 470PF 5%
C186	0140-0196	CAP 150PF 5%
C187	0160-5298	CAP .01UF 20%
C195	0160-5298	CAP .01UF 20%
C197	0160-2218	CAP 1000PF 5%
C198	0160-5332	CAP.1UF 20% 50V
C203	0160-2218	CAP 1000PF 5%
C213	0160-5298	CAP .01UF 20%
C214	0160-5298	CAP .01UF 20%
C215	0160-5332	CAP.1UF 20% 50V
C217	0160-2223	CAP 1600PF 5%
C235	0160-5332	CAP.1UF 20% 50V
C251	0160-5332	CAP.1UF 20% 50V
C252	0160-5332	CAP.1UF 20% 50V
C258	0160-2265	CAP 22PF 5%
C262	0160-2218	CAP 1000PF 5%
C263	0160-5298	CAP .01UF 20%
C264	0160-5332	CAP.1UF 20% 50V
C302	0160-5298	CAP .01UF 20%
C303	0160-5298	CAP .01UF 20%
C306	0160-5298	CAP .01UF 20%
C309	0160-5298	CAP .01UF 20%
C314	0160-5298	CAP .01UF 20%
C315	0160-5332	CAP.1UF 20% 50V
C316	0160-5332	CAP.1UF 20% 50V
C318	0160-4498	CAP 5.6PF 5%
C319	0160-3875	CAP 22PF 5%
C323	0160-5332	CAP.1UF 20% 50V
C329	0160-5298	CAP .01UF 20%
C333	0160-5332	CAP.1UF 20% 50V
C336	0160-5332	CAP.1UF 20% 50V
C337	0160-5332	CAP.1UF 20% 50V
C345	0160-2206	CAP 160PF 5%

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60205
07908-66205
07908-68205

DATE CODE : E-2300

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C347	0160-5298	CAP .01UF 20%
C348	0160-5298	CAP .01UF 20%
C354	0160-5298	CAP .01UF 20%
C355	0160-5298	CAP .01UF 20%
C357	0160-5298	CAP .01UF 20%
C401	0160-4084	CAP .1UF 20%
C406	0160-5298	CAP .01UF 20%
C408	0160-5298	CAP .01UF 20%
C420	0160-3874	CAP 10PF .5
C428	0160-5298	CAP .01UF 20%
C429	0160-2150	CAP 33PF 5%
C433	0160-3878	CAP 1000PF 20%
C435	0160-5298	CAP .01UF 20%
C438	0160-2206	CAP 160PF 5%
C442	0160-2206	CAP 160PF 5%
C444	0160-5298	CAP .01UF 20%
C447	0160-5298	CAP .01UF 20%
C453	0160-5332	CAP.1UF 20% 50V
C454	0160-5332	CAP.1UF 20% 50V
C463	0160-5332	CAP.1UF 20% 50V
C464	0160-5332	CAP.1UF 20% 50V
C476	0160-5332	CAP.1UF 20% 50V
C477	0160-5332	CAP.1UF 20% 50V
C486	0160-5298	CAP .01UF 20%
C501	0160-5298	CAP .01UF 20%
C502	0160-5298	CAP .01UF 20%
C503	0160-5298	CAP .01UF 20%
C514	0160-5298	CAP .01UF 20%
C515	0160-5298	CAP .01UF 20%
C518	0160-5298	CAP .01UF 20%
C519	0160-5298	CAP .01UF 20%
C520	0160-5298	CAP .01UF 20%
C523	0160-5298	CAP .01UF 20%
C524	0160-5298	CAP .01UF 20%
C525	0160-5298	CAP .01UF 20%
C526	0160-5298	CAP .01UF 20%
C528	0160-5298	CAP .01UF 20%
C529	0160-5298	CAP .01UF 20%
C532	0160-5298	CAP .01UF 20%
C540	0160-5332	CAP.1UF 20% 50V
C553	0160-5298	CAP .01UF 20%
C602	0160-5298	CAP .01UF 20%
C603	0160-5332	CAP.1UF 20% 50V
C604	0160-5332	CAP.1UF 20% 50V
C606	0180-2205	C-F .33UF 35V TA
C607	0180-0374	CAP 10UF 10%
C614	0180-0374	CAP 10UF 10%

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60205
07908-66205
07908-68205

DATE CODE : E-2300

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C615	0160-5332	CAP.1UF 20% 50V
C616	0160-5298	CAP .01UF 20%
C617	0160-5332	CAP.1UF 20% 50V
C618	0180-0374	CAP 10UF 10%
C623	0160-5298	CAP .01UF 20%
C624	0160-5332	CAP.1UF 20% 50V
C626	0160-5332	CAP.1UF 20% 50V
C628	0160-5298	CAP .01UF 20%
CR192	1901-0040	DIODE-SWITCHING
CR202	1901-0040	DIODE-SWITCHING
CR244	1901-0040	DIODE-SWITCHING
CR304	1901-0040	DIODE-SWITCHING
CR312	1901-0040	DIODE-SWITCHING
CR507	1901-0040	DIODE-SWITCHING
CR508	1901-0040	DIODE-SWITCHING
CR509	1901-0040	DIODE-SWITCHING
CR510	1901-0040	DIODE-SWITCHING
L256	9100-1619	INDUCTOR 6.8UH
L257	9100-1619	INDUCTOR 6.8UH
L343	9100-2262	COIL 3.9UH 10%
MP2	7120-6830	LABEL-INFO
MP3	1480-0116	PIN GRV .062X.25
MP5	0340-0164	INSUL-XSTR
MP6	4330-0145	BEADS INDIAN
MP7	0403-0453	EXTR-PC BD #3
MP7	1200-0455	SOCKET 8 DIP LO
Q101	1854-0637	XSTR NPN 2N2219A
Q152	1854-0295	XSTR-DUAL NPN
Q157	1854-0295	XSTR-DUAL NPN
Q199	1853-0281	XSTR PNP 2N2907A
Q221	1853-0281	XSTR PNP 2N2907A
Q225	1853-0314	XSTR PNP 2N2905A
Q226	1854-0637	XSTR NPN 2N2219A
Q233	1853-0314	XSTR PNP 2N2905A
Q605	1826-0215	IC MC7905.2CT
Q627	1826-0349	IC UA78M06HL
R103	0698-4037	RES 46.4 1%.125
R104	0698-3150	RES 2.37K 1%.125
R110	0698-3438	RES 147 1%.125
R111	0757-0279	RES 3.16K 1%.125
R112	0757-0278	RES 1.78K 1%.125
R113	0757-0280	RES 1K 1%.125
R114	0757-0278	RES 1.78K 1%.125
R115	0757-0416	RES 511 1%.125
R116	0757-0416	RES 511 1%.125
R121	0698-3453	RES 196K 1%.125
R121	0698-3454	RES 215K 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60205
07908-66205
07908-68205

DATE CODE : E-2300

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R121	0757-0472	RES 200K 1%
R122	0698-3453	RES 196K 1%.125
R122	0698-3454	RES 215K 1%.125
R122	0757-0472	RES 200K 1%
R123	0698-3442	RES 237 1%.125
R125	0757-0401	RES 100 1%.125
R126	0757-0200	RES 5.62K 1%.125
R132	0757-0424	RES 1.1K 1%.125
R135	0698-3444	RES 316 1%.125
R142	0757-0280	RES 1K 1%.125
R154	0757-0405	RES 162 1%.125
R155	0757-1094	RES 1.47K 1%.125
R156	0698-3440	RES 196 1%.125
R164	0757-1094	RES 1.47K 1%.125
R165	0698-3441	RES 215 1%.125
R166	0698-3441	RES 215 1%.125
R173	0698-3440	RES 196 1%.125
R175	0698-3442	RES 237 1%.125
R176	0698-3442	RES 237 1%.125
R181	0757-0180	RES 31.6 1% .125
R182	0698-3440	RES 196 1%.125
R191	0757-0400	RES 90.9 1%.125
R193	0698-3440	RES 196 1%.125
R194	0757-0401	RES 100 1%.125
R196	0757-0401	RES 100 1%.125
R201	0698-3430	RES 21.5 1% .125
R204	0757-0274	RES 1.21K 1%.125
R205	0698-0083	RES 1.96K 1%.125
R211	0757-0279	RES 3.16K 1%.125
R212	0757-0280	RES 1K 1%.125
R216	0757-1094	RES 1.47K 1%.125
R223	0698-3132	RES 261 1%.125
R224	0698-3132	RES 261 1%.125
R227	0757-0317	RES 1.33K 1%.125
R228	0757-0401	RES 100 1%.125
R234	0757-0401	RES 100 1%.125
R236	0698-3440	RES 196 1%.125
R242	0698-3440	RES 196 1%.125
R243	0757-0280	RES 1K 1%.125
R245	0698-3159	RES 26.1K 1%.125
R246	0757-0439	RES 6.81K 1%.125
R253	0698-3153	RES 3.83K 1%.125
R254	0757-1094	RES 1.47K 1%.125
R259	0698-0082	RES 464 1%.125
R265	0757-0279	RES 3.16K 1%.125
R266	0757-0279	RES 3.16K 1%.125
R267	0757-0280	RES 1K 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60205
07908-66205
07908-68205

DATE CODE : E-2300

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R301	0764-0013	RES 56 5% 2W
R305	0757-0401	RES 100 1%.125
R307	0757-0280	RES 1K 1%.125
R308	0757-0280	RES 1K 1%.125
R313	0757-0401	RES 100 1%.125
R317	0757-0280	RES 1K 1%.125
R324	0757-0280	RES 1K 1%.125
R325	0757-0416	RES 511 1%.125
R326	0698-3154	RES 4.22K 1%.125
R327	0757-0438	RES 5.11K 1%.125
R328	0757-0200	RES 5.62K 1%.125
R338	0698-3150	RES 2.37K 1%.125
R339	0698-3150	RES 2.37K 1%.125
R346	0698-3441	RES 215 1%.125
R349	0698-3132	RES 261 1%.125
R353	0757-0279	RES 3.16K 1%.125
R356	0757-0401	RES 100 1%.125
R402	0757-0346	RES 10 1%.125
R403	0757-0280	RES 1K 1%.125
R404	0757-0280	RES 1K 1%.125
R405	0757-0442	RES 10K 1%.125
R407	0757-0280	RES 1K 1%.125
R413	0757-0280	RES 1K 1%.125
R415	0757-0280	RES 1K 1%.125
R416	0757-0280	RES 1K 1%.125
R417	0757-0280	RES 1K 1%.125
R418	0757-0280	RES 1K 1%.125
R423	0757-0280	RES 1K 1%.125
R424	0757-0280	RES 1K 1%.125
R425	0757-0442	RES 10K 1%.125
R426	0757-0442	RES 10K 1%.125
R427	0757-0280	RES 1K 1%.125
R434	0757-0280	RES 1K 1%.125
R437	0757-0459	R:F 56.2K 1%.125
R439	0757-0459	R:F 56.2K 1%.125
R443	0757-0280	RES 1K 1%.125
R445	0757-0280	RES 1K 1%.125
R448	0757-0280	RES 1K 1%.125
R457	0757-0279	RES 3.16K 1%.125
R458	0757-0280	RES 1K 1%.125
R459	0757-0280	RES 1K 1%.125
R466	0698-3154	RES 4.22K 1%.125
R467	0698-3154	RES 4.22K 1%.125
R468	0757-0280	RES 1K 1%.125
R473	0757-0280	RES 1K 1%.125
R474	0757-0440	RES 7.5K 1%.125
R475	0698-0084	RES 2.15K 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60205
07908-66205
07908-68205

DATE CODE : E-2300

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R479	0698-0083	RES 1.96K 1%.125
R483	0698-0083	RES 1.96K 1%.125
R484	0757-0280	RES 1K 1%.125
R485	0757-0280	RES 1K 1%.125
R504	0757-0401	RES 100 1%.125
R505	0757-0280	RES 1K 1%.125
R506	0757-0280	RES 1K 1%.125
R513	0757-0280	RES 1K 1%.125
R517	0757-0280	RES 1K 1%.125
R527	0757-0280	RES 1K 1%.125
R536	0757-0198	RES 100 1% .50
R537	0757-1060	RES 196 1% .50
R538	0757-1060	RES 196 1% .50
R601	0757-0280	RES 1K 1%.125
R613	0757-0280	RES 1K 1%.125
R625	0757-0280	RES 1K 1%.125
U161	1826-0065	IC 311
U181	1858-0032	XSTR-MULTI NPN
U2101	1826-0139	IC MC1458 P1
U261	1826-0327	IC 518K
U3101	1858-0032	XSTR-MULTI NPN
U321	1826-0138	IC LM339
U341	1826-0139	IC MC1458 P1
U351	1826-0327	IC 518K
U381	1826-0194	IC 592
U4101	1810-0317	NETWORK-RES DIP
U4102	1826-0869	IC-AM686
U412	1820-0629	IC SN74S112N
U421	1820-0471	IC SN7406N
U422	1820-0697	IC SN74S140N
U431	1820-1197	IC SN74LS00N
U432	1820-1212	IC SN74LS112N
U441	1820-0629	IC SN74S112N
U442	1820-0681	IC SN74S00N
U452	1820-1199	IC SN74LS04N
U461	1820-2369	IC SN74LS629N
U462	1820-0693	IC SN74S74N
U472	1820-0629	IC SN74S112N
U481	1826-0138	IC LM339
U482	1820-0629	IC SN74S112N
U492	1820-1212	IC SN74LS112N
U5101	1820-1300	IC SN74LS195AN
U511	1820-1077	IC SN74S157N
U512	1820-1201	IC SN74LS08N
U521	1810-0198	I.C. DELAY LINE
U522	1820-1212	IC SN74LS112N
U532	1820-0629	IC SN74S112N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

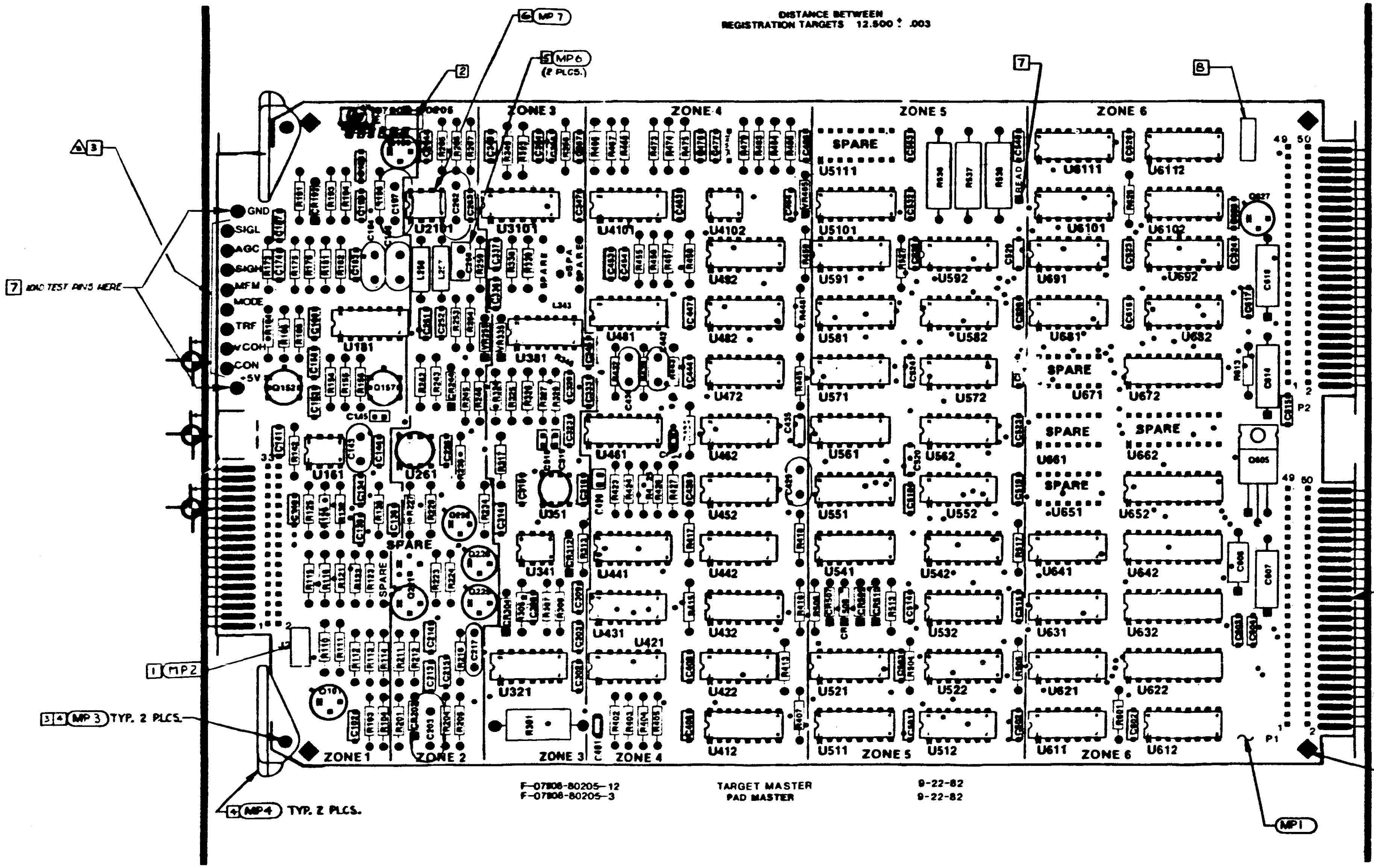
PART-NUMBER(S): 07908-60205
07908-66205
07908-68205

DATE CODE : E-2300

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U541	1820-1173	IC MC10124L
U542	1820-1212	IC SN74LS112N
U551	1820-0629	IC SN74S112N
U552	1820-1199	IC SN74LS04N
U561	1820-0694	IC SN74S86N
U562	1820-1206	IC SN74LS27N
U571	1820-1322	IC SN74S02N
U572	1820-1201	IC SN74LS08N
U581	1820-1212	IC SN74LS112N
U582	1820-1112	IC SN74LS74N
U591	1820-1201	IC SN74LS08N
U592	1820-1112	IC SN74LS74N
U6101	1820-1431	IC SN74LS162N
U6102	1810-0286	NETWORK-RES DIP
U611	1820-1112	IC SN74LS74N
U6111	1820-1431	IC SN74LS162N
U6112	1820-1431	IC SN74LS162N
U612	1810-0461	NETWORK-RES DIP
U621	1820-1416	IC SN74LS14N
U622	1820-2024	IC SN74LS244N
U631	1820-1197	IC SN74LS00N
U632	1820-1730	IC SN74LS273N
U641	1820-1197	IC SN74LS00N
U642	1820-1730	IC SN74LS273N
U652	1820-1918	IC SN74LS241N
U672	1820-2024	IC SN74LS244N
U681	1820-1449	IC SN74S32N
U682	1820-1440	IC SN74LS279N
U691	1820-1112	IC SN74LS74N
U692	1820-1440	IC SN74LS279N
VR255	1902-0049	DIODE 6.19V
VR335	1902-0049	DIODE 6.19V
VR465	1902-0049	DIODE 6.19V

END OF MATERIAL LIST.

		F-07908-60805-1	
A	AS ISSUED PER PCO 48 4870		
B	CORRECTED TEST PINS PER P.C.O. 48-6090.		
C	DATE CODE WAS E-2244 PC 48 6354		4-17-84



F-07908-80205-9 GRAPHICS-COMPONENT SIDE 9-22-82

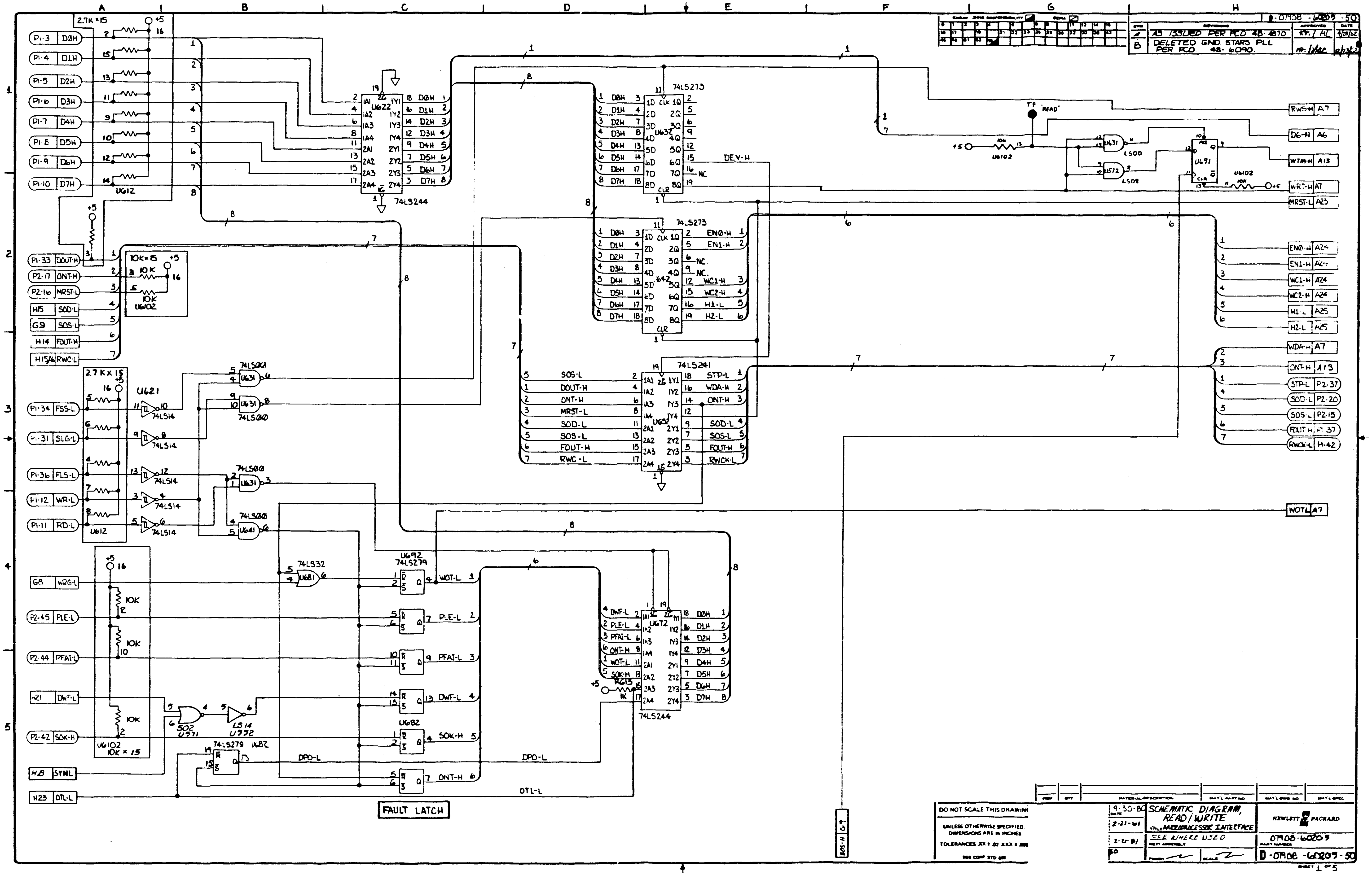
REFERENCE DRAWINGS:
SCHEMATIC D-07908-60805-50

UNLESS OTHERWISE SPECIFIED:

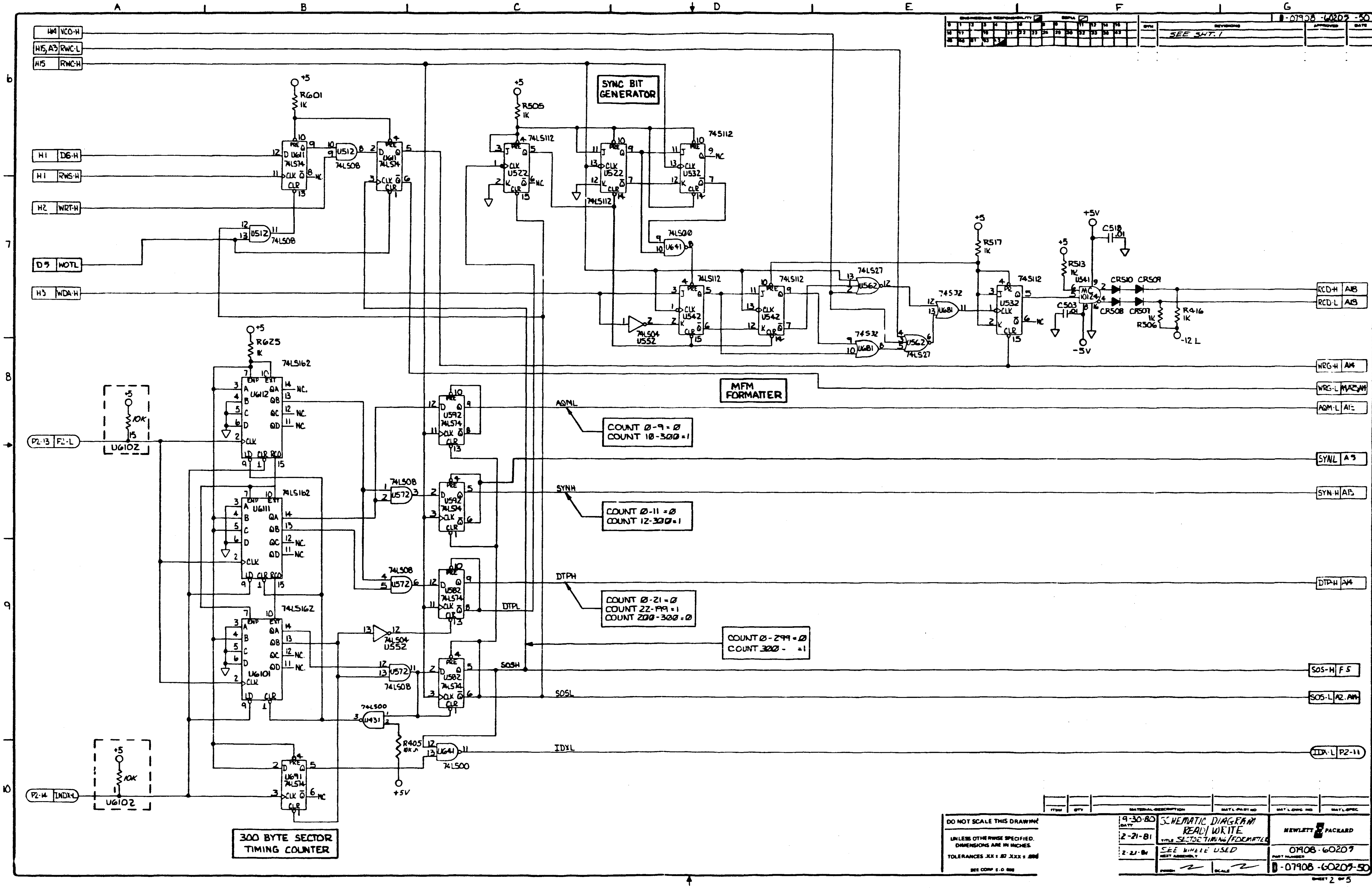
THIS BOARD CONFORMS TO CORPORATE AUTOMATIC INSERTION STANDARDS AS PER AXIAL LEAD STANDARDS 4-14-80.

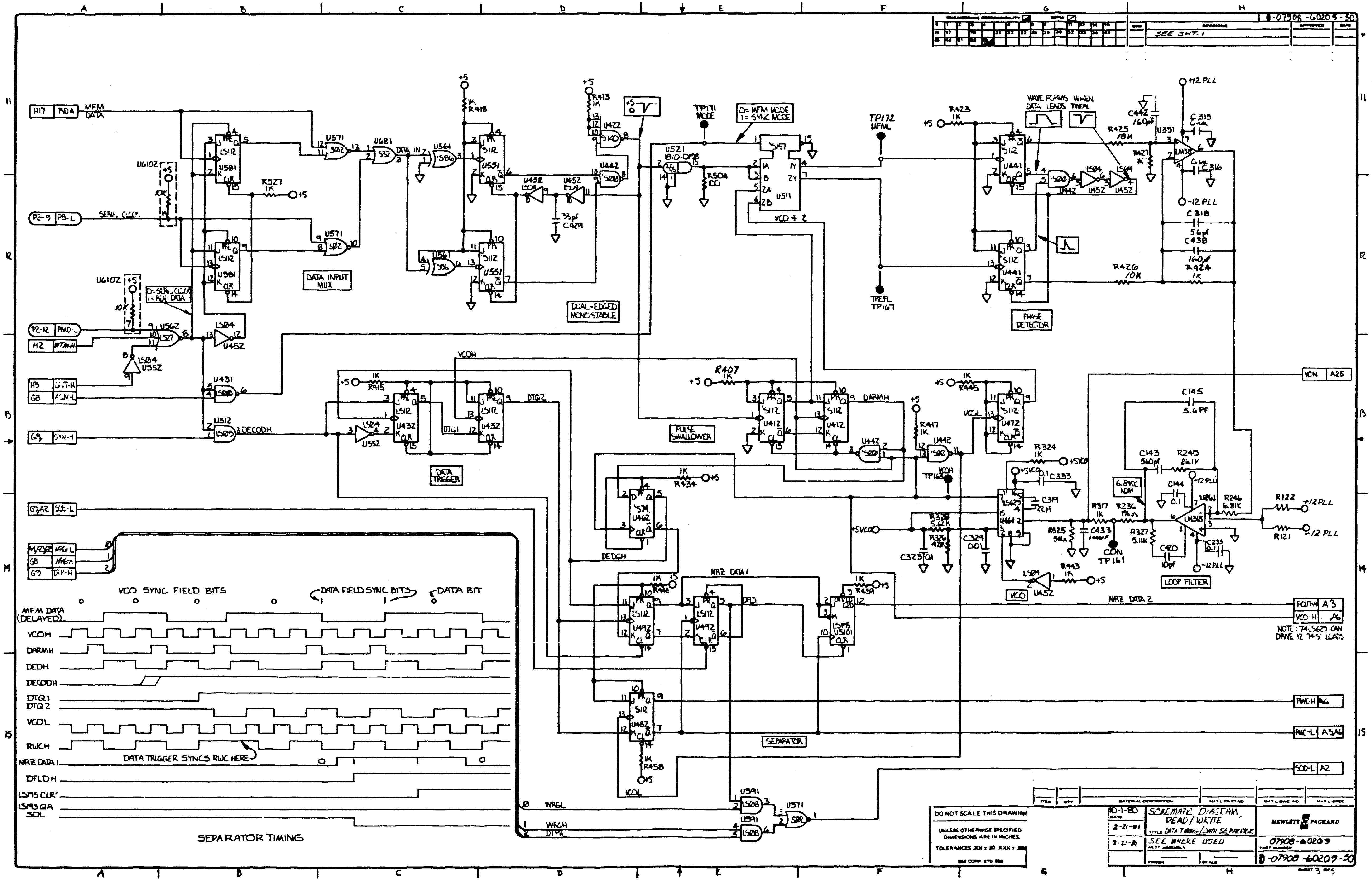
NOTES:
1. INSTALL MP2 AFTER LINE TEST.
2. OPR. 264 :MARK ASSEMBLY DATE CODE E-2300
3. OPR. 265 :MASK PRIOR TO LOADING
4. OPR. 266 :TOUCH UP. INSTALL MP3-4
5. INSTALL MP6 ON LEADS AT LOADING.
6. INSTALL SOCKET MP7 WHEN LOADING BOARD.
7. INSTALL TEST PINS AS INDICATED.
8. P.C. PRODUCTION: MARK ASSEMBLY WORK ORDER NUMBER ON COMP. SIDE ONLY

10-24-80	BOARD ASSEMBLY, READ/WRITE	HEWLETT PACKARD
2-21-81		
	SEE WHERE USED	07908-60805
	2:1	F-07908-60205-1

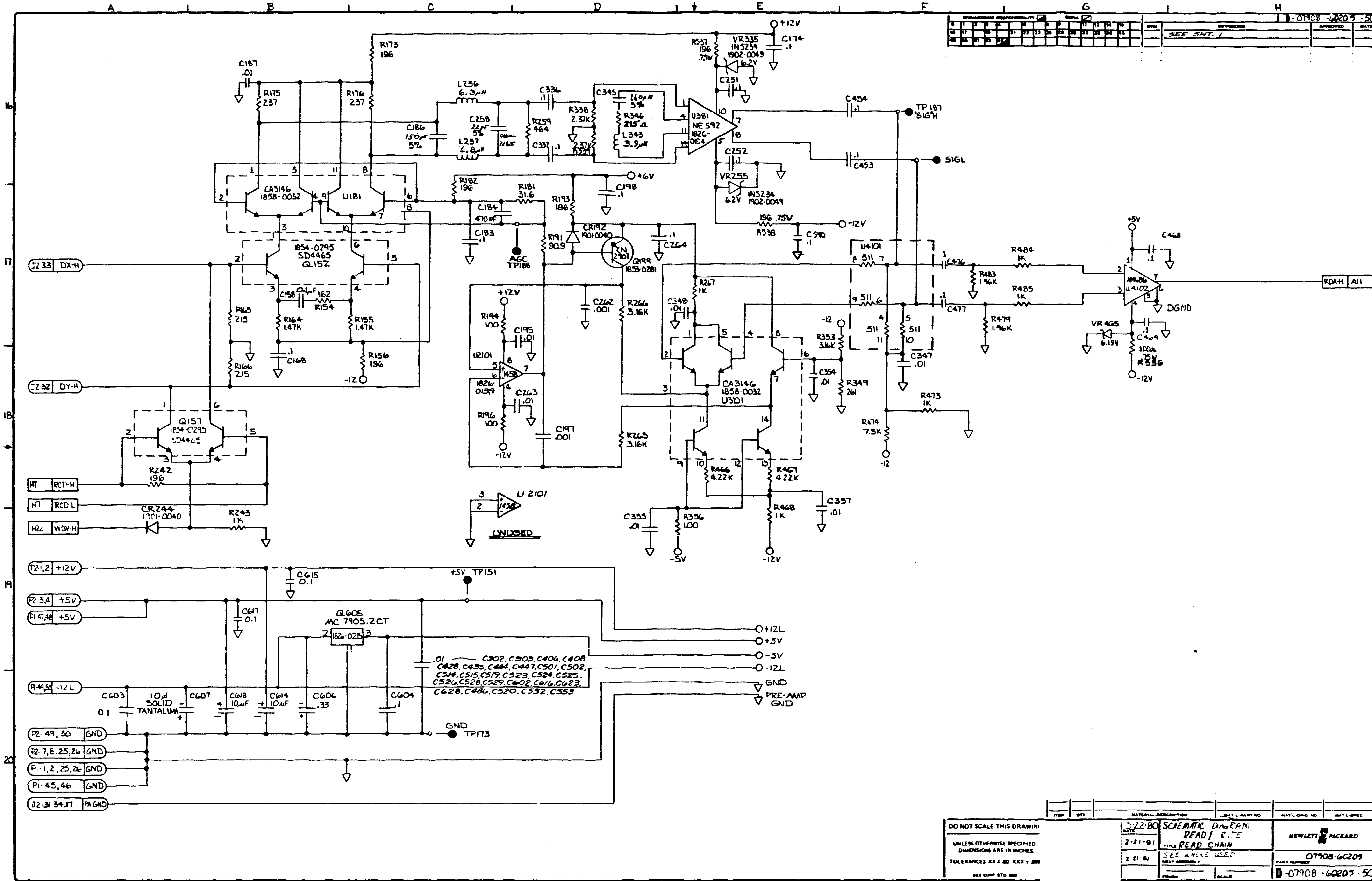


A AS ISSUED PER PCO 48-4870
B DELETED GND STARS PLL PER PCO 48-6090.
74LS244
74LS273
74LS241
74LS279
FAULT LATCH
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
SCHEMATIC DIAGRAM, READ/WRITE MICROPROCESSOR INTERFACE
SEE WHERE USED
HEWLETT PACKARD
07908-60205
D-07908-60205-50

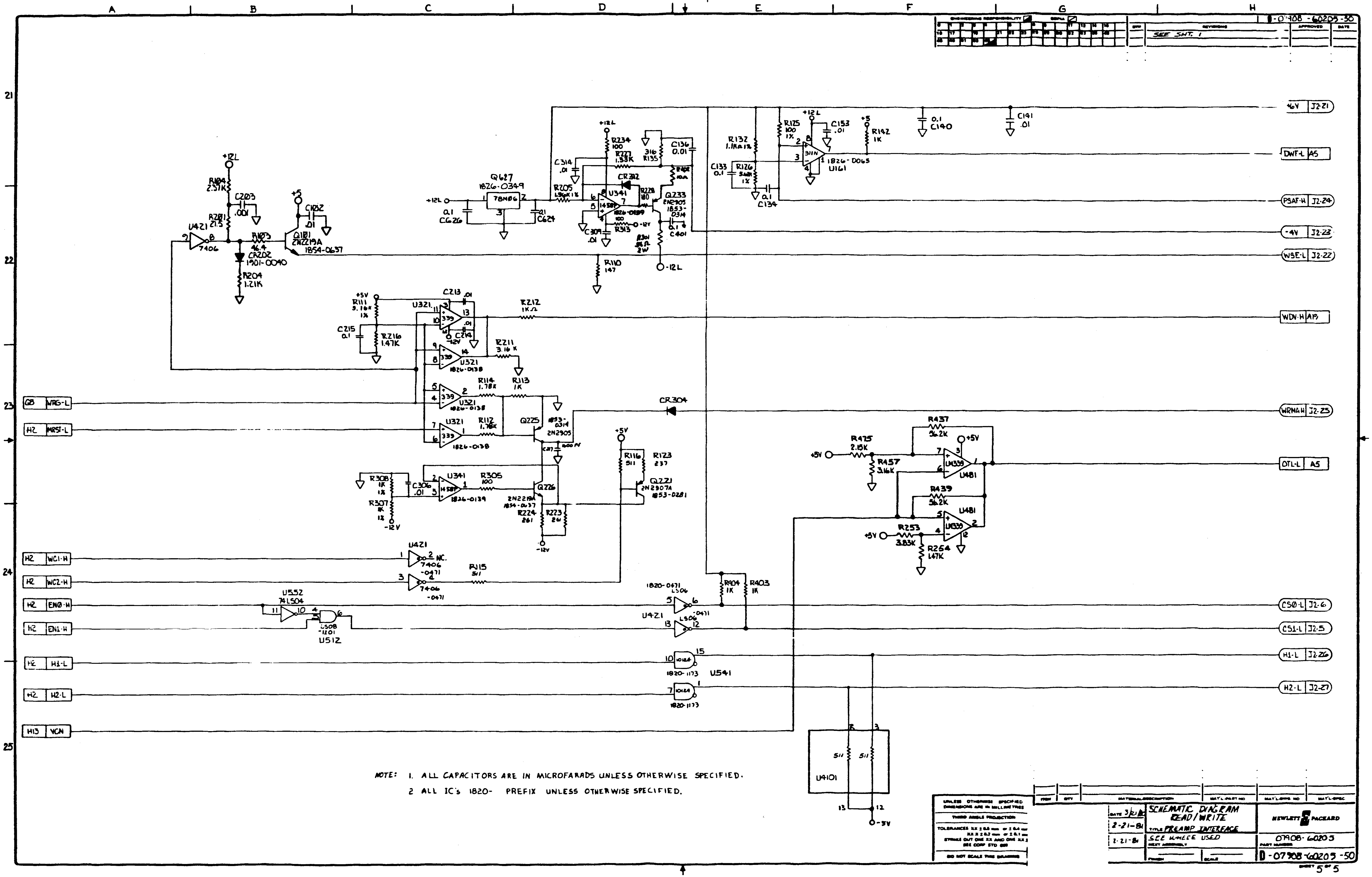

SYNC BIT GENERATOR
MFM FORMATTER
300 BYTE SECTOR TIMING COUNTER
COUNT Ø-9 = Ø
COUNT 10-300 = 1
COUNT Ø-11 = Ø
COUNT 12-300 = 1
COUNT Ø-21 = Ø
COUNT 22-199 = 1
COUNT 200-300 = Ø
COUNT Ø-299 = Ø
COUNT 300- = 1
AQML
SYNH
DTPH
DTPL
SOSH
SOSL
IDXL
VCO-H
RWC-L
RWC-H
DS-H
RWS-H
WRT-H
WDTL
WDA-H
RCD-H
RCD-L
WRG-H
WRG-L
AQM-L
SYNL
SYN-H
DTP-H
SOS-H
SOS-L
IDX-L
F2-L
INDX-L
U6102
SEE SHT. 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
SCHEMATIC DIAGRAM READ/WRITE
SECTOR TIMING/FORMATTER
9-30-80
2-21-81
SEE WHERE USED
HEWLETT PACKARD
01908-60207
D-07908-60205-50
SHEET 2 OF 5



DATA INPUT MUX
DUAL-EDGED MONOSTABLE
PHASE DETECTOR
PULSE SWALLOWER
DATA TRIGGER
SEPARATOR
LOOP FILTER
VCO
WAVE FORMS WHEN DATA LEADS TREFL
0= MFM MODE 1= SYNC MODE
VCO SYNC FIELD BITS
DATA FIELD SYNC BITS
DATA BIT
DATA TRIGGER SYNCS RWC HERE
SEPARATOR TIMING
NOTE: 74LS629 CAN DRIVE 12 74'S' LOADS
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
SCHEMATIC DIAGRAM, READ/WRITE
DATA TIMING / DATA SEPARATOR
SEE WHERE USED
HEWLETT PACKARD
07908-60203



SCHEMATIC DIAGRAM
READ/WRITE
READ CHAIN
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
HEWLETT PACKARD
07908-60205
D-07908-60205-50
SHEET 4 OF 5
SEE SHT. 1
5-22-80
2-21-81
SEE WHERE USED
U381 NE592 1826-0164
CA3146 1858-0052 U181
1854-0295 SD4465 Q152
Q157 1854-0295 SD4465
CA3146 1858-0032 U301
U4101
AM686 U4102
U2101 1458
UNUSED
Q605 MC 7905.2CT 1826-0215
J2-33 DX-H
J2-32 DY-H
H7 RCD-H
H7 RCD L
H22 WDV-H
RDA-H A11
TP187 SIG H
SIGL
AGC TP188
+5V TP151
GND TP173
P2-1,2 +12V
P2-3,4 +5V
P1-47,48 +5V
P1-49,50 -12L
P2-49,50 GND
P2-7,8,25,26 GND
P1-1,2,25,26 GND
P1-45,46 GND
J2-31,34,17 PA GND
+12L
+5V
-5V
-12L
GND
PRE-AMP GND
.01 — C302, C303, C406, C408, C428, C435, C444, C447, C501, C502, C514, C515, C519, C523, C524, C525, C526, C528, C529, C602, C616, C623, C628, C484, C520, C532, C553
10µF SOLID TANTALUM



NOTE: 1. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

2 ALL IC's 1820- PREFIX UNLESS OTHERWISE SPECIFIED.

SEE SHT. 1

SCHEMATIC DIAGRAM READ/WRITE

TITLE PREAMP INTERFACE

SEE WHERE USED

HEWLETT PACKARD

07908-60205

D-07908-60205-50

SHEET 5 OF 5

P/N 07908-60009

DISC MEMORY ACCESS (DMA) PCA-A4

. Series Code D-2302

HEWLETT-PACKARD CO. /hp/

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline). (G39)

LTR	REVISIONS	DATE	INIT	MF
A	AS ISSUED	12-4-81	db/RGE	M
B	REVISED PER DCO 48-6198	02-25-83	sd/JSK	M
C	ADDED 7914 PER DCO 48-6268	04-05-83	sd/JSK	M

A	ISSUED	ba/JK	12-14-81	MODEL SEE PAGE ONE | STK # SEE PAGE ONE
B	48-6198		02-18-83	DMA INTERNAL MAINTENANCE SPECIFICATION
C	48-6268		04-05-83	BY | DATE DEC 1, 1981
LT	P.C. #	APPR	DATE	APPD | SHEET # 1 OF 73
REVISIONS				SUPERSEDES | DWG # A-5955-3497-1

HEWLETT-PACKARD CO. / hp /

DMA INTERNAL MAINTENANCE SPECIFICATION
FOR THE
DISC MEMORY ACCESS BOARD OPERATION

07908-60009
07912-60010
07930-60001

TABLE OF CONTENTS

DMA INTERNAL MAINTENANCE SPECIFICATION

1 SCOPE

This IMS details operation of the DMA (Disc Memory Access) board (07908-60009), (07912-60010), and the (07930-60001).

2 RELATED DOCUMENTS

2.1 Self Test ERS

2.2 DMA Micro-Diagnostics

2.3 DMA/F/S/ECC Interface Specification

2.4 PHI (1AA6-6004) Data Sheets

3 BLOCK DIAGRAM

3.1 Overall Perspective

The DMA board's purpose is to provide serial/parallel data conversion, provide an HP-IB interface to the disc/tape, buffer data between the disc/tape back-up and the host computer, and implement the cyclic redundancy check for data integrity on disc transfers. The DMA board has three separate external interfaces. (See Figure 1). The F/S/ECC/DMA interface consists of a serial data path with associated control lines. This interface is used to access the disc or tape back-up. The HP-IB interface is used to interface the disc/tape to the host computer through the IEEE Standard 488 Bus. The micro-processor interface gives the Z-80 based micro-processor board the ability to control data transfers through the DMA. This interface also allows the micro-processor access to the HP-IB for command interpretation/execution.

3.2 Micro-processor Interface

The micro-processor interface consists of 12 address lines (A0-H through A11-H), 8 data lines (D0-H through D7-H), 2 control lines (RD-L and WR-L), and 3 select lines (BUFSE-L, IOSE-L, and DMASE-L). The three select lines allow the MPU (micro-processor unit) access to: (1) Data Buffer Ram, (2) PHI (HP-IB interface chip) registers and, (3) DMA Control/Status registers and Header Ram.

3.2.1 Data Buffer Ram

The Data Ram consists of 4K bytes of static Ram. This ram is accessible by the MPU only when data transfers are not in progress. To access this Ram with the MPU, the BUSCNCTL bit of Control register 2 must be set = 0.

3.2.2 PHI REGISTERS

The PHI is mapped as eight I/O ports when accessed by the MPU. These eight ports correspond to the eight internal registers of the PHI chip as outlined in the PHI (1AA6-6004) data sheets. To access the PHI registers with the MPU, the PHICNCTH bit of control register 2 must be set = 1. The PHI must be accessed by the MPU only when data transfers between HP-IB and Data Ram are not in progress. However, Data transfers between HP-IB and Data Ram can be interrupted to allow MPU access of PHI Registers by the following control sequence.

1) Set DMAENH = 0 (Control Byte 2)

2) Set PHICNCTH = 1 (Control Byte 2)

3) Make the desired access to any PHI register except register 2.

4) Set PHICNCTH = 0 (Control Byte 2)

5) Set DMAENH = 1 (Control Byte 2)

The above sequence must be accomplished in four separate writes to control byte 2, to avoid bus conflicts.

3.2.3 DMA Control/Status registers and Header Ram

The DMA select line along with five address bits are decoded by the DMA hardware to provide 32 memory mapped ports. Of these 32 ports, the first 16 ports allow access to the 16 bytes of Header Ram. The remaining 16 possible addresses are decoded only enough to provide 8 control registers (write registers) and 6 status registers (read registers).

3.3 Detailed Block Description

Now for a look at the internal workings of the DMA, from a more detailed point of view. For the following explanation refer to Figure 2.

3.3.1 PHI and HP-IB Drivers

The PHI is used to transfer bytes of data across the HP-IB. The MPU will normally set up the direction of transfer and certain control options to allow the transfer to take place. During a Write operation data is transferred from the HP-IB to the Data Ram. A Read operation allows data transfer from Data Ram to the HP-IB. Once the proper direction and control bits are set up the MPU starts the PHI/Data Ram transfer by asserting DMAENH and IOENH of Control register 2. Only Register 2 (FIFO) of the PHI is ever accessed by the DMA function. The MPU can access any of the 8 PHI registers, but only after connecting the PHI address and data buses as illustrated in the previous section. The PHI address and control lines are multiplexed between the MPU and the DMA byte control. The PHI data bus can be accessed by the PHI LATCH or the MPU since either source can be tri-stated. The PHICNCTH bit (Control register 2) is used to switch control between the MPU and the PHI LATCH. The HP-IB Drivers buffer all HP-IB signals to/from the PHI chip. These driver chips exhibit the high current drive required to talk on the multi-device bus.

3.3.2 PHI LATCH

The PHI Latch consists of 10 bits of bi-directional register. This register acts as a holding register for one data byte plus two control bits during DMA data transfer. The two control bits are decoded by the DMA (Write operation) to differentiate between data bytes, secondary command bytes, and last data byte (data byte tagged with EOI). These two control bits are used to tag the last byte during a Read operation with EOI. Data bytes in transit between PHI and the Data Ram must pass through the PHI Latch. Because of the PHI's relatively slow access time, the PHI Latch provides extra time for a byte to be extracted from or deposited into the PHI's FIFO. In effect, any byte transferred to/from the PHI during a disc access must steal a cycle from the disc. Since the minimum disc byte time could be as short as 720 nsec, (7912) the PHI cycle must be as short as possible to allow time for a disc cycle at least once every 720 nsec.

3.3.3 Header Ram

The Header Ram consists physically of two bipolar 16X4 ram chips arranged as 16 bytes of very fast (35 nsec. access time) read/write memory. This ram is used to store the preamble and postamble information during each sector of disc access. The disc address counter is designed to access the lower 6 bytes of Header Ram at the beginning of each sector then increment into the Data Ram address field (256 bytes). After the data field, the disc address counter will wrap around into the first seven bytes of the Header Ram. Figure 3a illustrates the sector format of the data on the disc. During a disc write operation the 6 bytes of preamble are taken from the Header Ram. The disc address counter is preloaded to Hex address 0FA (see Figure 3b) and increments through the data field to Hex address 1FF. At this point the lower 9 bits of the disc address counter wrap around to the postamble (Hex address 000).

If a Fullsector transfer has been selected (FULSECL = 0 of Control register 1), the two CRC bytes are taken from the Header ram. The DMA board also sends the 5 bytes of ECC from the Header ram. These 5 bytes are replaced by the proper ECC bytes if the ECC circuit is present, otherwise, these 5 ECC bytes are written to the disc with the data contained in the Header ram. During a disc read operation the Preamble, CRC, and ECC bytes are read into the Header ram. This occurs independent of the value of the FULSECL bit.

The Header ram should only be accessed by the MPU if (1) a DMA data transfer is not in progress, or (2) during DMA data transfers, only when the disc address counter is addressing the Data field (DATFH = 1 of Status register 2). Header ram access at times other than those mentioned above will cause data bus conflicts and possible damage to the DMA board.

3.3.4 Data Ram

The Data Ram consists of 4K bytes of static NMOS Ram. Since each disc sector consists of 256 bytes of data, the Data ram is capable of buffering 16 sectors of data enroute to or from the disc. This ram is effectively converted into a two port ram by multiplexing the disc and I/O address counters during data transfers. All Data enroute to or from the disc/tape must pass through the Data Ram.

3.3.5 Disc Address Counter

The disc address counter is a 13-bit counter used to address the Header and Data ram during data transfers between the disc and DMA. The lower 9 bits of this counter are used to address the two rams within each sector as explained in the Header ram section previously. These bits of the counter are automatically loaded with Hex address 0FA prior to the start of each sector. The four most significant bits of this counter are used to determine which sector of the Data ram will be accessed in the next transfer initiated. The value of these four MSB's are clocked into a holding register at the beginning of each sector by the Start of Sector (SOSH) signal.

This allows the MPU the option of changing the sequence of sectors transferred to or from the disc or tape. If a non sequential order of sectors is required (by interleaving or disc/tape copy data operations) the MPU must load the four MSB's of the Disc address counter with the desired sector number prior to the SOSH of the next sector transferred to/from the disc/tape. If the data is to be transferred in normal sequential sector order no intervention by the MPU is necessary.

The MPU can write a value for the four most significant bits into the counter. It can also read the value of these bits.

3.3.6 I/O Address Counter

The I/O Address Counter is a 12-bit counter used to address the Data ram during data transfer between the Data ram and the PHI. This counter can be loaded with a 12-bit value (two separate write operations) by the MPU. It's content can also be examined by the MPU (two separate read operations).

3.3.7 I/O Byte Counter

The I/O Byte Counter is a 12-bit down counter which provides a means of stopping the transfer of data over the HP-IB at a predetermined byte count. Before the data transfer is started, the host computer will tell the MPU how many bytes of data to expect in the transfer. This total byte count will be divided by 4096 (maximum count with a 12 bit counter) and the remainder loaded into the I/O Byte Counter. The integer portion of the quotient from the above division is actually the number of times the I/O byte counter will wrap around to the remainder number to which it was loaded. Now, the MPU keeps track of how many sectors it has transferred to/from the disc and when it is 16 sectors from the end of the transfer, the MPU will set the ISTPENH bit (Self Test register). When the I/O byte counter counts down to zero with the ISTPENH bit set the DMA will halt data transfer over the HP-IB and signal the MPU that byte count has expired.

The MPU does not have the speed required to keep track of the byte count on a byte by byte basis. It does, however, save hardware to let the MPU keep track of how many 16 sector blocks have been transferred.

3.3.8 SERDES (Serializer/Deserializer)

The SERDES is the place that serial data from the disc is changed to parallel bytes for buffering and subsequent transfer over the HP-IB. And you're right, it is also the place where the parallel data enroute to the disc gets changed to a serial data stream.

3.3.9 F/S-ECC-DMA INTERFACE

The Formatter/Separator-Error Correction Code-Disc Memory Access Interface is basically the serial data path interface between the DMA and either the Formatter/Separator or the ECC. The interface is defined in the F/S-ECC-DMA Interface specification. As far as the DMA is concerned. this interface consists of the following 5 lines: (1) Start of Sector (SOSL) (2) Start of Data (SODL), (3) Read/Write Clock (RWCL), (4) Read Data (DINH), and (5) Write Data (DOUTH). The normal sequence of events in a disc read or write is as follows: (1) SOSL is asserted as a low true pulse. This tells the DMA to get ready to transfer a sector. (2) SODL is asserted as a low true pulse. This tells the DMA that the serial data stream is starting on the next RWCL edge. The first actual data bit may be delayed several clock edges from SODL depending on the direction of transfer. (3) Serial data is clocked into or out of the DMA until the end of the sector is reached. (4) SOSL for the next sector is received which either resets the DMA or continues the transfer depending on MPU activity during the previous sector.

3.3.10 DMA Byte Control

The DMA Byte Controller is in charge of all data byte movement within the DMA board. It consists of two ROM based state machines, a sector counter, and other appropriate logic to accomplish the above task.

The larger ROM based state machine (hereafter referred to as the DMA Controller) controls data transfer between the SERDES and Data Ram as well as the data transfer between the Data Ram and PHI LATCH. This state machine handshakes directly with the smaller state machine to synchronize data transfer through the PHI LATCH.

The smaller state machine (referred to as the PHI Controller) controls data transfer between the PHI LATCH and the PHI. Both state machines run on an internally generated 12MHz clock.

The sector counter is a 5-bit up/down counter which prevents incoming data from overrunning the Data in the Ram. These 5 bits are readable by the MPU providing the firmware with the capability of overrun handling on disc reads/writes. In the case of a disc read, the sector counter is incremented after each sector is read from the disc and decremented after each sector (or partial sector if the last sector does not contain 256 bytes) is transferred over the HP-IB. For a disc write, the sector counter is incremented after the sector is received from the HP-IB and decremented after each sector is written to the disc. During a disc read, HP-IB data transfer is automatically held off by the sector counter when the Data ram becomes empty and does not resume until at least one full sector is read in from the disc. Also, during a disc write, the HP-IB data transfer is held off by the sector counter when the Data Ram becomes full and does not resume until at least one sector (256 bytes) of room is available.

3.3.11 SERDES Control

The SERDES Control module controls loading and shifting of the serializing/ deserializing shift register. It is responsible for synchronizing the DMA to the NRZ data at the beginning of each sector. It also generates byte service requests sent to the DMA controller. This module consists of a bit counter to define the byte boundaries plus the SERDES to DMA controller handshake circuitry. It functions as a data path switcher in conjunction with the Sector Control module in switching the CRC bytes into the data path at the proper time.

3.3.12 Sector Control

The Sector Control module serves one basic function. It decodes the disc address count to obtain an end of sector signal used to accomplish certain tasks near the end of the sector. Included in these tasks are the CRC data path switching and SERDES reset pulse.

3.3.13 CRC

The Cyclic Redundancy Code generator/checker provides data error detection in the serial data portion of the disc interface. During a Write operation the serial data (6 Header bytes and 256 Data bytes) is clocked through the CRC generator. From this generation, 16 bits of Cyclic Redundancy Code is appended to the end of sector. On read back of this sector, the serial data is passed through the CRC checker. If no errors occurred, the checker will be filled with zeroes after the last CRC bit is clocked in. If an error occurs at least one bit will be set in the 16 bit CRC shift register.

4 LOGICAL OPERATION

This section will cover in detail each function of tne DMA. The DMA can be conviently broken into two major blocks. One block deals with data transfer between the Data Ram and the Disc, henceforth referred to as the Disc Interface. The other consists of data transfer between the Data Ram and the HP-IB, referred to as the I/O Interface. This discussion will begin with the Disc Interface starting at the disc/tape interface and proceed through the Buffer Ram, then to the I/O Interface.

4.1 Disc Interface

The Disc Interface runs synchronous to RWCL which in the case of a disc write is derived from the servo clock or some clock that is actually synchronous to the serial data being written to the disc. In the case of a read, the clock is usually derived from the data being read from the disc.

4.1.1 SERDES Control Module

The SERDES Control Module (See Fig. 4) controls start up of the disc read or write. It also generates signals to control shifting/loading of registers in the SERDES. This module is the source of signals initiating the disc byte handshake (DISCRQH) to the ROM based state machine. Timing diagrams for the beginning of the disc read and write sequence are illustrated in figures 5 and 6 respectively. The Interface read/write clock (RWCL) is buffered/inverted for use on the DMA board and referred to as buffered read/write clock high (BRWCH). With the exception of DINH and Latched Start Of Data (LSODH), all Disc Interface flip-flops are clocked with the positive edge of BRWCH.

The sequence of events encountered during a normal disc read will now be discussed. Referring to Figure 5, if the MPU has enabled the DMA for a read in the next sector, Start Of Sector (SOSL) negative edge will set DISCGOH (U9112-5) B31. This will remove all clears from U9112-14 C31 and U9122 F31 allowing the next Start Of Data (SODL) to be latched as Latched Start Of Data high (LSODH U9122-9) C31.

Six positive edges of the BRWCH later, Data Go (DATAGOH, U9121-9) F32 goes high swinging the DMA into action for the disc read. These six clock cycles are required to compensate for bit delays caused by the interface and the three (garbage) sync bits written at the beginning of each sector. A bit counter (U8121) G32 is used to frame each byte. It is loaded with the count of one until DATAGOH goes high. At this time, the bit counter starts counting. When the count of eight is reached, the bit counter issues an End Of Byte (EOBH) pulse and reloads to the count of one.

The timing diagram of Fig. 5 shows the position, in relation to SODL, of the serial data at three locations along the read path. DINH is the serial data at the edge card connector. S1,S2,S3 signify the three sync (garbage) bits generated during the disc write. D1,D2 etc. represent the first, second and so on data bits of the sector. Note that Latched Data In High (LDINH, U9102-9) B23 is the data sampled at the midpoint of each data bit allowing both hold and set-up time to the flip-flop. Deserializer bit 0 (RCRCH) represents the LSB of the deserializing shift register U982-15 F23. During a disc write, DATAGOH goes high only one clock cycle after SODL is asserted (see Fig. 6). This is because the DMA is the source of the serial data during a write and no delay other than the three sync bits are introduced by the DMA. Again, the bit counter functions the same as it does during a read. Write CRC (WCRCH, U981-12) F22 is the MSB of the serializing shift register. This shift register is held in the load mode until DATAGOH goes high. At this point, the shifting of the serial data is started. The DOUTH flip-flop U992-5 C24 is held in the preset mode to shift out the three sync bits as zeros until DATAGOH goes high.

4.1.2 Handshake Module

The Handshake Module (see Fig. 4) controls the interface between serial data (synchronous to the read/write clock) and byte wide data (synchronous to the internal 12 MHZ clock). This module is composed of three flip-flops and various gates.

During a disc read, each EOBH from the bit counter clears disc request F/F U7101-2 G35. The Q output of this F/F going low asserts DISCRQH through U891-9 H33. When the DMA Controller services this DISCRQH by transferring that byte from SERDES to Buffer Ram, it sets F/F U7101-2 G35 completing the handshake for that byte. During a disc write, F/F U7101-2 G35 accomplishes the DISCRQH handshake function in the same way as it does for the read. However, because the DMA is the Data source on a write, the first two data bytes of each sector must be treated as special cases. This is accomplished by the two F/F's of U7121 G33. The first byte of each sector is requested by DISCGOH going high (derived from SOSL). This transition clears F/F U7121-1 G33 providing the first DISCRQH. The second byte of each sector is requested by DATAGOH (9121-9) F32 going high. This transition clears F/F U7121-2 G34 providing the second DISCRQH (U891-10) H34.

4.1.3 Serializer

The Serializer consists of an 8-bit holding register and an 8-bit shift register. During the write, a byte is written (upon request) into the 8-bit holding register sometime prior to the time it will be shifted out by the shift register. The next positive edge of BRWCH after EOBH goes high loads the shift register with the byte being held in the holding register. The holding register consists of U971 G24 and U972 G24. The shift register serves a dual purpose as both a Serializing and Deserializing shift register. It consists of two 74LS195, U981 F23 and U982 F24. Serial data out of the Serializing shift register is fed into two multiplexors. One Mux (U9101-1) E34 selects either the output of the CRC (for the two CRC bytes) or the serial data as the source of the serial data out. The other Mux (U9121-2) A33 selects the serial data out or serial read data in as the source of the input to the CRC.

4.1.4 Deserializer

The Deserializer consists of an 8-bit shift register (physically the same parts as the Serializing shift register) and an 8-bit holding register. During a read, the serial data is shifted into the deserializing shift register, and at the end of the byte, it is loaded into the holding register. Sometime during each byte, the DMA controller extracts the byte from the holding register and transfers it to the Buffer Ram. Note that the shift register (U981 and U892 F23) and the holding register (U871 G22) are synchronous to BWRCH. The tri-state outputs of the holding register are enabled onto the Serdes/Buffer Data Bus (SBD0H-SBD7H) by Serdes Output Enable (SOEL) which is synchronous to the 12 MHZ clock.

4.1.5 CRC

The Cyclic Redundancy Checker (CRC) implements the popular CRC-16 polynomial used in many of HP's disc drives. An equivalent circuit for the CRC-16 polynomial is given in figure 7. This circuit is implimented by using the eight F/Fs of a 74LS273 U8131 A35 and C35 and a 74LS166 U9131 B34.

During a write, the serial data is fed into the CRC generator until the last bit of the data field has been clocked in. At this point, the output data Mux (U9101) E34 is switched to clock the 16 bits in the CRC shift register out as the two CRC bytes. If the fulesector (FULSECL of Control register 1) bit is asserted the output data Mux will not switch in the two CRC bytes. The source of the CRC bytes will then become the Header Ram. This gives the DMA the ability to write a sector with a bad CRC value during diagonistics and check the CRC function during read back.

During a read, the serial data is fed into the CRC checker until the last bit of CRC is clocked in. At this point, the input to the CRC is disabled. If no data error has been detected, all 16 F/F's of the CRC shift register will contain zeroes. If any detectable error has occurred at least one of the 16 F/F's will contain a one. Now, by enabling the input to the CRC Error F/F (U691-1) F35 and shifting the CRC bits out one at a time as inputs to this F/F any value of one will be latched as a CRC error.

4.1.6 Sector Control Module

The Sector Control Module (see Fig. 8) controls events that happen near the end of a sector on a read or write to the disc. The disc address counter gives the Sector Control Module an input at the end of the data field of each sector. This input (Control End Of Data - CEOD-H) is a decode of the disc address counter lower 9 bits (1FF hex). CEOD-H is shifted into an eight-bit shift register (U9111) C32 by EOBH+1 (End of Byte + 1 bit). Various taps are taken off this shift register corresponding to certain byte times. These taps are used to control such functions as Multiplex the CRC bytes (U9111-4 & 6) C32 into the data path, latch the CRC error signal (U9111-12) C32, and reset the DATAGOH signal (U9111-12 for Read, U9111-13 for Write). Timing for these control signals can be seen in Figures 9,10,11, and 12. In figure 9 the MUXCRCL signal is derived from two of the outputs of the eight bit shift register (U9111) C32.

This signal is used to multiplex the two CRC bytes into the data path on the disc write. Again, referring to figure 9, the SHHDL (U9101-6, Shift Hold) signal is used to hold the serializing register in the shift mode after DATAGOL returns high. This assures the last few bits of ECC-5 have been shifted out of this register. Figure 10 is a continuation of figure 9. Here QG is inverted to give RQENH (Request Enable, U8111-8) D33. This signal disables any further DISCRQH's from being generated by EOBH. RSTDGOL (Reset Discgo, U8101-11) D32 is derived from QH going low and EOBH+1. This pulse resets F/F U9112-1 B31 (DISCGOH) which in turn clears other F/F's in the Byte Control Module.

Figure 11 shows where QB is essentially the signal that allows the output of the CRC to enter the D input of the CRC error F/F (U691-1) F35. Since the CRC shift register will be filled with zero's (no error) or contain at least one (error) after the last CRC check byte has entered the shift register, enabling the output to be clocked into the CRC error F/F for at least 16 clocks will assure a complete sampling of the CRC shift register.

Figure 12 illustrates the position of the Reset Discgo (RSTDGOL) and Request Enable (RQENH) signals for a disc read.

4.1.7 Disc Address Counter

The Disc Address Counter is a 13-bit counter used to address the Buffer Ram during transfers to/from the disc. This counter is broken into two sections. The most significant four bits address which sector of the sixteen sectors of Data Ram will be used during the next transfer. These four bits consist of a four-bit counter (U231) A11 and a four-bit register (U321) C11. The counter is incremented each time the disc address counter transitions through the header/data field boundary (low 9 bits count from 0FF hex to 100 hex). This only occurs if a sector is actually being transferred to/from the disc. The count at the output of the counter is loaded into the four-bit register at the start of the sector (clocked by BSOSL positive edge).

The lower 9 bits (U421 A14, U221 A13, and U581-1 A15) are used to address the byte location of each byte in a disc sector. These 9 bits are loaded to a starting address of 0FA hex at the beginning of the sector (see figure 3). During the sector transfer, this counter is incremented by INCENH (Increment Enable). This signal is an output of the DMA controller state machine which is high for one 12 MHZ clock cycle at the end of each disc byte transfer. At the end of each sector, the lower 9 bits of this counter are loaded to 0FA hex in preparation for the next sector.

4.1.8 Header Ram

The Header Ram is composed of 16 bytes of fast bipolar ram (U821 F8 and U831 F6) This ram is used for preamble and postamble storage during Disc transfers. The Header Ram is accessible by the MPU any time no transfer is in progress or anytime the disc address counter is addressing the Data portion of a sector (i.e. disc address counter lower 9 bits = 1XX hex). The Header Ram has separate input and output data buses. The ram chips invert the data internally which is why the output data bus buffers are inverting tri-state buffers (U841 F9 and U851 H9) while the input buffers are non-inverting multiplexors (U731 F8 and U721 H8). U721 H8, U731 F8, and U851 H10 allow the MPU assess to the header ram data bus at times specified above. While U731 F9, U721 H8 and U841 F9 allow the DMA controller access to the Header Ram during disc transfers.

4.2 I/O Interface

The I/O Interface is the part of the DMA that is responsible for the transfer of data bytes between the HP-IB and the Data Ram. Also included in this section is the DMA Controller and Sector Counter. These two modules actually tie the I/O and Disc Interfaces together.

4.2.1 I/O Address Counter

The I/O Address Counter provides the byte ram address during an I/O transfer. This counter is 12 bits wide and can be loaded as well as read by the MPU (see figure 8). This counter is composed of three 74LS191's (U541 E13, U621 E12, and U531 E12). All three counters are always counting up. The counter is incremented by DADSEH (Disc Address Select, U4111-14 E4). This signal goes low at the start of an I/O cycle. It serves the dual purpose of multiplexing the address counter onto the Buffer address bus as well as providing the positive edge that increments the I/O address counter.

4.2.2 I/O Byte Counter

The I/O Byte Counter is composed of three 74LS191's (U511 D13, U611 D12, and U521 D12 (see figure 8). This counter is physically identical to the I/O Address Counter. Its function is somewhat different, however. This counter is used to provide a byte count expiration or stop signal to the DMA controller. In the command to execute a normal transfer, the host CPU will designate the length of the transfer in bytes. It then becomes the disc drives responsibility to stop upon completion of the transfer. The counter provides the stop signal by use of modulo arithmetic. Before the start of the I/O transfer, the MPU loads the I/O Byte Counter with the remainder of the result obtained from dividing the Total byte count by 4096 (12 bit counter). The I/O Byte counter, operating in the down count mode, is decremented each time an I/O byte is transferred. While the sector, precisely 16 sectors prior to the last sector of the transfer, is being transferred to/from the disc, the MPU will enable the I/O stop signal by asserting ISTPENH (I/O Stop Enable, U661-5 E19). When the I/O byte counter is decremented to zero and ISTPENH is high, IOSTOPH (I/O Stop, U491-12 C13) is asserted. This signal tags the last byte with an EOI (End Or Identify) being sent over the HP-IB in the case of a disc read. It also halts the DMA from receiving any more bytes over the HP-IB in the case of a disc write.

4.2.3 Data Ram

The Data Ram is composed of 4K bytes of static ram used strictly for data buffer during data transfers (U911 C8 and U912 C7). This ram receives its address from three sources: (1) MPU, (2) Disc Address Counter, and (3) I/O Address Counter. The MPU can only access the Data Ram when no data transfer is in progress. To access the Data Ram, the BUSCNCTL bit (Bus Connect of Control Register 2, U461-15 C19) must be low. This bit controls the tri-state buffers of the address counter multiplexor (U411 F14, U211 E14, and U311 D14) and the MPU Buffer Address buffers (U941 B6 and U951 B7). The Data Ram is effectively a two port ram during data transfer because the DMA controller transfers I/O bytes and Disc bytes to/from the ram to/from different physical locations within the Data Ram.

4.2.4 Phi Latch

The Phi Latch is a bi-directional buffer register composed of (U151 E28, U161 E28, and U261 E30). This register is used to hold one byte of data enroute to the PHI FIFO (disc read) or just extracted from the PHI FIFO (disc write). This buffering is necessary because of the PHI chip's relatively slow access time during data transfers. The Phi Latch also provides a data interface between the DMA controller and the PHI controller. During a transfer from the HP-IB to the Data Ram, the Phi controller extracts a byte from the PHI and clocks it into the the PHI Latch (U261 E30). It then signals the DMA controller that a byte is available in the PHI Latch. The DMA controller enables the tri-state outputs of the PHI Latch onto the Serdes Buffer Data bus (SBD0H-SBD7H), then it writes this data into the Data Ram.

During a transfer from Data Ram to HP-IB, the DMA controller enables the output of the Data Ram onto the Serdes Buffer Data bus and then clocks this byte into the PHI Latch (U151 E28 and U161 E30). The DMA controller then signals the PHI controller that a byte is available in the PHI Latch. The PHI controller then clocks this byte into the PHI FIFO. More detailed explanation of the actual control of this latch can be obtained from the discussion on the DMA and PHI controllers.

4.2.5 Sector Counter

The Sector Counter is a five-bit up/down counter responsible for assuring no data is lost due to Data Ram overruns. This counter counts from zero to sixteen. Each count is equivalent to one sector of data having been transferred. The sector counter indicates that the buffer is full at the count of 16. The count of zero indicates an empty buffer. To illustrate the internal workings of the Sector Counter it is easier to look at what happens during a read and write separately. During a disc read, the sector counter is incremented by the disc and decremented by the I/O. The Sector Counter is composed of a 74LS191 U371 E1) and a 74S112 (U481-2 G1). Both are clocked by the 12 MHZ clock and count is enabled at the appropriate times. The enable input of the 74LS191 must be asserted for only one clock cycle each time it is required to count. This accounts for the combinational logic required to control the enable input. The counter is incremented and decremented on the following conditions:

Incremented

1. After each sector has been entered into the Buffer Ram during a read.

   Exceptions

   a. CRC error during the read.
   b. Uncorrectable ECC error during the read (assumes ECC present).
   c. Formatter error during the read. (assumes the formatter is designed with a FUNERL (formatter error) line)

Decremented

1. Each time a full sector of data has been sent over the HP-IB.

2. If the last sector is a partial sector, the byte count expiration will decrement the counter.

During a write the sector counter is incremented by the I/O and decremented by the disc. The direction of the count is determined by the value of DADSEL (Disc address select low). This signal becomes DOWNH as it is selected by WRITEH in the multiplexor U471 D2. The count enable (CNTENH/L) signals are again only asserted for one clock cycle (12 MHZ) at the appropriate time to increment/decrement the counter. The Sector Counter is decremented or incremented during a write as follows:

Incremented

1. Each time a full sector of data has been received over the HP-IB.

Decremented

1. After each complete sector has been written to the disc.

Exceptions:

Again CRC error, ECC uncorrectable error and Formatter error would disable the count enable circuitry. However, these errors do not normally occur during a disc write.

4.2.6 DMA Controller

The DMA Controller is basically a ROM based state machine in control of all data transfers between the PHI Latch, Data Ram, and SERDES. This state machine runs at a 12 MHZ clock frequency. Its inputs are all either already synchronous to the 12 MHZ clock or are synchronized to this clock by a 74S175 (U4121 B3). One 512X8 PROM (U4101 D4) performs the next state decoding logic of the state machine. Burn pattern for this PROM is given in Figure 16. The five outputs of the state machine are held in U5101 E3. These outputs are described as follows:

1. SOEL - (Serdes Output enable)

   This signal enables the output drivers of the Deserializer register (U871 G22) to let the deserialized byte of data from the disc, drive the Serdes Buffer Data bus.

2. SWRL - (Serdes Write)

   This signal clocks the data present on the Serdes Buffer Data bus into the Serializer holding register (U971 G23 and U972 G24). The positive edge of this signal does the clocking of the register.

3. PBWRL - (Buffer Write)

   This signal clocks the data present on the Serdes Buffer Data bus into either the Data Ram or Header Ram (depending on which is selected by the disc address counter).

4. PBOEL - (Buffer Output Enable)

This signal enables the output drivers of either the Data Ram or Header Ram. The Serdes Buffer Data bus is then driven with the addressed Ram data byte headed for either the PHI Latch or the SERDES.

5. PHIGOL - (PHI GO)

This signal serves a dual purpose. During a write, PHIGOL enables the output drivers of the PHI Latch (U261 E30) letting it drive the Serdes Buffer Data bus. During a read, PHIGOL clocks the data of the Serdes Buffer Data bus into the PHI Latch (U161 E28 and U151 E28).

The present state holding register is three out of the four F/F's contained in a 74S175 (U4111 E4). By constraining the changes of all inputs except Disc Request (DRQH) and I/O Request (IORQH), to state 0 it is possible to actually achieve more than eight states with only three feedback or present state variables. The state diagram for the DMA Controller is shown in figure 13.

The five bits making up the state number in the state diagram are:
VRFYH, WRITEH, U4111-7, U4111-2 AND U4111-15.

4.2.7 PHI Controller

The PHI Controller is a ROM based state machine that controls the transfer of data between the PHI Latch and the PHI FIFO (Register 2). This state machine is clocked by the same 12 MHZ clock that runs the DMA Controller. The next state decoder logic is done by a 32X8 PROM (U2121 B30). The burn pattern for this PROM is given in Figure 17. This state machine has only two outputs as follows:

1. IOGOL/H - (I/O Go)

This signal serves two purposes. Its main task is to clock data bytes into or out of the PHI chip. This signal goes through multiplexor U4131-1 B26 to drive the chip select and IOGO pins of the PHI chip. During a write, the positive edge of IOGOL clocks the byte on the PHI Data bus into the PHI Latch (U261 E30). During a read operation, this signal enables the PHI to accept the byte from the PHI Latch (U151 E28 and U161 E28) already present on the PHI Data bus.

2. STIORQH - (Set I/O Request)

This signal sets the handshake F/F (481-1 H3) between the DMA Controller and the PHI Controller. By setting this F/F the PHI Controller is able to tell the DMA Controller that (1) a byte is available in the PHI Latch (write) or (2) the PHI Latch is empty (read).

The state machine has three feedback or present state variables. They are held by three F/F's of a 74S175 (U2131 C30). The state diagram for this state machine is illustrated in figure 14. Note the outputs are indicated to the right of the state in which they occur. The vertical arrows associated with each output indicate an assertion level and have nothing to do with a voltage. For example, the arrow pointing up associated with STIORQ indicates that the signal is asserted upon entering states 110 and 011.

The arrow pointing down indicates STIORQ is deasserted upon leaving states 100 and 011. in other words, STIORQH (active high) is a logical one only during states 110 and 011. For a second example, the signal IOGO is asserted in states 101 and 011. It remains asserted until the state machine enters state 111 where it becomes deasserted. Thus, since IOGOL is actively low, it becomes a logical zero upon entering state 101 or 011 and it remains a logical zero during the sequences 101, 100, 110, 010 and 011, 001, 000. Upon entering state 111 from either 000 or 010 IOGOL returns to a logical 1 and remains there until a transition to either state 011 or 101 occurs.

Inputs to the state machine are indicated next to the transition arrows between states. Where no inputs are shown next to a state transition arrow, it is assumed the transition to the state indicated by the arrow will occur on the next rising edge of the 12 MHZ clock. As seen in figure 14, the PHI Controller has three inputs. Again, no reference is made to voltage levels when referring to inputs on the state diagram. The definition of the three PHI Controller inputs is given below.

WRITE - Direction of data flow (U4121-10 B3)(i.e. WRITE = data goes from PHI to PHI Latch, WRITE not = data goes from PHI Latch to PHI).

IORQ - Service request from the PHI Latch (U481-5 G3) (i.e. during a read operation, a byte is available in the PHI Latch or during a write operation, room is available in the PHI Latch for a byte).

PHIRQ - Service request from the PHI (U581-9 B27) (i.e. during a read operation, room is available for a byte in the PHI FIFO, or during a write operation, a byte is available in the PHI FIFO).

The three bits making up the state number in the state diagram are really the three feedback variables which represent the present state of the machine (U2131 C30 pins 7, 10, and 15).

4.2.8 End Of Transfer Sense Circuitry

The End Of Transfer Sense Circuitry halts the I/O process from four different sources. The I/O process completes normally or halts in an error state under the following conditions: (1) Receive a byte over the HP-IB tagged with EOI (normal completion if accompanied with No. (2); (2) Byte count expiration during a write (normal completion if accompanied with No. 1 above); (3) Receive a Secondary Command over the HP-IB before receiving a byte tagged with EOI or having the byte count expire (this is always an error condition); or (4) Byte count expiration during a read (normal completion during a read). Each of these four cases will be dealt with separately.

(1) Receive byte tagged with EOI.

If the byte read from the FIFO of the PHI is tagged with EOI, PHI Data Bit 0 (PHID0H) will be high. As this byte is clocked into the PHI Latch by the PHI Controller, F/F 4 of the 74LS175 (U3111 B28) will be set. This signal (EORTH - End Of Receive Transfer, U3111-15 B28) disables any further byte available signals (from the PHI's FIFO) from asserting a need for service by the PHI controller. As this EOI byte (now in the PHI Latch) is written into the Data Ram, by the DMA Controller, F/F 4 of the 74LS175 (U3101 C28) becomes set. This signal (REIO - Receive EOI) is one of the status bits (Status register 1) available to the MPU. When set, this signal tells the MPU that the last byte (tagged with EOI) is in the Data Buffer.

(2) Byte count Expiration during a write

During a write, if the ISTPENH (I/O Stop Enable) bit is asserted, and the I/O Byte Counter decrements to zero (Byte Count expired), IOSTOPH (I/O Stop, U491-12 C13) is asserted. This signal is clocked into F/F 2 of the 74LS175 (U3101 C28) as the byte is transferred from the PHI Latch to the Data Ram.

The output of this F/F called WTAFH (Write That's All Folks, U3101-7 C28) is latched by the next rising edge of the 12 MHZ clock into F/F U691 G5. The output of this F/F (U691-9 G5) is called NWTAFH (New Write That's All Folks). It is used as a status bit to the MPU to indicate byte count expiration during a write. Relax, we're still not done. At this point during a write, the PHI Controller has stopped accepting bytes from the PHI. The DMA Controller, however, has not been told anything about the transfer being finished. In fact, the DMA controller has been deliberately lied to concerning this event. By not terminating the DMA Controller, and at the same time disabling the DMA Controller's ability to reset the handshake F/F (U481-1 H3), the remaining bytes in the sector are filled with the value of the byte count expiration byte. This phenomenon is explained later in the section under Security Circuit.

(3) Secondary Command without byte count expiration or EOI

During a disc write, should a secondary command arrive in the inbound FIFO of the PHI without a byte count expiration or a byte tagged with EOI, an error condition exists. This error condition is decoded by the DMA board and the following action taken. The I/O is halted and the MPU is notified (SECH bit of Status register 1 is set). The value of the secondary command is written into the Data Ram by the DMA in the next sequential location after the last data byte received from the HP-IB. The Sector Counter is not incremented, keeping the MPU from writing the sector containing the secondary byte onto the disc. The Secondary Command is decoded from the two high order bits of the PHI data bus. The value of 01 on PHID0H and PHID1H respectively decodes to a secondary command received.

(4) Byte Count expiration during a Read Operation

During a read, the first byte clocked into the PHI Latch after IOSTOPH becomes asserted will set WTAFH. As this byte is transferred from the PHI Latch to the PHI FIFO, WTAFH is clocked into F/F 2 of U3111 B28. This signal RTAFH (Read That's All Folks) signals the MPU that all requested bytes have been sent to the host computer. Also during a read, PHI data bit 0 and 1 are being driven by two of the tri-state drivers contained in U631 D28. When WTAFH is low (no byte count expired) these two data bits are driven low indicating a data byte being transferred over the HP-IB. When WTAFH goes high, PHI Data bit 0 goes high. This tells the PHI to tag that byte with an EOI as it is sent over the HP-IB. Note that WTAFH signals the PHI to tag the last byte with EOI but RTAFH does not signal the MPU that the transfer is complete until the last byte is actually transferred from PHI Latch to the PHI FIFO.

4.2.9 Security Circuit

The purpose of the Security Circuit is to fill the sector of any partial sector write with the value of the last byte at byte count expiration. This feature is needed to eliminate any security problems. The security problems could arise from the fact that all data is buffered in Ram on the DMA board. Therefore, a person could effectively retrieve someone else's data by writing a partial sector and then reading back the full sector. The security circuit consists of a three state, two F/F state machine that senses the byte count expiration and abnormally controls the DMA Controller's stop mechanism.

The state diagram for this state machine can be seen in figure 15. The present state variables are indicated by the binary number inside each circle. These variables represent the states of the two state machine flip/flops (U6111 G5). U6111-2 is the MSB of the number indicated in the circles. State 00 is entered any time the I/O is not enabled (PIOEN') or any time the DMA is in the Read mode (WRITE'). These inputs are indicated by the straight arrow pointing to state 00 in fig. 15. State 00 is the only state used while in the Read mode (i.e. the circuit is only activated during a write). Once the I/O process has been enabled by the MPU (PIOEN asserted), the state machine is free to accept and act on the Write That's All Folks input (WTAF). A state transition occurs (state 00 to state 01) upon receipt of a WTAF (i.e. byte count expiration). Upon entering state 01, HSHLD (HandShake Hold) is asserted. This signal holds off all further handshakes between the DMA and PHI controllers. This forces the DMA controller to continue extracting a byte from the PHI Latch (the last byte of the transfer over and over until the sector is filled). At the end of the sector WRAP (I/O address counter wrap around) is asserted. This forces the state transition from state 01 to state 11. Upon entering state 11, WDONE (Write Done) is asserted. This signal terminates the DMA I/O process (i.e. no further bytes are written from the PHI Latch to the Data Ram. The Security state machine stays in state 11 until the MPU disables the I/O process (PIOEN deasserted). At that time the state machine is forced to state 00 to wait for the next transfer.

5.0 MNEMONIC DEFINITIONS

A0-H through A11-H - (microprocessor address bus).

ATN-L - (attention) Attention HP-IB control line.

BAD0-H through BAD11-H - (buffered address bus). The address bus that addresses the Data Ram.

BFUL-H - (buffer full). The 16 sector data ram is full of data.

BOE-L - (buffer output enable) Data and Header Ram output enable.

BRWC-H - (buffered read/write clock) Serial data read/write clock from the read/write board. (buffered on the DMA board).

BSOD-H - (buffered start of data) Indicates the start of the data during a disc sector (i.e. first header bit or thereabouts).

BSOS-L - (buffered start of sector) Indicates the beginning of a disc sector.

BUFSE-L - (buffer select) Data ram select line from the processor.

BUSCNCT-H/L - (bus connect) Connects the Data Ram to the microprocessor when active.

BWR-W/L - (buffer write) Data and Header Ram write enable.

CA0-H through CA4-H - (control address bus) Buffered A0-H through A4-H used by the DMA to address header ram, status registers and control registers.

CD0-H through CD7-H - (control data bus) The buffered microprocessor data bus. Once buffered it becomes a write only bus (i.e. one directional).

CEOD-H - (control end of data) Indicates the last byte of data (data field) has been transferred to/from the SERDES.

CLR-L (clear security state machine) Clears the security state machine every time PIOEN-L or WRITE-L are high (i.e. all the time during a read and only when the I/O enable is off during a write).

CNTEN-H/L - (count enable) Enables the sector counter to count on the next rising edge of the 12 MHZ clock.

CNTL1-L - (control one select) Port select for control register one.

CNTL2-L - (control two select) Port select for control register two.

CRCER-L - (CRC error) Indicates that the sector had a data error during a read.

CRCRST-L - (CRC reset) Resets the CRC error flag.

CRD-L - (control read) Buffered RD-L control line from the processor, used on the DMA.

CS-L - (chip select) Selects the state machine proms. (i.e. allows the DTS-70 to tri-state these proms during testing).

CWR-L - (control write) Buffered WR-L from processor used on the DMA.

D0-H through D7-H - (microprocessor data bus)

DA0-H through DA11-H - (disc address counter address bus) Input to address multiplexor.

DAC-H - (data accepted) Data accepted HP IB control line.

DADSE-H/L - (disc address select) Indicates the buffered address bus is being driven by the disc address counter vs. the I/O address counter.

DATAGO-H/L - (data go) Indicates a disc sector transfer is in progress.

DATF-H/L - (data field) Indicates the disc address counter is currently addressing the data portion of the sector.

DAV-L - (data valid) Data valid HP-IB control line.

DCEN-H - (disc enable) Enables the next disc sector to be transferred. (opposite polarity of DEN-L)

DDONE-H - (disc done) Indicates that the disc sector is complete.

DEN-L - (disc enable) Enables the next disc sector to be transferred. Set by the microprocessor.

DGO-H - (disc go) DEN-L after being clocked by start of sector. (i.e. present sector operation).

DIN-H - (data in) Serial read data line.

DIO1-L through DIO8-L - HP-IB data bus

DISCGO-H - (disc go) Asserted after SOS-L if a disc sector transfer is to be accomplished.

DISCRQ-H - (disc request) Request for service from the SerDes. (i.e. a byte is available in the Deserializer or room is available in the Serializer).

DMAEN-L - (DMA enable) Enables the PHI controller to begin operation.

DOUTEN-L - (data out enable) Enable for the tristate write data driver.

DOUT-H - (data out) The serial data out (i.e. enroute to the read/write board or ECC chip).

DOWN-H/L - (down) Direction of count for the up/down sector counter.

DRQ-H - (disc request) Service request from the SERDES, synced to 12 MHZ.

EMPT-H - (empty) The Data buffer is empty (i.e. contains less than one sector of data.)

EOB-H/L - (end of byte) Asserted for one bit time at the end of each byte during the serializing/deserializing process.

EOB+1-H (end of byte plus one) End of byte above plus one bit time.

EOI-L (end or identify) HP-IB control line.

EROR-L - (error) Either a FUNER-L or UNER-L occurred during the last sector.

EORT-H - (end of receive transfer) Indicates a byte tagged with EOI has been transferred from PHI to PHI Latch.

FULSEC-L - (full sector) Commands a full sector write. (i.e. the CRC bytes come from the header ram instead of the CRC generator)

FUNER-L - (formatter error) Indicates that an error occurred in the read/write board after a disc sector had begun transfer.

HD0-H through HD7-H - (header ram data bus) Header ram output data bus.

HD0-L through HD7-L - (header ram data bus) Header ram input data bus.

HDRSE-L - (header select) Selects the header ram vs. the data ram during a disc transfer.

HSHLD-H - (handshake holdoff) Disables the reset of the handshake F/F by the DMA controller. (i.e. used to finish filling a partial sector on an I/O write).

IFC-L (interface clear) HP-IB control line.

INCEN-H - (increment enable) Increment enable for the disc address counter.

IOA0-H through IOA11-H - (I/O address bus) The data and header ram address bus prior to becoming the buffered address bus. (i.e. the output of either the disc address counter or I/O address counter.)

IOEN-H - (I/O enable) Processor I/O enable bit after it has been synced to 12 MHZ.

IOGO-H - (I/O go) PHI chip enable as driven by the PHI controller.

IOHOLD-L - (I/O hold) Holds off any further I/O transfer until a sector of data is available in the data ram (read) or room is available for a sector of data in the data ram (write).

IORQ-H/L (I/O request) Handshake F/F output between the two DMA state machines.

IOSE-L (I/O select) Processor select line to select the PHI chip.

IOSTPH-L - (I/O stop load high) Loads the I/O byte counter high nibble. (i.e. processor decode of this write register)

IOSTPL-L - (I/O stop load low) Loads the I/O byte counter low nibble. (i.e. processor decode of this write register)

IOSTOP-H/L - (I/O stop) Indicates the last byte of HP-IB transfer has been done.

ISTPEN-H - (I/O stop enable) Enables the byte count expiration to stop the I/O process.

ISTP-L - (I/O write stop) Stops the I/O write at the end of a sector boundry.

LOAD-H/L - (load disc address counter) Pre-loads the disc address counter to 0FA hex prior to the start of a disc transfer.

MRST-L - (master reset) Power on master reset.

NMI-L - (non-maskable interrupt) Interrupt line tied to the non-maskable interrupt of the processor.

NWTAF-H (new write that's all folks) Latched WTAF-H.

PHICNCT-L - (PHI connect) Connects the PHI to the processor.

PHID0-H through PHID1-H - (PHI data bus) The high 2 bits of the PHI 10 bit data bus.

PHID8-H through PHID15-H - (PHI data bus) The lower 8 bits of the PHI data bus.

PHIGO-L - (PHI go) DMA PHI Latch enable line. (i.e. clocks a byte into the PHI Latch or enables the output of the PHI Latch)

PHIINT-L - (PHI interrupt) The PHI generated interrupt. Connected to the non-maskable interrupt of the processor.

PIOEN-H/L - (processor I/O enable) Enables the I/O data transfers.

PVRFY-H - (processor verify) Specifies a disc verify. (i.e. with this bit asserted the next disc transfer will be a disc read regardless of the state of the PWRITE bit. Data will only be written into the header ram during this disc read, however.)

PWRITE-H - (processor write) Control bit that specifies the direction of data transfer (i.e. asserted = disc write, not asserted = disc read)

RCRC-H - (read CRC) Serial data just prior to the CRC module during a read.

RDAD-L - (read disc address counter) Port select to read the high nibble of the disc address counter.

RDGO-H - (read go) Indicates a disc sector read will be performed on the next or present transfer.

RD-L - (read) Microprocessor read control line.

REOI-H - (receive EOI) Indicates a data byte tagged with end or identify has been received over the HP-IB.

RESET-L (reset) Buffered master reset.

RFD-H - (ready for data) HP-IB control handshake line.

REN-L - (remote enable) HP-IB control line.

RIOADH-L - (read I/O address high) Port select to read the high nibble of the I/O address counter.

RIOADL-L - (read I/O address low) Port select to read the low byte of the I/O address counter.

RTAF-H - (read that's all folks) Indicates that the last byte during a read has been sent to the PHI.

RWC-L - (read/write clock) The read/write clock used to clock in the serial data during disc operations.

RWRK-L - (revision/rework select) Port select for the revision/rework register.

SBD0-H through SBD7-H - (serdes buffer data bus) Data bus connecting the Data Ram, Header Ram, PHI Latch, and SERDES.

SCNT0-H through SCNT3-H - (sector counter outputs) The low nibble of the sector counter.

SECLD-L - (sector counter load) Processor load signal for the sector counter.

SECRST-L - (sector counter reset) Load data bits for the sector counter low nibble. This one line is connected to all four bits.

SEC-H - (secondary command) Indicates a secondary command has been received.

SHHD-L - (shift hold) Controls the shift/load function of the SERDES shift register.

SOD-L - (start of data) Indicates that the serial data stream is about to start.

SOE-L - (SERDES output enable) Output enable for the SERDES holding register during a disc read.

SOS-L - (start of sector) Indicates that the disc sector is about to begin. Comes a little before SOD-L.

SRQ-L - (service request) Service request (serial poll) HP-IB signal.

STAT1-L - (status one) Port select to read status byte one by processor.

STAT2-L - (status two) Port select to read status byte two by processor.

STIORQ-H - (set I/O request) Sets the Handshake F/F requesting service from the PHI state machine.

SWR-L - (SERDES write) Write enable for the SERDES holding register during a disc write.

TRASH-L - (trash) This signal assures that the three garbage bits at the beginning of each sector are zero. (i.e. it holds the write data F/F clear).

12 MHZ-H/L - (12 mega hertz clock) Internal state machine clock.

UNER-L - (uncorrectable error) Indicates that the ECC was unable to correct the data error in the sector just sent.

VRFY-H/L - (verify) The processor verify bit synced to 12 MHZ.

WCRC-H - (write CRC) Serial data line just prior to CRC entry.

WDAD-L - (write disc address counter) Processor load enable for the high nibble of the disc address counter.

WDAT-L - (write data) Serial data line which eventually becomes DOUT.

WDONE-H - (write done) Indicates the sector is filled in which a byte count expiration occurred.

WIOADH-L - (write I/O address counter high) Processor load enable for the high nibble of the I/O address counter.

WIOADL-L - (write I/O address counter low) Processor load enable for the low byte of the I/O address counter.

WRAP-H/L - (wraparound) Indicates that the I/O address counter has just wrapped around. (i.e. 256 bytes have been transferred over the HP-IB).

WRGO-H - (write go) Indicates a disc write operation. (i.e. a decode of WRITE and VRFY.)

WRITE-H/L - (write) The processor write bit synced to 12 MHZ.

WR-L - (processor write) Write control line from the processor.

WTAF-H - (write that's all folks) Indicates that the byte count has expired during a disc write operation.

DMA REGISTERS

Read Registers

HDMA'RIO'L - F350H

```
--------------------------------------------------------------------------
[               LOWER BYTE OF I/O ADDRESS COUNTER                        ]
--------------------------------------------------------------------------
```

HDMA'RIO'U - F351H

```
--------------------------------------------------------------------------
[ SODL   SOSL   DINH   RWCL][UPPER NIBBLE OF I/O ADDRESS COUNTER ]
--------------------------------------------------------------------------
```

HDMA'RDISC - F352

```
--------------------------------------------------------------------------
[                          ][UPPER NIBBLE OF DISC ADDRESS COUNTER]
--------------------------------------------------------------------------
```

HDMA'REV'NUM - F353H

```
--------------------------------------------------------------------------
[                          ][ REWORK NUMBER  ][ FUNERL    DOUTH  ]
--------------------------------------------------------------------------
```

HDMA'STAT'1 - F354H

```
--------------------------------------------------------------------------
[ WDONH   REOIH  SECH   RTAFH  NWTAFH  HPIB2H  HPIB1H   HPIB0H   ]
--------------------------------------------------------------------------
```

HDMA'STAT'2 - F355H

```
--------------------------------------------------------------------------
[ CRCERL  ERORL  DATFH  SECT4H SECT3H  SECT2H  SECT1H   SECT0H   ]
--------------------------------------------------------------------------
```

Write Registers

HDMA'WSTOP'L - F350H

```
-----------------------------------------------------------------
[               I/O STOP ADDRESS    (LOW BYTE)                  ]
-----------------------------------------------------------------
```

HDMA'WSTOP'U - F351H

```
-----------------------------------------------------------------
[                              ][ I/O STOP ADDRESS (HIGH NIBBLE) ]
-----------------------------------------------------------------
```

HDMA'WIO'L - F352H

```
-----------------------------------------------------------------
[               I/O ADDRESS COUNTER (LOW BYTE)                  ]
-----------------------------------------------------------------
```

HDMA'WIO'U - F353H

```
-----------------------------------------------------------------
[                              ][I/O ADDRESS COUNTER (HIGH NIBBLE)]
-----------------------------------------------------------------
```

HDMA'WDISC - F354H

```
-----------------------------------------------------------------
[                              ][DISC ADDRESS COUNTER (HIGH NIBBLE]
-----------------------------------------------------------------
```

HDMA'STEST - F355H

```
-----------------------------------------------------------------
[ISTPENH ][  3 BITS NOT USED  ][ DINH     SODL     SOSL     RWCL  ]
-----------------------------------------------------------------
```

HDMA'CNTRL'2 - F356H

```
-----------------------------------------------------------------
[ 3 BITS NOT USED  ][ BUSCNCTL  PHICNCTH  DMAENH  IOENH   DENH   ]
-----------------------------------------------------------------
```

HDMA'CNTRL'1 - F357H

```
-----------------------------------------------------------------
[ WRITEH  VRFYH  STH  CRCRSTL   DOUTENH FULSECL SECRSTL  SECLDL ]
-----------------------------------------------------------------
```

Data Ram - D000H TO DFFFH

Header Ram - F340H TO F34FH

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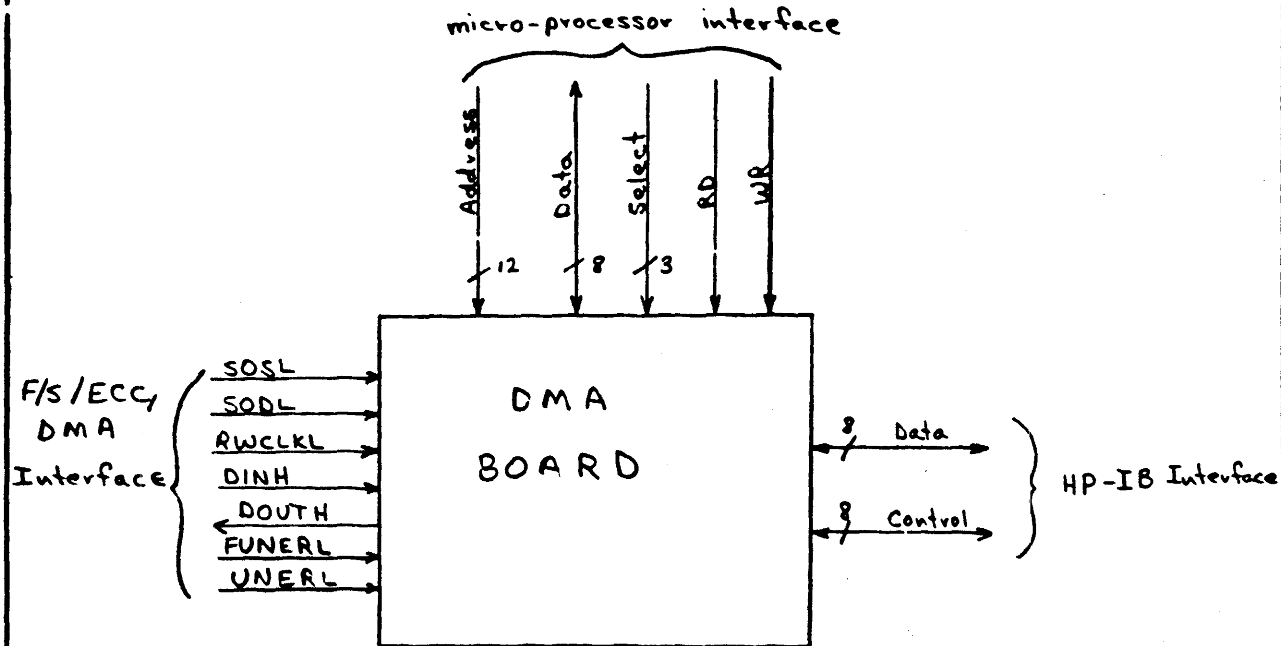


Fig. 1 DMA Interface Block Diagram

				MODEL	STK NO
				BY	DATE 12-1-81
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 55 OF 73
	REVISIONS			SUPERSEDES	DWG NO A-5955-3497-1

9320-2789 FORMERLY 0-700024

HEWLETT-PACKARD CO.

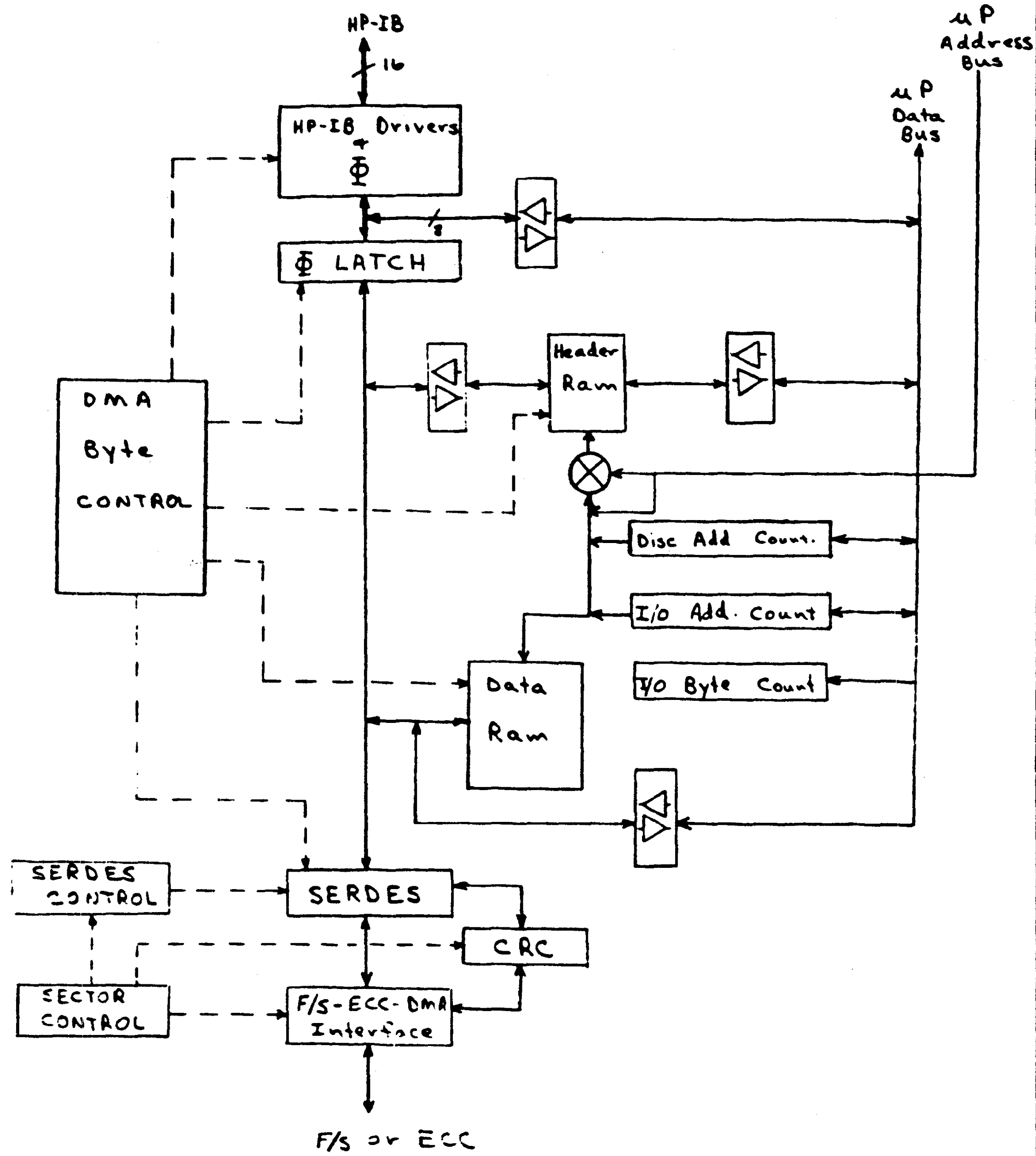
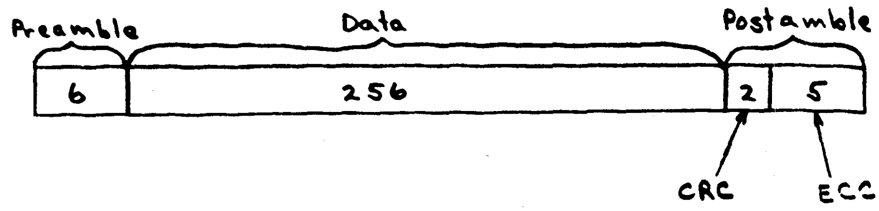


Fig. 2 DMA Detailed Block Diagram

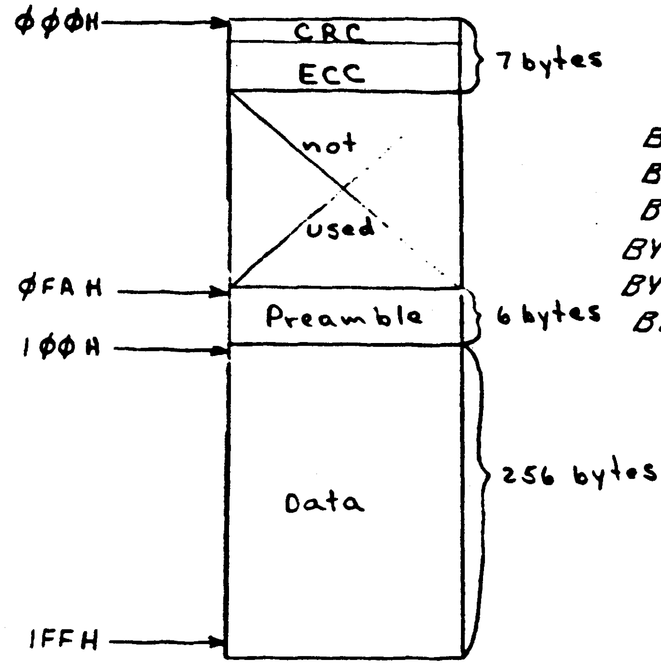
MODEL		STK NO	
BY		DATE	12-1-81
APPD		SHEET NO	56 OF 73
SUPERSEDES		DWG NO	A-5955-3497-1

LTR	PC NO	APPROVED	DATE
	REVISIONS		

HEWLETT-PACKARD CO.



(a)



PREAMBLE

BYTE 1 - STATUS BYTE
BYTE 2 - SECTOR NO.
BYTE 3 - HEAD NO.
BYTE 4 - CYLINDER# LOW
BYTE 5 - CYLINDER# HIGH
BYTE 6 - SPARE SECTOR

(b)

Figure 3 (a) Disc sector format.
(b) Disc sector as it exists in CNF RAM.

				MODEL	STK NO	
				BY	DATE	12-1-81
				APPD	SHEET NO	57 OF 73
LTR	PC NO	APPROVED	DATE			
	REVISIONS			SUPERSEDES	DWG NO	A-5955-3497-1

9320-2788 (FORMERLY D-700024)

HEWLETT-PACKARD CO.

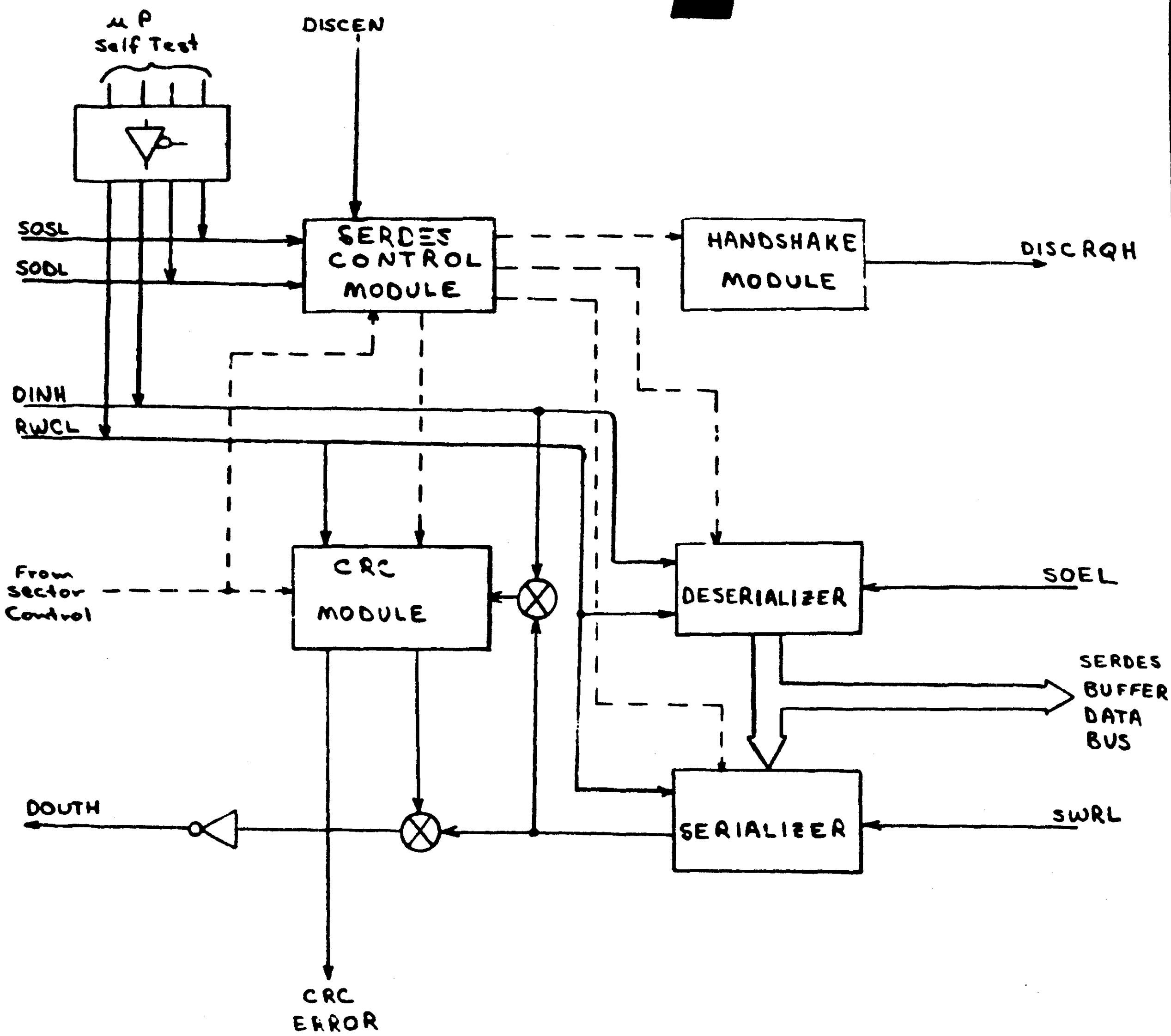


Fig. 4. Disc Interface Block Diagram

LTR	P C NO	APPROVED	DATE	MODEL	STK NO
REVISIONS				BY	DATE 12-1-81
				APPD	SHEET NO 58 OF 73
				SUPERSEDES	DWG NO A-5955-3497-1

9320-2788 (FORMERLY 0-700024)

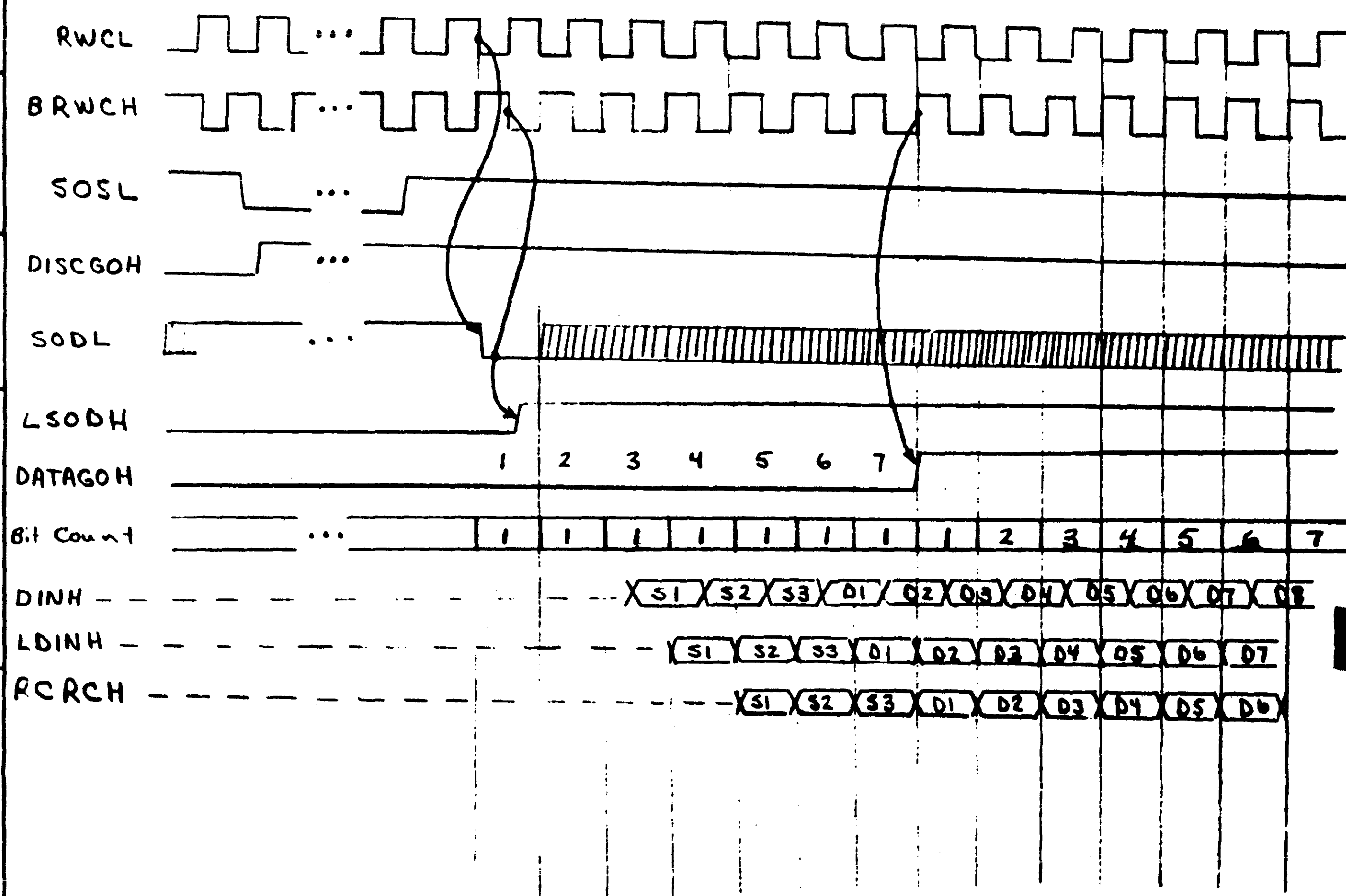


Fig. 5 Beginning of the sector timing for Disc Read

HEWLETT-PACKARD CO.

DATE 12-1-81

SHEET NO 59 OF 73

DWG NO A-5955-3497-1

HEWLETT-PACKARD CO.

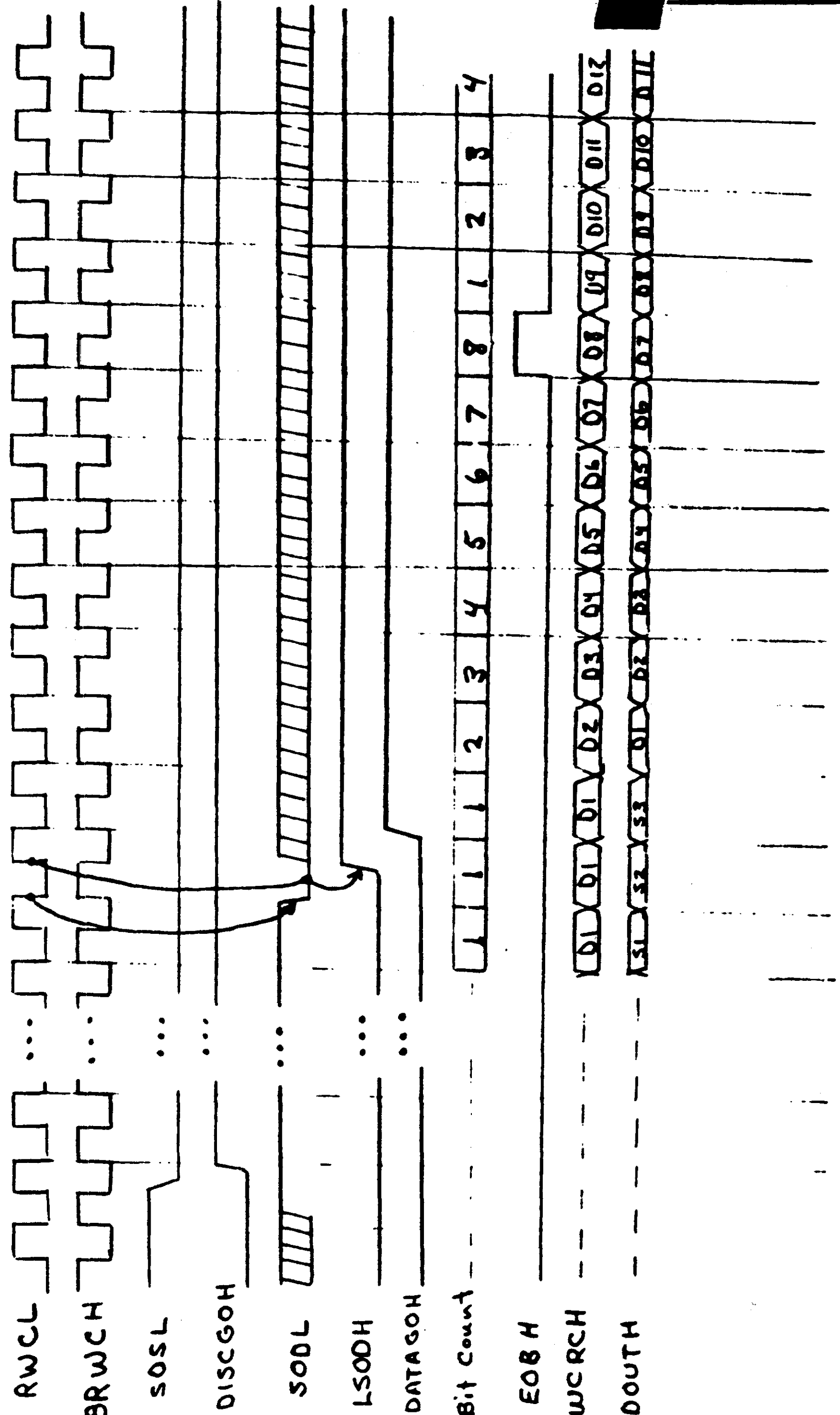


Fig. 6 Beginning of the sector timing for Disc WRITE

LTR	PC NO	APPROVED	DATE	MODEL	STK NO
REVISIONS				BY	DATE 12-1-81
				APPD	SHEET NO 60 OF 73
				SUPERSEDES	DWG NO A-5955-3497-1

HEWLETT-PACKARD CO.

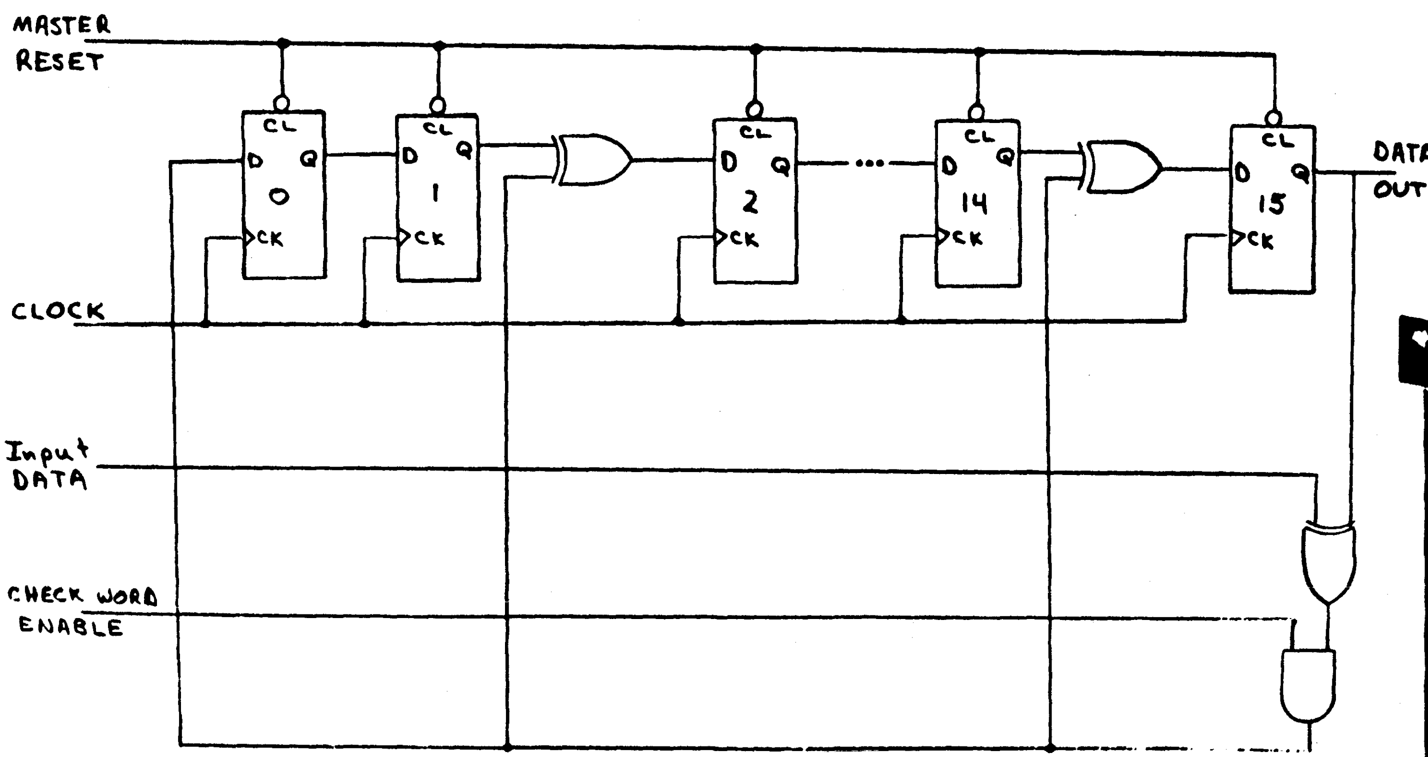


Fig. 7. Equivalent circuit for CRC-16 ($X^{16}+X^{15}+X^2+1$)

REVISIONS | LTR | PC NO | APPROVED | DATE
SUPERSEDES | APPD | BY | MODEL | STK NO
DATE 12-1-81
SHEET NO 61 of 73
DWG NO A-5955-3497-1
9320-2788 (FORMERLY 0-7002#)

HEWLETT-PACKARD CO.

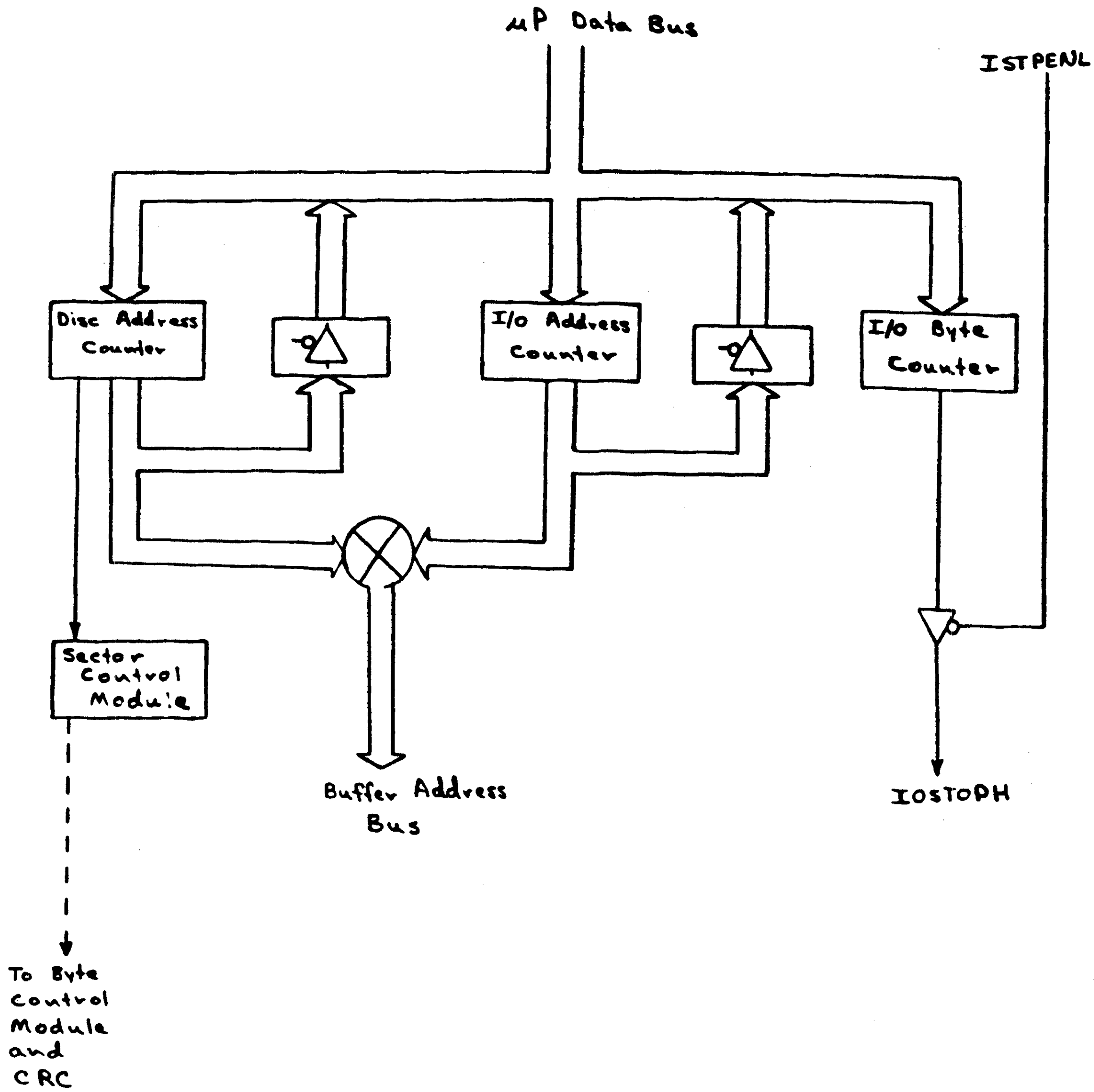


Fig. 8. Buffer Address Counters

				MODEL	STK NO	
				BY	DATE	12-1-81
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO	62 OF 73
	REVISIONS			SUPERSEDES	DWG NO	A-5955-3497-1

9320-2789 (FORMERLY 0-700024)

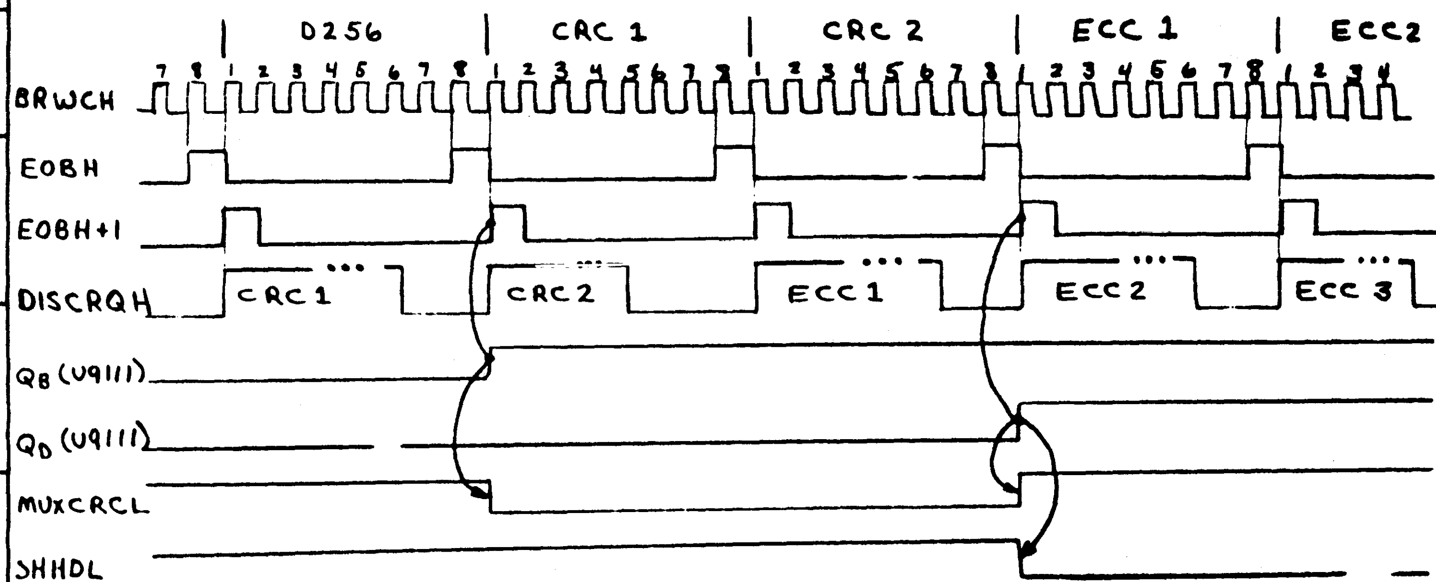


Fig. 9. End of Sector Timing for a Disc Write.

HEWLETT-PACK. RD CO.

REVISIONS | LTR | PC NO | APPROVED | DATE

SUPERSEDES | APPD | BY | MODEL | STK NO

DATE 12-1-81

SHEET NO 63 OF 73

DWG NO A-5955-3497-1

9320-2780 (FORMERLY 0-7002)

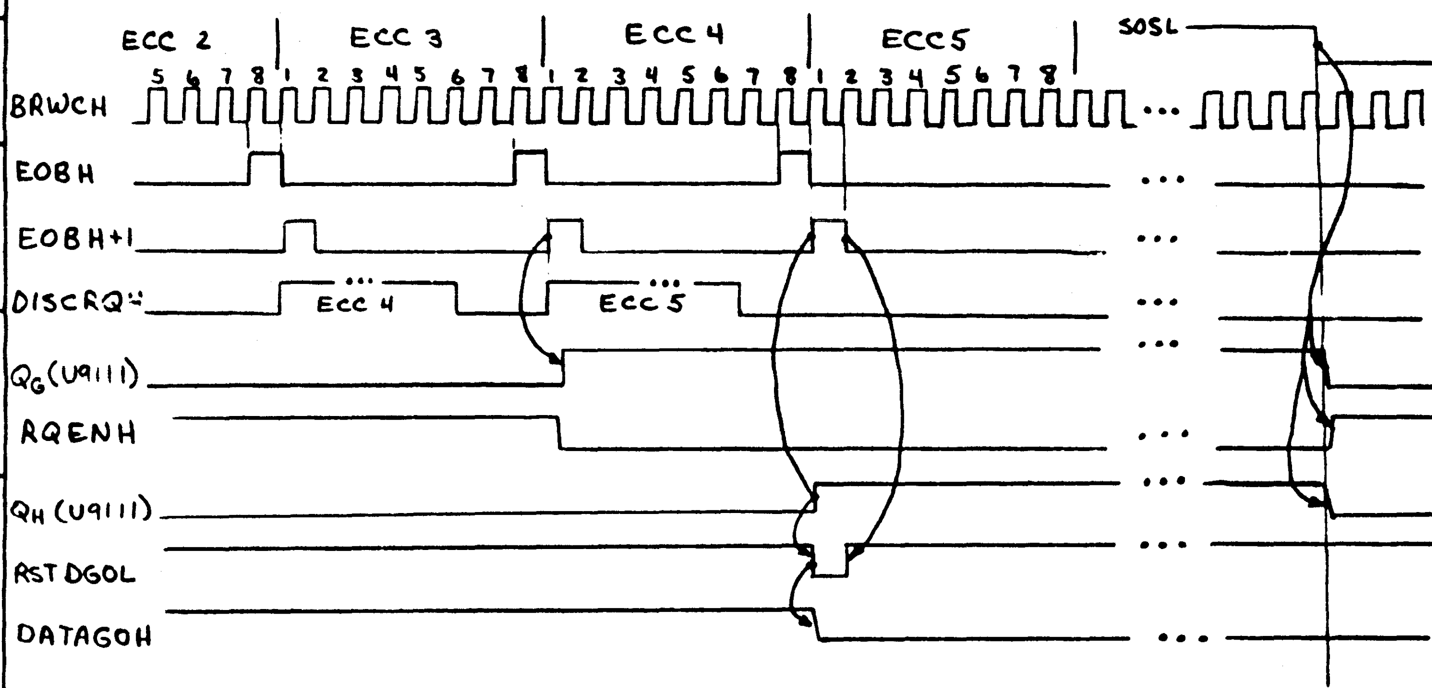


Fig. 10. End of Sector Timing for Disc Write.

HEWLETT-PACKARD CO.

DATE 12-1-81
SHEET NO 64 OF 73
DWG NO A-5955-3497-1

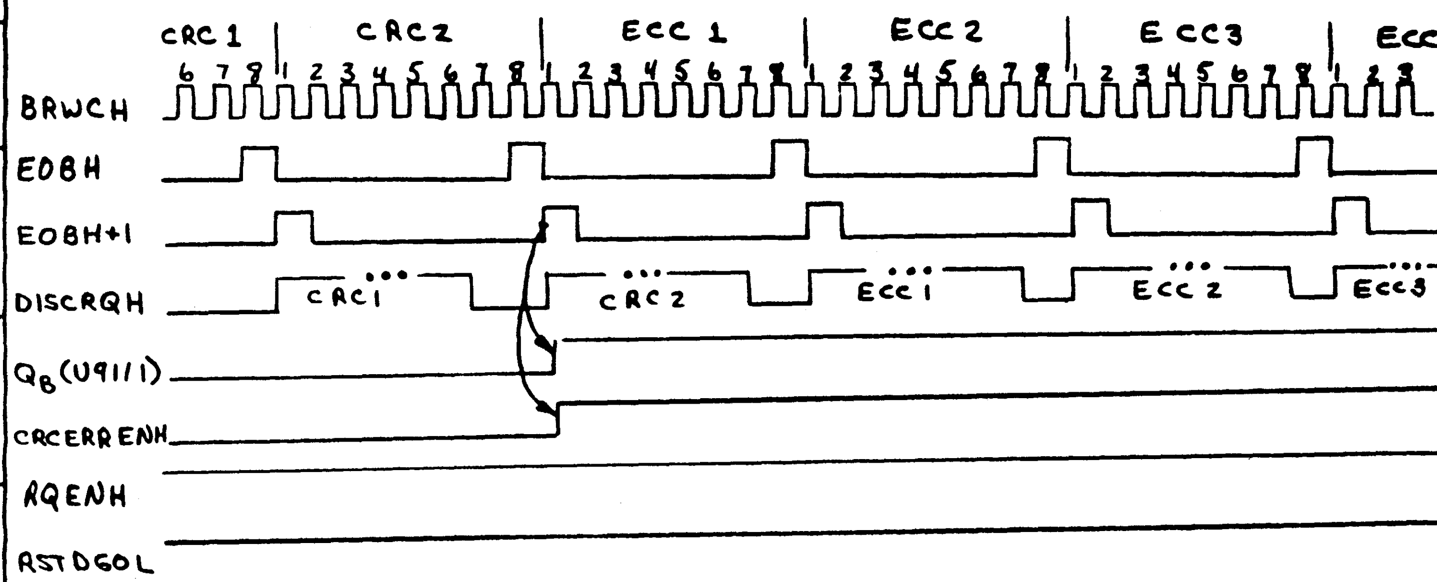


Fig. 11. End of Sector Timing for a Disc Read

HEWLETT-PACKARD CO.

DATE 12-1-81
SHEET NO 65 OF 73
DWG NO A-5955-3497-1

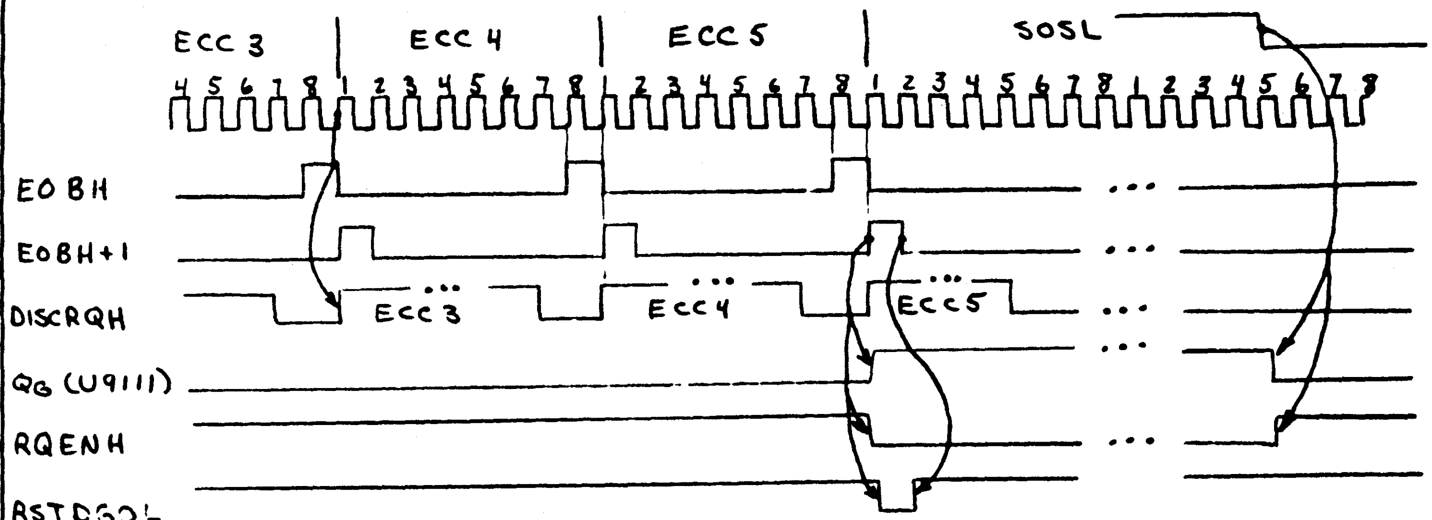


Fig. 12 End of Sector Timing for a Disc Read.

HEWLETT-PACKARD CO.

DATE 12-1-81

SHEET NO 66 OF 73

DWG NO A-5955-3497-1

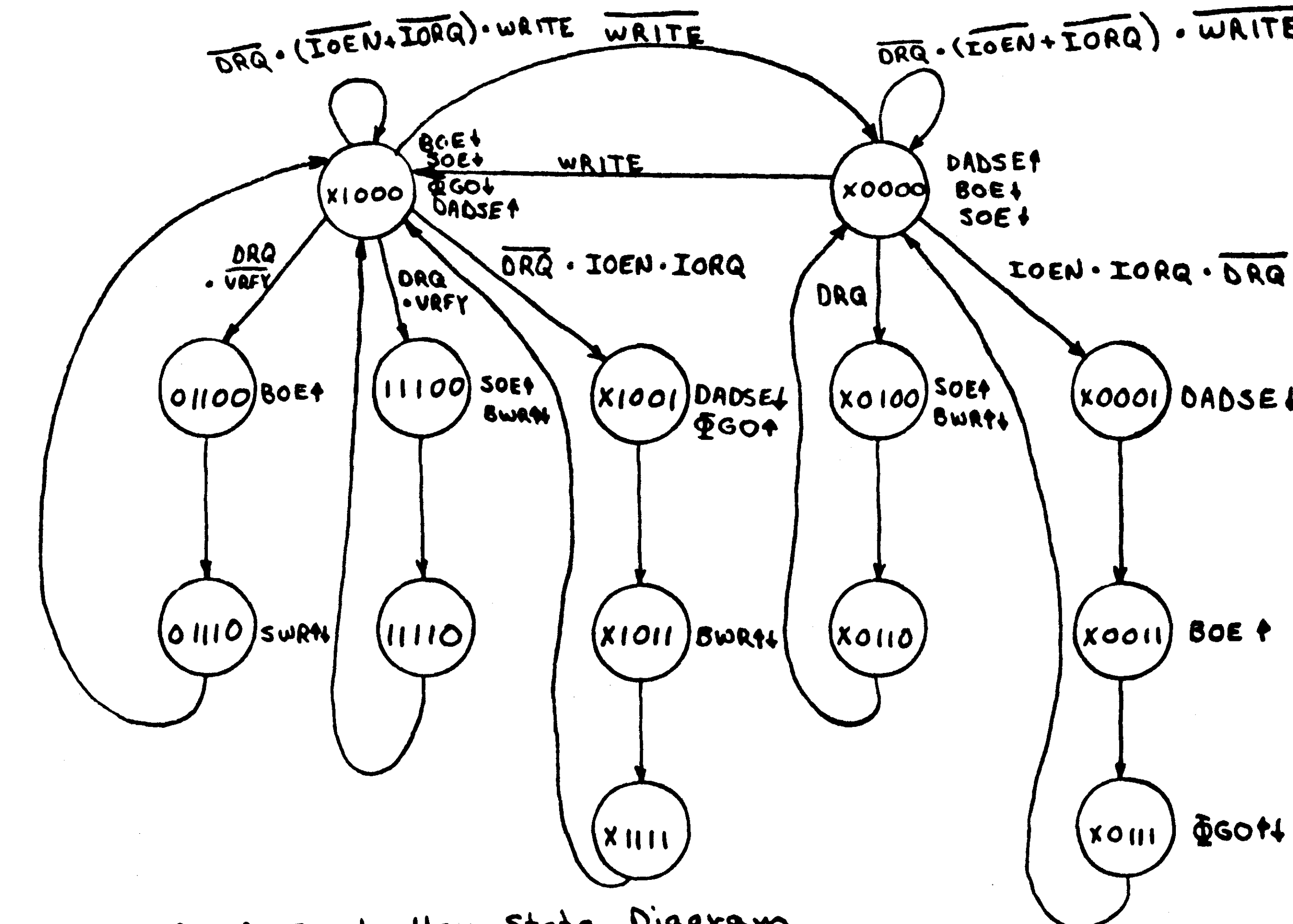


Fig. 13. DMA Controller State Diagram

HEWLETT-PACKARD CO.

DATE	12-1-81
SHEET NO	67 OF 73
DWG NO	A-5955-3497-1

9320-2788 (FORMERLY 0-7002?)

HEWLETT-PACKARD CO.

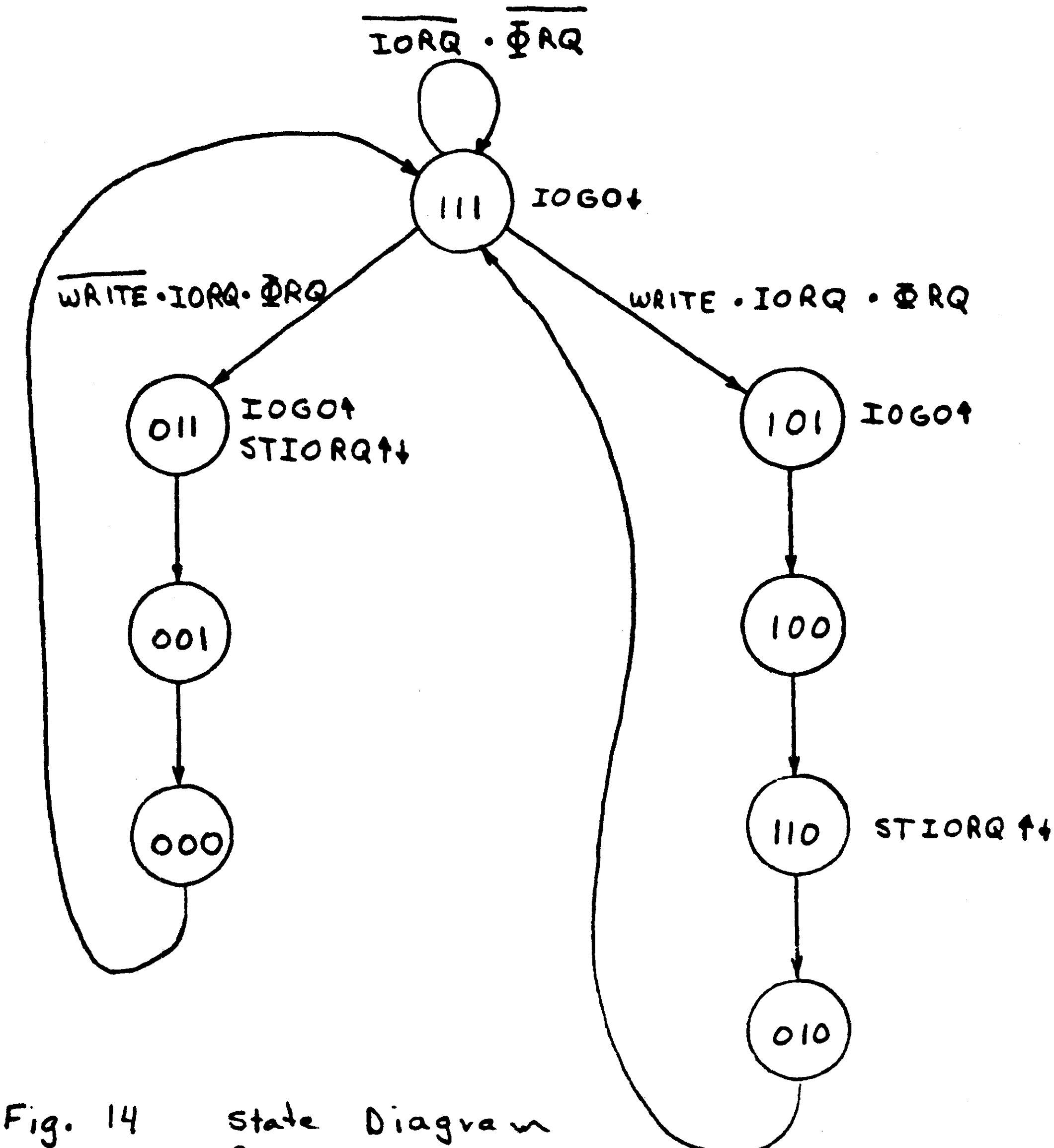


Fig. 14 State Diagram for the PHI Controller.

MODEL		STK NO.	
BY		DATE	12-1-81
APPD		SHEET NO	68 OF 73
SUPERSEDES		DWG NO	A-5955-3497-1

LTR	PC NO	APPROVED	DATE
	REVISIONS		

9320-2789 (FORMERLY D-70002A)

HEWLETT-PACKARD CO.

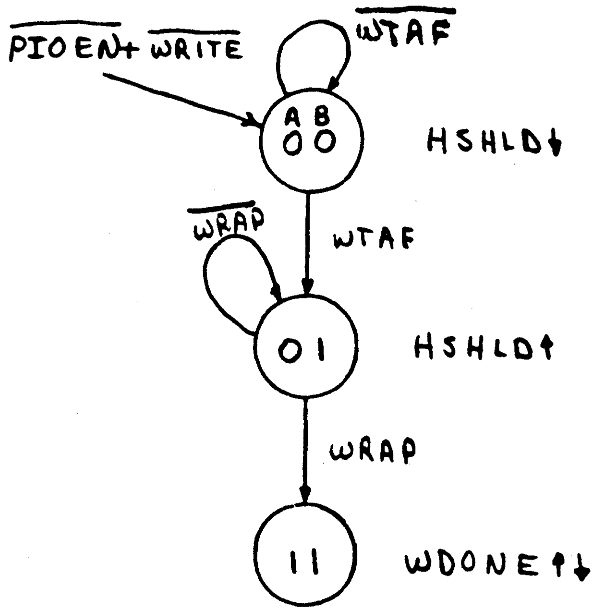


Figure 15. Security circuit state diagram

				MODEL	STK NO	
				BY	DATE	12-1-81
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO	69 OF 73
	REVISIONS			SUPERSEDES	DWG NO	A-5955-3497-1

9320-2789 (FORMERLY 0-700024)

HEWLETT-PACKARD CO.

BYTE CONTROLLER PROM FOR THE DMA BOARD
CHECK SUM = 3128
(7649-5)
U4101

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	8F	BE	8F	7E	E7	8F	8F	8F	8F	BE	8F	7E	E7	8F	8F	8F
010	C5	BE	8F	7E	E7	8F	8F	8F	C5	BE	8F	7E	E7	8F	8F	8F
020	8F	BE	8F	7E	E7	8F	8F	8F	8F	BE	8F	7E	E7	8F	8F	8F
030	C5	BE	8F	7E	E7	8F	8F	8F	C5	BE	8F	7E	E7	8F	8F	8F
040	8F	3D	8F	7F	EA	8F	8F	8F	8F	3D	8F	7F	EA	8F	8F	8F
050	CE	3D	8F	7F	EA	8F	8F	8F	CE	3D	8F	7F	EA	8F	8F	8F
060	8F	3D	8F	7F	E7	8F	8F	8F	8F	3D	8F	7F	E7	8F	8F	8F
070	C5	3D	8F	7F	E7	8F	8F	8F	C5	3D	8F	7F	E7	8F	8F	8F
080	9F	BE	8F	7E	E7	8F	8F	8F	8F	BE	8F	7E	E7	8F	8F	8F
090	C5	BE	8F	7E	E7	8F	8F	8F	C5	BE	8F	7E	E7	8F	8F	8F
0A0	9F	BE	8F	7E	E7	8F	8F	8F	8F	BE	8F	7E	E7	8F	8F	8F
0B0	C5	BE	8F	7E	E7	8F	8F	8F	C5	BE	8F	7E	E7	8F	8F	8F
0C0	1F	3D	8F	7F	EA	8F	8F	8F	8F	3D	8F	7F	EA	8F	8F	8F
0D0	CE	3D	8F	7F	EA	8F	8F	8F	CE	3D	8F	7F	EA	8F	8F	8F
0E0	1F	3D	8F	7F	E7	8F	8F	8F	8F	3D	8F	7F	E7	8F	8F	8F
0F0	C5	3D	8F	7F	E7	8F	8F	8F	C5	3D	8F	7F	E7	8F	8F	8F
100	8F	BE	8F	7E	E7	8F	8F	8F	8F	BE	8F	7E	E7	8F	8F	8F
110	C5	BE	8F	7E	E7	8F	8F	8F	C5	BE	8F	7E	E7	8F	8F	8F
120	8F	BE	8F	7E	E7	8F	8F	8F	8F	BE	8F	7E	E7	8F	8F	8F
130	C5	BE	8F	7E	E7	8F	8F	8F	C5	BE	8F	7E	E7	8F	8F	8F
140	8F	3D	8F	7F	EA	8F	8F	8F	8F	3D	8F	7F	EA	8F	8F	8F
150	CE	3D	8F	7F	EA	8F	8F	8F	CE	3D	8F	7F	EA	8F	8F	8F
160	8F	3D	8F	7F	E7	8F	8F	8F	8F	3D	8F	7F	E7	8F	8F	8F
170	C5	3D	8F	7F	E7	8F	8F	8F	C5	3D	8F	7F	E7	8F	8F	8F
180	9F	BE	8F	7E	E7	8F	8F	8F	8F	BE	8F	7E	E7	8F	8F	8F
190	C5	BE	8F	7E	E7	8F	8F	8F	C5	BE	8F	7E	E7	8F	8F	8F
1A0	9F	BE	8F	7E	E7	8F	8F	8F	8F	BE	8F	7E	E7	8F	8F	8F
1B0	C5	BE	8F	7E	E7	8F	8F	8F	C5	BE	8F	7E	E7	8F	8F	8F
1C0	1F	3D	8F	7F	EA	8F	8F	8F	8F	3D	8F	7F	EA	8F	8F	8F
1D0	CE	3D	8F	7F	EA	8F	8F	8F	CE	3D	8F	7F	EA	8F	8F	8F
1E0	1F	3D	8F	7F	E7	8F	8F	8F	8F	3D	8F	7F	E7	8F	8F	8F
1F0	C5	3D	8F	7F	E7	8F	8F	8F	C5	3D	8F	7F	E7	8F	8F	8F

Figure 16. DMA Controller PROM Pattern.

LTR	P C NO	APPROVED	DATE	MODEL	STK NO
				BY	DATE 12-1-81
				APPD	SHEET NO 70 OF 73
	REVISIONS			SUPERSEDES	DWG NO A-5955-3497-1

9320-2789 (FORMERLY 0-70002#)

HEWLETT-PACKARD CO.

PHI CONTROLLER PROM FOR THE DMA BOARD
(7603)
(U2121)

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	17	00	17	01	0E	04	02	17	17	00	17	01	0E	04	02	17
10	17	00	17	01	0E	04	02	0B	17	00	17	C1	0E	04	02	05

Figure 17. PHI Controller PROM Pattern.

				MODEL		STK NO
				BY	DATE 12-1-81	
				APPD	SHEET NO 71 OF 73	
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-5955-3497-1	
	REVISIONS					

8320-2789 (FORMERLY 0-700024)

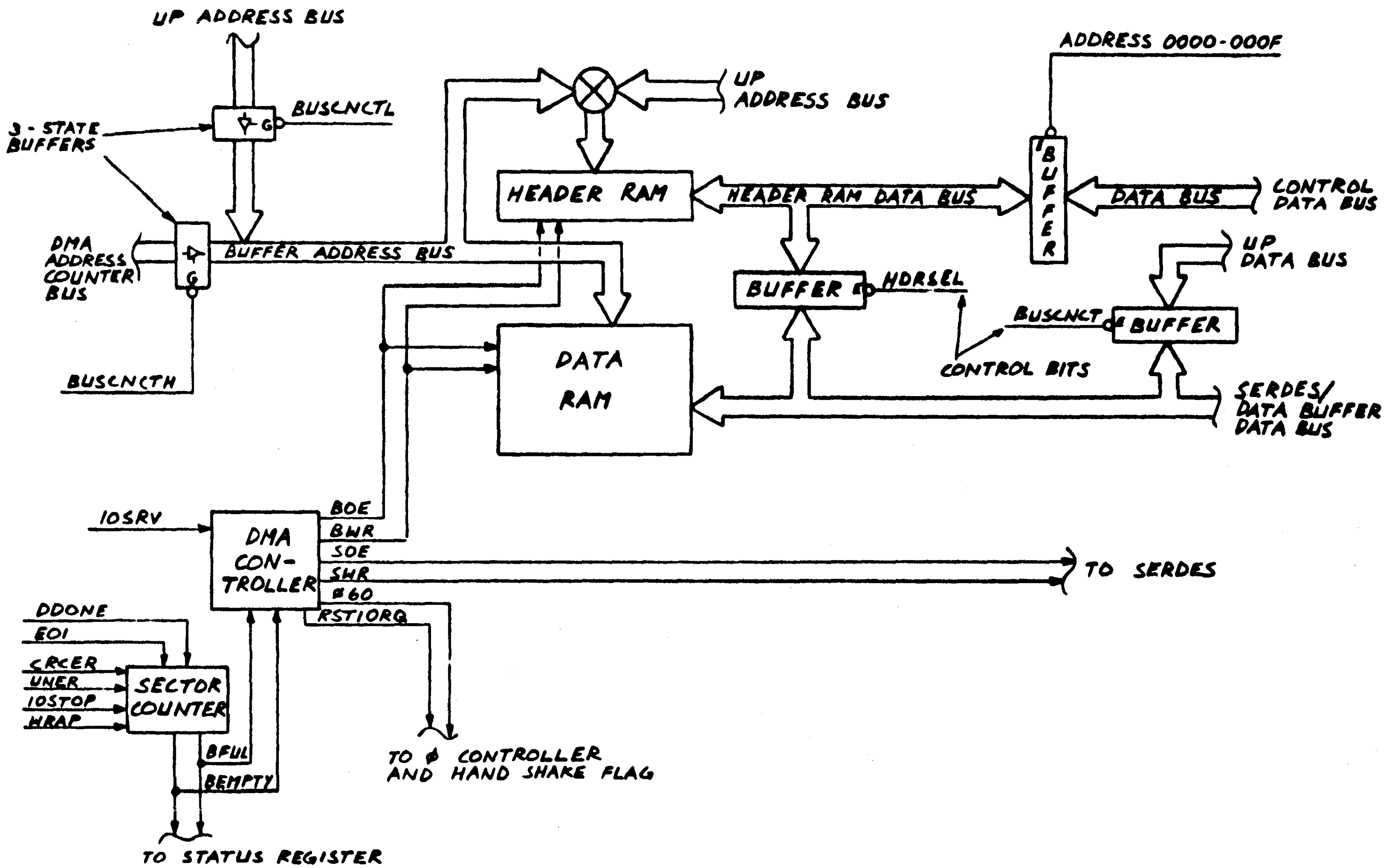

UP ADDRESS BUS
BUSCNCTL
3-STATE BUFFERS
DMA ADDRESS COUNTER BUS
BUFFER ADDRESS BUS
BUSCNCTH
UP ADDRESS BUS
HEADER RAM
HEADER RAM DATA BUS
ADDRESS 0000-000F
BUFFER
DATA BUS
CONTROL DATA BUS
UP DATA BUS
BUFFER
HDRSEL
BUSCNCT
BUFFER
CONTROL BITS
DATA RAM
SERDES/ DATA BUFFER DATA BUS
IOSRV
DMA CON-TROLLER
BOE
BWR
SOE
SWR
#60
RSTIORQ
TO SERDES
DDONE
EOI
CRCER
UNER
IOSTOP
WRAP
SECTOR COUNTER
BFUL
BEMPTY
TO STATUS REGISTER
TO ϕ CONTROLLER AND HAND SHAKE FLAG

FIGURE 18.

REV. NO. A

DATE 12-1-81

DWG. NO. A-5955-3497-1

SHEET 73 OF 73

HEWLETT PACKARD

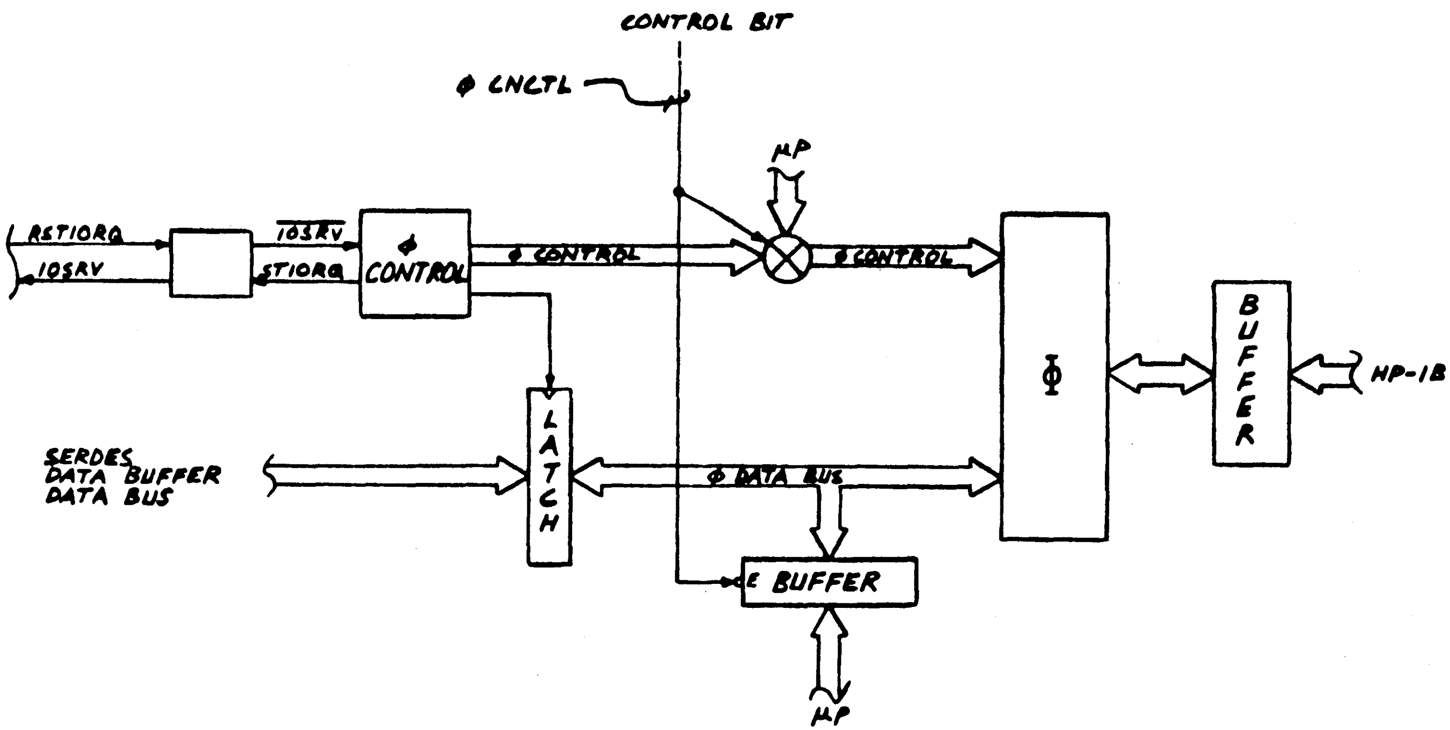


FIGURE 19.

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60009
07908-68009

DATE CODE : D-2302

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C110	0160-5298	CAP .01UF 20%
C210	0160-5298	CAP .01UF 20%
C215	0160-5298	CAP .01UF 20%
C220	0160-5298	CAP .01UF 20%
C225	0160-5298	CAP .01UF 20%
C230	0160-5298	CAP .01UF 20%
C235	0160-5298	CAP .01UF 20%
C240	0160-5298	CAP .01UF 20%
C245	0160-5298	CAP .01UF 20%
C250	0160-5298	CAP .01UF 20%
C255	0160-5332	CAP.1UF 20% 50V
C260	0160-5298	CAP .01UF 20%
C270	0160-5298	CAP .01UF 20%
C290	0160-5298	CAP .01UF 20%
C405	0160-5298	CAP .01UF 20%
C415	0160-5298	CAP .01UF 20%
C420	0160-5298	CAP .01UF 20%
C425	0160-5298	CAP .01UF 20%
C430	0160-5298	CAP .01UF 20%
C435	0160-5298	CAP .01UF 20%
C440	0160-5298	CAP .01UF 20%
C445	0160-5298	CAP .01UF 20%
C475	0160-5298	CAP .01UF 20%
C485	0160-5298	CAP .01UF 20%
C495	0160-5298	CAP .01UF 20%
C510	0160-5298	CAP .01UF 20%
C515	0160-5298	CAP .01UF 20%
C520	0160-5298	CAP .01UF 20%
C525	0160-5298	CAP .01UF 20%
C540	0160-5298	CAP .01UF 20%
C550	0160-5298	CAP .01UF 20%
C560	0160-5298	CAP .01UF 20%
C565	0160-5298	CAP .01UF 20%
C570	0160-5298	CAP .01UF 20%
C580	0160-5298	CAP .01UF 20%
C590	0160-5298	CAP .01UF 20%
C795	0160-5298	CAP .01UF 20%
C805	0160-5298	CAP .01UF 20%
C815	0160-5298	CAP .01UF 20%
C820	0160-5298	CAP .01UF 20%
C825	0160-5298	CAP .01UF 20%
C830	0160-5298	CAP .01UF 20%
C835	0160-5298	CAP .01UF 20%
C840	0160-5298	CAP .01UF 20%
C845	0160-5298	CAP .01UF 20%
C849	0160-5298	CAP .01UF 20%
C850	0160-5298	CAP .01UF 20%

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60009
07908-68009

DATE CODE : D-2302

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C855	0160-5298	CAP .01UF 20%
C860	0160-5298	CAP .01UF 20%
C865	0160-5298	CAP .01UF 20%
C870	0160-5298	CAP .01UF 20%
C875	0160-5298	CAP .01UF 20%
C880	0160-5298	CAP .01UF 20%
C925	0160-5298	CAP .01UF 20%
C930	0160-5298	CAP .01UF 20%
C935	0160-5298	CAP .01UF 20%
C940	0180-1746	CAP 15UF 10%
C960	0160-5298	CAP .01UF 20%
C970	0160-5298	CAP .01UF 20%
C980	0160-5298	CAP .01UF 20%
C985	0180-2208	CAP 220UF 10%
L955	9100-1788	CHOKE-WIDE BAND
MP1	07908-80009	ETCHED BD-DMA
MP10	07908-00011	GROUNDING BKT.
MP2	7120-6830	LABEL-INFO
MP3	0403-0454	EXTR-PC BD #4
MP4	1480-0116	PIN GRV .062X.25
MP5	2190-0586	WSHR-LK HLCL
MP6	1530-1098	CLEVIS
MP7	0361-0079	RIVET .123DX.312
MP8	1251-3283	CONN 24-PIN F
MP9	0380-0643	STANDOFF-METRIC
R265	0698-3136	RES 17.8K 1%.125
S150	3101-2264	SWITCH-ROCKER
U1101	1820-2058	IC MC3448AL
U1111	1820-2058	IC MC3448AL
U1121	1813-0224	CLOCK OSC 12MHZ
U131	1820-1281	IC SN74LS139N
U141	1810-0256	NETWORK-RES DIP
U151	1820-1885	IC DM74LS173N
U161	1820-1885	IC DM74LS173N
U171	1820-1416	IC SN74LS14N
U181	1820-2058	IC MC3448AL
U191	1820-2058	IC MC3448AL
U211	1820-1438	IC SN74LS257AN
U2111	1AA6-6104	PHI
U2121	1816-1527	IC MEMORY
U2131	1820-1191	IC SN74S175N
U221	1820-1430	IC-SN74LS161N
U231	1820-1278	IC SN74LS191N
U241	1820-1568	IC SN74LS125N
U251	1820-2075	IC SN74LS245N
U261	1820-2641	IC SN74LS374N
U3101	1820-1195	IC SN74LS175N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60009
07908-68009

DATE CODE : D-2302

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U311	1820-1438	IC SN74LS257AN
U3111	1820-1195	IC SN74LS175N
U3121	1820-1322	IC SN74S02N
U3131	1820-0681	IC SN74S00N
U321	1820-1195	IC SN74LS175N
U331	1820-1438	IC SN74LS257AN
U341	1820-1438	IC SN74LS257AN
U351	1820-1438	IC SN74LS257AN
U361	1820-1275	IC SN74S260N
U371	1820-1278	IC SN74LS191N
U381	1820-1208	IC SN74LS32N
U391	1820-1438	IC SN74LS257AN
U4101	1816-1526	IC MEMORY
U411	1820-1438	IC SN74LS257AN
U4111	1820-1191	IC SN74S175N
U4121	1820-1191	IC SN74S175N
U4131	1820-1158	IC SN74S51N
U421	1820-1430	IC-SN74LS161N
U431	1820-1438	IC SN74LS257AN
U441	1820-1438	IC SN74LS257AN
U451	1820-1885	IC DM74LS173N
U461	1820-1195	IC SN74LS175N
U471	1820-1428	SN74LS158N
U481	1820-0629	IC SN74S112N
U491	1820-1633	IC SN74S240N
U5101	1820-1076	IC SN74S174N
U511	1820-1278	IC SN74LS191N
U5111	1820-1367	IC SN74S08N
U5121	1820-1319	IC SN74S151N
U5131	1820-0688	IC SN74S20N
U521	1820-1278	IC SN74LS191N
U531	1820-1278	IC SN74LS191N
U541	1820-1278	IC SN74LS191N
U551	1820-2024	IC SN74LS244N
U561	1820-1730	IC SN74LS273N
U571	1820-0693	IC SN74S74N
U581	1820-0693	IC SN74S74N
U591	1820-0629	IC SN74S112N
U6101	1820-1322	IC SN74S02N
U611	1820-1278	IC SN74LS191N
U6111	1820-1212	IC SN74LS112N
U6121	1820-0686	IC SN74S11N
U6131	1820-1322	IC SN74S02N
U621	1820-1278	IC SN74LS191N
U631	1820-1121	IC 8093N
U641	1820-1216	IC SN74LS138N
U651	1820-1216	IC SN74LS138N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60009
07908-68009

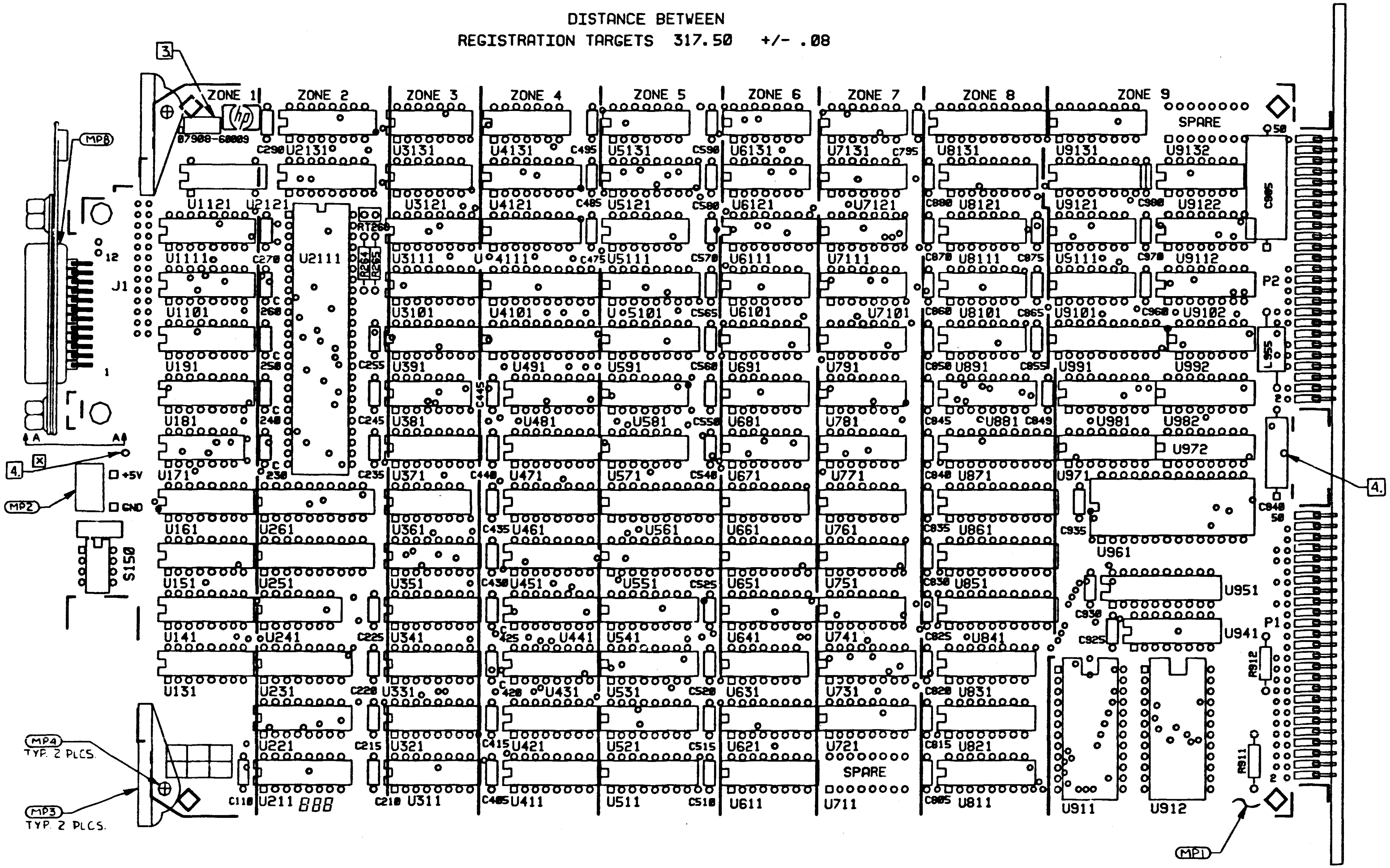
DATE CODE : D-2302

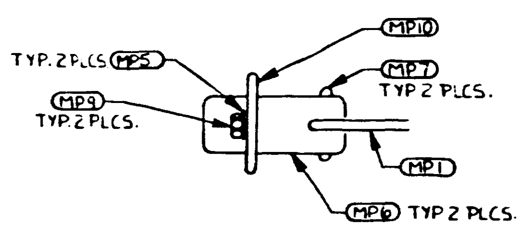
REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U661	1820-1112	IC SN74LS74N
U671	1820-1367	IC SN74S08N
U681	1820-0681	IC SN74S00N
U691	1820-1112	IC SN74LS74N
U7101	1820-0693	IC SN74S74N
U7111	1820-1197	IC SN74LS00N
U7121	1820-0693	IC SN74S74N
U7131	1820-0694	IC SN74S86N
U721	1820-1438	IC SN74LS257AN
U731	1820-1438	IC SN74LS257AN
U741	1820-1208	IC SN74LS32N
U751	1820-1367	IC SN74S08N
U761	1820-1208	IC SN74LS32N
U771	1820-1203	IC SN74LS11N
U781	1820-1202	IC SN74LS10N
U791	1820-0683	IC SN74S04N
U8101	1820-1367	IC SN74S08N
U811	1820-1438	IC SN74LS257AN
U8111	1820-0683	IC SN74S04N
U8121	1820-1430	IC-SN74LS161N
U8131	1820-1730	IC SN74LS273N
U821	1816-0724	IC-MEMORY
U831	1816-0724	IC-MEMORY
U841	1820-1917	IC SN74LS240N
U851	1820-1917	IC SN74LS240N
U861	1820-2075	IC SN74LS245N
U871	1820-1677	IC SN74S374N
U881	1810-0256	NETWORK-RES DIP
U891	1820-0685	IC SN74S10N
U9101	1820-1158	IC SN74S51N
U9102	1820-0629	IC SN74S112N
U911	1818-1718	RAM 2K X 8
U9111	1820-1433	IC SN74LS164
U9112	1820-0629	IC SN74S112N
U912	1818-1718	RAM 2K X 8
U9121	1820-1077	IC SN74S157N
U9122	1820-1433	IC SN74LS164
U9131	1820-1922	IC SN74LS166N
U941	1820-1641	IC SN74LS365N
U951	1820-2024	IC SN74LS244N
U971	1820-1885	IC DM74LS173N
U972	1820-1885	IC DM74LS173N
U981	1820-1300	IC SN74LS195AN
U982	1820-1300	IC SN74LS195AN
U991	1820-1633	IC SN74S240N
U992	1820-0693	IC SN74S74N

END OF MATERIAL LIST.

D		D-07908-60009-1
J	REVISED AND REDRAWN PER C0480112	
K	[illegible] D-2302 [illegible]	12-27-83

DISTANCE BETWEEN
REGISTRATION TARGETS 317.50 +/- .08





DETAIL A-A

NOTES:

UNLESS OTHERWISE SPECIFIED

1. THIS BOARD CONFORMS TO CORPORATE AUTOMATIC INSERTION STANDARDS AS PER AXIAL LEAD MANUAL DATED 4-14-80.
2. ARTWORK DATE 7-1-83.
3. MARK ASSEMBLY DATE CODE D-2302.
4. BOARD ERROR CORRECTION HOLES.

9-1-82	BOARD ASSEMBLY, DMA, 07908	HEWLETT PACKARD
9-2-83		
9-2-83	SEE WHERE USED	07908-60009
	SCALE 2:1	D-07908-60009-1

REVISIONS

The first assembly which may be revised is A-2138. All prior assemblies are to be scrapped.

A-2138 (PCO 48-4538) Changed extractors on PCA so they have identification number indicating where the PCA is to be placed in the card cage.

A	ISSUED	sb/ML	12-02-81	MODEL 7908	STK # 07908-69009	
B	48-6179	jr/JSK	02-01-83	UPDATE AND REVISION PROCEDURE		
		/	- -	BY	DATE APR 12, 1984	
LT	P.C. #	APPR	DATE	APPD	SHEET # 3 OF 4	
REVISIONS				SUPERSEDES	DWG # A-07908-69009-1	

PROCEDURE:

1.0 Inspect all boards for general mechanical and cosmetic defects. Repair all visible defects.

2.0 Identify all boards with the following logo:

07908-69009

2138

3.0 Affix, near the logo, a 7120-5480 label which indicates the month and year of final inspection.

A	ISSUED	sb/ML	12-02-81	MODEL 7908	STK # 07908-69009
B	48-6179	jr/JSK	02-01-83	UPDATE AND REVISION PROCEDURE	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 4 OF 4
REVISIONS				SUPERSEDES	DWG # A-07908-69009-1

ER48 D/H: C2, 50A

/ hp /

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NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline). (L208)

LTR	REVISIONS	DATE	INIT	M F
A	AS ISSUED	12-02-81	sb/ML	M
B	UPDATED PER PC 48-6179	02-01-83	jr/JSK	M

A	ISSUED	sb/ML	12-02-81	MODEL 7908	STK # 07908-69009
B	48-6179	jr/JSK	02-01-83	UPDATE AND REVISION PROCEDURE	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 4
REVISIONS				SUPERSEDES	DWG # A-07908-69009-1

ER48 D/H: C2, 50A

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UPDATING AND REVISION PROCEDURE

07908-69009

This procedure contains instructions for modification of the Disc Memory Access (DMA) PCA, 07908-60009 to version 07908-69009.

RELATED DOCUMENTS AND PROCEDURES

07908-68009	Material List
F-07908-60009-1	Assembly Drawing
F-07908-60009-20	Modification Drawing
F-07908-60009-21	Modification Drawing
D-07908-60009-50	Schematics
A-07908-90047-1	I/O Line Processing Procedure

A	ISSUED	sb/ML	12-02-81	MODEL 7908	STK # 07908-69009
B	48-6179	jr/JSK	02-01-83	UPDATE AND REVISION PROCEDURE	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 2 OF 4
REVISIONS				SUPERSEDES	DWG A-07908-69009-1

F-07908-60009-20

REV	REVISIONS	APPROVED	DATE
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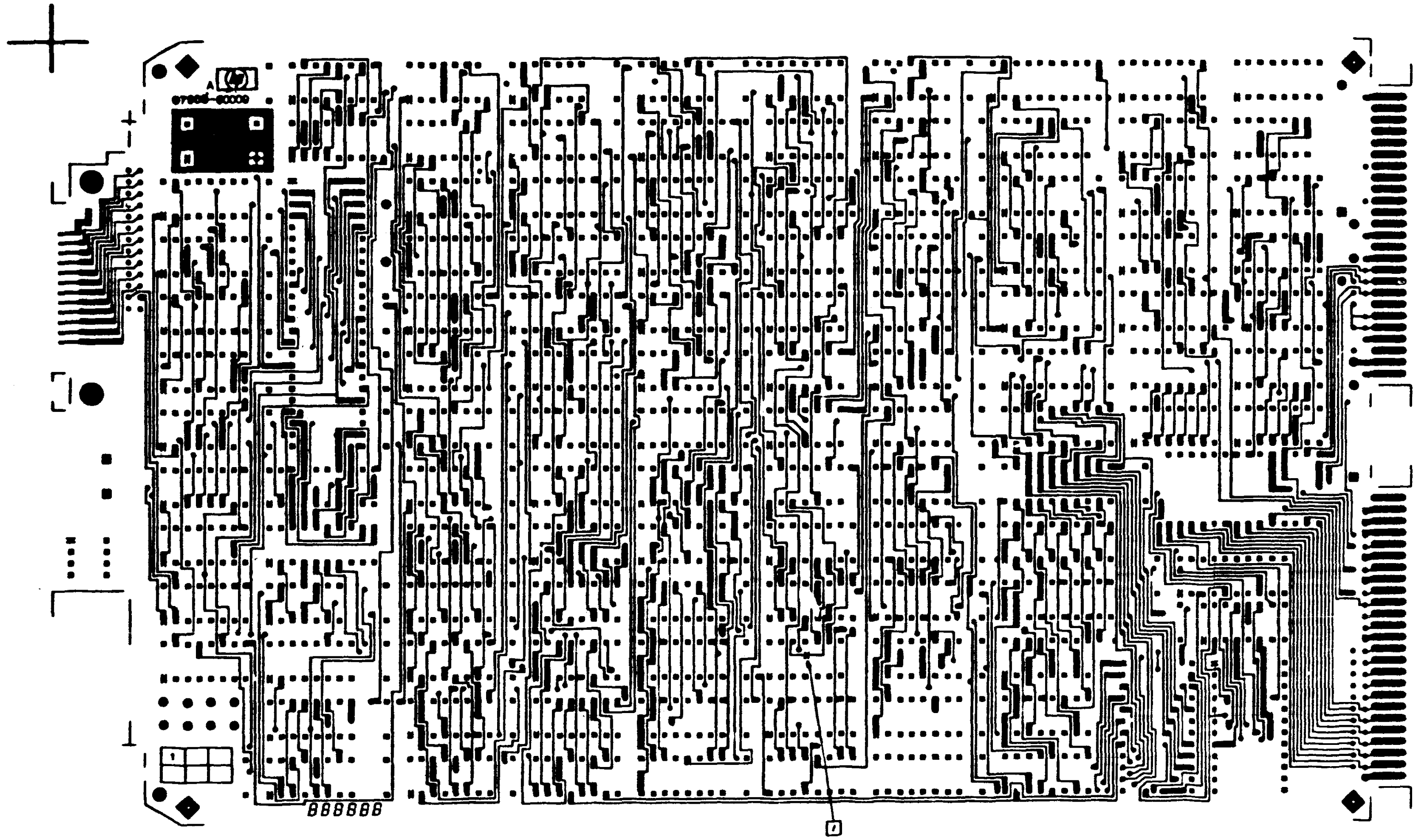


F-07908-80009-4
F-07908-80009-4

PAD MASTER
COMPONENT SIDE 1 OF 6

6-5-81
6-5-81

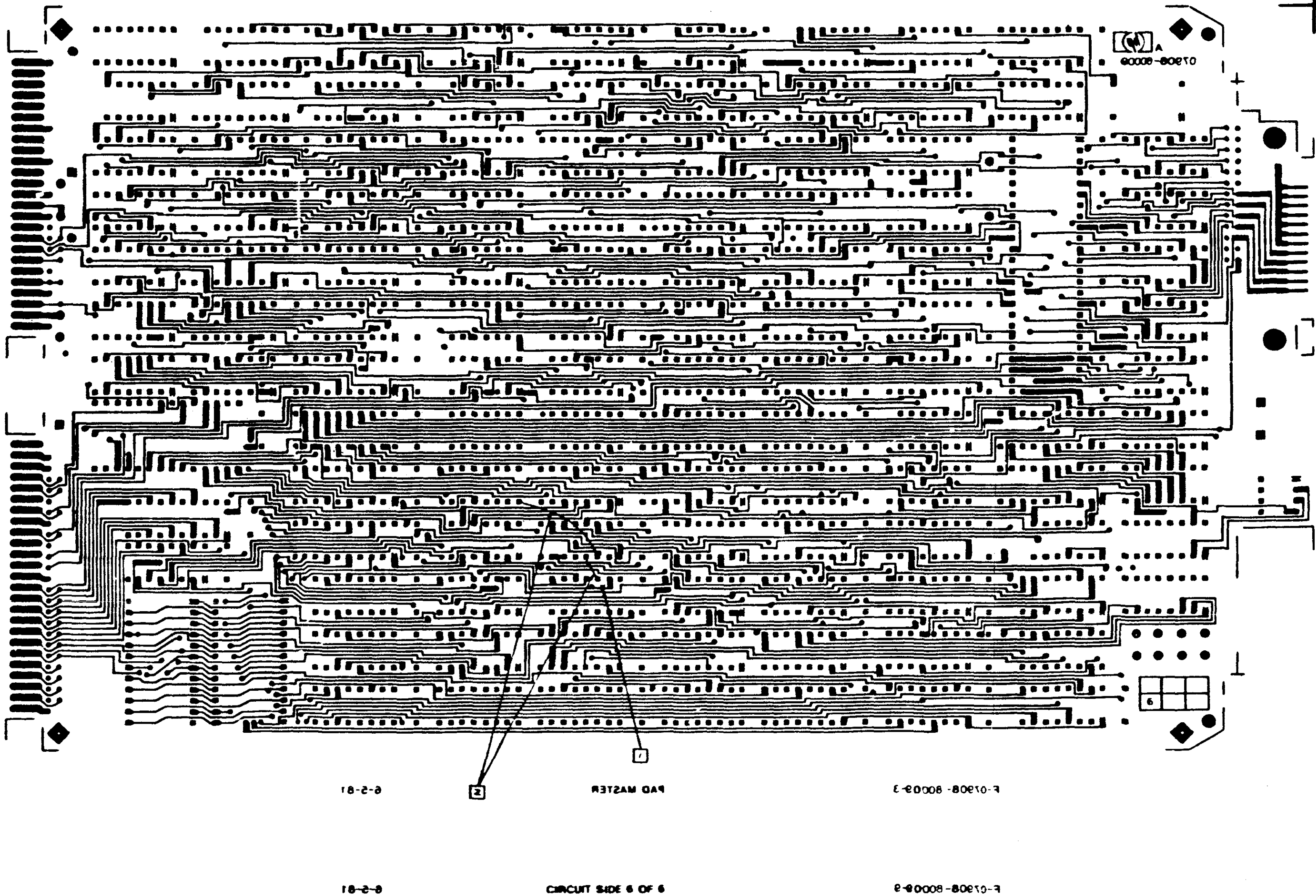
NOTE:
1 CUT TRACE

10-28-81 4/3/84 4/3/84	MODIFICATION	HEWLETT PACKARD
		07908-60009
		F-07908-60009-20

5

F-07908-60009-21

A	AS ISSUED PER PPLO 48-4315	MTS RL	10-29-81



NOTES:
1. CUT TRACE
2. ADD JUMPERS

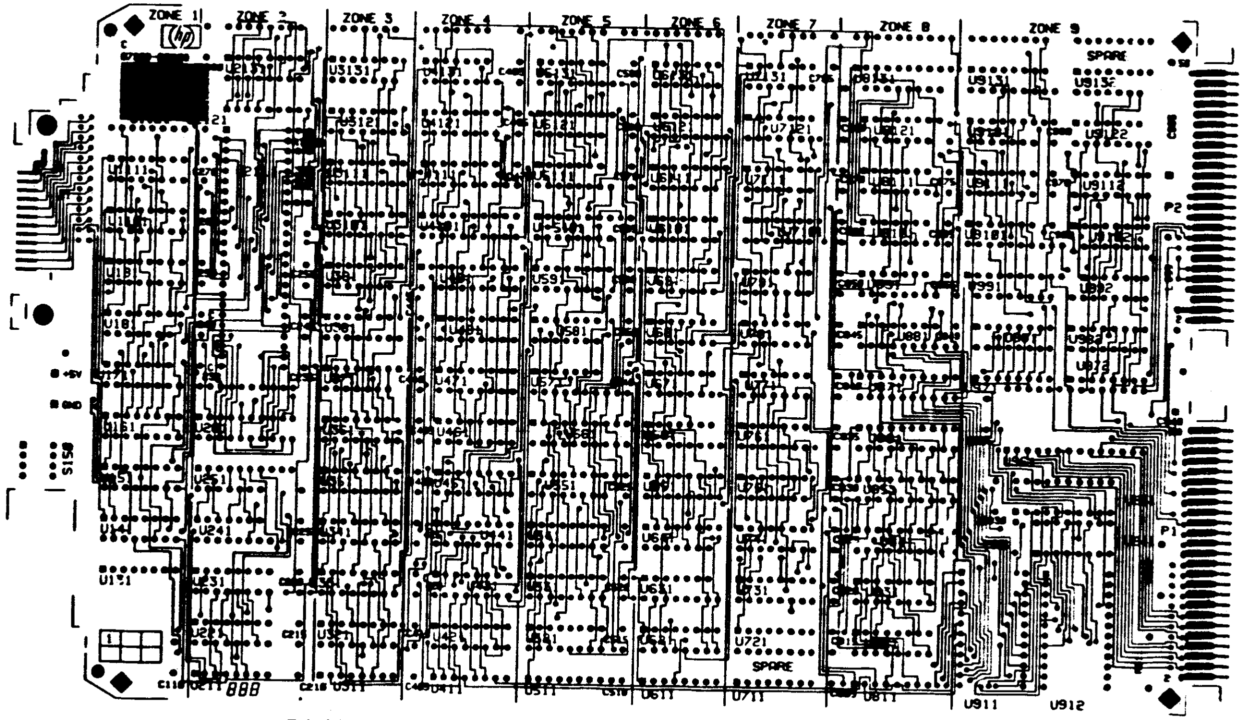
10-29-81	MODIFICATION	HEWLETT PACKARD
4/5/84		
4/5/84		07908-60009
		F-07908-60009-21

1 of 1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PER CO 48012	JAX	9-2-83

C-07908-60009-22

DISTANCE BETWEEN
REGISTRATION TARGETS 317.50 +/- .00



COMPONENT SIDE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

DO NOT SCALE THIS DRAWING

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

DATE 8-5-83
9-2-83
9-2-83

TITLE: DMA MODIFICATION DRAWING

HEWLETT PACKARD

PART NUMBER: 07908-60009

C-07908-60009-22

SCALE 1:1

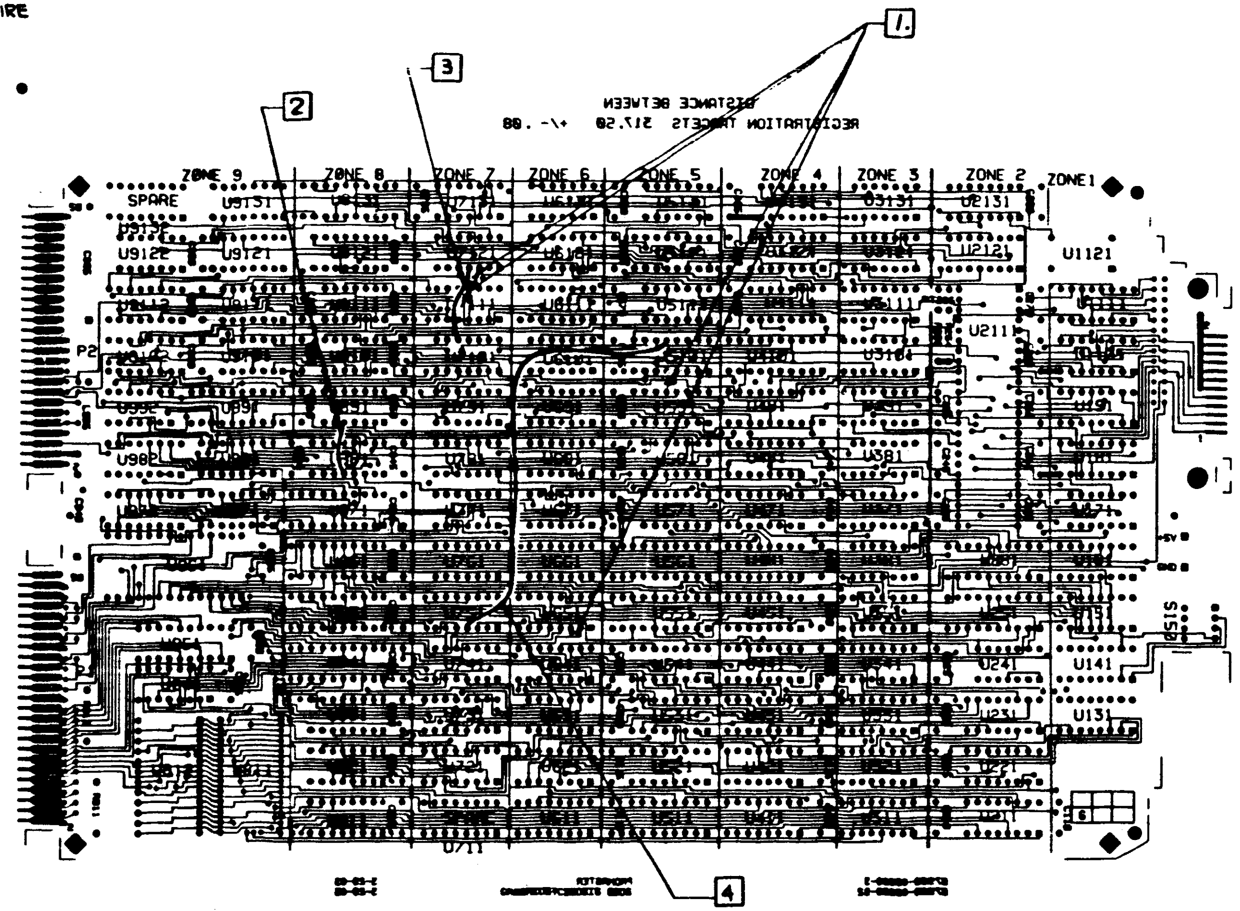
SHEET 1 OF 2

C-07908-60009-22

SYM	REVISIONS	APPROVED	DATE
	SEE SHT. ONE		

MODIFICATION INSTRUCTIONS:

1. PERFORM 4 TRACE CUTS ON LAYER 5 FROM THE CIRCUIT SIDE OF THE BOARD AS INDICATED.
2. ATTACH 30 AWG WHITE INSULATED WIRE FROM U881-5 TO U891-5.
3. ATTACH 30 AWG WHITE INSULATED WIRE FROM U7101-10 TO U7121-4.
4. ATTACH 30 AWG WHITE INSULATED WIRE FROM U751-4 TO U5101-12.



CIRCUIT SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES XX ± 0.5 mm or ± 0.4 mm
XX X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX
SEE CORP STD 608

DO NOT SCALE THIS DRAWING

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

8-3-83 DATE

TITLE: DMA MODIFICATION DRAWING

HEWLETT PACKARD

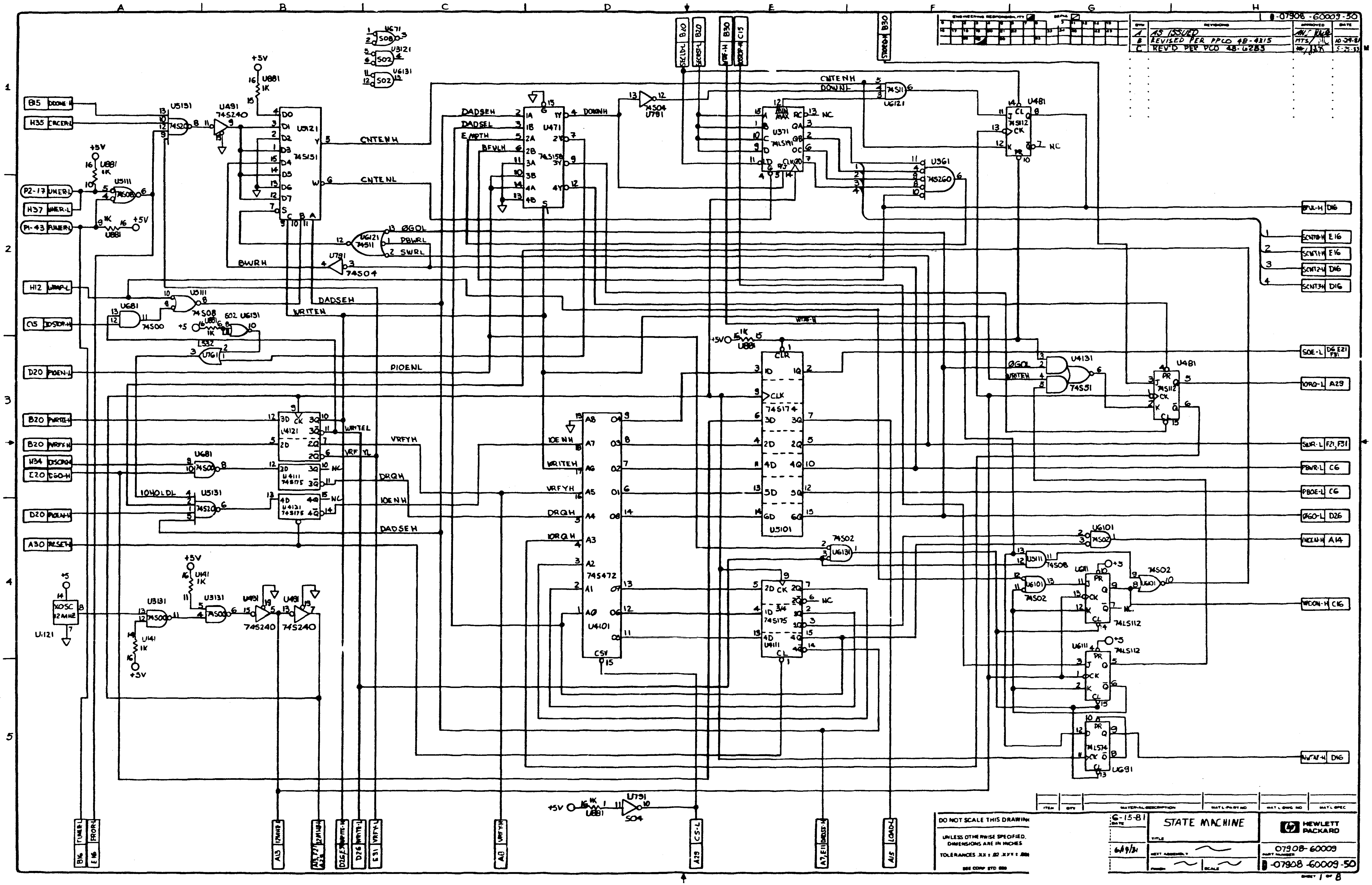
NEXT ASSEMBLY ~

PART NUMBER 07908-60009

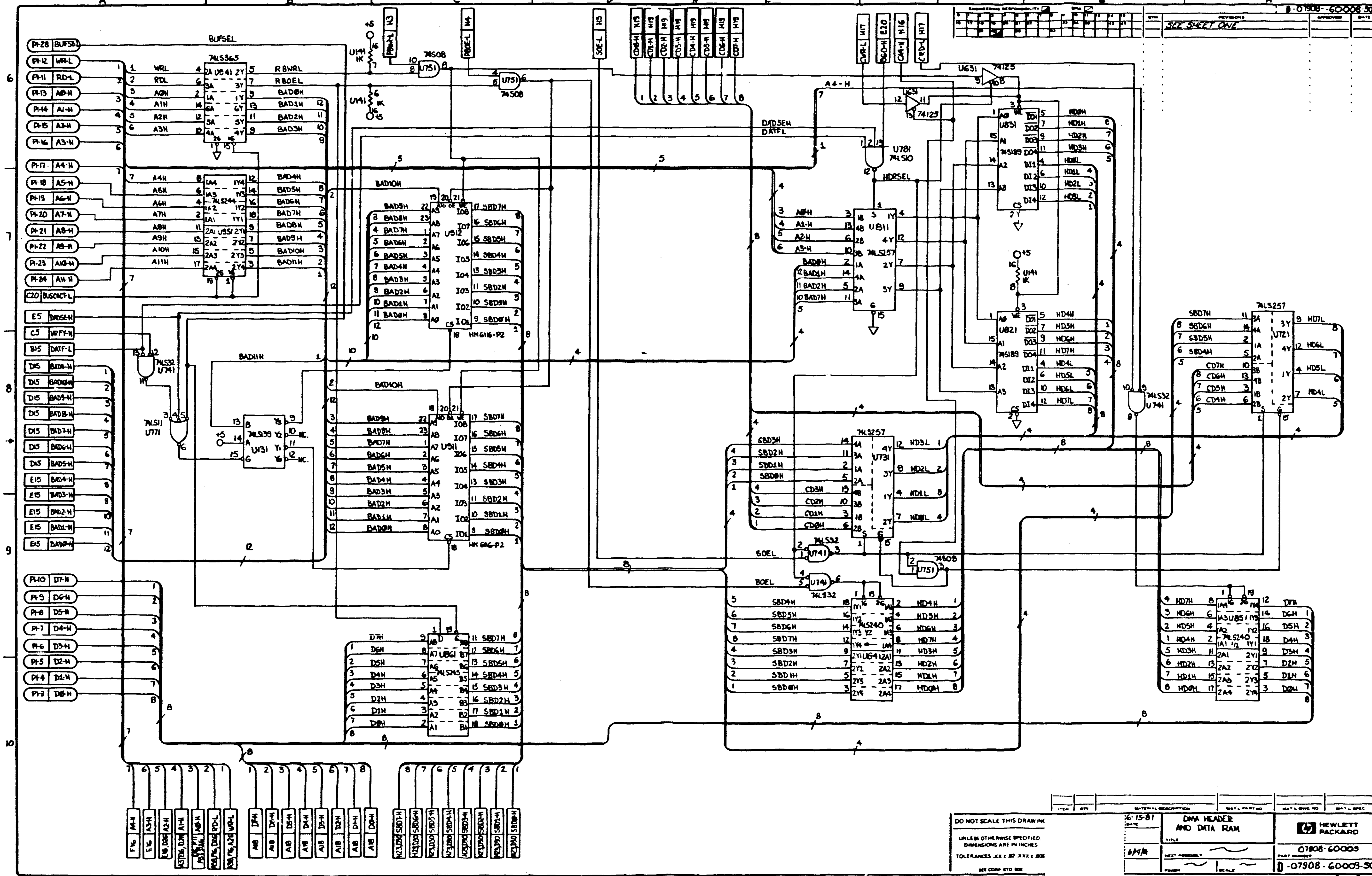
FINISH ~ SCALE 1:1

C-07908-60009-22

SHEET 2 OF 2



B-07908-60009-50
A AS ISSUED
B REVISED PER PPCO 48-4315
C REV'D PER PCO 48-6283
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
6-15-81
STATE MACHINE
HEWLETT PACKARD
07908-60009
B-07908-60009-50
SHEET 1 OF 8


D-07908-60009-50
SEE SHEET ONE
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
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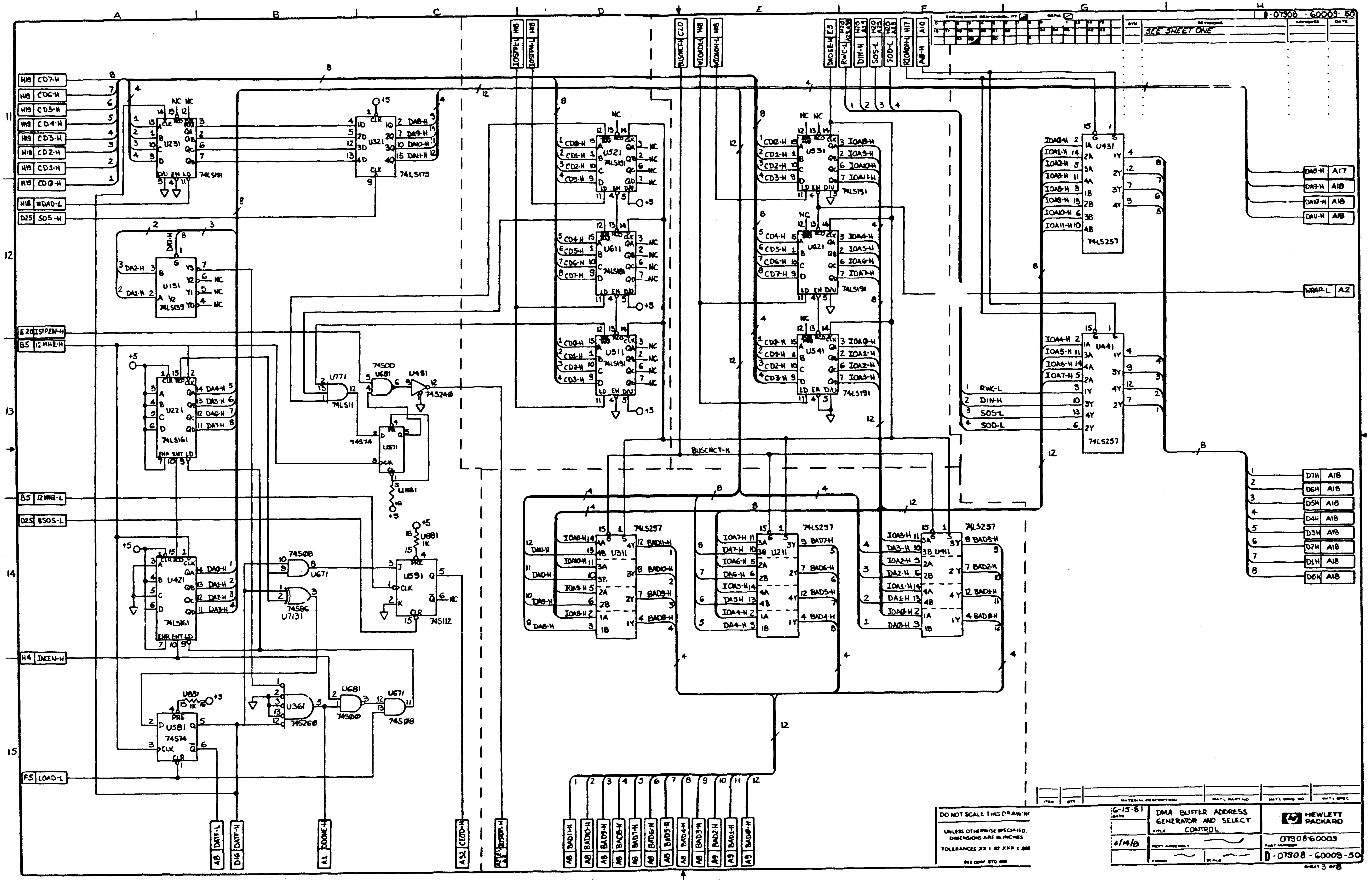
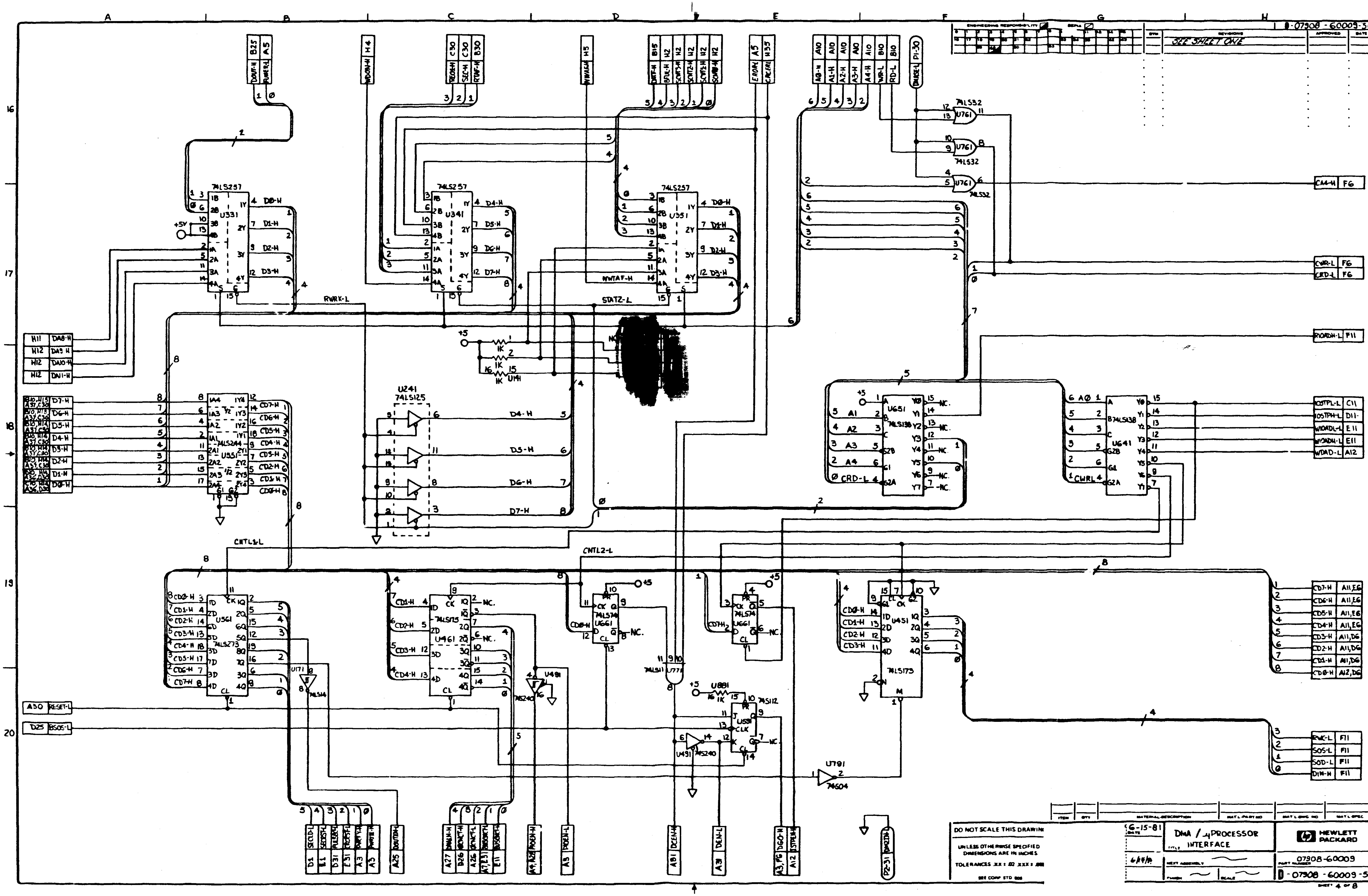
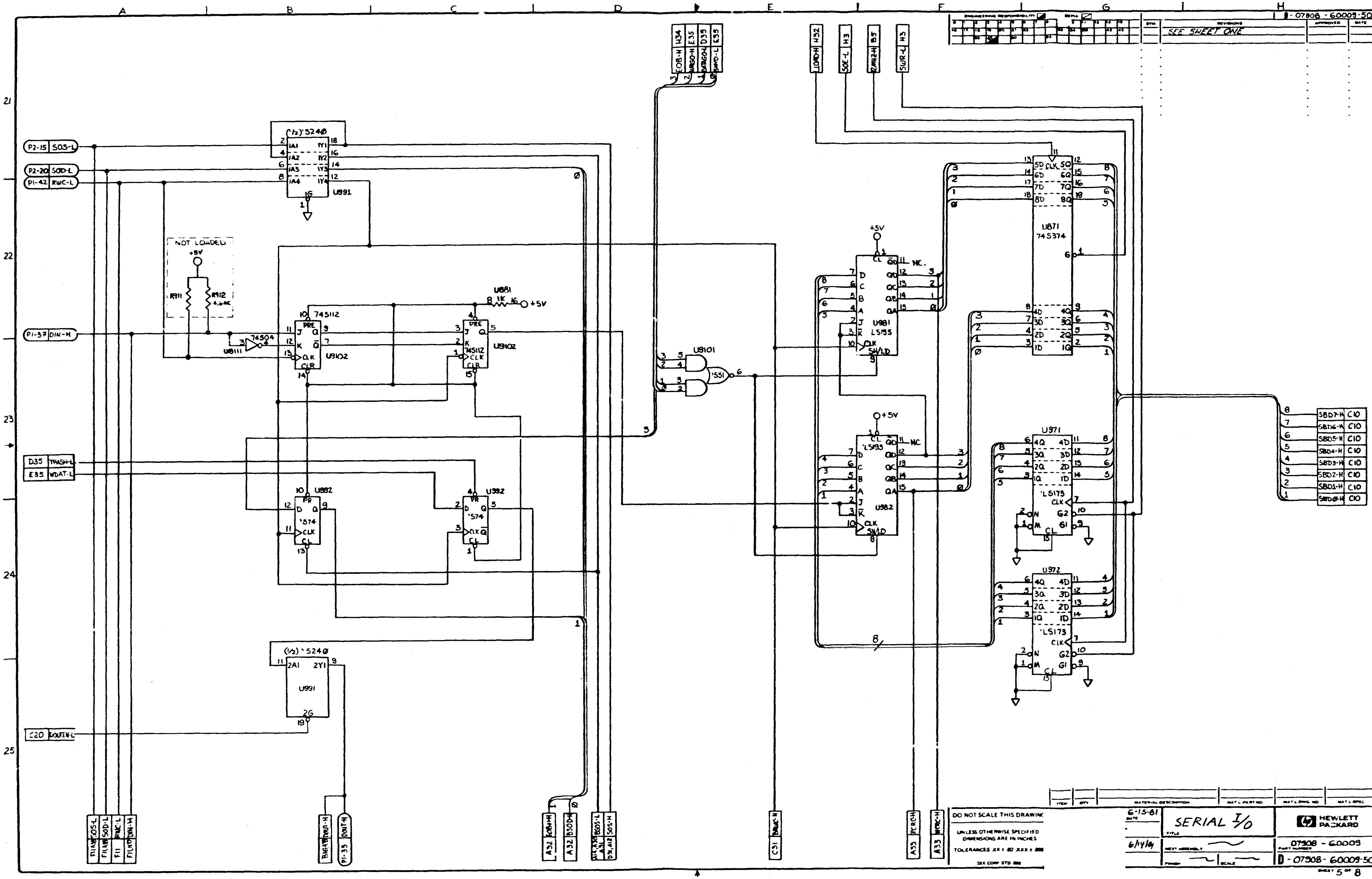
DMA HEADER AND DATA RAM
HEWLETT PACKARD
07908-60009
D-07908-60009-50
SHEET 2 OF 8



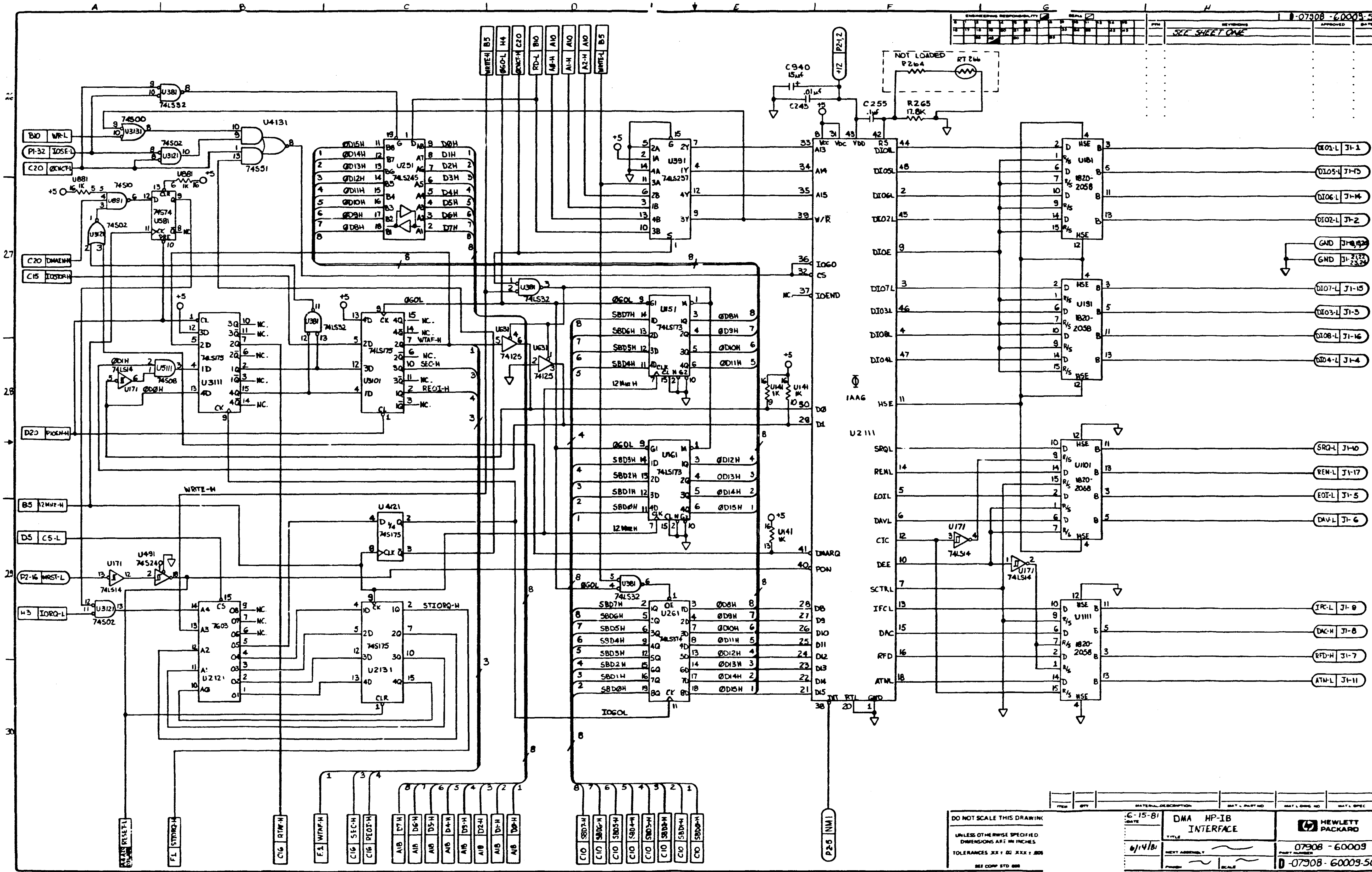
SEE SHEET ONE
D-07908-60009-50
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
6-15-81
DMA BUFFER ADDRESS GENERATOR AND SELECT CONTROL
HEWLETT PACKARD
07908-60009
D-07908-60009-50
SHEET 3 OF 8
CD7-H
CD6-H
CD5-H
CD4-H
CD3-H
CD2-H
CD1-H
CD0-H
WDAD-L
SOS-H
ISTPEN-H
12MHZ-H
12MHZ-L
BSOS-L
IKEN-H
LOAD-L
DATF-L
DATF-H
DDONE-H
CEOD-H
IOSTPI-L
IOSTPN-L
BUSCNCT-H
WIOADL-L
WIOADH-L
BADSEL-H
RWC-L
DIN-H
SOS-L
SOD-L
RIOADH-L
A0-H
DA8-H
DA9-H
DA10-H
DAV-H
WRAP-L
D7H
D6H
D5H
D4H
D3H
D2H
D1H
D0H
BAD11-H
BAD10-H
BAD9-H
BAD8-H
BAD7-H
BAD6-H
BAD5-H
BAD4-H
BAD3-H
BAD2-H
BAD1-H
BAD0-H
U251 74LS191
U321 74LS175
U131 74LS139
U221 74LS161
U421 74LS161
U581 74S74
U771 74LS11
U681 74S00
U481 74S240
U571 74S74
U671 74S08
U7131 74S86
U591 74S112
U361 74S260
U521 74LS191
U611 74LS191
U511 74LS191
U531 74LS191
U621 74LS191
U541 74LS191
U431 74LS257
U441 74LS257
U311 74LS257
U211 74LS257
U411 74LS257



D-07908-60009-50
SEE SHEET ONE
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
6-15-81
DMA / μPROCESSOR INTERFACE
HEWLETT PACKARD
07908-60009
D-07908-60009-50
SHEET 4 OF 8



SEE SHEET ONE
(½) 'S240
U991
U871
74S374
U981
LS195
U982
'LS195
U9101
'S51
74S112
U9102
U881
74S04
U8111
'S74
U992
U971
'LS173
U972
NOT LOADED
R911
R912
P2-15 SOS-L
P2-20 SOD-L
P1-42 RWC-L
P1-37 DIN-H
D35 TRASH-L
E35 WDAT-L
C20 DOUTEN-L
LOAD-H H52
SOE-L H3
2MHZ-H B5
SWR-L H3
SBD7-H C10
SBD6-H C10
SBD5-H C10
SBD4-H C10
SBD3-H C10
SBD2-H C10
SBD1-H C10
SBD0-H C10
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
6-15-81
6/14/81
SERIAL I/O
HEWLETT PACKARD
07908-60009
D-07908-60009-50
SHEET 5 OF 8



D-07908-60009-50
SEE SHEET ONE
DO NOT SCALE THIS DRAWING
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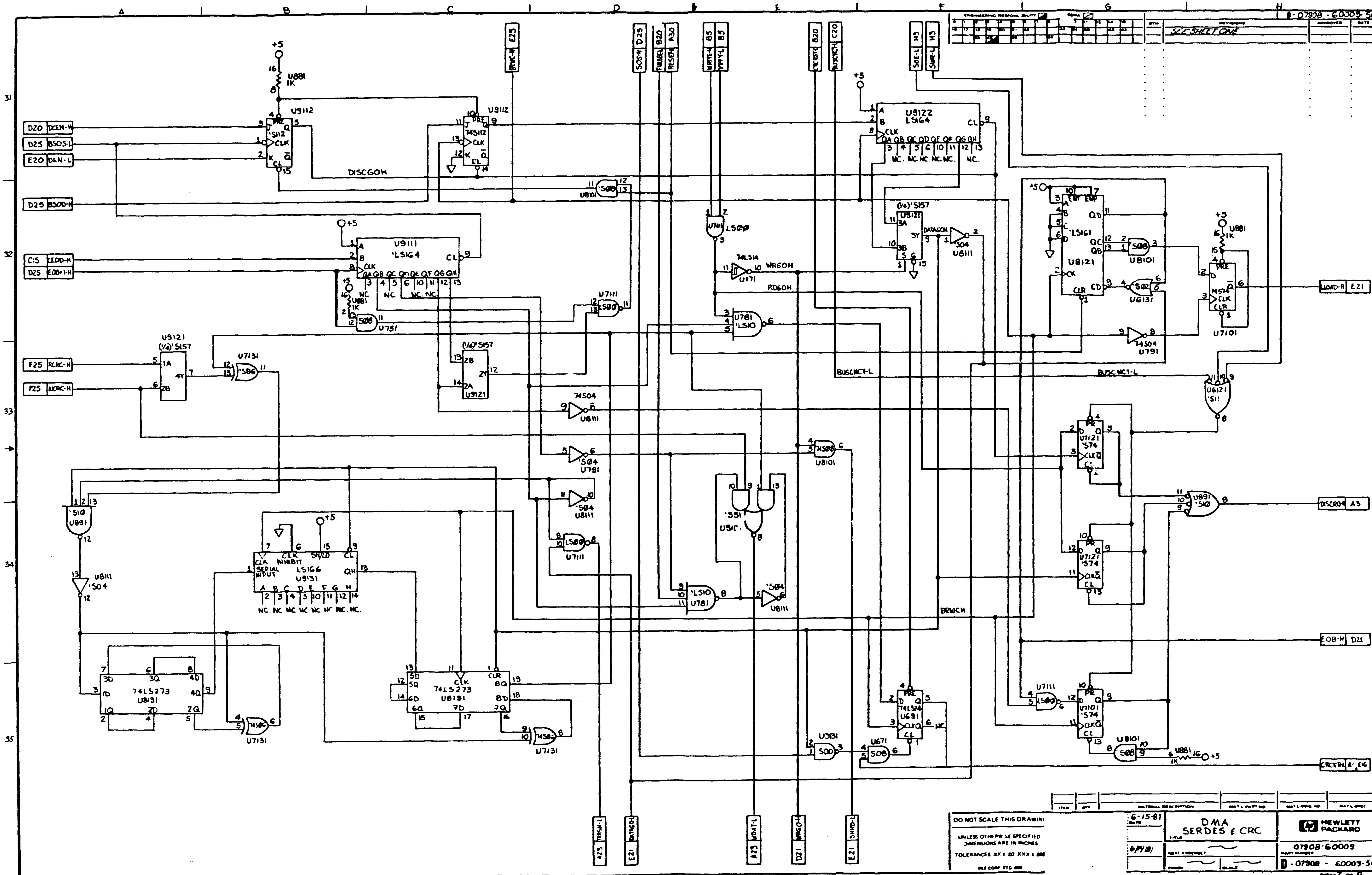
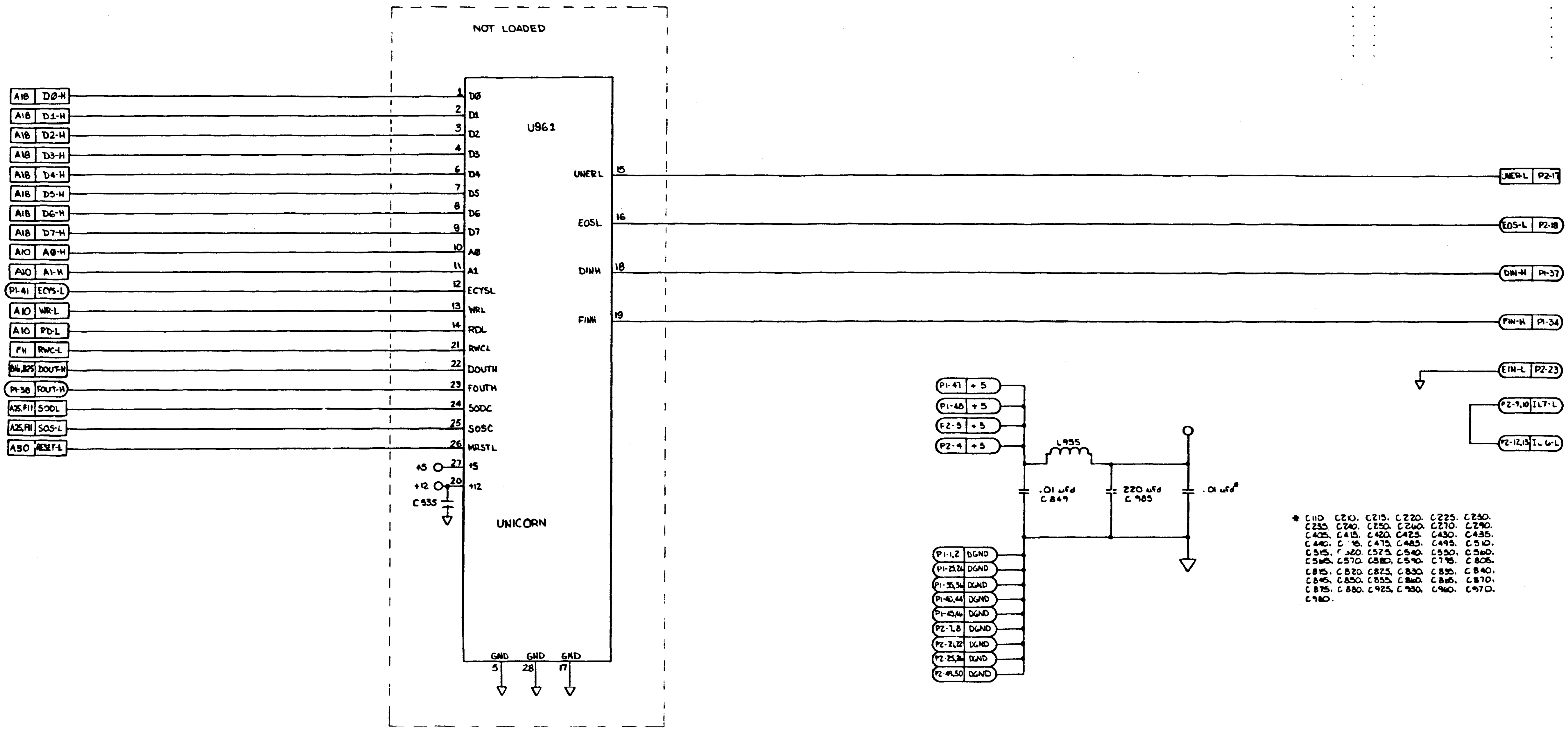
6/14/81
DMA HP-IB INTERFACE
HEWLETT PACKARD
07908-60009
D-07908-60009-50
SHEET 6 OF 8



D-07908-60009-50
SEE SHEET ONE
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
6-15-81
DMA
SERDES & CRC
HEWLETT PACKARD
07908-60009
D-07908-60009-50
SHEET 7 OF 8
DISCGOH
WRGOH
RDGOH
DATAGOH
BUSCNCT-L
BRWCH
LOAD-H E21
DISCRQ-H A3
EOB-H D21
ERCER-L A1, E16

D-07908-60009-50

SEE SHEET ONE



ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES XX ± .02 XXX ± .005

SEE CORP STD

6-15-81 DATE

6/14/81

ECC IC AND POWER DIST.

TITLE

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

07908-60009

PART NUMBER

D-07908-60009-50

SHEET 8 OF 8

P/N 07908-60002

MICROPROCESSOR PCA-A5

Series Code D-2139

ER48 D/H: C2,50A

hp

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline). (L142)

LTR	REVISIONS	DATE	INIT	MF
A	AS ISSUED	04-22-81	sb/RT	M
B	CORRECTED PER DCO 48-6199	02-09-83	db/JSK	M

A	ISSUED	sb/RT	04-22-81	MODEL 7908	STK # 07908-60002
B	48-6199	db/JSK	02-09-83	I.M.S. MICROPROCESSOR BOARD	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 34
REVISIONS				SUPERSEDES	DWG # A-07908-60002-4

ER48 D/H: C2,50A

HEWLETT-PACKARD CO. / hp /

MICROPROCESSOR INTERNAL MAINTENANCE SPECIFICATION

FOR THE

MICROPROCESSOR BOARD OPERATION

07908-60002

A	ISSUED	sb/RT	04-22-81	MODEL 7908		STK # 07908-60002
B	48-6199	db/JSK	02-09-83	I.M.S. MICROPROCESSOR BOARD		
		/	- -	BY		DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD		SHEET # 2 OF 34
	REVISIONS			SUPERSEDES		DWG # A-07908-60002-4

ER48 D/H: C2,50A

HEWLETT-PACKARD CO. hp

TABLE OF CONTENTS

A	ISSUED	sb/RT	04-22-81	MODEL 7908	STK # 07908-60002
B	48-6199	db/JSK	02-09-83	I.M.S. MICROPROCESSOR BOARD	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 3 OF 34
REVISIONS				SUPERSEDES	DWG # A-07908-60002-4

1 SCOPE

This IMS details operation of the Microprocessor Board (07908-60002) of the Low Cost Controller.

2 RELATED DOCUMENTS

1. MOSTEK Microcomputer Z80 Data Book
2. MPU Board Schematics (D-07908-60002-50)

3 BLOCK DIAGRAM

3.1 OVERVIEW

The detailed block diagram (Figure 1) shows the basic structure of the microprocessor (MPU) board. Central to the diagram is the Z80A Central Processing Unit (CPU) with its address and data buses (shown on the diagram as the Z-buses. All information to and from the CPU passes on the Z-Data bus. To prevent over loading this bus, buffers are used to distribute the load over three other buses. They are the Memory Data (MD) Bus, Processor Data (PD) Bus and Motherboard Data (D) Bus. All memory on board is connected to the Memory Data Bus. The Processor Data Bus accesses most of the remaining hardware on the board. The Motherboard Data bus connects the Z Data Bus to other boards in the drive which must communicate with the processor board.

The Z-Address Bus from the CPU is buffered and becomes the Memory Address (MA) Bus. It addresses the memory and is used by the address decode hardware for accessing circuitry on the rest of the board. Off the Memory Address Bus is the latched Motherboard Address (A) Bus. This bus is used to address other boards in the drive unit.

3.2 BRIEF DESCRIPTION OF EACH BLOCK

3.2.1 CPU

The Central Processing Unit, a Z80A-CPU, is the heart of the processor board. The Z80A-CPU has a maximum clock frequency of 4 MHz. On this board the clock frequency is 3.75 MHz.

3.2.2 Clock Circuit

The function of the processor clock circuit is to provide a reliable clock signal meeting the specifications of the processor chip.

3.2.3 Control Logic

This block of circuitry takes the control signals of the Z80A-CPU and generates signals necessary to control both on and off board memory and registers.

3.2.4 Address Decode and Bus Control Logic

This logic takes information on the address bus and generates select signals to allow accessing of the device being addressed. This section of circuitry also determines which of the three data buses are to be connected to the microprocessor data bus.

3.2.5 Memory

There are three types of memory which may be used on the board: Read Only Memory (ROM) for program storage, Read/Write Memory (RAM) for temporary storage of program variables, and Erasable Programmable Read Only Memory (EPROM) for program storage.

3.2.6 CTC

The Z80A-CTC (Counter Timer Circuit) chip provides the microprocessor board with four independently programmable counter/timers, each capable of generating an interrupt to the processor.

3.2.7 Linus Counter

The Linus Counter is a four bit counter which is cascaded with one channel of the CTC to provide a 12 bit counter which is used to keep track of sectors on the LINUS tape drive.

3.2.8 Drive Sense Register

The Drive Status Register provides the processor with eight input lines for monitoring vital drive functions.

3.2.9 Self Test Switches and Display

The self test switches and display provide user interface to the self test routines executing on the processor board.

4 LOGICAL OPERATION

4.1 MPU ADDRESS AND DATA BUS STRUCTURE

The Z80A-CPU address bus (ZA0H-ZA15H) is buffered by U141 and U171 to form the Memory Address Bus (MA0H-MA15H). Except for the ROMs (U241, U261, U271, U291, and U2101) which are on the Z-Address Bus, all other devices are on the Memory Address Bus. The Memory Address Bus is buffered by transparent latches U431 and U432 to form the Motherboard Address Bus (A0H-A11H).

The Z80 data bus (ZD0H-ZD7H) has three bi-directional buffers creating the Memory Data Bus (MD0H-MD7H) through U312, the Processor Data Bus (PD0H-PD7H) through U422, and the Motherboard Data Bus (D0H-D7H) through U412.

4.2 SOB INTERFACE

The Z80 emulator board (SOB) connects directly on the Z-Buses (ZA0H-ZA15H and ZD0H-ZD7H) through connector J1. All the control lines are directly accessable to the SOB through J1 except for M1L and RFSHL. When the SOB is connected to J1, it grounds the Bus Request line (BUSRQL) forcing the processor to tri-state all control lines except M1L and RFSHL.

Since M1L and RFSHL are not tri-stateable, a tri-state buffer (U172) is used to disable them upon a Bus Request from the SOB. The buffer is inverting because M1L is needed active high in the control logic circuitry and timing is too critical to use a non-inverting buffer and then invert the signal. Since the buffer is inverting, this requires RFSHL to be buffered twice to obtain the proper polarity.

The M1L signal from the SOB must be inverted to match the polarity required on the MPU board. Since this inverter (U172) is not tri-stateable (it is always enabled), a jumper (E158) is used to connect it to the control logic. A trace must also be cut betweem U161-27 amd U172-6 prior to connecting the SOB to the MPU board.

Also since the SOB has its own on-board clock, U181 must be removed from the board to permit the use of an external clock.

4.3 CLOCK CIRCUIT

The clock circuit takes a 7.5 MHz single-chip oscillator, Y192, and divides the output by two with flip-flop U181 to generate a 3.75 MHz signal with a 50% duty cycle. Gate U191 is used to disable the oscillator signal to the flip-flop and allow DTS-70 to control the processor clock by toggling the preset and clear inputs of the flip-flop. The 3.75 MHz output of the flip-flop goes to an active pull-up circuit to meet the Z80A-CPU clock specification which requires the minimum high level to be .6V below Vcc, and a rise and fall time of 30 nsec.

The active pull-up consists of a 74S240 inverting buffer, U172, and transistor Q193. A high output from the flip-flop turns off Q193 and causes U172 to go low. A low output from the flip-flop causes U172 to go high and turns on Q193 which quickly pulls the output of U172 close to Vcc.

4.4 CONTROL LOGIC

The control logic buffers and latches control signals from the processor and generate other signals necessary to interface with hardware both internal and external to the MPU board.

4.4.1 Control Buffer

U371 is used to buffer the ZMREQL, ZIORQL, and ZRDL lines from the processor, the power on reset (GRSTL), the latched read signal (RDL) from U351, and the latched write signal (LWRL) from U181. RDL (latched by U351 when LBSENL is active) is used by the processor to initiate reads from other boards in the drive. The buffered latched write signal (WRL) is similarly used to initiate a write. See timing diagrams (figures 2-6).

4.4.2 Control Latch

Quad-latch U382 is used to generate and latch various control signals. The first flip-flop, 1D, is used to latch the buffered I/O signal from U371. Gate U372 is used to OR the latched I/O signal and the IORQL signal to provide a latched signal which goes active soon after IORQL.

The next flip-flop, 2D, creates the latched interrupt signal, INTL. Gate U372 provides an active signal to the flip-flop when M1H goes active without a BMREQL (this condition signals an interrupt acknowledge cycle in the processor).

Flip-flop 3D is used to produce the latched memory request signal (LMREQL). Gate U352 provides an active signal to this flip-flop when buffered memory request (BMREQL) is active and there is no refresh or interrupt cycle (U342).

The last flip-flop, 4D, generates a bus enable signal, BUSENL, when there is either an I/O or memory request without an interrupt or refresh cycle (U392 and U342). J-K flip-flop, U3102, provides a latched bus enable signal (LBSENL) which is synchronized to the falling edge of the processor clock.

See timing diagrams (figures 2-6).

4.4.3 Latched Write Flip-flop

The latched write flip-flop, U181, goes active on the falling edge of the processor clock after BUSENL goes active and there is no read or power-on-reset signal. Gate U322 generates a window for toggling the flip-flop. Gate U372 will hold the flip-flop inactive if there is a read (or power-on-reset).

See timing diagrams (figures 2-6).

4.4.4 ROM Chip Enable Circuit

This circuit generates the chip enable signal for masked ROMs. When EPROMs are used in the ROM slots, the trace at E3113 grounds the chip enable and holds the EPROMs always enabled (this reduces noise on the board). The output enable is then used to select the addressed EPROM. ROMs, however, require the chip enable signal to go high for a period between each access cycle.

Jumper E3114 connects the chip enable (CEL) to the ROM chip enable circuitry. This signal is produced by J-K flip-flop U3102. On an op-code fetch, U3102 is activated on the falling edge of the processor clock when M1 is active. CEL goes inactive, when buffered read (BRDL) goes inactive. On a memory read cycle, U3102 is activated by BRDL going active and turned off when BRDL goes inactive. Note that the trace at E3113 must be cut to use ROMs. See timing diagrams (figures 2-6).

4.5 ADDRESS DECODING LOGIC

The address decoding and bus control functions are PROM based to provide maximum flexibility. PROM U311 takes address lines MA15H thru MA9H and divides the 64 Kbyte memory space into 128 blocks of 512 bytes. The A7 input of U311 is a sense line for the SOB. It allows one to disable the ROM memory space on the processor board in order to use the 16K bytes of dynamic RAM on the SOB for program memory.

The PROM's two chip select lines are tied to inverter U391 which has a resistor to +5v on its input. This allows the DTS-70 to disable the address decode logic.
The PROM pattern for the Address Decode PROM is shown in figure 13.

4.5.1 ROM and Patch EPROM Decoding

The four output lines (D0-D3) of U311 go to the bus control PROM, U341, and the transparent latch U351. This latch waits until the PROM outputs are valid before latching. The four output lines of the latch go to a 3 to 8 decoder, U361. When latched PROM output D0 is low, U361 activates the enable lines for the ROMs and/or EPROMs. The output of the decoder is synchronized by latched memory request (LMREQL) and disabled if there is a latched interrupt (INTL).

With a total of seven select lines, the ROMs and EPROMs can be configured in a number of ways. For development, all seven selects can be used with 4Kbyte EPROMs to provide a total of 28 Kbytes (see figure 7). For 8 Kbyte masked ROMs or EPROMs, six select lines can be used for a total of 48 Kbytes (see figure 8).

4.5.2 Ram, Register and Board Select Decoding

Latched PROM outputs D1 and D2 also become select lines SELA and SELB for the register and board select logic. The bus control PROM U341 generates an enable for the register and board select logic. This is output D1 of U341. It is latched by U351 and synchronized with LMREQL thru U381. This signal, OTHERL, goes to the enable of the upper half of U442, a 2-to-4 decoder with SELA and SELB as inputs. The upper half of U442 generates enables lines RAMEN1L and RAMEN2L (for the two RAM sockets) and SL1L (the board select signal for the DMA BUFFER). It also produces an enable signal for other board select and register select logic.

The lower half of U442 is enabled when the above enable and address lines A9H and A8H are both low (see gates U441 and U451). This part of U442 decodes address lines LA6H and LA7H into four 64 byte blocks for the register selects. CLST0L and CLST1L are used to reset the two self-test switch latches, ETSELL is used to select registers on a previously used ET, and MPREG enables the 2-to-4 decoder U321. U321 decodes address bits LA4H and LA5H into four 16 byte blocks. SLSENL is used to select the drive sense register and SLREVL to select the rev-rework register (see figure 9).

The board selects are generated by 3-to-8 decoder U452. It is enabled by LMREQL and the enable generated by output line 0 of the upper half of U442. U452 decodes address bits LA6H, LA7H and A8H into eight 64 byte blocks when address bit A9H is high (see figure 9). See Figure 11 for assignment of these selects to the various boards.

4.5.3 I/O Decoding

A 3 to 8 decoder (U421) is used to decode the I/O space. Address line LA7H enables the decoder when it is active high. This selects the upper 128 bytes of the I/O space. The other three address lines, LA4H-LA6H, divides this space into eight blocks of 16 bytes (see figure 10). These decoded I/O lines are used to select the PHI chip on the DMA board, the CTC chip and other devices on the MPU board. See table in figure 12 for select line assignments.

4.6 BUS CONTROL LOGIC

The bus control logic is PROM based to maintain the same flexibility as the address decoding logic. Outputs D2 and D3 of PROM U341 are latched by U351 and go to a 2-to-4 decoder, U321. The lower three outputs of this decoder enable the data bus transceivers for the Memory Data Bus (enable line MBENL), the Processor Data Bus (enable line RBSENL), and the Motherboard Data Bus (enable line MBSENL). The decoder outputs are synchronized with BUSENL thru gate U381.

Inverter U172 and pull-up resistor R197 are provided to disable the data bus transceivers for Signature Analysis and DTS-70 by grounding the data bus enable line (DBENH).

The inputs to the PROM include the four output lines from the address decode PROM, the latched I/O signal (LIORQL) and the outputs of three gates, U451, U461 and U322. Gate U451 helps to separate bus control functions for the board selects and register selects. LIORQL, gate U322 and both U461 gates, help separate bus control functions on the I/O mapped board and register selects. See Figure 14 for the PROM pattern.

4.7 MEMORY

The on board memory consists of ROM, RAM and EPROM. The processor board has six slots for 8 Kbyte ROMs or EPROMs for a total of 48 Kbytes. It also has one slot for a 4 Kbyte EPROM.

There are two RAM slots for use with either 1 Kbyte or 2 Kbyte RAMs. There are 3 Kbytes of memory space available for RAM.

4.8 CTC

Channel 0 of the CTC (U211) is triggered by the Track Crossing signal (TKX) which comes from off-board and is buffered with Schmitt-trigger U3101. This channel is used by the firmware in instrumenting seeks.

Channel 1 is cascaded with Channel 0 to produce a 16 bit counter which is used by the Command Executive.

Channel 2 is cascaded with the Linus counter and is used for seeks in the Linus tape drive. The output of this channel (CTCMOH) is buffered by U371 and sent to the Linus TIB board.

Channel 3 of the CTC is triggered by the sector timing pulse signal (STPL) which comes from off-board and is buffered by Schmitt-trigger U3101. This channel is used to count sectors in read and write firmware routines.

The interrupt line of the CTC is tied directly to the maskable interrupt input of the Z80A-CPU. The CTC uses Mode 2 interrupt configuration.

4.9 LINUS COUNTER

The Linus Counter, U462, is a four-bit down counter which can be loaded by the processor and read through the drive sense register (see figure 16). Gate U441 generates a load signal to the counter when the Linus counter select line (LCNTRL) and latched write (LWRL) are active.

The counter is clocked by an offboard signal (CTCTH) from the Linus TIB board. This signal is buffered by by Schmitt-trigger U3101 and inverted by U391 to obtain the proper polarity.

The Linus Counter is cascaded with Channel 2 of the CTC. The CTC is clocked by gate U461 when the Linus Counter reaches a count of zero (MIN/MAX output active) and CTCTH is active. The MIN/MAX output (CTCLOH) also goes offboard to the TIB.

4.10 DRIVE SENSE REGISTER

The drive sense register consists of two multiplexers, U472 and U492. The A channel of the multiplexer connects eight sense lines to the Processor Bus. The table in fig.15 defines the bits in the register. All of the sense lines sense lines come directly off the mother board and into the sense register except for the index pulse (RB1). It is buffered with a schmitt-trigger, U3101, and used to toggle a flip-flop, U332. This allows the processor to catch the short index pulse by watching for the register bit to toggle with each index pulse.

The lower two bits of the B channel indicate the status of the self-test latches. The third bit is not used. The fourth bit is used by the firmware to detect the connection of the Signature Analysis test fixture used in manufacturing. The upper four bits of the B channel contains the status (count) of the Linus Counter. See figure 16.

Memory address bit 0 (MAOH) is used to select between the channels. Gate U451 is used to enable the output of the multiplexers by taking the sense register select line (SLSENL) and gating it with the buffered read signal (BRDL) to produce a low true signal when the former two are active.

4.11 SELF-TEST SWITCHES AND LED DISPLAY

The two self-test switches, S120 and S140, set two flip-flops (both in U142) when activated. These flip-flops can be read by channel B of the drive sense register (see figure 16). Each flip-flop can be cleared by addressing it (processor read or write to latch addresses).

The self-test display, DS129, is a seven-segment LED driven by an eight-bit latch, U131. Resistor pack, R130, limits current in the LEDs. Gate U381 clocks the latch when the LED select line (LEDSLL) and latched write (LWRL) are asserted.

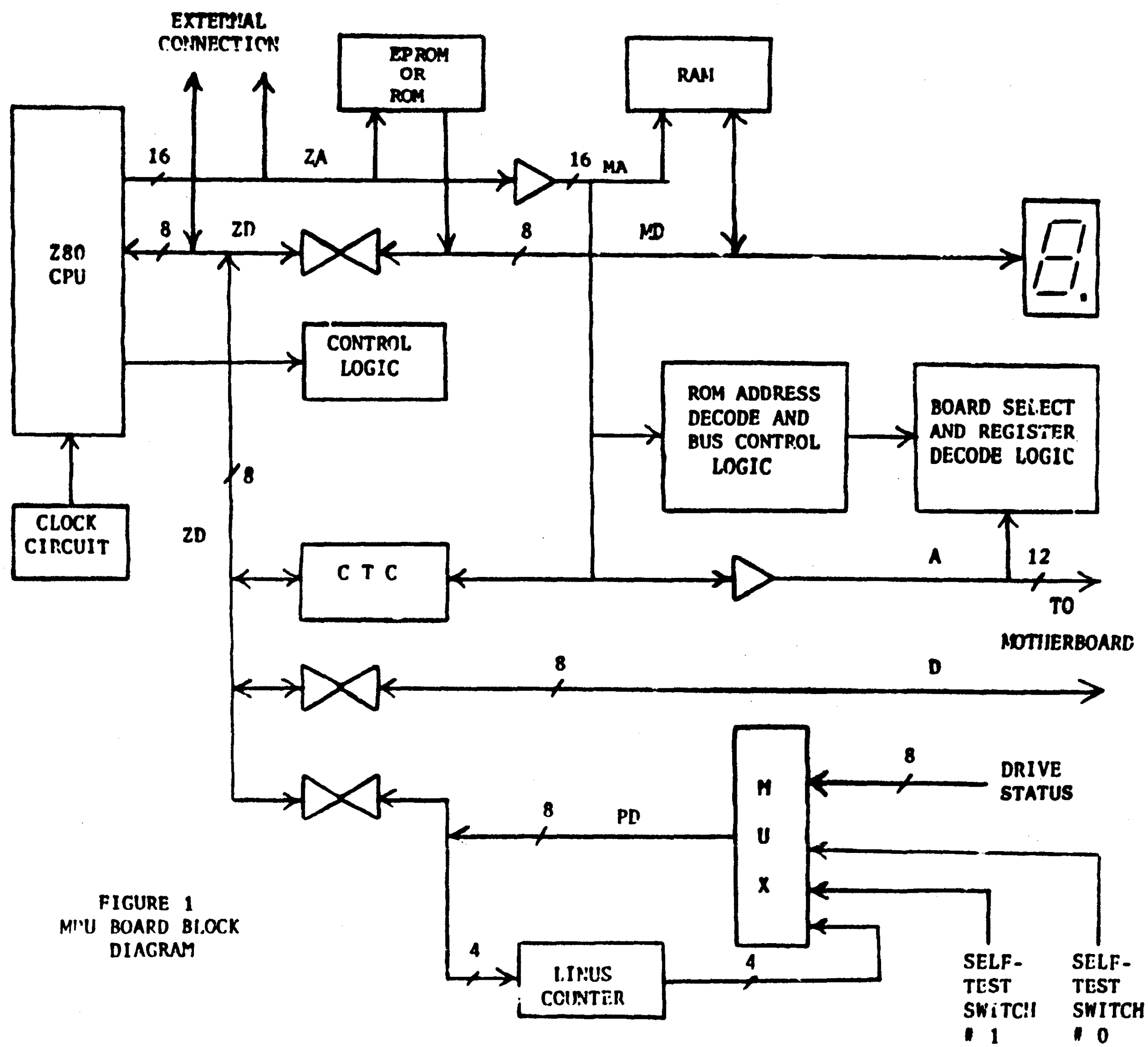


FIGURE 1
MPU BOARD BLOCK DIAGRAM

HEWLETT-PACKARD CO.

MODEL 7908
STK NO 07908-60002
DATE April 22, 1981
SHEET NO 19 OF 34
DWG NO 07908-60002-4

HEWLETT-PACKARD CO. / hp /

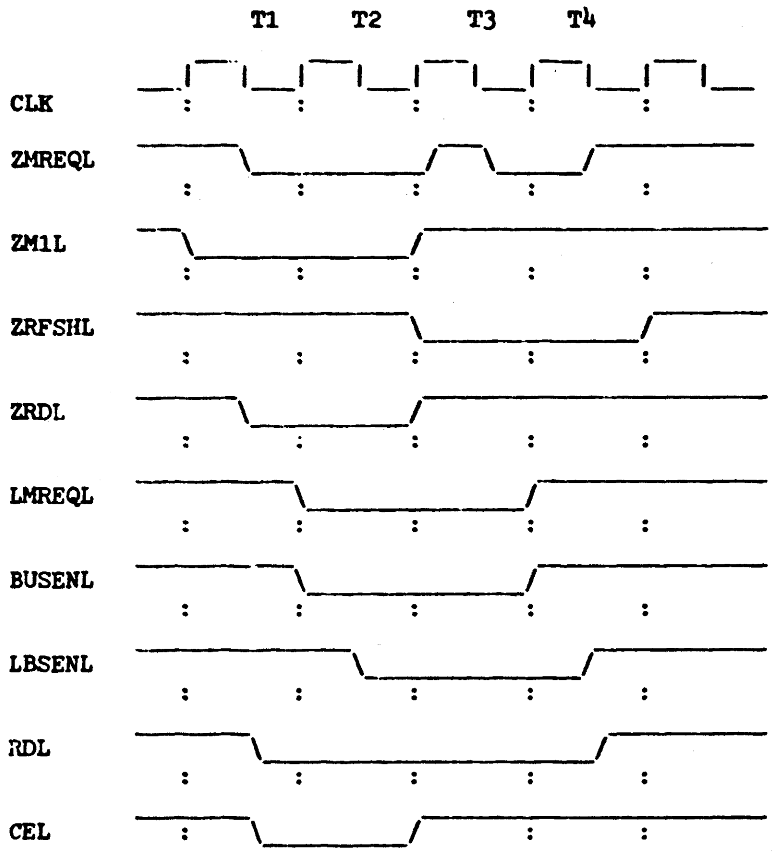


FIGURE 2
OP-CODE FETCH CYCLE

A	ISSUED	sb/RT	04-22-81	MODEL 7908	STK # 07908-60002
B	48-6199	db/JSK	02-09-83	I.M.S. MICROPROCESSOR BOARD	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 20 OF 34
REVISIONS				SUPERSEDES	DWG # A-07908-60002-4

ER48 D/H: C2,50A

HEWLETT-PACKARD CO.

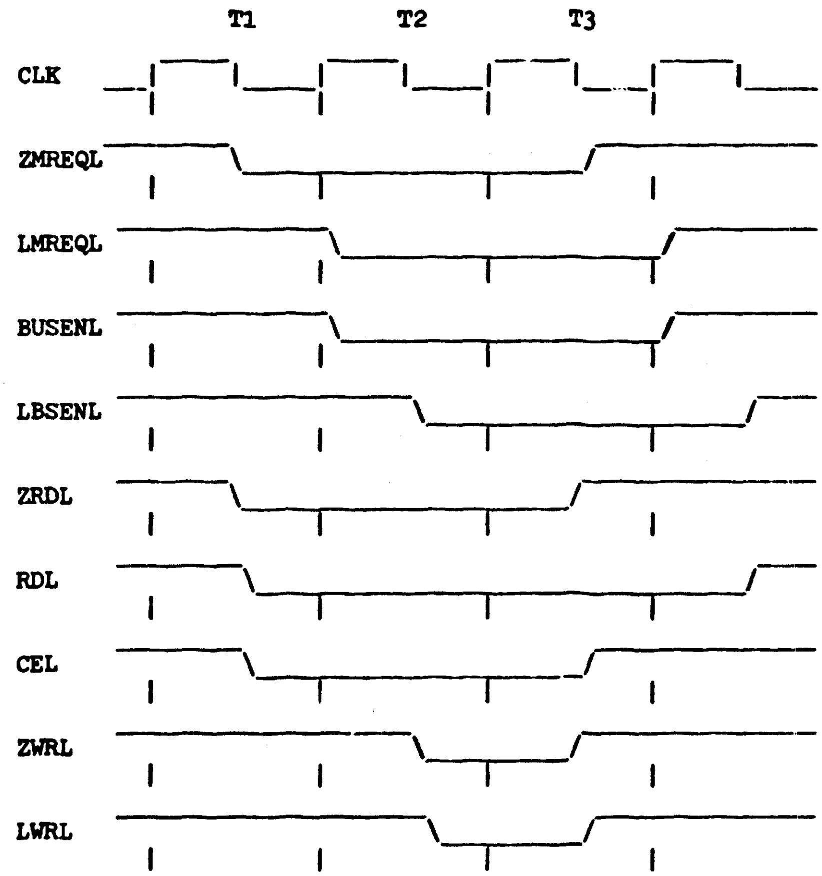


FIGURE 3
MEMORY READ/WRITE CYCLE

A	ISSUED	sb/RT	04-22-81	MODEL 7908	STK # 07908-60002
B	48-6199	db/JSK	02-09-83	I.M.S. MICROPROCESSOR BOARD	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 21 OF 34
REVISIONS				SUPERSEDES	DWG # A-07908-60002-4

ER48 D/H: C2,50A

HEWLETT-PACKARD CO.

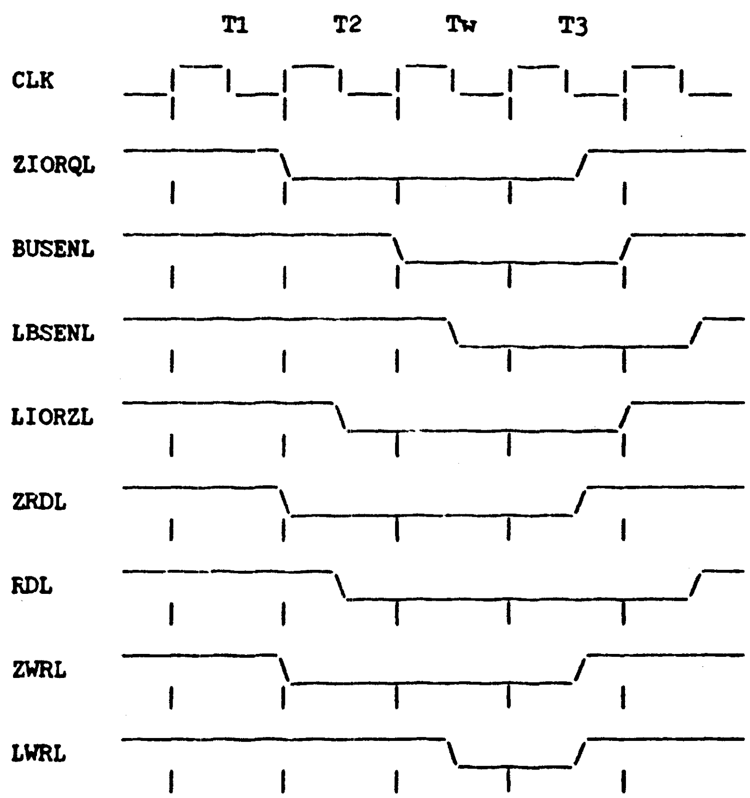


FIGURE 4
I/O READ/WRITE CYCLE

A	ISSUED	sb/RT	04-22-81	MODEL 7908	STK # 07908-60002
B	48-6199	db/JSK	02-09-83	I.M.S. MICROPROCESSOR BOARD	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 22 OF 34
REVISIONS				SUPERSEDES	DWG # A-07908-60002-4

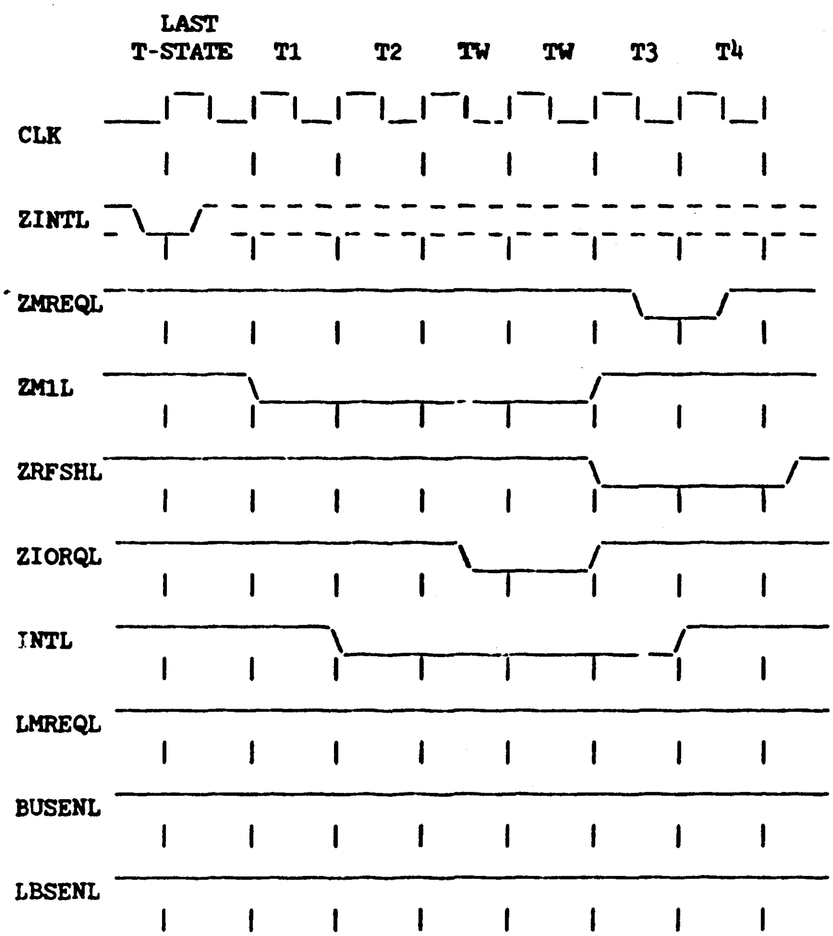


FIGURE 5
INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

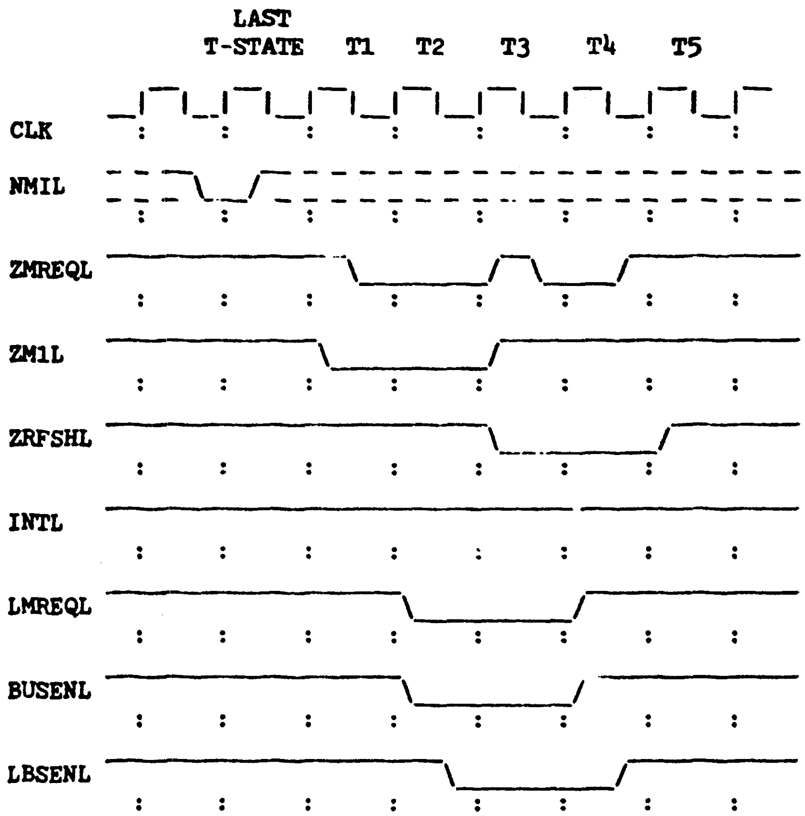
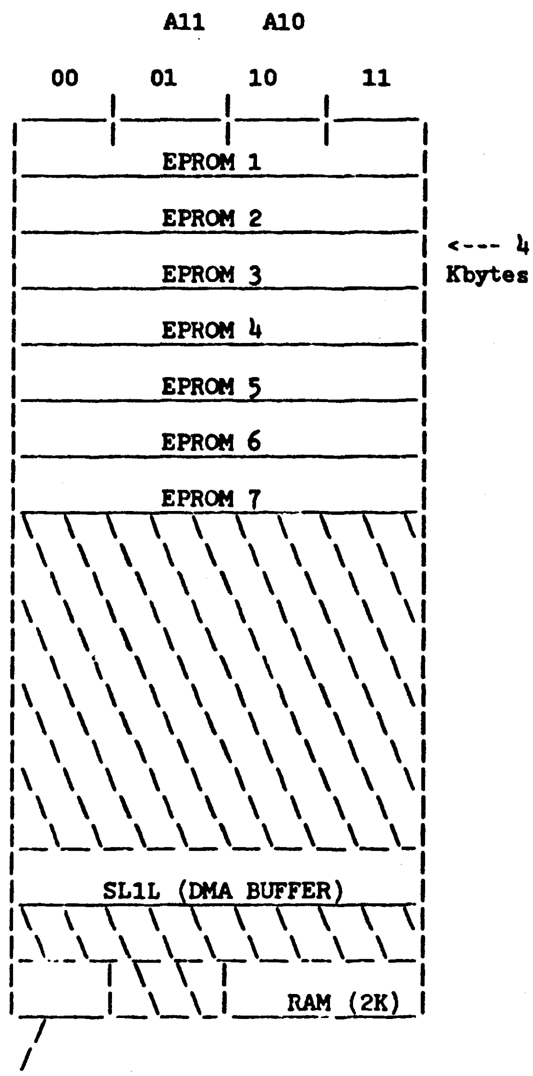


FIGURE 6
NON-MASKABLE INTERRUPT REQUEST

HEWLETT-PACKARD CO. hp

A15	A14	A13	A12
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



REGISTER & BOARD SELECTS (SEE FIGURE 9)

FIGURE 7
MEMORY MAP (EPROMs)

A	ISSUED	sb/RT	04-22-81	MODEL 7908	STK # 07908-60002
B	48-6199	db/JSK	02-09-83	I.M.S. MICROPROCESSOR BOARD	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 25 OF 34
	REVISIONS			SUPERSEDES	DWG # A-07908-60002-4

hp

HEWLETT-PACKARD CO.

A15	A14	A13	A12	00 / 01 / 10 / 11	
0	0	0	0	EPROM 1	
0	0	0	1		
0	0	1	0	EPROM 2	
0	0	1	1		
0	1	0	0	EPROM 3	<--- 8 Kbytes
0	1	0	1		
0	1	1	0	EPROM 4	
0	1	1	1		
1	0	0	0	EPROM 5	
1	0	0	1		
1	0	1	0	EPROM 6	
1	0	1	1		
1	1	0	0	\\\\\\\\	
1	1	0	1	SL1L (DMA BUFFER)	<--- 4 Kbytes
1	1	1	0	\\\\\\\\	
1	1	1	1	(register & board selects) \\\\ RAM (2K)	

REGISTER & BOARD SELECTS (SEE FIGURE 9)

FIGURE 8
MEMORY MAP (EPROMs)

A	ISSUED	sb/RT	04-22-81	MODEL 7908	STK # 07908-60002
B	48-6199	db/JSK	02-09-83	I.M.S. MICROPROCESSOR BOARD	
		/	- -	BY	DATE APR 12, 1984
	P.C. #	APPR	DATE	APPD	SHEET # 26 OF 34
	REVISIONS			SUPERSEDES	DWG # A-07908-60002-4

A15	A14	A13	A12	A11	A10
1	1	1	1	0	0

A9	A8	A7	A6				
0	0	0	0	CLST1L			
0	0	0	1	ETSELL			
0	0	1	0	CLST0L			
0	0	1	1	NOT USED	SLSENL	NOT USED	SLREVL
0	1	0	0	NOT DECODED			
0	1	0	1	NOT DECODED			
0	1	1	0	NOT DECODED			
0	1	1	1	NOT DECODED			
1	0	0	0	SL2L			
1	0	0	1	SL7L			
1	0	1	0	SL9L			
1	0	1	1	SL8L			
1	1	0	0	SL4L			
1	1	0	1	SL3L			
1	1	1	0	SL0L			
1	1	1	1	SL6L			

- 64 bytes

FIGURE 9
REGISTER & BOARD SELECT MEMORY MAP

SP;.NF

A7	A6	A5	A4	
0	0	0	0	NOT DECODED
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	S L 5 L (-16 bytes)
1	0	0	1	(NOT USED)
1	0	1	0	P R R B I L
1	0	1	1	C T C S L L
1	1	0	0	L C N T R L
1	1	0	1	S P T S T L
1	1	1	0	(NOT USED)
1	1	1	1	L E D S L L

FIGURE 10
I/O MAP

SELECT LINE	ADDRESS	SYMBOL	NAME
SL0L	F380	SAL	SERVO SELECT A
SL1L	D000	BUFSL	DMA BUFFER SELECT
SL2L	F200	SBL	SERVO SELECT B
SL3L	F340	DMASL	DMA SELECT
SL4L	F300	RWSL	READ/WRITE SELECT
SL5L	80(I/O)	IOSL	I/O SELECT (PHI)
SL6L	F3C0	TIBSL	TIB SELECT
SL7L	F240	FSSL	FORMATTER/SEPARATOR SELECT
SL8L	F2C0	-Not Used-	--- Not Used ---
SL9L	F280	FLSL	FAULT LATCH SELECT

FIGURE 11
BOARD SELECT ASSIGNMENT

ADDRESS	SYMBOL	FUNCTION
80	SL5L	I/O (PHI) SELECT
90	-Not Used-	---Not Used ---
A0	PRRB1L	Preset Disc Status Register Bit 1
B0	CTCSLL	CTC SELECT
C0	LCNTRL	LINUS COUNTER SELECT (Write Only)
D0	SPTSTL	Speed OK Test (Not Used on 7908)
E0	-Not Used-	---Not Used ---
F0	LEDSLL	LED DISPLAY SELECT (Write Only)

FIGURE 12
I/O SELECTS

ADDRESS DECODE PROM
(U311)

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
10H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
20H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
30H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
40H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
50H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
60H	F	F	F	F	F	F	F	F	5	5	5	5	5	5	5	5
70H	F	F	F	F	F	F	F	F	1	1	7	7	3	3	3	3
80H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
90H	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
A0H	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
B0H	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
C0H	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
D0H	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
E0H	F	F	F	F	F	F	F	F	5	5	5	5	5	5	5	5
F0H	F	F	F	F	F	F	F	F	1	1	7	7	3	3	3	3

FIGURE 13
ADDRESS DECODE PROM PATTERN

ER48 D/H: C2,50A

HEWLETT-PACKARD CO. hp

BUS CONTROL PROM

(U341)

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	7	B	F	3	7	B	F	3	7	B	F	3	7	B	F	3
10H	7	B	F	3	7	B	F	3	7	B	F	3	7	B	F	3
20H	7	B	F	3	7	B	F	3	7	B	F	3	7	B	F	3
30H	7	B	F	3	7	B	F	3	7	B	F	3	7	B	F	3
40H	7	B	F	3	7	B	F	3	7	B	F	3	7	B	F	3
50H	7	B	F	3	7	B	F	3	7	B	F	3	7	B	F	3
60H	7	B	F	3	7	B	F	3	7	B	F	3	7	B	F	3
70H	7	B	F	3	7	B	F	3	7	B	F	3	7	B	F	3
80H	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
90H	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
A0H	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
B0H	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
C0H	9	9	D	D	1	1	1	1	5	5	5	5	5	5	5	5
D0H	1	1	1	1	1	1	1	1	5	5	5	5	5	5	5	5
E0H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
F0H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

FIGURE 14
BUS CONTROL PROM PATTERN

A	ISSUED	sb/RT	04-22-81	MODEL 7908	STK # 07908-60002
B	48-6199	db/JSK	02-09-83	I.M.S. MICROPROCESSOR BOARD	
		/	- -	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 32 OF 34
REVISIONS				SUPERSEDES	DWG # A-07908-60002-4

OGBL	OFH	IGBL	PKDET	TCH	ONH	INDXL	CYLL

BIT 7 BIT 0

DRIVE SENSE REGISTER
(ADDRESS F0D0)

CYLL - Cylinder Address LSB

INDXL - Latched Index Pulse

ONH - On Track

TCH - Track Crossing Pulse

PKDET - Peak Detect (Position Error Signal)

IGBL - Inner Guard Band

OFH - Off Track

OGBL - Outer Guard Band

FIGURE 15

DRIVE SENSE REGISTER

- CHANNEL A -

HEWLETT-PACKARD CO. /hp/

				SA			
LC3H	LC2H	LC1H	LC0H	TEST	1	ST1H	ST0H

BIT 7 BIT 0

SELF-TEST LATCHES/LINUS COUNTER REGISTER

(ADDRESS F0D1)

ST0H - Self-Test Switch Latch 0

ST1H - Self-Test Switch Latch 1

1 - Not Used, Always High

SA TEST - Test flag for SA Test ET

LC0H-LC3H - Contents of Linus Counter

FIGURE 16

DRIVE SENSE REGISTER

- CHANNEL B -

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-68002
07908-66002
07908-60002

DATE CODE : D-2139

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C104	0160-5298	CAP .01UF 20%
C107	0160-5298	CAP .01UF 20%
C112	0160-5298	CAP .01UF 20%
C114	0160-5298	CAP .01UF 20%
C137	0160-5298	CAP .01UF 20%
C144	0160-5298	CAP .01UF 20%
C163	0160-5298	CAP .01UF 20%
C164	0160-5298	CAP .01UF 20%
C178	0160-5298	CAP .01UF 20%
C188	0160-4350	CAP 68PF 5%
C205	0160-5298	CAP .01UF 20%
C215	0160-5298	CAP .01UF 20%
C225	0160-5298	CAP .01UF 20%
C235	0160-5298	CAP .01UF 20%
C245	0160-5298	CAP .01UF 20%
C255	0160-5298	CAP .01UF 20%
C265	0160-5298	CAP .01UF 20%
C305	0160-5298	CAP .01UF 20%
C318	0160-5298	CAP .01UF 20%
C328	0160-5298	CAP .01UF 20%
C335	0160-5298	CAP .01UF 20%
C345	0160-5298	CAP .01UF 20%
C358	0160-5298	CAP .01UF 20%
C365	0160-5298	CAP .01UF 20%
C378	0160-5298	CAP .01UF 20%
C385	0160-5298	CAP .01UF 20%
C398	0160-5298	CAP .01UF 20%
C408	0160-5298	CAP .01UF 20%
C418	0160-5298	CAP .01UF 20%
C425	0160-5298	CAP .01UF 20%
C438	0160-5298	CAP .01UF 20%
C445	0160-5298	CAP .01UF 20%
C458	0160-5298	CAP .01UF 20%
C460	0180-0229	CAP 33UF 10%
C465	0160-5298	CAP .01UF 20%
C478	0160-5298	CAP .01UF 20%
C485	0160-5298	CAP .01UF 20%
C498	0160-5298	CAP .01UF 20%
DS129	1990-0452	INDICATOR
MP1	07908-80002	BD-ETCHED
MP2	7120-6830	LABEL-INFO
MP3	0403-0455	EXTR-PC BD #5
MP4	1480-0116	PIN GRV .062X.25
Q193	1853-0405	XSTR PNP 2N4209
R130	1810-0283	NETWORK-RES DIP
R138	0757-0280	RES 1K 1%.125
R139	0757-0280	RES 1K 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-68002
07908-66002
07908-60002

DATE CODE : D-2139

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R148	0757-0442	RES 10K 1%.125
R154	0757-0280	RES 1K 1%.125
R156	0757-0280	RES 1K 1%.125
R165	0757-0280	RES 1K 1%.125
R181	0757-0280	RES 1K 1%.125
R182	0757-0280	RES 1K 1%.125
R183	0757-0280	RES 1K 1%.125
R190	0757-0274	RES 1.21K 1%.125
R191	0757-0422	RES 909 1%.125
R195	0757-0279	RES 3.16K 1%.125
R196	0757-0346	RES 10 1%.125
R197	0757-0280	RES 1K 1%.125
R3111	1810-0083	NETWORK-RES DIP
R362	1810-0083	NETWORK-RES DIP
R411	1810-0162	NTWK-RES DP 4.7K
S120	3101-1675	SW-TGL DPST NS
S140	3101-1675	SW-TGL DPST NS
TP171	0360-1682	TERM-PIN
TP173	0360-1682	TERM-PIN
U112	1818-1611	IC-MEMORY
U131	1820-1461	IC SN74273N
U141	1820-2024	IC SN74LS244N
U142	1820-1112	IC SN74LS74N
U161	1820-2298	IC-Z80A-CPU
U171	1820-2024	IC SN74LS244N
U172	1820-1633	IC SN74S240N
U181	1820-0629	IC SN74S112N
U191	1820-1367	IC SN74S08N
U211	1820-2301	IC-Z80A-CTC
U3101	1820-1416	IC SN74LS14N
U3102	1820-0629	IC SN74S112N
U311	1816-1528	IC MEMORY
U312	1820-2075	IC SN74LS245N
U321	1820-1072	IC SN74S139N
U322	1820-1201	IC SN74LS08N
U332	1820-1112	IC SN74LS74N
U341	1816-1499	MEMORY PROM
U342	1820-0681	IC SN74S00N
U351	1820-1676	IC SN74S373AN
U352	1820-1449	IC SN74S32N
U361	1820-1216	IC SN74LS138N
U371	1820-2075	IC SN74LS245N
U372	1820-1367	IC SN74S08N
U381	1820-1208	IC SN74LS32N
U382	1820-1191	IC SN74S175N
U391	1820-0683	IC SN74S04N
U392	1820-1158	IC SN74S51N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-68002
07908-66002
07908-60002

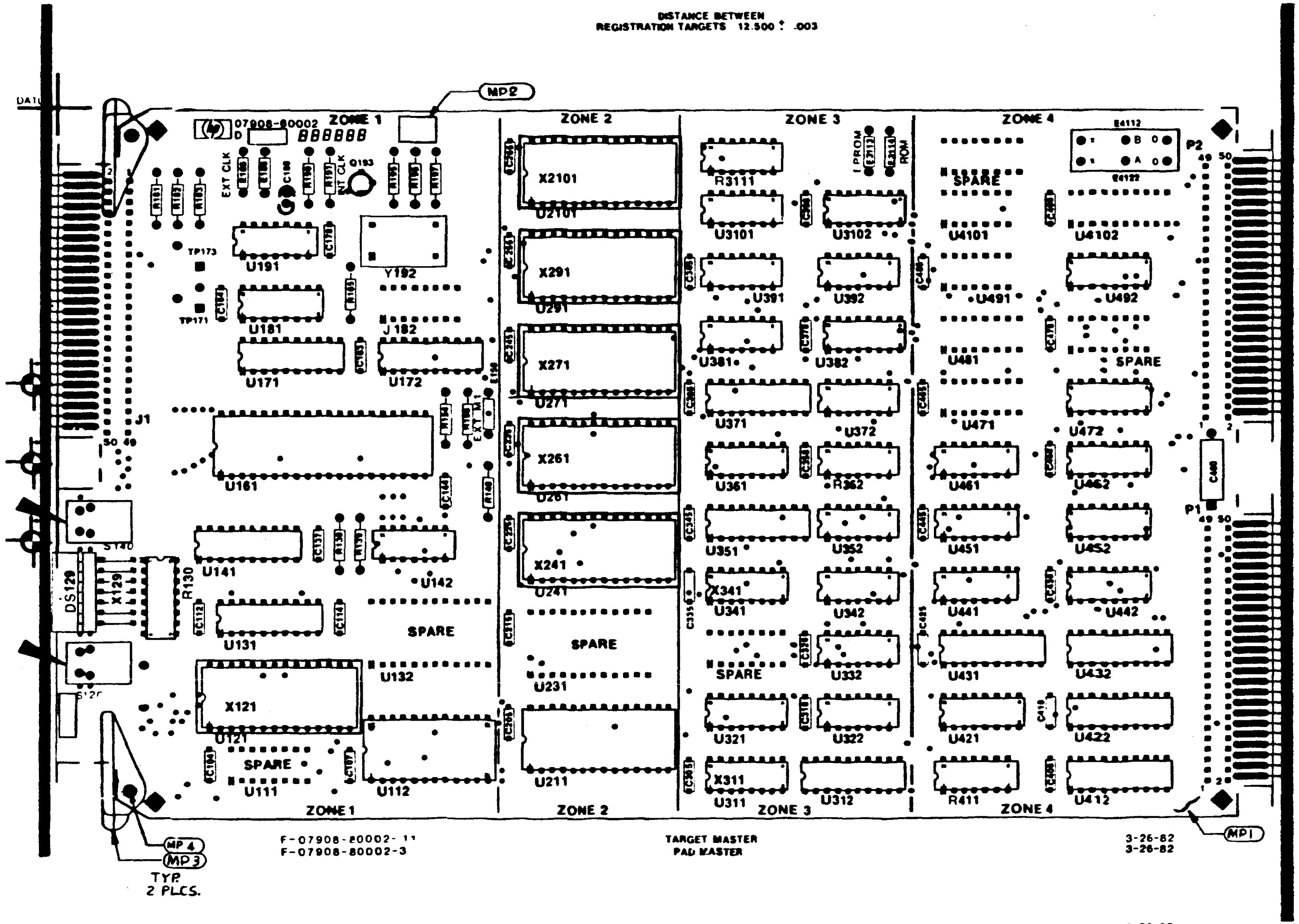
DATE CODE : D-2139

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U412	1820-2075	IC SN74LS245N
U421	1820-1240	IC SN74S138N
U422	1820-2075	IC SN74LS245N
U431	1820-2102	IC SN74LS373N
U432	1820-2102	IC SN74LS373N
U441	1820-1208	IC SN74LS32N
U442	1820-1072	IC SN74S139N
U451	1820-1449	IC SN74S32N
U452	1820-1240	IC SN74S138N
U461	1820-1197	IC SN74LS00N
U462	1820-1278	IC SN74LS191N
U472	1820-1438	IC SN74LS257AN
U492	1820-1438	IC SN74LS257AN
X121	1200-0861	SKT-IC 28 CONT
X129	1200-0640	SKI-DSPL 14-CONT
X2101	1200-0861	SKT-IC 28 CONT
X241	1200-0861	SKT-IC 28 CONT
X261	1200-0861	SKT-IC 28 CONT
X271	1200-0861	SKT-IC 28 CONT
X291	1200-0861	SKT-IC 28 CONT
Y192	1813-0198	CLOCK OSC 7.5MHZ

END OF MATERIAL LIST.

REV	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	[illegible]	[illegible]
B	[illegible]	[illegible]	[illegible]
C	ADD NOTE 7 PER PPCO-48-4033	[illegible]	[illegible]
D	DATE CODE WAS 2106, PER PPCO 48-4188	[illegible]	[illegible]
E	REVD NOTE 2 DATE CODE WAS B-2128 PER PC 48-4226	[illegible]	[illegible]
F	DATE CODE WAS 2128; ADDED NOTE 7; RENUMBERED NOTES / PPCO 48-[illegible]	[illegible]	[illegible]
G	DELETE NOTE 8, CLARIFY MASKING NOTE, MARK SPARES / PPCO 48-4311	[illegible]	[illegible]
H	BD REV WAS CODED "REV-C-" E 101, DELETED COMPONENT OUTLINE; PHOTO-DATE WAS 20-82 PER PCO 48-4637	[illegible]	[illegible]
J	JUMPERS E 313, E 185 & E 186 REMOVED, ADDED NOTE 7. PER PCO 4967.	[illegible]	[illegible]
K	REMOVED NOTES 2-7 PER PCC-6350	[illegible]	[illegible]

F-07908-60002-1



UNLESS OTHERWISE SPECIFIED

THIS BOARD CONFORMS TO CORPORATE AUTOMATIC INSERTION STANDARDS

NOTES

1

ASSEMBLY DATE CODE 2139

11-19-80	MICROPROCESSOR ASSEMBLY
2/,3/6	HEWLETT PACKARD
	07908-60002
	F-07908-60002-1

SHEET 1 OF 1

ER48 D/H: C2, 50A

HEWLETT-PACKARD CO. / hp /

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline). (L204)

LTR	REVISIONS	DATE	INIT	MF
A	AS ISSUED	12-02-81	sb/ML	M
B	REVISED PER PC48-4345, REV B	05-14-82	jr/ML	M
C	UPDATED PER PC48-6178	02-08-83	sd/JSK	M

A	ISSUED	sb/ML	12-02-81	MODEL 7908	STK # 07908-69002
B	48-4345	jr/ML	05-14-82	UPDATE AND REVISION PROCEDURE	
C	48-6178	sd/JSK	02-08-83	BY	DATE APR 12, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 6
REVISIONS				SUPERSEDES	DWG # A-07908-69002-1

HEWLETT-PACKARD CO. hp

UPDATING AND REVISION PROCEDURE

07908-69002

This procedure contains instructions for modification of the microprocessor (MPU) PCA, 07908-60002 to version 07908-69002.

RELATED DOCUMENTS AND PROCEDURES:

07908-68002	Material List
07908-66002	Material List
F-07908-60002-1	Assembly Drawing
D-07908-60002-50	Schematic
F-07908-60002-20	Modification Drawing
A-07908-90047-1	I/O Line Processing Procedure

REVISIONS:

The first revision which may be revised is B-2106. All prior assemblies are to be scrapped.

B-2106	(PCO 48-4053)	Removes components used in the "Speed OK" portion of the circuitry since it is used on the 791X and not the 7908.
	(PCO 48-4071)	Changes 64K EPROMS to 64K ROMS.
	(PCO 48-4091)	Increases ROM Memory space from 32K to 40K by changing EPROMS.
B-2128	(PCO 48-4188)	Changes configuration of EPROMS from 2-8K and 6-4K to 5-8K EPROMS, and changes Decode Proms. Also adds 2 jumpers to allow 1611A Logic Analyzer to be hooked up to J1 connector. Changes Date code to 2128.
B-2133	(PCO 48-4226)	Updates Firmware. Changes Date Code to 2133.
	(PCO 48-4245)	Restructures EPROMS from MPU Board to Disc Module Assembly. This allows EPROM changes to be made without affecting the MPU PCA.

REVISIONS: (con't)

B-2139	PCO (48-4345)	Adds space for 6th 8K EPROM thus bringing total memory space to 48K and changes Decode Prom. Deletes all sockets on the board except for those on EPROMS. Changes Date Code to 2139.
	PCO (48-4538)	Changes Extractors on PCA so they have identification number indicating where the PCA is to be placed in the card cage.
	PCO (48-4657)	Changes EPROM sockets to a more reliable type.

PROCEDURE:

1. Inspect all boards for general mechanical and cosmetic defects. Repair all visible defects.

2. Identify all boards with the following logo:

07908-69002

2139

3. Affix, near the logo, a 7120-5480 label which indicates the month and year of final inspection.

   A) On Board Revision: B-2106 (to get to 2128)

      1) See PCO 48-4188 and Mod Drawing 07908-60002-20,Rev.D
      2) Remove Decode PROM 07908-89008 at U111
      3) Connect U161-27 to U171-6 using 30 AWG White wire as shown on the Mod Drawing.
      4) Install Jumper Wire (8159-0005) at E185.

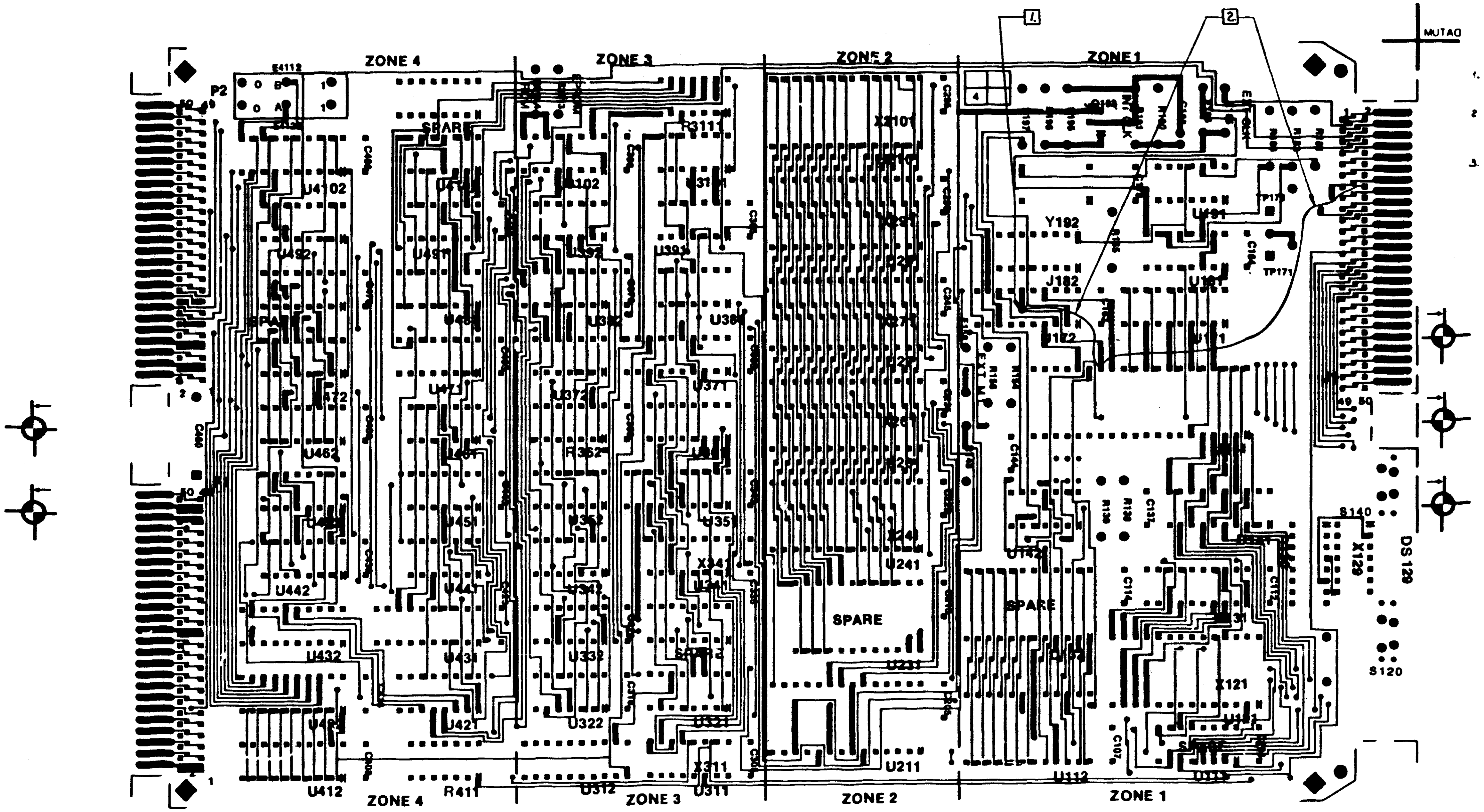
B) On Board Revision B-2128 (to get to 2139)

1) See PCO 48-4345 and Mod Drawing 07908-60002-20,Rev.E.
2) Replace Decode PROM at U311 with 07908-89018 PROM.
3) Connect the following points together using 30 AWG White wire as shown on Mod Drawing:

U121-26	to	U121-27
U121-1	to	U121-28
U111-4	to	U111-12
U111-5	to	U111-9
U111-6	to	U111-10
U111-7	to	U111-11

C) On Board Revision B-2139

1) See PCO 48-4657
2) If the Board has been returned because one or more of the Sockets on the EPROMS have failed, and the Socket Part Number is 1200-0567, all of the sockets must be removed and replaced with Part Number 1200-0861 Sockets.



NOTES:
1. DATE CODE PER BOARD REVISION - C- 15: C-2139.
2. DRILL OUT FEED THRU CHECK FOR OPEN BETWEEN U-172-15 / GROUND.
3. ADD TWO JUMPERS USE RED WIRE, P/N 8150-2188.

CIRCUIT SIDE 4 OF 4

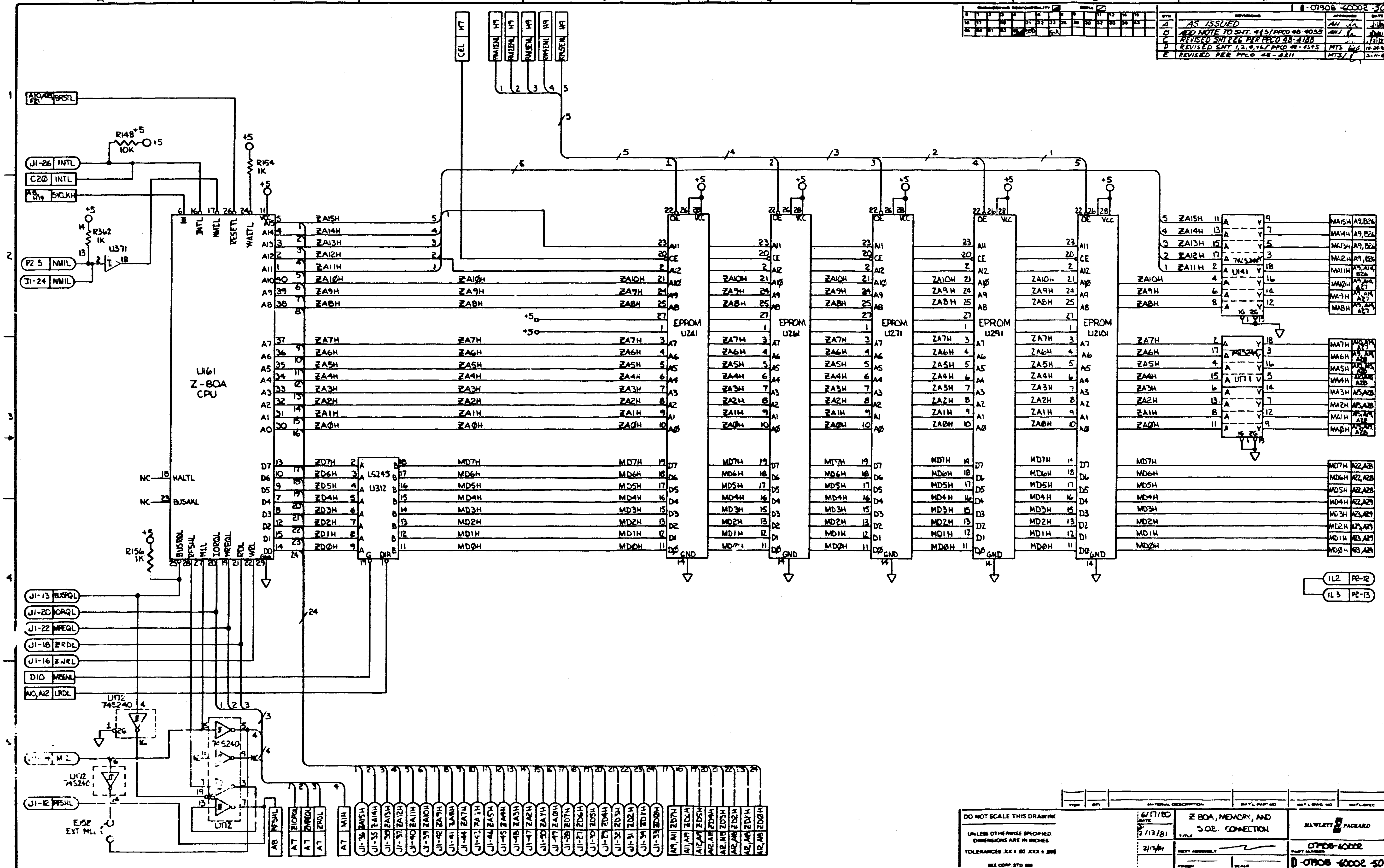
GRAPHICS-CIRCUIT SIDE

MICROPROCESSOR MODIFICATION DRAWING

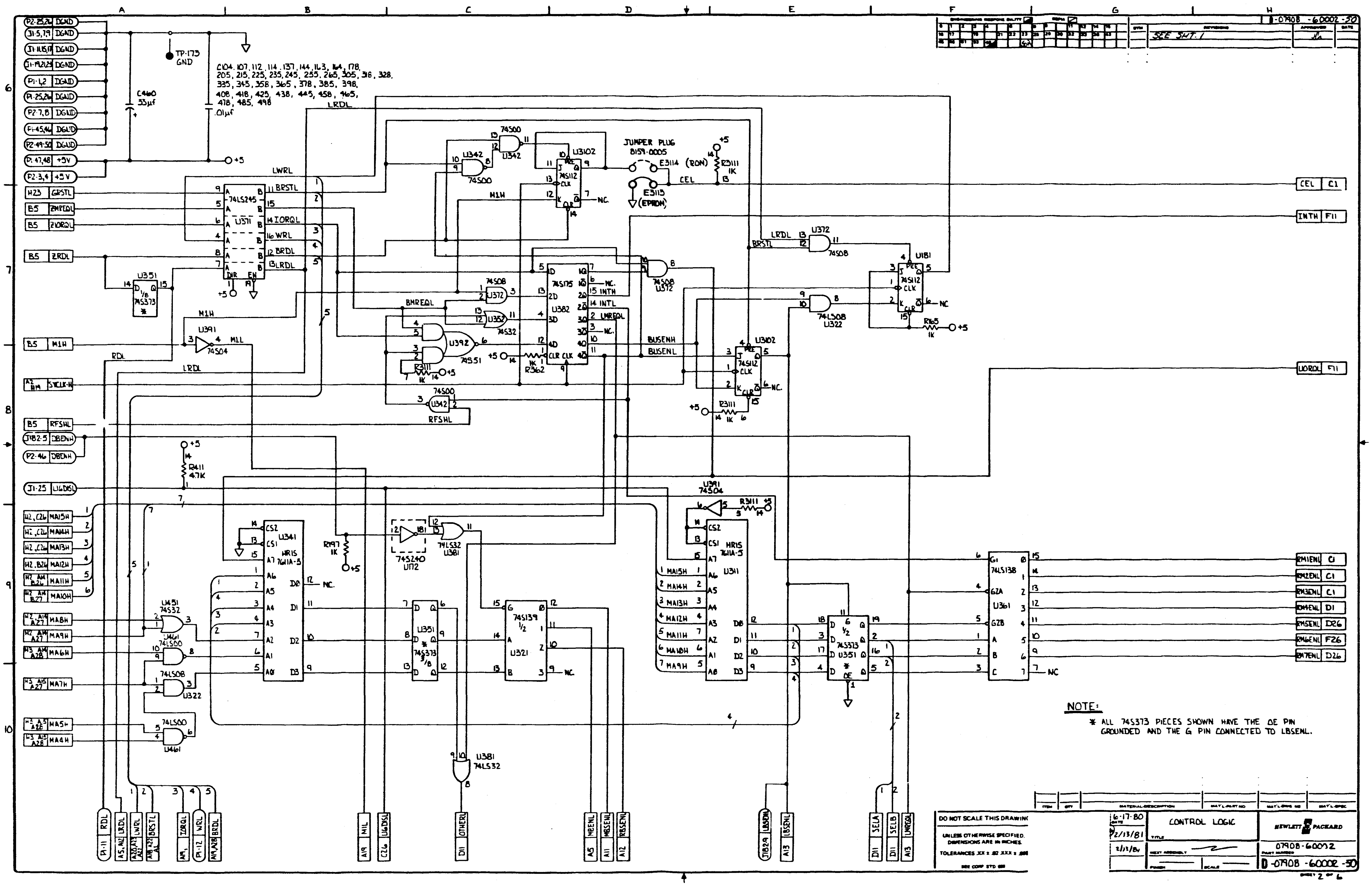
HEWLETT PACKARD

07908-60002

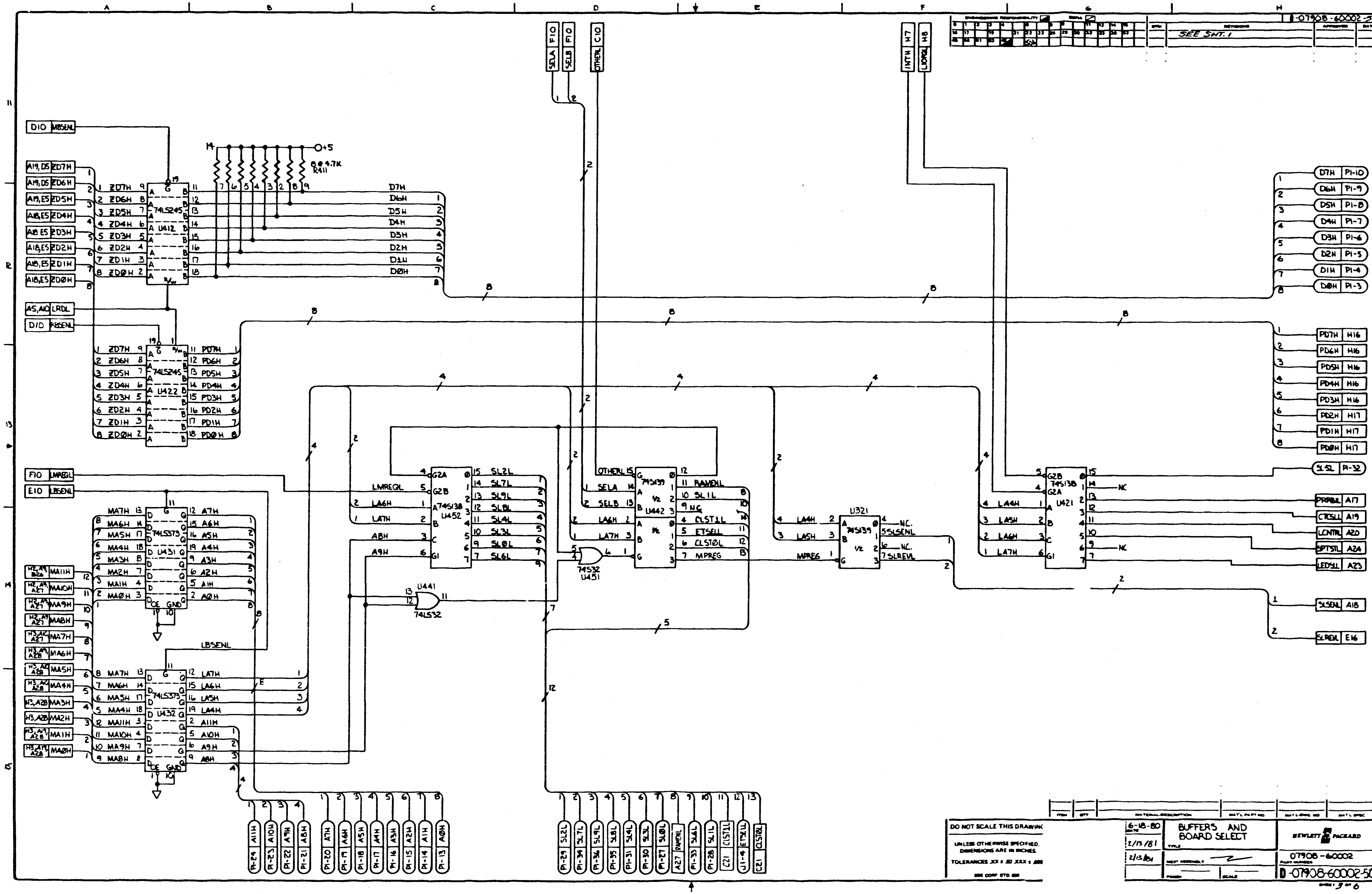
D 07908 60002 21



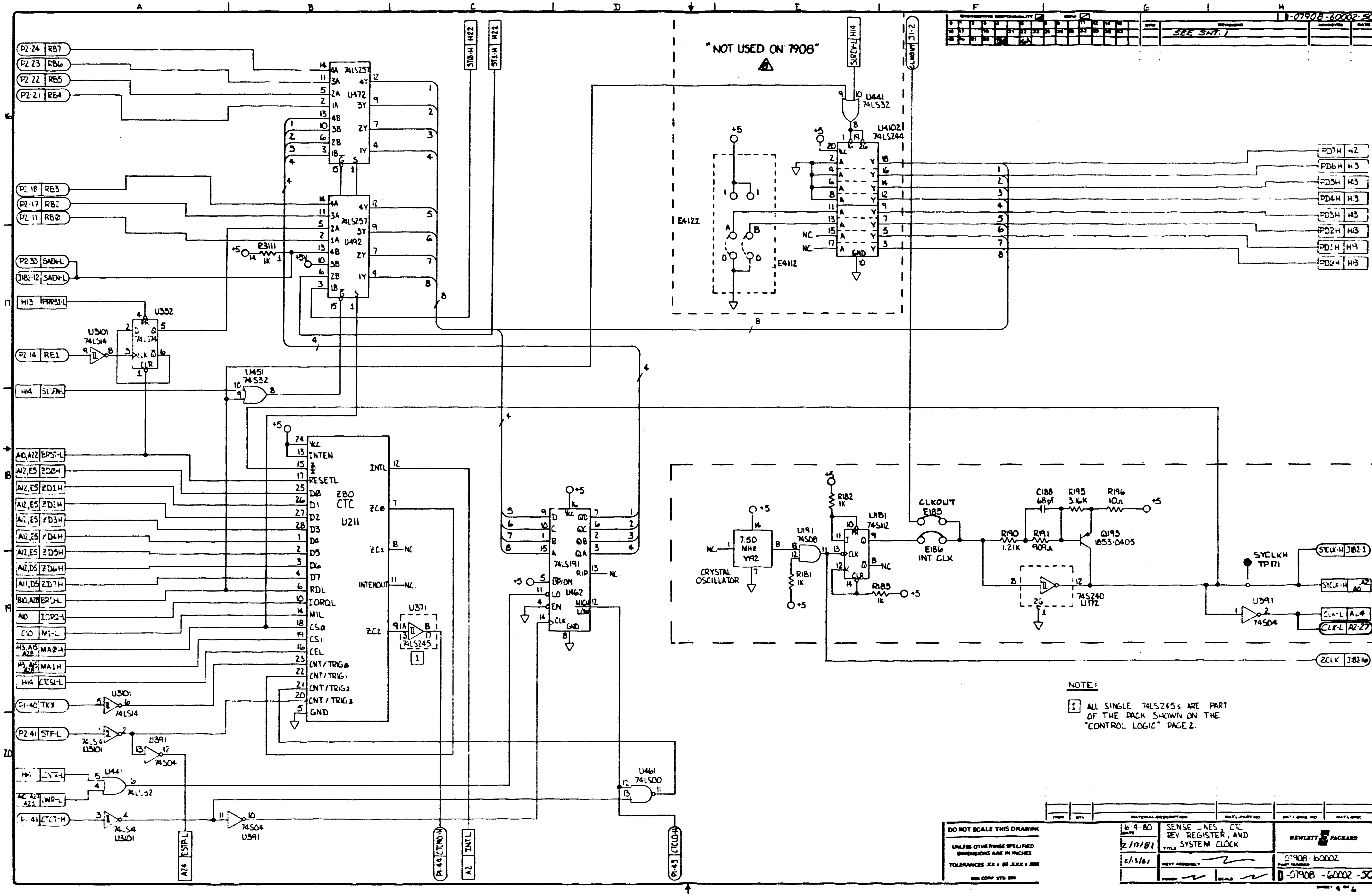
D-07908-60002-50
A AS ISSUED
B ADD NOTE TO SHT. 4&5 / PPCO 48-4055
C REVISED SHT 2&6 PER PPCO 48-4188
D REVISED SHT 1,2,4,5&6 PPCO 48-4345
E REVISED PER PPCO 48-4211
U161
Z-80A
CPU
EPROM
U241
EPROM
U261
EPROM
U271
EPROM
U291
EPROM
U2101
LS245
U312
74LS244
U141
74LS244
U171
U172
74S240
R148
10K
R154
1K
R362
1K
R156
1K
U371
E/58
EXT M1L
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
6/17/80
2/13/81
2/13/81
Z 80A, MEMORY, AND S.O.E. CONNECTION
HEWLETT PACKARD
07908-60002
D-07908-60002-50
SHEET 1 OF 6



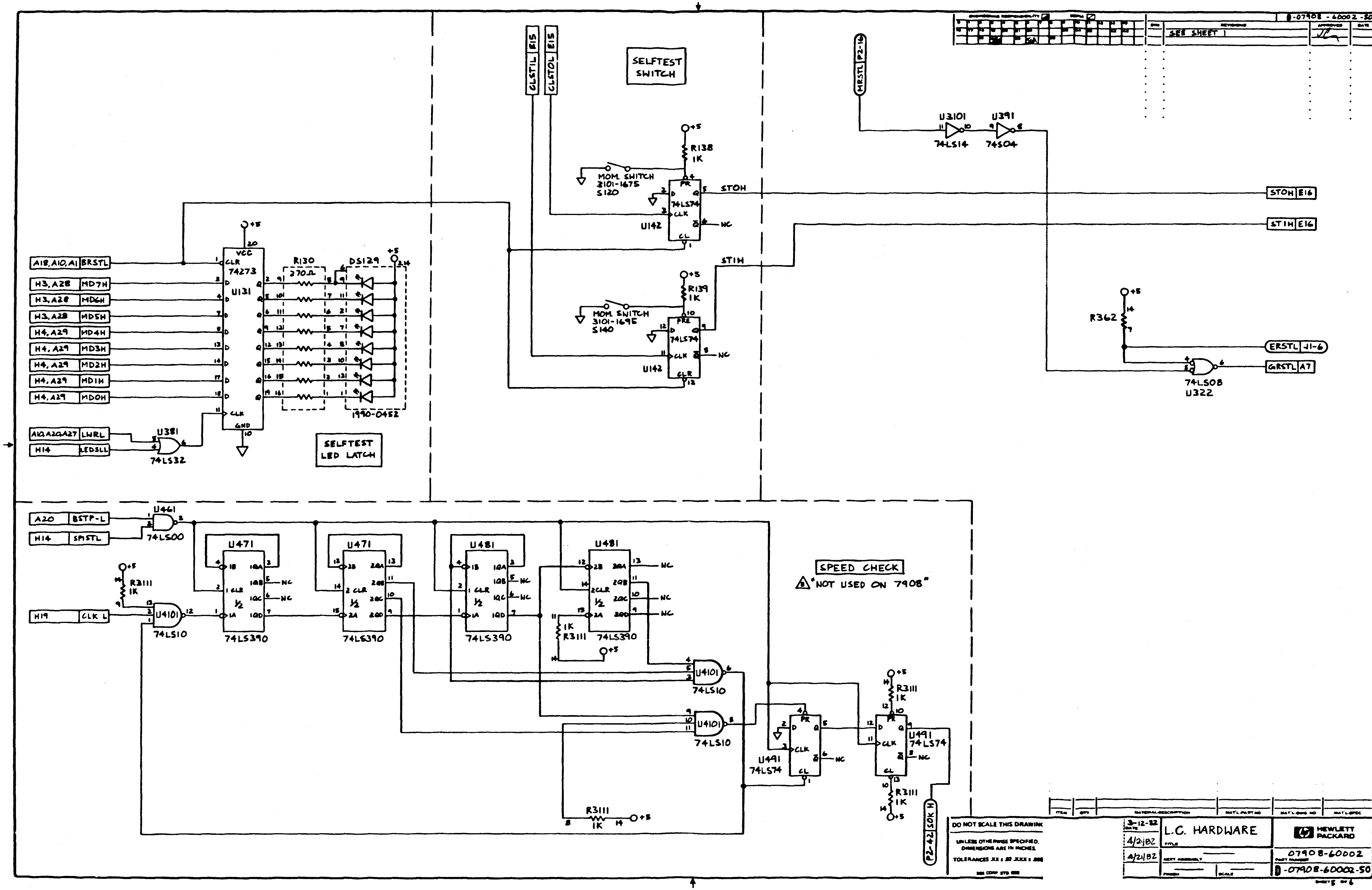
CONTROL LOGIC
NOTE:
* ALL 74S373 PIECES SHOWN HAVE THE OE PIN GROUNDED AND THE G PIN CONNECTED TO LBSENL.
JUMPER PLUG 8159-0005
E3114 (ROM)
E3113 (EPROM)
TP-173 GND
C460 33µf
C104, 107, 112, 114, 137, 144, 163, 164, 178, 205, 215, 225, 235, 245, 255, 265, 305, 316, 328, 335, 345, 358, 365, 378, 385, 398, 408, 418, 425, 438, 445, 458, 465, 478, 485, 498
.01µf
74LS245 U371
74S175 U382
74S112 U3102
74S112 U181
74S138 U361
74S139 1/2 U321
HRIS 7611A-5 U341
HRIS 7611A-5 U311
74S373 U351
74S240 U112
74LS32 U381
74S51 U392
NOTE:
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
HEWLETT PACKARD
07908-60002
D-07908-60002-50
SEE SHT. 1



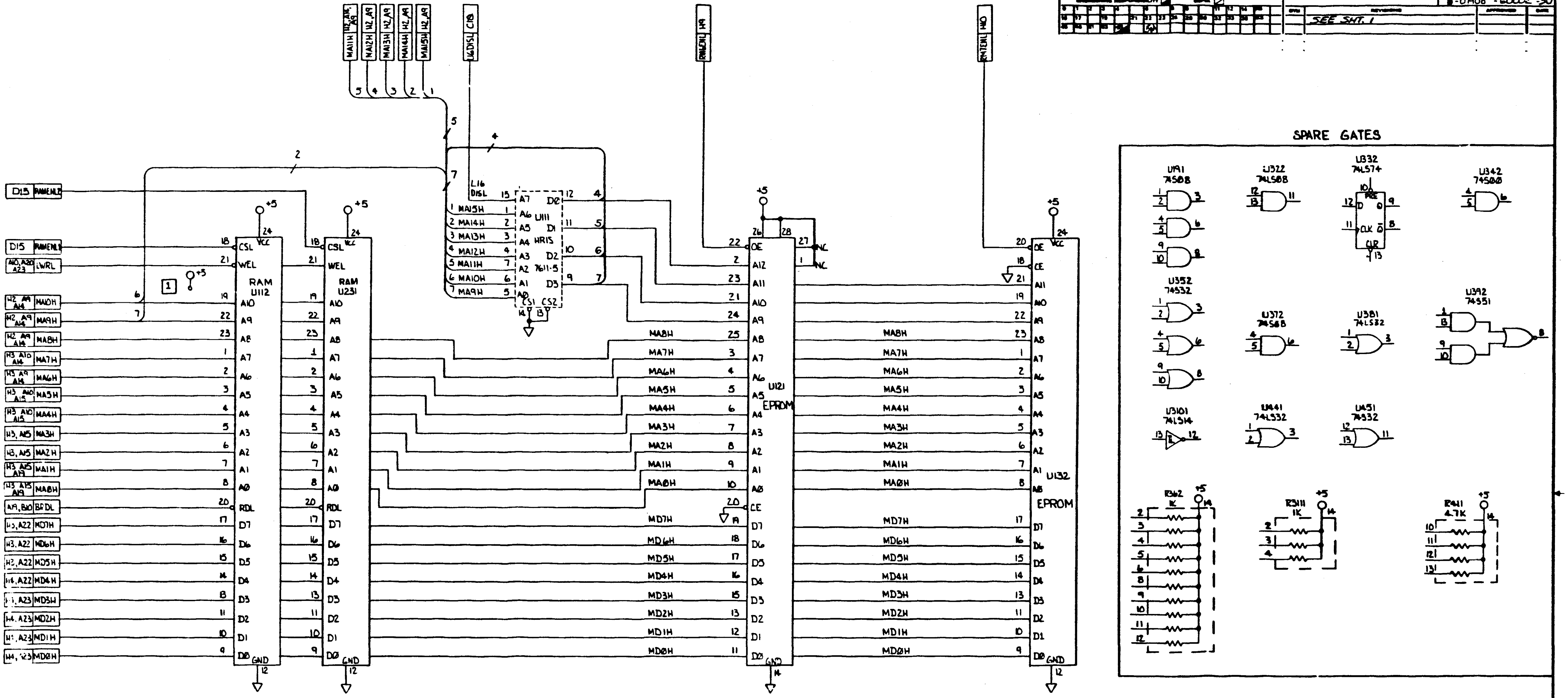
D-07908-60002-50
SEE SHT. 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
6-18-80
2/13/81
BUFFERS AND BOARD SELECT
HEWLETT PACKARD
07908-60002
D-07908-60002-50



"NOT USED ON 7908"
74LS257
U472
U492
R3111 1K
U332 74LS74
U3101 74LS14
U451 74S32
U441 74LS32
U4102 74LS244
E4122
E4112
Z80 CTC
U211
U462 74LS191
U371 74LS245
U391 74S04
U461 74LS00
7.50 MHz Y192
CRYSTAL OSCILLATOR
U191 74S08
U181 74S112
R182 1K
R181 1K
R183 1K
CLKOUT E185
E186 INT CLK
C188 68pf
R195 3.16K
R196 10Ω
R190 1.21K
R191 909Ω
Q193 1853-0405
74S240 U172
SYCLKH TP171
NOTE:
1 ALL SINGLE 74LS245's ARE PART OF THE PACK SHOWN ON THE "CONTROL LOGIC" PAGE 2.
SEE SHT. 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
SENSE LINES, CTC REV REGISTER, AND SYSTEM CLOCK
6-4-80
2/10/81
HEWLETT PACKARD
07908-60002
D-07908-60002-50



SELFTEST SWITCH
GLSTIL E15
GLSTOL E15
MOM. SWITCH 3101-1675 S120
MOM. SWITCH 3101-1695 S140
R138 1K
R139 1K
74LS74
U142
STOH
STIH
STOH E16
STIH E16
MRSTL P2-16
U3101
U391
74LS14
74S04
R362
ERSTL J1-6
GRSTL A7
74LS08
U322
A18, A10, A1 BRSTL
H3, A28 MD7H
H3, A28 MD6H
H3, A28 MD5H
H4, A29 MD4H
H4, A29 MD3H
H4, A29 MD2H
H4, A29 MD1H
H4, A29 MD0H
A10, A20, A27 LWRL
H14 LEDSLL
U381
74LS32
74273
U131
R130
270Ω
DS129
1990-0452
SELFTEST LED LATCH
A20 BSTP-L
H14 SPISTL
H19 CLK L
U461
74LS00
R3111 1K
U4101
74LS10
U471
U481
74LS390
NC
SPEED CHECK
"NOT USED ON 7908"
U491
74LS74
P2-42 SOK H
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
3-12-82
4/21/82
4/21/82
L.C. HARDWARE
HEWLETT PACKARD
07908-60002
D-07908-60002-50
SEE SHEET 1



NOTES:

1. U231, U111, AND U132 ARE SPARES AND ARE SHOWN FOR REFERENCE ONLY

SEE SHT. 1

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

6-16-80
2/13/81
2/17/81

SUPPLEMENTAL MEMORY & RAM

HEWLETT PACKARD

07908-60002

D 07908-60002-50

SHEET 6 OF 6

P/N 07908-60241

TAPE INTERFACE BOARD (TIB) PCA-A6

Series Code F-2336

ER48 D/H:C6

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline). (L460)

LTR	REVISIONS	DATE	INIT	MF
A	AS ISSUED PER PCO 48-6116	03-15-83	sjb/RF	M

A	48-6116	sjb/RF	03-15-83	MODEL 7908	STK. NO. 07908-60241
		/	- -	INTERNAL MAINTENANCE SPECIFICATION, TAPE INT	
		/	- -	BY	DATE MAR 13, 1984
LTR	P.C. NO.	APPROVED	DATE	APPD.	SHEET NO. 1 OF 88
REVISIONS				SUPERSEDES	DWG. NO. A-07908-60241-10

9320-2861 (5/82)

HEWLETT-PACKARD CO.

TABLE OF CONTENTS

A	48-6116	sjb/RF	03-15-83	MODEL 7908	STK. NO. 07908-60241
		/	- -	INTERNAL MAINTENANCE SPECIFICATION, TAPE INT	
		/	- -	BY	DATE MAR 13, 1984
LTR	P.C. NO.	APPROVED	DATE	APPD.	SHEET NO. 2 OF 88
REVISIONS				SUPERSEDES	DWG. NO. A-07908-60241-10

HEWLETT-PACKARD CO.

INDEX OF ILLUSTRATIONS

HEWLETT-PACKARD CO.

1.0 SCOPE

This document describes the Tape Interface Board (TIB) which is used to interface the HCD-75 tape drive module, OEMed by the 3M Company, to the set of Controller boards presently used by the HP7908 and HP7912 disc drives.

2.0 RELATED DOCUMENTS

2.1 Linus Final Proto ERS (Rev. D)--10/24/80

2.2 Diagnostics for the Tape Interface Board--1/27/81

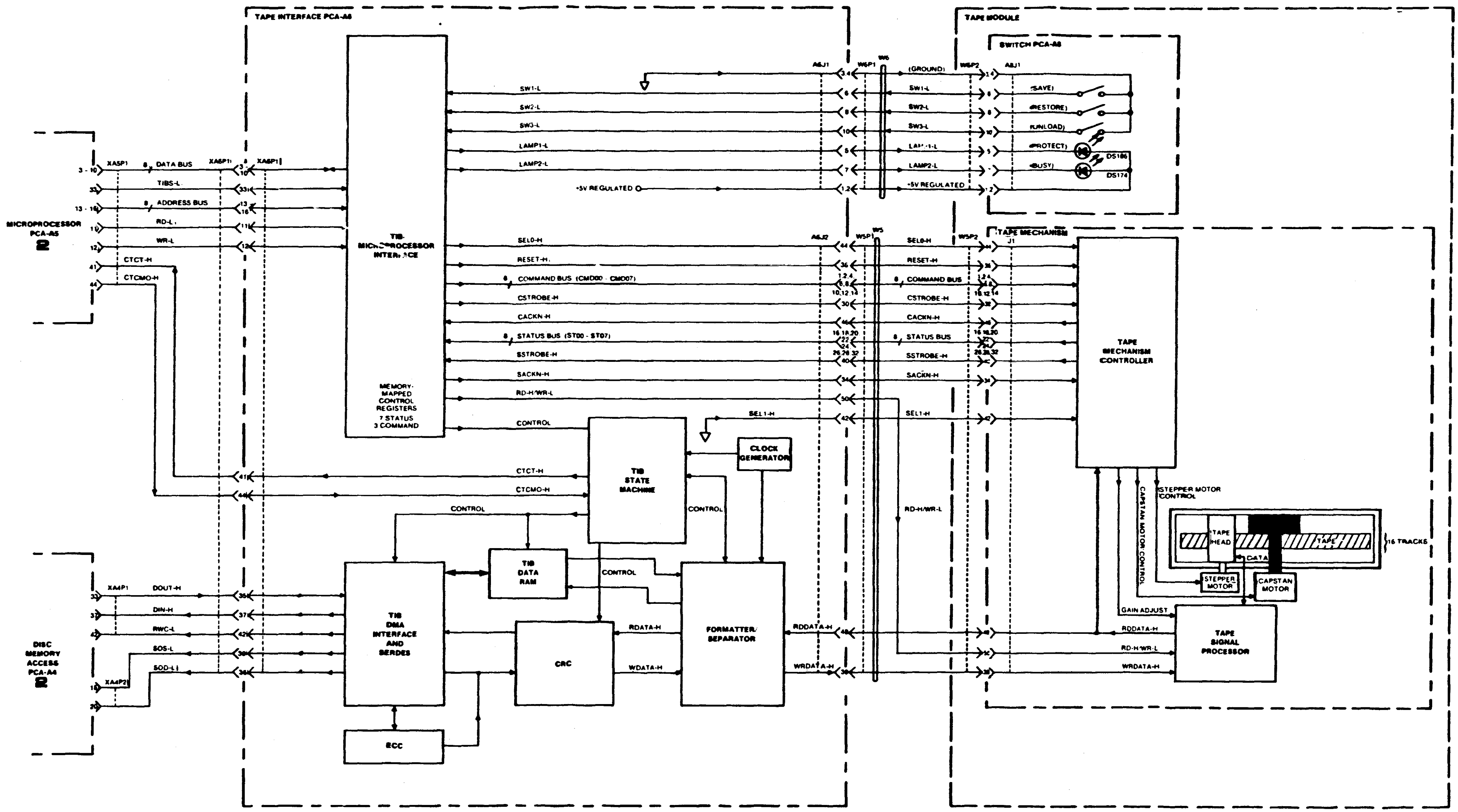
2.3 3M Company Documents

2.3.1 Interface Information, HCD-75 Drive Module--7/29/80

2.3.2 Description, DC600HC High Capacity Data Cartridge, Prerecorded Format--4/9/80

2.3.3 DC600HC Recorded Format, 16 Tracks, 67.1 Megabytes

2.4 Tape Interface Board State Machine Flowchart, 07908-60241-11



4

FIGURE 3.1

TIB FUNCTIONAL BLOCK DIAGRAM

REV. NO. A	DATE 1-28-83	DWG. NO. A-07908-60241-10	SHEET 5 OF 88

HEWLETT PACKARD

3.0 BLOCK DIAGRAMS and General Descriptions

The TIB can be considered a composition of seven blocks. Each block will be described briefly here as to its function and relationship to the others. A comprehensive explanation of the circuitry can be found in Section 4.

3.1 Microprocessor Interface

The TIB is treated as a memory-mapped peripheral to the microprocessor. As such it uses ten bytes of system memory space, seven for status to be read by the processor and three command bytes to control the state machine and tape drive. When TIBS-L is active, RD-L or WR-L pulses will be gated from the processor to the memory location selected by A0-H through A3-H. The processor's data bus (D0-H through D7-H) will then be logically connected to the TIB's internal data bus to accept status from Addresses 0 through 6 for RD-L to latch a command at Addresses 8 through 10 in response to WR-L.

3.2 Clock Generation

A 19.2-MHz hybrid crystal oscillator is at the basis of the TIB's timing circuits. From this master oscillator is derived a 9.6-MHz clock with fifty-percent duty cycle which becomes RWC during DMA transfers. A 4.8-MHz clock that is high 75% of the time free-runs for use as SCLK to the state machine. Further divisions produce a free-running BITC-H that is gated for WCLK when writing to the tape. BYTCK-H is the lowest frequency derived from the crystal time-base and runs at one-eighth of the 600-kHz BITC-H rate or 37,500 Hz. The timing derived from the phase-locked loop during reads from the tape will be discussed separately in the sections on Tape Data Paths.

3.3 State Machine Controller

The power needed by the TIB to manipulate data paths, both to the DMA and the tape, as well as interfacing control paths with the tape drive and microprocessor, is derived from a PROM-based state machine. Having nearly five hundred states this machine tests thirty-two conditions and outputs combinations of twenty-eight control bits, being the equivalent of a heavily vertical micro-coded machine which would use a 44-bit microword.

3.4 HCD-75 Control Path

The control path for the tape drive interfaces primarily to the microprocessor, with only one instance where the state machine intervenes. The commands sent to the drive to control motion of the tape, stepping of the head and other functions (see reference 2.3.1) are stored by the processor into the latch at Address 8. The processor then issues a CSTROBE via Address 10, which register is also used to acknowledge drive fault status with SACKN. Drive status, whether primary (normal) or secondary (in case of a fault), is relayed to the processor through Address 0 and the drive's willingness to accept new commands can be monitored using SSTROBE and CACKN located at TIB Address 1. Also at this address is SW0 which may be used to select between two tape drives connected to the same TIB. The powerful RESET bit which initiates the drive's Autoload sequence a clears fault status is contained in command register 10.

The one instance in which the state machine takes control of the drive is when it overrides the current drive command stored at address 8 and forces a Stop Motion command using its own FCSTR in place of the CSTROBE coming from the processor through register 10. This may be done to terminate a Seek at the target block, to interrupt a Tape Verify at a faulty block for inspection, or when the processor issues a nonsensical command or fails to respond predictably and in a timely fashion when its attention is needed. This jamming of the drive command bus is only initiated when the drive is willing to accept new commands and will not override an already faulty drive condition in which case the drive should bring itself to an orderly halt.

3.5 Direct Memory Access (DMA) Interface

Data is passed between the RAM buffers and external DMA assembly under control of the state machine. The state machine generates SOS-L and SOD-L plus the proper number of dummy bits depending upon the direction of the transfer, then passes the header and user data to or from the RAM followed by space holding dummies for two bytes of CRC and five (Fire Code used by some discs) ECC bytes. The data is either received from the DMA on DOUT-H which becomes FIDAT-H or is output to DIN-H after transformation from FODAT-H. In all cases, without regard to the direction of transfer, the clock RWC-L is produced by the clock generator on the TIB and gated by the state machine using DMAEN-H even though RWC runs at twice the frequency of the state machine clock SCLK.

3.6 Data Management, including Data Buffers and Error Detection and Correction

As data is written from the DMA to the TIB, it is converted from serial to byte-parallel form via a pair of identical universal shift registers operating in the right shift mode. Depending upon the frame (sector) counter the output of one of these registers will be loaded into its corresponding RAM at the end of each byte; the first two frames go into RAM0 and the second two are loaded into RAM1. Each RAM is two kilobytes in size, allowing for the storage of two frames plus the header which had been assigned by the microprocessor for the particular frame with a given target block address on the tape; the 73% of the RAM locations that remain unused results in an overall cost-effective, efficient and reliable design (see Section 4.6 for an explanation of how this can be so).

Based upon mode control lines and prompting from the state machine, the next logical step is to write this data to the tape. This is done by running the address (byte) AB-counter from an initial address smaller than that of the location of the first header byte in RAM and decoding these extra unused addresses to output the all-zero sync field followed by a single one-bit inserted at the appropriate count by SYNC1. The state machine then fetches the header and user data from the proper RAM and routes it through its corresponding universal shift register in a left shift fashion appending two CRC bytes to the end of each frame using CWE-L. The four data frames are written in this manner, two from each of RAM0 and RAM1, then the two ECC frames are generated and added to the block. The headers for the ECC frames, numbered 5 and 6, are produced by using HINST-H to add four arithmetically to the headers from the first two data frames. The data for the ECC frames is generated by retrieving data simultaneously from both RAMs and exclusive-ORing the two alternate frames together bit-by-bit. CRC is then appended to the concocted frames as it is shipped off to be encoded into MFM before being written to the tape.

On the return trip, during a read from the tape, the read circuitry will recover RCLK from the data stream at RDDATB and supply it, along with decoded data, to the buffer circuit block. Loading of the information to the RAMs is accomplished in the same manner as during a DMA transfer except that all transfers between the TIB and tape use a left shift mode while the DMA interfaces via right shifts. As the data is shifted into the SERDES, the CRC Checker monitors it, header included, and at the end of each frame a flag is strobed into the CRC-flag register at address 5, being set if an error was detected or cleared if not. Each of the four user data frames is stored into the same RAM locations that it would have passed through during a write. When the ECC frames are reached, some decisions must be made as to their utility. If, for instance, the first data frame had resulted in an erroneous CRC being calculated, then the first ECC frame, number 5, will be needed in order to exclusive-OR it bit-by-bit with frame 3 to reproduce frame 1. Therefore, as frame 5 is read from the tape and decoded, it will be overlaid in RAM onto the bad data stored for frame 1, unless frame 3 was also known to be bad in which case the errors are uncorrectable and frame 5 will be ignored. Similarly, if frame 3 had been detected as bad, but frame 1 was good, then frame 5 would be written over the bad number 3 to be exclusive-ORed later with frame 1 to perform the recovery. Also, similarly, when frame 6 is read, it will be saved as necessary to correct either of frames 2 or 4, providing the alternate has been detected as good. Of course, if a pair of data frames was both good, that is 1 and 3, or 2 and 4, then there is no need to save the contents of the ECC frames.

Now that the data has been retrieved from the tape and set up as necessary for recovery from errors, the final step in the round trip would be to perform a Read to the DMA. During this operation, the same CRC flags that were generated and stored in register 5 above are again tested by the state machine in order to determine the origin of each frame, and hence the activity necessary to restore usable data. If, for a data frame pair, neither or both of the CRC flags had been set during the reading from the tape, then the data will be taken as is from the RAM and output to the DMA, as the data is either good or uncorrectable. On the other hand, if one and only one CRC flag has been set in a frame pair, then the ECC frame would have been overlaid upon the flagged erroneous frame and to restore the data, this ECC field must be exclusive-ORed bit-by-bit with its mated frame in the pair as it is sent to the DMA interface. This method, of a two-part correction, the first being performed during the read from the tape and the second during the DMA transfer, is used within the two triplets, frames 1, 3 and 5, and frames 2, 4 and 6, to recover from bursts of errors as long as two frames in length on-the-fly, without the necessity of a rewind and retry.

3.7 TIB to Tape Data Path

The basic block diagram of the read and write data paths from the TIB buffers to the HCD-75 drive module is shown in Figure 3.7.1. A brief description of the functional blocks and signals is presented in Sections 3.7.1 through 3.7.4. An exhaustive component level description is deferred until Section 4.4.

3.7.1 Gap Detection

The HCD-75 drive module contains all of the analog circuitry used to drive the read/write head. The interface to the drive module consists strictly of TTL level signals. Data to be recorded, already MFM-encoded, is presented to the drive on the WRDATA line, while data read from the tape (still MFM-encoded) is available from the drive on the RDDATA line.

Gaps (blank areas of the tape) are detected by monitoring whether the RDDATB line (buffered RDDATA) is toggling in a legitimate MFM-encoded fashion. The output of the gap detector is GAPX-L and is shown in Figure 3.7.2a for a blank (though preformatted) tape and in Figure 3.7.2b for a recorded tape.

The preformatting (which is done by the tape manufacturer) consists of writing key marks with a spacing of about 1.75 inches. The key mark consists of a ten-byte forward key followed by a two-byte interkey gap followed by a ten-byte reverse key. The forward key can only be read in the forward direction and the reverse key can only be read in the reverse direction. These preformatted keys serve to segment the tape into blocks which represent the smallest quantity of data which is ever read or rewritten at a time.

Figure 3.7.2 shows only one block. Each block consists of six frames plus the associated key mark. The first four frames each hold 256-bytes of user data and the last two frames each hold 256-bytes of ECC. The preamble and postamble bring the total size of each frame up to 270-bytes. The existence of six frames per block is known only by the TIB and drive module. At the external interface the user sees only 1024-bytes of data per block. With 1024-bytes of user data in each of 4096 blocks on sixteen tracks the total formatted capacity of the DC600HC cartridge is 67.1-megabytes, or 16.7-MB for the shorter DC615HC data cartridge. For more information on the recorded format of the DC600 cartridges consult the paper prepared by the 3M Company referenced in 2.3.3.

3.7.2 Recognition of Pre-recorded Format

In order to determine the current position of the tape we must request a read during the appropriate (forward or reverse) key. The signal which flags the appropriate key is KYEXP-H. This line becomes active during a gap to denote that the next information on the tape is a key number which can be read in the current direction of tape motion. KYEXP is generated from the GAPX-L signal. Figure 3.7.3a shows KYEXP-H assuming that the tape is running forward whereas Figure 3.7.3b shows KYEXP-H assuming reverse motion.

3.7.3 MFM Encoder

Figure 3.7.1 contains a simplified block diagram of the MFM encoder and its external signals. The output of the MFM encoder is a TTL-level waveform WRDATB which is buffered and then sent to the HCD-75 drive module as WRDATA. The MFM encoder's only control line is WEN-H. While WEN-H is held low the WRDATB line is also held low. When WEN-H goes high the MFM encoder begins accepting binary data off of WDATA-H and sends the corresponding MFM code to the drive module via WRDATB. Bits are accepted from WDATA-H on each rising edge of BITC-H as long as WEN-H is high. BITC-H is a free running clock with frequency of 600-kHz, to allow for the fact that the tape travels at 60 inches per second and is recorded at 10,000 bits/inch. Note that WEN-H enables only the MFM encoder. The drive module itself also must be enabled to write using its RNWEN-H line.

3.7.4 MFM Decoder

Figure 3.7.1 also contains a simplified block diagram of the MFM decoder and its external signals. During a read, the HCD-75 drive module presents the still MFM-encoded read data on the RDDATA line. Due to tape speed variation it is necessary to phase-lock a local oscillator to this MFM pattern in order to decode the corresponding binary data. The MFM decoder's principal component therefore is the phase lock loop which generates a local clock that tracks the jittered MFM pattern on RDDATB (buffered RDDATA). The local clock is then used to accomplish the decoding from MFM to binary. The decoded binary bits are output on the RDATA line and sent to the TIB data buffers. These decoded bits are clocked into the TIB buffer by the RCLK signal generated from the PLL oscillator.

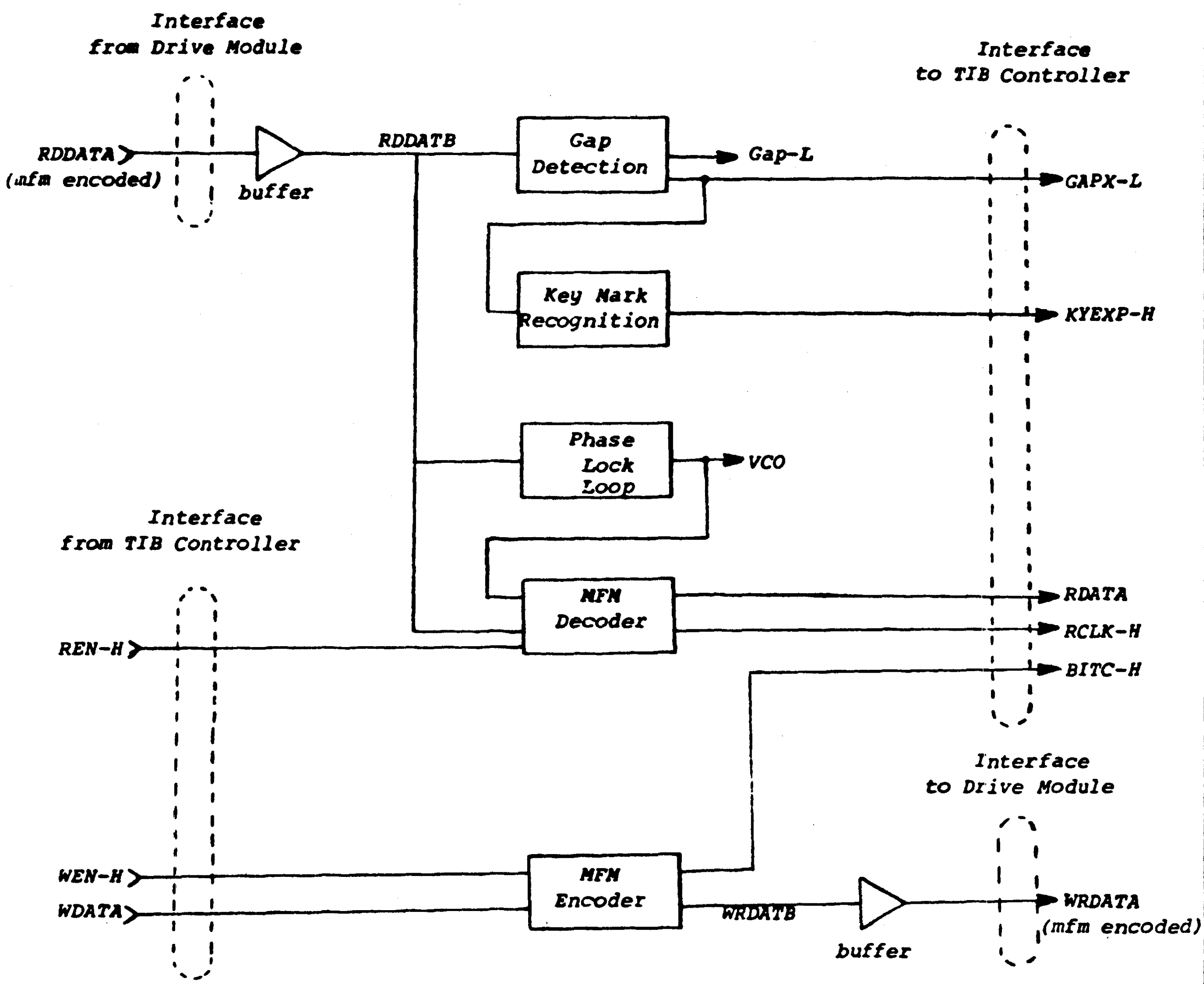


FIGURE 3.7.1

Simplified Block Diagram of
"TIB to Tape" Data Path

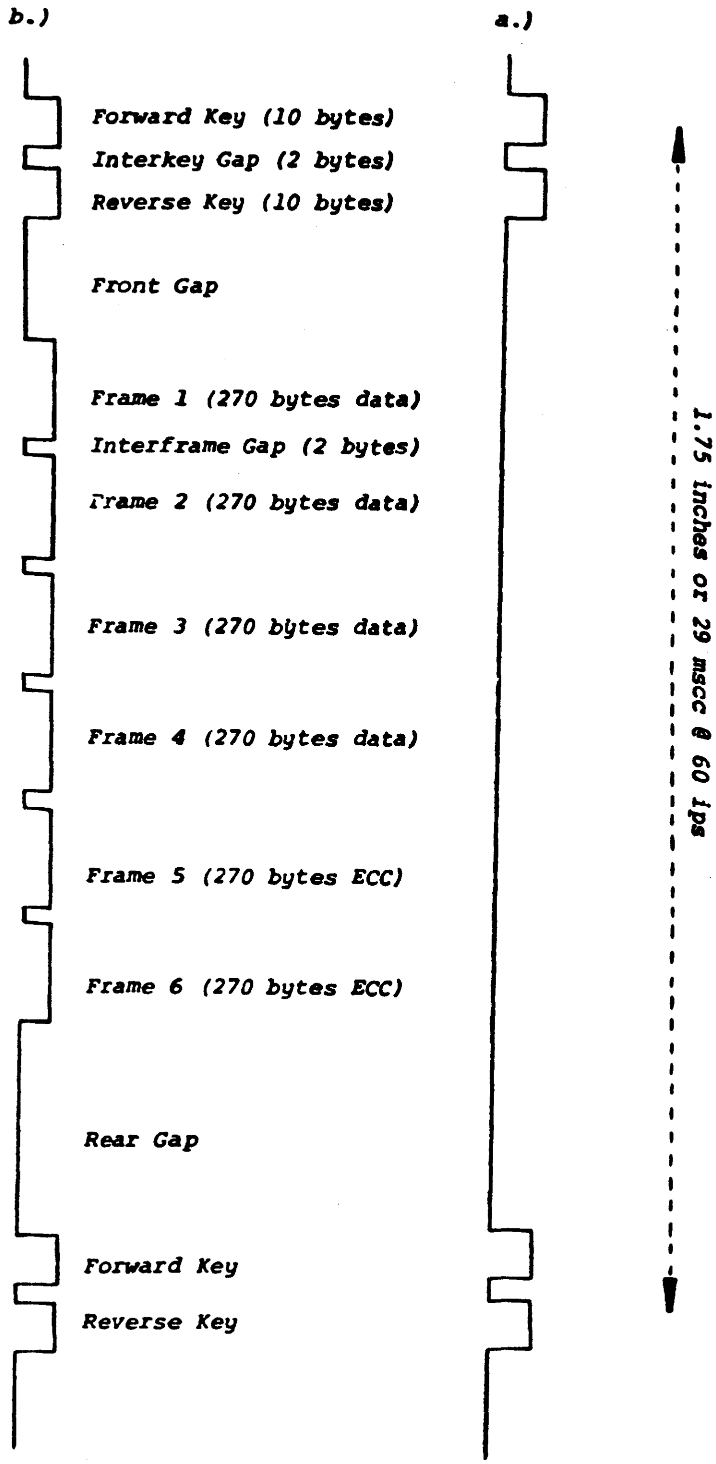


FIGURE 3.7.2

GAPX-L SIGNAL SHOWING TAPE FORMAT FOR
a.) BLANK AND b.) RECORDED TAPES

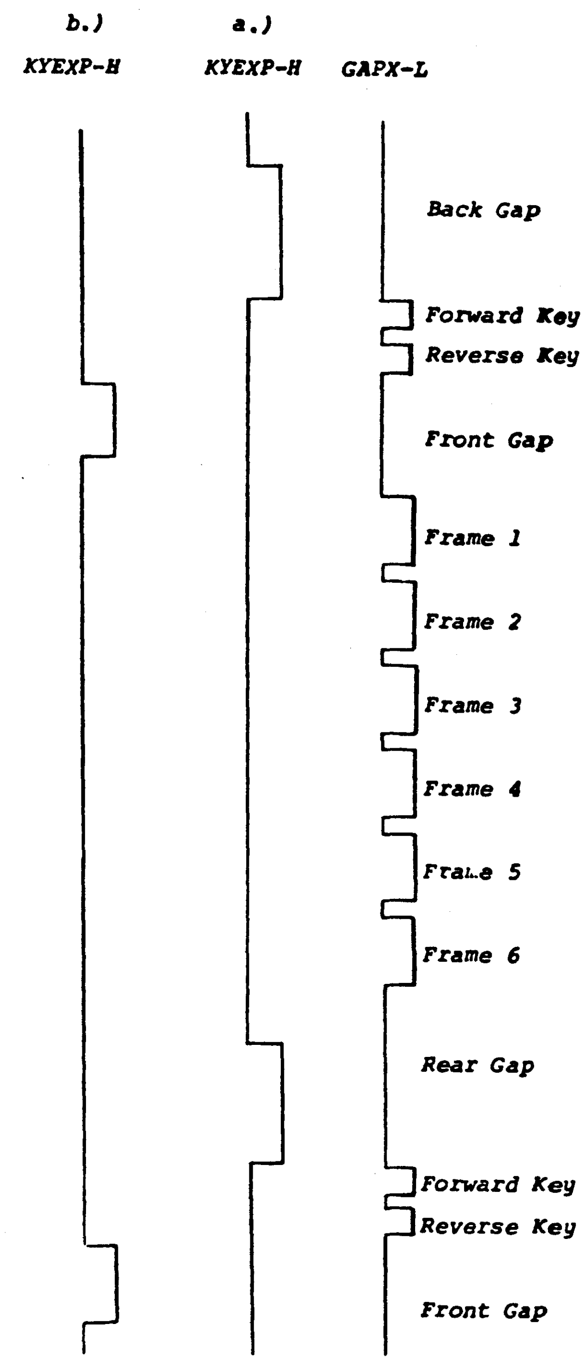


FIGURE 3.7.3

KYEXP-H Signal for a.) forward and b.) reverse Tape Motion. Note: that the frames are numbered for an even number (forward motion) track.

3.8 Control Lines and Modes of Operation

The TIB recognizes three bytes of command from, and offers seven bytes of status to, the microprocessor. The ten control registers used are in a sixteen-byte subspace of the 64-byte register space covered by the TIB Select line, TIBS-L. Table 3.1 shows the allocation of this register space as an offset from the base address of !F3C0; figure 3.8 gives a bit-by-bit description.

Table 3.1
TIB Command/Status Registers

ADDR	RD-L	WR-L	Data Bus
0	0	1	Drive Status ST00-ST07
1	0	1	Tape Interface Status
2	0	1	Key Number, More-Significant-Byte
3	0	1	Key Number, Lesser-Significant-Byte
4	0	1	Task Completion Code
5	0	1	CRC Flags
6	0	1	PC Revision/Rework Number
7	X	X	unused
8	1	0	Drive Command CMD00-CMD07
9	1	0	Tape Interface Control
10	1	0	Drive Interface Control
11-15	X	X	unused
XXXX	0	0	illegal

```
                    Drive Status Register
                          Address 0

   D7      D6      D5      D4      D3      D2      D1      D0
:-------:-------:-------:-------:-------:-------:-------:-------:
:       :       :       :       :       :       :       :       :
:ST07-H :ST06-H :ST05-H :ST04-H :ST03-H :ST02-H :ST01-H :ST00-H :
:       :       :       :       :       :       :       :       :
:-------:-------:-------:-------:-------:-------:-------:-------:


                    Tape Interface Status
                          Address 1

   D7      D6      D5      D4      D3      D2      D1      D0
:-------:-------:-------:-------:-------:-------:-------:-------:
:Int-   : Unit  :Sector :Unload :Restore: Save  :Command:Status :
: errupt: Select: Toggle: Switch: Switch:Switch :Acknow-: Strobe:
: Flag  : Switch: (STOG): (SW3) : (SW2) : (SW1) :  ledge:SSTROBE:
:-------:-------:-------:-------:-------:-------:-------:-------:


                  Block Number, upper byte
                          Address 2

   D7      D6      D5      D4      D3      D2      D1      D0
:-------:-------:-------:-------:-------:-------:-------:-------:
:New Key:  Bad  :       : 4096    2048    1024    512     256
: Flag  :  Key  :   0   : (-----------Key Number--------------)
:(NEWKY):       :       : (msb)
:-------:-------:-------:-------:-------:-------:-------:-------:


                  Block Number, lower byte
                          Address 3

   D7      D6      D5      D4      D3      D2      D1      D0
:-------:-------:-------:-------:-------:-------:-------:-------:
   128     64      32      16      8       4       2       1    :
(-----------------------Key Number---------------------------)  :
                                                        (lsb)   :
:-------:-------:-------:-------:-------:-------:-------:-------:
```

Figure 3.8-1 Tape Interface Status Register Map, lower half

HEWLETT-PACKARD CO.

Task Completion Code Register
Address 4

```
   D7       D6       D5       D4       D3       D2       D1       D0
:--------:--------:--------:--------:--------:--------:--------:--------:
:Suc-    :Blank   : Zero   :Loss of:Verify  :Drive   :Self-   :        :
:cessful: Data    : Count  : Hand-  : Error  : Fault  : Test   :unused  :
:Compl'n: Frames:          :  Shake:          :        :Results:        :
:(SUCCS):(BLANK):(ZCNT)  :(LOHS)  :(VERR)  :(ST07)  :(STEST):          :
:--------:--------:--------:--------:--------:--------:--------:--------:
```

CRC Flag Register
Address 5

```
   D7       D6       D5       D4       D3       D2       D1       D0
:--------:--------:--------:--------:--------:--------:--------:--------:
:CRC of :Good    :CRC of :CRC of :CRC of :CRC of :CRC of :CRC of  :
:  Key   :Key Not:  ECC   :  ECC   : Data   : Data   : Data   : Data   :
:        : Found :Frame 2:Frame 1:Frame 4:Frame 3:Frame 2:Frame 1:
:(CRCK) :(CRCNF):(CRC5) :(CRC4) :(CRC3) :(CRC2) :(CRC1) :(CRC0)  :
:--------:--------:--------:--------:--------:--------:--------:--------:
```

Tape Interface Revision Register
Address 6

```
   D7       D6       D5       D4       D3       D2       D1       D0
:--------:--------:--------:--------:--------:--------:--------:--------:
:                                   : <-------------> :        :        :
: <-----Artwork Revisions-----> :  Rework           :unused  :(GAPX   :
:                            (lsb):  Revisions        :        :    -L):
:--------:--------:--------:--------:--------:--------:--------:--------:
```

Address 7

```
   D7       D6       D5       D4       D3       D2       D1       D0
:--------:--------:--------:--------:--------:--------:--------:--------:
:                                                                       :
: <--------------------------unused--------------------------->  :
:                                                                       :
:--------:--------:--------:--------:--------:--------:--------:--------:
```

Figure 3.8-2 Tape Interface Status Register Map, upper half

A	48-6116	sjb/RF	03-15-83	MODEL 7908	STK. NO. 07908-60241
		/	- -	INTERNAL MAINTENANCE SPECIFICATION, TAPE INT	
		/	- -	BY	DATE MAR 13, 1984
LTR	P.C. NO.	APPROVED	DATE	APPD.	SHEET NO. 18 OF 88
REVISIONS				SUPERSEDES	DWG. NO. A-07908-60241-10

Drive Command Register
Address 8

```
     D7       D6       D5       D4       D3       D2       D1       D0
:--------:--------:--------:--------:--------:--------:--------:--------:
:        :        :        :        :        :        :        :        :
:CMD07-H:CMD06-H:CMD05-H:CMD04-H:CMD03-H:CMD02-H:CMD01-H:CMD00-H:
:        :        :        :        :        :        :        :        :
:--------:--------:--------:--------:--------:--------:--------:--------:
```

Tape Interface Mode Register
Address 9

```
     D7       D6       D5       D4       D3       D2       D1       D0
:--------:--------:--------:--------:--------:--------:--------:--------:
:RUN-H/ :Self-  :  DMA   :Block   :Drive   :       Mode Select         :
:Restart:  Test :Connect: Enable: Select: <-------------------->  :
:     -L: Select:        :        :        :        (see note)         :
:        :(STEST): (DMAC):(BLKEN): (SEL0):  M2       M1       M0   :
:--------:--------:--------:--------:--------:--------:--------:--------:
```

Note: See Table 3.2 for function of Mode Select bits
with respect to STEST

Drive Interface/Front Panel Register
Address 10

```
     D7       D6       D5       D4       D3       D2       D1       D0
:--------:--------:--------:--------:--------:--------:--------:--------:
:        :        :        : Busy   :Protect:        :Status  :Command:
:unused :unused :unused :  Lamp  : Lamp   : RESET  :Acknow.: Strobe:
:        :        :        :(LAMP2):(LAMP1):        :(SACKN):CSTROBE:
:--------:--------:--------:--------:--------:--------:--------:--------:
```

Figure 3.8-3 Tape Interface Command Register Map

Table 3.2
TIB Mode Selection Bits

M2	M1	M0	Operation when: STEST = 0	STEST = 1
0	0	0	not supported	Loop on Write of DMA to TIB
0	0	1	Write TIB to Tape	Write Bad CRC on Frames 2 & 5
0	1	0	Read Tape to TIB	not supported
0	1	1	Read TIB to DMA	Loop on Read of TIB to DMA
1	0	0	Verify N Blocks	not supported
1	0	1	Seek N Blocks	not supported
1	1	0	illegal	Buffer Fill of TIB RAM for DMA
1	1	1	illegal	illegal

Note: M2, M1, M0 and STEST are located in the register at address 9. See Figure 3.8-3.

3.8.1 Status Registers

Address 0, Drive Status: Data Bus will pass Status ST00-ST07 directly from drive in real-time buffered by a 74LS244, an octal three-state driver.

Address 1, Tape Interface Status:

D0 = Status STROBE directly from Drive

D1 = Command ACKNowlege directly from Drive

D2 = Save, Disc to Tape, front panel switch

D3 = Restore, Tape to Disc, front panel switch

D4 = Unload, front panel switch

D5 = Sector Toggle bit assists microprocessor with control of DMA by signalling transfer of each new sector to or from the DMA.

D6 = Unit Select switch, signals processor to exchange unit numbers between tape and system disc. This switch is not presently loaded.

D7 = Interrupt FLAG is set by TIB upon completion of a task, whether successfully or by fault.

Address 2, Block Number, upper byte:

D0-D4 = Five most-significant bits of last Key Number read

D5 = unused, should be 0

D6 = BAD KeY, a copy of bit D6 from the CRC Flag register at address 5 below.

D7 = NEW KeY is set when the Key Number is loaded into its register from the tape and cleared automatically when the least significant byte of that register (address = 3) is read. Failure of the microprocessor to read the Key Number register (both bytes) prior to recognition of a newer key will result in a Loss Of HandShake depending upon the current mode of operation.

Address 3, Block Number, lower byte: Least significant byte of Key Number register. Trailing edge of a read at this address will automatically clear the NEW KeY flag, D7 of address 2.

Address 4, Task Completion Code:

D0 = unused

D1 = Self-Test Results, will be set if Completion Code being reported is from a self-test mode.

D2 = Drive Fault is a copy of ST07 directly from Drive

D3 = Verify ERRor is set at the end of a block during Verify mode if a CRC failure occurred within that block and the BLocK was ENabled; catches key errors as well as errors in data and ECC frames.

D4 = Loss Of HandShake will be set if NEW KeY flag is still set when another Key is encountered on the tape, the idea being that the microprocessor must be involved in another task and not paying proper attention to the Tape Interface.

D5 = Zero CouNT is asserted in Seek or VeriFY modes when the block counter decrements to zero.

D6 = BLANK bit is set to signify that the previous block was read but contained no user data. This tells the microprocessor that there is nothing to be gained by reading the TIB buffers as the data they contain are left over from the previous transfer.

D7 = SUCCeSsful Completion bit should be self-explanatory.

Address 5, CRC Flags:

D0-D3, if set, imply that a CRC error was detected in the corresponding data frame, 1 to 4.

D4-D5, if set, mean that a CRC error was detected in either ECC frame 1 or 2, respectively.

D6 = Good Key Not Found, means that the current block number could not be read with a valid CRC, whether from the Key Mark itself or by an attempt to extract it from one of the first four data frames. This bit is copied into bit D6 of address 2.

D7 = Bad CRC on Key Mark

Address 6, Printed Circuit Revision Number: The buffer necessary to access this register is not presently being loaded.

D0 = GAPX-L; available for test purposes or to allow the microprocessor to monitor tape format; high when the tape head is over a written portion of the tape, low when over an erased area.

D1 = unused

D2-D3 = P.C. Rework Number hardwired by Production

D4-D7 = Artwork Revision Number, coded by P.C. Layout

3.8.2 Command Registers

Address 8, Drive Command: Data Bus will be stored and buffered by a 74LS273 octal flip-flop and passed directly to the HCD-75 Tape Drive.

Address 9, Tape Interface Control:

D0-D2 = Mode Select Bits, see Section 3.8.3.

D3 = Drive Select, normally low to enable the interface to the HCD-75 Tape Drive, this line may be brought high to select the second of two drives in a two drive system. No indication is given that this feature will ever be used.

D4 = BLocK ENable, must be set to enable writing of data onto the tape, implying that the microprocessor is certain that the current block is the appropriate target for the data currently buffered. In read modes the data will be read but ignored, not transferred to the DMA buffers, if this bit is not set. In the VeriFY mode this control bit may be used to inhibit verification of the first few blocks after the mode is selected but prior to reaching the target block. This feature behaves as a fine seek, exactly as in the read mode.

D5 = DMA Connect bit connects the drivers and receivers on the TIB to the DMA channel. By disconnecting, clearing, this bit, the microprocessor may then connect another device to the DMA thereby making greater use of the channel.

D6 = Self-Test Mode Select, which causes the mode chosen by bits D0-D2 to alter its operction for use as a test procedure.

D7 = RUN if high, ReSTaRT when low. Bringing this bit low forces the state machine to state 0, suspending its operation. This bit should only be raised after the operation mode bits have stabilized, in order to avoid potential illegal conditions. Asserting this bit will allow normal operation of the state machine to resume.

Address 10, Drive Interface Control:

D0 = Command STRobe directly to the tape dr ve. This line is a direct connection to allow the micro processor to strobe commands to the drive for operations not implemented in the state machine. It is a latch that must be set (by a WRite-L to this address), held for at least one microsecond, then rewritten to be cleared.

D1 = Status ACKNowledge directly to the drive is to be treated as CSTRobe above. This must be used with two-byte commands and to clear secondary status, as described in the ive Interface document referred to in 2.3.1.

D2 = Drive Reset is similar in operation to the two signals above, but with a minimum pulse-width of ten microseconds.

D3 = Write Protect lamp on the front panel can be turned on and off by the processor via this latched bit.

D4 = Busy lamp on the front panel is controlled by means of this latched bit.

D5-D7 = unused

3.8.3 Modes of Operation

These modes are selected in accord with the value encoded in bits 0-2 of the command latched at register address 9. The value of the mode control should only be changed when ReSTaRT is already active (low), or is made active at the same time, that is, RUN (bit 7, same address) is to be low. RUN may be reasserted on the next instruction cycle, after the mode decoding logic has settled.

3.8.3.1 Mode 0, Write DMA to TIB

This mode is presently used for self-test only, although there are no necessary restrictions to that effect. It will be assumed that the DMA has been set up appropriately and connected to the TIB via the DMA Connect bit (address 9, D5). The TIB will issue a Start-of-Sector signal to the DMA and make a Sector TOGgle bit available to the microprocessor (address 1, D5), wait out the appropriate number of clock periods to satisfy DMA and ECC requirements, issue Start-of-Data and then transfer a sector of data based upon a bit clock rate of 9.6-MHz. This procedure will be repeated for a total of four sectors, accepting 1k-byte of user or disc data with headers in accord with the tape format and allowing space for, but ignoring the contents of, CRC and ECC bytes in keeping with the DMA/ECC formats. This transfer will end after an extra Sector TOGgle has signalled the end of transfer to the microprocessor. The state machine will then loop with a SUCCeSsful completion code waiting for acknowledgment of task completion in response to its Interrupt FLaG. This mode will ordinarily be used only for test purposes, as mode 1 incorporates this procedure followed by an automatic transfer to tape.

3.8.3.2 Mode 1, Write DMA to Tape

As mentioned above, this mode is a combination of two more specific functions. It consists of a Write from TIB to Tape with an embedded Write from DMA to TIB (mode 0) automatically included.

After the tape head has been located on the desired track and the drive has achieved the requested operating speed in the direction appropriate to that track, this mode becomes meaningful. First, the state machine reads a key and sets the NEW KeY flag, provided that the previous key had been read in order to avoid a Loss Of HandShake error. Then a timer, contained in a CTC chip on the processor board, will be triggered to time out a long enough delay so that the erase head will safely clear the key marks which are a part of the preformatted tape. While the timer is running, the state machine will watch for the processor to set BLocK ENable, signalling that the current block is the intended target and that the DMA has been connected to the TIB in readiness for a data transfer. When the DMA transfer is complete, the state machine will check the CTC timer to make certain that it has not timed out as this would result in an excessively long gap on the tape. If the DMA completed too late and the timer has run out, a Loss Of HandShake flag will be set; but if the DMA completed in time, the timer will be allowed to timeout and then be retriggered when the erase current is established to begin a write to the tape.

At the end of this second timeout, writing of data will begin. The four sectors of data acquired from the DMA will be placed in the first four frames along with the appropriate header information, which had been generated by the microprocessor and passed through the DMA, and the CRC bytes which will be produced in the TIB. Two additional frames will be generated in the TIB by creating headers from those used for the first two frames, combining data via the exclusive-OR function from alternate data frames, and appending proper CRCs. The state machine then requests a third timeout at the end of which the drive will have its write current switched off, having erased any stray transitions or overwritten data. The BLocK ENable signal is nulled by the TIB upon recognition of each new block (key mark) and must be set again by the processor after verifying the key number. The microprocessor will then be sent an Interrupt FLaG along with a SUCCeSsful completion code, asking it to issue another command.

3.8.3.3 Mode 2, Read from Tape to TIB

Like the Write mode above, this command is sent to the TIB by the microprocessor while it holds ReSTaRT active and tells the drive to go to the desired speed and direction. When RUN is asserted, the TIB will wait until the requested speed has been achieved and begin to look for key numbers. When a key number has been recognized, it will be stored and the NEW KeY flag set. If the previous key had not been read prior to this, the TIB will flag a Loss Of HandShake error and force the tape drive to a stop. In the case of an unrecognizable key number due to a CRC error on the key mark, the state machine will attempt to recover the key number from the header of the four data frames, which are protected by ECC; if all three frames are bad then the data is uncorrectable so that the key number is unnecessary. In a multi-block read it is necessary only to extract the key number from the preformatted key mark of the first block for orientation. On successive blocks the state machine will time past any missing key marks and recover block numbers from the data frames. This procedure is valid only for read operations and does not apply to writing or verifying of tapes.

Data for the current block will be read and buffered in RAM on the TIB. The first four frames of data are read as written, headers being stored and CRC's being checked. A bit to signify a zero (good) or non-zero (bad) CRC will be placed in the CRC register, Status address 5, for each frame. If any of the first four data frames is in error, the ECC frame that corresponds to it will be stored in place of the bad data in the RAM as the first of two phases of the error correctio process. That is, if frame 1 or 3 results in a non-zero CRC check, then frame 5 will be stored in its position, and a similar situation for data frames 2 and 4 and ECC frame 6. If, however, both of a data frame pair are found to be in error, then the error is known to be uncorrectable and the overlay will not take place, as is also the case when both data frames are thought to be good. [The ECC frames in these instances will be doubly buffered and carefully stored away in one of a pair of bit buckets to be recalled as necessary for correction of future tapes.]

After data has been read and buffered in RAM, BLocK ENable will be checked to see if the processor has decided that this block is of value. If the enable is not set, then the data will be ignored and a search will begin for the next key mark; this constitutes provision for a fine seek under close supervision by the microprocessor. On the other hand, if the block was enabled, but contained no previously written data, it will be assumed that a mistake has been made with regard to the host's directory, a BLANK completion code will be issued and the drive brought to a stop. With a previously written tape, if the block was enabled, the TIB would signal a SUCCeSsful completion and issue an Interrupt FLaG, then await further instructions, presumably a DMA transfer. As in the Write mode above, the BLocK ENable is cleared after each new key number is read and must again be set by the processor for each block.

3.8.3.4 Mode 3, Read from TIB into DMA

As was the case for Mode 0, the TIB will assume that the DMA has been set up to expect four sectors of data and connected to the TIB. This transfer will normally be executed during the final gap, between the last frame of a block and the following key mark, but this timing is not necessary. Start-Of-Sector and Sector TOGgle signals are issued identical to those used in the Write mode. Data transfer begins, following a Start-Of-Data pulse and appropriate dummy bits, header first at a rate of 9.6-Mbps.

If a correctable combination of CRC flags are set, then the second phase of the automatic error correction process will take place. To wit, if frame 1 was thought to be in error and frame 3 was good, then upon reading frame 5 from the tape it would have overlayed frame 1. During the DMA transfer the apparent contents of frame 1, which is actually ECC information from frame 5, will be exclusive-ORed with frame 3 to recreate a good data frame 1. Other data frames may be recreated accordingly as the data is passed to the DMA RAM.

It should be noted that this mode in conjunction with Mode 0 can be used to implement a loopback of data through RAM on the TIB to self-test a significant portion of the operation of the TIB. During a DMA Write (Mode 0), the CRC flags are cleared so that when this feature is used there will be no interference from CRC flags remaining from a recent reading of the tape. Such CRC bits would invoke tha automatic error correction, generating perhaps predictable but definitely unexpected results.

3.8.3.5 Mode 4, Verify N Blocks

This mode is similar to a Read from Tape to TIB, mode 2, above. Before releasing the ReSTaRT-L line to begin the operation, the microprocessor must set the block counter in the CTC chip to the number of blocks to be verified. Since the state machine on the TIB is not capable of selecting head positions and tape speeds, this block counter is limited to 4096, the number of blocks which can be contained on a single track. This block count is stored in part in one of the eight bit channels of the CTC chip with the necessary remaining four bits contained in another discrete counter register, all on the MPU board.

When the TIB is released to RUN, it begins by looking for key numbers. When one is found, it is reported to the microprocessor as always. The TIB reads the data and checks CRCs as normal until the entire block has been read. The BLocK ENable line is then checked. If the block was not enabled, the results are ignored and a new key number is sought, as for a slow seek. The microprocessor must monitor this slow seek by reading key numbers in order to avoid Loss Of HandShake error until the BLocK ENable is set, after which the TIB is on its own and the key numbers need not be read by the processor, though they will be available if desired.

If the block was enabled, the TIB will continue to read and verify the data stored on the tape using CRCs until an error is found, whether it be in a data frame or an ECC frame or even in the key mark. Any of these errors will cause the tape to be stopped and an Interrupt FLaG to be raised along with a completion code indicating a Verify ERRor. Blank data blocks are ignored so that key marks may be verified on new tapes. Each block that passes this verification causes the block counter to be decremented. If the tape is stopped due to an error, the operation may be resumed without adjusting the block counter. When the counter decrements to zero, the tape will be stopped with an indication of Zero CouNT. This verification procedure is intended to be capable of use in an off-line manner where the processor needs only to occassionally test for an Interrupt FLaG, otherwise the TIB will be self-controlled.

3.8.3.6 Mode 5, Seek N Blocks

The processor sets up the CTC block counter as mentioned under Verify, mode 4 above, and selects the mode while the TIB is idle due to ReSTaRT. After its release to RUN, the TIB waits for the drive to reach operating speed, whether it be 60- or 90-ips, the faster being preferred for Seeks. The TIB then decrements the block counter each time it encounters a key mark until the count is exhausted, at which time it stops the drive and signals a Zero CouNT with an Interrupt FLaG.

This process will count only the blocks seen while at the requested speed; the microprocessor will have to make allowance for the effects of varying tape loads on the time to accelerate and decelerate. This is a coarse seek only and the processor will need to verify the location of the tape by reading the key number as required by the fine seek portion of any other tape operation, though it should be repeatable to within one block of the target.

3.8.3.7 Mode 6, DMA Test

This mode causes the same behavior as mode 3, Read TIB to DMA, with a single exception. Prior to transmitting data to the DMA, the state machine generates a known data pattern by manipulating the CLR0/1 control lines to the SERDES to produce zeros and using the output enable lines in conjunction with the pullup resistors to produce ones while clocking the data into the RAM using a combination of WCLK and RWC. This procedure preloads the RAM on the TIB with a known pattern, including header, user data and CRC space. This pattern is a checkerboard alternating between four bytes of all ones and four bytes of all zeroes. This mode will usually be associated with a DMA loopback, utilizing both directions of DMA transfers, modes 0 and 3, for use in isolating the mode which may be causing difficulties in case of a failure. For more detailed instructions as to the use of this mode, refer to the document of section 2.2. Note that selection of this mode also requires assertion of the Self-Test Mode Select bit D6 of command register 9.

3.8.3.8 Write to Tape, Self-Test

This diagnostic mode is selected by asserting the Self-Test Select bit, D6 of Command register 9, at the same time as Write to Tape, mode 1, is chosen. From the processor and DMA viewpoint, the operation proceeds as normal, but upon readback it will be noted that the CRC fields were written improperly so as to cause errors to be detected on the second and fifth frames. This causes the CRC Flags at status register 5 to show !12. A subsequent DMA read should result in an invocation of the automatic error correction procedure so as to restore the data of frame 2 to its initial contents; the only indication that this has taken place will be that the header will be mostly zeroed-out by the exclusive-OR processing. Since the data frames corresponding to the presumably erroneous fifth frame (first ECC frame) are not flagged as bad, error correction will not be invoked in this case and only the CRC flags will be affected. More on this can be found in the discussion of diagnostics at reference 2.2.

4.0 THEORY OF OPERATION

4.1 Microprocessor Interface

The Tape Interface Board interfaces in turn to the microprocessor for reception of commands and return of status according to the control words mentioned in Section 3.8 above. These control words are passed through a three-state bi-directional buffer, U422 a 74LS245, in order to reduce the loading seen by the drivers on the MPU PCA. This buffer is enabled by TIBS-L, which is decoded on the MPU PCA, in order to avoid interference with other devices on the data bus. The direction of the data passing through U422 is controlled by RD-L, which remains in its inactive high state during Writes to the TIB. All data bus lines are pulled up via R418 on the TIB side of the buffer so as to guarantee a high level, for test purposes, when the bus is turned off. Status words read from the TIB by the processor are addressed via the 74LS138 decoder U432 enabled by TIBS-L and RD-H; whereas Commands are sent to their target register as selected by another decoder U442 enabled by TIBS-L and WR-L.

4.1.1 Tape Interface Board Status

Status from the TIB is stored in or buffered through seven registers. ST00 to ST07 from the HCD-75 is passed through the three-state buffer U131 when enabled by RDST-L from the address decoder. Similarly, Status of the Interface, including front panel switches and drive control, as well as the Interrupt Flag from the TIB, is handled by U171. The CRC Flags stored in U221 are output by buffer U112 when requested by RCRCF-L, as the contents of the Revision/Rework register U421 are output under control of REVNO-L. The Completion Code register U111 is an octal flip-flop which is latched by the rising edge of the Interrupt Flag, which is sampled by the microprocessor via U171 as mentioned above with RIF-L, and connected to the data bus by a low level on RCCOD-L.

As the Key Number is read from the tape by the TIB it is stored in the register pair U431 and U441. These Universal Shift Registers are used in the left-shift mode with serial input from RDATA-H since the data is stored on the tape in a least-significant bit first manner. They are loaded by the NEWKEN command from the state machine and their three-state outputs are activated by RKNM-L and RKNL-L to place their contents onto the data bus. RKNM-L has the additional function of enabling two quarters of the quad three-state buffer U451 to place copies of BADKEY and NEWKeY onto the data bus in place of the upper two bits of the block address which would otherwise be unused due to the fact that the maximum block number accomodates 4096 blocks of user data and a few overhead blocks, thereby requiring barely thirteen bits. The NEWKeY flag is set into U322 by SNUKY-L from the state machine, read as just mentioned using RKNM-L, and cleared automatically on the trailing edge of a read of the lower byte of the Key Number using RKML-L.

4.1.2 Tape Interface Board Commands

There are three command registers addressed with TIBS-L and a hexadecimal address of 8, 9, or !A, as decoded by U442, a one of eight decoder. Commands, as defined by the 3M Company in the reference of section 2.3.1, to be sent to the HCD-75 tape drive are loaded into octal latch U161 by the decoding of WDMOD-L corresponding to TIB address 8. The microprocessor may then generate a CSTROBE and send it to the drive by setting the proper bit (D0) into the Write Interface latch U122, addressed by !A, decoded as WIF-L. Also contained in the !A register are the processor's copies of SACKN and RESET, as well as control bits for the two front panel lamps BUSY and Write Protect. In some instances the TIB's own state machine may deem it necessary to stop the motion of the tape drive; this is done by using JAM-L to connect a hard-wired !3D, the Stop Motion command, to the drive module via U141 in place of the normal output register U161, by switching the three-state output enables with JAM.

Register 9 is contained in U312, an octal latch, and half of U322, a D-type flip-flop. The uppermost bit of the octal latch contains the Restart bit which is used to hold the state machine at state 0, when the bit is low, or to allow the state machine to run, when high. The DMAC and DSEL0 bits are used, respectively, to connect the TIB to the DMA and to select one of two tape drives tied to the same TIB. (This latter feature is not and probably will not be used.) BLKEN is held by the flip-flop being set by the microprocessor and cleared (U332) by the reading of a New Key except when the Verify mode has been selected.

The remaining four bits of the WFMOD latch U312, namely M0-M2 and STEST, determine the operation to be carried out by the state machine when it is allowed to run by raising Restart-L. These modes will be described in detail later in Section 4.8.

4.2 Clock Generation

The heart of the clocking circuits is a 19.2-MHz hybrid crystal oscillator Y2131 (schematic zone C4) containing a buffered, self-starting circuit. Schottky NAND gates from U2132 provide further buffering and the pull-up resistors on their other inputs provide means of controlling the master clock during testing. This 19.2-MHz signal is used directly by U3131, a 74LS164 eight-bit shift register acting as a digital differentiator in the Tape Read circuitry, and by the half of U292, a 74S74 D-type flip-flop, that generates the MFM-encoded WRDATB.

The buffered master clock is also fed to U2102, another 74S74, each half of which produces a fifty-percent divided-by-two version of the input with the outputs of the two halves in quadrature. A NAND gate U291 serves to OR together all of the negative portions of the two half-rate clocks yielding SCLK-H which is a quarter-rate 4.8-MHz clock with seventy-five percent duty cycle. SCLK-H is inverted by U1102 (A10) to provide the alternate phase of the two-phase clock needed by the state machine. The pull-up resistors on the NAND gates are again used for test purposes. U3121, an exclusive-OR gate, picks off the two quarters of the sequence when the outputs of U2102 are at opposite logic levels. This produces a fifty-percent 9.6-MHz RWCB-H clock for use in DMA operations. Generation of the RWC in this manner guarantees the correct phasing of it with respect to the state clock SCLK, so that even though the DMA operations occur at twice the state rate, the state machine can manage them without confusion. Two remaining quarters of U1102 (A8) are used as inverting buffers to provide the alternate phase of RWC with propagation delays roughly matched to those in the SCLK path and to allow control of the individual phases while testing the PCA.

The final use of the master oscillator is to feed the four-bit counter U2112. This 74S163 is used to provide timing for write data precompensation as well as acting as the lower half of an eight-bit divider along with U2122. U3111 and U392 act as decoder and buffer, respectively, to produce BIT Clock BITC-H, a 600-kHz signal with a one-eighth duty cycle. WCLK is also picked off of this divider as a 600-kHz clock but with fifty-percent duty cycle. The last tap on this divider chain results in BYTCK which is at the byte rate, one-eight of the bit rate.

4.3 State Machine Controller, General

The control intelligence for the TIB is derived from a PROM-based state machine. The PROMS U142 and U241 are addressed by a nine-bit counter comprised of 74LS163's U212, U222 and U232. This counter is cleared to select state number zero in response to GTO-L as a result of Restart, Drive Fault or Master Reset upon power-up. When GTO is released the addresses will begin to sequence on the rising edge of SCLK-H. GTO is synchronized via U1111 (zone F20) to allow for the fact that the nine-bit PROM address counter is composed of three different IC packages which may have varying set-up time requirements.

The capacity of each PROM is 512 eight-bit bytes. They are connected in parallel to produce 512 sixteen-bit words of output. These outputs are defined in Table 4.3. The two most-significant bits of the output words are used to select between one of two output register pairs or to choose to branch on a selected condition at the time of the rising edge of the opposite phase of the state clock, namely SCLK-L. The output registers are built from two pairs of 74LS377 octal latches with synchronized enable lines. When the most significant PROM output bit is low at the appropriate edge of SCLK, the word presented by the PROM will be latched into Output Register pair number One, U152 and U261. Likewise, the next significant PROM bit being low at clock time will cause the addressed contents of the PROM to be loaded into OREG0, U162 and U251. Since the upper two bits of the output word are used to select which of the two output registers is to be loaded, it should be noted that each register contains only fourteen usable control bits, for a total of twenty-eight control lines to be distributed around the TIB. Under special circumstances, and only with the utmost of caution, both output registers may be loaded simultaneously (obviously both with the same contents) simply by coding the PROMs to have both enable bits low; this feature is used to inhibit activity while the state machine is held at state zero.

In the instance of neither output register being selected, that is, the upper two bits of the PROM word being both high, a jump condition will be tested. The particular qualifier to be examined will be selected by the decoding of the next five bits of the PROM word. A first layer of decoding is done by the one-of-eight selector U172, a 74S138. Decoder outputs 0 to 3 are unused. The two output register control bits act to enable the decoding of the four outputs 4 to 7, each of which in turn is used to enable one of the four eight-bit qualifier selectors, U311, U321, U331 or U341. The enabled 74S251 then selects one of its eight inputs, based upon the next three bits of the PROM word, and passes this condition bit to its output where it is wire-ORed to become SADAT, the feedback line used for testing by means of Signature Analysis. The rising edge of SCLK-L captures this result in the D-type flip-flop U371 with pin 9 FALSE-L becoming the signal that indicates a Jump If Condition Not Met. When a tested condition fails, FALSE-L will cause the nine-bit PROM address counter to synchronously load the next address from the lower nine bits of the current PROM word. If the condition which is tested proves to be true, FALSE being high, then no branch occurs and the address counter increments to select the next higher PROM word.

You may recall from Section 4.2 on Clock Generation that SCLK has a seventy-five percent duty cycle. It is the rising edge of SCLK that begins selection of a new PROM address. The selected output must then be ready to be latched into the output registers on the opposite clock edge, on the one hand, the easier case, or the PROM outputs must be decoded to select one of thirty-two qualifiers, which takes more time. At the falling edge of SCLK, the output registers are latched for new command words or the test condition result is latched and then set-up to load the next PROM address into the counter. Both of these paths are very quick compared to the delays through the PROMs and qualifier multiplexor; hence, the asymmetric clock.

In some cases the address counter will reach state number 511, known as LAST, either sequentially or through a special branch. It will then roll over through a do-nothing state to state 0. This guarantees that the uppermost bit of the address counter toggles from high to low giving an edge on SASS to act as the Start and Stop signal for Signature Analysis. Also, for testing purposes, the PROM outputs may be disabled to float by pulling the input of the inverter U192 low causing ROMEN-L to go high.

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Table 4.3
State Machine Control Bits

Outputs

Position	Register 0	Register 1
0	LDAB-L	F1-H
1	LDCRC-L	F2-H
2	SNUKY-L	F3-H
3	NEWKEN-H	JAM-H
4	CS0-L	RCFLG-L
5	CS1-L	FCSTR-H
6	CLR0-L	CTCT-H
7	CLR1-L	DRNW-H
8	REN-L	IFLG-H
9	DMAEN-H	LOHS-H
10	WCKEN-H	VERR-H
11	WEN-L	ZCNT-H
12	CRCMR-H	BLANK-H
13	CWE-L	SUCCS-H

Qualifier Bits

Position	Mux 0	Mux 1	Mux 2	Mux 3
0	M0-H	ABCLK-L	CRCA-H	B250-H
1	M1-H	ABCLK-H	CRCB-H	B2-H
2	M2-H	CRCD	B6-H	B3-H
3	F2-H	GAPX-H	CRCL-H	B0-H
4	BLKEN-H	F0-L	CRCK-H	F1-H
5	PCTC-H	F0-H	CRCNF-H	STEST-H
6	ATSPD-H	CMDOK-H	F3-H	REN-H
7	NEWKY-L	KYEXP-H	BIT7-H	UNCOND

4.4 Read/Write Interface to Tape Drive

A comprehensive description of the read and write data paths from the TIB buffers to the HCD-75 drive module follows in the next four sections.

4.4.1 Gap Detection

The HCD-75 drive module contains all the electronics for the support of the read head, including preamplifiers, differentiators, zero crossing detectors, etc. These are necessary to generate a TTL-level signal RDDATA which toggles every time the read head encounters a flux transition. Note that this waveform is still MFM-encoded. Gaps in the tape format are detected by waiting for the RDDATA line to quit toggling.

The drive module uses a data density of 10,000 bits per inch (bpi) and a read/write tape speed of 60 inches per second (ips). Therefore the burst data transfer rate on RDDATA is 600,000 bits per second or 1.67-microseconds per bit. The longest distance between two consecutive transitions in an MFM waveform is two bit-times or 3.3-microseconds. (MFM coding rules are discussed in Section 4.4.3.) Any time that there is not at least one transition on RDDATA every 5-microseconds the gap detection circuitry drops GAP-L to indicate that the read head is presently in a gap. GAP-L is returned high by the first transition after the gap.

The GAP-L signal is implemented as the Q (active high) output of a bidirectional retriggerable one-shot which uses RDDATB (buffered RDDATA) as the trigger input. In actuality the bidirectional one-shot is formed using both halves of U391, a 74LS123, (one half triggered on the rising edge of RDDATB, the other triggered on the falling edge) with the two Q outputs OR-ed together. Both halves of the 'LS123 use a 5-microsecond pulse-width which is conservatively larger than the maximum transition spacing of 3.3-microseconds. As long as valid MFM code is present on RDDATB the one-shots will keep retriggering and GAP-L will remain high. As soon as RDDATB quits toggling GAP-L drops low.

The HCD-75 drive module uses a single track head and steps it across the tape to access one of sixteen tracks. This head contains three gapped ferrite cores: one for reading and writing and the other two for straddle erasing. The erase core is energized in the front gap of a block to be written and left energized until the rear gap. The turning on and off of the erase core records two undesirable transitions in the midst of the gaps. This problem is encountered in all saturation magnetic recording products and has acquired the trade name of "crap in the gap." These undesired transitions will trigger the GAP-L one-shots for 5-microseconds thus creating noise on the GAP-L signal.

The GAPX-L signal is a cleaned up version of the GAP-L signal. GAPX-L goes high sixteen bit periods (27-microseconds) after GAP-L goes high and goes low immediately with GAP-L. Thus, GAPX-L never has a chance to respond to isolated transitions. The penalty is that GAPX-L does not come high until two bytes into the sync field of any frame or key.

4.4.2 Recognition of pre-recorded format

The DC600 tape cartridges as sold are preformatted with key marks approximately every 1.75-inches. Each key mark contains a forward and a reverse key number (with CRC) so that the key can be read in either direction. These key marks delineate 4096-blocks per track each block of which can store 1024-bytes of user data for a total tape capacity of 67-megabytes per cartridge. The quarter length DC615HC cartridge contains 1024 such blocks per track for a formatted capacity of over 16-MB. Each block is recorded as four 256-byte frames of user data plus two 256-byte frames of ECC; thus the error correction scheme chosen by 3M consists of 50% redundant recording. Note that the preamble and postamble bring each frame up to 270-bytes. The tape format is shown in Figure 3.7.2. For more information consult reference 2.3.3.

Besides GAPX-L (see Section 4.4.1), the TIB state machine requires only one other signal in order to determine the current location of the read/write head on the tape. This signal is KYEXP-H which comes high during a gap to indicate that a key number which can be read in the current direction of tape travel is expected to immediately follow the present gap. Figure 3.7.3a shows KYEXP-H assuming that the tape is currently moving forward and Figure 3.7.3b shows KYEXP-H assuming that the tape is moving in reverse.

The circuit which generates KYEXP-H must distinguish the front gap during forward motion and the rear gap during reverse motion without actually knowing which direction the tape is moving. The circuit to accomplish this is shown in Figure 4.4.1.

The 74LS161 counter U1122 is clocked once per byte. If it reaches a count of fifteen, then it will latch up in this state until cleared. The ripple carry-out constitutes KYEXP-H. The counter is cleared by GAP-H so it only counts during gaps. The fact that it has to count up to fifteen guarantees that KYEXP-H will not come on in the inter-key gap (which is only two bytes long) or in any of the inter-frame gaps (also two bytes long). The only remaining problem is to decide between the front and rear gaps and this is accomplished by the 74LS123 one-shots, U1121. The first one-shot fires for 500-microseconds on the rising edge of GAPX-L. The second one-shot fires for roughly 15-milliseconds on the falling edge of GAPX-L if the first one-shot is still active. Thus, the only time that the second one-shot gets a chance to fire is right at the inter-key gap, since this is the only time that GAPX-L's falling edge follows within 500-microseconds of its rising edge. (Note that 500-microseconds represents roughly 37 bytes at 60-ips.)

While the second one-shot is active, the 74LS161 counter is disabled. Therefore, while in forward tape motion the second one-shot disables the counter during the front gap and when in reverse motion the counter is disabled during the rear gap. This ensures that KYEXP-H will come up only in the rear gap during forward tape motion and in the front gap during reverse tape motion. Figure 4.4.1 shows the GAP-L, GAPX-L, Q1 (output of first one-shot), Q2 (output of second one-shot), and KYEXP-H signals for forward and reverse tape motion.

4.4.3 MFM Encoder

The HCD-75 drive module records data using the MFM (or Miller) code. This code is defined by the following encryption rules:

1) Each data bit is encoded in one bit cell. (The HCD-75 records 10,000 bits per inch at 60 inches per second so the bit cell period is 1.67-microseconds.)
2) Transitions are allowed only at the beginning or middle of a bit cell (but not both). However, each bit cell need not contain a transition.
3) A transition in the middle of a bit cell indicates that that bit cell represents a "one."
4) A transition between two bit cells indicates that these two adjacent bit cells both represent "zeros."

Thus MFM only allows three different spacings between transitions: 2T, 3T, and 4T, where 2T is the bit cell width. These transition rates correspond to the 2f, 1.5f, and 1f frequencies, respectively, which are often used to specify the frequency response of magnetic heads. A continuous string of zeros or of ones gets encoded as a square wave of period 4T, or a transition to transition distance of 2T. The data pattern 100100100... gets encoded as a square wave of period 6T and the data pattern 10101010... has a period of 8T.

Straight MFM encoding is easily accomplished by merely a few flip-flops. Unfortunately, the job is complicated by the need for precompensation. In saturation magnetic recording each transition is formed (written) by reversing the direction of the flux in the write head core. Due to the inductive time constants, this reversal in flux more resembles an arctangent function than a true step function. The read head output is proportional to the time rate of change of the flux linking the read head core by Faraday's law. Therefore, the arctangent flux reversal produces a Lorentzian type read pulse. Now, at high data densities the Lorentzian pulses from adjacent transitions overlap and interfere with each other. This interference tends to shift the peaks of the read pulses away from each other, a phenomenon referred to as "peak shift." If the peak shift is too severe, then the phase lock loop which tracks the transitions read back will be unnecessarily agitated and might dump improperly decode the data.

The purpose of precompensation then is to slightly shorten the distance between interfering transitions so that upon read back the peak shift phenomenon will push the peaks back to their correct position. Each MFM data pattern has its own characteristic peak shift which can be estimated based upon the recording density (flux reversals per inch) and the Lorentzian pulse width observed for an isolated transition. The worst case peak shift for MFM encoding occurs for the 2T, 4T, 2T, 4T ... (i.e. 1101101...) data pattern. Most MFM encoders only bother to watch for and precompensate the most severe data patterns. However, the MFM encoder on the TIB can assign a different precompensation value to every different five bit pattern. This is to say that the MFM encoder looks at the i-2, i-1, i, i+1, i+2 bits in the write data stream to decide how to encode the i-th bit. It is assumed that the i-th bit is not affected by bits farther away than two bit cells.

The MFM encoder employs a master clock (provided by a crystal oscillator, Y2131) which runs at 32 times the bit rate. This master clock drives a 5-bit counter which is implemented with two 74S163 counter chips U2112 and U2122. Counts 28 through 31 are decoded by a three-input AND gate U3111 on the three most significant bits of the counter. The output of this AND gate is delayed one clock period by U491, a 74LS109 flip flop, to become the bit clock (BITC-H). Thus,BITC-H has only a one-eighth duty cycle.

The bit clock gates binary data into the MFM encoder from the write data buffers via the WDATA line. Thus, the five-bit counter goes through an entire cycle of thirty-two states for each data bit. The binary data bits are fed into a five-bit shift register U2121. The middle bit in the five-bit shift register is the bit currently being encoded and the other neighboring bits are provided so that the encoder can decide on the appropriate amount of precompensation.

The decision making element is PROM U2111 which uses the five consecutive WDATA bits as its address and outputs a five-bit quantity which represents the count at which the MFM transition for the middle shift register bit should be generated. When the five-bit counter matches the five-bit PROM output, the 74S85, a five-bit comparator, causes a D-type flip-flop U292 to toggle. This flip-flop's output (WRDATB) is the actual MFM code, which after buffering becomes WRDATA and is sent to the drive module.

Since the master clock runs at 32 times the bit frequency there are 32 places within the bit cell where the MFM transition can be located. Thus, we have 3% resolution in our precompensation. The MFM transition for a one is placed in the middle of the bit cell which has been defined as a count of eight. The MFM transition for a pair of zeros is placed between the two bit cells which is then a count of 24 (= 8 + 32 / 2). If we want to precompensate a "one" transition 12% early then we code the PROM for an output of 4 (= 8 - 12% / 3%). If we want to precompensate a paired zero transition 6% late then we code the PROM for an output of 26 (= 24 + 6% / 3%).

Certain MFM patterns (such as for the zero in 101) require a bit cell with no transition. To accomplish this we code the PROM for an output of 31. During counts 29, 30, 31 and 0, the five-bit comparator, U2101, is disabled and therefore the final flip-flop U292 does not toggle during this bit cell. The disabling of the comparator during these counts is necessary for another reason: the next write data bit is clocked into the shift register U2121 at count 29, the rising edge of BITC-H, so that during the next two counts the PROM is settling to a new value and the comparator must be disabled to avoid the possibility of a false comparison.

Note that the bit rate is 10,000 bpi times 60 ips or 600,000 bits/sec so the master clock frequency must be 19.2 Mhz. The five-bit counter period is then 52-nanoseconds. The shift register has a propagation delay of 25-nanoseconds and the PROM access time is 60-nanoseconds. For this reason the PROM had to be allowed at least two states (counts 29 and 30) to settle.

The actual contents of the PROM were chosen based upon error rate studies and other information supplied by 3M. The PROM coding is given in Table 4.4 which can be summarized by the following rules:

1.) Precompensate all 2T, 4T patterns by 15%.

2.) Precompensate all 2T, 3T patterns by 12%.

3.) Precompensate all 3T, 4T patterns by 3%.

The worst case MFM pattern is the 1101 (or its dual 1011) which gets encoded as a 4T transition followed by a 2T transition. The transition corresponding to the middle "one" bit gets severely peak shifted ahead. Therefore, we precompensate the location of this middle transition by moving it back 15% from its normal location, which would have been a count of 8, so that the PROM gets coded with a count of thirteen for the five-bit patterns 01101 and 11101. Similarly, U2111 is coded for a count of 3 for the patterns 10110 and 10111.

4.4.4 MFM Decoder

The decoding of an MFM waveform back into binary data is a straightforward task. The only complication (and it's a beaut) is that this MFM waveform has come off a moving tape and thus is distorted due to tape speed variation and peak shift problems. The peak shift problem is addressed by the precompensation circuitry covered in the previous section at the time data is written. The tape speed variation problem is solved by phase locking a local oscillator to the output of the read head. This local oscillator is then used as a clock to decode the MFM waveform. A complete block diagram of the read data path is shown in Figure 4.4.2.

I will delay discussion of the phase locked loop momentarily in order to first describe the simpler task of MFM decoding. The decoder requires only three inputs, "VCO", "R", and "LOCK-UP". Assume the existence of a local oscillator called "VCO" which is synchronized with the incoming MFM code. This oscillator runs at twice the frequency of the incoming bit rate, or 1.2-Megahertz. We feed the MFM encoded read data line RDDATB into a bidirectional one-shot of period T/2, where 2T is the MFM bit cell period. Note that this bidirectional one-shot is implemented by a digital circuit consisting of a shift register U3131, giving a delay of T/2, and an exclusive-OR gate U3121 (schematic zone D2). The digital circuit was chosen over an analog one-shot so that no trim pots would be required to set the pulse-width. The output of this bidirectional one-shot is known as R (standard notation for one of the phase detector inputs in a phase locked loop). A third signal LOCK-UP comes high once we are assured that th phase lock loop has synchronized VCO with RDDATB. These three signals are fed into the MFM decoder to produce a binary data output RDATA which is clocked into the TIB data buffers by RCLK. The MFM decoder consists of four flip-flops and is best explained by the timing diagram of Figure 4.4.3.

The first flip-flop U492 is merely a divide-by-two on the VCO line to produce "VCO/2." The next flip-flop serves to detect ones in the data stream. A "one" bit is detected whenever the rising edge of R (therefore any edge of RDDATB) occurs during the "ones window" which is defined by VCO/2-L. After each bit cell the detect ones flip-flop is cleared.

The third flip-flop, the other half of U492, latches the output of the ones detector and properly synchronizes it with RCLK. This flip-flop's output is the read data (RDATA) which is transfered to the TIB data buffers. The fourth flip-flop U491 serves as a "data valid" flag. After the lock-up signal goes high (indicating that the VCO is properly synchronized) this flip-flop begins watching the RDATA line for any detected ones. The lock-up signal goes high 32 bits into the 48-bit sync field. Prior to this time the VCO might not be properly phase locked and the RDATA line might detect spurious ones. But by the thirty-second bit the decoder should be stably detecting all zeros. Now the 48-bit sync field actually consists of 47 zeros plus a one. This final bit is the "sync bit" and heralds the end of the sync field and the start of data. It is this one bit for which the data valid flip-flop watches. Once this first one is detected the RCLK is enabled and the data transfer to the TIB data buffers actually begins. Note that the sync bit is swallowed and is not transfered to the data buffers.

The only problem left is that of keeping the VCO synchronized with RDDATB and this is the job of the phase locked loop. Any phase lock loop (PLL) consists of three basic functional blocks: a phase detector, a loop filter, and a voltage controlled oscillator (see Figure 4.4.2). The phase detector has two inputs, R and V, and two outputs, "speed-up" and "slow-down." R is the output of a bidirectional one-shot triggered by RDDATB. The one-shot period is T/2 where the bit cell period is 2T. Note that the only allowed MFM transition spacings are 2T, 3T, and 4T (corresponding to the 2f, 1.5f, and 1f frequencies used in specifying magnetic heads).

The R phase detector input got its name because this is the reference signal to which you are phase/frequency locking a local oscillator. The other phase detector input V is fed back from the voltage controlled oscillator. The phase detector compares the two input waveforms R and V and signals on its two outputs whether the VCO needs to speed up or slow down to match the reference. MFM decoding requires an edge sensitive phase detector. That is, it outputs a correction signal only between the falling edges of the R and V pulse inputs. Thus, R and V need not have the same duty cycle to achieve lock up, although in actuality they do.

The loop filter accepts the two phase detector outputs and filters them to present a smoothly varying control signal (Verror in Figure 4.4.2) to the VCO. This loop filter is generally an integrator and its time constants are the major determinant of the PLL's transient (locking and tracking) behavior and noise bandwidth. These time constants are chosen so that Verror displays roughly critical damping and achieves lock-up about half way (40-microseconds) into the sync field.

The PLL bandwidth is set by the loop filter at the absolute minimum that will still allow lock-up within the first half of the sync field. This bandwidth means that the PLL can track (without losing lock or misdecoding data) a plus or minus five percent sinusoidal speed variation on RDDATA at up to a 4400-Hz typical modulation frequency and ten percent variation up to a 1400-Hz modulation frequency.

The R phase detector input will receive a pulse, of width T/2, on every edge of RDDATB. These pulses can be separated by 2T, 3T, or 4T. The feedback nature of the phase locked loop attempts to align a pulse on V with every pulse on R and therefore V must run with period T so that there is a V pulse available to match up with each incoming R pulse. The excess V pulses must not confuse the phase detector into thinking that the VCO needs to be slowed down. The phase detector must output a correction signal only when an R and V pulse arrive roughly simultaneously and must output no correction when a V pulse arrives by itself. Recall that the phase detector aligns only the negative edges of the R and V pulse trains so that it is possible to use the pulse width of R to define what is meant by "arriving roughly simultaneously." If V goes through a complete cycle (i.e., rises and falls) before R even starts a cycle (rises), then the phase detector ignores this V pulse and does not generate a correction signal. If, however, R is high when V falls then a "slow down" signal is sent from the falling edge of V until the falling edge of R. Anytime R falls before V a "speed up" correction is output.

You can consider each pulse on the R and V inputs to carry a certain amount of information about the current synchronization of the two signals. We make use of all the information available on the R input. Every R pulse will result in some type of speed correction being output. At most, only every other V pulse results in the generation of a correction signal.

Every recorded area on the tape (including key numbers) has the basic format of sync field, preamble (header), data and postamble (CRC). The sync field is intended for the sole use of the PLL. It provides the PLL a chance to acquire lock with the RDDATB signal before actual MFM decoding begins. The first data actually passed out of the decoder is the preamble.

While the tape head is in a gap, the PLL is locked to an alternate clock derived from the 19.2-Mhz crystal. This keeps the PLL running at roughly the correct frequency in order to minimize the time required to lock to RDDATB. The GAP-L signal comes high at the beginning of the sync field. This switches the R phase detector input from the crystal to actual RDDATB.

Since it is always known what is written in the sync field (47 zeros followed by the sync bit), the PLL can be configured to take maximum advantage of the pattern. The R input will be a regular pulse train of T/2-width pulses separated by 2T. This is shown in Figure 4.4.4. To take advantage of this fact the phase detector is placed in the acquisition mode by having the LOCK-UP signal low. In this mode the phase detector is made both phase and frequency sensitive and only every other VCO pulse is fed back to the V input. The R and V inputs are identical during acquisition. The feedback nature of the PLL then forces the VCO to adopt a frequency of 1/T in phase with RDDATB. Two-thirds (32 bits) of the sync field are allocated for the PLL to settle to the RDDATB signal.

After the sync field, the R phase detector input will become an unknown pattern of 2T, 3T, and 4T spaced pulses. Therefore, the phase detector cannot remain frequency sensitive. The PLL must now generate speed correction signals only when roughly coincident R and V pulses arrive at the phase detector.

A bit counter waits until 2/3 of the sync field has passed before raising LOCK-UP to signify the end of the acquisition mode and the beginning of the track mode. In track mode the phase detector is only phase sensitive and does not mind the fact that V runs with twice the maximum frequency of R. The VCO signal is now fed back in its entirety to the V phase detector input so that there is always a V pulse available to line up with the R pulses regardless of whether these pulses arrive with 2T, 3T, or 4T spacing. It is now up to the phase detector to choose among the V pulses in generating speed correction signals to the VCO.

When LOCK-UP goes high 2/3 of the way into the sync field, the VCO will be properly synchronized with RDDATB, and decoding of MFM is therefore possible. The MFM decoder is enabled by LOCK-UP and begins watching for the first one bit, which will be the sync bit. After finding the sync bit the decoder begins clocking the succeeding preamble bits into the data buffers. Since the sync field has ended, the R input will quit being a constant frequency squarewave and will become a complicated pulse train with 2T, 3T, and 4T pulse spacings. The phase detector now occassionally has to wait up to two bit-cells before it sees coincident R and V pulses so that it can output a new speed correction signal on Verror to the VCO.

No discussion of the read process for magnetic tapes would be complete without a mention of drop-outs. A media imperfection or a momentary head to tape separation will cause a degradation in signal amplitude known as a drop-out. At the TTL-level interface to the drive module a drop-out is characterized by missing transitions in a frame or key. Any missing transitions will just about guarantee that the data will be incorrectly decoded. Therefore, it is up to the 50% redundant recording method of error correction to come to the rescue and recover the data.

Once the MFM decoder has begun shipping data to the TIB data buffers it will continue to do so until the TIB controller drops the REN-H line. Thus, once LOCK-UP comes high it will remain high until REN-H drops. Therefore, it is up to the controller to distinguish between valid format gaps and drop-outs. Once the controller requests data, the PLL will remain locked to the RDDATB signal (regardless of whether or not it is even toggling) until the controller has decided that it has received enough bits. The controller will then drop REN-H which will drop LOCK-UP and the PLL will return to tracking the alternate clock generated from the on-board crystal. Note that RCLK (which clocks decoded data into the TIB buffers) is enabled by DATA VALID which in turn is enabled by LOCK-UP which is enabled by REN-H.

If it should happen that the PLL remains enabled through a dropout where RDDATB is not toggling (so that the R phase detector input is quiet), the VCO will coast at the current frequency. Neither speed-up nor slow-down signals will be generated.

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Table 4.4
MFM Precompensation PROM Contents as Percent

PROM Input A4	3	2	1	0	hex	Transition Pattern	Precompensation in percent	PROM Output dec	hex
0	0	0	0	0	0	2, 2	0	24	18
0	0	0	0	1	1	2, 2	0	24	18
0	0	0	1	0	2	2, 3	-12	28	1C
0	0	0	1	1	3	2, 3	-12	28	1C
0	0	1	0	0	4	3, 3	0	8	8
0	0	1	0	1	5	3, 4	-3	9	9
0	0	1	1	0	6	3, 2	+12	4	4
0	0	1	1	1	7	3, 2	+12	4	4
0	1	0	0	0	8	none	NA	31	1F
0	1	0	0	1	9	none	NA	31	1F
0	1	0	1	0	A	none	NA	31	1F
0	1	0	1	1	B	none	NA	31	1F
0	1	1	0	0	C	2, 3	-12	12	C
0	1	1	0	1	D	2, 4	-15	13	D
0	1	1	1	0	E	2, 2	0	8	8
0	1	1	1	1	F	2, 2	0	8	8
1	0	0	0	0	10	3, 2	+12	20	14
1	0	0	0	1	11	3, 2	+12	20	14
1	0	0	1	0	12	3, 3	0	24	13
1	0	0	1	1	13	3, 3	0	24	18
1	0	1	0	0	14	4, 3	+3	7	7
1	0	1	0	1	15	4, 4	0	8	8
1	0	1	1	0	16	4, 2	+15	3	3
1	0	1	1	1	17	4, 2	+15	3	3
1	1	0	0	0	18	none	NA	31	1F
1	1	0	0	1	19	none	NA	31	1F
1	1	0	1	0	1A	none	NA	31	1F
1	1	0	1	1	1B	none	NA	31	1F
1	1	1	0	0	1C	2, 3	-12	12	C
1	1	1	0	1	1D	2, 4	-15	13	D
1	1	1	1	0	1E	2, 2	0	8	8
1	1	1	1	1	1F	2, 2	0	8	8

^ This bit (column 2) is the one being encoded.

A	48-6116	sjb/RF	03-15-83	MODEL 7908	STK. NO. 07908-60241
		/	- -	INTERNAL MAINTENANCE SPECIFICATION, TAPE INT	
		/	- -	BY	DATE MAR 13, 1984
LTR	P.C. NO.	APPROVED	DATE	APPD.	SHEET NO. 56 OF 88
REVISIONS				SUPERSEDES	DWG. NO. A-07908-60241-10

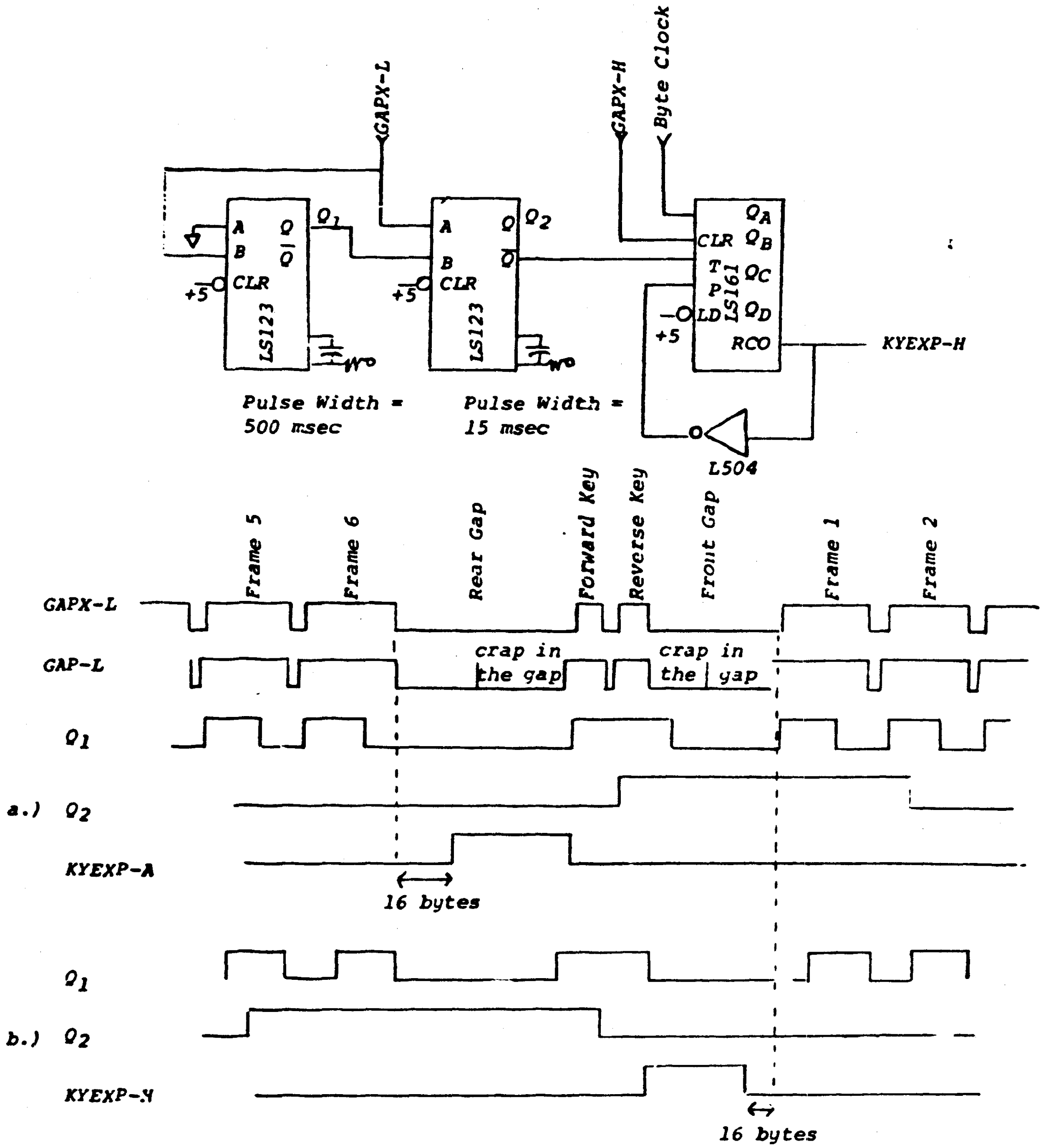

FIGURE 4.4.1
Key Mark Recognition Circuit
Showing Operation During a.)
Forward and b.) Reverse Tape
Motion. Note that the Frames
are Numbered for an Even Number
(Forward Motion) Track.

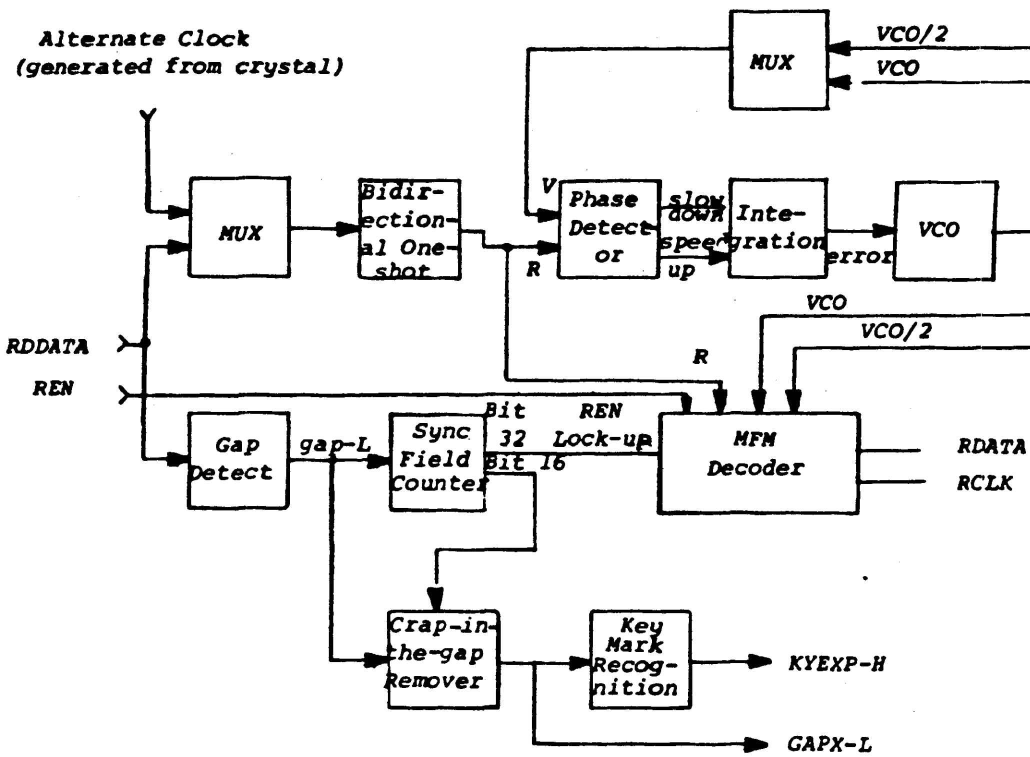

FIGURE 4.4.2

Block Diagram of Read Data Path
Showing Phase Lock Loop and MFM Decoder

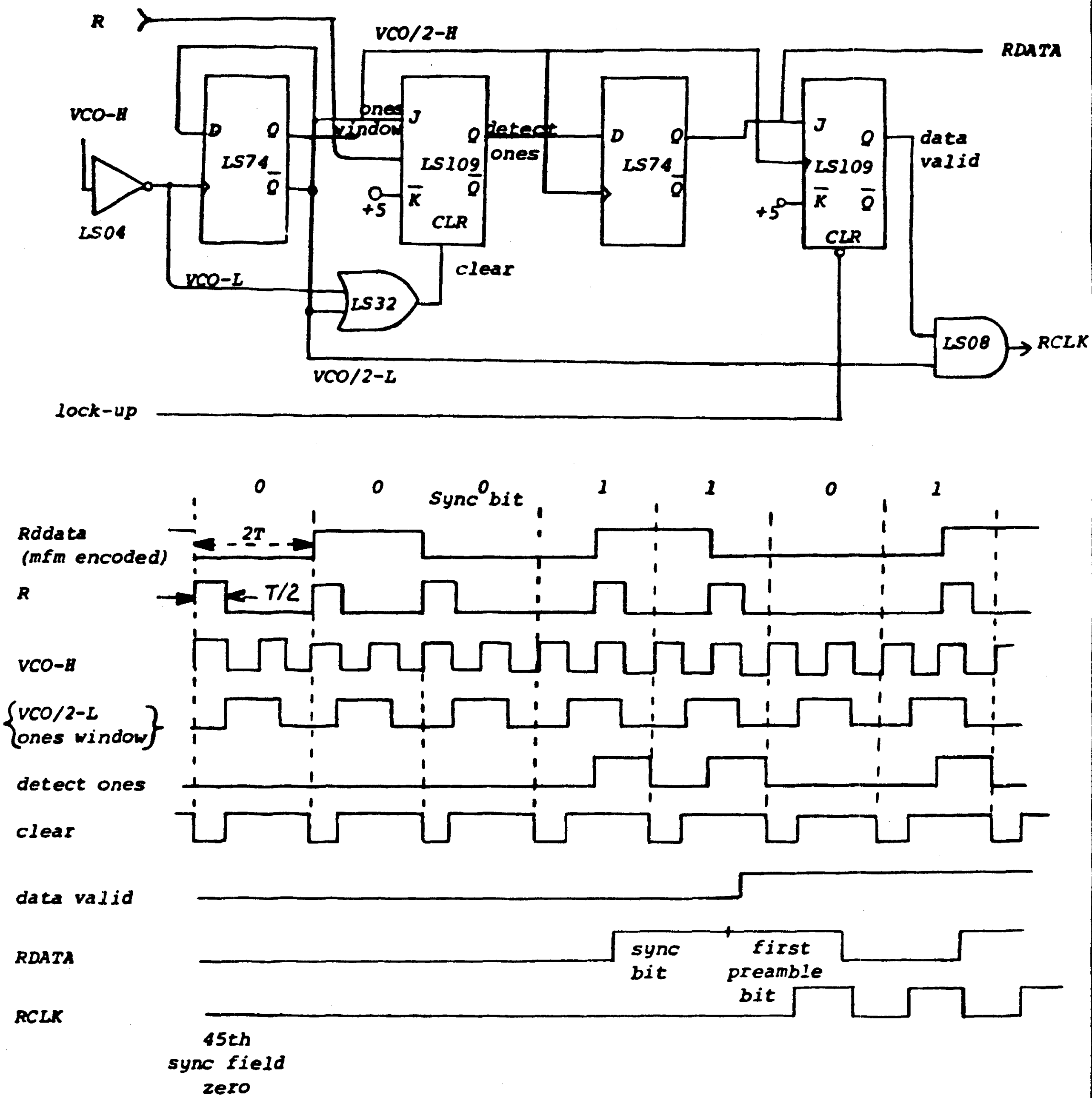

FIGURE 4.4.3

MFM Decoder Circuit
and Timing Diagram. Note that
LOCK-UP has been high since 32nd
sync field bit

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REV. NO.	DATE	DWG. NO.	SHEET
A	1-28-83	A-07908-60241-10	60 OF 88

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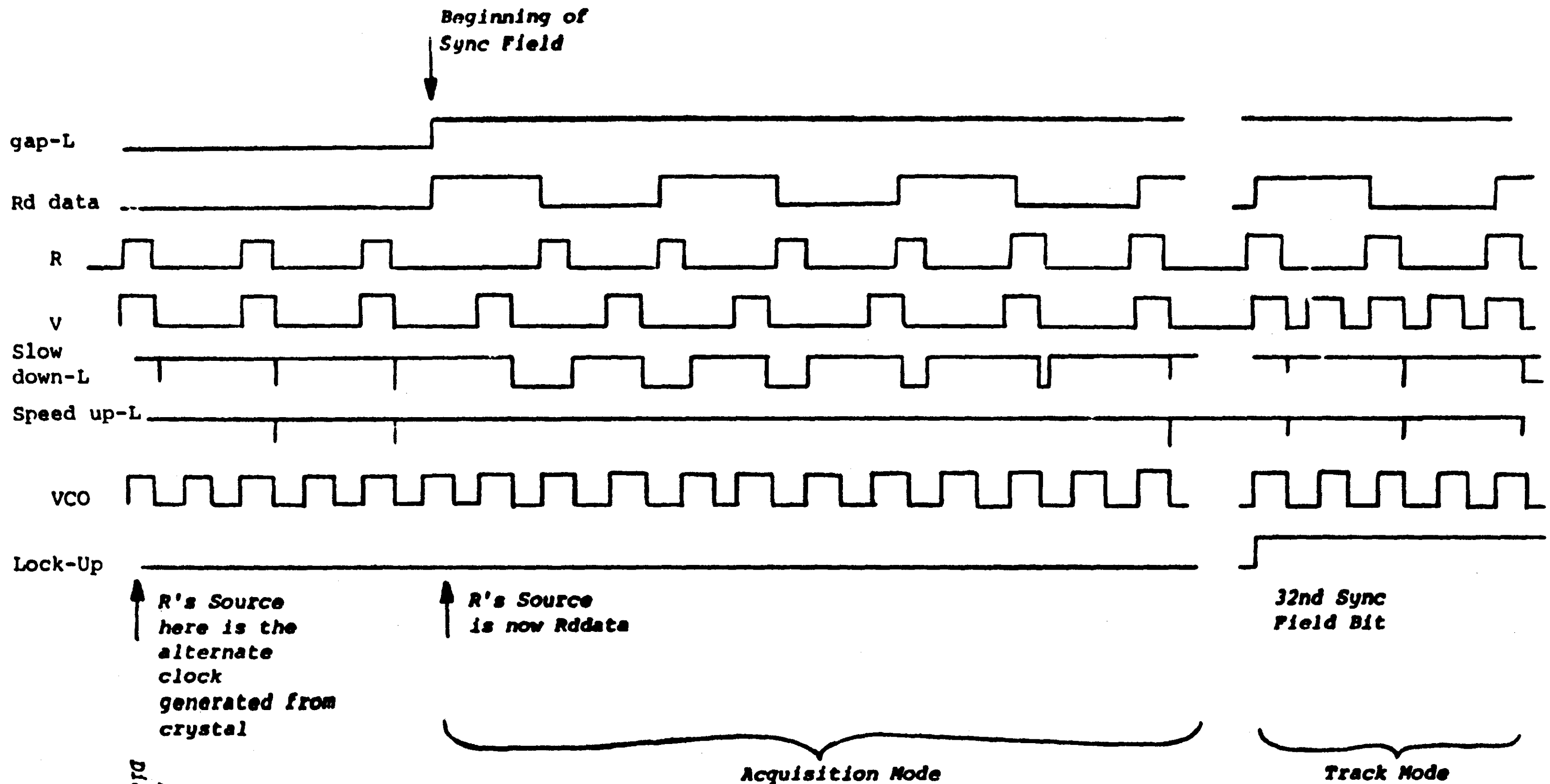

FIGURE 4.4.4
Phase Lock Loop Timing Diagram During Acquisition

4.5 DMA Interface, including State Machine Control

The interface between the TIB and the DMA (Direct Memory Access) boards consists of five signal lines. Only one of these, DOUT-H, is always connected to the corresponding output signal from the DMA, whereas the remaining four are inputs to the DMA being driven by the TIB and are capable of being disconnected via a three-state buffer (U452) under control of the microprocessor by means of the DMAC-H signal. This allows another device, such as a disc drive to timeshare the same DMA port. Three of these four lines are used for control in passing DOUT-H or the fourth line, DIN-H. The RWC-L, a 9.6-MHz clock signal with a fifty percent duty cycle, was covered in section 4.2 above. The other two control lines are SOS-L and SOD-L.

The TIB pulses SOS-L to its active low state (U462, U452) for two full RWC periods as it loads its own byte counter (using LDAB-L) with an initial count of 248. This acts as a wakeup alarm to get the attention of the DMA. Several clock cycles after this Start Of Sector, the TIB will pulse low on SOD-L (through the other half of U462) to indicate the Start O Data. The number of clock periods between these two control pulses depends upon the direction of data transfer, being twelve for a write from the DMA to the TIB and eighteen for a read from the TIB to the DMA, and is controlled by gate U262 (schematic zone F24). The data transfer begins in a most-significant bit first manner with the six-byte header followed by 256 bytes of data, a two-byte CRC and place holding dummy bits for five bytes of Fire Code check word which may later be filled in by some discs. Due to DMA design requirements, the first usable bit of data is separated from the SOD-L pulse by four dummy bits in the mode in which the DMA is writing to the TIB and by six dummy bits in the read mode. The microprocessor is responsible for setting up the DMA circuitry to converse with the TIB. The Sector Toggle STOG-H line is used to monitor the progress of the transaction since the TIB expects to transfer four sectors (one block) of data at a time whereas a disc connected to the same DMA port would only pass one sector at a time. A fifth STOG transition and a fifth SOS pulse are sent to the microprocessor and DMA, respectively, to terminate a block transaction. More information on the DMA interface can be found in the IMS for that board.

4.6 Modes of Operation

4.6.1 Non Data-Transfer Operations

The TIB is capable of controlling and/or participating in various modes which do not involve the transfer of data. These include seeking to a particular block on the tape, an off-line verification of any number of blocks on the tape track currently over the head, and various diagnostic and debug modes.

4.6.1.1 Seek (Coarse)

Certainly the most frequently invoked, and yet the most humble, mode is Seek. Prior to attempting a read, write or verify on a particular block on the tape, the controlling microprocessor must first cause the transport to locate that block. The processor has direct access, via control register 8 mentioned in section 3.8, to the drive electronics for the positioning of the head onto the proper track of the tape and can initiate motion along that track, but must rely on the TIB to locate the desired block. Since the TIB is only capable of carrying out a relative seek it must in turn rely on the processor to set up the length. But then the processor only knows where it wants to go and cannot compute the relative distance until it knows the current location. This is easy if either BOT or EOT (Beginning or End OF Tape) status is showing in the Drive Status register 0, but, if not, the TIB must be requested to do a "Fine Seek" in order to return the current location. This "Fine Seek" is a subset of any data transfer operation and will be covered in section 4.6.2.

Given the current location of the tape and knowing the target address along a given track, the processor computes the relative distance in units of data blocks and sets this number into a register in the Counter Timer Circuit (CTC) on its own board. This number is adjusted to allow for worst case rates of acceleration and deceleration of the tape drive as well as an offset to allow for pre-positioning for the next operation. This offset will stop short of the target for the case in which the next operation will continue in the same direction as the seek or it will cause the tape to overshoot the target to allow for an acceleration following a reversal in direction.

Once the seek length is loaded into the CTC and the tape is in motion, the processor requests the TIB (via register 9) to begin the countdown to the target. The state machine first waits for the tape drive to return At Speed status, then begins monitoring the KYEXP signal which was covered in section 4.4.2. Since only one KYEXP pulse occurs per block and since this circuitry was designed to work for both the 60-ips read/write speed and the 90-ips seek speed, all the state machine has to do is to count the number of pulses. The state machine pulses the CTC on the processor board each time KYEXP goes high and watches for the CTC to return a carry output. The state machine then jumps to its ZCNT (zero count) routine and jams a Stop Motion command to the tape drive, while returning appropriate status to the processor.

4.6.1.2 Read Key, or "Fine Seek"

While not a mode by itself, a "fine seek" is a necessary prerequisite to any activity involving data and the tape. This operation therefore is a subset of the read, write and verify modes. The coarse seek of the preceding section puts the target block on the tape near the head then requests one of the data transfer modes which includes this fine positioning algorithm. Essentially, the data transfer operation is begun, but no data is actually transfered pending the assertion of BLKEN (Block Enable) by the processor. The state machine will continue reading the tape and passing block numbers to the processor until it finds the desired target (known only to the processor) and then enables the block for transfer.

More specifically, the state machine waits for the tape drive to return At Speed status and then begins looking for a Key Mark. In this case the KYEXP hardware is not used but a similar algorithm is implemented in firmware. Basically, this amounts to watching the GAPX signal and picking out gaps having a width exceeding the time equivalent of twenty-seven bytes (a convenient count, greater than sixteen), or 360-usecs. Gaps of this length occur as long dropouts in data frames, or legitimately between the Reverse Key Mark and the first data frame of a block, or immediately prior to the Forward Key Mark. It is the latter that we wish to segregate.

The state machine begins with the assumption that any data following such a gap is indeed a key mark until proven otherwise. In this manner it signals the PLL (part of section 4.4.4) to Lock-up and to begin passing data following recognition of the Sync bit. The state machine shifts the first two bytes of this data, least significant bit first, into a sixteen bit register composed of U431 and U441 enabled by control bit NEWKEN. This same data stream along with the next two bytes, presumably the CRC code bytes for the Key Mark, are routed to the CRC checker U1112. If, after these four bytes have been trapped, the CRC syndrome tests equal to zero, then we have made a successful capture of the Key and will so notify the processor by using SNUKY to set the NEWKY flag U322. If the CRC does not go to zero, we still have a chance that this really was the Key Mark but contained an error. We can double-check by testing that the length of the data field is appropriate to a four-byte Key Mark, following the usual six-byte sync field, which was stripped by the PLL circuitry. If the data area is of the proper length but contains a CRC-detected error, we will continue, assuming that at least we are properly oriented with respect to the block timing on the tape. In the case of this being a fine seek which is part of a read operation, we will later extract the correct block number from the data frames, in which case we will wait with SNUKY, but if we are being asked to do a write operation, we will set NEWKY and rely on the processor to notice the CRC flag set in register 5 for the bad key and therefore to hold off on BLKEN. If, in the remaining case, the data field is too long to be a valid Key Mark, then we must have come upon either the first data frame or have stumbled into a dropout; in either case, the state machine returns to searching for a twenty-seven byte gap.

In a read or verify mode, the state machine will continue toward the data transfer portion of the operation following recognition of a Key Mark, whether the data is correct or not. For a write operation, however, further action depends upon the condition of BLKEN. Once a Key Mark is detected, good or bad, the CTC, which had been set up by the processor as a timer, is triggered by the state machine to begin a timeout to guarantee that the erase head clears the preformatted region of the tape by a suitable margin. This same time interval allows the processor to pass judgment on the key number and its CRC. If the processor likes what it sees it will set BLKEN high and the state machine will jump to the DMA portion of the data transfer. If, on the other hand, the processor either sees a CRC flag or the wrong target number, it will withhold BLKEN, the state machine will see the CTC time out, and return to find the next Key Mark; the default is to abort the write to tape.

4.6.2 Data Tranfer Operations

4.6.2.1 Write Data from DMA to Tape via TIB

A Write to Tape operation is accomplished in several steps. The first of these requires positioning of the tape head at the appropriate location on the tape; this is accomplished by utilization of the coarse and fine Seeks which were covered in section 4.6.1. Once the proper block on the tape has been found through the coarse seek, the microprocessor will put the TIB state machine into the Write mode and it will do the fine seek. This locates the block to be written, usually (explanation coming soon).

Before passing control to the TIB, the processor will have preloaded the appropriate channel of the CTC with a delay time corresponding to the time between the Key mark and the turn-on of the erase current, varying according to forward or reverse direction of tape motion. If the key number read by the TIB and passed to the processor is the proper target, the processor will raise BLKEN prior to the expiration of the delay. On the other hand, if the key read is not the target or it has a bad CRC, then the processor will allow the CTC to timeout without raising BLKEN and the TIB will return to the fine seek mode looking for the next key. (In reality, the processor restarts the CTC with a time value set near zero so that it will time out very quickly, but without giving BLKEN.)

Once the target has been found and the first CTC value has timed out with BLKEN present, the state machine will retrigger the CTC for the delay from erase to data and begin a DMA transfer. During the first delay the processor will have loaded the CTC with the proper time value and set up the DMA buffers as needed. As soon as this second delay expires, the TIB will begin writing from its RAM buffers to the tape. The four data frames are copied directly from the RAM with insertions for sync fields. The two ECC frames are created on the fly by simultaneously reading data from both RAMs and exclusive-ORing the results for transmission to the MFM encoder and on to the tape. HINST is ORed into the data stream to create the proper frame number in the header of the ECC frames. Two-byte interframe gaps are generated between adjacent frames.

At the end of the data area of the block, the state machine again triggers the CTC (preset by the processor) and holds the WRDATA line quiet to erase a clean final gap. When the CTC completes, the TIB reverts to the fine seek mode in preparation for the next block.

4.6.2.2 Read Data from Tape to DMA via TIB

To read from the tape it is first necessary to find the target block; this is accomplished using the Seek modes mentioned earlier. The target is approached using the fine seek contained in Read Mode 2. After each Key Mark is recognized and passed back to the processor, the state machine continues reading the data and storing it in the appropriate RAMs. If, after the reading from the tape is complete, the TIB notices that the processor has set BLKEN high, then a Successful Completion status will be passed to the MPU and the state machine will halt expecting to be restarted for a DMA Read transfer. If, however, BLKEN had not been set prior to completion of the read from tape, then the state machine will treat its activity as a fine seek and continue to do more of the same. This process will continue until either the TIB is restarted, the tape runs into BOT or EOT, or the processor fails to clear the New Key flag NEWKY by reading one key number prior to the receipt of the next, in which case the TIB will stop the tape using JAM and issuing a Loss of Handshake status message.

While reading data from the tape, the first two frames are stored into RAM0 U362 and the next two into RAM1 U461. At the end of each frame the CRC status for that frame's header and data areas is sampled and stored away into the eight-bit addressable latch U221. When the fifth frame is reached on the tape, the CRC's for the first and third frames are checked to detect whether or not error correction is required. If the frames are signalled to be either both good or both bad, then the fifth frame is not stored and the first and third will stand without alteration. If, on the other hand, one of the pair of data frames is shown to be good and the other bad, then the first step of the two-part correction procedure will take place, namely the overwriting of the bad data frame with the presumed good error correction frame. Similarly, the sixth frame may be used to overwrite either the second or fourth frame in the upper half of one of the RAMs. The actual writing of the data into the RAMS is controlled by the state machine through its output register U251 using the chip selects to select one RAM at a time even though both will receive a common write enable RAMWE and output disable (a function of MOUT).

After BLKEN has been recognized following the read of a block of data from the tape and the TIB has sent a Successful Completion flag to the processor, it is assumed that the processor will set up the DMA, connect it to the TIB using DMAC and restart the state machine in Mode 3 for the actual transfer of data to the DMA. It is during this transfer that the second of the two-part error correction scheme is executed. Prior to the transmission of any frame the state machine will sample the CRC status bit in U221 for that particular frame. If the bit is low, the frame being good, then the frame will be sent as is. However, a high CRC due to a bad frame will cause transmission of the bit-by-bit exclusive-OR function of the frame in question and its correspondent in the frame pair (that is, frame one with three and two with four). The assumption here is that if a frame is marked bad then it has already been overlayed by the proper error correction frame. For a specific example, take the case of a bad frame two. When frame six was read from the tape it would have been written to RAM over the top of frame two -- this is the first phase. During the DMA transfer it is noted that the second frame was bad and therefore presumably overwritten by the sixth which will now be exclusive-ORed with the fourth to create a good copy of the second,providing of course that the sixth was good -- the second, and completing phase. In any case where the error correction frame in use is also bad the error is automatically uncorrectable, since the correction would not have been attempted if another associated frame had not also been bad. It is left to the microprocessor to determine directly from the contents of U221 whether or not an uncorrectable error has occurred.

4.6.2.3 Tape Verification, Offline by TIB

Though not presently supported by the microprocessor with regard to user data, this mode (TIB op code 5) is used to verify the system blocks (spare tables and such). Very similar to the Read from Tape, the hardware Verify begins with a fine seek phase. The processor loads the TIB's channel of the CTC with the number of blocks to be verified, up to 4096 for one full track. Once BLKEN is asserted to show approval of the key number, the TIB will do the equivalent of the read operation without requiring the processor to approve any additional key numbers. The Verify varies from the read in the action performed at the end of the block. If the block was completely acceptable, the CTC will be counted down by pulses from the state machine until it reaches zero. At the zero count, ZCNT status is asserted and the tape is stopped by the TIB via the JAM signal which strobes a !3D command to the HCD-75. On the other hand, any time that even a single frame or a key is found to be in error based upon the CRC results, the tape is also brought to a halt by the same means and a Verify Error status is reported. In the course of a verification blocks that are not recorded are distinguished from long dropouts and are not flagged as faulty so that this mode may be used to verify the key marks on an otherwise unwritten preformatted tape. Since this mode is completely self-contained once set up, disc operations can be executed by the processor while the tape is running on its own without intervention, until the end of the track is reached, at which time the processor is needed to step the head to the next track and initiate the change of direction of motion command sequence to the tape mechanism. It is possible for the processor to be clever and set a much larger number into the CTC and rely on the EOT and BOT detectors in the tape mechanism to stop the tape and flag the processor through the TIB; in this manner a full tape could be verified essentially without attention except on a periodic interrupt basis to step tracks and reverse direction.

4.6.3 Diagnostic Modes

4.6.3.1 DMA Loopback

Selection of mode 0 causes a response almost identical to the DMA portion of the Write from DMA to Tape mode 1. In this manner a transfer from the DMA to RAM on the TIB can be executed without the presence of a tape. When this is followed by a mode 3 transfer from the TIB's RAM back to the DMA, the loopback is completed. This sequence, controlled by the microprocessor which is responsible for generating the random data patterns, storing them in the DMA's RAM and comparing the data when it is returned, is used as a quick detection of problems in the RAMs and SERDES as well as the interface circuits between the DMA and TIB boards. Mode 0 only differs from the DMA portion of mode 1 in that the CRC flags stored in U221 are cleared prior to the first (write) transfer so as to avoid the unpredictable results that would occur if the subsequent call of mode 3 were to attempt the second phase of the error correction process described in the appropriate section above.

4.6.3.2 Buffer Fill Mode

If execution of the DMA/TIB loopback sequence should point up a failure in some portion of the circuitry tested, it becomes desirable to narrow the field of suspected components. This is assisted by use of mode 6. This mode when called upon will cause the TIB's state machine to generate a known data pattern and store it into the RAM. The pattern can then be transferred to the DMA via mode 3 and checked by the processor to segregate problems between the read and write paths connecting the TIB and DMA. The pattern generated is an alternation of four bytes each of all ones and all zeros through all four frames.

4.6.3.3 Write Bad CRC to Tape

By raising the Self Test Select bit simultaneously with the selection of mode 1, the TIB can be commanded to write information containing known faults to the tape. The specific faults are bad CRCs on the second and fifth frames. A subsequent read of the improperly written block will show CRC tags set for these two frames, cause the error correction circuitry to be invoked to restore frame two and produce no error correction response to the faulty fifth frame. This mode is normally executed as part of the power-on self-test on a particular block in the system area of the tape near BOT.

5.0 GLOSSARY of Signal Names and Other Terms

A0-H thru A3-H: The lower four bits of the microprocessor's address bus are decoded on the TIB to select one of the ten registers which are used in the processor interface. When A3 is at a logical low, one of seven Status registers may be read at the concurrence of TIBS-L and RD-L. One of three Command registers may be written when both TIBS-L and WR-L are active.

AC0 through AC2: These three signals are the outputs of the bit counter and will be decoded for various timing signals that occur within each byte.

ABCLK-H: A composite signal made up of RCLK-H when REN-H is active in a Read from Tape mode, or BITC-H during an active WCKEN-H in the Write to Tape mode, or RWCB-H while DMAEN-H is asserted during a DMA transfer in either direction.

ASM: Algorithmic State Machine is the name used within HP for a sequential logic circuit whose outputs are a function of variable inputs with regard to their history. See Chris Clare's book "Designing Logic Systems Using State Machines".

ATSPD-H: The conjunction of ST06-H being asserted while ST07-H is low signifies that the HCD-75 Drive Module is At the requested operating Speed.

B0-H through B7-H: These eight signal lines are the outputs of the counter which determines the current byte location within a page of the RAM buffer. They will be decoded for the placement of various control and overhead bytes associated with each sector of a DMA transfer and each frame of a Tape transfer.

B2-H: Recognition of this signal, one of the eight above, allows the state machine to watch data pass in four-byte increments.

B3-H: The state machine monitors this line, one of the eight above, to count off data in eight-byte parcels.

B6-H: A state machine qualifier for counting sixty-four bytes at a time.

B249-L: Byte 249 is one of the outputs decoded from the byte counter while F0-H is deasserted. This signal is used to generate the SOD-L pulse for the DMA interface at the appropriate time during a Write from the DMA to the TIB.

B250-L: Byte 250, also decoded from the byte counter whenever F0-H is deasserted, serves two purposes. During DMA Reads from the TIB, the SOD-L will be placed during this byte, whereas during a Write to the Tape, this byte signifies the end of the sync field.

B253-L: Byte 253, locates the Track/Frame-Number Byte of the header during a data transfer when F0-H is low.

BIT2-L: A marker for the third bit (counting 0 to 7) of each byte, this locates SOD-L for DMA Reads and modifies frame numbers for writing the headers of the Error Correction Frames to the tape.

BIT4-L: Marks the fifth bit (numbered from 0) of each byte and is used to place the SOD-L for a DMA Write operation.

BIT6-L: The seventh bit of each byte provides an edge that is timed appropriately for writing into the RAM buffer.

BIT7-L: The location of the last bit of each byte is used by the state machine to count out the passage of single bytes and, when in the Write to Tape mode, is used at appropriate times to insert the final one-bit at the end of the all-zeroes sync field.

BITC-H: Bit Clock occurs at 600-kHz for writing data to the tape.

BLANK-H: When the microprocessor requests a block of data to be read from the tape and the TIB finds that that block contains no user data, a BLANK error status is returned indicating that the read operation should not have been performed on the block in question. This avoids the confusion that would result if the data remaining in the RAM from a previous read were to be transferred to the DMA as if it came from the current block.

BLKEN: Block Enable, command from microprocessor raises high after key has been accepted so state machine can read or write.

BSOD-L: Buffered Start-of-Data is the sum of the signals for the DMA read and write modes decoded from appropriate bit and byte locations.

BYTCK-H: Byte Clock, occurring with a 13-1/3 microsecond period, is used as a timer input to circuitry which anticipates the preformat of the tape during a Read operation.

CACKN-H: Command Acknowledge from the HCD-75 Drive Module indicates readiness for another command or for the second byte of a two-byte command from the TIB.

CLR0-L,CLR1-L: These two signals Clear the respective contents of the two SERDES (Serial/Parallel) Registers which interface the DMA and tape to the buffer RAM. They are generated directly by the state machine.

CLRX: Shorthand notation for referring to both CLR0 and CLR1 at the same time.

CMD00 thru CMD07: The Command Bus from the TIB to the Drive Module is defined in the 3M Company document mentioned in Section 2.3.1 above. The commands sent to the drive on this bus ordinarily are generated by the microprocessor and passed through the TIB Command Register at Address 8, but in some cases where the TIB determines that the drive should be halted more quickly than the microprocessor may be able to respond, the TIB may issue a Stop Command (3D, hexadecimal) on its own.

CMDOK-H: Command Okay is the conjunction of both CACKN and SSTROBE being deasserted, indicating that current Drive Status is valid and that the drive is ready to accept another command.

CRC: Industry standard abbreviation for Cyclic Redundancy Code or Check. The code used to detect errors in data transmissions between TIB and tape is CRC-16, also known as Bi-Sync, with the polynomial X^16+X^15+X^2+1.

CRCA-H: Cyclic-Redundancy-Check Results, 0 if good and 1 if in error, are reported for the first two data frames depending upon the odd/even condition of the frame number. If the frame number is even, F1 low, then CRC status for the first frame (CRC0) is shown here; if currently selecting an odd frame, F1 high, then CRCA is equivalent to the CRC status of the second frame, CRC1.

CRCB-H: As for CRCA above, this bit reflects the status of the CRC Results for the third or fourth data frames, bits 2 or 3 of the CRC Flag Register at Status Address 5, depending upon the present value of F1, the least-significant-bit of the frame counter.

CRCD-H: Data to the Cyclic-Redundancy-Code Generator/Checker is derived from RDATA-H or WDDAT-H depending upon which one of REN-H or WCKEN-H is asserted.

CRCK-H: CRC Results for the Key, referred to as frame 7, are reported to the state machine via this bit.

CRCL-H: CRC Latched is a memory bit that indicates whether or not any CRC error has occurred within the block being read. This is used during the Verify mode so that all errors within a block will be detected before the process is interrupted.

CRCMR-H: CRC Master Reset allows the state machine to clear the CRC Generator/Checker at the appropriate time to assure valid operation.

CRCN0-H: CRC Not Zero indicates that the CRC Generating and Checking Register does not currently contain all (sixteen) zeroes. If this occurs at the end of a frame during a Read, it indicates that an error has been detected.

CRCNF-H: CRC Not Found is a memory bit that indicates, primarily to the state machine, that a valid Key has not yet been found for the block currently being read. If the Key CRC shows an error, an attempt will be made to recover a valid Block Number from the first four data frames. (There is no point in looking further as the data would show unrecoverable errors anyhow so the Block Number would be irrelevant.)

CS0-L,CS1-L: Chip Selects to the lower and upper buffer RAMs are generated directly by the state machine. Ordinarily only one of these will be active (low) at a time, but while generating Error Correction Frames on a Write to the Tape or when Error Correction is invoked during a Read to the DMA, both RAMs will be selected.

CSTROBE-H: Command Strobe is used to strobe the contents of the Command Register at Address 8 to the Drive Module. When it is necessary, the state machine will generate an FCSTR-H signal in order to transmit a Stop Motion Command to the Drive, but ordinarily CSTROBE results from the microprocessor setting bit 0 of Address 10 (ten). For timing requirements, see the reference at Section 2.3.1.

CSX: Shorthand notation for referring to both CS0 and CS1 at the same time.

CTC: The Counter/Timer Chip is located on the microprocessor assembly and is used to count data blocks on the tape or to time gaps.

CTCO: Output from the CTC is latched for use as a branch condition by the state machine.

CTCT-H: Counter-Timer-Chip Trigger is produced by the state machine to run a block count to zero during Seek and Verify Modes, or to begin running the timer for Write operations.

CWE-L: Check Word Enable is normally at a logical low to allow the Cyclic Redundancy Check Generator to perform the feedback shift register function to produce the two-byte check word. When raised to a logical one state, the feedback is inhibited and the check word is shifted out to be appended to the data stream.

D0-H thru D7-H: This is the eight-bit bi-directional Data Bus between the TIB and the microprocessor.

DC600HC: 3M Company's name for their High Capacity (due to High Coercivity) 600-foot Data Cartridge.

DC615HP: Same Data Cartridge as the DC600HC but only 150 feet long and only available to HP and its customers.

DGND: Digital Ground is the return path for Logic Power (VCC = +5v) and for Analog Power = +12v.

DIN-H: Data In to the DMA from the TIB is tri-stateable.

DMAC-H: DMA Connect is set high through the Command Register at Address 8 to connect the TIB to the DMA. DMAC should be low when another device, such as the system disc, is connected to the DMA.

DMAEN-H: DMA Enable from the state machine is set high to select the 9.6-MHz RWC as the clock for data transfer between the TIB and the DMA.

DOUT-H: Data Out of the DMA to the TIB is latched on the falling edge of RWC-H.

DRNW-H: Drive Read / Not Write will normally be high, in order to read keys or data from the tape, and drops low only when writing data and the associated gaps to the tape. For details see Reference at Section 2.3.1.

DTOF-L: DMA To Formatter/Separator mode is decoded by a PROM and used to select the proper BSOD for a DMA transfer to the TIB.

ECC: Industry standard abbreviation for Error Correction Code. The ECC used in the HCD-7S is a fifty-percent redundancy code using exclusive-ORing to restore very long dropouts. The disc that may be associated with the TIB through a common DMA and microprocessor may use as an option another ECC board that implements a Fire Code which is more powerful in terms of the number of check bits required but will only correct short bursts (twelve bits at present) of data errors. The TIB ignores the Fire Code circuitry, if present, but always adds extra time to DMA transfers to allow for the appended check bits.

F0-H: This is a pseudo-frame counter bit, derived from the byte counter; one bit more significant than B7-H. When high, it signifies that a user data portion of the buffer RAM is being addressed. When at a logical low condition, the corresponding RAM locations will contain Header or CRC information, or dummy fields for Sync, ECC (DMA variety, Fire Code, is not used) or spare timing slots for DMA overhead.

F1-H thru F3-H: Encoded Frame selector outputs from the state machine. Though the frames on the tape are labelled from one to six in each block, internally the TIB refers to frames zero through three as user data, frames four and five as ECC fields, and the Key Mark is read as if it was frame seven, frame six being unused.

FALSE-L: This is the summation of all conditions that may be tested by the state machine after it has been latched. When it is low on the proper clock edge, a jump will occur in the addressing sequence to the PROMs, giving a Jump-If-Test-False capability.

FCSTR-H: Formatter/Separator-generated Command Strobe is used to send only Stop Motion commands to the drive when appropriate.

FIDAT-H: Formatter/Separator Input Data is the result of latching DOUT-H from the DMA. It will be right-shifted into the SERDES registers for storage in the buffer RAM.

FODAT-H: Formatter/Separator Output Data has been exclusive-ORed as necessary from the SERDES and will be latched for transmission to the DMA.

FOUT-L: Formatter/Separator Output is the latched form of FODAT-H before it is three-state buffered to become DIN-H to the DMA.

FTOD-L: Formatter/Separator To DMA mode has been decoded by the PROM and is used to select the proper timing mark for BSOD-L.

GAP-L: When at a logical low level, this signifies the absence of data coming from the tape drive. This is assumed if no transitions of either polarity have been detected in the MFM pattern in approximately four bit times.

GAPX-H, GAPX-L: Gap Extended is derived from GAP-L by filtering out, digitally, any data bursts shorter than sixteen bits. This allows the state machine to ignore sporadic transitions caused by such things as turning the erase current on and off at the tape heads.

GTO-L: Go To Zero may be activated by a Master Reset, Restart from the Command Register at Address 9 or by a Drive Fault. It forces the state machine to return to its idle state at address zero.

HCD-75: The model name used by the 3M Company for their High Capacity Drive that would have stored 75-Mbytes on a 600-foot tape but was downgraded to 67-Mbytes to accomodate a binary number (4096) of records per track.

HINST-H: Header Insert goes high to convert the header information stored in the lower RAM for the first two frames to headers valid for the two ECC frames.

IFLG-H: Interrupt Flag is examined by the microprocessor to detect a request by the TIB for service in a polled system. It is a direct state machine output.

INSRT-H: Insert is the alternation of HINST-H and SYNC1-H which bits are ORed into the data stream at proper times for writing to the tape.

JAM-H: Jam a Stop Motion Command to the Drive is an output from the state machine used to disable the three-stateable Command Register at Address 8 which is set by the microprocessor.

JAM-L: The inverse of JAM-H, this signal enables the hexadecimal 3D, Stop Motion, Command to the HCD-75 Drive.

KYEXP-H: Key Expected is generated by masking out all gaps except the one immediately prior to the Key Mark preformatted on the DC600-series tapes. It is used in locating position before a read or write can occur and its occurrences are counted during Seeks to locate a specific block.

LAMP1-H: This signal is current-limited to drive an LED which is used to indicate that the cartridge currently in the tape drive is Protected against accidental writing.

LAMP2-H: Similar to LAMP1, but this indicator signals to the user that the drive is Busy.

LDAB-L: Load the A/B counters is a request from the state machine to load the bit and byte counters on the next edge of the ABCLK. The value to be loaded depends upon which of the three possible clocks are assigned to ABCLK.

LDCRC-L: Load CRC result into the CRC Flag Register at Address 5 and the CRCL latch.

LOCKUP-L: Occurs four bytes into the sync field on a read from the tape indicating that the phase-locked loop should have acquired lock onto the signal coming from RDDATA.

LOHS-H: Loss Of Handshake is set by the state machine as status to the microprocessor indicating that the processor has failed to read the previous key number prior to the discovery of the current key number on the tape being read.

M0-H, M1-H, M2-H: These Mode select bits are set by the processor into Command Register 9 and become the instruction to be executed by the state machine. The three bits are decoded to select one of the six modes--Write DMA to TIB buffers only, Write DMA to Tape, Read Tape into TIB buffers, Read from TIB to DMA, Verify N-blocks, or Seek N-blocks from current position.

M3-H: An additional mode select bit being used to select between drives in a system having two HCD-75's connected to one TIB.

MFM: Modified Frequency Modulation is the self-clocking method of encoding data to be stored on tape by the HCD-75.

MOUT-L: Mode is Output-type from the TIB, that is data is being transmitted from the TIB either to the DMA or to the tape.

MRST-L: Master Reset is provided by the Power Supply assembly to bring control registers up in a predictable condition.

NEWKEN-H: New Key Enable is output by the state machine to allow the passing of RDATA into the Key Number Registers at Addresses 2 and 3.

NEWKY-H: New Key is a latched bit indicating to both the state machine and the microprocessor that the value stored in the Key Number Registers (Addresses 2 and 3) has not been read by the processor. The processor reads this flag as the most-significant bit of Register 2. Failure of the controlling processor to read this bit prior to finding the next Key Mark results in LOHS.

OSEL0-L, OSEL1-L: Output Select lines chose between the two fourteen-bit output latches into which the PROM contents are stored to become control bits. Ordinarily only one of these will be active (low) at a time.

PCA: Standard terminology for Printed Circuit Assembly, a PCB that has been loaded with components.

PCB: Printed Circuit Board, an empty one holding no components.

PCTC-H: Pulse from the CTC is the result of latching CTC0-H to be used as a state machine qualifier.

PLL: Phase Lock Loop is a voltage controlled oscillator that outputs clock pulses whose period and phasing vary to track incoming data from a tape that is not moving at a perfectly constant speed.

PROM: Standard abbreviation for Programmable Read Only Memory. PROMs are used on the TIB for state machine control memory, for mode decoding and for pattern precompensation during writing to the tape. This allows easy updates and expansion for unforeseeable changes in production, changes in product definition or for bootstrapping into new products.

RAM: Standard acronym for Random Access Memory, also known as Read-Write Memory. The TIB uses two 2048-byte RAMs for speed-matching buffers between the slow tape and fast DMA.

RCCOD-L: Read Completion Code Register is the result of RD-L occurring at Address 4.

RCFLG-L: Reset the CRC Flag Register at Address 5.

RCLK-H: Read Clock is the bit-rate clock extracted from the self-clocking MFM data pattern by the phase-lock loop

RCRCF-L: Read the CRC Flag Register at Address 5 as status to the microprocessor.

RDATA-H: Read Data is data from the tape after it has been MFM decoded and separated from the sync field by the Read/Write circuitry.

RDDATA-H: This version of Read Data is the original output, still MFM-encoded, as it comes from the HCD-75 to the TIB.

RDDATB-H: Read Data (RDDATA) after it has been buffered by a Schmitt-triggered device.

RDST-L: Read Drive Status to the processor via Address 0.

REN-H: Read Enable is a state machine output bit that selects RCLK as a source for ABCLK, RDATA for CRCD and the proper value to be loaded by LDAB.

RESET-H: This is the line that is used by the processor to initiate the drive's autoload sequence.

REVNO-L: Read Revision Number Register 6 at which location the processor can find the Artwork Revision Number (upper four bits), the Rework Number (next two lower bits) and a copy of GAPX-L in the least-significant bit position.

RIF-L: Read Interface Status at Address 1 which contains the IFLG, SW0 through SW3, the Sector Toggle flag, and CACKN and SSTROBE from the HCD-75.

RKNL-L: Read Key Number Lower byte at Address 3. This operation results automatically in a clearing of the NEWKY-H flag.

RKNM-L: Read Key Number More-significant byte at Address 2 at which location also are copies of NEWKY-H and CRCNF-H which indicate the validity of the contents of the Key Number Register pair.

RNWEN-H: Read/Not Write Enable is the buffered version of DRNW that controls the HCD-75 tape drive recording circuitry.

ROMEN-L: ROM Enable is normally low to activate the state machine and mode select PROMS but may be put at a logic high level, through a pull-up resistor and inverter, to disable these PROMS for testing.

RWC-H: Read/Write Clock is a 9.6-MHz timing signal used in the transmission of data between the TIB and DMA.

RWC-L: This inverted form of RWC-H is the clock actually sent to the DMA by the TIB.

RWCB-H: This is the free-running version of the Read/Write Clock before it is gated by DMAEN-H as it has been appropriately phased with respect to SCLK to allow DMA data to pass at a bit rate twice that of the state machine without getting out of control.

SADAT: The Egyptian who made peace with the Israelis.

SADAT-H: Signature Analysis Data is the central node in the state machine qualifier feedback loop which can be monitored by an HP5004A or other Signature Analyzer for a quick debug of the control portion of the TIB. When latched in normal operation, this becomes FALSE-L to implement jumps within the PROM space.

SAEN-L: Signature Analysis Enable when brought to a logic low level will disable FALSE-L thereby breaking the feedback loop on the state machine so that no jumps will occur. This results in a repeatable cycle through the PROM addresses with a likewise repeatable, if meaningless, sequence of signals throughout the TIB which can be used for testing components at their normal operating frequencies. Note: This line must never be low when a tape drive is connected to the TIB, as it may result in damage of the preformat on an installed data cartridge.

SASS-H: Signature Analysis Start/Stop can be used to trigger an HP5004A or equivalent instrument for testing the TIB at device operating speeds. This is the most-significant bit of the state machine's address counter.

SCLK-H: State Clock in the active high form is a 4.8-MHz clock, high for approximately 156-nsec and low for 52-nsec, 75% duty cycle, which drives the address counter to the state machine PROMs.

SCLK-L: State Clock in the active low condition is logically the inverse of SCLK-H and is used to latch SADAT-H to generate FALSE-L for conditional jumps within the state machine, as well as to latch the PROM outputs into one of the control registers in response to OSEL0 or OSEL1.

SERDES: Conjunction for Serializer/De-serializer. In the TIB a Universal Shift Register, that is, bi-directional and serial or parallel in or out, is used to convert a serial data stream for retrieval from or storage into the byte-parallel buffer RAMs.

SNUKY-L: Set New Key is a state machine output bit that sets the NEWKY latch to indicate that either a valid key number has been found or the key number cannot be found and that the best guess is stored in the Key Number Registers 2 and 3.

SOD-L: Start-of-Data is generated by decoders off of the bit/byte counter to indicate that header information will be sent to or received from the DMA immediately following the proper number of dummy bits, three for a write to the TIB and five for a read to the DMA. SOD occurs a minimum of twelve bits later than SOS-L. SOD-L is a three-stateable version (by means of DMAC) of SOD-H which in turn is a latched form of BSOD-L.

SOS-L: Start-of-Sector is derived from LDAB-L to initialize the DMA circuitry to begin receiving RWCs from the TIB. This will be followed by SOD-L at the appropriate time and then by data. At the end of a block transfer of four sectors, an extra SOS-L is sent to the DMA to satisfy its requirements. SOS-L is an inverted three- stateable form of SOS-H and can be disabled using DMAC to allow another device such as a disc to use the same DMA interface bus.

SRS0-H, SRS1-H: Shift Register Selects are produced by the mode decoding PROM to control the loading, holding and shifting of the universal shift registers used in the SERDES.

ST00-H thru ST07-H: Status from the HCD-75 Drive which is buffered and read by the microprocessor through Register 0.

STEST-H: Self-Test is one of the bits in the TIB control register at Address 9 which can be set by the processor to select among a set of special test modes. This control bit is copied into the Completion Code Register at Address 4 to signify that the register contains self-test information rather than ordinary completion conditions.

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STOG-H: Sector Toggle is derived from SOS-H, simply toggling on each occurrence. This signal is used to stretch SOS-H to a low enough rate that the microprocessor can follow it, counting out the number of sectors that have been transferred.

SUCCS-H: Successful Completion is one of the completion codes set by the state machine into Register 4 to indicate to the processor that the requested operation has terminated without status level error conditions, though there may have been data errors.

SYNC1-H: This is the signal that is ORed into the data stream during a write to the tape to terminate the sync field of forty-seven zeroes followed by a single one-bit.

TIB: Acronym used in this document to refer to the Tape Interface Board.

TIBS-L: TIB Select is decoded from bits 6 through 15 of the microprocessor's address bus on the Processor Assembly. Since bits 4 and 5 of that bus are neither decoded by the processor or on the TIB, these two bits are logically "don't cares", resulting in multiple "virtual" copies of the ten TIB registers.

TSTCK-H: Test Clock is the buffered 9.6-MHz crystal-controlled clock which is brought to an edge-connector for real-time testing of the read/write circuitry.

TSTEN-L, TSTEN-H: Test Enable in the active low form is normally pulled high; but can be brought to a logic low condition via the TSTEN-L pin at the edge-connector for test purposes. In this state TSTEN-H serves to disconnect REN-H, RDDATB-L, WEN-H and WDATA-H from the read/write circuitry so that this portion of the TIB may be tested separately.

VCO-H: Voltage-Controlled Oscillations resulting from the phase-lock loop will track RDDATA-H from the tape, during a read from tape operation, in order to produce RCLK-H. A half-rate VCO signal is fed back to the phase detector once lock has been achieved in order to maintain that lock on data.

VERR-H: Verify Error is output by the state machine in response to CRCL-H at the end of any block in which a CRC error, whether in data or key mark, was detected during a Verify operation. The drive will be sent a Stop Motion command so that the microprocessor may examine the CRC bits before attempting a retry.

VFY-L: Verify N Blocks mode has been selected when this line is low.

WCKEN-H: Write Clock Enable is a state machine output used to select WCLK-H as the source for ABCLK-H. This is done not only during write to tape operations, but also during periods when the state machine uses the low frequency (600-kHz) crystal-controlled WCLK-H as a timer in order to anticipate the duration of gaps.

WDATA-H: Write Data is the composite of sync field, header, user data and CRC bytes as sent to the MFM encoder to be converted before being written to the tape.

WDDAT-H: Write DData (the stuttering is necessary) is the result of inserting header bits and sync field into the data stream taken from the RAM. This is fed to the CRC Generator.

WEN-H: Write Enable is a control line generated by the state machine to enable the write encoder during a write to tape operation.

WR-L: The Write pulse from the microprocessor is used to latch the contents of the data bus into one of the three command registers on the TIB.

WRDATA-H: Write Data is the buffered version of WRDATB-H as it appears at the ribbon cable going to the drive.

WRDATB-H: Write Data (before being) Buffered is the MFM-encoded form of WDATA-H which will be buffered and sent to the drive to be written onto the tape.

ZCNT-H: Zero Count is a status bit set by the state machine to indicate to the microprocessor that either a Seek or a Verify operation has terminated by virtue of the CTC block counter having been decremented to zero at the target block.

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60241 07908-66241
07908-68241
07908-67241

DATE CODE : F-2336

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C100	0160-5298	CAP .01UF 20%
C105	0160-5298	CAP .01UF 20%
C110	0160-5298	CAP .01UF 20%
C113	0160-5311	CAP 330PF 5%
C115	0160-5298	CAP .01UF 20%
C120	0160-5298	CAP .01UF 20%
C125	0160-5298	CAP .01UF 20%
C130	0160-5298	CAP .01UF 20%
C135	0160-5298	CAP .01UF 20%
C140	0160-5298	CAP .01UF 20%
C145	0160-5298	CAP .01UF 20%
C150	0160-5298	CAP .01UF 20%
C160	0160-5298	CAP .01UF 20%
C165	0160-5298	CAP .01UF 20%
C170	0160-4002	CAP .22UF 10%
C175	0160-5298	CAP .01UF 20%
C180	0160-5298	CAP .01UF 20%
C185	0160-5298	CAP .01UF 20%
C205	0160-5298	CAP .01UF 20%
C210	0160-5298	CAP .01UF 20%
C215	0160-5298	CAP .01UF 20%
C225	0160-5298	CAP .01UF 20%
C230	0160-5298	CAP .01UF 20%
C235	0160-5298	CAP .01UF 20%
C240	0160-5298	CAP .01UF 20%
C245	0160-5298	CAP .01UF 20%
C249	0160-5298	CAP .01UF 20%
C250	0160-5298	CAP .01UF 20%
C255	0160-5298	CAP .01UF 20%
C260	0160-5298	CAP .01UF 20%
C265	0160-5298	CAP .01UF 20%
C270	0160-5298	CAP .01UF 20%
C275	0160-5298	CAP .01UF 20%
C285	0160-5298	CAP .01UF 20%
C300	0160-5298	CAP .01UF 20%
C305	0160-5298	CAP .01UF 20%
C310	0160-5298	CAP .01UF 20%
C320	0160-5298	CAP .01UF 20%
C325	0160-5298	CAP .01UF 20%
C330	0160-5298	CAP .01UF 20%
C340	0160-5298	CAP .01UF 20%
C345	0160-5298	CAP .01UF 20%
C350	0160-5298	CAP .01UF 20%
C360	0160-5298	CAP .01UF 20%
C365	0160-5298	CAP .01UF 20%
C375	0160-5298	CAP .01UF 20%
C380	0160-5313	CAP 1000PF 5%

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60241 07908-66241
07908-68241
07908-67241

DATE CODE : F-2336

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C385	0160-5313	CAP 1000PF 5%
C390	0160-5298	CAP .01UF 20%
C395	0160-5298	CAP .01UF 20%
C397	0160-5298	CAP .01UF 20%
C399	0160-5298	CAP .01UF 20%
C412	0160-5298	CAP .01UF 20%
C420	0160-5298	CAP .01UF 20%
C422	0160-5298	CAP .01UF 20%
C424	0160-5298	CAP .01UF 20%
C426	0160-5298	CAP .01UF 20%
C426	0180-2207	CAP 100UF 10%
C432	0160-5298	CAP .01UF 20%
C434	0160-5298	CAP .01UF 20%
C438	0160-5298	CAP .01UF 20%
C442	0180-0374	CAP 10UF 10%
C444	0160-5298	CAP .01UF 20%
C446	0160-5298	CAP .01UF 20%
C448	0160-5298	CAP .01UF 20%
C450	0160-5316	CAP 4700PF 20%
C452	0160-5298	CAP .01UF 20%
C454	0160-5312	CAP 470PF 5%
C456	0160-5311	CAP 330PF 5%
C460	0160-5312	CAP 470PF 5%
C462	0160-5298	CAP .01UF 20%
C464	0160-5316	CAP 4700PF 20%
C466	0160-5310	CAP 220PF 5%
C468	0160-5298	CAP .01UF 20%
C470	0160-52[illegible]	CAP .01UF 20%
C472	0160-5310	CAP 220PF 5%
CR492	1901-0033	RECTIFIER SIL
J1	1251-5647	CONN 10-PIN M
L435	9100-1788	CHOKE-WIDE BAND
MP1	07908-80241	ETCHED-BD-TIB
MP2	7120-6830	LABEL-INFO
MP4	1480-0116	PIN GRV .062X.25
MP5	1251-5595	PLZG KEY
MP6	0403-0456	EXTR-PC BD #6
R118	1810-0280	NTWK RES 9X10K
R128	1810-0275	NTWK RES 9X1K
R152	0757-0401	RES 100 1%.125
R154	0757-0401	RES 100 1%.125
R158	1810-0275	NTWK RES 9X1K
R168	0757-0467	RES 121K 1%.125
R188	0757-0467	RES 121K 1%.125
R222	1810-0280	NTWK RES 9X10K
R248	1810-0275	NTWK RES 9X1K
R328	1810-0275	NTWK RES 9X1K

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60241 07908-66241
07908-68241
07908-67241

DATE CODE : F-2336

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R368	1810-0280	NTWK RES 9X10K
R386	0698-3156	RES 14.7K 1%.125
R388	0698-3156	RES 14.7K 1%.125
R418	1810-0275	NTWK RES 9X1K
R436	1810-0280	NTWK RES 9X10K
R458	1810-0275	NTWK RES 9X1K
R476	0698-3156	RES 14.7K 1%.125
R478	0698-3156	RES 14.7K 1%.125
R480	0698-3156	RES 14.7K 1%.125
R482	0698-3156	RES 14.7K 1%.125
R484	0757-0438	RES 5.11K 1%.125
R490	0757-0438	RES 5.11K 1%.125
R494	0757-0447	RES 16.2K 1%.125
R498	0757-0443	RES 11K 1%.125
U1101	1816-1550	IC-MEM 1K BIT
U1102	1820-0681	IC SN74S00N
U111	1820-2641	IC SN74LS374N
U1111	1820-1112	IC SN74LS74N
U1112	1820-2016	IC 9401PC
U112	1820-2024	IC SN74LS244N
U1121	1820-1423	IC SN74LS123N
U1122	1820-1430	IC-SN74LS161N
U121	1820-2024	IC SN74LS244N
U122	1820-1196	IC SN74LS174N
U131	1820-2024	IC SN74LS244N
U141	1820-2024	IC SN74LS244N
U142	07908-89072	PROM TIB
U152	1820-1858	IC SN74LS377N
U161	1820-1677	IC SN74S374N
U162	1820-1858	IC SN74LS377N
U171	1820-2024	IC SN74LS244N
U172	1820-1240	IC SN74S138N
U182	1820-1208	IC SN74LS32N
U191	1820-1144	IC SN74LS02N
U192	1820-1199	IC SN74LS04N
U2101	1820-1321	IC SN74S85N
U2102	1820-0693	IC SN74S74N
U211	1820-1470	IC SN74LS157N
U2111	07908-89074	PROM-MEMORY
U2112	1820-1453	IC SN74S163N
U212	1820-1432	IC SN74LS163N
U2121	1820-1433	IC SN74LS164
U2122	1820-1453	IC SN74S163N
U2132	1820-0681	IC SN74S00N
U221	1820-1729	IC SN74LS259N
U222	1820-1432	IC SN74LS163N
U232	1820-1432	IC SN74LS163N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60241 07908-66241
07908-68241
07908-67241

DATE CODE : F-2336

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U241	07908-89073	PROM TIB
U242	1820-1240	IC SN74S138N
U251	1820-1858	IC SN74LS377N
U252	1820-1216	IC SN74LS138N
U261	1820-1858	IC SN74LS377N
U262	1820-1206	IC SN74LS27N
U271	1820-1197	IC SN74LS00N
U272	1820-0694	IC SN74S86N
U281	1820-1210	IC SN74LS51N
U282	1820-1199	IC SN74LS04N
U291	1820-0688	IC SN74S20N
U292	1820-0693	IC SN74S74N
U3101	1820-1208	IC SN74LS32N
U3102	1820-1197	IC SN74LS00N
U311	1820-1302	IC SN74S251N
U3111	1820-1204	IC SN74LS20N
U3112	1820-1210	IC SN74LS51N
U312	1820-1730	IC SN74LS273N
U3121	1820-0694	IC SN74S86N
U3122	1820-1430	IC-SN74LS161N
U3131	1820-1433	IC SN74LS164
U3132	1820-1282	IC SN74LS109N
U321	1820-1302	IC SN74S251N
U322	1820-1112	IC SN74LS74N
U331	1820-1302	IC SN74S251N
U332	1820-1201	IC SN74LS08N
U341	1820-1302	IC SN74S251N
U342	1820-1112	IC SN74LS74N
U351	1820-1430	IC-SN74LS161N
U352	1820-1430	IC-SN74LS161N
U361	1820-1430	IC-SN74LS161N
U362	1818-1611	IC-MEMORY
U371	1820-0693	IC SN74S74N
U381	1820-1144	IC SN74LS02N
U382	1820-3104	IC 74ALS299
U391	1820-1423	IC SN74LS123N
U392	1820-1199	IC SN74LS04N
U4101	1820-1112	IC SN74LS74N
U4111	1826-0519	TL 071
U4112	1820-2369	IC SN74LS629N
U422	1820-2075	IC SN74LS245N
U431	1820-1987	IC AM74LS299N
U432	1820-1216	IC SN74LS138N
U441	1820-1987	IC AM74LS299N
U442	1820-1216	IC SN74LS138N
U451	1820-1568	IC SN74LS125N
U452	1820-1633	IC SN74S240N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60241 07908-66241
07908-68241
07908-67241

DATE CODE : F-2336

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U461	1818-1611	IC-MEMORY
U462	1820-0693	IC SN74S74N
U472	1820-1416	IC SN74LS14N
U481	1820-3104	IC 74ALS299
U482	1820-0693	IC SN74S74N
U491	1820-1282	IC SN74LS109N
U492	1820-1112	IC SN74LS74N
VR496	1902-0048	DIODE BD 6.81V
X2111	1200-0482	SOCKET 16 DIP LO
Y2131	1813-0223	CLOCK OSC19.2MHZ

END OF MATERIAL LIST.

ER48 D/H: 50A/50B/C6

/ hp /

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline). (L240)

LTR	REVISIONS	DATE	INIT	MF
A	As Issued	03-17-82	jr/HM	M
B	Revised per PC48-4726	04-12-82	js/JC	M
C	Revised per PC48-4887	07-09-82	sb/ML	M
D	Revised pre-comp change per PC48-6040	12-20-82	cr/JC	M
E	Revised per PC48-6082	02-16-82	jr/JC	M
F	Made "2249" Mandatory change per C0480143	08-02-83	db/JC	M
G	Made "2336" Change RFI Fix per C0480276	09-14-83	jr/JC	

E	48-6082	jr/JC	02-10-83	MODEL 7908	STK # 07908-69241
F	C0480143	db/JC	08-02-83	UPDATE/REVISION	
G		jr/JC	09-14-83	BY	DATE MAR 17, 1982
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 6
REVISIONS				SUPERSEDES	DWG # A-07908-69241-1

HEWLETT-PACKARD CO. hp

UPDATING AND REVISION PROCEDURE

07908-69241

This procedure contains instructions for modification of the Tape Interface Board (TIB), 07908-60141, 07908-69141, or 07908-60241 to version 07908-69241.

REFERENCES:

SML:	07908-68241	Untested PCA
	07908-66241	Reel
Dwgs:	F-07908-60241-1	Assembly Dwg.
	A-07908-60241-2	Debug Procedure
	A-07908-60241-3	PC Assembly Procedure
	D-07908-60241-50	Schematics
	D-07908-60241-60	Signature Schematics
	07908-80141	Tape Masters
	F-07908-80241-1	Assembly Drawing

ER48 D/H: 50A/50B/C6

HEWLETT-PACKARD CO. /hp/

PRODUCTION CHANGES FOR:

-60141	48-4176	New PC design for state machine
	48-4373	Mandatory Prom change (Rev. D)
	48-4536	Parts change to correct timing error.
	48-4637	Cut trace to eliminate RFI problem
	48-4251	Implement Rev. E board and change to 2K RAMs.
	48-4538	Changed the extractor handles to numbered ones.
-60241	48-4693	Changes two PROMs and adds two jumpers. (skew timing fix)
	48-4726	Change state machine PROMs, completion code and diagnostic 28 error, waiting for block.
	48-4887	Added capacitor to Rdata line to desensitize TIB against glitching drives.
	48-6040	Changed precompensation prom U2111. Improved margin for precompensation.
	48-6082	New Photo Revision: Eliminates Rework. State Machine change takes care of no data found for large media drop outs, Also remove 2 (20pin) IC sockets for reliability problem.
	C0480276	RFI Fix

E	48-6082	jr/JC	02-10-83	MODEL 7908	STK # 07908-69241
F	C0480143	db/JC	08-02-83	UPDATE/REVISION	
G		jr/JC	09-14-83	BY	DATE MAR 17, 1982
LT	P.C. #	APPR	DATE	APPD	SHEET # 3 OF 6
REVISIONS				SUPERSEDES	DWG # A-07908-69241-1

INTRODUCTION:

This article will provide information concerning the eligibilty of the TIB board for revision and also concerning the revisions themselves.

REVISABLE ASSEMBLIES:

The first assembly which may be revised is E-2137. All prior assemblies are to be scrapped.

REVISIONS:

```
E-2137        60141
E-2149
E-2151

-------------------

E-2206 E-2336 60241
E-2210
E-2221
E-2240
E-2249
F-2249
F-2336
```

CURRENT ASSEMBLY:

E,F-2336

PROCEDURE:

1. Inspect all boards for general mechanical and cosmetic defects per A-5950-9205-1. Repair all component malfunctions.

2. Identify all boards with the following logo;

   07908-69241
   2336

   to replace existing logo for date codes 2137 or later.

3. Affix, near the logo, a 7120-5480 label which is stamped with the month and year of final inspection.

4. On board revision: E-2137 (to get 2149) of 60141

   a) Replace U462 with 1820-0693.

   b) See Mod Dwg. for jumpers added.

5. On board revision: E-2149 (to get 2151) of 60141

   a) Drill out the feed through near U2132 (see Mod. Dwg.).

PROCEDURE: (Continued)

6. On board revision: E-2151 of 60141 (to get 2206) of 60241

    a) Replace U142 with 07908-89037.
    b) Replace U241 with 07908-89038.
    c) Unsolder pin 13 of U321 and lift the leg out of the hole.
    d) Run a jumper wire from the pin, through the empty hole, to U221-3. Put glue on the wire near the hole on the circuit side.
    e) Cut the trace coming from U331-2.
    f) Install a jumper from U331-2 to U271-8. Glue the jumper in place.

7. On board revision: E-2206 (to get 2210) of 60241

    a) Replace U142 with 07908-69063; U241 with 07908-89064.

8. On board revision E-2210 (to get 2221)

    a) Add 330P capacitor, see MOD Dwg. D-07908-60241-20, Rev C.

9. On board revision E-2221.

    a) Replace Prom U2111 with 07908-89074
    b) Inspect underneath sockets X362 and X461 for flux contamination.

10. On board revision E-2240.

    a) Replace U142 with 07908-89072 and U241 with 07908-89073.
    b) Remove sockets and solder PROMS in (2 places).

11. On board revisions E and F-2249

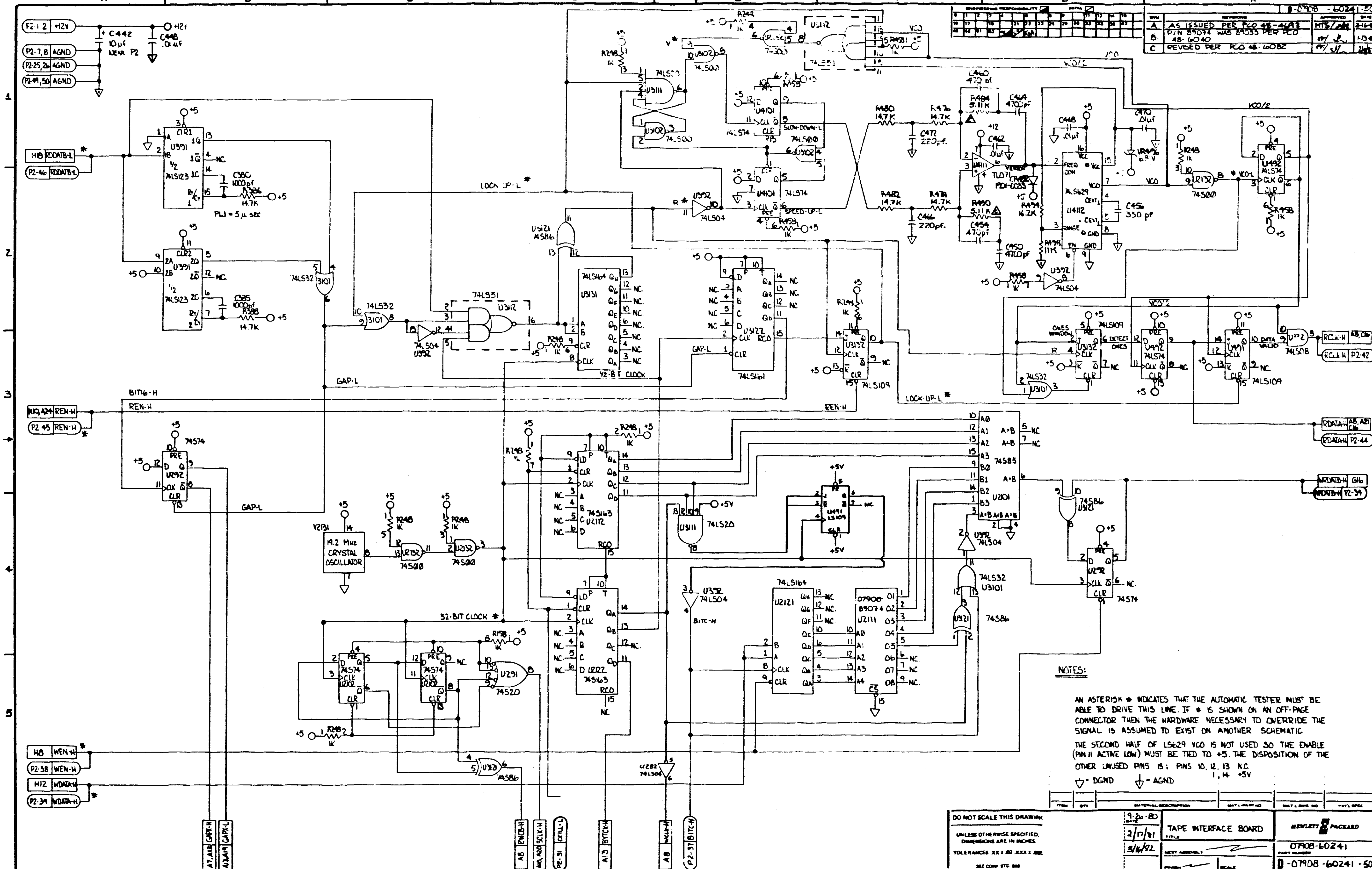
    a) On Rev F see Mod. Dwg. D-07908-60241-1
    b) On Rev E Remark E-2336

12. On board E and F-2336

    a) Current Revision

13. Test per A-07908-60241-2

E	48-6082	jr/JC	02-10-83	MODEL 7908	STK # 07908-69241
F	C0480143	db/JC	08-02-83	UPDATE/REVISION	
G		jr/JC	09-14-83	BY	DATE MAR 17, 1982
LT	P.C. #	APPR	DATE	APPD	SHEET # 6 OF 6
REVISIONS				SUPERSEDES	DWG # A-07908-69241-1



NOTES:

AN ASTERISK * INDICATES THAT THE AUTOMATIC TESTER MUST BE ABLE TO DRIVE THIS LINE. IF * IS SHOWN ON AN OFF-PAGE CONNECTOR THEN THE HARDWARE NECESSARY TO OVERRIDE THE SIGNAL IS ASSUMED TO EXIST ON ANOTHER SCHEMATIC.

THE SECOND HALF OF LS629 VCO IS NOT USED SO THE ENABLE (PIN 11 ACTIVE LOW) MUST BE TIED TO +5. THE DISPOSITION OF THE OTHER UNUSED PINS IS; PINS 10, 12, 13 N.C. 1, 14 +5V

▽ = DGND ⏚ = AGND

REV	REVISIONS	APPROVED	DATE
A	AS ISSUED PER PCO 48-4683	MTS	3-16-82
B	P/N 89094 was 89035 PER PCO 48-6040		1-13-83
C	REVISED PER PCO 48-6082		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

9-26-80 · 2/17/81 · 3/16/82

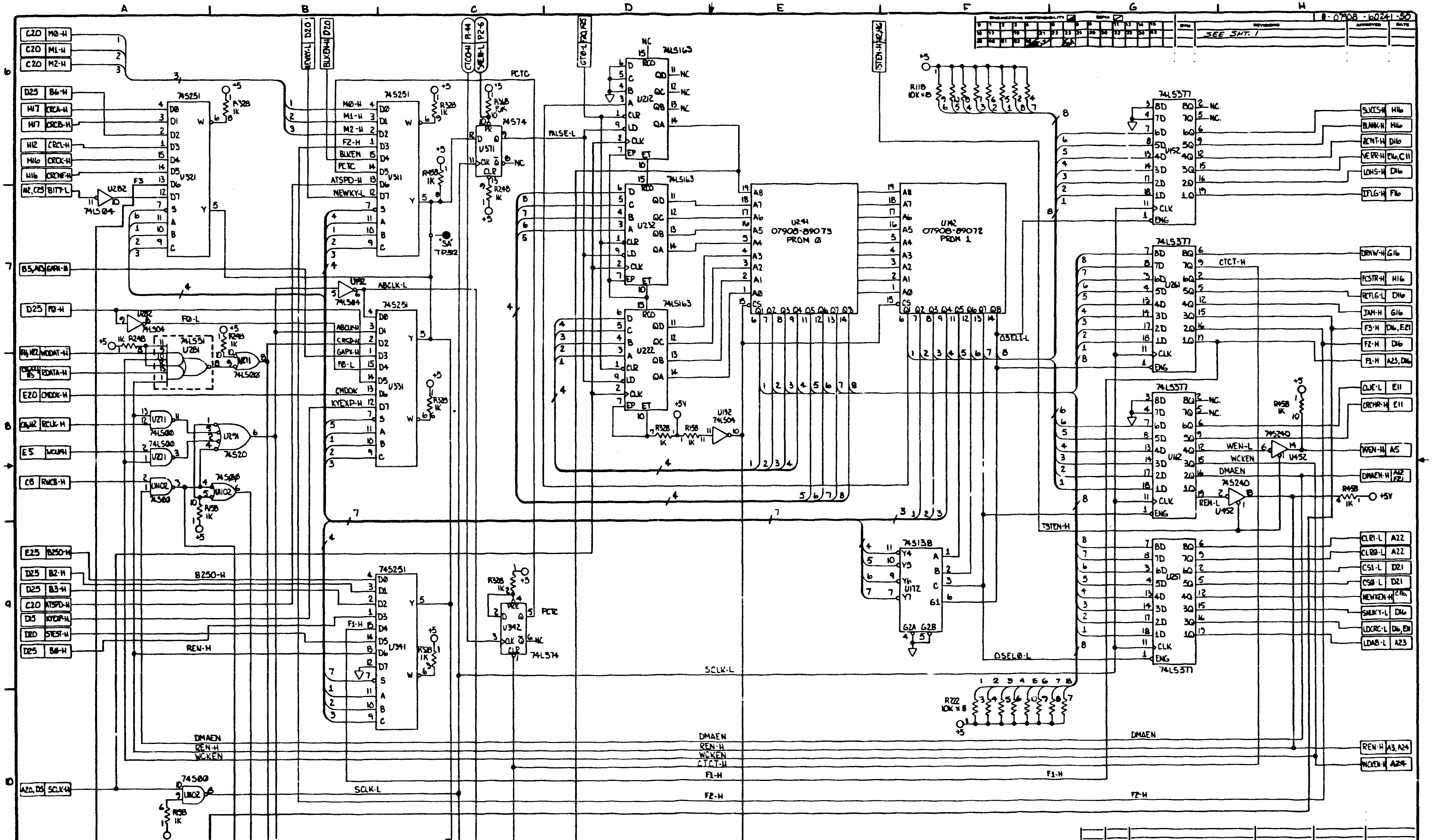
TAPE INTERFACE BOARD

HEWLETT PACKARD

07908-60241

D-07908-60241-50

SHEET 1 OF 3



SEE SHT. 1

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

9-25-80

2/17/81

3/16/81

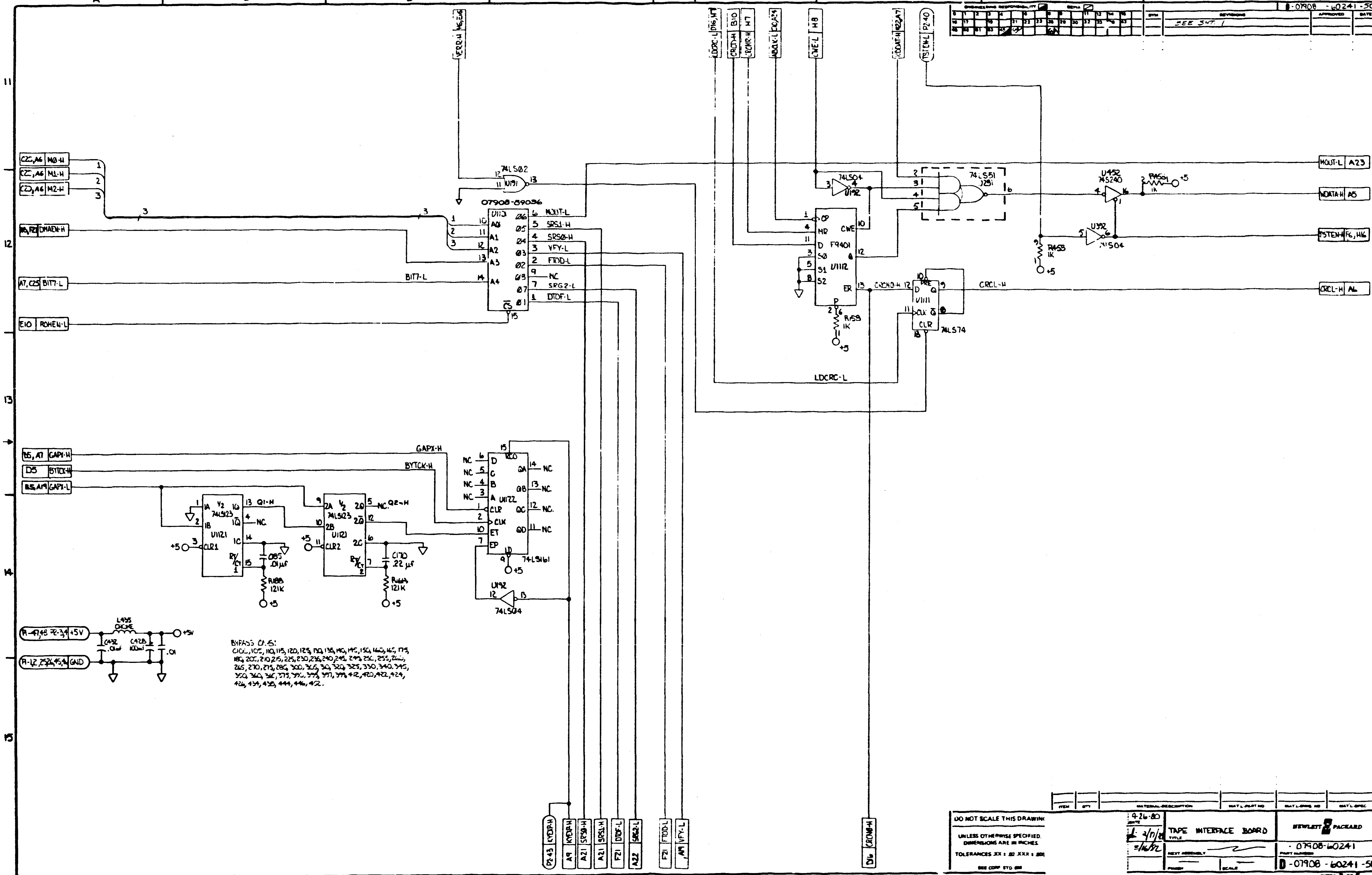
TAPE INTERFACE BOARD

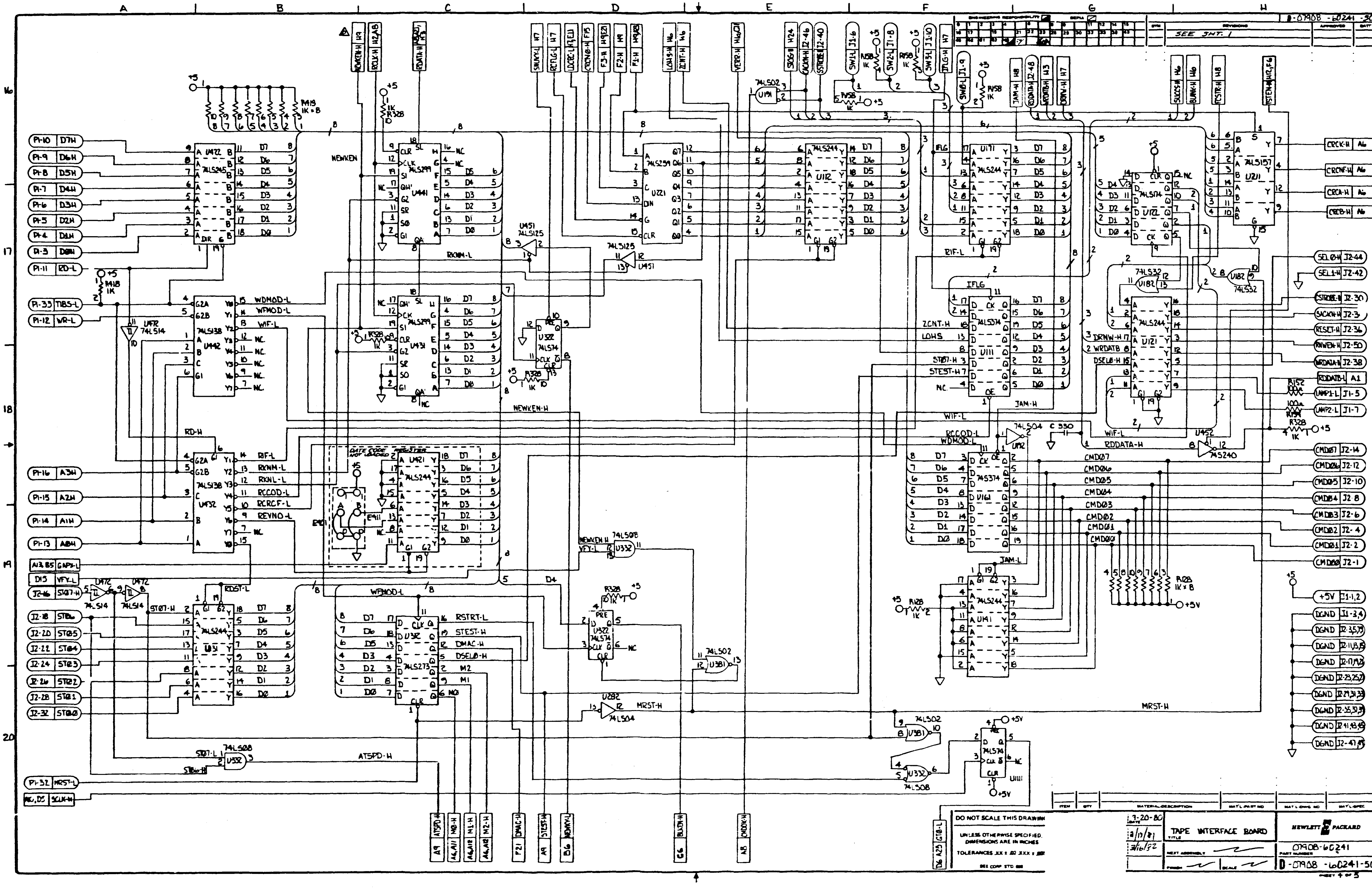
HEWLETT PACKARD

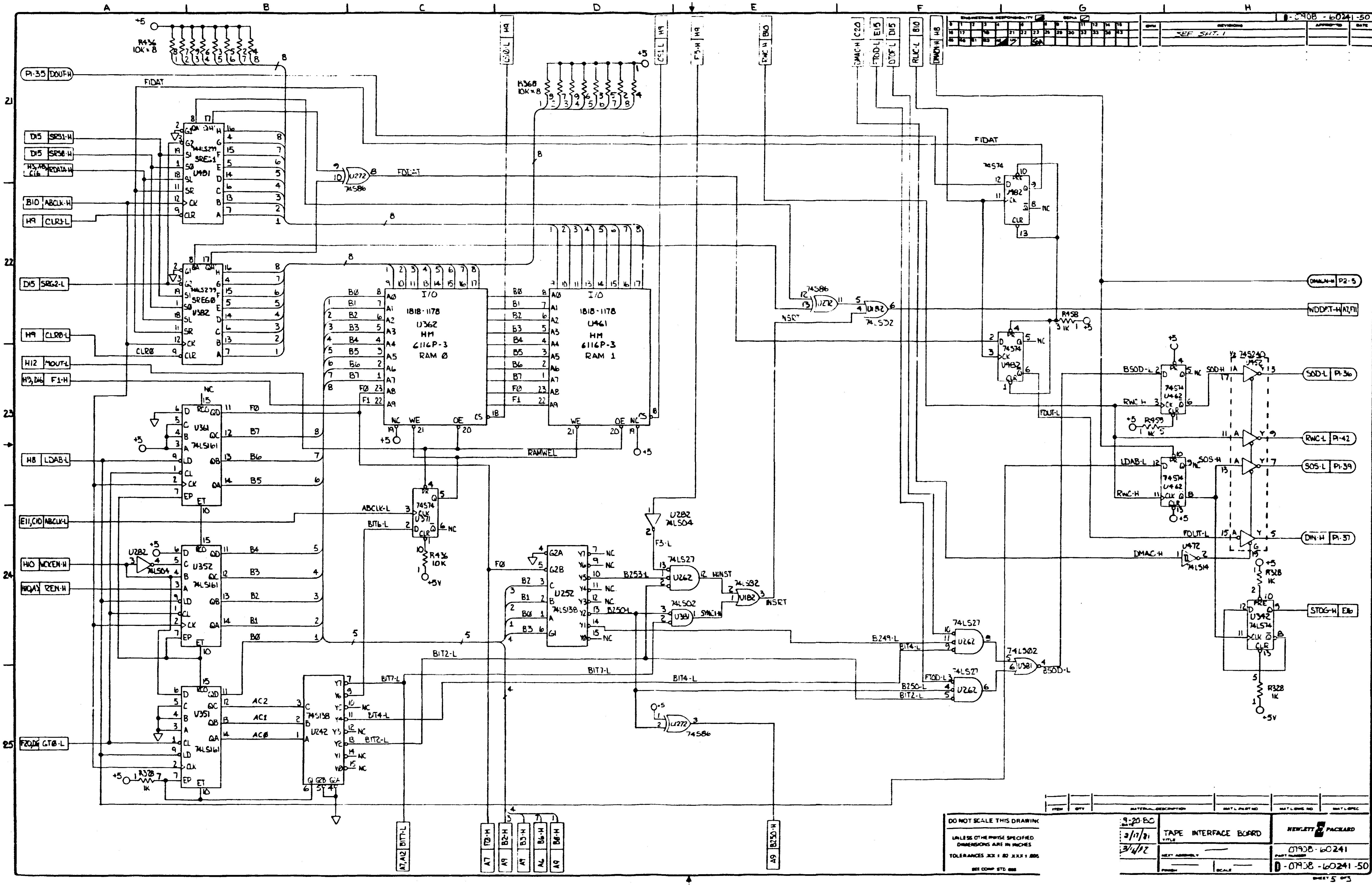
07908-60241

D-07908-60241-50

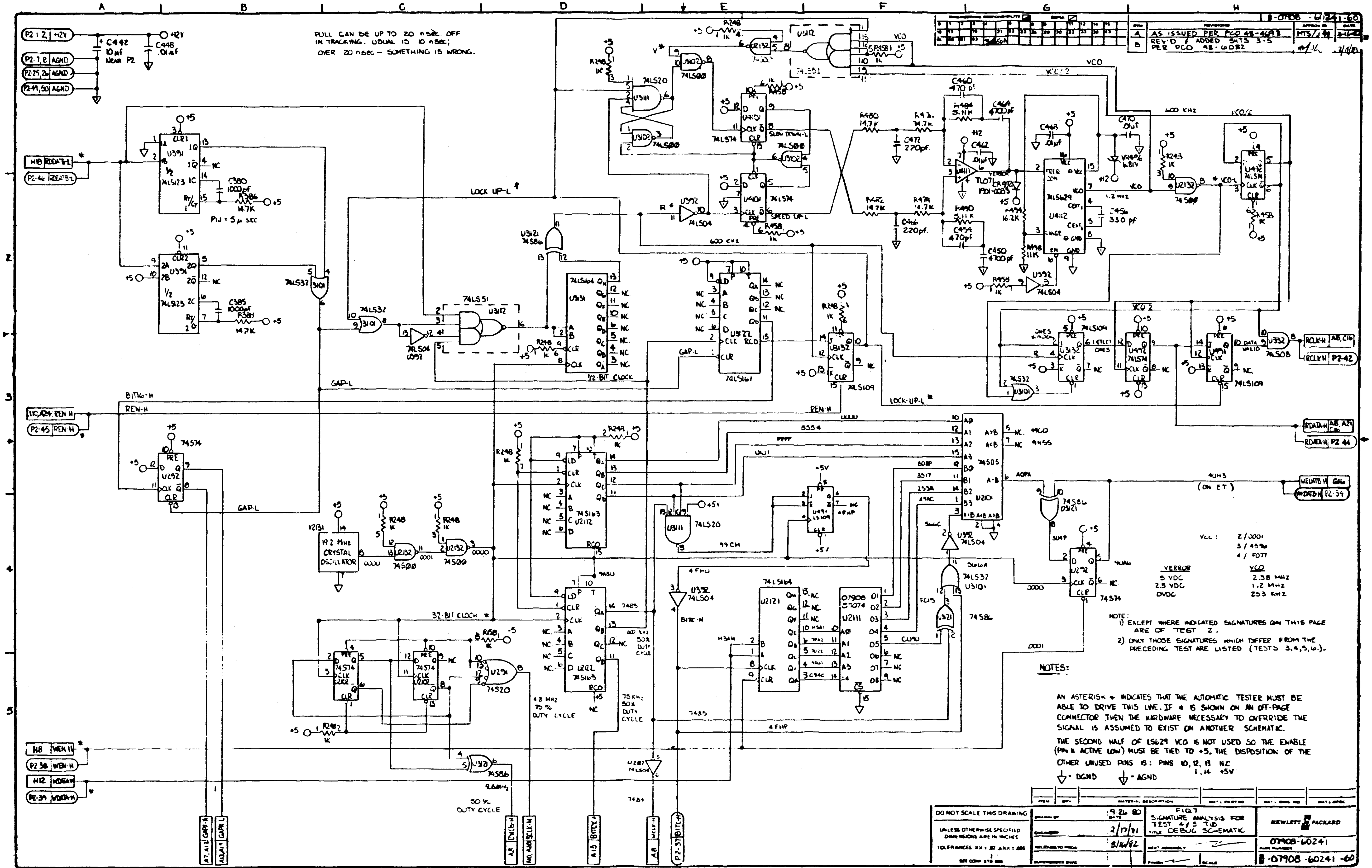
SHEET 2 OF 5


D-07908-60241-50
SEE SHT. 1
MOUT-L A23
NDATA-H A5
TSTEN-H F6, H16
CRCL-H A6
C2, A6 M0-H
C2, A6 M1-H
C2, A6 M2-H
DMAEN-H
A7, C25 BIT7-L
E10 ROMEN-L
B5, A7 GAPX-H
D5 BYTCK-H
B5, A19 GAPX-L
VERR-H
LDCRC-L D16, H7
CRCH-H B10
CRCMR-H H7
ABCLK-L
CWE-L H8
RDDAT-H
TSTEN-L P2-40
74LS02
U1191
07908-89056
U1113
MOUT-L
SRS1-H
SRS0-H
VFY-L
FTOD-L
NC
SRG2-L
DTOF-L
BIT7-L
74LS04
U1192
F9401
U1112
R459 1K
74LS51
U1291
U452
74S240
R450 1K
U392
74LS04
R453 1K
CRCHO-H
CRCL-H
74LS74
U1111
LDCRC-L
GAPX-H
BYTCK-H
Q1-H
Q2-H
1/2 74LS123
U1121
C085 .01µf
R188 121K
C170 .22µf
R463 121K
U1122
74LS161
U1192
74LS04
L435
C432
C428
+5V
GND
BYPASS CAPS:
C100, 105, 110, 115, 120, 125, 130, 135, 140, 145, 150, 160, 165, 175, 180, 200, 210, 215, 225, 230, 236, 240, 245, 249, 250, 255, 260, 265, 270, 275, 286, 300, 305, 310, 320, 325, 330, 340, 345, 350, 360, 365, 375, 390, 395, 397, 399, 412, 420, 422, 424, 426, 434, 438, 444, 446, 452.
KYEDP-H
A9 KYEDP-H
A21 SRS0-H
A21 SRS1-H
F21 DTOF-L
A22 SRG2-L
F21 FTOD-L
A9 VFY-L
D16 CRCHO-H
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
9-26-80
TAPE INTERFACE BOARD
HEWLETT PACKARD
07908-60241
D-07908-60241-50
SHEET 3 OF 3


SEE SHT. 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED. DIMENSIONS ARE IN INCHES
3-20-80
8/13/81
3/16/82
TAPE INTERFACE BOARD
HEWLETT PACKARD
07908-60241
D-07908-60241-50
SHEET 4 OF 5



D-07908-60241-50
SEE SHT. 1
TAPE INTERFACE BOARD
HEWLETT PACKARD
07908-60241
D-07908-60241-50
9-20-80
2/17/81
3/4/82
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
SHEET 5 OF 5
1818-1178
HM 6116P-3
RAM Ø
RAM 1
U362
U461
U481
U382
U361
U352
U351
U242
U252
U371
U262
U381
U182
U272
U282
U472
U462
U482
U342
U452
74LS279
74LS161
74LS138
74S74
74S86
74LS04
74LS27
74LS02
74S02
74LS14
74S240
R436 10K×8
R368 10K×8
R458 1K
R459
R328 1K
R378 1K
FIDAT
FDLAT
INSRT
RAMWEL
HINST
SYNCH
FDUT-L
FOUT-L
BSOD-L
SOD-H
SOS-H
DMAC-H
P1-35 DOUT-H
D15 SRS1-H
D15 SRS0-H
RDATA-H
B10 ABCLK-H
H9 CLR1-L
D15 SRG2-L
H9 CLR0-L
H12 MOUT-L
F1-H
H8 LDAB-L
E11,C10 ABCLK-L
H10 NCKEN-H
IREN-H
F20,D6 GTØ-L
CS1-L
CS0-L
F3-H
RWC-H
DMAC-H
FTOD-L
DTOF-L
RLIC-L
DMAEN-H
DMAEN-H P2-5
NDDPT-H A7,F11
SOD-L P1-36
RWC-L P1-42
SOS-L P1-39
DIN-H P1-37
STOG-H E16
BIT7-L
B250-H
B249-L
B253-L
B250-L
BIT4-L
BIT2-L
BIT6-L
F3-L
F0-H
B2-H
B3-H
B6-H
B8-H



NOTE:
1) EXCEPT WHERE INDICATED SIGNATURES ON THIS PAGE ARE OF TEST 2.
2). ONLY THOSE SIGNATURES WHICH DIFFER FROM THE PRECEDING TEST ARE LISTED (TESTS 3,4,5,6.).

NOTES:

AN ASTERISK * INDICATES THAT THE AUTOMATIC TESTER MUST BE ABLE TO DRIVE THIS LINE. IF * IS SHOWN ON AN OFF-PAGE CONNECTOR THEN THE HARDWARE NECESSARY TO OVERRIDE THE SIGNAL IS ASSUMED TO EXIST ON ANOTHER SCHEMATIC.

THE SECOND HALF OF LS629 VCO IS NOT USED SO THE ENABLE (PIN 8 ACTIVE LOW) MUST BE TIED TO +5. THE DISPOSITION OF THE OTHER UNUSED PINS IS: PINS 10, 12, 13 N.C
1, 14 +5V

- DGND
- AGND

LTR	REVISIONS	APPROVED	DATE
A	AS ISSUED PER PCO 48-4693	MTS	
B	REV'D & ADDED SHTS 3-5. PER PCO 48-6082		3/11/83

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DATE 9-26-80 | 2/17/81 | 3/16/82

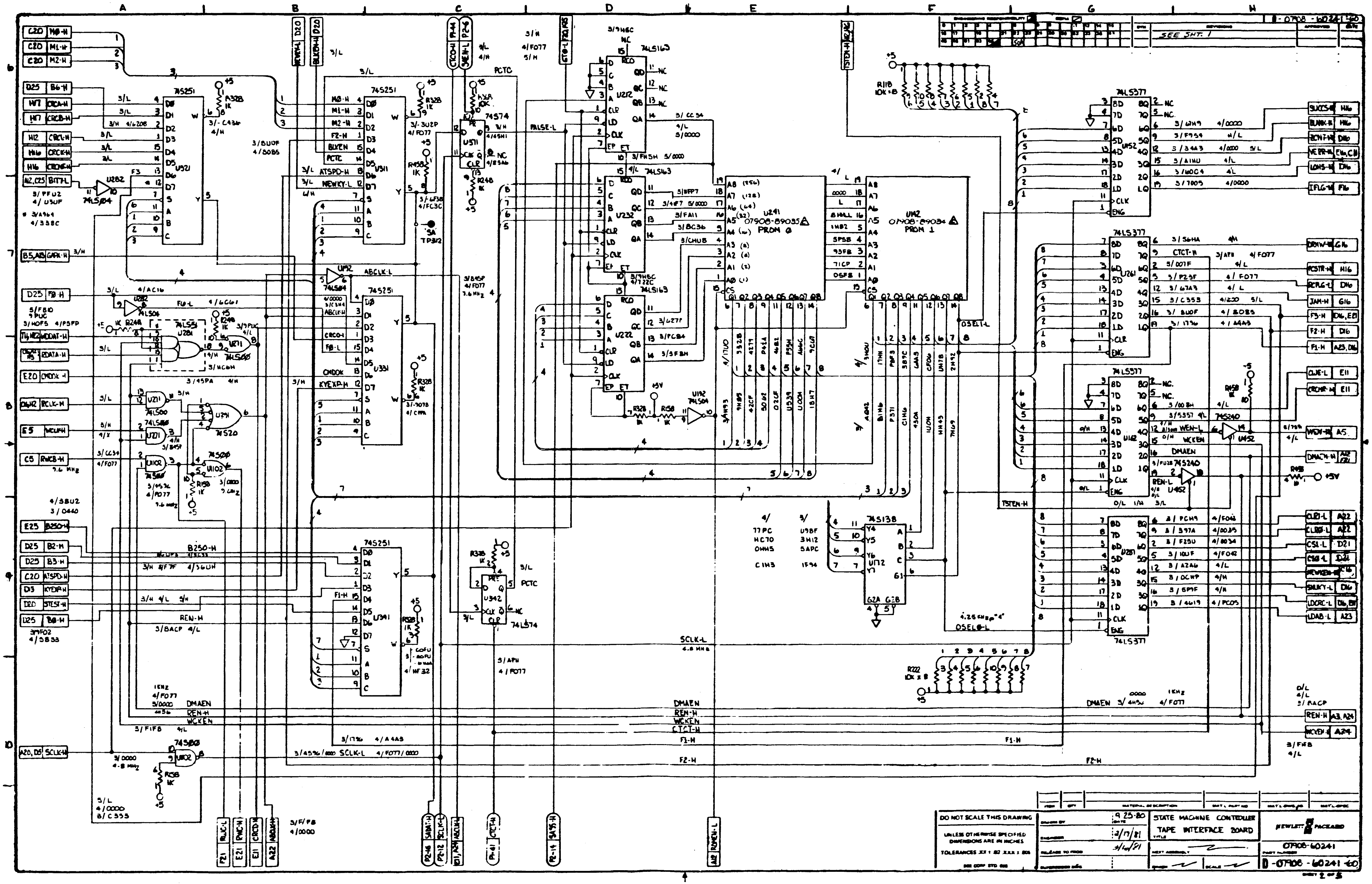
FIG 7
SIGNATURE ANALYSIS FOR TEST 4/5 TIB
TITLE DEBUG SCHEMATIC

HEWLETT PACKARD

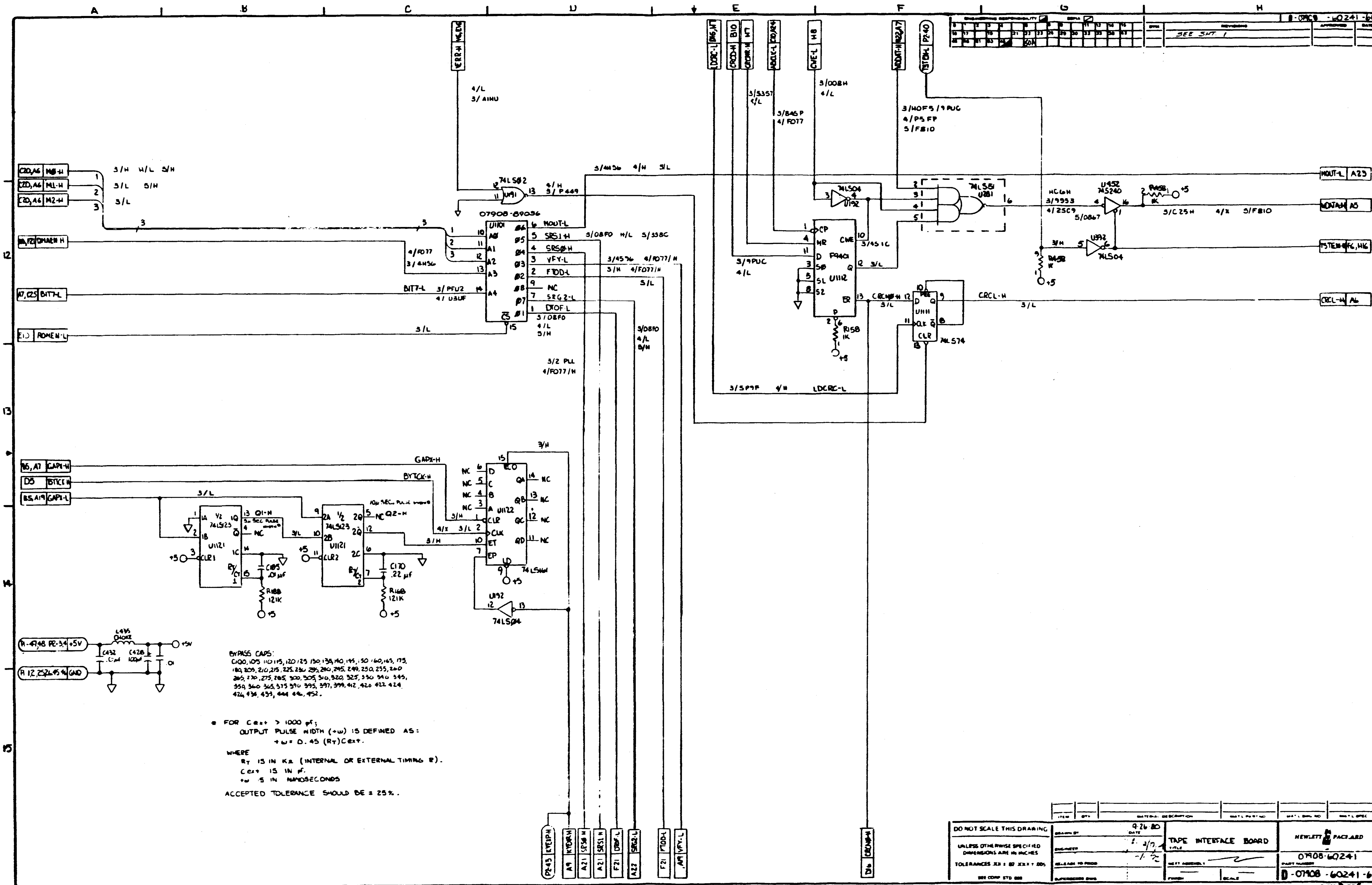
07908-60241

B-07908-60241-60

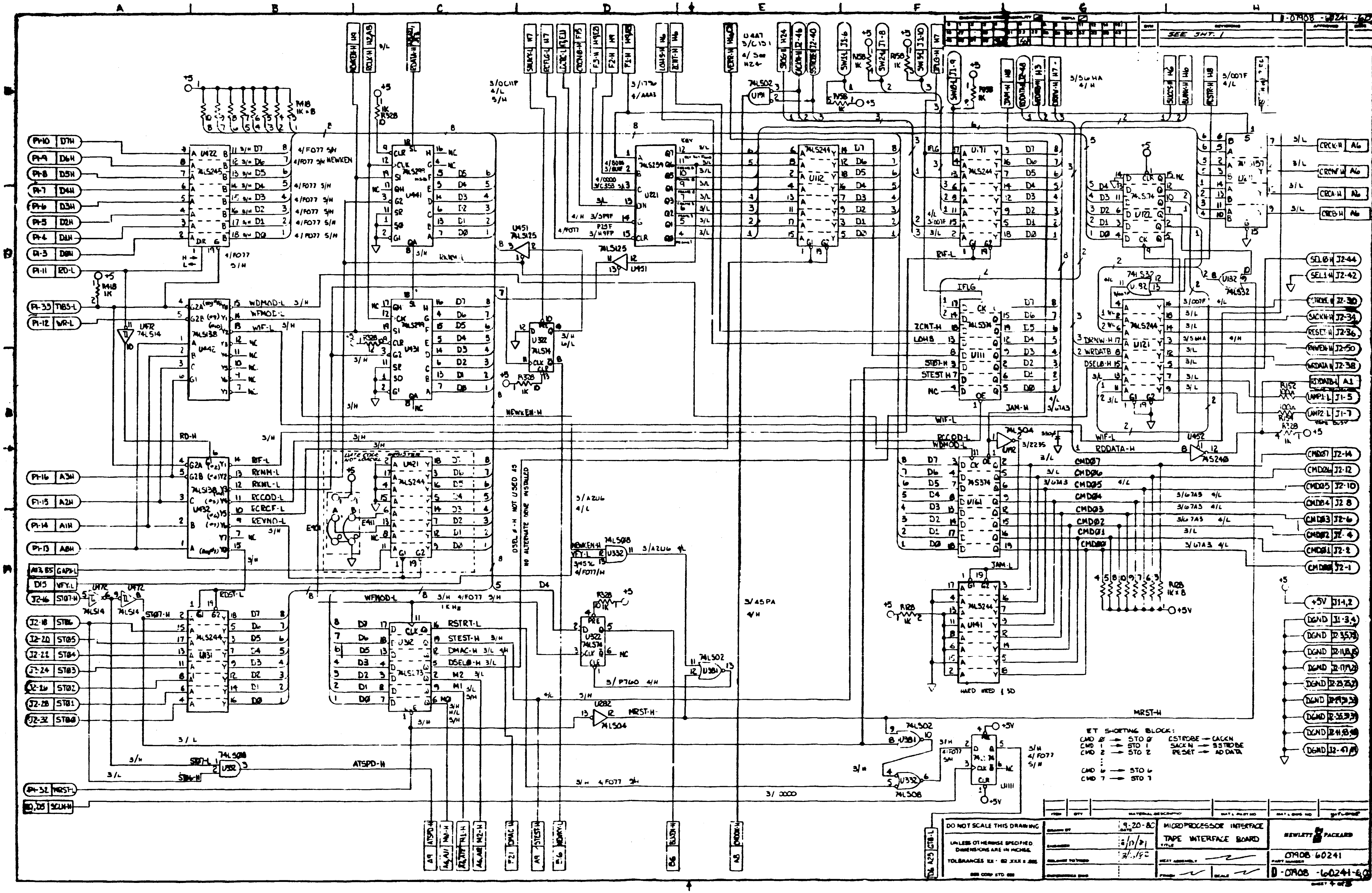
SHEET 1 OF 5



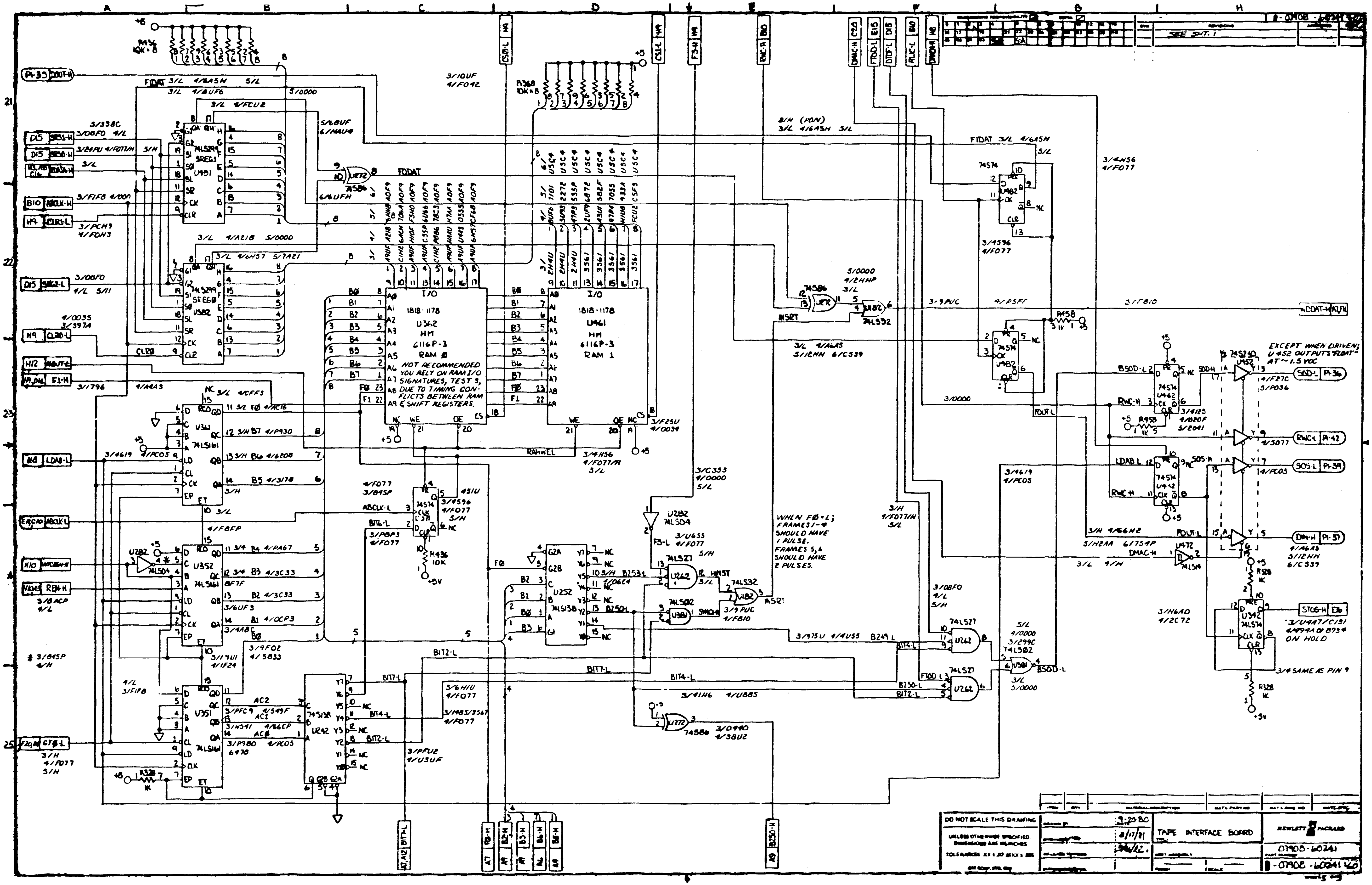
SEE SHT. 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
9-25-80
3/17/81
3/10/81
STATE MACHINE CONTROLLER
TAPE INTERFACE BOARD
HEWLETT PACKARD
07908-60241
D-07908-60241-60
SHEET 2 OF 3



74LS02
U91
07908-89036
U1101
74LS161
U1122
74LS123
U1121
74LS04
U192
F9401
U1112
74LS51
U1281
74S240
U452
74LS74
U1111
MOUT-L
SRS1-H
SRSØ-H
VFY-L
FTOD-L
SRG2-L
DTOF-L
GAPX-H
BYTCK-H
CRCL-H
LDCRC-L
TSTEN-H
SEE SHT. 1
BYPASS CAPS:
C100, 105 110 115, 120 125 130, 135, 140, 145, 150 160, 165, 175,
180, 205, 210, 215, 225, 230 235, 240, 245, 249, 250, 255, 260
265, 270, 275, 285, 300, 305, 310, 320, 325, 330 340 345,
350, 360 365, 375 390 395, 397, 399, 412, 420 422 424,
426, 436, 439, 444 446, 452.
* FOR Cext > 1000 pf;
OUTPUT PULSE WIDTH (tw) IS DEFINED AS:
tw = 0.45 (RT)Cext.
WHERE
RT IS IN KΩ (INTERNAL OR EXTERNAL TIMING R).
Cext IS IN pf.
tw IS IN NANOSECONDS
ACCEPTED TOLERANCE SHOULD BE ± 25%.
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
9-26-80
TAPE INTERFACE BOARD
HEWLETT PACKARD
07908-60241
D-07908-60241-60
SHEET 3 OF 3

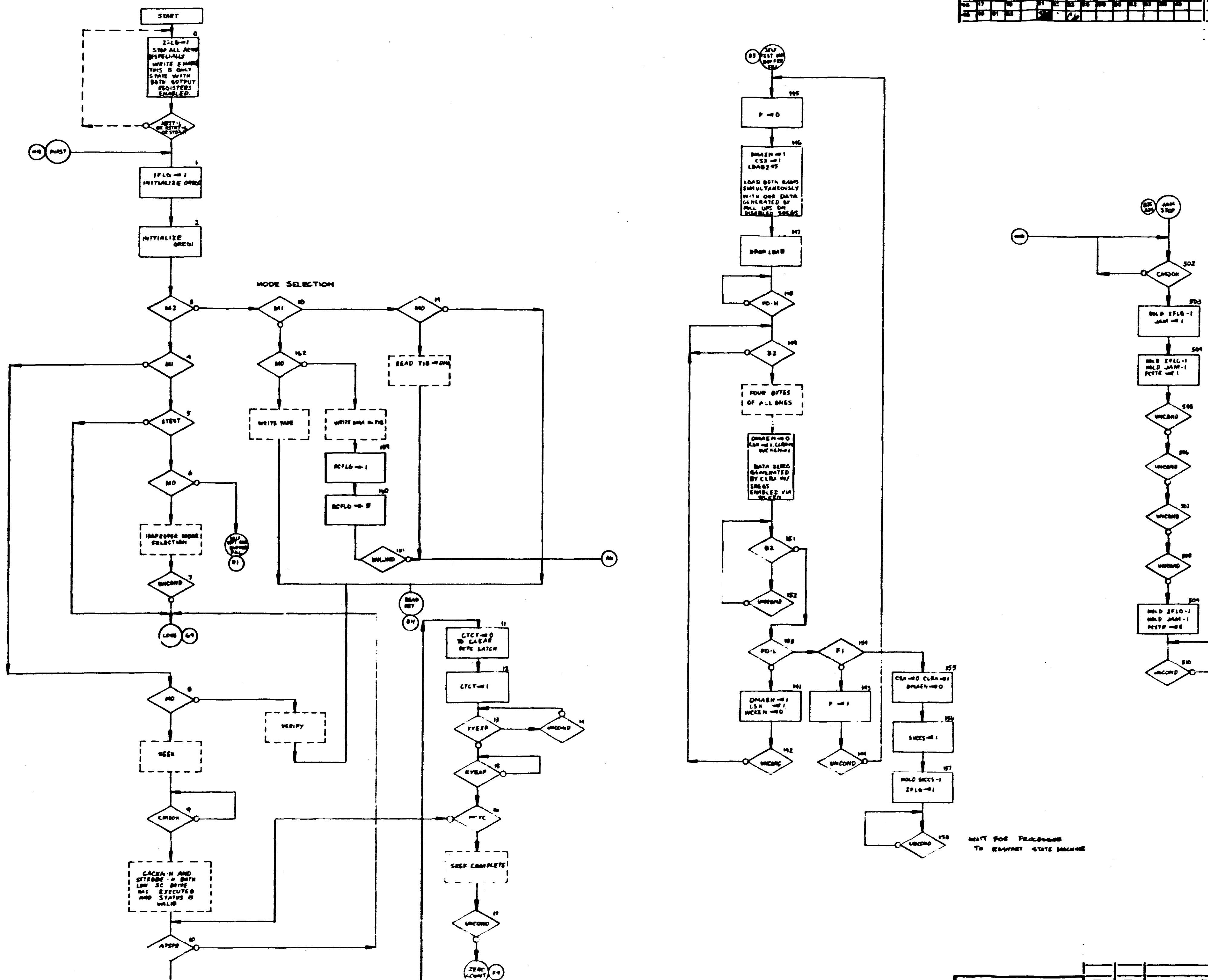


SEE SHT. 1
ET SHORTING BLOCK:
CMD Ø → STO Ø
CMD 1 → STO 1
CMD 2 → STO 2
CMD 6 → STO 6
CMD 7 → STO 7
CSTROBE → CACKN
SACKN → SSTROBE
RESET → ADDATA
HARD WIRED ↓ 5D
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
9-20-80
MICROPROCESSOR INTERFACE
TAPE INTERFACE BOARD
HEWLETT PACKARD
07908-60241
D-07908-60241-6



NOT RECOMMENDED YOU RELY ON RAM I/O SIGNATURES, TEST 3, DUE TO TIMING CONFLICTS BETWEEN RAM & SHIFT REGISTERS.
WHEN FØ=L; FRAMES 1-4 SHOULD HAVE 1 PULSE. FRAMES 5,6 SHOULD HAVE 2 PULSES.
EXCEPT WHEN DRIVEN; U452 OUTPUTS "FLOAT" AT ~ 1.5 VDC
1818-1178 U362 HM 6116P-3 RAM Ø
1818-1178 U461 HM 6116P-3 RAM 1
SEE SHT. 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
9-20-80
TAPE INTERFACE BOARD
HEWLETT PACKARD
07908-60241

MODE
Ø - WRITE DMA TO TIB
1 - WRITE DMA TO TAPE
2 - READ TAPE TO TIB
3 - READ TIB TO DMA
4 - VERIFY N BLOCKS
5 - SEEK N BLOCKS
6 - DMA TESTS



STATE	OPERATION	LOCATION
0-8	START MODE SELECT	B1-3
9-17	SEEK	A4-D5
18-19	MODE SELECT	B2
20-51	DMA	A6-18, C6-9
52-54	LOHS ERROR	C9-8
55-124	WRITE DATA TO TAPE	C9-18, D6-C8
125-127	CHECK FOR BLANK	B26
128-137	KYEXP REPLACEMENT	C11-D12
143-160	DMA BUFFER FILL	E1-4
161	MODE SELECT	C3
163-205	READ KEY	B11-D14
206-215	CHECK FOR BLANK	A21-B23
111-212	READ HEADERS 1.2	C23
216-223	BLANK ERROR	B23-24 A23-24
224-228	READ HEADERS 1.2	B21-22
229-238	TIME THRU FRAME	B23-C24
229-248	READ HEADERS 1.2	B22-C24
249-256	READ FRAME NO.7	A16-D16
257-262	READ DATA TO RAM OF EXPECTED FRAME	G17-18
263-271	SUCCS STATUS ON READ	G18-H19
272-289	READ HEADERS 3.4	F12, B21-D24
290-312	READ HEADERS 5.6	F15, E21-23
249-338	READ FRAME No.	A16-C17
339-341	SKIP 4TH FRAME	C19
342-352	READ NEXT FRAME	C19-20
353-359	SKIP 5TH FRAME	B19-C20
360-394	SKIP 2ND OR 3RD FRAME	F16-17 B19-20 H21-22
395-406	READ 1ST OR 2ND FRAME	F24-G24
407	INCREMENT FRAME TO 5	F19
408-418	CHECK IF GAP WIDTH	F12-17
419-429	INCREMENT FRAME COUNT	E14-E19
430-441	READ 1ST OR 2ND	E21-E25
442-456	CHECK IF GAP SPRING	G12-14
491-494	READ 1ST OR 2ND DATA FRAMES	C17
495-499	VERR STATUS	H19, G9-10
500-501	VERIFY COUNT	A23-24
502-510	ZERO COUNT STATUS	F9
511	JAM STOP	G2-3
	LAST	H9

SPARES 139-142
162
463-490

WAIT FOR PEACEFUL RESTART STATE MACHINE

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	TH	2/18/83
B	REV'D PER C0480253		8/27/83

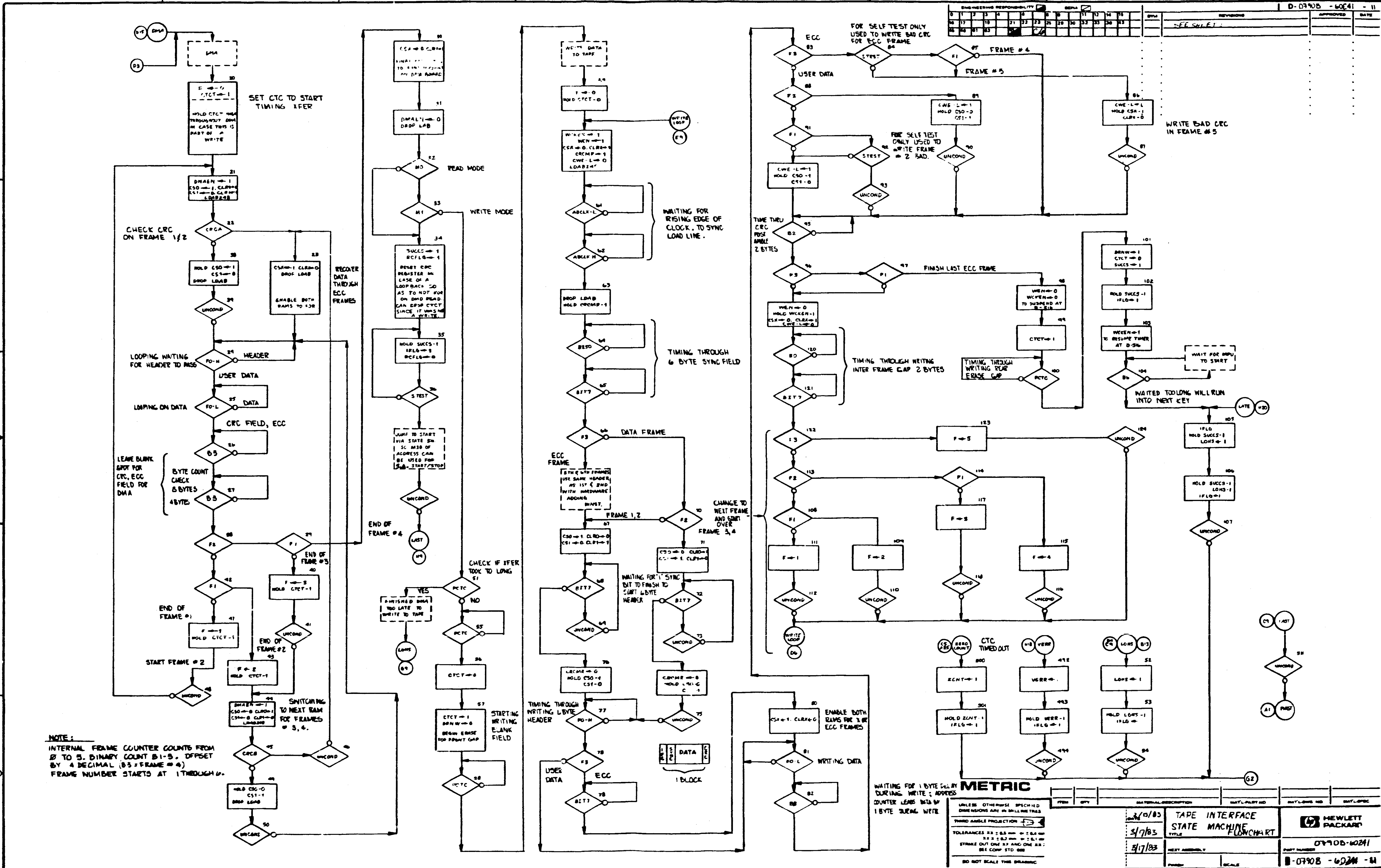
TAPE INTERFACE STATE MACHINE FLOWCHART

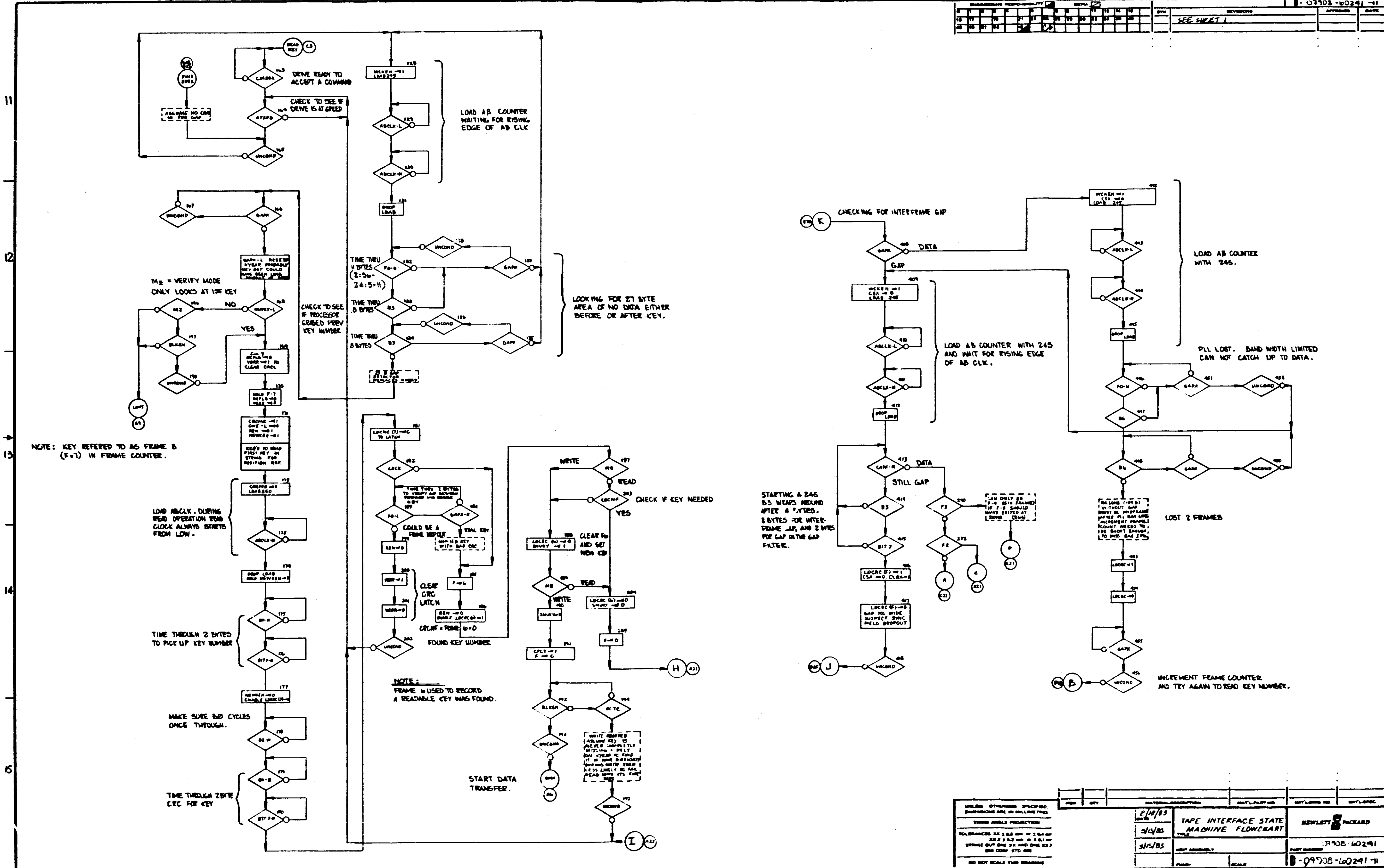
HEWLETT PACKARD

07908-60241

B-07908-60241-11

SHEET 1 OF 5


SET CTC TO START TIMING XFER
HOLD CTCT THROUGHOUT DMA IN CASE THIS IS PART OF A WRITE
CHECK CRC ON FRAME 1/2
RECOVER DATA THROUGH ECC FRAMES
ENABLE BOTH RAMS TO ECB
LOOPING WAITING FOR HEADER TO PASS
HEADER
USER DATA
LOOPING ON DATA
DATA
CRC FIELD, ECC
LEAVE BLANK SPOT FOR CRC, ECC FIELD FOR DMA
BYTE COUNT CHECK 8 BYTES
4 BYTES
END OF FRAME #3
END OF FRAME #1
END OF FRAME #2
START FRAME # 2
SWITCHING TO NEXT RAM FOR FRAMES # 3, 4.
NOTE:
INTERNAL FRAME COUNTER COUNTS FROM Ø TO 5. BINARY COUNT B1-5. OFFSET BY 4 DECIMAL (B3 = FRAME # 4)
FRAME NUMBER STARTS AT 1 THROUGH 6.
READ MODE
WRITE MODE
RESET CRC REGISTER IN CASE OF A LOOPBACK SO AS TO NOT FOR ON DMD READ. CAN ERSP CTCT SINCE IT WAS NOT A WRITE.
END OF FRAME #4
CHECK IF XFER TOOK TO LONG
YES
NO
FINISHED DMA TOO LATE TO WRITE TO TAPE
STARTING WRITING BLANK FIELD
BEGIN ERASE FOR FRONT GAP
WRITE DATA TO TAPE
WAITING FOR RISING EDGE OF CLOCK. TO SYNC LOAD LINE.
DROP LOAD
TIMING THROUGH 6 BYTE SYNC FIELD
DATA FRAME
ECC FRAME
FRAME 1, 2
CHANGE TO NEXT FRAME AND START OVER
FRAME 3, 4
WAITING FOR "1" SYNC BIT TO FINISH TO START 6 BYTE HEADER
TIMING THROUGH WRITING 6 BYTE HEADER
USER DATA
ECC
DATA
1 BLOCK
ECC
FOR SELF TEST ONLY USED TO WRITE BAD CRC FOR ECC FRAME
FRAME # 4
FRAME # 5
USER DATA
FOR SELF TEST ONLY USED TO WRITE FRAME # 2 BAD.
WRITE BAD CRC IN FRAME # 5
TIME THRU CRC POST AMBLE 2 BYTES
FINISH LAST ECC FRAME
TO SUSPEND AT
TIMING THROUGH WRITING INTER FRAME GAP 2 BYTES
TIMING THROUGH WRITING REAR ERASE GAP
TO RESUME TIMER
WAIT FOR MPU TO START
WAITED TOO LONG WILL RUN INTO NEXT KEY
ENABLE BOTH RAMS FOR 3 & 4 ECC FRAMES
WRITING DATA
WAITING FOR 1 BYTE DELAY DURING WRITE ; ADDRESS COUNTER LEADS DATA BY 1 BYTE DURING WRITE
CTC TIMED OUT
METRIC
TAPE INTERFACE STATE MACHINE FLOWCHART
HEWLETT PACKARD
07908-60241
D-07908-60241-11
SHEET 2 OF 5
DO NOT SCALE THIS DRAWING



SEE SHEET 1

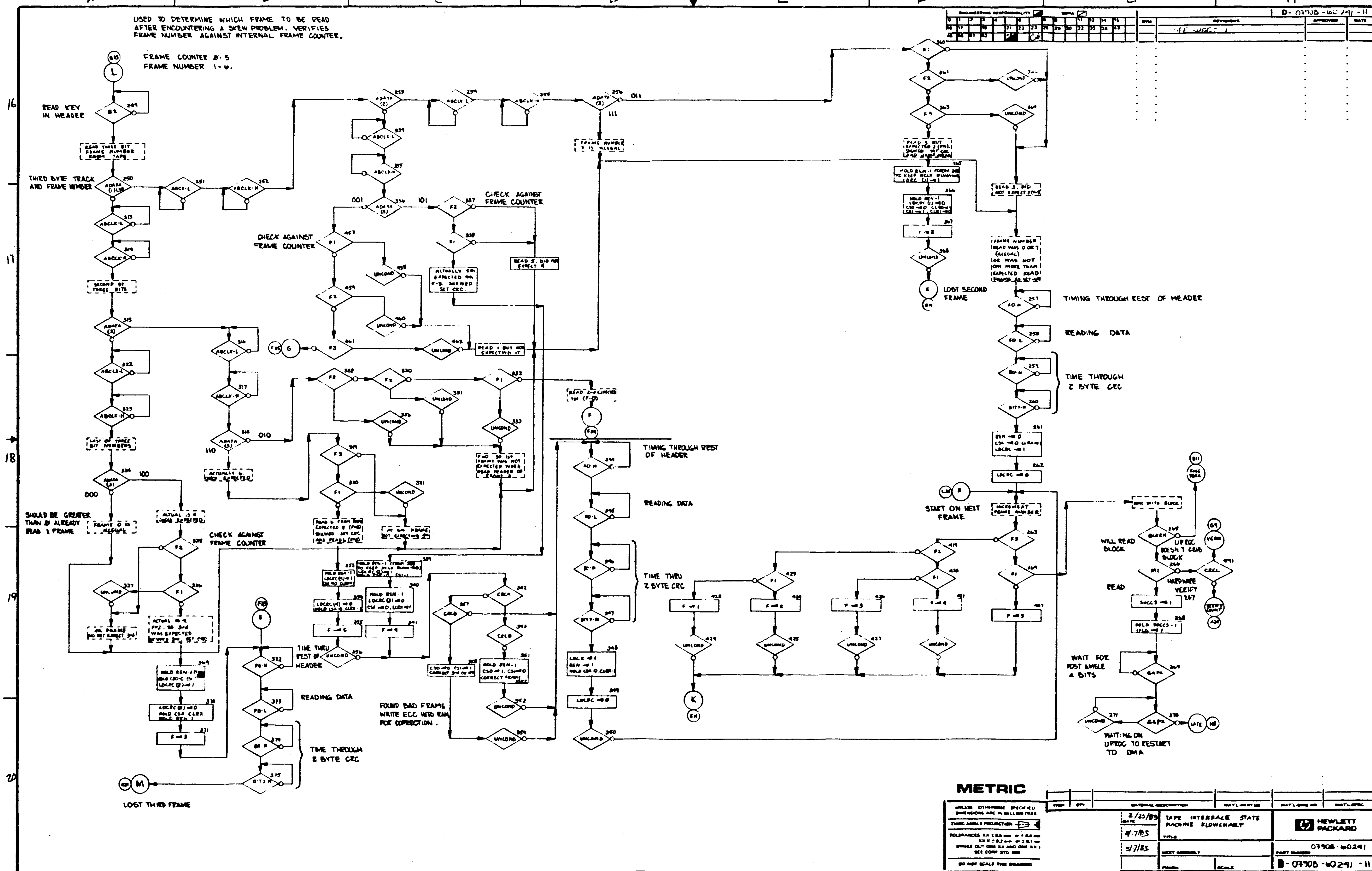
TAPE INTERFACE STATE MACHINE FLOWCHART

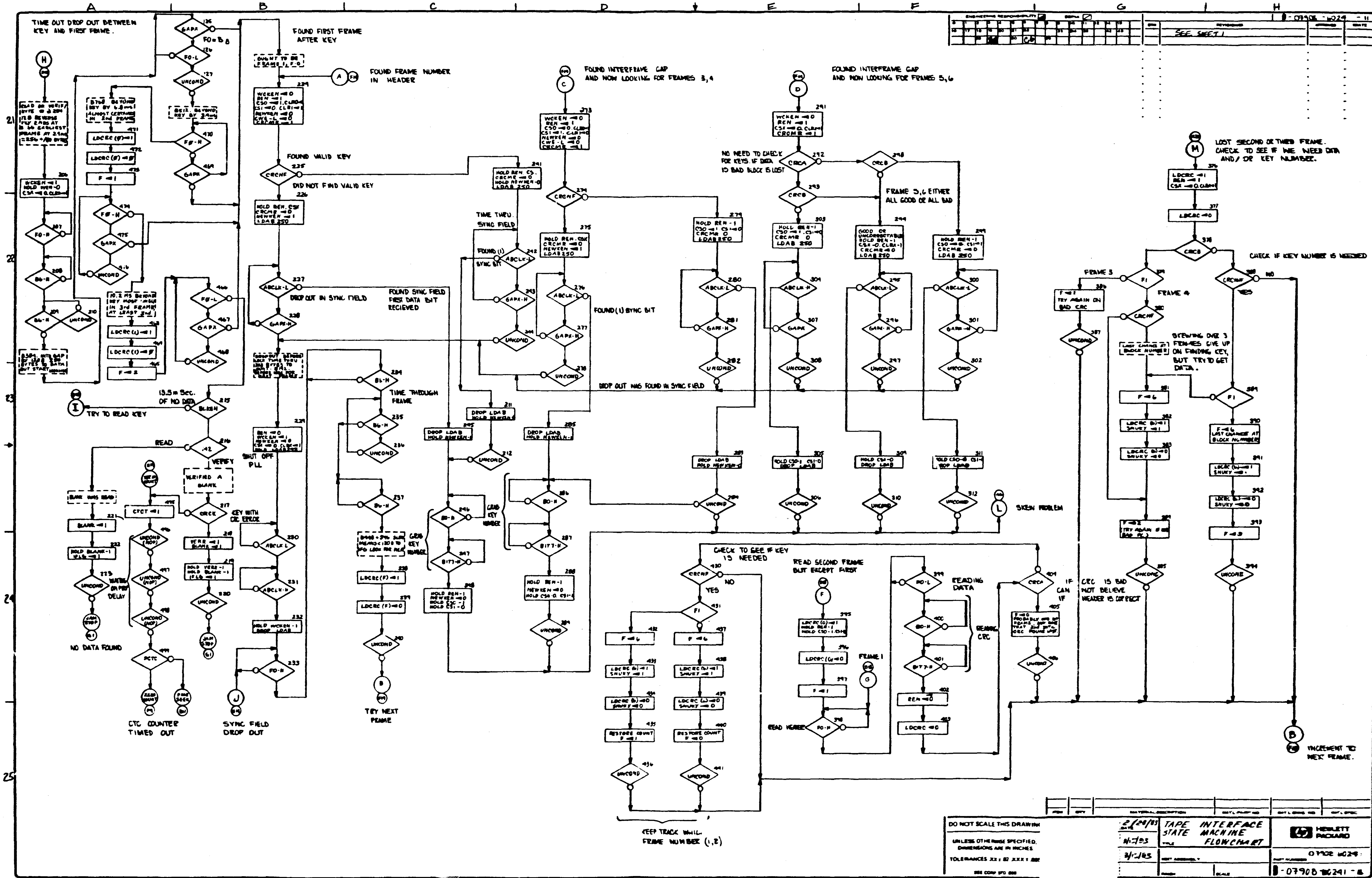
HEWLETT PACKARD

09908-60291

D-09908-60291-11

SHEET 3 OF 5


USED TO DETERMINE WHICH FRAME TO BE READ AFTER ENCOUNTERING A SKEW PROBLEM. VERIFIES FRAME NUMBER AGAINST INTERNAL FRAME COUNTER.
FRAME COUNTER 0-5
FRAME NUMBER 1-6.
READ KEY IN HEADER
THIRD BYTE TRACK AND FRAME NUMBER
CHECK AGAINST FRAME COUNTER
SHOULD BE GREATER THAN Ø ALREADY READ 1 FRAME
LOST THIRD FRAME
TIME THRU REST OF HEADER
READING DATA
TIME THROUGH 2 BYTE CRC
FOUND BAD FRAME WRITE ECC INTO RAM FOR CORRECTION.
TIMING THROUGH REST OF HEADER
TIME THRU 2 BYTE CRC
LOST SECOND FRAME
TIMING THROUGH REST OF HEADER
TIME THROUGH 2 BYTE CRC
START ON NEXT FRAME
WILL READ BLOCK
UPROC DOESN'T GRAB BLOCK
HARDWARE VERIFY
READ
WAIT FOR POST AMBLE & BITS
WAITING ON UPROC TO RESTART TO DMA
METRIC
TAPE INTERFACE STATE MACHINE FLOWCHART
HEWLETT PACKARD
07908-60241
B-07908-60241-11



TIME OUT DROP OUT BETWEEN KEY AND FIRST FRAME.
FOUND FIRST FRAME AFTER KEY
FOUND FRAME NUMBER IN HEADER
FOUND INTERFRAME GAP AND NOW LOOKING FOR FRAMES 3, 4
FOUND INTERFRAME GAP AND NOW LOOKING FOR FRAMES 5, 6
LOST SECOND OR THIRD FRAME. CHECK TO SEE IF WE NEED DATA AND/OR KEY NUMBER.
FOUND VALID KEY
DID NOT FIND VALID KEY
NO NEED TO CHECK FOR KEYS. IF DATA IS BAD BLOCK IS LOST
FRAME 5, 6 EITHER ALL GOOD OR ALL BAD
TIME THRU. SYNC FIELD
FOUND (1) SYNC BIT
DROP OUT IN SYNC FIELD
FOUND SYNC FIELD FIRST DATA BIT RECIEVED
CHECK IF KEY NUMBER IS NEEDED
FRAME 3
FRAME 4
TRY AGAIN ON BAD CRC
SKEWING OVER 3 FRAMES GIVE UP ON FINDING KEY, BUT TRY TO GET DATA.
DROP OUT WAS FOUND IN SYNC FIELD
13.5 m Sec. OF NO DATA
TRY TO READ KEY
READ
VERIFY
VERIFIED A BLANK
BLANK WAS READ
KEY WITH CRC ERROR
SHUT OFF PLL
TIME THROUGH FRAME
GRAB KEY NUMBER
SKEW PROBLEM
CHECK TO SEE IF KEY IS NEEDED
READ SECOND FRAME BUT EXCEPT FIRST
READING DATA
READING CRC
IF CRC IS BAD CAN NOT BELIEVE IF HEADER IS CORRECT
FRAME 1
READ HEADER
NO DATA FOUND
CTC COUNTER TIMED OUT
SYNC FIELD DROP OUT
TRY NEXT FRAME
INCREMENT TO NEXT FRAME.
KEEP TRACK WHILE FRAME NUMBER (1, 2)
SEE SHEET 1
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
TAPE INTERFACE STATE MACHINE FLOWCHART
HEWLETT PACKARD
07908-60241

P/N 07908-60004

MOTHERBOARD PCA-A7

Series Code C-2146

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60004
07908-68004

DATE CODE : C-2146

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
J1	1251-7070	CONN 3-PIN M
J2	1251-7068	CONN 2-PIN M
MP1	07908-80004	BD-ETCHED
MP2	7120-6830	LABEL-INFO
XA1P1	1251-4573	CONN-PC 2X25
XA1P2	1251-4573	CONN-PC 2X25
XA2P1	1251-4573	CONN-PC 2X25
XA2P2	1251-4573	CONN-PC 2X25
XA3P1	1251-4573	CONN-PC 2X25
XA3P2	1251-4573	CONN-PC 2X25
XA4P1	1251-4573	CONN-PC 2X25
XA4P2	1251-4573	CONN-PC 2X25
XA5P1	1251-4573	CONN-PC 2X25
XA5P2	1251-4573	CONN-PC 2X25
XA6P1	1251-4573	CONN-PC 2X25
XA6P2	1251-4573	CONN-PC 2X25

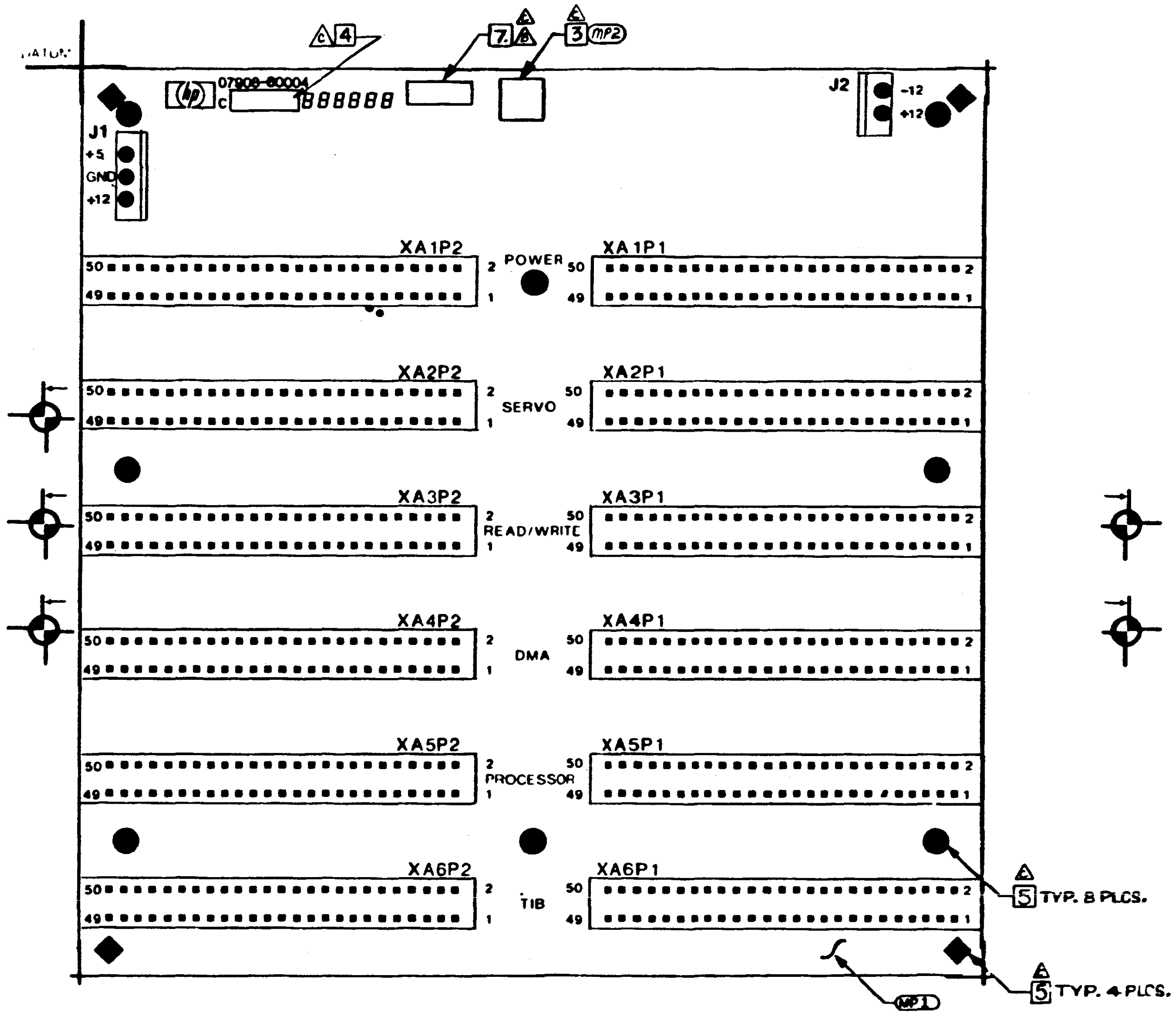
END OF MATERIAL LIST.

F-07908-60004-1

LTR	REVISIONS	APPROVED	DATE
A	AS ISSUED	AH / [illegible]	2-11-81
B	ADDED SOLDERMASK TO COMP SIDE; REV'D NOTE 2; ADDED NOTE 6 PC 48-4465	[illegible]	9-29-81
C	RENUMBERED EXISTING NOTES & ADDED NOTES 1 & 7 PER PC 48-4301/REVA	[illegible]	12-11-81
D	DATE CODE WAS 2106 PER PPCO 48-4475	[illegible]	1/26/82
E	DATE CODE WAS 2146 REVISED TO C-2146 PER PCO. 48-4696.	[illegible]	4/7/82

METRIC

DISTANCE BETWEEN
REGISTRATION TARGETS 190.50 ± .08



REFERENCE DRAWINGS:

SCHEMATIC D-07908-60004 -50

UNLESS OTHERWISE SPECIFIED:

1. THIS BOARD CONFORMS TO CORPORATE AUTOMATIC INSERTION STANDARDS AS PER AXIAL LEAD MANUAL DATED 4-80.
2. THIS BOARD IS NOT ONE-TENTH INCH GRID TESTABLE.
3. INSTALL MP2 AFTER LINE TEST.
4. OPR. 264: MARK ASSEMBLY DATE CODE C-2146.
5. OPR. 265: MASK PRIOR TO LOADING.
6. USE TOOL NUMBER T-213876 TO POSITION CONNECTORS WHILE IN FLOW SOLDER.
7. P.C. PRODUCTION MARK ASSEMBLY WORK ORDER NUMBER COMPONENT SIDE ONLY.

F-07908-80004-12	TARGET MASTER	10-14-81
F-07908-80004-3	PAD MASTER	10-14-81
F-07908-80004-7	GRAPHICS-COMPONENT SIDE	10-14-81

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO	MAT'L-LOG NO	MAT'L-SPEC

DATE 10-27-80
2-11-81
2-11-81

TITLE MOTHER BOARD ASSEMBLY

NEXT ASSEMBLY ~

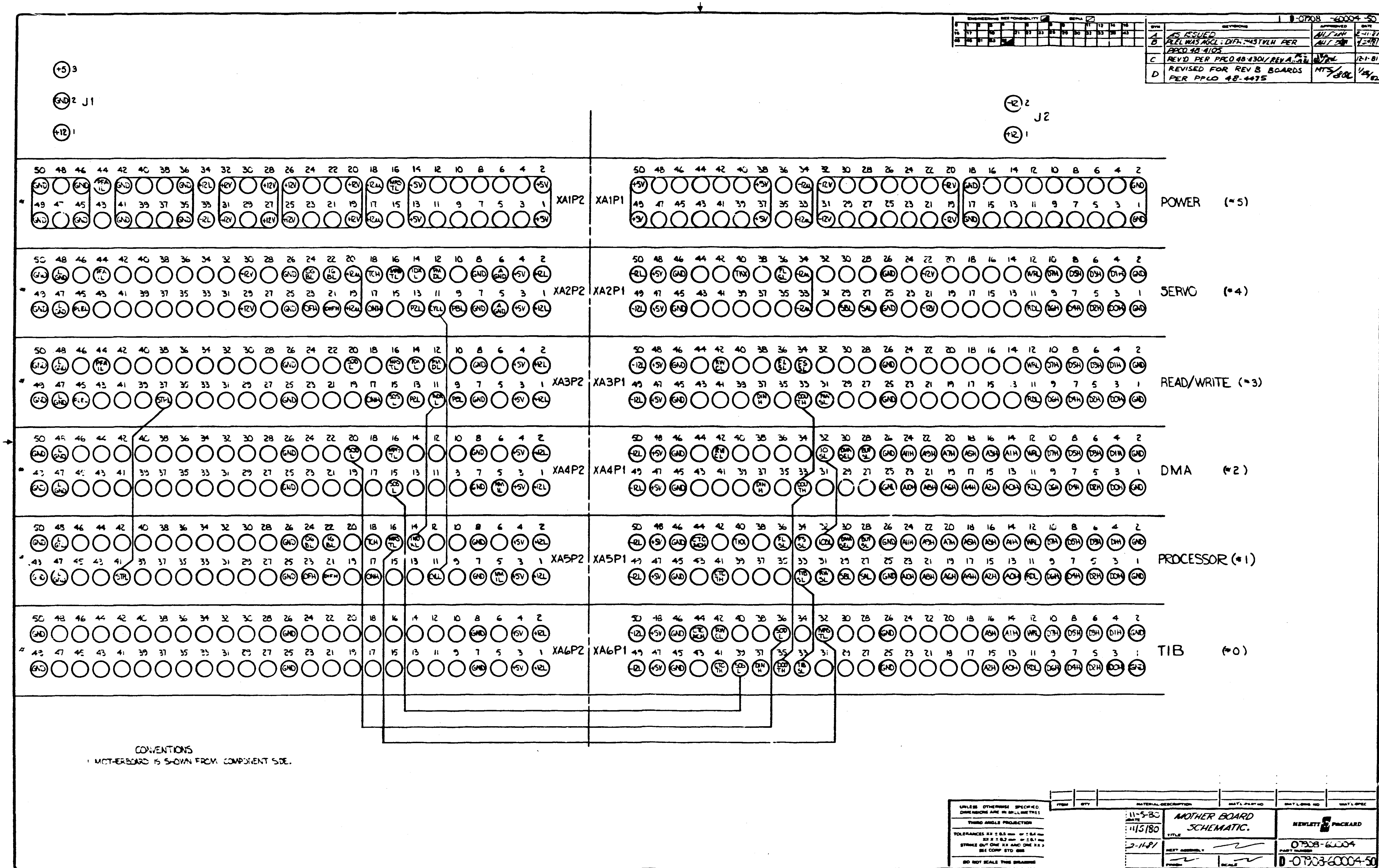
FINISH ~ SCALE ~

HEWLETT PACKARD

PART NUMBER 07908-60004

F-07908-60004-1

SHEET 1 OF 1



A AS ISSUED
B PLEL WAS AGCL; DIFH WAS TVLH PER PPCO 48-4105
C REV'D PER PPCO 48-4301/REV A
D REVISED FOR REV B BOARDS PER PPCO 48-4475
J1
J2
XA1P2 XA1P1 POWER (#5)
XA2P2 XA2P1 SERVO (#4)
XA3P2 XA3P1 READ/WRITE (#3)
XA4P2 XA4P1 DMA (#2)
XA5P2 XA5P1 PROCESSOR (#1)
XA6P2 XA6P1 TIB (#0)
CONVENTIONS
1 MOTHERBOARD IS SHOWN FROM COMPONENT SIDE.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETRES
THIRD ANGLE PROJECTION
DO NOT SCALE THIS DRAWING
MOTHER BOARD SCHEMATIC.
HEWLETT PACKARD
07908-60004
D-07908-60004-50

P/N 07908-60142

SWITCH PCA-A8

Series Code D-2119

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60142
07908-67142
07908-68142

DATE CODE : D-2119

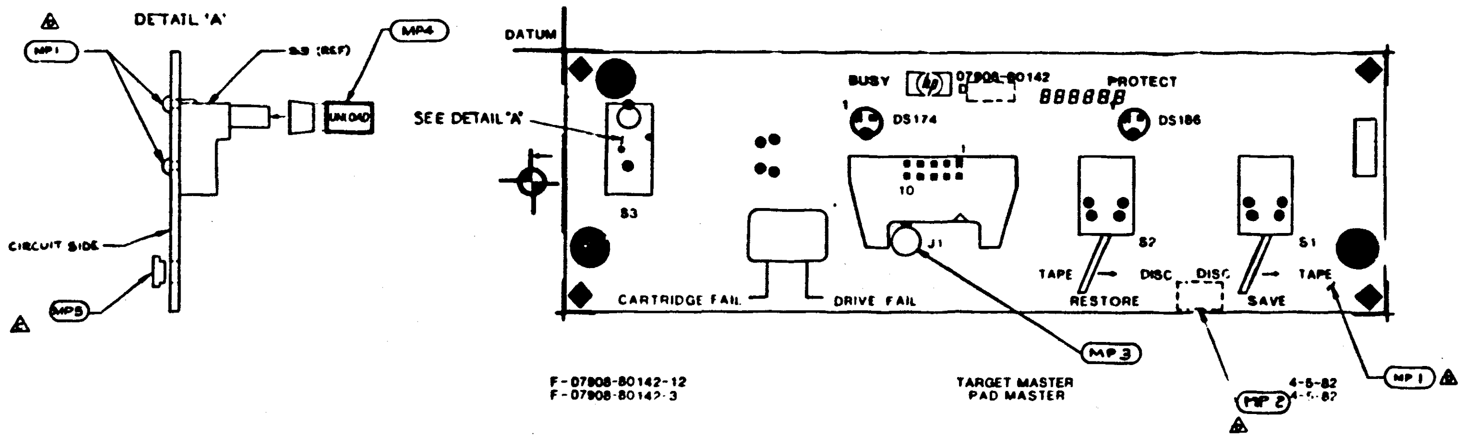
REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
DS174	1990-0487	LED-VISIBLE
DS186	1990-0487	LED-VISIBLE
J1	1251-5647	CONN 10-PIN M
MP1	07908-80142	BD-ETCHED
MP2	7120-6830	LABEL-INFO
MP3	1251-5595	PLZG KEY
MP4	5041-2711	KEY CAP UNLOAD
MP5	0380-0322	SPCR-RVT-ON
MP6	07908-40009	LIGHT PIPE
MP6	5060-9436	SWITCH-PUSHBUTTN
S1	3101-1675	SW-TGL DPST NS
S2	3101-1675	SW-TGL DPST NS
S3	5060-9436	SWITCH-PUSHBUTTN

END OF MATERIAL LIST.

F-07908-60142-1

LTR	DESCRIPTION	APPROVED	DATE
A	AS ISSUED		
B	REV'D TITLE TO SWITCH/PPCO-48-4018		
C	NOTE 2 WAS D-04: NOTE 5. ADDED MP5; DELETE S4 UNIT SELECTS PPCO-48-4114		
D	REV'D NOTE 1 ADDED NOTE 6 : REV MP 1 & MP 2 REF PER PPCO 48-4312		
E	REV'D NOTE 6 PER PCO 48-4737		
F	DELETED NOTES 3-9 PER PCO 48-4303		

DISTANCE BETWEEN
REGISTRATION TARGETS 196.85 ±.08



F-07908-80142-12
F-07908-80142-3

TARGET MASTER
PAD MASTER

4-5-82
4-5-82

F-07908-80142-7

GRAPHICS COMPONENT SIDE

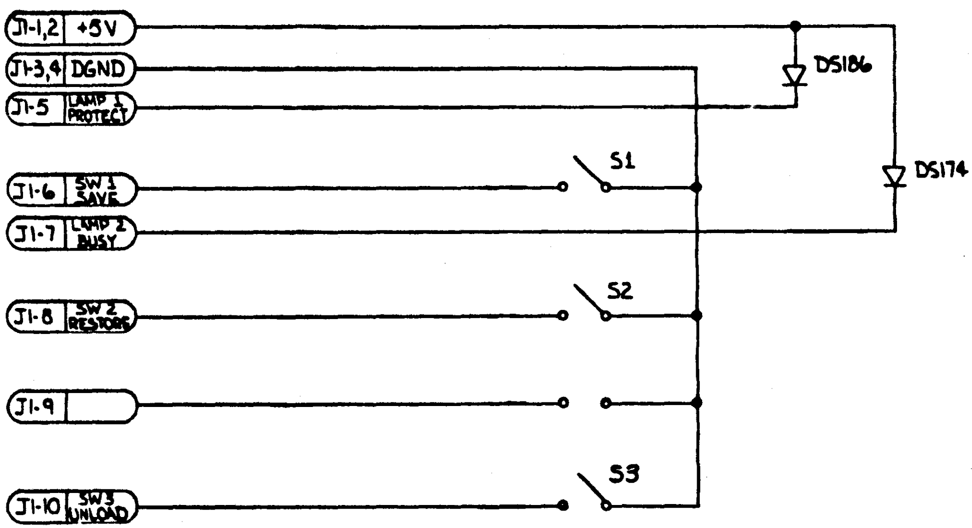
4-5-82

NOTES:

1. THIS BOARD CONFORMS TO CORPORATE AUTOMATIC INSERTION STANDARDS; AS PER AXIAL LEAD MANUAL DATED 10-22-81.
2. ASSEMBLY DATE CODE D-2119.

7-22-80	SWITCH ASSY DRAWING
1-26-81	
1-26-81	SEE WHERE USED
	2:1

HEWLETT PACKARD
07908-60142
F-07908-60142-1



SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		1-26-81
B	DELETE SW4 UNIT SEL & S4 PER PC 48-4114		6-2-81

B-07908-60142-50

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

DATE 7-30-80

1-26-81

1/26/81

TITLE: LINUS FRONT PANEL BOARD-SCHEMATIC

HEWLETT PACKARD

PART NUMBER 07908-60142

B-07908-60142-50

SHEET 1 OF 1

P/N 07908-60013

RECTIFIER PCA-A9

Series Code E-2220

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART NUMBER(S): 07908-60013
07908-68013
07908-69013

DATE CODE : E-2220

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C103	0180-2217	CAP 350UF 50V AL
C139	0160-3828	CAP .068UF 20%
C145	0160-0127	CAP 1UF 20%
C152	0160-3828	CAP .068UF 20%
C153	0180-0116	CAP 6.8UF 10%
C154	0180-0291	CAP 1UF 10%
C166	0180-0291	CAP 1UF 10%
C168	0160-3828	CAP .068UF 20%
C250	0180-0291	CAP 1UF 10%
CR138	1901-0743	DIO-1N4004
CR157	1901-0040	DIODE-SWITCHING
CR161	1901-0040	DIODE-SWITCHING
CR162	1901-0040	DIODE-SWITCHING
CR167	1901-0743	DIO-1N4004
CR253	1901-0743	DIO-1N4004
DS170	1990-0529	LED-VISIBLE RED
DS171	1990-0523	LED-VISIBLE GRN
DS172	1990-0529	LED-VISIBLE RED
DS173	1990-0523	LED-VISIBLE GRN
DS174	1990-0529	LED-VISIBLE RED
DS175	1990-0523	LED-VISIBLE GRN
F194	2110-0001	FUSE 1A 250V
F195	2110-0523	FUSE 10A 32V
F255	2110-0001	FUSE 1A 250V
F290	2110-0523	FUSE 10A 32V
F291	2110-0048	FUSE 15A 32V
J1	1251-5803	CONN 12-PIN F
J2	1251-3837	CONN 4-PIN M
J3	1251-4780	CONN 2-PIN M
J4	1251-4780	CONN 2-PIN M
J5	1251-3819	CONN 6-PIN M
MP1	07908-80013	BD-ETCHED
MP10	1200-0043	INSL-XSTR TO3 AL
MP11	0380-0757	STDF-RVT-ON
MP12	6040-0239	COMPOUND-THERMAL
MP2	7120-6830	LABEL-INFO
MP3	2200-0600	SCREW-MACHINE
MP5	1200-0081	INSUL-FLG-BSHG
MP6	2260-0009	NUT 4-40 W/LK
MP7	1205-0310	HEAT SINK TO-3
MP8	2110-0551	FUHLR-CLIP 250V
MP9	0340-0164	INSUL-XSTR
Q120	1854-0611	XSTR NPN 2N6055
Q133	1854-0023	XSTR NPN SI
Q137	1853-0314	XSTR PNP 2N2905A
R108	0757-0839	RES 10K 1% .5
R110	0811-1666	RES 1.0 5% 3W

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

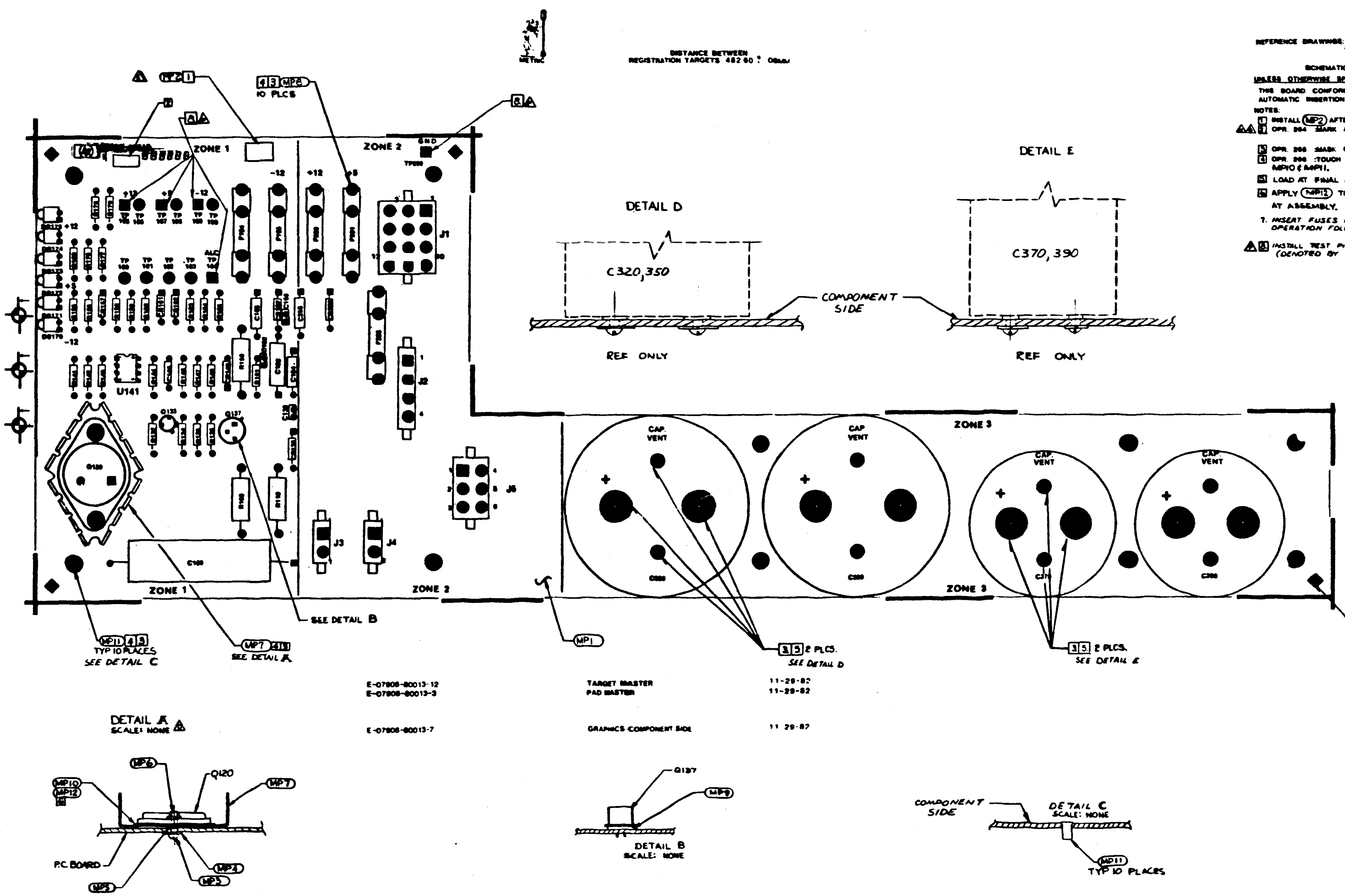
MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60013
07908-68013
07908-69013

DATE CODE : E-2220

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R132	0757-0280	RES 1K 1%.125
R134	0757-0280	RES 1K 1%.125
R135	0757-0280	RES 1K 1%.125
R136	0757-0401	RES 100 1%.125
R141	0698-3150	RES 2.37K 1%.125
R142	0698-3151	RES 2.87K 1%.125
R143	0698-3441	RES 215 1%.125
R144	0698-0084	RES 2.15K 1%.125
R146	0757-0465	RES 100K 1%.125
R147	0757-0465	RES 100K 1%.125
R148	0757-0465	RES 100K 1%.125
R150	0698-3403	RES 348 1% .5
R151	0757-0465	RES 100K 1%.125
R155	0757-0317	RES 1.33K 1%.125
R156	0757-0442	RES 10K 1%.125
R158	0698-0084	RES 2.15K 1%.125
R159	0757-0402	RES 110 1%.125
R160	0757-0280	RES 1K 1%.125
R163	0757-0280	RES 1K 1%.125
R164	0757-0280	RES 1K 1%.125
R165	0757-0280	RES 1K 1%.125
R169	0757-0421	RES 825 1%.125
R176	0757-0416	RES 511 1%.125
R177	0698-3442	RES 237 1%.125
R178	0757-0421	RES 825 1%.125
R179	0757-0317	RES 1.33K 1%.125
TP184	0360-1682	TERM-PIN
TP185	0360-1682	TERM-PIN
TP187	0360-1682	TERM-PIN
TP189	0360-1682	TERM-PIN
TP299	0360-1682	TERM-PIN
U141	1826-0346	IC 358
VR149	1902-0689	DIO-ZNR 5.1V 1%

END OF MATERIAL LIST.



REFERENCE DRAWINGS: SCHEMATIC - D-07908-60013-50

SCHEMATIC D-07908 60013-50

UNLESS OTHERWISE SPECIFIED:

THIS BOARD CONFORMS TO CORPORATE AUTOMATIC INSERTION STANDARDS

NOTES:

1. INSTALL MP2 AFTER LINE TEST.
2. OPR. 204 :MARK ASSEMBLY DATE CODE E-2220
3. OPR. 206 :MASK PRIOR TO LOADING
4. OPR. 208 :TOUCH UP. INSTALL Q120, MP3 THRU MP8, MP10 & MP11.
5. LOAD AT FINAL ASSEMBLY C320, C350, C370 & C390.
6. APPLY MP12 TO BOTH SURFACES OF MP10 AT ASSEMBLY.
7. INSERT FUSES INTO FUSE CLIPS IN THE TOUCH-UP OPERATION FOLLOWING WAVE SOLDER OF PCBS.
8. INSTALL TEST PINS AT THE 6 LOCATIONS ONLY (DENOTED BY SQUARE PAD.)

RECTIFIER ASSEMBLY	HEWLETT PACKARD
SEE WHERE USED	07908-60013
NOTED 2:1	E-07908-60013-1

ER48 D/H:

H E W L E T T - P A C K A R D C O. / hp /

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline). (L209)

LTR	REVISIONS	DATE	INIT	MF
A	AS ISSUED	12-02-81	sb/ML	M
B	ADDED APPENDIX A PER PPCO 48-4364	01-04-81	sr/ML	M
C	REVISED PER PCO 48-4837	06-09-82	sr/ML	M
D	ADDED BOARD REV E PER PCO 48-6065	01-05-83	db/ML	M
E	DELETE APPENDIX A PER DCO 48-6229	03-03-83	sjb/ML	M

C	48-4837	sr/ML	06-10-82	MODEL 7908	STK # 07908-69013
	48-6065	db/ML	01-05-83	UPDATE/REVISION PROCEDURE	
E	48-6229	sjb/ML	03-03-83	BY	DATE MAY 16, 1984
IT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 4
	REVISIONS			SUPERSEDES	DWG # A-07908-69013-1

/ hp /

HEWLETT-PACKARD CO.

UPDATING AND REVISION PROCEDURE

07908-69013

This procedure contains instructions for modification of the rectifier PCA, 07908-60013 to version 07908-69013.

REFERENCES:

SML: 07908-68013 Untested PCA

07908-66013 Reel

Dwgs: E-07908-60013-1 Assembly Dwg.

D-07908-60013-50 Schematics

A-07908-60013-2 Test procedures

A-07908-60013-3 Debug procedures

E-07908-60013-20 Modification Drawing

07908-80013 Tape masters

Production Changes:

48-4052 change R144 to 2.15K (0698-0084)

48-4086 add 2 capacitors and term-pin

48-4142 change resistor pack (DIP) to discrete resistors

48-4215 fuse change to normal blow fuse

48-4837 change VR149 to 5.10v 1% zener diode

48-6065 Rev E board made with 1/2 oz. copper

HEWLETT-PACKARD CO. hp

INTRODUCTION:

This article will provide information concerning the eligibilty of the rectifier board for revision and also concerning the revisions themselves.

REVISABLE ASSEMBLIES:

The first assembly which may be revised is B-2108. All prior assemblies are to be scrapped.

REVISIONS:

B,C-2108	48-4052,4086
B,C,D-2119	48-4142
B,C,D-2132	48-4215
B,C,D-2220	48-4837
B,C,D,E-2220	48-6065

CURRENT ASSEMBLY:

B,C,D,E-2220

HEWLETT-PACKARD CO. hp

PROCEDURE:

1.0 Inspect all boards for general mechanical and cosmetic defects per A-5950-9205-1. Repair all component malfunctions.

2.0 Identify all boards with the following logo:

07908-69013
2220

to replace existing logo for date codes 2108 or later.

3.0 Affix, near the logo, a 7120-5480 label which has been stamped with the month and year of final inspection.

4.0 On board revision: B,C-2108 (to get 2119)

a) Remove U181 and replace with header (1251-0554) and six discrete resistors according to mod. dwg. D-07908-60013-20.

4.1 On board revision: B,C,D-2119 (to get 2132)

a) Replace: F195 with 2110-0523 (10A).
F290 with 2110-0523 (10A).
F291 with 2110-0048 (15A).

4.2 On board revision: B,C,D-2132 (to get 2220)

a) Replace VR149 with 1902-0689
(Non-Mandatory Change)

4.3 On board revision: B,C,D,E-2220

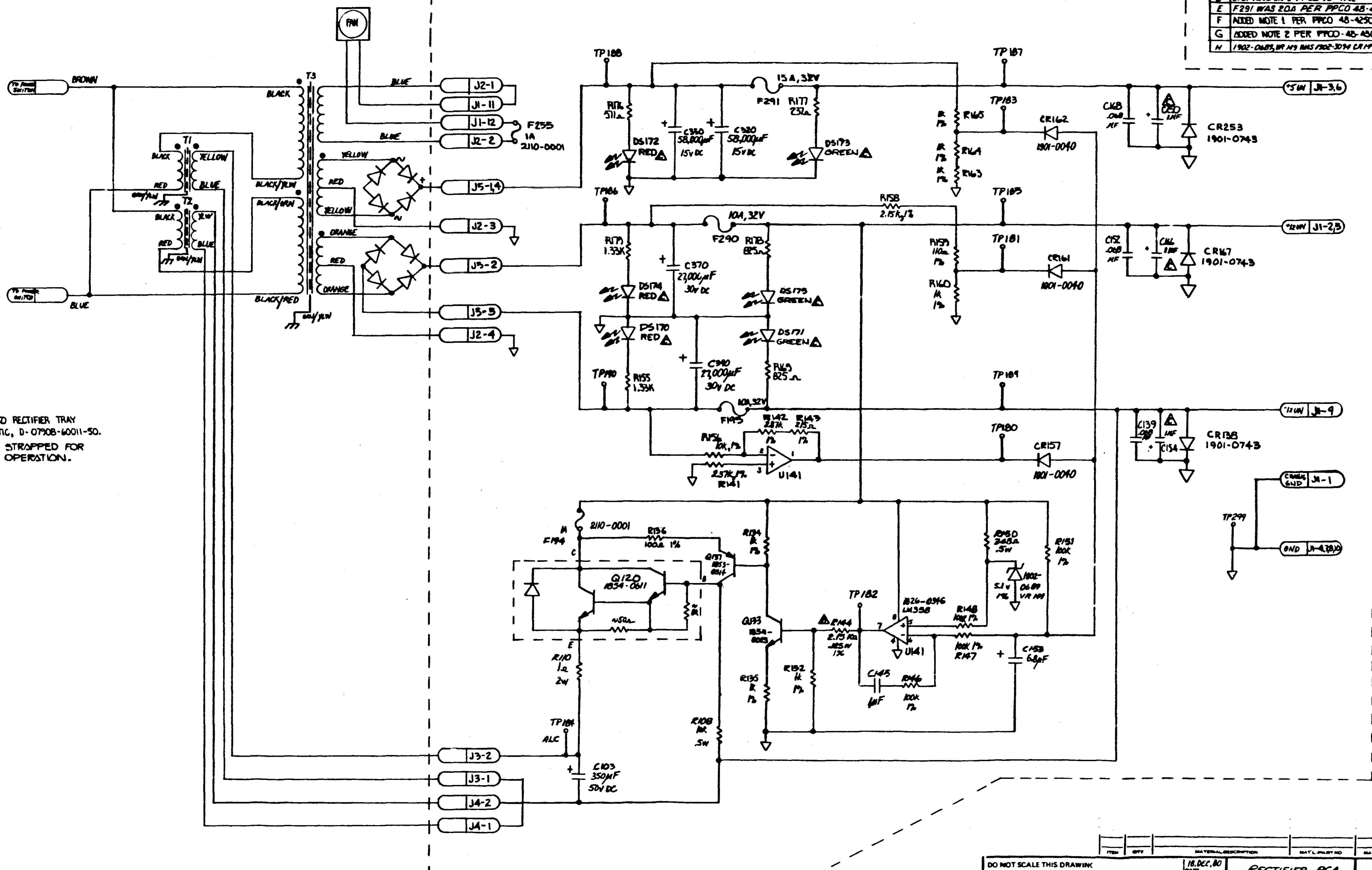
a) Current Assembly.

5.0 Test per A-07908-60013-3

C	48-4837	sr/ML	06-10-82	MODEL 7908	STK # 07908-69013
	48-6065	db/ML	01-05-83	UPDATE/REVISION PROCEDURE	
E	48-6229	sjb/ML	03-03-83	BY	DATE MAY 16, 1984
	P.C. #	APPR	DATE	APPD	SHEET # 4 OF 4
REVISIONS				SUPERSEDES	DWG # A-07908-69013-1

B-07908-60013-50

LTR	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	R144 WAS 4.64 k 1% PER PPCO 48-4032		
C	ADD COLOR FOR LED'S: MOD TRACES ADDED PER PPCO 48-4066		4/1/81
D	U161 WAS 1K J PPCO 48-4142		
E	F291 WAS 20A PER PPCO 48-4215		
F	ADDED NOTE 1 PER PPCO 48-4250	ML	
G	ADDED NOTE 2 PER PPCO-48-4308	KT / ML	10/29/81
H	1902-0683, VR 149 WAS 1902-3094 CR 149 PC 48-4837	ML	6-16-82



1. REFER TO RECTIFIER TRAY SCHEMATIC, D-07908-60011-50.
2. SHOW STRAPPED FOR 110V OPERATION.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 000

DATE 18.DEC.80

25.FEB.81

2/25/81

TITLE RECTIFIER PCA SCHEMATIC

NEXT ASSEMBLY

FINISH

SCALE

HEWLETT PACKARD

PART NUMBER 07908-60013

B-07908-60013-50

SHEET 1 OF 1

P/N 07908-60012

POWER INTERCONNECT PCA-A10

Series Code B-2120

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 07908-60012
07908-68012

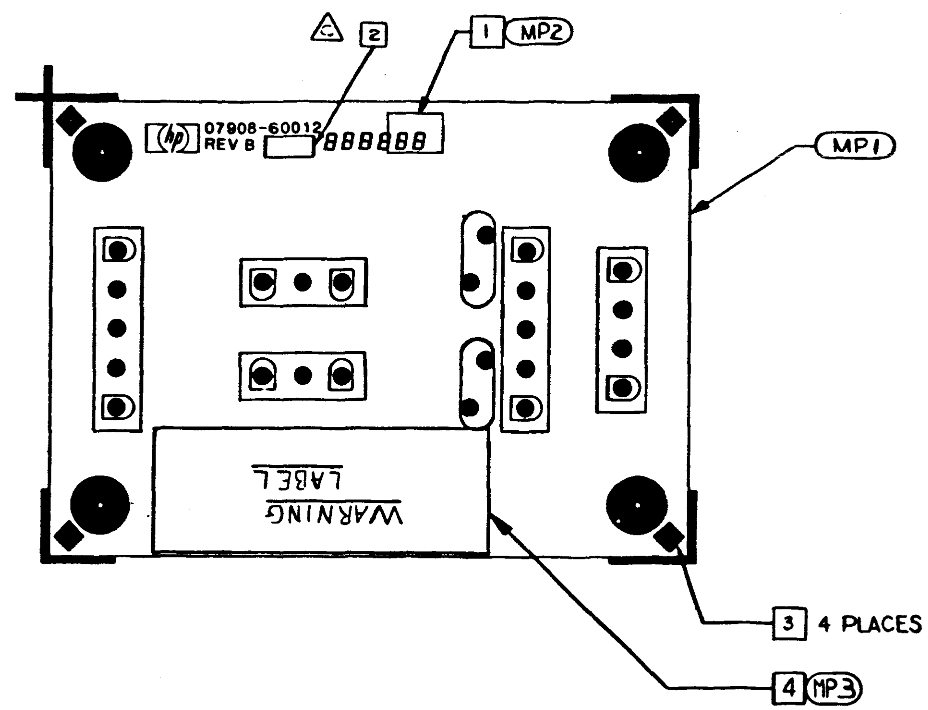
DATE CODE : B-2120

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
J1	1251-6832	CONN 5-PIN M
J2	1251-4781	CONN 3-PIN M
J3	1251-4781	CONN 3-PIN M
J4	1251-6832	CONN 5-PIN M
J5	1251-3837	CONN 4-PIN M
MP1	07908-80012	BD-ETCHED
MP2	7120-6830	LABEL-INFO
MP3	7120-4567	LABEL-WARNING
RV1	0837-0213	VARISTOR
RV2	0837-0213	VARISTOR

END OF MATERIAL LIST.

F-07908-60012-1

LTR	REVISIONS	APPROVED	DATE
A	AS ISSUED		26FEB81
B	REV NOTE 2. DATE CODE WAS 2108 PER PC 48-4161	AHS 2CM	6/12/81
C	CORRECTED DATE CODE LOCATION; ADDED KEYING MARKS PER PPCO. 48-4313	RAT ML	10/22/81



F-07908-80012-3 PAD MASTER 3-13-81

REFERENCE DRAWINGS:
SCHEMATIC C-07908-60012-50

UNLESS OTHERWISE SPECIFIED:

THIS BOARD CONFORMS TO CORPORATE AUTOMATIC INSERTION STANDARDS

NOTES:

1. INSTALL (MP2) AFTER LINE TEST.
2. OPR. 264 :MARK ASSEMBLY DATE CODE 2120
3. OPR. 265 :MASK PRIOR TO LOADING.
4. OPR. 266 :TOUCH UP. INSTALL (MP3) UPSIDE DOWN IN RELATION TO GRAPHICS.

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO	MAT'L-DWG NO	MAT'L-SPEC

3-13-81
26FEB81
2/26/81

ASSEMBLY POWER INTERCONNECT

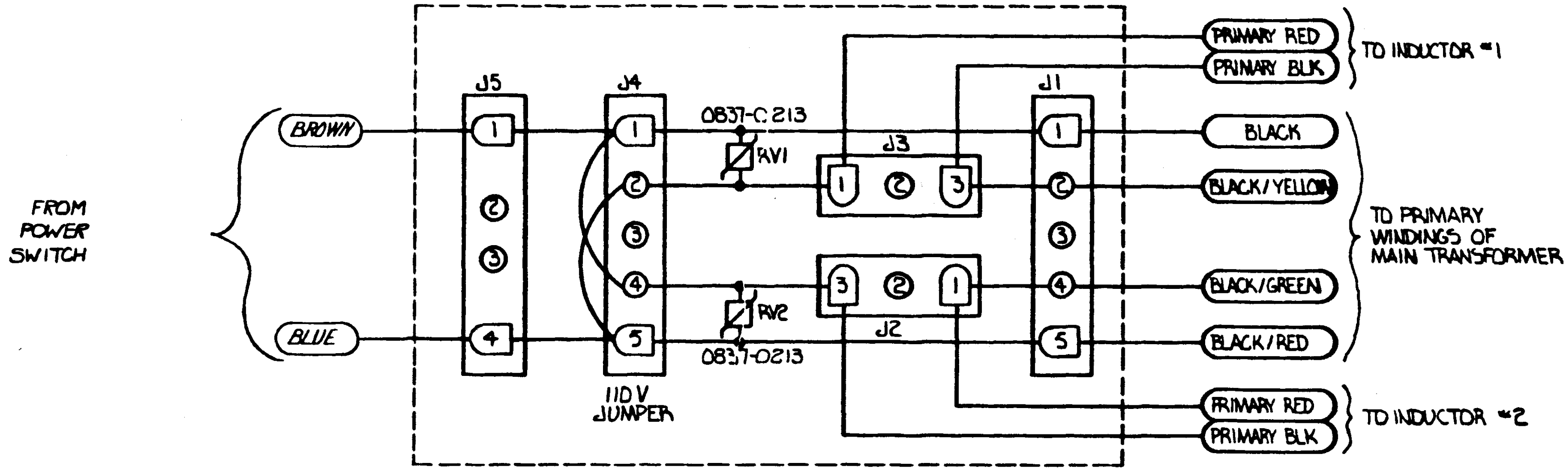
HEWLETT PACKARD

PART NUMBER 07908-60012

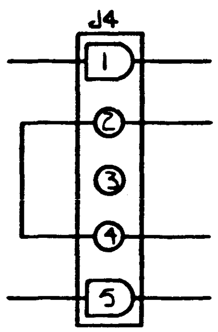
F-07908-60012-1

SHEET 1 OF 1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		26 FEB 81
B	MODIFIED PER PCO 48-4250	JDC ML	9-2-8
C	PART 0837-0213 WAS 0837-0191; ADDED WIRE COLORS; CORRECTED KEYING MARKS PER PPCO 48-4313	KAT/ ML	



NOTE:
1. FOR 220V OPERATION, CONNECT JUMPER AS SHOWN BELOW.



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO	MAT'L-DWG NO	MAT'L-SPEC

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 808

DATE: 2-24-81 / 26 FEB 81 / 2/26/81

TITLE: POWER INTERCONNECT -SCHEMATIC-

HEWLETT PACKARD

NEXT ASSEMBLY

PART NUMBER: 07908-60012

FINISH

SCALE

C-07908-60012-50

SHEET 1 OF 1

P/N 07908-60340

TAPE MODULE

Series Code 2349

ER43 DH:C6/50A

HEWLETT-PACKARD CO. / hp /

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline). (L430)

LTR	REVISIONS	DATE	INIT	M F
A	AS ISSUED PER PCO 48-6074	12/16/82	clr/ML	M

A	48-6074	clr/[illegible]	12-16-82	MODEL 7908	STK # 07908-60340
				HCD-75 DMI ERS	
				BY	DATE FEB 13, 1984
LT	P.C. #	APPR	DATE	APPD	SHEET # 1 OF 21
REVISIONS				SUPERSEDES	DWG # A-07908-60340-2

HCD-75 DRIVE MODULE INTERFACE ERS
(07908-60140)

GENERAL DESCRIPTION

This document describes the HCD75 (3M Company Product No.) cartridge tape drive interface to our Controller. A brief description of the DC600HC preformatted cartridge used by the drive is also included.

The Controller referenced in this document consists of the following elements:

MICROPROCESSOR Assy
(or equivalent)

DMA Assy
(or equivalent)

TIB Assy

The cartridge is pre-recorded by a full width recording device which writes completely across the full one quarter inch width of the tape. The 600 foot tape length is divided into three areas. There is a unique "Beginning of Tape" (BOT) pattern area at the front of tape, a unique "End of Tape" (EOT) pattern area at the end of tape and a data area for user recording. The data area is divided into 4114 erased areas which are separated by identifying key marks. It is important that the BOT, EOT and short key recordings should not be erased in user recording. The 4114 erased areas between keys are each approximately 1.75 inches long. Four thousand ninety six of these areas can be recorded by the user on 16 tracks across the width of the tape. A movable write-read head on the drive will select the desired track. Fifteen areas are reserved for system diagnostics and usage.

GENERAL DESCRIPTION (Continued)

Serpentive recording is used. This method writes and reads forward on even numbered tracks, and reverse on odd numbered tracks (the 1st track is 0). This method saves rewind times by using the 600 feet of recording area in a continuous flow.

The keys identify the record areas in ascending numerical order from BOT. Key zero is near BOT. Key 4112 is near EOT.

Nearly gapless recording can be employed by the user. Small gaps must be provided to inhibit the possibility of speed variations accidently erasing the keys. A read operation is always required before writing occurs. The recording zone must first be identified.

The drive module is cabled with a 50 pin flat cable. No termination resistors are used, but tri-state drivers will function well over a maximum 15-foot cable length. The Controller has all its drivers in the constant enable mode; the drive must not see the tri-state condition. It must see only one of the two T.T.L. levels.

After a power up reset, the drive will wait for cartridge insertion and then execute an automatic cartridge load sequence. This sequence starts at the end of tape area and takes about two minutes to execute. The purpose is to condition the cartridge, set the electronic gain control, and locate a positive reference for track location. After this sequence, the drive will "park" at BOT and wait for commands.

HCD-75 DRIVE SPECIFICATIONS

MEDIA: DC600HC or DC615HC Data Cartridge

POWER SUPPLY: NOMINAL CURRENT (AMPS)

	IDLE	RUNNING	SURGE
+5VDC -2%/+5%	1.5	1.5	
+12VDC -5%/+10%	0.13	0.75*	3.5 (45 MS,@ 60 ips)
		1.0 *	3.5 (80 ms,@ 90 ips)
		1.0 STEPPING*	

* ADDITIVE DEPENDING UPON OPERATIONS

TYPICAL POWER: 9W IDLE

18W RUNNING

WEIGHT: 6 POUNDS

SERVO: 60 ips +/- 3% forward-reverse, 75 mS ramp.
90 ips +/- 3% forward-reverse, 100 mS ramp.

HCD-75 DRIVE SPECIFICATIONS (Continued)

HEAD STEPPER: 0.00078 inch head movement per step.

19 steps per track, driven at 100 steps per second.

16 tracks on 1/4 inch tape.

HEAD: Single track, ferrite construction.

RECORDING METHOD: Serial M.F.M. 10,000 f.r.p.i. max at 60 i.p.s.

TRANSFER RATE: 60 K bits per second (exclusive of gaps).

CARTRIDGE INTERLOCK: Locked when head is on tape.

Released when head is at its lowest mechanical travel.

HCD-75 DRIVE SPECIFICATIONS (Continued)

OPERATION ENVIRONMENT:

Temperature:	41 degrees Fahrenheit to 113 degrees Fahrenheit (5 degrees Centigrade to 45 degrees Centigrade)
Relative Humidity:	20% to 80% non-condensing
Max Wet Bulb Temp:	79 degrees Fahrenheit (26 degrees Centigrade)

STORAGE/TRANSPORTATION ENVIRONMENT:

Temperature:	-40 degrees Fahrenheit to 149 degrees Fahrenheit (-40 degrees Centigrade to 65 degrees Centigrade)

MEAN TIME BETWEEN FAILURE (M.T.B.F.):

Greater than 10,000 hours

HCD-75 DRIVE SPECIFICATIONS (Continued)

NOMINAL LIFETIME:

Drive Motor:	Greater than 15,000-600 ft. cartridge cycles
Head:	Greater than 50,000,600 ft. cartridge cycles
Stepper Motor:	Greater than 15,000,000 steps.

MATING INTERFACE CONNECTOR:

3M 3425	Socket Connector (50 Contacts)
3M 3469/50	Flat Cable, 15 Ft. Max.

MATING POWER CONNECTOR:

MOLEX 09-50-3041, housing and three MOLEX 2 GL pins.

Minimum 16 GA. wire, 4 ft. max.

MATING INDICATOR CONNECTOR:

MOLEX 22-01-2085, housing and eight MOLEX 08-56-0110, pins

HCD-75 DRIVE INTERFACE

COMMAND LINES CMD07 through CMD00

The eight command lines (07m.s.b.) convey the command which the selected drive is to execute. These lines are T.T.L. high true for a binary one. They must be stable on the leading edge of the minimum one microsecond long CSTROBE pulse.

CSTROBE Line

The command strobe line is a minimum one microsecond long T.T.L. positive going pulse which the Controller sends at command transfer. The command data shall be stable on the leading positive edge. The drive will accept the command on the negative going trailing edge.

CACKN Line

The command acknowledge is a positive going T.T.L. pulse which is used to synchronize command transfers. The leading positive edge of command acknowledge will occur on the trailing edge of command strobe. The Controller must wait for the trailing negative going edge of command acknowledge before sending the second byte of a command or before testing status of execution for the present command.

HCD-75 DRIVE INTERFACE (Continued)

STATUS LINES ST07 through ST00

The eight status lines (07m.s.b.) convey primary and secondary status as well as memory read data from the selected drive. These lines are T.T.L. high true for a binary one.

Normally these lines have primary status in real time and ST07 is a 0. They can then be sensed at any time without acknowledge. If a drive fault condition occurs, secondary status will appear and ST07 will be a 1. Secondary status must be acknowledged. If data is requested, the lines must be sampled and acknowledged only after SSTROBE goes low.

STROBE Line

The status strobe line is a T.T.L. compatible level which is used as a drive busy flag. Status strobe must be low before a command will be accepted by a selected drive. When a command is transferred, status strobe will go high before the trailing edge of command acknowledge. Status strobe will remain high during execution of the command. Status strobe will return low only after command execution is over or when a drive fault has occurred during the execution of the command. For the four motion commands 31, 34, 37, 3A, execution is over after the drive has achieved the requested operating speed.

HCD-75 DRIVE INTERFACE (Continued)

SACKN Line

The status acknowledge line ia a T.T.L. compatible pulse which is used by the Controller to acknowledge certain drive status transfers. When issued, it is a positive pulse of one microsecond minimum duration. The Controller need only acknowledge these status transfers:

a) Secondary status drive fault transfers as indicated by ST07 = 1.

b) Memory read data transfers upon completion of a 76 command.

It should be noted that drive fault conditions are not tested during (b) above so that ST07 = 1 will not be confused with secondary status. The drive will always revert back to primary status after acknowledge.

SELECT LINES SEL1 AND SEL0

The select lines (1m.s.b.) are T.T.L. high true for a binary one. They are used to select one of four drives for use. They must be stable for all data, status or command transfers. Only one drive at a time can be on the interface.

HCD-75 DRIVE INTERFACE (Continued)

RESET LINE (Causes cartridge load sequence at all drives).

The Reset line is a T.T.L. compatible pulse which is controlled by the Controller. When issued, it must go high and remain high for one of two designated periods of time. The pulse must have clean T.T.L. compatible edges that do not ring. The trailing negative going edge will cause all drive units to initialize their programs. Communication is lost for 500 microseconds. The drives will once again be able to communicate after this time interval as signaled by SSTROBE going low. These reset pulse durations apply:

(a) During power interruption, reset must go high and remain high for at least 100 msec after power has once again stabilized.

(b) During power stable conditions, the Controller may choose to reset. The pulse must then remain high for 10 microseconds. If head reference has not been lost the drive will not execute the auto load sequence. Drive motion will stop, status will be cleared, and the drive will be receptive to commands.

READ DATA LINE

The read data line is a T.T.L. compatible signal line on which the selected drive places the same M.F.M. polarity signal on playback as was written on tape originally from the write data line. The use of this line is gated by drive select and by RW enable high.

RW ENABLE LINE

This line is a T.T.L. compatible signal line which the Controller places low to write and high to read data at the selected drive.

HCD-75 DRIVE INTERFACE (Continued)

WRITE DATA LINE

The write data line is a T.T.L. compatible signal line on which the Controller places the M.F.M. write data pattern to be written at the selected drive.

DRIVE INTERFACE PIN ASSIGNMENTS

All odd pins 3 through 49 are ground.

1	CMD00	26	ST02
2	CMD01	28	ST01
4	CMD02	30	CSTROBE
6	CMD03	32	ST00
8	CMD04	34	SACKN
10	CMD05	36	RESET
12	CMD06	38	WRDATA
14	CMD07	40	SSTROBE
16	ST07	42	SEL1
18	ST06	44	SEL0
20	ST05	46	CACKN
22	ST04	48	RDDATA
24	ST03	50	RW ENAB

DRIVE POWER CONNECTOR PIN ASSIGNMENTS

1	+12V	3	KEY
2	GROUND	4	+5V

INDICATOR CONNECTOR PIN ASSIGNMENTS

1	+5V	5	CART IN AND LOCKED
2	FILE PROTECTED	6	DRIVE FAILURE
3	SPARE	7	CARTRIDGE FAILURE
4	DRIVE SELECTED	8	GROUND

HCD-75 STATUS CODES

The HCD-75 presents two different groups of status codes, primary and secondary. Primary status is presented in real time as the drive is executing commands or is idle. Primary status indicates normal drive operating conditions and is always available on the status lines except for the times indicated below. Secondary status indicates drive or cartridge failure.

(a) Secondary status is placed on the status lines along with STTROBE low. Secondary status will remain until acknowledged, then primary status is returned.

(b) Memory data is placed on the status lines at the end of a 76 command execution and stays until acknowledged. Primary status is then returned.

When data is requested, SSTROBE will go low to indicate that data is ready for transfer. Otherwise, status can be read at any time. The sign bit ST07 should be tested (except for the 76 command) for positive or negative indication to tell whether primary or secondary status is being presented. Primary status is a low (0 bit or plus polarity). Secondary status is a high (1 bit or minus polarity).

HCD-75 STATUS CODES (Continued)

PRIMARY STATUS

ST07	Always 0, low, positive sign polarity.
ST06	Tape at requested operating speed.
ST05	Head moving
ST04	Cartridge is not ready for use.
ST03	Reserved, except that during Auto load this bit is true (=1) for a file protected cartridge.
ST02	Beginning of tape
ST01	End of tape
ST00	Cartridge automatic load sequence is in progress.

HCD-75 STATUS CODES (Continued)

SECONDARY STATUS

ST07	Always 1, high, negative sign polarity
ST06	Illegal command
ST05	Abnormal drive motor load
ST04	Abnormal tachometer feedback
ST03	Rom checksum or ram error
ST02	Stepper motor error
ST01	Off tape
ST00	Read amplifier or electronic gain control error.

After the acknowledgement of any secondary status error, except illegal command, the cartridge will be unlocked and the drive will go not ready. The drive will then respond only to:

- a 76 commands
- b Write memory commands
- c 4F command
- d Reset
- e Cartridge out - then cartridge in

Illegal commands will stop motion; however, normal operation can be resumed.

HCD-75 DRIVE COMMAND LIST

HEX CODE		NO. OF BYTES
04	Put out drive L.E.D.	
07	Put out cartridge L.E.D.	
0A	Unload cartridge (go to E.O.T. then unlock). This command can be used to abort the auto load sequence.	
10	AGC - 14%	
19	Light the drive fault indicator	1
1C	Light the cartridge fault indicator	1
*1F	Head up one step (+127 step tr offset max)	1
*22	Head down one step (-127 step tr offset max)	1
25	A.G.C. -7%	1
28	A.G.C. nominal	1
2B	A.G.C. +7%	1
2E	A.G.C. +14%	1
31	Run tape forward at 60 i.p.s.	1
34	Run tape forward at 90 i.p.s.	1
37	Run tape reverse at 60 i.p.s.	1
3A	Run tape reserse at 90 i.p.s.	1
3D	Stop tape motion	1
43	Unlock the tape cartridge (stops motion). This command can be used to abort the cartridge automatic load sequence.	1
46	Position tape at B.O.T. 90 i.p.s.	1
4C	Position tape at E.O.T. 90 i.p.s.	1
4F	Execute the automatic cartridge load sequence.	1

HCD-75 DRIVE COMMAND LIST (Continued)

HEX CODE		NO. OF BYTES
70	Set the read base upper byte to a value equal to the second byte of this command. The default selection with reset is 00 so that the user can read any ram cell 0000 to 00FF. This command can be used to set up a prom read transfer of any cell from C000 to CFFF. The data transfer occurs on a subsequent 76 command execution.	2
*73	Move the head to the track specified by the second byte. 00 is the lowest, 0F is the highest track position. This command will clear any head offset prior to track change.	2
76	Transfer the contents of th_ memory cell specified by the second byte (stops motion). The data transfer must be acknowledged. Ram or prom memory can be read. (See 70 command.)	

HCD-75 DRIVE COMMAND LIST (Continued)

70C0 Set prom read base C0.

7601 Read low prom revision level from location C001.

70C8 Set prom read base C8.

7601 Read high prom revision level from location C801.

7000 Set ram read base.

7602 Stop motion and report cartridge - in - place and file protect switch status on the status lines.

```
7  6 X X X X X X
|  |
|  |______________ Write permitted (High true)
|
|_________________ Cartridge in place (High true)
```

Other ram locations of user interest:

00DD Read per byte which is stored by the 70 command.
00D7 Temporary storage for secondary status of data which is passed over the status lines to the user.
00E3 Primary status storage.
00EE Current track number (00 lowest, 0F highest).

80-B7 Write the second byte into the ram cell specified by the first byte of this command. Ram memory 0080 through 00B7 can be written.

* The end sense circuits are defeated if the head is stepped while the drive is in motion. Tape could run off the hubs.

HCD-75 DRIVE-ILLEGAL COMMANDS

In the event of an illegal command, drive motion will stop. After status acknowledge is received, normal operation can be resumed. The following list will produce illegal command status:

1. The command is not in the repertoire.

* 2. A command other than write ram, 76, or 4F was attempted when the drive was "not ready", after unlocking the cartridge.

3. Write ram instructions which attempt to write in protected memory are illegal.

4. Forward motion was attempted from EOT or reverse motion was attempted from BOT.

5. The write enable line (RW ENABLE) was low at transfer.

* The 0A or 43 commands can be used to abort the cartridge auto load sequence even though the drive is not ready.

ADDITIONAL PROGRAM INFORMATION

FORTY THREE AND 0A COMMANDS

The 43 (unlock) or the 0A (unload) commands can be used to abort the automatic load sequence. They will be executed even though SSTROBE is high when issued. The cartridge will be at rest and unlocked when SSTROBE goes low. To resume the automatic load sequence, either execute a 4F command or remove then reinsert a cartridge.

HEAD OFFSET COMMANDS 1F AND 22

These commands can be used to offset the normal head reference. No writing is allowed during head offset. The head will automatically return to normal track reference after a track change command. Even selecting the same track number will return the head to normal reference, provided that the head is not stepped more than +/- 127 steps off normal. Improper track selection will result in future track changes, if these limits are exceeded.

A.G.C. COMMANDS 10, 25, 28, 2B AND 2E.

These commands can be used to alter the normal read amplifier gain. The 28 command returns gain to normal. The amplifier cannot be altered beyond +/- 14% limits.

ADDITIONAL PROGRAM INFORMATION (Continued)

SECONDARY STATUS

Memory Error

Both ROM and RAM memory are tested following reset. Memory error status is set, if either fails.

Motherboard L.E.D. Indicators

Two indicators on the front of the drive motherboard can be used to isolate possible trouble sources. One indicator is for possible drive problems, the other is for possible cartridge problems. These patterns apply:

CONDITION	DRIVE L.E.D.	CARTRIDGE L.E.D
Reset	ON	ON
Start of auto load sequence	OFF	OFF
Abnormal drive motor load	OFF	ON
Abnormal tach feedback	ON	OFF
Memory error	ON	OFF
Stepper motor error	ON	ON
Off tape	ON	ON
Read ampl. or A.G.C. error in drive	ON	OFF
Read ampl. error due to foreign cartridge	OFF	ON

HP7908, HP7911, HP7912, AND HP7914

TAPE DRIVE & CARTRIDGE

EXTERNAL

REFERENCE

SPECIFICATION

October 15, 1984

THE LINUS, THIRD ANNUAL, FINAL ERS (REV. G)

Component Specification -- Cartridge Tape Drive Oct 15, 1982

1.0 SCOPE

This specification provides engineering documentation and system user information of the operating features and performance characteristics designed into this product.

2.0 DESCRIPTION AND FEATURES

2.1 General Description

Linus is a low cost cartridge tape drive intended for back-up of low to medium range discs. Secondary uses will be a data exchange medium between HP systems, software distribution, in data/transaction logging applications, and for personal I/O.

The Linus subsystem consists of a "smart" mechanism, a half size Amigo P.C.Assy., and preformatted, removable tape cartridges. As a component, this subsystem will be integrated into the 16 Mbyte 7908, the 28 Mbyte 7911, the 65 Mbyte 7912, and the 132 Mbyte 7914 disc systems. In these products, the packaging, power supplies, and controller will be shared with the discs.

2.2 Product Features

Up to 67.0 Mbytes of formatted capacity on tape cartridges preformatted into 1K byte data blocks.

"Exclusive Or" error correction.

Linus and its associated disc are capable of direct data transfers without involving the HPIB.

Mechanical cartridge interlock engaged during tape operations.

Data blocks on any portion of tape are randomly accessable and over- writable.

Uses command set '80 disc protocol (ie locate and read, locate and write, etc.).

2.3 Mechanism Description

The tape drive module consists of the drive mechanism plus motor and head control electronics packaged together within the mechanism frame. The high capacity is achieved by positioning a single track, ferrite head via a stepper motor/lead screw to 16 track locations across the tape. The data is recorded serpentine fashion (each track recorded the opposite direction as the adjacent track) to eliminate rewind times between tracks. Head positioning and capstan motor digital servo control are accomplished via a microprocessor resident in the mechanism. The microprocessor also tests and calibrates the mechanism every time a cartridge is installed.

2.4 Cartridge Description

The cartridge is a DC600 preformatted data cartridge. (This is a 4x6 in. version of the HP mini-cartridge used in HP calculators and terminals!) Two sizes are available: The 67MB "L" cartridge with 600 feet of tape, and the 16.7MB "S" type with 150ft. of tape. The formatted blocks include space for 1K of data, error correction, block addresses, and CRC's. A mechanical write protect key is built into the cartridge also.

```
+------------------------------------------------------------------------+
|   |    |    | 65407| 65406|             | 61321| 61320|    |    |    |15
|   |--------------------------------------------------------------|    |
|   |                                                              |    | T
|   |                                                              |    | R
|   |                                                              |    | A
|   |                       "L" Cartridge                          |    | C
|   |                                                              |    | K
|BOT|                                                              |EOT|
|   |                                                              |    | #
|   |--------------------------------------------------------------|    |
|   |    |    |8177  |8178  |             |      |      |    |    |    | 2
|   |--------------------------------------------------------------|    |
|   |    |    | 8176| 8175|               | 4089| 4088|     |    |    | 1
|   |--------------------------------------------------------------|    |
|   |    |    |0     |1     |             |4086  |4087  |    |    |    | 0
+------------------------------------------------------------------------+

+------------------------------------------------------------------------+
|   |    |    | 16351| 16350|             | 15331| 15330|    |    |    |15
|   |--------------------------------------------------------------|    |
|   |                                                              |    | T
|   |                                                              |    | R
|   |                                                              |    | A
|   |                       "S" Cartridge                          |    | C
|   |                                                              |    | K
|BOT|                                                              |EOT|
|   |                                                              |    | #
|   |--------------------------------------------------------------|    |
|   |    |    |2044  |2045  |             |      |      |    |    |    | 2
|   |--------------------------------------------------------------|    |
|   |    |    | 2043| 2042|               | 1023| 1022|     |    |    | 1
|   |--------------------------------------------------------------|    |
|   |    |    |0     |1     |             |1020  |1021  |    |    |    | 0
+------------------------------------------------------------------------+

    |<------->|<----------------User Space----------------->|<------->|
    spare table          (Including Spares)                  use logs
    error log &
    diag.blocks
```

3.0 OPERATOR INTERACTION

3.1 Controls and Indicators

UNLOAD button - This button is mounted on the front panel of the tape mechanism and provides the user a way of indicating to the controller that the tape should be unloaded. When the controller senses that the button has been depressed it will:

a) During an autoload - stop the autoload and UNLOAD.

b) During a SAVE or RESTORE operation - temporarily stop those operations. If it is then pushed a second time and while the busy light is flickering, an UNLOAD will occur. If it is not pushed in 5 sec., the SAVE or RES will resume.

c) During any other active operation - invoke the unload sequence (below).

The unload sequence first requests release from the host system when release is granted, the controller updates the error logs (near the front of tape), rewinds the tape to "End of Tape" (EOT), updates the Use log, and unlocks the cartridge with an audible buzz.

EJECT lever - This slide lever ejects the cartridge out of the drive mechanism. A mechanical interlock prevents its actutation unless the cartridge has "unloaded" as described above.

*SAVE button - This button is located behind the front panel. It is intended for use by service personnel and users when the host system is down and a copy of the disc is desired. Backup is normally done with system commands.

Pushing the SAVE button will initiate a full volume transfer of the disc's contents to the in-place tape cartridge. The transfer will start from logical block zero on the disc and tape, and proceed until the disc volume has been completely transfered, or end of volume occurs on the tape. After the last block is written, a file mark is added. Mismatched volume sizes between the disc and tape are allowed within the above definition.

The 7914 will, after the first tape, prompt the user to load another tape. With this second tape the controller restarts the copy from where it left off on the disc. The address of the first disc sector stored on each tape is recorded in a tape maintenance block.

The SAVE operation starts with a request for release from the host. After release has been granted the busy light is flickered. If the button is pushed again within 5 seconds, the controller will start copying the disc data onto the tape. If no button or the wrong button is pushed, the subsystem returns to its idle state. If a data error is encountered on the disc, the best guess is sent to the tape, and the SAVE continues to completion. However, the tape is not unloaded and the flashing busy light indicates a fault. Pushing the unload button now, unloads the cartridge and clears the fault conditions. Unreadable keys on the tape are marked in the spare table and skipped. The SAVE continues to conclusion with no fault indicated, and the cartridge unloaded. If a hardware fault interupts the SAVE, the busy light flashes (if possible) and the tape is stopped. At the completion of the first tape on the 7914 the busy LED is flashed alternately fast and slow to prompt the user for another tape. If end of volume is reached on the disc a file mark is written on the tape and the tape unload sequence is invoked. If the end of the tape (second tape on the 7914) is encountered first the tape unload sequence only is invoked.

*RESTORE button - This button is also mounted behind the front panel. It functions the same as SAVE but in reverse (tape to disc). Additionally, RESTORE will stop at file marks and blank blocks. Data and hardware faults are handled analogously to SAVE. The 7914 uses the disc address written on the tape for restoration of both tapes.

BUSY indicator - This LED visible from the front panel indicates that a tape operation is in progress when it is lit. During Save and RES sequences this LED is flickered (8/sec.) while waiting for a button, flashed (1/sec) to indicate a fault, and strobed while flickering to indicate that the 7914 is waiting for a second tape.

WRITE PROTECT indicator - when lit this LED, visible from the front panel, indicates that the cartridge is write protected, and that writes to the tape are not allowed. When write protected, the controller cannot modify the system blocks on a tape so sparing, logging of errors, and tallying og total tape use are disabled.

*These switches are only used on the shared controller versions of Linus.

3.2 Cartridge Loading

The loading sequence is initiated whenever a cartridge is plugged in. The tape is moved to the beginning of tape (BOT), the drive tests itself, then calibrates itself to the particular cartridge in the mechanism. This process takes about two minutes for the "L", or about 55 seconds for the "S" cartridge. At the conclusion of this, it is ready to be accessed by the host.

3.3 Cartridge Unloading

The unload sequence (described under the UNLOAD button) has to be executed to remove a cartridge from the drive. It can take up to 80 seconds to rewind the tape to EOT for a "L" cartridge, and 20 seconds for an "S" cartridge.

4.0 HOST SYSTEM INTERACTION

4.1 Functional Description of Command Sequence

To access the tape, a starting block address, burst size and transfer length must be specified. The physical block size is 1024 bytes, and up to four blocks may be buffered by the controller. The starting address is converted internally to a two dimensional key and track address. A locate and read (or write or verify) command initiates the shortest seek to this key and track location. Seek times are 195 msec per track, about 100 msec accel. and decel. times per seek, plus about 20 msec per key traversed. (ie, to go from block 0 to block 4087 takes 80 seconds. To go from Block 0 to Block 8177 takes about 390 msec.). Seeks can take relatively long periods of time, especially if done without regard to the inherent personality of the tape.

Once the target address is reached, writes, reads and verifies are commenced in much the same manner as with discs. If the transaction overflows a track, auto seeks to the next track are done. Retries are also accomodated during reads and verifies.

Verifies can be done at the conclusion of a write transfer. They should not in general be done on a block by block basis, however, as this results in extremely poor performance, and excessive wear on the drive and cartridge.

4.2 Linus File Mark Capability

3M sells a controller for a stand alone Linus configuration which implements file mark capability. The 3M controller uses data block headers to record file marks which are requested by the user via a write file mark comand. In order to allow HP controllers to be compatible with 3M tapes, an equivalent function will be implemented on Linus.

The rules for handling file marks involve a new write file mark command, and modification to locate and read to allow termination of a transfer when a file mark is encountered. File marks are not involved in tape positioning prior to a read, write, or verify command. No skip file mark commands are implemented.

Whenever a file mark is encountered during a read, the data transfer is terminated. The End of File indication in the status request message becomes asserted when the host attempts to access the byte after the last byte in a file. Whenever EOF is encountered, a message terminator byte, "01", is sent to the host. The contents of this byte are not part of the requested data.

Unless a file mark is encountered, the length of the execution message is determined by the current value of the length parameter. If a data transfer ends on the last byte of a file, the EOF indication is saved until the host attempts to read the next byte. In this case the message terminator byte is sent in a single byte execution message. If an EOF is encountered in the middle of a data transfer, that transfer is terminated and EOF occurs immediately. In this case the message terminator byte is appended to the data message. The length of the execution message is never longer than the length parameter specification. Burst mode operation is independent of the rules involving file marks.

4.3 Defect Handling

Two types of media errors are possible with the Linus tape : an unreadable key for a given block and an unrecoverable data error. Bad keys are relatively common (0 - 10 per "L" cartridge) and can be detected on a virgin tape during any operation. With the internal error correction, uncorrectable data errors are rather infrequent (<1 in 10 "L" cartridges) but can only be detected during read and verify operations. To ease the handling of errors the Linus controller sets aside one block in 512 as a spare (total of 32 blocks on the "S" tape and 128 on the "L"tape). These blocks are not in the users addressing space and are only used to replace bad blocks.

Two methods of using the spare blocks are provided by the Linus controller. In the first method, refered to here as skip sparing, a bad block is spared by adding its address to a table of blocks to be skipped and removing the next available spare from the same table. This type of sparing results in minimal latency but the addresses of the blocks between the bad block and its spare are altered. In the second method, jump sparing, the bad block is directly replaced by the closest, by seek time, available spare. Any future reference to the block generates a seek to its spare requiring on the average a latency of 2.5 seconds to get to it and nearly the same time to resume with the next sequential block. This method, however, does not alter the address of other blocks and is safe for use when needed data resides beyond the bad block. In the special case when a skip spare is asked for but no spare blocks are available beyond the bad block a jump spare is substituted for the skip. There is a limit of 32 jump spares for any Linus tape.

Sparing is invoked by the host sending a Spare Block command, with a parameter byte indicating the method, or by the host writing to a known bad block after enabling Auto Sparing via the Set Device Specific Options command. Each spare operation requires the controller to rewrite a sparing information block near BOT, this will be done at the end of any transaction causing the spare but before status is returned.

4.4 Commands Supported by Linus

4.4.1 Real Time Commands

Locate and Write

Linus will execute the locate and write command in the same manner as the disc. Complete disc operations may be executed in parallel with the 'locate' portion of a Linus transaction, as described under parallel operations (to be implemented at a later date). Also note the sparing rules in section 4.4.

After completion of a write operation, the tape will automatically be repositioned to a point in front of the next block to be written. This way the seek required in preparation for a sequential write will take place in parallel with the receiving and decoding of the next command.

Locate and Read

The read and cold load read operations are executed in the same manner as the disc, with the following exceptions.

File marks will be treated as mentioned earlier.

The user will be able to configure the drive to take advantage of character count capability during reads. This is necessary for 3M controller compatability. If character counts are ignored, partial blocks will be padded with 0's to their full length during a read operation. If the character count function is enabled, the controller will skip the unfilled part of a partially written block, and proceed with the next block. The default is to ignore this powerful capability.

Upon completion of a read command, the controller will instruct the tape drive to read the next block, in case a sequential read command should follow. This is done in parallel with other controller activity, and does not impact the controller's interaction with the host.

Attempting to read a block which has never been written will terminate the transfer with a No Data Found media error.

Verify Command

The verify command on Linus operates like the disc verify command. The host should consider the following characteristics when using this command:

1 - The command will verify n logical blocks where n equals the transfer length divided by 1024. There is no adjustment for empty, partial or filemark blocks within this range.

2 - Verify will terminate immediately on an unrecoverable data error unless the bad block has been spared.

3 - Verify will not terminate on a file mark.

Copy Data

Copy data is described in the CS 80 (Feb 1981) referance manual. The following comments should be noted when using this command:

1 - When Linus is the source unit and a End of File (EOF) is encountered the Copy transaction stops and EOF status is reported.

2 - If an unwritten block is encountered while Linus is the source device, the transfer will be terminated with a No Data Found media error.

3 - The full 7914 disc image cannot be backed up on a single tape cartridge.

4 - The command is not executable on the dual controller version of the 7911, 7912 and 7914.

4.4.2 Complimentary Commands

The following complimentary commands are implemented:

SET Block Address
SET Block Displacement
SET Length
SET Burst
SET Retry Time
SET Status Mask
SET Device Specific Options

All of this commands function in exactly the same manner as described in the CS 80 reference manual with the following extension:

Set Device Specific Options C,R

```
 --------   --------
:00111000: :00000ASC:
 --------   --------
```

C = 0: Disable character count capability.
C = 1: Enable character count capability.

A = 0: Auto sparing disabled.
A = 1: Auto sparing enabled.

S = 0: Auto spare invokes Jump Sparing.
S = 1: Auto spare invokes Skip Sparing.

The C bit in this complementary command configures the controller to utilize the tape drive's character count capablilty. This does not impact write operations. Character counts are always written in block headers. If this function is disabled for a read operation, partially filled blocks will be padded with 0's during a read. It the function is enabled, only the filled portions of blocks will be sent to the host. The character count will be used to cause Linus to skip to the next block when all of the user data in a given block has been sent. No dummy data is synthesized.

When the A bit is set the Linus controller has permission to spare any bad blocks encountered while writing user blocks. Bad blocks are limited to those with an unreadable key and any blocks previously put in the error log. If the S bit is set Auto sparing will use the skip rather than the jump method of sparing. The skip method is recommended when the user doesn't care about any data which may reside beyond the current target address.

4.4.3 General Commands

Describe

The format of the describe message does not require modification for Linus. The number of user blocks given by describe reflect the size of the current cartridge loaded in the drive. It will be zero when no cartridge is loaded, 16352 for a "S" cartridge with spares, and 65408 for a "L" cartridge with spares. A cartridge which has never been written to or has been initialized to have no spares would be describes as having 16384 or 65536 blocks.

Release, Release Denied

The Linus controller requests release for the following events:

1 - A tape cartridge finishes auto load. Release is required to obtain controller resources to execute Linus Self Test and Table initialization routines.

2 - The operator pushes the Store, Restore, Unload or Selftest buttons. Release is of course required before any of these actons can be taken as controller resources are needed and the host may have file or directory maintenance to perform before allowing such drastic actions.

3 - The run time error table in the controller fills. The controller then requests release for maintenance so it can post the new errors.

The host grants or denies release with the appropriate command. If a controller defined timeout (~2 seconds) elapses before the host acts on a request for release the Linus controller grants itself release and proceeds as it desires.

Write File Mark C,R

```
 --------
:01001001:
 --------
```

This Real Time command causes a file mark to be written at the current position of the tape. The actual file mark indication appears as a bit in the header of a data block (1K). No data is stored in the block containing the file mark. This is a real time command.

Spare Block Command C,R

```
 --------    --------
:00000110:  :000000s1:
 --------    --------
```

s = 0: Skip spare.
s = 1: Jump spare.

This command causes the controller to spare the current target block by the method indicated in the option byte. This action includes updating the sparing table near BOT thus tape motion is involved and this command may take 90 seconds to execute. This command does not retain data in the spare block.

Initialize Tape C,R

```
 --------    --------    --------
:00110111:  :00000CWZ:  :00000000:
 --------    --------    --------
```

Z = 0: Rewrite sparing table with no jump spares.
Z = 1: Reset sparing table to initial spares.

W = 0: Initial spares are every 512th block plus a track offset.
W = 1: Initial spares are no spares.

C = 0: Runs certification if necessary.
C = 1: Does not force a certify test.

With all the option bits (Z,W,C) cleared, this command certifies a tape (if it hasn't already been certified), sets up a spare table on the tape (if one hasn't already been set up), and spares out any defective blocks discovered during the certify test. If the Z bit is cleared, but a spare table does exist on the tape, all jump spares are converted to skip spares. If the Z bit is set, the spare table is cleared and rewritten to an initial state as per bit W. In this case if N is zero there will be an unused spare for each 512 blocks and these available spares are staggered from block to block. No spares are used; thus all bad blocks are to be rediscovered. For W = 1 a null spare table is written allocating no spares on the tape. The certify test is also skipped. Sparing becomes the responsibility of the user as the controller is left with no resources for it. This option should be used only for compatibility with non-HP systems. When the C bit is set the certify test is not done. The media will return an initialized media status when loaded into a drive in this condition, even though the spare table is initialized. The command takes 15-60 minutes to execute on an uncertified tape.

The following table defines the controller activity for all possible combinations of previous tape state and format parameters.

Tape State \ C / W / Z	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
No Spare Table Not Certified	C	C	X	X	B	B	X	X
Spare Table Not Certified	C	C	X	X	O	B	X	X
Spare Table Certified	O	C	X	X	O	B	X	X

C - Certify the tape
O - Optimize the spare table
B - Build a new spare table
X - Clear the spare table

Unload C,R

```
--------
:01001010:
--------
```

When the Linus controller receives an unload tape command, the error log is written, if necessary, and the tape is unloaded. This action may require rewritting a block at BOT as well as EOT so prepare for a possible three minute wait until status is returned. The controller supports parallel disc operations during this operation.

4.5 Diagnostic Commands

The three following Diagnostic Commands are supported:

Request Status
Initiate Diagnostic
Execute Utility

With these catagories of commands, it is possible to initiate tests and gather results at both the interface and functional levels. In addition, the utilities provide a mechanism for retrival of logs, diagnostic results, and characterization of the head/media interface. The Error Rate Test Log and the Error Log will be stored in the system blocks found near the BOT (Between KEYS 9&10 and 10&11 respectively). As part of the unload sequence the "USE" Log will be updated. The "USE" log resides between physical 4107 & 4108 on the "L" tape and 1035 & 1036 on the "S" tape. A short discussion of the purpose and content of the above mentioned logs are included in the explanations of the utilities which pertain to them.

4.5.1 Request Status

```
 --------
:00001101:
 --------
```

The Request Status command operates exactly as described in the disk ERS. In summary, the Request Status command returns a 20 byte status report (in an execution message) indicating the status of the last transaction. The status request consists of a 2-byte identification field, an 8-byte error classification field, and 10 bytes of additional error dependent parameters. A summary of the format of the status report is found in the CS-80 Instruction Set Manual. A more detailed discussion of this command is provided in the CS-80 ERS.

4.5.2 Initiate Diagnostic

```
 --------     ----------------     --------
:00110011:   : LOOP PARAMETER :   :SECTION#:
 --------     ----------------     --------
  OPCODE          2 bytes           1 byte
```

The Initiate Diagnostic command will perform the phase of the internal diagnostic which is indicated by the diagnostic section number. The internal diagnostic is divided into several sections, the following two of which pertain to Linus. These tests are invoked at Power-On, and may be run individually through the Initiate Diagnostic command. TCP two Linus related diagnostic sections are specified as follows.

```
 --
: 8: - TIB MICRO Diagnostic:
 --     Functional testing of the Tape Interface Board,
        including special diagnostic mode testing.

 --
:11:  (A)-Initiate AUTO-LOAD Sequence:
 --         Performs the OEM Self Test, tensioning, and Head
            alignment functions with the cartridge in place.

      (B)-DMA/TIB MACRO Diagnostic:
            Tests all control lines and the serial data
            path between the DMA and Tape Interface Boards

      (C)-TIB/LINUS MACRO Diagnostic:
            Tests control and data paths between the Tape
```

Interface Board and the LINUS mechanism... includes a short R/W and command/response tests. The R/W test will seek to a diagnostic key near BOT and attempt to write a test pattern on 2 of 16 tracks. Tape length is also retrieved from the "manufacturer's block".

4.5.3 Execute Utility

```
 --------    --------        ----     ----
:001100XX:  :u OPCODE:      :    :   :    :
 --------    --------        ---- ..... ----
             1 BYTE         0-4 PARAMETER BYTES
```

XX = Execution Message Qualifier
 00 -> No Execution Message
 01 -> Receive Execution Message
 10 -> Send Execution Message

The Execute Utility Command is followed by a micro-opcode which defines a variety of disc and tape utilities. Depending on the utility selected, a pre-defined number of parameter bytes may be expected to follow the utility number. Although, the interface to this family of utilities tends to be device independent, the internal algorithms do depend on the specific device. The following Linus utilities present a consistent disc/tape interface.

Pattern Error Rate Test:

```
 --------   --------   --------   --------   --------
:11001000: :  LOOP  : :  TYPE  : :TST AREA: :DATA SRC:
 --------   --------   --------   --------   --------
 u OPCODE    1 byte     1 byte     1 byte     1 byte
```

Parameter Definition:

```
LOOP     -> 1-255 = Loop Count
            0   = NOT Allowed

TYPE     -> 00 = Read only ERT
            01 = Write/Read ERT
            10 = Certification
                 (Sparing KEY errors and
                 blks with >=2 frame errors)

TST AREA -> 00 = Use Current Address &
                 Current Length.(Logical)
            01 = Specified & Next Track
                 (Phy)-(XXXX0001),
                 Where XXXX=Specified Track
            10 = Entire Tape(Phy)

DATA SRC -> Defines data source
            00 = Use Internal Pattern Tbl.
            01 = Use User defined pattern.
            10 = Use Random Data
```

This error rate test and certification utility is provided to aid in characterizing the head/media interface. Write/Read and certification tests are destructive to stored data. Tape certification includes a write/read pass on all physical blocks while sparing all blocks with a key errror or two or more frames in error. Therefore, the test area is ignored when certification is selected. The test area may be either logical, using the current address and length, or physical, specifying a pair of tracks or the entire tape. The data source may be from a pseudo-random data generator, an internal Pattern Table, or user defined by the "RECEIVE USER PATTERN" utility described later. The results of this may be recovered using the "Read ERT Log Utility". *Permanent correctable and *uncorrectable data errors are logged, including their logical addresses where possible. Since reserved spare blocks may also exhibit errors, the appropriate error counts will be incremented, but no records will be returned for those blocks because there is no corresponding logical address. The sum of the error counts (permanent and key), may therefore, be larger than the number of records returned. *Transient data errors and key errors are counted. Since the error log is written to a system block on the tape, rather than returned directly to the user, the tape must not be write protected even for a Read Only ERT. The parameters bytes for this test are position specific. Therefore, a parameter bounds error will not be set when undefined bit positions in the byte are used.

Read Error Rate Test Log:

```
 --------   --------
:11000110: :00000000:
 --------   --------
 u OPCODE    1 byte
```

The ERT Data Error Log is the standard log for all errors found while executing the Pattern Error Rate Test. The single byte "null" parameter indicates that the results will cover all blocks specified during the ERT run. The log is composed of a header which contains the number of blocks accessed and error counts, and records which contain relevant addresses and error qualifiers. This log contains data and key errors, and is kept separate from the "Run Time" Error log so cumulative errors are not a concern during testing. Records are kept for permanent errors (correctable and uncorrectable) and key errors.

Log Format:

<u>LOG HEADER</u>

```
  # of records _____________  1 byte
  # of blocks accessed ______  4 bytes
* # of permanent errors _____  2 bytes
* # of transient errors _____  2 bytes
* # of uncorrectable errors __  1 byte
```

# of key errors __________ 1 byte

LOG RECORD

ADDRESS PORTION:
Logical Block address _____ 2 bytes

ERROR PORTION:
ERROR BYTE(See definition below) __ 1 byte

```
ERROR BYTE - Bit 0 = 0 frame 1 NO CRC error
                   = 1 frame 1 CRC error
             Bit 1 = 0 frame 2 NO CRC error
                   = 1 frame 2 CRC error
             Bit 2 = 0 frame 3 NO CRC error
                   = 1 frame 3 CRC error
             Bit 3 = 0 frame 4 NO CRC error
                   = 1 frame 4 CRC error
             Bit 4 = 0 ECC 5 - NO CRC error
                   = 1 ECC 5 - CRC error
             Bit 5 = 0 ECC 6 - NO CRC error
                   = 1 ECC 6 - CRC error
             Bit 6 = 0 correctable error
                   = 1 uncorrectable error
             Bit 7 = 0 Frame error
                   = 1 Key error
```

* A PERMANENT ERROR is a block with one or more defects in the data area. Most defects are correctable. A block with 2+ defects in non-adjacent frames is an UNCORRECTABLE ERROR. A TRANSIENT ERROR is any frame error that disappears in less than three retries.

As a suggested output format for the ERROR byte, display only those categories of errors which are "active"(Bit position = 1).

Read Error Log

```
 --------   --------
:11000101: :00000000:
 --------   --------
 u OPCODE    1 byte
```

This Run Time Log provides a history of performance for a given tape. The "null" parameter byte indicates the results are over all tracks and all blocks. The Clear Log Utility (Described later) will clear this log of all records and counts. The only records kept are for uncorrectable and key errors. This log is stored near BOT, between KEYS 10 & 11, in the following format. Certification is zero for uncertified tapes; otherwise greater than zero.

LOG FORMAT:

LOG HEADER

# of records ______________________ 1 byte

# of uncorrectable errors _________ 1 byte
# of key errors ___________________ 1 byte
Type of certification* ____________ 1 byte

LOG RECORD

THE LOG RECORD IS OF THE SAME FORMAT AS THAT KEPT FOR THE ERT LOG.

*Possible values for the "Type of certification" are:
0 = Not certified
1 = 3M certified
2 = HP factory certified
4 = Certified on-line

Read "USE" Log

```
 --------
:11000111:
 --------
```

The "USE" log provides a history of the total tape activity. It contains two entries, auto-load count and number of blocks accessed. This log resides at physical block 1035 on the "S" tape and 4107 on the "L" tape. The log is only updated during the unload sequence and will therefore remain unchanged during any single session where a tape is inserted. To preserve an accurate record of tape activity, this log may not be cleared. The "USE" log has the following format:

LOG RECORD

Count of Auto-load sequences
performed on this tape ________ 2 bytes
Count of blocks accessed ________ 4 bytes

Read Drive Tables

```
 --------      ------------
:11000100:    :Table Numb r:
 --------      -------- --
```

This command will return the RAM values stored in the drive table specified by the p ameter value. This information can be used to achieve a understanding of the drive state. The possible parameter oyte values and the associated tables are:

Table Number = 10 Manuf ture's Block table
= 11 Spare lock Table
= 12 Copy Start Address

MANUFACTURER'S TABLE

The manufacturer's table is the only system block not written by HP controllers. It is written by the manufacturer as part of media formatting. Unlike the other blocks on the tape it is written in the same direction on all tracks (moving towards EoT) between keys zero and one. Its data is recorded in 7 bit ASCII code with the most significant bit set to zero. The format is as follows:

```
<CR><LF>DC6##HC
<CR><LF>####
<CR><LF>Format c<BS>O MINN. MINING AND MFR. CO,
<CR><LF>XXXXXXNNNNNNNNNN
<CR><LF><ESC>
```

Line 1 Cartridge type - ## is 00 for the long tape
or 15 for the short tape
Line 2 Number of user blocks per track, 4096 or 1024
Line 3 Copywrite notice
Line 4 Cartridge identification code
XXXXXX is the manufacturer's control code
NNNNNNNNNN is the date code

The cartridge identification code contains both numeric and alphabetic characters and is unique for each cartridge.

The symbols <CR>, <LF>, <BS>, and <ESC> represent the carriage control, linefeed, backspace, and escape characters respectively. The manufacturer's block is used by the Linus controller to determine the length of the tape just loaded. The full block is available to host computers thru the use of a utility.

SPARE BLOCK TABLE

The Spare Block table contains the physical addresses of all those blocks which are spared. It may be cleared by using the Initialize Tape CS-80 command with the appropriate parameters. The Table is provided to inform external diagnostic utilities which areas of the cartridge are bad but are not mentioned in the Error Log, because physical addressing is not available to the host. There is no direct way to verify these blocks.

TABLE HEADER

# of table entries ________ 1 byte

TABLE RECORD

Block number ____________ 2 bytes
Track number ____________ 1 byte

COPY START ADDRESS

This table is holds a six byte logical address that indicates where an image restore of this tape should begin on the disc. The address is given in block mode with the most significant byte sent first.

Receive User Pattern

```
 --------
:11010001:
 --------
```

This utility will accept 64 bytes of data (passed from the host) and write them to the controller RAM area for later use with the error rate test.

Clear Logs

```
 --------      ----------
:11001101:    : LOG CODE :
 --------      ----------
```

This utility will clear logs indicated by the parameter byte.

```
Log Code = 0   Clear the Error Log and ERT log.
         = 1   Clear the ERT log only.
```

Read Revision Numbers

```
 --------
:11000011:
 --------
```

This utility reads the firmware revision numbers for disc/tape/and controller firmware. The first byte returned is equal to the number of bytes which will follow.

Preset Drive

```
 --------
:11001110:
 --------
```

This command will force all periodic upkeep required by the device controller. This includes updating logs containing run time data errors or drive faults. This command should be issued periodically by the host, so it has control over the timing of periodic logging.

Read Error Summary

```
 --------   ------------------
:11000001: :Recent or Previous:
 --------   ------------------
 u OPCODE    1 byte
```

Parameter:

```
0 = Most resent results (1 summary)
1 = Last 4 summaries with errors.
    (Does not include current summary.)
```

This utility returns 1 or 4 (parameter dependent) 64 byte "bit maps" which represent the results of all tests executed. Where the Linus Drive is the only unit besides the controller, the "0" parameter is the only valid parameter. When the controller is common to disc and tape, the previous 4 error summaries may be cleared with the CLEAR LOGS (ALL) command issued to the disc. Since the bit positions correspond to actual errors, their definition is now in progress. One test's successful completion may depend on the results of another test, and therefore, the host may intelligently combine a list of test dependencies with these results to perform fault isolation. This utility is provided so field testing tools may intelligently adapt to field experience.

4.6 Power-On Sequence

Four separate diagnostic phases are entered during Linus System Power-On.

They are:

(1) Controller (Including the Tape Interface board) power on diagnostics.
(2) Linus Auto-Load Sequence.
(3) Tape Interface Board to Linus interface tests (Macro-diagnostics)
(4) System blocks are loaded into controller RAM.

The Linus auto-load sequence (2), begins when a tape is detected in the drive. If a tape is present at power-on, the auto-load sequence and the controller power-on diagnostics execute in parallel with the disc coming on-line before the more lengthy auto-load is complete. In the normal situation, the controller will be "up" when the tape is inserted. For this case, phase (2), (3), and (4) summarize the Linus Tests before coming on line.

In the first phase, the controller and disc (if present) "board and interface" tests are executed. This includes controller to Tape Interface Board Data and Control Path Testing. This testing occurs whether or not a tape is present in the drive. In the second phase, the Linus drive performs tape tensioning and head alignment functions, as well as checking internal RAM and registers for proper operation. This phase is initiated when a tape is inserted or found (during system power-on) in the drive. The functions are all performed with the Linus's internal micro-processor.

In the third phase, the controller attempts to communicate with the cartridge using a short Read/Write test. This test is non-destructive, using blocks invisible to the user. In the last phase, the controller reads system information from the Linus cartridge into the controller RAM. This information includes the manufacture's block and Spare tables.

LINUS POWER-ON SEQUENCE

```
   Tape      ---------------            ---------------
Presence :    LINUS        :          :   CONTROLLER   : Power-On
Detected :  AUTO - LOAD    :          :   POWER - ON   :<-Detected
    --->:     BEGINS      :           ---------------
         :                 :                 | |
         :                 :                  V
         :                 :          -----------------
         :(TAPE PRESENCE   :        : IF DISC PRESENT,  :
         : DETECTION MAY   :        : IT COMES ON-LINE. :
         : OCCUR AT POWER  :        : OTHERWISE, WAIT   :
         : ON OR ANYTIME   :        : FOR AUTO-LOAD TO  :
         :  THEREAFTER)    :        : COMPLETE          :
         :                 :          -----------------
          ---------------                   | |
         :  AUTO - LOAD    :                 | |
         :    COMPLETE     :                 | |
          ---------------                   | |
               | |                           | |
                V                             V
               VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                           | |
                            V
          -----------------------------------
         :   IF A SINGLE CONTROLLER EXISTS    :
         :  FOR BOTH TAPE AND DISC, IT MUST   :
         :REQUEST RELEASE OF THE ON-LINE DISC:
          -----------------------------------
                           | |
                            V
               -------------------------
               :TIB/LINUS MACRODIAGNOSTIC:
               -------------------------
                           | |
                            V
            -------------------------------
            :SYSTEM BLOCKS => CONTROLLER RAM:
            -------------------------------
                           | |
                            V
                ***********************
                * LINUS COMES ON-LINE *
                ***********************
```

5.0 PERFORMANCE SPECIFICATIONS

5.1 DATA CAPACITY

Formatted Data Capacity:	67.0 Mbytes Per "L" Cartridge
	16.7 Mbytes Per "S" Cartridge

5.2 Data Transfer Rate

Average Data Transfer Rate:	35.0K bytes/sec. (2.1Mbyte/min)
Burst Transfer Rate:	~ 900K bytes/sec.

5.3 Access Time

Total access time is the sum of the following factors:

Track to Track Seek	195 msec/track
Key to Key Search	19.8 msec/key (1Kbyte/key)

(Worst case access is 83 sec.)

5.4 Tape Speed

Read/Write/Verify	60 ips
Search (Key)	90 ips

5.5 Recording Parameters

Encoding Technique	MFM
Bit Density	10000 bpi
Number of Tracks	16
*Number of User Blocks	65408 for "L", 16352 for "S"
Data/Block	1024 bytes

5.6 Error Rate

< 2 errors in 10E10 bits transfered, unrecoverable e.r.

* For initialized tape

6.0 ENVIRONMENTAL

The Linus tape subsystem is designed to meet the Class B requirements of the HP Corporate Ervironmental Specification A-6950-5344-1. Exceptions to this specification are noted.

6.1 Temperature

OPERATING - five degrees centigrade to forty five degrees centigrade.

NON-OPERATING - negative forty degrees centigrade to sixty five degrees centigrade.

6.2 Humidity

OPERATING - 8% to 80% non-condensing.

NON-OPERATING - 5% to 95% non-condensing.

6.3 Vibration

Operating and non-operating per DMD dwg A-5955-3439-1

6.4 Shock

11 msec, 1/2 sine wave, 30 g's non-operating.

6.5 Altitude

The unit will withstand altitudes from 300 meters below sea level to 4600 meters above sea level, operating; and non-operating to 15000 meters.

7.0 RELIABILITY

7.1 Failure Rate

The failure rate goal is 6.6% /1000 hours of power on time, and tape moving at 17% duty cycle.

7.2 Repair Time

The mean time to repair (MTTR) goal is <1 hour excluding travel time.

7.3 Average Use Estimates

Power on - 50% duty cycle

Tape in motion - 2 hours/day average

7.4 Service

No field preventative maintenance is required. The head and capstan can be cleaned by the customer using a chemical head cleaner. (Every week)

7.5 Cartridge Life

Average life of the cartridge is 2500 end to end cycles of the tape. One cycle is moving from EOT to BOT to EOT.

8.0 PHYSICAL SPECIFICATIONS

8.1 Size

Drive Module - 117mm. high x 178mm. wide x 210mm. deep

Tape Interface Bd. - 178mm. x 305mm. (1/2 Amigo size)

8.2 Input Power

5v - 3.6 amps

12v - .75 amps (4.0 amp surge)

9.0 Examples of Linus media defect handling

The following examples show how the host should interact with the Linus controller to minimize error handling problems. For these examples the tape has a bad key for block 5, a bad data area in block 10; blocks 7 and 15 are allocated as spares. The host is working with a 18 kbyte file starting at block 0.

```
L  0  1  2  3  4  5  6     7  8  9 10 11 12 13    14 15 16 17 18
 +--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+-
 |  |  |  |  |  *  |  |ss|  |  |**|  |  |  |  |ss|  |  |  |  |  |
 +--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+-
P  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20
```

```
     * - defect over key
    ** - defect in block
    ss - available spare block
    xx - block deleted by sparing
```

NOTE: P-## indicates physical block ##. Physical addresses are not accessible to the host.

L-## indicates logical block ##. All host addresses are Logical addresses.

Case 1 - Writing the file on virgin tape.

The host issues a write at 0 for 18 kbytes.

Linus writes blocks L-0 to L-4.
The Linus controller adds block 5 to the Error Log.
Linus accepts and sinks blocks L-5 to L-17.
The returned status indicates that block 5 is of no use.

The host should issue a command to skip spare block L-5.
The host then reissues a write at 0 for 18 kbytes.

Linus writes blocks L-0 to L-4.
Linus skips block P-5.
Linus writes block L-5 (in block P-6).
Linus writes blocks L-6 to L-13. (P-7 becomes a data block)
Linus skips block P-15.
Linus writes blocks L-14 to L-17. (in blocks P-16 to P-20)
Linus returns normal status as the error at block 10 cannot be detected yet.

The tape now contains...

```
L  0  1  2  3  4     5  6  7  8  9 10 11 12 13    14 15 16 17 18
 +--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+-
 |  |  |  |  |  *xx|  |  |  |  |**|  |  |  |  |ss|  |  |  |  |  |
 +--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+-
P  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20
```

Case 2 - Reading the above file.

The host issues a read at 0 for 18 kbytes.

Linus returns data from blocks L-0 to L-4.
Linus skips block P-5.
Linus reads data from blocks L-5 to L-8.
The Linus controller enters block P-10 in the Error Log.
Linus returns it's best guess for L-9, and reads L-10 to L-13.
Linus skips block P-15.
Linus reads blocks L-14 to L-17 (from blocks P-16 to P-20).
The returned status indicates unrecoverable data in block L-9.

Case 3 - Rewriting the above file.

The host reads the error log and is told about block L-9.
The host issues a Spare Block L-9 command, with jump option.

Linus logs P-10 in its Jump block table with a link to P-15.

The host issues a write at 0 for 18 kbytes.

Linus writes blocks L-0 to L-4.
Linus skips to block P-6.
Linus writes blocks L-5 to L-8.
Linus seeks to block P-15.
Linus writes block L-9.
Linus seeks to block P-11.
Linus writes blocks L-10 to L-13.
Linus skips block P-15.
Linus writes blocks L-14 to L-17.
Linus returns a normal completion.

The tape now contains...

```
L  0  1  2  3  4     5  6  7  8    10 11 12 13  9 14 15 16 17 18
 +--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+-
 |  |  |  |  |  *xx|  |  |  |  |xx|  |  |  |  |  |  |  |  |  |  |
 +--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+-
P  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20
```

Case 4 - Reformatting the Tape

The host issues a Initialize Tape command, saving spares.

Linus logs blocks P-5 and P-10 in the skip table.
Linus clears the Jump table.
Linus returns good completion.

The host issues a write to 0 for 18 kbytes.
Linus writes blocks L-0 to L-4.
Linus skips block P-5.
Linus writes blocks L-5 to L-8 (in blocks P-6 to P-9).
Linus skips blocks P-10.
Linus writes blocks L-9 to L-17 (in blocks P-17 to P-19).
Linus reports good completion.

The tape now contains...

```
L  0  1  2  3  4     5  6  7  8     9 10 11 12 13 14 15 16 17 18
 +--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+-
 |  |  |  |  |  |*xx|  |  |  |  |xx|  |  |  |  |  |  |  |  |  |  |
 +--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+--+-
P  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20
```

Case 5 - Use of Auto sparing

Start with situation before case 1
The host enables Auto sparing with the skip option.
The host then says to write 18 Kbytes starting at block 0.

Linus writes blocks L-0 to L-4 (P-0 to P-4).
Linus detects the bad key at P-5 and skip spares that block.
The tape now maps as at the end of case 1.
Linus writes blocks L-5 to L-13 (P-6 to P-14).
Linus skips the spare block P-15.
Linus writes blocks L-14 to L-17 (P-16 to P-19).
Linus rewrites the sparing table and returns status.

Some time later the host has read the file (see case 2) and found it lacking in quality.
As the directory shows there are files present beyond this one the host enables Auto sparing with the jump option.
The host recreates the file and tells Linus to write it.

Linus writes blocks L-0 to L-4 (P-0 to P-4).
Linus skips spared block P-5.
Linus writes blocks L-5 to L-8.
Linus jump spares block P-10 to P-15 because it was logged.
Linus writes block L9 at P-15.
Linus writes blocks L-10 to L-13 (P-11 to P-14).
Linus writes blocks L-14 to L-17 (P-16 to P-19).
Linus rewrites the sparing table and returns status.

The tape is now as at the end of case 3.

10.0 LOGICAL INTERCHANGE COMPATIBILITY

Linus is compatible with the HP Logical Mass Memory Format Standard (LIF) as revised in January '81. The following notes apply to Linus when used for LIF:

1. Sector (physical block) = 1024 bytes

2. The number of usable sectors per take is readable from the DESCRIBE command (16352 for initialized short tape, 65408 for initialized long tape).

3. For writing, use skip spacing, SPARE BLOCK command S = 0. (Auto skip spacing is recommended, device specific options A = 1, S = 1).

4. On used tapes convert jump spares to skip spares, INITIALIZE TAPE, E = 1.

5. It is also recommended that a file mark be written at the third sector to prevent the disc from accidentally being "image" restored by a LIF tape.