

# **IBM**® **Field Engineering** **Maintenance Manual**

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# **2250** **Display Unit Model 1**

## PREFACE

This manual provides the customer engineer (CE) with information useful for preventive and corrective maintenance of the IBM 2250 Display Unit, Model 1. This edition updates the former edition (Form Y27-2045-0) and incorporates the graphic design feature FE supplement (Form Z27-2572).

Text in this maintenance manual is supported by references to diagrams located in the FE Diagram Manual (Form Y27-2044). The following are related manuals and reference material that may be used in conjunction with this manual:

2250-1 FE Theory of Operation (FETOM),  
Form Y27-2043  
2250-1 FE Diagram Manual (FEDM), Form  
Y27-2044  
2250-1 FE Installation Manual (FEIM), Form  
226-2022

2250-1 Illustrated Parts Catalog (IPC), Form  
123-0442  
IBM System/360 I/O Interface - Channel to  
Control OEMI, Form A22-6843  
SLT Component Circuits Manual, Form  
Z22-2798 (IBM Confidential, for release only  
to authorized persons)  
SLT Common Power Supply Manual, Form  
223-2799  
SLT Packaging Manual, Form Z22-2800 (IBM  
Confidential, for release only to authorized  
persons)

It is assumed that the CE who services the 2250-1 has had experience and/or training on the unit and is familiar with the following:

1. 2250-1 Diagnostic Programs
2. Use of oscilloscope and related tools
3. CRT Safety precautions and protective equipment

This manual has been prepared by the IBM Systems Development Division Product Publications, Dept. 520, CPO Box 120, Kingston, N.Y., 12401. Address comments concerning the manual to this address.

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To ensure personal safety and the safety of co-workers, each CE should make it a practice to observe safety precautions at all times.

The CE must be especially aware of the dangerous voltages present in a 2250-1 and of the potential hazard presented by an unprotected cathode-ray tube (CRT). Thus, the following DANGER notices appear here.

**DANGER**

Voltages of 16,000 and 450 are used in the 2250-1. Exercise extreme caution when working in the area of the high-voltage power supply and CRT's. Do not remove the high-voltage lead from the CRT following power-off until the power-off sequence has been completed. Field repair of the high-voltage power supply is limited to replacement of pluggable cards.

**DANGER**

Cathode-ray tubes are subject to implosion. Protective gear must be worn by persons working with or in the area of an unprotected CRT.

All CE's should become familiar with the general safety practices and procedures for performing artificial respiration that are outlined in CE Safety Practices (Form 229-1264).

**CATHODE-RAY TUBES - SAFE HANDLING**

Cathode-ray tubes contain a high vacuum and are subject to implosion. Such as implosion can propel flying glass, thus presenting a source of personal injury. Therefore, when handling CRT's, exercise extreme caution.

**TRANSPORTATION - HANDLING**

1. Cathode-ray tubes must be enclosed when received, transported, or moved from area to area. If they are shipped in a carton, they must be in the original carton or one of equivalent strength, securely sealed to prevent accidental opening. Also, original or equivalent packing materials and/or

forms must be placed inside the carton to properly support and protect the tube. If tubes are transported in a unit or piece of equipment, the equipment must be able to contain the glass fragments if an implosion occurs.

2. Each CRT carton must be identified with a "Danger Cathode Ray Tube-Implosion Hazard" label.
3. All persons handling tubes or in the vicinity of exposed CRT's under vacuum must wear protective gear.

**STORAGE**

1. Tubes must be kept in the carton or unit except when exposure is required for inspection or test.
2. Adequate storage area must be provided for all CRT's. Tubes should be stacked in such a manner that they cannot easily be tipped over and will not be difficult to handle when removed from stack. It is recommended that the storage area be away from the normal flow of internal trucking and pedestrian traffic.

**TESTING**

Personnel involved in testing CRT's must be instructed in the hazards involved and precautions to be observed.

**PROTECTIVE EQUIPMENT**

Persons handling or working with or near unprotected CRT's must wear:

1. Full-face shield
2. Apron, synthetic rubber
3. Gloves, welder's
4. Cape, welder's rawhide

**DEFECTIVE-CRT DISPOSITION**

No attempt should be made to repair defective CRT's in the field. A defective CRT should be properly packed and disposed of in accordance with the CRT-disposition procedures.

This chapter contains general reference data, diagnostic techniques, and service aids to assist the CE in effecting quick diagnosis and/or repair.

### SECTION 1. REFERENCE DATA

This section contains miscellaneous information that may be helpful to the CE in troubleshooting and maintaining the equipment. Most of the information summarized in Figures 1-1 through 1-5 is covered in detail in the 2250-1 Theory of Operation manual.

Class	Command Designation	Mnemonic	Hex. Code	Feature(s) Required
Control	No Operation	NOOP	03	None
	Set Audible Alarm	ALRM	0B	None
	Set Buffer Address and Stop	SBA	07	Buffer
	Set Buffer Address and Start	SBAS	27	Buffer
	Insert Cursor	CSRI	0F	Buffer Char. Gen A/N kbd
	Remove Cursor	CSRR	1F	Buffer Char. Gen A/N Kbd
	Set Program Function Indicators	SPFI	1B	Prog Funct Kbd
Write	Write Direct	WRT	01	None
	Write Buffer	WBFR	01	Buffer
Read	Read Buffer	RBFR	02	Buffer
	Read Cursor	RCSR	06	Buffer Char. Gen A/N Kbd
	Read Manual Inputs	RMAN	0E	A/N Kbd and/or Prog Funct Kbd
	Read X-Y Position Registers	RXY	12	None
Sense	Basic Sense	SNS	04	None
	Test I/O		00	None

Figure 1-1. Display Unit Commands

Mode	Order Designation	SM Byte Hex. Code	MC Byte Hex. Code	Mnemonic	Remarks
Control	Enter 2-Byte No Op	2A	80	GNOP2	2-Byte Class
	End Order Sequence	2A	81	GEOS	
	Start Regeneration Timer	2A	82	GSRT	
	Enter 4-Byte No Op	2A	C0	GNOP4	4-Byte Class
	Transfer Unconditional	2A	FF	GTRU	
Graphic	Enter Graphic Mode Point Plot	2A	00	GEPM	2-Byte Class
	Enter Graphic Mode Line/Vector	2A	02	GEVM	
	Enter Point Plot Incremental*	2A	04	GEPI2	
	Enter Vector Plot Incremental*	2A	05	GEVI2	
Character	Enter Fixed Space Size A - Unprotected	2A	40	GECF	2-Byte Class
			50	GECV	
		52	GECV		
	Enter Fixed Space Size B - Unprotected	2A	41	GECF	
		51	GEVC		
	Enter Fixed Space Size A - Protected	2A	44	GECF	
	Enter Fixed Space Size B - Protected	2A	45	GECF	
Light Pen	Enable Switch Detect*	2A	84	GESD	
	Disable Light Pen Detects*	2A	85	GDPD	
	Enable No Switch Detects*	2A	86	GENSD	
	Transfer on No Detect*	2A	FD	GTND	4-Byte Class

\*Operational only when Graphic Design feature is installed.

Figure 1-2. Display Unit Orders

Characteristics	Character Size	
	Basic	Large
Characters per line (max.)	74	49
Lines per display (max.)	52	35
Number of characters on display (max.)	3848	1715
Displayed character time* (includes average character time and adjacent character spacing).	9.2usec	11.2usec
Blank character time* (includes adjacent character spacing).	5.4usec	7.4usec
Character spacing (raster units)	14	21
Line spacing (raster units)	20	30

\*Approximate time is indicated. The display character time is for a six-stroke character. (The number of strokes for a character is variable from one to nine, but six is average.) Flyback time is not included.

Figure 1-3. Character Display Characteristics

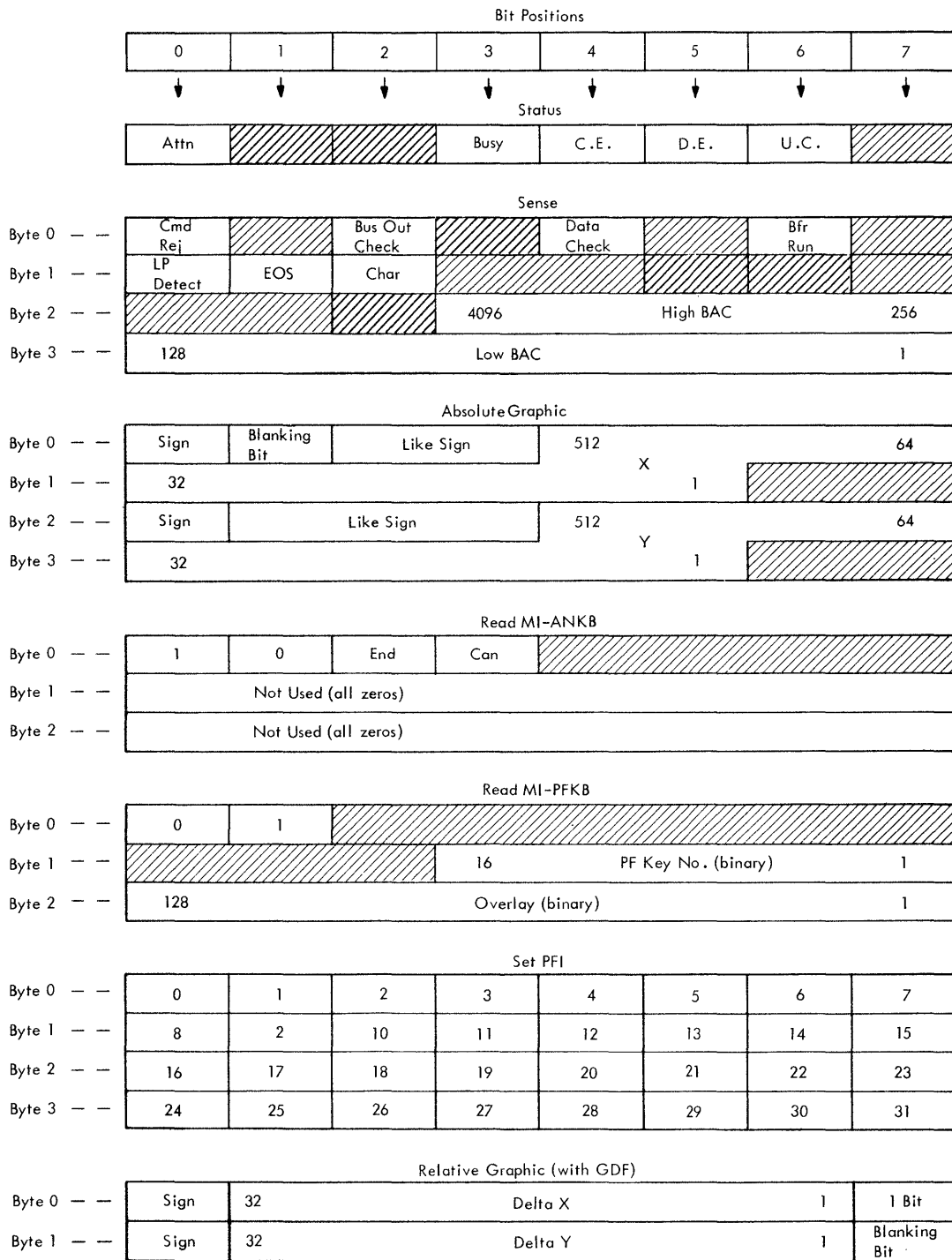


Figure 1-4. Formats



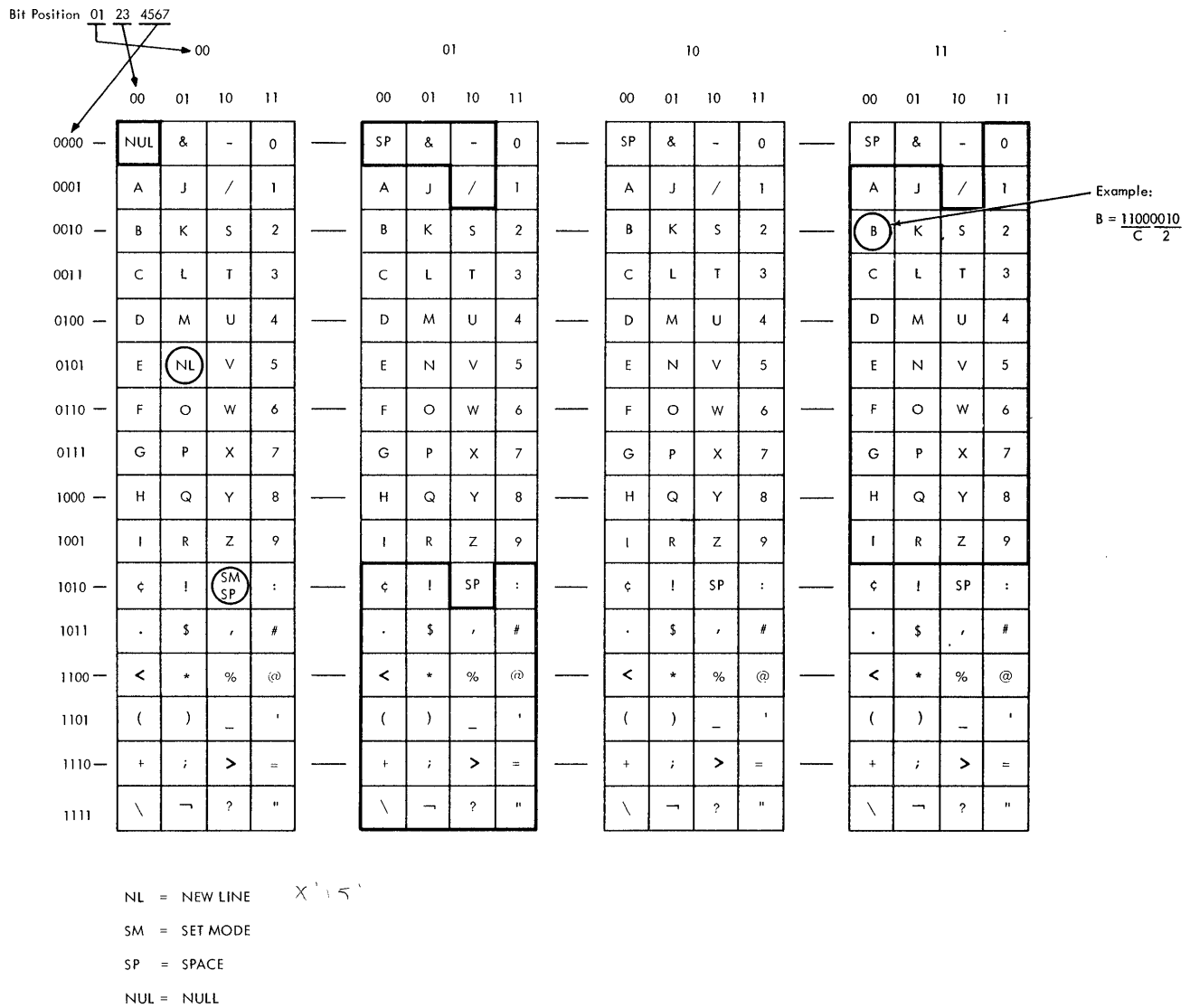


Figure 1-5. Character Set and Code Assignment

## SECTION 2. DIAGNOSTIC TECHNIQUES

This section contains diagnostic information and material that will aid in the diagnosis and correction of 2250-1 malfunctions. Included are maintenance philosophy, diagnostic programs, pattern analysis techniques, diagnostic flow charts, and a catastrophic troubleshooting procedure.

### 1.1 MAINTENANCE PHILOSOPHY

In general, the 2250-1 maintenance philosophy is as follows:

1. On-line failure detection.
2. On-line localization of failures to a functional area through the use of diagnostic programs and techniques.
3. Off-line isolation and correction of failure.
4. On-line verification of repair.

#### 1.1.1 Error Detection

The occurrence of a machine-detectable error sets the Unit Check bit (bit 6) in the 2250-1 status byte and an error-indicating bit (indicating type of error) in the 2250-1 sense byte.

The status byte is presented to the channel at the beginning of an operation to indicate acceptance or rejection of a command. The byte is also presented to the channel at the end of an operation to indicate success or failure of the operation.

The transfer of the status byte to the channel occurs as an integral part of the initial and ending sequences, whereas the sense byte is transferred only in response to a Sense command.

If the status byte contains a Unit Check, it indicates only that an error has been detected by the 2250-1. If more details regarding the error are required (as defined by the program), the Sense command is issued, and the sense byte is transferred to the channel for program interrogation. Subsequent action is determined by the program.

Error conditions that are not machine-detectable become apparent through image loss, image distortion, or the inability to perform manual intervention.

#### 1.1.2 On-Line Localization

While the unit is on-line, appropriate diagnostic routines should be used to localize failures that cannot otherwise be readily diagnosed to a functional area (digital, analog, etc.).

#### 1.1.3 Isolation and Repair

The method used to isolate a failure depends on the feature makeup of the machine. On a 2250-1 that is not equipped with the buffer feature, off-line failure isolation can be performed only when the CRT does not require a test pattern. If test patterns are required, the 2250-1 without the buffer feature must be placed in the On Line mode and must receive test patterns from the CPU.

On a 2250-1 equipped with the buffer feature, most failure isolation can be performed in the Off Line mode. By loading the buffer with appropriate diagnostic routines or test patterns (while on-line), off-line diagnosis can be performed without interfering with the CPU or the channel.

#### 1.1.4 On-Line/Off-Line - Power On/Off Switching

Units without the Isolation feature require the processor to be placed in the STOP or WAIT state before power is switched or the unit is enabled or disabled. These same conditions must exist to switch from on-line to off-line or off-line to on-line.

Units with the Isolation feature must be switched as outlined in the following paragraphs.

##### 1.1.4.1 On-Line to Off-Line Switching

1. Place ENABLE/DISABLE switch (located under the left side of CRT housing, adjacent to the usage meters) in down (disabled) position.
2. Wait for I/O INTF DSBLD indicator (green indicator on Ace panel) to light.
3. Place I/O INTF DEGATE switch on CE panel in up position.

The unit is now off-line and can be used for off-line troubleshooting procedures.

##### 1.1.4.2 Off-Line to On-Line Switching

1. Place I/O INTF DEGATE switch in down position.
2. Place ENABLE/DISABLE switch in up position (enable). The green I/O INTF DSBLD indicator should go out.

When the channel drops the Clock Out signal, the unit will be on-line.

1.1.4.3 On-Line Power On/Off Switching

1. Place ENABLE/DISABLE switch in down (disable) position.
2. Wait for I/O INTF DSBLD indicator to light.
3. Depress POWER OFF pushbutton.  
 To bring power up, depress the POWER ON pushbutton. The unit will automatically sequence itself to power on, on-line, but disabled (I/O INTF DSBLD indicator lit). To enable the machine:
  1. Place ENABLE/DISABLE switch in up position (enabled).
  2. Wait for I/O INTF DSBLD indicator to extinguish and the channel to drop the Clock Out signal.
 The unit is now enabled.

1.1.5 Repair of Field-Replaceable Assemblies

Assemblies replaced in the field should be handled as follows:

1. Analog cards should be returned to IBM Kingston for repair.
2. Power supplies should be returned to IBM Kingston for repair if not field-repairable.
3. Digital cards should be returned to SLT Repair Center for repair.
4. CRT's should be disposed of locally in accordance with General Safety CEM No. 45 (or any FE procedure replacing it).
5. Fan assemblies should be returned to Kingston for repair.
6. Buffer arrays should be returned to Kingston for repair.
7. Light pen assemblies should be returned to Kingston for repair.

1.2 DIAGNOSTIC PROGRAMS

The diagnostic programs for the 2250 Model 1 are available in two packages: one for the 2250-1 without the buffer feature and one for the 2250-1 with the buffer feature. Each diagnostic program package consists of three programs: Automatic, Manual, and Timing. Each program is further divided into independent program sections, each requiring 4,000 positions of CPU storage. The independent sections of the diagnostic programs are given in Figure 1-6. The programs can operate on any System/360 from the 8K Model 30 to the Model 92.

All sections of the diagnostic programs operate under control of the Diagnostic Monitor (DM) programs, and all standard DM options are available.

Program Number		Program Title	A - Automatic M - Manual T - Timing
With Buffer	Without Buffer*		
F760	F750	Interface Commands	A
F761		Buffer Storage	A
F762	F751	Regeneration Order	A
F763	F752	Data Sequencing	A
F764	F753	Data Registers	A
F766	F756	Graphic Display	M
F767	F757	Absolute Vector Graphic Display	M
F768	F758	Character Generation	M
F769	F759	A/N Keyboard	M
F76A	F75A	PF Keyboard	M
F76B	F75B	Light Pen Detection	M
F76C		A/N Keyboard (Cursor)	M
F76E	F75E	XCPU Tests	T

\*A buffer is now mandatory in all 2250-1 Display Units. However, several earlier machines did not have a buffer; these require F75X diagnostic series programs.

Figure 1-6. Diagnostic Programs

1.2.1 Without Buffer

1.2.1.1 Automatic Program

The Automatic program consists of four sections (Figure 1-6) and operates without manual intervention or visual checks. The various sections are designed to detect equipment failures associated with the 2250-1 channel-interface commands, the regeneration control orders, and the data registers. These sections use functional commands, status bits, sense bytes, and X and Y register feedback to detect and diagnose failures. This program does not include tests of the keyboards, light pen, character generator, or analog circuits; however, portions of the associated control logic are tested.

1.2.1.2 Manual Program

The Manual program consists of five sections (Figure 1-6) and operates with manual testing and/or visual failure-detection. The various sections are designed to functionally exercise and test the equipment not covered in the Automatic program. The sections include test patterns to visually check the graphic display and character generation logic and manual tests of the program function keyboard, alphanumeric keyboard, and light pen. Diagnosis of

failures is performed by combined program, manual, and visual means. Analog circuit alignment may be checked and corrected with the Manual program.

#### 1.2.1.3 Timing Program

The Timing program consists of one section (Figure 1-6) and performs timing and time-dependent tests in the Exclusive CPU mode of the Diagnostic Monitor programs. This section operates without requiring manual intervention or visual checks.

### 1.2.2 With Buffer

#### 1.2.2.1 Automatic Program

The Automatic program consists of five sections (Figure 1-6) and operates without manual intervention or visual checks. The various sections are designed to detect equipment failures associated with the 2250-1 channel-interface commands, the 4K or 8K buffer storage, the regeneration control orders, the data registers, and the cursor and light pen control logic. These sections use functional commands, status bits, sense bytes, and X and Y register feedback to detect failures. Though the program does not include tests of the keyboards,

light pen, character generator, or analog circuits, portions of the associated control logic are tested.

#### 1.2.2.2 Manual Program

The Manual program with the buffer feature is as described in paragraph 1.2.1.2. However, the alignment procedures can be, and should be, performed off-line.

#### 1.2.2.3 Timing Program

The Timing program has one section (Figure 1-6) which operates in the Exclusive CPU mode of the Diagnostic Monitor programs. This program performs timing and time-dependent tests of the interface and of buffer regeneration.

### 1.3 PATTERN FAILURES IDENTIFIED

An explanation of the various portions of the general alignment pattern is shown in Figure 1-7. If a display on the CRT appears to be misaligned, the failing area can possibly be determined by displaying the general alignment pattern and observing the various portions of the display as indicated in Figure 1-7.

When there is a high probability that trouble has developed in the analog section of the 2250, pattern

Portion of Display	Area under Observation
Overall Display	Blank-unblank circuitry
Full-Size Square	Overall display size; affords rough check on high-voltage status; vector dynamic intensity early blank operating; minimum position change time SS set for approximately 7.25usec; +11v clamp; +60v clamp.
X and Y Bit Staircase	Switching of bits Weight of bits Gain control status
Vector Fan	Damping Vector intensity Yoke time constant
Point Plot Fan	Damping Point plot intensity Minimum position time SS approximately correct
Character Information	Character generator bit status Character damping Character size Dynamic intensity; character Preintensification and de-intensification time delays; character overdrive
Vertical Vectors	Vector preintensification Early blank Dynamic intensity, position system

Figure 1-7. Pattern Explanation

analysis techniques (comparing patterns with known standards) can be used to locate defective cards. Figure 1-8 (sheets 1 and 2) shows six photographs with patterns in alignment. Sheets 3 through 22 of the figure show photographs of patterns that are misaligned; the failing areas are identified.

Note that these photographs represent failures in the indicated component and location only. Component failures similar to those identified can also be determined when a display appears similarly misaligned but displayed at a different location on the CRT. For example, the "X'Bit 0 Switch" with a collector to emitter shorted looks similar to an "X Bit 0 Switch" similarly shorted, but the display would appear on the right side of the CRT. If the failure cannot be determined by this pattern analysis technique, proceed to paragraph 1.4.

#### 1.4 DIAGNOSTIC FLOW CHARTS

The General Alignment program displays visual information for all operating modes. If appropriate portions of the display are viewed in conjunction

with the use of the analog flow charts (FEDM Figures 6031 through 6038), troubleshooting time should be minimized.

Figure 1-7 provides a pattern explanation to aid in understanding visual defects; however, the flow chart priority should be observed.

#### 1.5 CATASTROPHIC TROUBLESHOOTING PROCEDURE

The following troubleshooting procedure is recommended for analog failures involving multiple troubles that prevent the normal analog diagnostic programs from being loaded and displayed. The procedure should be used as a last resort and only if the analog diagnostic flow charts (paragraph 1.4) have failed to help isolate the problem.

The two programs indicated by this procedure are described in paragraphs 1.5.5 and 1.5.6. The scope sync point for the Full Square program is 02BB1J2B04; for the Character program, the sync point is 02BB1C5B03.

For this procedure, assume that the 2250-1 has every feature. On machines lacking certain features, ignore the procedural steps that apply to those features. In addition, two 2250-1 logic pages, AN101 (PN 5704665) and AN102 (PN 5704676), should be used as reference when performing this procedure.

1. Turn dc power off.
2. Remove the following analog cards on 01BA2, 01BA3, and 01AA2. Also remove the light pen amplifier card (PN 5807078) at location 01EA1 if the graphic design feature is installed.

#### CAUTION

Power must be turned off before inserting or removing any analog cards.

#### Board 01BA2

<u>Card No.</u>	<u>Location</u>	<u>Function</u>
5804248	J2/J3	X, X' Character Driver
5804247	K2/K3	X, X' Character Buffer
5804247	L2/L3	Y, Y' Character Buffer
5804249	M2/M3	Y, Y' Character Driver
5804246	J4/J5	Character Ref V
5804732	H2/H3	Char. Isolation
5804733	H6/H7	Char. Dynamic Intensity II
5800450	B6	Light Pen Verification
5801306	B4/B5	Light Pen Amplifier*
5801307	G6/G7	Blank-Unblank I
5801308	J6/J7	Blank-Unblank II
5800827	G3	Async Delay III

\*Not used when GDF is installed.

Board 01BA2

<u>Card No.</u>	<u>Location</u>	<u>Function</u>
5800825	G4/G5	Async Delay II
5800826	F4/F5	Async Delay I
5800828	H4/H5	Deskew Ref
5801305	M6/M7	Deskew Switch
5804732	L6/L7	Position Isolation
5804733	K6/K7	Vector Dynamic Intensity II
5804731	B2/B3	X, X' DC Offset II
5804731	C2/C3	Y, Y' DC Offset II

Board 01BA3

<u>Card No.</u>	<u>Location</u>	<u>Function</u>
5800831	F2/F3	X Centering and Gain
5800831	H2/H3	Y Centering and Gain
5800832	C4/C5	X Bit 0
5800832	H4/H5	Y Bit 0
5800829	D4/D5	X Bits 1 and 4
5800829	J4/J5	Y Bits 1 and 4
5801304	E4/E5	X Bits 2 and 3
5801304	K4/K5	Y Bits 2 and 3
5801303	F4/F5	X' Bits 5 through 9
5801303	G4/G5	X Bits 5 through 9
5801303	L4/L5	Y Bits 5 through 9
5801303	M4/M5	Y' Bits 5 through 9
5800833	G2/G3	Reference Voltage
5800830	E3	Deflection Overdrive
5801309	D2/D3	X, X' DC Offset I
5801309	K2/K3	Y, Y' DC Offset I
5807042	E2	X DC Offset
5807042	J2	Y DC Offset

Board 01AA2 (AVG)

<u>Card No.</u>	<u>Location</u>	<u>Function</u>
5801685	G4/G5	Bit 4
5801686	H4/H5	Bit 3
5801684	J4/J5	Bit 2
5801687	K4/K5	Bit 1
5801687	L4/L5	1/2 Bit 0B
5801687	M4/M5	1/2 Bit 0A
5801690	H2/H3	042 Transistor
5801689	K2/K3	Zener Diodes
5801688	M2/M3	Reference Voltage

3. Turn dc power on and measure voltage at following locations:
  - a. -36v at laminar bus in 01B.
  - b. +36v at laminar bus in 01B.
  - c. -36v delayed at laminar bus in 01B.
  - d. +3v at laminar bus in 01B.
  - e. -3v at laminar bus in 01B.
  - f. +6v at laminar bus in 01B.

4. Measure yoke clamp voltages at:
  - a.  $9v \pm 2v$  at 01BA1C1TB3A20.
  - b.  $+61v \pm 5v$  at 01BA1C1TB3A21.

**DANGER**

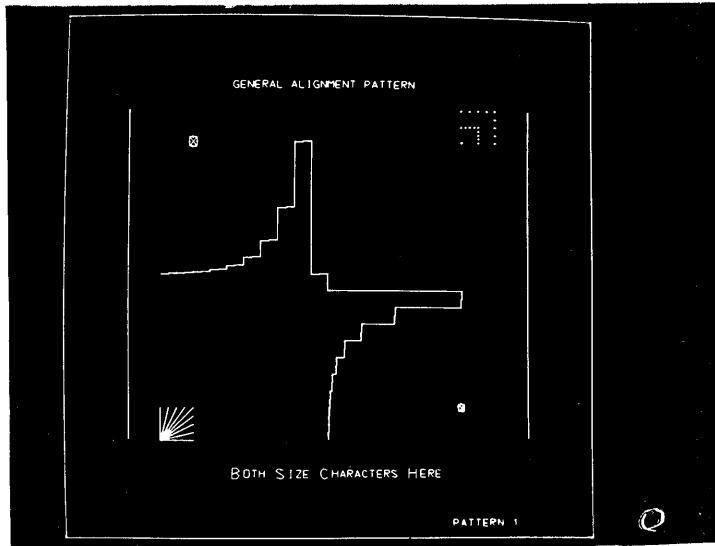
Perform the following steps with extreme caution because of the magnitude of the voltage involved.

5. Turn operator's brightness control and the brightness limiting potentiometer at 01E/A1R4 fully counterclockwise. Remove dc power and then remove CRT socket from neck of tube. Turn dc power on, and measure the voltages between the following points:
  - a. Pins 1 and 12       $6.8vac \pm 10\%$
  - b. Pin 6 and ground    $+450v \pm 5\%$
  - c. Pin 10 and ground    $+450v \pm 5\%$
  - d. Pin 2 and ground     $-36v \pm 4\%$
  - e. Measure voltage between pin 11 of the CRT socket and ground. Simultaneously, vary brightness control and brightness limiting potentiometer from minimum to maximum. Voltage should vary from approximately +80v to approximately +20v.
  - f. Set both controls fully counterclockwise (meter should read approximately +80v). Remove dc power, and replace CRT socket on neck of tube.
6. Turn dc power on. Depress CRT INTENSITY switch, located on 01BA1A1 potentiometer panel, and turn brightness controls slowly in clockwise direction. A spot should be visible within 0.75 inch of center of CRT. Release the switch, turn off power, and insert analog cards as described in the steps that follow.

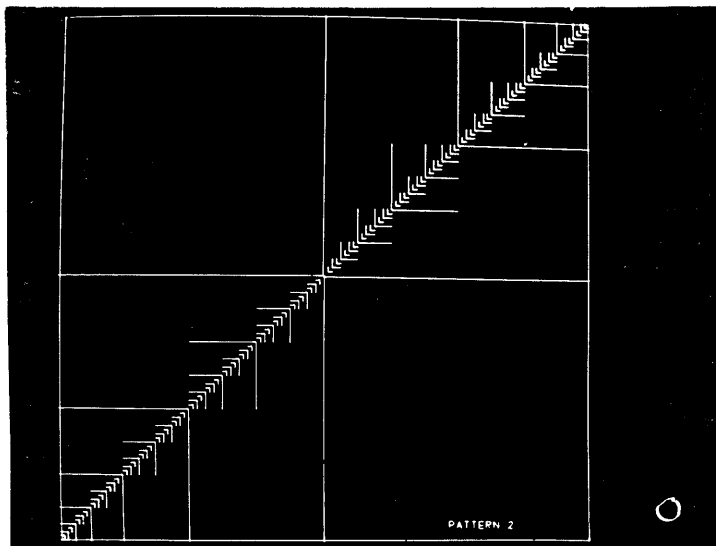
**CAUTION**

Power must be turned off before inserting or removing any analog cards.

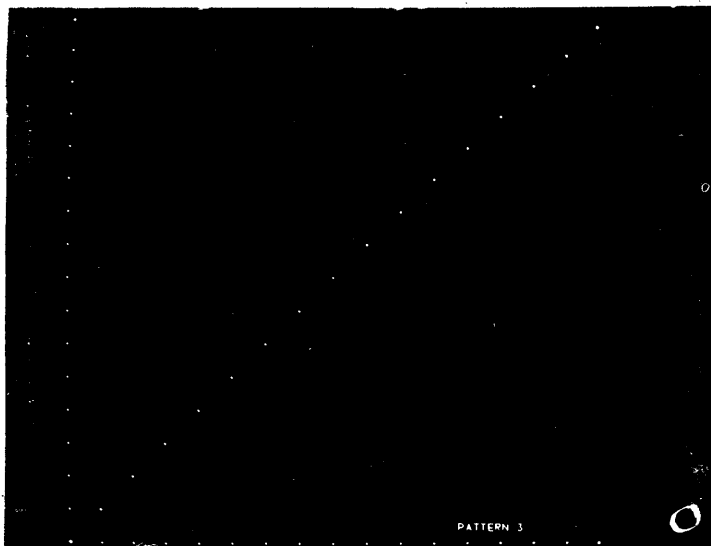
7. Insert DC offset cards (PN 5804731) in locations 01BA2B2/B3 and 01BA2C2/C3.
8. Turn on dc power, and check voltage at card (PN 5804732) location 01BA2L6/L7, pins L6B02, L7B09, and L7B10 with Simpson 270 meter or equivalent. Voltages at these points should be +35v to +36v (ground reference). Also, scope pin L6B03 to determine that on-line noise does not exceed  $\pm 2\%$ .
9. Remove dc power, and insert X and Y centering and gain control cards (PN 5800831). These cards are packaged with the centering and gain functions on the same card. The X card location is 01BA3F2/F3; the Y card location, 01BA3H2/H3. It should be possible to move the CRT spot approximately 1-1/2 inches in the X-axis and approximately 1-1/2



1. Pattern 1 in alignment .

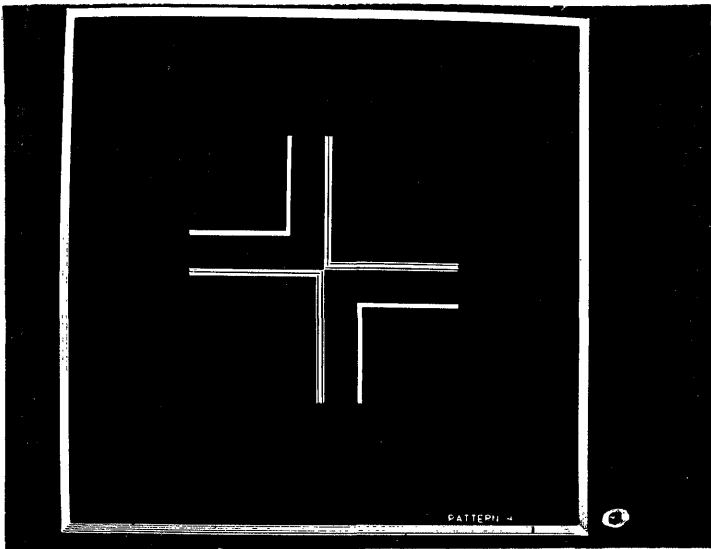


2. Pattern 2 in alignment .

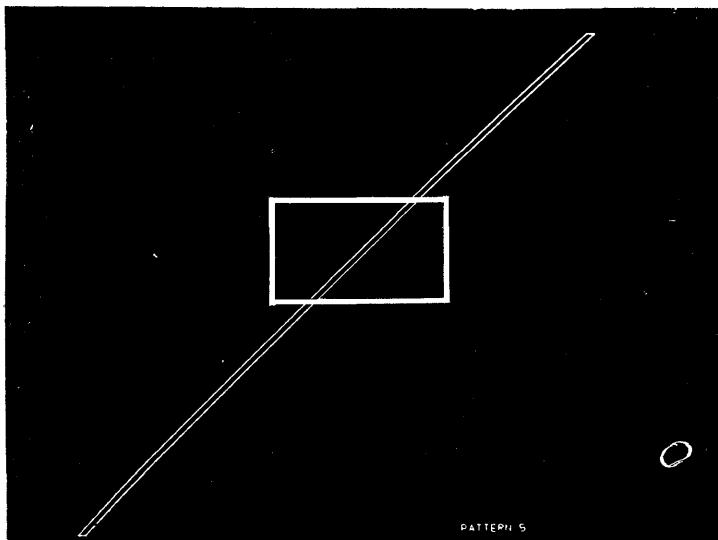


3. Pattern 3 in alignment .

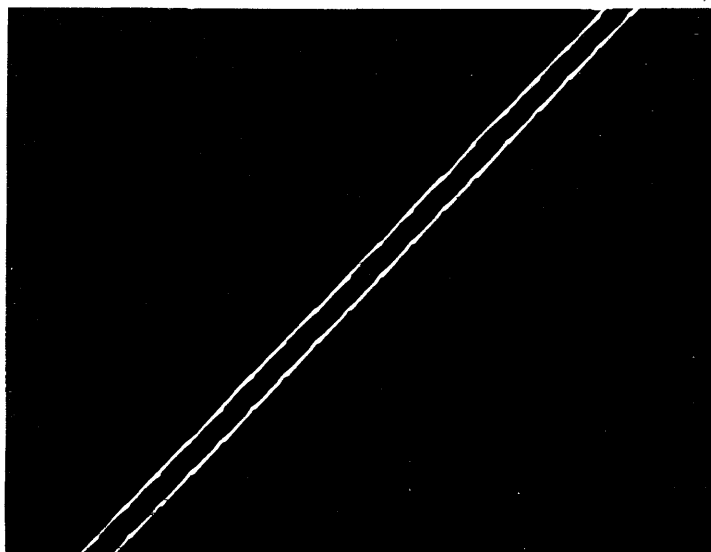
Figure 1-8. Visible Pattern Malfunctions (Sheet 1 of 22)



4. Pattern 4 in alignment.



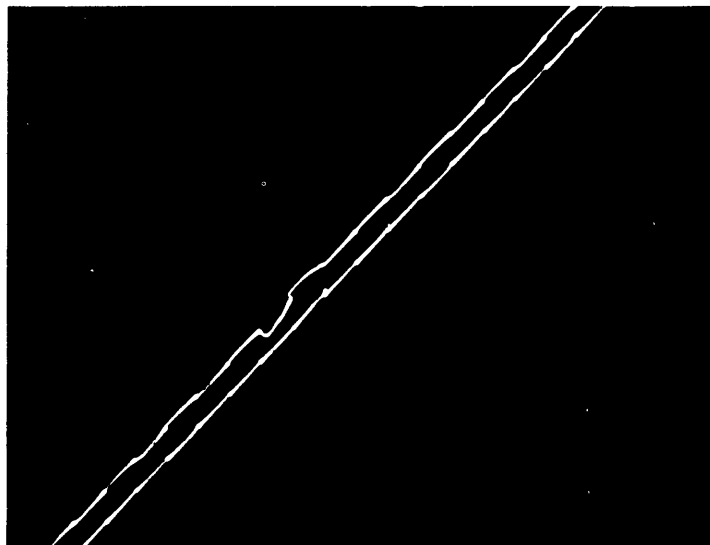
5. Pattern 5 in alignment. Section marked is shown expanded in pictures numbered 5a, 5b, 5c, and 5d.



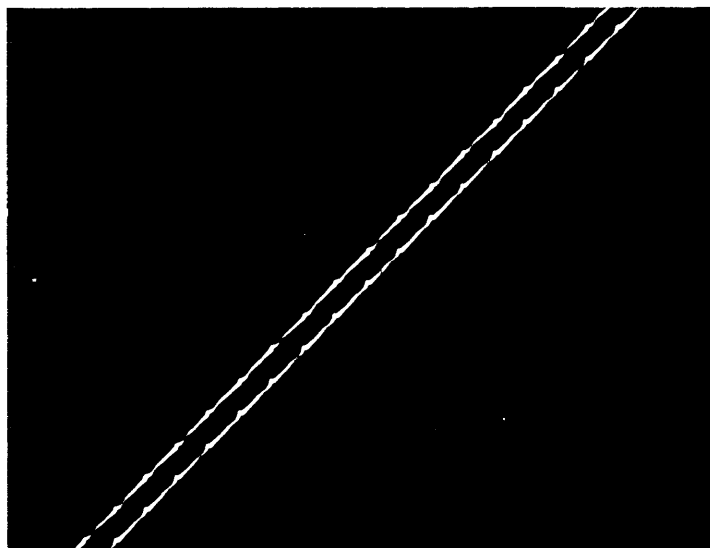
5a. Expanded pattern 5 in alignment.

Figure 1-8. Visible Pattern Malfunctions (Sheet 2 of 22)

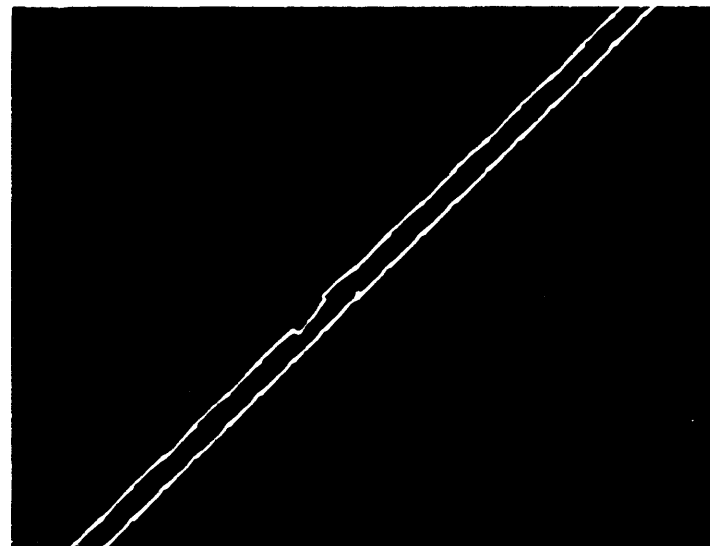




5b. Expanded pattern 5. De-skew reference - loss of voltage. Check 01BA2 H04, H05.

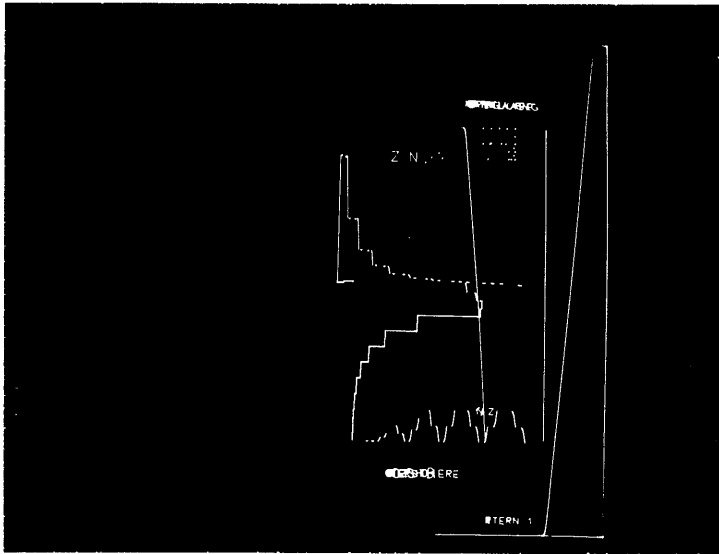


5c. Expanded pattern 5. De-skew reference - shorted transistor on card. Check 01BA2 H04, H05.

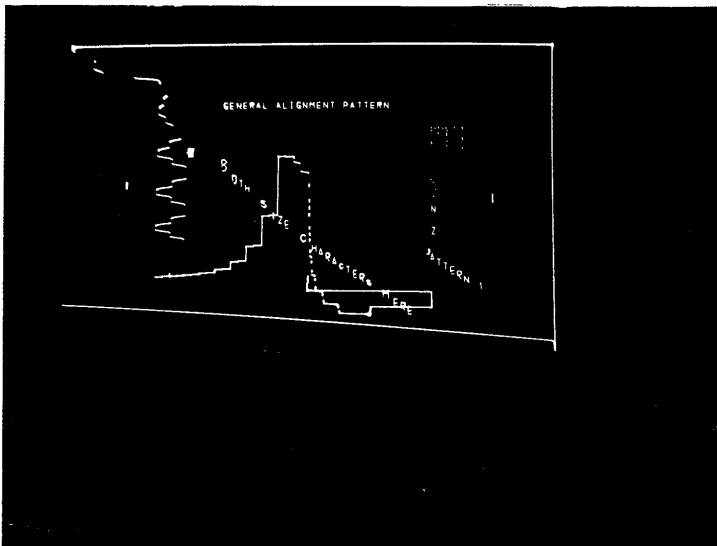


5d. Expanded pattern 5. De-skew switch - open 138 transistor. Check 01BA2 M06, M07.

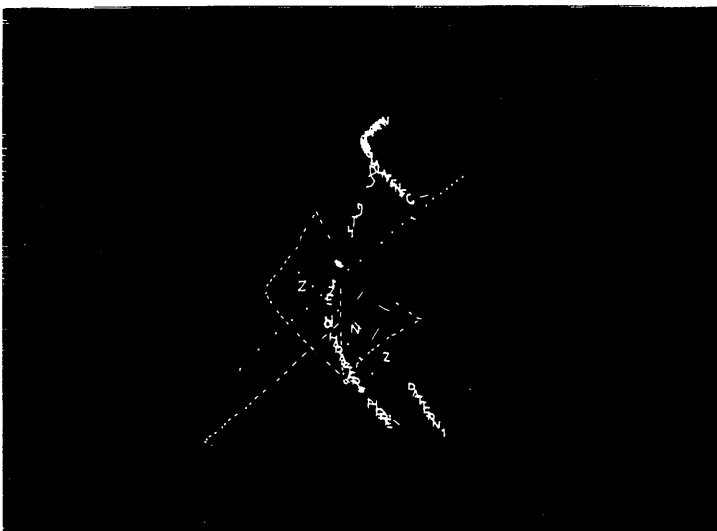
Figure 1-8. Visible Pattern Malfunctions (Sheet 3 of 22)



6. Position isolation - Shorted input diode - L7B09 input. Check 01BA2 L06, L07. X axis input.

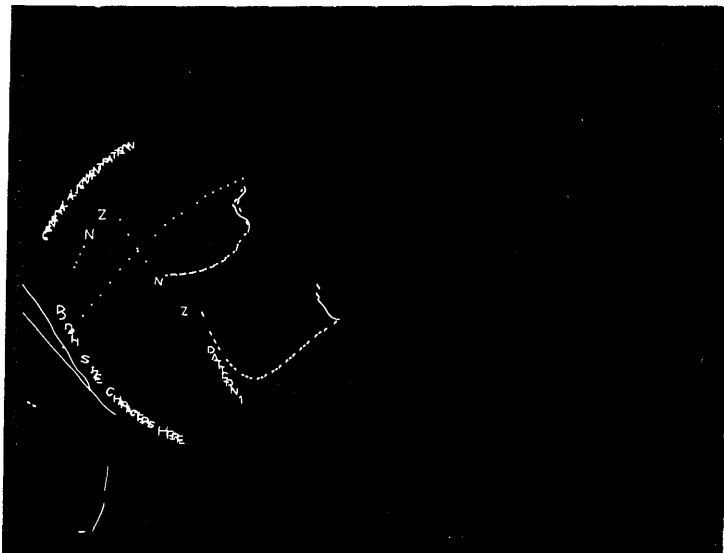


7. Position isolation - Shorted input diode - L7B02 input. Check 01BA2 L06, L07. Y axis input.

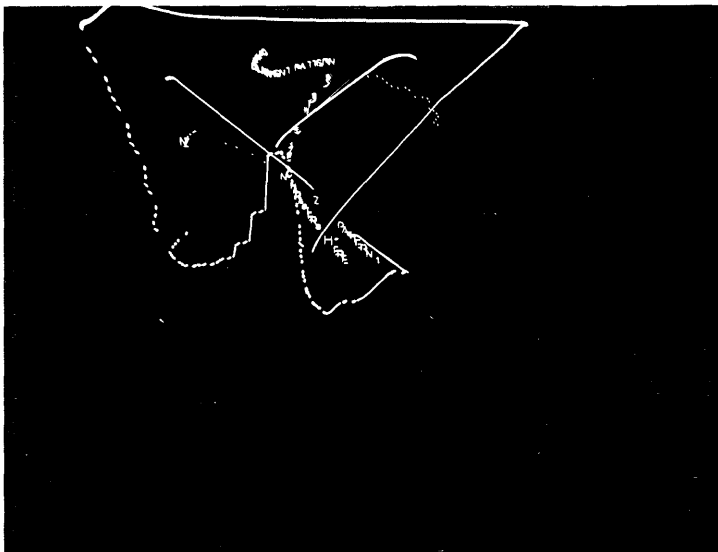


8. De-skew switch - shorted 138 transistor. Check 01BA2 M06, M07.

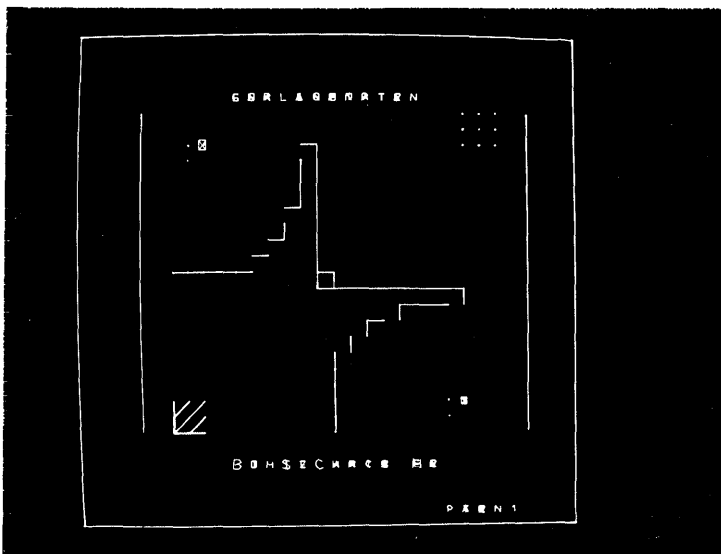
Figure 1-8. Visible Pattern Malfunctions (Sheet 4 of 22)



9. De-skew switch - shorted diode across X yoke. Check 01BA2 M06, M07.

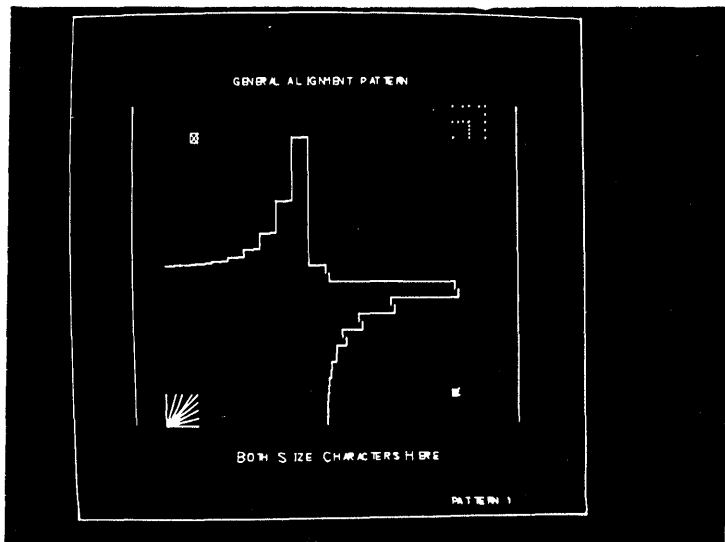


10. De-skew switch - shorted diode across Y yoke. Check 01BA2 M06, M07.

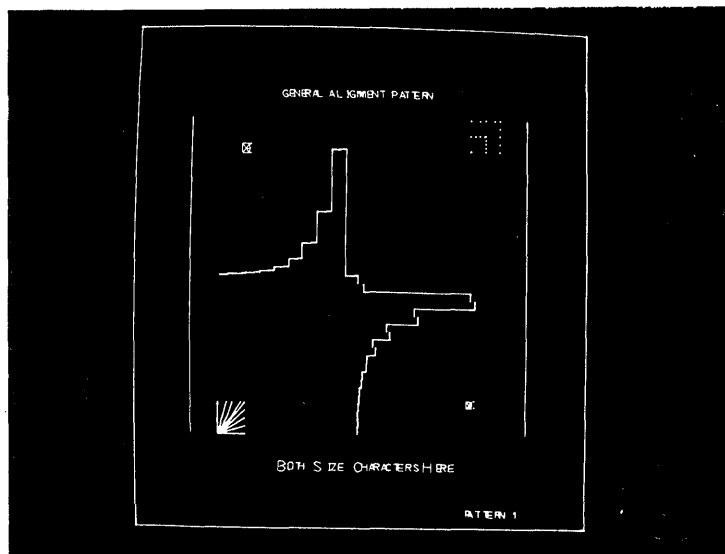


11. Loss of reference voltage inverter. Check 01BA3 G02, G03.

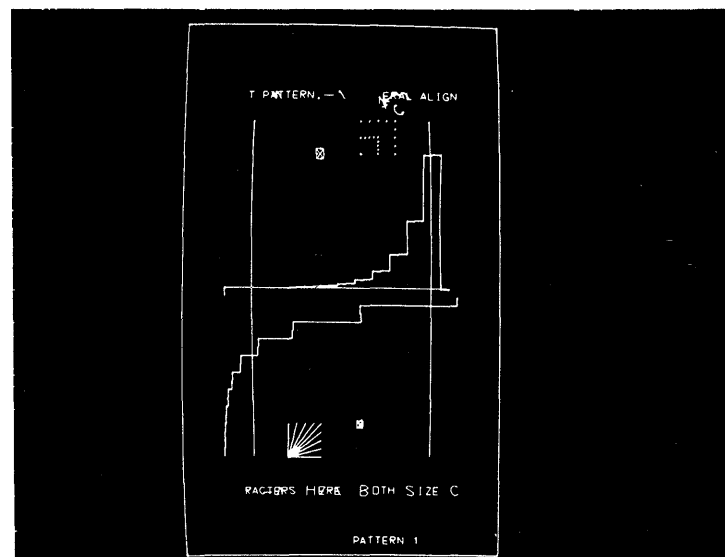
Figure 1-8. Visible Pattern Malfunctions (Sheet 5 of 22)



12. Reference voltage inverter; open 026 transistor. Check 01BA3 G02, G03.

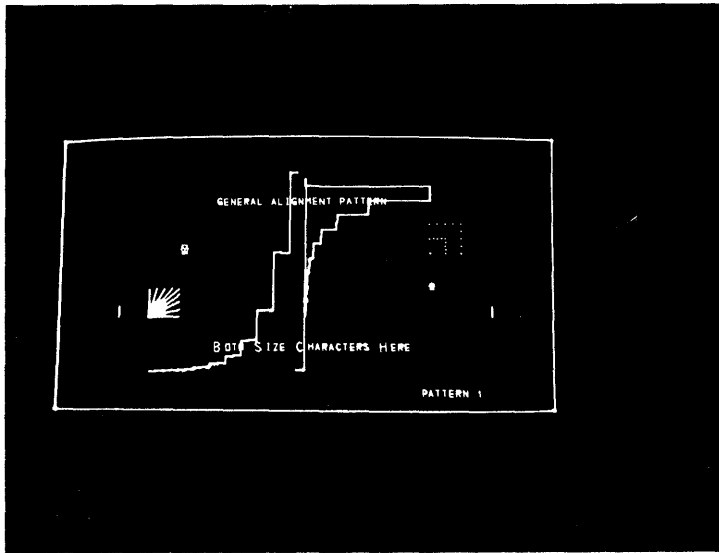


13. Open output transistor gain control (189 transistor). Check 01BA3 F02, F03. X axis.

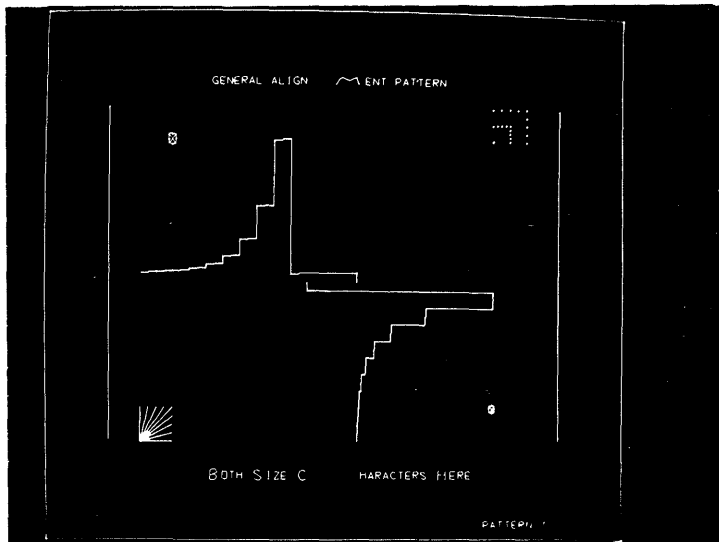


14. Bit 0 constant current source open. Check 01BA3 C04, C05. X axis.

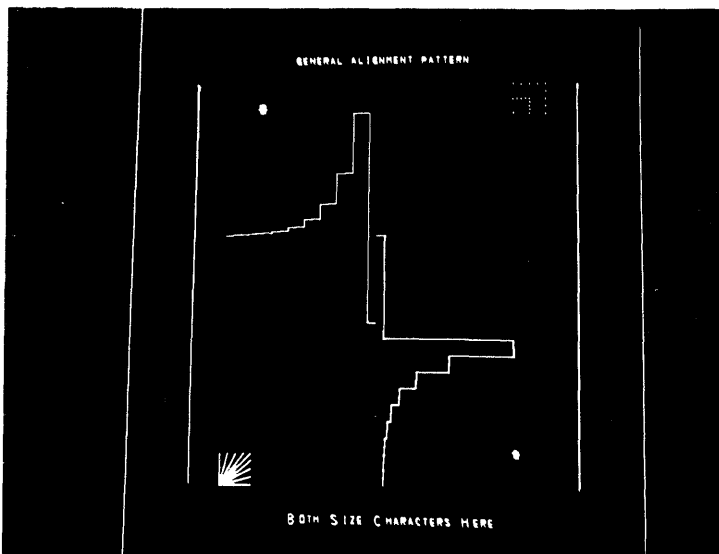
Figure 1-8. Visible Pattern Malfunctions (Sheet 6 of 22)



- 15. Bit 0 constant current source open. Check 01BA3 H04, H05. Y axis.

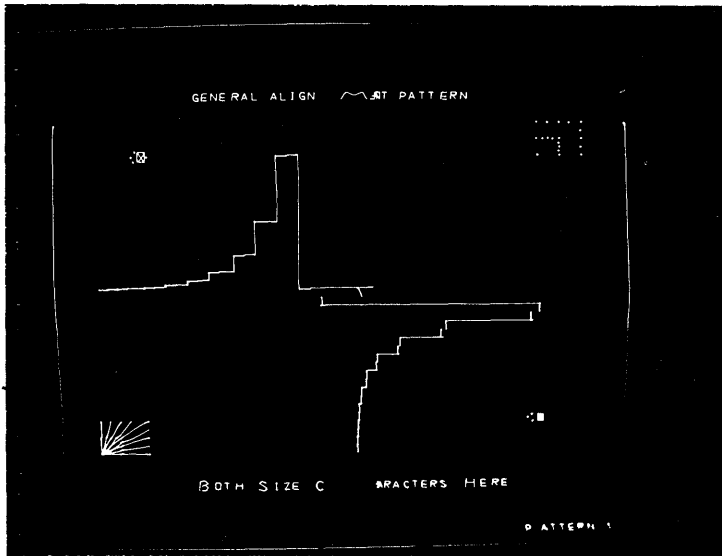


- 16. Bit 0 constant current source shorted, collector to emitter. Check 01BA3 C04, C05. X axis.

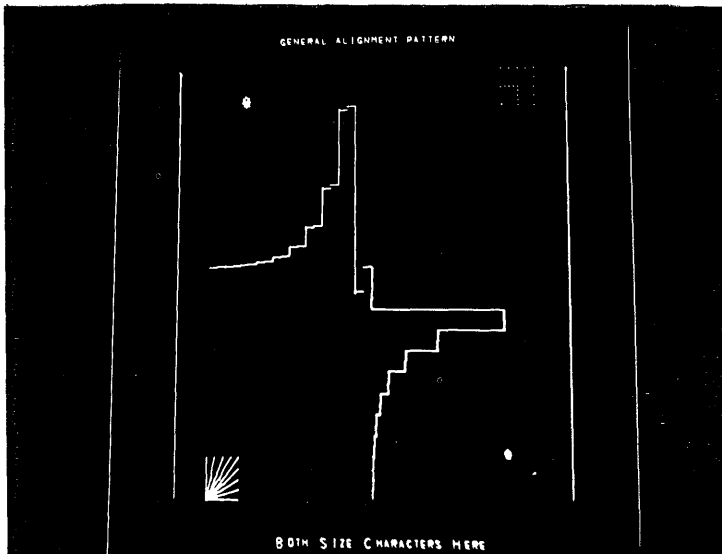


- 17. Bit 0 constant current source shorted, collector to emitter. Check 01BA3 H04, H05. Y axis.

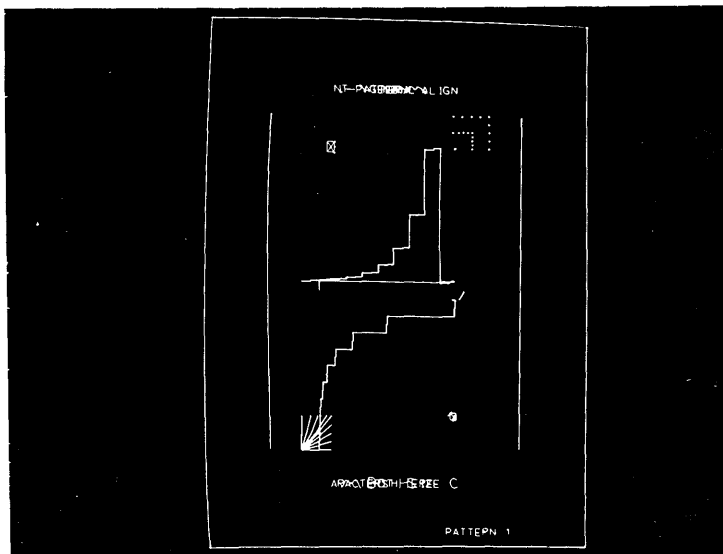
Figure 1-8. Visible Pattern Malfunctions (Sheet 7 of 22)



18. Bit 0 constant current source shorted, base to collector. Check 01BA3 C04, C05. X axis.

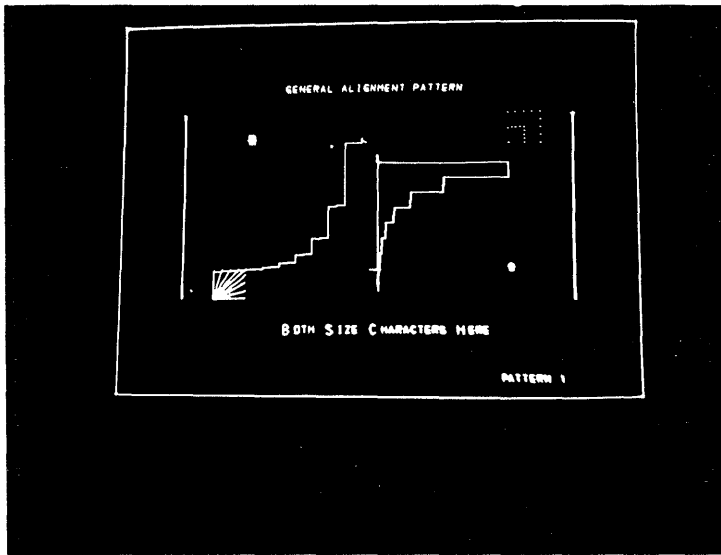


19. Bit 0 constant current source shorted, base to collector. Check 01BA3 H04, H05. Y axis.

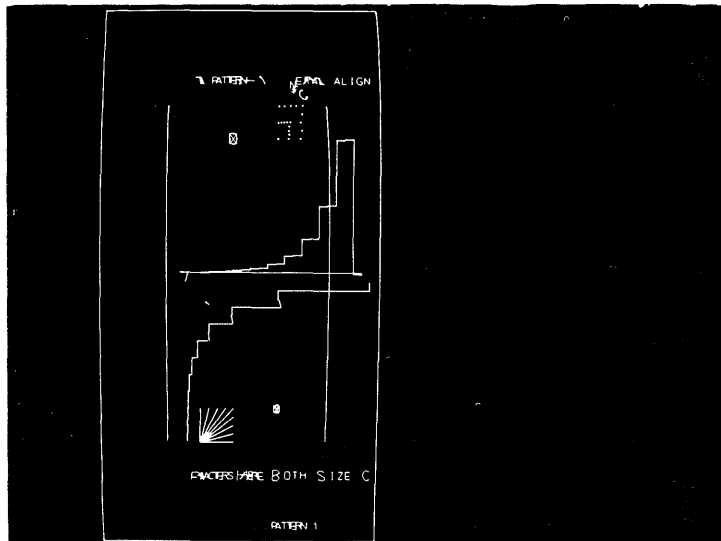


20. Bit 0 switch open - B03 input. Check 01BA3 C04, C05. X axis.

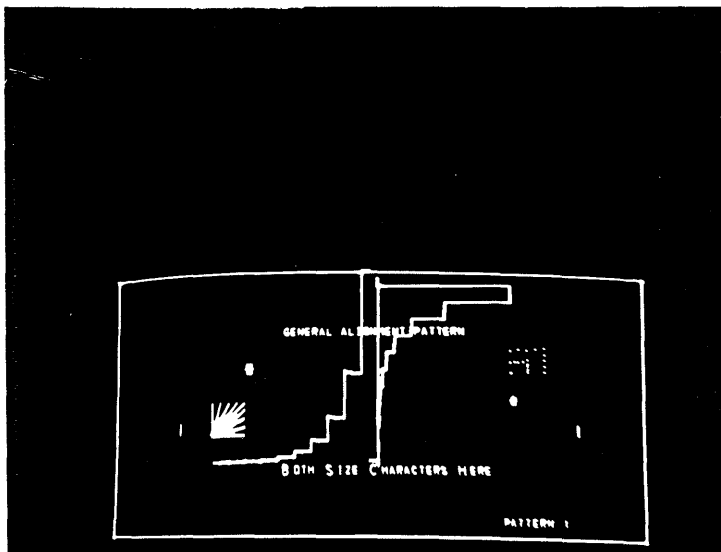
Figure 1-8. Visible Pattern Malfunctions (Sheet 8 of 22)



21. Bit 0 switch open - B03 input. Check 01BA3 H04, H05. Y axis.

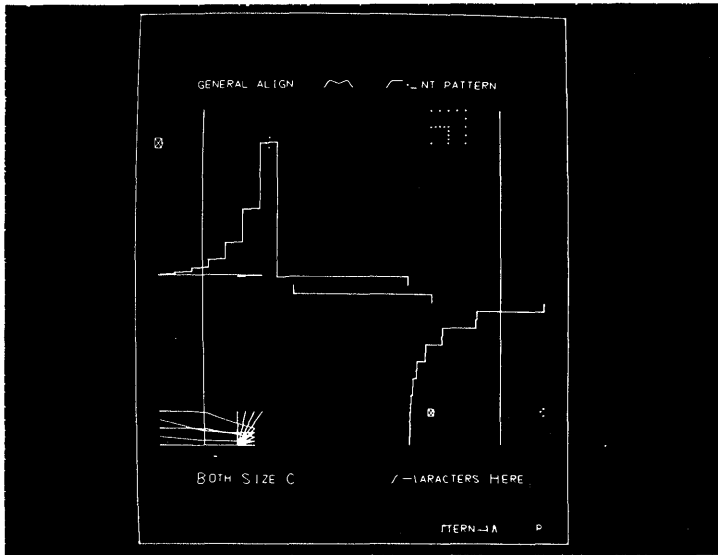


22. Bit 0 switch shorted collector to emitter - B03 input. Check 01BA3 C04, C05. X axis.

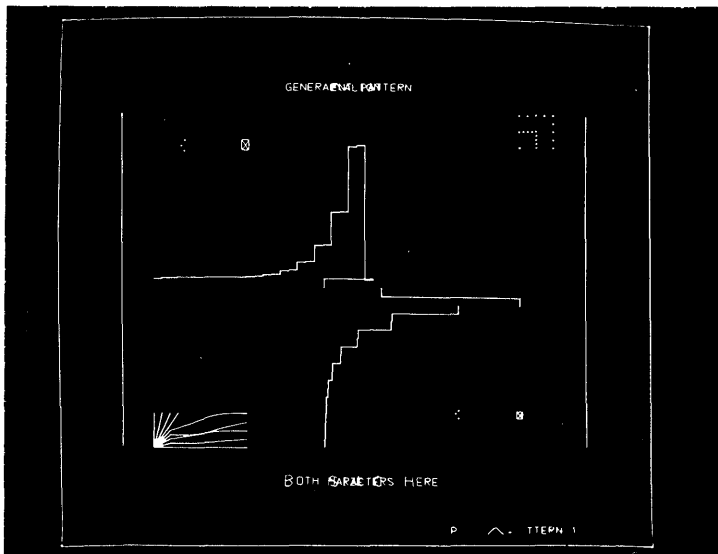


23. Bit 0 switch shorted collector to emitter - B03 input. Check 01BA3 H04, H05. Y axis.

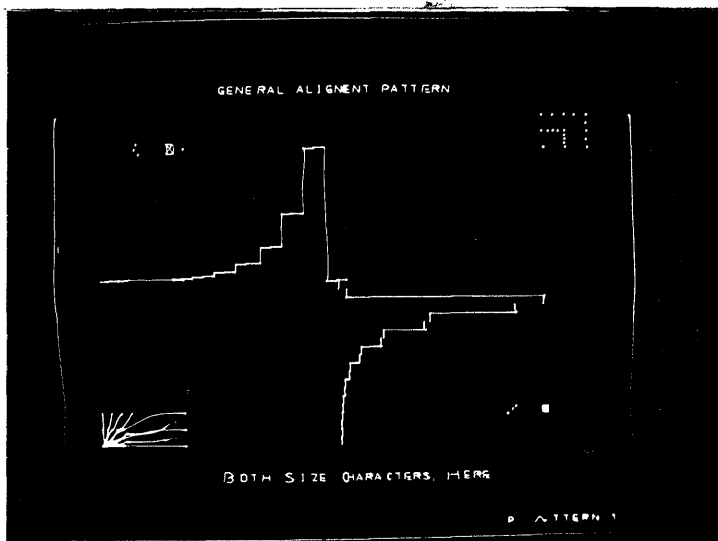
Figure 1-8. Visible Pattern Malfunctions (Sheet 9 of 22)



24. Bit 1 constant current source open. Check 01BA3 D04, D05. X axis.



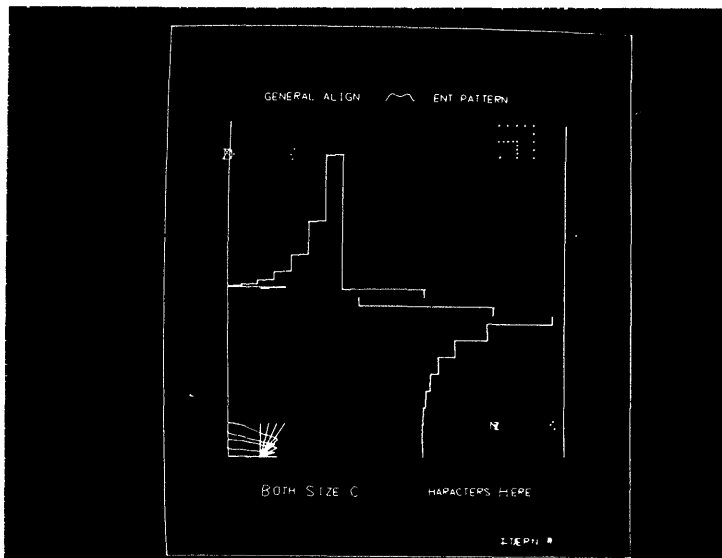
25. Bit 1 constant current source shorted, collector to emitter. Check 01BA3 D04, D05. X axis.



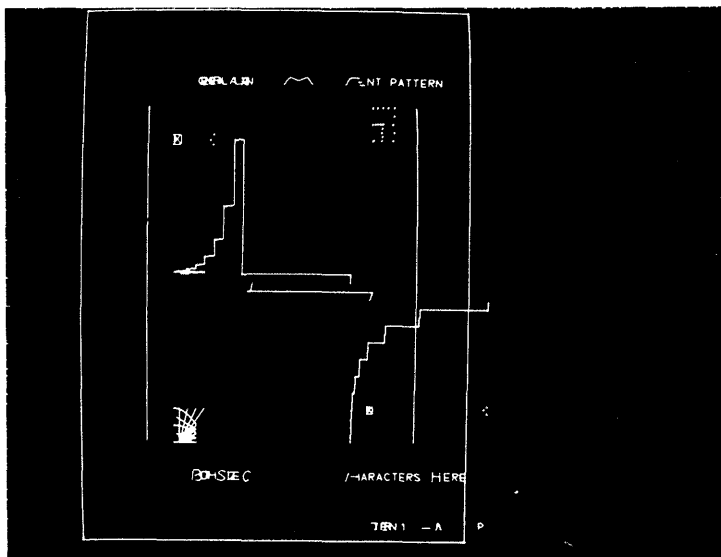
26. Bit 1 constant current source shorted, base to collector. Check 01BA3 D04, D05. X axis.

Figure 1-8. Visible Pattern Malfunctions (Sheet 10 of 22)

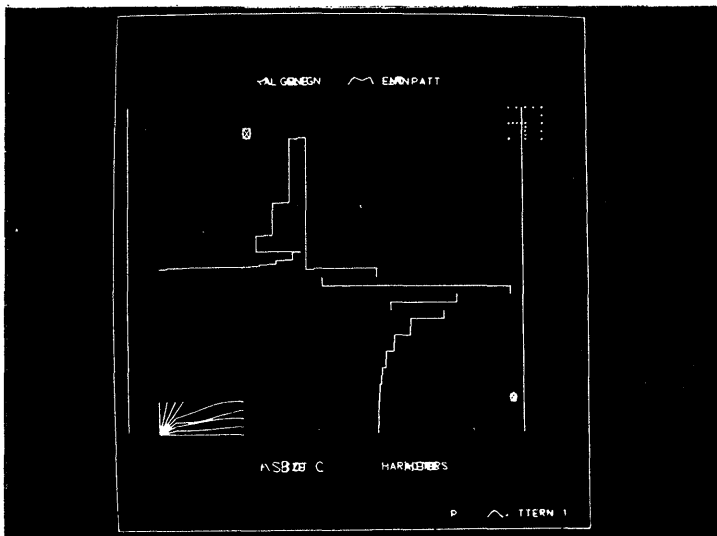




27. Switch 1 open - D10 input.  
Check 01BA3 D04, D05. X axis.

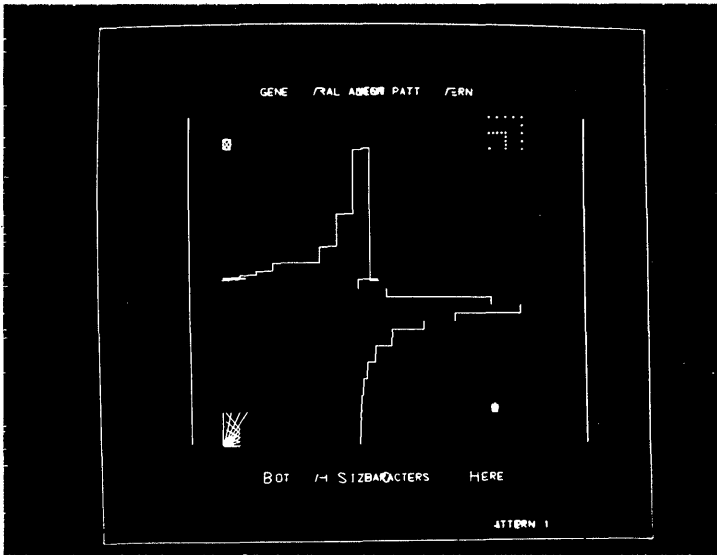


28. Switch 1 shorted, collector to emitter - D10 input. Check 01BA3 D04, D05. X axis.

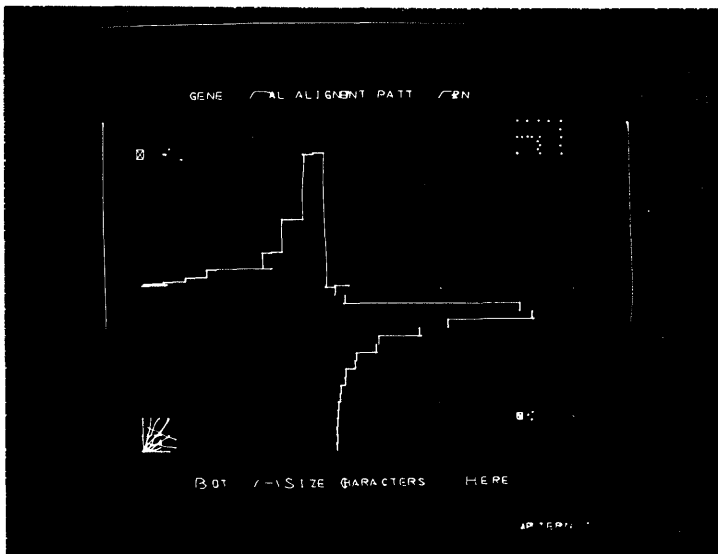


29. Bit 2 constant current source open. Check 01BA3 E04, E05. X axis.

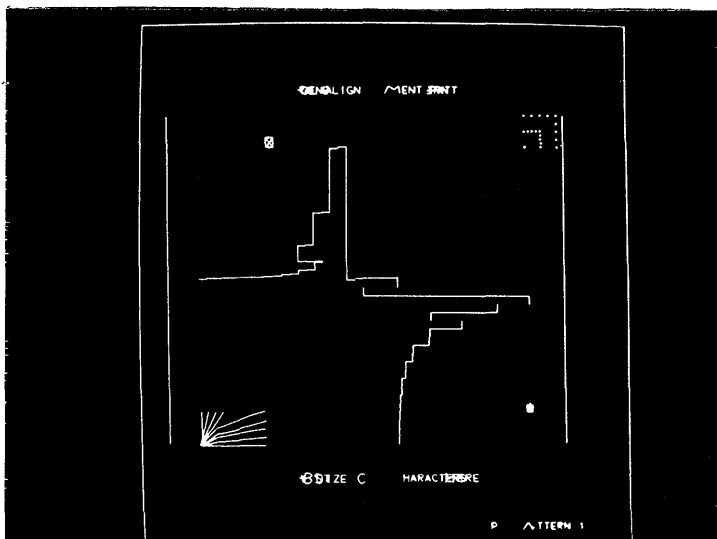
Figure 1-8. Visible Pattern Malfunctions (Sheet 11 of 22)



30. Bit 2 constant current source shorted, collector to emitter. Check 01BA3 E04, E05. X axis.

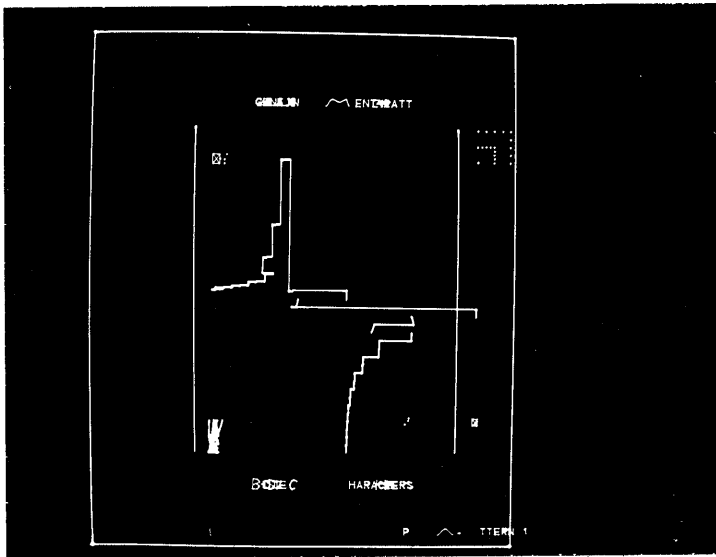


31. Bit 2 constant current source shorted, base to collector. Check 01BA3 E04, E05. X axis.

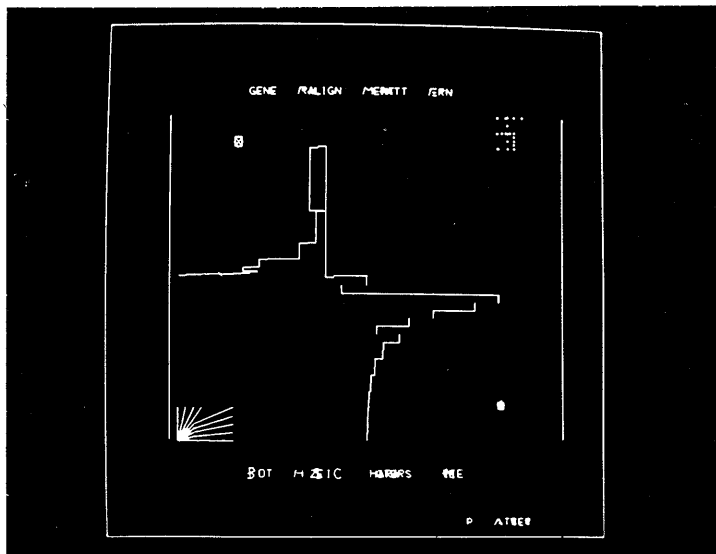


32. Bit 2 switch open - D09 input. Check 01BA3 E04, E05. X axis.

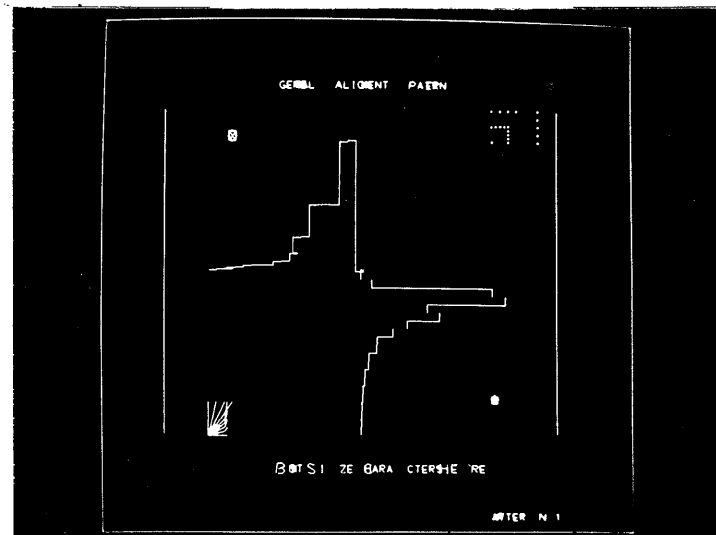
Figure 1-8. Visible Pattern Malfunctions (Sheet 12 of 22)



33. Bit 2 switch shorted, collector to emitter - D09 input. Check 01BA3 E04, E05. X axis.

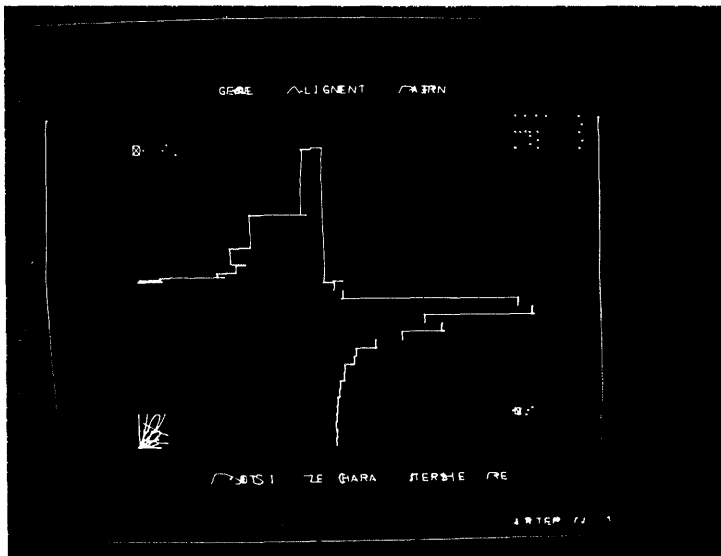


34. Bit 3 constant current source open. Check 01BA3 E04, E05. X axis.

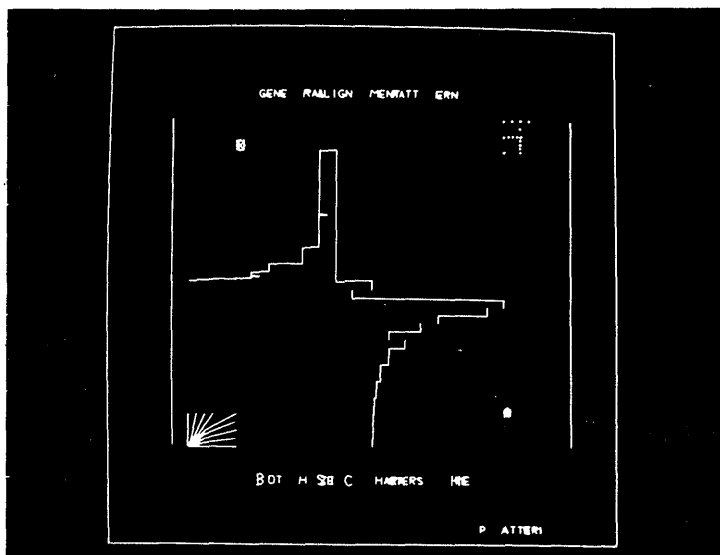


35. Bit 3 constant current source shorted, collector to emitter. Check 01BA3 E04, E05. X axis.

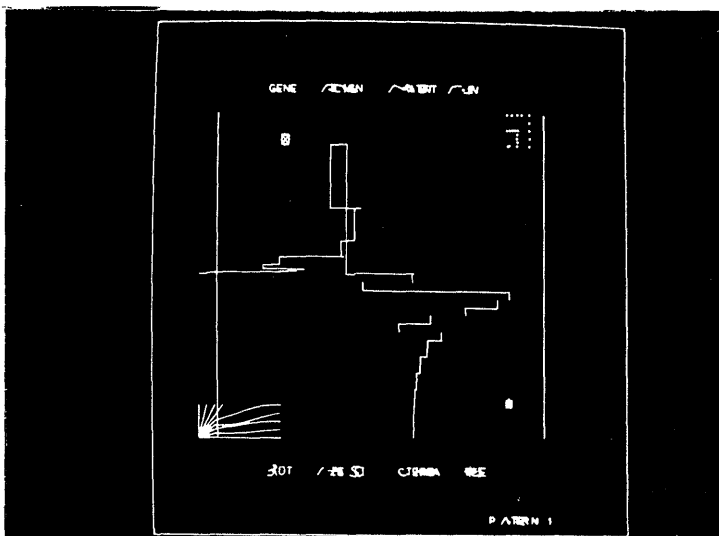
Figure 1-8. Visible Pattern Malfunctions (Sheet 13 of 22)



36. Bit 3 constant current source shorted, base to collector.  
Check 01BA3 E04, E05.  
X axis.

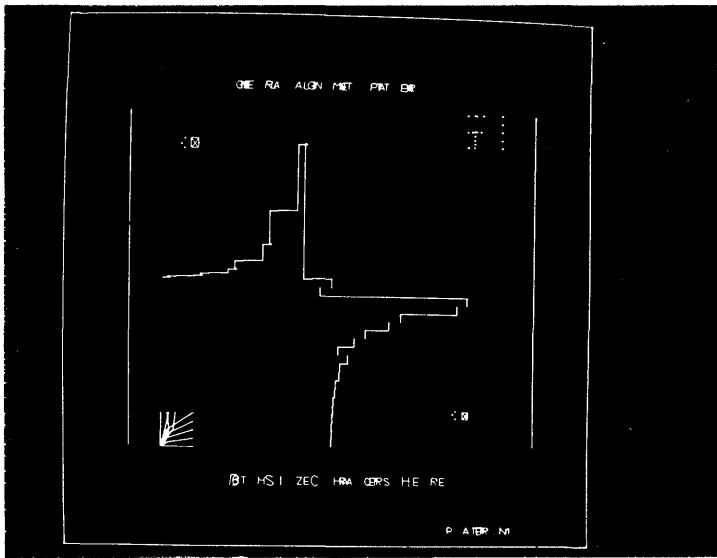


37. Bit 3 switch open - J10 input.  
Check 01BA3 E04, E05. X axis.

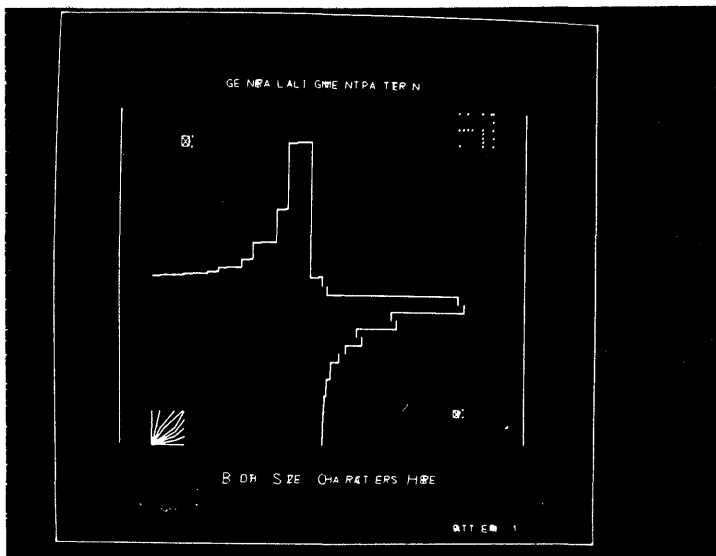


38. Bit 3 switch shorted - J10 input.  
Check 01BA3 E04, E05. X axis.

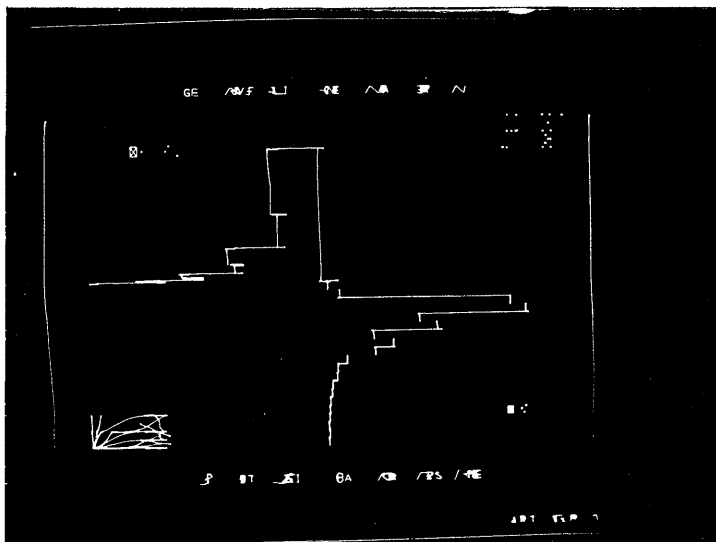
Figure 1-8. Visible Pattern Malfunctions (Sheet 14 of 22)



39. Bit 4 constant current source open.  
Check 01BA3 D04, D05. X axis.

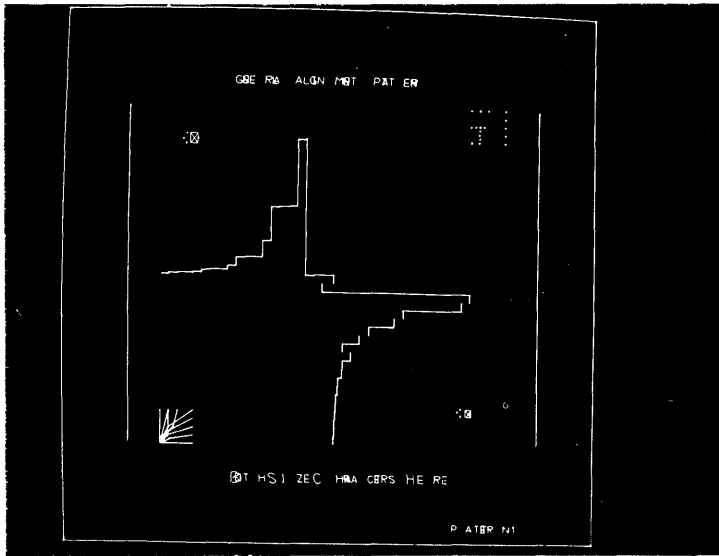


40. Bit 4 constant current source shorted, collector to emitter.  
Check 01BA3 D04, D05, X axis.

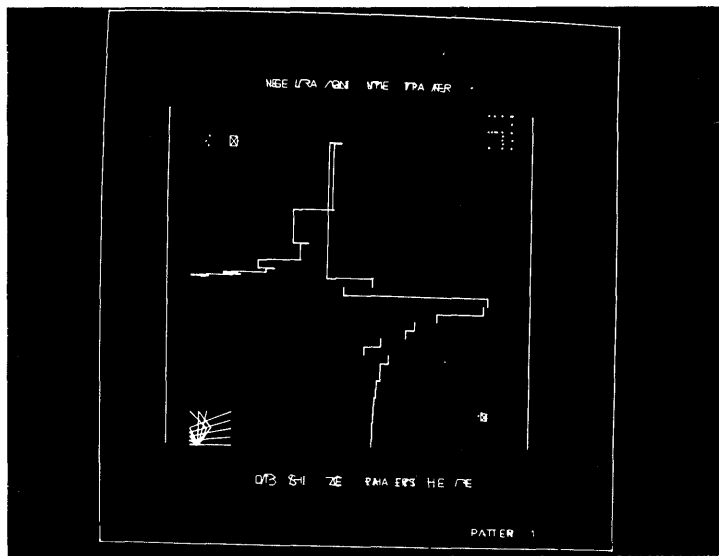


41. Bit 4 constant current source shorted, base to collector.  
Check 01BA3 D04, D05. X axis.

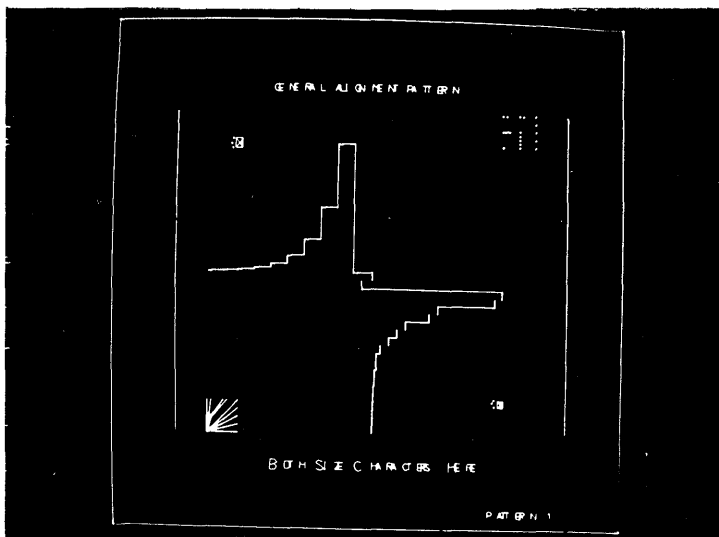
Figure 1-8. Visible Pattern Malfunctions (Sheet 15 of 22)



42. Bit 4 switch open - B02 input.  
Check 01BA3 D04, D05. X axis.

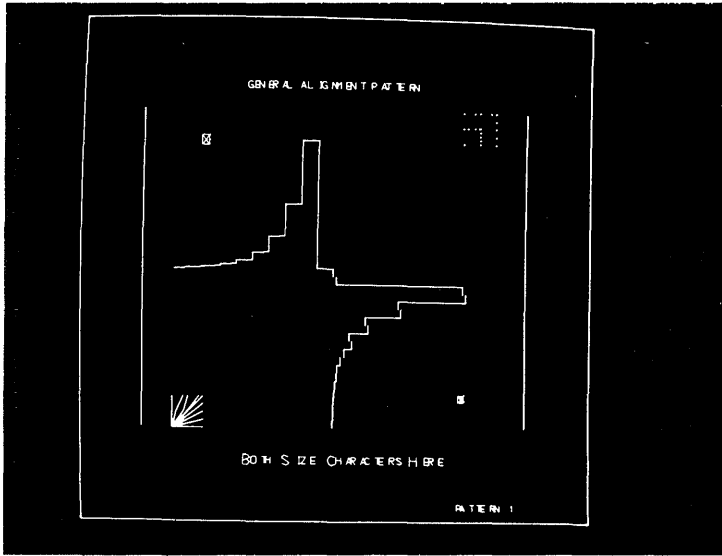


43. Bit 4 switch shorted, collector to emitter. B02 input. Check 01BA3 D04, D05. X axis.

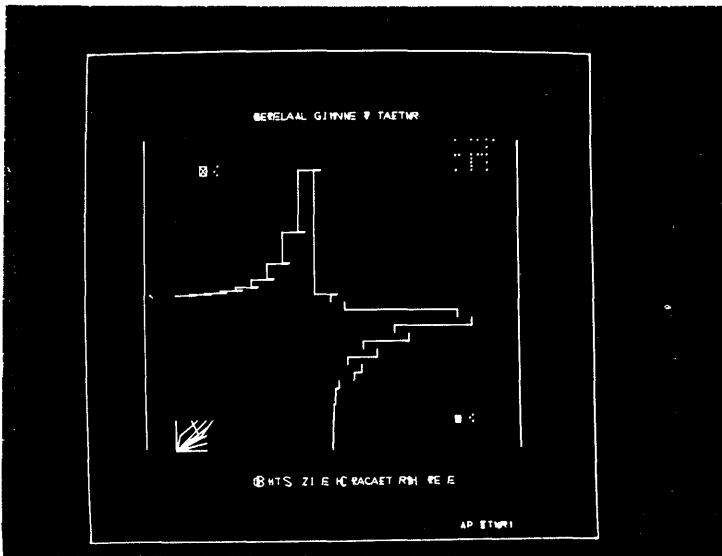


44. Low - order bits open (card removed F4F5). Check 01BA3 F04, F05. X axis.

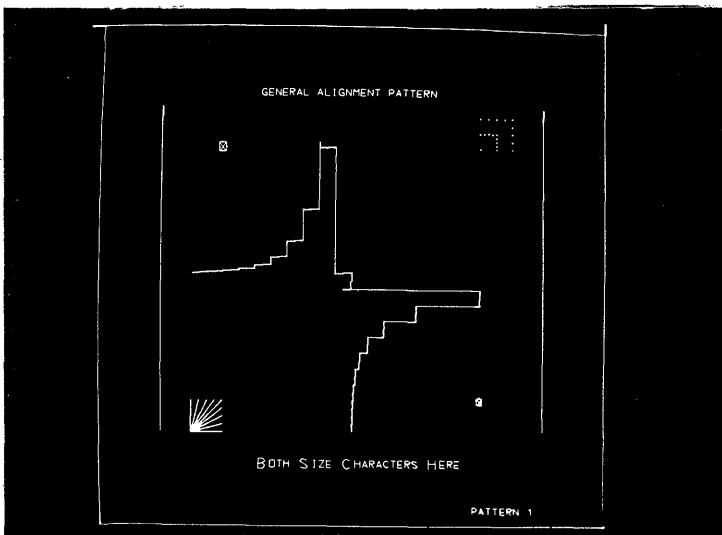
Figure 1-8. Visible Pattern Malfunctions (Sheet 16 of 22)



45. Low - order bit input diode shorted. Check 01BA3 F04, F05. X axis.

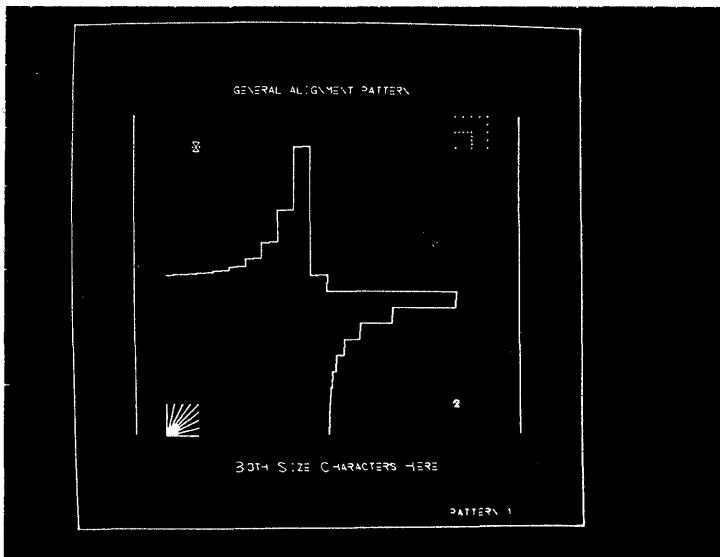


46. Low - order bit; 2 input diodes shorted. Check 01BA3 F04, F05. X axis.

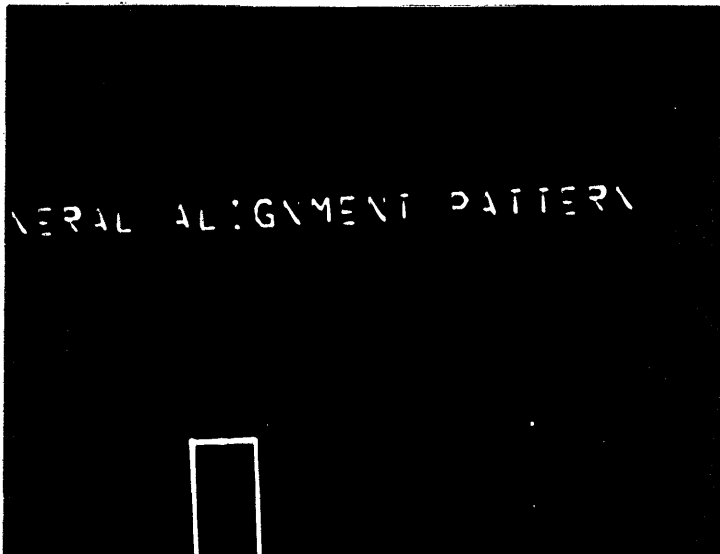


47. Loss of +11v clamp. Check circuit located at 01BA1C1 and 01BA1D1.

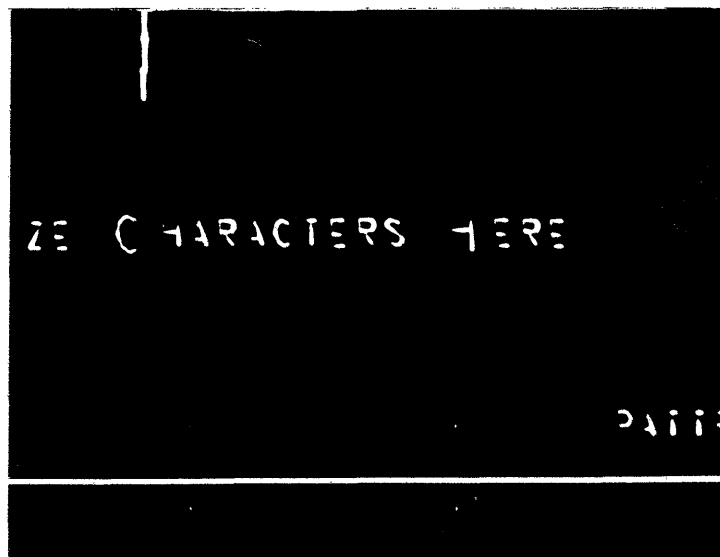
Figure 1-8. Visible Pattern Malfunctions (Sheet 17 of 22)



48. Character isolation; open input diode. Check 01BA2 H02, H03. (Also see 48a and 48b.) Y axis.



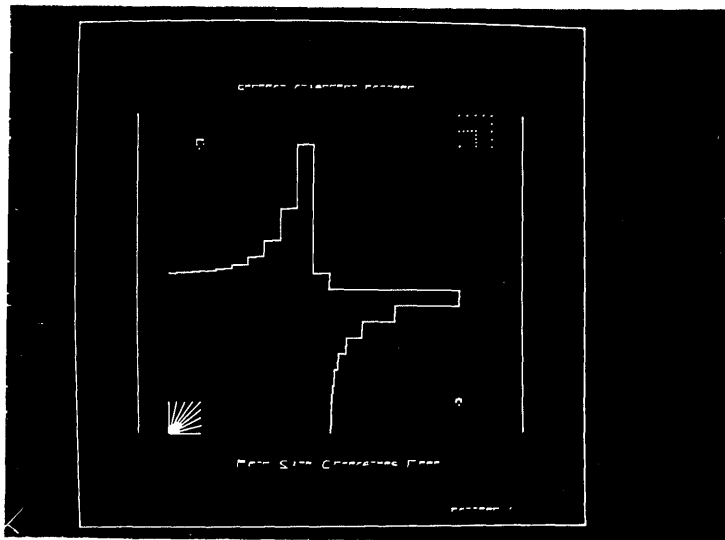
48a. Character isolation; open input diode. Check 01BA2 H02, H03. Regular-size characters shown. Y axis.



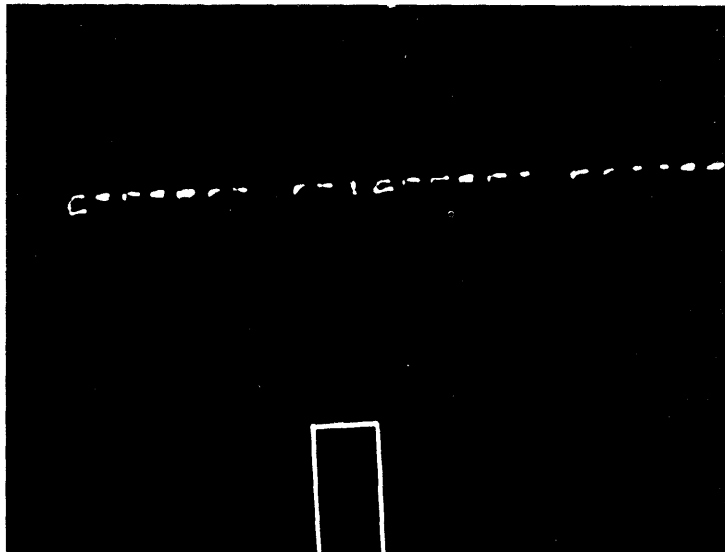
48b. Character isolation; open input diode. Check 01BA2 H02, H03. Large-size characters shown. Y axis.

Figure 1-8. Visible Pattern Malfunctions (Sheet 18 of 22)

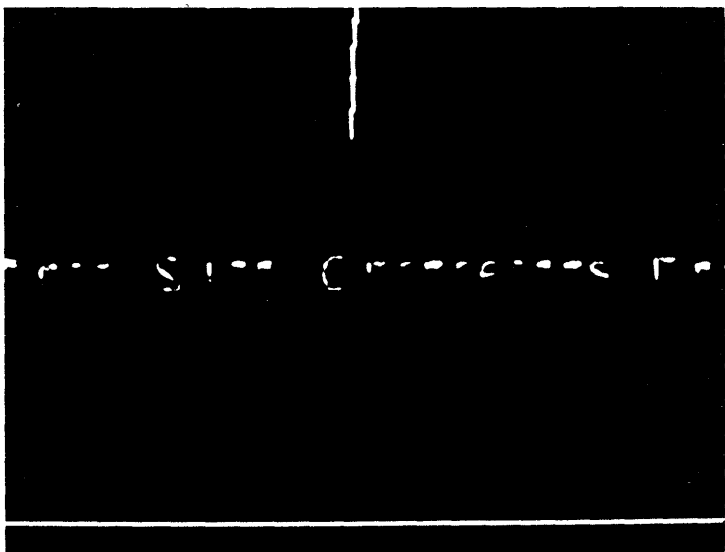




49. Character isolation-shorted input diode. Check 01BA2 H02, H03. (Also see 49a and 49b.) Y axis.

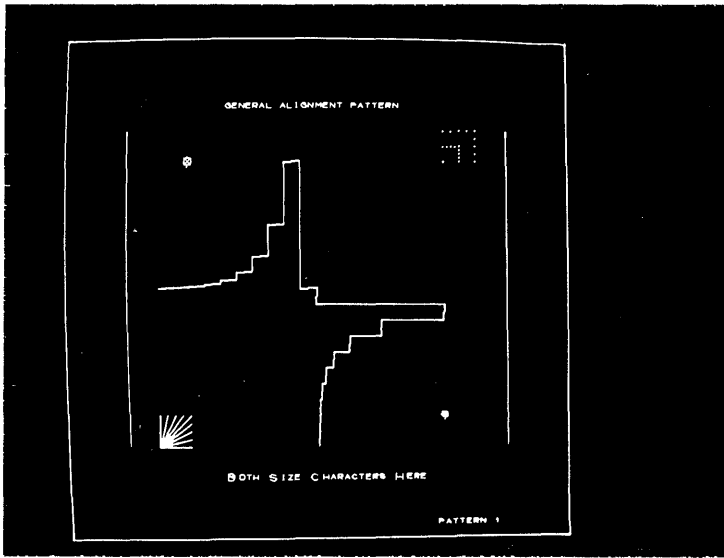


49a. Character isolation-shorted input diode. Check 01BA2 H02, H03. Effect on regular-size characters shown. Y axis.

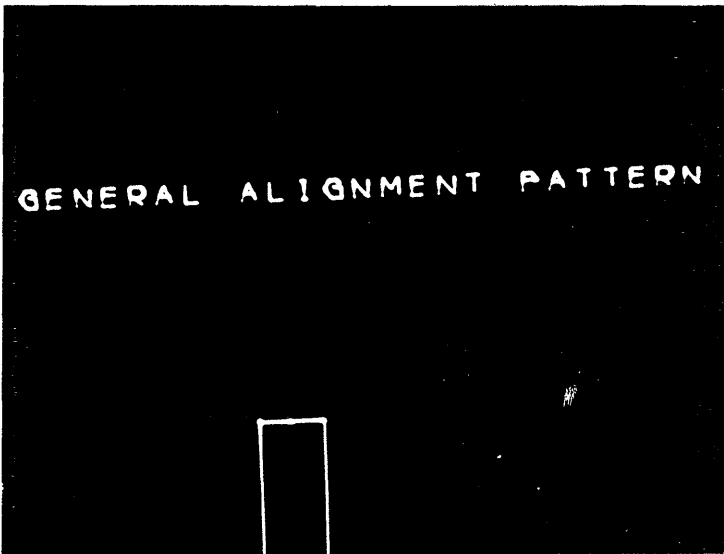


49b. Character isolation-shorted input diode. Check 01BA2 H02, H03. Effect on large-size characters shown. Y axis.

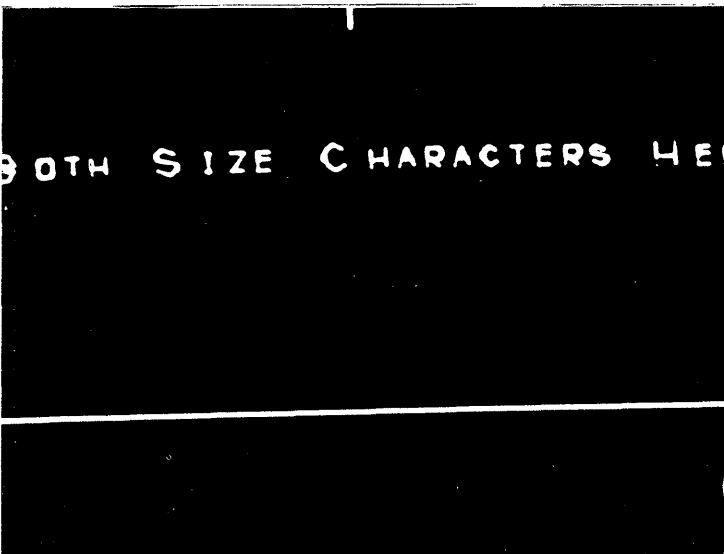
Figure 1-8. Visible Pattern Malfunctions (Sheet 19 of 22)



50. Character generator - shorted bit 4 collector to emitter. Check 01BA2 M02, M03. (Also see 50a and 50b.) Y axis.

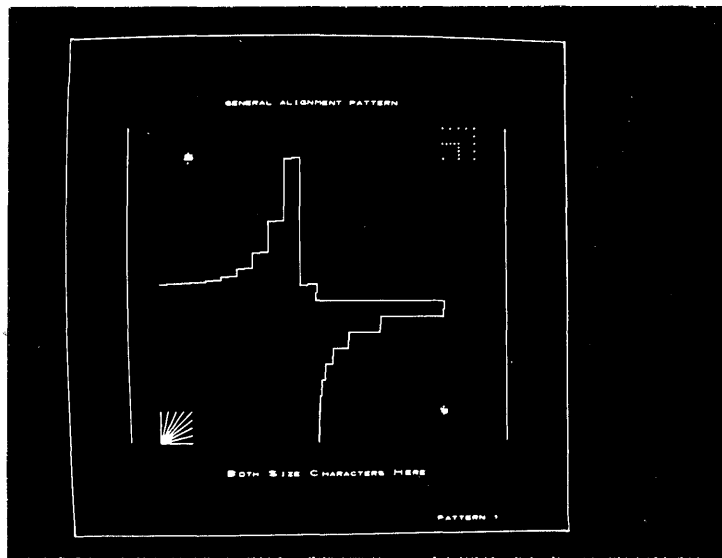


50a. Character generator - shorted bit 4 collector to emitter. Check 01BA2 M02, M03. Effect on regular-size characters shown. Y axis.

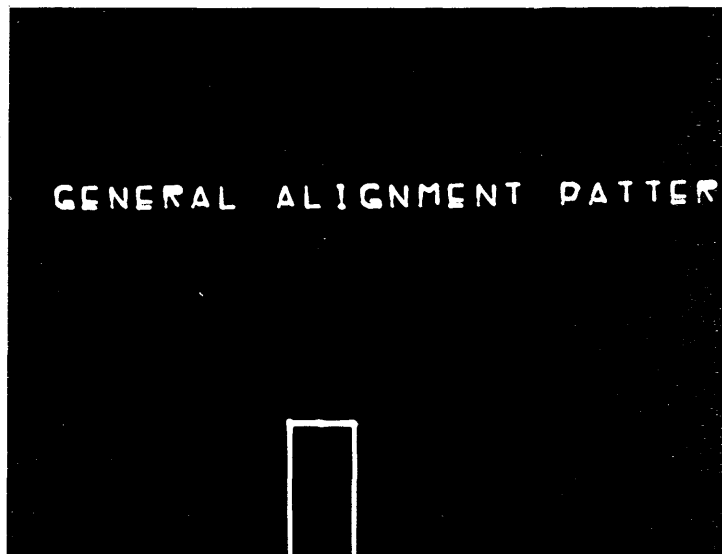


50b. Character generator - shorted bit 4 collector to emitter. Check 01BA2 M02, M03. Effect on large-size characters shown. Y axis.

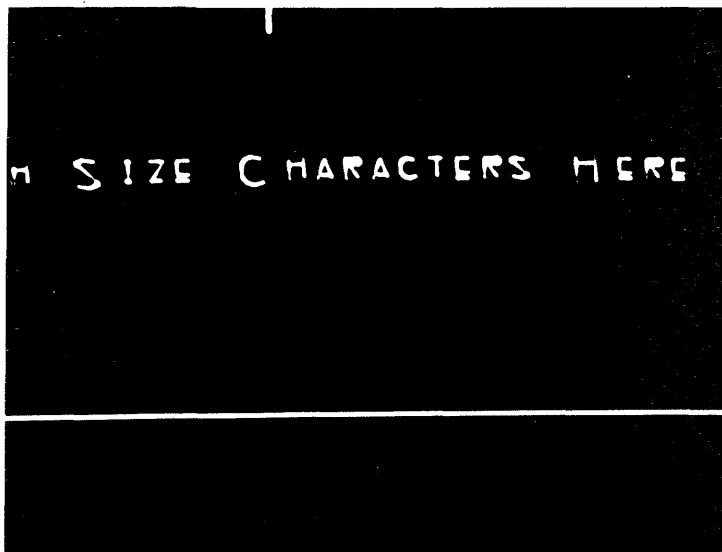
Figure 1-8. Visible Pattern Malfunctions (Sheet 20 of 22)



51. Open character buffer. Check 01BA2 L02, L03. (Also see 51a and 51b.) Y axis.

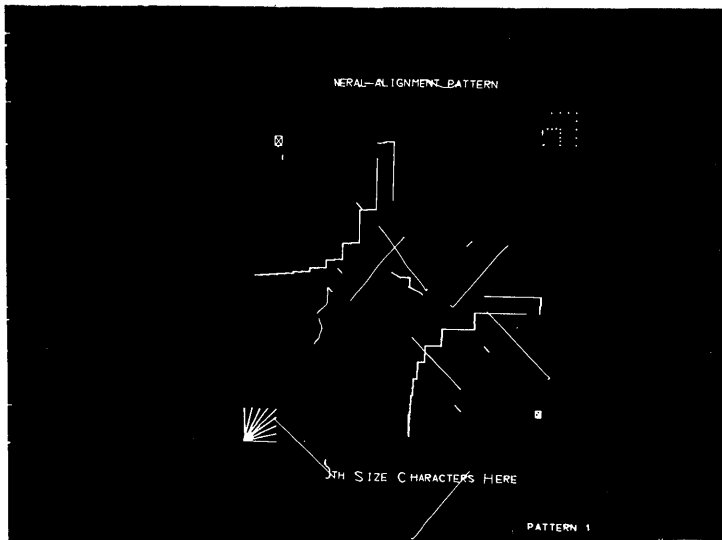


51a. Open character buffer. Check 01BA2 L02, L03. Effect on regular-size characters shown. Y axis.

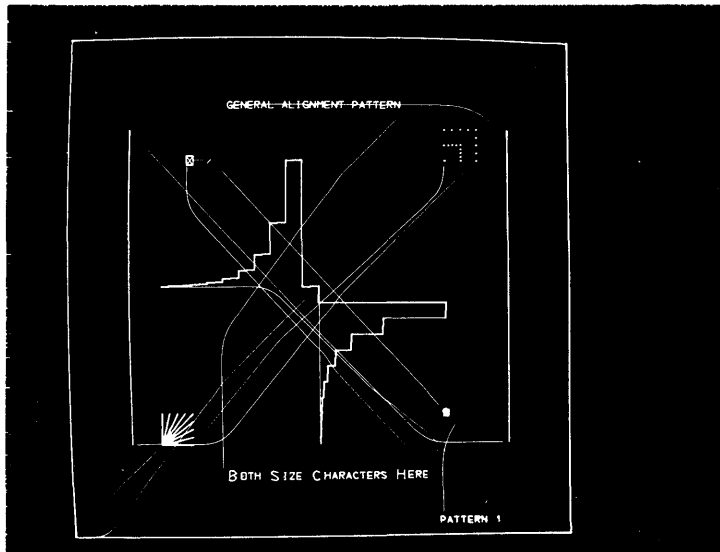


51b. Open character buffer. Check 01BA2 L02, L03. Effect on large-size characters shown. Y axis.

Figure 1-8. Visible Pattern Malfunctions (Sheet 21 of 22)



52. Analog deflection complete line plus all the time. Check 01BA2 G04, G05.



53. Maladjusted blank-unblank card mounted potentiometer (simulates poor adjustment or partial switching of unblank transistor). Readjust 01BA2 J06, J07.

Figure 1-8. Visible Pattern Malfunctions (Sheet 22 of 22)

inches in the Y-axis by use of the centering controls. Return the spot to approximate center of CRT.

10. Turn on dc power, and check voltage variations on the outputs of the X gain control at 01BA3F3D06 by turning X GAIN potentiometer. Voltage should vary from 0v to approximately -12v. Set voltage at -5v.
11. Check for voltage variation in the Y gain control output at 01BA3H3D06. Voltage should vary between 0v and approximately -12v. Set voltage at -5v.
12. Remove dc power, and insert blank-unblank I card (PN 5801307) in location 01BA2G6/G7. Turn on dc power, and load the Full Square program (program #1) from CE panel as directed. Scope for voltage swing from

ground to approximately +8v at 01BA2G7D02. See Figure 1-9.

13. Remove dc power, and insert blank-unblank II card (PN 5801308) in location 01BA2J6/J7.

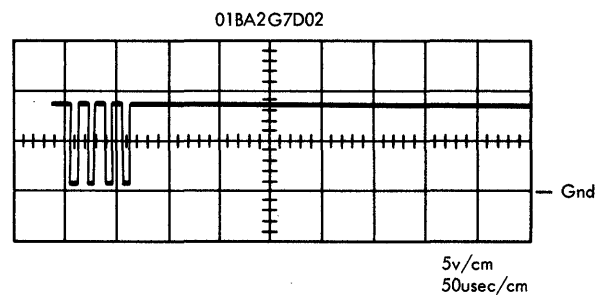


Figure 1-9. DC Intensity I CRT Output

Turn on dc power, and scope for a voltage swing of -30v to ground at 01BA2J6B04. If necessary, adjust card-mounted potentiometer until -30v level slowly goes positive. Then, reverse direction of control until -30v level is again solid, and rotate control approximately two more turns. With potentiometer adjusted, a spot should appear in the middle of the CRT. See Figure 1-10. (CRT INTENSIFY pushbutton should not be used now.)

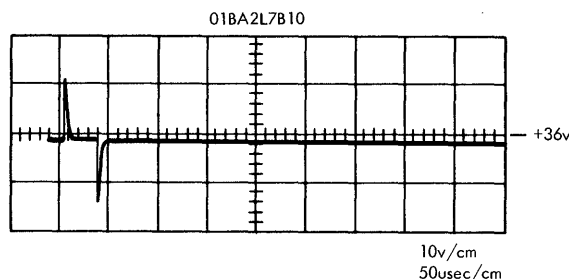
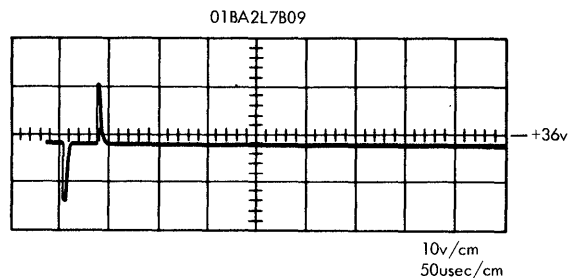
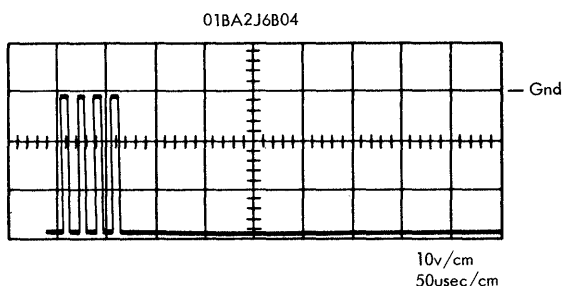


Figure 1-10. Blank-Unblank II CRT Output

14. Remove dc power, and install reference voltage inverter driver card (PN 5800833) in location 01BA3G2/G3.
15. Turn on dc power, and check the voltage for X output at 01BA3G2D09 and Y output at 01BA3G3D09. Voltage should vary between ground and at least -12v when associated gain control potentiometer is adjusted from minimum to maximum. Set potentiometers for -4v output.
16. Remove dc power, and install bits 5 through 9 for both the X- and Y-axes, which comprises a total of four cards (PN 5801303). The X card locations are 01BA3F4/F5 and 01BA3G4/G5; the Y card locations, 01BA3L4/L5 and 01BA3M4/M5.
17. Turn on dc power. Using the Full Square program, observe bit-switching on the CRT. The display should be a square of approximately 3/8 inch. If the corners are overshooting, it may be necessary to adjust position damping. Observe the yoke waveforms at the points indicated in Figure 1-11.
18. Remove dc power, and insert position isolation card (PN 5804732) in location 01BA2L6/L7. Turn on power, and scope the output at 01BA2L6D07 for signal swing of +36v to approximately +20v. See Figure 1-12.
19. Turn off power, and insert asynchronous delay card PN 5800825 in position 01BA2G4/G5, PN 5800826 in 01BA2F4/F5, and PN 5800827 in 01BA2G3. Turn on power, and ensure that full-square pattern is still present and undistorted.

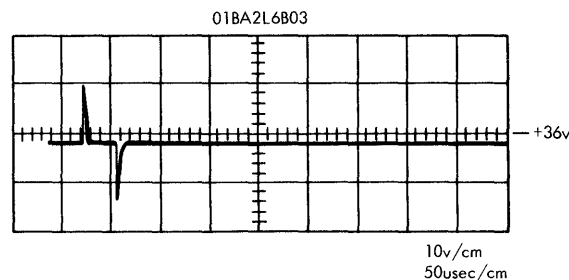
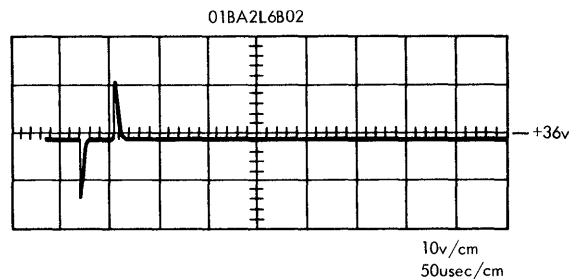


Figure 1-11. Yoke Waveforms, Bits 5 Through 9 Active

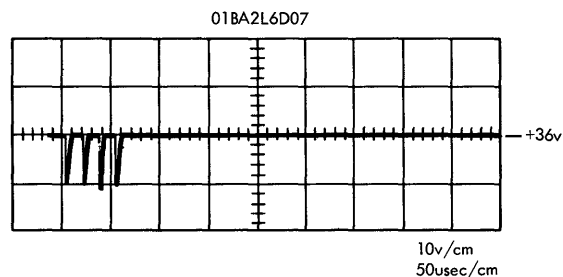


Figure 1-12. Position Isolation Output

20. Turn off power, and insert X and Y bit 0 cards (PN 5800832) in 01BA3C4/C5 and 01BA3H4/H5.
21. Turn on power, and check CRT for approximately a 6-inch square. Observe yoke waveforms at points indicated in Figure 1-13.

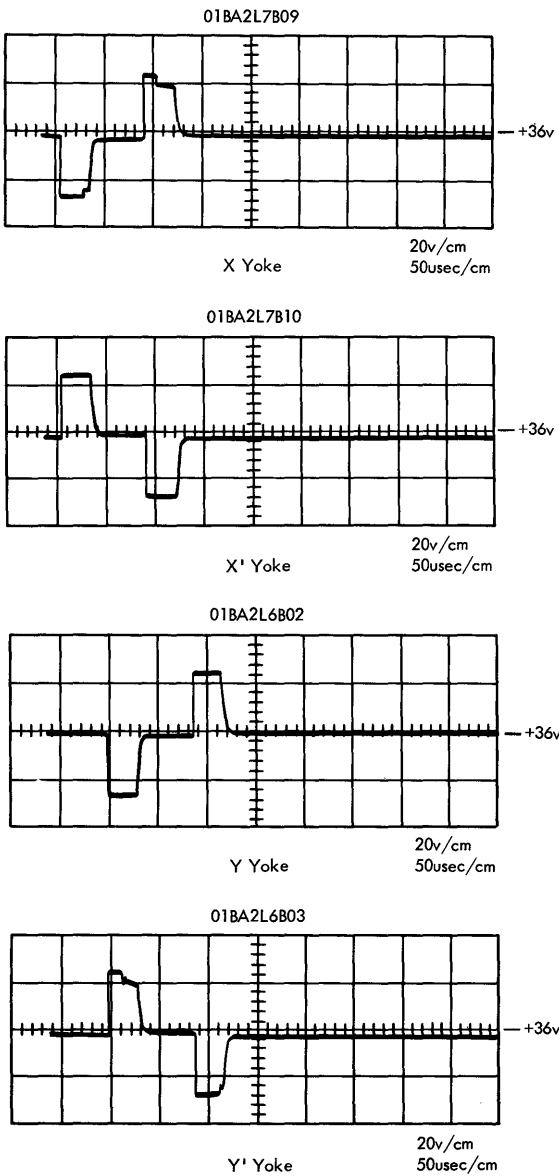


Figure 1-13. Yoke Waveforms, Bit 0, and Bits 5 Through 9 Active

22. Observe change in waveform at 01BA2L6D07 as shown in Figures 1-12 and 1-14.
23. Observe asynchronous delay waveforms at 01BA2G4B02, 01BA2G5B12, and 01BA2G3B02. They should be as shown in Figure 1-15.

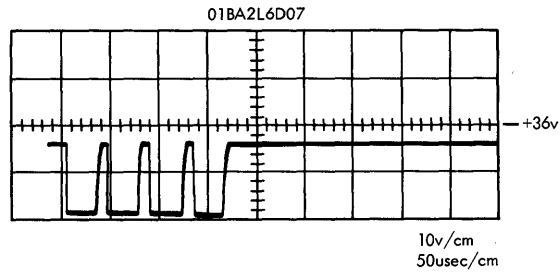


Figure 1-14. Position Isolation Output, Yoke Clamped

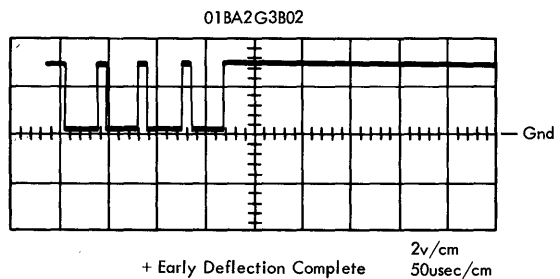
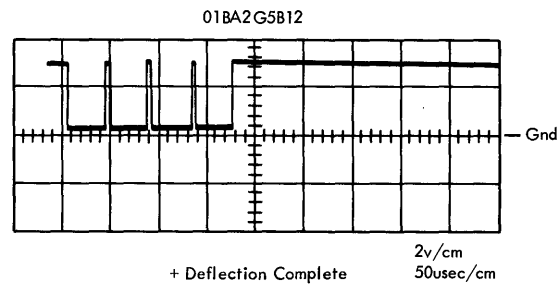
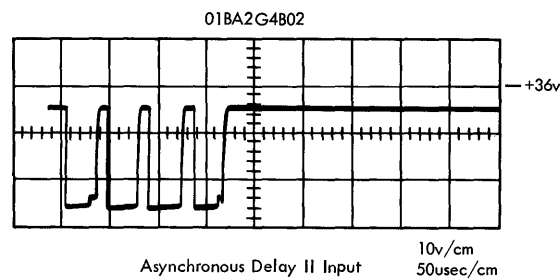


Figure 1-15. Asynchronous Delay Waveforms

24. Observe blank-unblank waveforms at 01BA2J7B13 and 01BA2J6B04. They should be as shown in Figure 1-16.
25. Turn off power, and install X and Y bits 1 and 4, card PN 5800829, in locations 01BA3J4/J5 and 01BA3D4/D5.
26. Turn on power, and check CRT for approximately a 9-1/2-inch square. (Waveforms will be essentially the same. The only difference will be longer times because of longer deflection distances.)

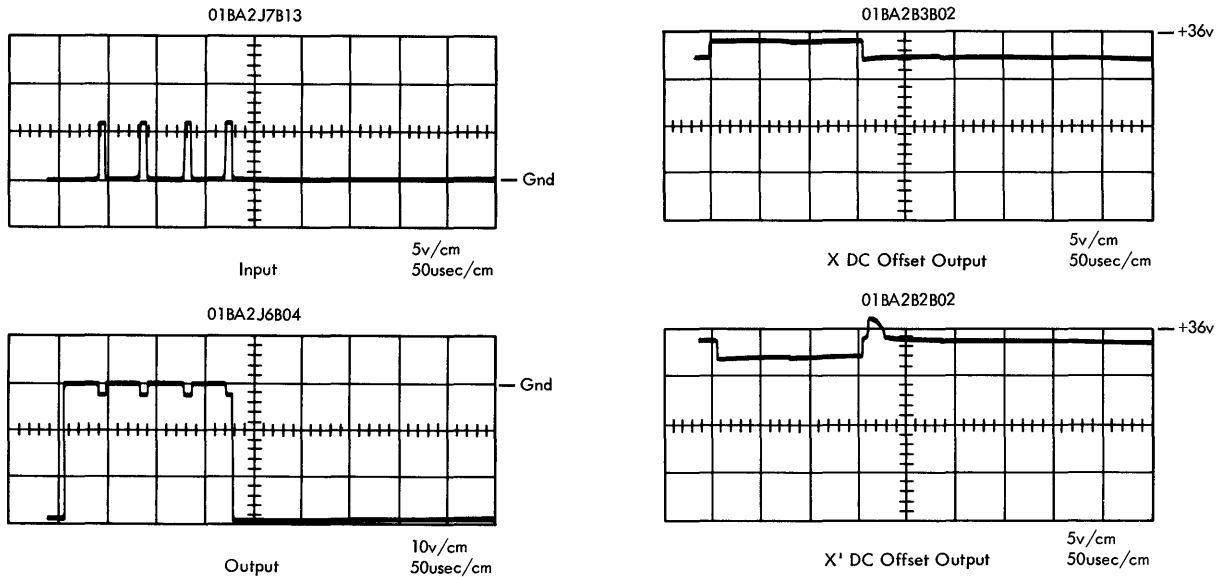


Figure 1-16. Blank-Unblank Waveforms

27. Turn off power, and install bits 2 and 3, card PN 5801304, in locations 01BA3E4/E5 and 01BA3K4/K5.
28. Turn on power, and check CRT for approximately a 12-inch square. (Waveforms will be essentially the same. The only difference will be longer times because of longer deflection distances.)
29. Insert DC offset cards (PN 5801309) in 01BA3D2/D3 and 01BA3K2/K3. Install low-order DC offset card (PN 5807042) in 01BA3E2 and 01BA3J2. Scope at points indicated in Figure 1-17.
30. At this point, the analog deflection system is operating correctly and should be capable of being aligned. Display normal analog alignment program (#766 pattern 1), and align as prescribed in paragraph 4.2. That is, adjust size, centering, dc offset, damping, bit weights, and brightness controls.
31. Turn off power, and insert dynamic intensity II, card PN 5804733, in location 01BA2K6/K7. With power on, but before starting program, measure voltage at 01BA2L6D07. Adjust card-mounted potentiometer in location 01BA2L6/L7 for a 0.5v negative level with respect to +36v. Using Full Square program, scope at 01BA2K7D07 (maximum positive amplitude depends on vector contrast control setting). See Figure 1-18.

#### 1.5.1 De-Skew Check

1. Turn off dc power.
2. Insert de-skew card (PN 5801305) in

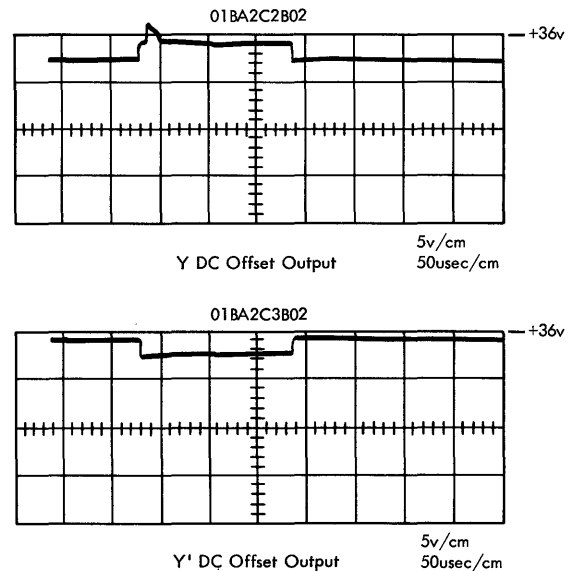


Figure 1-17. DC Offset Outputs

01BA2M6/M7 and card PN 5800828 in 01BA2H4/H5.

3. Turn on power.
4. Using normal De-Skew Alignment program (pattern 5 of program F756 or F766), adjust single-shot in 02BB1F2D02 for a negative pulse whose trailing edge occurs 100ns before the positive transition of TP6 at 02BB1H6B09. (Refer to Note 13 of Figure 4-6 for SS adjustment.) Adjust single-shot in 02BB1E2D13 (middle) to minimize any irregularities on CRT.

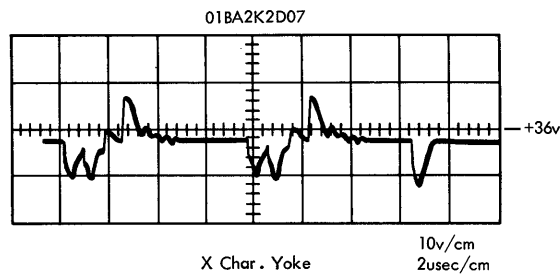
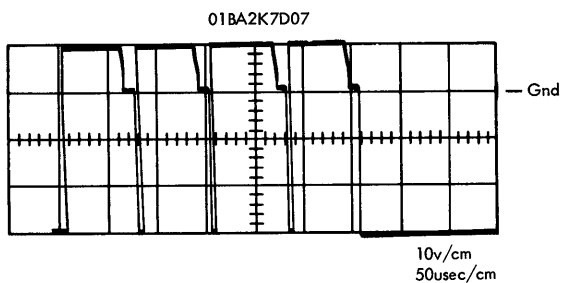


Figure 1-18. Position System Dynamic Intensity II Output

### 1.5.2 Character Generator Check

1. Turn off power.
2. Insert character reference voltage card (PN 5804246) in location 01BA2J4/J5.
3. Turn on power.
4. Check voltage at 01BA2J4D09 with Simpson 270 (or equivalent) meter while rotating the X CHAR SIZE potentiometer. This voltage should vary approximately 1v somewhere in the range of +4.0v to +6.3v.
5. Check 01BA2J4B04, and rotate Y CHAR SIZE potentiometer. This voltage should vary approximately 1v somewhere in the range of 4.0v to 6.3v.
6. Turn off dc power, and insert the following character cards:
  - X buffer 5804247 in location 01BA2K2/K3.
  - Y buffer 5804247 in location 01BA2L2/L3.
  - X driver 5804248 in location 01BA2J2/J3.
  - Y driver 5804249 in location 01BA2M2/M3.
7. Turn on dc power. Load the character program (program #2), and, if required, perform the following operations while observing the CRT:
  - a. While observing the character "A", adjust X, X', Y, Y' CHAR DAMPING potentiometers for the best straight lines and so that the end points are not dropped.
  - b. Adjust X and Y CHAR SIZE controls. The character size should be adjusted for Y displacement of approximately 0.160 inch and X displacement of approximately 0.120 inch. (Character overdrive is still out; therefore, spacing for the second "A" may not be correct.)

The character yoke waveforms should be as shown at the indicated points in Figure 1-19.

8. Turn off dc power, and insert character overdrive card (PN 5800830) in location 01BA3E3.
9. Turn on dc power.
10. Check to ensure that single-shot located in 02BB1F3B02 is set for approximately 2.75usec

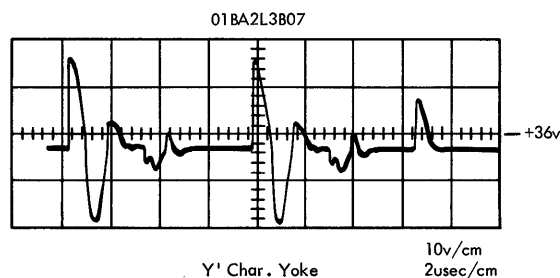
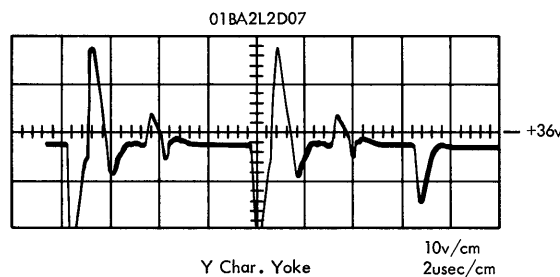
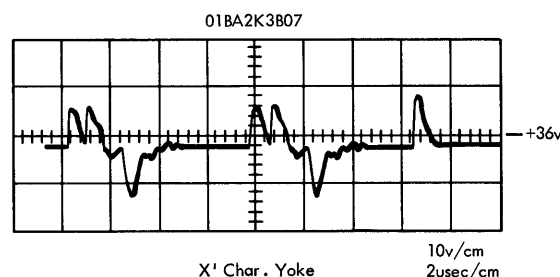


Figure 1-19. Character Yoke Waveforms

and that single-shot located in 02BB1G2B02 is set for approximately 3.0usec (for B-size characters). (See Note 13 of Figure 4-6 for method of adjusting SS.)

11. Use character program #2, and adjust single-shot located in 01BA3M6B02 until characters become distorted. Reverse adjustment slightly until characters are normal. Spacing between the characters should now be corrected.
12. Remove dc power, and insert character isolation card (PN 5804732) in 01BA2H2/H3. Insert dynamic intensity II card (PN 5804733) in 01BA2H6/H7. Turn on dc power, but, before starting program, measure voltage at



01BA2H2D07. Adjust card-mounted potentiometer in location 01BA2H2/H3 for 0.5v negative level with respect to +36v. Using the Character program, scope at 01BA2H7D07 (maximum positive amplitude dependent on setting of character contrast control). See Figure 1-20.

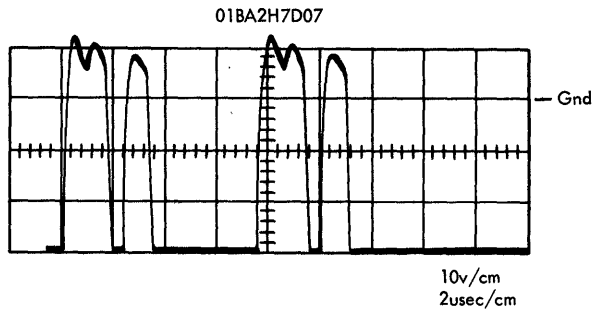


Figure 1-20. Character System Dynamic Intensity II Output

### 1.5.3 Light Pen Check With GDF

Use program F76B for this check. If the proper intensity alignment procedure has been followed as specified in paragraph 4.2.2, step 1, correct light pen alignment and operation will be obtained if the operator's brightness control is set fully clockwise (maximum brightness).

Perform light pen check as follows:

1. Remove dc power, and insert light pen verification card in 01B-A2B6. Turn on dc power, run program, and check display for intensity distortion (broken vectors or noise on CRT).
2. If no intensity distortion is present, remove dc power, and install light pen amplifier card (PN 5807078) in 01E-A1.

NOTE: Do not operate the Light Pen Detect switch during alignment.

3. Turn on dc power and run program. Place LP ALIGN switch (potentiometer panel) in ON position. This will affect targets as follows:
  - a. Distortion to a character.
  - b. A partial blanking of a vector near the pen.
  - c. A small unblanked vector will appear displaced down and to the left from a detected point.
4. Place LP ALIGN switch in OFF position.

### 1.5.4 Light Pen Check Without GDF

Use program F784 for this check. If the proper intensity alignment procedure has been followed as specified in paragraph 4.2.2, step 1, correct light pen alignment and operation will be obtained if the operator's brightness control is set fully clockwise (maximum brightness).

Perform light pen check as follows:

1. Remove dc power, and insert light pen verification card in 01B-A2B6. Turn on dc power, run program, and check display for intensity distortion (broken vectors or noise on CRT).
2. If no intensity distortion is present, remove dc power, and ensure that light pen paddle card is in 01BA2A5.
3. Insert light pen amplifier card (PN 5801306) in 01BA2B4/B5.
4. Turn on dc power, and measure level at 01BA2B5B07. Voltage should be +10v  $\pm$ 1v.
5. Measure dc level at 01BA2B5B13. Voltage should be +33v  $\pm$ 0.5v.
6. Align light pen as described in paragraph 4.2.8.

### 1.5.5 AVG Check

1. Turn off power, and insert 30v reference supply cards in the following locations:
  - a. Heat sink and 042 transistor, PN 5801690; install in 01AA2H2/H3.
  - b. Heat sink and Zener diode, PN 5801689; install in 01AA2K2/K3.
  - c. Reference voltage amplifier, PN 5801688; install in 01AA2M2/M3.
2. Apply power, and (using Simpson 270 meter or equivalent) measure the voltage from pin locations 01AA2H2B08 and 01AA2H2B09 to ground as the REF VOLTS potentiometer on the 01AA1 potentiometer panel is varied from maximum clockwise to maximum counter-clockwise. Voltage at the pins should vary from at least +28vdc to +32vdc. Adjust this voltage to +29vdc  $\pm$ 0.1v.
3. With power off, insert card PN 5801685 in location 01AA2G4/G5. Apply power, and display the vector graphic alignment pattern (Program Set 767/757).
4. Scope 01AA2G4B03 (sync at 02BB1J2B04), and ascertain that square wave is 2.5usec  $\pm$ 1 percent in width for both positive and negative transitions. (The delay line is located at 01AA2G6.)
5. Scope 02BB1K2D12, and (using upper potentiometer) adjust the negative pulse for 200ns  $\pm$ 5 percent.

6. Scope 02BB1M6D12, and (using upper potentiometer) adjust the negative pulse for 250ns  $\pm 10$  percent.
7. Ensure that BIT 4 control on 01AA1 potentiometer panel can vary the second set of 45-degree double-traced lines at the four corners of the display. Adjust for minimum spacing between lines.
8. Remove power, and insert card PN 5801686 in location 01AA2H4/H5. Apply power, and ensure that BIT 3 control on 01AA1 potentiometer panel can vary the third set of 45-degree double-traced lines at the four corners of the display. Adjust for minimum spacing between the lines.
9. Remove power, and insert card PN 5801684 in location 01AA2J4/J5. Apply power, and ensure that BIT 2 control on 01AA1 potentiometer panel can vary the fourth set of 45-degree double-traced lines at the four corners of the display. Adjust for minimum spacing between the lines.
10. Remove power, and insert card PN 5801687 in location 01AA2K4/K5. Apply power, and ensure that BIT 1 control on 01AA1 potentiometer panel can vary the fifth set of 45-degree double-traced lines at the four corners of the display. Adjust for minimum spacing between the lines.
11. Remove power, and insert two PN 5801687 cards in locations 01AA2L4/L5 and 01AA2M4/M5. Apply power, and ensure that BIT 0 controls on 01AA1 potentiometer panel can vary the diagonals on the 12-inch by 12-inch display. Adjust for minimum spacing between the lines.
12. Normal AVG alignment should now be made as prescribed in paragraph 4.2.9.
13. With the exception of the waveforms in Figure 1-21, the previously shown waveforms should not be altered (except a longer time base) as a result of the absolute vector graphic feature. Use the Full Square program, sync at 02BB1J2B04, and scope at points called out in Figure 1-21.

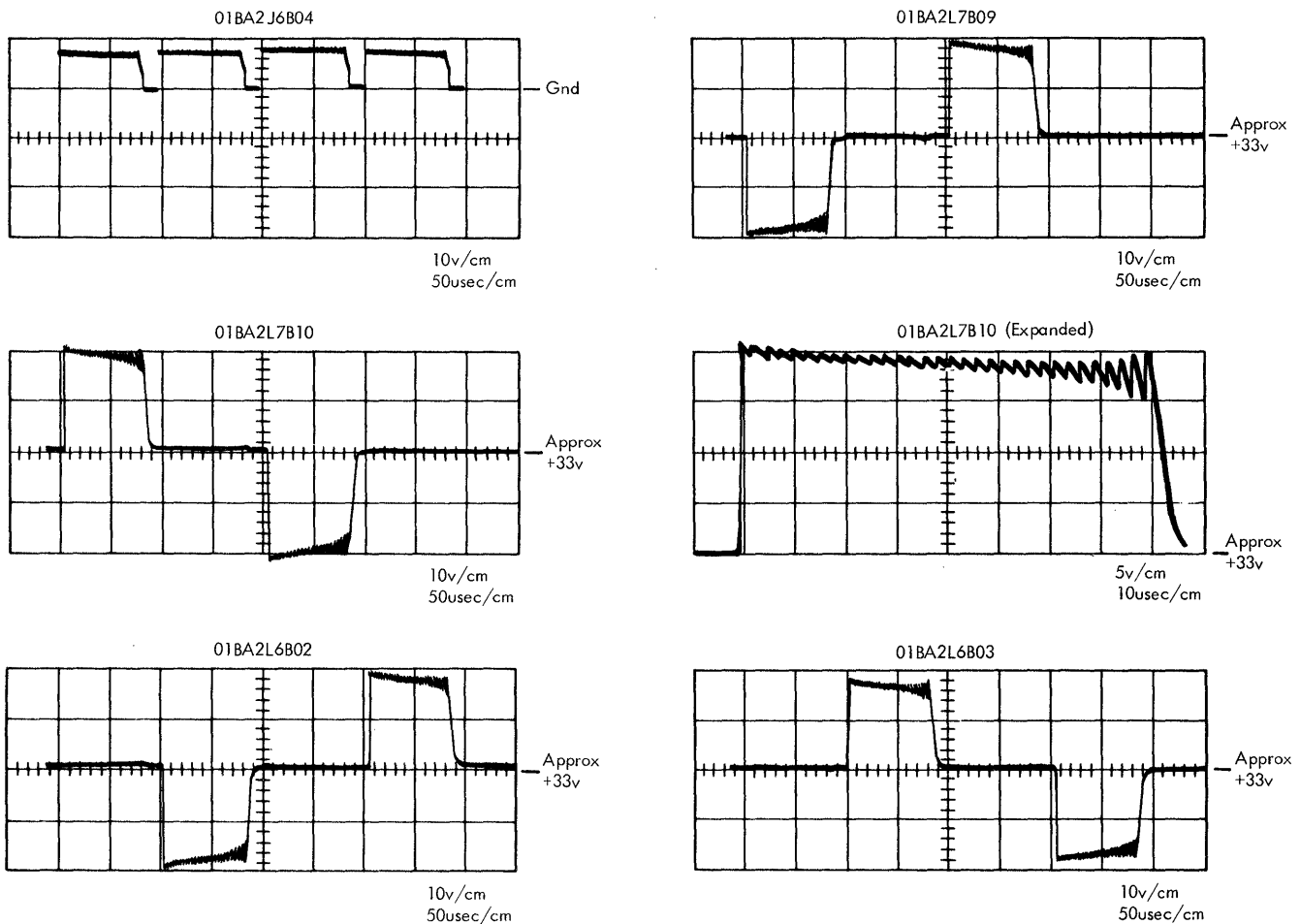


Figure 1-21. AVG Waveforms

### 1.5.6 Program 1, Full Square

The following procedure results in a 12-inch by 12-inch full square display. The program is loaded from the CE panel as follows:

1. Set LOAD SELECT switch to BUFFER position, and place REGENERATE switch in the off (down) position.
2. Depress MACHINE RESET.
3. Place switches in the order listed below, and depress ENTER switch after each setting:
  - a. 2A
  - b. 82
  - c. 2A
  - d. 02
  - e. 0F  
FC  
00  
00
  - f. 0F  
FC  
0F  
FC
  - g. 00  
00  
0F  
FC
  - h. 00  
00  
00  
00
  - i. 2A
  - j. FF
  - k. 00
  - l. 00

4. Depress MACHINE RESET.
5. Start regeneration.

### 1.5.7 Program 2, "A" Characters

The following procedure results in a display of two "A" characters on the left center of the CRT. The program is loaded from the CE panel as follows:

1. Set LOAD SELECT switch to BUFFER position, and place REGENERATE switch in the off (down) position.
2. Depress MACHINE RESET.
3. Set switches in the order listed below, and depress ENTER switch after each setting:
  - a. 2A
  - b. 82
  - c. 2A
  - d. 02
  - e. 40
  - f. 00
  - g. 08
  - h. 00
  - i. 2A
  - j. 40
  - k. C1
  - l. C1
  - m. 2A
  - n. FF
  - o. 00
  - p. 00
4. Depress MACHINE RESET.
5. Start regeneration.

### SECTION 3. SYMPTOM INDEX

Field Engineering generates and distributes the Symptom Index. Insert this index following this page.

### SECTION 4. SERVICE AIDS

Field Engineering generates and distributes Service Aids. Insert these service aids following the Symptom Index.

## CHAPTER 2. MAINTENANCE FEATURES

This chapter outlines and briefly describes the features of the 2250-1 that are provided to aid the CE during scheduled and corrective maintenance. The feature include the operator, power, and manual controls and indicators (CE panel and analog potentiometer panel) and the program-monitoring capabilities provided by the sense and status bytes and the Read XY Position command.

### 2.1 OPERATOR CONTROLS

The operator controls, located along the right side of the tube housing, are briefly described as follows:

BRIGHTNESS LIMITING	
POTENTIOMETER:	Limits CRT intensity.
BRIGHTNESS:	Adjusts CRT intensity.
LINE/VECTOR CONTRAST:	Adjusts line and vector contrast.
CHARACTER CONTRAST:	Adjusts character contrast.
POWER ON:	Initiates power-on sequence if REMOTE/LOCAL switch is set to LOCAL position.
POWER OFF:	Drops power if REMOTE/LOCAL switch is in LOCAL position.

### 2.2 POWER SUPPLY PANEL

The power supply panel is located under the console station.

REMOTE/LOCAL:	The power-on/-off sequences are controlled by the system power contacts when REMOTE/LOCAL switch is in REMOTE position. The power-on/-off sequences are controlled by POWER ON and POWER OFF console switches when REMOTE/LOCAL switch is in LOCAL position.
THERM RESET:	Restores power after a thermal condition when the thermal condition has cooled and no power control switches have been operated. If one of the power control switches has been operated, THERM RESET is ineffective.
LINE BREAKER:	Removes power from entire power system when primary power input is overloaded.
HIGH VOLTAGE ON:	When lit, indicates that the 16kv supply is on.

CB ALARM:	Indicates that one of the CB's has tripped.
THERM ALARM:	Indicates that operating temperatures have exceeded a safe level.
24V CONTROL:	Indicates a fuse blown in the 24v supply.

### 2.3 CE PANEL CONTROLS AND INDICATORS

#### 2.3.1 Controls

All CE panel controls except IND TEST, MACHINE RESET, and the FEATURE ENABLE switch are inoperative unless the machine is logically disabled and the CE Key switch is in the CE position. (See FEDM Figure 9006.) In the following list, if a feature is required to activate a control, the feature is identified:

IND TEST:	Checks all operational indicators when depressed.
MACHINE RESET:	Resets all registers and controls when depressed.
INTERFACE OUT:	Seven switches that simulate the interface control signals from the channel. In the down position, they simulate the 2250 response to the control signals.
BUS OUT:	Nine switches that simulate bus out data from the channel.
LOAD SELECT:	Four-position switches that select areas to be loaded with data from Bus Out switches. The four positions are: <ol style="list-style-type: none"> <li>1. BAC HIGH - Enters data into the high-order positions of the BAC.</li> <li>2. BAC LOW - Enters data into the low-order positions of the BAC.</li> <li>3. BUFFER - Permits data entry into the 2250-1 buffer.</li> <li>4. REG B - Permits data entry into registers A and B.</li> </ol>
ENTER:	Transfers contents of BUS OUT switches to area selected by LOAD SELECT switch.
CURSR:	This switch removes (REMV) or inserts (INS) a Cursor bit when LOAD SELECT is in BUFFER or REG B position and ENTER switch is depressed.
TPD MODE:	A two-position switch that selects mode of TPD operation as follows: <ol style="list-style-type: none"> <li>1. AUTO NORM - TPD operates at machine speed.</li> </ol>

2. SINGLE STEP - TPD generates one pulse for each depression of SINGLE STEP pushbutton.

**SINGLE STEP:** Causes TPD to generate a single pulse when TPD MODE switch is in SINGLE STEP position.

**READ BUFFER:** Depressing this switch causes contents of buffer address to be read into register B. Releasing the switch writes the information back into the buffer and steps BAC to next-higher address. Repeated operation sequentially steps through any portion of the buffer. (Buffer feature required.)

**REGENERATE SINGLE MODE:** Regeneration starts from address contained in BAC and stops when next SM code is decoded. (Buffer feature required.)

**REGENERATE CONT:** Allows CE to start regeneration from address contained in BAC. Regeneration continues until switch is turned off and next SM code is decoded. (Buffer feature required.)

**BYPASS CHK STOP:** Allows bypassing of Check Stops resulting from a parity error in register B if 2250-1 is in Off Line mode.

**REPEAT CHAR:** Permits recycling character generator on the same character (character code must be in register A). (Character generator feature required.)

**SINGLE STROKE:** Permits character generator to be stepped through a character, one stroke at a time, each time switch is depressed (character code must be in register A). (Character generator feature required.)

**FEATURE ENABLE:** A row of seven switches that must be set to agree with the combination of features present on the machine. One or more features may be logically disabled as an aid to failure location.

**BFR:** A toggle switch that is set to correspond with the buffer capacity.

**INDICATOR SELECTOR:** An eight-position rotary switch (mounted on side of CE panel) that provides the ability to assign two rows of 10 indicators each to a any one of eight machine functions.

Assignment of switch positions is described in paragraph 2.3.2 under "Switched Indicators."

### 2.3.2 Indicators

All indicators are mounted on the CE panel (FEDM Figure 9006) except sense byte 0, which is located to the left of the CRT under the table top. In the list that follows, the feature that is required to activate the indicator is identified.

#### Sense Byte 0 (4 indicators)

**Command Reject (bit 0):** Indicates an invalid modifier bit in the command or an invalid command sequence.

**Bus Out Check (bit 2):** Indicates a parity error on Bus Out (command or data byte).

**Data Check (bit 4):** Indicates that a buffer parity error has occurred during a read operation or a buffer service. (Buffer feature required.)

**Buffer Running (bit 6):** Indicates that buffer is being regenerated. (Buffer feature required.)

#### Sense Byte 1 (3 indicators)

**L PEN DET (bit 0):** Indicates an output from light pen. (Light pen detection feature required.)

**E O SEQ (bit 1):** Indicates that an End Order Sequence has been detected.

**CHAR (bit 2):** Set when in Character mode.

#### Status Byte (5 indicators)

**ATN (bit 0):** Indicates a service request from features (such as A/N keyboard, program function keyboard, or light pen). It is also used with UNIT CHK light to indicate errors during a buffer regeneration cycle. End Order Sequence also sets Attention bit and lights the indicator.

**BUSY (bit 3):** Indicates that an interrupt condition exists.

**CHAN END (bit 4):** Indicates that the transfer of data or control information between unit and channel is complete.

**DEV END (bit 5):** Indicates that device has completed the previous command and is free to accept a new one.

**UNIT CHK (bit 6):** Indicates programming or equipment error conditions at the 2250-1. Unit Check is also set by Light Pen Detection and End Order Sequence.

INTERFACE OUT:	A row of seven indicators to enable monitoring Bus Out tags from channel.	STA STKD	The console has pending status which is available to the channel.
INTERFACE IN:	A row of six indicators to enable monitoring console response to Bus Out tags from channel.	I/O RESET	Indicates a machine reset initiated by the channel.
Switched Indicators:	Two rows of indicators (10 in each row) that display each of the eight machine functions selected by rotary switch mounted on side of CE panel. The eight positions are: 1. BUS OUT/BUS IN 2. REG B/REG A 3. ASSEMBLY REG/REG A-B INPUTS 4. XY DEFL REG 5. BUFFER ADR CTR 6. BUFFER ADR REG 7. XY SUM STORE 8. STROBE CTR/REG	MODE:  REMEMBER:	Consists of four indicators that display the present mode of operation. Indicates which control latches will be sampled after the buffer cycles. The latches, if set, cause TPD to generate pulse that corresponds to title of the set latch. For example, if REMEMBER 7 is set, the TPD generates a TP7 pulse before continuing or terminating operation in progress.
COMMAND REGISTER:	Indicates bits (0-7) of command byte. The contents of this register are used to drive the command decoder.	DIGITAL CHARACTER CONTROLS:	These indicators monitor operation of character generator controls and the functions required to properly space characters being displayed on CRT.
CMND DCDR OUTPUTS:	Indicate which command is being decoded.	CONNECT DATA	The character generator is receiving data from register A. (Character generator feature required.)
TIMING PULSE DISTRIBUTOR:	A row of seven indicators that allow monitoring TPD operation as follows:	CURSR	The character generator will generate a cursor instead of a character. (Character generator feature required.)
WAIT 1	A 1-pulse delay is in progress. (Buffer feature required.)	ADD X14	The main beam will be stepped 14 raster units of X deflection for an A size character. (Character generator feature required.)
STR	Indicates the presence of starting pulse.	ADD X21	The main beam will be stepped 21 raster units of X deflection for a B size character. (Character generator feature required.)
TPD's 1, 2, 4, 8, and 16:	Indicate encoded number of TP trigger that is set; e.g., TPD 11 trigger turns on indicators 1, 2, and 8.	ADD Y 20	The main beam will be stepped 20 raster units of Y deflection for an A size character. (Character generator feature required.)
BASIC CONTROLS:	These controls are associated with the transmission interface control (TIC) and indicate interface activity as follows:	ADD Y 30	The main beam will be stepped 30 raster units of Y deflection for a B size character. (Character generator feature required.)
SERV REQ	Device request service.	SIZE B	Expanded characters will be displayed. (Character generator feature required.)
WORD HOLD	A multibyte transfer of information across interface is in process.	DEFLECTION:	These indicators allow monitoring of deflection controls.
CH REQ	The channel is selecting the 2250-1.	INTLK	Indicates that beam deflection is in progress and another deflection cannot start until interlock is reset.
IRPT	Display requires selection by channel.	UNBLK	Beam intensified.
STOP	Indicates that channel is ending current operation.	PT/LINE	When lit, a point is displayed; when not lit, a line is drawn.
CNSL SEL	A command is being executed.	COMPLT	Analog deflection is complete.
I/O DISC	A Halt I/O signal has been received from channel.		

COMPLT WAIT	Digital logic is waiting for Deflection Complete latch to be set.	SHIFT KEY	Indicates that a shift to upper case has been selected.
ANALOG CONTROLS:	These indicators allow monitoring of the analog controls, as follows:	EOM	Indicates that End of Message key has been depressed.
PERMIT N DPLY	Indicates that the last character has been completed and that a new character can be requested. (Character generator feature required.)	CURSOR BKSP	Indicates that Backspace key has been depressed and that cursor will be backspaced when recognized.
DCD CPLT	Indicates that the last stroke is in progress and register A contents may be changed. (Character generator feature required.)	ADV	Indicates that Advance key has been depressed and that cursor will be advanced when recognized.
PERMIT M B DFL	Indicates that beam can be repositioned to display next character. (Character generator feature required.)	CNCL	Indicates that Cancel key has been depressed.
GATED	Indicates permission (delayed) to position next character. (Character generator feature required.)	JUMP	Indicates that Jump key has been depressed and that Jump Cursor function will be performed.
BYTE CTR:	Displays stages 1, 2, and 4 of a binary counter that counts bytes of data obtained from CPU or from buffer during regeneration.	<b>PROGRAM FUNCTION KEYBOARD</b> (program function keyboard feature required):	
LOAD CTR:	Displays stages 1 and 2 of a binary counter used to count incoming command bytes from channel.	DATA AVL	Indicates that a key has been depressed and that coded data is ready to be transferred to channel.
BUFFER CONTROLS:	These indicators allow monitoring of buffer controls as follows: (Buffer feature required.)	CODE BITS	Display the code generated by depression of a key.
BFR ADR CTR		MANUAL INPUTS:	These indicators indicate the contents of MI sense byte which informs the CPU what type of MI message is forthcoming:
STEP	Indicates that BAC will be stepped.	ALPHA KB	An alphameric keyboard message follows. (Alphameric keyboard feature required.)
+1	Indicates that BAC count will be increased by 1.	PFKB	A program function keyboard message follows. (Program function keyboard feature required.)
-1	Indicates that BAC count will be decreased by 1.	END	Indicates End of Message key has been depressed. (Alphameric keyboard feature required.)
CURSOR		CNCL	Indicates Cancel key has been depressed. (Alphameric keyboard feature required.)
CLEAR	Indicates that a cursor bit in buffer will be reset to 0.	REGENERATE	These indicators permit monitoring condition of regeneration controls as follows:
SET	Indicates that a cursor bit in buffer will be set to 1.	CONTROLS:	
SET SERV REQ:	Indicates that a data byte will be requested from channel and stored in buffer.	CURSOR	
<b>ALPHAMERIC KEYBOARD</b> CONTROLS (alphameric keyboard feature required):		JUMP	A Cursor Jump is in progress.
INS CODE	Indicates that new data will be inserted (stored) in buffer in place or original data.	JUMP PROT	Set when in Protected Character mode.
DATA AVL	Indicates that keyboard key has been depressed and information is available for processing.	OP	The Advance, Backspace, or Jump keyboard key has been depressed and recognized by digital logic.



BKSP LIMIT	Prevents backspacing into an Enter Character Mode control order.
SET MODE	
PROT	Prevents advancing into an Enter Character Mode control order.
SKIP	A four-byte control order is being executed.
SRCH	Next byte could be a Set Mode order.
MODE CODE SRCH	Decode next byte (if 2A HEX) as a Mode Code.
STOP SYNC	Stop regeneration after next SM.
STOP	Regeneration is stopping.
EVEN COUNT	
DATA	Keeps track of odd or even bytes of data. The count is even when indicator is on.
LIGHT PEN:	These indicators allow monitoring light pen controls as follows: (Light pen feature required.)
SYNC	Light Pen Activate switch is closed.
ACTIVE	Light pen is enabled.
DET	Indicates that light pen has detected a target.
BIT A ASM REG:	Indicates a conditional intensification of beam when in Vector Graphics mode. (Absolute vector graphics feature required.)
ABS:	Indicates that display unit is in Absolute Vector Graphics mode.
CMPTA:	Indicates a new $\Delta X$ and $\Delta Y$ are being computed by the display unit.
$\Delta$ COUNTER:	Indicates contents of counter controlling switches that switch the damping resistors in and out for linear deflection.

REGEN ON/OFF:

\*MACH RESET:

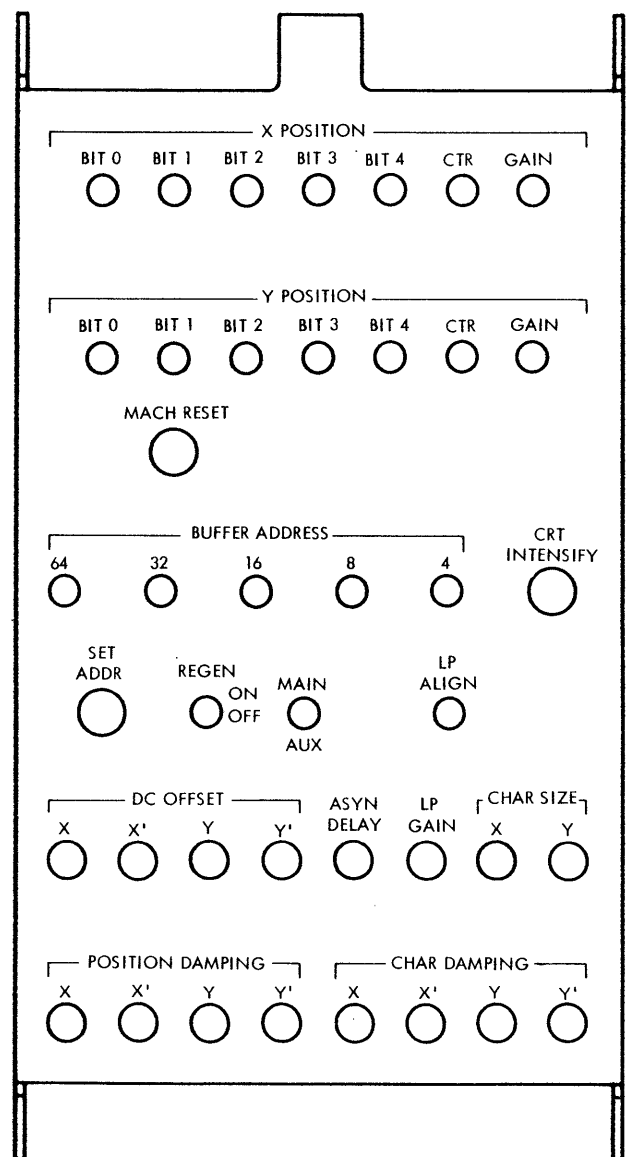
addresses will contain transfer orders to blocks of core storage which contain various analog alignment patterns. (Buffer feature required.)  
Performs same function as REGENERATE CONT switch described in paragraph 2.3.1. (Buffer feature required.)  
Performs same function as MACHINE RESET switch described in paragraph 2.3.1.

## 2.4 ANALOG POTENTIOMETER PANEL CONTROLS

The analog potentiometer panel is shown in Figure 2-1.

### 2.4.1 Switches

*BUFFER ADDRESS:	These switches provide the ability to set bits 4, 8, 16, 32, and 64 of BAC by selecting desired address and depressing SET ADDR button. (Buffer feature required.)
*SET ADDR:	Sets BAC to address selected by Buffer Address switches when depressed. This maintenance feature allows the CE to select any of the 32 addresses of core storage. These



Note:  
LP GAIN not used when GDF is installed.

Figure 2-1. Analog Potentiometer Panel

- \*MAIN/AUX: Selects either the auxiliary or main buffer storage. Auxiliary storage is provided for manual insertion of small exercising programs for troubleshooting and maintenance. (Buffer feature required.)
- \*LP ALIGN: Allows visual indication of light pen detection.
- \*CRT INTENSIFY: Intensifies beam by overriding the blank level.

\*These switches are operative in both CE and on-line modes.

**CAUTION**

Before using this switch, turn BRIGHTNESS control fully counterclockwise. After depressing button, slowly advance BRIGHTNESS control until beam is intensified.

**2.4.2 Potentiometers**

- X POSITION
  - BIT 0 through BIT 4 Establish weight of respective bits in X.
  - CTR Determines horizontal center of display.
  - GAIN Determines horizontal size of display.
- Y POSITION
  - BIT 0 through BIT 4 Establish weight of respective bits in Y.
  - CTR Determines vertical center of display.
  - GAIN Determines vertical size of display.
- DC OFFSET (X, X', Y, Y'): Corrects for yoke half-axis dc voltage drops.
- ASYN DELAY: Establishes total time required by an analog area for each position change.
- LP GAIN: Establishes firing-point level for light pen. (Not used with GDF.)
- CHAR SIZE (X, Y): Determines overall character height and width for both standard and expanded size character.
- POSITION DAMPING (X, X', Y, Y'): Adjusts position-yoke time constant for X and Y axis.
- CHAR DAMPING (X, X', Y, Y'): Adjusts character-yoke time constant for X and Y axis.

**2.5 PROGRAM MONITORING**

**2.5.1 Sense and Status Bytes**

Through proper programming, the 2250-1 will detect interface error conditions and, with the buffer

feature, erroneous data resulting from a buffer error condition. Detected errors are presented to the CPU in the form of sense and status bytes. Combinations of bits are set in these bytes to indicate the type of error.

Detectable interface errors and responses are as follows:

1. Invalid modifier bits. The 2250-1 is not equipped with the feature or features necessary to execute the command (Initial Status):
  - Status byte - Unit Check (bit 6)
  - Sense byte - Command Reject (bit 0)
2. Parity error in command byte (Initial Status):
  - Status byte - Unit Check (bit 6)
  - Sense byte - Bus Out Check (bit 2)
3. Write or Read command given with the buffer running (Initial Status):
  - Status byte - Unit Check (bit 6).
  - Sense byte - Command Reject and Buffer Running (bits 0 and 6)
4. Insert or Remove Cursor command given with the buffer running (Initial Status):
  - Status byte - Unit Check (bit 6)
  - Sense byte - Command Reject and Buffer Running (bits 0 and 6)
5. Parity error on Write (Ending Status):
  - Status byte - Unit Check, Device End, and Channel End (bits 6, 5, and 4, respectively)
  - Sense byte - Bus Out Check (bit 2)
6. Parity error on Read Buffer (Ending Status):
  - Status byte - Unit Check, Device End, and Channel End (bits 6, 5, and 4 respectively)
  - Sense byte - Data Check (bit 4)

**2.5.2 Read XY Position Register Command**

The Read XY Position Register command is a non-operational command that is used only for diagnostic purposes. This command enables the processor to compare the XY position data with an expected value. Buffer regeneration must be stopped before the command is issued. The XY position is transferred in four bytes. The byte format is shown below.

Byte 1		Byte 2		Byte 3		Byte 4	
Note 1	X Position				Note 1		
Note 1	Y Position				Note 1		
0	3	4			13	14	15

Note 1: Bits 0-3, 14, and 15 are always zero.

## 2.6 CE OPERATING PROCEDURES

This section contains the step-by-step procedures required to simulate the 2250-1 Command and Display Generation routines by using the manual controls of the CE panel.

### 2.6.1 Command Performance

This section contains information that will enable manual simulation, at the CE panel, of the standard interface lines and controls. Step-by-step procedures are described in the following paragraphs.

#### 2.6.1.1 Prepare Unit for Manual Control

1. Place unit off-line as described in paragraph 1.1.4.
2. Set FEATURE ENABLE switches in upper positions to correspond with features on unit. All other switches on CE panel should be in lower position.
3. Depress MACHINE RESET pushbutton.
4. Turn Register Indicator knob to BUS OUT/BUS IN (position 1).

#### 2.6.1.2 Initial Selection Sequence

The initial selection sequence is performed by operation of the INTERFACE and BUS OUT switches as described in the following procedure. The indicator condition associated with each step is shown below each switch operation.

1. Set BUS OUT switches to upper position to correspond with unit address (address that selects this unit). Set BUS OUT P switch for odd parity.
2. Set OP OUT (raise Operational Out). OP OUT, on.
3. Set ADR OUT (raise Address Out)
  - a. ADR OUT, on
  - b. CH REQ, on
4. Set HOLD OUT (raise Hold Out). HOLD OUT, on.
5. Set SEL OUT (raise Select Out)
  - a. SEL OUT, on
  - b. OP IN, on
6. Set ADR IN (drop Address Out)
  - a. ADR OUT, off
  - b. ADR IN, on
  - c. Unit address on Bus In register.
7. Set command desired in BUS OUT switches. Typical commands are:
  - a. Set BAC and Stop (0 0 0000 0111)
  - b. Write Buffer (0 0 0000 0001)
  - c. Read Buffer (0 0 0000 0010)
  - d. Sense (0 0 0000 0100)

Interface control proceeds with a service cycle sequence if the decoded command entails data transfer or proceeds with an ending sequence if no data transfers are involved.

8. Set CMND OUT (raise Command Out)
  - a. CMND OUT, on
  - b. COMMAND REGISTER contains the command placed in the BUS OUT in step 7.
  - c. CMND DCDR OUTPUT indicator corresponding to the command selected in step 7, on.
  - d. ADR IN, off
9. Set STA IN (drop Command Out)
  - a. CMND OUT, off
  - b. STA IN, on
  - c. Zero status on Bus In register (100000000)
10. Set SERV OUT (raise Service Out)
  - a. SERV OUT, on
  - b. CH REQ, off
  - c. STA IN, off
  - d. CNSL SEL, on
  - e. SERV REQ, on
  - f. LOAD CTR, clear
  - g. BUSY, on
  - h. Step BAC (Write command only)
  - i. REQ IN, ADPT REQ ON (Sense command only)

#### 2.6.1.3 Set BAC and Stop

When the Set BAC and Stop command is given, the initial selection sequence is followed by a service cycle request. In this sequence, the number of data transfers (two bytes) is determined by the display unit.

1. Set SERV IN (drop Service Out)
  - a. SERV OUT, off
  - b. SERV IN, on
  - c. WORD HOLD, on
  - d. SERV REQ, off
2. Set data byte BAC HIGH (at address desired) in BUS OUT switches. Set correct parity as desired.
3. Set SERV OUT (raise Service Out and transfer BUS OUT to BAC HIGH)
  - a. SERV OUT, on
  - b. SERV IN, off
  - c. LOAD CTR - 01, on
  - d. SERV REQ, on
  - e. EVEN COUNT, on
4. Set SERV IN (drop Service Out)
  - a. SERV OUT, off
  - b. SERV IN, on
  - c. WORD HOLD, off
  - d. SERV REQ, off

5. Set data byte BAC LOW (at address desired) in BUS OUT switches. Set correct parity as required.
  6. Set SERV OUT (raise Service Out and transfer BUS OUT to BAC LOW).
    - a. SERV OUT, on
    - b. SERV IN, off
    - c. DEV END, on
    - d. CHAN END, on
    - e. IRPT, on
    - f. CNSL SEL, off
    - g. BAC address appears at buffer address counter position when Register Indicator knob is set at 5.
  7. Set STA IN (drop Service Out)
    - a. SERV OUT, off
    - b. COMMAND REGISTER, clear
    - c. SET BAC & STOP, off
    - d. STA IN, on
    - e. Bus In register (0 1 0000 1100)
  8. Proceed to ending sequence.
7. Set SERV IN (drop Service Out)
    - a. SERV OUT, off
    - b. SERV IN, on
    - c. WORD HOLD, on
    - d. SERV REQ, off
  8. Set byte (0 1 0000 0000) in BUS OUT switches.
  9. Set CMND OUT (raise Command Out and step BAC back one)
    - a. CMND OUT, on
    - b. WORD HOLD, off
    - c. DEV END, on
    - d. CH END, on
    - e. IRPT, on
    - f. CNSL SEL, off
    - g. SERV IN, off
  10. Set STA IN (drops Command Out)
    - a. CMND OUT, off
    - b. STA IN, on
    - c. WRITE, off
    - d. COMMAND REGISTER, clear
    - e. (0 1 0000 1100) appears in Bus In register when Register Indicator knob is set at position 1.
  11. Proceed to Ending Sequence (paragraph 2.6.1.7).

#### 2.6.1.4 Write Buffer

When a Write Buffer command is given, the initial selection sequence is followed by service cycles, with the number of data transfers from the channel to the display unit determined by the channel.

Service cycles for the Write Buffer command are simulated by performing the following procedure (Write Buffer command is transferred in the initial selection sequence):

1. Set SERV IN (drop Service Out)
  - a. SERV OUT, off
  - b. SERV IN, on
  - c. WORD HOLD, on
  - d. SERV REQ, off
2. Set data byte, 2A (0 0 0010 1010), in BUS OUT switches.
3. Set SERV OUT (raise Service Out and transfer BUS OUT to register B)
  - a. SERV OUT, on.
  - b. SERV IN, off
  - c. SERV REQ, on
4. Set SERV IN (drop Service Out)
  - a. SERV OUT, off
  - b. SERV IN, on
  - c. WORD HOLD, on
  - d. SERV REQ, off
5. Set data byte, 82 (0 1 1000 0010), in BUS OUT switches.
6. Set SERV OUT (raise Service Out and transfer BUS OUT to register B)
  - a. SERV OUT, on
  - b. SERV IN, off
  - c. SERV REQ, on

#### 2.6.1.5 Read Buffer

When a Read Buffer command is given, the initial selection sequence is followed by service cycles, with the number of data transfers from the display unit to the channel determined by the latter.

Service cycles for the Read Buffer command are simulated by performing the following procedure (Read Buffer command is transferred in the initial selection sequence):

1. Set SERV IN (drop Service Out and transfer register B to BUS IN)
  - a. SERV OUT, off
  - b. SERV REQ, off
  - c. WORD HOLD, on
  - d. Read address zero appears on the Bus In register when Register Indicator knob is set at position 1.
  - e. SERV IN, on
2. Set SERV OUT (raise Service Out)
  - a. SERV OUT, on
  - b. SERV IN, off
  - c. SERV REQ, on
3. Set SERV IN (drop Service Out and transfer register B to BUS IN)
  - a. SERV OUT, off
  - b. SERV IN, on
  - c. SERV REQ, off
  - d. WORD HOLD, on
  - e. Read address 1 appears on Bus In register.

NOTE: The channel continues to read the buffer until the word count equals zero (step 4).

4. Set (0 1 0000 0000) on BUS OUT switches.
5. Set CMND OUT (raise Command Out which steps the BAC back one)
  - a. CMND OUT, on
  - b. WORD HOLD, off
  - c. DEV END, on
  - d. CH END, on
  - e. IRPT, on
  - f. CNSL SEL, off
  - g. SERV IN, off
6. Set STA IN (drop Command Out)
  - a. CMND OUT, off
  - b. STA IN, on
  - c. READ BFR, off
  - d. COMMAND REGISTER, clear
  - e. (100001100) appears on Bus In register.
7. Proceed to Ending Sequence.

#### 2.6.1.6 Sense

When a Sense command is given, the initial selection sequence is followed by service cycles, with the number of transfers to the channel determined by the display unit.

The service cycles for the Sense command are simulated by performing the following procedure:

1. Set SERV IN (drop Service Out)
  - a. SERV OUT, off
  - b. SERV IN, on
  - c. WORD HOLD, on
  - d. SERV REQ, on
  - e. Sense byte 0 on BUS IN
  - f. REQ IN, off
  - g. ADPT REQ, off
2. Set SERV OUT (raise Service Out)
  - a. SERV OUT, on
  - b. LOAD CTR contains 01
  - c. SERV IN, off
  - d. SERV REQ, on
  - e. REQ IN, ADPT REQ, on
3. Set SERV IN (drop Service Out)
  - a. SERV OUT, off
  - b. SERV IN, on
  - c. SERV REQ, off
  - d. Sense byte 1 on BUS IN.
4. Set SERV OUT (raise Service Out)
  - a. SERV OUT, on
  - b. LOAD CTR contains 10
  - c. SERV IN, off
  - d. SERV REQ, on
5. Set SERV IN (drop Service Out)
  - a. SERV OUT, off
  - b. SERV IN, on

- c. SERV REQ, off
  - d. BAC High bits on BUS IN.
6. Set SERV OUT (raise Service Out)
  - a. SERV OUT, on
  - b. LOAD CTR contains 11
  - c. SERV IN, off
  - d. SERV REQ, on
7. Set SERV IN (drop Service Out)
  - a. SERV OUT, off
  - b. SERV IN, on
  - c. SERV REQ, off
  - d. WORD HOLD, off
  - e. BAC Low bits on BUS IN
8. Set SERV OUT (raise Service Out)
  - a. SERV OUT, on
  - b. SERV IN, on
  - c. CNSL SEL, off
  - d. DEV END, on
  - e. CH END, on
  - f. IRPT, on
9. Set STA IN (drop Service Out)
  - a. SERV OUT, off
  - b. COMMAND REGISTER, clear
  - c. BASIC SEN, off
  - d. STA IN, on
  - e. Bus In register contains (0 1 0000 1100)
10. Proceed to Ending Sequence.

#### 2.6.1.7 Ending Sequence

The interface ending sequence is performed as follows:

1. Set SERV OUT (raise Service Out)
  - a. SERV OUT, on
  - b. DEV END, off
  - c. CH END, off
  - d. IRPT, off
  - e. STA IN, off
  - f. BUSY, off
2. Set SERV OUT switch to lower position (drop Service Out)  
SERV OUT, off
3. Set SEL OUT and HOLD OUT switches to lower position (drop Select Out and Hold Out)
  - a. SEL OUT, off
  - b. HOLD OUT, off
  - c. OP IN, off

After the interface ending sequence is performed, the interface allows the channel to start the initial selection sequence for a new command.

#### 2.6.1.8 Initial Selection with Bad Parity

This routine describes a simulated initial selection in which bad parity is placed on the BUS OUT.

1. Set BUS OUT switches to correspond with Unit Address. Set good parity.
2. Set ADR OUT (raise Address Out)
  - a. ADR OUT, on
  - b. CH REQ, on
3. Set HOLD OUT (raise Hold Out). HOLD OUT, on.
4. Set SEL OUT (raise Select Out)
  - a. SEL OUT, on
  - b. OP IN, on
5. Set ADR IN (drop Address Out)
  - a. ADR OUT, off
  - b. ADR IN, on
  - c. Unit Address on BUS IN (Indicator Selector knob set at position 1).
6. Set Basic Sense command on the BUS OUT switches with bad parity (0 1 0000 0100).
7. Set CMND OUT (raise Command Out)
  - a. CMND OUT, on
  - b. COMMAND REGISTER, clear
  - c. UNIT CHK, on
  - d. BUS OUT CHECK (Sense Byte Zero), on

- b. REQ IN, off
- c. ADR IN, off
4. Set STA IN (drop Command Out)
  - a. CMND OUT, off
  - b. STA IN, on
  - c. Status byte on BUS IN (0 0 0000 0010)
  - d. STATUS BYTE - UNIT CHK, on
  - e. REQ IN, off
- B. Ending Sequence
  1. Set SERV OUT (raise Service Out)
    - a. IRPT, off
    - b. BUSY, off
    - c. UNIT CHK, off
    - d. STA IN, off
    - e. SERV OUT, on
  2. Set SERV OUT, HOLD OUT, and SEL OUT switches to lower position.
    - a. SERV OUT, off
    - b. HOLD OUT, off
    - c. SEL OUT, off
    - d. OP IN, off

NOTE: Sense Byte Zero is reset when Command Out drops if command other than Sense, Test I/O, or No Op was given.

#### 2.6.2 Display Generation

Manual programming is accomplished by loading consecutive addresses of the buffer with a sequence of order and data codes. Thus, test displays containing vectors, points, or characters (or combinations of these) can be obtained.

To be able to go from one type of display to another in a continuation of the manual buffer load, the SM code is entered at an even address, an MC code is entered in the next address, and data bytes corresponding to the MC code are entered in succeeding addresses. After the entire program has been entered, the display will appear on the screen when the REGENERATE-CONT switch is placed in the upper position.

A specific display is generated in five sequential steps:

- e. CH REQ, on
  8. Set STA IN (drop Command Out)
    - a. CMND OUT, off
    - b. STA IN, on
    - c. If status byte on BUS IN is not zero, UNIT CHECK indicator comes on (status byte on BUS IN, 000 000 010).
  9. Set CMND OUT (raise Command Out)
    - a. BUSY, on
    - b. STA STKD, on
    - c. IRPT, on
  10. Set HOLD OUT, SEL OUT, and CMND OUT switches to lower position.
    - a. HOLD OUT, off
    - b. SEL OUT, off
    - c. OP IN, off
    - d. CMND OUT, off
    - e. REQ IN, on (if Suppress Out is up, Request In will not go on and polling should not work)
- A. Polling
1. Set HOLD OUT (raise Hold Out). HOLD OUT, on,
  2. Set SEL OUT (raise Select out)
    - a. SEL OUT, on
    - b. OP IN, on
    - c. ADR IN, on
    - d. Unit Address on BUS IN
  3. Set CMND OUT (raise Command Out)
    - a. CMND OUT, on

1. Prepare display unit for manual buffer loading.
  - a. Place the unit off-line as described in paragraph 1.1.4.
  - b. Set LOAD SELECT rotary switch to BUFFER position.
  - c. Depress MACHINE RESET switch.
2. Enter SM Code (2A HEX).
  - a. Check that BAC is at an even count by rotating Register Indicator to position 5, BAC indicators. Bit 7 of BAC should be a 0, indicating an even address; if BAC bit 7 is a 1, depress LOAD SELECT/ENTER pushbutton once.
  - b. Place BUS OUT switches 2, 4, and 6 in upper position.

- c. Depress LOAD SELECT/ENTER pushbutton.
  - d. Set Start Regeneration Timer code (82 HEX) at BUS OUT switches, and depress LOAD SELECT/ENTER pushbutton. The Start Regeneration Timer code is entered only once in the program, following the first SM code.
3. Referring to Figure 1-2, enter desired MC code.
  4. Determine configuration of data bytes in accordance with display unit mode (Graphic, Character, or Transfer) set by the MC code. Enter data in accordance with the procedure for a particular mode, as follows:
    - a. Graphic mode (blanked vector, unblanked vector, or point). In this mode, four data bytes are required to complete each beam deflection. Complete each byte at the BUS OUT switches, and store each byte by depressing the LOAD SELECT/ENTER pushbutton. If beam deflection is to be blanked, bit 1 of the first byte should be a 1.
    - b. Character mode. Before entering character codes, place beam at desired screen location for first character by entering Graphic mode (blanked vector) and the four data bytes required for beam deflection. Proceed as follows:
      - (1) Enter SM code (even address).
      - (2) Enter MC code (size A protected, size B protected, size A unprotected, size B unprotected).
      - (3) Place A character code (0 11000001) at BUS OUT switches.
      - (4) Place CURSR INS switch in upper position.
      - (5) Depress LOAD SELECT/ENTER pushbutton.
      - (6) Place CURSR INS switch in lower position.
      - (7) Depress LOAD SELECT/ENTER pushbutton 20 or more times.
      - (8) Check that BAC is at an even count. When regeneration starts, the following conditions should prevail for this character display: (1) the A character should appear as many times as it has been entered; (2) the cursor should appear under the first A character (see steps 4 and 5); (3) if unprotected Character mode was entered with the MC code, the A characters can be replaced with different characters entered at the A/N keyboard, and nulls can also be entered; (4) the cursor can be advanced, backspaced, or jumped.
- c. Transfer mode. This mode allows BAC to return to buffer address 0 after entering a succession of order and data codes. To enter this mode, proceed as follows:
    - (1) Determine that BAC is at an even count.
    - (2) Enter SM code.
    - (3) Place BUS OUT switches 0 through 7 and P in upper position. (This sets the transfer code.)
    - (4) Depress LOAD SELECT/ENTER pushbutton.
    - (5) Place BUS OUT switches 0 through 7 in lower position.
    - (6) Depress LOAD SELECT/ENTER pushbutton twice. As the BUS OUT switches are in the lower position, BAC high-order and low-order bits (all 0's) are respectively entered with the two depressions of the ENTER pushbutton.
5. Start regeneration by placing REGENERATE-CONT switch in upper position. The programmed display should appear on the screen.

## 2.7 MARGINAL CHECKING

Marginal checking is performed by varying the output of the +6v power supply. This is accomplished by attaching an external marginal check (MC) power supply (PN 5712439) to the +6v supply in a manner that allows the MC supply to control the output of the +6v supply,  $\pm 1/2v$ . A jack is provided on the +6vdc power supply for insertion of the output lead of the MC supply. When inserted, the output lead of the MC supply interrupts the +6v supply output sensing circuit that normally monitors the supply output and controls the regulating circuit. In this manner, the output of the MC supply influences the +6v sense circuit and, by a control on the MC supply, is able to control the output of the +6v supply through the supply's regulating circuit.

When the MC supply output is decreased by means of the MC potentiometer, the +6v supply sensing circuit senses the change as an output variation and causes the +6v supply to increase its output. Conversely, the +6v supply is caused to decrease its output when the output of the MC supply is increased. The variation of the +6v supply output is reflected in circuits that use +6v and will affect circuit operation and increase the tendency of a weak component to fail.

Excursions (voltage variations) beyond circuit tolerances may cause sound (nonfailing) circuits to fail, with confusing and misleading symptoms.

It is therefore suggested that analysis be as thorough as possible prior to marginal checking and that excursion be effected slowly; i. e., vary the MC potentiometer a little at a time, waiting after each variation to determine whether excursion is producing the desired effects. It is further suggested that an accurate dc voltmeter be connected to the +6v at TB1 on 01B to measure the amount of excursion and to ensure that circuit tolerances

are not exceeded.

Marginal checking may be performed in conjunction with other diagnostic techniques (vibration, etc.) and with diagnostic or other programs.

Excursion of the +6v marginal check voltage beyond normal circuit tolerance will cause the analog diagnostic displays to be slightly distorted. This condition is normal and should not be considered a failure.



## CHAPTER 3. PREVENTIVE MAINTENANCE

This chapter is provided as an aid to performance of preventive maintenance on the 2250-1.

The Preventive Maintenance Chart (Figure 3-1) lists the components of the 2250-1 that require periodic attention, the frequency with which they require it, and the specific checks. Also included are references to the applicable servicing procedures.

Unit	Frequency	Action	Reference
Circuits	1 month	Check deflection interlock. Check Light Pen Detect trigger.	None Par. 4.2.8
Power	4 months	Monitor voltage.	Par. 5.5
D/A	4 weeks	Check D/A alignment and deflection (including alignment for standard- and extra-size characters).	Par. 4.2.2
CRT	12 months	Replace and align CRT*.	Par. 4.1 (replacement) Par. 4.2.2 (alignment)
Single-Shots	12 months	Check single-shot timings.	Par. 4.3
Diagnostics	6 months	Run Diagnostics program.	None
Blowers and Filters	6 months	Check blowers and filters.	Paragraph 4.11, 4.12, 4.13
Connectors	6 months	Check connections.	None

\*Frequency of CRT replacement is an approximate period based on the amount of serviceability expected. CRT's are to be replaced as needed.

Figure 3-1. Preventive Maintenance Chart

## 4.1 CRT REMOVAL/REPLACEMENT PROCEDURES

**DANGER**

Protective equipment must be worn by persons working with, or in the area of, an exposed CRT. All persons not wearing protective equipment must be vacated from the vicinity of the exposed CRT. The Safety section in the front of this manual must be read before the removal/replacement procedure is begun, and the safety rules contained therein must be complied with.

When it is necessary to replace the CRT, proceed as follows:

1. Turn power off, and wait for completion of sequencing-down operation.
2. Open wing gates of frame 01, and remove protective cover from high-voltage lead connection, if used.
3. Disconnect high-voltage lead from CRT.
4. Clip a grounding strap from the high-voltage male connector (located on the cowling) to ground.
5. Remove CRT tube socket.
6. Remove magnetic shield from neck of CRT.
7. Loosen yoke clamp.
8. Remove yoke assembly from CRT neck; set assembly on 01 frame.
9. Place protective CRT neck cap over CRT neck and under yoke clamp. Tighten yoke clamp.
10. Remove nut that secures green/yellow ground lead of CRT assembly.
11. Remove the four screws located underneath the shroud (two on right side and two on left side).
12. Disconnect ground strap from male high-voltage connector (connected during step 4).
13. Lift entire CRT housing from frame 01, and carry it from the office environment to a protected area for CRT removal.
14. Put on protective clothing, face mask, lead apron, and gloves.
15. Remove bezel by removing the two screws located under the faceplate and by pulling forward.
16. With a 10-inch screwdriver, loosen CRT strap located around faceplate.
17. Loosen yoke clamp, and remove protective CRT neck cap.
18. Slide CRT forward, and disconnect high-voltage lead from bell of CRT.
19. Remove magnetic shield from bell of CRT, and place CRT in box.
20. Place magnetic shield around new CRT. Ensure that cutout for high-voltage connector is in line with high-voltage socket on tube. Tape shield to tube when properly aligned.
21. Insert new CRT with shield, and connect high-voltage lead securely to bell of new tube.
22. Push CRT until it is fully seated in shroud.
23. Insert protective CRT neck sleeve under yoke clamp. Tighten clamp.
24. Place a rigid straightedge horizontally across front of housing and approximately halfway up vertical sides of housing. The face of the CRT should be  $3/8$  inch  $\pm$   $1/16$  inch back from the straightedge.
25. Use a retrieving tool to grasp a dental mirror. Then, with a flashlight, observe that aquadag ground contact is aligned with cut-out in shield.
26. Tighten strap around front of tube (faceplate), making certain that the rubber pads are under the strap at the top corners of the CRT.
27. Install bezel.
28. Remove protective clothing.
29. Carry assembly to display unit, and position it in 01 frame.
30. Install four holding screws.
31. Connect CRT assembly ground wire.
32. Remove protective cover from neck, and install yoke assembly as far forward as possible.
33. Replace CRT socket.
34. Replace high-voltage lead.
35. Replace high-voltage lead protective cover, if used.
36. Turn power on, and wait for power-up sequencing.
37. From the aux panel, address and start regenerating section of buffer that contains alignment pattern. If alignment program is not in buffer, it will be necessary to go on-line to load the buffer. After loading, return to off-line operation.
38. Adjust X and Y centering controls together for orientation and location of positioning yoke until full-size square is centered and has no neck shadow. Tighten yoke clamp.

**DANGER**

Do not touch high-voltage connection on tube.

39. Turn power off, and wait for completion of power-down sequence.
40. Remove CRT tube socket, and replace magnetic shield on CRT neck.
41. Replace CRT tube socket.
42. Close 01 frame.

The above procedure requires approximately one hour.

## 4.2 ANALOG ALIGNMENT PROCEDURES

The procedures for aligning the analog circuits follow in the order in which they should be performed. When only one area (e.g., character generator) is to be adjusted, the procedure can be entered at the appropriate point. When more than

one area is to be adjusted, the area that appears earliest in the procedure should be performed first. Adjustments should be made in conformity with the image specifications given in paragraph 4.2.1.

Several single-shots and delay lines significantly affect analog presentation. Their function, location, and initial settings are given in Figure 4-1. The single-shot and delay lines associated with the analog area to be adjusted should be checked before beginning the adjustment.

NOTE: For general analog alignment, disable the absolute vector graphic feature; otherwise, on some single-shot adjustments, no output will be seen.

Control	Function	Location	Logic Page	Initial Setting Before Optimizing
Character Preintensify	Allows unblank transition to settle before character deflection occurs.	02B B3H2D13 02B B3H2B02	ST031 ST031	20ns delay 20ns delay
Character Deintensify	Allows blank transition to settle in coincidence with deflection settling time.	02B B3M3D13 Upper	ST031	125ns delay
Vector Preintensify	Allows unblank transition to settle before vector deflection begins.	02B B1K2D13 Middle	PP031	200ns
Point Plot	Controls the length of time during which the beam is intensified while in Point Plot mode.	02B B1E2D12 Upper	PP011	700ns
Character Position Overdrive	Controls the duration that overdrive current is applied to position yoke while in the Typewriter mode for character writing.	01B A3M6B02*	XR011	2.5usec
Position Change Time, Character Mode Standard Size	Controls the positioning time of the main deflection system while writing standard-size characters in the Typewriter mode.	02B B1F2B02*	PP011	2.75usec
Position Change Time, Character Mode Expanded Size	Controls the positioning time of the main deflection system while writing expanded-size characters in the Typewriter mode.	02B B1G2B02*	PP011	3.0usec
Minimum Positioning Time	Allows 7.25usec for all positioning times $\leq 32RU$ .	02B B1G6B02 Upper	PP011	7.25usec
		02B B1G7B02** Upper	PP021	7.25usec
De-skew	Controls the time that De-skew pulse is applied to analog prior to positive transition of TP6.	02B B1F2D02*	PP021	200ns
		02B B1E2D13 Middle	PP021	400ns

\*See Figure 4-6, Note 13.

\*\*This single-shot is present only if the graphic design feature is installed.

Figure 4-1. Analog Alignment Controls

#### 4.2.1 2250-1 CRT Image Specifications

The image specifications listed below should be used as criteria for image quality. Adjustments to the analog system should be made in conformity with these specifications:

1. Image size: 12 inches x 12 inches  $\pm 2.5\%$ .
2. Relative positional accuracy - The distance measured between the corresponding points on parallel vectors or lines should be within  $\pm 2.5\%$  or one spot size, whichever is greater, from line to line when the lines are within the center 6-inch square section of the display area. The like distance should be within  $\pm 6\%$  or one spot size, whichever is greater, from line to line when the lines are not within the center 6-inch square section of the display area. The above figures exclude irregularities as defined below.
3. Linearity - Excluding irregularities, no point on a line should be more than  $\pm 1.5\%$  of line length or 2 raster units (RU), whichever is greater, from a straight line between end points.
4. Smoothness - Excluding irregularities, images produced should not show gaps or overlapping of lines exceeding 4 RU.
5. Irregularity - The maximum irregularities, when crossing various points of the CRT, are as follows: Center of CRT < 4 RU  
 $1/4$  and  $3/4$  points < 3 RU
6. Analog position changes should be completed in a period  $\leq 7.25\text{usec} + 92 \times \frac{N-16}{1007}$   
where T = time in usec  
N = raster units of deflection
7. Repositioning accuracy - Using pattern 3 of program F756 or F766 and the timing relationship indicated in step 6, observe that the gap between any pair of corresponding points on the display should be  $\leq 1$  spot size.
8. Resolution - Point plots located in 4 RU centers should be discernible.

#### 4.2.2 Alignment

Alignment adjustments should be made in accordance with the image specifications given in paragraph 4.2.1. When complete analog alignment is necessary, proceed as follows:

##### CAUTION

If power is on, do not, under any circumstances, remove an analog card.

1. Display General Alignment Pattern (pattern 1 of program F756 or F766). (See Figure

4-2.) Turn operator's dynamic character contrast and dynamic vector contrast controls fully counterclockwise. Brightness, dynamic vector contrast, and dynamic character contrast are the front, center, and rear control knobs, respectively, located on the operator's panel (right CRT housing support). Using a screwdriver, turn CE brightness-limiting potentiometer located at 01EA4 (recessed potentiometer near operator's brightness control) fully counterclockwise. Turn operator's brightness control fully clockwise. Next, adjust the CE brightness-limiting potentiometer so that point plots, end points, and short length vectors are just adequately visible. If this results in nonuniform intensity on characters and lines, the display may be optimized by adjusting appropriate operator's dynamic control. For more detailed information, refer to the Intensity Alignment Procedure, paragraph 4.16.

NOTE: Failure to observe this procedure may result in faulty light pen operation.

2. Check following voltages at points indicated:  
+36v at laminar bus in 01B  
-36v at laminar bus in 01B  
+6v at laminar bus in 01B  
+3v at laminar bus in 01B  
-3v at laminar bus in 01B  
+80v at 01C/TB1-A6  
+450v at 01C/TB3-B10
3. The adjustments for card-mounted potentiometers in 01BA2, indicated in a through d of this step, are performed only at locations where a card replacement has been made or a possible maladjustment is suspected. Because these adjustments are made with the gate open, drift can occur as a normal consequence of temperature change after the gate is closed. This drift should not be a matter of concern, since provision has been made for it in the adjustment.
  - a. At A2J6, A2J7 (DC Intensity Adjustment), adjust card-mounted potentiometer until -30v level, as measured by scope probe at 01BA2J6B04, begins to go positive. Back off until -30v level is solid, and rotate potentiometer two additional full turns.
  - b. At L06, L07 (Vector Dynamic Intensity Adjustment), place voltmeter leads between +36v bus and pin L06D07 (positive terminal of voltmeter is connected to +36v bus). Adjust card-mounted potentiometer for 0.5v reading while power is on, but with machine reset.

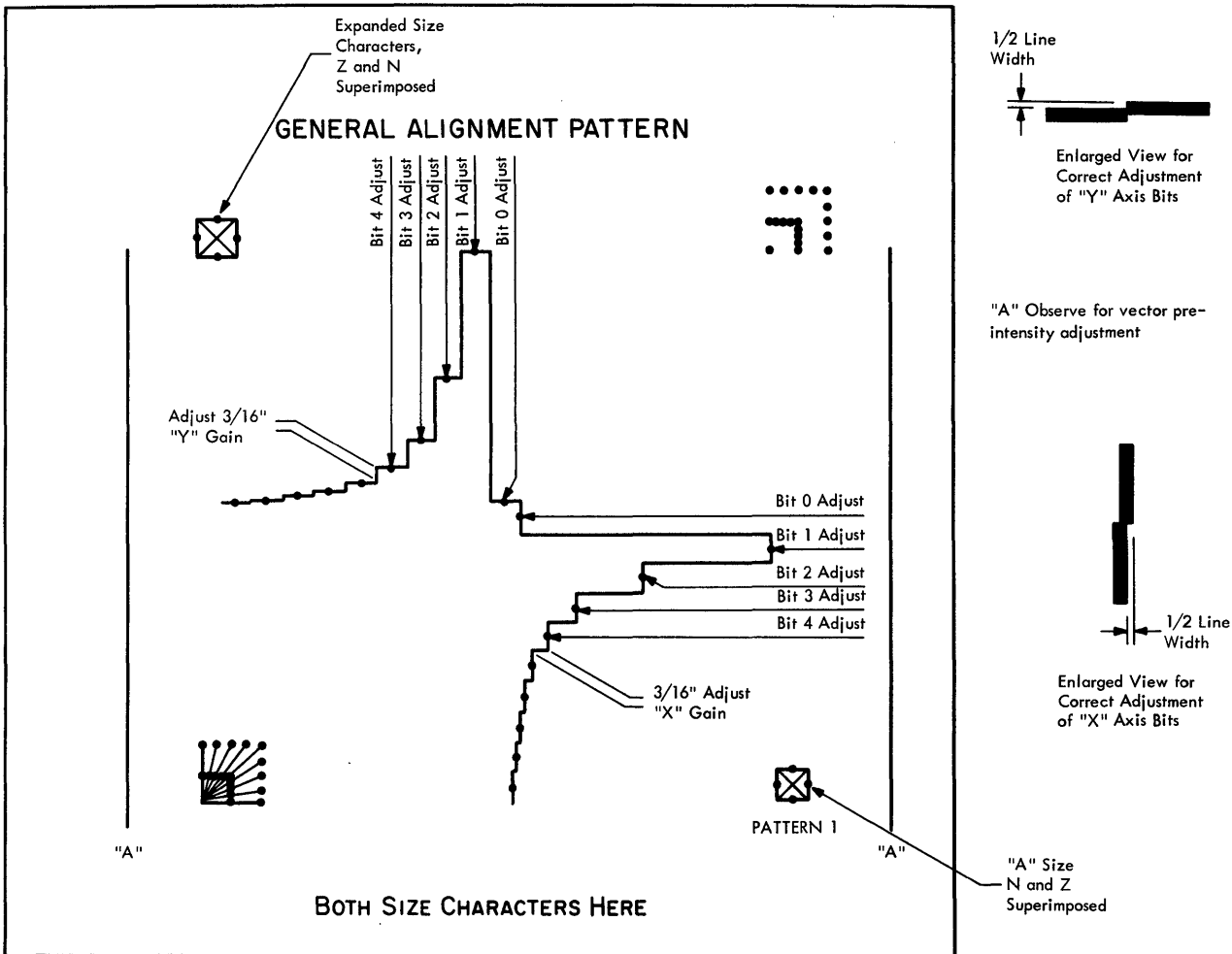


Figure 4-2. General Alignment Pattern

- c. At H02, H03 (Character Dynamic Intensity Adjustment), place voltmeter leads between +36v bus and pin H02D07 (connect positive terminal of voltmeter to +36v bus). With power on, but with machine reset, adjust card-mounted potentiometer for 0.5v reading.
- d. Before proceeding to the potentiometer panel adjustments below, be sure to close the gate cover.
4. Place all potentiometers (except LP GAIN) on potentiometer panels (01B-A1A1 and 01B-A1B2) in mid-range. Set LP GAIN potentiometer fully clockwise.
5. Adjust X and Y centering controls until full-size square is visually centered within display area.
6. Adjust brightness potentiometer (operator control) for comfortable intensity level.
7. Scope points listed below, and adjust the four DC OFFSET potentiometers until signals generated by General Alignment Pattern all return to same dc base line of  $+33v \pm 1v$  with minimum base line variation.
 

X DC OFFSET	Scope 01B-A2L7B09
X' DC OFFSET	Scope 01B-A2L7B10
Y DC OFFSET	Scope 01B-A2L6B02
Y' DC OFFSET	Scope 01B-A2L6B03
8. Adjust X GAIN control so that bits 5-9 in X on General Alignment Pattern measure 3/16 inch (Figure 4-2).
9. Adjust BIT 4 in X until bit 4 exceeds (to the right) bits 5-9 by 1/2 spot size.
10. Adjust BIT 3 in X until bit 3 exceeds bits 4-9 by 1/2 spot size.
11. Adjust BIT 2 in X until bit 2 exceeds bits 3-9 by 1/2 spot size.

12. Adjust BIT 1 in X until bit 1 exceeds bits 2-9 by 1/2 spot size.
13. Adjust BIT 0 in X until bit 0 exceeds bits 1-9 by 1/2 spot size.
14. Repeat procedure outlined in steps 8 through 12 for Y axis.
15. Adjust X and X' POSITION DAMPING potentiometers until vertical dots or point plots in General Alignment Pattern are collinear and intensity is not gapped. It may be necessary to readjust the DC OFFSET potentiometers (step 7).
16. Adjust Y and Y' POSITION DAMPING potentiometers until horizontal dots or point plots are collinear and intensity is not gapped. It may be necessary to readjust the DC OFFSET potentiometers (step 7).
17. Adjust vector preintensification single-shot (02B-B1K2 middle) until starting point of the two vertical vectors is intensified (Figure 4-2).
18. Observe small vectors in fan portion of Alignment Pattern, and make fine modification to X and Y POSITION DAMPING potentiometers until 0-degree, 45-degree, and 90-degree vectors in fan pattern are linear and point plots are collinear, with vector intensity not gapped.

#### 4.2.3 De-skew Adjustment

Use de-skew pattern (pattern 5 of program F756 or F766).

1. Adjust single-shot in 02B-B1F2D02 (Figure 4-6, note 13) so that trailing edge of negative pulse occurs 100ns prior to positive transition of TP6 at 02B-B1H6B09.
2. Adjust single-shot in position 02B-B1E2D13 (middle) to minimize irregularities on CRT. Maximum deviation should not exceed  $\pm 1.5$  spot size. Verify setting of this single-shot by observing pulse width at 02B-B1E2D13. This pulse width should not exceed 1usec.

#### 4.2.4 Asynchronous Adjustments (for Machines Without Absolute Vector Graphics)

Use dot repositioning pattern (pattern 3 of program F756 or F766).

1. Turn off power.
2. Remove asynchronous delay card (PN 5800825) located in 01BA2-G04, G05.
3. Adjust potentiometer resistance, as measured between G02 and J02, to zero. (Early versions of this card do not have a potentiometer; thus, this step does not apply to them.)

4. Insert a jumper (PN 811824) between the first and fourth program caps. Count from left, with card oriented so that program caps are at top.
5. Reinsert card.
6. Turn on power.
7. Display pattern.
8. Adjust ASYN DELAY potentiometer on potentiometer panel 01BA1 until gap between any pair of points addressed to same X, Y address  $\leq 1.0$  spot size.
9. To verify that the timing specification has not been exceeded, monitor input and output waveforms at 01BA2-G4B02 and 01BA2-G5B12, respectively. For any given deflection, the time T, measured from the instant the input waveform is 0.2v below the baseline to the time that the output waveform is at the 50% amplitude point of the positive transition, shall satisfy the following relation:

$$T \leq 7.25 \quad N < 16$$

$$T \leq 7.25 + 92 \frac{N-16}{1007} \quad N \geq 16$$

T = time in microseconds.

N = deflection in raster units. (In the case of deflections occurring simultaneously in the X and Y axes, use the value of N corresponding to the larger change.)

The values of N to be used for this pattern (pattern 3 of program F756 or F766) are:

$$N = 64d \text{ for } d = 1 \text{ through } 15,$$

$$N = 1023 \text{ for } d = 16,$$

where d corresponds to the first, second, etc. dot away from the origin (at the lower left), regardless of whether the dots are positioned horizontally, vertically, or diagonally.

10. If excessive time is being used for the small deflections (those in the range 16 to 32 raster units, for example) and the large deflections are within specification, relocate the jumper terminal inserted in the fourth program cap to a lower-numbered program cap. Conversely, move the jumper to the fifth program cap if slightly more time is desired for the small deflections.
11. Readjust ASYN DELAY potentiometer, if necessary.
12. At a certain point within the range 0 to 32 raster units, no output will be obtained at 01BA2G5B12. Timing control thereupon reverts to the single-shot located in 02BB1G6B02 upper.

#### 4.2.5 Character Generator Alignment

Use general alignment pattern (pattern 1 of program F756 or F766).

1. Set X and Y CHAR SIZE potentiometers to mid-range.
2. Adjust X and Y CHAR DAMPING potentiometers so that ends of character strokes are not dropped (particularly in vertical and horizontal strokes), while maintaining linearity in letters containing diagonal strokes.
3. Adjust X and Y CHAR SIZE potentiometers while viewing standard-size characters for 0.12 inch and 0.16 inch, respectively. Variation from these values (to suit user's preference) is permissible.
4. Adjust character contrast potentiometer while viewing an image containing characters, lines, or vectors, and point plot information for desired intensity level. Since the brightness control affects all visual modes, it may be adjusted in conjunction with character contrast. Do not set contrast too high or intensity distortion will occur.
5. Adjust time delays located in 02B-B3H2 until beginnings and ends of character strokes are uniformly unblanked. This may be seen by viewing characters such as A, N, or H.

#### 4.2.6 Character Overdrive Adjustment

Use general alignment pattern (pattern 1 of program F756 or F766). See note 13 of Figure 4-6 for the method of adjusting single-shots described in this procedure.

1. Scope and adjust following single-shots:
  - Standard size - 02B-B1F2B02 to 2.75usec.
  - Expanded size - 02B-B1G2B02 to 3.0usec.
2. Adjust 01BA3M6, while viewing a line of standard-size characters, until character distortion occurs.
3. Back off until characters are distortion-free.
4. Observe expanded-size characters, and adjust single-shot in 02B-B1G2B02 until character distortion occurs.
5. Back off until characters are distortion-free.

#### 4.2.7 Line or Vector Contrast

Use general alignment pattern (pattern 1 of program F756 or F766). Adjust line or vector contrast potentiometer while viewing an image or lines or vectors. The intensity should be equal to character

intensity. Do not set contrast too high or intensity distortion (blooming) will occur.

#### 4.2.8 Light Pen Gain

Use program F75B or F76B for this adjustment. If the proper intensity alignment procedure has been followed as specified in paragraph 4.2.2, step 1, correct light pen alignment and operation will be obtained if the operator's brightness control is set fully clockwise (maximum brightness).

NOTE: Do not operate the Light Pen Detect switch during alignment.

1. Place LP ALIGN switch (potentiometer panel) in ON position. This will affect targets as follows:
  - a. Distortion to a character.
  - b. A partial blanking of a vector near the pen.
  - c. A small unblanked vector will appear displaced down and to the left from a detected point.
2. If 2250-1 has graphic design feature, skip steps 3 through 5. There is no light pen adjustment when GDF is installed.
3. Place LP GAIN potentiometer in extreme clockwise position.
4. Adjust (counterclockwise) until it is possible to fire on characters without causing false returns on other portion of display.
5. When false returns are observed, back off slightly until they no longer occur.
6. Place LP ALIGN switch in OFF position.

#### 4.2.9 Absolute Vector Graphics Alignment

Proper alignment of the vector generator depends on proper alignment of the digital and analog circuits for the basic unit. Use absolute vector graphics alignment pattern (program F757 and F767, pattern 1) for this procedure. (See Figure 4-3.)

1. Measure voltage on pins 01AA2H2B08 to ground. This voltage is nominally +29vdc and can be varied between +28vdc and +32vdc with the reference voltage potentiometer on 01AA1 potentiometer panel. If adjustment cannot be made, proceed to paragraph 4.2.11, step 16.
2. Adjust X' DC OFFSET potentiometer on 01BA1 potentiometer panel until vertical lines to right of display center coincide with crosses displayed horizontally.
3. Adjust X DC OFFSET potentiometer on 01BA1 potentiometer panel until vertical lines to left

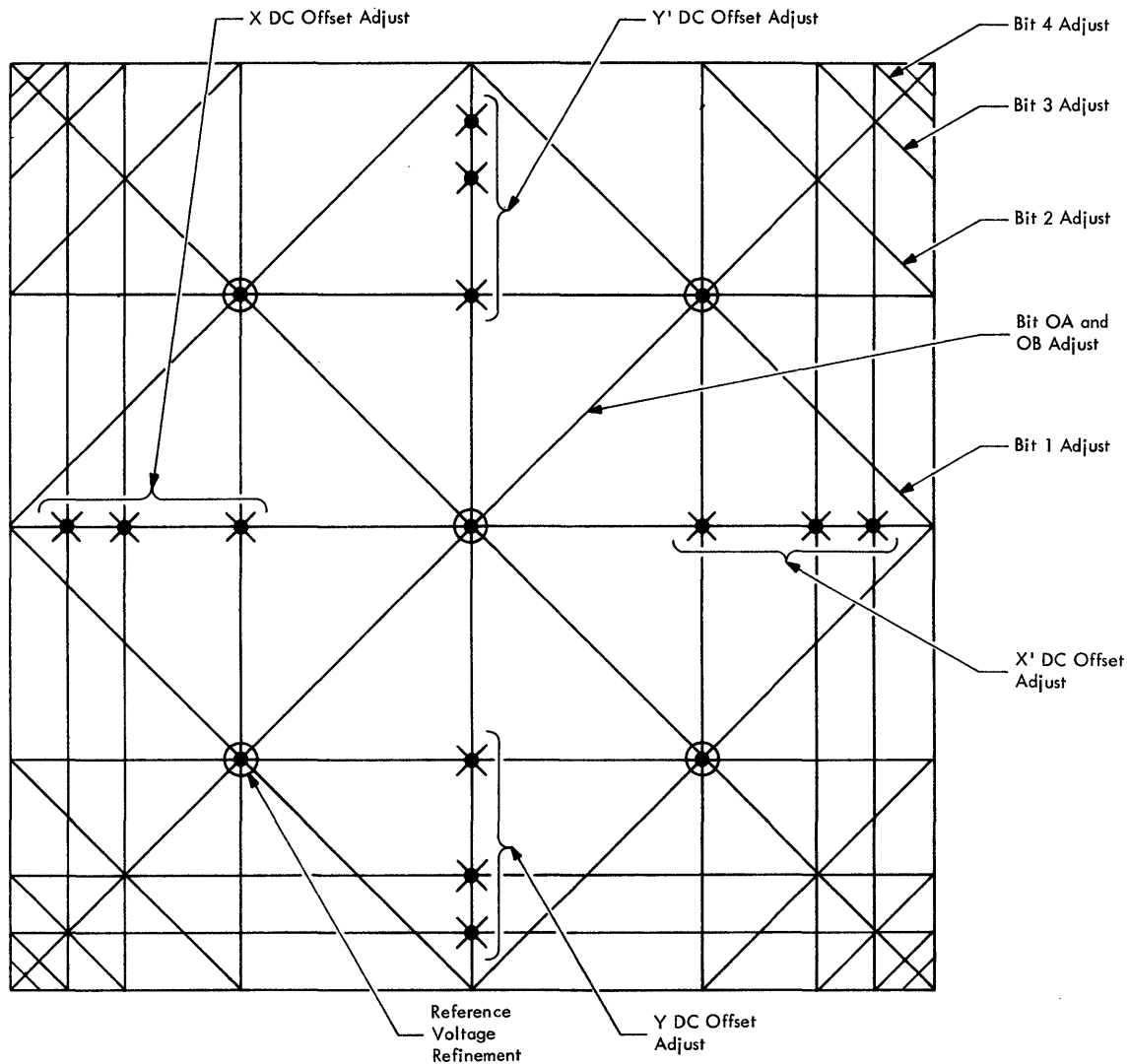


Figure 4-3. Absolute Vector Graphics Alignment Pattern

- of display center coincide with crosses displayed horizontally.
4. Adjust Y' DC OFFSET potentiometer on 01BA1 potentiometer panel until horizontal lines above display center coincide with crosses displayed vertically.
  5. Adjust Y DC OFFSET potentiometer on 01BA1 potentiometer panel until horizontal lines below display center coincide with crosses displayed vertically.
  6. Adjust BIT 4 potentiometer on 01AA1 potentiometer panel until second set of 45-degree double-traced lines from upper right-hand corner and corresponding lines at other three corners coincide and are linear.
  7. Adjust BIT 3 potentiometer on 01AA1 potentiometer panel until third set of 45-degree double-traced lines from upper right-hand corner and corresponding lines at other three corners coincide and are linear.
  8. Adjust BIT 2 potentiometer on 01AA1 potentiometer panel until fourth set of 45-degree double-traced lines from upper right-hand corner and corresponding lines at other three corners coincide and are linear.
  9. Adjust BIT 1 potentiometer on 01AA1 potentiometer panel until fifth set of 45-degree double-traced lines that form a diamond coincide and are linear.
  10. BIT 0 consists of two potentiometers on 01AA1 potentiometer panel labeled 0A and 0B. Set each to mid-range, and begin to adjust them for coincidence of diagonals of 12-inch x 12-inch display, attempting to maintain same setting on each potentiometer.
  11. Observe that lines crossing through display



center and at circled crossovers intersect within displayed point-plot circles. The intersection of these lines can be optimized by a slight adjustment of the reference voltage potentiometer on 01AA1 potentiometer panel. If it is necessary to readjust reference voltage, repeat steps 1 through 9.

#### 4.2.10 Asynchronous Adjustment (with Absolute Vector Graphics Feature)

1. Turn off power.
2. Remove asynchronous delay card (PN 5800825) located in 01BA2 - G04, G05.
3. Adjust resistance of the card-mounted potentiometer to 16K. Measure between G02 and J02, with the positive terminal of the ohmmeter at G02.
4. Insert jumper (PN 811824) between the first and fourth program caps. Count from left, with card oriented so that program caps are at top.
5. Reinsert card.
6. Turn on power.
7. Display repositioning pattern (pattern 3 of F756 or F766).
8. Adjust ASYN DELAY potentiometer on potentiometer panel 01BA1 until the separation between any pair of points addressed to the same X, Y address  $\leq 1.5$  spot size.
9. To verify that the timing specification has not been exceeded, monitor the input and output waveforms at 01BA2 - G4B02 and 01BA2 - G5B12, respectively. For any given deflection, the time T, measured from the instant the input waveform is 0.2v below the baseline to the time that the output waveform is at the 50% amplitude point of the positive transition, shall satisfy the following relation:

$$T \leq 6.75 \quad N < 16$$

$$T \leq 6.75 + 92 \left( \frac{N-16}{1007} \right) \quad 16 \leq N \leq 31$$

$$T \leq 6.75 + 92 \left( \frac{N^*-16}{1007} \right) \quad N \geq 32$$

T = time in microseconds

$N^* = 31 + 32n$

n = smallest integer satisfying the inequality

$$n \geq \frac{N-31}{32}$$

N = deflection in raster units

10. Under certain conditions, the setting of the ASYN DELAY potentiometer needed to satisfy the above timing relationships will be at or near one end of the potentiometer. In this case, make additional adjustment by varying the card-mounted potentiometer in

location 01BA2 - G04, G05 for additional resistance.

11. If excessive time is being used for the small deflections (e.g., those in the range from 16 to 32 raster units) and the large deflections are within specification, relocate jumper terminal inserted in the fourth program cap to a lower-numbered program cap. Conversely, move jumper to the fifth program cap if slightly more time is desired for the small deflections.
12. Readjust ASYN DELAY potentiometer, if necessary.

At a certain point within the range 0 to 32 raster units, no output will be obtained at 01BA2G5B12. Timing control thereupon reverts to the single-shot located in 02BB1G6B02 upper in machines without the graphic design feature and alternates between single-shots 02BB1G6B02 upper and 02BB1G7B02 upper when the graphic design feature is installed.

#### 4.2.11 Absolute Vector Generator Maintenance

Indication of malfunction of the vector generator can be determined by nonlinearity of vectors and the inability of vectors to meet end points. If a malfunction is observed, it must be analyzed to determine whether it is of a system, logic, analog, or interpretive origin.

The following procedure localizes the problem or malfunction to the vector graphics analog area, with the assumption that all digital inputs are present with nominal pulse widths and nominal time relationships. Faulty digital inputs to the Vector Graphics switches that are always in the On state have the same effect as shorted switches, whereas those that are always in the Off state have the same effect as open switches. This procedure isolates the problem whether the fault occurs in the switches or in the inputs to the switches.

1. Load buffer with general alignment pattern (pattern 1 of F766) and absolute vector graphics alignment pattern (pattern 1 of program F767).
2. Place unit off-line, set absolute vector graphics (AVG) feature switch to ENABLE, and display AVG alignment pattern (Figure 4-3).
3. If AVG pattern is not in alignment, display general alignment pattern. Align basic pattern as described in paragraph 4.2.1. If pattern can be aligned, proceed to step 8.
4. If basic pattern cannot be aligned, remove AVG switches from yoke:
  - a. Turn off power.
  - b. Disconnect cable, PN 5705460, from 01AA2N3.

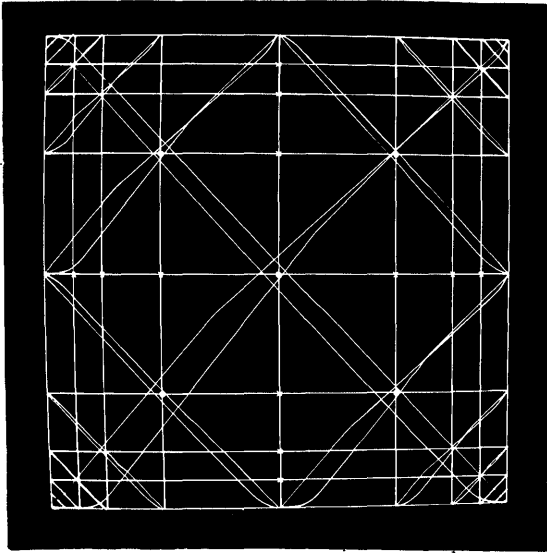
5. Turn on power and align basic pattern. (Refer to paragraph 4.2.1.) If pattern can be aligned, proceed to step 7.
6. If basic pattern cannot be aligned, refer to paragraph 1.4 to locate the trouble.
7. After the basic pattern has been aligned:
  - a. Turn off power.
  - b. Reinsert cable removed in step 4.
  - c. Turn on power.
  - d. Display AVG alignment pattern.
8. Realign AVG feature as described in paragraph 4.2.9.
9. If the AVG feature cannot be aligned, make a comparison between AVG alignment pattern (Figure 4-3) and photographs (Figure 4-4) to determine whether pattern indicates open or shorted switches.
  - a. Open switches. By observing the double-traced angular vectors, an open switch can be isolated. Horizontal and vertical vectors do not show the effects of open switches.
    - (1) Bit 4. An open switch in bit 4 affects all vectors in the pattern.
    - (2) Bit 3. An open switch in bit 3 affects all vectors that are equal in length to the Bit 3 Adjust and longer (i.e., bit 2 Adjust, etc.). The vectors labeled bit 4 are unaffected (Figure 4-3).
    - (3) Bit 2. An open switch in bit 2 affects all vectors that are equal in length to the Bit 2 Adjust vectors and longer. Shorter vectors such as Bit 3 Adjust and Bit 4 Adjust are unaffected.
    - (4) Bit 1 and Bit 0. Similar effects can be observed for open switches in bit 1 and bit 0.
  - b. Shorted switches. Shorted vector graphics switches cause every vector in the display to be distorted. All double-traced vectors can be observed as two distinct vectors, with the separation between them dependent upon the switch that is shorted. The degree of failure to meet the end points is also determined by the shorted switch. The crosses on the alignment pattern cannot be recognized as crosses.
10. If pattern (step 9) indicates no open or shorted switches, proceed to step 16. If faulty card cannot be determined (step 9), proceed to step 11. If malfunction can be isolated to a unique card:
  - a. Turn off power.
  - b. Replace faulty card.
  - c. Turn on power.
  - d. Display AVG alignment pattern.
  - e. Check and adjust alignment.

If alignment can be obtained, proceed to step 19. If not, proceed to step 16.

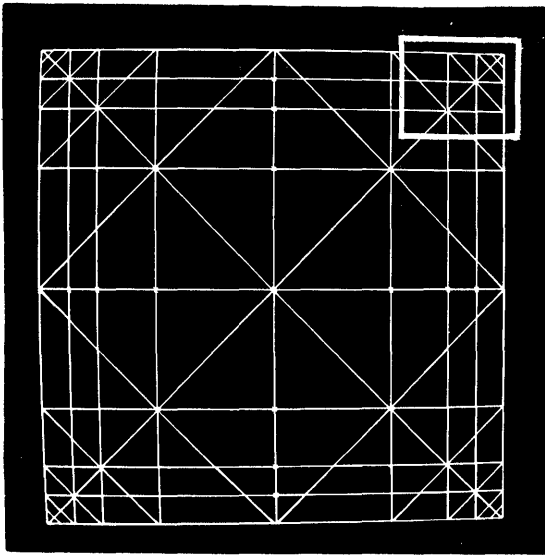
11. To determine faulty card indicated (step 9), proceed as follows:
  - a. Turn off power.
  - b. Remove cards from locations:
    - (1) 01AA2L4/L5 (1/2 bit 0)
    - (2) 01AA2M4/M5 (1/2 bit 0)
    - (3) 01AA2K4/K5 (bit 1)
  - c. Turn on power.
  - d. Display alignment pattern.

NOTE: Removal of the above three cards will cause the double-traced angular vectors (labeled Bit 0A and 0B) and Bit 1 Adjust and corresponding vectors in the other corners to appear as two nonlinear lines.

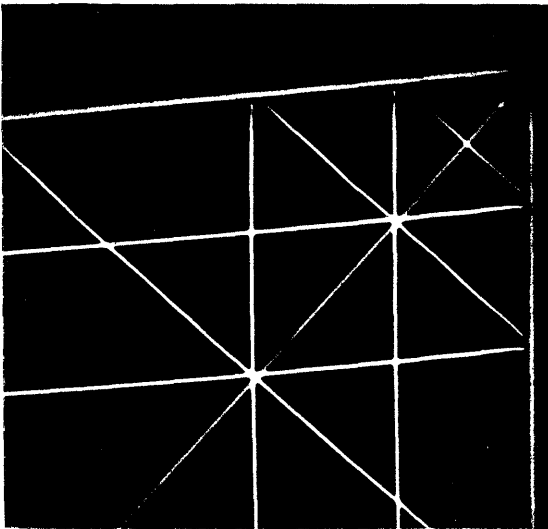
  - e. Check for linearity of vectors labeled Bit 4 Adjust, Bit 3 Adjust, and Bit 2 Adjust (Figure 4-3). If these vectors are linear, problem has been isolated to one or more of the three identical cards removed. If vectors are not linear, proceed to step 13.
12. To determine faulty card indicated (step 11e), proceed as follows:
  - a. Turn power off.
  - b. Reinsert in position 01AA2K4/K5 (bit 1 position) any one of the three removed cards.
  - c. Display AVG alignment pattern, and check for linearity of vectors labeled Bit 1 Adjust in Figure 4-2.
  - d. Repeat this process until malfunction has been isolated to one of the three cards.
  - e. If feature cannot be aligned, proceed to step 16.
13. If removal of the three cards does not satisfy step 11, malfunction exists in the three cards in positions 01AA2G4/G5 (bit 4), H4/H5 (bit 3) and J4/J5 (bit 2). Turn off power, and replace the cards removed in accordance with procedure 11.
14. Substitute a spare PN 5801684 card for that in 01AA2J4/J5. Apply power, and display AVG alignment pattern to determine whether the malfunction has been removed (by checking for linearity and coincidence of all vectors).
15. Turn off power, and repeat step 14, substituting spare card, PN 5801686, in location 01AA2H4/H5 (bit 3). If the malfunction is not removed, turn off power and repeat step 14, substituting spare card, PN 5801685, in location 01AA2G4/G5 (bit 4).
16. If proper alignment cannot be obtained, measure voltage from pins 01AA2H2 B08/B09



1. AVG Disabled

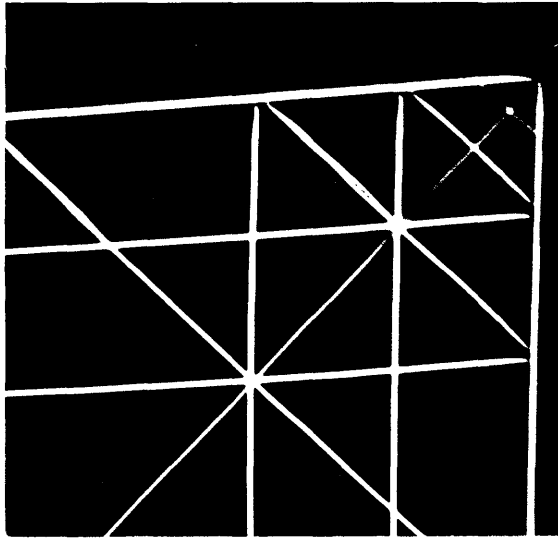


2. Unit in alignment. Section marked is shown expanded in 2a, 2b, 2c, and 2d.

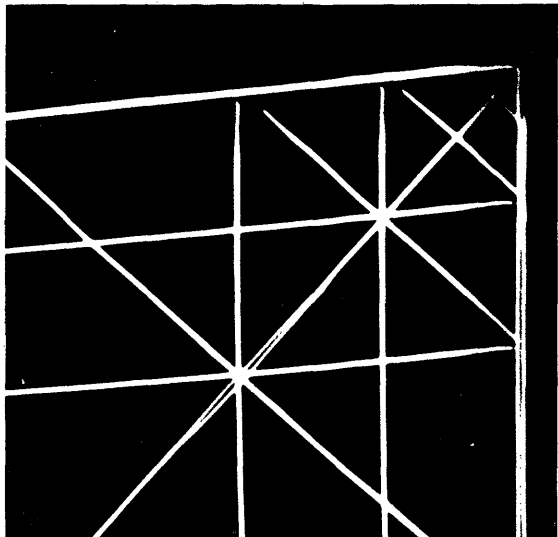


2a. Unit in alignment

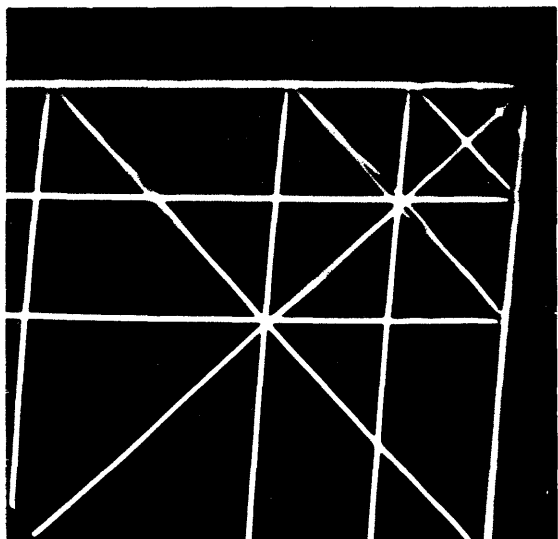
Figure 4-4. Absolute Vector Graphics Malfunctions (Sheet 1 of 7)



2b. Open switch in bit 4. Shorted switch similar to bit 3 short. Check 01AA2 G4/G5.

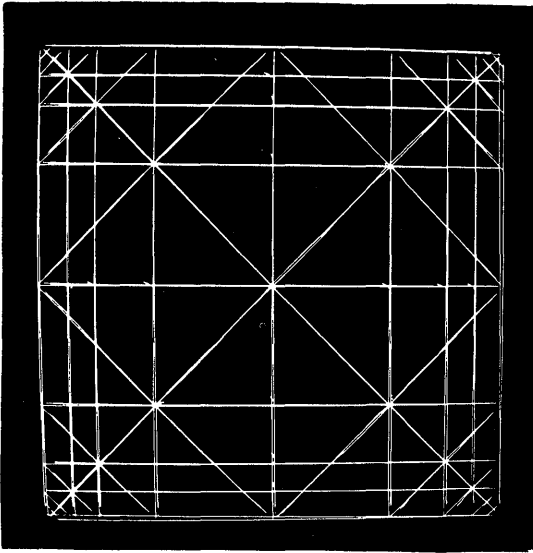


2c. Shorted switch in bit 3. Note crosses and failure to meet endpoints. Check 01AA2 H4/H5.

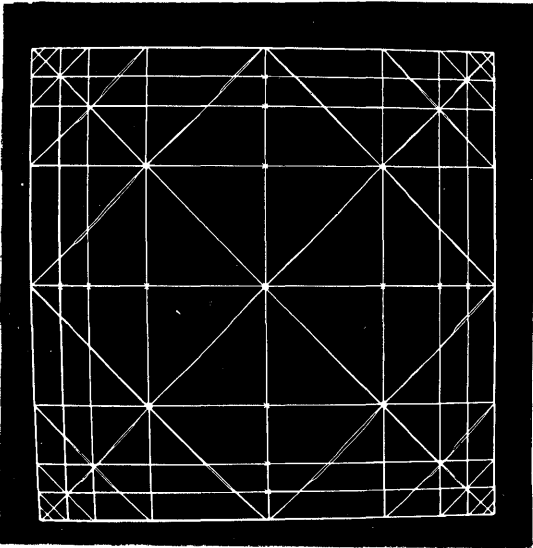


2d. Open switch in bit 3. Check 01AA2 H4/H5.

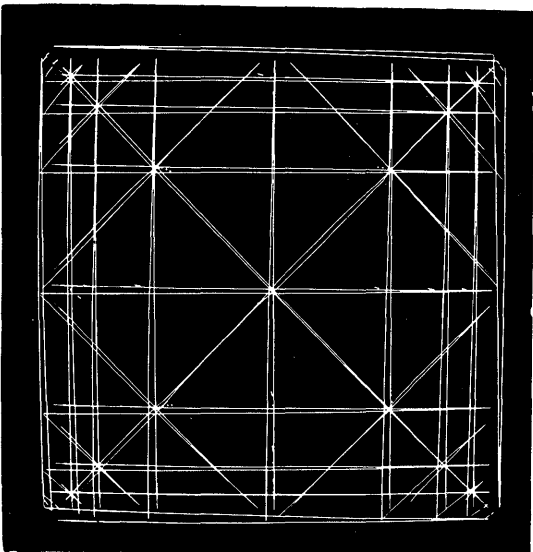
Figure 4-4. Absolute Vector Graphics Malfunctions (Sheet 2 of 7)



3. Shorted switch in bit 2. Note crosses. Check 01AA2 J4/J5.

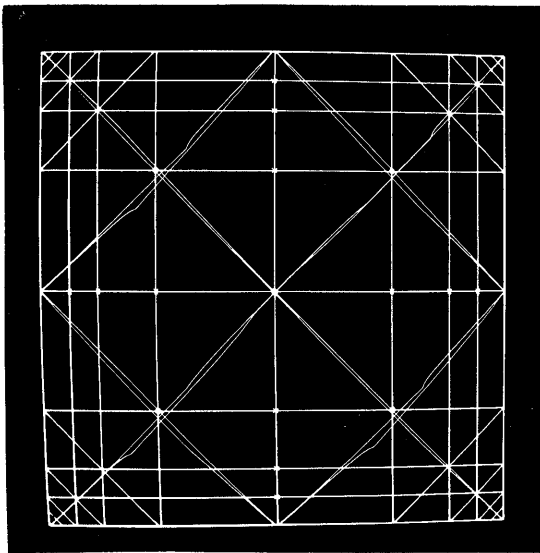


4. Open switch in bit 2. Check 01AA2 J4/J5.

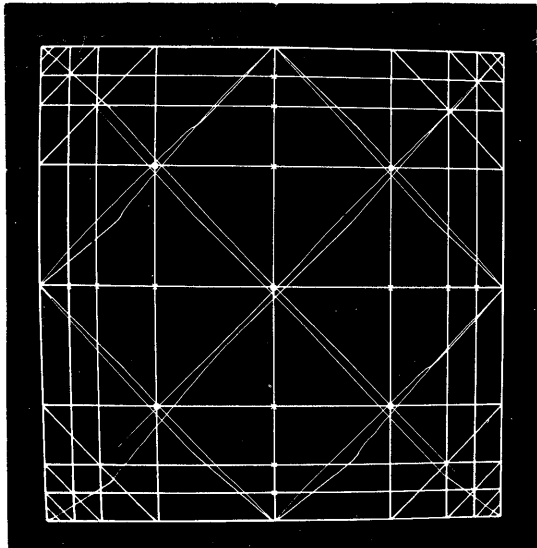


5. Shorted switch in bit 1. Check 01AA2 K4/K5.

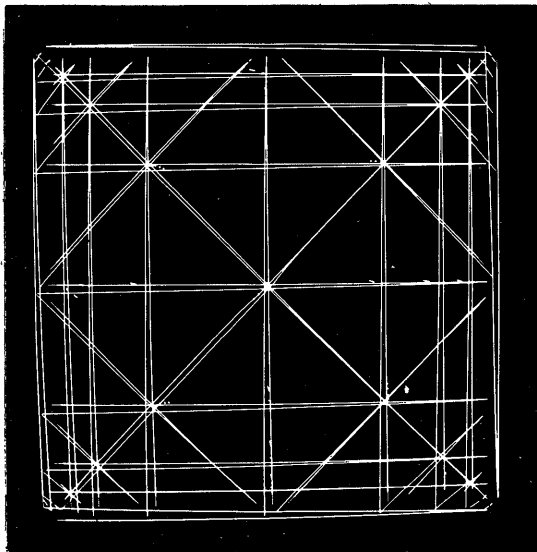
Figure 4-4. Absolute Vector Graphics Malfunctions (Sheet 3 of 7)



6. Open switch in bit 1. Check 01AA2 K4/K5.

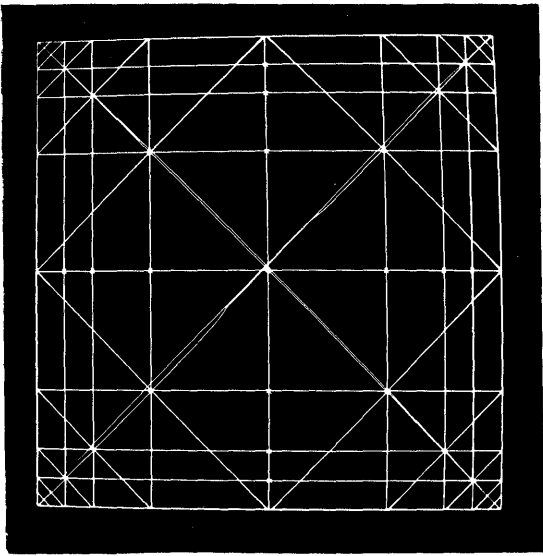


7. Both switches open in bit 1. Check 01AA2 K4/K5.

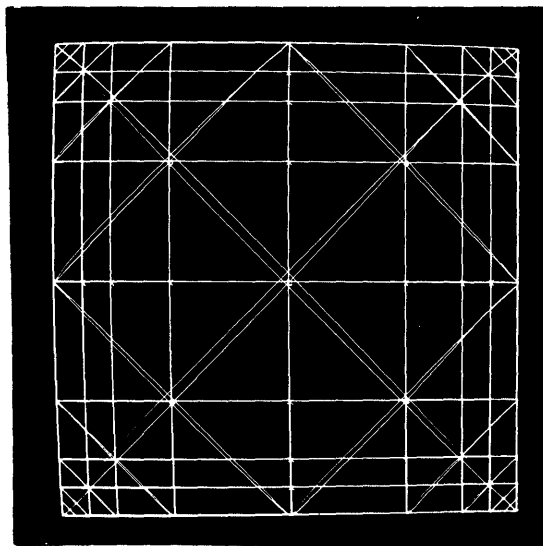


8. Shorted switch in 1/2 bit 0. Check 01AA2 M4/M5 or 01AA2 L4/L5.

Figure 4-4. Absolute Vector Graphics Malfunctions (Sheet 4 of 7)

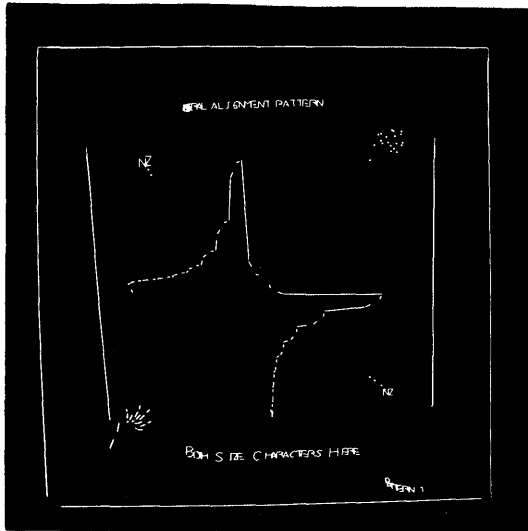


9. Open switch in 1/2 bit 0. Check 01AA2 M4/M5 or 01AA2 L4/L5.

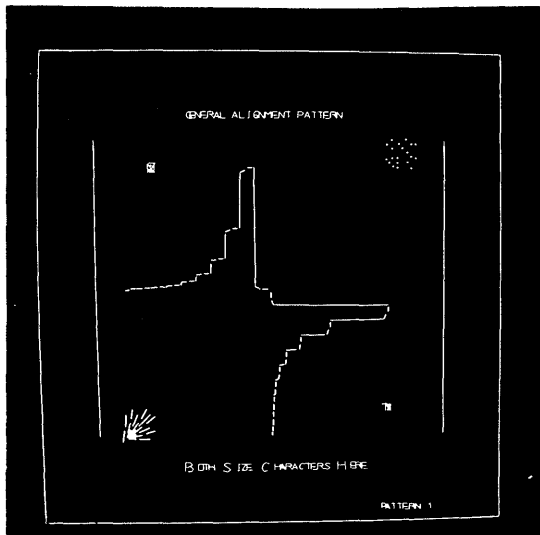


10. Open 042 transistor in ref. voltage supply. Check 01AA2 H2/H3.

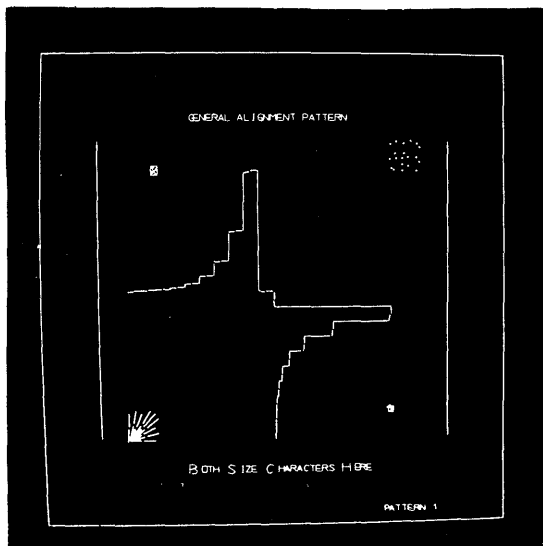
Figure 4-4. Absolute Vector Graphics Malfunctions (Sheet 5 of 7)



11. Shorted switch in 1/2 bit 0.  
Shorted switch in bit 1 is identical.



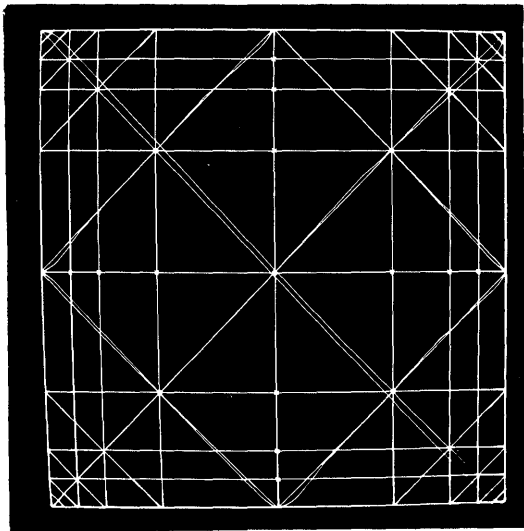
12. Shorted switch in bit 3. Note decrease in distortion. No decrease in distortion as weight of shorted bit decreases. Check 01AA2 H4/H5.



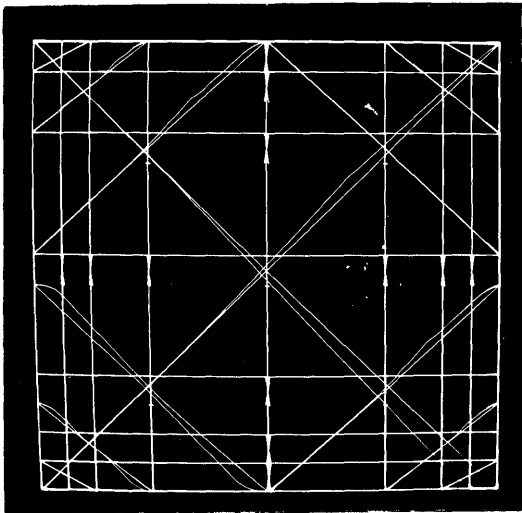
13. Shorted switch in bit 4. This fault could be mistaken for improper basic unit damping. Check 01AA2 G4/G5.

Figure 4-4. Absolute Vector Graphics Malfunctions (Sheet 6 of 7)



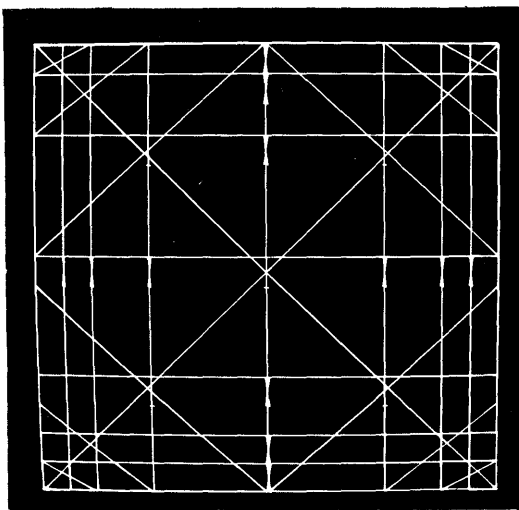


14. 01AA2G6D13 single-shot in Delta Cntr Clock too wide.\*



15. Both 02BB1M6B13 and 02BB1K2D12 outputs too wide.\*

\*Narrow pulses are noncritical.



16. Analog delay too great to - clear Compute Delta latch and + Start Delta Cntr. Either 02BB1K2D12 or 02BB1M6B13 single-shot adjusted for excessive pulse width.\*

Figure 4-4. Absolute Vector Graphics Malfunctions (Sheet 7 of 7)

to ground. This voltage is nominally +29vdc and can be varied between +28 and +32vdc with the reference voltage potentiometer on the 01AA1 potentiometer panel. If this voltage is present, proceed to step 17. If this voltage is not present:

- a. Turn off power.
  - b. Replace cards in 01AA2H2/H3, K2/K3, and M2/M3.
  - c. Turn on power.
  - d. Adjust voltage to +29vdc  $\pm$  0.1vdc.
17. Check for alignment of dc offset. If vertical and horizontal vectors intersect the crosses properly, proceed to step 18. If all full-length vectors are not coincident with the crosses:
- a. Determine faulty half-axis.
  - b. Turn off power.
  - c. Replace the following analog cards as required:
    - (1) X' and X axes - Cards 01BA2B2/B3, 01BA3D2/D3, and 01BA3E2
    - (2) Y' and Y axes - Cards 01BA2C2/C3, 01BA3K2/K3, and 01BA3J2
  - d. Turn on power, and display AVG alignment pattern.
  - e. Readjust dc offset. (Refer to paragraph 4.2.9.)
  - f. Check the pattern for proper alignment.
18. Failure of this procedure to correct trouble should have isolated the malfunction to the digital logic. Using flow charts (paragraph 1.4) and ALD's, determine failing components by scoping. Also refer to Figure 4-5.
19. When the malfunction has been removed, align absolute vector graphics generator. (Refer to paragraph 4.2.9.) Restore the equipment.

#### 4.2.12 Phasing of Fans

After analog alignment of console is completed, observe display for jitter of analog alignment pattern. If jitter is present, proceed as follows:

1. Turn off console, disconnect one of the fans in 02B gate, and reverse the two leads at the two outer pin connections of the fan socket. Reconnect fan and turn on console. If amount of jitter decreases, leave fans in 02B as connected. If amount of jitter increases, after fan leads have been reversed, turn off console and return fan leads to their initial condition.
2. If no jitter is present after fan leads in 02B have been reversed, fans are properly oriented.
3. If some jitter is still apparent, turn off

console and disconnect one of the fans in 02A gate. Reverse the two leads at the two outer pin connections of the fan socket. Reconnect fan and turn on console. If amount of jitter decreases, leave fans in 02A as connected.

4. If jitter becomes worse, turn off console and return fan in 02A to its initial condition.

#### 4.2.13 Visual Effects of Controls on Analog Circuits

The following photographs (Figure 4-5) represent different sections of the General Alignment and Skew programs and show the effects of various digital controls on the analog circuits. The locations indicated refer to points called out on the overall Block Diagram Analog Print, FEDM Figure 9023. Some controls, when misadjusted, have only a slight visual effect on these programs, whereas others have a severe effect.

##### 4.2.13.1 Character Pre-Intensity Time Delays

Figure 4-5 (sheets 1 and 2) shows the effect of character pre-intensity time delays adjusted at 02BB3H2. The setting of this delay controls the interval between the start of the unblank pulse and the transfer of character stroke information to the character drivers.

The minimum setting of this delay has only a slight effect on the display (it works in conjunction with the character de-intensify time delay, paragraph 4.2.13.2). However, the maximum setting causes unblanking of strokes too early, as shown by the curvature of characters Z and T.

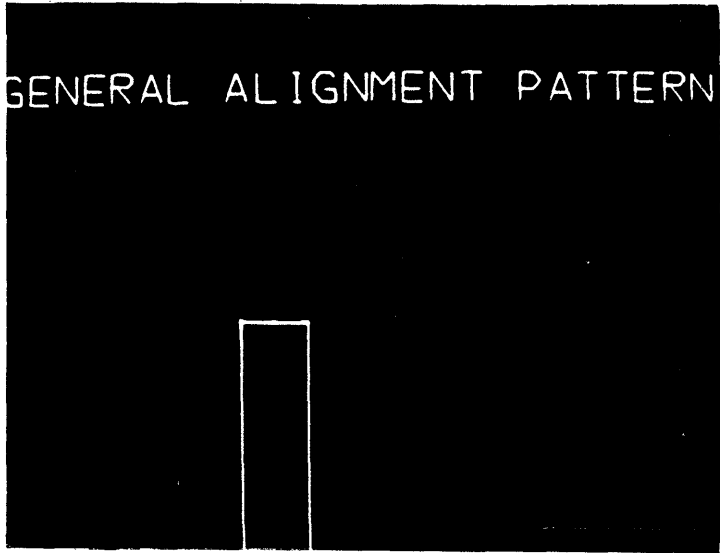
##### 4.2.13.2 Character De-Intensify Time Delay

Figure 4-5 (sheets 3 and 4) shows the effect of the character de-intensify time delay adjusted at 02BB3M3D13. The setting of this delay affects both the start and completion of the stroke unblank pulse. That is, it shifts the Stroke Unblank pulse with respect to the Stroke Length pulse. This shift provides an amount of early stroke blanking at the end of the stroke equal to the amount of early stroke unblanking at the beginning of the stroke.

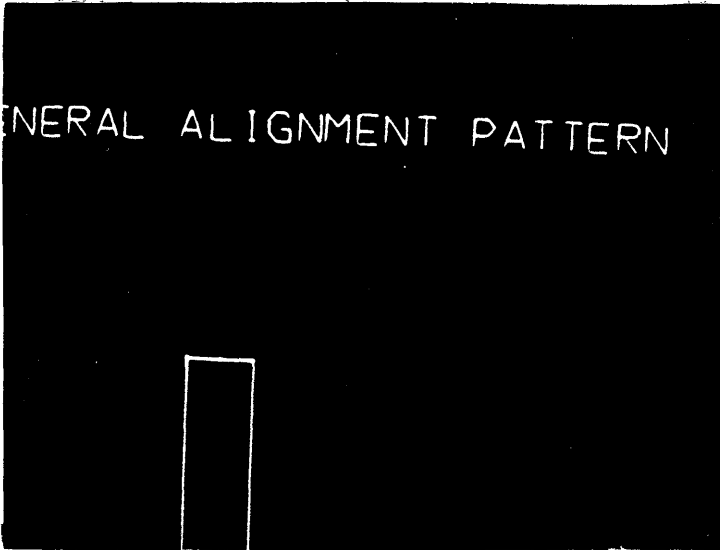
The minimum setting of this time delay has only a slight visual effect on the display. However, the maximum setting causes the early unblank of character strokes as seen on characters Z and T and, at the same time, causes the early blanking of strokes as seen on characters A, H, N, and T.

##### 4.2.13.3 Vector Pre-Intensify SS

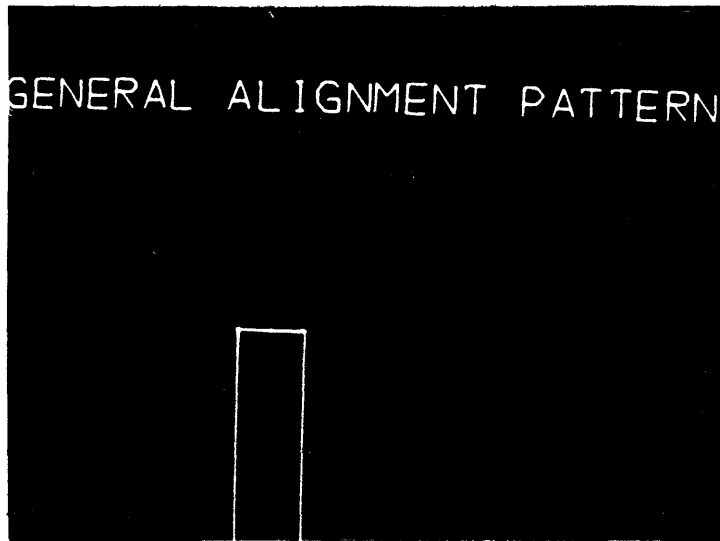
Figure 4-5 (sheet 5) shows the effect of the vector pre-intensify single-shot adjusted at 02BB1K2D13.



Standard size - Characters in adjustment

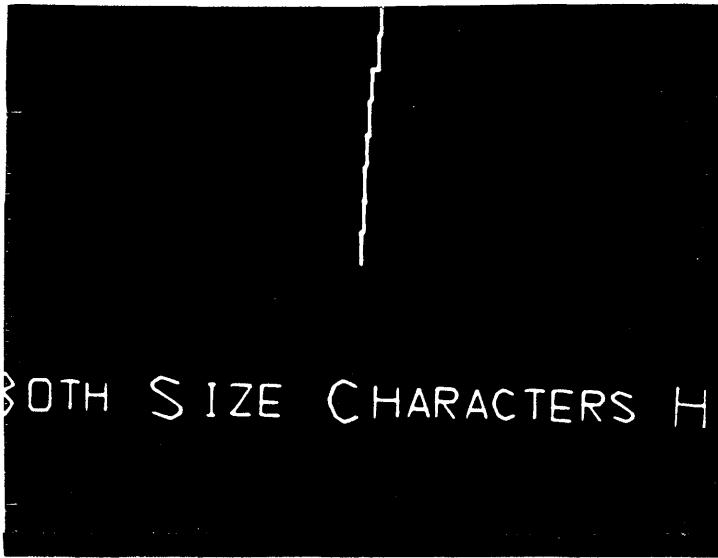


Standard size - Minimum setting of delays in 02BB3H2

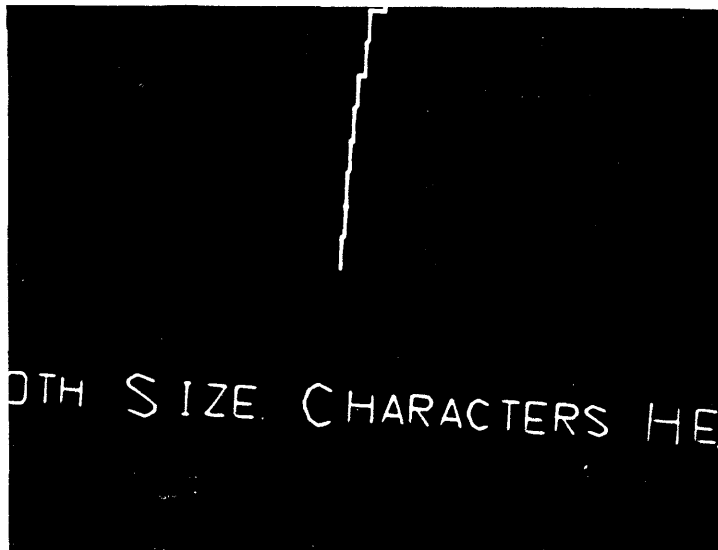


Standard size - Maximum setting of delays in 02BB3H2

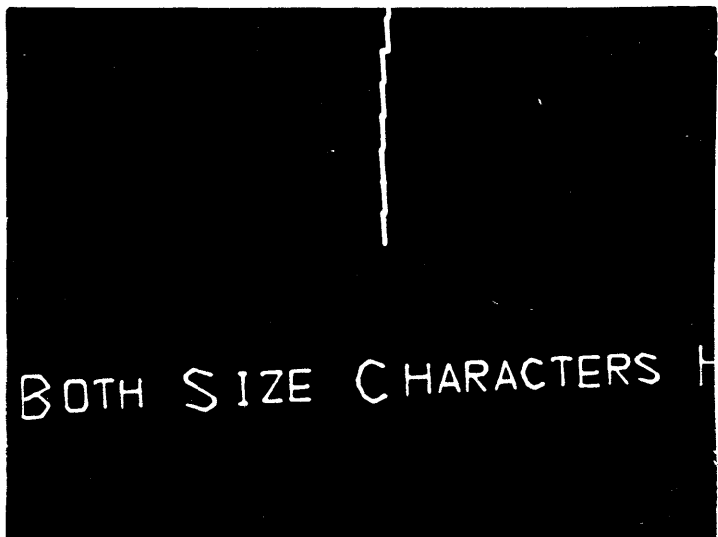
Figure 4-5. Analog Patterns (Sheet 1 of 12)



Expand size - Characters in adjustment

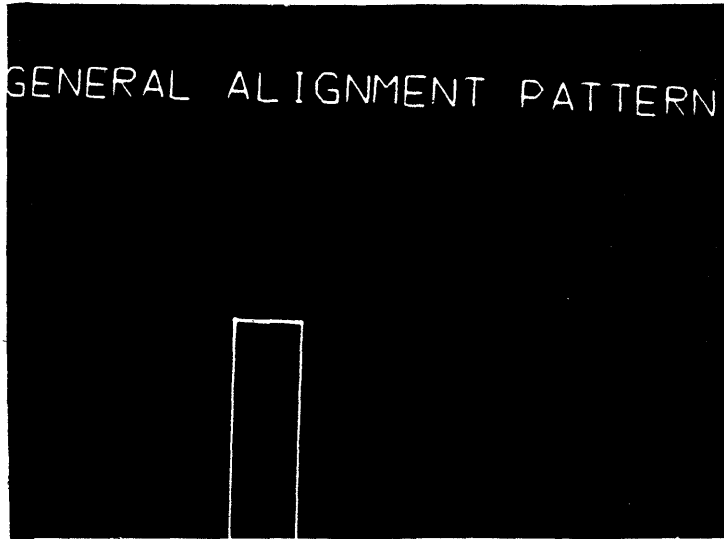


Expanded size - Minimum setting of delays in 02BB3H2

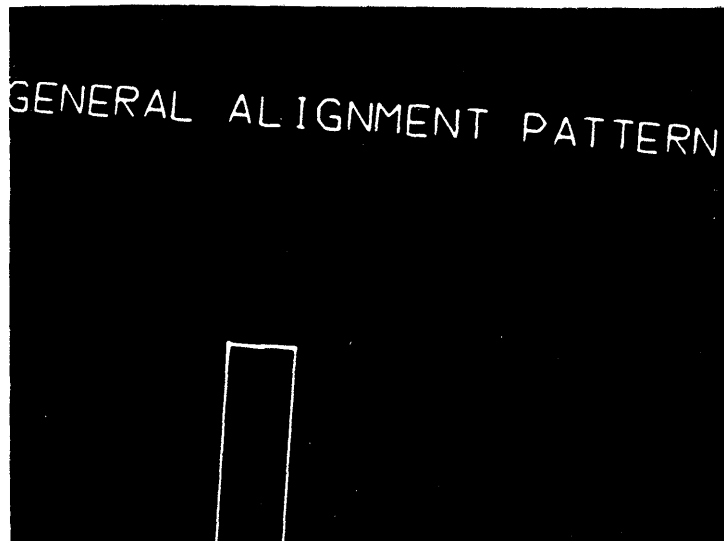


Expanded size - Maximum setting of delays in 02BB3H2

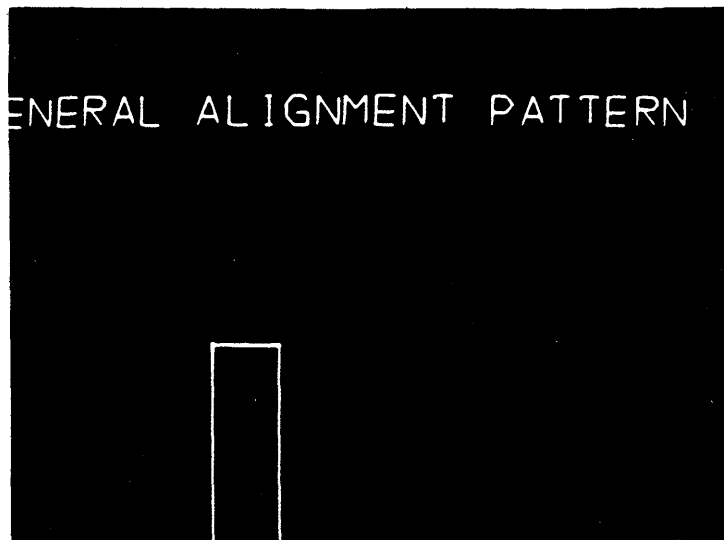
Figure 4-5. Analog Patterns (Sheet 2 of 12)



Standard size - Characters in adjustment

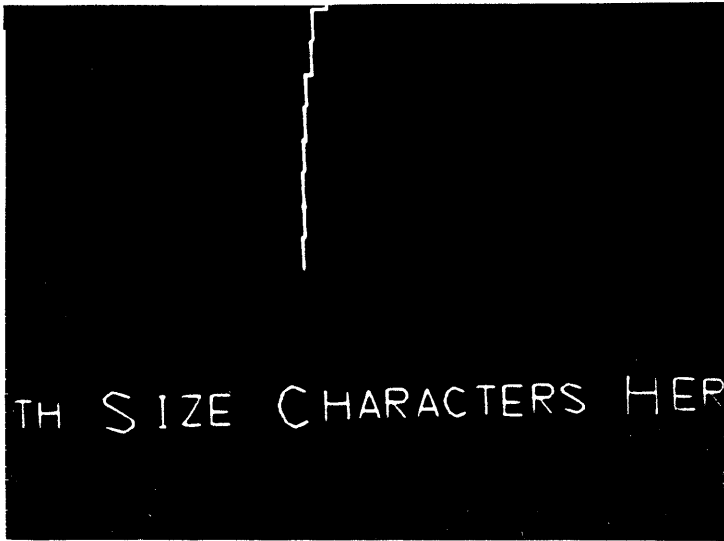


Standard size characters - Minimum setting of delay in 02BB3M3D13 upper

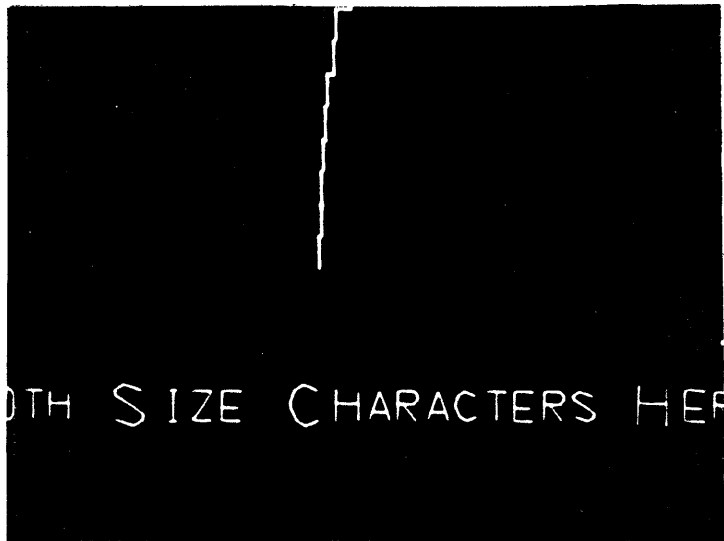


Standard size character - Maximum setting of delay in 02BB3M3D13 upper

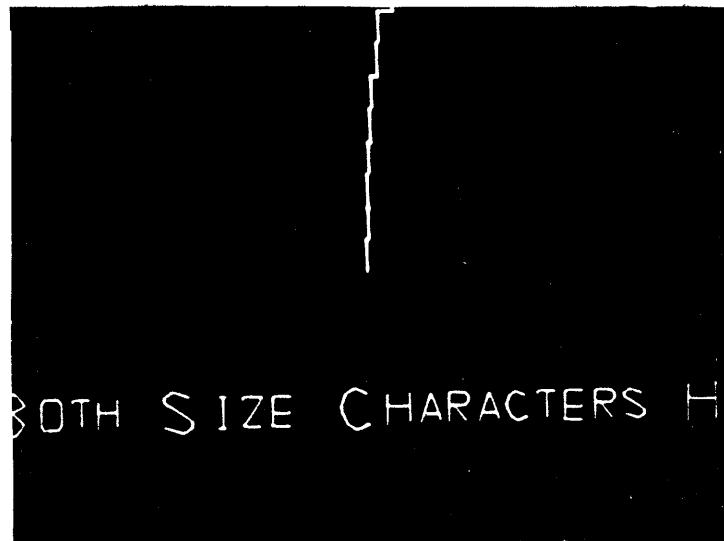
Figure 4-5. Analog Patterns (Sheet 3 of 12)



Expanded size - Characters in adjustment

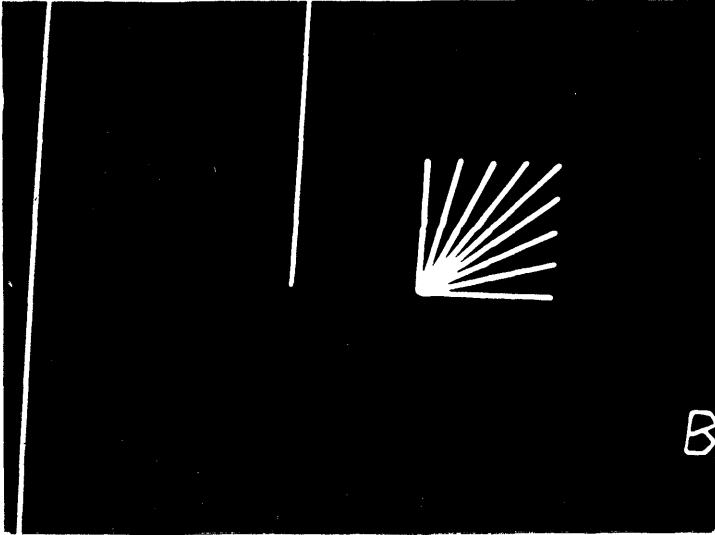


Expanded size characters - Minimum setting of delay in 02BB3M3D13 upper

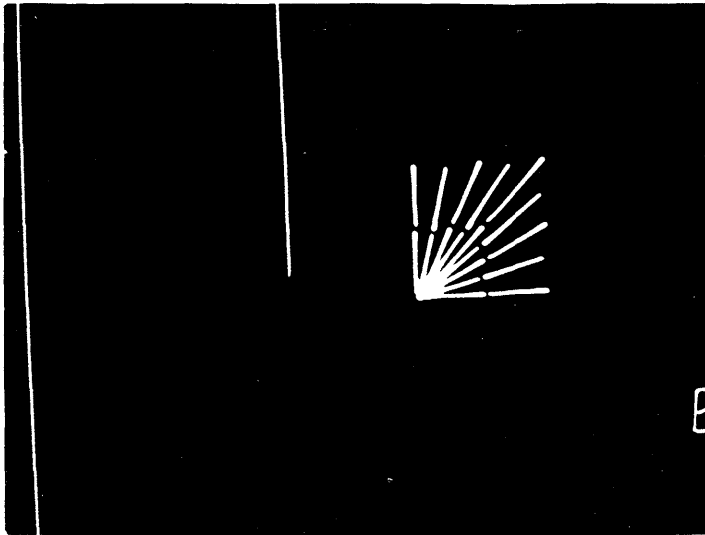


Expanded size characters - Maximum setting of delay in 02BB3M3D13 upper

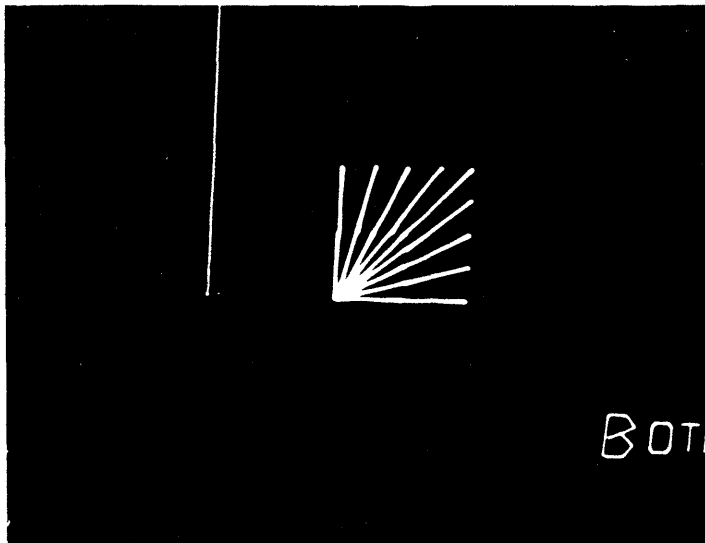
Figure 4-5. Analog Patterns (Sheet 4 of 12)



Normal alignment

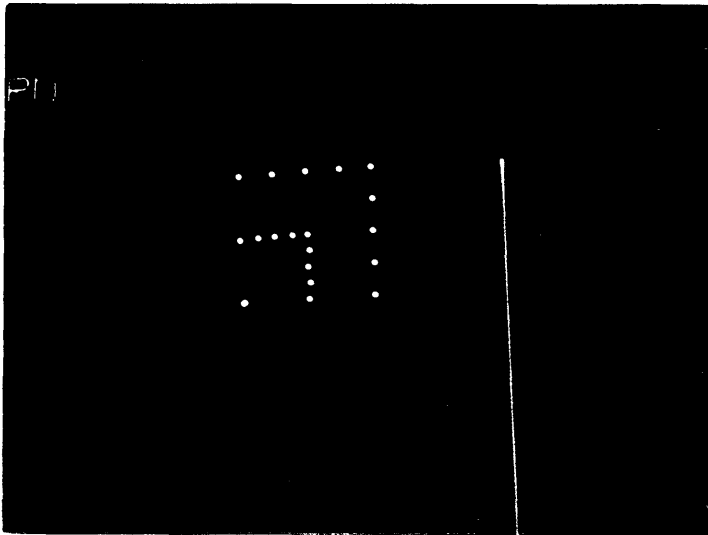


Insufficient vector - Preintensification  
single-shot located in 02BB1K2D13  
middle

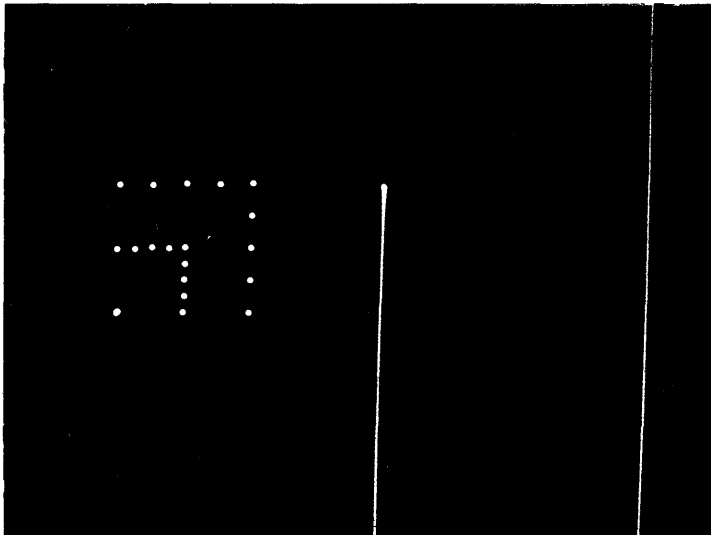


Excessive vector - Preintensification  
single-shot located in 02BB1K2D13  
middle

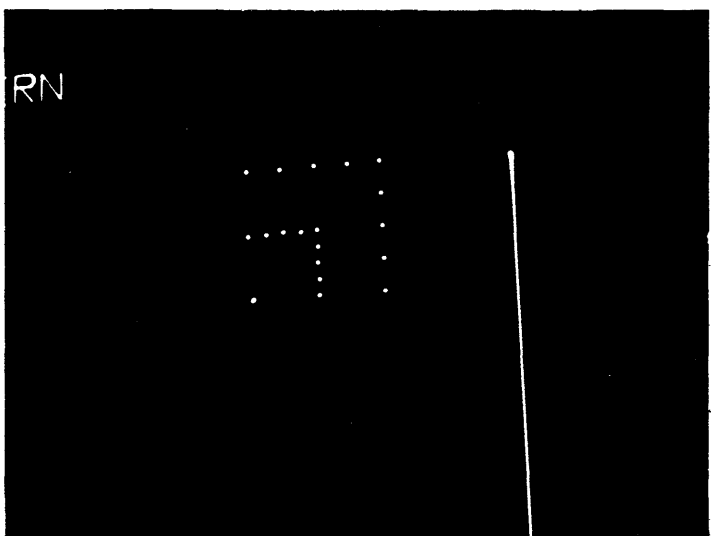
Figure 4-5. Analog Patterns (Sheet 5 of 12)



Point plot time = 700ns. Single-shot  
located in 02BB1E2D12 upper



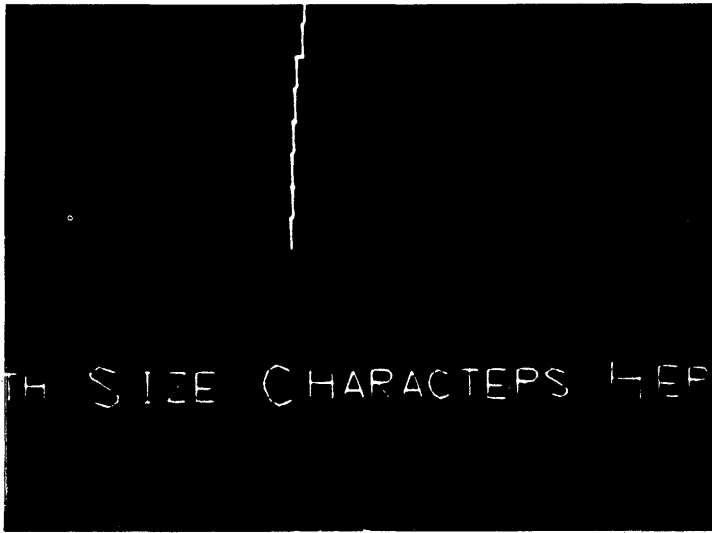
Point plot time = 1.1usec. Single-shot  
located in 02BB1E2D12 upper



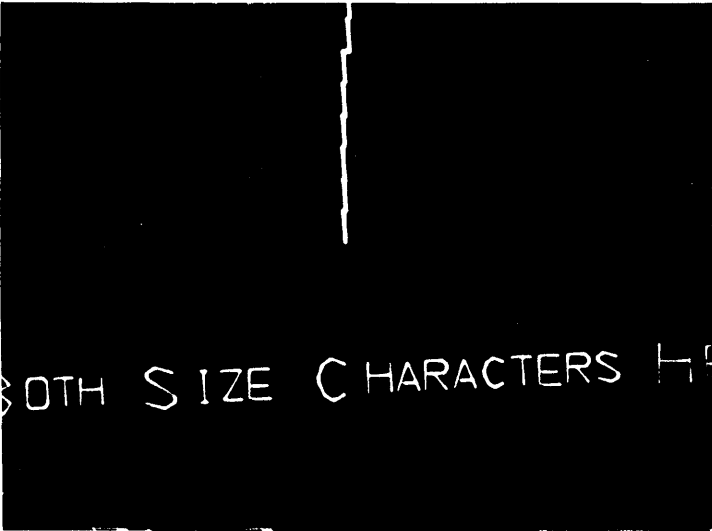
Point plot time = 150ns. Single-shot  
located in 02BB1E2D12 upper

●Figure 4-5. Analog Patterns (Sheet 6 of 12)

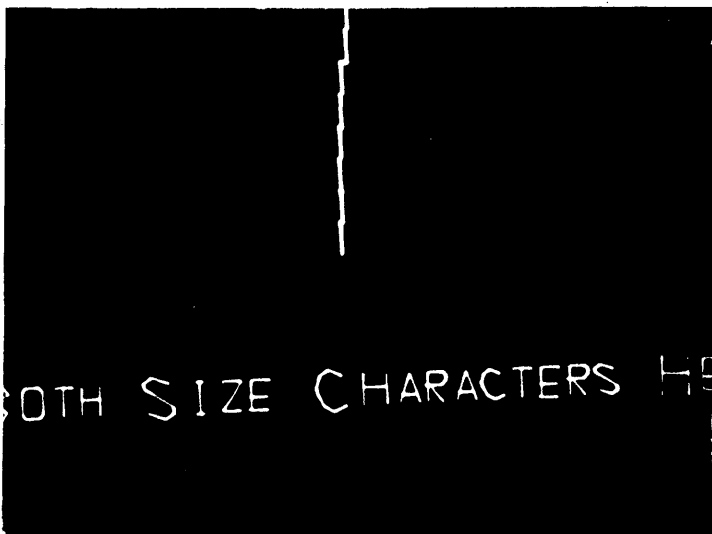




Character position overdrive adjusted.  
Single-shot located in 01BA3M6B02.\*



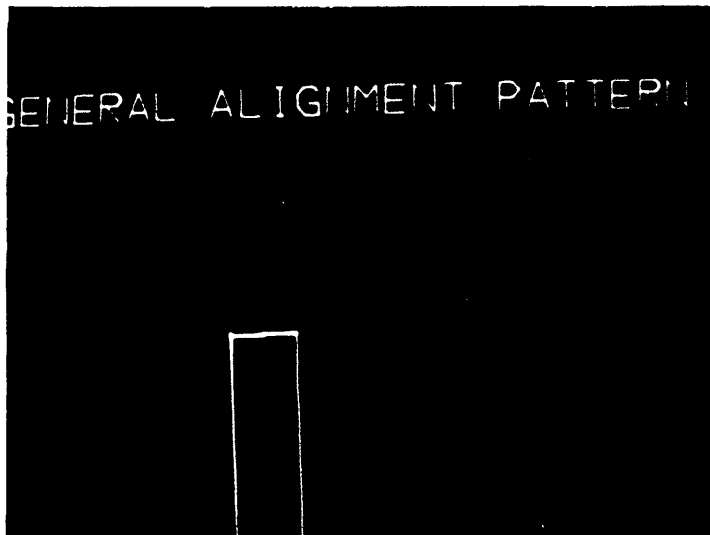
Character position overdrive.  
Single-shot located in 01BA3M6B02.\*  
Set for 500ns.



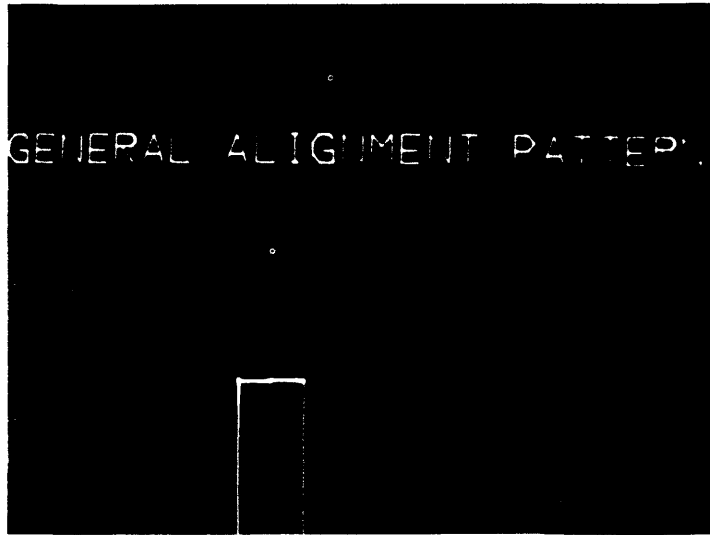
Character position overdrive.  
Single-shot located in 01BA3M6B02.\*  
Set for 4.25usec.

\*See Note 13, Figure 4-6.

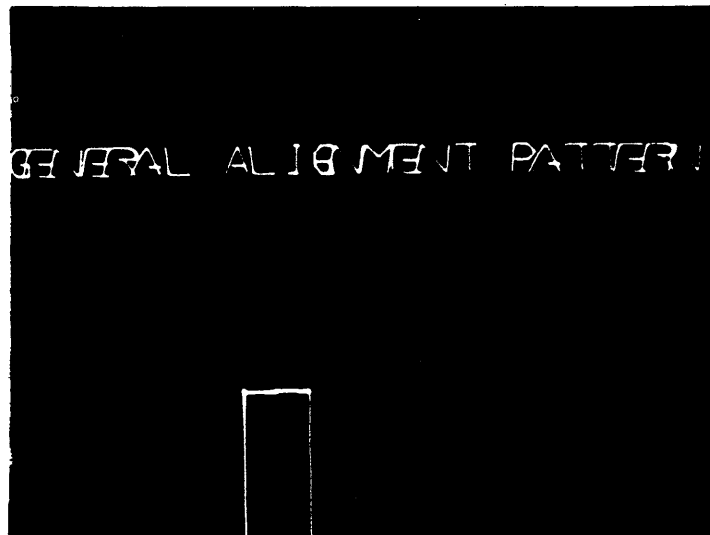
Figure 4-5. Analog Patterns (Sheet 7 of 12)



Position change time. Standard size.  
Normal  $\approx 3\mu\text{sec}$  single-shot located  
in 02BB1F2B02.\*



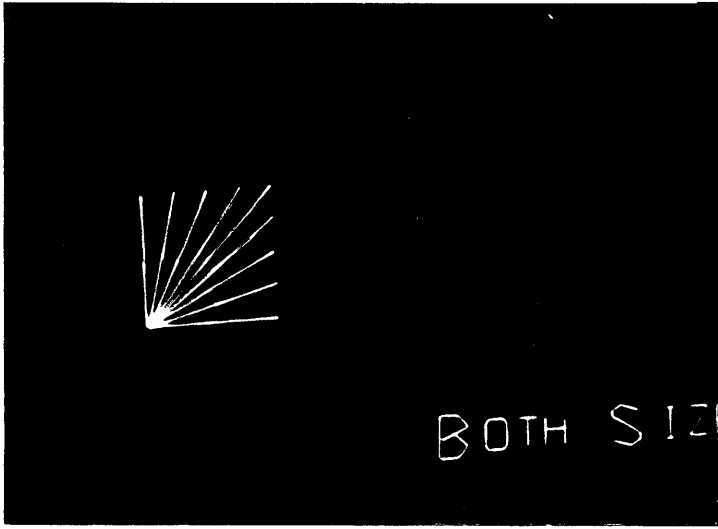
Position change time. Standard size.  
Change time set high  $\approx 5\mu\text{sec}$   
single-shot located in 02BB1F2B02.\*



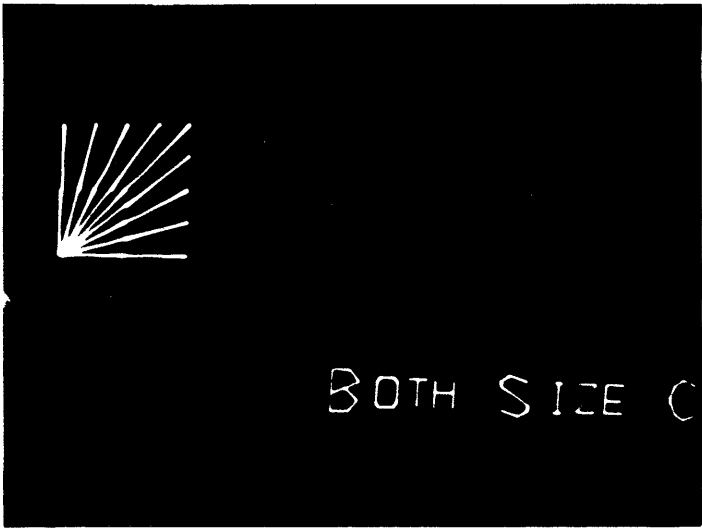
Position change time. Standard size.  
Change time set low  $\approx 500\text{ns}$   
single-shot located in 02BB1F2B02.\*

\*See Note 13, Figure 4-6.

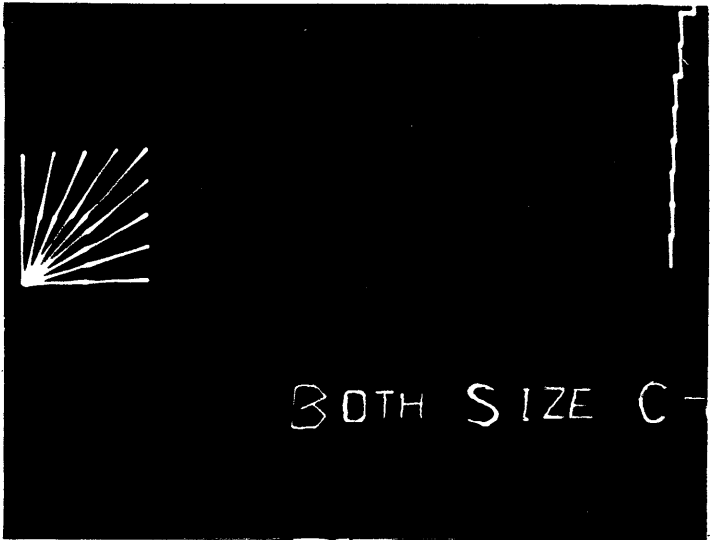
Figure 4-5. Analog Patterns (Sheet 8 of 12)



Position change time. Character mode.  
Expanded size adjusted. Single-shot  
located in 02BB1G2B02.\*



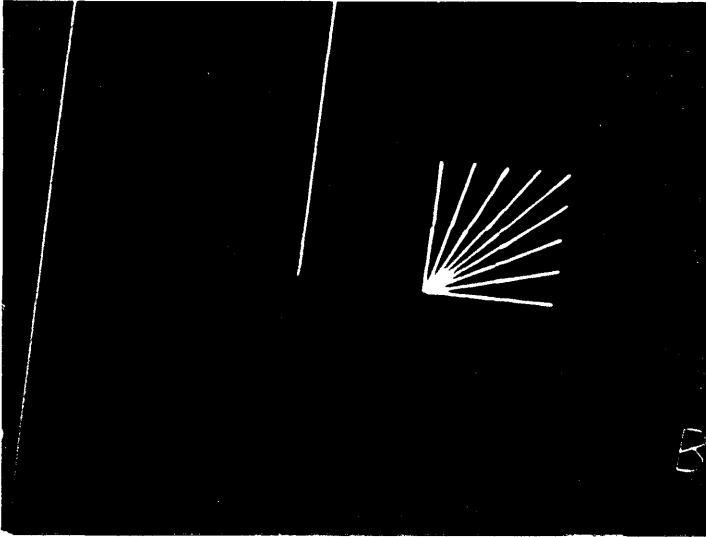
Position change time. Character mode.  
Expanded size. Single-shot located in  
02BB1G2B02.\* Set for 4usec.



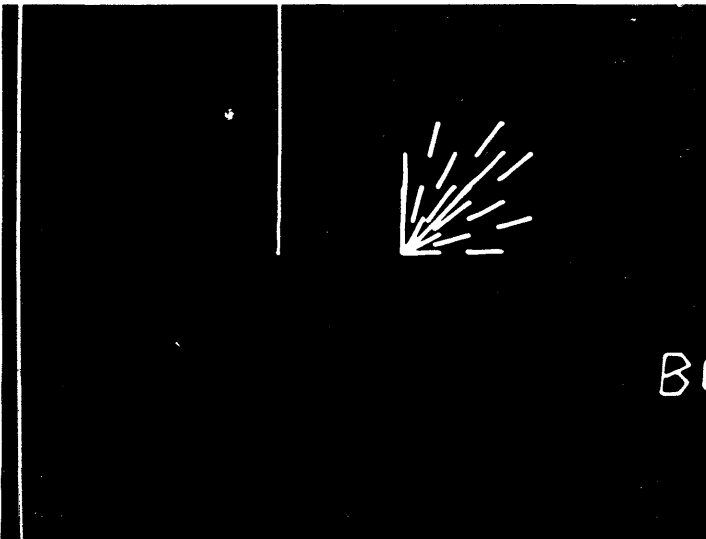
Position change time. Character mode.  
Expanded size. Single-shot located in  
02BB1G2B02.\* Set for 500ns.

\*See Note 13, Figure 4-6.

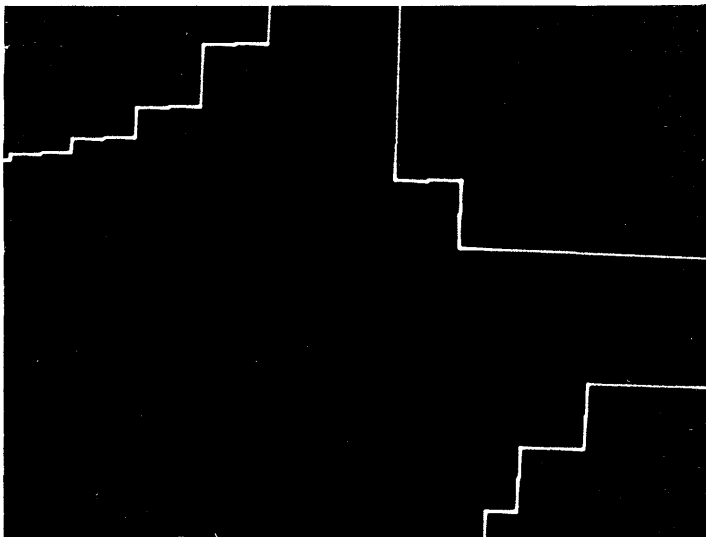
●Figure 4-5. Analog Patterns (Sheet 9 of 12)



Minimum position time adjusted.  
 Single-shot located in 02BB1G6B02  
 upper. Set for 7.25usec.

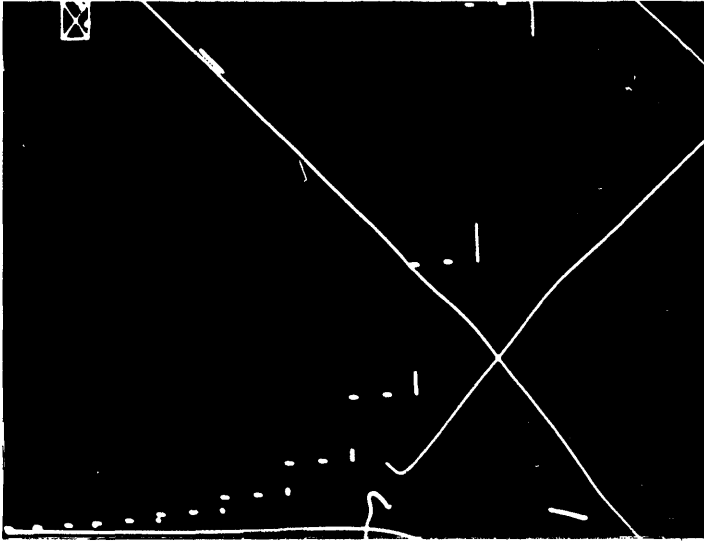


Minimum position time. Single-shot  
 located in 02BB1G6B02 upper. Set  
 for 2.5usec.

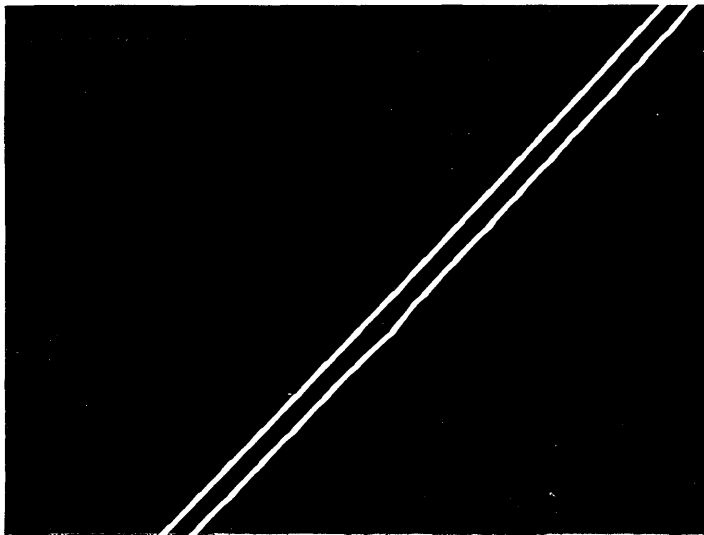


Minimum position time adjusted.  
 Single-shot located in 02BB1G6B02  
 upper. Set for 7.25usec.

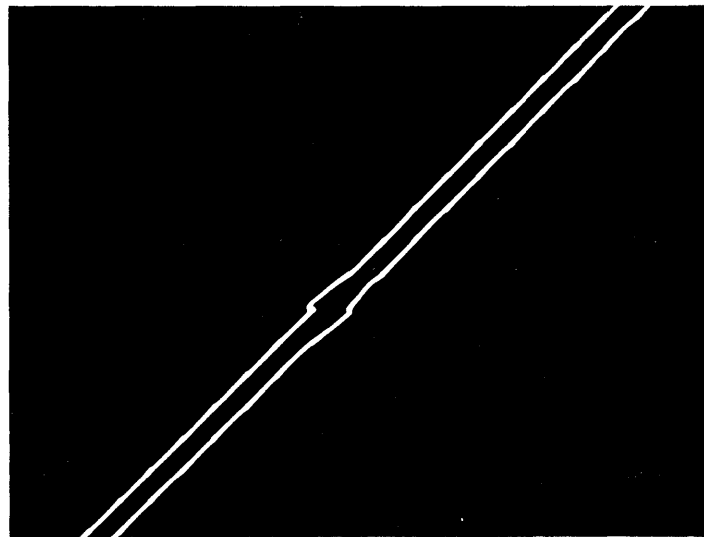
Figure 4-5. Analog Patterns (Sheet 10 of 12)



Minimum position time. Single-shot located in 02BB1G6B02 upper. Set for 1usec.

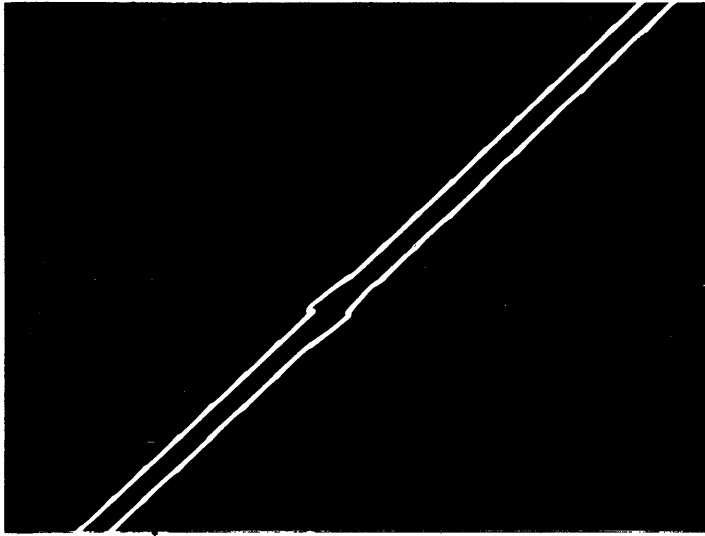


De-skew single-shot adjusted 02BB1F2 = 200ns. 02BB1E2 adjusted for minimum. Straight line variation  $\approx$  400ns.

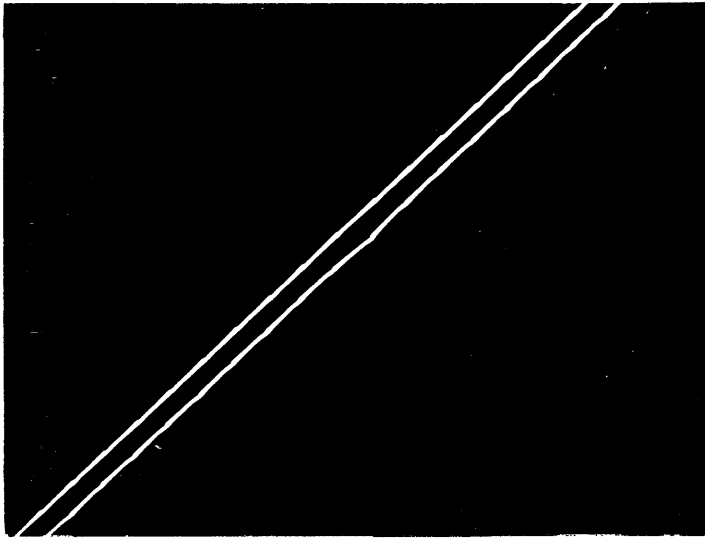


02BB1F2 = 100ns  
02BB1E2 = 100ns

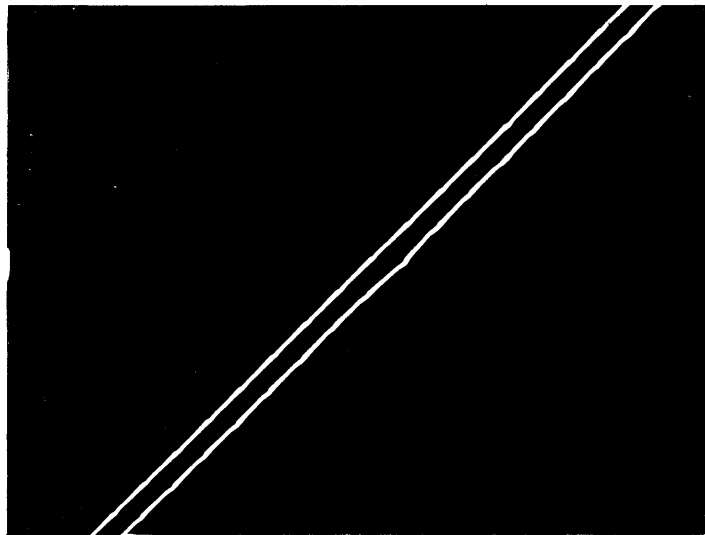
Figure 4-5. Analog Patterns (Sheet 11 of 12)



De-skew single-shot adjusted 02BB1F2  
= 50ns. 02BB1E2  $\approx$  400ns.



02BB1F2 = 400ns  
02BB1E2 = 400ns



02BB1F2 = 200ns  
02BB1E2 = 950ns

Figure 4-5. Analog Patterns (Sheet 12 of 12)

The setting of this delay controls the interval between the start of the unblank pulse and the transfer of information into the main positioning X-Y registers.

Insufficient vector pre-intensification causes gapping on the vector fan and loss of the beginning of the vertical vector. Excessive vector pre-intensification causes intensity pile-up on the vector fan and intensity pile-up at the beginning of the vertical vector.

#### 4.2.13.4 Point Plot SS

Figure 4-5 (sheet 6) shows the effect of the point-plot single-shot adjusted at 02BB1E2D12. The single-shot controls the length of the unblank pulse while the unit is in the Point Plot mode.

Excessive time will cause the point-plot fan dots to have excessive intensity with respect to characters and vectors, whereas minimum time results in insufficient intensity of points with respect to characters and vectors.

#### 4.2.13.5 Character Position Overdrive SS

Figure 4-5 (sheet 7) shows the effect of the character position overdrive single-shot adjusted at 01BA3M6B02. This single-shot controls the length of time that overdrive current is added to the main positioning current during positioning time while in the Character mode.

Insufficient time prevents the single-shot from reaching the true address before the character strokes are started. This is evidenced by a horizontal stroke on the A not meeting the left diagonal stroke, by the vertical stroke on the E not quite meeting the bottom two horizontal strokes, and by the first stroke on the H not being vertical.

Excessive time causes the single-shot to overshoot the true address and then starts the character strokes. This is shown by the vertical stroke on the E starting to the right of the beginning of the bottom horizontal stroke. This distortion is also evidenced on the R and A.

#### 4.2.13.6 Position Change Time, Standard Characters

Figure 4-5 (sheet 8) shows the effects of the position change time, standard size characters single-shot adjusted at 02BB1F2B02. This single-shot controls the time duration for positioning the beam between characters while the unit is in the Character mode, standard size.

Excessive time has no visual effect on the display, as this just ensures that the main positioning yoke will be settled before the character strokes are started.

Insufficient time does not allow the main positioning yoke to completely settle before the character strokes are started, resulting in the distortion shown. Since this single-shot works in conjunction with the character position overdrive single-shot, the alignment procedure should be performed when an adjustment is necessary.

#### 4.2.13.7 Position Change Time, Expanded Characters

Figure 4-5 (sheet 9) shows the effects of the position change time, expanded size characters single-shot adjusted at 02BB1G2B02. This single-shot controls the time duration for positioning the beam between characters while the unit is in the Character mode, expanded size.

The effects of these controls are the same for expanded-size characters as the effects of the position change time standard size single-shot are for the standard-size characters.

#### 4.2.13.8 Minimum Position Time SS

Figure 4-5 (sheets 10 and 11) shows the effects of the minimum position time single-shot adjusted at 02BB1G6B02. If the graphic design feature is installed, minimum position time is controlled by a complementing flip-flop that selects single-shots 02BB1G6B02 upper and 02BB1G7B02 upper (alternately).

The single-shot(s) ensures that all positioning movement equal to or less than 32 raster units will be allowed 7.5usec to settle before a new positioning change occurs.

Excessive positioning time does not affect the visual display.

A positioning time of 2.5usec results in the distortion shown on the fan pattern. A positioning time of 1usec is catastrophic to the visual display.

#### 4.2.13.9 De-Skew SS

Figure 4-5 (sheets 11 and 12) shows the effects of the de-skew single-shots adjusted at 02BB1F2D02 and 02BB1E2D13. The single-shot adjusted at 02BB1F2D02 controls the time that the de-skew pulse starts prior to the transfer of new information into the X-Y registers. The single-shot adjusted at 02BB1E2D13 controls the amount of time the de-skew pulse overlaps the transfer of new information into the X-Y registers. The analog signal generated by this de-skew pulse prohibits a current change in the main positioning yoke during this time, ensuring that all deflection bit switches are fully switched and settled before the new deflection current is applied to the yoke.

Insufficient time on either of these single-shots results in the distortion shown, whereas excessive time has no visual effect.

#### 4.2.14 CRT Arc-Protection Check

The CRT arc-protection circuit (01C-TB1 and 01C-TB3) check ensures that the circuit is operating properly. This procedure is useful because the arc-protection circuit cannot be changed quickly. All measurements are made with a voltmeter.

If any of the measurements cannot be obtained as described in the following procedure, the circuit is not operating correctly. Refer to Appendix C of FE Theory of Operation, Form Y27-2043-0, and to the analog reference drawings on page AN101 of the logic manuals.

1. Turn off power, and wait for machine to cycle down.
2. Remove CRT socket from CRT, turn on power, and wait for machine to cycle up.

#### **DANGER**

A current of 450v is present on the CRT socket when measurements are made in the steps that follow.

3. Measure voltage between pin 2 of CRT socket and ground. Reading should be  $-30v \pm 2v$ .
4. Measure voltage between pin 11 of CRT socket and ground. Turn CE brightness limiting potentiometer fully clockwise, and vary operator's brightness control. Voltage readings should vary from approximately +19v to approximately +80v. Set brightness control at +45v.
5. Turn off power, and wait for it to cycle down.
6. Remove SLT card (PN 5801308) in location 01B-A2J6/J7.
7. Place a temporary jumper between 01C-TB3A2 and 01C-TB3A5 (+36v to input network of 183 transistor). Ensure that jumper is not shorted against any other points.
8. Turn on power, and wait for it to cycle up.
9. Again measure voltage between pin 11 of CRT socket and ground. Voltage reading at this time should be approximately +80v.
10. Turn off power, and wait for it to cycle down.
11. Remove jumper inserted in step 7. Connect CRT socket to CRT, and insert SLT card (PN 5801308) in 01B-A2J6/J7.
12. Turn on power, wait for it to cycle up, and readjust console brightness controls as described in step 1 of paragraph 4.2.2.

### 4.3 SINGLE-SHOTS, TIMING, AND ADJUSTMENT

Figure 4-6 lists the single-shots found in a 2250-1 with all available features. The figure contains SLT card locations, logic page references, input pins, output pins, potentiometer locations on the SLT card (upper, middle, lower), and output durations. Also included is a diagnostic program column that refers either to a diagnostic program or to a note. The three-digit number is the number of the diagnostic program to be used to check and adjust the associated single-shot. The notes are at the bottom of the figure. Single-shots listed at 02BA2J2 are not used when the graphic design feature is installed.

The single-shots are adjusted by means of a potentiometer mounted on the SLT card. All single-shot output tolerances are  $\pm 5$  percent unless otherwise specified.

### 4.4 DELAY LINE ADJUSTMENTS

Figure 4-7 lists the delay lines used in a fully equipped 2250-1. Included are the physical locations, logic pages, the locations of the delay line circuits on the SLT card (upper, lower), the jumper positions to obtain the desired delay, and the delay of each circuit.

The time delay of each delay line, except the fixed delay in position 02B-B3M6, is set by inserting jumpers in accordance with Figure 4-7. Delay line tolerances are  $\pm 5$  percent, unless otherwise specified. Figure 4-8 is a schematic of the adjustable delay line circuit.

### 4.5 M-8 STORAGE ADJUSTMENTS

The board location for the M-8 storage (buffer) is 02A-A1. Storage adjustment should not be made in the field unless a card having a potentiometer is replaced or unless there is a clear indication that the storage is not adjusted properly. If storage adjustments must be made in the field, use the storage adjustment procedure described on systems manual page SC011 (PN 2196629).

### 4.6 POWER PACK REMOVAL

To remove the power pack assembly (PN 5712354) from the 2250-1, proceed as follows:

1. Remove all power from 2250-1.
2. Open wing gates (01A and 01B) as far as possible.
3. Remove screws from frame side of bottom hinge of wing gate 01A. (Removal of the



Note 1 Diagnostic Program	Board	Card Location	Card PN	Logic Page	Jumper from/to	Input Pin	Pot Pos	Test Point	Nom	Min.	Max.	
	BASIC:											
762	02A-B3	G6	3333	TA111	B13-D04	D07	Lo	D02	250ns	238ns	262ns	
762		G6	3333	TA111		B03	Up	B02	2usec	1.9usec	2.1usec	
762		H6	3333	TA111		D07	Lo	D02	250ns	238ns	262ns	
762		H6	3333	TA111		B03	Up	B02	3usec	2.85usec	2.15usec	
Note 2		J6	3333	TA101		B03	Up	B02	40ms	38ms	42ms	
Note 2		K7	3338	TA101		B03	Mid	D13	1.0usec	.95usec	1.05usec	
762		K7	3338	TA001		B02	Up	D12	150ns	143ns	157ns	
762		L7	3338	TA031		D11	Up	D12	200ns	190ns	210ns	
762		L7	3338	CD041		B03	Mid	D13	350ms	332ms	368ms	
766		02A-A3	E6	3333		LD031	B08	Lo	D02	135ns	128ns	142ns
766	02A-A3	G6	3338	XY001	B03	Mid	D13	400ns	380ns	420ns		
766		G6		LD071	D06	Lo	B13	250ns	238ns	262ns		
766		G6		LD061	B02	Up	D12	1.1usec	1.0usec	1.2usec		
Note 2		L6	3339	MR001	B03-B04	D13	Up	D06	100ms	95ms	105ms	
759		L6		TC232	B03-B04	B12	Lo	D04	300usec	285usec	315usec	
766		M6	3338	XY011	B03	Mid	D13	.65usec	.62usec	.68usec		
766		M6		XY011	D04	Lo	B13	.65usec	.62usec	.68usec		
766		M6		XY011	D11	Up	D12	200ns	190ns	210ns		
766		M2	3338	XY011	B03	Mid	D13	250ns	238ns	262ns		
76B		M2		XY011	D04	Lo	B13	.5usec	.48usec	.52usec		
76B	M2		XY011	D11	Up	D12	250ns	238ns	262ns			
766	02A-A3	D4	3339	LD071	B04-B02	B12	Lo	D04	12.0ms	10.0ms	12.5ms	
766		D4		LD071	B05-B09	D13	Up	D06	12.0ms	10.0ms	12.5ms	
766		02B-A2	G2	3338	LP001	B03	Mid	D13	250ns	238ns	262ns	
766		G2		LP001	D04	Lo	B13	250ns	238ns	262ns		
Note 3		G2		LP011	D11	Up	D12	200ns	190ns	210ns		
Note 4		J4	3333	LP011	B07	Lo	D02	250ns	238ns	262ns		
Note 4		J4		LP011	B13-D04	B05	Up	B02	See Note 14			
766		J2	3333	LT011	B07	Lo	D02	50ns	48ns	52ns		
766		J2		LT011	B03	Up	B02	200ns	190ns	210ns		
766		D2	3338	LP001	B03	Mid	D13	250ns	238ns	262ns		
766	D2		BC001	D11	Up	D12	250ns	238ns	262ns			
Note 15	02B-A2	D2	3338		D04	Lo	B13	See Note 15				
762	02A-B1	J3	3338	TC271	B03	Mid	D13	250ns	238ns	262ns		
Note 2		J3		TC271	D04	Lo	B13	250ns	238ns	262ns		
759		J3		TC232	D11	Up	D12	500ns	475ns	525ns		
762		M3	3338	TC231	B03	Mid	D13	250ns	238ns	262ns		
762		M3		TC232	D04	Lo	B13	250ns	238ns	262ns		
762		M3		TC232	D11	Up	D12	250ns	238ns	262ns		
Note 5		02A-B1	L2	3338	TC301	B03	Mid	D13	250ns	238ns	262ns	
Note 2		02A-B2	D2	3333	TA091	B07	Lo	D02	250ns	238ns	262ns	
762		D2		TA021	B03	Up	B02	150ns	143ns	157ns		
762		J7	3333	SS021	B07	Lo	D02	150ns	140ns	160ns		
Note 2	J7		MR021	D13-D04	B03	Up	B02	100ns	95ns	105ns		
762	K7	3333	CD021	B07	Lo	D02	200ns	190ns	210ns			
Note 2	K7		MR021	D09-D04	B03	Up	B02	35usec	33.3usec	36.7usec		
750	02A-B2	M3	3337	CL041	Note 12	L4B02	1.5sec	1.4sec	1.6sec			
750	02A-B3	J6	3333	TA051	B07	Lo	D02	250ns	238ns	262ns		
760	02A-B3	B6	3338	TA091	B04	Mid	D13	400ns	380ns	420ns		
760		B6		TA091	D05	Lo	B13	250ns	238ns	262ns		
760		B6		TA091	B02	Up	D12	250ns	238ns	262ns		
750		02A-B3	K7	3338	TA031	D04	Lo	B13	150ns	140ns	160ns	
766		02B-B1	E2	3338	PP021	B03	Mid	D13	See par. 4.2.3			
766		E2		PP011	D04	Lo	B13	200ns	190ns	300ns		
766		E2		PP011	B02	Up	D12	700ns	665ns	735ns		
766		F2	1697	PP021	B07	Note 13	D02	See par. 4.2.3				
766		F2		PP011	B13-D04	B03	Note 13	B02	2.75uscc	2.0usec	3.0usec	
758		F6	3333	CS021	B07	Lo	D02	230ns	238ns	262ns		
Note 6	02B-B1	F6		CE081	B03	Up	B02	10usec	9.5usec	10.5usec		

●Figure 4-6. Single-Shots (Sheet 1 of 3)

Diagnostic Program	Board	Card Location	Card PN	Logic Page	Jumper from/to	Input Pin	Pot Pos	Test Point	Nom	Min.	Max.	
766	02B-B1	G2	1697	PP011		B08	Note 13	D02	200ns	190ns	210ns	
766		G2		PP011	B13-D04	B03	Note 13	B02		See par. 4.2.6		
758		G5	3333	CS021		B07	Lo	D02	200ns	190ns	210ns	
758		G5		CS021	B13-D04	B03	Up	B02	2usec	1.9usec	2.1usec	
766		G6	3333	PP011		B07	Lo	D02	200ns	190ns	210ns	
766		G6		PP011	B13-D04	B03	Up	B02	7.25usec	6.9usec	7.6usec	
Note 6		J4	3338	CE071		B03	Mid	D13	135ns	128ns	142ns	
Note 6		J4		CE071		D04	Lo	B13	135ns	128ns	142ns	
Note 7		J4		CE071		B02	Up	D12	250ns	238ns	262ns	
766		K2	3338	PP031		D04	Lo	B13	250ns	238ns	262ns	
766		K2		PP031		B03	Mid	D13		See par. 4.2.3		
757, 767		02B-B1	K2	3338	VG101		D11	Up	D12		See par. 4.2.2	
766		02B-B2	J2	3333	TP001		B08	Lo	D02	Note 16	Note 16	Note 16
766		01B-A3	M6	1697	XR011		B05	Note 13	B02		See par. 4.2.6	
Note 9	01A-A3	B2	3339	PF031	B04-B02	D10	Lo	D04	36ms	34ms	38ms	
Note 9	01A-A3	B2		PF041	B05-B09	D13	Up	D06	115ms	109ms	121ms	
Note 10	02A-A2	J7	3338	CE091		B03	Mid	D13	250ns	238ns	262ns	
Note 10	02A-A2	J7		CE091		D04	Lo	B13	250ns	238ns	262ns	
Note 11	02A-A2	J7		CE091		D07	Up	D12	250ns	238ns	262ns	
	02B-A1	E7	3338	LP003		B03	Mid	D13	250ns	238ns	262ns	
	02B-A1	E7		LP003		D04	Lo	B13	300ns	285ns	315ns	
	02B-A1	E7		LP003		D11	Up	D12	250ns	238ns	262ns	
<u>ANKB:</u>												
Note 8	01A-A3	D7	3333	KB031		B07	Lo	D02	370ns	350ns	390ns	
Note 8	01A-A3	B7	3339	KB031	B04-B02	B12	Lo	D04	40ms	38.5ms	41.5ms	
Note 8	01A-A3	G7	3339	KB031	B04-B02	B12	Lo	D04	10ms	9ms	11ms	
<u>LPEN: OR GDF:</u>												
	02B-A1	F7	3338	LP002		B03	Mid	D13	250ns	238ns	262ns	
	02B-A1	F7		LP002		D04	Lo	B13	300ns	285ns	315ns	
	02B-A1	F7		LP002		D11	Up	D12	250ns	238ns	262ns	
<u>GRAPHIC DESIGN:</u>												
768	02B-B1	G7	3333	PP021	B13-D04	B03	Up	B02	7.25usec	6.90usec	7.60usec	
768	02B-B1	G7		VG111		B07	Lo	D02	250ns	238ns	262ns	
<u>CHARACTER GENERATOR:</u>												
766	02B-B3	L2	3338	ST011		B03	Mid	D13	200ns	190ns	210ns	
766		L2		ST011		D05	Lo	B13	200ns	190ns	210ns	
766		H3	3338	ST031		B03	Mid	D13	200ns	190ns	210ns	
766		H3		ST031		D04	Lo	B13	200ns	190ns	210ns	
766	02B-B3	H3		ST031		B02	Up	D12	200ns	190ns	210ns	
758	01A-A3	M2	3338	YA041		B03	Mid	D13	1.1usec	1.05usec	1.15usec	
766	01A-A3	M2		XA071		D04	Lo	B13	200ns	190ns	210ns	
758	01A-A3	M2		YA081		B02	Up	D12	250ns	238ns	262ns	
<u>CURSOR:</u>												
Note 8	02B-A1	H7	3339	AB011	B04-B03	B12	Lo	D04	60usec	57usec	63usec	
<u>ABSOLUTE VECTOR GRAPHICS:</u>												
757, 767	01A-A2	G6	3338	DC021		B03	Mid	D13	250ns	238ns	262ns	
757, 767	02B-B1	M6	3338	VG101		D04	Lo	B13	200ns	190ns	210ns	
757, 767	02B-B1	M6		VG101		D11	Up	D12		See par. 4.2.2		
757, 767	02B-B1	M6		VG101		B03	Mid	D13	250ns	238ns	262ns	

●Figure 4-6. Single-Shots (Sheet 2 of 3)

NOTES:

1. Use the Diagnostic Program indicated by the three-digit number to adjust associated single-shot.
2. This single-shot is fired by depressing the MACHINE RESET switch.
3. This single-shot is fired by depressing the Light Pen switch.
4. This single-shot is fired by depressing the Light Pen switch while running Diagnostic Program 766.
5. This single-shot can be fired while off line by activating the CE OP OUT switch.
6. This single-shot can be fired while off line by activating the SINGLE MODE REGENERATION pushbutton with Diagnostic Program 766 stored in the buffer.
7. This single-shot can be fired while off line by activating the SINGLE STEP pushbutton while the TPD MODE switch is in the SINGLE STEP position.
8. This single-shot can be fired while off line and displaying the general alignment pattern (program 766 in buffer) by activating the Advance Cursor key on the alphanumeric keyboard.
9. This single-shot can be fired while Diagnostic Program F76A is being run by depressing a program function keyboard key.
10. This single-shot can be fired while off line by activating the CE ENTER switch, with the CE LOAD SELECT switch in the buffer position.
11. This single-shot can be fired while off line by activating the CE READ BUFFER switch.
12. This single-shot must be adjusted in the home position. Use the CE controls or Diagnostic Program 750 or 760 to generate the Set Audible Alarm command.
13. On cards (PN 5801697) with the potentiometers mounted adjacent to each other, adjust the lower potentiometer for the D02 output and the upper potentiometer for the B02 output. On cards with a module separating the potentiometers, adjust the upper potentiometer for the D02 output and the lower potentiometer for the B02 output.
14. This single-shot should be adjusted to one of the following:

	<u>Nominal</u>	<u>Minimum</u>	<u>Maximum</u>
a. GDF not installed	8usec	7.6usec	8.4usec
b. GDF installed	4usec	3.8usec	4.2usec

15. This single-shot should be adjusted to one of the following:

	<u>Nominal</u>	<u>Minimum</u>	<u>Maximum</u>	<u>Diagnostic Program</u>	<u>Logic</u>
a. GDF not installed	300ns	285ns	315ns	766	LT011
b. GDF installed	250ns	238ns	262ns	76B	LP021

16. Refer to ALD TP001 for adjustment.

Figure 4-6. Single-Shots (Sheet 3 of 3)

hinges is necessary to obtain sufficient clearance for the power pack to be removed from the 2250-1.) Support the gate during this operation.

**CAUTION**

Avoid swinging the wing gate while it is supported by only one hinge.

4. Remove four keepers from each corner of power pack assembly.
5. Disconnect blower lead.
6. Remove external leads from terminal boards TB1 and TB2. Remove only those leads that would prevent assembly removal and not those coming from assembly components to terminal boards.
7. Slide assembly out a sufficient distance to gain access to diode leads.
8. Unsolder external leads to diodes (only those leads that would prevent removal of the assembly).
9. Remove ground strap.
10. Remove power pack assembly.

11. Replace power pack assembly by reversing procedure.

**4.7 SLT POWER SUPPLY REMOVAL**

To remove the individual SLT power supplies, proceed as follows:

1. Remove all power from 2250-1.
2. Remove external leads from SLT supply terminal board. Remove only those leads that prevent removal of supply.
3. Remove two keepers.
4. Remove power supply carefully to avoid breaking wires or cables in path of removal.
5. Replace by reversing procedure.

**4.8 HIGH-VOLTAGE POWER SUPPLY REMOVAL**

**DANGER**

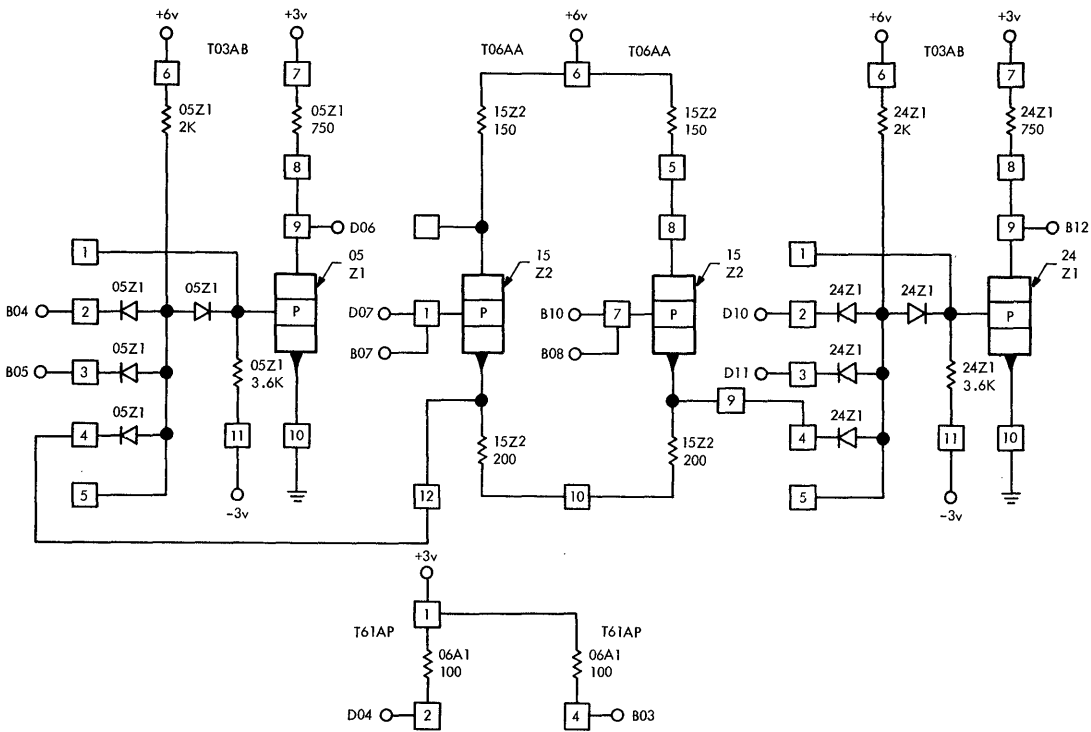
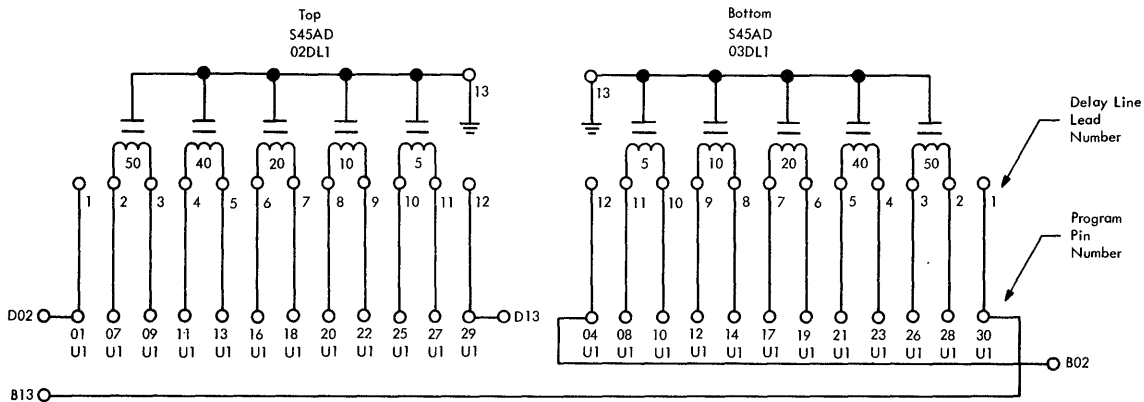
The high-voltage power supply develops +16,000v, +450v, and +80v. Exercise extreme caution when working on or near the high-voltage power supply. Do not attempt to repair the high-voltage supply beyond replacement of pluggable cards.

Physical Location	Logic Page	Delay Circuit Location on SLT Card	Jumper Positions	Nom.	Delay Min.	Max.
02A-A3 C6	LD081AM	Upper	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02A-A3 C6	LD081AN	Lower	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02A-B1 C2	TC231DR	Upper	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02A-B1 D2	TC231DP	Upper	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02A-B1 D2	TC231DQ	Lower	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02A-B1 G2	TC231EA	Upper	1-2, 3-4, 5-6 7-8, 9-12	120ns	114ns	126ns
02A-B1 G2	TC231DK	Lower	1-2, 3-4, 5-6 7-8, 9-12	120ns	114ns	126ns
02A-B1 H2	TC232DM	Upper	1-2, 3-4, 5-6 7-8, 9-12	120ns	114ns	126ns
02A-B1 H2	TC232DN	Lower	1-2, 3-4, 5-6 7-8, 9-12	120ns	114ns	126ns
02A-B2 K6	CD021AX	Upper	1-2, 3-4, 5-8 9-12	100ns	95ns	105ns
02A-B2 K6	CD001BB	Lower	1-2, 3-12	50ns	47ns	53ns
02A-B3 L6	TA001BU	Upper	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02A-B3 L6	TA001AB	Lower	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02B-B1 K3	BC001BY	Upper	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02B-B2 L2	TP001BM	Upper	1-2, 3-4, 5-8 9-10, 11-12	See logic page TP001.		
02B-B2 L2	TP001AH	Lower	1-2, 3-4, 5-8 9-10, 11-12	See logic page TP001.		
02B-B2 K3	TP001BN	Lower	1-2, 3-4, 5-8 9-10, 11-12	See logic page TP001.		
02B-B2 K3	TP001BH	Upper	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02B-B2 K2	TP001BG	Upper	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02B-B2 K2	TP001BF	Lower	1-2, 3-4, 5-6 7-8, 9-10, 11-12	125ns	119ns	131ns
02B-B3 M3	ST031BA	Upper	1-12	See note on logic page ST031.		
02B-B2 K2	ST031AK	Lower	1-2, 3-4, 5-6	125ns	120ns	130ns
02B-B3 M6	ST031AF		(Fixed Delay)	700ns	665ns	735ns
02B-B3 H2	ST031	Upper*	1-2, 3-6, 7-12	70ns	65ns	75ns
02B-B3 H2	ST031	Lower*	1-12	See Character Generator		
01A-A2 H6	DC021	Upper	Fixed Delay	125ns	119ns	131ns
01A-A2 H6	DC021	Lower	Fixed Delay	350ns	333ns	367ns
01A-A2 J6	DC021	Upper	Fixed Delay	1000ns	950ns	1050ns
01A-A2 J6	DC021	Lower	Fixed Delay	900ns	855ns	945ns
01A-A2 G7	DC021	Upper**	1-2, 3-12	50ns	47ns	53ns
01A-A2 G7	DC021	Lower	1-2, 3-12	50ns	47ns	53ns

\*Adjust until beginnings and ends of character strokes are uniformly unblanked. This may be seen by viewing characters such as A, N, and H.

\*\*Adjust upper delay line at 01A-A2 G7 for 2.5usec  $\pm$  1% at 01A-A2G6D13. Make adjustment while running Diagnostic Program F757 or F767.

●Figure 4-7. Delay Lines



●Figure 4-8. Adjustable Delay Lines

1. Remove all power from 2250-1. Wait for completion of power-off sequence.
2. Remove two keepers.
3. Remove four external leads from TB1.
4. Remove catch for decorative panel.
5. Slide assembly out far enough to permit removal of ground strap.
6. Remove ground strap.
7. Disconnect 450v and 16kv output leads from rear of supply housing. (The +80v output is connected to the terminal strip.)

8. Remove supply.
9. Replace by reversing procedure.
10. Adjust catch for panel to make panel flush with bottom kickplate.

4.9 PRIMARY POWER ASSEMBLY REMOVAL

The primary power assembly (PN 5712333) is removed from the front of the 2250-1 as follows:

## DANGER

Line voltage is present in the primary power assembly with the Main Line switch off.

1. Remove all power from 2250-1.
2. Remove two assembly keepers.
3. Remove front decorative panel.
4. Slide assembly out far enough to permit removal of rear cover plate.
5. Remove rear cover plate.
6. Disconnect wires that prevent removal of assembly.
7. Remove primary power assembly.
8. Replace by reversing procedure.
9. Adjust three mounting screws to make front decorative panel flush with bottom kickplate.

### 4.10 24V POWER SUPPLY REMOVAL

The 24v power supply is housed in the primary power assembly (PN 5712333). See paragraph 4.9.

### 4.11 LOGIC GATE BLOWER REMOVAL

To prevent binding of fan blades, use caution when handling blowers; proceed as follows:

1. Remove blower housing cover.
2. Unplug blower lead.
3. Remove blower lead bracket.
4. Remove blower mounting screws.
5. Remove blower.
6. Replace by reversing procedure.
7. Check replacement blower for correct operation.

### 4.12 SLT POWER SUPPLY BLOWER REMOVAL

The SLT power supply blower, mounted behind the 3v and 12v power supplies (VR 5 and VR 6), is removed as follows:

1. Remove all power from 2250-1.
2. Remove -3v and +12v SLT power supplies (VR 5 and VR 6). (See paragraph 4.7.)
3. Disconnect blower lead.
4. Loosen left blower mounting screw.
5. Remove two right blower mounting screws.
6. Remove blower.
7. Replace by reversing procedure.
8. Check replacement blower for correct operation.

### 4.13 HIGH-VOLTAGE POWER SUPPLY BLOWER REMOVAL

On 2250-1's equipped with a high-voltage power supply blower, the blower is removed as follows:

## DANGER

The high-voltage power supply develops 16,000v, 450v, and 80v. Exercise extreme caution when working in the area of this voltage supply.

1. Remove all power from 2250-1.
2. Remove high-voltage power supply. (See paragraph 4.8.)
3. Disconnect blower lead.
4. Remove blower mounting screws.
5. Remove blowers.
6. Replace by reversing procedure.
7. Check replacement blower for correct operation.

### 4.14 RELAY PANEL REMOVAL

1. Remove all power from 2250-1.
2. Remove four keepers.
3. Slide relay panel assembly forward to gain access to three paddle connectors.
4. Disconnect paddle connectors.
5. Remove relay panel assembly.
6. Replace by reversing procedure.

### 4.15 OPTIC LIGHT PEN ADJUSTMENTS

The optic light pen is used when the graphic design feature is installed. The adjustments described in this section are applicable only to the optic light pen.

#### 4.15.1 Optic Focusing

Optical focusing of the fiber light pen can be accomplished by the following procedure:

1. Remove drive screw (PN 1091418) from pen assembly (Figure 4-9) and slide pen barrel (sleeve PN 5771510) off.
2. Loosen two setscrews (PN 74530) on boat (PN 5771514). Setscrews are located 90 degrees apart on boat.
3. Grasp the fiber cable assembly (PN 5771534) by the metal ferrule protruding from the rear of the light pen. Place the light pen halfway between the center of the CRT and the edge of the bezel. Gently slide the fiber cable assembly forward (towards CRT) or toward the rear (maximum travel is approximately 0.125 inch) until the images of the individual fibers (two aiming dots) are observed to be in focus when projected on the phosphor of the CRT. Move the pen to the center and corners of the CRT face to obtain the optimum setting. When optimum adjustment has been located, tighten the two setscrews on the boat.

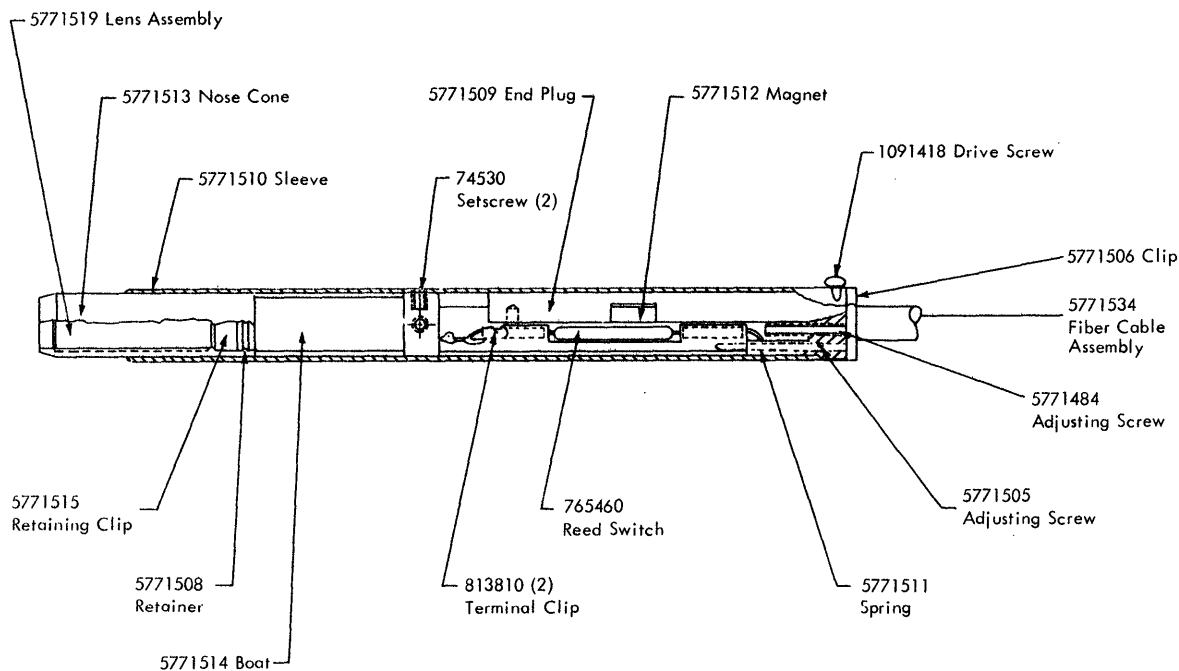


Figure 4-9. Optic Light Pen Assembly

4. To reassemble the pen, insert the pen assembly into sleeve (end of sleeve with small hole goes first). When sleeve has reached the shoulder of the end plug (PN 5771509), rotate sleeve until hole in sleeve lines up with a mating hold located in end plug.
5. Press drive screw (PN 1091418) into aligned holes.

#### 4.15.2 Switch Adjustment

To adjust the light pen switch closure, turn the adjusting screw (PN 5771484) so that when the end plug is pushed forward and the magnet (PN 5771512) causes a switch closure, there will be approximately 0.030 inch of overtravel (measured from the end of the adjusting screw to the stop).

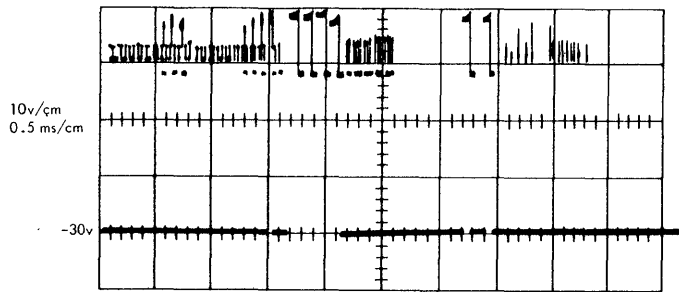
To adjust the pressure required to operate the pen assembly, turn adjusting screw (PN 5771505) until pen assembly restores properly when nose cone is depressed.

#### 4.16 INTENSITY ALIGNMENT PROCEDURE

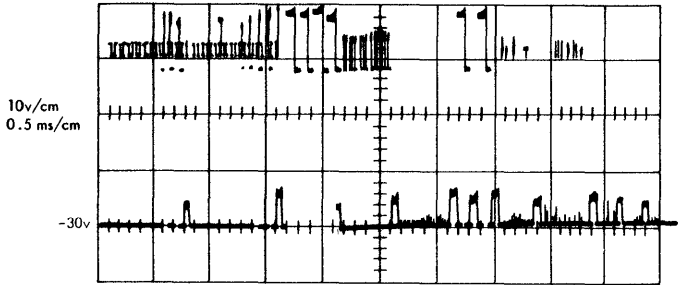
To obtain proper intensity alignment, perform the following steps:

1. Adjust all dc voltages to correct value (+36v, -36v, +3v, -3v, +6v).
2. Ensure vector and character damping is adjusted correctly by viewing the Analog General Alignment program (F766, pattern 1).

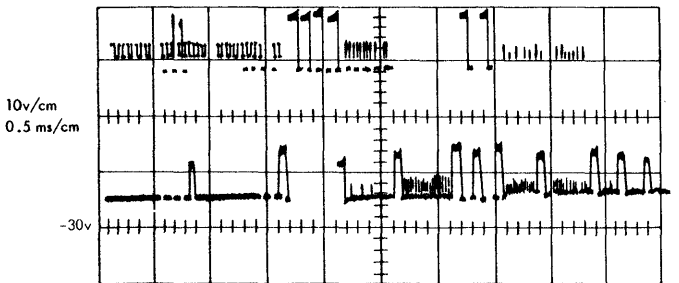
3. Remove caps (if used) from character contrast control and vector contrast control. (These controls are located directly behind operator's brightness control.)
4. Turn fully counterclockwise operator's brightness control, CE brightness limit control (screwdriver-adjustable potentiometer is recessed in front of operator's brightness control), and the two contrast controls.
5. Stop program, and reset machine.
6. With meter, adjust character-isolation card-mounted potentiometer at location 01BA2H2 for -0.5v in respect to +36v at 01BA2H2-D07.
7. With meter, adjust position-isolation card-mounted potentiometer at location 01BA2L6 for -0.5v in respect to +36v at 01BA2L6-D07.
8. Start program F766, Pattern 1.
9. With scope at 01BA2J6-B04, adjust card-mounted potentiometer at location 01BA2J6 until -30v level slowly goes positive. At this point, back potentiometer off approximately one turn. If -30v level "snaps" to the upper level (ground), potentiometer is adjusted incorrectly, and correct adjustment should be made. (See Figure 4-10.)
10. Turn operator's brightness control to maximum intensity (fully clockwise).
11. Turn CE brightness limit control (recessed potentiometer) clockwise until beginning of character strokes, short-length vectors, and point plots are adequately visible.



Card mounted potentiometer at location 01BA2J6 adjusted correctly. The -30v level is solid.



Card mounted potentiometer at location 01BA2J6 adjusted incorrectly. Portions of -30v level are starting to rise positive.



Card mounted potentiometer at location 01BA2J6 adjusted incorrectly. Entire -30v level is rising.

Note:  
The above drawings represent waveshapes using program F766, pattern one. Use internal sync positive on scope.

Figure 4-10. 01BA2J6 Card Output Levels

12. If beginnings of vectors are not being intensified at an adequate level of brightness, adjust single-shot located at 02BB1K2-D13 middle (machines without AVG feature) or 02BB1M6 upper (machines with AVG feature) until vector beginnings are present.

13. If beginnings of character strokes are not being intensified at an adequate level of brightness, add more delay at location 02BB3H2 (total available 250ns). If pile-up is present at beginnings of character strokes, remove some delay from location 02BB3H2. This is a visual adjustment and, as such, may have to be done several times until optimum results are obtained. (See step 14.)

NOTE: The character generator feature switch should be turned off when removing this delay line from its socket. It is not necessary to turn down dc power.

14. If too much end-point pile-up is present on character strokes, add more delay in location 02BB3M3 upper (total available 125ns). If character end points are not adequately intensified, use less delay in location 02BB3M3 upper. As this adjustment will also influence the beginning of character strokes, it should be made in conjunction with step 13.

NOTE: The character generator feature switch should be turned off when removing this delay line from its socket. It is not necessary to turn down dc power.

15. A slight increase in dynamic intensity may be desired to obtain more uniform intensity. If so, adjust appropriate contrast control (vector or character). The normal setting of these controls is fully counterclockwise or, at the most, approximately 1/3 clockwise rotation.

16. With adjustments completed, if potentiometer caps are used (step 3), replace caps on contrast controls, and tighten.



The information in this chapter will aid in adjusting, repairing, and diagnosing failures on the power supplies used in the 2250-1.

5.1 GENERAL

The following power supplies are used in the 2250-1:

- 6v at 20 amp  $\pm$  2%, series-regulated
- 3v at 26 amp  $\pm$  2%, series-regulated
- 3v at 8 amp  $\pm$  2%, series-regulated
- 12v at 2 amp  $\pm$  20%, series-regulated
- 36v at 4.5 amp  $\pm$  2%, series-regulated (two used)
- 16kv at 0.2ma  $\pm$  500v
- 450v at 0.4ma  $\pm$  15v, high-voltage supply
- 80v at 15ma  $\pm$  3v
- 24v at 1 amp  $\pm$  10%
- 6.3vac at 0.6 amp, unregulated
- 40vac at 0.25 amp, unregulated

5.2 POWER SUPPLY PROTECTION

All of the power supplies except the 24v supply are individually protected by magnetic circuit breakers that operate when the current load on a supply exceeds a safe level. A tripped circuit breaker (SLT supply) causes the CB TRIP indicator on the power panel to glow. The SLT supplies have both over-voltage and overcurrent protection circuits. The 24v supply is protected by a fuse on each input leg. Wired in parallel with each fuse is a neon lamp that glows when its associated fuse is blown (LINE BREAKER on the primary power panel must be turned off before 24v supply fuses are replaced).

The power system is further protected by a circuit breaker on the input leg of the bulk transformer, which, when operated, removes input voltage from power supply blower PS2 and all the supplies except the 24v supply. The entire power system, including the 24v supply and all blowers, is protected by a circuit breaker (CB1) at the primary power input. The power system is also protected from overheat by a thermal switch (paragraph 5.3).

5.3 POWER COOLING

The 2250-1 power system is air-cooled by means of a blower (two blowers on earlier machine) mounted at the bottom of the power frame. The blower aids in dissipating heat by circulating room-temperature air past the power supply heat sinks.

Detection of an overtemperature condition in the power system is provided by a thermal sensing switch. If operating temperatures exceed a safe

level (because of a blower failure or another cause), the switch opens, power is cycled down, and the THERMAL ALARM indicator on the power control panel lights.

5.4 THERMAL RESET

Once a thermal condition occurs, a Power On status can only be attained following a cooling period that allows the thermal switch to close. The length of time required for the switch to close depends on the environmental conditions but should normally not exceed 30 minutes. The cooling period can be shortened by removing the machine covers and opening the machine to permit faster heat dissipation.

Before an attempt is made to restore power, the cause for the condition must be fully investigated. Figure 5-1 lists some of the possible causes of overheating; the figure indicates the causes to check for during the Power Off status and the causes best checked during the Power On status.

Power can be restored in two ways, both of which depend on the thermal switch being closed:

1. Depress THERMAL RESET switch. Power will be restored if the following switches

Possible Cause	Check With	
	Power Off	Power On
Clogged filter: paper, rag, card, dirt, etc. blocking passage of air.	x	
Binding blower. Bind in blower can be felt by manually turning blade. Use screwdriver, pencil, etc. to rotate fan.	x	
Intermittent binding blower. Observe suspected blower operating. Check for variations in speed or intermittent start-stop.		x
Defective blower. Observe with power on.		x
Overheating component. Check suspected component for signs of overheating: discoloration, smoking, etc.	x	x
Defective thermal switch. Open switch can be checked with meter.	x	
Intermittent failing switch can be monitored with power on, using meter or scope.		x
Environment temperatures. Check room temperature. See Appendix B for operating temperature range.	x	x

Figure 5-1. Possible Causes of Thermal Conditions

have not been operated since the thermal condition occurred:

- 2250 ON/OFF
- LOCAL/REMOTE
- System POWER ON/OFF
- EMERGENCY POWER OFF (System)

2. Restore power in the normal manner. If any of the switches in step 1 have been operated since the thermal condition occurred, CONTROL K1 and other control relays will have been dropped, rendering the THERMAL RESET switch ineffective.

### 5.5 VOLTAGE CHECKS AND ADJUSTMENTS (SLT SUPPLIES)

The outputs of the individual SLT power supplies (+3, -3, +6, +12, +36, and -36) must be measured at TB1 in gate 01B. The output of each supply is adjusted by means of a potentiometer located on the dc module of each supply:

1. Loosen lock nut that holds potentiometer in position.
2. Slowly vary potentiometer while monitoring output of supply (laminar bus 01B) with reliable dc voltmeter.
3. When desired output is obtained, carefully tighten lock nut.
4. Check output after tightening to be sure no change occurred during tightening.

If the correct output cannot be obtained by varying the potentiometer, refer to paragraph 5.6.

The voltage at any large board should be within  $\pm 2\%$  of the voltage at TB1 in gate 01B.

### 5.6 POWER SUPPLY FAILURES

Failures in the power area can cause varied and misleading symptoms. Only a few of the failures can be immediately traced to the power system.

For power failure symptoms, proceed with the recommended approaches (paragraphs 5.6.1 through 5.6.4) for localizing the failures.

#### 5.6.1 Loss of Power

If loss of power is due to a thermal condition (THERMAL ALARM indicator on), refer to paragraph 5.4 and to Figure 5-1.

If loss of power is due to a tripped circuit breaker (CB TRIP indicator on), determine which power supply is failing, reset circuit breaker, and proceed in accordance with paragraph 5.6.1.1 or 5.6.1.2.

#### 5.6.1.1 Inability to Restore Power Following CB Trip

If power cannot be restored and the failing supply is determined, replace the regulating cards associated with the failing supply. It is advisable to replace the cards one at a time, attempting to restore power after each replacement. If unsuccessful, replace all the cards in the supply. If power still cannot be restored, replace supply with a spare, if available, and repair failing supply (paragraph 5.7).

#### DANGER

Field repairs to high-voltage supply are limited to card replacement.

#### 5.6.1.2 Ability to Restore Power Following CB Trip

If power can be restored, check the output of the failing supply, and adjust if necessary. If unable to adjust, proceed as follows:

1. Check input voltage to supply. Figure 5-2 lists the correct input voltages to the SLT supplies.

Power Supply	Input Voltage
3v at 8 amp	7.5v 4% ripple
3v at 26 amp	7.5v 4% ripple
6v at 20 amp	11.5v 4% ripple
12v at 2 amp	17.2v 4% ripple
36v at 4.5 amp	50v 4% ripple
36v at 4.5 amp	50v 4% ripple

Figure 5-2. Input Voltages to SLT Supplies

2. Replace regulating cards associated with failing supply. Replace cards one at a time, attempting to adjust voltage with each replacement. If unsuccessful, replace all the cards in the failing supply.
3. If still unsuccessful, replace supply with a spare, if available, and repair failing supply (paragraph 5.7).

#### DANGER

Field repairs to the high-voltage supply are limited to card replacement.

#### 5.6.1.3 Causes of Power Loss

Figure 5-3 lists some of the possible causes of power loss other than those discussed in paragraphs 5.6.1.1 and 5.6.1.2.

Cause	Area
Power supply failure	See paragraph 5.6.1.
Burned or corroded control relay points	Control relays
Insufficient tension or rise on control relays	Control relays
Loose points on control relays	Control relays
Open relay coil	Control relays
Open or loose wire or cable	Control relays power system
Defective power supply circuit breaker	Power system
Input voltage fluctuations	Primary power
Unit or system Power On switch	System CPU, 2250
Emergency Power Off switch	System CPU
LOCAL/REMOTE switch	2250
Loss of 24v supply	Power system

Figure 5-3. Causes of Power Loss

#### 5.6.2 Display Raster Changing Size

If the display raster is decreasing in size or blooming, check the output of the high-voltage supply (paragraph 5.8).

#### 5.6.3 Loss of Display/Distorted Image

Loss of display and distorted images can be caused by a failing power supply. The voltage level should be within  $\pm 2\%$  of specified value, and line noise should be within a  $\pm 2\%$  tolerance. When either condition occurs and power is suspected, monitor the power supplies, and correct the failing supply.

#### 5.6.4 Machine Hangup/Error Conditions in Status Byte

Error conditions in the status byte and machine hangups can be caused by power fluctuations, by momentary power loss, or by an incorrect power supply output.

When power failure is suspected as the cause, the power supplies should be monitored (while diag-

nostic programs are being run), and the failing power supply should be isolated and repaired.

#### 5.7 SLT POWER SUPPLY REPAIR

Field repair of SLT power supplies is limited to replacing control and regulating cards and to replacing defective transistors and resistors on the power supply heat sink. Power supplies that require further repair should be replaced.

#### 5.8 HIGH-VOLTAGE SUPPLY OUTPUT

The +16kv output is active when the HIGH VOLTAGE ON neon indicator is lit.

**DANGER**  
Do not measure the +16kv output.

#### 5.9 HIGH-VOLTAGE POWER SUPPLY REPAIR

**DANGER**  
Power must be off and extreme caution must be exercised while working in this area. Field repair of the high-voltage supply is limited to the unenclosed area of the supply. If trouble is traced to the enclosed area, replace the entire 16kv power supply.

#### 5.10 POWER DISTRIBUTION

Figure 5-4 shows the ac and dc voltage distribution for the 2250-1.

#### 5.11 POWER-ON SEQUENCE

Figure 5-5 is a flow chart of the power-on sequence.

#### 5.12 POWER-OFF SEQUENCE

Figure 5-6 is a flow chart of the power-off sequence.

#### 5.13 +36V, -36V MINIBUS ROUTING

Distribution of the +36v and -36v is shown in Figure 5-7. Each minibus is connected to the laminar bus of the indicated polarity.

#### 5.14 POWER CONTROL AND DISTRIBUTION WIRING DIAGRAM

FEDM Figure 9003 is a power control and distribution wiring diagram.

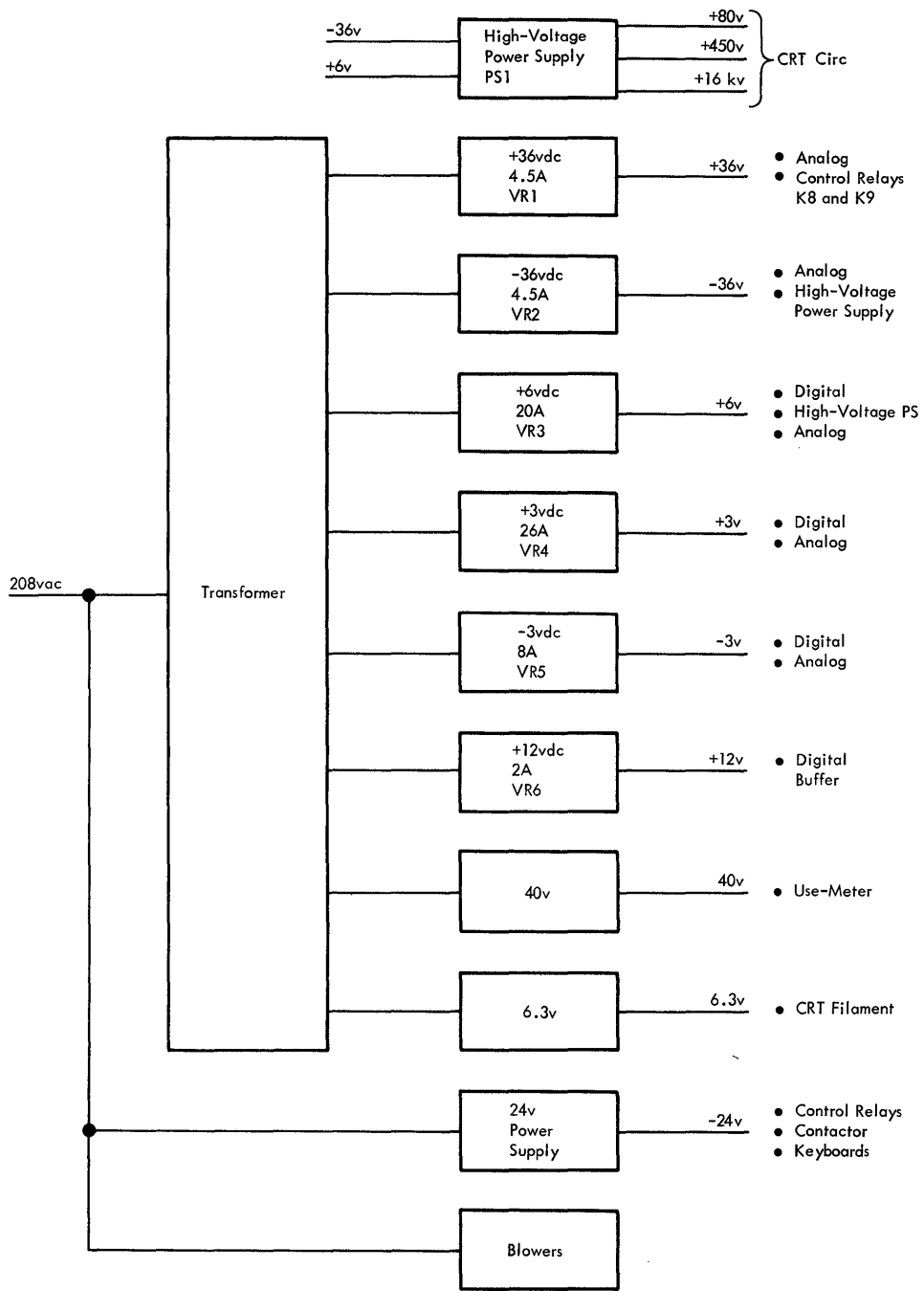


Figure 5-4. AC/DC Voltage Distribution

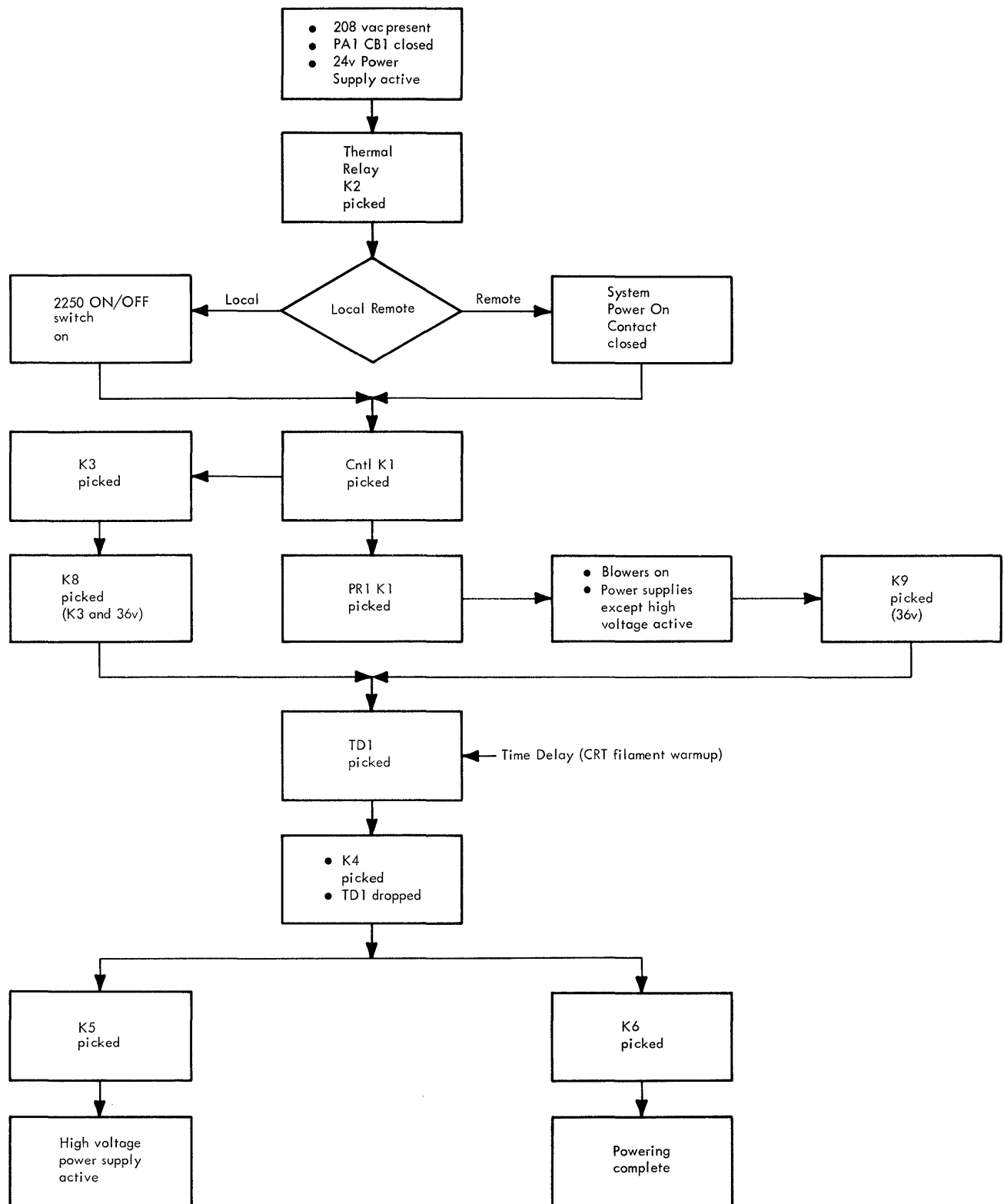


Figure 5-5. Power-On Sequence

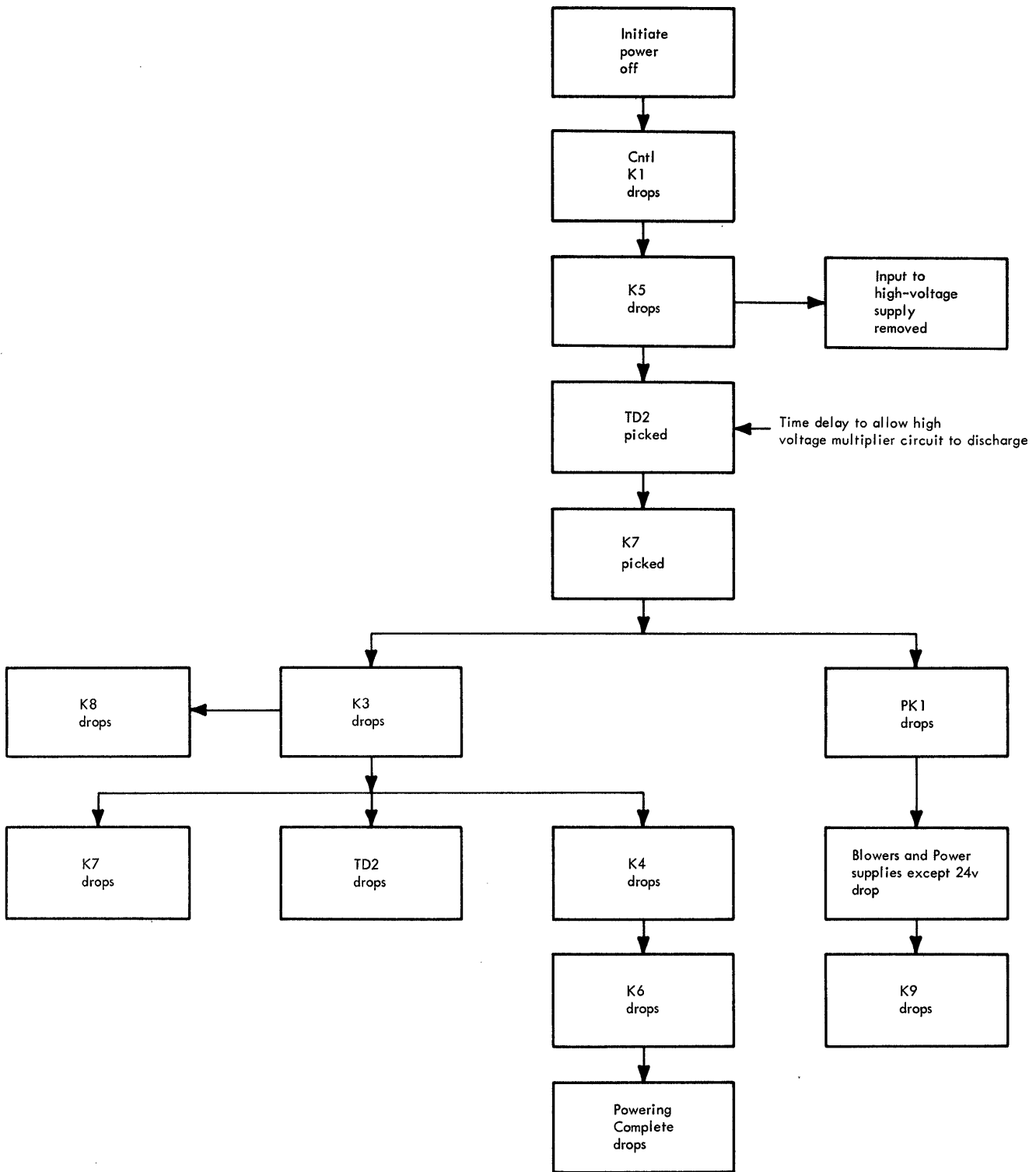


Figure 5-6. Power-Off Sequence

01BA3 (Card Side)

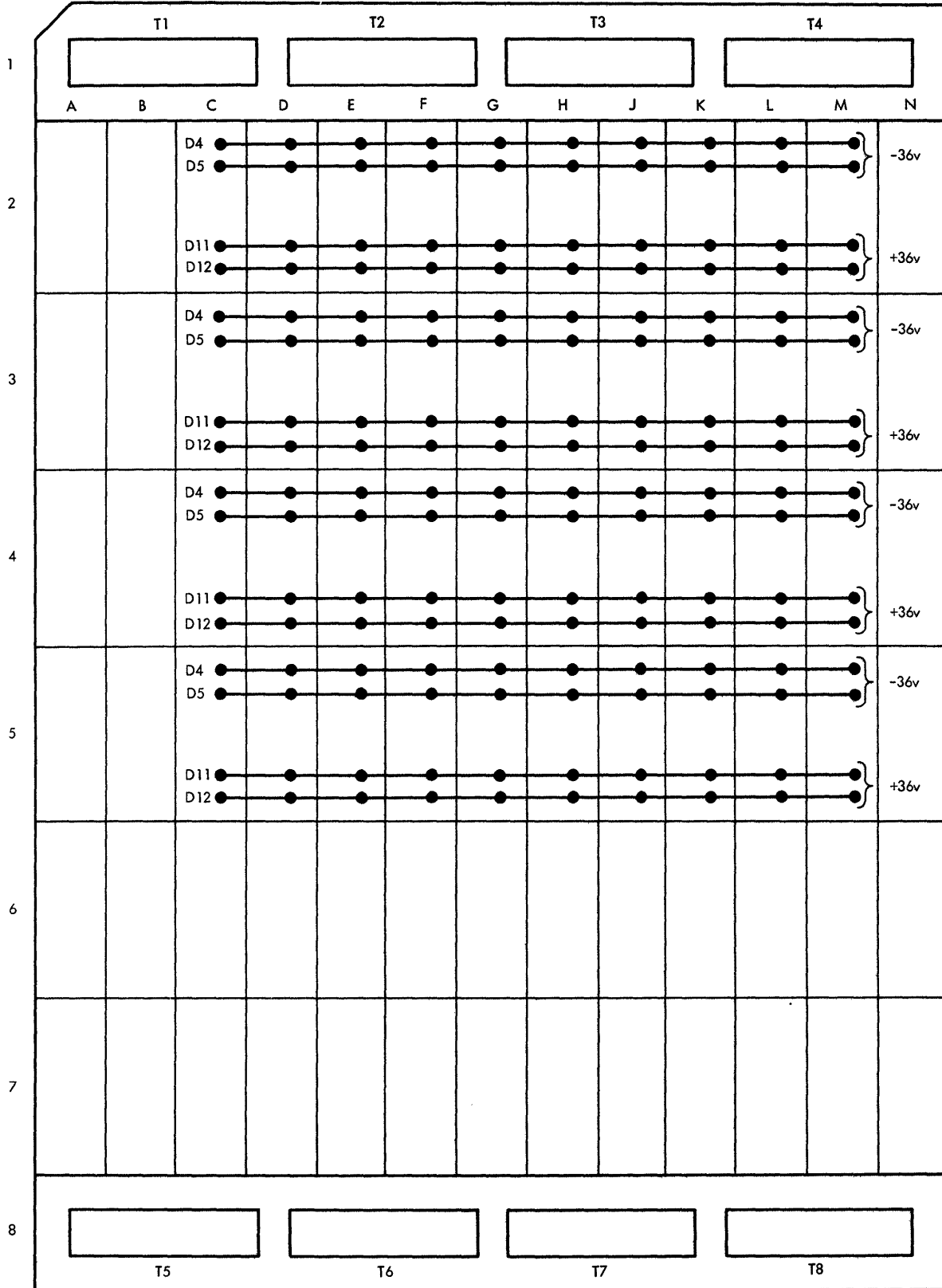


Figure 5-7. +36V, -36V Minibus Routing (Sheet 1 of 3)

01BA2 (Card Side)

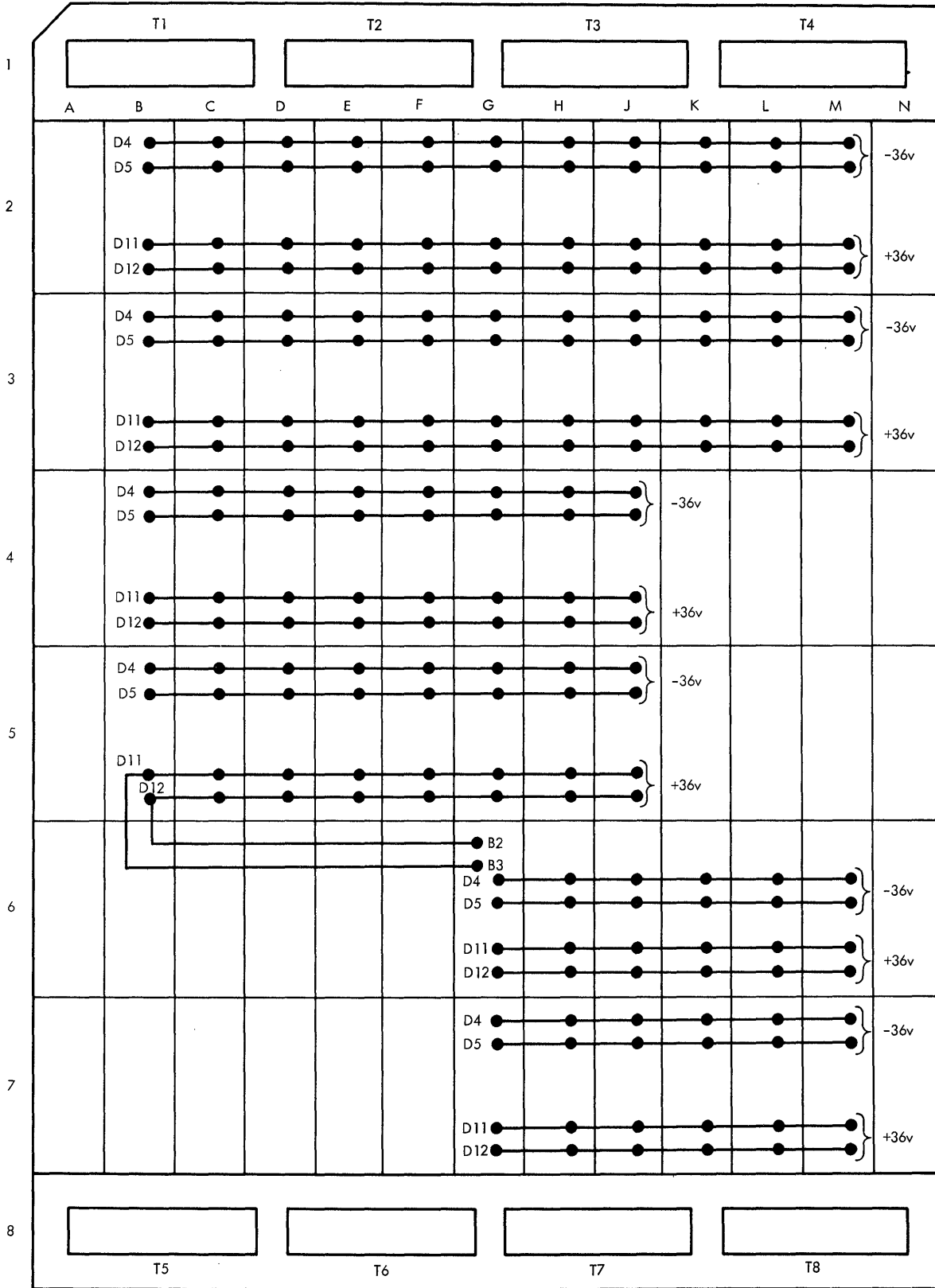


Figure 5-7. +36V, -36V Minibus Routing (Sheet 2 of 3)



01AA2 (Card Side)

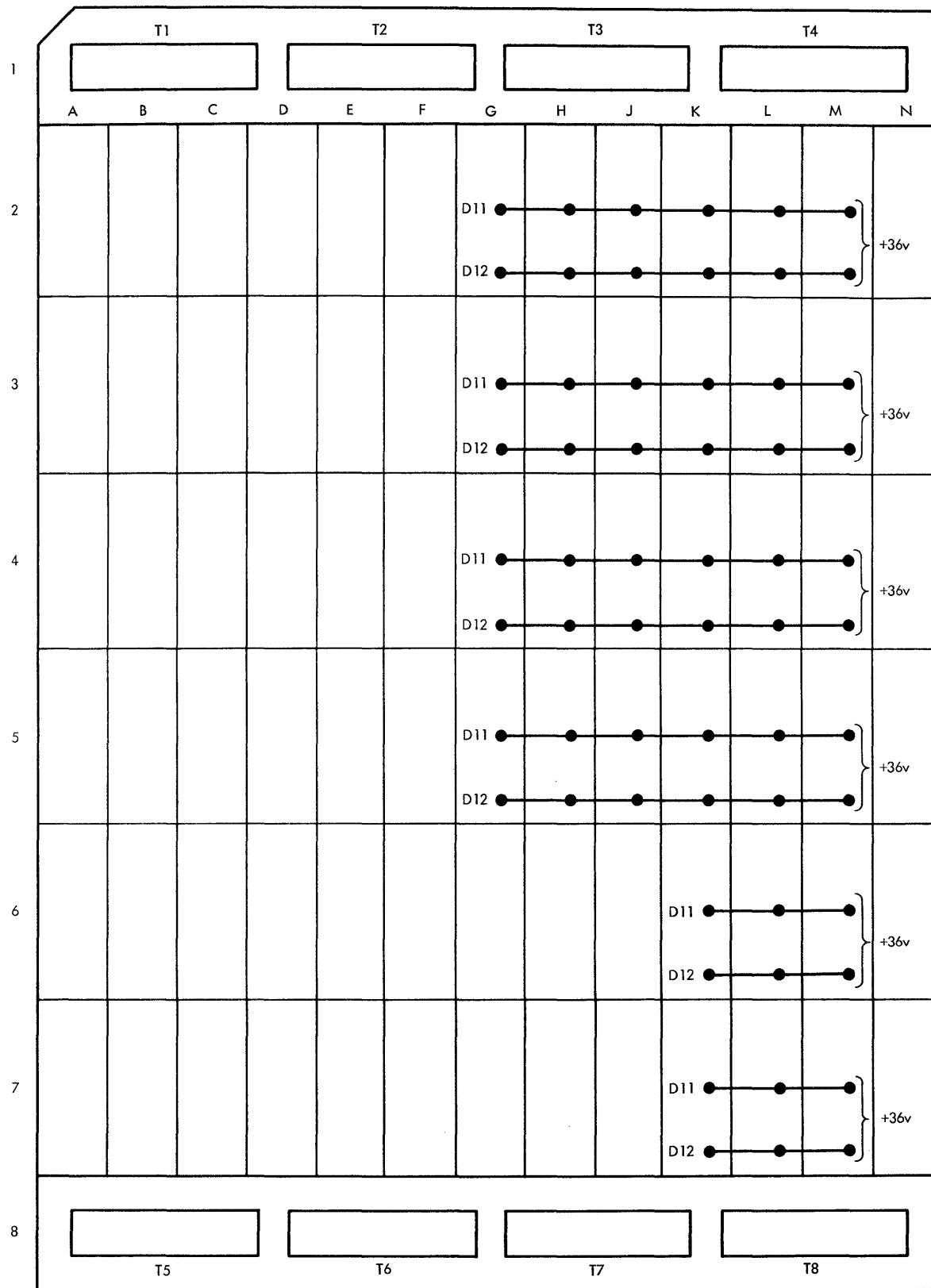


Figure 5-7. +36V, -36V Minibus Routing (Sheet 3 of 3)

This chapter will familiarize the CE with the component location coding of the 2250-1 and help him to locate a particular area or part within the machine.

To facilitate locating areas and parts of the 2250-1, the machine is sectionalized as follows: frame 01 contains the CRT, power supplies, and attached SLT gates; frame 02 contains the operator control unit, the I/O panel, and SLT gates. These frames are further divided into sections and coded alphabetically, as follows:

1. Frame 01
  - 01A SLT logic gate
  - 01B SLT logic gate
  - 01C Power supplies
  - 01D CRT
  - 01E Console reading board, controls and components attached (keyboards, Power On/Off, etc.).
2. Frame 02
  - 02A SLT logic gate
  - 02B SLT logic gate
  - 02C CE panel

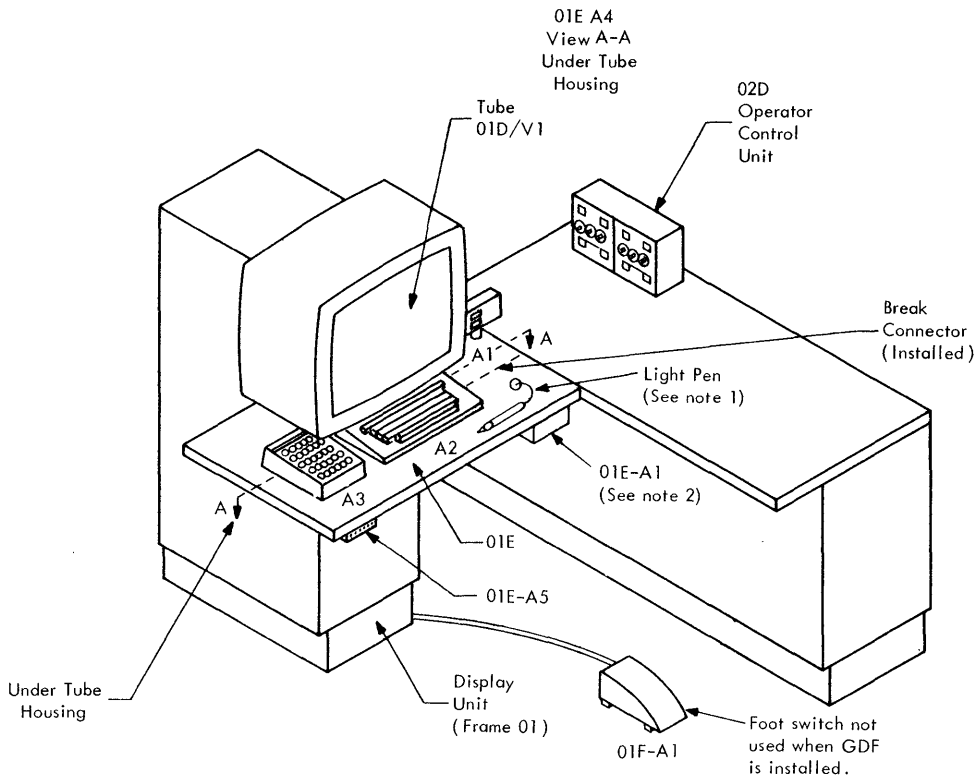
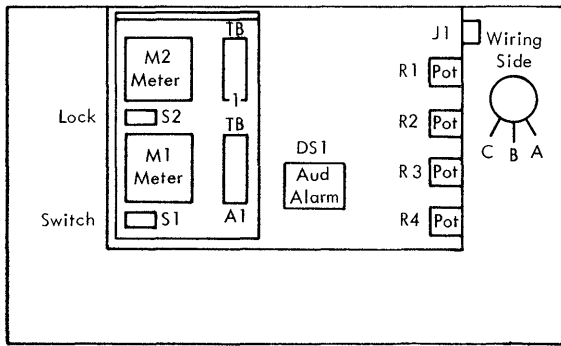
02D Operator control unit

02S Rear panel of frame 02, including I/O panel.

The three-position code (01A, 02A, etc.) prefixes a location designation and directs the CE to the correct frame and area within it. To define a part or component further, the initial, the number symbol, or a combination of these follows the frame and section designation. For example, 01A/TB1-4 refers to Post 4 of Terminal Block 1, located in Section A of Frame 01.

Figures 6-1, 6-2, and 6-3 illustrate the component location coding and identify the major areas by code. Also identified are parts, terminals, etc. within the major areas.

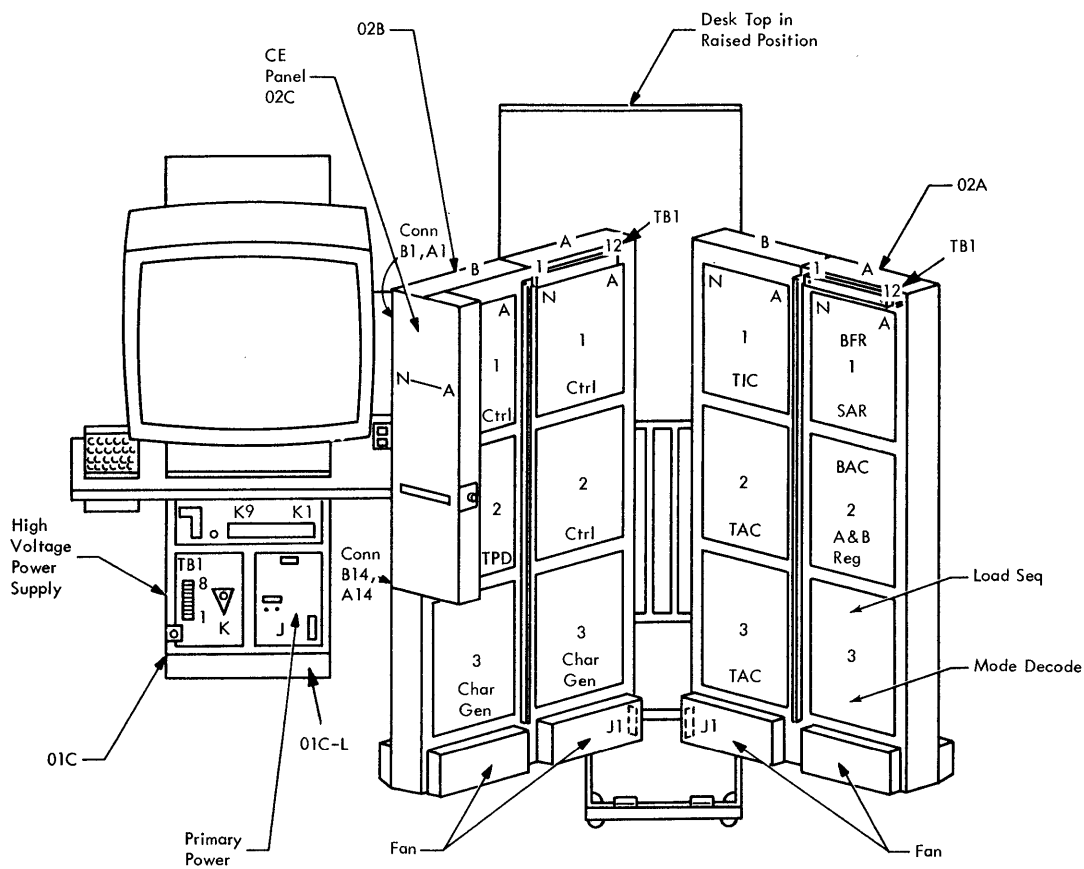
Figure 6-4 is a front view of the lower portion of frame 01 (01C). It shows in detail the relay panel, the high-voltage power supply, and the primary power assembly. Figure 6-5 is a rear view of the lower portion of frame 01 (01C). It shows in detail the power pack assembly, the location of the SLT power supply blower, and the locations of the SLT power supplies.



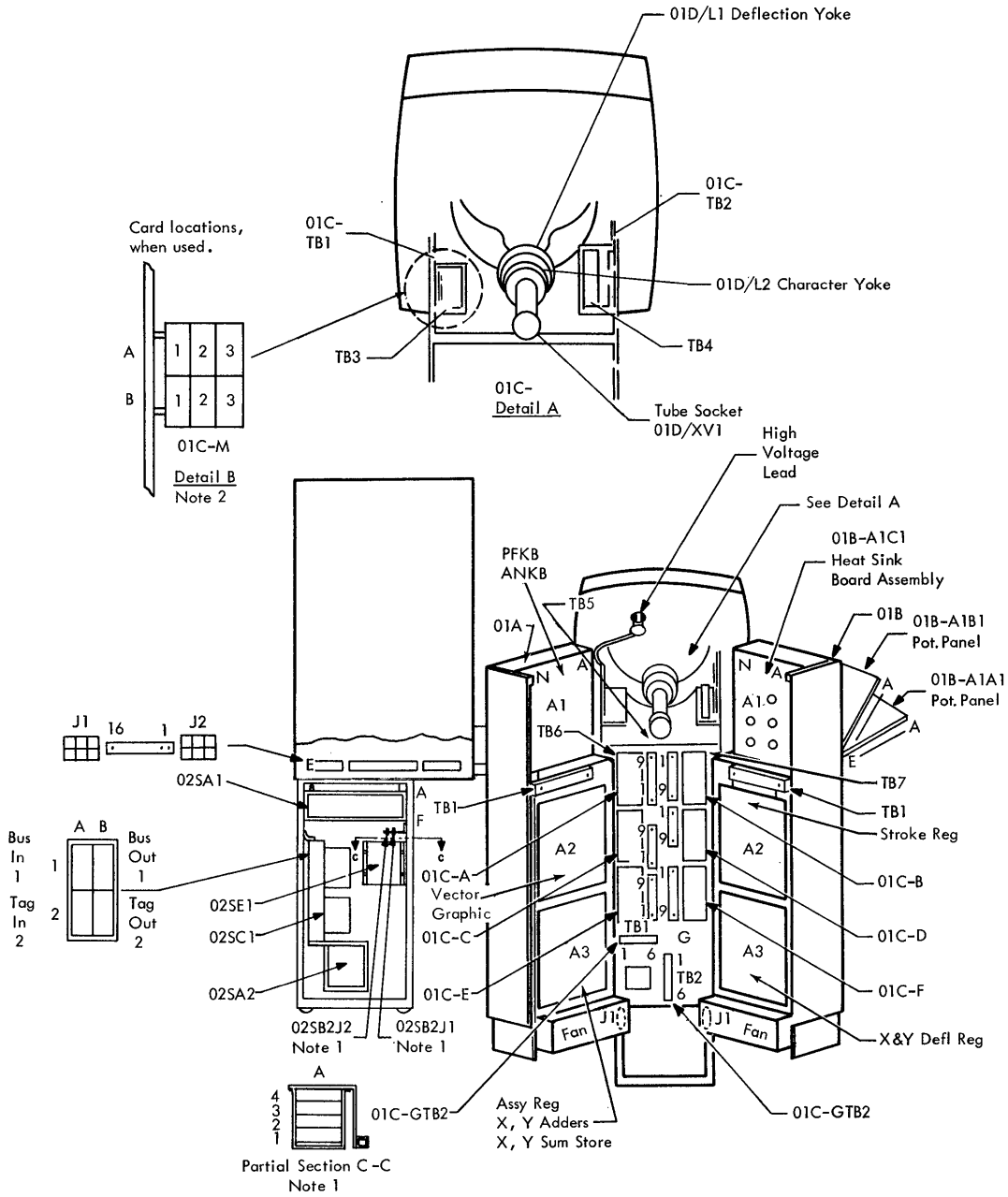
Notes:

1. Optic light pen shown is used when GDF is installed. When GDF is not installed, light pen plugs into jack J1 (shown in view A-A)
2. Light pen amplifier card is located at 01E-A1 when GDF is installed.

Figure 6-1. Component Location, Operational



●Figure 6-2. Component Location, Front View



Notes:

1. Coding 02SB2 and 02SE1 applies only when operator control panel feature is used.
2. Use coding as shown in Detail B if circuitry is packaged on SMS card; otherwise, use as shown in Detail A.

●Figure 6-3. Component Location, Rear View

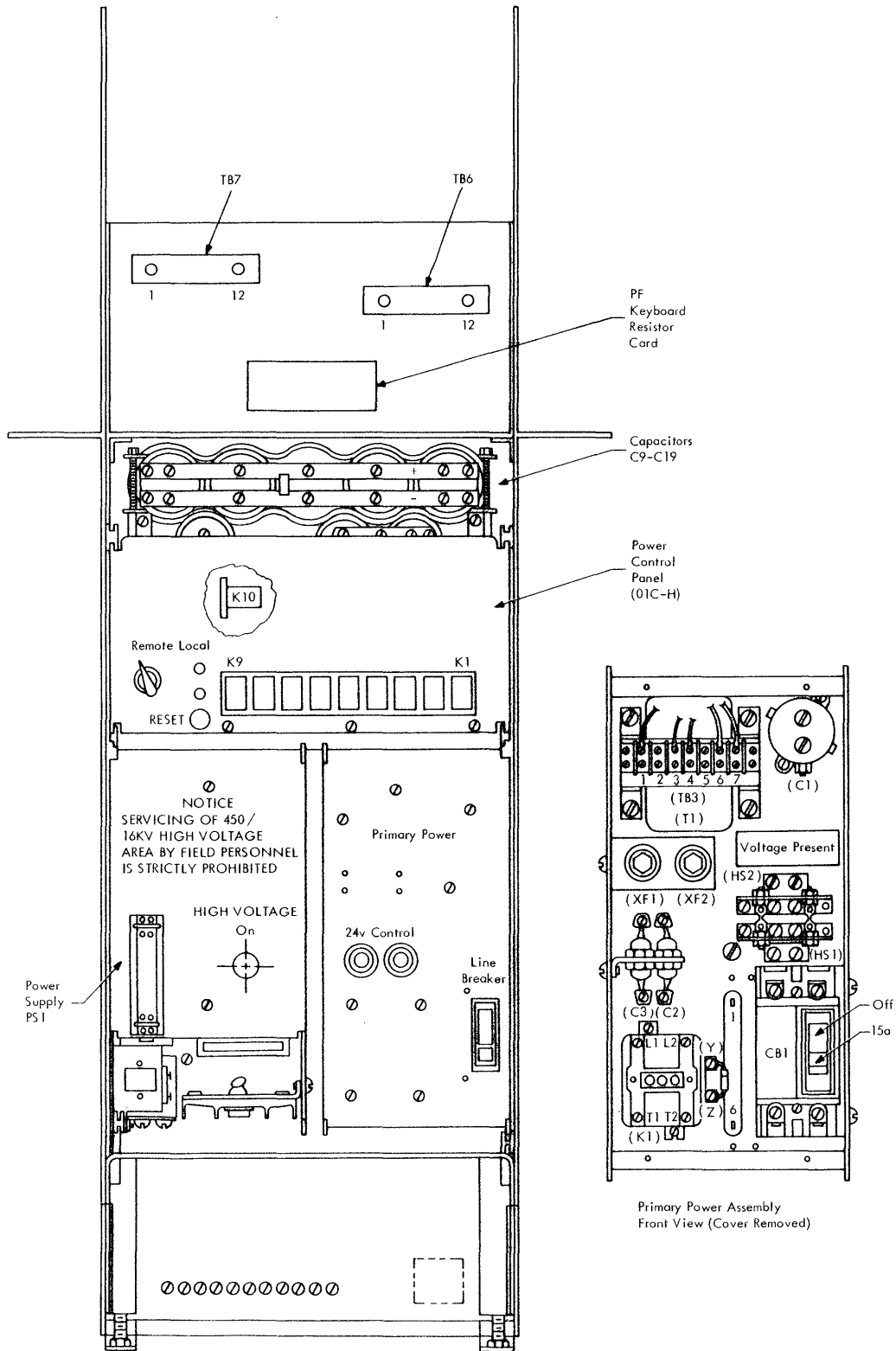


Figure 6-4. Detail 01C, Front View

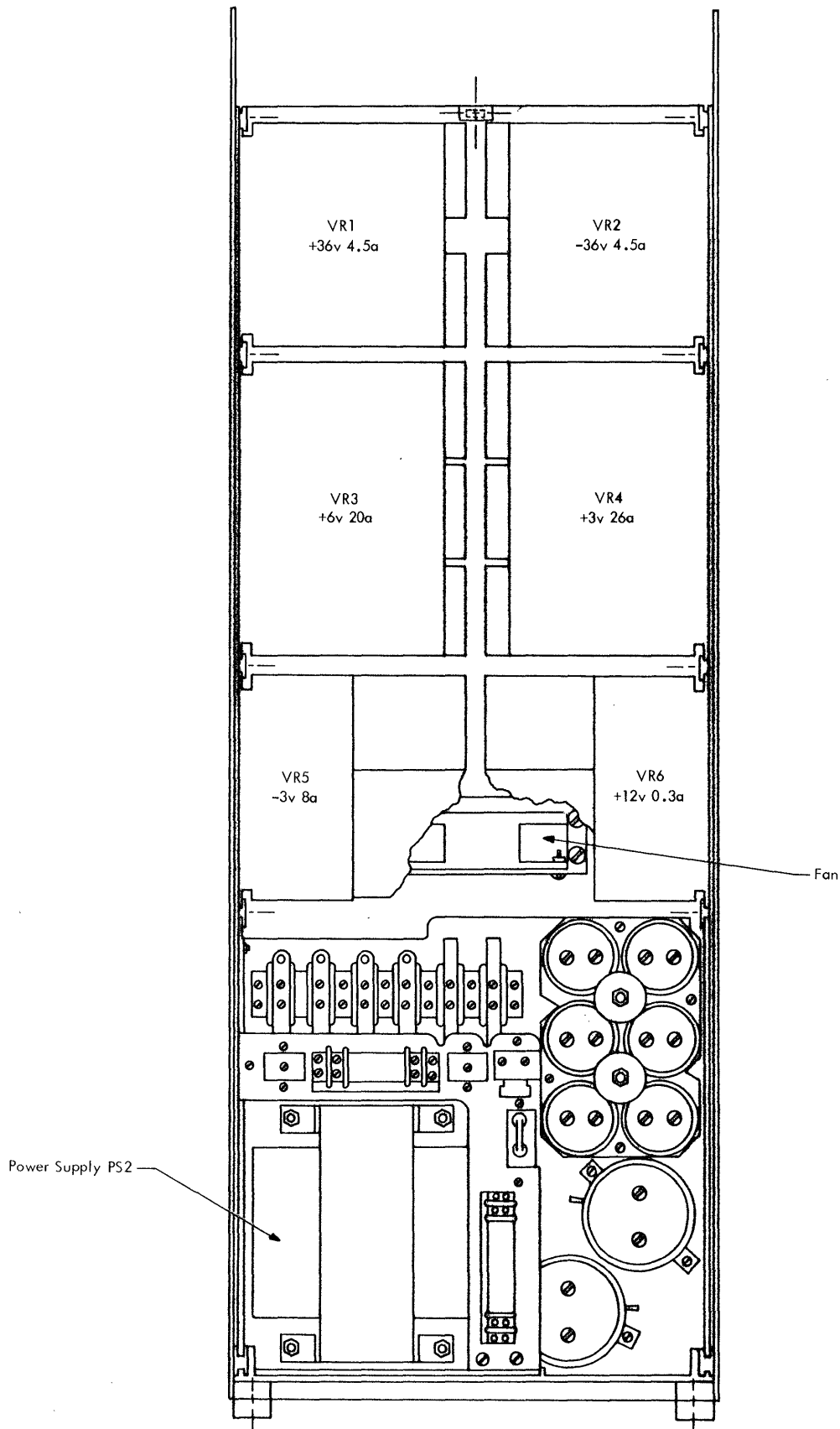


Figure 6-5. Detail 01C, Rear View

APPENDIX A. TOOLS, TEST EQUIPMENT, AND SAFETY EQUIPMENT

This appendix lists the tools, test equipment, and safety equipment required to maintain and repair the 2250-1.

A.1 TOOLS

- 7-inch long-nose pliers
- 6-inch needle-nose pliers
- 6-inch needle-nose diagonal cutters
- 4-1/2-inch needle-point diagonal cutters
- Wire strippers (such as Miller Model 101S)
- 6-inch screwdriver
- 10-inch screwdriver
- Jeweler's screwdriver
- Nut driver set
- Crimping tool
- GE soldering iron with transformer
- Solder sucker
- Electric wire-wrap gun with No. 30 bit
- Delete tool
- Wire stripper (such as that of General Cement Mfg. Co.)
- Stepdown transformer (110vac to 22vac)

- SLT pin straightener
- SLT single- and double-card puller
- Grounding strap (high-voltage)

A.2 TEST EQUIPMENT

- Tektronix, 545 or 585 oscilloscope with Main Sweep Delayed feature
- Scope cart
- 10X probe (2)
- Type CA plug-in unit (dual-trace)
- Type D plug-in unit (high-gain)
- SLT probe tips (2)
- Simpson Model 270 VOM W/leads
- SLT portable marginal check supply

A.3 SAFETY EQUIPMENT

- Welder's gloves
- Full-face shield
- Synthetic rubber apron
- Welder's rawhide cape
- Protective CRT neck cap



APPENDIX B. 2250-1 CHARACTERISTICS

This appendix specifies the physical dimensions, power requirements, and other characteristics of the 2250-1.

Display Area

12" x 12" (1024 x 1024 raster units)

Speed

Minimum time required for one deflection -  
16.8 usec

CRT Persistence

30ms

Dimensions

	<u>Width</u>	<u>Height</u>	<u>Depth</u>
Frame 01	36"	50"	44"
Frame 02	22"	29"	50"

Weight

Frame 01                    528 pounds  
Frame 02                    366 pounds  
Combined weight:        894 pounds

Primary Power Requirements

60-cycle, single-phase, at 208vac or 230vac  
50-cycle, single-phase, at 195vac, 220vac, or  
235vac

Power Dissipation

2.8kva

Heat Dissipation

7200 btu/hr  
480 cfm

Cooling

Forced room-temperature air

Operating Environment

Temperature: 60° F to 90° F  
Relative Humidity: 8 to 80%  
Wet Bulb: 78° F

Nonoperating Environment

Temperature: 50° F to 110° F  
Relative Humidity: 8 to 80%  
Wet Bulb: 85° F

Connections

Plug: R & S FS3720  
Connector: R & S FS3913

Features

1. Buffer (4K or 8K)  
4K - 4096 positions of core storage.  
8K - 8192 positions of core storage.
2. Character generator
3. Alphameric keyboard
4. Program function keyboard
5. Light pen detection
6. Operator's control panel (Model 50 and above)
7. Absolute vector graphics
8. Graphic design
9. Isolation

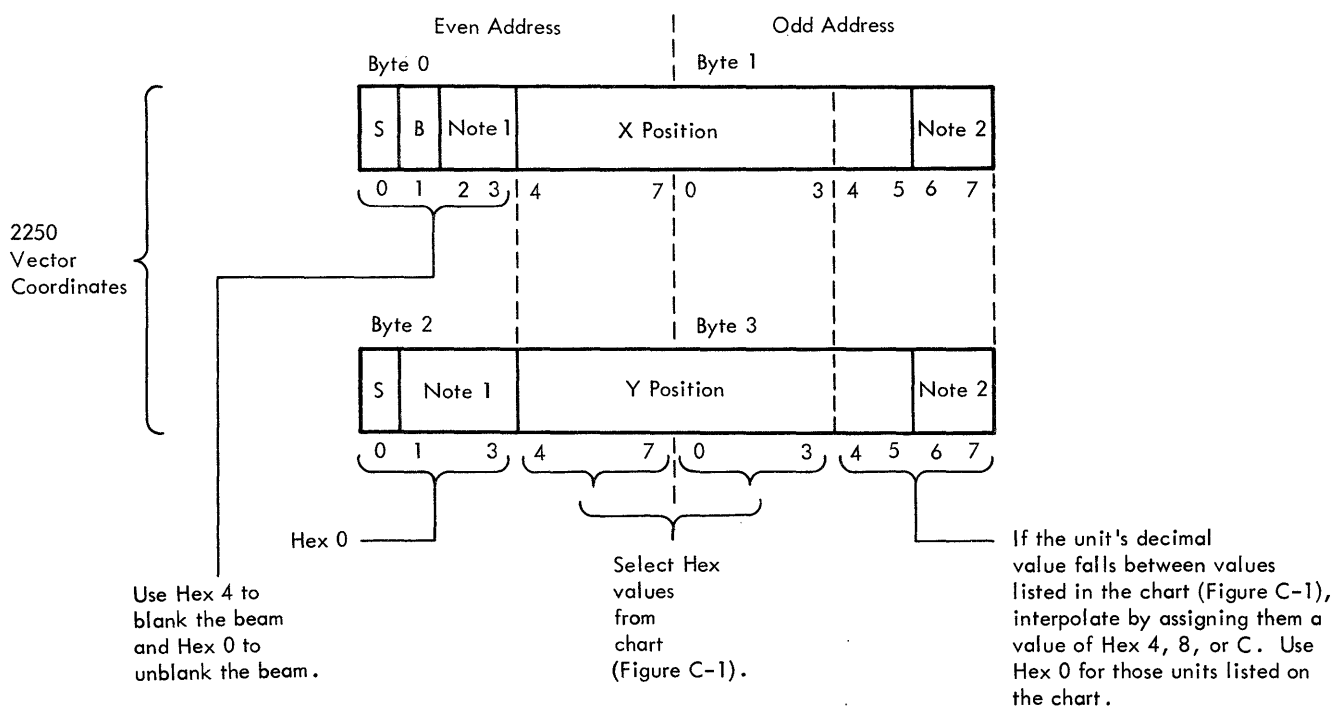
Internal 2250-1 Resistance on Channel Interface Lines

Select In/Select Out Line	1.50 ohms
All other lines	0.10 ohm

This appendix contains conversion charts that will aid in determining X and Y vector coordinates for the 2250 Display Unit.

C.1 FOUR-BYTE ABSOLUTE VECTOR CONVERSION

The intersection of the hundreds column and the units row (Figure C-1) gives the high-order hexadecimal values of the X and Y positions as indicated below. The low-order hexadecimal value must be interpolated as indicated.



- Notes:
1. These bits must be the same as the sign (S) bit.
  2. These bits are not presently used; however, 12-bit accuracy should be used so that programming will not be necessary when operating with the IBM 2280 or IBM 2282 film units.

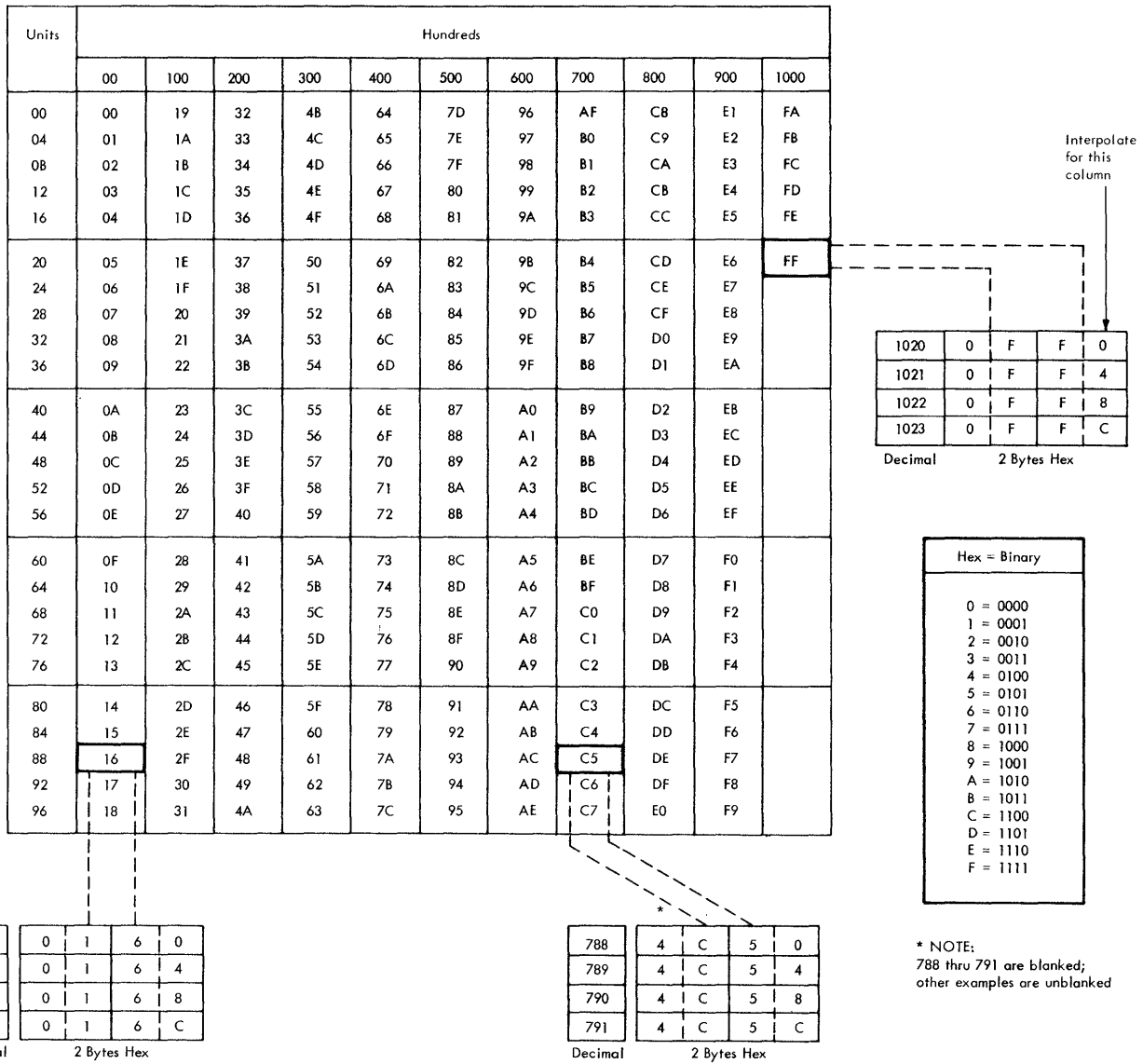
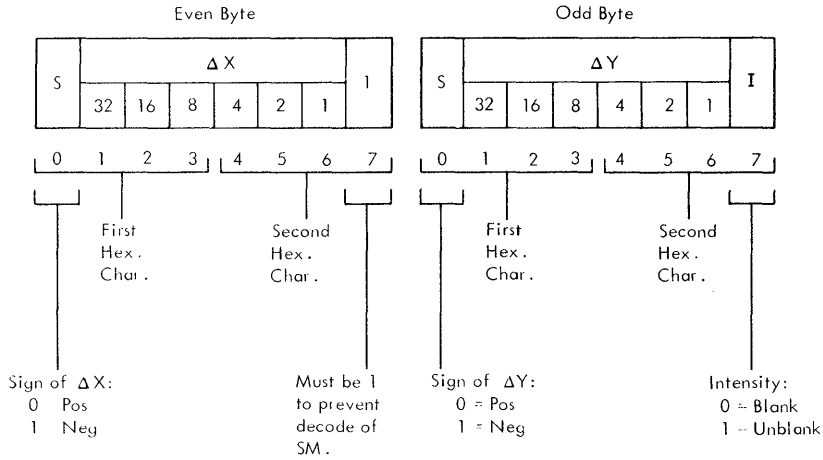


Figure C-1. Decimal-Hexadecimal Conversion Chart for Four-Byte Absolute Vectors

## C.2 TWO-BYTE RELATIVE VECTOR CONVERSION

The following is the structure of the buffer address for a relative vector ( $\Delta X$ -  $\Delta Y$ ) coordinate:



A direct conversion chart for determining the hexadecimal code from number of raster units is contained on Figure C-2. To use this chart, locate number of raster units desired for the  $\Delta X$  coordinate. The Hex code can be determined by dropping a vertical line to intersect the First Hex Character Row and then a horizontal line to intersect the appropriate Second Hex Character column. (Refer to note 1, Figure C-2.) Repeat procedure for the  $\Delta Y$  coordinate using the correct Second Hex Character column according to note 2 of Figure C-2.

Second Hex. Char. of Byte		Number of Raster Units															
Unblank	Blank																
E	F	-57	-49	-41	-33	-25	-17	-9	-1	+7	+15	+23	+31	+39	+47	+55	+63
C	D	-58	-50	-42	-34	-26	-18	-10	-2	+6	+14	+22	+30	+38	+46	+54	+62
A	B	-59	-51	-43	-35	-27	-19	-11	-3	+5	+13	+21	+29	+37	+45	+53	+61
8	9	-60	-52	-44	-36	-28	-20	-12	-4	+4	+12	+20	+28	+36	+44	+52	+60
6	7	-61	-53	-45	-37	-29	-21	-13	-5	+3	+11	+19	+27	+35	+43	+51	+59
4	5	-62	-54	-46	-38	-30	-22	-14	-6	+2	+10	+18	+26	+34	+42	+50	+58
2	3	-63	-55	-47	-39	-31	-23	-15	-7	+1	+9	+17	+25	+33	+41	+49	+57
0	1	-64	-56	-48	-40	-32	-24	-16	-8	+0	+8	+16	+24	+32	+40	+48	+56
		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		First Hex. Char. of Byte															

Notes:

1. For even byte ( $\Delta X$ ), second hexadecimal character is always odd (1, 3, 5, 7, 9, B, D, or F).
2. For odd byte ( $\Delta Y$ ), second hexadecimal character is odd if beam is to be blanked. If beam is to be unblanked, the second hexadecimal character is even (0, 2, 4, 6, 8, A, C, or E).

Figure C-2. Decimal-Hexadecimal Conversion Chart for Two-Byte Relative Vectors

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System  
Maintenance  
Library**

**System**

cut here

Y27-2045-1

IBM 2250 Display Unit Model 1 Printed in U.S.A. Y27-2045-1



**International Business Machines Corporation  
Field Engineering Division  
112 East Post Road, White Plains, N. Y. 10601**