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P/N 5994670

IBM®

LOGIC DIAGRAM MANUAL

IBM PART NO. 1277303

2741 COMMUNICATIONS TERMINAL VERSION 002

WIRED TO ACCEPT THE FOLLOWING SPECIAL FEATURES:

1- RIBBON CONTROL

2- TRANSMIT INTERRUPT

3- PRINT INHIBIT

4- AUTO ADDRESS ANSWERBACK

EC. NO.	308747					
.DATE	JUN70					
E.C. NO.						
DATE						

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JUN70	308747				
				PART NO. 5994671	PAGE NO. 0001
				IBM 2741	VER 002

TERMINAL IDENTIFICATION

MACHINE TYPE & MODEL NO. _____ SERIAL NUMBER _____

LINE NUMBER _____ TERMINAL ADDRESS _____ GROUP ADDRESS _____

TYPE OF SERVICE (DIAL, PRIVATE, LEASED LINE OR IBM MODEM TYPE _____

DATA SET MODEL _____

COMMON CARRIER IDENTIFICATION OF LINE _____

MULTIPLEXOR TYPE SERIAL NO. _____ TELEPHONE NO. _____

MULTIPLEXOR LOCATION _____

LOCAL COMMON CARRIER CONTACTS RESPONSIBLE FOR THIS SYSTEM

	NAME	TELEPHONE
PLANT (MAINTENANCE)		
MARKETING (COORDINATION)		
ENGINEERING (ASSISTANCE)		

INFORMATION TO COMPLETE THE ABOVE IS AVAILABLE FROM CUSTOMER ENGINEERING FIELD MANAGEMENT OR THE ACCOUNT SALESMAN.

FEATURE LISTING

✓	FEATURE	SALES FEATURE NUMBER	FACTORY FEATURE NUMBER	FIELD FEATURE NUMBER
	VOLTAGE			
—	112.5V AC 50 HZ	2810	1176628	5190255
—	123.5V AC 50 HZ	2811	1176629	5190255
—	195V AC 50 HZ	2812	1176630	5190255
—	220V AC 50 HZ	2813	1176631	5190255
—	235V AC 50 HZ	2814	1176632	5190255
—	115V AC 60 HZ	9880 OR 9881 OR 9901	1176607	5190251
—	208V AC 60 HZ	9884 OR 9885 OR 9902	1176625	5190252 OR 5190253
—	230 AC 60 HZ	9886 OR 9887 OR 9904	1176468	5190252 OR 5190253
	DATA SET ATTACHMENTS			
—	WE 103A OR 113A	9114	1176627	5190226
—	WE 103F	9115	1176611	5190228
—	3976 MODEL 1	2949	1176611	5190228
—	WESTERN UNION CLASS D	9116	1186331	5190229
—	150 BAUD SCHEDULE 3A	9120	1186331	5190230
—	2 WIRE LIMITED DISTANCE TYPE 1	4634	1176613	5190231
—	4 WIRE LIMITED DISTANCE TYPE 1	4635	1176624	5190232
—	*2 WIRE LIMITED DISTANCE TYPE 11	4790	1176608	5190233
—	*2 WIRE LEASED LINE ADAPTER	4639	1186217	5190234
—	*4 WIRE LEASED LINE ADAPTER	4647	1186218	5190235
—	*2 WIRE SHARED LINE ADAPTER CH 1	4641	1186280	5190236
—	*2 WIRE SHARED LINE ADAPTER CH 2	4642	1186281	5190237
—	*2 WIRE SHARED LINE ADAPTER CH 3	4643	1186282	5190238
—	*2 WIRE SHARED LINE ADAPTER CH 4	4644	1186283	5190239
—	*4 WIRE SHARED LINE ADAPTER CH 1	4691	1186284	5190240
—	*4 WIRE SHARED LINE ADAPTER CH 2	4692	1186285	5190241
—	*4 WIRE SHARED LINE ADAPTER CH 3	4693	1186286	5190242
—	*4 WIRE SHARED LINE ADAPTER CH 4	4694	1186287	5190243
—	*C BOARD REQUIRED FOR THESE FEATURES			
—	SYSTEM FEATURES			
—	DIAL UP	3255	1176626	5190227
—	RECEIVE INTERRUPT	4708	1176610	5190248
—	TYPAMATIC	8341	1176609	5190247
—	6 FT(1,83M) POWER CORD 60 HZ	9986	CONTACT PROD. ENG.	
—	TRANSMIT INTERRUPT	7900	5162726	5190846
—	PRINT INHIBIT CPU CONTROL	5501	5162728	5190347
—	RED RIBBON CONTROL	RPQ 868019	1277300	1277300 OR 1277052
—	AUTO ADDRESS ANSWERBACK	RPQ E46148	1277051 OR 1277344	1277051 OR 1277344

DATE	EC. NO.	DATE	EC. NO.	TERMINAL IDENTIFICATION
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2741 VERSION 002

GENERAL DESCRIPTION

A. Functional Objectives

This version machine adds two additional features and two RPQ features to the standard 2741. They are:

1. Ribbon Control (RPQ 868019)
2. Print Inhibit (SF 5501)
3. Transmit Interrupt (SF 7900)
4. Automatic Address Answerback (RPQ E46148)

These features are modular and may be installed individually or in groups.

A brief description of each of the features follows.

1. Ribbon Control - The terminal is placed in red ribbon mode when a "Prefix" followed by an "A" is received. It remains in this mode until a "Prefix - B" sequence is received or the terminal is removed from a receive status or a power off-on sequence is performed. The "A" and "B" mentioned above are in BCD code (A = BA1, B = BA2). See P.7000 for equivalent Correspondence Codes.
2. Print Inhibit - The terminal is placed in a "No-Print" status when a Bypass code is received. Receiving a Restore code or a power Off-On sequence returns the 2741 to a printable status. When in a "No-Print" status, the element "Spaces" when a normally printable character is received or transmitted.
3. Transmit Interrupt - The CPU can force the terminal to leave the Transmit Text mode by sending it a "long space" (200 ms or longer in duration). The 2741 must be equipped with a full duplex line adapter or data set.
4. Auto Address Answerback - The CPU will send the 2741 a "Prefix" followed by a "+" and a "Ⓒ". The terminal will assume the Transmit Text mode and will automatically transmit (1) Ⓓ, (2) its programmable four character station address, and (3) Ⓒ. The Ⓒ will take the terminal to the Receive Control Mode. Codes which have special meanings (such as Ⓒ) should not be included in the allowable address codes. The "+" mentioned above is the BCD "+" (BAC). See P.7000 for the equivalent Correspondence Code.

B. Circuit Modifications

Since the features are installed in a modular fashion, the change to the standard machine consists of only additions. The electronics package is electrically identical to the standard 2741 when none of the RPQ's are installed.

C. I/O Modifications

Minor changes to the I/O wiring are necessary when the Print Inhibit feature is installed. The Ribbon Control feature requires a rather major I/O modification. The feature additions are depicted on the I/O schematic in this manual.

IBM PART NO. 1277357

EC No.	545071	308734	
DATE	11-15-66	MAR70	

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INSTALLATION INSTRUCTIONS

IBM PART NO. 1186225

2741 COMMUNICATIONS TERMINAL

E.C. NO.	506826	507567	306754	307100		
DATE	16 AUG 66	24 FEB 67	MAY 67	APR 68		

2741 INSTALLATION INFORMATION

1. SPECIAL TOOLS AND TEST EQUIPMENT

The following tools should be available during installation:

CE Aid Box, PN 1272825
SLT Test Light, PN 453601
Oscilloscope (Tektronix 561 or equivalent) modem installation
Selectric I/O Tools
CARD EXTENDER P/N 452554 (MODEM INSTALLATIONS)

2. ASSEMBLY

A. UNIT PLACEMENT

The unit should be moved to the final position, indicated by the customer. CAUTION: Care must be exercised during handling and moving of unit since the printer is not fastened to the console. Do not remove the straps holding the printer to the console until final unit placement is accomplished. If the cables are to be routed under the floor, the cutout should be located at the left rear of the unit. Adjust foot of machine for proper leveling.

B. PREPARATION FOR RESHIPMENT

Shipping of systems and units is described in detail in the branch office manual. Packing material required for shipment may be ordered from the manufacturing plant as described in the branch office manual. The packing material for the 2741 Communications Terminal is in BM 7340966, for padded van shipment, or BM 7340961 for common carrier and export, available from IBM, Raleigh, N. C.

3. CABLE INSTALLATION

A. PRELIMINARY CHECK

Before applying power to unit make a complete visual check of unit for possible damage or loose parts. Check SLT gate for loose cards, edge connectors, or bent back panel pins. Check power supply mounting for damage during shipment.

B. AC POWER

Voltage specifications may be found on back of stand under rear cover. Be sure to check that Customer voltage matches machine requirements before installation.

Electrical Requirements

Voltage: 115 or 208/230 ± 10% or 112.5, 123.5, 195, 220 or 235 ± 10%

Frequency: 60 ± 1/2 HZ or 50 ± 1/2 HZ

Phase: 1

Service: 15 AMPS

C.. DATA SET CABLE

All data set installations should be completed prior to arrival of machine. Connection to data set is accomplished with 8' data set cable supplied with unit. Connection is made to rear of data set with 25 pin socket marked "Customer Equipment." Check that data set has AC voltage applied.

D.. MODEM INSTALLATIONS

Limited Distance Line Adapter Type 1A SLT 2-wire

When all terminals have been installed & all lines without terminals have been terminated properly (3K, 1/4 watt resistor across communication line), the following procedure is used to terminate the terminals at the ends of the network or at end of all radial lines.

1. Remove modem cable P/N 1176471 from terminal (B1M4 socket). Insert jumper P/N 811824 on cable card.
2. Insert paddle on SLT extender P/N 452554 & place extender in machine (B1M4 socket).
3. Set up scope with a DIFFERENTAL PRE-AMP OR THE ALGEBRAIC ADD OPTION AND MEASURE ACROSS PINS B02AND B07 SOCKET POSITION B1K4.
4. Place terminal in transmit mode or bring up request to send

   2741 - Depress Communicate

5. Adjust potentiometer on paddle card until 0.9 volts peak to peak is attained as a maximum transmitted mark level on the largest signal viewed.
6. The other end of the line is then set as stated above, (or all radial ends).
7. Have system or terminal at other end of line send the character "V" repetitively to give alternating mark & space frequency.
8. Check that both mark & space frequency received - signal levels must be equal to or exceed 370 millivolts peak to peak.
9. For a system which is maximally loaded (line length versus number of terminals) it may be necessary to repeat steps 5 and 6 to satisfy step 8.
10. Remove extender and set machine back to normal and test on line.

Limited Distance Line Adapter Type 1B SLT 4-wire

When all terminals have been installed & all lines without terminals have been terminated properly (3K, 1/4 watt resistor across receive line & 5K, 1/4 watt resistor across transmit line) the following procedure is used to terminate the terminals at the ends of the network or at end of all radial lines.

1. Remove modem cable P/N 1176471 from terminal (B1M4 socket). Insert jumper P/N 811824 on cable card.
2. Insert paddle on SLT extender P/N 452554 & place extender in machine (B1M4 socket).
3. Set up scope with a differential pre-amp or the algebraic add option & measure across pins B02 & B07 socket position B1K4.
4. Place terminal in transmit mode or bring up request to send.

   2741 - Depress communicate

5. Adjust potentiometer on paddle card until 0.9 volts peak to peak is attained as a maximum transmitted mark level on the largest signal viewed.
6. The other end of the line is then set as stated above (or all radial ends).
7. Set up scope across J05 & J07 socket position B1K4.
8. Have system or terminal at other end of line send the character "V" repetitively to give alternating mark or space frequency.
9. Check that both mark & space frequency received - signal levels must be equal to or exceed 370 millivolts peak to peak.
10. For a system which is maximally loaded (line length versus number of terminals) it may be necessary to repeat steps 4 and 5 to satisfy step 8.
11. Remove extender and set machine back to normal and test on line.

Limited Distance Line Adapter Type 2B SLT 2-wire

When all terminals have been installed and all transmission lines without terminals have been terminated properly (600 ohm, 1/4 watt across the ends of a long line network or at the end of all radial lines or a 5K ohm, 1/4 watt across all side legs) the following procedure is used:

1. Card P/N 5806182 socket C1B6 is plugged as follows:

   a) Transmit Level

      0 DBM Jumper 1 to 3 All In-House Line

      -8 DBM No Jumpers Common Carrier Lines

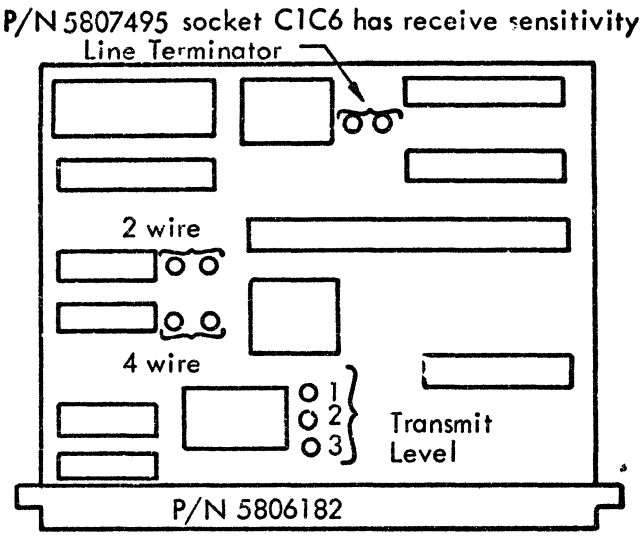
   b) 2 wire is jumpered

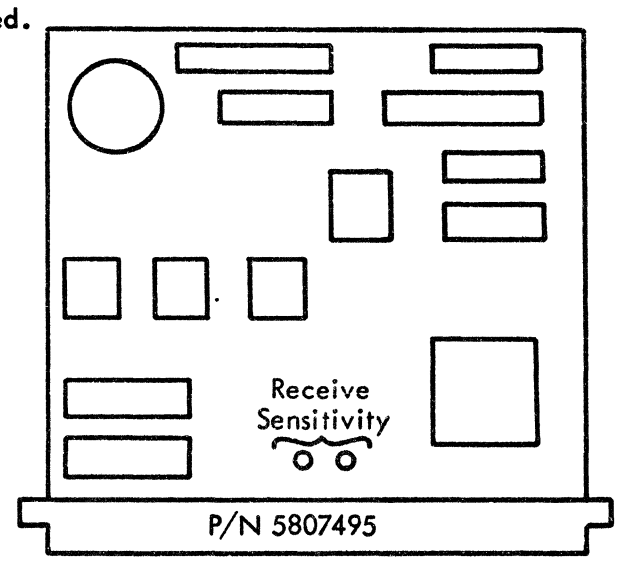
      4 wire is not jumpered

   c) Line Termination (680 ohm resistor) is jumpered at the ends of a long line network or at the end of all radial lines.

      JUMPERED.

2. Card P/N 5807495 socket C1C6 has receive sensitivity plugged.





Leased Line Adapter Type 1A SLT 2-wire

When all terminals have been installed & all lines without terminals have been terminated properly (620 ohm or 680 ohm, 1/4 watt across communication line) the following procedure is followed to set line adapters on all terminals in the network:

1. Card P/N 5808123 socket C1B6 is plugged:

   a) Transmit Level

      0 dbm Jumper 1 to 3 all in house lines

      -8 dbm No Jumpers Common Carrier Lines

   b) 2 wire is jumpered

      4 wire is not jumpered

   c) Line termination (680 ohm resistor) is jumpered

2. Card P/N 5807495 socket C1C6 has receive sensitivity plugged (Refer to Modem type 2B for card layout)

3. Card P/N 5808121, 2 wire is plugged.

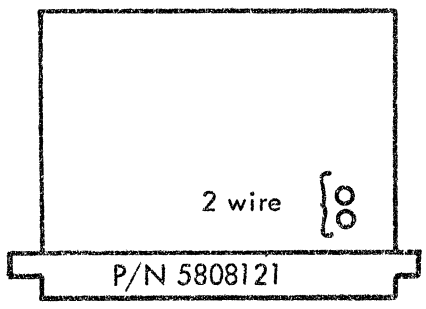
4. Modem Wrap test.

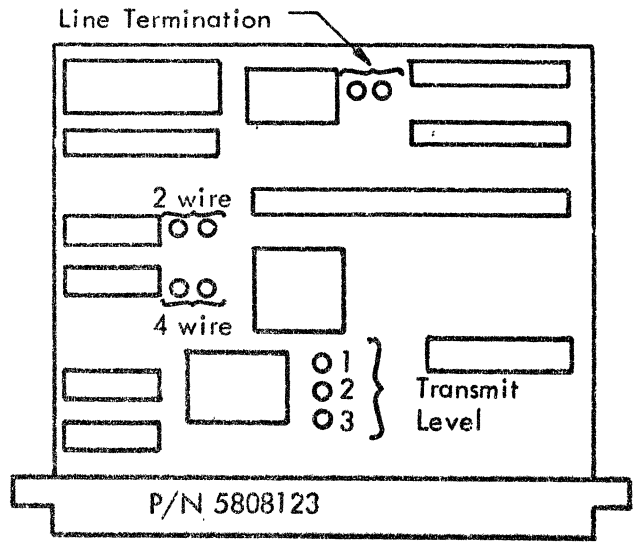
   a) Place machine in communicate mode

   b) Place modem test switch to "MOD" position.

   c) Key characters from keyboard - MODEM TEST light will blink showing test is functioning correctly.

   d) Place modem test switch to "off" position





Leased Line Adapter Type 1B SLT 4-wire

When all terminals have been installed & all lines without terminals have been terminated properly (620 ohm or 680 ohm, 1/4 watt across Transmit Line & 620 ohm or 680 ohm, 1/4 watt across Receive Line) the following procedure is followed to set Line adapters on all terminals in network.

1. Card P/N 5808123* socket C1B6 is plugged.

   a) Transmit Level

   0 dbm jumper 1 to 3 all in house lines

   -8 dbm No jumpers Common Carrier lines

   b) 2 wire not jumpered

   4 wire jumpered

   c) Line termination (680 ohm resistor) is jumpered (transmit)

*Refer to LLA 2 wire section for card layout.

2. Card P/N 5807495 socket C1C6 has receive sensitivity plugged (Refer to Modem type 2B section for card layout).

3. Card P/N 5808121, 2 wire is not plugged (Refer to LLA 2 wire section for card layout)

4. Card P/N 5808119, Line termination Receive is plugged.

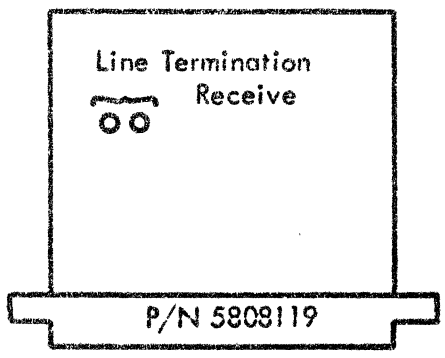
5. Modem Wrap test

   a) Place machine in communicate mode

   b) Place modem wrap test switch to "MOD" position

   c) Key characters from Keyboard - MODEM TEST light will blink showing test is functioning correctly.

   d) Place Modem test switch to "off" position.



Shared Line Adapter Type 1A SLT 2-wire

When all terminals have been installed and all transmission lines terminated properly (Insert termination plug P/N 5151250 into the telephone jack provided for line termination). THE FOLLOWING PROCEDURE IS USED:

1. Card P/N 5808125 should be plugged for 2 wire.

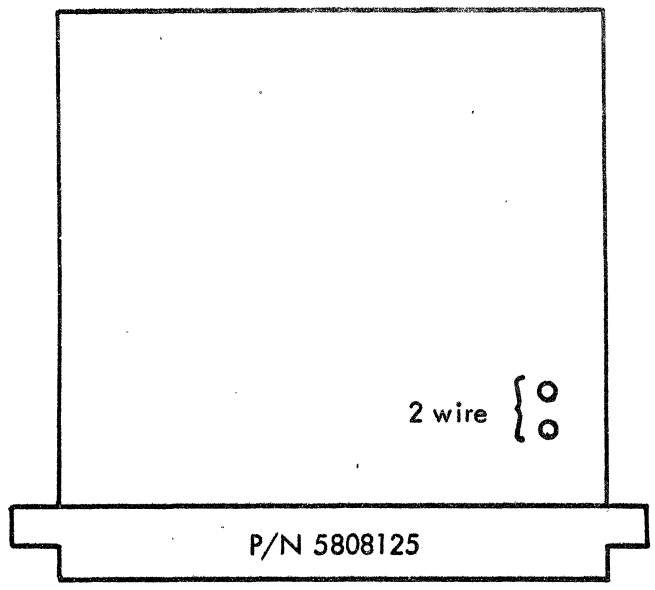
2. MODEM WRAP TEST

   a) Place machine in communicate mode.

   b) Place Modem Text switch to "MOD" position.

   c) Key characters from keyboard- MODEM TEST light will blink showing test is functioning correctly.

   d) Place Modem Text switch to "off" position.



Shared Line Adapter Type 1B SLT 4-wire

When all terminals have been installed and all transmission lines terminated properly [insert termination plug (P/N 5151251) into the telephone jack provided for line termination] the following procedure is used:

1. Card P/N 5808125 should not be plugged 2 wire (Refer to Shared Line 2w for card layout).
2. Modem Wrap Test

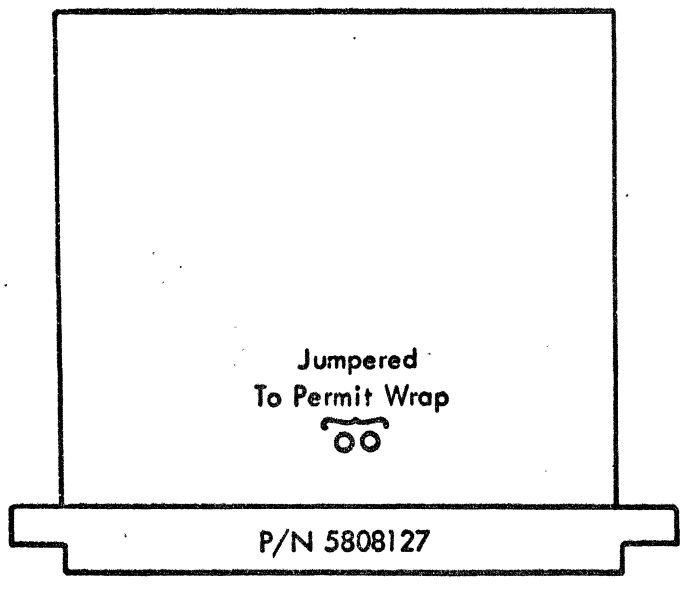
   a) Card P/N 5808127 must be plugged to permit wrapping (socket C1A6)

   b) Place machine in communicate mode

   c) Place Modem Test switch to "MOD" position.

   d) Key characters from keyboard (MODEM TEST light will blink showing test is functioning correctly)

   e) Place Modem Test switch to "off" position



4. UNIT TESTING

A. PROGRAM CAP PLUGGING

1. Check card in OIA-B1J4 PN 5804515 for correct plugging (Ref. page 7000)

B. VOLTAGE CHECK

Apply power to unit and check voltages to SLT Gate.

+48 Volts, ±4 Volts measured at location A-B1L1DØ5

+12 Volts, ±.6 Volt measured at location A-B1L1DØ3

-12 Volts, ±1 Volt measured at location A-B1L1BØ6

C. LOCAL MODE TEST (2741)

With machine in local mode, test all typewriter functions for proper operation. Perform preliminary test of electronics, using check loop as follows:

1. Local - Communicate switch in local.
2. Depress attn key and hold.
3. Depress key of character.
4. Character will continuously print until attn key is released. Check as many characters as necessary to properly check the 1B register, 2B register and tilt rotate magnets.

D. 2741 TESTING

On systems using 2701, 2702, OR 2703 Control Units, a program titled 2741 checkout (FD 13) is available to test the 2741 terminal installation. The following items should be noted prior to scheduling the running of the program:

1. The Customer Engineer at the terminal location must establish voice communication prior to and during testing with the CE at the CPU location. It will be necessary for the terminal Customer Engineer to give the central operator several items of information required to operate the program.

   a) Does the terminal have the Interrupt (break) feature?

   b) Does the terminal have the 2-wire line adapter?

There are several error messages that may be printed at the central location. If terminal test procedures do not work the way they are described, the error printouts may provide information helpful to the terminal CE. Contact the central operator for this information. After the program is loaded and data communication between the CPU and the terminal is established, the program is started when the terminal operator depresses the attention key. The CPU will respond by transmitting a standard message to the terminal. The program then prepares the central to receive the same standard message from the terminal.

The central compares the received message with the standard message to determine whether they are identical. The next program mode is the alternate mode in which the central receives a message from the terminal and transmits it back to the terminal. The first character of the message transmitted to the central must be a number between 1 and 9, which determines the number of times the message will be automatically transmitted back to the terminal.

IBM MAINTENANCE DIAGNOSTIC PROGRAM

2741 CHECKOUT

The program will insert a minimum delay of approximately 5 seconds between repeats of messages to the terminal. This delay will also be inserted between any program repeats due to program detected errors.

NOTE: (CR) Represents a carrier return

(UC) Represents upper case shift

(LC) Represents lower case shift

A step by step description of the operation follows:

a) CPU operator starts program

b) CPU sends the following message:

Ⓓ (UC)ASDFGHJKL(LC)1234567890(CR)

This message is repeated 10 times, with the last line being terminated with a Ⓒ.

In lines 2 through 10, the Ⓓ will appear as the data character, 9.

The Ⓒ will put the terminal in transmit and the terminal will send a Ⓓ to the CPU.

c) The terminal operator then keys in the same message as received from the CPU--

(UC)ASDFGHJKL(LC)1234567890(CR) Ⓒ

NOTE: Keying CR ends the message by automatically generating Ⓒ (EOT).

d) The CPU will compare the received message with the message sent in step "b" above; and if they don't compare, the CPU will respond to the terminal with the following message--

Ⓓ (CR) TRANSMISSION NO GOOD Ⓒ

and will wait for a retransmission of the message.

e) If the message was received correctly by the CPU, the program will proceed to alternate mode and send the following message to the terminal--

Ⓓ START ALTERNATE MODE (CR) Ⓒ

The alternate mode of the program consists of a tete-a-tete between the terminal and the CPU.

f) The terminal operator may now send a message to the CPU. The first character of the message must be a numeral from 1 to 9 followed by no more than 100 additional characters. A tab or carrier return is counted as 16 characters. The message is ended with a CR.

g) Sample tete-a-tete message

Terminal sends--

Ⓓ 4(UC)TEXT(CR) Ⓒ

The CPU will send the message back to the terminal a number of times equal to the numeral entered.

Only the last line will contain the ending ©, and all lines after the first line will recognize the Ⓓ as a data character, 9.

CPU return transmission--

D 4(UC) TEXT (CR) ... 15 idles ....

94(UC) TEXT (CR) ... 15 idles ....

94(UC) TEXT (CR) ... 15 idles ....

94(UC) TEXT (CR) ... 15 idles .... ©

The © places the terminal in transmit mode.

h) The alternate mode of the program may now be repeated; or if desired, the program may be terminated by the terminal operator.

NOTE: The interrupt feature must be tested during the alternate mode, if desired. If the attention key is depressed while the CPU is transmitting, the line will break and the CPU will send a © to the terminal and then wait for another message.

Program Termination

1. To terminate the program, the terminal operator sends the following message to the CPU--

(UC) END ©

The CPU upon receiving this end message will idle the line by sending a ©.

Keyboard Note: Standard message listings assume the 2741 has a Courier 72 Correspondence Keyboard. If the keyboard is different, the CE may observe some differences in the standard message and Ⓓ translation. This will not affect the logic of the program.

IBM Field Engineering

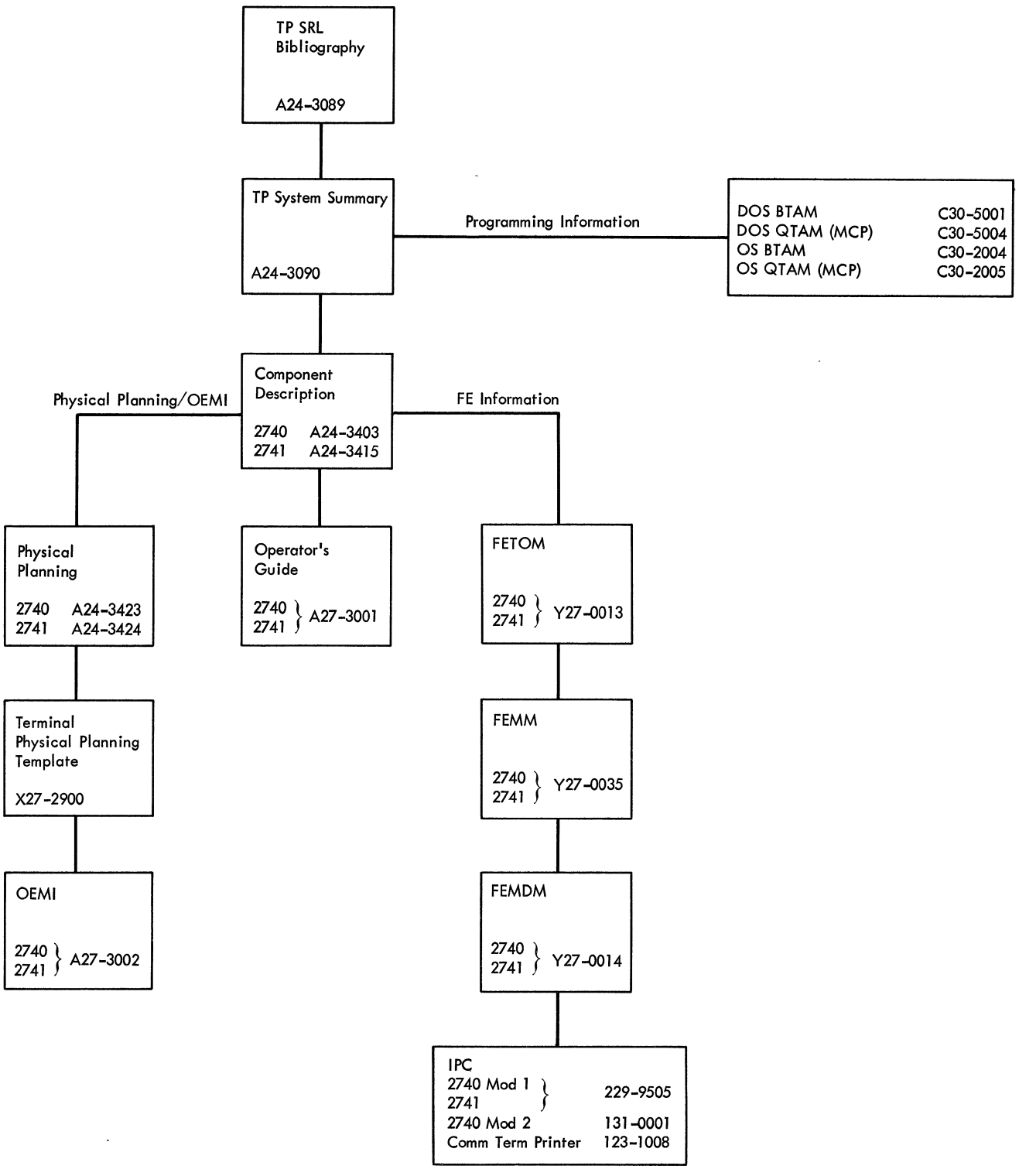
Maintenance Diagrams

2740 Communications Terminal Model 1
2740 Communications Terminal Model 2
2741 Communications Terminal

SY27-0014-3

2740/2741 SRL/FE Publications Availability Guide

Use this guide to determine what available publications will best fulfill your individual requirements



IBM Field Engineering

Maintenance Diagrams

2740 Communications Terminal Model 1
2740 Communications Terminal Model 2
2741 Communications Terminal

SY27-0014-3

PREFACE

Detailed explanations of the diagrams in this manual are in the 2740 Model 1/2740 Model 2/2741 Communication Terminals Theory of Operation manual, Form Y27-0013-2.

All diagrams in this manual are positive logic; that is, a positive level is required to condition ANDs, ORs, etc. Triggers and latches also require a positive level to be turned on or off.

The upper half of triggers and latches is the turn-on (set); the lower half is the turn-off (reset). Lines going directly into the trigger blocks are dc set or reset; lines going to an AND butted against the trigger block are the ac set or reset (indicated by a capacitor symbol in one line).

HISTORY

FEMDM	Y27-0014-0	December 66	EC 506395
FES	Y27-1020	February 68	EC 506395
FEMDM	Y27-0014-1	April 68	2741 at EC 307100 2740-1 at EC 306848 2740-2 at EC 307147
FES	Y27-1031	July 68	2740-2 at EC 307426
FEMDM	Y27-0014-2	October 68	2741 at EC 307100 2740-1 at EC 306848 2740-2 at EC 307426
FES	Y27-1037	January 69	2740-2 at EC 307463
FEMDM	Y27-0014-3	September 69	2741 at EC 307100 2740-1 at EC 307460 2740-2 at EC 307500

ABBREVIATIONS

◊	Symbol used in ALDs and MDM to indicate feature lines
CA	Control Address Mode
CAS	Control Address Selected Mode
CASS	Control Address Selected Slave Mode
CL	Control LRC
CR	Control Receive Mode
CS	Control Selected
CSS	Control Selected Slave Mode
IPM	Intermediate Polling Mode
LRC	Longitudinal Redundancy Check
NAO	Negative Answerback Override
OIU	Optical Image Unit
RCAB	Receive Check Answerback Mode
RCS	Receive Check Slave
RL	Receive LRC
RLS	Receive LRC Slave
RT	Receive Text, Reverse Transmission
RTS	Receive Text Slave Mode
SC	Station Control
TC	Transmit Control
TCAB	Transmit Check Answerback
TL	Transmit LRC
TNS	Transmit Nonselected Mode
TPAB	Transmit Poll Answerback Mode
TT	Transmit Text
TSAB	Transmit Status Answerback
VRC	Vertical Redundancy Check

Fourth Edition (September 1969)

This is a major revision of, and obsoletes, Y27-0014-2. It incorporates FE Supplement Y27-1037 and information on the 2760 Optical Image Unit Attachment feature and includes other minor changes.

Changes are periodically made to the specifications herein; any such changes will be reported in subsequent revisions or Field Engineering Supplements.

This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. 860, P. O. Box 12275, Research Triangle Park, North Carolina 27709. A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be addressed to the above address.

TAB

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PLEASE NOTE:

In an attempt to increase the usefulness of FE manuals, we are trying this "tab indexing" scheme in this manual. If you feel that this scheme is:

of assistance in locating diagrams,
not needed, or
can use improvement

please tell us so by returning the Reader's Comment form at the back of the manual.

Thank you,

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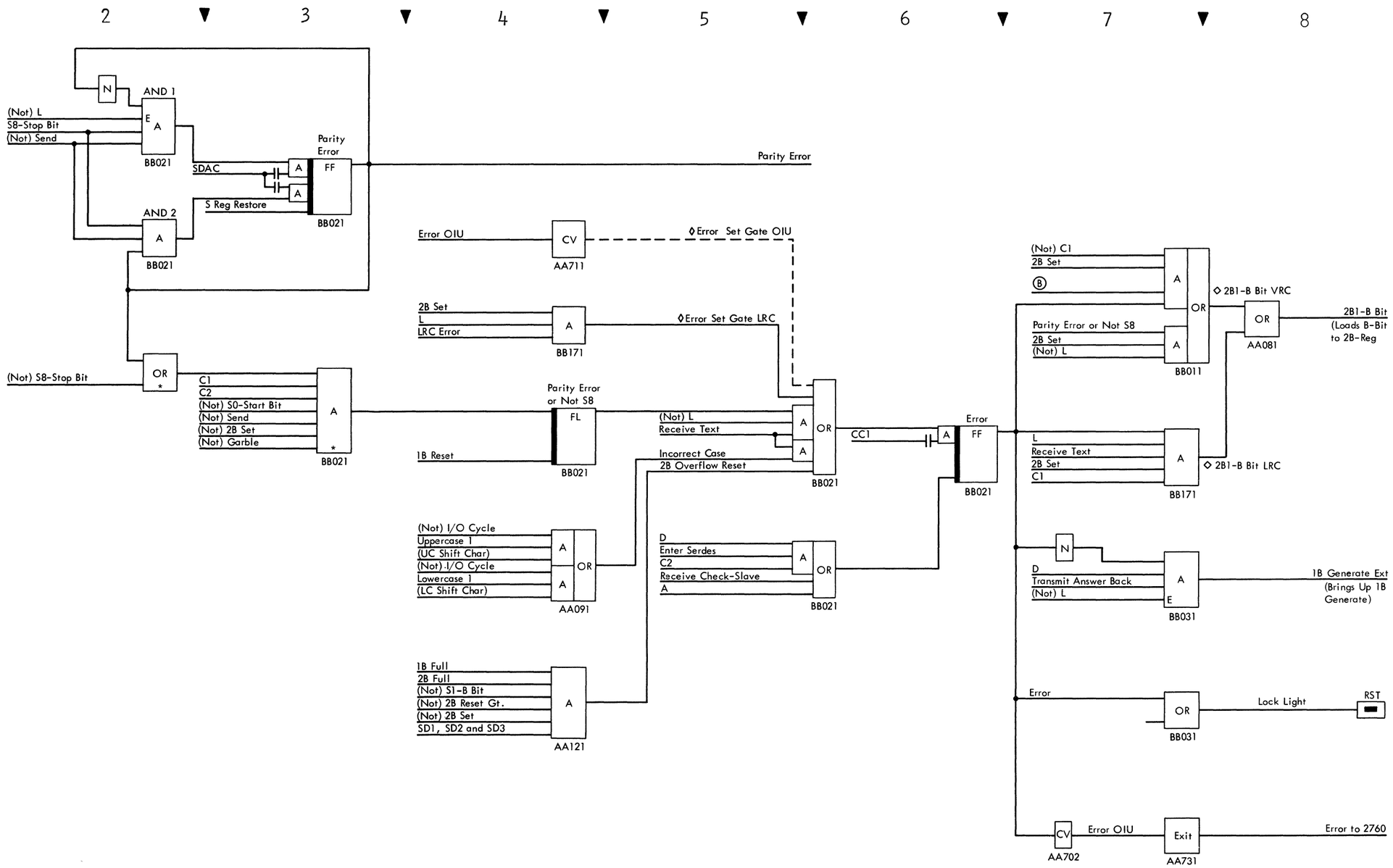
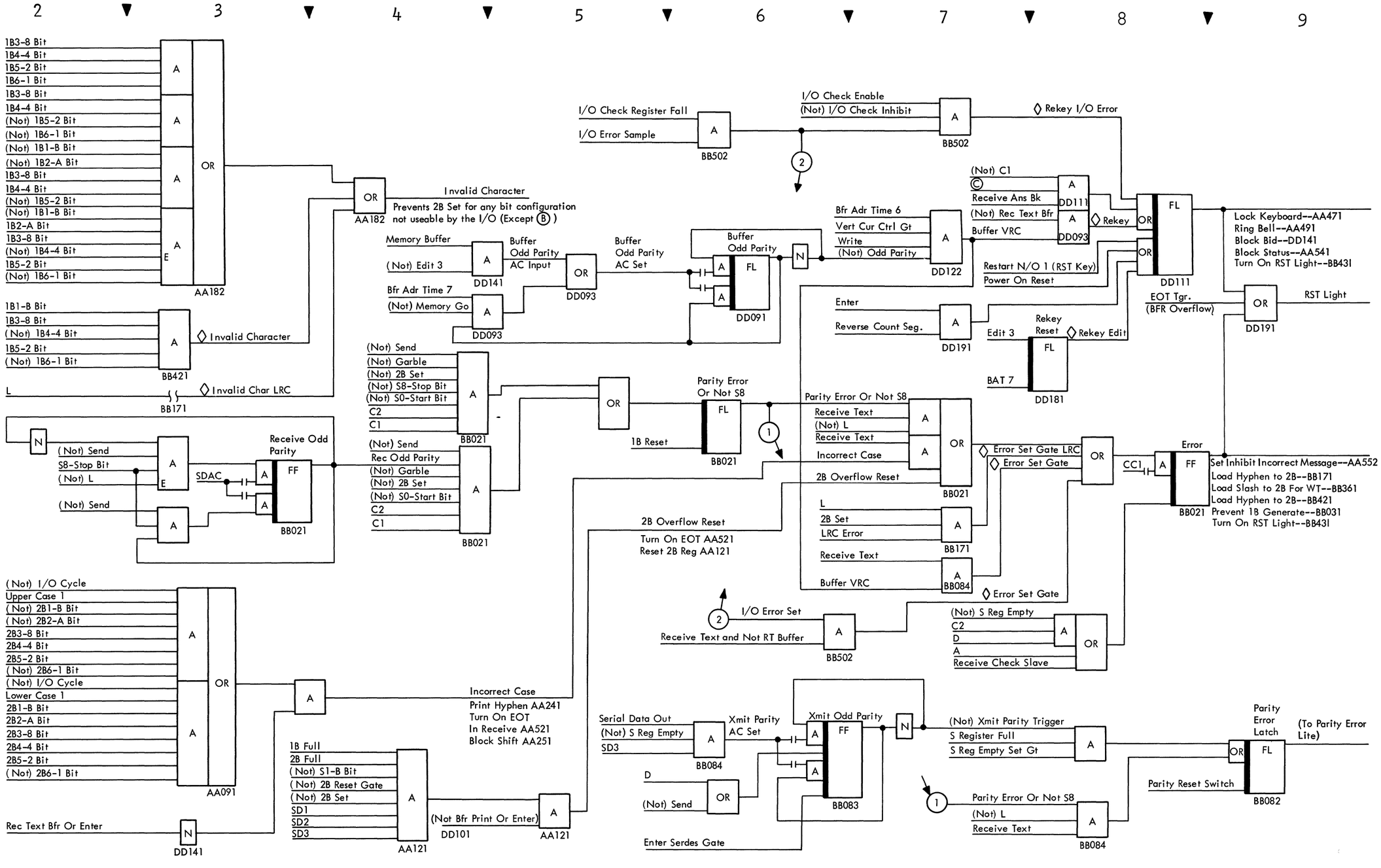
Research Triangle Park, N. C.

CONTENTS



* Logically, but not technically correct.

Diagram 2-2. Error Conditions and Invalid Character (2740-2)



H G F E D C B A

Receive Text
(Not) RT Buffer
A
BB502
Receive Text and Not RT Buffer

OR
BB502
I/O Check Enable

1

Buffer Print
Communicate
A
BB502
Buffer Print and Comm.

I/O Cycle
2B Reset Latch
A
BB511
Set I/O Latches

Notes: * I/O Check Enable and I/O Check Registers have seven latches (1 for each Bit).
* - * Seven Lines (1 for each Bit).
See Diagram 2-4.

2B (* - *) Bit
Set I/O Latches
A
BB521

I/O Check (*) Enable
A FL
Reset I/O Latches
BB521-2

2

N
A
A
BB521
I/O Check (*)
OR FL
OR
BB521-2
I/O Check (*)

OR
BB521

Intergrated Printer (*-*) Bit
I/O Check Strobe

2

1

Transmit Answerback
1st Status Character Answerback
1B Set Not EOT
A
BB501
Load 1st Char. Answerback

(Not) Transmit Odd Parity
(Not) S Register Full
A FL
Power On Reset
OR
BB501
Transmit Parity Error

Status
A
BB501
Error Latch Reset

2nd Status Char. Ansbk.
C1
A
BB511
1st Status Character Latch Reset

Parity Error or Not S-8
Receive Text
(Not) L
A FL
Power On Reset
OR
BB502
Receive Parity Error

Jmpr.

Note: This jumper is used to disable Receive parity error latch.

I/O Error Sample
I/O Check Reg Full
A
BB502

1

I/O Check Enable
(Not) I/O Check Inhibit
Power On Reset
A FL
OR
BB502
I/O Error

N

2B Overflow Reset
1
I/O Check Enable
Incorrect Case
A
A
OR
BB501

I/O Check Inhibit
FL
I/O Check Inhibit

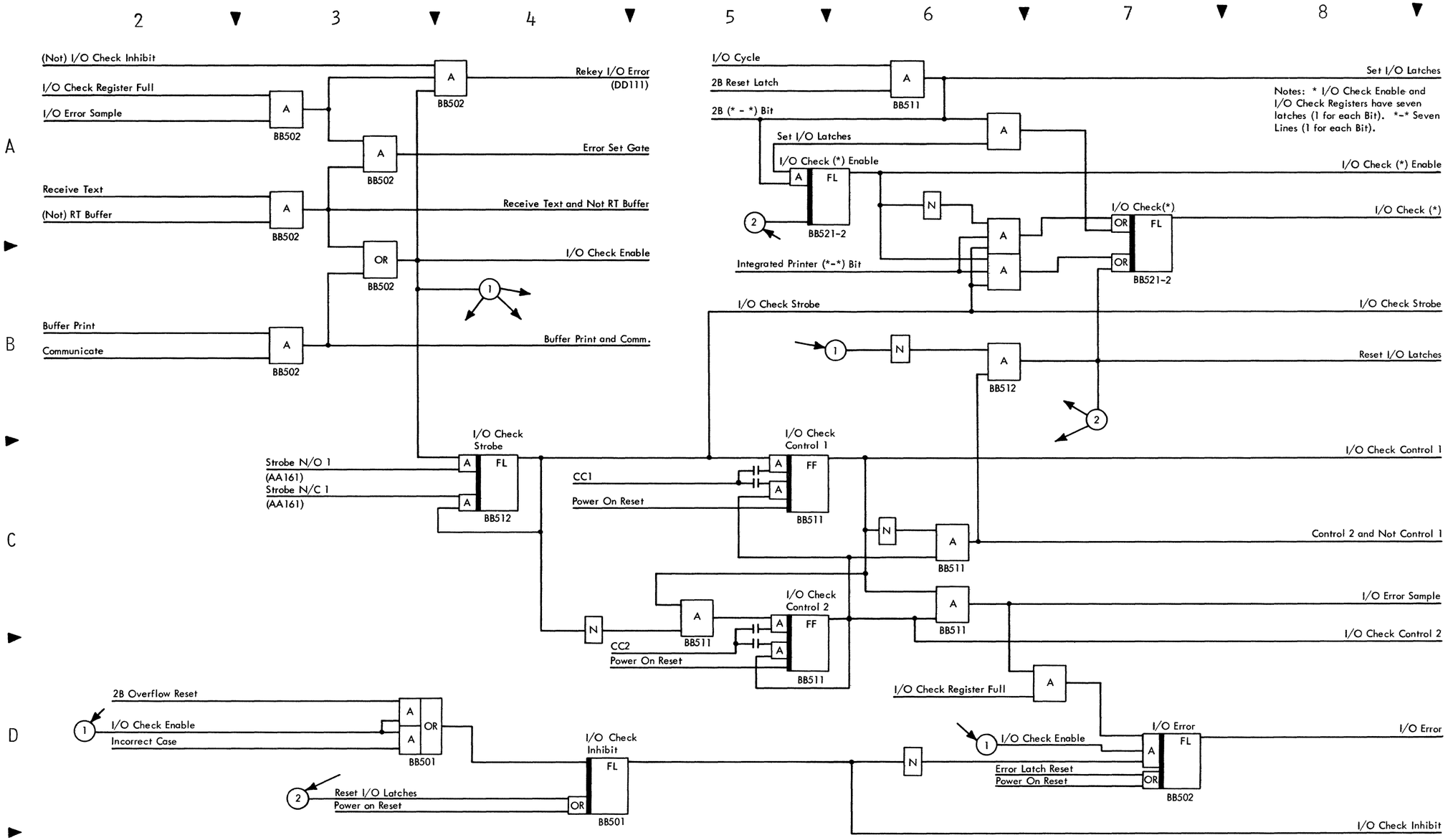
Control 2 and Not Control 1
Power On Reset
OR
BB501

Receive Text Buffer
Buffer Print & Comm.
OR
BB501

Buffer VRC
Power On Reset
A FL
OR
BB501
Electronic Error

2 3 4 5

Diagram 2-4. I/O Checking (2740-2) Part 1 of 2



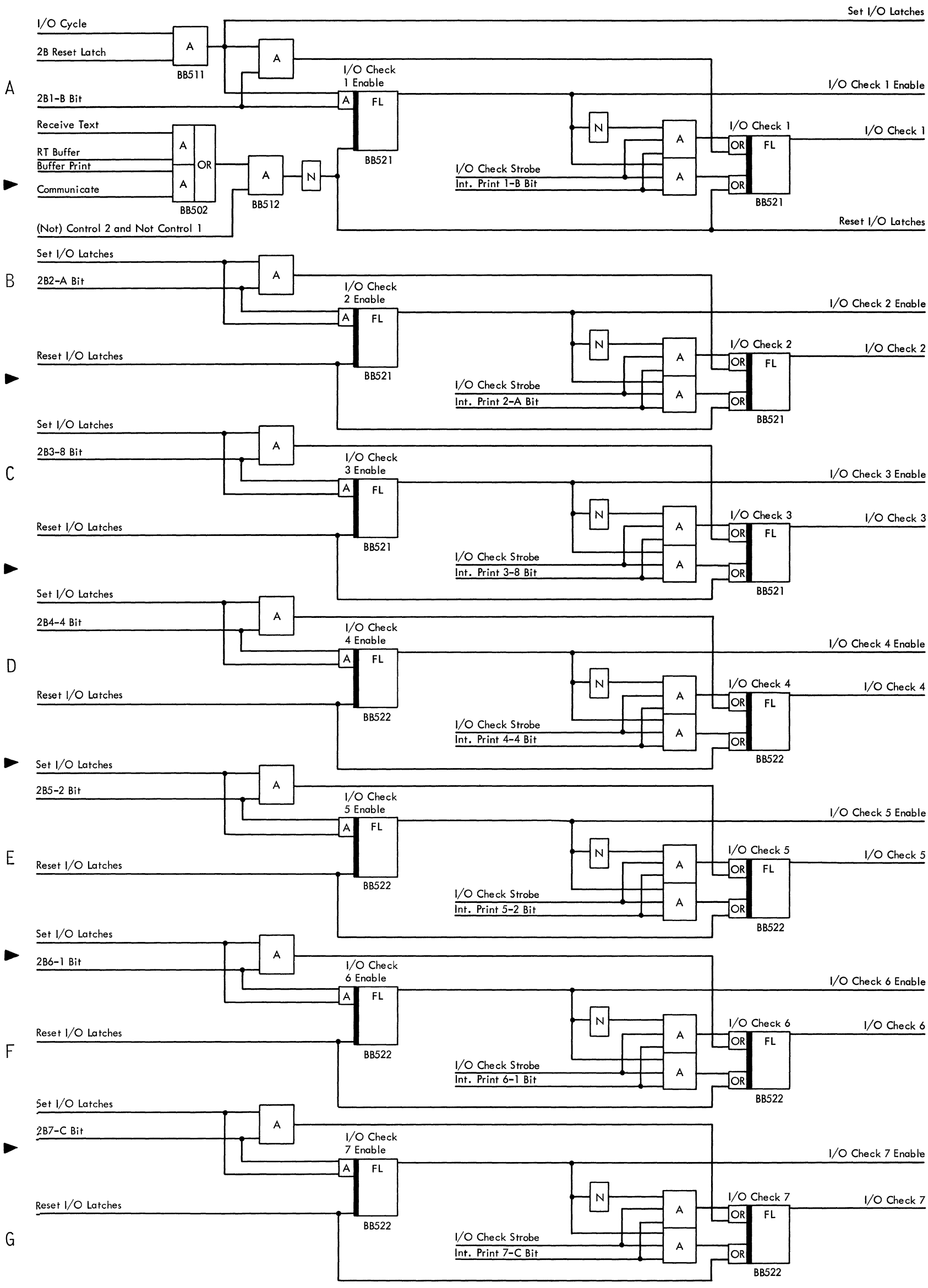


Diagram 2-4. I/O Checking (2740-2) Part 2 of 2

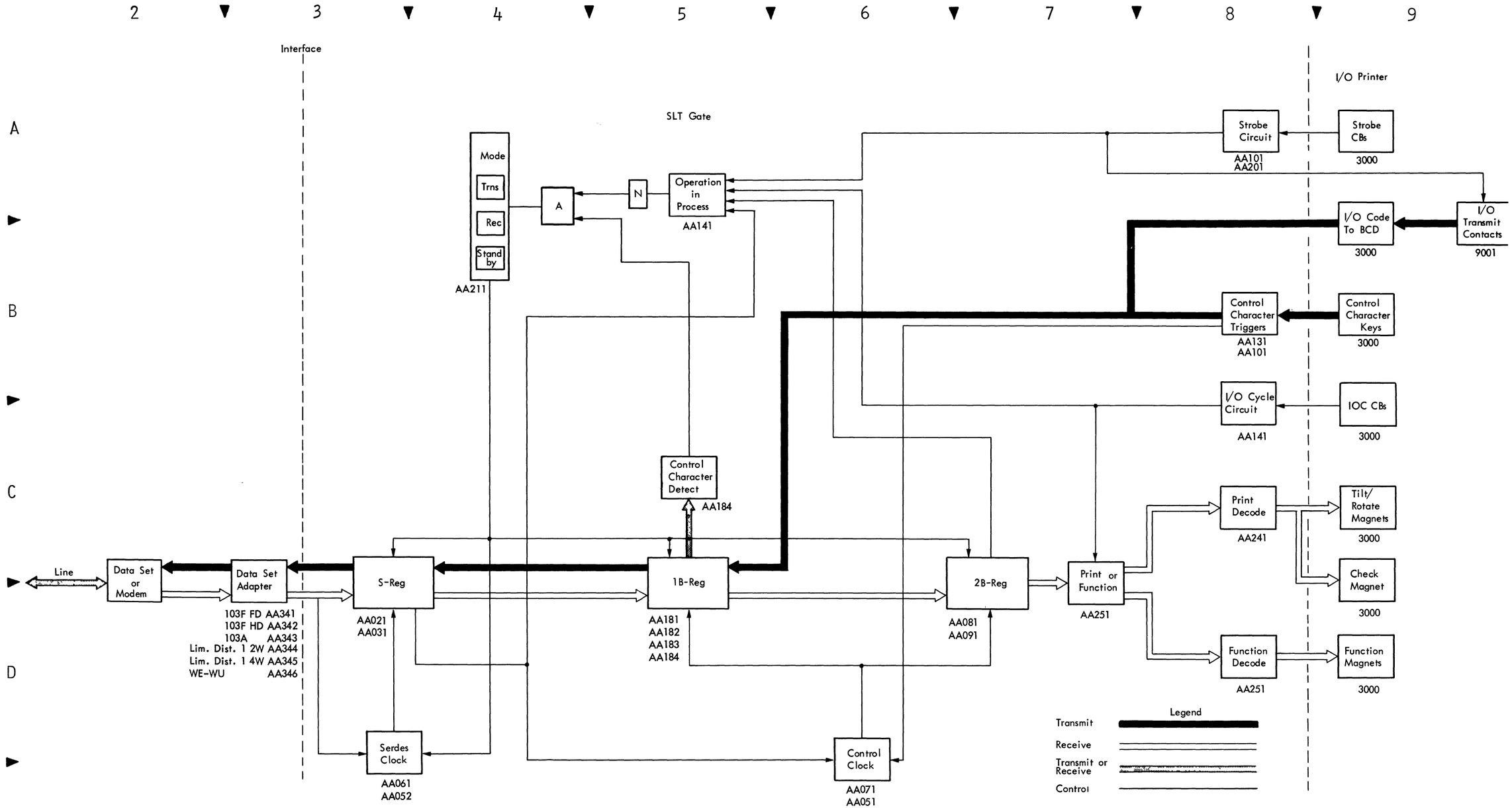
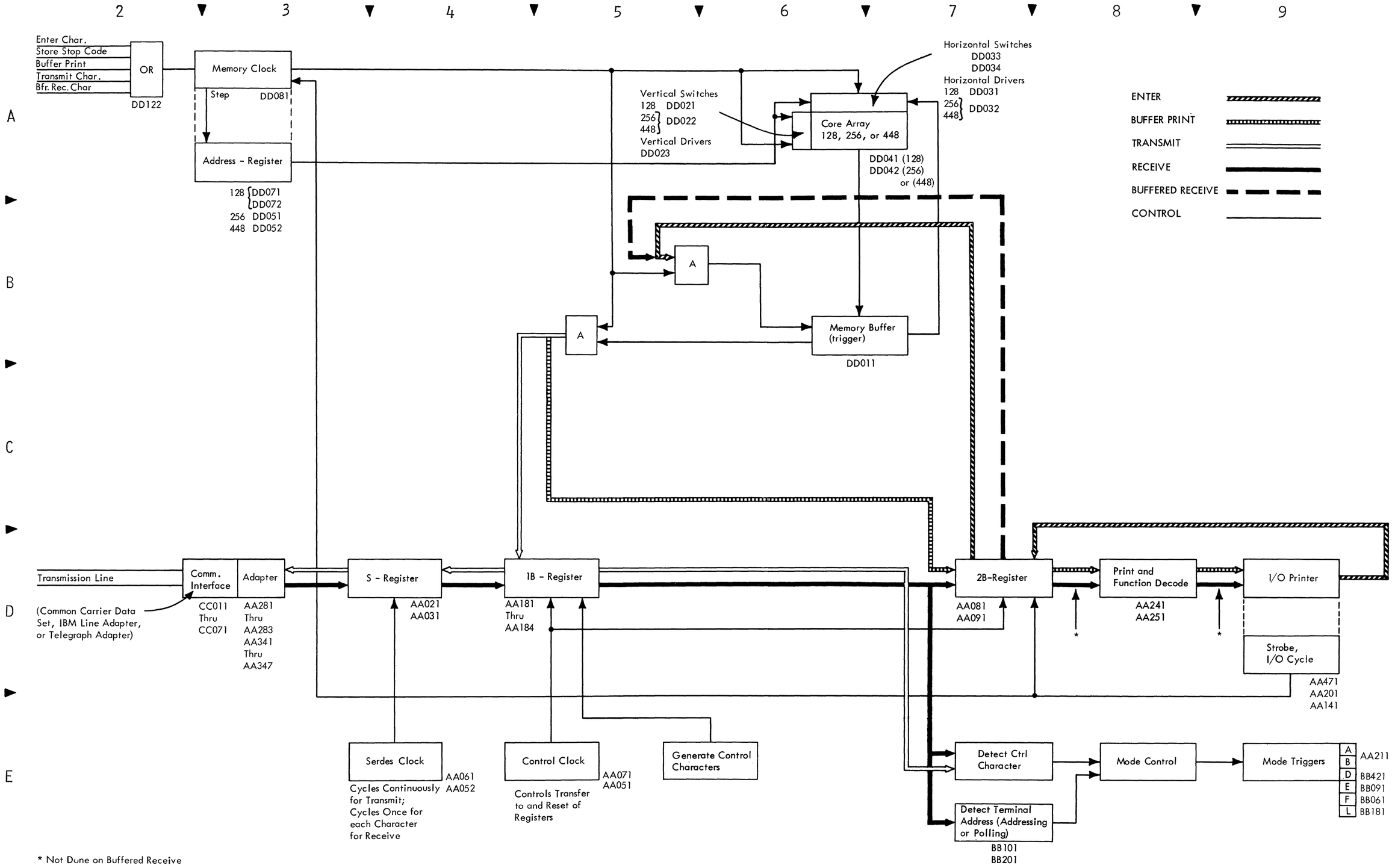
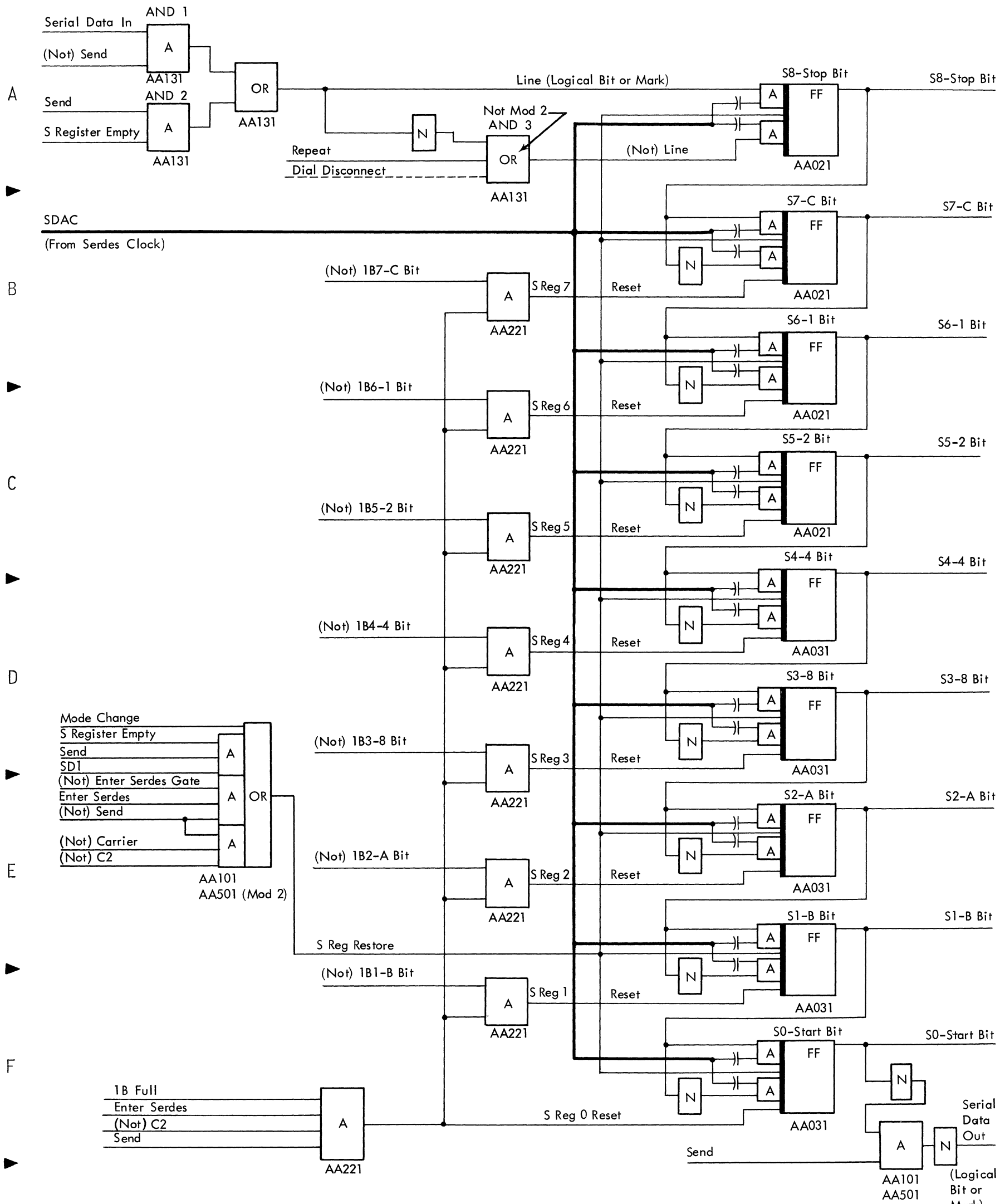

2
3
4
5
6
7
8
9
A
B
C
D
E
Interface
I/O Printer
SLT Gate
Mode
Trns
Rec
Stand by
AA211
A
N
Operation in Process
AA141
Strobe Circuit
AA101
AA201
Strobe CBs
3000
I/O Code To BCD
3000
I/O Transmit Contacts
9001
Control Character Triggers
AA131
AA101
Control Character Keys
3000
I/O Cycle Circuit
AA141
IOC CBs
3000
Control Character Detect
AA184
Print Decode
AA241
Tilt/ Rotate Magnets
3000
Check Magnet
3000
Function Decode
AA251
Function Magnets
3000
Line
Data Set or Modem
Data Set Adapter
103F FD AA341
103F HD AA342
103A AA343
Lim. Dist. 1 2W AA344
Lim. Dist. 1 4W AA345
WE-WU AA346
S-Reg
AA021
AA031
1B-Reg
AA181
AA182
AA183
AA184
2B-Reg
AA081
AA091
Print or Function
AA251
Serdes Clock
AA061
AA052
Control Clock
AA071
AA051
Legend
Transmit
Receive
Transmit or Receive
Control

Diagram 3-2. Data Flow and Control (2740-2)





Note: Dotted lines indicate feature inputs.

Diagram 4-1. S-Register

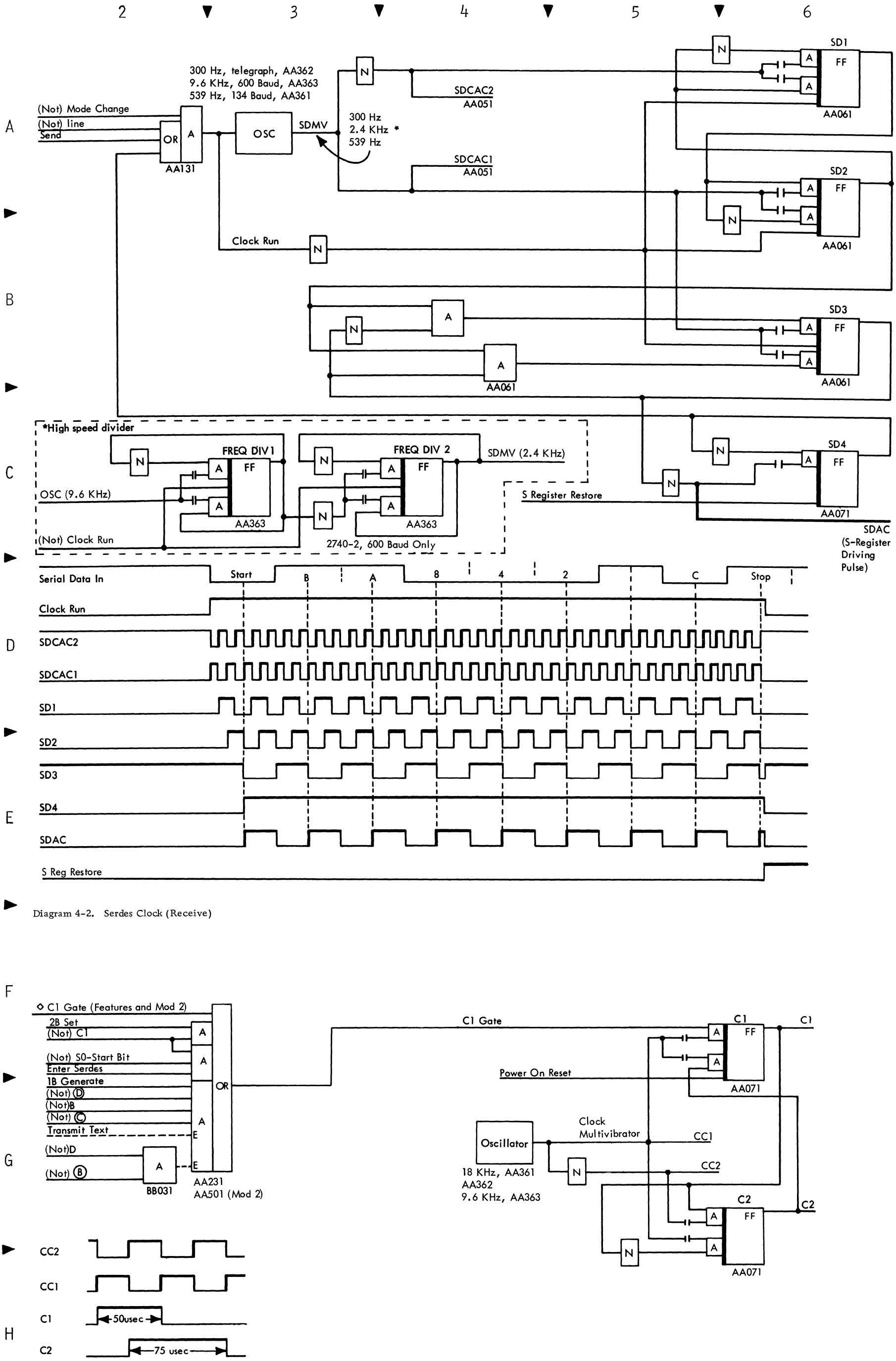
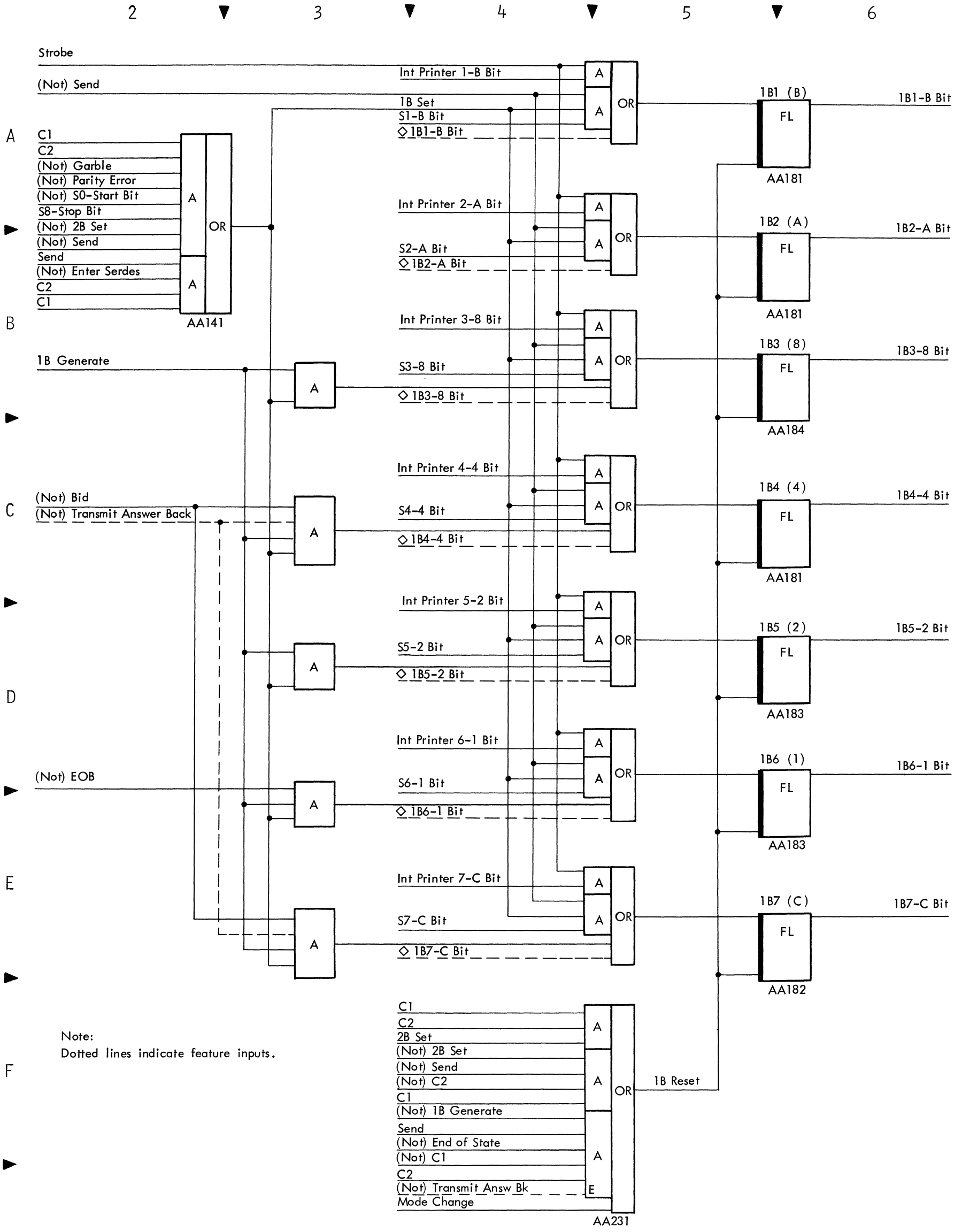


Diagram 4-2. Serdes Clock (Receive)

Note: Timing is slightly slower with 9.6 KHz oscillator. CC pulse duration is approx. 50 microseconds.

Diagram 4-3. Control Clock

Diagram 4-2. Serdes Clock
Diagram 4-3. Control Clock



Note:
Dotted lines indicate feature inputs.

Diagram 4-4. 1B Register (2740-1/2741)

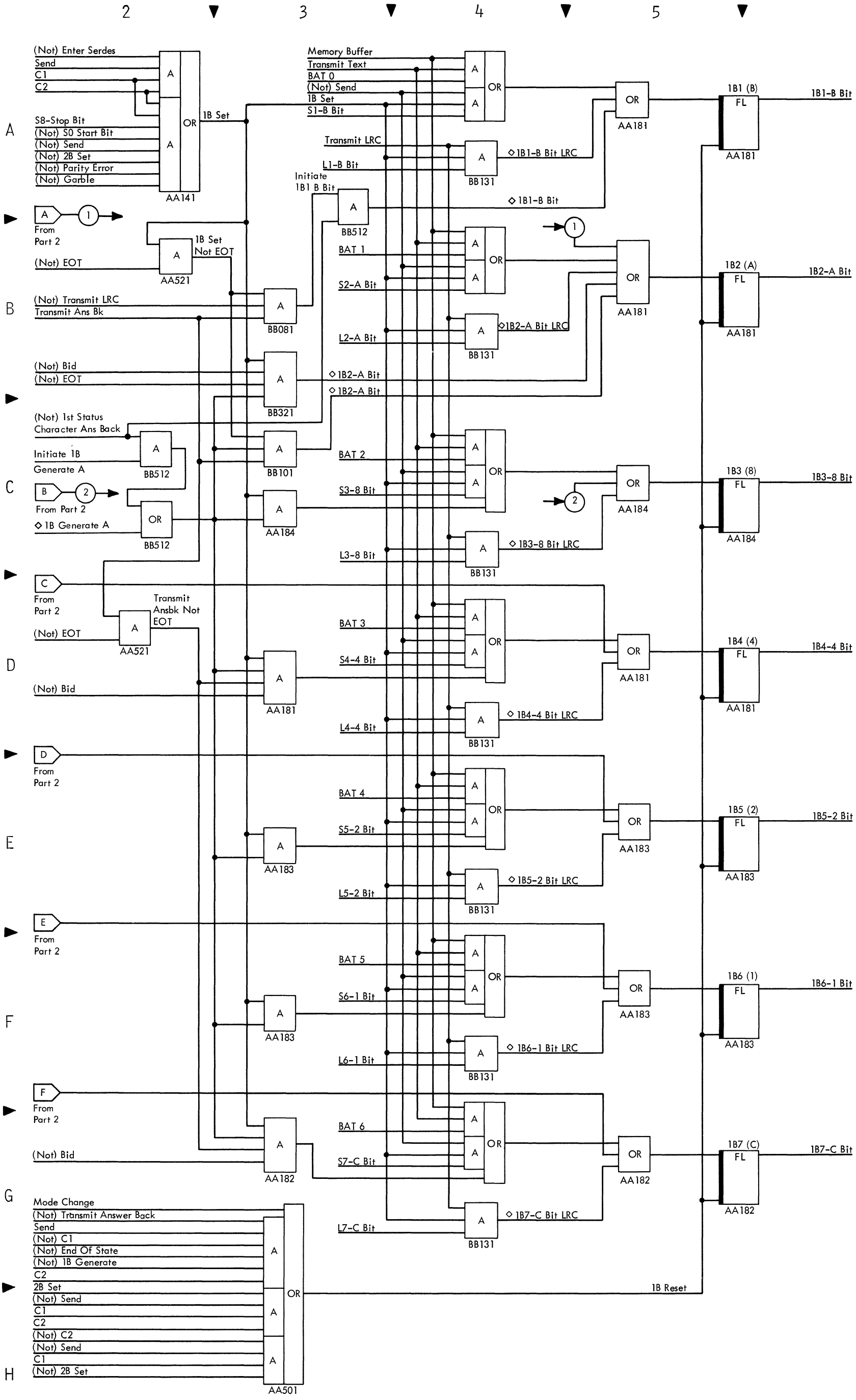
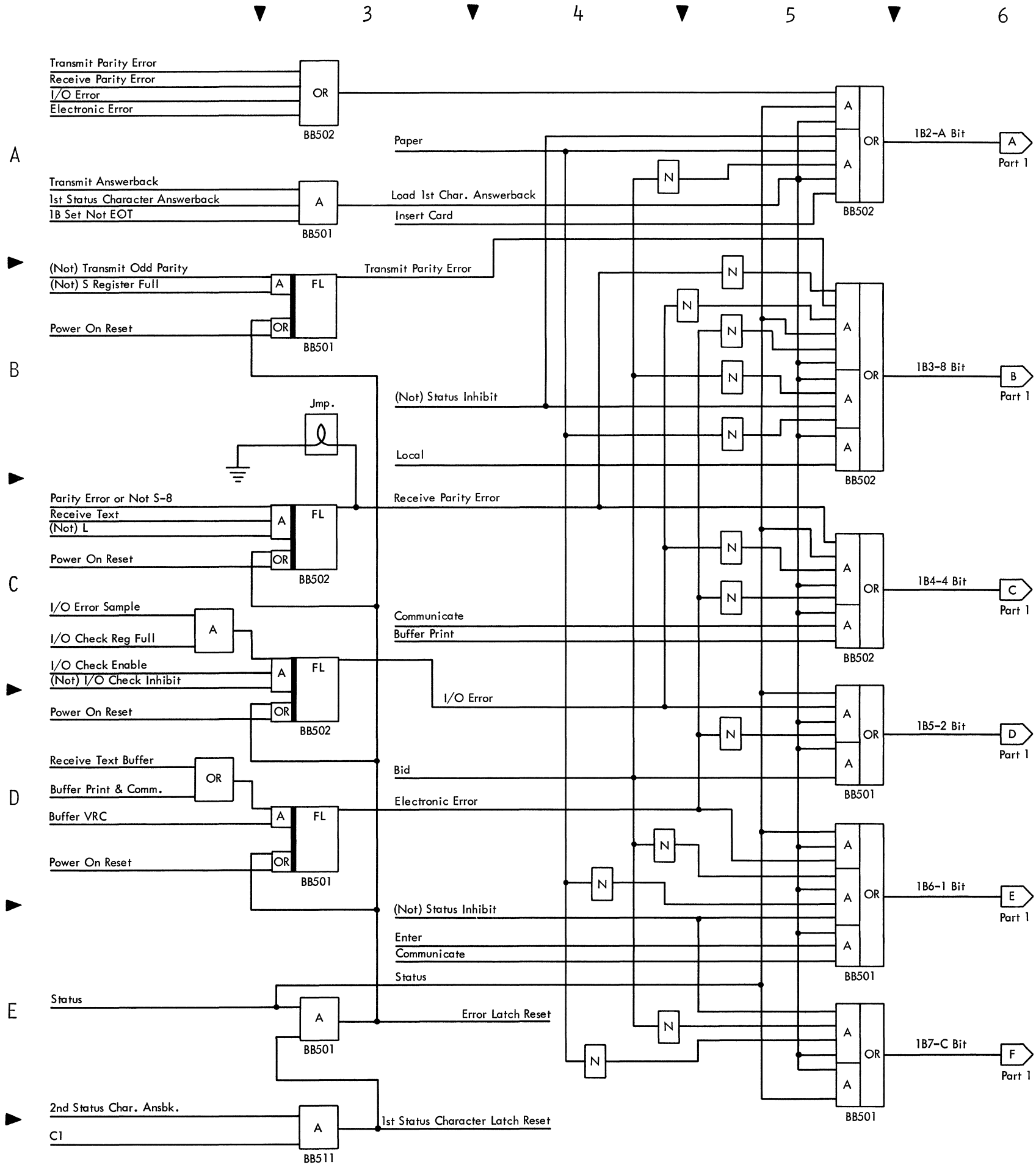


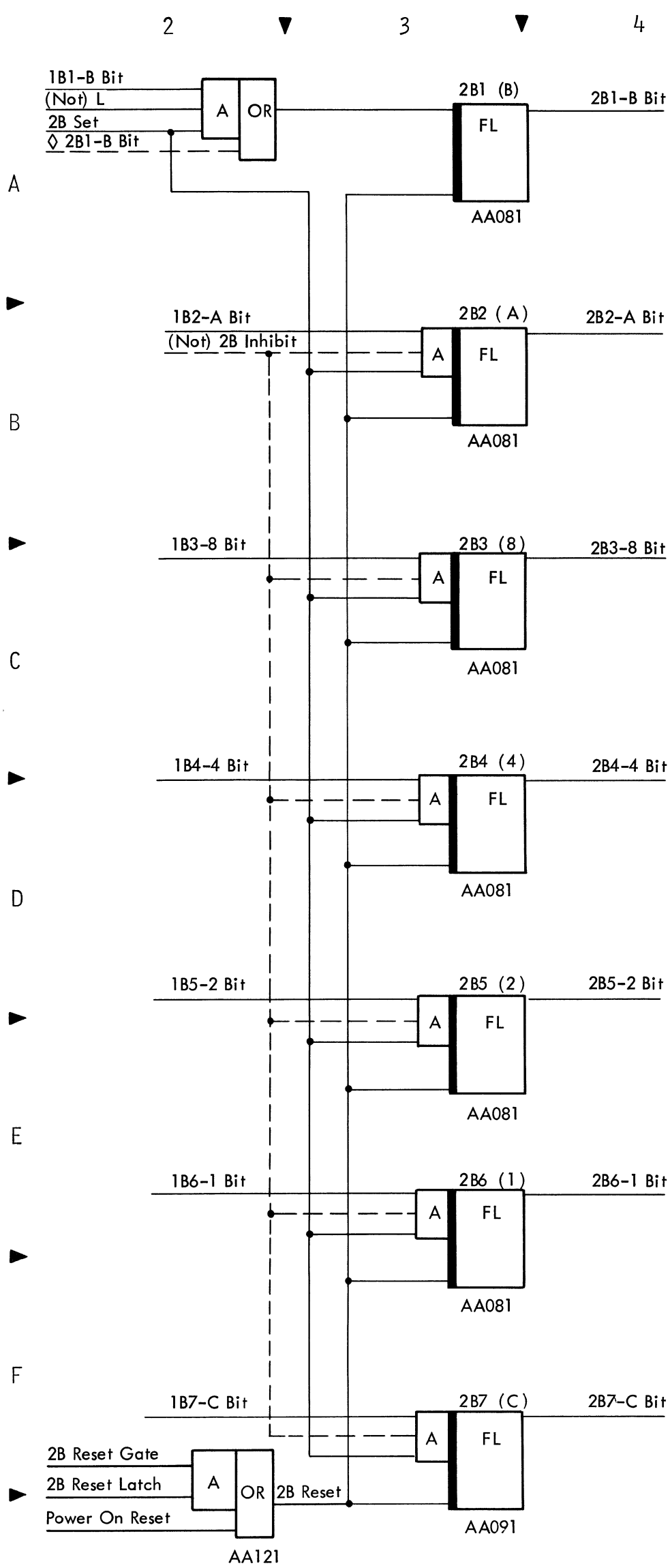
Diagram 4-5. 1B-Register (2740-2) Part 1 of 2



		1st Status Character Set In 1B-Register														
Latches and Bits		1B2 (A)		1B3 (8)			1B4 (4)		1B5 (2)		1B6 (1)			1B7 (C)		Char.	Bit Configuration
Diagram 4-5 AND Blocks		1	2	1	2	3	1	2	1	2	1	2	3	1	2		
Terminal Without Receive Status (Buffer Busy Condition)	Status Inhibit		not		not							not		not		—	———
	Bid Latch		not		not					X		not		not		2	2
	No Paper		not		X							X		X		9	1 8 C
	Insert Device Down		X													@	A
	Local					X										8	8
	Buffer Print							X								4	4
	Communicate							X					X			—	———
	Enter												X			1	1
Terminal With Receive Status	Status	X		X			X		X		X				X	—	Space
	Electronic Error	Ⓧ		not			not		not		X				*	/	A 1 C
	I/O Error	Ⓧ		not			not		X						*	S	A 2 C
	Receive Parity Error	Ⓧ		not			X								*	U	A 4 C
	Trans. Parity Error	Ⓧ		X											*	Y	A 8 C
Load 1st Character Ans. back		X	X	X	X	X	X	X	X	X	X	X	X	X	X	—	———

Note: Ⓧ Any error condition through an OR block with receive status.
* The C Bit is set because the terminal has receive status.

Diagram 4-5. 1B-Register (2740-2) Part 2 of 2



Note: Dotted lines indicate feature inputs.

Diagram 4-6. 2B Register (2740-1/2741)

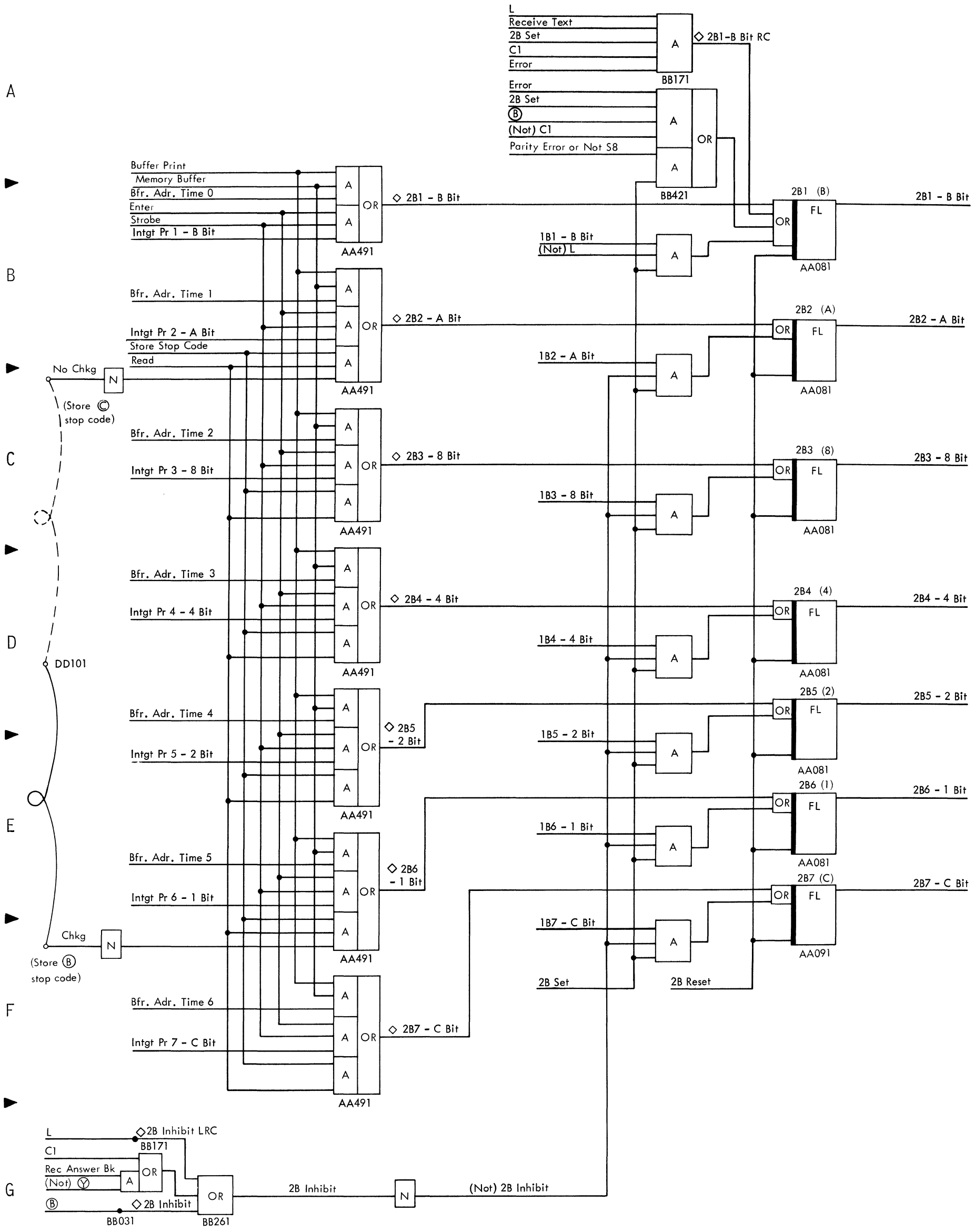
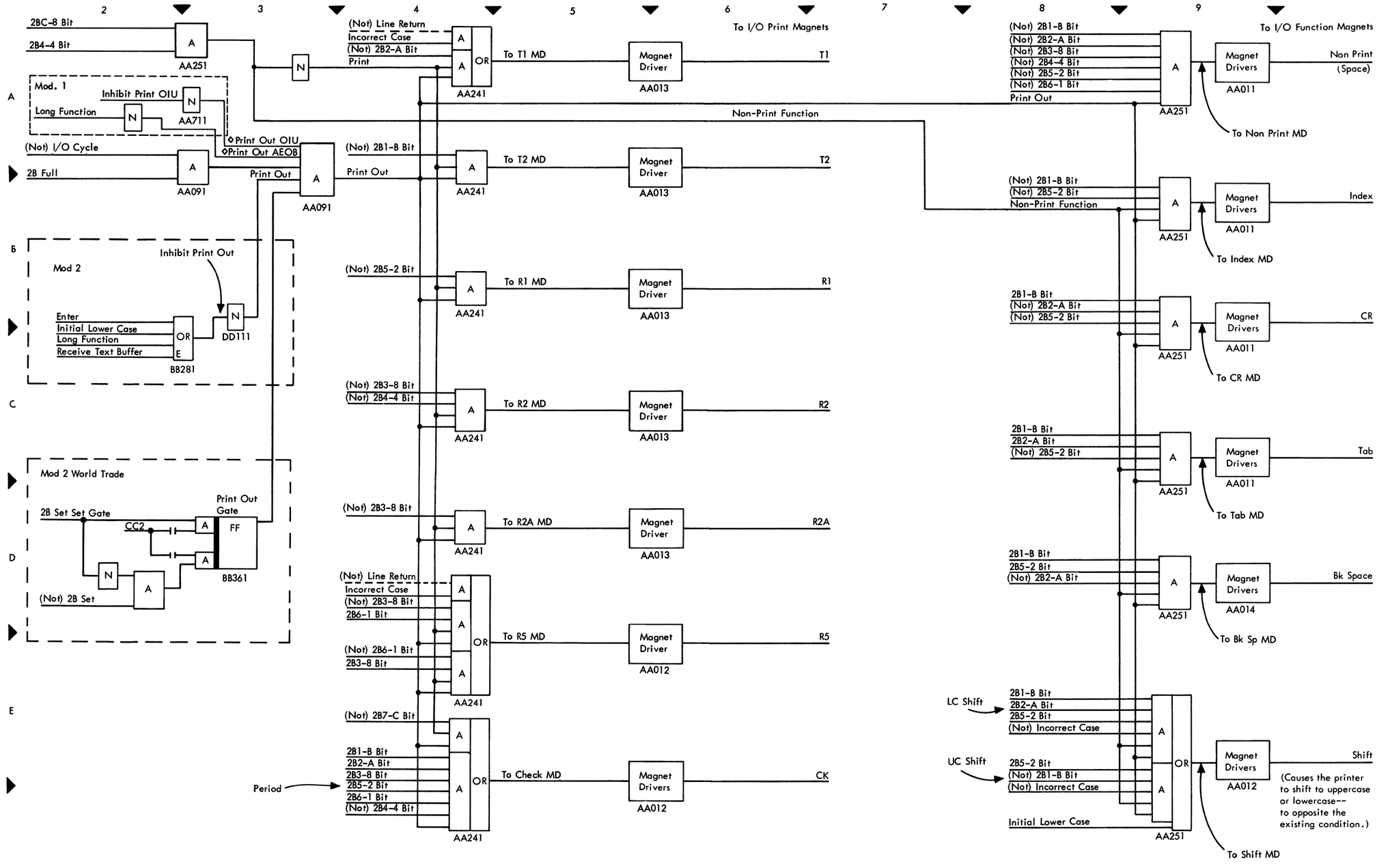
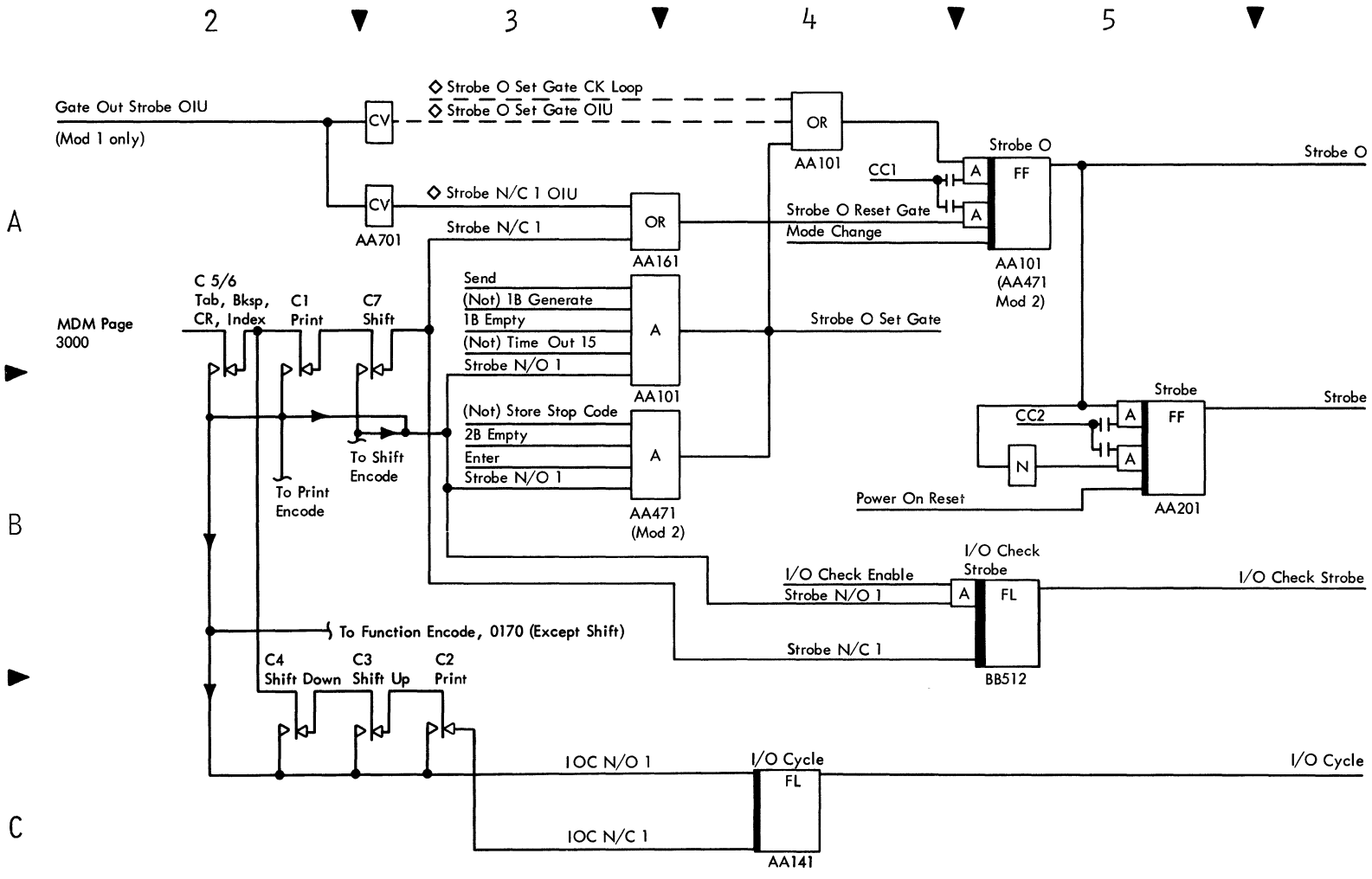


Diagram 4-7. 2B Register (2740-2)

Diagram 4-8. Print and Function Decode





AA141

Operation	Strobe 1	IOC 1
Print	85°-130°	20°-120°
Shift	100°- 120°	35°-145°
Tab, Bksp	55°- 130°	55°- 130°
CR, Index	165°-300°	165°-300°

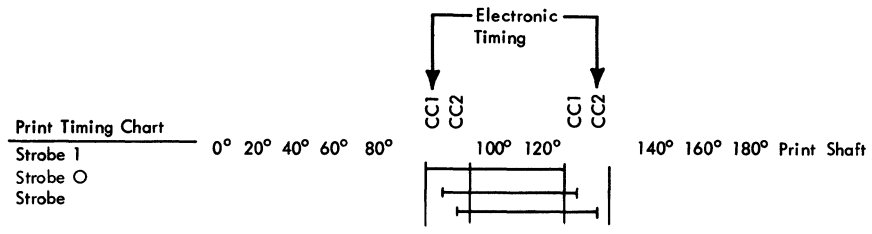


Diagram 4-9. Strobe and I/O Cycle

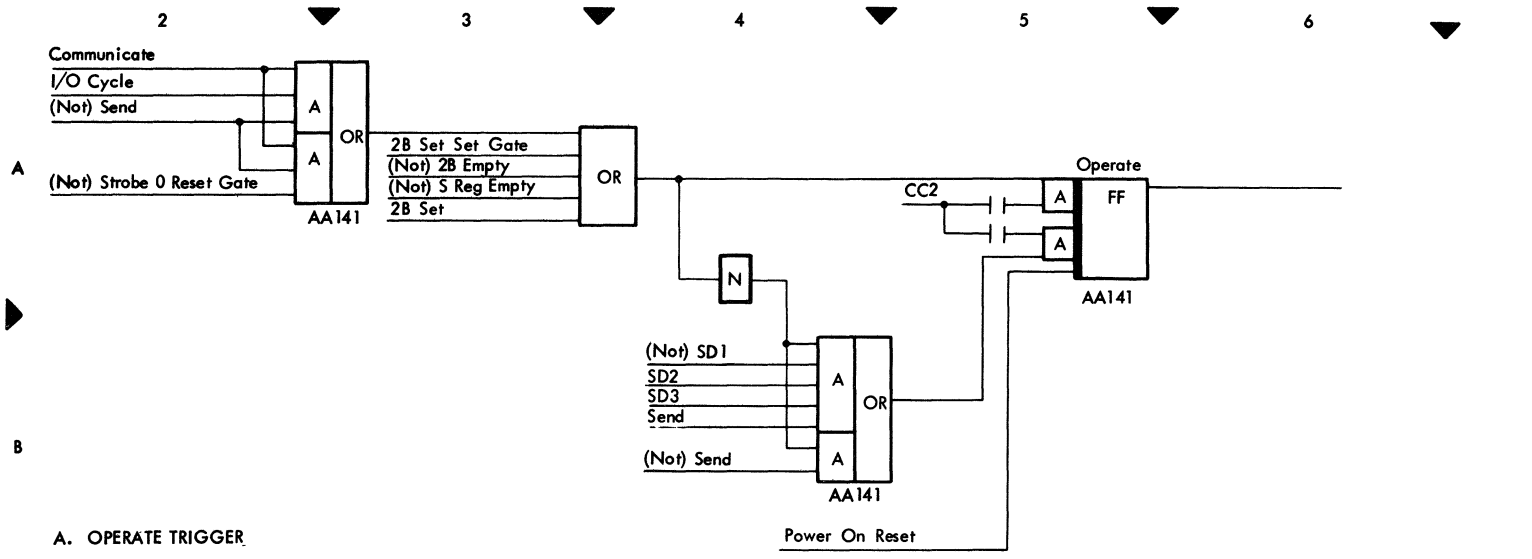
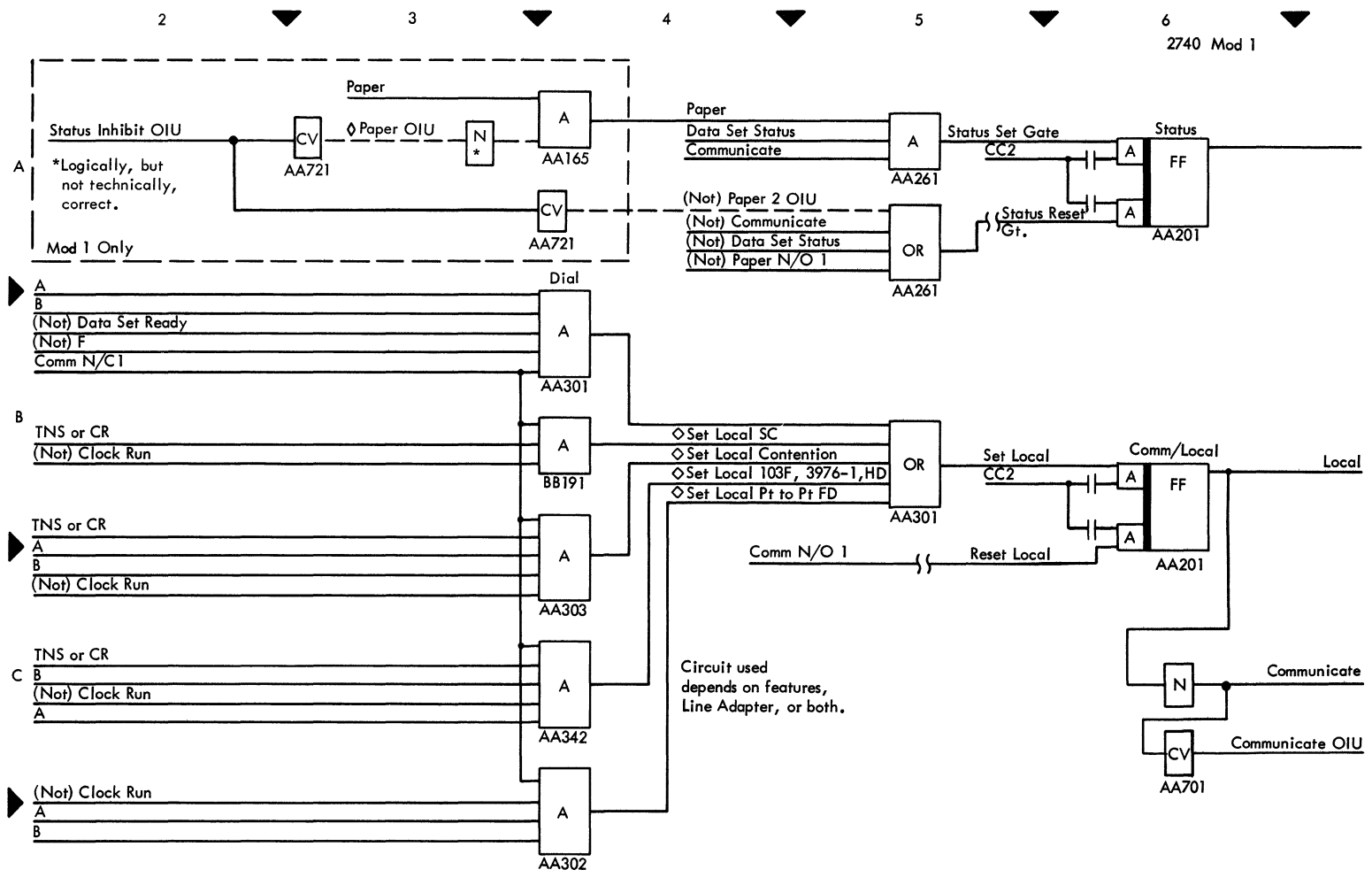


Diagram 4-10. Operate Trigger, Initial Lower Case, I/O Motor Control, Keyboard Lock, and Power-On Reset



Digram 4-11. Local/Communicate, Status (2740-1/2740-2)

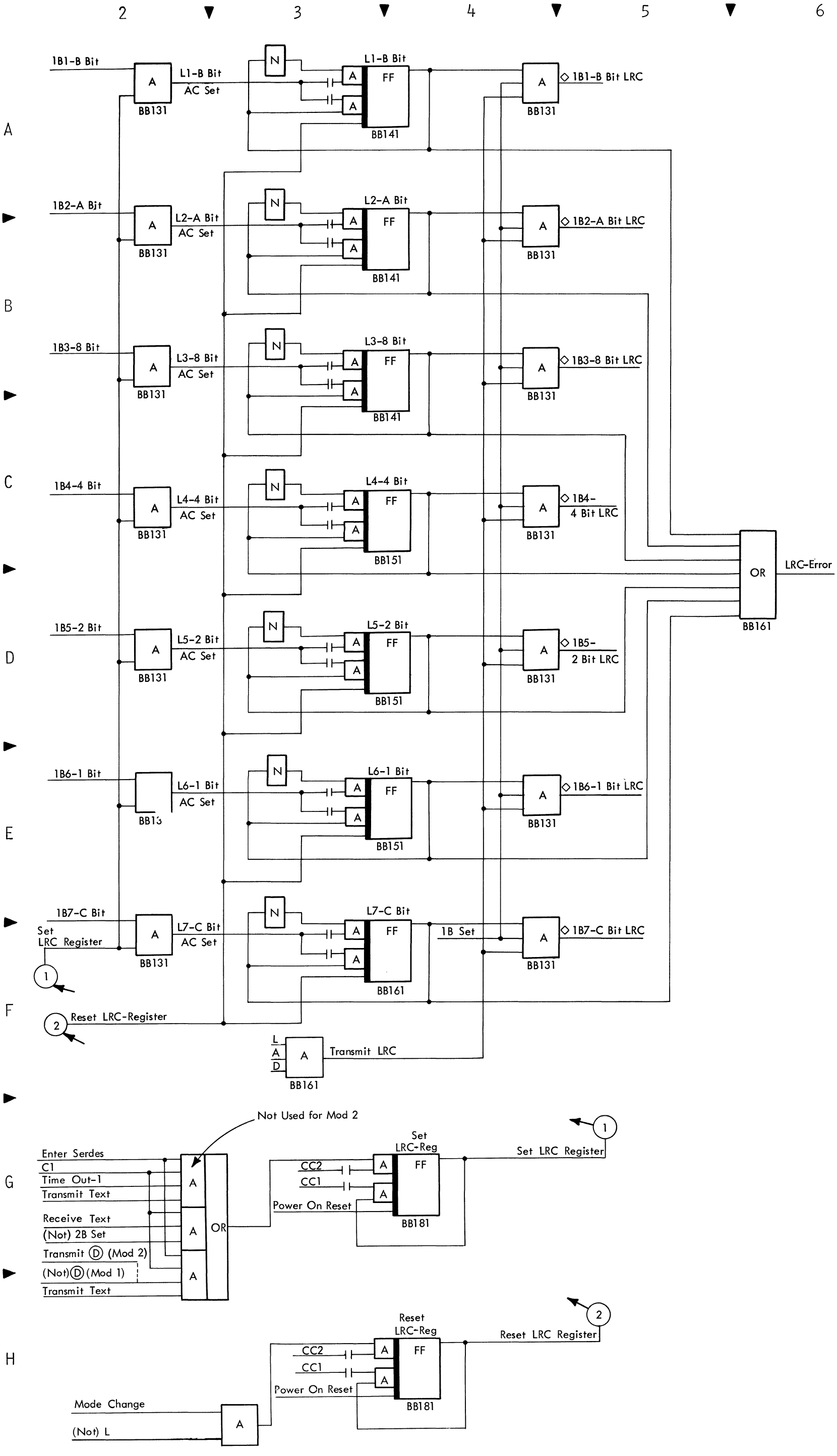


Diagram 4-12. LRC Register

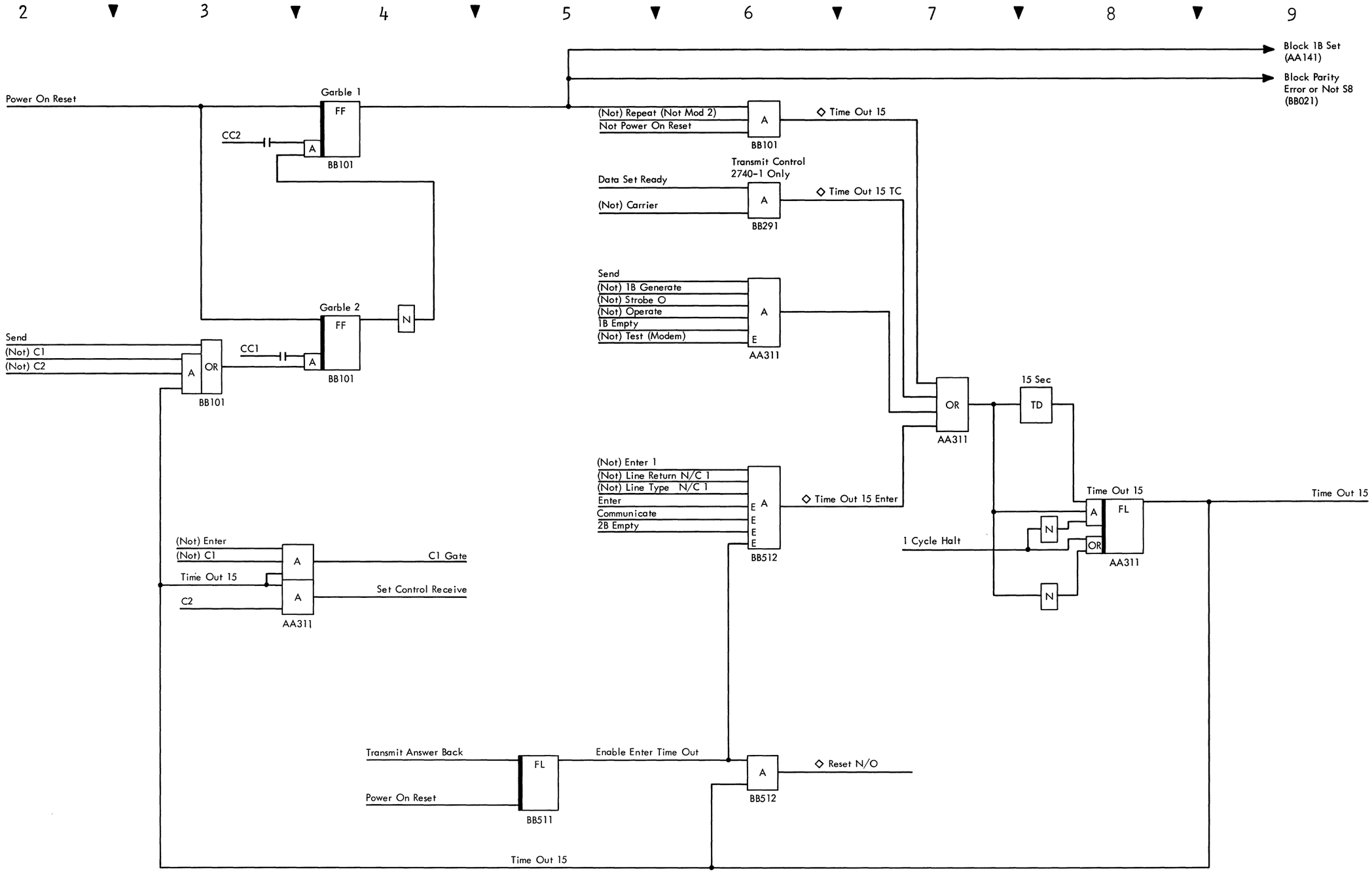
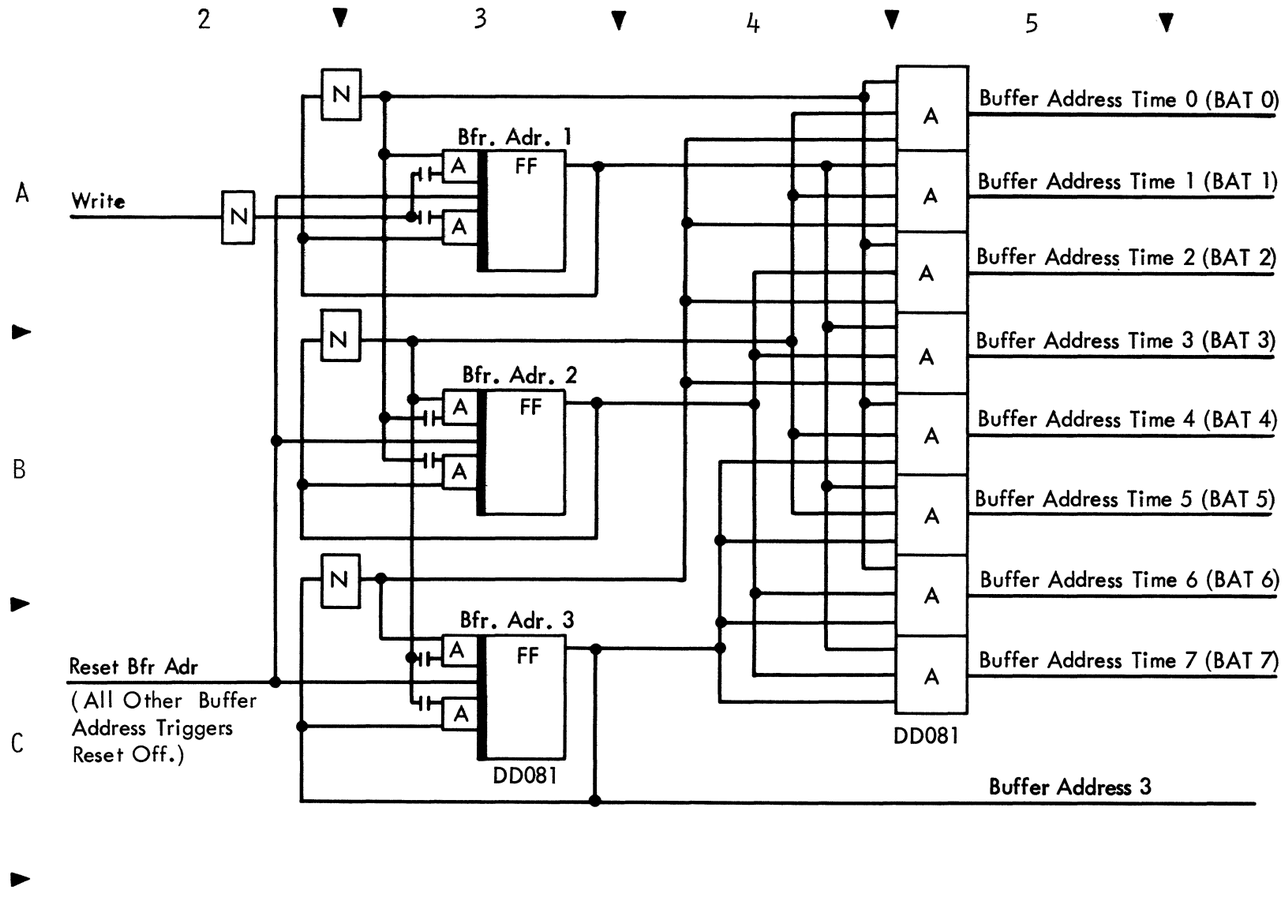
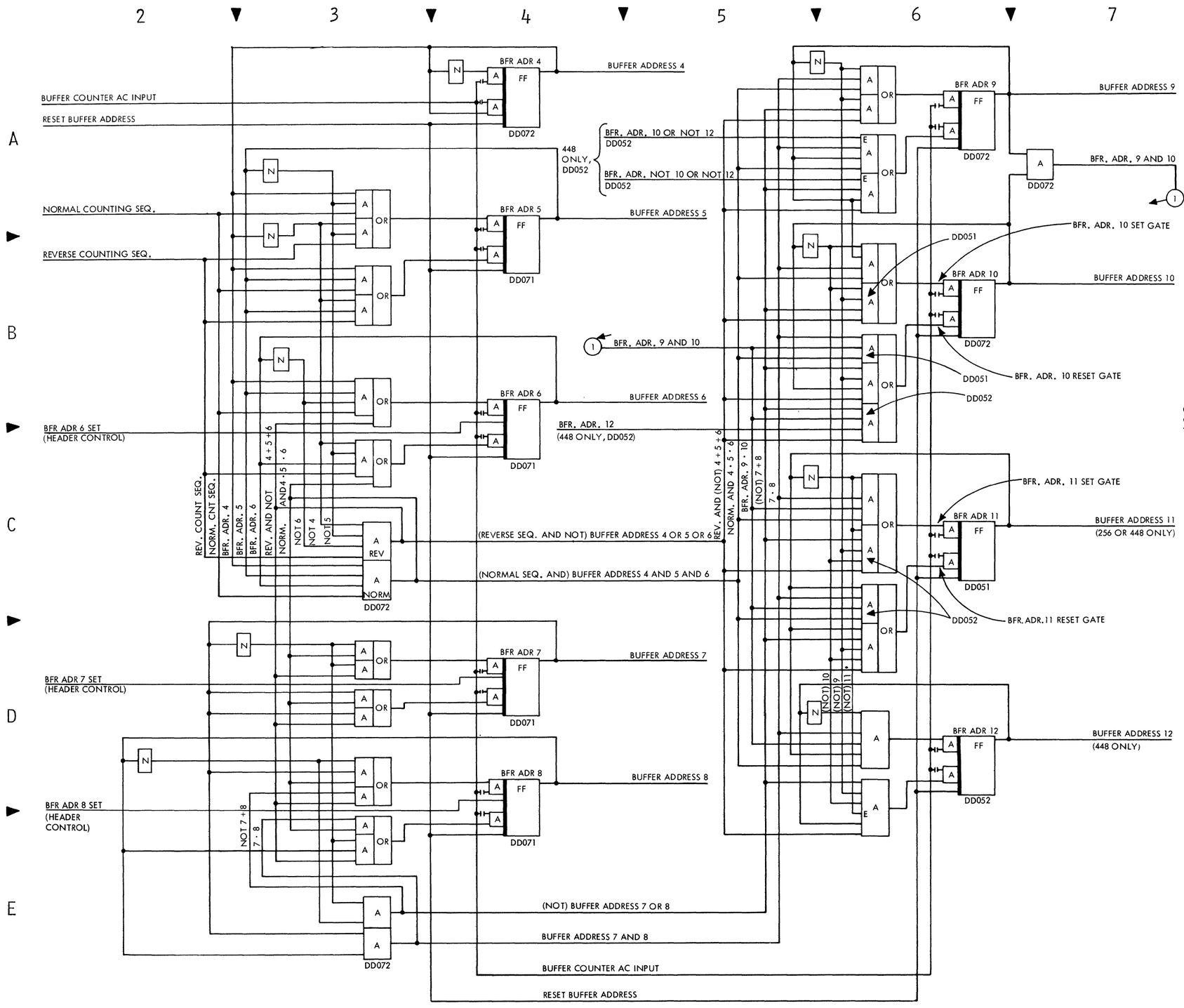

2
3
4
5
6
7
8
9
A
B
C
D
E
Block 1B Set (AA141)
Block Parity Error or Not S8 (BB021)
Power On Reset
Garble 1
FF
CC2
A
BB101
Garble 2
FF
N
CC1
Send
(Not) C1
(Not) C2
A
OR
BB101
(Not) Repeat (Not Mod 2)
Not Power On Reset
A
BB101
◇ Time Out 15
Transmit Control 2740-1 Only
Data Set Ready
(Not) Carrier
A
BB291
◇ Time Out 15 TC
Send
(Not) 1B Generate
(Not) Strobe O
(Not) Operate
1B Empty
(Not) Test (Modem)
A
E
AA311
OR
AA311
15 Sec
TD
(Not) Enter 1
(Not) Line Return N/C 1
(Not) Line Type N/C 1
Enter
Communicate
2B Empty
A
E
E
E
E
BB512
◇ Time Out 15 Enter
Time Out 15
A
FL
OR
N
N
AA311
1 Cycle Halt
Time Out 15
(Not) Enter
(Not) C1
Time Out 15
C2
A
A
AA311
C1 Gate
Set Control Receive
Transmit Answer Back
Power On Reset
FL
BB511
Enable Enter Time Out
A
BB512
◇ Reset N/O
Time Out 15

Diagram 4-14. Bit Counter and Buffer Address Time Decode (2740-2)



Character Cycle

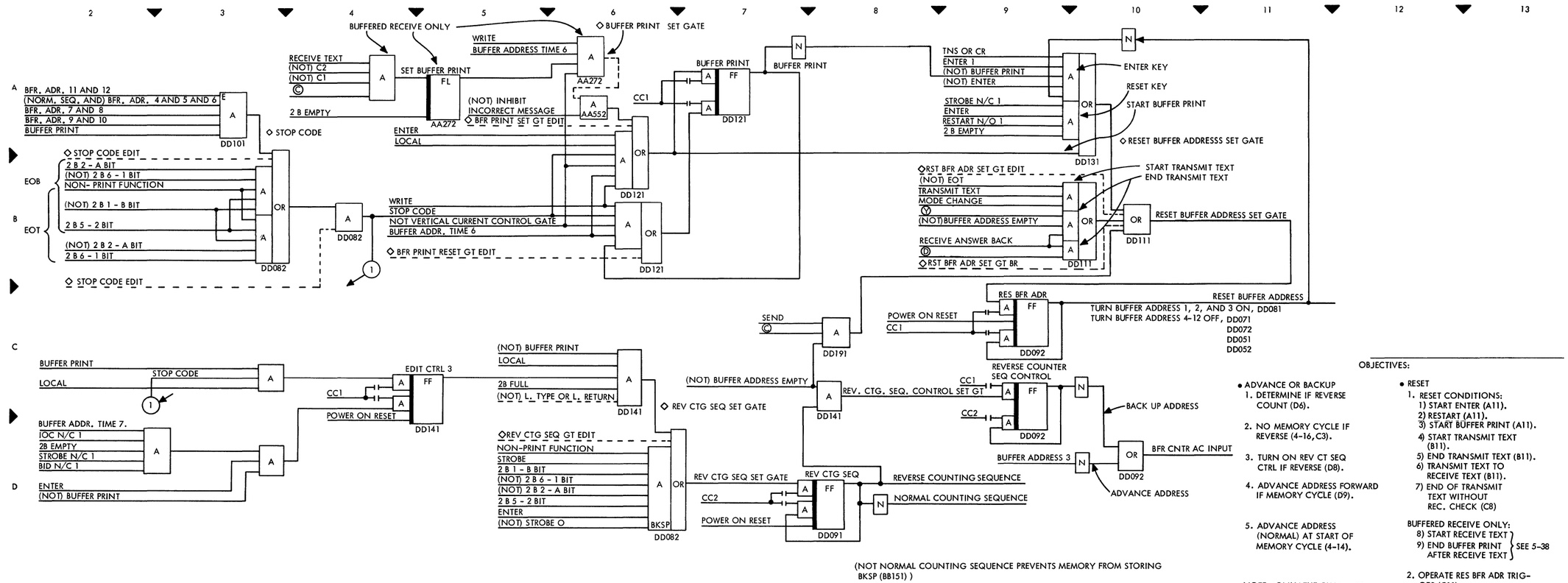
BA3	BA2	BA1	Bfr. Adr. Time	1B or 2B Register
X	X	X	7	-
			0	1
		X	1	2
	X		2	3
	X	X	3	4
X			4	5
X		X	5	6
X	X		6	7
X	X	X	7	-



ADDRESS ADVANCE EXAMPLES, NORMAL AND REVERSE

CHARACTER COUNT	12 256	11 128	10 64	9 32	8 16	7 8	6 4	5 2	4 1	BUFFER ADDRESS TRIGGERS BINARY VALUE
Not Used	–	–	–	–	–	–	–	–	–	0
1	–	–	–	–	–	–	–	–	x	1
2	–	–	–	–	–	–	–	x	–	2
3	–	–	–	–	–	–	–	x	x	3
4	–	–	–	–	–	–	x	–	–	4
5	–	–	–	–	–	–	x	–	x	5
6	–	–	–	–	–	–	x	x	–	6
7	–	–	–	–	–	–	x	x	x	7
8	–	–	–	–	–	x	–	–	–	8
9-14										9-14
15	–	–	–	–	–	x	x	x	x	15
16	–	–	–	–	x	–	–	–	–	16
17-30										17-30
31	–	–	–	–	x	x	x	x	x	31
32	–	–	–	x	–	–	–	–	–	32
33-62										33-62
63	–	–	–	x	x	x	x	x	x	63
64	–	–	x	–	–	–	–	–	–	64
65-126										65-126
127	–	–	x	x	x	x	x	x	x	127
128	–	x	–	–	–	–	–	–	–	128
129-254										129-254
255	–	x	x	x	x	x	x	x	x	255
256	x	–	–	–	–	–	–	–	–	256
257-318										257-318
319	x	–	–	x	x	x	x	x	x	319) SKIP 32 *
320	x	–	x	x	–	–	–	–	–	352)
321-350										353-382
351	x	–	x	x	x	x	x	x	x	383
352	x	x	–	–	–	–	–	–	–	384
353-414										385-446
415	x	x	–	x	x	x	x	x	x	447) SKIP 32 *
416	x	x	x	x	–	–	–	–	–	480)
417-446										481-510
447	x	x	x	x	x	x	x	x	x	511
512										
-32										
-32										
448 MAXIMUM CAPACITY										

* (12 • $\overline{10}$, LEAVE 9 ON (NORMAL)
(12 • 10, LEAVE 9 ON (REVERSE)



OBJECTIVES:

- ADVANCE OR BACKUP
  1. DETERMINE IF REVERSE COUNT (D6).
  2. NO MEMORY CYCLE IF REVERSE (4-16, C3).
  3. TURN ON REV CT SEQ CTRL IF REVERSE (D8).
  4. ADVANCE ADDRESS FORWARD IF MEMORY CYCLE (D9).
  5. ADVANCE ADDRESS (NORMAL) AT START OF MEMORY CYCLE (4-14).

NOTE: ONLY THE CHAR. ADR. REVERSES. THE BIT CTR ALWAYS ADVANCES FORWARD.

- RESET
  1. RESET CONDITIONS:
     1) START ENTER (A11).
     2) RESTART (A11).
     3) START BUFFER PRINT (A11).
     4) START TRANSMIT TEXT (B11).
     5) END TRANSMIT TEXT (B11).
     6) TRANSMIT TEXT TO RECEIVE TEXT (B11).
     7) END OF TRANSMIT TEXT WITHOUT REC. CHECK (C8)

BUFFERED RECEIVE ONLY:
8) START RECEIVE TEXT
9) END BUFFER PRINT AFTER RECEIVE TEXT
} SEE 5-38

2. OPERATE RES BFR ADR TRIGGER (C11).
3. RESET BIT CTR TO BAT 7(4-13) AND CHAR. ADR. TO 0(4-14).

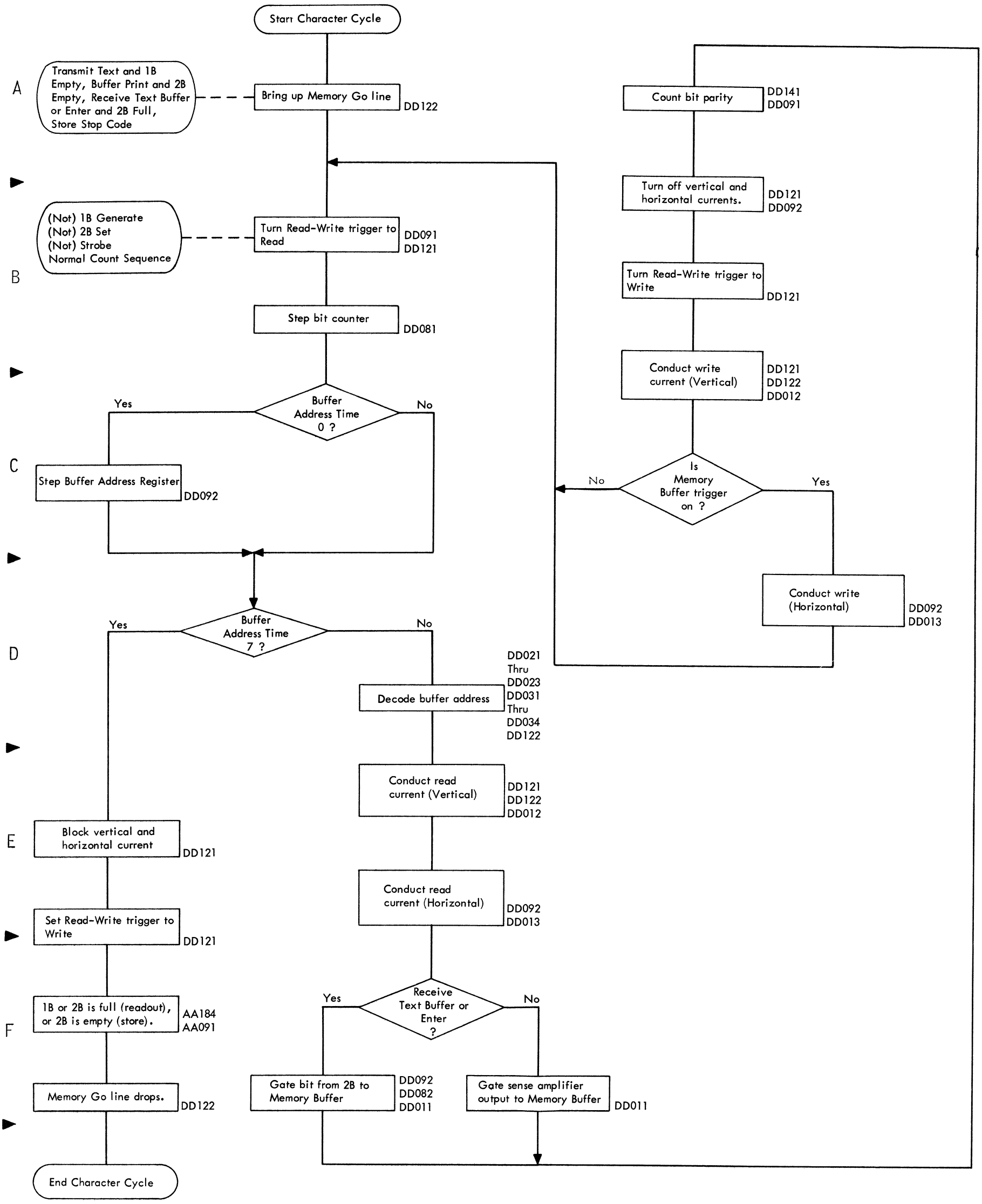
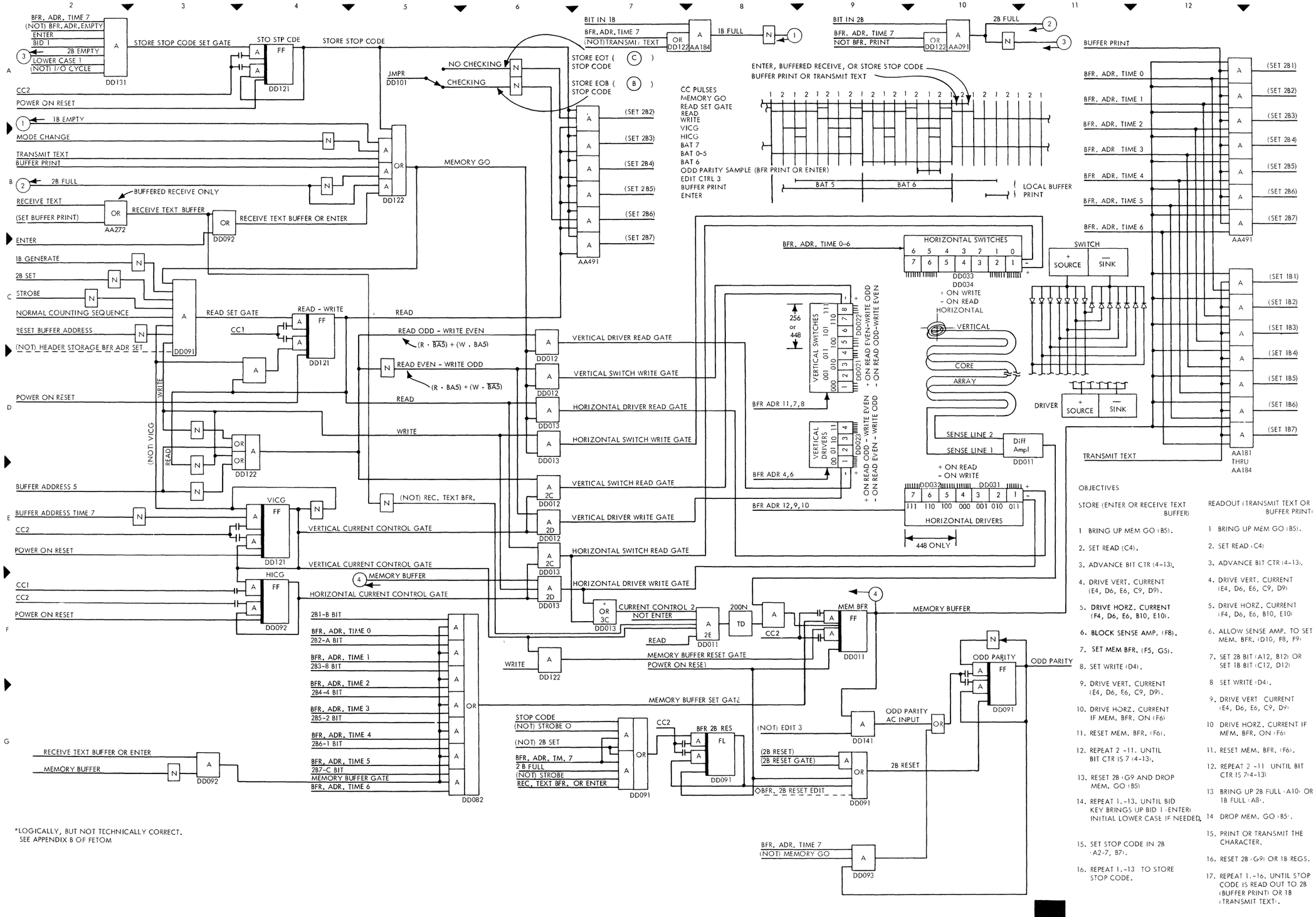


Diagram 4-17. Buffer Storage Operation (2740-2)



*LOGICALLY, BUT NOT TECHNICALLY CORRECT.
SEE APPENDIX B OF FETOM

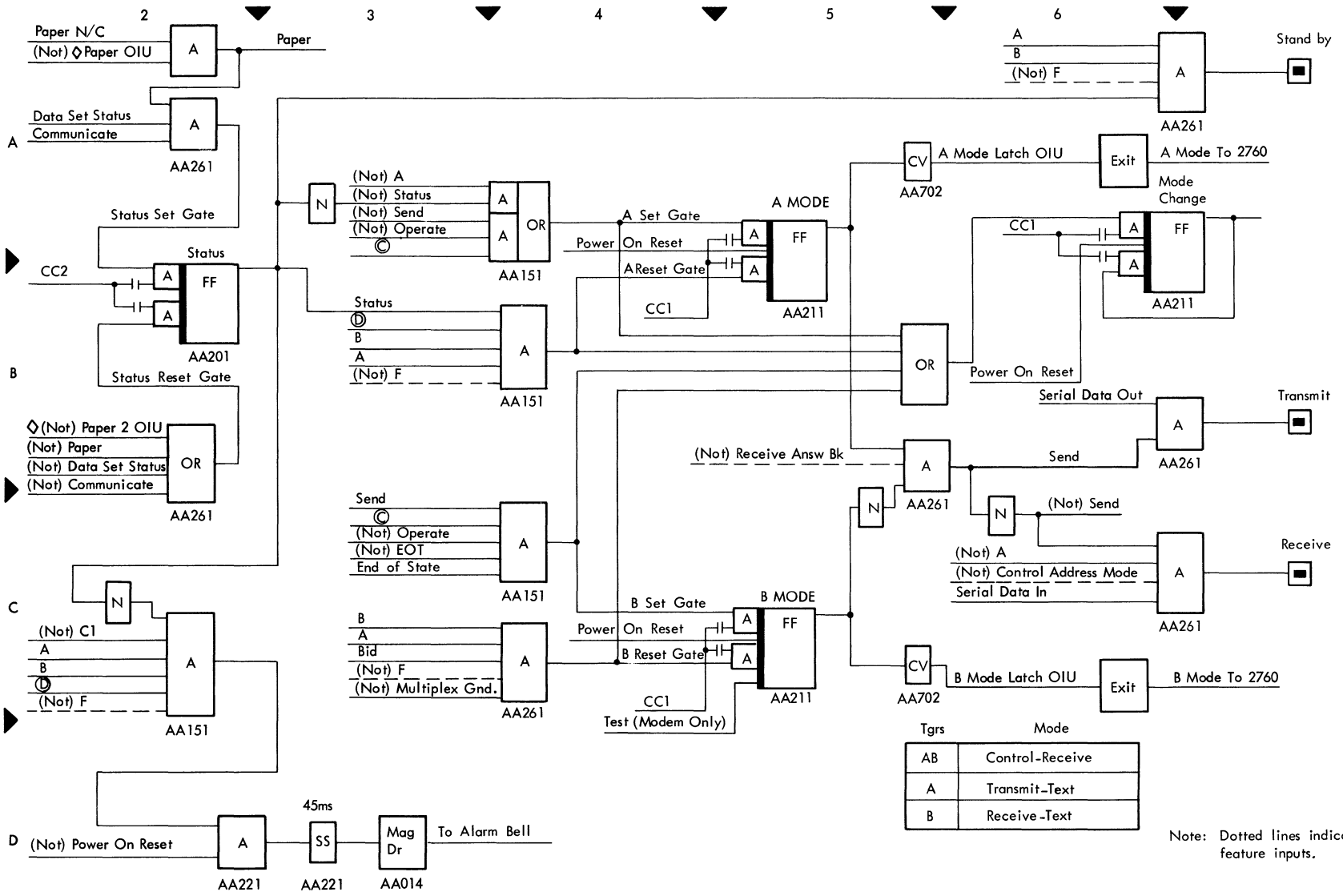
OBJECTIVES

STORE (ENTER OR RECEIVE TEXT BUFFER)

1. BRING UP MEM GO (B5).
2. SET READ (C4).
3. ADVANCE BIT CTR (4-13).
4. DRIVE VERT. CURRENT (E4, D6, E6, C9, D9).
5. DRIVE HORZ. CURRENT (F4, D6, E6, B10, E10).
6. BLOCK SENSE AMP. (F8).
7. SET MEM BFR. (F5, G5).
8. SET WRITE (D4).
9. DRIVE VERT. CURRENT (E4, D6, E6, C9, D9).
10. DRIVE HORZ. CURRENT IF MEM. BFR. ON (F6)
11. RESET MEM. BFR. (F6).
12. REPEAT 2 -11. UNTIL BIT CTR IS 7 (4-13).
13. RESET 2B (G9 AND DROP MEM. GO (B5)
14. REPEAT 1.-13. UNTIL BID KEY BRINGS UP BID 1 (ENTER) INITIAL LOWER CASE IF NEEDED.
15. SET STOP CODE IN 2B (A2-7, B7).
16. REPEAT 1.-13 TO STORE STOP CODE.

READOUT (TRANSMIT TEXT OR BUFFER PRINT)

1. BRING UP MEM GO (B5).
2. SET READ (C4)
3. ADVANCE BIT CTR (4-13).
4. DRIVE VERT. CURRENT (E4, D6, E6, C9, D9)
5. DRIVE HORZ. CURRENT (F4, D6, E6, B10, E10)
6. ALLOW SENSE AMP. TO SET MEM. BFR. (D10, F8, F9)
7. SET 2B BIT (A12, B12) OR SET 1B BIT (C12, D12)
8. SET WRITE (D4).
9. DRIVE VERT CURRENT (E4, D6, E6, C9, D9)
10. DRIVE HORZ. CURRENT IF MEM. BFR. ON (F6)
11. RESET MEM. BFR. (F6).
12. REPEAT 2 -11 UNTIL BIT CTR IS 7 (4-13)
13. BRING UP 2B FULL (A10) OR 1B FULL (A8).
14. DROP MEM. GO (B5).
15. PRINT OR TRANSMIT THE CHARACTER.
16. RESET 2B (G9) OR 1B REGS.
17. REPEAT 1.-16. UNTIL STOP CODE IS READ OUT TO 2B (BUFFER PRINT) OR 1B (TRANSMIT TEXT).



Tgrs	Mode
AB	Control-Receive
A	Transmit-Text
B	Receive-Text

Note: Dotted lines indicate feature inputs.

Diagram 5-1. Mode Triggers (Basic 2740-1)

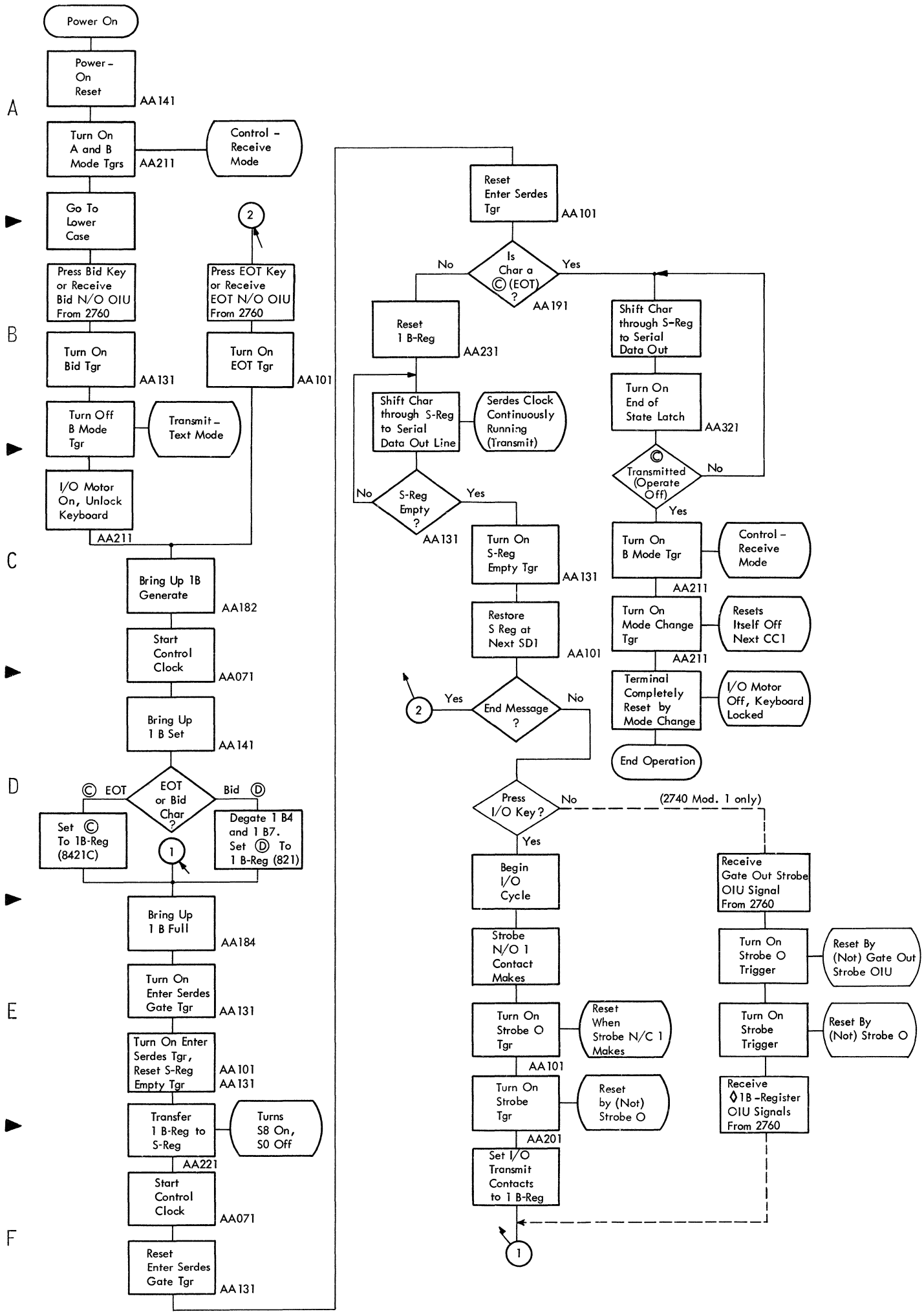
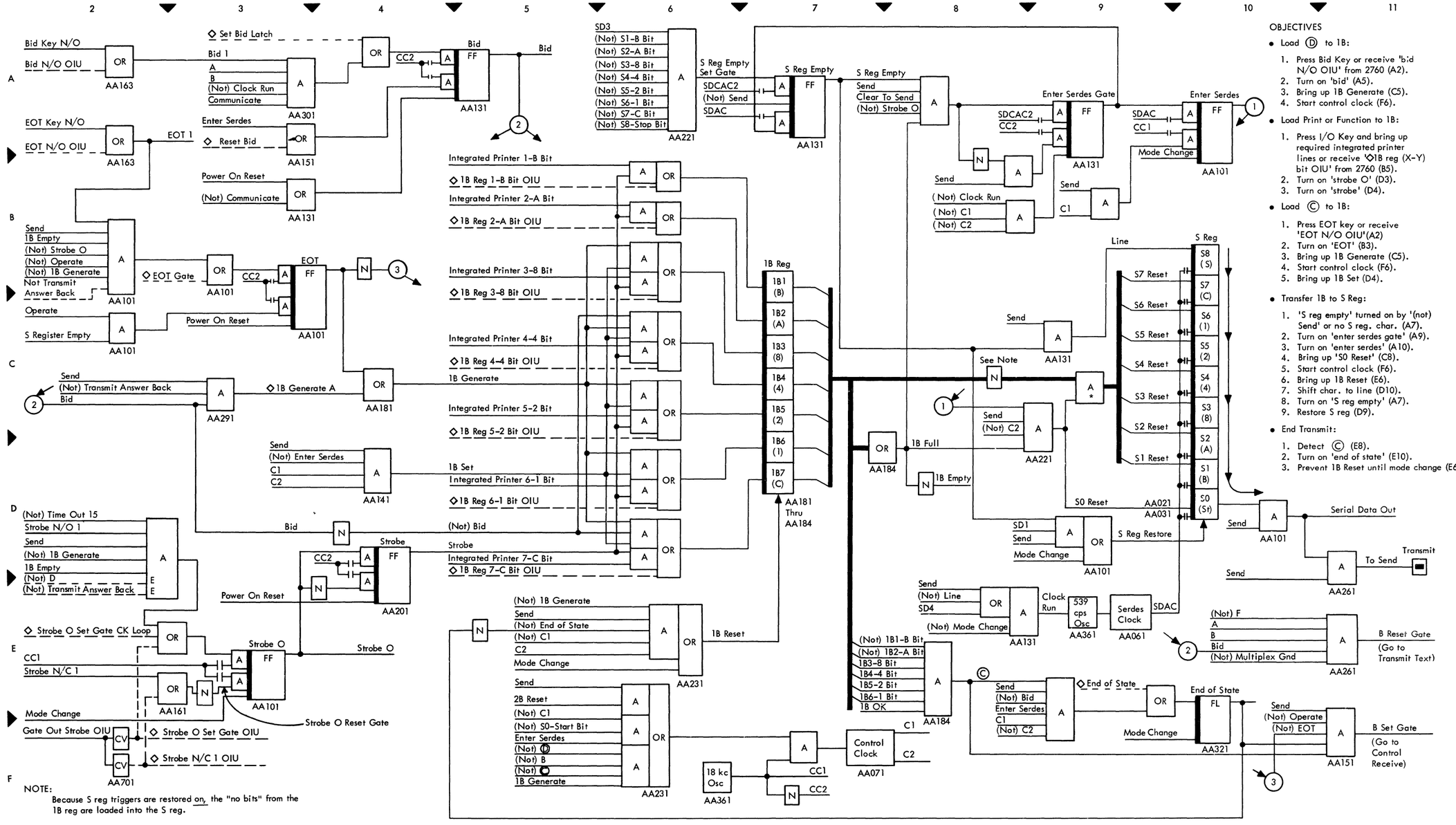


Diagram 5-2. Transmit Flowchart (2740-1/2741)



OBJECTIVES

- Load Ⓓ to 1B:
  1. Press Bid Key or receive 'bid N/O OIU' from 2760 (A2).
  2. Turn on 'bid' (A5).
  3. Bring up 1B Generate (C5).
  4. Start control clock (F6).
- Load Print or Function to 1B:
  1. Press I/O Key and bring up required integrated printer lines or receive '◇1B reg (X-Y) bit OIU' from 2760 (B5).
  2. Turn on 'strobe O' (D3).
  3. Turn on 'strobe' (D4).
- Load Ⓒ to 1B:
  1. Press EOT key or receive 'EOT N/O OIU'(A2)
  2. Turn on 'EOT' (B3).
  3. Bring up 1B Generate (C5).
  4. Start control clock (F6).
  5. Bring up 1B Set (D4).
- Transfer 1B to S Reg:
  1. 'S reg empty' turned on by '(not) Send' or no S reg. char. (A7).
  2. Turn on 'enter serdes gate' (A9).
  3. Turn on 'enter serdes' (A10).
  4. Bring up 'S0 Reset' (C8).
  5. Start control clock (F6).
  6. Bring up 1B Reset (E6).
  7. Shift char. to line (D10).
  8. Turn on 'S reg empty' (A7).
  9. Restore S reg (D9).
- End Transmit:
  1. Detect Ⓒ (E8).
  2. Turn on 'end of state' (E10).
  3. Prevent 1B Reset until mode change (E6).

NOTE:
Because S reg triggers are restored on, the "no bits" from the 1B reg are loaded into the S reg.

*Multiple ANDS.
Dotted Lines indicate feature inputs

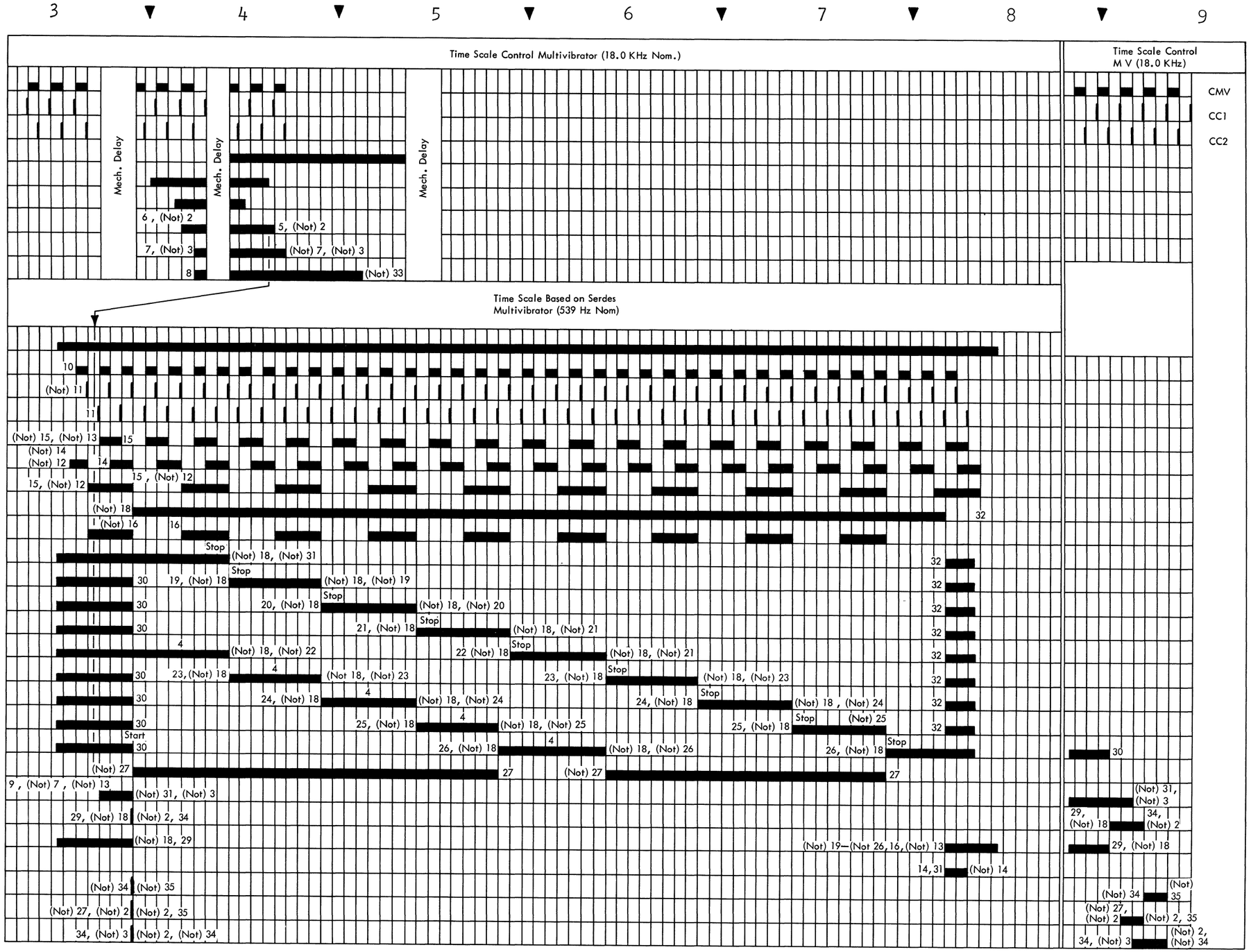
Diagram 5-3. Transmit Logic (2740- 1/2741)

Diagram 5-4. Transmit Timing Chart (Chart 1 of 3)--Transmit Numeral 4

	No.	Signal Name	SP	Logic
	1	CMV	G6J13	AA361
	2	CC1	F7D07 a	AA051
A	3	CC2	F7D04 b	AA051
	4	Intg Printer 4	K1B09	AA162
	5	Strobe N-C 1	J2D06	AA161 *
	6	Strobe N-O 1	J2B09	AA161 *
►	7	Strobe O	E2G07	AA101
	8	Strobe	E4D05	AA201
	9	1B Full	D4B04	AA184
B				
	10	Send	C2G07 c	AA261 ⊛
	11	SDMV	G6J07	AA361
	12	SDCAC 1	G1D05 d	AA052
►	13	SDCAC 2	G1D04 e	AA052
	14	SD1	H2D05	AA061
	15	SD2	H2D04	AA061
	16	SD3	H2D02	AA061
C	17	SD4	H2B07	AA061
	18	SDAC	G1D07 f	AA052
	19	S8 - Stop Bit	H4D07	AA021
	20	S7 - C Bit	H4D10	AA021
►	21	S6 - 1 Bit	H4J11	AA021
	22	S5 - 2 Bit	H4B12	AA021
	23	S4 - 4 Bit	H4G02	AA031
	24	S3 - 8 Bit	H4J13	AA031
D	25	S2 - A Bit	H4G09	AA031
	26	S1 - B Bit	H4J06	AA031
	27	S0 - Start Bit	H4G07	AA031
	28	Serial Data Out	E2G04	AA101
►	29	Enter Serdes Gt	G2D02	AA131
	30	Enter Serdes	E2B09	AA101
	31	S Register Empty	G2B03	AA131
	32	S Register Restore	E2D04	AA101
E	33	1B Reset	D6J07	AA231
	34	C1	H2G04	AA071
	35	C2	H2G07	AA071

SP for 2741
a. F7B07
b. F7B04
c. J4B07
d. F6D05
e. F6D04
f. F6D07

Logic for 2741
* AA163
⊛ AA411

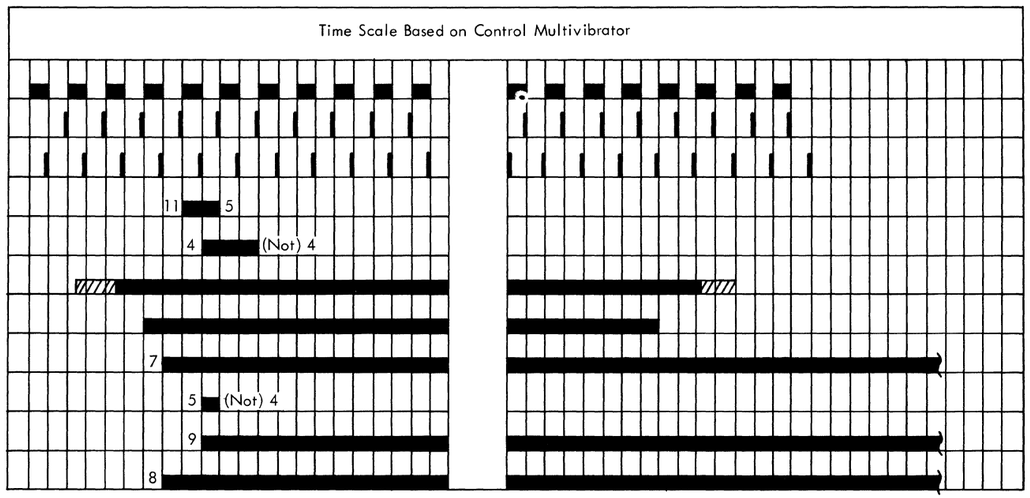


TRANSFER A CHARACTER (NUMERAL 4) FROM KEYBOARD TO 1B, THEN 1B TO SERDES AND TRANSMIT

Diagram 5-4. Transmit Timing Chart (Chart 2 of 3)--Transmit Control Character, and Mode Change (2740)

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

	No.	Signal Name	SP	Logic
A	1	CMV	G6J13	AA361
	2	CC1	F7D07	AA051
	3	CC2	F7D04	AA051
	4	C1	H2G04	AA071
	5	C2	H2G07	AA071
►	6	Button N-C	*	*
	7	EOB 1 or EOT 1	*	*
	8	Function	*	*
B	9	1B Set	J6G08	AA141
	10	1B Full	D4B04	AA184
	11	1B Generate	E6B12	AA182
►				



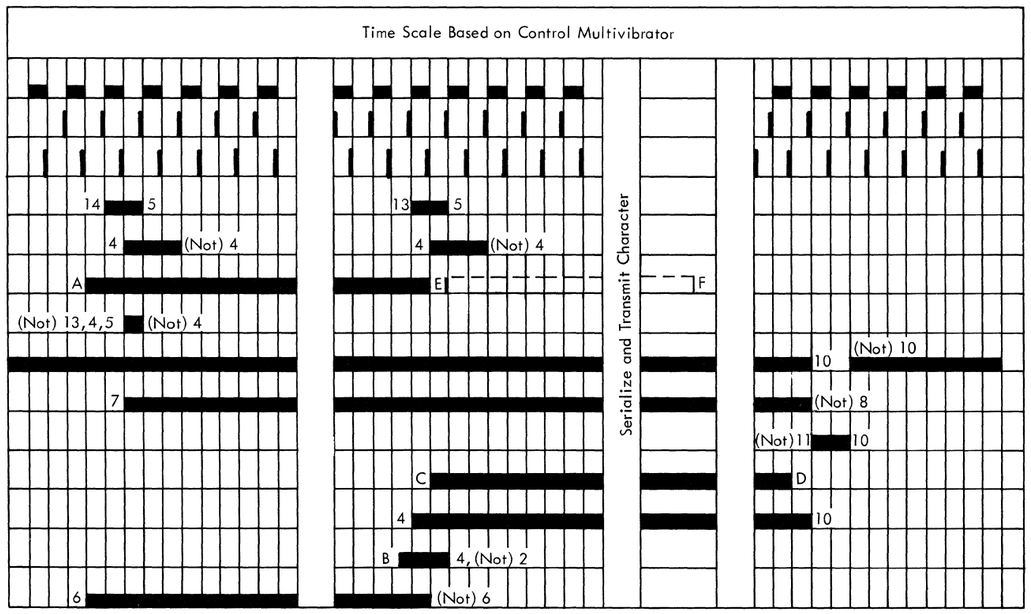
TRANSFER A CHARACTER FROM OPERATOR CONTROL BUTTON TO 1B.

* No.	Signal Name	SP	Logic
6	EOB N-C	J3J13	BB041
7	EOB-1	H2J09	BB051
7a	EOT-1	K3B09	AA163
8	EOB	J3J02	BB041
8a	EOT	E2J06	AA101

⌑

No.	Signal Name	SP	Logic
6	EOB	J3J02	BB041
6a	EOT	E2J06	AA101

	No.	Signal Name	SP	Logic
C	1	CMV	G6J13	AA361
	2	CC1	F7D07	AA051
►	3	CC2	F7D04	AA051
	4	C1	H2G04	AA071
	5	C2	H2G07	AA071
D	6	Function	⌑	⌑
	7	1B Set	J6G08	AA141
	8	1B Reset	D6J07	AA231
	9	1B Full	D4B04	AA184
►	10	Mode Change	E4J02	AA211
	11	Operate	J6J11	AA141
	12	End of State	F6D11	AA321
E	13	Enter Serdes	E2B09	AA101
	14	1B Generate	E6B12	AA182



TRANSMIT A CONTROL CHARACTER - THEN CHANGE MODES AFTER TRANSMISSION.

A. Function (as 6, 6a) Set 1 as in Signal 8 above.
Note - This Timing Chart is a continuation of above chart-i.e. Transfer Control Character from Keybutton to 1B to S Register and Transmit.

B. 1B Full and (not) SDCAC2 Set Enter Serdes Gate-Enter Serdes 'Gate and SDAC Set Enter Serdes.

C. Operate is Set when S Register Empty (not shown) is reset -i.e. Character Entered into S Register.

D. Operate is Reset by S Register Empty, SD3,SD2, and (not) SD1-i.e. At End of Serialize Character.

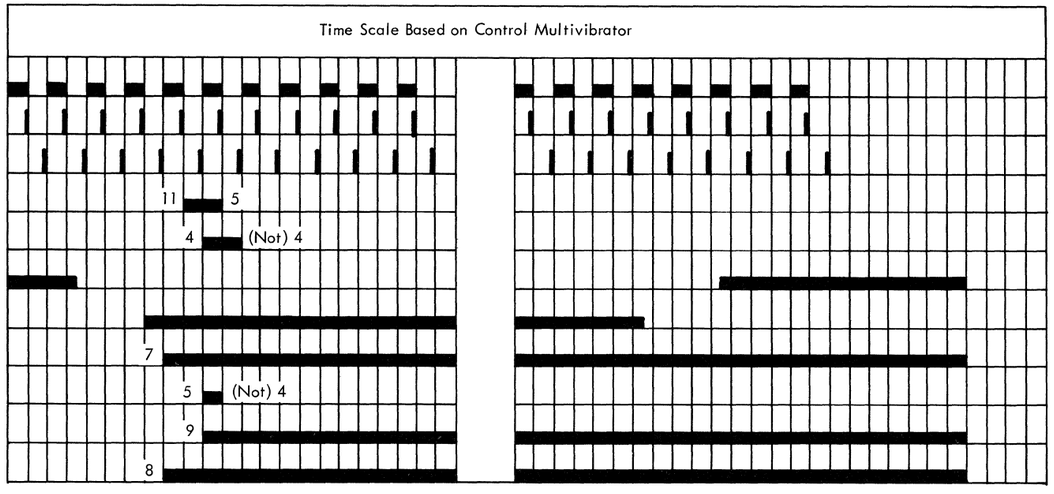
E. Function (as EOB) Reset to Zero on 13.

F. Function (as EOT) Reset when S Register Empty is set (not shown).

Diagram 5-4. Transmit Timing Chart (Chart 3 of 3)--Transmit Control Character, and Mode Change (2741)

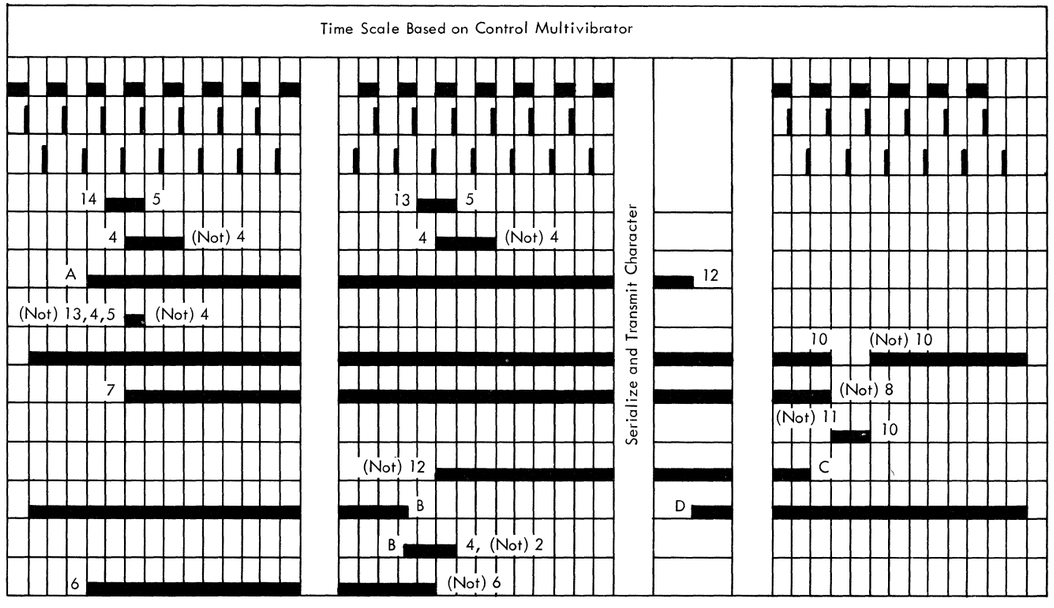
2 3 4 5 6 7 8 9

	No.	Signal Name	SP	Logic
	1	CMV	G6J13	AA361
A	2	CC1	F7B07	AA051
	3	CC2	F7B04	AA051
	4	C1	H2G04	AA071
	5	C2	H2G07	AA071
►	6	Attn 2	L3B09	AA171
	7	Attn 1	L3B07	AA171
	8	EOT	E2J06	AA101
B	9	1B Set	J6G08	AA141
	10	1B Full	D4B04	AA184
	11	1B Generate	E6B12	AA182



TRANSFER A CHARACTER FROM OPERATOR CONTROL BUTTON TO 1B.

	No.	Signal Name	SP	Logic
	1	CMV	G6J13	AA361
	2	CC1	F7B07	AA051
►	3	CC2	F7B04	AA051
	4	C1	H2G04	AA071
	5	C2	H2G07	AA071
	6	EOT	E2J06	AA101
D	7	1B Set	J6G08	AA141
	8	1B Reset	D6J07	AA231
	9	1B Full	D4B04	AA184
►	10	Mode Change	E4J02	AA211
	11	Operate	J6J11	AA141
	12	S Reg. Empty	G2B03	AA131
	13	Enter Serdes	E2B09	AA101
E	14	1B Generate	E6B12	AA182



TRANSMIT A CONTROL CHARACTER - THEN CHANGE MODES AFTER TRANSMISSION.

A. EOT is Set as in Signal 8 Above.
Note: This Timing Chart is a Continuation of Above Chart - i.e. Transfer Control Character From Keybutton to 1B to S Register and Transmit

B. 1B Full and (not) SDCAC2 Set Enter Serdes Gate - Enter Serdes Gate and SDAC Set Enter Serdes and Also Resets S Register Empty.

C. Operate is Reset by S Register Empty, SD3, SD2, and (not) SD1-i.e. At End of Serialize Character

D. S Register Empty is Set by SD3 and SDCAC2 Negative Shift after S1 Thru S8 are restored (see Sheet 1)

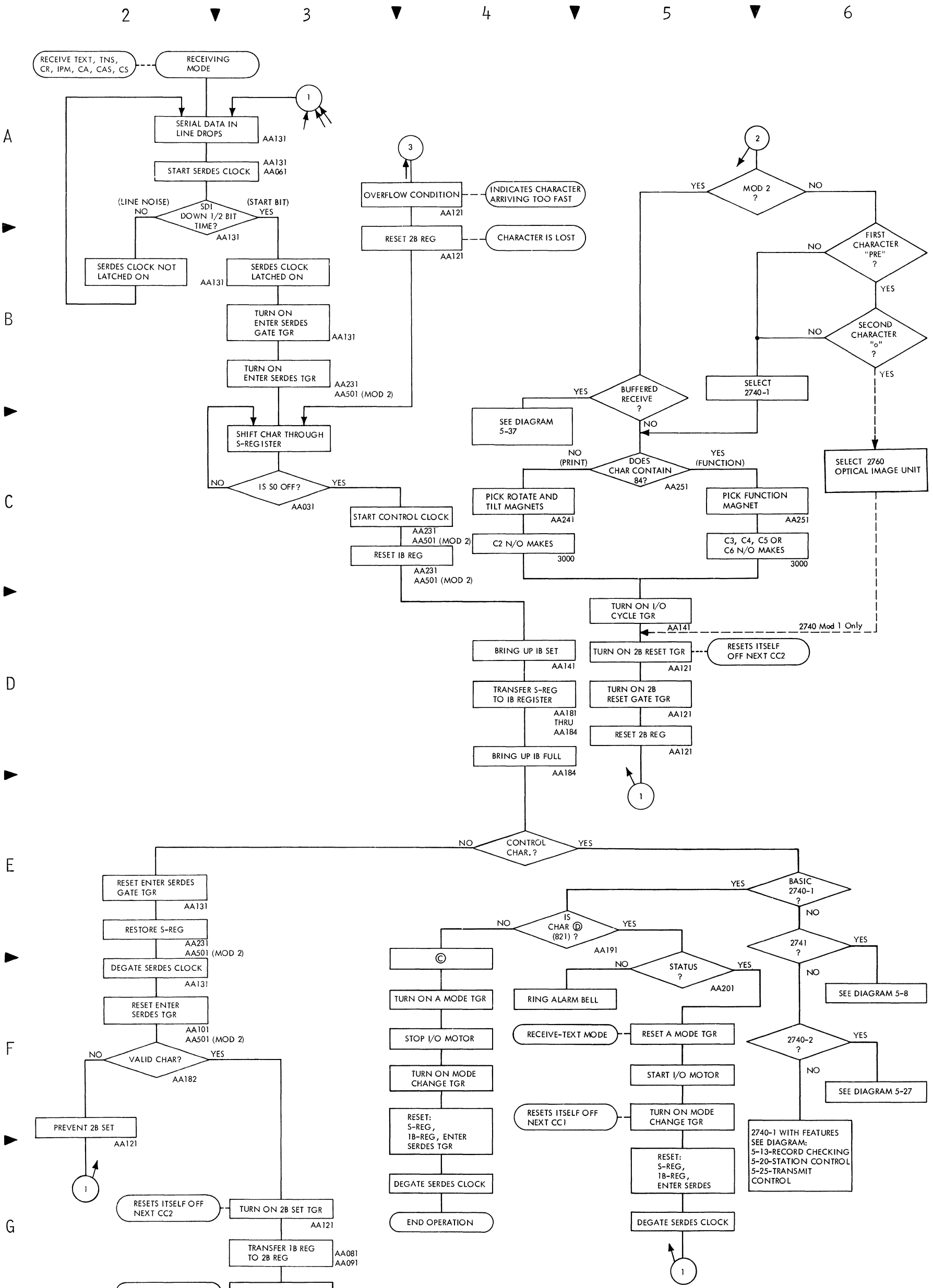
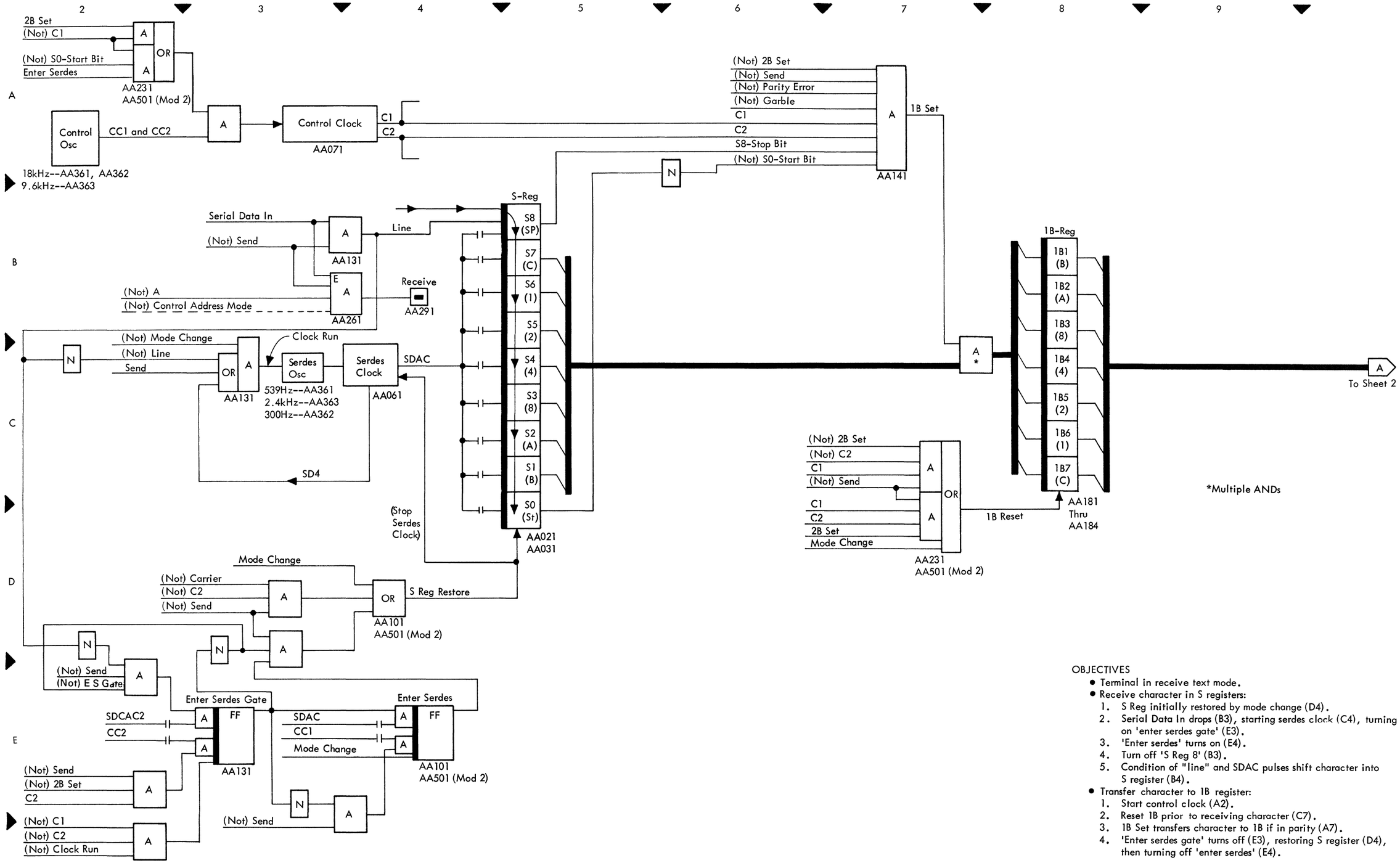


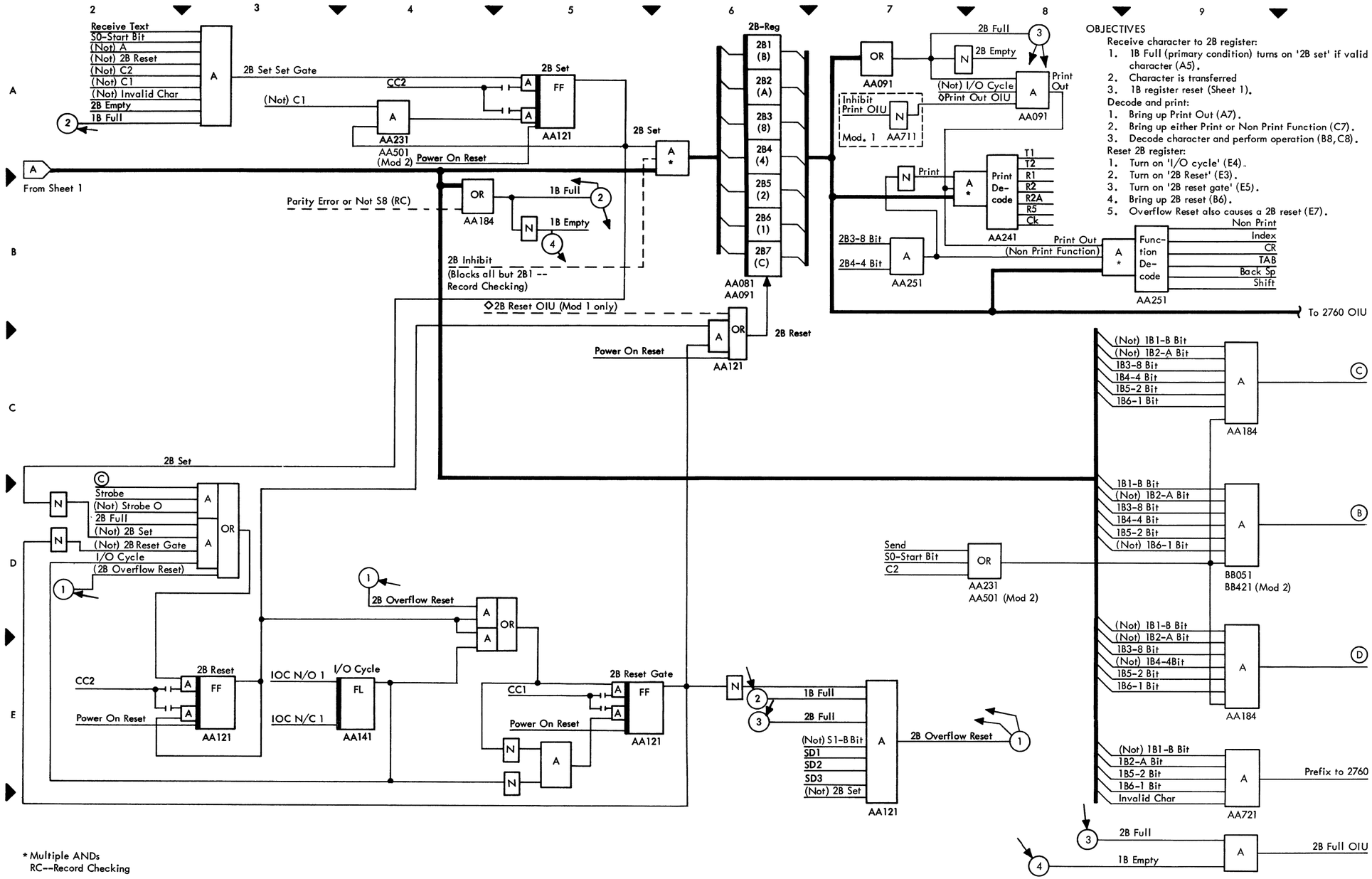
Diagram 5-5. Receive Flowchart (All Terminals)

Diagram 5-6. Receive, Part 1 of 2 (All Terminals)



OBJECTIVES

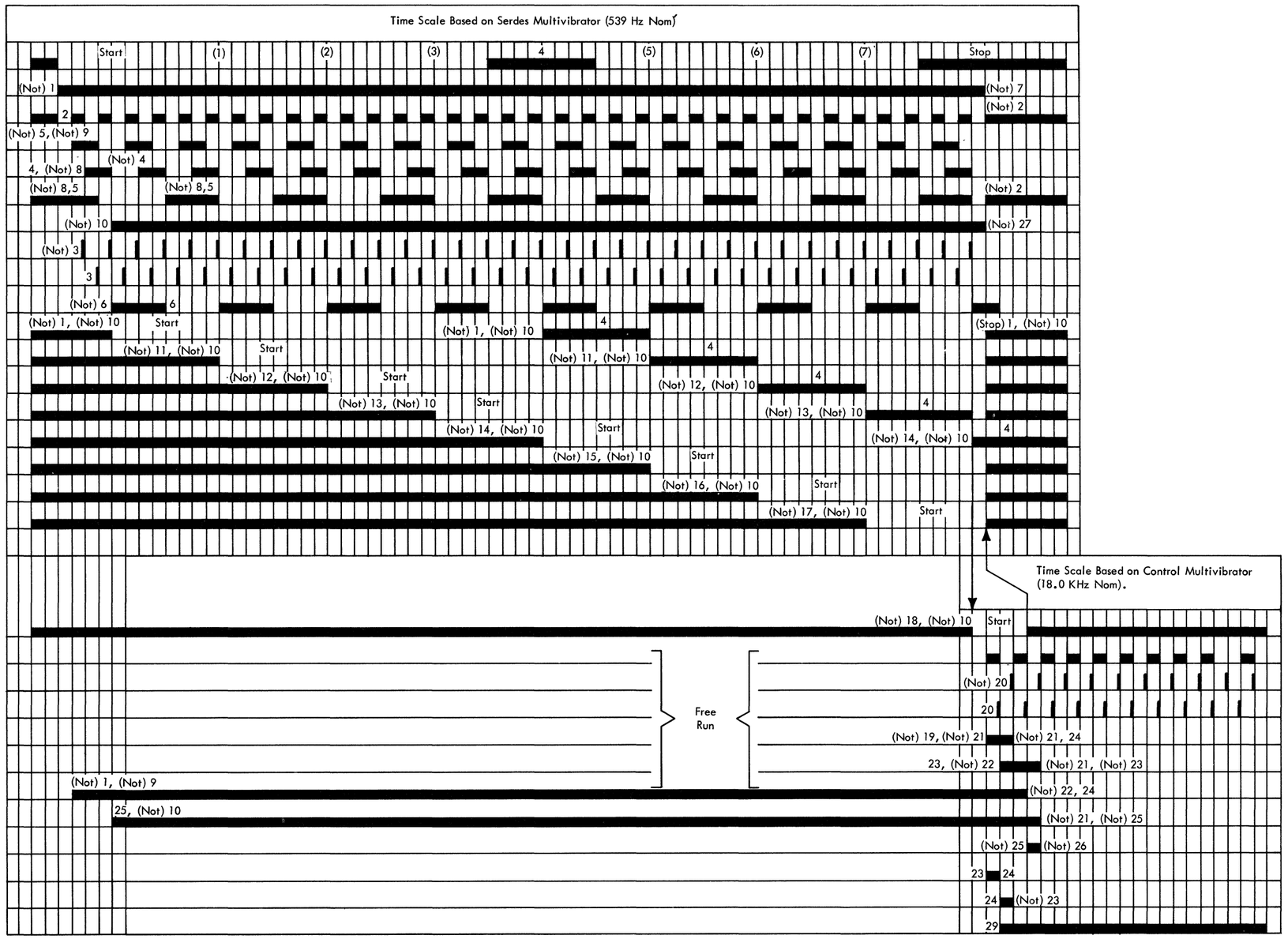
- Terminal in receive text mode.
- Receive character in S registers:
  1. S Reg initially restored by mode change (D4).
  2. Serial Data In drops (B3), starting serdes clock (C4), turning on 'enter serdes gate' (E3).
  3. 'Enter serdes' turns on (E4).
  4. Turn off 'S Reg 8' (B3).
  5. Condition of "line" and SDAC pulses shift character into S register (B4).
- Transfer character to 1B register:
  1. Start control clock (A2).
  2. Reset 1B prior to receiving character (C7).
  3. 1B Set transfers character to 1B if in parity (A7).
  4. 'Enter serdes gate' turns off (E3), restoring S register (D4), then turning off 'enter serdes' (E4).



* Multiple ANDs
RC--Record Checking

Diagram 5-7. Receive Timing Chart (Chart 1 of 2)--Deserialize Numeral 4

No.	Signal Name	SP	Logic
1	Line	G2G07	AA131
2	Clock Run	G2J05	AA131
3	SDMV	G6J07	AA361
4	SD 1	H2D05	AA061
5	SD 2	H2D04	AA061
6	SD 3	H2D02	AA061
7	SD 4		AA061
8	SDCAC 1	G1D05a	AA052
9	SDCAC 2	G1D04b	AA052
10	SDAC	G1D07c	AA052
11	S 8 - Stop Bit	H4D07	AA021
12	S 7 - C Bit	H4D10	AA021
13	S 6 - 1 Bit	H4J11	AA021
14	S 5 - 2 Bit	H4B12	AA021
15	S 4 - 4 Bit	H4G02	AA031
16	S 3 - 8 Bit	H4J13	AA031
17	S 2 - A Bit	H4G09	AA031
18	S 1 - B Bit	H4J06	AA031
19	S 0 - Start Bit	H4G07	AA031
20	CMV	G6J13	AA361
21	CC1	F7D07d	AA051
22	CC2	F7D04e	AA051
23	C1	H2G04	AA071
24	C2	H2G07	AA071
25	Enter Serdes Gt	G2D02	AA131
26	Enter Serdes	E2B09	AA101
27	S Register Restore	E2D04	AA101
28	1B Reset	D6J07	AA231
29	1B Set	J6G08	AA141
30	1B Full	D4B04	AA184



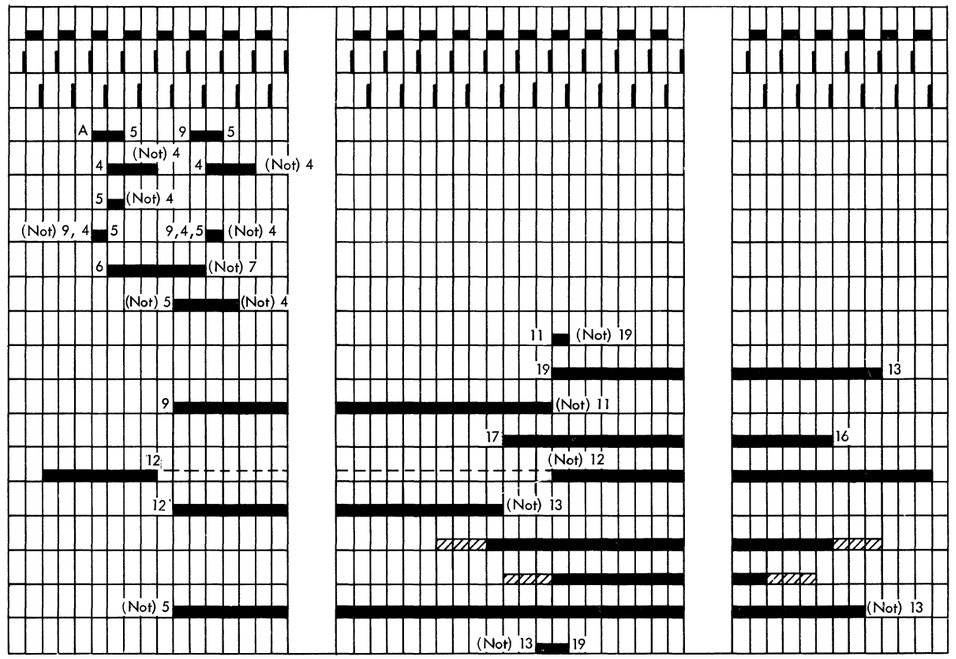
SP for 2741
a. F6D05
b. F6D04
c. F6D07
d. F7B07
e. F7B04

Diagram 5-7. Receive Timing Chart (Chart 2 of 2)--Print and Mode Change

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

	No.	Signal Name	SP	Logic
	1	CMV	G6J13	AA361
	2	CC1	F7D07 a	AA051
A	3	CC2	F7D04 b	AA051
	4	C1	H2G04	AA071
	5	C2	H2G07	AA071
	6	1 B Set	J6G08	AA141
►	7	1 B Reset	D6J07	AA231
	8	1 B Full	D4B04	AA184
	9	2 B Set	F2D04	AA121
	10	2 B Reset	F2G08	AA121
B	11	2 B Reset Gate	F2G07 c	AA121
	12	2 B Full	D2B07	AA091
	13	I/O Cycle	J6G03	AA141
	14	Print	F4B09	AA251
►	15	Print Out	D2D11	AA091
	16	I/O C N-C	J2D09	AA161 *
	17	I/O C N-O	J2D02	AA161 *
	18	Operate	J6J11	AA141
C	19	2 B Reset	F2J09 d	AA121

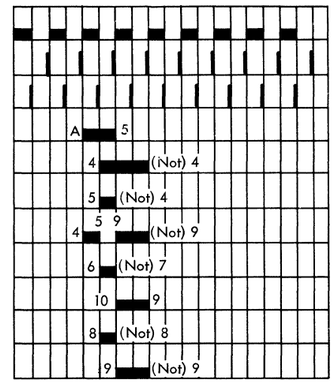
Time Scale Based On Control Multivibrator



A. The Final Gate Condition for C1 is '(Not) S0' TRANSFER A CHARACTER FROM 1B TO 2B AND PRINT

SP for 2741 *Logic for 2741
a. F7B07 AA163
b. F7B04
c. F2B02
d. F2J11
e. F7B07
f. F7B04

	No.	Signal Name	SP	Logic
	1	CMV	G6J13	AA361
	2	CC1	F7D07 e	AA051
	3	CC2	F7D04 f	AA051
	4	C1	H2G04	AA071
	5	C2	H2G07	AA071
	6	1 B Set	J6G08	AA141
	7	1 B Reset	D6J07	AA231
	8	1 B Full	D4B04	AA184
	9	Mode Change	E4J02	AA211
	10	Control Funct.		
	11	S Reg. Restore	E2D04	AA101



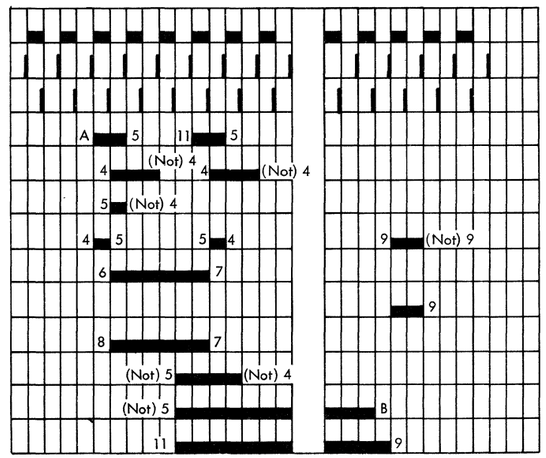
CHANGE MODES ON RECEIPT OF A CONTROL CHARACTER AFTER PRINTING (2740 ONLY)

D

►

E

	No.	Signal Name	SP	Logic
	1	CMV	G6J13	AA361
	2	CC1	F7D07	AA051
	3	CC2	F7D04	AA051
	4	C1	H2G04	AA071
	5	C2	H2G07	AA071
	6	1 B Set	J6G08	AA141
	7	1 B Reset	D6J07	AA231
	8	1 B Full	D4B04	AA184
	9	Mode Change	E4J02	AA211
	10	Control Funct.		
	11	2 B Set	D4D11	AA184
	12	Operate	J6J11	AA141
	13	End of State	F6D11	AA321



CHANGE MODES ON RECEIPT OF A CONTROL CHARACTER WITHOUT PRINTING

B. I/O Cycle going to Zero is the Final Gating Condition Allowing Operate to be Reset by CC2

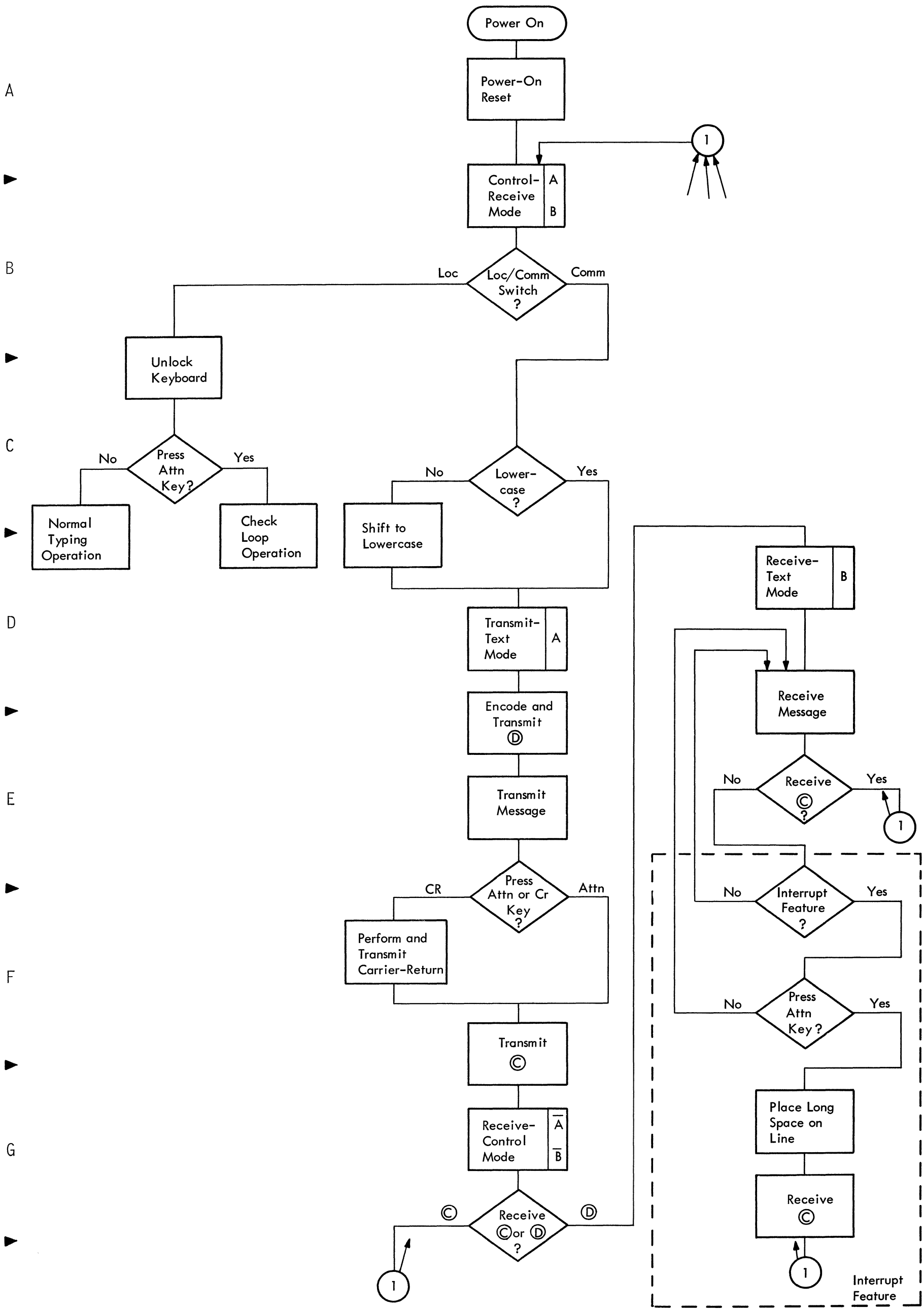
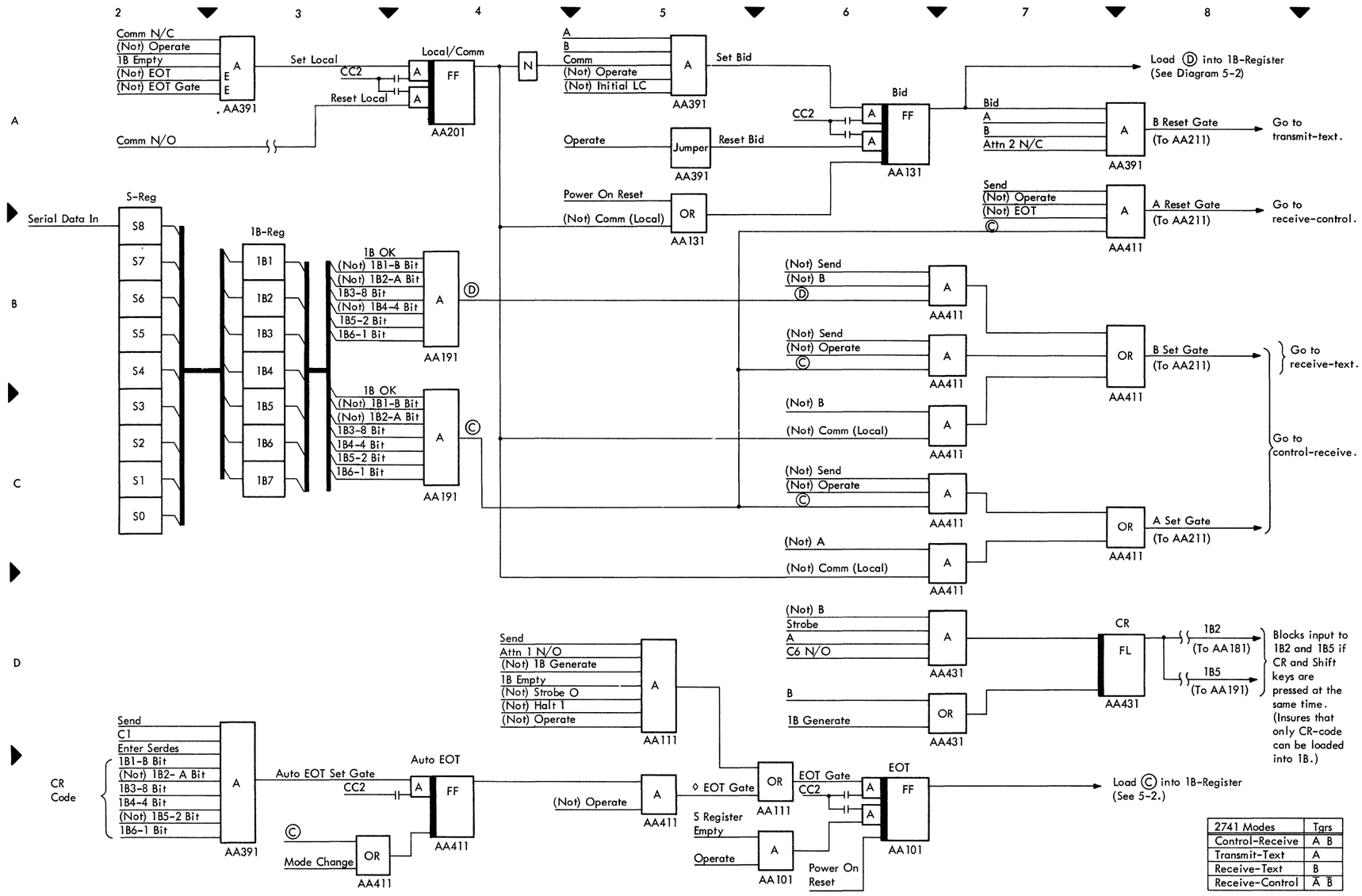


Diagram 5-8. 2741 with Interrupt

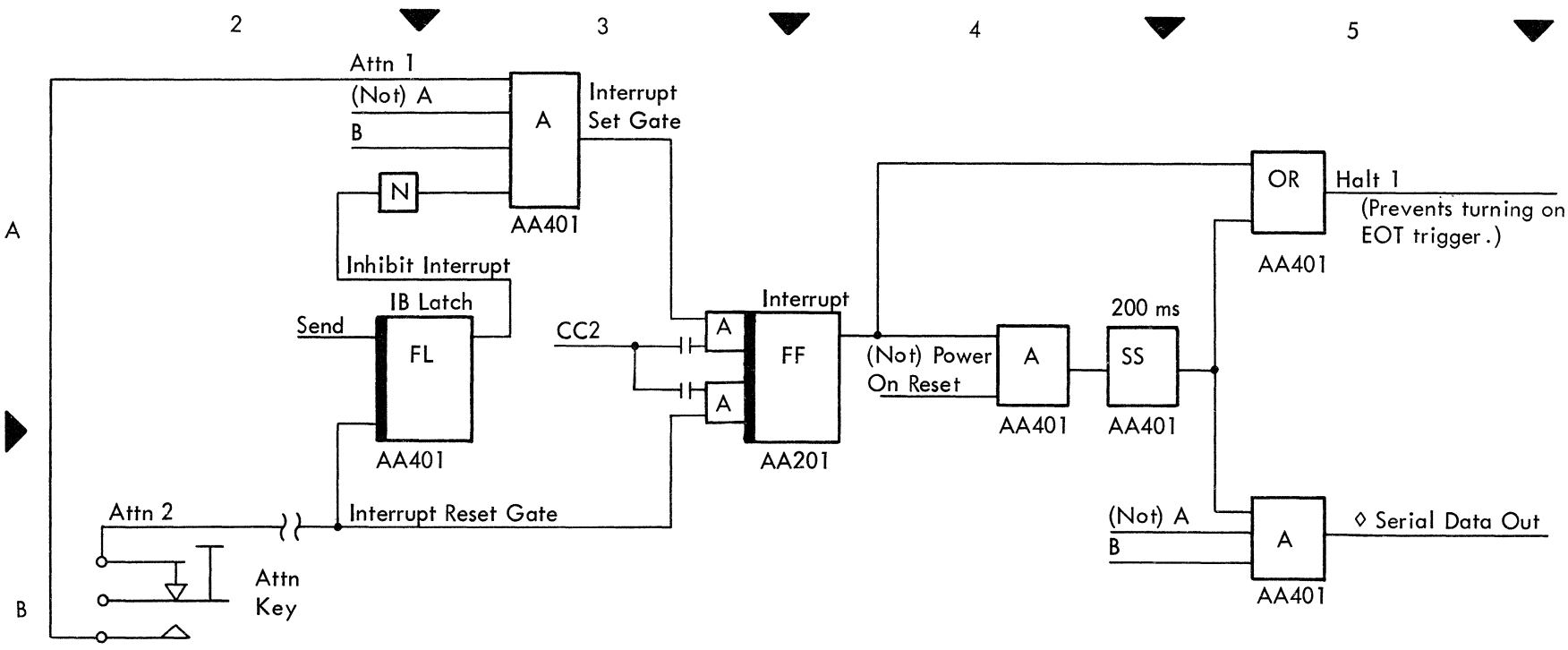


2741 Modes	Tgrs
Control-Receive	A B
Transmit-Text	A
Receive-Text	B
Receive-Control	$\bar{A}$ $\bar{B}$

Objectives

Terminal in Control Receive Mode.

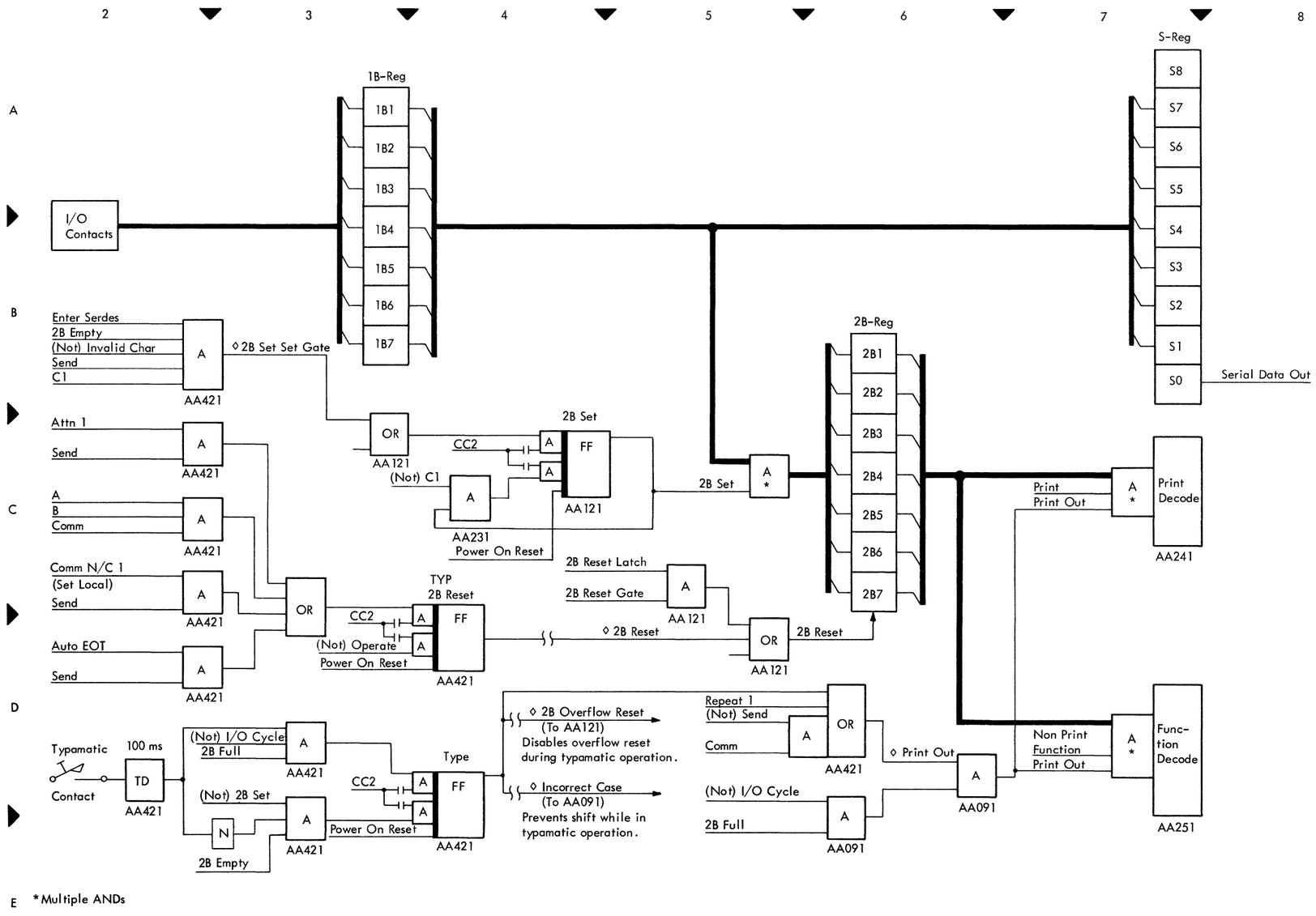
- Transmit Ⓓ :
  1. Turn on 'bid' (A6).
  2. Bring up B Reset Gate (A8).
  3. Go to Transmit Text mode.
  4. Encode and transmit Ⓓ (5-2 A5).
- Transmit Ⓒ (Attention Key):
  1. Press Attention key.
  2. Turn on 'EOT' (E6).
  3. Encode and transmit Ⓒ (5-2 A5).
  4. Bring up A Reset Gate (A8).
  5. Turn off 'EOT' when Ⓒ is transmitted (E6).
  6. Go to receive control mode.
- Transmit Ⓒ (CR Key):
  1. Press CR key.
  2. Turn on 'CR' (D8).
  3. Detect CR and turn on 'Auto EOT' (E4).
  4. Transmit CR.
  5. Turn on 'EOT' (E6).
  6. Steps 3 through 6 above.
  7. Turn off 'CR' (D8).
- Receive Ⓓ in Receive Control Mode:
  1. Recognize Ⓓ (B4).
  2. Bring up B Set Gate (B8).
  3. Go to receive text mode.
- Receive Ⓒ in Receive Control Mode:
  1. Recognize Ⓒ (C4).
  2. Bring up A Set Gate and B Set Gate (B8, C8).
  3. Go to control receive mode.
  4. From control receive terminal will automatically go to transmit text and send Ⓓ (See first objective).



Objectives

- Interrupt Incoming Message:
  1. Press Attention key
  2. Turn on 'Interrupt'--1B Latch is off
  3. Start 200 MS Singleshot
  4. Hold up Serial Data Out for 200 MS space
  5. Turn off 'interrupt' and '1B Latch' when key is released
  6. '1B' latch prevents sending a space instead of a ⓒ during transmit operations
  7. Halt 1 prevents sending a ⓒ instead of a space during receive operations

Diagram 5-10. Interrupt (2741)



Objectives

- Send Repetitive Characters:
  1. Press and hold one of the typamatic keys (D2).
  2. Load character to both 1B and 2B.'
  3. After 100 MS turn on 'type' (D4).
  4. Allow Print Out to come up when print cycle completes (D6).
  5. Begin new print cycle.
  6. Reset 2B in normal manner (C5).
  7. Turn off 'type' (D4).
  8. Repeat steps 3 through 6 until key is released.
- Force 2B Reset:
  1. 'TYP 2B reset' (D4) forces a 2B reset:
     a. when Attn is pressed.
     b. when going to control receive.
     c. when terminal is switched to Local.
     d. when CR is pressed.

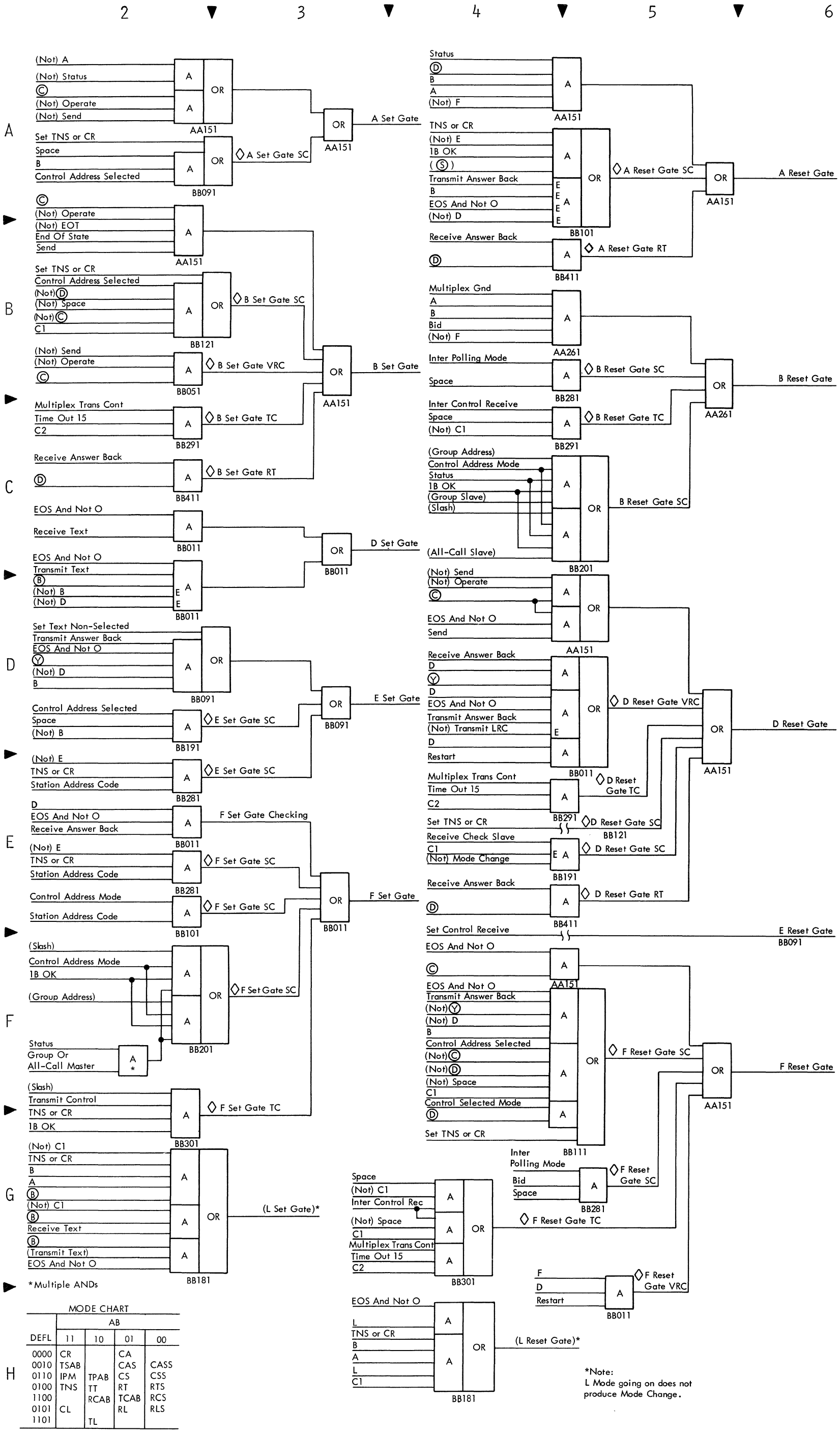


Diagram 5-12. Mode Control, All Features (2740-1)

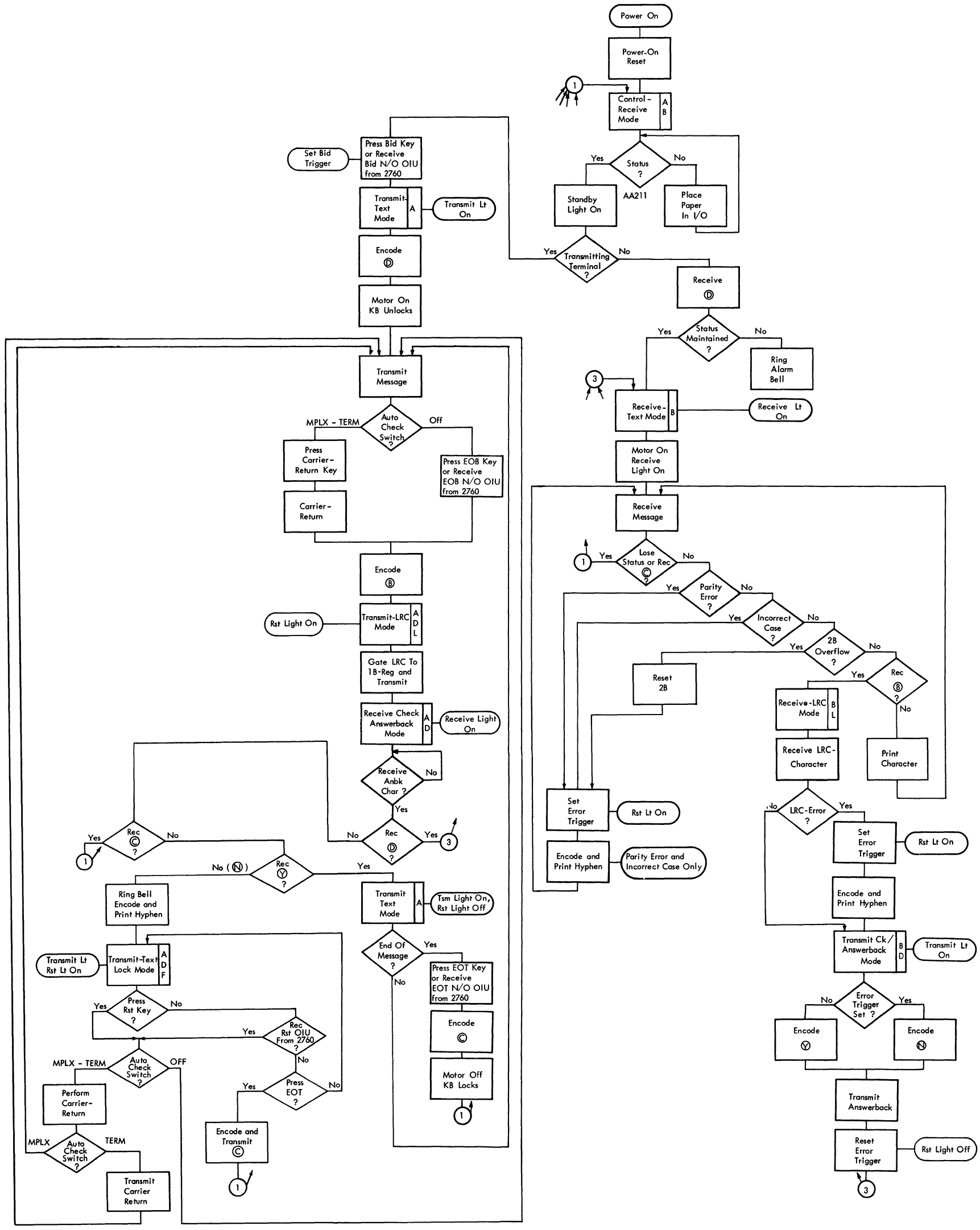
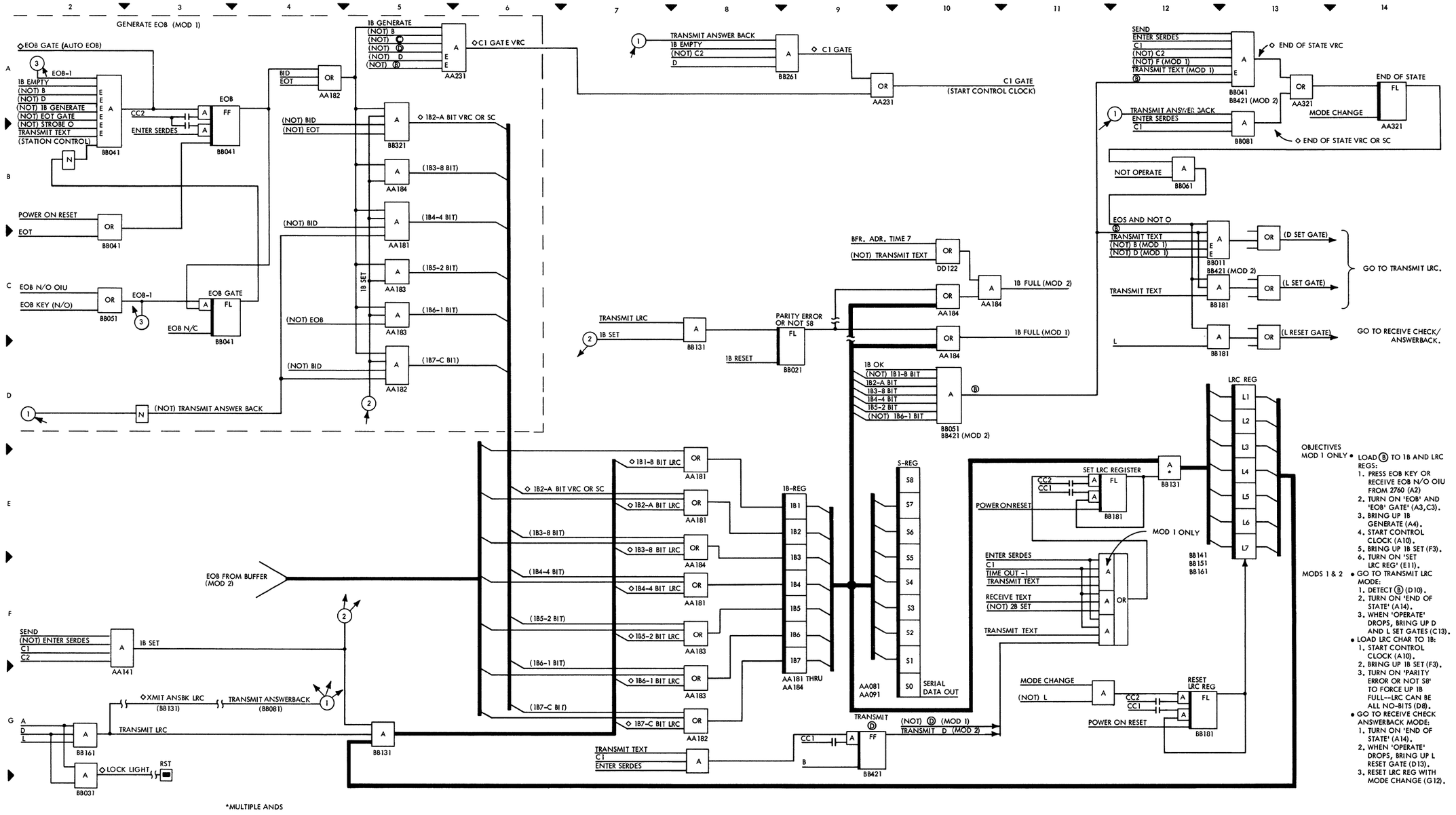
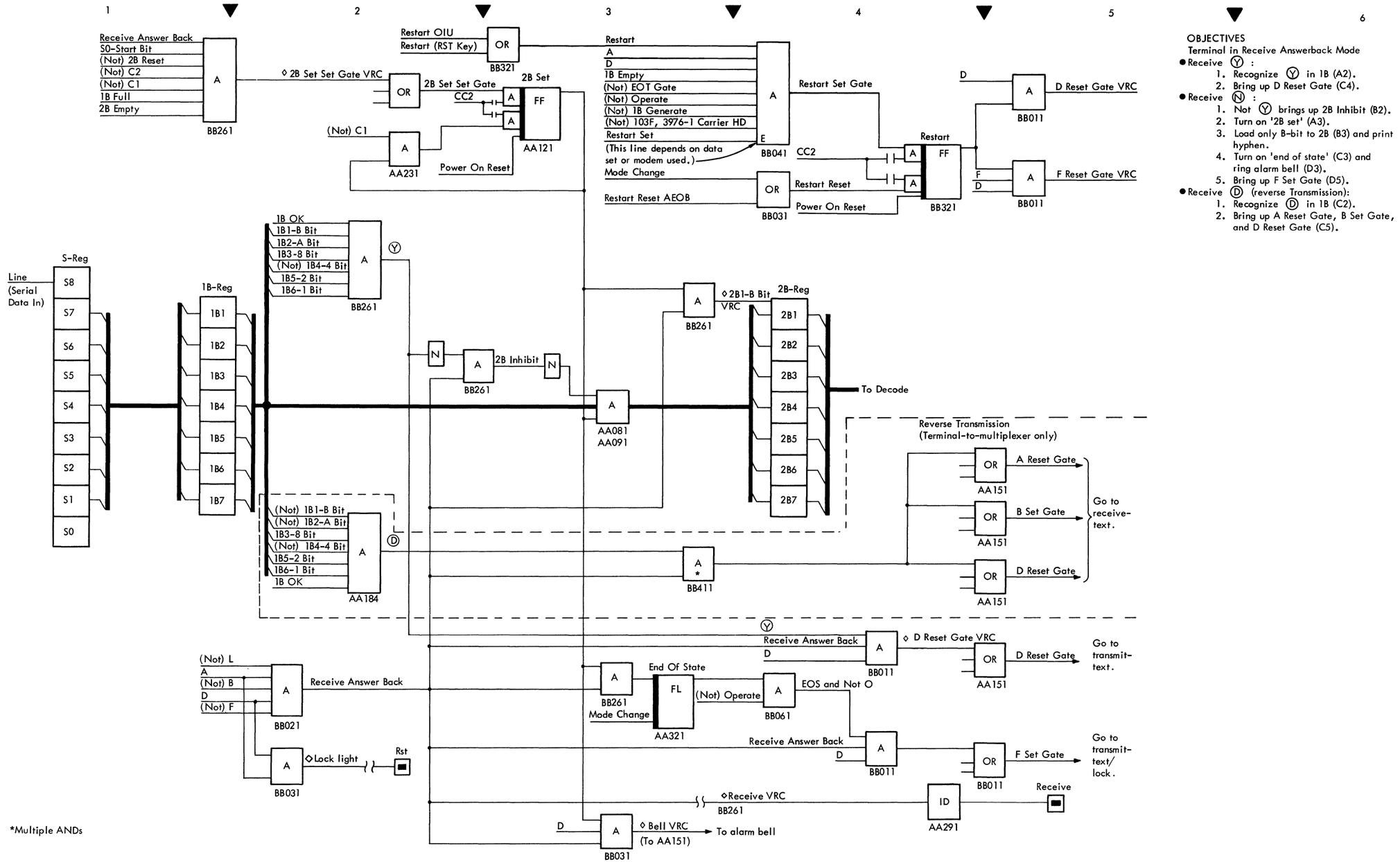


Diagram 5-13. Record Checking and Auto EOB Flow (2740-1)

Diagram 5-14. Transmit EOB and LRC Characters (2740-1/2740-2)

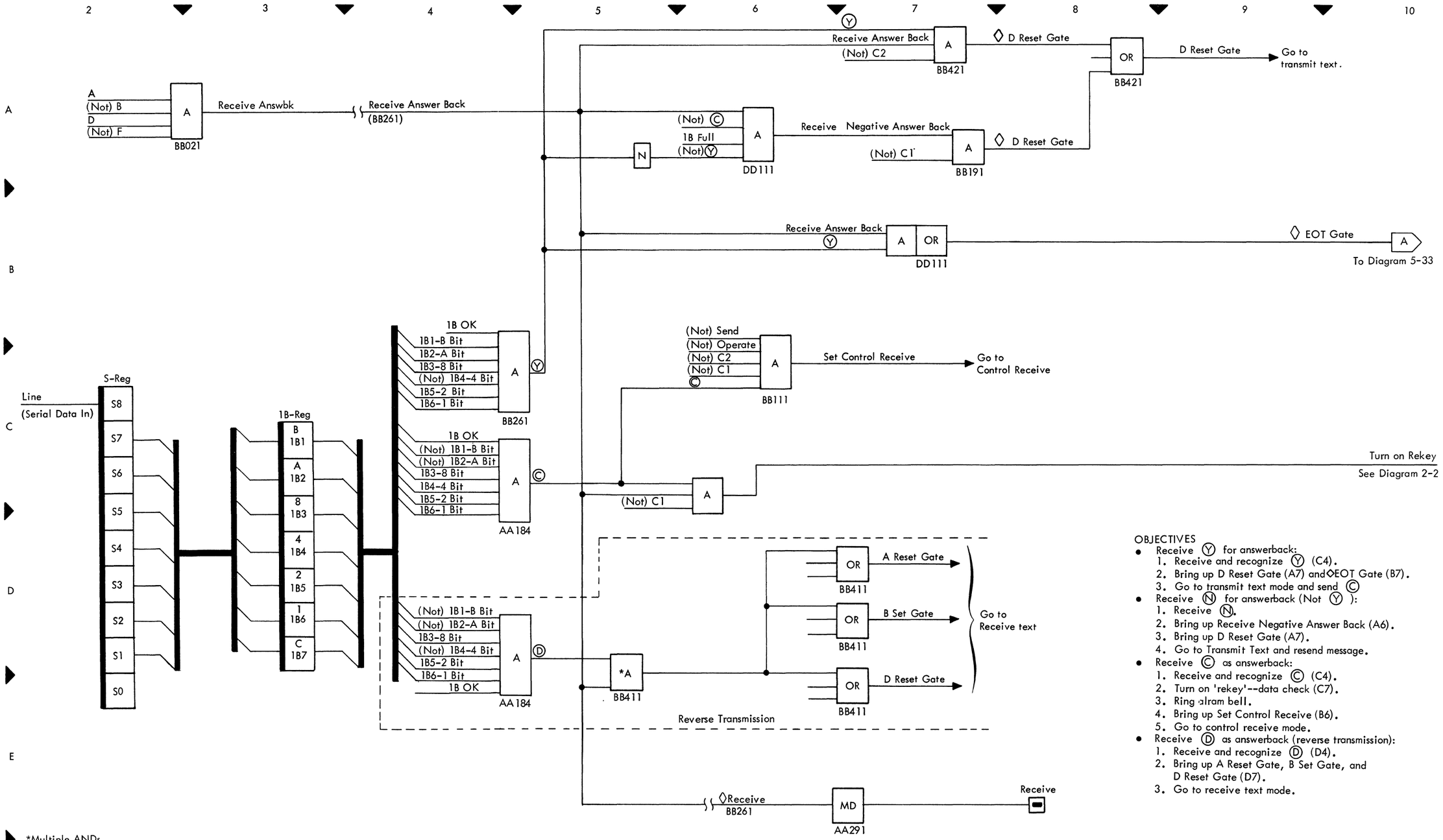


*MULTIPLE ANDS



*Multiple ANDs

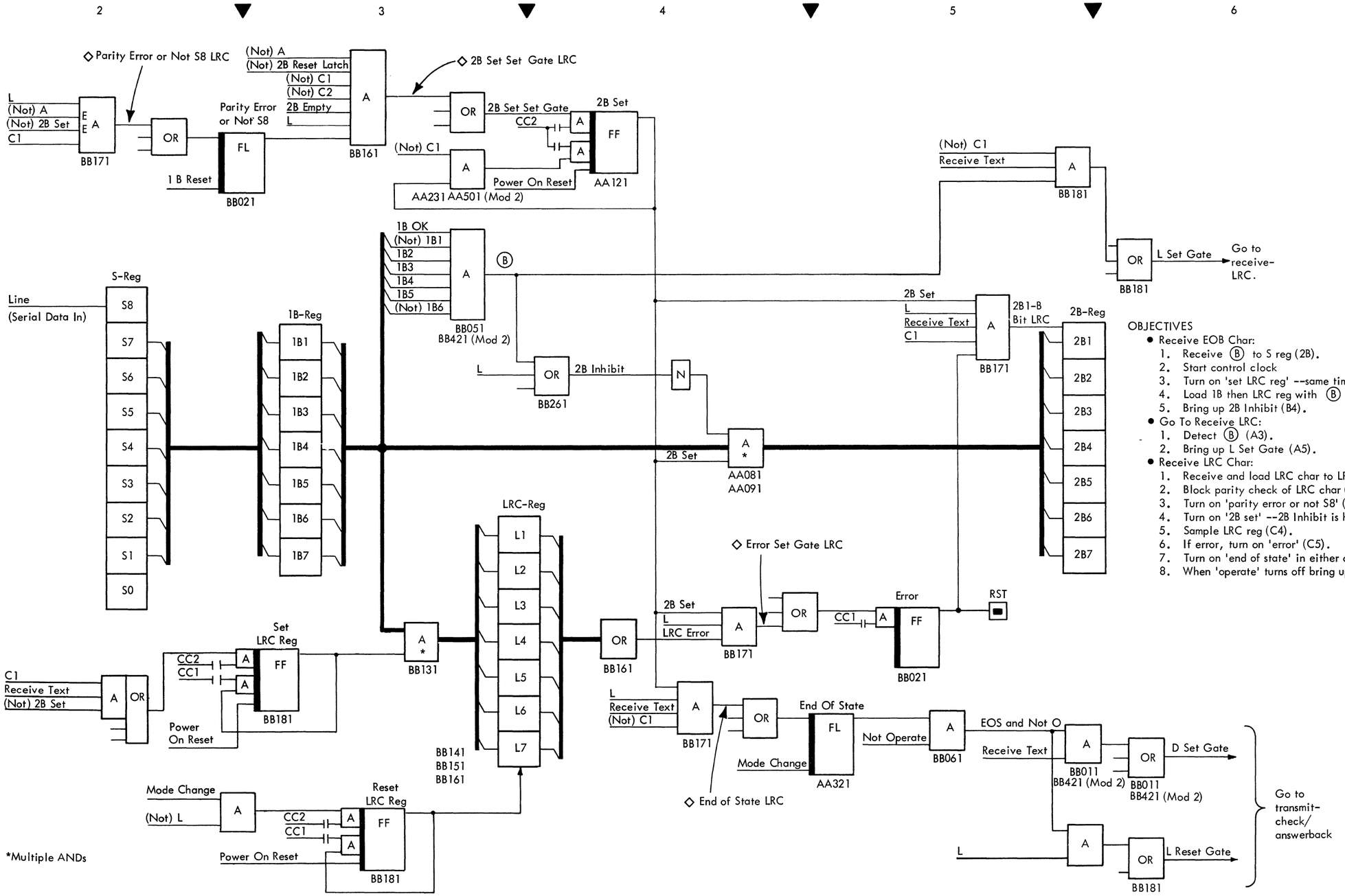
Diagram 5-16. Receive Check Answerback (2740-2)



*Multiple ANDs

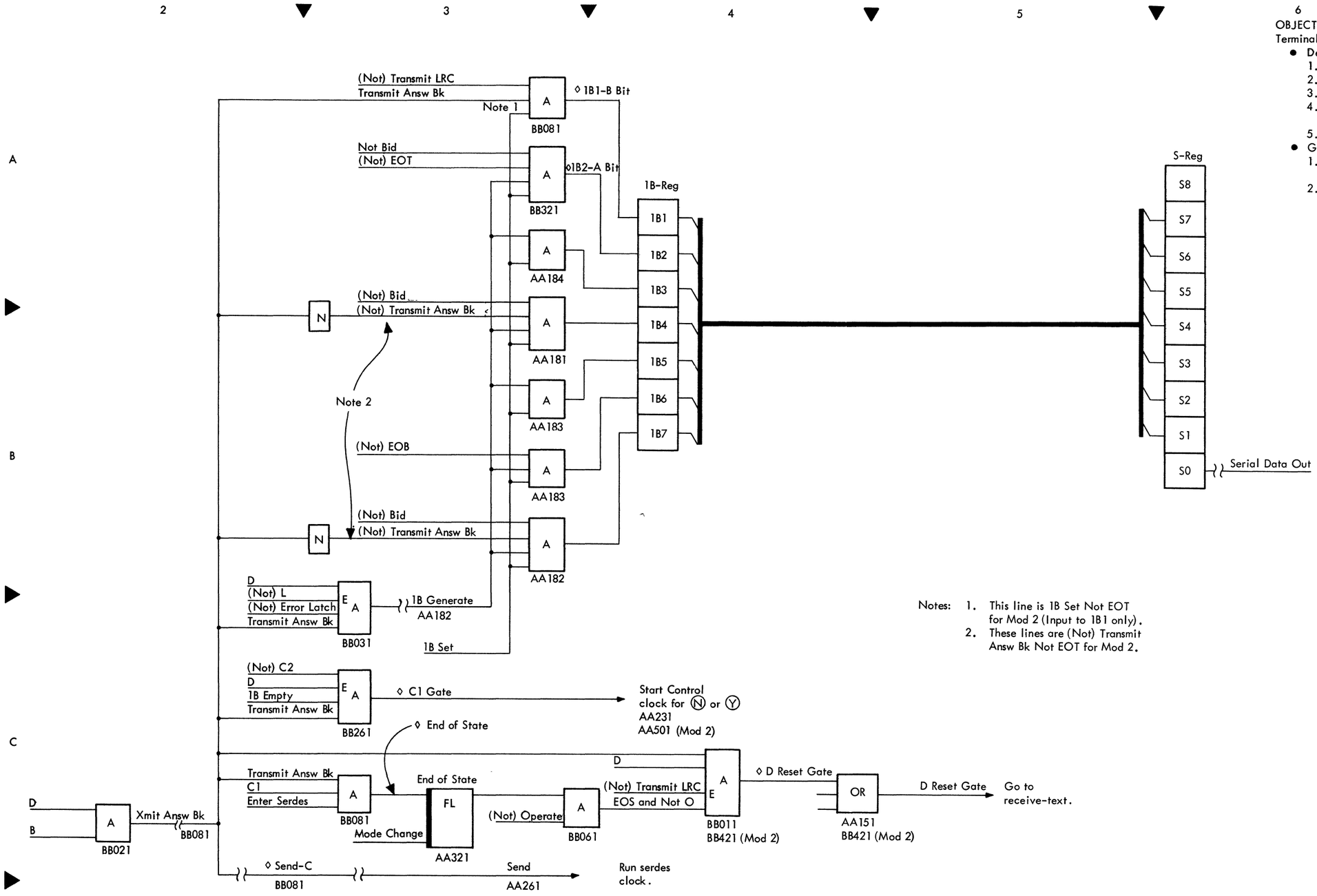
OBJECTIVES

- Receive Ⓨ for answerback:
  1. Receive and recognize Ⓨ (C4).
  2. Bring up D Reset Gate (A7) and ◊EOT Gate (B7).
  3. Go to transmit text mode and send Ⓒ
- Receive Ⓝ for answerback (Not Ⓨ):
  1. Receive Ⓝ.
  2. Bring up Receive Negative Answer Back (A6).
  3. Bring up D Reset Gate (A7).
  4. Go to Transmit Text and resend message.
- Receive Ⓒ as answerback:
  1. Receive and recognize Ⓒ (C4).
  2. Turn on 'rekey'--data check (C7).
  3. Ring alram bell.
  4. Bring up Set Control Receive (B6).
  5. Go to control receive mode.
- Receive Ⓓ as answerback (reverse transmission):
  1. Receive and recognize Ⓓ (D4).
  2. Bring up A Reset Gate, B Set Gate, and D Reset Gate (D7).
  3. Go to receive text mode.



OBJECTIVES

- Receive EOB Char:
  1. Receive (B) to S reg (2B).
  2. Start control clock
  3. Turn on 'set LRC reg' --same time as 1B Set (C2).
  4. Load 1B then LRC reg with (B) (B2, C2).
  5. Bring up 2B Inhibit (B4).
- Go To Receive LRC:
  1. Detect (B) (A3).
  2. Bring up L Set Gate (A5).
- Receive LRC Char:
  1. Receive and load LRC char to LRC reg --same as (B)
  2. Block parity check of LRC char (See Diagram 2-1).
  3. Turn on 'parity error or not S8' (A2).
  4. Turn on '2B set' --2B Inhibit is held up by 'L' (A4).
  5. Sample LRC reg (C4).
  6. If error, turn on 'error' (C5).
  7. Turn on 'end of state' in either case (C5).
  8. When 'operate' turns off bring up D Set Gate and L Reset Gate (C5).

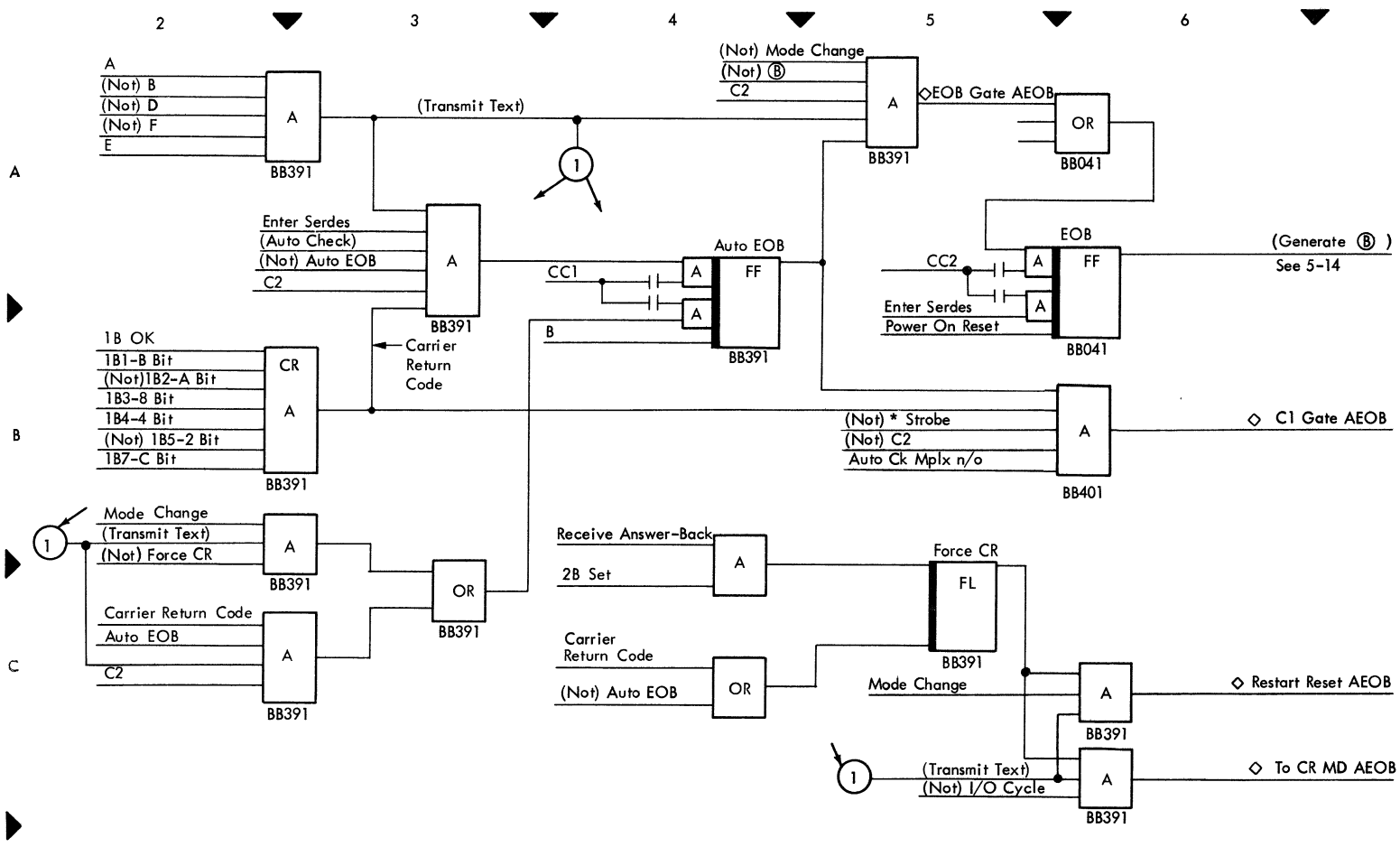


OBJECTIVES

Terminal in Transmit Check Answerback Mode.

- Determine if Ⓨ or Ⓝ is to be transmitted:
  1. If 'error' off, bring up 1B Generate (C2).
  2. Start control clock (C2).
  3. Bring up 1B Set (C2).
  4. Load B-bit to 1B for Ⓝ (A2); B-, A-, 8-, 2-, 1-bits for Ⓨ (A2,B2).
  5. Turn on 'end of state' (C2).
- Go to Receive Text:
  1. When answerback is transmitted, drop Operate (C2).
  2. Bring up D Reset Gate (C4).

Notes:
1. This line is 1B Set Not EOT for Mod 2 (Input to 1B1 only).
2. These lines are (Not) Transmit Answ Bk Not EOT for Mod 2.



Objective:

- Perform EOB Check When CR Key is Pressed:
  1. Press Carrier Return Key, decode CR code.
  2. Turn on Auto EOB, return carrier.
  3. Turn on EOB Trigger, Transmit Ⓑ .
  4. Gate LRC character to 1B-Reg and Transmit.
  5. Go to Receive Check Answerback Mode.
  6. a. Receive Ⓨ , return to transmit text.
     b. Receive Ⓝ (Not Ⓨ)
        1. Turn on 'force CR'.
        2. Perform CR
        3. Switch in TERM--transmit CR Char.
        4. Switch in MPLX--bring up C1 Gate. Reset CR from 1B.

Diagram 5-19. Automatic EOB (2740-1)

Addressing Sequence:

© Ⓢ Address Char Space Ⓝ or Ⓨ Ⓓ Receive-Text ©

Polling Sequence:

© Address Char Space Ⓝ or Ⓓ Transmit-Text ©

Note: For Model 2 See Diagram 5-27. Mode Control (2740-2).

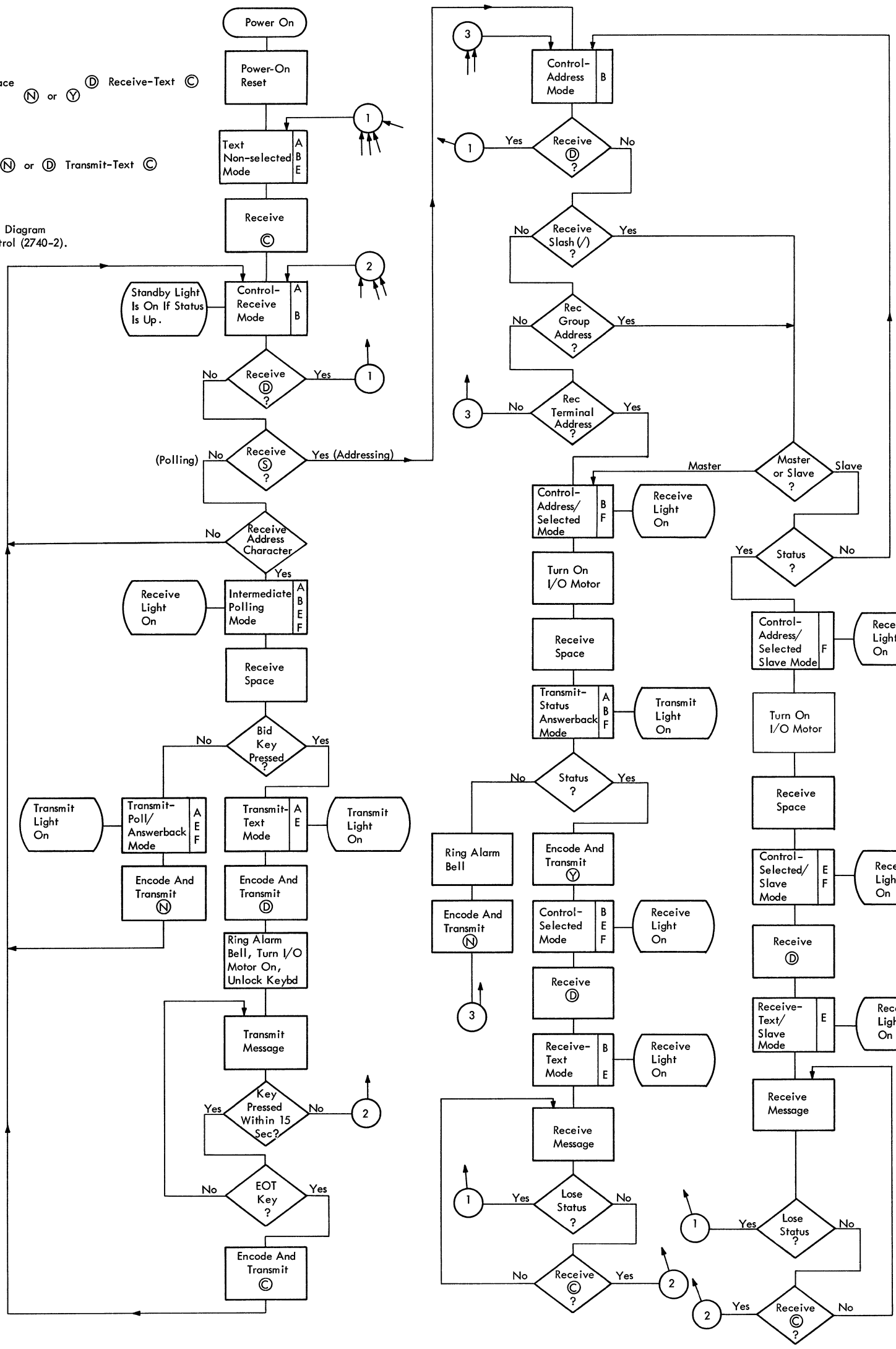


Diagram 5-20. Station Control (2740-1)

OBJECTIVES
- Receive Ⓒ:
  1. Receive and recognize Ⓒ (A4).
  2. Bring up Set Control Receive (B5).
- Receive Ⓢ:
  1. Receive and recognize Ⓢ (C4).
  2. Bring up A Reset Gate--control address mode (D6).
- Receive Terminal Address:
  1. Recognize address character--station (G4)--Group (F4)--All Call (C4).
  2. Bring up F Set Gate--control-address/selected mode (G6,F6,D6).
- If all -call or group address determine if master or slave:
  1. Bring up B Reset Gate if jumpered for slave (E6).
- Receive Space:
  1. Receive and recognize Space (H4).
  2. Bring up A Set Gate if master--Transmit status answerback (H6).
  3. Bring up E Set Gate if slave--control selected slave mode (G6).
- Receive Ⓓ after positive answerback:
  1. Receive and recognize Ⓓ (I4).
  2. Bring up F Reset Gate--receive text mode (I6).

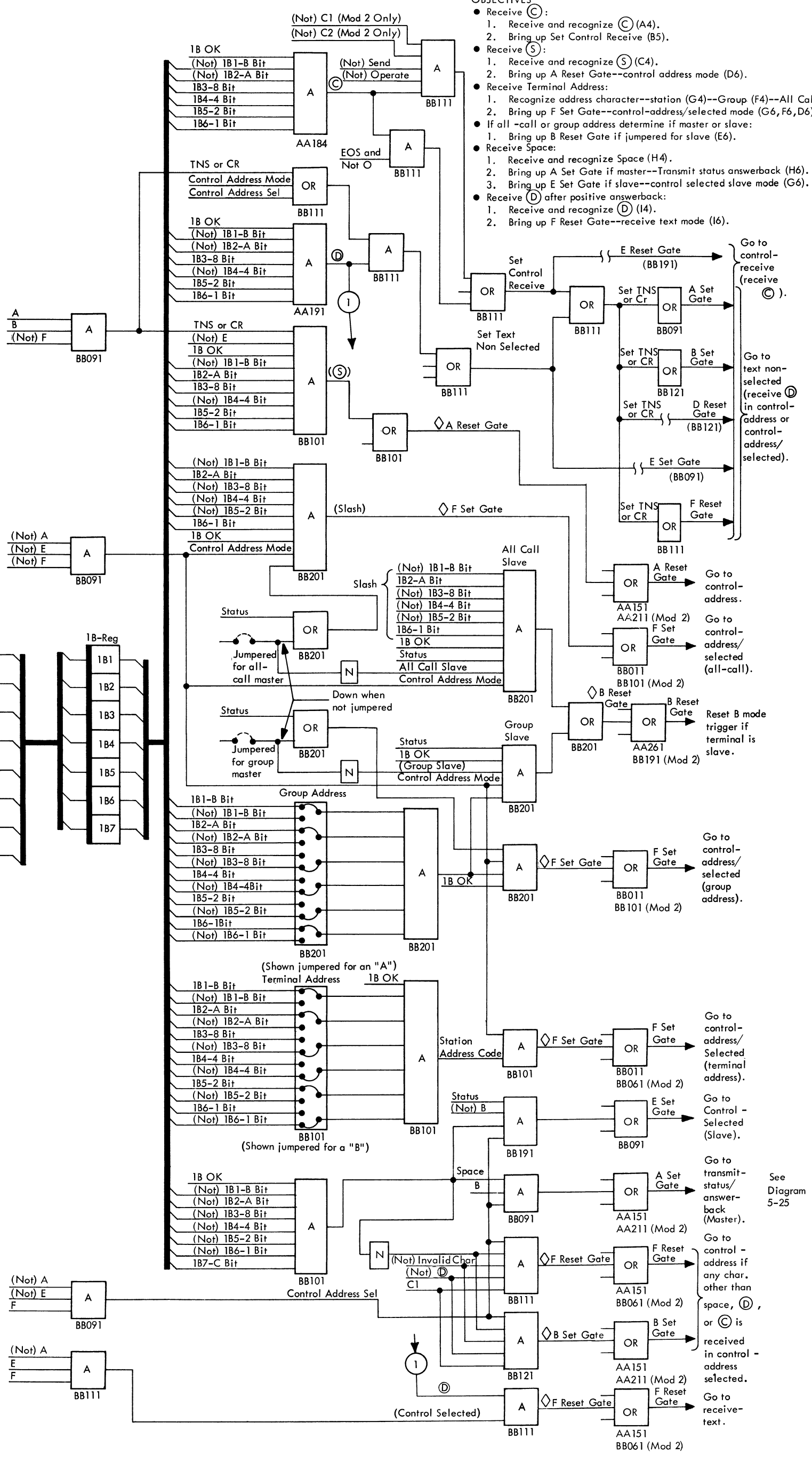
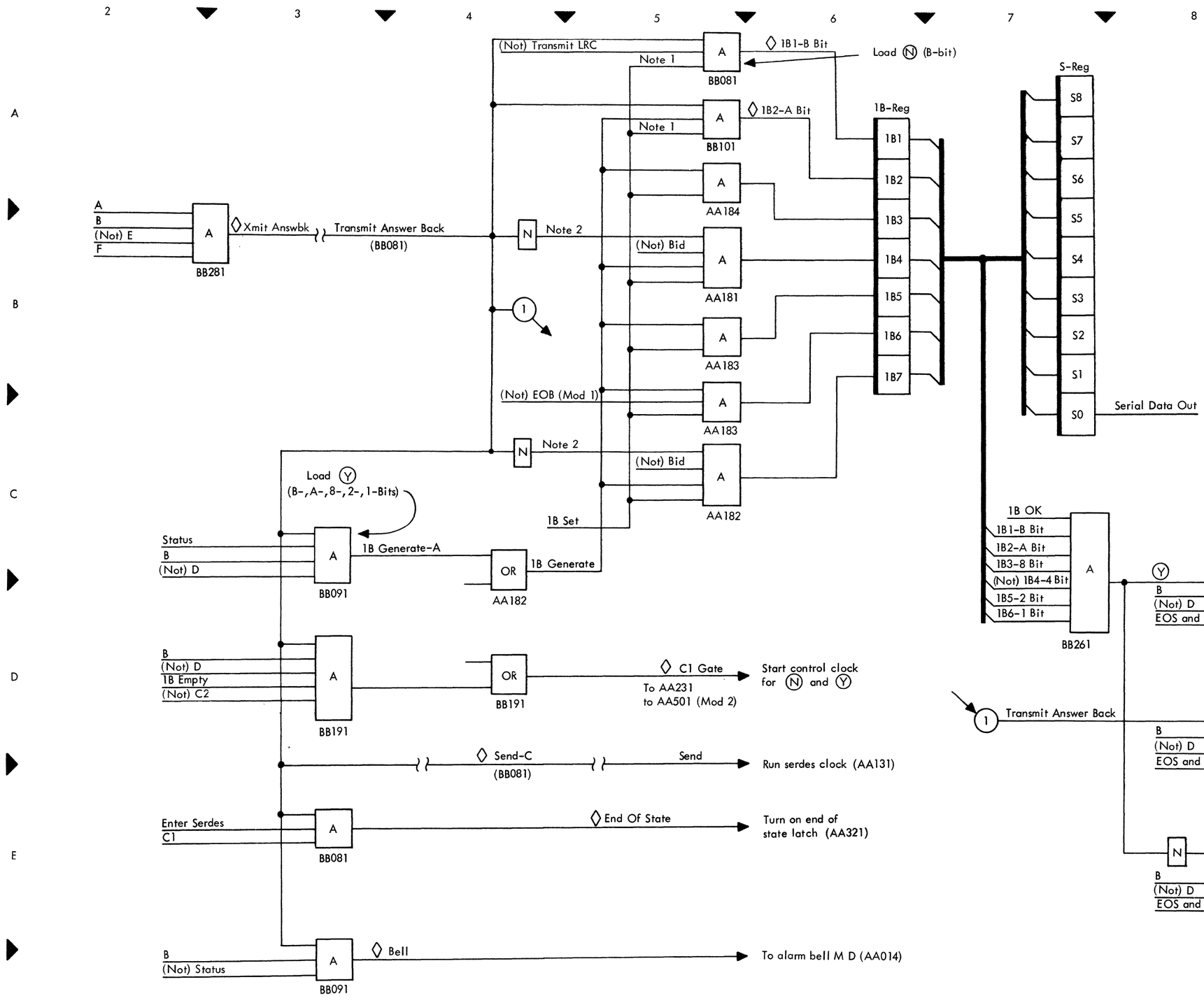


Diagram 5-21. Receive Addressing Character Sequence, Master or Slave (2740-1/2740-2)

Diagram 5-22. Addressing, Transmit Status Answerback,(2740-1) Part 1 of 3



OBJECTIVES

- Terminal in transmit status answerback mode.
- Generate and transmit (Y) if terminal has status:
  1. Bring up 1B Generate (C4).
  2. Start control clock (D5).
  3. Bring up 1B Set (C5).
  4. Load (Y) (B,A,8,2,1) to 1B register (A5,B5,C5).
  5. Transmit normally (serdes clock runs continuously when Send comes up).
- Go to control selected mode if terminal has status:
  1. Turn on 'end of state'(E5).
  2. Detect (Y) in 1B (C7).
  3. Bring up E Set Gate and A Reset Gate (D9).
- Generate and transmit (N) if terminal does not have status:
  1. Start control clock' (D5).
  2. Bring up 1B Set (C5).
  3. Load (N) (B-bit) to 1B (A5).
  4. Transmit normally.
- Go to control address if terminal does not have status:
  1. Turn on 'end of state' (E5).
  2. Detect not (Y) in 1B (C7).
  3. Bring up A Reset Gate and F Reset Gate (D9,E9).

Notes:

1. These lines are 1B Set Not EOT for Mod 2.
2. These lines are (Not) Transmit Answbk Not EOT for Mod 2.

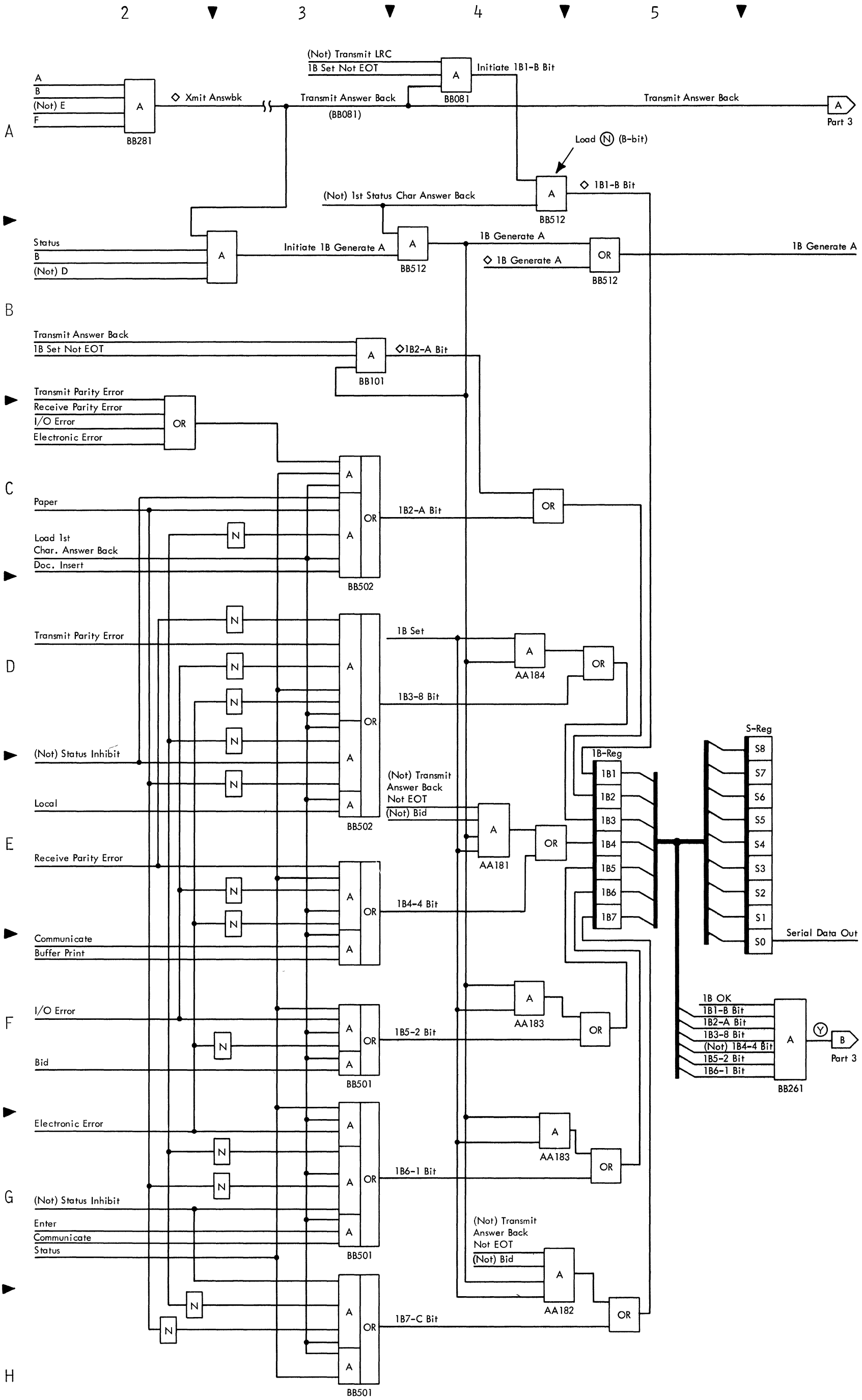


Diagram 5-22. Addressing, Transmit Status Answerback,(2740-2) Part 2 of 3

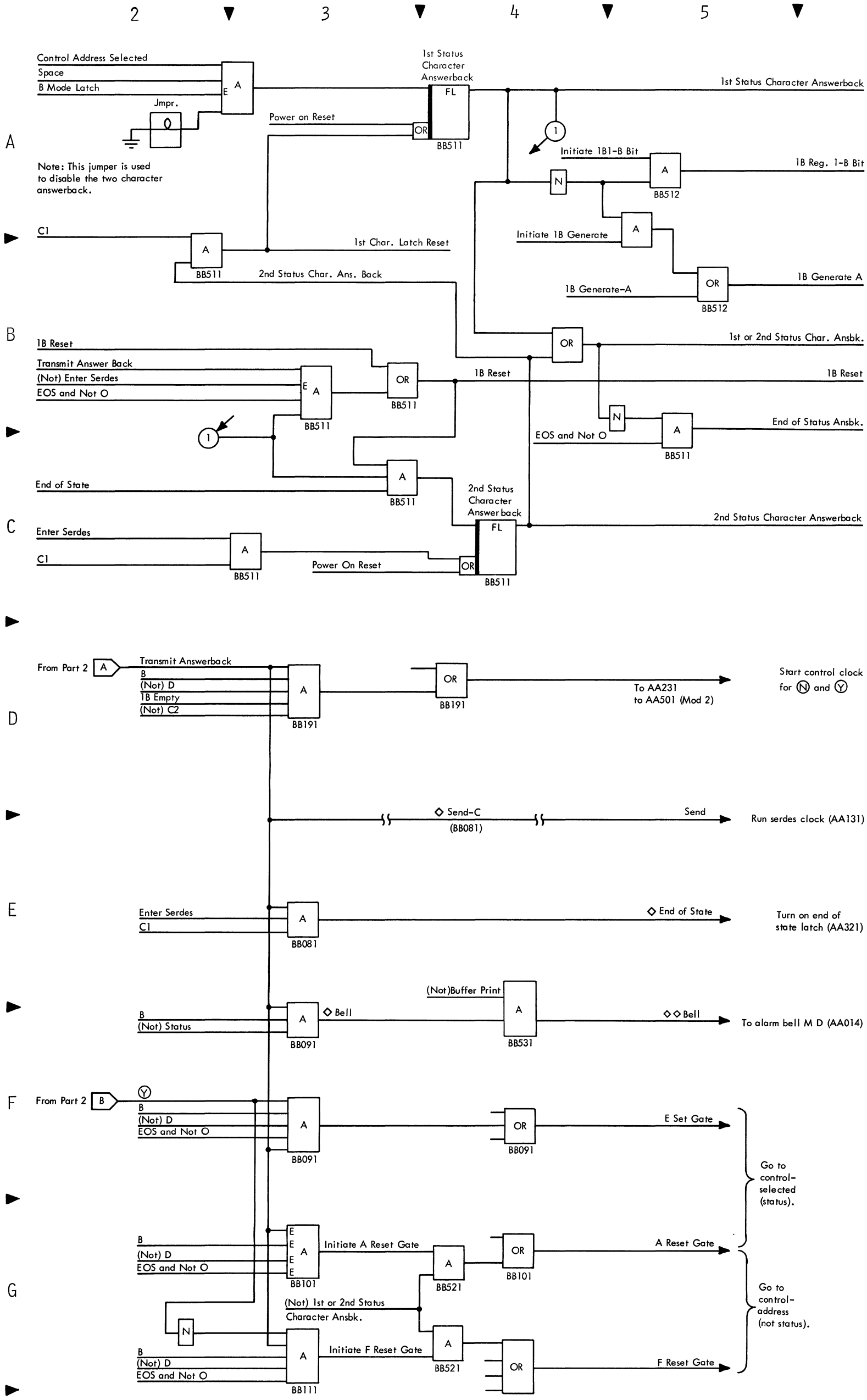
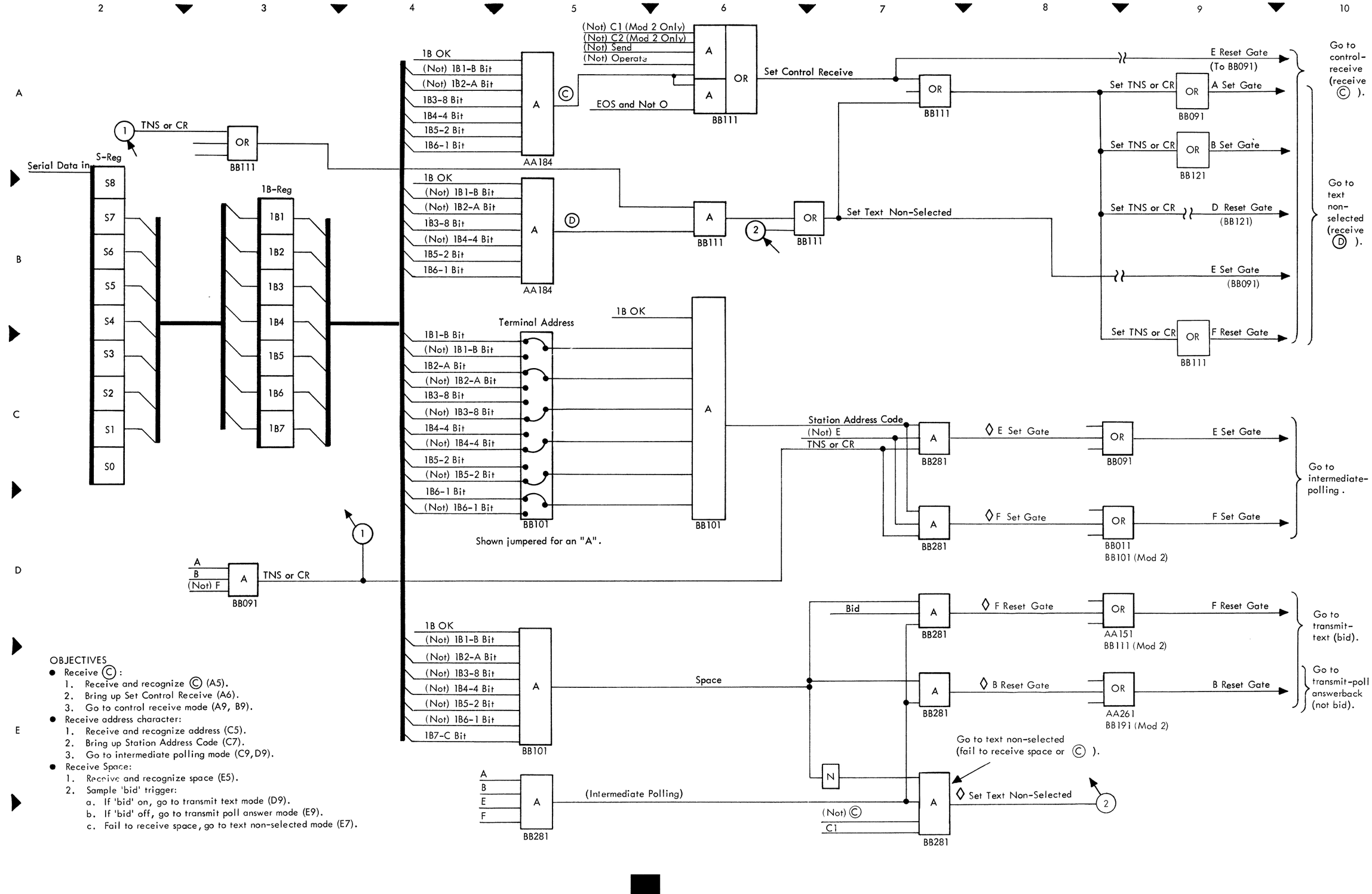


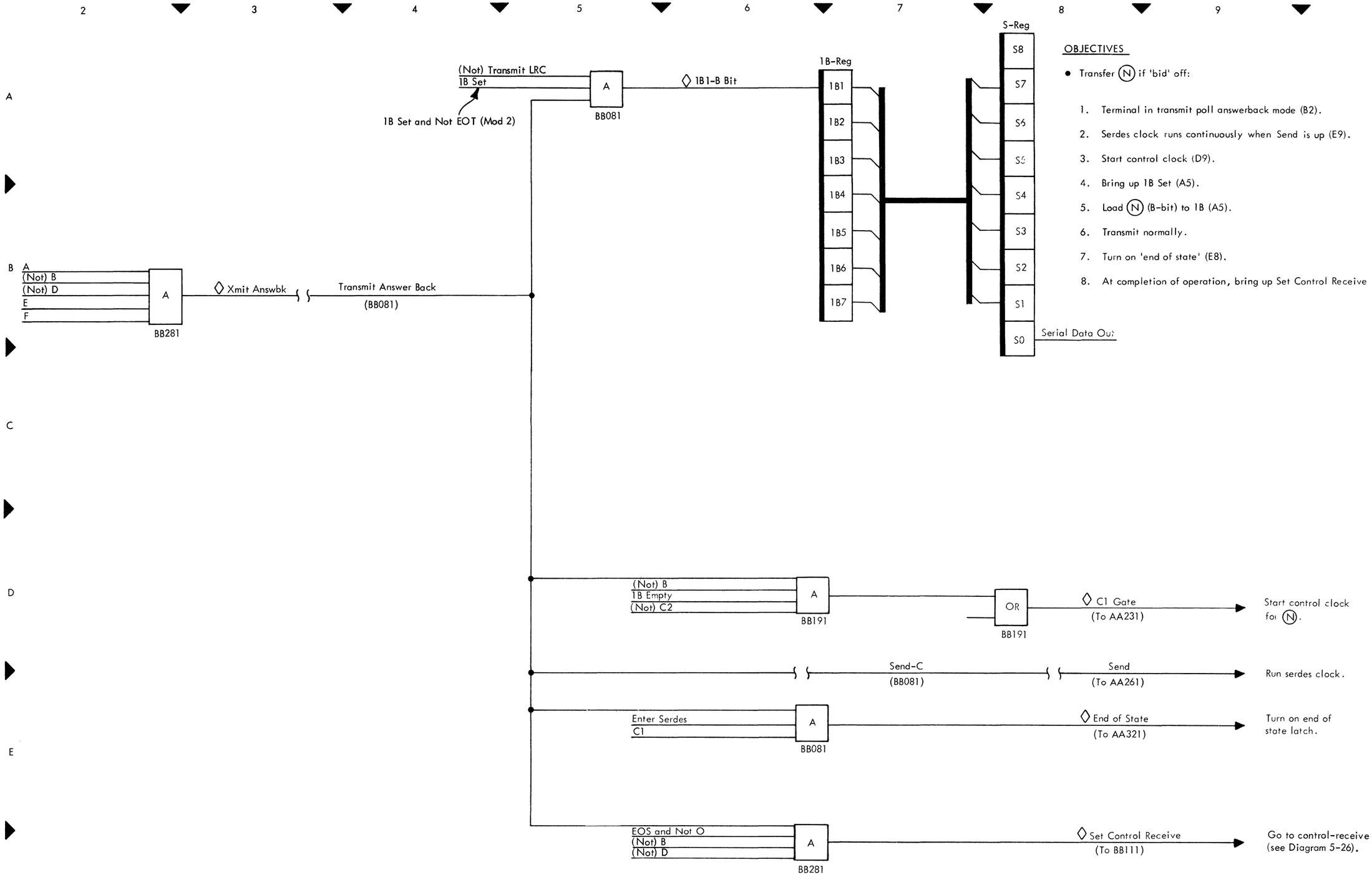
Diagram 5-22. Addressing, Transmit Status Answerback,(2740-2) Part 3 of 3



OBJECTIVES

- Receive Ⓒ:
  1. Receive and recognize Ⓒ (A5).
  2. Bring up Set Control Receive (A6).
  3. Go to control receive mode (A9, B9).
- Receive address character:
  1. Receive and recognize address (C5).
  2. Bring up Station Address Code (C7).
  3. Go to intermediate polling mode (C9, D9).
- Receive Space:
  1. Receive and recognize space (E5).
  2. Sample 'bid' trigger:
     a. If 'bid' on, go to transmit text mode (D9).
     b. If 'bid' off, go to transmit poll answer mode (E9).
     c. Fail to receive space, go to text non-selected mode (E7).

Diagram 5-24. Transmit Poll Answerback (2740-1/2740-2)



OBJECTIVES

- Transfer (N) if 'bid' off:

1. Terminal in transmit poll answerback mode (B2).
2. Serdes clock runs continuously when Send is up (E9).
3. Start control clock (D9).
4. Bring up 1B Set (A5).
5. Load (N) (B-bit) to 1B (A5).
6. Transmit normally.
7. Turn on 'end of state' (E8).
8. At completion of operation, bring up Set Control Receive (F8).

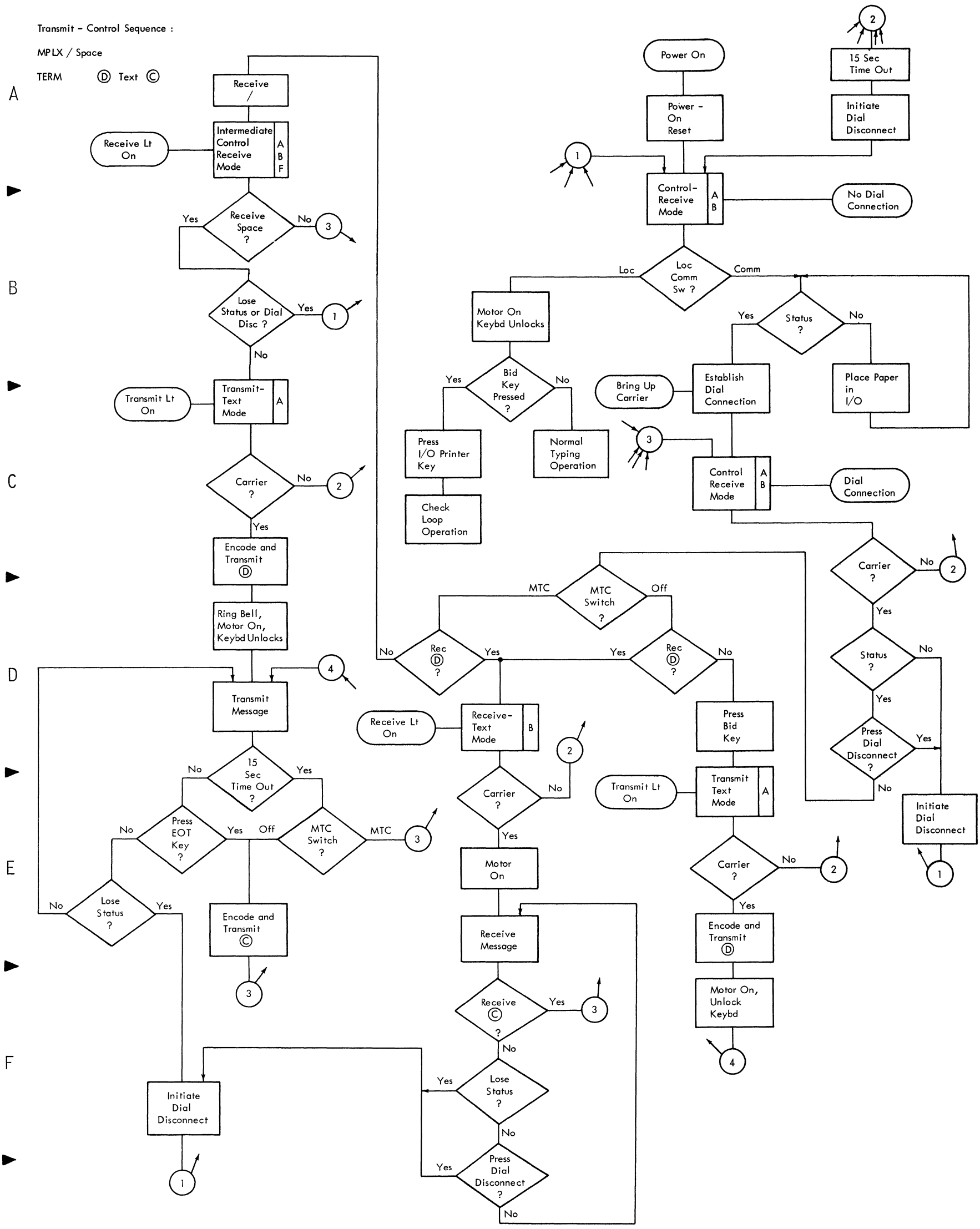


Diagram 5-25. Transmit Control with Dial Up (2740-1)

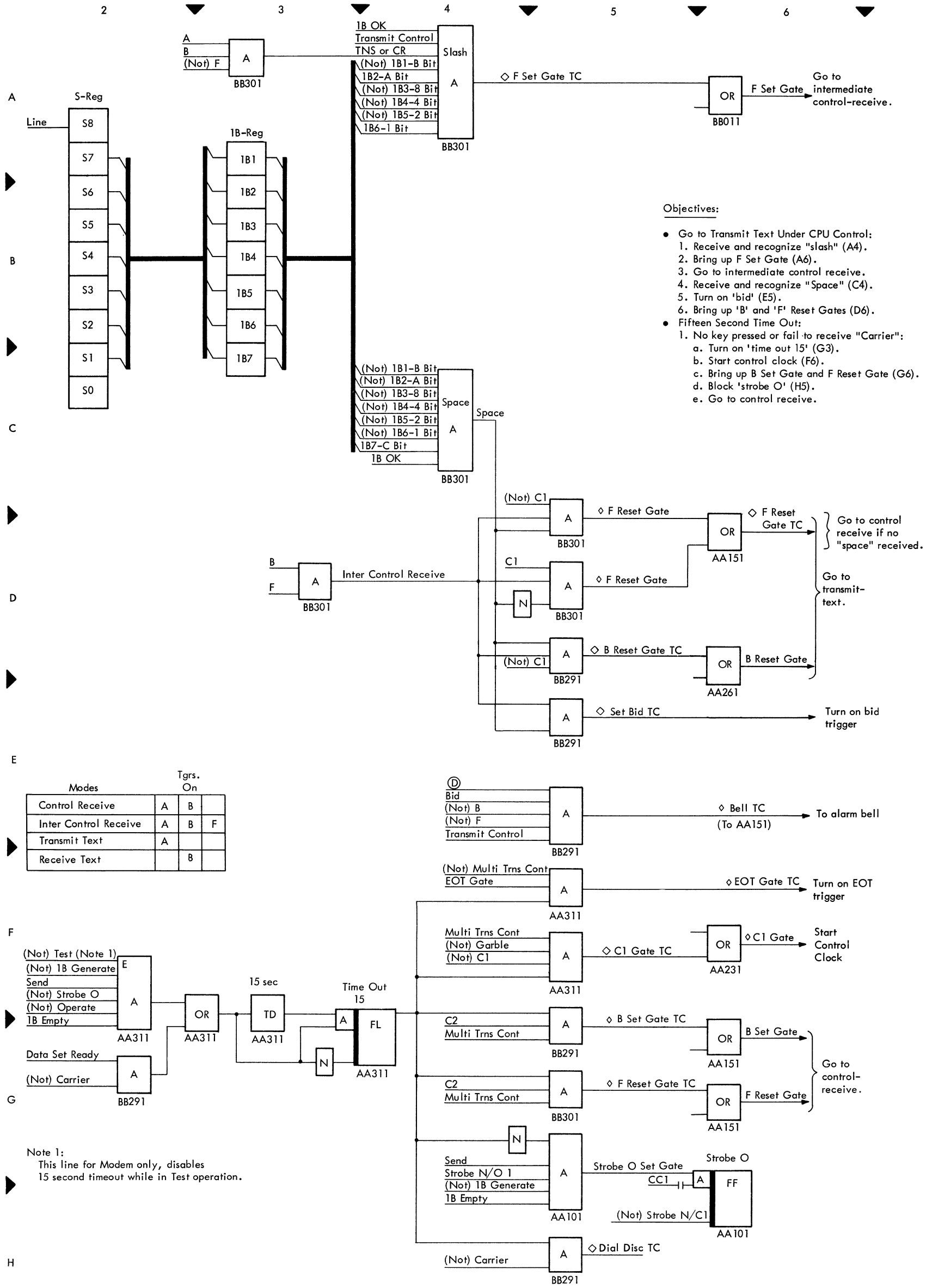


Diagram 5-26. Transmit Control (2740-1)

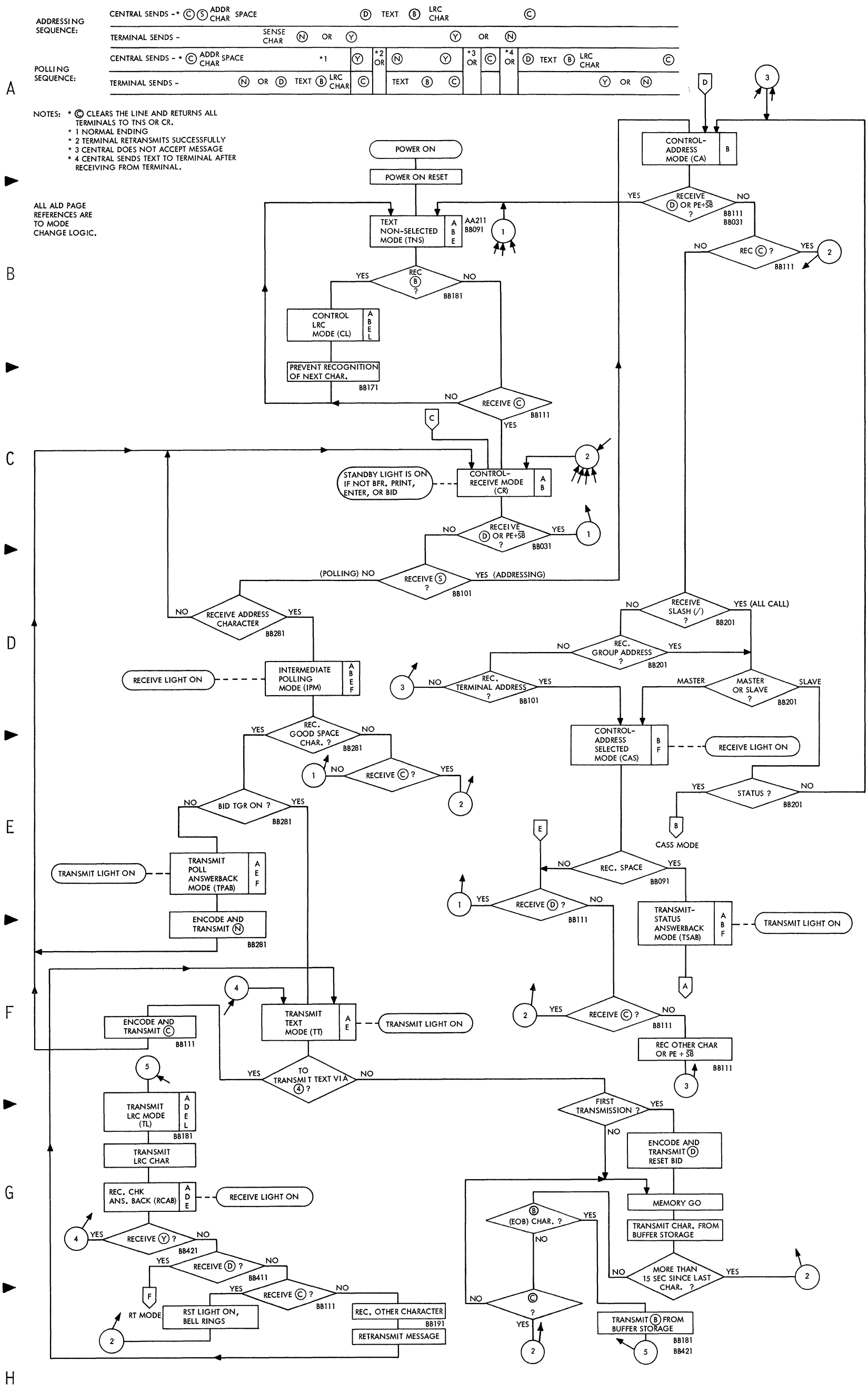
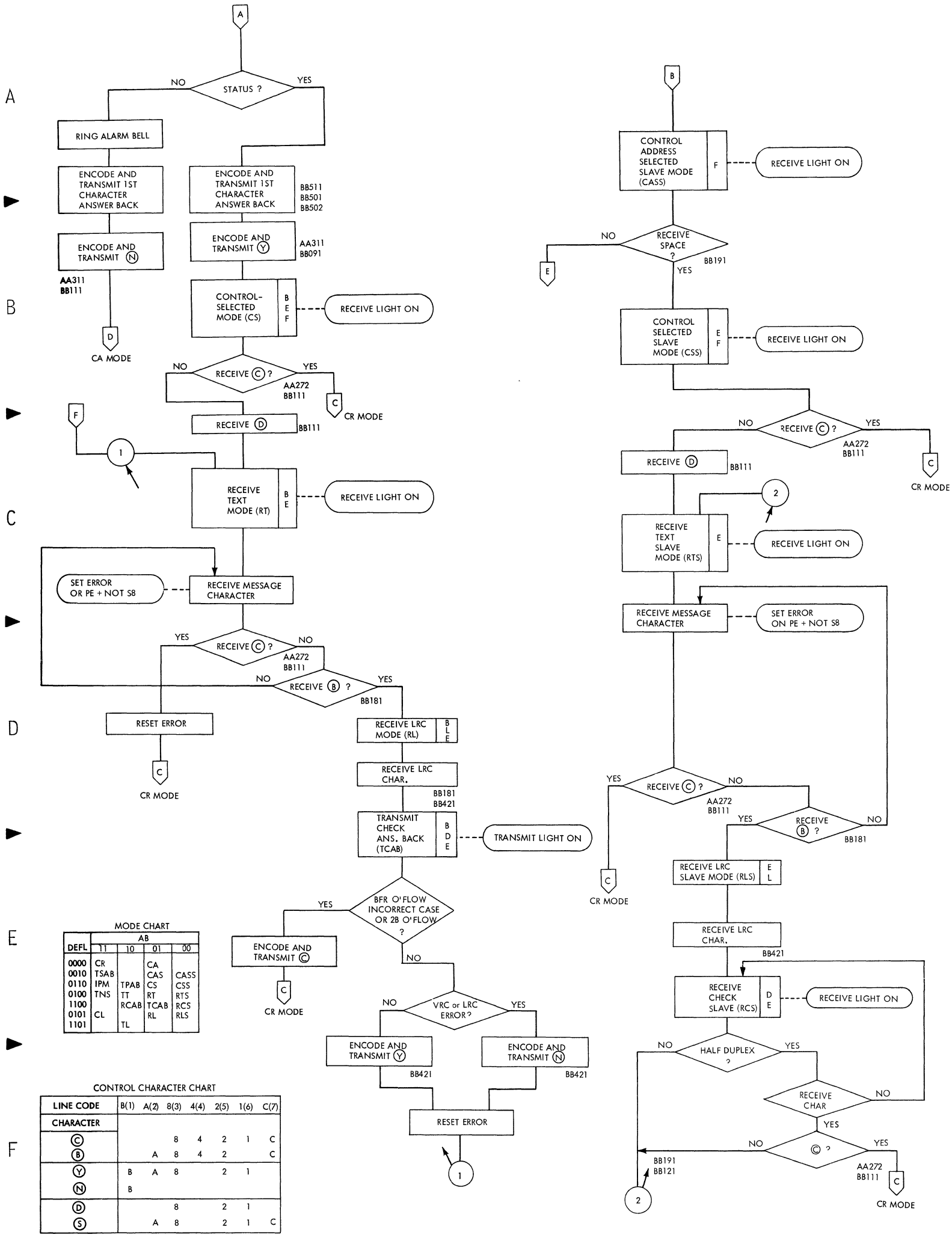


Diagram 5-27. Mode Control, Part 1 of 2 (2740-2)



MODE CHART

DEFL	AB 11	10	01	00
0000	CR		CA	
0010	TSAB		CAS	CASS
0110	IPM	TPAB	CS	CSS
0100	TNS	TT	RT	RTS
1100		RCAB	TCAB	RCS
0101	CL		RL	RLS
1101		TL		

CONTROL CHARACTER CHART

LINE CODE	B(1)	A(2)	8(3)	4(4)	2(5)	1(6)	C(7)
CHARACTER							
(C)			8	4	2	1	C
(B)		A	8	4	2		C
(Y)	B	A	8		2	1	
(N)	B						
(D)			8		2	1	
(S)		A	8		2	1	C

Diagram 5-27. Mode Control, Part 2 of 2 (2740-2)

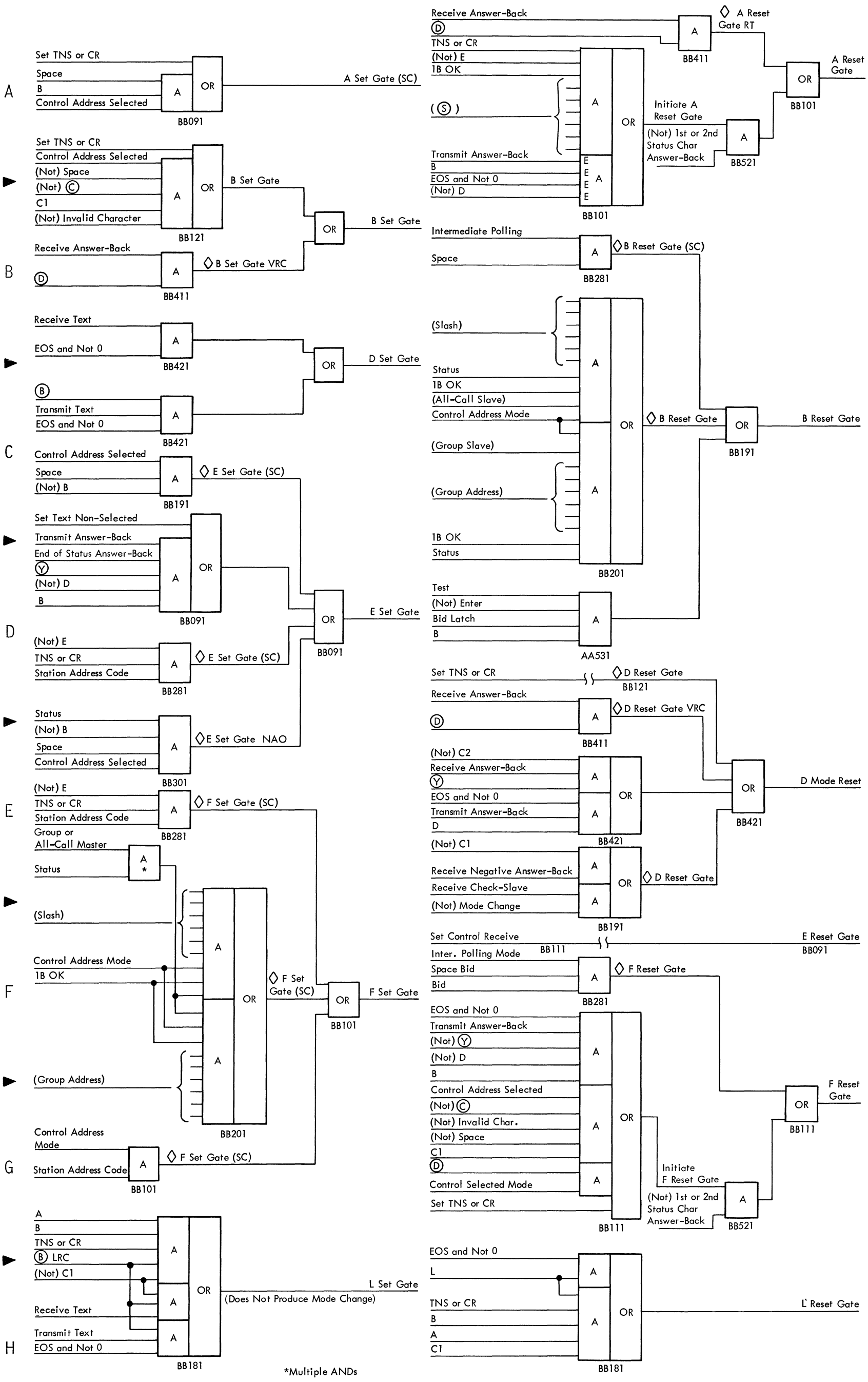


Diagram 5-28. Mode Control (2740-2)

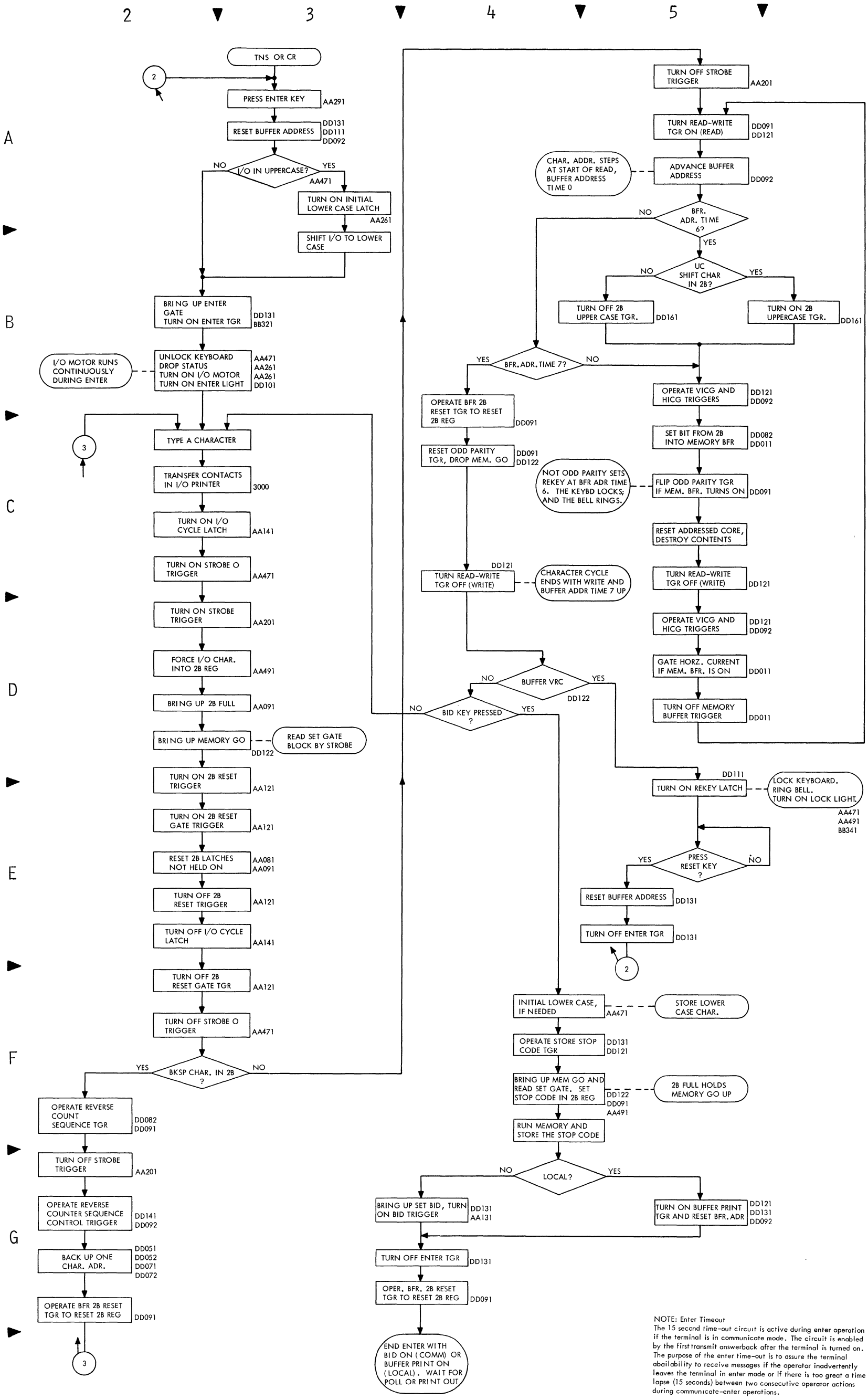
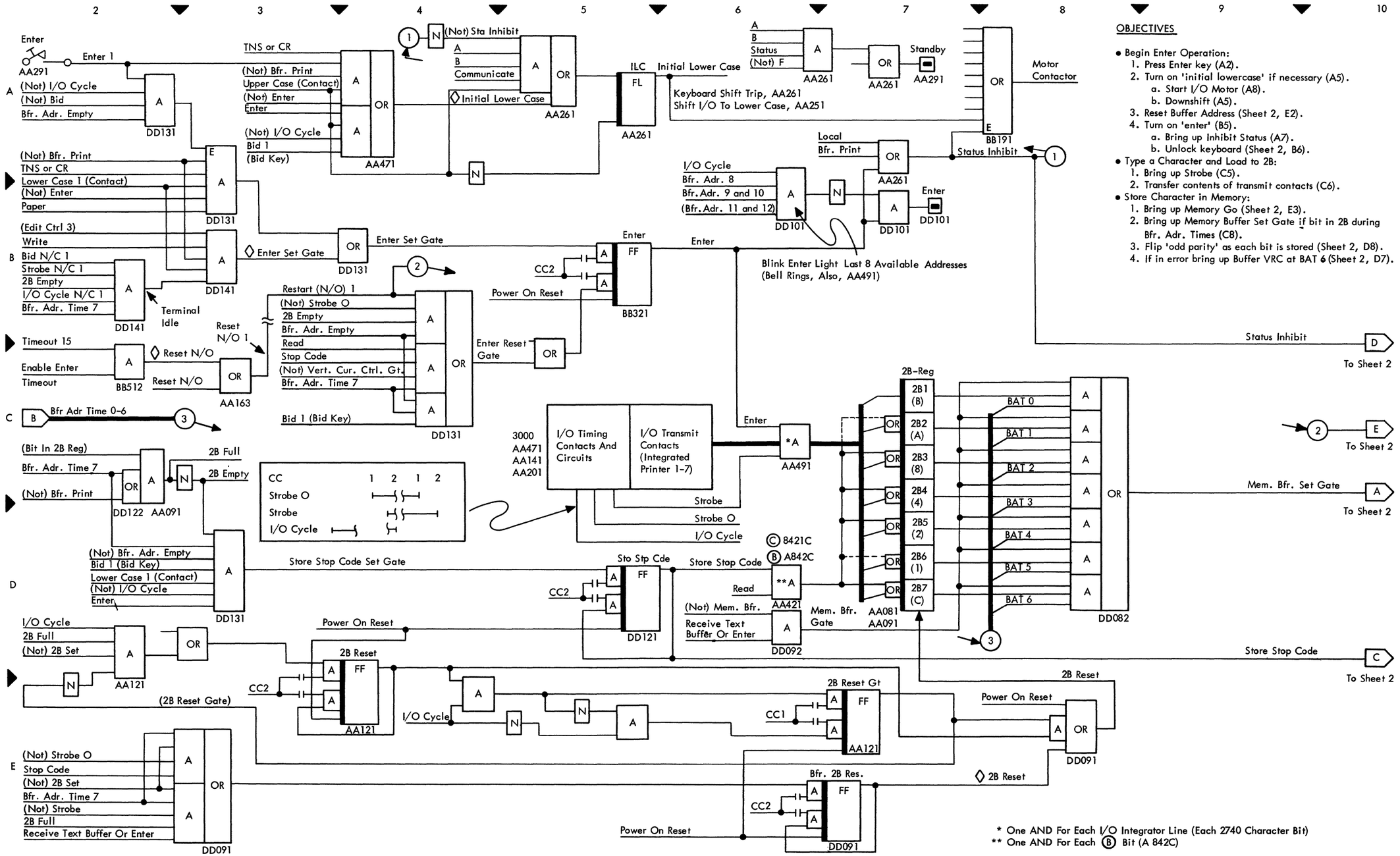
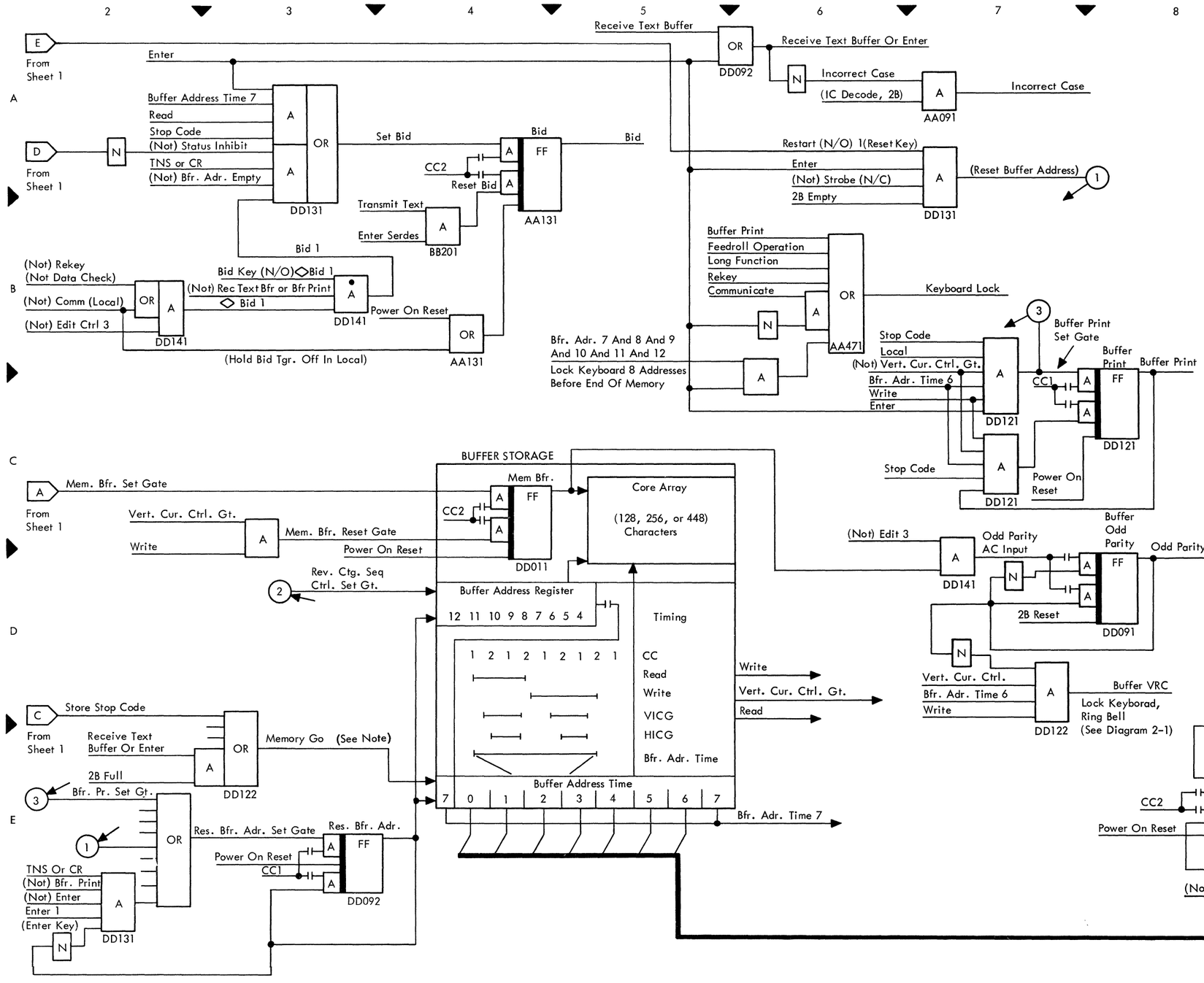


Diagram 5-29. Enter (2740-2)

Diagram 5-30. Enter (2740-2) Part 1 of 2





OBJECTIVES (Cont.)

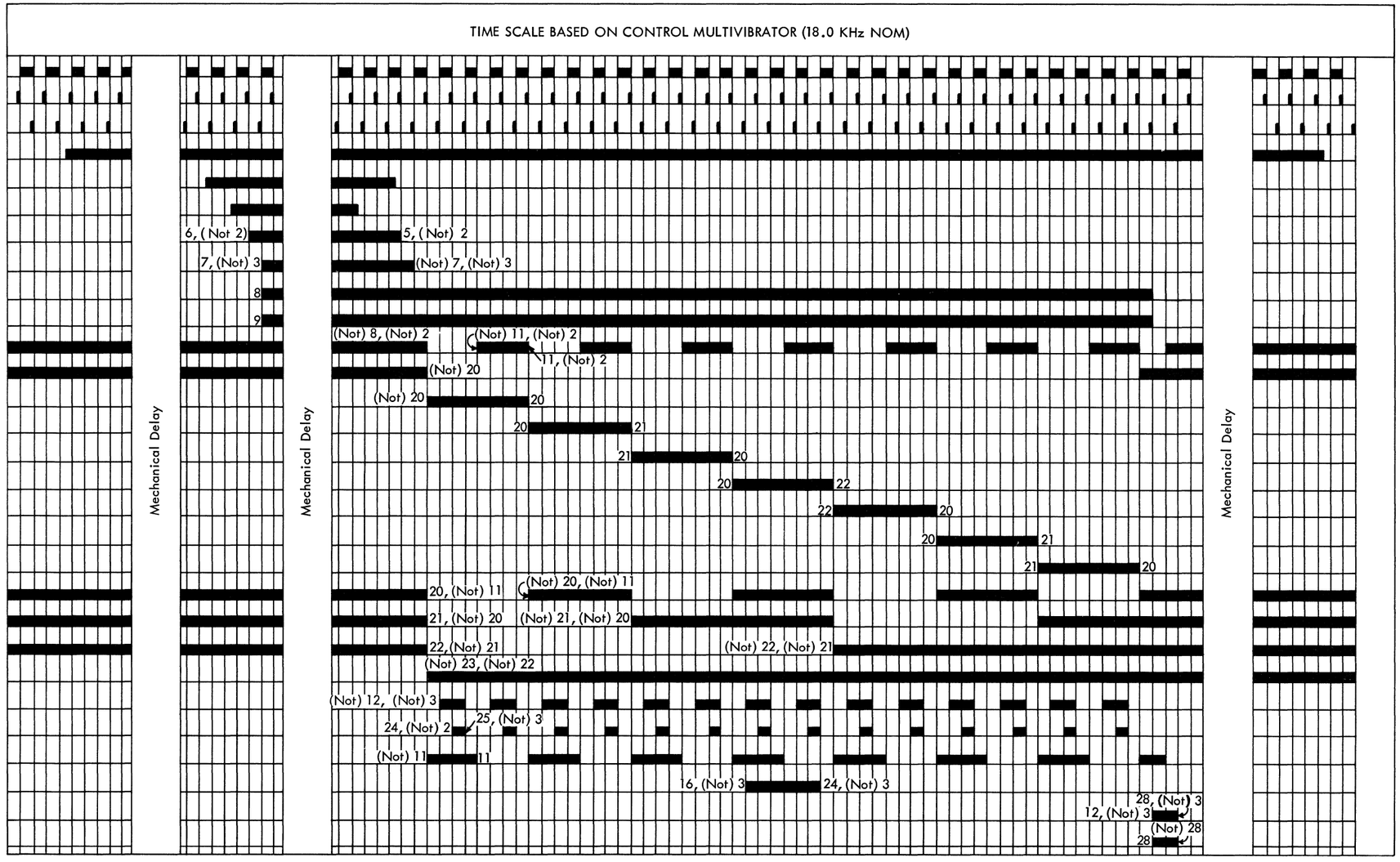
- Back Up Address to Correct a Character:
  1. Press Backspace key.
  2. Turn on 'rev ctg seq' (E9).
  3. Buffer backs up one address (D4).
  4. Correct character can be typed.
- Reset 2B Reg to Receive Next Character:
  1. Turn on 'Bfr. 2B Reset' (Sheet 1, E6).
  2. Bring up 2B Reset (Sheet 1, E8).
- Reach End Of Memory:
  1. Ring bell and blink Enter light 9 - 16 characters before end of memory (Sheet 1, B6).
  2. Lock keyboard 8 characters before absolute end of memory (B5).
- End Enter Operation:
  1. Press Bid key.
  2. Downshift if needed (Sheet 1, A5).
  3. Turn on 'sto stp code' (Sheet 1, D5).
  4. Store stop code.
     a. (B) with checking feature (Sheet 1, D5)
     b. (C) without checking feature (Sheet 1, D5)
  5. Turn on 'bid' (A4).
  6. Turn on 'buffer print' if in local (C8).
  7. Turn off 'enter' (Sheet 1, B4).

- Enter Time Out
  1. Bring up 'transmit answerback.'
  2. Turn on 'enable enter timeout' (Sheet 1, C2).
  3. Start '15 sec' time delay.
  4. No operator activity at keyboard for 15 seconds.
  5. Set 'time out 15' (Sheet 1, C2).
  6. Bring up ' ◆ reset N/O' (Sheet 1, C3).
  7. Reset 'enter' trigger (Sheet 1, B6) 'reset buffer address' (A7), and reset 'rekey' latch (if set).

Note:
Memory Go cannot start storage timing during 1B Generate, 2B Set, Strobe, Reset Buffer Address, or Reverse Counting Sequence.

Diagram 5-31. Enter (2740-2)

	NO.	SIGNAL NAME	SP	LOGIC
A	1	CMV	G6J13	AA361
	2	CC1	F7D07	AA051
	3	CC2	F7D04	AA051
	4	KYBD Contact		
	5	Strobe N/C 1	J2D06	AA161
	6	Strobe N/O 1	J2B09	AA161
►	7	Strobe O	E2G12	AA471
	8	Strobe	E4D05	AA201
	9	2B Full	D2B07	AA091
	10	Memory Go	E4G12	DD122
B	11	Write	E4J02	DD121
	12	Buffer Address Time 7	F6G04	DD081
	13	Buffer Address Time 0	F6G09	DD081
	14	Buffer Address Time 1	F6J05	DD081
►	15	Buffer Address Time 2	F6J02	DD081
	16	Buffer Address Time 3	F6J04	DD081
	17	Buffer Address Time 4	F6G02	DD081
	18	Buffer Address Time 5	F6B10	DD081
C	19	Buffer Address Time 6	F6J09	DD081
	20	BFR Address 1	F6G13	DD081
	21	BFR Address 2	F6J07	DD081
	22	BFR Address 3	F6G12	DD081
►	23	BFR Address 4	G6B03	DD072
	24	Vertical Current Control Gate	E4D12	DD121
	25	Horizontal Current Control Gate	E6J04	DD092
	26	Read Odd Write Even	E4J12	DD122
D	27	Memory BFR	M4J13	DD011
	28	BFR 2B Reset	E6D07	DD091
	29	2B Reset	F2G08	AA121



Note: In the Enter Mode, Transfer a Character (Numeral 4) from Keyboard to 2B, then from 2B to Memory

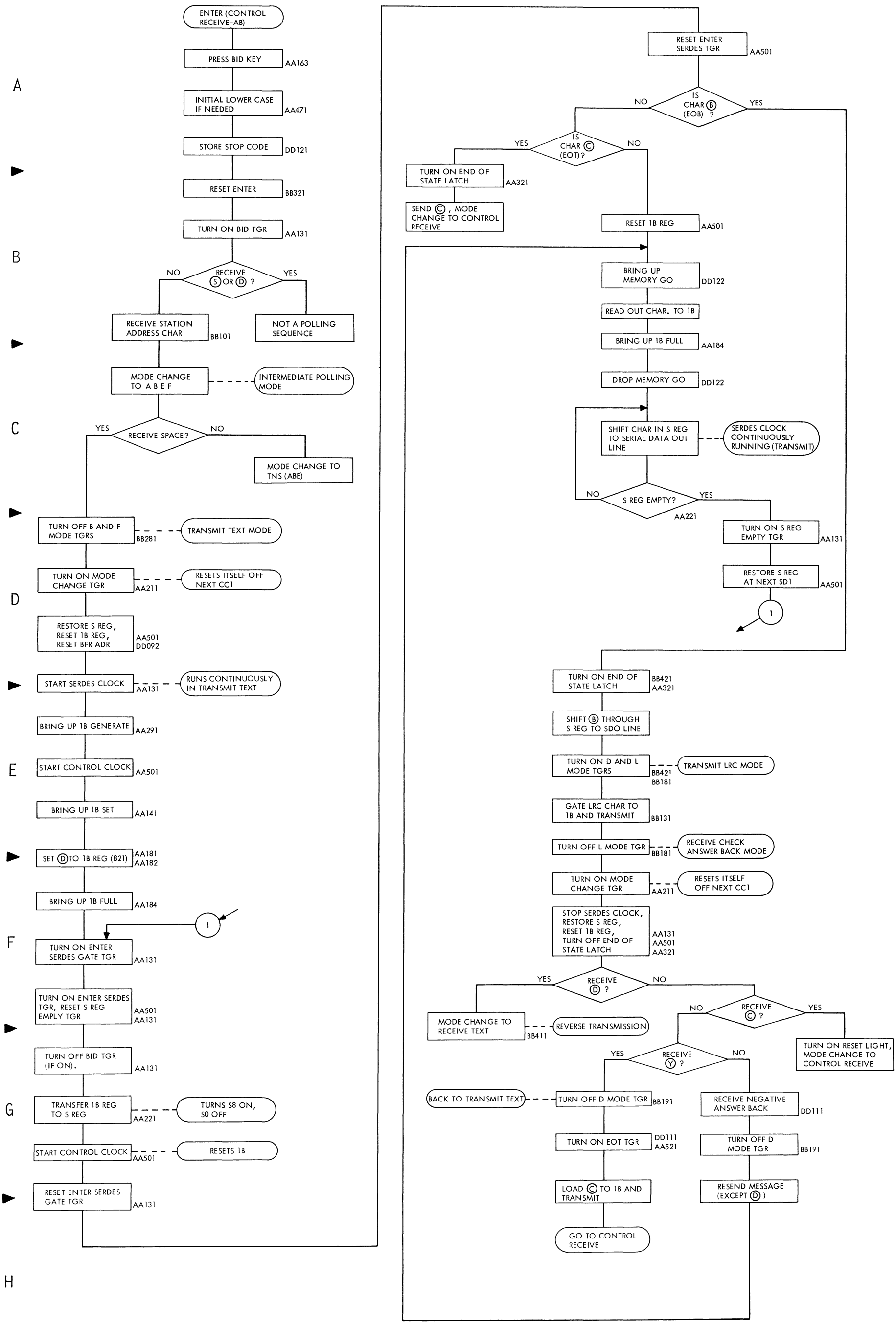
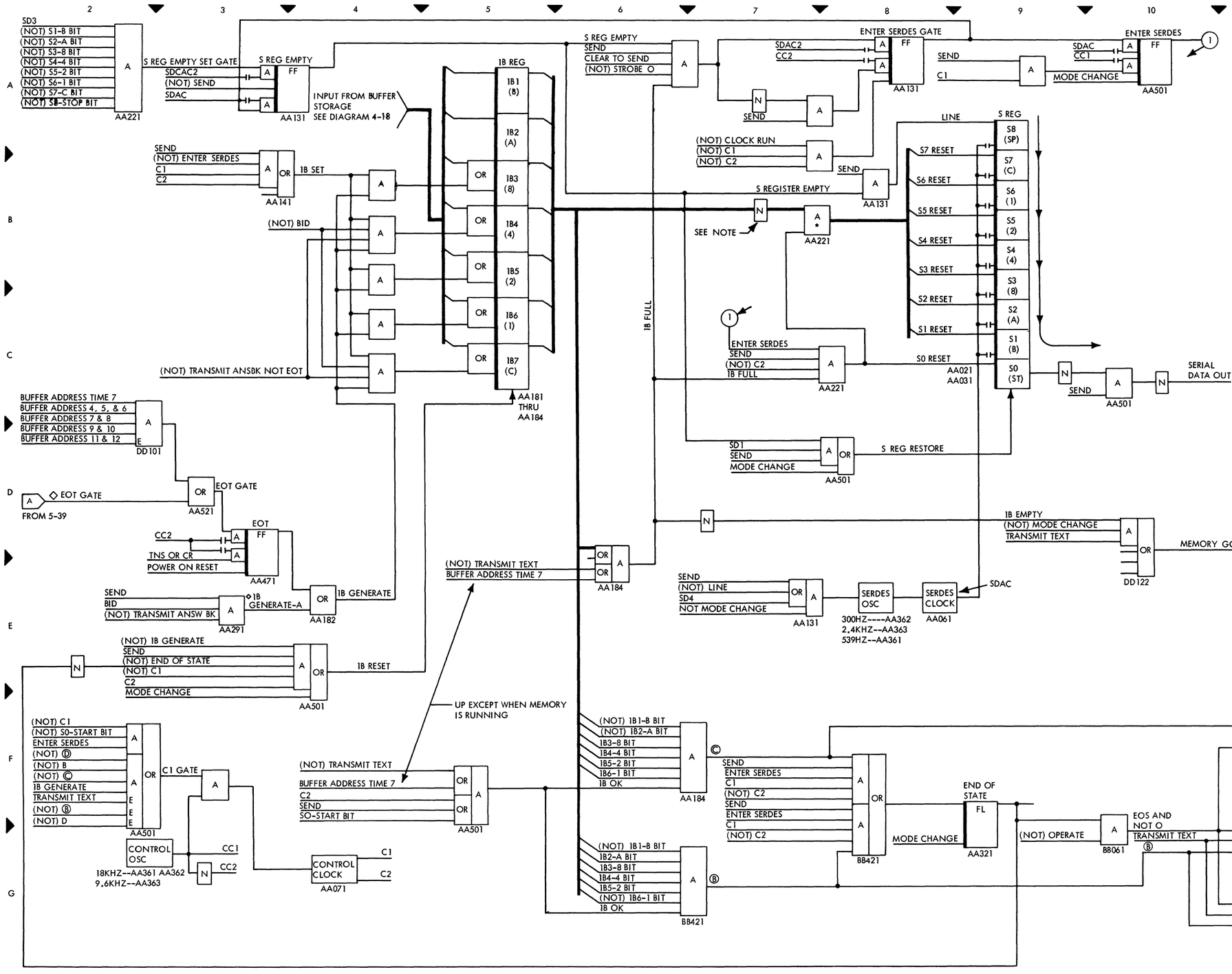


Diagram 5-32. Transmit (2740-2)



OBJECTIVES

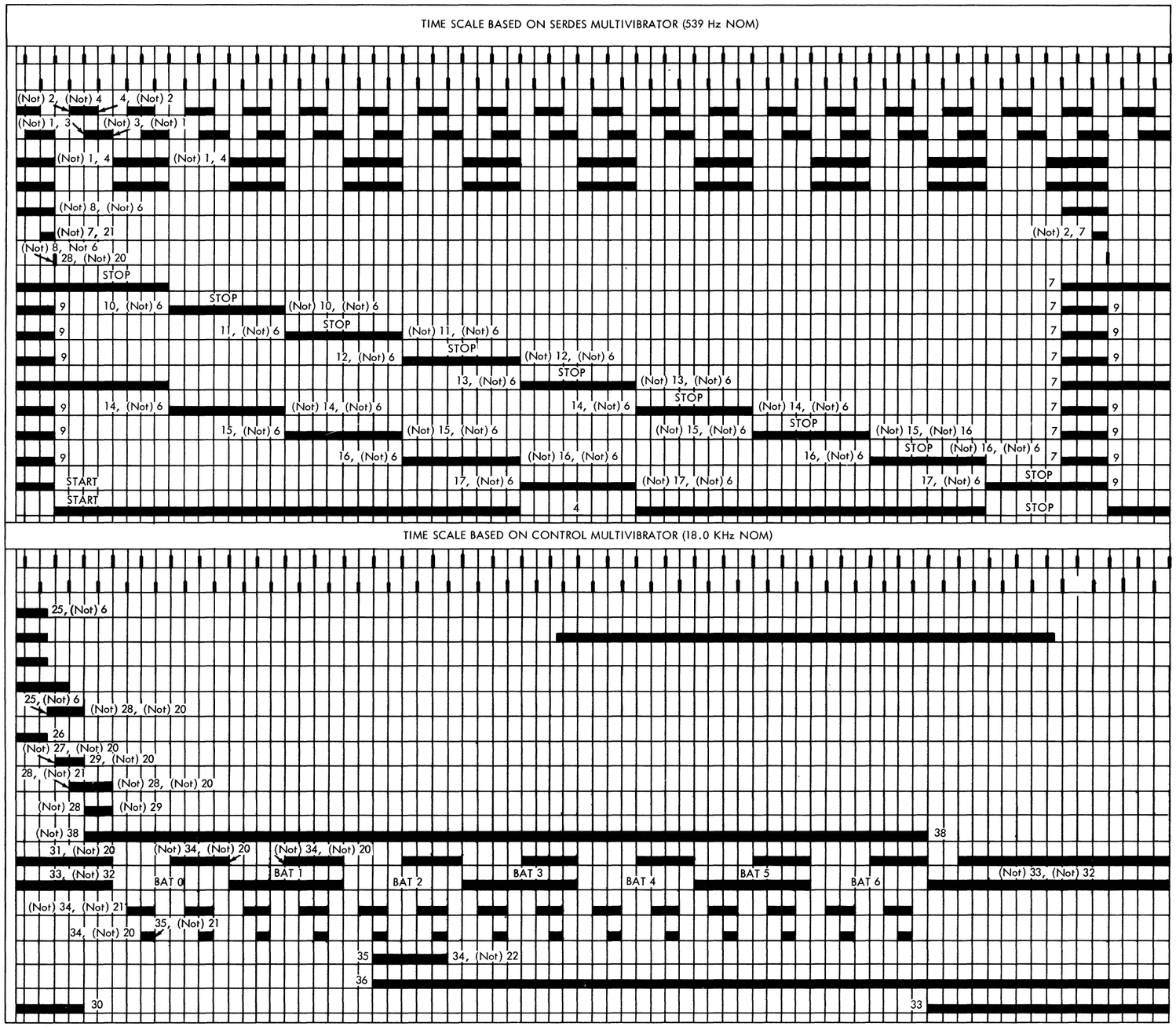
- GENERATE Ⓓ (8, 2, 1, BITS) AFTER SUCCESSFUL POLL:
  1. BRING UP 1B GENERATE (E4).
  2. START CONTROL CLOCK (G4).
  3. BRING UP 1B SET (B3).
  4. NOT TRANSMIT ANSBK NOT EOT BLOCKS SET OF '1B4' AND '1B7' (C4).
- TRANSFER CHARACTER TO S REGISTER:
  1. 'S REGISTER EMPTY' TURNED ON BY NOT SEND (FROM PREVIOUS MODE) OR WHEN S REGISTER EMPTIED FOLLOWING TRANSMISSION OF PREVIOUS CHARACTER (A4).
  2. TURN ON 'ENTER SERDES GATE' AND BRING UP S REGISTER RESTORE (A8 AND C8).
  3. TURN ON 'ENTER SERDES' (A10).
- TRANSMIT CHARACTER:
  1. SERDES CLOCK RUNS CONTINUOUSLY DURING SEND OPERATIONS (E8).
  2. CHARACTER IS SHIFTED TO SERIAL DATA OUT LINE
- RESET 1B REGISTER:
  1. START CONTROL CLOCK (G4).
  2. BRING UP 1B RESET (E4).
- LOAD 1B FROM BUFFER STORAGE:
  1. BRING UP MEMORY GO (D10).
  2. SCAN CHARACTER TO 1B.
- DETECT FINAL CHARACTER FROM MEMORY:
  - A. IF Ⓑ (CHECKING)
    1. RECOGNIZE Ⓑ (G7).
    2. TURN ON 'END OF STATE' (F9).
    3. PREVENT 1B RESET (E4).
    4. GO TO TRANSMIT LRC MODE (G12).
    5. RESET 1B DURING MODE CHANGE (E4).
  - B. IF Ⓒ (WITHOUT CHECKING)
    1. RECOGNIZE Ⓒ WHILE IN 1B (F7).
    2. TURN ON 'END OF STATE (F9).
    3. WHEN Ⓒ IS TRANSMITTED, BRING UP SET CONTROL RECEIVE (F12).
    4. GO TO CONTROL RECEIVE.
    5. RESET 'END OF STATE' (F9) AND 1B (E4) WITH MODE CHANGE.

* MULTIPLE ANDs.

NOTE: BECAUSE S REG TRIGGERS ARE RESTORED ON, THE "NO BITS" FROM THE 1B REG ARE LOADED INTO THE S REG.

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

	NO.	SIGNAL NAME	SP	LOGIC
	1	SDCAC1	G1D05	AA052
	2	SDCAC2	G1D04	AA052
A	3	SD1	H2D05	AA061
	4	SD2	H2D04	AA061
	5	SD3	H2D02	AA061
	6	SDAC	G1D07	AA052
▶	7	S Reg Empty	G2B03	AA131
	8	Enter Serdes Gate	G2D06	AA131
	9	Enter Serdes	D6J12	AA501
	10	S8-Stop Bit	H4D07	AA021
	11	S7-C Bit	H4D10	AA021
B	12	S6-1 Bit	H4J11	AA021
	13	S5-2 Bit	H4B12	AA021
	14	S4-4 Bit	H4G02	AA031
	15	S3-8 Bit	H4J13	AA031
▶	16	S2-A Bit	H4G09	AA031
	17	S1-B Bit	H4J06	AA031
	18	S0-Start Bit	H4G07	AA031
	19	SER Data Out	D6B03	AA501
C	20	CC1	F7D07	AA051
	21	CC2	F7D04	AA051
	22	S Reg Empty	G2B03	AA131
▶	23	SDCAC1	G1D05	AAC52
	24	SDAC	G1D07	AA052
	25	Enter Serdes Gate	G2D06	AA131
	26	Enter Serdes	D6J12	AA501
	27	S0	H4G07	AA031
D	28	C1	H2G04	AA071
	29	C2	H2G07	AA071
	30	1B Reset	D6J09	AA501
	31	Memory Go	E4G12	DD122
▶	32	Write	E4J02	DD121
	33	BFR Address 1	F6J05	DD081
	34	Vertical Current Control Gate	E4D12	DD121
	35	Horz Current Control Gate	E6J04	DD092
E	36	Memory BFR	M4J13	DD011
	37	1B3	D4D05	AA184
	38	1B Full	D4B04	AA184



Note:
Transfer character (Numeral 4) from 1B to Serdes and begin transmission, then read from memory (Numeral 8) and store in 1B.

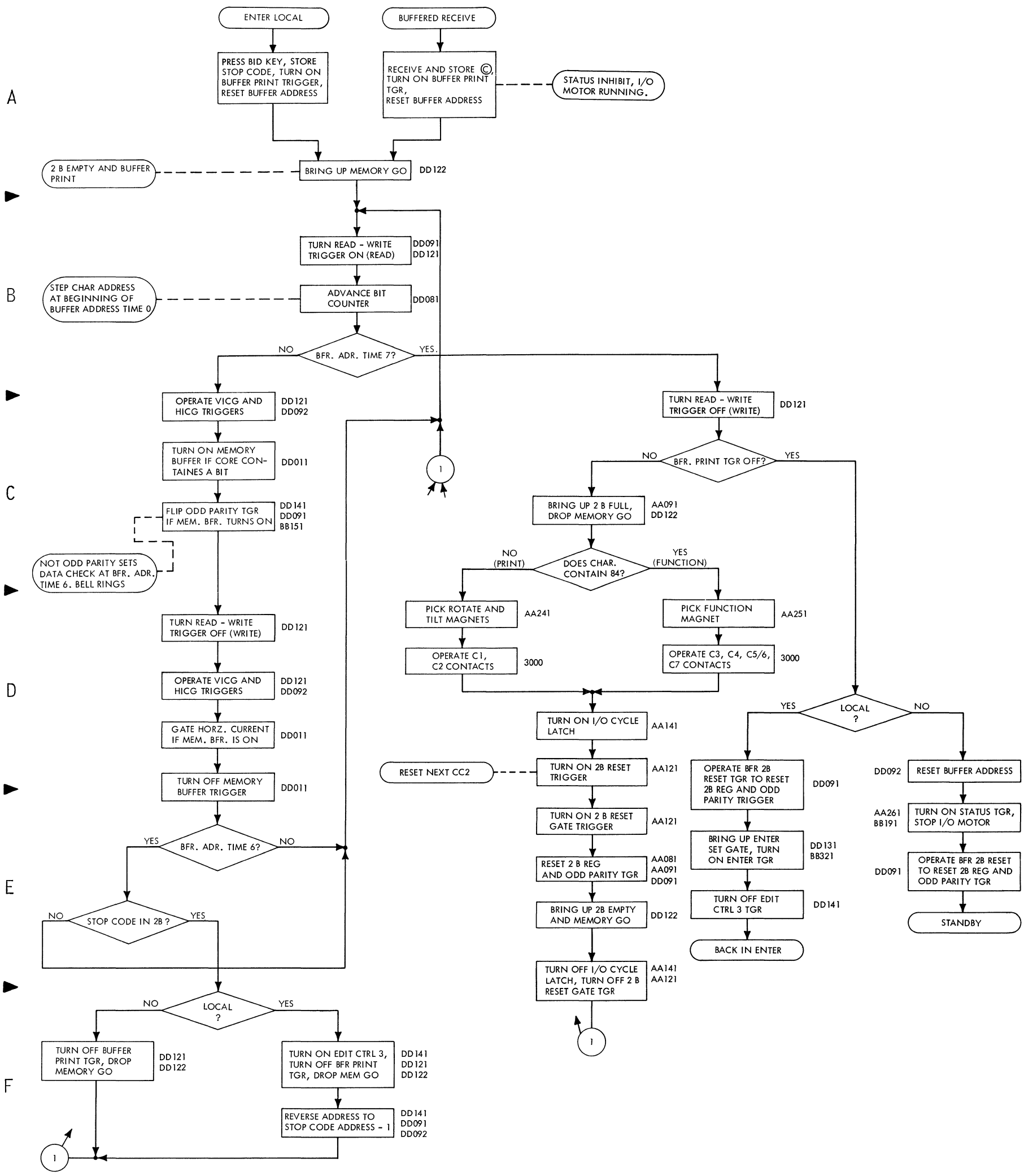
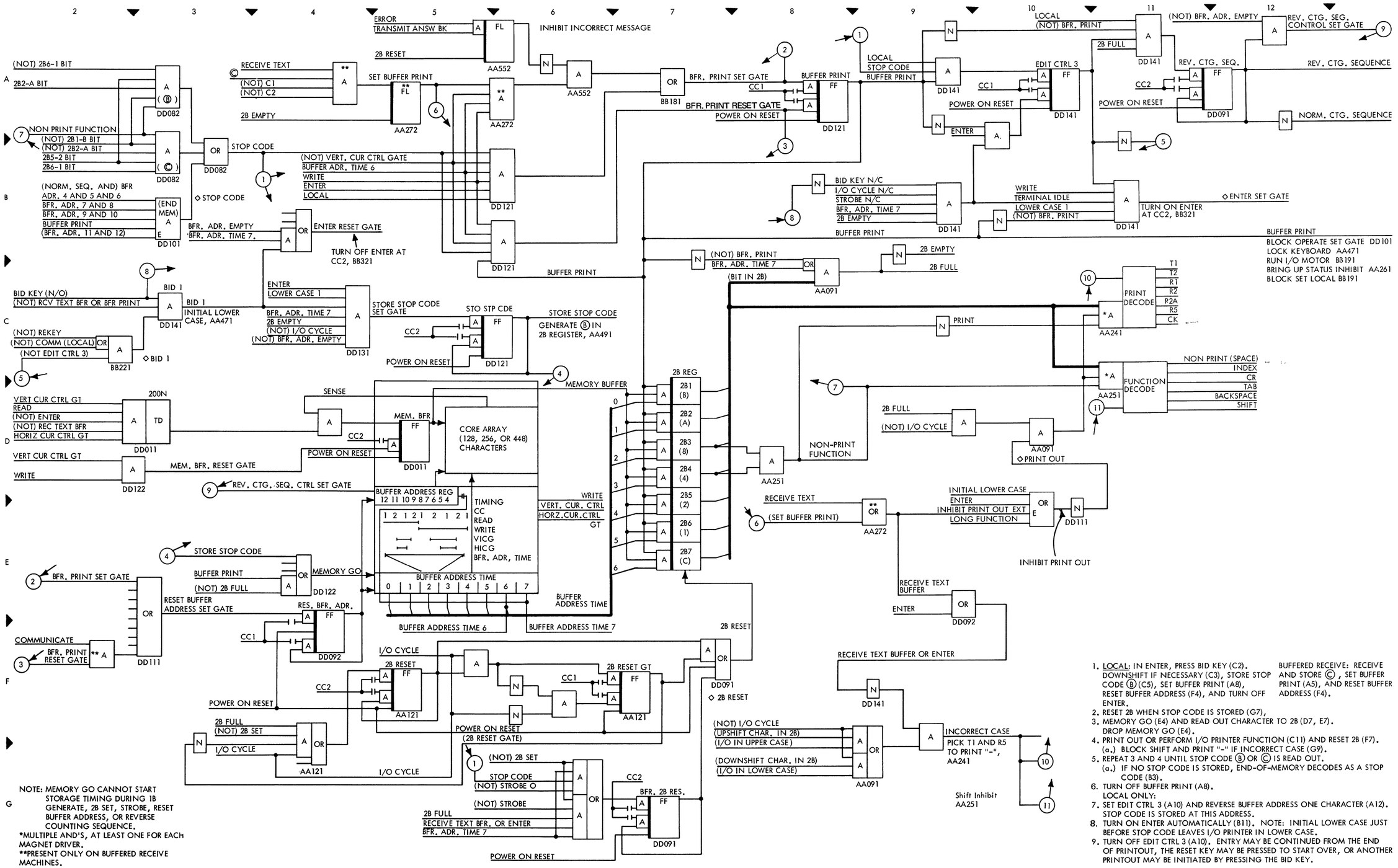


Diagram 5-35. Buffer Print (2740-2)



NOTE: MEMORY GO CANNOT START STORAGE TIMING DURING 1B GENERATE, 2B SET, STROBE, RESET BUFFER ADDRESS, OR REVERSE COUNTING SEQUENCE.
*MULTIPLE AND'S, AT LEAST ONE FOR EACH MAGNET DRIVER.
**PRESENT ONLY ON BUFFERED RECEIVE MACHINES.

BUFFER PRINT
BLOCK OPERATE SET GATE DD101
LOCK KEYBOARD AA471
RUN I/O MOTOR BB191
BRING UP STATUS INHIBIT AA261
BLOCK SET LOCAL BB191

1. LOCAL: IN ENTER, PRESS BID KEY (C2). DOWNSHIFT IF NECESSARY (C3), STORE STOP CODE (B) (C5), SET BUFFER PRINT (A8), RESET BUFFER ADDRESS (F4), AND TURN OFF ENTER.
   BUFFERED RECEIVE: RECEIVE AND STORE (C), SET BUFFER PRINT (A5), AND RESET BUFFER ADDRESS (F4).
2. RESET 2B WHEN STOP CODE IS STORED (G7),
3. MEMORY GO (E4) AND READ OUT CHARACTER TO 2B (D7, E7). DROP MEMORY GO (E4).
4. PRINT OUT OR PERFORM I/O PRINTER FUNCTION (C11) AND RESET 2B (F7).
   (a.) BLOCK SHIFT AND PRINT "-" IF INCORRECT CASE (G9).
5. REPEAT 3 AND 4 UNTIL STOP CODE (B) OR (C) IS READ OUT.
   (a.) IF NO STOP CODE IS STORED, END-OF-MEMORY DECODES AS A STOP CODE (B3).
6. TURN OFF BUFFER PRINT (A8).
   LOCAL ONLY:
7. SET EDIT CTRL 3 (A10) AND REVERSE BUFFER ADDRESS ONE CHARACTER (A12). STOP CODE IS STORED AT THIS ADDRESS.
8. TURN ON ENTER AUTOMATICALLY (B11). NOTE: INITIAL LOWER CASE JUST BEFORE STOP CODE LEAVES I/O PRINTER IN LOWER CASE.
9. TURN OFF EDIT CTRL 3 (A10). ENTRY MAY BE CONTINUED FROM THE END OF PRINTOUT, THE RESET KEY MAY BE PRESSED TO START OVER, OR ANOTHER PRINTOUT MAY BE INITIATED BY PRESSING THE BID KEY.

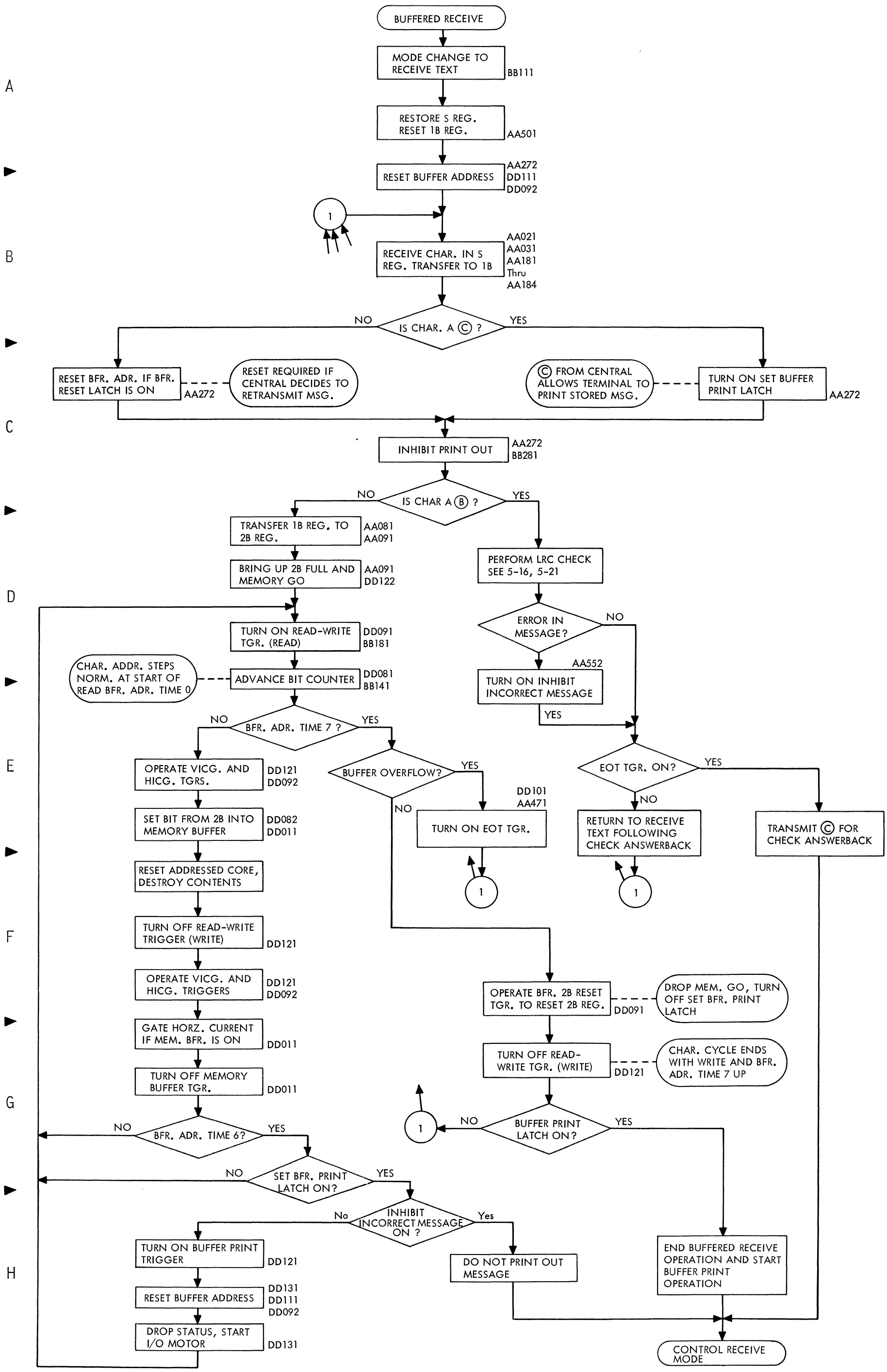
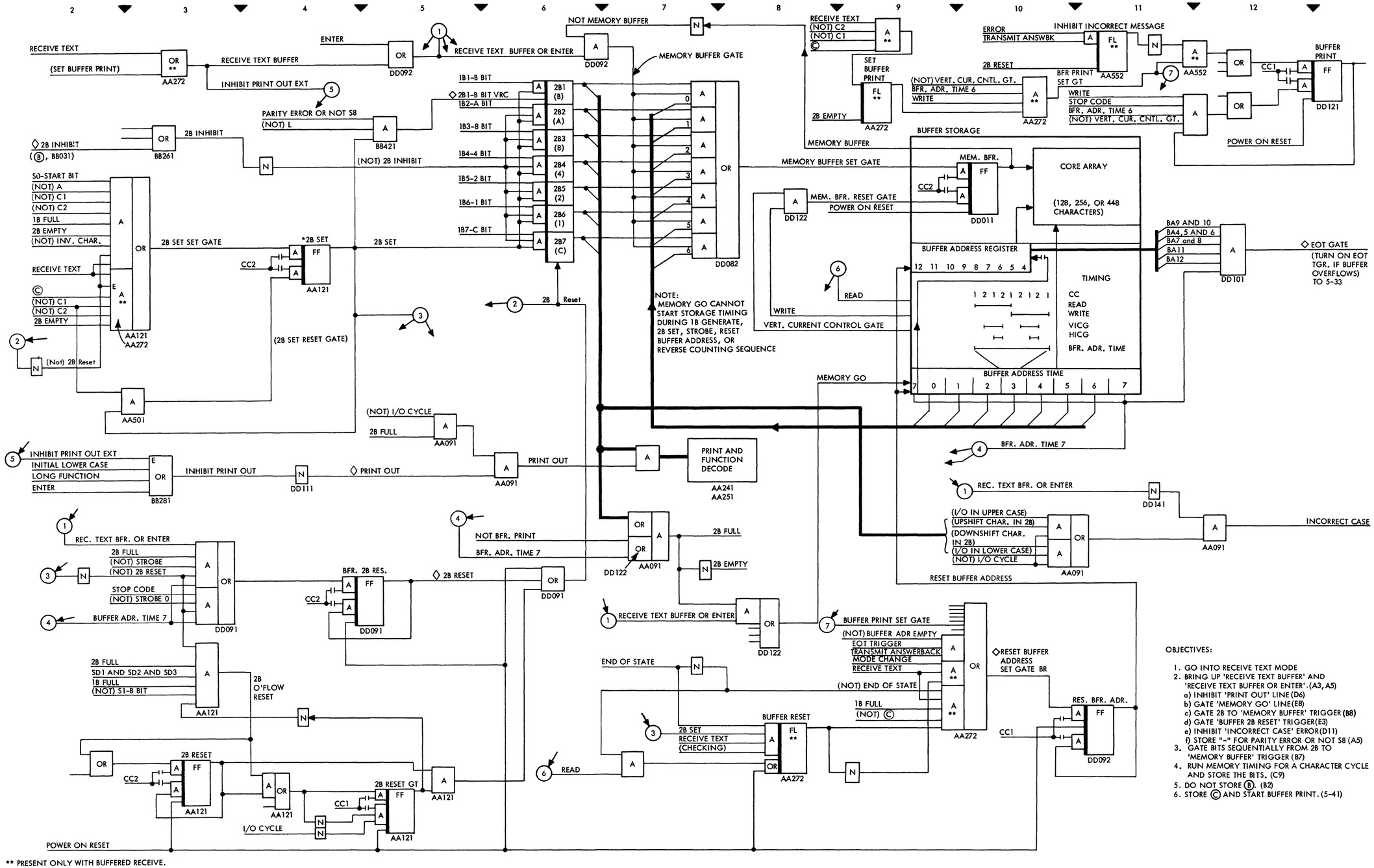


Diagram 5-37. Buffered Receive (2740-2)


RECEIVE TEXT
(SET BUFFER PRINT)
OR ** AA272
RECEIVE TEXT BUFFER
INHIBIT PRINT OUT EXT
ENTER
OR DD092
RECEIVE TEXT BUFFER OR ENTER
NOT MEMORY BUFFER
A DD092
MEMORY BUFFER GATE
PARITY ERROR OR NOT S8
(NOT) L
A BB421
1B1-B BIT
◇2B1-B BIT VRC
1B2-A BIT
1B3-B BIT
1B4-4 BIT
1B5-2 BIT
1B6-1 BIT
1B7-C BIT
2B1 (B)
2B2 (A)
2B3 (B)
2B4 (4)
2B5 (2)
2B6 (1)
2B7 (C)
◇2B INHIBIT
(B), BB031)
OR BB261
2B INHIBIT
(NOT) 2B INHIBIT
S0-START BIT
(NOT) A
(NOT) C1
(NOT) C2
1B FULL
2B EMPTY
(NOT) INV. CHAR.
RECEIVE TEXT
©
(NOT) C1
(NOT) C2
2B EMPTY
AA121
AA272
2B SET SET GATE
*2B SET
FF AA121
CC2
2B SET
(2B SET RESET GATE)
(Not) 2B Reset
AA501
2B Reset
NOTE:
MEMORY GO CANNOT START STORAGE TIMING DURING 1B GENERATE, 2B SET, STROBE, RESET BUFFER ADDRESS, OR REVERSE COUNTING SEQUENCE
OR DD082
0 1 2 3 4 5 6
RECEIVE TEXT
(NOT) C2
(NOT) C1
©
SET BUFFER PRINT
FL ** AA272
2B EMPTY
ERROR
TRANSMIT ANSWBK
INHIBIT INCORRECT MESSAGE
FL ** AA552
2B RESET
BFR PRINT SET GT
AA552
(NOT) VERT. CUR. CNTL. GT.
BFR. ADR. TIME 6
WRITE
A ** AA272
WRITE
STOP CODE
BFR. ADR. TIME 6
(NOT) VERT. CUR. CNTL. GT.
OR
CC1
BUFFER PRINT
FF DD121
POWER ON RESET
BUFFER STORAGE
MEMORY BUFFER
MEMORY BUFFER SET GATE
MEM. BFR.
FF DD011
CC2
CORE ARRAY
(128, 256, OR 448 CHARACTERS)
MEM. BFR. RESET GATE
POWER ON RESET
A DD122
BUFFER ADDRESS REGISTER
12 11 10 9 8 7 6 5 4
BA9 AND 10
BA4,5 AND 6
BA7 and 8
BA11
BA12
A DD101
◇EOT GATE
(TURN ON EOT TGR. IF BUFFER OVERFLOWS) TO 5-33
READ
WRITE
VERT. CURRENT CONTROL GATE
TIMING
1 2 1 2 1 2 1 2 1
CC
READ
WRITE
VICG
HICG
BFR. ADR. TIME
BUFFER ADDRESS TIME
7 0 1 2 3 4 5 6 7
MEMORY GO
BFR. ADR. TIME 7
REC. TEXT BFR. OR ENTER
N DD141
(I/O IN UPPER CASE)
(UPSHIFT CHAR. IN 2B)
(DOWNSHIFT CHAR. IN 2B)
(I/O IN LOWER CASE)
(NOT) I/O CYCLE
A OR A AA091
INCORRECT CASE
RESET BUFFER ADDRESS
(NOT) I/O CYCLE
2B FULL
AA091
(NOT) 1/O CYCLE
2B FULL
AA091
PRINT OUT
A AA091
PRINT AND FUNCTION DECODE
AA241
AA251
INHIBIT PRINT OUT EXT
INITIAL LOWER CASE
LONG FUNCTION
ENTER
E OR BB281
INHIBIT PRINT OUT
N DD111
◇ PRINT OUT
REC. TEXT BFR. OR ENTER
2B FULL
(NOT) STROBE
(NOT) 2B RESET
STOP CODE
(NOT) STROBE 0
BUFFER ADR. TIME 7
A OR DD091
BFR. 2B RES.
FF DD091
CC2
◇ 2B RESET
OR DD091
NOT BFR. PRINT
BFR. ADR. TIME 7
OR OR DD122
2B FULL
AA091
2B EMPTY
RECEIVE TEXT BUFFER OR ENTER
A OR DD122
BUFFER PRINT SET GATE
(NOT) BUFFER ADR EMPTY
EOT TRIGGER
TRANSMIT ANSWERBACK
MODE CHANGE
RECEIVE TEXT
A ** A ** OR AA272
◇RESET BUFFER ADDRESS SET GATE BR
END OF STATE
(NOT) END OF STATE
1B FULL
(NOT) ©
BUFFER RESET
2B SET
RECEIVE TEXT
(CHECKING)
FL ** OR AA272
RES. BFR. ADR.
FF DD092
CC1
2B FULL
SD1 AND SD2 AND SD3
1B FULL
(NOT) S1-8 BIT
A AA121
2B O'FLOW RESET
2B RESET
FF AA121
CC2
OR AA121
2B RESET GT
FF AA121
CC1
I/O CYCLE
A AA121
READ
POWER ON RESET
** PRESENT ONLY WITH BUFFERED RECEIVE.
OBJECTIVES:
1. GO INTO RECEIVE TEXT MODE
2. BRING UP 'RECEIVE TEXT BUFFER' AND 'RECEIVE TEXT BUFFER OR ENTER'.(A3, A5)
a) INHIBIT 'PRINT OUT' LINE (D6)
b) GATE 'MEMORY GO' LINE(E8)
c) GATE 2B TO 'MEMORY BUFFER' TRIGGER (B8)
d) GATE 'BUFFER 2B RESET' TRIGGER(E3)
e) INHIBIT 'INCORRECT CASE' ERROR(D11)
f) STORE "-" FOR PARITY ERROR OR NOT S8 (A5)
3. GATE BITS SEQUENTIALLY FROM 2B TO 'MEMORY BUFFER' TRIGGER (B7)
4. RUN MEMORY TIMING FOR A CHARACTER CYCLE AND STORE THE BITS. (C9)
5. DO NOT STORE (B). (B2)
6. STORE © AND START BUFFER PRINT. (5-41)

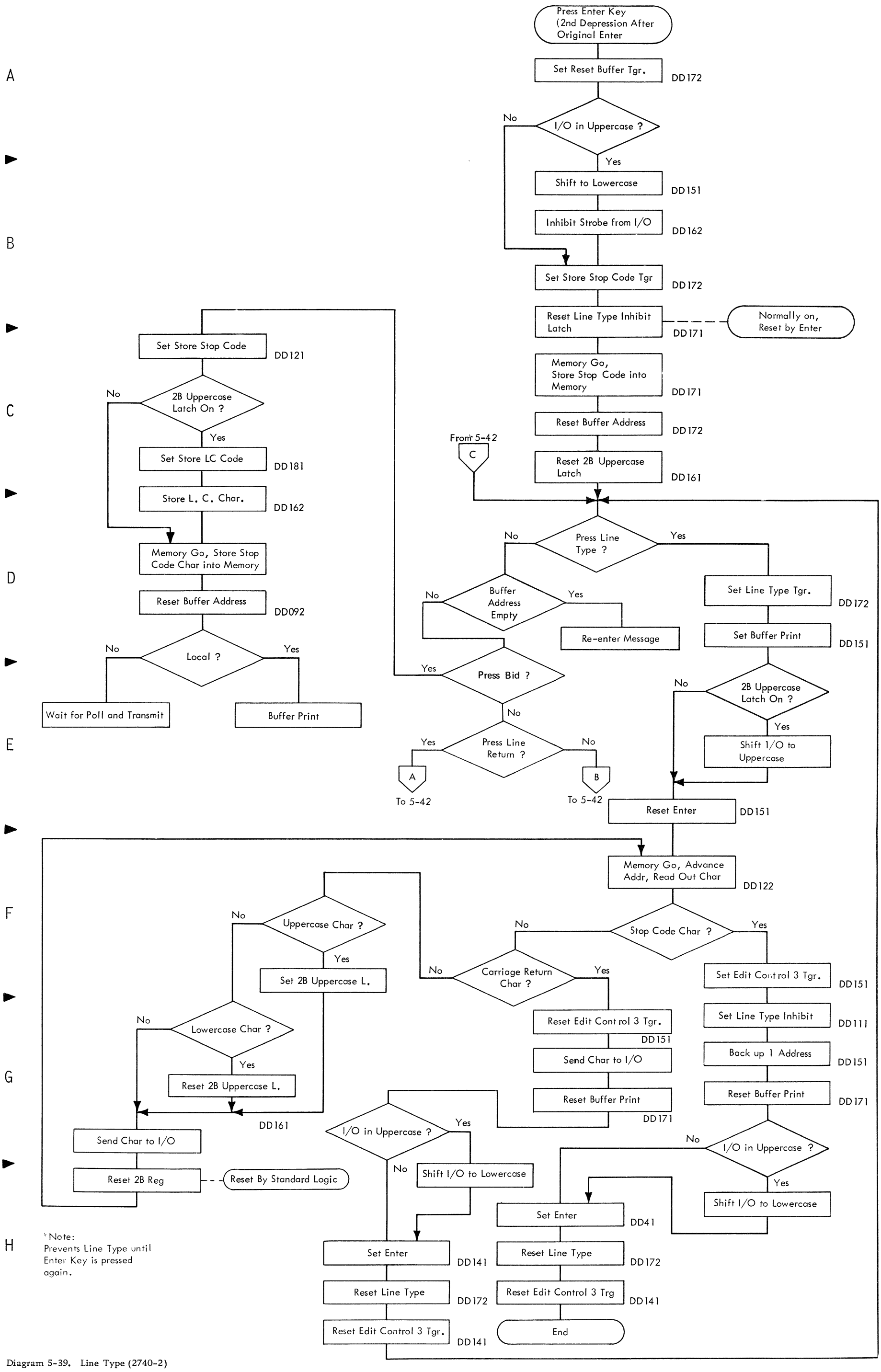
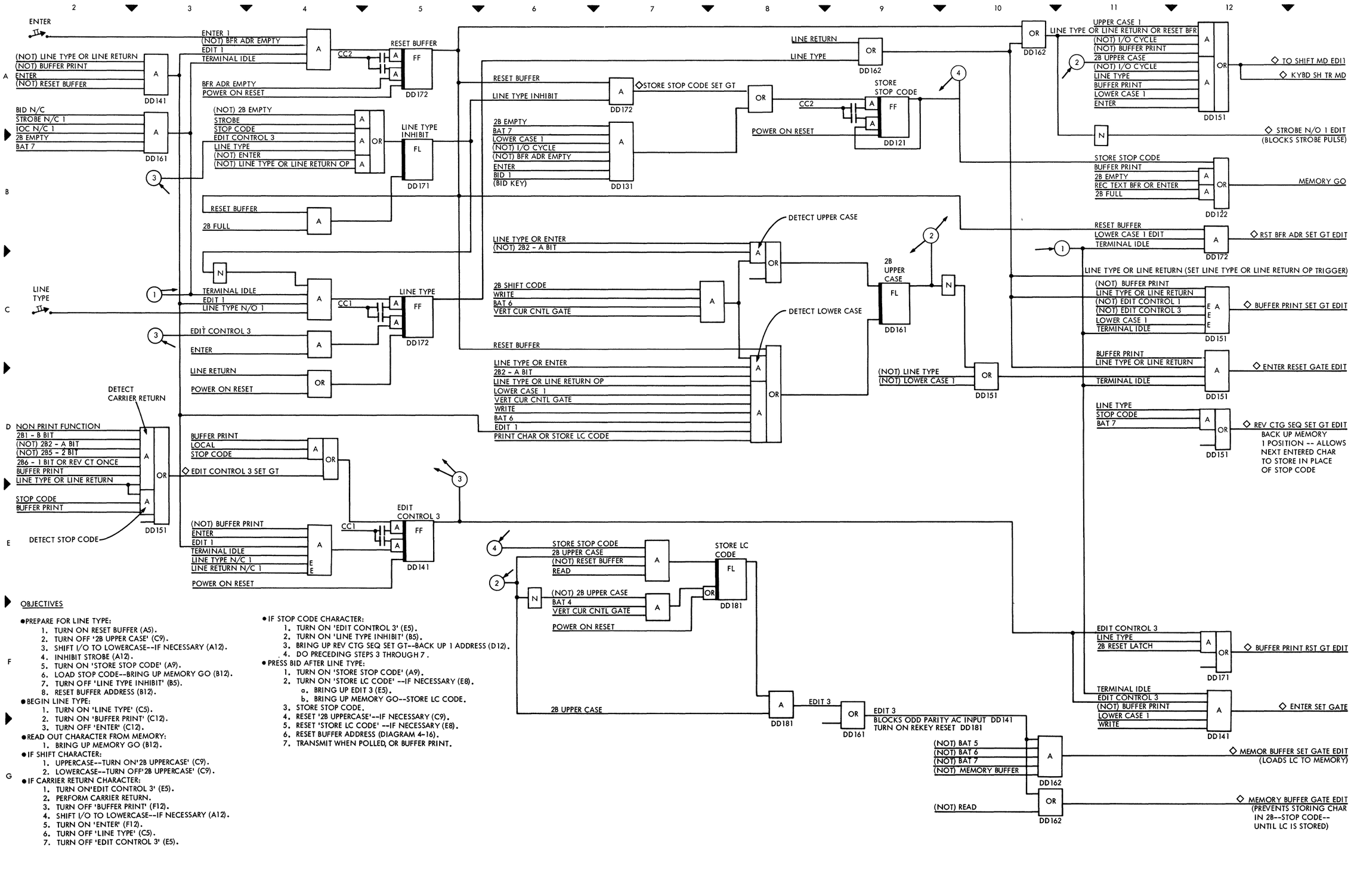


Diagram 5-39. Line Type (2740-2)

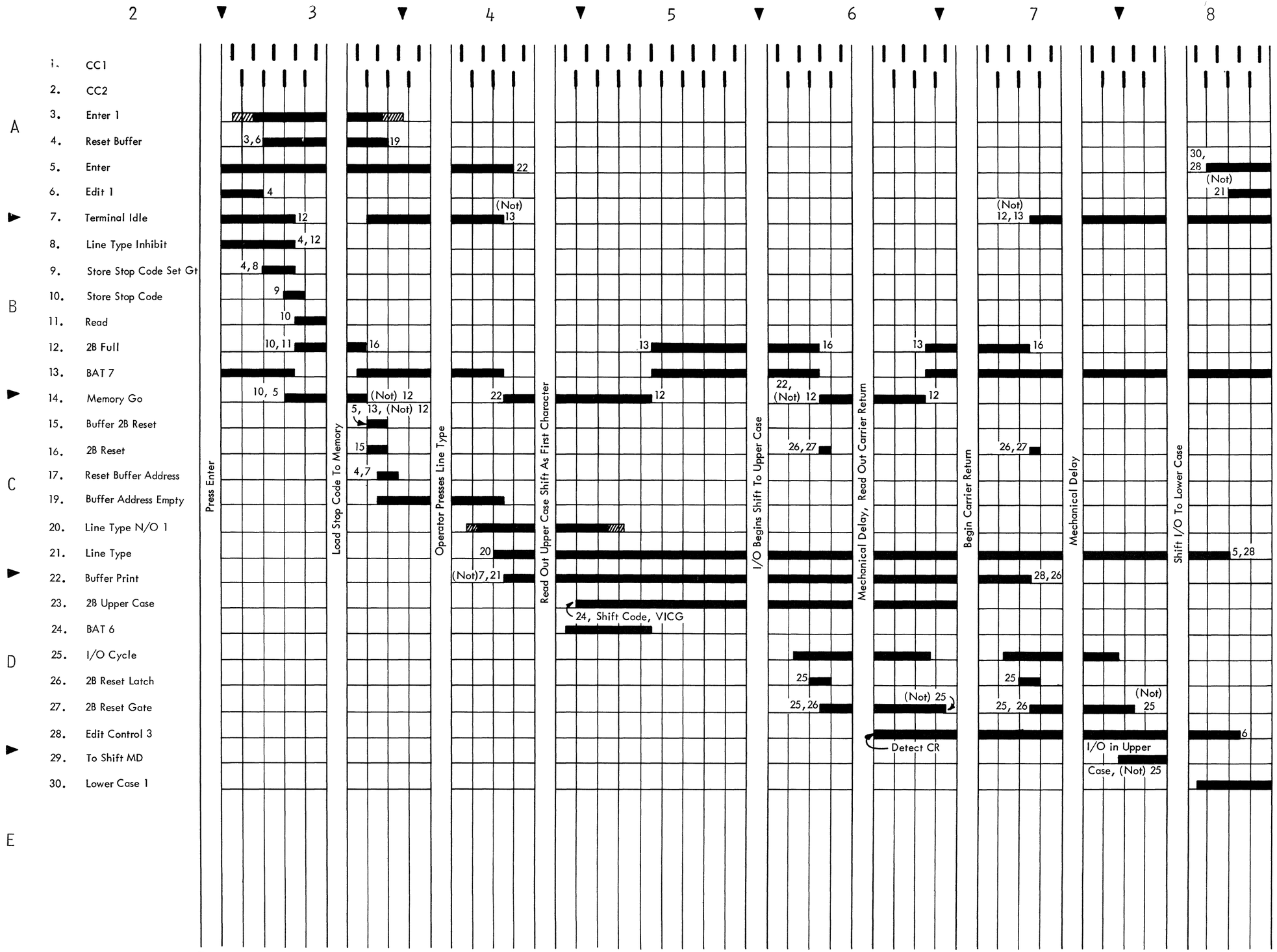
Diagram 5-40. Line Type (2740-2)



OBJECTIVES

- PREPARE FOR LINE TYPE:
  1. TURN ON RESET BUFFER (A5).
  2. TURN OFF '2B UPPER CASE' (C9).
  3. SHIFT I/O TO LOWERCASE--IF NECESSARY (A12).
  4. INHIBIT STROBE (A12).
  5. TURN ON 'STORE STOP CODE' (A9).
  6. LOAD STOP CODE--BRING UP MEMORY GO (B12).
  7. TURN OFF 'LINE TYPE INHIBIT' (B5).
  8. RESET BUFFER ADDRESS (B12).
- BEGIN LINE TYPE:
  1. TURN ON 'LINE TYPE' (C5).
  2. TURN ON 'BUFFER PRINT' (C12).
  3. TURN OFF 'ENTER' (C12).
- READ OUT CHARACTER FROM MEMORY:
  1. BRING UP MEMORY GO (B12).
- IF SHIFT CHARACTER:
  1. UPPERCASE--TURN ON'2B UPPERCASE' (C9).
  2. LOWERCASE--TURN OFF'2B UPPERCASE' (C9).
- IF CARRIER RETURN CHARACTER:
  1. TURN ON'EDIT CONTROL 3' (E5).
  2. PERFORM CARRIER RETURN.
  3. TURN OFF 'BUFFER PRINT' (F12).
  4. SHIFT I/O TO LOWERCASE--IF NECESSARY (A12).
  5. TURN ON 'ENTER' (F12).
  6. TURN OFF 'LINE TYPE' (C5).
  7. TURN OFF 'EDIT CONTROL 3' (E5).

- IF STOP CODE CHARACTER:
  1. TURN ON 'EDIT CONTROL 3' (E5).
  2. TURN ON 'LINE TYPE INHIBIT' (B5).
  3. BRING UP REV CTG SEQ SET GT--BACK UP 1 ADDRESS (D12).
  4. DO PRECEDING STEPS 3 THROUGH 7.
- PRESS BID AFTER LINE TYPE:
  1. TURN ON 'STORE STOP CODE' (A9).
  2. TURN ON 'STORE LC CODE' --IF NECESSARY (E8).
     a. BRING UP EDIT 3 (E5).
     b. BRING UP MEMORY GO--STORE LC CODE.
  3. STORE STOP CODE.
  4. RESET '2B UPPERCASE'--IF NECESSARY (C9).
  5. RESET 'STORE LC CODE' --IF NECESSARY (E8).
  6. RESET BUFFER ADDRESS (DIAGRAM 4-16).
  7. TRANSMIT WHEN POLLED, OR BUFFER PRINT.



Line Type Complete. Operator may now Enter, Line Return or Perform another Line Type.

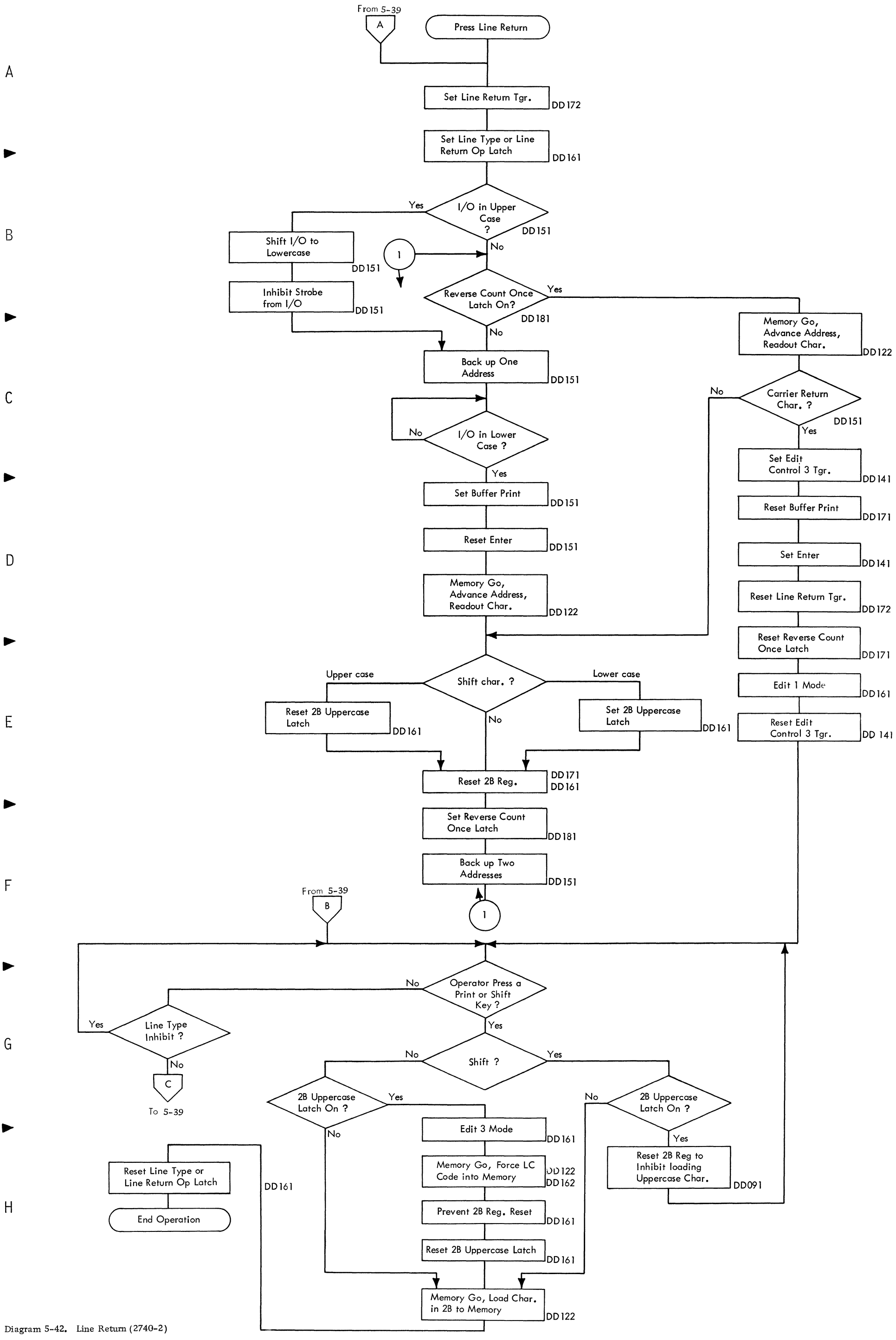
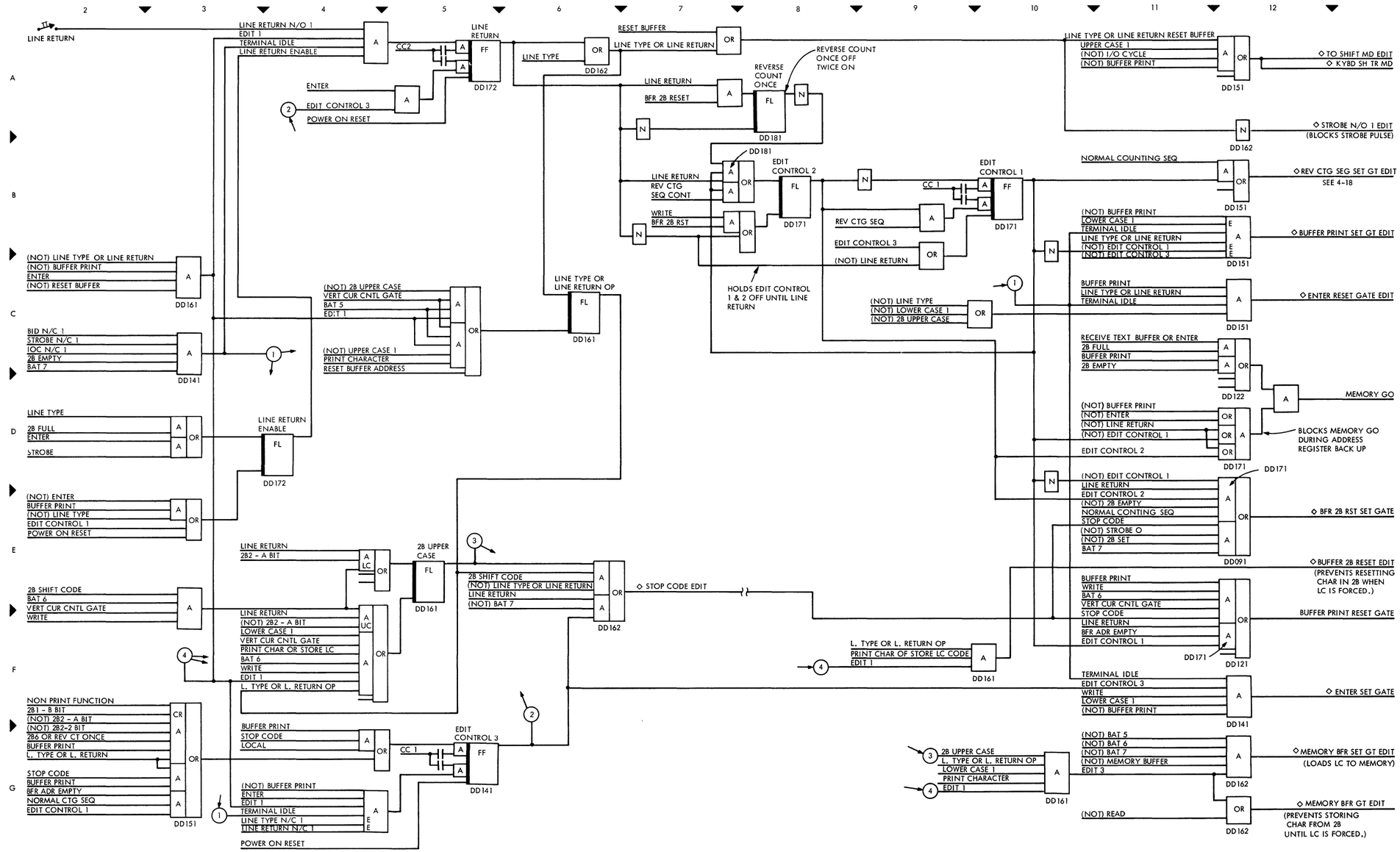


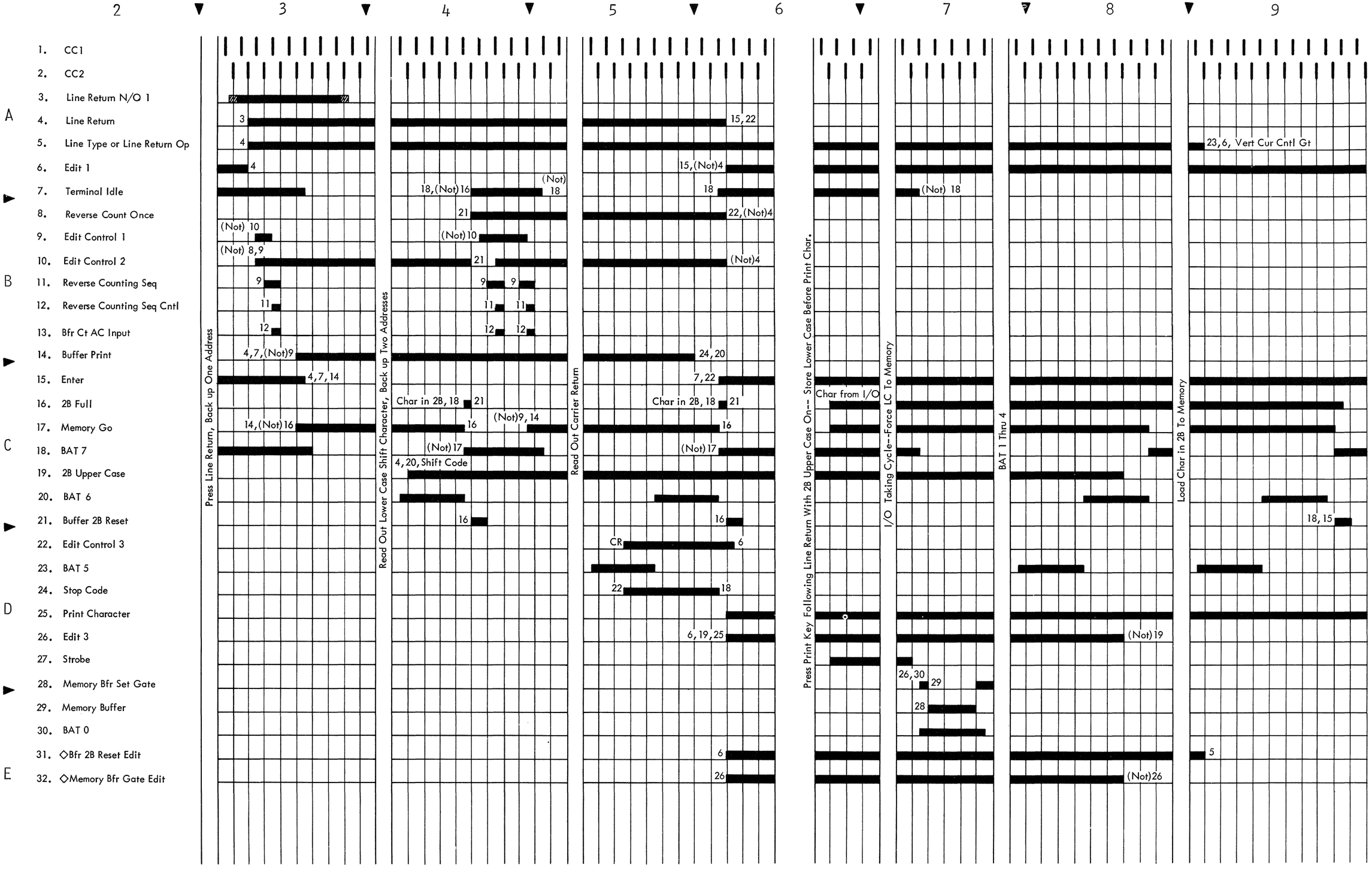
Diagram 5-42. Line Return (2740-2)



OBJECTIVES

- BEGIN LINE RETURN:
  1. TURN ON 'LINE RETURN' (A5).
  2. TURN ON 'LINE TYPE OR LINE RETURN OP' (C6).
  3. SHIFT I/O TO LOWER CASE--IF NECESSARY (A12).
- BACKUP ONE ADDRESS:
  1. TURN ON 'EDIT CONTROL 1' (B10).
  2. BRING UP REV CTG SEQ SET GT (B12).
  3. TURN ON 'EDIT CONTROL 2' (B8).
  4. TURN OFF 'EDIT CONTROL 1' (B10).
- PREPARE TO READOUT CHARACTER FROM MEMORY:
  1. TURN ON 'BUFFER PRINT' (B12).
  2. TURN OFF 'ENTER' (C12).
  3. BRING UP MEMORY GO (C12).
- IF CHARACTER IS:
  1. UPPERCASE--TURN OFF '2B UPPERCASE' (E5).
  2. LOWERCASE--TURN ON '2B UPPERCASE' (E5).
  3. TURN ON 'BUFFER 2B RESET' (E12).
  4. TURN ON 'REVERSE COUNT ONCE' (A8).
- BACKUP TWO ADDRESSES:
  1. TURN OFF 'EDIT CONTROL 2' (B8).
  2. TURN ON 'EDIT CONTROL 1' (B10).
  3. BRING UP REV CTG SEQ SET GT (B12).
  4. TURN ON 'EDIT CONTROL 2' (B8).
  5. TURN OFF 'EDIT CONTROL 1' (B10).
- READ OUT NEXT CHARACTER:
  1. BRING UP MEMORY GO (C12).
- DETFCT CARRIER RETURN CHARACTER:
  1. TURN ON 'EDIT CONTROL 3' (G5).
  2. BRING UP STOP CODE (E6).
  3. TURN OFF 'BUFFER PRINT' (F12).
  4. RESET 2B REG (E12).
  5. TURN ON 'ENTER' (F12).
  6. TURN OFF 'LINE RETURN' (A5).
  7. TURN OFF 'REVERSE COUNT ONCE' (A8).
  8. TURN OFF 'EDIT CONTROL 3' (G5).
- PRESS UPPERCASE KEY WITH '2B UPPERCASE' ON:
  1. BRING UP STOP CODE (E6).
  2. TURN ON 'BUFFER 2B RESET'(E12)--RESETS CHARACTER BEFORE IT CAN BE STORED.
- PRESS PRINT KEY WITH '2B UPPERCASE' ON:
  1. BRING UP EDIT 3 (G10).
  2. BRING UP MEMORY GO (C2).
  3. FORCE LC CHARACTER INTO MEMORY (G12).
  4. PREVENT 2B RESET (E12).
  5. MEMORY GO STAYS UP (C12).
  6. LOAD PRINT CHARACTER.
  7. TURN OFF 'LINE TYPE OR LINE RETURN OP' (C6).

Diagram 5-44. Line Return (2740-2)



2 3 4 5 6 7 8 9

A

Transmit Text

(Not) Header N/O 1

OR

Reset Buffer Address

CC2

Header Storage
Bfr Adr Set

A

A

FF

DD061

Jumper

Buffer Address 6 Set

Buffer Address 7 Set

Buffer Address 8 Set

To Read Set Gate DD091

B

(Not) Bfr Adr 4

(Not) Bfr Adr 5

(Not) Bfr Adr 9

(Not) Bfr Adr 10

(Not) Bfr Adr 11

Header N/O 1

A

Buffer Address Empty

E

E

E

E

Jumper

(Not) Bfr Adr 6

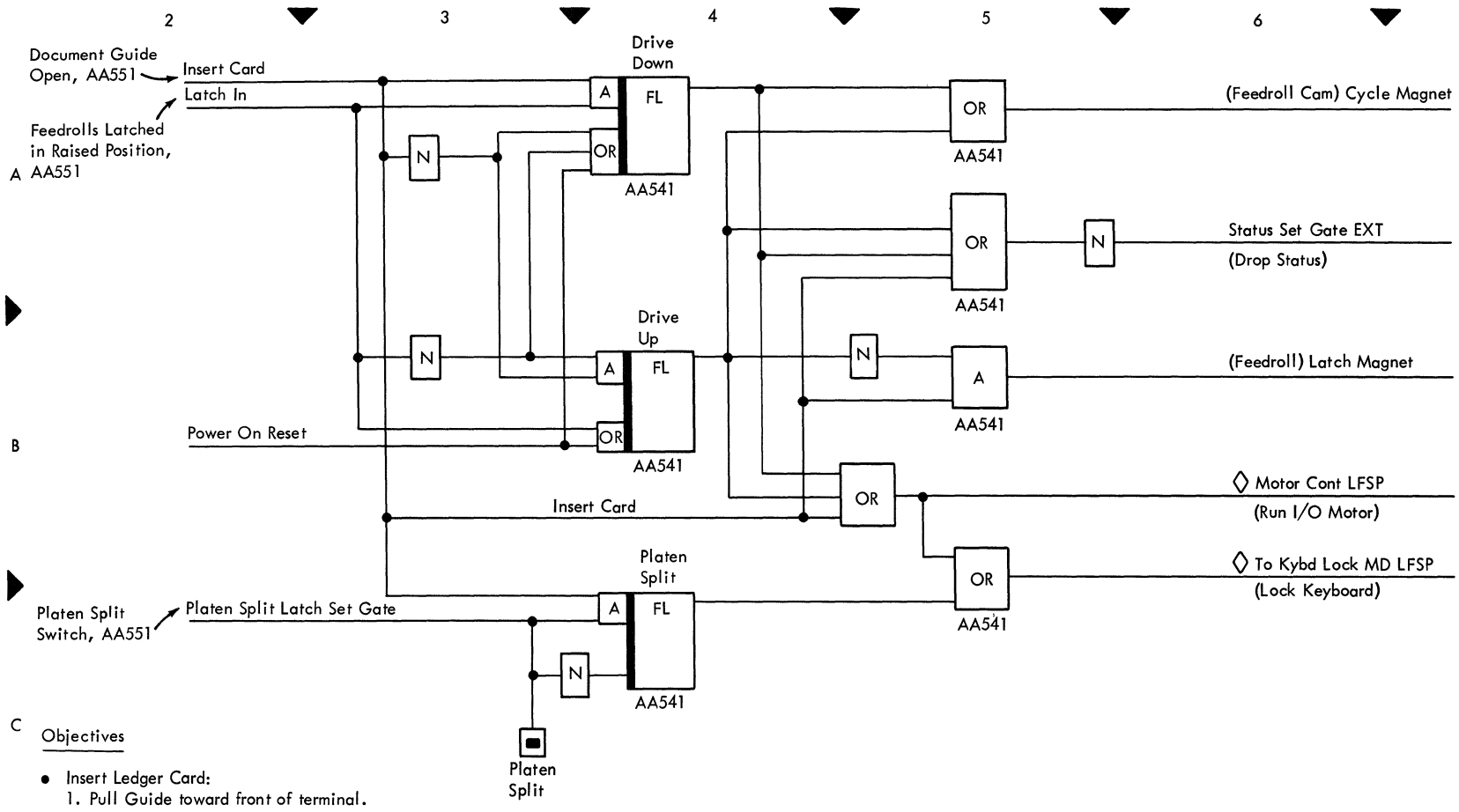
(Not) Bfr Adr 7

(Not) Bfr Adr 8

C

D

E



Objectives

- Insert Ledger Card:
  1. Pull Guide toward front of terminal.
  2. Turn on 'drive down'.
  3. Lower feedrolls.
  4. Drop status, run I/O motor, lock keyboard.
  5. Push Guide toward rear of terminal.
  6. Turn off 'drive down'.
  7. Turn on 'drive up'.
  8. Raise feedrolls.
  9. Turn off 'drive up'.
  10. Bring up status, stop I/O motor (if no other condition to run the motor is present), unlock keyboard.
- Split Platen:
  1. Do steps 1 through 5.
  2. Pull left platen knob.
  3. Turn on 'platen split'.
  4. Lock keyboard.

Diagram 5-46. Document Insertion (2740-2)

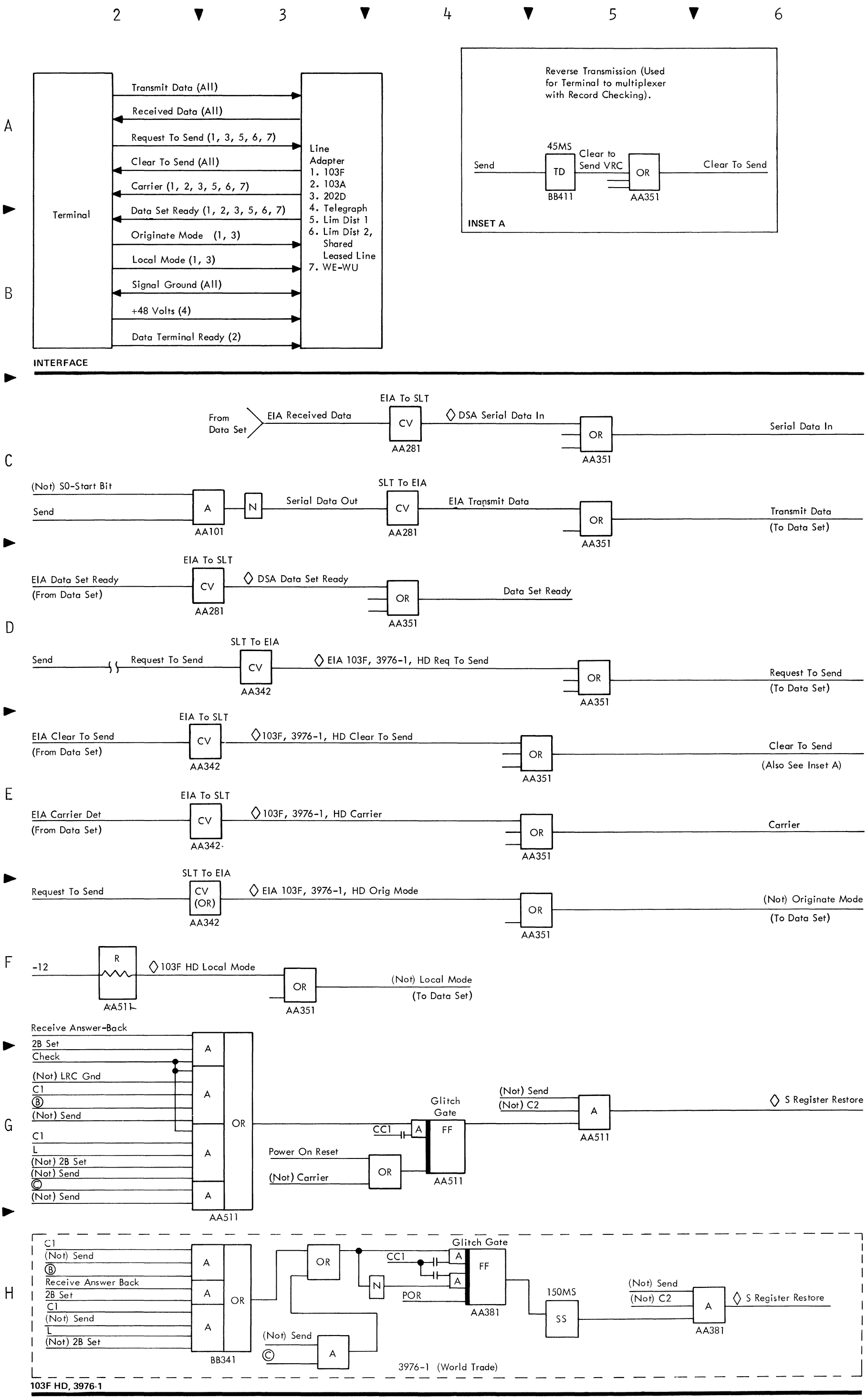


Diagram 5-47. Terminal to Line Adapter Interface (All Terminals), Part 1 of 5

A

EIA Recevied Data
(From Data Set)
EIA To SLT
CV
AA281
◇ DSA Serial Data In
OR
AA351
Serial Data In

(Not) S0-Start Bit
Send
A
AA101
AA501 (2740-2)
N
Serial Data Out
SLT To EIA
CV
AA281
◇ EIA Transmit Data
OR
AA351
Transmit Data
(To Data Set)

B

EIA Data Set Ready
(From Data Set)
EIA To SLT
CV
AA281
◇ DSA Data Set Ready
OR
AA351
Data Set Ready

Request to Send
FD (2740-2)
CA-X
(2740-1)
EOB (2740-1)
Send (2740-2)
OR
Control Add. Mode (2740-2)
TNS or CR (2740-2)
OR
B (2740-1)
FL
Req to Send-X
JMP
Term to Mplx
RC Feature (2740-1); Basic (2740-2)
(Reverse Transmission)
SEND
OR
AA341
SLT to EIA
CV
AA341
◇ Request to Send EIA
OR
AA351
Request to Send
(To Data Set)
Jumper Present for Full Duplex D/S Only.

C

EIA Clear To Send
(From Data Set)
EIA To SLT
CV
AA341
◇ Clear to Send
OR
AA351
Clear To Send
(Also see Inset A on Sheet 1)
Send (2740-2)
45MS
TD
BB411

EIA Carrier Detector
(From Data Set)
EIA To SLT
CV
AA341
◇ Carrier
OR
AA351
Carrier

D

-12
R
AA341
◇ Originate Mode
OR
AA351
(Not) Originate Mode
(To Data Set)

-12
R
AA341
◇ Local Mode
OR
AA351
(Not) Local Mode
(To Data Set)

103F FD, 3976-1, 3977-1 (2740-2 ONLY), WE-WU (2740-2 ONLY)

E

Received Data
EIA To SLT
CV
AA281
DSA Serial Data In
OR
AA351
Serial Data In

(Not) S0-Start Bit
Send
A
AA101
N
Serial Data Out
SLT To EIA
CV
AA281
◇ EIA Transmit Data
OR
AA351
Transmit Data
(To Data Set)

F

EIA Data Set Ready
(From Data Set)
EIA To SLT
CV
AA281
◇ DSA Data Set Ready
OR
AA351
Data Set Ready

330 MS (2741)
45 MS (2740-1)
Send
TD
AA343
◇ 103A Dial Clear To Send
OR
AA351
Clear To Send
(Also see Insert A on Sheet 1)

Note:
Request to Send is not used for 103A.

G

EIA Clear To Send
(From Data Set)
EIA To SLT
CV
AA343
◇ 103A Dial Carrier
OR
AA351
Carrier

H

Dial Disc. Key
Dial Disc N/O
(Not) Clock Run
A
Dial Disc
FL
AA301
(Not) Data Set Ready
Power On Reset
OR
N
(Not) Dial Disc
Status
A
AA343
N
Data Terminal Not Ready
(3976-2--2740-1 Only)
SLT to EIA
CV
103A Dial Data Term Ready *
(To Data Set)
*Data Terminal Ready is Held up for 2741.

103A (2740-1/2741 ONLY), 3976-2 (2740-1 ONLY)

Diagram 5-47. Terminal to Line Adapter Interface (All Terminals), Part 2 of 5

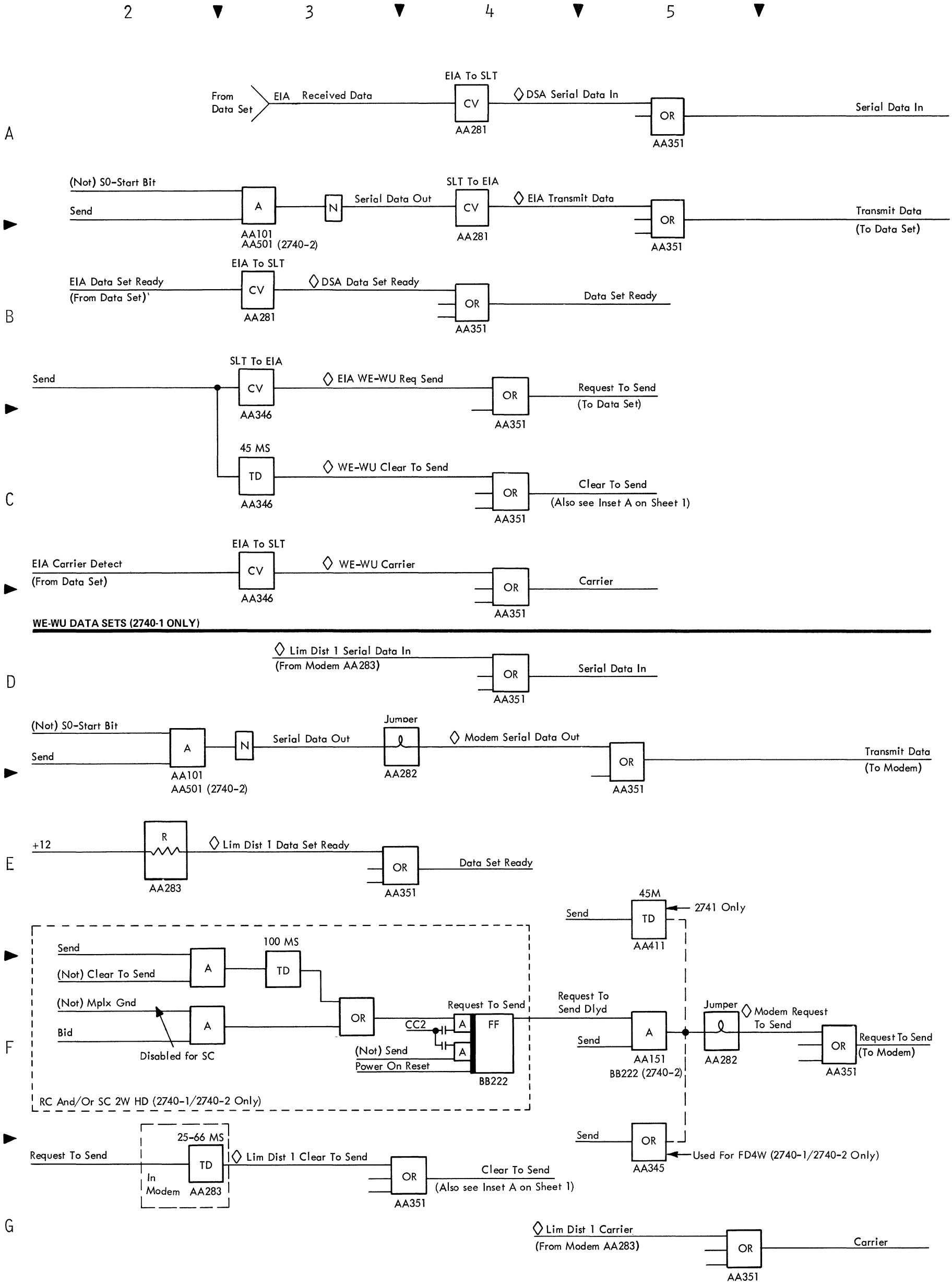


Diagram 5-47. Terminal to Line Adapter Interface (All Terminals), Part 3 of 5

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

A

LD Type 2 Received Data
Leased Line 4W Received Data
Leased Line 2W Received Data
Shared Line 4W Received Data
Shared Line 2W Received Data
(From Modems)
OR
CC061
Received Data
N
AA282
◇ Modem Serial Data In
OR
AA351
Serial Data In

(Not) S0-Start Bit
Send
A
AA101
AA501 (2740-2)
N
Serial Data Out
Jumper
AA282
◇ Modem Serial Data Out
OR
AA351
Transmit Data
(To Modem)

▶

(Power On Reset)
CC061
4 Sec
TD
AA282
◇ Modem Data Set Ready
OR
AA351
Data Set Ready

B

Send
(Not) Clear To Send
100 MS
TD
A
(Not) Mplx Gnd Disabled For SC
Bid
A
OR
CC2
A
A
FF
BB222
Request To Send
(Not) Send
Power On Reset

Send
45MS
TD
AA411
2741 Only
Request To Send Dlyd
Send
A
AA151
BB222 (2740-2)
Request To Send
Jumper
AA282
◇ Modem Req To Send
OR
AA351
Request To Send
(To Modem)

C

RC And/Or SC (2740-1/2740-2 Only)

2740-1 Only (Without RC or SC)

▶

D

Request To Send
See Note
TD
◇ Modem Clear To Send
Jumper
AA282
◇ Modem DSA Clear To Send
OR
AA351
Clear To Send
(Also see Inset A on Sheet 1)

(Not) S1-B Bit
(Not) Send
Glitch Protection
A
FL
CC022
OR
◇ Modem Carrier

▶

(Not) Enter Serdes

◇ Mod Carrier or Lim Dist TP6

A
AA351
Carrier

E

LD Type 2 Carrier
LL 4W Carrier
LL 2W Carrier
SL 4W Carrier
SL 2W Carrier
OR
CC061
Enter Serdes
OR
AA282
◇ Modem DSA Carrier

Note:
LD Type 2 12.5 MS CC011
LL 4W 20 MS CC021
LL 2W 146-252 MS CC031
SL 4W 20 MS CC041
SL 2W 146-252 MS CC051

▶

F

LIMITED DISTANCE TYPE 2, LEASED LINE, SHARED LINE MODEMS (2 AND 4 WIRE)

▶

G

▶

H

Diagram 5-47. Terminal to Line Adapter Interface (All Terminals), Part 4 of 5

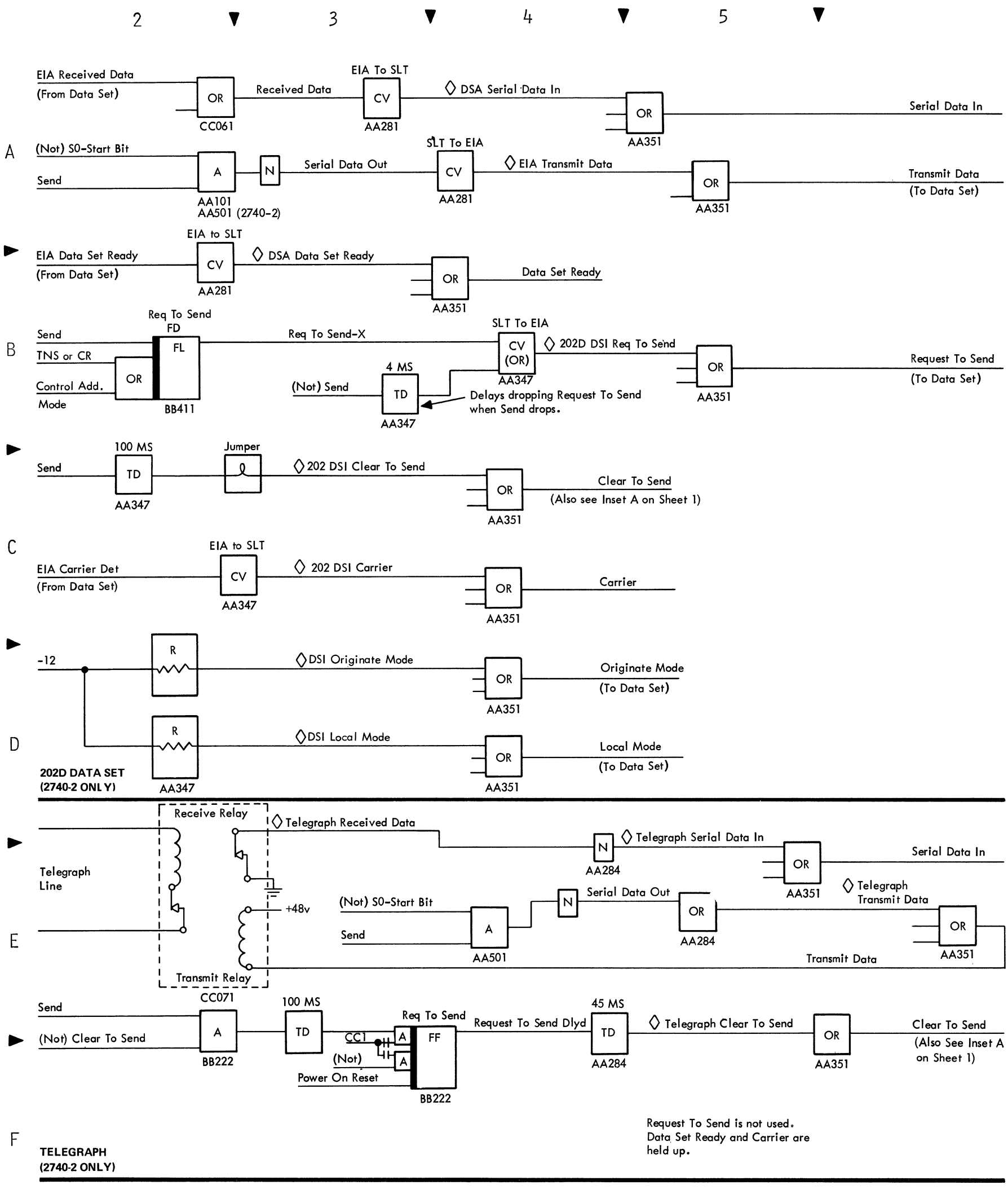


Diagram 5-47. Terminal to Line Adapter Interface (All Terminals), Part 5 of 5

2760 MDM	2760 ALD	Line Name from 2760	Entry	Line Name to 2740	Interface	Line Name in 2740	2740 ALD	2740 MDM
3-5	AA041	Bid N/O	Paddle-card Cable Connector	Bid N/O OIU Bid N/O	OR	* Bid -1	AA163	5-3
3-9	AA161	EOT N/O		EOT N/O OIU EOT N/O	OR	EOT-1	AA163	5-3
3-7	AA161	EOB N/O		EOB N/O OIU EOB N/O	OR	EOB-1	BB051	5-14
3-2	AA162	Error		Error OIU	CV	◇ Error Set Gate OIU	BB021	2-1
3-6	AA022	Gate Out Strobe		Gate Out Strobe OIU	CV	Strobe O Set Gate OIU	AA101	4-9 and
						Strobe N/C OIU	AA161	5-3
3-2	AA022	Inhibit Print		Inhibit Print OIU	CV	◇ (Not) Print Out OIU	AA091	4-8 and
					A	◇ Motor Contactor OIU	AA151	4-10
3-2	AA022	Keyboard Lock		Keyboard Lock OIU	CV	◇ Keyboard Lock OIU	AA014	4-10
3-9	AA161	Restart		Restart OIU Restart N/O Key	OR	* Restart	BB321	5-15
3-11	AA062	Status Inhibit		Status Inhibit OIU	CV	◇ Paper OIU	AA165	4-11 and
					CV	◇ (Not) Paper 2 OIU	AA261	5-1
3-7	AA012	1B Reg 1-B Bit		1B Reg 1-B Bit OIU	CV	◇ 1B Reg 1-B Bit OIU	AA181	5-3
3-7	AA012	1B Reg 2-A Bit		1B Reg 2-A Bit OIU	CV	◇ 1B Reg 2-A Bit OIU	AA181	5-3
3-7	AA012	1B Reg 3-8 Bit		1B Reg 3-8 Bit OIU	CV	◇ 1B Reg 3-8 Bit OIU	AA184	5-3
3-7	AA012	1B Reg 4-4 Bit		1B Reg 4-4 Bit OIU	CV	◇ 1B Reg 4-4 Bit OIU	AA181	5-3
3-7	AA012	1B Reg 5-2 Bit		1B Reg 5-2 Bit OIU	CV	◇ 1B Reg 5-2 Bit OIU	AA183	5-3
3-7	AA012	1B Reg 6-1 Bit		1B Reg 6-1 Bit OIU	CV	◇ 1B Reg 6-1 Bit OIU	AA183	5-3
3-7	AA012	1B Reg 7-C Bit		1B Reg 7-C Bit OIU	CV	◇ 1B Reg 7-C Bit OIU	AA182	5-3
3-2	AA022	2B Reset	AA731	2B Reset OIU	CV	◇ 2B Reset OIU	AA121	5-6

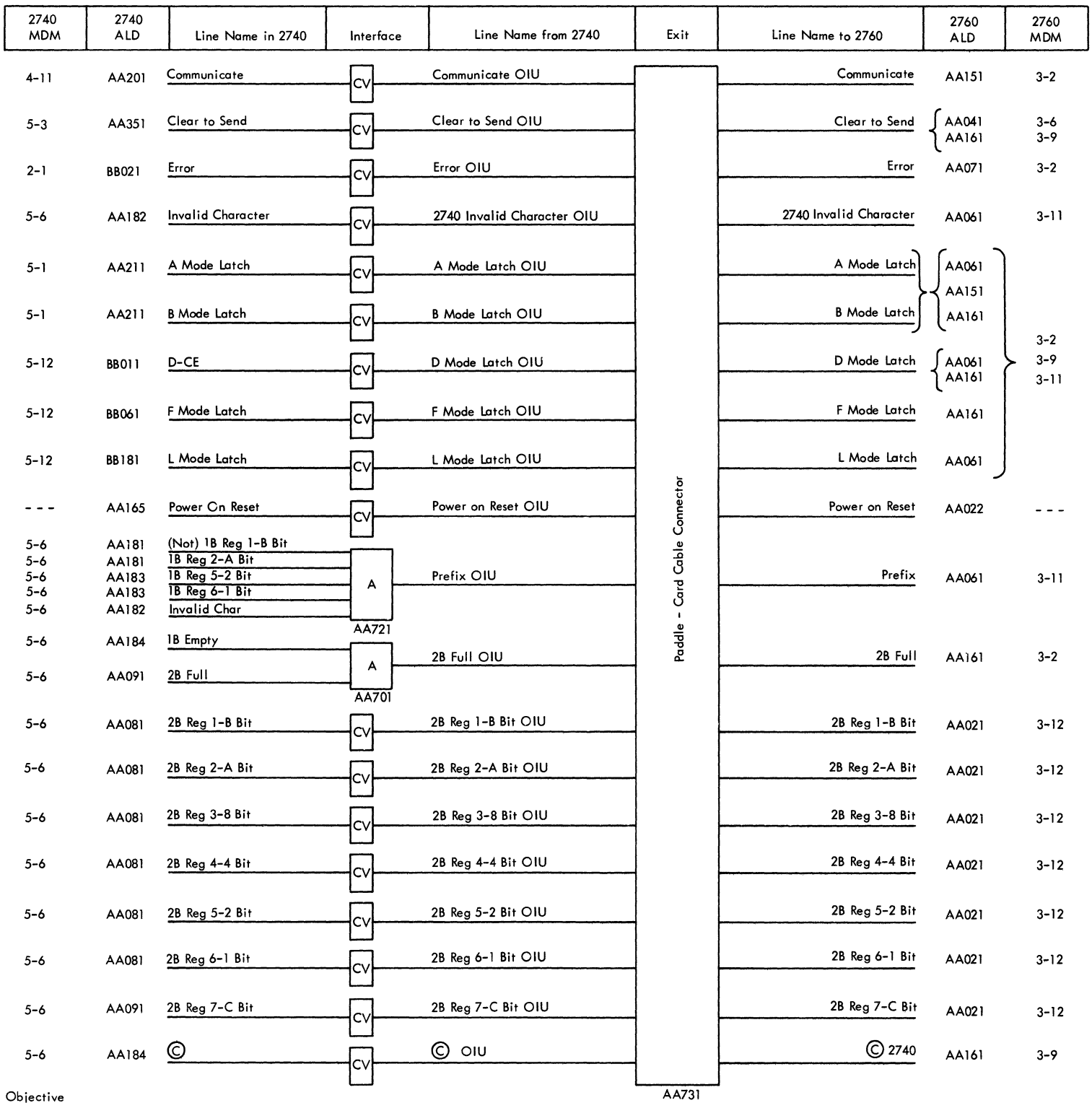
Objective

- Transmit message from 2760 via 2740-1.

1. Probe operation at the 2760 starts the 2760 oscillator, sets OIU 'send' latch and brings up 'bid N/O OIU' from 2760.
2. 'Clear to send' ANDed with 2760 'send' brings up 'on line' which allows position counter advance and 'gate out' to take place.
3. The 2760 position counter advances to generate the initial PRE, O sequence followed by gate out of Image Index Counter and V- and H-registers to the 2760 output bus.
4. 'Gate output bus' ANDed with the output bus lines in the 2760 brings up the 1B-reg bit lines from the 2760 each time the position counter advances.
5. For each character time 'gate out' comes up in the 2760 to bring up 'gate out strobe OIU' which sets the 'strobe O' latch and the 'strobe' latch in sequence.
6. The bits are gated into the 1B-register by 'strobe'.
7. A basic 2740-1 cycle transmits the character via the S-register.
8. 'Position 8' count and 'gate output bus' in the 2760 bring up 'EOB N/O OIU' to initiate a basic 2740 EOB/LRC sequence.
9. 'Restart OIU' from 2760 initiates 'restart' at the 2740 if an error is detected at EOB/LRC time.
10. 'Receive answerback,' 'not F,' 'not D,' and 'not B' in the 2760 bring up 'send EOT to 2740. ' 'EOT N/O OIU' from 2760 sets 'EOT Trigger' which brings up '1B generate' to send EOT.

NOTE: While the 2760 is transmitting, 'Keyboard lock OIU' from the 2760 locks the I/O printer keyboard.

Diagram 5-48. Interface, Part 1 of 2 (2760 to 2740)



Objective

- Receive Ⓓ , PRE, o, F, A_1 , A_2 , EOB, LRC by 2760 with status .

1. Ⓓ received to activate terminal.
2. PRE (A8421) decoded in 1B-register.
3. 1B-reg A, 2, 1 bits and (not) B bit ANDed with 'invalid character' brings up 'prefix' line to 2760.
4. "o" (B42) received in S-reg and sent to 2B-register via 1B-register.
5. The 2760 decodes "o" on the 2B-register lines from the 2740-1. (All 2B-register bits are sent to 2760.)
6. The 2760 sends 'inhibit print OIU' to the 2740 to turn off I/O motor and inhibit printout.
7. 2B-register is reset by '2B reset OIU' from the 2760.
8. The text message F, A_1 , A_2 is received via S-reg, 1B-reg, 2B-reg, and 2B-reg lines to 2760.
9. The message is ended by EOB/LRC sequence.
10. LRC checking is initiated. If there is an error in the message, 'error set gate OIU' from the 2760 sets 'error' trigger in the 2740 which generates a negative answerback. (The 'error' trigger is also set when errors are detected by the 2740-1.)

- Message to 2760 without Status

1. Ⓓ , PRE, o selects 2760
2. Status inhibit' in 2760 becomes 'status inhibit OIU' in the 2740-1 to bring up 'paper OIU' and '(not) paper 2 OIU' at the 'status' latch.
3. Status' latch is reset to drop status
4. Terminal is reset to A B mode.

- Message to 2740-1

If either the PRE or the "o" character is missing from the message, the 2740 is enabled and the message is directed to the I/O printer.

Diagram 5-48. Interface, Part 2 of 2 (2740 to 2760)

READER'S COMMENT FORM

IBM 2740-1/2740-2/2741 Communications Terminals FEMDM

SY27-0014-3

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  As a reference source ☐
  As a classroom text ☐
  As a self-study text ☐

- Based on your own experience, rate this publication . . .

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As a text:	Very Good	Good	Fair	Poor	Very Poor

- What is your occupation?

- We would appreciate your other comments; please give specific page and line references where appropriate. If you wish a reply, be sure to include your name and address.

- Thank you for your cooperation. No postage necessary if mailed in the U. S. A.

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As a text:	Very Good	Good	Fair	Poor	Very Poor

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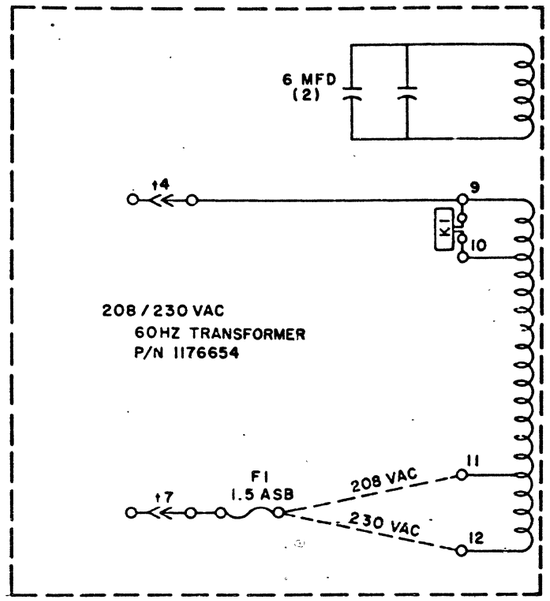
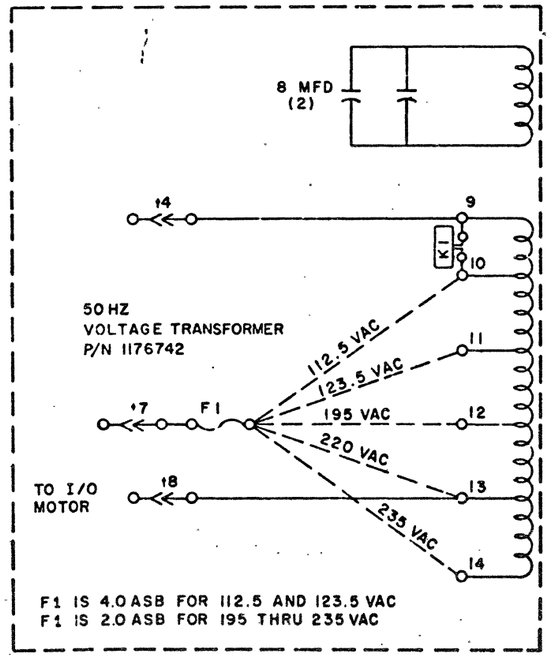
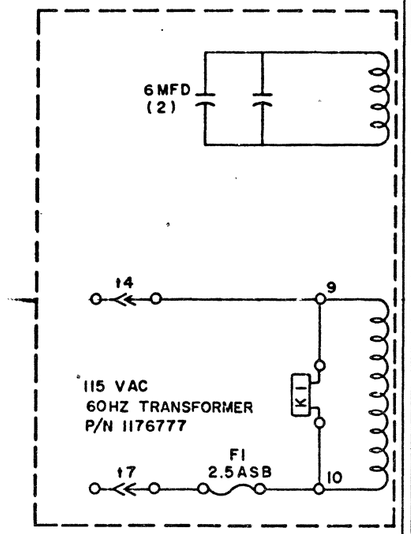


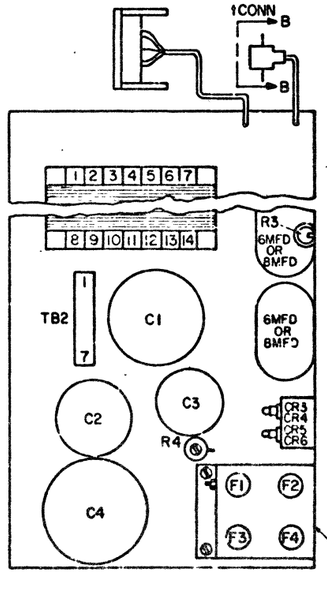
DETAIL A

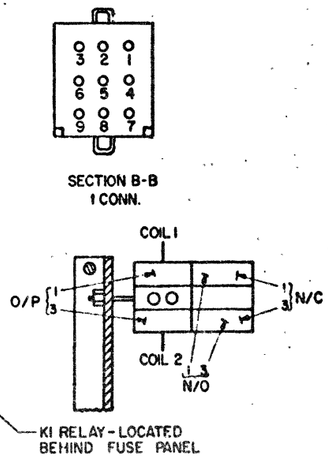


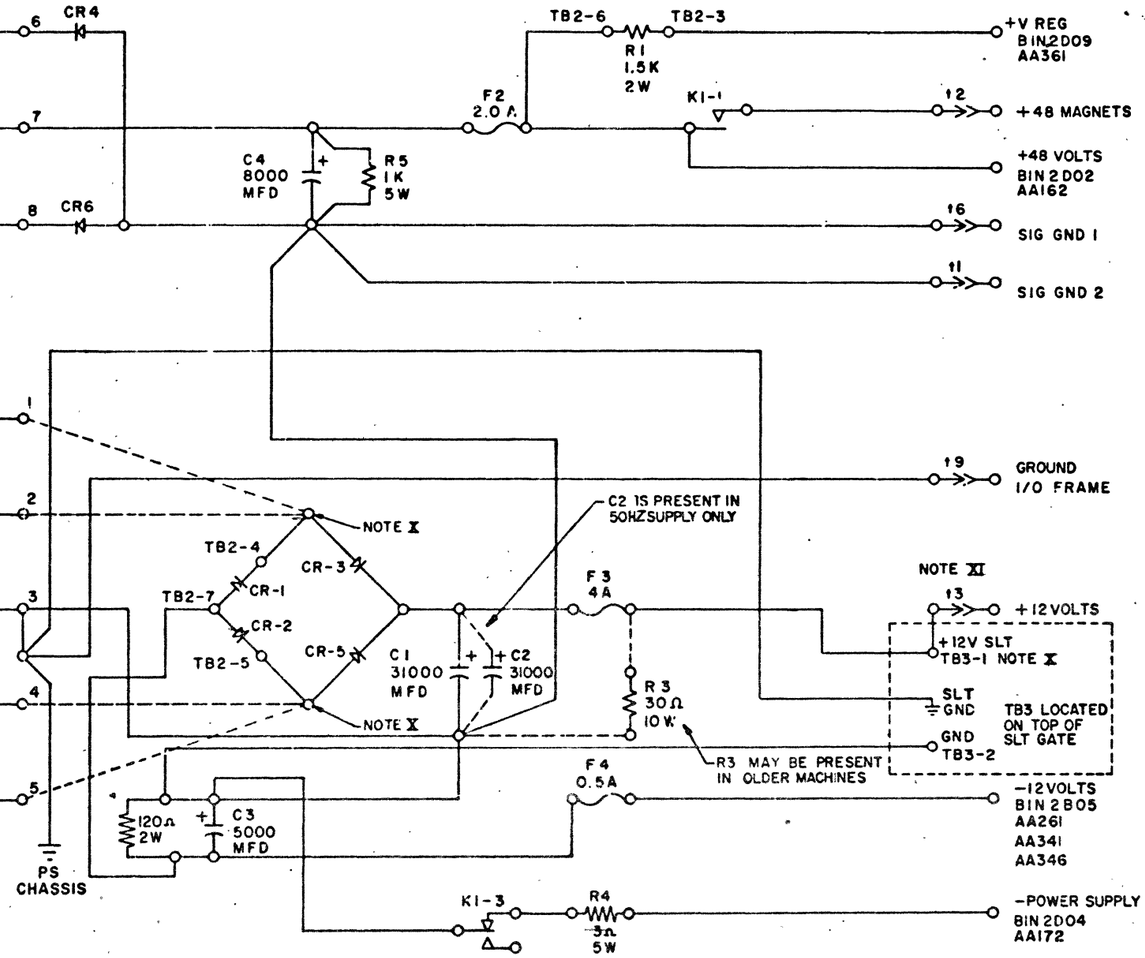
DETAIL B

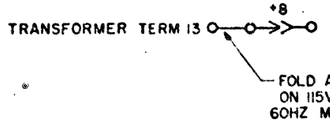


SEE DETAIL A FOR 208/230V 60HZ
SEE DETAIL B FOR WORLD TRADE
NOTE: DO NOT WIRE 115 VAC 60HZ INTO P/N 1176654 OR 208/230 VAC 60HZ INTO P/N 1176777









NOTE

X IF THE +12V SLT SUPPLY IS BELOW 11.7 VDC, CHANGE THE TRANSFORMER TAPS ON THE SECONDARY WINDING FROM POSITIONS 2 AND 4 TO POSITIONS 1 AND 5 IF NOT DONE ALREADY

XI +12V GOES TO 13 BUT IS NOT USED IN THE MACHINE

DATE	E.C. NO.	DATE	E.C. NO.	POWER SUPPLY—SCHEMATIC	
16 DEC 65	506021	MAY 67	306754		
4 AUG 66	506352	AUG 67	306762	PART NO. 1176191	PAGE NO. 2000
16 AUG 66	506826	APR 68	307100	IBM 2741	
24 FEB 67	507567				

INPUTS TO PRINTER		
SIGNAL NAME	ALD PAGE	SIGNAL PIN
SIG GND 1	——	T6
-T2 MD	AA013	NIB09
-CHECK MD	AA012	NIB08
-TI MD	AA013	NIDI0
-R2A MD	AA013	NIBI0
-RI MD	AA012	NIBI2
-R2 MD	AA013	NIDII
-R5 MD	AA012	NID09
+48	——	t2
-RIB SHIFT MAG	AA651	NIDI2
-SH LA KNOCK OFF MD	AA014	MIBI2
-KEYBOARD LOCK MD	AA014	NID07
-INDEX MD	AA011	MID02
-CR MD	AA011	MIB03
-BK SP MD	AA014	MIB04
-TAB MD	AA011	MID04
-NON PRINT MD	AA011	NIB02
-NON PRINT HOLD MD	AA691	NIB05
-SHIFT MD	AA012	NIB03
SIG GND 2	——	t1
GND (VIA MID08)	AA361	MIDI2
+12	CC061	A5805
-MODEM TEST LIGHT	CC061	A5802

OUTPUTS FROM PRINTER		
SIGNAL PIN	ALD PAGE	SIGNAL NAME
NIDI3	AA431	+C6 N-O
NIDO5	AA161	-CR OR TAB INTLK
MIBI0	AA163	+IOC N-C
MIDI0	AA163	-IOC N-O
NID02	AA163	+STROBE N-C
MIDII	AA163	-STROBE N-O
MIB09	AA162	-PRINTER OUT 1-B BIT
MID09	AA162	-PRINTER OUT 2-A BIT
MIB08	AA161	-PRINTER OUT 3-B BIT
MID07	AA162	-PRINTER OUT 4-4 BIT
MIB07	AA161	-PRINTER OUT 5-2 BIT
MID06	AA161	-PRINTER OUT 6-1 BIT
MIB05	AA162	-PRINTER OUT 7-C BIT
MID05	AA421	+TYPAMATIC N-O
NIBI3	AA671	+INH TRANSMIT INTR
NID06	AAI71	+ATTN N-C
NIB07	AAI71	-ATTN N-O
NID04	AAI71	-LCC
NIB04	AAI71	-UCC
MIDI3	AAI72	+COMM N-O
MIBI3	AAI72	-COMM N-C
A5804	CC021 CC031 CC041 CC051	+MOD TEST

CB6 · CR INLK · TAB INLK · BK SP TAB CB5 · LC SHIFT CB4 · UC SHIFT CB3 · CB2 · CB1 · CB7 SHIFT

LC SHIFT · UC SHIFT

T2 · CK · TI · R2A · RI · R2 · R5

TYPAMATIC UNDERSCORE · TYPAMATIC BACKSPACE OR SPACE · NOTE XIV

IND · CR · BS · TAB

ATTN · COMM · MOUNTED ON STAND · LCL

+48 V · REL · SLK · KL · IND · CR · BS · TAB · NP · LC · UC · NOTE XI · NOTE X · NOTE XII · NOTE XIII

INNER · OUTER · SHIFT MODE (SHOWN IN LC)

OFF · TEST · MOD · MODEM TEST LIGHT · LIGHT AND SWITCH MOUNTED ON STAND · TO POWER SUPPLY PRIMARY

OPERATIONAL CONTACT ASSEMBLY

TAB · BS · CR · IND

DETAIL A

115,208,230 VAC-60HZ OR 112.5,123.5,195,220,235 VAC-50HZ

WHT · BLK · GRN · BN [FOR 50 HERTZ VOLTAGES ONLY] · BLACK · YELLOW · WHITE · (REMOVE JUMPER FOR 50 HERTZ VOLTAGES) · FRAME GND · MOTOR GND

NOTES

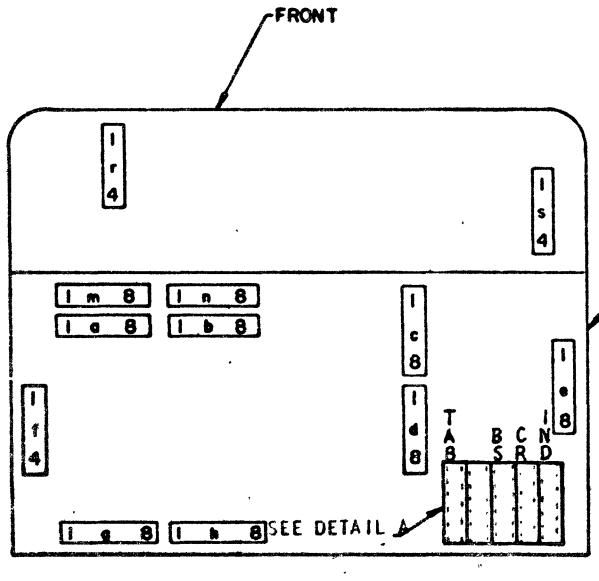
X THIS WIRE REMOVED ON MACHINES WITH RED RIBBON CONTROL FEATURE

XI [- - -] WIRING INSTALLED FOR RED RIBBON CONTROL FEATURE

XII [▬▬] WIRING INSTALLED FOR PRINT INHIBIT FEATURE

XIII MOVE THIS WIRE FROM S4 TO S3 ON MACHINES WITH PRINT INHIBIT FEATURE

XIV THIS WIRING MAY BE PRESENT ON SOME MACHINES WITH THE TRANSMIT INTERRUPT FEATURE INSTALLED



BOTTOM SKETCH OF PRINTER SHOWING LOCATION OF TERMINAL BLOCKS

DATE	E.C. NO.	DATE	E.C. NO.	TYPEWRITER
16AUG66	506823	JUN 68	345323	WIRING SCHEMATIC
19NOV66	545071	DEC 68	346052	PART NO. 1277307 | PAGE NO. 3000
27DEC66	507476	MAR70	308734	IBM 2741 VER 002
JUN 67	345317			

BOARD 01A-B1
CARD SIDE

	1	2	3	4	5	6	7
N	I/O CABLE	POWER SUPPLY CABLE		MODEM XOVER		← RPQ →	
M	I/O CABLE			DATA SET CABLE *SEE NOTES		← RPQ →	
L	5803567 AA161 INTEGRATORS	5803569 AA014 MAGNET DRIVER-4	5803566 AA171 INTEGRATORS	** SEE NOTES		5803744 AA371 CHECK LOOP	
K	5803567 AA162 INTEGRATORS	5803569 AA013 MAGNET DRIVER-3	5803852 AA172 INTEGRATORS	*** SEE NOTES			
J	5803569 AA011 MAGNET DRIVER-1	5803565 AA163 INTEGRATORS	5803569 AA012 MAGNET DRIVER-2	AA411 5804515 AUTO EOT AND ILC LATCH		AA141 5807365 OR 5804377 I/O CYCLE & OPERATE LATCHES	
H	5800889 AA431 CARRIER RETURN LATCH	5804439 AA061 - SERDES CLOCK AA071 - CONTROL CLOCK		AA021 5804440 AA031 OR 5807362 S REGISTER			
G		AA131 5804374 OR 5807364 S REG EMPTY, ES GATE & BID LATCHES		AA221 5804375 S REGISTER RESET LOGIC		AA361 5804381 CLOCKS 539Hz & 18KHZ	
F	5803849 AA401 INTERRUPT	AA121 5804373 2B SET & RESET LATCHES		AA241 5804441 AA251 PRINTER OUTPUT DECODES		5803570 AA052 SERDES CLOCK	5803086 AA051 CONTROL CLOCK
E	CE AID CABLE	AA101 5804372 OR 5807361 STROBE 0, ENTER SERDES & EOT LATCHES		5804371 AA201 - INTERRUPT, LOCAL & STROBE LATCHES AA211 - A B & MODE CHANGE LATCHES		5804368 AA181 - 1B REG (1, 2, 4) AA182 - 1B REG (7) & INVALID CHAR	
D	CE AID CABLE	AA081 AA091 5804370 2B REGISTER		5807374 AA183 - 1B REG (5 & 6) AA184 - 1B REG (3) & ⓒ ⓓ DECODES		AA231 5804376 KEYBOARD LOCK, 1B & 2B REGISTER LOGIC LINES	
C	5803846 AA671 TRANSMIT INTERRUPT	AA391 5801324 LINE CONTROL		AA421 5806005 TYPAMATIC			
B		AA651 5807372 PREFIX & RIBBON SHIFT		AA601 5807370 AUTO ADDRESS ANSWER BACK-1		5800287 AA691 PRINT INHIBIT	5800299 AA691 PRINT INHIBIT
A				AA611 5807371 AUTO ADDRESS ANSWER BACK-2			

NOTES

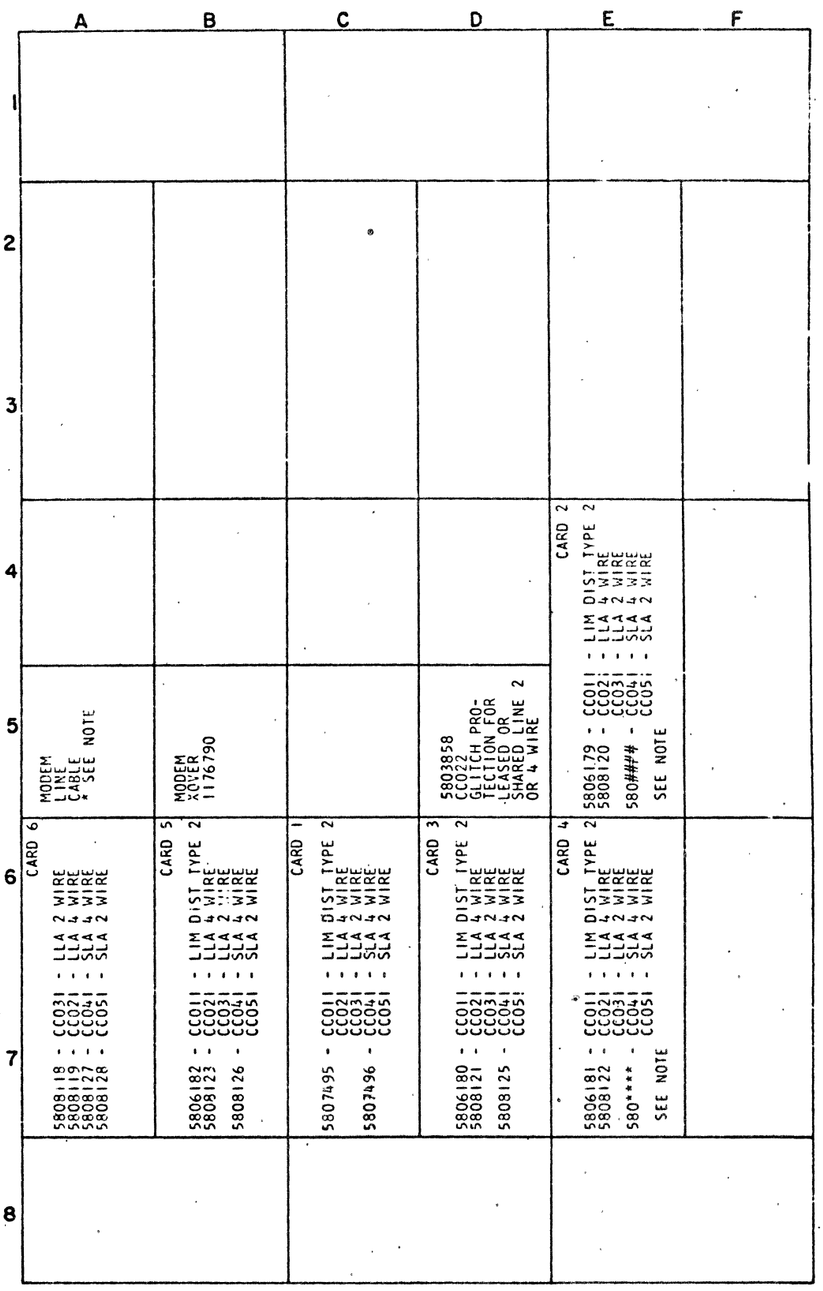
* POSITION M4 - CABLE P/N 1176745 FOR 103A,113A,103F, 150 BAUD OR WU CLASS D
CABLE P/N 1176471 FOR LIM DIST TYPE 1 (2 OR 4 WIRE)

** POSITION L4 - CARD P/N 5803561 - AA281 - DATA SET ADAPTER
CARD P/N 5803850 - AA283 - LIMITED DISTANCE 1 ADAPTER 2W-HD OR 4W-FD
CARD P/N 5803854 - AA282 - MODEM DATA SET ADAPTER EXCEPT LIMITED DISTANCE TYPE 1

*** POSITION K4 - CARD P/N 5801278 - AA346 - WE-WU DATA SET ADAPTER
CARD P/N 5801315 - AA341 - 103F OR 3976 MOD 1 FULL DUPLEX DATA SET ADAPTER
CARD P/N 5803855 - AA343 - 103A DIAL ADAPTER (NOT TWIN CARD)
CARD P/N 5806001 - AA344 - LIM DIST TYPE 1 2W ADAPTER
CARD P/N 5806002 - AA345 - LIM DIST TYPE 1 4W ADAPTER

DATE	E. C. NO.	DATE	E. C. NO.	BOARD DIAGRAM 01A-B1	
JUN70	308747			PART NO. 5994673	PAGE NO. 4001
				IBM 2741	VER 002

BOARD 01A-C1
CARD SIDE



NOTES

* POSITION A5 - CABLE P/N 1176648 - LIM DIST TYPE 2
CABLE P/N 1176647 - LEASED LINE 2 & 4 WIRE
CABLE P/N 1186279 - SHARED LINE 2 & 4 WIRE

580**** POSITION E6 - CARD P/N 5808133 - SUB CHANNEL 4 - 2 OR 4 WIRE SLA
CARD P/N 5808134 - SUB CHANNEL 3 - 2 OR 4 WIRE SLA
CARD P/N 5808135 - SUB CHANNEL 2 - 2 OR 4 WIRE SLA
CARD P/N 5808136 - SUB CHANNEL 1 - 2 OR 4 WIRE SLA

LLA - LEASED LINE ADAPTER
SLA - SHARED LINE ADAPTER

580#### POSITION E4 - CARD P/N 5808129 - SUB CHANNEL 1 - 2 OR 4 WIRE SLA
CARD P/N 5808130 - SUB CHANNEL 2 - 2 OR 4 WIRE SLA
CARD P/N 5808131 - SUB CHANNEL 3 - 2 OR 4 WIRE SLA
CARD P/N 5808132 - SUB CHANNEL 4 - 2 OR 4 WIRE SLA

REFER TO INSTALLATION INSTRUCTIONS FOR CARD JUMPER PLUGGING

P.N. 5162302

DATE	E. C. NO.	DATE	E. C. NO.	BOARD DIAGRAM
APR68	307100			01A-C1
				PART NO. 5162302 / PAGE NO. 4002
				IBM 2741

BASE MACHINE							
5804440 OR 5807362-B1H4 5804372 OR 5807361-B1E2 5804374 OR 5807364-B1G2 5804377 OR 5807365-B1J6	5803852-B1K3 5803565-B1J2 5803086-B1F7 5801324-B1C2	5803566-B1L3 5803567-B1K1 5803567-B1L1 5803569-B1J1	5803569-B1J3 5803569-B1K2 5803569-B1L2 5803570-B1F6	5803744-B1L7 5804368-B1E6 5804439-B1H2 5804370-B1D2	5804371-B1E4 5804515-B1J4 5804373-B1F2 5804441-B1F4	5804375-B1G4 5804376-B1D6 5803889-B1H1 5804381-B1G6	5804369 OR 5807374-B1D4 SEE NOTES * * *

- LIMITED DIST. TYPE 1 2W — 5803850-B1L4, 5806001-B1K4
- LIMITED DIST. TYPE 2 — 5803854-B1L4, 5807495-C1C6, 5806179-C1E4, 5806180-C1D6, 5806181-C1E6, 5806182-C1B6
- LEASED LINE 2W — 5803854-B1L4, 5808118-C1A6, 5808120-C1E4, 5808121-C1D6, 5808122-C1E6, 5807495-C1C6, 5808123-C1B6, 5803858-C1D5
- SHARED LINES — 5803854-B1L4, 5803958-C1D5, 5808126-C1B6, 5807496-C1C6, 5808125-C1D6
  - SUB CHANNEL 1 — 5808129-C1E4, 5808136-C1E6
  - SUB CHANNEL 2 — 5808130-C1E4, 5808135-C1E6
  - SUB CHANNEL 3 — 5808131-C1E4, 5808134-C1E6
  - SUB CHANNEL 4 — 5808132-C1E4, 5808133-C1E6
  - 2 WIRE — 5808128-C1A6
  - 4 WIRE — 5808127-C1A6
- 150 BAUD SCHEDULE 3A — 5803561-B1L4, 5801278-B1K4
- LIMITED DIST. TYPE 1 4W — 5803850-B1L4, 5806002-B1K4
- LEASED LINE 4W — 5803854-B1L4, 5808119-C1A6, 5808120-C1E4, 5808121-C1D6, 5808122-C1E6, 5807495-C1C6, 5808123-C1B6, 5803858-C1D5
- 103F OR 3976-1 — 5803561-B1L4, 5801315-B1K4
- 113A OR 103A — 5803561-B1L4
  - DIAL UP — 5803855-B1K4
- WU CLASS D — 5803561-B1L4, 5801278-B1K4
- RECEIVE INTERRUPT — 5803849-B1F1
- * ** TRANSMIT INTERRUPT — 5803846-B1C1
- * RIBBON CONTROL OR AUTO ADDRESS ANSWER BACK — 5807372-B1B2
  - * AUTO ADDRESS ANSWER BACK — 5807370-B1B4, 5807371-B1A4
- * PRINT INHIBIT — 5800287-B1B6, 5800299-B1B7
- TYPAMATIC — 5806005-B1C4

NOTE:

* INDICATES SPECIAL FEATURES ADDED BY THIS VERSION.

* * ONE BACK PANEL DIODE IS ALSO REQUIRED FOR THIS FEATURE

* * * A ONE MICROFARAD CAPACITOR IS MOUNTED ON THE PIN SIDE OF THE 01A-B1 SLT BOARD BETWEEN PINS B1UB05 (POS) AND B1UD08 (NEG)

DATE	E.C. NO.
JUN 70	309747

IBM 2741 VER 002

PART NO. 5994674 PAGE NO. 5000

FEATURE LISTING AND CARD LOCATION

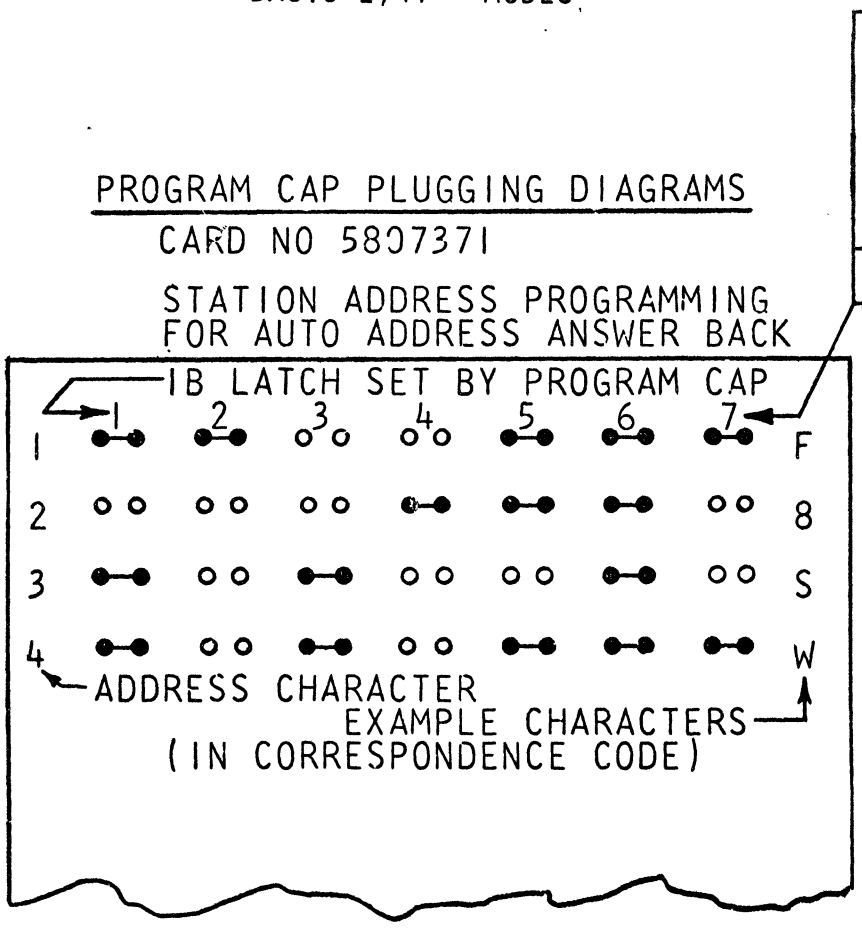
MODES	TRIGGERS ON	
CONTROL RECEIVE	A	B
TRANSMIT TEXT	A	
RECEIVE TEXT		B
RECEIVE CONTROL		

BASIC 2741 MODES

PROGRAM CAP PLUGGING DIAGRAMS

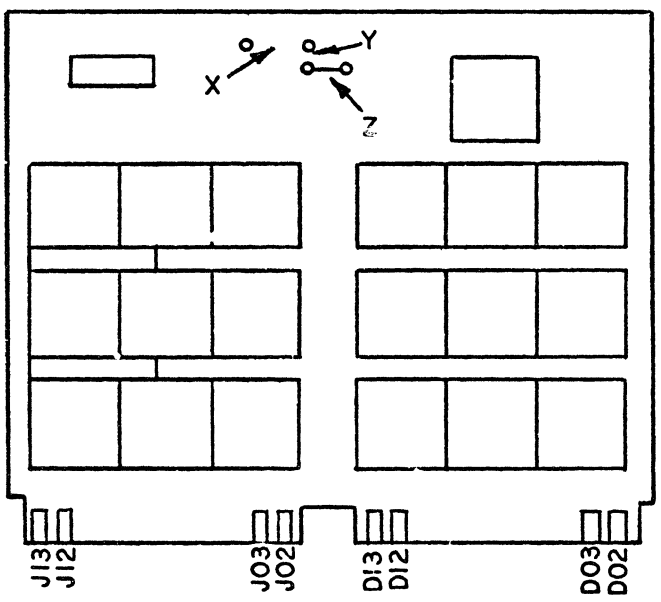
CARD NO 5807371

STATION ADDRESS PROGRAMMING
FOR AUTO ADDRESS ANSWER BACK



IN THIS EXAMPLE THE ADDRESS IS F8SW

CARD NO 5804515



	FOR	PLUG
*	DIAL	X JUMPER
	HALF DUPLEX	Y JUMPER
**	FULL DUPLEX	Z JUMPER

← SHOWN PLUGGED AS AN EXAMPLE

* DIAL (X JUMPER) ALSO HAS TO HAVE FULL DUPLEX (Z JUMPER)
** FOR WU CLASS D OR 150 BAUD SCHEDULE 3A, INSERT Z JUMPER FOR ALL INSTALLATIONS

CODE CHART

6 BIT CODE
(WITH ODD PARITY CHECK BIT "▼")

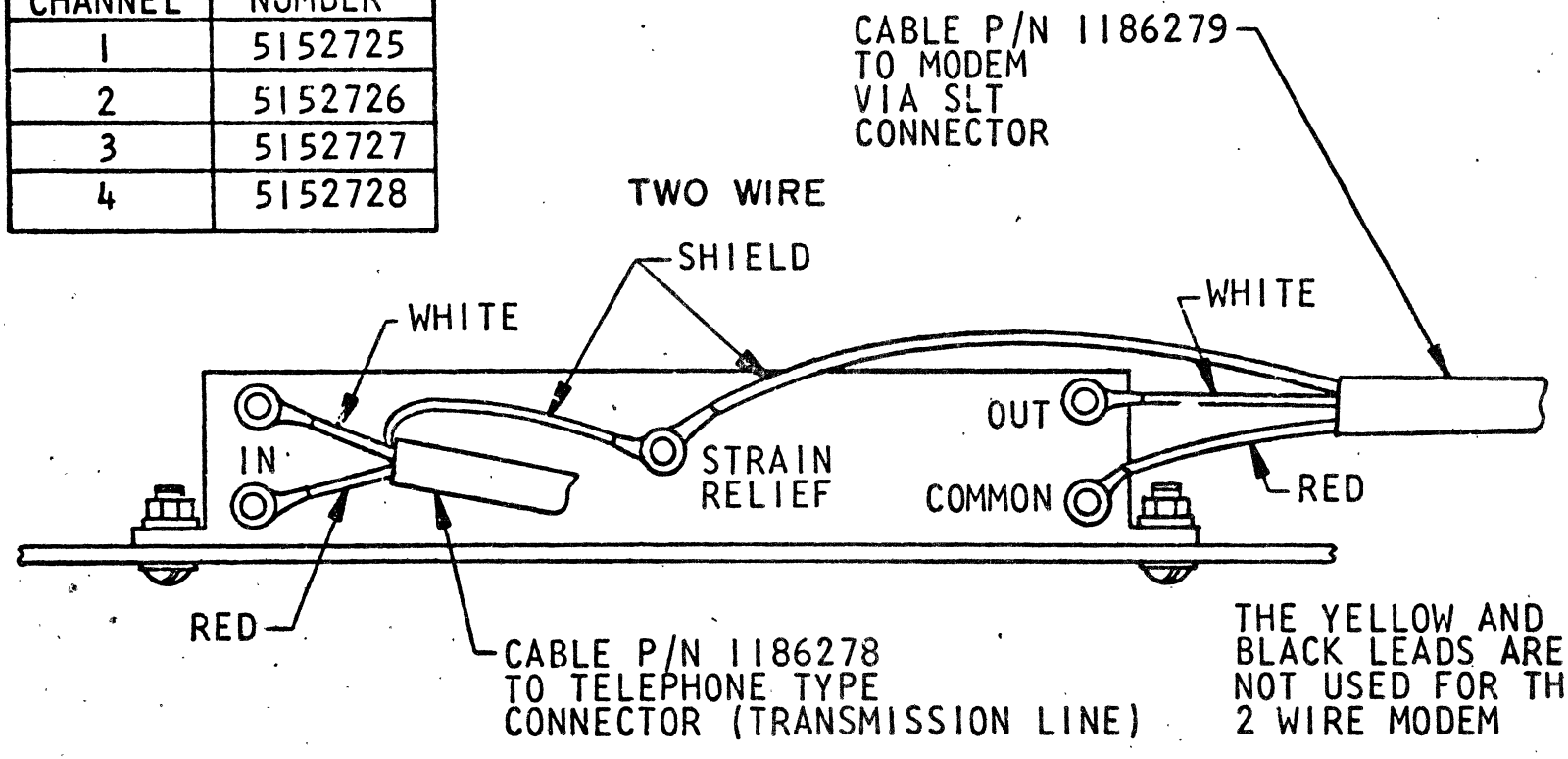
LINE CODE BIT ORDER-ALSO REPRESENTS REGISTER POSITIONS

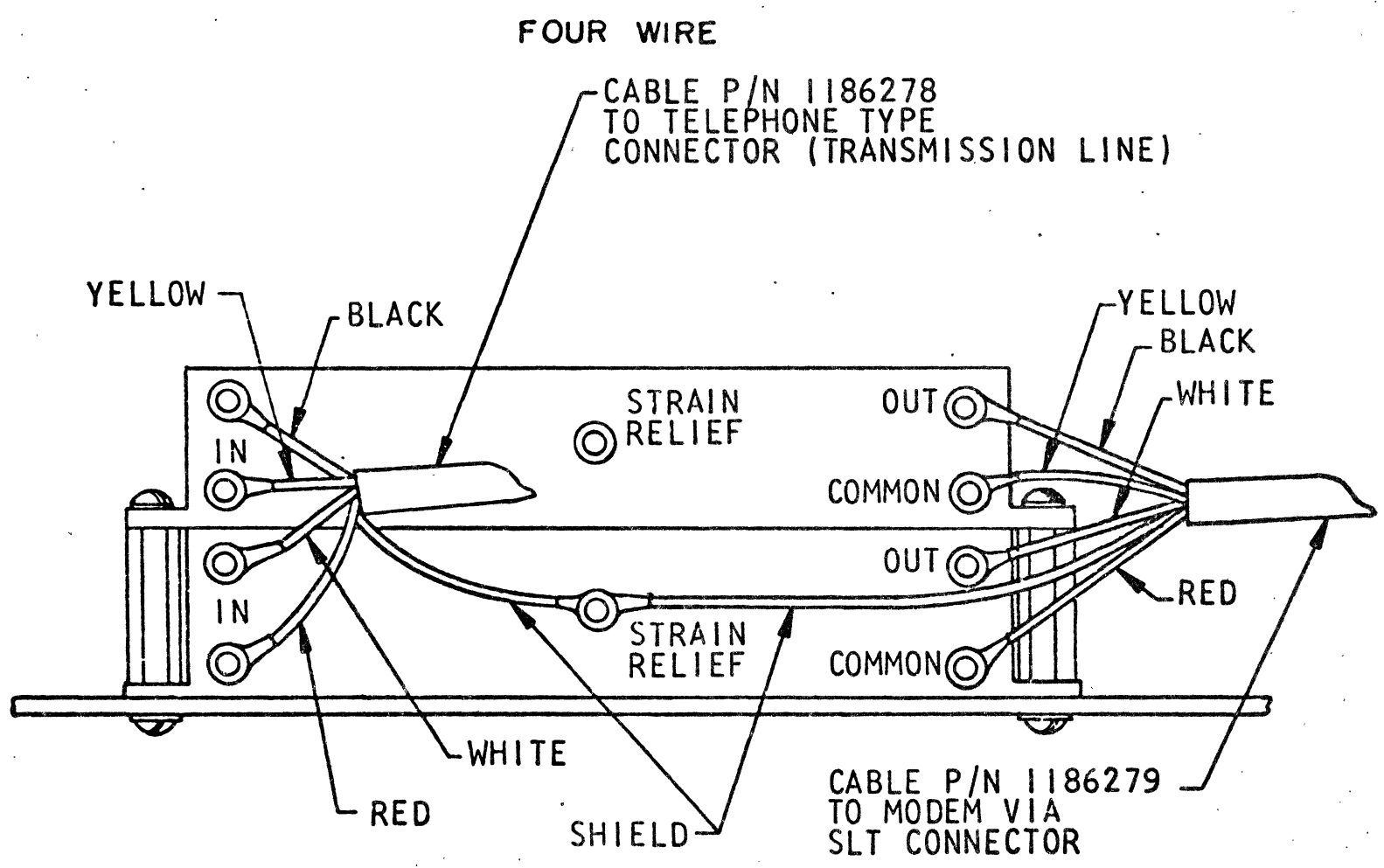
3456	CORRESPONDENCE 12 00	CORRESPONDENCE 12 01	CORRESPONDENCE 12 10	CORRESPONDENCE 12 11	BCD 12 00	BCD 12 01	BCD 12 10	BCD 12 11
0000	SP / SP	T / t	° / !	J / j	SP / SP	¢ / @	– / –	+ / &
0001	[± / ¦]	X / x	M / m	G / g	▼ / ¦	? / /	J / j	A / a
0010	/ 2	N / n	• / •	+ / =	° / 2	S / s	K / k	B / b
0011	# / 3	U / u	V / v	F / f	; / 3	T / t	L / l	C / c
0100	% / 5	E / e	" / '	P / p	: / 4	U / u	M / m	D / d
0101	& / 7	D / d	R / r	: / ;	% / 5	V / v	N / n	E / e
0110	¢ / 6	K / k	I / i	Q / q	¦ / 6	W / w	O / o	F / f
0111	* / 8	C / c	A / a	, / '	" / 7	X / x	P / p	G / g
1000	$ / 4	L / l	O / o	? / /	* / 8	Y / y	Q / q	H / h
1001	) / 0	H / h	S / s	Y / y	(/ 9	Z / z	R / r	I / i
1010	Z / z				) / 0			
1011	(/ 9	B / b	W / w	— / –	± / #	, / ,	! / $	• / •
1100		BY-PASS	RE-STORE			BY-PASS	RE-STORE	
1101		LF INDEX (LS)	CR	TAB		LF INDEX (LS)	CR	TAB
1110	UC SHIFT		BK SPACE	LC SHIFT	UC SHIFT		BK SPACE	LC SHIFT
1111	EOT	PRE-FIX			EOT	PRE-FIX		

DATE	E C NO.	DATE	E C NO.	PROGRAM CAP, CODE AND
16DEC65	506021	JUN68	345323	MODE CHARTS - VERSION 002
19NOV66	545071	NOV 68	346052	PART NO. 1277311 PAGE NO. 7000
27DEC66	507476	MAR70	308734	IBM 2741
JUN67	345317			

SHARED LINES FILTERS

SUB CHANNEL	PART NUMBER
1	5152725
2	5152726
3	5152727
4	5152728





THESE FILTERS ARE MOUNTED AT THE BACK OF THE STAND BENEATH THE READING BOARD

REFER TO PAGE AA352
NOTE THAT WIRE COLORS DO NOT CORRESPOND TO THE TELEPHONE TYPE CONNECTOR TERMINAL DESIGNATIONS

DATE	E.C. NO.	DATE	E.C. NO.	SHARED LINES FILTER	
1 DEC 66	507247			CONNECTIONS	
APR 68	307100			PART NO. 1186498	PAGE NO. 8000
				IBM 2741	

MFI DESCRIPTIONS

SYMBOL	DESCRIPTION
BA	BASIC MACHINE
CE	CE AID BOX CARDS
DSFM	103F DATA SET
D/S	DATA SET 103A, 103F, WU CLASS D AND 150 BAUD SCHEDULE 3A, 3976-1
INT	RECEIVE INTERRUPT
LDI4	LIM DIST TYPE 1 - 4 WIRE
LDTI	LIM DIST TYPE 1 - 2 AND 4 WIRE
MLI	ALL MODEMS EXCEPT LIM DIST TYPE 1,2 AND 4 WIRES
TYP	TYPAMATIC
WEWU	150 BAUD SCHEDULE 3A OR WU CLASS D DATA SET
103A	103A DATA SET
TI	TRANSMIT INTERRUPT
PRI	PRINT INHIBIT CPU CONTROL
RRS	RED RIBBON SHIFT
AAAB	AUTO ADDRESS ANSWERBACK

DATE	E.C. NO.	DATE	E.C. NO.	MFI DESCRIPTION	
MAR70	308734				
				PART NO. 5162729	PAGE NO. 9000
				IBM 2741	

SIGNAL NAME	NET NO.
+XA	AA411AF4
+A MODE LATCH	AA211AN2
-A MODE LATCH	AA211AN6
-XA LITE	CE021AU4
-A RESET GATE	AA411BE4
-A SET GATE	AA411BB4
+ATTENTION 1	AA171AE2
-ATTENTION 2	AA171AH2
+AUTO EOT	AA411BH2
-AUTO EOT	AA411BH6
-AUTO EOT EXT	AA391AC7
-AUTO EOT SET GATE	AA391AC4
+XB	AA391AM4
+B MODE LATCH	AA211AU2
-B MODE LATCH	AA211AU6
-B SET GATE	AA411AT4
+BID LATCH	AA131BD2
-BID LATCH	AA131BD6
-XB LITE	CE011AL4
-BK SP MD	AA014AA2
-B RESET GATE	AA391AL4
+B RESET GATE EXT	AA391AL7
+CARRIER	AA351AL4
+◇CARRIER	AA411AU3
+◇LIM DIST 1 CARRIER	AA283AC3
+◇MODEM CARRIER	CC022AL4
+◇MODEM DSA CARRIER	AA282AB4
+◇WE-WU CARRIER	AA346AG2
+◇103A DIAL CARRIER	AA343AH2
+◇103F FD CARRIER	AA341AC2
-◇CARRIER	CE041AE4
-◇MODEM CARRIER	CC061AA4
-CHECK MD	AA012AB2
+CIRCLE C	AA184AJ4
-CIRCLE C	AA184AE4
+CIRCLE D	AA184AK4
-CIRCLE D	AA184AF4
+CLEAR TO SEND	AA351AM4
+◇CLEAR TO SEND	AA411AU2
+◇LIM DIST 1 CLEAR TO SEND	AA283AH4
+◇MODEM CLEAR TO SEND	CC061AC4
+◇MODEM DSA CLEAR TO SEND	AA292AG4
+◇WE-WU CLEAR TO SEND	AA346AJ2
+◇103A DIAL CLEAR TO SEND	AA343AG4
+◇103F FD CLEAR TO SEND	AA341AA2
+CLOCK MULTIVIBRATOR	AA361AB4
-CLOCK MULTIVIBRATOR	AA361AC4
+CLOCK RUN	AA131BQ4
+◇CLOCK RUN	CE021AA4
-CLOCK RUN	AA131AL4
+COMMUNICATE	AA201AN6
-COMM N-O 1	AA172AC2
-COMM N-C 1	AA172AE2
-CR MD	AA011AQ2
-CYCLE	CE031AX6
-CYCLE INTERLOCK	CE011AK4
+CYCLE N-O 1	CE031AD2
-CYCLE N-C 1	CE031AT2

SIGNAL NAME	NET NO.
+C1	AA071BA4
+XC1	AA071AK2
-C1	AA071AY4
-C1 GATE	AA231AZ4
+C2	AA071BC4
-C2	AA071AQ4
-CC1	AA051AA2
-CC1 GATE	AA182AS4
-◇CC1 GATE	CE021AB4
-CC2	AA051AR2
-CC2 GATE	AA391AN4
+DATA SET READY	AA351AD4
+◇DSA DATA SET READY	AA281AC2
+◇LIM DIST 1 DATA SET READY	AA283AJ4
+◇MODEM DATA SET READY	AA282AE4
+103A DIAL DATA TERM READY,	AA343AC4
+DEMODULATOR INPUT	AA351AH4
+◇LIM DIST 1 2W DEMOD IN	AA344AJ1
+◇LIM DIST 1 4W DEMOD IN	AA345AG1
-E LITE	CE011AM4
+ENTER SERDES	AA101BH2
-ENTER SERDES	AA101BH6
-ENTER SERDES GATE	AA131AU6
-EOT	AA101BK6
-EOT GATE	AA101AS4
-◇EOT GATE	AA411BG4
GROUND-X	AA391AK4
-HALT-1	AA401AJ4
+INCORRECT CASE	AA091AN4
-INCORRECT CASE	AA091AM4
-◇INCORRECT CASE	AA421BL4
-INDEX MD	AA011AS2
+INITIAL LOWER CASE	AA411AX4
-INITIAL LOWER CASE	AA411BJ4
+INTEGRATED PRINTER 1-8 BIT	AA162AA2
+INTEGRATED PRINTER 2-A BIT	AA162AC2
+INTEGRATED PRINTER 3-8 BIT	AA161AG2
+INTEGRATED PRINTER 4-4 BIT	AA162AG2
+INTEGRATED PRINTER 5-2 BIT	AA161AE2
+INTEGRATED PRINTER 6-1 BIT	AA161AF2

SIGNAL NAME	NET NO.
+INTEGRATED PRINTER 7-C BIT	AA162AE2
-INVALID CHAR	AA182AP4
-◇INVALID CHAR	AA411AR4
-IOC N-C 1	AA163AA2
+IOC N-O 1	AA163AC2
+IO CYCLE	AA141AP4
-IO CYCLE	AA141AN4
+INTERRUPT	AA201AG2
-INTERRUPT	AA201AG6
-INTERRUPT RESET GATE	AA201AY4
-◇INTERRUPT RESET GATE	AA401AF4
-INTERRUPT SET GATE	AA401AE4
-KEYBOARD MD	AA014AP2
-LIM DIST TYPE 2 CARRIER	CC011AQ4
+LIM DIST TYPE 2 RECEIVED DATA	CC011AN4
LIM DIST TYPE 2 LINE 1	CC011AP6
LIM DIST TYPE 2 LINE 2	CC011AP2
+LEASED LINE 2W CLEAR TO SEND	CC031AA6
+LEASED LINE 4W CLEAR TO SEND	CC021AA6
+LIM DIST TYPE 2 CLEAR TO SEND	CC011AA6
◇LIM DIST 1 2W LINE 1	AA344AE3
◇LIM DIST 1 2W LINE 2	AA344AE5
◇LIM DIST 1 4W TRANS LINE 1	AA345AE2
◇LIM DIST 1 4W TRANS LINE 2	AA345AE3
+LINE	AA131BB4
-LINE	AA131AV4
LIM DIST TYPE 1 LINE 1	AA351AK4
LINE 1 (2W) OR XMIT (4W)	CC061AD4
LIM DIST TYPE 1 LINE 2	AA351AJ4
LINE 2 (2W) OR XMIT (4W)	CC061AE4
LEASED LINE 2W LINE 1	CC031AV6
LEASED LINE 2W LINE 2	CC031AV2
-LEASED LINE 2W CARRIER	CC031AW4
+LEASED LINE 2W RECEIVED DATA	CC031AU4
LEASED LINE 4W XMIT LINE 1	CC021AV6
LEASED LINE 4W XMIT LINE 2	CC021AV2
-LEASED LINE 4W CARRIER	CC021AW4
+LEASED LINE 4W RECEIVED DATA	CC021AU4
+LOCAL	AA201AN2
-LOCAL MODE	AA351AF4
-◇103F LOCAL MODE	AA341AE4
-◇EIA WE WU LOCAL MODE	AA346AH4
+LONG FUNCTION	AA161AJ2
+LOWER CASE 1	AA171AF2
-◇MODE CHANGE-A	AA371AA4
+MODE CHANGE LATCH	AA211AG2
-MODE CHANGE LATCH	AA211AG6
-MODEM TEST LIGHT	CC022AM4
-MODEM POR-X	CC061AF4

SIGNAL NAME	NET NO.
-NON PRINT MD	AA011AN2
-XOPERATE	AA391AJ4
+OPERATE LATCH	AA141BF2
-OPERATE LATCH	AA141BF6
-◇103F FD ORIGINATE MODE	AA341AD4
+POWER ON RESET	AA121AL4
-POWER ON RESET	AA141AH4
-XPOWER ON RESET	AA201AZ4
-POWER ON RESET-X	AA172AK4
+POWER ON RESET-1	AA141BJ4
+◇POWER ON RESET-1	AA371AE4
+◇POWER ON RESET-1	CE041AG4
+PRINT	AA251AM4
+PRINT INHIBIT LATCH	AA691SP4
+PRINTOUT	AA091AJ4
+◇PRINTOUT	AA421BK4
+RECEIVED DATA	CC061AB4
-REPEAT	AA371AT6
-◇REPEAT SET GATE	AA421AJ4
+REQUEST TO SEND	AA411AU1
+ EIA WE-WU REQ TO SEND	AA346AA2
+◇103F FD REQ SEND EIA	AA341AB2
+◇MODEM REQUEST TO SEND	AA282AF4
-RESET BID	AA391AG4
-RESET LOCAL	AA131AC4
-R1MD	AA012AC2
-R2MD	AA013AA2
-R2A MD	AA013AB2
-R5MD	AA012AA2
+SDAC	AA061AY4
-SDAC	AA052AA2
-SDCAC1	AA052AB2
-SDCAC2	AA052AC2
+SERDES MV	AA361AE4
-SERDES MV	AA361AD2
+SD1	AA061AS2
-SD1	AA061AS6
+SD2	AA061AT2
+SD3	AA061AU2
-SD4	AA061BG6
+SEND	AA411AQ4
-SEND	AA391AH4
-(SEND)	AA391AF4
+SERIAL DATA IN	AA131AH4
+◇SERIAL DATA IN	CE041AF4

DATE	E.C. NO.	DATE	E.C. NO.
	SEE INDEX		
FEB67	507567		
APR68	307100		

SIGNAL SOURCE LISTING

NUMBER 1

PART NO. 1176195 PAGE NO. 9001

IBM 2741

SIGNAL NAME	NET NO
-SERIAL DATA IN	AA351AA4
-◇DSA SERIAL DATA IN	AA281AA2
-◇LIM DIST I SERIAL DATA IN	AA283AE4
-◇MODEM SERIAL DATA IN	AA282AA4
-◇SERIAL DATA IN	CE041AD4
-SERIAL DATA OUT	AA101AW4
+◇SERIAL DATA OUT	AA401AD4
-MODEM SERIAL DATA OUT	AA282AH4
-SET BID	AA391AB4
-SET LOCAL	AA391AA4
+SET LOCAL EXT	AA391AA7
+SHARED LINE 2W CLEAR TO SEND	CC051AA6
+SHARED LINE 2W RECEIVED DATA	CC051AY4
+SHARED LINE 4W CLEAR TO SEND	CC041AA6
+SHARED LINE 4W RECEIVED DATA	CC041BD4
-SHIFT LAT KNOCK OFF MD	AA014AC2
-SHIFT MD	AA012AD2
-SHARED LINE 2W CARRIER	CC051AZ4
+SHARED LINE 4W CARRIER	CC041BE4
SHARED LINE 2W LINE 1	CC051AX2
SHARED LINE 2W LINE 2	CC051AX6
SHARED LINE 4W XMIT LINE 1	CC041AV2
SHARED LINE 4W XMIT LINE 2	CC041AV6
+S REGISTER EMPTY	AA131AF2
+XS REGISTER EMPTY	AA131BM4
-S REG EMPTY SET GATE	AA221AX4
-S REGISTER RESTORE	AA101AT4
-S REGISTER TP	AA021AB4
+S REG 0-START BIT	AA031BA2
-S REG 0-START BIT	AA031BA6
-S REG 0 RESET	AA221AV4
+S REG 1-B BIT	AA031AV2
-S REG 1-B BIT	AA031AV6
-S REG 1 RESET	AA221AP4
+S REG 2-A BIT	AA031AQ2
-S REG 2-A BIT	AA031AQ6
-S REG 2-RESET	AA221AN4
+S REG 3-8 BIT	AA031AK2
-S REG 3-8 BIT	AA031AK6
-S REG 3 RESET	AA221AM4
+S REG 4-4 BIT	AA031AE2
-S REG 4-4 BIT	AA031AE6
-S REG 4 RESET	AA221AL4
+S REG 5-2 BIT	AA021AX2
-S REG 5-2 BIT	AA021AX6
-S REG 5 RESET	AA221AK4
+S REG 6-1 BIT	AA021AS2
-S REG 6-1 BIT	AA021AX6
-S REG 6 RESET	AA221AJ4
+S REG 7-C BIT	AA021AM2
-S REG 7-C BIT	AA021AM6
-S REG 7 RESET	AA221AH4
+S REG 8-STOP BIT	AA021AG2
-S REG 8-STOP BIT	AA021AG6
+STOP CLOCK	CE011AY2
-STOP CLOCK	CE011AY6
-STOP CLOCK AC RESET	CE031AW4
-STOP CLOCK RESET GATE	CE031AU4
+XSTROBE	AA201AU2
-XSTROBE	AA201AU6
-STROBE N-C 1	AA163AE2
+STPOBE N-O 1	AA163AG2
+STROBE 0 LATCH	AA101BJ2
-STROBE 0 LATCH	AA101BJ6
-STROBE 0 RESET GATE	AA101AR4
-◇STROBE 0 SET GATE	AA371AB4

SIGNAL NAME	NET NO
-TAB MD	AA011AP2
-TO BK SP MD	AA251AJ4
-TO CHECK MD	AA241AQ4
-TO CR MD	AA251AK4
-TO INDEX MD	AA251AH4
-TO KYBD LOCK MD	AA231AV4
-TO KYBD SH TR MD	AA411BF4
-TO NON PRINT MD	AA251AN4
-TO R1 MD	AA241AL4
-TO R2 MD	AA241AS4
-TO R2A MD	AA241AN4
-TO R5 MD	AA241AD4
-TO SHIFT MD	AA251AS4
-TO TAB MD	AA251AL4
-TO T1 MD	AA241AF4
-TO T2 MD	AA241AB4
-TRANSMIT DATA	AA351AC4
-◇EIA TRANSMIT DATA	AA281AB2
-T1 MD	AA013AC2
-T2 MD	AA013AD2
+UPPER CASE 1	AA171AG2
+1B EMPTY	AA184AL4
+1B FULL	AA184AG4
+X1B FULL	AA391AP4
+1B GENERATE	AA182AA4
-1B GENERATE	AA201AX4
-1B1 LITE-B BIT	CE021AD4
-1B2 LITE-A BIT	CE021AF4
-1B3 LITE-8 BIT	CE021AH4
-1B4 LITE-4 BIT	CE021AK4
-1B5 LITE-2 BIT	CE021AM4
-1B6 LITE-1 BIT	CE021AP4
-1B7 LITE-C BIT	CE021AS4
+1BOK	AA371BB4
+◇1BOK	AA231BD4
+1B REG 1-B BIT	AA181BB4
-1B REG 1-B BIT	AA181BE4
+1B REG 2-A BIT	AA181BC4
+◇1B REG 2-A BIT	AA431AG4
-1B REG 2-A BIT	AA181BH4
+1B REG 3-8 BIT	AA184AN4
-1B REG 3-8 BIT	AA184AP4
+1B REG 4-4 BIT	AA181AM4
-1B REG 4-4 BIT	AA181BF4
+1B REG 5-2 BIT	AA183AU4
-1B REG 5-2 BIT	AA183AT4
+◇1B REG 5-2 BIT	AA431AH4
+1B REG 6-1 BIT	AA183AR4
-1B REG 6-1 BIT	AA183AK4
+1B REG 7-C BIT	AA182AQ4
-1B REG 7-C BIT	AA182AL4
-1B RESET	AA231BC4

SIGNAL NAME	NET NO.
+1B SET	AA141AD4
+1 CYCLE HALT	CE031AA2
+2B EMPTY	AA091AG4
+2B FULL	AA091AF4
+◇2B OVERFLOW RESET	AA421BM4
-◇2B OVERFLOW RESET-A	AA391AD4
+2B REG 1-8 BIT	AA081AE4
-2B REG 1-8 BIT	AA081BB4
+2B REG 2-A BIT	AA081AJ4
-2B REG 2-A BIT	AA081AH4
+2B REG 3-8 BIT	AA081AN4
-2B REG 3-8 BIT	AA081AM4
+2B REG 4-4 BIT	AA081AS4
-2B REG 4-4 BIT	AA081AR4
+2B REG 5-2 BIT	AA081AW4
-2B REG 5-2 BIT	AA081AV4
+2B REG 6-1 BIT	AA081BA4
-2B REG 6-1 BIT	AA081AZ4
-2B REG 7-C BIT	AA091AC4
-2B RESET	AA121AK4
-◇2B RESET	AA421BN4
+2B RESET LATCH	AA121BE2
+2B SET	AA183AN4
+X2B SET	AA121AZ2
-2B SET	AA121AZ6
-X2B SET	AA231AY4
-2B SET RESET GATE	AA231AN4
-2B SET SET GATE	AA121BQ4
-◇2B SET SET GATE	AA371AC4
-◇2B SET SET GATE	AA421AV4
+48 VOLTS	AA261AA4

NOTE: VERSION 002 ADDED THE FOLLOWING NETS FOR SPECIAL FEATURES-AUTO ADDRESS A/B, TRANSMIT INTERRUPT RED RIBBON CONTROL AND PRINT INHIBIT

+A-B BIT 5	AA611SR4
+A-B BIT 6	AA611SS4
+A-B BIT 7	AA611SM4
-AUTO ADD LATCH	AA601SD4
-◇AUTO EOT SET GATE	AA601SR4
-CHARACTER 1	AA601SV4
-CHARACTER 2	AA601SW4
-CHARACTER 3	AA601SN4
-CHARACTER 4	AA601SM4
-◇INVALID CHARACTER	AA651SX4
-KYBD LOCK EXT	AA231AS7
+PREFIX	AA651SH2
+PRINT INHIBIT LATCH	AA691SP4
-NON PRINT HOLD MD	AA691SR2
-RIB SHIFT MAG	AA651SU1
+SEND	AA651TA4
-◇1B REG 1-B BIT	AA181BE4
-◇1B REG 2-A BIT	AA181BH4
-◇1B REG 3-8 BIT	AA184AH4
-◇1B REG 4-4 BIT	AA181BF4
-◇1B REG 5-2 BIT	AA183AJ4
-◇1B REG 6-1 BIT	AA183AK4
-◇1B REG 7-C BIT	AA182AL4
-◇1B RESET	AA651SK4

DATE	E.C. NO.	DATE	E.C. NO.	SIGNAL SOURCE LISTING
JUL 68	345323			NUMBER 2
DEC 68	348062			PART NO. 1827350 PAGE NO. 9002
MAR70	308734			IBM 2741 VER 002

SIGNAL NAME	NET NO.	ALD PAGE
+ATTENTION N-C	003	AA171
-ATTENTION N-O	001	AA171
-C6 N-O	001	AA431
+COMM N-C	002	AA172
-COMM N-O	001	AA172
-CR OR TAB INTLK	004	AA161
+CYCLE N-C	003	CE031
-CYCLE N-O	002	CE031
-CYCLE HALT N-O	001	CE031
+EIA CARRIER DETECTOR	002	AA341
	002	AA346
+EIA CLEAR TO SEND	003	AA341 AA343 AA346
+EIA DATA SET READY	001	AA281
-EIA RECEIVED DATA	002	AA281
-GROUND	001	AA391
+IOC N-C	001	AA163
-IOC N-O	002	AA163
-LOWER CASE CONT	004	AA171
+MODEM TEST	003	CC021
		CC031
		CC041
		CC051

SIGNAL NAME	NET NO.	ALD PAGE
-POWER SUPPLY N-C	003	AA172
-PRINTER OUT 1-B BIT	001	AA162
-PRINTER OUT 2-A BIT	002	AA162
-PRINTER OUT 3-8 BIT	003	AA161
-PRINTER OUT 4-4 BIT	004	AA162
-PRINTER OUT 5-2 BIT	001	AA161
-PRINTER OUT 6-1 BIT	002	AA161
-PRINTER OUT 7-C BIT	003	AA162
RECEIVE LINE 1	001	AA345
RECEIVE LINE 2	001	AA345
RECEIVE - 1 (4W)	002	CC021
		CC041
RECEIVE - 2 (4W)	001	CC021
		CC041
-SPACE N-O	001	CE041
+STROBE N-C	003	AA163
-STROBE N-O	004	AA163
-TYPAMATIC N-O	001	AA421
-UPPER CASE CONT	002	AA171,
+V REG	001	AA361
-1 CYCLE HALT N-O	001	CE031
+12 VOLTS	001	AA343
-12 VOLTS	001	AA261
-12 VOLTS	001	AA341
-12 VOLTS	001	AA346

DATE	E.C. NO.	DATE	E.C. NO.	SIGNAL SOURCE LISTING
APR68	307100			NUMBER 3
				PART NO. 5162304 PAGE NO. 9003
				IBM 2741

9500

P/N 5994675
E.C. 308747

ALD'S
(AUTOMATED LOGIC DIAGRAMS)

2741
COMMUNICATIONS
TERMINAL
VERSION 002

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				PART NO.5994676	PAGE NO.9501
				IBM 2741	Y55 002

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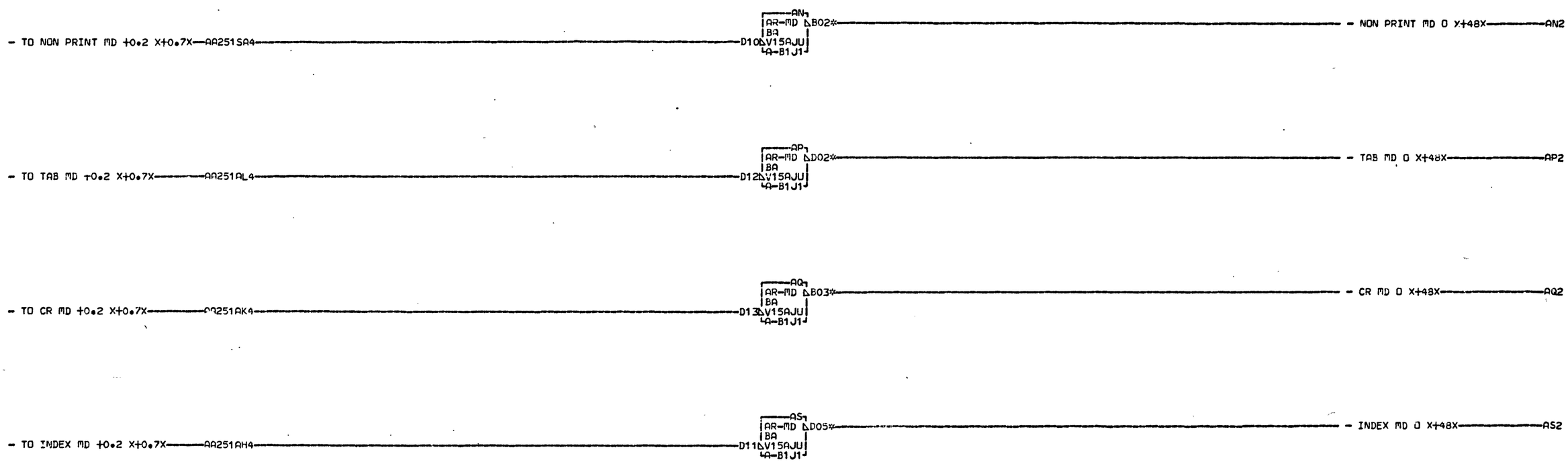
LIMITED DISTANCE TYPE-2	CC011	307100	5162289
LEASED LINE 4 WIRE ADAPTER	CC021	307100	5162290
MOD TEST AND GLITCH PROTECTION	CC022	307100	5162291
LEASED LINE 2 WIRE ADAPTER	CC031	307100	5162292
SHARED LINE 4 WIRE ADAPTER	CC041	307100	5162293
SHARED LINE 2 WIRE ADAPTER	CC051	307100	5162294
SERV BLOCKS AND MODEM DOT OVERLAYS	CC061	345323	1277402
CE AID CYCLE INKL AND STOP CLOCK LATCHES	CE011	307100	1176242
CE AID INDICATOR DRIVERS	CE021	307100	1176243
CE AID CYCLE LATCH	CE031	307100	1176244
CE AID	CE041	345323	1277403

DATE	EC.NO.	DATE	E.C.NO.	TABLE OF CONTENTS
JUN 68	345323			
NOV 68	346052			PART NO. 5166222 PAGE NO. 9502
				IBM 2741 VER 002



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AP2 A-B1M1D04
AQ2 A-B1M1503
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LOC. TYPE
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P-N 5803569
E.C. HISTORY
MACH.2741A
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DATE LAST EC
06-03-68 345323
P.N. 1277183

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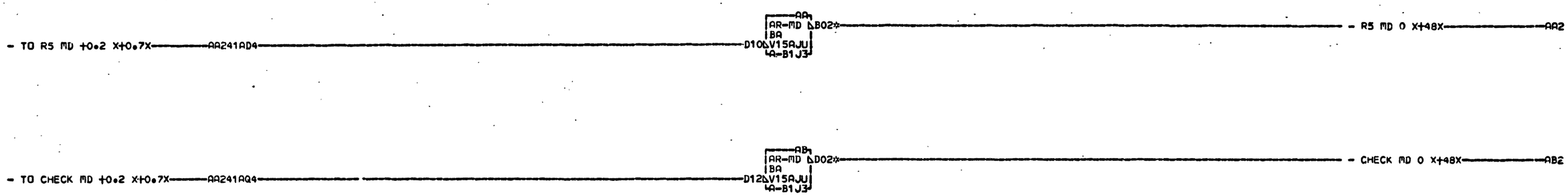
002
SIM TO PN 1176207 EC 307100



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AA2 A-B1N1D09
AB2 A-B1N1B08
AC2 A-B1N1B12
AD2 A-B1N1B03

LOC. TYPE
A-B1J3

MAGNET DRIVERS-2
P-N 5803569
—E.C.—HISTORY—
MACH.2741A
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IBM CORP. SDD
DATE LAST EC
10-30-67 307100
P.N. 5162277

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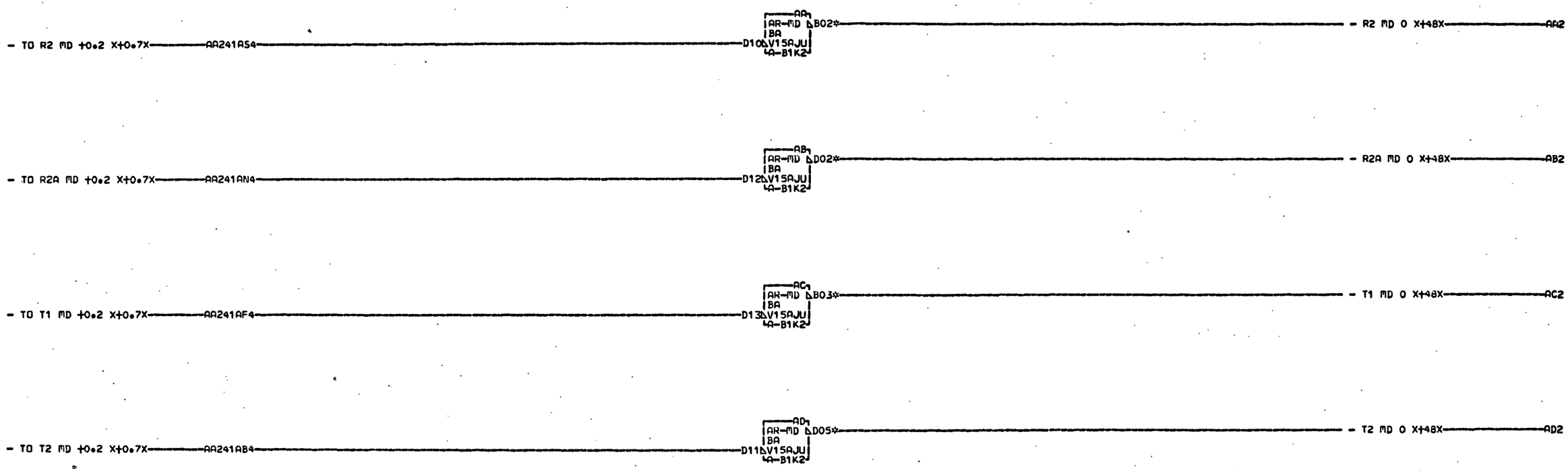

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AB2 A-B1N1B10
AC2 A-B1N1D10
AD2 A-B1N1B09

LOC. TYPE
A-B1K2

MAGNET DRIVERS-3
P-N 5803569
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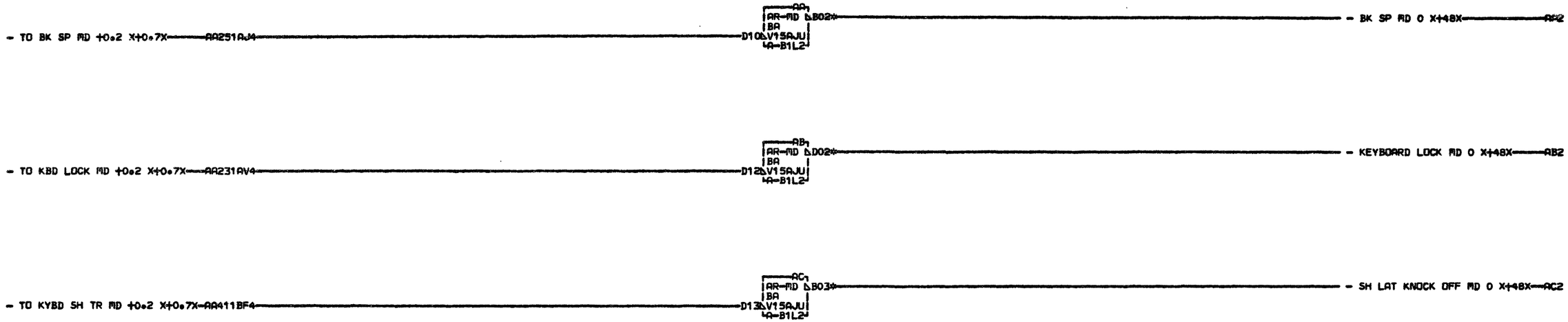
FRAME 01
IBM CORP. SDD
DATE LAST EC
10-30-67 307100
P.N. 5162278



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AB2 A-B1N1D07
AC2 A-B1M1B12

LOC. TYPE
A-B1L2

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002
SIM TO PN 5162285 EC 307100

MAGNET DRIVERS-4
P-N 5803569
E.C.-HISTORY
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IBM CORP. SDD
DATE LAST EC
11-13-67 345323
P.N. 5166217

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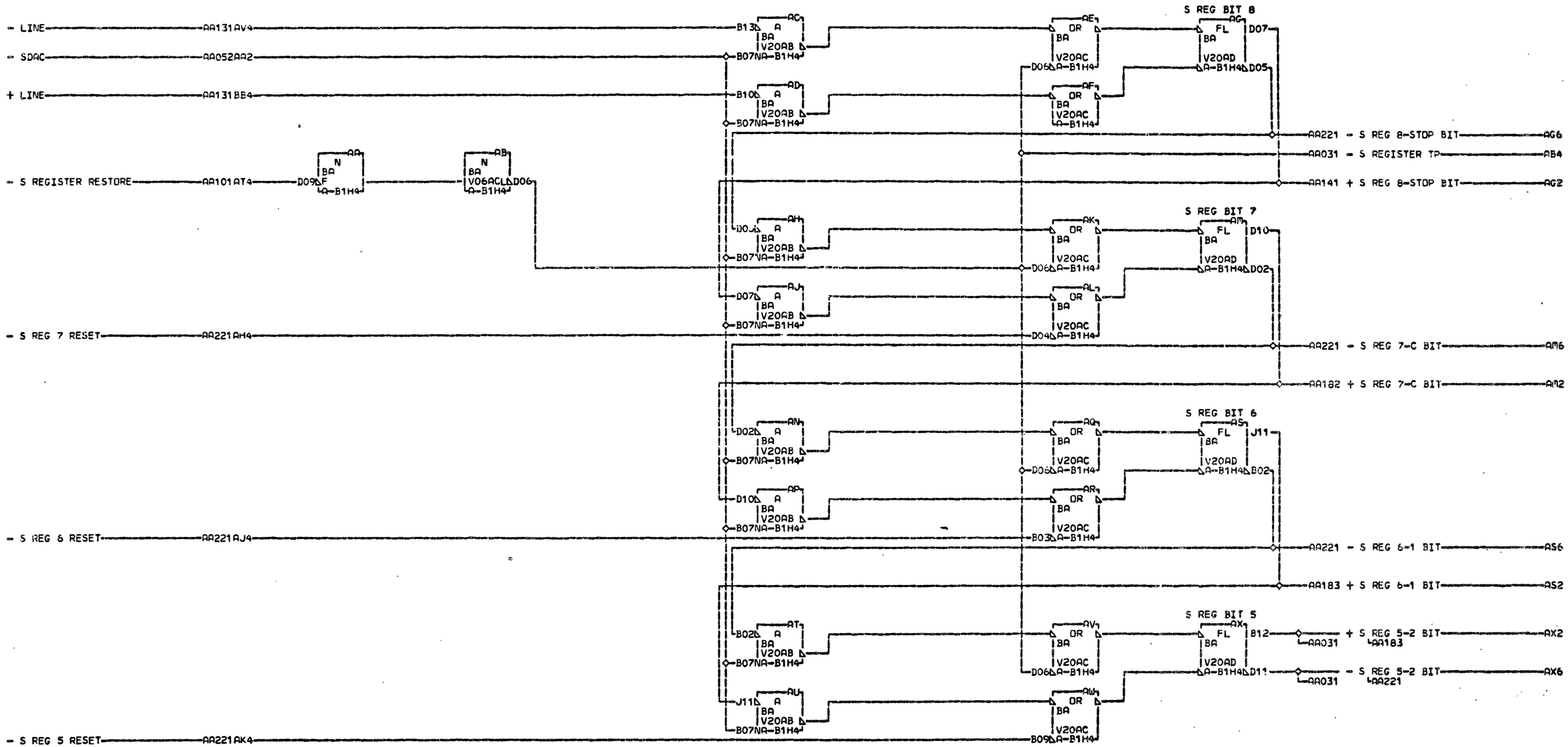
002



THE LOGIC ON SLT CARD
P-N 5804440 IS EQUIVALENT
A TO THAT SHOWN ON THIS PAGE
A INPUT AND OUTPUT PIN
0 FUNCTIONS ARE IDENTICAL
2
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LOC. TYPE
A-B1H4

S REGISTER P-N 5807362		
E.C.-HISTORY	MACH.2741A	A A 0 2 1
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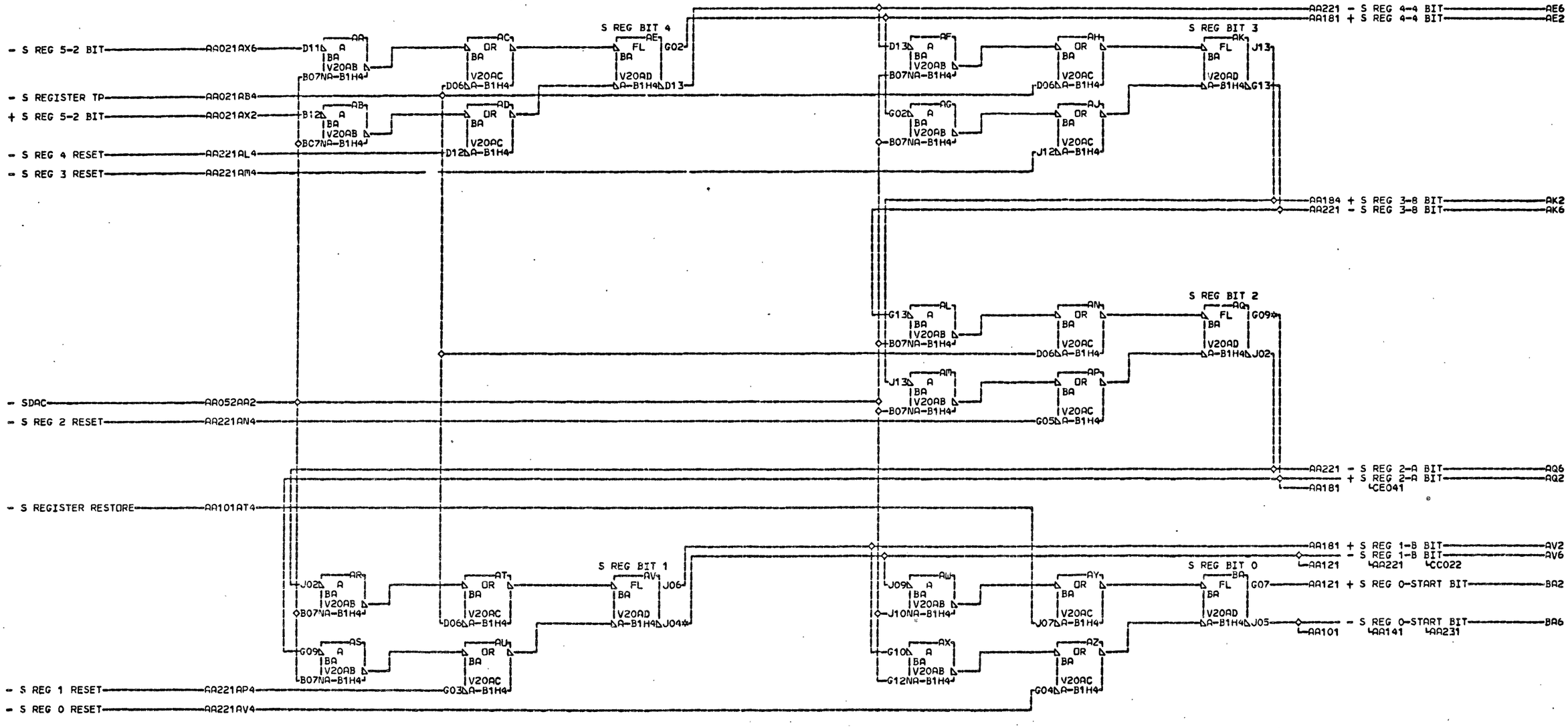

THE LOGIC ON SLT CARD
P-N 5804440 IS EQUIVALENT
TO THAT SHOWN ON THIS PAGE
INPUT AND OUTPUT PIN
FUNCTIONS ARE IDENTICAL

AQ2 A-B1D1D11
AV6 A-B1N4D05
01A-C1B5D05

LOC. TYPE
A-B1H4

S REGISTER P-N 5807362	
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	FRAME 01
	IBM CORP. LX
DATE LAST EC	P.N. 1176209
05-03-68 307100	

AA031

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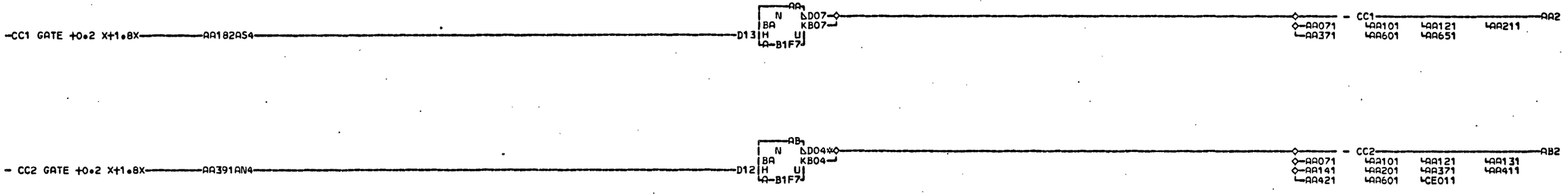

AB2 A-B1D1D05

LOC. TYPE
A-B1F7

AA051
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SIM TO PN 1176211 EC 307100

CONTROL CLOCK-1
P-N 5803086
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FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.N. 1277316

AA051
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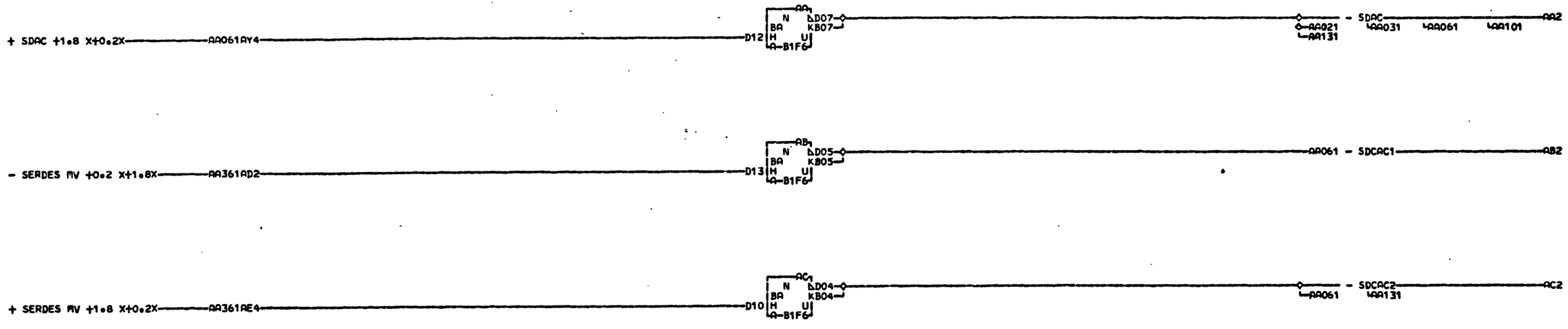

A A 0 5 N

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LOC. TYPE
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P.N. 5162286

DATE LAST EC
11-09-67 307100

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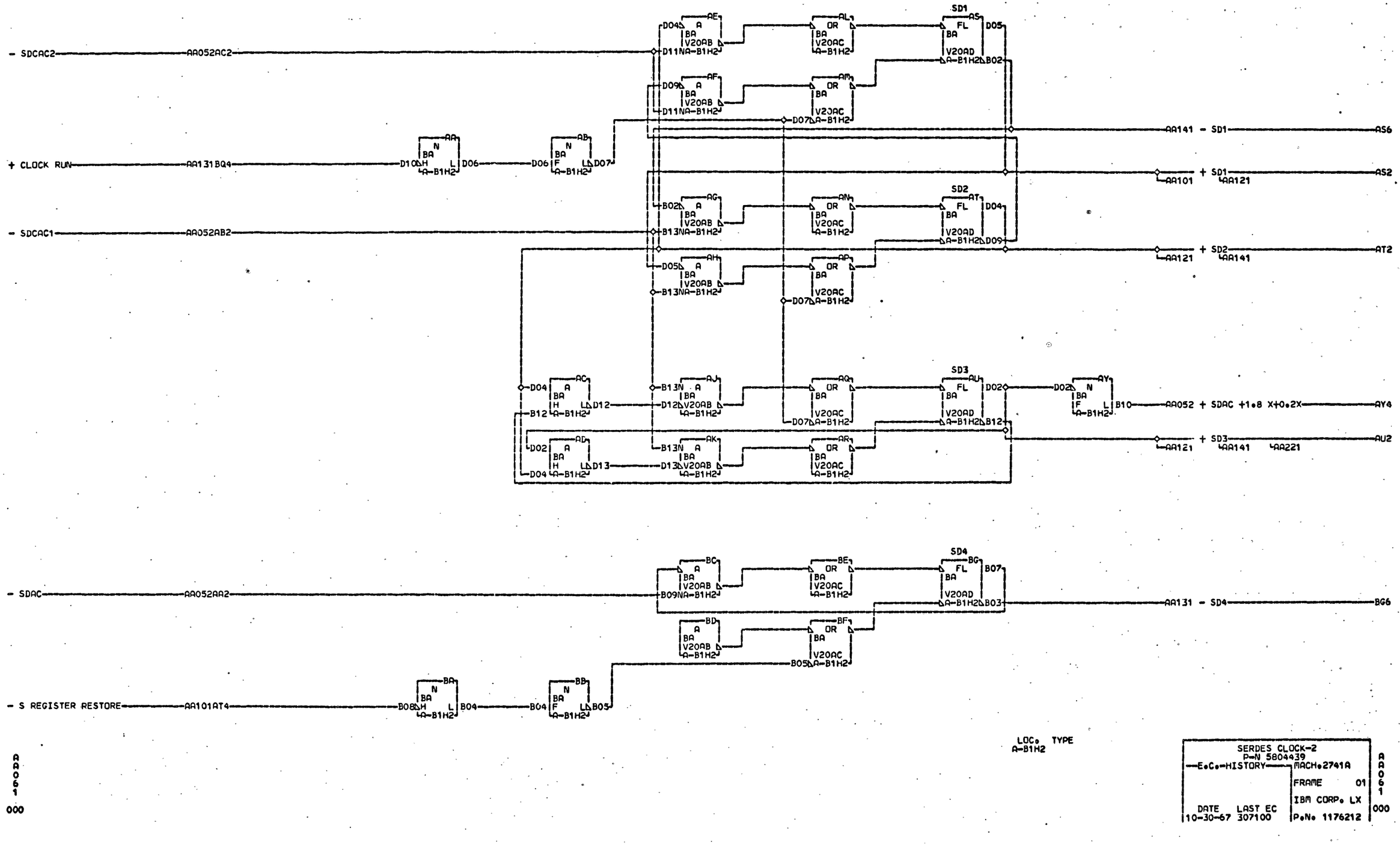
- SDCAC2
AA052AC2
D11 NA-B1H2
D04
D09
AE
AF
A
BA
V20AB
A-B1H2
OR
V20AC
AL
AM
SD1
AS
FL
V20AD
D05
B02
D07
AA141 - SD1 AS6
+ CLOCK RUN
AA131 BQ4
D10 H L D06
D06 F L D07
AA
AB
N
AA101 + SD1 AS2
AA121
- SDCAC1
AA052AB2
B13 NA-B1H2
B02
AG
AN
AT
D04
AA121 + SD2 AT2
AA141
D05
AH
AP
D12
AC
AJ
B12
D13
AD
AK
AQ
AU
D02
AY
B10
AA052 + SDAC +1.8 X+0.2X AY4
AR
AV2
AA221
- SDAC
AA052AA2
B09 NA-B1H2
BC
BE
BG
B07
B03
AA131 - SD4 BG6
SD4
BD
BF
B05
- S REGISTER RESTORE
AA101AT4
B08 H L B04
B04 F L B05
BA
BB
LOC. TYPE
A-B1H2
SERDES CLOCK-2
P-N 5804439
E.C.-HISTORY
MACH.2741A
FRAME 01
IBM CORP. LX
DATE LAST EC
10-30-67 307100
P.No 1176212
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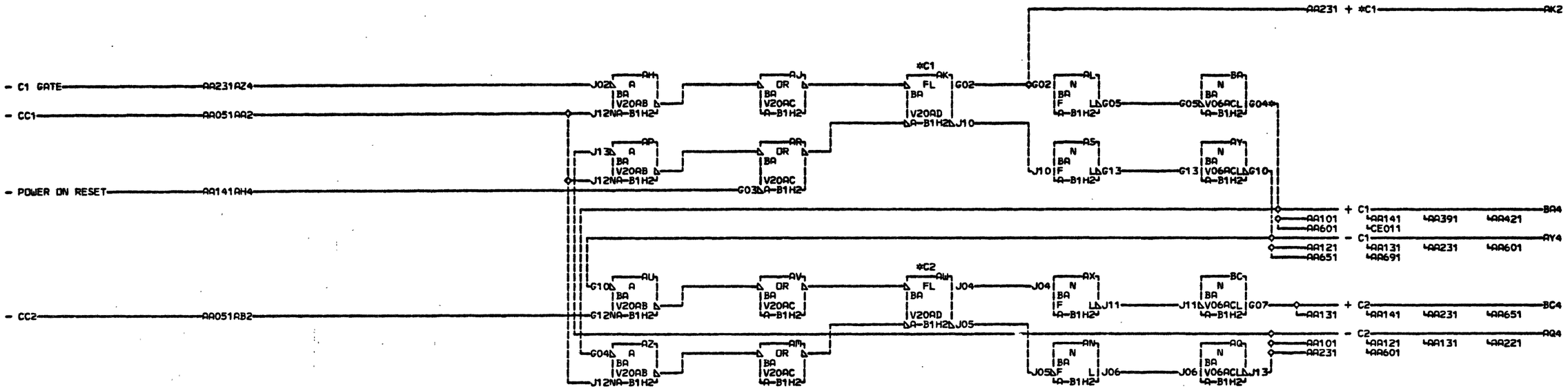

BA4 A-B1D1B02

AA071

002

SIM TO PN 1176213 EC 307100

CONTROL CLOCK-2
P-N 5804439
E.C.-HISTORY
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FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.N. 1277317

AA071

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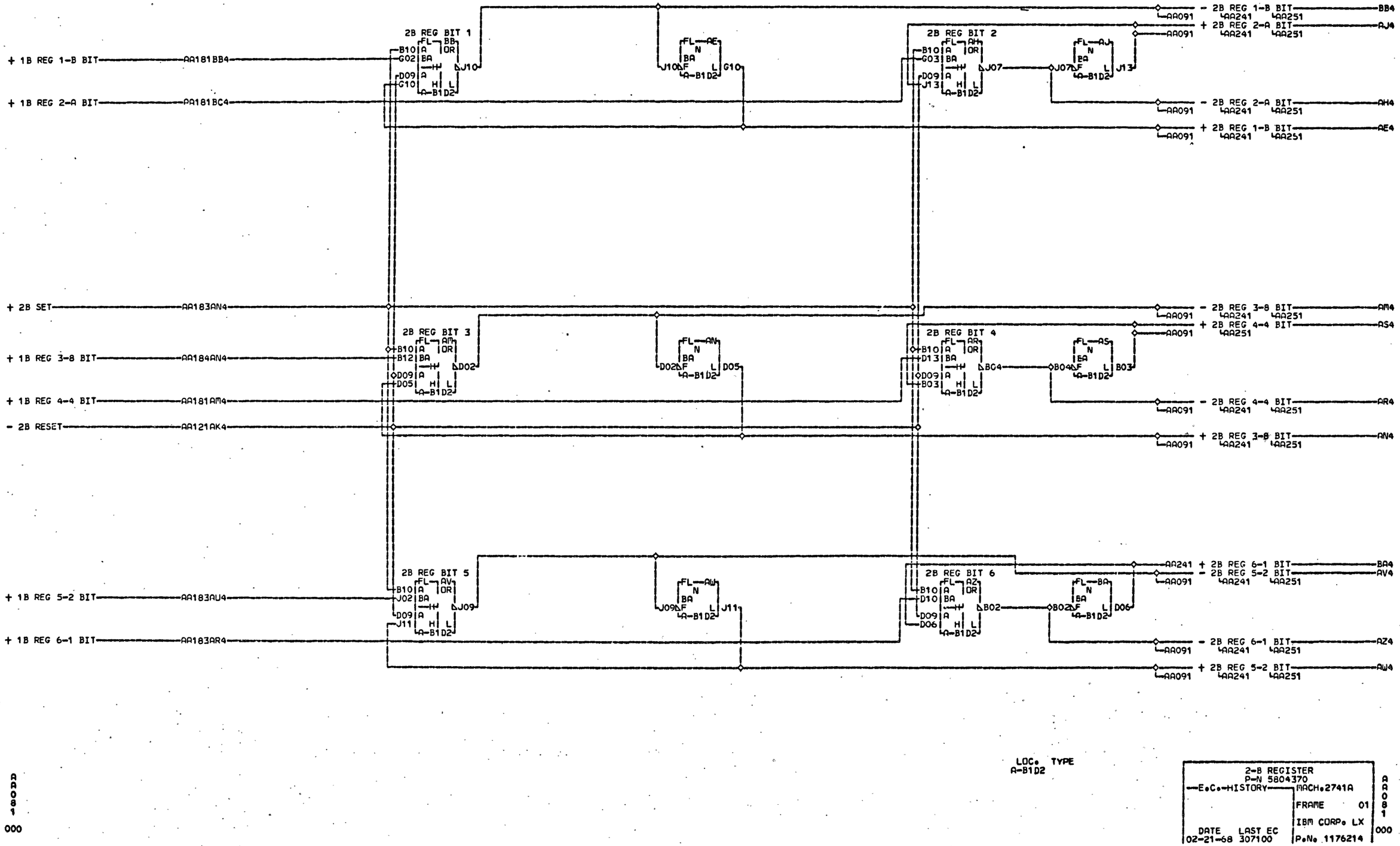

AA081 000

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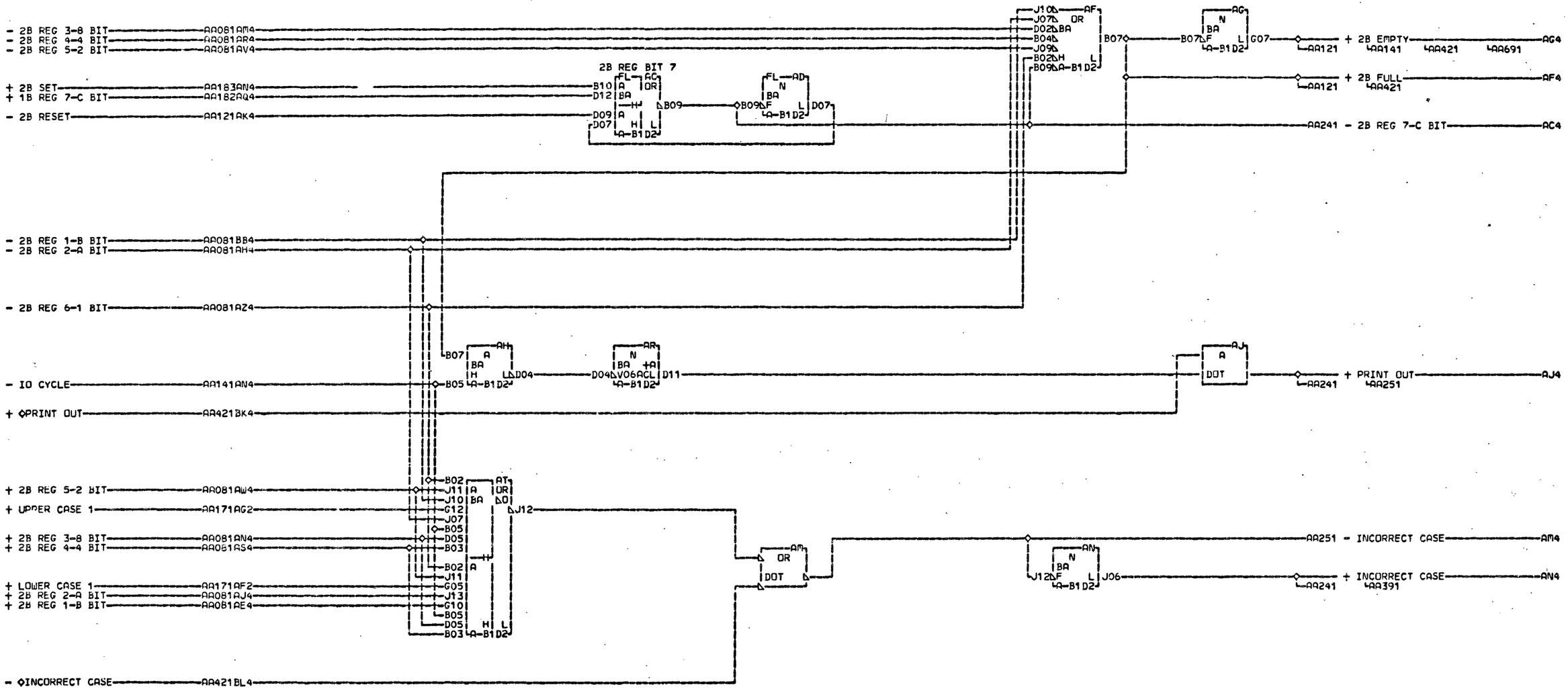
FRAME 01
IBM CORP. LX
DATE LAST EC
02-21-68 307100
P.No. 1176214

AA081 000



LOC. TYPE
A-B1 D2

A A0 91 002
SIM TO PN 1176215 EC 307100

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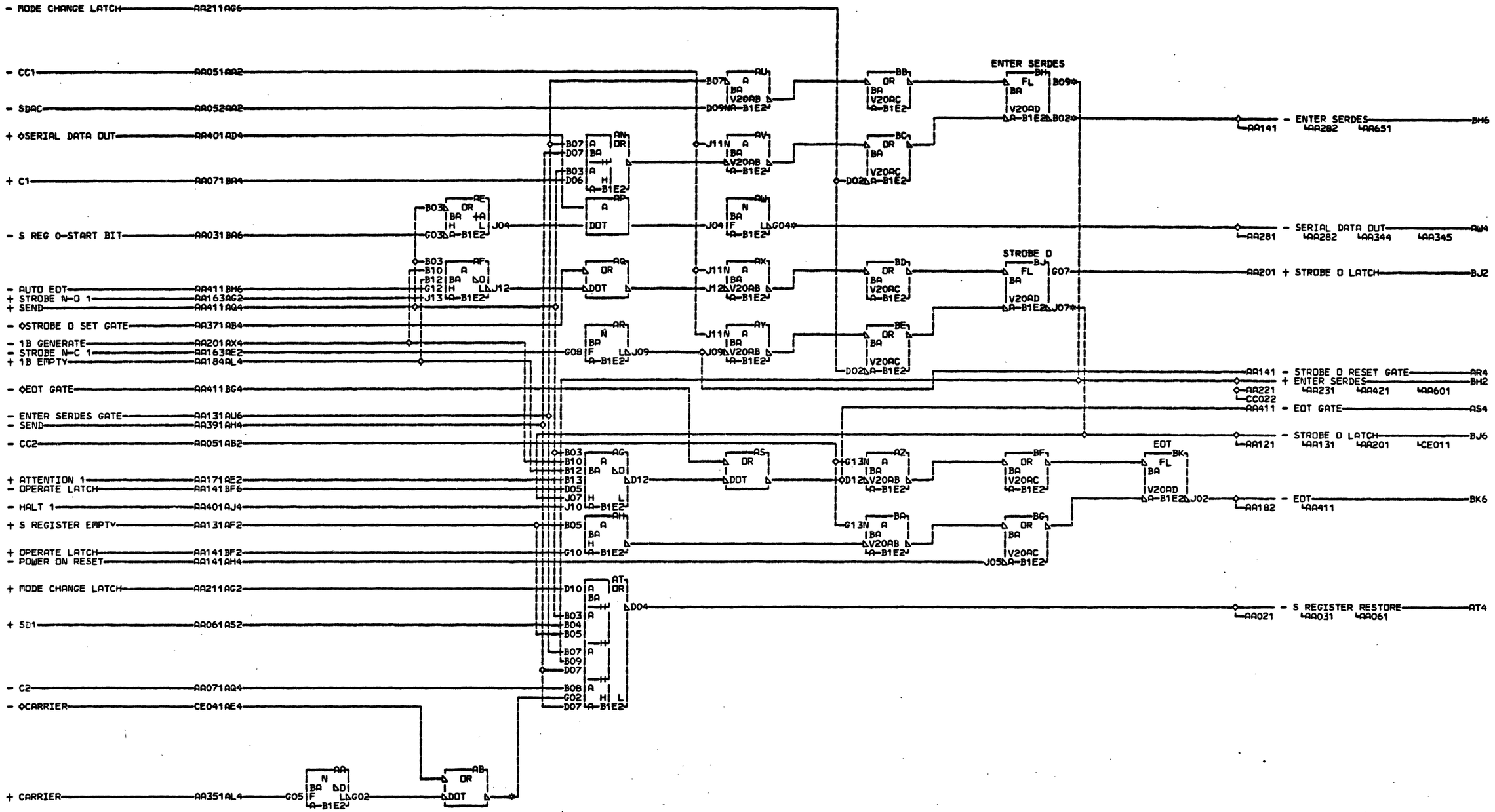
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.No. 1277318
A A0 91 002



THE LOGIC ON SLT CARD
P-N 5804372 IS EQUIVALENT
A TO THAT SHOWN ON THIS PAGE
A INPUT AND OUTPUT PIN
1 FUNCTIONS ARE IDENTICAL
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1

002
SIM TO PN 1176216 EC 307100

AB4 A-B1E1D11
AW4 A-B1K4D02
01A-B1L4D11
BH2 A-B1N4D04
01A-C1B5D04
BK6 A-B1L4B09
BJ6 A-B1D1D06

LOC. TYPE
A-B1E2

STROBE 0-ENTER SERDES AND EOT LATCHES P-N 5807361 A
E.C.-HISTORY MACH.2741A A
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FRAME 01 0
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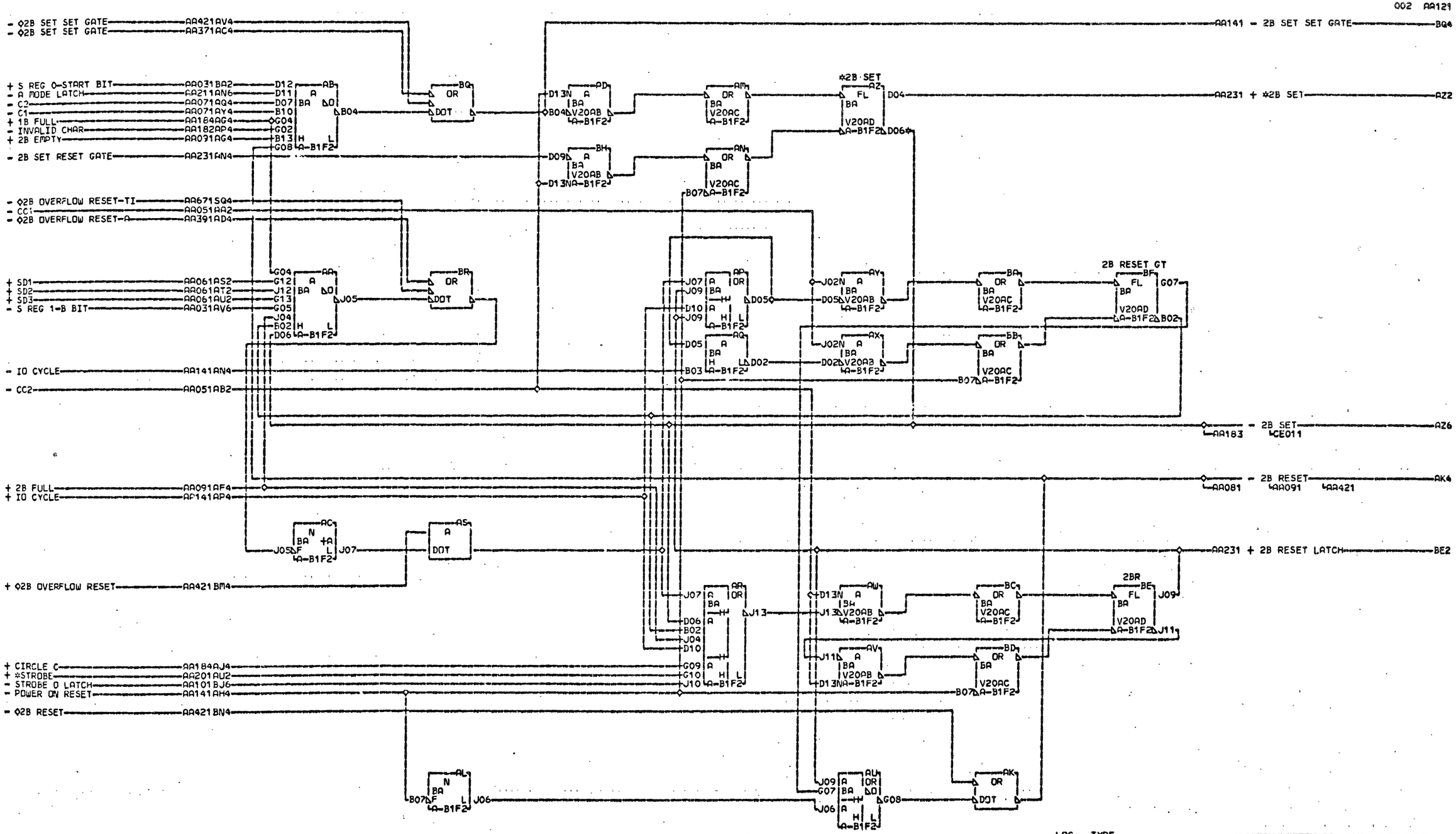
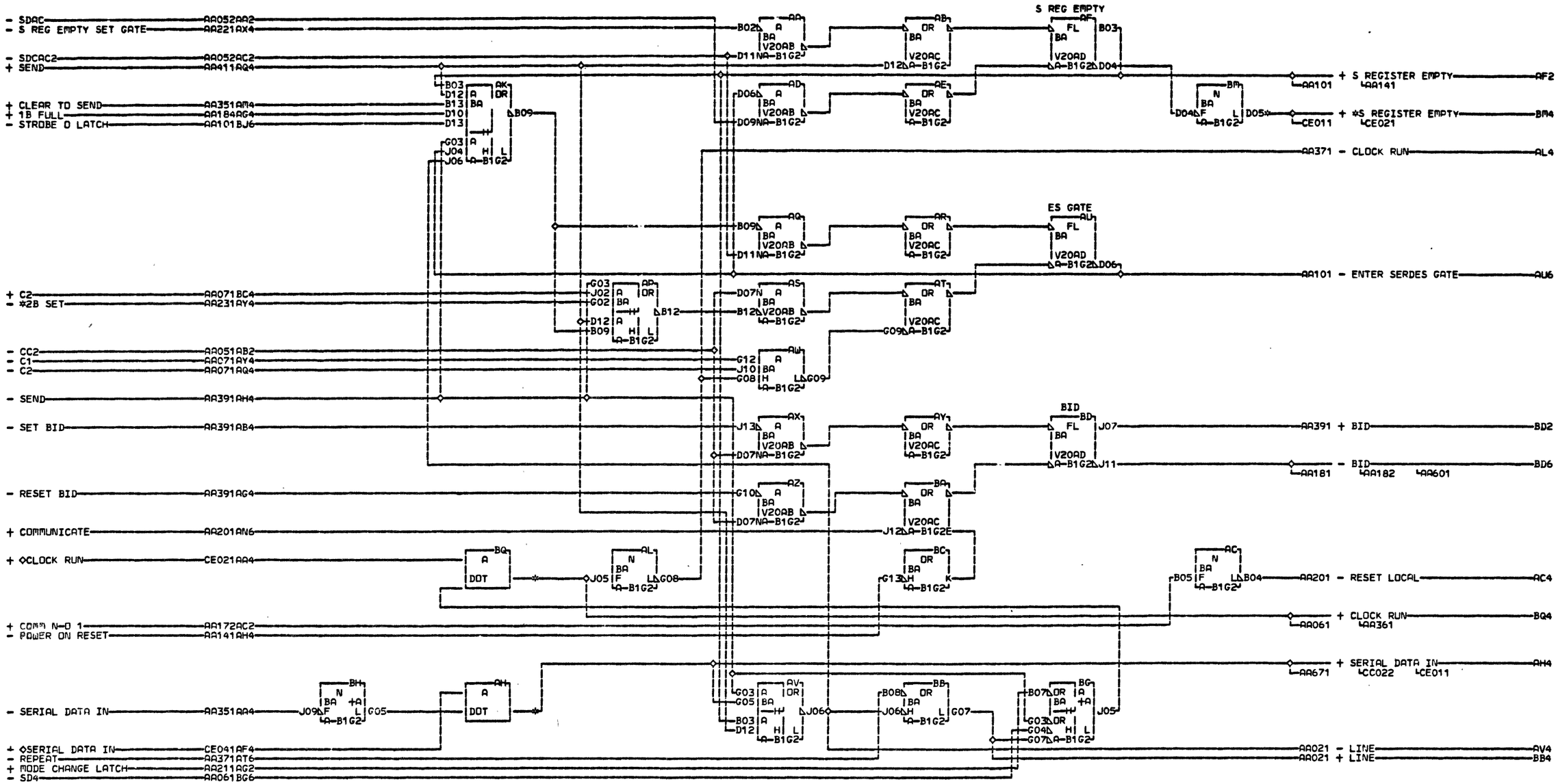
IBM CORP. SDD
DATE LAST EC 002
06-03-68 345323 P.No. 1277319


- ◇2B SET SET GATE AA421AV4
- ◇2B SET SET GATE AA371AC4
AA141 - 2B SET SET GATE BQ4
+ S REG 0-START BIT AA031BA2
- A MODE LATCH AA211AN6
- C2 AA071AQ4
- C1 AA071AY4
+ 1B FULL AA184AG4
- INVALID CHAR AA182AP4
+ 2B EMPTY AA091AG4
- 2B SET RESET GATE AA231AN4
*2B SET
AA231 + *2B SET AZ2
- ◇2B OVERFLOW RESET-TI AA671SQ4
- CC1 AA051AA2
- ◇2B OVERFLOW RESET-A AA391AD4
2B RESET GT
+ SD1 AA061AS2
+ SD2 AA061AT2
+ SD3 AA061AU2
- S REG 1-B BIT AA031AV6
- IO CYCLE AA141AN4
- CC2 AA051AB2
- 2B SET AA183 CE011 AZ6
+ 2B FULL AA091AF4
+ IO CYCLE AF141AP4
- 2B RESET AA081 AA091 AA421 AK4
AA231 + 2B RESET LATCH BE2
+ ◇2B OVERFLOW RESET AA421BM4
+ CIRCLE C AA184AJ4
+ *STROBE AA201AU2
- STROBE D LATCH AA101BJ6
- POWER ON RESET AA141AH4
- ◇2B RESET AA421BN4
OR
DOT
FL
V20AB
V20AC
V20AD
A-B1F2
AZ6 A-B1E1B07
LOC. TYPE
A-B1F2
2B SET AND RESET LATCHES
P-N 5804373
-E.C.-HISTORY-
MACH.2741A
FRAME 01
IBM CORP. RAL
P.N. 5994641
DATE LAST EC
02-09-70 308734
AA121 002
SIM TO PN 1176218 EC 307100



THE LOGIC ON SLT CARD
P-N 5804374 IS EQUIVALENT
A TO THAT SHOWN ON THIS PAGE
A INPUT AND OUTPUT PIN
1 FUNCTIONS ARE IDENTICAL
3 SIM TO PN 1176219 EC 507567
1

AH4	A-B1D1B08
	01A-B1D1B10
	01A-B1N4B13
	01A-C1B5B13
BM4	A-B1E1B05
BQ4	A-B1E1B09

002
SIM TO PN 1176219 EC 307100

LOC. TYPE
A-B1G2

S REG EMPTY-ES GATE AND BID LATCHES P-N 5807364 A
E.C.-HISTORY MACH.2741A A
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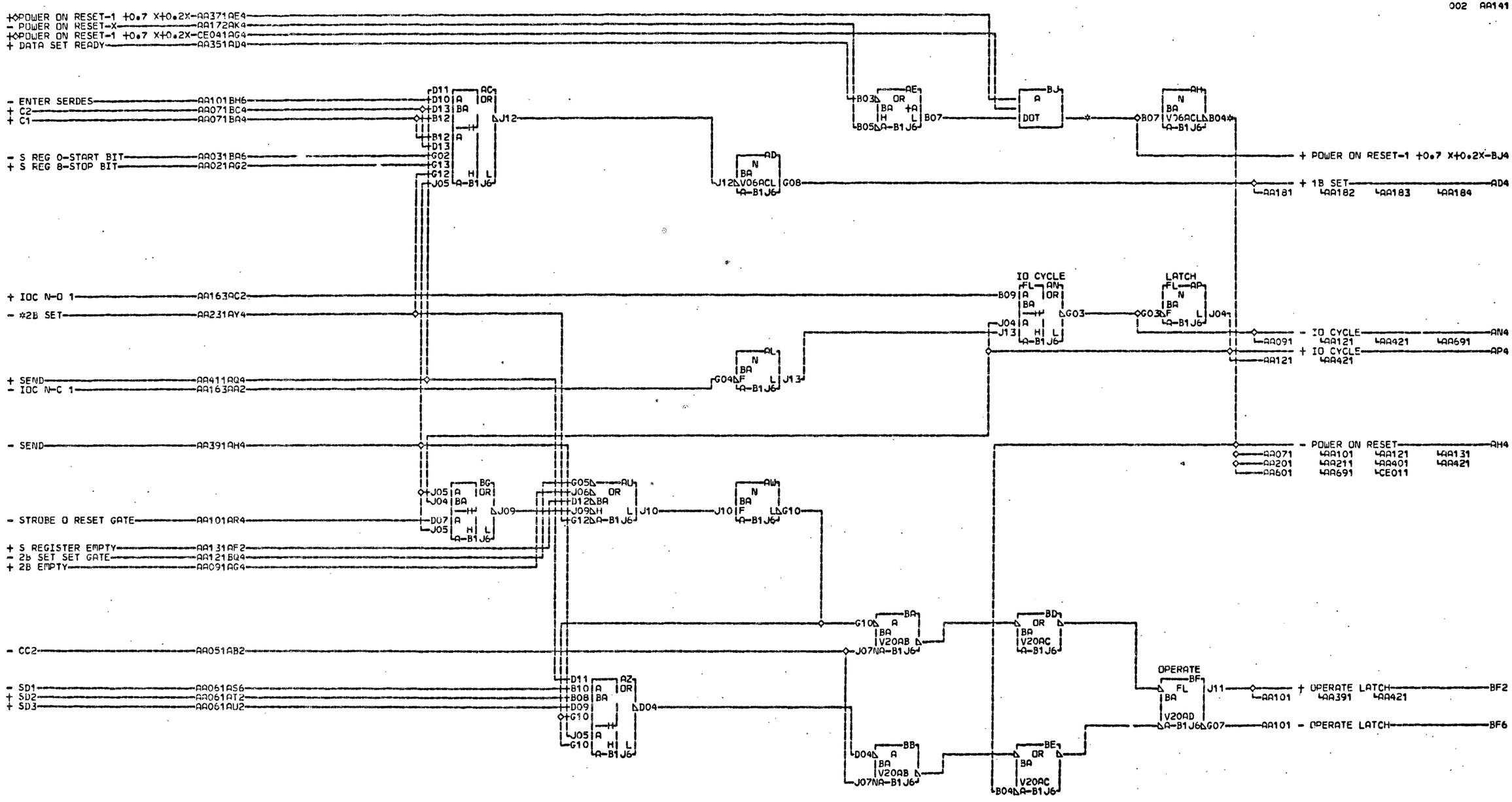
FRAME 01 3
IBM CORP. SDD 1
DATE LAST EC 002
06-03-68 345323 P.N. 1277320



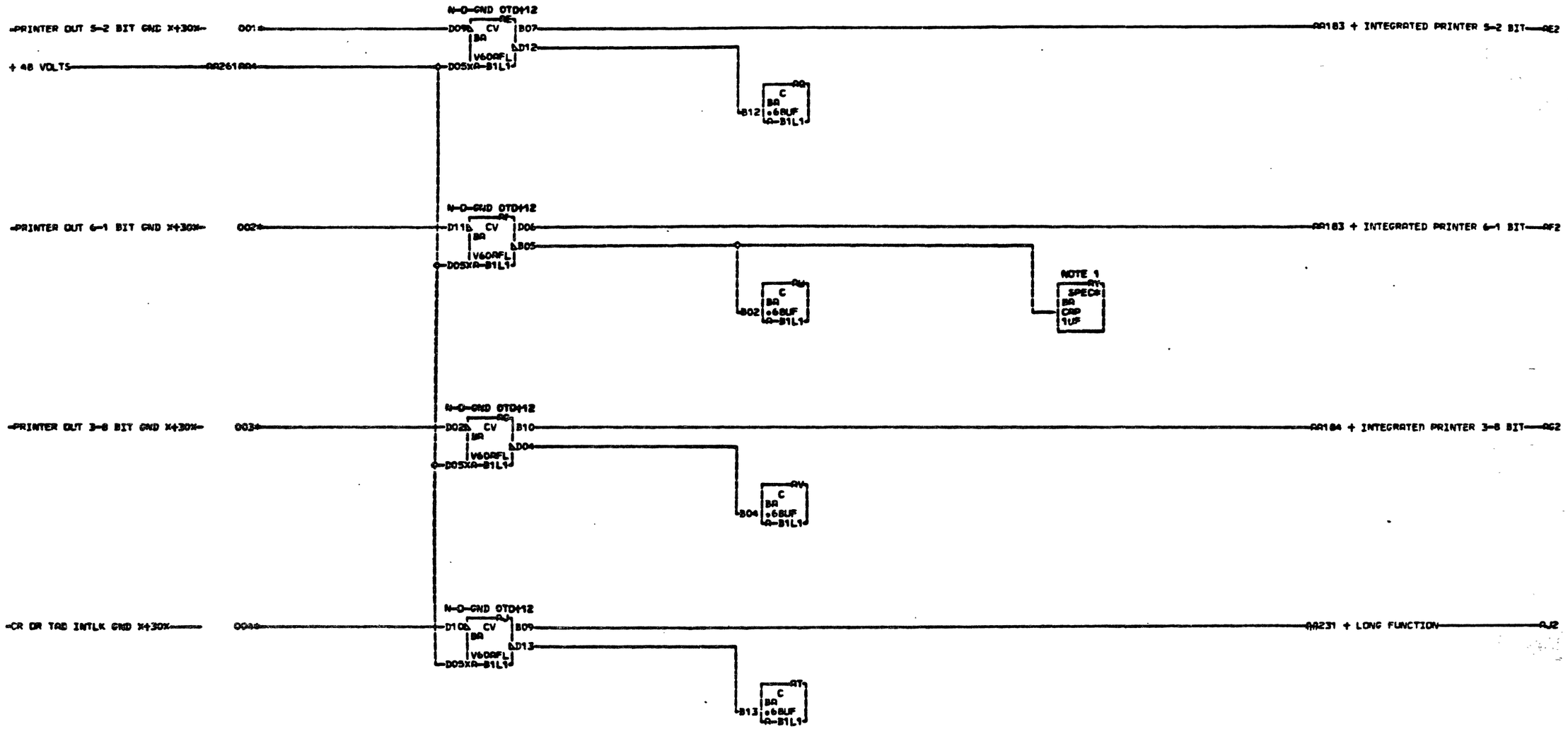
THE LOGIC ON SLT CARD
A P-N 5804377 IS EQUIVALENT
A TO THAT SHOWN ON THIS PAGE
1 INPUT AND OUTPUT PIN
4 FUNCTIONS ARE IDENTICAL
1

002
SIM TO PN 1176220 EC 307100

AH4 A-B1D1B05
BJ4 A-B1E1B10

LOC. TYPE
A-B1J6

I-O CYCLE AND OPERATE LATCHES P-N 5807365		
-E.C.-HISTORY-	MACH.2741A	A
	FRAME 01	A 1 4 1
DATE LAST EC	IBM CORP. SDD	
06-03-68 345323	P.No. 1277321	002



NOTE 1 BACK PANEL CAPACITOR MOUNTED BETWEEN PINS B1L1B09 (POS) AND B1L1D08 (NEG).

A 1 6 1 000

001 01A-B1A1B07
002 01A-B1A1D06
003 01A-B1A1B08
004 01A-B1A1D09

LOC. TYPE
A-B1L1

INTEGRATORS 1
P-N 5803567
E.C.-HISTORY: 307100
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FRAME 01
IBM CORP. LX
DATE 02-25-70
LAST EC 308739
P.N. 1176221

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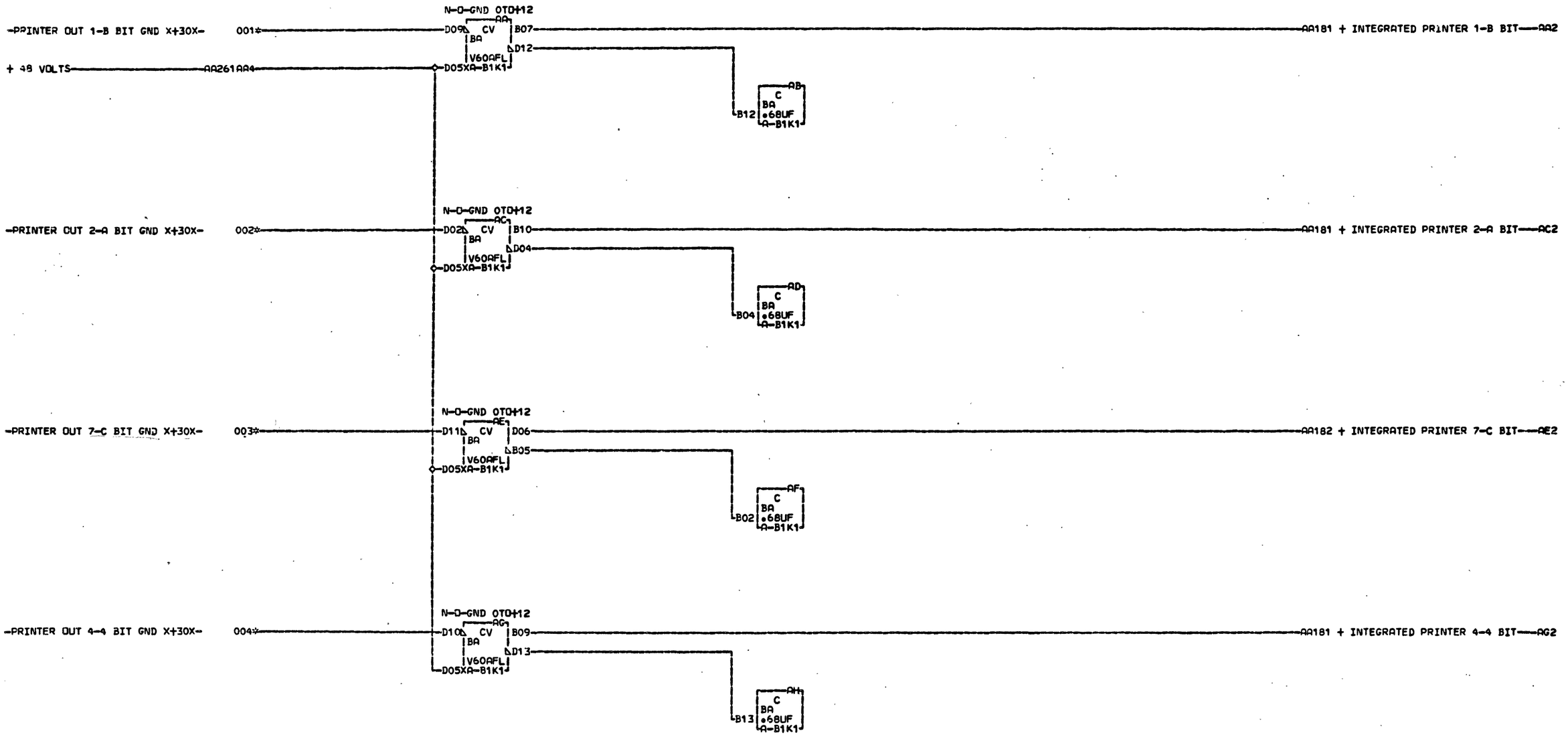

A
A
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001
01A-B1M1B09
002
01A-B1M1D09
003
01A-B1M1B05
004
01A-B1M1D07

LOC. TYPE
A-B1K1

INTEGRATORS 2
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-E.C.-HISTORY- MACH.2741A
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IBM CORP. LX
DATE LAST EC
02-21-68 307100
P.N. 1176248

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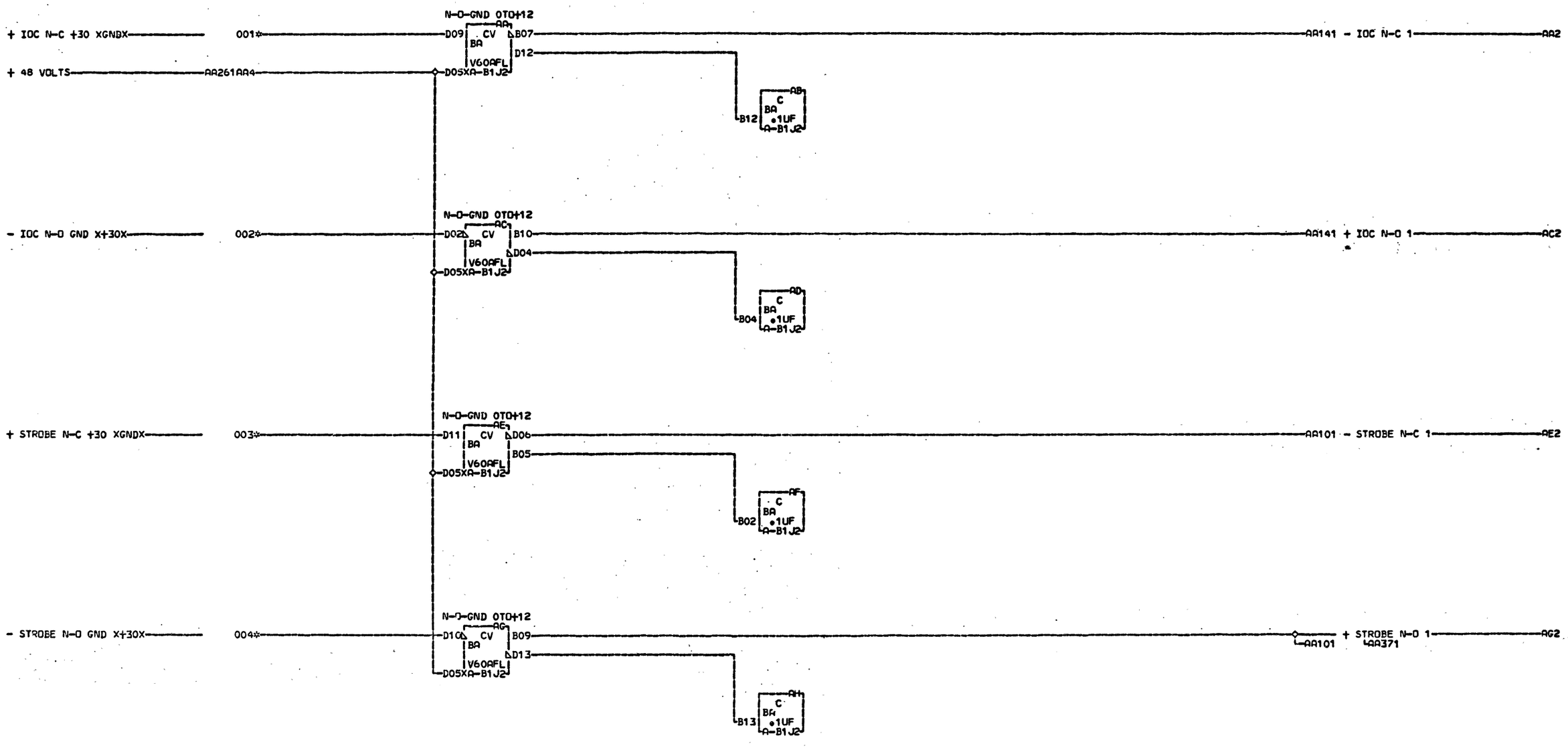

A
A
1
6
3

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001
01A-B1M1B10
002
01A-B1M1D10
003
01A-B1N1D02
004
01A-B1M1D11

LOC. TYPE
A-B1J2

INTEGRATORS 3
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E.C.-HISTORY
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DATE LAST EC
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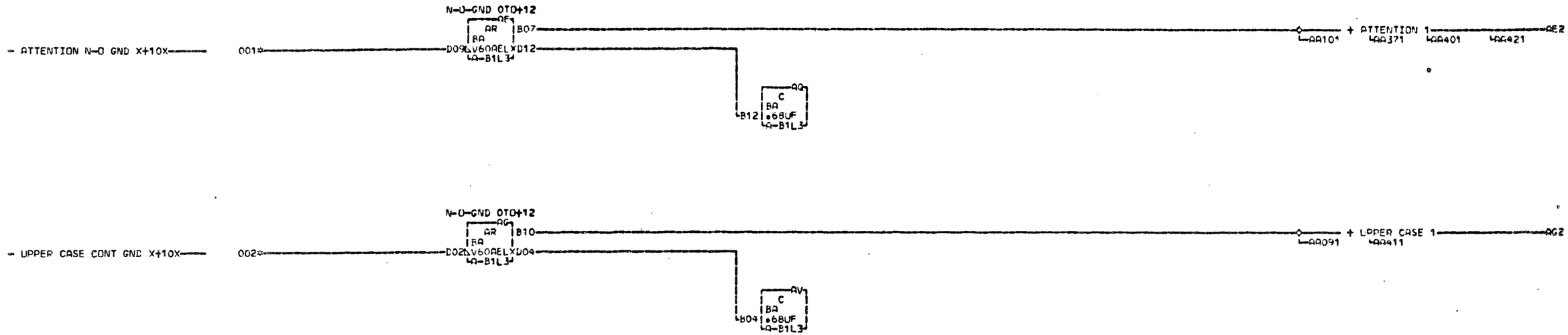

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001
01A-B1N1B07
002
01A-B1N1B04
003
01A-B1N1D06
004
01A-B1N1D04

LOC. TYPE
A-B1L3

INTEGRATORS 4
P-N 5803566
—E.C.—HISTORY— MACH.2741A
FRAME 01
IBM CORP. LX
DATE LAST EC
02-21-68 307100
P.No 1176222

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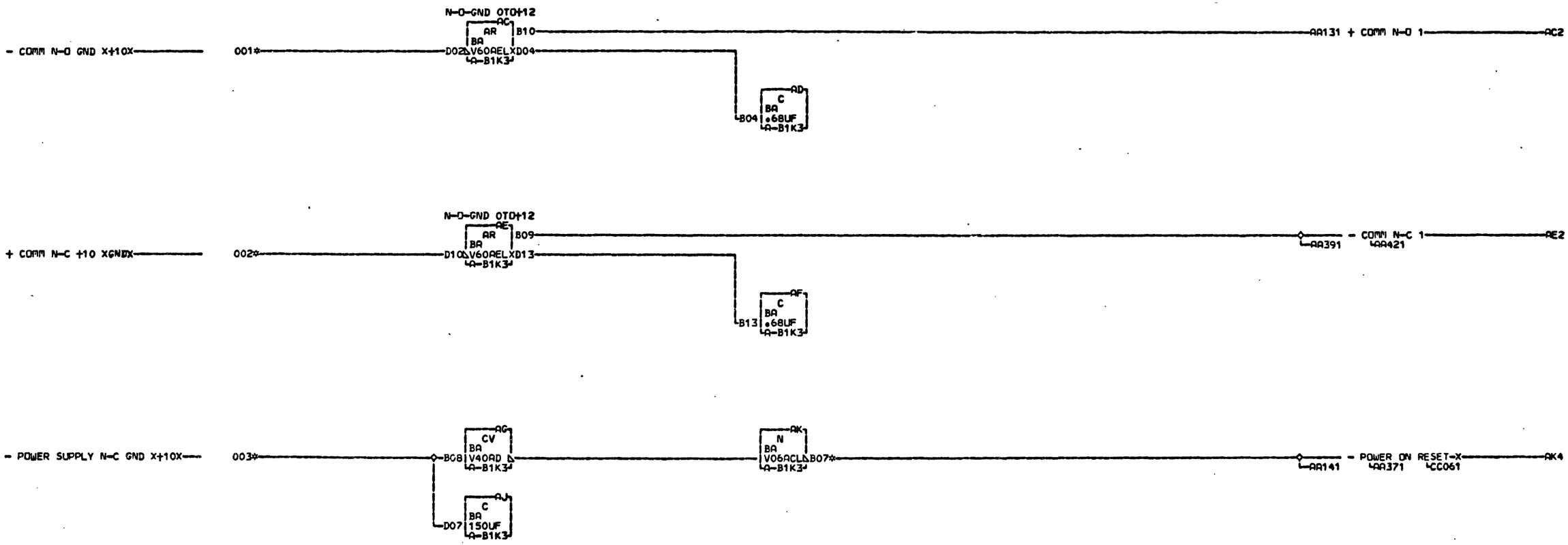

A A 1 7 2 000

001
01A-B1M1D13
002
01A-B1M1B13
003
01A-B1N2D04
AK4 A-B1N4B02

LOC. TYPE
A-B1K3

INTEGRATORS 5
P-N 5803852
E.C.-HISTORY
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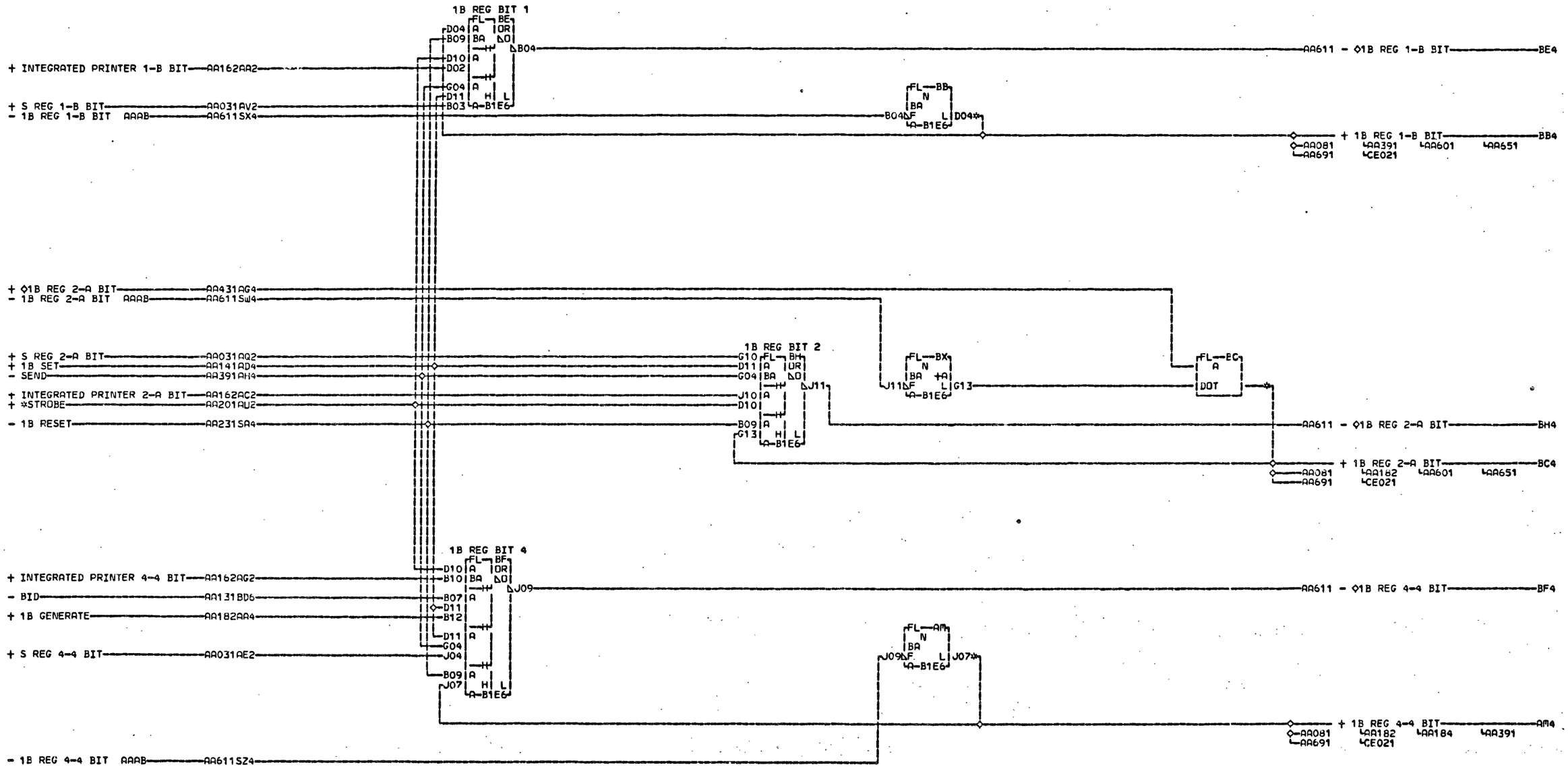
FRAME 01
IBM CORP. LX
DATE LAST EC
02-21-68 307100
P.N. 1176250

A A 1 7 2 000



AM4
01A-B1E1B03
BB4
01A-B1D1B04
BC4
01A-B1D1D04

LOC. TYPE
A-B1E6

002
SIM TO PN 1176223 EC 307100

1B REGISTER BITS-1-2-4
P-N 5804368
—E.C.-HISTORY— MACH.2741A
FRAME
IBM CORP. SDD
DATE LAST EC
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P.N. 1277322
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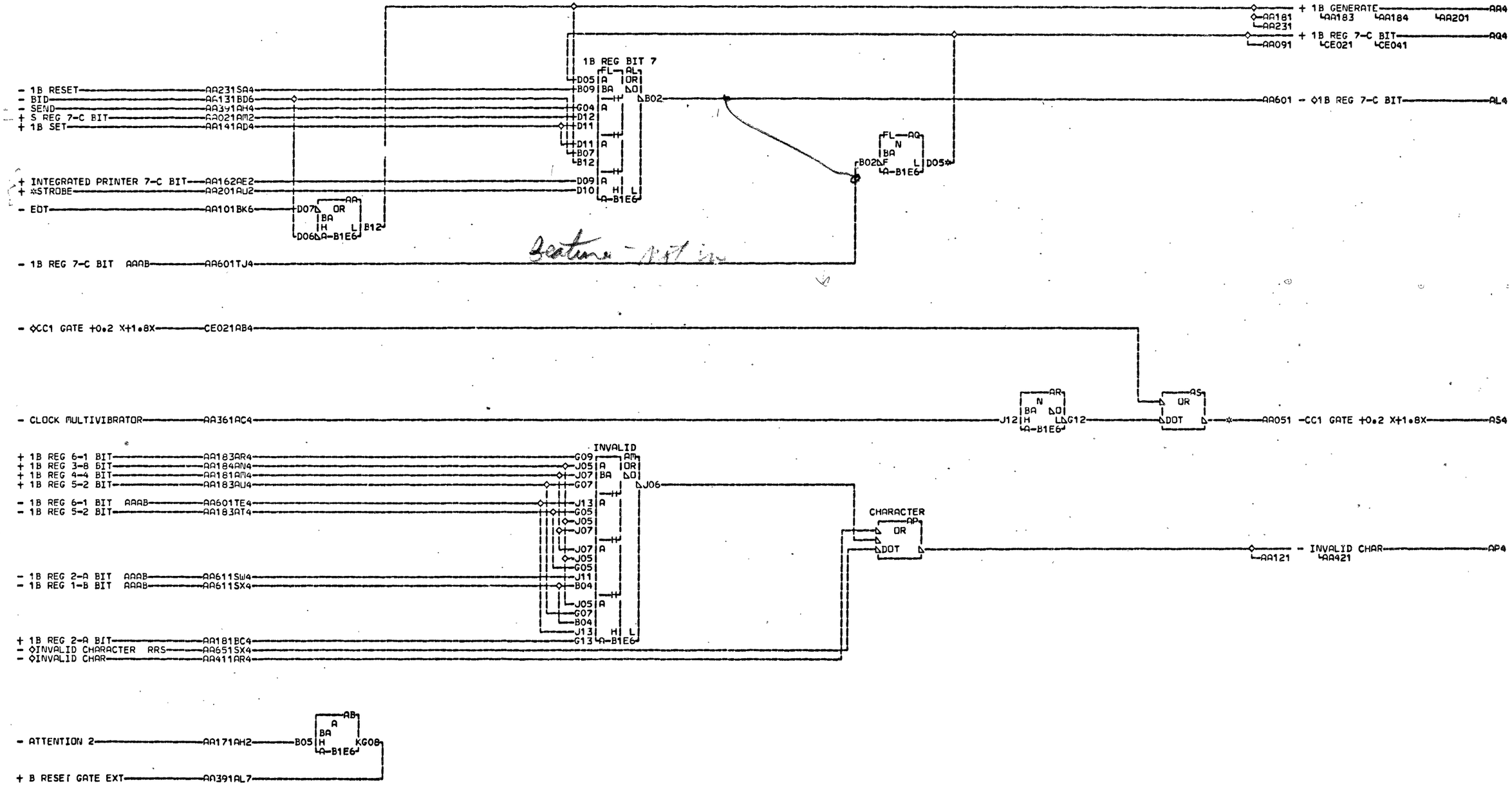

AQ4 A-B1D1B03
AS4 A-B1E1D10

LOC. TYPE
A-B1E6

1B REG BIT-7 AND INVALID CHAR.
P-N 5804368
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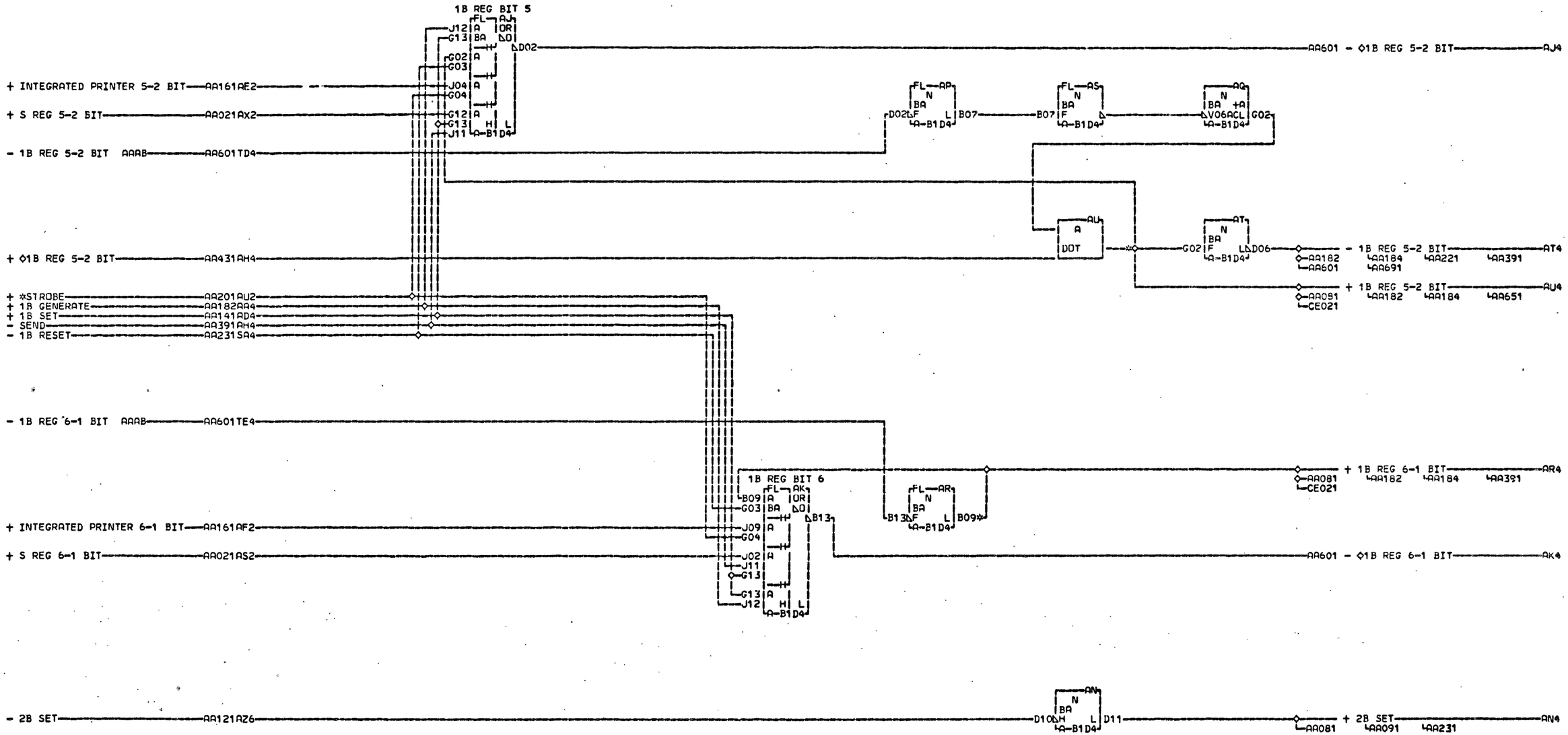
06-03-68 345323
P.N. 5166218

A AA182 002

002
SIM TO PN 5162287 EC 307100



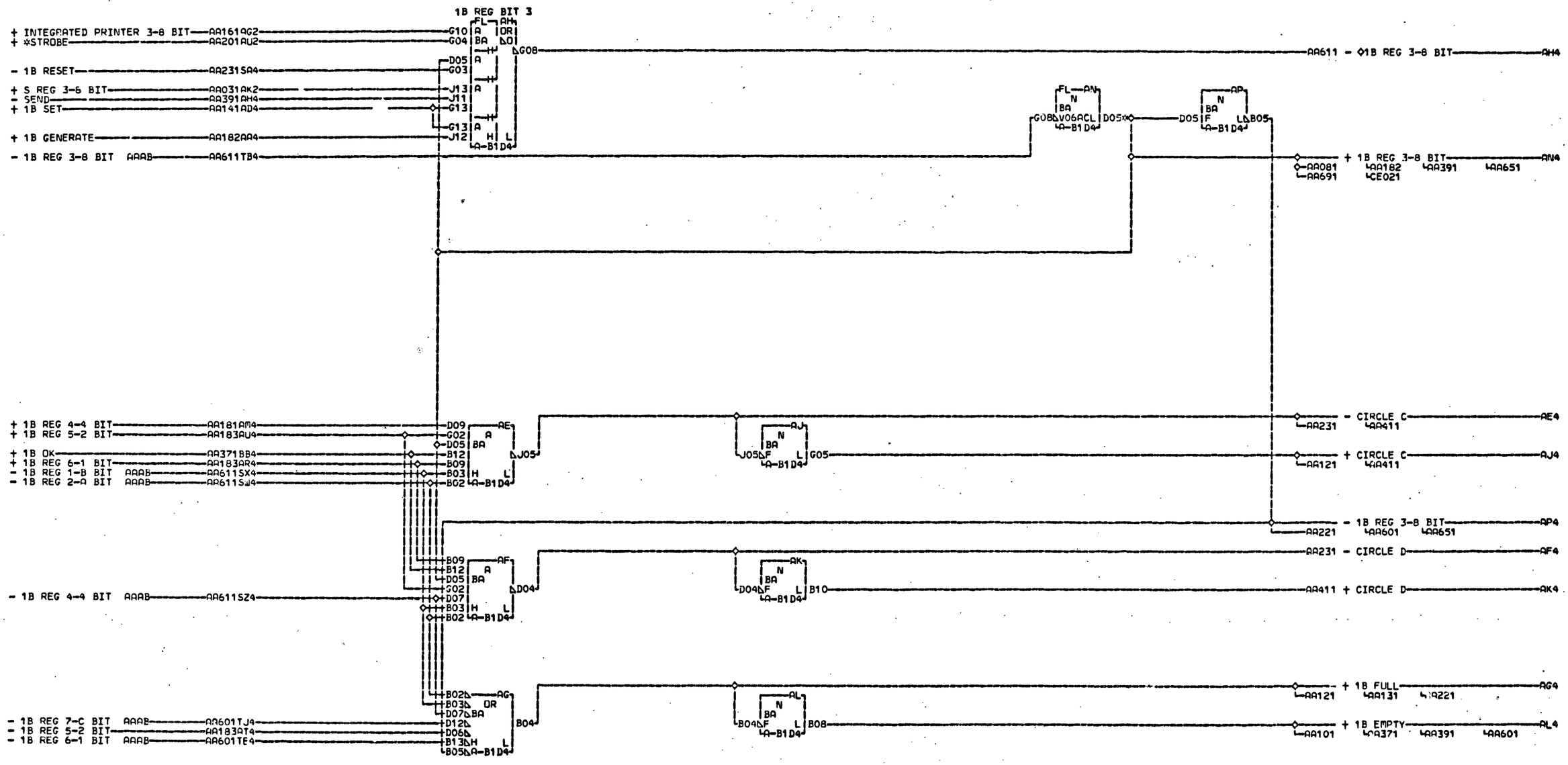
AR4 A-B1E1D02
AU4 A-B1E1D04

LOC. TYPE
A-B1D4

1B REGISTER BITS-5-6
P-N 5807374
E.C.-HISTORY
MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.N. 5166219

AA183 002

002 SIM TO PN 5162288 EC 307100



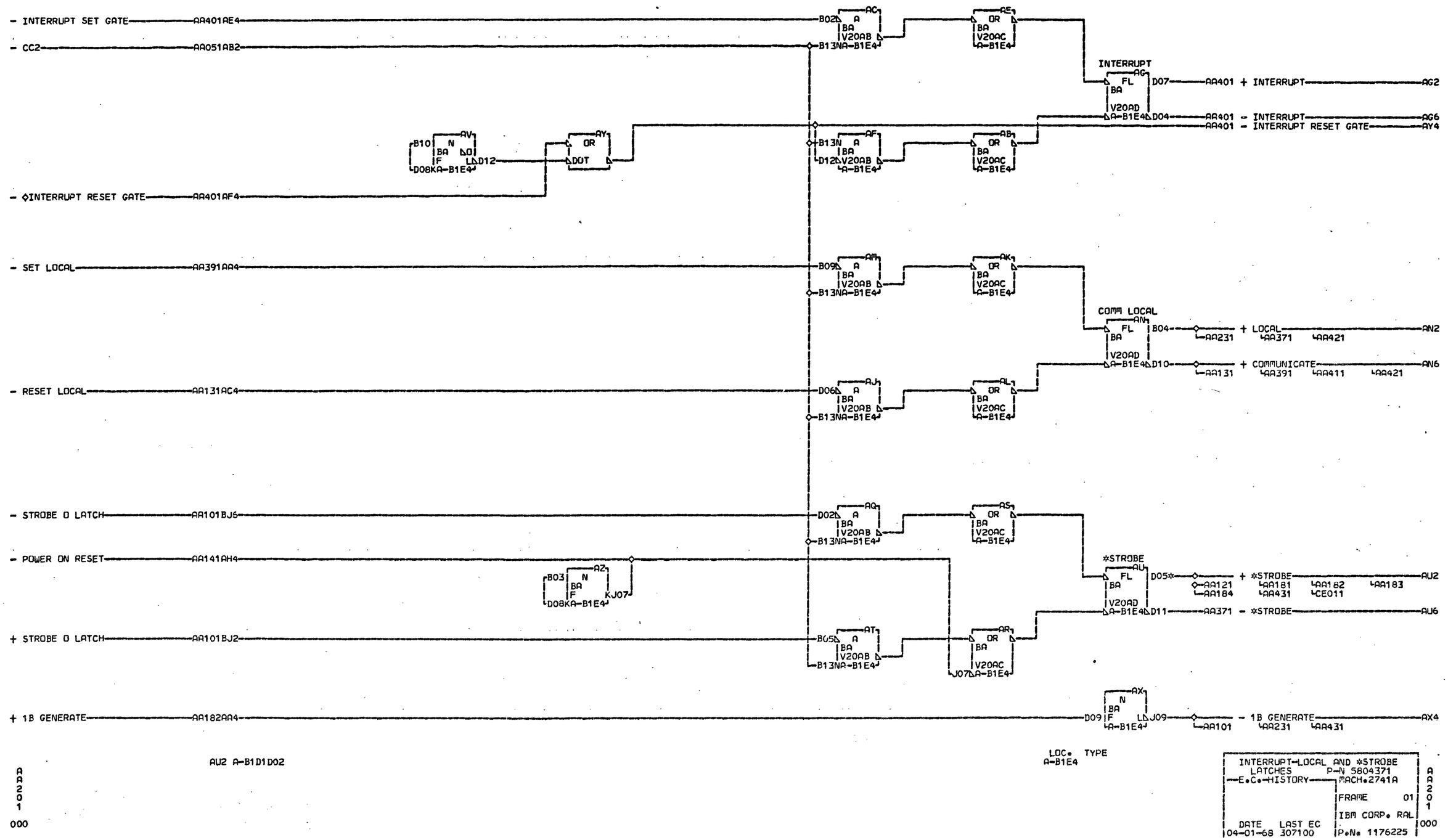
AN4 A-B1E1B04

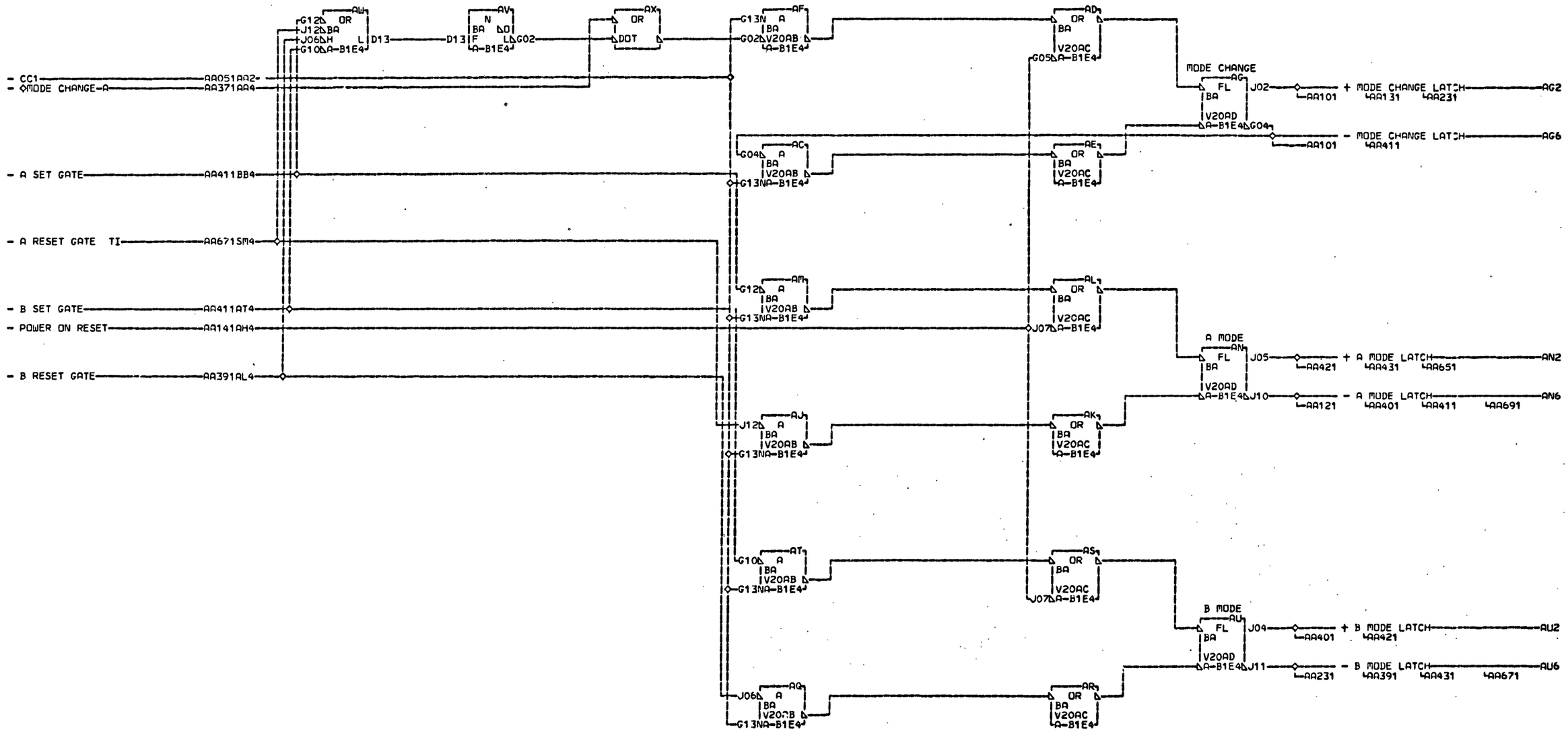
LOC. TYPE
A-B1D4

1B REG BIT-3 AND CIRCLE C-D DECODES P-N 5807374	A A 1 8 4
—E.C.—HISTORY— MACH.2741A	
FRAME 01	
IBM CORP. SDD	002
DATE LAST EC 06-03-68 345323	P.N. 1277323

A A 1 8 4

002
SIM TO PN 1176224 EC 307100


- INTERRUPT SET GATE
AA401AE4
- CC2
AA051AB2
- ◇INTERRUPT RESET GATE
AA401AF4
- SET LOCAL
AA391AA4
- RESET LOCAL
AA131AC4
- STROBE D LATCH
AA101BJ5
- POWER ON RESET
AA141AH4
+ STROBE D LATCH
AA101BJ2
+ 1B GENERATE
AA182AA4
AC
AE
AV
AY
AF
AB
AM
AK
AJ
AL
AQ
AS
AZ
AT
AR
AX
INTERRUPT
AG
FL
D07
AA401 + INTERRUPT
AG2
D04
AA401 - INTERRUPT
AG6
AA401 - INTERRUPT RESET GATE
AY4
COMM LOCAL
AN
B04
+ LOCAL
AN2
AA231
AA371
AA421
D10
+ COMMUNICATE
AN6
AA131
AA391
AA411
AA421
*STROBE
AU
D05*
+ *STROBE
AU2
AA121
AA181
AA182
AA183
AA184
AA431
CE011
D11
AA371 - *STROBE
AU6
D09
J09
- 1B GENERATE
AX4
AA101
AA231
AA431
AU2 A-B1D1D02
LOC. TYPE
A-B1E4
INTERRUPT-LOCAL AND *STROBE LATCHES
P-N 5804371
E.C.-HISTORY
MACH.2741A
FRAME 01
IBM CORP. RAL
DATE LAST EC
04-01-68 307100
P.N. 1176225
AA201
000



LOC. TYPE
A-B1E4

A-B AND MODE CHANGE LATCHES
P-N 5804371
E.C.-HISTORY
MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.No 1277324

AA211 002

002
SIM TO PN 1176226 EC 307100

- S REG 1-B BIT — AA031AV6 — D13 — AX
- S REG 2-A BIT — AA031AQ6 — D12 — A
- S REG 3-8 BIT — AA031AK6 — D11 — BA
- S REG 4-4 BIT — AA031AE6 — B10 — J04
- S REG 5-2 BIT — AA021AX6 — B13
- S REG 6-1 BIT — AA021AS6 — B12
- S REG 7-C BIT — AA021AM6 — G03
- S REG 8-STOP BIT — AA021AG6 — G04 — H L
+ SD3 — AA061AU2 — G08 — A-B1G4

AA131 - S REG EMPTY SET GATE — AX4

- 1B REG 6-1 BIT AAAB — AA601TE4 — J11 — AJ — A — BA — H — LA J10 — J09 A-B1G4

AA021 - S REG 6 RESET — AJ4

- 1B REG 7-C BIT AAAB — AA601TJ4 — J13 — AH — A — BA — H — LA G13 — J09 A-B1G4

AA021 - S REG 7 RESET — AH4

- 1B REG 5-2 BIT — AA183AT4 — G12 — AK — A — BA — H — LA G10 — J09 A-B1G4

AA021 - S REG 5 RESET — AK4

+ 1B FULL — AA184AG4 — B07 — AV — A — BA — H — LA D06
+ ENTER SERDES — AA101BH2 — D09
- C2 — AA071AQ4 — D10
+ SEND — AA411AQ4 — B09 — A-B1G4

D06 — AY — N — BA — F L — A-B1G4 — J09

AA031 - S REG 0 RESET — AV4

- 1B REG 4-4 BIT AAAB — AA611SZ4 — J12 — AL — A — BA — H — LA G09 — J09 A-B1G4

AA03* - S REG 4 RESET — AL4

- 1B REG 3-8 BIT — AA184AP4 — G05 — AM — A — BA — H — LA G02 — J09 A-B1G4

AA031 - S REG 3 RESET — AM4

- 1B REG 2-A BIT AAAB — AA611SW4 — G07 — AN — A — BA — H — LA J07 — J09 A-B1G4

AA031 - S REG 2 RESET — AN4

- 1B REG 1-B BIT AAAB — AA611SX4 — J05 — AP — A — BA — H — LA J06 — J09 A-B1G4

AA031 - S REG 1 RESET — AP4

+ PRINT INHIBIT LATCH — AA691SP4

GROUND — 001 — J02 — SA — N — BA — V05AF — J08 A-B1G4 — B08 — B08 — D07 — SB — A — BA — H — A-B1G4

45 MS — SC — SS * — BA — C3K D02 — V21AT B02 — A-B1G4 — B04 — B04 — SD — N — BA — H — LA D04 — A-B1G4

AA251 -◇TO NON PRINT MD PRI +0.2 +.7-SD4

LOC. TYPE
A-B1G4

S REGISTER RESET LINES
P-N 5804375
E.C.-HISTORY — MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.N. 1277325

AA221 002

002 SIM TO PN 1176227 EC 307100

002 AA231

+ ◇1B OK — AA371 — BD4
- *2B SET — AA131 — AA141 — AA391 — AA421 — AY4

- ◇1B RESET RRS — AA651 SK4
+ MODE CHANGE LATCH — AA211 AG2
+ *2B SET — AA121 AZ2
+ *C1 — AA071 AK2
- SEND — AA391 AH4
+ C2 — AA071 BC4
- S REG 0-START BIT — AA031 BA6
- C2 — AA071 AQ4
+ 2B SET — AA183 AN4
+ 1B GENERATE — AA182 AA4
- CIRCLE D — AA184 AF4
+ ENTER SERDES — AA101 BH2
- C1 — AA071 AY4
+ 2B RESET LATCH — AA121 BE2
+ SEND — AA411 AQ4
- B MODE LATCH — AA211 AU6
- 1B GENERATE — AA201 AX4

- CIRCLE C — AA184 AE4

+ LONG FUNCTION — AA161 AJ2
+ LOCAL — AA201 AN2
+ CLEAR TO SEND — AA351 AM4

- 1B RESET — AA181 — AA182 — AA183 — AA184 — SA4

AA014 - TO KBD LOCK MD +0.2 X+0.7X — AV4

AA121 - 2B SET RESET GATE — AN4

AA601 - KYBD LOCK EXT — AS7

AA071 - C1 GATE — AZ4

AA231
1
002
SIM TO PN 1176228 EC 307100

LOC. TYPE
A-B1D6

KEYBOARD LOCK-1B AND 2B REGISTER LINES P-N 5804376
E.C.-HISTORY — MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.N. 1277326

AA231
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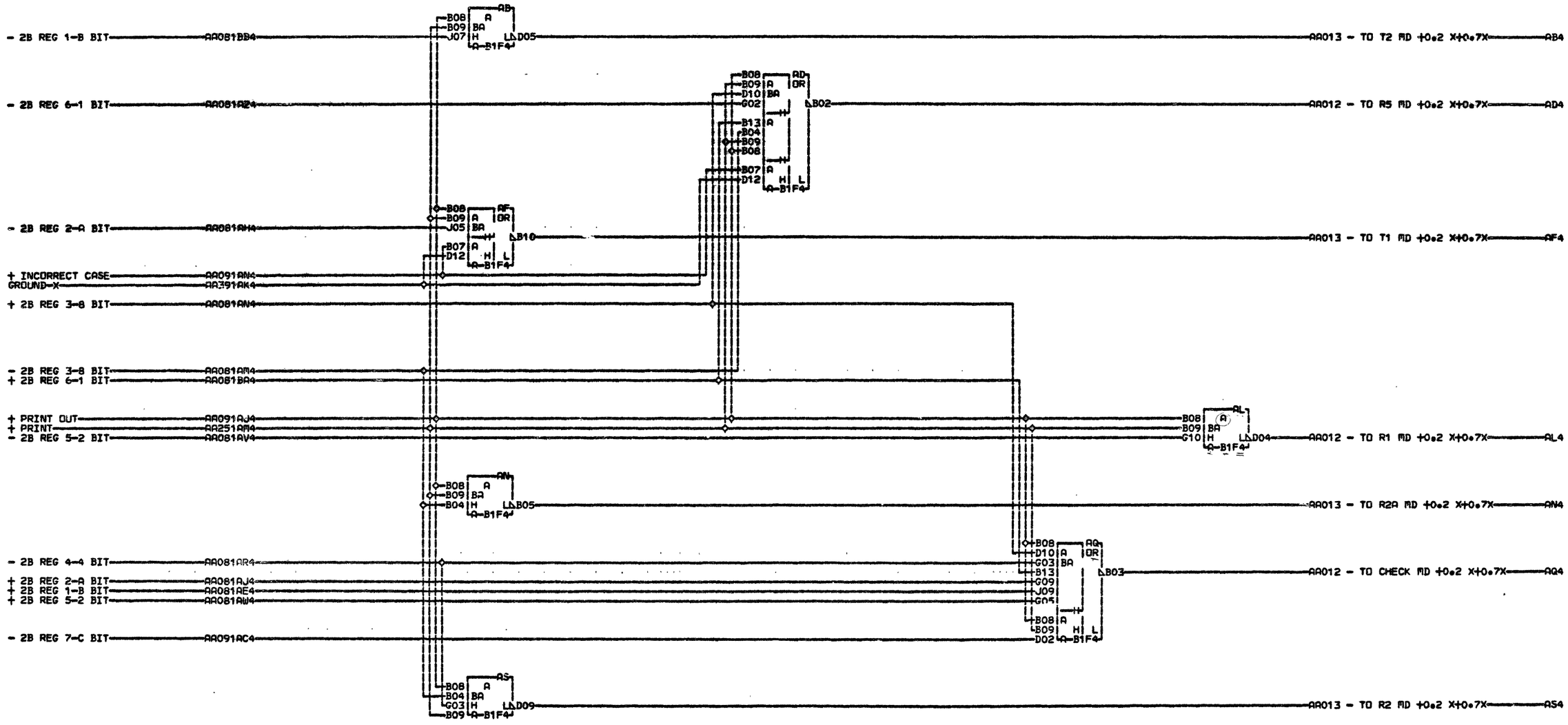
002

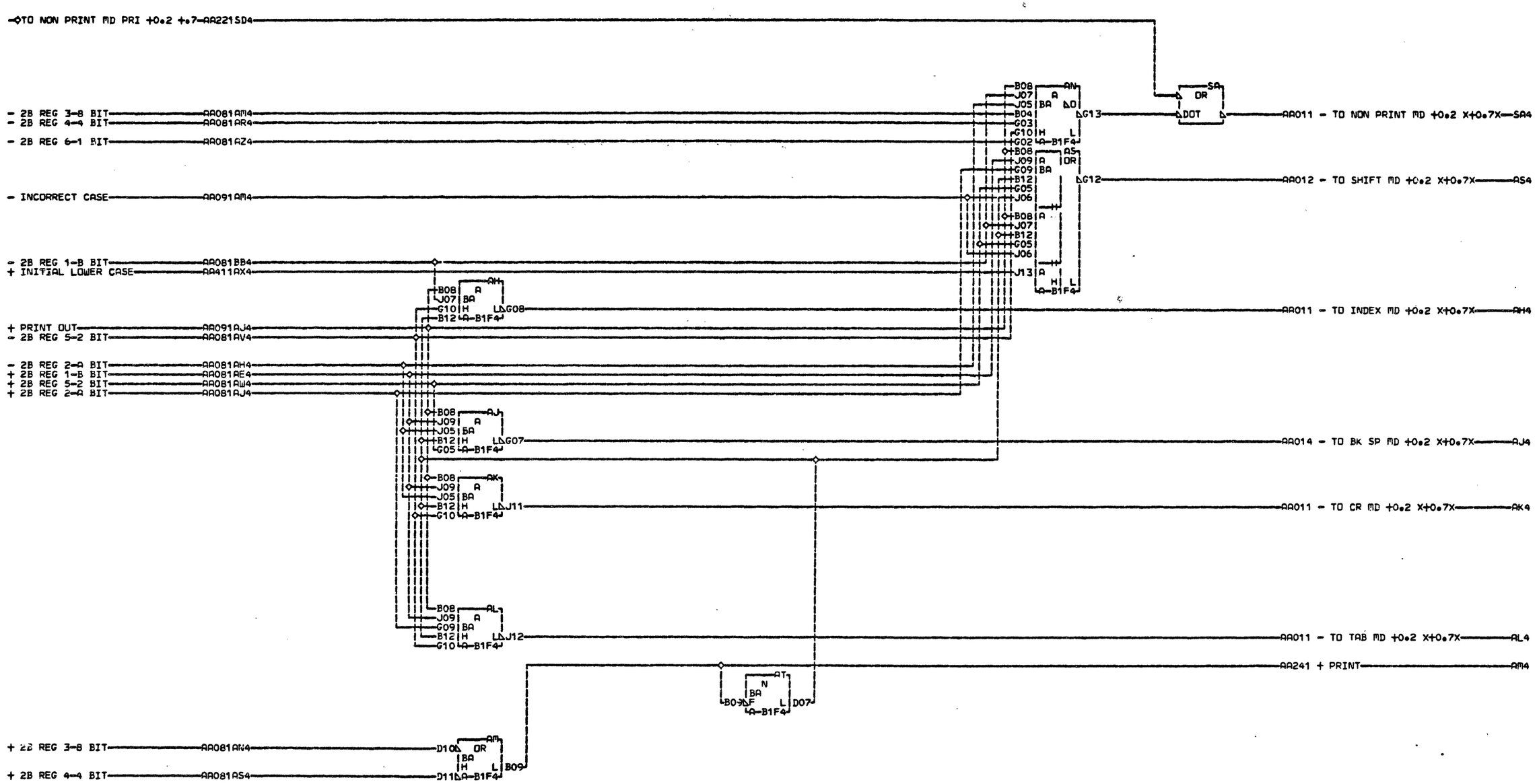


LOC. TYPE
A-B1F4

OUTPUT DECODE-DOMESTIC P-N 5800441	
E.C. HISTORY	MACH. 2741A
	FRAME 01
	IBM CORP. SDD
DATE LAST EC	P.N. 1277327
06-03-68 345323	

AA241 002

002
SIM TO PN 1176229 EC 307100

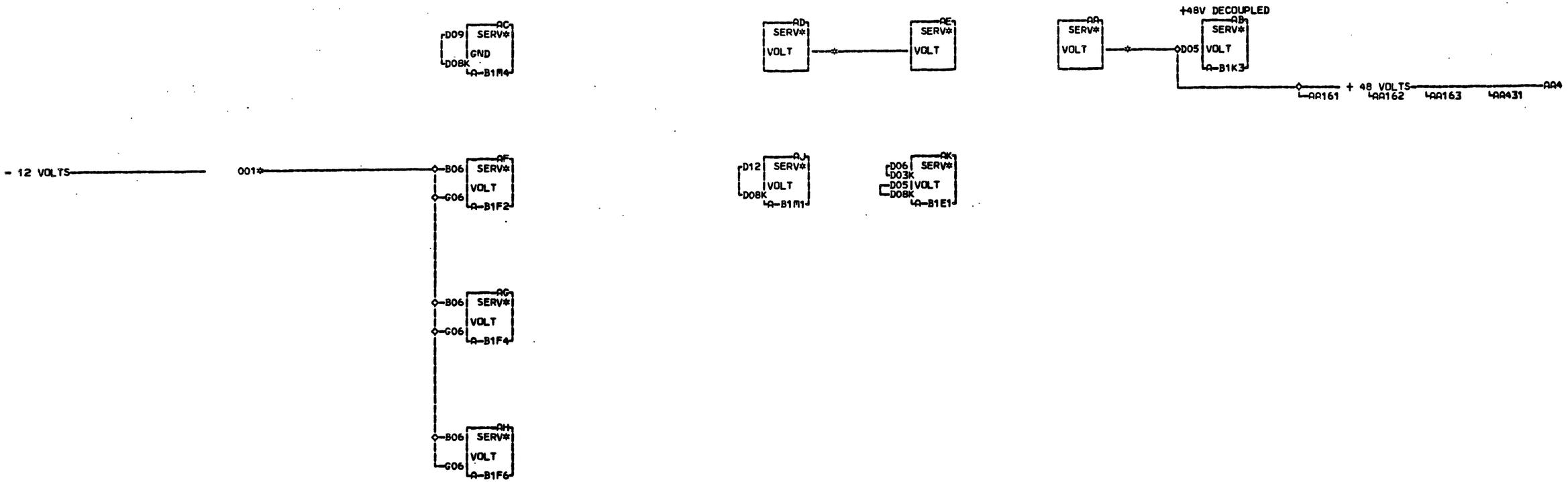


LOC. TYPE
A-B1F4

OUTPUT DECODE-DOMESTIC
P-N 5804441
E.C. HISTORY
MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.N. 1277328

AA251 002

002
SIM TO PN 1176230 EC 307100



001
01A-B1N2B05
AA4 A-B1N2D02
AD4 A-B1M4B03
C1A-B1M4D04

SERV BLOCKS

E.C. HISTORY

MACH. 2741A

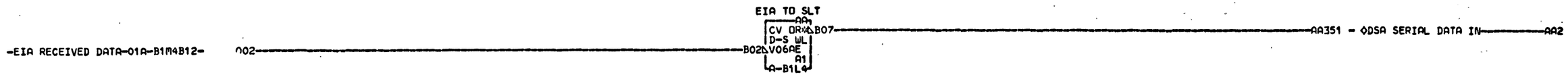
FRAME 01

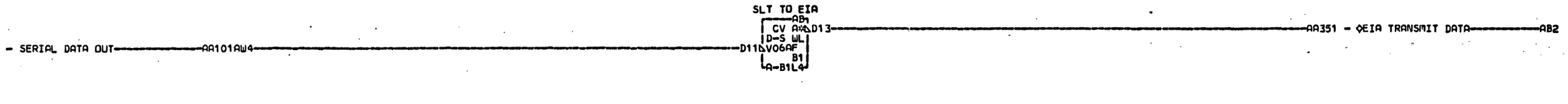
IBM CORP. LX

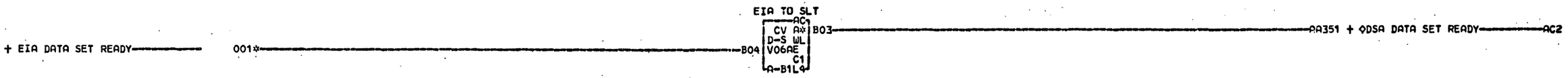
DATE LAST EC
11-03-67 307100

P.N. 1176252

AA261 000





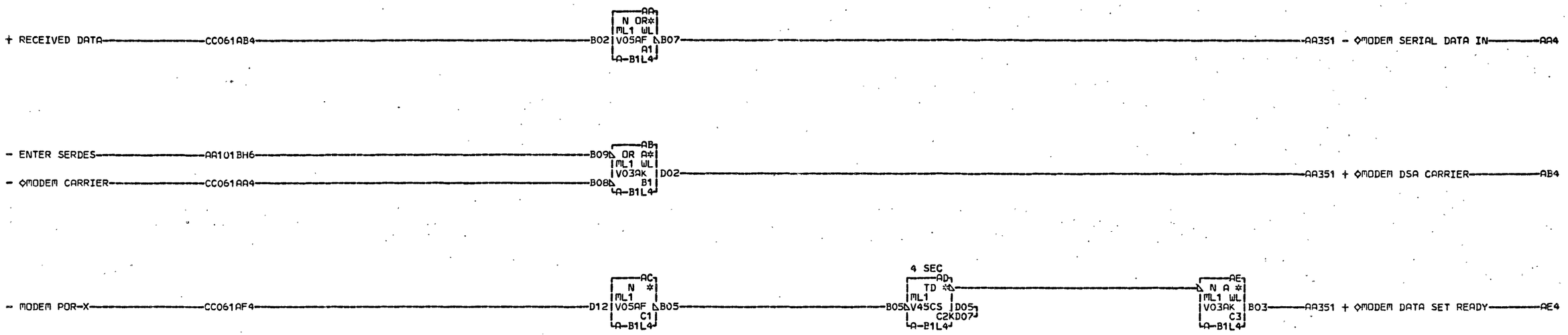


THIS CARD P-N 5803561 IS AN
OVERLAY CARD SEE PAGES AA282 001
A AND AA283 01A-B1M4D13
A SEE ALSO PAGES AA351 AND AA352 01A-B1L4B04
2
8
1

000

COMMON DATA SET ADAPTER
P-N 5803561
E.C. HISTORY — MACH. 2741A
FRAME 01
IBM CORP. LX
DATE LAST EC
02-26-68 307100
P.N. 1176231

A A 2 8 1 000



THIS CARD P-N 5803854 IS AN
OVERLAY CARD SEE PAGES AA281
AND AA283
SEE ALSO PAGES AA351 AND AA352

AA282

000

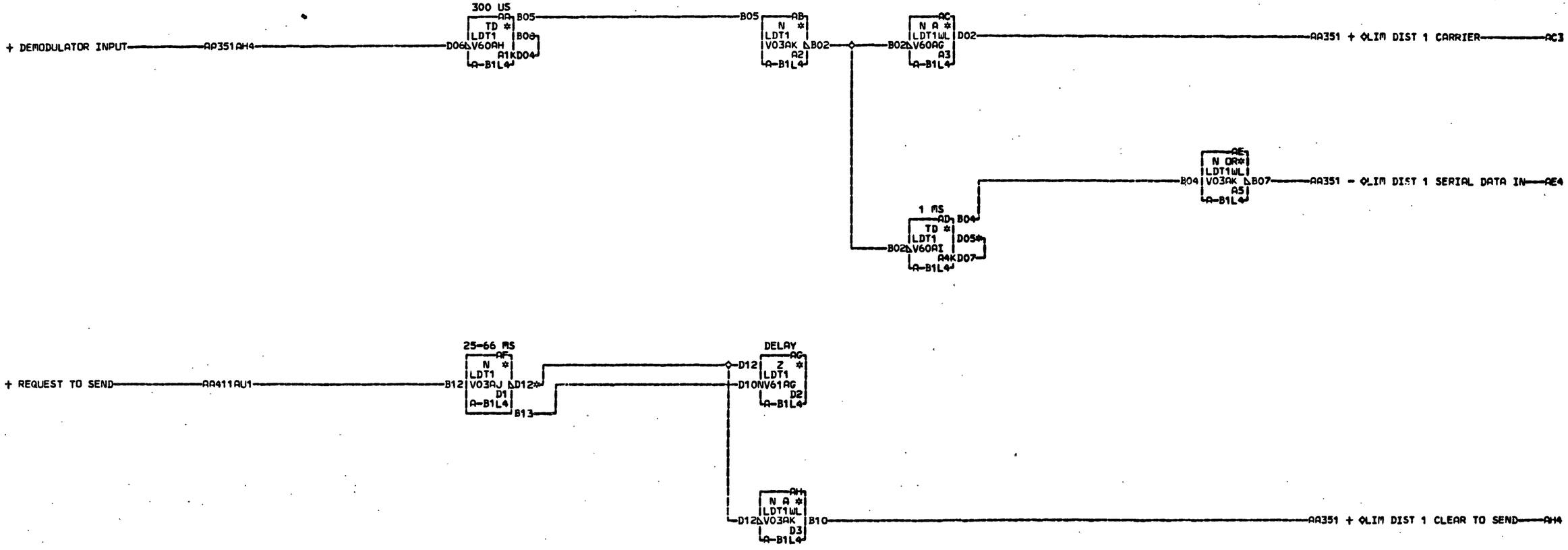
MODEM DATA SET ADAPTER
P-N 5803854
E.C. HISTORY — MACH 2741A

DATE	LAST EC
02-26-68	307100

FRAME 01
IBM CORP. LX
P.N. 1176232

AA282

000



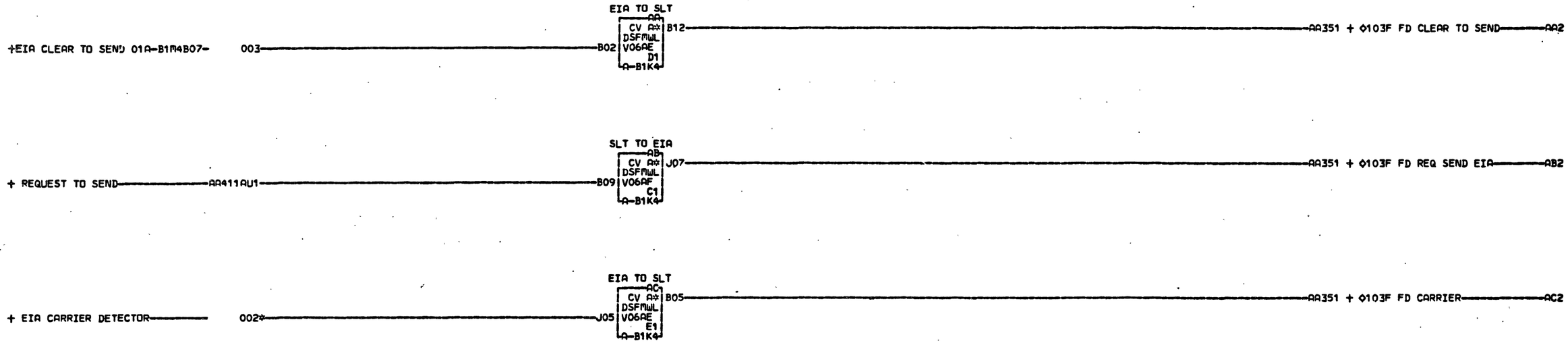
THIS CARD P-N 5803850 IS AN
OVERLAY CARD SEE PAGES AA281 AND AA282
A SEE ALSO PAGES AA351 AND AA352

AD3 A-B1L4D05
01A-B1L4D07
AF4 A-B1N4B03
01A-C1B5B03
01A-C1B5B02
01A-B1L4D12

000

LIMITED DISTANCE 1 ADAPTER
2W-HD OR 4W-FD P-N 5803850
—E.C.-HISTORY— MACH.2741A
FRAME 01
IBM CORP. LX
DATE LAST EC
02-26-68 307100
P.N. 1186487

A A 2 8 3 000



THIS CARD P-N 5801315 IS AN OVERLAY CARD SEE PAGES 002

A AA343 AA344 AA345 AND AA346 01A-B1M4B09

A SEE ALSO PAGES AA351 AND AA352 01A-B1K4J05

3

4

1

000

103F OR 3976-1 FD DATA SET ADAPTER P-N 5801315

E.C.-HISTORY MACH.2741A

FRAME 01

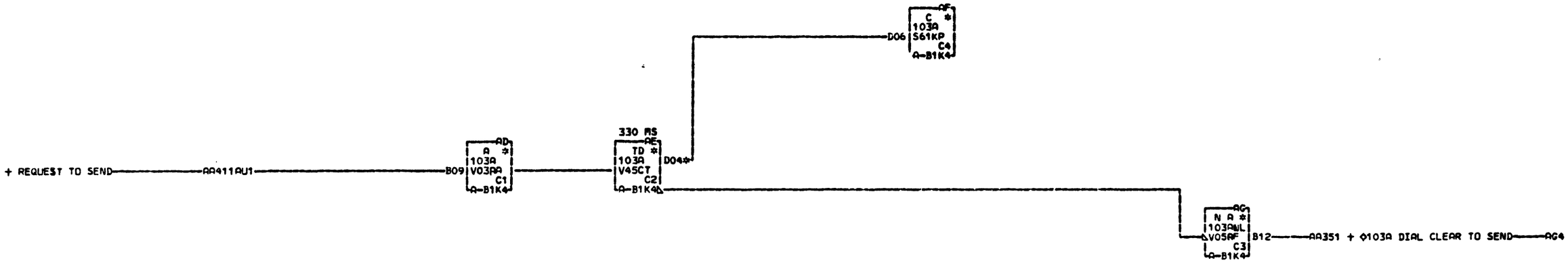
IBM CORP. LX

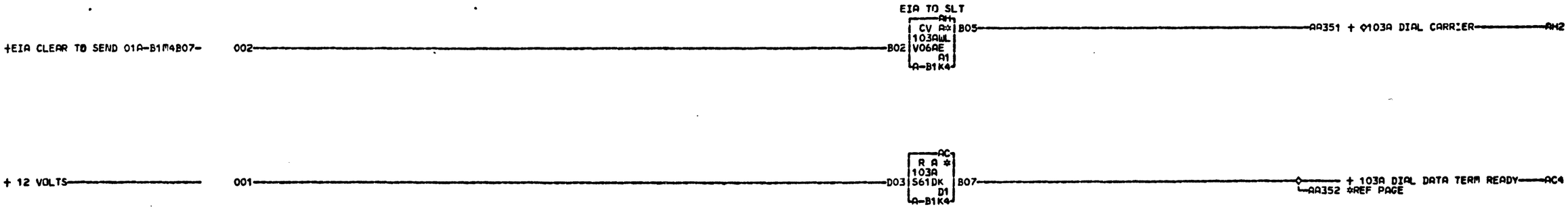
DATE LAST EC

02-26-68 307100

P.N. 1176233

A A 3 4 1 000



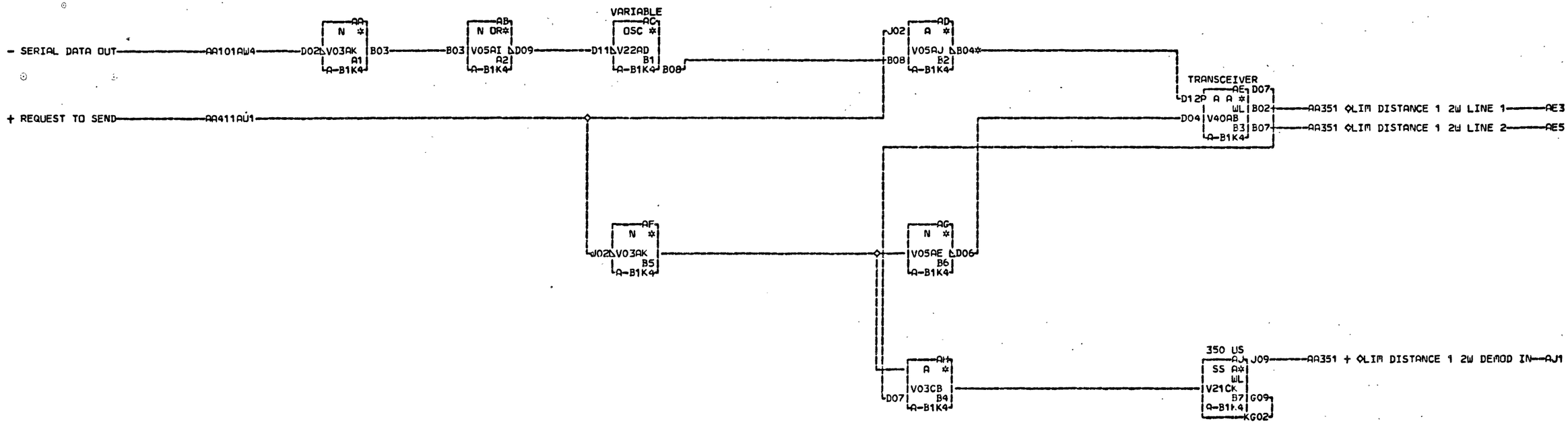


THIS CARD P-N 5803855 IS AN
OVERLAY CARD SEE PAGES AA341 AE3 A-B1K4D04
A AA344 AA345 AND AA346 01A-B1K4D06
A SEE ALSO PAGES AA351 AND AA352
3
4
3

000

103A DIAL DATA SET ADAPTER
P-N 5803855

E.C.-HISTORY | MACH.2741A | A
| | A
| FRAME 01 | 3
| | 4
| IBM CORP. LX | 3
DATE LAST EC | P.No. 1186488 | 000
02-26-68 307100 |

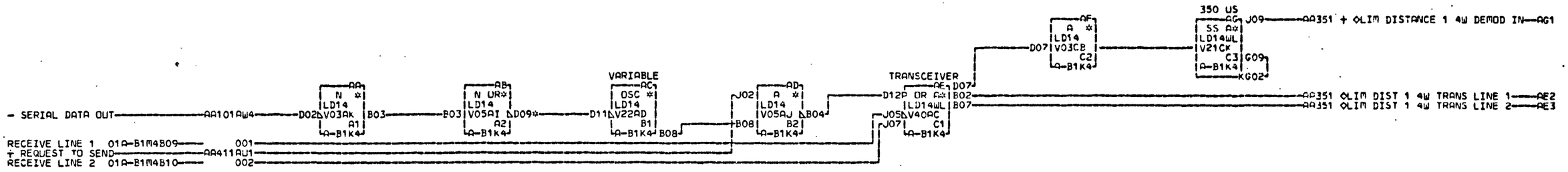


THIS CARD P-N 5806001 IS AN
OVERLAY CAPD SEE PAGES AA341 AD4 A-B1K4B04
A AA343 AA345 AND AA346 01A-B1K4D12
A SEE ALSO PAGES AA351 AND AA352
3
4
4

000

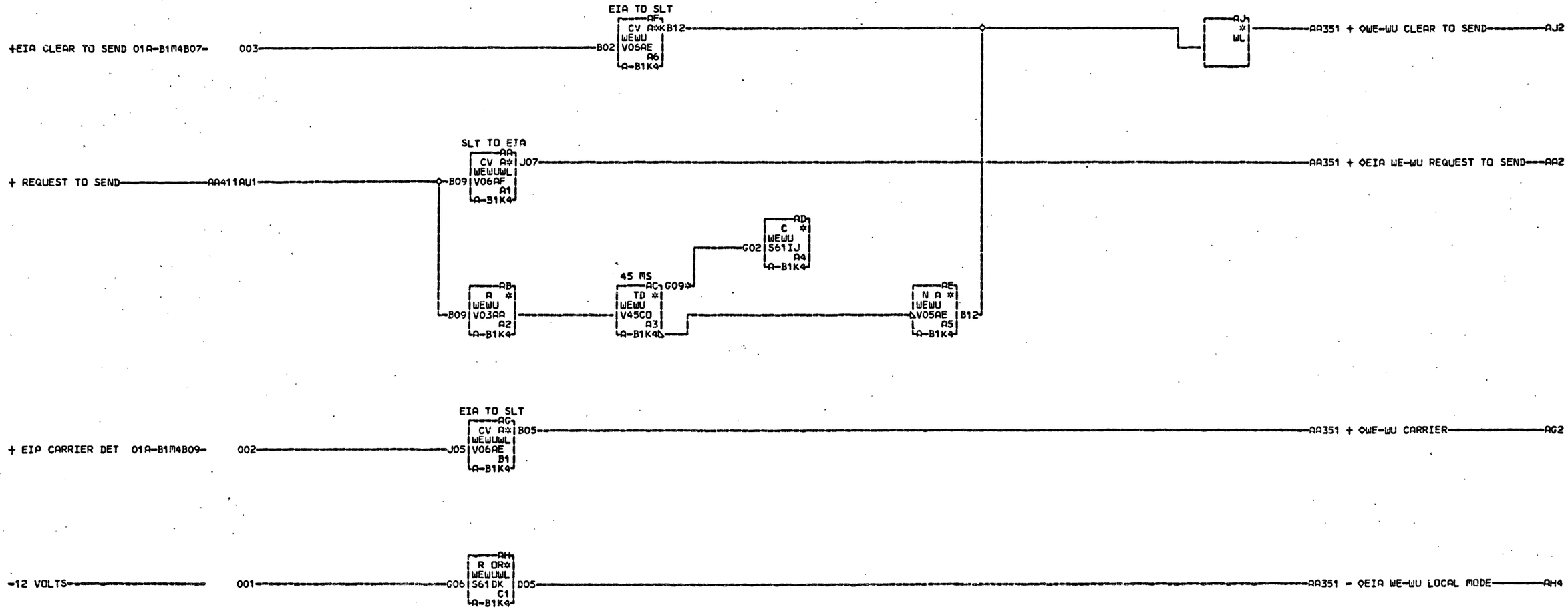
LIMITED DISTANCE 1 2W
P-N 5806001
E.C. HISTORY | MACH. 2741A
FRAME 01
IBM CORP. LX
DATE LAST EC
02-21-68 307100
P.N. 1186489

A A 3 4 4 000



THIS CARD P-N 5806002 IS AN
OVERLAY CARD SEE PAGES AA341 AB4 A-F1M4D10
AA343 AA344 AND AA346 01A-E1K4D11
SEE ALSO PAGES AA351 AND AA352 01A-B1K4D09

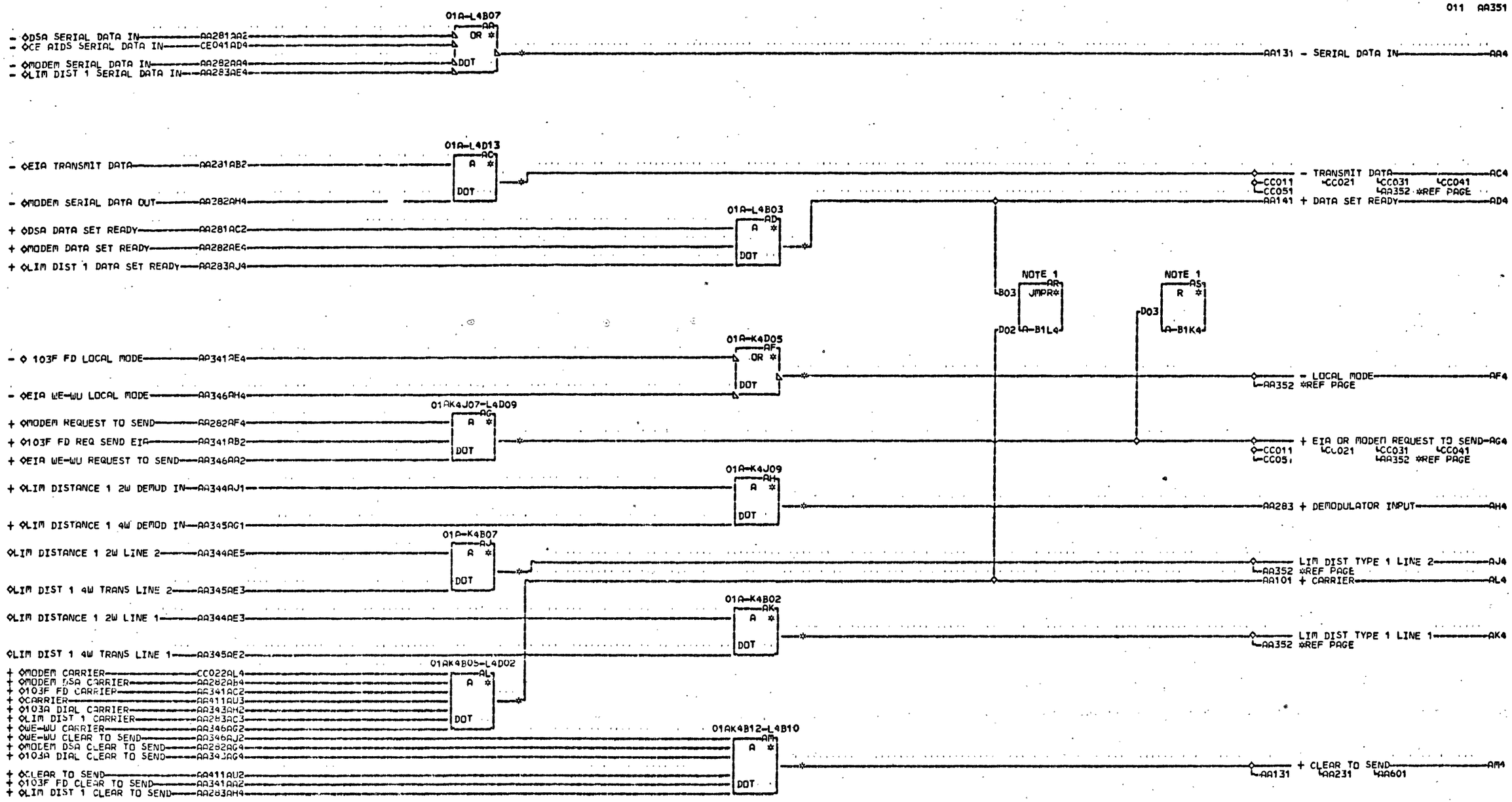
LIMITED DISTANCE 1 4W P-N 5806002	
E.C. HISTORY	MACH. 2741A
	FRAME 01
DATE LAST EC 02-26-68 307100	IBM CORP. LX P.N. 1186490



THIS CARD P-N 5801278 IS AN
OVERLAY CARD SEE PAGES AA341 AC1 A-B1K4G09
A AA343 AA344 AND AA345 01A-B1K4G02
A SEE ALSO PAGES AA351 AND AA352
3
4
6

000

WE-WU DATA SET ADAPTER
P-N 5801278
E.C.-HISTORY | MACH.2741A | A
A
3
4
6
FRAME 01
IBM CORP. LX
DATE LAST EC
02-21-68 307100
P.N. 1186491 | 000



NOTE 1 BACKPANEL
JUMPER FROM L4B03
A TO L4D02 AND BACKPANEL
A RESISTOR FROM L4D09
3 TO K4D03 INSTALLED
5 FOR 103A AND 113A
1 ONLY.

011
SIM TO PN 1176234 EC 307100

AA4 A-B1E1B12	01A-E1K4D05	01A-B1L4D06	01A-B1L4D02	
01A-B1L4B07	AG4 A-B1M4B10	AJ4 A-B1M4B08	01A-B1K4B05	
AC4 A-B1M4B13	01A-B1N4B07	01A-B1M4D05	AM4 A-B1L4B10	
01A-B1N4B10	01A-C1B5B07	01A-B1K4B07	01A-B1K4B12	
01A-C1B5B10	01A-C1E4D06	AK4 A-B1M4B07		
01A-C1E4J12	01A-C1D6D06	01A-B1M4B04		
01A-B1L4D13	01A-B1L4D09	01A-B1K4B02		
AD4 A-B1L4B03	01A-B1K4J07	AL4 A-B1N4D02		
AF4 A-B1M4D12	AH4 A-B1K4J09	01A-C1B5D02		

OVERLAY DOT BLOCKS
SOCKETS A-B1L4 AND A-B1K4
--E.C.--HISTORY-- MACH.2741A

DATE	LAST EC
05-27-70	308747

FRAME 01
IBM CORP. LX
P.N. 5994677

A A 3 5 1 C11

DATA SET AND MODEM SIGNALS

COMMON CARRIER DATA SET CABLE

TERMINAL					DATA SET		
NET NUMBER	REF TO PAGE	SLT CONN	TERM LINE NAME	FLOW	DATA SET LINE NAME	EIA DESIG	EIA PIN NO
AA351AC4	AA351	BIM4B13	- TRANSMIT DATA	→	TRANSMITTED DATA	BA	2
002	AA281	BIM4B12	-- EIA RECFIVED DATA	←	RECEIVED DATA	BB	3
AA351AG4	AA351	BIM4B10	+EIA OR MODEM REQUEST TO SEND	→	REQUEST TO SEND	CA	4
003	AA341 AA343 AA346	BIM4B07	+ EIA CLEAR TO SEND	←	CLEAR TO SEND	CB	5
001	AA281	BIM4D13	+EIA DATA SET READY	←	DATA SET READY	CC	6
AA261ACC	AA261	BIM4D09		↔	SIGNAL GROUND	AB	7
002	AA341 AA346	BIM4B09	+EIA CARRIER DETECTOR	←	DATA CARRIER DETECTOR	CF	8
AA341AD4	AA341	BIM4D10	-103F FD ORIGINATE MODE	→	ORIGINATE MODE	CY	11
AA351AF4	AA351	BIM4D12	-LOCAL MODE	→	LOCAL MODE	CX	12
SPARE		BIM4D11					14
SPARE		BIM4D07					15
AA343AC4	AA343	BIM4B08	+103A DIAL DATA TERM READY	→	DATA TERMINAL READY	CD	20

NOTE 1: FOR A PARTICULAR COMMON CARRIER DATA SET, THERE MAY NOT BE SOURCES OR SINKS FOR SOME OF THE ABOVE LISTED SIGNALS

NOTE 2: EIA PIN NO. REFERS TO THE PIN NUMBERS OF THE DATA SET CABLE CONNECTOR WHICH MATES WITH THE DATA SET CONNECTOR

LIMITED DISTANCE TYPE 1 MODEM CABLE

TERMINAL					MODEM CABLE	
NET NUMBER	REF TO PAGE	SLT CONN.	TERM LINE NAME	FLOW	CABLE LINE NAME	PIN
AA351AK4	AA351	BIM4B07	LIM DIST TYPE 1 LINE 1	↔	2 WIRE TRANSMIT AND RECEIVE	GN
AA351AJ4	AA351	BIM4B08	LIM DIST TYPE 1 LINE 2	↔	PAIR OR 4 WIRE TRANSMIT PAIR	R
001	AA345	BIM4B09	RECEIVE LINE 1	←	4 WIRE RECEIVE PAIR	BK
002	AA345	BIM4B10	RECEIVE LINE 2	←		Y

NOTE 3: "PIN" REFERS TO THE TERMINALS OF THE TELEPHONE TYPE CONNECTOR

LIMITED DISTANCE TYPE 2, LEASED, AND SHARED LINES MODEM CABLES

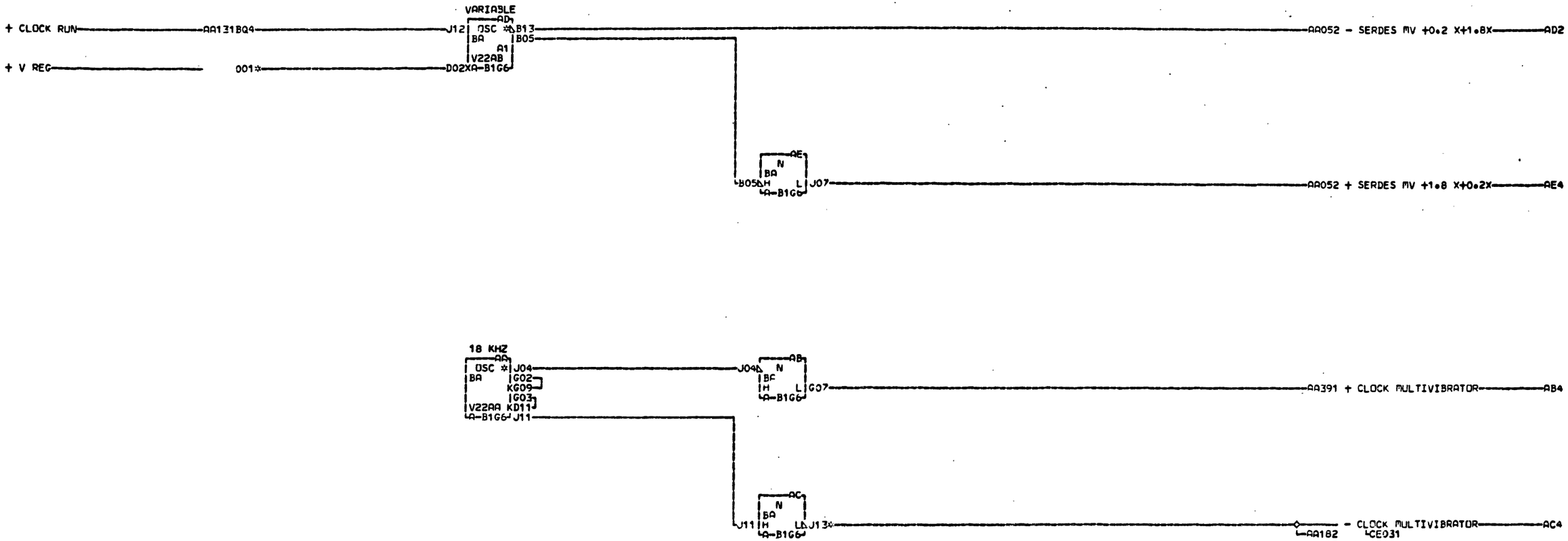
	TERMINAL					MODEM CABLE	
	NET NUMBER	REF TO PAGE	SLT CONN.	TERM LINE NAME	FLOW	CABLE LINE NAME	PIN
	CC061AE4	CC061	CIA5B07	LINE 2 (2W) OR TRANSMIT(4W)	↔	2 WIRE TRANSMIT AND RECEIVE	GN
	CC061AD4	CC061	CIA5B08	LINE 1 (2W) OR TRANSMIT(4W)	↔	PAIR OR 4 WIRE TRANSMIT PAIR	R
	002	CC021 & 41	CIA5B09	RECEIVE 1(4W)	←	4 WIRE RECEIVE PAIR	BK
	001	CC021 & 41	CIA5B10	RECEIVE 2(4W)	←		Y
*	CC061AM4	CC022 3000	CIA5B02	- MODEM TEST LIGHT	→	THIS LEAD CONNECTS THE LIGHT DRIVER TO THE MODEM TEST LIGHT MOUNTED ON THE SIDE OF THE STAND	
*			CIA5B03	NOT USED IN THE 2741			
*	003 001 003 001	CC021 CC031 CC041 & 51 3000	CIA5B04	+MOD TEST NOTE: THIS SIGNAL CONTROLS THE MODEM WRAP TEST	←	NORMALLY OPEN, "TEST" SWITCH MOUNTED ON SIDE OF STAND	
*	CC061AK4	CC061 3000	CIA5B05	+12 VOLTS	→	ARM, "TEST" SWITCH MOUNTED ON SIDE OF STAND	
*	NONE EXISTS	3000	CIA5D08	TERM SIGNAL GND NOT USED IN THE 2741			

SEE NOTE 3

* LEASED AND SHARED LINES MODEM CABLES ONLY

SEE PAGE 9011 FOR SHARED LINES FILTER CONNECTIONS

DATE	E.C. NO.	DATE	E.C. NO.	DATA SET AND MODEM SIGNALS	
1 DEC 66	507247				
APR 68	307100			PART NO. 1186497	PAGE NO. AA352
				IBM 2741	



AA361
000

001
01A-B1N2D09
AC4 A-B1E1B02

LOC. TYPE
A-B1G6

CLOCK5-539HZ AND 18KHZ
P-N 5804381
—E.C.—HISTORY—
MACH.2741A
FRAME 01
IBM CORP. LX
DATE LAST EC
11-03-67 307100
P.N. 1176235

AA361
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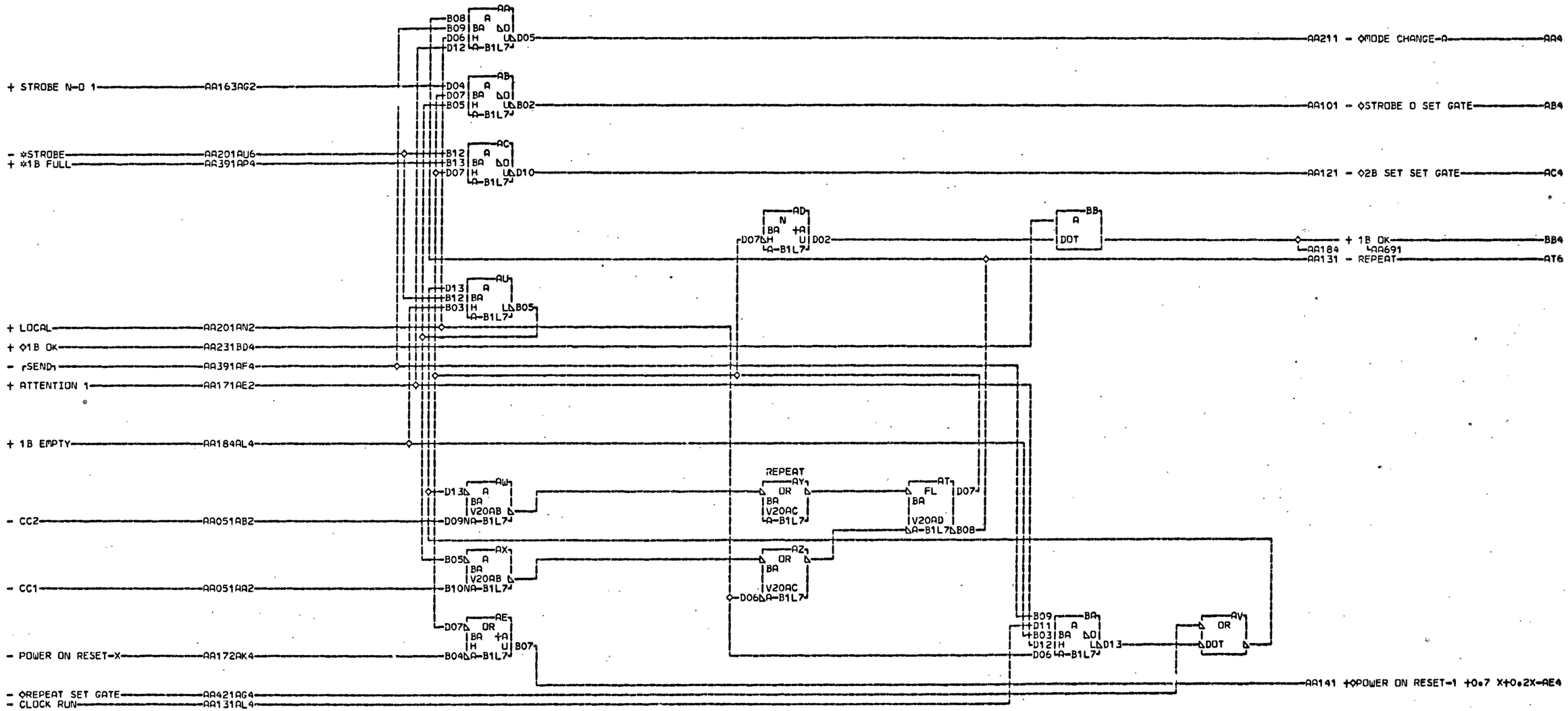
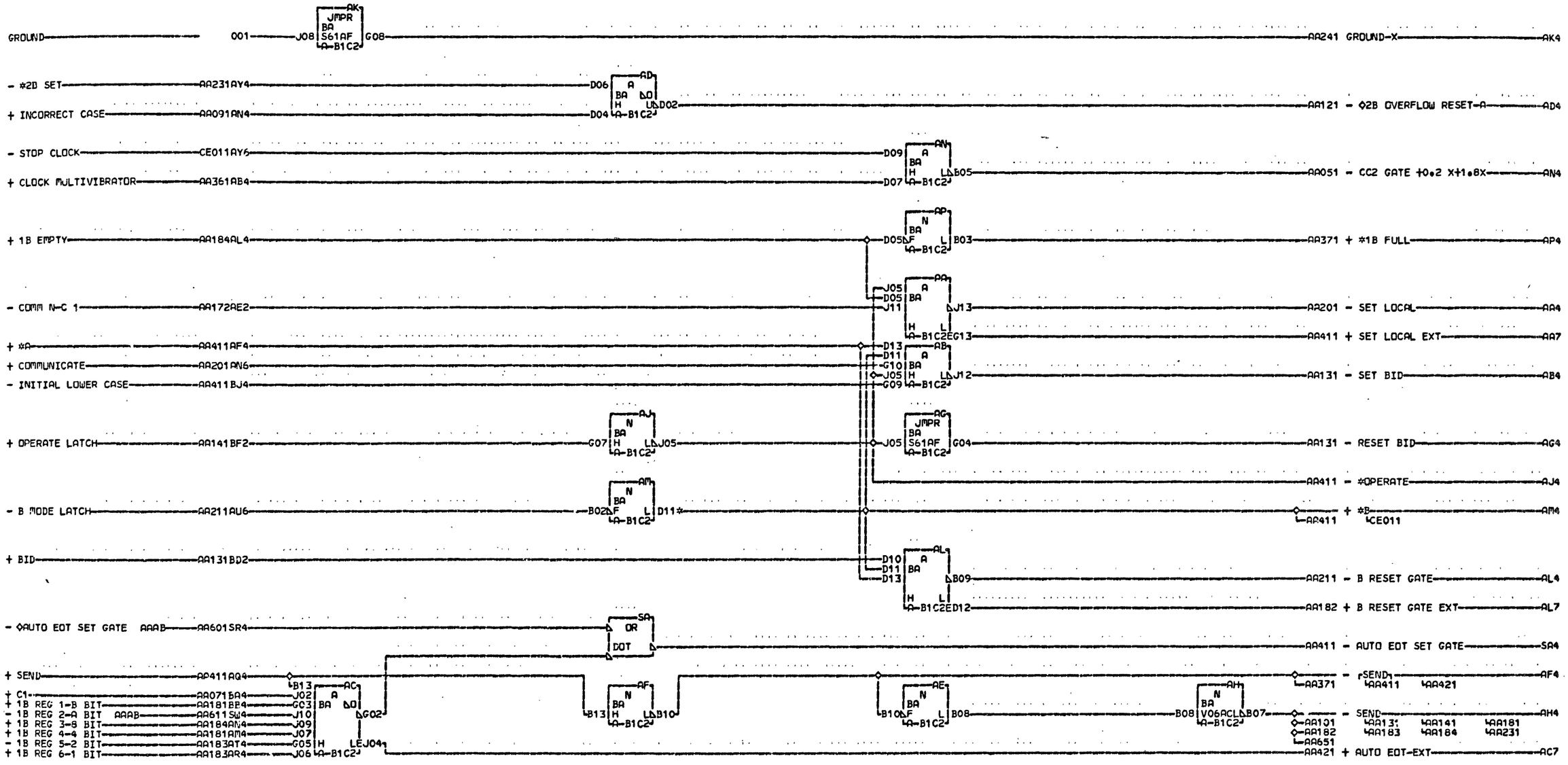


LOC. TYPE
A-B1L7

CHECK LOOP AND REPEAT LATCH
P-N 5803744
-E.C.-HISTORY- MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.No. 5166220

AA371 002

002
SIM TO PN 1176236 EC 307100



AM4 ?-B1D1D07

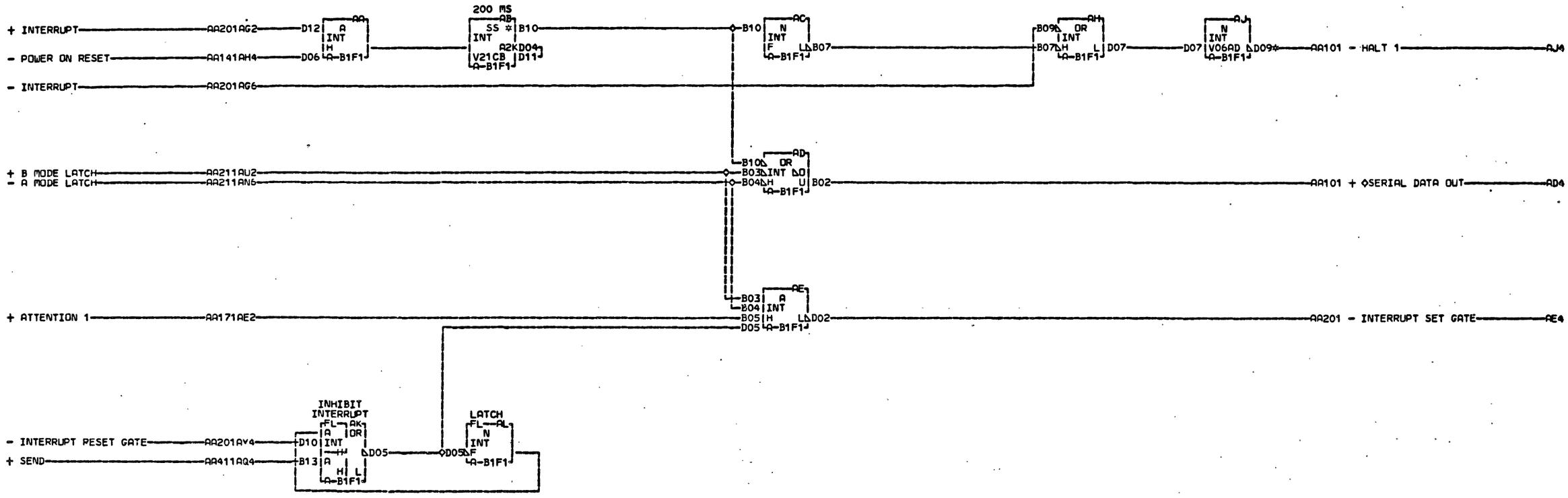
LOC. TYPE
A-B1C2

2741 LINE CONTROL
P-N 5801324
—E.C.—HISTORY— MACH.2741A
345323
FRAME 01
IBM CORP. SDD
DATE LAST EC
02-09-70 308734
P.N. 1277331

A A 3 9 1 002

002

SIM TO PN 1176237 EC 307100

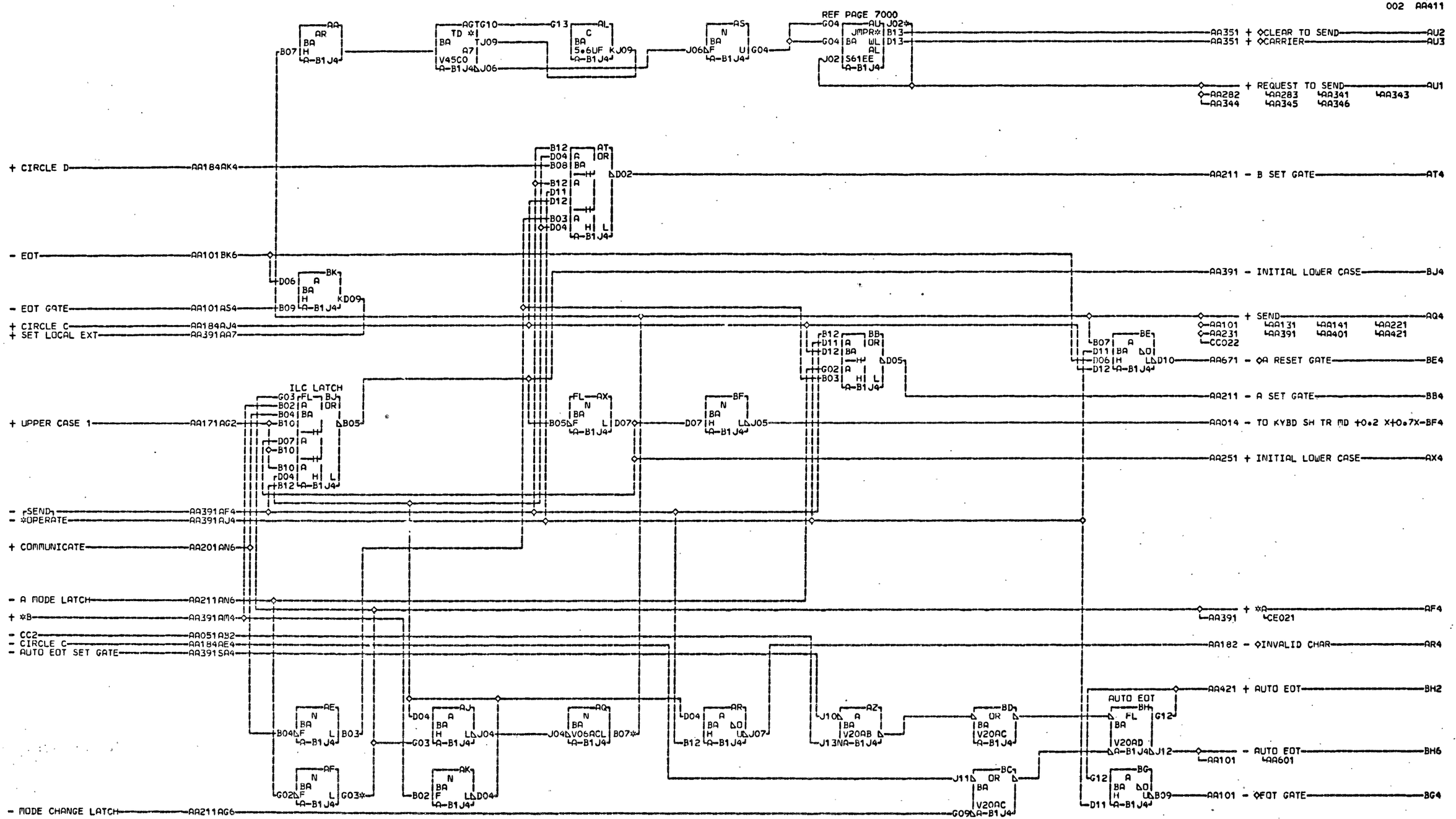


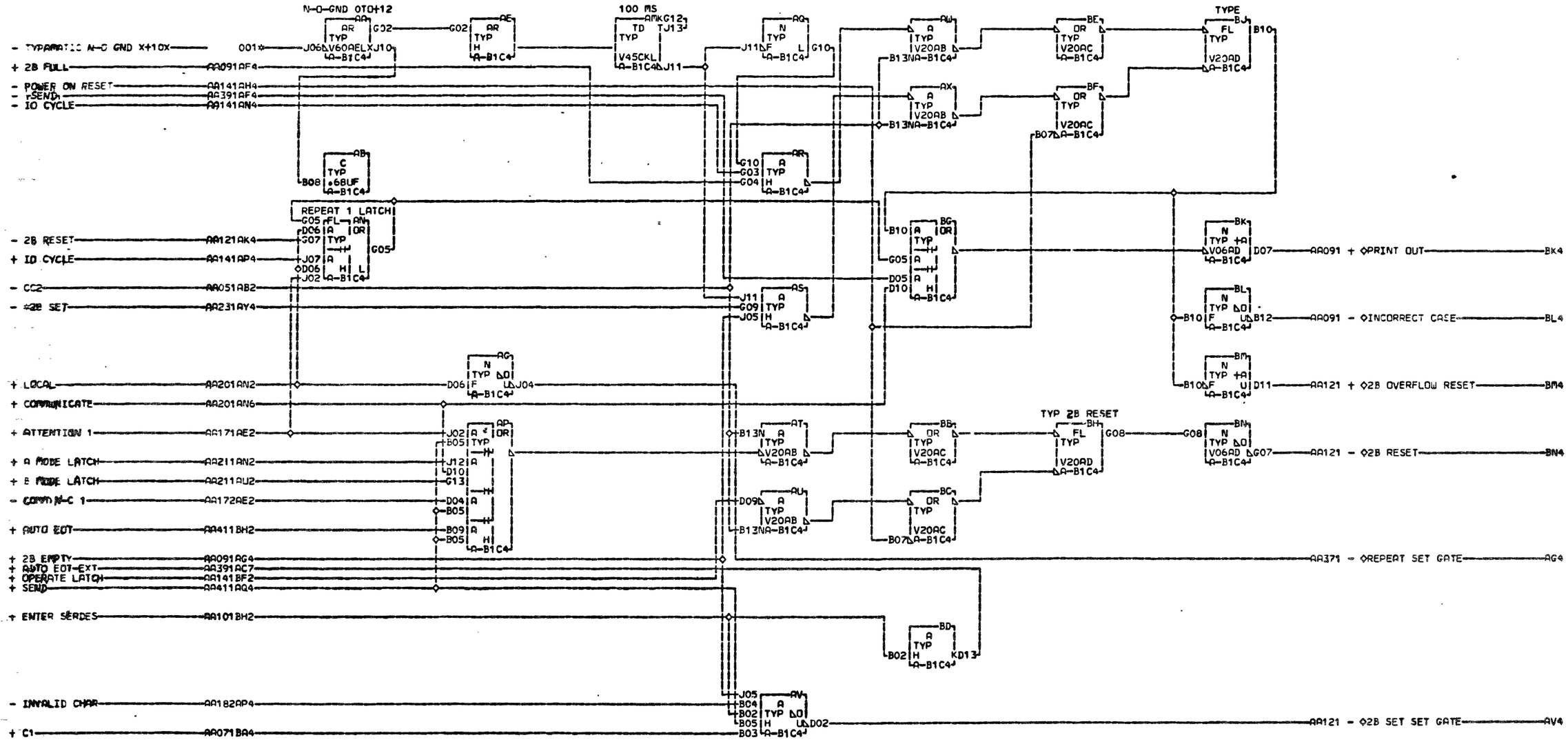
AJ4 RESISTOR
A-B1F1B08

LOC. TYPE
A-B1F1

INTERRUPT
P-N 5803849
E.C. HISTORY
MACH.2741A
FRAME 01
IBM CORP. LX
DATE LAST EC
02-21-68 307100
P.No. 1176238

AA401 000


REF PAGE 7000
+ CIRCLE D
AA184AK4
- EOT
AA101BK6
- EOT GATE
AA101AS4
+ CIRCLE C
AA184AJ4
+ SET LOCAL EXT
AA391AA7
ILC LATCH
+ UPPER CASE 1
AA171AG2
- SEND
AA391AF4
- *OPERATE
AA391AJ4
+ COMMUNICATE
AA201AN6
- A MODE LATCH
AA211AN6
+ *B
AA391AM4
- CC2
AA051AB2
- CIRCLE C
AA184AE4
- AUTO EOT SET GATE
AA391SA4
- MODE CHANGE LATCH
AA211AG6
AA351 + ◇CLEAR TO SEND AU2
AA351 + ◇CARRIER AU3
+ REQUEST TO SEND AU1
AA282 AA283 AA341 AA343
AA344 AA345 AA346
AA211 - B SET GATE AT4
AA391 - INITIAL LOWER CASE BJ4
+ SEND AQ4
AA101 AA131 AA141 AA221
AA231 AA391 AA401 AA421
CC022
AA671 - ◇A RESET GATE BE4
AA211 - A SET GATE BB4
AA014 - TO KYBD SH TR MD +0.2 X+0.7X-BF4
AA251 + INITIAL LOWER CASE AX4
+ *A AF4
AA391
CE021
AA182 - ◇INVALID CHAR AR4
AA421 + AUTO EOT BH2
AUTO EOT
- AUTO EOT BH6
AA101
AA601
AA101 - ◇EOT GATE BG4
V20AB
V20AC
V20AD
S61EE
V45C0
5.6UF
JMPR*
AF4 A-B1E1D07
AQ4 A-C1B5D06
01A-B1N4D06
AU1 A-B1L4B12
01A-B1K4B09
01A-B1K4J02
RESISTOR
A-B1J4J02
LOC. TYPE
A-B1J4
AUTO EOT AND ILC LATCHES
P-N 5804515
-E.C.-HISTORY-
MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.N. 1277332
002
SIM TO PN 1176239 EC 307100

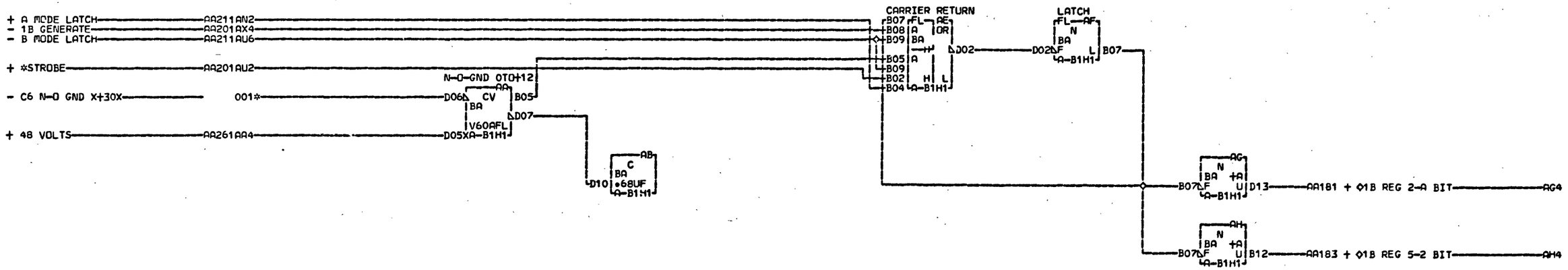


001
01A-B1M1D05

LOC. TYPE
A-B1C4

TYPAMATIC
P-N 5806005
E.C. HISTORY
MACH. 2741A
FRAME 01
IBM CORP. LEX
DATE LAST EC
02-26-68 307100
P.N. 1176240

AA421 000



AA431
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001
01A-B1N1D13

LOC• TYPE
A-B1H1

CARRIER RETURN LATCH
P-N 5800889
—E•C•—HISTORY—
MACH•2741A
FRAME 01
IBM CORP• LX
DATE LAST EC
02-26-68 307100
P•N• 1186239

AA431
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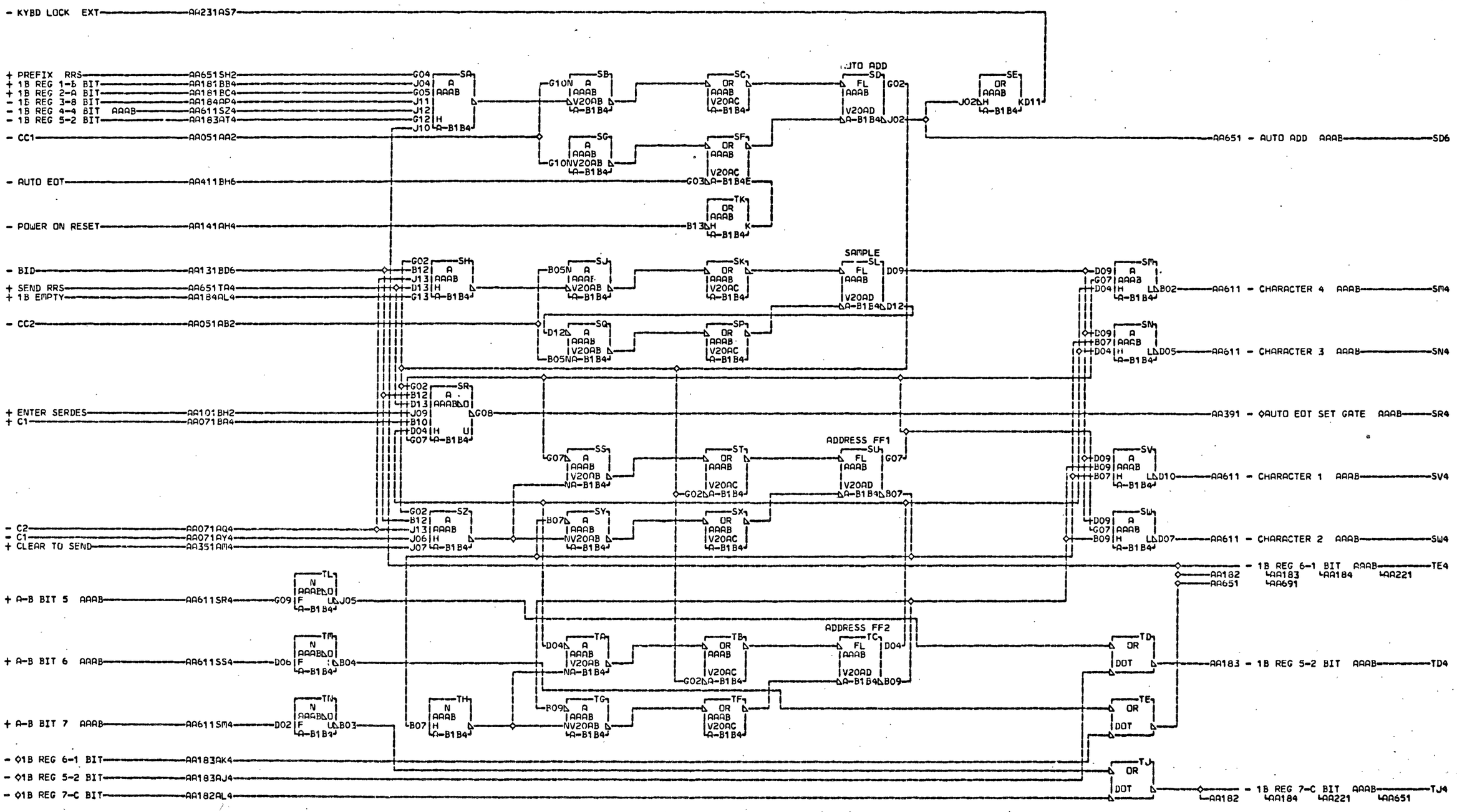
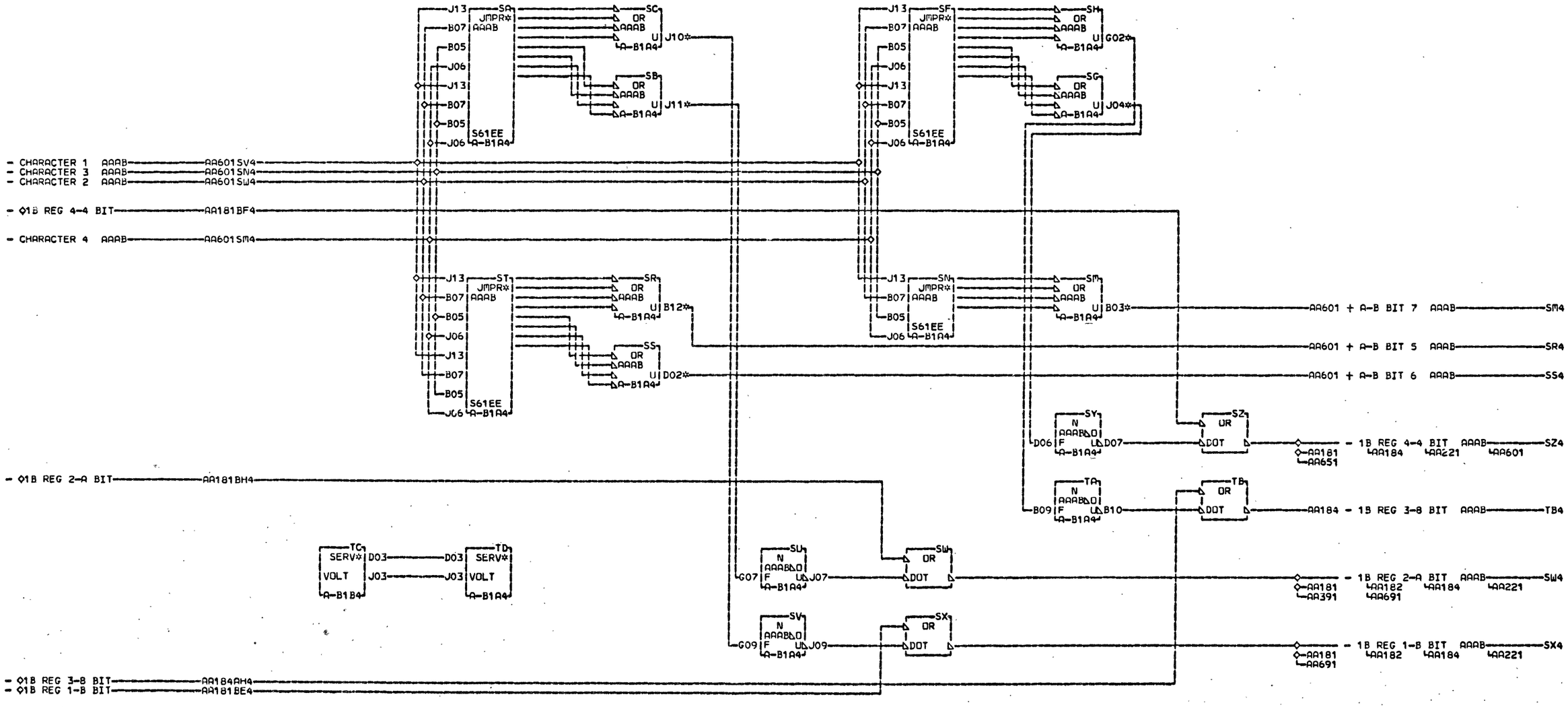

- KYBD LOCK EXT AA231AS7
+ PREFIX RRS AA651SH2
+ 1B REG 1-6 BIT AA181BB4
+ 1B REG 2-A BIT AA181BC4
- 1B REG 3-8 BIT AA184AP4
- 1B REG 4-4 BIT AAAB AA611SZ4
- 1B REG 5-2 BIT AA183AT4
- CC1 AA051AA2
- AUTO EOT AA411BH6
- POWER ON RESET AA141AH4
- BID AA131BD6
+ SEND RRS AA651TA4
+ 1B EMPTY AA184AL4
- CC2 AA051AB2
+ ENTER SERDES AA101BH2
+ C1 AA071BA4
- C2 AA071AQ4
- C1 AA071AY4
+ CLEAR TO SEND AA351AM4
+ A-B BIT 5 AAAB AA611SR4
+ A-B BIT 6 AAAB AA611SS4
+ A-B BIT 7 AAAB AA611SM4
- ◇1B REG 6-1 BIT AA183AK4
- ◇1B REG 5-2 BIT AA183AJ4
- ◇1B REG 7-C BIT AA182AL4
AUTO ADD
SAMPLE
ADDRESS FF1
ADDRESS FF2
AA651 - AUTO ADD AAAB SD6
AA611 - CHARACTER 4 AAAB SM4
AA611 - CHARACTER 3 AAAB SN4
AA391 - ◇AUTO EOT SET GATE AAAB SR4
AA611 - CHARACTER 1 AAAB SV4
AA611 - CHARACTER 2 AAAB SW4
- 1B REG 6-1 BIT AAAB TE4
AA182 AA183 AA184 AA221 AA651 AA691
AA183 - 1B REG 5-2 BIT AAAB TD4
- 1B REG 7-C BIT AAAB TJ4
AA182 AA184 AA221 AA651
LOC. TYPE
A-B1B4 7370
AUTO ADDRESS ANSWER BACK-1
P-N 5807370
E.C.-HISTORY
MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.No. 1277333
AA601 002



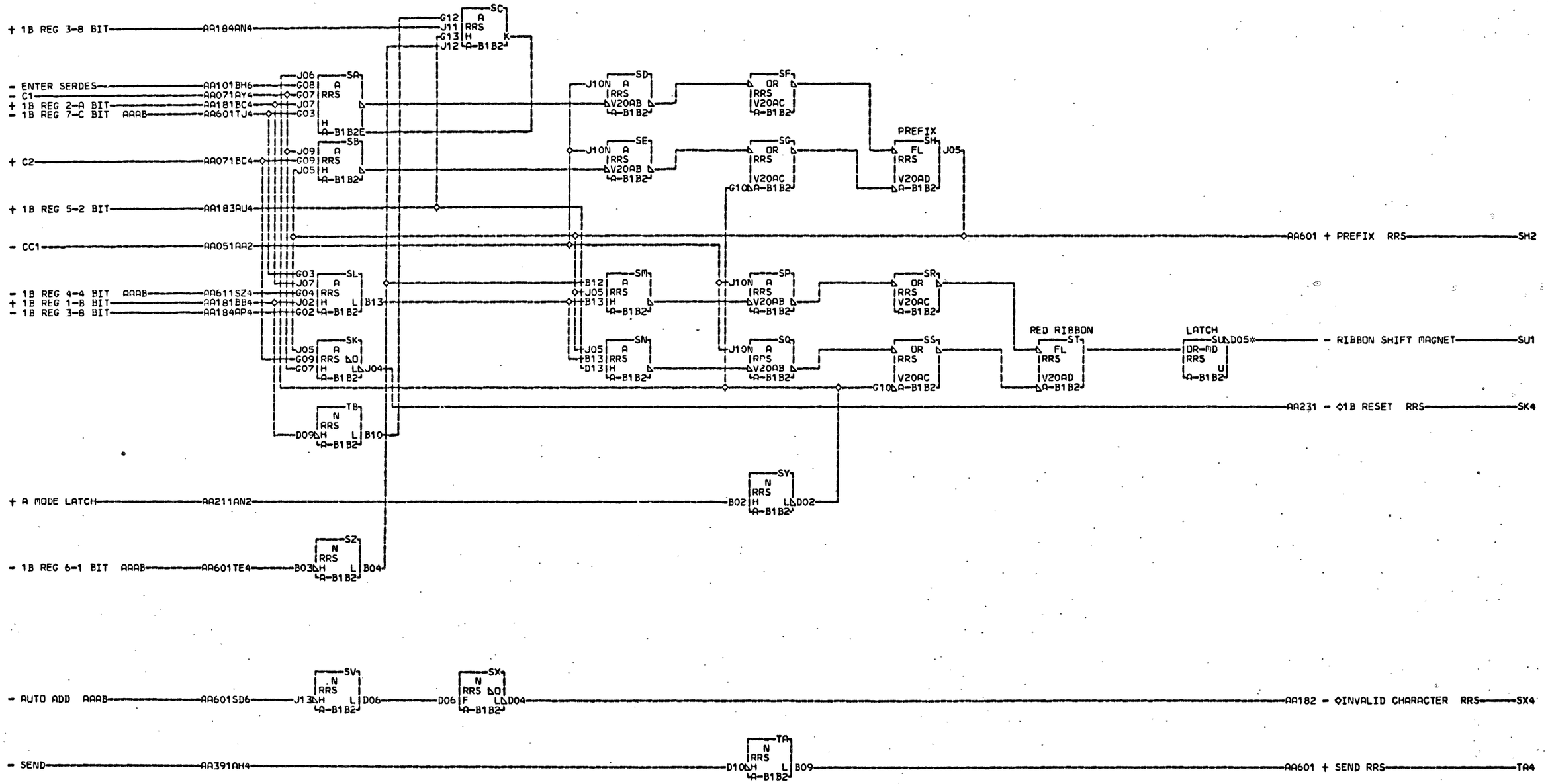
A A 6 1 1 002

SB4 RESISTOR A-B1A4D04
A-B1A4J12 SR4 RESISTOR
SC4 RESISTOR A-B1A4D12
A-B1A4G12 SS4 RESISTOR
SG4 RESISTOR A-B1A4D05
A-B1A4J05
SH4 RESISTOR
A-B1A4G05
SM4 RESISTOR

LOC. TYPE
A-B1A4 7371

AUTO ADDRESS ANSWER BACK-2
P-N 5807371
—E.C.—HISTORY— MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.No. 1277334

A A 6 1 1 002

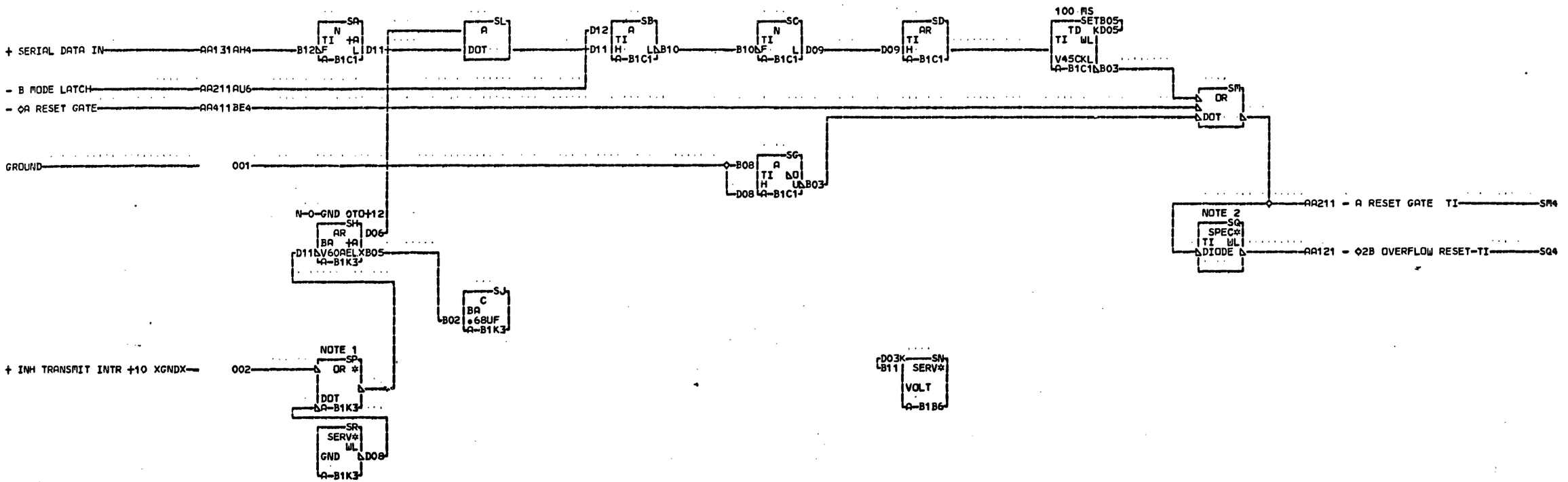


SU1 A-B1N1D12

LOC. TYPE
A-B1B2 7372

RIBBON SHIFT
P-N 5807372
-E.C.-HISTORY- MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.No. 1277335

AA651 002



NOTE 1 ON SOME MACHINES
THIS NET WILL BE GROUNDED
A THROUGH THE I-O CABLE
A RATHER THAN WITH PIN D08
6 NOTE 2 BACK PANEL DIODE
7 PIN C1B03 (CATHODE) TO
1 PIN C2D02

002

SP4 A-B1N1B13

LOC. TYPE
A-B1C1 3846
A-B1K3

TRANSMIT INTERRUPT

—E.C.-HISTORY— MACH.2741A

345323

FRAME 01

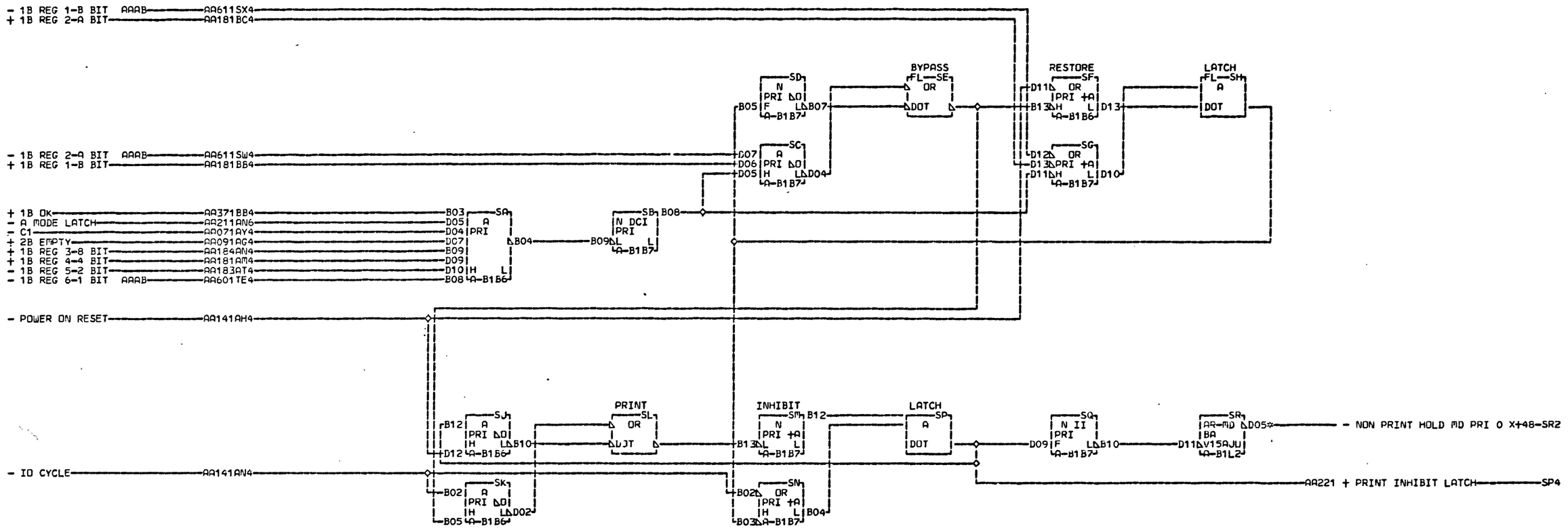
IBM CORP. SDD

DATE LAST EC

02-09-70 308734

P.N. 1277336

A A 6 7 1 002

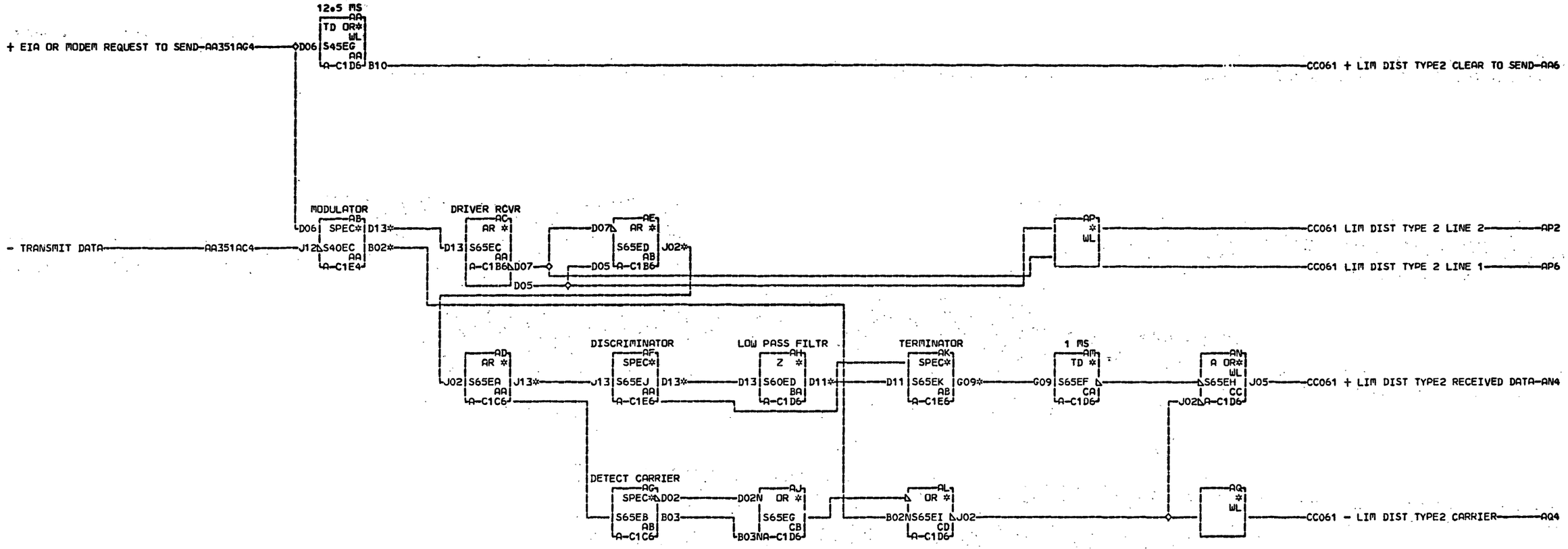


SR2 A-B1N1B05

LOC.	TYPE
A-B1B6	0287
A-B1B7	0299
A-B1L2	

AA691 002

PRINT INHIBIT		
E.C. HISTORY	MACH. 2741A	AA691
	FRAME 01	002
	IBM CORP. SDD	
DATE LAST EC	P.N. 1277337	
06-03-68 345323		



SEE FE MAINTENANCE MANUAL
FORM 226-3004 TO DETERMINE
C CORRECT JUMPERING OF
C PROGRAMMABLE RECEPTACLES.
0
1
1

000

AB2 A-C1E4D13 01A-C1D6D13
01A-C1B6D13 AH4 A-C1D6D11
AB4 A-C1E4B02 01A-C1E6D11
01A-C1D6B02 AK4 A-C1E6G09
AD4 A-C1C6J13 01A-C1D6G09
01A-C1E6J13
AE4 A-C1B6J02
01A-C1C6J02
AF4 A-C1E6D13

LIMITED DISTANCE TYPE-2

E.C.-HISTORY

MACH.2741A

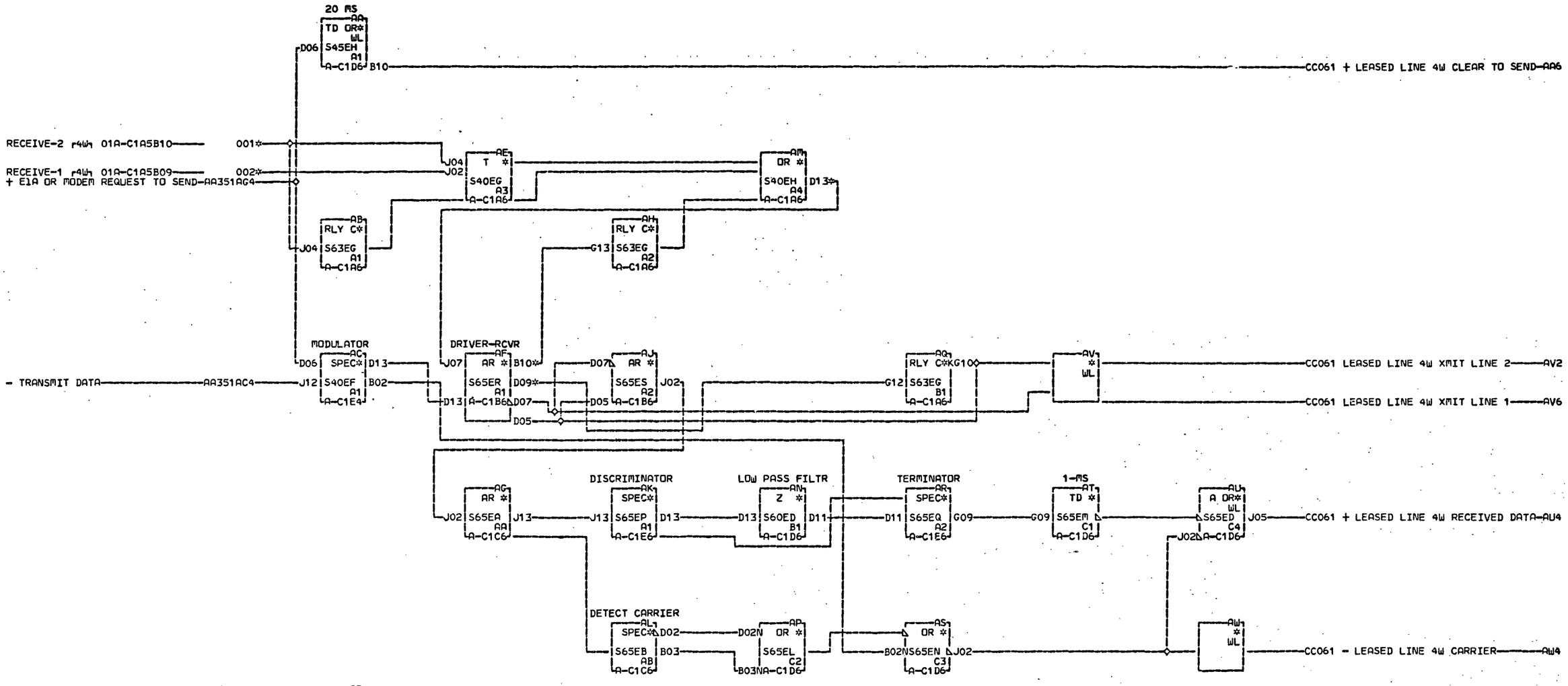
FRAME 01

IBM CORP. SDD

DATE LAST EC
02-21-68 307100

P.N. 5162289

C C 0 1 1 000



PROGRAMMABLE RECEPTACLES ON
CARD 5808121 MUST NOT BE
C JUMPERED FOR 4 WIRE OPERATION.
C SEE FE MAINTENANCE MANUAL
0 FORM 226-3004 TO DETERMINE
2 CORRECT JUMPERING OF OTHER
1 RECEPTACLES.

CCC

001		AF2 A-C1B6B10
	01A-C1A5B10	01A-C1A6G13
	01A-C1A6J04	AF4 A-C1B6D09
002		01A-C1A6G12
	01A-C1A5B09	AM4 A-C1A6D13
	01A-C1A6J02	01A-C1B6J07
003		
	01A-C1A5B04	
	01A-C1A6G09	

LEASED LINE 4 WIRE ADAPTER

E.C.-HISTORY — MACH.2741A

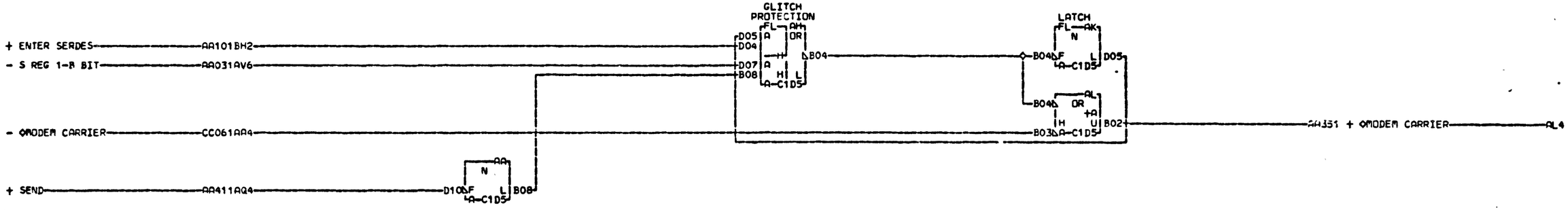
FRAME 01

IBM CORP. SDD

DATE LAST EC
02-26-68 307100

P.N. 5162290

C C 0 2 1 000

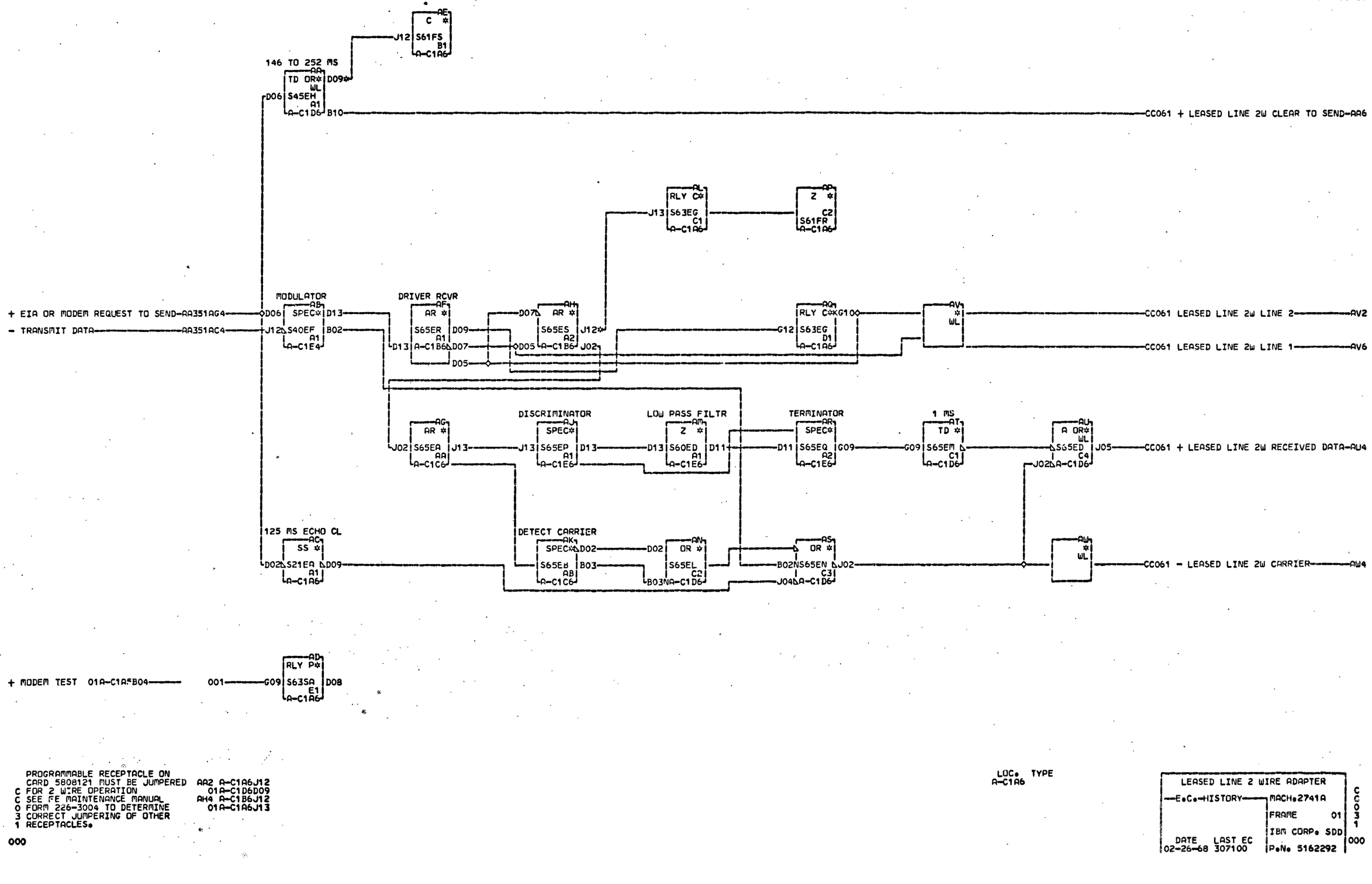


AM4 A-C1A5B02

LOC. TYPE
A-C1D5

MOD TEST AND GLITCH PROTECTION
LL OR SL 2 OR 4W ADAPTER
—E.C.—HISTORY—
MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
02-21-68 307100
P.N. 5162291

CCCNN 000
CCCNN 000



PROGRAMMABLE RECEPTACLE ON CARD 5808121 MUST BE JUMPERED
C FOR 2 WIRE OPERATION
C SEE FE MAINTENANCE MANUAL
0 FORM 226-3004 TO DETERMINE
3 CORRECT JUMPERING OF OTHER
1 RECEPTACLES.

AA2	A-C1A6J12
	01A-C1D6D09
AH4	A-C1B6J12
	01A-C1A6J13

000

LOC. TYPE
A-C1A6

LEASED LINE 2 WIRE ADAPTER

E.C.-HISTORY

MACH.2741A

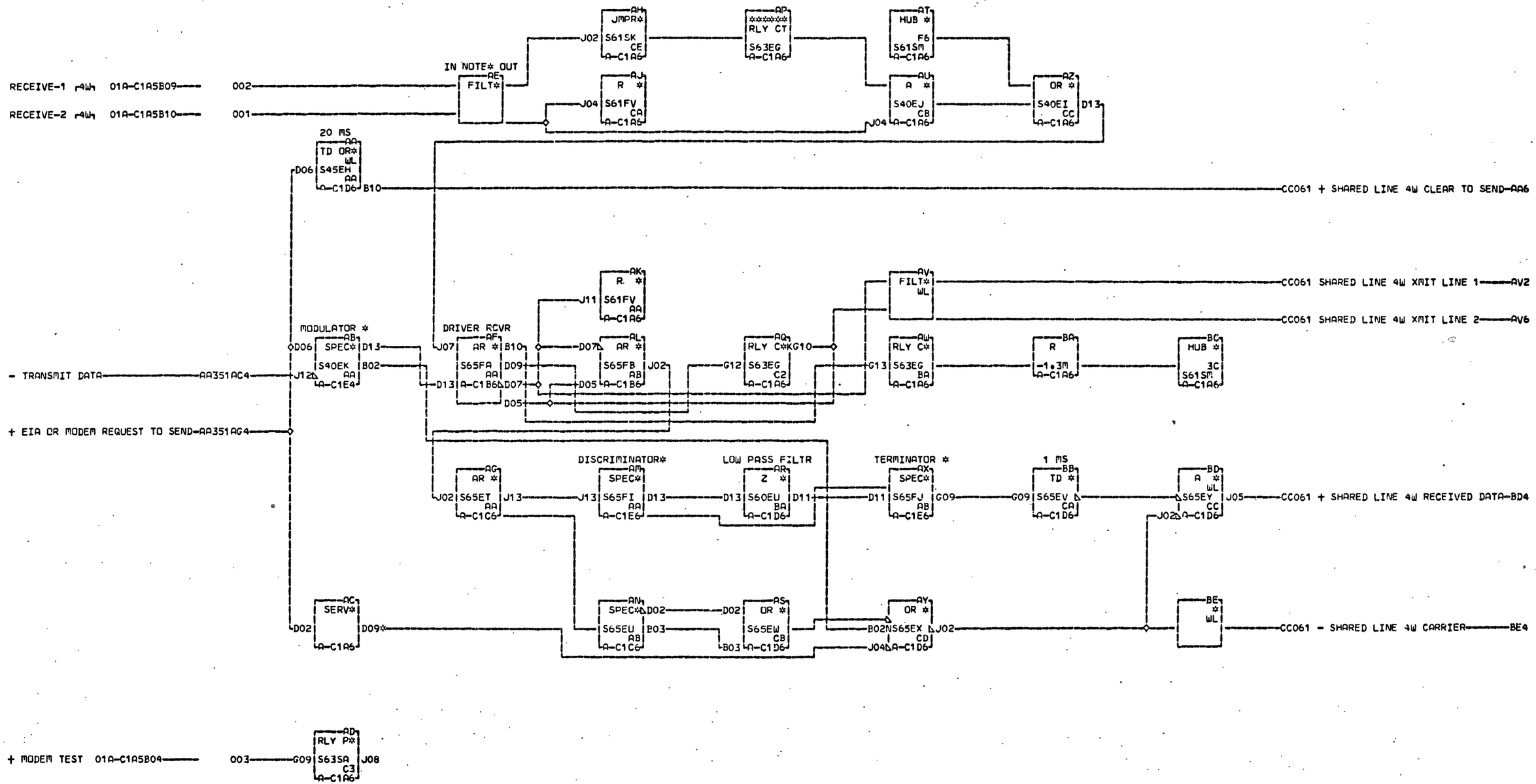
FRAME 01

IBM CORP. SDD

DATE LAST EC
02-26-68 307100

P.N. 5162292

CCO31 000



* SEE REFERENCE PAGE 5000 FOR CARD AND PAGE 8000 FOR FILTER VARIATIONS.

SERV BLOCKS PERFORM NO LOGIC FUNCTION-USED FOR WIRING ONLY

PROGRAMMABLE RECEPTACLES ON CARD 5808125 NOT JUMPERED FOR 4 WIRE OPERATION.

000

AC4 A-C1D6J04

LOC. TYPE
A-C1A6

SHARED LINE 4 WIRE ADAPTER

E.C.-HISTORY

MACH.2741A

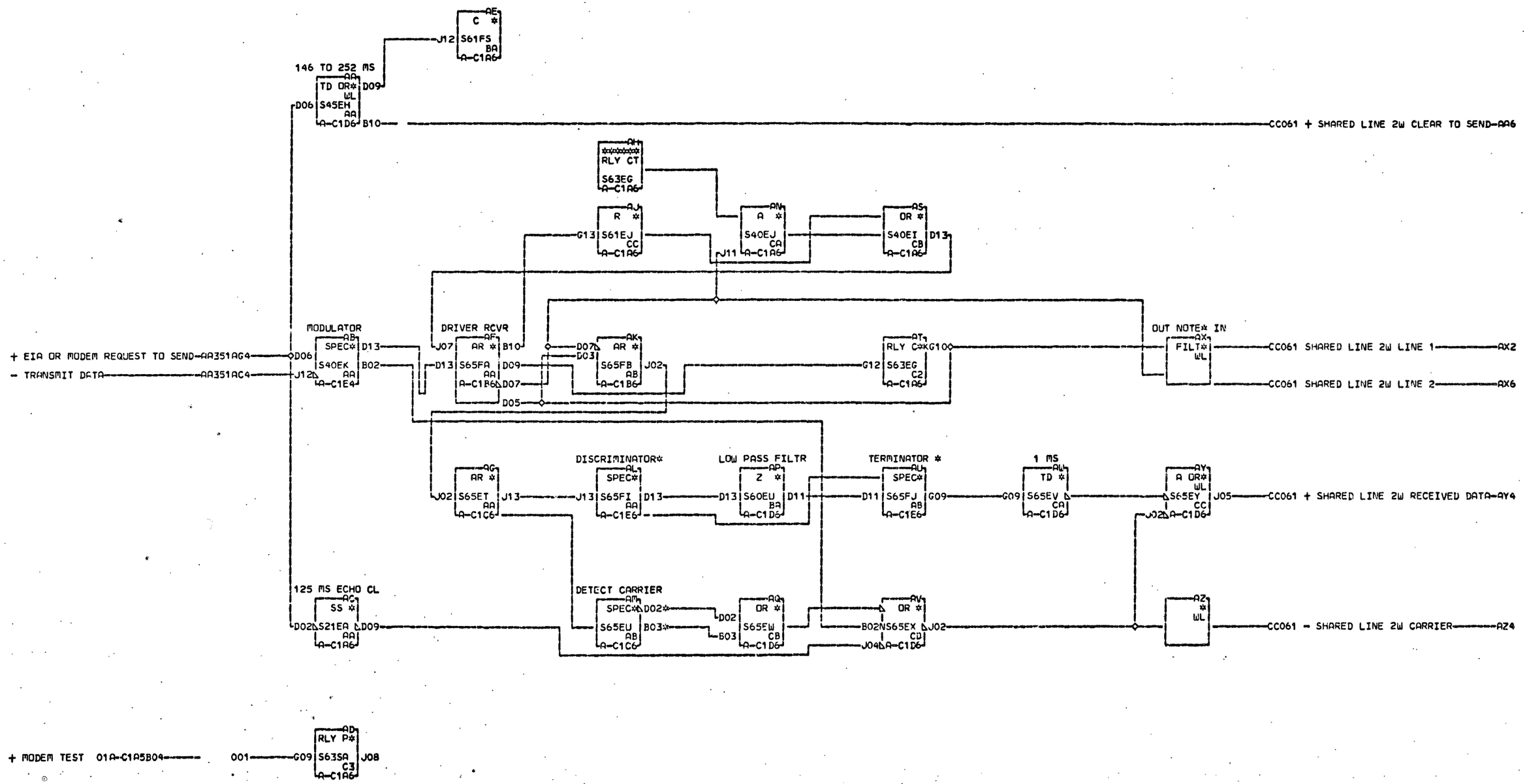
FRAME 01

IBM CORP. SDD

DATE LAST EC
02-21-68 307100

P.No. 5162293

CC041 000



* SEE REFERENCE PAGE 5000 FOR CARD AND PAGE 8000 FOR FILTER VARIATIONS.

C PROGRAMMABLE RECEPTACLES ON CARD 5808125 MUST BE JUMPERED FOR 2 WIRE OPERATION

AM2 A-C1C6D02
01A-C1D6D02
AM4 A-C1C6B03
01A-C1D6B03

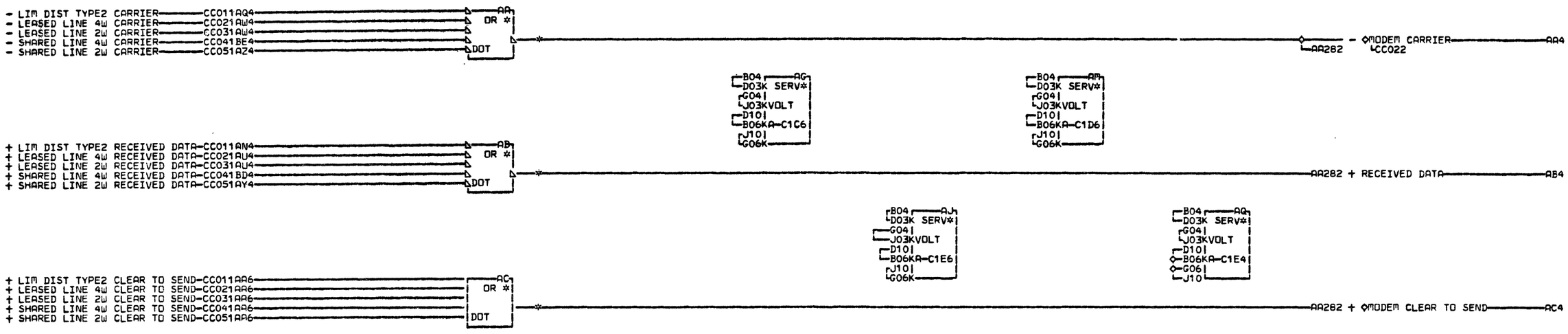
LOC. TYPE
A-C1A6

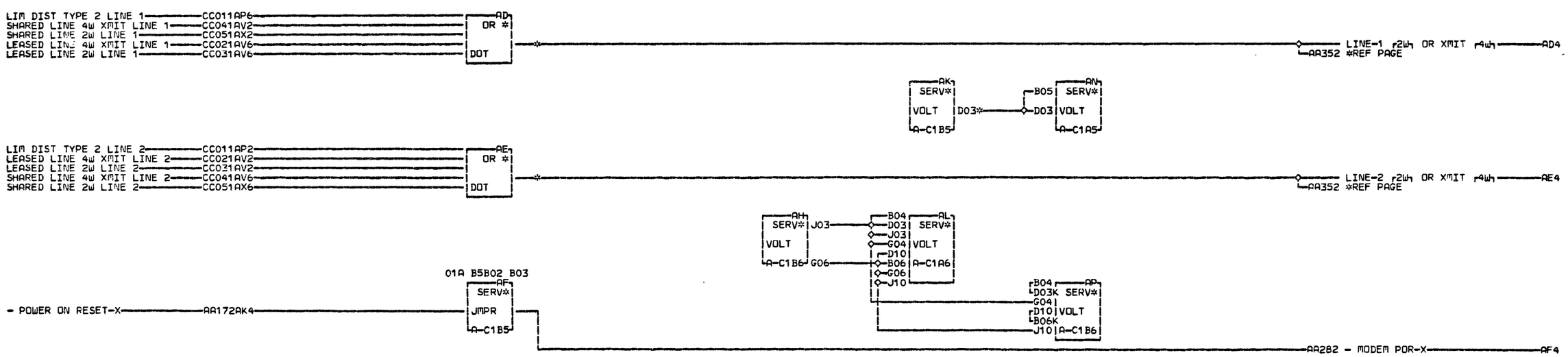
SHARED LINE 2 WIRE ADAPTER

E.C.-HISTORY | MACH.2741A | FRAME 01 | IBM CORP. SDD | P.No. 5162294

DATE 02-21-68 | LAST EC 107100

CC051 000





C C 0 6 1 002

SIM TO PN 1176241 EC 307100

SERV BLOCKS AND MODEM DOT OVERLAYS

E.C.-HISTORY

MACH.2741A

FRAME 01

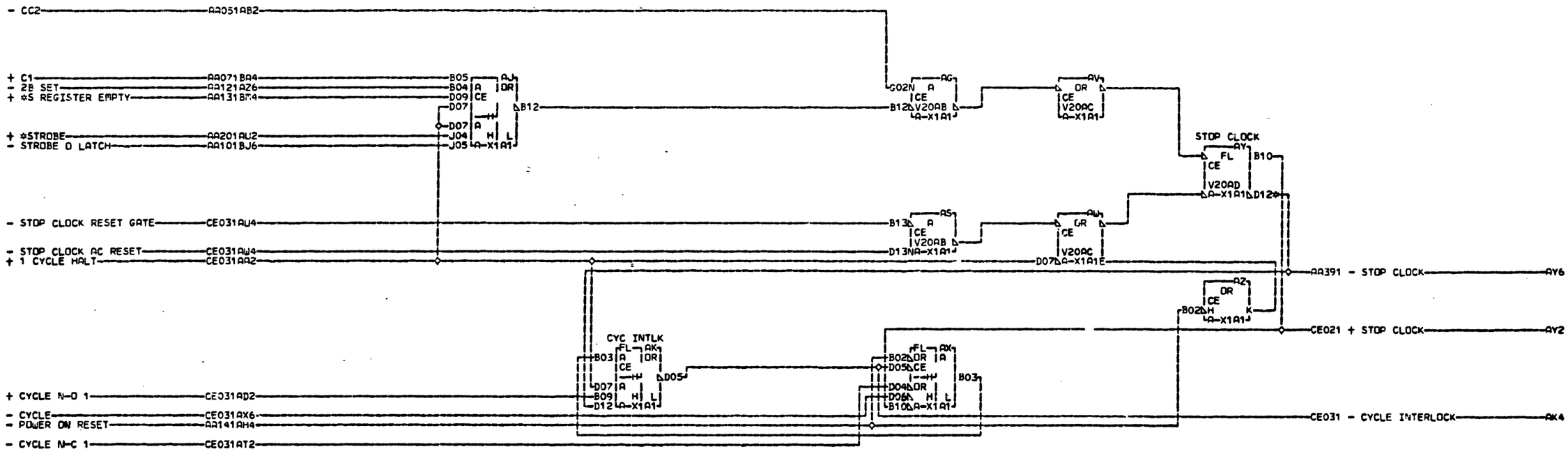
IBM CORP. SDD

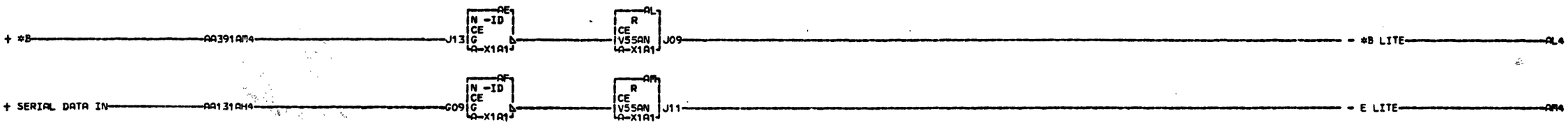
DATE LAST EC

06-03-68 345323

P.N. 1277402

C C 0 6 1 002





AY6 A-B1D1B09

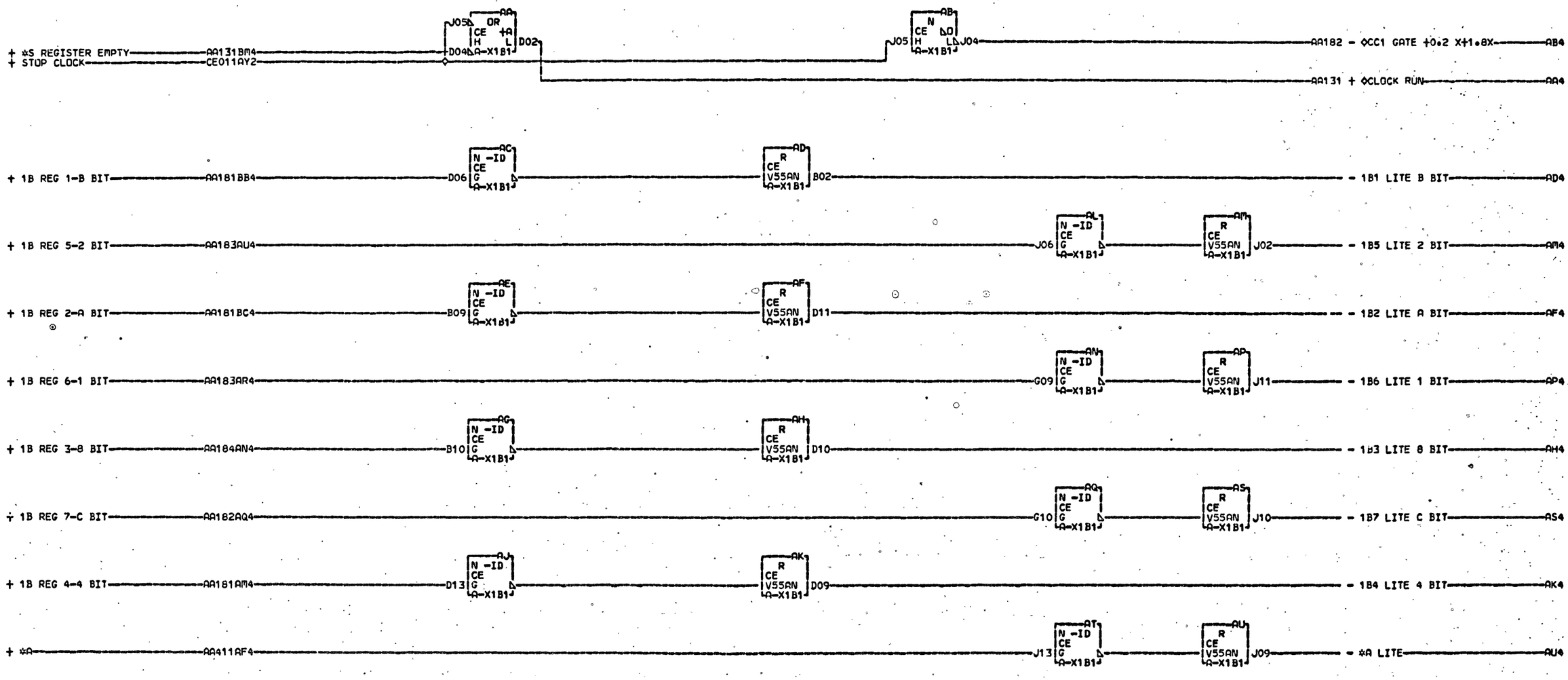
LOC. TYPE
A-X1A1

CE AID CYCLE INLK AND STOP CLOCK LATCHES
P-N 5801333
MACH.2741A
FRAME 01
IBM CORP. LX
P.No. 1176242

E.C. HISTORY

DATE LAST EC
02-21-68 307100

CE011 000

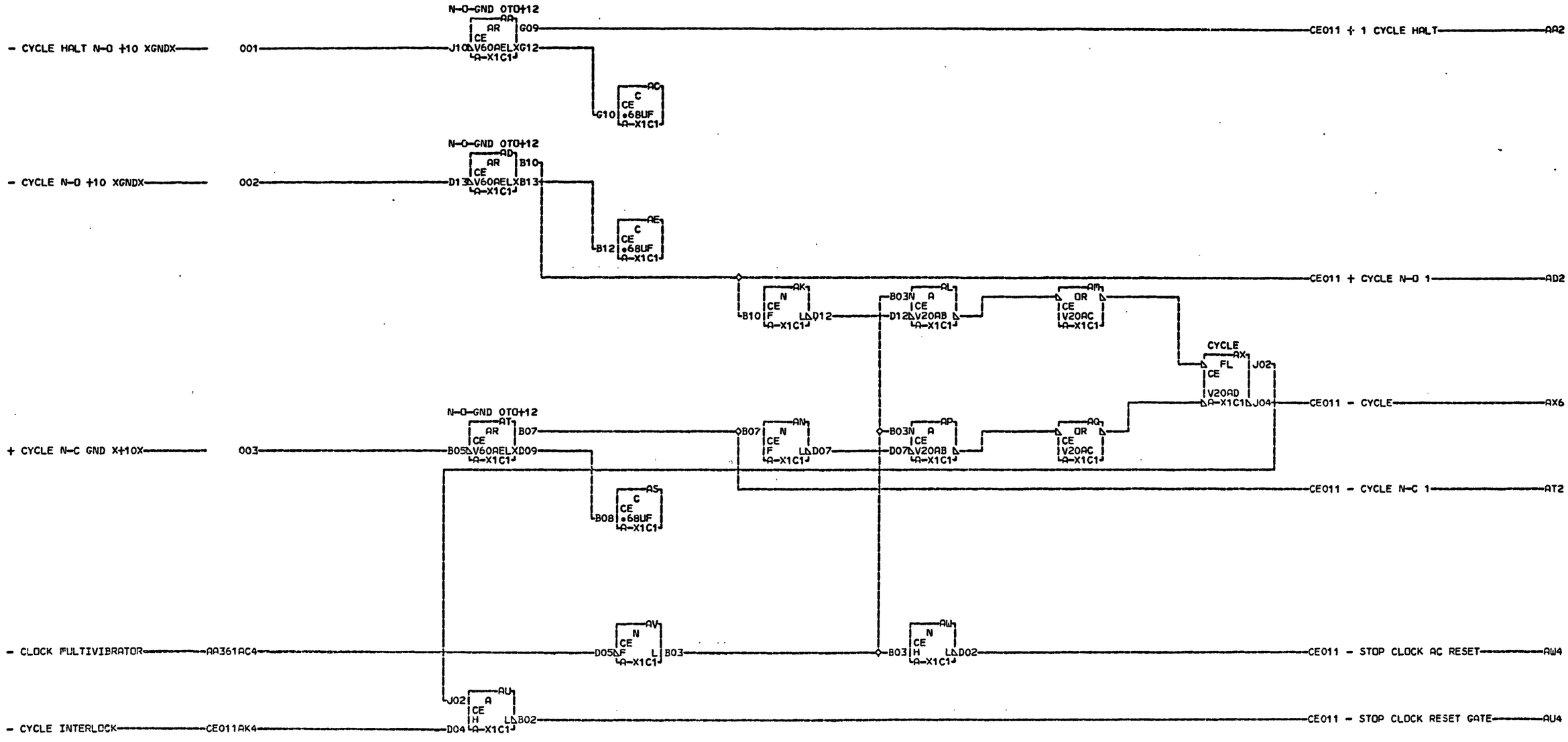


LOC. TYPE
A-X1B1

CE AID INDICATOR DRIVERS
P-N 5801334
E.C.-HISTORY
MACH.2741A
FRAME 01
IBM CORP. LX
DATE LAST EC
10-30-67 307100
P.N. 1176243

CE021
000

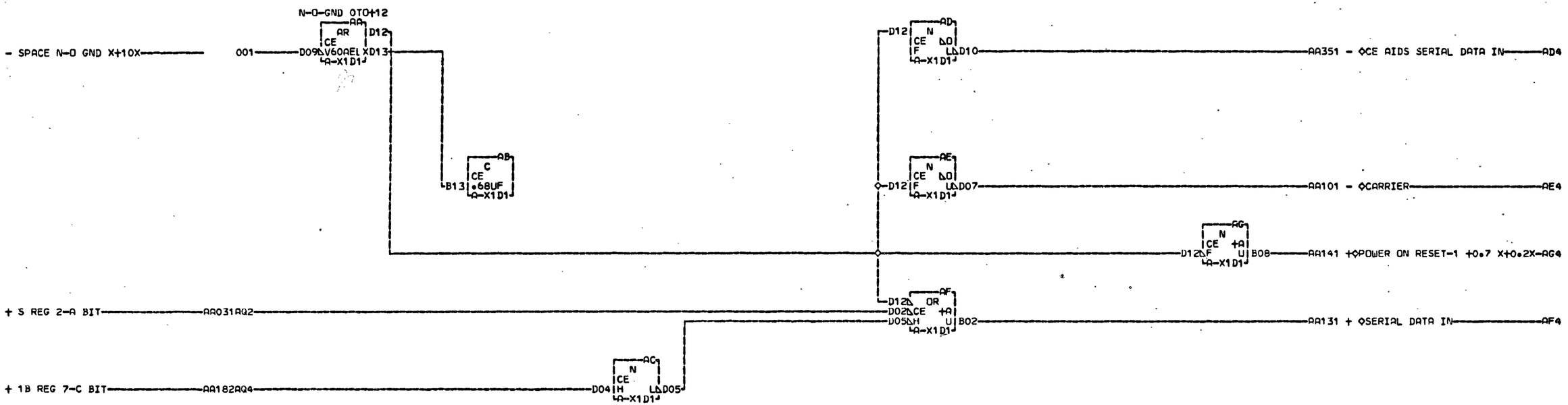
CE021
000



LOC. TYPE
A-X1C1

CE AID CYCLE LATCH
P-N 5801335
E.C.-HISTORY
MACH.2741A
FRAME 01
IBM CORP. LX
DATE LAST EC
02-21-68 307100
P.N. 1176244

CE31 000



LOC. TYPE
A-X1 D1

CE AID
P-N 5800885
—E.C.-HISTORY— MACH.2741A
FRAME 01
IBM CORP. SDD
DATE LAST EC
06-03-68 345323
P.N. 1277403

CE041 002

CE041 002

SIM TO PN 1176245 EC 307100