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# 8100 Information System

# 8130/8140 Processors

# 8101 Storage and Input/Output Unit

(Volume 4 of 4)

## Maintenance Information

SY27-2521-3

The following listing shows, by volume (binder) number, the basic contents of the *8100 Information System Maintenance Information Manual*. The column not shaded indicates the volume you are using; the shaded columns indicate the contents of the other three volumes.

## Volume 1 (Binder 1)

**Chapter 1. Start (ST)**
- ST100 Distributed Processing Programming Executive (DPPX)
- ST200 Distributed Processing Control Executive (DPCX)
- ST300 Non-IBM Program Product
- ST400 Common Messages, Action Plans, and Procedures

**Chapter 2. Configuration and Maintenance Procedures (CP)**
- CP100 System Configuration Information
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- CP300 MD Diskette Configuration Procedures
- CP400 Maintenance Device Function and Use
- CP500 Initial Program Load (IPL)
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- LT200 8140 Locations
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**Chapter 4. General Reference Information (GR)**
- GR100 8100 Information System Description and Operation
- GR200 Components
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- GR600 Basic Data Flow
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## Volume 2 (Binder 2)

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**Display and Printer Adapter (AD)**
- AD100 General Information
- AD200 Offline and Online Tests
- AD300 Intermittent Failure Repair Strategy
- AD400 Signal Paths and Detailed Operational Description
- AD500 Attached Device Information

**Bringup (BU)**
- BU100 General Information
- BU200 Offline and Online Bringup and Basic Operator Panel Tests
- BU300 Intermittent or Random Failure Repair Strategy
- BU400 Signal Paths and Detailed Operational Description
- BU500 Adjustment, Removal, Replacement, and Voltage Check Procedures

## Volume 3 (Binder 3)

**Communications Features (CA)**
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- CA100 General Information
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- DA200 Offline Tests
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## Volume 4 (Binder 4)

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**Power (PA)**
- PA100 General Information
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**System Control Facility (SC)**
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**Expanded Function Panel (SP)**
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- SP200 Offline Tests
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**Magnetic Tape Adapter (TA)**
- TA100 General Information
- TA200 Offline and Online Tests
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- TA500 Console Messages

**Appendix A. Hexadecimal-to-Binary Conversion**

# Chapter 5. MAP Reference Information
# Disk Storage
# (FA)

## Introduction

This part of Chapter 5 provides maintenance information needed to service the disk storage unit in the 8130, 8140, or 8101. When used with the MAP Maintenance Package, the FA MAP diagnoses disk storage problems and refers you to this part of Chapter 5 for information such as hardware locations, actions, and wiring checks.

This part also contains maintenance information and action plans for diagnosing intermittent problems not found with the MAPs.

This part has five sections:

1. General Information (FA100–FA131) – Contains information on FA configuration, theory of operation, and repair strategy.
2. Offline Tests (FA200–FA250) – Contains disk storage test information, error messages, and actions.
3. Intermittent Failure Repair Strategy, (FA300–FA350) – Contains System Error Log information that you use to service intermittent failures.
4. Signal Paths and Detailed Operational Description (FA400–FA452) – Contains signal path diagrams, wiring and signal paths, and net lists.
5. Adjustment, Removal, and Replacement Information (FA500–FA590) – Contains disk storage service checks, and adjustment, removal, and replacement procedures.

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## Abbreviations

| | |
|---|---|
| ADWA | adapter work area address |
| AGC | automatic gain control |
| ARC | adapter return code |
| CA | channel address |
| (CC) | pseudo for control cable |
| CHCV | channel control vector |
| CHIO | channel input output |
| CIL | condition/incident log |
| CNT | count |
| COMPSTAT | completion status |
| CPR | channel pointer register |
| CRC | cyclic redundancy check |
| (DD) | pseudo for dedicated cable |
| DE | disk enclosure |
| DH | data handler |
| DPCX | Distributed Processing Control Executive |
| DPPX | Distributed Processing Programming Executive |
| DSD | disk storage drive |
| DT | device type |
| ECC | error correction code |
| FAX | pseudo for disk storage card type |
| FCB | function control block |
| FDM | function definition module |
| (FH) | pseudo for fixed head cable |
| FRU | field replaceable unit |
| FRWA | function request work area address |
| GFI | General Failure Index |
| ID | identification |
| I/O | input/output |
| IOEP | I/O interrupt entry point |
| LV | level |
| MAP | Maintenance Analysis Procedure |
| MD | Maintenance Device |
| (MH) | pseudo for moving head cable |
| MI | manual intervention |
| OP | option |
| PA | physical address |
| PCI | program-controlled interrupt |
| PES | position error signals |
| PIO | programmed I/O |
| PLO | phase locked oscillator |
| RES | reserved |
| R/W | read/write |
| rws | read write storage |
| SCA | secondary component address |
| SCF | System Control Facility |
| SCX | pseudo for system control facility card type |
| SEQ NO | sequence number |
| TCC | top card connector |
| TCM | test control monitor |
| UT | unit type |
| VCM | voice coil motor |
| W | pseudo for top card connector row 2 |
| X | pseudo for top card connector row 3 |
| Y | pseudo for top card connector row 4 |
| Z | pseudo for top card connector row 5 |

## FA100 General Information

The 8100 system disk storage drive (Figure FA100-1) consists of a disk enclosure (DE), a drive motor, and a card gate mounted on a subframe. The DE consists of a sealed unit that houses the disks, the access mechanism, and some associated electronics. Three shock mounts inside the 8100 system units fasten the disk drive subframe to the 8130, 8140, or 8101 frame; the frame supplies ac and dc power.

The DE uses either three or six disks stacked on a spindle, and resides within the frame in a horizontal position. These disks rotate at 3125 rpm and provide a 27-ms average access time. The DE provides various byte capacities by using a combination of fixed and movable heads. The DE has a filtered closed air circulation system to prevent read/write head contamination. A voice coil motor controls a pivoted arm actuator that allows read/write heads to be attached.

The DE cannot be repaired in the field, and must be replaced as a FRU. Defective DEs must be returned to the plant of manufacture with the cover seal intact to obtain the maximum credit value.

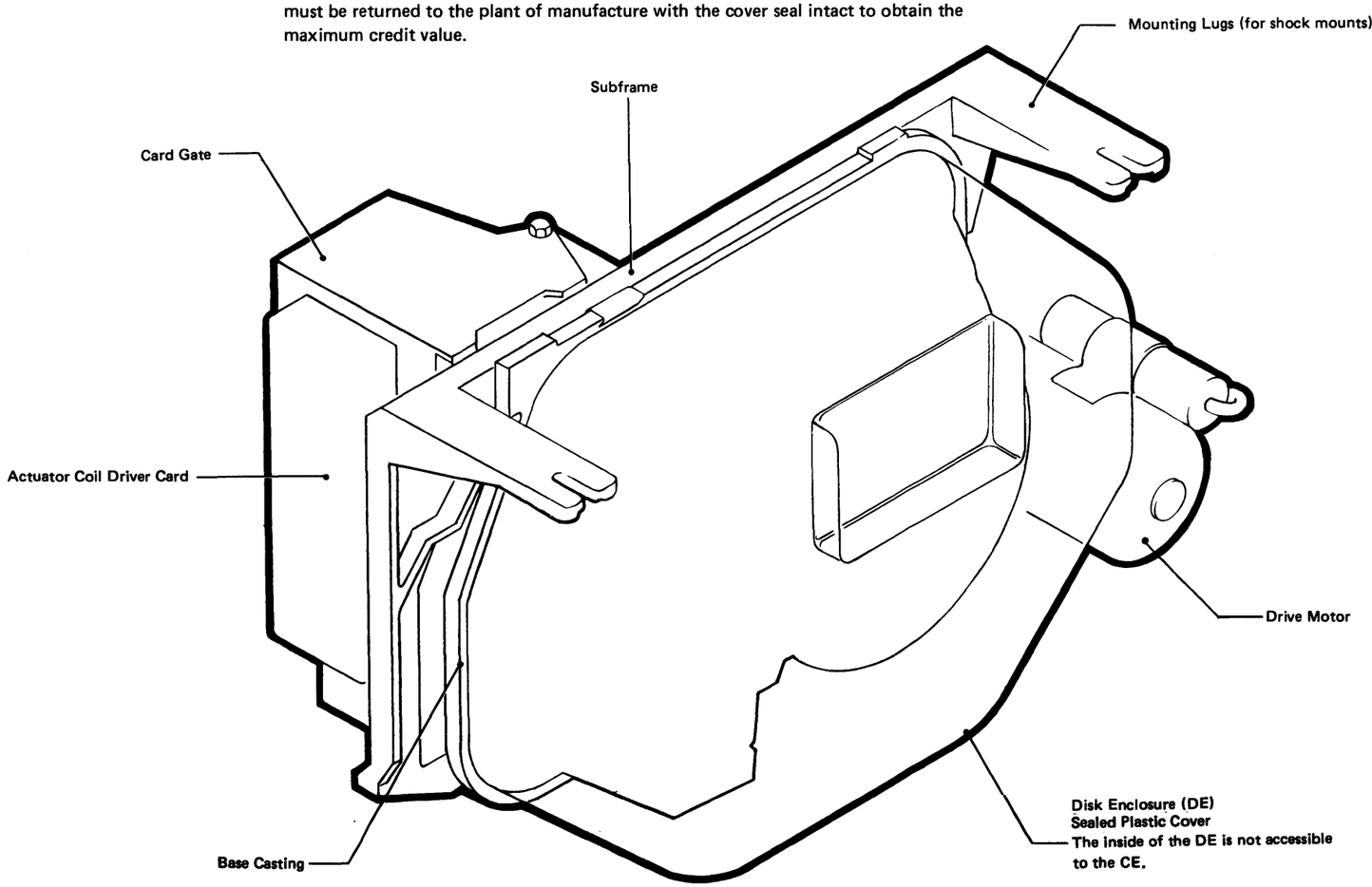



**Figure FA100-1. Disk Storage Drive Basic Diagram**

The following 8100 Information System units contain the disk storage drive (DSD) and adapter:

- IBM 8130 Processor, Models A21–A24.
- IBM 8140 Processor, Models A31–A34, A41–A44, A51–A54, B51, B52, B61, B62, B71, and B72.
- IBM 8101 Storage and Input Output Unit, Models A11, A13, A23, and A25.

Disk storage is available in four configurations giving a storage capacity range from 23 to 64 million bytes of data, as follows:

| Model* | Disk Elements | Moving Head Capacity | Fixed Head Capacity |
|---|---|---|---|
| Ax1 | 3 | 29, 327, 360 bytes | 0 |
| Ax2 | 3 | 23, 461, 888 bytes | 131,072 |
| Ax3 | 6 | 64, 520, 192 bytes | 0 |
| Ax4 | 6 | 58, 654, 720 bytes | 131,072 |
| Ax5 | 6 (2 units) | 64, 520, 192 bytes | 0 |

*x = 1, 2, 3, 4, or 5. There is no model A12 or A14.

| Model* | Disk Elements | Moving Head Capacity | Fixed Head Capacity |
|---|---|---|---|
| Bx1 | 6 | 58, 654, 720 bytes | 131,072 |
| Bx2 | 6 (lower) | 58, 654, 720 bytes | 131,072 |
| | 6 (upper) | 64, 520, 192 bytes | 0 |

*x = 5, 6, 7

## FA110 Components and Addressing

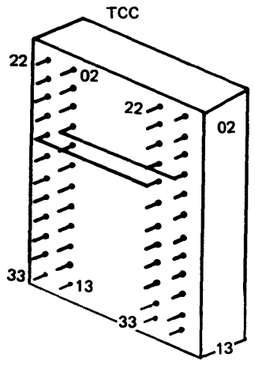
### *FA111 Hardware Components*

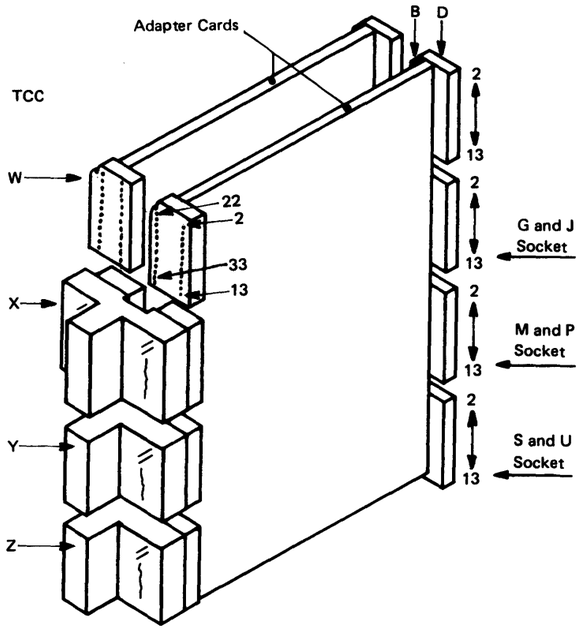
Disk storage consists of two disk storage adapter cards that attach to the PIO bus and a disk storage drive (DSD).

**Disk Storage Adapter Cards**

Two logic cards attach the DSD to the processor through the SC card and the System Control Facility (SCF) bus. These cards plug into the 8130 A1 board, the 8140 A2 or B2 board, and the 8101 A2 board. Connections between the cards are through top card connectors (TCC) W, X, Y, Z and board wiring. Connections between the adapter cards and the DE are through the control cable (CC) and the dedicated cable (DD). See Figures FA111-1 through FA111-4 for the locations of these cards and cables. The cards are:

- FA1 card – Function Control Block (FCB) Processor
- FA2 card – Data Handler (DH)




**Notes:**

1. *04 and 31 pins are ground.*
2. *TCC W, X, Y, and Z are interchangeable with each other, but are not necessarily interchangeable with those of other adapters. For part numbers, refer to Chapter 3, Figures LT140-1, LT140-2, LT240-1, LT240-2, LT240-3, LT240-4, and LT340-1.*

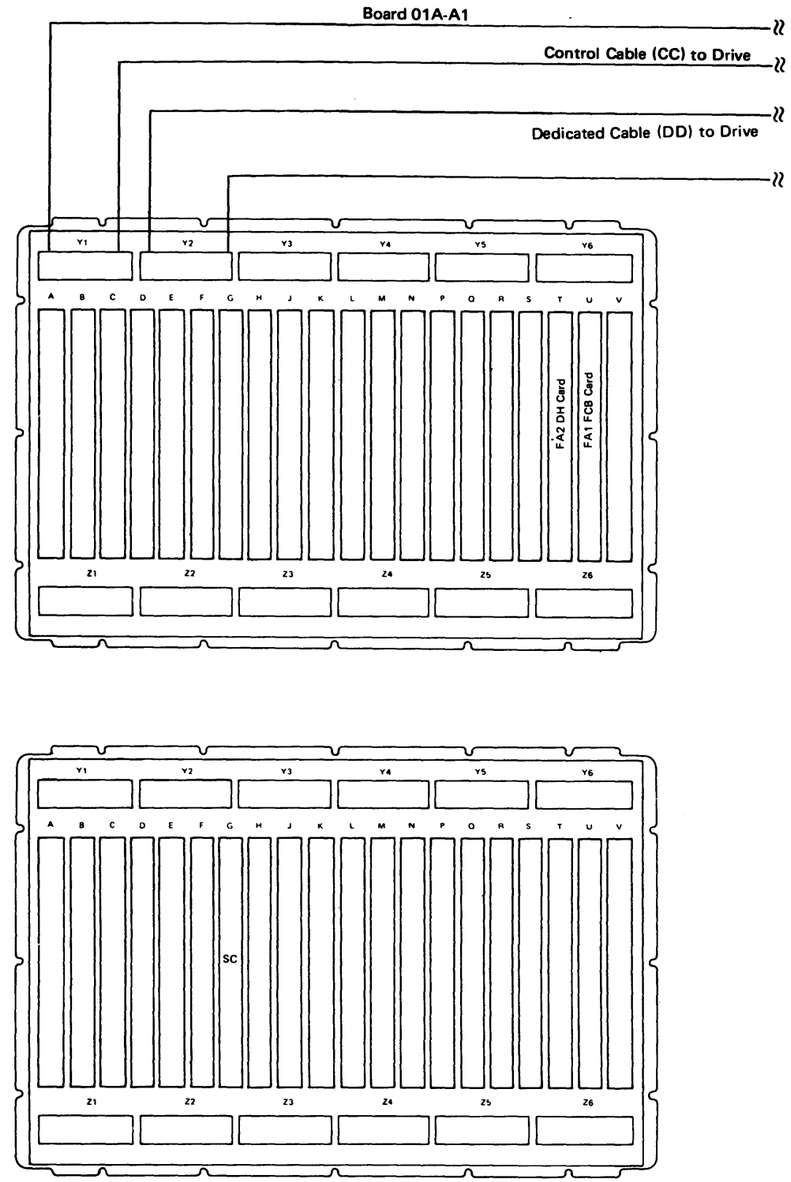
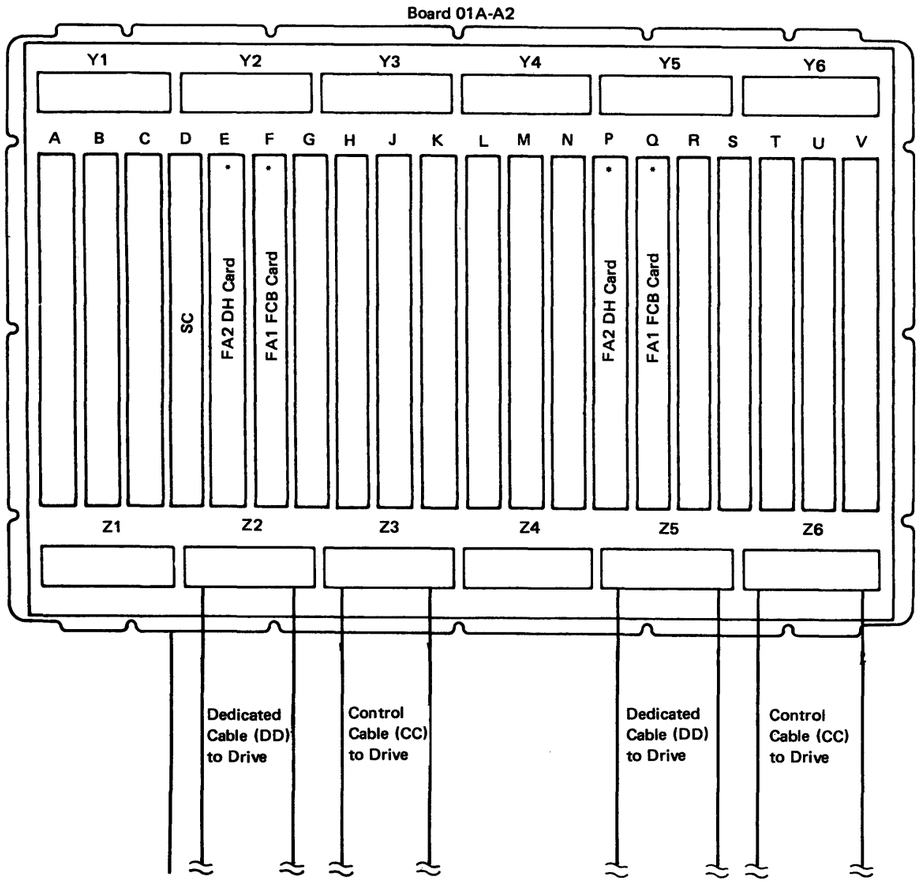



**Figure FA111-1. 8130 Processor Adapter Card Locations**




| Models | Locations* | | | | |
|---|---|---|---|---|---|
| | SC | FA1 | FA2 | (CC) | (DD) |
| A3X/A4X<br>A5X | A2D2<br>A2D2 | A2Q2<br>A2F2 | A2P2<br>A2E2 | A2Z6<br>A2Z3 | A2Z5<br>A2Z2 |

**Figure FA111-2. 8140 Processor Model AXX Adapter Card Locations**

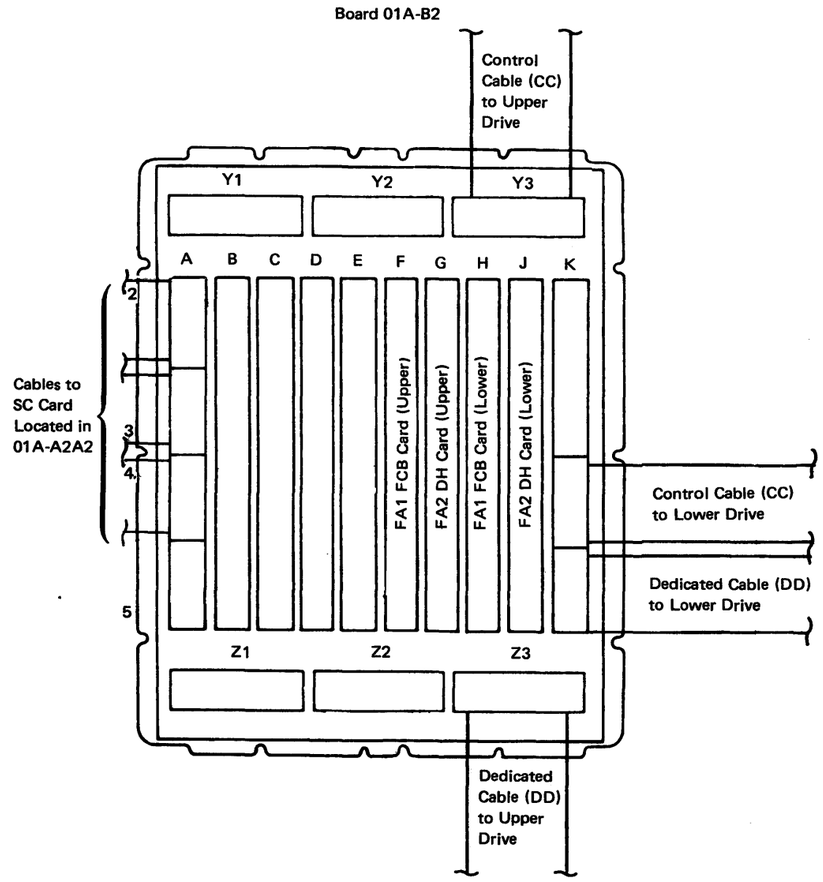



**Figure FA111-3. 8140 Processor Model BXX Adapter Card Locations**

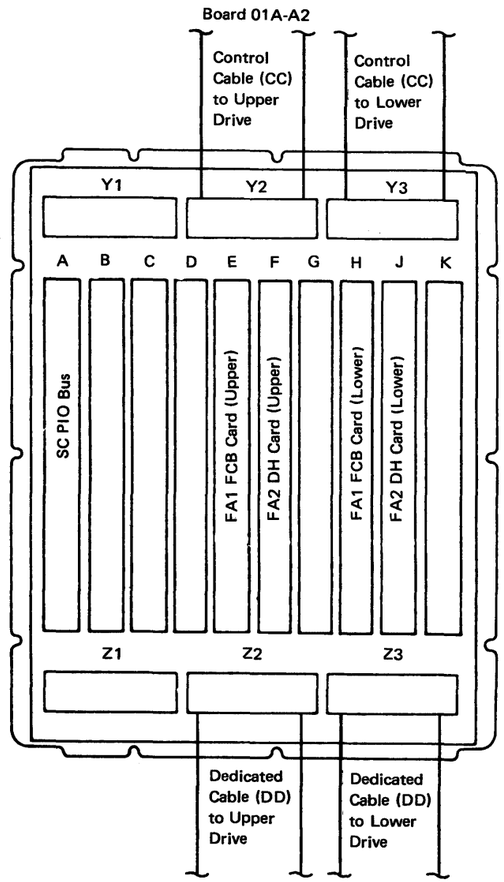



**Figure FA111-4. 8101 Storage and I/O Unit Card Locations**

## Disk Storage Drive (DSD)

The DSD (Figure FA111-5) includes:

- Disk Enclosure (DE) – The actual storage device that contains the disks, R/W heads, and the access mechanism.
- Disk electronics – Six circuit cards plugged in the 01X–A1 board, that is hinge-mounted on the DSD subframe, and one circuit card that is mounted on the card gate. The cards on the A1 board (Figure FA111-5 and FA111-6) are:
  - FA3 card – Data channel card
  - FA4 card – Logic 1 card
  - FA5 card – Logic 2 card
  - FA6 card – Servo 1 card
  - FA7 card – Servo 2 card
  - FA8 card – Voice coil motor (VCM) driver card. (Mounted on the card gate)
  - FA9 card – Terminator card

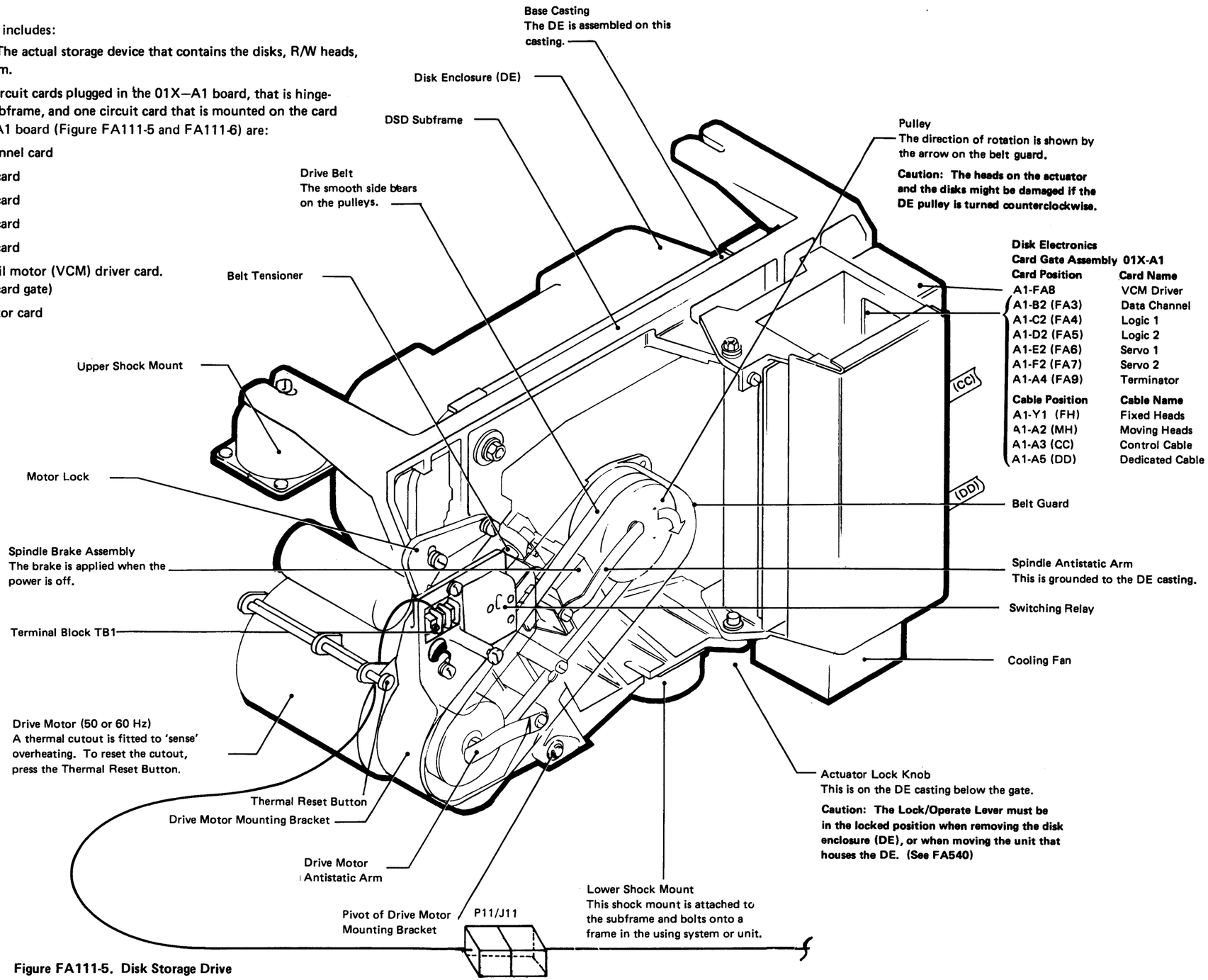



**Figure FA111-5. Disk Storage Drive**

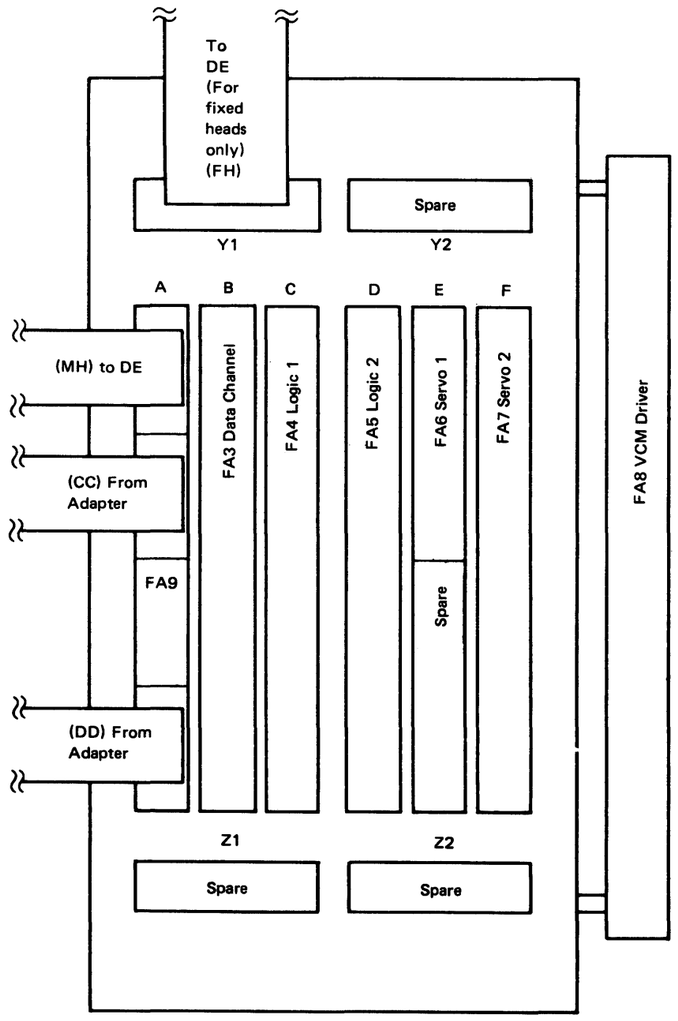



**Figure FA111-6. Disk Storage Drive Logic Board and Card Gate**

### *FA112 Addressing*

The only software addressing needed for the DSD is the physical address (PA) of the adapter cards. No logical address (LA) is necessary since only one device can be attached to a disk storage adapter. The disk storage PA consists of two hex characters. The first character, I/O group address, is determined by switch settings on the associated SCF card (see Chapter 2 for a detailed discussion of addressing) and is assigned according to the location of disk storage. The second character of the address, 0, is fixed by board wiring. For example, the processor disk storage PA is 80 and the first 8101 disk storage PA is 90.

### *FA113 Configuration Table Entry*

LV PA UTUT OPOP OPOP

LV = Level
01

PA = Physical Address
P = I/O Group address – set in the SCF switches
A = Fixed wiring on the board

| Disk Storage Location | PA | |
|---|---|---|
| | Lower | Upper |
| 8130 | 80 | – |
| 8140 | 80 | – |
| 8140 Model BXX | 84 | 85 |
| 1st 8101 | 90 | 91 |
| 2nd 8101 | A0 | A1 |
| 3rd 8101 (8140 only) | B0 | B1 |
| 4th 8101 (8140 only) | C0 | C1 |

UTUT = Unit Type
0020

OPOP =

| Option | Disk Feature | Moving Heads | Fixed Heads |
|---|---|---|---|
| 1000 | 29 Meg | 5 | 0 |
| 2000 | 64 Meg | 11 | 0 |
| 3000 | 23 Meg | 4 | 8 |
| 4000 | 58 Meg | 10 | 8 |

OPOP = 0000

## FA120 Basic Operational Description

The operation of the DSD can be divided into four broad categories:

Seek: Positions selected heads over desired tracks.

Read/Write: Reads or writes data on selected head.

Integrity: Checks device operation and ensures data integrity.

Sense: Provides error and status information to the adapter.

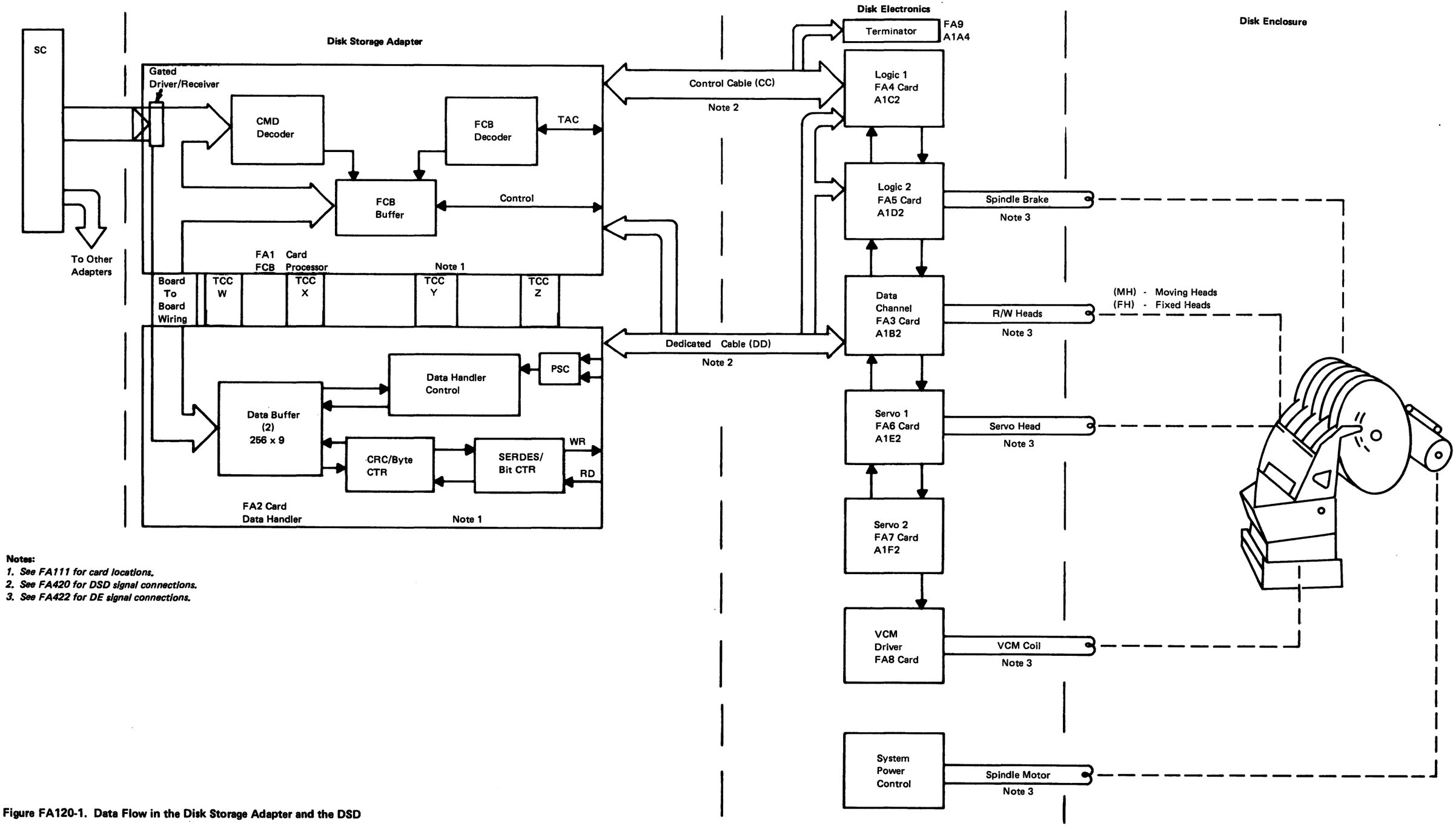
Further categories can be defined for:

Control: Defines signal bus operations between adapter cards and DSD.

Power: Includes motor drive, braking, power on and off sequencing.

Operationally, these categories all interact and cannot normally be separated. However, they are treated separately in the descriptions found in FA450 "Detailed Data Flow".

Figure FA120-1 is a high-level diagram of the data flow in the disk storage adapter and the DSD.




**Notes:**

1. *See FA111 for card locations.*
2. *See FA420 for DSD signal connections.*
3. *See FA422 for DE signal connections.*

**Figure FA120-1. Data Flow in the Disk Storage Adapter and the DSD**

## FA130 DSD Unique Repair Strategy

The General Failure Index (GFI) contained in Chapter 1 provides procedures for initial disk storage fault isolation. If the GFI isolates a problem to disk storage, it directs you to use the maintenance device (MD) to execute the FA MAP contained on test diskette 03 for problem resolution. The primary repair strategy for disk storage problems involves use of the FA MAP offline. If random or intermittent failures occur that cannot be resolved by the MAPs, the MD prompts you to use the intermittent repair strategies, or action plans, contained in FA350.

### *FA131 Disk Storage Unique Intermittent Repair Strategy*

See FA300 for detailed information on intermittent failures. An intermittent failure can be defined as:

- An error occurring so infrequently that it is not detectable by looping the test. Go to FA350 "Action Plan to Correct Intermittent Failures".
- An error occurring at random times (different test error messages occur), thereby making the MAPs ineffective. After the MAPs detect three different test error messages, you are instructed to go to FA350.
- An error that is detected only after looping the diagnostics for more than 5 minutes. Record the test message error number and continue using the FA MAPs. In this case, repair verification will again require looping.

## FA200 Offline Tests

Offline tests check the disk storage operation. They consist of 48 routines on maintenance diskette 03. The offline tests are invoked using the maintenance device (MD), either by the FA MAP or the Free-Lance Option.

- When using the FA MAP, the MAPs invoke the tests as needed.
- Valid offline routines are: 01–47 and 50 (see FA210).
- When using the Free-Lance Option, the following test invocation message must be entered:

  At 80BC, enter PAB.

  At 80BC, enter SLRRB.

  PA = Disk storage address (see FA112)

  S = Sense Option (one character)

  0 = run disk storage adapter tests only

  1 = run disk storage adapter and device tests

  2 = not used by disk storage

  L = Loop Option (one character)

  0 = run selected routines one time

  1 = loop selected routines; stop on error

  2 = loop selected routines; bypass error

  RR = Routine Number (two characters)

  If 00 or no entry is made, all routines will run. If a routine number is entered, only that routine will run.

  B = begin execution, enters the invoke message.

## FA210 Offline Test Routine Descriptions

The offline disk storage tests consist of 48 routines arranged to test the functions within the disk storage in an order that isolates the problem to the most likely failing FRU(s). Routines 01–19 tests the adapter logic (see FA211), and Routines 20–47 and 50 test the drive (see FA212).

Generally, the tests begin by checking the basic functions (for example, I/O instructions) and then progress to checking complex functions (for example, function definition module, FDM, interface).

All I/O instructions that are defined are executed with minimal setup to get predictable results from an I/O instruction. All accessible registers are set to values to verify that each latch of the register can be turned on and turned off.

Error generation tests are included to test the error detection logic. The objective is to have functional errors cause the various status bits (indicating the error) to be turned on. These routines require a somewhat more sophisticated use of an I/O sequence.

A functional exercise of the hardware is done by executing a random program of Seeks, Writing of data, Reading of data, and Reading of IDs. Any errors recorded during this exercise are considered potential solid failures.

All writing of data and IDs is confined to the test cylinder (cylinder 359). Reading data is also confined to the test cylinder and the fixed head area. Reading IDs is unrestricted. There are cases in which the error is displayed while a bad ID exists (on the test track of head 1 only). A normal termination of the test (such as a FREE or BEGIN) clears the bad ID. Since the possibility of an abnormal end to a test exists (such as, loss of power), the Operational Format Utility must be used to restore the correct IDs. Errors that could cause a bad ID condition are:

| Routine | Error Numbers |
|---|---|
| 27 | 13, 14, 15 |
| 29 | 16, 17, 18, 19, 1A, 1B |
| 30 | 13, 14, 15, 16, 17 |
| 32 | 13, 14, 15, 16, 17 |
| 33 | 13, 14, 15, 16, 17 |
| 34 | 13, 14, 15, 16, 17, 18, 19 |
| 35 | 13, 14, 15 |
| 36 | 13, 14, 15 |
| 46 | 10, 11, 12, 13 |
| 50 | 11 |

**Note:** *After FRU replacement, depending on the nature of the problem, the disk surface may contain bad data, thus preventing a good verification run. When this occurs, it may be advisable to run the Operational Format Utility.*

*Also, these failures may have resulted in bad data on the customer/user area, requiring re-creation of the data by the user and possibly reformat (IDs) of the defective area by use of the utilities. Affected areas are tracks 0, 1, and 128 of head 1, fixed heads, and the CE cylinder (359).*

*FA211 Adapter Logic Offline Test Routine Descriptions*

**Routine 01.** Tests the adapter reset command by checking all registers reset by the command for correct reset values. The registers tested are: basic status, FCB processor status, seek status, burst register, first value register, next function request register, data CHCV, FCB CHCV, and seek register.

**Routine 02.** Tests the basic status register and the commands that modify the register (set/reset basic status under mask, read basic status).

**Routine 03.** Tests the next function request register. The register is reset and written to all 1's and then all 0's. The state of the NFR register is tested after each write.

**Routine 04.** Tests the seek register and the commands that modify the seek register. The seek register is reset then written with all 1's plus the recalibrate bit. It is then read for the correct state. Next the seek register is written with all 0's and tested for the correct state.

**Routine 05.** Tests the FCB channel control vector and the commands that modify the CHCV. It is written first to all 1's and then to all 0's and tested for the correct state.

**Routine 06.** Tests the data channel control vector and the commands that modify the CHCV. It is written first to all 1's and then to all 0's and tested for the correct state.

**Routine 07.** Tests the first value register and the commands that modify the register. It is written first to all 1's and then to all 0's and tested for the correct state in each case.

**Routine 08.** Tests the initiate command and basic FCB operation. Prior to the first command being issued in this test, the PA80 channel hang message is outputted on the invoking device. This message is overlaid by the test before it is seen unless a Channel Hang condition really exists. This precaution is necessary as this routine transfers data between the processor storage and the adapter. The test issues the initiate command with the adapter disabled and checks the CHCVs. The adapter is then enabled and an FCB of 'NO–OP' is processed. Again the CHCVs are tested.

**Routine 09.** Tests for an FCB timeout error. The error is generated in the routine. The test executes an FCB with channel request inhibited. Basic status and seek status are compared.

**Routine 10.** Verifies that a program-controlled interrupt can be executed and that an interrupt is generated. The adapter is enabled and an FCB of 'NO–OP, PCI' is processed. Basic status is checked to ensure that an interrupt occurs.

**Routine 11.** Tests the store memory control FCB command. The adapter is enabled and an FCB is processed for the SMC subcommand. Basic status is checked as well as the appropriate channel pointer registers.

**Routine 12.** Is an extended test of a program-controlled interrupt. It insures that PCI alone sets the interrupt bit. The adapter is enabled but file interrupts are disabled. An FCB of 'PCI,NO–OP,SMC,NO–OP' is processed and basic status is checked for an interrupt.

**Routine 13.** Tests that interrupt is set when device error is set. The adapter is enabled with file interrupts disabled. The device error bit is set in basic status and the basic status register is checked for an interrupt.

**Routine 14.** Tests that all invalid PIO commands generate equipment checks. The adapter is enabled and each invalid command is issued. Basic status is then compared for the correct setting.

**Routine 15.** Tests the file reset command. A reset file command is issued and basic status is checked for all 0's.

**Routine 16.** Tests the FDM initialization of the file. The FDM initialization function request is issued followed by a request to the FDM to read basic status. FDM return codes are checked after each function.

**Routine 17.** Tests the load burst count, store new track, and load sector count FCB commands. FCB's of 'SNT,LSC,LDburst' are processed. The residual count register, seek register, and burst register are read and tested for the appropriate status.

**Routine 18.** Tests the adapter data buffers for the ability to retain 1's and 0's. FCBs are processed to write and read both data buffers in the adapter and the data received is compared with what is expected.

**Routine 19.** Tests the adapter data buffer for parity check generation. A parity check is generated in the data buffer, and FCB is processed to write data into buffer 1 with odd parity, a second FCB is processed to read the data with even parity, and data handler basic status bit 1 (data handler error) is checked to see that it is set.

**Routine 20.** Tests the recalibrate FCB command and file recalibrate. The ability to read the file sense is also tested. FCBs are processed to recalibrate and to read file status; status is checked after each to ensure correct setting. This routine checks the control sample pulsing logic by issuing 32 requests for file sense. After each request, a check is made to ensure the index/sector bit is on. This routine also tests the file rotational speed bit in the adapter basic status. Bit 1 of the data handler extended status (file speed ok) is checked to ensure that it is on.

**Routine 21.** Tests the ability of the file to wrap data on the cable. FCBs are processed to recalibrate, read file status, and to perform file wrap. Status is checked after each to ensure correct setting.

**Routine 22.** Tests the read ID immediate command. FCBs are processed to perform recalibrate, read ID immediate, and to store new track (359) followed by a read ID immediate. Status is checked to ensure operations were performed correctly.

**Routine 23.** Tests the seek command and file arm movement. The test includes a seek from cylinder 0 to cylinder 1 to cylinder 0. The seek controls are tested. FCBs processed are: recalibrate; seek head 1, cylinder 001; read ID immediate; seek head 1, cylinder 000; file sense; and read ID immediate. Status is checked after each operation.

**Routine 24.** Tests servo calibration. FCBs processed are: recalibrate; seek head 1, cylinder 128; and recalibrate. Status is checked after each operation.

**Routine 25.** Tests write data, read data, and readback check FCB commands. FCBs processed are: recalibrate; seek head 1, cylinder 359; read ID immediate; write sector; read file status; read sector; read file status; (compare data); readback check. Status is checked after each operation. This routine performs 64 cycles of all operations excepting the initial recalibrate.

**Routine 26.** Tests the ability of the file control electronics to read the IDs of all heads according to model. A recalibrate is issued first: then each moving head that is installed (figured from Test Control Monitor (TCM) configuration option byte) is tested using a seek, read ID normal, and write sector. Each fixed head present is tested using a seek, SNT, and read ID normal.

The configuration definitions are (from TCM option byte):

| **Offline Use Option Byte** | **Definition** | |
|---|---|---|
| 10 | 5 moving heads | (29M) |
| 20 | 11 moving heads | (64M) |
| 30 | 4 moving heads and 8 fixed heads | (23M) |
| 40 | 10 moving heads and 8 fixed heads | (58M) |

**Routine 27.** Tests sector ID flags. The following FCBs are processed: recalibrate; seek head 1, cylinder 359; read ID immediate; write,read ID; (set ID flag bit); write,read ID; and read residual count register. Status is checked after each operation.

**Routine 28.** Tests the multisector operation of the file. The file is exercised with skip factors of 1, 2, 4, and 8. For each skip factor, sector counts of 2, 4, 8, 16, 32 and 64 are used. The test proceeds as follows: recalibrate, seek (cylinder 359), read ID immediate, write sector, read sector, set skip factor and sector count, load sector count, read sector, test buffer areas for correct data. The test is looped until all of the combinations of sector count and skip factor have been tested. After each operation, status is checked to ensure all correct conditions exist.

**Routine 29.** Tests the format and retrieve FCB commands. This routine first performs a recalibrate, seek (359), and read ID immediate. The ID is saved. Next the routine performs a write sector, read sector, and retrieve. The retrieved data is then checked. A format (FFFF) is then performed on the sector. A read sector is performed and the data compared for hex FF. Next a format (0000) is performed. A read sector is executed and the data compared for hex 00. The ID is restored. Status is checked after each operation.

**Routine 30.** Tests the read displaced ID and write displaced ID FCB commands. The test first does a recalibrate, seek (359), and a read ID immdediate. The ID is saved. Next, FCBs are issued to write displaced ID, read displaced ID, and read ID normal. The ID is restored. Status is checked after each operation. Reformatting is done to clean up the data file.

**Routine 31.** Performs extended testing of the recalibrate command. After a recalibrate and seek (359) is performed, a read ID immediate is performed. Status is checked after each operation.

**Routine 32.** Tests that the adapter can generate an ID error. The error is indicated in the basic status by attempting to write to a defective sector. First a recalibrate, seek (359), and read ID immediate are performed. The ID is saved. A write ID is performed to set defective sector. A write sector is then attempted and should fail. The proper error codes are checked. The ID is restored. Status is checked after each operation.

**Routine 33.** Tests that the adapter can generate an ID error by accessing a sector with an incorrect ID written on the file. The routine does a recalibrate, seek (359), and read ID immediate. The ID is saved. A write ID normal is done with a bad ID field. A read ID normal and read sector are issued. The appropriate error conditions are checked. Status is checked after all operations. The good ID is restored.

**Routine 34.** Tests that the disk adapter can generate a data field error indication in the basic status. The error is generated by attempting to write data to a protected sector. FCBs are processed as follows: recalibrate, seek (359), read ID immediate. The ID is saved. Next, FCBs are processed for write sector, write ID (protected), read ID normal, write sector normal, and read sector normal. Proper status is checked after each operation. The good ID is restored.

**Routine 35.** Tests that the disk adapter can generate a CRC error and an ID error. This is done by reading an ID with bad CRC. The routine creates and restores the ID. FCBs are processed for recalibrate, seek (359), and read ID immediate. The ID is saved. The sector is formatted with the CRC bad for that ID. A read sector normal is performed. Proper status is checked after each operation. The good ID is restored.

**Routine 36.** Tests that the disk adapter generates a CRC error and a data field error in the basic status. This is done by reading data sector with bad CRC. This routine creates the bad CRC and restores a good CRC at completion. A recalibrate, seek (359), and read ID immediate are issued and the ID is saved. The sector is formatted with bad data CRC. A read sector FCB is processed. The original good ID is restored. Two write sectors are performed. Status is checked after each operation for the correct setting.

**Routine 37.** Tests that the disk adapter generates a sector not found error in the basic status. This is done by attempting to access sector numbers beyond the valid range. A recalibrate, seek (359), and read ID immediate are issued. Next, a readback check is issued for an invalid sector. The readback check is looped for sector addresses 42—7F.

**Routine 38.** Tests that the disk can generate a multisector error indication. This routine writes multiple sectors so that a count remains in the residual count register. A recalibrate, seek (359), read ID immediate, and write sector are issued. An FCB for load sector count and read multiple sector is issued. Status is checked after each operation.

**Routine 39.** Tests that the adapter can generate a file error indication in the basic status and FCB processor status. This is done by sending the file a control byte with even parity. A recalibrate, seek (359), and read ID immediate are issued. Next, an FCB is processed to send a control byte with even parity. Status is checked after each operation.

**Routine 40.** Tests that the disk adapter generates a file error indicated in the basic status and the FCB processor status. This is done by sending the file an address larger than the maximum for the file. A recalibrate, seek (359), and read ID immediate are issued. Next, a seek for cylinder 511 is issued. Status is checked after each operation.

**Routine 41.** Tests that the disk adapter can generate a control bus parity error in the basic status and the FCB processor status. This is done by writing a control byte to the file with odd parity and reading it back with even parity. One FCB is processed which writes the control byte odd and reads it back even. Status is checked for the error when the operation is completed.

**Routine 42.** Tests that the disk adapter can generate a command error indication in the basic status and the seek status register. This is done by issuing a diagnostic write command when the FCB processor is busy. A recalibrate, seek (359), and read ID immediate are issued. An FCB is then processed with seek, PCI, seek, and SMC commands chained. The PCI causes an immediate return to the driver. At this time the diagnostic write is issued. Status is checked after each operation.

**Routine 43.** Tests the ability of the file control electronics to access random cylinders and heads, and to read the track IDs according to model. An FCB is processed to: issue recalibrate, seek (128), recalibrate, seek (359), and read ID immediate. Next, an FCB is processed to perform 73 random seeks followed by a read ID normal on different cylinders on all heads (1—4). Status is checked after each operation.

**Routine 44.** Performs a seek speed test by doing a recalibrate, a seek (359), and a read ID normal (PSC = 0). An FCB is then issued and timed while performing four seeks, alternating between cylinder 0 and cylinder 359. The seek speed is checked for a ±15% tolerance. The speed constants are adjusted for each processor.

**Routine 45.** Tests the file rotational speed bit in the adapter basic status and then verifies that the speedbit functions correctly. The test issues a recalibrate, a seek (359), and a read ID normal (PSC = 0). The routine is then delayed about 10 ms (about 1/2 of a revolution). The routine then issues a read ID normal (PSC = 0) and times the operation. The next time PSC 0 comes under the head should be near 9.2 ms. One revolution takes exactly 19.2 ms. The speed is then checked for a +/— 10% tolerance. The speed constants are adjusted for each processor.

**Routine 46.** Ensures that a multisector write of IDs only writes requested IDs. The test performs a recalibrate and then a seek to head 1 of the CE track. The test then writes two IDs using a multisector write operation. The IDs are read and compared to ensure that the write worked. Next, all IDs on the disk are checked to ensure that only the requested writes were performed. Status is checked after each operation.

**Routine 47.** Ensures that a multisector read of 32 data sectors are processed within approximately 40—60 ms. The test first issues a recalibrate and then a seek to head 1 of the CE track. The test then reads 32 sectors using a multisector retrieve. The expired time is tested. Status is checked after each operation. Speed constants are adjusted for each processor.

**Routine 48.** Checks that the DSD subsystem can successfully process multisector write operations. The routine processes Recalibrate, Seek (cylinder 359), and Read ID Immediate FCBs. Next, the routine issues Multisector Writes for skip factors 1, 2, 4, and 8, with a count of 2. Finally, the routine loops 10 times issuing a Multisector Write for skip factor 2 with a count of 64. After each operation, status is checked to ensure all correct conditions exist.

**Routine 50.** Performs a checkout of the fixed heads. No data is written in the sector fields under a fixed head; however, the write circuitry of each fixed head is tested by writing IDs. These IDs are rewritten correctly by the test. If an error condition causes a bad ID to remain under a fixed head, reformatting of that track should resolve the problem. The customer data under a fixed head should then be available, as previously, to the test. This routine processes one FCB that performs seek, read ID, write ID (error), read ID (to test), and restore ID operations.

The configuration definitions are (from TCM option byte):

**Offline Use**

| Option Byte | Definition | |
|---|---|---|
| 10 | 5 moving heads | (29M) |
| 20 | 11 moving heads | (64M) |
| 30 | 4 moving heads and 8 fixed heads | (23M) |
| 40 | 10 moving heads and 8 fixed heads | (58M) |

## FA220 Not Used

## FA230 Test Message Formats and Status Information

The formats of the output messages are:

| Format | Content | Bytes |
|---|---|---|
| 1 | YYBC | 02 |
| 2 | PAZZ | 02 |
| 3 | PAXE RREN CCMO | 06 |
| 4 | PAXE RREN RCVD EXPD | 08 |
| 5 | PAXE RREN FSTB AFAP BFBP CFCP SSFE HSBS HER1 R200 | 20 |

**Legend**

YY — System message number
BC — Indicates a system error
PA — Disk storage physical address
ZZ — MI number
X = 1 — Indicates that PA is the adapter address
X = 2 — Indicates that PA is the device address
E = E — Indicates that this is an error message
RR — Routine number
EN — Error number
CC — One byte of command code (current PIO operation)
MO — One byte of error modifier data defined by failure description
RCVD — Two bytes of received data defined by error description
EXPD — Two bytes of expected data defined by error description
FS — One byte of file status
TB — One byte of wrap fail status (00 = good, 80 = fail)
AF — One byte of file sense 1 (101)
AP — One byte of file pulsing 1 (101)
BF — One byte of file sense 2 (110)
BP — One byte of file pulsing 2 (110)
CF — One byte of file sense 3 (111)
CP — One byte of file pulsing 3 (111)
SS — One byte of seek status
FE — One byte of FCB processor extended status
HS — One byte of data handler basic status
BS — One byte of adapter basic status
HE — One byte of data handler extended status
R1 — One byte of next function request register, part 1
R2 — One byte of next function request register, part 2
00 — One byte of hex 00 for pad

**Note:** *When entering test error messages (as in menu selection 'C'), spaces must not be entered as shown in the above format.*

### *FA231 Offline Adapter Test Message Formats*

The adapter tests use only formats 1, 2, 3, and 4.

### *FA232 Drive Test Message Formats*

The disk drive tests use all the formats (1, 2, 3, 4, and 5)

### *FA233 Status and Sense Byte Formats*

**File Status (FS) Byte (Tag 100)**

| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| File Status (FS) | Fixed Head Not Selected | Brake Applied * | Track Not Avail * | Command Error * | Data Unsafe * | Seek Inc | Home | Not Ready * |

**Note:** *The active condition of any bit is a 1.*

*Bits with an asterisk indicate error conditions when they are set to a 1. All other bits indicate DSD status at the time the adapter sampled the status register.

**Bit 0 — Fixed Head Not Selected.** This bit is set to 1 at the conclusion of a seek, power-up, recalibrate or moving head select. This bit is set to 0 at the conclusion of a fixed head select operation, even if fixed heads are not present.

**Bit 1 — Brake Applied.** This bit is set if the brake coil is no longer energized and the brake is applied. It provides sense information for the fact that the dedicated line 'brake applied' was activated. The DSD powers down within 5 seconds of the brake applied line being active.

**Bit 2 — Track Not Available.** If a command requires the DSD to access an invalid cylinder (valid cyclinders are 0 to 359), then an interrupt is given and this sense bit set. The actuator will not move. This bit is reset after a seek tag sequence with a valid address.

**Bit 3 — Command Error.** This sense bit is set when the DSD detects a parity error on either the control bus or tag lines, or an invalid tag code. An interrupt is then generated. The resulting sense cycle clears the interrupt caused by a tag error. In this case, 'reset error' must be activated followed by a further sense command to clear the interrupt as tag parity error removes confidence in control and sense cycle communication. Correct parity is presented on the control bus by the DSD even after a 'command error' is detected. Cylinder and head address is checked after a command error before a write operation is performed.

**Bit 4 — Data Unsafe.** Certain conditions can occur during read/write operations which may change/risk customer data. A 'data unsafe' incident may result in loss of a maximum of one sector of customer information. These conditions are monitored by the DSD and their occurrence will result in an interrupt. Write current is immediately inhibited at source and all data heads are deselected by the DSD. All system commands except the sense command are ignored. The DSD adpater reselects the appropriate head after resetting an unsafe condition.

The following conditions result in 'data unsafe' being set:

Write or read and multiple module selection error

Write and data servo unsafe

Write and no write transitions

Not write and write current detected

Write and not on track and moving head selected

Write and read. If write and read commands overlap by 10 ns or more, 'data unsafe' is set.

Write and head short circuit to ground indication

Write and moving head selected during sector pulse. Can only write in the data areas.

Write and 'not ready'

'Reset error' in all cases clears the 'unsafe condition'.

**Bit 5 — Seek Incomplete.** This sense bit is set when any access, recalibrate, or moving head select operation is in process. (This bit is not relevant to fixed head seeks.) This bit is also set by 'not ready'. A read, write, or moving head seek operation must not be attempted with the bit active. A sense cycle performed during an access will correctly indicate 'seek incomplete'. If this bit is still set after the access should have been completed, then a recalibrate may be performed.

**Bit 6 — Home.** This bit is set at the end of a successful power-up sequence or recalibrate operation; the actuator is at cylinder 0 with moving head '00001' selected. An interrupt is then issued and the resulting sense command indicates 'home'. A normal access to cylinder 0 will not cause a 'home' indication. If 'home' is not indicated after a powerup or a recalibrate, then a recalibrate should be performed.

'Home' is reset when the next tag code '001' is issued.

**Bit 7 — Not Ready.** The DSD indicates 'not ready' for any of the following reasons, and will issue an interrupt:

- 'Seek' operation not completed within 1.7 seconds.
- 'Invalid move' is active. The internal DSD latch 'invalid move' detects actuator motion which is not in response to an access command or an attempt to write on moving heads during an access operation.
- The PLO is out of synchronization for any reason including loss of disk speed.
- Disk not moving.
- Oscillator not running.
- Not 'power OK'.
- Excessive noise on the +24V line.
- Servo unsafe.
- 'Power good' pulsing (should be a solid level).
- The wires on the top right voltage connector on the C gate are pulled out or not making connection.

This bit is reset by a recalibrate operation. If 'brake applied' is on, do a power-down/power-up sequence. If the recalibrate is successful, then a 'reset error' completes the error recovery.

**File Sense (AF) Byte 1 (Tag 101) and File Pulsing (AP) Byte 1**

| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| File Sense 1 (AF) | On Track | Linear Region Pulse | Ind/ Sect | Out Direct | Not Out Drive | Not In Drive | Tag Pty Error | Velocity Profile Error |
| File Pulsing 1 (AP) | X | X | X | X | X | X | X | X |

X = 0: Not pulsing
= 1: Pulsing

**Note:** *Active sense and pulsing bits are set to a 1. An active pulsing bit indicates that the associated sense bit changed state while it was being sampled 256 times. Thus, the sense bit is intermittent and not valid.*

*Bit description is the condition when an active (set to "1") pulsing bit indicates that, after being repetitively sampled 256 times, the associated sense bit has changed state (pulsing). Another way to state it is, if the pulsing bit is set, the condition of the associated sense bit has no valid meaning.*

**Bit 0 — On Track.** Is normally set when the actuator is on track (within 10% of track center). It is reset if the actuator deviates from the center of the track by 10% (as defined by 'servo sample').

**Bit 1 — Linear Region Normal and Even.** Changes state when the actuator crosses a track. The level is +5V for an even track and 0V for an odd track. The line normally pulses when on track.

**Bit 2 — Index and Sector Pulses Missing.** Is normally reset indicating that index and sector pulses are present.

**Bit 3 — Out Direction.** Indicates the direction of seek.

**Bit 4 — Not Out Drive, Bit 5 — Not In Drive.** These bits indicate the logic level of the voice coil drives respectively 'out' and 'in':

| Bit 4 | Bit 5 | Meaning |
|---|---|---|
| 0 | 0 | The actuator drive is turned off and the actuator is being pushed in by return spring. |
| 0 | 1 | The actuator is being accelerated outwards. |
| 1 | 0 | The actuator is being accelerated inwards. |
| 1 | 1 | The actuator is either on track or setting on track at the end of an access. |

**Bit 6 — Tag Parity Error.** Is set if the DSD receives other than tag codes '001' to '111' with correct parity. It is reset by 'reset error'.

**Bit 7 — Velocity Profile Error.** Is set by an internal test on the DSD circuits, which sets the instantaneous velocity of the actuator. It is reset by 'reset error'.

**File Sense (BF) Byte 2 (Tag 110) and File Pulsing (BP) Byte 2**

| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| File Sense 2 (BF) | Behind Home | Missing Clocks ÷ 2 | Not Missing Clock Error Latch | Coil Current Low | Missing Servo Signal | Off Data Track | Not Missing Position Error Signal | CTR 5 In Sync |
| File Pulsing 2 (BP) | X | X | X | X | X | X | X | X |

X = 0: Not pulsing
= 1: Pulsing

**Note:** *Active sense and pulsing bits are set to a 1. An active pulsing bit indicates that the associated sense bit changed state while it was being sampled 256 times. Thus, the sense bit is intermittent and not valid.*

*Bit description is the condition when an active (set to "1") pulsing bit indicates that, after being repetitively sampled 256 times, the associated sense bit has changed state (pulsing). Another way to state it is, if the pulsing bit is set, the condition of the associated sense bit has no valid meaning.*

**Bit 0 — Behind Home.** Is set when the DSD actuator is over a cylinder between the landing zone and track 0. This bit is reset when the actuator is outside cylinder 0.

**Bit 1 — Missing Clocks ÷ 2.** Changes state every time a 'missing clock' is detected. Missing clocks are used to code positional information on the director servo surface.

**Bit 2 — Not Missing Clocks Error Latch.** Is normally set. It is reset when six consecutive missing clocks are detected. It is set by 'reset error'.

**Bit 3 — Coil Current Low.** Is set when the coil current is below a threshold level. It is reset by 'recalibrate'.

**Bit 4 — Missing Servo Signal.** Is set if the amplitude of the signal from the dedicated Servo Read is too small for the DSD electronics to use. The bit is reset by 'reset error'.

**Bit 5 — Off Data Track.** Indicates the servo is off track, as defined by the 'servo sample', by plus or minus 10%. Bit 5 is reset by 'recalibrate'.

**Bit 6 — Not Missing Position Error Signals (PES).** Indicates that the PES reference signals used by the actuator when accessing and following a track are correct. It is set by 'recalibrate'.

**Bit 7 — Counter 5 In Sync.** Indicates that the phase locked oscillator (PLO) in the DSD is in synchronism.



**File Sense (CF) Byte 3 (Tag 111) and File Pulsing (CP) Byte 3**

| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| File Sense 3 (CF) | Not Shift | Not (Off Track and Write) | Inside AGC Window | Not AGC Freeze | Demod Pulsing | Not (Read and Write) | Not (Servo Protect and Write) | Invalid Move |
| File Pulsing 3 (CP) | X | X | X | X | X | X | X | X |

X = 0: Not pulsing
= 1: Pulsing

**Note:** *Active sense and pulsing bits are set to a 1. An active pulsing bit indicates that the associated sense bit changed state while it was being sampled 256 times. Thus, the sense bit is intermittent and not valid.*

*Bit description is the condition when an active (set to "1") pulsing bit indicates that, after being repetitively sampled 256 times, the associated sense bit has changed state (pulsing). Another way to state it is, if the pulsing bit is set, the condition of the associated sense bit has no valid meaning.*

**Bit 0 — Not Shift.** Indicates that the position of the actuator agrees with the desired cylinder address given in the previous tag 2, tag 1 sequence. Indicates that a seek command is not in progress.

**Bit 1 — Not (Off Track and Write).** Indicates that the DSD is not trying (erroneously) to write when off track. The bit is set by 'reset error'.

**Bit 2 — Inside AGC Window.** Indicates that signal from the selected head is of sufficient amplitude to be used by the head-position control circuits. (Does not apply if non-existent head is selected.)

**Bit 3 — Not AGC Freeze.** Indicates that the AGC freeze line pulses correctly once per sector.

**Bit 4 — Demod Pulsing.** Indicates that part of the position-detection electronics is working correctly. This bit should normally be pulsing.

**Bit 5 — Not (Read and Write).** Indicates that the DSD is trying to read and write at the same time.

**Bit 6 — Not (Servo Protect and Write).** Indicates that the DSD is trying to write between sectors.

**Bit 7 — Invalid Move.** Indicates that the servo head in the DSD has been offset by more than half a track from its normal position without a seek request. It is reset by 'recalibrate'.

**(FA233 Cont)**

**Seek Status (SS)**

| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 6 7 |
|---|---|---|---|---|---|---|
| Seek Status (SS) | Tag Seq Error | CMD Error | FCB Proc Error | FCB Time Error | Cable Cont OK | Seek Status |

**Notes:**

1. *The status bits are set to 1 when active.*
2. *Bits 0, 1, and 2 are set to indicate errors that occur during an operation between the adapter and the processor. Bit 3 is set to indicate an error that occurs during an operation between the adapter and the file.*

**Bit 0 — Tag Sequence Error.** Indicates that the adapter received the improper interface sequence from the processor. This bit is set when:

1. Two adapters are addressed at the same time.
2. The file detects the TC tag.
3. An invalid tag sequence of the I/O, TA, TD, and channel grant tags is detected.

This bit sets adapter basic status (BS) bits 5 and 7.

**Bit 1 — Command Error.** Indicates that the adapter received an invalid command or command parity error from the processor. This bit is set when:

1. The adapter receives an invalid command.
2. The adapter receives a valid command with bad parity.
3. An initiate signal is issued to the adapter and it is busy.
4. The adapter receives an invalid command when adapter basic status bit 3 (busy) is on.

This bit sets adapter basic status (BS) bits 5 and 7.

**Bit 2 — FCB Processor Error.** Indicates an internal parity error within the FCB processor card. This bit, which is set during TA or TD time of the I/O command, sets adapter basic status (BS) bits 1, 5, and 7.

**Bit 3 — FCB Timeout Error.** Indicates the adapter is busy and more than 2 seconds have elapsed between channel requests to the processor. The 6-1/2 second single-shot has expired (this single-shot is started when the start signal is issued to the adapter). (This may not be an error if the system code has disabled interruptions.) This bit sets adapter basic status (BS) bits 1 and 7.

**Bit 4 — Cable Continuity OK.** Bit is set as long as continuity is complete through the adapter and drive cards; all must be properly seated. This line does not go through the file cards (see FA522). This line is +3V when good.

**Bit 5, 6, 7 — Seek Status.** Indicate seek status of file.

| 5, 6, 7 | Activity |
|---|---|
| 0 0 0 | No MHS, FHS, or RECAL in progress. |
| 0 0 1 | RECAL begun and not yet completed. (Not seek complete.) |
| 0 1 0 | FHS begun and not yet completed. NO MHS or RECAL in progress. (Not seek complete.) If FHS is not complete in 52 ms, 'seek incomplete' is set. |
| 1 0 0 | MHS begun and not yet completed. No FHS or RECAL in progress nor begun after MHS. (Not seek complete.) |
| 1 0 1 | MHS begun then FHS begun. FHS completed and MHS not completed. (Not seek complete.) |
| 1 1 0 | MHS begun then FHS begun. Neither completed. (Not seek complete.) |
| 1 1 1 | MHS begun then FHS begun. MHS completed and FHS not completed. No data is transferred until FHS is complete. |

MHS — Moving Head Seek
FHS — Fixed Head Seek
RECAL — Recalibrate

**FCB Processor Extended Status (FE)**

| Bit Position | 0 | 1 | 2 3 4 5 6 7 |
|---|---|---|---|
| FCB Processor Extended Status (FE) | 0 | 0 | FCB Processor Extended Status |

| 2 3 4 5 6 7 | Significance |
|---|---|
| (00) 0 0 0 0 0 0 | Idle state |
| (01) 0 0 0 0 0 1 | Adapter waiting to make channel request or continually servicing a hot file interrupt |
| (03) 0 0 0 0 1 1 | Waiting for Channel Grant |
| (04) 0 0 0 1 0 0 | Op decode state (interface hang condition). |
| (05) 0 0 0 1 0 1 | Waiting for acknowledge signal from Data Handler (cannot communicate between FA1 and FA2 cards). |
| (07) 0 0 0 1 1 1 | Waiting for proceed signal from Data Handler to enable next file operation. |
| (0F) 0 0 1 1 1 1 | Waiting for proceed signal from Data Handler (doing data transfer to/from storage). |
| (11) 0 1 0 0 0 1 | Incomplete End Op processing. Decoding 'end-op' has not presented adapter basic status (BS) but is presenting an interruption. If a seek or data transfer command in the FCB precedes 'end-op', cannot get 'end-op complete' until those commands complete. |
| (27) 1 0 0 1 1 1 | Incomplete PCI processing |
| (2C) 1 0 1 1 0 0 | Waiting for seek completion before processing Data Op. Will have a 'read' or 'write' in the next function request register. Must wait for 'seek complete' before any data transfer can be done. |

| | 2 | 3 | 4 | 5 | 6 | 7 | Significance |
|---|---|---|---|---|---|---|---|
| (37) | 1 | 1 | 0 | 1 | 1 | 1 | End op processing delayed by outstanding seek. There is no data transfer command in the FCB list. Need 'seek complete' before executing end-op. |
| (38) | 1 | 1 | 1 | 0 | 0 | 0 | Multisector transfer past sector 63. The number of sectors to transfer exceed the number of sectors remaining on the disk. |
| (39) | 1 | 1 | 1 | 0 | 0 | 1 | Data Handler error. The following conditions turn on this error: (1) data CRC, (2) ID error, (3) track does not compare, (4) something is wrong with the data the file presented to the data handler card (FA2 card). See data handler basic status and data handler extended status to determine the type of error. When this error occurs, the following is true: (1) seek was OK, (2) can transfer data, (3) alternate sector sets an FCB status of hex 39. |
| (3A) | 1 | 1 | 1 | 0 | 1 | 0 | File error (non data); not doing a data transfer. In conjunction with this error, file status bits 1, 2, 3, 4, or 7 is on. |
| (3B) | 1 | 1 | 1 | 0 | 1 | 1 | File error (data related); error during a read or write, not necessarily a data problem. |
| (3C) | 1 | 1 | 1 | 1 | 0 | 0 | Data flow parity error. There is a parity error in the tags between the FA1 and FA2 cards. This is a control parity error, not a data parity error. |
| (3D) | 1 | 1 | 1 | 1 | 0 | 1 | Control sample timeout. Sent 'control sample' to the file but did not get 'control sample' back within 1.8 $\mu$sec. |
| (3E) | 1 | 1 | 1 | 1 | 1 | 0 | CHIO equipment check (file adapter check). The adapter connected to the processor by means of CHIO and 'halt' became active. If data handler status bit 6 is off, the adapter is doing a control operation; if the bit is on, the adapter is doing an FCB operation. |
| (3F) | 1 | 1 | 1 | 1 | 1 | 1 | Control bus parity error. The adapter detected bad parity during a sense operation to the file. |

**Data Handler Basic Status (HS)**

| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Data Handler Basic Status (HS) | FCB Proc Error | DH Error | CRC Error | ID Error | Data Field Error | Sector Not Found | Equip Check / Halt | File Write Gate Error |

**Note:** *The status bits are set to a 1 when active.*

**Bit 0 — FCB Processor Error.** Indicates Data Handler received bad parity from FCB Processor.

**Bit 1 — Data Handler Error.** Indicates error was detected internal to data handler card (FA2 card).

**Bit 2 — CRC Error.** Indicates that CRC received from file does not compare to CRC generated. See bits 3 and 4 to determine the type of CRC error.

**Bit 3 — ID Error.** Indicates an ID error. This bit is set if the defective bit is on in the ID field on a read ID, read data, or write data command.

**Bit 4 — Data Field Error.** Indicates CRC error or write operation to a write protected field.

**Bit 5 — Sector Not Found.** Indicates that the sector cannot be found. Set if:

1. Sector search and two indexes are detected before the sector is found.
2. Not getting sector pulses (sector counter does not run).
3. Sync byte is not decoded in read ID (see if the NRZI line is pulsing).

**Bit 6 — Equip Check/Halt.** Indicates that equipment check occurred after the data channel grant. Data transfer is halted. This bit sets adapter basic status bits 1, 5, and 7.

**Bit 7 — File Write Gate Error.** Indicates a miscompare between write gate to file and write gate return from file (Data Unsafe condition). Set if:

1. File was told to write, but no write gate was returned.
2. File was not told to write, but a write gate was returned.

If NFR equals write, this indicates a good write gate error. If NFR equals read or write, this indicates a multisector data transfer is in process and the write gate return should be active.

**Adapter Basic Status (BS)**

| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Adapter Basic Status (BS) | PCI | Device Error | File Int Disab | Busy | Chan Req Frozen | Equip Check | Req Enab | Int |

**Note:** *The status bits are set to a 1 when active.*

**Bit 0 — Program Controlled Interrupt (PCI).** Indicates when the adapter decodes a PCI operation.

**Bit 1 — Device Error.** Indicates adapter has detected an error which was caused by the device. The 'file not ready' bit is set.

**Bit 2 — File Interrupt Disabled.** Set by program. Adapter ignores interrupts from file.

**Bit 3 — Busy.** Indicates that the adapter is processing FCBs.

**Bit 4 — Channel Request Frozen.** Set by program. Prevents adapter from requesting a new FCR operation. Allows the current data transfer to complete, then stops the adapter.

**Bit 5 — Equipment Check.** Indicates that this adapter has detected an error. The adapter is selected, but received halt tag on an internal check. This bit is also set by a parity error in the NFR. When this bit is on, 'file not ready' is set.

**Bit 6 — Requests Enabled.** Set by program. Enables adapter to make requests to the processor. If this bit is off, the adapter cannot perform CHIO operations.

**Bit 7 — Interrupt.** Set when adapter wants to interrupt processing. Occurs for normal reasons as well as error detection.

**Data Handler Extended Status (HE)**

| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Data Handler Extended Status (HE) | BFR A to File | File Speed Good | Wrt Prot 1 | Wrt Prot 0 | Sector Disp | Sector Reas-signed | Sector Defect | Alt Sector |

**Note:** *The status bits are set to a 1 when active.*

**Bit 0 — Buffer A to File.** Indicates buffer A connected to file. "0" indicates buffer B connected to file.

**Bit 1 — File Speed Good.** Indicates file speed tolerance is within 2-1/2% nominal. This bit is off if sector pulses are not detected every 600 ms.

**Note:** *Bits 2–7 are valid only for the last good ID read. If the read was not successful, these bits are left over from the previous ID read.*

**Bit 2 — Write Protect 1.** Indicates second half of sector is Write Protected.

**Bit 3 — Write Protect 0.** Indicates first half of sector is Write Protected.

**Bit 4 — Sector Displaced.** Indicates sector is displaced form normal position (pushed down).

**Bit 5 — Sector Reassigned.** Indicates sector is reassigned to an alternate sector.

**Bit 6 — Sector Defective.** Indicates a defective sector.

**Bit 7 — Alternate Sector.** Indicates that the sector is an alternate.

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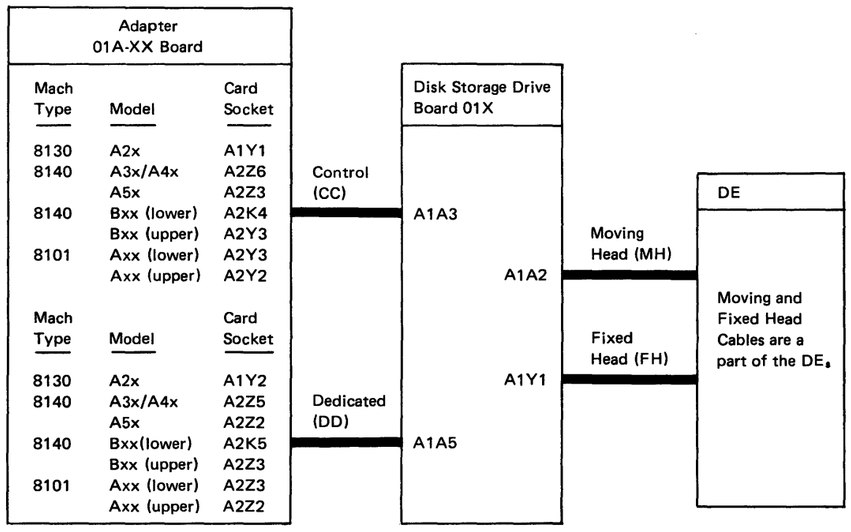
Use Figure FA240-1 to identify locations for sections FA241, FA242, and FA243.

| Mach Type | Model | Pseudo Card Locations | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Gate 01A | | | Disk Storage Gate 01C | | | | | | |
| | | SC | FA1 | FA2 | FA3 | FA4 | FA5 | FA6 | FA7 | FA8 | FA9 |
| 8130 | A2x | A2G2 | A1U2 | A1T2 | A1B2 | A1C2 | A1D2 | A1E2 | A1F2 | VCM | A1A4 |
| 8140 | A3x/A4x<br>A5x | A2D2<br>A2D2 | A2Q2<br>A2F2 | A2P2<br>A2E2 | A1B2<br>A1B2 | A1C2<br>A1C2 | A1D2<br>A1D2 | A1E2<br>A1E2 | A1F2<br>A1F2 | VCM<br>VCM | A1A4<br>A1A4 |
| 8140 | Bxx (lower)<br>Bx2 (upper) | A2A2<br>A2A2 | B2H2<br>B2F2 | B2J2<br>B2G2 | A1B2<br>A1B2 | A1C2<br>A1C2 | A1D2<br>A1D2 | A1E2<br>A1E2 | A1F2<br>A1F2 | VCM<br>VCM | A1A4<br>A1A4 |
| 8101 | Axx (lower)<br>Axx (upper) | A2A2<br>A2A2 | A2H2<br>A2E2 | A2J2<br>A2F2 | A1B2<br>A1B2 | A1C2<br>A1C2 | A1D2<br>A1D2 | A1E2<br>A1E2 | A1F2<br>A1F2 | VCM<br>VCM | A1A4<br>A1A4 |

**A. Pseudo Card Locations**




**B. Pseudo Cable Locations**

**Figure FA240-1. Pseudo Card and Cable Locations**

**Manual Intervention (MI) or Operator Messages**

| Msg No. | Message | Actions* |
|---|---|---|
| PA00 | Successful completion. | |
| PA80 | CHIO hang, attempted data transfer. | 1. Reseat or exchange FA1, FA2, SC, and TCC W and X.<br>2. Check continuity in nets:<br>FA1B08–SC D09<br>FA1G03–SC P02 |
| PA84 | CE cylinder degraded. | 1. Run Surface Status and Format utility (see CP653) on cylinder 359.<br>2. Rerun FA MAP.<br>3. If same failure occurs, reseat or exchange FA1, FA2.<br>**Note:** *If the problem still occurs, the CE cylinder has been degraded so that a Write Multisector (full track) operation can not be tested. All other diagnostic tests have completed successfully.* |
| PAF0 | Test in progress. | |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

*FA241 Common Test Error Messages and Actions*

| RREN | Failure Desription | Actions* |
|---|---|---|
| XX01 | System check | 1. Reseat or exchange FA1, FA2, SC, FA4, FA3.<br>2. Check wiring on TCCs W, X, Y, Z.<br>3. Check continuity in the nets:<br>• FA2B02–FA1S02<br>• FA2B09–FA1D09<br>• FA2B10–FA1B10<br>• FA2D02–FA1D02<br>• FA2D06–FA1D06<br>• FA2D07–FA1D07<br>• FA2D10–FA1D10<br>• FA2D11–FA1D11<br>• FA2D12–FA1D12<br>• FA2G09–SCG12<br>• FA2G12–FA1J05<br>• FA2S10–FA1D04–FA1G09–FA1J11<br>• FA1B02–FA1G05–FA1J13<br>• FA1G02–SCD07<br>• FA1J04–SCJ06<br>• FA1M08–SCG10<br>• FA1M10–SCP10<br>• FA1P02–SCG02<br>• FA1P10–SCM12<br>• FA1S04–SCB02<br>• FA1S05–SCG05<br>• FA1S07–SCD11<br>• FA1S08–SCM02<br>• FA1S10–SCB10<br>• FA1S12–SCP11<br>• FA1S13–SCG09<br>• FA1U02–SCD13 |
| XX01 (cont) | | 3. (cont)<br>• FA1U04–SCJ09<br>• FA1U05–SCG04<br>• FA1U07–SCP06<br>• FA1U10–SCJ07<br>• FA1U11–SCB08<br>• FA1U12–SCP13<br>• FA1U13–SCG08 |
| XX04 | Unexpected interrupt | 1. Reseat or exchange FA5, FA7, FA4. |
| XX07 | Initialize error. | 1. Reseat or exchange FA1, FA4, FA9, FA2, FA5, FA7.<br>2. Reseat or replace TCCs W, X.<br>3. Reset or replace cables (CC), (DD).<br>4. Check continuity in nets:<br>• TCC W24<br>• TCC X05<br>• TCC X24<br>• FA1G13–(CC)B04–FA4P07–FA9B04<br>• FA1B04–(CC)B12–FA9B12–FA4P09<br>• FA1B05–(DD)B04–FA4D06<br>• FA1G07–(CC)B05–FA4M08–FA9B05<br>• FA1G10–(CC)B03–FA4M07–FA9B03<br>• FA1G12–(CC)B02–FA4M09–FA9B02<br>• FA1J09–(CC)D05–FA9D05–FA4P02<br>• FA1M12–(DD)B03–FA4G09 |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| XX0A | Save ID error. | 1. Run Surface Status and Format Utility (CP653) on cylinder 359.<br>2. Rerun tests (even if utility failed). |
| XX0B | ID not stored. | 1. Run Surface Status and Format Utility (CP653) on cylinder 359.<br>2. Rerun tests (even if utility failed). |
| XX0C | Restore ID error. | 1. Run Surface Status and Format Utility (CP653) on cylinder 359.<br>2. Rerun tests (even if utility failed). |
| XX0F | Internal equipment check. | Reseat or exchange FA1, FA2. |
| XX66 | CE cylinder in degraded state | 1. Run Surface Status and Format Utility (CP653) on cylinder 359, all heads.<br>2. Suspect DE; request aid. |
| XX77 | Data handler basic status error. | 1. Reseat or exchange FA2, FA1.<br>2. Check continuity in TCC Y and Z. |
| XX99 | Adapter machine check. | 1. Reseat or exchange FA2, FA1.<br>2. Check continuity in nets:<br>• FA1B10–FA2B10<br>• FA1D02–FA2D02<br>• FA1D06–FA2D06<br>• FA1D07–FA2D07<br>• FA1D09–FA2B09<br>• FA1D10–FA2D10<br>• FA1D11–FA2D11<br>• FA1D12–FA2D12<br>• FA1S02–FA2B02 |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

*FA242 Adapter Test Messages, Error Numbers, and Actions*

| RREN | Failure Description | Actions* |
|---|---|---|
| 0110 | Residual count error. | Reseat or exchange FA1, FA2. |
| 0111 | FCB processor error. | Reseat or exchange FA1, FA2. |
| 0112 | Seek status error. | 1. Reseat or exchange FA1.<br>2. Check continuity in nets:<br>• TCC Y03<br>Wiring: See FA522 |
| 0113 | Burst reg error. | Restart or exchange FA1, FA2. |
| 0114 | First value reg error. | 1. Reseat or exchange FA1, FA4, (DD).<br>2. Check continuity in nets:<br>• FA1B05–(DD)B04–FA4D06 |
| 0115 | Next function request reg error. | Reseat or exchange FA1. |
| 0116 | Data CHCV error. | Reseat or exchange FA1, FA2. |
| 0117 | FCB CHCV error. | Reseat or exchange FA1, FA2. |
| 0118 | Seek reg error. | Reseat or exchange FA1, FA2. |
| 0210<br>0211 | Set basic status error. | Reseat or exchange FA1, FA2, FA4, FA5. |
| 0212<br>0213 | Reset basic status error. | Reseat or exchange FA1, FA2. |
| 0214 | Set basic status error. | Reseat or exchange FA1, FA2. |
| 0215 | Reset basic status error. | Reseat or exchange FA1, FA2. |
| 0310<br>0311 | Write NFR reg error. | Reseat or exchange FA1. |
| 0315 | Reset NFR reg error. | Reseat or exchange FA1. |
| 0410 | NFR reg error.<br>(write NFR reg) | Reseat or exchange FA1. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 0411 | Seek reg error.<br>(load NFR reg to seek reg) | Reseat or exchange FA1. |
| 0412 | NFR reg error.<br>(write NFR reg) | Reseat or exchange FA1. |
| 0413 | Seek reg error.<br>(load NFR reg to seek reg) | Reseat or exchange FA1. |
| 0414 | NFR reg error.<br>(write NFR reg) | Reseat or exchange FA1. |
| 0415 | NFR reg error.<br>(controller reset) | Reseat or exchange FA1. |
| 0416 | Seek reg error.<br>(load NFR reg to seek reg) | Reseat or exchange FA1. |
| 0418 | Seek reg error.<br>(controller reset) | Reseat or exchange FA1. |
| 0510 through 0517 | FCB CHCV error. | Reset or exchange FA1, FA2. |
| 0610 through 0618 | Data CHCV error. | Reseat or exchange FA1, FA2. |
| 0710 | Set first value. | Reseat or exchange FA1, FA2. |
| 0711 | Write first value. | Reseat or exchange FA1, FA2. |
| 0714 | Reset first value. | Reseat or exchange FA1, FA2. |
| 0810 | FCB CHCV error.<br>(using Initiate command) | Reseat or exchange FA1, FA2. |
| 0811 | Basic status error.<br>(after Initiate command) | 1. Reseat or exchange FA1, FA2.<br>2. Check continuity in TCCs W, X. |
| 0812 | Error in FCB channel pointer reg address.<br>(using Initiate command) | Reseat or exchange FA1. |
| 0813 | Basic status error.<br>(after Initiate command) | 1. Reseat or exchange FA1, FA2, SC.<br>2. Check continuity in TCCs W, X.<br>3. Check continuity in net:<br>• FA1J02–SCJ02<br>• FA2G09–SCG12 |
| 0814 | FCB CHCV error.<br>(using Initiate command) | Reseat or exchange FA1. |
| 0910 | Basic status error<br>(during Initiate Timeout) | Reseat or exchange FA1, FA2, FA4, FA5. |
| 0911 | Seek status error.<br>(during Initiate Timeout) | Reseat or exchange FA1, FA2, FA4, FA5, FA6. |
| 1010 | Basic status error.<br>(on set PCI) | 1. Reseat or exchange FA1, FA2.<br>2. Check continuity in TCC W05. |
| 1110 | Basic status error. (after store memory control) | 1. Reseat or exchange FA1, FA2.<br>2. Check continuity in TCCs W, X. |
| 1111 | Data CHCV error.<br>(after store memory control) | Reseat or exchange FA1, FA2. |
| 1112 | FCB CHCV error.<br>(after store memory control) | Reseat or exchange FA1, FA2. |
| 1113<br>1114 | Error in address remaining in FCB CHCV.<br>(after store memory control) | Reseat or exchange FA1, FA2. |
| 1210 | Basic status error after PCI. | Reseat or exchange FA1, FA2. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 1310 | Basic status error after Set Basic Status Under Mask command. | Reseat or exchange FA1, FA2. |
| 1410 | Invalid PIO command failed to set equipment check. | Reseat or exchange FA1, FA2. |
| 1519 | Basic status error after File Reset P10 command. | 1. Reseat or exchange FA4, FA2, (DD).<br>2. Check continuity in nets:<br>• FA2G13—(DD)D11—FA4G12 |
| 1610 | Basic status error during initialize function request. | Reseat or exchange FA2, FA1. |
| 1711 | Failure in program function request block (FRB). | Reseat or exchange FA1, FA2, FA3. |
| 1712 | Residual count error | Reseat or exchange FA1, FA2. |
| 1713 | Seek reg error | Reseat or exchange FA1, FA2. |
| 1714 | Burst reg error. | Reseat or exchange FA1, FA2. |
| 1715 | FRB complete with error. | Reseat or exchange FA1, FA2. |
| 1716 | Residual count error. | Reseat or exchange FA1, FA2. |
| 1717 | Seek reg error. | Reseat or exchange FA1, FA2. |
| 1718 | Burst reg error. | Reseat or exchange FA1, FA2. |
| 1811 | Write buffer error. | 1. Reseat or exchange FA1, FA2.<br>2. Check continuity in TCCs W, X. |
| 1812 | Read buffer error. | 1. Reseat or exchange FA1, FA2.<br>2. Check continuity in TCCs W, X, Y, Z. |
| 1813 | Data buffer error (0000) | 1. Reseat or exchange FA1, FA2, SC.<br>2. Check continuity in TCC X. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 1814 | Data buffer error (FFFF). | 1. Reseat or exchange FA1, FA2.<br>2. Check continuity in TCCs Y, Z. |
| 1815 | Write buffer error. | Reseat or exchange FA1, FA2. |
| 1816 | Read buffer error. | Reseat or exchange FA1, FA2. |
| 1817 | Data error (FFFF). | Reseat or exchange FA1, FA2. |
| 1818 | Data buffer error (0000). | Reseat or exchange FA1, FA2. |
| 1910 | Write buffer error. | Reseat or exchange FA1, FA2. |
| 1911 | Read buffer error. | Reseat or exchange FA1, FA2. |
| 1912 | Basic status error after read buffer. | Reseat or exchange FA1, FA2. |

*FA243 Disk Logic Test Messages, Error Numbers, and Possible Causes*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2010 | Control sample not received. | 1. Reseat or exchange FA1, FA4, FA9, (CC).<br>2. Check whether jumper at C-A1A5B12 to B13 is properly installed and has good continuity.<br>3. Check continuity in nets:<br>• FA1B04—(CC)B12—FA9B12—FA4P09<br>• FA1J06—FA2J12—(DD)B12—FA4B03<br>• FA7G10—(J1-2)<br>• FA5G11—(J5-1)<br>4. Check power interface lines (see PA452):<br>• — Power good<br>• + Brake applied |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2011 | Seek timeout error (spindle turning and appears to be running normally) | 1. Reseat or exchange FA5, FA4, FA7, FA3, FA8, FA2, FA1, (DD).<br>2. Check drive power.<br>3. Check that actuator lock is fully disengaged. (see FA590)<br>4. Check continuity in nets:<br>• FA4B06–FA5U10<br>• FA4D07–FA5S09<br>• FA4D11–FA5B03<br>• FA4D13–FA5U11<br>• FA4J07– FA5D06–FA7S13<br>• FA1B05–(DD)B04–FA4D06<br>• FA3M05–FA4D09–FA5J04<br>• FA3P05–FA4P10<br>• FA3P06–FA4G02<br>• FA3P10–FA4J06<br>• FA4B13–FA5S04<br>• FA4M12–FA5P09<br>• FA4P11–FA5J13–FA7S07<br>• FA4S05–FA5D07<br>• FA4S06–FA5D05<br>• FA4S07–FA5M12<br>• FA4S08–FA5M07<br>• FA4U06–FA5B05<br>• FA5G04–FA7D09<br>• FA4M13–FA5S07–FA7P11<br>• FA4U02–FA5U07–FA7M13<br>• FA4U10–FA5G07<br>• FA5G02–FA7B09<br>• FA5G03–FA7B08<br>• FA5J06–FA7B10 |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*



| RREN | Failure Description | Actions* |
|---|---|---|
| 2011 (cont) | | • FA5S13–(DD)D07–FA2B03<br>• FA6D10–FA7D10, J10, P10, U10 |
| | Seek timeout error (spindle stops turning after 20 second power on delay) | 1. Check that spindle lock is fully disengaged (see FA590).<br>2. Reseat or exchange FA5, FA7, FA6, FA3, FA4.<br>3. Check continuity in nets:<br>• FA3M10–FA6G12<br>• FA3U12–FA5J05<br>• FA4S03–FA5S08<br>• FA5B13–FA6G07<br>• FA5G05–FA7B04<br>• FA5J02–FA6J07<br>• FA7D05–(MH)D11<br>• FA7D06–(MH)D10<br>• FA7S04–(MH)B10, B12, D09, D13<br>4. Suspect DE; request aid. |
| | Seek timeout error (spindle never starts turning at all) | 1. Check that spindle lock is fully disengaged (see FA590).<br>2. Check belt, motor (see FA580, FA570)<br>3. Check ac to motor (see FA570)<br>4. Reseat or exchange FA4, FA5, FA7<br>5. Check continuity in nets:<br>• FA4S13–FA5U09–FA7P02<br>• FA5M09–FA7P09–B2A01 (J1-8) |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

**(FA242 Cont, FA243)**

| RREN | Failure Description | Actions* |
|---|---|---|
| 2012 | File sense not '82' after recal failure | 1. Reseat or exchange FA4, FA9, FA1, FA5, FA3, FA7, FA2, FA6, (CC), (DD).<br>2. Check continuity in nets:<br>• TCC-W22<br>• FA1B03–(CC)D06–FA9D06–FA4M03<br>• FA1G08–(CC)D09–FA9D09–FA4M05<br>• FA1G12–(CC)B02–FA9B02–FA4P07<br>• FA1J07–(CC)D07–FA9D07–FA4M02<br>• FA1J09–(CC)D05–FA9D05–FA4P02<br>• FA1J10–(CC)D04–FA9D04–FA4M04<br>• FA1J12–(CC)D13–FA9D13–FA4P04<br>• FA1M03–(CC)D11–FA9D11–FA4P05 |
| 2012 (cont) | | • FA1M04–(CC)D10–FA9D10–FA4P06<br>• FA1P04–(CC)D12–FA9D12–FA4M06<br>• FA2D04–(DD)B05–FA5S10<br>• FA3B12–(MH)D03–(FH)A13<br>• FA3G10–FA4M11<br>• FA3M02–FAS11<br>• FA3M05–FA4D09–FA5J04<br>• FA4B08–FA5P07–FA7M02<br>• FA4S07–FA5M12<br>• FA4U07–FA5P10<br>• FA5B09–FA7S10<br>• FA5G02–FA7B09<br>• FA5S12–FA7D13<br>• FA5U04–FA7P07<br>3. Suspect DE; request aid. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2013 | File sense not '82' after successful sense operation | 1. Reseat or exchange FA4, FA5, FA7<br>2. Check continuity in net:<br>• FA4B08–FA5P07–FA7M02 |
| 2014 | Control bus error | 1. Reseat or exchange FA7, FA6, FA1, FA9, FA3, FA4, FA5, FA2, (CC).<br>2. Check continuity in nets:<br>• FA1B03–(CC)D06–FA9D06–FA4M03<br>• FA1G07–(CC)B05–FA9B05–FA4M08<br>• FA1G10–(CC)B03–FA9B03–FA4M07<br>• FA1J07–(CC)D07–FA9D07–FA4M02<br>• FA1J09–(CC)D05–FA9D05–FA4P02<br>• FA1J10–(CC)D04–FA9D04–FA4M04<br>• FA4B08–FA5P07–FA7M02<br>• FA5B07–FA7D11<br>• FA6B13–FA7P06<br>• FA6D10–FA7D10–FA7J10–FA7P10–FA7U10<br>• FA6D13–FA7D02 |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2015 | Recalibrate failure | 1. Reseat or exchange FA5, FA4, FA7, FA3, FA6, FA2, FA1, (DD)<br>2. Check continuity in nets:<br>• FA5J06–FA7B10<br>• FA5U12–FA7M08 |
| 2016 | Speed OK bit failure | 1. Reseat or exchange FA2. |
| 2017 | Recal failure | 1. Reseat or exchange FA5, FA7.<br>2. Check continuity of net:<br>• FA5U12–FA7M08<br>• FA6D13–FA7D02 |
| 2018 | Control sample pulsing logic error | 1. Reseat or exchange FA1, FA4. |
| 2110 | Recal failure | 1. Reseat or exchange FA5, FA7, FA4, FA1.<br>2. Check continuity in net:<br>• FA5J06–FA7B10 |
| 2111 | Control bus failure | 1. Reseat or exchange FA4, FA9, FA1, (CC)<br>2. Check continuity of net:<br>• FA1B03–(CC)D06–FA9D06–FA4M03<br>• FA1G08–(CC)D09–FA9D09–FA4M05<br>• FA1J09–(CC)D05–FA9D05–FA4P02 |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2112 | Control bus parity error. | Reseat or exchange FA4. |
| 2113 | Control bus failure | 1. Reseat or exchange FA4, FA9, FA1, (CC). |
| 2114 | FRB complete with control bus parity error. | 1. Reseat or exchange FA4, FA1, FA9, (CC).<br>2. Check continuity in nets:<br>• FA4P04–(CC)D13–FA1J12–FA9D13 |
| 2115 | FRB complete with error and no file error. | 1. Reseat or exchange FA6, FA7.<br>2. Check wiring in net:<br>• FA6D10–FA7D10, J10, P10, U10 |
| 2116 | FRB complete with control bus parity error. | Reseat or exchange FA1, FA4, (CC). |
| 2117 | FRB complete with error and no file error. | Reseat or exchange FA1, FA2, FA4. |
| 2210 | Recal failure. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 2212 | FRB complete with error. | 1. Run Surface Status and Format Utility (CP653) on track 0, head 1, then rerun diagnostic tests.<br>2. Reseat or exchange FA3, FA2, FA4, FA5, FA1, FA7, FA6.<br>3. Reseat or replace cables (DD), (FH), (MH), TCCs W, X, Y.<br>4. Check continuity in nets:<br>• FA1P06–(DD)D04–FA4J13<br>• FA2B07–FA2B08<br>• FA2B12–FA2D13–FA2G02–FA2G03–FA2J02<br>• FA2G07–(DD)D10–FA3U07<br>• FA2G08–(DD)B08–FA3S07 |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2212 (cont) | | 4. (cont)<br>• FA2J06–(DD)D12–FA3U11<br>• FA2J07–(DD)D09–FA4J11<br>• FA2J09–(DD)D05–FA3S02<br>• FA3B04–FA4J02–FA5G09<br>• FA3B12–(MH)D03–(FH) A1A13<br>• FA3J12–FA4J12<br>• FA3M04–(MH)B03–(FH) A1E13<br>• FA3M05–FA4D09–FA5J04<br>• FA3M07–(FH) A1E11<br>• FA3M09–(MH)B02<br>• FA3P05–FA4P10<br>• FA3P09–(MH)B06<br>• FA3P10–FA4J06<br>• FA3U06–FA6G03<br>• FA4J07–FA5D06–FA7S13<br>5. See net in FA521.<br>6. Suspect DE; request aid. |
| 2213 | FRB complete without error after error test. | 1. Run Surface Status and Format Utility (CP653) on track 0, head 1, then rerun diagnostic tests.<br>2. Reseat or exchange FA4, FA3, FA2, FA1, FA5<br>3. Check continuity in nets:<br>• FA1P06–(DD)D04–FA4J13<br>• FA2G08–(DD)B08–FA3S07<br>• FA2J07–(DD)D09–FA4J11<br>• FA3B04–FA4J02–FA5G09<br>• FA3J12–FA4J12<br>4. Suspect DE; request aid. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2214 | Basic status not correct after error test. | Reseat or exchange FA1, FA2. |
| 2310 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 2311 | Seek to track 1 error. | 1. Reseat or exchange FA4, FA5, FA7, FA6, FA1, FA9, (CC).<br>2. Check continuity in nets:<br>• FA1J10–(CC)D04–FA9D04–FA4M04<br>• FAJ05–FA5U02<br>• FA4M06–(CC)D12–FA1P04–FA9D12<br>• FA4S07–FA5M12<br>• FA4S09–FA6J06–FA7B03<br>• FA4U06–FA5B05<br>• FA5G03–FA7B08<br>• FA7S02–FA5J07<br>• FA1G13–(CC)B04–FA9B04–FA4M09<br>• FA4B08–FA5P07–FA7M02 |
| 2312 | File status error. | 1. Reseat or exchange FA4, FA9, FA1, FA6, FA7, (CC).<br>2. Check continuity in nets:<br>• FA1B03–(CC)D06–FA9D06–FA4M03<br>• FA1G08–(CC)D09–FA9D09–FA4M05<br>• FA4S09–FA6J06–FA7B03 |
| 2313 | File status not = 80. | 1. Reseat or exchange FA4, FA5.<br>2. Check continuity in nets:<br>• FA4G04–FA5P12 |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2314 | Read ID error. | 1. Run Surface Status and Format Utility (CP653) on track 1, head 1, then rerun diagnostic tests.<br>2. Reseat or exchange FA5, FA4, FA7.<br>3. Reseat or replace cable (DD).<br>4. Check continuity in nets:<br>• FA4G05–FA5M08<br>• FA5B09–FA7S10<br>5. See net in FA521<br>6. Suspect DE; request aid. |
| 2315 | Seek to track 0 error. | 1. Reseat or exchange FA5, FA4, FA7.<br>2. Check continuity in nets:<br>• FA4J05–FA5U02<br>• FA5S12–FA7D13 |
| 2316 | File status error. | Reseat or exchange FA4, FA1, (CC). |
| 2317 | File status not = 80. | Reseat or exchange FA4, FA6, FA7, FA1. |
| 2318 | Read ID error. | Reseat or exchange FA5, FA7. |
| 2410 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 2411 | Seek to track 128 error. | 1. Reseat or exchange FA7, FA5, FA4.<br>2. Check continuity in nets:<br>• FA4S06–FA5D05<br>• FA5D04–B1E4A14–(J9-3)<br>• FA4S05–FA5D07<br>• FA5B07–FA7D11<br>• FA5J07–FA7S02<br>• FA5S12–FA7D13 |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2412 | Recalibrate error after 128. | Reseat or exchange FA4, FA6, FA7, FA1. |
| 2510 | Recalibrate error. | Reseat or exchange FA4, FA6, FA7, FA1. |
| 2511 | Seek to track 359 error. (CE track) | 1. Run Surface Status and Format Utility (CP653) on cylinder 359, then rerun diagnostic tests. (even if utility fails)<br>2. Reseat or exchange FA5, FA7.<br>3. Check continuity in net:<br>• FA4S05–FA5D07<br>4. Check that actuator lock is fully disengaged. (See FA590.)<br>5. Suspect DE; request aid. |
| 2512 | Read ID error. | 1. Run Surface Status and Format Utility (CP653) on cylinder 359, then rerun diagnostic tests. (even if utility fails)<br>2. Reseat or exchange FA4, FA7, FA5.<br>3. Check continuity in net:<br>• FA5B09–FA7S10<br>4. Suspect DE; request aid. |
| 2513 | Write data error. | 1. Run Surface Status and Format Utility (CP653) on cylinder 359, then rerun diagnostic tests. (even if utility fails)<br>2. Reseat or exchange FA6, FA3, FA5, FA2, FA1, FA4, FA7, FA8, (DD).<br>3. Check continuity in nets:<br>• FA1M13–(DD)D06–FA4S10–FA5P13<br>• FA2B03–(DD)D07–FA5S13<br>• FA2D09–(DD)B09–FA5G08<br>• FA2G13–(DD)D11–FA4G12<br>• FA2M04–(DD)D03–FA3J07<br>• FA3D05–(MH)D05 |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2513 (cont) | | 3. (cont)<br>• FA3D06–(MH)D04<br>• FA3D07–(MH)D07–(FH)A1D11<br>• FA3D12–(J1-3)<br>• FA3G03–(MH)B08–(FH)A1C13<br>• FA3G13–FA4U12<br>• FA3J06–FA4G11<br>• FA3P11–FA6G08<br>• FA3S02–(DD)D05–FA2J09<br>• FA3U06–FA6G03<br>• FA4B12–FA6G13–FA7G12<br>• FA4G10–FA5U06<br>• FA4G13–FA6J13<br>• FA4J11–(DD)D09–FA2J07<br>• FA5G08–(DD)B09–FA2D09<br>• FA5J09–FA6G10<br>• FA5J10–FA6J04<br>• FA5U13–FA6G04<br>• FA6B12–FA6G05<br>4. Suspect DE, request aid. |
| 2514 | File status error. | Reseat or exchange FA4, FA6, FA7,FA1. |
| 2515 | Read sector error. | 1. Reseat or exchange FA3, FA2, (DD).<br>2. Check continuity in nets:<br>• FA2J11–(DD)B10–FA3U02 |
| 2516 | File status error. | Reseat or exchange FA4, FA6, FA7, FA1. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2517 | Readback check error. | Reseat or exchange FA4, FA3, FA5, FA1, FA2. |
| 2518 | Seek, write, read back, check error. | 1. Reseat or exchange FA7, FA8, FA2.<br>2. Suspect DE, request aid. |
| 2519 | Seek to track 0 error. | 1. Reseat or exchange FA5, FA4, FA7.<br>2. Check continuity in net:<br>• FA4S05–FA5D07 |
| 2520 | Sector ID error. | Reseat or exchange FA1, SC, FA2. |
| 2610 | Recalibrate, seek (128), recalibrate. | 1. Run Surface Status and Format Utility (CP653) on track 128, head 1. Then rerun diagnostic tests.<br>2. Reseat or exchange FA4, FA5, FA7, FA1. |
| 2611 | Model invalid. | See FA113; model and/or configuration are not valid. |
| 2613<br>2614<br>2615<br>2616 | Seek moving heads 1–4 (model 30).<br>Seek moving heads 0–4 (model 10).<br>Seek moving heads 1–A (model 40).<br>Seek moving heads 0–A (model 20). | 1. Run Surface Status and Format Utility (CP653) on cylinder 359, all heads. Then rerun diagnostic tests.<br>2. Reseat or exchange FA3, FA4, FA1, FA2.<br>3. Reseat cable (MH), TCC X.<br>4. Check continuity in nets:<br>• FA3M04–(MH)B03–(FH)A1E13<br>• FA3M09–(MH)B02<br>• FA3M11–(MH)B05<br>• FA3P09–(MH)B06<br>• FA3P07–FA4P12<br>• FA3P04–(MH)B04–(FH)A1C11<br>5. Possible defective head. Replace DE. Request aid. |
| 2617<br>2618 | Seek moving head 0 (model 30).<br>Seek moving head 0 (model 40). | See FA113; model and/or configuration do not agree. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*



| RREN | Failure Description | Actions* |
|---|---|---|
| 2619<br>261A<br>261B<br>261C<br>261D<br>261E | Seek moving heads 5 (model 10/30).<br>Seek moving heads 6 (model 10/30).<br>Seek moving heads 7 (model 10/30).<br>Seek moving heads 8 (model 10/30).<br>Seek moving heads 9 (model 10/30).<br>Seek moving heads A (model 10/30). | See FA113; model and/or configuration do not agree. |
| 2620<br>2621<br>2622<br>2623<br>2624<br>2625<br>2626<br>2627<br>2628<br>2629<br>262A | RD/WRT moving head 0.<br>RD/WRT moving head 1.<br>RD/WRT moving head 2.<br>RD/WRT moving head 3.<br>RD/WRT moving head 4.<br>RD/WRT moving head 5.<br>RD/WRT moving head 6.<br>RD/WRT moving head 7.<br>RD/WRT moving head 8.<br>RD/WRT moving head 9.<br>RD/WRT moving head A. | 1. Run Surface Status and Format Utility (CP653) on cylinder 359, all heads. Then rerun diagnostic tests.<br>2. Reseat or exchange FA1, FA2.<br>3. Check +24V ripple.<br>4. Suspect DE; request aid. |
| 2630<br>2631<br>2632<br>2633<br>2634<br>2635<br>2636<br>2637 | RD failure fixed head 0.<br>RD failure fixed head 1.<br>RD failure fixed head 2.<br>RD failure fixed head 3.<br>RD failure fixed head 4.<br>RD failure fixed head 5.<br>RD failure fixed head 6.<br>RD failure fixed head 7. | 1. Run Surface Status and Format Utility (CP653) on all fixed heads.<br>2. Reseat or exchange FA3, FA5, FA6.<br>3. Rerun tests.<br>4. If failure persists, suspect DE; request aid. |
| 2710 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 2711 | Seek to CE track error. | Reseat or exchange FA5, FA7. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

**(FA243 Cont)**

| RREN | Failure Description | Actions* |
|---|---|---|
| 2712 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 2713 | Write ID error. | Reseat or exchange FA5,FA7. |
| 2714 | File status error. | Reseat or exchange FA4, FA6, FA7, FA1, FA2. |
| 2715 | Sector flag error. | 1. Reseat or exchange FA4, FA3, FA5, FA1, FA2, (DD).<br>2. Check continuity in nets:<br>• TCC X32<br>• FA2G13–(DD)D11–FA4G12<br>• FA1M13–(DD)D06–FA4S10–FA5P13<br>• FA3G13–FA4U12 |
| 2810 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 2811 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 2812 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 2813 | Write data error. | Reseat or exchange FA6, FA3, FA4, FA5, FA2, FA7, FA1. |
| 2814 | Read data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 2815 | Read data error. | Reseat or exchange FA1, FA3, FA2. |
| 2816 | Multisector error. | Reseat or exchange FA3, FA2, FA1. |
| 2817 | Data overrun. | Reseat or exchange FA2. |
| 2910 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 2911 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 2912 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 2913 | Write data error. | Reseat or exchange FA6, FA3, FA4, FA5, FA2, FA7, FA1. |
| 2914 | Read data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 2915 | Retrieve error. | Reseat or exchange FA2, FA1. |
| 2916 | Format error. | Reseat or exchange FA2, FA1. |
| 2917 | Read data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 2918 | Data does not compare. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 2919 | Format error. | Reseat or exchange FA2, FA1. |
| 291A<br>291B | Read data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3010 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3011 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3012 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 3013 | WRT ID displaced error. | Reseat or exchange FA5, FA7, FA1. |
| 3014 | RD ID displaced error. | Reseat or exchange FA3, FA6, FA2, FA7, FA1. |
| 3015 | Displaced ID error. | Reseat or exchange FA3, FA6, FA2, FA7, FA1. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 3016 | RD ID error. | Reseat or exchange FA3, FA6, FA2, FA7, FA1. |
| 3017 | Restore ID error. | Reseat or exchange FA3, FA6, FA2, FA7, FA1. |
| 3018 | Format error. | Reseat or exchange FA1, FA2. |
| 3110 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3111 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3112 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 3210 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3211 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3212 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 3213 | Write ID error. | Reseat or exchange FA5, FA7. |
| 3214 | Data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3215 | Write data error. | Reseat or exchange FA6, FA3, FA4, FA5, FA2, FA7, FA1. |
| 3216 | Basic status error. | Reseat or exchange FA1, FA2, FA4, FA9. |
| 3217 | Residual count error. | Reseat or exchange FA2, FA1. |
| 3310 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3311 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3312 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 3313 | Write ID error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3314 | Read ID normal error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3315 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 3316 | Read data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3317 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 3410 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3411 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3412 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 3413 | Write data error. | Reseat or exchange FA6, FA3, FA4, FA5, FA2, FA7, FA1. |
| 3414 | Write ID error. | Reseat or exchange FA5, FA7. |
| 3415 | Protect bit error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3416 | Write data error. | Reseat or exchange FA6, FA3, FA4, FA5, FA2, FA7, FA1. |
| 3417 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 3418 | Read data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3419 | Protect data error. | Reseat or exchange FA3, FA6, FA2, FA7. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 3510 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3511 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3512 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 3513 | Format error. | Reseat or exchange FA2, FA1. |
| 3514 | Read data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3515 | Basic status error. | Reseat or exchange FA1, FA4 FA5, FA2, FA9. |
| 3610 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3611 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3612 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 3613 | Format error. | Reseat or exchange FA2, FA1. |
| 3614 | Read data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3615 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 3616<br>3617 | Write data error. | Reseat or exchange FA6, FA3, FA4, FA5, FA2, FA7, FA1. |
| 3710 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3711 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3712 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 3713 | Readback check error. | Reseat or exchange FA3, FA6, FA2, FA7, FA1. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 3714 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 3810 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3811 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3812 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 3813 | Write data error. | Reseat or exchange FA6, FA3, FA4, FA5, FA2, FA7, FA1. |
| 3814 | Read data error. | Reseat or exchange FA3, FA6, FA2, FA7. |
| 3815 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 3816 | Extended status error. | Reseat or exchange FA2, FA4, FA5, FA1, FA9. |
| 3910 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 3911 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 3912 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 3913 | Control bus error. | Reseat or exchange FA3, FA1. |
| 3914 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 3915 | Extended status error. | Reseat or exchange FA2, FA4, FA5, FA1, FA9. |
| 4010 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 4011 | Seek to CE track error. | Reseat or exchange FA4, FA5. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

| RREN | Failure Description | Actions* |
|---|---|---|
| 4012 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 4013 | Invalid seek address. | Reseat or exchange FA3, FA1. |
| 4014 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 4015 | Extended status error. | Reseat or exchange FA2, FA4, FA5, FA1, FA9. |
| 4113 | Control bus error. | Reseat or exchange FA4, FA1. |
| 4114 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 4115 | Extended status error. | Reseat or exchange FA2, FA4, FA5, FA1, FA9. |
| 4210 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 4211 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 4212 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 4213<br>4214 | PCI error. | Reseat or exchange FA1, FA2. |
| 4215 | Basic status error. | Reseat or exchange FA1, FA4, FA5, FA2, FA9. |
| 4216 | Extended status error. | Reseat or exchange FA2, FA4, FA5, FA1, FA9. |
| 4310<br>4311 | Seek error. | 1. Reseat or exchange FA4, FA5, FA7.<br>2. Suspect DE; request aid. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*



| RREN | Failure Description | Actions* |
|---|---|---|
| 4411 | Seek speed error. | 1. Reseat or exchange FA4, FA5.<br>2. Check continuity in nets:<br>• FA4D02–FA5B02<br>• FA4B02–FA5B08<br>3. Suspect DE; request aid. |
| 4412 | Seek timeout | 1. Reseat or exchange FA4, FA5.<br>2. Check continuity in nets:<br>• FA4D02–FA5B02<br>• FA4B02–FA5B08<br>3. Suspect DE; request aid. |
| 4413 | Controller error. | Reseat or exchange FA1, FA2. |
| 4510 | Seek speed bit error. | Reseat or exchange FA2. |
| 4511 | Speed out of tolerance. | Reseat or exchange FA5, FA7, FA4, FA6. |
| 4512 | Timeout. | Reseat or exchange FA1, FA2. FA2, FA4. |
| 4513 | Error during FCB processing. | Reseat or exchange FA1, FA2. |
| 4610 | Multisector write ID operational error. | Reseat or exchange FA6, FA3, FA4, FA5, FA2, FA7, FA1. |
| 4611 | Write IDs not requested. | Reseat or exchange FA1, FA2. |
| 4612 | Timeout occurred waiting for processing. | Reseat or exchange FA1. |
| 4613 | Error during FCB processing. | Reseat or exchange FA1, FA2. |
| 4711 | Multisector read too slow. | 1. Reseat or exchange FA1.<br>2. Run diagnostics on other adapters and/or disconnect other adapters located on the same board as the disk in question; repair failing adapter.<br>**Note:** *A channel grant problem in another adapter may be affecting the disk operation.* |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

**(FA243 Cont)**

| RREN | Failure Description | Actions* |
|---|---|---|
| 4713 | Error during FCB processing. | Reseat or exchange FA1, FA2. |
| 4810 | Recalibrate error. | Reseat or exchange FA4, FA5, FA7, FA1. |
| 4811 | Seek to CE track error. | Reseat or exchange FA4, FA5. |
| 4812 | Read ID error. | Reseat or exchange FA4, FA6, FA7. |
| 4813 | Write multisector error (2 sectors). | Reseat or exchange FA1, FA2. |
| 4814 | Write multisector error (full track). | Reseat or exchange FA1, FA2. |
| 5010 | Invalid model. | Correct configuration table to agree with DSD model.<br>**Note:** *After a configuration correction, the processor must be re-IPLed.* |
| 5011 | Fixed head write error. | Suspect DE; request aid. |
| 5012 | Fixed head read error. | 1. Run Surface Status and Format Utility (CP653) on all fixed heads.<br>2. Reseat or exchange FA3, FA5, FA6, (FH).<br>3. Rerun tests.<br>4. If failure persists, suspect DE; request aid. |

**Notes:**

1. **Use Figure FA240-1 to identify card and cable locations.*
2. *Unplug associated cards when checking continuity.*
3. *TCC W, X, Y, and Z are interchangeable with each other. However, they may be different than those used on other adapters. See Chapter 3, Figures LT140-1 through LT140-3, LT240-1 through LT240-8, LT340-1 and LT340-2 for TCC locations and part numbers.*

## FA250 Action Plan

1. If the unit is available, and the offline tests have not been run, do a power-on reset and run the tests.
2. Record the error message (RREN) for future reference. If there is no failure, go to step 8.
3. The unit must be released by the customer before replacing the FRU(s) indicated on the MD. Always power the unit down when instructed to reseat or replace a FRU, or check nets for continuity or shorts.
4. For multiple FRU callouts, replace them in the order shown on the MD display because they are listed in the order of failure probability. After replacing each FRU, key 'FWD' and the verification tests are automatically performed.
5. Check FA240 for the error number to be sure that all of the possible FRUs have been replaced. Only the most likely FRUs are listed on the MD display.
6. If replacing the FRUs does not correct the problem, check the continuity of the nets listed for the error number in FA240. Also check each net to ground, there should be no shorts.
   a. Open nets are field repairable by installing a BLU/WHT wire to complete the path. First use a test jumper to verify the fix.
   b. For a grounded net, check for foreign matter on the board in the area of the net pins. (For example, pieces of wire, nuts, screws, tight wire.)
7. If the failure still occurs, try this action plan one more time starting at step 1 before requesting assistance.
8. If the tests run without a failure, loop the tests for five passes (see FA311) or until there is a failure.
   - If a failure occurs, go to step 3.
   - If no failure occurs, terminate the test by entering an 'F' on the MD and then 'ENT'.
9. If the tests do not fail after five passes, go to FA350.

## FA300 Intermittent Failure Repair Strategy

### FA310 Adapter-Unique Intermittent Repair Strategy

Intermittent failures may be detected by looping the FA offline tests, or by examining the error log.

#### *FA311 Looping with MAP Interaction to Determine Failures*

To loop the disk storage tests, answer "YES" to the question: "Do you want to check for intermittent failure by looping FA test?" The test loops continuously until an error is detected or the test is terminated by entering an F on the MD keypad. While the test is looping, PAF0 is displayed on the MD.

If an error is detected while looping, the MAP analyzes and directs repairs of the failure in the same manner as a solid failure. Once a repair action has been performed, the MAP loops the tests to verify the repair.

**Note:** *If an error is not detected after five passes while looping the tests, or if the error detected occurs randomly (test error messages vary), the MAP operation is ineffective and more information is required. Go to FA350.*

*Another option is the free-lance looping operation (see FA313).*

#### *FA312 Using the System Error Log to Determine Failures*

DPPX and DPCX record in their error logs any DSD failure that occurs during system operation. The error log can be used to select specific failure types or all failures. Obtain all error log records associated with the DSD. Refer to Chapter 2 (CP700 for DPPX; CP800 for DPCX) for information on how to obtain the error log and to FA340 "How to Use the Error Log". Examine the log to determine the type of failure and go to FA350 to correct the failure.

#### *FA313 Using the Free-Lance Utility to Determine Failures*

The disk storage tests can be looped using the free-lance operation provided by the maintenance device (MD). The test invocation message is PAPN B – 11B (see FA210). The test loops continuously until an error is detected or the test is terminated by entering an F on the MD keyboard.

If an error is detected while looping, the MD displays the test message error number. Record the number and go to FA240 to identify and repair the failure. Once a repair action has been taken, loop the disk storage tests for at least five passes to verify the repair.

## FA320 Not Used



## FA330 Error Log Formats and Meanings Used for the FA MAP

The format of the error log depends upon whether the customer is using DPPX or DPCX. For DPPX formats, see FA331; for DPCX, see FA332.

### *FA331 DPPX Error Log Formats and Meanings*

Disk storage failures are stored in the DPPX error log in the Type 5 record format. Only those fields necessary for the FA MAPs are identified. See Chapter 2 (CP700) for complete error log details.

The error log for Class 05, Subclass 01, consists of either Header I or II plus the main body of the Record.

If bit 0 of the Option Mask (Option) = 1, then Header I is supplied with a time stamp. If bit 0 of the Option Mask = 0, then Header II is supplied with a sequence number.

The BCLE is part of the record of bit 1 if the option Mask = 1.

The D fields are variable by adapter type.

**DPPX Error Log Format**

**Header I**

CLASS 05 SUBCLASS 01 OPTION (5)
DATE YY.DDD TIME HH/MM/SS

**Header II**

CLASS 05 SUBCLASS 01 OPTION (5)
DATE YY.DDD SEQ NO. (1)

**Record**

PA (2) SCA (3) DT (4)
CRC (7) COMPSTAT (8) ARC (9)
DATA (11) RES (12) CNT (13)
IOEP (14) ADWA (15)
CA (16) CPR (17) FRWA (18)
RES (19)

**Extended Data**

| | | | |
|---|---|---|---|
| D01 (24) (25) | D02 (26) (27) | D03 (28) (29) | D04 (30) (31) |
| D05 (32) (33) | D06 (34) (35) | D07 (36) (37) | D08 (38) (39) |
| D09 (40) (41) | D10 (42) (43) | D11 (44) (45) | D12 (46) (47) |
| D13 (48) (49) | | | |

**Content Meaning**

The following listing describes the error log records used for the FA MAPs:

( 1) SEQ NO. Sequence Number of the error log record. This part of the Header II format is provided through DISPLAY.ERRLOG if bit 0 of the Option Mask (field 5) = 0. If bit 0 = 1, then Header I is provided with a time stamp. The format of the time stamp is hour/minute/second.

With either header, a data field is provided consisting of the year and Julian date.

Date is only valid when the customer sets it after every IPL using the SET.DATE command. Time is only valid when the customer runs DPPX with Timer Management and sets the time after every IPL using the SET.TOD command.

( 2) PA Physical Adapter Address – Byte 0 of the FRB byte.

( 3) SCA Secondary Component Address – Bytes 26, 27 of the FRB – N/A

( 4) DT Device Type – 40D7

( 5) OPTION Option Mask – Byte 4 of DPPX Header:

Bit 0 – 1 time stamp (Header I)
– 0 sequence number (Header II)
Bit 1 – 1 BCLE present
Bit 2 – 1 Extended data present
Bit 3–7 – Specifies format for extended data

( 7) CRC FDM Request Code (in hex) – Byte 1 of the FRB:

00 = Initialize
0B = Close
69 = Diagnose
6A = Low priority start
6C = Restart
6E = Hold
7A = High priority start

( 8) COMPSTAT Completion Status – Byte 2 of the FRB.
Byte 2 has the following meaning:

Bit 0 – Error Record Indicator
Bit 1 – Reenter
Bit 2 – Reenter FRB Indicator
Bit 3 – Reserved
Bit 4 – Complete
Bit 5 – Error
Bit 6 – Exception
Bit 7 – Attention

( 9) ARC Adapter Return Code (in hex) – Byte 3 of the FRB.
Valid entries are:

00 – Normal Completion
01 – Program Controlled Interrupt
02 – FRB Busy
04 – Equipment Check
06 – ECC Successful
10 – Program Check
11 – FRB Program Check
19 – Record Not Found
1A – Multisector Count Error
1B – Write Protect Error
20 – Unexpected Interrupt
21 – Adapter Parity Error
2A – Adapter Timeout
2B – Seek Check
33 – Data CRC Error – Primary
39 – Data CRC Error – Alternate
3A – ID CRC Error – Primary
3B – ID CRC Error – Alternate
62 – File Not Ready
63 – Data Unsafe
68 – File Speed Not OK

**Note:** *The values in fields 8 and 9 represent the status of the adapter when it terminated its activity (either successfully or with an error) and returned control to DPPX.*

(11) DATA Bytes 4–7 of the FRB.

(12) RES Reserved – Bytes 8, 9 of the FRB – N/A.

(13) CNT Count – Bytes 10, 11 of the FRB.

(14) IOEP I/O Interrupt Entry Point – Bytes 12–15 of the FRB.

(15) ADWA Adapter Work Area Address – Bytes 16–19 of the FRB.

(16) CA Channel Address – Byte 24 of the FRB – N/A.

(17) CPR Channel Pointer Register – Byte 25 of the FRB – N/A.

(18) FRWA Function Request Work Area Address – Bytes 20–23 of the FRB. Contains address of FDM error log.

(19) RES Reserved – Bytes 28–31 of the FRB – N/A.

D01 (24) Error Record Flags – Byte 0 of the FRWA. Defined as:

Bits 0–1 – Reserved
Bit 2 – Partial Log Indicator
Bits 3–7 – Reserved

**Note:** *If bit 2 is set, then the information in fields D01 through D13 are not complete and not correct.*

(25) FRB Byte 1 (Retry Count) – The number of retries attempted on the following operation before successful recovery or termination with error.

D02 (26) FRB Byte 2 (completion status) as logged on the initial detection of an error.

(27) FRB Byte 3 (ARC) as logged on the initial detection of an error.

D03 (28) Data handler extended status (see FA233):

Bit 0 – Buffer A to File
Bit 1 – File Speed Good
Bit 2 – Write Protect 1
Bit 3 – Write Protect 0
Bit 4 – Sector Displaced
Bit 5 – Sector Reassigned
Bit 6 – Sector Defective
Bit 7 – Alternate Sector

(29) Residual Sector Count — Residual count of the number of sectors remaining for a multisector operation that has been terminated with an error (Bits 10—15).

D04 (30) Data handler basic status (see FA233):

Bit 0 — FCB Processor Error
Bit 1 — Data Handler Error
Bit 2 — CRC Error
Bit 3 — ID Error
Bit 4 — Data Field Error
Bit 5 — Sector Not Found
Bit 6 — Equip Check/Halt
Bit 7 — File Write Gate Error

(31) Seek status (see FA233):

Bit 0 — Tag Sequence Error
Bit 1 — Command Error
Bit 2 — FCB Processor Error
Bit 3 — FCB Timeout Error
Bit 4 — Cable Continuity OK
Bits 5—7 — Seek Status:

000 — No MHS, FHS, RECAL in progress
001 — RECAL begun
010 — FHS begun
100 — MHS begun
101 — MHS begun, FHS done
110 — MHS begun, FHS begun
111 — MHS done, FHS begun

MHS = Moving Head Seek
FHS = Fixed Head Seek
RECAL = Recalibrate

D05 (32) Data handler basic status
See D04 (30) above.

(33) Basic status (see FA233):

Bit 0 — Program Controlled Interrupt
Bit 1 — Device Error
Bit 2 — File Interrupt Disabled
Bit 3 — Busy
Bit 4 — Channel Request Frozen
Bit 5 — Equipment Check
Bit 6 — Requests Enabled
Bit 7 — Interrupt

D06 (34) Data handler basic status
See D04 (30) above.

(35) FCB Processor status (see FA233):
Bit 0 — 0
Bit 1 — 0
Bits 2—7 (in hex):

| | |
|---|---|
| 00 | Idle state. |
| 01 | Adapter waiting to make channel request, or continually servicing a hot file interrupt. |
| 03 | Waiting for Channel Grant. |
| 04 | OP decode state. |
| 05 | Waiting for acknowledge signal from Data Handler. |
| 07, 0F | Waiting for proceed signal from Data Handler. |
| 11 | Incomplete End-Op processing. |
| 27 | Incomplete PCI processing. |
| 2C | Waiting for seek completion before processing Data Op. |
| 37 | End-Op processing delayed by outstanding seek. |
| 38 | Multisector error |
| 39 | Data Handler error |
| 3A | File error (non-data) |
| 3B | File error (data related) |
| 3C | Data flow parity error |
| 3D | Control sample timeout |
| 3E | CHIO equipment check |
| 3F | Control bus parity error |

D07 (36,37) Next Function Request (in hex) — FCB operation being executed.

| Code | Command |
|---|---|
| 0000 | End-Op |
| 0800 | No-Op |
| 0900 | PCI (Program-Controlled Interrupt) |
| 0A0X | Load Burst Register |
| 1000 | TIC End-Op |
| 18XX | Load Sector Count |
| 20XX | Read ID Normal |
| 21XX | Read ID Displaced |
| 23XX | Read ID PSC — Normal |
| 24XX | Read ID Compare |
| 26XX | Read ID Immediate |
| 28XX | Write ID |
| 29XX | Write ID Displaced |
| 30XX | Read Sector Normal |
| 34XX | Read Sector Compare |
| 38XX | Write Sector Normal |
| 3CXX | Write Sector Compare |
| 4200 | Recalibrate |
| 4XX0 | Control Bus — Bit 4 of byte 1 set |
| 5X00 | Store Memory Control |
| 60XX | Read Back Check Normal |

| | |
|---|---|
| 64XX | Read Back Check Compare |
| 6X00 | Buffer Diagnostic – Bit 4 of byte 1 set |
| 70XX | Read CRC |
| 71XX | Retrieve |
| 78XX | Format |
| 8YYY | Seek (Moving Heads) |
| 9YYY | Seek (Moving Heads) |
| AYYY | Seek (Fixed Heads) |
| CYYY | Store New Track (Moving Heads) |
| DYYY | Store New Track (Moving Heads) |
| EYYY | Store New Track (Fixed Heads) |

YYY bit layout = BBFHHHHC CCCCCCCC

where: BB = 10 = seek
11 = store new track

F = 1 = fixed head select
0 = moving head select

HHHH = head address

CCCCCCCCC = cylinder address

Examples (in hex):

| | | | | | |
|---|---|---|---|---|---|
| 1. Seek to moving head 5, cylinder 128 | 10 | 0 | 0101 | 1 | 00101000 |
| 2. Seek to fixed head 3 (cylinder address not applicable) | 10 | 1 | 0011 | C | CCCCCCCC |
| 3. Store new track moving head 2, cylinder 167 | 11 | 0 | 0010 | 1 | 01100111 |
| 4. Store new track fixed head 7 (cylinder address not applicable) | 11 | 1 | 0111 | C | CCCCCCCC |

D08 (38,39) Seek Register:

Bit 0 – Reserved
Bits 1–5 – Head Address
Bit 6 – Reserved
Bits 7–15 – Cylinder Address

D09 (40,41) FDM Flags – Condition Flags set by FDM for internal use.

D10 (42,43) File Status (see FA233):

Byte 1:

Bit 0 – Fixed Head Not Selected
Bit 1 – Brake Applied
Bit 2 – Track Not Available
Bit 3 – Command Error
Bit 4 – Data Unsafe
Bit 5 – Seek Incomplete
Bit 6 – Home
Bit 7 – Not Ready

Byte 2 – Reserved

D11 (44,45) File Sense 1 (see FA233):

Byte 1:

Bit 0 – On Track
Bit 1 – Linear Region Normal and Even
Bit 2 – Index and Sector Pulses Missing
Bit 3 – Out Direction
Bit 4 – Not Out Drive
Bit 5 – Not In Drive
Bit 6 – Tag Parity Error
Bit 7 – Velocity Profile Error

Byte 2 – Pulsing Information (same bit definition as Byte 1)

D12 (46,47) File Sense 2 (see FA233):

Byte 1:

Bit 0 – Behind Home
Bit 1 – Missing Clocks ÷ 2
Bit 2 – Not Missing Clocks Error Latch
Bit 3 – Coil Current Low
Bit 4 – Missing Servo Signal
Bit 5 – Off Data Track
Bit 6 – Not Missing Position Error Signals
Bit 7 – Counter 5 In Sync

Byte 2 – Pulsing Information (same bit definition as Byte 1)

13 (48,49) File Sense 3 (see FA233):

Byte 1:

Bit 0 – Not Shift
Bit 1 – Not (Off Track and Write)
Bit 2 – Inside AGC Window
Bit 3 – Not AGC Freeze
Bit 4 – Demod Pulsing
Bit 5 – Not (Read and Write)
Bit 6 – Not (Servo Protect and Write)
Bit 7 – Invalid Move

Byte 2 – Pulsing Information (same bit definition as Byte 1)

## *FA332 DPCX Condition/Incident Log Formats and Meanings*

Disk storage failures are stored in the DPCX condition/incident log in the Type 5 record format. Only those fields necessary for the FA MAPs are identified. See Chapter 2 (CP800) for complete error log details.

**Type 5 Record**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| (1) 5-TYPE | I-REC | (2) SEQ-XXXX | (3) PA-XX | LA-XX | D1-XX | D2-XX | D3-XX | D4-XX |
| (4) D5-PL | D6-XX | D7-XX | D8-XX | D9-XXXXXX | | | | |
| (5) D10-HESC | | (6) D11-HSSS | | (7) D12-HSBS | | | | |
| (8) D13-HSFE | | (9) D14-NANB | | D15-SKRG | | | | |
| D16-XXX | | (10) D17-FS00 | | (11) D18-AFAP | | | | |
| (12) D19-BFBP | | (13) D20-CFCP | | D21-XXXX | | | | |

| | | |
|---|---|---|
| D22-XXXX | D23-XXXX | D24-XXXX |
| D25-XXXX | D26-XXXX | D27-XXXX |
| D28-XXXX | D29-XXXX | D30-XXXX |

**Type 5 Record Description**

(1) Type 5 Indicates an extended variable incident record.

(2) SEQ A four-digit decimal number (0001–4095). This number identifies the relative time the incident occurred.

(3) PA A two-digit number indicating the physical address of the FA adapter/device. (See FA113.)

LA

(4) D5 PL – Partial Logout
Bits 0, 1, 3, 4, 5, 6, 7 – Reserved
Bit 2 – 0 = Complete Logout
1 = Partial Logout

(5) D10 Byte 1 = Data-Handler Extended Status (HE) (see FA233):

Bit 0 – Buffer A to File
Bit 1 – File Speed Good
Bit 2 – Write Protect 1
Bit 3 – Write Protect 0
Bit 4 – Sector Displaced
Bit 5 – Sector Reassigned
Bit 6 – Sector Defective
Bit 7 – Alternate Sector

Byte 2 = Residual Sector Count

Residual Sector Count is not used for intermittent problem determination.

Bits 8–15 Equal the number of remaining sectors for a multisector operation that was terminated with an error.

(6) D11 Byte 1 = Data Handler Basic Status (HS) (see FA233):

Bit 0 – FCB Processor Error
Bit 1 – Data Handler Error
Bit 2 – CRC Error
Bit 3 – ID Error
Bit 4 – Data Field Error
Bit 5 – Sector Not Found
Bit 6 – Equip Check/Halt
Bit 7 – File Write Gate Error

Byte 2 = Seek Status (SS) (see FA233):

Bit 0 – Tag Sequence Error
Bit 1 – Command Error
Bit 2 – FCB Processor Error
Bit 3 – FCB Timeout Error
Bit 4 – Cable Continuity OK
Bits 5–7 – Seek Status:

000 – No MHS, FHS, RECAL in progress
001 – RECAL begun
010 – FHS begun
100 – MHS begun
101 – MHS begun, FHS done
110 – MHS begun, FHS begun
111 – MHS done, FHS begun
MHS = Moving Head Seek
FHS = Fixed Head Seek
RECAL = Recalibrate

(7) D12 Byte 1 = Data Handler Basic Status (HS)

(See D11 field bits 0–7.)

Byte 2 = Basic Status (BS) (see FA233):

Bit 0 – Program Controlled Interrupt
Bit 1 – Device error
Bit 2 – File Interrupt Disabled
Bit 3 – Busy
Bit 4 – Channel Request Frozen
Bit 5 – Equipment Check
Bit 6 – Requests Enabled
Bit 7 – Interrupt

(8) D13 Byte 1 = Data Handler Basic Status (HS)

(See D11 field bits 0–7.)

Byte 2 = FCB Processor Status (FE) (see FA233):

Bit 0 – 0
Bit 1 – 0

Bits 2–7 in hex:

| | |
|---|---|
| 38 | Multisector error |
| 39 | Data Handler error |
| 3A | File error (non-data) |
| 3B | File eror (data related) |
| 3C | Data flow parity error |
| 3D | Control sample timeout |
| 3E | CHIO equipment check |
| 3F | Control bus parity error |

(9) D14 Next Function Request (in hex)

Hold the FCB operation currently being executed.

| Code | Command |
|---|---|
| 0000 | End-Op |
| 0800 | No-Op |
| 0900 | PCI (Program Controlled Interrupt) |
| 0A0X | Load Burst Register |
| 1000 | TIC End-Op |
| 1800 | Load Sector Count |
| 20XX | Read ID Normal |
| 21XX | Read ID Displaced |
| 23XX | Read ID PSC – Normal |
| 24XX | Read ID Compare |
| 26XX | Read ID Immediate |
| 28XX | Write ID |
| 29XX | Write ID Displaced |
| 30XX | Read Sector Normal |
| 34XX | Read Sector Compare |

| | |
|---|---|
| 38XX | Write Sector Normal |
| 3CXX | Write Sector Compare |
| 4200 | Recalibrate |
| 4XX0 | Control Bus — Bit 4 of byte 1 set |
| 5X00 | Store Memory Control |
| 60XX | Read Back Check Normal |
| 64XX | Read Back Check Compare |
| 6X00 | Buffer Diagnostic — Bit 4 of byte 1 set |
| 71XX | Retrieve |
| 78XX | Format |
| 8YYY | Seek (Moving Heads) |
| 9YYY | Seek (Moving Heads) |
| AYYY | Seek (Fixed Heads) |
| CYYY | Store New Track (Moving Heads) |
| DYYY | Store New Track (Moving Heads) |
| EYYY | Store New Track (Fixed Heads) |

YYY bit layout = BBFHHHHC CCCCCCCC

where: BB = 10 = seek
11 = store new track

F = 1 = fixed head select
0 = moving head select

HHHH = head address

CCCCCCCCC = cylinder address

Examples (in hex):

| | | | | | | |
|---|---|---|---|---|---|---|
| 1. Seek to moving head 5, cylinder 128 | 10 | 0 | 0101 | 1 | 00101000 |
| 2. Seek to fixed head 3 (cylinder address not applicable) | 10 | 1 | 0011 | C | CCCCCCCC |
| 3. Store new track moving head 2, cylinder 167 | 11 | 0 | 0010 | 1 | 01100111 |
| 4. Store new track fixed head 7 (cylinder address not applicable) | 11 | 1 | 0111 | C | CCCCCCCC |

D15 Seek Register:

Bit 0 — Reserved
Bits 1–5 — Head Address
Bit 6 — Reserved
Bits 7–15 — Cylinder Address

(10) D17 Byte 1 = File Status (FS) — (in hex) (see FA233):

| | | |
|---|---|---|
| Bit 0 | — Fixed Head Not Selected | 80 |
| Bit 1 | — Brake Applied | 40 |
| Bit 2 | — Track Not Available | 20 |
| Bit 3 | — Command Error | 10 |
| Bit 4 | — Data Unsafe | 08 |
| Bit 5 | — Seek Incomplete | 04 |
| Bit 6 | — Home | 02 |
| Bit 7 | — Not Ready | 01 |

Byte 2 = Reserved

(11) D18 Byte 1 = File Sense 1 (AF) — (in hex) (see FA233):

| | | |
|---|---|---|
| Bit 0 | — On Track | 80 |
| Bit 1 | — Linear Region Normal and Even | 40 |
| Bit 2 | — Index and Sector Pulses Missing | 20 |
| Bit 3 | — Out Direction | 10 |
| Bit 4 | — Not Out Drive | 08 |
| Bit 5 | — Not In Drive | 04 |
| Bit 6 | — Tag Parity Error | 02 |
| Bit 7 | — Velocity Profile Error | 01 |

Byte 2 = Pulsing Sense 1 (AP) (same bit definition as Byte 1)

(12) D19 Byte 1 = File Sense 2 (BF) — (in hex) (see FA233):

| | | |
|---|---|---|
| Bit 0 | — Behind Home | 80 |
| Bit 1 | — Missing Clocks ÷ 2 | 40 |
| Bit 2 | — Not Missing Clocks Error Latch | 20 |
| Bit 3 | — Coil Current Low | 10 |
| Bit 4 | — Missing Servo Signal | 08 |
| Bit 5 | — Off Data Track | 04 |
| Bit 6 | — Not Missing Position Error Signals | 02 |
| Bit 7 | — Counter 5 In Sync | 01 |

Byte 2 = Pulsing Sense 2 (BP) (same bit definition as Byte 1)

(13) D20 Byte 1 = File Sense 3 (CF) (see FA233):

Bit 0 — Not Shift
Bit 1 — Not (Off Track and Write)
Bit 2 — Inside AGC Window
Bit 3 — Not AGC Freeze
Bit 4 — Demod Pulsing
Bit 5 — Not (Read and Write)
Bit 6 — Not (Servo Protect and Write)
Bit 7 — Invalid Move

Byte 2 = Pulsing Sense 3 (CP) (same bit definition as Byte 1)

## FA340 How to Use the Error Log

The procedure for examining the error log depends upon whether the customer is using DPPX or DPCX. For the DPPX operating system, see FA341; for DPCX, see FA342.

### *FA341 Using the DPPX Error Log*

Examine the error log for the failing DSD. Using FA331 (DPPX Error Log Formats and Meanings) identify the latest error log with a complete logout of the most frequent failure type (Field D01 = hex 00XX for a complete logout and hex 20XX for a partial logout). Also a complete logout has valid pulsing bits in Fields 45, 47, and 49. If there are no complete logout records, use the latest partial logout record. When instructed to by the MD display, enter the requested data fields from this error log. The MD will display the action plan. To verify the repair, return the system to the customer. Obtain a new error log after the customer has used the system. End the repair action when there are no FA failures in the error log.

### *FA342 Using the DPCX Condition/Incident Log*

Examine the condition/incident log records for the failing DSD. Using FA332, identify the latest condition/incident log with a complete logout of the most frequent failure type (Field D5 = hex 00 for a complete logout and hex 20 for a partial logout). Also a complete logout has valid pulsing bits in Fields D18, D19 and D20. If there are no complete logout records, use the latest partial logout record. When instructed to by the MD display, enter the requested

data fields from this log record. The MD will display the action plan. To verify the repair, return the system to the customer. Obtain a new error log after the customer has used the system. End repair action when there are no FA failures in the error log.

### FA350 Action Plan to Correct Intermittent Failures

This procedure assumes that there is an intermittent hardware failure. It is also possible, however, that the problem may be a defective/intermittent ID or data field on the customer surface. Since the diagnostic tests utilize only the CE track (359), customer surface problems will not be detected. In such cases, it is recommended that the Surface Status and Format utility be run on the entire file (refer to CP653).

1. The offline tests should have been run.
   a. If they have not been run, go to FA250.
   b. If there were random errors, go to step 2.
   c. If the tests were looped without error for five passes, go to step 8.
2. Obtain the error log for failing DSD physical address (PA). Refer to Chapter 2 (CP700 for DPPX; CP800 for DPCX) for information on obtaining the error log.
3. Enter into the MD the information from the latest complete logout record of the most frequent type of failure (see FA340). If there are no complete logouts, use the latest partial logout.
4. The MD display recommends FRU replacements or possible causes of failure in the order of probable cause. Replace and record the FRUs. (If, after all recommended FRUs have been replaced, the problem still exists, request aid.)
5. Loop the tests for five passes. Enter "F" into the MD keyboard to end looping. If there is a failure, the MD will continue prompting.
6. Return the system to the customer.
7. End Repair action when there are no more DSD failures in the error log after a satisfactory period.
8. If the drive has fixed heads installed, run Routine 50 in free-lance mode (this is a special test for "write" capabilities of the fixed heads). If there are no fixed heads or Routine 50 runs without error, go to step 2.

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## FA400 Signal Paths and Detailed Operational Description

This section contains card socket wiring charts, board and card jumpers, and detailed operational description.

### FA410 Card Socket Wiring Charts

This section shows the card pins and associated line names. Where possible, input/output directions are shown with arrows. See FA111 for card locations.

*FA1 FCB Processor Card*

| | | | | | |
|---|---|---|---|---|---|
| SC5 | - data bit P (0-7) | P10 | B12 | - int/req/bus in 0 | |
| SC5 | - data bit 0 | S04 | B08 | - end of chain | SC5 |
| SC5 | - data bit 1 | U11 | B09 | - IRR | SC5 |
| SC5 | - data bit 2 | S07 | G02 | - valid halfword | SC5 |
| SC5 | - data bit 3 | U05 | D05 | - parity valid | SC5 |
| SC5 | - data bit 4 | U10 | J02 | - ch req low | SC5 |
| SC5 | - data bit 5 | S13 | D04 | + 9 MHz | FA2 |
| SC5 | - data bit 6 | S08 | G09 | | FA2 |
| SC5 | - data bit 7 | M10 | J11 | | FA2 |
| SC5 | - data bit P (8-15) | U12 | B13 | - 4V reg | FA2 |
| SC5 | - data bit 8 | S09 | J06 | + file bus degate | FA2-FA4 |
| SC5 | - data bit 9 | S10 | G07 | - tag bit P | FA4 |
| SC5 | - data bit 10 | U02 | G12 | - tag bit 2 | FA4 |
| SC5 | - data bit 11 | S05 | G10 | - tag bit 1 | FA4 |
| SC5 | - data bit 12 | U13 | G13 | - tag bit 0 | FA4 |
| SC5 | - data bit 13 | U04 | M12 | - control sample | FA4 |
| SC5 | - data bit 14 | U07 | P06 | - data select | FA4 |
| SC5 | - data bit 15 | S12 | M13 | - reset error | FA4-FA5 |
| SC5 | - ch grant low | G03 | G04 | - ch grant low pass (TP) | |
| SC5 | - system reset | M05 | B02 | + sample clock (TP) | |
| SC5 | - TA tag | M08 | G05 | | |
| SC5 | - I/O tag | D13 | J13 | | |
| SC5 | - halt tag | J04 | P05 | + gate bus driver on (VE) | |
| SC5 | - TD tag | P02 | U06 | | |
| FA2 | - DH stat bit P | D07 | D08 | ground | |
| FA2 | - DH stat bit 0 | D12 | B07 | - tie down | |
| FA2 | - DH stat bit 1 | D10 | M02 | | |
| FA2 | - DH stat bit 2 | D06 | M09 | | |
| FA2 | - DH stat bit 3 | B10 | P09 | | |
| FA2 | - DH stat bit 4 | D11 | P11 | | |
| FA2 | - DH stat bit 5 | S02 | P12 | | |
| FA2 | - DH stat bit 6 | D09 | P13 | | |
| FA2 | - DH stat bit 7 | D02 | U09 | | |
| FA2 | + continuity to ctrl ad | M07 | | | |
| FA2 | - clock ring reset | J05 | | | |
| FA4 | - control bus bit P* | J12 | | | |
| FA4 | - control bus bit 0* | J10 | | | |
| FA4 | - control bus bit 1* | J09 | | | |
| FA4 | - control bus bit 2* | B03 | | | |
| FA4 | - control bus bit 3* | J07 | | | |
| FA4 | - control bus bit 4* | G08 | | | |
| FA4 | - control bus bit 5* | M04 | | | |
| FA4 | - control bus bit 6* | M03 | | | |
| FA4 | - control bus bit 7* | P04 | | | |
| FA4 | - cntl sample recd | B04 | | | |
| FA4 | - file interrupt | B05 | | | |

| Volts | Pins |
|---|---|
| PA + 5 VDC | D03, J03, P03, U03 |
| PA + 8.5 VDC | B11, G11, M11, S11 |
| PA - 5 VDC | B06, G06, M06, S06 |
| PA Ground | D08, J08, P08, U08 |

*Bi-directional bus

(TP) = test point

*FA2 Data Handler Card*

| | | | | | |
|---|---|---|---|---|---|
| SCF | + gate bus driver on (VE) | G10 | D07 | - DH stat bit P | FA1 |
| SC5 | - system reset | G09 | D12 | - DH stat bit 0 | FA1 |
| SC5 | - release | J13 | D10 | - DH stat bit 1 | FA1 |
| FA1 | - 4V reg | B13 | D06 | - DH stat bit 2 | FA1 |
| FA1 | + 9 MHz | S10 | B10 | - DH stat bit 3 | FA1 |
| FA1 | + file bus degate | J12 | D11 | - DH stat bit 4 | FA1 |
| FA3 | 1F read clock | G07 | B02 | - DH stat bit 5 | FA1 |
| FA3 | 1F write clock | J06 | B09 | - DH stat bit 6 | FA1 |
| FA3 | + NRZ data | G08 | D02 | - DH stat bit 7 | FA1 |
| FA3 | + write gate return | M04 | G12 | - clock ring reset | FA1 |
| FA5 | - index | B03 | M02 | + continuity from cntl | FA1 |
| FA5 | - sector | D04 | J09 | - fast sync | FA3 |
| FA5 | - sector pulses missing | D09 | J11 | - write data | FA3 |
| | + write load (TP) | B04 | G13 | - write | FA4 |
| | | B05 | J07 | - read | FA4 |
| | + gate P clock (TP) | B07 | D08 | ground | |
| | | B08 | G05 | - tie down | |
| | + select clock (TP) | B12 | M03 | | |
| | | D13 | U10 | | |
| | | G02 | | | |
| | | G03 | | | |
| | | J02 | | | |
| | + byte start (TP) | J04 | | | |
| | | J10 | | | |

| Volts | Pins |
|---|---|
| PA + 5 VDC | D03, J03, P03, U03 |
| PA + 8.5 VDC | B11, G11, M11, S11 |
| PA - 5 VDC | B06, G06, M06, S06 |
| PA Ground | D08, J08, P08, U08 |

(TP) = test point

## *FA3 Data Channel Card*

| | | |
|---|---|---|
| FA2 | - fast sync | S02 |
| FA2 | - write data | U02 |
| FA4 | - head select 1 | P07 |
| FA4 | - head select 2 | P05 |
| FA4 | - head select 4 | P10 |
| FA4 | - head select 8 | P06 |
| FA4 | + write select | G13 |
| FA4 | + read select | J12 |
| FA4 | - servo unsafe | M02 |
| FA4 | + common reset | M03 |
| FA4 | - fixed head select | M05 |
| FA4 | + write clock | J06 |
| FA5 | - AGC freeze | B04 |
| FA6 | 2F write clock | M10 |
| FA6 | + servo VCO inhibit | U06 |
| DE | center taps | G03 |
| DE | actuator I/O line A | D05 |
| DE | actuator I/O line B | D06 |
| DE | fixed head I/O line A | D10 |
| DE | fixed head I/O line B | D09 |
| DE | M safety | D11 |
| DE | + data select gated | P12 |
| | - I write select (TP) | B05 |
| | - read actr (TP) | B07 |
| | - 1.32V int (TP) | B08 |
| | + 5.8V int (TP) | B09 |
| | - read fixed heads (TP) | B10 |
| | - diff analog signal (TP) | B13 |
| | write I def res (TP) | D04 |
| | diff analog signal (TP) | D13 |
| | AGC ref volt (TP) | G02 |
| | - multi module select (TP) | G04 |
| | + IW error squelch (TP) | G05 |
| | trans error (TP) | G07 |
| | - 1.32V ref (TP) | G08 |
| | - sat squelch (TP) | G09 |
| | - heads grounded (TP) | G11 |
| | + write DC (TP) | G12 |
| | AGC control volt (TP) | J02 |
| | + inhibit trans error (TP) | J04 |

| | | |
|---|---|---|
| S07 | + NRZ data | FA2 |
| J07 | + write gate return | FA2 |
| U07 | 1F read clock | FA2 |
| U11 | 1F write clock | FA2 |
| G10 | + data unsafe | FA4 |
| U12 | 1F wrt clk ungated to PLO | FA5 |
| B02 | - buffered analog data A | FA6 |
| B03 | - buffered analog data B | FA6 |
| P11 | data servo 2F burst | FA6 |
| B12 | - M positive supply | DE |
| M04 | head select A | DE |
| P04 | head select B | DE |
| P09 | - module select 1 | DE |
| M11 | - module select 2 | DE |
| M09 | - module select 3 | DE |
| M08 | - module select 4 | DE |
| M07 | - module select 5 | DE |
| D07 | write current | DE |
| J05 | - IW during read (TP) | |
| J09 | transient blanking (TP) | |
| J10 | - multi module sel error (TP) | |
| J11 | - head ground error (TP) | |
| J13 | shift reg shift pul (TP) | |
| M12 | - servo sample (TP) | |
| M13 | inhibit SS (TP) | |
| P02 | - operation (TP) | |
| P13 | data (TP) | |
| S03 | combined data (TP) | |
| S04 | OP ext (TP) | |
| S05 | tie up (-0.8V) (TP) | |
| S08 | test data I/P (TP) | |
| S09 | 1F read clock MST (TP) | |
| S10 | zener +2V (TP) | |
| S11 | increase (TP) | |
| S12 | decrease (TP) | |
| U04 | + gate test data (TP) | |
| U05 | internal fast sync (TP) | |
| U09 | high current (TP) | |
| U10 | data SS (TP) | |
| U13 | VCO error signal (TP) | |

| Volts | | Pins |
|---|---|---|
| PA | + 5 VDC | D03, J03, P03, U03 |
| PA | + 12 VDC | B11 |
| PA | Ground | D08, J08, P08, U08 |
| PA | - 4 VDC | B06, G06, M06, S06 |
| PA | - 12 VDC | D12 |

(TP) = test point

## *FA4 Logic Card 1*

| | | |
|---|---|---|
| FA1 | + file bus degate | B03 |
| FA1 | - control sample | G09 |
| FA1 | - tag bit P | M08 |
| FA1 | - tag bit 0 | P07 |
| FA1 | - tag bit 1 | M07 |
| FA1 | - tag bit 2 | M09 |
| FA1 | - reset error | S10 |
| FA1 | - data select | J13 |
| FA2 | - write | G12 |
| FA2 | - read | J11 |
| FA3 | + data unsafe | M11 |
| FA5 | profile gain voltage | B02 |
| FA5 | + half track (REL) | B04 |
| FA5 | - go home or P.O.F.L. | B06 |
| FA5 | + brake applied (logic) | B08 |
| FA5 | missing clocks 2 | B10 |
| FA5 | - index sector pulses | G08 |
| FA5 | + servo protect | G10 |
| FA5 | pulsing and O/P | M10 |
| FA5 | - in drive | M13 |
| FA5 | + missing servo sig latch | S02 |
| FA5 | + byte cntr bit 16 | S03 |
| FA5 | - count down 2 tracks | S05 |
| FA5 | - count up 2 tracks | S06 |
| FA5 | + not ready | S08 |
| FA5 | + quarter track (REL) | D04 |
| FA5 | + lin reg N of even trk | D11 |
| FA5 | + behind home | D13 |
| FA5 | - AGC freeze | J02 |
| FA5 | + out direction | J07 |
| FA5 | - missing clk err latch | J09 |
| FA5 | - seek complete | P11 |
| FA5 | - out drive | U02 |
| FA5 | + ROS DA error | U04 |
| FA5 | + move not valid | U05 |
| FA5 | - ABS track address 1 | U06 |
| FA5 | + home | U07 |
| FA5 | - cntr 5 out of sync | U10 |
| FA5 | + seek timeout | U13 |
| FA6 | - outside AGC window | G03 |
| FA6 | + off data track | G13 |
| FA7 | + on track | B12 |
| FA7 | + low coil current | G07 |
| FA7 | - power on delay | S13 |
| FA7 | - bad AGC level | U11 |

| | | |
|---|---|---|
| P04 | - control bus bit P* | FA1 |
| M04 | - control bus bit 0* | FA1 |
| P02 | - control bus bit 1* | FA1 |
| M03 | - control bus bit 2* | FA1 |
| M02 | - control bus bit 3* | FA1 |
| M05 | - control bus bit 4* | FA1 |
| P06 | - control bus bit 5* | FA1 |
| P05 | - control bus bit 6* | FA1 |
| M06 | - control bus bit 7* | FA1 |
| D06 | - file interrupt | FA1 |
| P09 | - cntl sample recd | FA1 |
| P12 | - head select 1 | FA3 |
| P10 | - head select 2 | FA3 |
| J06 | - head select 4 | FA3 |
| G02 | - head select 8 | FA3 |
| G11 | + write clock | FA3 |
| S11 | - servo unsafe | FA3 |
| J12 | + read select | FA3 |
| U12 | + write select | FA3 |
| U09 | + common reset | FA3 |
| D09 | - fixed head select | FA3 |
| B13 | - shift | FA5 |
| G04 | - go home bit | FA5 |
| G05 | - calibration address | FA5 |
| M12 | + head 1 selected | FA5 |
| S07 | - set seek | FA5 |
| D02 | + desired velocity | FA5 |
| D05 | - reset calibration | FA5 |
| D07 | - tag 001 clock 2 | FA5 |
| J05 | + out | FA5 |
| S09 | - even | FA6-FA7 |
| S12 | + data select gated | DE |
| B05 | - tag 010 CS (TP) | |
| B07 | EMROS parity (TP) | |
| B09 | - force DAC O/P to 0 (TP) | |
| D10 | + rel trk addr 128 (TP) | |
| G06 | - tag 001 CS no fxhd (TP) | |
| J04 | + track unavailable (TP) | |
| J10 | + 1/2 TTG (TP) | |
| P13 | + data S110 (TP) | |
| S04 | + common reset (TP) | |

| Volts | | Pins |
|---|---|---|
| PA | + 5 VDC | D03, J03, P03, U03 |
| PA | + 12 VDC | B11 |
| PA | Ground | D08, J08, P08, U08 |
| PA | - 12 VDC | D12 |

*Bidirectional bus

(TP) = test point

## *FA5 Logic Card 2*

| | | |
|---|---|---|
| FA1 | - reset error | P13 |
| FA3 | 1F wrt clk ungated to PLO | J05 |
| FA4 | + desired velocity | B02 |
| FA4 | - calibration address | M08 |
| FA4 | - set seek | M12 |
| FA4 | - shift | S04 |
| FA4 | - tag 001 clock 2 | S09 |
| FA4 | - fixed head select | J04 |
| FA4 | + head 1 selected | P09 |
| FA4 | - reset calibration | P11 |
| FA4 | - go home bit | P12 |
| FA4 | + out | U02 |
| FA7 | - Q/2 error | B07 |
| FA7 | coil current signal | B09 |
| FA7 | + servo clock SS | G05 |
| FA7 | - power good delayed | M09 |
| FA7 | + N/2 error | S12 |
| FA7 | + Q/2 error | J07 |
| FA7 | - missing servo clock | P06 |
| FA7 | - power on delay | U09 |
| FA7 | - N/2 error | U12 |
| DE | compensation coil | D04 |
| DE | compensation coil (GND) | P08 |
| | + vel > profile (TP) | B04 |
| | + counter 5 (TP) | B12 |
| | + (G + N) (TP) | G06 |
| | - common reset (TP) | G12 |
| | + quad error (TP) | M05 |
| | - cntr 4 (TP) | M06 |
| | rel track addr 128 (TP) | M10 |
| | + V timeout (TP) | M11 |
| | handover vel (TP) | S03 |
| | dedicated ready (TP) | S11 |
| | - hybrid velo (TP) | D02 |
| | QSW (up open) (TP) | J11 |
| | NSW (up closed) (TP) | J12 |
| | + seek timeout SS (TP) | U05 |

| | | |
|---|---|---|
| G08 | - sector pulses missing | FA2 |
| S10 | - sector | FA2 |
| S13 | - index | FA2 |
| G09 | - AGC freeze | FA3-FA4 |
| B03 | + lin reg N or even track | FA4 |
| B05 | - ABS track address 1 | FA4 |
| B08 | profile gain voltage | FA4 |
| B10 | + quarter track (REL) | FA4 |
| G07 | - cntr 5 out of sync | FA4 |
| M02 | + missing servo sig latch | FA4 |
| M03 | - missing clk err latch | FA4 |
| M04 | pulsing and O/P | FA4 |
| M07 | + not ready | FA4 |
| M13 | + seek timeout | FA4 |
| S08 | + byte cntr bit 16 | FA4 |
| D05 | - count up 2 tracks | FA4 |
| D07 | - count down 2 tracks | FA4 |
| D09 | + ROS DA error | FA4 |
| D10 | + half track (REL) | FA4 |
| P02 | missing clocks 2 | FA4 |
| P04 | + move not valid | FA4 |
| P05 | - index sector pulses | FA4 |
| P10 | + home | FA4 |
| U06 | + servo protect | FA4 |
| U10 | - go home or P.O. F. L. | FA4 |
| U11 | + behind home | FA4 |
| S07 | - in drive | FA4-FA7 |
| D06 | + out direction | FA4-FA7 |
| J13 | - seek complete | FA4-FA7 |
| P07 | + brake applied (logic) | FA4-FA7 |
| U07 | - out drive | FA4-FA7 |
| B13 | - osc early | FA6 |
| D13 | + head change gate | FA6 |
| J02 | - osc late | FA6 |
| J09 | + shift reg clock | FA6 |
| J10 | + enable servo sample | FA6 |
| U13 | + enable mark detect | FA6 |
| G02 | - select demod Q2 | FA7 |
| G03 | - select demod Q1 | FA7 |
| J06 | - select demod N2 | FA7 |
| G04 | - select demod N1 | FA7 |
| G13 | + normal error | FA7 |
| S05 | - select integrator | FA7 |
| D11 | + seek | FA7 |
| U04 | - sector integrator | FA7 |
| G10 | brake coil 1 | DE |
| G11 | brake applied to power | PA |

| Volts | | Pins |
|---|---|---|
| PA | + 5 VDC | D03, J03, P03, U03 |
| PA | + 12 VDC | B11 |
| PA | + 24 VDC | S02 |
| PA | Ground | D08, J08, P08, U08 |
| PA | - 12 VDC | D12 |

(TP) = test point

## *FA6 Servo Card 1*

| | | |
|---|---|---|
| FA3 | buffered analog data A | B03 |
| FA3 | buffered analog data B | D02 |
| FA3 | data servo 2F burst | G08 |
| FA4 | - even | J06 |
| FA5 | + enable mark detect | G04 |
| FA5 | - osc early | G07 |
| FA5 | + shift reg clock | G10 |
| FA5 | + head change gate | D11 |
| FA5 | + enable servo sample | J04 |
| FA5 | - osc late | J07 |
| FA7 | VTP 1 ref | B04 |
| FA7 | + on track | G13 |
| FA7 | - 7 volts | D10 |
| FA7 | - dedicated sw PES | D13 |
| | + AGC control (TP) | B02 |
| | VCO (TP) | B05 |
| | reset bucket | B07 |
| | linear data sig (TP) | B08 |
| | - reset cap (TP) | B10 |
| | + positive zero crossing (TP) | B12, G05 |

| | | |
|---|---|---|
| G03 | + servo VCO inhibit | FA3 |
| G12 | 2F write clock | FA3 |
| D09 | - outside AGC window | FA4 |
| J13 | + off data track | FA4 |
| B13 | data PES | FA7 |
| G02 | + select demod A (TP) | |
| G11 | - B (TP) | |
| G09 | - D (TP) | |
| B09 | - G (TP) | |
| D04 | AGC ref (TP) | |
| D05 | + 6 volts (TP) | |
| D06 | linear data signal (TP) | |
| D07 | + select gain adj (TP) | |
| J02 | + demod 8 (TP) | |
| J05 | - counter run (TP) | |
| J09 | - bit 0 (TP) | |
| J10 | + enable data (TP) | |
| J11 | - enable data (TP) | |
| J12 | 2F write clock (TP) | |

| Volts | | Pins |
|---|---|---|
| PA | + 5 VDC | D03, J03 |
| PA | + 12 VDC | B11 |
| PA | Ground | D08, J08 |
| PA | - 4 VDC | B06, G06 |
| PA | - 12 VDC | D12 |

(TP) = test point

## *FA7 Servo Card 2*

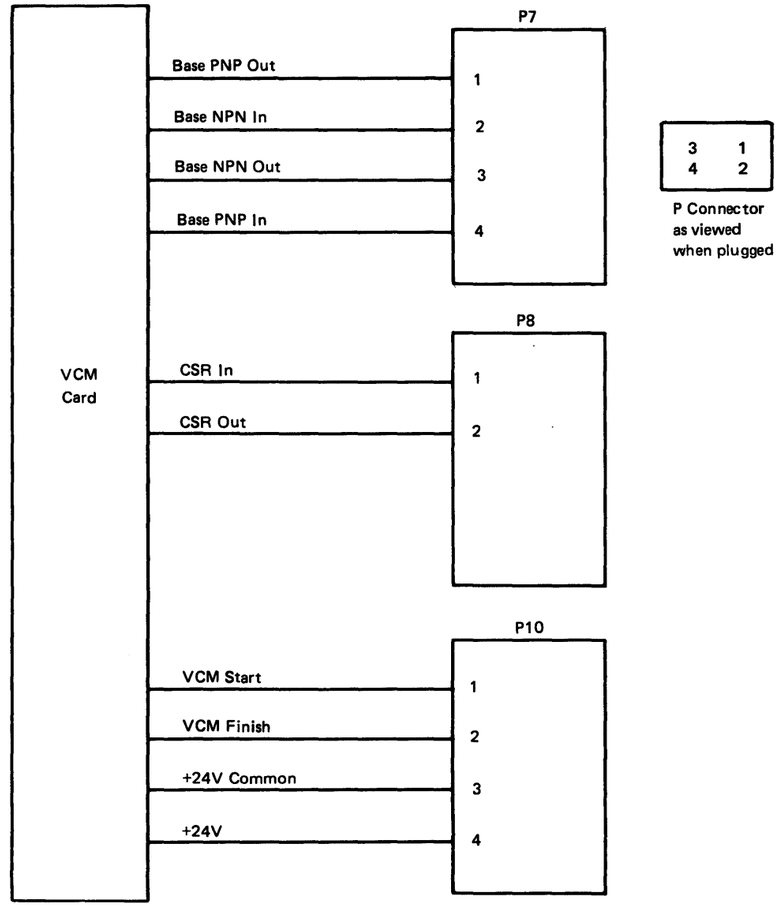
| | | | | | |
|---|---|---|---|---|---|
| FA4 | – even | B03 | G03 | + low coil current | FA4 |
| FA5 | – select demod Q1 | B08 | J04 | – bad AGC level | FA4 |
| FA5 | – select demod Q2 | B09 | G12 | + on track | FA4-FA6 |
| FA5 | – select demod N1 | D09 | P02 | – power on delay | FA4-FA5 |
| FA5 | – select demod N2 | B10 | B04 | + servo clock SS | FA5 |
| FA5 | + normal | B12 | G13 | – missing servo clock | FA5 |
| FA5 | + brake applied (logic) | M02 | M08 | – N/2 error | FA5 |
| FA5 | – out drive | M13 | S02 | + Q/2 error | FA5 |
| FA5 | – seek complete | S07 | S10 | coil current signal | FA5 |
| FA5 | + seek | S08 | D11 | – Q/2 error | FA5 |
| FA5 | + out direction | S13 | D13 | + N/2 error | FA5 |
| FA5 | – select integrator | P05 | P09 | – power good delayed | FA5 |
| FA5 | + select integrator | P07 | B07 | VPT 1 ref | FA6 |
| FA5 | – in drive | P11 | D02 | – dedicated sw PES | FA6 |
| FA6 | data PES | P06 | D10 | – 7 volts | FA6 |
| FA8 | + 24V common | S09 | J10 | | |
| DE | – servo preamp O/P | D05 | P10 | | |
| DE | + servo preamp O/P | D06 | U10 | | |
| PA | – power good | G10 | M12 | base PNP out | FA8 |
| | tribits (TP) | B02 | S05 | CSR out | FA8 |
| | hybrid PES Q (TP) | G04 | U02 | base NPN out | FA8 |
| | on track threshold cntl (TP) | G05 | U04 | base NPN in | FA8 |
| | hybrid PES (TP) | G09, J11 | U05 | CSR in | FA8 |
| | ret spring curr comp (TP) | M03 | U07 | base PNP in | FA8 |
| | integrator (TP) | M07 | M04 | VCM finish | FA8-DE |
| | + M servo clock (TP) | M09 | M05 | VCM start | FA8-DE |
| | notch filter amp O/P (TP) | M10 | S04 | SPA – 8V | DE |
| | base 179 in (TP) | S03 | J05 | DE adj res B | DE |
| | + NSW (TP) | S12 | J08 | DE adj res A | DE |
| | + VGA (TP) | D04 | P13 | base 179 out (TP) | |
| | + sw sequence (TP) | J02 | U03 | – servo offset inj (TP) | |
| | hybrid PES N (TP) | J09 | U09 | driver preamp SS (TP) | |
| | – comp I O/P (TP) | J13 | U11 | pre-driver I/P (TP) | |
| | integrator O/P (TP) | P04 | U13 | servo offset (TP) | |

| Volts | Pins |
|---|---|
| PA + 5 VDC | D03, J03, P03 |
| PA + 12 VDC | B05, B11, G11, M11, S11 |
| PA + 24 VDC | G02 |
| PA Ground | D08, J08, P08, U08 |
| PA – 4 VDC | B06, G06, M06, S06 |
| PA – 12 VDC | D12, J12, P12, U12 |

(TP) = test point

## *FA8 Voice Coil Motor (VCM) Drive Card*

(Located on the side of the 01X–A1 Gate.)

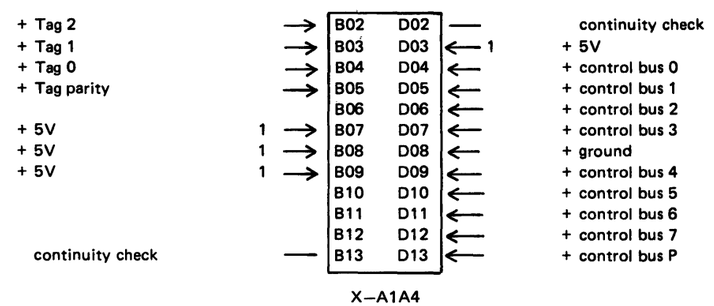






P Connector as viewed when plugged

## *FA9 Terminator Card*




X–A1A4

**Note:** *Numbers indicate common connections.*

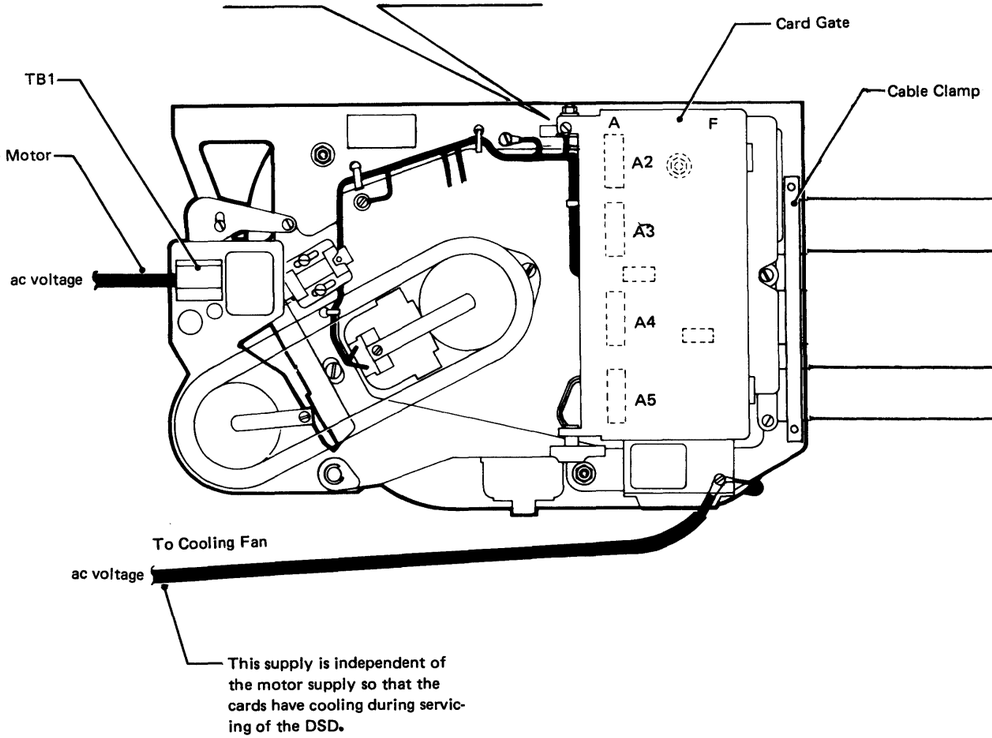
*Adapter to Drive Cables, (CC) and (DD)*

CONNECTIONS

The routing of this cable depends on the Unit 8130, 8140, or 8101

Brake Cable
+ 24V
+ 24V
+ 12V
+ 5V
– 4V
– 12V
From Power Supplies

J1-2 – Power Good – From power supply logic
Ground – From power supply logic
J5-1 – Brake Applied – To power supply logic




(CC)

| | | | | |
|---|---|---|---|---|
| + tags bit 2 | → B02 | | D02 → | + continuity to adapter |
| + tags bit 1 | → B03 | | D03 — | |
| + tags bit 0 | → B04 | | D04 ← | + control bus bit 0 |
| + tags bit P | → B05 | | D05 ← | + control bus bit 1 |
| | — B06 | | D06 ← | + control bus bit 2 |
| | — B07 | | D07 ← | + control bus bit 3 |
| | — B08 | | D08 ← | + ground |
| | — B09 | | D09 ← | + control bus bit 4 |
| | — B10 | | D10 ← | + control bus bit 5 |
| | — B11 | | D11 ← | + control bus bit 6 |
| + control sample rcvd | ← B12 | | D12 ← | + control bus bit 7 |
| + continuity | → B13 | | D13 ← | + control bus bit P |

Control Cable (CC)

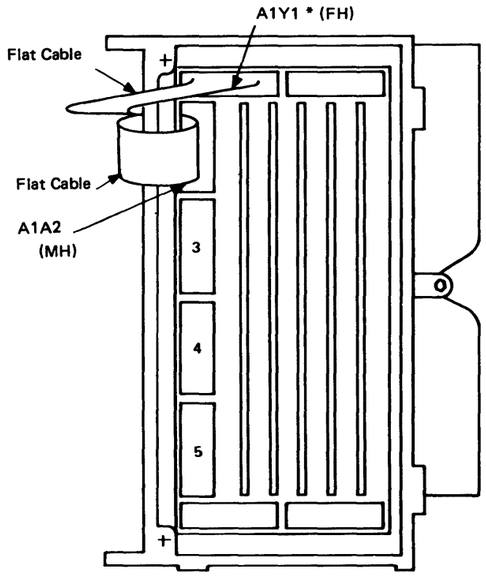
Dedicated Cable (DD)

| | | | | |
|---|---|---|---|---|
| + continuity from adapter | → B02 | | D02 ← | + ground |
| + control sample | → B03 | | D03 → | – write gate return |
| + disk interrupt | ← B04 | | D04 ← | + data select |
| – sector | ← B05 | | D05 ← | – fast sync |
| | — B06 | | D06 ← | + reset error |
| + ground | → B07 | | D07 → | – index |
| + NRZI data | ← B08 | | D08 ← | + ground |
| – sector pulse missing | ← B09 | | D09 ← | – read select |
| – write data | → B10 | | D10 → | + read clock |
| | — B11 | | D11 ← | – write select |
| + disk bus degate | → B12 | | D12 → | + write clock |
| + ground | → B13 | | D13 → | + continuity |

(DD)

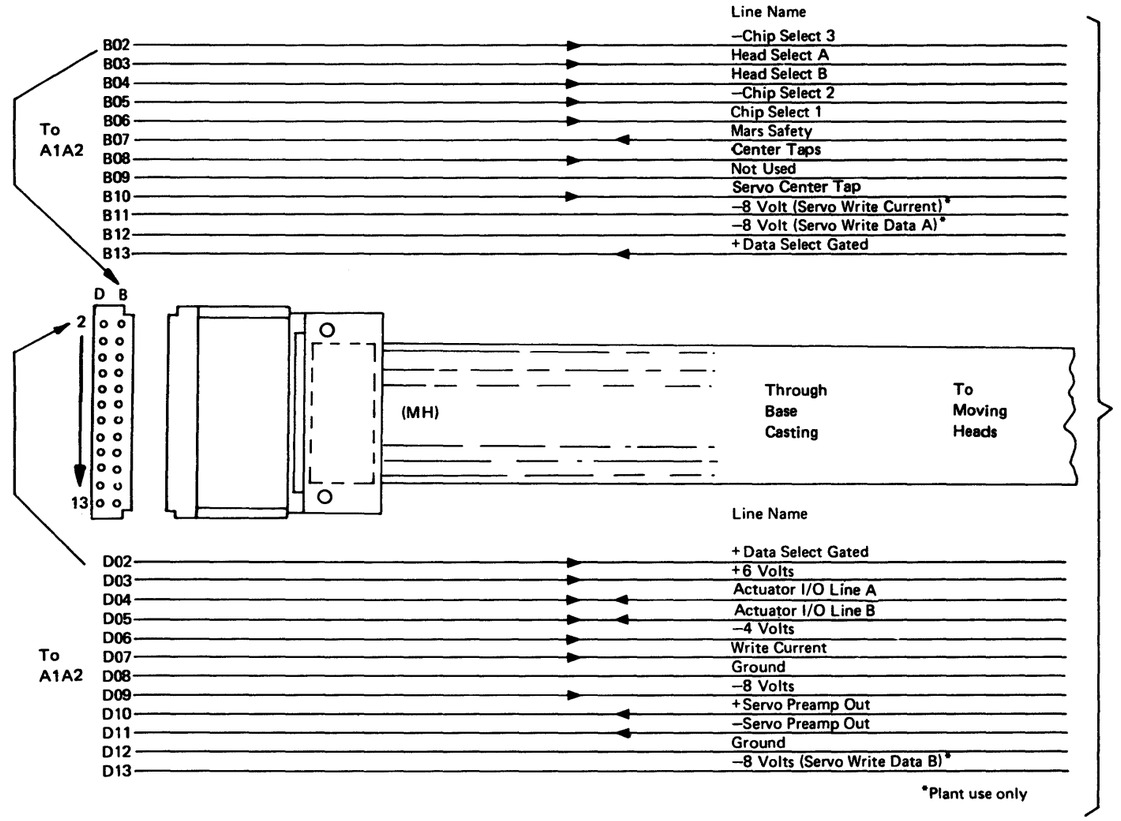
## *Drive Logic Board to DE Cables, (FA) and (MH)*

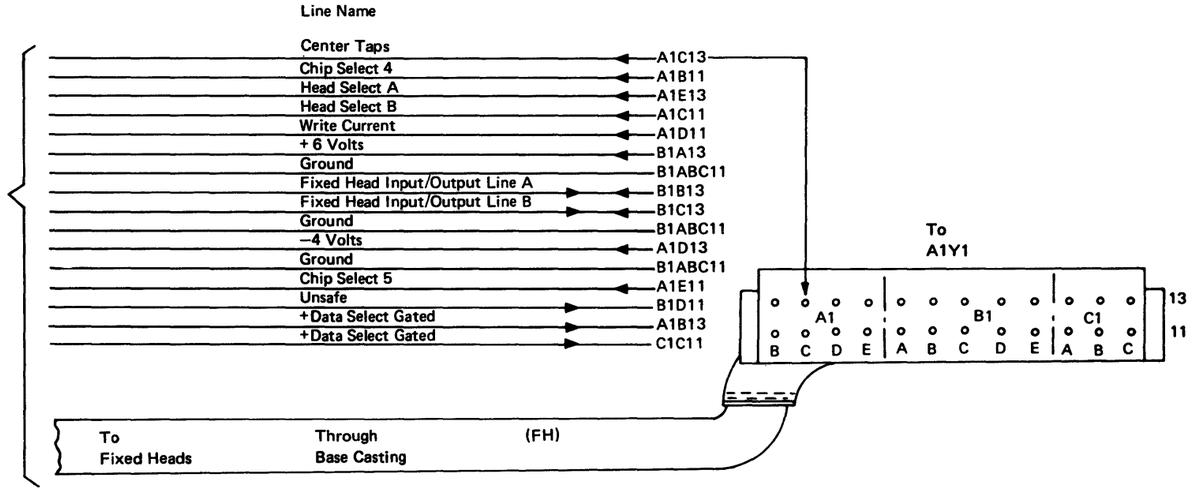
Pin connections and signal titles for both the fixed and moving head flat cables are shown.




Card Gate with Cover Removed, Showing (MH) and (FH) Plug Positions

*(FH) is installed only when the fixed head feature is installed.

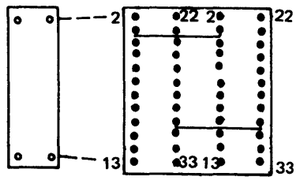


*Top Card Connectors W, X, Y, and Z*

| | | | | |
|---|---|---|---|---|
| – dh valid | ← | W22 | W02 | → – dh csr |
| – dh eoc | ← | W23 | W03 | → – sync clk (b) |
| – sync clk (c) | → | W24 | W04 | — + ground |
| + dflow bus bit 2 | → | W25 | W05 | ← + dflow bus bit 7 |
| + spiral 1 | → | W26 | W06 | ← – sampled td |
| + dflow bus bit 5 | → | W27 | W07 | ← – td sync |
| – gt in status | → | W28 | W08 | ← + spiral 2 |
| – ctl csr | → | W29 | W09 | ← – sync clk (b) |
| – XXX clock | → | W30 | W10 | ← + dflow bus pty |
| + ground | → | W31 | W11 | ← – sync clock (c) |
| + dflow bus bit 6 | → | W32 | W12 | ← + gt dh x st |
| + dflow bus bit 1 | → | W33 | W13 | ← – dhi 0 |
| + dflow bus bit 0 | → | X22 | X02 | ← + dflow bus bit 4 |
| – nfr sel | ← | X23 | X03 | ← + skip factor 1 |
| – dhi 1 | → | X24 | X04 | — + ground |
| + dflow bus bit 3 | → | X25 | X05 | → – dhctl/ops 0 |
| – sync clock (p) | ← | X26 | X06 | → + dflo sel |
| + cs attached | → | X27 | X07 | → – dhctl/ops 1 |
| + XXX b clki | — | X28 | X08 | ← – proc window 1 |
| + buffer rd | ← | X29 | X09 | → – proc busy |
| – time out | ← | X30 | X10 | → – XXX clock |
| + ground | — | X31 | X11 | ← – equipment check |
| – file window | → | X32 | X12 | → + dfhi sel |
| – XXX clock | ← | X33 | X13 | ← – proc window 2 |
| reserved | — | Y22 | Y02 | ← + burst reg bit 1 |
| reserved | — | Y23 | Y03 | → + cable continuity out |
| – proc lo int 15 | → | Y24 | Y04 | — + ground |
| – pty proc lo | ← | Y25 | Y05 | → – pty proc hi |
| – RWS hi int 7 | ← | Y26 | Y06 | → – RWS hi int 6 |
| – proc lo int 13 | → | Y27 | Y07 | ← + burst reg bit 2 |
| – RWS lo int 5 | ← | Y28 | Y08 | ← – reset |
| – RWS lo int 7 | ← | Y29 | Y09 | ← – proc lo int 14 |
| – RWS lo int 6 | ← | Y30 | Y10 | → – RWS hi int 5 |
| + ground | — | Y31 | Y11 | ← – proc hi int 7 |
| – proc hi int p0 | → | Y32 | Y12 | ← – proc hi int 6 |
| – proc hi int 5 | → | Y33 | Y13 | ← – proc lo int p1 |
| – proc hi int 3 | → | Z22 | Z02 | ← – proc lo int 11 |
| – proc lo int 10 | → | Z23 | Z03 | ← – proc hi int 4 |
| – proc lo int 9 | → | Z24 | Z04 | — + ground |
| – proc lo int 8 | → | Z25 | Z05 | → – RWS lo int 3 |
| – RWS hi int 4 | ← | Z26 | Z06 | → – RWS hi int 3 |
| – proc hi int 0 | → | Z27 | Z07 | → – RWS hi int 2 |
| + burst reg bit 4 | → | Z28 | Z08 | — reserved |
| – RWS hi int 1 | ← | Z29 | Z09 | → – RWS lo int 4 |
| – RWS hi int 0 | ← | Z30 | Z10 | → – RWS lo int 0 |
| + ground | — | Z31 | Z11 | → – RWS lo int 1 |
| – RWS lo int 2 | ← | Z32 | Z12 | ← – proc lo int 12 |
| – proc hi int 2 | → | Z33 | Z13 | ← – proc hi int 1 |

Top Card Connector
(Pin Side)




Each top card pin is connected to the corresponding pin on the other card.

Example:

FA1 W02 to FA2 W02
FA1 X22 to FA2 X22
FA1 Y33 to FA2 Y33
FA1 Z13 to FA2 Z13

## FA420 Adapter to Disk Drive Interface Description

### Control Bus (CC)

**Control Bus Bits 0–7 and Parity.** This section of the control bus is used to transfer data to and from the DSD. The decode of the three tag bits determines the significance and direction of data flow. Parity is checked by the DSD for incoming data and generated for outgoing data.

**Tag Bus Bits 0, 1, 2 and Parity.** The three tag bus bits are decoded to eight control lines as shown in the table below:

| Tag Bits | | | |
|---|---|---|---|
| 0 | 1 | 2 | Meaning |
| 0 | 0 | 0 | Interrupt Control |
| 0 | 0 | 1 | Head Selection |
| 0 | 1 | 0 | Track Selection |
| 0 | 1 | 1 | Diagnostic Wrap |
| 1 | 0 | 0 | Sense |
| 1 | 0 | 1 | Diagnostic Sense 1 |
| 1 | 1 | 0 | Diagnostic Sense 2 |
| 1 | 1 | 1 | Diagnostic Sense 3 |

**Tag 000 Interrupt Control.** The 000 and bit 1 on the bus suppresses the '-seek complete' interrupt. Tag 000, and not bit 1, resets the condition. Any suppressed interrupt will now become active.

**Tag 001 Head Selection (Seek Control).** Tag 001 gates control bus bits 5–0 to the head address register. Bit 7 is gated to the desired address register bit 256. Bit 6 is unused.

**Tag 010 Track Selection (Required Address).** Tag 010 gates the control bus bits 7–0 into the desired address register bits 1–128 respectively.

**Tag 011 Diagnostic Wrap Back.** Tag 011 gates the low order bits (1–128) of the desired address register, back to the control bus for wrap around transmission back to the using system.

**Tags 100, 101, 110 and 111.** These tags gate sense and status information onto the control bus. For details of sense and status lines, see FA233.

**'– Control Sample Received'.** This line is activated by the DSD after it reads the tag lines and, if necessary, the control lines following a 'control sample' signal from the system controller.

### Dedicated Cable (DD)

**'– Control Sample' (Input to DSD from System).** The control bus is looped through up to four DSDs and the information carried is available to them all. '– Control sample' can only be active on one DSD at any time and is ANDed with the 001 or 010 tag decbdes to gate head or track selection into the correct DSD.

'– Control sample' also generates '+ enable bus' for any tag other than 001 or 010 which gates sense and status to the control bus.

**'+ Interface Driver Degate'.** This line disables the control bus, control bus parity, and control sample received.

**'– Reset Error'.** This line is used to reset the 'data unsafe' or 'command error' sense bits. It may also be used to clear an interrupt.

**'– Write'.** This line activates the 'write' circuits in the DSD. It causes the 'write' current source to be turned on.

**'– Read'.** This line with 'data select' causes the data separator to decode data read from the disk, and present it on the 'NRZI' data line.

**Note:** *'– Write' and '– read' are mutually exclusive. An error interrupt occurs if they are both active at the same time.*

**'– Data Select'.** This is only active in one DSD at any time. It is used to gate '– write' or '– read'.

**'– Write Data'.** This is serial binary data for writing to the disk. '– Write data' is synchronized with '– write clock'.

**'– Fast Sync'.** This line must be activated to synchronize the data separator:

1. Before Reading ID
2. Before Reading Data
3. For Displaced Sector ID

### Output Lines from DSD to System

**'– 1F Write Clock'.** Synchronized to servo clock, pulses from the servo surface '– 1F write clock' are used by the using system to synchronize write data.

**'– Read Clock'.** Derived from raw 'read' data by the data separator.

**'+ NRZ Data' to System.** This line is the output from the data separator denoting 1's by an up level, and 0's by a down level.

**'– System Index'.** '– System Index' indicates the track start to the using system. It is derived from data in the dedicated servo area just prior to the start of the first sector on any track.

**'– System Sector'.** '– System Sector' is similar to '–system index' but indicates the start of all sectors after the first. It is derived from the dedicated servo area.

**'– Sector Pulses Missing'.** This indicates to the using system that the DSD failed to detect one or more sector or index pulses at the time that one was expected.

**'– Interrupt'.** An Interrupt is raised by any one of the following:

- Seek Incomplete
- Not Ready
- Data Unsafe
- Command Error
- Brake Applied
- Track Unavailable

**'+ Write Gate Return'.** This indicates to the using system that the write current has been switched on.

**'+ Dedicated Ready'.** This indicates to the system that the DSD is 'ready'.

**Individual Cabling Via Voltage Crossovers**

**'– Power Good'.** This is active only when all power lines are within tolerance. When inactive, it causes the DSD brake to be applied immediately.

**'+ Brake Applied'.** This indicates to the system that the brake has been applied either due to an unsafe or error condition, or due to brake failure. The system will respond by removing ac power from the motor within 5 seconds of '+ brake applied' becoming active.

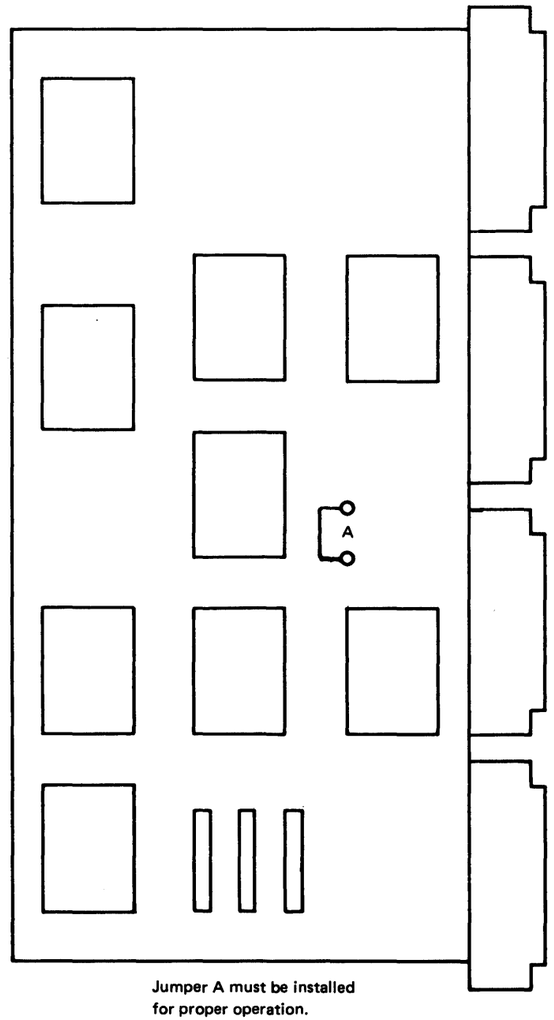
## FA430 Not Used

## FA440 Jumpers

### *FA441 Board Jumpers*

The only board jumper used is the file degate jumper from C–A1A5B12 to C–A1A5B13. This jumper must be installed for proper disk operation. However, the MD instructs you to remove it for certain tests.

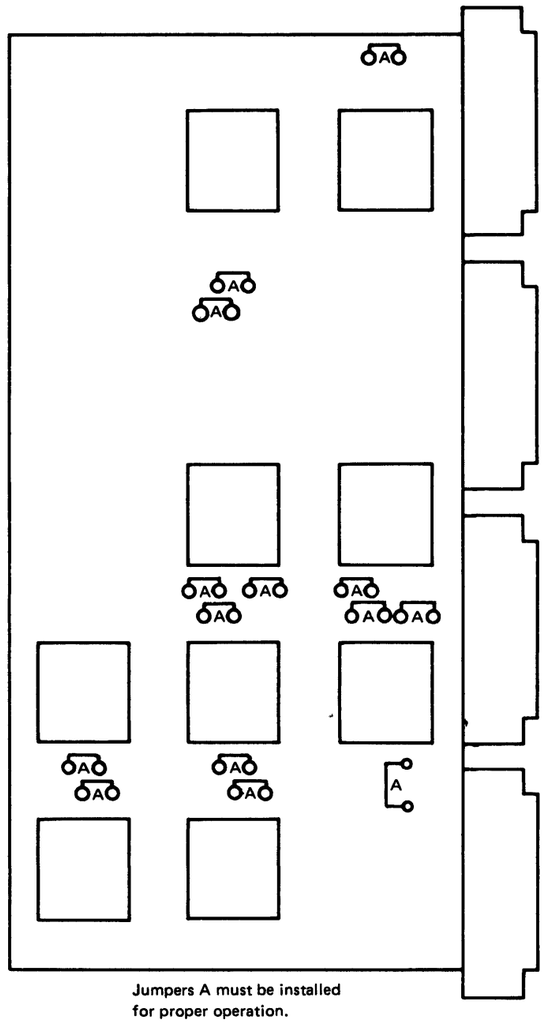
### *FA442 FA4 Logic Card 1 Jumper*




Jumper A must be installed for proper operation.

The FA4 Logic 1 card is located in 01X-A1C2.

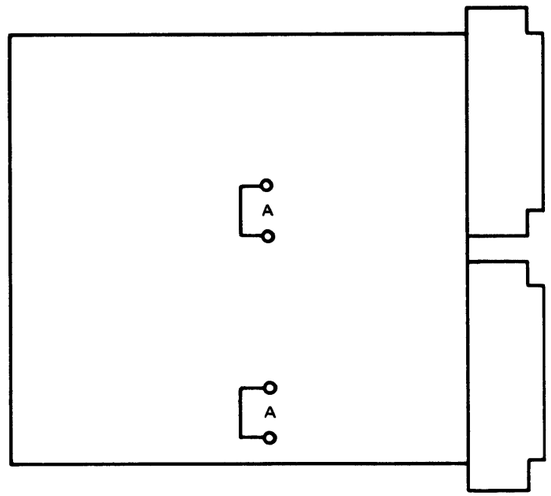
*FA443 FA5 Logic Card 2 Jumpers*




Jumpers A must be installed
for proper operation.

The FA5 Logic 2 card is located in 01X-A1D2.

*FA444 FA6 Servo Card 1 Jumpers*




Jumpers A must be installed
for proper operation.

The FA6 Servo 1 card is located in 01X-A1E2.

## *FA451 Data Flow Diagrams*

Figure FA451-1 shows the adapter data flow. Figures FA451-2, FA451-3, and FA451-4, respectively, show data flow for a seek operation, a read/write operation, and for error detection and safety circuits.

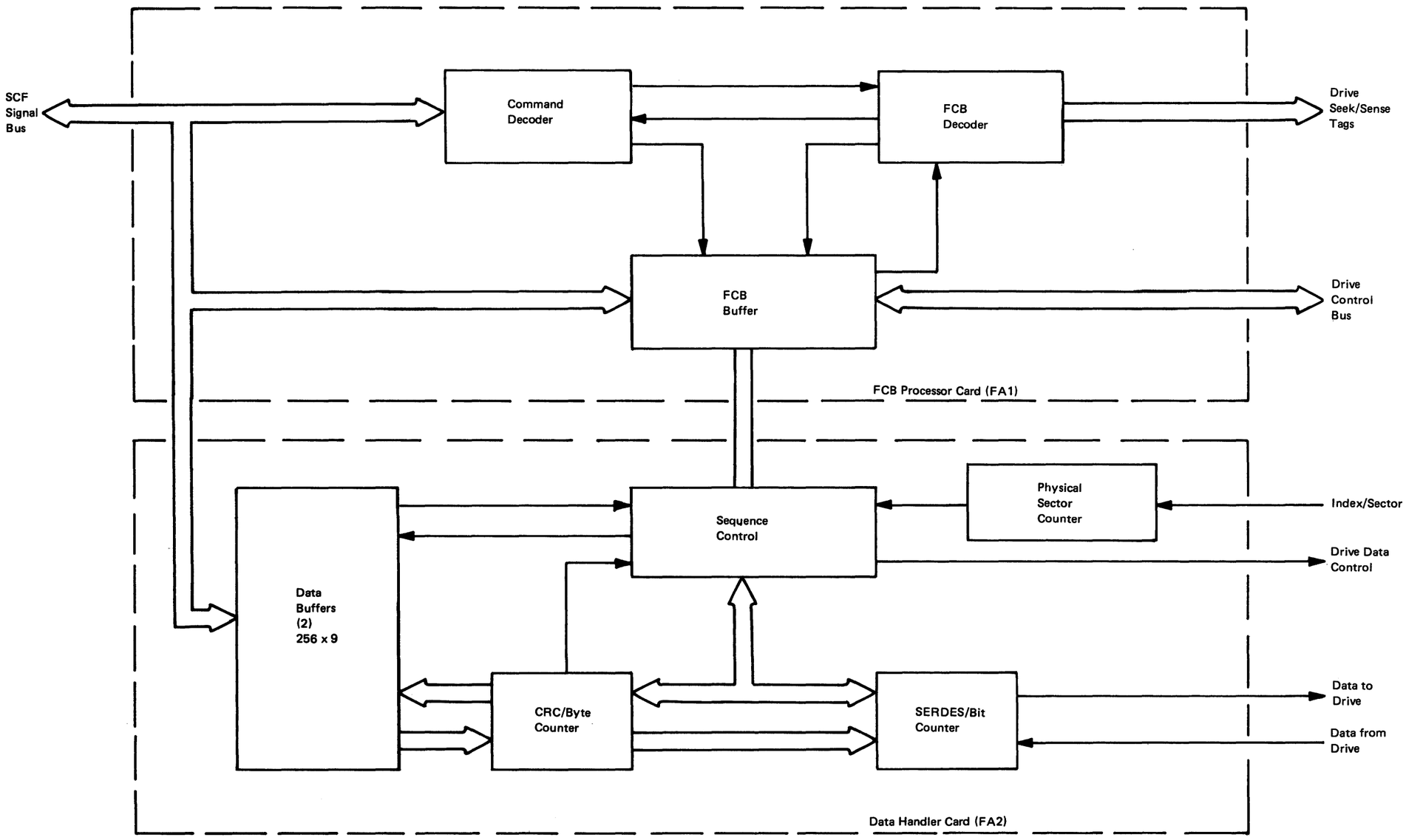



**Figure FA451-1. Adapter Data Flow Diagram**

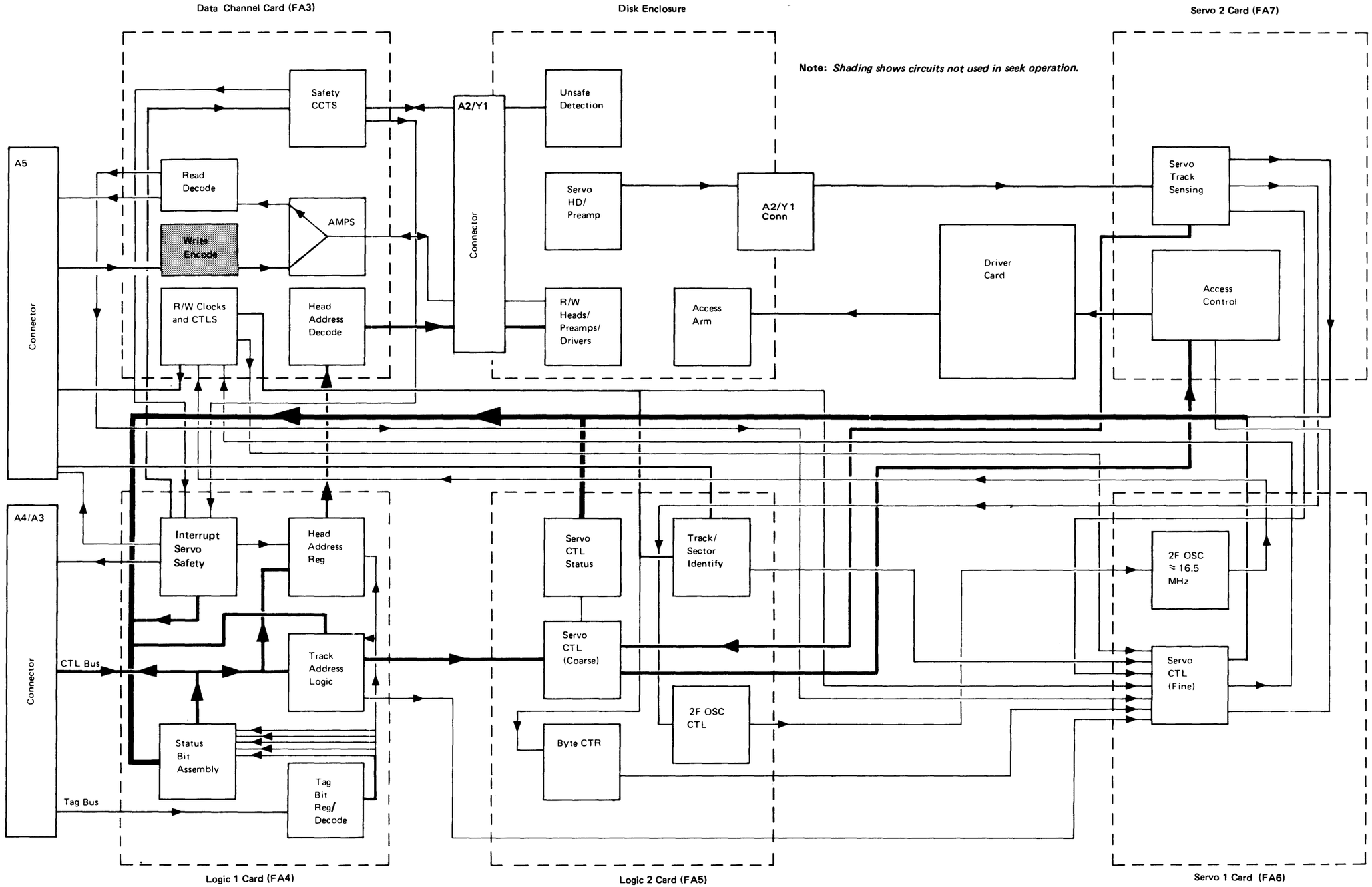



**Figure FA451-2. Data Flow Diagram, Seek Operation**

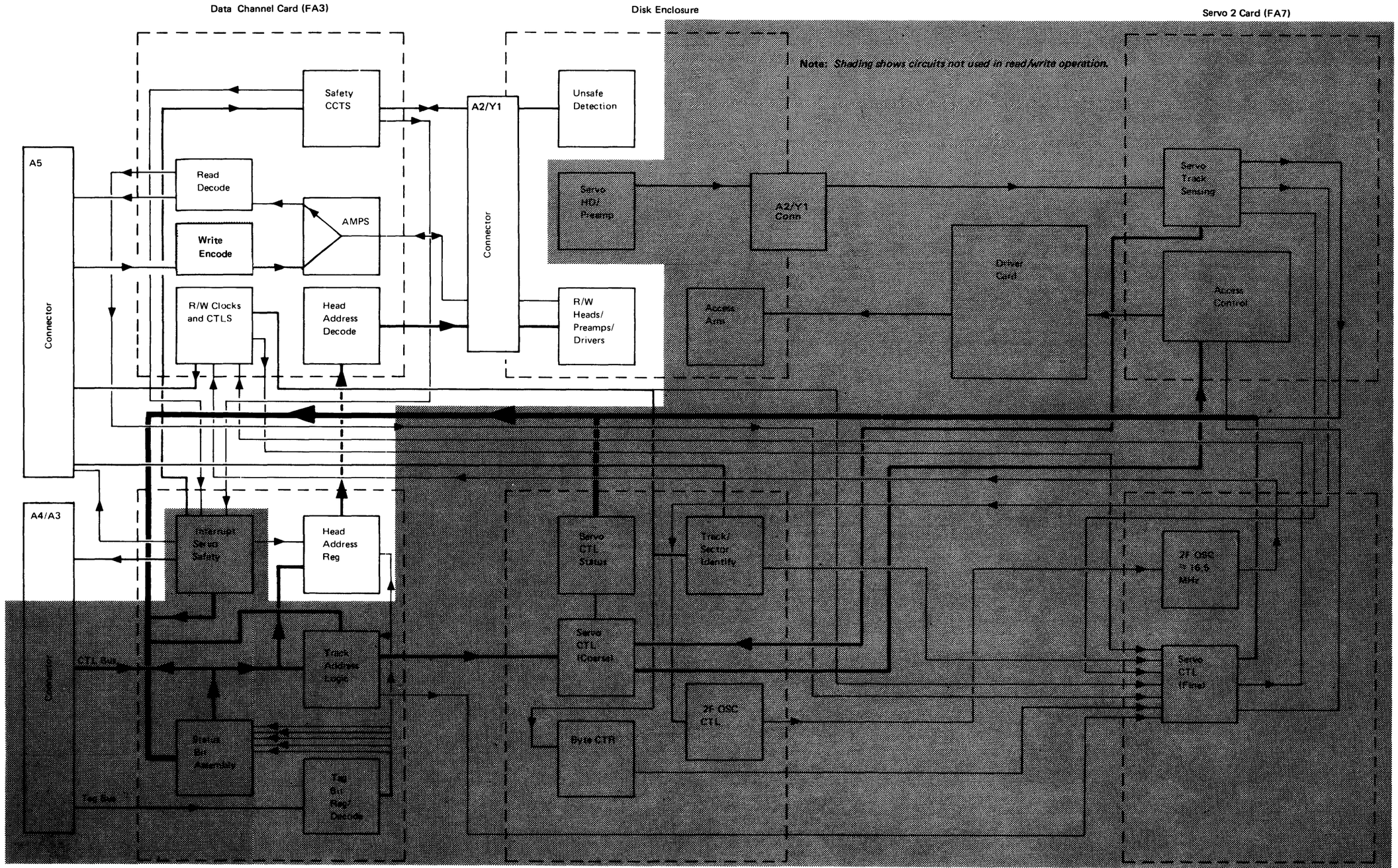



**Figure FA451-3. Data Flow Diagram, Read/Write Operation**

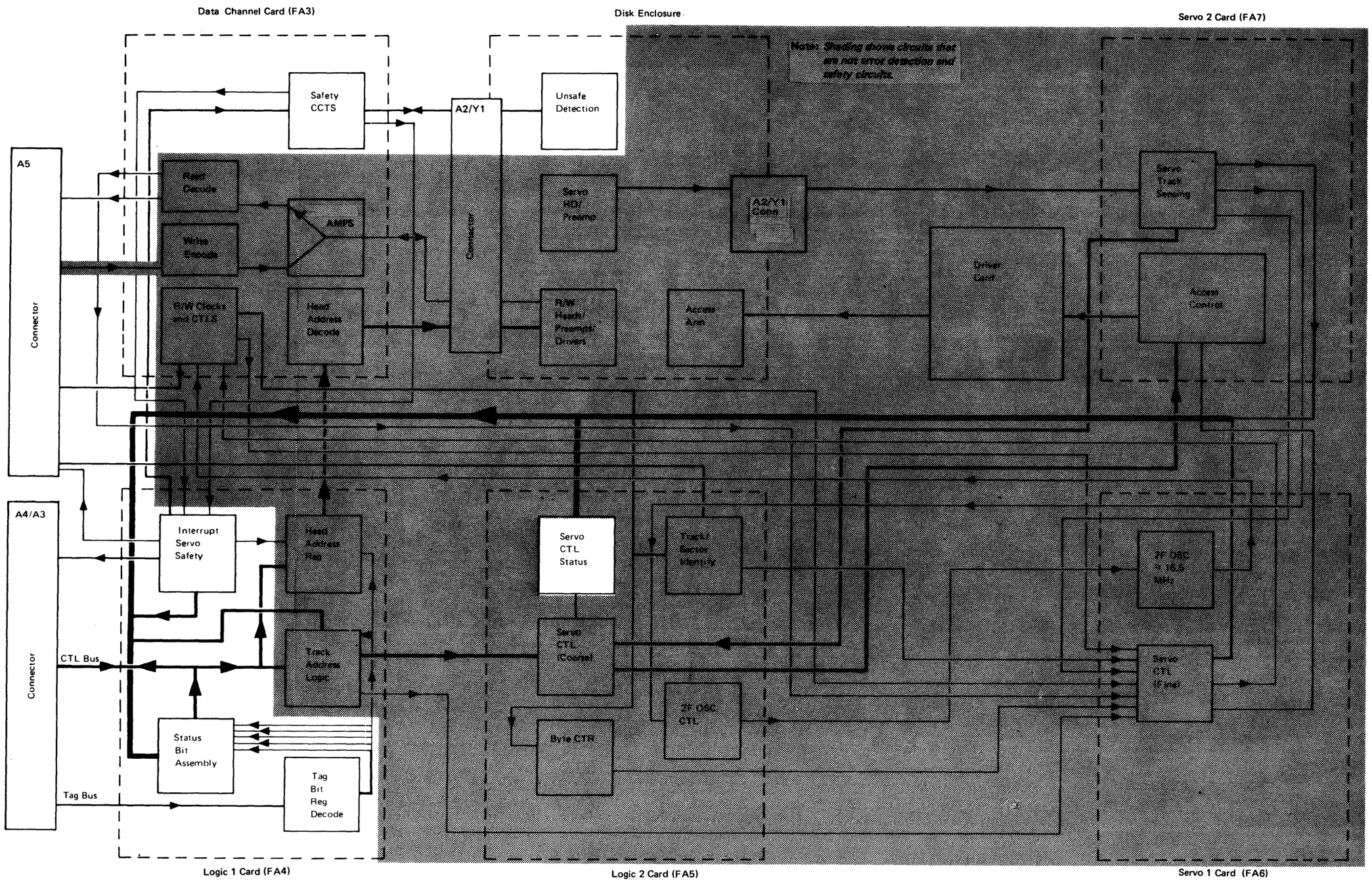



**Figure FA451-4. Data Flow Diagram, Error Detection and Safety Circuits**

**File Adapter**

**Function Definition Module (FDM).** System code builds Functional Control Blocks (FCBs), which are queues of functions to be executed by the adapter. System code then requests the FDM to execute the FCB. The FDM issues the appropriate commands to the adapter hardware to cause it to fetch the enqueued functions from the FCB. The adapter hardware makes the necessary data transfers and interrupts back to the FDM when all functions in the FCB have been executed.

**Function Control Block Processor Card (FA1).** The FA1 card communicates with the FDM through commands and status. It also fetches operations from the FCB, controls seeking and sensing of the drive, causes the data handler to initiate data transfer operations, and maintains adapter status.

When an operation is fetched from the FCB, the FA1 card decodes it and causes the necessary actions to occur to complete its execution. Once the action is initiated, the FA1 card may fetch the next FCB operation to allow overlapped operations (that is, fixed head data transfers and a moving head seek).

When the end of an FCB is reached or an error occurs, the FA1 card causes an interrupt back to the FDM.

**Data Handler Card (FA2).** When the FCB processor determines that data transfer to or from the drive is required, the FA2 card is activated. The FA2 card monitors the position of the head with respect to the disk. The Physical Sector Counter (PSC) in the FA2 card is able to predict the next physical sector on the track. The sequence control logic inspects the FCB operation and, at the correct sector count, verifies the ID (in the case of a read or write of a data field), and executes that read or write operation.

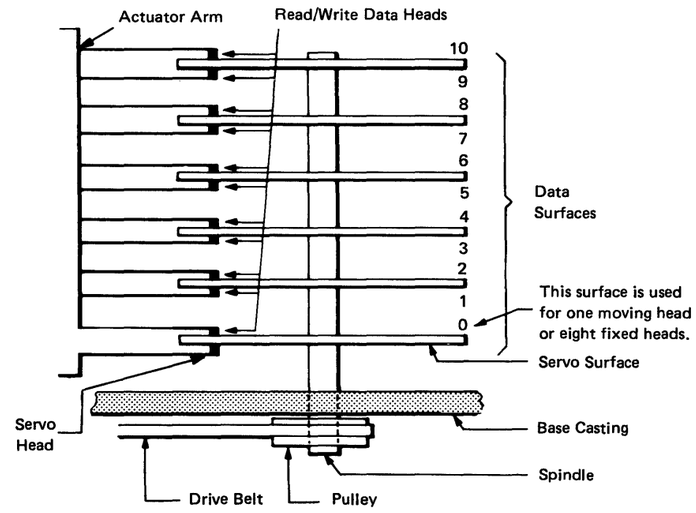
Two 256-byte data buffers reside in the FA2 card. While one buffer is receiving one data field from the drive (or processor), the other buffer may be transmitting to the processor (or drive). Within the FA2 card, Cyclic Redundancy Check (CRC) data is checked and generated and correct parity is maintained on the data.

When the transfer of one field is completed, the FA2 card requests the next function from the FCB processor. In this fashion, a read (or write) of all 64 data fields on a track may occur within one revolution.

**Disk Enclosure (DE)**

The DE is a sealed unit that contains the read/write components, actuator, spindle, and some of the DE electronics. This unit is available in 3- and 6-disk models as shown in Figure FA452-1. The DE drive motor, spindle brake, and the remainder of the electronics are attached to the DE base casting.

**Six-Disk Model**




**Three-Disk Model**

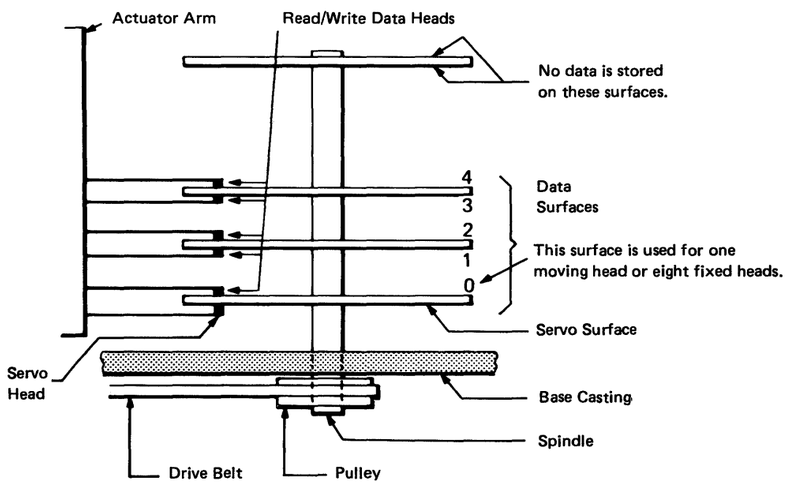



**Figure FA452-1. Disk Configurations**

**Spindle/Brake**

Depending on the type of DE, either three or six disks are clamped onto the spindle hub. A fourth (dummy) disk is fitted on the end of the three-disk spindle to assist the closed air circulation system.

The spindle is coupled to the drive motor by a belt that runs on the spindle and motor pulleys. If the DE is switched off or power fails, a mechanical drive brake operates against the spindle pulley to control deceleration of the disks. The brake also prevents disk rotation during transit.

The spindle and the conductive belt are grounded to the DE frame through antistatic brushes attached to the DE casting.

**Actuator**

The moving heads are attached to the end of each arm of a pivoted arm actuator. See Figure FA452-2.

Because the head-to-disk spacing is small, contamination prevention is important. Therefore, a closed-air circulation is used in which blades on the spindle hub continually circulate air through an absolute filter. A breather filter controls air pressure during startup, and ambient temperature changes.

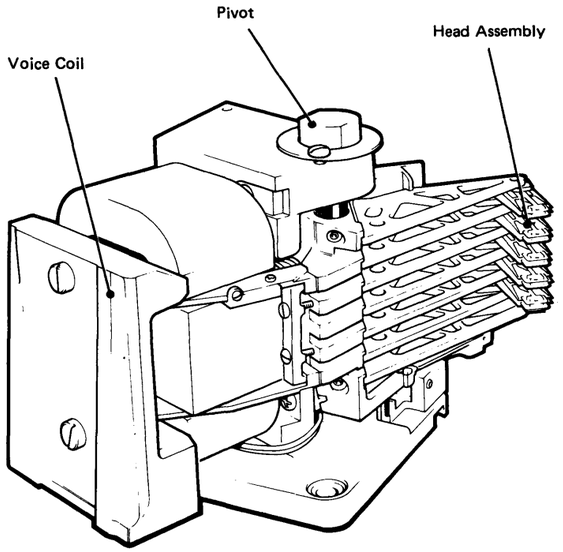



**Figure FA452-2. Actuator**

A rectangular coil is attached on the opposite side of the actuator pivot within a two-gap magnet, and current in the coil causes the heads to move in an arc across the disk surface.

Servo tracks on one disk surface are read continuously by the dedicated servo head and provide information to enable a closed loop servo system to be used for accessing.

Additional servo information is contained in each sector of the data tracks on all disk surfaces. This sampled servo information supplements the dedicated servo for fine control of the data head position when on track and during read or write operations.

Preamplifiers for servo and data heads and head section circuits are mounted on the actuator close to the heads, together with write driver circuits. During start and stop cycles, the actuator retracts the heads to the guard band area on the disk surfaces.

A retract spring pulls the heads to the landing zones if loss of disk speed occurs or if the actuator power supply fails. A magnetic catch on the actuator holds the heads over the landing zones in a normal power-off state.

A mechanical lock is provided for locking the actuator in the retracted position during removal and installation of the DE or transit of the DSD.

**Read/Write Components**

The disks rotate at a nominal 3125 revolutions per minute. A single head flies over each disk surface. To minimize wear of the disks and heads, the start and stop times are controlled by the drive motor and drive brake.

The disk surface nearest the base casting is dedicated to the servo head. The remaining surfaces each have a data head. Up to eight fixed heads can be fitted in place of the data head nearest the base casting. Each fixed head remains permanently over its own data track.

**Note:** *Fixed heads land on the data track and, for this reason, it is recommended that any permanent data be rewritten by the customer after a maximum of 20 power on/off cycles.*

**DSD Data Formatting**

The DSD format is written so that there are two data records of 256 bytes.

**Track Format.** The number of tracks on each disk data surface is 376. The band of 16 tracks closest to the disk spindle forms the guard band, which is behind home. The cylinder home is defined as cylinder zero, and the remaining cylinders are numbered from this cylinder outwards.

Sector boundaries are derived from information permanently encoded within the dedicated servo pattern under the zero head. These boundaries are defined by pulses on the dedicated sector line.

Each track is divided into 33 sectors (0–32) of 600 bytes. Sector 32 is reserved as an alternate sector to provide backup for defective disk areas. Cylinder 64 is also reserved for alternate sector usage, and cylinder 359 is reserved for maintenance test purposes.

**Data Surface.** Each data surface (Figure FA452-3) has 360 concentric data tracks, each of which has 32 sectors. A factory-written sample servo used for track following is contained in each sector. Each track has a reserved sector to which failed sectors are reassigned.

When this alternative sector has been used, further reassignment is to track 64, which has been reserved as an alternative track.

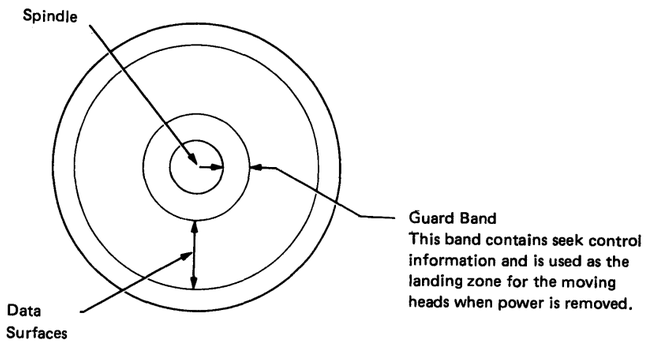



**Figure FA452-3. Data Surface**

**Servo Surface.** The servo surface (Figure FA452-4) is used for seek operations. It has 360 concentric tracks, with index and sector coding that corresponds to the data tracks on the other surfaces. The guard band has 16 tracks without encoding.

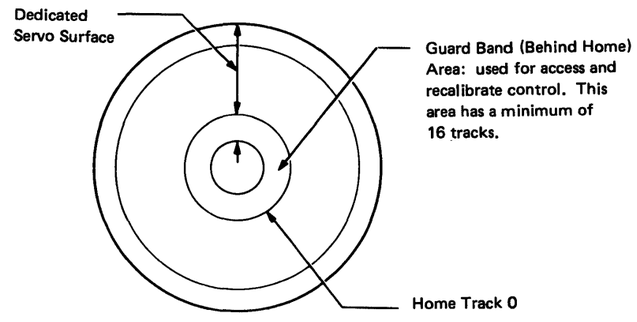



**Figure FA452-4. Servo Surface**

**Sector Format.** Each sector (see Figures FA452-5 and FA452-6) has a gross length of 600 bytes and is made up of three basic areas:

1. ID area, which contains flag byte, sector, head, track numbers, and cyclic check code.
2. Data area, which contains two 256-byte data fields.
3. Servo sample area, which is used by the DSD position servo to establish the data head position over the track. This area is not available and is interlocked to prevent accidental erasure or overwriting.

As shown in Figure FA452-6, a two-byte CRC field is provided for each of the 256-byte data fields, and a four-byte ECC field is provided for each of the 256-byte data fields.

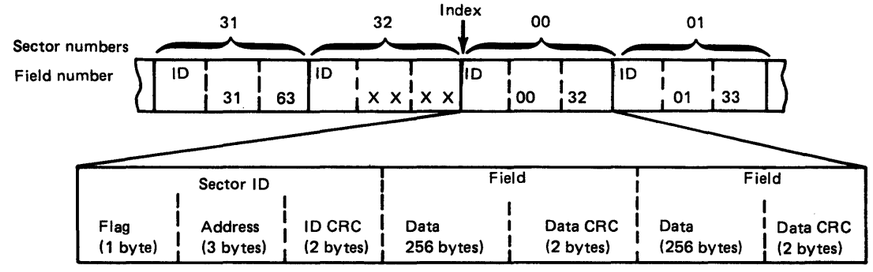
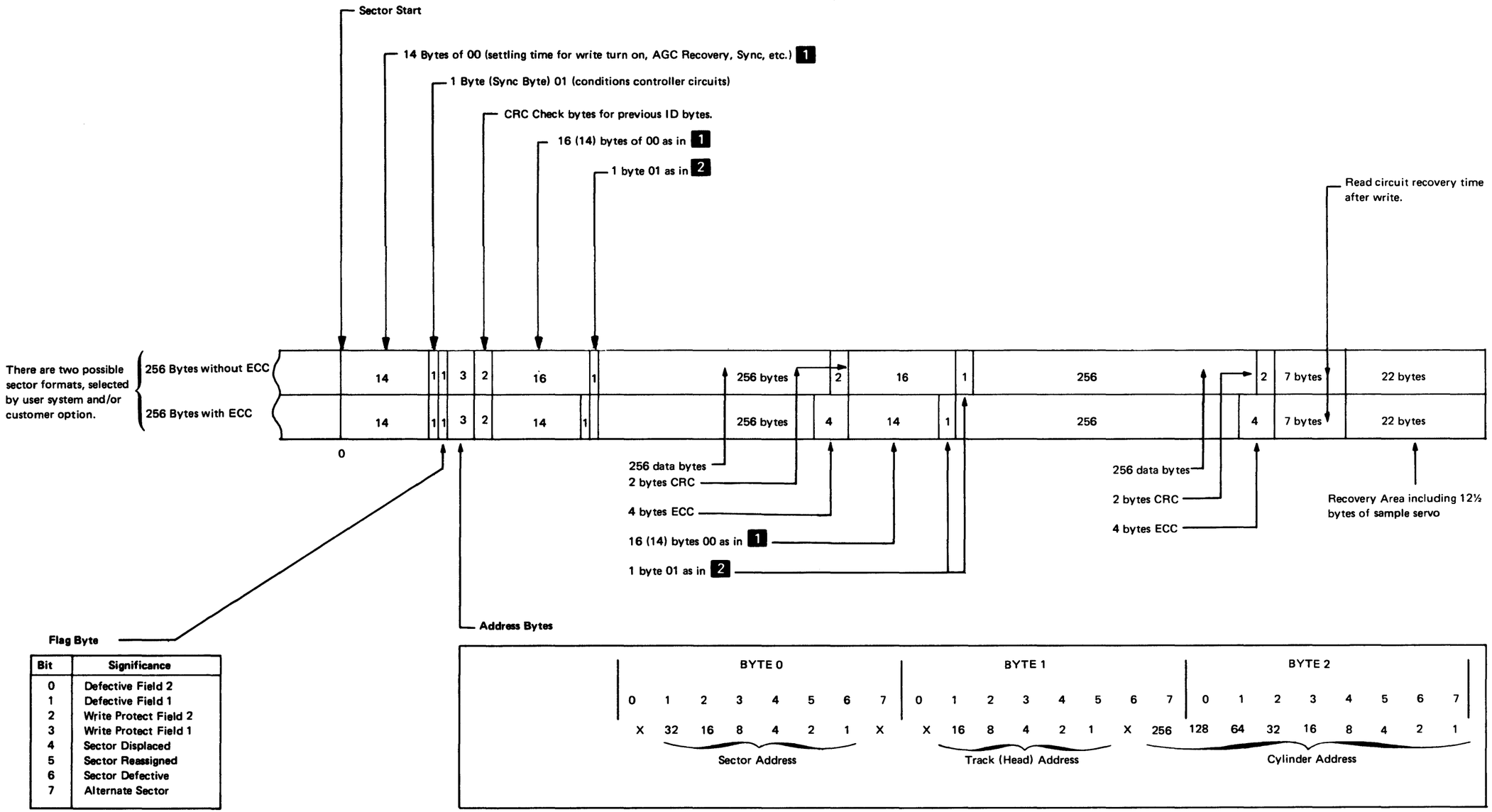



**Figure FA452-5. Sector Format**




| Bit | Significance |
|---|---|
| 0 | Defective Field 2 |
| 1 | Defective Field 1 |
| 2 | Write Protect Field 2 |
| 3 | Write Protect Field 1 |
| 4 | Sector Displaced |
| 5 | Sector Reassigned |
| 6 | Sector Defective |
| 7 | Alternate Sector |

**Figure FA452-6. Sector Organization**

**Spiraling.** Large volumes of data are sometimes required to be read or written on sequential sectors and tracks. In these cases, after all remaining sectors on the first track have been written, the next sequential head is selected and writing continues on the next track. A maximum of eight sectors is required for the read/write circuit to stabilize after a head change; therefore to ensure that data transfer can continue with the minimum interruption, sector addresses on each succeeding track are displaced by eight sectors (see Figure FA452-7). This avoids the requirement to wait for a full disk rotation before restarting the read or write operation. Fixed heads do not follow this principle as they are not intended for use with bulk data.

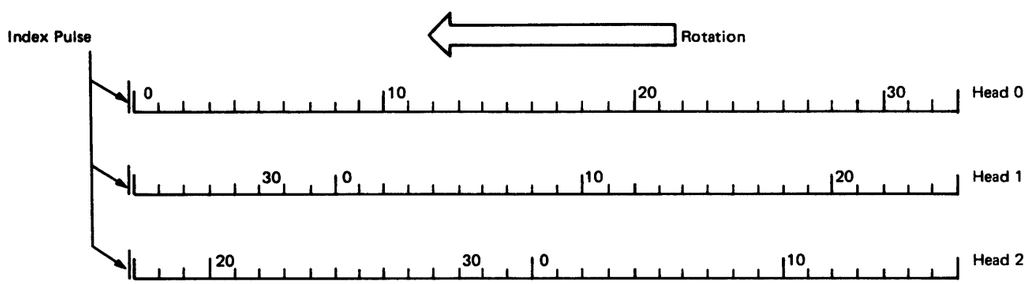



**Figure FA452-7. Spiraling**

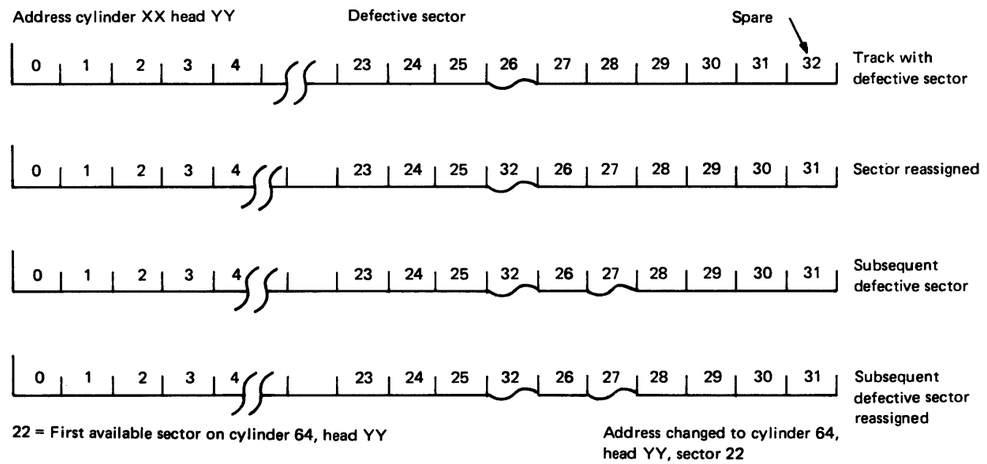



**Figure FA452-8. Example of Defective Sector Reassignment**

**Flag Byte.** Bits 4 through 7 have been described previously under Defective Sector Handling. Bits 0 and 1 (Defective Fields 2 and 1) indicate the location of a defect to the first or second data field in 256-byte mode. Bits 2 and 3 (Write Protect Fields 2 and 1) directly identify sectors that contain protected data which must not be overwritten.



**Defective Sector Handling.** Occasionally, defects in the disk surface will cause a sector to be unusable for normal operations. These surface defects may occur at any time, although originally they are detected and flagged during the manufacturing process.

Section 32 on each track is reserved as an alternate for the first defective sector on that track. In addition, cylinder 64 is reserved as an alternate for any subsequent sector failures.

When the first defective sector is identified, the sector number in the address bytes is changed to 32 and the flag byte 6 is set. All subsequent sectors will be reassigned so that the defective sector will now occupy the space currently occupied by the next sequential sector, and sector 32 will be occupied by sector 31. All sectors that have been moved in this way have bit 4 set in the flag byte (Sector Displaced) and the sector address changed to show the new sector assignment.

Any subsequent defect on the same track will have bits 6, 5, and 4 set in the flag byte (Sector Defective, Reassigned, and Displaced respectively). Its address also is exchanged with that of the first available sector on cylinder 64 using the same head (see Figure FA452-8).

If the defect on any sector prevents reading of the ID field, then the whole ID field is rewritten 64 bytes later on the sector. If this area is also defective, then provision is made for the ID field to be written 256 bytes later instead. Bits 5 and 7 are set in the flag byte (Sector Reassigned and Alternate Sector).

**Access Positioning.** A dedicated servo surface and read head control the primary access positioning and locate the access mechanism over a selected data cylinder. However, with dense packing of data tracks on each surface, any minor misalignment between data heads and data track cannot be tolerated.

Final access positioning, therefore, is controlled by short bursts of servo information written at the start of each sector. The servo head may therefore be marginally off track, but the data head is correctly aligned at all times.

The sample servo error signal is reset to zero at the end of each sector, and is set by the sample servo electronics to its required level every time a sector or index area passes under the selected read head.

**Dedicated Servo.** A seek operation is initiated by two commands on the logic card control bus. The adapter places the binary equivalent of the low-order eight bits of the desired address on the control bus, and encodes a tag of 010 to the tag bus.

After permitting the two buses to stabilize, the adapter activates the control sample, which permits the tag bus register to accept the tag code. The tag code is decoded and gates the control bus to the desired address register, bits 1–128. The high-order bit (256) of the address is provided in a similar manner by a tag decode of 001; this gates the head address data to the head address register.

The desired address is compared with the current address position, stored in the absolute address accumulator by the subtractor. At the same time, the decode verifies the validity of the address required and raises track unavailable if the track requested is outside the usable track address. Track unavailable is combined with parity error to inhibit set seek, thereby preventing an attempt to seek under error conditions.

The desired and absolute addresses are compared in the subtractor. The lower of the two addresses is subtracted from the higher, and the difference count obtained. The count is equivalent to the number of tracks that have to be crossed for the access arm to arrive at the desired address.

Any output from the subtractor other than all zeros activates shift. This indicates to the access logic that the heads are not positioned at the required track.

Internal carry lines in the subtractor determine the direction of subtraction. If the absolute address is higher than the desired address, the subtraction is absolute address minus the desired address. The -carry 256 signal from the subtractor controls the direction of access motion.

To obtain the fastest possible movement of the access arm, the voice coil motor is driven at its maximum possible acceleration for as long as possible, then decelerated quickly to a stop immediately over the desired track without overshooting or undershooting. Because each successive access move can vary in length from 1 to 359 tracks, a very sophisticated servo control system is necessary.

For any access length, the actuator is driven at maximum acceleration until its velocity exceeds the velocity profile. From that point until the completion of the access, the actuator velocity is controlled to follow the profile. The velocity profile is stored as 512 words in a read-only storage (ROS) module.

At all times during the course of an access, the DSD calculates the distance of the actuator from the desired track by taking the difference between the absolute track address and the desired track address. This difference is updated at 1/4 track intervals and used to address the ROS. On long accesses, when the difference exceeds 512 quarter tracks (that is, 128 tracks), the ROS address is forced to 511.

The ROS output feeds a digital-to-analog converter so that, as the difference count decrements from 127 to 0, a graduated output is produced that corresponds to the desired velocity profile. To compensate for mechanical and electrical tolerances, and for drift caused by environmental conditions, the graduated output of the access velocity generator is variable and controlled by the profile gain voltage.

Profile gain voltage is generated all the time that power is available to the DSD. The maximum access performance of the DSD is obtained by calibrating the profile gain voltage using the following sequence:

1. Recalibrate — This causes the DSD to access to the home position with head 1 selected.
2. Seek to track 128 with head 1 selected — During this 128-track seek, the velocity profile is compared with the true velocity of the access arm.

The counter increments until the velocity is not greater than profile or until the counter is full.

A compensation coil in the DE minimizes drift caused by temperature variations. The compensation coil is made of the same material as the voice coil motor windings. Therefore, any resistance changes in the compensation coil mirror those of the voice coil and provide corresponding compensation to the analog circuits.

One further offset to the desired velocity is provided by the handover velocity. The handover velocity is recalibrated automatically after a calibrate operation, and sets the slow seek timing for the last 1/4 track of a seek operation.

The access arm is forced to seek in two-track increments. The time taken is compared in a slope detector block against a reference voltage. If the time is less than 1.9 ms, the counter, previously preset to 7, is decremented, and the cycle repeated until the time is equal to or greater than 1.9 ms, or until the counter has reached 0.

When the access arm has reached the desired address, + seek is deactivated and, after a suitable delay, seek complete is activated. This raises an interrupt that signals to the adapter that the operation is completed.

**Read/Write**

A prerequisite for any read/write operation is that one, and only one, read/write head must be selected.

Control bus bits 1 through 5 are gated into the head address register by a tag decode of 001. These five lines are then converted to five module-select lines by the head-select decode logic. Module-select lines 1 through 3 are routed directly to the DE logic circuits through the (MH) cable.

**Note:** *The DE contains up to five modules each capable of driving up to four heads.*

When a module select line is activated, the positive supply is gated to the appropriate module. Decoding the head select pair then gates the selected head.

Each module contains the following: four write drives, four read preamplifiers, a common read output amplifier, head selection logic, read/write selection logic, and safety circuits.

The DE does not reject invalid codes. However, the safety circuits indicate an error condition if a write operation is attempted on an invalid head.

The read/write heads are center-tapped, and the center tap lines are connected together. A read or write operation is controlled by the center tap of the selected head. A plus level on the center tap line provides the current for writing; a zero level provides the necessary grounding for a differential output while reading.

Read and write signals pass to and from the module through the actuator I/O lines (or fixed-head I/O lines on a fixed head DE).

**Write Data.** Write data from the dedicated cable enters a four-bit shift register and is clocked through the shift register by a clock pulse derived from the write clock. The four bits of the shift register are fed to a precompensation encoder where the bit pattern is encoded to become a modified frequency modulation (MFM) signal that, after feeding through the signal bus amplifier modules, is passed to the moving and fixed heads for writing by the selected head.

Precompensation in the encoder is a technique used to counteract timing errors that occur in the read signal caused by the high density of data on the disk surface. In principle, as the data flows through the shift register, bit 3 of the shift register is the bit being wrritten, bit 4 is the bit that was written previously, and bits 1 and 2 are yet to be written. The timing logic supplies the encoder with three clock lines at 2F frequency, 2F early, 2F on-time, and 2F late; early and late are approximately ± 9 ns from the on-time signal.

The encoder examines the four bits in the shift register and, from the 16 possible bit combinations, decides whether bit 3 should be written on the disk on time, late, or early and uses one of the three 2F clocks to achieve this. Write data is also fed to the head circuits during a write operation for test purposes.

**Read Data.** Any time that a head is selected and not writing, it is reading data from the disk. Read data is amplified within the DE and passed by the actuator I/O line to the signal bus amplifier for further amplification. Two outputs are available from this stage: the first provides sample servo input; the second is amplified again by a variable gain stage that provides a differential output at a constant level, regardless of the input variations.

Figure FA452-9 shows the expected output at this point D13 or B13. Synchronization is provided by the system sector line. The figure shows a full scan across one sector using a delayed 10:1 sweep on a time base of 0.2 ms/division.

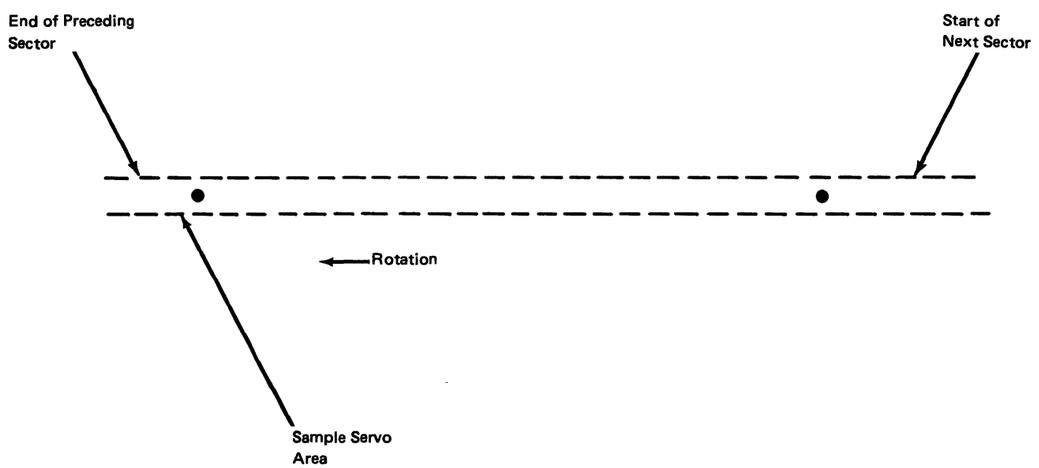



**Figure FA452-9. Sector Scan**

The data -V detector extracts timing information from the differential output of the amplifier by detecting the signal peaks. Each peak produces a pulse output that is fed to the voltage controlled oscillator (VCO) sync control logic. VCO sync logic controls the following operations:

1. The VCO is synchronized with the incoming data stream in frequency and phase. The phase discriminator detects differences in phase between the oscillator and the data stream, and raises or lowers the control voltage to the oscillator, through the charge pump, to keep them in step. The servo inhibit VCO line stops the oscillator during the sample servo area. Rapid changes in operation cause the VCO to go out of sync; the controller, therefore, issues a fast sync command when changing from write to read, for example.
2. Fast sync momentarily stops the oscillator and restarts it in proper synchronism with the data stream so that control can be rapidly resumed.
3. The VCO output is used by the data separation circuits (MFM decoder and NRZ data generator) to time the extraction of data from the data stream. NRZ data is applied to the controller in the using system in serial mode together with a read clock to drive the deserializer.

**Error Detection and Safety Circuits.** Comprehensive error detection is provided by the DSD, and write operations are immediately inhibited if any unsafe condition is detected while writing. Recovery actions, however, must be handled by the adapter.

Thirty-two status and sense conditions are available to the 8100 system, in groups of eight. By selecting the appropriate tag (100, 101, 110, or 111), the 8100 system can gate the selected group in the control bus out register.

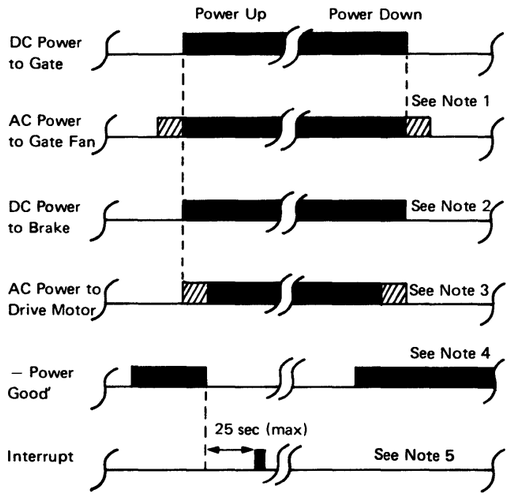
Provided that the degate bus and power-on delayed are not active, the contents of the register will be gated to the control bus.

**Sense Cycle.** Certain conditions will cause an interrupt to be raised. This interrupt may result from (1) the normal completion of an access, head select, recalibrate, or power-up sequence, or (2) alternatively, as a result of DSD error condiitions such as not ready, data unsafe, command error, track unavailable, or brake applied.

The issue of an interrupt by the DSD is serviced by a control bus sense cycle with tag code 100. Further sense cycles may then be initiated with tag codes 101, 110, and 111 to provide further sense information if the tag 100 sense indicated an error condition.

**Power Sequencing**

The 8130/8140 Processor or the 8101 Storage and I/O Unit supplies and sequences the ac and dc power to the DSD. The basic sequence in Figure FA452–10 applies.




**Notes:**

1. *The ac power to the gate cooling fan must be on any time that dc power is supplied to the logic cards to prevent overheating of the electronic components.*
2. *The brake is retracted when dc power is applied and – power good is at dc-ground level. This should occur within ±500 ms of ac power being applied to the drive motor.*

   *If brake failure occurs, that is, the brake is released, ac power is removed from the motor within 5 seconds (maximum) by the 8130/8140 Processor or by the 8101 Storage and I/O Unit.*
3. *The ac power is not applied to the drive motor unless dc power to the gate is on and within tolerance.*
4. *– Power good is applied to the DSD (VC-1) and indicates that the dc voltages are within tolerance at the user system, and that ac power is applied to the DSD drive motor. When power good goes active (that is, to ground level), it provides the dc ground for the brake electromagnet.*

   *Power good must be active within ±500 ms of ac power being applied to the drive motor.*
5. *The DSD issues an interrupt within 25 seconds of power good being active. Power good is filtered by the DSD and used to hold the DSD reset for 17 seconds by – POD. At the end of the 17-second delay, the DSD effects a calibrate operation and raises the interrupt.*

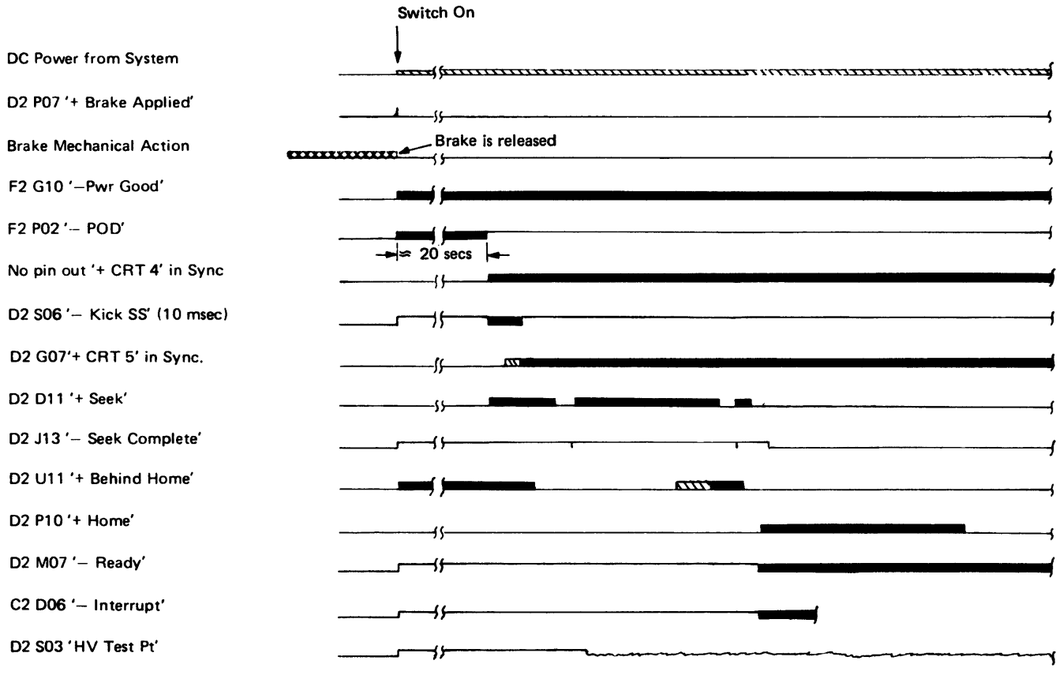
**Figure FA452-10. Power Sequencing**

**Power-On Logic Sequence (Figure FA452-11)**

1. The ac and dc power are applied to the DSD.
2. Brake applied remains essentially negative to provide a return path for brake current which retracts the brake and permits the spindle to accelerate.
3. –Power good is raised by the processor when dc voltages are within tolerance.
4. –POD becomes active for approximately 20 seconds to permit the disk speed to stabilize at 3125 rpm.
5. CTR 4 comes into synchronization after –POD times out and triggers the kick SS. If CTR 4 fails to come into sync before –POD and PLO holdover SS times out, brake applied will be raised, the brake will activate, and brake applied to the adapter will be raised. The ac and dc power will then be switched off within 5 seconds.
6. –Kick SS applies maximum acceleration to the actuator arm for 10 ms to move the actuator arm into the data area.
7. During the initial access movement, CTR 5 comes into synchronization.
8. + Seek is raised with the kick SS cycle and is lowered when the actuator comes to rest.
9. –Seek complete initiates a recalibrate cycle.
10. At the completion of the recalibrate cycle, home and ready become active and an interrupt is raised.
11. During this recalibrate cycle, handover velocity (HV) is calibrated. This is an analog voltage that should set to a similar level each time the DSD is powered up.

**Power Down.** When the DSD is powered down normally, through software or an emergency, the moving heads are moved to the landing zone of the disks, and the motor brake is applied when its +24V holdoff voltage is removed.

If a dc supply goes outside the specified limits, all ac and dc voltages are removed within 5 seconds. This reduces the risk of possible loss of data.




**Note:** *This chart indicates the correct sequence of events. Actual times and wave forms will vary.*

**Figure FA452-11. Power-On Logic Sequence Timing**

**Power Interlocks.** Power-failure detection is not provided by the DSD. However, failing conditions are indicated to the system.

**Not-Ready Condition.** A not-ready signal is issued and an interrupt is raised when:

- The Phase Lock Oscillator (PLO) loses synchronization. This can be due to loss of disk speed that can occur if the drive motor fails, ac power removed from the motor, or the brake fails.
- The brake applied line is active due to failure of the brake drive. The line is reset when the power-down sequence of the 8130/8140 Processor or the 8101 Storage and I/O Unit is complete.
- The invalid move line is active. This line is actuated either when actuator motion is not in response to an access command, or when writing is attempted during an access operation.

Recalibrate (see Figure FA452-15) resets not ready except when brake applied is active or when a power-down sequence is required. If recalibrate is not successful, reset error completes the recovery process.

**Thermal Failure.** A thermal cutout detects overheating in the drive motor. If the cutout operates, it can be reset manually only after the motor has cooled to within safe limits. After a thermal cutout trips, the PLO will go out of synchronization, thus activating brake-applied and initiating a power-off sequence in the 8130/8140 or the 8101.

## Signal Bus Descriptions

### Control Cable (CC)

Control Cable Bits 0-7 and Parity. This section of the control cable is used to transfer data to and from the DSD. The decode of the three tag bits determines the significance and direction of data flow. Parity is checked by the DSD for incoming data and generated for outgoing data.

Tag Bus Bits 0, 1, 2 and Parity. The three tag bus bits are decoded to seven conrol lines as shown in the following table:

| Tag Bits | | | |
|---|---|---|---|
| 0 | 1 | 2 | Meaning |
| 0 | 0 | 0 | Not Used |
| 0 | 0 | 1 | Head Selection |
| 0 | 1 | 0 | Track Selection |
| 0 | 1 | 1 | Test Wrap |
| 1 | 0 | 0 | Sense |
| 1 | 0 | 1 | Test Sense 1 |
| 1 | 1 | 0 | Test Sense 2 |
| 1 | 1 | 1 | Test Sense 3 |

Tag 001 Head Selection. Tag 001 gates control bus bits 5—0 to the head address register. Bit 7 is gated to the desired address register bit 256. Bit 6 is unused.

Tag 010 Track Selection. Tag 010 gates the control bus bits 7—0 into the desired address register bit 1—128 respectively.

Tag 011 Test Wrap. Tag 011 gates the low order bits (1—128) of the desired address register, back to the controll bus for wrap around transmission back to the adapter.

Tags 100, 101, 110 and 111. These tags gate sense and status information onto the control bus.

—Control Sample Received. This indicates to the adapter that control sample has been received and responded to.

**Dedicated Cable (DD)**

–Control Sample (input to DSD from the adapter). –Control sample and the 001 tags decode gate head or track selection. –Control sample also generates +enable bus for any tag other than 001 or 010 which gates sense and status to the control bus.

+Degate Bus. This line is normally held negative. When activated, it prevents sense and status information from being gated to the control bus.

–Reset Error. This line is used to reset the data unsafe or command error sense bits. It may also be used to clear an interrupt.

–Write. This line activates the write circuits in the DSD.

–Read. This line activates the read circuits in the DSD.

**Note:** *–Write and –read are mutually exclusive. An error interrupt occurs if they are both active at the same time.*

–Data Select. Data Select is used to gate –write or –read.

–Write Data. This is serial binary data for writing to the disk. –Write data is synchronized with –write clock.

–Fast Sync. This rapidly forces the read PLO into synchronization after any event that requires a long resync, using normal sync control. For example, after change from write to read.

**Output Lines from DSD to the Adapter**

–1F Write Clock. Synchronized to servo clock, pulses from the servo surface –1F write clock are used by the adapter to synchronize write data.

–Read Clock. Synchronized to data during read operations, –read clock is used by the adapter to clock read data into the deserializer.

+NRZ Data to the Adapter. Serial data read from the disks.

–System Index. –System index indicates the track start to the adapter. It is derived from data in the sample servo area just prior to start of first sector on any track.

–System Sector. –System sector is similar to –system index but indicates the start of all sectors after the first.

–Sector Pulses Missing. This indicates to the controller that the DSD failed to detect a sector pulse at the time one was expected.

–Interrupt. An interrupt is generated for home and ready, after power up, for seek complete and some error conditions.

±Write Gate Return. This indicates to the controller that the write current to the DSD has been switched on.

**Individual Cabling Through Voltage Crossovers**

–Power Good. This is active only when all dc power lines are within tolerance at the 8130/8140 or the 8101. Its loss causes the DSD brake to be applied immediately.

+Brake Applied. This indicates to the controller that the brake has been applied, either because of an unsafe or error condition or brake failure. The 8130/8140 or the 8101 will respond by removing ac power from the motor within 5 seconds of + brake applied becoming active.

**Phase-Locked Oscillator (PLO) Loop**

The PLO (Figure FA452–12) is synchronized in phase and frequency by the servo signal clock pulses as follows:

The voltage-controlled oscillator (VCO) runs at approximately 16.5 MHz. The output 2F is divided by 2 to give 1F write clock.

The 1F write clock drives a 5-bit counter (counter 4) whose output is 1/16th of the PLO frequency. The servo clock pulses trigger a single shot (+ servo clock SS – 280 ns).

For the PLO to be in synchronization, the trailing edge of the servo clock SS must coincide with the midpoint of the negative level of the counter 4 signal.

A comparative circuit on the Logic 2 card looks for this coincidence and provides an output of oscillator early or late to the VCO to correct any misalignment.

During normal synchronous operation, narrow oscillator late and oscillator early signals are produced continuously as shown in Figure FA452-13.

The PLO is used by the processor to serialize write data.

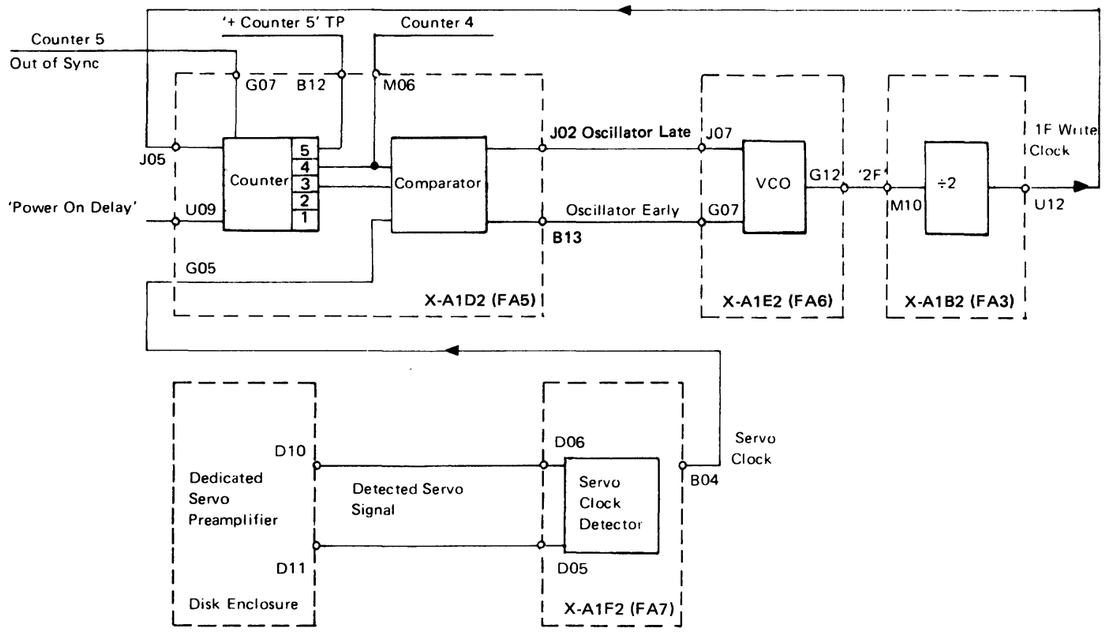



**Figure FA452-12. PLO Data Flow**

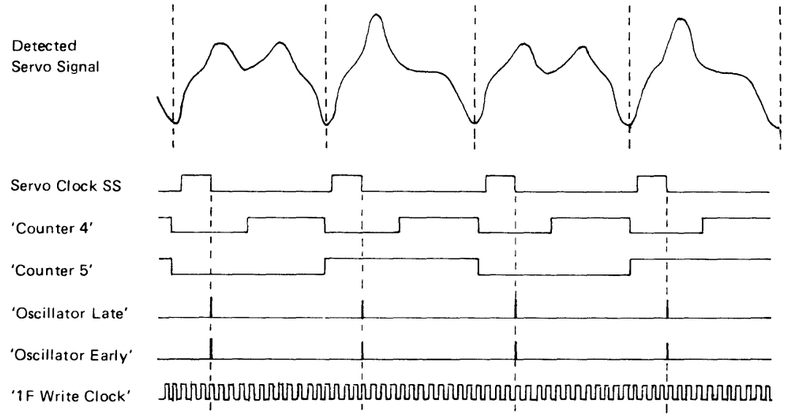



**Figure FA452-13. PLO Timing**

### Voltage Controller Oscillator (VCO) Control

The VCO and associated control circuit (Figure FA452-14) form a phase-locked loop that tracks the frequency and average phase of the read input data signal, and corrects for any drift in these signal components.

**Circuit Operation.** The 2F clock applied to the data latch is compared with the data SS (single shot) for coincidence. If the data SS pulse is completed before the end of the corresponding data latch pulse, an increase line is activated. If the data SS pulse is completed after the end of the corresponding data latch pulse, a decrease line is activated. The combined output (an analog control voltage) is applied to the VCO to restore the correct coincidence of the data latch pulses with the data SS pulse.

Relatively large discontinuities of the data signal can cause loss of synchronization of the data latch and data SS signals. Therefore, when the source of the data signal changes, for example when changing from writing to reading, the VCO control circuit is switched momentarily to the fast synchronization state.

During fast synchronization, the VCO operates as previously described, except that the signals involved are much greater.

The fast sync signal applied to the fast sync logic can be in one of two phases, depending on the mode (read or write) in which the DSD is operating. The fast sync logic selects the appropriate fast sync input, that is, fast sync from the processor or internal fast sync.

The circuit is reset by the end of the inhibit SS pulse and the data pulses; the VCO is then restarted so that the data pulses and the VCO output are synchronized.

When the DSD is not under the control of the disk adapter, the VCO is synchronized with the write clock.

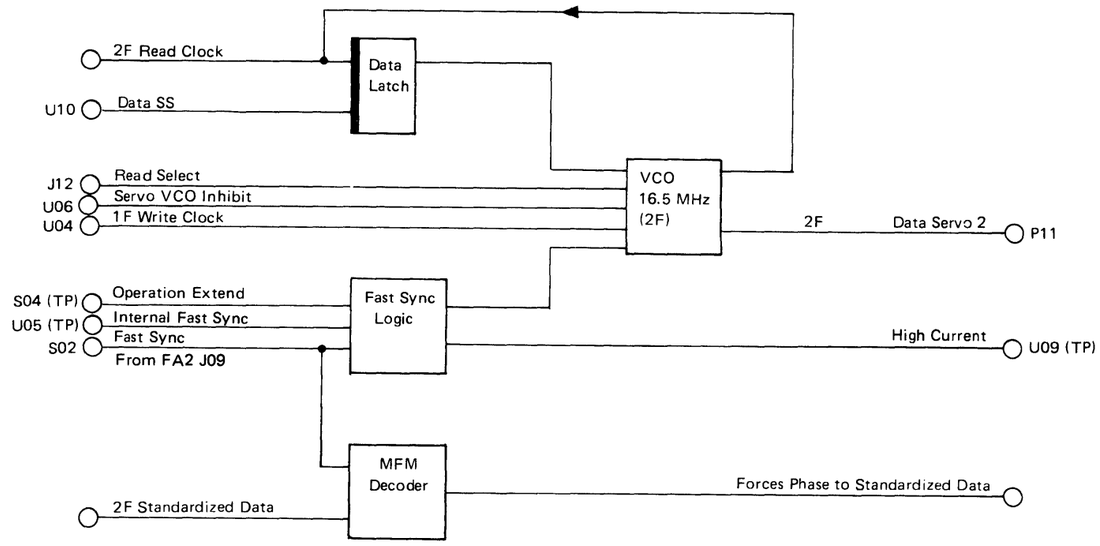



**Figure FA452-14. VCO Control**

### Recalibrate Issued by Processor or Storage and I/O Unit

Recalibrate sequence is as follows (see Figure FA452-15):

1. A recalibrate command issued by the processor is initiated by a tag code of 001 with bus bit 0 active (–).
2. Tag 001 CLK 2 with –go home bit sets –go home.
3. +Out direction drops and + seek is raised.
4. When the actuator arm arrives in the behind home position, seek drops and 4 ms later –seek complete is activated.
5. –Seek complete initiates a further seek with + out direction active to the home position.
6. 4 ms after the seek ends, –seek complete is activated again together with + home and an interrupt to signify completion of the recalibrate.
7. +Home is reset by the next seek operation and remains negative until a further calibrate command sets it again.
8. Handover velocity is not affected by a recalibrate command after the initial power-up sequence.

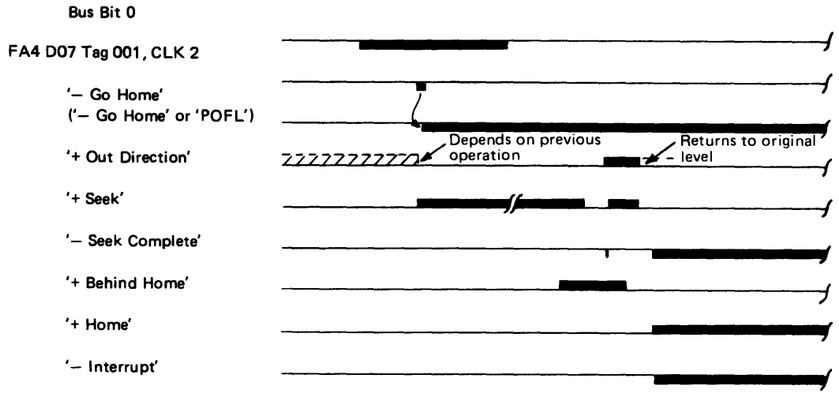



**Figure FA452-15. Recalibration Timing Chart**

## Access and Head Change

Figure FA452-16 indicates the sequence of events for a seek to a higher number cylinder followed by a head change only operation. For a seek in the other direction (to a lower number cylinder), only + out direction will show a different response.

1. A tag decode of 010 and –control sample reads the low-order bits (1–128) of the desired address into the desired address register. If this address is different from the current address, –shift becomes active. +Out direction sets according to the different count from the subtractor. (It may then switch to the opposite condition when the high-order bit 256 of the desired address is received in the next tag cycle.)
2. The subsequent decode of tag 001 with control sample sets the high-order bit 256 of the desired address. + out direction sets and + seek are raised; –shift is deactivated when the desired address and absolute address are equal. This occurs at 1/4 track from the on-track position. + seek deactivates when on track and 4 ms later –seek complete is activated together with –interrupt.
3. The adapter performs a sense cycle which resets the interrupt.
4. During a head change only operation, tags 010 and 001 are used in exactly the same way as for an access. – shift and + out direction may show a response to tag 010 bus data if the low-order address bits differ from the absolute address. They will, however, return to the inactive state when the second tag cycle 001 is received. A seek complete interrupt occurs 4 ms after –control sample received.

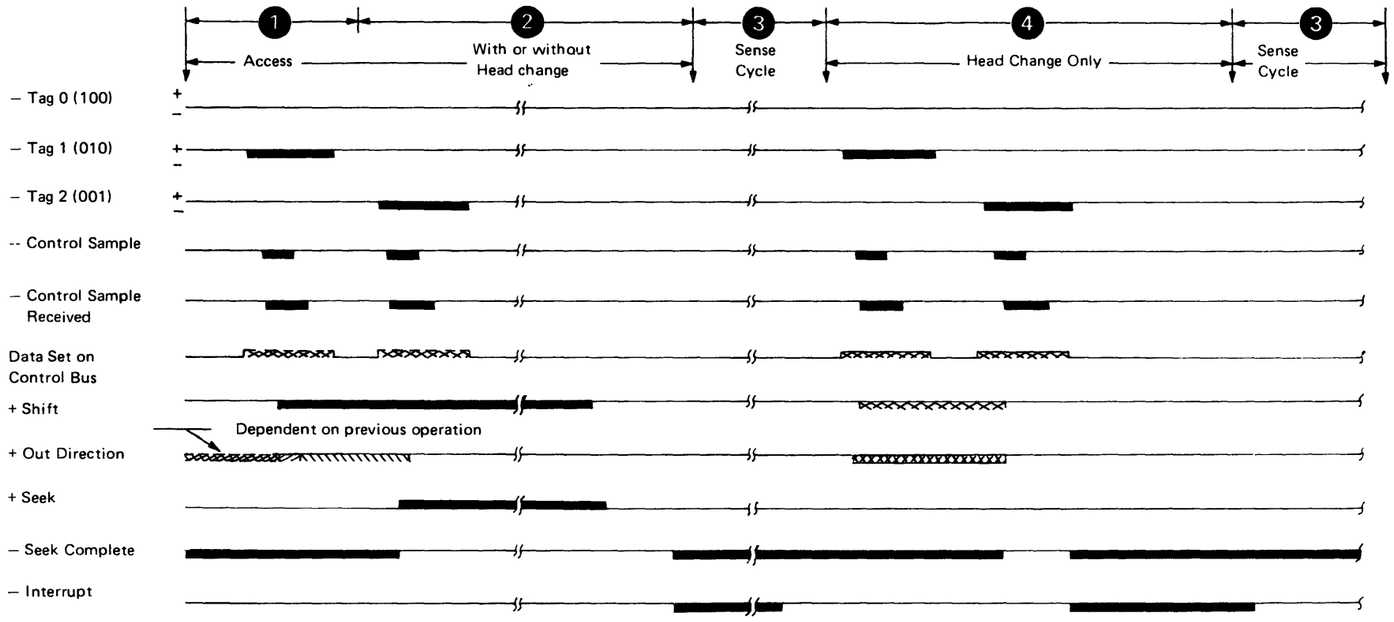



**Figure FA452-16. Access and Head Change Timing Chart**

## Write Safety Detection

**General.** Write safety detection circuits (Figure FA452-17) on the data channel card check operation of the DSD that could affect data written on the disks or data being written.

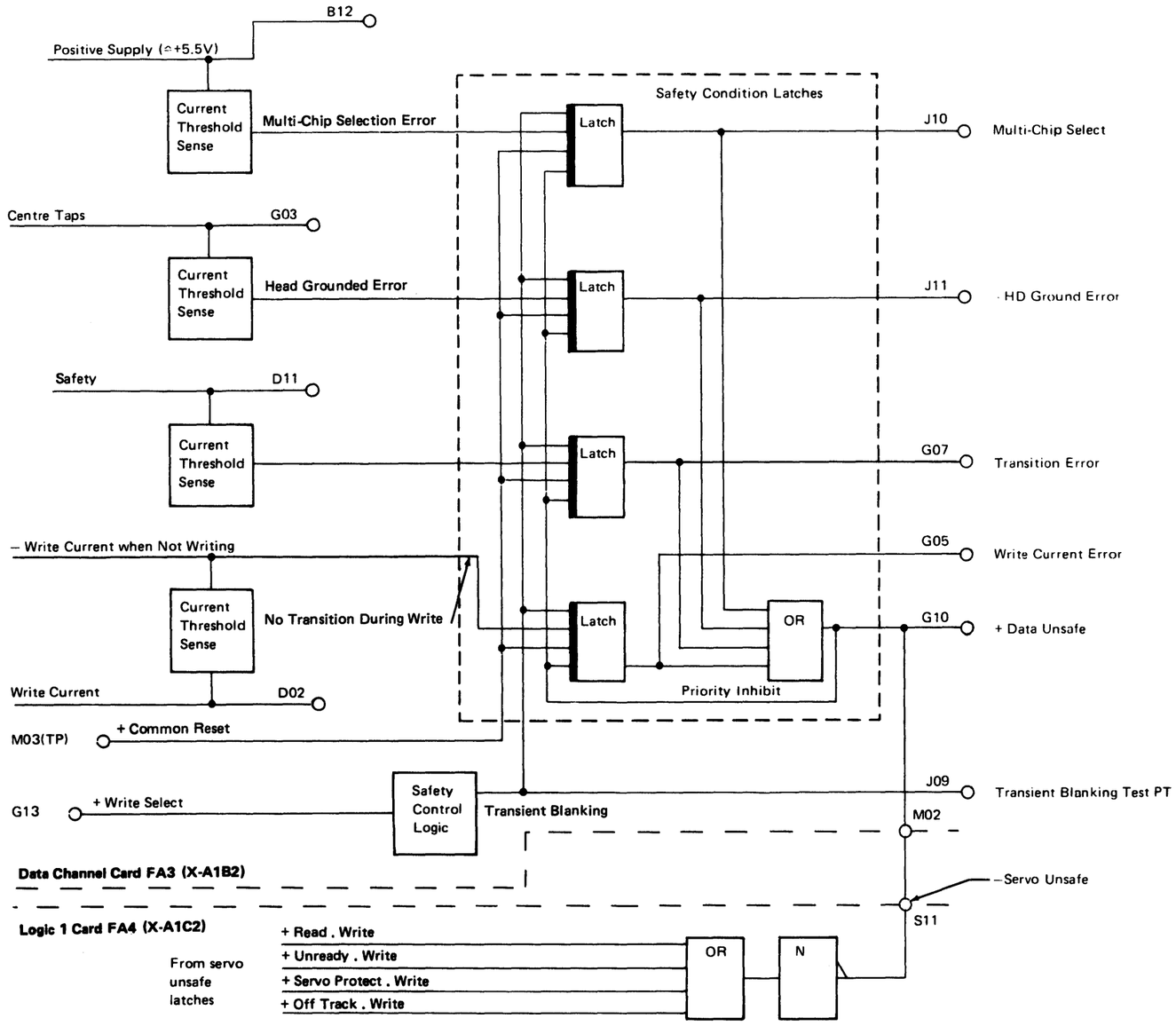



**Figure FA452-17. Write Safety Detection Circuits**

These circuits check for the following unsafe conditions:

- No transitions – that is, failure of write drivers to switch current in a head in write mode.
- Head grounded – this causes excessive current in the center-tap line.
- Multimodule selection – this causes excessive current in the positive power supply to the DE circuits.
- Servo unsafe – logical or analog unsafe conditions external to the data channel.
- Write current when not writing.

Each of the first four unsafe conditions listed above causes a latch to be set in the safety condition latches.

The latch outputs are connected with + servo unsafe to produce the line + data unsafe.

**No Transitions.** Normally, when the current in a head is reversed during a write operation, voltage spikes are produced in the head winding. If these spikes are missing (that is, no transitions occur), either the head or the write driver has failed.

The voltage spikes caused by this failure and the – write gate produce the – no transitions during the writing signal. This signal sets the appropriate safety condition latch.

**Head Grounded.** A head-to-ground short circuit can cause current in the center-tap line to exceed the threshold set in the associated current threshold sense circuit; then a head grounded error signal is produced.

**Multimodule Selection.** If current in the positive supply to the DE exceeds the threshold set in the associated current threshold sense circuit, a multimodule selection error signal is produced.

**Servo Unsafe.** Unsafe logical or analog conditions cause the –servo unsafe signal to be applied to the write safety detection circuit. The –servo unsafe signal is connected with any of the unsafe conditions latched in the safety condition latches to produce + data unsafe.

**Write Current When Not Writing.** An error signal caused by write current flowing when not in writing mode is processed through the sense circuit and safety condition latches, and is then applied to the processor as a 1W error.

**Priority Inhibit.** Priority inhibit prevents any subsequent error from setting the safety condition latches so that only the first error condition is held in the latches.

**Transient Blanking.** Transient conditions that would otherwise set the safety condition latches are inhibited by transient blanking that gates off the latches. Transient blanking is provided in the unsafe detectors circuit. See Figure FA452-18.

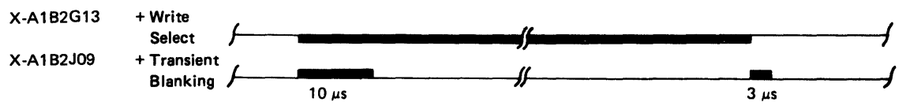



**Figure FA452-18. Transient Blanking Timing**

**Sense/Status Cycle**

A sense or status cycle is initiated by the processor encoding a sense or status tag (tags 011–111) and raising –control sample (see Figure FA452-19). This may be in response to an interrupt or simply a normal housekeeping command.

The tag is decoded by the DSD. Control sample, control sample received, and tags 000, 001, or 010 are combined to raise the internal line enable bus.

Meanwhile, the tag decode has selected the appropriate sense or status bits for transmission to the adapter. Enable bus gates the selected bits to the bus out drivers and, provided that – POD and degate bus are inactive, the bits are transmitted to the using system.

– POD prevents the DSD from responding to a sense or status cycle during the power-up sequence.

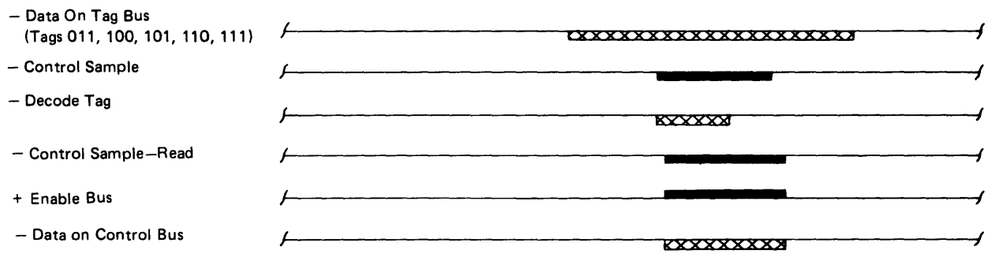



**Figure FA452-19. Sense/Status Timing Chart**

## FA500 Adjustment, Removal, and Replacement Information

### FA510 Scope Charts

The following scope charts were obtained using a Tektronic 453 and are to be used in conjunction with the FA MAP. See Scope Chart 1 for initial scope set up. Subsequent scope charts will only list the changes from the initial setup.

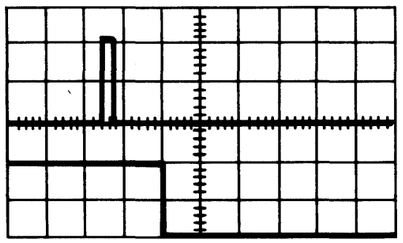
*Scope Chart 1*

1. Use 1X scope probes.
2. Place oscilloscope Channel 1 probe on X-A1D2J09 +SR Clock.
3. Place oscilloscope Channel 2 probe on X-A1D2J10 +Enable Servo Sample.
4. Place oscilloscope EXT TRIG probe on X-A1D2S10.
5. Set oscilloscope controls as shown in the following table:

| | |
|---|---|
| HORIZ DISPLAY | NORMAL TRIG |
| MAG | OFF |
| A SWEEP LENGTH | FULL |
| A TIME BASE | 5 us/DIV |
| MODE | ALT |
| TRIGGER SOURCE | EXT |
| A SWEEP MODE | NORMAL TRIG |
| A TRIG SLOPE | – |
| A TRIG COUPLING | AC |
| TRIG | NORMAL |
| A TRIG LEVEL | 0 |
| A TRIG HF STAB | 0 |
| INVERT | I |

6. Switch CHAN 1 INPUT to GND and adjust trace.
7. Position trace until the center line is ground.
8. Switch CHAN 1 INPUT to DC.
9. Switch CHAN 2 INPUT to GND and adjust trace.
10. Position trace until the center line is ground.
11. Switch CHAN 2 INPUT to DC.
12. Adjust A TRIG LEVEL to display trace.
13. Adjust a POSITION control to start trace at left-hand line.

SCOPE DISPLAY



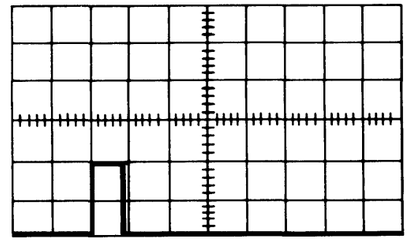
X-A1D2J09 + SR Clock

X-A1D2J10 + Enable Servo Sample

*Scope Chart 2*

1. Move CHAN 2 probe to X-A1D2U13 (+ Enable Mark Detect).
2. Switch MODE to CHAN 2.

SCOPE DISPLAY

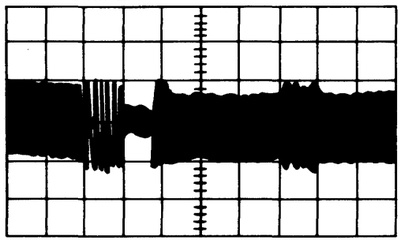


X-A1D2U13 + Enable Mark

*Scope Chart 3*

1. Move CHAN 1 probe to X-A1E2B03 (Data A).
2. Set CHAN 1 V/DIV to 20 mV.
3. Switch CHAN 1 INPUT to AC.
4. Switch MODE to CHAN 1.

SCOPE DISPLAY

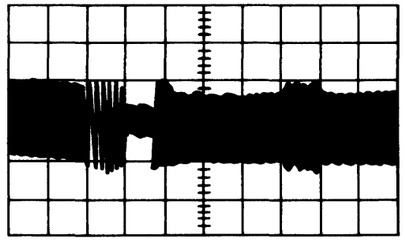


X-A1E2B03 Data A

*Scope Chart 4*

1. Move CHAN 2 probe to X-A1E2D02 (Data B).
2. Set CHAN 2 V/DIV to 20 mV.
3. Switch CHAN 2 INPUT to GND and adjust.
4. Position until the center line is ground.
5. Switch CHAN 2 INPUT to AC.
6. Switch MODE to CHAN 2.
7. Pull INVERT switch.

SCOPE DISPLAY

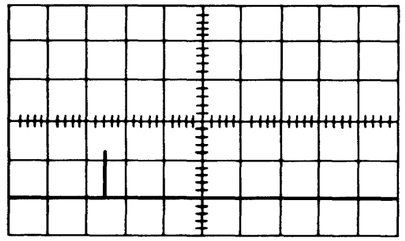


X-A1E2B03 Data A

*Scope Chart 5*

1. Move CHAN 1 probe to X-A1E2G03 (+Vco Inhibit).
2. Set MODE to CHAN 1.
3. Set CHAN 1 V/DIV to 1V.

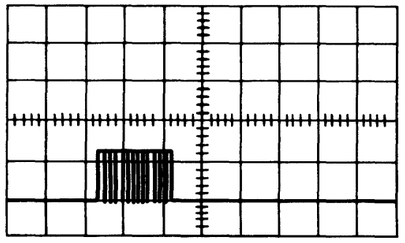
SCOPE DISPLAY



X-A1E2G13 + VCO Inhibit

*Scope Chart 6*

SCOPE DISPLAY

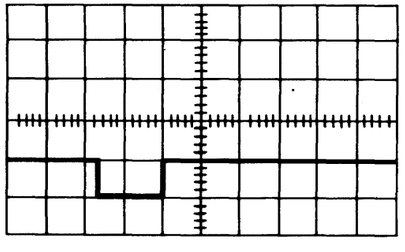


X-A1E2G03 + VCO Inhibit

*Scope Chart 7*

1. Move CHAN 1 probe to X-A1E2J05 (-CRT RUN).

SCOPE DISPLAY

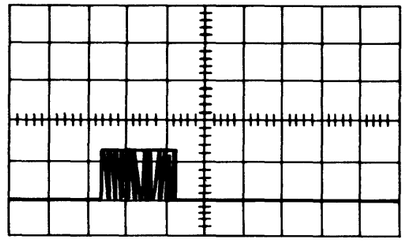


X-A1E2J05 – CTR Run

*Scope Chart 8*

1. Move CHAN 1 probe to X-A1E2G08 (+2F Burst).

SCOPE DISPLAY



X-A1E2G08 + 2F Burst

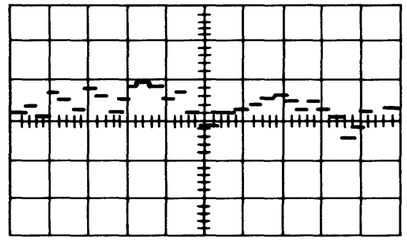
*Scope Chart 9*

SCOPE DISPLAY = a valid MST 1 level (–0.8V to –1.8V)

*Scope Chart 10*

1. Move CHAN 1 probe to X-A1E2B13 (Data PES).
2. Set A TIME BASE to 2 ms.
3. Move EXT TRIG probe to X-A1D2S13 – (System Index).
4. Adjust A TRIG LEVEL to display trace.

SCOPE DISPLAY



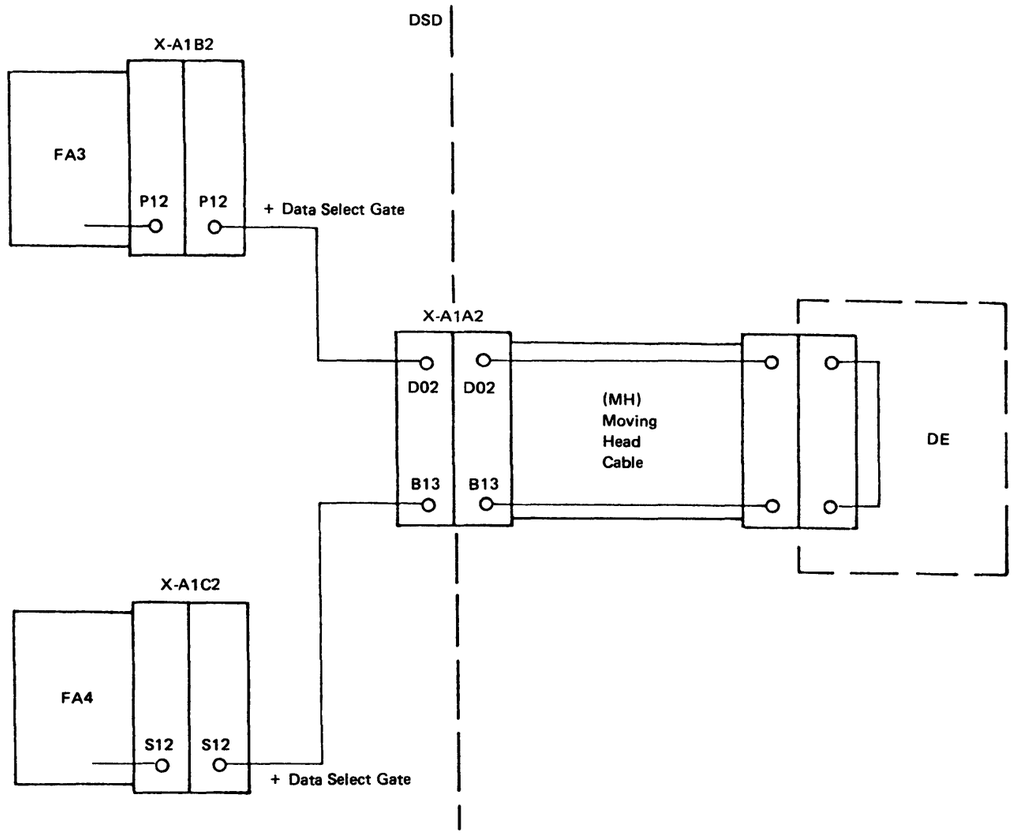
X-A1E2B13 Data PES

## FA520 Adapter and DSD Cable and Card Continuity

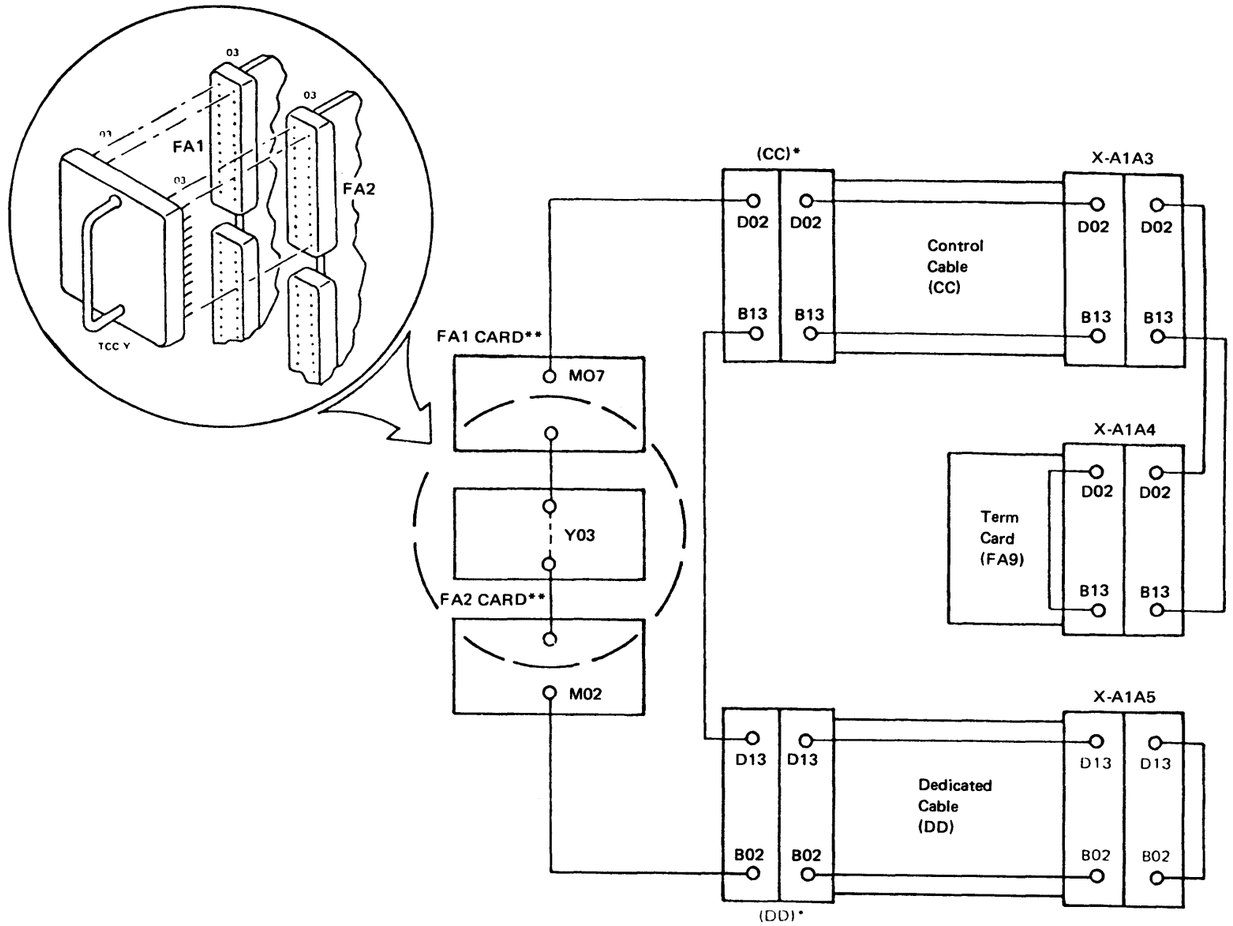
There are two separate areas for cable and card continuity:

1. Data Select Gate continuity checks the Moving Head (MH) cable X-A1A2, the FA3 Data Channel card, and the FA4 Logic 1 card.
2. System continuity checks the Control cable (CC), Dedicated cable (DD), the FA1 and FA2 adapter cards, the TCC Y03, and the FA9 terminator card.

### *FA521 Data Select Gate Continuity*




### *FA522 Disk Adapter to DSD Continuity*




| Mach Type | Model | Pseudo Card and Cable Locations | | | |
|---|---|---|---|---|---|
| | | FA1 ** | FA2 ** | Control (CC) * | Dedicated (DD) * |
| 8130 | A2X | A–A1U2 | A–A1T2 | A–A1Y1 | A–A1Y2 |
| 8140 | A3X/A4X | A–A2Q2 | A–A2P2 | A–A2Z6 | A–A2Z5 |
| 8140 | A5X | A–A2F2 | A–A2E2 | A–A2Z3 | A–A2Z2 |
| 8101 | AXX (Low) | A–A2H2 | A–A2J2 | A–A2Y3 | A–A2Z3 |
| 8101 | AXX (Up) | A–A2E2 | A–A2F2 | A–A2Y2 | A–A2Z2 |
| 8140 | BXX (Low) | A–B2H2 | A–B2J2 | A–A2K4 | A–A2K5 |
| 8140 | BXX (Up) | A–B2F2 | A–B2G2 | A–A2Y3 | A–A2Z3 |

**FA530 Not Used**

## FA540 Disk Enclosure (DE) Removal and Replacement

It is necessary to remove the DSD subframe from the unit to remove the DE. Removing the drive motor eliminates the need to remove the actuator lock lever bracket.

**Cautions:**

1. **Do not remove the DE without requesting aid.**
2. **The DSD weighs 25kg (55 lb). The card gate may be removed to lighten the load (see FA550). Also, in the case of the 8101 Mod A25, removal of the top DSD should require assistance due to weight and leverage constraints.**
3. **The heads on the actuator and the disks might be damaged if the DE pulley is turned counterclockwise.**

### DSD Subframe Removal

1. Switch off electrical power.
2. With the actuator lock lever in the Operate position, remove the spindle lock bracket (2 screws) from the subframe. Do not loosen or remove cable from the spindle lock bracket.
3. Remove the motor from the subframe. Do not disconnect the wires, but lay the motor on the unit frame floor until the new subframe is installed. (See FA570.)
4. If you want to lighten the load, remove the card gate (see FA551) and go to step 11.
5. If you have not removed the card gate, continue by disconnecting the DE ground.
6. Remove the card gate cover and cable retaining plate.
7. Loosen the card gate screw and swing the gate open.
8. Release the fan retainer at the rear of the card gate and withdraw the fan from the gate.
9. Unplug cables Y1 (if fixed heads are installed), A2, A3, and A5.
10. Unplug cables J1, J2, J4, J5 and J9. (J9 also requires that both bottom board retainers be loosened in order to remove cable.)
11. Move the Operator/Lock Lever to the Lock position.
12. Remove the flat cable retaining straps.

    **Note:** *For 8101 Mod A25 units, it will also be necessary to remove the OPERATE/LOCK lever plate.*

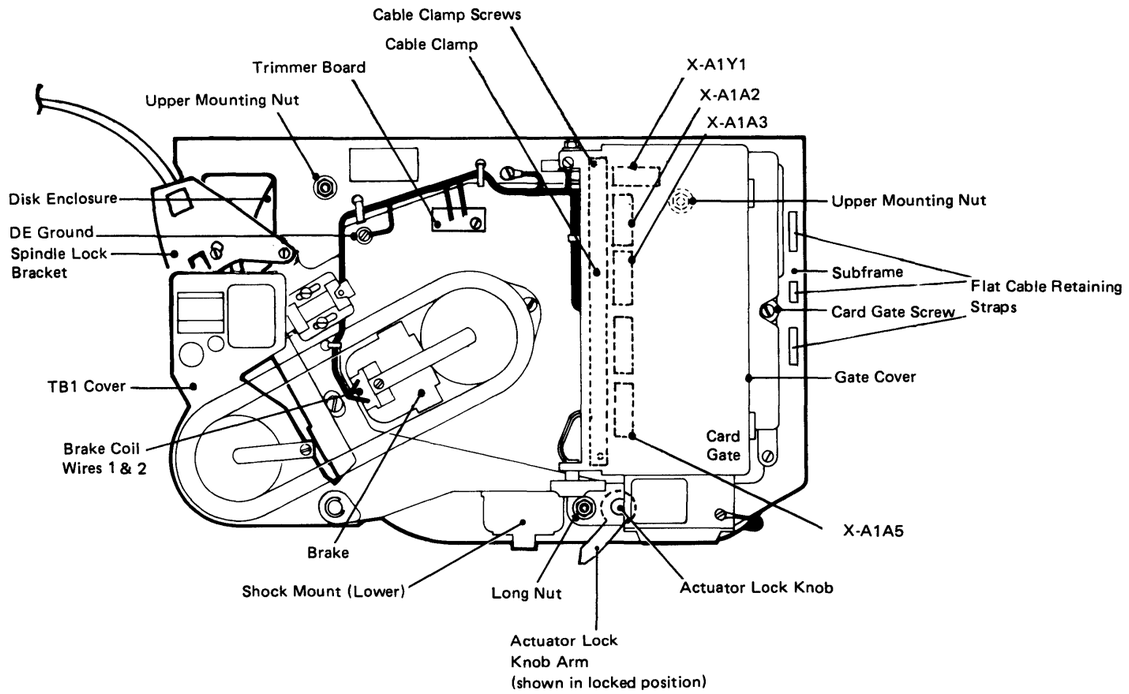
13. Loosen the actuator lock cable retaining bracket.
14. Disconnect the actuator lock cable from the nylon actuator lock knob arm. (See FA590.)
15. Disconnect the frame ground strap.
16. Loosen the three shock mounts, and remove the subframe by sliding it out of the screws. (See FA541.) Stand the DSD on the DE cover on a clean surface.

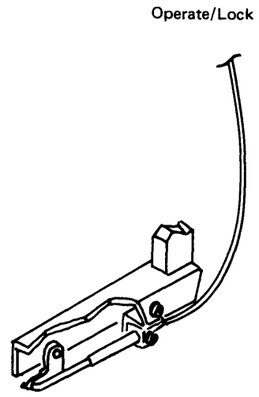
### DE Removal

1. Disconnect the slip-on terminals from the brake and the trimmer resistor.
2. Remove the nylon actuator lock knob bracket.
3. Unscrew the lower (long) DE mounting nut and the two upper DE mounting nuts.
4. Lift the subframe from the DE.

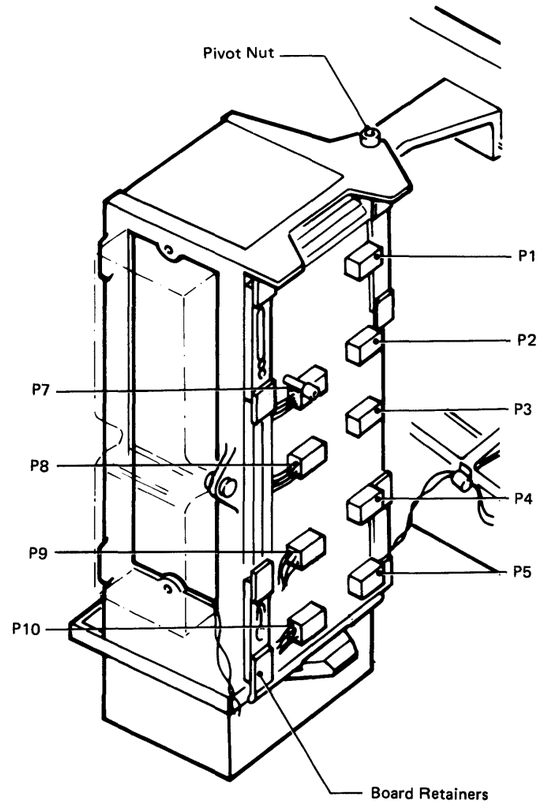
### DE Replacement

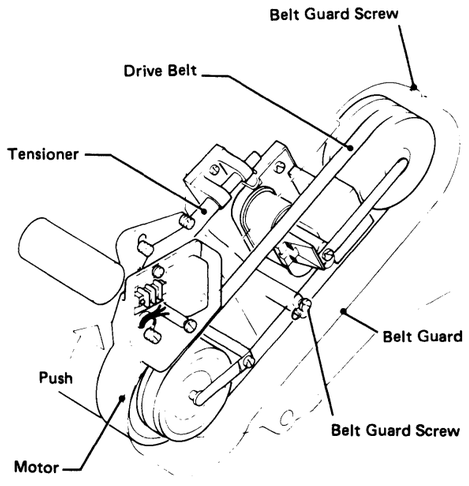
1. To install the DE, reverse the removal procedure.
2. Adjust the belt tensioner and the brake as detailed in FA580 and FA572.
3. Insure that the actuator lock knob is turned fully counterclockwise (the Lock/Operate lever is in the Operate position).
4. Run diagnostics.
5. Format DE using the format utility. (See CP650)

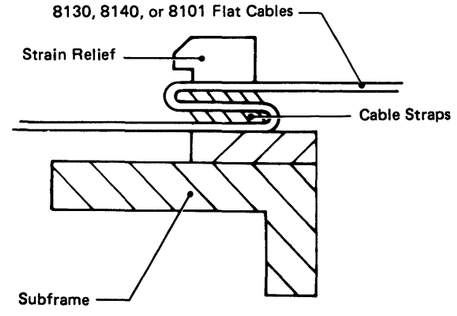



Actuator Lock Lever Assembly



*FA541 Shock Mount Removal*

There are two types of shock mounts: A and B. Determine if the shock mount is type A or type B and use the corresponding procedure.

**Type A (Figure FA541-1)**

1. Loosen the 1/4-20 UNC screws (hex head) to a point that allows the subframe to slide out.

**Type B (Figure FA541-2)**

1. Loosen the 1/4-20 UNC screws (allen head) that attach the subframe to the two upper shock mounts.
2. Insert a hex wrench through the access hole in the machine frame base and remove the hex screw from the lower shock mount. See Figure FA541-3.

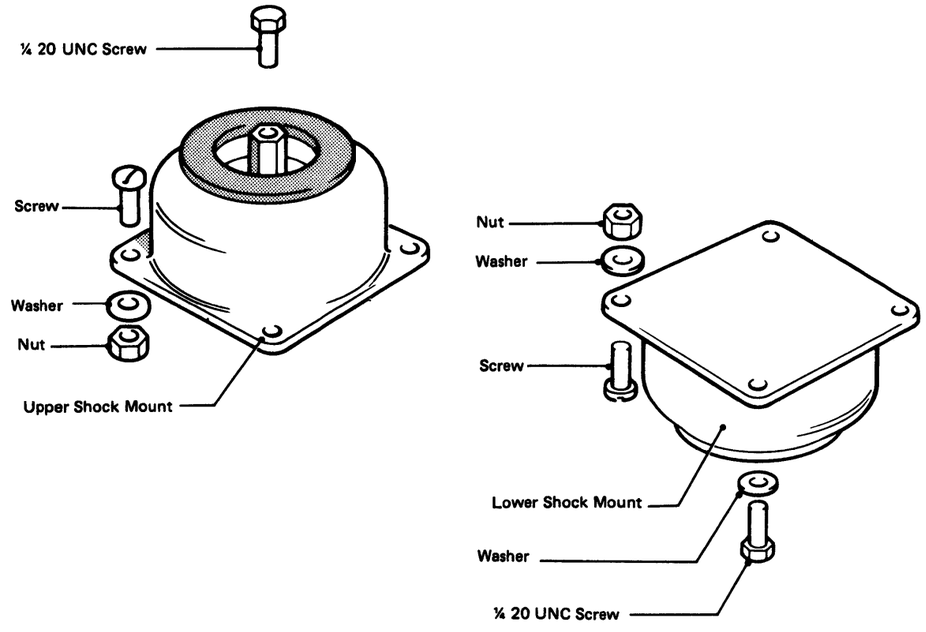



**Figure FA541-1. Type A Shock Mount**

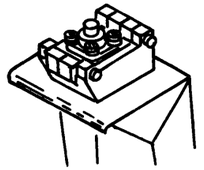


**Figure FA541-2. Type B Shock Mount**

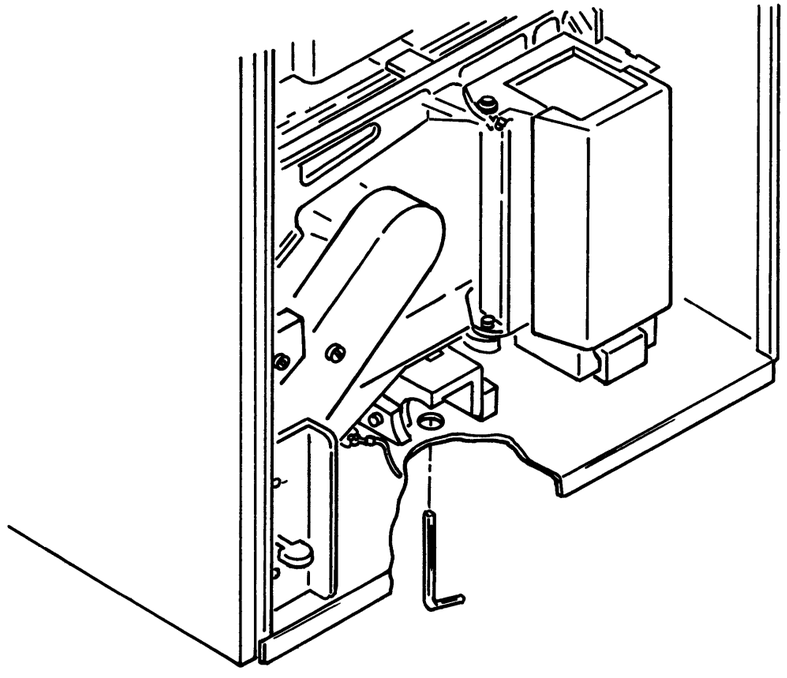


**Figure FA541-3. Type B Shock Mount Access**

## FA550 Card Gate, Board, and VCM Driver Card Removal/Replacement

### *FA551 Card Gate Removal/Replacement*

**Removal**

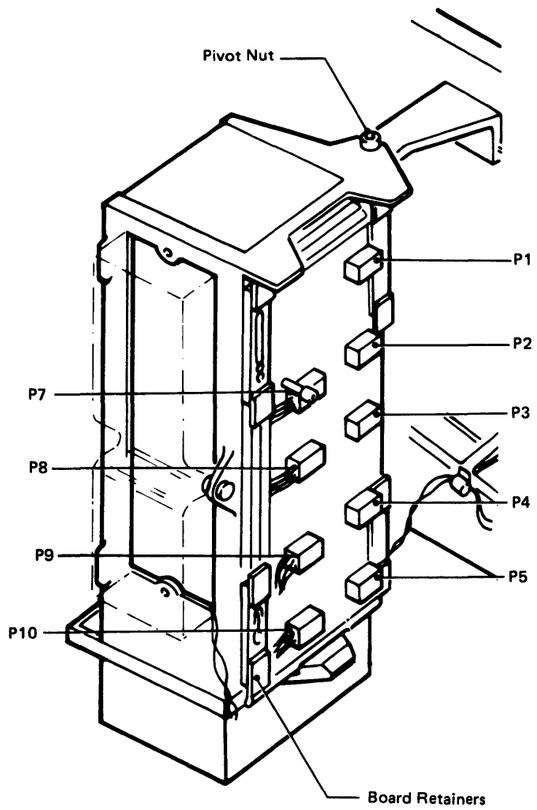
1. Switch off electrical power.
2. Remove the card gate cable clamp screws, then remove the cable clamp and card cover.
3. Disconnect flat cable connectors (CC), (DD), (MH), (FH if installed), and terminator FA9 (A4). See Figure FA111-5.
4. Loosen the card gate screw and open the card gate.
5. If it is necessary to release the 8130, 8140, or 8101 flat cables, remove the cable straps to release the cables.
6. Disconnect voltage connectors J1 through J5, and J9.
7. Disconnect the ground connector from the gate casting.
8. Release the cables from under the board retainers by loosening the board retainer screws and lifting the retainers.
9. Disconnect the fan supply from terminal block TB2.
10. Unscrew the pivot nut from the upper pivot and lift the gate off both pivots.

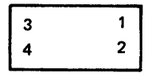
**Replacement**

Install the card gate in the reverse order to that used to remove it.

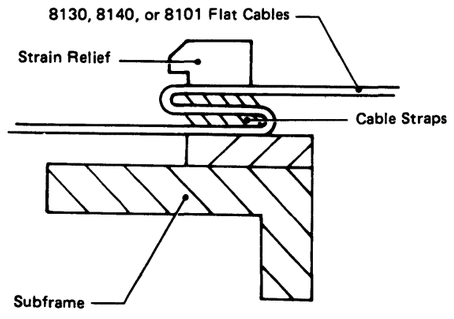
**Note:** *If the 8130, 8140, or 8101 flat cables were released from the subframe cable clamp, reclamp the cables with the rubber straps as shown.*

*Allow sufficient slack cable around the pivot area of the card gate (the length of cable should be approximately 240 mm (1 inch) from the cable clamp to the end of the socket.)*




P-Connector as viewed when plugged



### *FA552 Board Removal/Replacement*

**Removal**

1. Switch off electrical power
2. Remove the cable clamp and the card cover.
3. Unplug the cards and the flat cable connectors.
4. Note card part numbers and locations.
5. Open the card gate.
6. Unplug the voltage connectors from the pin side of the A1 board.
7. Loosen four screws holding the board retainers and lift out.

**Replacement**

1. Install board A1 in the reverse order to that used to remove it.

### *FA553 Voice Coil Motor (VCM) Driver Card Removal/Replacement*

The card is screwed to the inside of a plastic cover attached to the right-hand end of the card gate.

**Removal**

1. Unplug the voltage connectors J7, J8, and J10.
2. Remove the cover screws and cover.
3. Remove card retaining screws and card.

**Replacement**

1. Install the VCM driver card in the reverse order to that used to remove it.

### FA560 Card Gate Fan Removal/Replacement

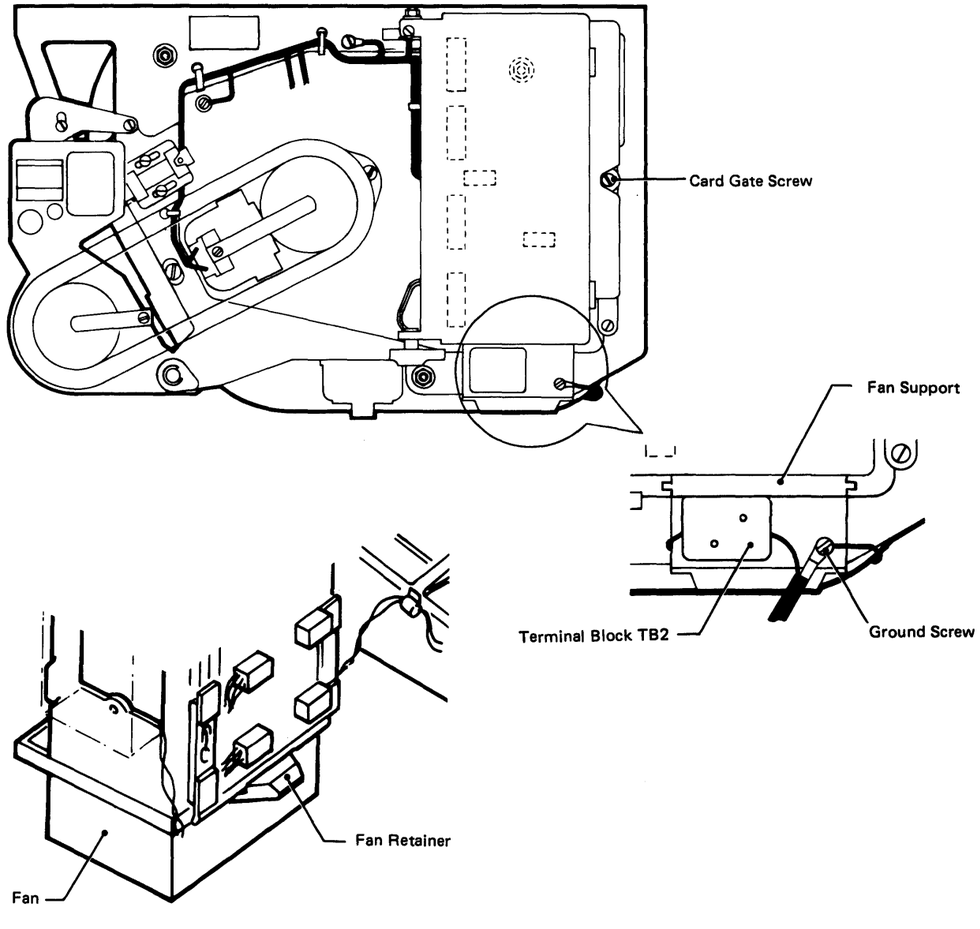
**Removal**

**Caution: Before removing the fan, note the 'direction-of-airflow' arrow to ensure that the fan can be refitted correctly.**

1. Remove all power from DSD.
2. Disconnect the fan supply wires from terminal block TB2 and the adjacent ground screw.
3. Loosen the card gate screw and open the card gate.
4. Release the fan retainer at the rear of the card gate and withdraw the fan from the card gate.

**Replacement**

1. Install the card gate cooling fan in the reverse order to that used to remove it.



## FA570 Drive Motor and Drive Belt

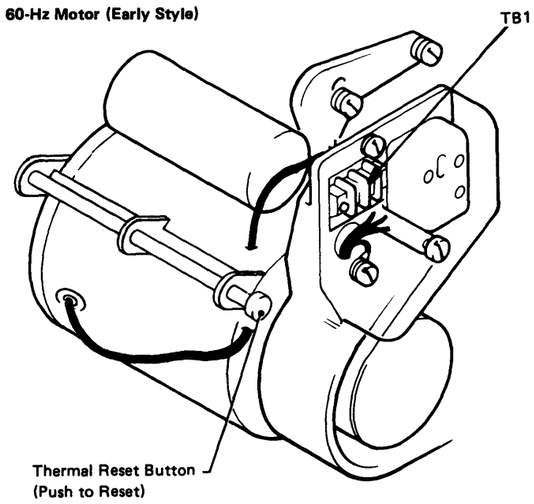
### *FA571 Drive Motor*

**Drive Motor Characteristics**

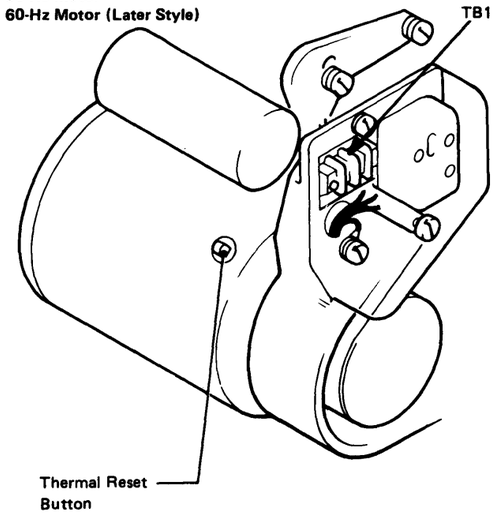
The drive motor is fitted with a thermal cutout that prevents overheating of the motor. The thermal cutout will not reset until the motor has cooled.

**Caution: Switch off all power to the DSD before pressing the Thermal Reset button.**

**60-Hz Motor (Early Style)**




**50-Hz Motor**
**60-Hz Motor (Later Style)**




The following table shows the motor frequencies and voltage ranges:

| Country | Hz | Nom | Min | Max |
|---|---|---|---|---|
| U.S. | 60 | 120 | 104 | 127 |
| Other than U.S. & Canada | 60 | 100 | 90 | 110 |
| | | 110 | 96.5 | 119 |
| | | 120 | 104 | 127 |
| | | 127 | 111 | 137 |
| | | 200 | 180 | 225 |
| | | 208 | 180 | 225 |
| | | 220 | 193 | 238 |
| | | 230 | 201 | 254 |
| | | 240 | 201 | 254 |
| Other than U.S. & Canada | 50 | 100 | 90 | 110 |
| | | 110 | 96.5 | 119 |
| | | 200 | 180 | 220 |
| | | 220 | 193 | 238 |
| | | 230 | 202 | 249 |
| | | 240 | 210 | 259 |

**Note:** *Drive motor input VAC may be measured at TB1.*

## Drive Motor Assembly Removal/Replacement

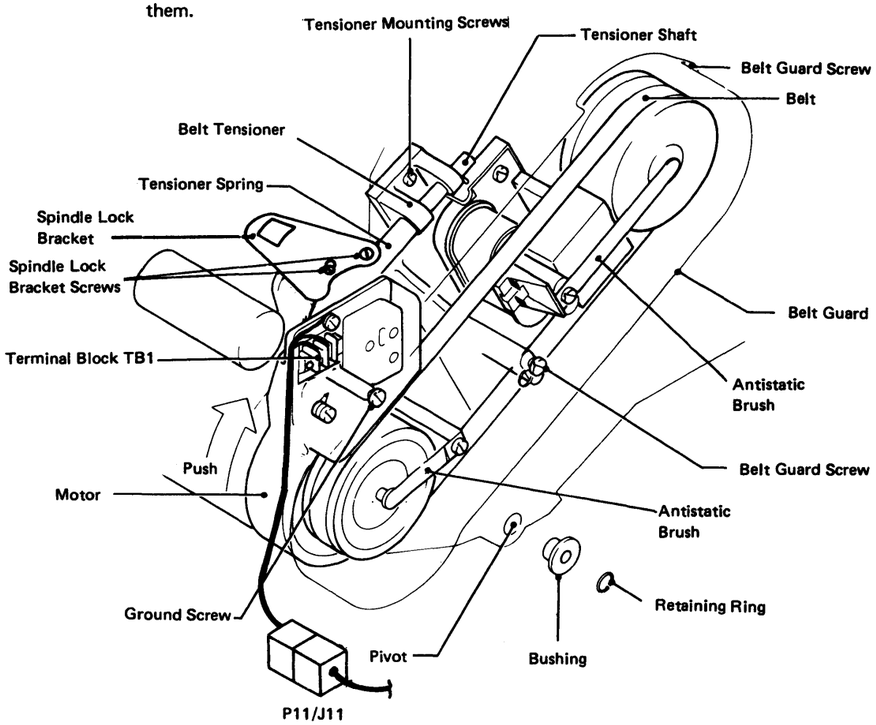
### Removal

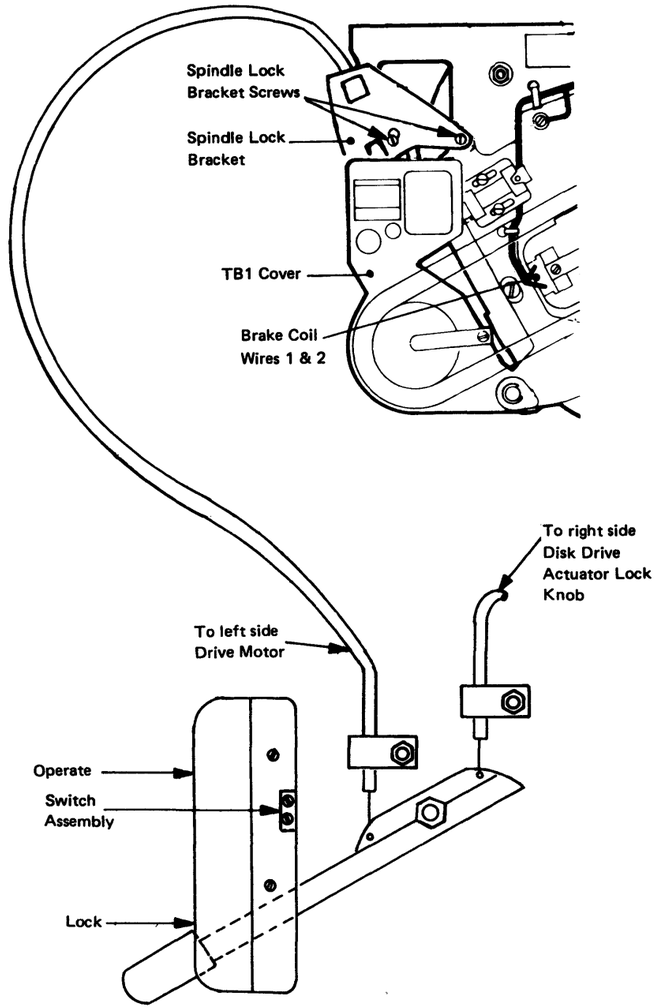
The drive motor assembly is a field replaceable unit (FRU) that consists of the motor, the motor bracket with pivots, and the driving pulley.

1. Switch off electrical power.
2. Remove the spindle lock bracket.
3. Disconnect operated lock mounting bracket from the frame.
4. If removing the motor for DE replacement, go to step 7.
5. Remove the motor terminal block TB1 cover.
6. Disconnect the wires from TB1 and the adjacent ground screw.
7. Loosen the two belt guard screws and slide the belt guard off.
8. Push the motor against the belt tensioner and turn the tensioner shaft so that the tensioner spring is held in compression.
9. Remove the tensioner mounting screws and remove the tensioner. Allow the belt to support the weight of the motor.
10. Remove the retaining ring (C clip) from the motor pivot.
11. Supporting the weight of the motor, remove the belt, then move the motor toward the rear until the pivots are clear of the holes.

    **Note:** *The motor pivot bushings might fall off as the motor is removed.*

12. Remove the pivot bushings and inspect them carefully; if they are damaged, renew them.



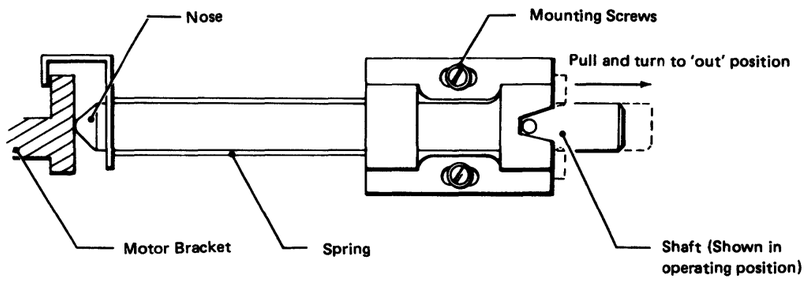

### Replacement

1. Install drive motor in the reverse order of removal.
2. Adjust the belt tensioner as detailed in FA572.

*FA572 Drive Belt*

**Drive Belt Tensioner**

1. Switch off all power to the DSD.
2. Pull the shaft and turn it through 90 degrees so that it locks in the 'out' position.
3. Loosen the two mounting screws.
4. Allow the tensioner assembly to find its own position resting against the motor bracket.
5. Retighten the two mounting screws.
6. Turn the shaft and release it so that it is pulled into the operating position.




**Drive Belt Removal/Replacement**

**Removal**

**Caution: Do not turn the DE spindle pulley counterclockwise as this may damage the heads and disks.**

1. Switch off all power to the DSD.
2. Loosen the two belt guard screws and remove the belt guard.
3. Lift the motor against the force of the belt tensioner and lift off the belt.
4. Gently lower the motor till it rests on its stop.

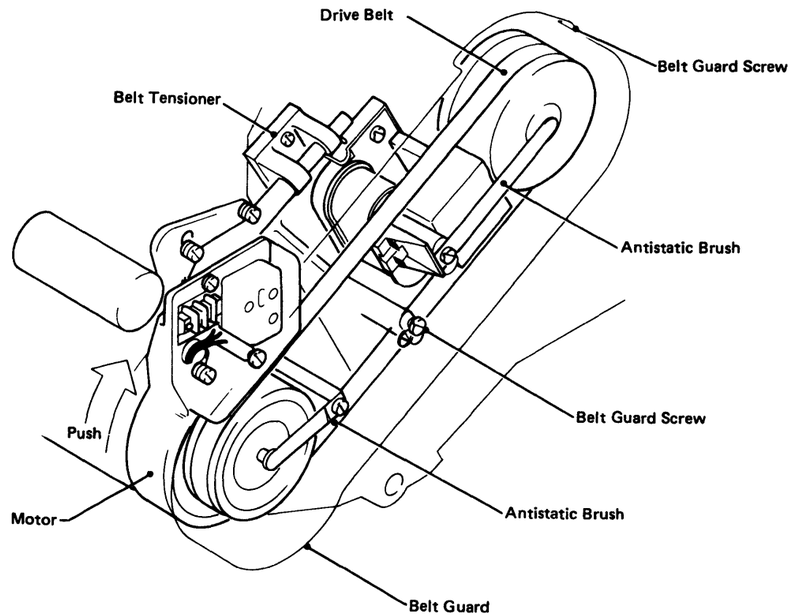
**Replacement**

Make sure that the belt to be fitted is clean, dry, and not frayed or otherwise damaged.

1. Push the motor against the tensioner and fit the belt centrally on the pulleys.

   **Note:** *The smooth side of the belt should bear on the faces of the pulleys.*

2. Allow the motor to be supported by the belt. Fit the belt guard and tighten the screws.
3. Adjust the tensioner.
4. Refit the belt guard.




**Antistatic Brushes**

The antistatic brushes are accessible when the belt guard is removed as described in the previous procedure.

When fitting a new brush, ensure that the carbon brush is centered on the associated pulley.

Refit the belt guard.

## FA580 Brake Assembly and Coil Removal, Adjustment, and Replacement

### Removal

**Caution: When the brake assembly has been removed, do not turn the DE spindle pulley counterclockwise as this may damage the heads and disks.**

1. Switch off all power to the DSD.
2. Loosen the two belt guard screws and remove the belt guard.
3. Push the motor against the force of the belt tensioner and lift off the belt.
4. Disconnect wires 1 and 2 from the brake coil.
5. Remove the two screws that attach the brake assembly and lift out the brake assembly complete with the antistatic arm.

### Adjustment

1. Switch off all power to the DSD.
2. Remove the belt guard.
3. Check that there is a gap of 0.25 mm (0.010 in.) between the coil core on the base and the armature. If not, adjust the brake as follows:
   a. Insert a 0.25 mm (0.010 in.) feeler gauge between the coil core and the armature, and hold the two castings and the pulley together, as shown.

      **Note:** *Ensure that the feeler gauge is clear of the small coil spring (not illustrated) recessed in the armature.*

   b. Tighten the two mounting screws.
   c. Remove the feeler gauge.
   d. Recheck the adjustment.

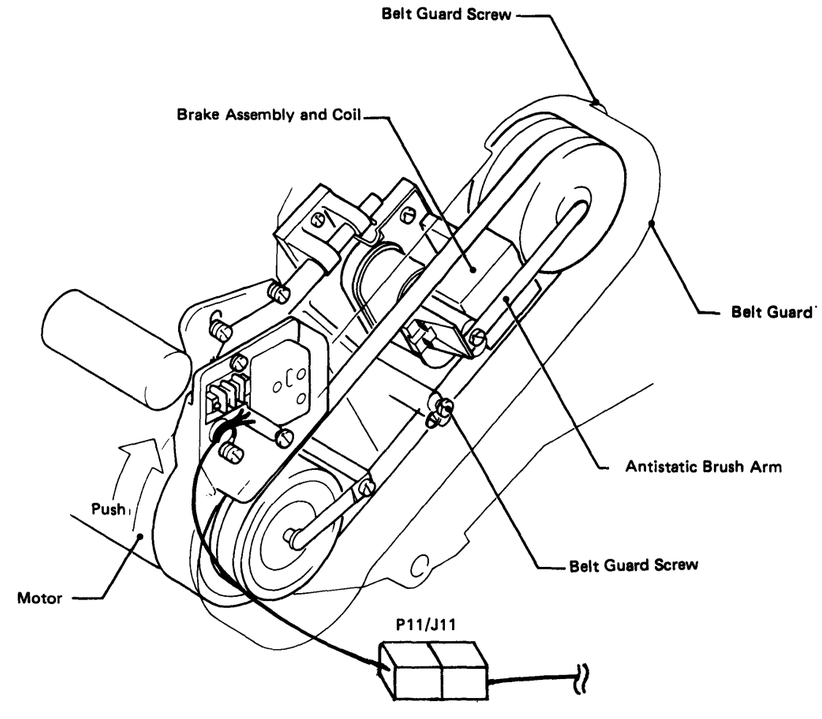
### Replacement

1. Attach the brake and coil loosely to the DE with the two brake mounting screws.
2. Attach the antistatic brush arm to the core casting with the brush arm screw.
3. Adjust the brake as follows:
   a. Insert a 0.25 mm (0.010 in.) feeler gauge between the core casting and the armature casting, and hold the two castings and the pulley together.

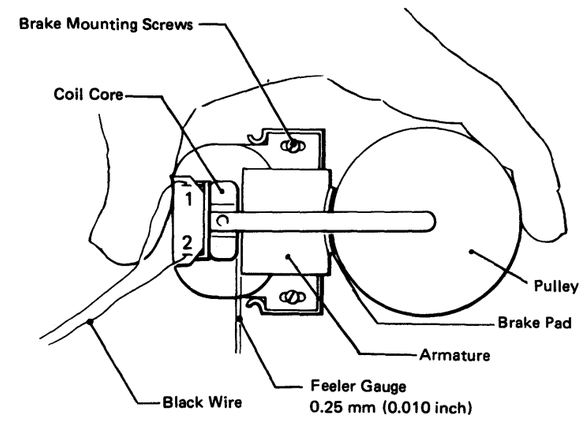
      **Note:** *Ensure that the feeler gauge is clear of the spring (not illustrated) recessed in armature.*

   b. Tighten the two brake mounting screws.
   c. Remove the feeler gauge.

**Caution: The wires 1 and 2 must be connected to the correct terminals (marked 1 and 2) on the coil.**




4. Connect wires 1 and 2 to their respective coil terminals marked 1 and 2.
5. If necessary, adjust the antistatic brush arm until the brush bears centrally on the DE pulley spindle.
6. Lift the motor against the force of the belt tensioner and fit the drive belt. Ensure that the smooth side of the belt bears on the pulleys. Allow the motor to be supported by the belt.
7. Fit the belt guard and tighten the belt guard screws.



## FA590 Actuator Lock Knob and Lock/Operate Switch Adjustment

**Actuator Lock Lever Cable Adjustment**

1. Position both Lock/Operate lever and Actuator Lock Knob Arm in the LOCK position.
2. If cable has been removed, insert control cable into levers.
3. Tighten cable clamps (see insert for correct position of the clamp).
4. Adjust outer sleeves of cables and tighten clamps as required to give satisfactory lockout operation. Provide full travel of the actuator lock arm on the DE in both lock and operate positions.

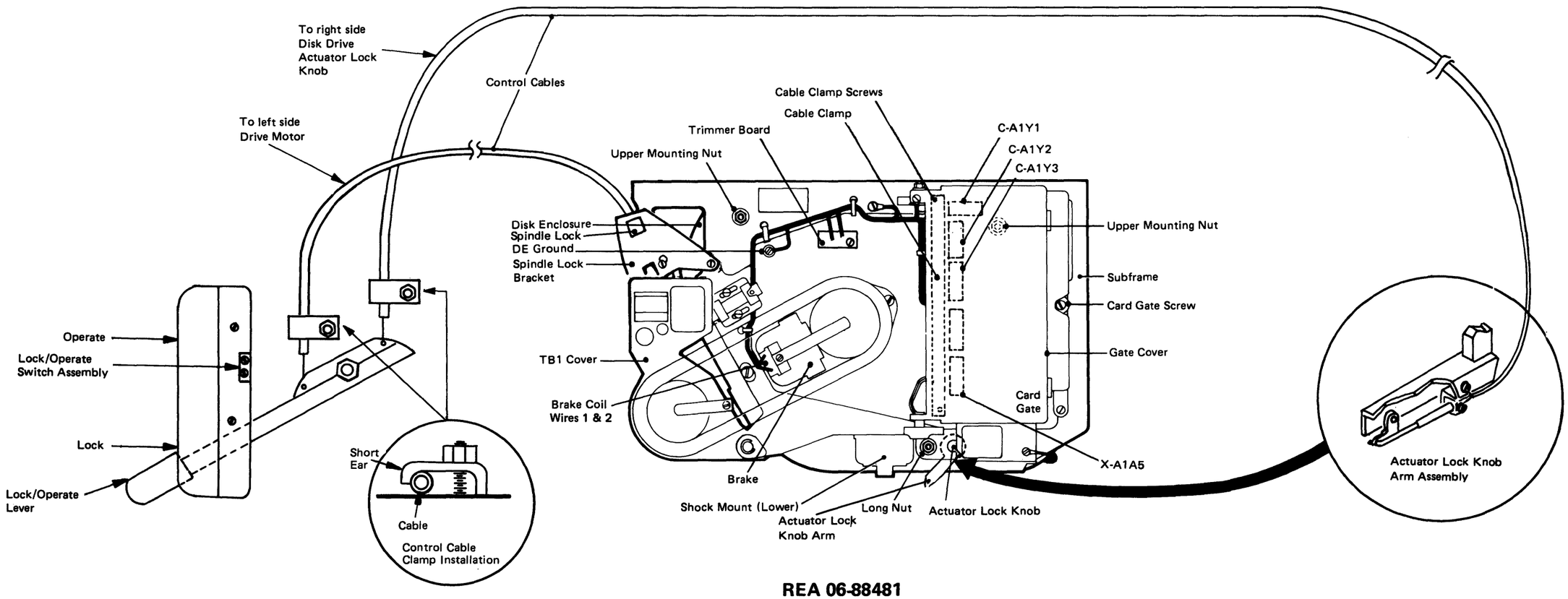
Use the following figure to locate and adjust the Lock/Operate lever cables.

**Lock/Operate Switch Adjustment**

1. Place the Lock/Operate lever in the OPERATE position slot.
2. Adjust the switch down, and rotate counterclockwise until the switch actuator over-travel is taken up.
3. Tighten screws.

**Note:** *The ACTUATOR LOCK KNOB ARM has been known, in some cases, to slip around the ACTUATOR LOCK KNOB. This could result in an improper unlocking condition, even though the ACTUATOR LOCK KNOB ARM is moving its full travel.*

*Visually inspect to see that the ACTUATOR LOCK KNOB turns with the full travel of the ACTUATOR LOCK KNOB ARM, while operating the LOCK/OPERATE LEVER.*



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# Chapter 5. MAP Reference Information
# Power
# (PA)

## Introduction

This part of Chapter 5 provides maintenance information to service the 8130/8140/8101 power. The PA MAP guides you in isolating power failures, and refers to this part of Chapter 5 for locations, adjustments, service checks, or replacement procedures.

This part has seven sections:

1. General Information (PA100–PA130): Contains information on PA configuration, operation, and repair strategy.
2. Offline Tests (PA200–PA253): Contains test information and failure plans.
3. Intermittent Failure Repair Strategy (PA300–PA310): Contains information to repair intermittent failures.
4. Signal Paths (PA400–PA466): Contains figures and wiring charts which show wiring and signal paths.
5. Adjustment, Removal, and Replacement Information (PA500–PA540): Contains information for adjusting the plus 5 volt dc and for removing the LED and BOP.
6. Service Checks (PA600–PA680): Contains information for checking transformers, diodes, and voltages.
7. Locations (PA700–PA760): Contains information for basic locations.



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## Abbreviations

| | |
|---|---|
| BOP | basic operator panel |
| CRP | channel request priority |
| EFP | expanded function operator panel |
| FRU | field-replaceable unit |
| Hz | Hertz |
| IPL | initial program load |
| LED | light emitting diode |
| MAP | maintenance analysis procedure |
| OV | overvoltage |
| PN | part number |
| POR | power-on reset |
| PSCF | Primary System Control Facility |
| SCF | System Control Facility |
| SCR | silicon-controlled rectifier |
| SSCF | Secondary System Control Facility |
| TB | terminal block |
| UV | undervoltage |

# PA100 General Information

**DANGER**
**With the power cord connected to the wall outlet, line voltage and the +5 and +24 control voltages are always present in all:**

- **8130s, 8140 Models AXX, and 8101s.**
- **8140 Models BXX with the line voltage circuit breaker (CB1) on.**

**Before removing metal covers or internal power components (except for power control (PC) and logic cards), either (1) disconnect the power cord for all 8130s, 8140 Models AXX, and all 8101s, or (2) turn off CB1 for 8140 Models BXX.**

**Note:** *If the +5V or +24V control voltage is missing, the 8130/8140/8101 will not power up.*

Eight system voltages are developed from the 01G-T2 transformer windings: +5, +8.5, +12, +24, -5, -8.5, -4, and -12 volts. If the disk storage is not installed, only the -5 volts is sensed. If the -5 volts is not present, the 8130/8140/8101 will not power on. If the disk storage is connected, +12, +24, -4, -12 and one +5V supply are sensed to ensure that the voltages are present. See PA124 for more information on voltage sensing.

A thermal switch is located in the 01A gate, and manual reset thermal circuit breakers are located in the 01C and 01E gate disk drive motors. Excessive gate temperature will cause the 01A gate thermal switch to open and the machine will power down. Excessive motor temperatures causes the disk drive thermal circuit breaker to open and turn off ac power to that disk drive motor. All other power remains on. If the disk storage is connected and the disk drive fails to get up to speed, the power to that disk drive motor drops in approximately 20 seconds. This 20-second time-out can also result from an open thermal switch in the motor, a broken or misaligned drive belt, a deenergized disk motor brake, or the lock-operate lever not in the operate position.

The 8130/8140/8101 can be connected to one of several different line voltage sources. The 01G gate power supply contains one of three types of ferro transformers in the line voltage circuit. Which type of transformer is installed depends upon the country and frequency of the source voltage. All of the transformers have the same output voltages and power controls; the only differences are the input voltages and frequency. The following table lists the transformer part number for the appropriate input voltages and frequencies:

| Input Voltage | Frequency | Phase | Where Used | Transformer Part Number |
|---|---|---|---|---|
| 120 Note 1 | 60 Hz | 1 | U.S. and Canada | 7389040 |
| 208, 240 | 60 Hz | 1 | U.S. and Canada | 7389042 |
| 100/110/115/120/127/ 200/208/220/230/240 | 60 Hz | 1 | Other than U.S. and Canada | 7389042 |
| 100/110/200 220/230/240 | 50 Hz | 1 | Other than U.S. and Canada | 7389041* 7389297** |

*The value of C12 must be 15 microfarads.
**The value of C12 must be 18 microfarads.

**Note 1:** *Check all voltages with CE voltmeter (PN 1749231 or equivalent), using meter lead set PN 453697 and either probe set PN 453698 or probe PN 453718.*

## PA110 Components

The PA power is made up of a line cord, the basic power gate (01G) other power gates (8140 models BXX), and the distribution to other components. Mounted on the rear of the 01G gate are transformers 01G-T1 and 01G-T2, line filter (FL1) mounted on TB4, card PC1, and various capacitor, fuse, and diode modules. The PC3 and PC4 cards mount on the PC1 card. The PC2 card is part of the -4V supply for the first disk drive, and mounts on the front of the 01G power gate for 8130s, 8140 Models AXX, and 8101s and on the M/N gate ofr 8140 Models BXX. The PC50 card is part of the -4V supply used for the second disk drive. See Figure PA110-1 and PA740 for 01G component locations.

You must know the unit model number to use this power section of the MIM. Always verify the model number.

**Note:** *The 8101 does not have a convenience outlet or fuse F13.*

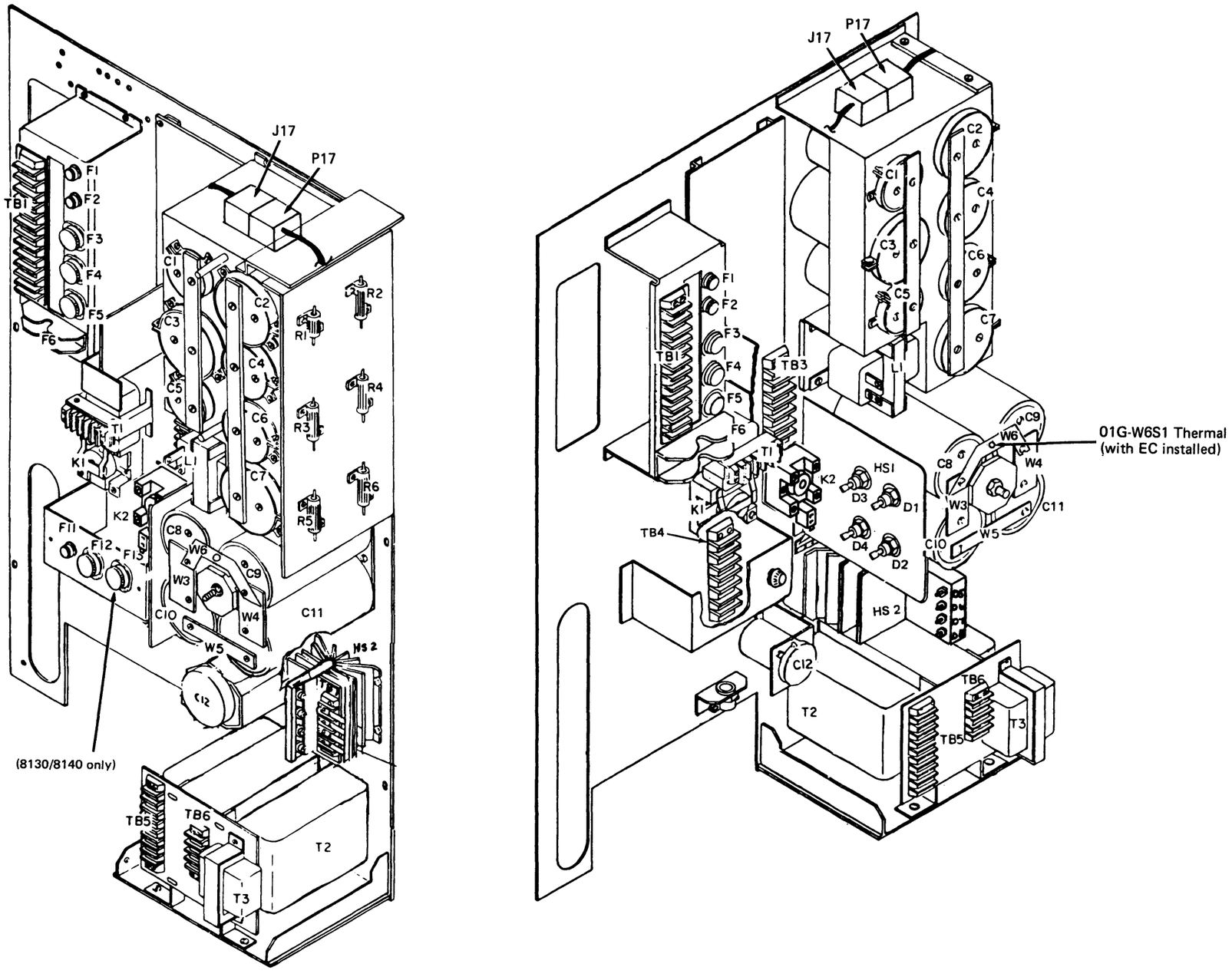



Figure PA110-1. 01G Power Gate Hardware Configuration, Rear View

## PA120 Basic Operational Description

Line voltage is supplied to the system through the line filter, TB4, and fuse F11 to control voltage transformer 01G-T1. The secondary windings of T1 develop two control voltages that are present as long as the power cord is connected to the line voltage, except on 8140 Models BXX (see PA100). These control voltages (+5V CTL and +24V CTL) are used to start the power-up sequence, and the absence of either voltage will prevent system power from cycling up.

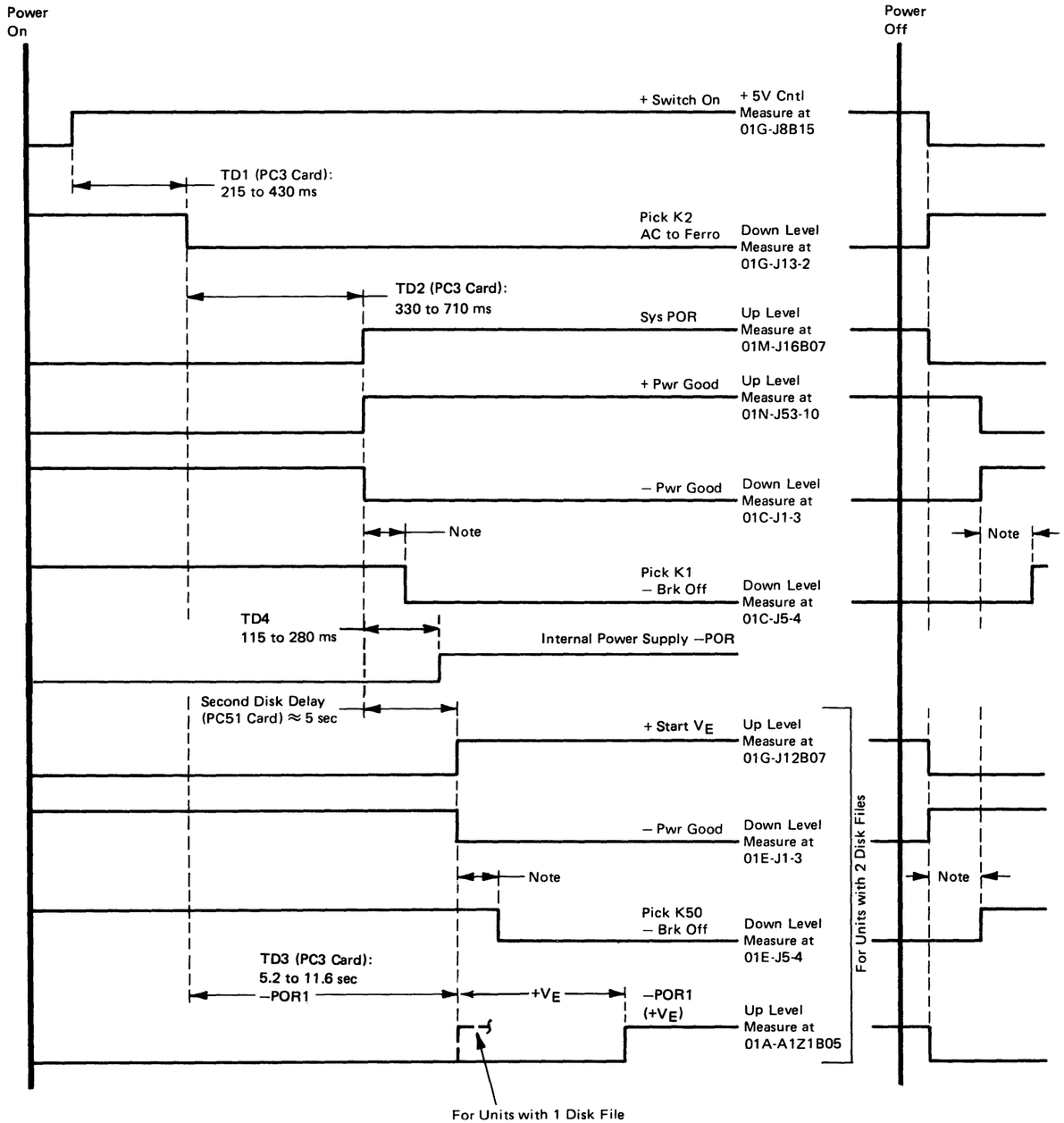
When the main power switch is placed in the on position, K2 is picked and ac power is applied to transformer 01G-T2, the diskette drive motor, and all fans. After a time delay to permit the dc voltages to stabilize, ac power is applied to the first disk drive motor through the points of contactor K1 (see Figure PA120-1) and approximately 5 seconds later, to the second disk drive motor (if installed) through K50.

The secondary windings of T2 develop the system voltages which are distributed to the 01A gate through 01G-TB1, 01A-TB1, and 01A-TB2. The system voltages are further distributed by jack connectors to the different functional components. See Figure PA120-2 for basic power on logic, Figure PA120-3 for the basic power distribution, and PA440 through PA443 for more detailed information on dc distribution.

When 8101 units are attached to the 8130/8140, they are powered up using the following procedure:

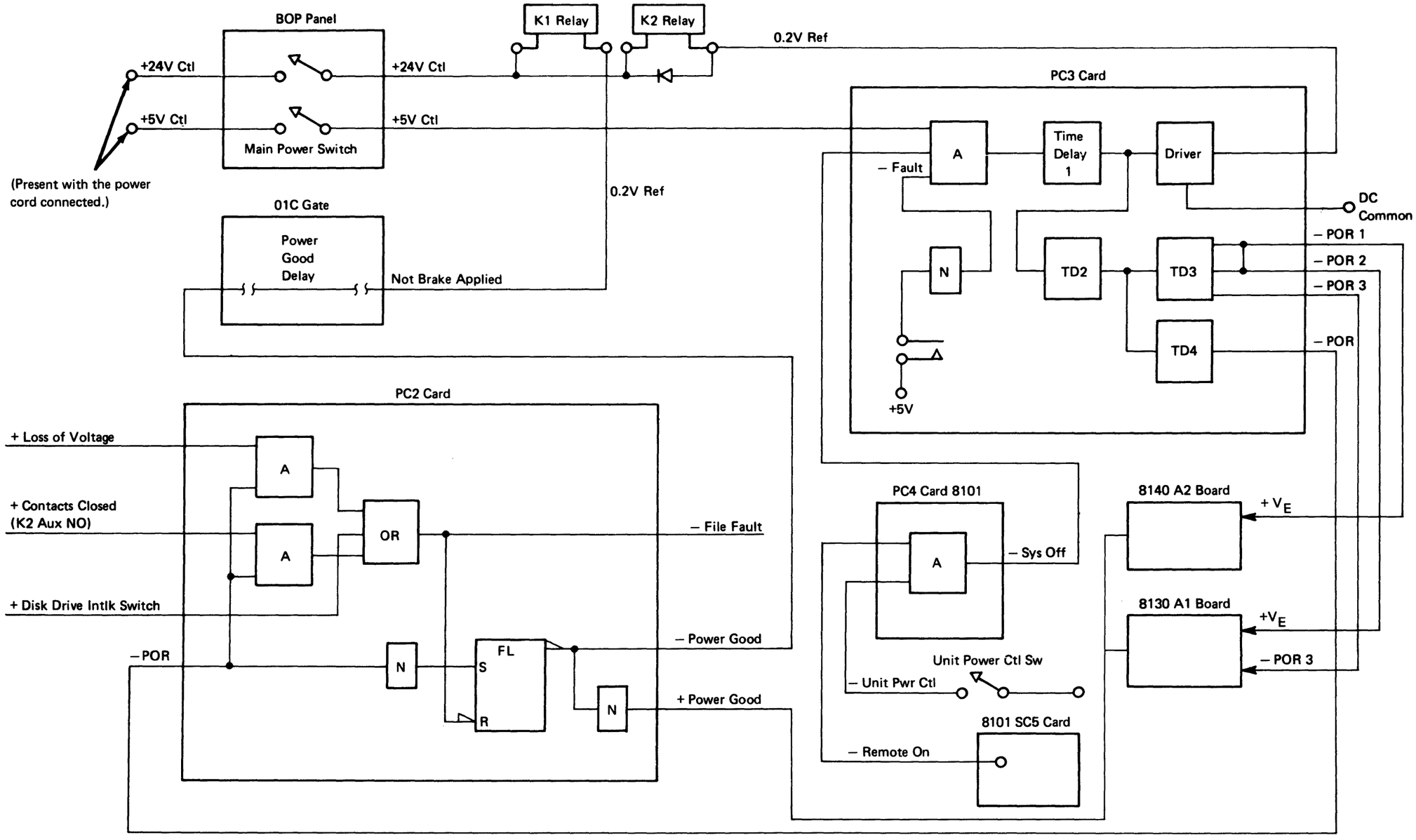
1. Set the 8101 power control switch to Remote.
2. The main power switch should be set to the On position (▮) on all of the attached 8101s.
3. Set the 8130/8140 power switch to the Power On position (▮).
4. The system control facility (SCF) will then send a turn-on signal to each 8101 in a timed sequence.

If the 8130/8140 system is inoperable, an 8101 may be powered up by first setting the unit power control switch to Local and then set the 8101 power switch to On (▮).



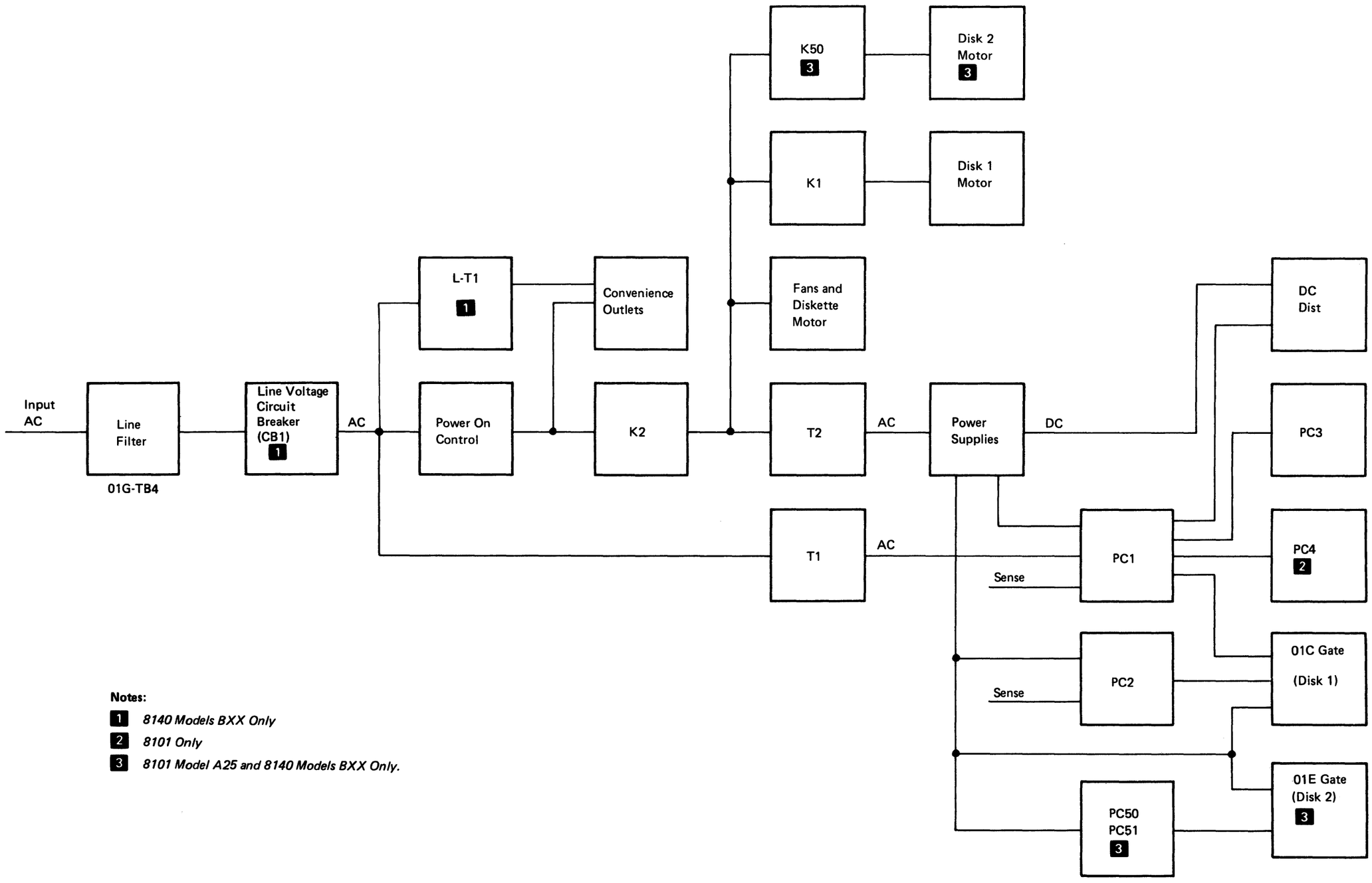

**Note:** ***The disk determines the timing relationship between the Power Good and Brake On/Off signal.***

**Figure PA120-1. Power On/Off Sequence Timing**




**Note:** *For more detail see individual components; for machine with two disks, see PA400.*

**Figure PA120-2. Basic Power-On Logic for Machines with One Disk Drive**



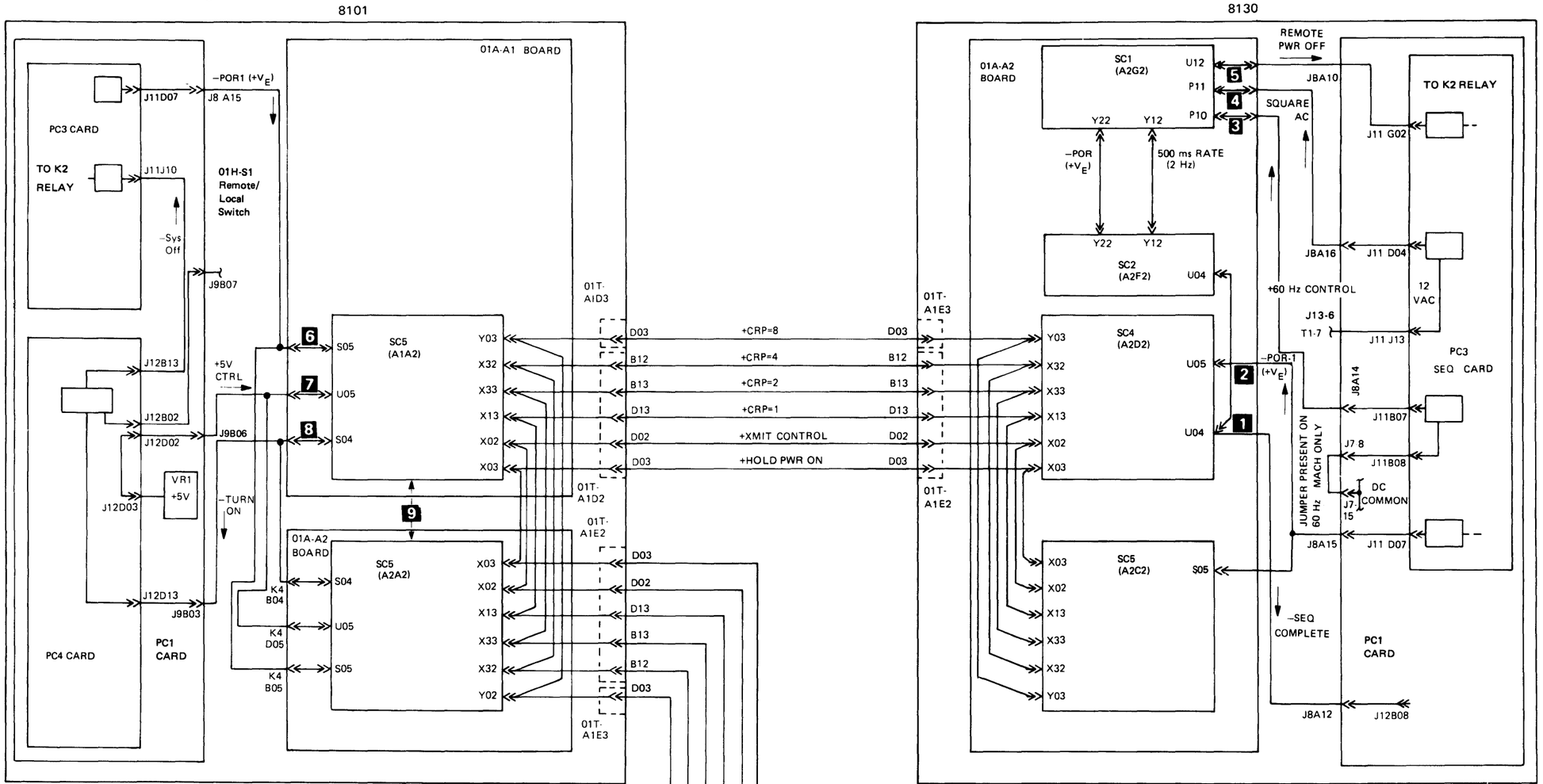

**Notes:**

1. *8140 Models BXX Only*
2. *8101 Only*
3. *8101 Model A25 and 8140 Models BXX Only.*

**Figure PA120-3. Basic Power Distribution**

*PA121 PSCF Power Control Logic*

**8130 PSCF Power Control Logic**

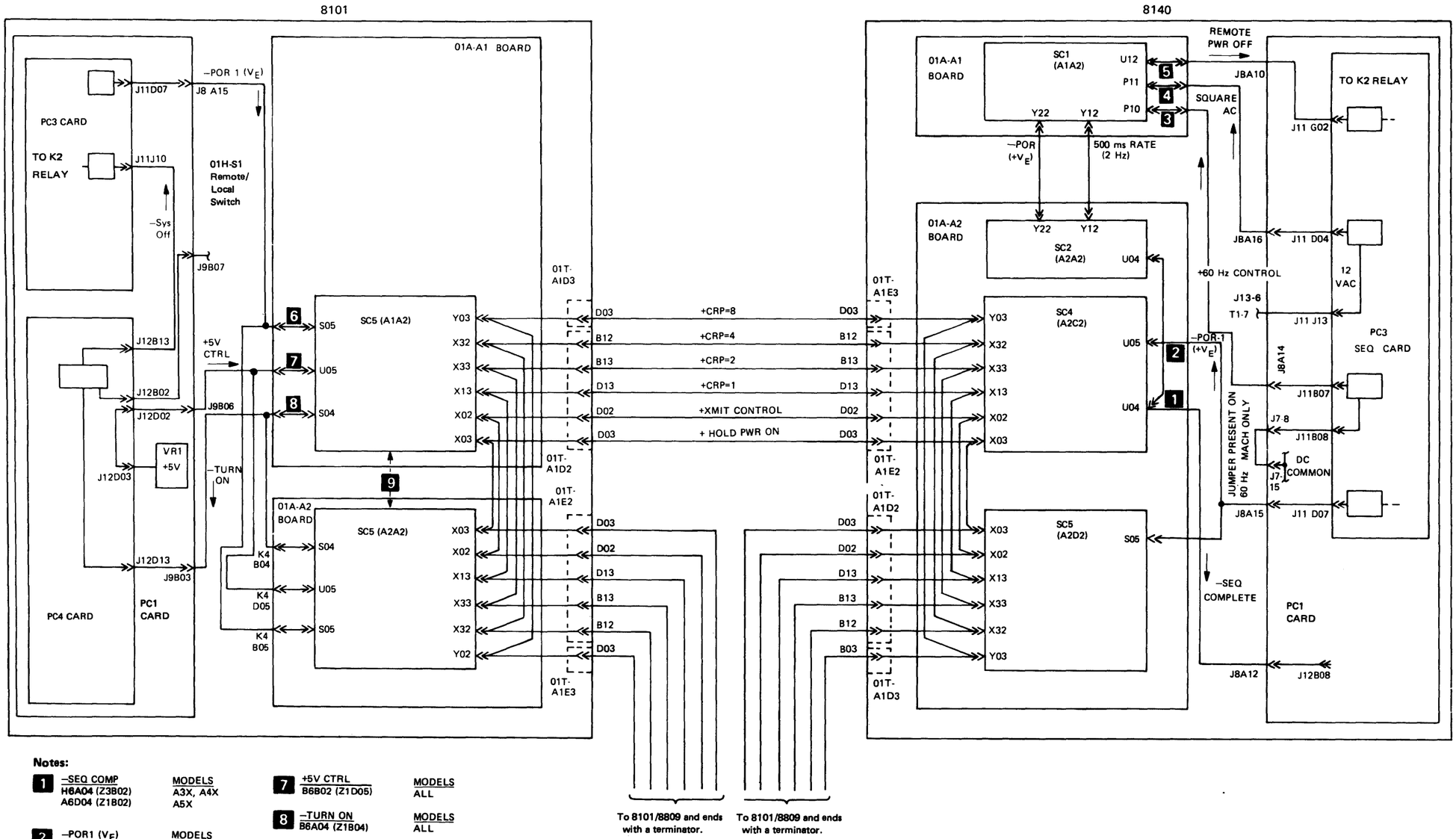



To 8101/8809 and ends with a terminator.

**Notes:**

1. -SEQ COMP — H6A04 (Z3B02), A6D04 (Z1B02) — MODELS A3X, A4X, A5X, A2X
2. -POR1 (+$V_E$) — H6B04 (Z3B03), A6E04 (Z1B03) — MODELS A3X,A4X, A5X, A2X
3. +60 HZ CONTROL — A6D02 (Z1D02) — MODELS ALL
4. SQUARE AC — A6D04 (Z1B02) — MODELS ALL
5. -REMOTE PWR OFF — A6E04 (Z1B03) — MODELS ALL
6. -POR1(+$V_E$) — B6B04 (Z1B05) — MODELS ALL
7. +5V CTRL — B6B02 (Z1D05) — MODELS ALL
8. -TURN ON — B6A04 (Z1B04) — MODELS ALL
9. 8101-01A-A1 and 01A-A2 are feature boards.

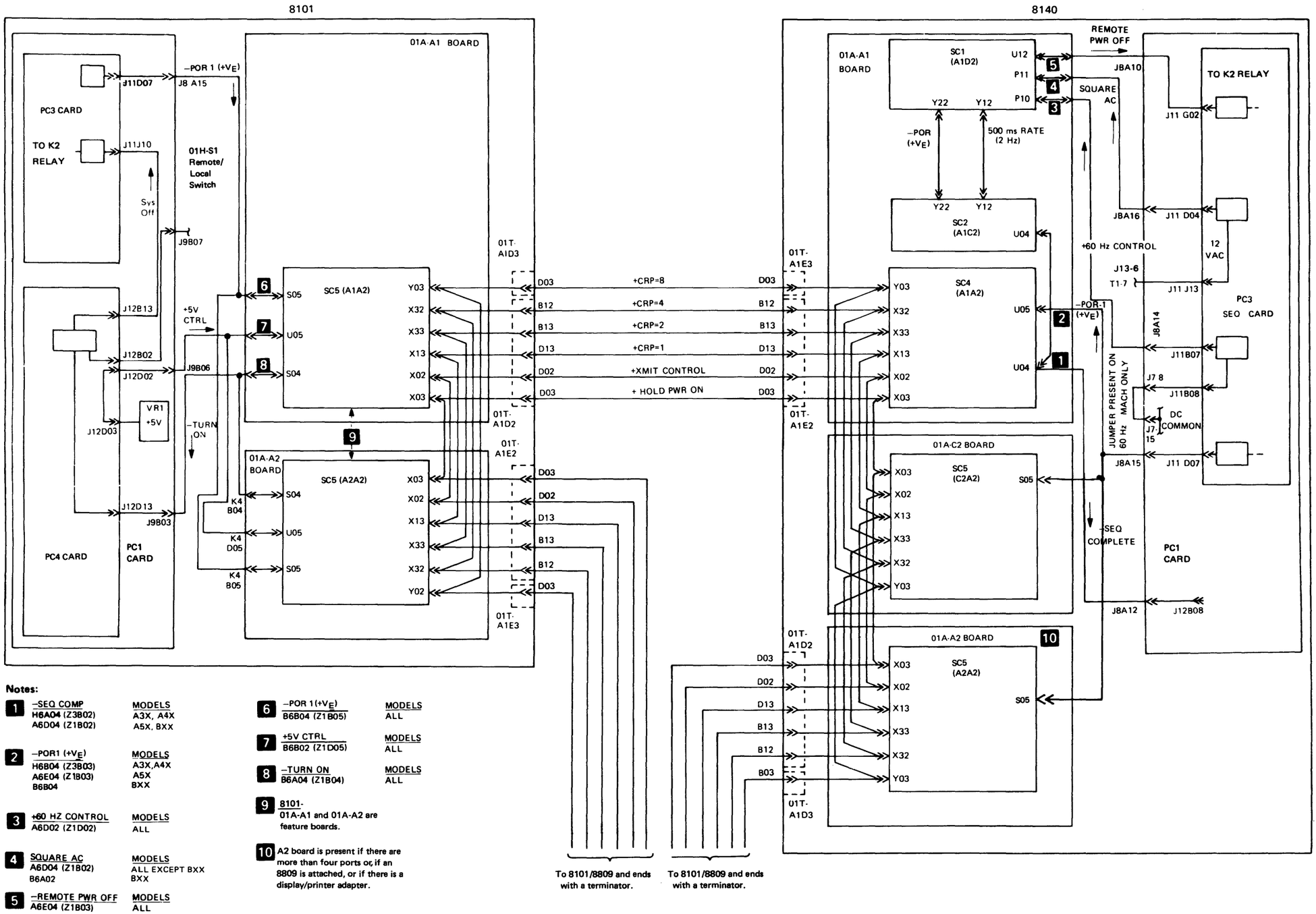
## 8140 Models AXX PSCF Power Control Logic




**Notes:**

1. –SEQ COMP — H6A04 (Z3B02), A6D04 (Z1B02) — MODELS A3X, A4X, A5X
2. –POR1 ($V_E$) — H6B04 (Z3B03), A6E04 (Z1B03), E6A04 (Z2B03) — MODELS A3X,A4X, A5X, A6X, A7X
3. +60 HZ CONTROL — A6D02 (Z1D02) — MODELS ALL
4. SQUARE AC — A6D04 (Z1B02) — MODELS ALL
5. –REMOTE PWR OFF — A6E04 (Z1B03) — MODELS ALL
6. –POR1 ($+V_E$) — B6B04 (Z1B05) — MODELS ALL
7. +5V CTRL — B6B02 (Z1D05) — MODELS ALL
8. –TURN ON — B6A04 (Z1B04) — MODELS ALL
9. 8101- 01A-A1 and 01A-A2 are feature boards.

## 8140 Models BXX PSCF Power Control Logic




**Notes:**

1. -SEQ COMP — H6A04 (Z3B02), A6D04 (Z1B02) — MODELS A3X, A4X, A5X, BXX
2. -POR1 (+VE) — H6B04 (Z3B03), A6E04 (Z1B03), B6B04 — MODELS A3X, A4X, A5X, BXX
3. +60 HZ CONTROL — A6D02 (Z1D02) — MODELS ALL
4. SQUARE AC — A6D04 (Z1B02), B6A02 — MODELS ALL EXCEPT BXX, BXX
5. -REMOTE PWR OFF — A6E04 (Z1B03) — MODELS ALL
6. -POR 1(+VE) — B6B04 (Z1B05) — MODELS ALL
7. +5V CTRL — B6B02 (Z1D05) — MODELS ALL
8. -TURN ON — B6A04 (Z1B04) — MODELS ALL
9. 8101-01A-A1 and 01A-A2 are feature boards.
10. A2 board is present if there are more than four ports or if an 8809 is attached, or if there is a display/printer adapter.

*PA122 Not Used*

*PA123 Attached 8101 Power-On Control*

A +5V control level (+5 Ctl) must be available at each 8101 as a prerequisite to power up. This voltage is required by the power control logic in each device and is furnished by the 8101 power supply (see PA440).

**Note:** *When the 8130 with the System Expansion Feature or the 8140 is powered up, only the Power On indicator on the 8130/8140 operator panel is valid during the power-on signal sequence (approximately 73 seconds). All other indicators and hexadecimal displays are INVALID. This is because the 8130/8140 is held in a system-reset state until the 8101 unit power-on sequence is complete, at which time the IPL process begins.*

**Sequence Control**

When the 8130/8140 is powered on, +5V Ctl is generated and 250 ms later –POR1 ($+V_E$) becomes active. The 8101 power-on signal sequencing starts when –POR1 ($+V_E$) becomes active. The 8130/8140 remains in a system-reset state until the power-on-signal sequence is complete. In the PSCF –POR1 ($V_E$) is sent to PSCF cards 2, 3, and 5 which control power-on signal sequencing. When the operation is complete –POR1 ($V_E$) is sent to the PSCF1 card which controls initialization reset functions.

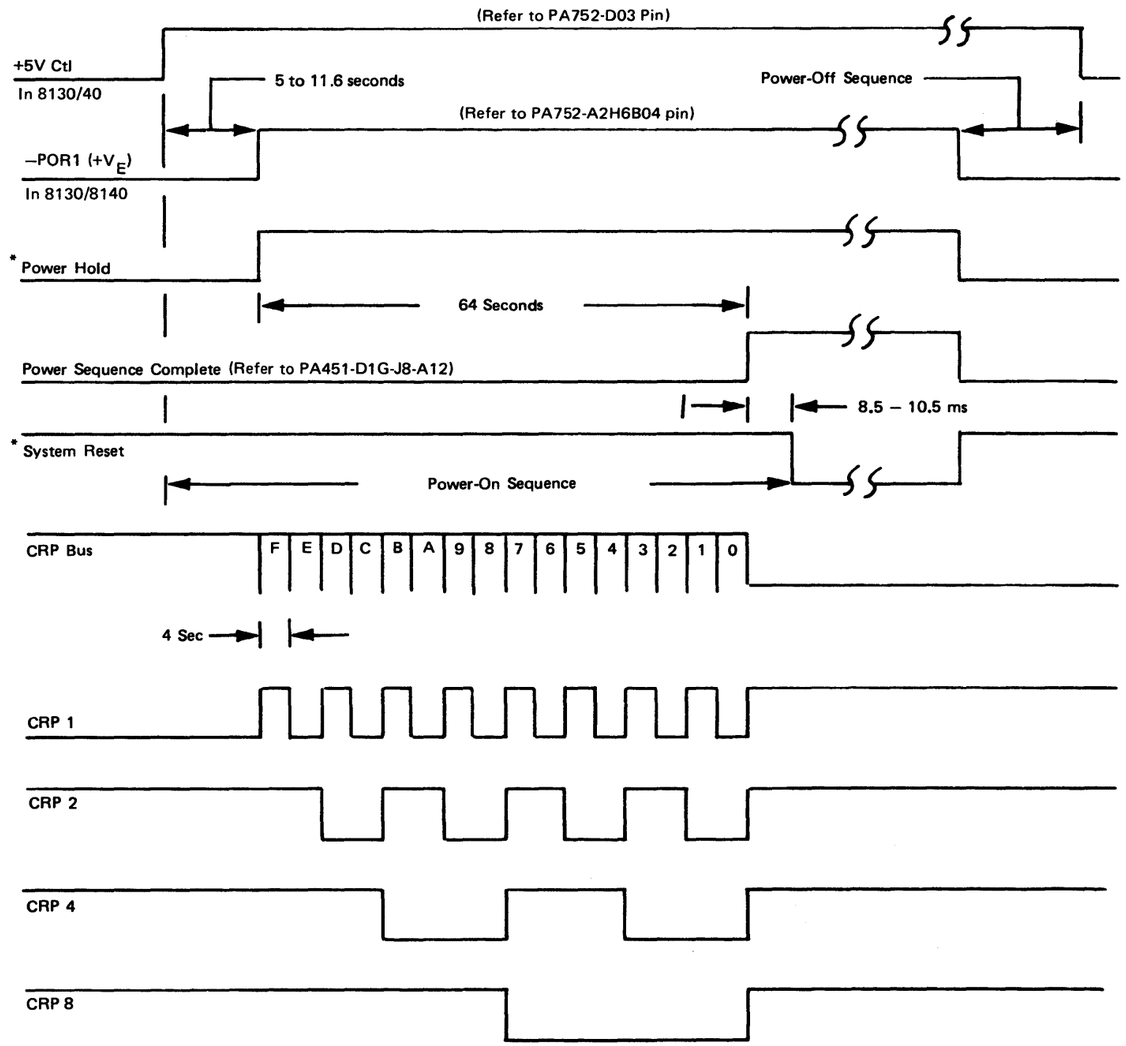
The PSCF and SSCF –POR1 ($+V_E$), together with +5V ctl, control the POR signal.

Primarily, –POR1 ($+V_E$) becomes active 5.2 to 11.6 seconds after the power switch is activated and provides the gating for the I/O drivers to ensure a noise-free environment when the drivers are turned on or off. The –POR1 ($+V_E$) in both the PSCF and SSCF is deactivated before +5V Ctl, which generates a POR. This causes the I/O drivers to turn off before the loss of +5V Ctl.

8101 power-on signal sequencing is controlled by the PSCF using the channel request logic in the SSCFs, the channel request priority (CRP) bus between the PSCF and SSCFs, and the Transmit Control (Xmit Ctrl) line. When an SSCF is powered down, the Transmit Control line enables a comparison between its predetermined CRP value and the contents of the CRP bus. When the contents of the CRP bus are equal to or less than the SSCF's CRP value, the "sequence on" signal is activated.

The sequence in which the units are optioned to power up is determined by their CRP assignment. The unit with the highest CRP assignment is activated first, followed by the remaining units in descending order of CRP assignment. The PSCF controls this sequencing by using the 4-bit power-up sequence counter as the source for the value it places on the CRP bus. The counter is first reset and then set to a value of B'1111' at the time the 8130/8140 is powered up. The PSCF places the value B'1111' on the CRP bus and raises the Transmit Control line. At that time, all SSCFs compare their CRP value with the value B'1111' on the CRP bus. If an SSCF is assigned the CRP value B'1111', the unit to which it is attached is powered on. The PSCF waits 4 seconds, decrements the counter by 1, places the new value on the CRP bus, and raises the Transmit Control line. Again all SSCFs compare the CRP bus with their predetermined CRP value, and, if a comparison is made, the unit to which that SSCF is attached is powered up. This sequence continues until the counter value overflows from being decremented past the value B'0000'. At this time, all attached 8101 units, with their power control switch set to Remote, are powered up and the PSCF returns a Sequence Complete signal to the processor power control logic to show that the 8101 power-on signal sequencing is complete.

Figure PA123-1 shows the timings for the power-on signal sequence for the attached 8101 units. The 8130/8140 +5VCC signal initiates this sequence




*SCF signals. Refer to the Chapter 5 SC section for the complete SCF power sequence.

**Figure PA123-1. 8101 Unit Power-On Signal Sequence Timings**

## *PA124 DC Overvoltage and Undervoltage Sensing*

The 8100 power logic monitors certain dc voltages for overvoltage (OV) and undervoltage (UV) conditions and, if detected, performs a machine power off. Refer to the following text and also to Figure PA124-1 to determine those machine voltages sensed for OV/UV conditions, and also for those dc voltages not sensed.

### Overvoltage Sensing

The 8100 senses only the -4V dc for an overvoltage condition. The PC-2 and PC-50 logic cards generate and sense this voltage; PC-2 supplies the first disk drive and PC-50 supplies the second (if installed). When PC-2 or PC-50 detects a -4V dc overvoltage after power is applied to the regulator, the PC card logic turns on a silicon-controlled rectifier (SCR) to remove the overvoltage. This condition opens fuse F14 (F50 on PC-50), which drops the —4V dc and powers down the machine.

### Undervoltage Sensing

The PC-2, PC-3, and PC-50 cards sense undervoltage conditions as follows:

- PC-2 senses the -4, -12, one +5, +12, and +24 dc voltages at the load side of the fuse that corresponds to the voltage. (See Figure PA124-1). When PC-2 (PA462) detects an undervoltage condition for any of these voltages at any time except during a power-on or power-off operation, it:
  - Powers down the machine
  - Turns on the disk storage fault indicator (DS4)
  - Turns on the Power/Thermal indicator (DS3)
  - Generates a machine turn-off signal
- PC-3 senses the -5V dc voltage at 01A-TB1-8 for an 8130 (PA441 and PA451), at 01A-TB2-3 for an 8140 Model AXX and at 01A-TB2-7 for Model BXX (Figure PA440-3 and PA442 and PA452) and at 01A-TB2-3 for an 8101 (PA443 and PA453). When PC-3 detects a -5V undervoltage condition at any time (PA463) except during a power-on or power-off operation, it drops machine power.
- PC-50 senses the -4V dc for the second disk drive (if installed). When this PC card detects a -4V undervoltage condition, it powers down the machine and turns on its disk storage fault indicator (DS50).

| DC Voltage | OV | UV | Sensed By | Fused By | Comments |
|---|---|---|---|---|---|
| -4 | X | X | PC-2 | 01G-F14 | 1st disk drive |
| **-4 | X | X | PC-2 | 01M-F14 | 8140 1st disk drive |
| -4 | X | X | PC-50 | 01N-F50 | 8140 2nd disk drive |
| -4 | X | X | PC-50 | 01G-F50 | 8101 2nd disk drive |
| +5 | — | X | PC-2 | 01G-F3 | |
| +5 | — | — | -------- | 01G-F4 | Not sensed |
| +5 | — | — | -------- | 01G-F5 | Not sensed |
| +5 | — | — | -------- | 01G-F6 | Not sensed |
| ** +5 | — | — | -------- | 01R-F1 | Not sensed |
| ** +5 | — | — | -------- | 01R-F2 | Not sensed |
| ** +5 | — | — | -------- | 01R-F3 | Not sensed |
| * -5 | — | X | PC-3 | 01G-F8 | |
| -8.5 | — | — | -------- | 01G-F7 | Not sensed |
| +8.5 | — | — | -------- | 01G-F2 | Not sensed |
| -12 | — | X | PC-2 | 01G-F1 | |
| +12 | — | X | PC-2 | 01G-F10 | |
| +24 | — | X | PC-2 | 01G-F9 | |

*An 8101 Model A10 (no disk drive) senses only this voltage.
**Present only on 8140 Models BXX.

**Figure PA124-1. DC Overvoltage/Undervoltage Sensing Summary**

Figure PA124-1 shows all 8100 dc voltages and if they are sensed for either OV or UV conditions. It also shows the PC card that senses these voltages, which occurs at the load (output) side of the respective fuse. Refer to PA660 for a list of all system voltages, fusing, and test points.

## PA130 Power-Unique Repair Strategy

Access to power components and test points normally requires removal of exterior covers over the area being checked.

You should perform all initial 8100 power fault isolation by using the maintenance device and the power (PA) MAPs located on MD diskette 01.

- Use MD diskette 01 menu option 4 either for 8130/8140 power problems or if you cannot determine the failing machine type.
- Use MD diskette 01 menu option 5 if you know an 8101 failed but cannot determine which one.

Always have the maintenance device plugged into the 8130/8140 01H gate convenience outlet unless you have either:

- disconnected or plan to disconnect the power cord.
- turned off the line voltage circuit breaker (CB1) on 8140 Models BXX.
- otherwise have no 01H gate convenience outlet power because of a machine problem.

PA211 describes the PA MAP menu options and their meanings used for 8130, 8140, and undetermined power problem isolation; PA212 describes the PA MAP menu options available for an 8101.

When using PA211 or PA212, find the symptom meaning that most closely describes your failure and select the corresponding PA MAP option. If you isolate the problem to a field-replaceable unit (FRU), repair or exchange the FRU; for a problem other than a defective FRU, repair as necessary; if you cannot determine the problem, request aid.

If the Chapter 1 General Failure Index (GFI) directed you to the PA MAP, use MD diskette 01 menu option 4 or 5 as explained above. The PA MAP then directs you to either:

- Exchange a FRU.
- Locate opens by checking circuit continuity.
- Locate shorts by unloading particular circuits.
- Locate power control failures.
- Verify correct power supply operation.

Intermittent failures make all MAPs ineffective. If either an intermittent power problem occurs or the PA MAP cannot isolate the failure, go to PA300.

## PA200 Offline Tests

To perform initial power problem fault isolation, you must obtain the entire system from the customer. As the PA MAPs are standalone programs and do not require system interaction, you do not need to plug the MD signal cable into the 8130/8140 01H gate socket. You should, however, plug the MD power cable into an 01H gate convenience outlet if power is available there. (See note after PA211 options). Power on the MD, load MD diskette 01, and use:

- MD diskette 01 menu option 4 either for 8130/8140 power problems or if you cannot determine the failing machine type.
- MD diskette 01 menu option 5 for 8101 power problems.

### PA210 PA MAP Menu Options

*PA211 PA MAP Options for 8130, 8140, and Undetermined Power Problems*

The following lists and briefly describes the PA MAP options, symptoms, and meanings used for MD diskette 01 menu option 4. To use these options, find the symptom meaning that most closely describes your failure, then select the corresponding PA MAP option and symptom as displayed on the MD. If none of the meanings apply or you cannot determine the symptom, select option 09, UNKNOWN PROBLEM.

If you isolate the problem to a field-replaceable unit (FRU), repair or exchange the FRU; for a problem other than a defective FRU, repair as necessary; if you cannot determine the problem, request aid.

| PA MAP Menu Option | Symptom | Meaning |
|---|---|---|
| 01 | SOUND; NO LIGHTS | After a power-up, fans and motors run but no indicators are on. |
| 02 | NO POWER-UP INDICATION | After attempting a power-up, no fans or motors run and all indicators are off. |
| 03 | VOLTAGE OUT OF TOLERANCE | Voltage measurements indicate that one or more voltages are low. |
| 04 | 1 VOLTAGE MISSING AT LOAD POINT | You have determined that a voltage is missing either at the 01A gate, a disk drive, the diskette drive, or a fan. |
| 05 | DISKETTE DRIVE MOTOR | You know or suspect that a diskette drive motor problem exists. |
| 06 | DISK DRIVE MOTOR | You know or suspect that a disk drive motor problem exists. The disk storage fault indicator on PC-2 or PC-50 (if installed) could be on. |
| 07 | FAN NOT RUNNING | One or more fans do not run. |
| 08 | POWER/THERMAL CHECK | The Power/Thermal Check indicator is on and the system does not power up. |
| 09 | UNKNOWN PROBLEM | Use this option to begin PA MAP fault isolation if you cannot determine a symptom. |
| 10 | OPEN FUSE | You have exchanged a fuse and want to verify the repair. If the fuse again opens, the PA MAP provides fault isolation. |
| *11 | CUSTOMER CB TRIPS | The customer's line voltage CB trips either when connecting the power cord or when powering up. |
| *12 | 8130/8140 AC OUTLET | No ac voltage at the 8130/8140 convenience outlet(s). |
| 13 | EXIT POWER MAP | Returns you to the MD diskette 01 menu. |
| 14 | POWER ON DISABLED | The Power On Disabled indicator is on and the system does not power up. |
| 15 | MENU OPTIONS | Displays the PA MAP menu options. |

*You cannot plug the MD into the 8130/8140 convenience outlet when selecting this option, as the outlet has no power.

*PA212 PA MAP Options for 8101 Power Problems*

The following lists and briefly describes the PA MAP options, symptoms, and meanings used for MD diskette 01 menu option 5.

- If the symptom meaning describes your failure, select the corresponding PA MAP option and symptom as displayed on the MD.
- If none of the meanings apply or you cannot determine the symptom, select option 0C, POWER PROBLEM.
- For any 8101 symptom not listed, use MD diskette 01 option 4 and go to PA211.

**Note:** *If a MAP step asks you to check a voltage that does not apply or an indicator that is not installed, reply as if the voltage or indicator were installed and good.*

If you isolate the problem to a field-replaceable unit (FRU), repair or exchange the FRU; for a problem other than a defective FRU, repair as necessary; if you cannot determine the problem, request aid.

| PA MAP Menu Option | Symptom | Meaning |
|---|---|---|
| 0C | POWER PROBLEM | Isolates a system power problem to a particular 8101. |
| 0D | SCF POWER SIGNALS | An 8101 operates with the local/remote switch set to Local but not when set to Remote. |

## PA250 Action Plans

Use the information in this section to aid in fault isolation of solid power failures. For intermittent power problems, refer to PA300.

### *PA251 Possible Causes of Failure — General*

- If all voltages appear momentarily but the 8130/8140/8101 does not power up, the PC-3 card could be defective.
- If the 8130/8140/8101 operates normally with the disk storage sensing logic disabled and fails when connected, the PC-2 sensing circuits could be defective.

### *PA252 Possible Causes of Failure Using the Status of 8101 Fuses and Indicators*

Use the status of the following fuses and indicators to determine possible causes of power failures.

| Fuse/Indicator | Status | Possible Cause |
|---|---|---|
| F14 or F50<br>Power/Thermal Check<br>DS4 (on PC-2)<br>and/or<br>DS50 (on PC-50) | Open<br>On<br><br>On | −4V undervoltage |
| F14 or F50<br>Power/Thermal Check<br>DS4 (on PC-2)<br>and/or<br>DS50 (on PC-50) | Good<br>On<br><br>On | • Disk drive interlock switch open<br>• Undervoltage condition on one or more dc voltages (+5, +12, +24, −4, −12) |
| Power/Thermal Check<br>DS4 (on PC-2)<br>DS50 (on PC-50) | On<br>Off<br>Off | • −5V undervoltage condition at the gate<br>• Power-up failed due to an open gate thermal |
| DS51 (on PC-51) | On | 01E gate disk brake active |
| Any dc fuse | Open | • Overcurrent condition due to circuit overload (PA650)<br>• Undervoltage condition |
| Any ac fuse | Open | • Overcurrent condition<br>• Wrong tap connected to 01G-T1 or T2 transformer primary (PA410-PA430) |
| All indicators | On | Open ground condition |
| All indicators | Off | • Missing line voltage<br>• Open ac circuit (PA410-PA430)<br>• Defective SSCF (SC5) card<br>• Remote on signal missing<br>• Line circuit breaker (CB1) tripped (8140 Models BXX only) |

### *PA253 PC-2/PC-3/01C Disk Drive Power Fault Isolation*

If PC-2, PC-3, or the 01C disk drive appears to cause a power on failure, use the following procedure to aid in fault isolation. See also PA450 through PA453 and PA460 through PA462.

Providing the disk storage fault indicator (DS-4) is on, disconnect J16/P16 on PC-2 and also disconnect the power plug (01C-J11/P11) to the 01C disk drive motor.

- If power remains on, either a PC-2 input or the PC-2 card caused the fault indication. Use Figure PA253-1.
- If the machine does not power up, either a PC-3 input or output caused the problem. Use Figure PA253-2 and PA453.

Figure PA253-1 describes the voltages expected at certain PC-2 J16 pins before and after a power up attempt.

| J16 Pin | Voltage Before | Voltage After | Comments |
|---|---|---|---|
| A03 | 0 | +24* | |
| A05 | 0 | +12* | |
| A06 | 0 | +5* | |
| A07 | 0 | -4* | |
| B12 | 0 | -12* | |
| A12 | 0 | 0 | |
| A10 | 0 | 0 | +5V after power up if the disk storage interlock switch or switch path is open. |
| A01 | 0 | +24* | +24V path through the K2 relay indicating that the relay is picked. (PA440) |
| B07 | 0 | +3.5 | Approximately 3.5V if the -POR signal is coming from PC-3 G10. (PA452, PA461, and PA462) |
| B11 | 0 | +5 | -Sw Off signal. (PA450, PA461, and PA463) |
| A11 | +5 | +5 | This point is also called -POR but comes from PC-3 G07 and indicates +24V ac from the T1 transformer. (PA461, PA463, PA410, and PA440) |
| B06 | +5 | +5 | Disk Storage (File) Fault signal from PC-2 to PC-3. If measured when the fault occurs, the meter deflects lower, then returns to +5V. |
| B09 | 0 | 0 | -Power Good signal to the disk drive logic that allows the K1 relay to pick, which starts the disk drive motor. During power up, this signal is +2V to +3V. |
| B08 | 0 | +5 | +Power Good signal to the 01A gate and the SCF logic. |

*If power remains up.

**Figure PA253-1. PC-2 J16 Input/Output Levels**

Figure PA253-2 shows the signal path of certain PC-3 power reset lines used to determine fault isolation when using this action plan.

| Line Name | PC-3 Pin | PC-1 Pin | PC-2 Pin | 01A Pin | Disk Pin |
|---|---|---|---|---|---|
| −POR 1 | D07 | J8A15 | − | J12-3 | − |
| −POR 2 | D13 | J8B09 | − | J16-3 | − |
| −POR 3 | B09 | J8B10 | − | J16-6 | − |
| −POR* | G05 | J1A01 | J16A11 | − | − |
| −POR | G10 | J1A06 | J16B07,<br>J16B09 | | 01C J1-3 |
| −Sw Off | G07 | J1A03 | J16B11 | | |

**Figure PA253-2. PC-3 Power Reset Line Distribution**

## PA300 Intermittent Failure Repair Strategy

Use the information in this section to aid in fault isolation of either intermittent power problems or for those failures that the PA MAP could not isolate.

### PA310 General Intermittent Failure Repair Strategy

Use the following general procedure to aid in isolating intermittent power failures:

1. Turn off machine power at the operator panel and either disconnect the power cord from the wall outlet on all 8130 and 8140 Models AXX, or turn off the line voltage circuit breaker (CB1) on 8140 Models BXX.
2. Disconnect all P/J connectors one at a time and inspect for cracked housings and loose or bent pins. Reconnect them if not defective, or repair or replace as necessary. See PA760 for connector part numbers.
3. Reseat all pluggable cards in the power supply gate(s) and all 01A logic gate cards.
4. Check all TBs and filter capacitors for loose screws.
5. Check power cables for possible chafing or pinching.
6. Check power cables and connections for opens or shorts.
7. Either connect the power cord to the wall outlet or turn on CB1 (8140 models BXX).

**DANGER**
**With the power cord connected to the wall outlet, line voltage and the +5 and +24 control voltages are always present in all:**

- **8130s, 8140 Models AXX, and 8101s.**
- **8140 Models BXX with the line voltage circuit breaker (CB1) on.**

8. Turn on machine power at the operator panel and check relay contactors for proper operation.
9. When powered up, vibrate the machine while visually checking for arcing or smoking.
10. Go to PA610 and perform the AC Ripple Service Check.
11. Check for extra or missing ac (PA405) and dc (PA440) grounds.

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## PA400 Signal Paths and Detailed Operational Description

**DANGER**
**With the power cord connected to the wall outlet, line voltage and the +5 and +24 control voltages are always present in all:**

- **8130s, 8140 Models AXX, and 8101s.**
- **8140 Models BXX with the line voltage circuit breaker (CB1) on.**

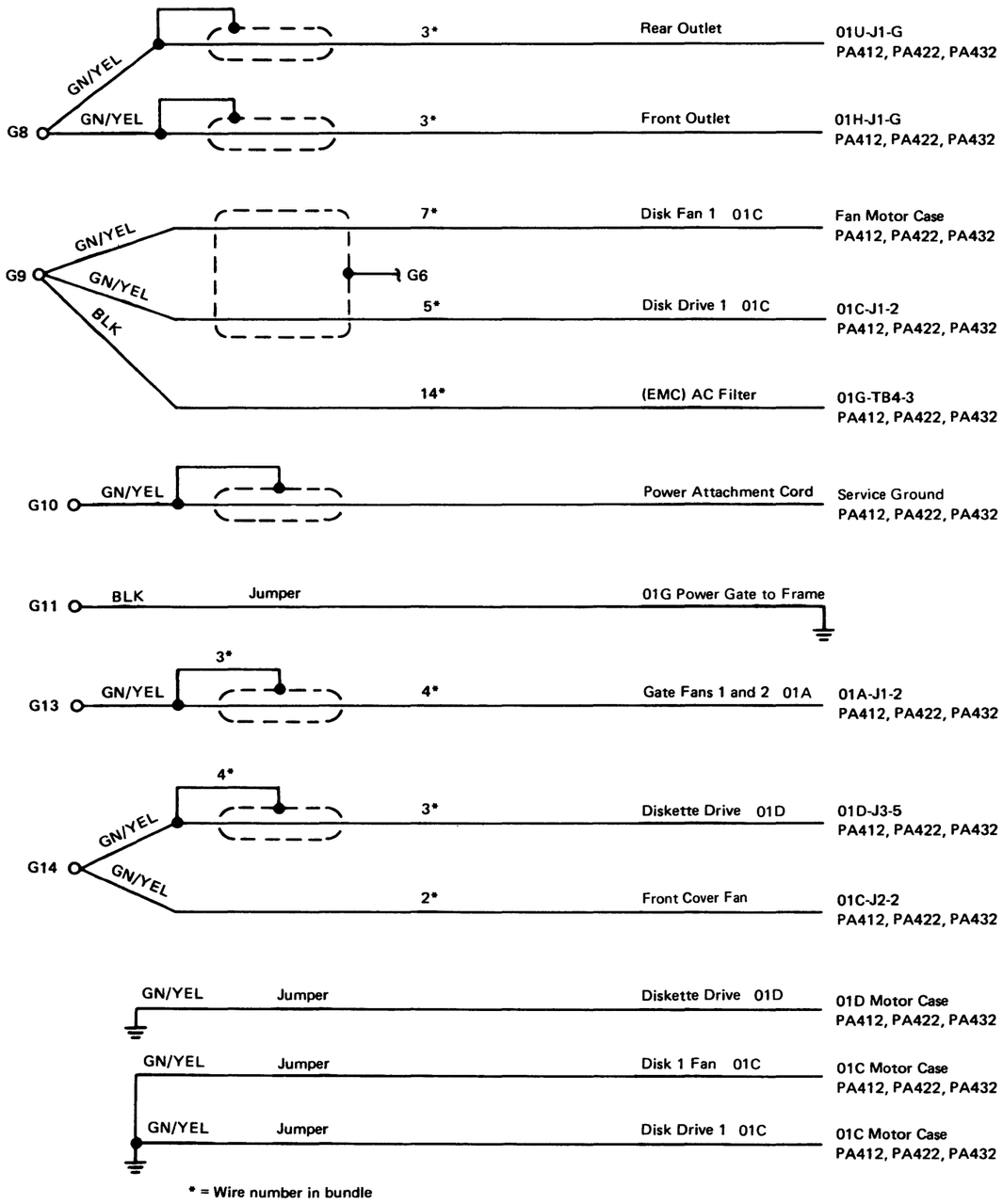
The following summarizes PA400, the first five sections of which are grouped according to machine type, where:

X = 1 = 8130
X = 2 = 8140
X = 3 = 8101

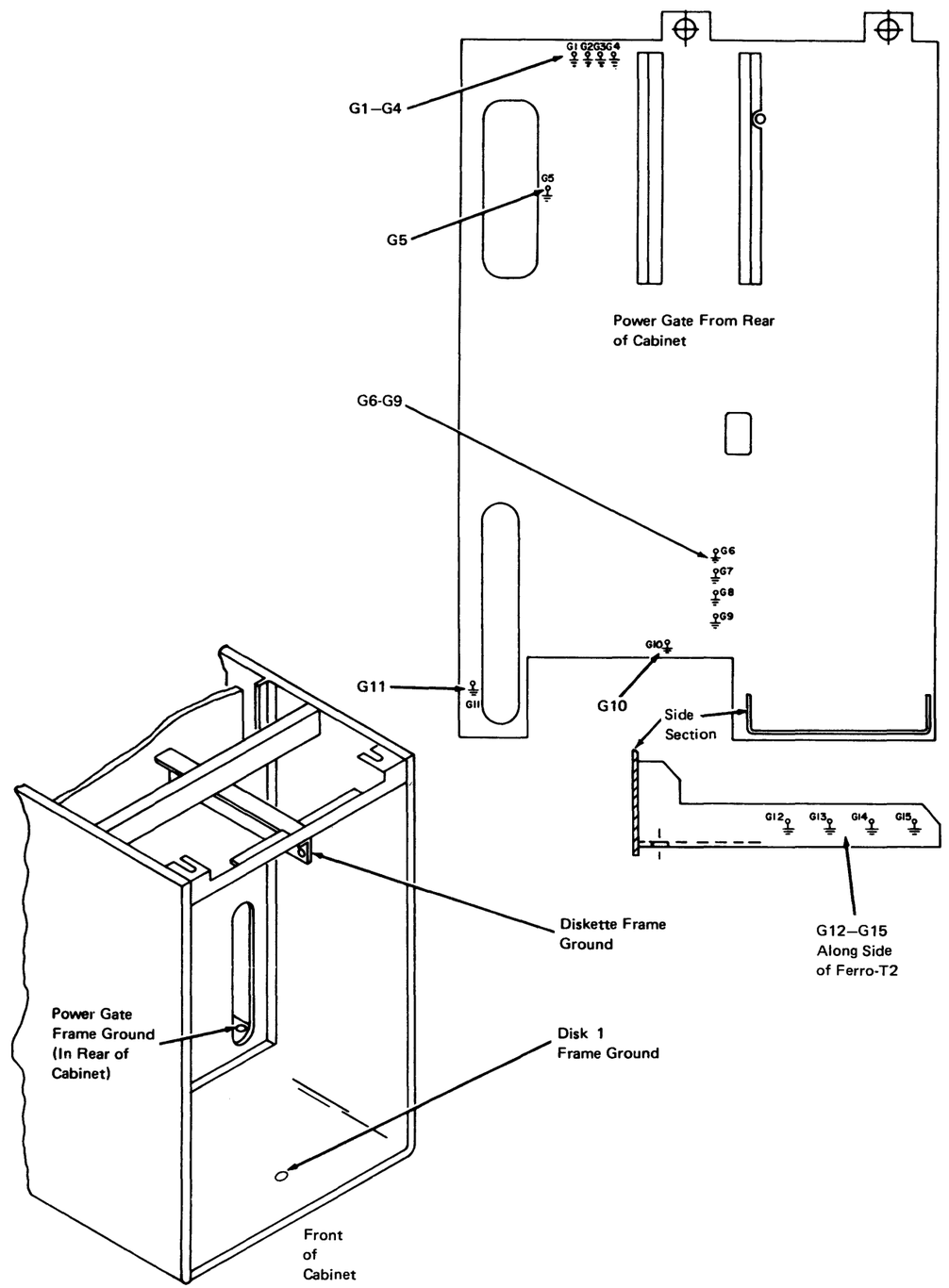
- PA41X contains the 60-Hz ac power logic for machines used in the United States and Canada.
- PA42X contains the 60-Hz ac power logic for machines used in countries other than the United States and Canada.
- PA43X contains the 50-Hz ac power logic.
- PA44X contains the dc power logic.
- PA45X contains the power control (PC) card external logic connections.
- PA460 contains PC card diagrams and internal logic connections sectionalized by PC card type.

*PA405 Safety Grounds*

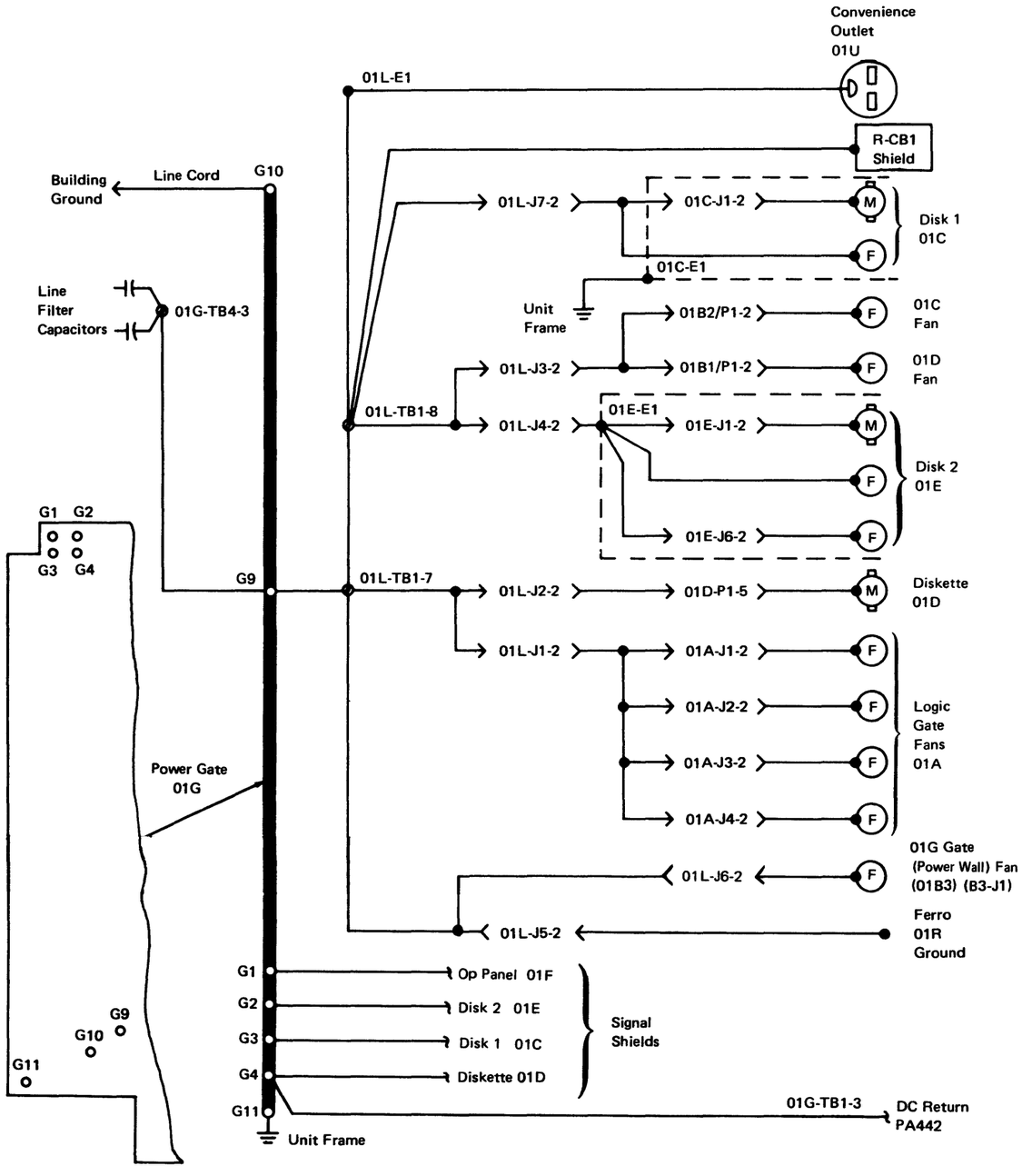
**8130/8140 Models AXX Safety Grounds**



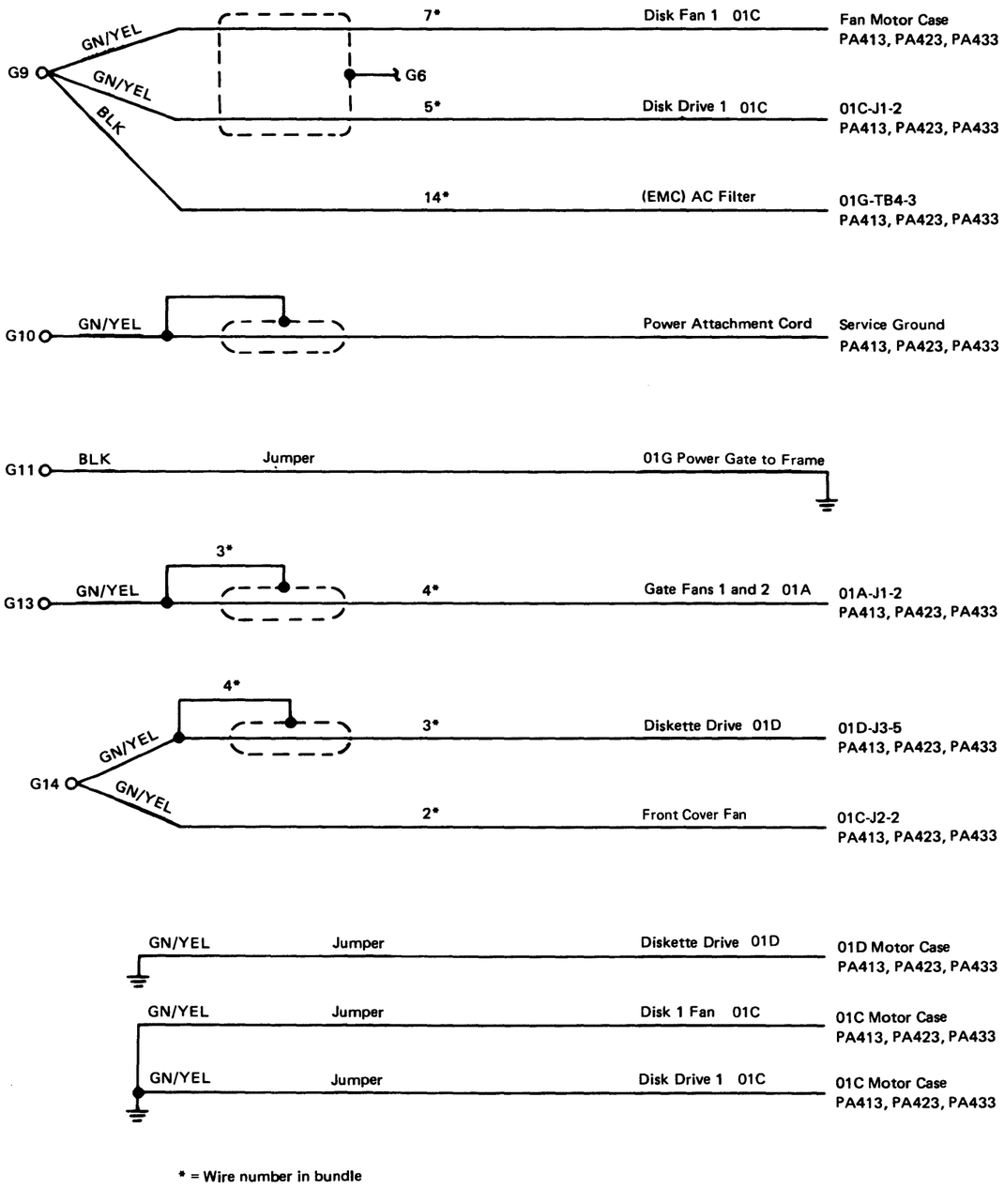

* = Wire number in bundle



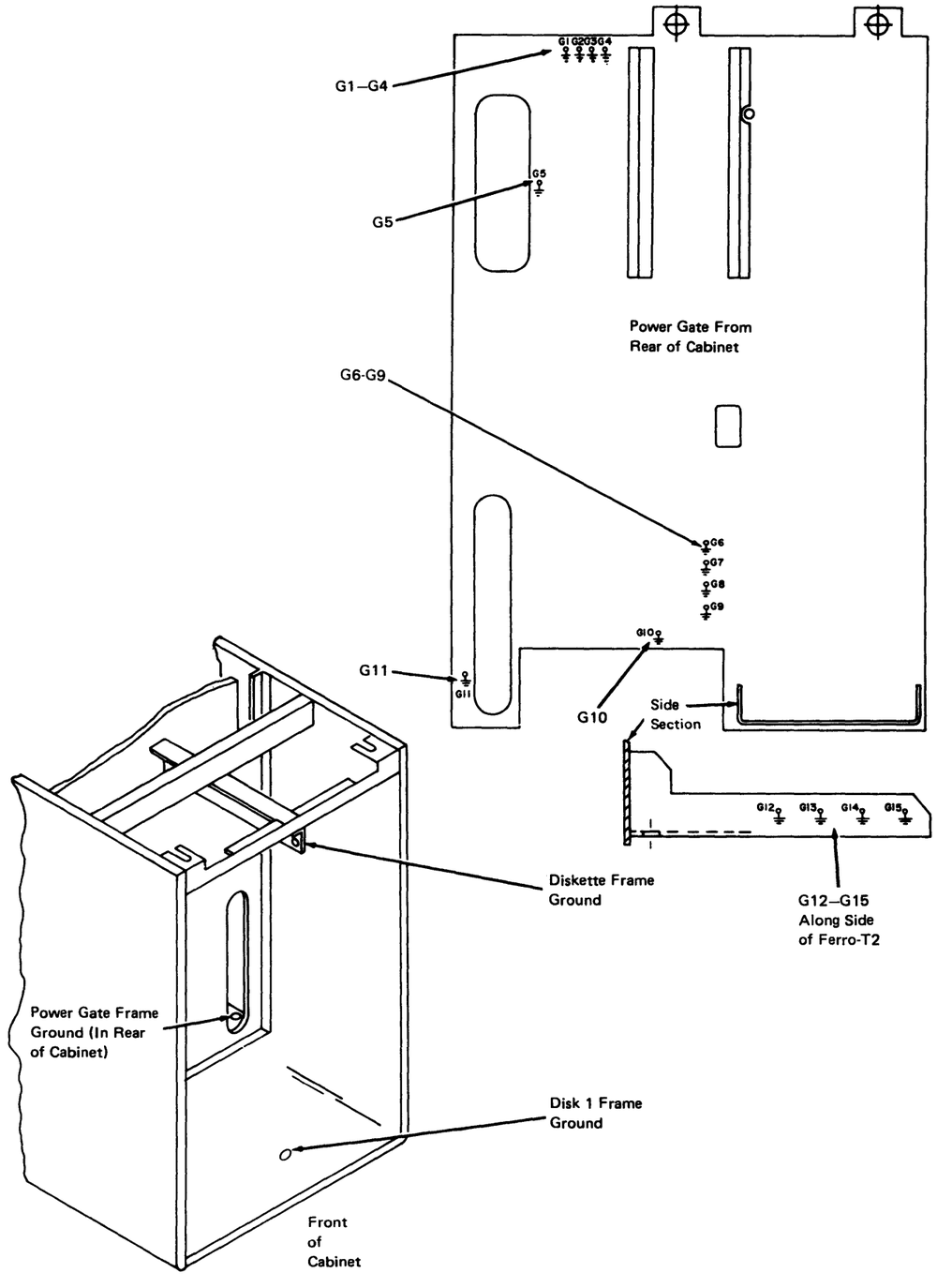
**8140 Models BXX Safety Grounds**



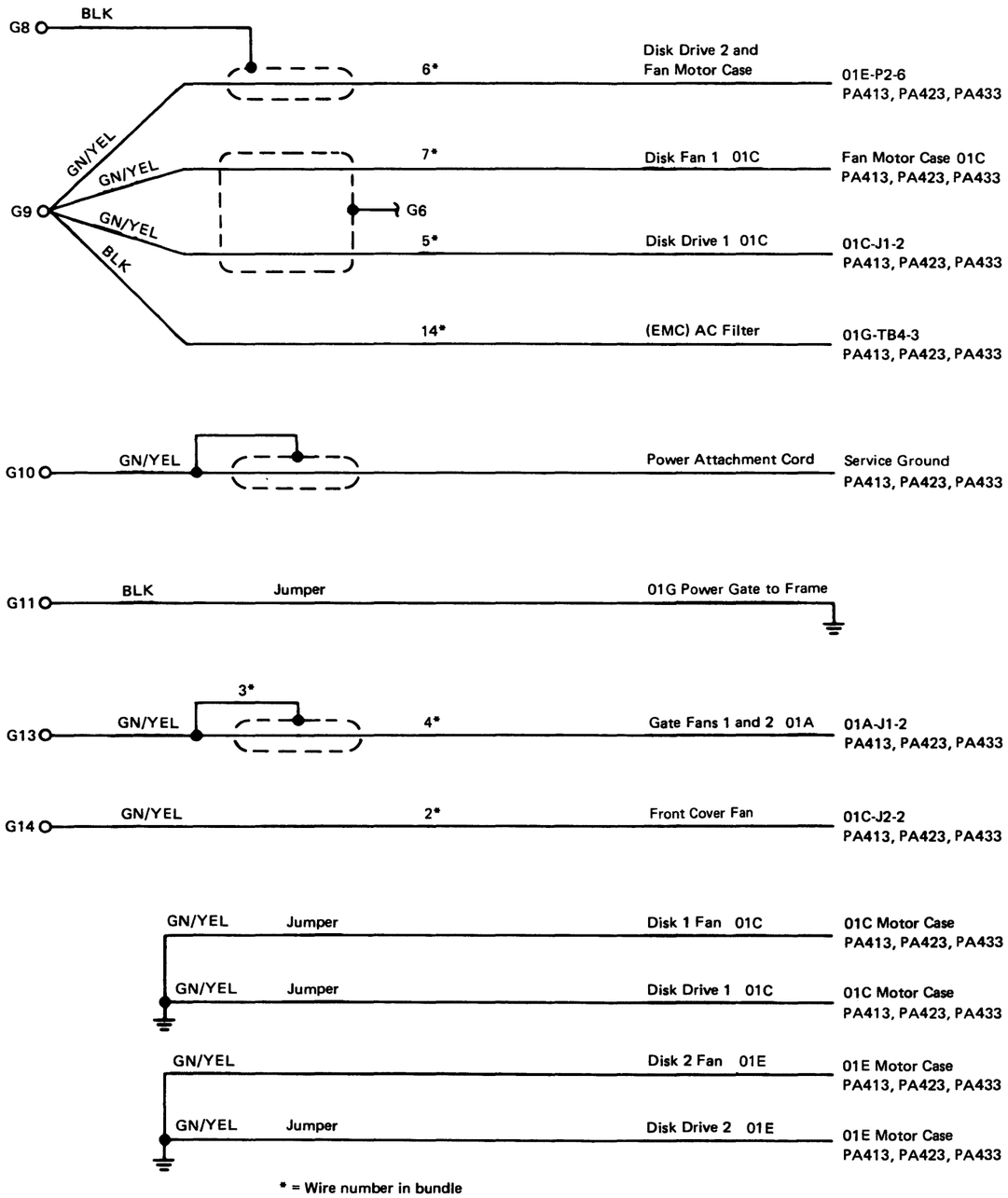
**8101 Models A1X, A20, and A23 Safety Grounds**



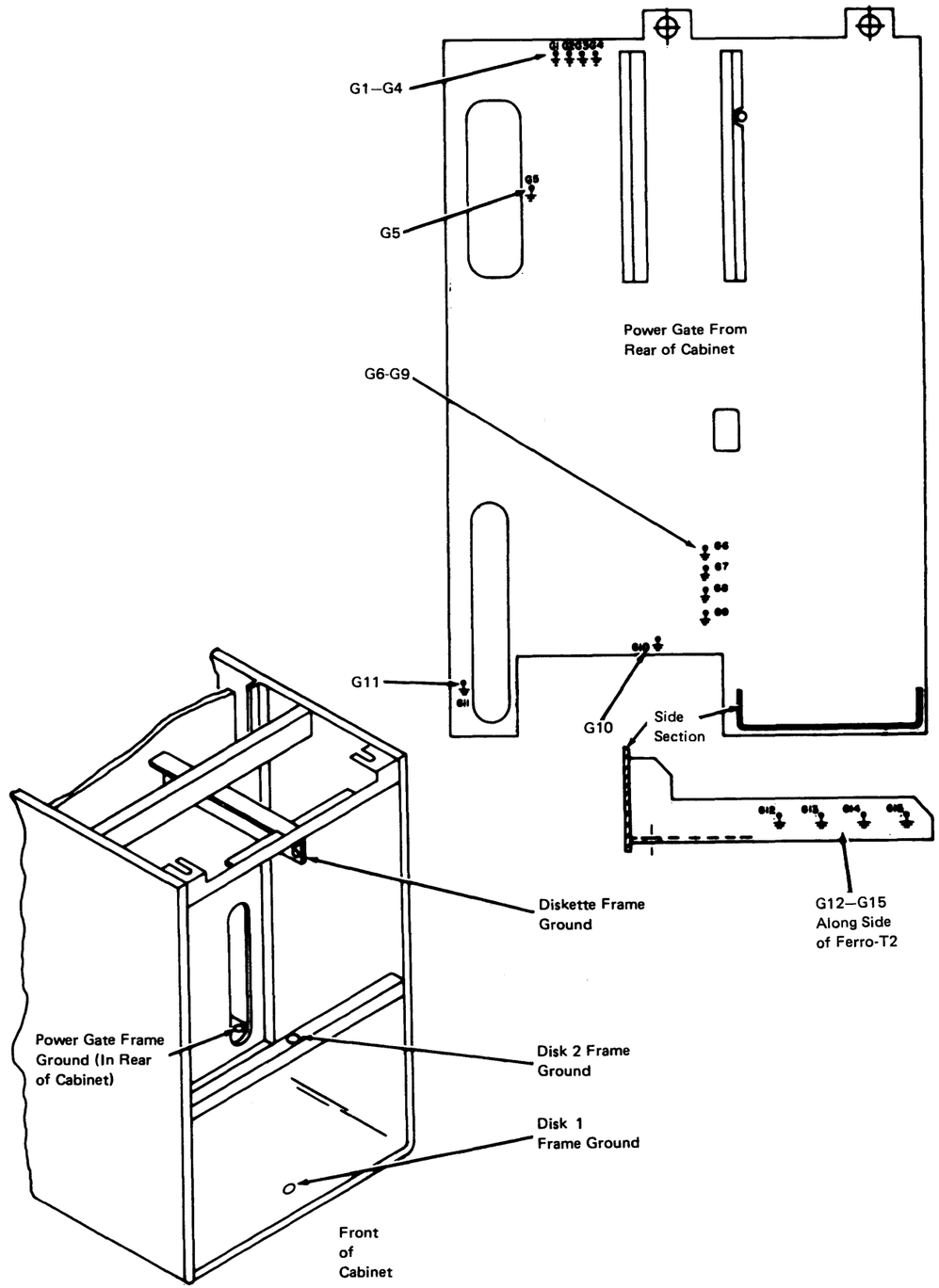

* = Wire number in bundle



**8101 Model A25 Safety Grounds**

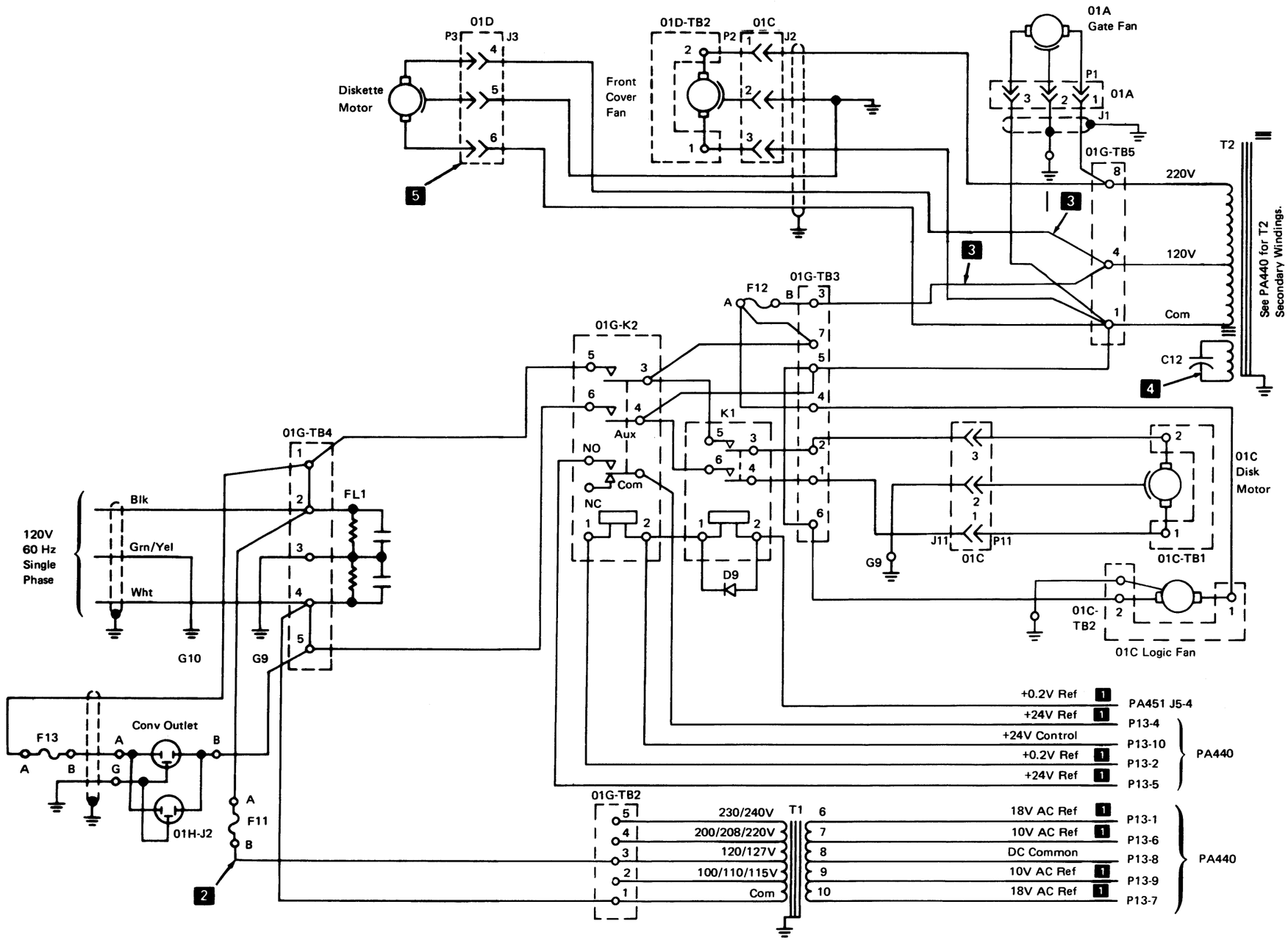



* = Wire number in bundle



**PA410 60-Hz AC Power (U.S. and Canada)**

*PA411 8130 60-Hz AC Power (U.S. and Canada)*

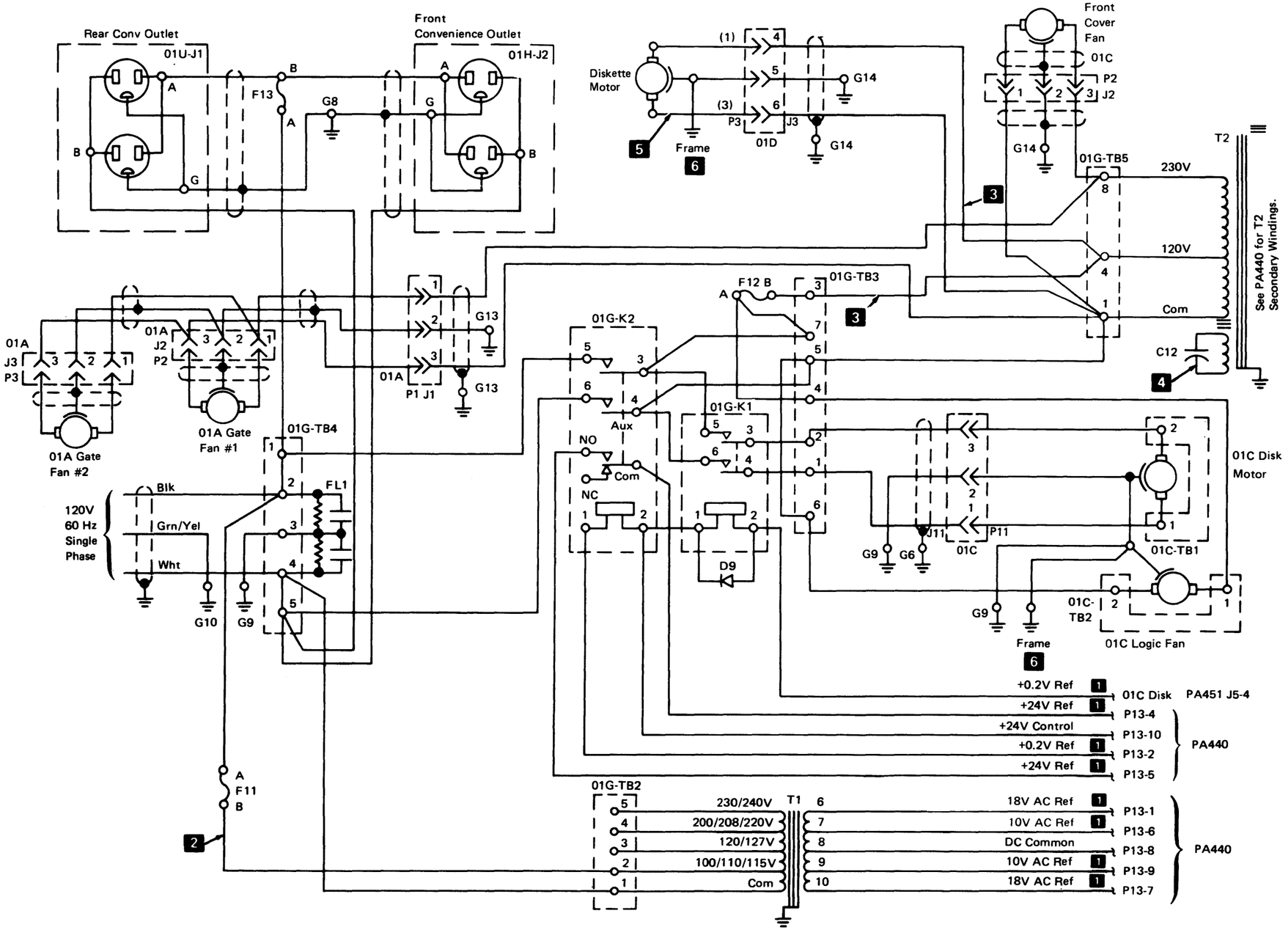



**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Leads in P3 and J3 are connected to pins 4, 5, and 6 for 100 to 127 volts and to pins 1, 5, and 3 for 200 to 240 volts. See also Note 3.*

*PA412 8140 60-Hz AC Power (U.S. and Canada)*

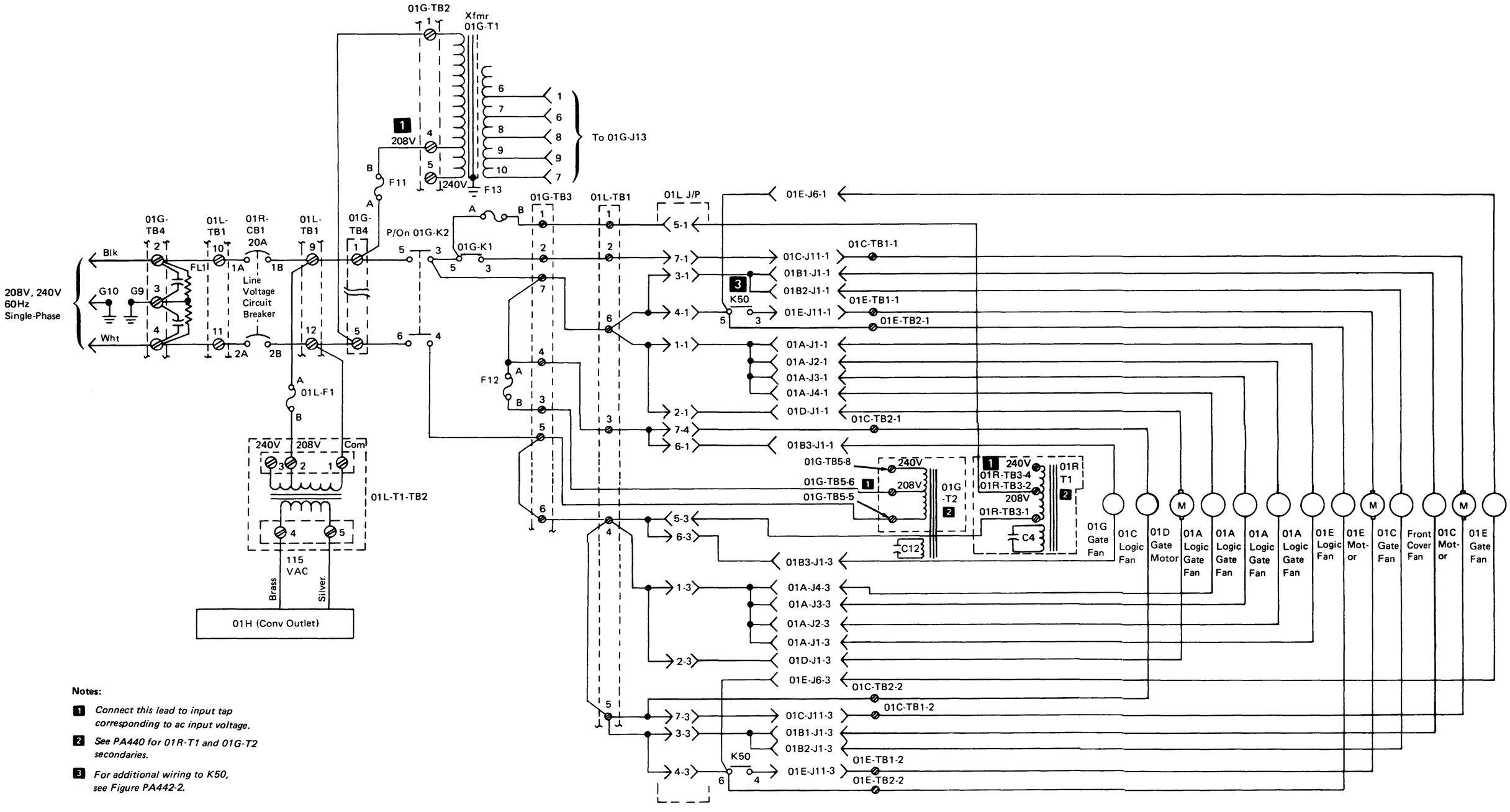
**8140 Models AXX 60-Hz AC Power (U.S. and Canada)**




**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Leads in P3 and J3 are connected to pins 4, 5, and 6 for 100 to 127 volts and to pins 1, 5, and 3 for 200 to 240 volts. See also Note 3.*
6. *All units built after EC 862592 have disk and diskette double-grounded.*

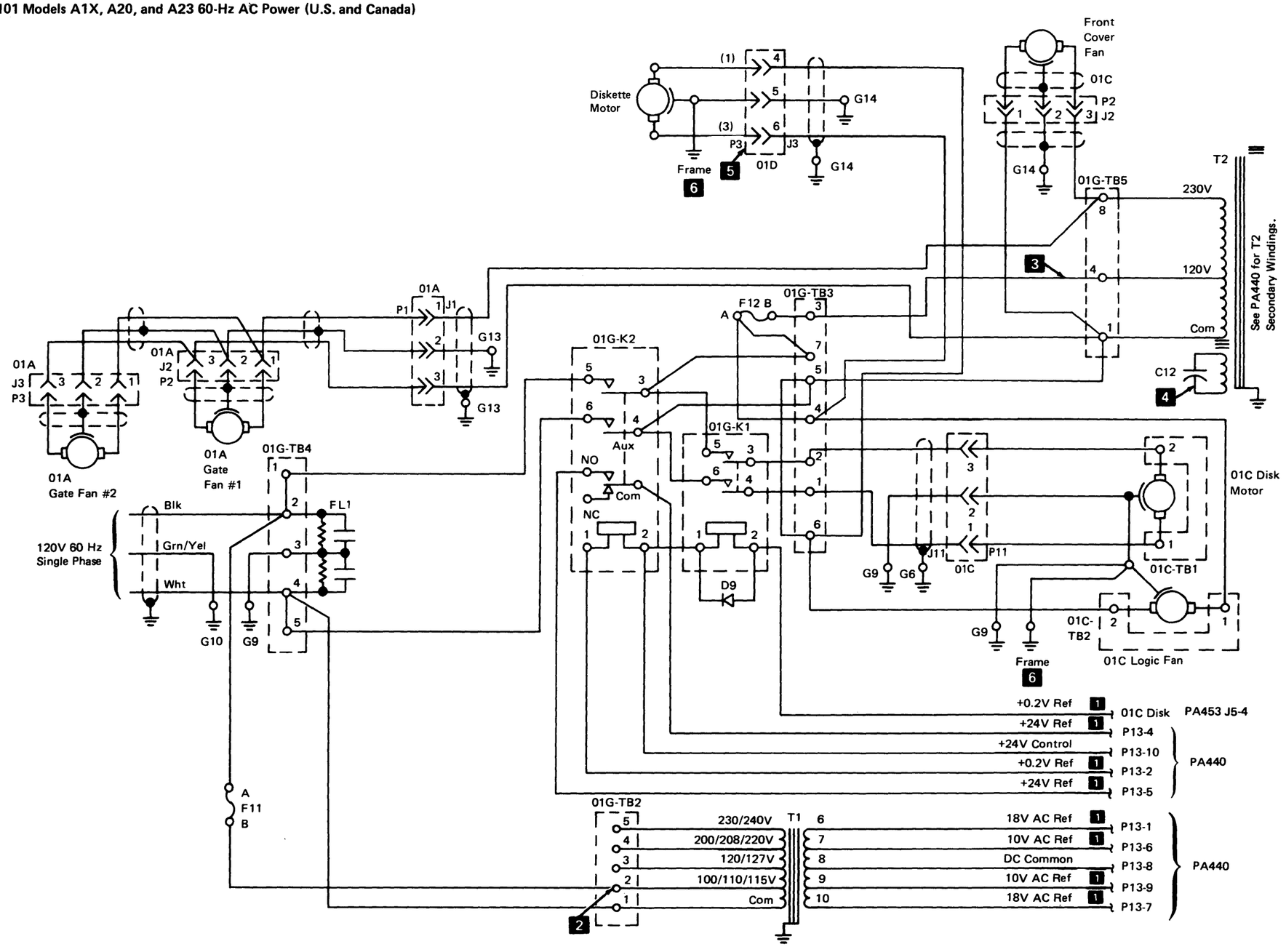
8140 Models BXX 60-Hz AC Power (U.S. and Canada)




**Notes:**

1. *Connect this lead to input tap corresponding to ac input voltage.*
2. *See PA440 for 01R-T1 and 01G-T2 secondaries.*
3. *For additional wiring to K50, see Figure PA442-2.*

**8101 Models A1X, A20, and A23 60-Hz AC Power (U.S. and Canada)**

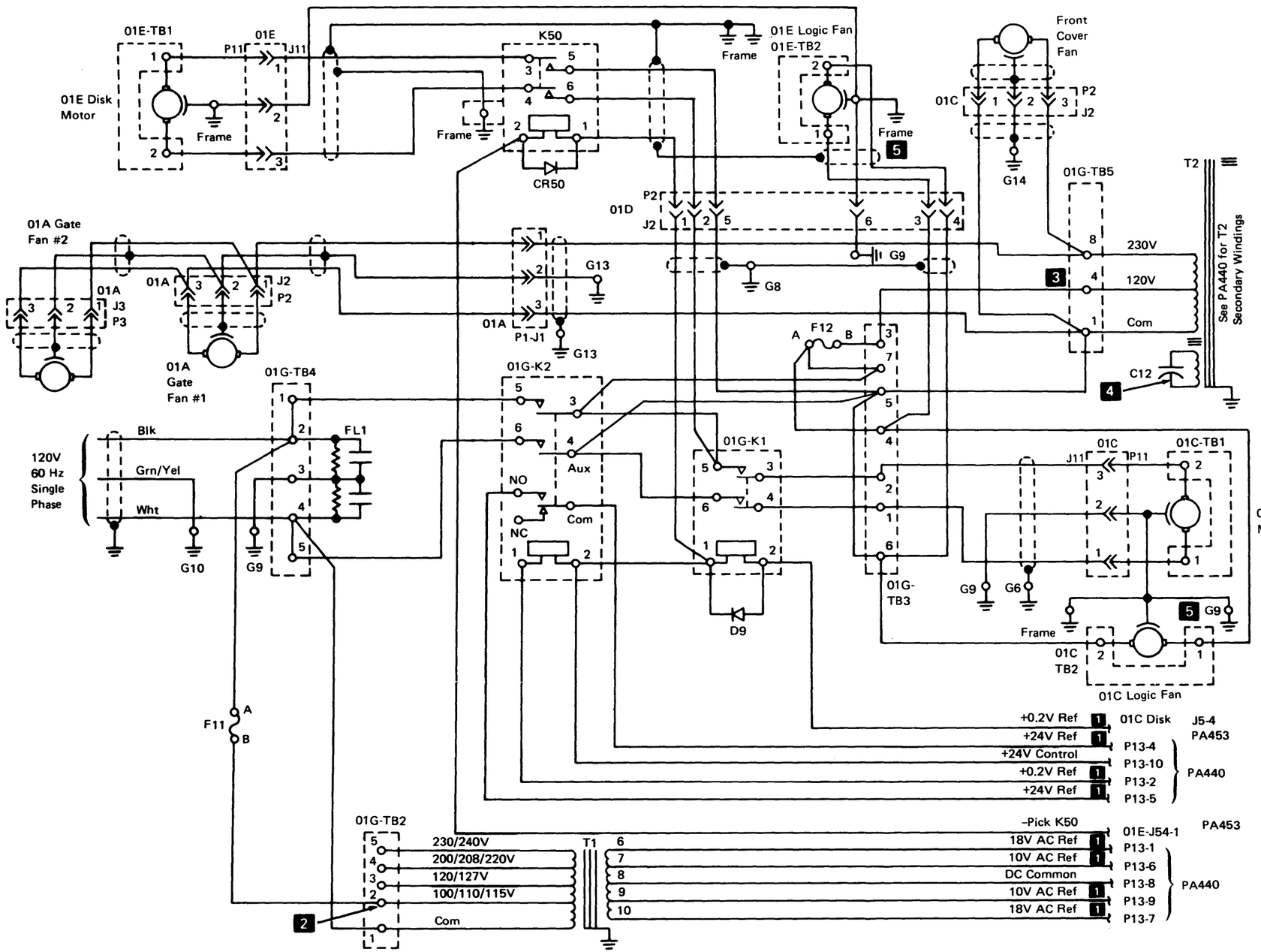



**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Leads in P3 and J3 are connected to pins 4, 5, and 6 for 100 to 127 volts and to pins 1, 5, and 3 for 200 to 240 volts. See also Note 3*
6. *All units built after EC 862592 have disk and diskette double-grounded.*

**REA 06-88481**
**SY27-2521-3**

**8101 Model A25 60-Hz AC Power (U. S. and Canada)**

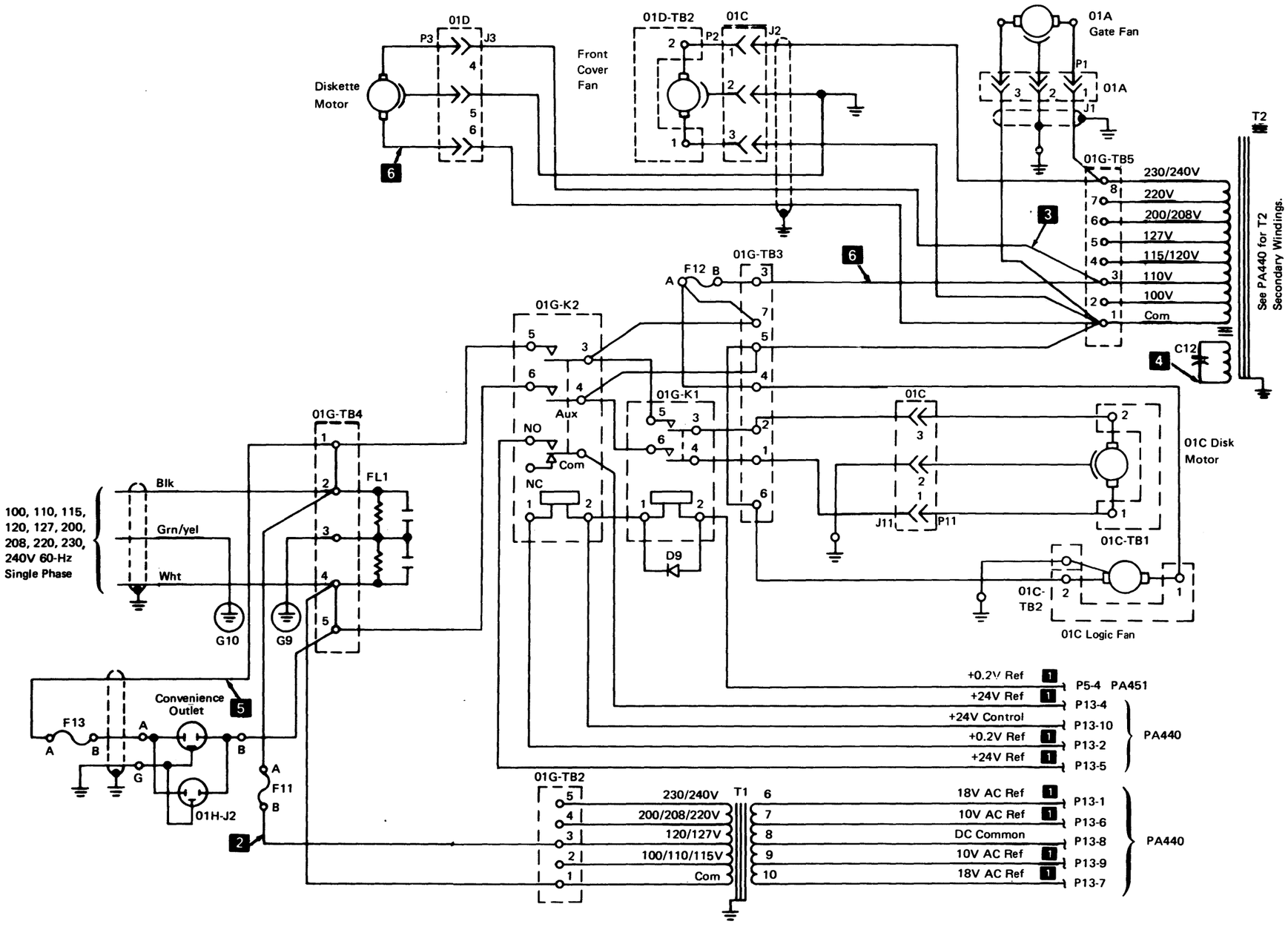



**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *All units built after EC 862592 have disk and diskette double-grounded.*

## PA420 60-Hz AC Power (Other than U.S. and Canada)

*PA421 8130 60-Hz AC Power (Other Than U.S. and Canada)*

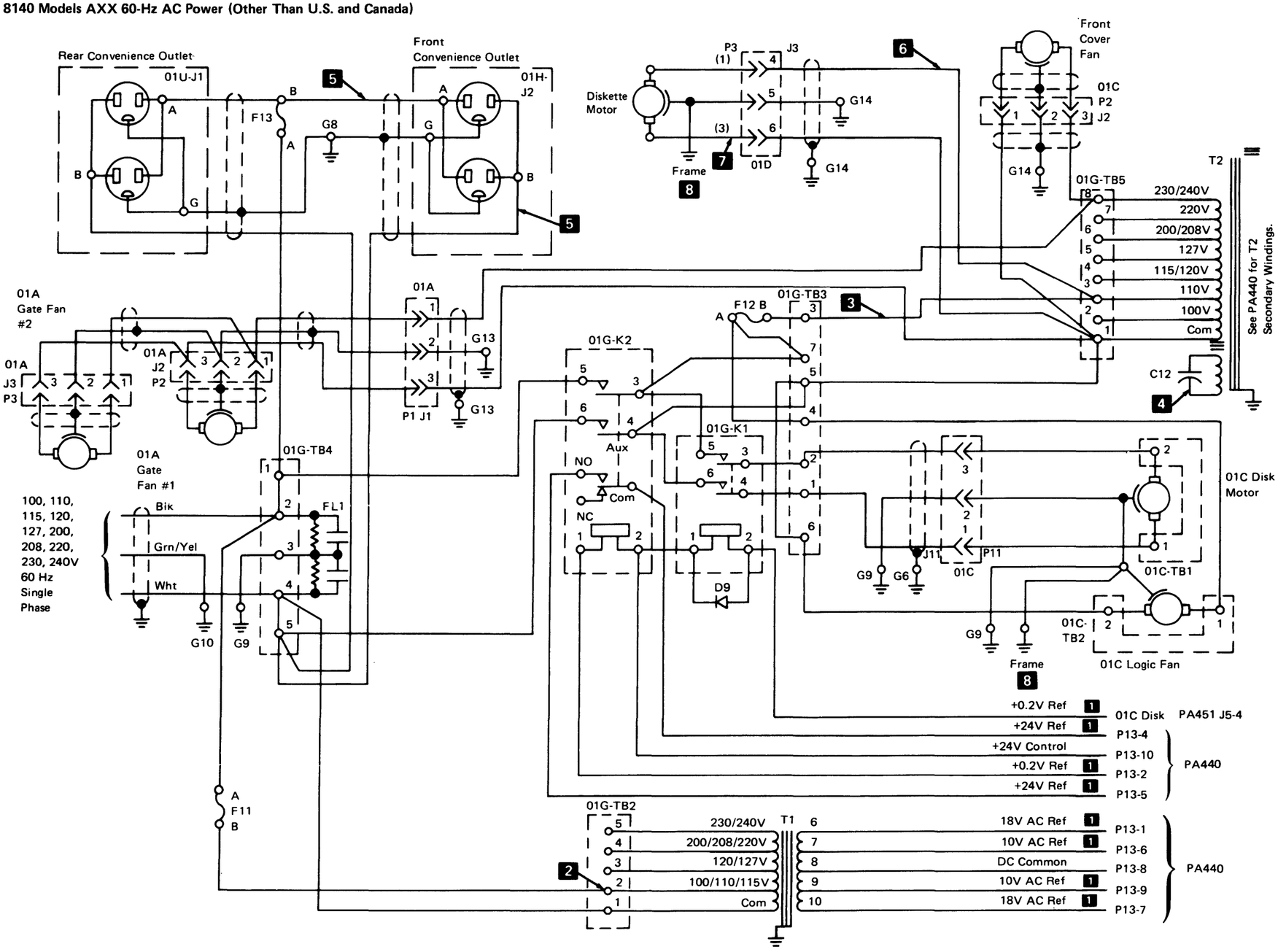



**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage for 100V and 110V. For all other input voltages, connect this lead to TB5-5.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Low-voltage convenience outlet receptacle to be connected for 100V and 110V inputs. High-voltage convenience outlet receptacle to be connected for 200V to 240V inputs. Low-voltage shown. High-voltage outlet connections same as low voltage.*
6. *Leads in P3 and J3 are connected to pins 4, 5, and 6 for 100 to 127 volts and to pins 1, 5, and 3 for 200 to 240 volts. See also Note 3*

*PA422 8140 60-Hz AC Power (Other Than U.S. and Canada)*

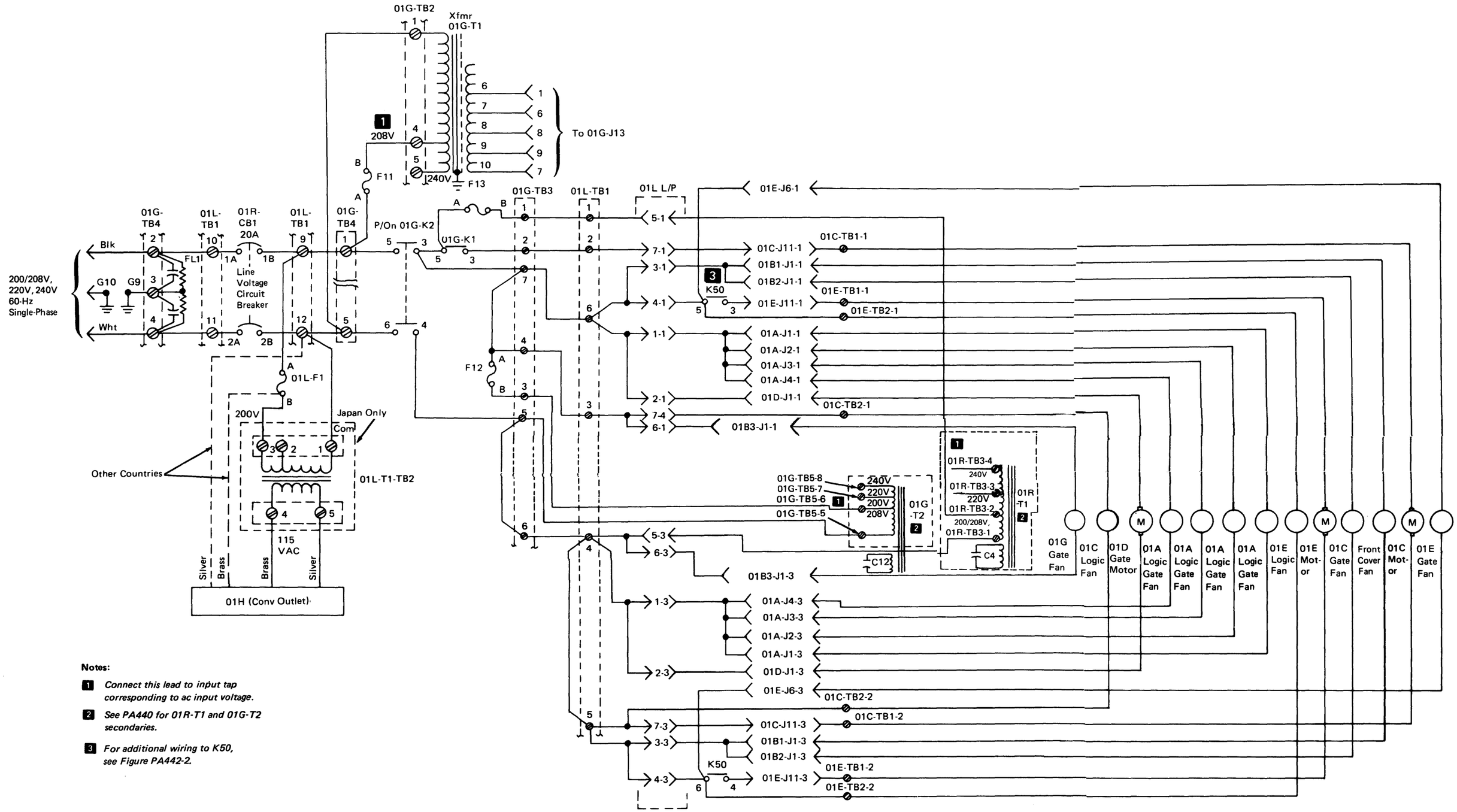
**8140 Models AXX 60-Hz AC Power (Other Than U.S. and Canada)**




**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Low-voltage convenience outlet receptacle to be connected for 100V to 127V inputs. High-voltage convenience outlet receptacle to be connected for 200V to 240V inputs. Low-voltage shown. High-voltage outlet connections same as low voltage.*
6. *Connect this lead to T2 input tap corresponding to AC input voltage for 100, 110, 115, and 120V. For 127V input, connect this lead to TB5-3. For 200, 208, 220, 230, and 240V inputs, connect this lead to TB5-7.*
7. *Leads in P3 and J3 are connected to pins 4, 5, and 6 for 100 to 127 volts and to pins 1, 5, and 3 for 200 to 240 volts. See also Notes 3 and 6.*
8. *All units built after EC 862592 have disk and diskette double-grounded.*

## 8140 Models BXX 60-Hz AC Power (Other Than U.S. and Canada)

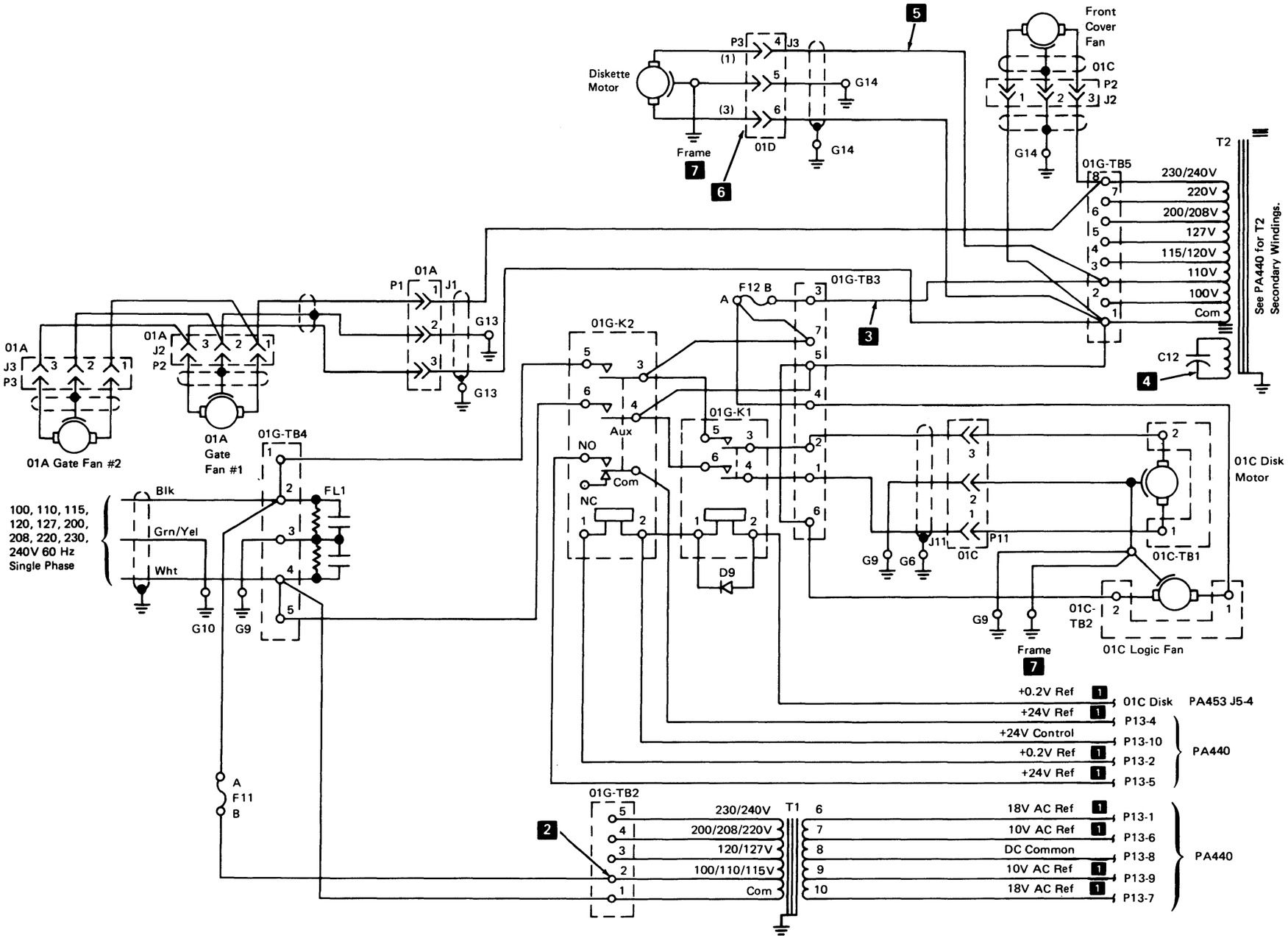



**Notes:**

1. *Connect this lead to input tap corresponding to ac input voltage.*
2. *See PA440 for 01R-T1 and 01G-T2 secondaries.*
3. *For additional wiring to K50, see Figure PA442-2.*

*PA423 8101 60-Hz AC Power (Other Than U.S. and Canada)*

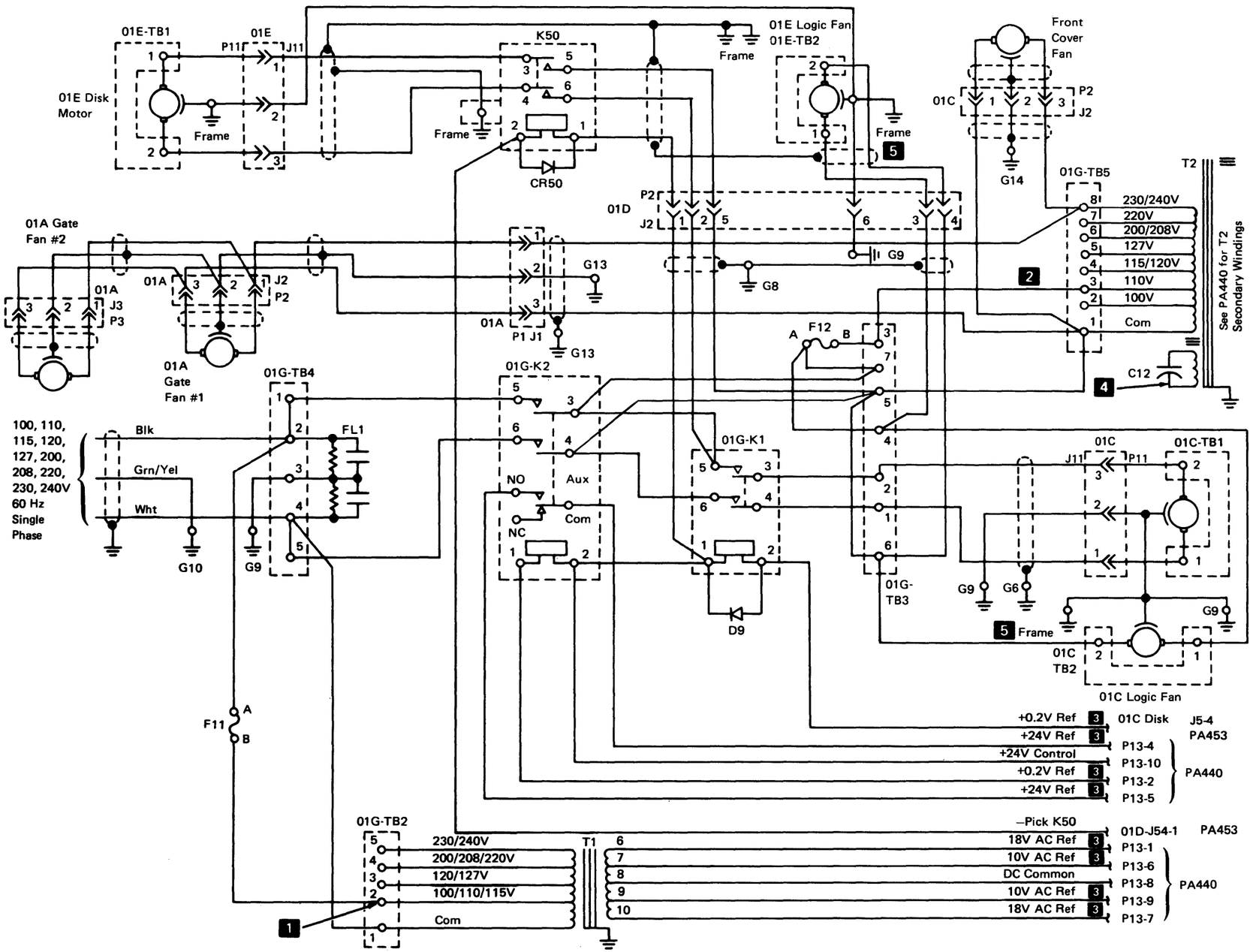
**8101 Models A1X, A20, and A23 60-Hz AC Power (Other Than U.S. and Canada)**




**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Connect this lead to T2 input tap corresponding to AC input voltage for 100, 110, 115, and 120V. For 127V, connect this lead to TB5-3. For 200, 208, 220, 230 and 240V, connect this lead to TB5-7.*
6. *Leads in P3 and J3 are connected to pins 4, 5, and 6 for 100 to 127 volts and to pins 1, 5, and 3 for 200 to 240 volts. See also Notes 3 and 5.*
7. *All units built after EC 862592 have disk and diskette double-grounded.*

## 8101 Model A25 60-Hz AC Power (Other Than U.S. and Canada)

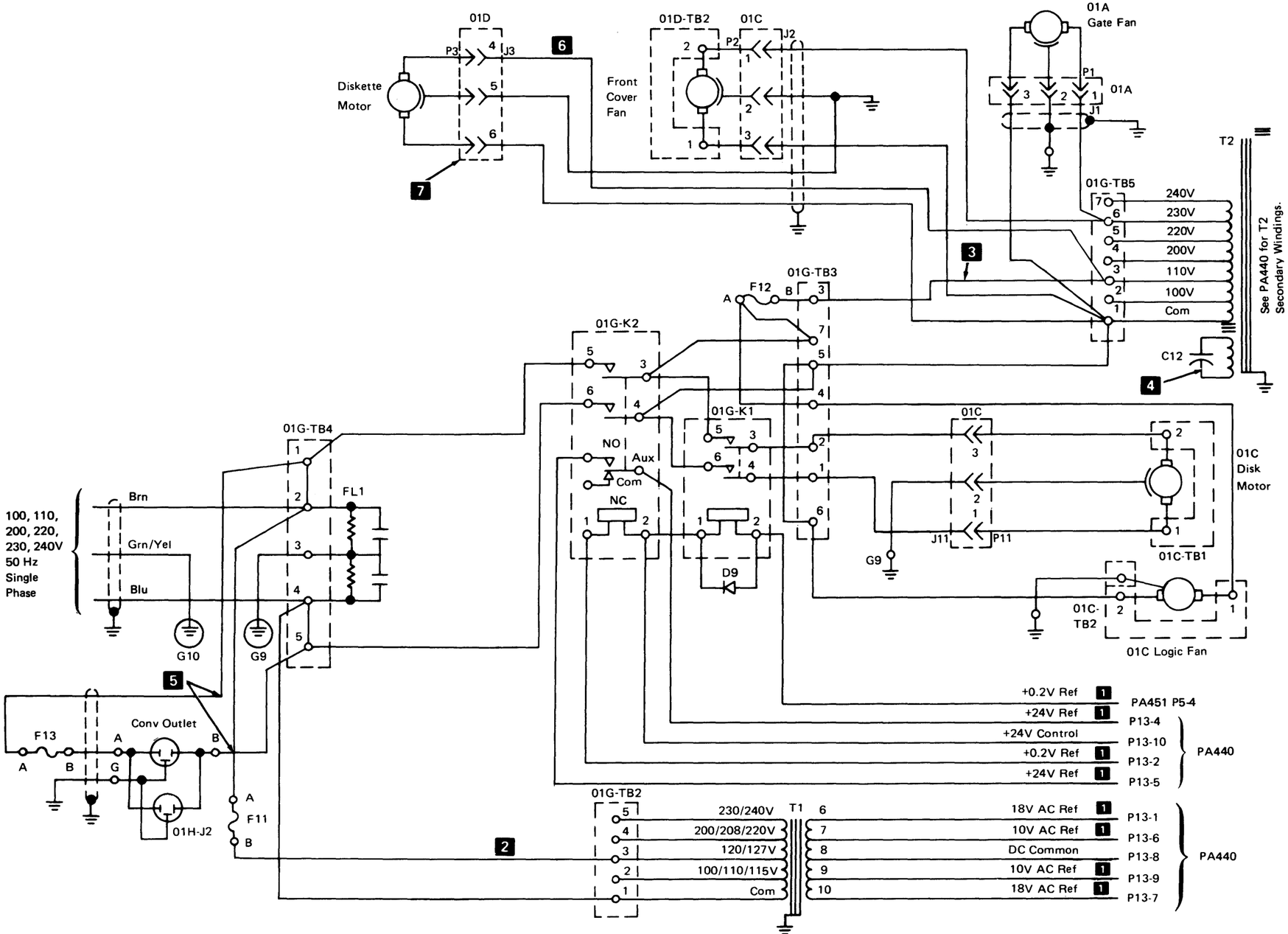



**Notes:**

1. *Connect this lead to T1 input tap corresponding to AC input voltage.*
2. *Connect this lead to T2 input tap corresponding to AC input voltage.*
3. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *All units built after EC 862592 have disk and diskette double-grounded.*

## PA430 50-Hz AC Power

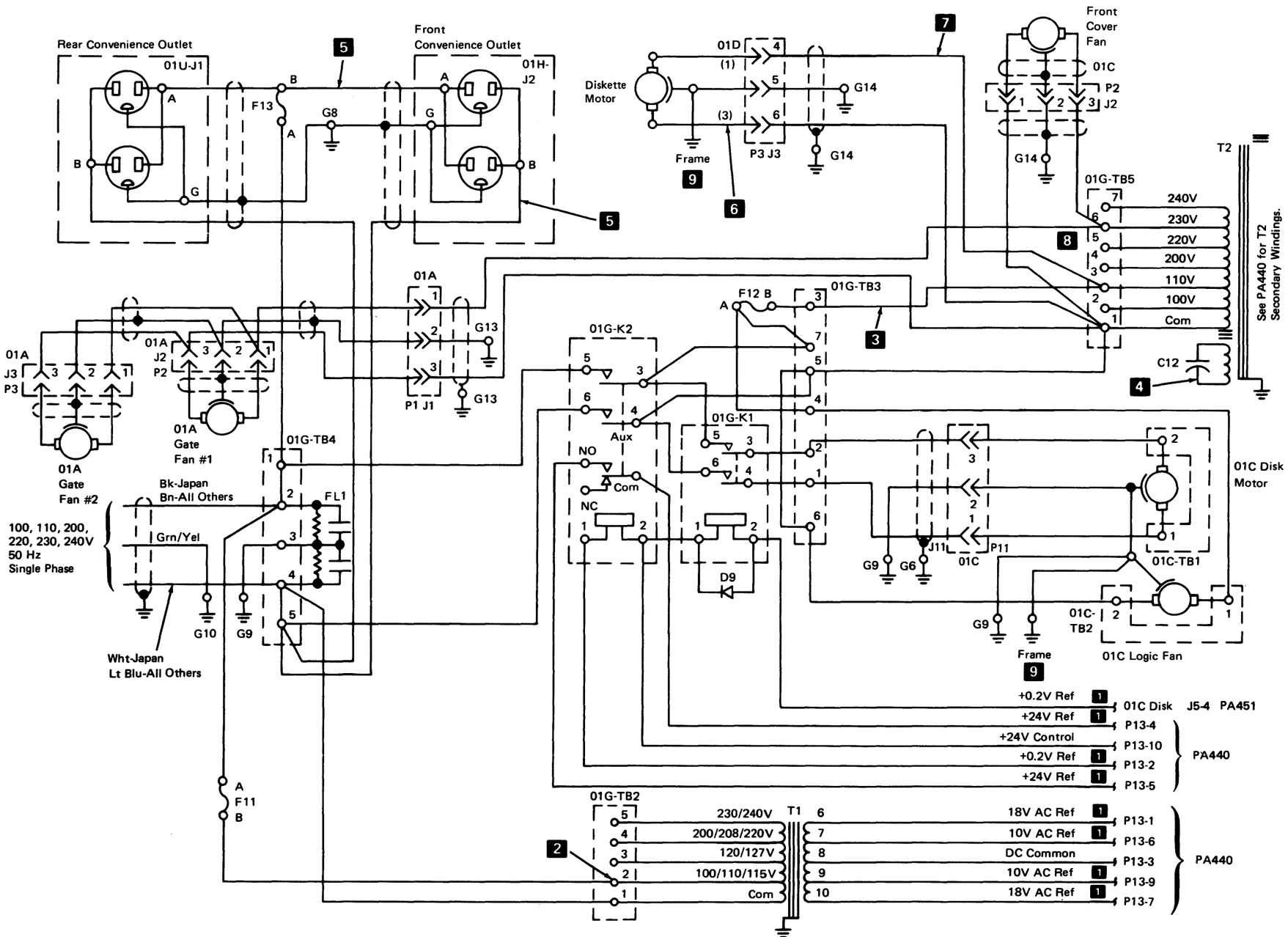
*PA431 8130 50-Hz AC Power*




**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Low-voltage convenience outlet receptacle to be connected for 100V-127V inputs. High-voltage convenience outlet receptacle to be connected for 200V to 240V inputs. Low-voltage shown. High-voltage outlet connections same as low voltage.*
6. *Connect this lead to T2 input tap corresponding to AC input voltage 100/110/115/120V. For 127V input, connect this lead to TB5-3. For all other input voltages (200/208/220/230/240V) connect this lead to TB5-7.*
7. *Leads in P3 and J3 are connected to pins 4, 5, and 6 for 100 to 126 volts and to pins 1, 5, and 3 for 200 to 240 volts. See also Notes 3 and 6.*

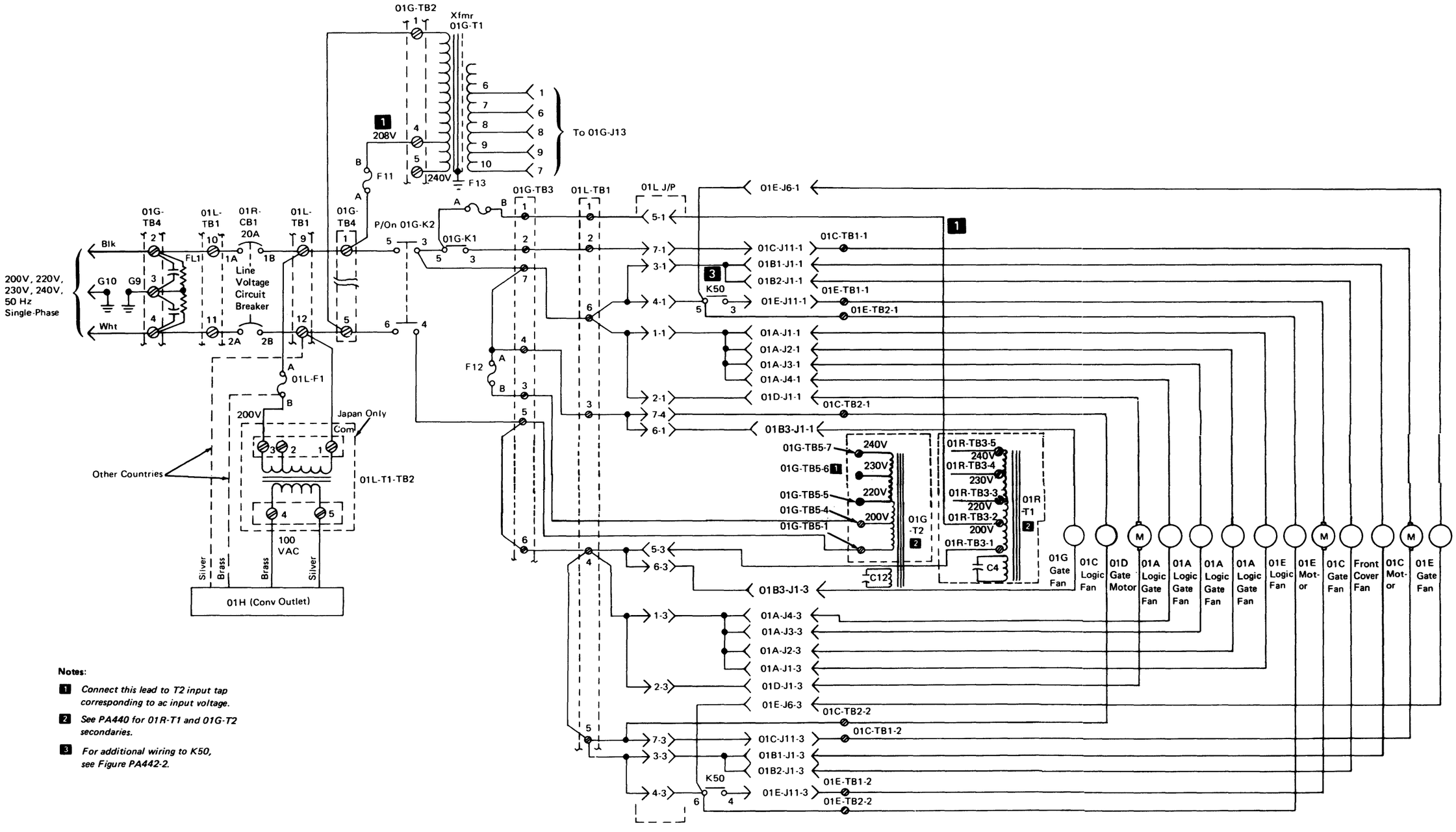
**8140 Models AXX 50-Hz AC Power**




**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Low-voltage convenience outlet receptacle to be connected for 100V and 110V inputs. High-voltage convenience outlet receptacle to be connected for 200V and 240V inputs. Low-voltage shown. High-voltage outlet connections same as low voltage.*
6. *Leads in P3 and J3 are connected to pins 4, 5, and 6 for 100 or 110 volts and to pins 1, 5, and 3 for 200 to 240 volts. See also Note 3.*
7. *Connect this lead to T2 input tap corresponding to AC input for 100 or 110V.*
8. *Taps 2 and 3 on T2 primary are not brought out on transformer PN 7389297.*
9. *All units after EC 862592 have disk and diskette double-grounded.*

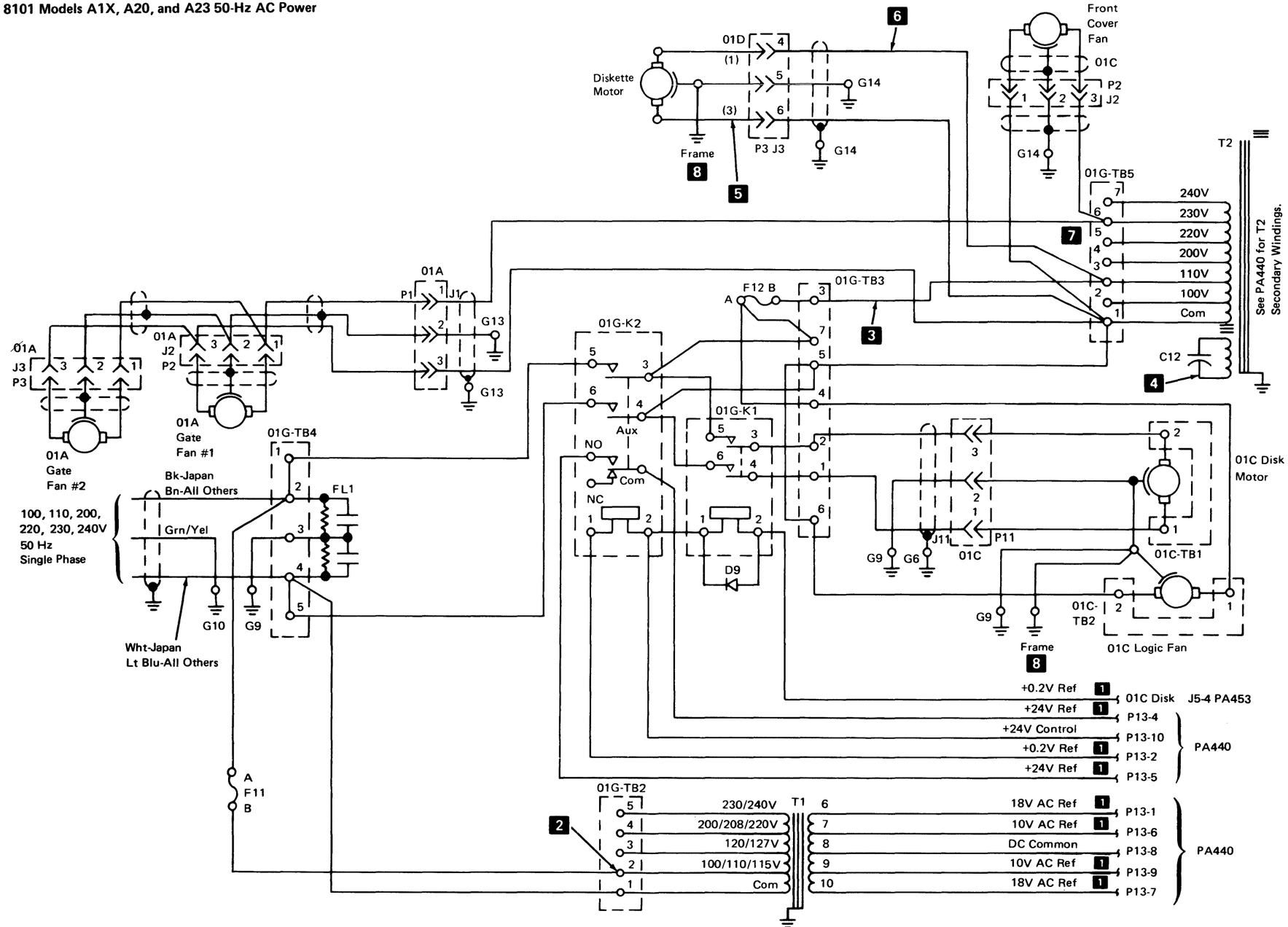
**8140 Models BXX 50-Hz AC Power**




**Notes:**

1. *Connect this lead to T2 input tap corresponding to ac input voltage.*
2. *See PA440 for 01R-T1 and 01G-T2 secondaries.*
3. *For additional wiring to K50, see Figure PA442-2.*

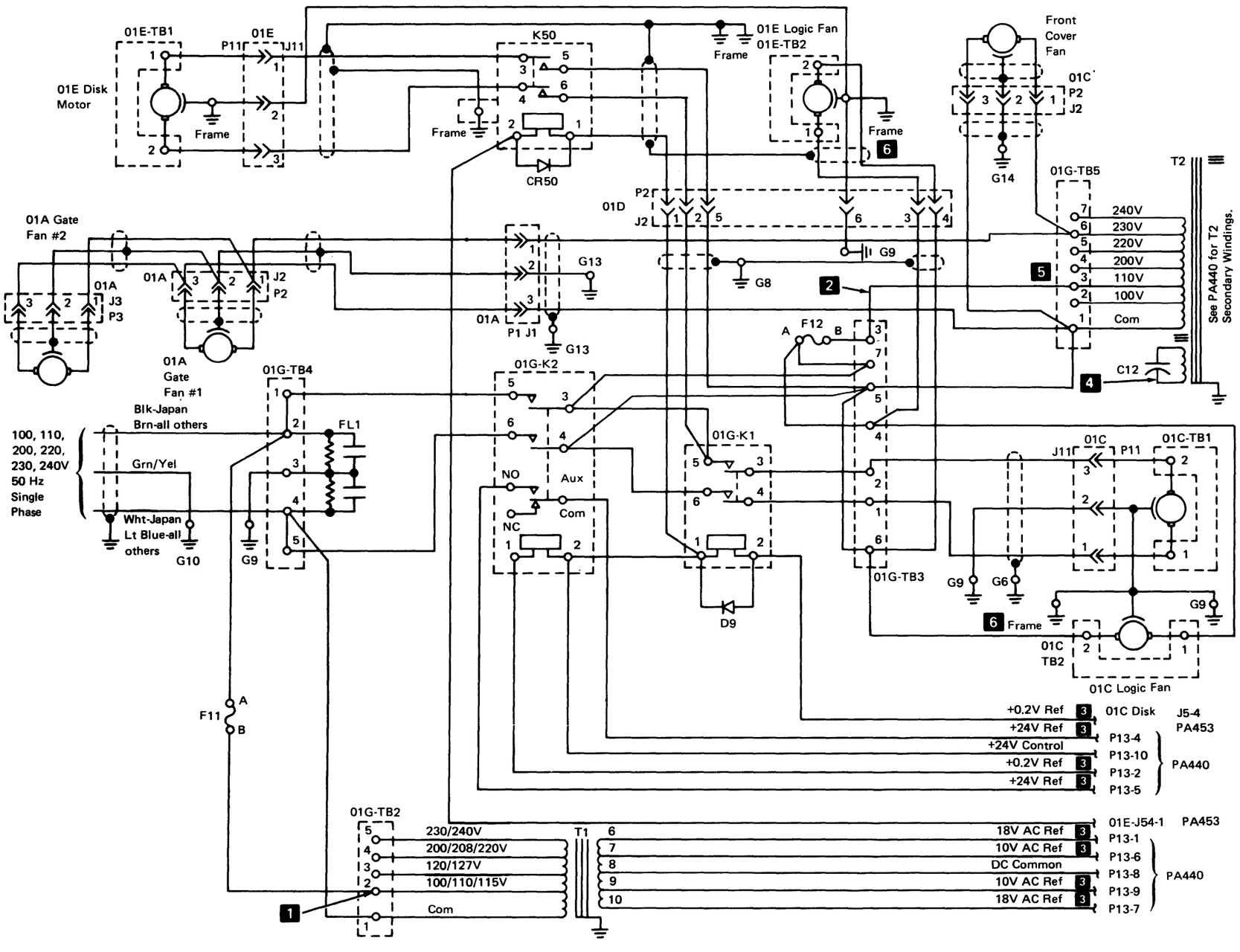
**8101 Models A1X, A20, and A23 50-Hz AC Power**




**Notes:**

1. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
2. *Connect this lead to T1 input tap corresponding to AC input voltage.*
3. *Connect this lead to T2 input tap corresponding to AC input voltage.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Leads in P3 and J3 are connected to pins 4, 5, and 6 for 100 or 110 volts and to pins 1, 5, and 3 for 200 to 240 volts. See also Note 3.*
6. *Connect this lead to T2 input tap corresponding to AC input for 100 and 110V. For 200, 220, 230, and 240V, connect this lead to TB5-6.*
7. *Taps 2 and 3 on T2 primary are not brought out on transformers PN 7389297.*
8. *All units built after EC 862592 have disk and diskette double-grounded.*

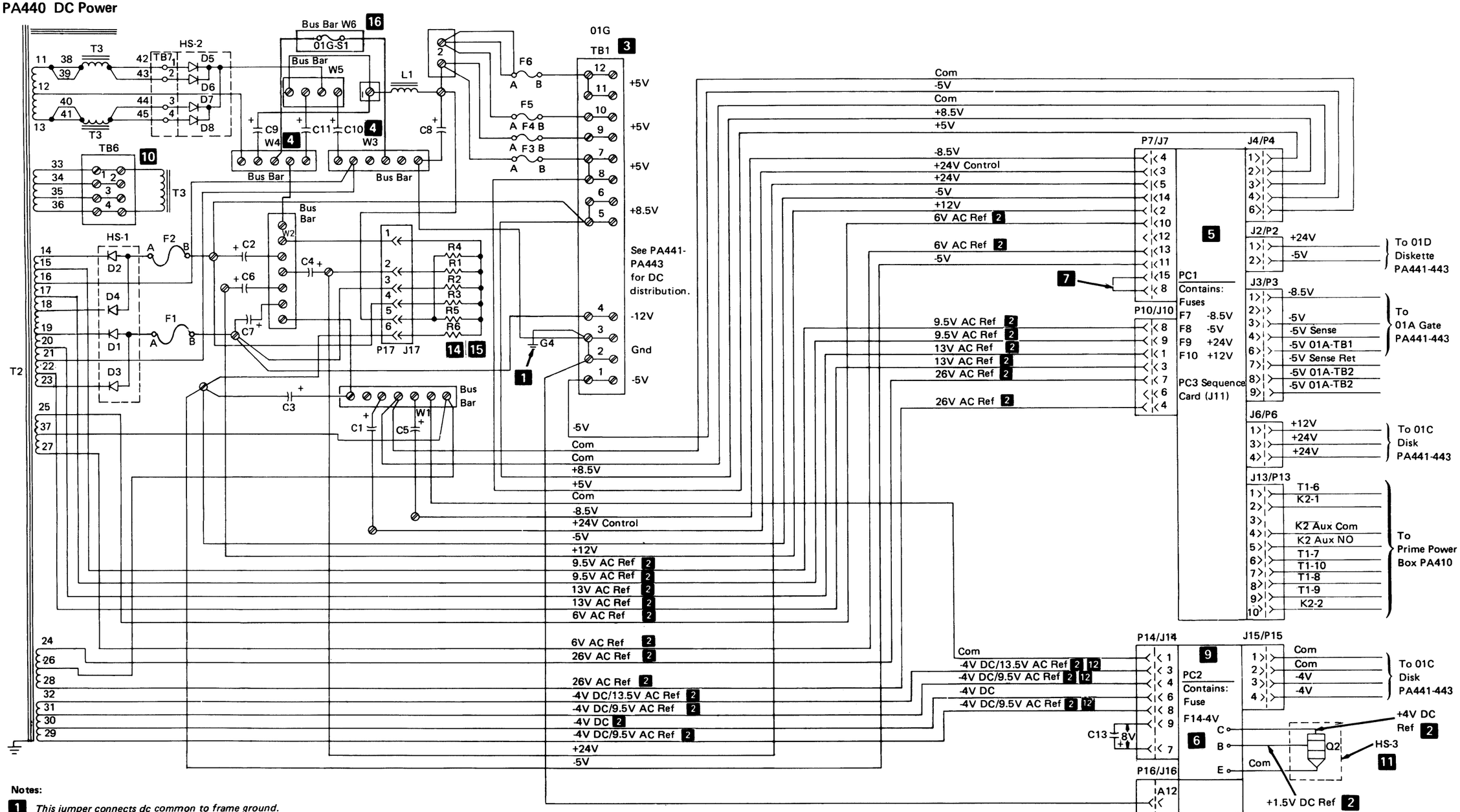
**8101 Model A25 50-Hz AC Power**




**Notes:**

1. *Connect this lead to T1 input tap corresponding to AC input voltage.*
2. *Connect this lead to T2 input tap corresponding to AC input voltage.*
3. *Typical value with system operating properly; for reference only. Voltage measured with respect to DC common.*
4. **DANGER**
   **High-voltage resonant circuit. Do not measure across C12 with power on.**
5. *Taps 2 and 3 on T2 primary are not brought out on transformer PN 7389297.*
6. *All units built after EC 862592 have disk and diskette double-grounded.*

## PA440 DC Power




See PA710 for physical location of Q2.

**Notes:**

1. *This jumper connects dc common to frame ground.*
2. *Typical value with system operating properly; for reference only.*
3. *For additional wiring to TB1, see PA441.*
4. *For additional wiring to W3 and W4, see PA441.*
5. *For additional wiring to PC1, see PA441, PA451, and PA461.*
6. *For additional wiring to PC2, see PA441, PA451, and PA462.*
7. *Jumper present on 60-Hz machines only.*
8. *For logic cable connections, see PA450.*
9. *Energized LED on PC2 indicates power fault associated with 01C disk.*
10. *For adjustment of T3, see PA510.*
11. *See PA710 for location and PA663 for connections.*
12. *Both AC and DC voltages on these lines simultaneously.*
13. *For additional wiring to P2/J2, P3/J3, P4/J4, P6/J6, P7/J7, and P15/J15, see PA441.*
14. *For R1–R6 values, see PA741.*
15. *R6 not connected for 768K and 1024K machines.*
16. *Present with EC 321965 installed.*

**Figure PA440-1. 8130 DC Power**

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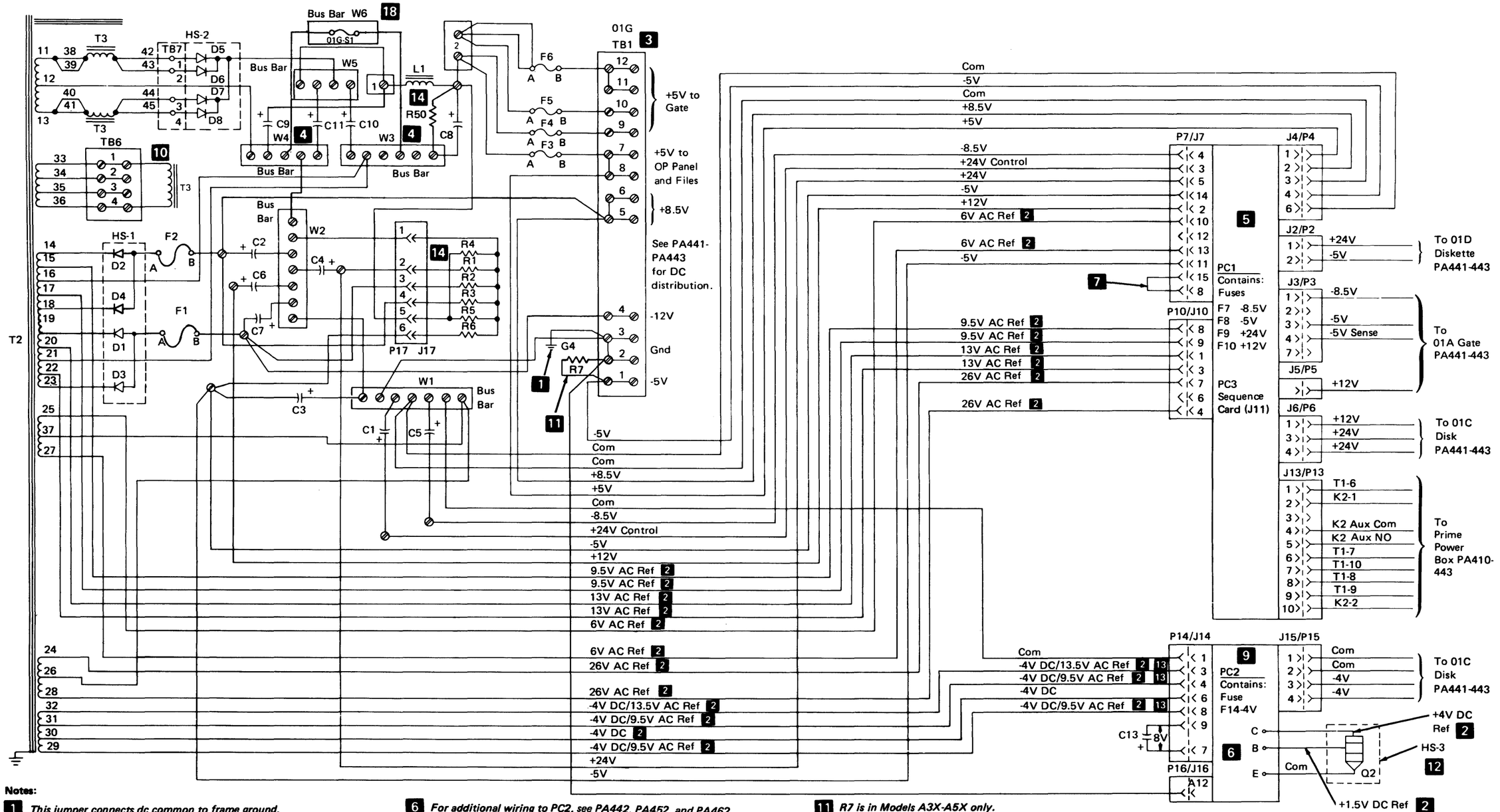



See PA710 for physical location of Q2.

**Notes:**

1. *This jumper connects dc common to frame ground.*
2. *Typical value with system operating properly; for reference only.*
3. *For additional wiring to TB1, see PA442.*
4. *For additional wiring to W3 and W4, see PA442.*
5. *For additional wiring to PC1, see PA442, PA452, and PA461.*
6. *For additional wiring to PC2, see PA442, PA452, and PA462.*
7. *Jumper present on 60-Hz machines only.*
8. *For logic cable connections, see PA450.*
9. *Energized LED on PC2 indicates power fault associated with 01C disk.*
10. *For adjustment of T3, see PA510.*
11. *R7 is in Models A3X-A5X only.*
12. *See PA710 for location and PA663 for connections.*
13. *Both AC and DC voltages on these lines simultaneously.*
14. *On some special-feature machines, R50 replaces R4 and R5 by being wired directly across the C2 terminals, and the C8 + end of the cable lead to J17-6 is disconnected and covered.*
15. *For additional wiring to P2/J2, P3/J3, P4/J4, P6/J6, and P15/J15, see PA442.*
16. *For additional wiring to P5/J5, see PA442 and PA452.*
17. *For additional wiring to P16/J16, see PA452.*
18. *Present with EC 867486 installed.*

**Figure PA440-2. 8140 Models AXX DC Power**

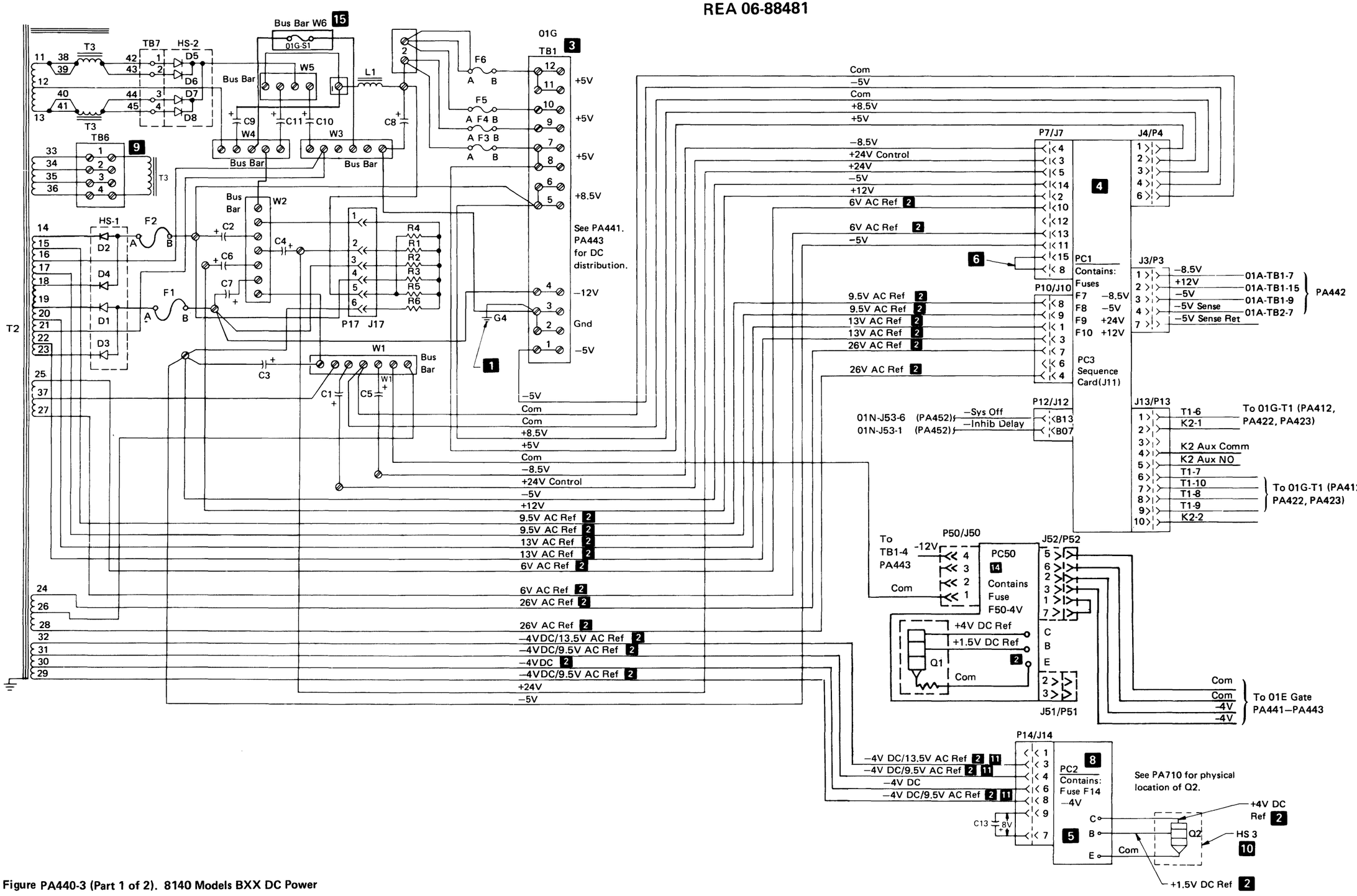



Figure PA440-3 (Part 1 of 2). 8140 Models BXX DC Power

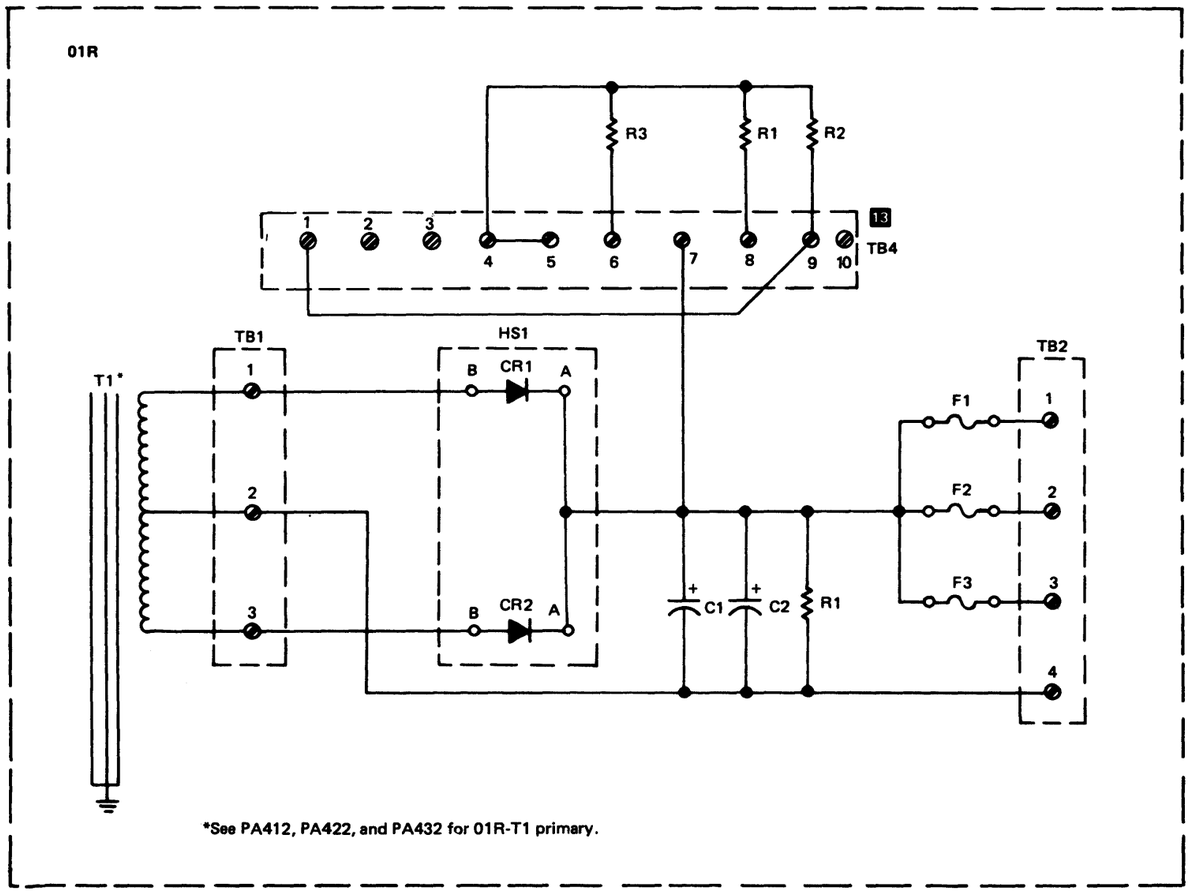



**Figure PA440-3 (Part 2 of 2). 8140 Models BXX DC Power**

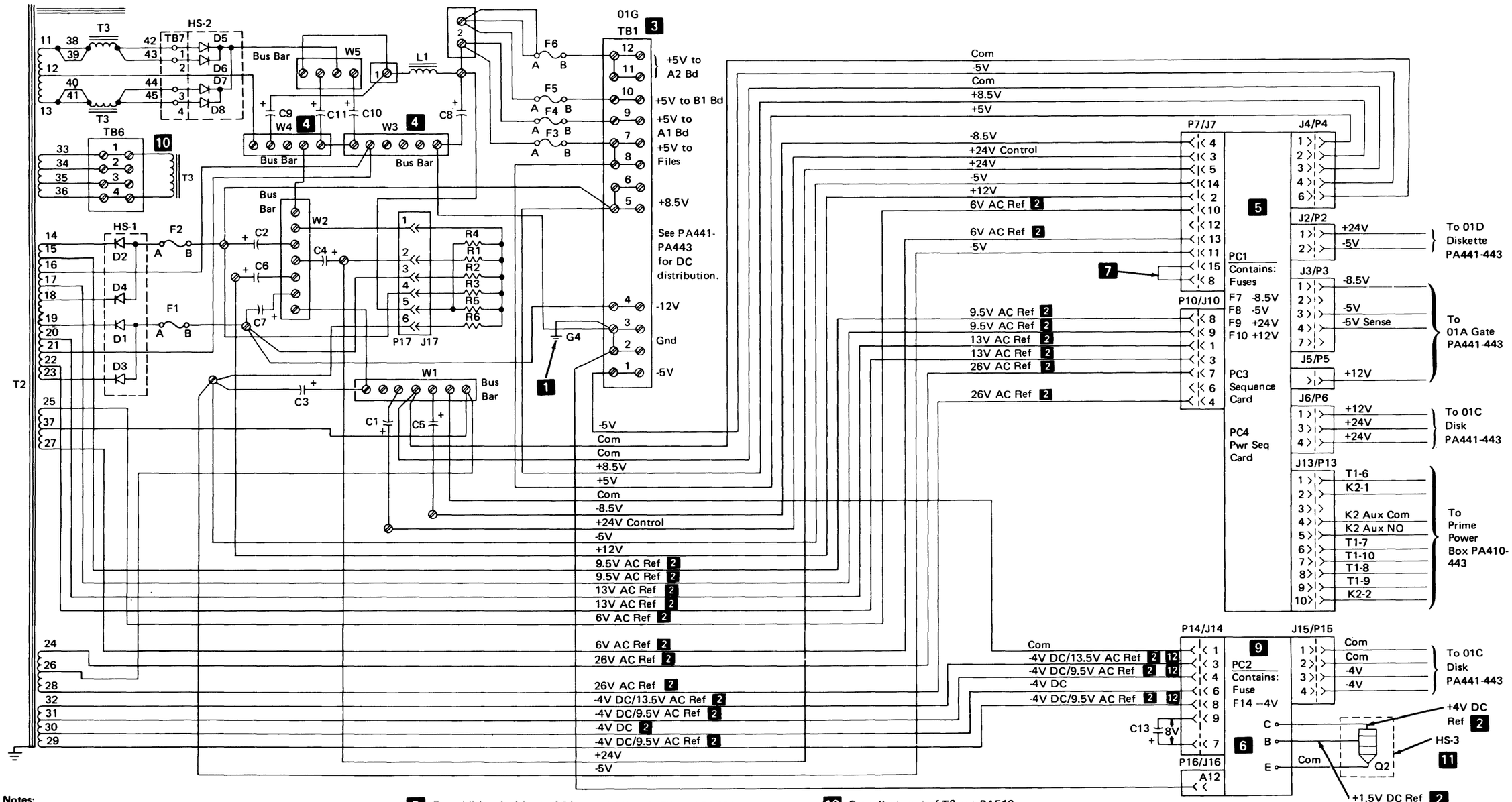
**Notes:**

1. *This jumper connects dc common to frame ground.*
2. *Typical value with system operating properly; for reference only.*
3. *For additional wiring to TB1, see PA442.*
4. *For additional wiring to PC1, see PA442, PA452, and PA461.*
5. *For additional wiring to PC2, see PA442, PA452, and PA462.*
6. *Jumper present on 60-Hz machines only.*
7. *For logic cable connections, see PA450.*
8. *Energized LED on PC2 indicates power fault associated with 01C disk.*
9. *For adjustment of T3, see PA510.*
10. *See PA710 for location and PA663 for connections.*
11. *Both AC and DC voltages on these lines simultaneously.*
12. *For additional wiring to P4/J4 and P15/J15, see PA442.*
13. *Depending on the features installed, add and/or remove jumpers on TB4 as follows:*

| Feature(s) Installed | Add Jumper | Remove Jumper |
|---|---|---|
| Communications or Tape or Communications and Tape | 3 to 6 | 3 to 8 |
| Communications and Floating-Point or Tape and Floating-Point or Communications and Tape | 3 to 6 | 2 to 8 and 3 to 8 |
| Communications in C2 and D2 boards or Display/Printer | None | 3 to 8 |
| Floating-Point | None | 2 to 8 |
| Display/Printer and Floating-Point | None | 2 to 8 and 3 to 8 |

**Note:** *Connect removed jumpers between TB4-7 and TB4-10.*

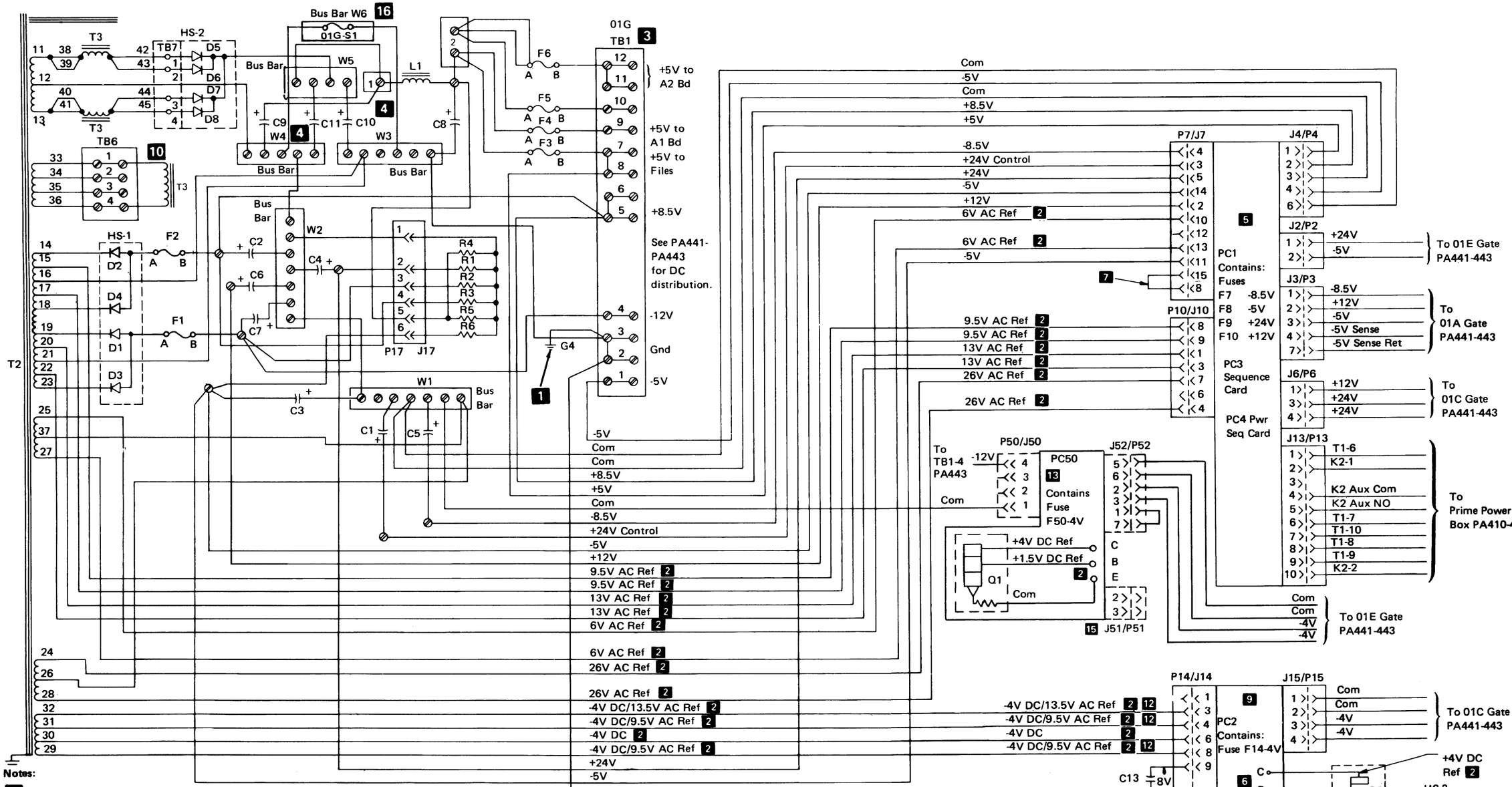
14. *For additional wiring to PC50 and PC51, see PA453.*
15. *Present with EC862250 installed.*




**Notes:**

1. *This jumper connects dc common to frame ground.*
2. *Typical value with system operating properly; for reference only.*
3. *For additional wiring to TB1, see PA443.*
4. *For additional wiring to W3 and W4, see PA443.*
5. *For additional wiring to PC1, see PA443, PA453, and PA461.*
6. *For additional wiring to PC2, see PA443, PA453, and PA462.*
7. *Jumper present on 60-Hz machines only.*
8. *For logic cable connections, see PA450.*
9. *Energized LED on PC2 indicates power fault associated with 01C disk.*
10. *For adjustment of T3, see PA510.*
11. *See PA710 for location and PA663 for connections.*
12. *Both AC and DC voltages on these lines simultaneously.*
13. *For additional wiring to P2/J2, P3/J3, P4/J4, P6/J6, P15/J15, and P16/J16, see PA443.*
14. *For additional wiring to P5/J5, see PA443 and PA453.*

**Figure PA440-4. 8101 Models A1X, A20, and A23 DC Power**




**Notes:**

1. *This jumper connects dc common to frame ground.*
2. *Typical value with system operating properly; for reference only.*
3. *For additional wiring to TB1, see PA443.*
4. *For additional wiring to W3 and W4, see PA443.*
5. *For additional wiring to PC1, see PA443, PA453, and PA461.*
6. *For additional wiring to PC2, see PA443, PA453, and PA462.*
7. *Jumper present on 60-Hz machines only.*
8. *For logic cable connections, see PA450.*
9. *Energized LED on PC2 indicates power fault associated with 01C disk.*
10. *For adjustment of T3, see PA510.*
11. *See PA710 for location and PA663 for connections.*
12. *Both AC and DC voltages on these lines simultaneously.*
13. *For additional wiring to PC50 and PC51, see PA453.*
14. *For additional wiring to P2/J2, P3/J3, P4/J4, P6/J6, and P15/J15, see PA443.*
15. *For additional wiring to P16/J16 and J51/P51, see PA453.*
16. *Present with EC 867485 installed.*

**Figure PA440-5. 8101 Model A25 DC Power**

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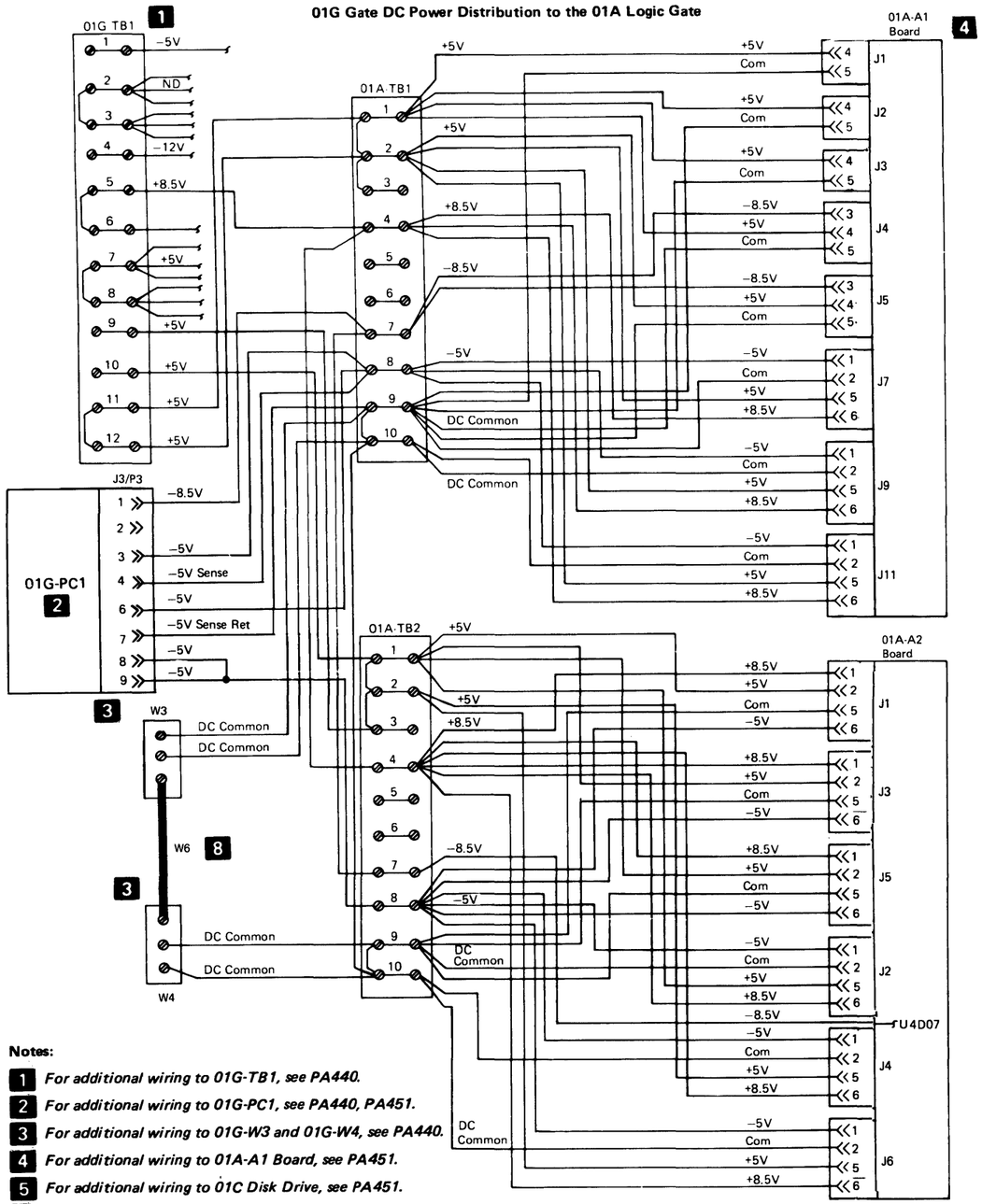
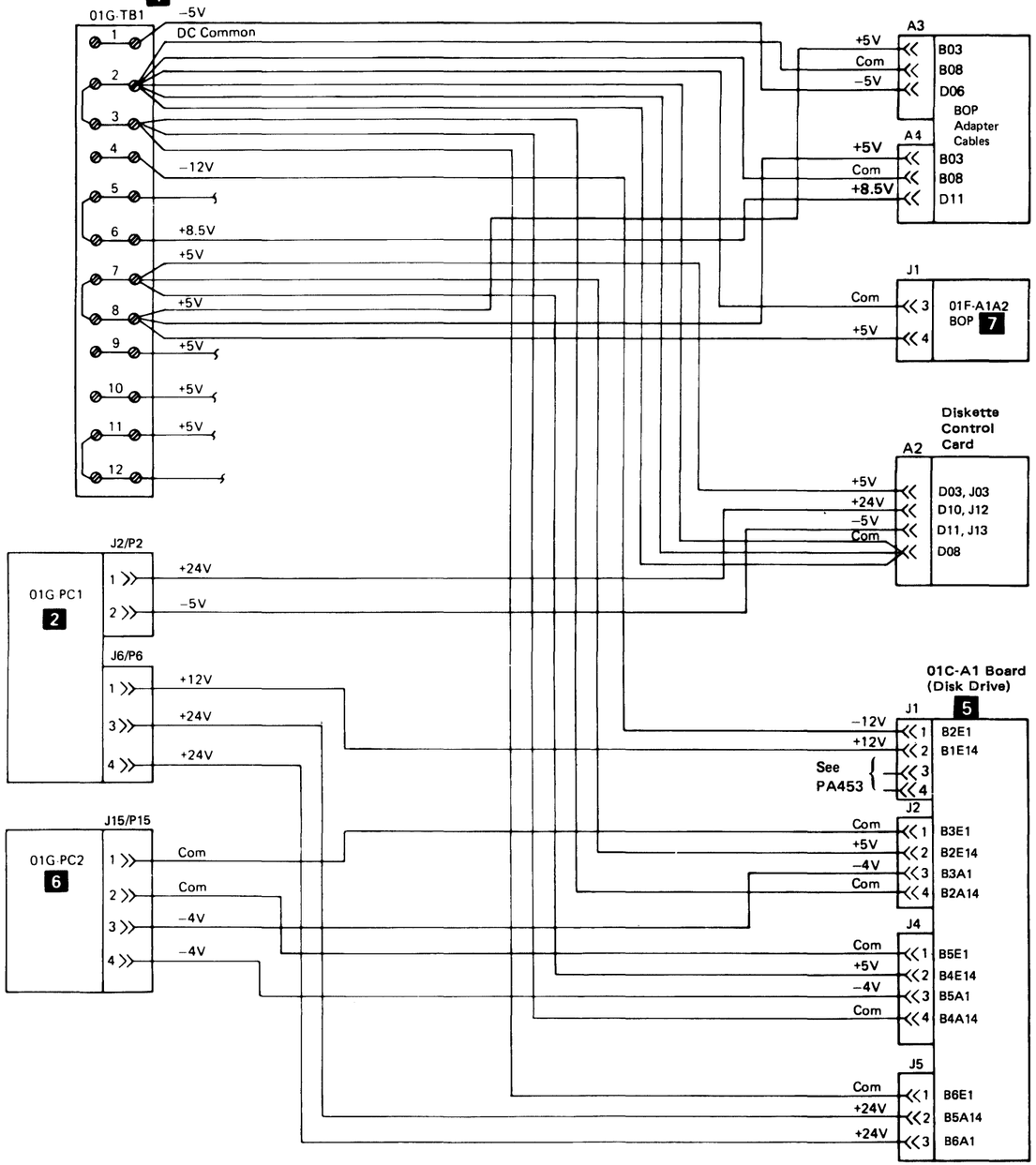
## 01G Gate DC Power Distribution to the 01A Logic Gate




**Notes:**

1. *For additional wiring to 01G-TB1, see PA440.*
2. *For additional wiring to 01G-PC1, see PA440, PA451.*
3. *For additional wiring to 01G-W3 and 01G-W4, see PA440.*
4. *For additional wiring to 01A-A1 Board, see PA451.*
5. *For additional wiring to 01C Disk Drive, see PA451.*
6. *For additional wiring to 01G-PC2, see PA440, PA451.*
7. *For additional wiring to 01F-BOP, see PA451.*
8. *Present with EC321965 installed.*

## 01G Gate DC Power Distribution to the Operator Panel, Disk, and Diskette




**Note:** *See PA740 through PA743 for locations.*

*PA442 8140 DC Distribution*

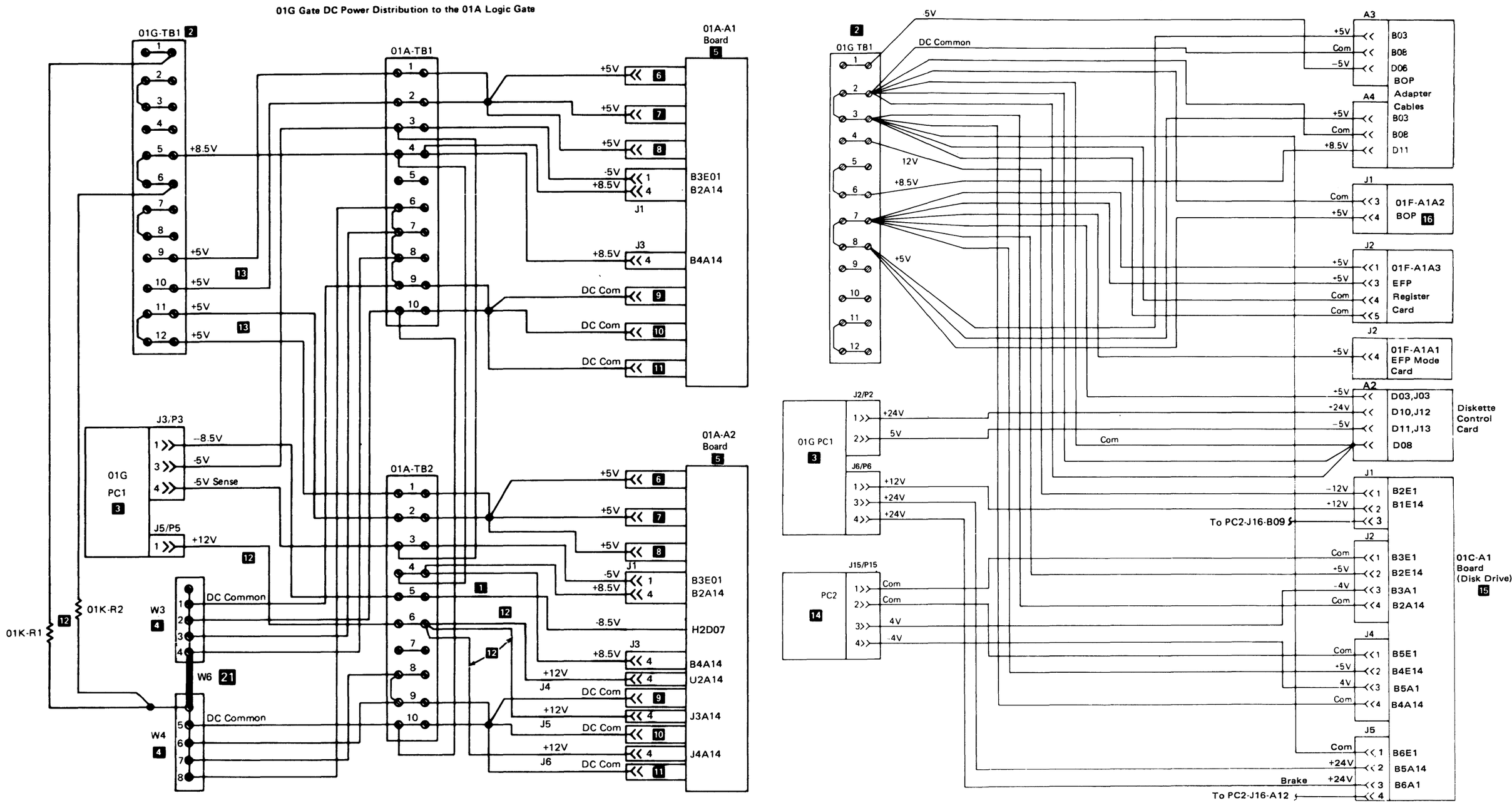



**Figure PA442-1 (Part 1 of 2). 8140 Models AXX DC Distribution**

Notes:

1. *This wire in Model A31-34 & A41-44 only.*
2. *For additional wiring to 01G-TB1, see PA440.*
3. *For additional wiring to 01G-PC-1, see PA440, PA452.*
4. *For additional wiring to 01G-W3 and 01G-W4, see PA440.*
5. *For additional wiring to 01A-A1 and 01A-A2 Boards, see PA452.*

6.

| | | | |
|---|---|---|---|
| PIN | E1B12 | OR | (Y2C04) |
| | E1C12 | | (Y2C05) |
| | E1D12 | | (Y2C06) |
| | E1E12 | | (Y2C07) |
| | F1A12 | | (Y2C08) |
| | F1B12 | | (Y2C09) |
| | F1C12 | | (Y2C10) |
| PIN | F1D12 | OR | (Y2C11) |

7.

| | | | |
|---|---|---|---|
| PIN | H1C12 | OR | (Y3C04) |
| | H1D12 | | (Y3C05) |
| | H1E12 | | (Y3C06) |
| | J1A12 | | (Y3C07) |
| | J1B12 | | (Y3C08) |
| | J1C12 | | (Y3C09) |
| | J1D12 | | (Y3C10) |
| PIN | J1E12 | OR | (Y3C11) |

8.

| | | | |
|---|---|---|---|
| PIN | M1A12 | OR | (Y4C04) |
| | M1B12 | | (Y4C05) |
| | M1C12 | | (Y4C06) |
| | M1D12 | | (Y4C07) |
| | M1E12 | | (Y4C08) |
| | N1A12 | | (Y4C09) |
| | N1B12 | | (Y4C10) |
| PIN | N1C12 | OR | (Y4C11) |

9.

| | | | |
|---|---|---|---|
| PIN | E6B03 | OR | (Z2C04) |
| | E6C03 | | (Z2C05) |
| | E6D03 | | (Z2C06) |
| | E6E03 | | (Z2C07) |
| | F6A03 | | (Z2C08) |
| | F6B03 | | (Z2C09) |
| | F6C03 | | (Z2C10) |
| PIN | F6D03 | OR | (Z2C11) |

10.

| | | | |
|---|---|---|---|
| PIN | H6C03 | OR | (Z3C04) |
| | H6D03 | | (Z3C05) |
| | H6E03 | | (Z3C06) |
| | J6A03 | | (Z3C07) |
| | J6B03 | | (Z3C08) |
| | J6C03 | | (Z3C09) |
| | J6D03 | | (Z3C10) |
| PIN | J6E03 | OR | (Z3C11) |

11.

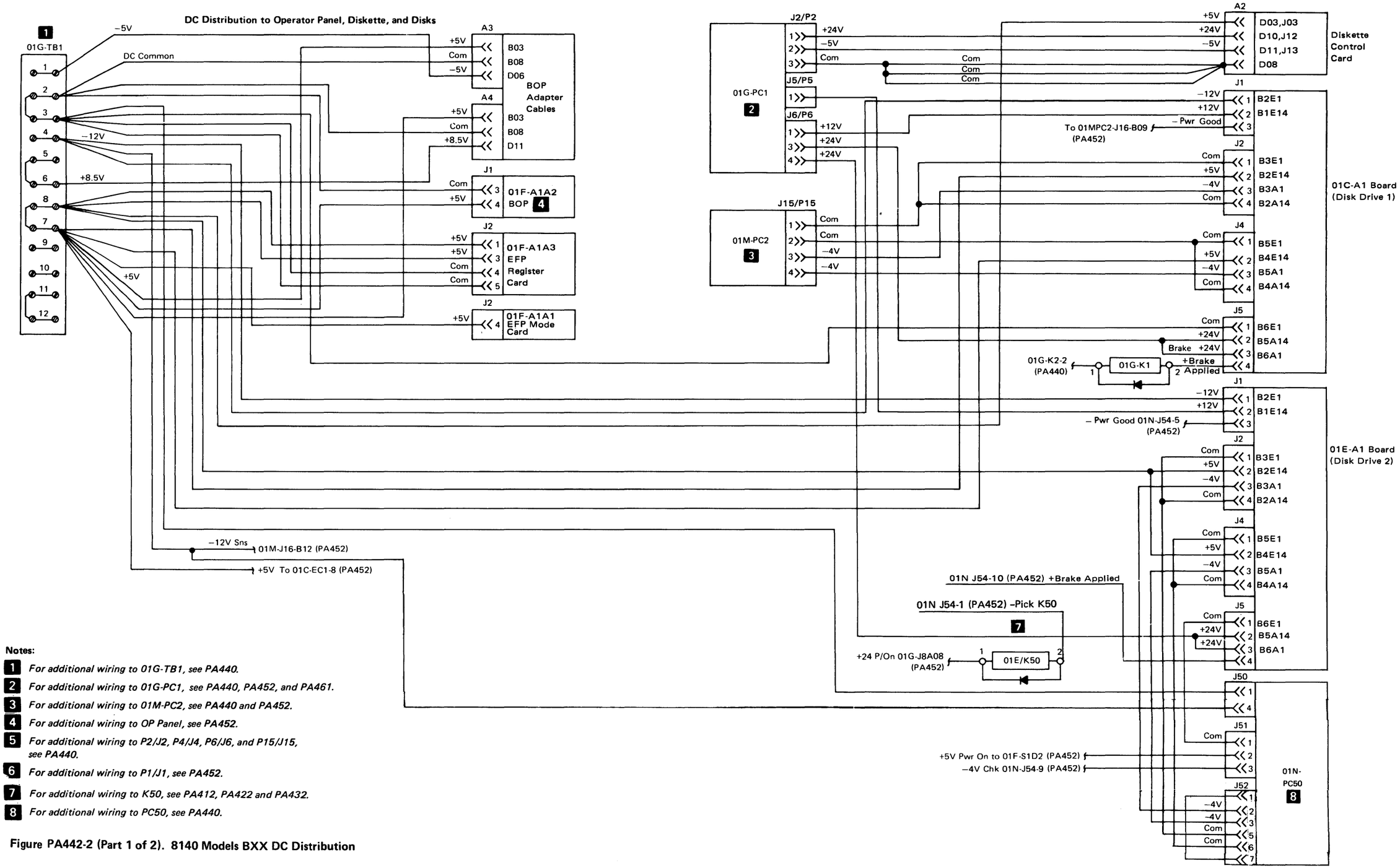
| | | | |
|---|---|---|---|
| PIN | M6A03 | OR | (Z4C04) |
| | M6B03 | | (Z4C05) |
| | M6C03 | | (Z4C06) |
| | M6D03 | | (Z4C07) |
| | M6E03 | | (Z4C08) |
| | N6A03 | | (Z4C09) |
| | N6B03 | | (Z4C10) |
| PIN | N6C03 | OR | (Z4C11) |

12. *Required for Models A61-A64 and A71-A74 only.*
13. *On some special featured machines to reduce voltage drop to match the new current loads, the position of the following leads are exchanged:*

    *Lead 1 at TB1-9 reattached to TB1-11*
    *Lead 2 at TB1-10 reattached to TB1-12*
    *Lead 16 at TB1-11 reattached to TB1-9*
    *Lead 15 at TB1-12 reattached to TB1-10*

14. *For additional wiring to 01G-PC-2, see PA440, PA452.*
15. *For additional wiring to 01C Disk Drive, see PA452.*
16. *For additional wiring to 01F, BOP Panel, see PA452.*
18. *For additional wiring to P2/J2, P3/J3, P4/J4, P6/J6, and P15/J15, see PA440.*
19. *For additional wiring to P1/J1, see PA452.*
20. *For additional wiring to P5/J5, see PA440 and PA452.*
21. *Present with EC867486 installed.*

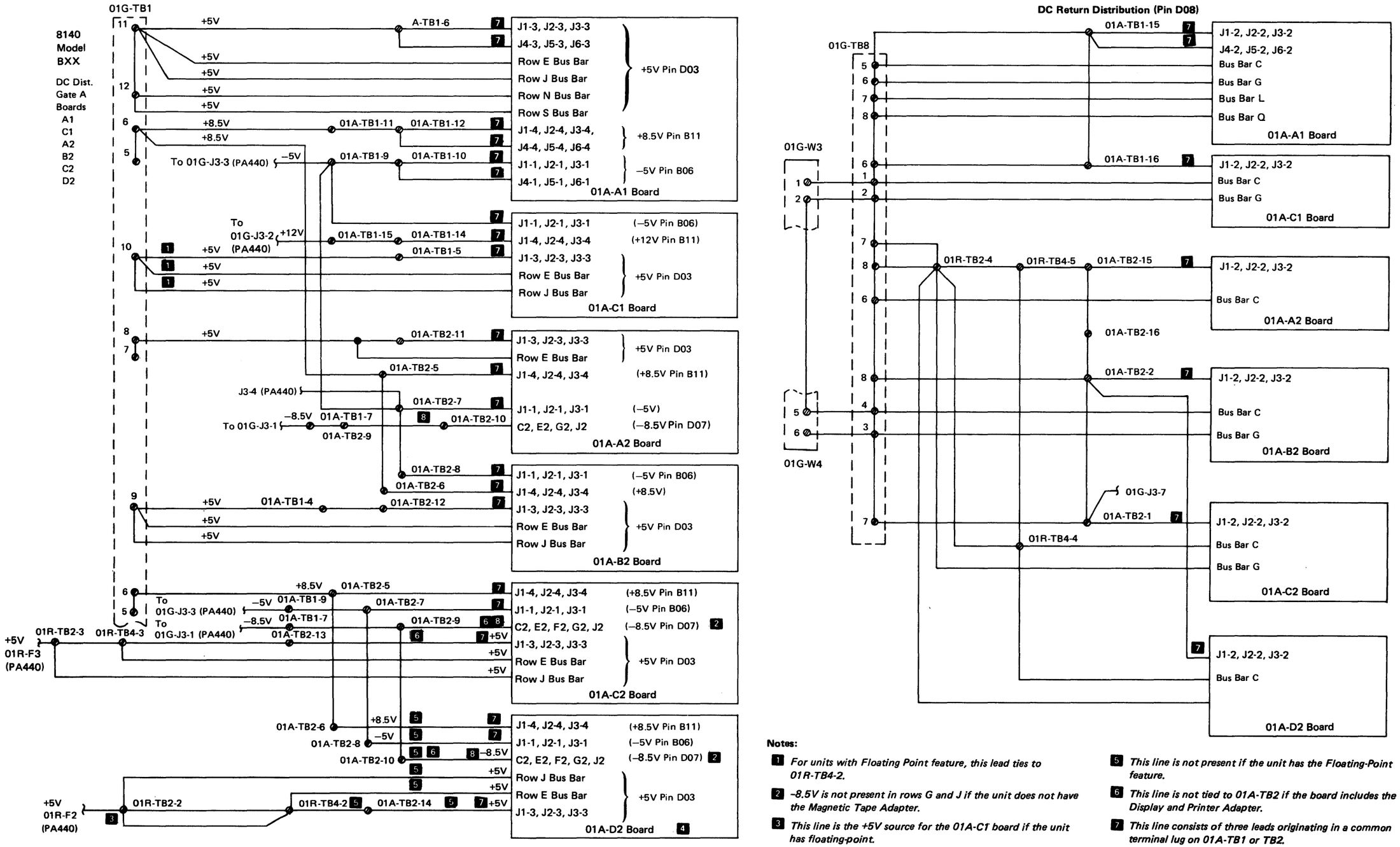
**Figure PA442-1 (Part 2 of 2). 8140 Models AXX DC Distribution**




**Notes:**

1. *For additional wiring to 01G-TB1, see PA440.*
2. *For additional wiring to 01G-PC1, see PA440, PA452, and PA461.*
3. *For additional wiring to 01M-PC2, see PA440 and PA452.*
4. *For additional wiring to OP Panel, see PA452.*
5. *For additional wiring to P2/J2, P4/J4, P6/J6, and P15/J15, see PA440.*
6. *For additional wiring to P1/J1, see PA452.*
7. *For additional wiring to K50, see PA412, PA422 and PA432.*
8. *For additional wiring to PC50, see PA440.*

**Figure PA442-2 (Part 1 of 2). 8140 Models BXX DC Distribution**







**Notes:**

1. *For units with Floating Point feature, this lead ties to 01R-TB4-2.*
2. *–8.5V is not present in rows G and J if the unit does not have the Magnetic Tape Adapter.*
3. *This line is the +5V source for the 01A-C1 board if the unit has floating-point.*
4. *This board is not present if the unit has the Floating-Point feature.*
5. *This line is not present if the unit has the Floating-Point feature.*
6. *This line is not tied to 01A-TB2 if the board includes the Display and Printer Adapter.*
7. *This line consists of three leads originating in a common terminal lug on 01A-TB1 or TB2.*
8. *This line consists of two leads originating in a common terminal lug on 01A-TB2.*

**Figure PA442-2 (Part 2 of 2). 8140 Models BXX DC Distribution**

*PA443 8101 DC Distribution*

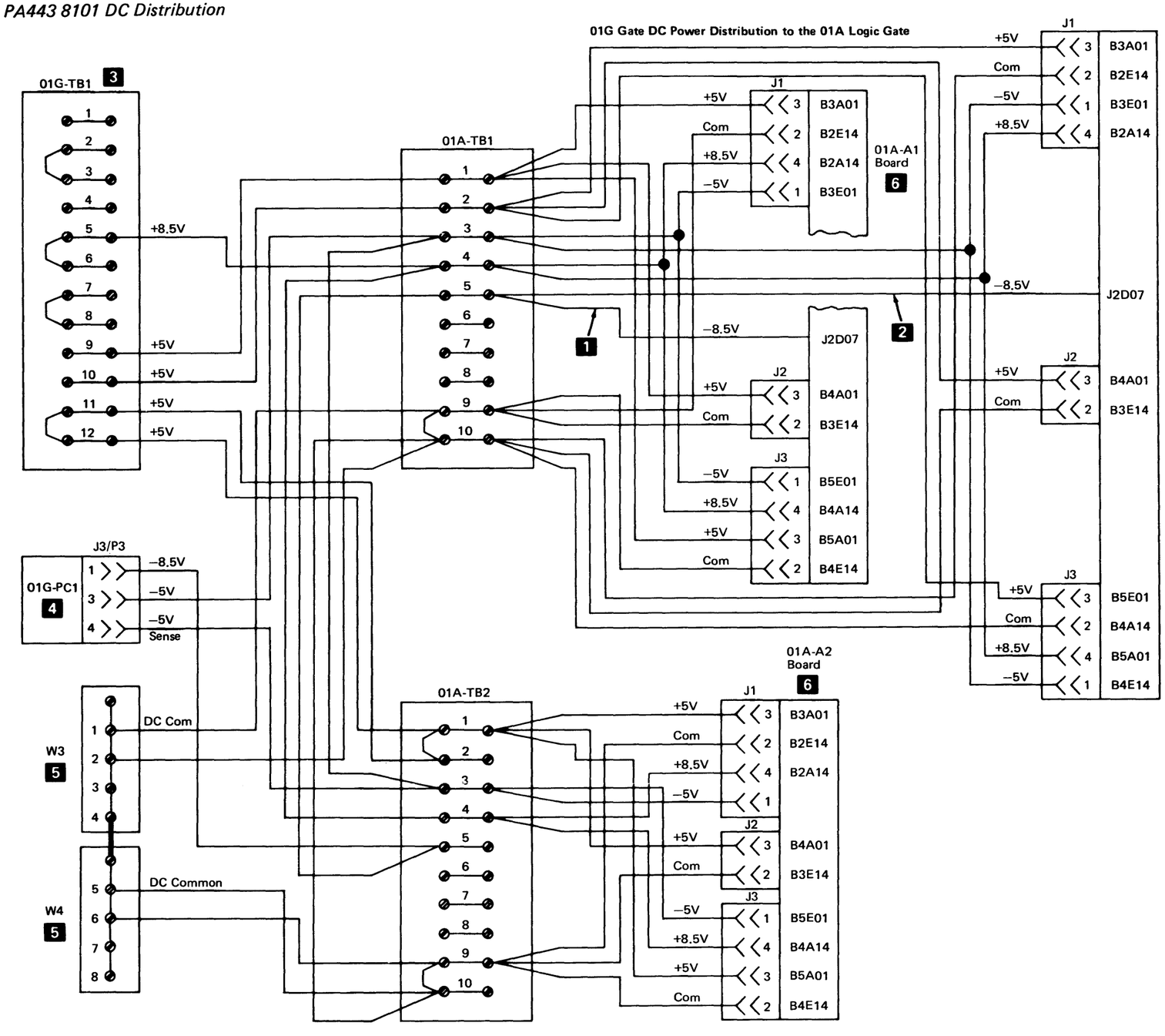
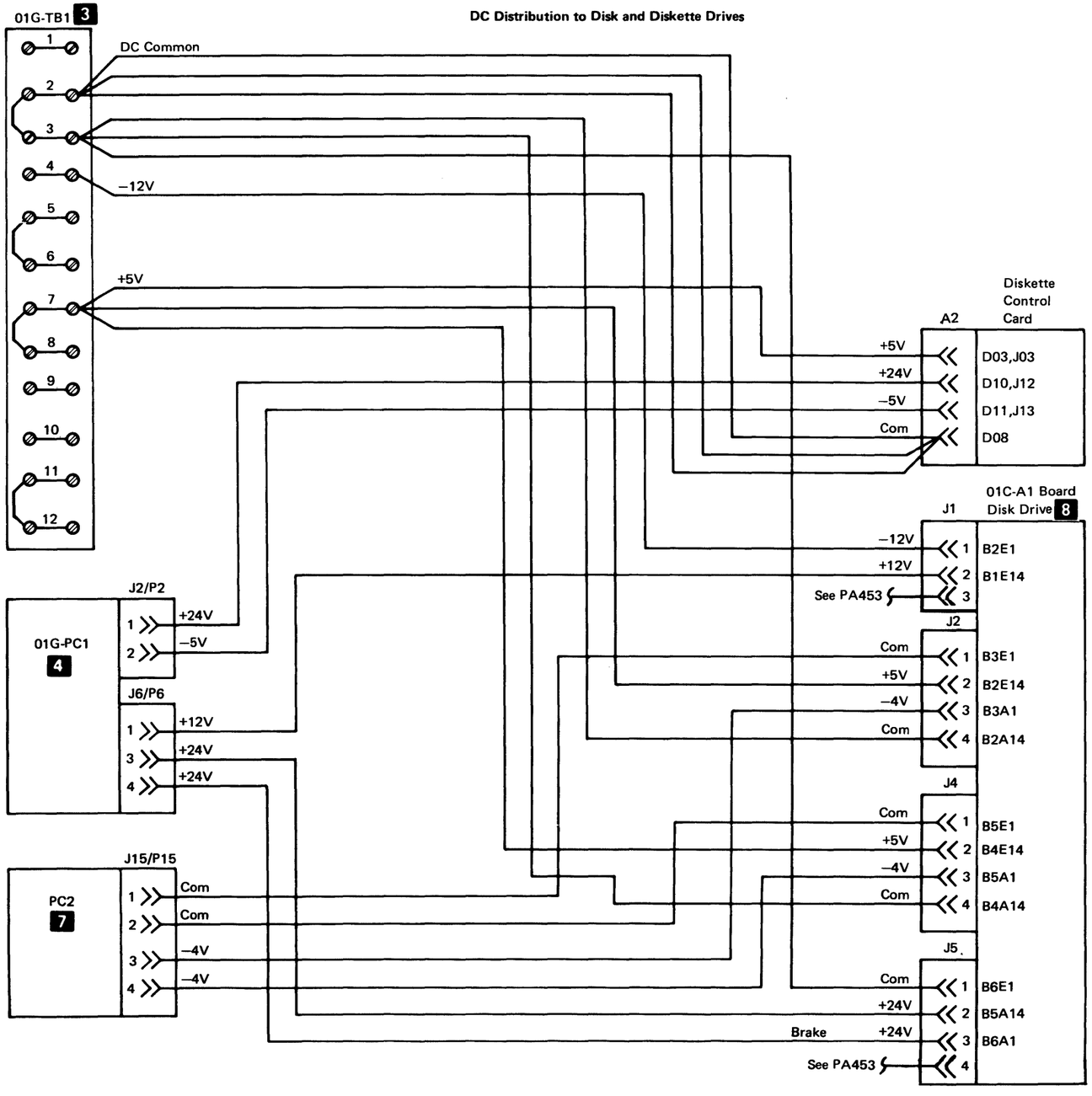



**Figure PA443-1 (Part 1 of 2). 8101 Models A1X, A20, and A23 DC Distribution**

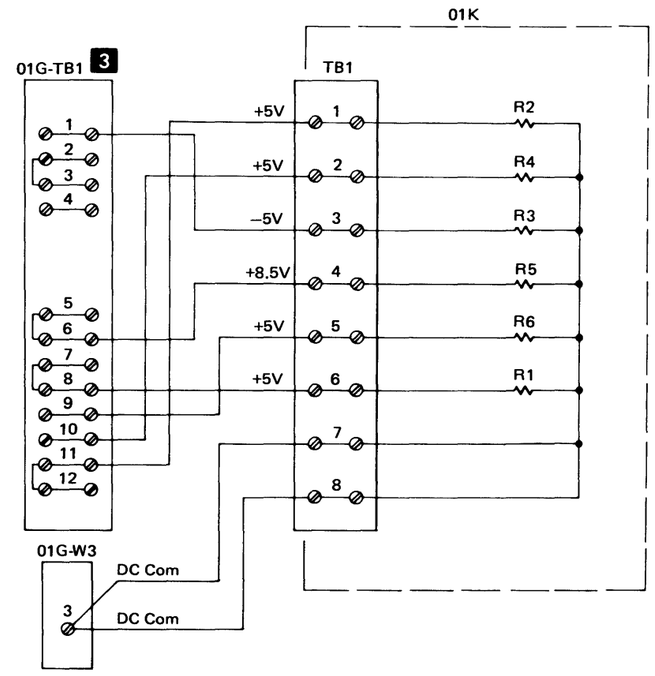
**Notes:**

1. *Required when code 9943 or 1503 is intalled (communication ports 1-4).*
2. *Required when code 1504 is installed (communication ports 5-8).*
3. *For additional wiring to TB1, see PA440.*
4. *For additional wiring to PC1, see PA440, PA453.*
5. *For additional wiring to 01G-W3, W4, see PA440.*
6. *For additional wiring to 01A-A1 and A2 boards, use PA453.*
7. *For additional wiring to 01G-PC2, see PA440 and PA453.*
8. *For additional wiring to 01C Disk Drive, see PA453.*
9. *For additional wiring to P2/J2, P3/J3, P4/J4, P6/J6, P15/J15, and P16/J16, see PA440.*
10. *For additional wiring to P1/J1, see PA453.*
11. *For additional wiring to P5/J5, see PA440, and PA453.*

**DC Distribution to Disk and Diskette Drives**




**DC Power – Resistor Box**




**Note:** *See PA743 for location.*

**Figure PA443-1 (Part 2 of 2). 8101 Models A1X, A20, and A23 DC Distribution**

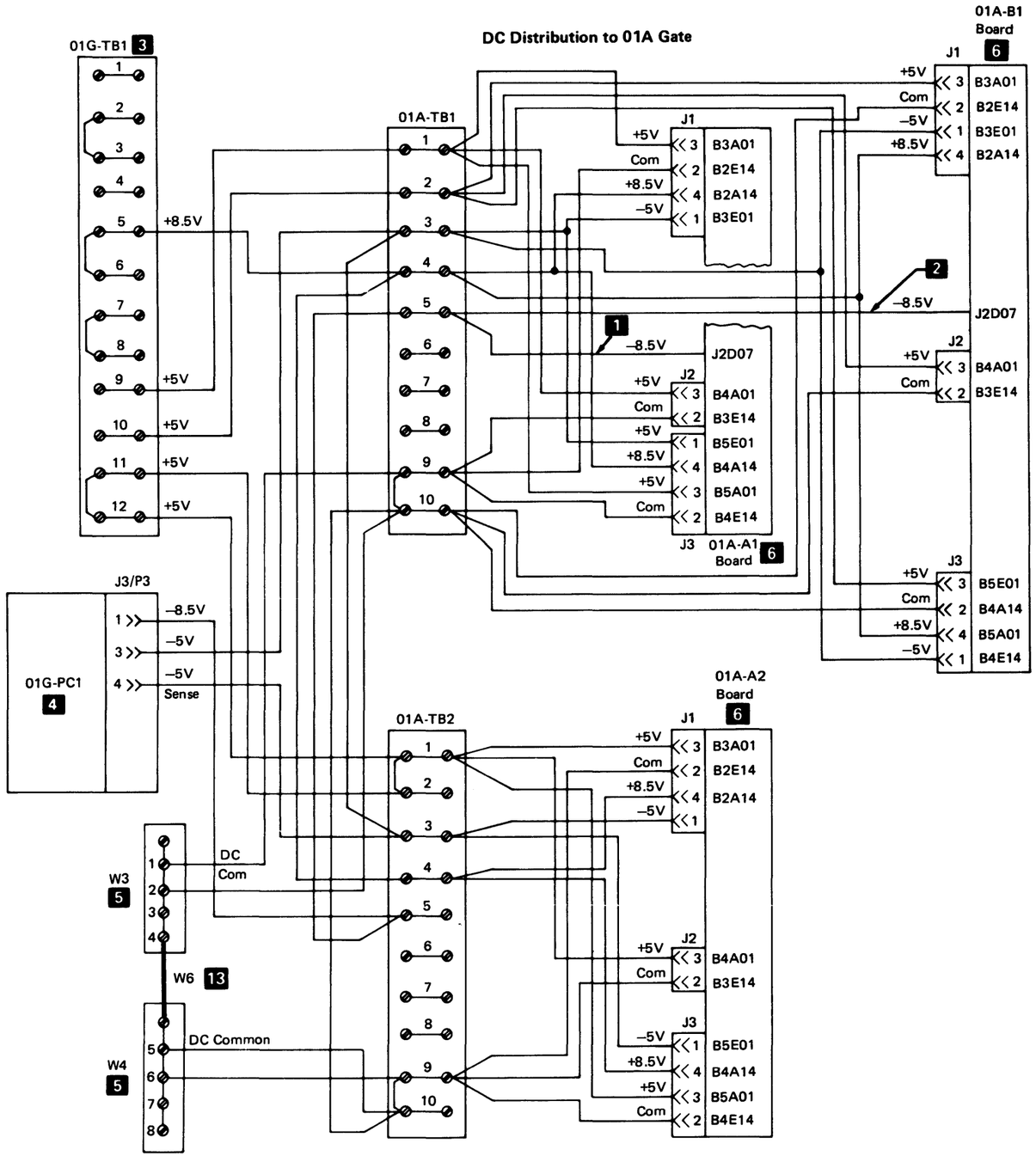
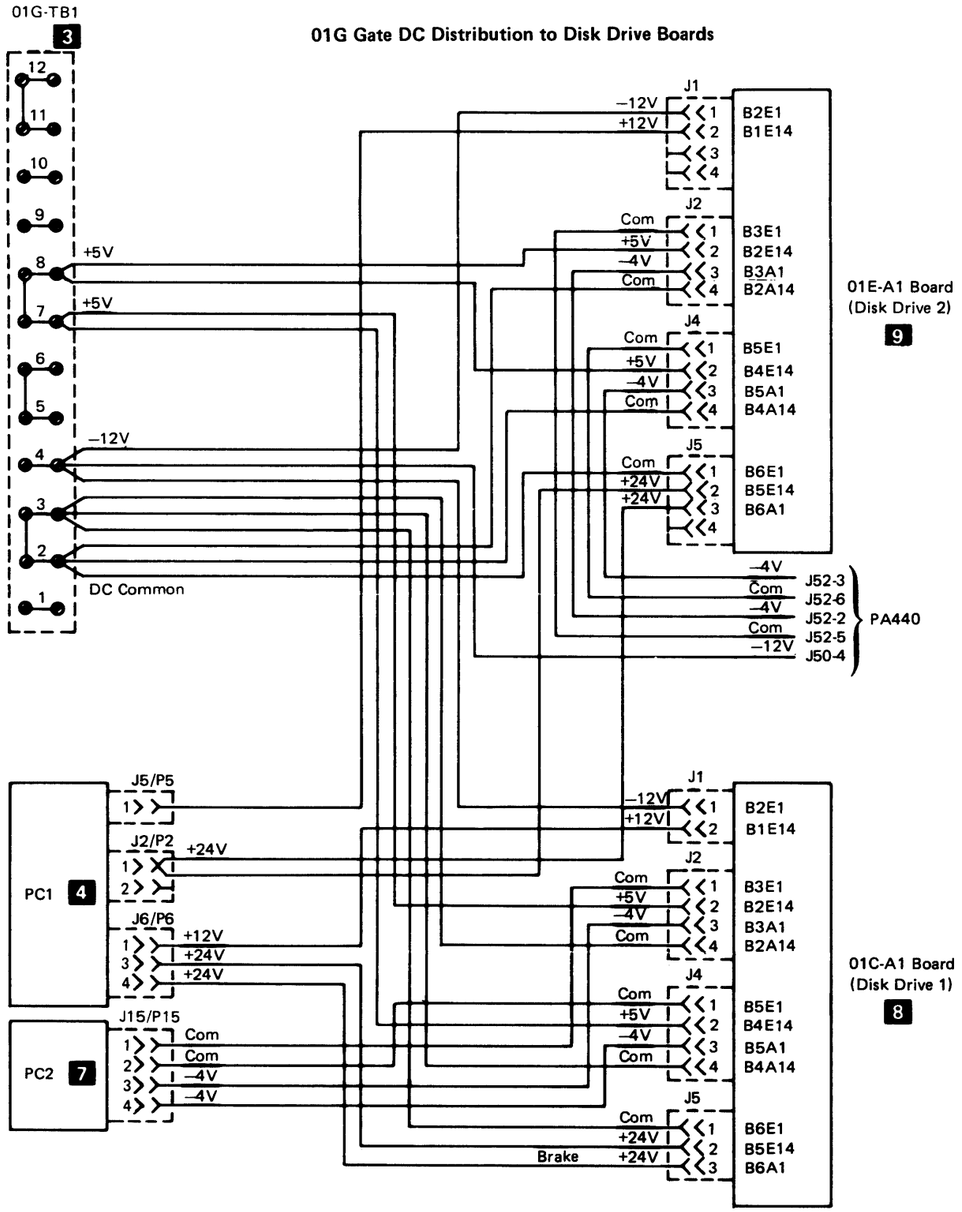



Figure PA443-2 (Part 1 of 2). 8101 Model A25 DC Distribution

**Notes:**

1. *Required when code 9943 or 1503 is installed (communication ports 1-4).*
2. *Required when code 1504 is installed (communication ports 5-8).*
3. *For additional wiring to TB1, see PA440.*
4. *For additional wiring to PC1, see PA440, PA453.*
5. *For additional wiring to 01G-W3, W4, see PA440.*
6. *For additional wiring to 01A-A1 and A2 boards, see PA453.*
7. *For additional wiring to 01G-PC2, see PA440, PA453.*
8. *For additional wiring to Disk Drive 1, see PA453.*
9. *For additional wiring to Disk Drive 2, see PA453.*
10. *For additional wiring to W3, see PA440.*
11. *For additional wiring to P1/J1, and P5/J5, see PA453.*
12. *For additional wiring to P2/J2, P3/J3, P4/J4, P6/J6, and P15/J15, see PA440.*
13. *Present with EC867485 installed.*



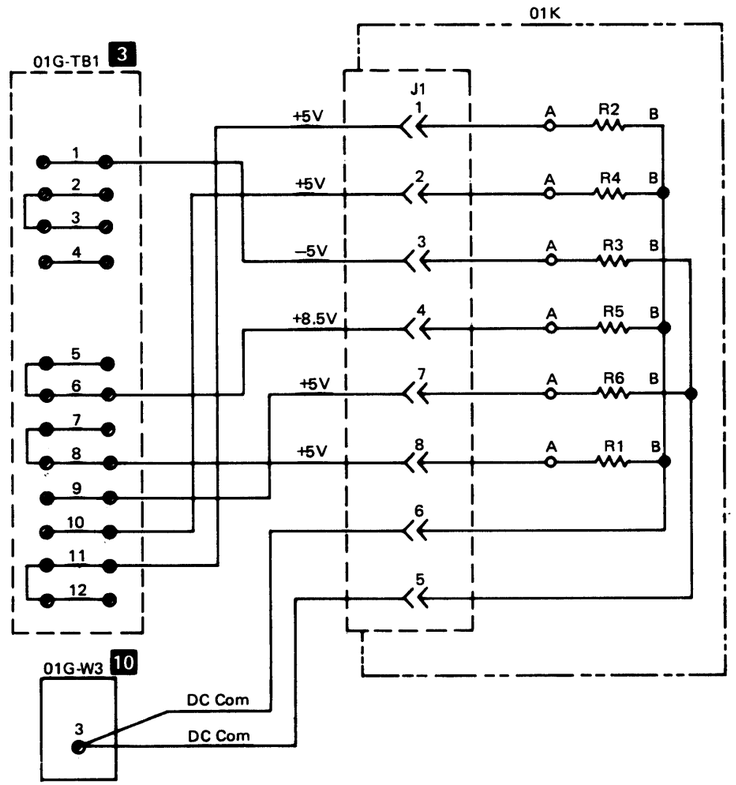
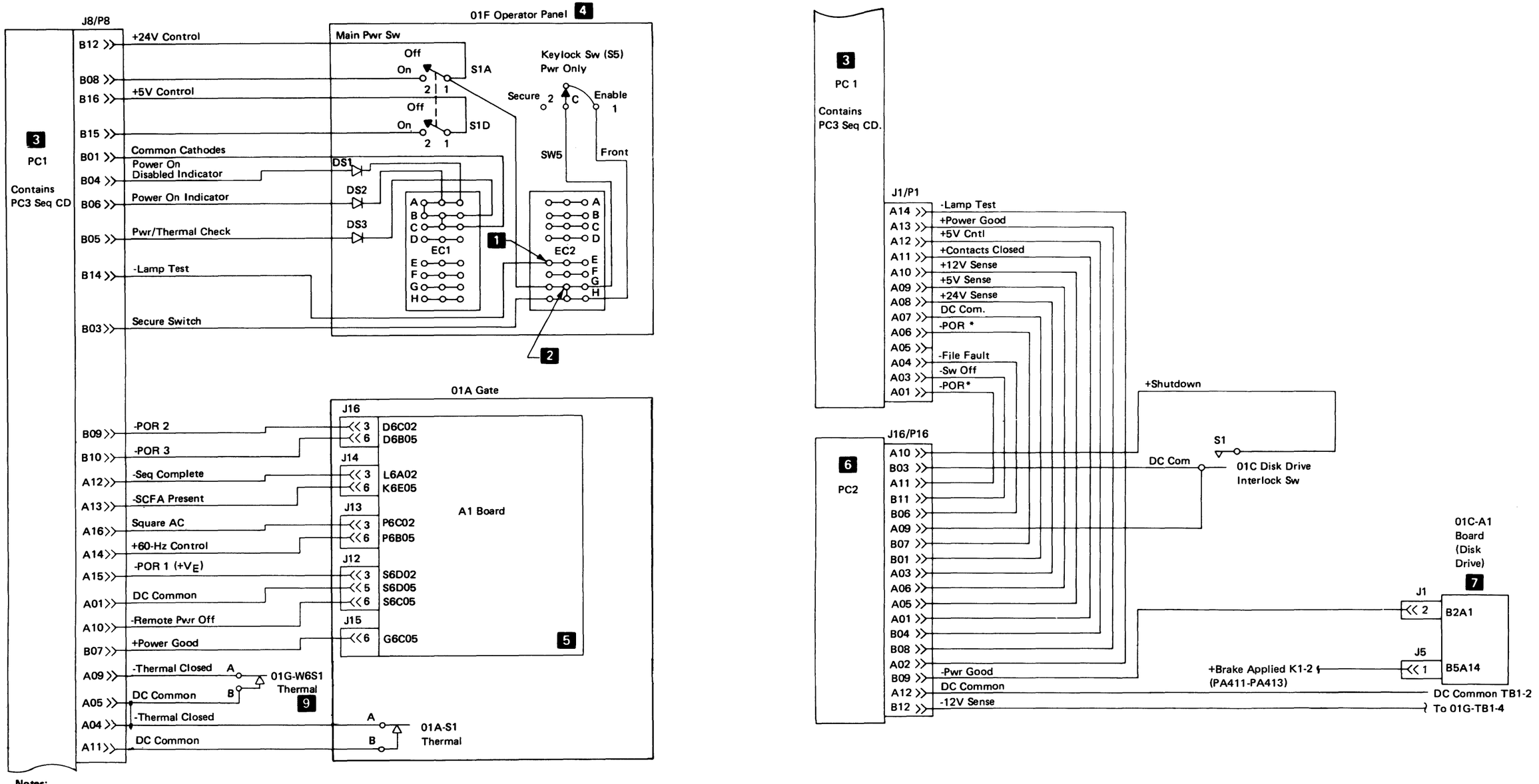




Figure PA443-2 (Part 2 of 2). 8101 Model A25 DC Distribution

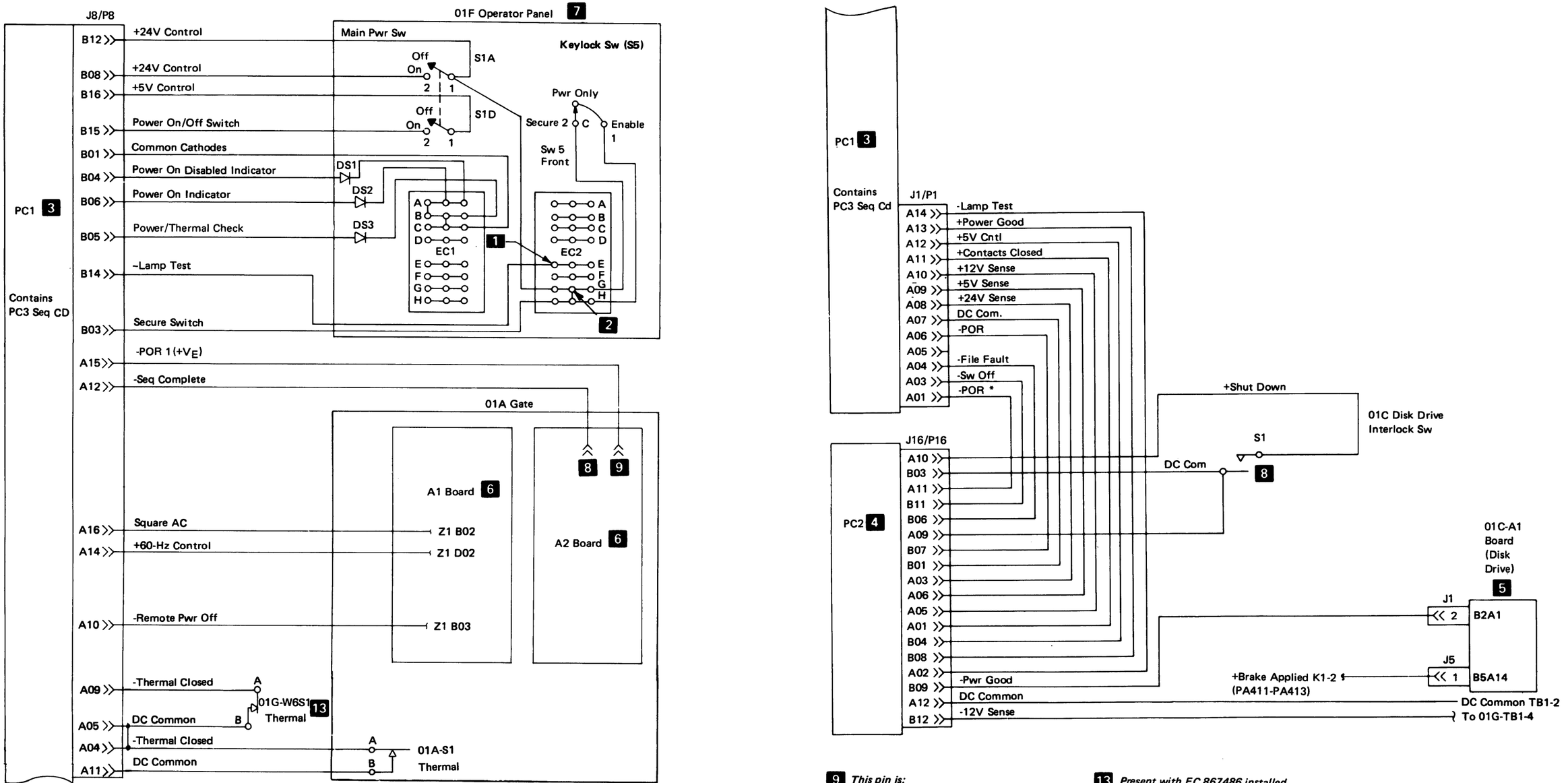
## PA450 Power Logic Interconnections

*PA451 8130 Power Logic Interconnections*




**Notes:**

1. *This point connected to ground for lamp test.*
2. *EC2-G is jumpered to EC2-H if keylock SW is not present.*
3. *For additional wiring to PC1, see PA440 and PA441.*
4. *For additional wiring to 01F BOP, see PA441.*
5. *For additional wiring to 01A-A1 board, see PA441.*
6. *For additional wiring to PC2, see PA440, PA441.*
7. *For additional wiring to 01C Disk Drive, see PA441.*
8. *For additional wiring to P1/J1 and P5/J5, see PA441.*
9. *Present with EC 321965 installed.*




**Notes:**

1. *This point connected to ground for lamp test.*
2. *EC2-G is jumpered to EC2-H if keylock SW is not present.*
3. *For additional wiring to PC1, see PA440, PA442.*
4. *For additional wiring to PC2, see PA440, PA442.*
5. *For additional wiring to 01C Disk Drive, see PA442.*
6. *For additional wiring to 01A-A1, A2 boards, see PA442.*
7. *For additional wiring to Op Panel, see PA442.*
8. *This pin is:*

| -Seq Comp | Models |
|---|---|
| H6A04 (Z3B02) | A3X, A4X |
| A6D04 (Z1B02) | A5X |

9. *This pin is:*

| -POR 1 ($V_E$) | Models |
|---|---|
| H6B04 (Z3B03) | A3X, A4X |
| A6E04 (Z1B03) | A5X |
| E6A04 (Z2B03) | A6X, A7X |

10. *For additional wiring to P1/J1, see PA442.*
11. *For additional wiring to P16/J16, see PA440.*
12. *For additional wiring to P5/J5, see PA440 and PA442.*
13. *Present with EC 867486 installed.*

**Figure PA452-1. 8140 Models AXX Power Logic Interconnections**

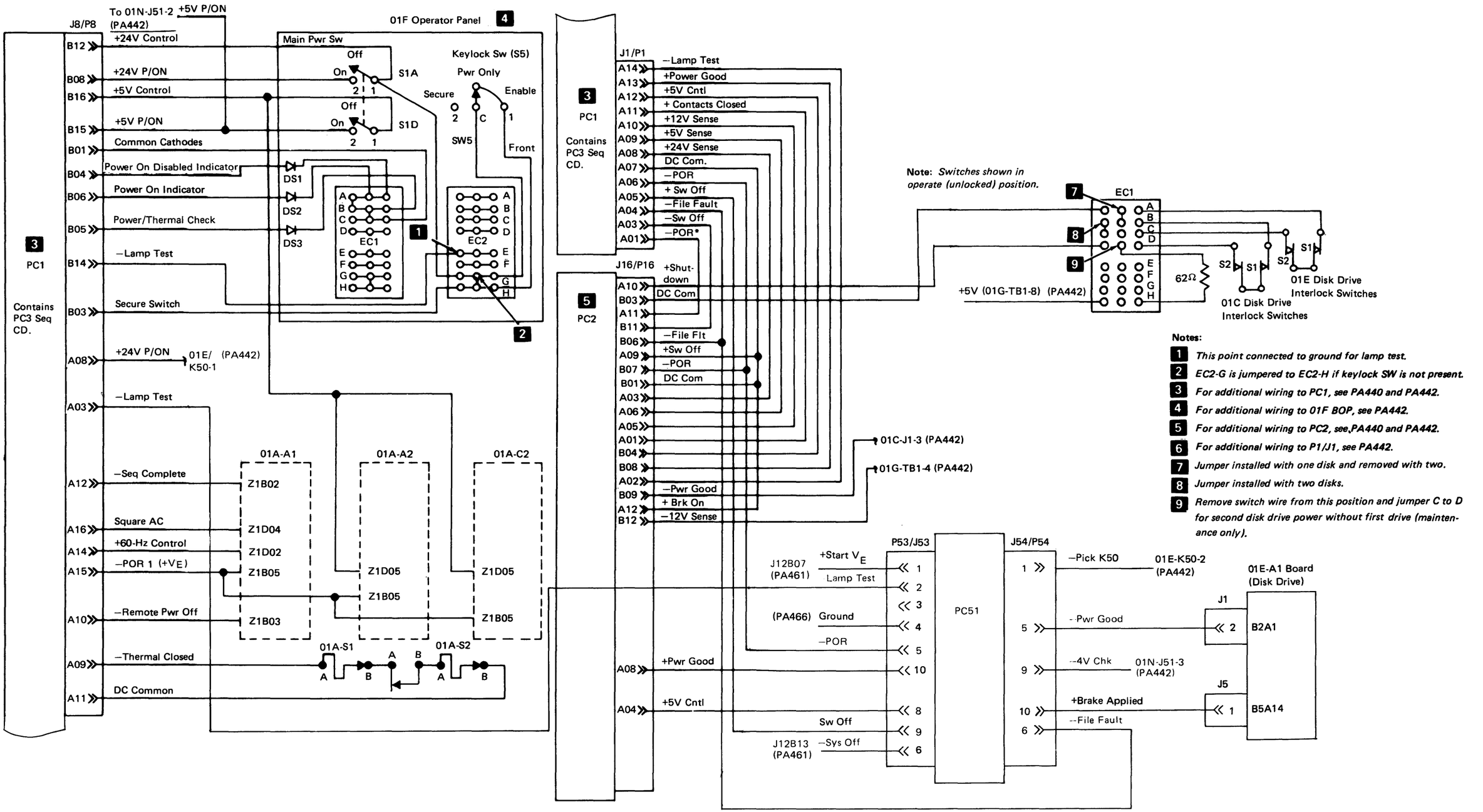



Figure PA452-2. 8140 Models BXX Power Logic Interconnections

*PA453 8101 Power Logic Interconnections*

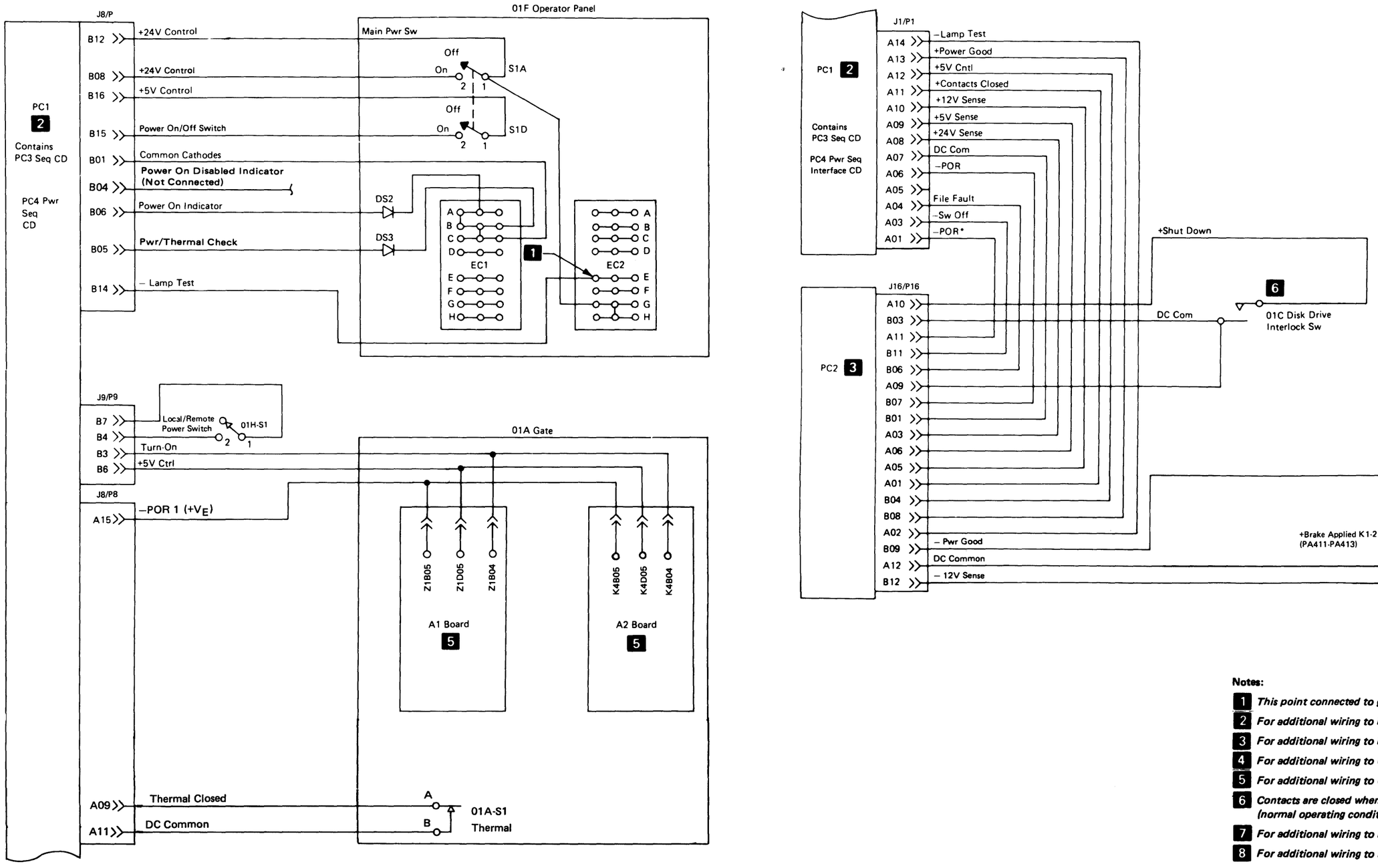



**Figure PA453-1. 8101 Models A1X, A20, and A23 Power Logic Interconnections**

**Notes:**

1. *This point connected to ground for lamp test.*
2. *For additional wiring to PC1, see PA440, PA443.*
3. *For additional wiring to PC2, see PA440, PA443.*
4. *For additional wiring to 01C Disk Drive, see PA443.*
5. *For additional wiring to 01A-A1 and A2 boards, see PA443.*
6. *Contacts are closed when Disk Drive heads are unlocked (normal operating condition).*
7. *For additional wiring to P1/J1, see PA443.*
8. *For additional wiring to P5/J5, see PA440 and PA443.*

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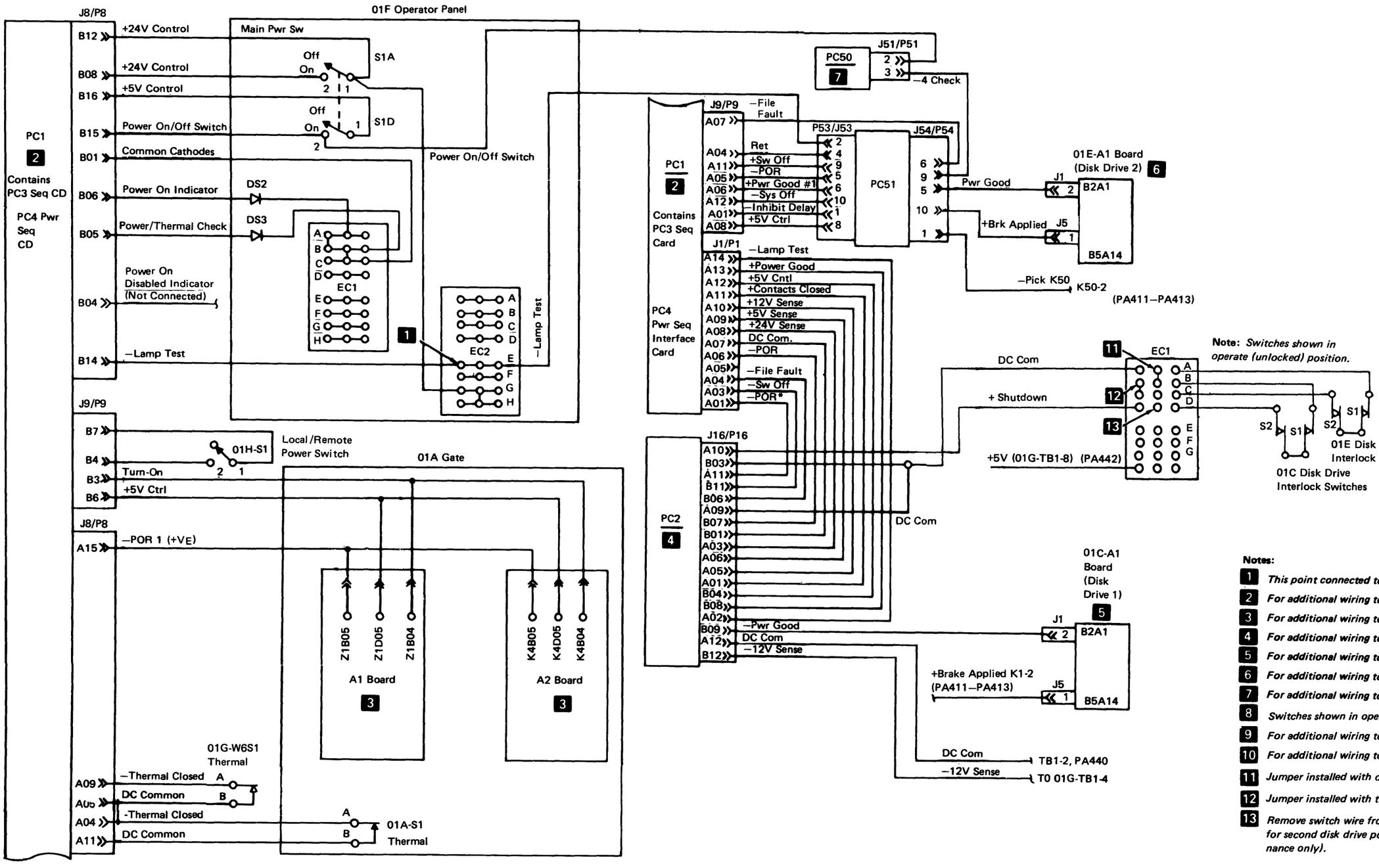


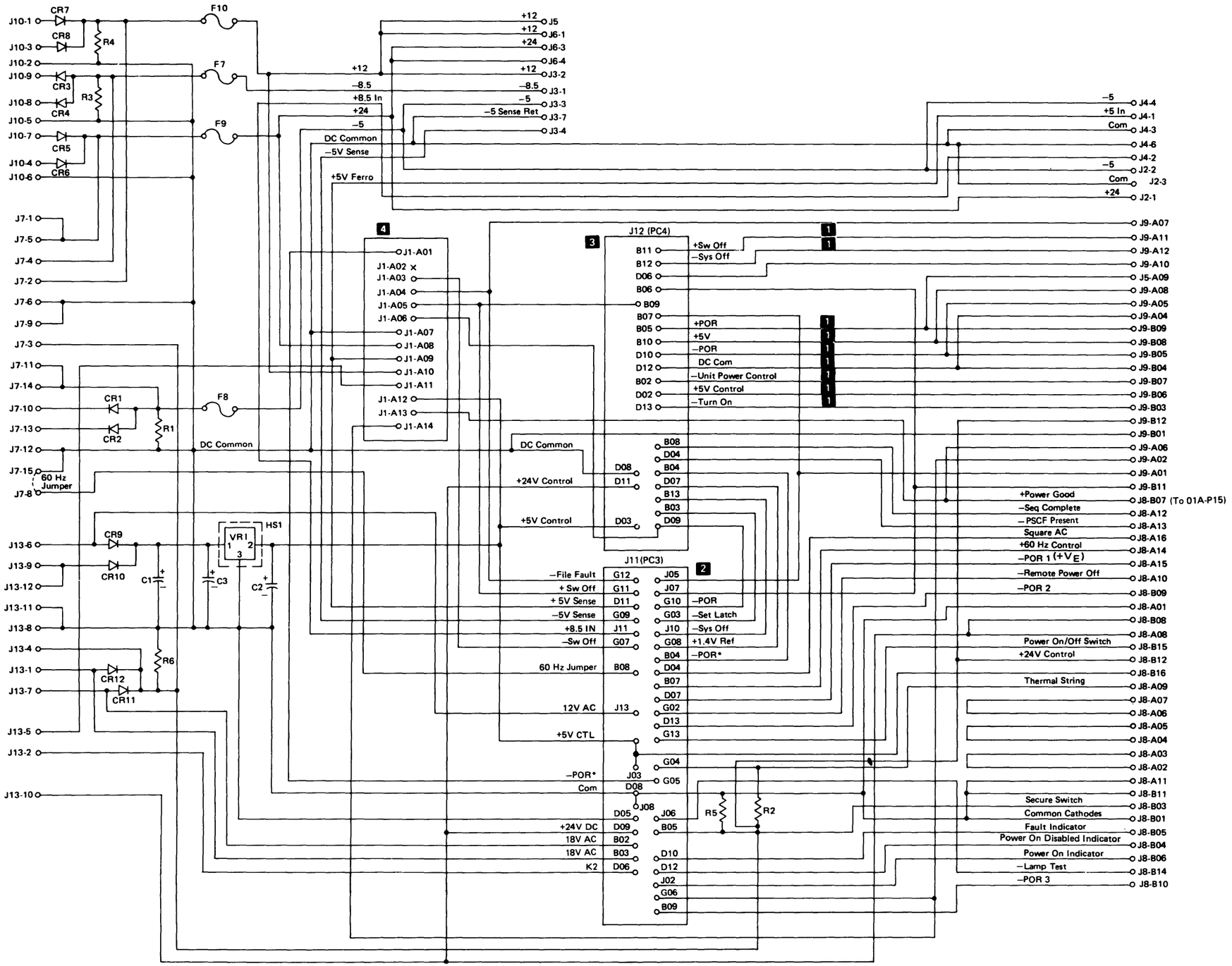

**Note:** *Switches shown in operate (unlocked) position.*

**Notes:**

1. *This point connected to ground for lamp test.*
2. *For additional wiring to PC1, see PA440, PA443.*
3. *For additional wiring to 01A, A1 and A2 boards, see PA443.*
4. *For additional wiring to PC2, see PA440, PA443.*
5. *For additional wiring to 01C Disk, see PA443.*
6. *For additional wiring to 01E Disk, see PA443.*
7. *For additional wiring to PC50, see PA440.*
8. *Switches shown in operate (unlocked) position.*
9. *For additional wiring to P1/J1 and P5/J5, see PA443.*
10. *For additional wiring to P16/J16, see PA440.*
11. *Jumper installed with one disk and removed with two.*
12. *Jumper installed with two disks.*
13. *Remove switch wire from this position and jumper C to D for second disk drive power without first drive (maintenance only).*

**Figure PA453-2. 8101 Model A25 Power Logic Interconnections**

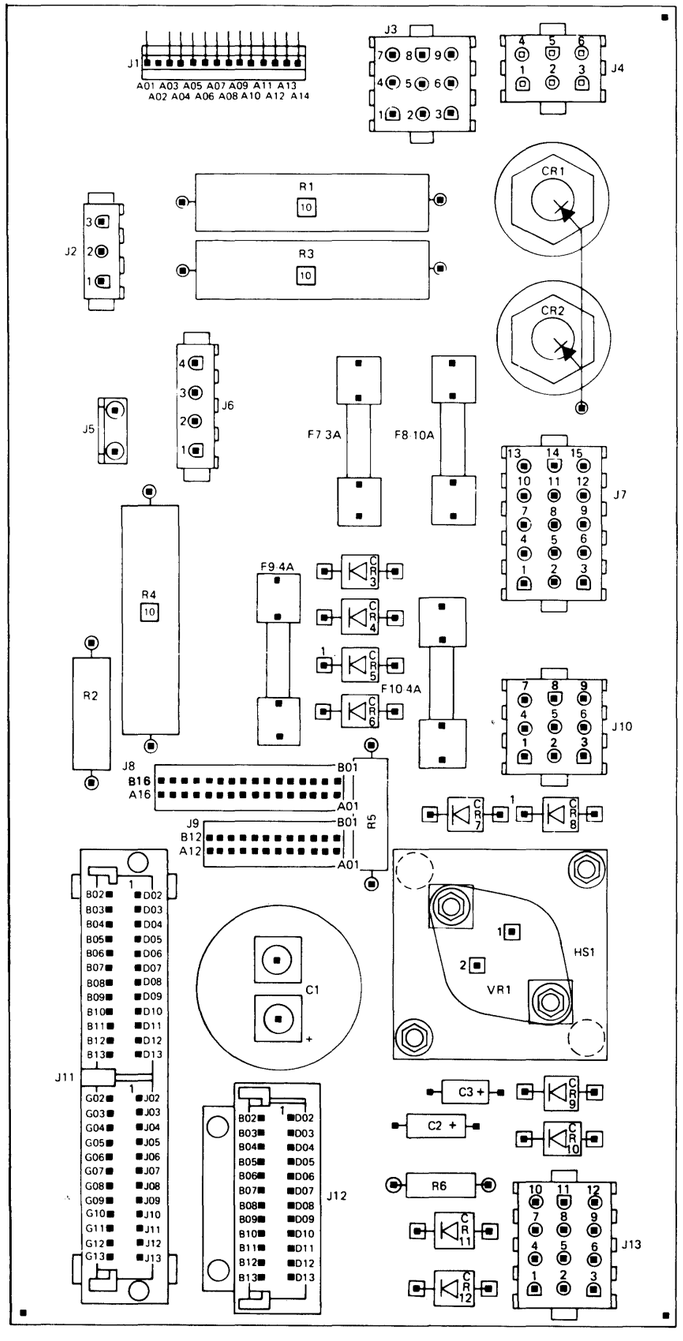
*PA461 PC-1 Power Card Assembly*




**A. PC-1 Power Card Diagram**

**Notes:**

1. *This signal used only in 8101.*
2. *PC-3 installs in J11.*
3. *PC-4 installs in J12 (8101 only).*
4. *See PA451-PA453.*

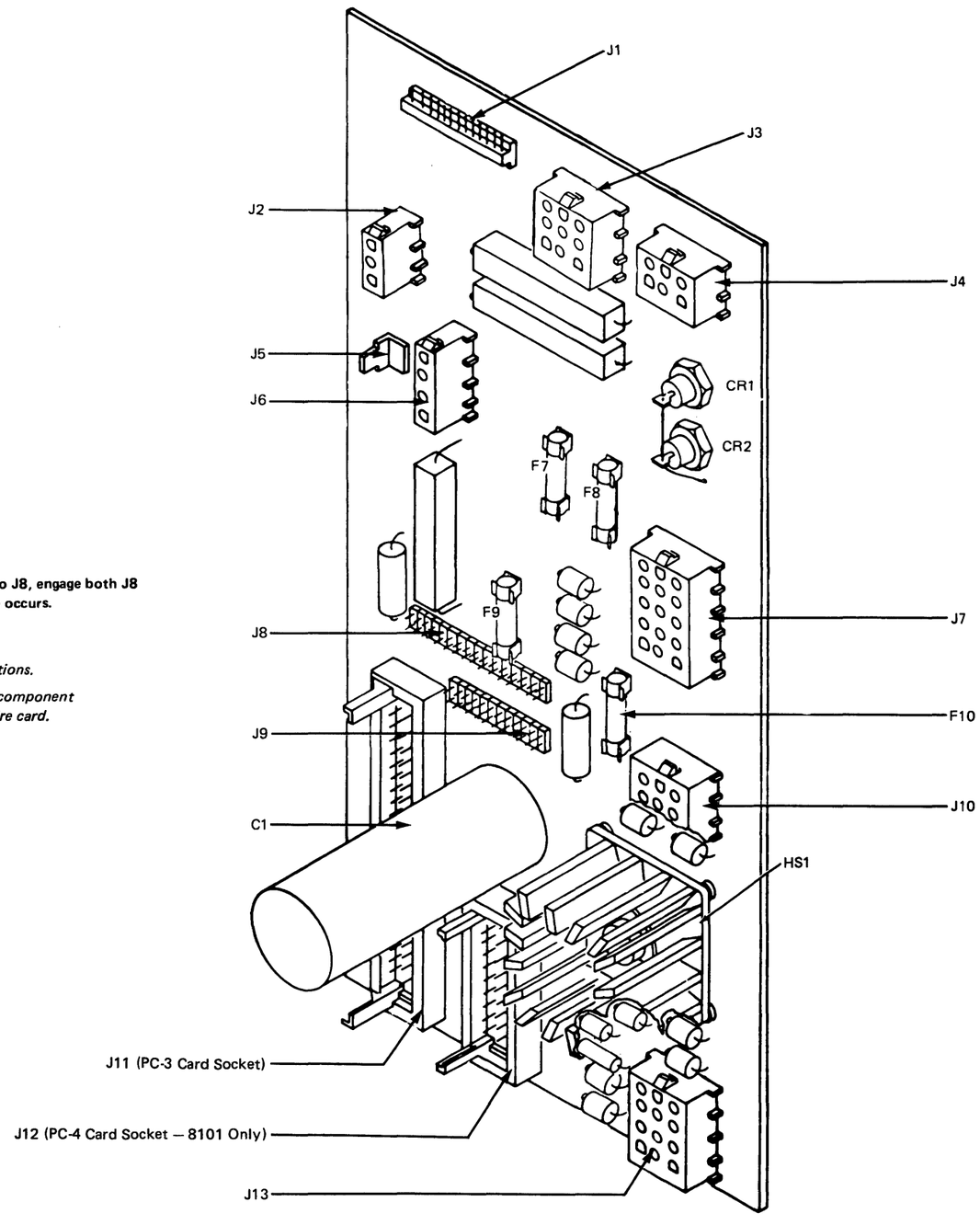



B. PC-1 Power Card Assembly Component Layout

**Caution: When connecting P8 to J8, engage both J8 pin rows, or component damage occurs.**

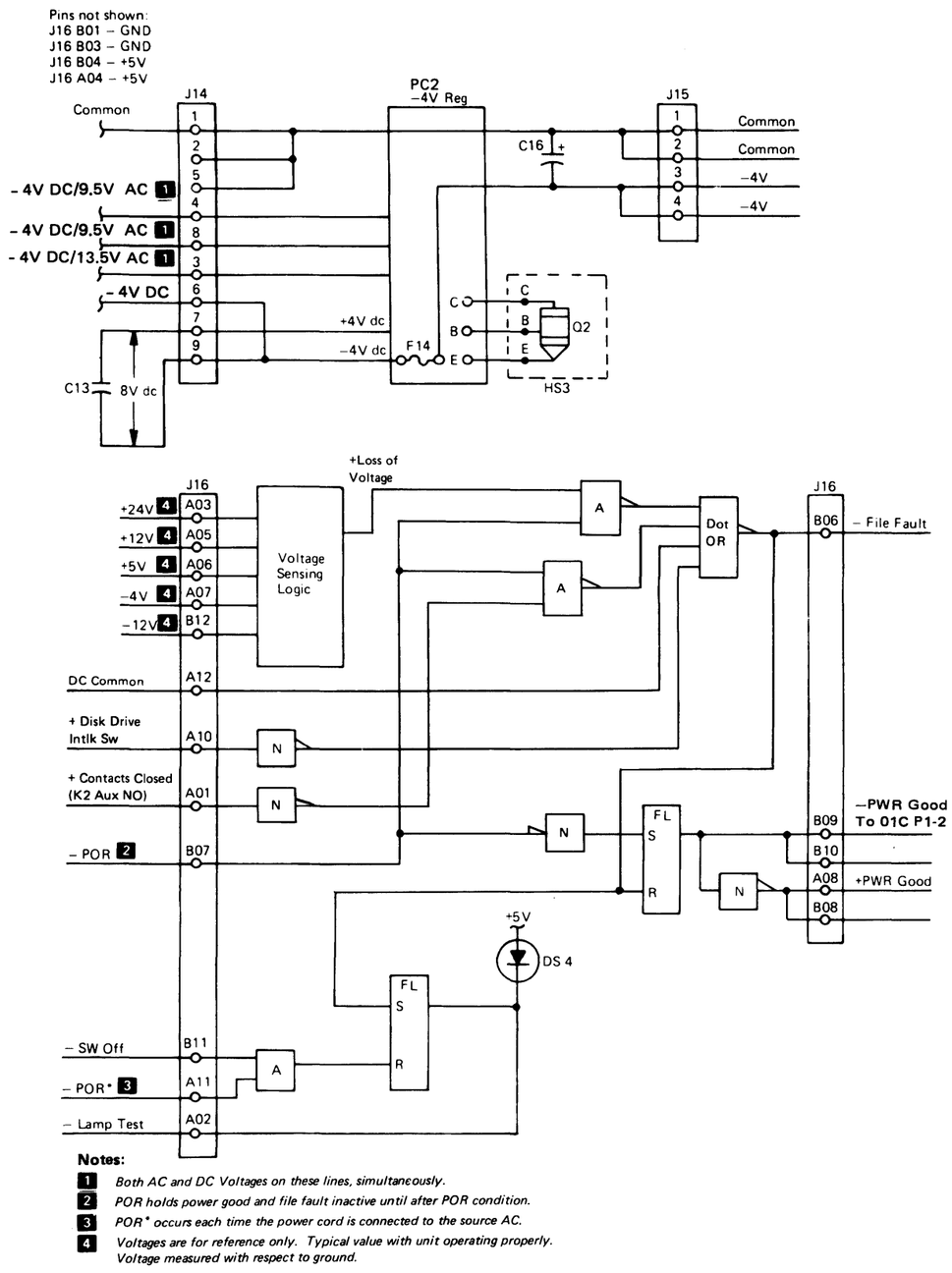
**Notes:**

1. *See PA650 for fuse specifications.*
2. *For any defective PC-1 card component except fuses, replace the entire card.*

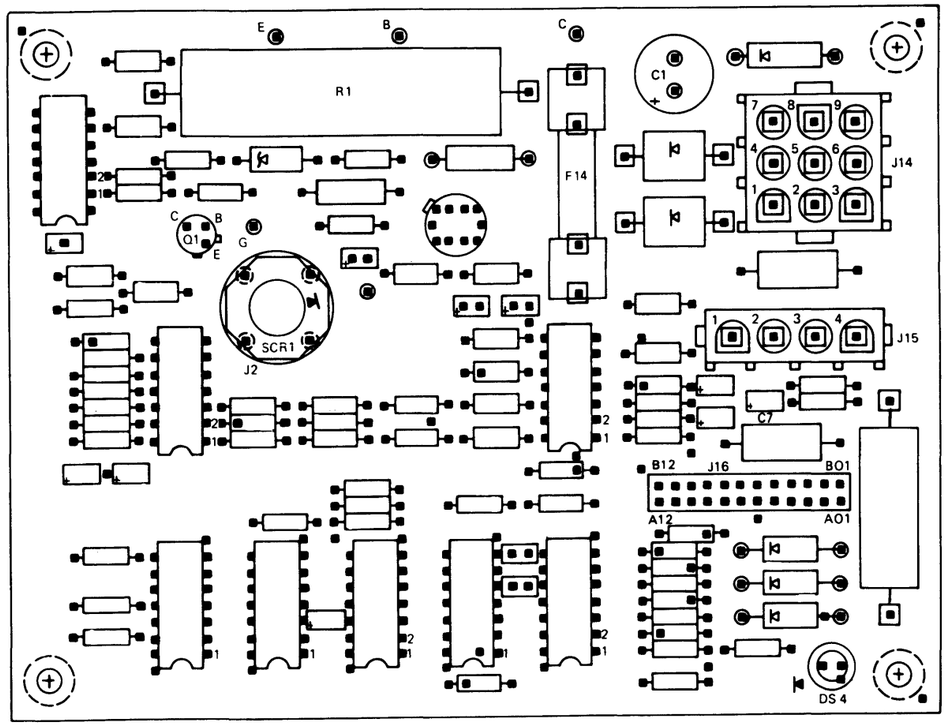



C. PC-1 Power Card Pictorial

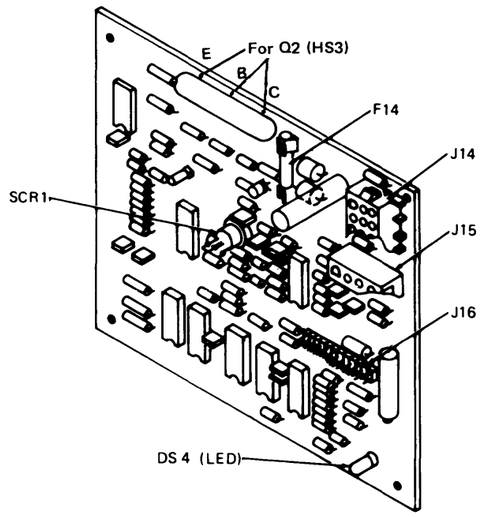
## *PA462 PC-2 First-Disk –4V Regulator and Sensing Logic Card*




**A. PC-2 Minus 4-Volt Regulator and Sensing Logic Card Diagram**




**B. PC-2 Minus 4-Volt Regulator Card Component Layout**

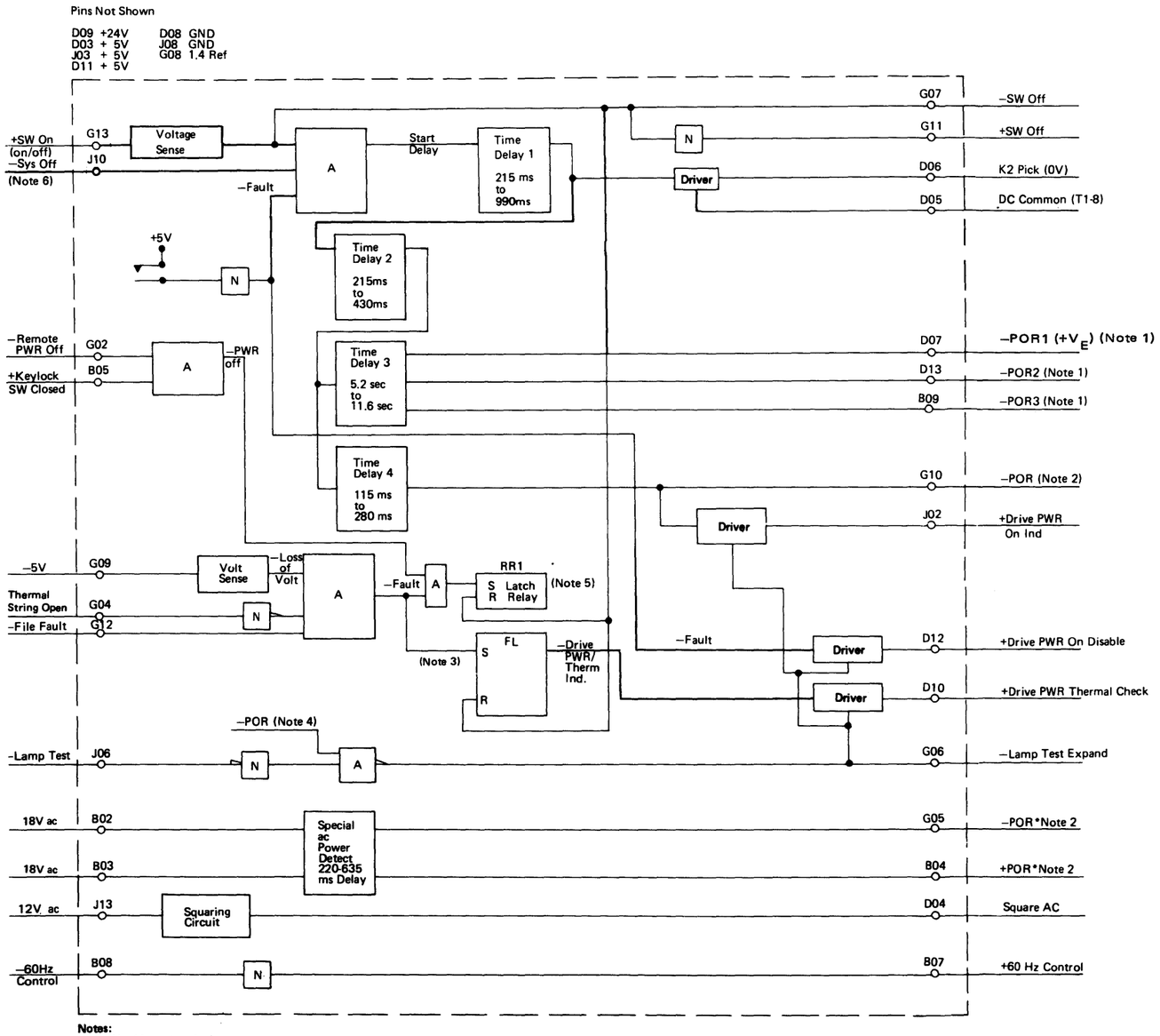



**C. PC-2 Minus 4-Volt Regulator Card Pictorial**

**Notes:**

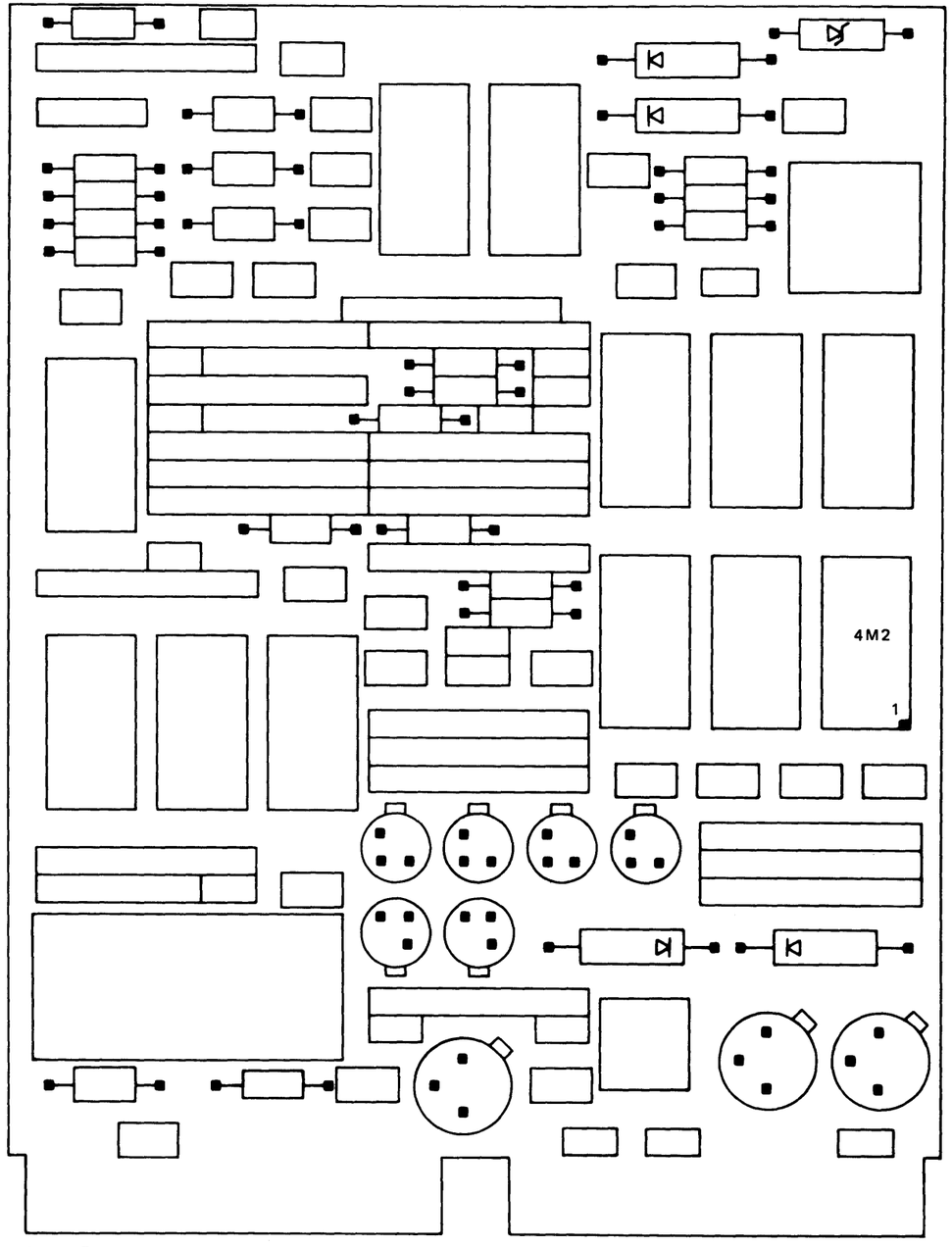
1. *See PA650 for fuse specification.*
2. *For any defective PC-2 card component except fuse F14, replace the entire card.*

## *PA463 PC-3 Power Sequence Card*




**Notes:**

1. *Used in system logic.*
2. *Used only in power system.*
3. *This circuit will drive one but not both indicators. The –Drive PWR/Thermal has priority if both signals are present.*
4. *Lamp test is degated by –POR.*
5. *This relay will latch in the set or reset state even if power is down.*
6. *See PA461 for J11 connections.*




**Note:** *For any defective PC-3 card component, replace the entire card.*

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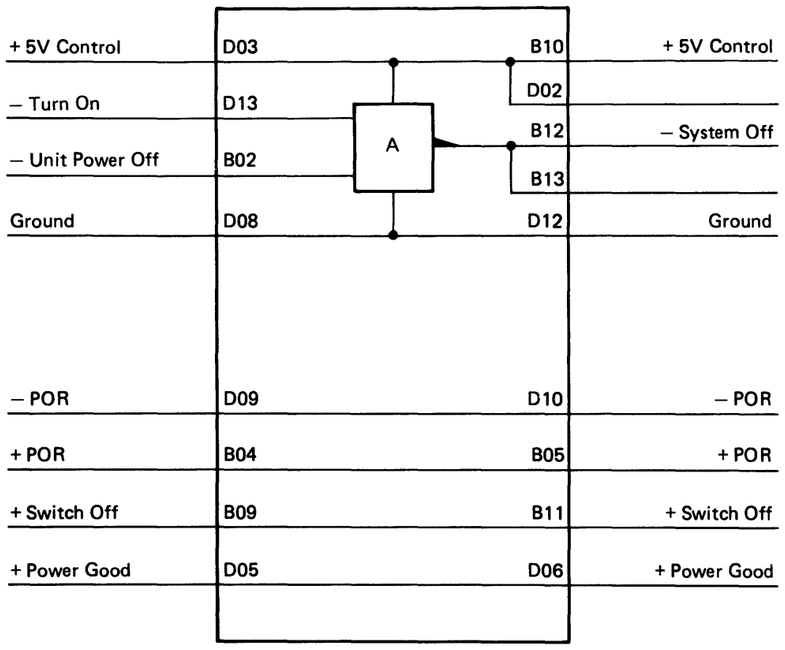
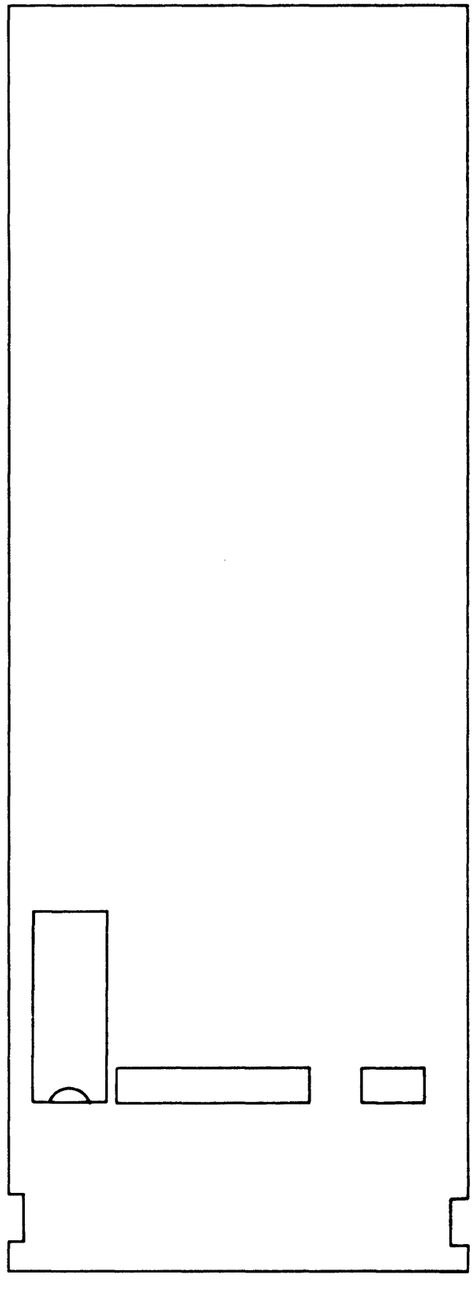
*PA464 PC-4 8101 Power Sequence Card*




**A. Logic Flow**

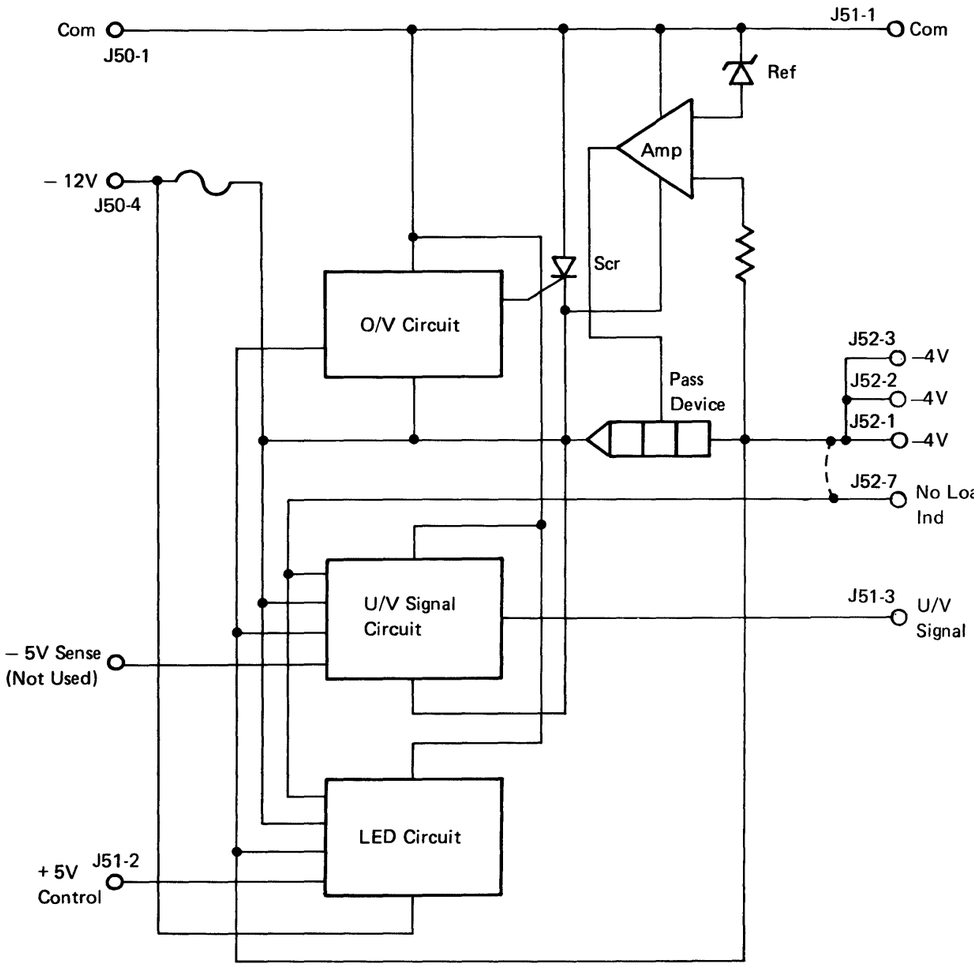
**Notes:**

1. *The PC-4 card is used in the 8101 only.*
2. *For any defective PC-4 card component, replace the entire card.*

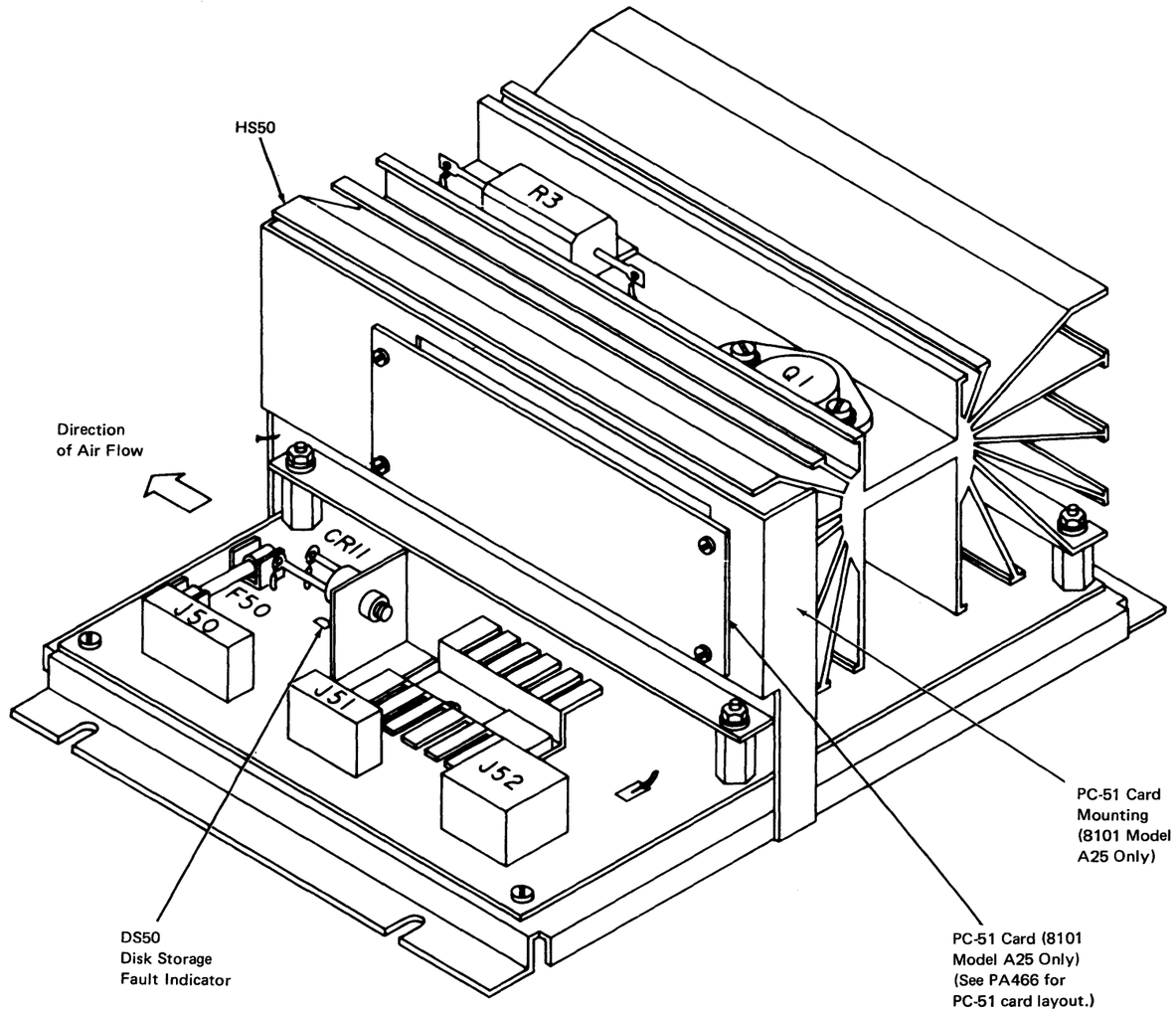


**B. Card Pictorial**

*PA465 PC-50 Second Disk -4V Regulator Card*



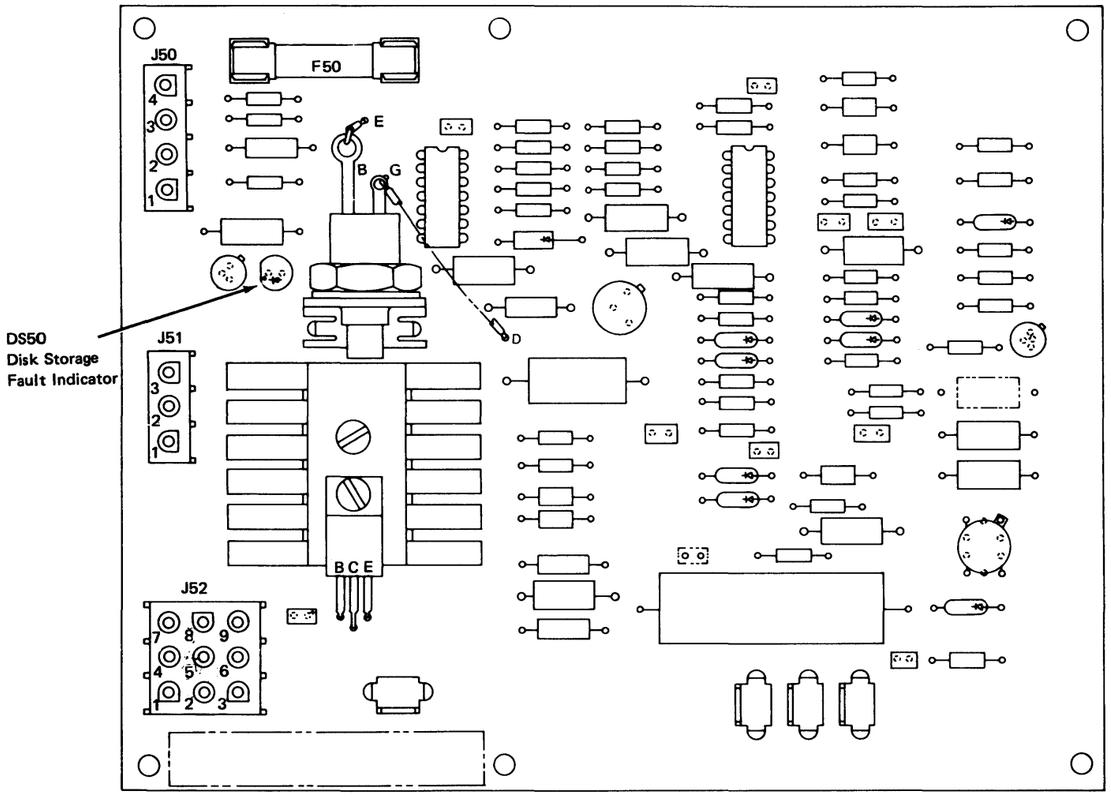

**A. PC-50 Card Logic Flow**




**Notes:**

1. *For any defective PC-50 card component except fuse F50, replace the entire card.*
2. *See PA650 for fuse specifications.*
3. *The PC-50 regulator assembly for the 8140 Models BXX is the same as for the 8101 Model A25 except that the PC-51 Card and its mounting are removed.*

**B. PC-50 Card Assembly**




C. PC-50 Card Pictorial

Figure PA465-1 shows the PC-50 card signals and voltage levels with the unit powered on and operating properly.

**Note:** *When probing VTL voltage levels, use the General Logic Probe (PN 453212) to verify line status; when probing an actual dc voltage level, use a voltmeter.*

If, after probing these lines:

- Any one input is incorrect, either the voltage source or distribution is the probable cause.
- Multiple inputs are incorrect, either the common voltage source or the PC-50 card is the probable cause.
- Some inputs and outputs are both incorrect, either the voltage input or the PC-50 card is the probable cause.
- One or more outputs are incorrect, PC-50 is probably defective.

If replacing the card does not fix the problem, either the voltage distribution or load could be the probable cause.

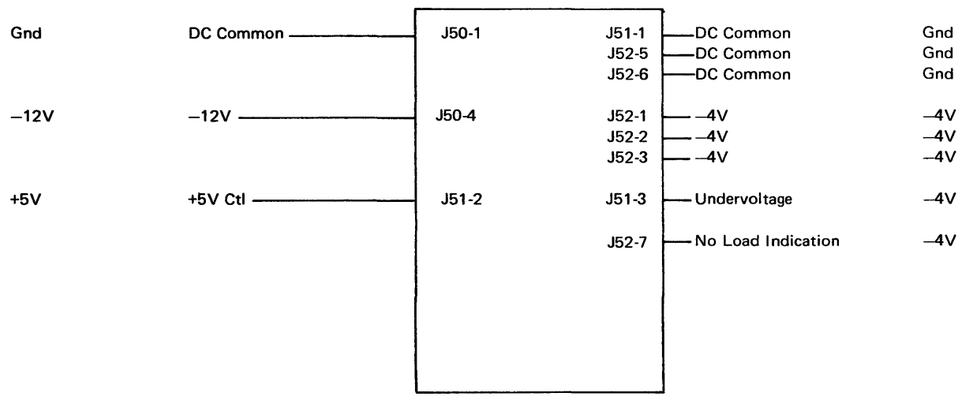
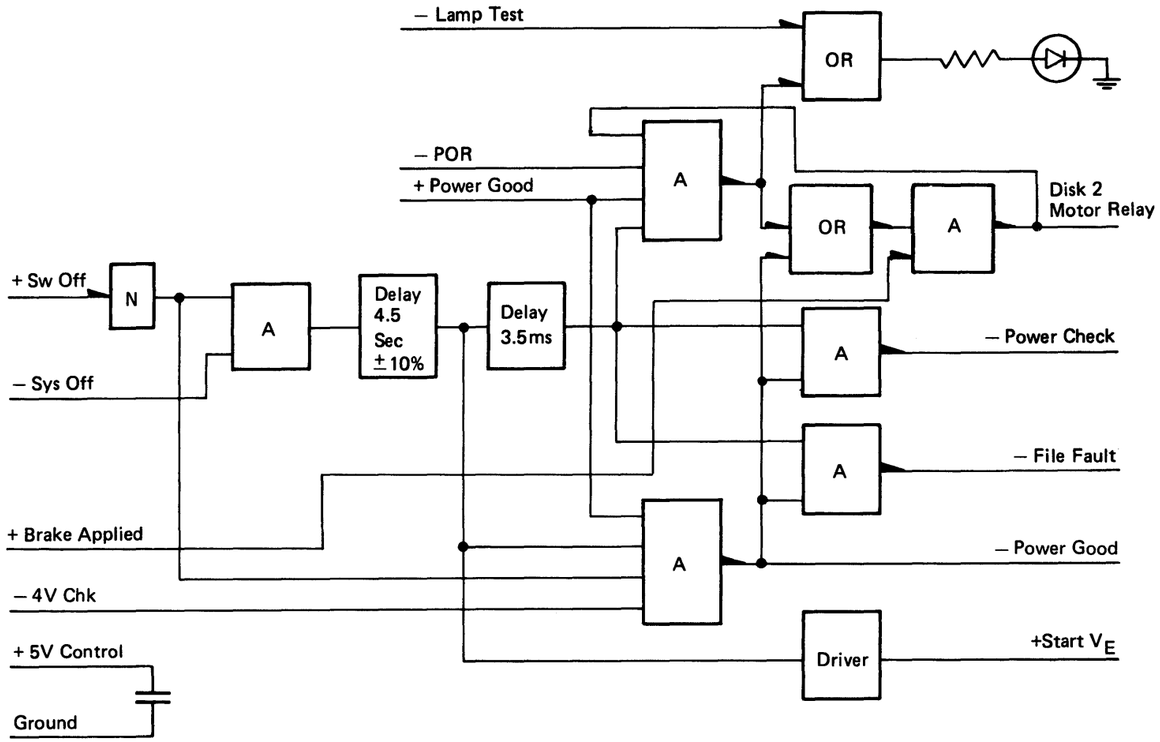
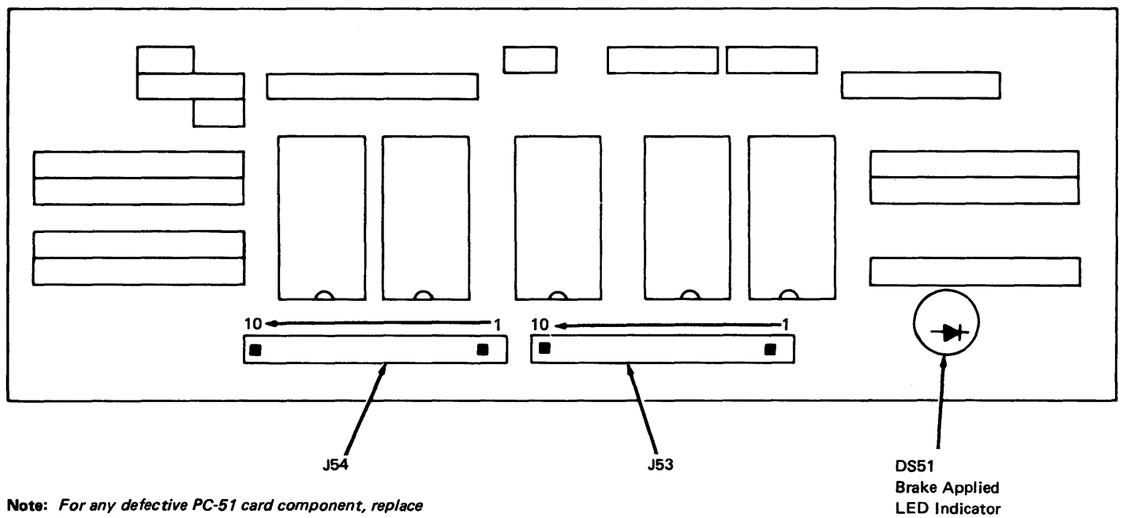



**Figure PA465-1. PC-50 Card Signals**

*PA466 PC-51 Second-Disk Control Card*




**A. Logic Flow**




**Note:** *For any defective PC-51 card component, replace the entire card.*

**B. Card Pictorial**

Figures PA466-1 and PA466-2 show the PC-51 card signals and voltage levels with the unit powered on and operating properly.

**Note:** *When probing VTL voltage levels, use the General Logic Probe (PN 453212) to verify line status; when probing an actual dc voltage level, use a voltmeter.*

If, after probing these lines:

- Any one input is incorrect, either the voltage source or distribution is the probable cause.
- Multiple inputs are incorrect, either the common voltage source or the PC-51 card is the probable cause.
- Some inputs and outputs are both incorrect, either the voltage input or the PC-51 card is the probable cause.
- One or more outputs are incorrect, PC-51 is probably defective.

If replacing the card does not fix the problem either the voltage distribution or load could be the probable cause.

| Input Voltage Level | Input Line Name | PC-51 Card | | Output Line Name | Output Voltage Level |
|---|---|---|---|---|---|
| +VTL | –Lamp Test | J53-2 | J53-1 | +Start $V_E$ | +VTL |
| Gnd | Ground | J53-4 | | | |
| +VTL | –Power On Reset | J53-5 | | | |
| +VTL | + Power Good | J53-10 | J54-5 | –Power Good | –VTL |
| +5V dc | + 5V Ctl | J53-8 | J54-6 | –File Fault | + VTL |
| –VTL | + Switch Off | J53-9 | | | |
| +VTL | –Sys Off | J53-6 | J54-10 | +Brake Applied | –VTL |
| –4V dc | –4V Check | J54-9 | J54-1 | –Pick K50 | –VTL |

**Figure PA466-1. 8140 Model BXX PC-51 Card Signals**

| Input Voltage Level | Input Line Name | PC-51 Card | | Output Line Name | Output Voltage Level |
|---|---|---|---|---|---|
| + VTL | –Lamp Test | J53-2 | J53-1 | + Start $V_E$ | + VTL |
| Gnd | Gnd | J53-4 | | | |
| + VTL | –Power On Reset | J53-5 | | | |
| + VTL | + Power Good | J53-6 | J54-5 | –Power Good | –VTL |
| + 5V dc | + 5V Ctl | J53-8 | J54-6 | –File Fault | + VTL |
| –VTL | + Switch Off | J53-9 | | | |
| + VTL | –Sys Off | J53-10 | J54-10 | +Brake Applied | –VTL |
| –4V dc | –4V Check | J54-9 | J54-1 | –Pick K50 | –VTL |

**Figure PA466-2. 8101 Model A25 PC-51 Card Signals**

## PA500 Adjustment, Removal, and Replacement Information

**DANGER**
**With the power cord connected to the wall outlet, line voltage and the +5 and +24 control voltages are always present in all:**

- **8130s, 8140 Models AXX, and 8101s.**
- **8140 Models BXX with the line voltage circuit breaker (CB1) on.**

**Before removing metal covers or internal power components (except for power control (PC) and logic cards), either (1) disconnect the power cord for all 8130s, 8140 Models AXX, and all 8101s, or (2) turn off CB1 for 8140 Models BXX.**

**Caution: To remove either power control (PC) or logic cards:**

1. **Place the operator panel power switch to the Off position.**
2. **Disconnect 01G-J8 from the PC-1 card.**

### PA510 +5V DC Adjustment

Before the customer receives the system, the factory adjusts the +5V dc level while having all devices connected to the system that use this voltage. As this is the only adjustable dc voltage, you should check all +5V dc outputs after adding or deleting any feature in the field. You can use your tool bag meter, (IBM PN 1749231 or equivalent) to make this adjustment but, if possible, use a Weston 201 meter for accuracy. Referring to Figure PA510-1, proceed as follows:

1. To measure the +5V, connect the positive meter lead to 01G L1-2 and the negative lead to 01G W3.

2. A voltage of from +5.15V to +5.25V dc is within tolerance and does not need adjustment; if out of tolerance, go to step 3.

   **Caution: Turn power off before moving the transformer leads.**

   **Note:** *Changing this +5V adjustment has some effect on other system voltages, but it should not cause an out of tolerance condition.*

3. Power off the machine at the operator panel.
4. Locate the T3 transformer leads marked 55 and 56 on 01G-TB6. Move both leads as necessary to adjust the +5V output according to the following chart. Moving both leads one position changes the +5V output approximately 0.1V. Adjust as close to 5.20V as possible.

| Lead 55 | Lead 56 | Comments |
|---|---|---|
| TB6-1 | TB6-4 | Minimum voltage level connections |
| TB6-1 | TB6-3 | |
| TB6-1 | TB6-2 | |
| TB6-1 | TB6-1 | Bypasses T3 through common connection |
| TB6-2 | TB6-1 | |
| TB6-3 | TB6-1 | |
| TB6-4 | TB6-1 | Maximum voltage level connections |

5. After moving the leads, power up and check the +5V output between each of the following points. All four outputs must be between 4.85V and 5.45V.

| +Lead | -Lead |
|---|---|
| 01G TB1-8 | 01G-W3 |
| 01G TB1-9 | 01G-W3 |
| 01G TB1-10 | 01G-W3 |
| 01G TB1-11 | 01G-W3 |

6. Check all other machine voltages (PA660).

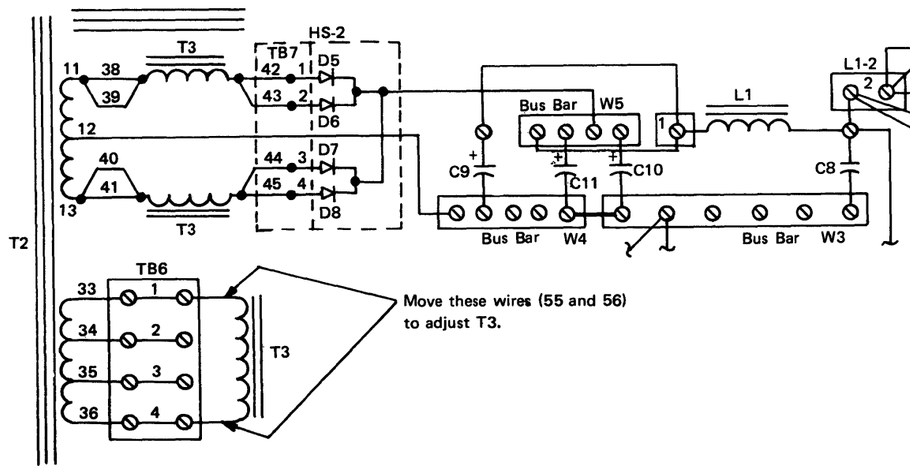



**Figure PA510-1. +5V DC Adjustment**

## PA520 LED Removal and Replacement Procedure

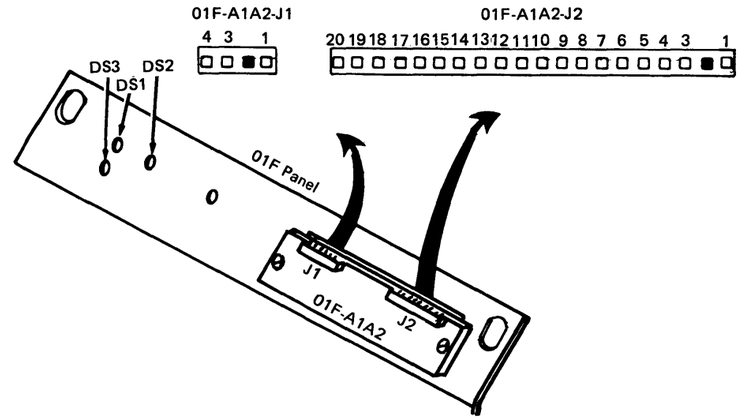
To replace the light emitting diodes (LEDs) mounted on the 8130/8140 operator panel requires replacing the mounting as well as the diode.

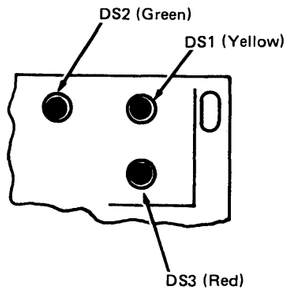
*Removal*

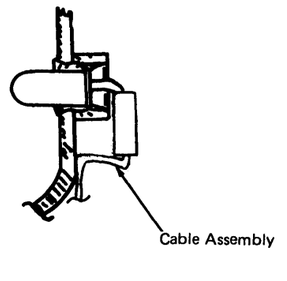
After turning off power, disconnect the cable to the diode pins. Cut through the diode and mount as close as possible to the metal panel as shown in Figure PA520-1, using diagonal cutting pliers, or equivalent.

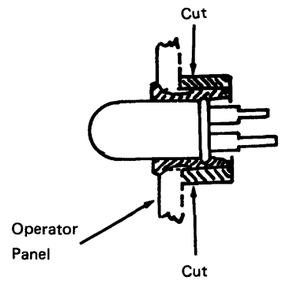
*Installation*

Using new parts, assemble the diode and mount by engaging the two rings of the mount in the panel, one over the other.



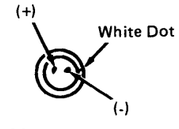




**Figure PA520-1. LED Assembly**

## PA530 BOP Adapter Card Removal and Replacement Procedure

Referring to Figure PA530-1, proceed as follows:

1. Remove the four front cables from the adapter card (locations B2A2, B2A3, B2A4, and B2A5).
2. Remove the two retaining nuts from the front card and cable connector bracket.
3. Remove the adapter card from the rear card and cable connector bracket with the front card and cable connector bracket still attached.
4. Remove the adapter card from the front card and cable connector.
5. To replace the card, perform the above steps in reverse order.

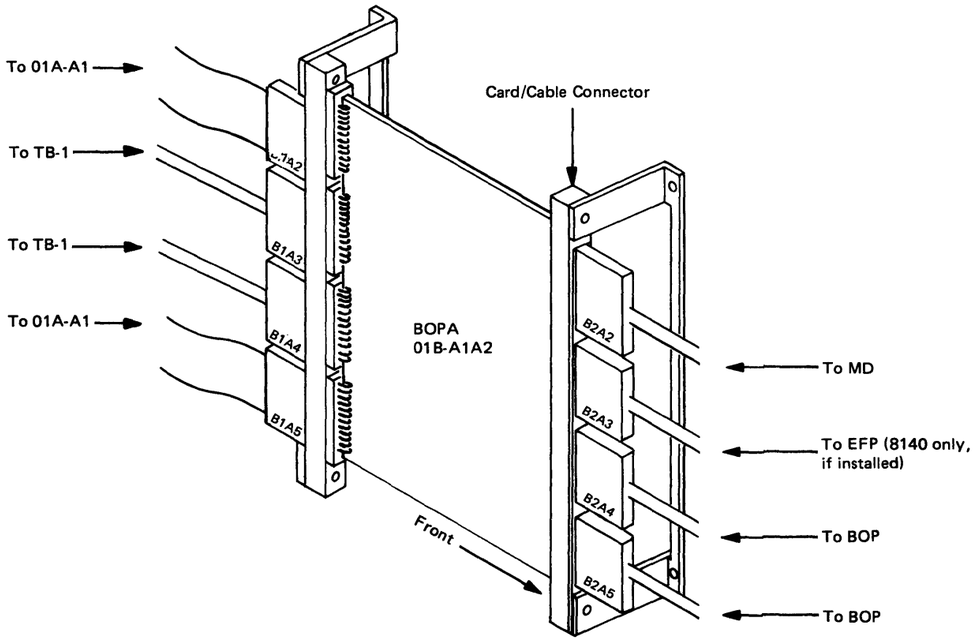



**Figure PA530-1. Basic Operator Panel Adapter Card (01B)**

## PA540 How to Gain Access to BOP Components

To replace any operator panel component, you must first gain access to the rear of the panel, as follows:

1. Remove 8130/8140 power plug from the wall or turn off the line voltage circuit breaker (CB1) on 8140 Models BXX.

**DANGER**
**DC voltage is still present at the operator panel with the 8130/8140 power switch in the Power Off position.**

2. Open the 8130/8140 front covers and remove the bezel by sliding the two retainer clips to the rear and lifting the front edge straight up and toward the front of the unit, ensuring that the studs are clear of the retainer clips (Figure PA540-1).
3. Pivot the BOP assembly toward the front of the 8130/8140 to gain access to any of the BOP field-replaceable units.

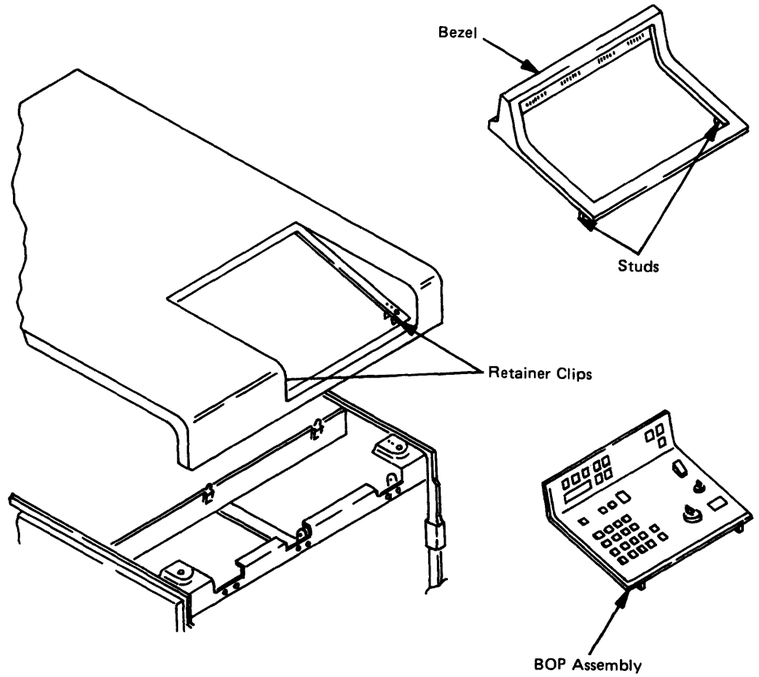



**Figure PA540-1. BOP Frame Mounting**

## PA550 01G Gate Capacitor and Thermal Replacement Procedure

Replace capacitors on the 01G gate as follows:

- If any capacitor C1 through C7 or C12 is defective, replace the capacitor only.
- If any capacitor C8 through C11 or the 01G gate thermal is defective, replace all capacitors C8—C11, and the W6 bus bar, which includes the thermal.

## PA600 Service Checks

**DANGER**
**With the power cord connected to the wall outlet, line voltage and the +5 and +24 control voltages are always present in all:**

- **8130s, 8140 Models AXX and 8101s.**
- **8140 Models BXX with the line voltage circuit breaker (CB1) on.**

**Before removing metal covers or internal power components (except for power control (PC and logic cards), either (1) disconnect the power cord for all 8130s, 8140 Models AXX, and all 8101s, or (2) turn off CB1 for 8140 Models BXX.**

**Caution: To remove either power control (PC) or logic cards:**

1. **Place the operator panel power switch to the Off position.**
2. **Disconnect 01G-J8 from the PC-1 card.**

## PA610 AC Ripple Service Check

Use the oscilloscope setups shown below with a Tektronix 453, 454, or similar scope; connect the scope ground lead to 01G TB1-2.

| Control | Setting |
|---|---|
| Channel A sweep mode | Normal |
| Channel A level | + |
| Channel A coupling | DC |
| Channel A slope | + |
| Channel A source | Internal |
| Trigger | Auto trig |
| Mode | Channel 1 |
| Channel 1 volts/div | 50 mv* |
| Channel 1 input | AC |
| Times per division | 0.1 sec |
| Channel 1 probe | See table below |

*Use a X1 probe; adjust the scope for sharp focus.

| DC Voltage | Maximum Ripple Peak to Peak | Channel 1 Probe | Fused by |
|---|---|---|---|
| - 4 | 40 mv | PC-2 J15-3 | 01G-F14 |
| * - 4 | 40 mv | PC-2 J15-3 | 01M-F14 |
| * - 4 | 150 mv | PC-50 J52-2 | 01N-F50 |
| ** - 4 | 150 mv | PC-50 J52-2 | 01G-F50 |
| + 5 | 100 mv | 01G TB1-7 | 01G-F3 |
| + 5 | 100 mv | 01G TB1-9 | 01G-F4 |
| + 5 | 100 mv | 01G TB1-10 | 01G-F5 |
| + 5 | 100 mv | 01G TB1-11 | 01G-F6 |
| * + 5 | 150 mv | 01R TB2-1 | 01R-F1 |
| * + 5 | 150 mv | 01R TB2-2 | 01R-F2 |
| * + 5 | 150 mv | 01R TB2-3 | 01R-F3 |
| + 5 Control | 200 mv | PC-1 J1A12 | |
| - 5 | 200 mv | 01G TB1-1 | 01G-F8 |
| + 8.5 | 340 mv | 01G TB1-5 | 01G-F2 |
| - 8.5 | 340 mv | PC-1 J3-1 | 01G-F7 |
| +12 | 960 mv | PC-1 J6-1 | 01G-F10 |
| -12 | 960 mv | 01G TB1-4 | 01G-F1 |
| +24 | 1920 mv | PC-1 J6-3 | 01G-F9 |
| +24 Control | 200 mv | PC-1 J9B12 | |

*Present only on 8140 Models BXX
**Present only on 8101 Model A25.

## PA620 8130/8140/8101 Indicator Check

The Lamp Test pushbutton provides a quick method to check the 8130/8140 operator panel indicators. You can also check the operation of all system indicators as follows:

1. Perform the procedure in PA540 to gain access to the rear of the panel.
2. On any operator panel, jumper 01F EC2-e to ground. This should turn on all system indicators except DS50. (See PA720 for EC2-e location and BU424 for EC2 point-to-point connections).
3. To check DS50, remove fuse F50. The indicator should turn on.
4. Perform the steps in PA540 in reverse order.

## PA630 Capacitor Resistance Check

**Caution: Check all capacitors for opens or shorts with the power cord disconnected from the wall outlet.**

The capacitor (micro)farad rating generally determines both how far and the speed at which your ohmmeter deflects. Capacitors with a numerically large rating generally cause a wide meter needle deflection toward the zero ohms position and a slow return to the infinity position; capacitors with a small rating cause little deflection and rapid return to zero and are, therefore, sometimes difficult to check.

Use your ohmmeter to check capacitors as follows:

1. Isolate the capacitor from the circuit.
2. Short the capacitor terminals with a resistor to discharge it. Generally, capacitors having a large (micro)farad rating retain a charge longer than those having a low value.
3. Set the meter on the R X 10 scale.
4. Connect the meter leads across the capacitor terminals. (Observe the + and - connections for polarized capacitors.) The needle should deflect rapidly toward zero ohms and then return slowly to the infinity position.

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## PA640 Tranformer Winding and Diode Service Checks

### *PA641 01G Gate T2 Transformer Winding and Diode Service Check*

Perform the following service check:

1. Unplug the power cord.
2. Disconnect the transformer winding leads from the diodes connected to the voltage in question. See PA410–PA430 AC Power to identify transformer windings and Figure PA641-1 for the location of the diodes.
3. With the meter set to Rx1, verify continuity through the windings.
4. Set the meter to the highest resistance scale and check the diode front-to-back ratio. Exchange any diode that does not have at least a 10:1 ratio reading.
5. Disconnect the center tap of winding under test. With the meter set to the highest resistance scale, check for an infinite reading between the winding and ground.
6. If a short to ground or open winding is found, exchange the transformer.
7. If no fault is found in the transformer winding at this point, connect the center tap of the winding, but not the leads that go to the diodes. Set the meter to the ac volt scale for the voltage expected for the windings to be checked. Make certain the leads are not touching anything. Connect the meter leads to the winding leads and power up. If power rises momentarily, check the ac voltage. If it was not correct, exchange the transformer.

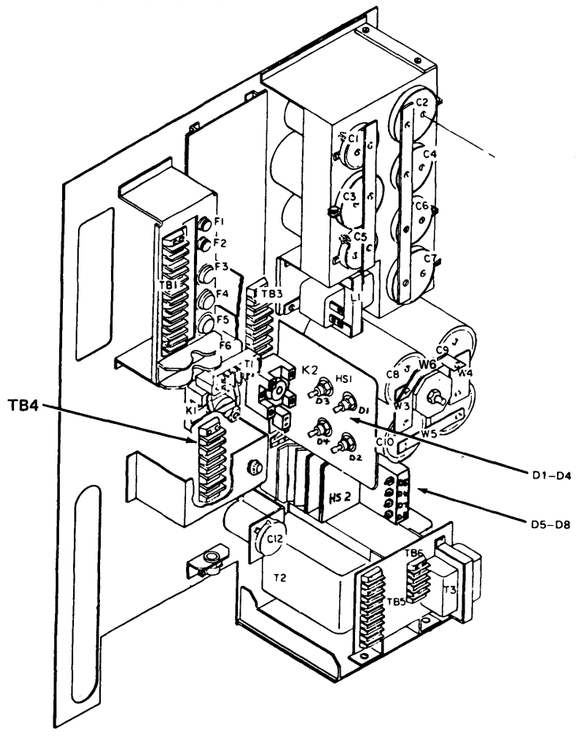



**Figure PA641-1. 01G Transformer and Diode Locations**

### *PA642 01G Gate Power Supply Diode Isolation*

To isolate diodes in the power supply for resistance checks, you should use one of the following procedures:

| Procedure | Diodes |
|---|---|
| A | D5, D6, D7, D8 |
| B | D2, D4 |
| C | D1, D3 |

**Procedure A — Diodes D5, D6, D7, D8**

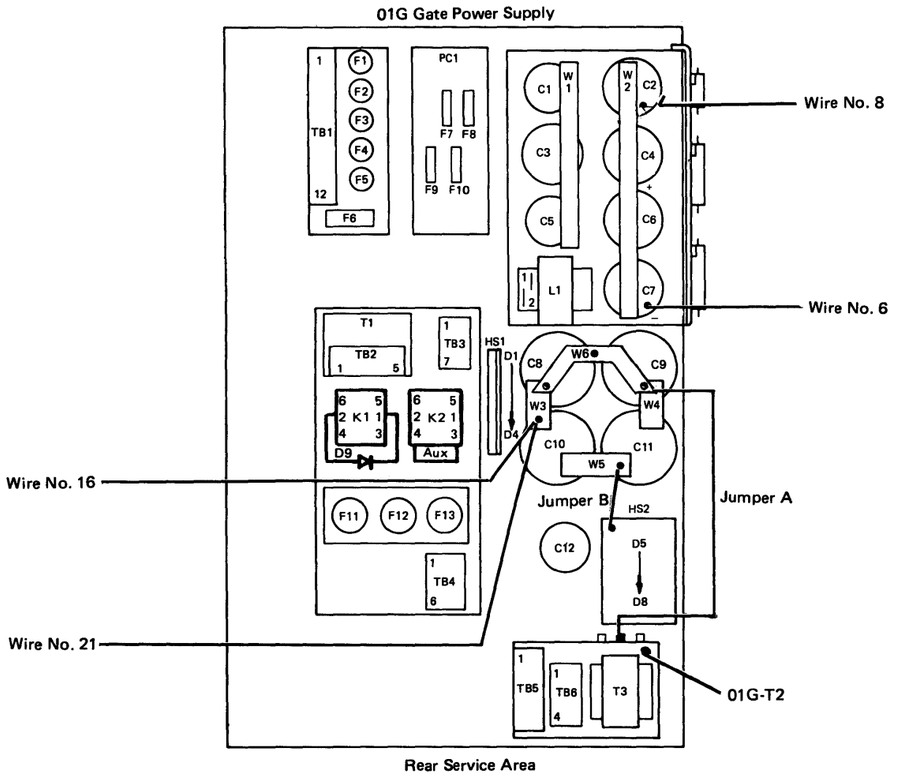
1. Power down the unit and unplug the ac power cord.
2. Remove the plastic safety shield covering the C8, C9, and C11 capacitor area (see Figure PA642-1).
3. Remove jumper B at the W5 bus bar end (Figure PA642-1).
4. Remove jumper A at the W4 bus bar end (Figure PA642-1).
5. Check the diodes using the diode resistance check procedure (PA641). Measure between the removed wire ends of jumper A and jumper B. See Notes 1 and 2 below for additional information.
6. If a shorted condition exists, the diodes must be unsoldered from the T3 windings (see PA440) to further isolate the shorted diode or diodes.
7. If an open condition exists, exchange all four diodes.
8. Reinstall the wires and the safety shield removed in the preceding steps after you have exchanged the defective diodes.

**Notes:**

1. *These diodes are wired in parallel. They can be isolated as a group to check them for a shorted condition. If a shorted condition exists, one or more diodes could be shorted.*
2. *The only valid open condition that can be found by this procedure is if all diodes in a group are open. A single open diode cannot be detected with this procedure. To check for a single open diode, remove the wires from each diode. Check each diode for an open condition using the diode resistance check procedure (PA641).*

**Procedure B — Diodes D2 and D4**

1. Power down the unit and unplug the ac power cord.
2. Remove the plastic safety shield covering bus bars W3, W4, and W5 (see Figure PA642-1).
3. Remove wires 16 and 21 at the W3 bus bar.
4. Remove the plastic safety shield covering bus bars W1 and W2 (see Figure PA642-1).
5. Remove wire number 8 from the plus terminal of capacitor C2.
6. Check the diodes using the diode resistance check procedure (PA641). Measure between the removed ends of wire numbers 8 and 16. See Notes 1 and 2 below for additional information.
7. If a shorted condition exists, the diodes must be unsoldered from the T2 windings (see PA440) to further isolate the shorted diode or diodes.




Note: *See PA440 for capacitor polarity.*

**Figure PA642-1. Diode Check Wire Removal**

8. Replace diodes only in pairs.
9. Reinstall the wires and the safety shield removed in the preceding steps after you have exchanged the defective diodes.

**Notes:**

1. *These diodes are wired in parallel. They can be isolated as a group to check them for a shorted condition. If a shorted condition exists, one or more diodes could be shorted.*
2. *The only valid open condition that can be found by this procedure is if all diodes in a group are open. A single open diode cannot be detected with this procedure. To check for a single open diode, remove the wires from each diode. Check each diode for an open condition using the diode resistance check procedure (PA641).*

**Procedure C — Diodes D1 and D3**

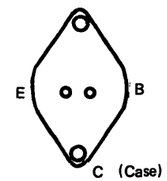
1. Power down the unit and remove the ac power cord.
2. Disconnect plug P10 from jack J10 on the PC1 card (PA461).
3. Remove the plastic safety shield covering bus bars W3, W4, and W5 (see Figure PA642-1).
4. Remove wire numbers 16 and 21 from the W3 bus bar.
5. Remove the plastic safety shield covering the W1 and W2 bus bars (Figure PA642-1).
6. Remove wire number 6 from the plus terminal of capacitor C7.
7. Check the diodes using the diode resistance check procedure (PA641). Measure between the removed ends of wire numbers 21 and 6. See Notes 1 and 2 below for additional information.
8. If a shorted condition exists, the diodes must be unsoldered from the T2 windings (see PA440) to further isolate the shorted diode or diodes.
9. If an open condition exists, exchange both diodes.
10. Reinstall the wires and the other safety shield removed in the preceding steps after you have exchanged the defective diodes.
11. Reinstall plug P10 on the PC1 card.

**Notes:**

1. *These diodes are wired in parallel. They can be isolated as a group to check them for a shorted condition. If a shorted condition exists, one or more diodes could be shorted.*
2. *The only valid open condition that can be found by this procedure is if all diodes in a group are open. A single open diode cannot be detected with this procedure. To check for a single open diode, remove the wires from each diode. Check each diode for an open condition using the diode resistance check procedure (PA641).*

## *PA643 Transistor Q1 and Q2 Check*

1. Set a CE VOM to RX1 scale.
2. Put the positive probe on "B" (base); see below.
3. Probe pins E and C (emitter and collector) with the negative probe. Each pin should read between 10 and 30 ohms.
4. Put the negative probe on B and probe pins E and C with the positive probe. Both pins should show an infinite reading.
5. Connect one probe on E and the other on C, then reverse the probes; there should be no reading either way. A low reading means a shorted transistor.




View From Bottom

## PA650 Fuse and Voltage Distribution

Isolate power problems by disconnecting the loads from a fuse that opens repeatedly. See Figure PA650-1, PA650-2, PA650-3 or PA650-4 to determine the points to disconnect to isolate all of the loads for that fuse.

**Caution: Unplug the power cord before disconnecting or connecting plugs or exchanging cards.**

Disconnect the plugs for the voltage distribution to be checked. Power up and verify that the fuse does not open again. If the fuse opens again, a short in the wiring exists. Refer to the wiring diagrams for the voltage path for that fuse. Using your ohmmeter and the diagrams, isolate the short and make the necessary repairs.

If the fuse does not open with all of the loads disconnected, reconnect the plugs one at a time. If the fuse opens, the gate or board for that plug has either a defective card or a short in the board. If the plug connects to a single card, exchange the card. If not, remove all of the cards from the gate and install a new fuse. If the fuse opens again, carefully inspect the board for bent pins, broken or shorted wires, and other external damage. If there are no visual problems, exchange the board.

If the fuse does not open with all of the cards removed, power down, insert one card, and power up. If inserting a card causes the fuse to open, exchange the card. If not, continue until all cards are inserted, one at a time.

Return to the start of the PA MAPs when all of the cards are inserted, all of the loads are reconnected, and the fuse remains good.

| Fuse | Size | Type | Part No. | Voltage | Load | Connector (Note) |
|---|---|---|---|---|---|---|
| 01G F1 | 10A | ABC | 511063 | -12 dc | 01C gate (disk) | J1 |
| 01G F2 | 15A | ABC | 596676 | +8.5 dc | 01A-A1 board<br>01A-A2 board<br>01B gate (BOPA card)<br>01G-PC-1 card | J7, J9, J11<br>J1 to J6<br>B1A4 cable<br>P4 |
| 01G F3 | 15A | BAF | 115971 | +5 dc | 01B gate (BOPA card)<br>01C gate (disk)<br>01D gate (diskette)<br>01F-A1A2 BOP ind. card<br>01G-PC-1 card | B1A3, B1A4 cables<br>J2, J4<br>A2 cable<br>J1<br>P4 |
| 01G F4 | 15A | BAF | 115971 | +5 dc | 01A-A2 board | J1, J2, J3 |
| 01G F5 | 15A | BAF | 115971 | +5 dc | 01A-A2 board | J1 to J6 |
| 01G F6 | 30A | NON | 7389944 | +5 dc | 01A-A1 board | J1 to J5, J7, J9, J11 |
| 01G F7 | 3A | AGC | 855252 | -8.5 dc | 01A-A1 board<br>01A-A2 board | J4, J5<br>U4D07 |
| 01G F8 | 10A | ABC | 511063 | -5 dc | 01A-A1 board<br>01A-A2 board<br>01B gate (BOPA card)<br>01D gate (diskette)<br>01G-PC-1 card | J7, J9, J11<br>J1 to J6<br>B1A3 cable<br>A2 cable<br>P2, P3, P4 * |
| 01G F9 | 4A | MTH | 111257 | +24 dc | 01C gate (disk)<br>01D gate (diskette) | J5<br>A2 cable |
| 01G F10 | 4A | MTH | 111257 | +12 dc | 01C gate (disk) | J1 |
| 01G F11 | 0.5A<br>0.3A | MDL<br>MDL | 78999<br>78998 | 100-127ac<br>200-240ac | 01G-T1 transformer | |
| 01G F12 | 15A<br>8A | FNM<br>FNM | 107670<br>107668 | 100-127ac<br>200-240 ac | 01G-T2 transformer | |
| 01G F13 | 4A<br>2A | FNM<br>FNM | 107665<br>92734 | 100-127ac<br>200-240ac | 01H and 01U gate<br>convenience outlets | |
| 01G F14 | 4A | MTH | 111257 | -4 dc | 01C gate (disk) | J2, J4 |

* -5V source.

**Note:** *The connectors referenced in this column are always located on the gate, board, or card that provides the load. For multiple connectors, disconnect all to isolate the load. See PA700 for connector locations.*

**Figure PA650-1. 8130 Fuse Specifications and Voltage Distribution Chart**

| Fuse | Size | Type | Part No. | Voltage | Load | Connector (Note) |
|---|---|---|---|---|---|---|
| 01G F1 | 10A | ABC | 511063 | -12 dc | 01C gate (disk) | J1 |
| 01G F2 | 15A | ABC | 511063<br>596676 | +8.5 dc | 01A-A1 board<br>01A-A2 board<br>01B gate (BOPA card) | J1, J3<br>J1, J3<br>B1A4 cable |
| 01G F3 | 15A | BAF | 115971 | +5 dc | 01B gate (BOPA card)<br>01C gate (disk)<br>01D gate (diskette)<br>01F-A1A2 BOP ind. card<br>01F-A1A3 EFP ind. card<br>01G-PC-1 card | B1A3, B1A4 cables<br>J2, J4<br>A2 cable<br>J1<br>J2<br>P4 |
| 01G F4 | 20A | BAF | 117252 | +5 dc | 01A-A1 board | Y2, Y3, Y4 |
| 01G F5 | 20A | BAF | 117252 | +5 dc | 01A-A1 board | Y2, Y3, Y4 |
| 01G F6 | 30A | NON | 7389944 | +5 dc | 01A-A2 board | Y2, Y3, Y4 |
| 01G F7 | 3A | AGC | 855252 | -8.5 dc | 01A-A2 board | H2 (Models A3X, A4X) |
| 01G F8 | 10A | ABC | 511063 | -5 dc | 01A-A1 board<br>01A-A2 board<br>01B gate (BOPA card)<br>01D gate (diskette)<br>01G-PC-1 card | J1<br>J1<br>B1A3 cable<br>A2 cable<br>P2, P3, P4 * |
| 01G F9 | 4A | MTH | 111257 | +24 dc | 01C gate (disk)<br>01D gate (diskette) | J1<br>A2 cable |
| 01G F10 | 4A | MTH | 111257 | +12 dc | 01C gate (disk) | J5 |
| 01G F11 | 1A<br>0.5A | MDL<br>MDL | 303549<br>78999 | 100—127 ac<br>200—240 ac | 01G-T1 transformer | |
| 01G F12 | 15A<br>8A | FNM<br>FNM | 107670<br>107668 | 100—127 ac<br>200—240 ac | 01G-T2 transformer | |
| 01G F13 | 4A<br>2A | FNM<br>FNM | 107665<br>92734 | 100—127 ac<br>200—240 ac | 01H and 01U gate convenience outlets | |
| 01G F14 | 4A | MTH | 111257 | -4 dc | 01C gate (disk) | J2, J4 |

* -5V source.

**Note:** *The connectors referenced in this column are always located on the gate, board, or card that provides the load. For multiple connectors, disconnect all to isolate the load. See PA700 for connector locations.*

**Figure PA650-2. 8140 Models AXX Fuse Specifications and Voltage Distribution Chart**

| Fuse | Size | Type | Part No. | Voltage | Load | Connector (Note) |
|---|---|---|---|---|---|---|
| 01G F1 | 10A | ABC | 511063 | -12 dc | 01C gate (disk 1)<br>01E gate (disk 2)<br>01N-PC-50 | J1<br>J1<br>P50 |
| 01G F2 | 15A | ABC | 596676 | +8.5 dc | 01A-A1 board<br>01A-A2 board<br>01A-B2 board<br>01A-C2 board<br>01A-D2 board<br>01B gate (BOPA card)<br>01G-PC-1 | J1-J6<br>J1, J2, J3<br>J1, J2, J3<br>J1, J2, J3<br>J1, J2, J3<br>B1A4 cable<br>P4 |
| 01G F3 | 15A | BAF | 115971 | +5 dc | 01A-A2 board<br>01B gate (BOPA card)<br>01C gate (disk 1)<br>01D gate (diskette)<br>01E gate (disk 2)<br>01F-A1A2 BOP ind. card<br>01F-A1A3 EFP ind. card<br>01G-PC-1 card | J1-J3, bus bar E<br>B1A3, B1A4 cables<br>J1, J4<br>A2 cable<br>J1, J4<br>J1<br>J2<br>P4 |
| 01G F4 | 20A | BAF | 117252 | +5 dc | 01A-B2 board | J1-J3, bus bars E, J |
| 01G F5 | 20A | BAF | 117252 | +5 dc | 01A-C1 board * | J1-J3, bus bars E, J |
| 01G F6 | 30A | | 6814327 | +5 dc | 01A-A1 board | J1-J6, bus bars E, J, N, and S |
| 01G F7 | 3A | AGC | 855252 | -8.5 dc | 01A-A2 board<br>01A-C2 board **<br>01A-D2 board ** | TB2-10<br>TB2-9<br>TB2-10 |
| 01G F8 | 10A | ABC | 511063 | -5 dc | 01A-A1 board<br>01A-C1 board<br>01A-A2 board<br>01A-B2 board<br>01A-C2 board<br>01A-D2 board<br>01B gate (BOPA card)<br>01D gate (diskette) | J1-J6<br>J1-J3<br>J1-J3<br>J1-J3<br>J1-J3<br>J1-J3<br>B1A3 cable<br>A2 cable |
| 01G F9 | 4A | MTH | 111257 | +24 dc | 01C gate (disk 1)<br>01D gate (diskette)<br>01E gate (disk 2)<br>01G-PC-1 card | J5<br>A2 cable<br>J5<br>P1 |
| 01G F10 | 4A | MTH | 111257 | +12 dc | 01A-C1 board<br>01C gate (disk 1)<br>01E gate (disk 2)<br>01G-PC-1 card | J1-J3<br>J1<br>J1<br>P1 |
| 01G F11 | 0.3A | MDL | 78998 | 208—240 ac | 01G-T1 transformer | |
| 01G F12 | 5A | FNM | 107666 | 208—240 ac | 01G-T2 transformer | |
| 01G F13 | 1.6A | | 228391 | 208—240 ac | 01R-T1 transformer | |
| 01L F1 | 1.8A | | 2495467 | 208/240 ac | Convenience outlets | |
| 01M F14 | 4A | MTH | 111257 | -4 dc | 01C gate (disk 1) | J2, J4 |
| 01N F50 | 6A | | 5214456 | -4 dc | 01E gate (disk 2) | J2, J4 |
| 01R F1 | 10A | ABC | 511063 | +5 dc | | |
| 01R F2 | 15A | | 5236559 | +5 dc | 01A-D2 board * | J1, J2, J3<br>Bus bars E and J |
| 01R F3 | 15A | | 5236559 | +5 dc | 01A-C2 board | J1, J2, J3<br>Bus bars E and J |

*Board D2 not present and 01R-F2 provides +5V source for board C1 when floating-point is installed.
**8.5V not present if these boards contain display/printer adapter.

**Note:** *The connectors referenced in this column are always located on the gate, board, or card that provides the load. For multiple connectors, disconnect all to isolate the load. See PA700 for connector loads.*

**Figure PA650-3. 8140 Models BXX Fuse Specifications and Voltage Distribution Chart**

| Fuse | Size | Type | Part No. | Voltage | Load | Connector (Note 1) |
|---|---|---|---|---|---|---|
| 01G F1 | 10A | ABC | 511063 | -12 dc | 01C gate (disk 1)<br>01E gate (disk 2) | J1<br>J1 |
| 01G F2 | 15A<br>(Note 2) | ABC | 596676 | +8.5 dc | 01A-A1 board<br>01A-A2 board<br>01A-B1 board | J1, J3<br>J1, J3<br>J1, J3 |
| 01G F3 | 15A | BAF | 115971 | +5 dc | 01C gate (disk 1)<br>01D gate (diskette)<br>01E gate (disk 2)<br>01G-PC-1 card | J2, J4<br>A2 cable<br>J2, J4<br>P4 |
| 01G F4 | 20A | BAF | 117252 | +5 dc | 01A-A1 board | J1, J2, J3 |
| 01G F5 | 20A | BAF | 117252 | +5 dc | 01A-B1 board | J1, J2, J3 |
| 01G F6 | 30A | NON | 7389944 | +5 dc | 01A-A2 board | J1, J2, J3 |
| 01G F7 | 3A | AGC | 855252 | -8.5 dc | 01A-A1 board<br>01A-B1 board | J2 **<br>J2 *** |
| 01G F8 | 10A | ABC | 511063 | -5 dc | 01A-A1 board<br>01A-A2 board<br>01A-B1 board<br>01D gate (diskette)<br>01G-PC-1 card | J1, J3<br>J1, J3<br>J1, J3<br>A2 cable<br>P2, P3, P4 * |
| 01G F9 | 4A | MTH | 111257 | +24 dc | 01C gate (disk 1)<br>01D gate (diskette)<br>01E gate (disk 2) | J5<br>A2 cable<br>J5 |
| 01G F10 | 4A | MTH | 111257 | +12 dc | 01C gate (disk 1)<br>01E gate (disk 2) | J1<br>J1 |
| 01G F11 | 1A<br>0.3A | MDL<br>MDL | 303549<br>78999 | 100—127 ac<br>200—240 ac | 01G-T1 transformer | |
| 01G F12 | 15A<br>8A | FNM<br>FNM | 107670<br>107668 | 100—127 ac<br>200—240 ac | 01G-T2 transformer | |
| 01G F14 | 4A | MTH | 111257 | -4 dc | 01C gate (disk 1) | J2, J4 |
| 01G F50 | 6A | | 5214456 | -4 dc | 01E gate (disk 2) | J2, J4 |

*-5V source
**Present for feature codes 1503 or 9943 (communications ports 1-4).
***Present for feature code 1504 (communications ports 5-8).

**Notes:**

1. *The connectors referenced in this column are always located on the gate, board, or card that provides the load. For multiple connectors, disconnect all to isolate the load. See PA700 for connector locations.*
2. *Use 10A for Models A25 (PN 511063).*

**Figure PA650-4. 8101 Fuse Specifications and Voltage Distribution Chart**

## PA660 Voltage Verification

Use PA661 through PA663 to verify system dc voltages, as well as PC card ac reference and dc logic voltages. Refer to the point-to-point diagrams in PA410-PA430 to verify the ac line voltage.

### *PA661 System DC Voltage Verification*

Use the following chart to verify that all system dc voltages are present and within tolerance. See PA710 and PA740 for TB and fuse locations, PA662 for PC-1 pin locations, PA663 for PC-2 pin locations, and PA664 for PC-50 pin locations.

- If a voltage is missing, use the PA MAP.
- If a voltage is present but missing at a gate or board, use PA440 and PA650 to isolate the open circuit.

| DC Voltage | Range in Volts | + Lead | - Lead | Fuse | Sensed |
|---|---|---|---|---|---|
| -4 | -3.8 to -4.2 | PC-2 J15-1 | PC-2 J15-3 | 01G-F14 | At PC-2 |
| -4** | -3.8 to -4.2 | PC-2 J15-1 | PC-2 J15-3 | 01M-F14 | At PC-2 |
| -4* | -3.8 to -4.2 | PC-50 J52-6 | PC-50 J52-2 | 01N-F50 | At PC-50 |
| -4** | -3.8 to -4.2 | PC-50 J52-6 | PC-50 J52-2 | 01G-F50 | At PC-50 |
| +5 | +4.8 to +5.5 | 01G TB1-7 | 01G W3 | 01G-F3 | At PC-2 |
| +5 | +4.8 to +5.5 | 01G TB1-9 | 01G W3 | 01G-F4 | No |
| +5 | +4.8 to +5.5 | 01G TB1-10 | 01G W3 | 01G-F5 | No |
| +5 | +4.8 to +5.5 | 01G TB1-11 | 01G W3 | 01G-F6 | No |
| +5 | +4.8 to +5.5 | 01R TB2-1 | 01R TB2-4 | 01R-F1 | No |
| +5 | +4.8 to +5.5 | 01R TB2-2 | 01R TB2-4 | 01R-F2 | No |
| +5 | +4.8 to +5.5 | 01R TB2-3 | 01R TB2-4 | 01R-F3 | No |
| +5 Ctl | +4.8 to +5.3 | PC-1 J1A12 | PC-1 J1A07 | None | No |
| -5 | -4.6 to -5.6 | 01G TB1-2 | 01G TB1-1 | 01G-F8 | At PC-1 |
| +8.5 | +7.9 to +9.5 | 01G TB1-5 | 01G W3 | 01G-F2 | No |
| -8.5 | -7.9 to -9.3 | 01G TB1-2 | PC-1 J3-1 | 01G-F7 | No |
| +12 | +11.0 to +13.2 | PC-1 J6-1 | 01G TB1-2 | 01G-F10 | At PC-1 |
| -12 | -11.0 to -13.1 | 01G W3 | 01G TB1-4 | 01G-F1 | At PC-1 |
| +24 | +22.0 to +26.4 | PC-1 J6-3 | 01G TB1-2 | 01G-F9 | At PC-1 |
| +24 Ctl | +17.0 to +30.0 | PC-1 J9B12 | PC-1 J9B01 | None | No |

*Present only on 8140 Models BXX.
**Present only on 8101 Model A25.

## *PA662 PC-1 Card AC and DC Voltage Verification*

The PC-1 card converts certain ac reference voltages into dc control and logic voltages, which are fused as indicated. Fuses F7—F10 mount on PC-1, while fuse F11 mounts on the 01G gate.

Use the following chart and Figure PA662-1 to verify the ac input and dc output voltages on the PC-1 card. See also PA461 for a point-to-point diagram, and PA650 for fuse specifications.

| AC Input | Input Pin | DC Output | Output Pin(s) | 01G Gate Fuse |
|---|---|---|---|---|
| --- | ----- | Common | J2-3, J4-3, J4-6 | * |
| 6V | J7-10 | -5V | J2-2, J3-3, J4-4 | F8 |
| 6V | J7-13 | -5V | J2-2, J3-3, J4-4 | F8 |
| 9.5V | J10-9 | -8.5V | J3-1 | F7 |
| 9.5V | J10-8 | -8.5V | J7-4, J10-5 | * |
| 10V | J13-6 | +5V Ctl | J1A12, J5, J11D03, J12D03 | F11 |
| 10V | J13-9 | +5V Ctl | J8B16 | F11 |
| --- | ----- | +5V Ctl | J8B15** | F11 |
| 13V | J10-1 | +12V | J1A10, J3-2, J5, J6-1 | F10 |
| 13V | J10-3 | +12V | J7-2 | * |
| 18V | J13-1 | +24V Ctl | J7-3, J8B12, J9B12, J13-4 | F11 |
| 18V | J13-7 | +24V Ctl | J13-4 | * |
| --- | ----- | +24V Ctl | J8A08** | F11 |
| --- | ----- | +24V Ctl | J11D09** | F11 |
| --- | ----- | +24V Ctl | J8B08** | F11 |
| --- | ----- | +24V Ctl | J12D11** | F11 |
| --- | ----- | +24V Ctl | J13-10** | F11 |
| 26V | J10-7 | +24V | J1A08, J2-1, J6-3, J6-4 | F9 |
| 26V | J10-4 | +24V | J7-1, J7-5 | * |

*Not fused
**Present only after power sequence completes successfully

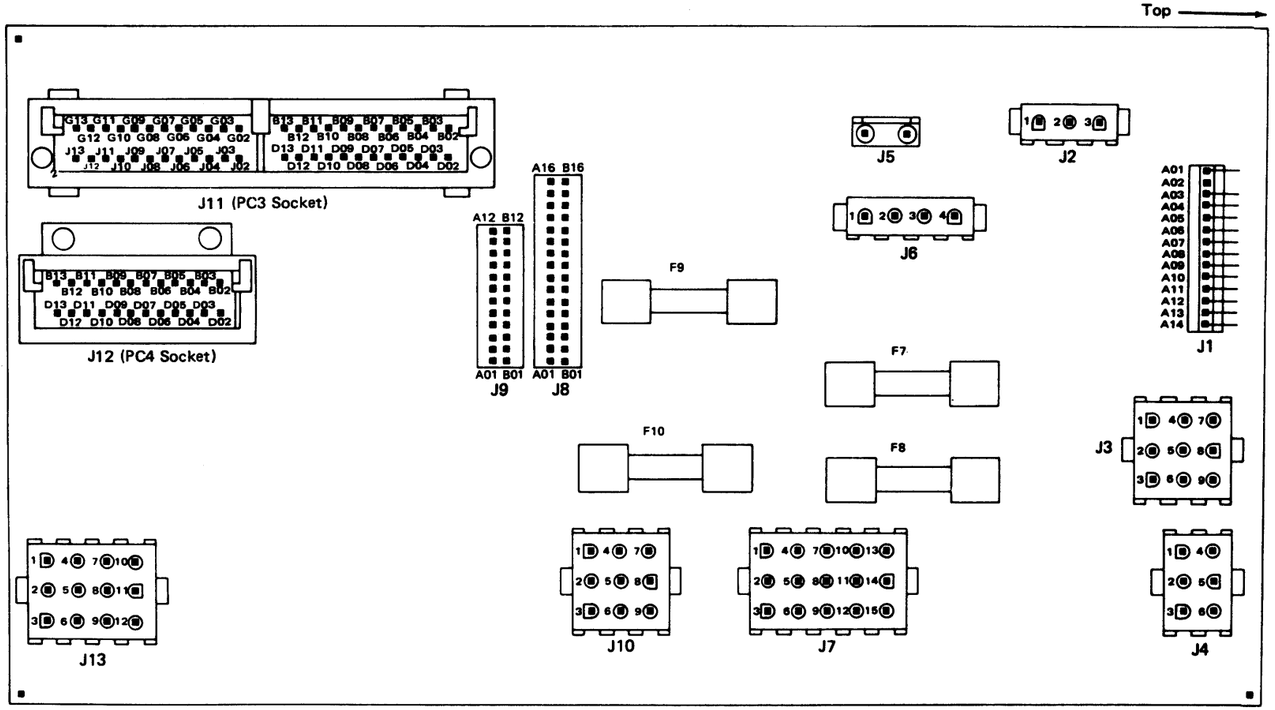



**Figure PA662-1. PC-1 Connector Locations**

*PA663 PC-2 Card DC Voltage Verification*

1. Use the following chart and Figure PA663-1 to check the dc input voltages on the PC-2 card.

| DC Voltage | Input Pin |
|---|---|
| Common | J14-1 |
| -4 | J14-3 |
| -4 | J14-4 |
| -4 | J14-8 |
| -4 | J14-9 |
| +4 | J14-7 |
| Common | J16B01 |
| -4 sense | J16A07 |
| +5 | J16B04 |
| +5 sense | J16A06 |
| -12 sense | J16B12 |
| +12 sense | J16A05 |
| +24 sense | J16A03 |

2. Check the output of fuse F14 (-4V) at PC-2 J15-3 and J15-4.

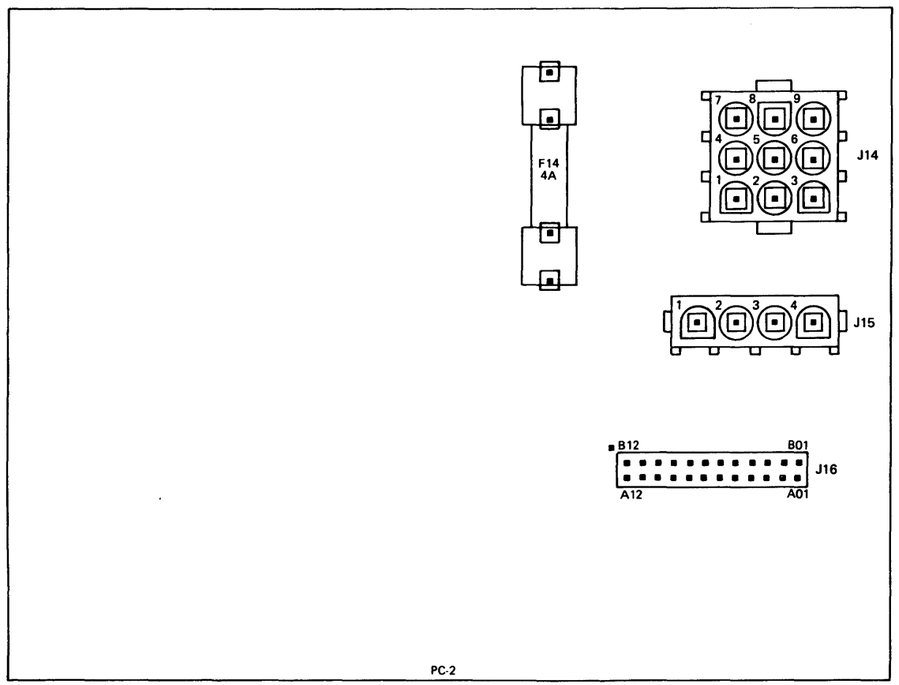



**Figure PA663-1. PC-2 Connector Locations**

**PA670 Power Status Indicators and Their Meaning**

The following table shows how the 8100 activates and resets its power-related status indicators.

| Indicator | Activated By | Reset By |
|---|---|---|
| Power On (DS2) | The end of a power-on sequence to indicate successful completion. | Start of power-off sequence. |
| Power/Thermal Check (DS3) | • An overvoltage or undervoltage fault.<br>• A high gate temperature.<br>• A disk drive interlock switch open. | Turning power off at the operator panel. (see Note) |
| Power On Disabled (8130/8140 only) (DS1) | • Disconnecting and reconnecting ac power after a high temperature power failure, providing the thermal signal is not active when reconnected.<br>• Disconnecting and reconnecting ac power after a power failure due to an undervoltage or overvoltage fault.<br>• A power off sequence caused by a program power off signal. This is not a power fault, but the power logic responds as if it were.<br>• Disconnecting and reconnecting ac power after a disk drive interlock switch opened, providing the switch is not still open when reconnected.<br>• The keylock switch in the Secure position with power off. | Turning power off at the operator panel and turning the keylock switch (if installed) to either Enable or Power Only. (see Note) |
| Disk Storage Power Fault (DS4 on PC-2) | • A disk storage-related undervoltage or overvoltage fault on the first disk drive.<br>• Drive interlock switch open on either the first or second disk drive. | Turning power off at the operator panel. (see Note) |
| Disk Storage Power Fault (DS50 on PC-50) | A -4V or -12V undervoltage condition on the second disk drive. | Turning power off at the operator panel. (see Note) |
| DS51 | Brake Applied signal present at the second disk drive. | Turning power off at the operator panel. (see Note) |

**Note:** *The indicator cannot be reset if either the thermal or the disk drive interlock switches remain open.*

## PA680 8140 Model BXX DC Parallel Wiring Check

Certain logic voltages in 8140 Models BXX have parallel wires used for voltage distribution. All loads, therefore, must be disconnected to check wiring continuity for these models.

Other than an open or shorted wire, noise or low-voltage problems in the dc parallel wiring can also cause a machine failure:

- Noise can be caused by bad connections, loose screws, or defective components.

  **Note:** *You cannot disconnect the load to troubleshoot noise problems that occur in circuits having parallel wiring. Disconnecting a good line from a noisy one gives a false error indication because either (1) the additional current through a defective connection can temporarily eliminate the noise or (2) the voltage drop exceeds allowable limits and causes a machine failure.*

- Low voltage can be caused by one broken wire or one bad connection.

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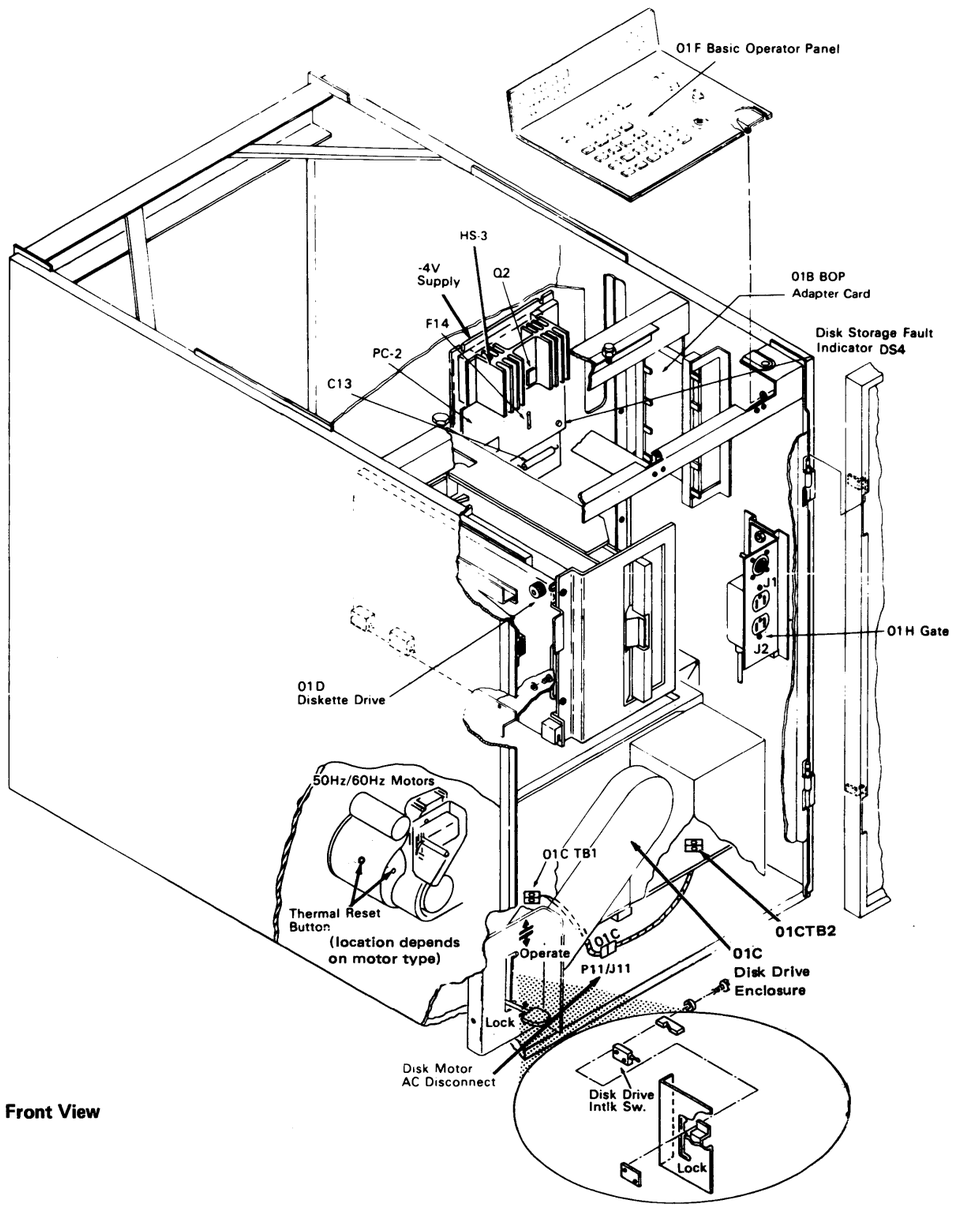
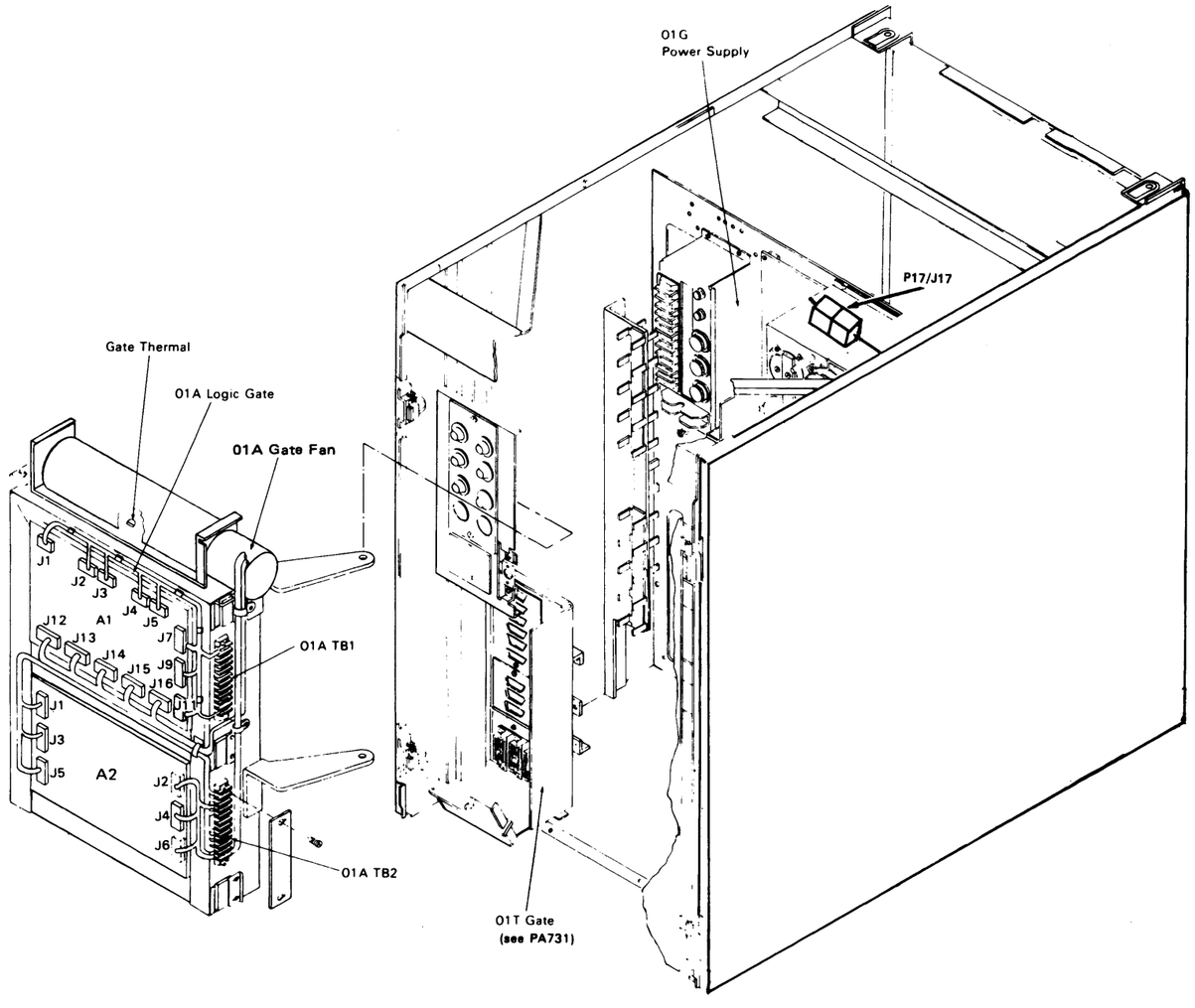
## PA700 Locations

### PA710 Gate and Other Subassembly Locations

*PA711 8130 Gate and Other Subassembly Locations*

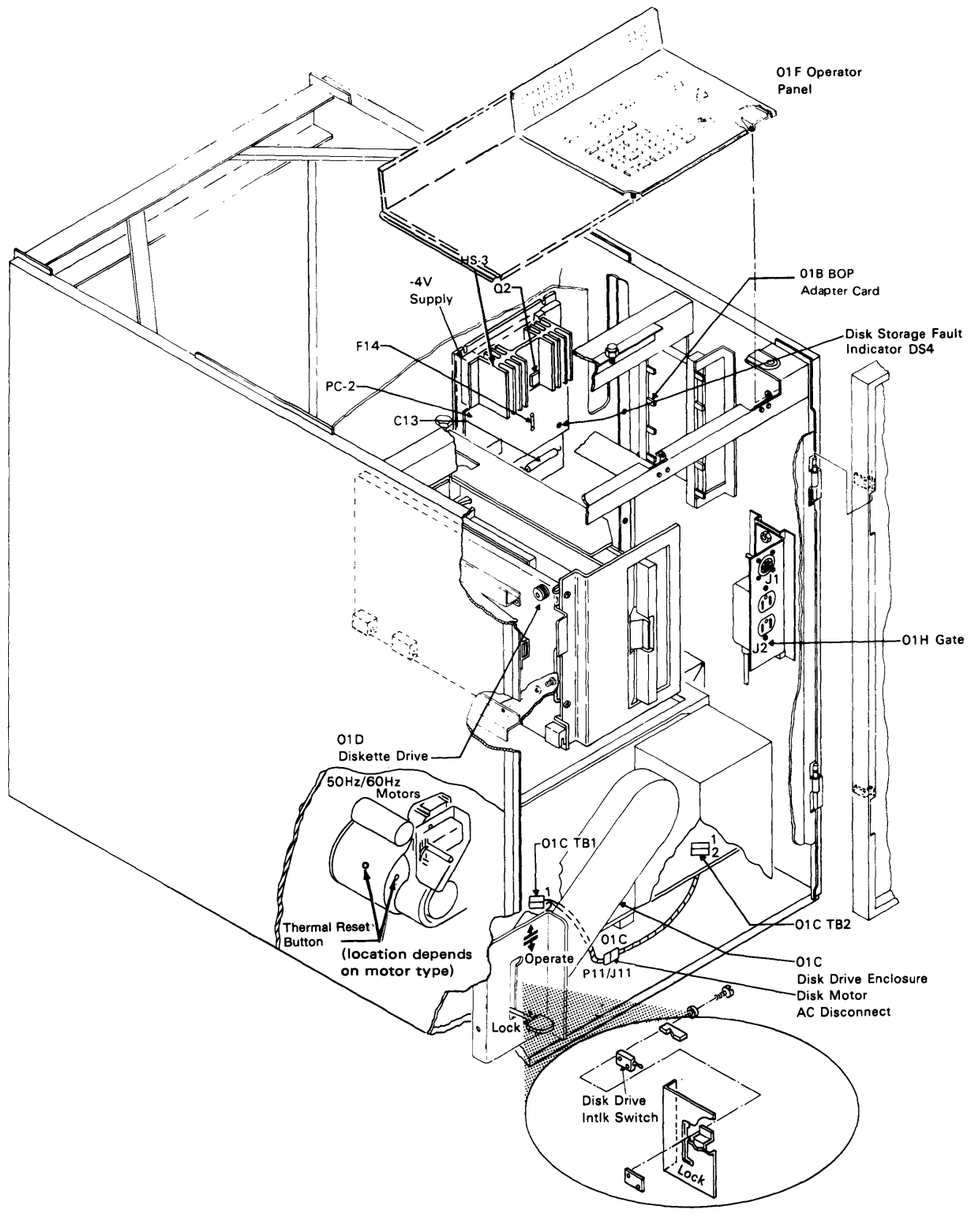



**Front View**

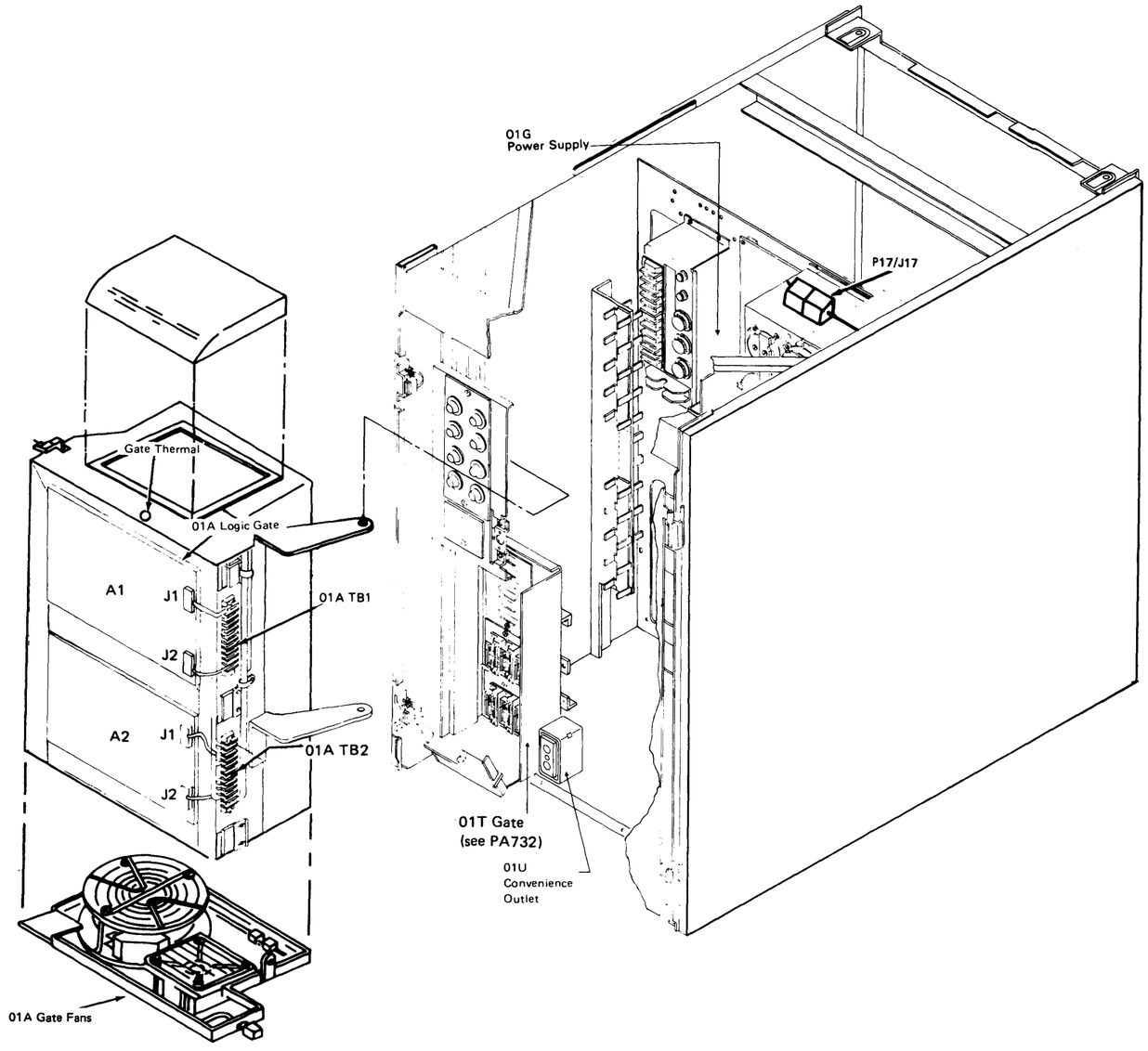



**Rear View**

*PA712 8140 Gate and Other Subassembly Locations*

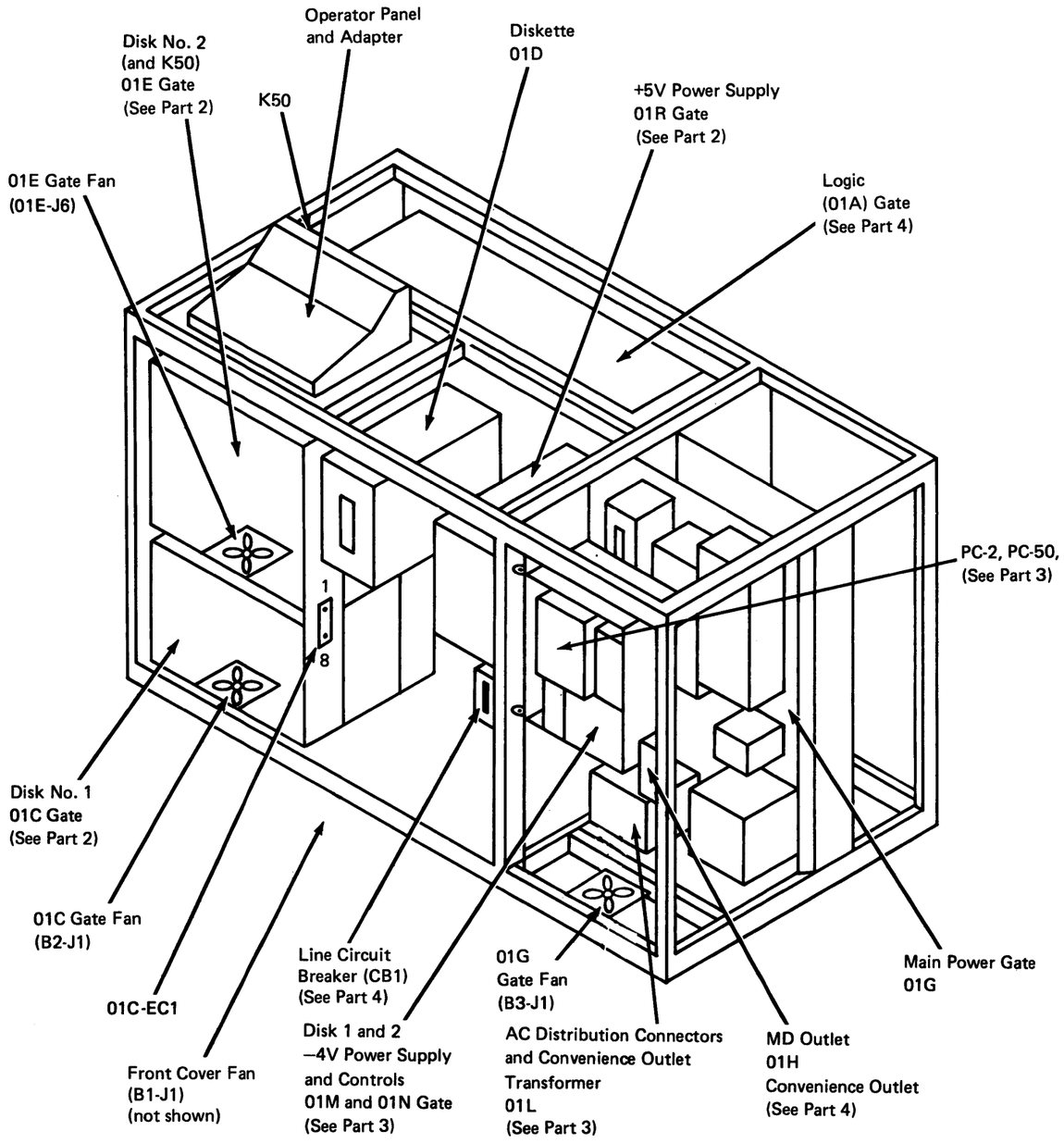



**Front View**




**Rear View**

**Figure PA712-1. 8140 Models AXX Gate and Other Subassembly Locations**



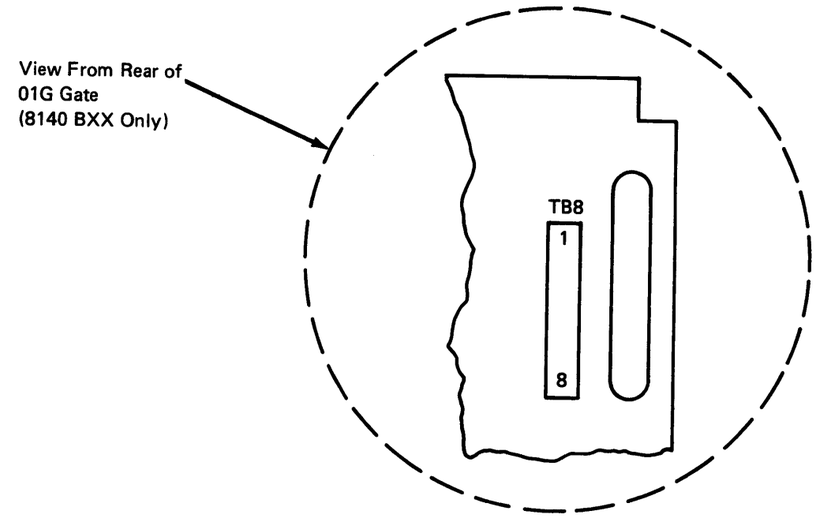
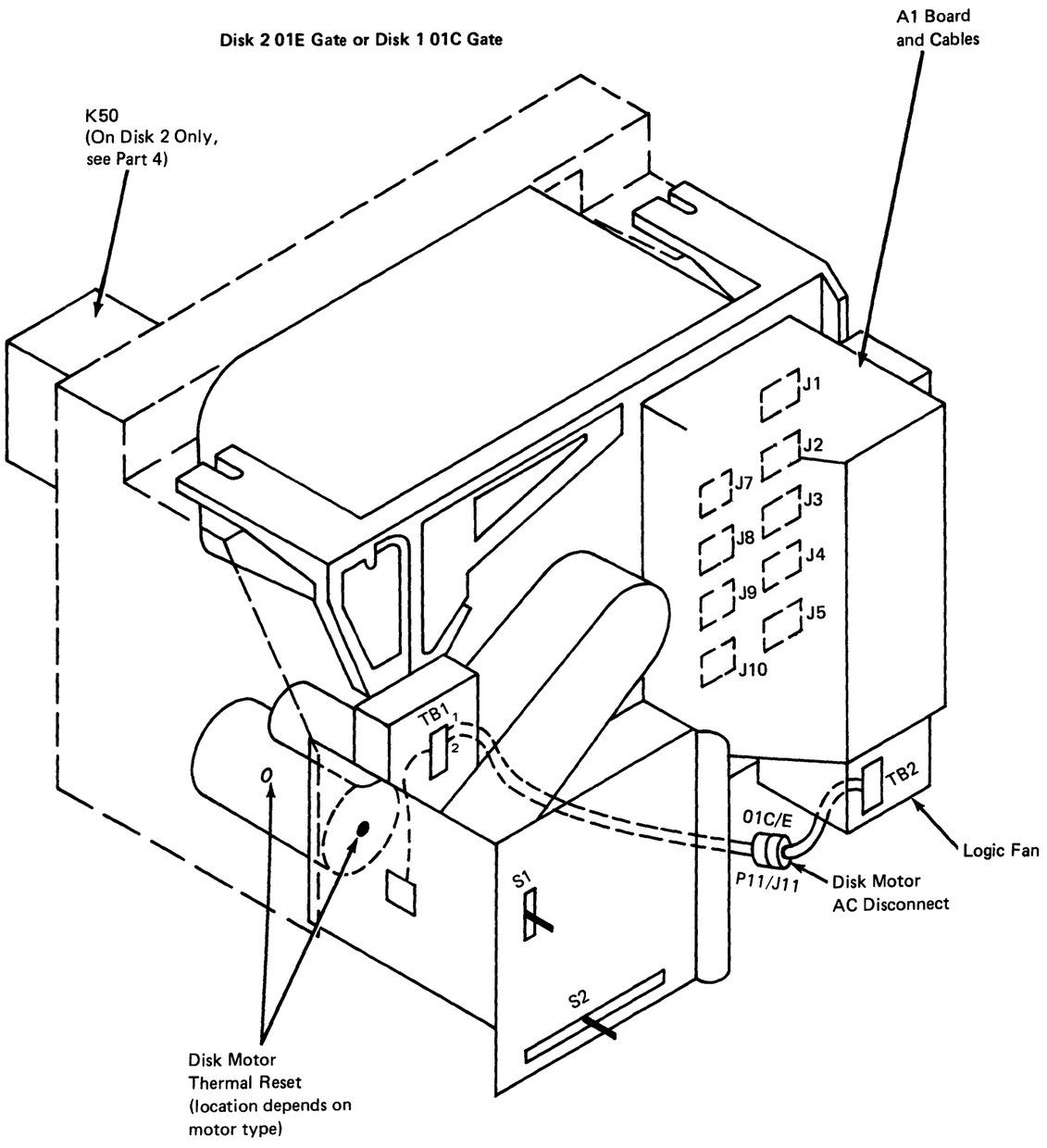




**Figure PA712-2 (Part 1 of 4). 8140 Models BXX Gate and Other Subassembly Locations**



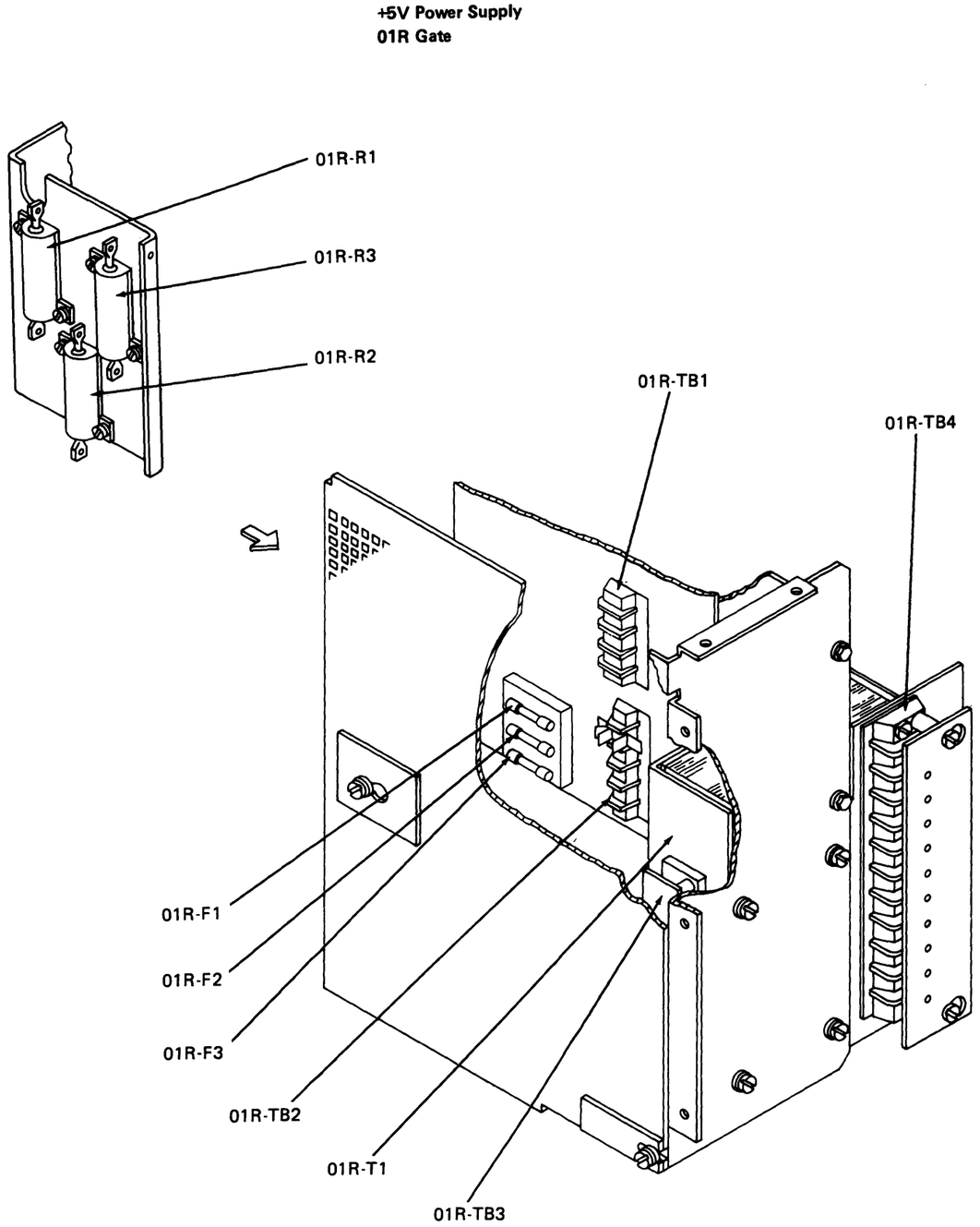
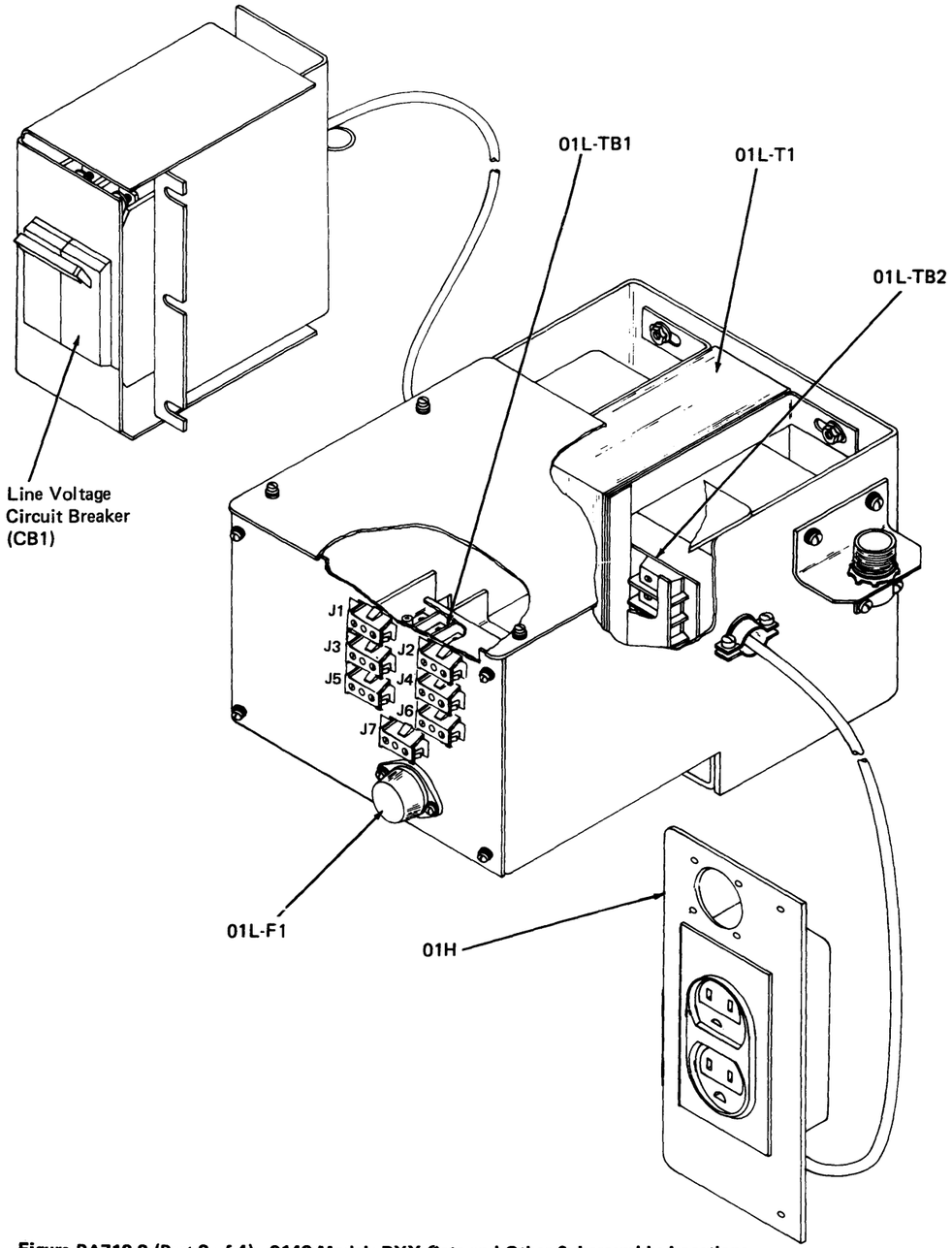




Figure PA712-2 (Part 2 of 4). 8140 Models BXX Gate and Other Subassembly Locations

**AC Distribution Connectors and Convenience Outlet Transformer**
**01-L Gate**




**Disk 1 and 2**
**—4V Power Supply and Controls**
**01M and 01N Gate**

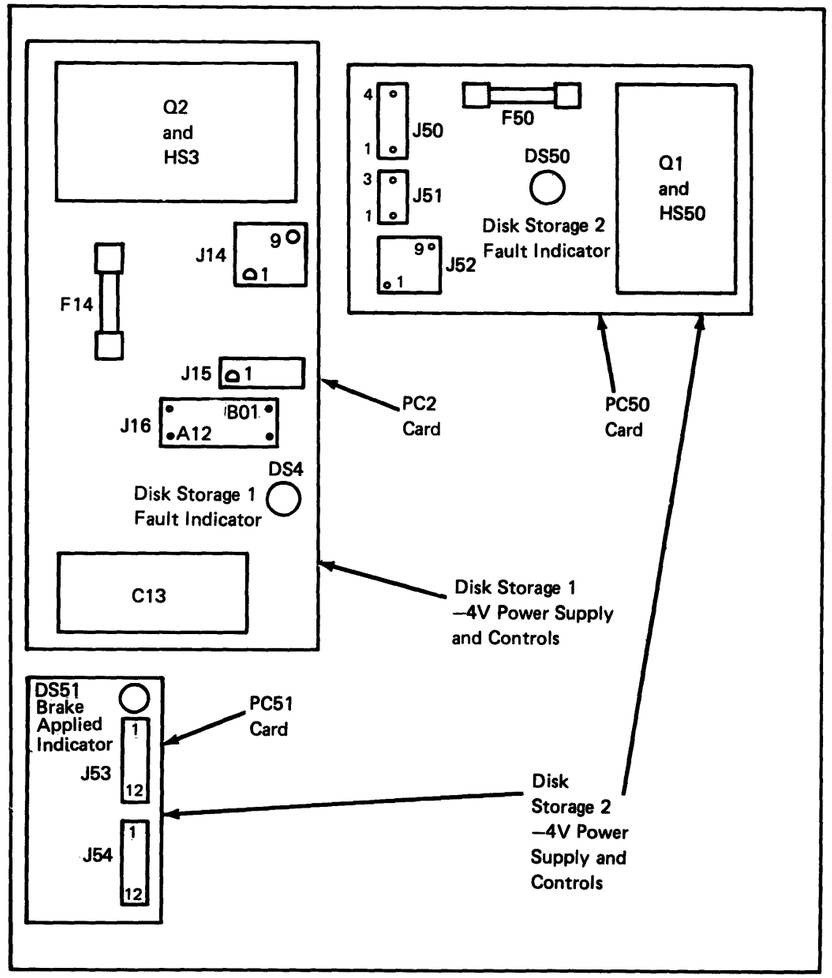
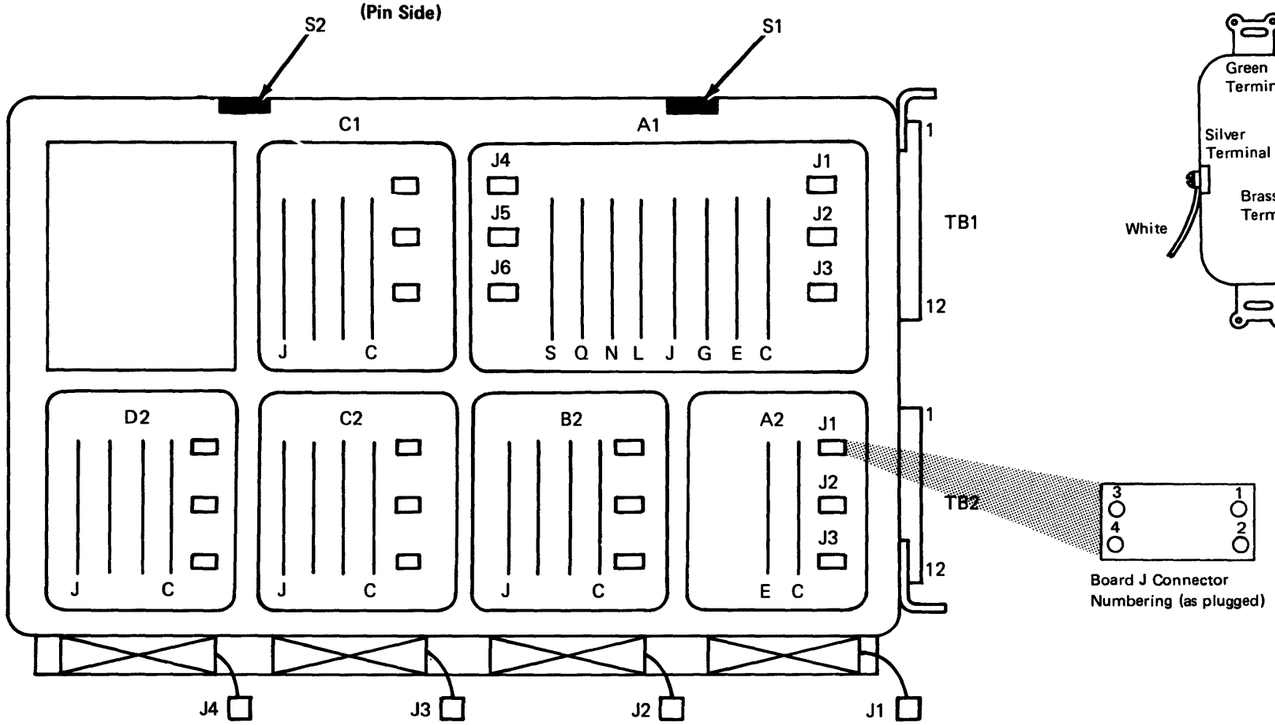
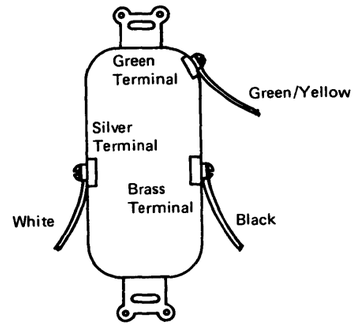



**Figure PA712-2 (Part 3 of 4). 8140 Models BXX Gate and Other Subassembly Locations**

Logic Gate – 01A Gate
(Pin Side)




01H – Convenience Outlet

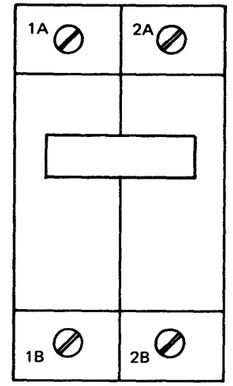






Board J Connector
Numbering (as plugged)

01R – Line Voltage Circuit Breaker (CB1)




K50 Relay

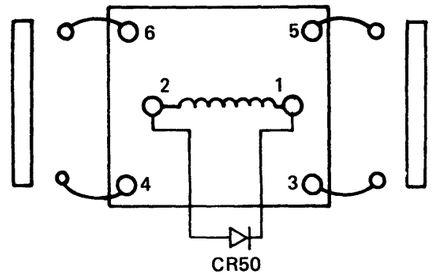
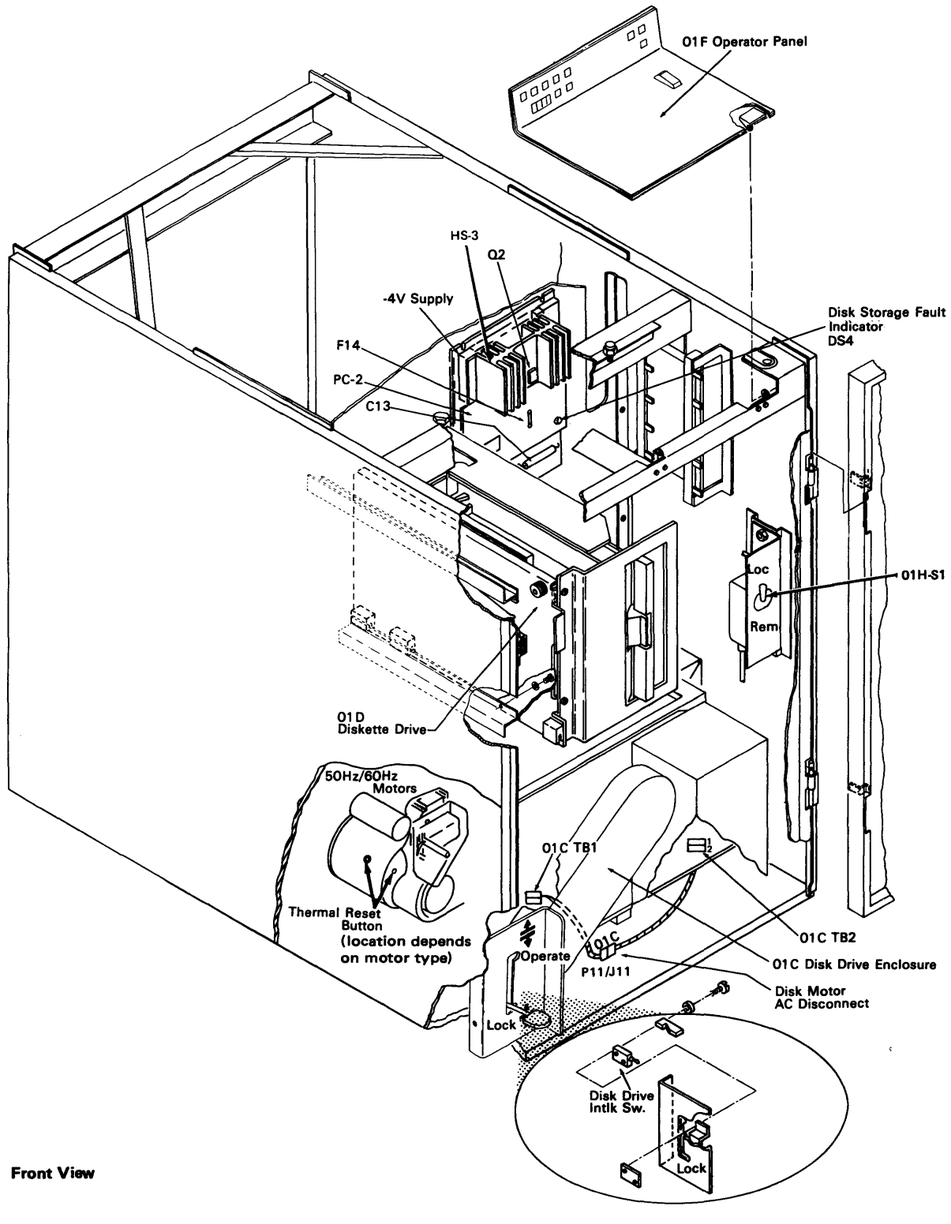
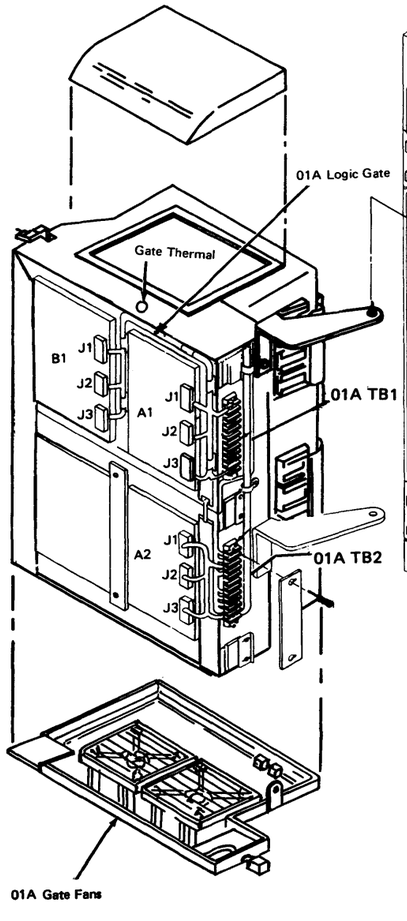


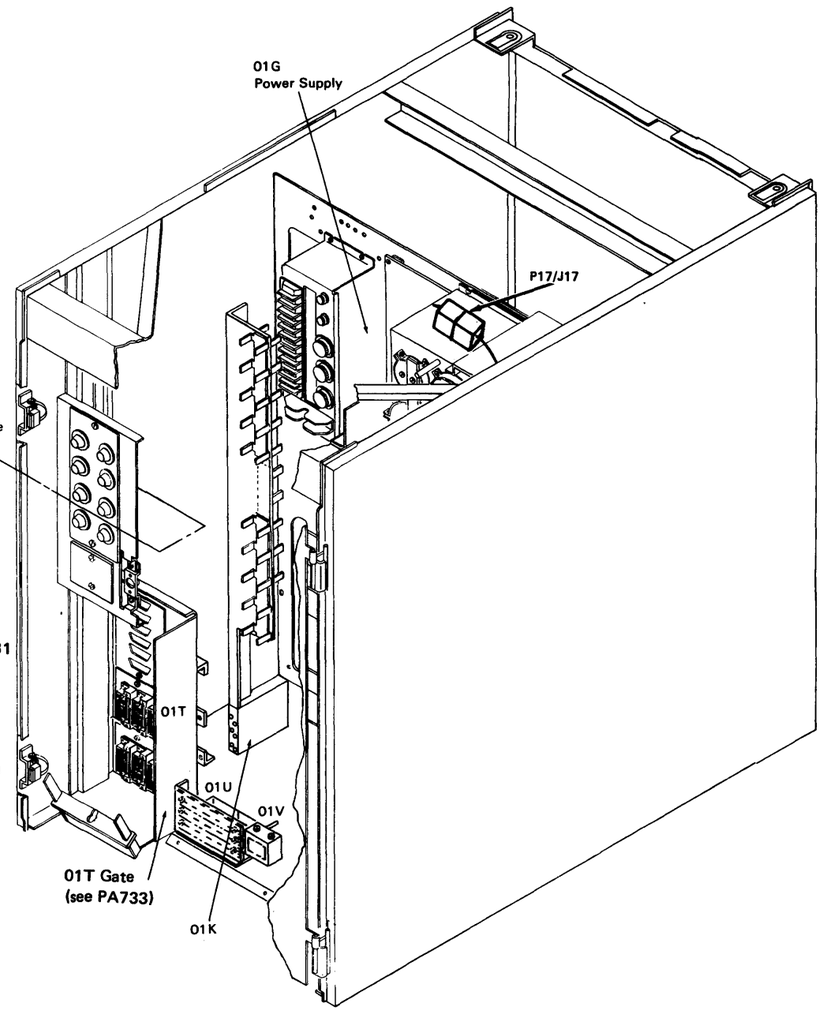

Figure PA712-2 (Part 4 of 4). 8140 Models BXX Gate and Other Subassembly Locations

*PA713 8101 Gate and Other Subassembly Locations*



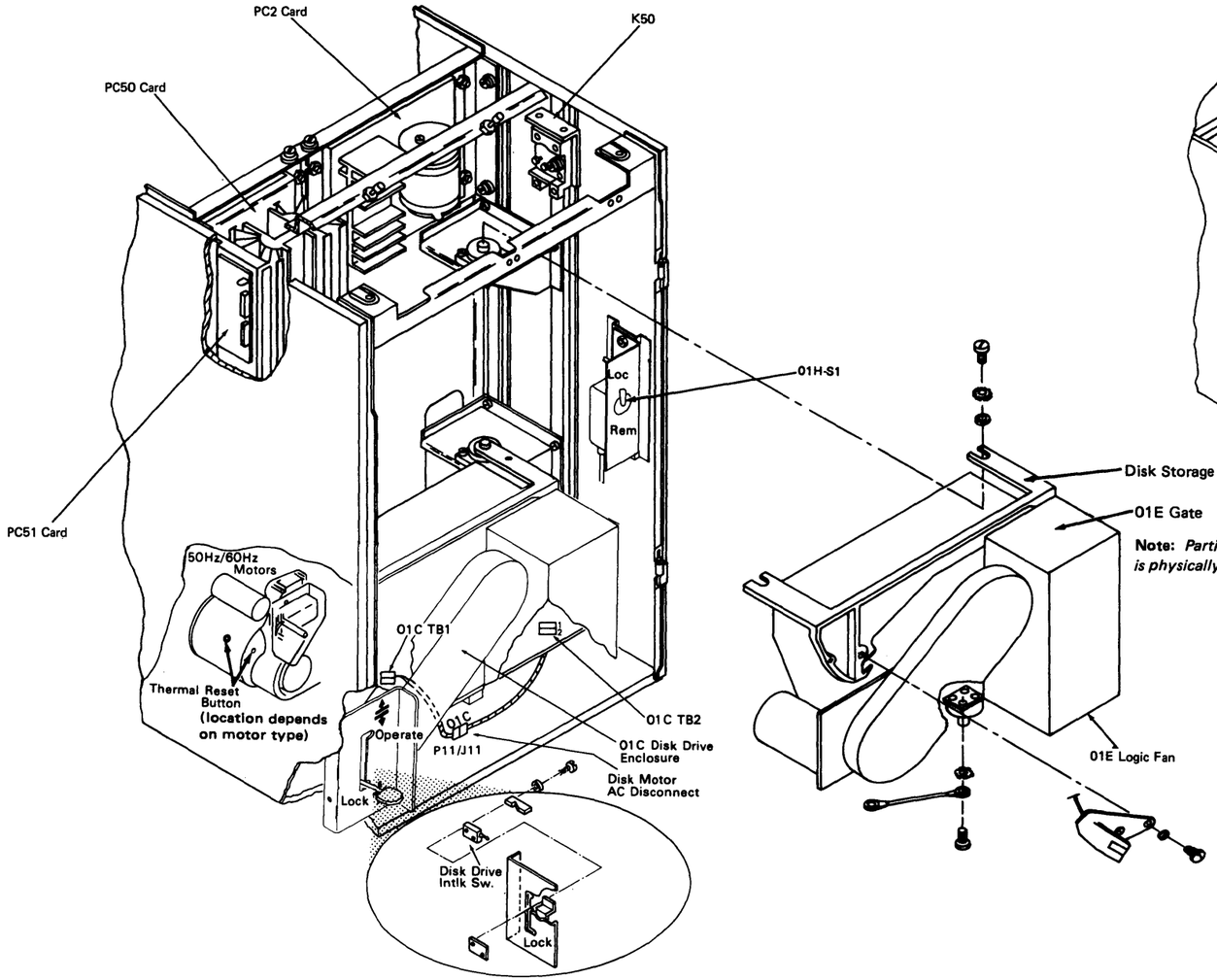

Front View




Rear View

**Figure PA713-1. 8101 Models A1X, A20, and A23 Gate and Other Subassembly Locations**



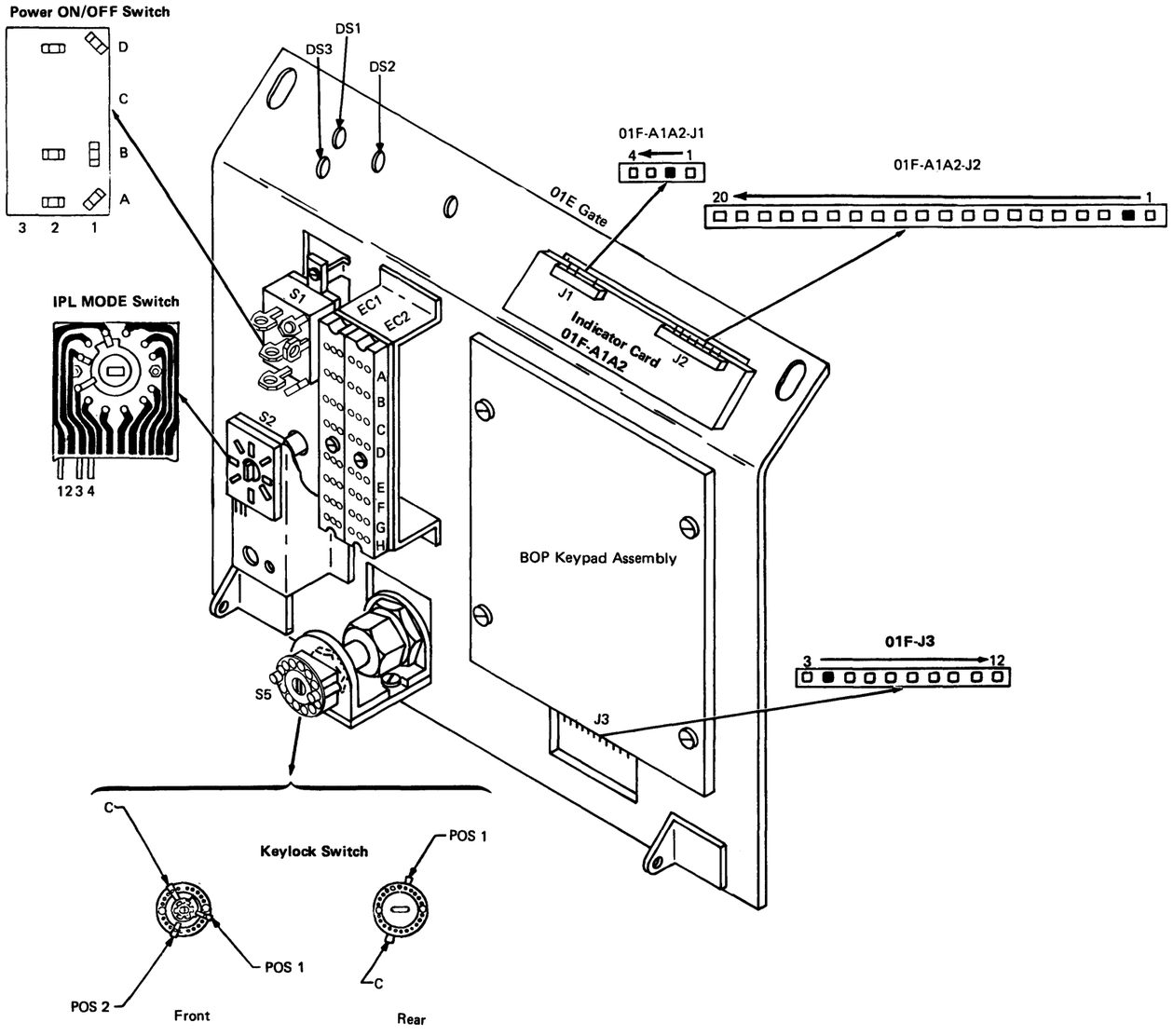

**Note:** *Partial detail only. Disk storage 2 is physically identical to disk storage 1.*

**Note:** *The second disk uses the PC-50 and PC-51 cards.*

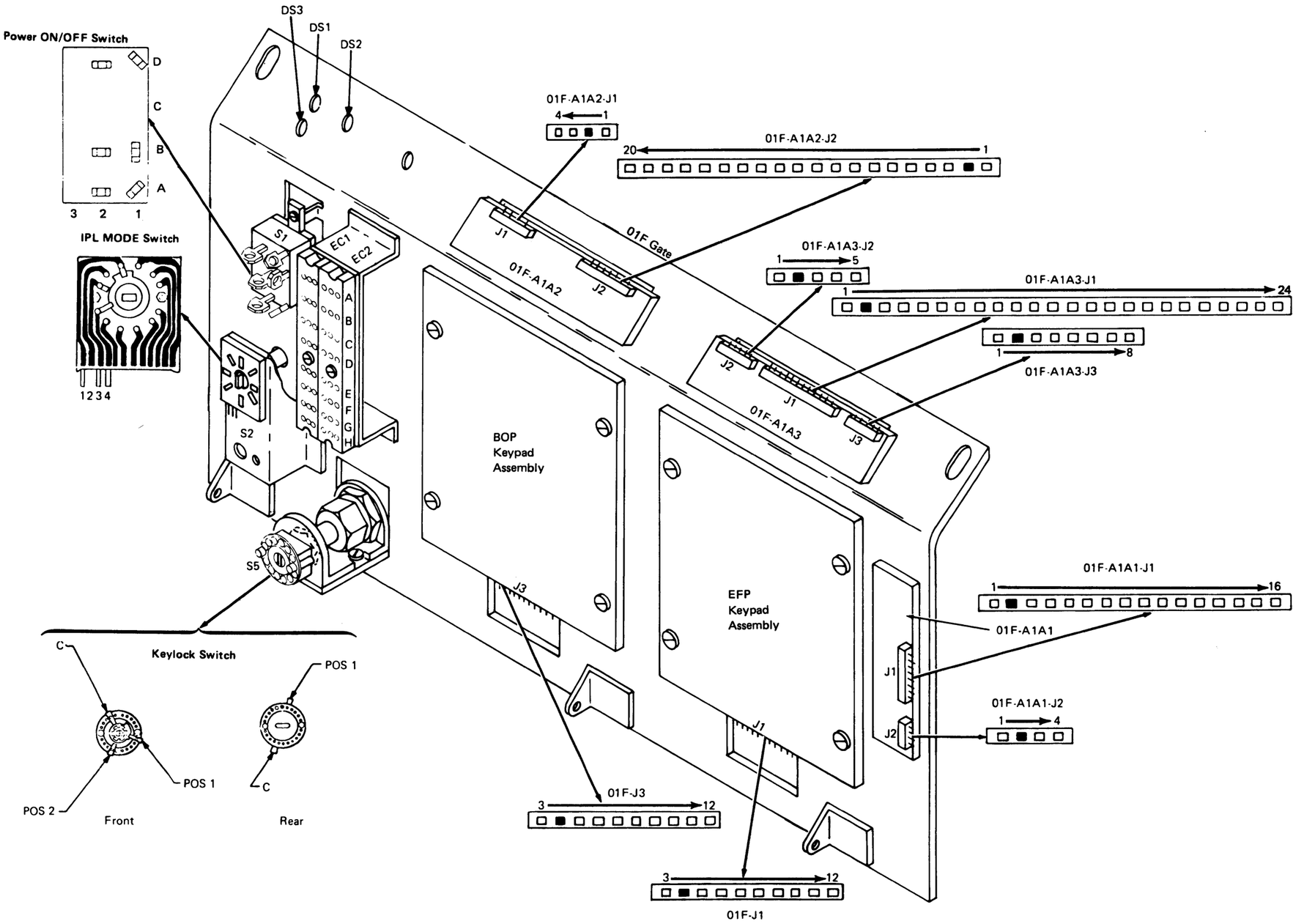
**Figure PA713-2. 8101 Model A25 Gate and Other Subassembly Locations**

## PA720 Operator Panel Component Locations

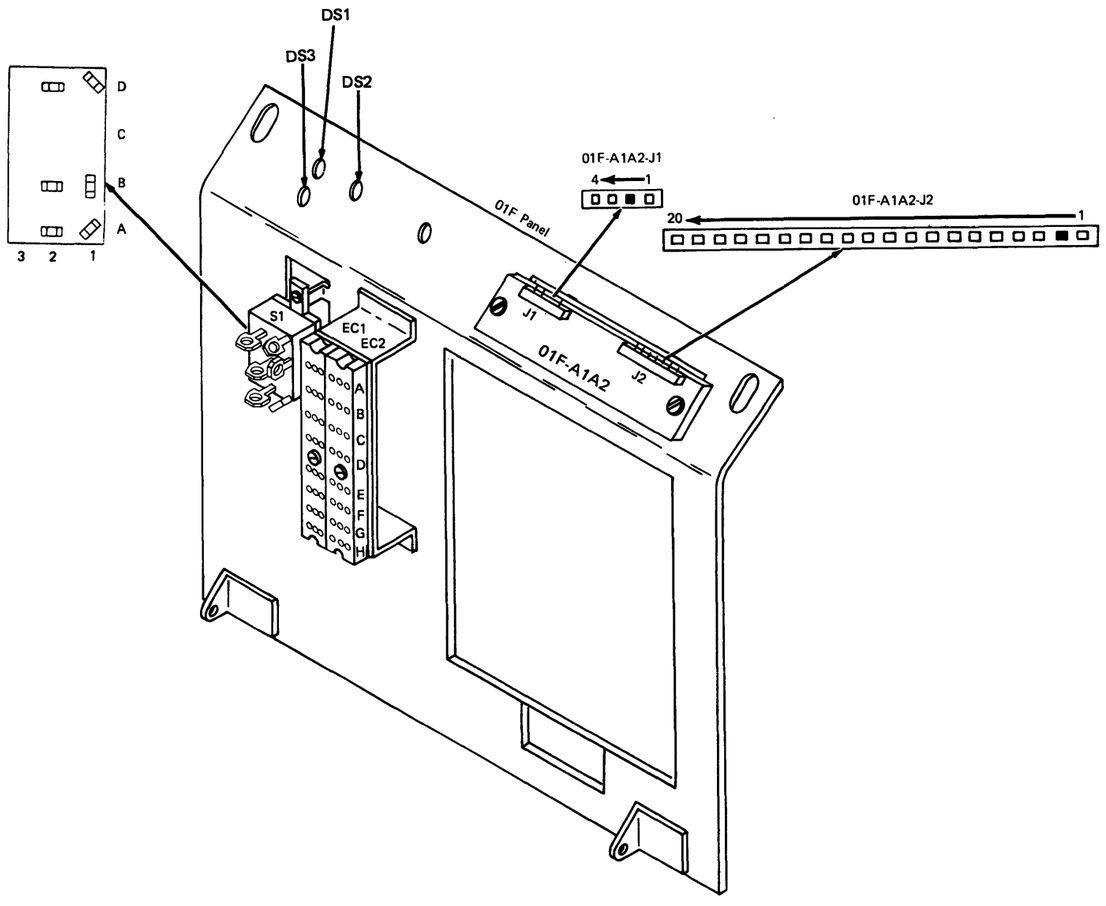
*PA721 8130/8140 Basic Operator Panel Locations*



*PA722 8140 Expanded Function Operator Panel Locations*

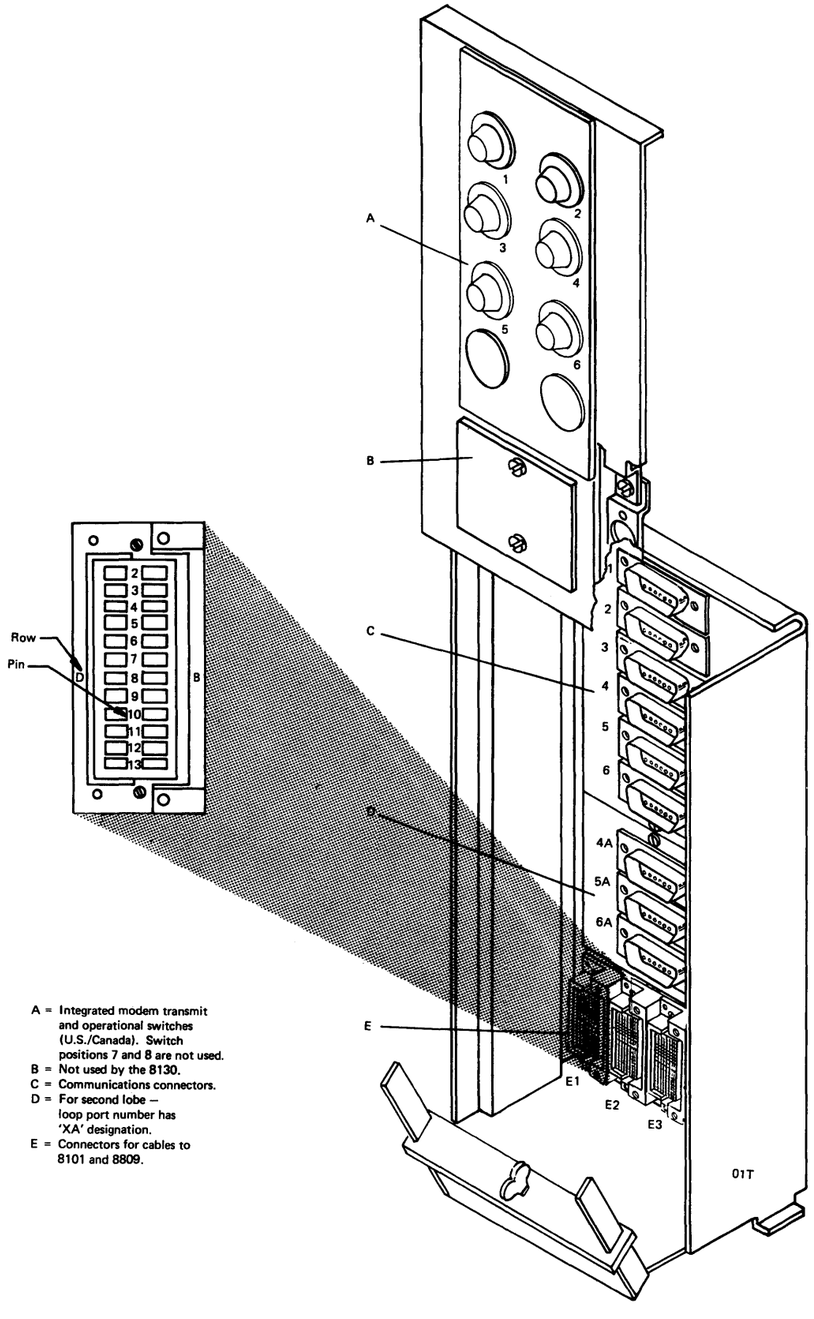


*PA723 8101 Operator Panel Locations*




**PA730 01T Gate (I/O Panel) Locations**

*PA731 8130 01T Gate Locations*




A = Integrated modem transmit and operational switches (U.S./Canada). Switch positions 7 and 8 are not used.
B = Not used by the 8130.
C = Communications connectors.
D = For second lobe — loop port number has 'XA' designation.
E = Connectors for cables to 8101 and 8809.

*PA732 8140 01T Gate Locations*

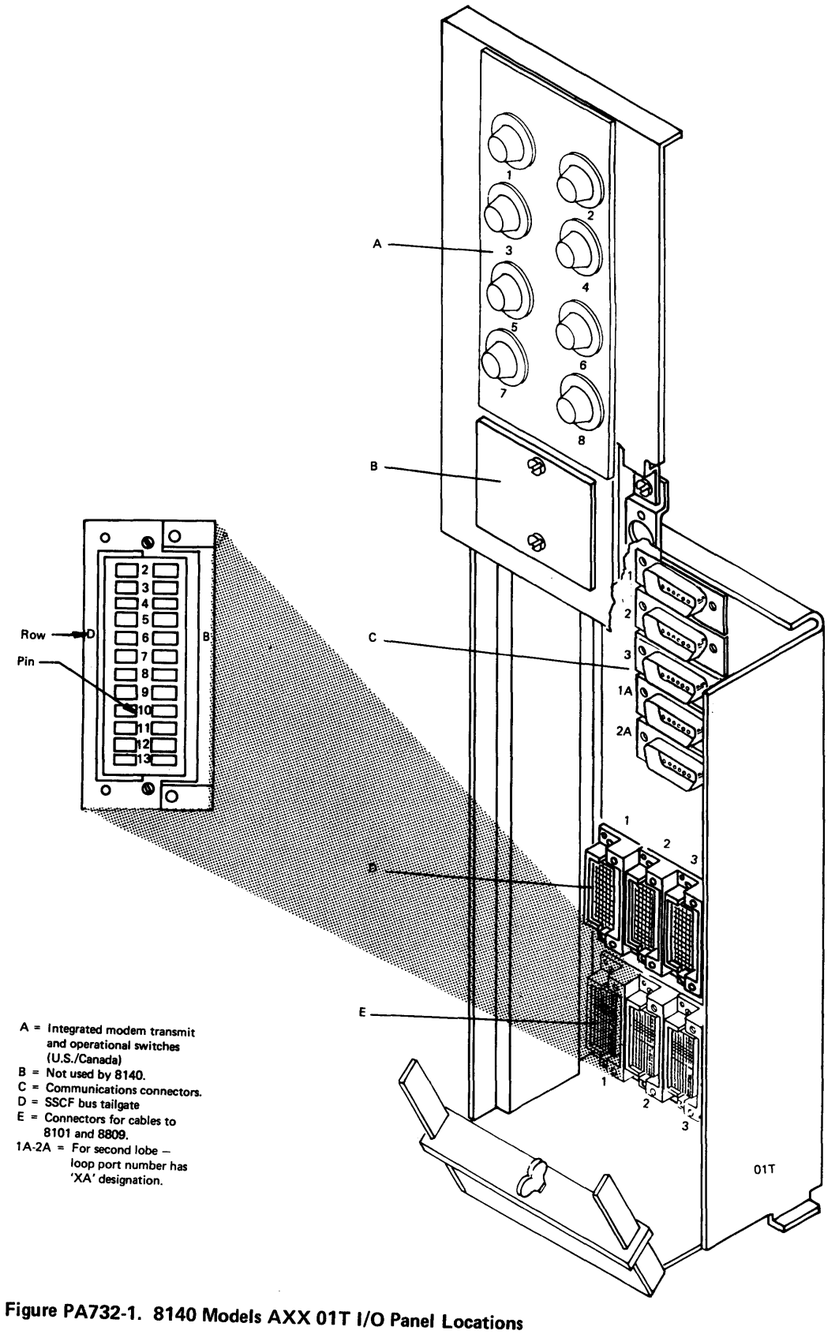



**Figure PA732-1. 8140 Models AXX 01T I/O Panel Locations**

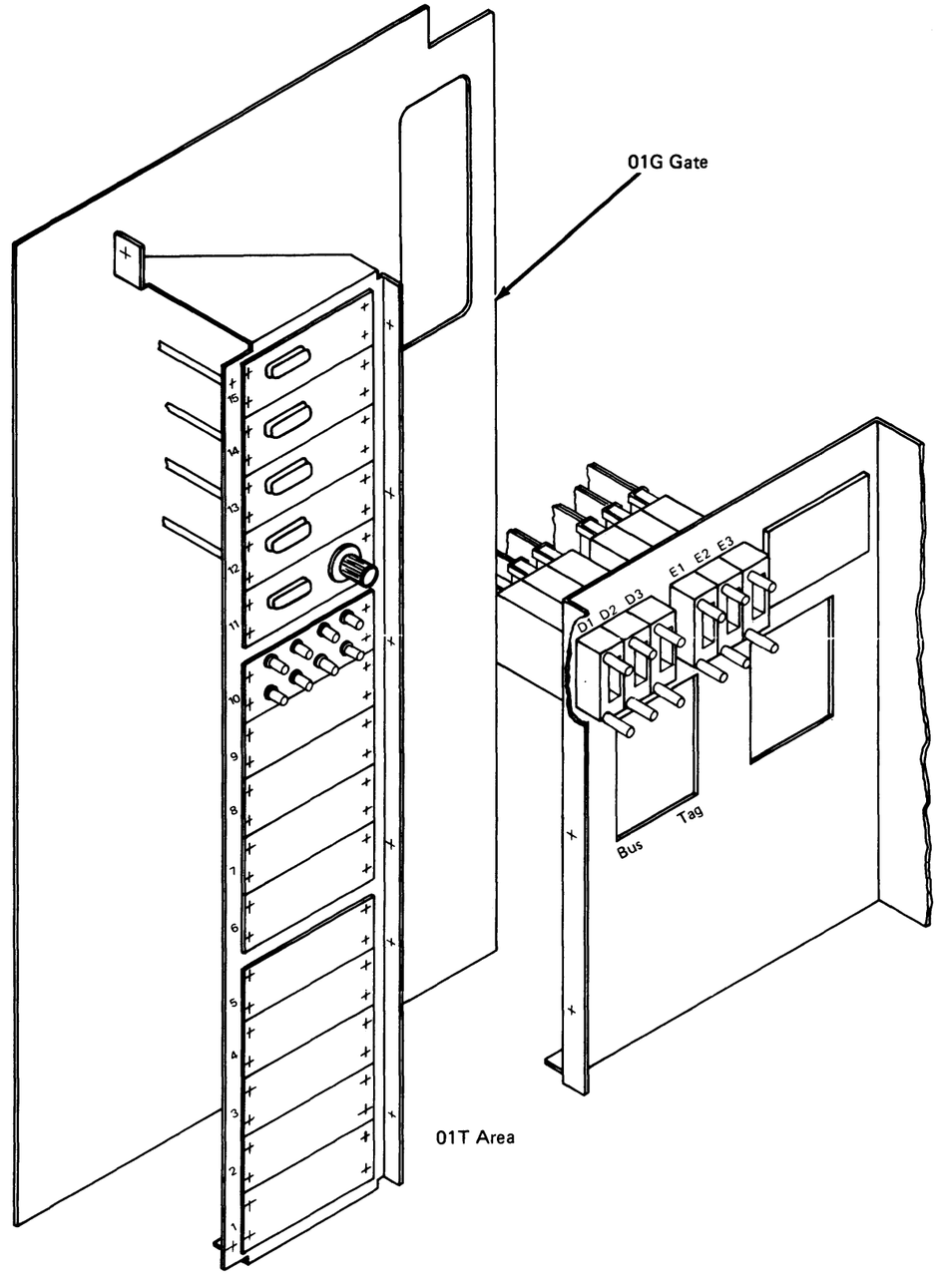
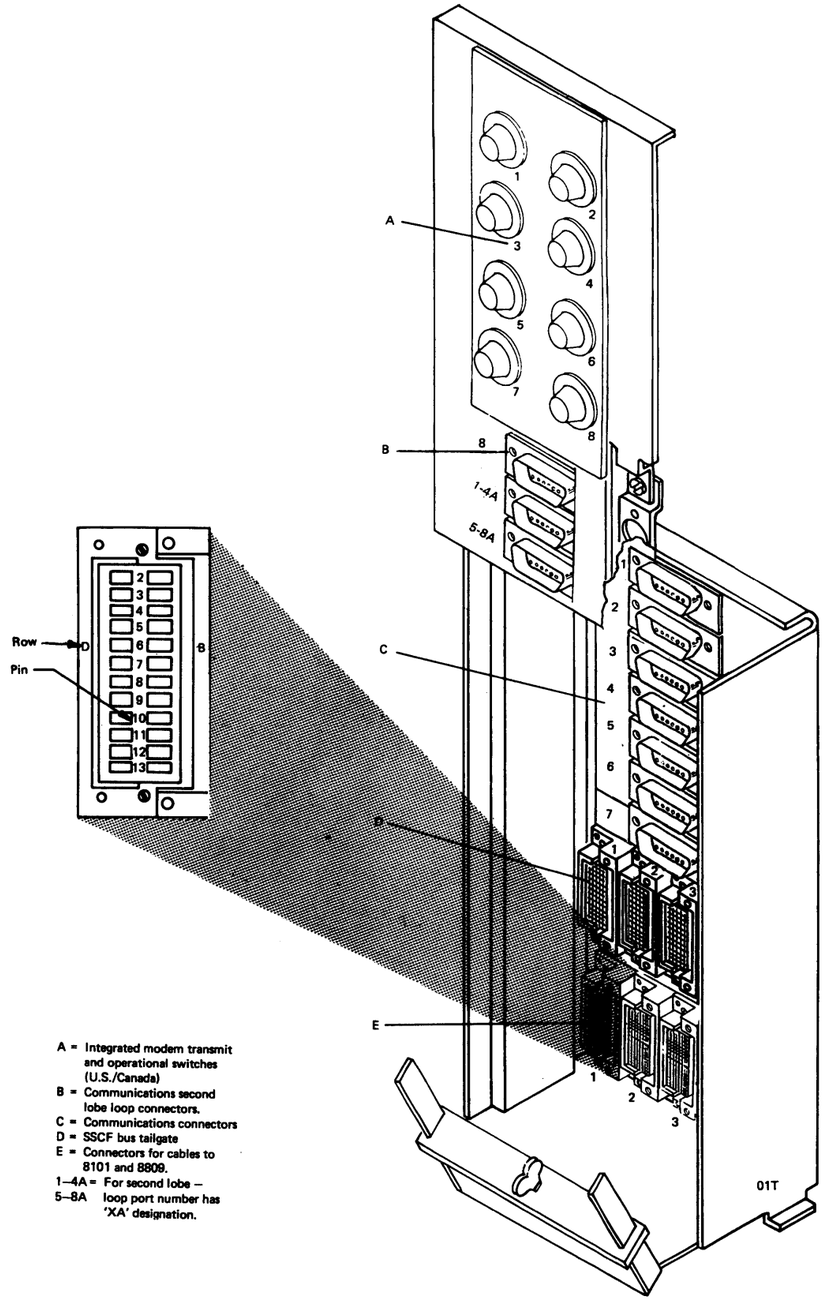



**Figure PA732-2. 8140 Models BXX 01T I/O Panel Locations**

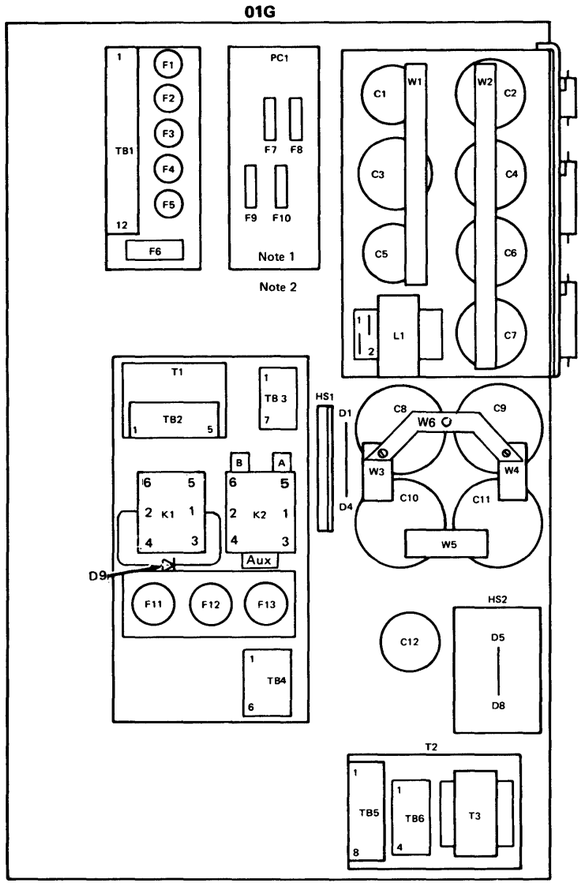
*PA733 8101 01T Gate Locations*




A = Integrated modem transmit and operational switches (U.S./Canada)
B = Communications second lobe loop connectors.
C = Communications connectors
D = SSCF bus tailgate
E = Connectors for cables to 8101 and 8809.
1–4A = For second lobe – 5–8A loop port number has 'XA' designation.

## PA740 01G Gate Power Supply Component Locations

*PA741 8130 01G Gate Power Supply Component Locations*




Rear Service Area

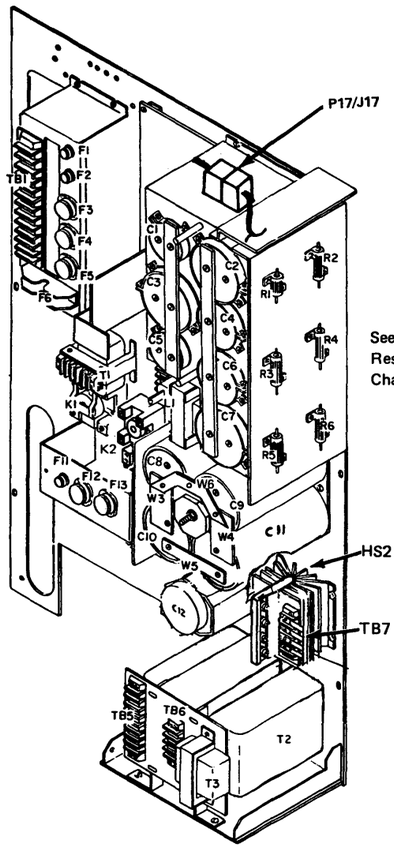
**Note 1:** *PC-3 plugs into PC-1.*
**Note 2:** *See PA440 for capacitor polarity and PA650 for fuse specifications.*

| Resistor Chart | | |
|---|---|---|
| Name | Resistance | Watt |
| R1 | 100 ohms | 25 |
| R2 | 10 ohms | 50 |
| R3 | 5 ohms* | 50 |
| R4 | 2 ohms | 50 |
| R5 | 2 ohms | 50 |
| R6** | 5 ohms | 50 |

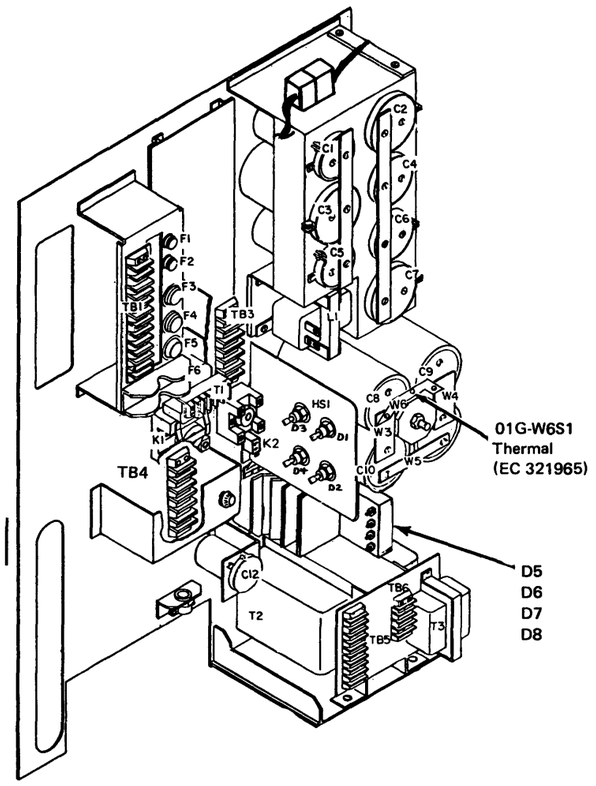
*30 ohms for 768K and 1024K storage. (PN 5724118)
**Disconnected for 768K and 1024K storage.




Front Service Area



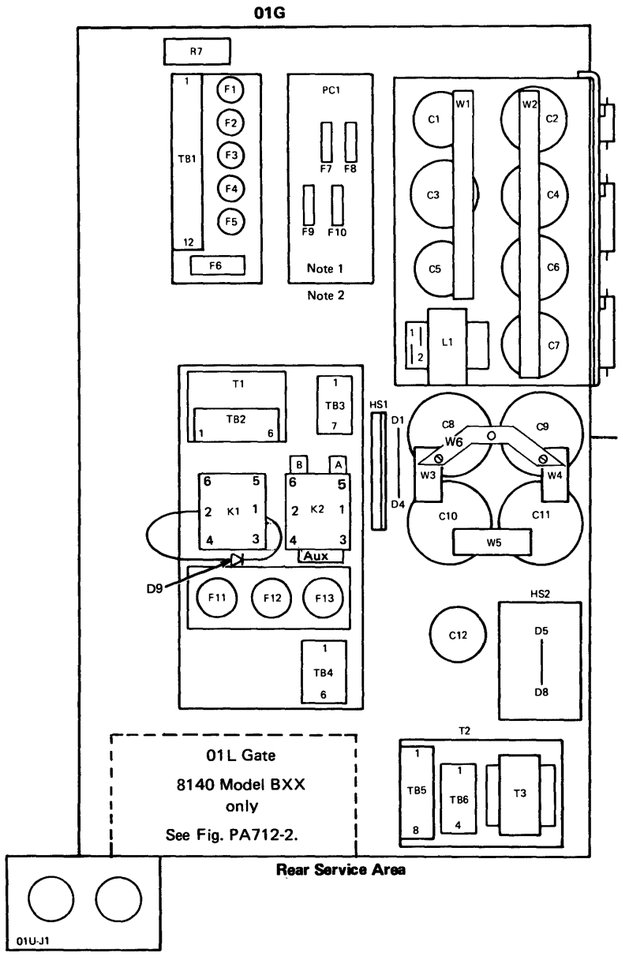

See Resistor Chart



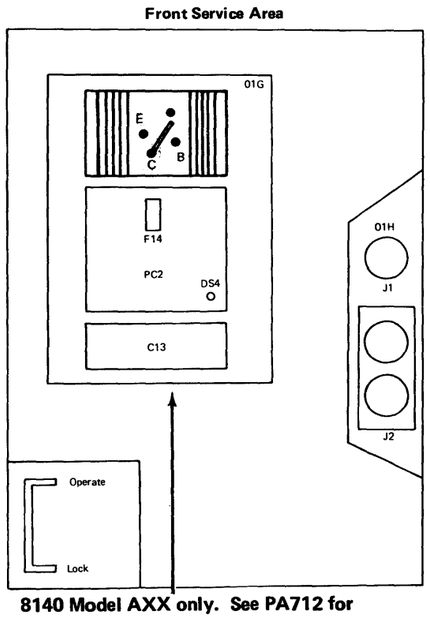

01G-W6S1 Thermal (EC 321965)

D5
D6
D7
D8

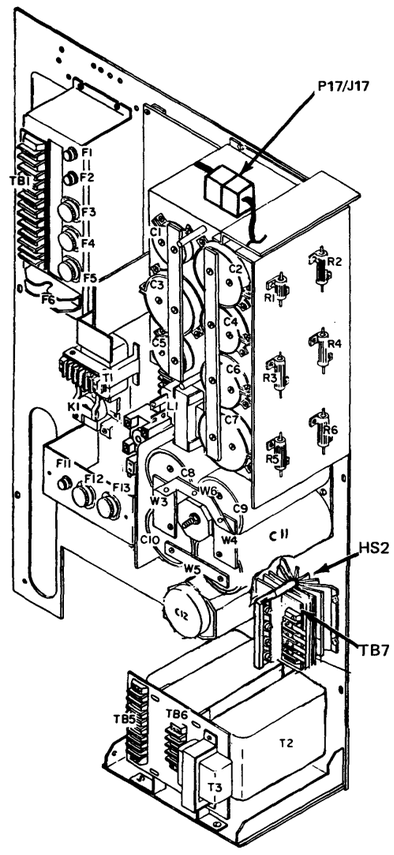
## *PA742 8140 01G Gate Power Supply Component Locations*



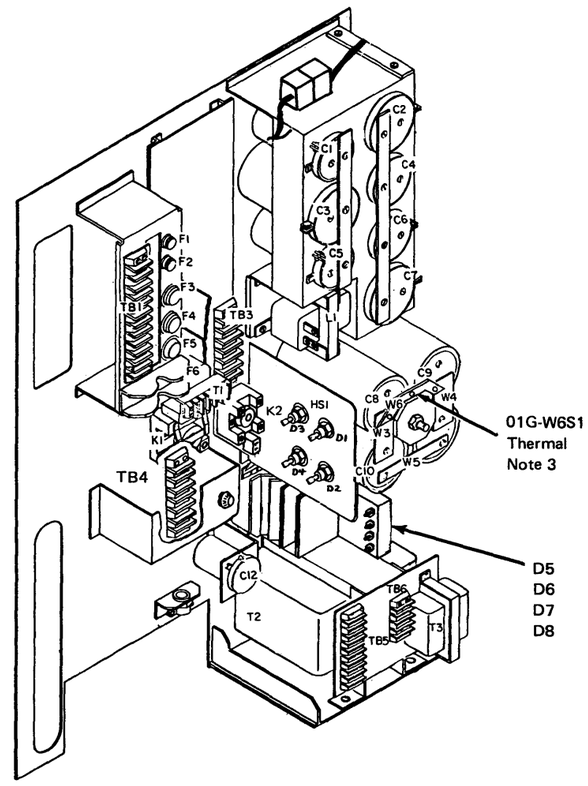

| Resistor Chart | | |
|---|---|---|
| Name | Resistance | Watt |
| R1 | 100 ohms | 25 |
| R2 | 10 ohms | 50 |
| R3 | 5 ohms | 50 |
| R4 | 2 ohms | 50 |
| R5 | 2 ohms | 50 |
| R6 | 5 ohms | 50 |




**8140 Model AXX only. See PA712 for more detailed 8140 Model BXX locations.**




See Resistor Chart

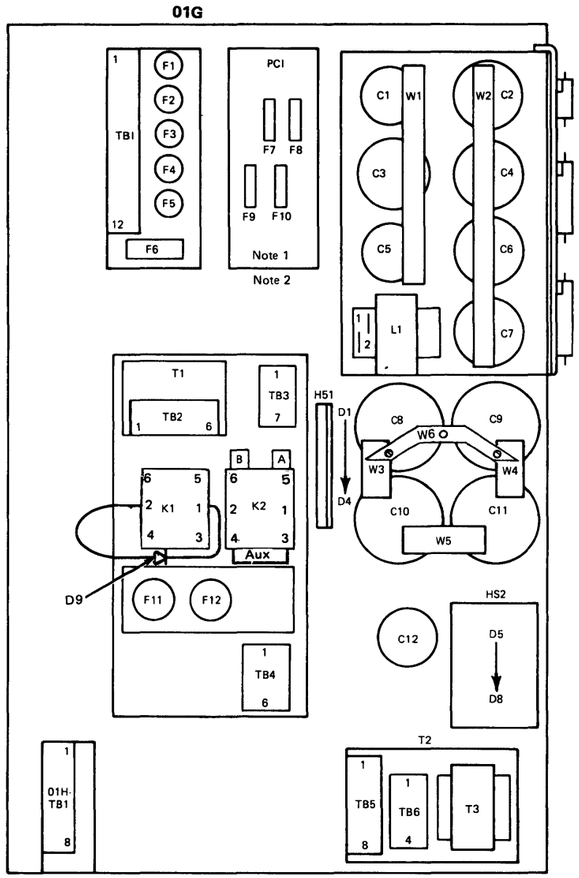



**Note 1:** *PC-3 plugs into PC-1.*

**Note 2:** *See PA440 for capacitor polarity and PA650 for fuse specifications.*

**Note 3:** *Present with EC 867486 (8140 AXX) or EC 862250 (8140 BXX) installed.*

*PA743 8101 01G Gate Power Supply Component Locations*



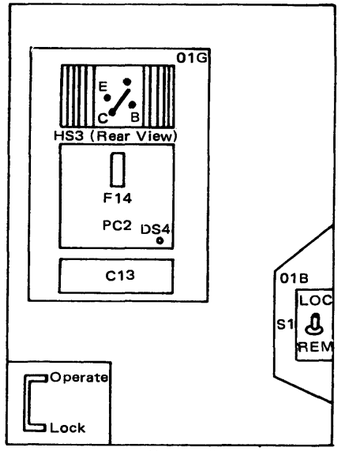

Rear Service Area

**Note 1:** *PC-3 and PC-4 plug into PC-1.*

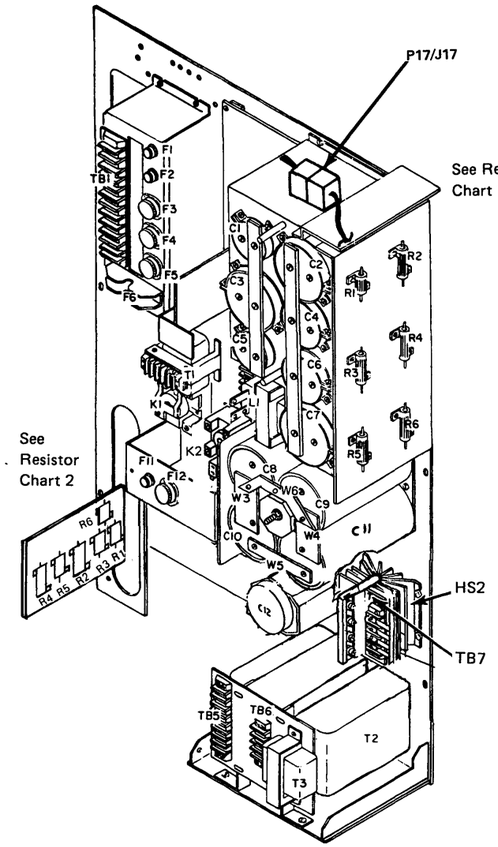
**Note 2:** *See PA440 for capacitor polarity and PA650 for fuse specifications.*

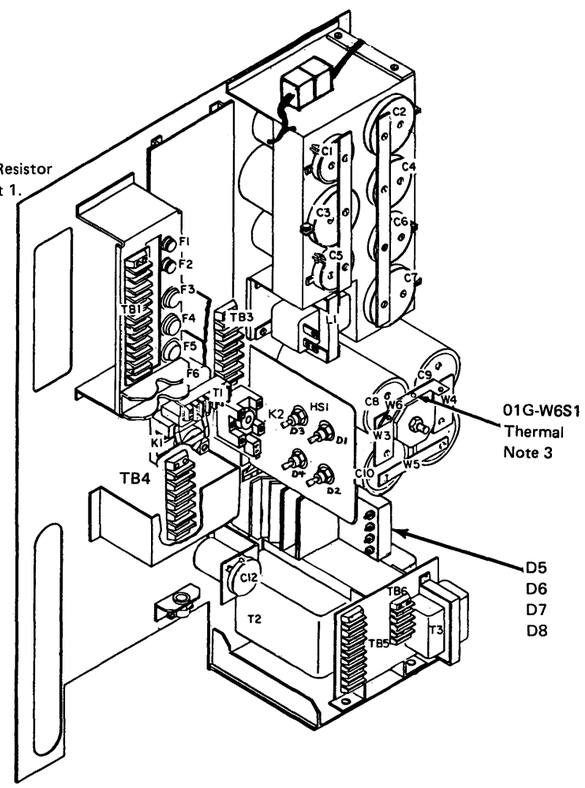
**Note 3:** *Present only on Model A25 with EC 867485 installed.*

| Resistor Chart 1 | | |
|---|---|---|
| Name | Resistance | Watt |
| R1 | 100 ohms | 25 |
| R2 | 10 ohms | 50 |
| R3 | 5 ohms | 50 |
| R4 | 2 ohms | 50 |
| R5 | 2 ohms | 50 |
| R6 | 5 ohms | 50 |

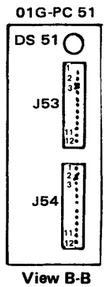



Front Service Area

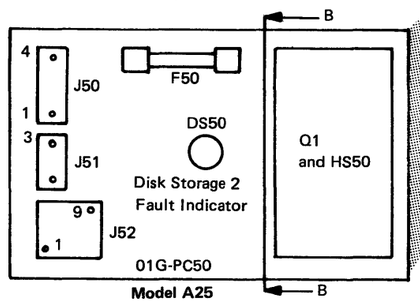


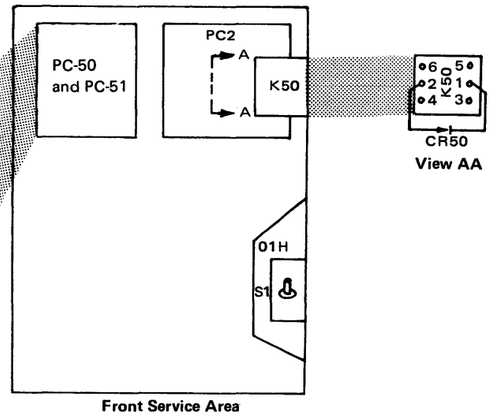

| Resistor Chart 2 | | |
|---|---|---|
| Name | Resistance | Watt |
| R1 | 2 ohms | 25 |
| R2 | 1 ohm | 50 |
| R3 | 15 ohms | 10 |
| R4 | 1 ohm | 50 |
| R5 | 8 ohms | 25 |
| R6 | 2 ohms | 25 |




View B-B




Model A25




View AA

Front Service Area
Model A25

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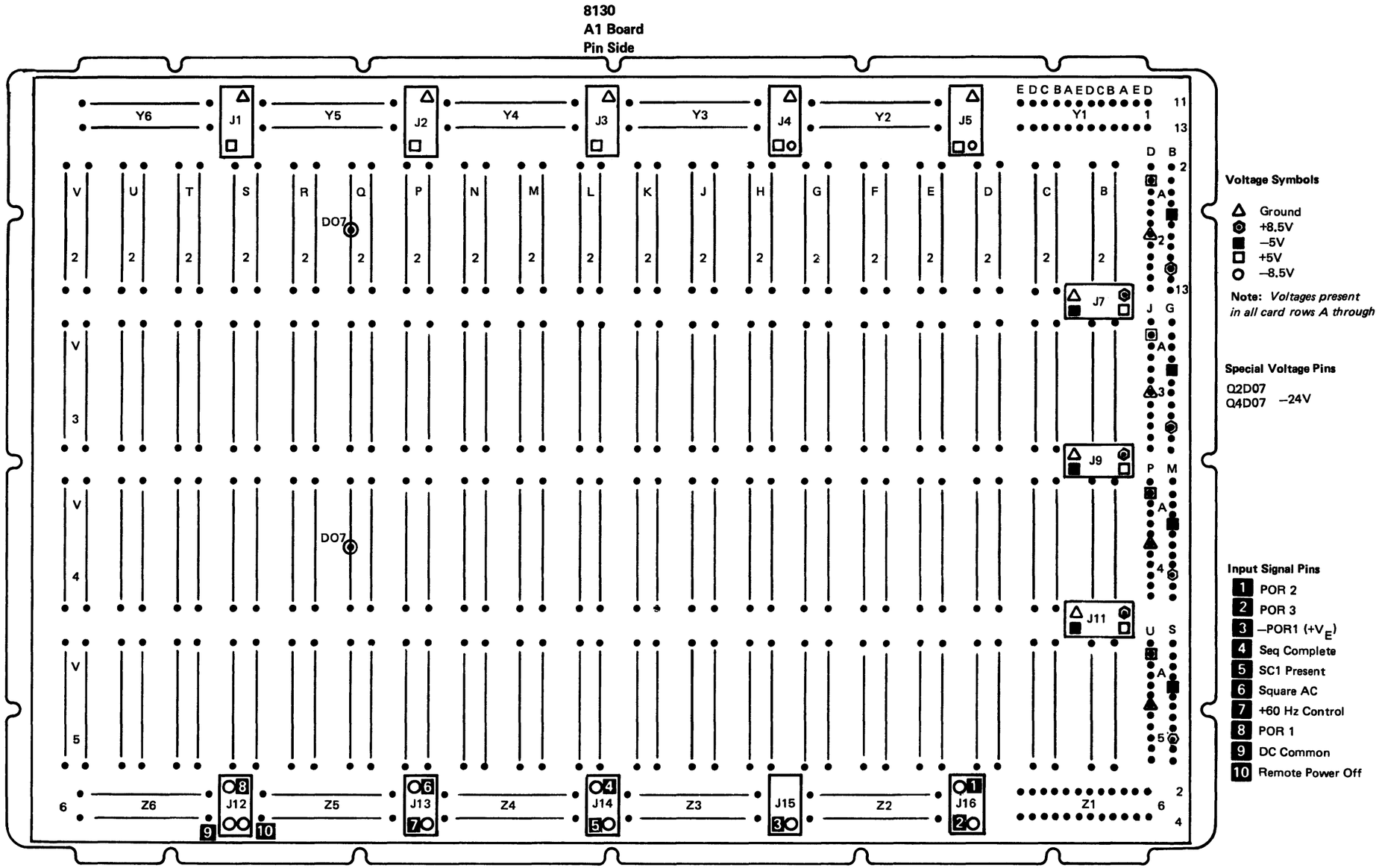
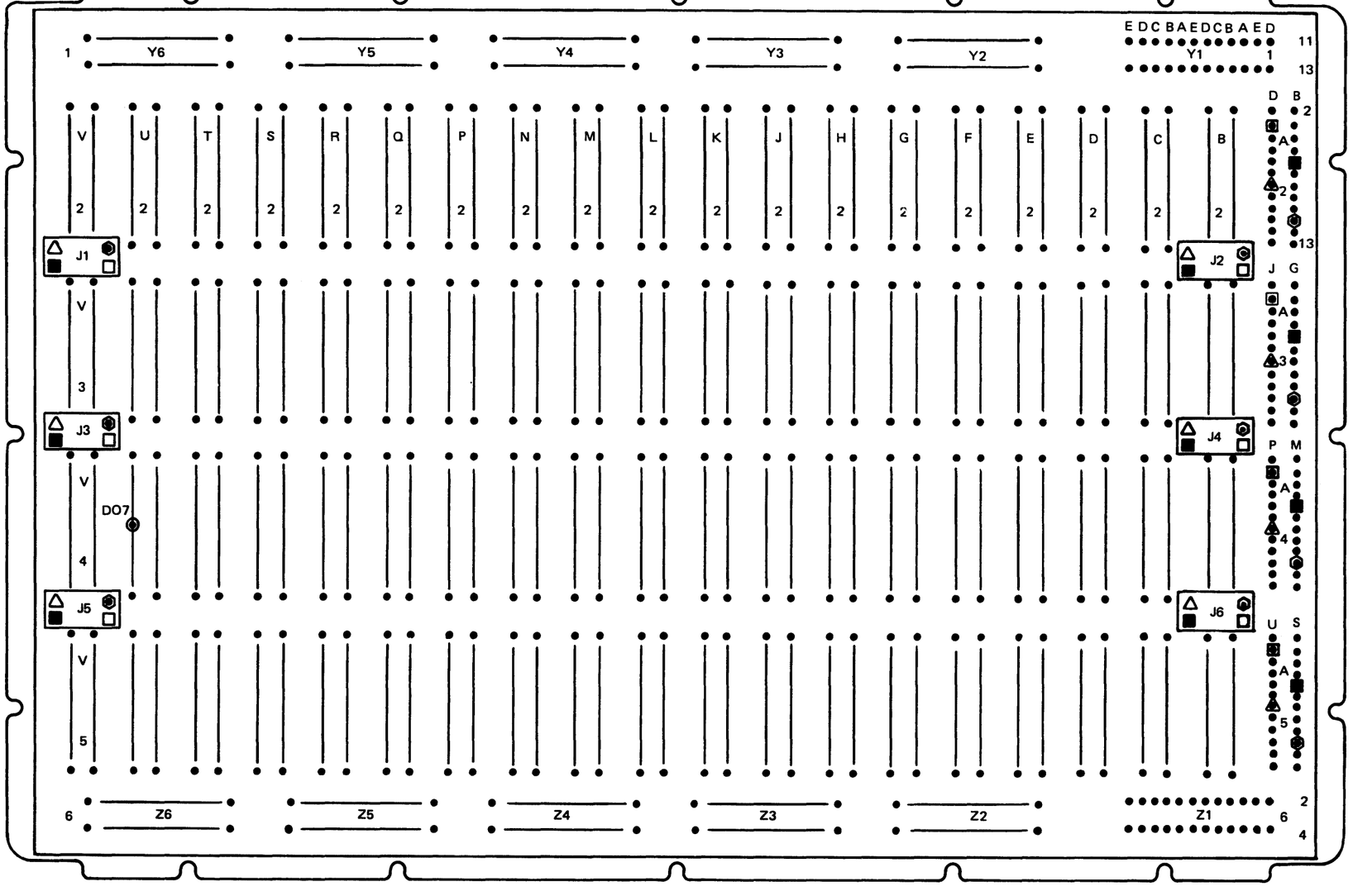
## PA750 Board DC Voltage Distribution

*PA751 8130 Board Voltages*



**8130**
**A2 Board**
**Pin Side**




**Voltage Symbols**

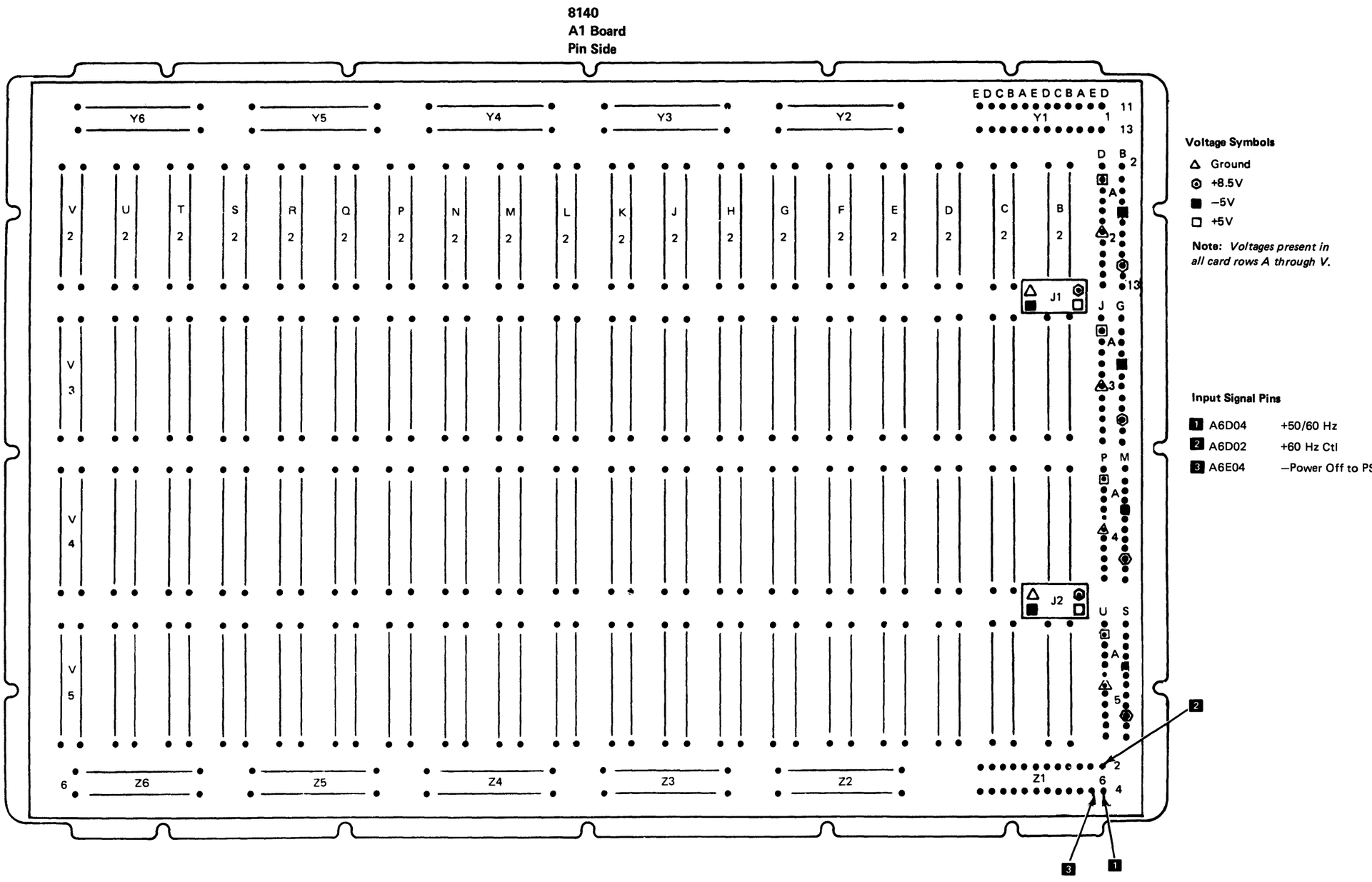
- Ground
- +8.5V
- −5V
- +5V

**Note:** *Voltages present in all card rows A through V.*

**Special Voltage Pin**

U4D07 −8.5V

*PA752 8140 Board Voltages*




**Voltage Symbols**

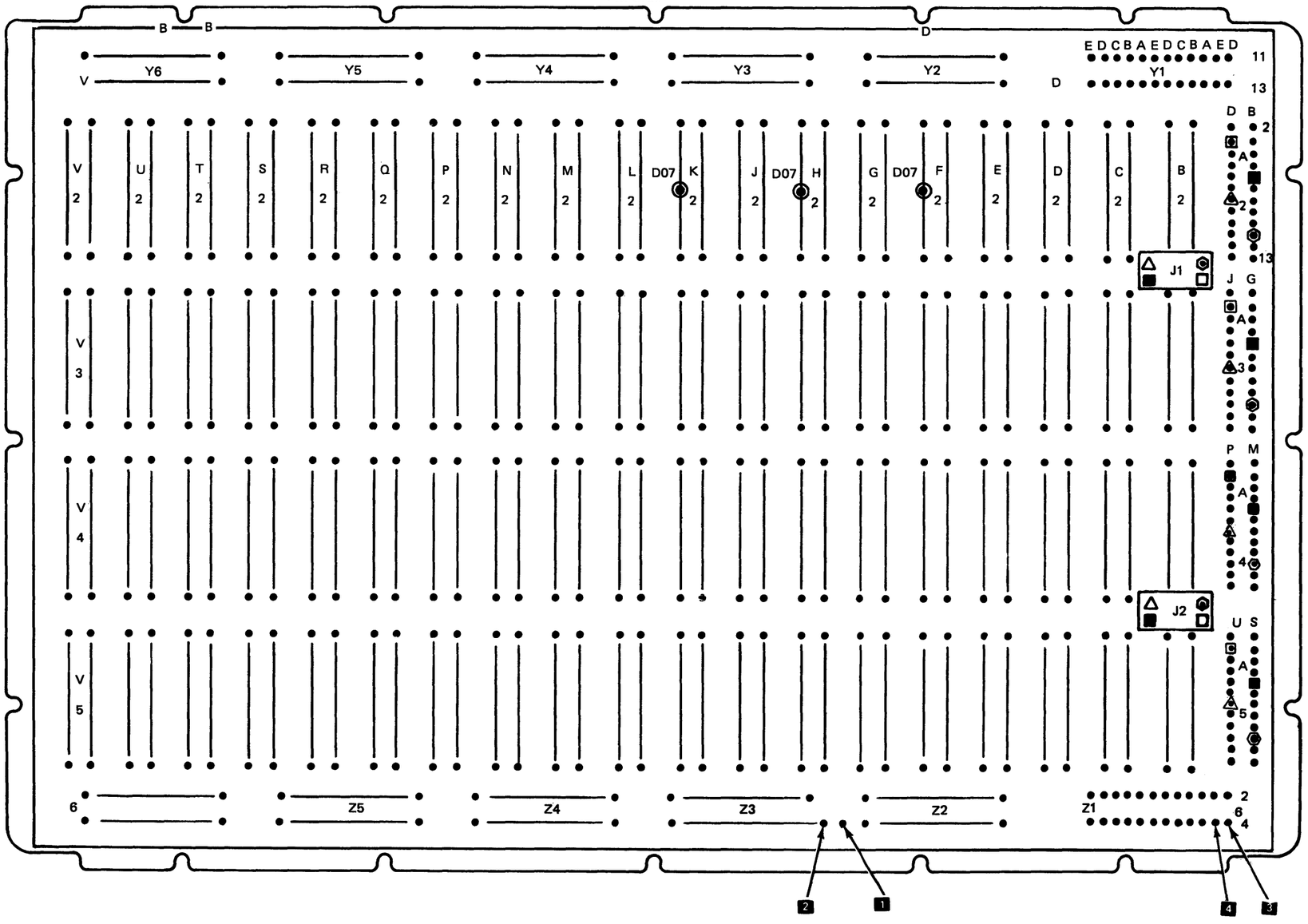
- △ Ground
- ⊙ +8.5V
- ■ −5V
- □ +5V

**Note:** *Voltages present in all card rows A through V.*

**Input Signal Pins**

| | | |
|---|---|---|
| 1 | A6D04 | +50/60 Hz |
| 2 | A6D02 | +60 Hz Ctl |
| 3 | A6E04 | −Power Off to PS |

**8140**
**A2 Board**
**Pin Side**




**Voltage Symbols**

- △ Ground
- ⬡ +8.5V
- ■ –5V
- □ +5V

**Note:** *Voltages present in all card rows A through V.*

**Special Voltage Pins**

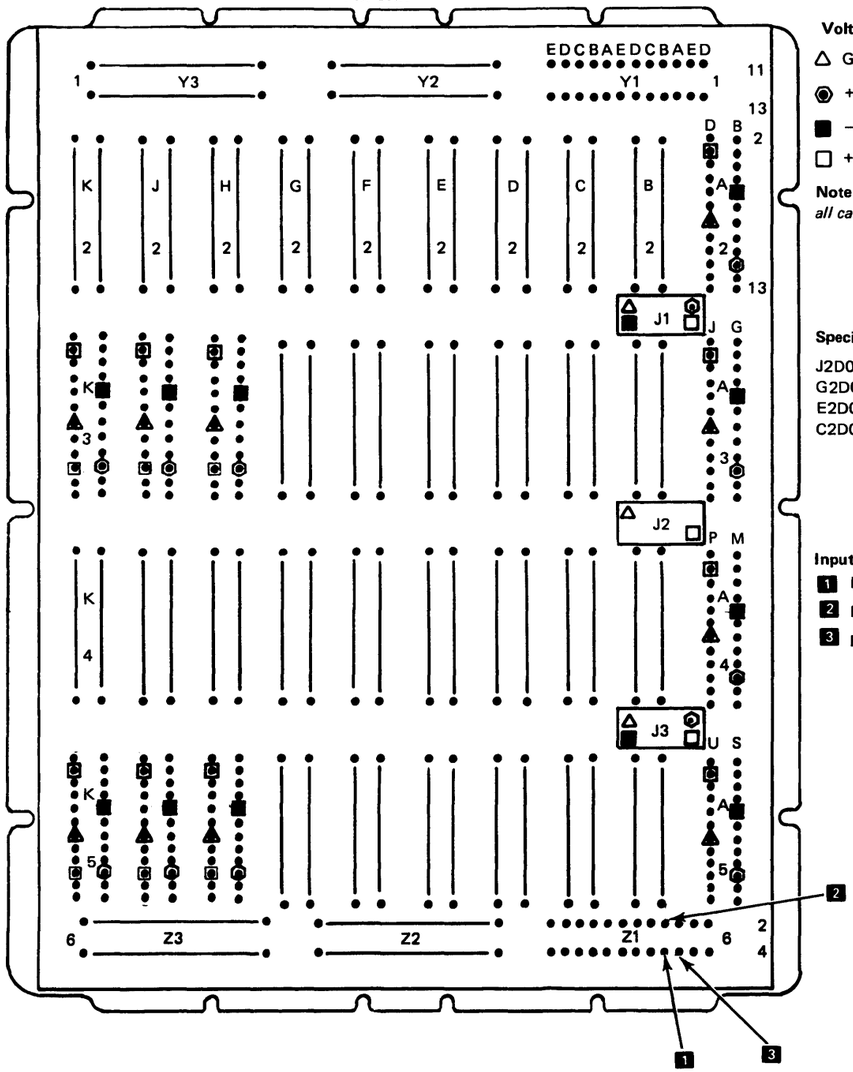
F2D07, H2D07, K2D07 } –8.5V

**Input Signal Pins**

| | | |
|---|---|---|
| 1 | H6A04 | -Pwr Seq Complete (Models A3X, A4X) |
| 2 | H6B04 | –POR1 ($+V_E$) (Models A3X, A4X) |
| 3 | A6D04 | -Pwr Seq Complete (Models A5X) |
| 4 | A6E04 | –POR1 ($+V_E$) (Models A5X) |

*PA753 8101 Board Voltages*

**8101 A1 or B1 Board**
**Pin Side**




**Voltage Symbols**
- △ Ground
- ⬡ +8.5V
- ■ –5V
- □ +5V

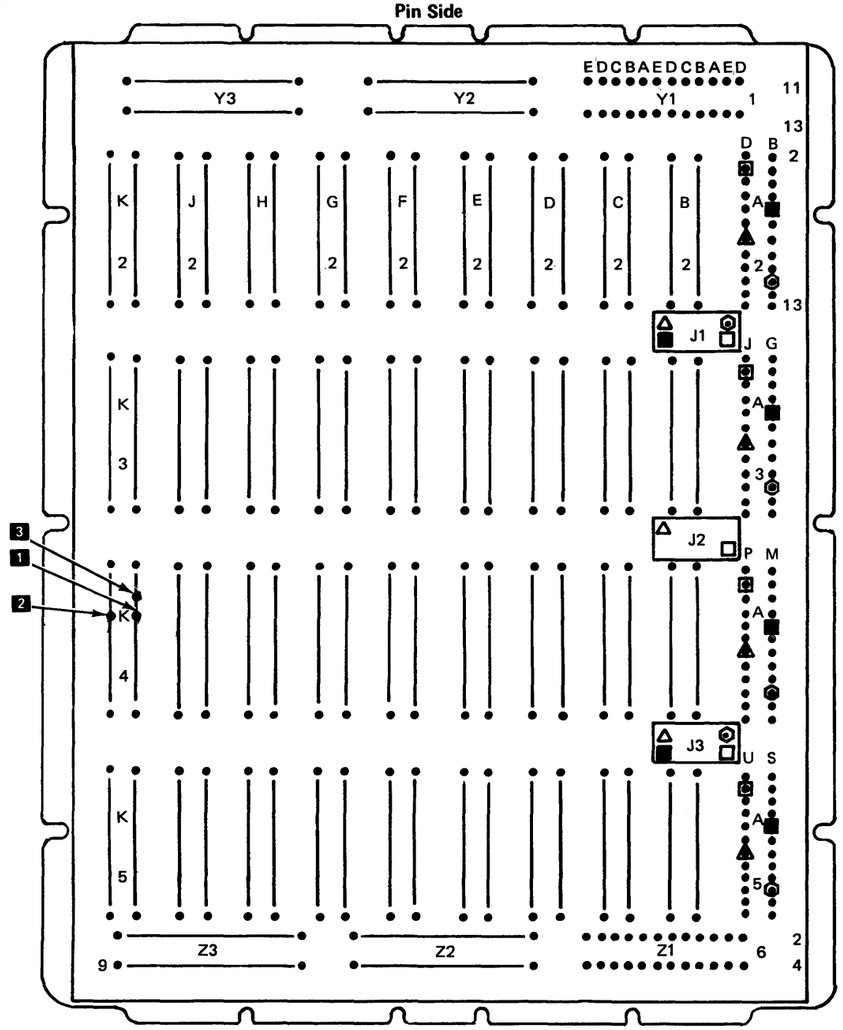
**Note:** *Voltages present in all card rows A through K.*

**Special Voltage Pins**

J2D07
G2D07
E2D07
C2D07
} -8.5V

**Input Signal Pins (A1 board only)**
- 1 B6B04 –POR1 (+$V_E$)
- 2 B6B02 +5V Ctl
- 3 B6A04 –Turn-On Power

**8101 A2 Board**
**Pin Side**

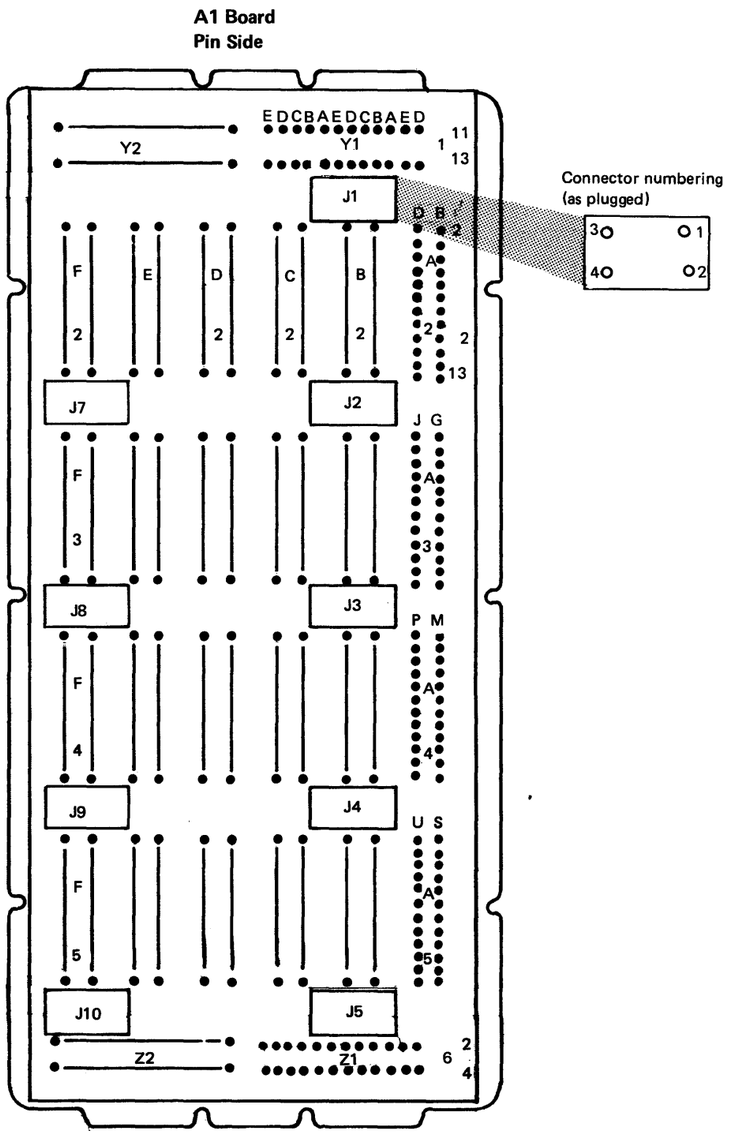



**Voltage Symbols**
- △ Ground
- ⬡ +8.5V
- ■ +5V
- □ –5V

**Note:** *Voltages present in all card rows A through K.*

**Input Signal Pins**
- 1 K4B04 –Turn-On Power
- 2 K4D05 +5V Ctl
- 3 K4B05 –POR1 (+$V_E$)

*PA754 Disk Board Signal and Voltage Distribution (01C and 01E Gates)*




J1-2 — B2A01 -Power Good
J1-3 — B1E14 +12V
J1-4 — B2E01 -12V

J2-1 — B2A14 Ground
J2-2 — B3A01 -4V
J2-3 — B2E14 +5V
J2-4 — B3E01 Ground

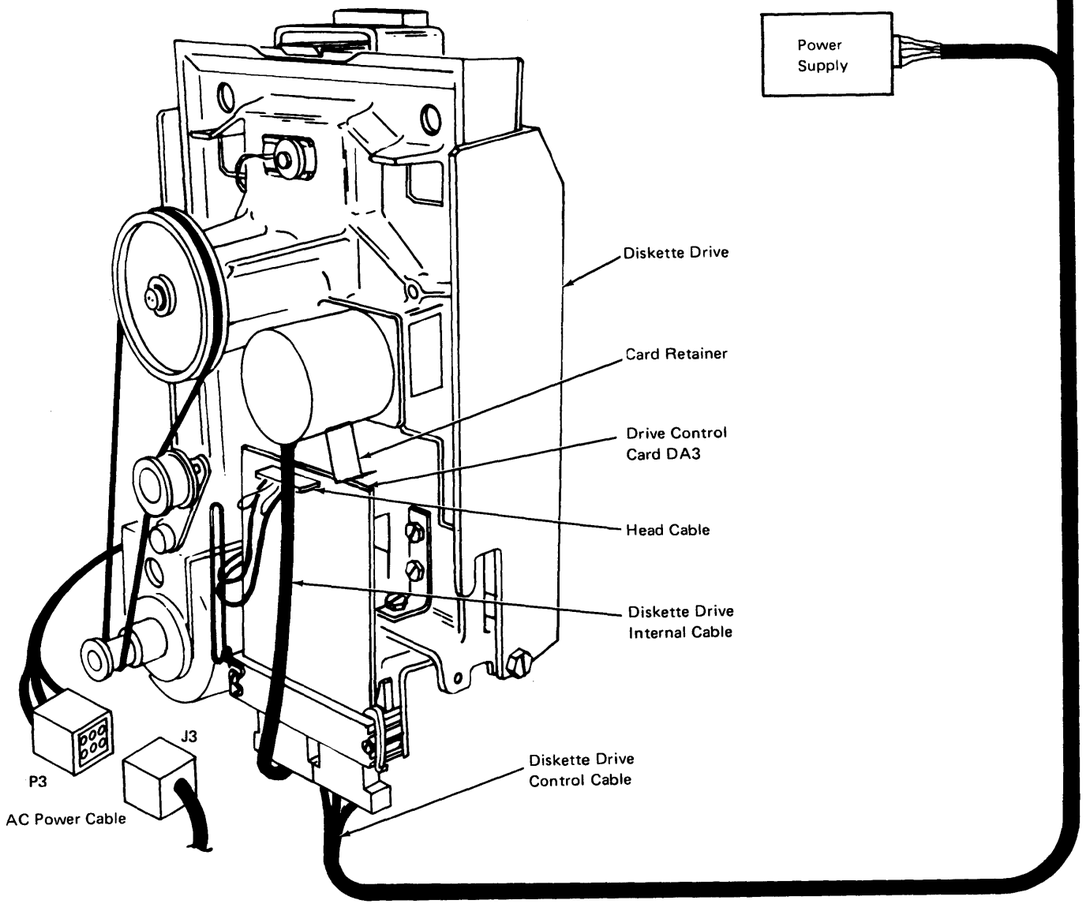
J3-1 — B3A14 Brake Coil 1
J3-2 — B4A01 Brake Coil 2
J3-3 — B3E14 DE Adjust Resistors B
J3-4 — B4E01 DE Adjust Resistors A

J4-1 — B4A14 Ground
J4-2 — B5A01 -4V
J4-3 — B4E14 +5V
J4-4 — B5E01 Ground

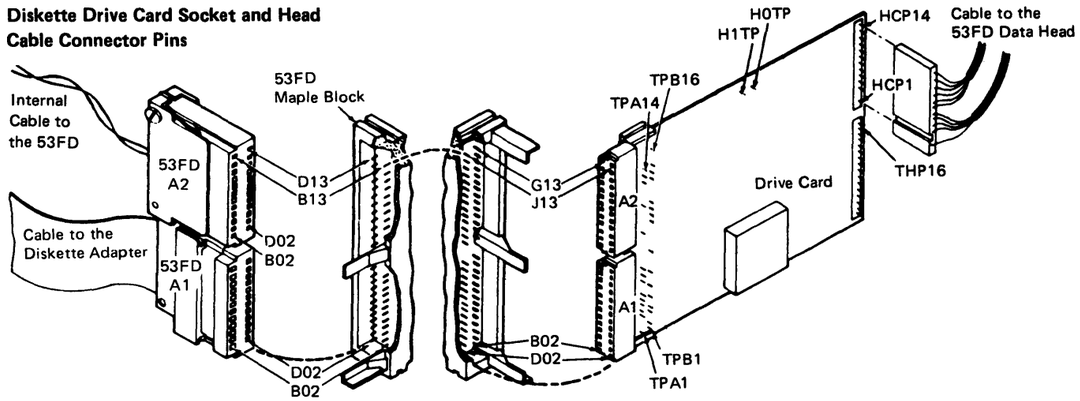
J5-1 — B5A14 Brake Applied to System
J5-2 — B6A01 Brake Coil/24V Brake
J5-3 — B5E14 +24V
J5-4 — B6E01 Ground (+24V)

*PA755 Diskette Signal and Voltage Distribution (01D Gate)*

| Line Name | Power Connections to Diskette Drive (see PA440) | Diskette Drive Control (DA3) Card (01D-A1) | | |
|---|---|---|---|---|
| | | Conn Pin | Card Pin | Test Point |
| Ground | TB1-2 | B08 | D08 | TPA6 |
| +24Vdc | PC1-J2-1 | B10 | D10/J12 | TPA8 |
| +5Vdc | TB1-7 | B03 | D03/J03 | TPB15 |
| -5Vdc | PC1-J2-2 | B11 | D11/J13 | TPA9 |

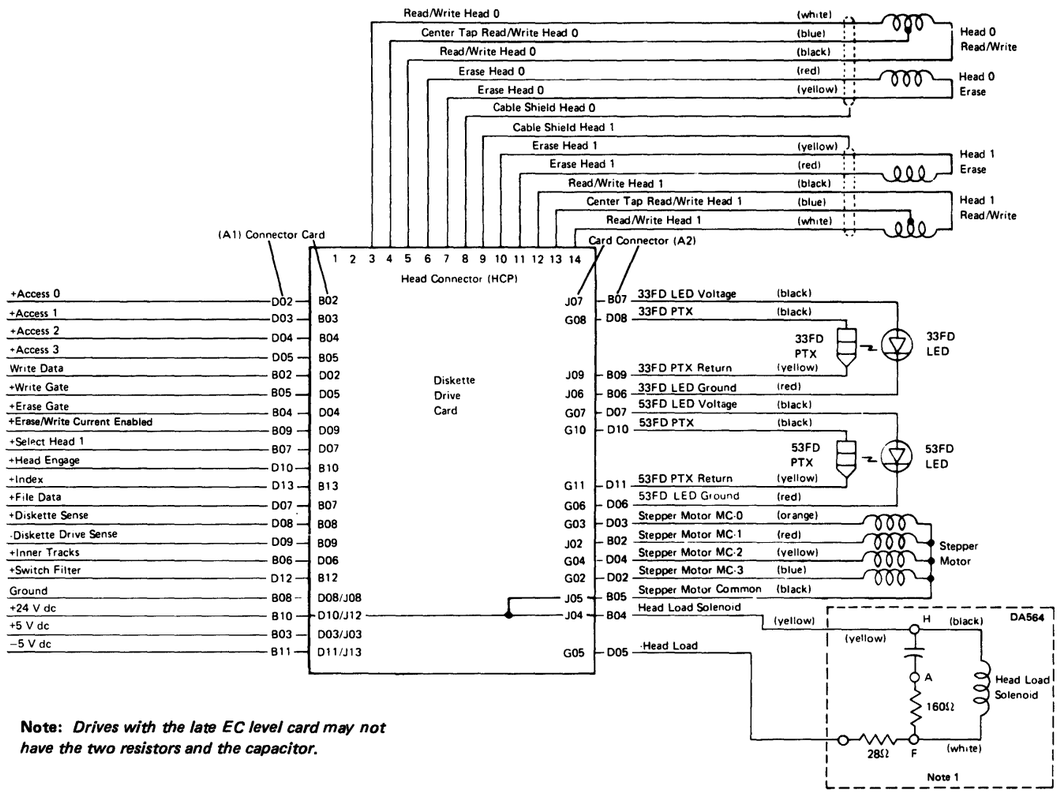



**Diskette Drive Card Socket and Head Cable Connector Pins**



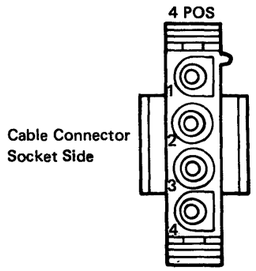

**Note:** ***Maple block causes B and D pin reversal.***

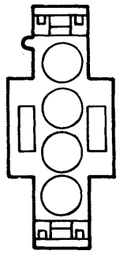
**Diskette Drive Card Logic Pins**

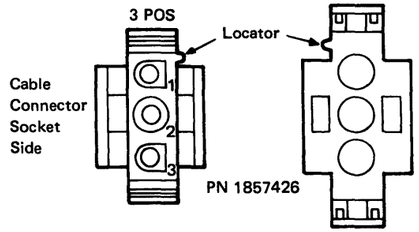


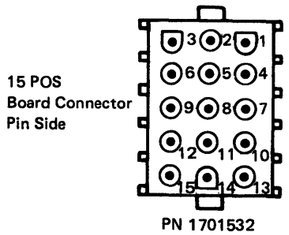

**Note:** ***Drives with the late EC level card may not have the two resistors and the capacitor.***

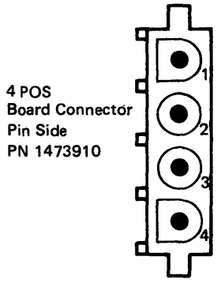
## PA760 Board and Cable Connectors

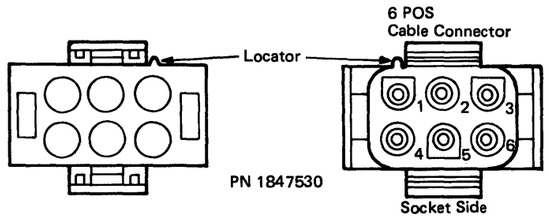


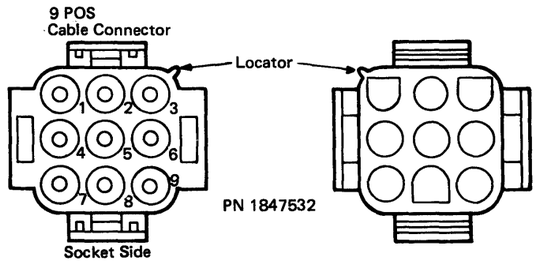



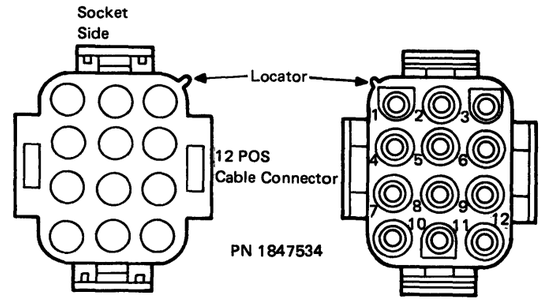



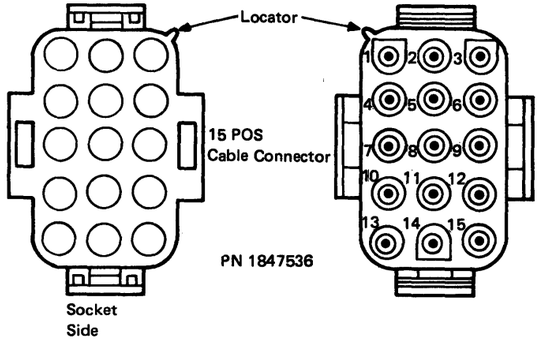



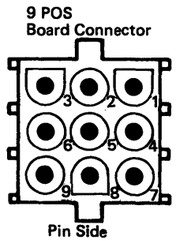



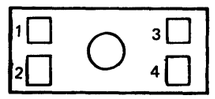



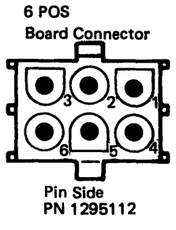



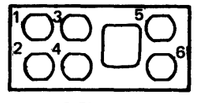




**Caution: The board connectors might not be mounted as shown in these drawings.**

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# Chapter 5. MAP Reference Information
# System Control Facility
# (SC)

## Introduction

This part of Chapter 5 provides maintenance information to service the 8100 system control facility (SCF). When used with the Maintenance Analysis Procedures (MAPs), the SC MAP diagnoses SCF problems and refers you to this part of Chapter 5 for information such as hardware locations, possible causes of failure, and wiring lists.

This part has five sections:

1. General Information (SC100–SC123) — Contains configuration, operation, and repair strategy information.
2. Offline Tests (SC200–SC250) — Contains test information and lists possible causes of failure.
3. Intermittent Failure Repair Strategy (SC300–SC351) — Contains information used to repair intermittent failures.
4. Signal Paths and Detailed Operational Description (SC400–SC464) — Contains diagrams and charts that show wiring and point-to-point signal paths.
5. SCF System Test and Internal I/O Bus Cable Change Procedures (SC500–SC520) — Contains information concerning a system test procedure and how to change SCF internal I/O bus cables.

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## Abbreviations

| | |
|---|---|
| adr | address |
| adwa | adapter work area address |
| ARC | adapter return code |
| BCLE | buffer control list element |
| BOP | basic operator panel |
| BSC | Binary Synchronous Communications |
| BSTAT | basic status register |
| CA | channel address |
| C-CODE | completion code |
| CHIO | channel I/O |
| CNT | count |
| COMPSTAT | completion status |
| CPR | channel pointer register |
| CRP | channel request priority |
| DPCX | Distributed Processing Control Executive |
| DPPX | Distributed Processing Programming Executive |
| DT | device type |
| EFP | expanded function panel |
| EIR | error information register |
| EIRV | error information register vector |
| EN | error number |
| FRB | function request block |
| FRU | field-replaceable unit |
| FRWA | function request work area address |
| hex | hexadecimal |
| I/O | input/output |
| IOEP | I/O interrupt entry point |
| IPL | initial program load |
| LV | level |
| lvl | level |
| MAP | Maintenance Analysis Procedure |
| MD | Maintenance Device |
| PA | physical address |
| PIO | Programmed I/O |
| PSCF | Primary System Control Facility |
| RES | reserved |
| ROS | read-only storage |
| SCA | secondary component address |
| SCF | System Control Facility |
| SDLC | Synchronous Data Link Control |
| SEQ NO | sequence number |
| SS | start/stop |
| SSCF | Secondary System Control Facility |
| SYS-COND | system condition |
| USR | unit status register |
| UT | unit type |

## SC100 General Information

This section illustrates and describes the system control facility (SCF) used in the 8130, 8140, and 8101. It enables you to understand basic operational differences as well as physical differences. It also enables you to understand the SCF addressing scheme, and describes any system-unique repair strategy involved when performing fault isolation.

## SC110 Components and Addressing

The following sections describe and illustrate the 8100 SCF components and locations that relate to the SC MAP, describe the SCF physical addressing scheme, and list the SCF configuration table entry.

### *SC111 Hardware Components*

Figures SC111-1 through SC111-19 show the physical components and locations of the SCF.

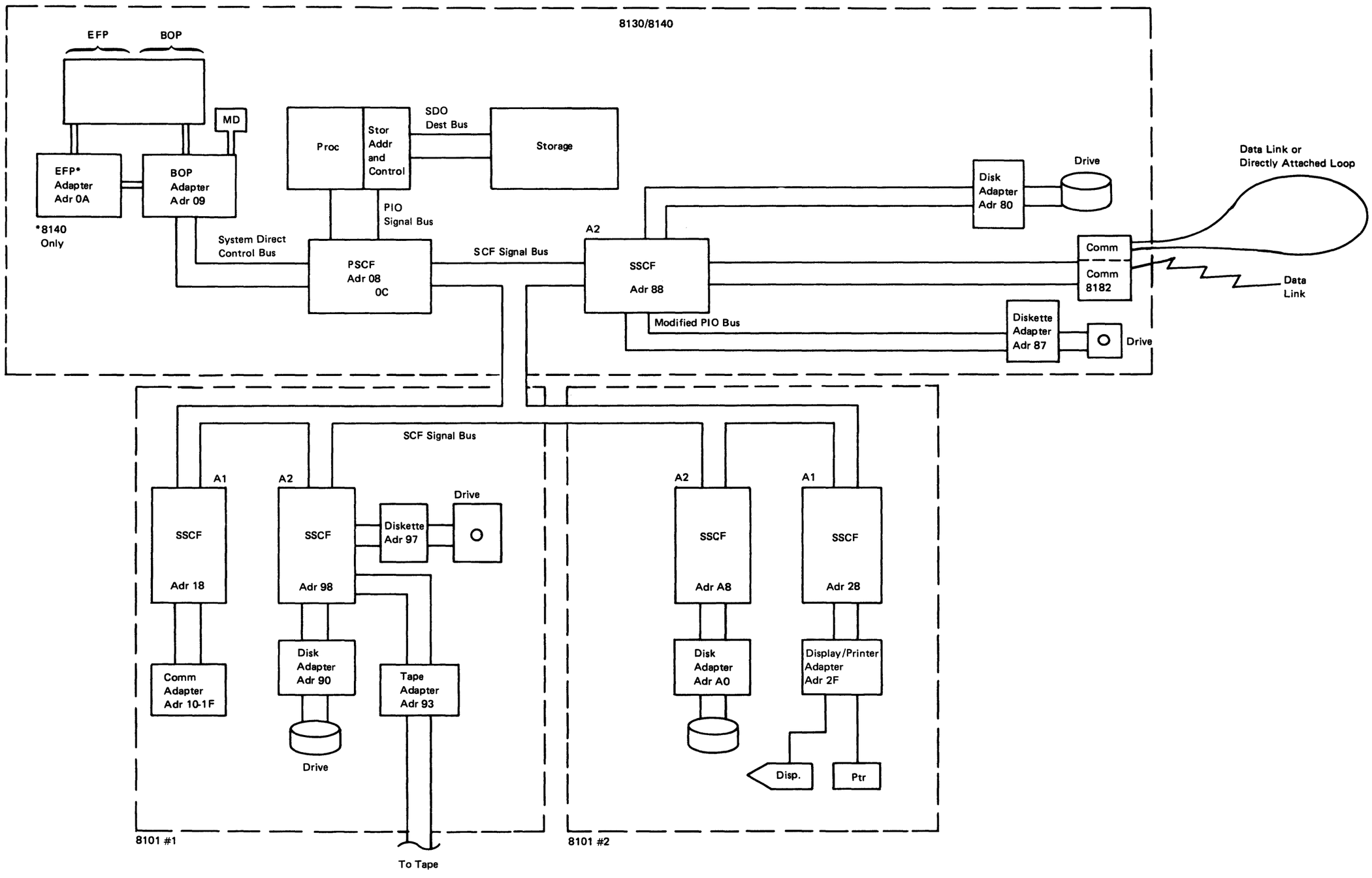



**Figure SC111-1. 8140 Model A and 8130 with System Expansion Feature SCF Basic Data Flow**

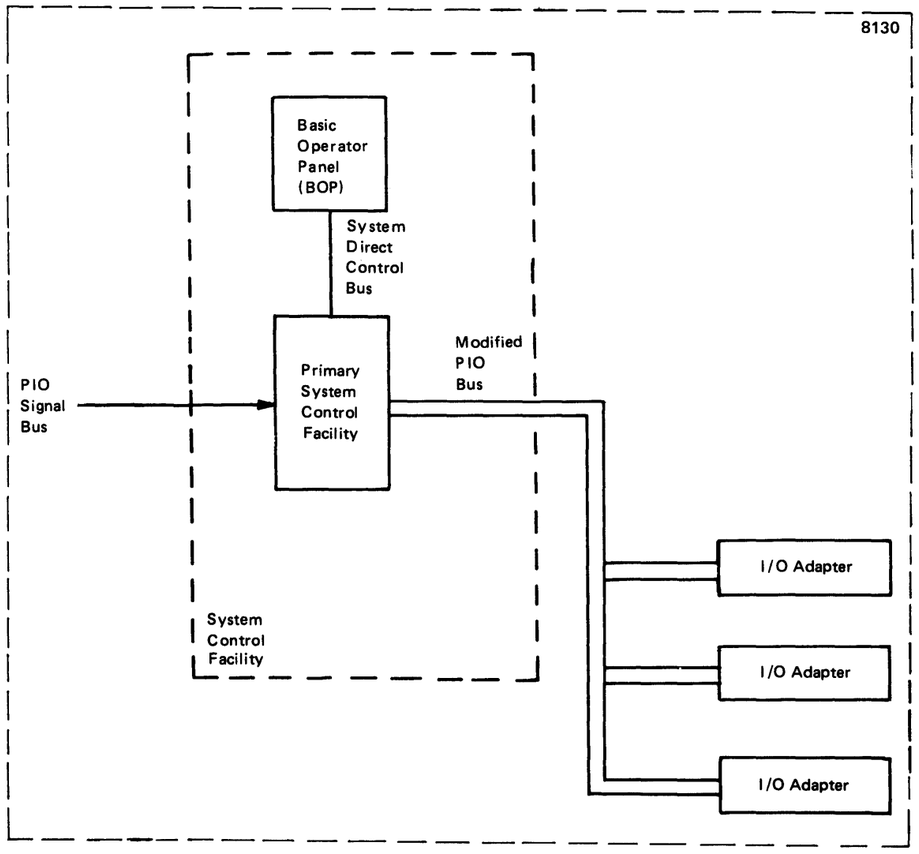


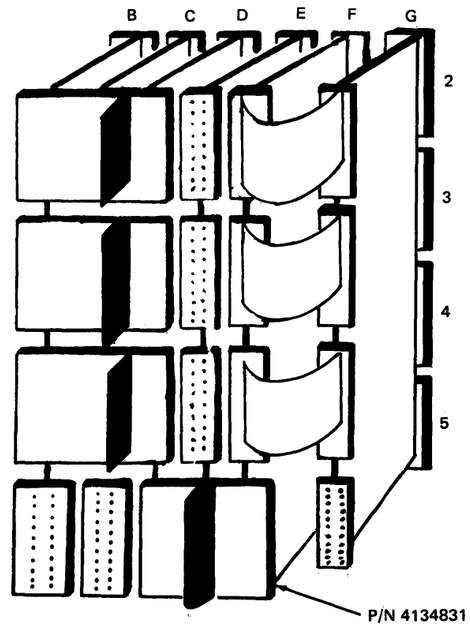

**Figure SC111-2. 8130 without System Expansion Feature SCF Basic Data Flow**

| Card | Location |
|---|---|
| SC1 | A2G2 |
| SC2 | *A2F2 |
| SC3 | *A2E2 |
| SC4 | *A2D2 |
| SC5 | *A2C2 |
| SC6 | *A2B2 |
| SC7 | **A2H2 |

*System Expansion Feature Only.
**Not used with System Expansion Feature.

**A2 Board Positions**

(With System Expansion Feature)

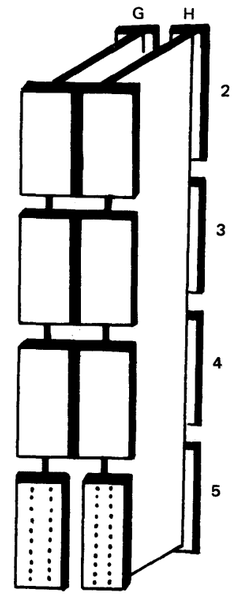



**Caution: In the above figure, the 2, 3, 4, and 5 rows use 3-position top card connectors. You must not swap the 3-position top card connector used on these cards with those used on the processor cards, as the SCF connector does not tie the grounds together and, therefore, is a different part number.**

**Figure SC111-3. 8130 A2 Board SCF Card/Connector Locations**

**A2 Board Positions**

(Without System Expansion Feature)




**Caution: In the above figure, the 2, 3, and 4 rows use 2-position top card connectors.**

**Note:** *Cables connect to the cards in A2F2 and A2G2 by a double male pin connector, PN 5997533.*

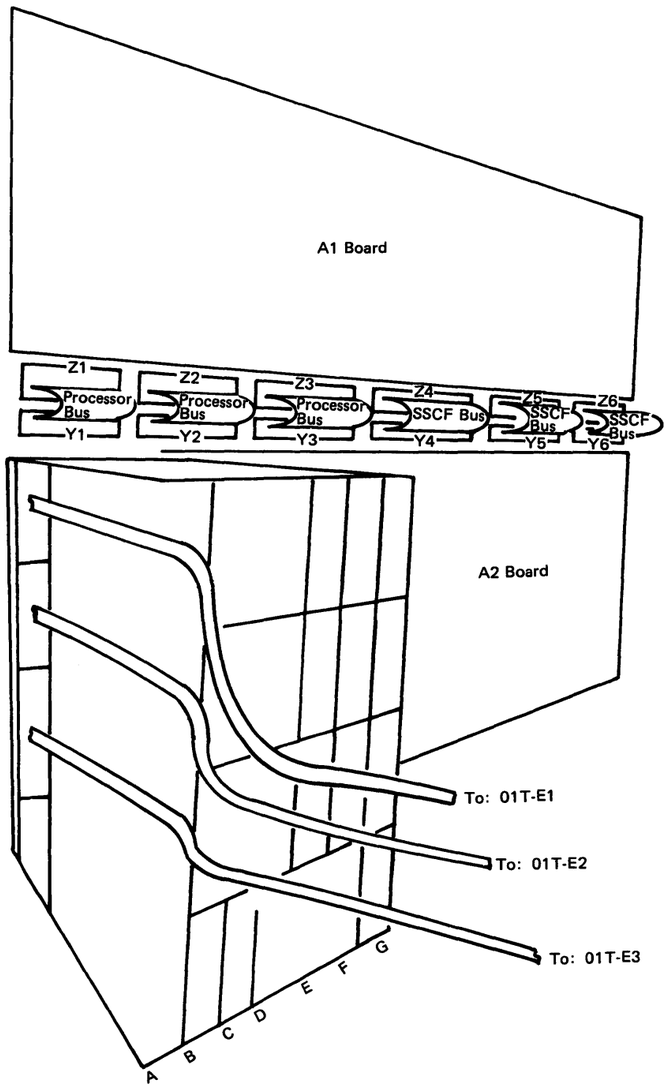



Figure SC111-4. 8130 A1 and A2 Board SCF Cables and Locations (with System Expansion Feature)

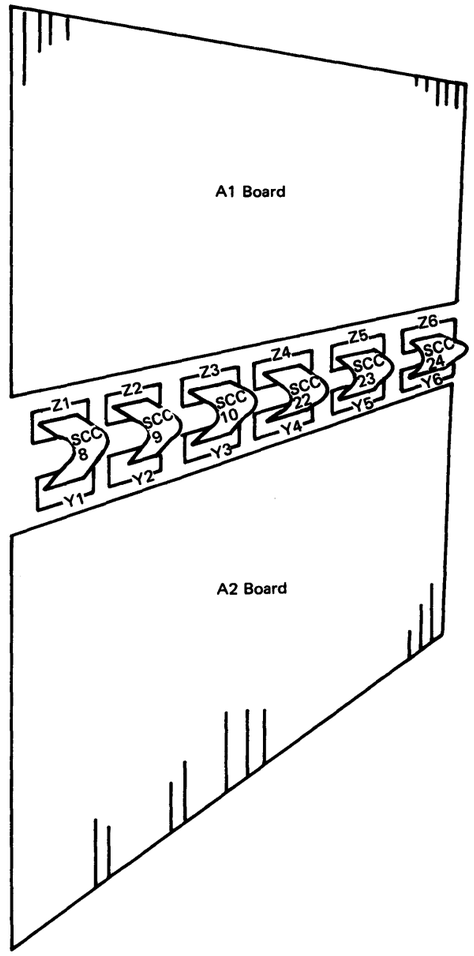



Figure SC111-5. 8130 A1 and A2 Board SCF Cables and Locations (without System Expansion Feature)

**Note:** *Terminators must be present whenever cables are not.*

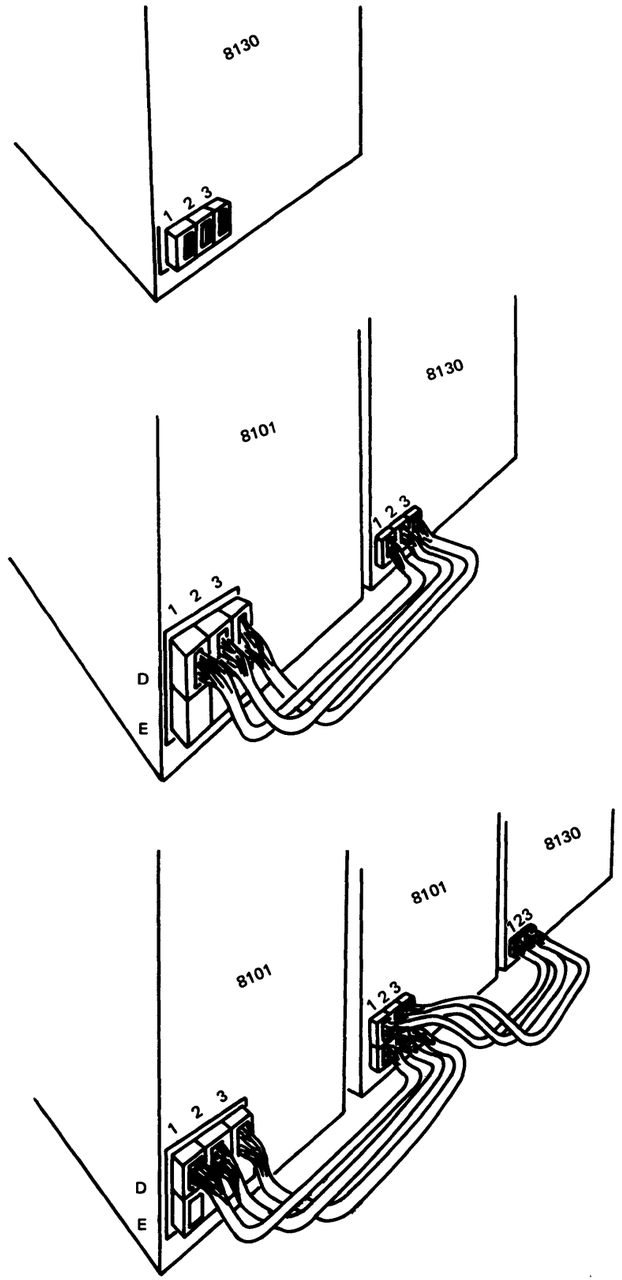
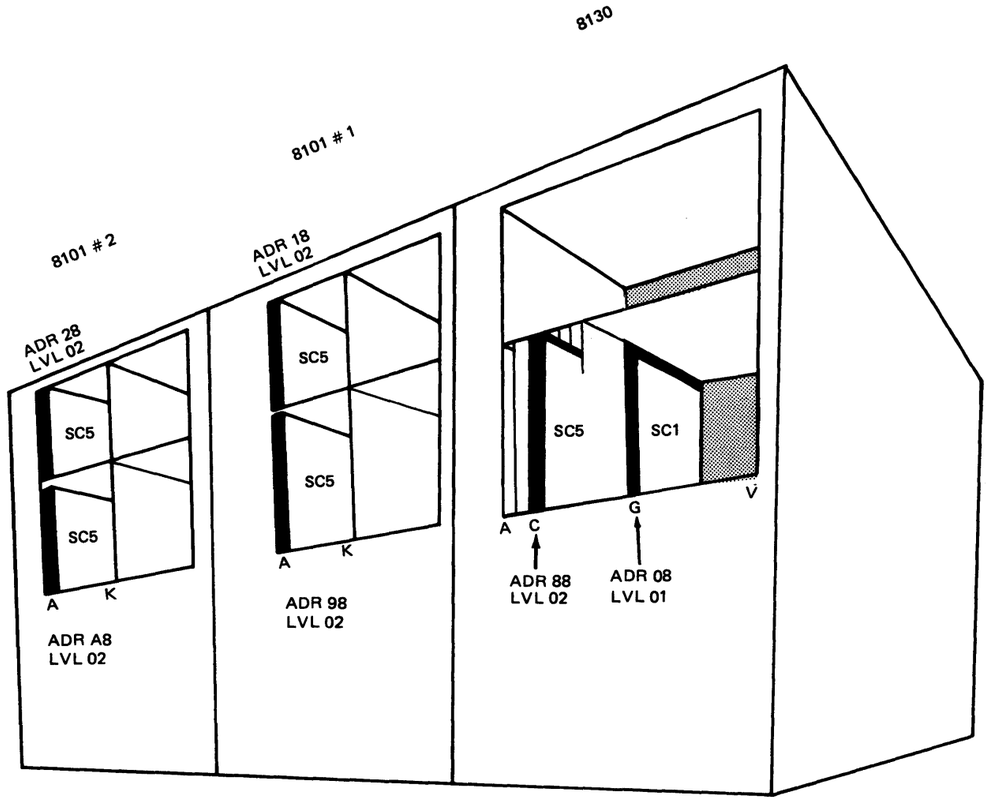


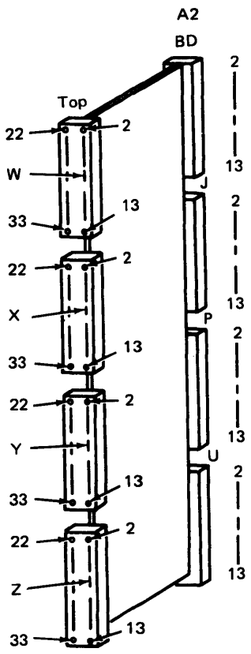

**Figure SC111-6. 8130 External Cable and Terminator Locations**




**Notes:**
1. *Physical locations of first and second 8101s can vary from the above configuration.*
2. *For an 8809 Model 1B, the SSCF address is hex 78 and the level is 02.*

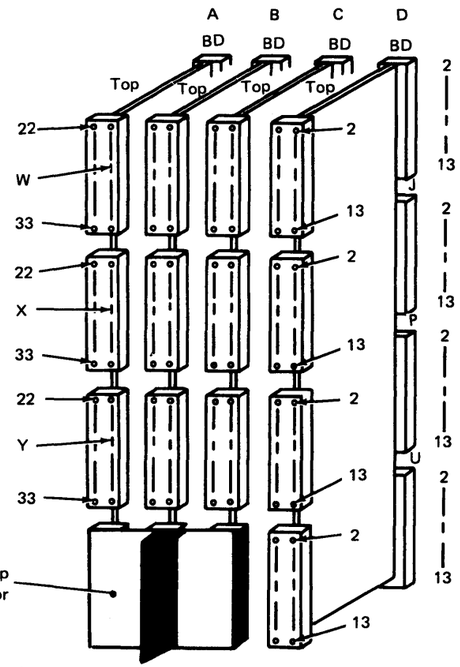
**Figure SC111-7. 8130 SCF Addressing and Card Locations**

A1 Board Position




| Card | Location |
|---|---|
| SC1 | A1A2 |
| SC2 | A2A2 |
| SC3 | A2B2 |
| SC4 | A2C2 |
| SC5 | A2D2 |

A2 Board Positions




**Note:** *Cables connect to the cards in A1A2, A2A2, A2C2, and A2D2 by a double male pin connector, PN 5997533.*

**Caution: You must not swap the 3-position top card connector used on these cards with those used on the processor cards, as the SCF connector ties the grounds together differently and, therefore, is a different part number. See Figure SC111-12 for orientation.**

**Figure SC111-8. 8140 Model A A1 and A2 Board SCF Card/Connector Locations**

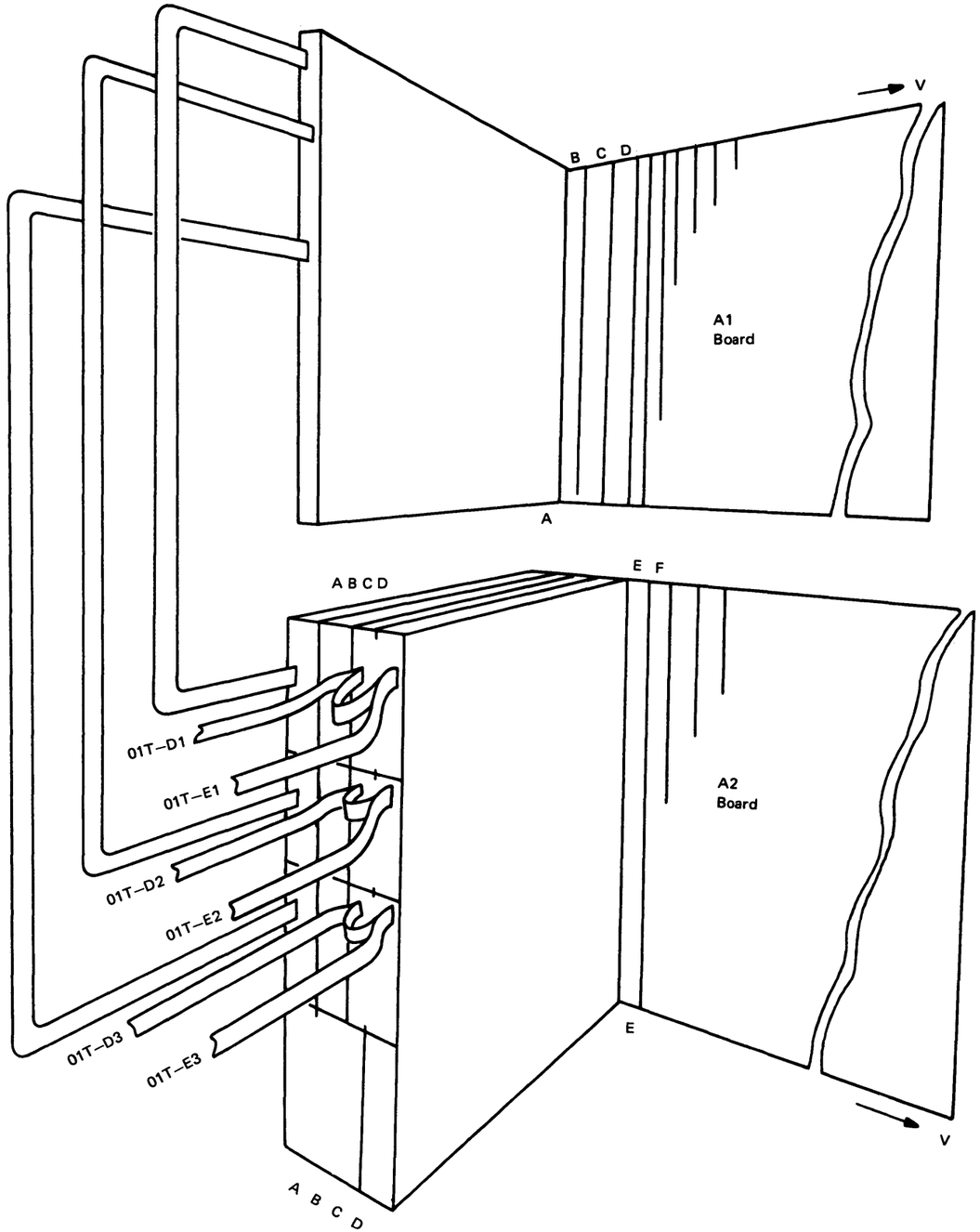
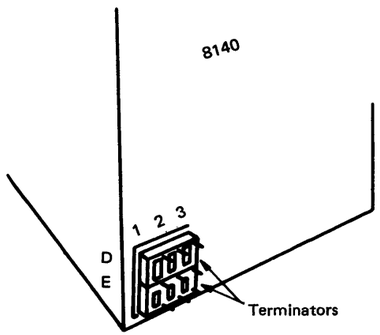
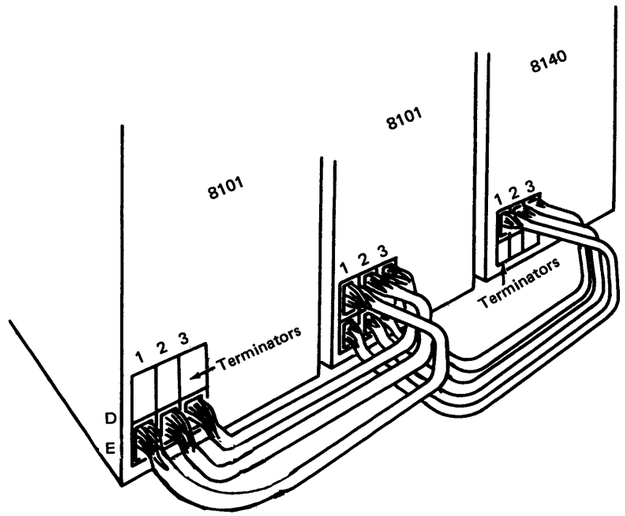
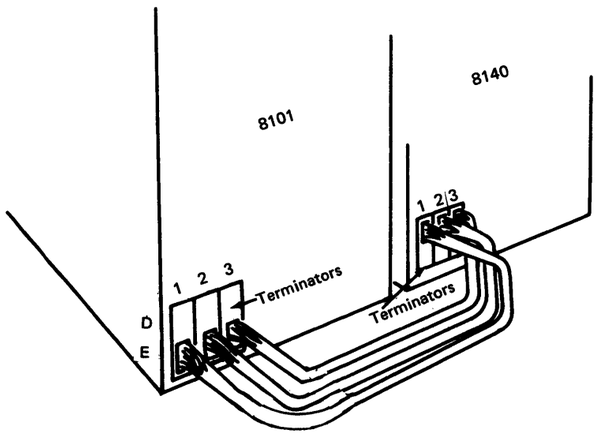



**Figure SC111-9. 8140 Model A A1 and A2 Board SCF Cable Locations**



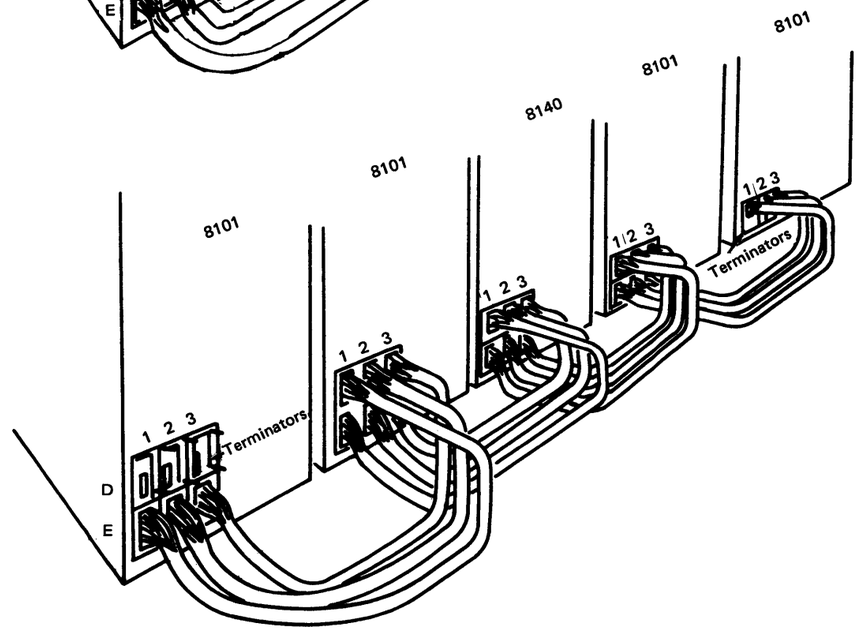




**Figure SC111-10. 8140 External Cable and Terminator Locations**

**Notes:**

1. *Physical locations of 8101s can vary from the configuration shown.*
2. *For an 8809 Model 1B, the SSCF address is hex 78, and the level is 02.*

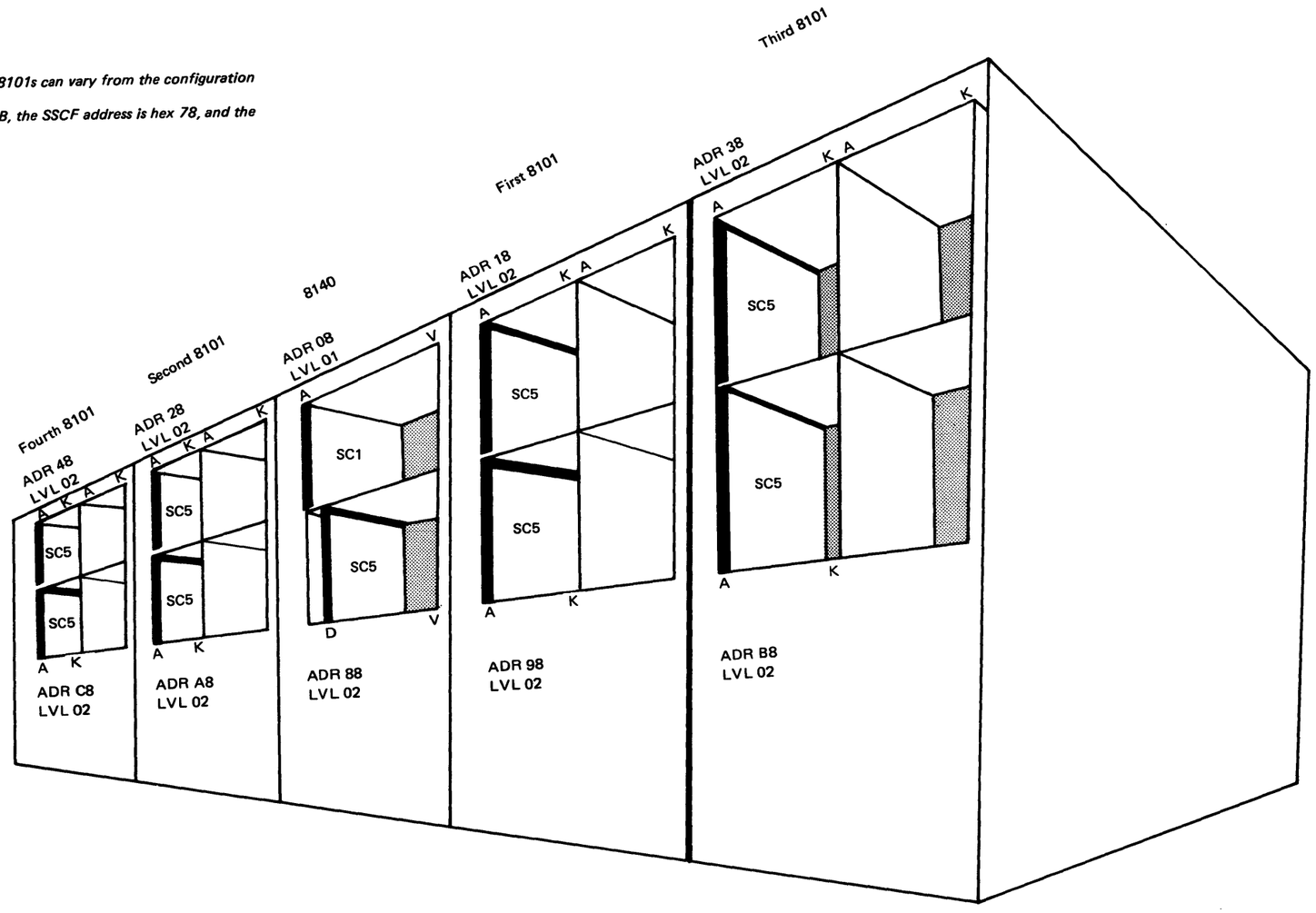
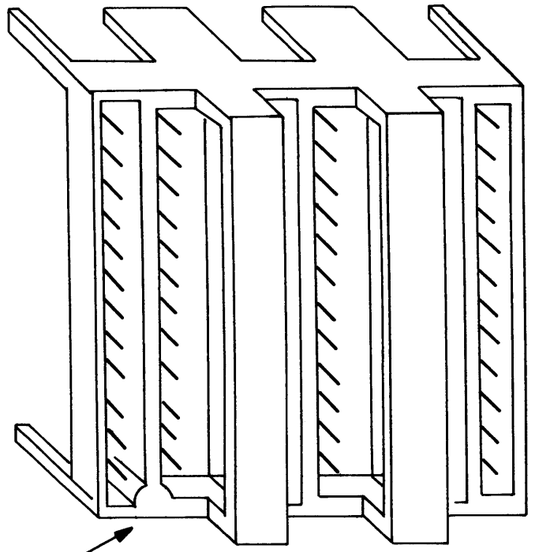



**Figure SC111-11. 8140 Model A/8101 SCF Addressing and Card Locations**



When installing the SCF 3-position top card connector, always keep the extra thickness of material down and to the left.

**Figure SC111-12. 8140 Top Card Connector Orientation**

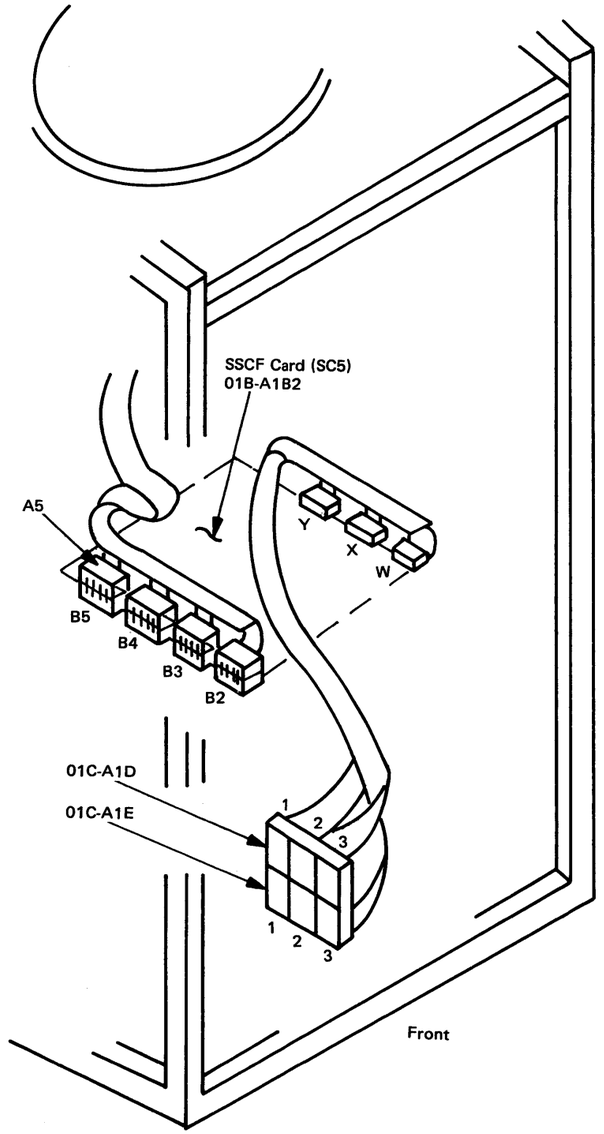



**Figure SC111-13. 8809 Model 1B SSCF Card and Cable Positions**

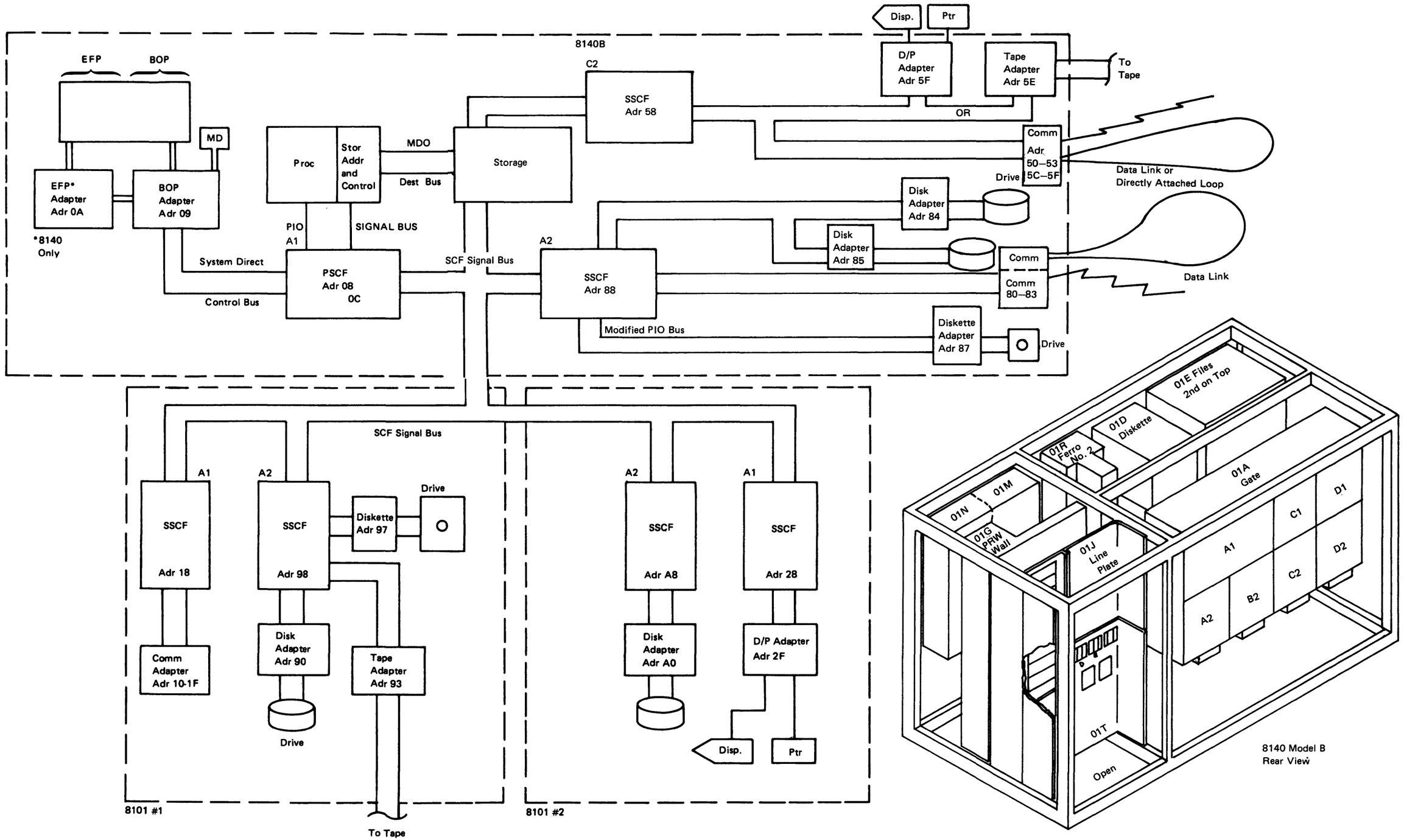



Figure SC111-14. 8140 Model B Basic Data Flow

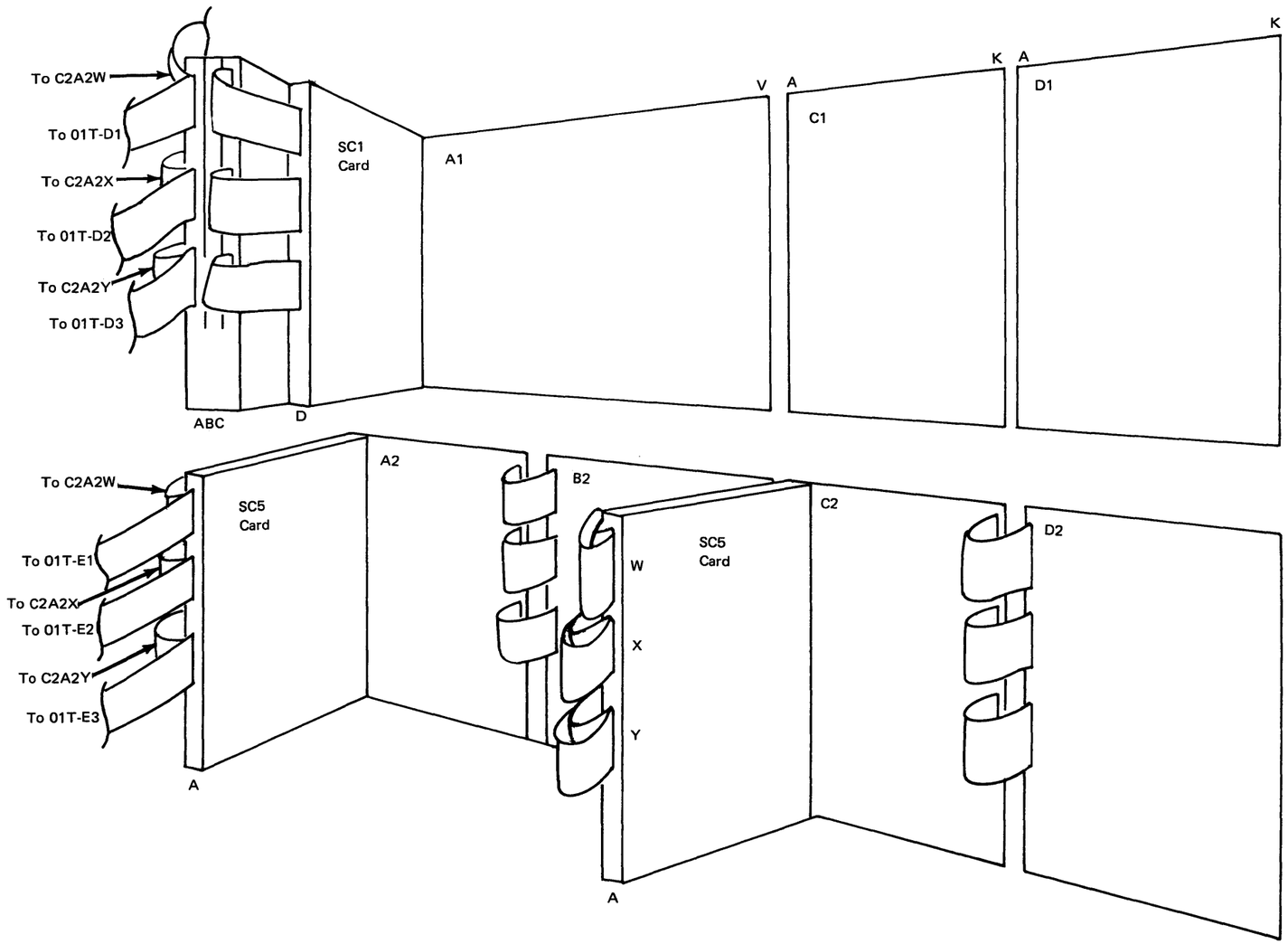
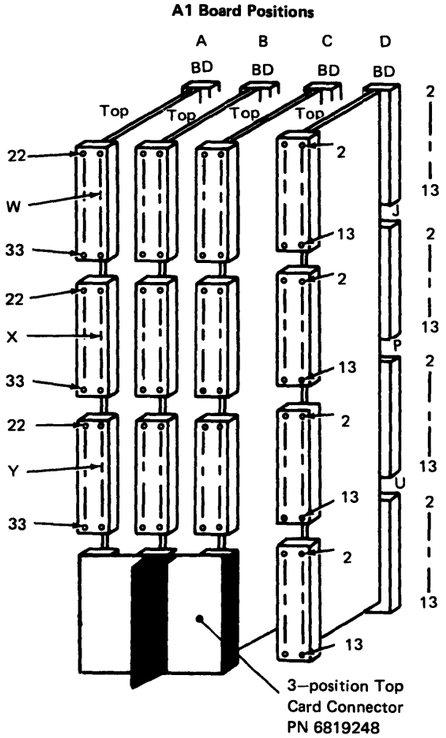
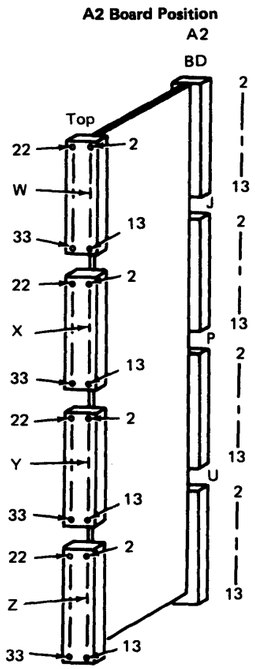
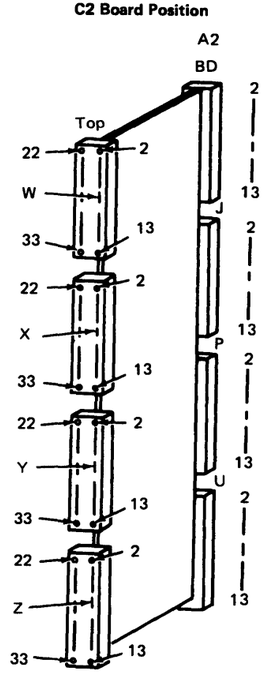



**Figure SC111-15. 8140 Model B Cable Locations**




| Card | Locations |
|---|---|
| SC1 | A1D2 |
| SC2 | A1C2 |
| SC3 | A1B2 |
| SC4 | A1A2 |
| 1ST SC5 | A2A2 |
| 2ND SC5 | C2A2 |

**Caution:** You must not swap the 3-position top card connector used on these cards with those used on the processor cards, as the SCF connector ties the grounds together differently and, therefore, is a different part number. See Figure SC111-12 for orientation.

**Note:** *Cables connect to the cards in A1A2, A1C2, A1D2, A2A2, and C2A2 by a double male pin connector, PN 5997533.*

Figure SC111-16. 8140 Model B Board SCF Card/Connector Locations

**Notes:**

1. *Physical locations of 8101s can vary from the configuration shown.*
2. *For an 8809 Model 1B, the SSCF address is hex 78, and the level is 02.*

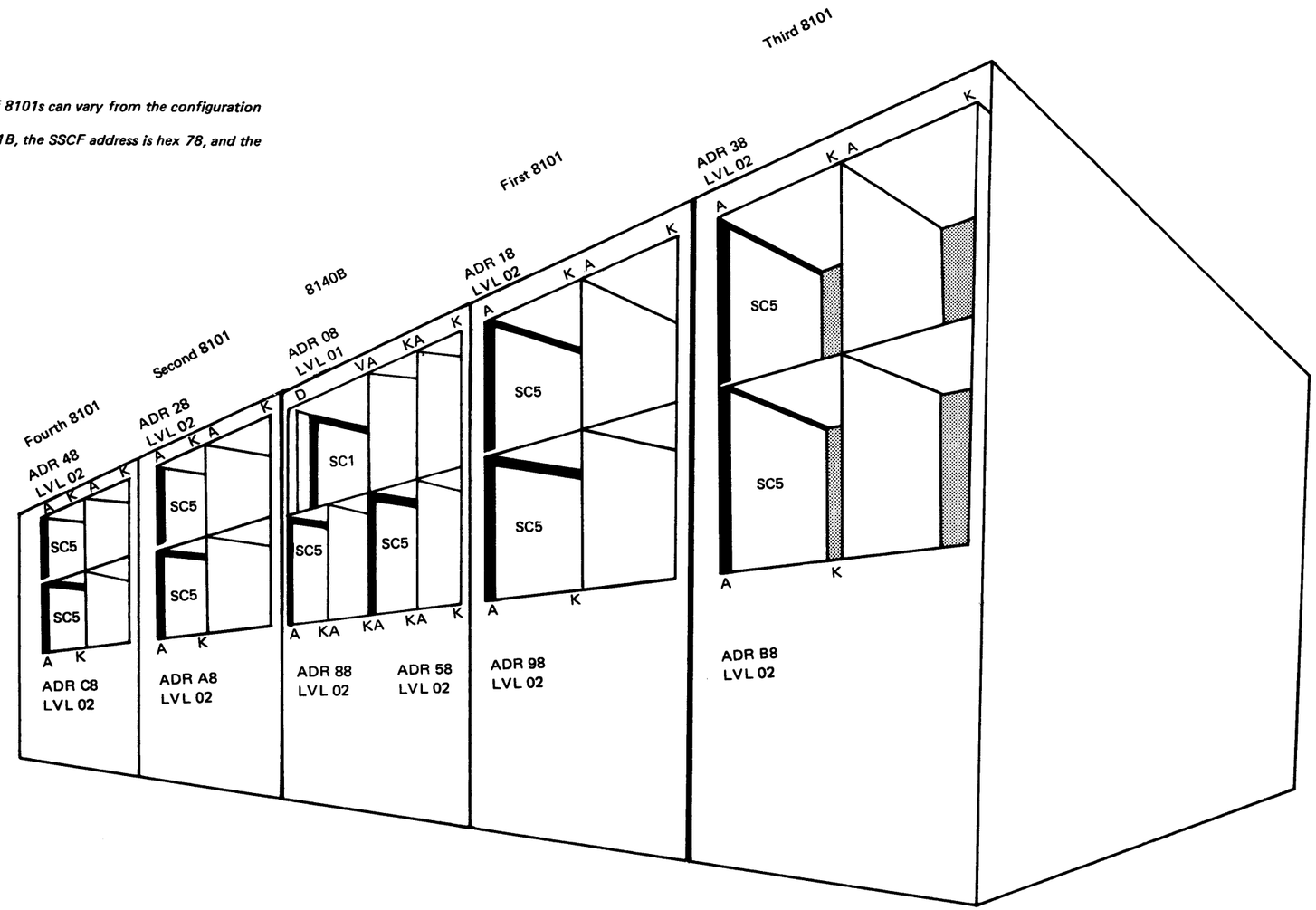
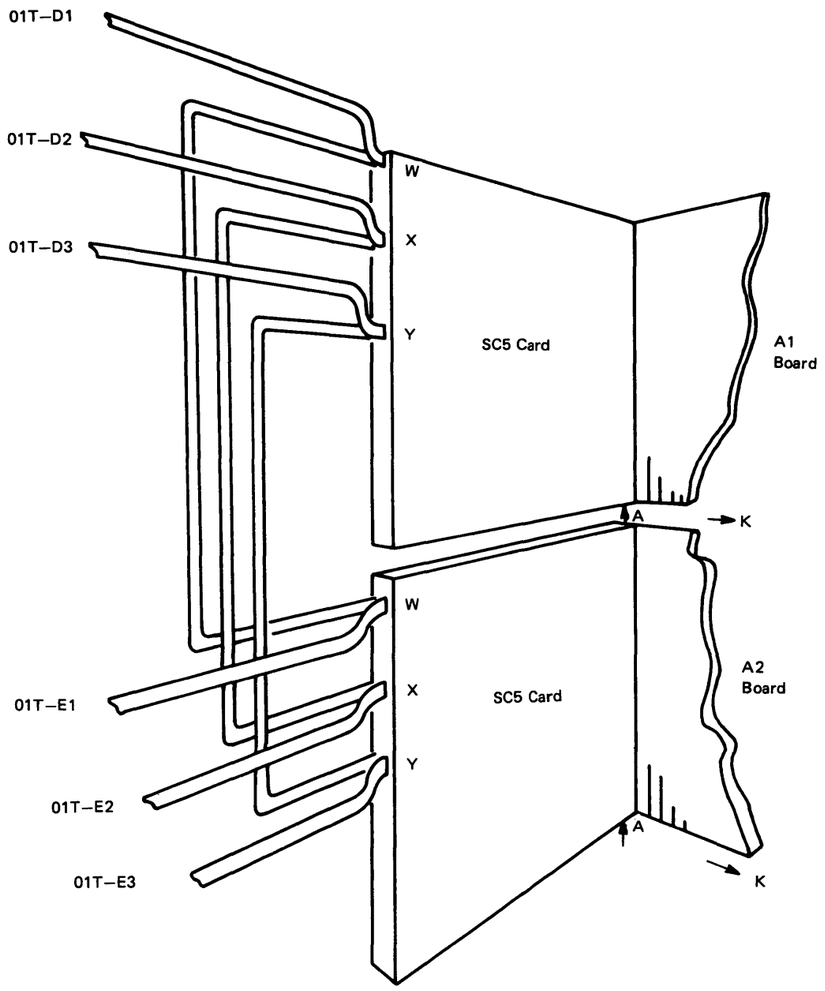


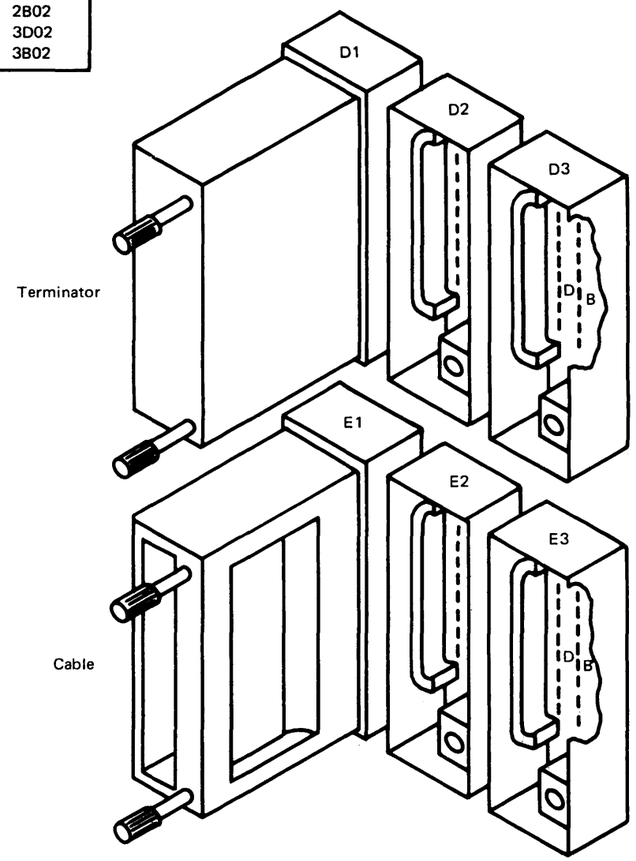

**Figure SC111-17. 8140 Model B SCF Addressing and Card Locations**




**Note:** *Depending on the type and number of adapters in an 8101, there may only be one SC5 card and it can be in either the A1 or A2 board.*

**Figure SC111-18. 8101 A1 and A2 Board SCF Card and Cable Locations**

| SC4/5 Pin No. | D and E Pin No. |
|---|---|
| W02 | 1D02 |
| W22 | 1B02 |
| X02 | 2D02 |
| X22 | 2B02 |
| Y02 | 3D02 |
| Y22 | 3B02 |




**Notes:**
1. *For correct cable and terminator locations according to system configuration, refer to Figures SC111-6 for 8130 and SC111-10 for 8140.*
2. *The 8130 does not have D1, D2, and D3 socket positions in 01T gate.*
3. *In the 8140 BXX the D1, D2, and D3 socket positions are alongside the E1, E2, and E3 positions.*

**Figure SC111-19. 8130/8140/8101 01T Gate D and E Positions Cable, Socket, and Terminator Location and Socket Pin Numbering**

SSCF addressing always requires two entries:

1. The physical address (PA) entry of hex 08, which defines the primary system control facility (PSCF).
2. This entry defines the address of any secondary system control facility (SSCF), which depends on its board location and application. For the 8130, it also depends on whether the System Expansion Feature is installed.

Figure SC112-1 shows the 8100 SCF physical addresses. PSCF address hex 08 is always the first two digits of the PA that specifies the SSCF.

Use Figures SC112-2 and SC112-3 to determine the PSCF and SSCF addresses of any 8130, 8140, or 8101. The address (PA) of the SSCF in an 8809-1B is always 78. See Figure SC111-13 for its location. If the 8140 is a model B, there may be a second SSCF with an address of 58.

| SCF Board Location | Physical Address | Typical Error** |
|---|---|---|
| 8130 A2 board or 8140 A1 or A2 board | 08 | 081E XXXX |
| 8130/8140 A2 board | 0888 | 882E XXXX |
| 8140B C2 board | 0858 | 582E XXXX |
| First 8101 A1 board | 0818 | 182E XXXX |
| First 8101 A2 board | 0898 | 982E XXXX |
| Second 8101 A1 board | 0828 | 282E XXXX |
| Second 8101 A2 board | 08A8 | A82E XXXX |
| Third 8101 A1 board | 0838* | 382E XXXX |
| Third 8101 A2 board | 08B8* | B82E XXXX |
| Fourth 8101 A1 board | 0848* | 482E XXXX |
| Fourth 8101 A2 board | 08C8* | C82E XXXX |
| 8809, Model 1B | 0878 | 782E XXXX |

*8140 only.
**X82E to occasionally X81E for system-type tests

**Figure SC112-1. SCF Physical Addresses**

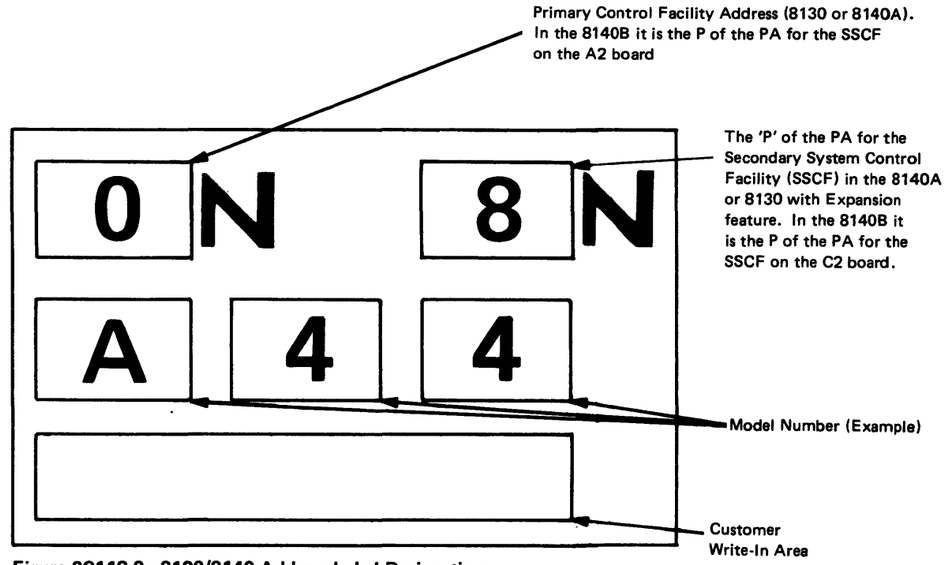



**Figure SC112-2. 8130/8140 Address Label Designations**

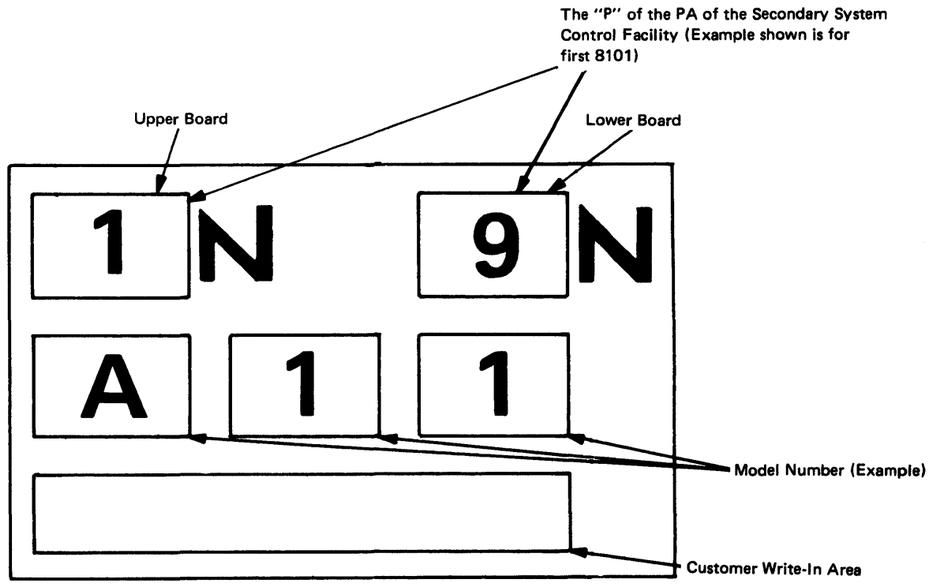



**Figure SC112-3. 8101 Address Label Designations**

*SC113 SCF Configuration Table Entry*

The configuration table defines the SCF address path in the following standard format:

LV PA UTUT OP(1*) OP (2*) OP (3*) OP (4*).

For the SCF, these values are:

PSCF LV = 01
SSCF LV = 02
PA = Board dependent. Refer to Figures SC112-2 and SC112-3.
UTUT = 00F0 (SCF unit type designation)
OP (1) = Channel request priority value (refer to Figure SC113-1.)
OP (2) = 00
OP (3) = 00 for SSCFs
OP (4) = 00 for SSCFs

*These fields are physically represented in the format OPOP OPOP. The numbers in brackets are only used to explain the entry values.

Figure SC113-1 shows the configuration table entries, card locations, physical addresses, unit types, and option field entries for the PSCF and each SSCF. The SSCF (SC5 card) channel request priority switches determine the value of the first option (OP1) parameter. As explained above, the format is shown as two physical addresses: the PSCF value hex 08 (LV01) and the SSCF address (LV02), both of which depend on the machine type and board location. For example, address 0818 specifies that the SSCF is contained in the first 8101 in the A1 board.

| PSCF Location | LV | PA | UTUT | OP(1) | OP(2) | OP(3) | OP(4) |
|---|---|---|---|---|---|---|---|
| 8130 A2 board<br>8140A A1 board | 01 | 08 | 00F0 | 10 | 00 | 43 | 80 |
| 8140B A2 board | 01 | 08 | 00F0 | 10 | 00 | 43 | 84 |

| SSCF Location | LV | PA | UTUT | OP(1) | OP(2) | OP(3) | OP(4) |
|---|---|---|---|---|---|---|---|
| 8130/40 A2 board | 02 | 88 | 00F0 | 54 | 00 | 00 | 00 |
| 8140B C2 board | 02 | 58 | 00F0 | 6C | 00 | 00 | 00 |
| First 8101 A1 board | 02 | 18 | 00F0 | *1C | 00 | 00 | 00 |
| First 8101 A2 board | 02 | 98 | 00F0 | **3C | 00 | 00 | 00 |
| Second 8101 A1 board | 02 | 28 | 00F0 | *14 | 00 | 00 | 00 |
| Second 8101 A2 board | 02 | A8 | 00F0 | **34 | 00 | 00 | 00 |
| ***Third 8101 A1 board | 02 | 38 | 00F0 | *0C | 00 | 00 | 00 |
| ***Third 8101 A2 board | 02 | B8 | 00F0 | **2C | 00 | 00 | 00 |
| ***Fourth 8101 A1 board | 02 | 48 | 00F0 | *04 | 00 | 00 | 00 |
| ***Fourth 8101 A2 board | 02 | C8 | 00F0 | **24 | 00 | 00 | 00 |
| 8809, Model 1B | 02 | 78 | 00F0 | 64 | 00 | 00 | 00 |

*This field becomes 74 if the board contains the display and printer adapter. If an 8140 Model BXX has a display/printer adapter in the C2 board (OP1 field 6C) or in an 8101 A1 board (OP1 field 74), this is the second display/printer adapter and has an OP1 field of 7C.

**This field becomes 5C if the board contains the Magnetic Tape Feature, becomes 4C if the board contains the Diskette Storage Feature without the Magnetic Tape Feature, and becomes 04 if the board contains only an SSCF card.

***8140 only.

**Note:** *Use the Machine Configuration List, stapled to the Machine Level Control (MLC) history sheets for this unit to help determine the correct values for the OP(1) field of the above table.*

**Figure SC113-1. SCF Configuration Table Entries and Card Locations**

## SC120 SCF Basic Operational Description

The functions provided by the 8130 without the System Expansion Feature are identical to those provided by the 8140 primary system control facility (PSCF) SC1 card. Effectively, the SC1 card permits information transfer within the 8130/8140 Processors. The functions provided by the 8130 with the System Expansion Feature are identical to those provided by the 8140 system control facility (SCF). These functions permit information transfer and provide interrupt and SSCF addressing control for devices attached externally to either the 8130 or 8140.

**Note:** *For purposes of discussion in this section, the terms "PSCF" and "SSCF" are used. "PSCF" refers to those functions performed by the SC1 card, while "SSCF" refers to those functions performed by the SC5 card. The SC2, SC3, and SC4 cards become part of the PSCF when there is an SC5 card in the system, while the SC6 card, used only in the 8130 with the System Expansion Feature, functions as a signal line terminator.*

For physical differences, see section SC110; for functional differences, refer to the detailed data flow contained in section SC450.

### *SC121 PSCF Basic Functions*

The following lists the functions provided by the PSCF and briefly describes what these functions perform:

- Power sequence – Controls power sequencing for the 8100.
- Operator panel and channel operations – Controls data transfer of the basic and expanded (8140 only, if installed) operator panels, and the logic necessary for processor-to-channel information transfer.
- Clocked interrupt – Provides a 100-ms timer used for processor program operation.
- Programmed IPL parameters – Provides a register used for program mode IPL operations.
- IPL switch parameters – Provides switches that determine primary mode IPL parameters.
- BOP and PSCF priority level assignments – Permits the program to alter the PSCF and BOP fixed hardware interrupt level from 3 to 0.
- Error detection – Enables parity error detection for the PSCF, as well as the BOP and EFP (if installed).
- KDO instruction decode for PSCF operations – Decodes certain types of KDO instructions to permit execution of specific SCF control functions.
- Reset control – Executes PSCF/SSCF and I/O group resets.
- Programmed SCF control – Uses the SSCF status register to control certain SCF functions under program control.

### *SC122 SSCF Basic Functions*

The following lists and basically describes the functions provided by the SSCF:

- I/O group address – Provides switches whose fixed assignment determine the first four bits of the PIO physical address used to specify the device.
- Channel request priority – Provides switches whose fixed assignments determine interrupt priority for channel I/O operations.
- Release request for BSC operations – Permits BSC operations to override channel I/O operations so that no BSC data overrun conditions occur.
- Interrupt translation array – Permits programmable interrupt level and sublevel assignments for all except the PSCF, SSCF, BOP, and EFP.

### *SC123 PSCF and SSCF Combined Basic Functions*

The following lists those SCF functions provided by combining PSCF and SSCF hardware:

- Wraps the SCF signal bus to check correct bus operation.
- Permits devices attached to any SSCF to present I/O interrupts.
- Determines SSCF addressing.

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## SC200 Offline Tests

The system control facility (SCF) can only be tested and repaired in offline mode with the system dedicated to fault isolation. These tests verify PSCF operation, and then verify operation of the PSCF with one of its SSCFs, if installed.

The tests are contained on MD diskette 01, and check SCF functions to isolate failures to the FRU or FRUs most likely defective. You invoke these tests only from the MD by using either the SC MAP for MAP interaction, or the Free-Lance Utility in which no MAP interaction occurs.

When using the MAP, the tests are automatically invoked and you are prompted by the MD display to perform test procedures. Refer to SC313 for procedures relating to free-lance operation.

## SC210 Offline Test Routine Descriptions

The SCF tests may be described by grouping them logically by overall function, as follows:

**Note:** *During Initialization there is a Configuration Table verification. These tests are always performed.*

**Group 1 —** PSCF Test, routine numbers less than 30. These routines test the SC1 card, and the basic functions of the SC2, SC3, and SC4 cards, when they are present. The routines can be invoked by entering '08B' at 80BC and 'B' at 81BC.

**Group 2 —** SSCF Tests, routines 30 through 89. These routines test the SC2, 3, 4, and 5 cards. They are run in addition to Group 1 on a single SSCF address when invoked by entering '08X8B' at 80BC and '1B' at 81BC. It should be noted that these tests include the use and testing of common adapter functions.

**Group 3 —** SCF System Tests. These tests assuume that all the individual adapter tests have been run successfully. These tests make use of the entire system (this includes all adapters, SSCFs and configuration table). Testing includes some multi-adapter operations. These tests are invoked by entering '69C' at 80BC and 'B' at 81BC. See SC510 for System Test operating procedures.

**Note:** *Routines 2C and 2D are the system routines for an 8130 system without the expansion feature. These routines must be invoked separately.*

### *SC211 PSCF Routine Descriptions*

**Routine 01, Reset Error Information Register (EIR) Test.** This test first performs a Reset Adapter command and issues Read PIO commands to the 16-bit PSCF EIR. It then compares the data read to the data expected.

**Routine 02, Set Error Information Register (EIR) Test.** Individually tests each bit of the PSCF EIR. All bits not used are masked before beginning the test. Starting with bit 0 and ending with bit 15, this routine individually places bits in the EIR, and then issues a Read command to verify the data.

**Routine 03, Reset Error Information Register (EIR) Data Test.** Places 1-bits in the EIR and issues a PIO reset command with a mask having only one bit on. It then reads the EIR to ensure that only the proper bit was reset. Bits 14 and 15 are not used, therefore no interrupts are expected.

**Routine 04, Reset Error Information Register Single Bit Data Test.** Places a single bit in the EIR and then issues a reset command with the same bit masked. The register should then be reset with only the forced bits on.

**Routine 05, Reset PSCF Basic Status Register (BSTAT) Test.** This test first performs a Reset Adapter command and issues Read PIO commands to the 16-bit PSCF BSTAT. It then compares the data read to the data expected.

**Routine 06, Set PSCF Basic Status Register (BSTAT) Test.** Individually tests each bit of the PSCF BSTAT. All bits not used are masked before beginning the test. Starting with bit 0 and ending with bit 15, this routine individually places bits in the BSTAT and then issues a Read command to verify the data.

**Routine 07, Reset PSCF Basic Status Register (BSTAT) Data Test.** Places 1-bits in the BSTAT and issues a PIO reset command with a mask having only one bit on. It then reads the BSTAT to ensure that only the proper bit was reset. The routine operates on level zero so that interrupt processing does not occur.

**Routine 08, Reset PSCF Basic Status Register Single Bit Data Test.** Places a single bit in the PSCF BSTAT and then issues a reset command with the same bit masked. The register should then be reset with only the forced bits on.

**Routine 09, Reset PSCF BSTAT Bit 3 (Power On Reset) Test.** Hardware turns on PSCF BSTAT bit 3 after a power-on reset, and the Reset Adapter command should not turn this bit off. This routine sets the bit, issues a Reset Adapter command, and ensures that the bit was not reset.

**Routine 0F, SCF Interrupt Request Test.** The SCF should present interrupt requests if bits 14 and 15 of the PSCF BSTAT are on. This routine sets PSCF BSTAT bits 14 and 15, using processing level zero. The IOIRV is then read to see that the proper I/O interrupt request is active. Both level 0 and N requests are tested.

**Routine 10, Timer Check Test.** Bit 8 of the PSCF EIR (timer check) should set when a timeout condition occurs (bit 8 of the PSCF BSTAT on). This routine sets bit 8 of the PSCF BSTAT, then enables the timer (PSCF BSTAT bit 9), which causes an immediate timer interrupt. PSCF EIR bit 8 (timer check) should be set.

**Routine 11, Timer Accuracy Test.** Tests the accuracy of the SCF timer logic that generates the 100-ms clocked interrupt. The routine first enables the timer, and, after the first active interrupt, enters a loop that counts 10 interrupts. The time used to complete this loop is then compared to the high and low tolerances, and, if within limits, the test completes successfully. The timer speed is based on the input AC line frequency. The limits are based on a variation of ± ½ cycle from the norm (50/60 cycle).

**Routine 12, PSCF Basic Status Register Invalid Operation Test.** The PSCF decodes all PSCF adapter commands. This routine issues all invalid commands to PSCF address 08 and then checks for a system check condition.

**Routine 13, PSCF Error Information Register Invalid Operation Test.** Issues all invalid commands to PSCF address 0C and then checks for a system-check condition.

**Routine 14, Byte Tag Test.** Checks that correct data transfer occurs between the PSCF and the processor for byte I/O commands.

**Routine 15, KDO Enable Test.** The I/O Power Drop command should not drop power if an improper sequence has occurred.

**Routine 17, PSCF BSTAT Interrupt Test.** Causes an interrupt request in PSCF BSTAT, then enables the adapter to ensure that an interrupt occurs. This test is done on level 7. Dynamic level switching to hardware level N is tested.

**Routine 18, PSCF BSTAT Interrupt Level Switching Test.** A stream of I/O instructions are used to set and reset active interrupt conditions. The processor should handle this maximum interrupt rate test.

This routine causes PSCF BSTAT interrupt requests by issuing I/O halfword commands to the BSTAT, which turns on bits 14 and 15. It then immediately issues another I/O halfword command that resets bit 14 to disable the interrupt. Many interrupts occur but the results are predictable. If the bits set and reset correctly, the proper level swaps have occurred.

**Routine 19, Read PSCF Programmed IPL Register Test.** The PSCF programmed two-byte IPL register is set and reset under program control. Before beginning, the routine reads the register. It then tests each bit by setting the bit (resetting the adapter) and then reading the register bit value. If successful, the register contents saved at the beginning of the routine are returned to the register.

**Routine 1A, BOP Primary Interrupt Level Test.** The BOP adapter is wired to present its interrupt requests on the same level as the SCF. This routine forces a BOP interrupt request, and then reads the IOIRV to ensure that the proper bit was set for the interrupt.

**Routine 1B, Read IPL Switch Register Test.** The 16 switches on the PSCF (SC1) card are contained in two 8-switch modules. This routine reads the PSCF IPL switches to ensure that the value is equal to the factory setting (as in the Configuration Table). The IPL switch settings are also checked for validity.

**Routine 1C, Condition Value Test.** The SCF should set the correct condition value into the processor after executing each I/O instruction. This routine tests that the correct condition value is set. A test is also made to insure that the condition value is not changed if the I/O instruction does not complete successfully (machine check).

**Routine 1D, Wait Test.** This routine tests the ability of the processor to enter the wait state and then, after an interval (signaled by an I/O interrupt), to continue processing on the same level. This is done by activating the SCF 100-ms timer. After the first interrupt, the interrupt is cleared and the SCF is enabled. The level is PIRR'D off. The system should remain in the wait state until the interrupt is fielded.

**Routine 20, I/O (Read) Bus "Parity Valid" Signal Test.** With the data tag active, the adapter activates the "parity valid" line to signal the processor that data parity should be checked. This routine uses the KDO instruction to force data bits 2 and 10 on, which should cause invalid parity. A system check should then occur with the EIRV indicating invalid parity.

**Routine 21, I/O (Read) Bus Parity Bit (KDO '0110'B) Test.** The adapter should raise the P-valid line during 'TD' time so that the processor will check the parity on the data. In this test the KDO instruction is used to force the data parity bits on, thereby causing bad parity. A machine check should occur with the EIRV indicating invalid parity.

**Routine 22, PSCF Parity Read Test.** The PSCF should detect bad parity on the I/O bus at TD time when data is being transferred to the processor from one of the system devices. The BOP is used to send bad parity data through the PSCF. If the "SDCI bus select" line is active (the device did not detect bad parity), the bad parity data causes a read check and a machine check in the PSCF. The "valid" signal is also suppressed, which causes an I/O timeout, setting the machine check bit in BOP basic status. After the test is completed, the BOP is re-initialized. If this fails, a BOP error is indicated, either a hot interrupt or an I/O Interface Check (panel indicator).

**Routine 23, PSCF I/O Parity Write Test.** The PSCF should detect bad outbound parity on the I/O bus. The KDO instruction forces data bits 2 and 10 on, which causes invalid parity. A system check should then occur with the EIRV indicating a timeout condition, and PSCF EIR bit 9 should be on (I/O Write check). When bad parity is detected by the processor, the halt signal should set the MCK bit in the selected adapter BSTAT.

**Routine 24, I/O Read B0/B1 Data Check Halt Test.** The marker force bit 2/10 command forces invalid parity. The EIRV I/O parity bit should also be on. The routine tests each byte separately.

**Routine 25, Marker Reset Function Test.** Uses the force 2/10 data command to test that the marker function is reset after the first I/O command. The routine first enables the marker function and then issues an I/O read data command to ensure odd parity. This is immediately followed by a command that should normally produce a system check. If marker function is properly reset, no system check should occur. If ECC is present, a storage test for bad parity is done via KDO commands.

**Routine 26, Read Secondary Level Command Test.** (Only run if Expansion feature is installed.) Adapters on the same primary level should be assigned to different secondary levels. When presenting interrupts, each adapter ORs its secondary bit to the bus in response to the Read Secondary Level command. This routine issues the Read Secondary Level command to each of the eight primary levels and then tests the returned data for no bits active (no adapters were presenting interrupts). A test is made to insure that the Expansion feature (bit 6 of EIRV) agrees with configuration type. This is the first test of the SC2, SC3, and SC4 Expansion feature cards.

**Routine 27, Unselected Unit Test.** (Only run if Expansion feature is installed.) When I/O units are not logically connected to the system, the I/O bus should be disabled. This routine attempts to read unit status in the reset condition. No data or response should occur, and the processor should report an I/O timeout.

**Routine 28, Unit Not Connected Broadcast Read Command Test.** (Only run if Expansion feature is installed.) SSCF status can be determined by using three commands: (1) Read USR bit 0, (2) Read USR bits 1 and 2, and (3) Read USR bit 3. This routine issues each command and then checks to see that all SSCFs have no status pending.

**Routine 29, Unit Not Connected Data Wrap Path Test.** (Only run if Expansion feature is installed.) The SCF can wrap a byte of data from the PSCF wrap register to the processor through the BO bus. This routine issues the Wrap (CRP) command without any I/O unit connected to test the path from the wrap register to the processor only. The test checks for bit 7 on, then bit 6, etc, then for no bits on. If an error is reported, a B message may be entered to continue checking the remaining bits. This is the first test of the wrap register in the SC3 card.

**Routine 2A, 8130 "Halt" Line System Test.** Can be used to isolate halt line failures in the PSCF. When the processor detects incorrect parity, it activates the "halt" signal and the selected adapter should set its machine check bit in basic status. This routine issues a Read BSTAT command (with incorrect parity forced) to each adapter in the system, which should cause the "halt" line to set the machine check bit. The routine does three different tests: Machine check, Halt, and Reset.

**Routine 2B, 8130 Data Bus Parity Check Test.** The marker force 2/10 command places invalid data parity on the I/O bus. This routine tests the adapter parity detection logic by using byte and halfword commands. The routine does a Machine Check and a Halt Test.

**Routine 2C, 8130 File Channel I/O and Release Request Test (selectable only).** This routine checks the operation of the operation of the release request line when activated by the BSC/S-S communications adapter. If the configuration table indicates this adapter was installed, and a BSC/S-S communications adapter is present, the routine will be run. The release request line should be activated by BYSNC interrupt request and should cause the file adapter doing CHIO operations to stop. The test should proceed as follows:

1. Run the test without the BSC/S-S adapter and check for success.
2. Force the BSC/S-S adapter to interrupt.
3. Start CHIO and test for release request.
4. Delay and check for CHIO complete.
5. Remove the BSC/S-S adapter interrupt.
6. Check for CHIO operation complete.
7. If ECC is installed, CHIO test is run with bad parity data in the buffer. CHIO and adapter machine checks should occur.

**Routine 2D, 8130 Diskette Channel I/O and Release Request Test (selectable only).** This routine checks the operation of the release request line when activated by the BSC/S-S communications adapter. If the configuration table indicates this adapter was installed, and a BSC/S-S communications adapter is present, the routine will be run. The release request line should be activated by BYSNC interrupt request and should cause the diskette adapter doing CHIO operations to stop. The test should proceed as follows:

1. Run the test without the BSC/S-S adapter and check for success.
2. Force the BSC/S-S adapter to interrupt.
3. Start CHIO and test for release request.
4. Delay and check for CHIO complete.
5. Remove the BSC/S-S adapter interrupt.
6. Check for CHIO operation complete.
7. If ECC is installed, CHIO test is run with bad parity data in the buffer. CHIO and adapter machine checks should occur.





The following tests run only on the 8140 and the 8130 with the System Expansion Feature installed.

**Routine 30, Unit Connected Command Test.** Unit status register (USR) bit 3 (unit connected) determines the logical attachment of the I/O unit (SSCF/SC5 card) to the 8100. This routine sets bit 3 in each adapter's USR, and then reads the register to ensure that a timeout does not occur.

**Routine 31, I/O Unit Invalid Operation Test.** Each I/O unit appears as an individual adapter to the SCF. This routine tests the ability of an I/O unit to reject all invalid commands.

**Routine 32, PSV Valid Bit I/O Test.** The processor always checks for invalid parity during I/O read commands. If the adapter does not activate the "valid" line, it sets the V bit in the PSV. This test issues a Read Sublevel command with the parity even, (one byte at a time). The parity valid line is not activated by this command.

**Routine 33, Tag/Valid Wrap Tests.** The SCF can wrap a byte of data (P, 0—7) from the PSCF wrap register to the processor on the B0 bus. The data is also sent over the Tag bus to the SSCF card. From the SSCF card it is sent to the PSCF on the Valid bus. From the PSCF it is sent to the processor over the B1 bus. The test checks one bit at a time. If an error is reported, a B message may be entered to continue checking the remaining bits. The last test is done using adapter address 08. This test sets all bits on.

**Routine 40, Unit Status Register Data Test.** After bit 3 (unit connected) has been set, this routine reads and writes the eight USR bits one at a time.

**Routine 41, Reset Unit Status Register under Mask Test.** Tests the Reset command by first setting the register to all 1's. The routine then issues a Reset command with the mask containing only a single bit. Bits 0—3 are individually reset, and bits 4—7 are loaded from the mask bits. Bit 3 must always be set to properly execute the read commands.

**Routine 42, Time Test.** This routine tests I/O timing of the 8100 System. A series of I/O write commands is given, and a count of the number of commands performed during a fixed interval is recorded. The same sequence is repeated using read commands; more read commands should be done during the time interval. The I/O commands are done in level 7, with the timer signaling an end to the time period by forcing a level-0 I/O interrupt. If more passes are required, the interrupt is reset and I/O instructions are resumed.

**Routine 43, Unit Connected Broadcast Read Command Test.** SSCF status can be determined by using three commands: (1) Read bit 0, (2) Read bits 1 or 2, and (3) Read bit 3. All selected bits are OR'ed into a halfword, and each bit occupies a particular position depending on the unit address of the SSCF.

**Routine 44, I/O Adapter Interface Connect Test.** The I/O connect bit (bit 0) can only be set if bit 3 is also set. This test attempts to set bit 0 without bit 3 on. Then bits 0 and 3 are turned on and bit 3 only is reset. The unit status register is then checked to see that bit 0 was also reset so that the I/O unit is truly disabled.

**Routine 45, Unit Interrupt BSR(N) Bit 12 Test.** Bit 1 of the unit status register is reserved. If bit 3 and bit 1 are on, then bit 12 of the BSR(N) should not be set. This test sets bit 1 of the test unit status register. The BSR(N) is then checked for proper setting.

**Routine 46, Unit Interrupt BSR(0) Bit 11 Test.** Bit 2 of the unit status register is set by data tag time parity errors. This bit should then set BSR(0) bit 11. This test sets unit status register bit 2 with the SSCF enabled.

**Routine 47, Selective Reset Test.** The Reset Adapter command issued to PSCF(N) should not reset the SCF unit status register. In this test, bits 1 and 2 of the selected SSCF are set. This should set bit 11 of the BSR(0) and bit 12 of the BSR(N). The Reset Adapter command (N) is then issued. The BSRs are checked to ensure that the tests bit remain set. The adapter is disabled.

**Routine 51, USR Bit 9 Interface Test.** USR bit 9 is reserved. Byte 1 should always return zeros when the USR is read.

**Routine 52, Channel Request Priority Switch Test.** Each I/O unit contains a set of 4-bit switches that are used to further define channel request priority. To ensure that these switches are set properly, this test reads them. The data is then compared to the configuration data. The read CRP wrap command is used in this test. Release request and the two-bit CRP bus are also tested. Before wrap testing, the CRP values in the option field of the configuration table are checked for validity by scanning adapter types to determine the correct CRP values. The CRP switches are in module 1 and are switch numbers 7, 8, 9, and 10. If an error is reported, a B message may be entered to continue checking the remaining switches.

**Routine 60, Translate Array and Command Test.** The translate array in the SSCF is a 1 x 16 hardware array. It is used to provide the system with programmable interrupt capability. There are eight 2-byte slots of which only the odd byte is used. Bits 1–3 are for the primary level, and bits 4–7 are for the second level decodes. I/O halfword instructions are used to read and write these array slots. This test does an addressing test of the array and verifies that the instructions perform correctly.

**Routine 61, Translate Array Primary Translator Test.** Each SSCF uses a translator to convert hex values to a 1-of-16 bit code. In this test, each adapter slot is set to a unique level code. The Test Read Primary Level command is issued. The corresponding bit in the B1 bus should be returned. After all eight levels have been tested, the array is rewritten so that each slot has a new primary level. The test is complete after all slots have been tested for all levels.

**Routine 62, Translator Array Error Test.** Each translator in the SSCF will only translate a primary code value less than 8. If the array has bit 0 set, a parity error will be signaled if the array slot is read, since bit 0 will always be read as a 0. This test sets bit 0 in all slots and then reads each slot. Bit 2 of the unit status register should be set, causing an SCF signal bus check in BSR(0) to also be set. A halt should also occur. The routine runs on Level 7.

**Routine 63, Translator Array Second Level Test.** Each SSCF translator converts a second hex value to a 1-to-16 bit code when requested by a Read Second Level command. Only the slots that have a matching primary level active (interrupt request pending) will be translated. In this test, each slot is assigned a primary equal to its slot address. All eight slots will be given unique second level assignments. The Read Second Level Translate command will then be used to force the translation one slot at a time. Each slot is tested for all 16 valid secondary translate values.

**Routine 69, Translate Array Primary Translator Test.** This test is similar to Routine 61, except array bit 0 is set.

**Routine 6F, Solid Data Bus or IR Bit Test.** The adapter data bus is connected when bits 0 and 3 of the USR are set on. This test uses a halfword read command (to the IPL SW Register) to read known data. All data bits, except the one under test, are set on in the IPL Register. If there is a stuck adapter data bus bit, (or adapter IRB1 bit) a machine check will occur when reading that pattern of data. If the data error is in byte 1, the IOIRR is read to determine if the error is the data of the IR bit. This is done by setting each translate slot so that its presented interrupt will come in on a different line than the data bit under test.

**Routine 70, Real I/O Connection Test.** I/O adapters are connected to the bus when both bits 0 and 3 in the USR are set. This test does a reset adapter command to each of the 16 possible adapter addresses. At least one of the adapters should respond without timing out. First the adapters are polled with the unit disconnected. No response is expected.

**Routine 71, I/O Bus Output Data Driver Test.** When bits 0 and 3 are set in the USR, the adapter data bus is connected to the SCF bus. This test checks the 'basic' adapter data bus bits (13, 14, 15) for opens. The 'basic' bits are those output bits required by I/O operations during the TA/TC time. All existing adapters on the SSCF participate in the test. The test first issues a Reset adapter command to each adapter (bit 14 + addr). If this is successful, a reset BSR command is issued (bit 13 + addr). The Read BSR command is issued (bit 15 + addr). The errors will indicate the first failing bit in the first error data byte plus all the adapters that fail. Note that the active bits of the adapter addresss also participate in the test.

**Routine 72, I/O Bus Input Data Receiver Test.** When bits 0 and 3 are set in the USR, the adapter data bus is connected to the SCF bus. This test checks the I/O adapter data bus for opens. Driver bits (13, 14, and 15) and adapter address bits have already been tested in the driver test. The open test is done by using the basic status register of the available I/O adapters as a data source. It should be noted that only byte 1 of the data bus will be tested if no halfword adapters exist on the SSCF. All adapters will be tested. The routine records all failing adapters; however, only the first failing bit is indicated.

**Routine 73, IO/IR Bus Open Test.** When Bits 0 and 3 are set (in the USR), the adapter IO/IR Bus is connected to the SCF bus. This test finds an adapter; then sets an interrupt on and reads the IO/IR Bus for the proper data. The test is done eight times using the same adapter. Each time the translate array is set for a different level. Then the eight tests are repeated for each adapter on the SSCF.

**Routine 74, I/O Adapter Interrupt Capacity Test.** Checks the ability of the SSCF translate hardware to translate the required maximum number of interrupts. This is done by causing all the adapters on the SSCF to present a different primary interrupt. The I/O bus is then disabled. When the bus is reconnected, the 101RV is immediately read and the number of interrupts compared with an expected mask (derived from configuration table data). This test is also a test of the IRR line.

**Routine 75, Selective I/O Group Reset Test.** An SSCF with status bits 0 and 3 reset to zero will activate an I/O reset to all adapters (on the I/O unit). In this test, all the attached adapters are enabled. Then each of the bits (0 and 3) are individually reset and set. The adapters (BSR) should remain enabled. The bits (0 and 3) are then reset and set. All the adapters should receive the I/O reset and be disabled.

**Routine 79, I/O Read B0/B1 Data Check Test.** The marker force bit 2/10 command is used in conjunction with the IOH instructions to verify that the I/O parity checkers are working properly. First a read without a parity valid is issued with bit 2 only, causing the even parity. Then the read with bit 10 causing even parity is issued. In each case, the data stored is tested.

**Routine 7A, Dynamic SSCF Parity Check Read Test.** When the processor detects bad parity on read I/O commands, the "halt" signal should be raised and the selected adapter should set its system check bit. This test forces a read with bad parity from the SSCF that should cause a system check at the processor. The halt line should then set USR 2 bit, which in turn should set BSR0 bit 11.

**Routine 7B, Dynamic SSCF Parity Check Write Test.** The SSCF should detect bad parity and set bit 2 of its USR directly. This should also cause the SSCF to withhold the "valid" signal and cause a processor timeout. In this test, a set USR command with bad data is used to set the test conditions.

**Routine 87, Unit Release Request Switch Test.** To be added.

**Routine 88, "Halt" Line System Test.** Can be used to isolate halt line failures in the PSCF and SSCFs.

When the processor detects incorrect parity, it activates the "halt" signal and the selected adapter should set its machine check bit in basic status. This routine issues a Read BSTAT command (with incorrect parity forced) to each adapter on the I/O unit, which should cause the "halt" line to set the machine check bits in the adapters BSTAT. The routine does 3 differenct tests:

Machine check test: Tests that each adapter that sends bad data will cause an I/O parity check.

Halt test: Tests that BSTAT bit 5 is set on a bad parity operation.

Reset test: Tests that KDO I/O reset will properly reset all adapters (BSTAT).

**Routine 89, Data Bus Parity Check Test.** The marker force 2/10 command places invalid data parity on the I/O bus. This routine tests the adapter parity detection logic by using byte and halfword commands. The routine does a Machine Check and a Halt Test.

*SC213 SCF System Test Routine Descriptions*

**Routine 90, File Channel I/O and Release Request Test.** This routine checks the operation of the release request line when activated by the BSC/S-S communications adapter. If the configuration table indicates a file adapter and a BSC/S-S communications adapter are present, the routine will be run. The release request line should be activated by BYSYNC interrupt request and should cause the file adapter doing CHIO operations to stop. The test should proceed as follows:

1. Run the test without the BSC/S-S adapter and check for success.
2. Force the BSC/S-S adapter to interrupt.
3. Start CHIO and test for release request.
4. Delay and check for CHIO complete.
5. Remove the BSC/S-S adapter interrupt.
6. Check for CHIO operation complete.
7. If ECC is installed, CHIO test is run with bad parity data in the buffer. CHIO and adapter machine checks should occur.



It should be noted that all CCA adapters using BSC must have the release request switch set on the SC5 card (SSCF). Start/Stop adapters must have the switch off. The switch is adapter/port-dependent. The test is run on all BSC/S-S adapters and file adapters in the system.

**Routine 91, Byte Tag Test.** Halfword adapters must deal with the BSR on a byte basis. This can be done by implementing the byte tag. In this test, all halfword adapters are scanned to see that they perform BSR operations properly. All errors are presented after the testing is completed. If all adapters failed, a different error message is issued.

**Routine 92, Maintenance Tests, and Power Down and Timer (BOP) Tests (selectable only).** The design of the 8140 allows for the online maintenance of adapters. To facilitate this feature, individual 8101s can be powered down without affecting the operation of the programs running in the 8140. In this test, the operator is told to power down a unit under test while the test is running. An I/O interrupt should occur (SSCF power drop). The operator can then repower the unit. After each change of power status, a message is issued confirming the change. The routine will run until the operator 'frees' the routine or 5 minutes have elapsed. This is done by allowing the timer to run and display on the BOP. The display is XYYZ (X = minutes, YY = seconds, Z = tenths).

**Routine 93, System Channel Request Priority Test.** Each I/O unit contains a set of 4-bit switches that are used to further define channel request priority. To ensure that these switches are set properly and that the priority/contention circuits are working properly, a CRP wrap is done with all the I/O units participating in the function. First the configuration table is used for determining the expected unit according to priority. Then several wraps are done to check the priority logic, and a test is also made to ensure no duplicate CRP values exist.

**Routine 94, Read Connected Control/Unit System Test.** The USR connected bit (0) connects all the adapters on the unit with the I/O bus. The Read Connected Status Broadcast command presents all unit status in a halfword. This test attempts to connect all of the possible I/O units. A test is made to ensure that they connect according to the configuration table. After the connecting has occurred, the status of the connected units is determined by issuing the Read Connected Unit bit 0 and bit 3 commands.

**Routine 95, Read Interrupt Request System Test.** The Read Interrupt Request Broadcast command reads the interrupt status of all system units. The interrupt sequence is a combination interrupt request or USR check. All the units on the system are connected, then all the interrupt request bits are set and read. Then all the USR check bits are set and read.

**Routine 96, Tape Channel I/O and Release Request Test.** This routine checks the operation of the release request line when activated by the BSC/S-S communications adapter. If the configuration table indicates a tape adapter and a BSC/S-S communications adapter are present, the routine will be run. The release request line should be activated by BYSNC interrupt request and should cause the tape adapter doing CHIO operations to stop. The test should proceed as follows:

1. Run the test without the BSC/S-S adapter and check for success.
2. Force the BSC/S-S adapter to interrupt.
3. Start CHIO and test for release request.
4. Delay and check for CHIO complete.
5. Remove the BSC/S-S adapter interrupt.
6. Check for CHIO operation complete.
7. If ECC is installed, CHIO test is run with bad parity data in the buffer. CHIO and adapter machine checks should occur.

It should be noted that all CCA adapters using BSC must have the release request switch set on the SC5 card (SSCF). Start/Stop adapters must have the switch off. The switch is adapter/port-dependent. The test is run on all BSC/S-S adapters and tape adapters in the system.

**Routine 97, Display/Printer Channel I/O and Release Request Test.** This routine checks the operation of the release request line when activated by the BSC/S-S communications adapter. If the configuration table indicates a display/printer adapter and a BSC/S-S communications adapter are present, the routine will be run. The release request line should be activated by BYSNC interrupt request and should cause the display/printer adapter doing CHIO operations to stop. The test should proceed as follows:

1. Run the test without the BSC/S-S adapter and check for success.
2. Force the BSC/S-S adapter to interrupt.
3. Start CHIO and test for release request.
4. Delay and check for CHIO complete.
5. Remove the BSC/S-S adapter interrupt.
6. Check for CHIO operation complete.
7. If ECC is installed, CHIO test is run with bad parity data in the buffer. CHIO and adapter machine checks should occur.

It should be noted that all CCA adapters using BSC must have the release request switch set on the SC5 card (SSCF). Start/Stop adapters must have the switch off. The switch is adapter/port-dependent. The test is run on all BSC/S-S adapters and display/printer adapters in the system.

**Routine 98, Diskette Channel I/O and Release Request Test.** This routine checks the operation of the release request line when activated by the BSC/S-S communications adapter. If the configuration table indicates a diskette adapter and a BSC/S-S communications adapter are present, the routine will be run. The release request line should be activated by BYSNC interrupt request and should cause the diskette adapter doing CHIO operations to stop. The test should proceed as follows:

1. Run the test without the BSC/S-S adapter and check for success.
2. Force the BSC/S-S adapter to interrupt.
3. Start CHIO and test for release request.
4. Delay and check for CHIO complete.
5. Remove the BSC/S-S adapter interrupt.
6. Check for CHIO operation complete.
7. If ECC is installed, CHIO test is run with bad parity data in the buffer. CHIO and adapter machine checks should occur.

It should be noted that all CCA adapters using BSC must have the release request switch set on the SC5 card (SSCF). Start/Stop adapters must have the switch off. The switch is adapter/port-dependent. The test is run on all BSC/S-S adapters and diskette adapters in the system.

**Routine 99, Power Down Test (selectable only).** The SCF should drop system power when the Drop Power command is issued and the KDO enable power drop and enable KDO commands have been issued. This test will fail only if the power does not drop.

**Routine 9A, Modifier Test.** This test of the modifier line is run on diskette and tape adapters. The modifier line is used by the diskette adapter to allow register sets 8–11 to be used for channel operations. The modifier line is used by the tape adapter to accomplish odd byte data transfers.

**Routine 9C, Adapter System Test.** Connects all the I/O units at once and then forces an I/O interrupt on all adapters possible on the system. Each adapter is assigned a unique primary/secondary interrupt level. The secondary level is set by the control address. The primary level is based on the I/O unit address. The IOIRV is tested for primary level interrupts. The Read Secondary command verifies that only the configured adapters respond. This test verifies the accuracy of the configuration table adapter addresses. All adapters are contained in the adapter table. All slots in the SSCF arrays are preset to interrupt on primary level 0, and the secondary level is the I/O unit address. The wired array adapter slot is contained in bits 0–2 of the configuration table byte entry for the adapter. This is set by routine 9F.

**Routine 9D, IPL Switch Display (selectable only).** This routine reads the IPL switch register and presents the data as an information display to the operator.

**Routine 9E, Release Request Switch Test.** This routine checks the Release Request switches on the SC5 card. These eight switches are numbered by port number. Only a BSC communications adapter should have the switch set on. This routine scans all adapter addresses and runs the test on all adapters except the BSC/SS adapters. The test is similar to routine 90. The CHIO device is the first file adapter in the configuration table. If the release line is activated, the Release Request switch is set on (error).

**Routine 9F, Real I/O Adapter Scan Routine (selectable only).** There can be a maximum of eight I/O adapters on each I/O unit. These adapters can have a possible 15 different addresses. This routine attempts to connect all 15 possible I/O units and then read the status for all possible I/O adapters. Any adapter that responds will be recorded and then presented to the operator as a list of all available adapters. The list will be given a line at a time on a unit basis, and will contain the slot that the adapter is actually assigned to. This is done by forcing a level 7 I/O interrupt to each responding adapter. The secondary level presented will be the slot assignment. For 8130, only the responding adapters are given.

**Routine A0, System Translator Read Test.** Each SSCF contains a translator array which is written at SYSGEN time. If a parity error occurs, improper I/O interrupts can occur, causing erroneous interrupt processing or a system hard wait. It is important not to run the SCF diagnostic as it could mask an intermittent error. This routine should be run and looped first. It will read all the slots in all the arrays in the system. It will force interrupts to I/O units and test interrupt translations for the I/O units on the system. The error message will indicate the failing SSCF card and the failing slot.

**Routine A1, Miscellaneous Channel Operation Tests.** Channel operation is allowed whenever the channel mask is set and the EIRV register bits 0–5 are zero. In the first test, a File is started with the channel mask off. The operation should not complete until the mask is enabled. The second group of tests is then done by setting all the 'EIRV' bits (5 to 0), one at a time. Each bit (except bit 4) being set should cause the channel to be masked off. A file CHIO operation should not start or finish until the MCPC is cleared. The last test checks that all channel pointer registers will operate properly. The same CHIO operation is performed with a different channel pointer set until each has been tested.

**Routine A2, Disabled Channel Operation Tests.** The channel request and grant lines are not gated by the SSCF cards. To test this function, the following tests are done:

1. The channel mask is disabled.
2. A channel buffered adapter is started.
3. Bit 0 of the SSCF status register is disabled.
4. The channel mask is enabled.
5. Wait for a period of time.
6. Turn off the channel mask.
7. Set SSCF status bit 0 on.
8. Read MCPC.
9. Test for successful completion.

**Routine AE, Run All Channel Adapters Test.** This routine runs all (see routine AF description) CHIO adapters while using storage volume 0 only. Each CHIO adapter is serially actuated to do an adapter write operation, and locations hex 0100 through hex FFFF are tested. (see background storage test)

**Routine AF, Selectable, Run All, Multi Adapter Channel Tests.** This selectable routine will run or loop routines B0 through BF only. This routine provides a storage scan looping facility. After invoking this routine, an "enter test address" message is issued. This message allows the operator to enter up to 16 adapter addresses to select the adapters to be run in routines AE through C0. The default of entering no adapter addresses is to run all adapters in the configuration table.

**Routine B0–BF, Multi Adapter Channel Test.** Channel operation is allowed whenever the channel mask is set. In this test all channel adapters are started with channel write operations (file, diskette, tape, display, HPCA). The channel mask is disabled. All operations use the same buffer. After all operations have been started, the channel mask is enabled. All operations should complete without error. The data buffer is started at the first location in a volume. The first test (buffer location 0 volume 0) should cause all CHIO adapters to generate a machine check during the test. Testing continues by moving the buffer upward through storage until the upper boundary has been reached (either 32K or 64K). This interactive test is designed to uncover adapter/storage problems. On error, the first error is captured but not printed. The EIRV is then cleared and the test allowed to complete. After all the adapters have finished their CHIO operations, the first error will be printed. Giving the 'B' message after this will present the adapter status of all the adapters participating in the test. The first error message will be as follows:

08X8, BX4B, ADP ADDR, ADP STATUS, MCPC, BUFFER VOL, BUFFER ADDR, EVEN CPR, ODD CPR

The second message will be as follows:

08X8, BX73, ADP, ADP STATUS, MCPC, ADPT 1, ADPT 1 STATUS, MCPC, ETC

**Notes:**

1. *CHIO devices must be ready.*
2. *Background Storage Test – When all Channel Requests are active, after the Channel Mask has been enabled, storage testing, using the same buffer, is started with CLS, MVHS, and TS instructions. Before each Move test, a TS instruction is issued to the 2-byte area used in the Move, except in the move test.*

   *The Move test will move the buffer to itself on a halfword basis. The buffer is saved and restored. The data pattern to be tested is a floated-one then a floated-zero for each address.*

   *The Compare test sets the destination bus to all ones and then compares each byte of data in the buffer. On machines with ECC, the background storage test is not run. Each hex 800 byte block of storage is tested for data integrity.*
3. *As an adjunct test, all adapter interrupt slots are set to a unique primary/secondary level. After a pass has been completed, the IOIRR, each interrupt, and all channel pointer registers are tested. The HPCAs only support 16-bit addressing and require three channel pointer registers. Each HPCA writes from a "pong" buffer (address under test) and then in full duplex mode reads into the "ping" buffer (fixed address).*

**Routine C0, Channel Request High Release Request Tests.** Adapters issuing a channel-high request should also activate the release request line (to stop burst data transfers). In the 8100, HPCAs are the only adapters wired to the channel request high line. In this test, each HPCA is wrapped so that a byte of HPCA data is placed in the write buffer of an operating buffered channel request adapter. If the HPCA is wired to the channel request high line (HPCAs above 9.6K), then the data written to the buffered adapter should include the byte of HPCA data. To check this, the buffered adapter is read. Low-speed HPCAs should not activate the release request line. The buffer used by the test CHIO device contains hex 20 data. The HPCA buffer contains hex FF data. This test is run as follows:

1. Find all HPCAs; count and identify high-speed HPCAs (above 9.6Kb).
2. Find a CHIO adapter (see routine AF description). Start the adapter; start an HPCA check for proper completion. Check for release line action.
3. Tests are repeated until all HPCAs are run against all CHIO adapters specified.

## SC230 Test Message Formats and Status Registers

This section describes the message formats used for SCF testing. These messages occur only offline, as there are no SCF online tests available.

### *SC231 SCF Offline Test Message Formats*

The following test messages can be generated during SCF testing:

PA00 = SCF tests completed successfully.

PAF0 = SCF tests are running.

The following test error message formats are generated during SCF testing:

Format 1 - PAXE RREN

Format 2 - PAXE RREN DBAD (AD is optional)

Format 3 - PAXE RREN ADAD ADAD ADAD ADAD*

Format 4 - PAXE RREN CNFG (8 BYTES) LOCA

Format 5 - PARR ADAD (AD is optional)

Format 6 - PAXE RREN IR

Where:

PA = Physical address. Depends on SSCF location. Refer to SC112.

X = Level 1 = PSCF
2 = SSCF

E = Error defined by the following:

RR = Failing routine number (01-A0)

EN = Error number. Refer to SC240, which defines the error.

DB = Data Bit

AD = Address of failing adapter*

CNFG = Configuration entry (see SC113)

LOCA = Location of configuration table entry from beginning of table in hex (0500 is the 6th entry in the configuration table).

IR = Interrupt request line number

*In Format 3, there may be from 1 to 8 failing adapter addresses.

The following error messages use Format 2:

PA2E 335X
PA2E 6F06
PA2E 6F11
PA2E 7161
PA2E 7163
PA2E 7203

The following error messages use Format 3:

PAXE RR01
PA1E 2A01
PA1E 2A2D
PA1E 282D
PA1E 2B02
PA2E 7420
PA2E 7520
PA2E 8802
PA2E 882D
PA2E 8902
PA2E 892D
PA2E 9C01
PA2E 9C02

The following error messages use Format 4:

PAXE 0018
PAXE 003F
PAXE 0041
PAXE 0042

**Note:** *RR = 00 indicates configuration table errors.*

The following error messages use Format 5:

PA15 - Test stopped at Routine 15.
PA20 - Test stopped at Routine 1D.
PA30 - Test stopped at Routine 30.
PA40 - Test stopped at Routine 40.
PA43 - Test stopped at Routine 43.
PA47 - Test stopped at Routine 47.
PA70 - Test stopped at Routine 70.
PA73 - Test stopped at Routine 73.
PA74 - Test stopped at Routine 74.
PA90 - Test stopped at Routine 90.
PA91 - Test stopped at Routine 9A.
PA92 - Test stopped at Routine 9E.
PA93 - Test stopped at Routine A1.
PA96 - Test stopped at Routine 96.
PA97 - Test stopped at Routine 97.
PA98 - Test stopped at Routine 98.
PA99 - Test stopped at Routine 99.

The following error message uses Format 6:

PAXE 7305

**Note:** *When entering a PAXE test error message into the MD, MAP menue selection 4, enter with no spaces:*

| *Correct* | *NOT Correct* |
|---|---|
| *PAXERREN* | *PAXE RREN* |

*SC232 Not Used*

*SC233 SCF Status Registers*

The two PSCF status registers, BSTAT and PSCF EIR, are both physically located in the SC1 card. Each SSCF (SC5) card also contains an SSCF unit status register.

**PSCF Basic Status Register (BSTAT)**

The SCF basic status register contains the current hardware status of SCF Levels 0 and 3. Several commands, such as Set, Reset, and Reset under Mask, can be used to perform various operations that affect the status of the register bits. This register is addressed with hex 08 on Level 3. The PSCF BSTAT, which uses address hex 08 for information transfer, also enables and controls the operation of the 100-ms timer. The following table describes the PSCF BSTAT bit meanings:

| Bit | Meaning |
|---|---|
| 0 | Reserved |
| 1 | Programmed IPL Register Valid — Set only by the program, and indicates that the programmed IPL register contents can be used during a program mode IPL sequence. Either a power-on reset sequence, pressing the BOP Reset/IPL pushbutton, or the program, can reset this bit. |
| 2 | Reserved |
| 3 | Power-on Reset — Set by hardware during a power-on reset sequence to indicate restoration of system power. This bit determines the system initialization required during IPL execution, and can also be set and reset by programming. |
| 4–6 | Reserved |
| 7* | Processor Storage Select — When on, all data read and write and all instruction fetch operations access processor storage and not ROS. When off and using a real storage address under 4K, all instruction fetch and read operations are from ROS, but all writes are to processor storage regardless of bit status. This bit can be set and reset by programming, and can also be reset by a power-on reset or pressing the Reset/IPL pushbutton on the BOP. |
| 8 | 100-ms Clocked Interrupt — Set by hardware when either bit 9 turns on or by a 100-ms elapsed time interval with bit 9 on. Can also be set and reset by program, and also turns on bit 15 when on. |
| 9 | Timer Enabled — Set only by programming, which then permits bit 8 to present an interrupt from the 100-ms clock. Can be reset both by hardware and programming, and, when reset and set, always turns on bit 8. |
| 10 | Reserved |
| 11** | SSCF Power Outage — An 8101 dropped power. Can be set by programming, and also turns on bit 15. |
| 12 | Reserved |
| 13 | PSCF Equipment Check — While executing a PIO to either PSCF level hex 08, the BOP, or the EFP, the channel detected an error and issued a "halt" signal. This bit can also be set and reset by programming, and reset by hardware. |
| 14 | PSCF Enabled — Permits the PSCF to interrupt processing on the currently assigned priority level. Bit 15 indicates the pending interrupts according to the status of bits 8 and 11. Only set by programming, and can be reset by both programming and hardware. |
| 15 | PSCF Interrupt Request — The PSCF is requesting processor interrupt servicing. Set by programming and also by bits 8, 9, 11 and 12. Cannot interrupt processing unless bit 14 is on, but stays set until being reset either from programming or hardware. |

*Applies only to 8130 with or without the System Expansion Feature.
**Applies only to 8130 with System Expansion Feature and all 8140s.

**PSCF Error Information Register (EIR)**

The PSCF EIR provides current PSCF error status, and uses commands such as Set, Reset, and Reset under Mask to perform various operations that affect the register bit status. The following table describes the PSCF EIR bit meanings:

| Bit | Meaning |
|---|---|
| 0 | Reserved |
| 1 | BOP/PSCF Priority Level Control — When set, BOP and PSCF are assigned to Level 0, and, when reset, they are assigned to Level 3. Set only by programming, and reset either by programming or hardware. |
| 2, 3 | Reserved |
| 4 | I/O Read Check — Set by hardware when an out-of-parity condition occurs while returning (reading) data to the program and using either the BOP, EFP, or PSCF. If using PSCF address hex 08, it also sets bit 13 in the PSCF BSTAT, and, if using PSCF address hex 0C, it sets bit 13 in this register. Can also be set by programming. |
| 5 | Reserved |
| 6 | SSCF installed. |
| 7 | Reserved |
| 8 | Timer Check — Set by programming, or by hardware when it detected a timeout condition of the 100-ms clocked interrupt. Reset either by programming or hardware. |
| 9 | I/O Write Check — Set by hardware when an out-of-parity condition occurs while receiving (writing) either data or the command byte from the program and using either the BOP, EFP, or PSCF. If write errors occur while using PSCF address hex 08, bit 13 in the PSCF BSTAT is set by the HALT signal, and, if using PSCF address hex 0C, it sets bit 13 in this register. Can also be set by programming, and reset either by programming or hardware. |

| Bit | Meaning |
|---|---|
| 10 | Reserved |
| 11* | SSCF Equipment Check – An enabled SSCF detected an error during a PIO operation. The SSCF in error sets its own status register bit 2, and, if the SSCF detected the error, it sets its own bit 2 and this bit also. Set by hardware or programming. |
| 12 | Reserved |
| 13 | PSCF Address Hex 0C Equipment Check – Set when (1) an invalid parity condition was detected on either the command byte or the data received (written) from a program, or the data sent (read) to the program, while performing a PIO operation to PSCF address hex 0C, or (2) the channel issued a halt to PSCF hex 0C. Reset by either hardware or programming. |
| 14 | Reserved |
| 15 | Reserved |

*Applies only to 8130 with the System Expansion Feature and the 8140.

**SSCF Unit Status Register (USR)**

The SSCF USR physically resides in the SC5 card and contains status information specifically related to information transfer from the PSCF to the attached device through the SSCF. The following table describes the SSCF Unit Status Register bit meanings:

| Bit | Meaning |
|---|---|
| 0 | I/O Group Enabled – If on, permits programmed access to devices attached to the register's associated SSCF. Set by program. |
| 1 | Reserved |
| 2 | SSCF-Detected Error – If on, the associated SSCF received either (1) a PIO command with invalid parity, (2) an invalid PIO command, (3) an invalid parity condition on a write data operation, (4) an invalid parity condition on a read translation array priority level assignment, or (5) a halt signal from the channel while executing an I/O operation. This bit sets bit 11 in the PSCF EIR. No SSCF information transfer can occur until the SSCF that detected the error turns off this bit. |
| 3 | SSCF Enabled – If on, permits programmed access to the SSCF and its attached devices for read and write-type operations. If off, only write-type operations can occur. |
| 4–7 | Reserved |

## SC240 Test Messages and Descriptions

The following table lists and describes the test error messages generated while using the system control facility MAP. Normally, only RREN values will be displayed. SC231 shows special error formats for certain routines.

| RREN | Meaning |
|---|---|
| RR01 | Unexpected system check |
| RR02 | System check did not occur when expected |
| RR03 | Wrong system check |
| RR04 | Unexpected I/O interrupt |
| RR05 | No I/O interrupt when expected |
| RR06 | Solid interrupt |
| RR07 | Basic status register error |
| RR08 | Device status register error |
| RR09 | Channel request for priority during write |
| RR0A | Channel request for priority during read |
| RR0B | Processor error |
| RR0C | SSCF array error |
| RR0D | SSCF translator error |
| RR0E | Spurious interrupt |
| RR0F | Halt error |
| RR10 | Wrong level |
| RR11 | Data error |
| RR12 | Operator panel error |
| RR13 | No secondary interrupt request |
| RR14 | Timer error |
| RR15 | Timer fast |
| RR16 | Timer slow |
| RR17 | Timer did not step |
| RR18 | Channel request high configuration error |
| RR19 | ROS/RAM bit error |
| RR1A | Driver error |
| RR1B | SSCF installed (status bit 6) error |
| RR1C | Reset device status register error |
| RR1D | Device connection error |
| RR1E | Channel request for priority error |
| RR1F | Switch error |
| RR20 | No response from I/O adapter |
| RR21 | Select error |
| RR22 | Multiple no responses from I/O adapters |
| RR23 | Byte operation error |
| RR24 | Condition code error |
| RR25 | Unexpected response |
| RR26 | Read secondary error |
| RR27 | CHIO error |
| RR28 | CHIO error 1 |
| RR29 | CHIO error 3 |
| RR2A | CHIO did not complete |
| RR2B | CHIO error 2 |
| RR2C | Enable error |
| RR2D | Reset error |
| RR2E | Power drop |
| RR2F | Exception error |
| RR30 | Timer slow |
| RR31 | Timer fast |
| RR32 | No exception |
| RR33 | Interrupt error |
| RR34 | CHIO error 4 |
| RR3E | Storage error |
| RR3F | Configuration table type error |
| RR40 | Wrap command error |
| RR41 | Configuration table error |
| RR42 | Configuration table system error |
| RR43 | KDO error |
| RR44 | Multiple system check |
| RR45 | Slot error |
| RR46 | Resource error |
| RR47 | Multiple byte error |
| RR48 | Input error |
| RR49 | CHIO device error |
| RR4A | CHIO machine check during release test |
| RR4B | CHIO machine check |
| RR4C | Modifier error |
| RR4D | Expansion feature error |
| RR4E | Configuration option byte 1 error |
| RR4F | Release error |
| RR51 | Wrap error number 1 |
| RR52 | Wrap error number 2 |
| RR53 | Wrap error number 3 |
| RR54 | Wrap error number 4 |
| RR55 | Wrap error number 5 |
| RR56 | Wrap error number 6 |
| RR61 | Test 1 bit 14 + address (Reset Adapter cmd) |
| RR62 | Test 2 bit 13 + address (Reset BSR cmd) |
| RR63 | Test 3 bit 15 + address (Read BSR cmd) |
| RR64 | Test 4 bit P1 + address (Set BSR cmd) |
| RR65 | DSR error 1 |
| RR66 | DSR error 2 |
| RR67 | Double MC error |
| RR70 | CHAN error with mask off |
| RR71 | CHAN error with mask on |
| RR72 | CHAN operation error |
| RR73 | CHAN machine check error |
| RR74 | Tape adapter status error |
| RR75 | Bit 0 error |
| RR76 | Message error |
| RR77 | Unexpected adapter error |
| RR87 | Basic status register contents wrong |
| RR9B | No device connection |
| RRFE | Release timeout error |
| RRFF | Control error |

## SC250 Action Plans

This section lists action plans that you can use, depending on the results of the SC tests.

**Caution: Power must be off before removing cards or installing cables.**

ACTION PLAN 1

If the error is PAXE 5241

or PAXE 524E

the configuration entry for the indicated PA does not match the table in SC113. Do steps 4 and 5 below to correct.

If the error is PAXE 0018 CNFG LOCA

or PAXE 003F CNFG LOCA

or PAXE 0041 CNFG LOCA

or PAXE 0042 CNFG LOCA

or PAXE 1B3F CNFG LOCA

or PAXE 1B41 CNFG LOCA

1. The LOCA field gives the location of the error in the configuration table in hex. (LOCA = 001F 31st entry from the beginning of the configuration table.)
2. RR = 00, which points to the configuration table.
3. EN = 3F, etc. (see (SC240).
4. Use the Free-lance Utility of the MD to check or change the configuration table.
5. After the configuration entry is corrected, run the SC tests.

ACTION PLAN 2

If the error is PA1E 2AXX ADAD ADAD ADAD ADAD

or PA1E 2BXX ADAD ADAD ADAD ADAD

1. Count the number of adapters that are failing. (The number of AD addresses in the error message; AD = 8X for 8130).
2. If there is only one adapter address in the error message, go to the MAP for that adapter to find the problem.
3. If all the adpaters in the 8130 are failing, go to Procedure 04 "SCF Signal Bus Fault Isolation" in Chapter 1, ST440, and loosen the adapters one at a time.
4. After loosening each adapter, run the SC tests in free-lance mode. When the error message changes, go to the MAP for that adapter to find the problem.
5. If after loosening all the adapters the error remains the same, go to the SC MAP to find the problem.
6. If more than one, but not all, adapters are in the error message, perform step 3 but only loosen the failing adapters one at a time.

ACTION PLAN 3

If the error is PA2E 4008

or PA2E 4308

or PA2E 6FXX

or PAXE 702X

or PAXE 7123

or PAXE 7161

or PAXE 7177

or PAXE 7211

or PAXE 732X (example: 881E 7320 or 982E 7320)

or one of the following MI messages:

PA30
PA40
PA43
PA47
PA70
PA73
PA74

1. Match the P in the error message to an address label on an operator panel of an 8101 or 8130/8140. (See SC112 for address label description and SC111 for locations of SSCFs.)
2. Go to Procedure 04 "SCF Signal Bus Fault Isolation" in Chapter 1, ST440, and loosen the adapters attached to that SSCF one at a time.
3. After loosening each adapter, run the SC tests in free-lance mode. When the error message changes, the error is in the loosened adapter. Go to the MAP for that adapter to find the problem. If the adapter tests give an error which is too basic for the adapter MAP, replace adapter cards for the failing adapter, one at a time.
4. If after loosening all the adapters the error remains the same, go to the SC MAP to find the problem.

ACTION PLAN 4

If the error is PAXE 7420 AD

or PAXE 9C01 AD

or PAXE 9C02 AD and other error messages using format 3 (see SC231):

1. Match the first digit of the AD field of the error message to an address label on an operator panel of an 8101 or 8130/8140 (see SC112 for address label description and SC111 for locations of SSCFs).
2. Run Routine 9F (see below) to confirm AD is the adapter address the SC tests have a problem with. If the AD address does not show in one of the Routine 9F displays, or if an 081E 9F01 AD message appears, it confirms that the adapter is causing the problem.
3. Go to the MAP for that adapter to find the problem. If the adapter tests give an error which is too basic for the adapter MAP, replace adapter cards for the failing adapter, one at a time.
4. If that MAP cannot find the problem, return to the SC MAP.

ACTION PLAN 5

If the error is PA2E 7520 ADAD ADAD ADAD ADAD

or PA2E 88XX ADAD ADAD ADAD ADAD

or PA2E 89XX ADAD ADAD ADAD ADAD

1. Count the number of adapters that are failing (the number of AD addresses in the error message).
2. Match the first digit of the AD field to an address label on an operator panel of an 8101 or 8130/8140. (See SC112 for address label description and SC111 for locations of SSCFs).
3. If there is only one adapter address in the error message, go to the MAP for that adapter to find the problem.
4. If all the adapters attached to an SSCF are failing, go to Procedure 04 "SCF Signal Bus Fault Isolation" in Chapter 1, ST440, and loosen the adapters one at a time.
5. After loosening each adapter, run the SC tests in free-lance mode. A PA2E 7161 0EAD error message will occur, where AD is the address of the loosened adapter. Ignore this message. Press the 'B' key on the MD hand held keypad. The test will continue. If the original error message appears, continue to loosen the adapters attached to that SSCF one at a time. When the error message changes, go to the MAP for that adapter to find the problem.
6. If after loosening all the adapters attached to that SSCF the error remains the same, go to the SC MAP to find the problem.
7. If more than one but not all of the adapter addresses attached to that SSCF are in the error message, perform step 4, but only loosen the failing adapters one at a time.

ACTION PLAN 6

If the error is PAXE52XX, perform the following procedure.

**Note:** *If the error is PAXE524E or PAXE5241, there is a configuration table error; go to Action Plan 1.*

1. Match the P in the error message to an address label on an operator panel of an 8101 or 8130/8140 (see SC112 for address label description and SC111 for locations of SSCFs).
2. Remove that SSCF (SC5 card).
3. Use Figure SC442-1 to check that SSCF switches 7 through 10 of module 1 are correct (see Figure SC442-2 for the SC5 card switch module locations).
4. There is a chance that switches 1-4 of module 1 may be wrong. If all the switches are correct, replace with a new card and run the SC tests again.

ACTION PLAN 7

1. Using MD diskette 01, select the SC MAP. At the MAP menu, select option 1 TO TEST EVERY SSCF. If an error message occurs, follow the MAP to fix the error.
2. If no error message occurs, select the Free-Lance Utility.
3. At 80BC, enter 08B; at 81BC, enter 009AB.
4. Look for an error 081E 9A4C AD, where AD is the address of the failing diskette adapter.
5. If there is another diskette adapter on the System, enter B.
6. If another 081E 9A4C AD error occurs and the two AD fields are the addresses of different diskette adapters, or if there is only one diskette adapter on the system, the error can be in the:

| | *8130* | *8140A* | *8140B* |
|---|---|---|---|
| a. SC1 card | at A2G2 | at A1A2 | at A1D2 |
| b. Processor card | at A1Q2 | at A1C2 | at A1F2 |
| c. Line between processor and SC1 card | A2G2G04-A1Q2U07 | A2G04-C2U07 | D2G04-F2U07 |

7. If only one error occurs when more than one diskette adapter was tested, change its SC5 card if not already exchanged. If the error is not corrected, return to step 6.

ACTION PLAN 8 – SCF BUS ERROR

(To be used when more than one SSCF is failing)

1. Pick an SSCF with an error message, preferably in the most outboard unit. (See SC111 for locations of SSCFs.)
2. Unplug the W, X, and Y top card cables from the SSCF. (See Note below.)
3. At the MD keypad, press the PF key. When the PF menu appears, select 1 to return to SC MAP menu. Re-IPL.
4. Select SC MAP menu 1, TO TEST EVERY SSCF.
5. When the SC tests have been run to every SSCF and the error messages are available, write them down. If only the SSCF with its W, X, and Y top card cables unplugged has an error message, go to step 11. Otherwise, go to step 6.
6. If all the SSCFs continue to have error messages (the SSCF with the W, X, and Y top card cables unplugged may now have a different error message), plug the W, X, and Y top card cables previously unplugged.
7. If there are other SSCFs you have not checked with this unplugging procedure, pick another SSCF and return to step 2.
8. If all the SSCFs have been checked with this unplugging procedure, at the MD keypad, press the PF key. When the PF menu appears, select 1 to return to SC MAP menu. Re-IPL.
9. Select SC MAP menu 4, TEST ERROR MESSAGE, using the 882E XXXX error message. Whenever the SC MAP calls out the SSCF card to be changed, ignore it as it has been isolated from the failure.
10. Leave this action plan and take directions from the MAP.
11. This SSCF card is holding down some line on the bus. Remove the SSCF card, replace it with a new SSCF card, making sure the switches on the card are set the same as on the old card. See SC442 if more information is needed about the switches.
12. Replug the W, X, and Y top-card cables.
13. Go to step 3 to rerun the tests to check there is no error message. If an error message occurs now, carefully check the ends of the top card cables and the interposers at the SSCF.
14. Go to step 3 again. If an error message persists, go to step 9.

**Note:** *In 8130s, remove the SSCF card, then replace the top card connectors so that outboard SSCFs remain connected to the PSCF.*

ACTION PLAN 9

1. Using MD diskette 01, select the SC MAP. At the MAP menu, select option 1 TO TEST EVERY SSCF. If an error message occurs, follow the MAP to fix the error.
2. If no error message occurs, select the Free-Lance Utility.
3. At 80BC, enter 08B; at 81BC, enter 0090B.
4. If there is no failure, a series of progress indicators will occur. A sample is as follows:

   X8908010 If the routine hangs here or X81E 904B 8000 error occurs, go to step 6.
   X8908011
   X8909010 If the routine hangs here or X81E 904B 9000 error occurs, go to step 5.
   X8909011

   These progress indicators show the machine running the first file adapter with the first communications adapter, then on through other combinations of both.
5. For instance this is the first time the file with address 90 is checked and the one with address 80 was OK. Error must come from the Modifier line being on between the SC5 card with address 98 and the DA1 or TA1 card with address 9X (see SC417 8101 Wiring), or the SC5, DA1, or TA1 card.
6. The error may be caused by the Modifier line being on in the following places (a meter is needed to check the condition of the signal):
   a. In the 8130/8140 between the SC5 card and the processor (see step 6 of Action Plan 7).
   b. In the 8130/8140 between SC5 card and the DA1 (see SC415 for 8140 DA1 board wiring or SC412 for 8130 board wiring).
   c. In an 8101 upper board where the Modifier line is not used but is turned on at the SC5 card (A1A2B12 at ground).
   d. In steps a and b above, the SC5, the DA1, or the TA1 card, if present, may be holding the Modifier line down.

ACTION PLAN 10 – TIMER ERRORS

| | | |
|---|---|---|
| 08XE 1114 | – Timer error | Go to step 5 |
| 08XE 1115 | – Timer extremely fast | Go to step 5 |
| 08XE 1117 | – Timer did not step | Go to step 1 |
| 08XE 1130 | – Timer slow | Go to step 2 |
| 08XE 1131 | – Timer fast | Go to step 2 |

where X = 1 or 2

1. Check to see if the -50/60-Hz line is open or grounded. This line enters the SC1 card at the P11 pin. Use PA450 and PA460 of the PA section to trace this line. It is called "Square AC" in the PA section. If no problem with this line is found, go to step 5.
2. If this error occurred while using a backup power source, the source may be out of specification. It may be checked at pin P11 of the SC1 card. If no problem is found, go to step 3.
3. If this is a 60-Hz machine, check that the jumper is present from J7-8 to J7-15. If this is a 50-Hz machine, check that the jumper is removed. (See PA460 of the PA section.) If the jumper is correct, go to step 4.
4. The +60-Hz Control line may be grounded. It may be checked at pin P10 of the SC1 card. Use PA450 and PA460 of the PA section to trace this line. This signal is inverted in the power logic so an open line may look like a grounded line at the SC1 card. If no problem with this line is found, go to step 5.
5. Return to the SC MAP to find the error. The SC1 card or the engine card containing the oscillator (A1Q2 in 8130) is suspect.

ACTION PLAN 11 – CHANNEL I/O ERRORS

Certain lines between SSCFs and Channel I/O adapters cannot be checked with the Primary and Secondary SCF tests. To check these lines, you must run certain routines of the SCF System tests.

If one or more files are on the 8100 System, run routine 90. If there is a tape drive on the 8100 System, run routine 96. If there is a display or printer on the system, run routine 97. If there is one or more diskette adapters on the system, run routine 98. The following table shows how to invoke these routines using the Free Lance utility:

| For Adapter | Routine to be Run | How to Invoke At 80BC | How to Invoke At 81BC |
|---|---|---|---|
| File | 90 | 08B | 0090B |
| Tape | 96 | 08B | 0096B |
| Display/Printer | 97 | 08B | 0097B |
| Diskette | 98 | 08B | 0098B |

Read the routine descriptions in section SC213 to familiarize yourself with the intent of each routine used. Read section SC510 for setup details and error message definitions.

Record each error message. From the error message (or combination of error messages) you may be able to pin-point the problem to a board, an adapter on a board, or a certain type of adapter (a byte-adapter, for example). Then use section SC410 to find the type of board or boards that match the suspected board(s), and check the continuity of Channel I/O lines that go to suspected adapters.

ACTION PLAN 12 – INTERRUPT BIT FAILURES WITH ERROR MESSAGE PA2E 7305 IR

1. Match the P in the error message to an address label on an operator panel of an 8101 or 8130/8140. See section SC112 for address label description and section SC111 for SSCF locations.
2. Go to section SC410 and pick the net listing that matches the board or boards with adapters using this SSCF.
3. Turn power off and use this net listing to check the continuity of the -IR/B1 bit line that matches the IR field of the error message.
4. If bad, replace the net or board; if good, return to the SC MAP.

ACTION PLAN 13 – SPECIAL POWER PROBLEM

After reading the SC diagnostic routine descriptions, a 1901 error message points you immediately to the SC1 card and its switches. Error message 1901 also occurs when the +5 Volts Control line going to the U05 pin of any SC5 card is open. To isolate this failure to one SC5 card, turn off power to the 8101 units on the system or loosen the SC5 cards in the system, one at a time, until the error message occurs beyond the 1901 error message.

Once you have isolated the problem to one SC5 card, check the continuity of the +5 Volts Control line. See section PA450 for the path this line takes to get to the board with the suspect SC5 card. The following table shows, for the various boards, the line name and path on the board to the U05 pin of the SC5 card:

| Unit | Line Name | Board | From | To (SC5) |
|---|---|---|---|---|
| 8130 | +5V | A2 | Any D03 | C2U05 |
| 8140 Mod A | +5V | A2 | Any D03 | D2U05 |
| 8140 Mod B | +5V Control | A2 | Z1D05 | A2U05 |
| 8140 Mod B | +5V Control | C2 | Z1D05 | A2U05 |
| 8101 | +5V Control | A1 | Z1D05 | A2U05 |
| 8101 | +5V Control | A2 | K4D05 | A2U05 |

While isolating to a single SC5 card, use the Free Lance utility. If the failure cannot be found, return to the SC MAP for further isolation.

HOW TO RUN ROUTINE 9F

To run SC routine 9F, use the Free-Lance Utility. At 80BC, enter 08B; at 81BC, enter 009FB.

A typical display is:

0805 adapter address
101112131F
0 1 2 3 7 } Wired in slots } these lines only show when SSCFs are in system

where 0805 is displayed because 08B was entered and five adapters are found to use the first SSCF checked. The second line contains the physical addresses of the adapters, the third line contains the SSCF array slots used by the adapters.

Enter B for the routine to display the same information for the next SSCF. Continue entering Bs until no more SSCFs are found. The 0800 is displayed to announce the routine is completed.

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## SC300 Intermittent Failure Repair Strategy

When intermittent failures occur, you can attempt fault isolation either by using the error log, looping the tests for an extended period while under MAP control, or using the Free-Lance Utility loop option to selectively loop the tests. Sections SC311, SC312, and SC313 explain these repair strategies, and SC350 lists the action plans you can use to help determine the cause of intermittent failures.

## SC310 Adapter-Unique Intermittent Repair Strategy

Other than the action plans contained in SC350, there are three options for determining the cause of an intermittent failure:

1. You can loop the SC tests offline under MAP control for 5 minutes.
2. You can obtain a copy of the system error log by using a DPPX or DPCX utility (see SC330 and also see Chapter 2, CP750 for DPPX and CP830 for DPCX). If the customer does not use an IBM operating system, error logging facilities are not available.
3. You can loop the tests selectively by using the Free-Lance Utility. In this manner, you can select a routine or group of routines and specify certain run options.

The following sections explain how to use these options.

### *SC311 Looping with MAP Interaction to Determine Failures*

The SC tests can be looped offline by using the SC MAP menu options 1, 2, or 3. All selections ask "DO YOU WISH TO CHECK FOR INTERMITTENT FAILURE BY LOOPING SC TESTS?"

- MAP menu option 1 consecutively tests each SSCF, and, when complete, automatically reinitiates testing.
- MAP menu option 2 loops only one SSCF continuously.
- MAP menu option 3 loops only the PSCF continuously.

These tests loop continuously and display "PA80 TEST LOOPING" on the MD until either an error is detected or you press the F pushbutton on the MD.

If the MAP detects an error while looping, the MAP directs you toward fault isolation in the same manner as a solid failure. Once you perform a repair action, the MAP loops the SC tests to verify the repair.

If the MAPs do not detect an error after looping the tests for 5 minutes, or random test errors messages occur, use the Free-Lance Utility looping option (see SC313).

### *SC312 Using the System Error Log to Determine Failures*

DPPX and DPCX use error logs to record any SCF failure that occurs during system operation. To use this log for intermittent fault isolation, obtain all error log records associated with the SCF. The information in the error log can be used to determine the failure type (see SC340) and also the action plan to use to correct this failure. If necessary refer to CP750 for DPPX and CP830 for DPCX in Chapter 2 for procedures. If the log does not contain any error entries, no SC failure occurred during system operation.

You can verify the repair action by running the SC tests using the Free-Lance Utility on the MD diskettes. (See CP462 in Chapter 2 and SC313.)



To invoke the Free-Lance Utility to verify a repair action on the System Control Facility:

1. On an 8140 or an 8130 with the System Expansion Feature installed, enter "08P8B" at 80BC and "1B" at 81BC.
2. On an 8130 without the System Expansion Feature, enter "08B" at 80BC and "B" at 81BC.

If the tests do not determine an error, return the system to the customer. After the system is operating, examine the error log for any SCF failures. If the error log indicates the same failure, you should perform the next step in the action plan. If the error log indicated that no failures occurred, end the repair action.

### *SC313 Using the Free-Lance Utility to Determine Failures*

Certain groups of SCF test routines are run depending on the invoke message used with the Free-Lance Utility:

| At 80BC | At 81BC | Routines Run |
|---|---|---|
| 08B | B | 01 through 2F |
| 08P8B | 1B | 01 through 8F |
| 69C | B | 90 through C0 |
| 08B | 00AFB | B0 through BF* |

*Routine AF is run to set up for Routines AE, B0–BF and C0.

The SCF tests can be looped without MAP interaction by using the Free-Lance Utility (see CP462 in Chapter 2). Also, refer to the following procedures for how to loop SCF tests or to loop a specific routine with test options.

To loop all SCF routines using the Free-Lance Utility:

1. At the 80BC or PA00 prompt message, enter either:
   - "08P8B" for an 8140 or an 8130 with the System Expansion Feature.
   - "08B" for an 8130 without the System Expansion Feature.

   Where:

   08 = PSCF physical address

   P8 = SSCF physical address (refer to SC113 for "P" value of SSCFs installed); otherwise use only the 08 entry

   B = Begin
2. At the 81BC prompt message, enter either:
   - "01B" if testing an 8130 without the System Expansion Feature.
   - "11B" if testing an 8140 or an 8130 with the System Expansion Feature.

The tests loop continuously until detecting an error. You terminate them by pressing "F" on the MD keypad.

If an error occurs while looping, the MD displays a test error message. Record this message and refer to the failure action plans contained in SC250 to diagnose and repair the failure.

After performing any repair action, loop the SC tests for at least 5 minutes to verify the repair.

To loop specific SCF routines and select run options using the Free-Lance Utility:

1. At either the 80BC or PA00 message, enter the 80BC parameters according to the procedure described in step 1 above for the 80BC or PA00 response.

2. At 81BC, enter SLRRB, where:

   S = 0 = run only PSCF routines 01 to 2F.

   1 = run the primary and designated SSCF using routines 01 to C0 (only on 8100s with SSCFs installed).

   L = 0 = run selected routine(s) once.

   1 = loop selected routine(s) and stop on error.

   2 = loop selected routine(s) and bypass errors.

   RR = zero or no entry runs all routines. A valid routine number runs only that routine, and must be specified to run selectable only routines 2C, 2D, 92, 99, 9D, 9F, or FF.

   B = begin test

## SC320 Error Log Information Needed for the SCF

Refer to Chapter 2 (CP750 for DPPX and CP830 for DPCX) for the procedure to obtain the error log. Perform two searches for log records. First, search for log records of the failing SSCF using its address 08P8 (see SC112). Then search for all log records of the SCF using 08 (see SC112).

## SC330 Error Log Formats and Meanings Used for the SC MAP

The format of the error log depends on whether the customer is using DPPX or DPCX. For DPPX formats, refer to SC331; for DPCX formats, refer to SC332.

### *SC331 DPPX Error Log Formats and Meanings*

**DPPX Type 5 Hardware Incident Record Format**

HEADER I

CLASS 05 SUBCLASS 01 OPTION (5)

DATE YY.DDD TIME HH/MM/SS

HEADER II

CLASS 05 SUBCLASS 01 OPTION (5)

DATE YY.DDD SEQ NO. (1)

RECORD

PA (2) SCA (3) DT (4)

CRC (7) COMPSTAT (8) ARC (9)

DATA (11) RES (12) CNT (13)

IOEP (14) ADWA (15)

CA (16) CPR (17) FRWA (18)

RES (19)

EXTENDED DATA

D01 (24)(25) D02 (26)(27) D03 (28)(29) D04 (30)(31)

D05 (32)(33) D06 (34)(35) D07 (36)(37) D08 (38)(39)

D09 (40)(41) D10 (42)(43) D11 (44)(45) D12 (46)(47)

D13 (48)(49) D14 (50)(51)

**DPPX Error Log Record Meanings**

The following listing describes the error log records used for SCF:

| Field | | Meaning |
|---|---|---|
| (1) | SEQ NO. | Sequence Number of the error log record. This is part of the Header II format provided by DISPLAY.ERRLOG if bit 0 of the Option Mask (field 5) = 0. If bit 0 = 1, header 1 has a time stamp in the format hour/minute/second.<br>With either header, a data field contains the year and Julian date.<br>The date is only valid when the customer sets it after every IPL using the SET.DATE command. The time is only valid when the customer runs DPPX with Timer Management and sets the time after every IPL using the SET.TOD command. |
| (2) | PA | Physical Adapter Address – Byte 0 of the FRB byte:<br>08 – PSCF Basic Status Register (BSTAT)<br>09 – Basic Operator Panel Adapter<br>0C – PSCF Error Information Register (EIR) |
| (3) | SCA | Secondary Component Address – Bytes 26, 27 of the FRB:<br>02 – TOD timer<br>01 – RTIT timer |
| (4) | DT | Device Type – "F" (hex 40C6) |
| (5) | OPTION | Option Mask – Byte 4 of DPPX Header:<br>Bit 0 = 1 – Time stamp (Header I)<br>= 0 – Sequence number (Header II)<br>Bit 1 = 1 – BCLE present<br>Bit 2 = 1 – Extended data present<br>Bit 3–7 = – Specifies format for extended data |
| (7) | CRC | FDM Request Code – Byte 1 of the FRB: |

| Function Request | CRC | Adapter Address | SCA |
|---|---|---|---|
| Read EIR status | 91 | 0C | |
| Set EIR status | 92 | 0C | |
| Reset EIR status | 96 | 0C | |
| Open adapter | 03 | 08 | |
| Terminate adapter | 6B | 08 | |
| No-op | 07 | 08 | |
| Read BSTAT status | 91 | 08 | |
| Set BSTAT status | 92 | 08 | |
| Reset BSTAT status | 96 | 08 | |
| Read IPL control | 89 | 08 | |
| Write IPL control | 86 | 08 | |
| Read IPL switch reg | 8D | 08 | |
| Program power off | 12 | 08 | |

| Field | | Meaning |
|---|---|---|
| (7) | CRC | FDM Request Code – Byte 1 of the FRB: (continued) |

| Function Request | CRC | Adapter Address | SCA |
|---|---|---|---|
| Read timer TOD | 81 | 08 | 02 |
| Write timer TOD | 82 | 08 | 02 |
| Disable timer TOD | 8A | 08 | 02 |
| Read timer RTIT | 81 | 08 | 01 |
| Write timer RTIT | 82 | 08 | 01 |
| Disable timer RTIT | 8A | 08 | 01 |
| Wrt SSCF xlate array | 22 | 08 | |
| Connect | AE | 08 | |
| Disconnect | A6 | 08 | |
| Read secondary interrupt | A5 | 08 | |
| Read SSCF xlate array | 21 | 08 | |
| Read SSCF status | A9 | 08 | |
| Open adapter (BOPA) | 03 | 09 | |
| Terminate adapter | 6B | 09 | |
| No-op | 07 | 09 | |
| Read BOPA BSTAT status | 91 | 09 | |
| Set BOPA BSTAT status | 92 | 09 | |
| Reset BOPA BSTAT status | 96 | 09 | |
| Read BOPA control byte | BD | 09 | |
| Write BOPA control byte | BA | 09 | |
| Read BOPA display | B5 | 09 | |
| Write BOPA display | B2 | 09 | |
| Diag rotate MD reg | 87 | 09 | |
| Write message to MD | 72 | 09 | |
| Read message from MD | 71 | 09 | |

| | | |
|---|---|---|
| (8) | COMPSTAT | Completion Status – Byte 2 of the FRB:<br>Bit 0 – Extended status indicator<br>Bit 1 – Reenter<br>Bit 2 – Reenter FRB indicator<br>Bit 3 – Reserved<br>Bit 4 – Complete<br>Bit 5 – Error<br>Bit 6 – Exception<br>Bit 7 – Attention<br>**Note:** *If bit 0 (ESI) equals 1, then Byte 4 of the FRWA (Extended Completion Status – field 28) has meaning.* |

| Field | | Meaning |
|---|---|---|
| (9) | ARC | Adapter Return Code – Byte 3 of the FRB.<br>**Note:** *The values in fields 8 and 9 represent the adapter status when it terminated its activity, either successfully or with error, and returned control to DPPX.* |
| (11) | DATA | Bytes 4–7 of the FRB. |
| (12) | RES | Reserved – Bytes 8, 9 of the FRB – not used |
| (13) | CNT | Count – Bytes 10, 11 of the FRB. |
| (14) | IOEP | I/O Interrupt Entry Point – Bytes 12–15 of the FRB. |
| (15) | ADWA | Adapter Work Area Address – Bytes 16–19 of the FRB |
| (16) | CA | Channel Address – Byte 24 of the FRB – not used |
| (17) | CPR | Channel Pointer Register – Byte 25 of the FRB – not used |
| (18) | FRWA | Function Request Work Area Address – Bytes 20–23 of the FRB. |
| (19) | RES | Reserved – Bytes 28–31 of the FRB – not used |
| (24) | | Reserved – Byte 0 of the FRWA |
| (25) | | Reserved – Byte 1 of the FRWA |
| (26) | | Reserved – Byte 2 of the FRWA |
| (27) | | Reserved – Byte 3 of the FRWA |
| (28) | | Byte 4 of the FRWA – extended completion status:<br>Bit 0 – Request Reject<br>Bit 1 – Error Record Indicator<br>Bit 2 – Program Request Interrupt<br>Bit 3 – Not used<br>Bit 4 – Not used<br>Bit 5 – Preemptive Request Complete<br>Bit 6 – Not used<br>Bit 7 – Reserved<br>**Note:** *Bit 1 is set whenever the FDM builds an error record in FRWA bytes 16–27 (fields 40–51).* |
| (29) | | Reserved – Byte 5 of the FRWA |
| (30)(31) | | Bytes 6, 7 of the FRWA – error record displacement (pointer to FRWA byte 16). |
| (32)–(35) | | Bytes 8–11 of the FRWA – not used |
| (36)(37) | | Bytes 12, 13 of the FRWA – residual count. |
| (38)(39) | | Reserved – Bytes 14, 15 of the FRWA |
| (40) | | Byte 16 of the FRWA – error record flags:<br>Bit 0 – Not used<br>Bit 1 – Not used<br>Bit 2 – Partial Log<br>Bit 3 – Not used<br>Bit 4 – Not used |

| Field | | Meaning |
|---|---|---|
| | | Bit 5 – Not used<br>Bit 6 – Not used<br>Bit 7 – Not used |
| (41) | | Byte 17 of the FRWA – retry count of failing operation. |
| (42) | | Byte 18 of the FRWA – not used |
| (43) | | Byte 19 of the FRWA – not used |
| (44)(45) | | FRWA Bytes 20, 21 – PSCF EIR<br>Byte 20:<br>Bit 0 – Not used<br>Bit 1 – BOP/PSCF Priority Level Control<br>Bit 2 – Not used<br>Bit 3 – Not used<br>Bit 4 – I/O Read Check<br>Bit 5 – Not used<br>Bit 6 – 1 = SSCF Installed<br>Bit 7 – Not used<br>Byte 21:<br>Bit 0 – 100-ms Clocked Interrupt Overrun<br>Bit 1 – I/O Write Check<br>Bit 2 – Reserved<br>Bit 3 – SSCF Equipment Check<br>Bit 4 – Not used<br>Bit 5 – PSCF Address 0C Equipment Check<br>Bit 6 – Not used<br>Bit 7 – Not used |
| (46)(47) | | FRWA Bytes 22, 23 – PSCF Basic Status Register<br>Byte 22:<br>Bit 0 – Not used<br>Bit 1 – IPL Register Valid<br>Bit 2 – Not used<br>Bit 3 – Power-On Reset<br>Bit 4 – Not used<br>Bit 5 – Not used<br>Bit 6 – Not used<br>Bit 7 – Not used |

| Field | | Meaning |
|---|---|---|
| | | Byte 23:<br>Bit 0 – 100-ms Clocked Interrupt<br>Bit 1 – 100-msec Clock Enabled<br>Bit 2 – Not used<br>Bit 3 – SSCF Power Outage<br>Bit 4 – Reserved<br>Bit 5 – Equipment Check<br>Bit 6 – Enable Interruption<br>Bit 7 – Interruption Request |
| (48)(49) | | FRWA Bytes 24, 25 – BOPA Basic Status<br>Byte 24:<br>Bit 0 – Invalid Command<br>Bit 1 – MD Signal Bus Check<br>Bit 2 – BOPA Write Check<br>Bit 3 – BOPA Read Check<br>Bit 4 – MD Enabled<br>Bit 5 – Reserved<br>Bit 6 – IPL/Keylock Encode<br>Bit 7 – IPL/Keylock Encode<br>Byte 25:<br>Bit 0 – Enter Data pushbutton<br>Bit 1 – Enter Function pushbutton<br>Bit 2 – MD Transfer Complete<br>Bit 3 – MD Status In<br>Bit 4 – Any IPL<br>Bit 5 – Machine Check<br>Bit 6 – Enable BOPA Interruption<br>Bit 7 – BOPA Interruption Request |

| Field | | Meaning |
|---|---|---|
| (50)(51) | | FRWA Bytes 26, 27 — SSCF basic status.<br>Byte 26:<br>Bit 0 — I/O Unit Enabled<br>Bit 1 — Not used<br>Bit 2 — SSCF-Detected Error<br>Bit 3 — SSCF Enabled<br>Bit 4 — Not used<br>Bit 5 — Not used<br>Bit 6 — Not used<br>Bit 7 — Not used<br>Byte 27:<br>Bit 0 — Not used<br>Bit 1 — Not used<br>Bit 2 — Not used<br>Bit 3 — Not used<br>Bit 4 — Not used<br>Bit 5 — Not used<br>Bit 6 — Not used<br>Bit 7 — Not used<br>SSCF basic status is only valid for machine checks during connect, disconnect, read/write translate array, and read SSCF status requests. |

### *SC332 DPCX Condition/Incident Log Formats and Meanings*

The DPCX Condition/Incident Log stores three types of record formats for system control facility failures:

**DPCX Type 1 Record Format**

| (1) | | (2) | (3) | (4) | (5) |
|---|---|---|---|---|---|
| 1-TYPE | 1-REC | SEQ-XXXX | NA-XX | PA-XX | LA-XX |

| (6) | (7) | (8) |
|---|---|---|
| C-CODE-XX | B-STAT-XX | C-FR-XX |

| (9) | (10) | (11) |
|---|---|---|
| X-STAT1-XX | X-STAT2-00 | S-FR-XX |

| (12) | (13) |
|---|---|
| 10CB-XXYY 00ZZ | RC-XX |

| (15) | (16) | (17) | (18) |
|---|---|---|---|
| D1-XXXX | D2-XXXX | D3-XXXX | D4-XXXX |

**DPCX Type 2 Record Format**

| (1) | | (2) | (3) | (4) | (5) |
|---|---|---|---|---|---|
| 2-TYPE | I-REC | SEQ-XXXX | NA-XX | PA-XX | LA-XX |

| (19) | | (20) | (8) |
|---|---|---|---|
| D21-XXXX | XXXX | LVL-XX | C-FR-XX |

| (21) | | (22) | (11) |
|---|---|---|---|
| D22-XXXX | XXXX | MC-XX | S-FR-XX |

| (23) | (24) | (25) |
|---|---|---|
| D23-XXXX | D24-XXXX | D25-XXXX |

**DPCX Type 4 Record Format**

| (1) | | (2) | (26) |
|---|---|---|---|
| 4-TYPE | I-REC | SEQ-XXXX | SYS-COND-XX |

| (27) | (28) | (29) | (30) | (31) |
|---|---|---|---|---|
| D01-XX | D02-XX | D03-XX | D04-XX | D05-XX |

**DPCX Types 1, 2, and 4 Condition/Incident Log Record Contents**

| Field | | Contents |
|---|---|---|
| (1) | X-TYPE | Indicates the record type (1, 2, or 4). |
| (2) | SEQ | A four-digit decimal number (0001—4095). This number identifies the relative time the incident occurred. |
| (3) | NA | A two-digit number indicating the number of active applications at the time of the error. |
| (4) | PA | A two-digit number indicating the physical address of the PSCF (see SC112). |
| (5) | LA | A two-digit number indicating the logical unit address (same as PA). |
| (6) | C-CODE | Completion code — A two-digit hex number indicating operation completion status. |
| (7) | B-STAT | PSCF Basic Status Register bits 8—15. See SC233 for bit definition. |
| (8) | C-FR | A two-digit hex number indicating operation when the error occurred. |
| (9) | X-STAT1 | PSCF EIR bits 0—7. See SC233 for bit definition. |
| (10) | X-STAT2 | PSCF EIR bits 8—15. See SC233 for bit definition. |
| (11) | S-FR | A two-digit hex number indicating system operation when the error occurred. |
| (26) | SYS-COND | A system condition code that identifies the system event being recorded. |

**Note:** *Presently, DPCX does not use fields 12-25 and 27-31 for SCF incidents.*

## SC340 How to Use the Error Log for Fault Isolation

The procedure for examining the error log depends upon whether the customer is using DPPX or DPCX. For DPPX, see SC341; for DPCX, see SC342.

### *SC341 Using the DPPX Error Log Record for Fault Isolation*

The log records should be examined for the failing area of the SCF. The physical address indicates the failing PSCF or SSCF (08 or P8 respectively).

Obtain the basic status information from the extended data field D11, D12, and the high order of D14. Convert the hex number to binary (see Appendix A) and see SC331 for field meaning.

### *SC342 Using the DPCX Condition/Incident Log for Fault Isolation*

Examine the log records for the failing area of the SCF. The PA indicates the failing PSCF or SSCF (08 or P8 respectively).

- If any Type 2 format records are found, use the Machine Check Action Plan (SC351) to initiate a repair action.
- If no Type 2 records are found, examine the Type 1 format records to determine the type of SCF failure.

Obtain the B-STAT value (field 7) from the Type 1 record and convert the hex number to binary (see Appendix A). If the B-STAT contains either an active 0 or 5 bit, use the Machine Check Action Plan (SC351) to initiate a repair action. Use Figures SC342-1, 2, and 3 to further define the error.

| B-STAT Bits | PSCF Basic Status Register Bits | Description |
|---|---|---|
| *0 | 8 | 100-ms clocked interrupt |
| 1 | 9 | 100-ms clock enabled |
| 2 | 10 | Not used |
| *3 | 11 | SSCF power outage |
| 4 | 12 | Reserved |
| 5 | 13 | PSCF equipment check |
| 6 | 14 | PSCF interruption enabled |
| 7 | 15 | PSCF interruption request |

*Turns on B-STAT bit 7.

**Figure SC342-1. Type 1 Record B-STAT Field Error Description**

| X-STAT1 Bits | PSCF EIR Bits | Description |
|---|---|---|
| 0 | 0 | Not used |
| 1 | 1 | BOP/PSCF priority level control |
| 2 | 2 | Not used |
| 3 | 3 | Not used |
| 4 | 4 | I/O read check |
| 5 | 5 | Not used |
| 6 | 6 | SSCF installed |
| 7 | 7 | Not used |

**Note:** *For more information concerning the errors contained in this figure, obtain the X-STAT1 and X-STAT2 fields from the Type 1 error record.*

**Figure SC342-2. Type 1 Record X-STAT1 Field Error Description**

| X-STAT2 Bits | PSCF EIR Bits | Description |
|---|---|---|
| 0 | 8 | 100-ms clocked interrupt overrun |
| 1 | 9 | I/O write check |
| 2 | 10 | Reserved |
| 3 | 11 | SSCF equipment check |
| 4 | 12 | Not used |
| 5 | 13 | PSCF addr 0C equipment check |
| 6 | 14 | Not used |
| 7 | 15 | Not used |

**Figure SC342-3. Type 1 Record X-STAT2 Field Error Description**

## SC350 Action Plan to Correct Intermittent Failures

Intermittent failures can most easily be determined by using the error log. To determine the type of failure recorded in the error log, refer to How to Use Error Log for Fault Isolation (SC340), which then refers you to the correct action plan.

### *SC351 Machine Check Action Plan*

Use this action plan for the following conditions:

- DPCX Type 2 log format errors — The processor logic detected an SCF hardware operational error, such as a parity error.
- DPCX Type 1 log format errors — The SCF detected a hardware error in the SCF logic.
- DPPX Type 5 log errors — A hardware failure occurred in the adapter bus logic during an SCF operation.

**Caution: Turn power off when removing or exchanging cards or cables.**

Troubleshoot this failure in the following sequence:

| Probable Cause | Action | Comment |
|---|---|---|
| 1. Incorrect voltage | Measure board voltages at 8130/8140 01A-A1 and 01A-A2 boards and also at the board of the failing SSCF.<br>a. D03 = +4.5 to +5.5 V dc<br>b. B11 = +7.7 to +9.3 V dc<br>c. B06 = −4.5 to −5.5 V dc | Missing or out-of-tolerance voltages; go to PA MAP. |
| 2. Loose or defective SCF control cables | Inspect for loose or defective cables (see SC111). | See Note 1 below. |
| 3. Defective SCF cards | Exchange, in order, the SC5, SC4, SC2, SC3, SC1, and SC6 cards. See the following chart for locations. | See Notes 1, 2, and 3 below. If this is an 8130 without the System Expansion Feature, only the SC1 card can be exchanged. If this is an 8140, there is no SC6 card. |

| Mach Type | SC5 | SC4 | SC2 | SC3 | SC1 | SC6 | 2nd SC5 |
|---|---|---|---|---|---|---|---|
| 8130 | A2C2 | A2D2 | A2F2 | A2E2 | A2G2 | A2B2 | |
| 8140A | A2D2 | A2C2 | A2A2 | A2B2 | A1A2 | | |
| 8140B | A2A2 | A1A2 | A1C2 | A1B2 | A1D2 | | C2A2 |

**Notes:**

1. To verify the fix, run the SC tests using the Free-Lance Utility. At 80BC, enter 08A; at 81BC, enter 1B (see SC211).
   a. If the tests fail, record the test error message and use the SC MAP menu option 4 to find the failure.
   b. If the tests complete successfully (P800), return the system to the customer. Obtain a new error log after the customer has used the system.
   c. If the log indicates a failure pertaining to this action plan, go to the next step in the table.
   d. End repair action when there are no SC failures indicated in the log.
2. If the system still fails after exchanging cards, reinstall the original cards and go to the next step in the table.
3. If the system still fails after exchanging the FRU and this is the last step in the action plan, go to SC250 and use the SCF Bus Error action plan (Action Plan 8).

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## *SC401 SCF General Data Flow*

Figures SC401-1 through SC401-4 show SCF general data flow in the processors. Figure SC401-1 depicts the 8130 without the expansion feature; Figure SC401-2 shows the 8130 with the expansion feature; Figure SC401-3 shows the 8140A; and Figure SC401-4 shows the 8140B.

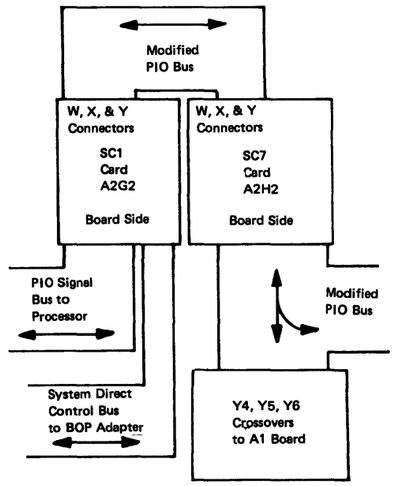



**Figure SC401-1. 8130 Hardware SCF Data Flow (without Expansion Feature)**

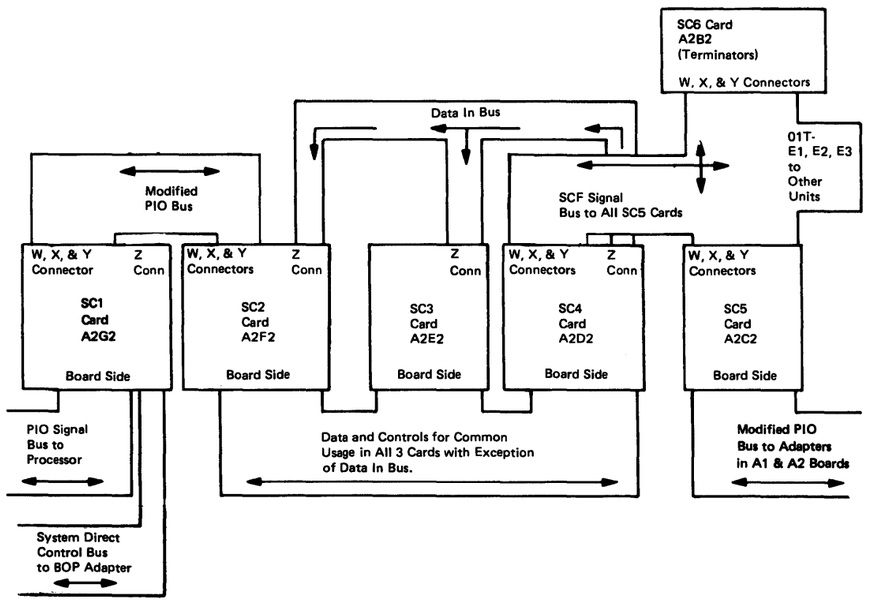



**Figure SC401-2. 8130 Hardware SCF Data Flow (with Expansion Feature)**

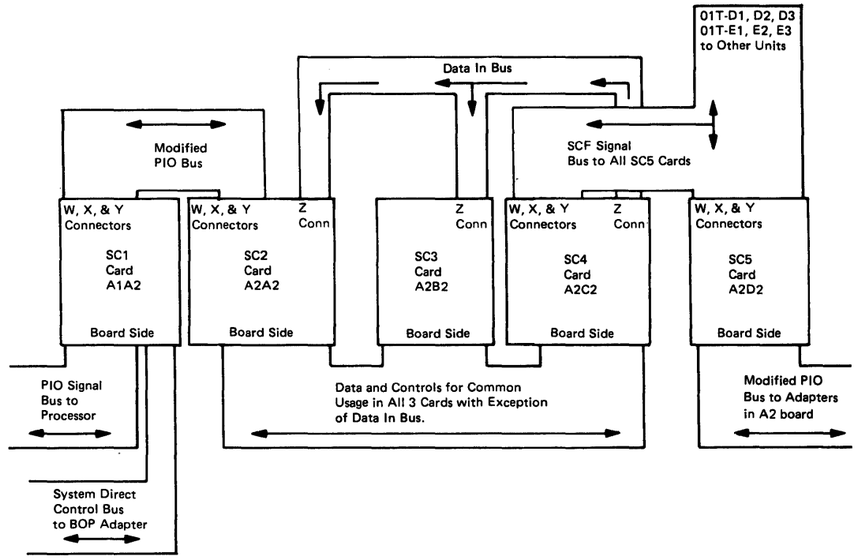



**Figure SC401-3. 8140 Model A Hardware SCF Data Flow**

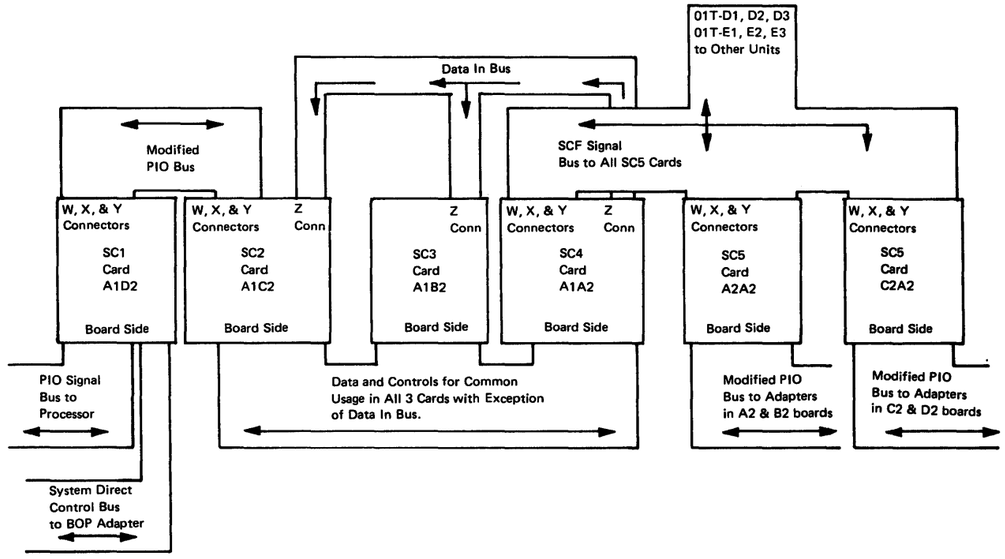



**Figure SC401-4. 8140 Model B Hardware SCF Data Flow**

## SC410 SCF Point-to-Point Net Listing

This section lists the point-to-point signal path for the SCF cards. It also lists the board wiring from the PSCF or SSCF card to the individual adapters.

### *SC411 8130 SCF Point-to-Point Net Listing*

**8130 Without Expansion Feature, I/O Bus to Adapters**

| | A2 Board | | A1 Board | | | A2 Board | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Communications Adapters | | | | | |
| Line Name | SCF Card A2G2 | Board Y4, Y5 & Y6 | Board Z4, Z5 & Z6 | Diskette DA A1S2 | File FA A1U2 | CA1 A2J4 A2K2 | CA2 A2J2 A2L2 | CA3 A2N4 A2M2 | CA4 A2Q4 A2P2 | CA5 A2S4 A2R2 | CA6 A2U4 A2T2 |
| –PIO Data 0 | W22 | T1C13 | L6D04 | G04 | S04 | K2G02 | L2G02 | M2G02 | P2G02 | P2G02 | T2G02 |
| –PIO Data 1 | W28 | T1E11 | M6E04 | D13 | U11 | K2J02 | L2J02 | M2J02 | P2J02 | R2J02 | T2J02 |
| –PIO Data 2 | W11 | T1D13 | N6C02 | J02 | S07 | K2D10 | L2D10 | M2D10 | P2D10 | R2D10 | T2D10 |
| –PIO Data 3 | W24 | U1C13 | M6A04 | G02 | U05 | K2G08 | L2G08 | M2G08 | P2G08 | R2G08 | T2G08 |
| –PIO Data 4 | W04 | U1B13 | M6A02 | J06 | U10 | K2J04 | L2J04 | M2J04 | P2J04 | R2J04 | T2J04 |
| –PIO Data 5 | W25 | T1C11 | M6B04 | G07 | S13 | K2D09 | L2D09 | M2D09 | P2D09 | R2D09 | T2D09 |
| –PIO Data 6 | W07 | T1D11 | M6D02 | G08 | S08 | K2B09 | L2B09 | M2B09 | P2B09 | R2B09 | T2B09 |
| –PIO Data 7 | W06 | U1A13 | M6C02 | G03 | M10 | K2D06 | L2D06 | M2D06 | P2D06 | R2D06 | T2D06 |
| –PIO Data P0 | W27 | U1A11 | M6D04 | B12 | P10 | K2B02 | L2B02 | M2B02 | P2B02 | R2B02 | T2B02 |
| –PIO Data 8 | W05 | M1B11 | M6B02 | D12 | S09 | | | | | | |
| –PIO Data 9 | W30 | N1B13 | M6B04 | J04 | S10 | | | | | | |
| –PIO Data 10 | W13 | N1E11 | N6B02 | G09 | U02 | | | | | | |
| –PIO Data 11 | W09 | N1A11 | N6A02 | J07 | S05 | | | | | | |
| –PIO Data 12 | W29 | N1A13 | N6A04 | D10 | B12 | | | | | | |
| | | | | M08 | U13 | | | | | | |
| –PIO Data 13 | W10 | N1B11 | N6B02 | J09 | U04 | | | | | | |
| –PIO Data 14 | W23 | L1E13 | L6E04 | G05 | U07 | | | | | | |
| –PIO Data 15 | W32 | N1D13 | N6D04 | J05 | S12 | | | | | | |
| –PIO Data P1 | W33 | N1E13 | N6B04 | B10 | U12 | | | | | | |
| –TD Tag | X22 | P1E13 | P6E04 | U05 | P02 | K2B05 | L2B05 | M2B05 | P2B05 | R2B05 | T2B05 |
| –I/O Tag | X05 | Q1C11 | Q6C02 | S09 | D13 | | | | | | |
| –I/O Tag (B) | X06 | Q1D11 | Q6D02 | | | K2B05 | L2B04 | M2B05 | P2B05 | R2B04 | T2B04 |
| –Halt | X09 | R1B11 | R6B02 | P02 | J04 | K2G04 | L2G04 | M2G04 | P2G04 | R2G04 | T2G04 |
| –TA Tag | X30 | R1C13 | R6C04 | U06 | M08 | K2D05 | L2D05 | M2D05 | P2D05 | R2D05 | T2D05 |
| –TC Tag | X10 | R1C11 | R6C02 | S05 | | K2B08 | L2B08 | M2B08 | P2B08 | R2B08 | T2B08 |
| –Byte Tag | X11 | R1D11 | R6D02 | | | | | | | | |

| | A2 Board | | A1 Board | | | A2 Board | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Communications Adapters | | | | | |
| Line Name | SCF Card A2G2 | Board Y4, Y5 & Y6 | Board Z4, Z5 & Z6 | Diskette DA A1S2 | File FA A1U2 | CA1 A2J4 A2K2 | CA2 A2J2 A2L2 | CA3 A2N4 A2M2 | CA4 A2Q4 A2P2 | CA5 A2S4 A2R2 | CA6 A2U4 A2T2 |
| –Valid HW | X02 | P1E11 | P6E02 | | G02 | | | | | | |
| –Exception | X23 | Q1A13 | Q6A04 | W07 | | | | | | | |
| –Modifier | X24 | Q1B13 | Q6B04 | P13 | | | | | | | |
| –EOC | X04 | Q1B11 | Q6B02 | U13 | B08 | K2P11 | L2P11 | M2P11 | P2P11 | R2P11 | T2P11 |
| –PV | X25 | Q1C13 | Q6C04 | U11 | D05 | K2D07 | L2D07 | M2D07 | P2D07 | R2D07 | T2D07 |
| –VB1 (B) | X27 | Q1E13 | Q6E04 | | | K2G03 | L2G03 | M2G03 | P2G03 | R2G03 | T2G03 |
| –VB1 | X07 | Q3E11 | Q6ED2 | U02 | | | | | | | |
| –IRR (B) | X28 | R1A13 | R6A04 | | | K2D02 | L2D02 | M2D02 | P2D02 | R2D02 | T2D02 |
| –IRR | X29 | R1B13 | R6B04 | P10 | B09 | | | | | | |
| –VB0 | X32 | R1E13 | R6E04 | | | | | | | | |
| –I/O Reset | Y13 | V1B11 | V6B02 | S03 | T2G09 M05 | X2J05 | L2J05 | M2J05 | P2J05 | R2J05 | T2J05 |
| –Release | Y09 | U1C11 | U6C02 | S02 | T2J13 | | | | | | |
| –IPR | Y30 | U1D13 | U6D04 | | | | | | | | |
| –Ch Reg Hi | X33 | S1A13 | S6A04 | | | X2M13 | L2M13 | M2M13 | P2M13 | R2M13 | T2M13 |
| –Ch Reg Med | X33 | U1D11 | U6D02 | | | | | | | | |
| –Ch Reg Lo | X13 | S1A11 | S6A02 | M05 | J02 | | | | | | |
| –CH Grant Hi | X12 | R1E11 | R6E02 | | | K2P05 | L2P05 | M2P05 | P2P05 | R2P05 | T2P05 |
| | | | | | | K2P04 | L2P04 | M2P04 | P2P04 | R2P04 | T2P04 |
| –CH Grant Med | | T1B13 | T6B04 | | | | | | | | |
| –CH Grant Lo | Y02 | T1A11 | T6A02 | U10 | G03 | | | | | | |
| –IR/B1 0 | Y24 | T1C13 | T6C04 | | | K2G09 | L2G09 | M2G09 | P2G09 | R2G09 | T2G09 |
| –IR/B1 1 | Y06 | T1E11 | T6E02 | | | K2J06 | L2J06 | M2J06 | P2J06 | R2J06 | T2J06 |
| –IR/B1 2 | Y25 | T1D13 | T6D04 | | | K2G07 | L2G07 | M2G07 | P1G07 | R2G07 | T2G07 |
| –IR/B1 3 | Y29 | U1C13 | U6C04 | | | K2B07 | L2B07 | M2B07 | P2B07 | R2B07 | T2B07 |
| | | | | | | K2J07 | L2J07 | M2J07 | P2J07 | R2J07 | T2J07 |
| –IR/B1 4 | Y28 | U1B13 | U6B04 | | | K2G10 | L2G10 | M2G10 | P2G10 | R2G10 | T2G10 |
| –IR/B1 5 | Y04 | T1C11 | T6C02 | | | K2J10 | L2J10 | M1J10 | P2J10 | R2J10 | T2J10 |
| –IR/B1 6 | Y05 | T1D11 | T6D02 | | | K2J11 | L2J11 | M2J11 | P2J11 | R2J11 | T2J11 |
| –IR/B1 7 | Y27 | U1A13 | U6A04 | | | K2J12 | L2J12 | M2J12 | P2J12 | R2J12 | T2J12 |
| –IR/B1 P | Y07 | U1A11 | U6A02 | | | K2G12 | L2G12 | M2G12 | P2G12 | R2G12 | T2G12 |
| +VE (POR) | Y22 | | | P05 | | J4D11 | J2D11 | M4D11 | Q4D11 | S4D11 | U4D11 |
| –10MHZ | Y33 | | | | | | | | | | |

## 8130 With Expansion Feature, I/O Bus to Adapters

| Line Name | A2 Board SSCF Card A2C2 | A2 Board Board Y4, Y5 & Y6 | A1 Board Board Z4, Z5 & Z6 | A1 Board Diskette DA A1S2 | A1 Board File FA A1U2 | A2 Board Communications Adapters CA1 A2J4 A2K2 | CA2 A2J2 A2L2 | CA3 A2N4 A2M2 | CA4 A2Q4 A2P2 | CA5 A2S4 A2R2 | CA6 A2U4 A2T2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| –PIO Data 0 | B02 | T1C13 | L6D04 | G04 | S04 | K2G02 | L2G02 | M2G02 | P2G02 | R2G02 | T2G02 |
| –PIO Data 1 | B08 | T1E11 | M6E04 | D13 | U11 | K2J02 | L2J02 | M2J02 | P2J02 | R2J02 | T2J02 |
| –PIO Data 2 | D11 | T1D13 | N6C02 | J02 | S07 | K2D10 | L2D10 | M2D10 | P2D10 | R2D10 | T2D10 |
| –PIO Data 3 | G04 | U1C13 | M6A04 | G02 | U05 | K2G08 | L2G08 | M2G08 | P2G08 | R2G08 | T2G08 |
| –PIO Data 4 | J07 | U1B13 | M6A02 | J06 | U10 | K2J04 | L2J04 | M2J04 | P2J04 | R2J04 | T2J04 |
| –PIO Data 5 | G09 | T1C11 | M6B04 | G07 | S13 | K2D09 | L2D09 | M2D09 | P2D09 | R2D09 | T2D09 |
| –PIO Data 6 | M02 | T1D11 | M6D02 | G08 | S08 | K2B09 | L2B09 | M2B09 | P2B09 | R2B09 | T2B09 |
| –PIO Data 7 | P10 | U1A13 | M6C02 | G03 | M10 | K2D06 | L2D06 | M2D06 | P2D06 | R2D06 | T2D06 |
| –PIO Data P0 | M12 | U1A11 | M6D04 | B12 | P10 | K2B02 | L2B02 | M2B02 | P2B02 | R2B02 | T2B02 |
| –PIO Data 8 | D05 | M1B11 | M6B02 | D12 | S09 | | | | | | |
| –PIO Data 9 | B10 | N1B13 | M6B04 | J04 | S10 | | | | | | |
| –PIO Data 10 | D13 | N1E11 | N6E02 | G09 | U02 | | | | | | |
| –PIO Data 11 | G05 | N1A11 | N6A02 | J07 | S05 | | | | | | |
| –PIO Data 12 | G08 | N1A13 | N6A04 | D10 | U13 | | | | | | |
| –PIO Data 13 | J09 | N1B11 | N6B02 | J09 | U04 | | | | | | |
| –PIO Data 14 | P06 | L1E13 | L6E04 | G05 | U07 | | | | | | |
| –PIO Data 15 | P11 | N1D13 | N6D04 | J05 | S12 | | | | | | |
| –PIO Data P1 | P13 | N1E13 | N6E04 | B10 | U12 | | | | | | |
| –TD Tag | G02 | P1E13 | P6E04 | U05 | P02 | K2B05 | L2B05 | M2B05 | P2B05 | R2B05 | T2B05 |
| –I/O Tag | J05 | Q1C11 | Q6C02 | S09 | D13 | | | | | | |
| –I/O Tag (B) | G13 | Q1D11 | Q6D02 | | | K2B05 | L2B04 | M2B05 | P2B05 | R2B04 | T2B04 |
| –Halt | J06 | R1B11 | R6B02 | P02 | J04 | K2G04 | L2G04 | M2G04 | P2G04 | R2G04 | T2G04 |
| –TA Tag | G10 | R1C13 | R6C04 | U06 | M08 | K2D05 | L2D05 | M2D05 | P2D05 | R2D05 | T2D05 |
| –TC Tag | J10 | R1C11 | R6C02 | S05 | | K2B08 | L2B08 | M2B08 | P2B08 | R2B08 | T2B08 |
| –Byte Tag | J11 | R1D11 | R6D02 | | | | | | | | |

| Line Name | A2 Board SSCF Card A2C2 | A2 Board Board Y4, Y5 & Y6 | A1 Board Board Z4, Z5 & Z6 | A1 Board Diskette DA A1S2 | A1 Board File FA A1U2 | A2 Board Communications Adapters CA1 A2J4 A2K2 | CA2 A2J2 A2L2 | CA3 A2N4 A2M2 | CA4 A2Q4 A2P2 | CA5 A2S4 A2R2 | CA6 A2U4 A2T2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| –Valid HW | D07 | P1E11 | P6E02 | | G02 | | | | | | |
| –Exception | D10 | Q1A13 | Q6A04 | W07 | | | | | | | |
| –Modifier | B12 | Q1B13 | Q6B04 | P13 | | | | | | | |
| –EOC | D09 | Q1B11 | Q6B02 | U13 | B08 | K2P11 | L2P11 | M2P11 | P2P11 | R2P11 | T2P11 |
| –PV | B04 | Q1C13 | Q6C04 | U11 | D05 | K2D07 | L2D07 | M2D07 | P2D07 | R2D07 | T2D07 |
| –VB1 (B) | J12 | Q1E13 | Q6E04 | | | K2G03 | L2G03 | M2G03 | P2G03 | R2G03 | T2G03 |
| –VB1 | D06 | Q1E11 | Q6E02 | U02 | | | | | | | |
| –IRR (B) | J13 | R1A13 | R6A04 | | | K2D02 | L2D02 | M2D02 | P2D02 | R2D02 | T2D02 |
| –IRR | B05 | R1B13 | R6B04 | P10 | B09 | | | | | | |
| –VB0 | B09 | R1E13 | R6E04 | | | | | | | | |
| –I/O Reset | G12 | V1B11 | V6B02 | S03 | T2G09 M05 | K2J05 | L2J05 | M2J05 | P2J05 | R2J05 | T2J05 |
| –Release | P09 | U1C11 | U6C02 | S02 | T2J13 | | | | | | |
| –IPR | M10 | U1D13 | U6D04 | | | | | | | | |
| –Ch Reg Hi | M05 | S1A13 | S6A04 | | | K2M13 | L2M13 | M2M13 | P2M13 | R2M13 | T2M13 |
| –Ch Reg Med | G03 | U1D11 | U6D02 | | | | | | | | |
| –Ch Reg Lo | J02 | S1A11 | S6A02 | M05 | J02 | | | | | | |
| –CH Grant Hi | M04 | R1E11 | R6E02 | | | K2P05 | L2P05 | M2P05 | P2P05 | R2P05 | T2P05 |
| | | | | | | K2P04 | L2P04 | M2P04 | P2P04 | R2P04 | T2P04 |
| –CH Grant Med | P12 | T1B13 | T6B04 | | | | | | | | |
| –CH Grant Lo | P02 | T1A11 | T6A02 | U10 | G03 | | | | | | |
| –IR/B1 0 | D02 | T1C13 | T6C04 | | B12 | K2G09 | L2G09 | M2G09 | P2G09 | R2G09 | T2G09 |
| –IR/B1 1 | D04 | T1E11 | T6E02 | | | K2J06 | L2J06 | M2J06 | P2J06 | R2J06 | T2J06 |
| –IR/B1 2 | B07 | T1D13 | T6D04 | | | K2G07 | L2G07 | M2G07 | P1G07 | R2G07 | T2G07 |
| –IR/B1 3 | J04 | U1C13 | U6C04 | | | K2B07 | L2B07 | M2B07 | P2B07 | R2B07 | T2B07 |
| | | | | | | K2J07 | L2J07 | M2J07 | P2J07 | R2J07 | T2J07 |
| –IR/B1 4 | G07 | U1B13 | U6B04 | | | K2G10 | L2G10 | M2G10 | P2G10 | R2G10 | T2G10 |
| –IR/B1 5 | P04 | T1C11 | T6C02 | | | K2J10 | L2J10 | M1J10 | P2J10 | R2J10 | T2J10 |
| –IR/B1 6 | P05 | T1D11 | T6D02 | | | K2J11 | L2J11 | M2J11 | P2J11 | R2J11 | T2J11 |
| –IR/B1 7 | M07 | U1A13 | U6A04 | M08 | | K2J12 | L2J12 | M2J12 | P2J12 | R2J12 | T2J12 |
| –IR/B1 P | P07 | U1A11 | U6A02 | | | K2G12 | L2G12 | M2G12 | P2G12 | R2G12 | T2G12 |
| +VE (POR) | B13 | | | P05 | | J4D11 | J2D11 | M4D11 | Q4D11 | S4D11 | U4D11 |
| –10MHZ | M13 | V1B13 | V6B04 | | | | | | | | |

8130 — SC2, SC3, and SC4 Signal Path

| Line Name | SC2 | SC3 | SC4 |
|---|---|---|---|
| +Parity Valid Lth | F2D04 | | D2D04 |
| +SSCF IR | F5D09 | | D5D09 |
| +SSCF Mck | F5D06 | | D5D06 |
| –SSCF Pwr Outage | | E4B03 | D4B03 |
| –Pwr Seq Comp | F5D04 | | D5D04 |
| –Cr to Card 2 | F3B13 | | D3B13 |
| +IPR to Card 2 | F4B08 | | D4B08 |
| –IRR to Card 2 | F2D05 | | D2D05 |
| +Exception Lth | F2B10 | | D2B10 |
| +X8 Tag Wrap | F4D07 | E4D07 | D4D07 |
| +08 Brdcst Cmd | | E2B04 | D2B04 |
| +0C Stat Cmd | F2B02 | E2B02 | |
| +08 Stat Cmd | F2B03 | E2B03 | |
| +X8 Crp Wrap | F4B09 | E4B09 | D4B09 |
| +Inward | F3D06 | E3D06 | D3D06 |
| +Pwr Outage Lth | F3B04 | E3B04 | |
| +Go | F3B02 | E3B02 | |
| +Enable Data Lths | F5B04 | E5B04 | |
| –10 Mhz | F5B02 | E5B03 | |
| –Parity Good | F4D10 | E4D10 | |
| +Load Chcw Reg | F4B02 | E4B02 | |
| +Valid Hw Lth | F2B07 | E2B07 | D2B07 |
| +Valid Byte 0 Lth | F2D09 | E2D09 | D2D09 |
| +Valid Byte 1 Lth | F2D06 | E2D06 | D2D06 |
| +Modifier Latch | F2D12 | E2D12 | D2D12 |
| –EOC DOT | F2B09 | E2B09 | D2B09 |
| –Data Out P0 | F4D12 | E4D12 | D4D12 |
| –Data Out 0 | F2D02 | E2D02 | D2D02 |
| –Data Out 1 | F2B08 | E2B08 | D2B08 |
| –Data Out 2 | F2D11 | E2D11 | D2D11 |
| –Data Out 3 | F3D04 | E3D04 | D3D04 |
| –Data Out 4 | F3B07 | E3B07 | D3B07 |
| –Data Out 5 | F3D09 | E3D09 | D3D09 |
| –Data Out 6 | F4D02 | E4D02 | D4D02 |
| –Data Out 7 | F4B10 | E4B10 | D4B10 |
| –Data Out P1 | F4B13 | | D4B13 |
| –Data Out 8 | F2B05 | E2B05 | D2B05 |
| –Data Out 9 | F2D10 | E2D10 | D2D10 |
| –Data Out 10 | F2B13 | E2B13 | D2B13 |
| –Data Out 11 | F3D05 | E3D05 | D3D05 |
| –Data Out 12 | F3B08 | E3B08 | D3B08 |
| –Data Out 13 | F3B09 | E3B09 | D3B09 |
| –Data Out 14 | F4D06 | E4D06 | D4D06 |
| –Data Out 15 | F4D11 | E4D11 | D4D11 |

| Line Name | SC2 | SC3 | SC4 |
|---|---|---|---|
| +I/O | F3B05 | E3B05 | D3B05 |
| +TA | F3D10 | E3D10 | D3D10 |
| +TC | F3B10 | E3B10 | D3B10 |
| +TD | F3D02 | E3D02 | D3D02 |
| +Ch Grant | F3B12 | E3B12 | D3B12 |
| +Any Tag | F4D05 | E4D05 | D4D05 |
| –Byte Tag | F3D11 | | D3D11 |
| –Halt | F4B07 | | D4B07 |
| –SC1 Reset/not I/O | F4B12 | E4B12 | |
| –SC1 Reset | F3D12 | E3D12 | |
| –SC5 Reset | F4D09 | E4D09 | D4D09 |
| –I/O Reset | F2B12 | | D2B12 |
| –Outbound Ctrl | F3D13 | E3D13 | D3D13 |
| –Xmit Ctrl | F2D13 | | D2D13 |
| –Int or MI Vhw | F3D07 | E3D07 | D3D07 |
| –Val Dly 150–200 | F4D04 | | D4D04 |
| –Val Dly 250–300 | F4B04 | | D4B04 |
| –Any Val Lth | F3D13 | E4D13 | D4D13 |
| +10 Mhz | F4B05 | E4B05 | D4B05 |
| +2 Hz Free Run | F3B03 | | D3B03 |
| –Pwr Seq Complete | F5D04 | | D5D04 |

*SC414 8140 SCF Point-to-Point Net Listing*

**8140 Model AXX – SC2, SC3, and SC4 Signal Path on A2 Board**

| Line Name | SC2 | SC3 | SC4 |
|---|---|---|---|
| +Parity Valid Lth | A2D04 | | C2D04 |
| +SSCF IR | A5D09 | | C5D09 |
| +SSCF Mck | A5D06 | | C5D06 |
| –SSCF Pwr Outage | | B4B03 | C4B03 |
| –Pwr Seq Comp | A5D04 | | C5D04 |
| –Cr to Card 2 | A3B13 | | C3B13 |
| +IPR to Card 2 | A4B08 | | C4B08 |
| –IRR to Card 2 | A2D05 | | C2D05 |
| +Exception Lth | A2B10 | | C2B10 |
| +X8 Tag Wrap | A4D07 | B4D07 | C4D07 |
| +08 Brdcst Cmd | | B2B04 | C2B04 |
| +0C Stat Cmd | A2B02 | B2B02 | |
| +08 Stat Cmd | A2B03 | B2B03 | |
| +X8 Crp Wrap | A4B09 | B4B09 | C4B09 |
| +Inward | A3D06 | B3D06 | C3D06 |
| +Pwr Outage Lth | A3B04 | B3B04 | |
| +Go | A3B02 | B3B02 | |
| +Enable Data Lths | A5B04 | B5B04 | |
| –10 Mhz | A5B02 | A5B03 | |
| –Parity Good | A4D10 | B4D10 | |
| +Load Chcw Reg | A4B02 | B4B02 | |
| +Valid Hw Lth | A2B07 | B2B07 | C2B07 |
| +Valid Byte 0 Lth | A2D09 | B2D09 | C2D09 |
| +Valid Byte 1 Lth | A2D06 | B2D06 | C2D06 |
| +Modifier Latch | A2D12 | B2D12 | C2D12 |
| –EOC DOT | A2B09 | B2B09 | C2B09 |
| –Data Out P0 | A4D12 | B4D12 | C4D12 |
| –Data Out 0 | A2D02 | B2D02 | C2D02 |
| –Data Out 1 | A2B08 | B2B08 | C2B08 |
| –Data Out 2 | A2D11 | B2D11 | C2D11 |
| –Data Out 3 | A3D04 | B3D04 | C3D04 |
| –Data Out 4 | A3B07 | B3B07 | C3B07 |
| –Data Out 5 | A3D09 | B3D09 | C3D09 |
| –Data Out 6 | A4D02 | B4D02 | C4D02 |
| –Data Out 7 | A4B10 | B4B10 | C4B10 |
| –Data Out P1 | A4B13 | | C4B13 |
| –Data Out 8 | A2B05 | B2B05 | C2B05 |
| –Data Out 9 | A2D10 | B2D10 | C2D10 |
| –Data Out 10 | A2B13 | B2B13 | C2B13 |
| –Data Out 11 | A3D05 | B3D05 | C3D05 |
| –Data Out 12 | A3B08 | B3B08 | C3B08 |
| –Data Out 13 | A3B09 | B3B09 | C3B09 |
| –Data Out 14 | A4D06 | B4D06 | C4D06 |
| –Data Out 15 | A4D11 | B4D11 | C4D11 |

| Line Name | SC2 | SC3 | SC4 |
|---|---|---|---|
| +I/O | A3B05 | B3B05 | C3B05 |
| +TA | A3D10 | B3D10 | C3D10 |
| +TC | A3B10 | B3B10 | C3B10 |
| +TD | A3D02 | B3D02 | C3D02 |
| +Ch Grant | A3B12 | B3B12 | C3B12 |
| +Any Tag | A4D05 | B4D05 | C4D05 |
| –Byte Tag | A3D11 | | C3D11 |
| –Halt | A4B07 | | C4B07 |
| –SC1 Reset/not I/O | A4B12 | B4B12 | |
| –SC1 Reset | A3D12 | B3D12 | |
| –SC5 Reset | A4D09 | B4D09 | C4D09 |
| –I/O Reset | A2B12 | | C2B12 |
| –Outbound Ctrl | A3D13 | B3D13 | C3D13 |
| –Xmit Ctrl | A2D13 | | C2D13 |
| –Int or MI Vhw | A3D07 | B3D07 | C3D07 |
| –Val Dly 150–200 | A4D04 | | C4D04 |
| –Val Dly 250–300 | A4B04 | | C4B04 |
| –Any Val Lth | A4D13 | B4D13 | C4D13 |
| +10 Mhz | A4B05 | B4B05 | C4B05 |
| +2 Hz Free Run | A3B03 | | C3B03 |
| –Pwr Seq Complete | A5D04 | | C5D04 |

## 8140 Models A3X and A4X Board Wiring — SC5 to 01A-A2 Board Adapters

| Line Name | SSCF (SC5) | CA Adapter | CA Adapter | CA Adapter | DA Diskette Adapter | FA Disk Adapter |
|---|---|---|---|---|---|---|
| —Valid Half Word | D2D07 | | | | | Q3B02 |
| —Parity Valid | D2B04 | E2D07 | G2D07 | J2D07 | M5D11 | Q2D05 |
| —End of Chain | D2D09 | L2B02 | L2B03 | L2B04 | M5D13 | Q2B08 |
| —IRR (HW) | D2B05 | | | | M4D10 | Q2B09 |
| —CR Low | D3D02 | | | | M4B05 | Q3D02 |
| —Exception | D2D10 | | | | M5D07 | |
| —Modifier | D2B12 | | | | M4D13 | |
| —Valid Byte 1 | D2D06 | | | | M5D02 | |
| —IR/BI P1 | D4D07 | E3B12 | G3B12 | J3B12 | | |
| —IR/BI 0 | D2D02 | E3B09 | G3B09 | J3B09 | | Q2B12 |
| —IR/BI 1 | D2D04 | E2B07 | | | | |
| | | E3D06 | G3D06 | J3D06 | | |
| —IR/BI 2 | D2B07 | E3B07 | G2B07 | | | |
| | | | G3B07 | J3B07 | | |
| —IR/BI 3 | D3D04 | E3D07 | G3D07 | J3D07 | | |
| | | | | J2D07 | | |
| —IR/BI 4 | D3B07 | E3B10 | G3B10 | J3B10 | | |
| —IR/BI 5 | D4D04 | E3D10 | G3D10 | J3D10 | | |
| —IR/BI 6 | D4D05 | E3D11 | G3D11 | J3D11 | | |
| —IR/BI 7 | D4B07 | E3D12 | G3D12 | J3D12 | M4B08 | |
| —Valid Byte 1 (Byte) | D3D12 | E3B03 | G3B03 | J3B03 | | |
| —IRR (Byte) | D3D13 | E2D02 | G2D02 | J2D02 | | |
| —Ch Req Med | D3B03 | L2B13 | L2B12 | L2B10 | Specials | |
| —Ch Req Hi | D4B05 | L2B09 | L2B08 | L2B07 | | |
| +5 Volts Ctrl | D5D05 | C5D03 | (just plain +5V) | | | |
| —DB PH | D4B12 | E2B02 | G2B02 | J2B02 | M2B12 | Q4D10 |
| —DB 0 | D2B02 | E3B02 | G3B02 | J3B02 | M3B04 | Q5B04 |
| —DB 1 | D2B08 | E3D02 | G3D02 | J3D02 | M2D13 | Q5D11 |
| —DB 2 | D2D11 | E2D10 | G2D10 | J2D10 | M3D02 | Q5B07 |
| —DB 3 | D3B04 | E3B08 | G3B08 | J3B08 | M3B02 | Q5D05 |
| —DB 4 | D3D07 | E3D04 | G3D04 | J3D04 | M3D06 | Q5D10 |
| —DB 5 | D3B09 | E2D09 | G2D09 | J2D09 | M3B07 | Q5B13 |

| Line Name | SSCF (SC5) | CA Adapter | CA Adapter | CA Adapter | DA Diskette Adapter | FA Disk Adapter |
|---|---|---|---|---|---|---|
| —DB 6 | D4B02 | E2B09 | G2B09 | J2B09 | M3B08 | Q5B08 |
| —DB 7 | D4D10 | E2D06 | G2D06 | J2D06 | M3B03 | Q4B10 |
| —DB PL | D4D13 | | | | M2B10 | Q5D12 |
| —DB 8 | D2D05 | | | | M2D12 | Q5B09 |
| —DB 9 | D2B10 | | | | M3D04 | Q5B10 |
| —DB 10 | D2D13 | | | | M3B09 | Q5D02 |
| —DB 11 | D3B05 | | | | M3D07 | Q5B05 |
| —DB 12 | D3B08 | | | | M2D10 | Q5D13 |
| —DB 13 | D3D09 | | | | M3D09 | Q5D04 |
| —DB 14 | D4D06 | | | | M3B05 | Q5D07 |
| —DB 15 | D4D11 | | | | M3D05 | Q5B12 |
| —TD | D3B02 | E2B05 | G2B05 | J2B05 | M5D05 | Q4D02 |
| | | | | | | P4B08 |
| —I/O Op | D3D05 | | | | M5B09 | Q2D13 |
| —Halt | D3D06 | E3B04 | G3B04 | J3B04 | M4D02 | Q3D04 |
| —TA | D3B10 | E2D05 | G2D05 | J2D05 | M5D06 | Q4B08 |
| —TC | D3D10 | E2B08 | G2B08 | J2B08 | M5B05 | |
| —System Reset | D3B12 | E3D05 | G3D05 | J3D05 | M5B03 | Q4B05 |
| —I/O Op (Byte) | D3B13 | E2B04 | G2B04 | J2B04 | | P3B09 |
| —Ch Grant Lo | D4D02 | | | | M5D10 | |
| —Ch Grant Hi (Special) | D4B04 | L3B04 | L3B07 | L3B08 | L3B09 | L3B10 |
| —Release | D4D09 | | | | M5B02 | P3D13 |
| —10 Mhz | D5B02—D5D02 | | | | | |
| —Gate Inf Drvrs On (VE) | C5D05 | | | | | |
| | D5B05 | H6B04 | H4D11 | | | |
| | | | F4D11 | | | |
| | | | F2D11 | | | |
| | | | H2D11 | | | |
| | | | K2D11 | | | |
| | | | P3B10 | | | |
| | | | M4D05 | | | |
| | | | Q4D05 | | | |
| | | | Q5D06 | | | |

**8140 Model A5X Board Wiring — SC5 to 01A-A2 Board Adapters**

| Line Name | SSCF (SC5) | DA Diskette Adapter | FA Disk Adapter |
|---|---|---|---|
| –Valid Half Word | D2D07 | | F3B02 |
| –Parity Valid | D2B04 | G5D11 | F2D05 |
| –End of Chain | D2D09 | G5D13 | F2B08 |
| –IRR (HW) | D2B05 | G4D10 | F2B09 |
| –CR Low | D3D02 | G4B05 | F3D02 |
| –Exception | D2D10 | G5D07 | |
| –Modifier | D2B12 | G4D13 | |
| –Valid Byte 1 | D2D06 | G5D02 | |
| –IR/BI P1 | D4D07 | | |
| –IR/BI 0 | D2D02 | | F2B12 |
| –IR/BI 1 | D2D04 | | |
| –IR/BI 2 | D2B07 | | |
| –IR/BI 3 | D3D04 | | |
| –IR/BI 4 | D3B07 | | |
| –IR/BI 5 | D4D04 | | |
| –IR/BI 6 | D4D05 | | |
| –IR/BI 7 | D4B07 | G4B08 | |
| –Valid Byte 1 (Byte) | D3D12 | | |
| –IRR (Byte) | D3D13 | | |
| –Ch Reg Med | D3B03 | | |
| –Ch Reg Hi | D4B05 | | |
| +5 Volts Ctrl | D5D05 | | |
| –DB PH | D4B12 | G2B12 | F4D10 |
| –DB 0 | D2B02 | G3B04 | F5B04 |
| –DB 1 | D2B08 | G2D13 | F5D11 |
| –DB 2 | D2D11 | G3D02 | F5B07 |
| –DB 3 | D3B04 | G3B02 | F5D05 |
| –DB 4 | D3D07 | G3D06 | F5D10 |
| –DB 5 | D3B09 | G3B07 | F5B13 |

| Line Name | SSCF (SC5) | DA Diskette Adapter | FA Disk Adapter |
|---|---|---|---|
| –DB 6 | D4B02 | G3B08 | F5B08 |
| –DB 7 | D4D10 | G3B03 | F4B10 |
| –DB PL | D4D13 | G2B10 | F5D12 |
| –DB 8 | D2D05 | G2D12 | F5B09 |
| –DB 9 | D2B10 | G3D04 | F5B10 |
| –DB 10 | D2D13 | G3B09 | F5D02 |
| –DB 11 | D3B05 | G3D07 | F5B05 |
| –DB 12 | D3B08 | G2D10 | F5D13 |
| –DB 13 | D3D09 | G3D09 | F5D04 |
| –DB 14 | D4D06 | G3B05 | F5D07 |
| –DB 15 | D4D11 | G3D05 | F5B12 |
| –TD | D3B02 | G5D05 | F4D02 |
| | | | E4B08 |
| –I/O Op | D3D05 | G5B09 | F2D13 |
| –Halt | D3D06 | G4D02 | F3D04 |
| –TA | D3B10 | G5D06 | G4B08 |
| –TC | D3D10 | G5B05 | |
| –System Reset | D3B12 | G5B03 | F4B05 |
| –I/O Op (Byte) | D3B13 | | E3B09 |
| –Ch Grant Lo | D4D02 | G5D10 | |
| –Ch Grant Hi (Special) | D4B04 | | |
| –Release | D4D09 | G5B02 | E3D13 |
| –10 MHz | D5B02–D5D02 | | |
| –Gate Inf Drvrs On (VE) | C5D05 | | |
| | D5B05 | E3B10 | |
| | | G4D05 | |
| | | F4D05 | |
| | | F5D06 | |

**8140 Model BXX – SC2, SC3, and SC4 Signal Path on A1 Board**

| Line Name | SC2 | SC3 | SC4 |
|---|---|---|---|
| +Parity Valid Lth | C2D04 | | A2D04 |
| +SSCF IR | C5D09 | | A5D09 |
| +SSCF Mck | C5D06 | | A5D06 |
| –SSCF Pwr Outage | | B4B03 | A4B03 |
| –Pwr Seq Comp | C5D04 | | A5D04 |
| –Cr to Card 2 | C3B13 | | A3B13 |
| +IPR to Card 2 | C4B08 | | A4B08 |
| –IRR to Card 2 | C2D05 | | A2D05 |
| +Exception Lth | C2B10 | | A2B10 |
| +X8 Tag Wrap | C4D07 | B4D07 | A4D07 |
| +08 Brdcst Cmd | | B2B04 | A2B04 |
| +0C Stat Cmd | C2B02 | B2B02 | |
| +08 Stat Cmd | C2B03 | B2B03 | |
| +X8 Crp Wrap | C4B09 | B4B09 | A4B09 |
| +Inward | C3D06 | B3D06 | A3D06 |
| +Pwr Outage Lth | C3B04 | B3B04 | |
| +Go | C3B02 | B3B02 | |
| +Enable Data Lths | C5B04 | B5B04 | |
| –10 Mhz | C5B02 | A5B03 | |
| –Parity Good | C4D10 | B4D10 | |
| +Load Chcw Reg | C4B02 | B4B02 | |
| +Valid Hw Lth | C2B07 | B2B07 | A2B07 |
| +Valid Byte 0 Lth | C2D09 | B2D09 | A2D09 |
| +Valid Byte 1 Lth | C2D06 | B2D06 | A2D06 |
| +Modifier Latch | C2D12 | B2D12 | A2D12 |
| –EOC DOT | C2B09 | B2B09 | A2B09 |
| –Data Out P0 | C4D12 | B4D12 | A4D12 |
| –Data Out 0 | C2D02 | B2D02 | A2D02 |
| –Data Out 1 | A2B08 | B2B08 | A2B08 |
| –Data Out 2 | C2D11 | B2D11 | A2D11 |
| –Data Out 3 | C3D04 | B3D04 | A3D04 |
| –Data Out 4 | C3B07 | B3B07 | A3B07 |
| –Data Out 5 | C3D09 | B3D09 | A3D09 |
| –Data Out 6 | C4D02 | B4D02 | A4D02 |
| –Data Out 7 | C4B10 | B4B10 | A4B10 |
| –Data Out P1 | C4B13 | | A4B13 |
| –Data out 8 | C2B05 | B2B05 | A2B05 |
| –Data Out 9 | C2D10 | B2D10 | A2D10 |
| –Data Out 10 | C2B13 | B2B13 | A2B13 |
| –Data Out 11 | C3D05 | B3D05 | A3D05 |
| –Data Out 12 | C3B08 | B3B08 | A3B08 |
| –Data Out 13 | C3B09 | B3D09 | A3B09 |
| –Data Out 14 | C4D06 | B4D06 | A4D06 |
| –Data Out 15 | C4D11 | B4D11 | A4D11 |

| Line Name | SC2 | SC3 | SC4 |
|---|---|---|---|
| +I/O | C3B05 | B3B05 | A3B05 |
| +TA | C3D10 | B3D10 | A3D10 |
| +TC | C3B10 | B3B10 | A3B10 |
| +TD | C3D02 | B3D02 | A3D02 |
| +Ch Grant | C3B12 | B3B12 | A3B12 |
| +Any Tag | C4D05 | B4D05 | A4D05 |
| –Byte Tag | C3D11 | | A3D11 |
| –Halt | C4B07 | | A4B07 |
| –SC1 Reset/not I/O | C4B12 | B4B12 | |
| –SC1Reset | C3D12 | B3D12 | |
| –SC5 Reset | C4D09 | B4D09 | A4D09 |
| –I/O Reset | C2B12 | | A2B12 |
| –Outbound Ctrl | C3D13 | B3D13 | A3D13 |
| –Xmit Ctrl | C2D13 | | A2D13 |
| –Int or MI Vhw | C3D07 | B3D07 | A3D07 |
| –Val Dly 150–200 | C4D04 | | A4D04 |
| –Val Dly 250–300 | C4B04 | | A4B04 |
| –Any Val Lth | C4D13 | B4D13 | A4D13 |
| +10 Mhz | C4B05 | B4B05 | A4B05 |
| +2 Hz Free Run | C3B03 | | A3B03 |
| –Pwr Seq Complete | C5D04 | | A5D04 |

## 8140 Model BXX Board Wiring — SC5 to 01A-A2 Communications Adapter Board

| Line Name | SC SSCF | CA Port 4 | CA Port 3 | CA Port 2 | CA Port 1 | To Board A-B2 |
|---|---|---|---|---|---|---|
| —IR/BI P1 | A4D07 | B3B12 | D3B12 | F3B12 | H3B12 | K4D07 |
| —IR/BI 0 | A2D02 | B3B09 | D3B09 | F3B09 | H2B07 | K2D02 |
| —IR/BI 1 | A2D04 | B3D06 | D3D06 | F2B07 | H3D06 | K2D04 |
| —IR/BI 2 | A2B07 | B3B07 | D2B07 | F3B07 | H3B07 | K2B07 |
| —IR/BI 3 | A3D04 | B2B07 | D3D07 | F3D07 | H3D07 | K3D04 |
| —IR/BI 4 | A3B07 | B3B10 | D3B10 | F3B10 | H3B10 | K3B07 |
| —IR/BI 5 | A4D04 | B3D10 | D3D10 | F3D10 | H3D10 | K4D04 |
| —IR/BI 6 | A4D05 | B3D11 | D3D11 | F3D11 | H3D11 | K4D05 |
| —IR/BI 7 | A4B07 | B3D12 | D3D12 | F3D12 | H3D12 | K4B07 |
| —Valid Byte 1 (Byte) | A3D12 | B3B03 | D3B03 | F3B03 | H3B03 | K3D12 |
| —Parity Valid | A2B04 | B2D07 | D2D07 | F2D07 | H2D07 | K2B04 |
| —IRR (Byte) | A3D13 | B2D02 | D2D02 | F2D02 | H2D02 | K3D13 |
| —Valid Byte 1 (HW) | A2D06 | | | | | K2D06 |
| —Valid HW | A2D07 | | | | | K2D07 |
| —Valid Byte 0 | A2B09 | | | | | K2B09 |
| —End of Chain | A2D09 | G4B10 | G4B09 | G4B08 | G4B07 | K2D09 |
| —Exception | A2D10 | | | | | K2D10 |
| —Modifier | A2B12 | | | | | K2B12 |
| —Ch Req Lo | A3D02 | | | | | K3D02 |
| —Ch Req Med** | A3B03 | G4B05 | G4B04 | G4B03 | G4B02 | K3B03 |
| —Ch Req Hi** | A4B05 | G4D13 | G4D11 | G4B13 | G4B12 | K4B05 |
| —IPR | A4B10 | | | | | K4B10 |
| —DB PH | A4B12 | B2B02 | D2B02 | F2B02 | H2B02 | K4B12 |
| —DB 0 | A2B02 | B3B02 | D3B02 | F3B02 | H3B02 | K2B02 |
| —DB 1 | A2B08 | B3D02 | D3D02 | F3D02 | H3D02 | K2B08 |
| —DB 2 | A2D11 | B2D10 | D2D10 | F2D10 | H2D10 | K2D11 |
| —DB 3 | A3B04 | B3B08 | D3B08 | F3B08 | H3B08 | K3B04 |
| —DB 4 | A3D07 | B3D04 | D3D04 | F3D04 | H3D04 | K3D07 |
| —DB 5 | A3B09 | B2D09 | D2D09 | F2D09 | H2D09 | K3B09 |
| —DB 6 | A4B02 | B2B09 | D2B09 | F2B09 | H2B09 | K4B02 |
| —DB 7 | A4D10 | B2D06 | D2D06 | F2D06 | H2D06 | K4D10 |
| —DB PL | A4D13 | | | | | K4D13 |
| —DB 8 | A2D05 | | | | | K2D05 |
| —DB 9 | A2B10 | | | | | K2B10 |
| —DB 10 | A2D13 | | | | | K2D13 |
| —DB 11 | A3B05 | | | | | K3B05 |
| —DB 12 | A3B08 | | | | | K3B08 |
| —DB 13 | A3D09 | | | | | K3D09 |
| —DB 14 | A4D06 | | | | | K4D06 |
| —DB 15 | A4D11 | | | | | K4D11 |
| +5 Ve | A2B13 | C2D11 | E2D11 | G2D11 | J2D11 | K2B13 |
| —TD Tag | A3B02 | B2B05 | D2B05 | F2B05 | H2B05 | K3B02 |
| —I/O Tag | A3D05 | | | | | K3D05 |
| —Halt Tag | A3D06 | B3B04 | D3B04 | F3B04 | H3B04 | K3D06 |
| —TA Tag | A3B10 | B2D05 | D2D05 | F2D05 | H2D05 | K3B10 |
| —TC Tag | A3D10 | B2D08 | D2B08 | F2B08 | H2B08 | K3D10 |
| —Byte Tag | A3D11 | | | | | K3D11 |
| —System Reset | A3B12 | B3D05 | D3D05 | F3D05 | H3D05 | K3B12 |

| Line Name | | SC SSCF | CA Port 4 | CA Port 3 | CA Port 2 | CA Port 1 | To Board A-B2 |
|---|---|---|---|---|---|---|---|
| —I/O Tag (Byte) | | A3B13 | B2B04 | D2B04 | F2B04 | H2B04 | K3B13 |
| —Ch Grant Lo | | A4D02 | | | | | K4D02 |
| —Ch Grant Hi | | A4B04 | | | | G5B03 | |
| —Ch Grant Pass | | | | | G5B07 | G5B04 | |
| —Ch Grant Pass | *** | | | G5B09 | G5B08 | | |
| —Ch Grant Pass | | | G5B12 | G5B10 | | | |
| —Ch Grant Pass | | | G5B13 | | | | K4B04 |
| —Ch Grant Med | | A4D12 | | | | G5D02 | |
| —Ch Grant Pass | | | | | G5D06 | G5D05 | |
| —Ch Grant Pass | | | | G5D10 | G5D07 | | |
| —Ch Grant Pass | | | G5D12 | G5D11 | | | |
| —Ch Grant Pass | | | G5D13 | | | | K4D12 |
| —Release | | A4D09 | | | | | K4D09 |
| —Release Request | | A4B08 | | | | | |

**Mutually exclusive.

***Illustrates Ch Grant (+) being passed through but not connected to any ports in the A1 board and sent to the B1 board by wiring.

## 8140 Model BXX Board Wiring — 01A-B2 Disk/Diskette Adapter Board

| Line Name | Lines From 01A-A2 | DA Diskette | 2nd FA Disk | 1st FA Disk |
|---|---|---|---|---|
| –Valid Byte | A2D06 | C5D02 | | |
| –Valid HW | A2D07 | | F3B02 | H3B02 |
| –Parity Valid | A2B04 | C5D11 | F2D05 | H2D05 |
| –End of Chain | A2D09 | C5D13 | F2B08 | H2B08 |
| –IRR | A2B05 | C4D10 | F2B09 | H2B09 |
| –Chan Reg Lo | A3D02 | C4B05 | F3D02 | H3D02 |
| –Modifier | A2B12 | C4D13 | | |
| –IR/BI 0 | | | | |
| –IR/BI 1 | | | | |
| –IR/BI 2 | | | | |
| –IR/BI 4 | A3B07 | | | H2B12 |
| –IR/BI 5 | A4D04 | | F2B12 | |
| –IR/BI 6 | | | | |
| –IR/BI 7 | A4B07 | C4B08 | | |
| –IR/BI P1 | | | | |
| –DB PH | A4B12 | C2B12 | F4D10 | H4D10 |
| –DB 0 | A2B02 | C3B04 | F5B04 | H5B04 |
| –DB 1 | A2B08 | C2D13 | F5D11 | H5D11 |
| –DB 2 | A2D11 | C2D02 | F5B07 | H5B07 |
| –DB 3 | A3B04 | C3B02 | F5D05 | H5D05 |
| –DB 4 | A3D07 | C3D06 | F5D10 | H5D10 |
| –DB 5 | A3B09 | C3B07 | F5B13 | H5B13 |
| –DB 6 | A4B02 | C3B08 | F5B08 | H5B08 |
| –DB 7 | A4D10 | C3B03 | F4B10 | H4B10 |
| –DB PL | A4D13 | C2B10 | F5D12 | H5D12 |
| –DB 8 | A2D05 | C2D12 | F5B09 | H5B09 |
| –DB 9 | A2B10 | C3D04 | F5B10 | H5B10 |
| –DB 10 | A2D13 | C3B09 | F5D02 | H5D02 |
| –DB 11 | A3B05 | C3D07 | F5B05 | H5B05 |
| –DB 12 | A3B08 | C2D10 | F5D13 | H5D13 |
| –DB 13 | A3D09 | C3D09 | F5D04 | H5D04 |
| –DB 14 | A4D06 | C3B05 | F5D07 | H5D07 |
| –DB 15 | A4D11 | C3D05 | H5B12 | H5B12 |
| +5 Ve | A2B13 | C4D05 | F4D05 | H4D05 |
| | | | F5D06 | H5D06 |
| –TD Tag | A3B02 | C5D05 | F4D02 | H4D02 |
| –I/O Tag | A3D05 | C5B09 | F2D13 | H2D13 |
| –Halt Tag | A3D06 | C4D02 | F3D04 | H3D04 |
| –TA Tag | A3B10 | C5D02 | F4B08 | H4B08 |
| –TC Tag | A3D10 | C5B05 | | |
| –Sys Reset | A3B12 | C5B03 | F4B05 | H4B05 |
| | | | G3B09 | J3B09 |
| –Release | A4D09 | C5B02 | G3D13 | J3D13 |
| –Ch Grant Lo | A4D02 | C5D10 | | |
| –Ch Grant Lo Pass | | C5B10 | | |
| –Ch Grant Lo Pass | | | F3B03 | H3B03 |

## 8140 Model BXX Board Wiring — SC5 to 01A-C2 or 01A-D2 Tape Adapter Boards

| Line Name | Cable or SC5 SSCF | TA Tape |
|---|---|---|
| –Valid Byte | A2D06 | G3D11 |
| –Valid HW | A2D07 | G3D02 |
| –Parity Valid | A2B04 | G3B03 |
| –End of Chain | A2D09 | G3D05 |
| –IRR | A2B05 | G3B08 |
| –Chan Req Lo | A3D02 | G3B10 |
| –Modifier | A2B12 | G5B13 |
| –IR/BI 0 | | |
| –IR/BI 1 | | |
| –IR/BI 2 | | |
| –IR/BI 3 | | |
| –IR/BI 4 | | |
| –IR/BI 5 | | |
| –IR/BI 6 | A4D05 | G3D10 |
| –IR/BI 7 | | |
| –IR/BI P1 | | |
| –DB PH | A4B12 | G4B04 |
| –DB 0 | A2B02 | G4B05 |
| –DB 1 | A2B08 | G4B03 |
| –DB 2 | A2D11 | G4D06 |
| –DB 3 | A3B04 | G4B09 |
| –DB 4 | A3D07 | G4B07 |
| –DB 5 | A3B09 | G4D11 |
| –DB 6 | A4B02 | G4D05 |
| –DB 7 | A4D10 | G4D12 |
| –DB PL | A4D13 | G4D09 |
| –DB 8 | A2D05 | G4D13 |
| –DB 9 | A2B10 | G4B12 |
| –DB 10 | A2D13 | G4B10 |
| –DB 11 | A3B05 | G4D10 |
| –DB 12 | A3B08 | G4B13 |
| –DB 13 | A3D09 | G4D04 |
| –DB 14 | A4D06 | G4B08 |
| –DB 15 | A4D11 | G4D07 |
| +5 Ve | A2B13 | H5B02 |
| –TD Tag | A3B02 | G3D09 |
| –I/O Tag | A3D05 | G2B12 |
| –Halt Tag | A3D06 | G3B09 |
| –TA Tag | A3B10 | G5B04 |
| –TC Tag | A3D10 | |
| –Sys Reset | A3B12 | G2B05 |
| –Release | A4D09 | H3D02 |
| –Ch Grant Lo | A4D02 | |
| –Ch Grant Lo Pass | | G3B07 |
| –Ch Grant Lo Pass | | G3D07 |

## 8140 Model BXX Board Wiring — SC5 to 01A-C2 or 01A-D2 Communications Adapter Board

| Line Name | SC SSCF | CA Port 8/12 | CA Port 7/11 | CA Port 6/10 | CA Port 5/9 | To Board A-D2 |
|---|---|---|---|---|---|---|
| —IR/BI P1 | A4D07 | B3B12 | D3B12 | F3B12 | H3B12 | K4D07 |
| —IR/BI 0 | A2D02 | B3B09 | D3B09 | F3B09 | H2B07* | K2D02 |
| —IR/BI 1 | A2D04 | B3D06 | D3D06 | F2B07* | H3D06 | K2D04 |
| —IR/BI 2 | A2B07 | B3B07 | D2B07* | F3B07 | H3B07 | K2B07 |
| —IR/BI 3 | A3D04 | B2B07* | D3D07 | F3D07 | H3D07 | K3D04 |
| —IR/BI 4 | A3B07 | B3B10 | D3B10 | F3B10 | H3B10* | K3B07 |
| —IR/BI 5 | A4D04 | B3D10 | D3D10 | F3D10* | H3D10 | K4D04 |
| —IR/BI 6 | A4D05 | B3D11 | D3D11* | F3D11 | H3D11 | K4D05 |
| —IR/BI 7 | A4B07 | B3D12* | D3D12 | F3D12 | H3D12 | K4B07 |
| —Valid Byte 1 (Byte) | A3D12 | B3B03 | D3B03 | F3B03 | H3B03 | K3D12 |
| —Parity Valid | A2B04 | B2D07 | D2D07 | F2D07 | H2D07 | K2B04 |
| —IRR (Byte) | A3D13 | B2D02 | D2D02 | F2D02 | H2D02 | K3D13 |
| —Valid Byte 1 (HW) | A2D06 | | | | | K2D06 |
| —Valid HW | A2D07 | | | | | K2D07 |
| —Valid Byte 0 | A2B09 | | | | | K2B09 |
| —End of Chain | A2D09 | G4B10 | G4B09 | G4B08 | G4B07 | K2D09 |
| —Exception | A2D10 | | | | | K2D10 |
| —Modifier | A2B12 | | | | | K2B12 |
| —Ch Req Lo | A3D02 | | | | | K3D02 |
| —Ch Req Med** | A3B03 | G4B05 | G4B04 | G4B03 | G4B02 | K3B03 |
| —Ch Req Hi** | A4B05 | G4D13 | G4D11 | G4B13 | G4B12 | K4B05 |
| —IPR | A4B10 | | | | | K4B10 |
| —DB PH | A4B12 | B2B02 | D2B02 | F2B02 | H2B02 | K4B12 |
| —DB 0 | A2B02 | B3B02 | D3B02 | F3B02 | H3B02 | K2B02 |
| —DB 1 | A2B08 | B3D02 | D3D02 | F3D02 | H3D02 | K2B08 |
| —DB 2 | A2D11 | B2D10 | D2D10 | F2D10 | H2D10 | K2D11 |
| —DB 3 | A3B04 | B3B08 | D3B08 | F3B08 | H3B08 | K3B04 |
| —DB 4 | A3D07 | B3D04 | D3D04 | F3D04 | H3D04 | K3D07 |
| —DB 5 | A3B09 | B2D09 | D2D09 | F2D09 | H2D09 | K3B09 |
| —DB 6 | A4B02 | B2B09 | D2B09 | F2B09 | H2B09 | K4B02 |
| —DB 7 | A4D10 | B2D06 | D2D06 | F2D06 | H2D06 | K4D10 |
| —DB PL | A4D13 | | | | | K4D13 |
| —DB 8 | A2D05 | | | | | K2D05 |
| —DB 9 | A2B10 | | | | | K2B10 |
| —DB 10 | A2D13 | | | | | K2D13 |
| —DB 11 | A3B05 | | | | | K3B05 |
| —DB 12 | A3B08 | | | | | K3B08 |
| —DB 13 | A3D09 | | | | | K3D09 |
| —DB 14 | A4D06 | | | | | K4D06 |
| —DB 15 | A4D11 | | | | | K4D11 |
| +5 Ve | A2B13 | C2D11 | E2D11 | G2D11 | J2D11 | K2B13 |
| —TD Tag | A3B02 | B2B05 | D2B05 | F2B05 | H2B05 | K3B02 |
| —I/O Tag | A3D05 | | | | | K3D05 |
| —Halt Tag | A3D06 | B3B04 | D3B04 | F3B04 | H3B04 | K3D06 |
| —TA Tag | A3B10 | B2D05 | D2D05 | F2D05 | H2D05 | K3B10 |
| —TC Tag | A3D10 | B2D08 | D2B08 | F2B08 | H2B08 | K3D10 |
| —Byte Tag | A3D11 | | | | | K3D11 |
| —System Reset | A3B12 | B3D05 | D3D05 | F3D05 | H3D05 | K3B12 |

| Line Name | SC SSCF | CA Port 4 | CA Port 3 | CA Port 2 | CA Port 1 | To Board A-D2 |
|---|---|---|---|---|---|---|
| —I/O Tag (Byte) | A3B13 | B2B04 | D2B04 | F2B04 | H2B04 | K3B13 |
| —Ch Grant Lo | A4D02 | | | | | K4D02 |
| —Ch Grant Hi | A4B04 | | | | G5B03 | |
| —Ch Grant Pass | | | | G5B07 | G5B04 | |
| —Ch Grant Pass *** | | | G5B09 | G5B08 | | |
| —Ch Grant Pass | | G5B12 | G5B10 | | | |
| —Ch Grant Pass | | G5B13 | | | | K4B04 |
| —Ch Grant Med | A4D12 | | | | G5D02 | |
| —Ch Grant Pass | | | | G5D06 | G5D05 | |
| —Ch Grant Pass | | | G5D10 | G5D07 | | |
| —Ch Grant Pass | | G5D12 | G5D11 | | | |
| —Ch Grant Pass | | G5D13 | | | | K4D12 |
| —Release | A4D09 | | | | | K4D09 |
| —Release Request | A4B08 | | | | | |

*If A2D2 board:

| | |
|---|---|
| H2B07 = H3B09 | H3B10 = H2B07 |
| F2B07 = F3D06 | F3D10 = F2B07 |
| D2B07 = D3B07 | D3D11 = D2B07 |
| B2B07 = B3D07 | B3D12 = B2B07 |

**Mutually exclusive.

***Illustrates Ch Grant (+) being passed through but not connected to any ports in the A1 board and sent to the B1 board by wiring.

## 8140 Model BXX Board Wiring — SC5 to 01A-C2 or 01A-D2 Display/Printer Adapter Board

| Line Name | Cable or SC5 | Display/ Printer Cards | | | |
|---|---|---|---|---|---|
| —IRR | A2B05 | E4B13 | | | |
| —Ch Req Lo | A3D03 | B2D05 | | | |
| —End of Chain | A2D09 | B4D09 | | | |
| —Valid HW | A2D07 | B2B05 | | | |
| —IR/BI 7 | A4B07 | E4D13 | | | |
| —DB PH | A4B12 | C3B04 | | | |
| —DB 0 | A2B02 | C3D06 | | | |
| —DB 1 | A2B08 | C3B05 | | | |
| —DB 2 | A2D11 | C2D09 | | | |
| —DB 3 | A3B04 | C3B02 | | | |
| —DB 4 | A3D07 | C3D02 | | | |
| —DB 5 | A3B09 | C2B10 | | | |
| —DB 6 | A4B02 | C3B03 | | | |
| —DB 7 | A4D10 | C2D12 | | | |
| —DB PL | A4D13 | C3D12 | | | |
| —DB 8 | A2D05 | C4B04 | | | |
| —DB 9 | A2B10 | C4D04 | | | |
| —DB 10 | A2D13 | C4D02 | | | |
| —DB 11 | A3B05 | C4D07 | | | |
| —DB 12 | A3B08 | C4B02 | | | |
| —DB 13 | A3D09 | C4D05 | | | |
| —DB 14 | A4D06 | C3D11 | | | |
| —DB 15 | A4D11 | C3B13 | | | |
| +5 Ve | A2B13 | H2D13 | J2D13 | K2D13<br>H4D13 | K4D13<br>J4D13 |
| —TD Tag | A3B02 | B4B02 | E2D02 | | |
| —I/O Tag | A3D05 | E5B03 | | | |
| —Halt Tag | A3D06 | E4D02 | | | |
| —TA Tag | A3B10 | E2D06 | | | |
| —Sys Reset | A3B12 | E2D04 | | | |
| —Release | A4D09 | C5B09 | | | |
| —Ch Grant Lo | A4D02 | E2B08 | | | |

*SC417 8101 SCF Point-to-Point Net Listing*

## 8101 Model A25 Board Wiring — SC5 to 01A-A2 Disk/Diskette/ Tape Adapter Board

| Line Name | SC5 SSCF | TA Tape | 2nd FA Disk | DA Diskette | 1st FA Disk |
|---|---|---|---|---|---|
| —Valid Byte | A2D06 | B3D11 | | G5D02 | |
| —Valid HW | A2D07 | B3D02 | F3B02 | | H3B02 |
| —Parity Valid | A2B04 | B3B03 | F2D05 | G5D11 | H2D05 |
| —End of Chain | A2D09 | B3D05 | F2B08 | G5D13 | H2B08 |
| —IRR | A2B05 | B3B08 | F2B09 | G4D10 | H2B09 |
| —Chan Req Lo | A3D02 | B3B10 | F3D02 | G4B05 | H3D02 |
| —Modifier | A2B12 | B5B13 | | G4D13 | |
| —IR/BI 0 | A2D02 | | | | H2B12 |
| —IR/BI 1 | A2D04 | | F2B12 | | |
| —IR/BI 2 | | | | | |
| —IR/BI 3 | A3D04 | B3D10 | | | |
| —IR/BI 4 | | | | | |
| —IR/BI 5 | | | | | |
| —IR/BI 6 | | | | | |
| —IR/BI 7 | A4B07 | | | G4B08 | |
| —IR/BI P1 | | | | | |
| —DB PH | A4B12 | B4B04 | F4D10 | G2B12 | H4D10 |
| —DB 0 | A2B02 | B4B05 | F5B04 | G3B04 | H5B04 |
| —DB 1 | A2B08 | B4B03 | F5D11 | G2D13 | H5D11 |
| —DB 2 | A2D11 | B4D06 | F5B07 | G3D02 | H5B07 |
| —DB 3 | A3B04 | B4B09 | F5D05 | G3B02 | H5D05 |
| —DB 4 | A3D07 | B4B07 | F5D10 | G3D06 | H5D10 |
| —DB 5 | A3B09 | B4D11 | F5B13 | G3B07 | H5B13 |
| —DB 6 | A4B02 | B4D05 | F5B08 | G3B08 | H5B08 |
| —DB 7 | A4D10 | B4D12 | F4B10 | G3B03 | H4B10 |
| —DB PL | A4D13 | B4D09 | F5D12 | G2B10 | H5D12 |
| —DB 8 | A2D05 | B4D13 | F5B09 | G2D12 | H5B09 |
| —DB 9 | A2B10 | B4B12 | F5B10 | G3D04 | H5B10 |
| —DB 10 | A2D13 | B4B10 | F5D02 | G3B09 | H5D02 |
| —DB 11 | A3B05 | B4D10 | F5B05 | G3D07 | H5B05 |
| —DB 12 | A3B08 | B4B13 | F5D13 | G2D10 | H5D13 |
| —DB 13 | A3D09 | B4D04 | F5D04 | G3D09 | H5D04 |
| —DB 14 | A4D06 | B4B08 | F5D07 | G3B05 | H5D07 |
| —DB 15 | A4D11 | B4D07 | F5B12 | G3D05 | H5B12 |
| +5 Ve | A2B13 | C5B02 | F4D05<br>F5D06 | G4D05 | H4D05<br>H5D06 |
| —TD Tag | A3B02 | B3D09 | F4D02 | G5D05 | H4D02 |
| —I/O Tag | A3D05 | B2B12 | F2D13 | G5B09 | H2D13 |
| —Halt Tag | A3D06 | B3B09 | F3D04 | G4D02 | H3D04 |
| —TA Tag | A3B10 | B5B04 | F4B08 | G5D02 | H4B08 |
| —TC Tag | A3D10 | | | G5B05 | |
| —Sys Reset | A3B12 | B2D05 | F4B05<br>G3B09 | G5B03 | H4B05<br>J3B09 |
| —Release | A4D09 | C3D02 | G3D13 | G5B02 | J3D13 |
| —Ch Grant Lo | A4D02 | | | G5D10 | |
| —Ch Grant Lo Pass | | B3B07 | | G5B10 | |
| —Ch Grant Lo Pass | | B3D07 | F3B03 | | H3B03 |

## 8101 Board Wiring — SC5 to 01A-A1 or 01A-B1 Communications Adapter Board

| Line Name | SC SSCF | CA Port 4 | CA Port 3 | CA Port 2 | CA Port 1 | To Board A-B2 |
|---|---|---|---|---|---|---|
| –IR/BI P1 | A4D07 | B3B12 | D3B12 | F3B12 | H3B12 | K4D07 |
| –IR/BI 0 | A2D02 | B3B09 | D3B09 | F3B09 | H2B07* | K2D02 |
| –IR/BI 1 | A2D04 | B3D06 | D3D06 | F2B07* | H3D06 | K2D04 |
| –IR/BI 2 | A2B07 | B3B07 | D2B07* | F3B07 | H3B07 | K2B07 |
| –IR/BI 3 | A3D04 | B2B07* | D3D07 | F3D07 | H3D07 | K3D04 |
| –IR/BI 4 | A3B07 | B3B10 | D3B10 | F3B10 | H3B10* | K3B07 |
| –IR/BI 5 | A4D04 | B3D10 | D3D10 | F3D10* | H3D10 | K4D04 |
| –IR/BI 6 | A4D05 | B3D11 | D3D11* | F3D11 | H3D11 | K4D05 |
| –IR/BI 7 | A4B07 | B3D12* | D3D12 | F3D12 | H3D12 | K4B07 |
| –Valid Byte 1 (Byte) | A3D12 | B3B03 | D3B03 | F3B03 | H3B03 | K3D12 |
| –Parity Valid | A2B04 | B2D07 | D2D07 | F2D07 | H2D07 | K2B04 |
| –IRR (Byte) | A3D13 | B2D02 | D2D02 | F2D02 | H2D02 | K3D13 |
| –Valid Byte 1 (HW) | A2D06 | | | | | K2D06 |
| –Valid HW | A2D07 | | | | | K2D07 |
| –Valid Byte 0 | A2B09 | | | | | K2B09 |
| –End of Chain | A2D09 | G4B10 | G4B09 | G4B08 | G4B07 | K2D09 |
| –Exception | A2D10 | | | | | K2D10 |
| –Modifier | A2B12 | | | | | K2B12 |
| –Ch Req Lo | A3D02 | | | | | K3D02 |
| –Ch Req Med** | A3B03 | G4B05 | G4B04 | G4B03 | G4B02 | K3B03 |
| –Ch Req Hi** | A4B05 | G4D13 | G4D11 | G4B13 | G4B12 | K4B05 |
| –IPR | A4B10 | | | | | K4B10 |
| –DB PH | A4B12 | B2B02 | D2B02 | F2B02 | H2B02 | K4B12 |
| –DB 0 | A2B02 | B3B02 | D3B02 | F3B02 | H3B02 | K2B02 |
| –DB 1 | A2B08 | B3D02 | D3D02 | F3D02 | H3D02 | K2B08 |
| –DB 2 | A2D11 | B2D10 | D2D10 | F2D10 | H2D10 | K2D11 |
| –DB 3 | A3B04 | B3B08 | D3B08 | F3B08 | H3B08 | K3B04 |
| –DB 4 | A3D07 | B3D04 | D3D04 | F3D04 | H3D04 | K3D07 |
| –DB 5 | A3B09 | B2D09 | D2D09 | F2D09 | H2D09 | K3B09 |
| –DB 6 | A4B02 | B2B09 | D2B09 | F2B09 | H2B09 | K4B02 |
| –DB 7 | A4D10 | B2D06 | D2D06 | F2D06 | H2D06 | K4D10 |
| –DB PL | A4D13 | | | | | K4D13 |
| –DB 8 | A2D05 | | | | | K2D05 |
| –DB 9 | A2B10 | | | | | K2B10 |
| –DB 10 | A2D13 | | | | | K2D13 |
| –DB 11 | A3B05 | | | | | K3B05 |
| –DB 12 | A3B08 | | | | | K3B08 |
| –DB 13 | A3D09 | | | | | K3D09 |
| –DB 14 | A4D06 | | | | | K4D06 |
| –DB 15 | A4D11 | | | | | K4D11 |
| +5 Ve | A2B13 | C2D11 | E2D11 | G2D11 | J2D11 | K2B13 |
| –TD Tag | A3B02 | B2B05 | D2B05 | F2B05 | H2B05 | K3B02 |
| –I/O Tag | A3D05 | | | | | K3D05 |
| –Halt Tag | A3D06 | B3B04 | D3B04 | F3B04 | H3B04 | K3D06 |
| –TA Tag | A3B10 | B2D05 | D2D05 | F2D05 | H2D05 | K3B10 |
| –TC Tag | A3D10 | B2D08 | D2B08 | F2B08 | H2B08 | K3D10 |
| –Byte Tag | A3D11 | | | | | K3D11 |
| –System Reset | A3B12 | B3D05 | D3D05 | F3D05 | H3D05 | K3B12 |

| Line Name | | SC SSCF | CA Port 4 | CA Port 3 | CA Port 2 | CA Port 1 | To Board A-B2 |
|---|---|---|---|---|---|---|---|
| –I/O Tag (Byte) | | A3B13 | B2B04 | D2B04 | F2B04 | H2B04 | K3B13 |
| –Ch Grant Lo | | A4D02 | | | | | K4D02 |
| –Ch Grant Hi | | A4B04 | | | | G5B03 | |
| –Ch Grant Pass | | | | | G5B07 | G5B04 | |
| –Ch Grant Pass | *** | | | G5B09 | G5B08 | | |
| –Ch Grant Pass | | | G5B12 | G5B10 | | | |
| –Ch Grant Pass | | | G5B13 | | | | K4B04 |
| –Ch Grant Med | | A4D12 | | | | G5D02 | |
| –Ch Grant Pass | | | | | G5D06 | G5D05 | |
| –Ch Grant Pass | | | | G5D10 | G5D07 | | |
| –Ch Grant Pass | | | G5D12 | G5D11 | | | |
| –Ch Grant Pass | | | G5D13 | | | | K4D12 |
| –Release | | A4D09 | | | | | K4D09 |
| –Release Request | | A4B08 | | | | | |

*If A1B1 board:

| | |
|---|---|
| H2B07 = H3B09 | H3B10 = H2B07 |
| F2B07 = F3D06 | F3D10 = F2B07 |
| D2B07 = D3B07 | D3D11 = D2B07 |
| B2B07 = B3D07 | B3D12 = B2B07 |

**Mutually exclusive.

***Illustrates Ch Grant (+) being passed through but not connected to any ports in the A1 board and sent to the B1 board by wiring.

### 8101 Board Wiring (All Models Except A25) – SC5 to 01A-A2 Disk/Diskette/ Tape Adapter Board

| Line Name | SC5 SSCF | TA Tape | DA Diskette | FA Disk |
|---|---|---|---|---|
| –Valid Byte | A2D06 | B3D11 | G5D02 | |
| –Valid HW | A2D07 | B3D02 | | H3B02 |
| –Parity Valid | A2B04 | B3B03 | G5D11 | H2D05 |
| –End of Chain | A2D09 | B3D05 | G5D13 | H2B08 |
| –IRR | A2B05 | B3B08 | G4D10 | H2B09 |
| –Chan Req Lo | A3D02 | B3B10 | G4B05 | H3D02 |
| –Modifier | A2B12 | B5B13 | G4D13 | |
| –IR/BI 0 | A2D02 | | | H2B12 |
| –IR/BI 1 | | | | |
| –IR/BI 2 | | | | |
| –IR/BI 3 | A3D04 | B3D10 | | |
| –IR/BI 4 | | | | |
| –IR/BI 5 | | | | |
| –IR/BI 6 | | | | |
| –IR/BI 7 | A4B07 | | G4B08 | |
| –IR/BI P1 | | | | |
| –DB PH | A4B12 | B4B04 | G2B12 | H4D10 |
| –DB 0 | A2B02 | B4B05 | G3B04 | H5B04 |
| –DB 1 | A2B08 | B4B03 | G2D13 | H5D11 |
| –DB 2 | A2D11 | B4D06 | G3D02 | H5B07 |
| –DB 3 | A3B04 | B4B09 | G3B02 | H5D05 |
| –DB 4 | A3D07 | B4B07 | G3D06 | H5D10 |
| –DB 5 | A3B09 | B4D11 | G3B07 | H5B13 |
| –DB 6 | A4B02 | B4D05 | G3B08 | H5B08 |
| –DB 7 | A4D10 | B4D12 | G3B03 | H4B10 |
| –DB PL | A4D13 | B4D09 | G2B10 | H5D12 |
| –DB 8 | A2D05 | B4D13 | G2D12 | H5B09 |
| –DB 9 | A2B10 | B4B12 | G3D04 | H5B10 |
| –DB 10 | A2D13 | B4B10 | G3B09 | H5D02 |
| –DB 11 | A3B05 | B4D10 | G3D07 | H5B05 |
| –DB 12 | A3B08 | B4B13 | G2D10 | H5D13 |
| –DB 13 | A3D09 | B4D04 | G3D09 | H5D04 |
| –DB 14 | A4D06 | B4B08 | G3B05 | H5D07 |
| –DB 15 | A4D11 | B4D07 | G3D05 | H5B12 |
| +5 Ve | A2B13 | C5B02 | G4D05 | H5D05 |
| | | | | H5D06 |
| –TD Tag | A3B02 | B3D09 | G5D05 | G4D02 |
| –I/O Tag | A3D05 | B2B12 | G5B09 | H2D13 |
| –Halt Tag | A3D06 | B3B09 | G4D02 | H3D04 |
| –TA Tag | A3B10 | B5B04 | G5D02 | H4B08 |
| –TC Tag | A3D10 | | G5B05 | |
| –Sys Reset | A3B12 | B2D05 | G5B03 | H4B05 |
| | | | | J3B09 |
| –Release | A4D09 | C3D02 | G5B02 | J3D13 |
| –Ch Grant Lo | A4D02 | | G5D10 | |
| –Ch Grant Lo Pass | | B3B07 | G5B10 | |
| –Ch Grant Lo Pass | | B3D07 | | H3B03 |

### 8101 Board Wiring – SC5 to 01A-A1 or 01A-B1 Display/Printer Adapter Board

| Line Name | SC5 | Display/ Printer Cards | | | |
|---|---|---|---|---|---|
| –IRR | A2B05 | E4B13 | | | |
| –Ch Req Lo | A3D03 | B2D05 | | | |
| –End of Chain | A2D09 | B4D09 | | | |
| –Valid HW | A2D07 | B2B05 | | | |
| –IR/BI 7 | A4B07 | E4D13 | | | |
| –DB PH | A4B12 | C3B04 | | | |
| –DB 0 | A2B02 | C3D06 | | | |
| –DB 1 | A2B08 | C3B05 | | | |
| –DB 2 | A2D11 | C2D09 | | | |
| –DB 3 | A3B04 | C3B02 | | | |
| –DB 4 | A3D07 | C3D02 | | | |
| –DB 5 | A3B09 | C2B10 | | | |
| –DB 6 | A4B02 | C3B03 | | | |
| –DB 7 | A4D10 | C2D12 | | | |
| –DB PL | A4D13 | C3D12 | | | |
| –DB 8 | A2D05 | C4B04 | | | |
| –DB 9 | A2B10 | C4D04 | | | |
| –DB 10 | A2D13 | C4D02 | | | |
| –DB 11 | A3B05 | C4D07 | | | |
| –DB 12 | A3B08 | C4B02 | | | |
| –DB 13 | A3D09 | C4D05 | | | |
| –DB 14 | A4D06 | C3D11 | | | |
| –DB 15 | A4D11 | C3B13 | | | |
| +5 Ve | A2B13 | H2D13 | J2D13 | K2D13 | K4D13 |
| | | | | H4D13 | J4D13 |
| –TD Tag | A3B02 | B4B02 | E2D02 | | |
| –I/O Tag | A3D05 | E5B03 | | | |
| –Halt Tag | A3D06 | E4D02 | | | |
| –TA Tag | A3B10 | E2D06 | | | |
| –Sys Reset | A3B12 | E2D04 | | | |
| –Release | A4D09 | C5B09 | | | |
| –Ch Grant Lo | A4D02 | E2B08 | | | |

## SC420 Card Wiring Charts

Figure SC420-1 through SC420-5 are wiring charts that show SCF card and connector pin assignments.

| Board Signal Names | SC1 & SC7 Cards | | TCC Signal Names | SC7 Card Board Pins |
|---|---|---|---|---|
| – PIO Data 0 (0.0) | B02 ⟷ W22 | – | PIO Data 0 (0.0) | B02 |
| Spare | D02 — GND → W02 | – | SC Present | D02 |
| – PIO Data 14 (1.6) | B03 ⟷ W23 | – | PIO Data 14 (1.6) | B03 |
| + 5V | D03 | | GND | D03 |
| – PIO Data 3 (0.3) | B04 ⟷ W24 | – | PIO Data 3 (0.3) | B04 |
| – PIO Data 4 (0.4) | D04 ⟷ W04 | – | PIO Data 4 (0.4) | D04 |
| – PIO Data 5 (0.5) | B05 ⟷ W25 | – | PIO Data 5 (0.5) | B05 |
| – PIO Data 8 (1.0) | D05 ⟷ W05 | – | PIO Data 8 (1.0) | D05 |
| – 5V | B06 | | GND | B06 |
| – PIO Data 7 (0.7) | D06 ⟷ W06 | – | PIO Data 7 (0.7) | D06 |
| – PIO Data P0 (0.P) | B07 ⟷ W27 | – | PIO Data P0 (0.P) | B07 |
| – PIO Data 6 (0.6) | D07 ⟷ W07 | – | PIO Data 6 (0.6) | D07 |
| – PIO Data 1 (0.1) | B08 ⟷ W28 | – | PIO Data 1 (0.1) | B08 |
| GND | D08 | | GND | D08 |
| – PIO Data 12 (1.4) | B09 ⟷ W29 | – | PIO Data 12 (1.4) | B09 |
| – PIO Data 11 (1.3) | D09 ⟷ W09 | – | PIO Data 11 (1.3) | D09 |
| – PIO Data 9 (1.1) | B10 ⟷ W30 | – | PIO Data 9 (1.1) | B10 |
| – PIO Data 13 (1.5) | D10 ⟷ W10 | – | PIO Data 13 (1.5) | D10 |
| + 8.5 V | B11 | | GND | B11 |
| – PIO Data 2 (0.2) | D11 ⟷ W11 | – | PIO Data 2 (0.2) | D11 |
| – PIO Data 15 (1.7) | B12 ⟷ W32 | – | PIO Data 15 (1.7) | B12 |
| – Save PSW | D12 ⟵ W12 | – | Data In 6 (0.6) | D12 |
| – PIO Data P1 (1.P) | B13 ⟷ W33 | – | PIO Data P1 (1.P) | B13 |
| – PIO Data 10 (1.2) | D13 ⟷ W13 | – | PIO Data 10 (1.2) | D13 |
| | | | | |
| + TD Tag | G02 ⟷ X22 | – | TD Tag | G02 |
| – LVL N Request 2 | J02 ⟵ X02 | – | Valid Hw | J02 |
| – Exception | G03 ⟵ X23 | – | Exception | G03 |
| + 5V | J03 | | GND | J03 |
| – Modifier | G04 ⟵ X24 | – | Modifier | G04 |
| – End of Chain | J04 ⟵ X04 | – | End of Chain | J04 |
| – PV | G05 ⟵ X25 | – | PV | G05 |
| – I/O Tag | J05 ⟷ X05 | – | I/O Tag | J05 |
| – 5V | G06 | | GND | G06 |
| – Valid Hw | J06 ⟷ X06 | – | I/O Tag (B) | J06 |
| – Wait State Gate 10 | G07 ⟷ X27 | – | VB1 (B) | G07 |
| – VB1 | J07 ⟵ X07 | – | VB1 | J07 |
| Spare | G08 ⟵ X28 | – | Irr (B) | G08 |
| GND | J08 | | GND | J08 |
| – Irr | G09 ⟵ X29 | – | Irr | G09 |
| – Halt | J09 ⟷ X09 | – | Halt | J09 |
| – TA Tag | G10 ⟷ X30 | – | TA Tag | G10 |
| – TC Tag | J10 ⟷ X10 | – | TC Tag | J10 |
| + 8.5V | G11 | | GND | G11 |
| – Byte Tag | J11 ⟷ X11 | – | Byte Tag | J11 |
| – VB0 | G12 ⟵ X32 | – | VB0 | G12 |
| – Ch Grant | J12 ⟷ X12 | – | Ch Grant Hi | J12 |
| – Wait State Out | G13 ⟵ X33 | – | Ch Req Hi | G13 |
| – Ch Request | J13 ⟵ X13 | – | Ch Req Low | J13 |
| | | | | |
| – Dest 12 6 | M02 → Y22 | + | VE (– Por) | M02 |
| – Dest 13 6 | P02 → Y02 | – | Ch Grant Low | P02 |
| – Dest 14 6 | M03 → Y23 | – | Data In 12 (1.4) | M03 |
| + 5V | P03 | | GND | P03 |

| Board Signal Names | SC1 & SC7 Cards | | TCC Signal Names | | SC7 Card Board Pins |
|---|---|---|---|---|---|
| – Dest 15 | M04 → Y24 | – | IR/B1–0 | 8130 alone | M04 |
| – Restart | P04 ⟵ Y04 | – | IR/B1–5 | | P04 |
| – 1 MHz | M05 ⟵ Y25 | – | IR/B1–2 | | M05 |
| + PMO | P05 → Y05 | – | IR/B1–6 | | P05 |
| – 5V | M06 | | GND | | M06 |
| – Monitor | P06 → Y26 | | GND | | P06 |
| + VE (–POR) | M07 ⟵ Y06 | – | IR/B1–1 | | M07 |
| – SDCI Bus(BOP) Sel'td | P07 → Y27 | – | IR/B1–7 | | P07 |
| – SDCI Bus Halt | M08 ⟵ Y07 | – | IR/B1–P | | M08 |
| GND | P08 | | GND | | P08 |
| + RAM/–ROS Acc'bl 3 | M09 ⟵ Y28 | – | IR/B1–4 | | M09 |
| – BOP CT/CK (X2 Dec) | P09 ⟵ Y08 | | GND | | P09 |
| – BOP PNL/CK (X4 Dec) | M10 ⟵ Y29 | – | IR/B1–3 | | M10 |
| + 60 Hz Ctrl | P10 → Y09 | – | Release | | P10 |
| + 8.5V | M11 ⟵ Y30 | – | Ipr | | M11 |
| – 50/60 Hz | P11 → Y10 | – | Data In 11 (1.3) | | P11 |
| – 500 Ms Rate (2Hz) | M12 ⟵ Y31 | | GND | | M12 |
| – BOP Irpt | P12 → Y11 | – | SC1 Reset (Ext) | | P12 |
| – 1.02 Ms Rate (1 KHz) | M13 ⟵ Y32 | – | SCF–B Lvl N | | M13 |
| – 500 Ms Rate (2 Hz) | P13 ⟵ Y12 | – | 500 Ms Rate (2 Hz) | | P13 |
| | | → Y33 | – | 10 MHz (Repow'rd) | |
| | | → Y13 | – | I/O Reset | |
| – 1.02 Ms Rate (1 KHz) | S02 ⟵ Z22 | | Interlock | | S02 |
| – 10 MHz | U02 ⟵ Z02 | – | 1.024 Ms Rt (1 KHz) | | U02 |
| – I/O OP | S03 ⟵ Z23 | – | SDCI Bus 0 | | S03 |
| + 5V | U03 ⟵ Z03 | – | 500 Ms Rate (2Hz) | | U03 |
| – PB Request | S04 → Z24 | – | SDCI Bus 1 | | S04 |
| – System Reset | U04 ⟵ Z04 | – | I/O OP | | U04 |
| – SDCI Bus 2 | S05 ⟵ Z25 | – | SDCI Bus 2 | | S05 |
| – SDCI Bus 7 | U05 ⟵ Z05 | – | 1 MHz | | U05 |
| – 5V | S06 ⟵ Z26 | – | SDCI Bus 3 | | S06 |
| – SDCI Bus 6 | U06 ⟵ Z06 | – | SDCI Bus Sync | | U06 |
| – HFP Irpt | S07 → Z27 | | GND | | S07 |
| – SDCI Bus 3 | U07 ⟵ Z07 | | Spare | | U07 |
| – SDCI Bus 4 | S08 ⟵ Z28 | – | SDCI Bus 4 | | S08 |
| GND | U08 ⟵ Z08 | | GND | | U08 |
| – SDCI Bus 1 | S09 ⟵ Z29 | – | SDCI Bus 5 | | S09 |
| – SDCI Bus 0 | U09 ⟵ Z09 | – | System Reset | | U09 |
| – SDCI Bus 5 | S10 ⟵ Z30 | – | SDCI Bus 6 | | S10 |
| Spare | U10 ⟵ Z10 | – | PB Reset Req | | U10 |
| + 8.5M | S11 ⟵ Z31 | – | SDCI Bus 7 | | S11 |
| Spare | U11 ⟵ Z11 | | Spare | | U11 |
| – SDCI Bus P | S12 ⟵ Z32 | – | SDCI Bus P | | S12 |
| – Power Off To PS 5 | U12 ⟵ Z12 | | Spare | | U12 |
| – Read Gate Drivers | S13 → Z33 | | Interlock | | S13 |
| – SDCI Bus Sync | U13 ⟵ Z13 | | Spare | | U13 |

**Figure SC420-1. SC1 and SC7 Card and Connector Signals**

**I/O Pin Assignments**

| Board Signal Names | | | | | TCC Signal Names |
|---|---|---|---|---|---|
| + Oc Stat Cmd | > | B02 — 5 | 1 — W22 | – | PIO Data 0 (0.0) |
| – Data Out Bus 0 | < | D02 — 5, 3 | — W02 | – | SC1 Present |
| + 08 Stat Cmd | > | B03 — 5 | — W23 | – | PIO Data 14 (1.6) |
| + 5 Volts | > | D03 | — W03 | | GND |
| | — | B04 | 1 — W24 | – | PIO Data 3 (0.3) |
| + Parity Val Lth | > | D04 — 3 | — W04 | – | PIO Data 4 (0.4) |
| – Data Out Bus 8 | < | B05 — 5, 3 | 1 — W25 | – | PIO Data 5 (0.5) |
| – Irr to Card 2 | > | D05 — 3 | 1 — W05 | – | PIO Data 8 (1.0) |
| | — | B06 | 1 — W26 | | GND |
| + Val Byte 1 Lth | > | D06 — 3 | 1 — W06 | – | PIO Data 7 (0.7) |
| + Val Hw Lth | > | B07 — 3 | — W27 | – | PIO Data P0 (0.P) |
| | — | D07 | 1 — W07 | – | PIO Data 6 (0.6) |
| – Data Out Bus 1 | < | B08 — 5, 3 | 1 — W28 | – | PIO Data 1 (0.1) |
| GND | — | D08 | 1 — W08 | | GND |
| – End of Chain | > | B09 — 3 | 1 — W29 | – | PIO Data 12 (1.4) |
| + Val Byte 0 Lth | > | D09 — 3 | 1 — W09 | – | PIO Data 11 (1.3) |
| + Exception Lth | > | B10 — 3 | 1 — W30 | – | PIO Data 9 (1.1) |
| – Data Out Bus 9 | < | D10 — 5, 3 | 1 — W10 | – | PIO Data 13 (1, 5) |
| | — | B11 | 1 — W31 | | GND |
| – Data Out Bus 2 | < | D11 — 5 | 1 — W11 | – | PIO Data 2 (0.2) |
| – IO Reset To LLD | > | B12 — 3 | 1 — W32 | – | PIO Data 15 (1.7) |
| + Modifier Lth | > | D12 — 3 | 1 — W12 | – | Data In 6 (0.6) |
| – Data Out Bus 10 | < | B13 — 5, 3 | 1 — W33 | – | PIO Data P1 (I.P) |
| – Xmit Ctrl | < | D13 — 3 | 1 — W13 | – | PIO Data 10 (1.2) |
| | | | | | |
| + Go | > | G02 — 5 | 1 — X22 | – | TD Tag |
| + TD | < | J02 — 5, 3 | 1 — X02 | – | Valid Hw |
| 2 Hz Free Run | < | G03 — 3 | 1 — X23 | – | Exception |
| + 5 Volts | > | J03 — 3 | 1 — X03 | – | GND |
| + Pwr Outage Lth | > | G04 — 5 | 1 — X24 | – | Modifier |
| – Data Out Bus 3 | < | J04 — 5, 3 | — X04 | – | End of Chain |
| + I/O | < | G05 — 5 | 1 — X25 | – | PV |
| – Data Out Bus 11 | < | J05 — 5, 3 | 1 — X05 | – | I/O Tag |
| | — | G06 | 1 — X26 | | GND |
| + Inward | > | J06 — 5 | 1 — X06 | – | I/O Tag (B) |
| – Data Out Bus 4 | < | G07 — 5, 3 | — X27 | – | VB1 (B) |
| – Int or ML Vhw | <> | J07 — 5 | 1 — X07 | – | VB1 |
| – Data Out Bus 12 | < | G08 — 5, 3 | 1 — X28 | – | Irr (B) |
| GND | — | J08 | 1 — X08 | | GND |
| – Data Out Bus 13 | < | G09 — 5, 3 | 1 — X29 | – | Irr |
| – Data Out Bus 5 | < | J09 — 5, 3 | 1 — X09 | – | Halt |
| + TC | < | G10 — 5, 3 | 1 — X30 | – | TA Tag |
| + TA | < | J10 — 5, 3 | 1 — X10 | – | TC Tag |
| | — | G11 | — X31 | | GND |
| – Byte Tag To LLD | < | J11 — 3 | 1 — X11 | – | Byte Tag |
| + Ch Grant | < | G12 — 5 | 1 — X32 | – | VB0 |
| – SC1 Reset | < | J12 — 5 | — X12 | – | Ch Grant Hi |
| – CR to Card 2 | < | G13 — 3 | — X33 | – | Ch Req Hi |
| – Outbound Ctrl | < | J13 — 5, 3 | — X13 | – | Ch Req Low |

**I/O Pin Assignments**

| Board Signal Names | | | | | TCC Signal Names | |
|---|---|---|---|---|---|---|
| + Load Chcw Reg | < | M02 — 5 | 1 — Y22 | + | Ve (–POR) | |
| – Data Out Bus 6 | < | P02 — 5, 3 | 1 — Y02 | – | Ch Grant Low | |
| | — | M03 | 1 — Y23 | – | Data In 12 (1.4) | |
| + 5 Volts | > | P03 | — Y03 | | GND | |
| – Val Dly 250-300 | < | M04 — 3 | — Y24 | – | IR/B1-0 | Not Used |
| – Val Dly 150-200 | < | P04 — 3 | — Y04 | – | IR/B1-5 | |
| + 10 MHz | < | M05 — 5, 3 | — Y25 | – | IR/B1-2 | |
| + Any Tag | < | P05 — 5, 3 | — Y05 | – | IR/B1-6 | |
| | — | M06 | — Y26 | | GND | |
| – Data Out Bus 14 | < | P06 — 5, 3 | 1 — Y06 | – | IR/B1-1 | |
| – Halt To Lld | < | M07 — 3 | — Y27 | – | IR/B1-7 | |
| + X8 Tag Wrap | > | P07 — 5.3 | — Y07 | – | IR/B1-P | |
| + IPR To Card 2 | > | M08 — 3 | 1 — Y28 | – | IR/B1-4 | |
| GND | — | P08 | — Y08 | | GND | |
| + X8 Crp Wrap | > | M09 — 5 | 1 — Y29 | – | IR/B1-3 | |
| – SSCF Res To Lid | < | P09 — 5, 3 | — Y09 | – | Release | |
| – Data Out Bus 7 | < | M10 — 5, 3 | — Y30 | – | IPR | |
| – Parity Good | < | P10 — 5 | 1 — Y10 | – | Data In 11 (1.3) | |
| | — | M11 | — Y31 | – | GND | |
| – Data Out Bus 15 | < | P11 — 5, 3 | 1 — Y11 | | SC1 Reset (EXT) | |
| – SCFA Res/Not 10 | < | M12 — 5 | 1 — Y32 | – | PSCF Bstat | |
| – Data Out Bus P0 | < | P12 — 5, 3 | — Y12 | – | 500 Ms Rate (2Hz) | |
| – Data Out Bus P1 | < | M13 — 5, 3 | 1 — Y33 | – | 10 MHz (Repow'rd) | |
| – Any Val Lth | < | P13 — 5, 3 | 1 — Y13 | – | I/O Reset | |
| | | | | | | |
| | — | S02 | 3 — Z22 | + | Data In P0 | |
| | — | U02 | 3 — Z02 | + | Data In 0 | |
| | — | S03 | 3 — Z23 | + | Data In 1 | |
| + 5 Volts | > | U03 | — Z03 | | GND | |
| + Enable Data Lths | > | S04 — 5 | 3 — Z24 | + | Data In 2 | |
| – Power Seq Comp | > | U04 — 3 | 3 — Z04 | + | Data In 3 | |
| | — | S05 | 3 — Z25 | + | Data In 4 | |
| | — | U05 | 3 — Z05 | + | Data In 5 | |
| | — | S06 | — Z26 | | GND | |
| + SSCF MCK | > | U06 | 3 — Z06 | + | Data In 6 | |
| | — | S07 | 3 — Z27 | + | Data In 7 | |
| | — | U07 | 3 — Z07 | + | Data In P1 | |
| | — | S08 | 3 — Z28 | + | Data In 8 | |
| GND | — | U08 | — Z08 | | GND | |
| | — | S09 | 3 — Z29 | + | Data In 9 | |
| + SSCF IR | > | U09 — 3 | 3 — Z09 | + | Data In 10 | |
| | — | S10 | 3 — Z30 | + | Data In 11 | |
| | — | U10 | 3 — Z10 | + | Data In 12 | |
| | — | S11 | — Z31 | | GND | |
| | — | U11 | 3 — Z11 | + | Data In 13 | |
| | — | S12 | 3 — Z32 | + | Data In 14 | |
| | — | U12 | 3 — Z12 | + | Data In 15 | |
| | — | S13 | — Z33 | | | |
| | — | U13 | — Z13 | | | |

**Note:** *"1" indicates a signal is from/to SC1; "3" indicates a signal is from/to SC3; "5" indicates a signal is from/to SC4.*

**Figure SC420-2. SC2 Card and Connector Signals**

| Board Signal Names | | I/O Pin Assignments | | | TCC Signal Names | | |
|---|---|---|---|---|---|---|---|
| + OC Status Cmd | < | B02 | 2 | W22 | – | | |
| – Data Out Bus 0 | <> | D02 | 2 | W02 | – | | |
| + 08 Stat Cmd | < | B03 | 2 | W23 | – | | |
| + 5 Volts | > | D03 | | W03 | – | GND | |
| + 08 Broadcast | < | B04 | 3 | W24 | – | | |
| | | D04 | | W04 | – | | |
| – Data Out 8 | > | B05 | 2 | W25 | – | | |
| | | D05 | | W05 | – | | |
| | | B06 | | W26 | – | GND | |
| + Valid Byte 1 | > | D06 | 3 | W06 | – | | |
| + Valid Halfword | > | B07 | 3 | W27 | – | | |
| | | D07 | | W07 | – | | |
| – Data Out Bus 1 | <> | B08 | 2 | W28 | – | | |
| GND | | D08 | | W08 | – | GND | |
| – EOC | > | B09 | 3 | W29 | – | | |
| + Valid Byte 0 | > | D09 | 3 | W09 | – | | |
| | | B10 | | W30 | – | | |
| – Data Out Bus 9 | > | D10 | 3 | W10 | – | | |
| | | B11 | | W31 | – | GND | |
| – Data Out Bus 2 | <> | D11 | 3 | W11 | – | | |
| | | B12 | | W32 | – | | |
| + Modifier Lth | > | D12 | 3 | W12 | – | | |
| – Data Out 10 | > | B13 | 2 | W33 | – | | |
| | | D13 | | W13 | – | | |
| + G0 | < | G02 | 2 | X22 | – | | |
| + TD | > | J02 | 2 | X02 | – | | |
| | | G03 | | X23 | – | | |
| + 5 Volts | > | J03 | | X03 | – | GND | |
| + Pwr Outage Lth | < | G04 | 2 | X24 | – | | |
| – Data Out Bus 3 | <> | J04 | 2 | X04 | – | | |
| + IO | > | G05 | 2 | X25 | – | | |
| – Data Out Bus 11 | > | J05 | 2 | X05 | – | | |
| | | G06 | | X26 | – | GND | |
| + Inward | < | J06 | 3, 2 | X06 | – | | |
| – Data Out Bus 4 | <> | G07 | 2 | X27 | – | | |
| – Int/ML Vhw | > | J07 | 3, 2 | X07 | – | | |
| – Data Out Bus 12 | > | G08 | 2 | X28 | – | | |
| GND | | J08 | | X08 | – | GND | |
| – Data Out Bus 13 | > | G09 | 2 | X29 | – | | |
| – Data Out Bus 5 | > | J09 | 2 | X09 | – | | |
| + TC | > | G10 | 2 | X30 | – | | |
| + TA | > | J10 | 2 | X10 | – | | |
| | | G11 | | X31 | – | GND | |
| | | J11 | | X11 | – | | |
| + CG | > | G12 | 2 | X32 | – | | |
| – SC1 Reset | > | J12 | 2 | X12 | – | | |
| | | G13 | | X33 | – | | |
| – Outbound Ctrl | < | J13 | 3, 2 | X13 | – | | |
| + Load Chcw Reg | > | M02 | 2 | Y22 | – | | |
| – Data Out Bus 6 | <> | P02 | 2 | Y02 | – | | |
| – SSCF Pwr Out | > | M03 | 3 | Y23 | – | | |
| + 5 Volts | > | P03 | | Y03 | – | GND | |
| | | M04 | | Y24 | – | | |
| | | P04 | | Y04 | – | | |
| 10 MHz | > | M05 | 2 | Y25 | – | | |
| + Any Tag | > | P05 | 2 | Y05 | – | | |
| | | M06 | | Y26 | – | GND | |
| – Data Out Bus 14 | > | P06 | 2 | Y06 | – | | |
| | | M07 | | Y27 | – | | |

| Board Signal Names | | I/O Pin Assignments | | | | TCC Signal Names | | |
|---|---|---|---|---|---|---|---|---|
| + X8 Tag Wrap | < | P07 | 2, 3 | | Y07 | – | | |
| | | M08 | | | Y28 | – | | |
| GND | < | P08 | | | Y08 | – | GND | |
| + X8 Crp Wrap | < | M09 | 3, 2 | | Y29 | – | | |
| – SSCF Res To Lld | < | P09 | 3 | | Y09 | – | | |
| – Data Out Bus 7 | <> | M10 | 2 | | Y30 | – | | |
| – Parity Good | > | P10 | 2 | | Y10 | – | | |
| | | M11 | | | Y31 | – | GND | |
| – Data Out Bus 15 | > | P11 | 2 | | Y11 | – | | |
| – SCFA Res/Not IO | > | M12 | 2 | | Y32 | – | | |
| – Data Out P0 | < | P12 | 3 | | Y12 | – | | |
| | | M13 | | | Y33 | – | | |
| – Any Valid Lth | > | P13 | 2 | | Y13 | – | | |
| | | S02 | | 3 | Z22 | + | Data In P0 | |
| | | U02 | | 3 | Z02 | + | Data In 0 | |
| | | S03 | | 3 | Z23 | + | Data In 1 | |
| + 5 Volts | > | U03 | | | Z03 | | GND | |
| + Enbl Data Lths | < | S04 | 2 | 3 | Z24 | + | Data In 2 | |
| | | U04 | | 3 | Z04 | + | Data In 3 | |
| | | S05 | | 3 | Z25 | + | Data In 4 | |
| | | U05 | | 3 | Z05 | + | Data In 5 | |
| | | S06 | | | Z26 | | GND | |
| | | U06 | | 3 | Z06 | + | Data In 6 | |
| | | S07 | | 3 | Z27 | + | Data In 7 | |
| | | U07 | | | Z07 | | | |
| | | S08 | | 3 | Z28 | + | Data In 8 | |
| GND | | U08 | | | Z08 | – | GND | |
| | | S09 | | | Z29 | | | |
| | | U09 | | | Z09 | | | |
| | | S10 | | | Z30 | | | |
| | | U10 | | | Z10 | | | |
| | | S11 | | | Z31 | – | GND | |
| | | U11 | | | Z11 | – | | |
| | | S12 | | 3 | Z32 | + | Data In 14 | |
| | | U12 | | 3 | Z12 | + | Data In 15 | |
| | | S13 | | | Z33 | – | | |
| | | U13 | | | Z13 | – | | |

**Note:** *"2" indicates a signal is from/to SC2;*
*"3" indicates a signal is from/to SC4.*

**Figure SC420-3. SC3 Card and Connector Signals**

| Board Signal Names | I/O Pin Assignments | | | TCC Signal Names |
|---|---|---|---|---|
| | B02 | OI | W22 + | SCF Signal Bus P0 |
| – Data Out Bus 0 | D02 — 2, 5 | OI | W02 + | CR-1 |
| | B03 | | W23 | GND |
| + 5 Volts | D03 | OI | W03 + | CR-2 |
| + 08 Brdcst Cmd | B04 — 5 | OI | W24 + | Ch Grant |
| + Parity Valid | D04 — 2 | | W04 | GND |
| – Data Out Bus 8 | B05 — 2 | OI | W25 + | IPR |
| – Irr To Card 2 | D05 — 2 | OI | W05 + | SCF Signal Bus P1 |
| | B06 | OI | W26 + | IO Reset |
| + Valid Byte 1 | D06 — 2.5 | OI | W06 + | IO |
| + Valid Halfword | B07 — 2, 5 | | W27 | GND |
| | D07 | OI | W07 + | End of Chain |
| – Data Out Bus 1 | B08 — 2, 5 | OI | W28 + | SCF Signal Bus 0 |
| GND | D08 | | W08 | GND |
| – EOC Dot | B09 — 2, 5 | OI | W29 + | Halt |
| + Valid Byte 0 | D09 — 2, 5 | OI | W09 + | Valid Byte 0 |
| + Exception Lth | B10 — 2 | OI | W30 + | SCF Signal Bus 8 |
| – Data Out Bus 9 | D10 — 2 | OI | W10 + | SSCF Reset |
| | B11 | | W31 | GND |
| – Data Out Bus 2 | D11 — 2, 5 | OI | W11 + | SCF Signal Bus 1 |
| – IO Reset To Lld | B12 — 2 | OI | W32 + | 10 MHz (Unused) |
| + Modifier Lth | D12 — 2, 5 | | W12 | GND |
| – Data Out Bus 10 | B13 — 2 | | W33 | |
| – Xmit Ctrl | D13 — 2 | OI | W13 + | SCF Signal Bus 9 |
| | G02 | OI | X22 + | TC |
| + TD | J02 — 2 | OI | X02 + | Xmit Ctrl |
| 2 Hz Free Run | G03 — 2 | | X23 + | GND |
| + 5 Volts | J03 | OI | X03 + | Hold Power On |
| | G04 | OI | X24 + | SCF Signal Bus 2 |
| – Data Out Bus 3 | J04 — 2 | | X04 | GND |
| + IO | G05 — 2 | OI | X25 + | SCF Signal Bus 10 |
| – Data Out Bus 11 | J05 — 2 | OI | X05 + | Valid Byte 1 |
| | G06 | OI | X26 + | Release Req |
| + Inward | J06 — 5 | OI | X06 + | TD |
| – Data Out Bus 4 | G07 — 2, 5 | | X27 | GND |
| – Int/ML Vhw | J07 — 2, 5 | OI | X07 + | SCF Signal Bus 3 |
| – Data Out Bus 12 | G08 — 2 | OI | X28 + | SCF Signal Bus 11 |
| GND | J08 | | X08 | GND |
| – Data Out Bus 13 | G09 — 2 | OI | X29 + | SCF Signal Bus 4 |
| – Data Out Bus 5 | J09 — 2, 5 | OI | X09 + | SCF Signal Bus 12 |
| + TC | G10 — 2 | OI | X30 + | Valid Halfword |
| + TA | J10 — 2 | OI | X10 + | TA |
| | G11 | | X31 | GND |
| – Byte Tag To Lld | J11 — 2 | OI | X11 + | Parity Valid |
| + Ch Grant | G12 — 2 | OI | X32 + | CRP-4 |
| | J12 | | X12 | GND |
| – CR To Card 2 | G13 — 2 | OI | X33 + | CRP-2 |
| – Outbound Ctrl | J13 — 2, 5 | OI | X13 + | CRP-1 |
| | M02 | OI | Y22 + | SCF Signal Bus 5 |
| – Data Out Bus 6 | P02 — 2, 5 | OI | Y02 + | Outbound Ctrl |
| – SSCF Pwr Outage | M03 — 5 | | Y23 | GND |
| + 5 Volts | P03 | OI | Y03 + | CRP-8 |
| – Val Dly 250–300 | M04 — 2 | OI | Y24 + | Irr |
| – Val Dly 150–200 | P04 — 2 | | Y04 | GND |
| + 10 MHz | M05 — 2 | OI | Y25 + | Power Drop |
| + Any Tag | P05 — 2 | OI | Y05 + | Byte Tag |
| | M06 | OI | Y26 – | All SSCF Sel'd |

| Board Signal Names | I/O Pin Assignments | | | TCC Signal Names |
|---|---|---|---|---|
| – Data Out Bus 14 | P06 — 2 | OI | Y06 + | SCF Signal Bus 13 |
| – Halt To Lld | M07 — 2 | | Y27 | GND |
| + X8 Tag Wrap | P07 — 5 | OI | Y07 – | |
| + IPR To Card 2 | M08 — 2 | OI | Y28 + | SSCF Irp+ |
| GND | P08 | | Y08 | GND |
| + X8 Crp Wrap | M09 — 5 | OI | Y29 + | SSCF Mck Irpt |
| – SSCF Res To Lld | P09 — 2, 5 | OI | Y09 + | Modifier |
| – Data Out Bus 7 | M10 — 2, 5 | OI | Y30 + | Release |
| | P10 | OI | Y10 + | SCF Signal Bus 6 |
| | M11 | | Y31 | GND |
| – Data Out Bus 15 | P11 — 2 | OI | Y11 + | SCF Signal Bus 14 |
| | M12 | OI | Y32 + | SCF Signal Bus 7 |
| – Data Out Bus P0 | P12 — 2, 5 | | Y12 | GND |
| – Data Out Bus P1 | M13 — 2 | OI | Y33 + | Exception |
| – Any Valid Lth | P13 — 2 | OI | Y13 + | SCF Signal Bus 15 |
| | S02 | 2, 5 | Z22 + | Data In P0 |
| | U02 | 2, 5 | Z02 + | Data In 0 |
| | S03 | 2, 5 | Z23 + | Data In 1 |
| + 5 Volts | U03 | | Z03 | GND |
| | S04 | 2, 5 | Z24 + | Data In 2 |
| – Pwr Seq Comp | U04 — 2 Pwr Ctrl Card | 2, 5 | Z04 + | Data In 3 |
| | S05 | 2, 5 | Z25 + | Data In 4 |
| + 5 Volts Ve | U05 — Pwr Ctrl Card | 2, 5 | Z05 + | Data In 5 |
| | S06 | | Z25 | GND |
| + SSCF Mck | U06 — 2 | 2, 5 | Z06 + | Data In 6 |
| | S07 | 2, 5 | Z27 + | Data In 7 |
| | U07 | 2, 5 | Z07 + | Data In P1 |
| | S08 | 2, 5 | Z28 + | Data In 8 |
| GND | U08 | | Z08 | GND |
| | S09 | 2 | Z29 + | Data In 9 |
| – SSCF Irpt | U09 — 2 | 2 | Z09 + | Data In 10 |
| | S10 | 2 | Z30 + | Data In 11 |
| | U10 | 2 | Z10 + | Data In 12 |
| | S11 | | Z31 | GND |
| | U11 | 2 | Z11 + | Data In 13 |
| | S12 | 5, 2 | Z32 + | Data In 14 |
| | U12 | 5, 2 | Z12 + | Data In 15 |
| | S13 | | Z33 | |
| | U13 | | Z13 | |

**Note:** *"2" indicates a signal is from/to SC2; "5" indicates a signal is from/to SC3; "OI" indicates a signal is from/to SCF signal bus.*

**Figure SC420-4. SC4 Card and Connector Signals**

| To SC6 Card Pin | To SC4 Card Signal Name | Pin | SSCF Card (SC5) | Pin | I/O or Processor Board Signal Name |
|---|---|---|---|---|---|
| B02 | + SCF Signal Bus P0 < > | W22 | | B02 | – SCF Signal Bus 0 < > |
| D02 | + CR-1 < > | W02 | | D02 | – IR/B1-8 < |
| B03 | GND | W23 | | B03 | + 4 MHz Osc |
| D03 | + CR-2 < > | W03 | | D03 | + 5 Volts |
| B04 | + Ch Grant > | W24 | | B04 | – Parity Valid < |
| D04 | GND | W04 | | D04 | – IR/B1-9 < |
| B05 | + IPR < | W25 | | B05 | – IRR (Hw) < |
| D05 | + SCF Signal Bus P1 < > | W05 | | D05 | – SCF Signal Bus 8 < > |
| B06 | + I/O Reset > | W26 | | B06 | – 5 Volts (Unused) |
| D06 | + I/O Tag > | W06 | | D06 | – Valid Byte 1 < |
| B07 | GND | W27 | | B07 | – IR/B1-10 < |
| D07 | + End of Chain < | W07 | | D07 | – Valid Halfword < |
| B08 | + SCF Signal Bus 0 < > | W28 | | B08 | – SCF Signal Bus 1 < > |
| D08 | GND | W08 | | D08 | GND |
| B09 | + Halt > | W29 | | B09 | – Valid Byte 0 < |
| D09 | + Valid Byte 0 < | W09 | | D09 | – End of Chain < |
| B10 | + SCF Signal Bus 8 < > | W30 | | B10 | – SCF Signal Bus 9 < > |
| D10 | + SSCF Reset > | W10 | | D10 | – Exception < |
| B11 | GND | W31 | | B11 | + 8.5 Volts (Unused) |
| D11 | + SCF Signal Bus 1 < > | W11 | | D11 | – SCF Signal Bus 2 < > |
| B12 | | W32 | | B12 | – Modifier < |
| D12 | GND | W12 | | D12 | |
| B13 | | W33 | | B13 | + Ve > |
| D13 | + ML SCF Signal Bus 9 < > | W13 | | D13 | – SCF Signal Bus 10 < > |
| B02 | + TC > | X22 | | G02 | – TD > |
| D02 | + Xmit Ctrl > | X02 | | J02 | – Ch Request Low < |
| B03 | GND | X23 | | G03 | – Ch Request Med < |
| D03 | + Hold Pwr On > | X03 | | J03 | + 5 Volts |
| B04 | + SCF Signal Bus 2 < > | X24 | | G04 | – SCF Signal Bus 3 < > |
| D04 | GND | X04 | | J04 | – IR/B1-11 < |
| B05 | + SCF Signal Bus 10 < > | X25 | | G05 | – SCF Signal Bus 11 < > |
| D05 | + Valid Byte 1 < | X05 | | J05 | – I/O Tag (Hw) > |
| B06 | + Release Req < | X26 | | G06 | – 5 Volts (Unused) |
| D06 | + TD > | X06 | | J06 | – Halt > |
| B07 | GND | X27 | | G07 | – IR/B1-12 < |
| D07 | + SCF Signal Bus 3 < > | X07 | | J07 | – SCF Signal Bus 4 < > |
| B08 | + SCF Signal Bus 11 < > | X28 | | G08 | – SCF Signal Bus 12 < > |
| D08 | GND | X08 | | J08 | GND |
| B09 | + SCF Signal Bus 4 < > | X29 | | G09 | – SCF Signal Bus 5 < > |
| D09 | + SCF Signal Bus 12 < > | X09 | | J09 | – SCF Signal Bus 13 < > |
| B10 | + Valid Halfword < | X30 | | G10 | – TA > |
| D10 | + TA > | X10 | | J10 | – TC > |
| B11 | GND | X31 | | G11 | + 8.5 Volts (Unused) |
| D11 | + Parity Valid < | X11 | | J11 | – Byte Tag > |
| B12 | + CRP-4 < > | X32 | | G12 | – System Reset > |
| D12 | GND | X12 | | J12 | – Valid Byte 1 (B) < |
| B13 | + CRP-2 < > | X33 | | G13 | – I/O Tag (B) > |
| D13 | + CRP-1 < > | X13 | | J13 | – IRR (B) < |

**Figure SC420-5. SC5 and SC6 Card and Connector Signals**

| To SC6 Card Pin | To SC4 Card Signal Name | Pin | SSCF Card (SC5) | Pin | I/O or Processor Board Signal Name |
|---|---|---|---|---|---|
| B02 | + SCF Signal Bus 5 < > | Y22 | | M02 | – SCF Signal Bus 6 < > |
| D02 | + Outbound Ctrl > | Y02 | | P02 | – Ch Grant Low > |
| B03 | GND | Y23 | | M03 | |
| D03 | + CRP-8 < > | Y03 | | P03 | + 5 Volts |
| B04 | + IRR < | Y24 | | M04 | – Ch Grant High > |
| D04 | GND | Y04 | | P04 | – IR/B1-13 < |
| B05 | + Power Drop < | Y25 | | M05 | – Ch Request High < |
| D05 | + Byte Tag > | Y05 | | P05 | – IR/B1-14 < |
| B06 | – All SSCF Sel'd < | Y26 | | M06 | – 5 Volts (Unused) |
| D06 | + SCF Signal Bus 13 < > | Y06 | | P06 | – SCF Signal Bus 14 < > |
| B07 | GND | Y27 | | M07 | – IR/B1-15 < |
| D07 | | Y07 | | P07 | – IR/B1 P1 < |
| B08 | + SSCF Irpt < | Y28 | | M08 | – Release Req < |
| D08 | GND | Y08 | | P08 | GND |
| B09 | + SSCF MC Irpt < | Y29 | | M09 | |
| D09 | + Modifier < | Y09 | | P09 | – Release > |
| B10 | + Release > | Y30 | | M10 | – IPR < |
| D10 | + SCF Signal Bus 6 < > | Y10 | | P10 | – SCF Signal Bus 7 < > |
| B11 | GND | Y31 | | M11 | + 8.5 Volts (Unused) |
| D11 | + SCF Signal Bus 14 < > | Y11 | | P11 | – SCF Signal Bus 15 < > |
| B12 | + SCF Signal Bus 7 < > | Y32 | | M12 | – SCF Signal Bus P0 < > |
| D12 | GND | Y12 | | P12 | – Ch Grant Med > |
| B13 | + Exception < | Y33 | | M13 | – 10 MHz to Adapt > |
| D13 | + SCF Signal Bus 15 < > | Y13 | | P13 | – SCF Signal Bus P1 < > |
| B02 | | Z22 | | S02 | |
| D02 | GND | Z02 | | U02 | |
| B03 | + SSCF Stat A0 < > | Z23 | | S03 | |
| D03 | + SSCF Stat A8 < > | Z03 | | U03 | + 5 Volts |
| B04 | – SSCF Stat A1 < > | Z24 | | S04 | – Turn Pwr On > |
| D04 | – SSCF Stat A9 < > | Z04 | | U04 | |
| B05 | – SSCF Stat A2 < | Z25 | | S05 | + 5 Volts Ve < |
| D05 | – SSCF Stat A10 > | Z05 | | U05 | + 5 Volts Vctrl < |
| B06 | + SSCF Stat A3 < | Z26 | | S06 | – 5 Volts (Unused) |
| D06 | + SSCF Stat A11 > | Z06 | | U06 | |
| B07 | GND | Z27 | | S07 | |
| D07 | | Z07 | | U07 | |
| B08 | | Z28 | | S08 | |
| D08 | GND | Z08 | | U08 | GND |
| B09 | + SSCF Stat A4 < | Z29 | | S09 | |
| D09 | + SSCF Stat A12 > | Z09 | | U09 | |
| B10 | + SSCF Stat A5 < | Z30 | | S10 | |
| D10 | + SSCF Stat A13 > | Z10 | | U10 | |
| B11 | + SSCF Stat A6 < | Z31 | | S11 | + 8.5 Volts (Unused) |
| D11 | + SSCF Stat A14 > | Z11 | | U11 | |
| B12 | + SSCF Stat A7 < | Z32 | | S12 | |
| D12 | + SSCF Stat A15 > | Z12 | | U12 | |
| B13 | GND | Z33 | | S13 | |
| D13 | – SC6 Card Present < | Z13 | | U13 | |

## SC430 SCF Cable Connections

Sections SC431 and SC432 are charts that show the 8100 SCF cable routing. The SCC designation indicates the pseudo numbering for the SCF cables.

### *SC431 SCF Internal Cable Connections*

| 8130 Internal Without System Expansion Feature | | | | |
|---|---|---|---|---|
| From | Through | Through | To | Cable |
| A2G2W | ——— | ——— | A2H2W | SCC 19 |
| A2G2X | ——— | ——— | A2H2X | SCC 20 |
| A2G2Y | ——— | ——— | A2H2Y | SCC 21 |
| A2Y4 | ——— | ——— | A1Z4 | SCC 22 |
| A2Y5 | ——— | ——— | A1Z5 | SCC 23 |
| A2Y6 | ——— | ——— | A1Z6 | SCC 24 |
| A2A5 | ——— | ——— | B1A5 | SSC 7 |
| A2Z1 | ——— | ——— | B1A2 | SSC 11 |

| 8130 Internal With System Expansion Feature | | | | |
|---|---|---|---|---|
| From | Through | Through | To | Cable |
| A2G2W | ——— | ——— | A2F2W | SCC 1 |
| A2G2X | ——— | ——— | A2F2X | SCC 2 |
| A2G2Y | ——— | ——— | A2F2Y | SCC 3 |
| A2A2 | ——— | ——— | T-E1 | SCC 4 |
| A2A3 | ——— | ——— | T-E2 | SCC 5 |
| A2A4 | ——— | ——— | T-E3 | SCC 6 |
| A2Y1 | ——— | ——— | A1Z1 | SCC 8 |
| A2Y2 | ——— | ——— | A1Z2 | SCC 9 |
| A2Y3 | ——— | ——— | A1Z3 | SCC 10 |
| A2Y4 | ——— | ——— | A1Z4 | SCC 22 |
| A2Y5 | ——— | ——— | A1Z5 | SCC 23 |
| A2Y6 | ——— | ——— | A1Z6 | SCC 24 |
| A2A5 | ——— | ——— | B1A5 | SCC 7 |
| A2Z1 | ——— | ——— | B1A2 | SCC 11 |

| 8140 Model A Internal | | | | |
|---|---|---|---|---|
| From | Through | Through | To | Cable |
| A1A2W | ——— | ——— | A2A2W | SCC 1 |
| A1A2X | ——— | ——— | A2A2X | SCC 2 |
| A1A2Y | ——— | ——— | A2A2Y | SCC 3 |
| T-D1 | A2C2W | A2D2W | T-E1 | SCC 4 |
| T-D2 | A2C2X | A2D2X | T-E2 | SCC 5 |
| T-D3 | A2C2Y | A2D2Y | T-E3 | SCC 6 |

| 8101 Internal | | | | |
|---|---|---|---|---|
| From | Through | Through | To | Cable |
| T-D1 | A1A2W | ——— | T-E1 | SCC 7 |
| T-D2 | A1A2X | ——— | T-E2 | SCC 8 |
| T-D3 | A1A2Y | ——— | T-E3 | SCC 9 |
| T-D1 | ——— | A2A2W | T-E1 | SCC 7 |
| T-D2 | ——— | A2A2X | T-E2 | SCC 8 |
| T-D3 | ——— | A2A2Y | T-E3 | SCC 9 |
| T-D1 | A1A2W | A2A2W | T-E1 | SCC 7 |
| T-D2 | A1A2X | A2A2X | T-E2 | SCC 8 |
| T-D3 | A1A2Y | A2A2Y | T-E3 | SCC 9 |

**Note:** *The three cable locations depend on the 8101 features installed, and are always SCCs 7, 8, and 9.*

### *SC432 SCF External Cable Connections*

| 8130/8140 External | | | | |
|---|---|---|---|---|
| From | Through | Through | To | Cable |
| T-D1 | ——— | ——— | T-E1 | SCC 16 |
| T-D2 | ——— | ——— | T-E2 | SCC 17 |
| T-D3 | ——— | ——— | T-E3 | SCC 18 |

## SC440 Switches

### *SC441 SC1 Card Switches*

(See SC111 for location of SC1 card.) The SC1 card contains the switches used to specify the primary mode IPL parameters, and are fixed at hex 4380.

**Note:** ***If these switch settings are changed, DPPX and DPCX do not perform a primary mode IPL properly.***

Figure SC441-2 shows the switch settings as they relate to the IPL parameter bits specified in Figure SC441-1, and Figure SC441-3 shows their physical location.

**How To Test the IPL Parameter Switch Settings**

1. Press Reset/IPL at the BOP.
2. At the 0200 display message, press Enter Data.
3. At the 0201 display message, enter "0001" and press Enter Data.

The contents of the IPL parameter switches are then displayed in the BOP, and the value should be hex 4380.

| Bit | Meaning |
|---|---|
| 0 | Reserved |
| 1 | Auto restart primary IPL — If on, executes a primary IPL using the parameters specified in the PSCF IPL parameter switches. If off, terminates the IPL with 0122 in the BOP display. |
| 2 | Extended test — Specifies manual mode testing parameters according to DPPX or DPCX, and also according to whether IPL occurred either from a power-on sequence or from the IPL pushbutton. Refer to CP523 "Manual Mode IPL and Its Testing Options" in Chapter 2 for a detailed explanation. |
| 3 | Initialize storage — Refer to bit 2 for explanation. |
| 4—7 | IPL device type<br>0001 = diskette<br>0011 = disk<br>1111 = maintenance device |
| 8—15 | IPL device address according to the following:<br>8—11 = SSCF address<br>12—15 = device address<br>80 = Disk storage, 8130 or 8140A<br>84 = Disk storage, 8140B<br>90 = Disk storage, First 8101<br>A0 = Disk storage, Second 8101<br>B0 = Disk storage, Third 8101<br>C0 = Disk storage, Fourth 8101<br>87 = Diskette storage, 8130 or 8140<br>97 = Diskette storage, First 8101<br>A7 = Diskette storage, Second 8101<br>B7 = Diskette storage, Third 8101<br>C7 = Diskette storage, Fourth 8101 |

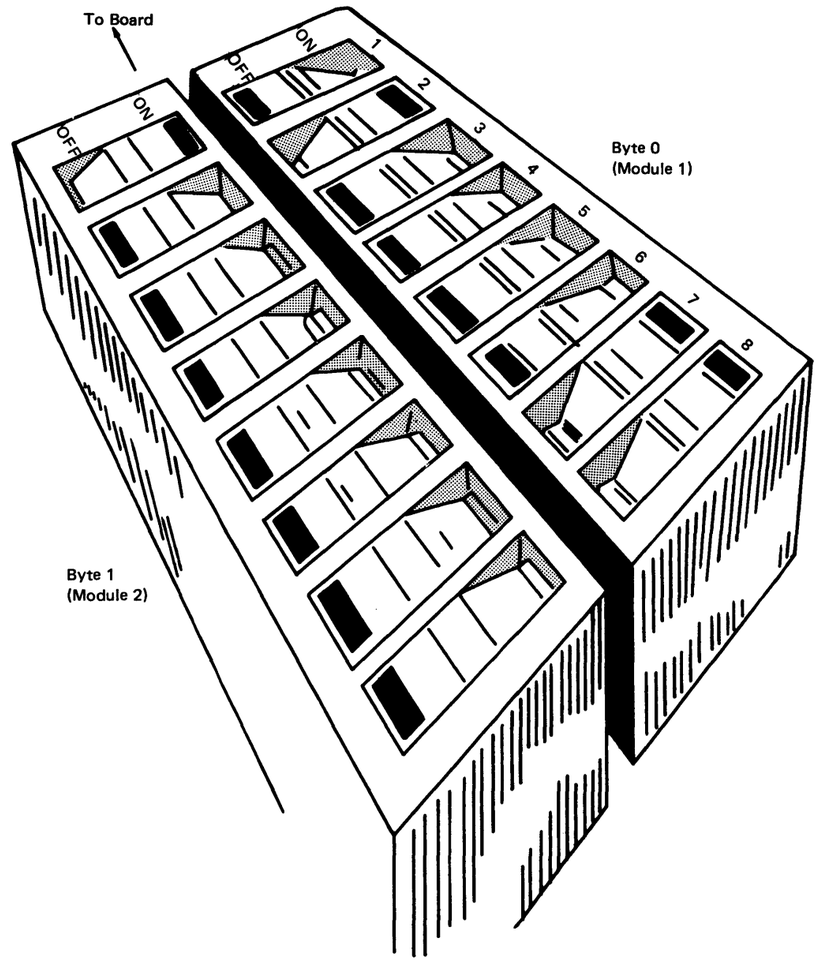
**Figure SC441-1. IPL Parameter Bit Descriptions**

| IPL Bit Number | Switch Number | Switch Module | Initial Setting | Description |
|---|---|---|---|---|
| 0 | 1 | 1 | On | Reserved |
| 1 | 2 | 1 | Off | Auto restart primary IPL |
| 2 | 3 | 1 | On | Extended test |
| 3 | 4 | 1 | On | Initialize storage |
| 4 | 5 | 1 | On | IPL device type |
| 5 | 6 | 1 | On | IPL device type |
| 6 | 7 | 1 | Off | IPL device type |
| 7 | 8 | 1 | Off | IPL device type |
| 8 | 1 | 2 | Off | IPL device address |
| 9 | 2 | 2 | On | IPL device address |
| 10 | 3 | 2 | On | IPL device address |
| 11 | 4 | 2 | On | IPL device address |
| 12 | 5 | 2 | On | IPL device address |
| 13 | 6 | 2 | On* | IPL device address |
| 14 | 7 | 2 | On | IPL device address |
| 15 | 8 | 2 | On | IPL device address |

**Note:** *The signals from the IPL switch register are inverted before being used, so the initial setting as indicated in the figure is read as 4380 at the IPL register.*

*Off if 8140 Model B

**Figure SC441-2. SC1 Card IPL Switch Settings**




**Note:** *Modules 1 and 2 are rocker switches. Pressing down the right side turns the switch on, and pressing the left side turns them off. (4380 shown)*

**Figure SC441-3. SC1 Card IPL Switch Module Locations**

## *SC442 SC5 Card Switches*

Figures SC442-1 and SC442-2 show the SC5 card switches, locations, and meanings. (See SC111 for locations of SC5 cards.)

- The ten Module 1 switches specify the SSCF address, release request signal propagation, tag delay, and channel request priority
- The eight Module 2 switches each enable use of an interrupt request bus to turn on release request.

Refer to the configuration table shown in SC113 to relate the following explanation of the SC5 card (SSCF) switch settings to the SCF physical addressing scheme.

| SSCF Board Location | Module 1 Switches and Settings | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| 8130/40 A2 | ON | OFF | OFF | OFF | ON | OFF | ON | OFF | ON | OFF |
| 8140 C2 | OFF | ON | OFF | ON | ON | OFF | ON | ON | OFF | ON |
| First 8101 A1* | OFF | OFF | OFF | ON | ON | OFF | OFF | OFF | ON | ON |
| First 8101 A2** | ON | OFF | OFF | ON | ON | OFF | OFF | ON | ON | ON |
| Second 8101 A1* | OFF | OFF | ON | OFF | ON | OFF | OFF | OFF | ON | OFF |
| Second 8101A2** | ON | OFF | ON | OFF | ON | OFF | OFF | ON | ON | OFF |
| Third 8101 A1* | OFF | OFF | ON | ON | ON | OFF | OFF | OFF | OFF | ON |
| Third 8101 A2** | ON | OFF | ON | ON | ON | OFF | OFF | ON | OFF | ON |
| Fourth 8101 A1* | OFF | ON | OFF | OFF | ON | OFF | OFF | OFF | OFF | OFF |
| Fourth 8101 A2** | ON | ON | OFF | OFF | ON | OFF | OFF | ON | OFF | OFF |
| 8809 Model 1B | OFF | ON | ON | ON | ON | OFF | ON | ON | OFF | OFF |

This figure shows settings for switches 7–10 for 8101 A1 boards containing only communications features and 8101 A2 boards containing only a file feature (see * and **).

*When adding the display and printer feature to any 8101 A1 or B1 board, switches 7–10 are set to ON, ON, ON, OFF (hex E) for the first adapter and to ON, ON, ON, ON (hex F) tor the second adapter (8140 model BXX systems only).

**When adding the Magnetic Tape Feature to any 8101 A2 board, switches 7–10 are set to ON, OFF, ON, ON (hex B). When adding the Diskette Storage Feature without the Magnetic Tape Feature to any 8101 A2 board, switches 7–10 are set to ON, OFF, OFF, ON (hex 9). Any board with only the SSCF card has switches 7–10 set to OFF.

**Figure SC442-1. SC5 Card Module 1 Switch Settings Relating to SSCF Board Locations**

### SC5 Card Module 1 Switch Description

Switches 1–4 determine the value of the leftmost hexadecimal digit of the SSCF physical address. The rightmost value is always hex 8. The PSCF physical address is fixed to hex 08. To address any SSCF, the PSCF and SSCF physical addresses are specified. Therefore, to address the SSCF contained in the fourth 8101 A2 board, for example, requires a PAPA designation of hex 08C8. Switches 1–4 specify the "C". The 08 and 8 are always the same.

Switches 6, 7, 8, 9, 10, and 5 in that order determine the first six bits of the first Op field of the table in SC113, and the last two are always zero. Therefore, the Op value for the SSCF contained in the fourth 8101 A2 board is hex 24. See Figure SC442-2 for the SC5 card module locations.
The following shows Module 1 switch assignments:

| Function | Switch | Switch Position |
|---|---|---|
| SSCF address | 1–4 | Dependent on board location |
| Release request | 5 | Always on |
| Tag delay | 6 | Always off |
| Channel request priority | 7–10 | Fixed according to system configuration |

### SC5 Card Module 2 Switch Description

The Module 2 switches enable the BSC/S-S communications adapters, when in BSC mode, to send a release request signal to the processor. The table below shows the relationship between the communications adapter physical addresses and the switch numbers. When a BSC/S-S adapter is in BSC mode, the switch corresponding to its physical address must be on.

| Communications Adapters Addresses | | | | SSCF Card |
|---|---|---|---|---|
| 8140B | 8130 | 8140A | 8101* | Module 2 Switch No. |
| 50 80 | | | X0 | 1 |
| 51 81 | 81 | 81 | X1 | 2 |
| 52 82 | 82 | 82 | X2 | 3 |
| 53 83 | 83 | 83 | X3 | 4 |
| 5C | 84 | | XC | 5 |
| 5D | 85 | | XD | 6 |
| 5E | 86 | | XE | 7 |
| 5F | | | XF | 8 |

*X = 1, 2, 3, or 4 depending on which 8101 the communications adapters are in.

Module 1 is the 10-position switch module; Module 2 is the 8-position switch module.

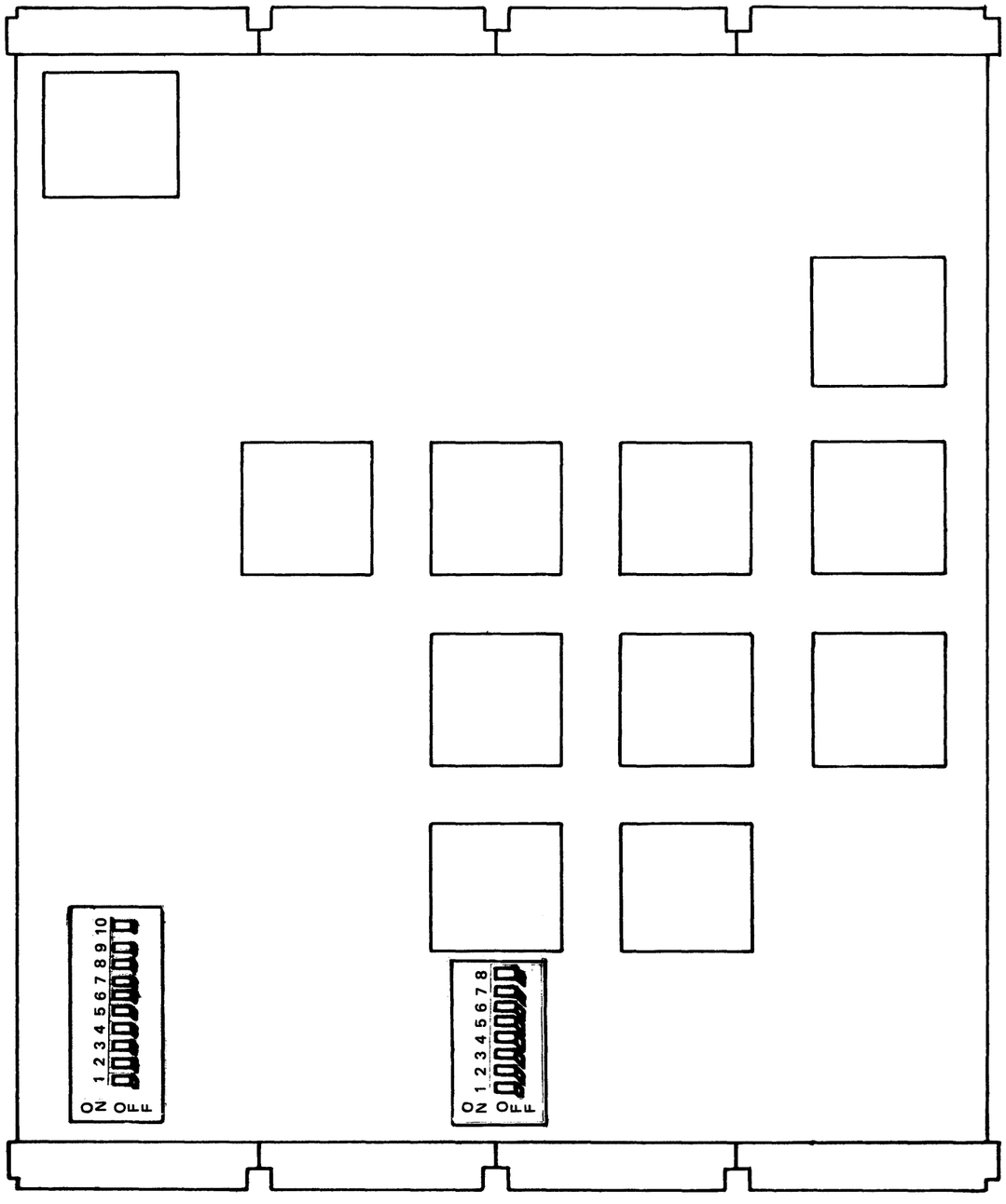
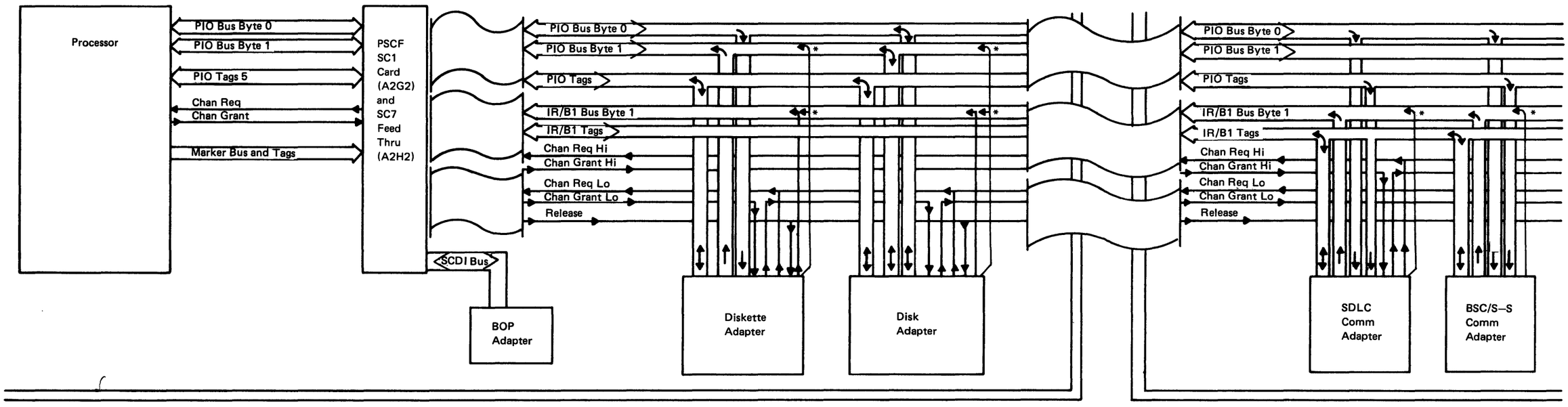



Figure SC442-2. SC5 Card Switch Module Locations

## SC450 8130/8140 Detailed Data Flow

Figures SC450-1 through SC450-7 show the SCF data flow and timing, as well as the data flow within each PSCF and SSCF card.




**Note:** ***This figure is for the 8130 without Expansion feature; see SC401 for other configurations.***

*Interrupt Connections for 8130 without Expansion Feature

| Adapter Type | Wired To | Interrupt Level |
|---|---|---|
| Bisync CCA | IR/B1 Bus Bit 1 | 1 |
| Start/Stop CCA | IR/B1 Bus Bit 3 | 3 |
| SDLC HPCA | IR/B1 Bus Bit 3 | 3 |
| Diskette | PIO Bus 1 Bit 4 | 4 |
| Disk | PIO Bus 1 Bit 4 | 4 |

**Figure SC450-1. SCF Signal Bus Data Flow Diagram**

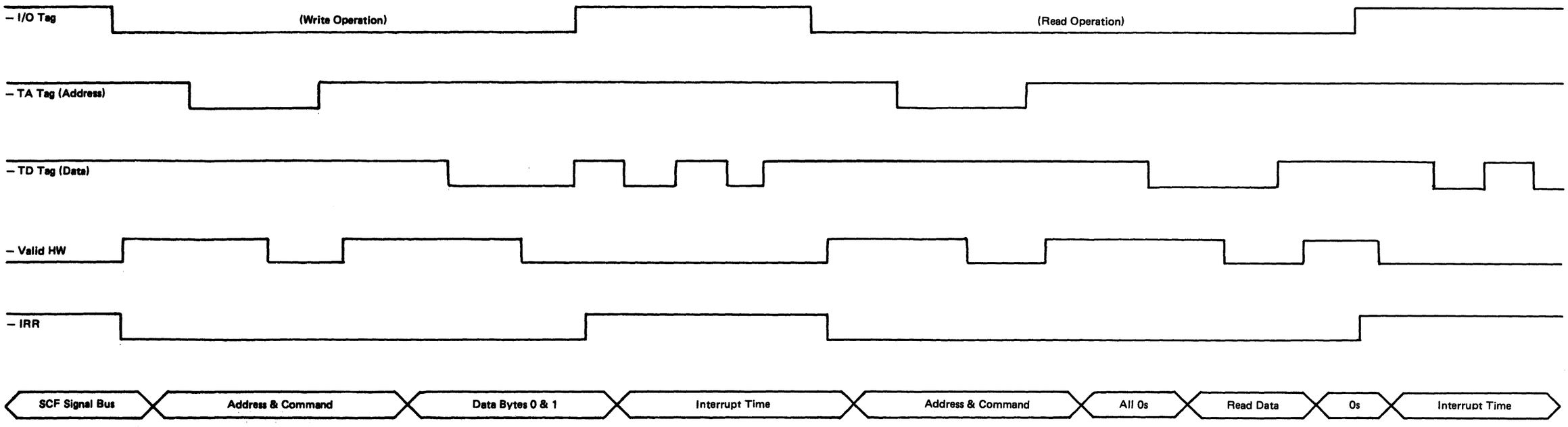



**Figure SC450-2. SCF Timing Chart for Read and Write Operations**

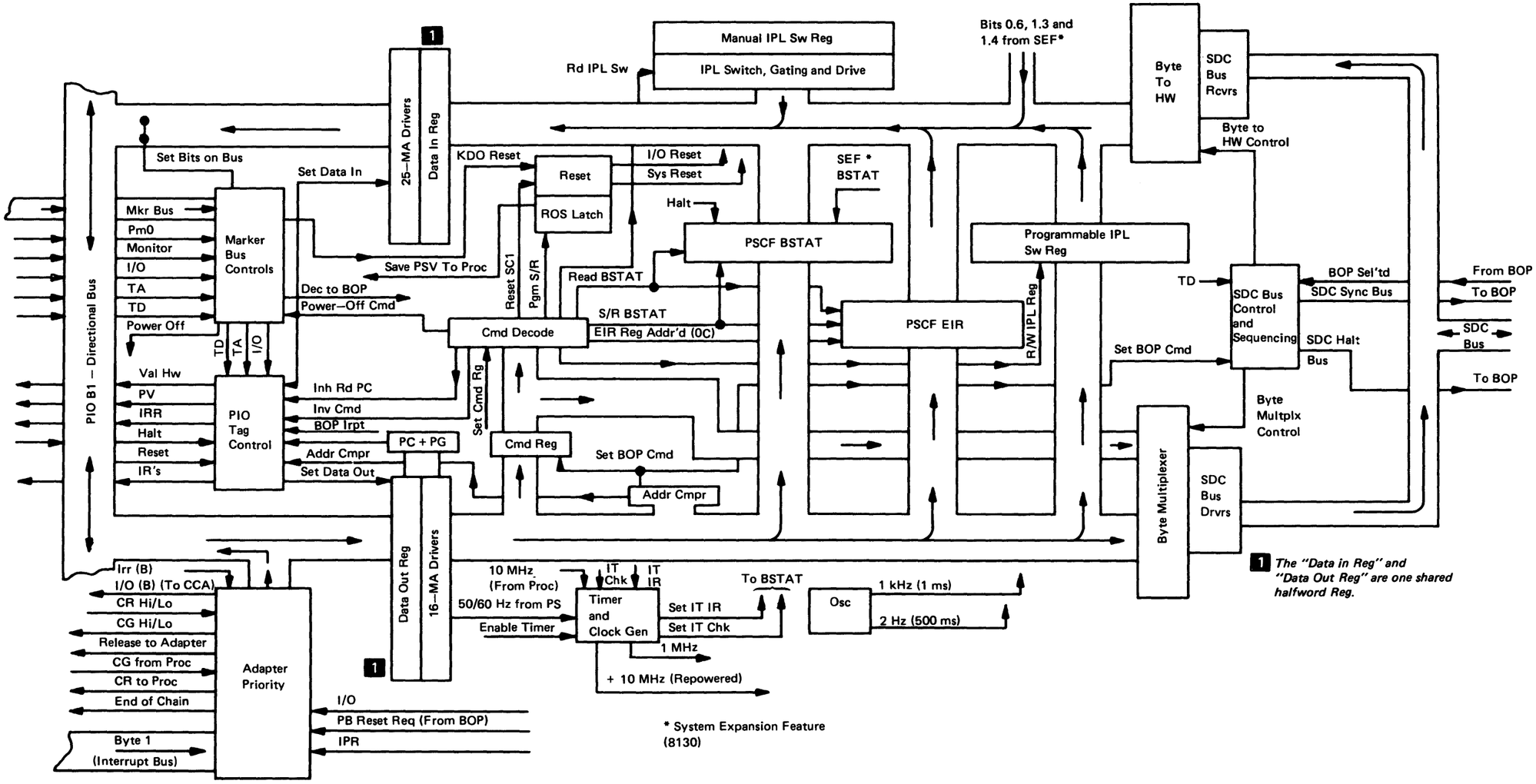



**Figure SC450-3. SCF SC1 Card Data Flow**

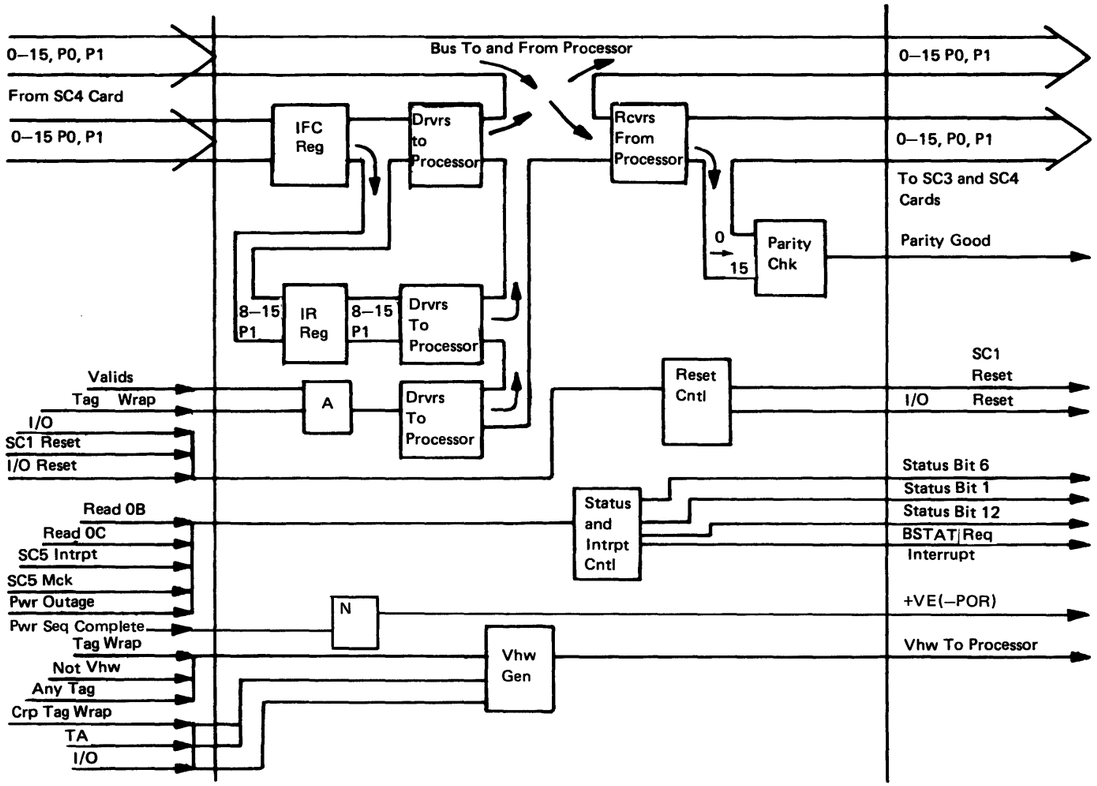



**Figure SC450-4. SCF SC2 Card Data Flow**

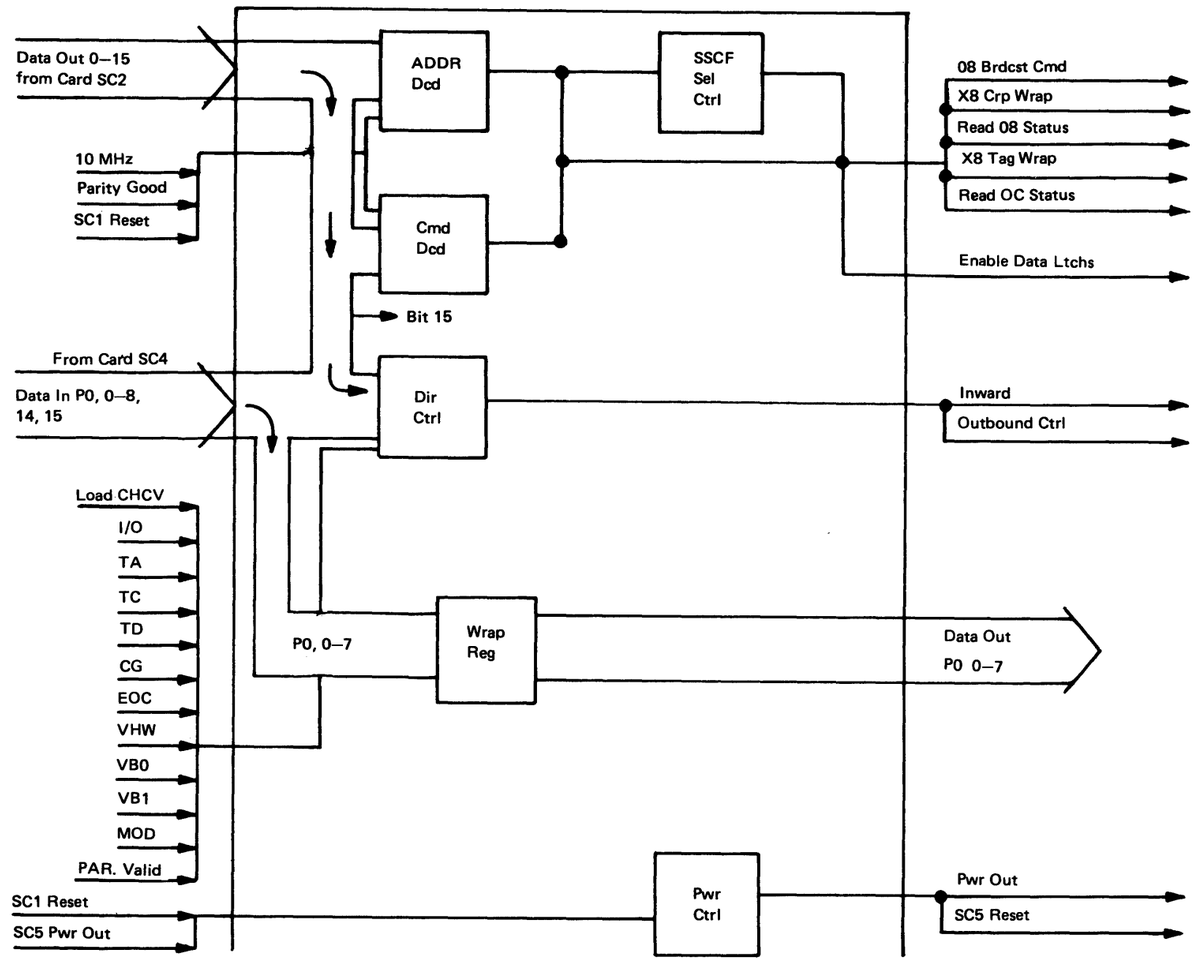



**Figure SC450-5. SCF SC3 Card Data Flow**

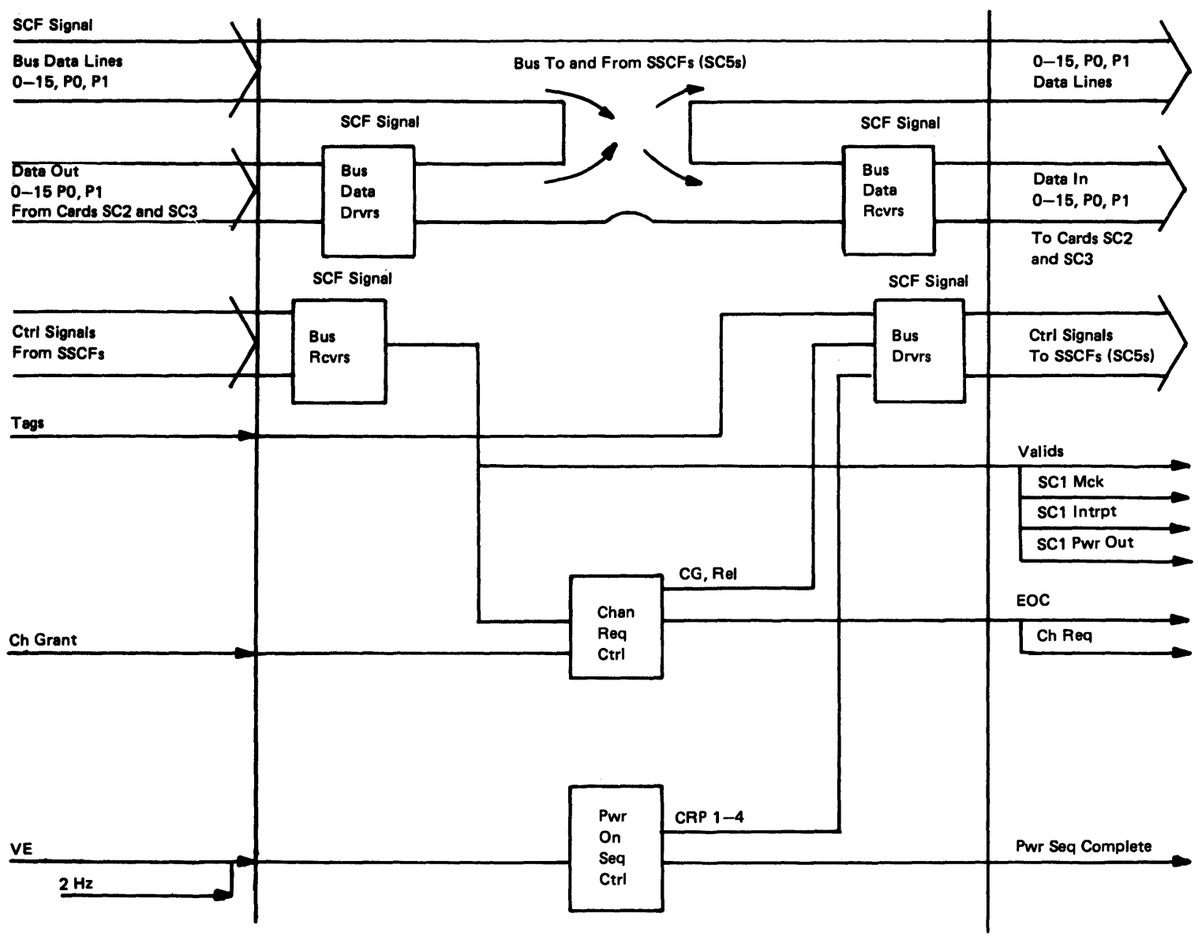
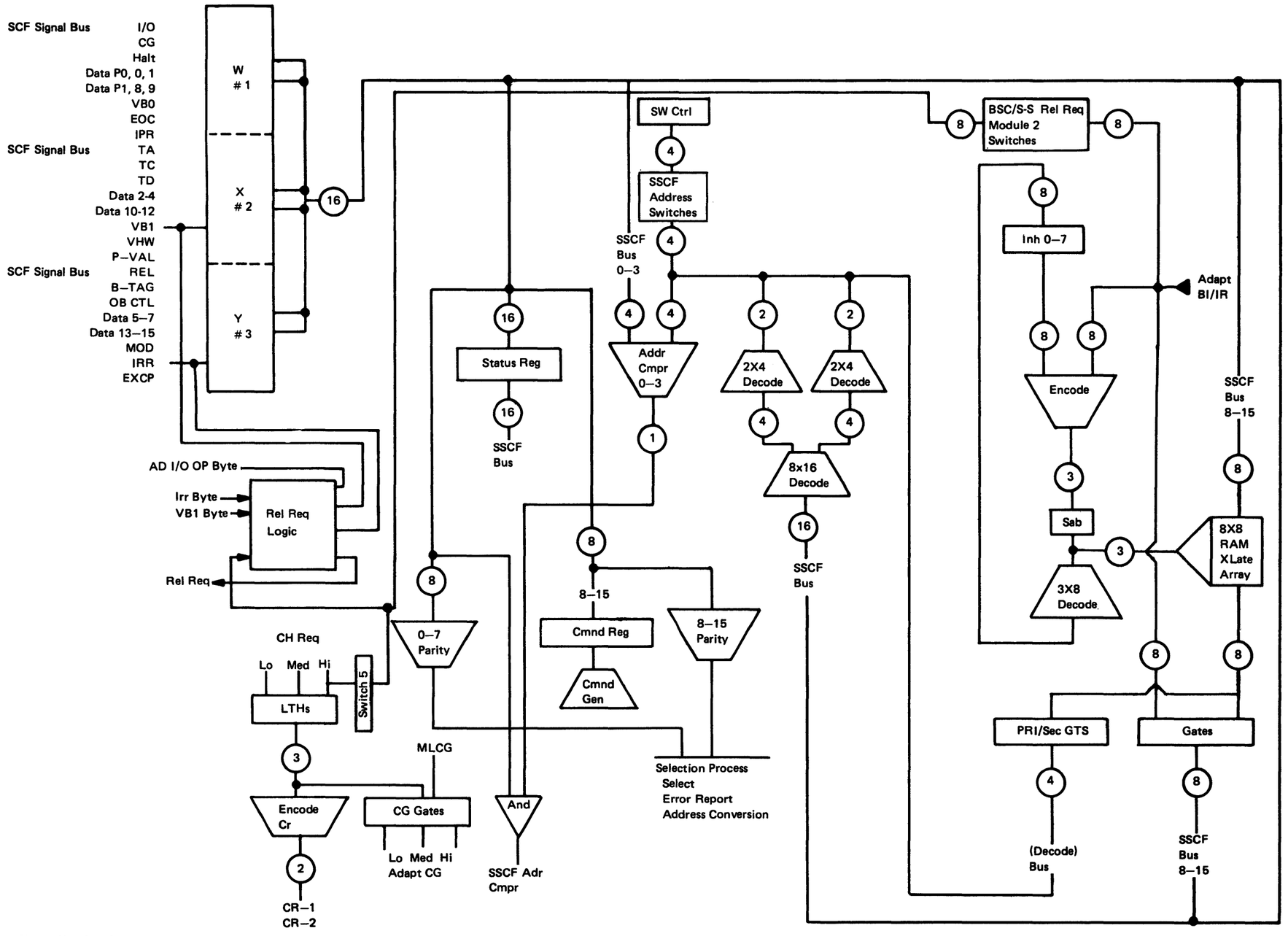



**Figure SC450-6. SCF SC4 Card Data Flow**




**Note:** *Numbers in circles specify number of bits on bus.*

**Figure SC450-7. SCF SC5 Card Data Flow**

## SC460 SCF Detailed Description

The SCF provides the logical attachment for I/O devices and communications control, performs 8101 power-on signal sequence control, and also provides several programmable functions.

The SCF hardware responds to addresses hex 08 (SCF Level 3), hex 0C (SCF Level 0), hex 09 (BOP), and hex 0A (EFP, if installed) for information transfer. It can request interrupts on Level 3 fixed assignment, which can be programmed to occur on Level 0. Level 3 interrupt requests can occur from:

- The BOP
- The 100-ms interval timer
- A control program
- The SCF adapter

Power can be turned off with a command to the Level 3 address after first enabling the power-off circuitry with a KDO command.

The physical location and functions performed depend on the processor model.

- The basic 8140 Processor provides all functions.
- The basic 8130 requires addition of the System Expansion Feature to perform those functions equivalent to the 8140.

The location and number of these cards also vary between the 8130 and 8140 because of physical board configuration. The PSCF cards and one SSCF card reside in the processor boards. Up to six more SSCF cards can reside in 8101 boards, with one or two in each 8101, depending on its I/O device configuration.

**Note:** *For purposes of discussion in this section, the terms "PSCF" and "SSCF" are used. "PSCF" refers to those functions performed by the SC1 card, while "SSCF" refers to those functions performed by the SC5 card. The SC2, SC3, and SC4 cards control interrupt priority, while the SC6 card, used only in the 8130 with the System Expansion Feature, functions as a signal line terminator.*

For physical differences, see section SC110; for functional differences, refer to the detailed data flow contained in section SC450; for operational differences, refer to the following information.

### *SC461 Primary System Control Facility (PSCF)*

The PSCF and SSCF each provide certain functions and also logically combine to provide others. The following explains the functions provided by the PSCF:

**Power Sequence Control.** As the 8130/8140 powers up, signals from the PSCF provide power sequencing to the attached devices. The sequencing order for attached 8101s depends on the setting of the channel request priority (CRP) switches of the SSCF, in the order of the highest CRP value first, and the sequence bypasses any 8101 not powered on. The complete sequence occurs in approximately 64 seconds.

**Operator Panel to Channel Operations.** The PSCF provides the method of information transfer with both operator panels (BOP and Expanded Function on the 8140) and the channel for processor operation. The panels use PIO halfword instructions for address and data transfer, and the panel adapter transmits any panel error conditions to the PSCF, which suppresses any response to the channel. The PSCF also parity checks operator panel address and data transfers before initiating any PIO operation to it, and does not initiate panel operation if errors occur.

**Clocked Interrupt.** The processor receives an interrupt every 100 ms, depending on PSCF BSTAT bits 8, 9, and 14. The interrupt occurs either on Level 0 or 3, according to the PSCF EIR bit 1 value. The program controls the timer that generates this clocked interrupt.

**Programmed IPL Parameters.** The PSCF has a programmable register to contain IPL parameters, and the PSCF BSTAT bit 1 determines its use when performing a program-initiated IPL. The bit meanings are identical to those contained in the IPL switches. Refer to SC441 for IPL switch meanings.

**IPL Switches.** Sixteen PSCF hardware switches provide a source for IPL parameters when normal register parameters are not available. The bit meanings are the same as the programmed IPL register, and determine:

1. The IPL device type.
2. Whether an automatic restart primary IPL sequence can be performed.
3. Whether extended bringup tests should be executed.
4. Whether storage should be initialized to FFs with correct parity.

Refer to SC441 for IPL parameter meanings.

**BOP and PSCF Level Assignments.** Processor board wiring assigns Level 3 to the BOP and the PSCF, which can be swapped to 0 by altering the value of the PSCF EIR bit 1 value, as DPPX and DPCX use the fixed value assignment. The expanded panel always operates on Level 0 and cannot be altered.

**Error Detection.** PSCF logic provides parity error detection for BOP and EFP operations as well as for its own functions. These conditions are indicated in the PSCF EIR.

**KDO Instruction Decode for PSCF Operations.** The marker bus decodes processor-to-PSCF KDO instructions, which perform I/O resets, system resets, enable power-off, and other operations used to test the SCF hardware.

When a program executing in either master or supervisor mode performs two sequential Control Direct Out (KDO) instructions, PSCF logic decodes the second KDO to perform certain control functions. The I-field of the first KDO must be 0, and the I-field value (from 0 to 7) of the second determines the function to be performed. These functions are: enable PSCF decodes, I/O reset, set I/O interface check, system reset, set panel check, force bits 2 and 10 to 1, force parity bits to 1, and enable system power-off.

**Reset Control.** Reset facilities for the SCF, PSCF, I/O devices, and the system, as well as selective programming resets are provided by PSCF logic. The PSCF responds to the following reset conditions:

Power-on reset from the power supply

IPL Pushbutton — Reset from panel

Marker bus — System reset

Marker bus — I/O reset

PIO command — Reset control

**PSCF Priority Assignments for Adapters.** The PSCF services adapters according to the following priority, and uses additional lines from the PSCF to the adapters to accomplish this:

| Priority | Class | Type | Example |
|---|---|---|---|
| First | Real time services | PIO | |
| Second | Unbuffered, overrunable | CHIO | SDLC communications |
| Third | Unbuffered, overrunable | PIO | BSC/S-S communications |
| Fourth | Buffered, non-overrunable | CHIO | Disk storage |
| Fifth | Buffered, non-overrunable | PIO | Basic Operator Panel |

**Programmed SCF Function Control.** The PSCF controls several functions of the SCF through specific bits in the SSCF status registers.

## *SC462 Secondary System Control Facility (SSCF)*

The following paragraphs explain the functions provided by the SSCF.

**I/O Group Addresses.** Hardware switches are used to determine the high-order four bits of the PIO address for each SSCF and its attached devices. These are fixed assignments; although you can change them at the user's request, it is not recommended, as both DPPX and DPCX use the fixed assignment values for addressing.

Refer to Chapter 2, CP220, for SSCF addressing assignment values.

**Channel Request Priority (CRP) Switches.** The fixed channel request priority switch value determines which SSCF receives interrupt servicing with more than one request pending. The values are hex 0 to hex F with hex F being the highest priority. These are fixed assignments; although you can change them at the user's request, it is not recommended, as both DPPX and DPCX use the fixed assignment values for addressing.

Refer to Chapter 2, CP220, for CRP addressing assignment values, and to SC441 for the switch settings.

**Release Request Switch.** Each SSCF has a switch used to activate the release request signal to the PSCF. This signal occurs when a device assigned to the SSCF channel-hi priority chain generates a channel request to the SSCF. This switch is set to the On position; although you can change it at the user's request, it is not recommended because it can result in improper operation of devices on the channel.

**Interrupt Translation Array.** Each SSCF has eight 8-bit locations used to contain the programmable priority level and sublevel assignments for its attached devices. Bit zero is not used, bits 1—3 specify the priority level (0—7), and bits 4—7 specify the sublevel (0—F). The PSCF, SSCFs, BOP, and EFP cannot be assigned through the translation array as their addresses are fixed, but all other devices can be assigned address priority through the programmable array values.

Refer to Chapter 2, CP220, for the translation array addressing values.

## *SC463 PSCF and SSCF Combined Functions*

The 8100 requires both the PSCF and the SSCF to provide the following functions:

- Wrap Testing and the SCF Signal Path — Logic in each of these components provides a path to all attached I/O devices through the SCF signal bus. It also uses this path to check SCF signal bus integrity by using certain test commands.
- I/O Interrupt Presentation — All requests to the processor's channel facility require use of specific functions logically controlled by both the PSCF and SSCFs. Each performs certain operations required to present and prioritize the requests from both the hardware and software.

## *SC464 How the SCF Controls the BOP, EFP, and Adapter Bus*

The PSCF responds to the BOP and EFP halfword commands, and controls processor-to-BOP/EFP information transfer through the 9-bit (8 + parity) system direct control bus. It also transfers information on the SCF signal bus and decodes certain processor KDO commands, which perform I/O resets, system resets, enable power-off, and other operations that test SCF hardware. The PSCF does not accept an out-of-parity address and command, and generates an I/O timeout error for this condition.

The system direct control bus transfers commands and data to the BOP and EFP one byte at a time. It does not check these commands for validity, but does perform parity checking.

The SCF signal bus transfers commands and data to PSCF addresses hex 08 and hex 0C, where the PSCF then checks them for both parity and validity. Invalid commands cause an equipment check, while commands with invalid parity cause an I/O timeout. The PSCF EIR also indicates invalid parity.

### PSCF Command Functions

If the PSCF accepts a command to address hex 08, it performs one of the following operations:

- Reads, sets, and resets the PSCF BSTAT.
- Reads the IPL switch register.
- Reads and writes the programmed IPL register.
- Turns power off.
- Resets the adapter.
- Loads the wrap register.

If the PSCF accepts a command to address hex 0C, it performs one of the following operations:

- Reads, sets, and resets the error information register.
- Resets the adapter.
- Loads the wrap register

**Halt Signal**

This signal terminates a PIO operation to either the BOP, EFP, or PSCF address hex 08, and indicates that one of the following conditions occurred:

- The PSCF received an out-of-parity command, and the "valid" response for that command was suppressed to force an interface timeout.
- The PSCF, BOP, or EFP received an invalid command, and the "valid" response was suppressed to force an interface timeout.
- A PSCF address hex 08 write operation was in progress, and the PSCF sensed out-of-parity data on either the B0 or B1 data bus. The "valid" response for that data is suppressed to force an interface timeout.
- A PSCF address hex 08 read operation was in progress, and the channel received out-of-parity data from the PSCF. The PSCF has not signaled the channel to assign parity to the data, and the channel then activates the Halt signal to terminate the PIO operation.
- The BOP failed to respond to the initial signal from the PSCF to initiate a channel operation. The PSCF suppresses all responses to force an interface timeout.

Out-of-parity conditions sensed during read or write operations with the PSCF (address 08 or 0C) or the BOP (address 09) are recorded in the PSCF EIR, bits 4 (I/O Read Check) and 9 (I/O Write Check) to further define the error condition.

## SC500 SCF System Test and Internal I/O Bus Cable Change Procedures

### SC510 SCF System Test Procedure

The SCF System Routines provide the additional testing needed to test system functions. In most cases the interaction of multiple adapters is needed. Therefore, run all adapter test, PSCF tests, and SSCF tests (see SC210) before using these SCF system routines.

Note that:

1. Normally an SCF System Routine will use all of the same type adapter needed for the test.
2. Testing will continue until all of the same type adapter have been tested. Multiple errors in a single routine can occur but only one per group of adapters.
3. Each time a new adapter is used in a test, a progress indicator is presented to describe the routine number and the adapters used in the test.
4. The tests are run using the Free-Lance Utility. At 80BC, enter 69C; at 81BC, enter B. Routines 90, 91, 93, 94, 95, 96, 97, 98, 9A, 9C, 9E, A0, A1, AE, AF, B0, BF, and C0 will be run; if the correct type of adapters is not available, a resource error will occur.
5. I/O devices must be ready (tape unit power on and ready, diskette in place and door closed, display powered, etc).
6. 08RR messages that flash on the hand held display are progress indicators that show the addresses of the adapters being tested. If these messages remain on the display for more than 1 minute, a hard error has occurred. Record the message, depress the 'B' key to continue. If the tests will not continue, start over to see if the same error halt occurs.

If a system test failure occurs, refer to the System Error Message Chart, below for the appropriate action. Be sure to record all error messages before calling for assistance.

**System Error Message Chart**

| Msg | Description/Action |
|---|---|
| 08RR ADAD | Progress indicator.<br>RR Does not always indicate the test routine being executed when in an MI message (see SC231).<br>AD Is the physical address of the adapter or adapters being used for the test. Go to the MAPs and run the tests for these adapters. |
| 08XE RR27 AD | CHIO Data register error.<br>Call support center. |
| 08XE RR28 ADAD | Unexpected interruption during Release Request test.<br>Bysync Release Request switch not set. |
| 08XE RR29 ADAD | Control CHIO register setting in error.<br>Call support center. |
| 08XE RR2A ADAD | CHIO operation did not complete during Release Request test. Bad 'AD'. Replace first AD. Retry test. |
| 08XE RR2B ADAD | Lost CHIO interruption during Release Request test.<br>CCA Release Request switch not set off. |
| 08XE RR34 ADAD | CHIO Data register error during Release Request test.<br>Bad AD. Replace first AD. Retry test. |
| 08XE RR3E ADDR | RR = First R always B<br>Second R 0-F is storage volume number (high-order address byte of storage)<br>ADDR = Storage address within a volume<br>Replace storage card at failing address. |
| 08XE RR46 | Resource error. Could not find a needed adapter. |
| 08XE RR49 AD | Device error. Not ready. Make device ready and retry test. (If AD = file adapter, refer to Action Plan 7.) |
| 08XE RR4A AD | CHIO machine check during Release Request test.<br>Replace AD. Call support center.<br>RR = AE, B0-BF |
| 08XE RR4B AD | CHIO machine check.<br>If RR = 9X, replace AD; call support center.<br>If RR = AE or B0-BF, see error message format in routine B0-BF description. |
| 08XE RR4C AD | Modifier error. Refer to Action Plan 7. |
| 08XE RRFE AD | CHIO device failed to complete.<br>Call support center. |

1st AD = CHIO
2nd AD = Release Request adapter



### SC520 Procedure to Change SCF Internal I/O Bus Cables

1. Power down the system and remove power plugs from the AC power source.
2. At the unit it is necessary to change the flat white I/O cables, open the front cover and front subcover, reach under the top cover to disengage the bezel stud latches, and remove the bezel (see Figure SC520-1).
3. Reach under the top cover frame members to disengage the top cover stud latches. Lift front of top cover, push to rear and lift off.
4. Open the rear cover and rear subcover, remove the card retention covers over the cable or cables you wish to change, then unplug the cable or cables.
5. If possible, swing the logic gate to its most advantageous position and remove the cable retainers and cable from the gate. If this is impossible:
   a. First, get someone to help you.
   b. Then remove the logic gate from its hinges and set it on the floor of the unit, or out of the unit, as far from the 01T panel and as gently as possible to not damage the fans at the bottom of the gate.
   c. Remove the cable retainers and cable from the gate.
6. Swing the logic gate open and using a mirror continue to remove the same cable from the cable trough through the unit and from the 01T I/O panel. If this is impossible:
   a. First, get someone to help you.
   b. Then remove the logic gate from its hinges and set it on the floor of the unit, or out of the unit, as far from the 01T panel and as gently as possible to not damage the fans at the bottom of the gate.
   c. Remove the cable from the cable trough through the unit and from the 01T I/O panel.
7. Reverse the above steps to install the replacement cable, starting at the 01T I/O panel.
8. Run the SC tests, using Menu Selection 1 to check if the new cable has corrected the problem.

(SC464 Cont—SC520)

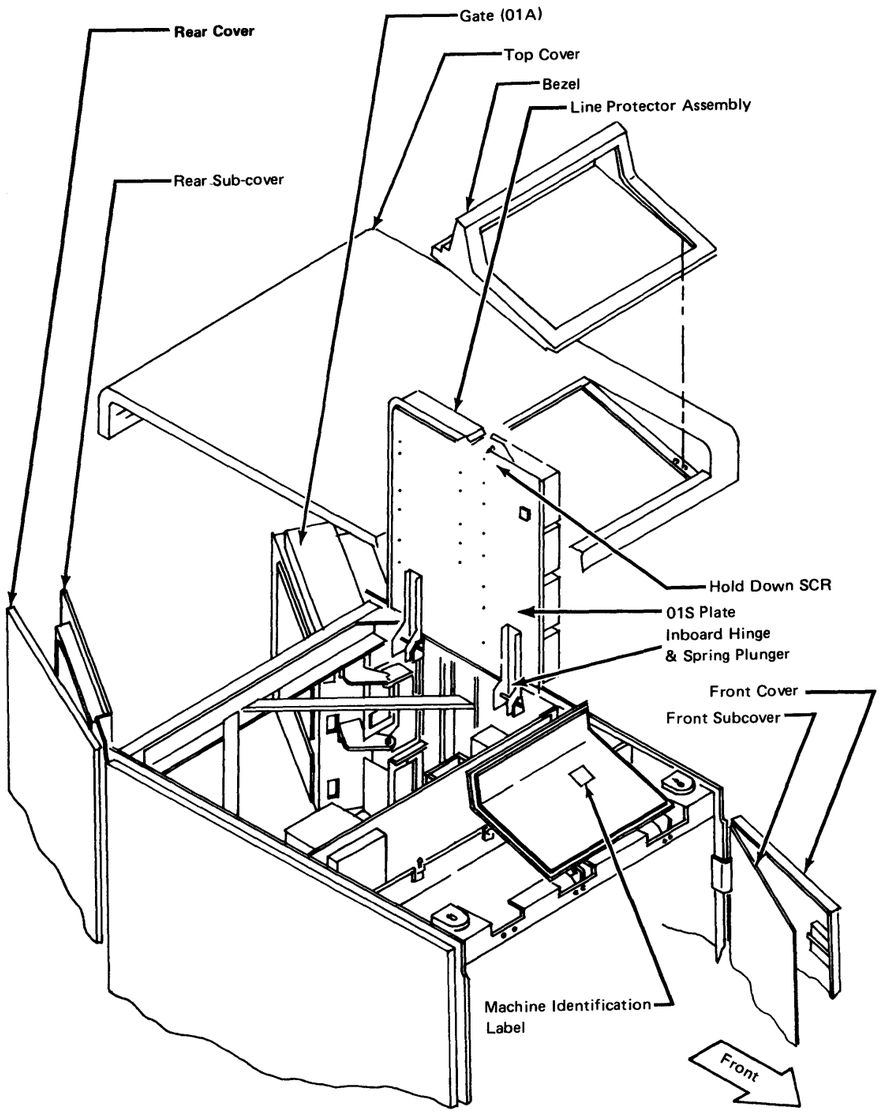



Figure SC520-1. Typical Top Covers

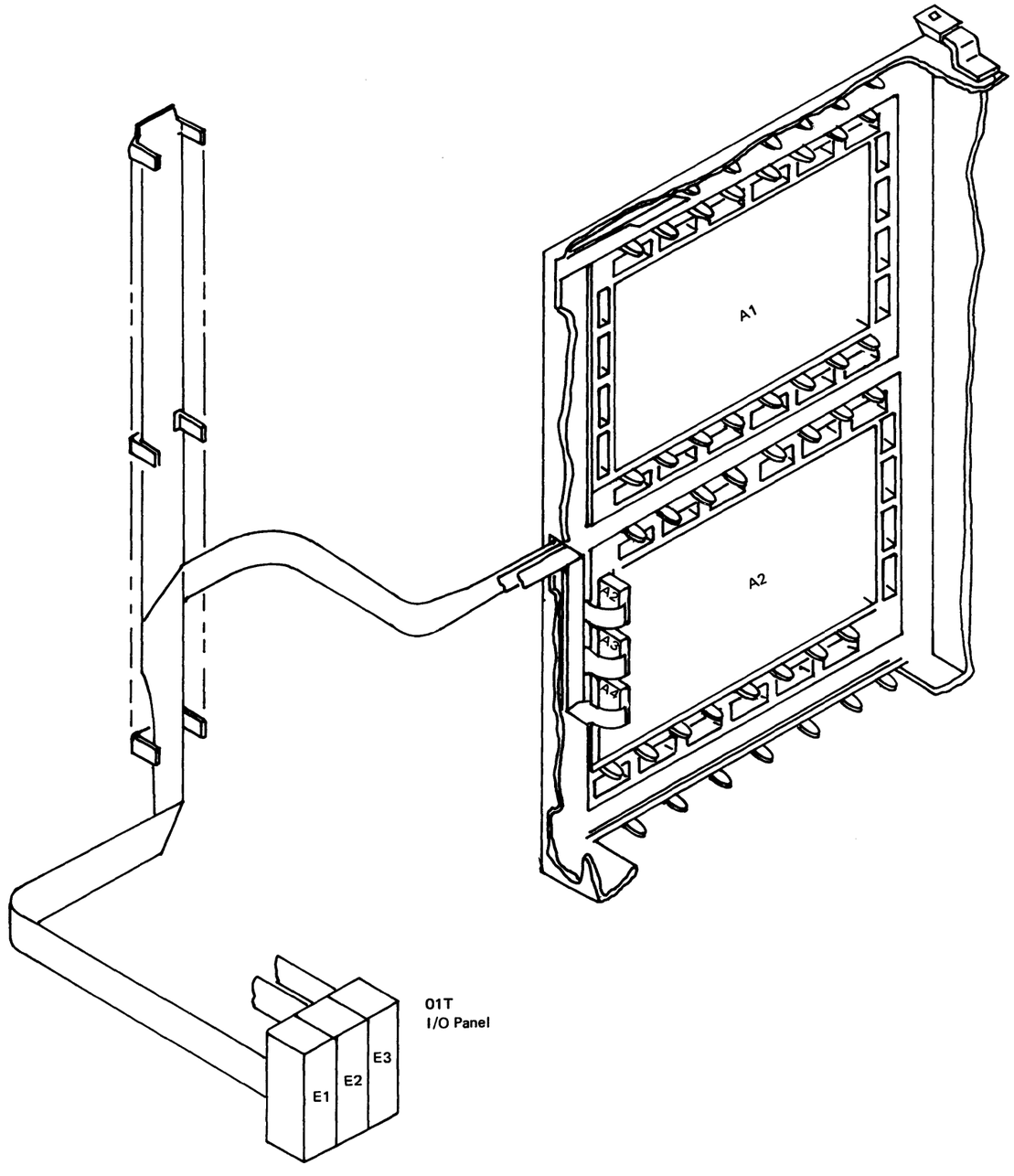



Figure SC520-2. Typical 8130 Cable Installation

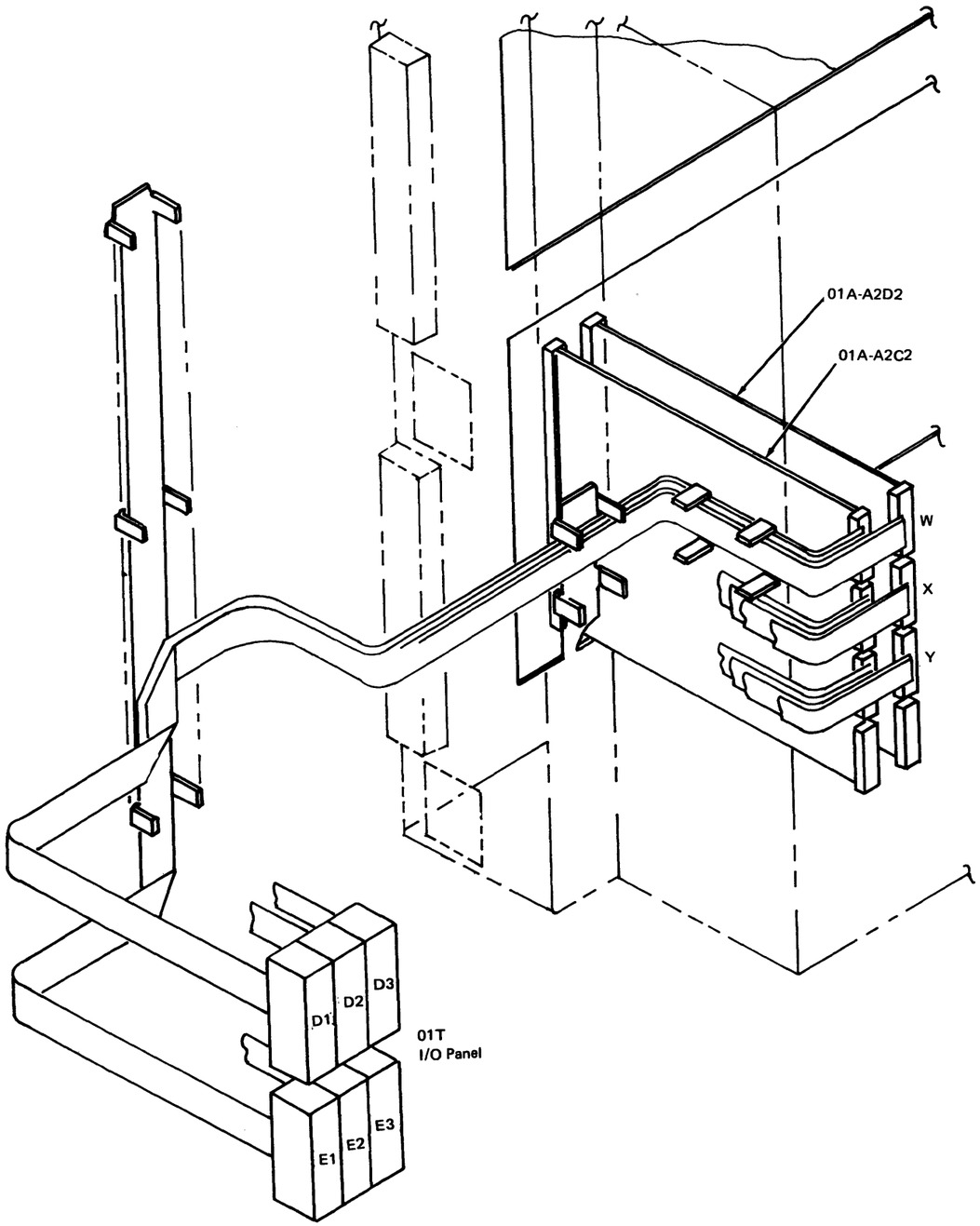



Figure SC520-3. Typical 8140 Cable Installation

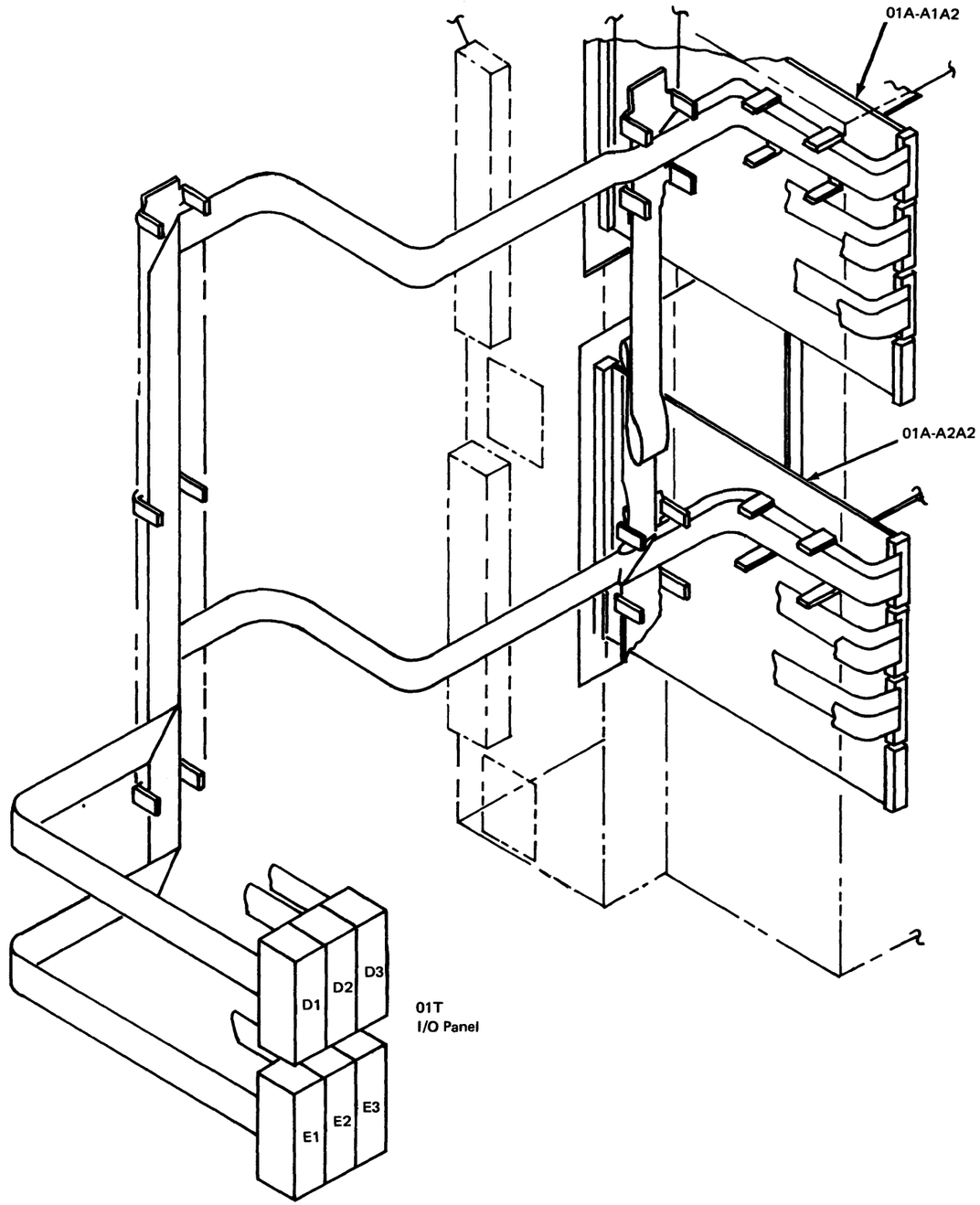



Figure SC520-4. Typical 8101 Cable Installation

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# Chapter 5. MAP Reference Information
# Expanded Function Panel
# (SP)

## Introduction

This part of Chapter 5 provides maintenance information to service the 8140 Expanded Function Operator Panel (EFP) Feature. When used with the Maintenance Analysis Procedures (MAPs), the MAP diagnoses EFP problems and refers to this part of Chapter 5 for information such as hardware locations, possible causes of failure, and wiring lists.

This part has five sections:

1. General Information (SP100–SP134) – Contains configuration, operation, and repair strategy information.
2. Offline Tests (SP200–SP254) – Contains test information and lists possible causes of failure.
3. Intermittent Failure Repair Strategy (SP300–SP350) – Contains information used to repair intermittent failures.
4. Signal Paths and Detailed Operational Description (SP400–SP450) – Contains diagrams and charts that show wiring and signal paths.
5. Adjustment, Removal, and Replacement Information (SP500–SP540) – Contains reference information used for card and component replacement.

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## Abbreviations

| | |
|---|---|
| BOP | basic operator panel |
| BOPA | basic operator panel adapter |
| BSTAT | Basic status register |
| conn | connector |
| DAT | dynamic address translation |
| DPPX | Distributed Processing Programming Executive |
| EF | expanded function |
| EFP | Expanded function operator panel |
| EIR | error interrupt request |
| EIRV | error interrupt request vector |
| EN | error number |
| EXPD | expected data |
| flt pt | floating point |
| FRU | field-replaceable unit |
| hex | hexadecimal |
| insn | instruction |
| I/O | input/output |
| IPL | Initial program load |
| LED | light emitting diode |
| MAP | Maintenance Analysis Procedure |
| MD | Maintenance Device |
| MI | Manual Intervention |
| op | operation |
| PA | Physical Address |
| PIO | programmed I/O |
| PSCF | primary system control facility |
| RECD | received data |
| reg | register |
| SCF | System Control Facility |

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## SP100 General Information

This SP section provides the reference information used to perform fault isolation for the 8140 Processor expanded function operator panel (EFP) feature. It should be used in conjunction with the EFP MAP, which can only be run offline using the Maintenance Device (MD). The MAP and EFP tests reside on MD diskette 01, and use reference material contained in this section for information such as hardware components and addressing, wiring checks, offline test routine descriptions and messages, and possible failure causes.

## SP110 Components and Addressing

This section contains information to assist in understanding the EFP physical components. It also describes the software addressing scheme and the configuration table entry used to specify the EFP.

### *SP111 Hardware Components*

The EFP is a physical extension of the basic operator panel (BOP). Refer to Figure SP120-1 for an illustration of the basic and expanded operator panels. The EFP uses one adapter card that plugs into the processor board, whose location depends on the 8140 model selected:

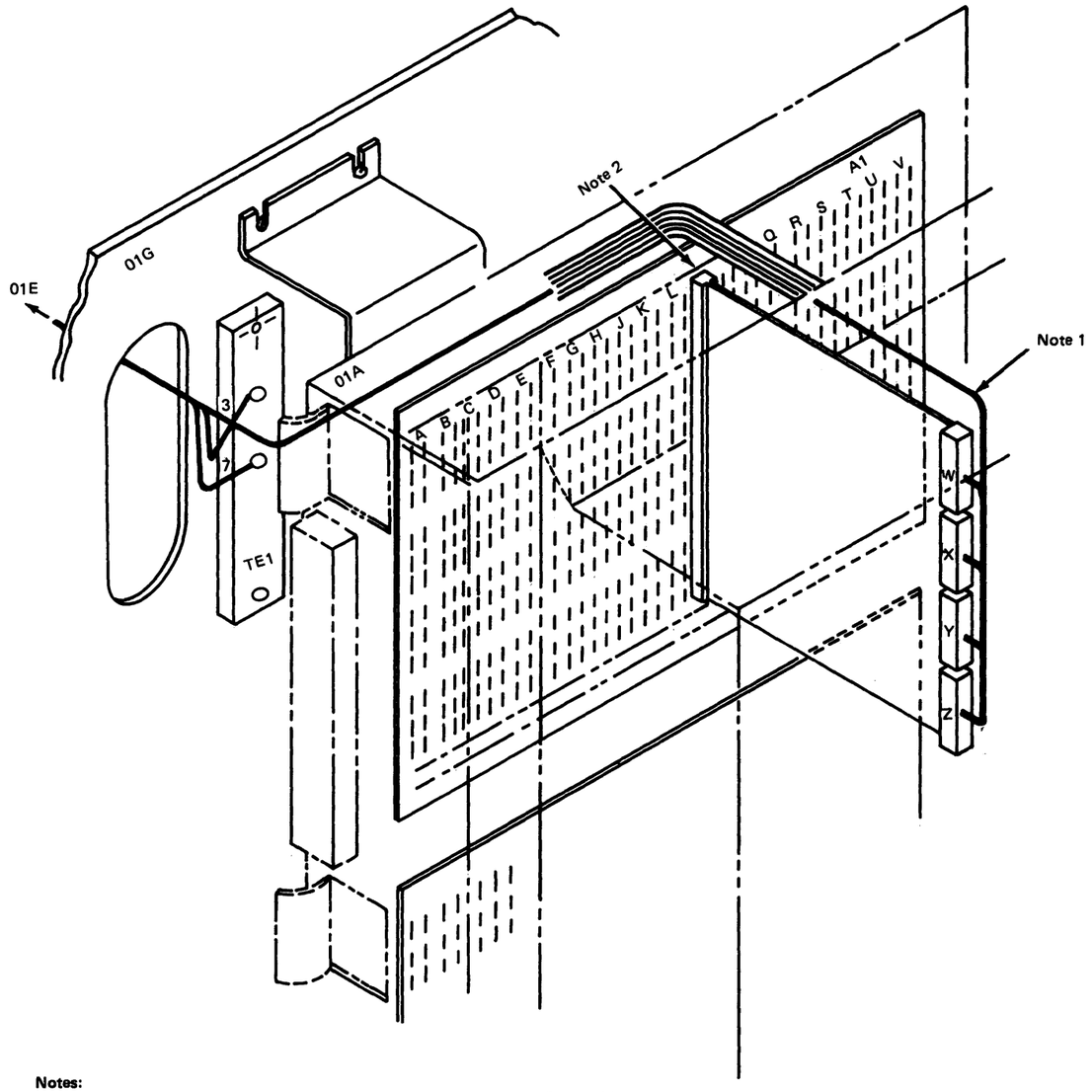
- Models A31–34 use board position A1M2.
- Other A models use board position A1P2.
- B models use board position A1S2.

The adapter card, board wiring and a single, multi-ended cable assembly provide the EFP hardware necessary for panel-to-processor information transfer. One of the cable connectors plugs into the top card connector "Z" position of the EFP adapter card, and the wires connected to it terminate at another connector that plugs into the basic operator panel keypad. In the same manner, the cable that plugs into the EFP adapter card "W" top card connector position plugs into the expanded panel's mode and state indicator card, the "X" connector to the EFP keypad card, and the "Y" connector to the EFP hexadecimal display card. The following chart shows the W, X, Y and Z connections:

| Connector | Attaches EFP Adapter Card To |
|---|---|
| W | EFP mode and state card |
| X | EFP keypad card |
| Y | EFP hex display card |
| Z | BOP Data/Function pushbuttons |

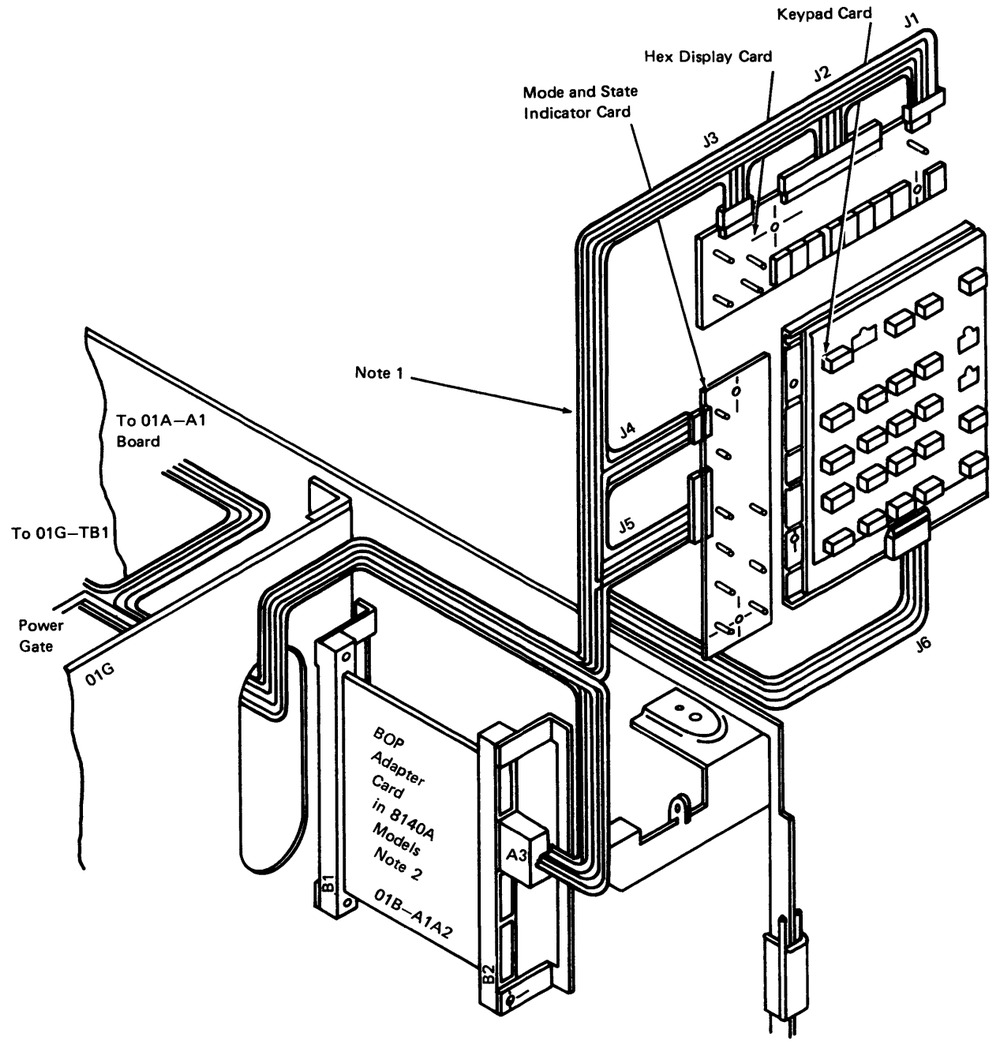
Additional wires in this cable assembly connect system power to the EF panel, and others terminate in a connector that plugs into the BOP Data/Function pushbutton keypad to permit its use by the EFP. Refer to Figures SP111-1 and SP111-2 for illustration of the cabling used to connect the EFP and its associated components.

Other than the adapter card, the EFP has three FRUs that attach to the rear of the panel (see Figure SP111-3): hexadecimal display card, EFP keypad card, and mode and state indicator card.




**Notes:**
1. *This cable is actually four flat cables, shown for illustration only. Each cable connects to the card by a double male pin-connector, PN 5997533.*
2. *Card location depends on 8140 model. See SP111 "Hardware Components."*

**Figure SP111-1. EFP Adapter Card and Cable Assembly**




**Note 1:** *This is actually a multiended cable assembly shown for illustration only.*
**Note 2:** *BOP Adapter Card lays flat under the Operators Panel in 8140B Models.*

**Figure SP111-2. EF Panel, BOP Adapter Card, and EFP Cable Assembly**

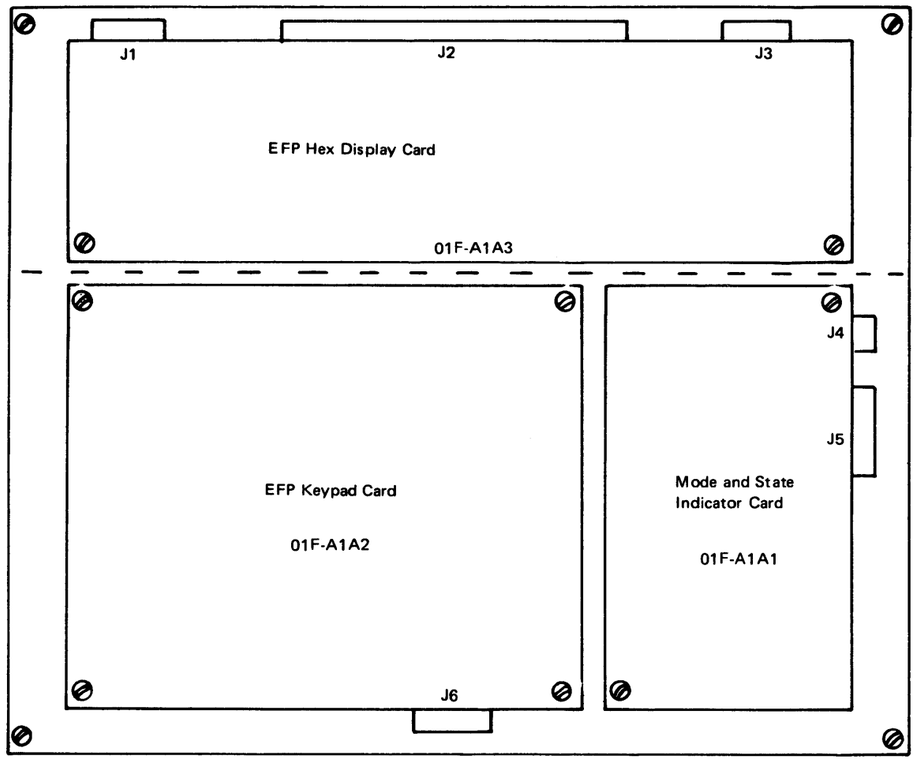



**Figure SP111-3. EF Panel FRU Components (Rear View)**

**Figure SP111-3. EF Panel FRU Components (Rear View)**

### *SP112 Addressing*

The EFP adapter has a fixed physical address (PA) of hex 0A, and all EFP to processor data transfer occurs through the system control facility (SCF) by using this address.

## SP120 Basic Operational Description

The EFP feature, available only on the 8140 Models A31–34, A41–44, A61–64, A71–74, and B51–72, combines hardware and software facilities to permit user access to the information contained within certain processor areas. Primarily, a programmer uses the EFP as an adjunct to conventional software troubleshooting aids.

**Note:** *The system must be offline to use the EFP.*

A typical EFP application would be to test and debug any control program that the customer can modify, such as the IBM Distributed Processing Programming Executive (DPPX). It can also be used to debug any application or I/O programs.

The EFP adapter card:

- Controls all instructions sent to the EFP.
- Physically and logically attaches the EFP pushbutton functions and indicators to the EFP program through the system direct control bus and system control facility. This permits processor hardware access so that the user can:
  - Stop on system check/program exception conditions.
  - Know when dynamic address translation occurs.
  - Perform address compares.
  - Know the current and last levels of processor instruction execution.
  - Determine the mode of processor instruction execution.
  - Know what PSV was used for each instruction.

The EFP feature allows you to read and write to the following areas through programming:

Storage locations

Registers

Translation table

Instruction addresses

Program status vectors

Address control vectors

In addition to the read and write capabilities, the EFP provides several special functions, which:

Transform an address.

Stop on an address compare.

Step instructions.

Start and stop processing.

Stop when detecting a system check/program exception.

With the EFP, certain conditions can be indicated by using discrete LEDs:

If using EFP register 1

If using EFP register 2

The processing instruction mode

If a primary or secondary PSV is in use

If using dynamic address translation

If the processor is stopped

If the BOP Data/Function pushbuttons are logically locked

The remaining LED indicators have a 4 x 7 matrix that indicates the current and last processing level and the contents of EFP registers 1 and 2.

**Note:** *Only DPPX provides commands to enable and disable EFP operation.*

The EFP presents I/O interruptions to the processor on priority level zero and uses physical address hex 0A, and both assignments are fixed. During actual interrupt presentations, only the Enable/Disable EF Panel pushbutton remains active. The EFP adapter enables the transfer of information from the panel to the processor. This information transfer occurs on the programmed I/O signal bus using only PIO halfword commands, and does not use any CHIO-type operations.

## *SP121 Panel Functional Operation*

The following text describes the function of the displays, pushbuttons, and indicators of the expanded function operator panel (EFP). See Figure SP121-1.

The eight position hexadecimal display, a Current or Last Level display, 15 discrete LED indicators, and 23 pushbuttons are divided into functionally associated groups. The following lists and describes the panel components by group:

### Displays

There are two displays used to indicate hexadecimal values:

**Current or Last Level** – Normally displays the current level, and used in conjunction with the Display Last Level pushbutton to indicate the last priority level (1–7 and not 0) active for the presently executing program.

**Address or Data** – Has eight hexadecimal positions and displays either data or address information. Depending on the status of EFP control register bit 4 that controls the Reg 1 and Reg 2 indicator status, the hex display contains either the register 1 or register 2 value. The characters enter the rightmost position and move to the left for successive entries. When all eight positions contain characters, each additional entry eliminates the leftmost position.

### Hardware Indicators

**Operator Attention/EF Panel** – The last expanded operation was incorrect. EFP control register bit 6 determines the indicator status, which blinks twice a second when on.

**EF Panel Check** – A parity check occurred during a programmed information exchange to the panel, or an interruption occurred in the physical panel cable interconnection.

**Reg 1** – When on during a store, fetch, or display operation, the hexadecimal display indicates the Register 1 Value. Either the Access Address Reg 1 pushbutton or a clear or default operation activates this indicator.

**Reg 2** – When on during a store, fetch, or display operation, the hexadecimal display indicates the Register 2 value. The Access Data Reg 2 pushbutton activates this indicator, which cannot be on the same time as the Reg 1 indicator.

**DAT Active** – Dynamic address translation is being used to access processor storage. All addresses generated are logical, and the address translation occurs on the level specified by the Current or Last Level display. The address mode register value determines the indicator status.

**Primary (Secdy) PSV** – Indicates whether the last instruction used a primary (indicator on) or secondary PSV for the processing level specified by the Current or Last Level display. Used in conjunction with the Display Last Level pushbutton to indicate the previous PSV used.

### State Indicators

**Keyboard Locked** – When on permits no functional keypad input except for the following pushbuttons: (1) Enable/Disable EF Panel, (2) Reset/Restore, (3) Display Last Level, (4) Access Address Reg 1, and (5) Access Data Reg 2. EFP control register bit 7 on turns on this indicator, and the Reset/Restore pushbutton resets it. Refer to SP233 for the conditions that turn on control register bit 7.

**Processor Stopped** – Priority Levels 1–7 are not active and processor is at level 0. Turned on by an address compare stop condition, a system check/program exception stop, or pressing the Stop pushbutton. EFP control register bit 5 determines the indicator status.

### Mode Indicators

The discrete LED mode indicators correspond to the program mode active when executing on the current priority level (1–7) specified by the Current or Last Level display. The program mode register determines which indicator turns on according to information in the current program status vector PSV. The mode indicators are: Master, Supervisor, I/O, and Application.

### Logical Pushbuttons

**Clear EF Panel** – Resets registers 1 and 2 to zero, and turns on the Reg 1 indicator. Resets the transform address bit (3) and the access register 2 bit (4) in the EFP basic status register, System Check on the BOP, and the Reg 2, Operator Attention, and Panel Check indicators on the EFP.

**Display Last Level** – When held, displays the priority level (1–7 and not 0) of the last active instruction in the Current or Last Level indicator, and permits display of the PSV used in the Primary (Secdy) PSV indicator.

**Access Address Reg 1** – Turns on the Reg 1 indicator and selects register 1 to receive any entry from the BOP Data/Function pushbuttons. Also pressed to return to register 1 after completing register 2 processing.

**Access Data Reg 2** – Turns on the Reg 2 indicator and selects register 2 to receive any entry from the BOP Data/Function pushbuttons indicator. Resets the transform address bit (3) and the access register 2 bit (4) in the EFP basic status register, System Check on the BOP, and the Reg 2, Operator Attention, and Panel Check indicators on the EFP.

**Enable/Disable EF Panel** – Enables or disables the expanded function panel and also transfers control of the Reset/IPL and Lamp Test pushbutton functions and hex keypad operation to the EFP. The keylock switch, if installed, must be set to Enable to permit operation.

Expanded Function Panel

Basic Operator Panel

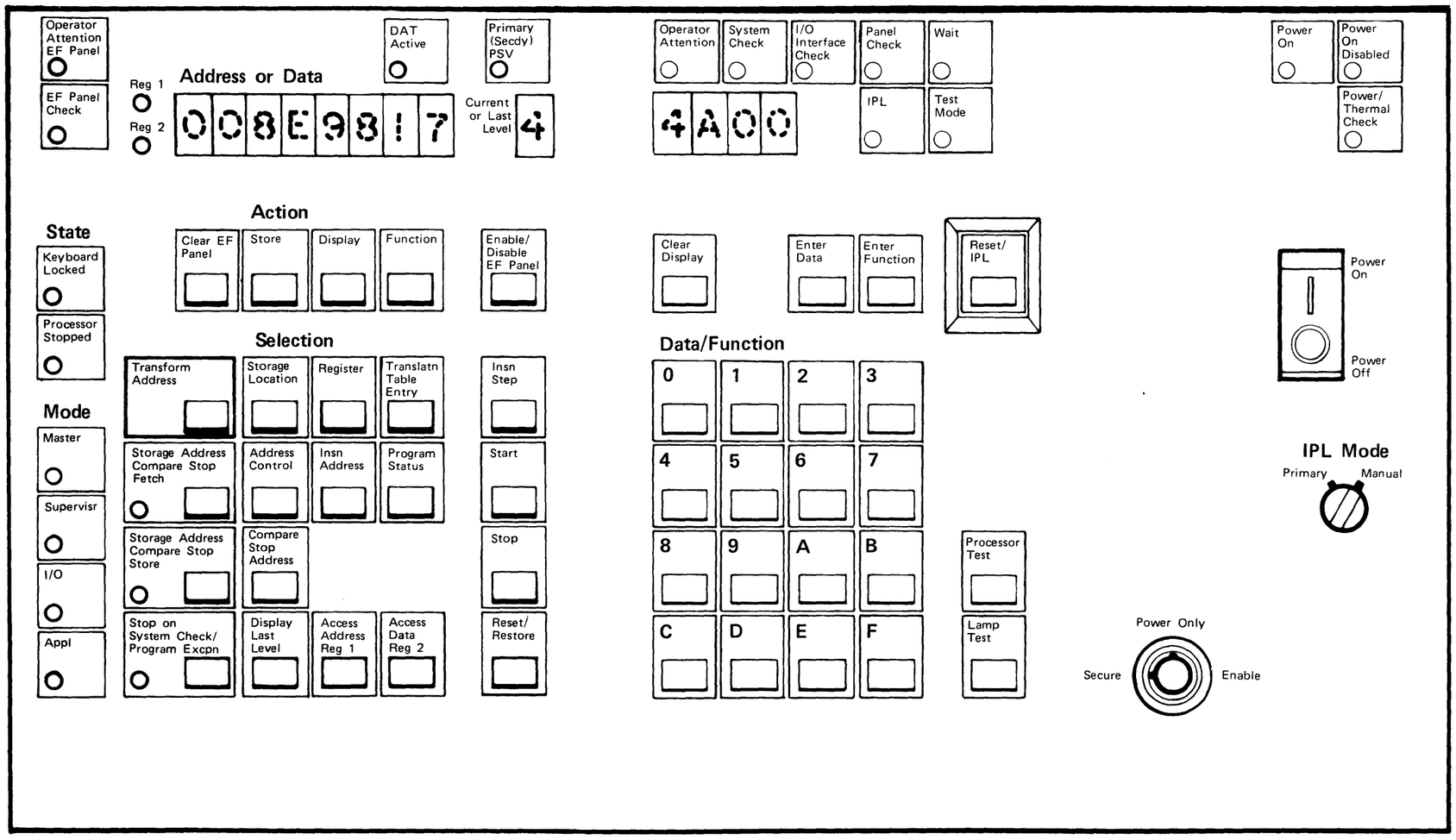



**Figure SP121-1. Basic and Expanded Function Operator Panel**

**Selection Pushbuttons**

**Transform Address** – Operates in conjunction with pushbuttons in the same row used to address the processor, registers, or storage, in either store or display modes. When pressed, transforms the logical address contained in register 1 into a real address, places it in register 2, and turns on EFP BSTAT bit 3. It is reset by the Clear Panel pushbutton.

**Storage Location** – When pressed, EFP BSTAT bit 2 turns on, and the next valid access is to the storage location specified by the register 1 value.

**Register** – When pressed, EFP BSTAT bit 1 turns on, and the next valid access is to the register location specified by register 1.

**Translatn Table Entry** – When pressed, EFP BSTAT bits 1 and 2 turn on, and the next valid access is to the translation table address specified by the register 1 value.

**Address Control** – When pressed, turns on EFP BSTAT bits 0, 1, and 2, and selects the specified adjunct register addressing information.

**Insn (Instruction) Address** – Pressed before a display or store operation, it displays or alters the first 32 bits of the PSV (instruction address) located in register 1, and turns on EFP BSTAT bit 0.

**Program Status** – Pressed before a display or store operation, it displays or alters the last 32 bits of the PSV, but not the instruction address, and turns on EFP BSTAT bits 0 and 2.

**Compare Stop Address** – Used in conjunction with Storage Address Compare Stop Fetch or Store pushbuttons, stores the register 1 address in the compare stop address register, stops processing when the addresses agree, and turns on EFP BSTAT bits 0 and 1.

**Display Last Level** – When held, displays the priority level (1–7 and not 0) of the last active instruction in the Current or Last Level indicator, and permits display of the PSV used in the Primary (Secdy) PSV indicator.

**Access Address Reg 1** – Turns on the Reg 1 indicator and selects register 1 to receive any entry from the BOP Data/Function pushbuttons. Also pressed when returning to register 1 after completing register 2 processing.

**Access Data Reg 2** – Turns on the Reg 2 indicator and selects register 2 to receive any entry from the BOP Data/Function pushbuttons.

**Action Pushbutton/Indicators**

**Store** – Either (1) places the contents of register 2 into the address specified by register 1, or (2) displays the contents of the address indicated in the hex display.

**Display** – When pressed in conjunction with a selection pushbutton, causes display of the address in register 1 according to the selection pushbutton used. If Transform Address was pressed for a display address function, the address is logical.

**Function** – Only active when in stop mode, and uses the register 1 contents for display or store operations according to the selection pushbutton pressed. This pushbutton can also be used to display the control vectors by using 28 control immediate (KI) instructions. Any store operation must have previously placed data in register 2.

**Insn (Instruction) Step** – Executes one instruction at the level indicated, and displays the PSV instruction address in register 1. The processor must be stopped for this to occur, and interruptible instructions do not execute completely by pressing this pushbutton once.

**Start** – Begins instruction execution at the highest pending interrupt level if the processor was previously in stop mode.

**Stop** – Turns on the Stop indicator and stops instruction execution. Last level display procedures indicate the last executed address, and logic forces a current processing level of zero.

**Reset/Restore** – Resets the processor but not the EFP logic, turns off the Keyboard Locked indicator if on, enables all EFP pushbuttons, turns on EFP BSTAT bits 8, 9, 10, and 15, and requests an interrupt if EFP BSTAT bit 14 is on.

**Storage Address Compare Stop Fetch** – Operates in conjunction with the Compare Stop Address pushbutton. Specifies that if the address compare register contents are identical with the priority level, PSV selection, and processor address used during a fetch storage operation, processing stops and the indicator turns on. EFP control register bit 0 determines the indicator status.

**Storage Address Compare Stop Store** – Operates in conjunction with the Compare Stop Address pushbutton. Specifies that if the address compare register contents and a processor storage address compare during a store operation, processing stops. EFP control register bit 1 determines the indicator status.

**Stop on System Check/Program Excpn** – Stops instruction execution after detecting a system check/program exception error. When this condition occurs, the panel indicators show either the failing instruction or the next instruction, together with status information. EFP control register bit 2 determines the indicator status, and the pushbutton turns on EFP BSTAT bit 6.

## SP130 Adapter-Unique Repair Strategy

The following sections refer to those repair strategies that are unique to the EFP. Refer to the Chapter 4 general maintenance approach section for those that are common to the 8100.

### *SP132 DPPX Repair Strategy*

The EFP cannot be tested online under DPPX.

**Caution: Serious damage to the customer control program could result from improper operation of the EFP.**

### *SP134 Intermittent Failure Repair Strategy*

For intermittent EFP error action plans, refer to section SP300.

## SP200 Offline Tests

All testing and repair of the EFP occurs offline. These tests reside on MD diskette 01, and require system dedication to verify operation or isolate failures, some of which may require manual intervention. The test can be initiated by specifying physical address hex 0A and the desired options.

The MAP either detects a failure in the adapter card, or prompts you to perform some action at the panel. As a result of this action, the test compares the results received with the results expected. If the MAP detects an error, refer to section SP250 for repair action according to the failure. If the MAP does not isolate the failure, refer to section SP250 for further corrective action.

## SP210 Offline Test Routine Descriptions

The first group of routines verify proper adapter card operation, and the last group permits you to perform manual intervention routines to determine panel problems. The adapter routines complete in less than 4 seconds, while the time required to run the manual intervention routines is operator-dependent. The SP MAP uses two logical sections: Routines 1–19 test only the adapter, while Routines 20–31 test the LED indicators, panel switches, and cables, including the adapter functions necessary to operate them.

The MD invokes the adapter routines either by the MAP or by using the Free-Lance Utility.

- When using the MAP, the tests are invoked automatically when required.
- When using the Free-Lance Utility, the following test invocation procedure must be used:
  1. At 80BC or PA00, enter 08PAB.
  2. At 81BC, enter SLRRB.

Where:

PA = adapter address (always 0A)

S = sense option:

- 0 = run only adapter tests, Routines 1–19, without using loop option 1.
- 1 = run adapter tests, Routines 1–19, using loop option 1.
- 2 = run adapter/device tests with manual intervention, routines 1–31

L = loop option:

- 0 = run selected routines one time.
- 1 = loop selected routines; stop on error.
- 2 = loop selected routines; bypass error.

RR = routine number. If 00 or no entry is made, all routines for sense option are run. If a routine number is entered, only that routine is run.

B = begins execution and enters the invocation message.

0A00 indicates successful completion of the adapter tests. For more information on test invocation and operation, refer to CP600 Common Test Procedures and Messages in Chapter 2.



## *SP211 Adapter Tests*

These routines test the adapter hardware, EFP I/O commands, and the SCF to EFP signal bus. The following describes the adapter test routines and the function performed by each.

**Routine 1, Reset Adapter Test.** The processor issues a Reset Adapter command to the EFP. This determines if the EFP recognizes the hex 0A address used for all EFP information transfer, and resets the EFP registers to zero. The test then issues read commands to determine if the adapter was completely reset. This routine tests the Reset Adapter, Read Basic Status, Read Register 1 Low, Read Register 1 High, Read Register 2 Low, Read Register 2 High, and Read Control Register commands. The valid routine test error messages are hex 0101, 0104, and 0120 to 0125.

**Routine 2, EFP Basic Status Register Test.** Issues Read and Write PIO commands to test the EFP basic status register and to verify that all bits set and reset correctly. This routine also tests proper operation of the adapter drivers and receivers common to all registers. It uses five data patterns, and tests the Set BSTAT and Reset BSTAT EFP commands. The valid routine test error messages are hex 0201, 0204, and 0220 to 0222.

**Routine 3, EFP Interrupt Request Test.** The EFP uses mostly interrupt requests for processor information transfer. This test enables the EFP interrupt request logic and conditions the EFP BSTAT to request an interrupt. The interrupt then occurs, and the EFP status indicates a pending interrupt request. The valid routine test error messages are hex 0301, 0304, 0305, and 0320.

**Routine 4, Control Register Data Test.** The 8-bit control register determines operation of address compare stop, system check/program exception stop, keyboard lock, enable panel, and indicator functions. This test verifies the correct set and reset of the control register data. It uses Read and Write commands to store and fetch the five data patterns used, and checks the Write Control Register command. The valid routine test error messages are hex 0401, 0404, and 0420.

**Routine 5, Register 2 High Data Test.** Control register bit 3, if active, permits access to EFP register 2. This 32-bit register has both a high and a low data area, each of which determines four EFP hexadecimal display values. Data characters enter the rightmost half byte and shift all other characters to the left. When full, each subsequent entry causes loss of the high-order position. This routine verifies that the 16 high-order register 2 bit positions can be correctly set and reset. It uses Read and Write commands to store and fetch the five data patterns used, and checks the Write Register 2 High command. The valid routine test error messages are hex 0501, 0504, 0520 and 0521.

**Routine 6.** NOT USED.

**Routine 7, Register 2 Low Data Test.** Verifies the correct set and reset of the 16 low-order register 2 bit positions. It uses Read and Write commands to store and fetch the five data patterns used, and checks the Write Register 2 Low command. The valid routine test error messages are hex 0701, 0704, 0720, and 0721.

**Routine 8, Register 1 Low Data Test.** Control register bit 3, if off, permits access to EFP register 1. This 32-bit register has both a high and a low data area, each of which determines four EFP hexadecimal display values. This routine verifies the correct set and reset of the 16 low-order register 1 bit positions. It uses Read and Write commands to store and fetch the five data patterns used, and checks the Write Register 1 Low command. The valid routine test error messages are hex 0801, 0804, 0820 and 0821.

**Routine 9, Register 1 High Data Test.** Verifies the correct set and reset of the 16 high-order register 1 bit positions. It uses Read and Write commands to store and fetch the five data patterns used, and checks the Write Register 1 High command. The valid routine test error messages are hex 0901, 0904, 0920, and 0921.

**Routine 10, Address Compare Test.** Places a test address value in the EFP address registers and sets the level compare to zero to compare only the test address value. It sets both store and fetch compare bits in the control register, and then fetches the test address. The test then verifies that an interrupt occurred, reads the status, and compares it to the expected value. The routine uses the Write Address Compare Register High and Write Address Compare Register Low commands. The valid routine test error messages are hex 1001, 1004, 1005, and 1020.

**Routine 11, Store Address Compare Test.** Fetches storage location hex 0000 and sets up an address compare condition for a store to this location. It then stores the previously fetched data, and an address compare occurs. The test then performs the same operation on storage locations 0000FFFE to 0007FFFE by incrementing address byte 1, and an equal compare should occur on each store. The valid routine test error messages are 1101, 1104, 1120, and 1121.

**Routine 12, Fetch Address Compare Test.** Uses storage address locations hex 0000 and FFFF to test the EFP fetch address compare logic. It conditions the control register to stop on a fetch address compare, fetches storage location hex 0000, and ensures that an equal compare occurs. It then fetches storage location hex FFFF and also ensures that an equal compare occurs, and, in both cases, checks proper status and interrupt conditions. The valid routine test error messages are hex 1201, 1204, and 1220 to 1222.

**Routine 13, No Stop on Store or Fetch Compare Test.** Places a test address, in the address compare register and then conditions the control register to stop on a store compare operation. It then fetches the test address and no equal compare should occur.

Next, it conditions the control register to stop on a fetch to the test address, performs a store to it, and does not expect an equal compare. The routine checks for proper status after each test location access. The valid routine test error messages are hex 1301, 1304, 1320, and 1321.

**Routine 14, Processing Level Address Compare Test.** Performs an address compare fetch on processing levels 1–7, using both the primary and secondary PSVs, and checks that the compare occurs only on the proper level with the correct PSV. It first conditions the address compare register for a specific level and PSV, executes on all levels, and then ensures that the compare occurred only for the correct level. The routine uses the secondary PSV for 49 passes and then uses the primary PSV for 49 more. It checks status for each valid compare to ensure proper operation, and uses the BOP to display errors if either no compare occurs on any level, a compare error occurs, or for incorrect status after a compare. The valid routine test error messages are hex 1401, 1404, and 1420 to 1422.

**Routine 15, Interruptible Instruction Compare Test.** Verifies that an address compare causes an interrupt request at the proper time. It first conditions the address compare register to compare on the first byte of a storage field, then issues an MVRS interruptible instruction to move data from the test field to another field. The address compare interrupt should occur on the first MVHS instruction data fetch. The test verifies correct operation by saving the count register when the interrupt occurs, and comparing it to the expected count when instruction execution completes. The valid routine test error messages are hex 1501, 1504, and 1520.

**Routine 16, No Compare on Unsuccessful Branch.** After conditioning the address compare logic to compare on the target of an unsuccessful branch, it executes the branch instruction and no branch or compare should occur. The valid routine test error messages are hex 1601, 1604, and 1620.

**Routine 17, Stop on Instruction Fetch Test.** Verifies that the panel presents an interrupt request at the proper time on an address compare during instruction fetch. It first conditions the address compare logic with an invalid op code, and then executes the instruction. The address compare should occur before the program check.

It next conditions the address compare logic, using the second half of an MVHS instruction, and executes a KI swap to the primary PSV. The address compare should occur before the KI swap. The valid routine test error messages are hex 1701, 1704, 1720, and 1721.

**Routine 18, Stop on System Check/Program Exception Test.** This routine first conditions the EFP to stop on either a system check or a program exception. It then issues an invalid command of hex FF to the EFP that causes a system check. The test then examines panel status to verify that the panel interrupted processing when the system check occurred.

Next, the test saves the level 7 primary PSV, changes it to point to the routine's program exception handler, and executes an op code of hex FFFF, which causes a program exception. It then stores the primary PSV, returns to the secondary PSV for program execution, and checks status to verify that the panel interrupted processing when the program exception occurred. The valid routine test error messages are hex 1801, 1804, 1820, and 1821.

**Routine 19, Invalid Command Test.** The previous routines tested all valid commands. This routine issues all the invalid EFP commands from hex 00 to FF, each of which should cause a system check. After issuing each invalid command sequence, the test checks EFP status to determine if the proper response occurred. The valid routine test error messages are hex 1901, 1904, 1920, and 1921.

### *SP212 Manual Intervention Panel Tests*

The manual intervention EFP routines test the panel logic, indicators, pushbuttons, and the panel adapter signal bus. This section describes these routines. Refer to SP242 for actions required by manual intervention messages.

**Routine 20, EFP Operator Attention Indicator Test.** Blinks the Operator Attention indicator and prompts you for a response to this condition. The MD display indicates an error for a negative response, and the BOP displays test error messages of either hex 2001 or 2004 if unexpected system conditions occurred during the test.

**Routine 21, Action Pushbutton Test.** Tests the function of the Display, Store, Start, Function, Insn Step, Stop, Reset/Restore, Storage Address Compare Stop Fetch, Storage Address Compare Stop Store, and Stop on System Check/Program Excpn pushbuttons.

The routine enables the EFP pushbuttons and uses the MD to prompt you for activation of these pushbuttons in the specified order. When each pushbutton generates an interrupt request, the test checks the corresponding EFP BSTAT bit to verify that it turned on. The BOP displays valid test error messages hex 2121, 2123, 2125, 2127, 2129, 2131, 2133, 2135, 2137, and 2139 for incorrect pushbutton functional operation, and 2101 and 2104 if unexpected system error conditions occurred.

**Routine 22, Selection Pushbutton Test.** Tests the function of the Storage Location, Register, Translation Table Entry, Address Control, Insn Address, Program Status, Compare Stop Address, and Transform Address pushbuttons.

The routine enables the EFP pushbuttons and prompts you from the MD. Each pushbutton should be pressed in the specified order, followed by the Start pushbutton to generate an interrupt request. The test then checks the corresponding EFP BSTAT bit to verify that it turned on. The BOP displays valid test error messages hex 2221 to 2225 and 2236 to 2238 for incorrect pushbutton functional operation, and 2201 and 2204 if unexpected system error conditions occur.

**Routine 23, Reg 1, Reg 2 and Hexadecimal Display LED Test.** The MD prompts you if all patterns should be tested, and, if not, uses only hex 0000 and FFFF. The test first places hex 00000000 in register 1 and hex BAD0BAD0 in register 2, and prompts you to verify that the hexadecimal display output from register 1 contains zeros with the Reg 1 indicator on. The test then reverses the register 1 and register 2 values and performs the same operation. The Reg 2 indicator should now be on, Reg 1 off, and the register 2 display value should be all zeros.

The test steps to either hex 11111111 or FFFFFFFF, depending on the option selected, performs the same operation with the new register values, and prompts for response to the display and indicator conditions. A negative response to the MD prompt results in an error message on the MD display, and the BOP displays test error message numbers hex 2301 and 2304 when unexpected system error conditions occur.

**Routine 24, Action Pushbutton Test.** Tests the Enable/Disable EF Panel, Clear Panel, Access Address Reg 1, and Access Data Reg 2 pushbuttons.

The test first turns on the EFP control register operator attention bit, but does not enable the panel. The MD then prompts you to press the Enable/Disable EF Panel pushbutton, followed by the Start pushbutton.

**Note:** *The Start pushbutton did not function properly if the panel pushbuttons remain inoperative. Before continuing, the test checks for valid basic status.*

The MD prompts for your response after observing if the Operator Attention indicator blinks. An EF panel reset then occurs, and BSTAT bits 3 and 14 turn on.

Next, the test fills registers 1 and 2 with hex FFFFFFFF and accesses register 2 with the Operator Attention indicator still blinking. The test prompts you to press the Clear Panel pushbutton and enter a '1' in the MD keypad. The EFP BSTAT should now have bit 3 reset, registers 1 and 2 should be all zeros, and the control register attention and access register 2 bits should be off. The test then resets the panel.

Finally, the test fills register 1 with hex 11111111, register 2 with hex 22222222, and accesses register 2. The prompt message requests verification of the display value, followed by pressing the Access Address Register 1 pushbutton. You should verify the register 1 display value of hex 11111111, press the Access Data Register 2 pushbutton, and verify the register 2 display value of hex 22222222.

The BOP displays valid test error messages hex 2421 and 2424 to 2427 for functions checked by this routine, and hex 2401 and 2404 when unexpected system errors occur.

**Routine 25, Data/Function Pushbutton to Register 1 and 2 Exerciser.** Checks the BOP Data/Function pushbutton encoding logic and the Data/Function pushbutton to register 1 and 2 data path. The MD prompts you to access registers 1 and 2 from the keypad. The test terminates by pressing Stop.

The MD prompt message then asks if the test functioned properly. A negative response prompts an MD display error message, and unexpected system error conditions display valid test error message numbers hex 2501 and 2504 on the BOP.

**Routine 26, Data/Function Pushbutton Locked Test.** Enables the panel and logically locks the Data/Function pushbuttons. The MD then asks you to check that the pushbuttons do not operate and that the Keyboard Locked indicator turned on. A negative response prompts an MD error message, and unexpected system error conditions cause the BOP to display valid test error message numbers hex 2601 and 2604.

**Routine 27, Compare Stop and Processor Stopped Indicator Test.** Tests the Storage Address Compare Stop Fetch, Storage Address Compare Stop Store, Stop on System Check/Program Excpn, and Processor Stopped indicators. The test turns on each indicator one at a time, and prompts a response from the MD for proper indicator operation. A negative response prompts an MD error message, and unexpected system error conditions cause the BOP to display valid test error message numbers hex 2701 and 2704.

**Routine 28, Panel Check Test.** Tests the panel check logic by attempting to execute an invalid command. The test first enables the panel indicators and issues an invalid command. This causes a system check, which should turn on the EF Panel Check indicator. The MD asks if the indicator is on, and displays an error message for a negative response. The MD then prompts you to press the Clear Panel pushbutton and ensure that the Panel Check indicator turned off. The MD again displays an error message for a negative response, and unexpected system errors result in valid test error messages hex 2801 and 2804.

**Routine 29, DAT Active Test.** Tests the panel's capability to detect and display dynamic address translation mode. The routine first builds a translation table that assigns the same actual storage locations to real addresses 0–66K and logical addresses 0–64K. It then sets the level 7 adjunct register contents to logical address values.

The MD instructs you to press the Start pushbutton to cause a level 0 interrupt. The test then returns to level 7 in logical addressing mode, which should turn on the expanded panel DAT Active indicator.

Next, the test restores the level 7 adjunct registers to real addressing values and prompts you to press Start if the DAT Active indicator turned on or Stop if it did not. Either pushbutton causes an interrupt to level 0, restores the processor to real addressing mode, and returns to level 7 processing. The test then checks status to determine the pushbutton used. The BOP displays the error message hex 2922 if it was the Stop pushbutton, and also displays test error messages 2901 and 2904 for unexpected system error conditions.

**Routine 30, Mode Indicator Test.** Checks the Master, Supervisor, I/O, and Appl mode indicators and logic.

After initiating the routine, the MD asks you to check the Supervisr mode indicator status. A negative reply places a test error message in the BOP display.

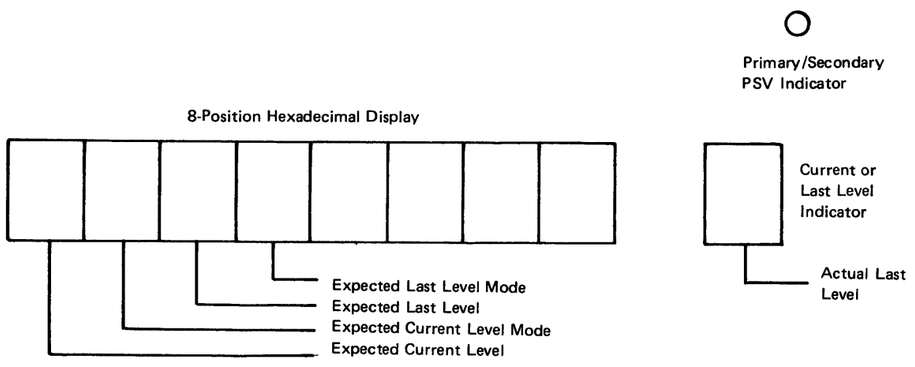
To test the other three indicators, the routine stores a test mode byte in a fixed storage location, and prompts you to press the Start pushbutton, which causes an interrupt to processing level 0. The level 0 interrupt handler then conditions level 7 for the test.

The test returns to level 7, and the indicator for the mode under test remains on for about 10 seconds. The MD then prompts you to press Start if the indicator comes on and then turns off, or Stop if it doesn't.

The test reads basic status after each operation to determine the pushbutton pressed, and each indicator must be tested three times. The BOP displays test error messages hex 3020, 3023, 3025, and 3027 for negative responses to the prompt message, and hex 3001 and 3004 if unexpected system error conditions occurred during testing.

**Routine 31, Current or Last Level Display and PSV Indicator Test.** Checks the Current or Last Level display, the Primary (Secdy) PSV indicator, and the Display Last Level pushbutton. During the test, the Current or Last Level indicator displays the level, and the Primary/Secdy PSV displays the mode.

The level steps once every 5 seconds for each primary level 1–7, and then repeats the stepping procedure using secondary mode. The eight-position hexadecimal display and Current or Last Level display provides test status information as follows, in conjunction with the Primary/Secdy PSV indicator:




The routine uses the four leftmost positions of the EFP hexadecimal display to indicate the expected status:

- The first and third indicate the expected current and last processing levels (1–7)
- The second and fourth indicate the expected mode (primary or secondary):
  - If the second and fourth digits are 1's, the Primary/Secdy PSV indicator should be on (primary PSV).
  - If the second and fourth digits are 0's, the Primary/Secdy PSV indicator should be off (secondary PSV).

Press the Display Last Level pushbutton during the test to check the correct last processing level and mode.

When the test terminates, the MD asks if the display values compared and the Display Last Level pushbutton operated properly. A negative response displays an error on the MD. Unexpected system error conditions display test error messages hex 3101 and 3104 on the BOP.

## SP230 Test Message Formats and Status Registers

The following sections describe the format of the test messages generated when performing offline testing.

### *SP231 Adapter Test Message Formats*

The following test message formats occur when performing adapter Routines 1–19.

| Test Messages | Meaning |
|---|---|
| 0A00 | Test ran successfully |
| 0AF0 | Tests running |
| 0A2E RREN 00MM IIII | Format 1 error message |
| 0A2E RREN 00ML IIII | Format 2 error message |
| 0A2E RREN 00BS EXPD RECD | Format 3 error message |

Where:

0A = EFP physical address
2 = Processing level
E = Error
RR = Failing routine
EN = Error number within the routine
00 = Not used
MM = EIRV contents when failure occurred
IIII = Instruction address when failure occurred
ML = PSV used and processing level active when failure occurred
M = 0 = Primary mode
M = 1 = Secondary mode
L = Processing level
EXPD = Expected data
RECD = Received data

## *SP232 Manual Intervention Test Message Format*

The EFP manual intervention routines use format 1 test error messages (RREN) if an unexpected error occurs. They also display 73 prompt messages numbered from 1 to 74, with 73 not used. These messages prompt you to answer questions concerning status, or to perform certain procedures. The following message format occurs when performing Routines 20–31:

TEST MESSAGE

PAMI

Where:

PA = EFP physical address hex 0A

MI = Prompt message number

## *SP233 EFP Registers*

This section describes the EFP basic status and control registers and their bit meanings, as well as all other EFP registers.

**Basic Status Register**

The 16-bit EFP basic status register indicates the pushbuttons that were activated, equal compare conditions, adapter-detected error conditions, and interrupt priority request status. The bits are programmable, and also reflect the activation of certain EFP pushbuttons. The following table describes the bit meanings when on.

| Bit | Pushbutton Pressed or Condition Detected |
|---|---|
| 0–2 | EFP selection pushbutton encode — Binarily determines which of the Selection pushbuttons were pressed according to the following:<br>000 = None<br>001 = Storage Location<br>010 = Register<br>011 = Translation Table Entry<br>100 = Insn Address<br>101 = Program Status<br>110 = Compare Stop Address<br>111 = Address Control |
| 3 | Transform Address pushbutton pressed. |
| *4 | Storage address compare stop fetch condition occurred. |
| *5 | Storage address compare stop store condition occurred. |
| *6 | Stop on system check/program exception condition occurred. |
| 7 | Reserved |
| *8–10 | EFP Action pushbutton encode — Binarily determines which of the Action pushbuttons were pressed according to the following:<br>000 = None<br>001 = Display<br>010 = Store<br>011 = Start<br>100 = Function<br>101 = Insn Step<br>110 = Stop<br>111 = Reset/Restore |
| 11 | Initialize — Only set by programming and reset by programming or the Enable/Disable EF Panel pushbutton. |
| *12 | Stop condition met — Address compare or system check/program exception condition occurred. When detected with bit 14 on, (1) signals the processor to stop execution and (2) in conjunction with bit 15, requests a level 0 interrupt to ensure the EPF control program receives control. |
| *13 | Equipment check — One of the following conditions occurred:<br>• I/O command parity error from the channel<br>• Data parity error from the processor<br>• Invalid program command<br>• I/O operation occurred after the channel halted EFP operation. This condition does not present an interrupt request.<br><br>This EFP-detected error occurred while the channel was waiting for a valid EFP response which was suppressed by the EFP adapter. The channel, therefore, turned on the timeout bit (1) in the EIRV which, in turn, activated the processor halt signal. The timeout bit also requests processing on level zero, which, if enabled, causes a system check interruption. For a processor-detected error, the PSCF would recognize the halt signal and turn on this bit. |
| 14 | EFP enabled — Set by programming and reset by programming and an EFP Control Reset command. When off, does not permit interrupt presentation to the processor. |
| 15 | EFP interrupt request — Turned on by bits 4, 5, 6, 8, 9, 10, 12, or 13. When on in conjunction with bit 14, presents a level 0 interrupt request to the processor and disables EFP pushbutton operation, except for Enable/Disable EF Panel. |

*Turns on EFP interrupt request (bit 15).

### EFP Control Register

The EFP control register permits program control of certain EFP functions and indicators. All bits of this 8-bit register can be set by the program, and bits 3 and 4 can also be set by EFP pushbuttons. The register is reset by either Reset EFP Control command or a system reset, and bits 3 and 4 can also be reset by EFP pushbuttons. The following table describes the bit meanings when on.

| Bit | Meaning |
|---|---|
| 0 | Stop on storage address compare fetch — Enables a comparison between the storage address compare register and a storage address issued by the processor during fetch operations. This bit determines the status of the corresponding EFP indicator. |
| 1 | Stop on storage address compare store — Enables a comparison between the storage address compare register and a storage address issued by the processor during store operations. This bit determines the status of the corresponding EFP indicator. |
| 2 | Stop on system check/program exception — Enables the EFP logic for this function and determines the status of the corresponding EFP indicator. |
| 3 | Enable EFP entry/display — Enables operation of EFP displays, indicators, pushbuttons, and BOP Data/Function pushbutton to register 1 and 2 information transfer. Bit status can either be programmed or changed by the Enable/Disable EF Panel pushbutton (with keylock, if installed, in Enable). |
| 4 | Access EFP register 2 — Enables access and display of EFP register 2 if on, and register 1 if reset, and determines register 1 and 2 indicator status. Bit status can either be programmed or changed by the Access Data Register 2 and Access Address Register 1 pushbuttons. |
| 5 | Processor stopped — Either an address compare stop or system check/program exception occurred, or the Stop pushbutton was pressed. |
| 6 | Operator attention — Determines the status of the corresponding indicator, which blinks twice each second. |
| 7 | Keyboard locked — Disables input and encoding of all but five EFP pushbuttons. Turned on by any "Stop on —" condition, a system check/program exception in the EFP, or a program-detected EFP error. |

### Expanded Panel Registers Other Than Control and BSTAT

This section describes EFP registers other than the control and basic status registers.

**Address Compare Register.** This 32-bit register operates in conjunction with address compare stop logic, and specifies:

- Whether a primary or secondary PSV should be active to permit a Stop on Compare (bit 3).
- The processing level that should be active to permit a Stop on Compare (bits 5–7).

**Note:** *If bits 3 and 5–7 are zeros, a Stop on Compare occurs on any processing level except zero for either PSV value.*

- The real address that should stop processing if a compare occurs (bits 12–30 with 31 ignored).

Either a system reset or a Reset Device command resets this register.

**Register 1.** A 32-bit register used for operations that can be performed either from the panel or by programming. EFP control register 4 being reset and 3 being set permits access to this register. Manual register output places the first character in the units position, which shifts to the left when entering another character. Either a system reset, Reset Device command, or the Clear Panel pushbutton resets this register.

**Register 2.** Functions identically to register 1, except that EFP control register bit 4 being set permits access to register 2.

**Current Level Register.** A read-only 4-bit register whose value results from processor logic, and cannot be programmed. It specifies the current processing level of the PSV being used, and displays this value (1–7 and not 0) in the Current or Last Level Display.

**Last Level Register.** Functions identically to the current level register, but retains the last processing level executed. Display of this level occurs in the Current or Last Level display by holding in the Display Last Level pushbutton.

**Program Mode Register.** Contains a read-only binary value that results from processor logic and cannot be programmed. The value reflects the current processing execution mode, encodes to activate one of the four Mode indicators, and cannot indicate the last processing execution mode.

**Address Mode Register.** A one-bit read-only register whose value results from processor logic and cannot be programmed. The value indicates whether the processor is currently performing real or logical addressing for the indicated PSV and current processing level, and determines the status of the DAT Active indicator. It does not indicate the last processing execution mode.

## SP240 Test Messages and Descriptions

This section describes those messages generated when running the EFP tests, which can only be run offline.

SP241 describes the messages generated while running all routines except those requiring manual intervention. SP242 describes messages used for the manual intervention routines.

### *SP241 EFP Offline Test Messages*

The messages listed below are in the RREN format, where RR indicates the routine number and EN the error number. See section SP231 for an explanation of the three error formats used.

| RREN | Format | Meaning |
|---|---|---|
| 0101 | 1 | Unexpected system check occurred. |
| 0104 | 2 | Unexpected I/O interrupt occurred. |
| 0120 | 3 | Basic status not zero after adapter reset. |
| 0121 | 3 | Register 1 low not zero after adapter reset. |
| 0122 | 3 | Register 1 high not zero after adapter reset. |
| 0123 | 3 | Register 2 low not zero after adapter reset. |
| 0124 | 3 | Register 2 high not zero after adapter reset. |
| 0125 | 3 | Control register not zero after adapter reset. |
| 0201 | 1 | Unexpected system check occurred. |
| 0204 | 2 | Unexpected I/O interrupt occurred. |
| 0220 | 3 | Status bits write/read do not compare. |
| 0221 | 3 | Extra bits reset in basic status register. |
| 0222 | 3 | Status bits not reset by Reset Status command. |
| 0301 | 1 | Unexpected system check occurred. |
| 0304 | 2 | Unexpected I/O interrupt occurred. |
| 0305 | 3 | Expected I/O interrupt did not occur. |
| 0320 | 3 | Basic status not hex 0001 after interrupt. |
| 0401 | 1 | Unexpected system check occurred. |
| 0404 | 2 | Unexpected I/O interrupt occurred. |
| 0420 | 3 | Control register write/read do not compare. |
| 0501 | 1 | Unexpected system check occurred. |
| 0504 | 2 | Unexpected I/O interrupt occurred. |
| 0520 | 3 | Register 2 high write/read do not compare. |
| 0521 | 3 | Register 2 high not zero after adapter reset. |
| 0701 | 1 | Unexpected system check occurred. |
| 0704 | 2 | Unexpected I/O interrupt occurred. |
| 0720 | 3 | Register 2 low write/read do not compare. |
| 0721 | 3 | Register 2 low not zero after adapter reset. |
| 0801 | 1 | Unexpected system check occurred. |
| 0804 | 2 | Unexpected I/O interrupt occurred. |
| 0820 | 3 | Register 1 low write/read do not compare. |
| 0821 | 3 | Register 1 low not zero after adapter reset. |
| 0901 | 1 | Unexpected system check occurred. |
| 0904 | 2 | Unexpected I/O interrupt occurred. |
| 0920 | 3 | Register 1 high write/read do not compare. |
| 0921 | 3 | Register 1 high not zero after adapter reset. |
| 1001 | 1 | Unexpected system check occurred. |
| 1004 | 2 | Unexpected I/O interrupt occurred. |
| 1005 | 3 | Expected I/O interrupt did not occur. |
| 1020 | 3 | Basic status incorrect after interrupt. |
| 1101 | 1 | Unexpected system check occurred. |
| 1104 | 2 | Unexpected I/O interrupt occurred. |
| 1120 | 3 | No address compare interrupt. |
| 1121 | 3 | Basic status incorrect after interrupt. |
| 1201 | 1 | Unexpected system check occurred. |
| 1204 | 2 | Unexpected I/O interrupt occurred. |
| 1220 | 3 | No address compare interrupt at address hex 5554. |
| 1221 | 3 | Basic status incorrect after interrupt. |
| 1222 | 3 | No address compare interrupt at address hex AAAA. |
| 1301 | 1 | Unexpected system check occurred. |
| 1304 | 2 | Unexpected I/O interrupt occurred. |
| 1320 | 3 | Received an address compare when none should have occurred. |
| 1321 | 3 | Extended status incorrect. |
| 1401 | 1 | Unexpected system check occurred. |
| 1404 | 2 | Unexpected I/O interrupt occurred. |
| 1420 | 3 | Received an address compare on incorrect level. |
| 1421 | 3 | Did not receive an address compare. |
| 1422 | 3 | Extended status incorrect. |
| 1501 | 1 | Unexpected system check occurred. |
| 1504 | 2 | Unexpected I/O interrupt occurred. |
| 1520 | 3 | Either no address compare occurred or it occurred late in the MVHS instruction. |
| 1601 | 1 | Unexpected system check occurred. |
| 1604 | 2 | Unexpected I/O interrupt occurred. |
| 1620 | 3 | Received an address compare on the target of an unsuccessful branch. |

| RREN | Format | Meaning |
|---|---|---|
| 1701 | 1 | Unexpected system check occurred. |
| 1704 | 2 | Unexpected I/O interrupt occurred. |
| 1720 | 3 | Did not receive an address compare before taking program exception. |
| 1721 | 3 | Did not receive an address compare on second half of MVHS just before a KI swap. |
| 1801 | 1 | Unexpected system check occurred. |
| 1804 | 2 | Unexpected I/O interrupt occurred. |
| 1820 | 3 | Panel operation did not stop on system check. |
| 1821 | 3 | Panel operation did not stop on program exception. |
| 1901 | 1 | Unexpected system check occurred. |
| 1904 | 2 | Unexpected I/O interrupt occurred. |
| 1920 | 3 | Invalid command did not cause a system check. |
| 1921 | 3 | Basic status incorrect after invalid command. |
| 2001 | 1 | Unexpected system check occurred. |
| 2004 | 2 | Unexpected I/O interrupt occurred. |
| 2101 | 1 | Unexpected system check occurred. |
| 2104 | 2 | Unexpected I/O interrupt occurred. |
| 2121 | 3 | Basic status incorrect after pressing Store. |
| 2123 | 3 | Basic status incorrect after pressing Display. |
| 2125 | 3 | Basic status incorrect after pressing Function. |
| 2127 | 3 | Basic status incorrect after pressing Insn Step. |
| 2129 | 3 | Basic status incorrect after pressing Start. |
| 2131 | 3 | Basic Status incorrect after pressing Stop. |
| 2133 | 3 | Basic status incorrect after pressing Reset/Restore. |
| 2135 | 3 | Basic status incorrect after pressing Storage Address Compare Stop Fetch. |
| 2137 | 3 | Basic status incorrect after pressing Storage Address Compare Stop Store. |
| 2139 | 3 | Basic status incorrect after pressing Stop on System Check/Program Excpn. |
| 2201 | 1 | Unexpected machine check occurred. |
| 2204 | 2 | Unexpected I/O interrupt occurred. |
| 2221 | 2 | Basic status incorrect after pressing Storage Location. |
| 2222 | 3 | Basic status incorrect after pressing Register. |
| 2223 | 3 | Basic status incorrect after pressing Translatn Table Entry. |
| 2224 | 3 | Basic status incorrect after pressing Address Control. |
| 2225 | 3 | Basic status incorrect after pressing Insn Address. |
| 2236 | 3 | Basic status incorrect after pressing Program Status. |
| 2237 | 3 | Basic status incorrect after pressing Compare Stop Address. |
| 2238 | 3 | Basic status incorrect after pressing Transform Address. |
| 2301 | 1 | Unexpected system check occurred. |
| 2304 | 2 | Unexpected I/O interrupt occurred. |
| 2401 | 1 | Unexpected system check occurred. |
| 2404 | 2 | Unexpected I/O interrupt occurred. |
| 2421 | 3 | Basic status incorrect after pressing Start. |
| 2424 | 3 | Modifier bit in basic status not reset by pressing Clear Panel. |
| 2425 | 3 | Reg 1 not zero after pressing Clear Panel. |
| 2426 | 3 | Reg 2 not zero after pressing Clear Panel. |
| 2427 | 3 | Control register incorrect after pressing Clear Panel. |
| 2501 | 1 | Unexpected system check occurred. |
| 2504 | 2 | Unexpected I/O interrupt occurred. |
| 2601 | 1 | Unexpected system check occurred. |
| 2604 | 2 | Unexpected I/O interrupt occurred. |
| 2701 | 1 | Unexpected system check occurred. |
| 2704 | 2 | Unexpected I/O interrupt occurred. |
| 2801 | 1 | Unexpected system check occurred. |
| 2804 | 2 | Unexpected I/O interrupt occurred. |
| 2901 | 1 | Unexpected system check occurred. |
| 2904 | 2 | Unexpected I/O interrupt occurred. |
| 2922 | 3 | DAT Active indicator did not turn on. |
| 3001 | 1 | Unexpected system check occurred. |
| 3004 | 2 | Unexpected I/O interrupt occurred. |
| 3020 | 3 | Supervisor mode indicator not on. |
| 3023 | 3 | Master mode indicator did not turn on, then off. |
| 3025 | 3 | I/O mode indicator did not turn on, then off. |
| 3027 | 3 | Appl mode indicator did not turn on, then off. |
| 3101 | 1 | Unexpected system check occurred. |
| 3104 | 2 | Unexpected I/O interrupt occurred. |

## *SP242 Manual Intervention Test Messages and Procedures*

The following table describes the actions required for the test messages that display when performing the EFP manual intervention routines. In the PAMI column, PA = the EFP physical address and MI = the manual intervention number.

| PAMI | Procedure |
|---|---|
| 0A01 | If Operator Attention indicator blinks, enter B. |
| 0A02 | Press Store. |
| 0A03 | Press Display. |
| 0A04 | Press Function. |
| 0A05 | Press Insn Step. |
| 0A06 | Press Start. |
| 0A07 | Press Stop. |
| 0A08 | Press Reset/Restore. |
| 0A09 | Press Storage Address Compare Stop Fetch. |
| 0A10 | Press Storage Address Compare Stop Store. |
| 0A11 | Press Stop On System Check/Program Excpn. |
| 0A12 | Press Storage Location and then press Start. |
| 0A13 | Press Register and then press Start. |
| 0A14 | Press Translatn Table Entry and then press Start. |
| 0A15 | Press Address Control and then press Start. |
| 0A16 | Press Insn Address and then press Start. |
| 0A17 | Press Program Status and then press Start. |
| 0A18 | Press Compare Stop and then press Start. |
| 0A19 | Press Transform Address and then press Start. |
| 0A20 | Reg 1 indicator = on and display = 00000000. Enter B if correct. |
| 0A21 | Reg 2 indicator = on and display = 00000000. Enter B if correct. |
| 0A22 | Reg 1 indicator = on and display = 11111111. Enter B if correct. |
| 0A23 | Reg 2 indicator = on and display = 11111111. Enter B if correct. |
| 0A24 | Reg 1 indicator = on and display = 22222222. Enter B if correct. |
| 0A25 | Reg 2 indicator = on and display = 22222222. Enter B if correct. |
| 0A26 | Reg 1 indicator = on and display = 33333333. Enter B if correct. |
| 0A27 | Reg 2 indicator = on and display = 33333333. Enter B if correct. |
| 0A28 | Reg 1 indicator = on and display = 44444444. Enter B if correct. |
| 0A29 | Reg 2 indicator = on and display = 44444444. Enter B if correct. |
| 0A30 | Reg 1 indicator = on and display = 55555555. Enter B if correct. |
| 0A31 | Reg 2 indicator = on and display = 55555555. Enter B if correct. |
| 0A32 | Reg 1 indicator = on and display = 66666666. Enter B if correct. |
| 0A33 | Reg 2 indicator = on and display = 66666666. Enter B if correct. |
| 0A34 | Reg 1 indicator = on and display = 77777777. Enter B if correct. |
| 0A35 | Reg 2 indicator = on and display = 77777777. Enter B if correct. |
| 0A36 | Reg 1 indicator = on and display = 88888888. Enter B if correct. |
| 0A37 | Reg 2 indicator = on and display = 88888888. Enter B if correct. |
| 0A38 | Reg 1 indicator = on and display = 99999999. Enter B if correct. |
| 0A39 | Reg 2 indicator = on and display = 99999999. Enter B if correct. |
| 0A40 | Reg 1 indicator = on and display = AAAAAAAA. Enter B if correct. |
| 0A41 | Reg 2 indicator = on and display = AAAAAAAA. Enter B if correct. |
| 0A42 | Reg 1 indicator = on and display = BBBBBBBB. Enter B if correct. |
| 0A43 | Reg 2 indicator = on and display = BBBBBBBB. Enter B if correct. |
| 0A44 | Reg 1 indicator = on and display = CCCCCCCC. Enter B if correct. |
| 0A45 | Reg 2 indicator = on and display = CCCCCCCC. Enter B if correct. |
| 0A46 | Reg 1 indicator = on and display = DDDDDDDD. Enter B if correct. |
| 0A47 | Reg 2 indicator = on and display = DDDDDDDD. Enter B if correct. |
| 0A48 | Reg 1 indicator = on and display = EEEEEEEE. Enter B if correct. |
| 0A49 | Reg 2 indicator = on and display = EEEEEEEE. Enter B if correct. |
| 0A50 | Reg 1 indicator = on and display = FFFFFFFF. Enter B if correct. |
| 0A51 | Reg 2 indicator = on and display = FFFFFFFF. Enter B if correct. |
| 0A52 | Press Enable/Disable EF Panel and then press Start. |
| 0A53 | If Operator Attention indicator blinks, enter B. |
| 0A54 | Press Clear Panel and then enter B. |
| 0A55 | Press Access Address Register1 pushbutton. The Reg 1 indicator should turn on and the display should be 11111111. Enter B if true. |
| 0A56 | Press Access Data Register 2. The Reg 2 indicator should turn on and the display should be 22222222. Enter B if true. |
| 0A57 | Exercise the hex keypad. Keys pressed should be displayed in the data display, entering from the right and moving to the left as keys are pressed. Press Access Address Register 1 and Access Data Register 2 to verify that register 1 and 2 both operate from the keypad. Press Stop to end test. |
| 0A58 | Keypad, register 1, and register 2 functioned correctly. Enter B if true. |
| 0A59 | Keypad does not work and Keyboard Locked indicator = on. Enter B if true. |
| 0A60 | Enter B if the Storage Address Compare Stop Fetch indicator = on. |
| 0A61 | Enter B if the Storage Address Compare Stop Store indicator = on. |
| 0A62 | Enter B if the Stop on System Check/Program Excpn indicator = on. |
| 0A63 | Enter B if the Processor Stopped indicator = on. |
| 0A64 | Enter B if the Panel Check indicator = on. |
| 0A65 | Press Clear Panel. The Panel Check indicator = off. Enter B if true. |
| 0A66 | Press Start. This should turn the DAT Active indicator on. If on, press Start. If off, press Stop. |

| PAMI | Procedure |
|---|---|
| 0A67 | Supervisor mode indicator = on. Enter B if on. |
| 0A68 | Press Start. This should cause the Master mode indicator to turn on, then off. If correct, press Start. If incorrect, press Stop. |
| 0A69 | Press Start. This should cause the I/O mode indicator to turn on, then off. If correct, press Start. If incorrect, press Stop. |
| 0A70 | Press Start. This should cause the Appl mode indicator to turn on, then off. If correct, press Start. If incorrect, press Stop. |
| 0A71 | The level indicator steps slowly and the expected level and mode are displayed. Enter B. |
| 0A72 | Test ran correctly. Enter B if true. |
| 0A74 | Enter 1 for short test. Enter 0 for long test. Used in Routine 23. |

## SP250 Action Plans

Action plans for correcting EFP failures are divided into three categories:

- Visually detected failures
- Adapter logic failures
- Panel failures

The test and manual intervention routines might refer you to one of the action plans in this section for problem isolation and recovery.

### *EFP Initial Action Plan Procedure*

The first procedure used for EFP fault isolation is to reseat the cards and connections. Before performing any of the individual action plans, you should reseat the following:

1. Adapter card
2. Adapter top card cables
3. EFP keypad connectors
4. Hex display card connectors
5. Mode and state indicator card connectors
6. Cable in position B2A3 on the BOP adapter card, 01B-A1A2

Refer to SP111 for EFP card and cable layouts, and BU111 for the BOP card and cable layouts. After performing the above procedure, again run the adapter tests and manual intervention routines. Return to this section if a problem still exists.

### *Action Plan Summary*

The following table should be used according to the failure indication. Find the failure in the Action Plan column, then go to the specified section to perform the action plan.

| Action Plan | Section |
|---|---|
| Visually detected failure | SP251* |
| Adapter logic failure | SP252 |
| Panel failure<br>Keypad failure<br>Hex display card failure<br>Mode and state indicator card failure | SP253 |
| Cable Check | SP254 |

* Use the action plan in SP251 only for fault isolation without MAP interaction. When the MAP refers you to SP250, first perform the Initial Action Plan Procedure described above. If the problem still exists, go to either SP252, SP253, or SP254, according to the failure indication.

### *SP251 Visually-Detected Failure Action Plans*

Use the following action plans only for any failure that can be detected visually:

| Probable Cause | Action |
|---|---|
| Pushbutton or LEDs | Observe condition of pushbuttons and hex displays. Any obvious loose or broken pushbuttons, or faulty LEDs indicate that the affected panel component should be replaced. |
| Indicators | Press Lamp Test on the BOP. If any indicators fail to turn on, replace the affected panel component. |
| Unknown | A visual panel failure can also be caused by other failures. The MAP and test program help to further isolate the problem. |

## *SP252 Adapter Failure Action Plans*

The following action plans isolate EFP adapter failures to either voltage, card, board, bus, or card-to-panel signal path problems. These action plans assume that both bring up tests and the system control facility (SC) MAP ran successfully. After performing this action plan, select the EFP test to verify any repair.

| Probable Cause | Action | Comment |
|---|---|---|
| Voltage | Check all dc voltages at the EFP adapter card socket.<br>D03 = +4.5 to +5.5V<br>B11 = +7.7 to +9.3V<br>B06 = –4.5 to –5.5V | If no voltage, or if voltage is out of tolerance, go to the PA MAP. |
| Card | Change the adapter card, if not already done, and return to the MAP. | For models A31–34, card is in board location A1M2.<br>For other A models, card is in A1P2.<br>For B models, card is in A1S2. |
| Bus | Change the SC1 card. Return to the MAP. | Card location 01A-A1A2 for A models.<br>Card location 01A-A1D2 for B models. |
| Card-to-Panel | Go to the cable check action plan SP254 | |
| Board | Check board wiring. | For net listings, go to SP410. |
| Unknown | Request aid. | |



## *SP253 Panel Failure Action Plans*

The panel failure action plans are grouped according to the three field replaceable panel units: EFP keyboard card, hexadecimal display card, and mode and state indicator card.

Use the description of the failing routine (SP212) to help select the proper action plan.

### Keypad Failure Action Plan

Use the following action plan for failures relating to the EFP keypad:

| Probable Cause | Action | Comment |
|---|---|---|
| Card | Replace the EFP adapter card. Return to MAP. | For models A31–34, card is in board location A1M2.<br>For other A models, card is in A1P2.<br>For B models, card is in A1S2. |
| Card-to-Panel | If the problem has not been solved, go to the cable check action plan. | See SP254. |
| Shorted or Stuck Keys | Use this action plan for manual intervention numbers 0A02-0A19, 0A52, 0A54, 0A55, 0A56, 0A71, 0A72, 0A73<br><br>Check for shorted, open, or binding pushbuttons according to the following list of J6 connector pins. | See SP430 for pin and connector locations.<br><br>If any switches are shorted or open, replace the EFP keypad and skip the next action plan. (See SP520) |
| Open Switches | Meter the J6 connector pins on the EFP keypad and press the corresponding keypad keys as follows:<br><br>J6–12 to J6–3<br>Clear Panel<br>J6–12 to J6–4<br>Transform Address<br>J6–12 to J6–5<br>Storage Address Compare Stop Fetch<br>J6–12 to J6–6<br>Storage Address Compare Stop Store<br>J6–12 to J6–7<br>Stop on System Check/ Program Excpn<br>J6–11 to J6–3<br>Store | |

(SP242 Cont–SP253)

| Probable Cause | Action | Comment |
|---|---|---|
| | J6–11 to J6–4<br>Storage Location<br>J6–11 to J6–5<br>Address Control<br>J6–11 to J6–6<br>Compare Stop Address<br>J6–11 to J6–7<br>Display Last Level<br>J6–10 to J6–3<br>Display<br>J6–10 to J6–4<br>Register<br>J6–10 to J6–5<br>Insn Address<br>J6–10 to J6–7<br>Access Address Reg 1<br>J6–9 to J6–3<br>Function<br>J6–9 to J6–4<br>Translatn Table Entry<br>J6–9 to J6–5<br>Program Status<br>J6–9 to J6–7<br>Access Data Reg 2<br>J6–8 to J6–3<br>Enable/Disable EF Panel<br>J6–8 to J6–4<br>Insn Step<br>J6–8 to J6–5<br>Start<br>J6–8 to J6–6<br>Stop<br>J6–8 to J6–7<br>Reset/Restore<br><br>After replacing the keypad, be sure that the face plate is aligned and all pushbuttons do not bind on the face plate before tightening the panel screws. | See SP520 for instructions on replacing the EFP keypad. |
| Board | Check board wiring. | For net listing, see SP410. |
| BOP Card | Replace the BOP adapter card if not already done and return to MAP. | Position 01B-A1A2 |
| BOP Card-to-Panel | If the problem still exists, go to the cable check action plan. | See SP254. |
| Board | Check board wiring. | For net listing, see SP410. |
| | Request aid. | |

**Hex Display Card Failure Action Plan**

Use the following action plan for failures relating to the hexadecimal display card that result from MI prompt messages 0A01, 0A20-0A51, 0A53-0A55, 0A59, 0A64-0A66, 0A71, 0A73, and 0A74.

| Probable Cause | Action | Comment |
|---|---|---|
| Card | Replace the EFP adapter card if not already done and return to MAP. | Card location on models A31–34: A1M2. Other A models: A1P2. B models: A1S2. |
| | Check board wiring. | For net listing, see SP410. |
| Card-to-Panel | Go to cable check action plan. | See SP254. |
| Hex Display | Replace hex display card. | See SP530 for instructions on replacing the hex display card. |
| BOP Card-to-Panel | Check cabling from the BOP adapter. | |
| Board | Check board wiring. | |
| Unknown | Request aid. | |

**Mode and State Indicator Card Failure Action Plan**

Use the following action plan for failures relating to the mode and state indicator card that result from MI prompt messages 0A59-0A63 and 0A67-0A70.

| Probable Cause | Action | Comment |
|---|---|---|
| Card | Replace the EFP adapter card if not already done and return to MAP. | Card location on models A31–34: A1M2. Other A models: A1P2. B models: A1S2. |
| Card-to-Panel | If the problem still exists, go to the cable check action plan. | See SP254. |
| Mode and State Indicator Card | If problem still exists, replace the mode and indicator card on the EFP. | See SP540 for instructions on replacing the mode and state indicator card. |
| Voltage at Mode and Indicator Card | Check voltage to mode and indicator card. | |
| Unknown | Request aid. | |

*SP254 Cable Check Action Plan*

| Probable Cause | Action | Comment |
|---|---|---|
| Card-to-Panel Cables | Check to be sure the connections between the appropriate top card connector and the EFP component or power section affected are good. | Figures SP254-2, -3, -4, and -5 illustrate the connections between top card connectors W, X, Y, and Z respectively, and the EFP components. Figure SP254-1 shows the power connections for the hex display card and mode and state indicator card. |

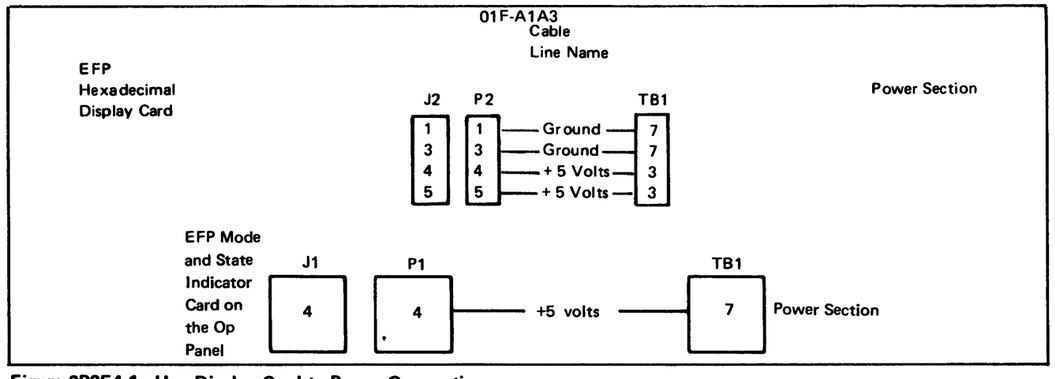



**Figure SP254-1. Hex Display Card-to-Power Connections**

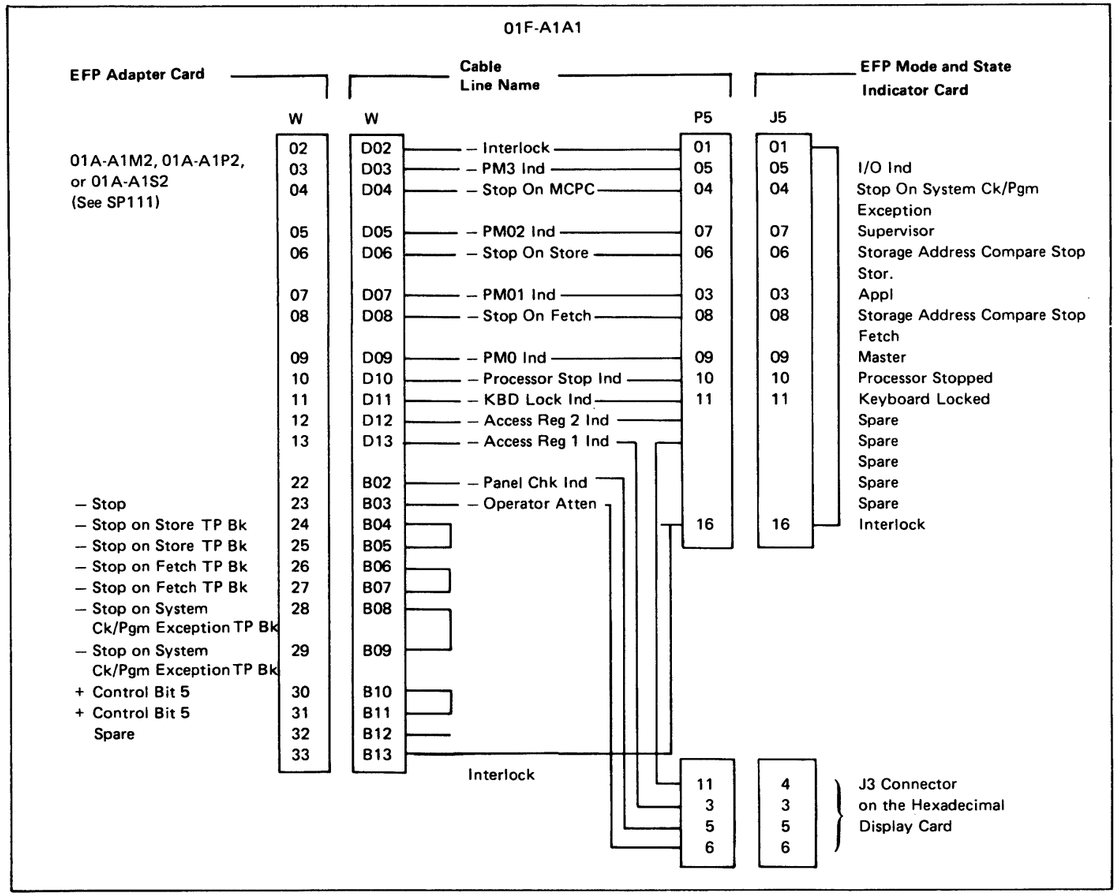



**Figure SP254-2. EFP Adapter Card-to-EFP Mode and State Indicator Card Wiring**

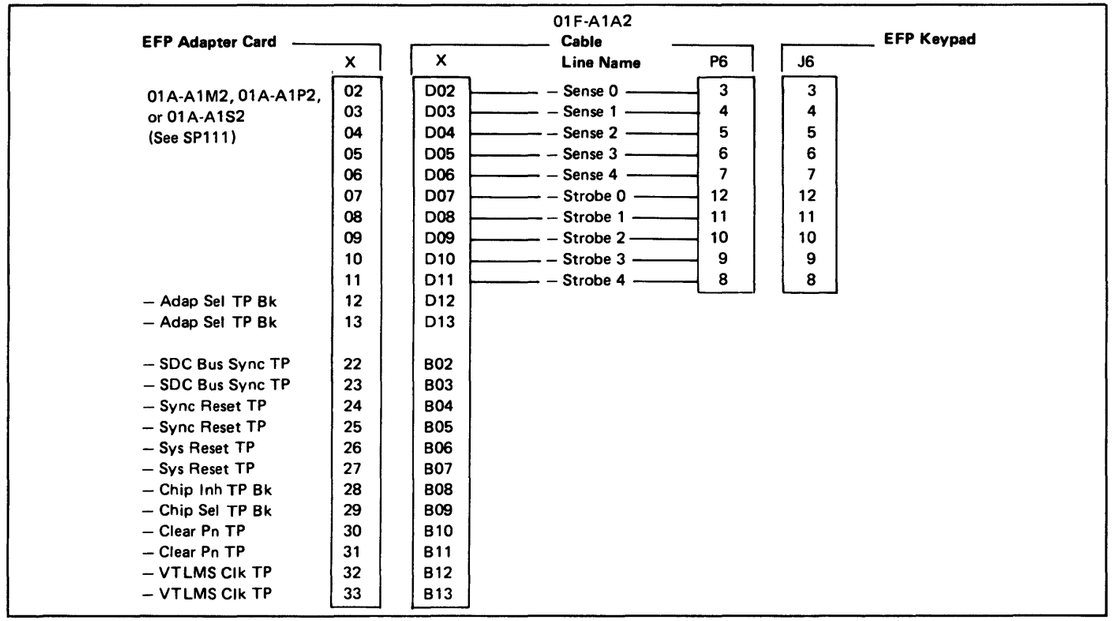



**Figure SP254-3. EFP Adapter Card-to-EFP Keypad Wiring**

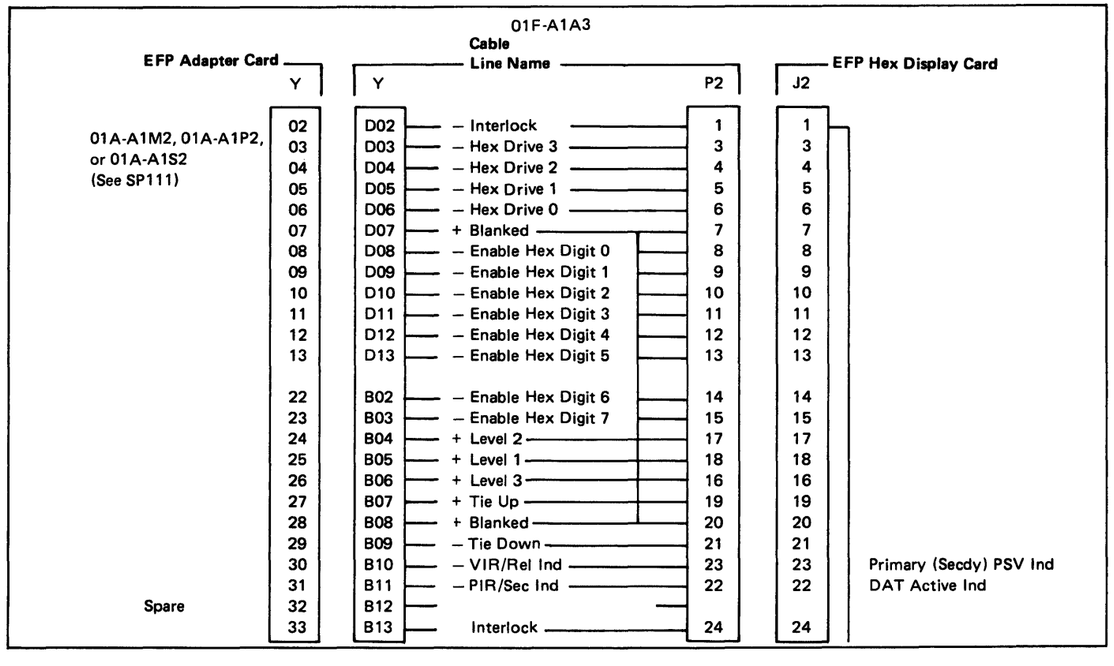



**Figure SP254-4. EFP Adapter Card-to-EFP Hex Display Card Wiring**

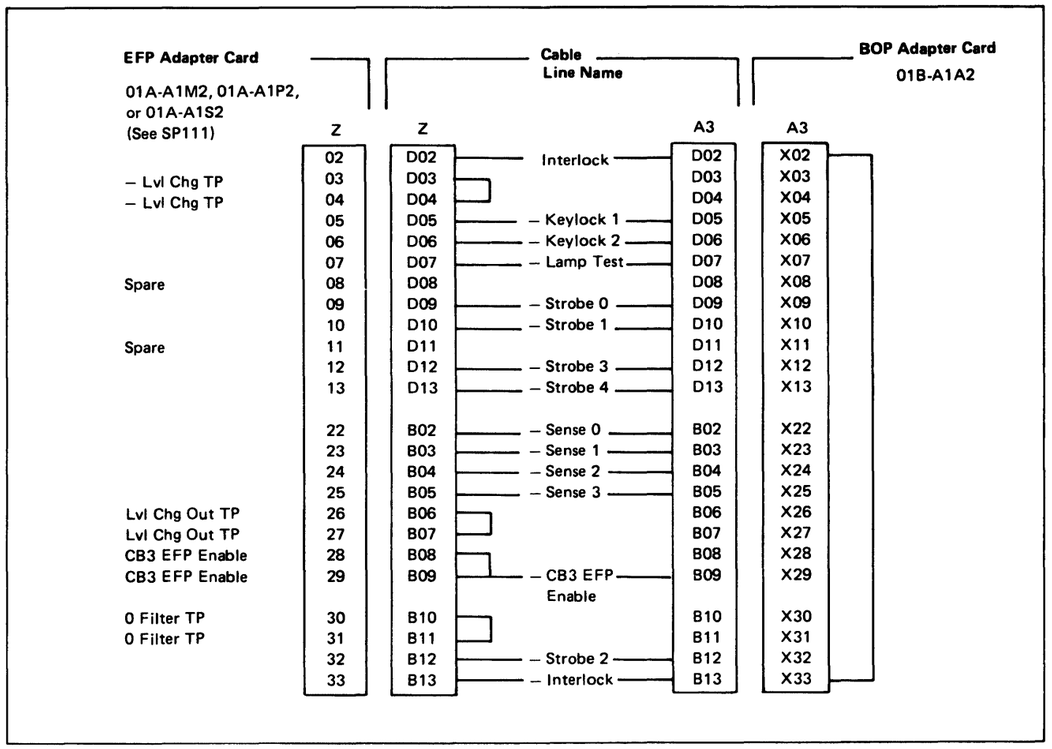



**Figure SP254-5. EFP Adapter Card-to-BOP Adapter Card Wiring**

## SP300 Intermittent Failure Repair Strategy

Intermittent failures can possibly never be detected, or might indicate different test error messages while running the test. Intermittent failures make the MAPs ineffective. To resolve this type of problem, you should record all information relating to the problem, such as the failing operation, visual symptoms, test error messages, and any other pertinent information. Refer to section SP350 for fault isolation of intermittent failures.

## SP310 Adapter-Unique Intermittent Repair Strategy

For intermittent failures that could possibly be caused by the EFP, obtain the system error log and use this information to determine if there might be an EFP problem. Refer to Chapter 2 for information on obtaining the error log. Use these results to develop your own action plan.

## SP350 Action Plan to Correct Intermittent Failures

Perform the following action plan, in order, from top to bottom. Any time you perform a repair action, action, you must run the expanded function panel tests to verify the repair.

| Probable Cause | Action | Comments |
|---|---|---|
| Unknown | Make sure that the bringup and System Control Facility tests have run correctly. | |
| Voltage | Check all dc voltages at EFP adapter card socket.<br>D03 = +4.5 to +5.5V<br>B11 = +7.7 to +9.3V<br>B06 = –4.5 to –5.5V | If missing or out of tolerance, go to PA MAP. |
| Adapter card defective | Change card. | |
| Board or bus | 1. Change PSCF card and BOP adapter card.<br>2. Check board wiring. See section SP410. | |
| Adapter to panel signal path | Go to the panel failure action plan, SP250. | |
| Failure still unknown | Request aid. | |

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## SP400 Signal Paths and Detailed Operational Description

This section contains information that is not usually necessary for fault isolation but assists in understanding EFP hardware operation.

### SP410 Point-to-Point Signal Path

Figure SP410-1 lists the signal lines by name from the processor to the EFP for most A models. Use the chart below for other models.

**Note:** *The "XX" designation is used for the storage card positions. See Chapter 3 for locations.*

Card locations on 01A-A1 board for various 8140 models:

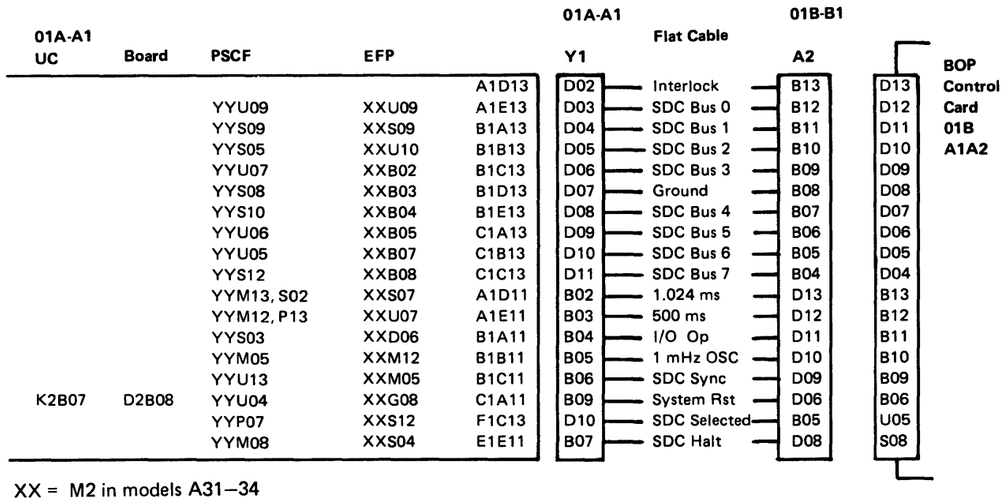
| Model Nos. | Processor | | | | | | | PSCF | STOR | FLT PT | EFP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | PICO ROS | ROS Decode | I/O & Intrpts | Princ Reg Stor | Instr Decode | Adj Reg Stor | Storage Addr | | | | |
| A51–54 | No EFP Feature Available | | | | | | | | | | |
| A31–34 | C2 | D2 | E2 | G2 | H2 | J2 | K2 | A2 | XX | – | M2 |
| Other A Models | C2 | D2 | E2 | G2 | H2 | J2 | K2 | A2 | XX | M2 | P2 |
| B Models | F2 | G2 | H2 | K2 | L2 | M2 | N2 | D2 | XX | Q2 | S2 |

| Net | Processor | Processor | PSCF | Flt Pt | EFP | Conn | BOPA |
|---|---|---|---|---|---|---|---|
| Wait St Gate | C2D02 | E2M10 | A2G07 | | P2D02 | | |
| PM 0 | J2M07 | H2G04 | A2P05 | M2G04 | P2D09 | | |
| System Reset | K2B07 | D2B08 | A2U04 | M2B07 | P2G08 | C1A11 | A2B06 |
| EFP Int Req | | | A2S07 | | P2D04 | | |
| SDC Bus 0 | | | A2U09 | | P2U09 | A1E13 | A2D12 |
| SDC Bus 1 | | | A2S09 | | P2S09 | B1A13 | A2D11 |
| SDC Bus 2 | | | A2S05 | | P2U10 | B1B13 | A2D10 |
| SDC Bus 3 | | | A2U07 | | P2B02 | B1C13 | A2D09 |
| SDC Bus 4 | | | A2S08 | | P2B03 | B1D13 | A2D08 |
| SDC Bus 5 | | | A2S10 | | P2B04 | B1E13 | A2D07 |
| SDC Bus 6 | | | A2U06 | | P2B05 | C1A13 | A2D06 |
| SDC Bus 7 | | | A2U05 | | P2B07 | C1B13 | A2D05 |
| SDC Bus 8 | | | A2S12 | | P2B08 | C1C13 | A2D04 |
| SDC Selected | | | A2P07 | | P2S12 | F1C13 | A2U05 |
| SDC Sync | | | A2U13 | | P2M05 | B1C11 | A2B09 |
| SDC Halt | | | A2M08 | | P2S04 | E1E11 | A2S08 |
| I/O Op | | | A2S03 | | P2D06 | B1A11 | A2B11 |
| 1 MHz Osc | | | A2M05 | | P2M12 | B1B11 | A2B10 |
| 500 ms | | | A2M12, P13 | | P2U07 | A1E11 | A2B12 |
| 1024 ms | | | A2M13, S02 | | P2S07 | A1D11 | A2B13 |

| Net | Processor | Processor | Processor | Storage | Flt Pt | EFP | Conn | BOPA |
|---|---|---|---|---|---|---|---|---|
| Sys Ck Not 0 | | | D2J07 | | | P2J07 | F1B13 | A2U06 |
| Pic Bit 0 | | J2B08 | D2D12 | | | P2D12 | | |
| PM 1 | K2D07 | J2P02 | H2D07 | | | P2D07 | | |
| R/V | | | K2B10 | | | P2B10 | | |
| ROS Stor Ctrl 1 | K2D11 | J2D13 | C2D13 | | | P2D13 | | |
| T2 | E2M05 | D2P11 | C2P11 | | | P2J06 | | |
| I Fetch | | | D2G07 | | M2G08 | P2G07 | | |
| Exit | H2D11 | E2P09 | D2D11 | | | P2D05 | | |
| Long Insn | | H2M09 | D2P04 | | | P2G09 | | |
| PSV Switch | | | E2S09 | | | P2D10 | | |
| Stk Adr Bus 9 | J2P13 | G2G13 | E2G13 | | | P2M12 | | |
| Stk Adr Bus 11 | J2M10 | G2M10 | E2U13 | | M2J10 | P2P11 | | |
| Stk Adr Bus 12 | J2P04 | G2P04 | E2U07 | | M2G02 | P2P05 | | |
| Stk Adr Bus 13 | J2M09 | G2M09 | E2S03 | | M2G05 | P2P07 | | |
| PSV 2 | K2J06 | J2S12 | E2S12 | | M2J06 | P2U02 | | |
| Stor Adr Bus 0 | | | K2P13 | XXU13/S12 | | P2P13 | | |
| Stor Adr Bus 1 | | | K2P12 | XXU12 | | P2P12 | | |
| Stor Adr Bus 2 | | | K2M08 | XXS07 | | P2M08 | | |
| Stor Adr Bus 3 | | | K2P06 | XXU05 | | P2P06 | | |
| Stor Adr Bus 4 | | | K2M03 | XXS03 | | P2M03 | | |
| Stor Adr Bus 5 | | | K2M04 | XXS04 | | P2M04 | | |
| Stor Adr Bus 6 | | | K2M10 | XXS09 | | P2M10 | | |
| Stor Adr Bus 7 | | | K2P09 | XXU09 | | P2P09 | | |
| Stor Adr Bus 8 | | | K2P10 | XXU10 | | P2P10 | | |
| Stor Adr Bus 9 | | | K2M09 | XXS08 | | P2M09 | | |
| Stor Adr Bus 10 | | | K2M13 | XXS10 | | P2M13 | | |
| Stor Adr Bus 11 | | | K2M07 | XXS05 | | P2M07 | | |
| Stor Adr Bus 12 | | | K2P04 | XXU04 | | P2P04 | | |
| Stor Adr Bus 13 | | | K2P02 | XXU02 | | P2P02 | | |
| Stor Adr Bus 14 | | | K2M09 | XXS02 | | P2M02 | | |
| Stor Write Hi | | | K2S02 | XXB13 | | P2S02 | | |
| Stor Write Lo | | | K2S03 | XXD13 | | P2S03 | | |
| Stor Sel 0 | | | K2J09 | XXU11 | | P2J09 | | |
| Stor Sel 1 | | | K2J11 | XXU11 | | P2J11 | | |
| Stor Sel 2 | | | K2J12 | XXU11 | | P2J12 | | |
| Stor Sel 3 | | | K2J13 | XXU11 | | P2J13 | | |
| Stor Sel 4 | | | K2P05 | XXU11 | | P2G12 | | |
| Stor Sel 5 | | | K2P07 | XXU11 | | P2G10 | | |
| Stor Sel 6 | | | K2U04 | XXU11 | | P2J10 | | |
| Stor Sel 7 | | | K2P11 | XXU11 | | P2G13 | | |

**Figure SP410-1. EFP Point-to-Point Signal Path**

Figure SP410-2 shows the processor-PSCF-BOPA card signal path.




XX = M2 in models A31–34
P2 in other A models
S2 in B models

YY = A2 in A models
D2 in B models

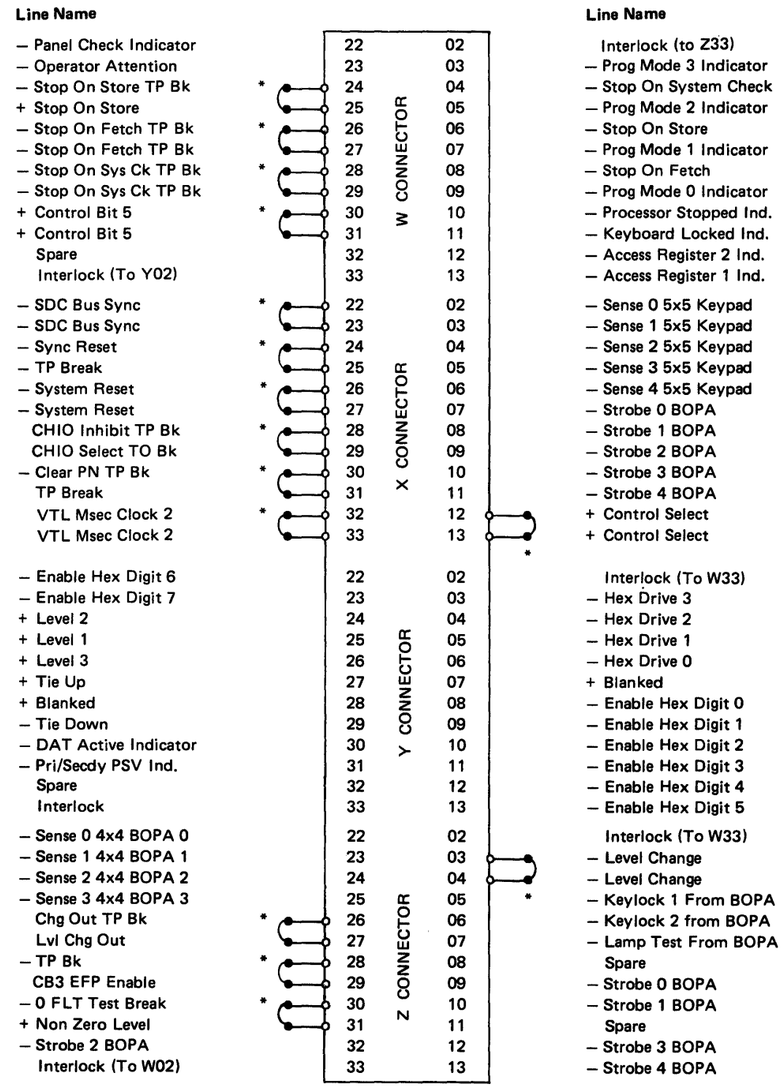
**Figure SP410-2. Processor-PSCF-BOPA Card Signal Path**

## SP420 Card and Top Card Connector Signals

Figures SP420-1 and SP420-2 show line names of the respective pins when the EFP adapter card plugs into any of the three possible board positions.

| Line Name | | | Line Name |
|---|---|---|---|
| – Wait State Gate | D02 | B02 | – SDC Bus 3 |
| + 5V | D03 | B03 | – SDC Bus 4 |
| – Panel Interrupt Req | D04 | B04 | – SDC Bus 5 |
| + Enable/Disable Panel | D05 | B05 | – SDC Bus 6 |
| – I/O Operation | D06 | B06 | – 5V |
| + Primary Mode 1 | D07 | B07 | – SDC Bus 7 |
| Ground | D08 | B08 | – SDC Bus P |
| + Primary Mode 0 | D09 | B09 | |
| – PSV Switch Gate | D10 | B10 | – DAT Active |
| | D11 | B11 | + 8.5V |
| – PIC Bit 0 | D12 | B12 | |
| – Stop Request | D13 | B13 | |
| – Select 1M Storage | J02 | G02 | – Compare Equal TP |
| | J03 | G03 | – Compare Equal TP |
| | J04 | G04 | |
| | J05 | G05 | |
| | J06 | G06 | – 5 Volts |
| – System Check Not Zero | J07 | G07 | – I Fetch |
| | J08 | G08 | – System Reset/Restore |
| – Storage Select Bit 0 | J09 | G09 | – Long Instruction |
| – Storage Select Bit 6 | J10 | G10 | – Storage Select Bit 5 |
| – Storage Select Bit 1 | J11 | G11 | – 8.5 Volts |
| – Storage Select Bit 2 | J12 | G12 | – Storage Select Bit 4 |
| – Storage Select Bit 3 | J13 | G13 | – Storage Select Bit 7 |
| – Storage Adr Bus 13 | P02 | M02 | – Storage Adr Bus 14 |
| | P03 | M03 | – Storage Adr Bus 4 |
| – Storage Adr Bus 12 | P04 | M04 | – Storage Adr Bus 5 |
| – Stack Adr Bus 12 | P05 | M05 | – SDC Bus Sync |
| – Storage Adr Bus 3 | P06 | M06 | – 5 Volts |
| – Stack Adr Bus 13 | P07 | M07 | – Storage Adr Bus 11 |
| | P08 | M08 | – Storage Adr Bus 2 |
| – Storage Adr Bus 7 | P09 | M09 | – Storage Adr Bus 9 |
| – Storage Adr Bus 8 | P10 | M10 | – Storage Adr Bus 6 |
| – Stack Adr Bus 11 | P11 | M11 | + 8.5 Volts |
| – Storage Adr Bus 1 | P12 | M12 | – Stack Adr Bus 9 |
| – Storage Adr Bus 0 | P13 | M13 | – Storage Adr Bus 10 |
| – PSV 2 | U02 | S02 | – Storage Write Hi |
| | U03 | S03 | – Storage Write Lo |
| – 1 Megahertz Osc | U04 | S04 | – SDC Halt |
| Clock TP | U05 | S05 | – 1 Megahertz Osc |
| Ground | U06 | S06 | – 5 Volts |
| – 500 Ms Rate Clock | U07 | S07 | – 1.024 Ms Rate Clock |
| | U08 | S08 | |
| – SDC Bus 0 | U09 | S09 | – SDC Bus 1 |
| – SDC Bus 2 | U10 | S10 | |
| | U11 | S11 | + 8.5 Volts |
| | U12 | S12 | – SDC Selected |
| | U13 | S13 | |

**Figure SP420-1. EFP Adapter Card Signal Lines (Pin Side)**




* These jumpers are physically in the top card connectors.

**Figure SP420-2. EFP Adapter Card Signal Lines (Card Side)**

## SP430 Expanded Panel FRU Component and Connector Diagrams

Figures SP430-1 through SP430-8 show the physical layout and wiring of the EFP keypad card, mode and state indicator card, and hex display card.

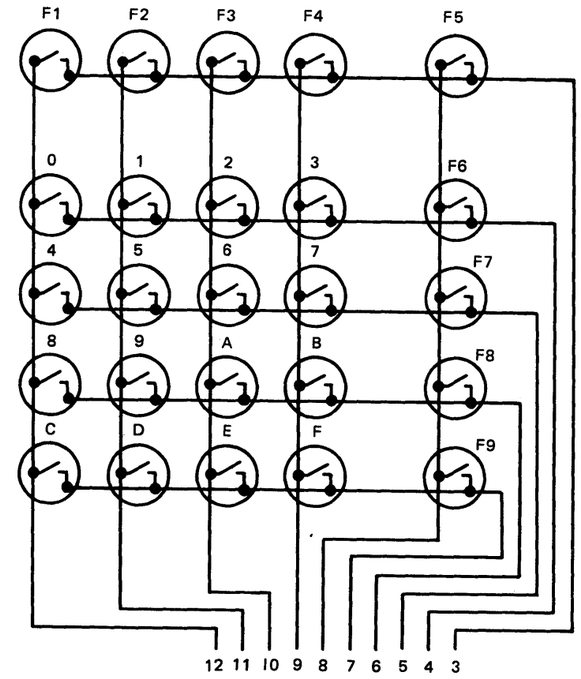



**Figure SP430-1. EFP Keypad Card**

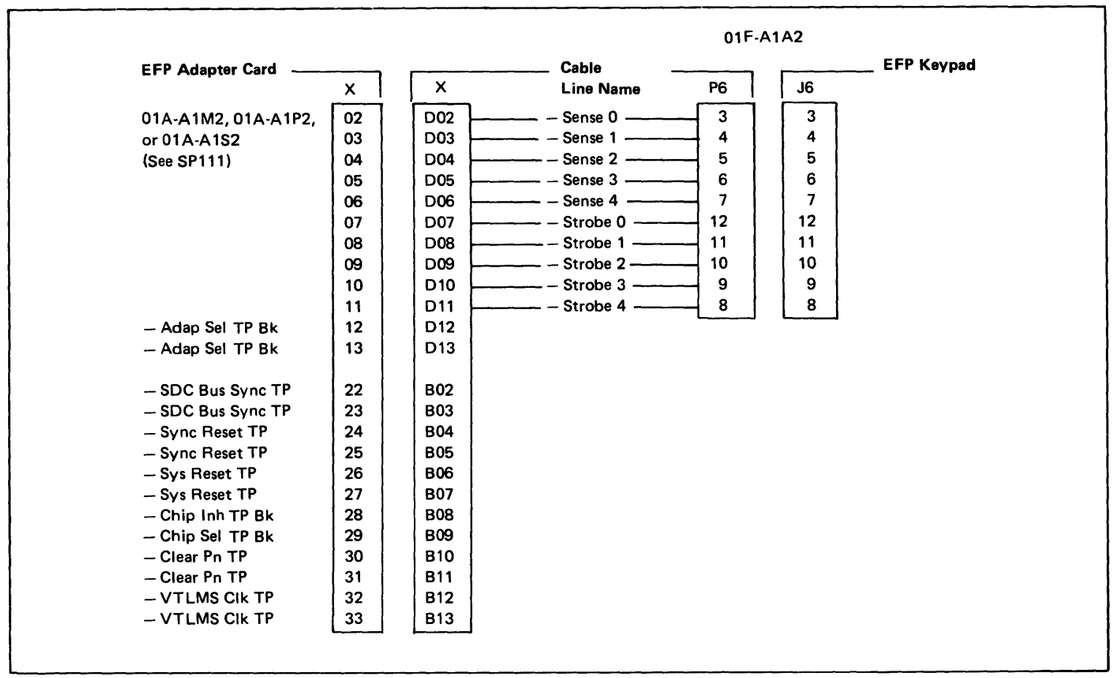



**Figure SP430-2. EFP Adapter Card-to-EFP Keypad Wiring**

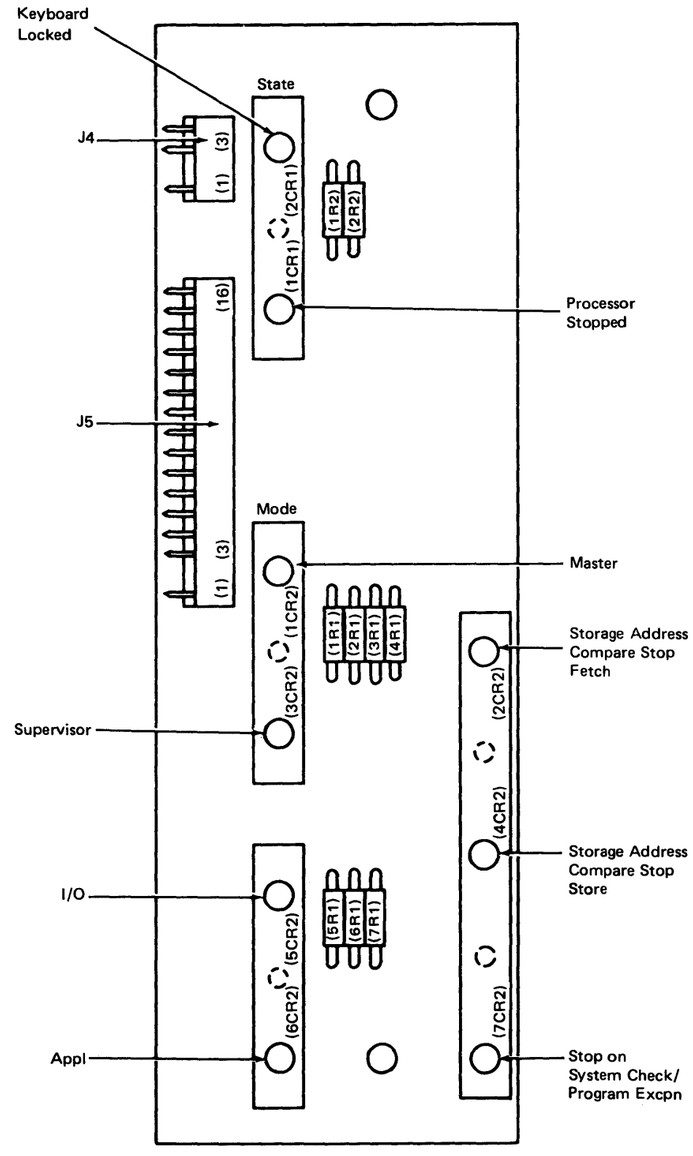



**Figure SP430-3. Mode and State Indicator Card (Front View)**

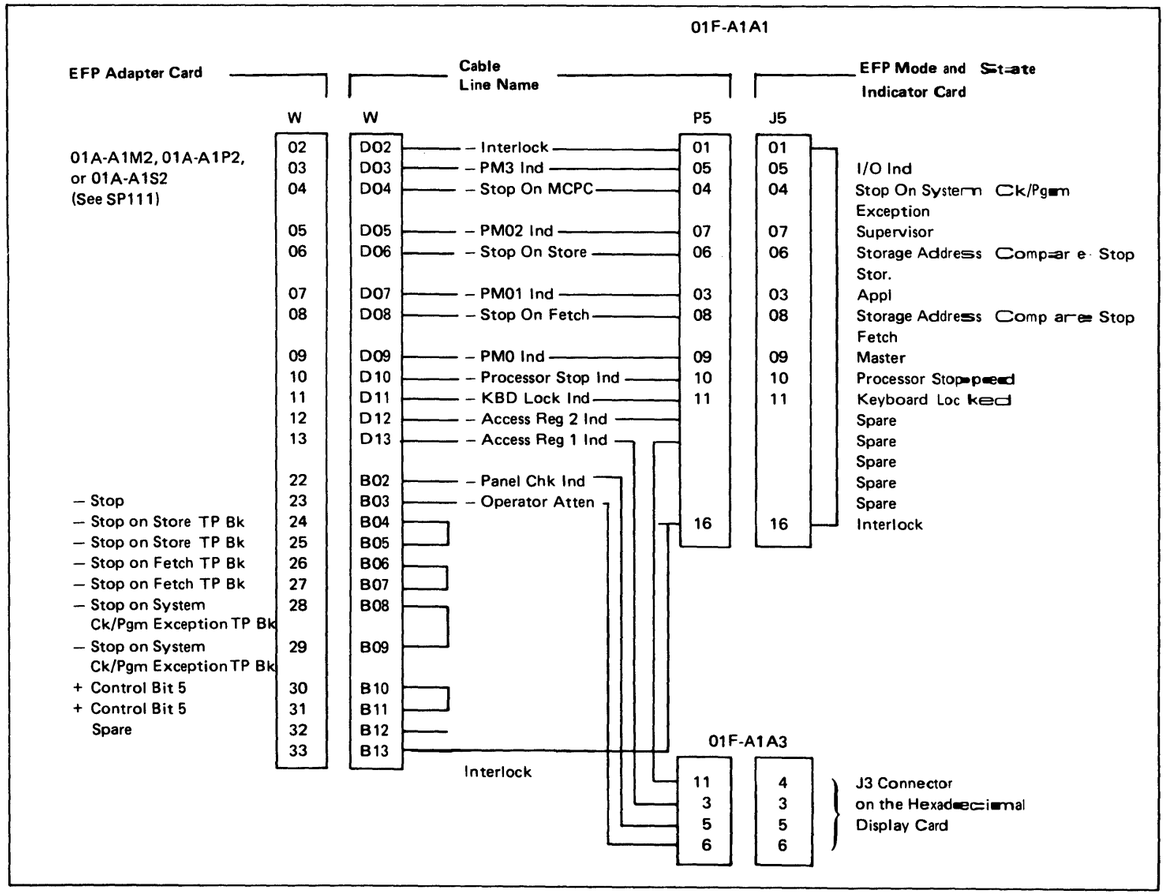



**Figure SP430-4. EFP Adapter Card-to-EFP Mode and State Indicator Card Wiring**

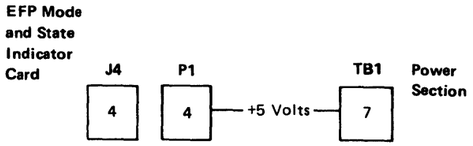



**Figure SP430-5. Mode and State Indicator Card-to-Power Connections**

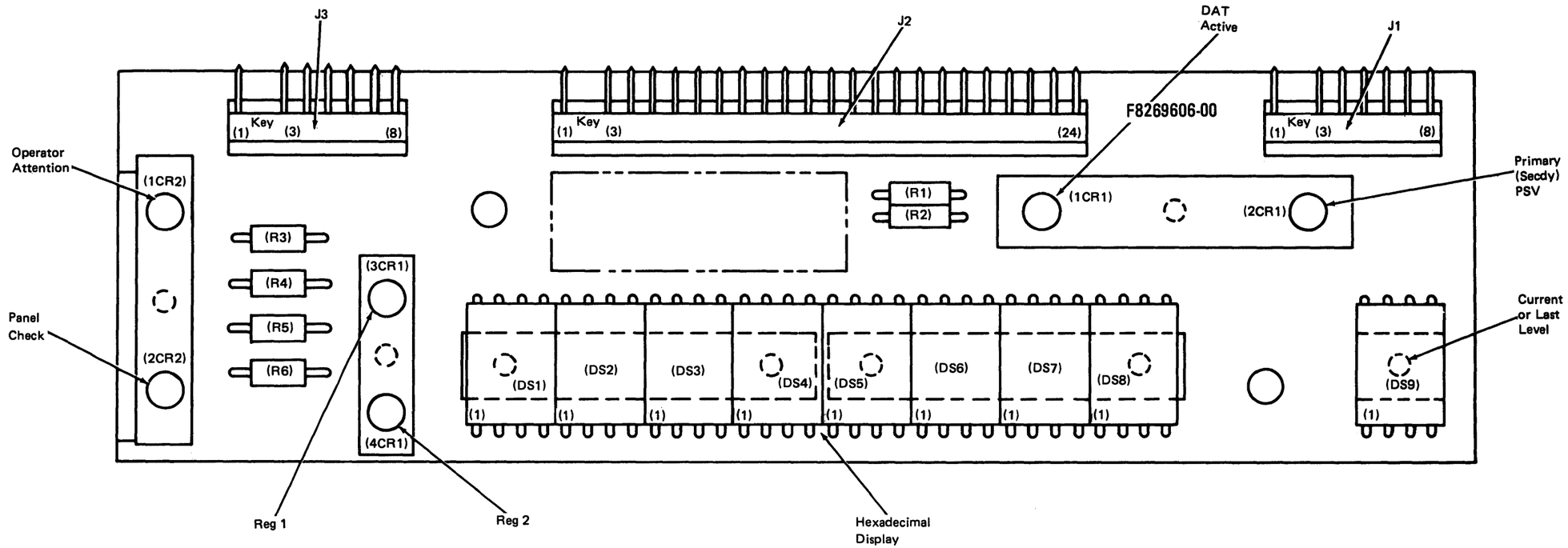



**Figure SP430-6. Hexadecimal Display Card (Front View)**

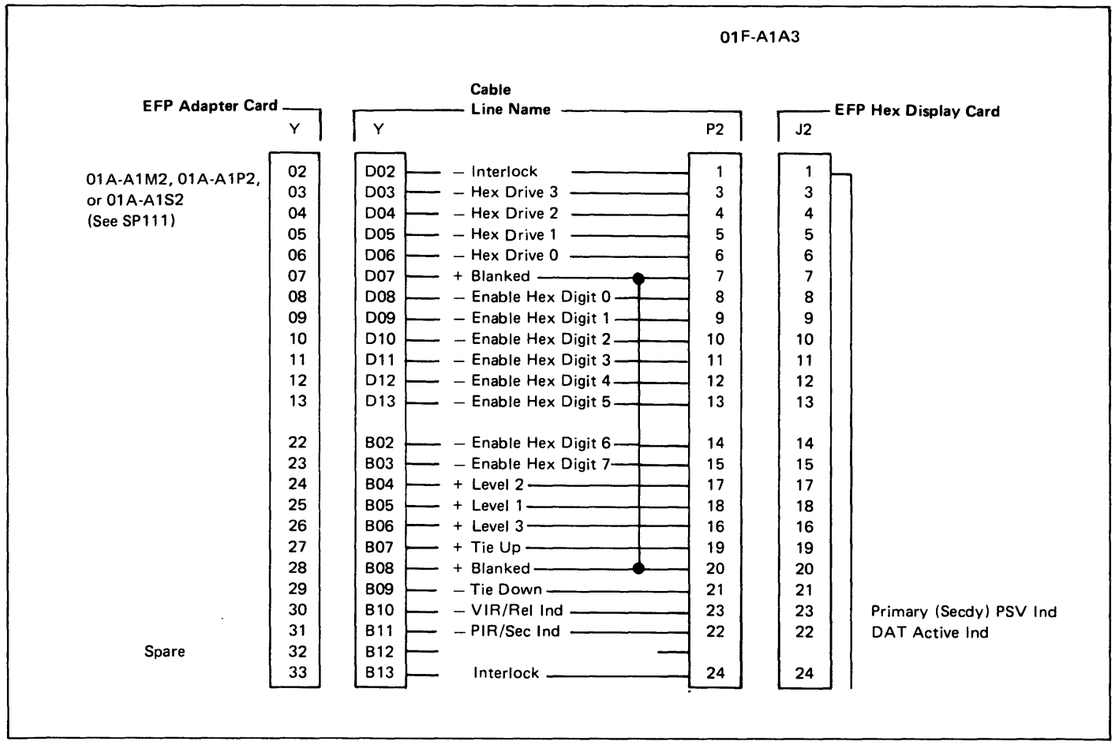



Figure SP430-7. EFP Adapter Card-to-EFP Hex Display Card Wiring

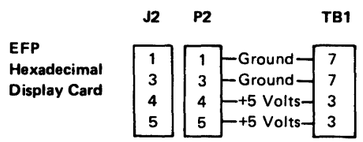



Figure SP430-8. Hex Display Card-to-Power Connections

## SP450 Detailed Data Flow

Figure SP450-1 shows the EFP adapter card detailed data flow and Figure SP450-2 shows the EFP adapter card to BOP adapter card wiring. Refer to SP120 for a brief operational description if necessary.

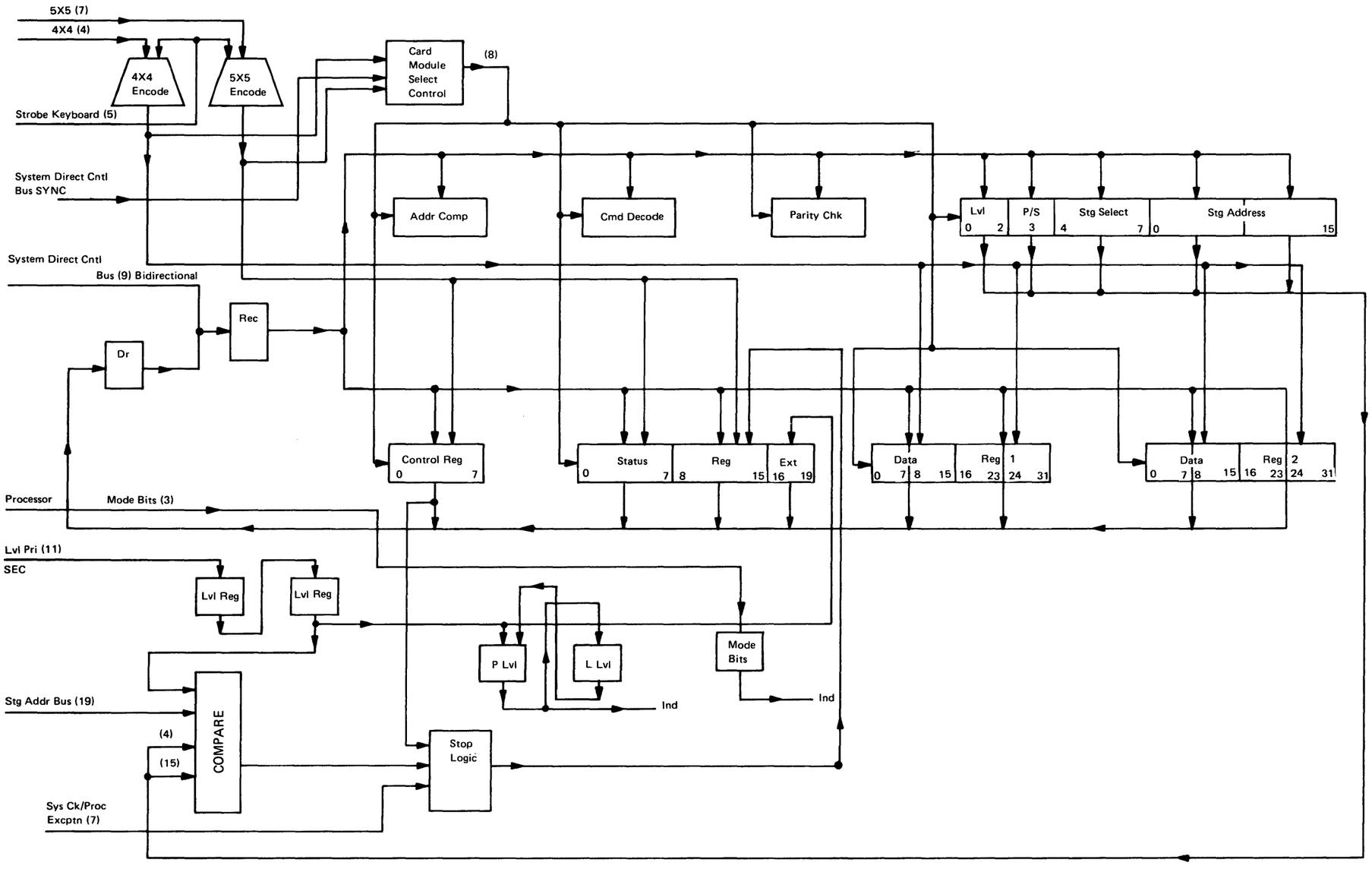



**Figure SP450-1. EFP Adapter Card Data Flow Diagram**

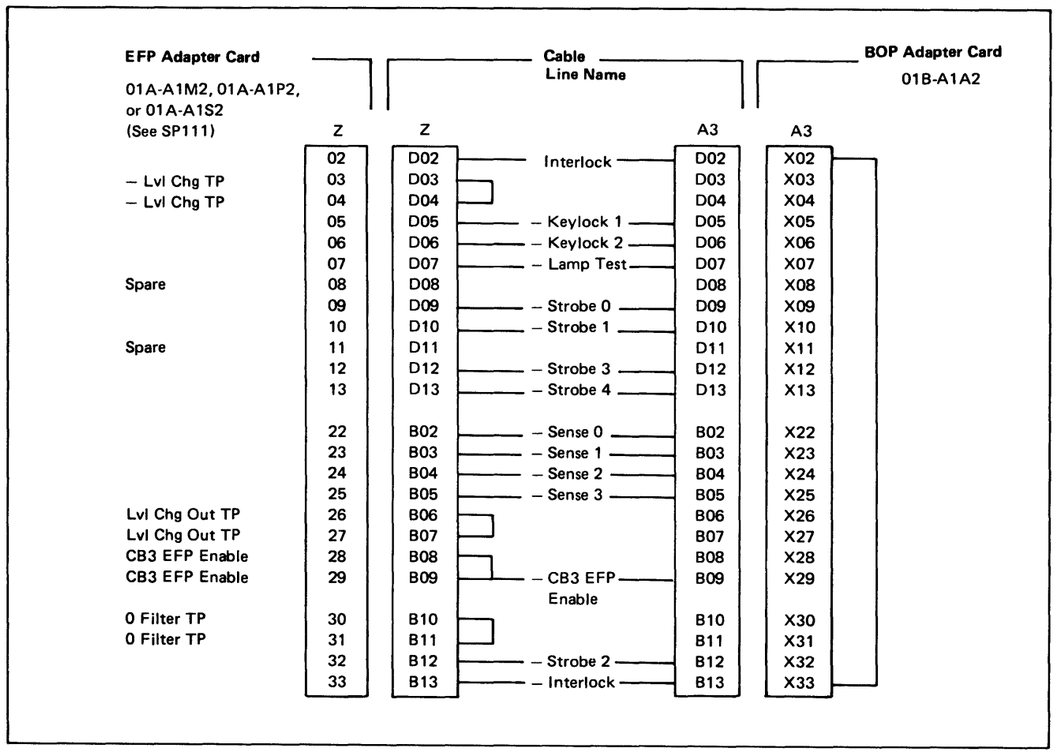



**Figure SP450-2. EFP Adapter Card-to-BOP Adapter Card**

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## SP500 Adjustment, Removal, and Replacement Information

This section describes how to adjust, remove, and install (exchange) EFP components. Refer to Figures SP500-1 through SP500-3, and if necessary, to SP111 for illustrations showing locations.

To replace any operator panel component, you must first gain access to the rear of the panel. Perform the following:

1. Remove 8140 power plug from the wall.

   **Caution: DC voltage is still present at the operator panel with the 8140 power switch in the Off position.**

2. Open the 8140 front covers and remove the BOP/EFP bezel by sliding the two retainer clips to the rear. These are located at the bottom of the bezel. Remove the bezel by lifting it straight up.
3. Pivot the BOP/EFP assembly toward the front of the 8140 to gain access to any of the EFP field-replaceable units.

### SP510 Adapter Card

1. Turn off power to the 8140.
2. Remove card from M2, P2, or S2, depending on the model.
3. Move any card jumpers to the replacement card.
4. Replace card, power up 8140 and run EFP test for verification of correct panel operation.

### SP520 Keypad

To remove the keypad:

1. Unplug cable from J6 connector on keypad FRU.
2. Remove keypad retaining hardware.
3. Remove keypad.

To replace keypad, reverse keypad removal procedure.

### SP530 Hexadecimal Display Card

To remove hexadecimal display card:

1. Unplug J1 and J2 connectors.
2. Remove card retaining hardware.
3. Remove card.

To replace hexadecimal display card, reverse the card removal procedure.

### SP540 Mode and State Indicator Card

To remove mode and state indicator card:

1. Unplug J3, J4, and J5 connectors.
2. Remove card retaining hardware.
3. Remove card.

To replace mode and state indicator card, reverse the card removal procedure.

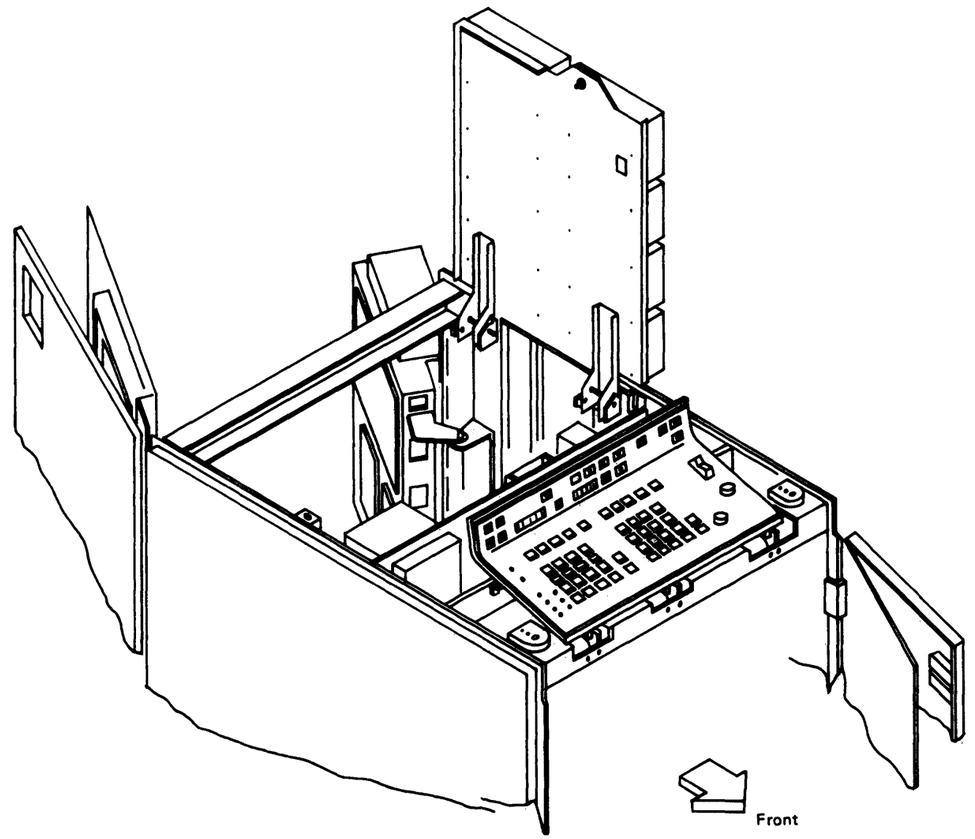


**Figure SP500-1. BOP and EFP Access**

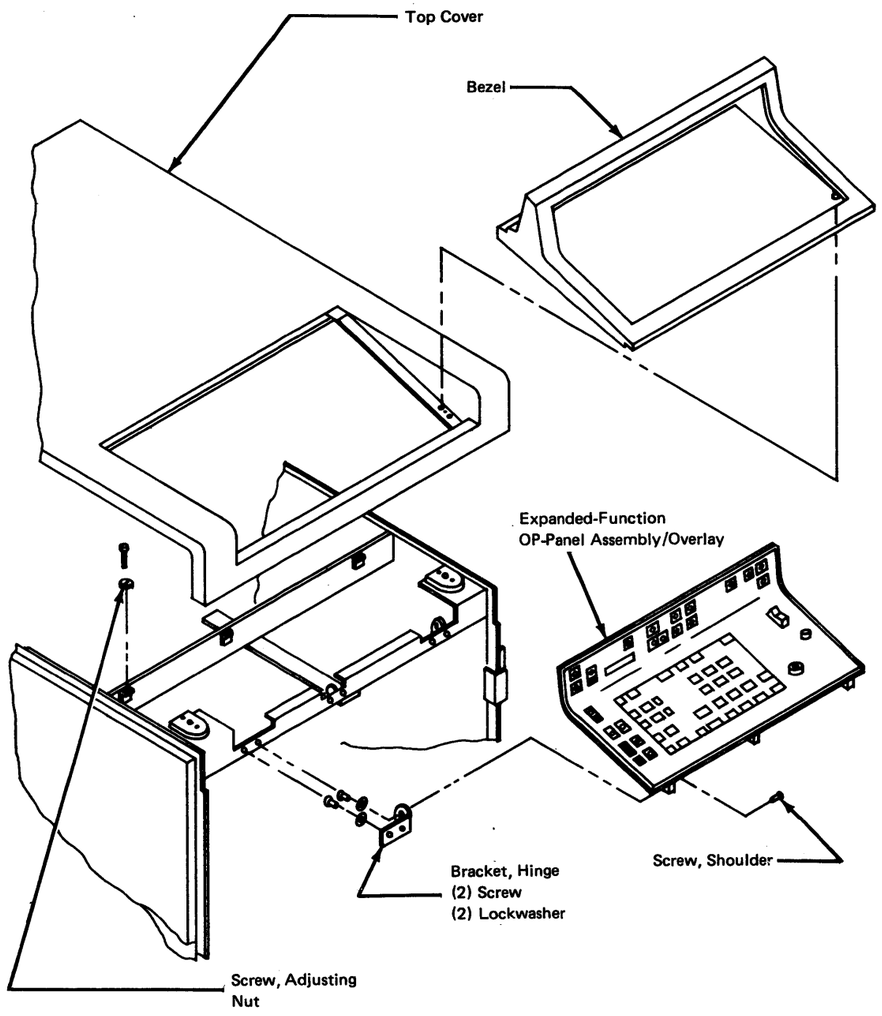


Figure SP500-2. BOP and EFP Frame Mounting

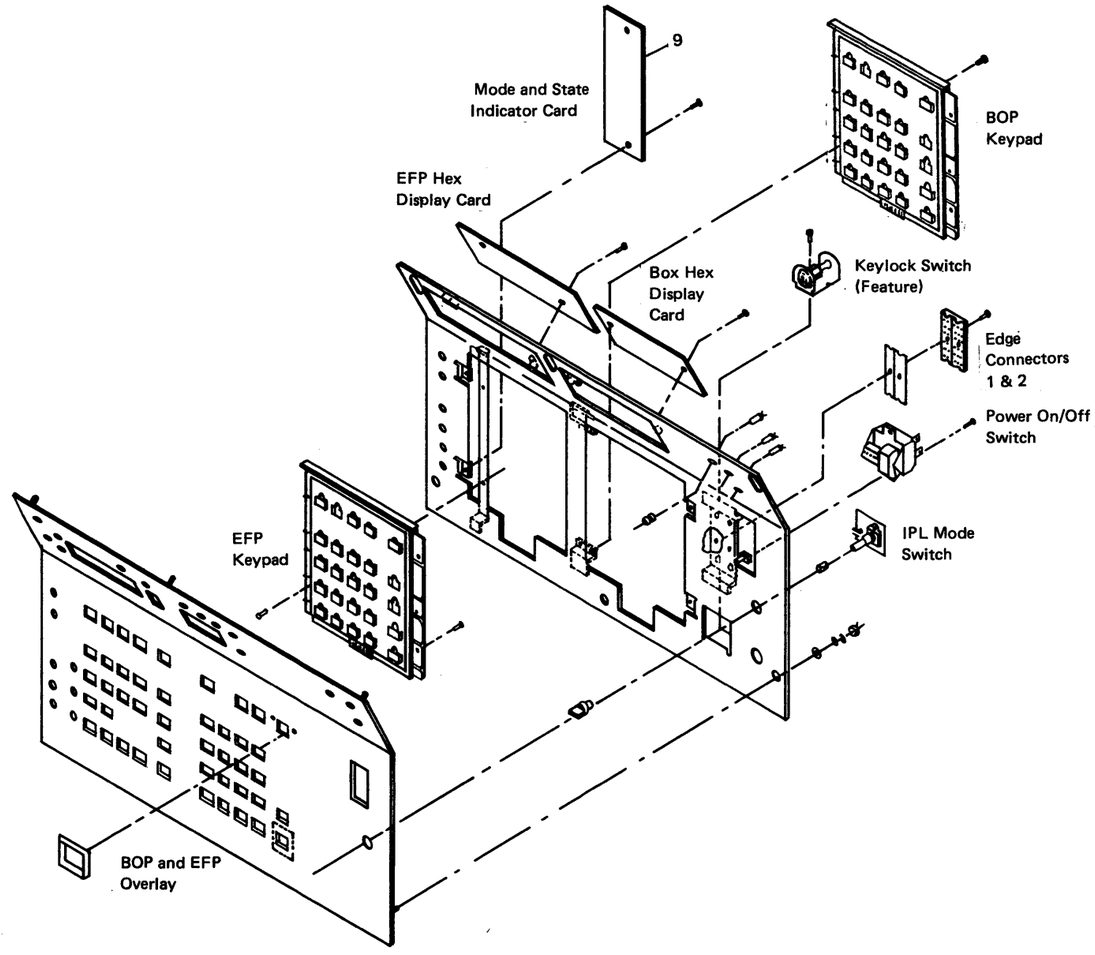


Figure SP500-3. BOP and EFP Component Bezel Mounting

# Chapter 5. MAP Reference Information
# Magnetic Tape Adapter
# (TA)

## Introduction

This part of Chapter 5 provides maintenance information to service the 8809 Magnetic Tape Attachment Feature adapter used for the IBM 8100 Information System. When used with IBM's MAP Maintenance Package, the TA MAP diagnoses tape adapter, problems and refers to this part of Chapter 5 for such information as hardware locations, possible-cause-of-failure lists, and wiring checks.

This part consists of five sections:

1. General Information (TA100–TA133): Contains information on TA components, addressing, operation, and repair strategy.
2. Offline and Online Tests (TA200–TA255): Contains test information and action plans.
3. Intermittent Failure Repair Strategy (TA300–TA353): Contains information to repair intermittent failures.
4. Signal Paths and Detailed Operational Description (TA400–TA453): Contains diagrams and wiring charts which show wiring and signal paths.
5. Console Messages (TA500–TA520): Contains information about the operating system console messages.

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## Abbreviations

| | |
|---|---|
| amp | Amplifier |
| ARC | Adapter Return Code |
| BADDR | Basic Address Register |
| BGERR | Background Error |
| BOP | Basic Operator Panel |
| BOT | Beginning of Tape |
| BSB | Back Space Block |
| BSF | Back Space File |
| CHCV | Channel Control Vector |
| CHCVC | Channel Control Vector Command |
| CHCVD | Channel Control Vector Data |
| CHIO | Channel I/O |
| CIL | Condition/Incident Log |
| ck | Check |
| CLSAR | Control Lines Storage Address Register |
| cmd | Command |
| cnt | Count |
| cntl | Control |
| CNTL-L | Control Lines |
| cntr | Counter |
| conn | Connector |
| DA | Drive address |
| det | Detect |
| DPCX | Distributed Processing Control Executive |
| DPPX | Distributed Processing Programming Executive |
| DRV/RCV | Driver/Receiver |
| DSE | Data Security Erase |
| EADDR | Extended Address Register |
| ELDA | Error Log Data Analysis |
| ELSA | Error Log Summary and Archive |
| env | Envelope |
| EOD | End of Data |
| ERG | Erase Gap |
| ERI | Error Record Indicator |
| FCB | Function Control Block |
| FDM | Function Definition Module |
| FRB | Function Request Block |
| FRU | Field Replaceable Unit |
| FSB | Forward Space Block |
| FSF | Forward Space File |
| fwd | Forward |
| GFI | General Failure Index |
| HW | Halfword |
| IBG | Inter Block Gap |
| IC | Isolation Code |
| ID | Identification |
| I/O | Input/Output |
| IPS | Inches Per Second |
| LA | Logical Address |
| LED | Light-Emitting Diode |
| LO | Low |
| LV | Level |
| LWR | Loop Write to Read |
| MAP | Maintenance Analysis Procedure |
| MCK | Machine Check |
| MD | Maintenance Device |
| MED | Medium |
| MTE | Multi-Track Error |
| PA | Physical Address |
| PEID | Phase Encoded Identification |
| PIO | Programmed I/O |
| PSAR | Processor Storage Address Register |
| REG | Register |
| R/W | Read/Write |
| SAR | Storage Address Register |
| SC | Symptom Code |
| SCF | System Control Facility |
| seg | Segment |
| SHS | Set High Speed |
| SLG | Set Long Gap |
| SLI | Suppress Length Indication |
| SLS | Set Low Speed |
| SSCF | Secondary System Control Facility |
| SYSLERR | System List Error Log |
| SYSLTSD | System List Tape Statistical Data |
| SYSTCM | System Test Control Monitor |
| TACH | Tachometer |
| TARC | Translated Adapter Return Code |
| TIC | Transfer in Channel |
| TM | Tape Mark |
| TSD | Tape Statistical Data |
| TSTCLP | Test Control Line Parity |
| UT | Unit Type |
| WRT | Write |
| WTM | Write Tape Mark |

## TA100 General Information

This section contains information on hardware components, addressing, operation, and adapter-unique repair strategy.

## TA110 Components and Addressing

### *TA111 Hardware Components*

An 8809 tape subsystem has three different configurations which are mutually exclusive. Each may have up to four tape units.

In the first configuration, the two tape adapter cards and a driver/receiver card reside in the 8101. The System Control Facility (SCF) card for the adapter can be shared with either the diskette or disk adapters or both, depending on the 8101 configuration. The first tape unit, always a Model 1A, connects to the 8101. See Figures TA111-1 and TA111-2.

In the second configuration, the two tape adapter cards and a driver/receiver card reside in the 8140 Model Bxx. The System Control Facility (SCF) card for the adapter can be shared with a display printer or communications adapter, depending on the 8140 configuration. The first tape unit, always a Model 1A, connects to the 8140. See Figures TA111-3 and TA111-4.

In the third configuration, which uses an 8809 Model 1B, the adapter cards, as well as the SCF card, reside in the first tape unit. In this configuration, the SCF is not shared, and the tape unit connects to the 8130 or 8140 Processor or the 8101 and must be physically adjacent. See Figures TA111-5 and TA111-6.

For a description of the Model 2 and 3 tape units, see Chapter 4, GR300.

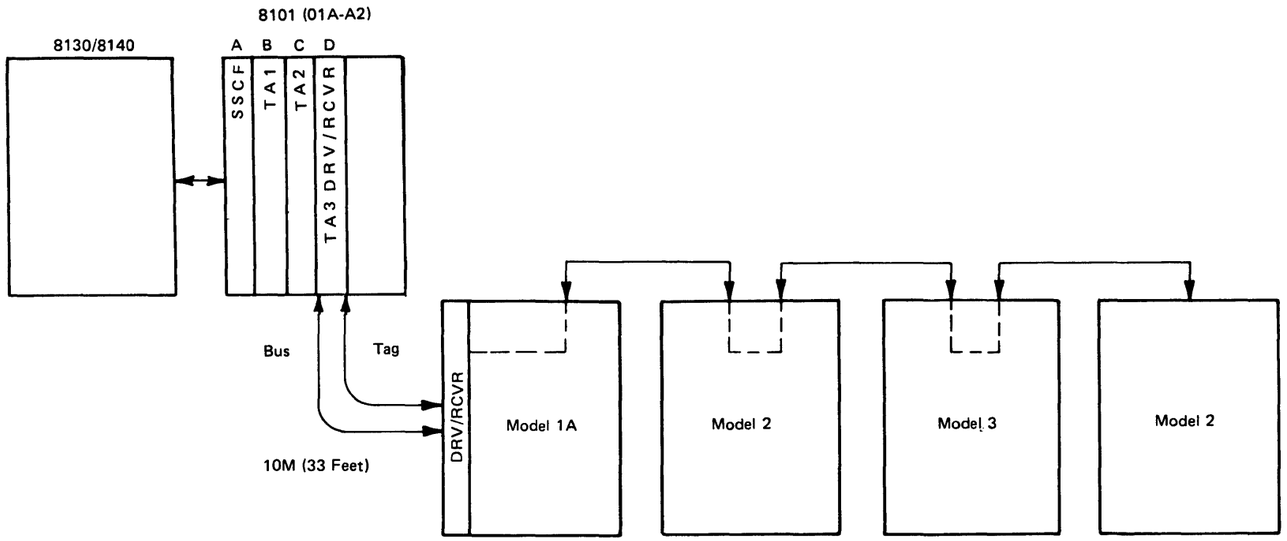
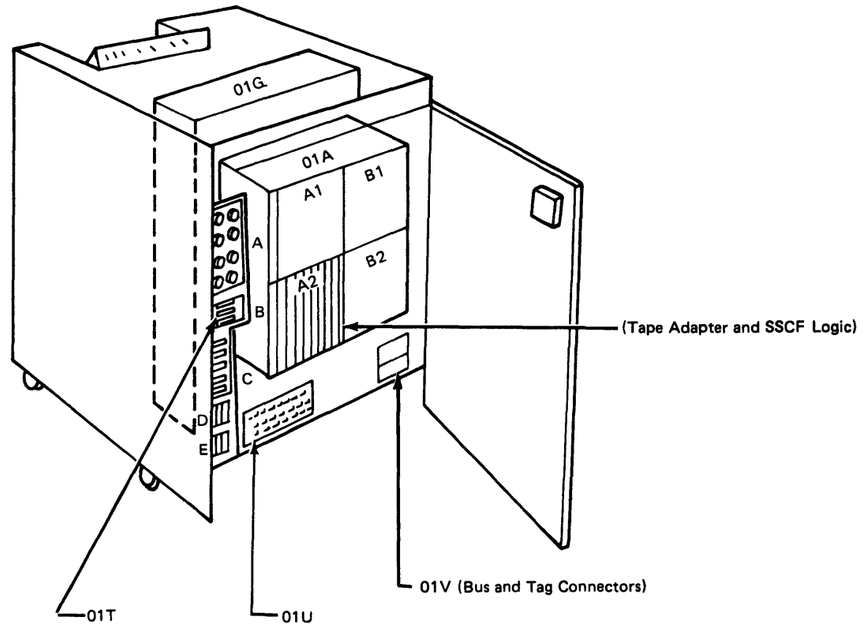



**Figure TA111-1. 8100/8809 Model 1A Tape System (Adapter in 8101)**




8101 Rear View

**Figure TA111-2. 8809 Model 1A Adapter and SCF Card and Cable Locations (Adapter in 8101)**

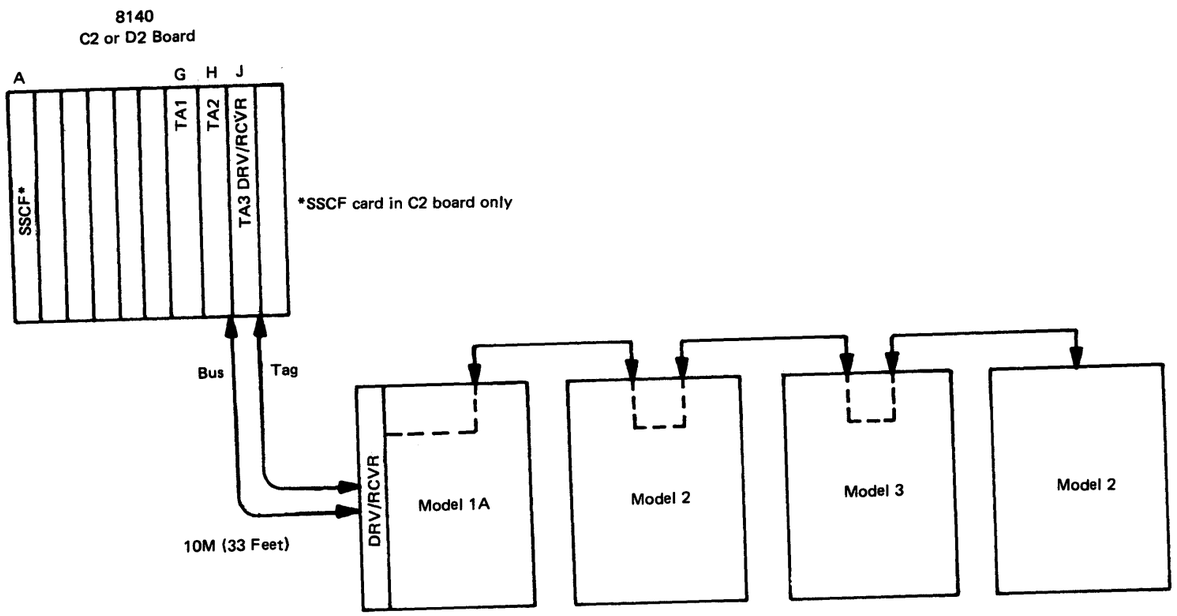



**Figure TA111-3. 8100/8809 Model 1A Tape System (Adapter in 8140)**

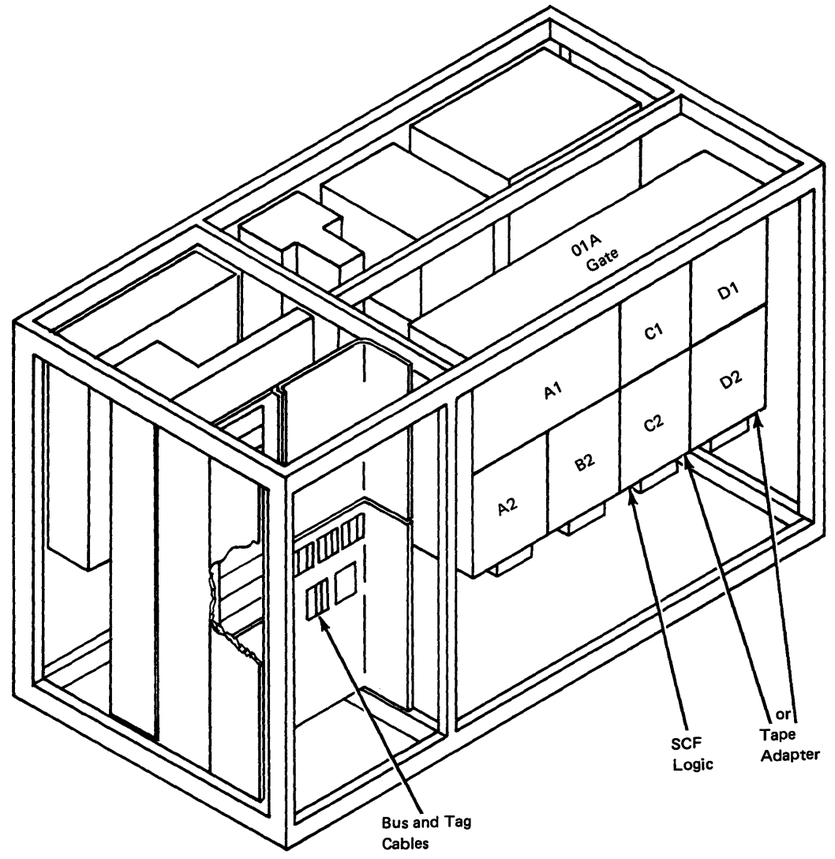



**Figure TA111-4. 8809 Model 1A Adapter and SCF Card Locations (Adapter in 8140)**

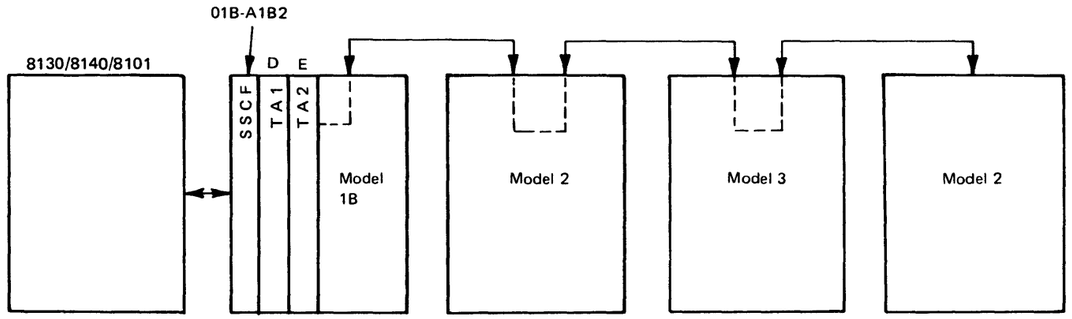



**Figure TA111-5. 8100/8809 Model 1B Tape System**

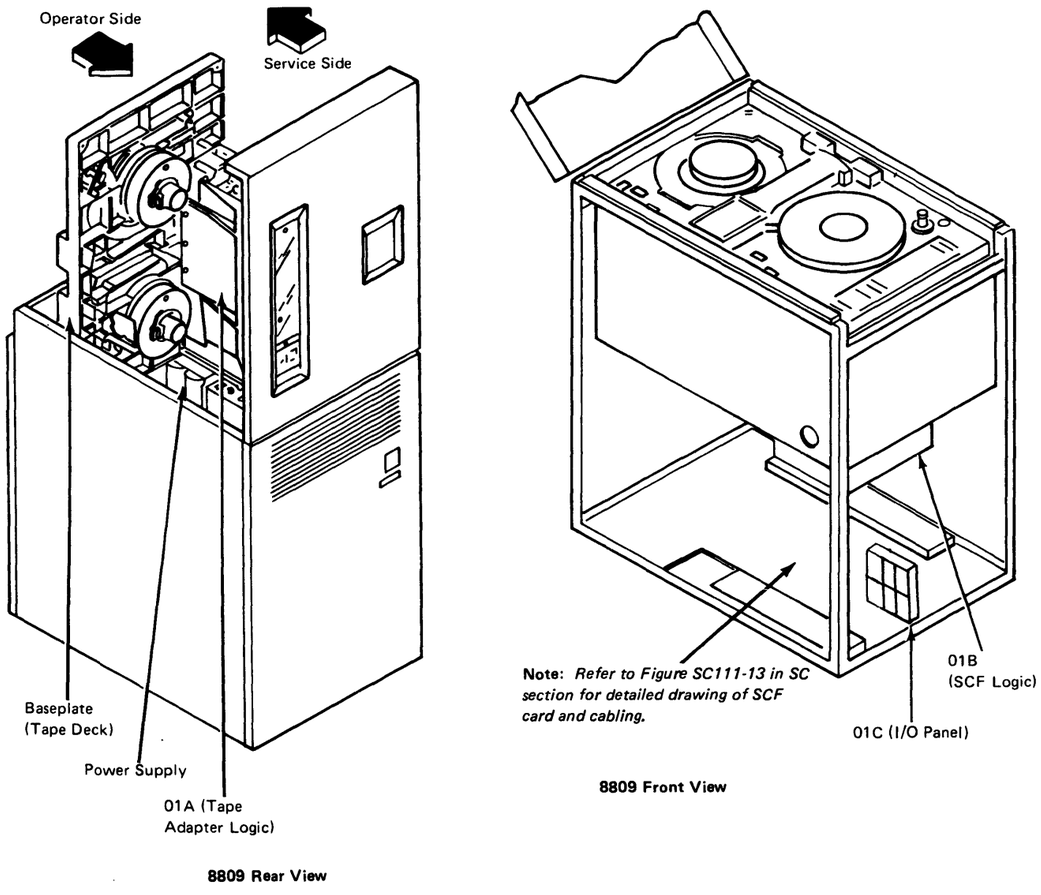



**Figure TA111-6. 8809 Model 1B Adapter and SCF Card and Cable Locations**

*TA112 Addressing*

To specify a particular tape drive for any operation, the adapter physical address (PA) and a drive address (DA) must be used.

The adapter PA consists of two hexadecimal (hex) characters. The first (P) specifies the SSCF Group address and is determined by the SSCF card address switch settings. The second (A) specifies the tape adapter address within the SSCF group address. Refer to Chapter 2, CP200, for a discussion of addressing. The DA also consists of two hex characters and is determined by switch settings on a tape drive card.

*TA113 Configuration Table Entry*

This configuration table entry example aids in understanding how to specify a particular tape drive for testing. When running tests and the prompt message 'Enter PADA' displays, you must specify both a level 01 and a level 02 (adapter and drive) address. For example, 9301 selects drive address 01 that is connected to the first 8101.

The following shows a maximum tape configuration entry. Be aware that only one level 01 PA entry can exist in the configuration table

**SSCF Group and Tape Adapter Addresses (PA)**

| LV | PA | UTUT | OPOP | OPOP | Comments |
|---|---|---|---|---|---|
| 01 | 5E | 0040 | 0000 | 0000 | 8140 Model Bxx |
| 01 | 73 | 0040 | 0000 | 0000 | 8809 Model 1B |
| 01 | 93 | 0040 | 0000 | 0000 | First 8101 |
| 01 | A3 | 0040 | 0000 | 0000 | Second 8101 |
| 01 | B3 | 0040 | 0000 | 0000 | Third 8101 |
| 01 | C3 | 0040 | 0000 | 0000 | Fourth 8101 |

**Tape Drive Addresses (DA)**

| LV | DA | UTUT | OPOP | OPOP |
|---|---|---|---|---|
| 02 | 00 | 0040 | 0000 | 0000 |
| 02 | 01 | 0040 | 0000 | 0000 |
| 02 | 02 | 0040 | 0000 | 0000 |
| 02 | 03 | 0040 | 0000 | 0000 |
| 02 | 04 | 0040 | 0000 | 0000 |
| 02 | 05 | 0040 | 0000 | 0000 |
| 02 | 06 | 0040 | 0000 | 0000 |
| 02 | 07 | 0040 | 0000 | 0000 |

## TA120 Basic Operational Description

The tape adapter consists of two adapter cards (TA1 and TA2) plus one driver/receiver card (Model 1A Tape System only). The adapter controls the operation of from 1 to 4 tape drives, depending upon the customer configuration. Figures TA120-1, TA120-2, and TA120-3 show the general layout and data flow of the adapter. Refer to the TA400 section for detailed information.

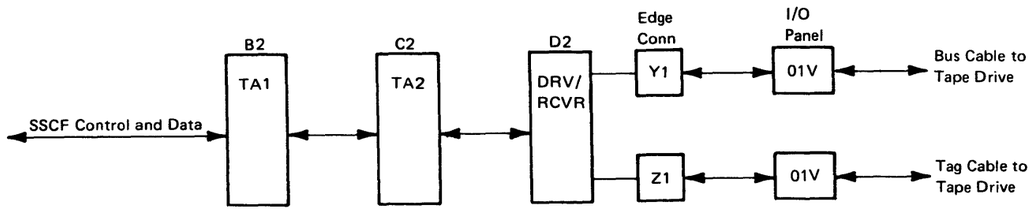



**Figure TA120-1. 8809 Model 1A Tape System Basic Data Flow (Adapter in 8101)**

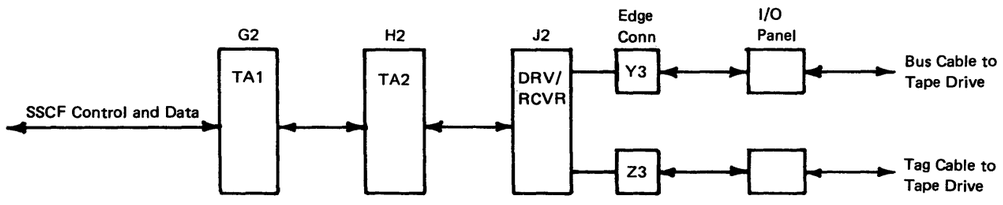



**Figure TA120-2. 8809 Model 1A Tape System Basic Data Flow (Adapter in 8140 Model Bxx)**

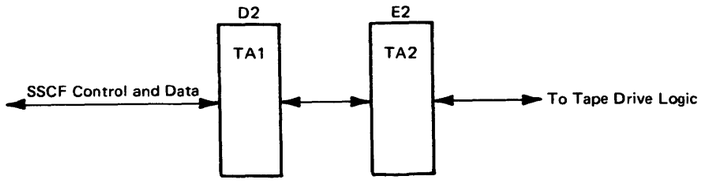



**Figure TA120-3. 8809 Model 1B Tape System Basic Data Flow (Adapter in 8809)**

## *TA121 8809 Adapter to Tape Drive Basic Operations*

Several basic types of operations use commands betwen the adapter and the attached tape drives. The following briefly describes these operations:

- Write—directs the adapter to transfer 'X' bytes of data from processor storage to the tape drive. The tape drive moves forward towards the end of tape (EOT) marker, while writing the data from processor storage to the tape.
- Read—directs the adapter to transfer 'X' bytes of data from the tape drive to processor storage. The tape drive moves tape forward towards the EOT marker, assembling the data from tape and passing it to the adapter, where it can then transfer to processor storage.
- Forward Space Block—moves tape forward towards the EOT marker to the next interblock gap (IBG). No data transfer or error detection occurs using the information contained within that block.
- Back Space Block—moves the tape backward towards the beginning of tape (BOT) marker either to the next interblock gap or to the load point, whichever comes first. No data transfer or error detection occurs using the information contained within that block.
- Forward Space File—moves tape towards the EOT marker to the interblock gap beyond the next tape mark. No data transfer or error detection occurs using the information contained within that file.
- Backspace File—moves tape towards the BOT marker either to the interblock gap beyond the next tape mark or to load point, whichever comes first. No data transfer or error detection occurs using the information contained within that file.
- Write Tape Mark—writes a tape mark (a block of significant non-data bytes separating files), and does not require processor information transfer.
- Data Security Erase—erases tape information from the present position of the tape to one meter beyond the EOT marker.
- Erase Gap—moves the tape forward towards the EOT marker, and erases approximately 8.75 cm (3.5 inches) of information.
- Rewind—rewinds the tape, which remains loaded when the tape reaches load point.
- Rewind/Unload—rewinds the tape to load point and unloads the tape. If already at load point, the tape immediately unloads.
- Mode Set—sets the speed and the IBG length.

## TA130 Adapter-Unique Repair Strategy

This section describes that repair strategy unique to the 8809 Magnetic Tape adapter. Refer to Chapter 4, GR500, for general 8100 Information System repair strategy.

The General Failure Index (GFI) initially determines whether the tape drive or the adapter caused a problem. Before entering the 8809/8100 maintenance package, ensure that the 8100 operates properly. Use the TA MAP contained on MD diskette 03 to determine the cause of the failure. When the MAPs instruct you to run a test and detects a failure, the MAP then generates an Isolation Code (IC). The IC then points to a MAP to provide further direction.

### *TA131 Offline Checkout*

To perform the adapter offline checkout, obtain the 8100 from the customer. Use maintenance device diskette 03 and specify the offline basic checkout option selection 'A' from the TA MAP menu. Run the offline tests to isolate the problem to the adapter, the tape drive, or to the unit's Secondary System Control Facility (SSCF).

If the problem is isolated to the adapter, the TA MAP directs you to replace the FRU(s) causing the problem. If the problem is not corrected, you are referred to TA250 (Failure Action Plans) for further corrective action.

If the problem is isolated to the tape drive, the TA MAP refers you to the 8809 Tape Drive MAPs for further corrective action.

If the problem is isolated to SSCF, the TA MAP refers you to the system control facility MAP (SC) for further corrective action.

### *TA132 DPCX Online Exerciser*

With DPCX, you can check the adapter and drive(s) online by using the DPCX Online Exerciser, which tests operations that a customer might normally execute. If a failure occurs, the program collects and analyzes the error data, and then generates a Symptom Code (SC) to identify the failing area or FRU. The SC points to a MAP which then provides further direction.

### *TA133 Intermittent Failures*

An intermittent failure can occur so infrequently that looping the test might not detect it. You should then use the system error log. See TA330 and TA340 for detailed information on the error log.

An error can also occur at random times and generate different test error messages, which makes the MAPs ineffective. After the MAPs detect three different test error messages, you are instructed to use the action plans in TA250.

If errors occur only after looping the tests for more than 15 minutes, record the test error message and use the free-lance looping operation (TA313) and the action plans in TA250.

See TA300 for detailed information on intermittent failures.

## TA200 Offline and Online Tests

To test and repair the adapter and attached tape drive(s), IBM provides offline tests and a DPCX online exerciser.

The offline tests reside on MD diskette 03. The DPCX online exerciser is provided only for those systems using DPCX, and is part of the program.

The offline tests detect and report failures between the System Control Facility (SCF) and the tape adapter, in the adapter, between the tape adapter and the tape unit, and in the tape unit under test.

The DPCX online exerciser contains routines to isolate data transfer problems from tape motion problems, and to functionally exercise the tape unit.

## TA210 Offline Test Routine Descriptions

The offline test, which consists of 48 routines on MD diskette 03, is divided into three parts: adapter routines, device routines, and special requirement tests. The maintenance device runs and controls offline test operation, which requires dedication of the entire 8100.

The adapter tests complete in 15 seconds, while the device tests take 5.5 minutes. For the run times of the special requirement tests, see the individual routine descriptions in TA213.

### *TA211 Adapter Tests*

The 14 adapter routines test the adapter hardware, I/O commands, and the SCF signal bus path from the SSCF to the tape adapter. The MD invokes the adapter routines either by the MAP or by a free-lance operation. See TA241 for error descriptions.

When using the MAP, the tests are invoked automatically when required. When using the free-lance operation, the following test invocation procedure must be used:

1. At 80BC or PA00, enter PADAB.
2. At 81BC, enter SLRRB

   Where:

   PA = adapter address (see TA113)
   DA = address of the drive to be tested (see TA113)
   S = sense option:
   - 0 = run only adapter tests, routine 01–15
   - 1 = run adapter/device tests, routines 01–56
   - 2 = run adapter/device tests with manual intervention routines 01–56

   L = loop option:
   - 0 = run selected routines one time
   - 1 = loop selected routines; stop on error
   - 2 = loop selected routines; bypass error

   RR = routine number. If 00 or no entry is made, all routines for sense option are run. If a routine number is entered, only that routine is run.
   B = begins execution and enters the invocation message.

Successful completion of the adapter tests (PA00) occurs in 15 seconds. A short description of each routine follows:

**Routine 01, Address Recognition Test.** Determines if the adapter under test recognizes its own address by issuing an Adapter Reset command. A machine check or an I/O interruption should not occur.

**Routine 02, Command Test.** Determines if the adapter under test responds to all valid commands and causes a machine check for all invalid commands. All bit patterns from hex 00 to hex FF are issued as commands.

**Routine 03, Adapter Register Test.** This routine tests: (1) whether all bit combinations can be written into each adapter register, and (2) whether all adapter registers are reset by the Reset Adapter command. Except for the status register, this routine checks all registers by writing all patterns to each register. It then reads them back while comparing the values to the write mask values. Each register is reset and checked for zero.

**Routine 04, Basic and Extended Status Register Set/Reset and Interrupt Test.** Tests that the basic and extended status registers: (1) can be written correctly, (2) can be reset selectively, and (3) have certain bit settings that cause generation of interruptions. Five tests are performed:

1. Reset the status registers.
2. Write hex FF to the status registers and test that selective bits are reset.
3. Check extended status for setting and reading all bit combinations,
4. Check that the extended bits set the interrupt bit.
5. Check basic status for setting and reading all bit combinations.

**Routine 05, Timer Test.** Tests the timer to ensure that an interruption: (1) occurs, (2) occurs only once, and (3) occurs within 800 to 1500 ms.

**Routine 06, Counter Test.** Checks that the Increment and Decrement commands cause the appropriate counters to increment or decrement correctly, and ensures that the adapter storage address counters wrap correctly. The counters are first set to a beginning value of either 1's or 0's, depending on whether the counter increments or decrements. The counters are then stepped through their complete range while being checked for the correct value at each step. They are also checked to ensure that only the correct command loads each counter.

**Routine 07, Buffer Test.** Checks that the alternate buffers can be written and read correctly, and that the processor storage address register (PSAR) counter steps during these Read/Write Buffer commands.

Five data patterns and their complements are used to test every buffer address:

| Pattern | Even Address | Odd Address |
|---|---|---|
| 1 | FF00 | 00FF |
| 2 | 00FF | FF00 |
| 3 | AA55 | 55AA |
| 4 | 55AA | AA55 |
| *5 | 0101 | F7F7 |

*Used for parity checking.

The routine writes every address by using a write loop, then reads and checks them by using a read and compare loop. The routine also checks the wrapping of the processor storage address register by using a loop count of 257 for 256 addresses.

**Routine 08, Wrap Test.** Tests that the Wrap command: (1) increments the control line storage address register (CLSAR) and (2) wraps data through the buffer with no errors.

The routine first issues a Reset Adapter command to set the processor storage address register (PSAR) and CLSAR to zero, and writes a halfword of hex FF00 into the first buffer address. The routine then issues a Wrap command and a Read Buffer command. The first address should now contain hex FFFF, and the CLSAR should increment.

The routine completes successfully when the hex FFFF pattern ripples through all buffer positions by using the Wrap command. The routine checks every step to ensure that it completed correctly and that no parity errors occurred.

**Routine 09, Function Control Block (FCB) Test.** Checks the FCB fetch operation by using no-op FCB values. It executes an FCB list containing five no-op FCBs and an end-op FCB, and then checks the channel pointer register for correct ending status and value.

**Routine 11, Command Transfer In Channel (TIC) Test.** Checks command TIC operation by using no-op FCB values. It executes an FCB list containing a no-op, TIC, and end-op, and then checks the channel pointer register for the correct command value.

**Routine 12, Program-Requested Interrupt (PRI) Test.** Checks program-requested interrupt operation in FCB mode by using no-op FCB values with the PRI bit on. It executes an FCB list containing a no-op (with the PRI bit on) and an end-op, and then checks status to ensure that the PRI and interrupt bits are on.

**Routine 13, Invalid Subcommand Test (FCB Mode).** Checks invalid subcommand detection in FCB mode. It executes four invalid FCBs, each one of which should set interrupt and invalid subcommand status.

**Routine 14, Parity Check Test.** Checks the parity status bit by wrapping a bad parity byte with the Test Control Line Parity (TSTCLP) command. The command is the same as the Wrap command, except that parity is inverted, which causes a parity error.

**Routine 15, Control Lines Sequence Error Test.** Checks that a control line sequence error occurs when issuing a command to a nonselected tape unit. It first issues a Stop command before selecting the drive, which should turn on the control line sequence error status bit.

### *TA212 Tape Drive Tests*

The 20 tape unit routines test for correct adapter-to-tape unit information transfer, as well as correct operation of the selected tape unit, and complete in 5.5 minutes. Refer to TA211 for the test invocation procedure when using free-lance mode.

These routines also use a background error (BGERR) function, which checks for errors on operations that have been tested by a previous routine. It is used to aid in resolving intermittent errors by giving the correct error indication for failures that occurred in previously tested hardware. The BGERR error numbers are F0, F1, F2, F7, F8, and F9. See TA242 for a description of these error numbers.

The DIAG section of the 8809 Maintenance Manual contains a detailed description of the tape drive tests. The following briefly describes each routine:

**Routine 40, Control Line Test.** Exercises the control lines into the tape unit. It first executes an adapter reset and checks status to verify that no inbound lines to the status register are active. It then selects a drive and checks status to verify that correct selection occurred and that the drive responded with the correct address on Bus In.

**Routine 41, Select Active Test.** Tests the ability of the adapter to get a control line sequence error when selecting a tape unit that was previously selected. The routine first selects the drive, which should operate correctly. It then reselects the drive, which should cause a control line sequence error because Select Active was still on.

**Routine 42, Sense Byte Test.** Verifies: (1) the operation of the Sense command and (2) that certain sense bytes contain the proper information after a Check Reset command.

**Routine 43, Loop Write-to-Read Test.** Tests the data transfer circuits by transferring data patterns, which vary in length and content, through the write and read path. This routine is the first one to check the data TIC function of the adapter.

**Routine 44, Poll Test.** Tests that the tape unit can both suppress response and correctly respond to a poll tag.

**Routine 46, Low-Speed Test.** Ensures that various functions can be performed in low speed mode.

**Routine 47, Write/Read Phase Encoded Identification (PEID) Test.** Writes a PEID and then performs a read back check.

**Routine 48, 31.75 Centimeter/sec (12.5 ips) Write/Read Test.** Writes stress data patterns that vary in length, and then performs a read back check.

**Routine 49, Dual Gap Test.** Checks that the Set Long Gap and Set Short Gap commands function correctly.

**Routine 4A. Backward Creep Test.** Ensures that a Backspace and Write command sequence does not destroy data in the record previous to the one being rewritten.

**Routine 4C, High-Speed Test.** Ensures that various functions can be performed in high-speed mode.

**Routine 4D, Repositioning Test.** Ensures that the hardware repositions the tape to the proper location when the Reinstruct command occurs too late. Only the 254 centimeter/second (100 ips) tape mode uses this routine.

**Routine 4E, Write Tape Mark Test.** Writes a tape mark (TM) and then performs a read back check. The tape is backspaced and then spaced forward over the tape mark to determine that the TM can be written and read correctly.

**Routine 4F, Basic Write/Read High-Speed Test.** Writes variable-length stress data pattern records, and then performs a read-back check with the tape unit in the 254 centimeter/second (100 ips) mode of operation.

**Routine 50, Incorrect Length Detection and Suppression Test.** Tests that the adapter can recognize an incorrect length record by reading both long and short. It also tests the suppress length indicator bit by reading long and short. No length error should occur with the suppress length indicator bit on.

**Routine 52, Erase Gap (ERG) Test.** Writes several 4K byte records, rewinds the tape, and executes erase gap operations to erase the records. It then reads the records to ensure that they were erased.

**Routine 53, Write High-Speed, Read Low-Speed Test.** Writes stress data patterns at 254 centimeters/second (100 ips) and then reads them at 31.75 centimeters/second (12.5 ips).

**Routine 54, Read High-Speed Test.** Uses high-speed mode to read the tape that was written by Routine 53. Status and data compare operations are used to verify correct operation.

**Routine 55, Magnetized Head Test.** Writes a 2K byte record, moves the record over the head assembly 10 times, and then reads the record. This sequence is repeated twice. If the last read operation is successful, the write head is considered to be properly demagnetized.

**Routine 56, Data Security Erase Test.** Tests the Data Security Erase command.

### *TA213 Special Requirement Tests*

These 14 tests are selectable and can only be invoked in free-lance mode. You use these tests to perform skew adjustment, verify the read operation, display the sense bytes, check read/write reliability-interchange, and to complete the functional testing of the read path.

These routines use the background error (BGERR) function. Refer to TA212 for a brief description of BGERR, and to TA211 for test invocation procedures. See TA243 for error descriptions.

The DIAG section of the 8809 Maintenance Manual contains a detailed description of the tape drive tests. The following briefly describes each routine:

**Routine 5A, Read Test Pattern Tape (Part 1).** Reads a previously written test tape to check read functions and error-checking circuits, and runs in approximately two minutes.

**Routine 5B, Read Test Pattern Tape (Part 2).** Reads a previously written test tape and compares the expected data with the data read. It also tests the Write command on a file-protected tape, and runs in approximately 5 minutes.

**Routine 60, Write Reliability-Interchange Test.** Tests the write operation by writing interchange test tapes, and runs in 35 seconds.

**Routine 61, Read Reliability-Interchange Test.** Reads tape written by Routine 60 and runs in 50 seconds.

**Routine 62, Tape Control Line Exerciser.** Exercises the control lines, and runs in 10 seconds.

**Routine 63, Load/Rewind/Ready Problem Analysis.** Performs an analysis of load, rewind, and ready problems, and runs in 10 seconds.

**Routine 64, Reinstruct Timing Test-Short Gap.** Checks Reinstruct command timing in short gap mode, and runs in approximately 5 minutes when using a 2400-foot reel.

**Routine 65, Reinstruct Timing Test-Long Gap.** Checks Reinstruct command timing in long gap mode, and runs in approximately 5 minutes when using a 2400-foot reel.

**Routine 66, Read Continuous High-Speed Test.** Reads continuously in high-speed mode, and runs in approximately 5 minutes when using a 2400-foot reel.

**Routine 67, Inter-Block Gap IBG Measurement Test.** Ensures that correct length gaps are written, and runs in 90 seconds.

**Routine 6A, Skew Adjustment Exerciser.** Exercises the tape while you perform mechanical skew adjustments. The routine takes 5 minutes when using a 2400-foot reel, and cannot be looped.

**Routine 6B, Sense Byte Display Utility.** Displays sense information from the most recent test error, and runs in 10 seconds.

**Routine 6C, Symptom Code (SC) Generator Utility.** Generates the symptom code for the most recent test error, and runs in 10 minutes.

**Routine 6D, 'P' Track Only (PTO) Exerciser.** Writes and reads a 4096-byte record of hex 00 by using a loop function to perform 40,000 operations. The run time is 3 1/2 hours.

**Note:** *The tape does not move when running routine 6D.*

## TA220 DPCX Online Exerciser

The DPCX online exerciser runs under the SYSTCM utility and uses the normal invocation procedure.

**Note:** *Only the tape unit under test must be dedicated.*

Normal error logging, as well as any program error recovery procedures, are suppressed for the tested unit, but all other tape units operate normally.

The online exerciser uses two routines (01 and 02) that test tape-unit operations under normal conditions. These routines, described briefly below, might not determine highly intermittent problems:

**Routine 01, Data Path and Tape Motion Test.** Isolates data transfer problems from tape motion problems. It uses the loop write-read and erase gap functions, and runs in 15 seconds.

**Routine 02, Functional Test Exerciser.** Performs a functional verification of each start I/O operation, such as write, read, forward space block, and rewind, and runs in 70 seconds.

When detecting an error, the exerciser presents the 16 tape unit sense bytes, the two adapter status bytes, the symptom code (SC) for that error, and any other important completion and error codes from the system.

### *TA221 Running the DPCX Online Tape Exerciser*

The SYSTCM utility must be used to invoke the DPCX online tape exerciser. This section contains information that relates only to tape-unique functions. For procedures on how to run the SYSTCM utility, refer to the Chapter 2, CP810, 'How to Log On and Run DPCX Online Tests.'

Before running the exerciser:

1. Clean the tape unit to be tested. Tape-cleaning instructions are found on OPER 60 of the 8809 Maintenance Information Manual.
2. Mount a known good scratch tape reel containing a write enable ring.
3. Load the tape drive and make it ready. (The READY indicator should be on.)

Invoke SYSTCM from either the basic operator panel or a terminal:

1. At the 80BC or PA00 message, enter 'PADAB', where PA = the tape physical address and DA = the drive address. Refer to TA113 for these values.
2. At the 81BC prompt message, enter any options in the SLRRB format. Refer to TA211 for these values; for the meaning of the test messages that can be generated while running this exerciser, see TA232.
3. To continue the test after an error, enter 'B' and press either Enter Function at the BOP, or ENTER at a terminal.
4. To terminate the exerciser, enter 'F' and press either Enter Function at the BOP or ENTER at a terminal. The exerciser terminates only at either a manual intervention or error stop, or at the end of testing.

### *TA222 DPCX Exerciser Invocation Examples Using the Basic Operator Panel*

The following chart can be used for a quick reference for invoking the DPCX online exerciser from the 8130/8140 operator panel:

| Routine | Options | Enter Data | Enter Function | Enter Data | Enter Function |
|---|---|---|---|---|---|
| 01 & 02 | No loop | PADA | B | - - - | B |
| 01 & 02 | No loop | PADA | B | 1 | B |
| 01 & 02 | Loop, stop on error* | PADA | B | 11 | B |
| 02 only | No loop | PADA | B | 1002 | B |
| 02 only | Loop, stop on error* | PADA | B | 1102 | B |
| 02 only | Loop, no stop on error** | PADA | B | 1202 | B |

* The tests will loop for 4 minutes unless an error is detected. The tests cannot be terminated until after the 4-minute loop or unless an error is detected.

**The tests cannot be terminated until after the 4-minute loop.

1. To terminate the utility at a terminal, enter 'D' and press ENTER. This action terminates the SYSTCM function, but the terminal is NOT logged off. To log off, perform the appropriate terminal logoff procedure.
2. To terminate the utility at the basic operator panel, enter 'D' and press Enter Function.

If invoked from a terminal, the terminal displays the complete error data. If using the basic operator panel, additional data must be displayed by entering 'E' and pressing Enter Function. Four hexadecimal digits display each time you enter 'E' and press Enter Function. The number of digits in a message varies according to the error format, but a blank field always indicates the end of the message. If you continue to enter 'E' and press Enter Function, it repeats the message fields.

## TA230 Test Messages and Status Information

### *TA231 Offline Tape Adapter Tests*

The following messages are generated while running the offline tests:

- PA00 = successful test completion
- PA80 = channel I/O hang condition
- PAF0 = test started
- XXBC = test control monitor error
- PAXE RREN = SCF, adapter, or tape drive error

The following table lists the different message formats produced by the tests:

| Format Type | Message |
|---|---|
| 1 | PAXE RREN SSSS |
| 2 | PAXE RREN AACC SSSS |
| 3 | PAXE RREN SSSS TTPP BBBB XXXX XXXX (See Note 1) |
| 4 | PAXE RREN EEGG TTPP BBBB XXXX XXXX (See Note 1) |
| 5 | XXBC |
| 5 | PA00 |
| 5 | PA80 |
| 5 | PAF0 |

Where:

PA = tape unit or adapter address
X = 1 then PA = adapter address
X = 2 then PA = tape unit address
E = E which indicates an error
RREN = Isolation Code, where:
  RR = Routine number
  EN = Error number
EE = Expected data byte
GG = Actual data byte
AA = Adapter address
CC = Adapter command
SSSS = Adapter status (See Note 2), where:
  Bit 0 = Nonrecoverable error
  1 = Invalid subcommand
  2 = Parity error
  3 = Control line sequence error
  4 = Poll detect
  5 = Count error
  6 = Disconnected operation
  7 = Overrun/underrun
  8 = Normal/FCB end
  9 = Bus not zero
  10 = Timeout
  11 = End error
  12 = Program requested interrupt
  13 = Machine check
  14 = Enabled
  15 = Interruption
TT = Tape unit status byte, where:
  Bit 0 = Ready
  1 = Busy
  2 = Write Enabled
  3 = Beginning of Tape
  4 = End of Tape
  5 = Op Complete
  6 = Low Speed
  7 = Positioning
PP = Program set status byte, where:
  Bit 0 = Adapter status indicates an error
  1 = Error on Read Sense command
  2 = Busy and Op Complete on together
  3 = 10-second ending timeout in disconnected Op
  4 = Sense information in storage is valid
  5 = 10-second ending status timeout not disconnected Op
  6 = Reel selected alert
  7 = Real control line timeout
BBBB = Last command sent to tape unit
XXXX = Sixteen tape unit sense bytes
XXBC = See General Failure Index (ST100)

**Notes:**

1. *Formats 3 and 4 may be truncated from the right, by field, on certain errors, depending on available information.*
2. *Will be FFFF if status is not reliable.*

## *TA232 DPCX Online Exerciser*

The following messages are generated while running the DPCX online exerciser.

| Format Type | Message |
|---|---|
| 1 | XXBC |
| 2 | PAXX |
| 3 | PAXE RREN SYMC CFPF ECOP ARCX TCSB XXXX – XXXX MC00 MEME |

**Note:** *XXBC and SYMC are the error messages needed for MAP "Test Symptom Code".*

Where:

Format 1 – XXBC:

XX = Error number
BC = Indicates a system error detected by the test control monitor (see General Failure Index, ST200)

Format 2 – PAXX:

PA = The address of the component under test
XX = 00 – Successful completion test
XX = 01 – Mount a tape. Enter 'B' when complete
XX = 02 – Waiting for ready
XX = 90 – Selected device busy or unavailable for testing
XX = F0 – Test in progress

Format 3 – PAXE:

PA = The address of the component under test
X = 1 – Indicates the 'PA' is the adapter address
X = 2 – Indicates the 'PA' is the tape drive address
E = E – Indicates that this is an error message
RR = Routine number that failed
EN = Error number (see TA244 for explanation)
SYMC = Symptom Code (see TA243 Routine 6C for list of codes)
*CF = Retry and Completion Flags (IOCB Byte 2)
*PF = Program Flags (IOCB Byte 3)
*EC = Error Code (IOCB Byte 23)
*OP = Operation number
*ARCX = Adapter Return Code
TCSB = Adapter Status Bytes
XXXX = Tape Unit Sense Bytes (16)
*MC00 = Macro completion Code plus 1 byte of 00
*MEME = Macro Error Code

*This information is not needed by the MAPs.

*TA233 Status and Sense Bytes*

This section lists and describes the status and sense bytes used for the 8809. Figure 233-1 shows all 16 tape drive sense bytes, as well as the two adapter status bytes, which are then discussed and shown in detail.

**Sense Byte 0 (Tape Unit Status)**

| Ready | Busy | Write Enable | BOT | EOT | Operation Complete | Low Speed | Positioning |
|---|---|---|---|---|---|---|---|

Bit 0 — Ready: indicates that the tape drive has a tape loaded with tension established.

Bit 1 — Busy: set with the initiation of a Disconnected command and remains set until receiving an Op Complete or a Check Reset. Also set while performing a load rewind operation from the tape operator panel.

Bit 2 — Write Enable: set when the tape is not file protected (write enable ring installed). Write commands set Selected Alert when issued to the tape drive with Write Enable off.

Bit 3 — BOT: set when the tape is positioned at the beginning of tape (BOT) marker. Any backward command issued to the tape drive with BOT on sets Selected Alert.

Bit 4 — EOT: set when sensing the end of tape (EOT) marker in the forward tape direction and reset when sensing the EOT marker in the reverse direction.

Bit 5 — Operation Complete: set when completing a disconnected command (other than space file) with the tape drive at the stop lock position. During a space file operation, the bit sets when a tape mark is detected. Also set when performing a load rewind from the tape operator panel. This bit is reset by Check Reset.

Bit 6 — Low Speed: when set, indicates that the speed of the tape drive is 31.75 centimeters/seconds (12.5 ips). When reset, the speed is 254 centimeters/second (100 ips).

Bit 7 — Positioning: indicates that the tape drive is in a positioning sequence.

| Status Byte | Sense Byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | Ready | Busy | Write Enable | BOT | EOT | Operation Complete | Low Speed | Positioning |
| | 1 | Check End Sense | Bus Out Parity Check * | Tag Bus Parity Check * | Formatter Write or CNT-L Failure * | CNTL-L Sequence Check * | Command Register Parity Chk * | Drive Control Parity Chk* | Formatter Read Failure * |
| | 2 | Data Overrun | Data Check | --- | BOT | EOT | Tape Mark Detected | Not Capable | --- |
| | 3 | Write Bus Parity Check * | Bus Out Register Parity Chk* | Gap Control Check * | Sync Out Check * | Drive Response Check * | Not Capable (Space File)* [1] | Track in Error P | Write Enable Error * |
| | 4 | Same as 3-0 | Read Bus Parity Check * | Same as 3-2 | Same as 3-3 | --- | --- | Same as 3-6 | Same as 3-7 |
| | 5 | POINTER REGISTER: Track 0 | Track 1 | Track 2 | Track 3 | Track 4 | Track 5 | Track 6 | Track 7 |
| | 6 [2] | 1 = Write Command | PE ID Check | Multitrack Error | End Data Check | Start Read Check | Read Back Failure [3] | Envelope Check | Write TM Error |
| | | 0 = Non Write | No Track Pointer | Multitrack Error | End Data Check | Start Read Check | Crease | Unused | Skew Error |
| | 7 | --- | --- | --- | --- | --- | --- | --- | --- |
| | 8 | TRANSPORT STATE: 0 | 1 | 2 | 3 | 4 | Sequence Error * | Sense Bus Parity Check * | --- |
| | 9 | Start Velocity Check * | End Velocity Check * | PE ID Velocity Check * | Clock Parity Error * | SERVO STATE: 0 | 1 | Same as 8-6 | --- |
| | 10 | Load Check * | Tension Check * | Cover/Reel Latch Interrupt * | Tension Status | Not Ready Due to Reset * | Long Gap Mode | Same as 8-6 | --- |
| | 11 | PRESENT TRANSPORT STATE: 0 | 1 | 2 | 3 | 4 | Cover/Reel Latch Interlock Status | Same as 8-6 | --- |
| | 12 | Servo Logic Failure * | Servo Analog Failure * | Write Current Failure * | Erase Current Failure * | PRESENT SERVO STATE: 0 | 1 | Same as 8-6 | --- |
| | 13 | Idler Tach Failure * | Machine Tach Failure * | File Tach Failure * | Idler Tach Rotation Check * | --- | --- | Same as 8-6 | --- |
| | 14 | BOT/EOT LED Failure | Tape Present LED Failure * | Reel Size LED Failure * | Drive Control Failure * | --- | --- | Same as 8-6 | --- |
| | 15 | File Amplifier Saturation * | Machine Amplifier Saturation * | Write Status | PA Cable Unseated * | LWR Failure | Adapter PIO Command | Same as 8-6 | Unexpected Adapter Status |
| Adapter Status Extended | | Non-Recoverable Error | Invalid Sub Command | Adapter Parity Check | CNTL-L Sequence Error | Poll/ Command Mach Chk | Residual Count Error | Disconnect | Overrun/ Underrun |
| Adapter Status | | Normal/ FCB End | Bus Not Equal to Zero | Timeout | End Error | Program Requested Interrupt | Machine Check ** | Interrupt Enable ** | Interrupt/ Halt ** |

[1] Sense byte 1, bit 0 (1-0) and 2-6.

[2] Any bit sets 2-1 (except Read Back Failure—see [3] .

[3] If 1-0 is off, brings up 1-7 and activates the Selected Alert line.

*These bits activate the Selected Alert line. **These adapter bits do *NOT* cause an interrupt.

**Figure TA233-1. Status and Sense Bytes**

**Sense Byte 1**

| Check End Sense | Bus Out Parity Check * | Tag Bus Parity Check * | Formatter Write or CNT-L Failure * | CNTL-L Sequence Check * | Command Register Parity Chk * | Drive Control Parity Chk* | Formatter Read Failure * |
|---|---|---|---|---|---|---|---|

*These bits activate the Selected Alert line.

Bit 0 — Check End Sense: indicates that either a Check End occurred following the last command or that Not Capable occurred during a space file operation. Sense byte 2 is valid when this bit is on.

Bit 1 — Bus-Out Parity Check: set if even parity is detected on the Control Line Bus Out during a Write Data transfer.

Bit 2 — Tag Bus Parity Check: set if even parity is detected on the Control Line Tag Bus Out.

Bit 3 — Formatter Write or Control Line Failure: indicates internal failure of either the Control Line or the Write modules.

Bit 4 — Control Line Sequence Check: set when a Control Line sequence error occurred.

Bit 5 — Command Register Parity Check: set when odd parity is detected on the Command Register bus from the formatter card to the drive control card.

Bit 6 — Drive Control Parity Check: set when odd parity is detected on the control bus from the drive control card.

Bit 7 — Formatter Read Failure: indicates either an internal failure of the Read, or read-back data did not occur when expected during a Write command.

**Sense Byte 2**

| Data Overrun | Data Check | --- | BOT | EOT | Tape Mark Detected | Not Capable | --- |
|---|---|---|---|---|---|---|---|

Bit 0 — Data Overrun: no write data available when the tape drive is ready to receive it.

Bit 1 — Data Check: indicates that one or more of the sense byte 6 bits are active.

Bit 2 — not used.

Bit 3 — BOT: see sense byte 0, bit 3.

Bit 4 — EOT: set only when EOT is detected during either a Write, Write Tape Mark, or Erase Gap operation.

Bit 5 — Tape Mark Detected: indicates a tape mark was detected during a Read or Space Block operation.

Bit 6 — Not Capable: set when a 1600-bpi ID burst is not detected while reading or spacing from BOT. This bit is also set with a Data Check (sense byte 2, bit 1) due to a PEID Burst Check (sense byte 6, bit 1) during a write from BOT.

Bit 7 — not used.

**Sense Byte 3**

| Write Bus Parity Check * | Bus Out Register Parity Chk * | Gap Control Check * | Sync Out Check * | Drive Response Check * | Not Capable [1] (Space File) | Track in Error P | Write Enable Error * |
|---|---|---|---|---|---|---|---|

* These bits activate the Selected Alert line.

[1] Sets sense byte 1, bit 0 and sense byte 2, bit 6.

Bit 0 — Write Bus Parity Check: indicates even parity on the 10-bit bus to the write card.

Bit 1 — Bus-Out Register Parity Check: indicates even parity on the internal formatter bus from the bus-out register.

Bit 2 — Gap Control Check: indicates the gap control line dropped before writing a complete record.

Bit 3 — Sync-Out Check (Write only): set when more than one sync-out signal is received from the adapter in response to a single sync-in, or the sync-out signal did not reset in the specified time.

Bit 4 — Drive Response Check: set if motion logic responds either early or late to the Formatter command.

Bit 5 — Not Capable (Space File): set when the PEID burst is not detected while executing a space file operation from BOT. This bit sets sense byte 1, bit 0 and sense byte 2, bit 6.

Bit 6 — Track in Error P: indicates the Track P pointer was on at the end of the last operation in which a data check occurred.

Bit 7 — Write Enable Error: indicates that a write was attempted with Write Enable off.

**Sense Byte 4**

| Same as 3-0 | Read Bus Parity Check * | Same as 3-2 | Same as 3-3 | --- | --- | Same as 3-6 | Same as 3-7 |
|---|---|---|---|---|---|---|---|

* These bits activate the Selected Alert line.

Bit 0 — Write Bus Parity Check: same as sense byte 3, bit 0.

Bit 1 — Read Bus Parity Check: indicates bad parity on the read data bus from the Read Control module to the Bus In Assembler.

Bit 2 — Gap Control Check: same as sense byte 3, bit 2.

Bit 3 — Sync-Out Check: same as sense byte, bit 3.

Bits 4 & 5 — Not used.

Bit 6 — Track in Error P: same as sense byte 3, bit 6.

Bit 7 — Write Enable Error: same as sense byte, bit 7.

**Sense Byte 5**

| POINTER REGISTER | | | | | | | |
|---|---|---|---|---|---|---|---|
| Track 0 | Track 1 | Track 2 | Track 3 | Track 4 | Track 5 | Track 6 | Track 7 |

This byte contains the track-in-error pointers for tracks 0-7. It contains track(s) for which pointers were on at the end of the last operation in which a data check occurred.

**Sense Byte 6 — Write Block or Write Tape Mark Only (Bit 0 = 1)**

| | 1 = Write Command | PEID Check | Multitrack Error | End Data Check | Start Read Check | Read Back Failure 3 | Envelope Check | Write TM Error |
|---|---|---|---|---|---|---|---|---|
| 2 | | | | | | | | |

2 Any bit sets sense byte 2, bit 1 except for a Read Back Failure (see 3 ).

3 If sense byte 1, bit 0 is off, sets sense byte 1, bit 7 and also activates the Selected Alert line.

Bit 0 = 1 = Write Command.

Bit 1 — PEID Check (with Data Check): set when PEID burst is not detected during read-back check when writing from the BOT marker.

Bit 2 — Multi-Track Error: set if a multiple track error (more than one pointer) is detected during read-back check.

Bit 3 — End Data Check: set when an IBG is detected earlier or later than expected during read-back check.

Bit 4 — Start Read Check: set if Beginning of Record drops, or an IBG is detected after Beginning of Record but before the first 1-bits of the preamble during read-back check.

Bit 5 — Read-Back Failure:

- Sense byte 1, bit 0 not set: indicates read-back data did not occur when expected during a Write command. Also sets Selected Alert and Formatter Read Failure (sense byte 1, bit 7).
- Sense byte 1, bit 0 set: indicates that a crease was detected during the read-back check of a Write command, and does not set Selected Alert.

Bit 6 — Envelope Check: set when a skew buffer parity check or any phase error is detected during read-back check.

Bit 7 — WTM Error: indicates fewer than 40 bytes of tape mark were written during a write tape mark operation.

**Sense Byte 6 — Not Write Block or Write Tape Mark (Bit 0 = 0)**

| | 0 = Non Write | No Track Pointer | Multitrack Error | End Data Check | Start Read Check | Crease | Unused | Skew Error |
|---|---|---|---|---|---|---|---|---|
| 2 | | | | | | | | |

2 Any bit sets sense byte 2, bit 1.

Bit 0 = 0 = Non-Write Command.

Bit 1 — No Track Pointer: indicates Skew Buffer parity check (VRC) with no track pointer on.

Bit 2 — Multi-Track Error: set if a multiple error (more than one pointer) is detected. The data was uncorrectable.

Bit 3 — End Data Check: set when an IBG is detected earlier or later than expected

Bit 4 — Start Read Check: set if Beginning of Record drops, or an IBG is detected after Beginning of Record but before the first 1-bits of the preamble.

Bit 5 — Crease: set when IBG is detected during data transfer and crease timeout is not reached.

Bit 6 — Not used.

Bit 7 — Skew Error: indicates a skew buffer overflow.

**Sense Byte 7 — Not Used**

**Sense Byte 8**

| TRANSPORT STATE | | | | | Sequence Error * | Sense Bus Parity Check * | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | | | - - - |

* These bits activate the Selected Alert line.

Bits 0–4 Transport State: show the encoded state of the tape drive at the time a sequence error (sense byte 8, bit 5) occurred.

The transport states are:

| Sense Bit 01234 | State Name |
|---|---|
| 00000 | Idle |
| 00001 | Take Up Slack |
| 00010 | Enable Servo |
| 00011 | Sample Radius |
| 00100 | High-Speed Load Point |
| 00101 | Rewind Stop |
| 00110 | Rewind Forward Space |
| 00111 | Rewind |
| 01100 | Low-Speed Load Point |
| 01101 | Move to BOT |
| 01111 | Space Over BOT |
| 01110 | Write ID Burst |
| 01001 | Unload Leader |
| 01000 | Space to Low-Speed Load |
| 11000 | Data Security Erase |
| 11001 | Set Erase Gate, Alternate Direction |
| 11011 | Low-Speed Degauss |
| 11010 | Prepare Gap Control, Alternate Direction |
| 11110 | Prepare Gap Control, Previous Direction |
| 11111 | Write Backward Hitch |
| 11101 | Set Erase Gate, Previous Direction |
| 11100 | Low-Speed Wait |
| 10100 | High-Speed Wait |
| 10101 | Overrun, Alternate Direction |
| 10111 | Move From Hold |
| 10110 | Degauss Area |
| 10010 | Reversal |
| 10011 | Overrun Same Direction |
| 10001 | Go Hold Over |

Bit 5 – Sequence Error: indicates the loss of tension while the servo is active (Tension Check – sense byte 10, bit 1) or a Load Check (sense byte 10, bit 0) occurred.

Bit 6 – Sense Bus Parity Check: set when even parity is detected on the internal sense bus during a Read Sense command for sense bytes 8–15. Any byte 8–15 can contain the first occurrence of this error indicator, and, once detected, sets bit 6 of all remaining check bytes.

Bit 7 – Not used.

**Sense Byte 9**

| Start Velocity Check * | End Velocity Check * | PE ID Velocity Check * | Clock Parity Error * | SERVO STATE | | Same as 8-6 | |
|---|---|---|---|---|---|---|---|
| | | | | 0 | 1 | | - - - |

* These bits activate the Selected Alert line.

Bit 0 – Start Velocity Check: indicates a velocity problem occurred before a write data transfer.

Bit 1 – End Velocity Check: indicates a velocity problem occurred during a write data transfer.

Bit 2 – PEID Velocity Check: indicates a velocity problem occurred while attempting to write a PEID burst.

Bit 3 – Clock Parity Error: set if an internal parity error is detected in the clock generation module.

Bits 4 & 5 – Servo State: indicate the encoded state of the servo at the time of a sequence error (sense byte 8, bit 5).

The following shows bits 4 and 5 interpretation:

| Bits 4 and 5 | State Name |
|---|---|
| 00 | Idle |
| 01 | Stoplock |
| 10 | Run |
| 11 | Plug Start |

Bit 6 – Sense Bus Parity Check: same as sense byte 8, bit 6.

Bit 7 – Not used.

**Sense Byte 10**

| Load Check * | Tension Check * | Cover/Reel Latch Interrupt * | Tension Status | Not Ready Due to Reset * | Long Gap Mode | Same as 8-6 | --- |
|---|---|---|---|---|---|---|---|

* These bits activate the Selected Alert line.

Bit 0 – Load Check: indicates that a load rewind initiated from the tape operator panel failed to execute.

Bit 1 – Tension Check: indicates tension failure caused a sequence error (sense byte 8, bit 5).

Bit 2 – Cover/Reel Latch Interrupt: indicates an active condition of either the cover interlock or the reel latch interlock while the tape is loaded and the reel motors are under servo control. This condition inhibits Ready and Reset.

Bit 3 – Tension Status: indication to the transducer channel that a tape is present as detected by the 'tape present' sensor.

Bit 4 – Not Ready Due to Reset: indicates that the RESET pushbutton on the tape operator panel has reset Drive Ready. Also set when a command was issued that expected a ready condition, and the drive was not ready.

Bit 5 – Long Gap Mode: indicates that the tape drive is in Long Gap Mode.

Bit 6 – Sense Bus Parity Check: same as sense byte 8, bit 6.

Bit 7 – Not used.

**Sense Byte 11**

| PRESENT TRANSPORT STATE | | | | | Cover/Reel Latch Interlock Status | Same as 8-6 | --- |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | | | |

Sense byte 11 presents the tape drive and cover interlock status while executing the Read Sense Byte 11 command.

Bits 0-4 – Present Transport State: show the present tape drive status. See Sense Byte 8 for an explanation of the bits.

Bit 5 – Cover/Reel Latch Interlock Status: indicates the cover is open.

Bit 6 – Sense Bus Parity Check: same as sense byte 8, bit 6.

Bit 7 – Not used.

**Sense Byte 12**

| Servo Logic Failure * | Servo Analog Failure * | Write Current Failure * | Erase Current Failure * | PRESENT SERVO STATE | | Same as 8-6 | --- |
|---|---|---|---|---|---|---|---|
| | | | | 0 | 1 | | |

* These bits activate the Selected Alert line.

Bit 0 – Servo Logic Failure: indicates a failure on the drive control card associated with the servo.

Bit 1 – Servo Analog Failure: indicates a failure on the power amplifier card.

Bit 2 – Write Current Failure: indicates either detection of no write current after setting write status or detection of improper current in the write head, which could destroy data.

Bit 3 – Erase Current Failure: indicates either detection of no erase current after setting erase status or detection of improper current in the erase head, which could destroy data.

Bits 4 & 5 – Present Servo State: indicate the state of the servo while executing the Read Sense Byte 12 command. See Sense Byte 9 for an explanation of the bits.

Bit 6 – Sense Bus Parity Check: same as sense byte 8, bit 6.

Bit 7 – Not used.

**Sense Byte 13**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Idler Tach Failure * | Machine Tach Failure * | File Tach Failure * | Idler Tach Rotation Check * | --- | --- | Same as 8-6 | --- |

* These bits activate the Selected Alert line.

Bit 0 – Idler Tach Failure: indicates detection of an idler tachometer failure in the 'run' servo state.

Bit 1 – Machine Tach Failure: indicates detection of a drive reel motor tachometer failure.

Bit 2 – File Tach Failure: Indicates detection of a file reel motor tachometer failure.

Bit 3 – Idler Tach Rotation Check: indicates the idler tachometer frequency is below a minimum allowable level during a normal start/stop operation. This condition can be caused by a tension failure, the tape sticking at the read/write head, or an idler tachometer failure.

Bits 4 & 5 – Not used.

Bit 6 – Sense Bus Parity Check: same as sense byte 8, bit 6.

Bit 7 – Not used.

**Sense Byte 14**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BOT/EOT LED Failure* | Tape Present LED Failure * | Reel Size LED Failure * | Drive Control Failure * | --- | --- | Same as 8-6 | --- |

* These bits activate the Selected Alert line.

Bit 0 – BOT/EOT LED Failure: indicates no current is detected in the BOT or EOT sensor LEDs.

Bit 1 – Tape Present LED Failure: indicates no current is detected in the tape sensor LED.

Bit 2 – Reel Size LED Failure: indicates either (1) that no current is detected in one of the reel size sensor LEDs, (2) that the measured radius of the tape exceeds the reel size, or (3) detection of an incorrect reel size.

Bit 3 – Drive Control Failure: indicates a failure in the control module.

Bits 4 & 5 – Not used.

Bit 6 – Sense Bus Parity Check: same as sense byte 8, bit 6.

Bit 7 – Not used.

**Sense Byte 15**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| File Amplifier Saturation * | Machine Amplifier Saturation * | Write Status | PA Cable Unseated * | LWR Failure | Adapter PIO Command | Same as 8-6 | Unexpected Adapter Status |

* These bits activate the Selected Alert line.

Bit 0 – File Amplifier Saturation: indicates that the file reel motor amplifier detected a voltage saturation condition.

Bit 1 – Machine Amplifier Saturation: indicates that the machine reel motor amplifier detected a voltage saturation condition.

Bit 2 – Write Status: indicates that the tape drive has just executed a Write, Write Tape Mark, Erase Gap, or Data Security Erase command.

Bit 3 – Power Amplifier Cable Unseated: indicates that the cable between the logic gate and the power amplifier board is not properly seated at either or both connectors.

Bit 4 – LWR Failure: indicates a failure occurred while performing an LWR command.

Bit 5 – Adapter PIO Command: indicates the last command issued by the adapter was a PIO-type command.

Bit 6 – Sense Bus Parity Check: same as sense byte 8, bit 6.

Bit 7 – Unexpected Adapter Status: indicates the adapter status bits were not as expected after issuing a command.

**Adapter Status Bytes**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Adapter Status Extended | Non-Recoverable Error | Invalid Sub Command | Adapter Parity Check | CNTL-L Sequence Error | Poll/ Command Mach Chk | Residual Count Error | Disconnect | Overrun/ Underrun |
| Adapter Status | Normal/ FCB End | Bus Not Equal to Zero | Timeout | End Error | Program Requested Interrupt | Machine Check ** | Interrupt Enable ** | Interrupt/ Halt ** |

** These adapter bits do *NOT* cause an interrupt.

Bit 0 — Nonrecoverable Error: set when the adapter detects a parity error when transmitting either the basic or extended address to the processor during a Transfer in Channel (TIC) command.

Bit 1 — Invalid Subcommand: set when (1) tape command bits 5–7 Byte 0, halfword 0 do not compare with bits 1–3 Byte 0, halfword 1 in the command FCB; (2) either an FCB data bit does not follow a read/write FCB command, or when receiving a new command before receiving the end of data in an 8809 read/write sequence; (3) receiving an invalid command during a PIO operation.

Bit 2 — Adapter Parity Check: an internal adapter parity error was detected.

- If the error occurred on data transfer from the tape bus, bit 3 is also set.
- If the error occurred on data transfer to the processor, parity is corrected before any transfer and the operation terminates.
- If the error occurred on data transfer to the tape, recycle drops, parity is corrected before any transfer, and the operation terminates.

Bit 3 — Control Line Sequence Error: set for the following conditions:

- Along with status bit 2 when a parity error is detected while transferring data from tape.
- Along with basic status bit 10 when no response causes a timeout error.
- When Select Hold and Select Active are not on either when initiating a sequence other than Selection, or when receiving a Select command with 'Select' active.
- Along with End Error when Normal End did not set with Tag Valid active.

Bit 4 — Poll/Command Machine Check: set when either receiving a response to a Poll command, or when a machine check occurs during any channel I/O operation using a channel control vector (CHCV).

Bit 5 — Residual Count Error: set during a read sequence with the Suppress Length Flag off, when the number of bytes transferred by a tape unit does not equal the segment count.

Bit 6 — Disconnect: set when the adapter issues a Disconnect command.

Bit 7 — Overrun/Underrun: set when a delay occurs in processor information transfer. The adapter either does not have sufficient buffer space to continue operation to the tape or sufficient data to transfer to the processor.

Bit 8 — Normal or FCB End: after receiving a Sequence command on the PIO bus, this bit sets when receiving a Normal End from the tape drive at the completion of an Execute sequence. For a Sequence command received from an FCB, this bit is set only: (1) if the Normal End Tag Line from the tape drive is active and Ending Status does not equal 0; (2) after the completion of the 'Disconnect Command Sequence'; or (3) after an FCB 'End Op' Command.

Bit 9 — Bus Not Equal to 0: set when receiving a Normal End (bit 8 is also set) with ending status not equal to hex 00 (BOT or EOT mark detected). If command was received from an FCB, no additional requests to the FCB are made. Also set when the address of the TAM responding to a Select sequence does not agree with the transmitted address.

Bit 10 — Timeout: set approximately one second after receiving the Enable Timer command. Also set when the entire sequence did not complete within the time expected, and also sets Status Bit 3 for this condition.

Bit 11 — End Error: set when receiving either Selected Alert or Check End from tape.

Bit 12 — Program Requested Interrupt: set when receiving Program Requested Interrupt (PRI bit) during FCB operation.

*Bit 13 — Machine Check: set when a processor machine check occurred while communicating with the tape adapter.

*Bit 14 — Interrupt Enable: set to allow the adapter to make interrupt requests and to initiate channel requests. When reset, the adapter removes any requests before responding with valid.

Bit 15 — Interrupt/Halt: this bit is the 'OR' of conditions defined that cause an interrupt. Set by the Halt signal, and also when the adapter is going to suppress a response because of receiving bad parity on the processor bus.

*Bits 13 and 14 do not cause an interrupt.

## TA240 Test Error Message Descriptions

All TA offline and DPCX online exerciser test error messages (such as PAXE RREN SSSS) have an error number (EN). This error number indicates the type of failure detected, as well as additional status information available according to the test error message format. The routine number (RR) and the EN determine the error message formats.

The following sections contain a list of all error numbers used for each routine and describe their meaning. Section TA241 lists and describes the adapter test error numbers, section TA242 contains those used for tape drive testing, TA243 contains the test error messages used for the special requirement tests, and TA244 lists and describes the test error messages generated when running the DPCX Online Exerciser. Refer to the TA230 section for test message formats.

### *TA241 Adapter Test Messages*

The following table lists, for each routine, the error numbers and their description for the adapter tests. For test message formats, see TA231.

| RREN | Format | Meaning |
|---|---|---|
| 0101 | 2 | Unexpected machine check. |
| 0104 | 1 | Unexpected I/O interruption. |
| 0106 | 1 | Interruption always active. |
| 0109 | 1 | CHIO machine check. |
| 010C | 2 | Solid I/O machine check. |
| 0201 | 2 | Unexpected machine check. |
| 0202 | 1 | Expected machine check did not occur. |
| 0204 | 1 | Unexpected I/O interruption. |
| 0206 | 1 | Interruption always active. |
| 0207 | 1 | Machine check status not set by invalid command. |
| 0208 | 1 | Invalid subcommand bit not set by invalid command. |
| 0209 | 1 | CHIO machine check. |
| 020C | 2 | Solid I/O machine check. |
| 0301 | 2 | Unexpected machine check. |
| 0304 | 1 | Unexpected I/O interruption. |
| 0306 | 1 | Interruption always active. |
| 0309 | 1 | CHIO machine check. |
| 030C | 2 | Solid I/O machine check. |
| 0310 | 1 | CHCVD register write-read did not compare. |
| 0311 | 1 | CHCVD register not 0 after adapter reset. |
| 0312 | 1 | CHCVC register write-read did not compare. |
| 0313 | 1 | CHCVC register not 0 after adapter reset. |
| 0314 | 1 | Segment count register write-read non-compare. |
| 0315 | 1 | Segment count register not 0 after adapter reset. |
| 0316 | 1 | BADDR write-read did not compare. |
| 0317 | 1 | BADDR not 0 after adapter reset. |
| 0318 | 1 | EADDR write-read did not compare. |
| 0319 | 1 | EADDR not 0 after adapter reset. |
| 031A | 1 | PSAR write-read did not compare. |
| 031B | 1 | PSAR not 0 after adapter reset. |
| 031C | 1 | CLSAR write-read did not compare. |
| 031D | 1 | CLSAR not 0 after adapter reset. |
| 031E | 1 | Burst length register write-read did not compare. |
| 031F | 1 | Burst length register not 0 after adapter reset. |
| 0320 | 1 | Burst length counter set-read did not compare. |
| 0321 | 1 | Burst length counter not 0 after adapter reset. |
| 0401 | 2 | Unexpected machine check. |
| 0404 | 1 | Unexpected I/O interruption. |
| 0405 | 1 | I/O interruption did not occur. |
| 0406 | 1 | Interruption always active. |
| 0409 | 1 | CHIO machine check. |
| 040C | 2 | Solid I/O machine check. |
| 0422 | 1 | Basic status not 0 after adapter reset. |
| 0423 | 1 | Extended status not 0 after adapter reset. |
| 0424 | 1 | Extended status set/read did not compare. |
| 0425 | 1 | Interrupt bit not set by extended status bit. |
| 0426 | 1 | Basic status set/read did not compare. |
| 0427 | 1 | Interrupt bit not set by basic status bit. |
| 0428 | 1 | Interrupt bit set by machine check bit. |
| 042A | 1 | Extended status bit not reset under mask. |
| 042B | 1 | Basic status bit not reset under mask. |
| 042C | 1 | Set basic status failed to set pending bit. |
| 042D | 1 | Enable bit not reset by reset basic status. |
| 0501 | 2 | Unexpected machine check. |
| 0504 | 1 | Unexpected I/O interruption. |
| 0506 | 1 | Interruption always active. |
| 0507 | 1 | Incorrect basic status after timer interruption. |
| 0509 | 1 | CHIO machine check. |
| 050C | 2 | Solid I/O machine check. |
| 052E | 1 | Timer did not cause interruption. |
| 052F | 1 | Incorrect extended status after timer interruption. |
| 0530 | 1 | Timer less than 800 ms. |
| 0531 | 1 | Timer longer than 1200 ms. |
| 0532 | 1 | Extra timer interrupt. |
| 0601 | 2 | Unexpected machine check. |
| 0604 | 1 | Unexpected I/O interruption. |
| 0606 | 1 | Interruption always active. |
| 0609 | 1 | CHIO machine check. |
| 060C | 2 | Solid I/O machine check. |
| 0633 | 1 | CLSAR set by Set PSAR command. |
| 0634 | 1 | PSAR set by Set CLSAR command. |
| 0635 | 1 | Burst Length Counter set by Write Segment Counter command. |
| 0636 | 1 | Segment Counter set by Load Burst Length Counter command. |
| 0637 | 1 | PSAR not stepping correctly. |
| 0638 | 1 | CLSAR not stepping correctly. |
| 0639 | 1 | Segment counter not stepping correctly. |
| 063A | 1 | Burst length counter not stepping correctly. |

| RREN | Format | Meaning |
|---|---|---|
| 0640 | 1 | CLSAR set by Write Segment Counter command. |
| 0641 | 1 | CLSAR set by Load Burst Length Counter command. |
| 0650 | 1 | PSAR set by Write Segment Counter command. |
| 0651 | 1 | PSAR set by Load Burst Length Counter command. |
| 0701 | 2 | Unexpected machine check. |
| 0704 | 1 | Unexpected I/O interruption. |
| 0706 | 1 | Interruption always active. |
| 0709 | 1 | CHIO machine check. |
| 070C | 2 | Solid I/O machine check. |
| 073B | 1 | Buffer write-read did not compare. |
| 073C | 1 | PSAR did not step on read buffer command. |
| 073D | 1 | PSAR did not step on write buffer command. |
| 073E | 1 | Parity error while reading buffer. |
| 073F | 1 | Parity error while writing buffer. |
| 0801 | 2 | Unexpected machine check. |
| 0804 | 1 | Unexpected I/O interruption. |
| 0806 | 1 | Interruption always active. |
| 0807 | 1 | Basic status incorrect. |
| 0809 | 1 | CHIO machine check. |
| 080C | 2 | Solid I/O machine check. |
| 082F | 1 | Extended status incorrect. |
| 0840 | 1 | CLSAR did not step on wrap command. |
| 0841 | 1 | Wrapped data not equal to original |
| 0901 | 2 | Unexpected machine check. |
| 0904 | 1 | Unexpected I/O interruption. |
| 0905 | 1 | No interruption after executing Function Control Block (FCB) list. |
| 0906 | 1 | Interruption always active. |
| 0909 | 1 | CHIO machine check. |
| 090C | 2 | Solid I/O machine check. |
| 0942 | 1 | Command CPR not stepping correctly. |
| 0943 | 1 | Normal end status not set after FCB list was executed. |
| 1101 | 2 | Unexpected machine check. |
| 1104 | 1 | Unexpected I/O interruption. |
| 1105 | 1 | No I/O interruption after executing FCB list. |
| 1106 | 1 | Interruption always active. |
| 1109 | 1 | CHIO machine check. |
| 110C | 2 | Solid I/O machine check. |
| 1143 | 1 | Command TIC did not branch. |
| 1201 | 2 | Unexpected machine check. |
| 1204 | 1 | Unexpected I/O interruption. |
| 1205 | 1 | No I/O interruption after executing FCB list. |
| 1206 | 1 | Interruption always active. |
| 1209 | 1 | CHIO machine check. |
| 120C | 2 | Solid I/O machine check. |
| 1244 | 1 | Program-Requested Interrupt (PRI) bit not on in status byte after PRI FCB. |

| RREN | Format | Meaning |
|---|---|---|
| 1301 | 2 | Unexpected machine check. |
| 1304 | 1 | Unexpected I/O interruption. |
| 1305 | 1 | No I/O interruption after executing in valid FCB. |
| 1306 | 1 | Interruption always active. |
| 1309 | 1 | CHIO machine check. |
| 130C | 2 | Solid I/O machine check. |
| 1345 | 1 | Invalid subcommand bit not set by bad FCB. |
| 1401 | 2 | Unexpected machine check. |
| 1404 | 1 | Unexpected I/O interruption. |
| 1405 | 1 | No interruption after executing TSTCLP command. |
| 1406 | 1 | Interruption always active. |
| 1408 | 3 | Open adapter failure. |
| 1409 | 1 | CHIO machine check. |
| 140C | 2 | Solid I/O machine check. |
| 1446 | 1 | Parity error status bit not on after TSTCLP command execution |
| 1501 | 2 | Unexpected machine check. |
| 1504 | 1 | Unexpected I/O interruption. |
| 1505 | 1 | No I/O interruption from test Stop command. |
| 1506 | 1 | Interruption always active. |
| 1509 | 1 | CHIO machine check. |
| 150C | 2 | Solid I/O machine check. |
| 1540 | 1 | Control line sequence error bit not set. |

## *TA242 Tape Drive Test Messages*

The following table lists, for each routine, the error numbers and their meaning for the tape drive tests. For test message formats, see TA231.

| RREN | Format | Meaning |
|---|---|---|
| 4001 | 2 | Unexpected machine check. |
| 4004 | 1 | Unexpected I/O interruption. |
| 4006 | 1 | Interruption always active |
| 4008 | 3 | Open adapter failure. |
| 4009 | 1 | CHIO machine check. |
| 400C | 2 | Solid I/O machine check. |
| 4011 | 3 | Selected Active did not come on or low-order 3 bits of returned adddress incorrect. |
| 4014 | 3 | End error up after adapter reset. |
| 4016 | 3 | Bus not 0 after adapter reset. |
| 4017 | 3 | Timeout on select command.<br>Check the following items for possible causes of failure:<br>1. Tape drive is powered down.<br>2. Tape drive was not ready prior to running tests. Power down tape drive, then power up drive and make ready.<br>3. Invalid drive address entered or no drive on system with that address.<br>4. Incorrect address set in drive address switches.<br>5. No LVL 02 entry in Configuration Table for drive address entered.<br>6. Bus and Tag cables loose or not connected (Model 1A only).<br>7. 8101 paddle connectors at A2 Y1 and A2 Z1 loose (Model 1A only). |
| 4018 | 3 | No normal end after select command. |
| 4019 | 3 | Bus-in parity error on selection. |
| 401A | 4 | High-order 5 bits of returned address on selection are incorrect. |
| 4021 | 4 | A bus-in bit did not turn on. |
| 40F0 | 3 | Selected Alert when not expected. |
| 40F1 | 3 | Check end status received. |
| 40F2 | 3 | Bus-in parity error. |
| 40F7 | 3 | End status 10-second timeout. |
| 40F8 | 3 | Control line timeout or selection error. |
| 40F9 | 3 | Unexpected adapter error. |
| 4101 | 2 | Unexpected machine check. |
| 4104 | 1 | Unexpected I/O interruption. |
| 4106 | 1 | Interruption always active. |
| 4108 | 3 | Open adapter failure. |
| 4109 | 1 | CHIO machine check. |
| 410C | 2 | Solid I/O machine check. |
| 4111 | 3 | Control line sequence error not set by selecting a selected drive. |
| 41F0 | 3 | Selected Alert when not expected. |
| 41F1 | 3 | Check end status received. |
| 41F2 | 3 | Bus-in parity error. |
| 41F7 | 3 | End status 10-second timeout. |
| 41F8 | 3 | Control line timeout or selection error. |
| 41F9 | 3 | Unexpected adapter error. |
| 4201 | 2 | Unexpected machine check. |
| 4204 | 1 | Unexpected I/O interruption. |
| 4206 | 1 | Interruption always active. |
| 4208 | 3 | Open adapter failure. |
| 4209 | 1 | CHIO machine check. |
| 420C | 2 | Solid I/O machine check. |
| 4210-17 | 4 | Sense byte 1 not correct. |
| 4218-1F | 4 | Sense byte 0 not correct. |
| 4220-27 | 4 | Sense byte 2 not correct. |
| 4228 | 3 | Control line timeout on check reset. |
| 4229 | 3 | Bus-in parity error on check reset. |
| 422A | 3 | Control line timeout reading status byte. |
| 422B | 3 | Bus-in parity error reading status byte. |
| 422C | 3 | Control line timeout reading byte 1. |
| 422D | 3 | Control line parity error reading byte 1. |
| 422E | 3 | Control line timeout reading byte 2. |
| 422F | 3 | Control line parity error reading byte 2. |
| 4230-37 | 4 | Sense byte 3 not correct. |
| 4238 | 3 | Control line timeout reading byte 3. |
| 4239 | 3 | Control line parity error reading byte 3. |
| 4240-47 | 4 | Sense byte 4 not correct. |
| 4248 | 3 | Control line timeout reading byte 4. |
| 4249 | 3 | Control line parity error reading byte 4. |
| 4258 | 3 | Control line timeout reading byte 5. |
| 4259 | 3 | Control line parity error reading byte 5. |
| 4268 | 3 | Control line timeout reading byte 6. |
| 4269 | 3 | Control line parity error reading byte 6. |
| 4278 | 3 | Control line timeout reading byte 7. |
| 4279 | 3 | Control line parity error reading byte 7. |
| 4280-87 | 4 | Sense byte 8 not correct. |
| 4288 | 3 | Control line timeout reading byte 8. |
| 4289 | 3 | Control line parity error reading byte 8. |
| 4290-97 | 4 | Sense byte 9 not correct. |
| 4299 | 3 | Control line parity error reading byte 9. |
| 42A0-A7 | 4 | Sense byte 10 not correct. |
| 42A9 | 3 | Control line parity error reading byte 10. |
| 42B0-B7 | 4 | Sense byte 11 not correct. |
| 42B9 | 3 | Control line parity error reading byte 11. |
| 42C0-C7 | 4 | Sense byte 12 not correct. |
| 42C9 | 3 | Control line parity error reading byte 12. |
| 42D0-D7 | 4 | Sense byte 13 not correct. |
| 42D9 | 3 | Control line parity error reading byte 13. |
| 42DA | 3 | Control line parity error reading byte 14. |
| 42DB | 3 | Control line parity error reading byte 15. |
| 42E0-E7 | 4 | Sense byte 14 not correct. |
| 42E8-EF | 4 | Sense byte 15 not correct. |

| RREN | Format | Meaning |
|---|---|---|
| 4301 | 2 | Unexpected machine check. |
| 4304 | 1 | Unexpected I/O interruption. |
| 4306 | 1 | Interruption always active. |
| 4308 | 3 | Open adapter failure. |
| 4309 | 1 | CHIO machine check. |
| 430C | 2 | Solid I/O machine check. |
| 4311 | 3 | Control line timeout on Loop write to Read (LWR) command. |
| 4313 | 3 | Check end on LWR and check byte 6, bit 0 = 0. |
| 4314 | 3 | Check end on LWR and check byte 6, bit 4 = 1. |
| 4315 | 3 | Check end on LWR and check byte 6, bits 1, 3, 6, 7 not all 0. |
| 4316 | 3 | Check end on LWR and check byte 6, bits 1, 3, 6, 7 all 0. |
| 4317 | 3 | LWR command failed. |
| 4318 | 3 | Tape drive file protected. |
| 4319 | 3 | One or more pointers are on following an LWR command that ended with normal end. |
| 431A | 3 | Normal End did not drop. |
| 431B | 3 | Check End not set. Normal End and Select Alert are both off. |
| 431C | 3 | Data overrun. |
| 431D | 3 | Sense byte 2, bit 1 failed. |
| 43A1 | 3 | Selected Alert on LWR and bus-out parity check was on. |
| 43A2 | 3 | Selected Alert on LWR and WRT/INTF PLA failure. |
| 43A3 | 3 | Selected Alert on LWR and sequence check is on. |
| 43A4 | 3 | Selected Alert on LWR and write bus parity check is on. |
| 43A5 | 3 | Selected Alert on LWR and gap control check is on. |
| 43A6 | 3 | Selected Alert on LWR and sync out check is on. |
| 43A7 | 3 | Selected Alert on LWR and no tape drive response. |
| 43A8 | 3 | Selected Alert on LWR and read back fail is on. |
| 43A9 | 3 | Selected Alert on LWR and write/erase current fail. |
| 43AA | 3 | Selected Alert on LWR. Appears to be a motion problem. |
| 43AB | 3 | Clock fail during LWR. |
| 43AC | 3 | Selected Alert on LWR and none of the above conditions. |
| 43AD | 3 | Read PLA fail. |
| 43F0 | 3 | Selected Alert when not expected. |
| 43F1 | 3 | Check end status received. |
| 43F2 | 3 | Bus-in parity error. |
| 43F7 | 3 | End status 10-second timeout. |
| 43F8 | 3 | Control line timeout or selection error. |
| 43F9 | 3 | Unexpected adapter error. |
| 4401 | 2 | Unexpected machine check. |
| 4404 | 1 | Unexpected I/O interruption. |
| 4406 | 1 | Interruption always active. |
| 4408 | 3 | Open adapter failure |
| 4409 | 1 | CHIO machine check. |
| 440C | 2 | Solid I/O machine check. |
| 4411 | 3 | Bus-in bit for device under test is on and should be off. |
| 4412 | 3 | Bus-in bit for device under test is off and should be on. |
| 4413 | 3 | Op Complete not on. |

| RREN | Format | Meaning |
|---|---|---|
| 4414 | 3 | Op Complete not reset by check reset. |
| 4415 | 3 | Bus-in bit for device under test is on and should be off. |
| 4416 | 3 | Bus-in bit for device under test is on. It was suppressed and should be off. |
| 4420 | 3 | Control line timeout on poll operation. |
| 4421 | 3 | Selected Alert on poll operation. |
| 4422 | 3 | Control line timeout on rewind operation. |
| 4423 | 3 | Selected Alert on rewind operation. |
| 4424 | 3 | Ready status off after rewind. |
| 4425 | 3 | Busy after reception of OP Complete |
| 44F0 | 3 | Selected Alert when not expected. |
| 44F1 | 3 | Check end status received. |
| 44F2 | 3 | Bus-in parity error. |
| 44F7 | 3 | End status 10-second timeout. |
| 44F8 | 3 | Control line timeout or selection error. |
| 44F9 | 3 | Unexpected adapter error. |
| 4601 | 2 | Unexpected machine check. |
| 4604 | 1 | Unexpected I/O interruption. |
| 4606 | 1 | Interruption always active. |
| 4608 | 3 | Open adapter failure. |
| 4609 | 1 | CHIO machine check. |
| 460C | 2 | Solid I/O machine check. |
| 4614 | 3 | Bus-in parity error on SLS. |
| 4615 | 3 | Bus-in parity error on ERG. |
| 4616 | 3 | EOT status after ERG operation. |
| 4617 | 3 | Control line timeout on SLS command. |
| 4618 | 3 | Ten-second ending status timeout on SLS operation. |
| 4619 | 3 | Busy still on after OP complete on SLS operation. |
| 461F | 3 | Sense byte 11, bits 0-4 = 01100 after SLS. |
| 4620 | 3 | Op Complete not reset by check reset. |
| 4621 | 3 | Sense byte 12, bits 4 & 5 not = 01 after rewind. |
| 4622 | 3 | Control line timeout on ERG operation. |
| 4623 | 3 | Ending status timeout on erase gap command. |
| 4627 | 3 | BOT status still on after erase gap command. |
| 4628 | 3 | Sense byte 11 not equal to 01100XXX after erase gap command. |
| 4629 | 3 | Sense byte 12 not equal to XXXX01XX after erase gap command. |
| 4631 | 3 | End status timeout on erase gap command. |
| 4632 | 3 | End statue timeout on rewind command. |
| 4633 | 3 | Busy status still on after rewind complete. |
| 4634 | 3 | BOT not on after rewind complete. |
| 4635 | 3 | Sense byte 11 not equal to 01100XXX after rewind command. |
| 4636 | 3 | Sense byte 12 not equal to XXXX01XX after rewind command. |
| 4637 | 3 | Cover/reel latch interlock interrupt check bit on. |
| 4638 | 3 | BOT/EOT LED failure check bit on. |
| 4639 | 3 | Tape present LED failure check bit on. |
| 463A | 3 | Reel size LED failure check bit on. |
| 463B | 3 | PA cable unseated check bit on. |
| 463C | 3 | Idle tach failure check bit on. |

| RREN | Format | Meaning |
|---|---|---|
| 463D | 3 | Match tach failure check bit on. |
| 463E | 3 | File tach failure check bit on. |
| 463F | 3 | Idler tach rotation check bit on. |
| 4641 | 3 | Drive control PLA failure check bit on. |
| 4642 | 3 | Servo logic failure check bit on. |
| 4643 | 3 | Servo analog failure check bit on. |
| 4644 | 3 | File AMP saturation check bit on. |
| 4645 | 3 | Mach AMP saturation check bit on. |
| 4646 | 3 | Load check bit on and sequence error bit not on. |
| 4647 | 3 | Not ready due to reset check bit on. |
| 464B | 3 | Tension check and sequence error bits on. |
| 464C | 3 | Load check and sequence check bits on. |
| 464D | 3 | Sequence error bit on without tension check bit or load check bit on. This condition indicates a false error. |
| 4651 | 3 | Start velocity check. |
| 4652 | 3 | End velocity check. |
| 4653 | 3 | PEID velocity check. |
| 4654 | 3 | Drive response check is on. |
| 4655 | 3 | Drive control parity check. |
| 4656 | 3 | Gap control check is on. |
| 4657 | 3 | Selected Alert is on and a motion error is not indicated in the sense bytes. The sense bits that were checked are shown in error numbers 37–56. |
| 46F0 | 3 | Selected Alert when not expected. |
| 46F1 | 3 | Check end status received. |
| 46F2 | 3 | Bus-in parity error. |
| 46F7 | 3 | End status 10-second timeout. |
| 46F8 | 3 | Control line timeout or selection error. |
| 46F9 | 3 | Unexpected adapter error. |
| 4701 | 2 | Unexpected machine check. |
| 4704 | 1 | Unexpected I/O interruption. |
| 4706 | 1 | Interruption always active. |
| 4708 | 3 | Open adapter failure. |
| 4709 | 1 | CHIO machine check. |
| 470C | 2 | Solid I/O machine check. |
| 4711 | 3 | Control line timeout on data securing erase command. |
| 4712 | 3 | Control line timeout on test set ready operation. |
| 4713 | 3 | Control line timeout on FSB command. |
| 4714 | 3 | No check end on FSB command. |
| 4715 | 3 | Not capable not on after FSB. |
| 4716 | 3 | Not capable not off. |
| 4717 | 3 | Sense byte 2, bit 6 not reset by check reset. |
| 4718 | 3 | Control line timeout on FSP command. |
| 4719 | 3 | Selected Alert not set by FSF command. |
| 471A | 3 | Sense byte 2, bit 6 not on. |
| 471B | 3 | Sense byte 3, bit 5 not on. |
| 471C | 3 | Sense byte 3, bit 5 not reset by check reset. |
| 471D | 3 | Sense byte 6, bit 1 is on (PEID check). |
| 471E | 3 | Sense byte 6, bit 0 not on (write command). |
| 471F | 3 | Sense byte 6, bit 0 is on (write command). |
| 4721 | 3 | Write status not on after DSE command. |
| 4722 | 3 | Write status not reset by FSB command. |
| 4723 | 3 | Busy not on during DSE operation. |

| RREN | Format | Meaning |
|---|---|---|
| 4724 | 3 | Busy not off after DSE operation. |
| 4725 | 3 | BSB at load point did not cause selected alert. |
| 4726 | 3 | Control line timeout on BSB at load point. |
| 4727 | 3 | Data check set on erase gap. |
| 47A1 | 3 | Selected Alert on erase gap operation. |
| 47A2 | 3 | Selected Alert and sense byte 12, bits 2 & 3 off. |
| 47A3 | 3 | Selected Alert and sense byte 12, bits 2 & 3 not = 00. |
| 47F0 | 3 | Selected Alert when not expected. |
| 47F1 | 3 | Check end status received. |
| 47F2 | 3 | Bus-in parity error. |
| 47F7 | 3 | End status 10-second timeout. |
| 47F8 | 3 | Control line timeout or selection error. |
| 47F9 | 3 | Unexpected adapter error. |
| 4801 | 2 | Unexpected machine check. |
| 4804 | 1 | Unexpected I/O interruption. |
| 4806 | 1 | Interruption always active. |
| 4808 | 3 | Open adapter failure. |
| 4809 | 1 | CHIO machine check. |
| 480C | 2 | Solid I/O machine check. |
| 4811 | 3 | 8-second control line timeout on write. |
| 4813 | 3 | Check end after a BSB command. |
| 4814 | 3 | Status error on write 2. |
| 4816 | 3 | Status error on write 3. |
| 4818 | 3 | Status error on write 4. |
| 481A | 3 | Status error on write 5. |
| 481B | 3 | 8-second control line timeout on read command. |
| 481C | 3 | Write sense bit is up on a read operation. |
| 481D | 3 | No data check on check end on read operation. |
| 481E | 3 | Data check on read operation. |
| 481F | 3 | 10-second ending status timeout on read command. |
| 4820 | 3 | Check end after a write command and write bit in sense is not on. |
| 4821 | 3 | PEID check on a write command. |
| 4822 | 3 | Envelope check on a write command. |
| 4823 | 3 | MTE, data check, or start read check on write operation. |
| 4824 | 3 | Check end on write and sense byte 6 bits 2–4 = 0. |
| 4826 | 3 | Check end set but not data check. |
| 482E | 3 | 10-second ending status timeout write 1. |
| 48A1 | 3 | Selected Alert on write 1 (WRT/ERASE fail). |
| 48A2 | 3 | Selected Alert on BSB operation. |
| 48A6 | 3 | Selected Alert and read back fail on read operation. |
| 48A7 | 3 | Selected Alert and gap control check on write 1. |
| 48A8 | 3 | Selected Alert and read back fail on write 1. |
| 48A9 | 3 | Selected Alert on write 1. |
| 48AF | 3 | Selected Alert on read operation. |
| 48F0 | 3 | Selected Alert when not expected. |
| 48F1 | 3 | Check end status received. |
| 48F2 | 3 | Bus-in parity error. |
| 48F7 | 3 | End status 10-second timeout. |
| 48F8 | 3 | Control line timeout or selection error. |
| 48F9 | 3 | Unexpected adapter error. |

| RREN | Format | Meaning |
|---|---|---|
| 4901 | 2 | Unexpected machine check. |
| 4904 | 1 | Unexpected I/O interruption. |
| 4906 | 1 | Interruption always active. |
| 4908 | 3 | Open adapter failure. |
| 4909 | 1 | CHIO machine check. |
| 490C | 2 | Solid I/O machine check. |
| 4912 | 3 | Control line timeout on set long gap operation. |
| 4913 | 3 | Selected Alert after reset long gap. |
| 4915 | 3 | Long gap sense bit did not reset. |
| 4916 | 3 | Low-Speed sense bit not on. |
| 491B | 3 | Selected Alert on set long gap command. |
| 491C | 3 | Control line timeout on set long gap operation. |
| 4921 | 3 | Long gap sense bit did not turn on. |
| 492C | 3 | Selected Alert on read block command. |
| 492D | 3 | 8-second ending status timeout. |
| 4931 | 3 | Selected Alert on read block command. |
| 4933 | 3 | Check end after a read block command. |
| 4934 | 3 | Ending status timeout on read block command. |
| 4935 | 3 | Data compare error on last record read. Adapter status in message is replaced by expected and actual data. |
| 4936 | 3 | Long gap mode not reset by RLG command. |
| 4937 | 3 | Selected Alert on read command. |
| 4939 | 3 | Check end while trying to read the hex 33 record. |
| 493A | 3 | After reading 12 records, the tape was not in position to read the hex 33 record. Long gap mode did not reset. |
| 493B | 3 | 8-second ending status timeout. |
| 49F0 | 3 | Selected Alert when not expected. |
| 49F1 | 3 | Check end status received. |
| 49F2 | 3 | Bus-in parity error. |
| 49F7 | 3 | End status 10-second timeout. |
| 49F8 | 3 | Control line timeout or selection error. |
| 49F9 | 3 | Unexpected adapter error. |
| 4A01 | 2 | Unexpected machine check. |
| 4A04 | 1 | Unexpected I/O interruption. |
| 4A06 | 1 | Interruption always active. |
| 4A08 | 3 | Open adapter failure. |
| 4A09 | 1 | CHIO machine check. |
| 4A0C | 2 | Solid I/O machine check. |
| 4A11 | 3 | Low speed did not set. |
| 4A12 | 3 | Long gap did not reset. |
| 4A16 | 3 | Selected Alert after backspace block. |
| 4A17 | 3 | Selected Alert on backspace operation. Not at load point. |
| 4A19 | 3 | Check end on backspace block. |
| 4A23 | 3 | Selected Alert on read 1. |
| 4A27 | 3 | Check end after read 1. |
| 4A2B | 3 | Selected Alert on read 2. |
| 4A2D | 3 | Check end on read 2. |
| 4A33 | 4 | Read compare error on read 2. |
| 4A35 | 3 | Selected Alert on read 3. |
| 4A37 | 3 | Check end on read 3. |
| 4A39 | 4 | Read compare error on record 3. |
| 4AF0 | 3 | Selected Alert when not expected. |
| 4AF1 | 3 | Check end status received. |
| 4AF2 | 3 | Bus-in parity error. |
| 4AF7 | 3 | End status 10-second timeout. |
| 4AF8 | 3 | Control line timeout or selection error. |
| 4AF9 | 3 | Unexpected adapter error. |
| 4C01 | 2 | Unexpected machine check. |
| 4C04 | 1 | Unexpected I/O interruption. |
| 4C06 | 1 | Interruption always active. |
| 4C08 | 3 | Open adapter failure. |
| 4C09 | 1 | CHIO machine check. |
| 4C0C | 2 | Solid machine check. |
| 4C11 | 3 | Control line timeout on set high-speed operation. |
| 4C12 | 3 | Selected Alert on set high-speed command. |
| 4C13 | 3 | Ending status timeout on set high-speed command. |
| 4C14 | 3 | Busy status on after set high-speed command. |
| 4C15 | 3 | Low-speed status on after set high-speed command. |
| 4C16 | 3 | Positioning status after set high-speed command. |
| 4C17 | 3 | Sense byte 11 not equal to 00100XXX after set high-speed command. |
| 4C18 | 3 | Sense byte 12 not equal to XXXX01XX after set high-speed command. |
| 4C19 | 3 | OP Complete not reset by check reset. |
| 4C1A | 3 | Selected Alert on ERG in high-speed command. |
| 4C1B | 3 | Ending status timeout on ERG operation. |
| 4C1C | 3 | Sense byte 11 not equal to 10100XXX after erase gap command. |
| 4C1D | 3 | Sense byte 12 not equal to XXXX01XX after erase gap command. |
| 4C1E | 3 | Sense byte 11 not equal to 00100XXX after rewind command. |
| 4C1F | 3 | Low-speed status not on after set low-speed command. |
| 4C21 | 3 | Bus-in parity error on set high-speed operation. |
| 4CF0 | 3 | Selected Alert when not expected. |
| 4CF1 | 3 | Check end status received. |
| 4CF2 | 3 | Bus-in parity error. |
| 4CF7 | 3 | End status 10-second timeout. |
| 4CF8 | 3 | Control line timeout or selection error. |
| 4CF9 | 3 | Unexpected adapter error. |
| 4D01 | 2 | Unexpected machine error. |
| 4D04 | 1 | Unexpected I/O interruption. |
| 4D06 | 1 | Interruption always active. |
| 4D08 | 3 | Open adapter failure. |
| 4D09 | 1 | CHIO machine check. |
| 4D0C | 2 | Solid I/O machine check. |
| 4D11 | 3 | Selected Alert on first write command. |
| 4D12 | 3 | Check end on first write command. |
| 4D13 | 3 | Selected Alert reading record 1. |
| 4D14 | 3 | Check end on reading record 1. |
| 4D15 | 4 | Compare error in record 1. |
| 4D16 | 3 | Selected alert reading record 2. |
| 4D17 | 3 | Check end on reading record 2. |

| RREN | Format | Meaning |
|---|---|---|
| 4D18 | 4 | Compare error in record 2. |
| 4D19 | 3 | Selected Alert reading record 3. |
| 4D1A | 3 | Check end on reading record 3. |
| 4D1B | 4 | Compare error in record 3. |
| 4D1C | 3 | Selected Alert reading record 4. |
| 4D1D | 3 | Check end on reading record 4. |
| 4D1E | 4 | Compare error in record 4. |
| 4D1F | 3 | Selected Alert reading record 5. |
| 4D20 | 3 | Check end on reading record 5. |
| 4D21 | 4 | Compare error in record 5. |
| 4D22 | 3 | Selected Alert reading record 6. |
| 4D23 | 3 | Check end on reading record 6. |
| 4D24 | 4 | Compare error in record 6. |
| 4D25 | 3 | Selected Alert reading record 7. |
| 4D26 | 3 | Check end on reading record 7. |
| 4D27 | 4 | Compare error in record 7. |
| 4D28 | 3 | Selected Alert reading record 8. |
| 4D29 | 3 | Check end on reading record 8. |
| 4D30 | 4 | Compare error in record 10. |
| 4D3A | 4 | Compare error in record 8. |
| 4D3B | 3 | Selected Alert reading record 9. |
| 4D3C | 3 | Check end on reading record 9. |
| 4D3D | 4 | Compare error in record 9. |
| 4D3E | 3 | Selected Alert reading record 10. |
| 4D3F | 3 | Check end on reading record 10. |
| 4DF0 | 3 | Selected Alert when not expected. |
| 4DF1 | 3 | Check end status received. |
| 4DF2 | 3 | Bus-in parity error. |
| 4DF7 | 3 | End status 10-second timeout. |
| 4DF8 | 3 | Control line timeout or selection error. |
| 4DF9 | 3 | Unexpected adapter error. |
| 4E01 | 2 | Unexpected machine check. |
| 4E04 | 1 | Unexpected I/O interruption. |
| 4E06 | 1 | Interruption always active. |
| 4E08 | 3 | Open adapter failure. |
| 4E09 | 1 | CHIO machine check. |
| 4E0C | 2 | Solid I/O machine check. |
| 4E11 | 3 | Control line timeout on write tape mark (WTM) operation. |
| 4E12 | 3 | Ending status timeout on WTM command. |
| 4E13 | 3 | Check end with PEID CK or WTM command. |
| 4E14 | 3 | Check end with WTM CK on WTM command. |
| 4E15 | 3 | Check end with check byte 6, bit 0 off on WTM operation. |
| 4E16 | 3 | Check end with check byte 6, bit 0 on during WTM operation. |
| 4E18 | 3 | BSB over TM failed to set check end. |
| 4E19 | 3 | TM detected bit not on. |
| 4E1A | 3 | Check end not set by BSB command. |
| 4E1B | 3 | TM detected bit not on. |
| 4E1C | 3 | TM detected not reset by check reset. |
| 4E1D | 3 | Control line timeout on BSF command. |
| 4E1F | 3 | Op Complete not on after BSF command. |
| 4E21 | 3 | Busy and Op Complete on after BSF command. |

| RREN | Format | Meaning |
|---|---|---|
| 4E22 | 3 | Op Complete not reset by check reset. |
| 4E23 | 3 | No normal end and data check not set. |
| 4EA1 | 3 | Selected Alert during a write tape mark command. |
| 4EF0 | 3 | Selected Alert when not expected. |
| 4EF1 | 3 | Check end status received. |
| 4EF2 | 3 | Bus-in parity error. |
| 4EF7 | 3 | End status 10-second timeout. |
| 4EF8 | 3 | Control line timeout or selection error. |
| 4EF9 | 3 | Unexpected adapter error. |
| 4F01 | 2 | Unexpected machine check. |
| 4F04 | 1 | Unexpected I/O interruption. |
| 4F06 | 1 | Interruption always active. |
| 4F08 | 3 | Open adapter failure. |
| 4F09 | 1 | CHIO machine check. |
| 4F0C | 2 | Solid I/O machine check. |
| 4F11 | 3 | Check end received writing record 1. |
| 4F12 | 3 | Check end received—not a write problem. |
| 4F13 | 3 | No normal end while writing record 2. |
| 4F14 | 3 | No normal end while writing record 3. |
| 4F15 | 3 | No normal end while writing record 4. |
| 4F16 | 3 | No normal end while writing record 5. |
| 4FA1 | 3 | Selected Alert on a write operation—record 1. |
| 4FF0 | 3 | Selected Alert when not expected. |
| 4FF1 | 3 | Check end status received. |
| 4FF2 | 3 | Bus-in parity error. |
| 4FF7 | 3 | End status 10-second timeout |
| 4FF8 | 3 | Control line timeout or selection error. |
| 4FF9 | 3 | Unexpected adapter error |
| 5001 | 2 | Unexpected machine check. |
| 5004 | 1 | Unexpected I/O interruption. |
| 5006 | 1 | Interruption always active. |
| 5008 | 3 | Open adapter failure. |
| 5009 | 1 | CHIO machine check. |
| 500C | 2 | Solid I/O machine check. |
| 5011 | 3 | Unable to write tape. |
| 5012 | 3 | No normal end on read with correct count. |
| 5013 | 3 | No count error on read long. |
| 5014 | 3 | No count error on read long. |
| 5015 | 3 | Count error on read long with SLI bit on. |
| 5016 | 3 | Count error on read short with SLI bit on. |
| 50F0 | 3 | Selected Alert when not expected. |
| 50F1 | 3 | Check end status received. |
| 50F2 | 3 | Bus-in parity error. |
| 50F7 | 3 | End status 10-second timeout. |
| 50F8 | 3 | Control line timeout or selection error. |
| 50F9 | 3 | Unexpected adapter error. |
| 5201 | 2 | Unexpected machine check. |
| 5204 | 1 | Unexpected I/O interruption. |
| 5206 | 1 | Interruption always active. |
| 5208 | 3 | Open adapter failure. |

| RREN | Format | Meaning |
|---|---|---|
| 5209 | 1 | CHIO machine check. |
| 520C | 2 | Solid I/O machine check. |
| 5211 | 3 | Write errors—could not write tape. |
| 5212 | 3 | Check end not on after BSB operation. |
| 5213 | 3 | TM detected not set after BSB operation. |
| 5214 | 3 | Check end not set on read. |
| 5215 | 3 | TM detected not set after read operation. |
| 5216 | 3 | Normal end off and data check off. |
| 52A1 | 3 | Selected Alert on write |
| 52F0 | 3 | Selected Alert when not expected. |
| 52F1 | 3 | Check end status received. |
| 52F2 | 3 | Bus-in parity error. |
| 52F7 | 3 | End status 10-second timeout. |
| 52F8 | 3 | Control line timeout or selection error. |
| 52F9 | 3 | Unexpected adapter error. |
| 5301 | 2 | Unexpected machine check. |
| 5304 | 1 | Unexpected I/O interruption. |
| 5306 | 1 | Interruption always active. |
| 5308 | 3 | Open adapter failure. |
| 5309 | 1 | CHIO machine check. |
| 530C | 2 | Solid I/O machine check. |
| 5311 | 3 | Unable to write pattern 1 after 5 retries. |
| 5312 | 3 | Unable to write pattern 2 after 5 retries. |
| 5313 | 3 | Unable to write pattern 3 after 5 retries. |
| 5314 | 3 | Unable to write pattern 4 after 5 retries. |
| 5315 | 3 | Unable to write pattern 5 after 5 retries. |
| 5316 | 3 | Status error reading record 1. |
| 5317 | 4 | Compare error record 1. |
| 5318 | 3 | Status error reading record 2. |
| 5319 | 4 | Compare error record 2. |
| 531A | 3 | Status error reading record 3. |
| 531B | 4 | Compare error record 3. |
| 531C | 3 | Status error reading record 4. |
| 531D | 4 | Compare error record 4. |
| 531E | 3 | Status error reading record 5. |
| 531F | 4 | Compare error record 5. |
| 53A1 | 3 | Selected Alert reading record 1. |
| 53F0 | 3 | Selected Alert when not expected. |
| 53F1 | 3 | Check end status received. |
| 53F2 | 3 | Bus-in parity error. |
| 53F7 | 3 | End status 10-second timeout. |
| 53F8 | 3 | Control line timeout or selection error. |
| 53F9 | 3 | Unexpected adapter error. |
| 5401 | 2 | Unexpected machine check. |
| 5404 | 1 | Unexpected I/O interruption. |
| 5406 | 1 | Interruption always active. |
| 5408 | 3 | Open adapter failure. |
| 5409 | 1 | CHIO machine check. |
| 540C | 2 | Solid I/O machine check. |
| 5416 | 3 | Status error on record 1 read. |
| 5417 | 3 | Read data compare error record 1. |
| 5418 | 3 | Status error on record 2 read. |
| 5419 | 4 | Read data compare error record 2. |
| 541A | 3 | Status error on record 3 read. |
| 541B | 4 | Read data compare error record 3. |
| 541C | 3 | Status error on record 4 read. |
| 541D | 4 | Read data compare error record 4. |
| 541E | 3 | Status error on record 5 read. |
| 541F | 4 | Read data compare error record 5. |
| 54A1 | 3 | Selected Alert on read record 1. |
| 54F0 | 3 | Selected Alert when not expected. |
| 54F1 | 3 | Check end status received. |
| 54F2 | 3 | Bus-in parity error. |
| 54F7 | 3 | End status 10-second timeout. |
| 54F8 | 3 | Control line timeout or selection error. |
| 54F9 | 3 | Unexpected adapter error. |
| 5501 | 2 | Unexpected machine check. |
| 5504 | 1 | Unexpected I/O interruption. |
| 5506 | 1 | Interruption always active. |
| 5508 | 3 | Open adapter failure. |
| 5509 | 1 | CHIO machine check. |
| 550C | 2 | Solid I/O machine check. |
| 5511 | 3 | Could not write tape. Tried five times. |
| 5512 | 3 | No normal end received after read due to read error or runaway tape. Either a write/read problem or magnetized head or cleaner blade. |
| 5513 | 4 | Data compare error on read. Possible magnetized head or cleaner blade. |
| 55A1 | 3 | Selected Alert while writing. |
| 55F0 | 3 | Selected Alert when not expected. |
| 55F1 | 3 | Check end status received. |
| 55F2 | 3 | Bus-in parity error. |
| 55F7 | 3 | End status 10-second timeout. |
| 55F8 | 3 | Control line timeout or selection error. |
| 55F9 | 3 | Unexpected adapter error. |
| 5601 | 2 | Unexpected machine check. |
| 5604 | 1 | Unexpected I/O interruption. |
| 5606 | 1 | Interruption always active. |
| 5608 | 3 | Open adapter failure. |
| 5609 | 1 | CHIO machine check. |
| 560C | 2 | Solid I/O machine check. |
| 5613 | 3 | Data record not erased. |
| 5614 | 3 | TM detected not set on FSB command. |
| 56A3 | 3 | Selected Alert or tape runaway on PSB command. |
| 56A4 | 3 | Selected Alert on write operation. |
| 56F0 | 3 | Selected Alert when not expected. |
| 56F1 | 3 | Check end status received. |
| 56F2 | 3 | Bus-in parity error. |
| 56F7 | 3 | End status 10-second timeout. |
| 56F8 | 3 | Control line timeout or selection error. |
| 56F9 | 3 | Unexpected adapter error. |

*TA243 Special Requirement Test Messages*

The following table lists, for each routine, the error numbers and their meaning for the special requirement tests. For test message formats, see TA231.

| RREN | Format | Meaning |
|---|---|---|
| 5A01 | 2 | Unexpected machine check. |
| 5A04 | 1 | Unexpected I/O interruption. |
| 5A06 | 1 | Interruption always active. |
| 5A08 | 3 | Open adapter failure. |
| 5A09 | 1 | CHIO machine check. |
| 5A0C | 2 | Solid I/O machine check. |
| 5A11 | 3 | Not ready, not at BOT, or not file protected. |
| 5A12 | 3 | Check end not set by FSB over TM. |
| 5A13 | 3 | Tape mark not detected. |
| 5A14 | 3 | Check end not reset by check reset. |
| 5A15 | 3 | Normal end not set by FSB operation. |
| 5A16 | 3 | Data check not set. |
| 5A21 | 3 | Test pattern delimiter not found by FSB. |
| 5A22 | 3 | Test pattern delimiter not found by BSB. |
| 5A23 | 3 | Test pattern delimiter not found by FSB. |
| 5A24 | 3 | No check end on reading BOR test record. |
| 5A25 | 3 | Start data check not set. |
| 5A26 | 3 | Data check not set. |
| 5A27 | 3 | Start read check not reset. |
| 5A28 | 3 | No normal end on FSB. |
| 5A29 | 3 | No normal end on BSB. |
| 5A2A | 3 | No normal end, no CK end or no TM DET on BSB. |
| 5A2B | 3 | No normal end on FSB. |
| 5A2C | 3 | No normal end on FSB. |
| 5A31 | 3 | Test pattern delimiter not found by FSB. |
| 5A32 | 3 | Pointers on for test record failure. |
| 5A33 | 3 | Check end on with no pointers. |
| 5A41 | 3 | IBG detect incorrect on FSB. |
| 5A42 | 3 | IBG detect incorrect on BSB. |
| 5A43 | 3 | No normal end on FSB. |
| 5A44 | 3 | MTE and crease not reset by check reset. |
| 5A51 | 3 | Check end not set by FSB over TM. |
| 5A52 | 3 | Tape mark not detected. |
| 5A53 | 3 | No check end on reading creased record. |
| 5A54 | 3 | MTE not set by reading creased record. |
| 5A55 | 3 | Crease bit not set by reading creased record. |
| 5A56 | 3 | Tape position is questionable. |
| 5A57 | 3 | TM DET not on reading creased record. |
| 5A58 | 3 | TM DET not on after BSB on creased record. |
| 5A59 | 3 | TM DET not on after FSB on creased record. |
| 5A5A | 3 | Crease with no pointers. |
| 5A5B | 3 | Start read check not reset. |
| 5A5C | 3 | Write command sense after read command. |
| 5A5D | 3 | Pointer P not set by creased record. |
| 5A5E | 3 | Data check not set. |
| 5A71 | 3 | Test record delimiter not found by FSB. |
| 5A72 | 3 | No check end on record with 2 bad tracks. |
| 5A73 | 3 | No MTE on record with 2 bad tracks. |
| 5A81 | 3 | Test record delimiter not found by FSB. |
| 5A82 | 3 | No check end. |
| 5A83 | 3 | No end data check. |
| 5A84 | 3 | Data check not set. |
| 5AA1 | 3 | Check end not set by tape mark. |
| 5AA2 | 3 | Tape mark not detected. |
| 5AA3 | 3 | Selected Alert on 1-bit skew record. |
| 5AA4 | 3 | Check end on 1-bit skew record. |
| 5AA5 | 3 | Skew check on 1-bit skew record. |
| 5AA6 | 3 | Data check not set. |
| 5AA7 | 3 | Data check not set. |
| 5AA8 | 3 | No check end on 3-bit skew record. |
| 5AA9 | 3 | No skew error on 3-bit skew record. |
| 5AF0 | 3 | Selected alert when not expected. |
| 5AF1 | 3 | Check end status received. |
| 5AF2 | 3 | Bus-in partity error. |
| 5AF7 | 3 | End status 10-second timeout. |
| 5AF8 | 3 | Control line timeout or selection error. |
| 5AF9 | 3 | Unexpected adapter error. |
| 5B01 | 2 | Unexpected machine check. |
| 5B04 | 1 | Unexpected I/O interruption. |
| 5B06 | 1 | Interruption always active. |
| 5B08 | 3 | Open adapter failure. |
| 5B09 | 1 | CHIO machine check. |
| 5B0C | 2 | Solid I/O machine check. |
| 5B11 | 3 | Test record delimiter not found by FSB. |
| 5B12 | 3 | Read fail pattern 1. |
| 5B13 | 4 | Data compare error pattern 1. |
| 5B14 | 3 | Read fail pattern 2. |
| 5B15 | 4 | Data compare error pattern 2. |
| 5B16 | 3 | Read fail pattern 3. |
| 5B17 | 4 | Data compare error pattern 3. |
| 5B18 | 3 | Read fail pattern 4. |
| 5B19 | 4 | Data compare error pattern 4. |
| 5B1A | 3 | Read fail pattern 5. |
| 5B1B | 4 | Data compare error pattern 5. |
| 5B1C | 3 | Read fail pattern 6. |
| 5B1D | 4 | Data compare error pattern 6. |
| 5B1E | 3 | Read fail pattern 7. |
| 5B1F | 4 | Data compare error pattern 7. |
| 5B21 | 3 | Read fail pattern 8. |
| 5B22 | 4 | Data compare error pattern 8. |
| 5B23 | 3 | Read fail pattern 9. |
| 5B24 | 4 | Data compare error pattern 9. |
| 5B25 | 3 | Read fail pattern 10. |
| 5B26 | 4 | Data compare error pattern 10. |
| 5B27 | 3 | Read fail pattern 11. |
| 5B28 | 4 | Data compare error pattern 11. |
| 5B29 | 3 | Read fail pattern 12. |
| 5B2A | 4 | Data compare error pattern 12. |
| 5B2B | 3 | Read fail pattern 13. |
| 5B2C | 4 | Data compare error pattern 13. |
| 5B2D | 3 | Read fail pattern 14. |

| RREN | Format | Meaning |
|---|---|---|
| 5B2E | 4 | Data compare error pattern 14. |
| 5B31 | 3 | Test pattern tape delimiter not found. |
| 5B32 | 3 | No select alert on write to protected tape. |
| 5B33 | 3 | Write enable error. |
| 5B34 | 3 | Write enable error did not reset. |
| 5B35 | 3 | Timeout with no EOT or check end. |
| 5B36 | 3 | Control line timeout on rewind unload. |
| 5B37 | 3 | Ending status timeout on rewind unload. |
| 5B38 | 3 | EOT status on early. |
| 5B39 | 3 | EOT status did not go off. |
| 5B3A | 3 | Busy not on during rewind unload. |
| 5B3B | 3 | Ending status timeout on rewind unload. |
| 5B3C | 3 | Busy did not drop after Op Complete. |
| 5B3D | 3 | Op Complete not reset by check reset. |
| 5BF0 | 3 | Select alert when not expected. |
| 5BF1 | 3 | Check end status received. |
| 5BF2 | 3 | Bus-in partity error. |
| 5BF7 | 3 | End status 10-second timeout. |
| 5BF8 | 3 | Control line timeout or selection error. |
| 5BF9 | 3 | Unexpected adapter error. |
| 6001 | 2 | Unexpected machine check. |
| 6004 | 1 | Unexpected I/O interruption. |
| 6006 | 1 | Interruption always active. |
| 6008 | 3 | Open adapter failure. |
| 6009 | 1 | CHIO machine check. |
| 600C | 2 | Solid I/O machine check. |
| 6011 | 3 | No normal end on write 1 at low speed. |
| 6012 | 3 | No normal end on write 2 at low speed. |
| 6013 | 3 | No normal end on write 3 at low speed. |
| 6014 | 3 | No normal end on write 4 at low speed. |
| 6015 | 3 | No normal end on write 5 at low speed. |
| 6016 | 3 | No normal end on write 6 at low speed. |
| 6017 | 3 | No normal end on write 7 at low speed. |
| 6018 | 3 | No normal end on write 8 at low speed. |
| 6019 | 3 | No normal end on write 9 at low speed. |
| 601A | 3 | No normal end on write 10 at low speed. |
| 601B | 3 | No normal end on write 11 at low speed. |
| 601C | 3 | No normal end on write 12 at low speed. |
| 601D | 3 | No normal end on write 13 at low speed. |
| 601E | 3 | No normal end on write 14 at low speed. |
| 6021 | 3 | No normal end on write 1 at high speed. |
| 6022 | 3 | No normal end on write 2 at high speed. |
| 6023 | 3 | No normal end on write 3 at high speed. |
| 6024 | 3 | No normal end on write 4 at high speed. |
| 6025 | 3 | No normal end on write 5 at high speed. |
| 6026 | 3 | No normal end on write 6 at high speed. |
| 6027 | 3 | No normal end on write 7 at high speed. |
| 6028 | 3 | No normal end on write 8 at high speed. |
| 6029 | 3 | No normal end on write 9 at high speed. |
| 602A | 3 | No normal end on write 10 at high speed. |
| 602B | 3 | No normal end on write 11 at high speed. |
| 602C | 3 | No normal end on write 12 at high speed. |
| 602D | 3 | No normal end on write 13 at high speed. |
| 602E | 3 | No normal end on write 14 at high speed. |
| 60F0 | 3 | Selected Alert when not expected. |
| 60F1 | 3 | Check end status received. |
| 60F2 | 3 | Bus-in parity error. |
| 60F7 | 3 | End status 10-second timeout. |
| 60F8 | 3 | Control line timeout or selection error. |
| 60F9 | 3 | Unexpected adapter error. |
| 6101 | 2 | Unexpected machine check. |
| 6104 | 1 | Unexpected I/O interruption. |
| 6106 | 1 | Interruption always active. |
| 6108 | 3 | Open adapter failure. |
| 6109 | 1 | CHIO machine check. |
| 610C | 2 | Solid I/O machine check. |
| 6111 | 3 | No normal end after read record 1. |
| 6112 | 3 | No normal end after read record 2. |
| 6113 | 3 | No normal end after read record 3. |
| 6114 | 3 | No normal end after read record 4. |
| 6115 | 3 | No normal end after read record 5. |
| 6116 | 3 | No normal end after read record 6. |
| 6117 | 3 | No normal end after read record 7. |
| 6118 | 3 | No normal end after read record 8. |
| 6119 | 3 | No normal end after read record 9. |
| 611A | 3 | No normal end after read record 10. |
| 611B | 3 | No normal end after read record 11. |
| 611C | 3 | No normal end after read record 12. |
| 611D | 3 | No normal end after read record 13. |
| 611E | 3 | No normal end after read record 14. |
| 6121 | 3 | No normal end after read record 15. |
| 6122 | 3 | No normal end after read record 16. |
| 6123 | 3 | No normal end after read record 17. |
| 6124 | 3 | No normal end after read record 18. |
| 6125 | 3 | No normal end after read record 19. |
| 6126 | 3 | No normal end after read record 20. |
| 6127 | 3 | No normal end after read record 21. |
| 6128 | 3 | No normal end after read record 22. |
| 6129 | 3 | No normal end after read record 23. |
| 612A | 3 | No normal end after read record 24. |
| 612B | 3 | No normal end after read record 25. |
| 612C | 3 | No normal end after read record 26. |
| 612D | 3 | No normal end after read record 27. |
| 612E | 3 | No normal end after read record 28. |
| 6151 | 4 | Data compare error on record 1. |
| 6152 | 4 | Data compare error on record 2. |
| 6153 | 4 | Data compare error on record 3. |
| 6154 | 4 | Data compare error on record 4. |
| 6155 | 4 | Data compare error on record 5. |
| 6156 | 4 | Data compare error on record 6. |
| 6157 | 4 | Data compare error on record 7. |
| 6158 | 4 | Data compare error on record 8. |
| 6159 | 4 | Data compare error on record 9. |
| 615A | 4 | Data compare error on record 10. |

| RREN | Format | Meaning |
|---|---|---|
| 615B | 4 | Data compare error on record 11. |
| 615C | 4 | Data compare error on record 12. |
| 615D | 4 | Data compare error on record 13. |
| 615E | 4 | Data compare error on record 14. |
| 6161 | 4 | Data compare error on record 15. |
| 6162 | 4 | Data compare error on record 16. |
| 6163 | 4 | Data compare error on record 17. |
| 6164 | 4 | Data compare error on record 18. |
| 6165 | 4 | Data compare error on record 19. |
| 6166 | 4 | Data compare error on record 20. |
| 6167 | 4 | Data compare error on record 21. |
| 6168 | 4 | Data compare error on record 22. |
| 6169 | 4 | Data compare error on record 23. |
| 616A | 4 | Data compare error on record 24. |
| 616B | 4 | Data compare error on record 25. |
| 616C | 4 | Data compare error on record 26. |
| 616D | 4 | Data compare error on record 27. |
| 616E | 4 | Data compare error on record 28. |
| 6191 | 3 | Tape mark detected not on after FSB operation over a tape mark. |
| 6192 | 3 | Tape mark detected not on after BSB operation over a tape mark. |
| 61F0 | 3 | Selected Alert when not expected. |
| 61F1 | 3 | Check end status received. |
| 61F2 | 3 | Bus-in partity error. |
| 61F7 | 3 | End status 10-second timeout. |
| 61F8 | 3 | Control line timeout or selection error. |
| 61F9 | 3 | Unexpected adapter error. |
| 6201 | 2 | Unexpected machine check. |
| 6204 | 1 | Unexpected I/O interruption. |
| 6206 | 1 | Interruption always active. |
| 6208 | 3 | Open adapter failure. |
| 6209 | 1 | CHIO machine cneck. |
| 620C | 2 | Solid I/O machine check. |
| 6211 | 3 | Normal routine completion. |
| 6301 | 2 | Unexpected machine check. |
| 6304 | 1 | Unexpected I/O interruption. |
| 6306 | 1 | Interruption always active. |
| 6308 | 3 | Open adapter failure. |
| 6309 | 1 | CHIO machine check. |
| 630C | 2 | Solid I/O machine check. |
| 6313 | 3 | Cover/reel latch interlock is open. |
| 6314 | 3 | Drive state is 'idle'. |
| 6315 | 3 | Drive state is 'take up slack'. |
| 6316 | 3 | Drive state is 'sample radius'. |
| 6317 | 3 | Drive state is 'enable servo'. |
| 6318 | 3 | Drive state is 'rewind FWD space'. |
| 6319 | 3 | Drive state is 'rewind'. |
| 631A | 3 | Drive state is 'rewind stop'. |
| 631B | 3 | Drive state is 'high-speed load point' and low speed is on. |
| 631C | 3 | Drive state is 'space to low-speed load point'. |
| 631D | 3 | Drive state is 'not low-speed load point' and the drive is in low-speed mode. |

| RREN | Format | Meaning |
|---|---|---|
| 631E | 3 | Drive state is 'low-speed load point' and busy. |
| 631F | 3 | Drive state is 'low-speed load point' and BOT is not on. |
| 6321 | 3 | Drive state is 'low-speed load point' and EOT is on. |
| 6322 | 3 | Drive state is 'low-speed load point' and Op Complete is not on. This error occurs if drive was reset after pressing LOAD REWIND or if LOAD REWIND is not pressed each time this routine is run. |
| 6323 | 3 | Drive state is 'low-speed load point' and positioning. |
| 6324 | 3 | Drive state is 'low-speed load point' and stoplock is not on. |
| 6325 | 3 | Drive state is 'low-speed load point' and READY light is not on. |
| 6326 | 3 | Drive state is 'low-speed load point' and all status appears correct. The READY light should be on; if not, check the READY light and circuit. |
| 6328 | 3 | Drive state is not 'high-speed load point' and the drive is in high-speed mode. |
| 6329 | 3 | Drive state is 'high-speed load point' and busy. |
| 632A | 3 | Drive state is 'high-speed load point' and BOT is not on. |
| 632B | 3 | Drive state is 'high-speed load point' and EOT is on. |
| 632C | 3 | Drive state is 'high-speed load point' and Op Complete is not on. This condition occurs if RESET is pressed after load rewind or if LOAD REWIND is not pressed each time this routine is run. |
| 632D | 3 | Drive state is 'high-speed load point' and positioning. |
| 632E | 3 | Drive state is 'high-speed load point' and stoplock is not on. |
| 632F | 3 | Drive state is 'high-speed load point' and READY light is not on. |
| 6331 | 3 | Drive state is 'high-speed load point' and the READY light should be on; if it is not, then check the READY light and circuit. |
| 6334 | 3 | Cover/reel latch interrupt is on. |
| 6335 | 3 | BOT/EOT LED failure. |
| 6336 | 3 | Tape present LED failure. |
| 6337 | 3 | Reel size LED failure. |
| 6338 | 3 | PA cable unseated. |
| 6339 | 3 | Idler tach failure. |
| 633A | 3 | Machine tach failure. |
| 633B | 3 | File tach failure. |
| 633C | 3 | Idler tach rotation check. |
| 6341 | 3 | Drive control PLA failure. |
| 6342 | 3 | Servo logic failure. |
| 6343 | 3 | Servo analog failure. |
| 6344 | 3 | File amp saturation. |
| 6345 | 3 | Machine amp saturation. |
| 6346 | 3 | Load check is on and sequence check is not on. This condition indicates a false error. |
| 6347 | 3 | Not ready due to reset. |
| 6348 | 3 | Selected Alert is on but there are not motion checks. |
| 634B | 3 | Tension check is on and drive state is rewind |
| 634C | 3 | Load check and sequence error are on. |
| 634D | 3 | Sequence check is on without tension or load check. This condition indicates a false error. |
| 634E | 3 | Tension check is on and drive state is not rewind. |

| RREN | Format | Meaning |
|---|---|---|
| 6351 | 3 | Drive control parity check. |
| 6352 | 3 | Drive response check is on. |
| 6361 | 4 | Write current failure. |
| 6362 | 4 | Erase current failure. |
| 63F0 | 3 | Selected Alert when not expected. |
| 63F1 | 3 | Check end status received. |
| 63F2 | 3 | Bus-in parity error. |
| 63F7 | 3 | End status 10-second timeout. |
| 63F8 | 3 | Control line timeout or selection error. |
| 63F9 | 3 | Unexpected adapter error. |
| 6401 | 3 | Unexpected machine check. |
| 6404 | 1 | Unexpected I/O interruption. |
| 6406 | 1 | Interruption always active. |
| 6408 | 3 | Open adapter failure. |
| 6409 | 1 | CHIO machine check. |
| 640C | 2 | Solid I/O machine check. |
| 6411 | 3 | Selected alert from write operation. |
| 6412 | 3 | Check end on write operation. |
| 6501 | 2 | Unexpected machine check. |
| 6504 | 1 | Unexpected I/O interruption. |
| 6506 | 1 | Interruption always active. |
| 6508 | 3 | Open adapter failure. |
| 6509 | 1 | CHIO machine check. |
| 650C | 2 | Solid I/O machine check. |
| 6511 | 3 | Selected Alert from write operation. |
| 6512 | 3 | Check end on write operation. |
| 6601 | 2 | Unexpected machine check. |
| 6604 | 1 | Unexpected I/O interruption. |
| 6606 | 1 | Interruption always active. |
| 6608 | 3 | Open adapter failure. |
| 6609 | 1 | CHIO machine check. |
| 660C | 2 | Solid I/O machine check. |
| 6611 | 3 | Selected Alert from read operation. |
| 6612 | 3 | Check end on read operation. |
| 6701 | 2 | Unexpected machine check. |
| 6704 | 1 | Unexpected I/O interruption. |
| 6706 | 1 | Interruption always active. |
| 6708 | 3 | Open adapter failure. |
| 6709 | 1 | CHIO machine check. |
| 670C | 2 | Solid I/O machine check. |
| 6711 | 3 | Positioning bit not turned on in 15 ms. |
| 6712 | 3 | Gap is too short—less than 1.4 cm (0.55 inch). |
| 6713 | 3 | Gap is too long—greater than 1.65 cm (0.65 inch). |
| 6714 | 3 | Bad status after read operation. |
| 6A01 | 2 | Unexpected machine check. |
| 6A04 | 1 | Unexpected I/O interruption. |
| 6A06 | 1 | Interruption always active. |
| 6A08 | 3 | Open adapter failure. |
| 6A09 | 1 | CHIO machine check. |
| 6A0C | 2 | Solid I/O machine check. |
| 6A11 | 3 | Not capable not on for first FSB. Check for proper skew tape. |
| 6AA2 | 3 | Tape motion was terminated by select alert condition other than tape running out. |
| 6AFF | 3 | Normal test end (tape ran out). |
| 6B01 | 2 | Unexpected machine check. |
| 6B04 | 1 | Unexpected I/O interruption. |
| 6B06 | 1 | Interruption always active. |
| 6B09 | 1 | CHIO machine check. |
| 6B0C | 2 | Solid I/O machine check. |
| 6B11 | 3 | Normal error number that is displayed with the sense information. |
| 6C01 | 2 | Unexpected machine check. |
| 6C04 | 1 | Unexpected I/O interruption. |
| 6C06 | 1 | Interruption always active. |
| 6C08 | 3 | Open adapter failure. |
| 6C09 | 1 | CHIO machine check. |
| 6C0C | 2 | Solid I/O machine check. |
| 6CFF | 3 | Normal message, not an error. (The symptom code is the last 2 bytes of the message; see Symptom Code table below.) |
| 6D01 | 2 | Unexpected machine check. |
| 6D04 | 1 | Unexpected I/O interruption. |
| 6D06 | 1 | Interruption always active. |
| 6D08 | 3 | Open adapter failure. |
| 6D09 | 1 | CHIO machine check. |
| 6D0C | 2 | Solid I/O machine check. |

**Symptom Codes (SCs) Generated by Routine 6C**

| Symptom Code | Meaning |
|---|---|
| AXXX | Adapter detected error |
| B001 | Sync out check |
| B002 | Sequence error |
| B004 | Control line tag bus parity error |
| B008 | Control line bus-out parity error |
| B010 | Formatter read failure |
| B020 | Formatter write or control line failure |
| B040 | Sense bus parity error |
| B080 | Clock failure |
| B120 | Check bus parity error |
| B140 | Bus-out gated parity error |
| B180 | Command register parity error |
| C008 | Power amp cable is unseated |
| C010 | Reel size LED failure |
| C020 | Tape present LED failure |
| C040 | BOT/EOT LED failure |
| C080 | Cover interrupt with cover closed |
| C081 | Cover interrupt with cover open |
| C110 | Idler tach rotation check |
| C120 | File tach failure |
| C140 | Machine tach failure |
| C180 | Idler tach failure |
| C208 | Machine amp saturation |
| C210 | File amp saturation |

| Symptom Code | Meaning |
|---|---|
| C220 | Servo analog failure |
| C240 | Servo logic failure |
| C280 | Drive control PLA failure |
| C380 | Sequence error and load check |
| C381 | Sequence error and tension check |
| C382 | Sequence check without tension or load check |
| C420 | PEID velocity check |
| C440 | End velocity check |
| C480 | Start velocity check |
| C520 | Gap control check |
| C540 | Drive control parity check |
| C580 | Drive response check |
| C640 | Not ready due to reset |
| C641 | Not ready due to reset and drive ready |
| C680 | Load check |
| D010 | Read back fail |
| D020 | Write-bus parity check |
| D040 | Write current fail |
| D080 | Erase current fail |
| D180 | Read-bus parity check |
| D220 | Selected Alert with BOT |
| D240 | Write enable error |
| D280 | Not capable on forward space fail |
| E001 | EOT on write |
| E020 | Tape mark detected |
| E040 | Not capable |
| E080 | Overrun |
| E202 | Not capable and write status |
| E204 | PEID check during write |
| E208 | Write tapemark error |
| E210 | MTE on write |
| E220 | ENV check on write |
| E240 | Start read check on write |
| E280 | End data check during write |
| E302 | Not capable and write status off |
| E304 | Creased |
| E308 | No pointer error on non-write |
| E310 | MTE on non-write |
| E320 | Skew error on non-write |
| E340 | Start read check on non-write |
| E380 | End data check on non-write |
| E404 | PEID check on loop write read (LWR) |
| E408 | WTM error on LWR |
| E410 | MTE on LWR |
| E420 | ENV CK on LWR |
| E440 | Start read check on LWR |
| E480 | End data check on LWR |

The following SCs could not be completely determined:

| Symptom Code | Meaning |
|---|---|
| FFF1 | Selected Alert but no select alert sense bits |
| FFF2 | Check end with data check on write |
| FFF3 | Check end with data check on LWR |
| FFF4 | Check end on but data check off |
| FFF5 | Check end with data check on |
| FFF6 | Invalid status and check bytes |
| FFFF | No Check End and no Selected Alert |

### *TA244 DPCX Online Exerciser Messages*

The following table lists, for each routine, the error numbers and their meanings for the DPCX online exerciser. See TA232 for error message formats.

| RREN | Meaning |
|---|---|
| 0101 | Failure during a rewind |
| 0121 | Failure during LWR—18 bytes, pattern = 0101010101010101 |
| 0122 | Failure during LWR—128 bytes, pattern = 2222222222222222 |
| 0123 | Failure during LWR—256 bytes, pattern = FFFFFFFFFFFFFFFF or pattern = 7F08AAFF5504FFAB |
| 0124 | Failure during LWR—2048 bytes, pattern = 7F08AAFF5504FFAB |
| 0125 | Failure during ERG—15 erase gaps |
| 01F0 | Failure on When Ready macro |
| 01F1 | Failure on Open Device macro—programming error |
| 01F2 | Failure on Open Device macro—hardware error |
| 01F3 | Failure on Close Device macro—programming error |
| 01F4 | Failure on Close Device macro—hardware error |
| 0201 | Failure during a rewind |
| 0203 | Failure during write—18 bytes, pattern = FFFFFFFFFFFFFFFF |
| 0204 | Failure during write—128 bytes, pattern = 7F08AAFF5504FFAB |
| 0205 | Failure during write—256 bytes, pattern = 7F08AAFF5504FFAB |
| 0206 | Failure during write tape mark |
| 0207 | Failure during read—18 bytes |
| 0208 | Failure during forward space block |
| 0209 | Failure during read—256 bytes |
| 020A | Failure during read (tape mark was being read) |
| 020B | Failure during backspace file |
| 020C | Failure during forward space file |
| 020D | Failure during read—128 bytes |
| 020E | Failure during backspace block |
| 020F | Failure while comparing data—128 bytes |
| 0210 | Failure while comparing data—256 bytes |
| 0211 | Failure during write—2048 bytes, pattern = 0123456789ABCDEF |
| 0212 | Failure during read—2048 bytes |
| 02F0 | Failure on When Ready macro |
| 02F1 | Failure on Open Device macro—programming error |
| 02F2 | Failure on Open Device macro—hardware error |
| 02F3 | Failure on Close Device macro—programming error |
| 02F4 | Failure on Close Device macro—hardware error |

## TA250 Failure Action Plans

This section provides an action plan for the type of error detected by the TA offline tests. The failing routine number in the test error message indicates the type of error detected (see TA230 for error message format). The types of errors and their action plans are:

| Failing Routine (RR) | Type of Failure | Go to Action Plan |
|---|---|---|
| 01, 02, 03, 09 | SCF/tape adapter | TA251 |
| 04-08, 11-15 | Tape adapter | TA252 |
| 40-43 | Tape adapter/tape drive | TA253 |
| 44-56 | Tape drive | TA254 |

| Other Test Error Messages | Type of Failure | Go to Action Plan |
|---|---|---|
| PA80 | Tape adapter failed to initiate a data transfer | TA251 |
| XXBC | SCF/tape adapter failure | TA251 |

Determine the type of error and go to the appropriate action plan. The action plan provides you with a list of possible failing FRUs to correct the type of failure.

**Caution: Turn power off when removing or exchanging cards or cables.**

### *TA251 SCF/Tape Adapter Failure Action Plan*

A failure was detected either in the SCF bus lines or the tape adapter circuitry associated with them. The operation that failed was not related to operations involving the tape drive. Proceed as follows:

1. Measure the board voltages. See TA440. If there are missing or out-of-tolerance voltages, either go to the PA MIM for an 8809 Model 1A or the 8809 START MAP for an 8809 Model 1B.
2. **Reseat tape adapter cards and the SCF card. See TA431, TA432, or TA433.**
3. Check SCF top card connectors.
4. Check card and board pins for bent or broken pins and connectors.
5. Exchange all possible cards that could cause the failure. For a list of cards related to the test error message, see TA255 (Routine 01, 02, 03, 09, XXBC, or PA80). Run tests after each exchange.
6. If the 8809 is a Model 1A, test all other adapters in the same SCF address group. Exchange any failing adapter.
7. **Check the board wiring and correct if necessary. See TA451, TA452, or TA453.**
8. If the error was 92BC, return to the ST action plan that sent you here, and continue with the next ST action plan step.
9. Request aid.

### *TA252 Tape Adapter Failure Action Plan*

A failure was detected in the tape adapter circuitry. The operation that failed was not related to operations involving the tape drive. Proceed as follows:

1. Measure the board voltages (see TA440). If there are missing or out-of-tolerance voltages, either go to the PA MIM for an 8809 Model 1A or to the 8809 START MAP for an 8809 Model 1B.
2. **Reseat tape adapter cards and top card connectors. Reseat SCF card and top card paddle connectors. Reseat cables from SCF card to 01A board (Model 1B only). See TA431, TA432, or TA433.**
3. **Model 1A only: Check and reseat paddle cards at Y1 and Z1 (adapter in 8101) or Y3 and Z3 (adapter in 8140).**
4. Check card and board pins for bent or broken pins and connectors.
5. Exchange all possible cards that could cause the failure. For a list of cards related to the test error message, see TA255 (Routines 04–08 and 11–15). Run tests after each exchange.
6. **Check the board wiring and correct if necessary. See TA451, TA452, or TA453.**
7. Request aid.

### *TA253 Tape Adapter/Tape Drive Failure Action Plan*

A failure was detected when the tape adapter initiated its first operations involving the tape drive. Proceed as follows:

1. Ensure that the tape drive is clean, has a known good reel of tape mounted, and the drive is ready. Correct if necessary and rerun tests.
2. **Reseat tape adapter cards and top card connectors. See TA431, TA432, or TA433.**
3. **Model 1A only: Check and reseat paddle cards at Y1 and Z1 (adapter in 8101) or Y3 and Z3 (adapter in 8140).**
4. **Model 1A only: Check the Bus and Tag cables for bent pins or loose connections. See TA111.**
5. Exchange all possible cards that could cause the failure. For a list of cards related to the test error message, see TA255 (Routines 40–43). Run tests after each exchange.
6. Check the board wiring and correct if necessary. **See TA451, TA452, or TA453.**
7. Go to TA254 (Tape Drive Action Plan) and perform that action plan.

### *TA254 Tape Drive Action Plan*

A failure was detected while running the device tests. Proceed as follows:

1. Ensure that the tape drive is clean, has a known good reel of tape mounted, and the drive is ready. Correct if necessary and rerun the tests.
2. Check the card list in TA255. If the routine number and error number (RREN) appear in the list, exchange the cards shown one at a time. Run tests after each exchange.
3. Go to the 8809 tape drive MAPs.

*TA255 Card Exchange Table*

| | Model 1A | | | | | | | | | Model 1B | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Adapter in 8101 Exchange in Order | | | Adapter in 8140 C2 Board Exchange in Order | | | Adapter in 8140 D2 Board Exchange in Order | | | Adapter in 8809 Exchange in Order | | |
| Error Pattern | 1st | 2nd | 3rd | 1st | 2nd | 3rd | 1st | 2nd | 3rd | 1st | 2nd | 3rd |
| PA80 | A2A2 | A2B2 | | C2A2 | C2G2 | | C2A2 | D2G2 | | SCF | A1D2 | |
| XXBC | A2A2 | A2B2 | A2C2 | C2A2 | C2G2 | C2H2 | C2A2 | D2G2 | D2H2 | SCF | A1D2 | A1E2 |
| PAXE 01XX | A2C2 | A2B2 | A2A2 | C2H2 | C2G2 | C2A2 | D2H2 | D2G2 | C2A2 | A1E2 | A1D2 | SCF |
| PAXE 02XX | A2C2 | A2B2 | A2A2 | C2H2 | C2G2 | C2A2 | D2H2 | D2G2 | C2A2 | A1E2 | A1D2 | SCF |
| PAXE 03XX | A2B2 | A2C2 | A2A2 | C2G2 | C2H2 | C2A2 | D2G2 | D2H2 | C2A2 | A1D2 | A1E2 | SCF |
| PAXE 04XX | A2B2 | A2C2 | A2D2 | C2G2 | C2H2 | C2J2 | D2G2 | D2H2 | D2J2 | A1D2 | A1E2 | |
| PAXE 05XX | A2B2 | A2C2 | | C2G2 | C2H2 | | D2G2 | D2H2 | | A1D2 | A1E2 | |
| PAXE 06XX | A2C2 | A2B2 | | C2H2 | C2G2 | | D2H2 | D2G2 | | A1E2 | A1D2 | |
| PAXE 07XX | A2C2 | A2B2 | | C2H2 | C2G2 | | D2H2 | D2G2 | | A1E2 | A1D2 | |
| PAXE 08XX | A2C2 | A2B2 | | C2H2 | C2G2 | | D2H2 | D2G2 | | A1E2 | A1D2 | |
| PAXE 09XX | A2B2 | A2A2 | A2C2 | C2G2 | C2A2 | C2H2 | D2G2 | C2A2 | D2H2 | A1D2 | SCF | A1E2 |
| PAXE 11XX | A2B2 | A2A2 | | C2G2 | C2A2 | | D2G2 | C2A2 | | A1D2 | SCF | |
| PAXE 12XX | A2B2 | A2A2 | | C2G2 | C2A2 | | D2G2 | C2A2 | | A1D2 | SCF | |
| PAXE 13XX | A2B2 | A2A2 | | C2G2 | C2A2 | | D2G2 | C2A2 | | A1D2 | SCF | |
| PAXE 14XX | A2C2 | A2B2 | | C2H2 | C2G2 | | D2H2 | D2G2 | | A1E2 | A1D2 | |
| PAXE 15XX | A2C2 | A2B2 | | C2H2 | C2G2 | | D2H2 | D2G2 | | A1E2 | A1D2 | |
| PAXE 40XX | A2C2 | A2D2 | A2B2 | C2H2 | C2J2 | C2G2 | D2H2 | D2J2 | D2G2 | A1E2 | A1D2 | |
| PAXE 41XX | A2C2 | A2D2 | A2B2 | C2H2 | C2J2 | C2G2 | D2H2 | D2J2 | D2G2 | A1E2 | A1D2 | |
| PAXE 42XX | A2D2 | A2C2 | A2B2 | C2J2 | C2H2 | C2G2 | D2J2 | D2H2 | D2G2 | A1E2 | A1D2 | |
| PAXE 43XX | A2D2 | A2C2 | A2B2 | C2J2 | C2H2 | C2G2 | D2J2 | D2H2 | D2G2 | A1E2 | A1D2 | |
| PAXE 4420 | A2C2 | A2D2 | A2B2 | C2H2 | C2J2 | C2G2 | D2H2 | D2J2 | D2G2 | A1E2 | A1D2 | |
| PAXE 4701 | A2D2 | A2C2 | A2B2 | C2J2 | C2H2 | C2G2 | D2J2 | D2H2 | D2G2 | A1E2 | A1D2 | |
| PAXE 4725 | A2D2 | A2C2 | A2B2 | C2J2 | C2H2 | C2G2 | D2J2 | D2H2 | D2G2 | A1E2 | A1D2 | |
| PAXE 481A | A2B2 | A2C2 | | C2G2 | C2H2 | | D2G2 | D2H2 | | A2D2 | A1E2 | |
| PAXE 4935 | A2B2 | A2C2 | A2A2 | C2G2 | C2H2 | C2A2 | D2G2 | D2H2 | C2A2 | A1D2 | A1E2 | SCF |
| PAXE 49F9 | A2C2 | A2B2 | A2A2 | C2H2 | C2G2 | C2A2 | D2H2 | D2G2 | C2A2 | A1E2 | A1D2 | SCF |
| PAXE 4A33 | A2B2 | A2C2 | | C2G2 | C2H2 | | D2G2 | D2H2 | | A1D2 | A1E2 | |
| PAXE 4AF8 | A2B2 | A2C2 | | C2G2 | C2H2 | | D2G2 | D2H2 | | A1D2 | A1E2 | |
| PAXE 5319 | A2B2 | A2C2 | | C2G2 | C2H2 | | D2G2 | D2H2 | | A1D2 | A1E2 | |
| PAXE 5512 | A2C2 | A2B2 | | C2H2 | C2G2 | | D2H2 | D2G2 | | A1E2 | A1D2 | |

* The Local/Remote power switch should be in Local, and the 8809 should be powered off when exchanging cards.

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## TA300 Intermittent Failure Repair Strategy

### TA310 Adapter-Unique Intermittent Repair Strategy

System-detected or customer-reported failures are considered intermittent if they cannot be readily reproduced by the DLS tests (see 8809 Maintenance Manual for definition) or other maintenance manual-instructed action by the service representative.

Looping the tests provides the most effective method of detection for an intermittent failure. Should a failure not occur, then you must use the error log.

#### *TA311 Looping with MAP Interaction to Determine Intermittent Failures*

The DLS tests may be looped using the MAP during basic checkout (MAP selection A). Each complete test sequence takes 7 minutes, and, if there are no errors on the first pass, the tests loop continuously. The MD displays 'PAF0 TEST LOOPING' until the test either detects an error, or you terminate the test by entering 'F' at the MD.

If an error is detected while looping, the MAP directs repairs of the failure in the same manner as a solid failure. Once you perform a repair action, the MAP loops the tests to verify the repair.

If the tests do not detect an error while looping, you should terminate the tests. The MAP directs you to run either ELDA (DPPX systems) or SYSLERR (DPCX systems) and obtain the symptom code for the customer-reported failure. You then reenter the MAP at Entry Point D (Test Symptom Code) and are directed to the appropriate FRU exchange list.

#### *TA312 Using the System Error Log to Determine Intermittent Failures*

To obtain this log for DPPX systems, you use the ELDA utility, and to obtain it for systems operating under DPCX, you use the SYSLERR utility and obtain a symptom code using the sense data collected at the time of failure.

In general, the procedure is to replace the highest probability FRU indexed by the symptom code. Once the FRU has been exchanged, run the DLS tests or the DPCX Online Exerciser. Assuming no detected failures, record the FRU in the FRU Exchange History Table, which is located in the 8809 Maintenance Manual MAP reference pages, and return the machine to the customer.

On subsequent calls for the same failure, exchange the next lower probability FRUs, one at a time, using the above procedure. When the list of FRUs is exhausted and the intermittent failure persists, go to TA250 and perform all action plans.

The action plans direct you to some low probability FRUs of a more general nature, but still related to the failure being diagnosed. If the failure still persists, you are directed to collect pertinent information before calling the support level.

#### *TA313 Using the Free-Lance Utility to Determine Intermittent Failures*

The TA test can be looped by using the Free-Lance Utility contained on the MD diskettes. A complete test sequence occurs in 7 minutes. To invoke the TA tests, at the 80BC message enter PADAB, at the 81BC message enter 11B (see TA211). The test loops continuously until either detecting an error or you terminate the test by entering an 'F' at the MD.

If an error occurs while looping, the MD displays the test error message (see TA231). Record this message and use the Failure Action Plans section (TA250) to isolate and repair the failure. Once a repair action has been taken, loop the test for at least 15 minutes to verify the repair.

### TA320 Error-Log Information Needed for the Tape Adapter

Error-log information may be obtained in several ways, depending upon which system the customer uses and what type of information you want. The following lists the different methods of obtaining the information and briefly describes the information.

#### *TA321 DPPX*

- DISPLAY.ERRLOG Command—Outputs either all or selected records in the error log, depending upon the options selected. The output is in detailed form.
- ELSA Utility—Outputs either all or selected records in the error log, depending upon the options selected. The output is in summary form.
- ELDA Utility—Outputs all records pertaining to the tape drive and the tape adapter. The records are in summary form and the user can select the type of information to be summarized. The output also includes the symptom code (SC).

#### *TA322 DPCX*

- SYSLERR Utility—Outputs all or selected records in the error log (called the Condition/Incident Log), depending upon the options selected. The output is in detailed form. In addition, if the record is a Type-5 tape unit or tape adapter record the utility generates the outputs the symptom code for the error. See TA332 for Type-5 record format.
- SYSLTSD Utility—Outputs the summary of all temporary errors occurring in the tape subsystem.

**Note:** *Chapter 2 contains the invocation procedures for each of these methods, as well as additional information about SYSLTSD and ELDA.*

## TA330 Error Log Formats and Meanings Used for the Tape Adapter

The format of the error log depends upon whether the customer is using DPPX or DPCX.

### *TA331 DPPX Error Log Formats and Meanings*

The following conditions generate an entry in the DPPX error log:

- Permanent errors. Figure TA331-2 shows the format of this record.
- Temporary errors. Temporary errors are not logged for each event but are counted by threshold counters in the program. See Figure TA334-1 for the Tape Statistical Data (TSD) threshold counters. When a threshold counter reaches a predetermined value, the Error Record Indicator (ERI) bit turns on in the extended status, and the data is logged. The record format is the same as for permanent errors.
- A volume is mounted or dismounted. Figure TA331-1 shows the contents of the entry.

#### DPPX Error Log Display

The DISPLAY.ERRLOG command prints the detailed error log data. Figure TA331-1 shows the Mount/Dismount display, and Figure TA331-2 shows the Error Record display.

The ELSA utility prints summary error data. Error data may also be printed using the Error Log Data Analysis (ELDA) report (see Chapter 2, CP730).

```
CLASS    04    SUBCLASS   02    OPTION     XX
DATE   YY.DDD     TIME   HH:MM:SS
PA  XX    SCA XXXX    DT    T
VOLID  XXXXXX           M/D  X
```

**Note:** *"X" indicates the field size in bytes, where two Xs equals one byte.*

**Figure TA331-1. DPPX Error Log Display for Mount/Dismount Records**

```
CLASS    05    SUBCLASS   01    OPTION     XX
DATE   YY.DDD     TIME   HH:MM:SS
PA  XX    SCA XXXX    DT    T
CRC  XX    COMPSTAT XX    ARC  XX
DATA  XXXXXXXX  RES  XXXX    CNT  XXXX
IOEP   XXXXXXXX  ADWA  XXXXXXXX
CA  XX    CPR  XX  FRWA  XXXXXXXX
RES  XXXXXXXX
BCLE   XX  XX  XXXX  XXXXXXXX
EXTENDED   DATA
D01  XXXX    D02  XXXX    D03  XXXX    D04  XXXX
D05  XXXX    D06  XXXX    D07  XXXX    D08  XXXX
D09  XXXX    D10  XXXX    D11  XXXX    D12  XXXX
D13  XXXX    D14  XXXX    D15  XXXX    D16  XXXX
D17  XXXX    D18  XXXX    D19  XXXX    D20  XXXX
D21  XXXX    D22  XXXX    D23  XXXX    D24  XXXX
D25  XXXX    D26  XXXX    D27  XXXX    D28  XXXX
D29  XXXX    D30  XXXX    D31  XXXX    D32  XXXX
D33  XXXX    D34  XXXX    D35  XXXX    D36  XXXX
D37  XXXX    D38  XXXX    D39  XXXX    D40  XXXX
D41  XXXX    D42  XXXX    D43  XXXX    D44  XXXX
D45  XXXX    D46  XXXX    D47  XXXX
```

**Note:** *"X" indicates the field size in bytes, where two Xs equals one byte.*

**Figure TA331-2. DPPX Error Log Display for Error Records (Format 1)**

#### Record Meaning

The following describes the meaning of the DPPX error log fields used to analyze tape hardware errors:

CLASS = 4 = Mount/dismount
5 = Hardware I/O error

SUBCLASS = 1 = Hardware I/O error record
2 = Mount/dismount record

DATE = YY.DDD = The year and Julian date of the log output

TIME = HH:MM:SS = The hour/minute/second of the log output

PA = XX = Tape adapter physical address
5E = Adapter in 8140 Model BXX
73 = Adapter in Model 1B tape drive
93 = Adapter in first 8101
A3 = Adapter in second 8101
B3 = Adapter in third 8101
C3 = Adapter in fourth 8101

SCA = XXXX = Indicates the tape drive address

DT = T = Tape device type

CRC = XX = Function Module Request Code (see TA333)

COMPSTAT = XX = Completion status (see TA333)

ARC = XX = Adapter Return Code (see TA333)

DATA = XXXXXXXX = Data address

RES = XXXX = Not used

CNT = XXXX = Byte count

IOEP = XXXXXXXX = I/O interrupt entry point

ADWA = XXXXXXXX = Adapter work area address

CA = XX = Channel address

CPR = XX = Channel pointer register

FRWA = XXXXXXXX = Function request work area

RES = XXXXXXXX = Not used

BCLE = 8 bytes = Buffer control list element
Byte 0 = Flag byte
Bits 0–2 = Not used
Bit 3 = Program request interrupt
Bits 4, 5 = Incorrect data length suppression
Bit 6 = Chain data
Bit 7 = Chain record
Byte 1 = Command byte (see TA333)
Bytes 2, 3 = Count = Number of bytes transmitted
Bytes 4–7 = Address or data

VOLID = XXXXXX = Volume ID

M/D = X = M/Mount
D/Dismount

EXTENDED DATA

D01, D02 = 4 bytes = Not used
D03 = XXXX = First byte = Extended completion status
Bit 0 = Not used
Bit 1 = Error record indicator
Bit 2 = Program request interrupt
Bit 3 = Not used
Bit 4 = Not used
Bit 5 = Preemptive request complete
Bit 6 = Not used
Bit 7 = Not used
= Second byte = Not used
D04 = XXXX = Error record displacement
D05, D06 = 4 bytes = BCLE address
D07 = XXXX = Residual count
D08 = XXXX = Not used
D09 = XXXX = DPPX/CAC control byte
D10, D11 = 4 bytes = Reserved
D12 = XXXX = Count (size of FCB build area)
D13, D14 = 4 bytes = Address of FCB build area
D15—D18 = 8 bytes = CAC work area
D19—D24 = 12 bytes = Reserved
D25—D36 = Tape Statistical Data (TSD) counters (see TA334)
D37 = XXXX = First byte = Tape sense byte 0 (see TA233)
Second byte = Tape sense byte 1 (see TA233)
D38 = XXXX = First byte = Tape sense byte 2 (see TA233)
Second byte = Tape sense byte 3 (see TA233)
D39 = XXXX = First byte = Tape sense byte 4 (see TA233)
Second byte = Tape sense byte 5 (see TA233)
D40 = XXXX = First byte = Tape sense byte 6 (see TA233)
Second byte = Tape sense byte 7 (see TA233)
D41 = XXXX = First byte = Tape sense byte 8 (see TA233)
Second byte = Tape sense byte 9 (see TA233)
D42 = XXXX = First byte = Tape sense byte 10 (see TA233)
Second byte = Tape sense byte 11 (see TA233)
D43 = XXXX = First byte = Tape sense byte 12 (see TA233)
Second byte = Tape sense byte 13 (see TA233)
D44 = XXXX = First byte = Tape sense byte 14 (see TA233)
Second byte = Tape sense byte 15 (see TA233)
D45 = XXXX = First byte = Adapter status extended (see TA233)
Second byte = Adapter status (see TA233)
D46 = XXXX = First byte = Device address
Second byte = PIO command (see TA333)
D47 = XXXX = First byte = Tag bus
Second byte = Bus Out

**Note:** *See* IBM 8809 Magnetic Tape Unit Description, *Form GA26—1659, for detailed explanation of D47 field.*

## *TA332 DPCX Condition/Incident Log Formats and Meanings*

### Temporary Errors

Temporary errors are not logged for each event but are counted by threshold counters in the program. When a threshold counter reaches a predetermined value, the error record indicator (ERI) bit turns on in the extended status, and the Tape Statistical Data (TSD) counters in processor storage save the data. When a TSD counter overflows or a tape is dismounted, a history file on disk storage (Data Set 24) is updated. The data is stored by Volume ID and Tape Unit LA. The history file has the ability to hold 80 volume entries and 4 tape unit entries. Refer to Chapter 2, CP853, for details.

### Permanent Errors

The 8100 enters selected system events into an error log (Condition/Incident Log), contained on the system-resident disk storage drive (see Figure TA332-1). An incident type and a sequence number identify each event. Sequence numbers are assigned in order of occurrence, sequentially from 1 to 4095. The log wraps around at 4095, starting over at 1, and any previous recordings are overwritten.

**Note:** *Some error log records may be lost after an 8100 power-off sequence if (1) the Control Operator did not perform a normal termination of system operations prior to power-off, or (2) you did not initalize the 8100 before power-off.*

Three types of error records are used by the tape adapter and tape drive:

- Type-2 records, associated with system check failures (Figure TA332-1).
- Type-4 records, associated with various system events such as system start, system abend, and system shutdown (Figure TA332-2).
- Type-5 records, associated with tape adapter and tape drive failures (Figure TA332-3).

The log typically can be used for intermittent failure analysis when the various tests do not detect a failure.

### Error Data Display, Temporary Errors

The SYSLTSD utility permits you to display or print the temporary error counters (tape statistical data or TSD) from the history file. See Chapter 2, CP853, for invocation procedures and allowable options. Supported devices are the same as for SYSLERR.

You can display the TSD counters in two different formats: detailed or summary. The detailed format shows all the counters sorted by tape unit LA and the major counters sorted by Volume ID and LA. The summary format shows the major counters summarized in percentages sorted by Volume ID and LA. Refer to Chapter 2, CP853, for details.

### Error Data Display, Permanent Records

The SYSLERR utility displays or prints permanent errors. See Chapter 2, CP830, for invocation procedures and allowable options.

During the SYSLERR processing of a Type-5 record, a call is made to a subroutine which generates a Symptom Code (SC) from the 8809 sense and status bytes, the tape adapter status bytes, and the Tag Bus Out. This symptom code displays in the D21 field of the record.

```
(1)                 (2)                 (3)     (4)     (5)
2-TYPE   1-REC      SEQ-XXXX            NA-XX   PA-XX   LA-XX
(6)                         (7)                 (8)
D21-XXXX XXXX               LVL-XX              C-FR-XX
(9)                         (10)                (11)
D22-XXXX XXXX               MC-XX               S-FR-XX
(12)                        (13)                (14)
D23-XXXX            D24-XXXX                    D25-XXXX
```

**Figure TA332-1. DPCX Type-2 System Check Record Display**

```
(1)                 (2)                 (3)
4-TYPE   1-REC      SEQ-XXXX            SYS-COND-XX
(4)      (5)        (6)        (7)      (8)
D01-XX   D02-XX     D03-XX     D04-XX   D05-XX
```

**Figure TA332-2. DPCX Type-4 System Condition Record Display**

```
(1)                 (2)                 (3)     (4)
5-TYPE   I-REC      SEQ-XXX             PA-XX   LA-XX
         (5)        (6)        (7)      (8)
         D1-XX      D2-XX      D3-XX    D4-XX
         (9)        (10)
         D5-XX      D6-XX      D7-XX    D8-XX

         D9-XXXXXX
         (11)
         D10-XXXX   D11-XXXX   D12-XXXX

         D13-XXXX   D14-XXXX   D15-XXXX
                               (12)
         D16-XXXX   D17-XXXX   D18-XXXX
         (13)       (14)       (15)
         D19-XXXX   D20-XXXX   D21-XXXX

         D22-XXXX   D23-XXXX   D24-XXXX

         D25-XXXX   D26-XXXX   D27-XXXX

         D28-XXXX   D29-XXXX   D30-XXXX
```

**Figure TA332-3. DPCX Type-5 Variable Data Record Display**

**Record Meaning**

2-TYPE = CIL record type 2 (see Figure CP840-2 in Chapter 2 for D21—D25 and LVL description)
4-TYPE = CIL record type 4 (see Figure CP840-4 in Chapter 2 for detailed description)
5-TYPE = CIL record type 5
SEQ = XXXX = A 4-digit decimal value from 0001 to 4095 that identifies the relative time when the record occurred.
NA = XX = Number of applications active when the error occurred
PA = XX = Tape adapter physical address
- 5E = Adapter in 8140 Model BXX
- 73 = Adapter in Model 1B tape drive
- 93 = Adapter in first 8101
- A3 = Adapter in second 8101
- B3 = Adapter in third 8101
- C3 = Adapter in fourth 8101

LA = XX = Tape drive logical address
- 04 = Tape drive unit 0
- 05 = Tape drive unit 1
- 06 = Tape drive unit 2
- 07 = Tape drive unit 3

C-FR = XX = Command byte (adapter operation) at time of error (see TA333)
MC = XX = System check code
- 1X = Program check
- 2X = Storage parity error
- 4X = I/O timeout
- 8X = I/O bus parity error

S-FR = XX = System Function Module Request code (see TA333)

EXTENDED DATA

D1 = XX = System Function Module Request code (see TA333)
D2 = XX = Command byte (adapter operation) at time of error (see TA333)
D3 = XX = Completion status (see TA333)
D4 = XX = Tape drive unit physical address
- 00 = Tape drive unit 0
- 01 = Tape drive unit 1
- 02 = Tape drive unit 2
- 03 = Tape drive unit 3

D5 = XX = Adapter Return Code (see TA333)
D6 = XX = Translated Adapter Return Code (see TA333)
D7 = XX = Not used (set to 00)
D8 = XX = Record type (FF = permanent error)
D9 = XXXXXX = Volume ID

D10 = XXXX = First byte = Tape sense byte 0 (see TA233)
Second byte = Tape sense byte 1 (see TA233)
D11 = XXXX = First byte = Tape sense byte 2 (see TA233)
Second byte = Tape sense byte 3 (see TA233)
D12 = XXXX = First byte = Tape sense byte 4 (see TA233)
Second byte = Tape sense byte 5 (see TA233)
D13 = XXXX = First byte = Tape sense byte 6 (see TA233)
Second byte = Tape sense byte 7 (see TA233)
D14 = XXXX = First byte = Tape sense byte 8 (see TA233)
Second byte = Tape sense byte 9 (see TA233)
D15 = XXXX = First byte = Tape sense byte 10 (see TA233)
Second byte = Tape sense byte 11 (see TA233)
D16 = XXXX = First byte = Tape sense byte 12 (see TA233)
Second byte = Tape sense byte 13 (see TA233)
D17 = XXXX = First byte = Tape sense byte 14 (see TA233)
Second byte = Tape sense byte 15 (see TA233)
D18 = XXXX = First byte = Adapter status extended (see TA233)
Second byte = Adapter status (see TA233)
D19 = XXXX = First byte = Device address

Device Address

| Adr Bit 4 | Adr Bit 2 | Adr Bit 1 | Not Used | Not Used | Not Adr 4 | Not Adr 2 | Not Adr 1 |
|---|---|---|---|---|---|---|---|

When an address mismatch occurs during selection, bits 0 through 7 are set to the value returned on the Control Line Bus In during Select Device Tag hex 83.

For all other cases, the drive address is binary encoded and placed in bits 0 to 2 by the Magnetic Tape Attachment; bits 3 to 7 are not used.

Second byte = PIO command (see TA333)
D20 = XXXX = First byte = Tag bus
Second byte = Bus Out

**Note:** *See* IBM 8809 Magnetic Tape Unit Description, *Form GA26-1659, for detailed explanation of D20 field.*

D21 = XXXX = Symptom code
D22 = XXXX = 0
D23—D30 = XXXX = Not used

## *TA333 DPPX and DPCX Common Error Log Byte Meanings*

Certain fields in the DPPX error log and the DPCX condition/incident log, although named differently, have identical bit or byte meanings. The following paragraphs explain these fields and their meanings, as well as list the field names as used by each operating system.

### Adapter Return Code (ARC)

You can find the DPPX adapter return code in the ARC field and the DPCX adapter return code in the D5 field. (For DPCX, a Translated Adapter Return Code (TARC) is found in the D6 field.) The following explains their meanings:

| ARC (in Hex) | Meaning |
|---|---|
| 00 | Normal completion |
| 02 | FRB busy |
| 03 | SCA busy |
| 09 | SCA not open |
| 0A | Adapter not open |
| 0B | SCA already open |
| 11 | FRB program check |
| 12 | BCL program check |
| 20 | Indeterminate equipment check |
| 21 | Adapter equipment check |
| 22 | SCA equipment check |
| 29 | Overrun |
| 2B | Position lost |
| 33 | PEID check |
| 38 | DSE failure |
| 39 | Read data check |
| 3A | Write data check |
| 3B | Loop write-to-read |
| 61 | File protected (TARC = 41) |
| 62 | SCA not ready (TARC = 42) |
| 68 | Incorrect mode (TARC = 48) |
| 69 | Marker sensor (TARC = 49) |
| 6A | Ready recovery (TARC = 4A) |
| 75 | AIO machine check (TARC = 45) |
| 76 | PIO machine check — nonrecursive (TARC = 46) |
| E3 | Data unsafe (TARC = 53) |
| F6 | PIO machine check — recursive (TARC = 56) |

### Command Byte

You can find the DPPX BCLE command byte in byte 1 of the BCLE field and the DPCX command byte in the D2 field or the C-FR field. The following explains their meanings:

| Command Byte (in Hex) | Meaning |
|---|---|
| 00 | Transfer control |
| 01 | Read |
| 02 | Write |
| 07 | No operation |
| 93 | Forward space file |
| 9B | Forward space block |
| B3 | Backspace file |
| BB | Backspace block |
| C2 | Data security erase |
| D3 | Rewind unload |
| F2 | Write tape mark |
| F3 | Rewind |
| FB | Mode set |

### Completion Status

You can find the DPPX completion status in the COMPSTAT field and the DPCX completion status in the D3 field. The following explains their meanings:

| Bit | Meaning |
|---|---|
| 0 | Extended status indicator |
| 1 | Reenter |
| 2 | Reenter FRB indicator |
| 3 | Not used |
| 4 | Complete |
| 5 | Error |
| 6 | Exception |
| 7 | Attention |

### Function Module Request Code

You can find the DPPX function module request code in the CRC field and the DPCX function module request code in the S-FR field or D1 field. The following explains their meanings:

| Code (in Hex) | Meaning |
|---|---|
| 00 | Execute |
| 03 | Open adapter |
| 05 | Read operational statistics |
| 07 | No operation |
| 0D | Terminate FRB |
| 23 | Open SCA |
| 25 | Read SCA state |
| 35 | Read SCA state when ready |
| AB | Close SCA |
| EB | Terminate adapter |

**PIO Command**

You can find the DPPX PIO command in the second byte of D46 field, and the DPCX PIO command in the second byte of D19 field. The following explains their meanings:

| PIO Command (in Hex) | Meaning |
|---|---|
| 02 | Adapter reset |
| 04 | Reset basic status |
| 06 | Set basic status |
| 07 | Read status |
| 08 | Enable timer |
| 0A | End op |
| 10 | Set burst length counter |
| 14 | Reset status |
| 16 | Set status |
| 24 | Step counters |
| 27 | Read burst length counter |
| 2C | Load burst length register |
| 2F | Read burst length register |
| 30 | Disconnect TAM |
| 34 | Set UC SAR counter |
| 37 | Read UC SAR counter |
| 38 | Test control line parity |
| 3A | Wrap |
| 3C | Set control line SAR counter |
| 3F | Read control line SAR counter |
| 48 | Set segment count |
| 4B | Read segment count |
| 50 | Write command pointer number |
| 53 | Read command pointer number |
| 54 | Set extended address register |
| 57 | Read extended address register |
| 58 | Write data pointer number |
| 5B | Read data pointer number |
| 5C | Set basic address register |
| 5F | Read basic address register |
| 61 | Read control lines bus in |
| 62 | Write buffer |
| 66 | Execute poll sequence |
| 69 | Read buffer |
| 6C | Execute selection sequence |
| 6E | Execute immediate sequence |
| 74 | Execute immediate disconnect sequence |
| 76 | Execute external without data sequence |
| 7C | Execute FCB list |

*TA334 Tape Statistical Data (TSD) Counters*

You can find Tape Statistical Data (TSD) counter information in the DPPX error log D25–D36 fields; for DPCX, run the SYSLTSD utility (see CP853 in Chapter 2) to obtain TSD counter information. Figure TA334-1 shows the 8809 TSD counters.

| Counter Size in Bytes | DPPX Error Log Byte | Counter Name | Set by Sense Byte | Set by Sense Bit |
|---|---|---|---|---|
| 2 | D32 | C01-Start I/O Count | Determined by FDM | |
| 2 | D35 | C02-Write Skips | Determined by FDM | |
| 2 | D36 | C03-Read Retry | Determined by FDM | |
| 1 | D31, first byte | *C04-Temp Read Errors | 1 | 0 (Byte 6 Bit 0 = 0) |
| 1 | D31, second byte | *C05-Temp Write Errors | 1 | 0 (Byte 6 Bit 0 = 1) |
| 1 | D34, first byte | C06-Tape Adapter Parity Errors | 16 | 2 |
| 1 | D34, second byte | C07-Overrun | 2 | 0 |
| 1 | D25, first byte | C08-Multi-Track Errors | 6 | 2 |
| 1 | D25, second byte | C09-End Data Check | 6 | 3 |
| 1 | D26, first byte | C10-Start Read Check | 6 | 4 |
| 1 | D26, second byte | C11-Read Back Failure | 6 | 5 (Bit 0 = 1) |
| 1 | D27, first byte | C12-Envelope Check | 6 | 6 |
| 1 | D27, second byte | C13-No Pointer Error | 6 | 1 (Bit 0 = 0) |
| 1 | D28, first byte | C14-Crease Error | 6 | 5 (Bit 0 = 0) |
| 1 | D28, second byte | C15-Skew Error | 6 | 7 (Bit 0 = 0) |
| 1 | D29, first byte | C16-Track 4 Error | 5 | 4 |
| 1 | D29, second byte | C17-Track 5 Error | 5 | 5 |
| 1 | D30, first byte | C18-Track P Error | 4 | 6 |
| 1 | D30, second byte | *C19-Velocity Check | 9 | 0, 1, or 2 |
| 1 | D33, second byte | *C20-Read Bus Parity Check | 4 | 1 |

| *THRESHOLDS: | | |
|---|---|---|
| | Temporary Read Errors | 16 |
| | Temporary Write Errors | 16 |
| | Read Bus Parity Checks | 16 |
| | Velocity Checks | 8 |
| | All others | Full Count |

**Figure TA334-1. 8809 Tape Statistical Data (TSD) Counters**

## TA340 How to Use the Error Log to Determine Tape Adapter Failures

The procedure for examining the error log depends upon whether the customer is using DPPX or DPCX. For DPPX, see TA341; for DPCX, see TA342.

### *TA341 DPPX Error Log*

Run ELDA and obtain the Symptom Code from the last error occurring on the suspected tape drive. You can then either use the TA MAP by selecting entry point D 'Test Symptom Code' or use the action plan in section TA350.

Chapter 2 contains the invocation procedures and output format for ELDA.

### *TA342 DPCX Condition/Incident Log*

**Run SYSLERR and obtain the Symptom Code (D21 field) from the last Type-5 error record occurring on the suspected tape drive. You can then use the TA MAP by selecting entry point D 'Test Symptom Code' or use the action plan in TA350.**

Chapter 2 contains the invocation procedures for SYSLERR, and TA332 shows the format of the log records and the location of the Symptom Code (field D21) in the Type-5 record.

## TA350 Action Plan to Correct Intermittent Failures

For any Symptom Code format of from BXXX to FXXX that you obtained by running ELDA or SYSLERR, go to the tape drive MAP to correct the problem. For any symptom **code format of AXXX, or if no symptom code is available, use either TA351, TA352, or TA353 to troubleshoot in the sequence tabulated below.**

**Caution: Turn power off when removing or exchanging cards or cables. If Model 1B, the Local/Remote power switch should be in Local position.**

### *TA351 8809 Model 1A Intermittent Failure Action Plan (Adapter in 8101)*

| Probable Causes | Action | Comments |
|---|---|---|
| 1. Incorrect voltages | Measure A2 board voltages:<br>D2D03 = +4.5 to +5.5V dc<br>D2B11 = +7.7 to +9.3V dc<br>D2B06 = -4.5 to -5.5V dc | For missing or out-of-tolerance voltages, go to 8100 PA MIM section |
| 2. Loose or defective cables. See TA431 for locations | Inspect for loose or defective cables:<br>1. Y1 to Bus<br>2. Z1 to Tag<br>3. SCF cable<br>4. Bus and Tag cables to tape drive (inspect both ends) | See Note. |
| 3. Defective tape adapter cards | Exchange A2B2, A2C2, and A2D2 cards with new ones. | See Note. |
| 4. Defective SCF card | Exchange card A2A2 with a new one. | See Note. |

**Note:** *To verify the fix, run the TA tests and loop for a minimum of 15 minutes (each loop takes 7 minutes). If the tests fail, use the TA MAP to find the failure. If the tests do not fail after looping, return the system to the customer. Obtain a new error log after the customer has used the system. If the same error has occurred, replace any cards that were exchanged and go to the next step in the table. If all steps have been performed and the error persists, request aid.*

### *TA352 8809 Model 1A Intermittent Failure Action Plan (Adapter in 8140)*

| Probable Causes | Action | Comments |
|---|---|---|
| 1. Incorrect voltages | Measure voltages on adapter board (C2 or D2):<br>J2D03 = +4.5 to +5.5V dc<br>J2B11 = +7.7 to +9.3V dc<br>J2B06 = -4.5 to -5.5V dc | For missing or out-of-tolerance voltages, go to PA section. |
| 2. Loose or defective cables. See TA432 for locations. | Inspect for loose or defective cables:<br>1. Y3 to bus<br>2. Z3 to tag<br>3. SCF cables (on C2A2 card)<br>4. Bus and tag cables to tape drive (inspect both ends). | See Note. |
| 3. Defective tape adapter cards. | Exchange G2, H2, and J2 on adapter board (C2 or D2) with new ones. | See Note. |
| 4. Defective SCF card | Exchange card C2A2 with a new one. | See Note. |

**Note:** *To verify the fix, run the TA tests and loop for a minimum of 15 minutes (each loop takes 7 minutes). If the tests fail, use the TA MAP to find the failure. If the tests do not fail after looping, return the system to the customer. Obtain a new error log after the customer has used the system. If the same error has occurred, replace any cards that were exchanged and go to the next step in the table. If all steps have been performed and the error persists, request aid.*

### *TA353 8809 Model 1B Intermittent Failure Action Plan*

| Probable Causes | Action | Comments |
|---|---|---|
| 1. Incorrect voltages | Measure 01A Gate voltages:<br>E2D03 = +4.5 to +5.5V dc<br>E2B11 = +7.7 to +9.3V dc<br>E2B06 = -4.5 to -5.5V dc<br>Measure the 01B gate voltage<br>B2D03 = +4.5 to +5.5V dc | For missing or out-of-tolerance voltages, go to 8809 Start MAP. |
| 2. Loose or defective cables. **See TA433** for locations. | Inspect for loose or defective SCF cables:<br>1. From 01A-B2 to 01B-A2<br>2. From SCF top-card connectors to I/O panel. | See Note 1. |
| 3. Defective tape adapter cards | Exchange 01A-D2 and 01A-E2 cards with new ones. | See Note 1. |
| 4. Defective SCF card | Exchange 01B-B2 card with a new one. | See Notes 1 and 2. |

**Notes:**

1. *To verify the fix, run the TA tests and loop for a minimum of 15 minutes (each loop takes 7 minutes). If the tests fail, use the TA MAP to find the failure. If the tests do not fail after looping, return the system to the customer. Obtain a new error log after the customer has used the system. If the same error has occurred, replace any cards that were exchanged and go on to the next step in the table. If all steps have been performed and the error persists, request aid.*
2. *The 8809 Local/Remote power switch should be in Local, and the 8809 should be powered off before exchanging the SCF card.*

## TA400 Signal Paths and Detailed Operational Description

This section contains point-to-point wiring diagrams and data flow illustrations of the 8809 adapter cards. Figure TA400-1 shows the detailed data flow of the tape adapter.

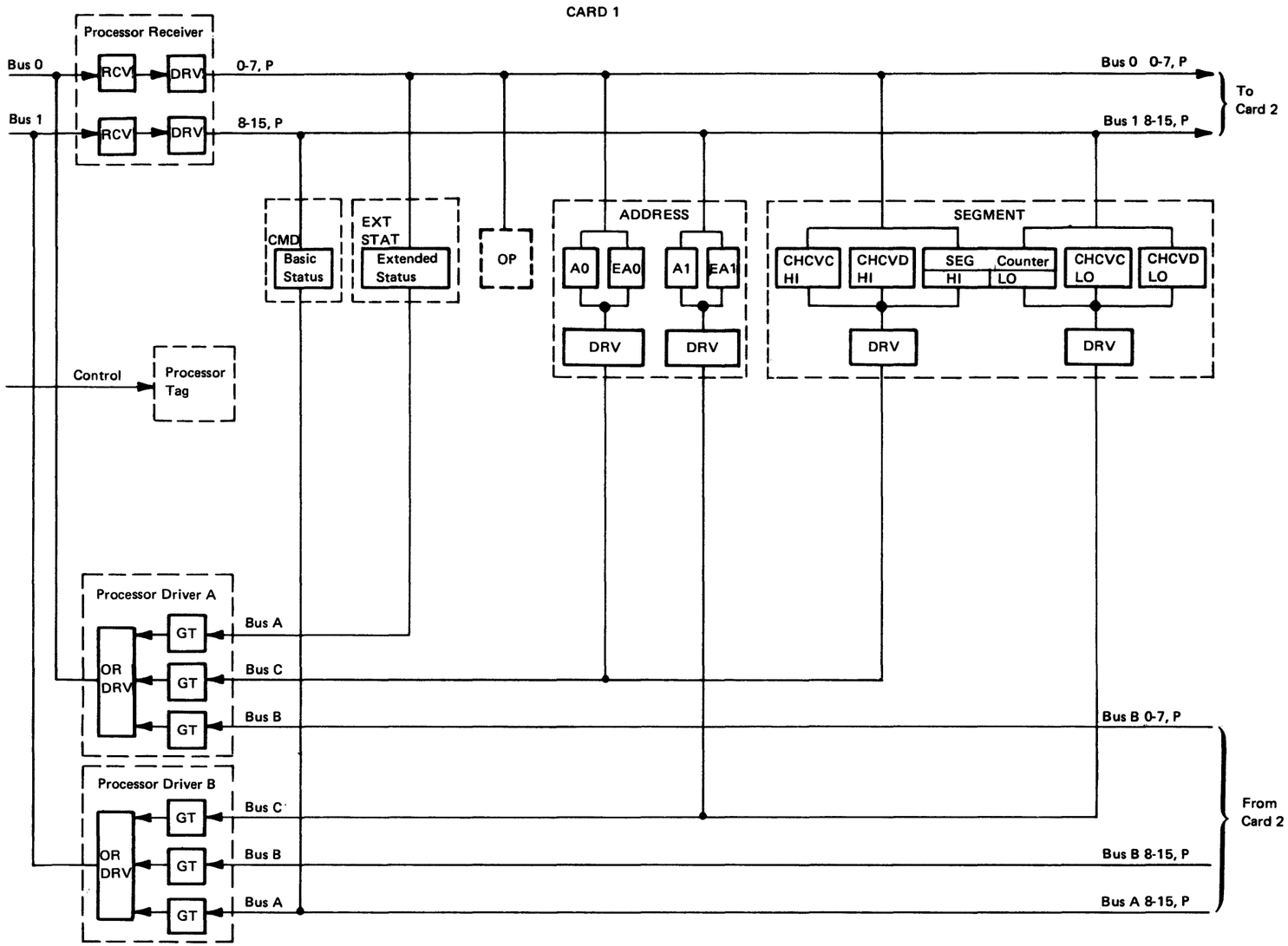



**Figure TA400-1 (Part 1 of 2). Adapter Detailed Data Flow Diagram**

CARD 2

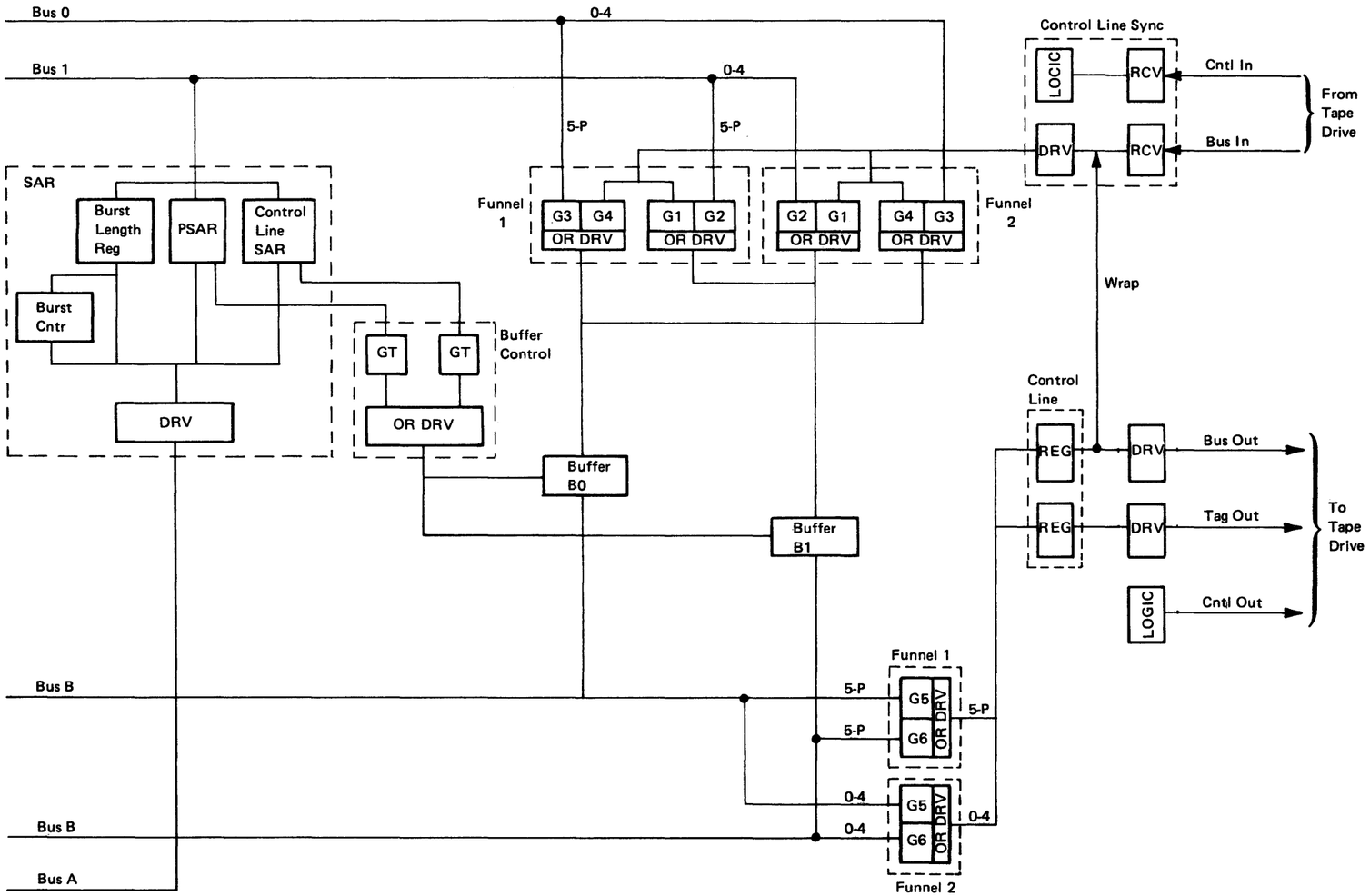



**Figure TA400-1 (Part 2 of 2). Adapter Detailed Data Flow Diagram**

## TA410 Adapter Card Interconnection Logic Signals

Figures TA410-1 and TA410-2 show the logic signals between the adapter cards for both 8809 models. See Figure TA410-3 for adapter card locations.

Top Card Connectors (See Note)

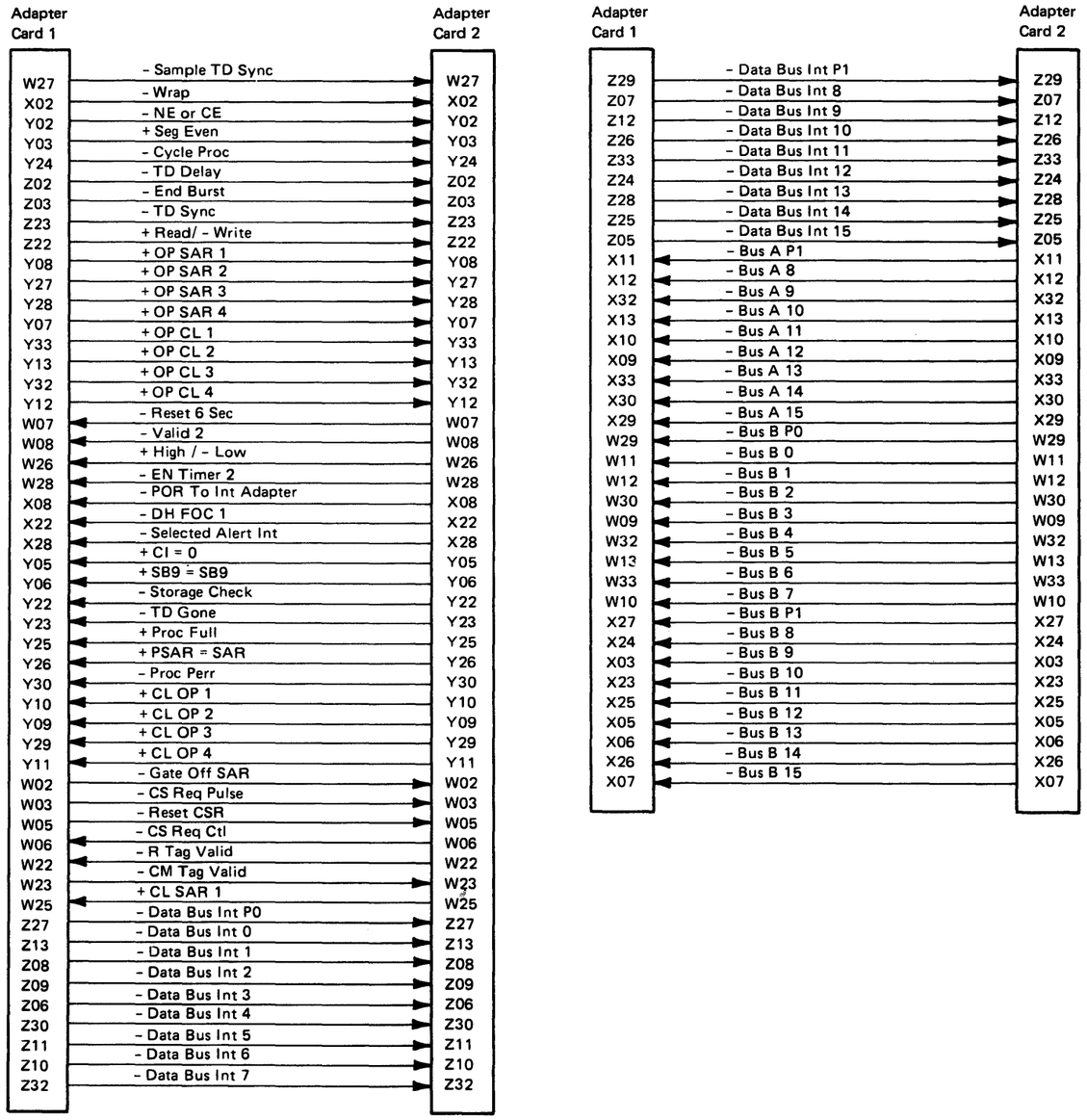



**Figure TA410-1. Logic Signals Between Adapter Top Card Connectors**

Intercard Connections

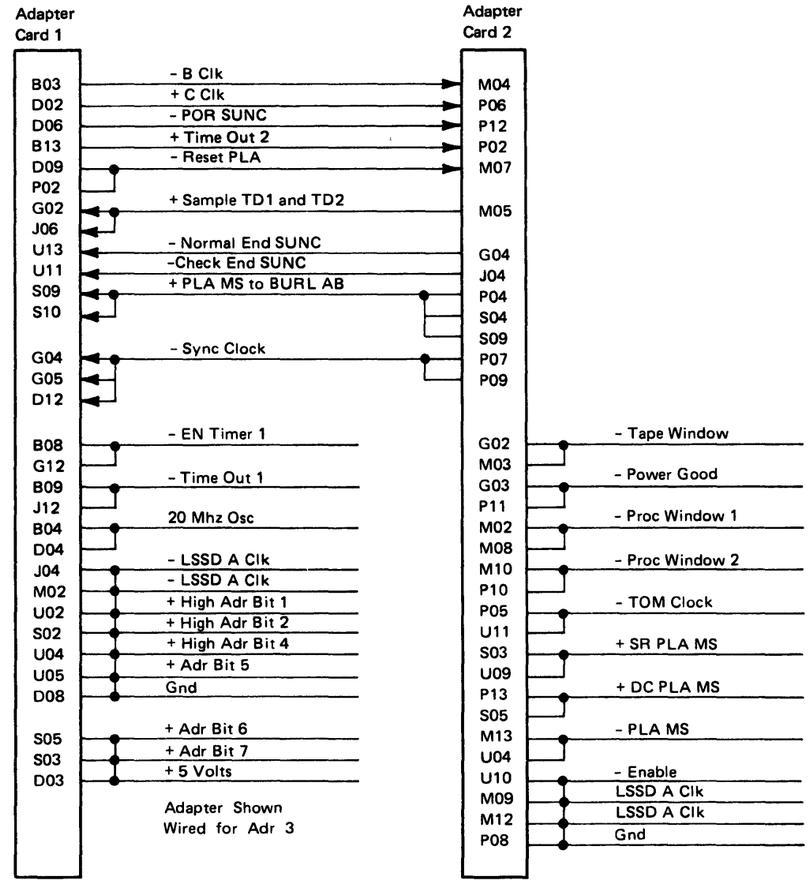



**Figure TA410-2. Logic Signals Between Adapter Cards**

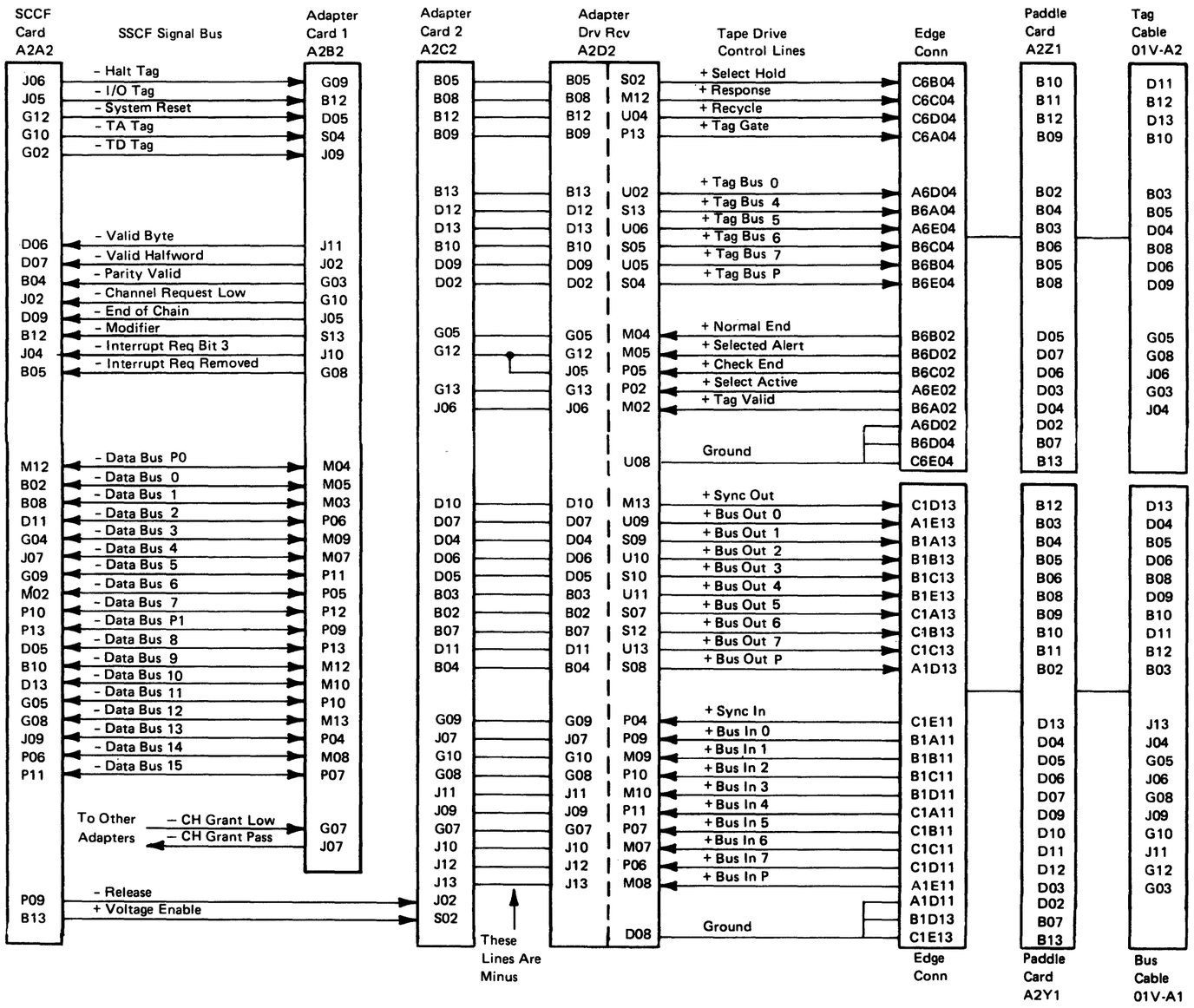
| | Model 1A | | | Model 1B |
|---|---|---|---|---|
| | **Adapter in 8101** | **Adapter in 8140 C2 Board** | **Adapter in 8140 D2 Board** | **Adapter in 8809** |
| Adapter Card 1 | A2B2 | C2G2 | D2G2 | A1D2 |
| Adapter Card 2 | A2C2 | C2H2 | D2H2 | A1E2 |

**Figure TA410-3. Adapter Card Locations**

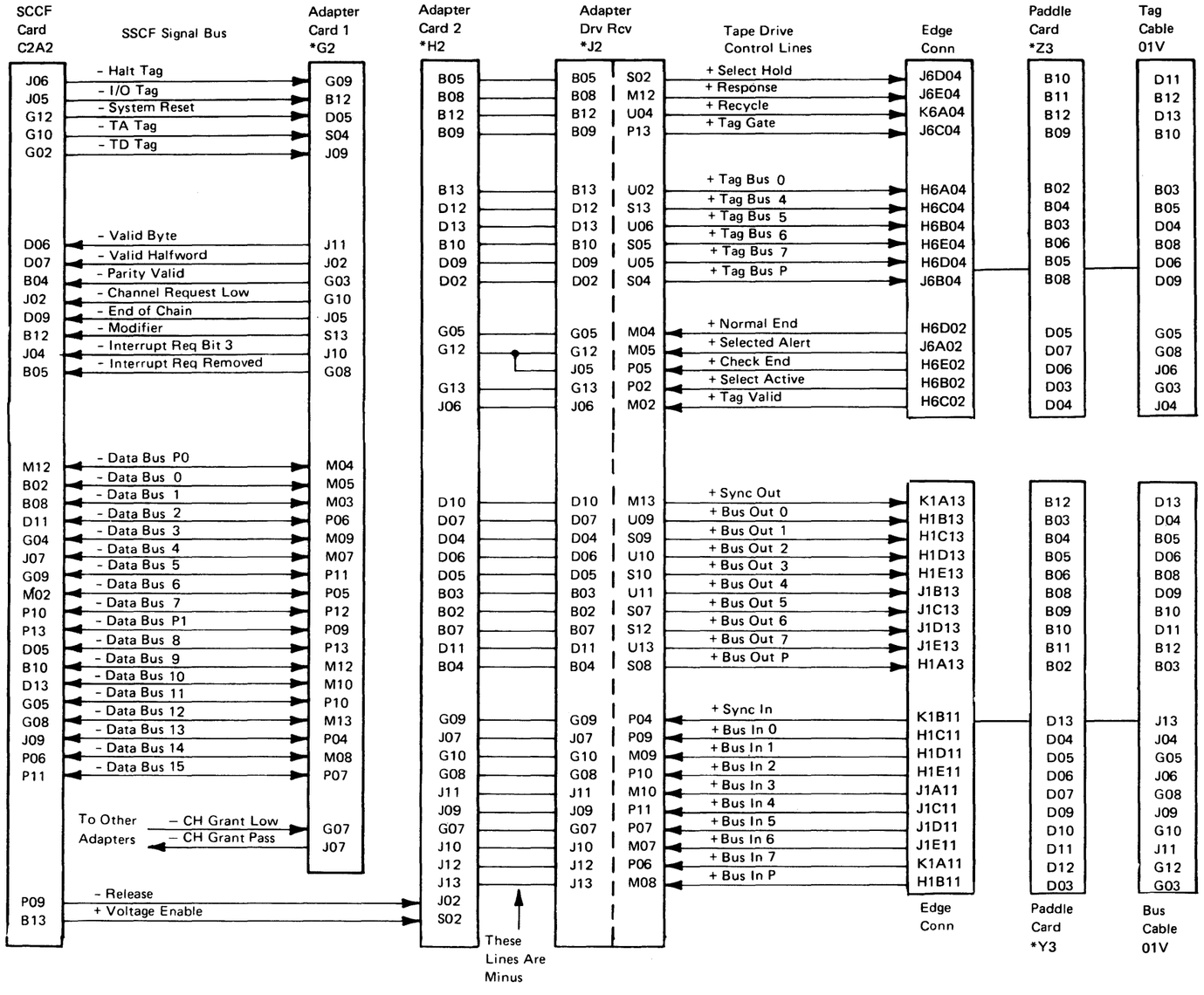
## TA420 Adapter Card Wiring Diagrams

Sections TA421-1, TA422-1, and TA423-1 show the point-to-point connections from the SSCF (SC5) card to adapter card 1 (TA1) and from adapter card 2 (TA2) to the tag and bus cables for 8809 Models 1A and 1B.

### *TA421 8809 Model 1A Adapter Card Wiring (Adapter in 8101)*

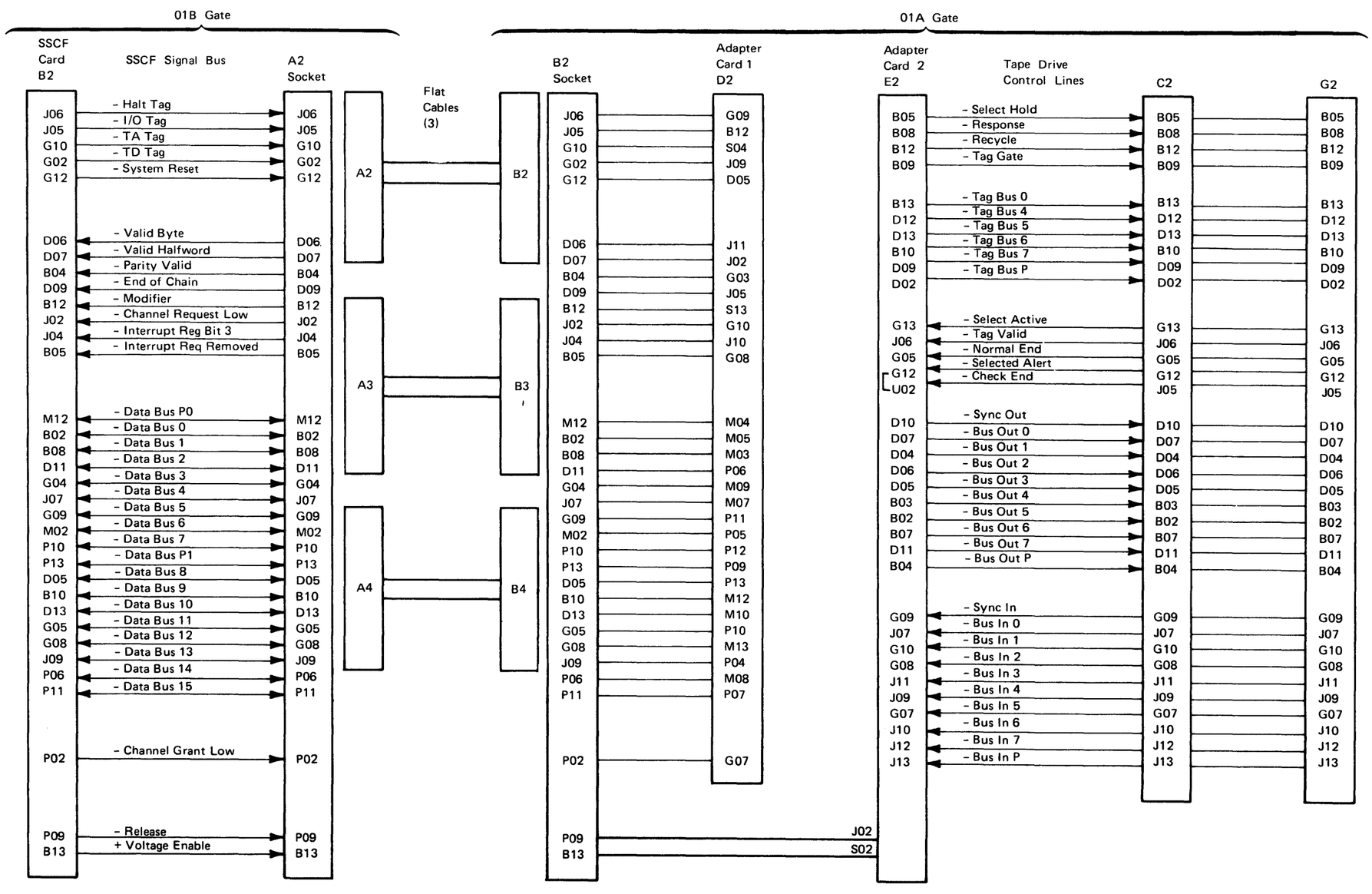


*TA422 8809 Model 1A Adapter Card Wiring (Adapter in 8140)*




*Card may be in C2 or D2 board

*TA423 8809 Model 1B Adapter Card Wiring*



## TA430 Adapter Card and Top Card Connector Locations and Illustrations

The figures in the following sections show the location and pin numbering scheme of the tape adapter card top card connectors, as well as locations and illustrations of the adapter cards for 8809 Models 1A and 1B.

### *TA431 8809 Model 1A Adapter Card and Top Card Connector Locations (Adapter in 8101)*

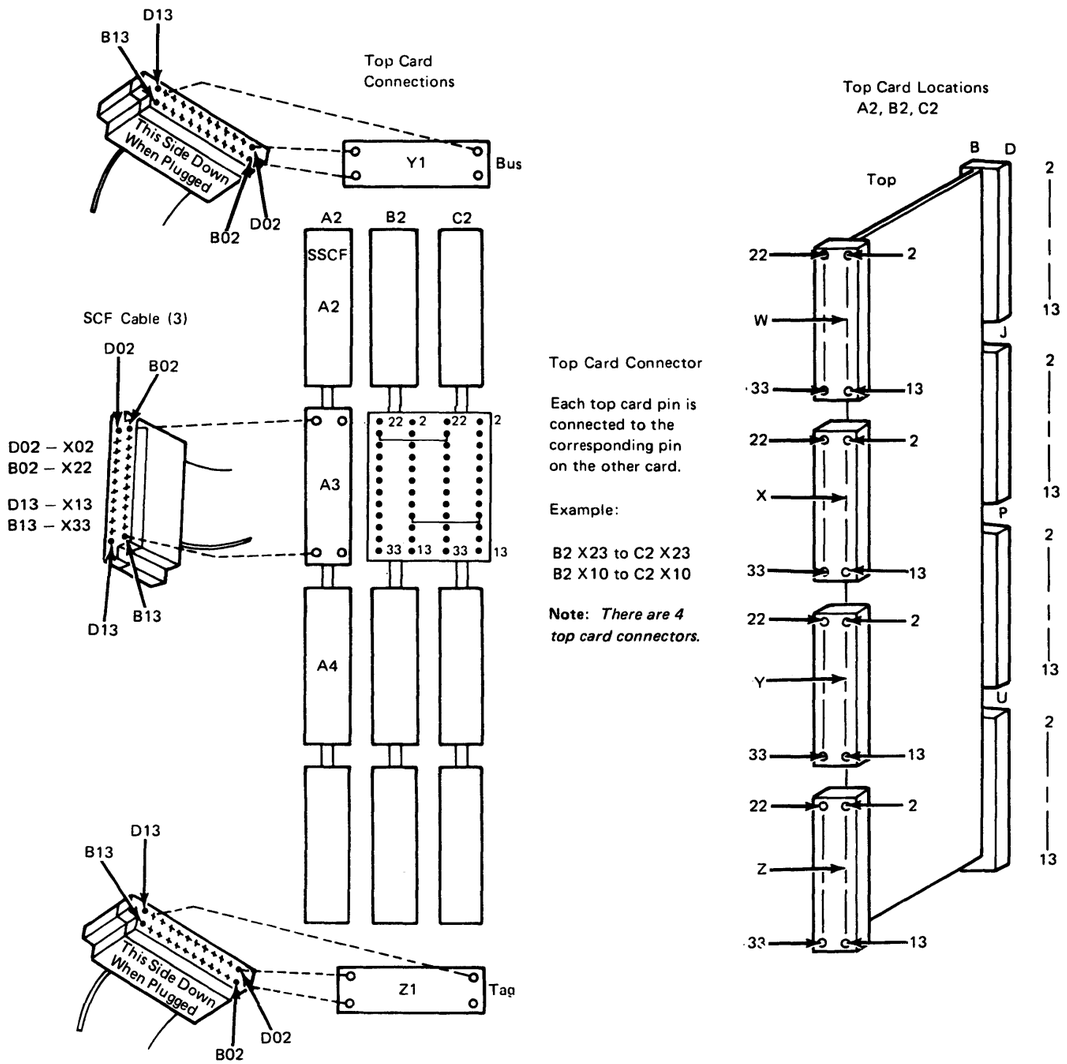



**Figure TA431-1. Top Card Connector Location and Pin Numbering, Model 1A (Adapter in 8101)**

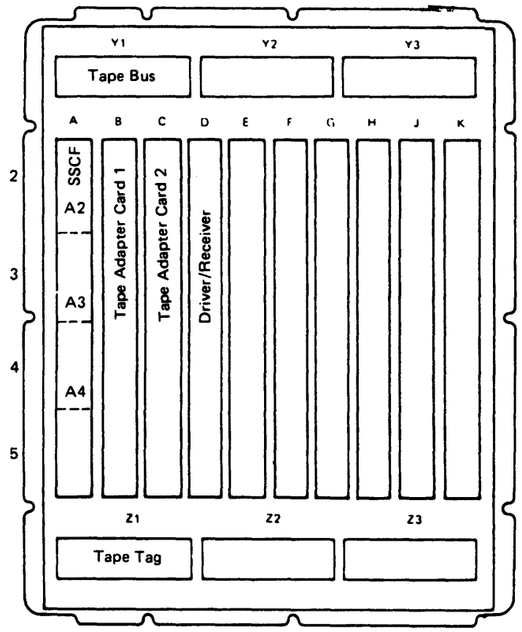



**Figure TA431-2. Adapter Card and Cable Locations—8101 01A-A2 Board (Card Side)**

*TA432 8809 Model 1A Adapter Card and Top Card Connector Locations (Adapter in 8140)*

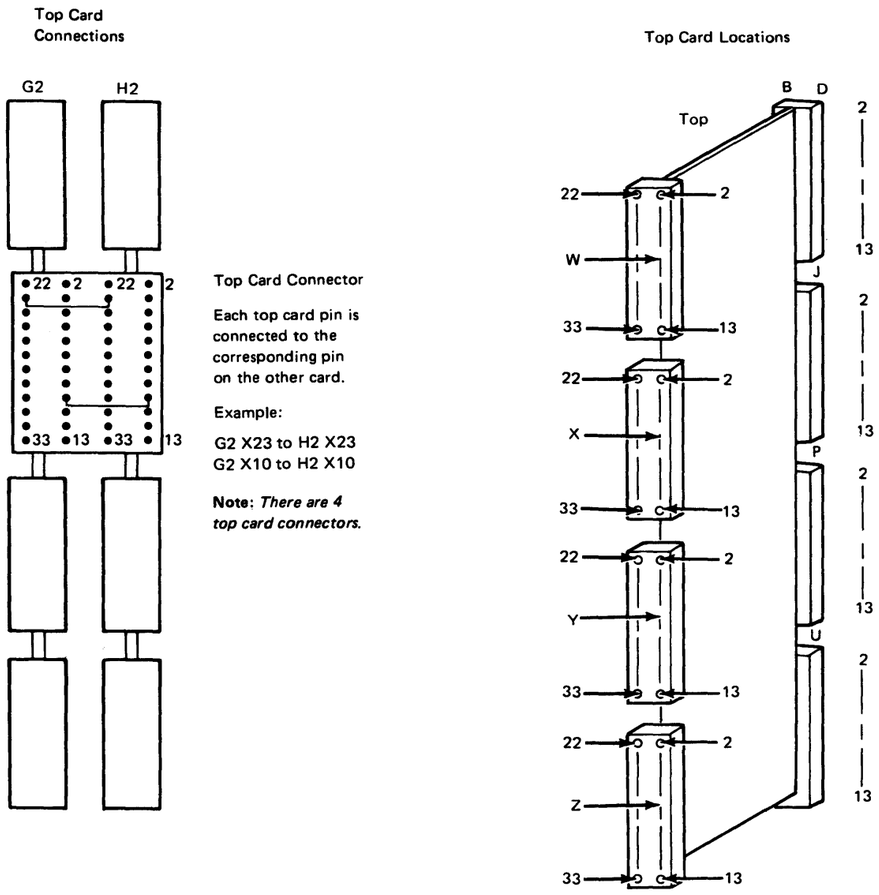
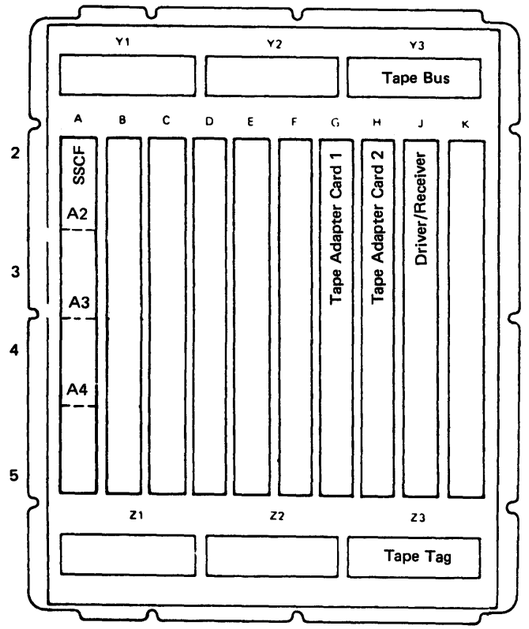



**Figure TA432-1. Top Card Connector Location and Pin Numbering, Model 1A (Adapter in 8140)**




**Note:** *SSCF card in C2 board only.*

**Figure TA432-2. Adapter and SCF Card Locations — 8140 C2 or D2 Board**

## *TA433 8809 Model 1B Adapter Card and Top Card Connector Locations (Figures TA433-1, -2)*

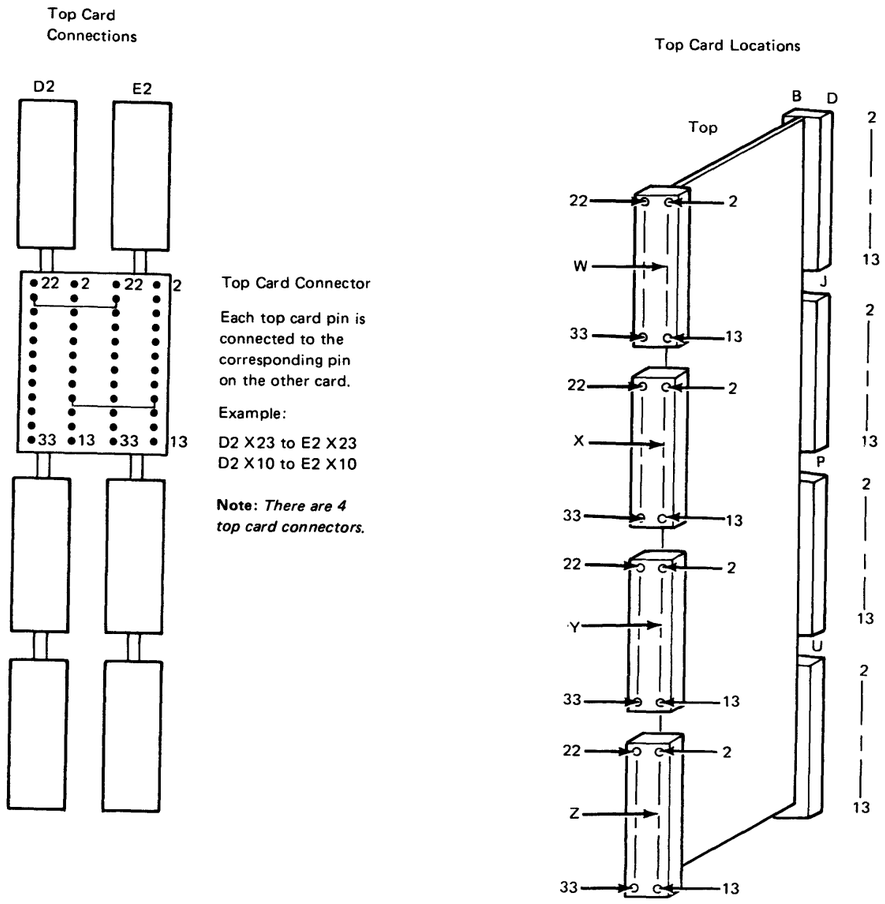



**Figure TA433-1. Top Card Connector Location and Pin Numbering, Model 1B**

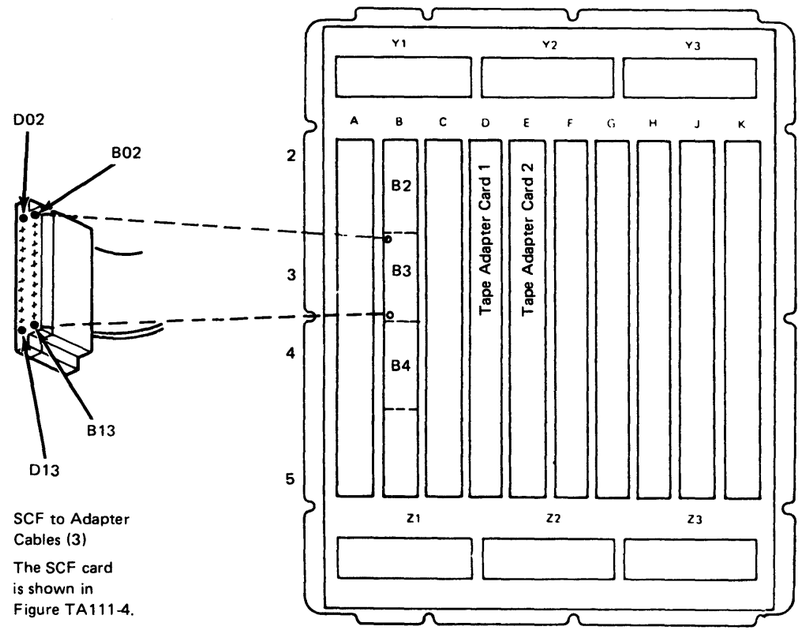
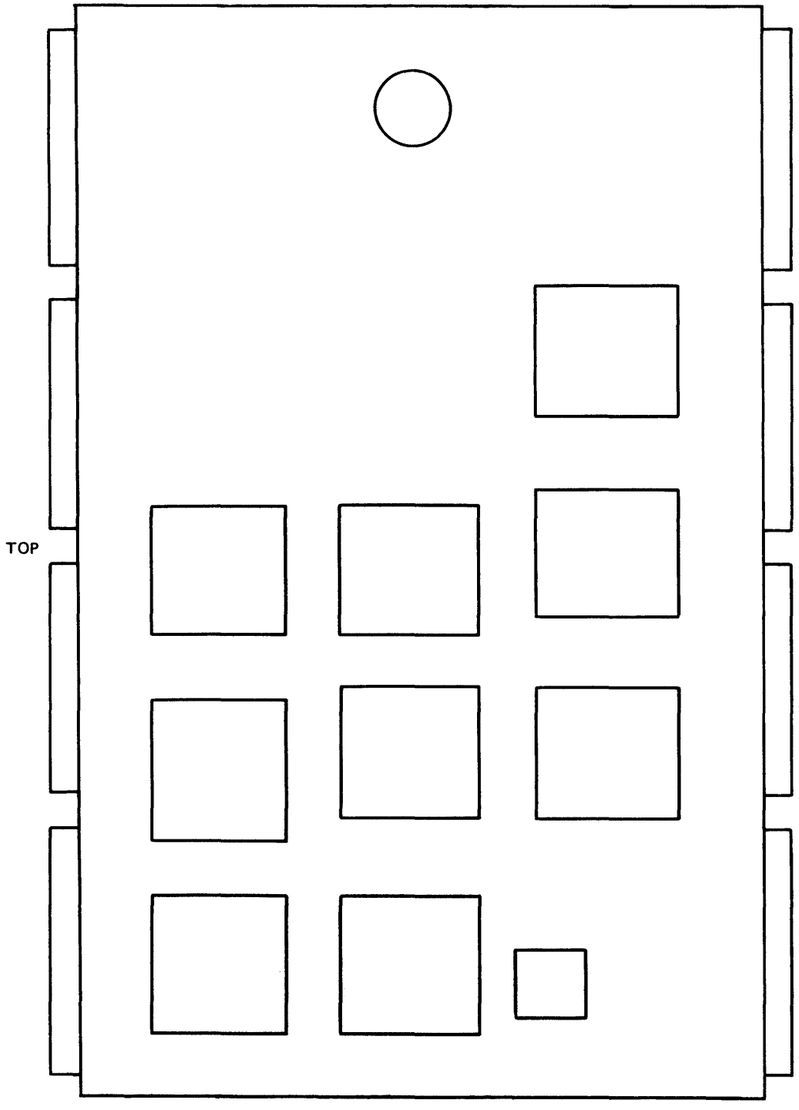


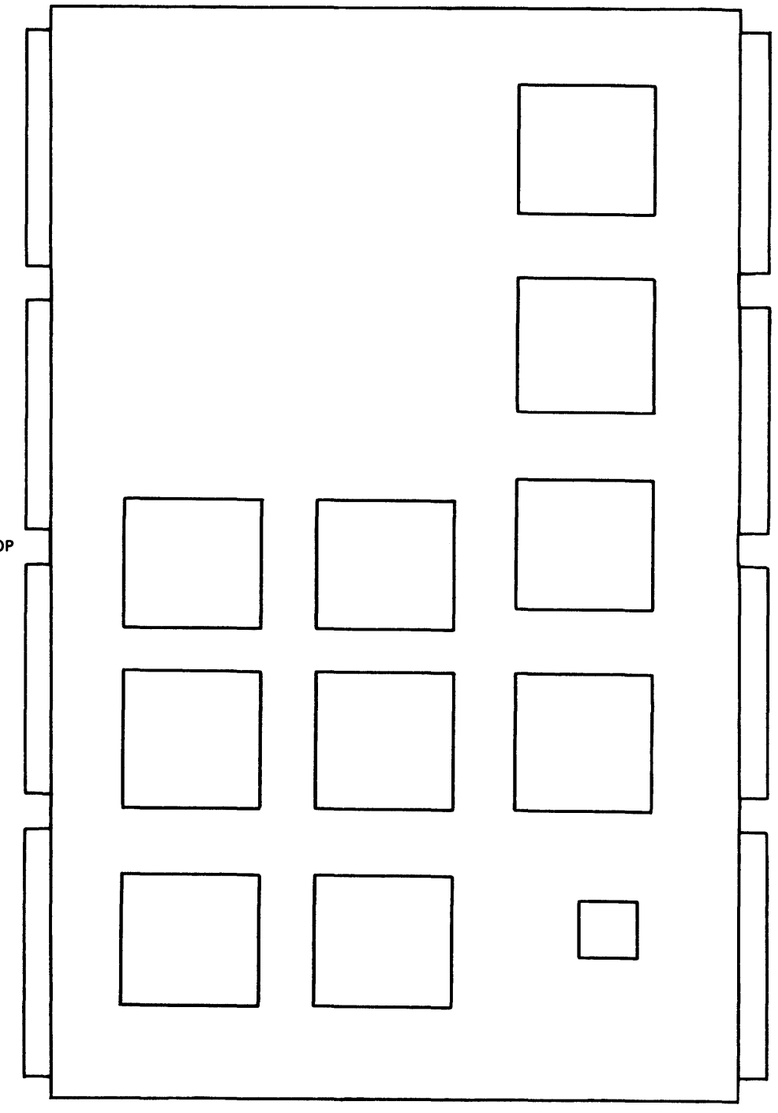

**Figure TA433-2. Adapter Card and Cable Locations—8809 01A-A1 Board (Card Side)**

*TA434 8809 Adapter Card Illustrations (Figures TA434-1, -2, and -3)*



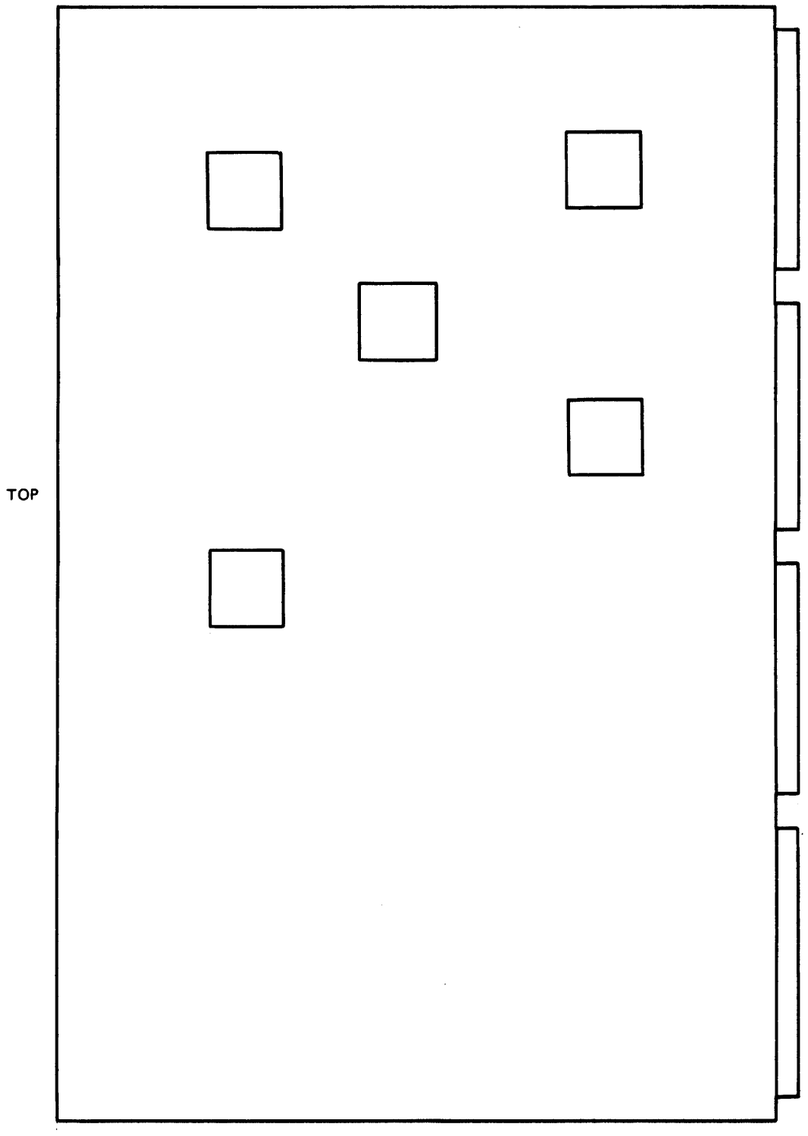

Note: *8101 Location = A2B2*
*8809 Location = A1D2*
*8140 Location = C2G2 or D2G2*

**Figure TA434-1. TA1 Card**




Note: *8101 Location = A2C2*
*8809 Location = A1E2*
*8140 Location = C2H2 or D2H2*

**Figure TA434-2. TA2 Card**




**Note:** *Used only for Model 1A.*
*8101 Location = A2D2*
*8140 Location = C2J2 or D2J2*

**Figure TA434-3. TA3 Card**

## TA440 Tape Adapter Voltage Checks

To ensure correct voltages to the tape adapter cards, meter the voltages as follows:

**8809 Model 1A Voltage Check Pins (Adapter in 8101)***

| Pin | Range |
|---|---|
| D2D03 | +4.5V to +5.5V dc |
| D2B11 | +7.7V to +9.3V dc |
| D2B06 | -4.5V to -5.5V dc |

*Meter these voltages on the 8101 01A-A2 board.

**8809 Model 1A Voltage Check Pins (Adapter in 8140)***

| Pin | Range |
|---|---|
| J2D03 | +4.5V to +5.5V dc |
| J2B11 | +7.7V to +9.3V dc |
| J2B06 | -4.5V to -5.5V dc |

*Meter these voltages on the 8140 adapter board (01A-C2 or D2).

**8809 Model 1B Voltage Check Pins***

| Pin | Range |
|---|---|
| E2D03 | +4.5V to +5.5V dc |
| E2B11 | +7.7V to +9.3V dc |
| E2B06 | -4.5V to -5.5V dc |

*Meter these voltages on the 8809 board. In addition, check the D03 pin on the SCF card for the presence of +5.0V dc.

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## A450 Adapter Point-to-Point Net Checklists

### *TA451 8809 Model 1A Point-to-Point Net Checklist (Adapter in 8101)*

Find the test error message pattern in Figure TA451-1. All nets in the figure refer to all test error patterns indicated. Line entries reading from left to right are separate nets, and apply for any error listed in the test error pattern column. Check continuity between the test points, which are all located on the 8101 A2 board. If any net does not indicate continuity, correct by wire-wrapping the points together.

| Test Error Pattern | Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|---|
| PA80 | B2B03 | C2M04 | | | |
| PA95 | B2B04 | B2D04 | | | |
| PA96 | B2B12 | A2J05 | | | |
| XXBC | B2D02 | C2P06 | | | |
| PAXE 01XX | B2D05 | A2G12 | | | |
| PAXE 02XX | B2D06 | C2P12 | | | |
| PAXE 03XX | B2D09 | B2P02 | C2M07 | | |
| PAXE 09XX | B2D12 | B2G04 | B2G05 | C2P07 | C2P09 |
| | B2G02 | B2J06 | C2M05 | | |
| | B2G03 | A2B04 | | | |
| | B2G08 | A2B05 | | | |
| | B2G09 | A2J06 | | | |
| | B2G10 | A2J02 | | | |
| | B2J02 | A2D07 | | | |
| | B2J04 | GND | | | |
| | B2J05 | A2D09 | | | |
| | B2J09 | A2G02 | | | |
| | B2J10 | A2J04 | | | |
| | B2J11 | A2D06 | | | |
| | B2M03 | A2B08 | | | |
| | B2M04 | A2M12 | | | |
| | B2M05 | A2B02 | | | |
| | B2M07 | A2J07 | | | |
| | B2M08 | A2P06 | | | |
| | B2M09 | A2G04 | | | |
| | B2M10 | A2D13 | | | |
| | B2M12 | A2B10 | | | |
| | B2M13 | A2G08 | | | |
| | B2P04 | A2J09 | | | |
| | B2P05 | A2M02 | | | |
| | B2P06 | A2D11 | | | |
| | B2P07 | A2P11 | | | |
| | B2P09 | A2P13 | | | |
| | B2P10 | A2G05 | | | |
| | B2P11 | A2G09 | | | |
| | B2P12 | A2P10 | | | |
| | B2P13 | A2D05 | | | |
| | B2S04 | A2G10 | | | |
| | B2S13 | A2B12 | | | |
| | C2M09 | GND | | | |
| | C2S03 | C2U09 | | | |
| | C2S04 | C2S09 | C2P04 | B2S09 | B2S10 |
| | B2J07 | H2G03 | | | |
| | B2G07 | G2S07 | | | |

**Figure TA451-1 (Part 1 of 2). Model 1A Adapter Net Checklist (Adapter in 8101)**

**Note:** *If an adapter is installed, the jumper at B2G07 to B2J07 MUST be removed.*

| Test Error Pattern | Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|---|
| PAXE 04XX | B2B08 | B2G12 | | | |
| through | B2B09 | B2J12 | | | |
| PAXE 08XX | B2G02 | B2J06 | C2M05 | | |
| and | C2G02 | C2M03 | | | |
| PAXE 11XX | C2G12 | D2G12 | D2J05 | | |
| through | C2M02 | C2M08 | | | |
| PAXE 15XX | C2M03 | C2G02 | | | |
| | C2M10 | C2P10 | | | |
| | C2P05 | C2U11 | | | |
| | C2P07 | C2P09 | B2D12 | B2G04 | B2G05 |
| | C2P13 | C2S05 | | | |
| | C2U10 | GND | | | |
| | B2J10 | A2J04 | | | |

| Test Error Pattern | Point A | Point B |
|---|---|---|
| PAXE 40XX<br>through<br>PAXE 43XX | B2B13 | C2P02 |
| | B2U11 | C2J04 |
| | B2U13 | C2G04 |
| | C2B02 | D2B02 |
| | C2B03 | D2B03 |
| | C2B04 | D2B04 |
| | C2B05 | D2B05 |
| | C2B07 | D2B07 |
| | C2B08 | D2B08 |
| | C2B09 | D2B09 |
| | C2B10 | D2B10 |
| | C2B12 | D2B12 |
| | C2B13 | D2B13 |
| | C2D02 | D2D02 |
| | C2D04 | D2D04 |
| | C2D05 | D2D05 |
| | C2D06 | D2D06 |
| | C2D07 | D2D07 |
| | C2D09 | D2D09 |
| | C2D10 | D2D10 |
| | C2D11 | D2D11 |
| | C2D12 | D2D12 |
| | C2D13 | D2D13 |
| | C2G05 | D2G05 |
| | C2G07 | D2G07 |
| | C2G08 | D2G08 |
| | C2G09 | D2G09 |
| | C2G10 | D2G10 |
| | C2G13 | D2G13 |
| | C2J02 | A2P09 |
| | C2J06 | D2J06 |
| | C2J07 | D2J07 |
| | C2J09 | D2J09 |
| | C2J10 | D2J10 |

| Test Error Pattern | Point A | Point B |
|---|---|---|
| PAXE 40XX<br>through<br>PAXE 43XX<br>(cont'd.) | C2J11 | D2J11 |
| | C2J12 | D2J12 |
| | C2J13 | D2J13 |
| | C2M13 | C2U04 |
| | D2M02 | B6A02 |
| | D2M04 | B6B02 |
| | D2M07 | C1C11 |
| | D2M08 | A1E11 |
| | D2M09 | B1B11 |
| | D2M10 | B1D11 |
| | D2M12 | C6C04 |
| | D2M13 | C1D13 |
| | D2P02 | A6E02 |
| | D2P04 | C1E11 |
| | D2P06 | C1D11 |
| | D2P07 | C1B11 |
| | D2P09 | B1A11 |
| | D2P10 | B1C11 |
| | D2P11 | C1A11 |
| | D2P13 | C6A04 |
| | D2S02 | C6B04 |
| | D2S04 | B6E04 |
| | D2S05 | B6C04 |
| | D2S07 | C1A13 |
| | D2S08 | A1D13 |
| | D2S09 | B1A13 |
| | D2S10 | B1C13 |
| | D2S12 | C1B13 |
| | D2U02 | A6D04 |
| | D2U04 | C6D04 |
| | D2U05 | B6B04 |
| | D2U09 | A1E13 |
| | D2U10 | B1B13 |
| | D2U11 | B1E13 |
| | D2U13 | C1C13 |

| Test Error Pattern | Point A | Point B | Point C |
|---|---|---|---|
| PAXE 44XX<br>through<br>PAXE 56XX | B2J11 | A2D06 | |
| | B2S13 | A2B12 | |
| | B2U13 | C2G04 | |
| | C2B05 | D2B05 | |
| | C2D09 | D2D09 | |
| | C2G10 | D2G10 | |
| | C2G12 | D2G12 | D2J05 |
| | D2M05 | B6D02 | |
| | D2M09 | B1B11 | |
| | D2M12 | C6C04 | |
| | D2M13 | C1D13 | |
| | D2P04 | C1E11 | |
| | D2P05 | B6C02 | |
| | D2P11 | C1A11 | |
| | D2S10 | B1C13 | |
| | D2S13 | B6A04 | |
| | D2U04 | C6D04 | |
| | D2U06 | A6E04 | |

The net check points listed below do not cause test failures when both open and grounded, but should be checked to ensure proper tape logic continuity and operation.

| Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|
| B2B08 | B2G12 | | | |
| B2B13 | C2P02 | | | |
| B2D09 | B2P02 | C2M07 | | |
| B2G03 | A2B04 | | | |
| B2G08 | A2B05 | | | |
| B2G09 | A2J06 | | | |
| B2M02 | Gnd | | | |
| B2U11 | C2J04 | | | |
| C2D12 | D2D12 | | | |
| C2D13 | D2D13 | | | |
| C2G03 | C2P11 | | | |
| C2G13 | D2G13 | | | |
| C2M10 | C2P10 | | | |
| C2M12 | Gnd | | | |
| C2M13 | C2U04 | | | |
| C2S02 | A2B13 | | | |
| C2S04 | C2S09 | C2P04 | B2S09 | B2S10 |
| C2P05 | C2U11 | | | |
| D2S13 | B6A04 | | | |
| D2U06 | A6E04 | | | |
| B2J07 | H2G03 | | | |
| C2J02 | A2P09 | | | |
| D2D08 | C1E13 | B1D13 | A1D11 | |
| D2U08 | C6E04 | B6D04 | A6D02 | |

**Figure TA451-1 (Part 2 of 2). Model 1A Adapter Net Checklist (Adapter in 8101)**

*TA452 8809 Model 1A Point-to-Point Net Checklist (Adapter in 8140)*

Find the test error message pattern in Figure TA452-1. All nets in the figure refer to all test error patterns indicated. Line entries reading from left to right are separate nets, and apply for any error listed in the test error pattern column. Check continuity between the test points, which are all located on the 8140 C2 or D2 board. If any net does not indicate continuity, correct by wire-wrapping the points together.

| Test Error Pattern | Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|---|
| PA80 | G2B03 | H2M04 | | | |
| PA95 | G2B04 | G2D04 | | | |
| PA96 | G2B12 | A2J05 | | | |
| XXBC | G2D02 | H2P06 | | | |
| PAXE 01XX | G2D05 | A2G12 | | | |
| PAXE 02XX | G2D06 | H2P12 | | | |
| PAXE 03XX | G2D09 | G2P02 | H2M07 | | |
| PAXE 09XX | G2D12 | G2G04 | G2G05 | H2P07 | H2P09 |
| | G2G02 | G2J06 | H2M05 | | |
| | G2G03 | A2B04 | | | |
| | G2G08 | A2B05 | | | |
| | G2G09 | A2J06 | | | |
| | G2G10 | A2J02 | | | |
| | G2J02 | A2D07 | | | |
| | G2J04 | GND | | | |
| | G2J05 | A2D09 | | | |
| | G2J09 | A2G02 | | | |
| | G2J10 | A2J04 | | | |
| | G2J11 | A2D06 | | | |
| | G2M03 | A2B08 | | | |
| | G2M04 | A2M12 | | | |
| | G2M05 | A2B02 | | | |
| | G2M07 | A2J07 | | | |
| | G2M08 | A2P06 | | | |
| | G2M09 | A2G04 | | | |
| | G2M10 | A2D13 | | | |
| | G2M12 | A2B10 | | | |
| | G2M13 | A2G08 | | | |
| | G2P04 | A2J09 | | | |
| | G2P05 | A2M02 | | | |
| | G2P06 | A2D11 | | | |
| | G2P07 | A2P11 | | | |
| | G2P09 | A2P13 | | | |
| | G2P10 | A2G05 | | | |
| | G2P11 | A2G09 | | | |
| | G2P12 | A2P10 | | | |
| | G2P13 | A2D05 | | | |
| | G2S04 | A2G10 | | | |
| | G2S13 | A2B12 | | | |
| | H2M09 | GND | | | |
| | H2S03 | H2U09 | | | |
| | H2S04 | H2S09 | H2P04 | G2S09 | G2S10 |
| | G2J07 | K2P02 | | | |
| | G2G07 | A2P02 | | | |

| Test Error Pattern | Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|---|
| PAXE 04XX | G2B08 | G2G12 | | | |
| through | G2B09 | G2J12 | | | |
| PAXE 08XX | G2G02 | G2J06 | H2M05 | | |
| | H2G02 | H2M03 | | | |
| and | H2G12 | J2G12 | J2J05 | | |
| | H2M02 | H2M08 | | | |
| PAXE 11XX | H2M03 | H2G02 | | | |
| through | H2M10 | H2P10 | | | |
| PAXE 15XX | H2P05 | H2U11 | | | |
| | H2P07 | H2P09 | G2D12 | G2G04 | G2G05 |
| | H2P13 | H2S05 | | | |
| | H2U10 | GND | | | |
| | G2J10 | A2J04 | | | |

**Note:** *If an adapter is installed, the jumper at G2G07 to G2J07 MUST be removed.*

**Figure TA452-1 (Part 1 of 2). Model 1A Adapter Net Checklist (Adapter in 8140)**

| Test Error Pattern | Point A | Point B |
|---|---|---|
| PAXE 40XX<br>through<br>PAXE 43XX | G2B13 | H2P02 |
| | G2U11 | H2J04 |
| | G2U13 | H2G04 |
| | H2B02 | J2B02 |
| | H2B03 | J2B03 |
| | H2B04 | J2B04 |
| | H2B05 | J2B05 |
| | H2B07 | J2B07 |
| | H2B08 | J2B08 |
| | H2B09 | J2B09 |
| | H2B10 | J2B10 |
| | H2B12 | J2B12 |
| | H2B13 | J2B13 |
| | H2D02 | J2D02 |
| | H2D04 | J2D04 |
| | H2D05 | J2D05 |
| | H2D06 | J2D06 |
| | H2D07 | J2D07 |
| | H2D09 | J2D09 |
| | H2D10 | J2D10 |
| | H2D11 | J2D11 |
| | H2D12 | J2D12 |
| | H2D13 | J2D13 |
| | H2G05 | J2G05 |
| | H2G07 | J2G07 |
| | H2G08 | J2G08 |
| | H2G09 | J2G09 |
| | H2G10 | J2G10 |
| | H2G13 | J2G13 |
| | H2J02 | A2P09 |
| | H2J06 | J2J06 |
| | H2J07 | J2J07 |
| | H2J09 | J2J09 |
| | H2J10 | J2J10 |

| Test Error Pattern | Point A | Point B |
|---|---|---|
| PAXE 40XX<br>through<br>PAXE 43XX<br><br>(cont'd) | H2J11 | J2J11 |
| | H2J12 | J2J12 |
| | H2J13 | J2J13 |
| | H2M13 | H2U04 |
| | J2M02 | H6C02 |
| | J2M04 | H6D02 |
| | J2M07 | J1E11 |
| | J2M08 | H1B11 |
| | J2M09 | H1D11 |
| | J2M10 | J1A11 |
| | J2M12 | J6E04 |
| | J2M13 | K1A13 |
| | J2P02 | H6B02 |
| | J2P04 | K1B11 |
| | J2P06 | K1A11 |
| | J2P07 | J1D11 |
| | J2P09 | H1C11 |
| | J2P10 | H1E11 |
| | J2P11 | J1C11 |
| | J2P13 | J6C04 |
| | J2S02 | J6D04 |
| | J2S04 | J6B04 |
| | J2S05 | H5E04 |
| | J2S07 | J1C13 |
| | J2S08 | H1A13 |
| | J2S09 | H1C13 |
| | J2S10 | H1E13 |
| | J2S12 | J1D13 |
| | J2U02 | H6A04 |
| | J2U04 | K6A04 |
| | J2U05 | H6D04 |
| | J2U09 | H1B13 |
| | J2U10 | H1D13 |
| | J2U11 | J1B13 |
| | J2U13 | J1E13 |

| Test Error Pattern | Point A | Point B | Point C |
|---|---|---|---|
| PAXE 44XX<br>through<br>PAXE 56XX | G2J11 | A2D06 | |
| | G2S13 | A2B12 | |
| | G2U13 | H2G04 | |
| | H2B05 | J2B05 | |
| | H2D09 | J2D09 | |
| | H2G10 | J2G10 | |
| | H2G12 | J2G12 | J2J05 |
| | J2M05 | J6A02 | |
| | J2M09 | H1D11 | |
| | J2M12 | J6E04 | |
| | J2M13 | K1A13 | |
| | J2P04 | K1B11 | |
| | J2P05 | H6E02 | |
| | J2P11 | J1C11 | |
| | J2S10 | H1E13 | |
| | J2S13 | H6C04 | |
| | J2U04 | K6A04 | |
| | J2U06 | H6B04 | |

The net check points listed below do not cause test failures when both open and grounded, but should be checked to ensure proper tape logic continuity and operation.

| Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|
| G2B08 | G2G12 | | | |
| G2B13 | H2P02 | | | |
| G2D09 | G2P02 | H2M07 | | |
| G2G03 | A2B04 | | | |
| G2G08 | A2B05 | | | |
| G2G09 | A2J06 | | | |
| G2M02 | GND | | | |
| G2U11 | H2J04 | | | |
| H2D12 | J2D12 | | | |
| H2D13 | J2D13 | | | |
| H2G03 | H2P11 | | | |
| H2G13 | J2G13 | | | |
| H2M10 | H2P10 | | | |
| H2M12 | GND | | | |
| H2M13 | H2U04 | | | |
| H2S02 | A2B13 | | | |
| H2S04 | H2S09 | H2P04 | G2S09 | G2S10 |
| H2P05 | H2U11 | | | |
| J2S13 | H6C04 | | | |
| J2U06 | H6B04 | | | |
| G2J07 | K2P02 | | | |
| H2J02 | A2P09 | | | |

**Figure TA452-1 (Part 2 of 2). Model 1A Adapter Net checklist (Adapter in 8140)**

*3 8809 Model 1B Point-to-Point Net Checklist*

Find the test error message pattern in Figure TA452-1. All nets in the figure refer to all test error patterns indicated. Line entries reading from left to right are separate nets, and apply for any error listed in the test error pattern column. Check continuity between the test points, which are all located on the 8809 01A gate unless otherwise indicated. If any net does not indicate continuity, correct by wire-wrapping the points together.

| Test Error Pattern | Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|---|
| PA80 | D2B12 | B2J05 | Cable B3 | 01B-A2J05 | 01B-B2J05 |
| PA95 | D2D05 | B2G12 | Cable B3 | 01B-A2G12 | 01B-B2G12 |
| PA96 | D2G03 | B2B04 | Cable B2 | 01B-A2B04 | 01B-B2B04 |
| XXBC | D2G08 | B2B05 | Cable B2 | 01B-A2B05 | 01B-B2B05 |
| PAXE 01XX | D2G09 | B2J06 | Cable B3 | 01B-A2J06 | 01B-B2J06 |
| PAXE 02XX | D2J02 | B2D07 | Cable B2 | 01B-A2D07 | 01B-B2D07 |
| PAXE 03XX | D2J05 | B2D09 | Cable B2 | 01B-A2D09 | 01B-B2D09 |
| PAXE 09XX | D2J09 | B2G02 | Cable B3 | 01B-A2G02 | 01B-B2G02 |
| | D2J11 | B2D06 | Cable B2 | 01B-A2D06 | 01B-B2D06 |
| | D2M03 | B2B08 | Cable B2 | 01B-A2B08 | 01B-B2B08 |
| | D2M04 | B2M12 | Cable B4 | 01B-A2M12 | 01B-B2M12 |
| | D2M05 | B2B02 | Cable B2 | 01B-A2B02 | 01B-B2B02 |
| | D2M07 | B2J07 | Cable B3 | 01B-A2J07 | 01B-B2J07 |
| | D2M08 | B2P06 | Cable B4 | 01B-A2P06 | 01B-B2P06 |
| | D2M09 | B2G04 | Cable B3 | 01B-A2G04 | 01B-B2G04 |
| | D2M10 | B2D13 | Cable B2 | 01B-A2D13 | 01B-B2D13 |
| | D2M12 | B2B10 | Cable B2 | 01B-A2B10 | 01B-B2B10 |
| | D2M13 | B2G08 | Cable B3 | 01B-A2G08 | 01B-B2G08 |
| | D2P04 | B2J09 | Cable B3 | 01B-A2J09 | 01B-B2J09 |
| | D2P05 | B2M02 | Cable B4 | 01B-A2M02 | 01B-B2M02 |
| | D2P06 | B2D11 | Cable B3 | 01B-A2D11 | 01B-B2D11 |
| | D2P07 | B2P11 | Cable B4 | 01B-A2P11 | 01B-B2P11 |
| | D2P09 | B2P13 | Cable B4 | 01B-A2P13 | 01B-B2P13 |
| | D2P10 | B2G05 | Cable B3 | 01B-A2G05 | 01B-B2G05 |
| | D2P11 | B2G09 | Cable B3 | 01B-A2G09 | 01B-B2G09 |
| | D2P12 | B2P10 | Cable B4 | 01B-A2P10 | 01B-B2P10 |
| | D2P13 | B2D05 | Cable B2 | 01B-A2D05 | 01B-B2D05 |
| | D2S04 | B2G10 | Cable B3 | 01B-A2G10 | 01B-B2G10 |
| | D2S13 | B2B12 | Cable B2 | 01B-A2B12 | 01B-B2B12 |
| | D2G07 | B2P02 | Cable B4 | 01B-A2P02 | 01B-B2P02 |
| | D2G10 | B2J02 | Cable B3 | 01B-A2J02 | 01B-B2J02 |
| | D2J10 | B2J04 | Cable B3 | 01B-A2J04 | 01B-B2J04 |
| | D2B03 | E2M04 | | | |
| | D2B04 | D2D04 | | | |
| | D2D02 | E2P06 | | | |
| | D2D06 | E2P12 | | | |
| | D2D09 | D2P02 | E2M07 | | |
| | D2D12 | D2G04 | D2G05 | E2P07 | E2P09 |
| | D2G02 | D2J06 | E2M05 | | |
| | D2J04 | GND | | | |
| | D2S09 | D2S10 | E2S04 | E2S09 | E2P04 |
| | E2M09 | GND | | | |
| | E2S03 | E2U09 | | | |

| Test Error Pattern | Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|---|
| PAXE 04XX | D2J10 | B2J04 | Cable B3 | 01B-A2J04 | 01B-B2J04 |
| through | D2B08 | D2G12 | | | |
| PAXE 08XX | D2B09 | D2J12 | | | |
| | D2G02 | D2J06 | E2M05 | | |
| and | E2G02 | E2M03 | | | |
| | E2G12 | C2G12 | G2G12 | | |
| PAXE 11XX | E2U02 | C2J05 | G2J05 | | |
| through | E2M02 | E2M08 | | | |
| PAXE 15XX | E2M03 | E2G02 | | | |
| | E2M10 | E2P10 | | | |
| | E2P05 | E2U11 | | | |
| | E2P07 | E2P09 | D2D12 | D2G04 | D2G05 |
| | E2P13 | E2S05 | | | |
| | E2U10 | GND | | | |

**Figure TA453-1 (Part 1 of 2). Model 1B Adapter Net Checklist**

| Test Error Pattern | Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|---|
| PAXE 40XX | D2B13 | E2P02 | | | |
| through | D2U11 | E2J04 | | | |
| PAXE 43XX | D2U13 | E2G04 | | | |
| | E2B02 | C2B02 | G2B02 | | |
| | E2B03 | C2B03 | G2B03 | | |
| | E2B04 | C2B04 | G2B04 | | |
| | E2B05 | C2B05 | G2B05 | | |
| | E2B07 | C2B07 | G2B07 | | |
| | E2B08 | C2B08 | G2B08 | | |
| | E2B09 | C2B09 | G2B09 | | |
| | E2B10 | C2B10 | G2B10 | | |
| | E2B12 | C2B12 | G2B12 | | |
| | E2B13 | C2B13 | G2B13 | | |
| | E2D02 | C2D02 | G2D02 | | |
| | E2D04 | C2D04 | G2D04 | | |
| | E2D05 | C2D05 | G2D05 | | |
| | E2D06 | C2D06 | G2D06 | | |
| | E2D07 | C2D07 | G2D07 | | |
| | E2D09 | C2D09 | G2D09 | | |
| | E2D10 | C2D10 | G2D10 | | |
| | E2D11 | C2D11 | G2D11 | | |
| | E2D12 | C2D12 | G2D12 | | |
| | E2D13 | C2D13 | G2D13 | | |
| | E2G05 | C2G05 | G2G05 | | |
| | E2G07 | C2G07 | G2G07 | | |
| | E2G08 | C2G08 | G2G08 | | |
| | E2G09 | C2G09 | C2G09 | | |
| | E2G10 | C2G10 | G2G10 | | |
| | E2G13 | C2G13 | G2G13 | | |
| | E2J02 | B2P09 | Cable B4 | 01B-A2P09 | 01B-B2P09 |
| | E2J06 | C2J06 | G2J06 | | |
| | E2J07 | C2J07 | G2J07 | | |
| | E2J09 | C2J09 | G2J09 | | |
| | E2J10 | C2J10 | G2J10 | | |
| | E2J11 | C2J11 | G2J11 | | |
| | E2J12 | C2J12 | G2J12 | | |
| | E2J13 | C2J13 | T2J13 | | |
| | E2M13 | E2U04 | | | |

| Test Error Pattern | Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|---|
| PAXE 44XX | D2J11 | B2D06 | Cable B2 | 01B-A2D06 | 01B-B2D06 |
| through | D2S13 | B2B12 | Cable B2 | 01B-A2B12 | 01B-B2B12 |
| PAXE 56XX | D2U13 | E2G04 | | | |
| | E2B05 | C2B05 | G2B05 | | |
| | E2D09 | C2D09 | G2D09 | | |
| | E2G10 | C2G10 | G2G10 | | |
| | E2G12 | C2G12 | G2G12 | | |
| | E2U02 | C2J05 | G2J05 | | |

The net check points listed below do not cause test failures when both open and grounded, but should be checked to ensure proper tape logic continuity and operation.

| Point A | Point B | Point C | Point D | Point E |
|---|---|---|---|---|
| D2G03 | B2B04 | Cable B2 | 01B-A2B04 | 01B-B2B04 |
| D2G08 | B2B05 | Cable B2 | 01B-A2B05 | 01B-B2B05 |
| D2G09 | B2J06 | Cable B2 | 01B-A2J06 | 01B-B2J06 |
| E2S02 | B2B13 | Cable B2 | 01B-A2B13 | 01B-B2B13 |
| E2J02 | B2P09 | Cable B2 | 01B-A2P09 | 01B-B2P09 |
| D2B08 | D2G12 | | | |
| D2B13 | E2P02 | | | |
| D2D09 | D2P02 | E2M07 | | |
| D2M02 | GND | | | |
| D2U11 | E2J04 | | | |
| E2D12 | C2D12 | G2D12 | | |
| E2D13 | C2D13 | G2D13 | | |
| E2G03 | E2P11 | | | |
| E2G13 | C2G13 | G2G13 | | |
| E2M10 | E2P10 | | | |
| E2M12 | GND | | | |
| E2M13 | E2U04 | | | |
| E2S04 | E2S09 | E2P04 | D2S09 | D2S10 |
| E2P05 | E2U11 | | | |

**Figure TA453-1 (Part 2 of 2). Model 1B Adapter Net Checklist**

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## TA500 Console Messages

Each permanent error generates a console message to the control operator. The operator then refers to the system messages and codes manual for appropriate action. The following paragraphs show the format and content of the console messages for DPPX and DPCX.

## TA510 DPPX

There are nine different console messages, each representing a different category of error:

1. HDIT0052P
   PA= XX SCA= XXXX DT= XXXX TAPE MEDIA PROBLEM
   ERROR CODE= XXXX
2. HDIT0053P
   PA= XX SCA= XXXX DT= XXXX TAPE OVERRUN
   ERROR CODE= XXXX
3. HDIT0055P
   PA= XX SCA= XXXX DT= XXXX INCORRECT TAPE MODE
   ERROR CODE= XXXX
4. HDIT0056P
   PA= XX SCA = XXXX DT= XXXX TAPE MARKER SENSOR FAILURE
   –TAPE DRIVE DEACTIVATED–ERROR CODE= XXXX
5. HDIT0057P
   PA= XX SCA= XXXX DT= XXXX TAPE DATA UNSAFE–ERASE HEAD IS LIVE, REMOVE TAPE FROM UNIT WITHOUT MOVING IT PAST HEADS–TAPE DRIVE DEACTIVATED–ERROR CODE= XXXX
6. HDIV0051P
   PA= XX SCA= XXXX DT= XXXX LOGIC ADAPTER CARD ERROR–LOGIC CARD DEACTIVATED–ERROR CODE= XXXX
7. HDIV0054P
   PA= XX SCA= XXXX DT= XXXX DEVICE NOT READY–INTERVENTION REQUIRED–ERROR CODE= XXXX
8. HDIV0058P
   PA= XX SCA= XXXX DT= XXXX PERMANENT I/O ERROR–DEVICE DEACTIVATED–ERROR CODE= XXXX
9. HDIV0059P
   PA= XX SCA= XXXX DT= XXXX INTERNAL SEQUENCE ERROR–DEVICE DEACTIVATED–ERROR CODE= XXXX

Where:

PA = Physical address of the tape adapter
SCA = Secondary component address
DT = Device type
ERROR CODE = Tape adapter return code

Refer to the DPPX General Failure Index (Chapter 1, ST110) for associated action plans.

## TA520 DPCX

The DPCX console message has the following format:

XXXX-LA=nn FPID=nnnn LOC=nnnnn OPID=nn
I/O ERROR, COMPLETION CODE=nnn
ERROR CODE=xnn

Where:

XXXX = System message number (SMN).
LA = The logical address (nn) of the unit on which the failure occurred.
FPID = The functional program identification number (nnnn).
LOC = The address (nnnnn) of the instruction being performed when the error occurred.
OPID = The operator ID number (nn).
COMPLETION CODE = The code (nnn) assigned by the program to indicate the category of error that occurred (for example; media, tape drive, tape control).
ERROR CODE = x = 0 Error while not accessing a tape data set.
= 1 Error while processing a label for input.
= 2 Error while processing a label for output.
= 3 Error while reading from an opened data set.
= 4 Error while writing to an opened data set.
= nn Translated tape adapter return code (TARC) (in decimal)
The TARC is derived from the last two digits of the adapter return code (ARC) returned by the FDM. The TARC and the ARC are the same except when the ARC = 6X or EX. Then the ARC translates into 4X and 5X respectively. See TA333 for list of TARCs.

Refer to the DPCX General Failure Index (Chapter 1, ST210) for associated action plan.

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# Appendix A. Hexadecimal-to-Binary Conversion

# Appendix A. Hexadecimal-to-Binary Conversion

Hexadecimal messages consist of two to four hex values. Use the following chart to convert the hex value to a binary bit value:

| Hex Value | Binary Bits (0123 / 4567) |
|---|---|
| 0 | 0000 |
| 1 | 0001 |
| 2 | 0010 |
| 3 | 0011 |
| 4 | 0100 |
| 5 | 0101 |
| 6 | 0110 |
| 7 | 0111 |
| 8 | 1000 |
| 9 | 1001 |
| A | 1010 |
| B | 1011 |
| C | 1100 |
| D | 1101 |
| E | 1110 |
| F | 1111 |

Two hex values equal one byte of status or sense information. For example:

Status byte = 3A (hex).

| Status Byte | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Hex Representation | 3 | | | | A | | | |
| Binary Bits | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |

Active bits are 2, 3, 4, and 6.

8130/8140/8101
Maintenance Information

Order No. SY27-2521-3

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