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Maintenance Library

PSG	MIM	PCM*	MDM	ECM*	MSM*
INTRO MLX START ISOLATE REPAIR MD LOG PROG SC-FRU INDEX (MASTER)	TRANS LGND/GLOS LOC PWR CARR MAP SAFETY INDEX	VISUAL INDEX CATALOG NUMERIC INDEX	MICROFICHE CARD/CABLE/ VOLTAGE CHARTS A-BOARD LRM B-BOARD LRM C-BOARD LRM POWER DIAGRAMS RD INST	ECDs INDEX	HELP SENSE OPER DIAG INDEX
VOL. R05	VOL. R10	VOL. R20	VOL. R30	VOL. R40	VOL. R60

* These volumes are shipped in microfiche and are located in volume R30.

3380

Direct Access Storage Models J and K Maintenance Information

P/N 4519943 2 Sides
EC 475248 25Apr88

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Preface

The Maintenance Support Manual (MSM), Volume R60 of the maintenance library, is designed to help the IBM service representative maintain the IBM 3380 Direct Access Storage, Models AJ4, BJ4, AK4, and BK4.

When maintaining any of these models, use the IBM Maintenance Device diskette and the maintenance library manuals shipped with the machine, and/or the manuals shipped with the AJ4 or AK4 unit to which the machine and the IBM Maintenance Device connect.

Always start any maintenance action on a 3380 Model AJ4, BJ4, AK4, or BK4 by following the instructions in the PSG, Volume R05.

When a 3380 Model AJ4 or AK4 is connected to the same storage director as a 3380 Model AA4, AD4, or AE4, instructions in the MD or notes in this manual indicate when to use the information in the other 3380 maintenance library manuals.

In this manual, the following terms are used to simplify the distinction among the various 3380 models.

3380	= all 3380 models
3380-J	= 3380 AJ4, BJ4
3380-K	= 3380 AK4, BK4
3380-JK	= 3380 AJ4, BJ4, AK4, BK4
A unit	= 3380 AJ4, AK4
B unit	= 3380 BJ4, BK4

The complete model name will be used to specify a single model. (For example, 3380 Model AJ4.)

Maintenance Manual Ordering Procedure

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Parts of this manual can be ordered from the IBM San Jose plant by using the Wiring Diagram/Logic Page Request, Order No. Z150-0130 (U/M 015). In the logic-page columns, enter the part number **[1]**, and engineering change number **[2]** shown at the bottom of each page.

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How to Update this Manual

This manual is under engineering change control. Put pages in by part number **[1]** and page number **[3]**. The EC level and date are given in the EC history block on the first page of the part-numbered group of pages.

Related Publications

The following is a list of documents that may help to understand and/or repair the 3380-JK:

- *IBM 3380-JK Direct Access Storage Introduction*, GC26-4491
- *Using the IBM 3380-JK Direct Access Storage in an MVS Environment*, GC26-4492
- *Using the IBM 3380-JK Direct Access Storage in a VM Environment*, GC26-4493
- *Using the IBM 3380-JK Direct Access Storage in a VSE Environment*. GC26-4494
- *Maintaining IBM Disk Storage Media*, GC26-4495
- *Master Index*, GC26-4496
- *IBM 3880 Storage Control, Models 1, 2, 3, and 4 Reference Manual*, GA26-1661
- *Device Support Facilities: Primer for the User of IBM 3380 Direct Access Storage*, GC26-4498
- *IBM 3990 Storage Control Introduction*, GC32-0098
- *IBM 3990 Storage Control Planning, Installation, and Storage Administration Guide*, GA32-0100
- *IBM 3990 Storage Control Reference*, GA32-0099
- *Cache Device Administration*, GC35-0101

About This Manual

The Maintenance Support Manual (MSM) is used with the Product Service Guide (PSG) when servicing a 3380.

The MSM is divided into four sections, each with specific purposes. The sections are:

- HELP
- SENSE
- OPER
- DIAG

A brief description of each section follows.

HELP

This section supplies the customer engineer with DASD maintenance information that is not supplied in the guided maintenance package.

SENSE

This section contains the 3380-JK sense data descriptions that identify the contents of each format by messages, bytes, and bits. It supplies page references to additional information on each error symptom, along with the priority of service actions and the primary symptom code.

OPER

This section contains the theory of operation for the 3380-JK.

DIAG

This section contains the run procedures for each diagnostic routine, along with its associated isolation codes.

EC History of Front Matter

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Notes:

Ordering This Manual

At least one hard copy of this manual should be in each account. To order a hard copy of this manual. complete and return the Documentation Request card No. 927-8390 included with the microfiche located in Volume R30 of each machine. A hard copy will be sent to the address indicated on the card, either home, office, or account. This manual is not shipped in hard copy form with each machine because of the expected low usage and storage space requirements. No EC updates will be made to the hard copy, they must be ordered. The machine will continue to receive microfiche updates for ECs.

Introduction

This manual should not be used for servicing 3380-DE, it should solely be used to maintain 3380-JK.

The purpose of the HELP section is to provide the CE with DASD maintenance information that is not provided in the guided maintenance package. This material is most beneficial if it has been read and understood prior to the more difficult repair action.

> **Note:** *The term storage control is used as an overall term in this section to mean the functions within the 3880-3 storage director or the functions within the 3990 storage path.*

Contents

The contents of this section are as follows:

"Guided Maintenance Procedures Failure"
"General"
"Unguided Maintenance Documentation" on page HELP-4
"Intermittent Failure Checklist" on page HELP-5
"Solid Failure Checklist" on page HELP-6
"Error and Check Handling" on page HELP-8
"Analyze Format of Sense Data" on page HELP-11
"Service Aids" on page HELP-18

Guided Maintenance Procedures Failure

The guided maintenance procedures could fail for one of the following reasons:

- The MD symptom analysis procedure might have omitted this FRU (card, board, cable, top-card connector, and so on) because of the low probability of failure or an incorrect symptom priority assignment.
- The fault is not in the circuits being monitored or the detection circuitry, but in the error collection circuitry.

The following failures can occur, primarily during installation:

- The MD diskette is not compatible with the storage control functional diskette or, the use of a down level MD or storage control functional diskette.
- Incorrect cable lengths or loose cables. The maximum CTL-I cable length is 61 meters (200 feet).
- Incorrect subsystem physical configuration.
- String address incorrectly set.
- Improperly defined system parameters, such as, SYSGEN, IOCP, and UCWs.

These failures can occur at any time:

- Bent pins in a board or in a cable socket.
- Environment (temperature, humidity) out of spec.
- Wall power, voltage change, loss of phase, and so on.
- Open grounds, ground loops, and so on.
- A misinterpretation of MAP instructions by the CE.

General

The material under this heading provides overall guidance in servicing the 3380-JK.

Using the ECM with symptom codes

It is presumed that you will come to this manual to resolve a problem that the MD did not resolve.

The ECM Index lists primary symptom codes only. A primary symptom code is a symptom code that is generated if one and only one symptom (check, error, message, etc.) was created by a failure. Therefore, **not** all symptom codes that you receive in 3380-JK sense data will be listed or explained.

If you need to determine which symptom code the system was identifying, and the exact code is not listed, look for similar codes with the letter 'X' replacing some of the characters. The entries with 'X' follow all normal entries. For example, 9XXX would indicate all codes beginning with '9'. 9XXX would be the last symptom code listing with the first character of 9.

The symptom code does not always provide all the available information about a fault. With many faults, you must analyze the first 24 bytes of the sense before you can be fully aware of all the symptoms. The symptom code generator only uses the highest priority symptoms to develop a code and discards the remaining symptoms. Those remaining symptoms may be needed to point to the fault. See "To Analyze Format 1 (SC=9xxx)" on page HELP-13

Solid and Intermittent Checklists

Use the solid and intermittent checklists located in this section to help resolve problems.

- Intermittent failure checklist - page HELP-5
- Solid failure checklist - page HELP-6

Before using the checklists, an understanding of the following material is suggested.

Swapped Cards

Cards should not be swapped between devices or machines for the following reasons:

1. The probability of creating an additional problem on another machine is too great. The impact of this type of problem is unacceptable to both the customer and IBM.

2. Problems affecting the data integrity of a device can be propagated to another device or the system.

If any card swapping occurs, it must only be done in instances where you absolutely cannot impact the customer's system or the customer's data. For example, card swapping is allowed between devices during an installation.

Block FRU Replacement

Install card FRUs singly with a solid failure. If the replacement FRU does not fix the problem, remove it and try the next FRU in the FRU list.

The CE is expected to perform block FRU replacement for an intermittent failure. On the subsequent service call, if the first set of FRUs listed by the MD fails to correct the problem, the second set of suggested FRUs are to be installed. ***Do not remove the first set of FRUs at that time!***

Block FRU replacement on an intermittent failure will reduce the number of calls required to resolve a failure. An intermittent failure is a failure that the MD can not repeatedly detect.

Single Symptom

If multiple symptoms are available, do not use a single symptom, like a console message, to resolve a problem. A single symptom might mislead you. Collect all the available symptoms and take action only after understanding all of them.

Attack the permanent error symptoms first, then the temporary error symptoms.

The priority of Sense Formats is 7, 8, 1, 9, 4. The priority of each error symptom is assigned in the SENSE section.

EREP Release Level

The maintenance package for the 3380-JK requires the use of the Environmental Recording, Editing, and Printing (EREP) Program at Release 3.3.2 or later to be fully effective. EREP is an important tool that must be in place and running when it is needed for the analysis of the more complex DASD problem. If your customer has not installed EREP at Release Level 3.3.2 or later, provide the assistance necessary to help get it installed. Data Check problems are virtually impossible to resolve without the use of the system exception report, due to the way the 3380-JK and storage controls handle data errors.

In addition, the CE should be trained in the proper use of EREP reports. If you are not trained in the use of EREP at Release 2.1 or later, request training from your manager.

EREP in a Multisystem Environment

If your installation has more than one operating system, each system has a separate error reporting data set (ERDS). Merge the records from all ERDS onto a history data set and run EREP against the combined data. Only EREP reports, that contain all DASD error records, can provide you with a complete picture of the performance of the DASD. See the EREP manual, GC28-1378-1 for details.

Definitions

An intermittent failure is an error that cannot repeatedly be detected by the 3380-JK microdiagnostics. An intermittent failure service call can be initiated with either a permanent or temporary error indication.

A Permanent failure is an error that can be detected by the microdiagnostic. It will probably be a customer reported error and a console message or EREP should be available. A permanent error is an error that an error recovery procedure did not successfully recover from.

A temporary equipment check can only be discovered from an EREP report. A temporary equipment check never generates a console message. A temporary data or seek check has a console message and Log Rec entries only on threshold counter overflow. A temporary error is an error that an error recovery procedure did successfully recover from.

A permanent equipment check or data check generates both a console message and a Log Rec entry that can be examined with EREP.

A Primary Symptom Code is the symptom code that is generated if one and only one symptom (check, error, message, etc.) were created by a fault.

Track, Record, Area, Field

Track, a track has records written on it.

Record, a record can contain the following areas, a count area, a key area, and a data area.

Area, for example, a count area contains the following fields, a skip displacement field, CCHHR field, data length field, etc.

Field, for example, a CCHHR field contains the cylinder number, head number and the record number.

Failure boundary

Failure boundary definitions for this maintenance package are as follows:

Device - A failure pertaining to an actuator and its associated logic and/or media, regardless of which controllers are failing. Sense byte 4, bits 3 through 7 identify the device.

Drive - A failure pertaining to both devices associated with a single head-disk-assembly (HDA), regardless of which controllers are failing. Sense byte 4, bits 3 through 6 identify the drive.

Port - A failure pertaining to multiple devices on both HDA's and limited to a single port number (0, 1, 2, etc.) regardless of which controllers are failing (see note). Sense byte 4, bits 3 through 5 identify the port.

Controller - A failure of two or more devices on different ports and limited to a single controller (see note). Sense byte 4, bits 0 and 1 identify the path.

> **Note:** *If only one port is in use, the determination between port and controllers cannot be made. For this situation, the failure boundary in EREP is 'Unknown'.*

Unknown - The failure boundary cannot be determined.

Unguided Maintenance Documentation

The material under this heading describes the 3380-JK maintenance package sections that help resolve the problems that the guided maintenance package failed to resolve.

The SENSE Section

The SENSE section lays out the sense bytes by format providing bit definition and a reference to additional information about each symptom. It also provides priority to each error.

The DIAG Section

The DIAG section contains the following:

- Descriptions of diagnostics
- Isolation code (IC) descriptions
- IC error byte descriptions with cross references
- Description of diagnostic commands

The diagnostic descriptions contain information about the routines and about the parameters and run options. The descriptions include references to the commands used to test the machine functions and to the isolation codes that identify specific kinds of errors.

Each IC description lists the associated error bytes. With the English names for the bytes (not the byte and number), you can easily locate the IC error byte bit descriptions for additional information in the SENSE section. Where applicable, the names used are the same as those used in the SENSE section. This section also provides cross references to the Isolation Code E-bytes.

The commands that are described in the DIAG section are those special commands that are not used during usual customer operations. See "Diagnostic looping" on page HELP-22.

The OPER Section

The commands that are used in customer operations are described in the OPER section. The OPER section does not contain procedures to perform, it contains the theory of operation for the 3380-JK.

Error Condition Descriptions

The error condition descriptions (ECDs) are located in the Error Conditions Manual (ECM).

The ECDs are formatted in most cases as follows:

- Title or the name of the check
- What the check means
- How the check is indicated:
  - Primary Symptom Code
  - Sense Data
  - Checkpoint Code
- Where in the hardware or software the checker is located
- How the checker works
- When the checker works
- How the checker is reset
- Diagnostics
  - that will force the checker on, and
  - that exercise the function that the checker is checking
- References to data in other manuals
- Service aids (may be provided)
- Nets known to set the checker (may be provided)

Reference Diagrams

The reference diagrams (RDs), located in the Maintenance Diagrams Manual (MDM) can be used to help define the following:

1. The source of the always active check indication.
2. Identify how errors of each of the formats are collected.
3. Identify associated errors and their collection paths.

4. The potential fault boundary of a failure when a forced diagnostic error is not being detected.

Intermittent Failures

The number of repeat calls can be reduced with action on an intermittent failure. This is the failure that usually takes a little extra effort and time, to prevent future problems.

Finding an Intermittent Failure

The FRU list usually finds an intermittent logic failure. The items that are often missed are loose or poor connections, and power. Once the error has been analyzed, a list of possible failing connections should be compiled. Next, select a diagnostic that exercises the failing portion of the machine. While looping the diagnostic, stress the connections in whatever way possible. Scope the connections while stressing them and watch for a change in amplitude or the presence of noise. Scope the nets involved with this failure and compare them with the same nets on a working device. Often a difference can be detected and yet the failure is intermittent. The scope can be used to find an intermittent voltage problem also. Check the scope for a ripple or voltage fluctuation that does not show up on the meter.

Additional test equipment is available for an intermittent problem and should be considered. A logic analyzer can be hooked up to trigger on the error and capture the condition of the nets involved or in question before and after the failure. A voltage analyzer can monitor ac or dc voltages for spikes or fluctuations. The time stamps can be used to compare with other failure indication times.

Have all of the available resources been used? Do not overlook the RETAIN system, the branch office specialist, and the support center.

Intermittent Failure Checklist

The following checklist provides the recommended corrective actions to take if the MD maintenance package fails to isolate an intermittent failure. An intermittent failure is one where the microdiagnostics do not detect a fault, yet EREP or system console messages indicate a problem. The actions are in a suggested sequence. However, you may perform them out of sequence if you have identified a suspect area.

___ Verify the MD MAP instructions. If necessary, review the initial isolation steps to confirm that no errors occurred.

___ Review as much symptom information about the problem as possible from the following sources:

Console messages
Customer problem report
Customer run program output, for example, ICKDSF and EREP

___ From the collected data, determine if the correct symptom code and failure boundary was chosen for the initial and following repair actions.

___ Verify that the DASD subsystem is correctly configured. Determine if the cables to the device under test have been swapped (Logic exchanged bit active in device status-2 byte Byte 20, bit 4 of Format 1, 8, or 9).

___ Verify compatibility of the storage control functional diskette with the 3380-JK MD diskette.

___ If this is a newly installed machine, verify the following:

- The total lengths of the CTL-I interface cables do not exceed 61 meters (200 feet).
- The base plate ground check has been performed.

___ Verify the ground connection on cables that use ground connectors (both ends).

___ If the fault is confined or located within an identifiable area, replace all the FRUs within that area.

___ Verify that the fault is not in the error and status reporting logic.

— Order a logic board to have on hand in case you need it later. Continue isolating the failure.

— Run the diagnostics against associated devices (if not already done) to verify or possibly redefine the failure boundary.

— If the failure is in a single device, perform the B-board cable swap procedure to aid in the isolation between the HDA and its associated logic (see CARR-1 Entry Q).

— Analyze the EREP data for the initial error. Define each error bit using the SENSE and ECD sections. Read the ECD references to understand the meaning of functions being checked and to be able to identify potential contributing nets by net names.

If additional symptoms exist, analyze each of these additional symptoms carefully. Try to identify the commonality of FRUs or nets. Determine if there are additional FRUs that should be replaced.

— Examine each net and replace any FRUs on the net not previously replaced.

— Remove each of the replaced FRUs and carefully examine the sockets for bent or broken pins or foreign material on the pins or in the sockets. Check the associated top-card connectors for bent or broken pins or open land patterns. Check the sockets of associated cables for bent or broken pins.

— Inspect the board back panels for a visible problem such as a loose wire, wires too tight, foreign material, and so on.

— Use a digital meter to measure the correct value of each of the board voltage pins in the replaced FRUs. Do not use a scope. See PWR-1 Entry A for the voltage values of the pins.

— Scope all of the power supplies for ripple or noise. Do not use a meter. See "Voltage and Ripple Checking" on page HELP-20.

— Run the diagnostic suggested by the ECD. Select the loop and stop on the error option. Stress the cables associated with the symptom while looking for an error stop.

— Scope nets identified in the ECD as contributors to the symptom. Look for an unusual condition. Run the diagnostic on a good device or controller in the same machine and compare signals.

— Consider the use of a logic analyzer or a voltage analyzer to gather more information to isolate the intermittent failure.

Solid Failure Checklist

The following checklist provides the recommended corrective actions to take to repair a solid failure. The actions are in a suggested sequence. However, you may perform them out of sequence if you have identified a suspect area.

If additional symptom information is gained during any of the steps, return to any previous step that may have required that information, and repeat the step using the additional information.

— Verify the MD MAP instructions. If necessary, review the initial isolation to confirm that no errors were made.

— Verify the DASD subsystem configuration (2-path? 4-path? 1 string? 2 strings? 1-unit string? 4-unit string? and so on.) Determine if the cables to the device under test have been swapped (Logic Exchanged bit active in device status-2 byte: Byte 20, bit 4 of Format 1, 8, or 9).

— If the MD maintenance procedure required definition of the failure boundary, ensure that it was correctly defined. Review the initial isolation if necessary.

— If system sense data, from EREP or the console is available, compare the symptoms identified by the IC error bytes. If they are different, examine each bit of both the IC and the sense data to get a fuller understanding of the fault.

___ Verify compatibility of the storage control functional diskette with the 3380-JK MD diskette.

___ Identify all the symptoms indicated by the diagnostic error stop. Analyze each of the bits of the error stop to identify both the symptom and the boundary of the fault. Use the ECD section of the ECM.

___ If necessary, run the diagnostics on other devices and paths to positively identify the fault boundary.

___ If this is a newly installed machine, verify the following:

- The total cable lengths of the CTL-I interface cables does not exceed 61 meters (200 feet)
- The subsystem configuration
- The string addressing
- The base plate ground check has been performed
- Inspect for loose cables, cards, or top-card connectors
- The top-card connectors are not located correctly
- The cable plugging on controller board
- Verify the ground connection on cables that ground connectors (both ends).

___ If the fault is confined or located within an identifiable area, replace all the FRUs within that area.

___ Verify that the fault is not in the error and status reporting logic.

___ Order a logic board to have on hand in case you need it later. Continue isolating the error.

___ Run the diagnostics against associated devices (if not already done) to verify or possibly redefine the fault boundary.

___ If the failure is in a single device, perform the B-board cable swap procedure to aid in the isolation between the HDA and its associated logic (see CARR-1 Entry Q).

___ Analyze the initial and following IC stops using the ECDs. Become familiar with the functions being checked to be able to identify potential contributing nets by net names. This means that the ECDs must be understood and that ECD references are read if required.

Note: *If, in the following steps, additional symptoms are developed, it is expected that the new symptoms will be just as carefully analyzed to determine what is failing.*

___ Remove each of the replaced FRUs and carefully examine the sockets for bent or broken pins or foreign material on the pins or in the sockets. Check the associated top-card connectors for bent or broken pins or open land patterns. Check the sockets of associated cables for bent or broken pins.

Note: *Remember that there are cables on the pin side of the A-Board.*

Be especially careful when checking sockets that have three rows of pins, because pushed-in pins are very hard to see.

___ Inspect the board back panels for a visible problem such as a loose wire, wires too tight, foreign material, and so on.

___ Use a digital meter to measure the correct value of each of the board voltage pins in the replaced FRUS. See the voltage charts in the Maintenance Diagrams Manual (MDM), Volume R30 to identify the voltage pins associated with each FRU Do not use a scope. See PWR-1 Entry A for the voltage values of the pins.

___ Scope all of the power supplies for ripple or noise. Do not use a meter. See "Voltage and Ripple Checking" on page HELP-20.

___ With a diagnostic suggested by the ECD, loop the diagnostic without stopping on the error. Scope nets identified in the ECD as contributors to the symptom. Look for an unusual condition. Run the diagnostic on a

good device or controller in the same machine and compare signals.

Error and Check Handling

Propagation and Priority of Errors

Check circuits cannot always prevent further processing. Therefore, some errors may cause other errors to be reported to the system. The problem of determining which error is the real error and which error is the result of the real error can only be resolved by understanding the errors.

The MD uses a priority process to resolve this problem, but it is not always successful. The reason it is not always successful is that not all of the bits of the sense data are examined. Only the bits with the highest priority are used to develop a symptom code or an IC stop. Other bits that can indicate the true error may not be examined. It is up to you to determine if the unexamined sense bits are relevant to your problem.

Only the examination of all the sense bits and your understanding of their meaning will make it possible for you to distinguish real errors from the propagated errors.

Failure Indications and Symptom Gathering

There are many different methods used by customers to provide problem data to the CE. Verify that the MD symptom code you used matches the problem reported by the customer. It may provide some needed information such as a better understanding of failure boundaries.

Console Messages

If you initiated the call with only console messages, request that an EREP report be run for the failing string or strings. It is strongly recommended that you ask your customer to provide a current EREP for the failing machine with each 3380-JK trouble call. This starts a practice which ensures an available EREP report with each call and a quicker intermittent failure resolution. Also, EREP shows both temporary and permanent errors. You may get a significantly different view of the problem.

An equipment check or data check console message is only provided by the system for permanent errors. While this may be the only system indication, the use of the console message should be reserved as the primary source of error information for only those failures where it is impossible to collect EREP. You should primarily rely on the expanded detail of EREP reports for error data to make repairs.

EREP

If you started your call with EREP, a more careful look at EREP may be required.

1. Do you have both System Exception and the Event History Reports?
2. Have you searched and marked all the entries and collected all of the symptoms provided by the failing device?
3. Are other devices on the string failing?
4. If there is another string on the CTL-I interface, are there failures on that string also?
5. Do all of the devices on the string show usage?
6. What is the failure symptom? If there is more than one failure symptom, did you choose the one with the most PERMs?
7. Determine the time window. What time did the first error occur? The last error occur? On all failing devices?
8. Have you chosen the right error?

   The priority of symptom codes on 3380-JK are D, E, 9, 4 (or Format 7, 8, 1, 9, 4).

At the completion of your analysis of EREP reports, you should be ready to answer the following questions:

- What symptom has the most permanent or temporary indications? Be able to list the other symptoms.
- Are all or some of the devices failing? Be able to identify the failing devices. Identify those devices that are probably not failing.
- Was the correct symptom used on the initial MD call.

For more details on EREP, see the Environmental Recording, Editing, and Printing Program User's Guide and Reference manual, Order No. GC28-1378.

DASD Error Log

When EREP is not available, it may be advisable to examine each of the error logs. Details on how to run the error log function can be found in the LOG section of the Product Support Guide.

Each error log can store sixteen 32 byte entries for errors that occur on the associated storage director/storage path. On a 3990-3380-JK 4-path subsystem of two strings, there are eight error logs. All of the first 24 bytes of sense data are included in the 32 bytes.

The 3990 error logs have a time stamp indicating the difference in hours from the time the error log was retrieved and the time the error actually took place. The 3880 does not have a time stamp capability. Searching in the error logs with the MD minimally impacts customer operations.

If you use the DASD Error Logs, be aware that all errors are logged, including all retry attempts. Careful examination of the time stamp is required, because the logs may be old and not pertinent to this failure. A single log only provides the information from one path, and unless all paths are examined, incorrect fault boundary assumptions will be made, confusing rather that aiding in the isolation of the problem. In that no usage data is available, the absence of errors is no indication that the path if exercised would not also fail. Therefore, use EREP, if it is at all available, to overcome the shortcomings of the DASD Error Log.

Error Thresholds and Storage Control Retry

The 3380-JK machine design expects a very small number of temporary data and seek checks. These temporary checks are thresholded so that they essentially become transparent to the customer normal operations and thruput. Thresholding is set low enough to ensure no data loss, yet high enough to ensure good performance without unnecessary maintenance activity.

The storage control maintains a Data Check and a Seek Check counter for each device. The storage control performs the error recovery for data checks and seek checks without significant operating system Error Recovery Procedure assistance.

Permanent Data Checks and Seek Checks detected by the storage control error recovery procedure are reported to the operating system for ending the job, developing a console message, and developing an entry to the system error logs.

Data Checks

With each successful 3380-JK data check recovery, the storage control examines the device's data check and bytes read counters. If the bytes read counter reaches its maximum value before the data check counter reaches its threshold then both counters will be reset. However, if the check counter exceeds the threshold, the 3990 storage path logs the temporary data check and the next 23 data checks occurring on that device on any path of the storage control. The 3880-3 storage director logs the temporary data check and the next 23 data checks occurring on that device only through that storage director. The first record will have the First Error Logged bit active, byte 2 bit 2. The EREP Data Transfer Summary will use that bit to indicate which device tripped the threshold. The last check will have the Message to the Operator Bit active. That will signal the system ERP to develop a console message indicating logging is complete.

Threshold logging mode cannot be reset by the MD. Only an IML of the storage control can prematurely terminate the logging of the 24 temporary data checks.

Seek Checks

Seek check logging is similar to data check logging. The storage control counts the number of temporary seek errors and compares it to a predetermined number of motion seeks. If the motion seek counter reaches its maximum value before the seek check threshold is reached, both counters will be reset. The first seek check that causes the storage control to enter logging mode will be a Format 1 sense record. The information in byte 2, bit 2 will indicate First Log Error in addition to the seek check sense data. The storage control will log the next seven seek checks reported by the device in logging mode. With the eighth seek check, the storage control will set a bit in the sense to indicate to the system ERP to generate a console message indicating that threshold logging is complete.

Summary

Temporary Data Checks and Temporary Seek Checks that the storage control error recovery procedure has successfully recovered from are counted in the independent device counters. When the check count exceeds a predetermined threshold, the storage control reports the next 24 (temporary or permanent) Data Checks of the device, or the next 8 (temporary or permanent) Seek Checks on the failing device to the operating system.

The checks are reported as Environmental Data Present sense data on the next Start I/O command to the device. The error reporting does not occur in the current CCW.

Error Recovery

There are times when it is necessary to know how checks and errors are usually recovered. An additional source for that information is in the IBM 3880 Storage Control Description, Order No. GA26-1661. IBM 3990 Storage Control Reference, Order No. GA32-0099-0. The information is in the Error Recovery Procedures chapter under the following headings:

- Error Correction Function - Count, Key, and Data Devices
- Internal Retry
- Command Retry
- Error Condition Table - 3380

Data Check Error Recovery

Data Check Detection and Correction: The storage control buffers all data transferred during a read operation. The buffer is large enough to contain an entire track. Previous storage controls were only capable of buffering the HA, Count and Key areas. Correction for the data area occurred in the host processor main memory. With the 3880-3 and 3990 storage controls the correction of the data area will occur in the storage control.

Data Check Detection: On recognition of a data check from the End Op code of the controller, the storage control issues commands to the controller ECC logic to generate and send to the storage control the data correction syndromes. The storage control analyzes the syndromes to determine if the syndrome data provides sufficient information to correct the data read or if the data read is uncorrectable.

First

The storage control on recognition of a data check responds to the channel with retry status (unit check, channel end, and status modifier).

The channel on recognition of the retry status, decrements its CCW pointer to return the pointer to the failing command. It does not generate an I/O interrupt to the system.

Second

The storage control collects and analyzes the syndromes to determine if the data check is correctable or uncorrectable.

1. If the Data Check is correctable, the storage control applies the correction to the HA, Count, Key or Data area that is still in its buffer. It reorients itself to the failing record and raises Request In to the channel. The channel then reissues the last command. While the storage control transfers the buffered corrected data to the channel, it clocks over the area on the disk. The storage control and the channel then, without interruption, continue processing the remainder of the CCW string.

2. If the Data Check is uncorrectable, the storage control holds up Request In until it receives a Locate Interrupt from the device indicating that the failing record is in position to be reread. The channel then reissues the command and the storage control rereads the record. The channel overlays the previously read data in main memory with the reread data.

   The reread results in one of three conditions.

   a. The record is reread without error.

If the data area is correctly reread, the storage control continues with the CCW string and reacts as if no error occurred.

The data check will only be reported to the system if logging mode is active because of threshold overflow. The data check will be reported, with the environmental data bit on. At the next Start I/O to the storage control a unit check causes the ERP to collect sense from the storage control and develop a Format 4 sense record, which the ERP will then log.

b. A record is reread with a correctable data check.

   If the data area is reread with a data check and the storage control determines that the error was correctable, it corrects it within its buffer. Also, if logging mode is in effect because of threshold logging, it reports the data check for logging on the next Start I/O to the storage control.

c. A record is reread with an uncorrectable data error again.

   If the record reread is again uncorrectable, the storage control again responds to the channel with Retry Status. While the storage control is waiting for the start of the record for another retry, it steps its retry counter, examines the retry counter to determine if offset should be invoked for this retry and performs other housekeeping chores. With the Locate Interrupt from the device and the subsequent Request In from the storage control, the channel reissues the command.

   If the record is never successfully read, the storage control posts Unit Check to the system. The ERP performs a sense command and receives, from the storage control, a Format 4 sense record with the Data Check and Permanent bits set.

Offset

During the uncorrectable data check retries, the storage control instructs the device to apply offset to the read head. Offset moves the head first to one side of the center of the track for a retry effort, then to the other. Each sequence moves the head further and further from the center of the track. Every data check that is recovered with offset is logged, so, that with EREP, a correct analysis can be performed.

It is possible for an intermittent read data error, which is occurring often, to be reported as a servo track following problem.

Analyze Format of Sense Data

This is the procedure to analyze any format of sense data. Use this procedure to analyze console messages that contain sense data, the sense bytes of an EREP summary, and the EREP Event History report sense data.

> **Note:** *Keep in mind that valid error and status bits are dependent on proper reporting and correct operation of the error reporting path. Power faults anywhere on the path may cause invalid reporting of errors.*

The following steps show how to examine a single sense record type. A later section covers the analysis of multiple symptom sense records.

It is assumed that you are familiar with DASD EREP reports. It is also assumed that you are aware of the importance of determining usage before determining failure boundaries, since unselected devices cannot log errors.

First Locate the SENSE section of this manual.

Second Determine the subsystem path in use at the time of failure by examining the first 24 bytes of the sense record.

Format of the sense data is defined in byte 7 bits 0 through 3.

Subsystem ID or **Storage Director Physical ID** for Formats 1, 4, 7, 8, and 9, is in byte 21.

String ID is in byte 3 except for Format 4, where it is in byte 14.

Device ID is the low-order 5 bits of byte 4.

Path Used is in byte 4 bits 0 and 1.

If multiple sense records are available, attempt to define the boundary of the failure. Determine the following:

- If one or more than one device is failing. Byte 4, bits 3 through 7, remain the same if only one device is failing.
- If one or more than one drive is failing. Byte 4, bits 3 through 6, remain the same if only one drive is failing.
- If one or more than one port is failing. Byte 4, bits 3 through 5, remain the same if only one port is failing.
- If one or more controllers in the string are failing. Byte 4, bits 0 and 1, remain the same if only one controller in the string is failing.
- If one or both controllers on a CTL-I interface is failing. Byte 21 and Byte 3 remain the same if only one controller on the CTL-I is failing.

With the above in mind, you can see that if only a single sense data record is available, the important initial boundary definition cannot be made.

To determine if only one device is failing, decide if the failing devices have similar symptoms. Do not make that decision based only on one symptom code; base it on the same or similar symptoms. The problem of similar symptoms may require bit analysis of the sense data. Some bits are status indicators and some bits are error indicators. It is beneficial to know the difference. Be aware that some of the status indicators, when off, indicate an error condition.

Third With the format of the sense data, locate the correct format chart to define the bits.

The charts, in addition to the names of the error bytes and bits, indicate the usual condition of the bit. Pointers are provided to byte and bit descriptions in the SENSE section. Bit description text gives pointers to ECD text that provide additional details about the symptom.

Fourth Determine what type of error recovery action the storage control requested of the operating system by examining bytes 0 through 2. For example, an equipment check causes the operating system to save the first sense data, retry the operation ten additional times, and log in Log Rec the first error data and whether the recovery was successful (temporary error) or unsuccessful (permanent error).

Fifth Determine the priority of the sense data records. In general, Format 7 identifies errors that require the highest service priority. The format service priority sequence for 3380-JK is Format 7, 8, 1, 9, and 4. Therefore, take action on the highest priority format, yet be familiar with the lower priority errors.

Before performing further analysis, review "Error Thresholds and Storage Control Retry" on page HELP-9 if you are not completely familiar with 3380 error thresholds.

Sixth Carefully examine the combined EREP data and determine the following:

- The permanent and temporary errors
- The time the error or check was logged
- The host processor unit that collected the error data

If the initial symptom code chosen to repair the machine with the MD did not resolve the problem, re-examine the EREP data closely. If at anytime you determine that the initial symptom code was not the best choice and you have determined what the correct symptom code is, use the MD to provide you with the new FRU list.

Examine byte 7, bit 0 - 3. If the format of the data you wish to analyze is:

Format 1 go to "To Analyze Format 1 (SC=9xxx)" on page HELP-13.

Format 4 go to "To Analyze Format 4 (SC=4xxx)" on page HELP-14.

Format 7 go to "To Analyze Format 7 (SC=Dxxx)" on page HELP-16.

Format 8 go to "To Analyze Format 8 (SC=Exxx)" on page HELP-17.

Format 9 go to "To Analyze Format 9 (SC=9xxx)" on page HELP-14.

To Analyze Format 1 (SC=9xxx)

The following procedure examines the Format 1 errors in a priority manner. While the highest priority bits are examined first, ensure that all the bits are examined to get a complete view of the symptoms being reported. Do not stop at the first symptom. Review all of the symptoms in the sense record.

Byte 20, bit 6 (Device Logic Undervoltage Status)

When active, this bit indicates a device undervoltage condition. This bit is a status bit and will not create an equipment check but will create a unique symptom code. This bit can only be reported concurrently with an equipment check. It will not indicate missing voltages.

Byte 7 (Format and Message)

Examine byte 7 for format and message. Bits 0 through 3 should have only bit 3 active, indicating Format 1. If bits 4 through 7 are other than zero, the storage control microcode detected the error and the message code description can be found in the SENSE section.

If the message code is other than zero, the remaining sense data will not, in most instances, contain significant symptom information. If the device itself has detected an error condition, that condition normally results in message code zero.

Byte 19, bit 3 (Device Error).

If this bit is on because of a check-2 error, there should be a bit on in sense byte 11 (Device Check-2 Status) and that error should be pursued.

1. **If byte 19, bit 3 is not active:**

   - Examine byte 20, bit 1 (Servo Inhibit) and bit 7 (Seek Incomplete). If these bits are on, it can mean servo inhibit or seek incomplete are active by themselves. Examine byte 15 for a checkpoint log value that is an indication of the reason for either or both of these errors.

   - Examine byte 10, bit 3 (Device Sequence Complete). This status bit should be on to indicate that the device has completed a normal power on, including a rezero, a clean cycle and a warm up cycle. The servo mechanism should also be track following.

     If bit 3 is not active and the contents of byte 10 (Device Power Status) is equal to hexcode '0E', the device is in the 3-minute clean cycle.

   - Examine byte 20, bit 5 (Operator Panel Disable Switch). This status bit, when active, indicates that the Enable/Disable switch on the A unit operator panel is in the Disable position.

   - Examine byte 19, bit 4 (Online). This bit should be on to indicate that the device is ready for customer use.

- If bit 4 is off:
  - Examine byte 10, bit 6 (Motor Brake Latch). This bit should be on indicating that the device sequencer has picked the brake relay which releases the drive motor brake.
  - Examine byte 10, bit 4 (Motor Run Latch). This bit should be on which indicates that the device sequencer started the motor.
  - Examine byte 10, bit 5 (Spindle Control Bit 0). This bit should be on, to indicate that the drive motor and brake relays are picked.
  - Examine byte 10, bit 7 (Spindle Control Bit 1). This bit should be off, to indicate that the MSA relay is not picked. This relay is picked to start the drive motor and then dropped.

2. **If byte 19, bit 3 is active:**
   - Examine byte 11, bit 3 (Checkpoint Check). If this bit is on, examine the contents of byte 15. See the SENSE section, Format 1, Byte 15 for checkpoint descriptions on page SENSE-66.
   - Examine byte 11, bit 6 (Power Card Check). When this bit is active, it indicates that there is a failure within the card.
   - Examine byte 11, bit 1 (Servo Control Check). When this bit is active, it indicates that there is an internal failure in the servo control function.
   - Examine byte 11, bit 2 (RPS Check). A failure in this area would prevent the correct detection of index, guard bands, and sector compare.
   - Examine byte 11, bit 0 (Device Sequencer Check). If this bit is active, the device sequencer is failing and the sequencer cannot execute the power-on sequence.
   - Examine byte 11, bit 7 (Funnel Parity Check). The Funnel is in the data path from the device to the CDP Bus.

To Analyze Format 9 (SC=9xxx)

The following procedure examines the Format 9 errors in a priority manner. While the highest priority bits are examined first, ensure that all the bits are examined to get a complete view of the symptoms being reported. Do not stop at the first symptom. Review all of the symptoms in the sense record.

Byte 20, bit 6 (Device Logic Voltage Status)

When active, this bit indicates a device undervoltage condition. This bit is a status bit and will not create an equipment check, but will create a unique symptom code. It can only be reported concurrently with an equipment check. This bit will not indicate missing voltages.

Byte 7 (Format and Message)

Examine the contents of byte 7 for a message code. Bits 0 and 3 active indicate Format 9. If bits 4 through 7 are other than zero, the storage control microcode detected the error and the message code description can be found in the SENSE section.

For message codes 7, A, or E examine bytes 16 and 17, Track Physical Address Read, and compare with bytes 5 and 6, Seek Address.

Byte 11, bit 5 (Read/Write Check)

This bit indicates that some other sense bit is on in byte 12, 13, 14 or 18. See Figure 1 to determine the source of the error. As an example, if the error was byte 18, bit 2 (Multi-Function), byte 12, bit 1 would be set along with byte 13, bit 0 and byte 11, bit 5.

Byte 13, bit 4 (Servo Cable Check)

The servo cable brings servo signals from the disk read/write channel board to the controller.

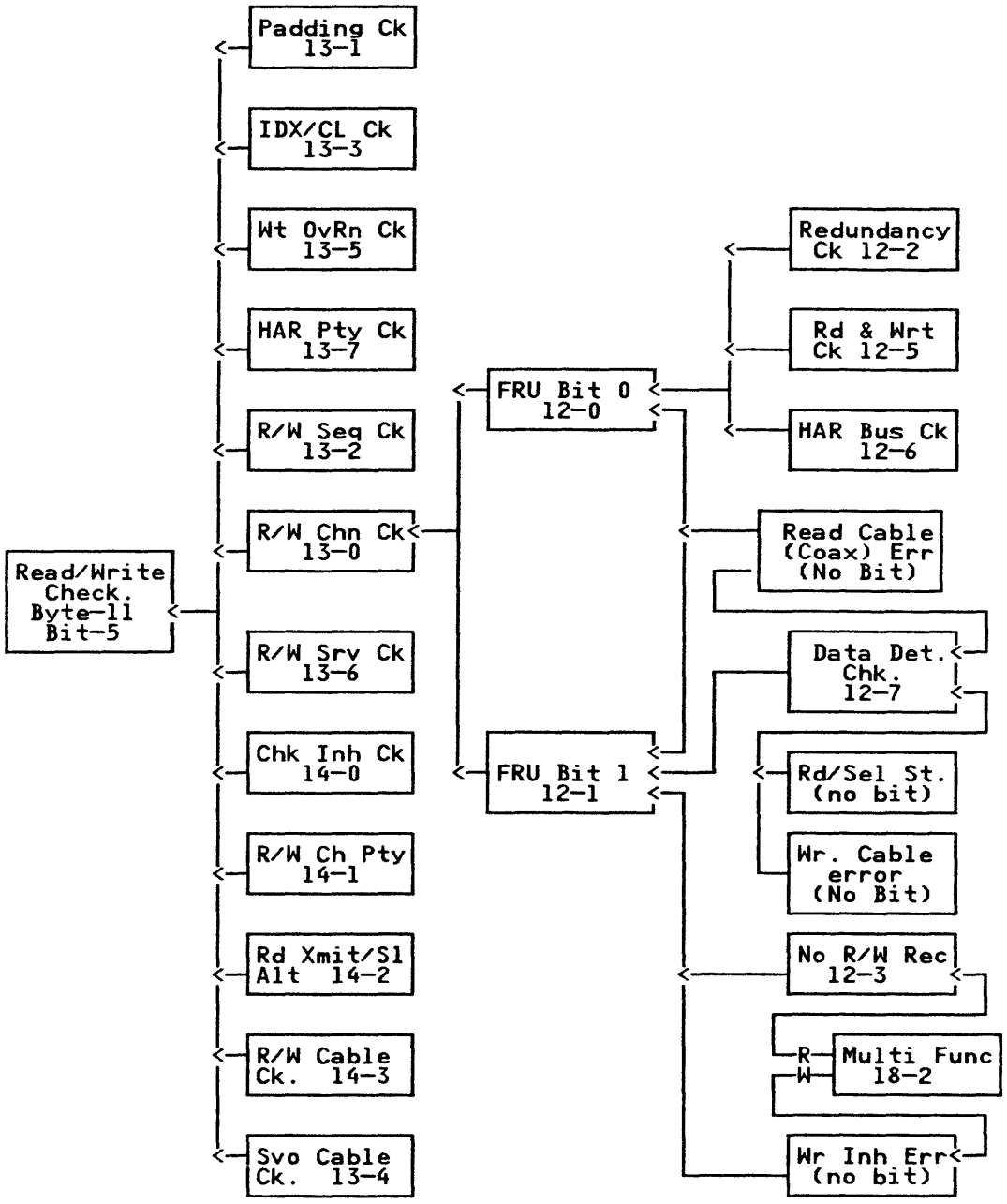

Figure 1. Read/Write Check, Byte 11, Bit 5

To Analyze Format 4 (SC=4xxx)

To fully understand the contents of this format, an understanding of Data Check error recovery is required. If you have not already done so, see the IBM 3880 Storage Control Description, Order No. GA26-1661, Error Recovery Procedures, Error Correction Function - Count, Key, and Data Devices.

Byte 7 (Format and Message Code)

Examine byte 7 for a format and message code. Bits 0 through 3 indicate the format, bits 4 through 7 identify areas where the data check occurred. See SENSE-16.

Bytes 22 and 23 (Symptom Code)

Examine bytes 22 and 23 for symptom codes. These bytes will indicate the area in which the data check occurred. It will also indicate whether the error was recoverable and if recovery required the use of offset. Byte 23 will also show whether an undervoltage condition existed at the time the data check was detected, whether track following was lost, and whether a No Read Data condition occurred.

Byte 1 (Unit Check Description)

Examine byte 1. If bit 0, the permanent error bit, is not active, it indicates that the storage control error recovery procedure was able to successfully recover the data. In this case, byte 2 bit 3, Environmental Data Present, will also be active in most instances. It is active to indicate that the storage control and the Operating System Error Recovery Procedure did not log the Format 4 data check during the data check recovery. The storage control waits until the next Start I/O command to the device to have the data check logged with the Environmental Data Present indication by the operating system. This logging occurs only if the temporary data check threshold for the device has been exceeded.

Byte 15 (Head Offset Value)

Examine Byte 15. If any of bits 0 through 3 are active, it indicates that head offset was required to successfully recover the record.

Bytes 5 and 6 (Head and Cylinder Address)

Bytes 5 and 6 indicate which head and cylinder address the storage control sent the device actuator for the last seek command.

Bytes 8 through 12 (Record ID)

Bytes 8 through 12 provide the last cylinder, head, and record address read from the disk before, or during, the read with the data check. This data may be unreliable on HA or Count area errors.

Single Error Records

The analysis of a single Format 4 record does not provide very much significant hardware fault information. The EREP System Exception Report Summaries provide a better analysis tool.

Multiple Error Records

For multiple error records, it is suggested that the EREP DASD Data Transfer Summaries be used to identify failing data paths and failing data tracks.

To Analyze Format 7 (SC=Dxxx)

The following procedure examines the Format 7 errors in a priority manner. While the highest priority bits are examined first, ensure that all the bits are examined to get a complete view of the symptoms being reported. Do not stop at the first symptom. Review all of the symptoms in the sense record.

Controller RCC Transfer Status

Examine byte 17 bit 0 for the controller addressed as 0 and byte 19 bit 0 for the controller addressed as 1 for a Controller Undervoltage condition. Zero is the active failing state and 1 is the normal state. This is a status bit and can only report concurrently with a Format 7 symptom code, not by itself. It also cannot report a missing voltage.

Byte 7 (Format and Message)

Examine byte 7 for a message code. If the message code is not zero, the storage control microcode detected an error condition.

Byte 10 (DTI/XES Register)

Examine byte 10, bits 0 through 3. If any of these bits are active, it indicates an error condition detected by the storage control. The low-order bits indicate the status of Tag In before sense collection.

Byte 3 (String ID)

Byte 3 is the string ID of the controller that initiated a connection check alert (CCA) or the ID of the controller the storage control suspects is having the problem indicated in the byte 7 message code.

> **Note:** *If the String ID in byte 3 is hexcode '00' or 'FF', it is invalid.*

Byte 11 (Connection Check Alert and Power Status)

Examine Byte 11. Bits 0 and 1 identify the controller on the CTL-I that had a controller check-1 condition. Byte 11, bit 0 and byte 17, bit 6 active together certify the error bits in bytes 12, 13, 16, and 17 for the controller addressed as 0. Byte 11, bit 1 and byte 19, bit 6 active together certify the error bits in byte 14, 15, 18, and 19 for the controller addressed as 1.

Controller Check-1 Status

Bytes 12 and 13 (Controller 0 Check-1 Status)
Sense bytes 12 and 13 have the Check-1 error information for the Controller addressed as 0.

Bytes 14 and 15 (Controller 1 Check-1 Status)
Sense bytes 14 and 15 have the Check-1 error information for the Controller addressed as 1.: Active bits in byte 12 or 13 and byte 14 or 15 indicate failures in both controllers on the CTL-I interface.

Path and Device Physical Identifier

CDP interface tag sequence errors can cause Format 7 errors. Examine byte 4 of several sense records and determine if more than one device address on a port is failing.

From usage data, determine which of the devices on the string was used.

Microcode Detected Errors

Examine byte 16 for Controller addressed as 0 and byte 18 for Controller addressed as 1 for controller sequencer microcode detected faults. If either of the bytes have other than hexcode '0A', refer to SENSE-80 for additional details.

Power Status

Examine byte 11 bit 6 and byte 17 bit 4 for Controller addressed as 0 and byte 11 bit 7 and byte 19 bit 4 for Controller addressed as 1 for Controller correct power indications at the time of failure. If any of these bits are inactive, refer to SENSE-78 and SENSE-81 for further details.

Successful Transfer Complete

Examine byte 17 bit 6 and byte 19 bit 6. If bit 6 is active, it indicates that the controller successfully transferred its connection check alert (CCA) data to the storage control for assembly into sense data.

To Analyze Format 8 (SC=Exxx)

The following procedure examines the Format 8 errors in a priority manner. While the highest priority bits are examined first, ensure that all the bits are examined to get a complete view of the symptoms being reported. Do not stop at the first symptom. Review all of the symptoms in the sense record.

Byte 11, bit 7 (Controller Undervoltage Test)

Examine byte 11, bit 7. When active, this bit indicates a controller undervoltage condition. This bit is a status bit and will not create an equipment check, but will create a unique symptom code. It can only be reported concurrently with an equipment check. It will not indicate missing voltages.

Byte 7 (Format and Message)

Examine byte 7 for a message code. If the message code is not zero, the storage control microcode detected an error condition.

If the message code is other than zero, in almost all instances, the remaining sense data will not contain significant symptom information. If the controller itself has detected an error condition, that condition results in a message code of zero.

Byte 10, bits 4 through 7 (CTL-I Tag-In)

Examine byte 10, bits 4 through 7. The low-order bits indicate the status of Tag In before sense collection.

Byte 16, bit 0 (DTB Bus Out Parity Check)

Examine Byte 16, bit 0 which identifies bidirectional CTL-I Bus Out problems.

Controller Fault Log

Examine and identify all active bits in bytes 11 through 17. These bytes are collected as a result of a Sense Fault Log Command. If the storage control determines that a fault log is not valid, it substitutes a hexcode 'FF' for the fault log value.

Only examine byte 15 when attached to 3880-3.

Byte 18 (Controller Sequencer Microcode Detected Check 2)

Examine Byte 18. If byte 9 contains an End Op code of 12 then the controller sequencer microcode detected an error. If byte 9 does not equal 12 byte 18 will contain, in most instances, the last Read/Write command on the CTL-I. When the high order bit of the byte is active it indicates that there was an undervoltage condition at the time of the microcode detected error. See SENSE-87 for further details.

Byte 17, bit 4 (Selected Device Check-1)

Determine if you have a Device Check-1 by examining byte 17 bit 4. To determine the device, use the chart in byte 14 (Controller Fault Log D) on SENSE-44. There are 8 different bits from 2 different bytes identifying which of a potential 64 devices you are examining. Plan to resolve the controller checks first.

Bytes 19 and 20 (Device Status)

Bytes 19 and 20 provide an indication of the status of the device at the time of sense collection.

Analysis with multiple ECDs

There will often be multiple error symptoms. To resolve these multiple symptom indications, try to determine the commonality of the symptoms. That commonality usually points to the failure area. What makes the task more difficult is fault propagation. If you do not understand general machine operation, fault propagation may become a problem. In that case, call for assistance.

Read each ECD carefully along with any suggested references and try to become familiar with both the error condition and expected operation. When comparing the error conditions, determine what is common in each of the symptoms.

Service Aids

The 0F0X Symptom (Format 0)

Format 0 is composed of all program or system check failures. These checks usually occur in the channel or the channel side of the channel interface, but are detected by the storage control.

To start problem determination break down the bits of sense bytes 0 and 1 to determine the type of failure. (Command Reject, Intervention Required, Write Inhibit etc.) With this information, refer to the storage control maintenance manuals for an explanation of the failure. In the same manuals, under Format 0 Messages, review the message indicated by sense byte 7. This will explain why the storage control returned the 0F0X Symptom Code. Listed below are possible causes, suggested ways to continue problem determination and fixes to the earlier 3380's. (Stage 1/2 and Model D/E)

Command Reject (Sense Byte 0, Bit 0)

If the failure can be easily recreated, use the system's CCW traces for further problem determination.

The following is a list of failures that caused Command Rejects on the earlier 3380's:

- Overlapping channel unit addresses (CUAs) on the channel interface.
- Channel control card in the system.
- Controller DPS card (if installed).
- The CTL-I interface cable connected incorrectly between controllers. (Not a valid configuration. See the installation instructions).

Intervention Required (Sense Byte 0, Bit 1)

Intervention Required console messages contain only sense bytes 0 through 6. The remainder of the sense record is not sent to the console. EREP reports do not contain Intervention Required messages. The error logs will contain all 24 bytes of the Intervention Required sense record. Disregard all but bytes 0 through 6 of that record.

Intervention Required on a 3380 is set when the device:

- Operator Panel Enable/Disable switch is set to Disable.
- Is performing warm up. (Busy device status only to the storage control, Intervention Required to the system)
- Is performing power off. (Busy device status only to the storage control, Intervention Required to the system)
- Is in CE mode.
- Is not installed.

Intervention Required is not set when the device:

- Motor switch is off. The storage control should note from the Device Status that the On Line bit inactive with the operator panel Disable switch bit inactive, (an inactive bit means the switch is set at Enable) indicates an equipment check.
- Fails to respond to selection and the configuration switches are correctly set. With correctly set configuration switches, the error condition that can cause the device not to respond causes an equipment check and logging.
- Status has the On Line bit inactive with the operator panel Disable switch set to Disable. This is an equipment check condition on 3380.

Overrun (Sense Byte 0, Bit 5)

The following is a list of failures that caused Overruns on the earlier 3380's:

- ADT and CSR cards in the storage control.
- UCW's or the IOCP incorrect at the system.
- Channel speed switches set wrong in the storage control.

Invalid Track Format (Sense Byte 1, Bit 1)

On the earlier 3380's, an Invalid Track Format was caused by running the wrong level of ICKDSF program for the machine. Breaking down sense bytes 5 and 6, the cylinder number was used to determine if this was the cause of the failure. If the cylinder number was for the CE cylinder of another model, then the wrong level of ICKDSF was being used.

No Record Found (Sense Byte 1, Bit 0)

This condition is reported to the operating system when two Index signals have been detected in the same CCW chain without an intervening read operation in the home address area or data area, or without an intervening write, sense, or control command.

There are some programming strategies that use No Record Found as a search criterion, therefore these are not errors and are not logged.

File Protect (Sense Byte 1, Bit 5)

By reading the Format 0 messages for this failure you see that it is most likely a programming problem. If the failure can easily be recreated without impacting the customer's operation, activate the system's CCW trace for further problem determination.

Write Inhibit (Sense Byte 1, Bit 6)

If sense bytes 0 and 1 have a value of hexcode '1002', Write Inhibit and Equipment Check active, refer to the PSG index for Write Inhibit and follow those procedures.

If Write Inhibit is active by itself, start the internal storage control trace. Have the trace stop on the 0F00 Symptom Code.

Motor Control Errors

The Motor Run Relay, the Motor Sequence Assembly (MSA or Soft Start) Relay, and the Motor Brake Relay are controlled by the Common Power card. This card in turn is getting relay control commands from both devices within a drive.

If a motor control problem is reported against one device, the failure could be in the opposite device. A check of the companion path and device should be performed when doing that type of problem determination.

Failures in error and status reporting logic

Consider faults in the error and status reporting logic whenever:

1. You cannot repair the problem after replacing all the FRUs associated with the symptom.

   The problem may not be the indicated error but the error reporting logic.

2. A hot error bit condition exists.

   Multiple errors are indicated for a device or controller with the same bit active in different sense bytes.

   An active error assembler net can cause the same bit to be active through multiple bytes of the sense data. In this case, suspect the status reporting logic and not the symptoms themselves.

3. A missing sense bit or a diagnostic IC indicates a forced error is not being reported.

   Controller and Device Check-2 and Device Check-1 error indications occur without specific errors being reported in the sense bytes.

The error reporting path and the error sensing paths are in most instances independent on the 3380-JK. When examining the status and error collection logic, also suspect gates of the error bytes stuck at either an active or inactive level. Examine the error reporting logic on the Reference Diagrams for each of the check conditions to develop a problem resolution strategy for each of the above situations. The symptom Reference Diagrams in the MDM are referenced from the SENSE, IC, and ECD sections dependent upon the error symptom.

Voltage and Ripple Checking

Go to the PWR section, Entry A, for the voltage pins and the voltage values for board voltages and ripple limits.

Check the voltage pins on the error checker FRU and on the FRUs that were replaced. See the reference diagrams to determine the checker FRU. If the voltage measured is questionable, compare it to the same pin on an operating device. If a voltage is out of tolerance, it causes the weakest circuit to fail first but may affect other circuits later. The following questions are provided as aids to potential failure areas.

1. If a voltage level is wrong, where does it come from?

2. Is the voltage developed on the card or does it come from a voltage net on the board? See the board ALD page AA000 index and find the Voltage/Ground Service page.

3. Why is the voltage incorrect?

4. Is there a FRU dragging the voltage down?

5. Was a voltage net blown because of a short on a card?

6. Check all the voltages on a power boundary. If multiple voltages are incorrect, look for the common component, a transformer, a resonant capacitor, etc.

7. Use a scope to measure the amount of ripple.

8. Use a digital meter to measure voltage levels.

No Sense Data Failures

The following list provides only an initial understanding of the problems. Do not waste time by delaying a call for assistance if it is required.

A Paging Pack Error

Usually errors on paging devices result in Hard Wait states by the operating system. Help from the customer Systems Programming personnel or similar help is required to resolve the failing device address. Once the device address is obtained, use the Subsystem Log (See START-1, Entry C, of the Product Service Guide (PSG) for procedures) to obtain the sense data of the failure.

Missing Interrupts

Missing interrupts have been known to occur because the actuator is not arriving at a desired track and the storage control Error Recovery Procedure is performing retries. Because of a Rezero operation, the retries take such a long period of time, a time-out occurs.

In an environment that has multiple systems with shared DASD, a missing interrupt can be caused by the imprudent setting of the Reserve command. For example, system A starts a job that needs device 1, then device 2. System B starts a job that needs device 2 and then device 1. If the reserves are not issued simultaneously at the start of the job but are issued only when the device is needed, system A attempts to reserve device 2 in the middle of its job, while at the same time system B attempts to reserve device 1. This can result in system management indicating missing interrupts.

On the earlier 3380's, (stage 1/2, Model D/E) Missing Interrupts were also caused by a Controller DPS card.

Slow System

- No obvious symptoms to the CE. No console or EREP messages. Slow response time is recognized by users and or the system operator. You may be informed by the customer programmers that the Control Unit Busy response or Device Busy response is occurring at a high rate.

- For Control Unit Busy, there is no quick isolation possible in most instances. A trace of current operations is probably necessary to identify the cause of the problem.

- For Device Busy, you can suspect a Device Port/RW Control card or device Sequencer/Servo/RPS card. Promptly call for assistance if replacing these cards did not resolve the problem.

- There has been an instance when the DHPLO card in the controller has caused a drive to waste a full revolution with almost every operation.

- A controller that is failing to detect an Address Mark. This causes the drives to always go to Index and space count out to the desired record. This can be caused by the Clock/SERDES/ECC card in the controller. Device Diagnostics should catch the fault.

- Always look for recent changes to the computer room, both in the software area and the hardware configuration.

ABEND

Look at the device address associated with the ABEND and test that device.

Look in the EREP Event History Report to find any errors, even temporary, that are associated with the JOB ID that had the ABEND.

Condition Code 1

Condition Code 1 can be set when the DPS arrays are mismatched.

Condition Code 3

Usually, when the operating system attempts to select a device, the channel puts the Unit Address on channel Bus Out. The storage control, on detecting its address, blocks the propagation of channel Select Out. The storage control attempts to select the addressed device by putting the device and controller address on CTL-I Bus Out and raising a Select tag. The controller, on recognition of its address, responds to the storage control.

The channel posts a Condition Code 3 when it receives a Select In tag in response to a Select Out tag. If none of the attached storage control units capture Select Out, the Channel sees Select In.

Condition Code 3 is set when:

1. The storage control times out waiting for the controller to respond. It then propagates Select Out.
2. The storage control fails to recognize its address and fails to block the propagation of Select Out.
3. No installed storage control has the address the channel has placed on channel Bus Out.
4. No installed controller has an address the storage control placed on CTL-I Bus Out. The storage control will time out.

Condition Code 3 is not set:

1. If the device fails to respond to a controller selection. A Format 1, message 5, Device Does Not Respond To Selection, is set.

Diagnostic looping

If the failure can be reproduced with a diagnostic, loop the diagnostic and use the scope.

Scope the input and output net listed in the ECDs. Compare what you see on a failing device with the pins on a working device.

Scoping

All of the logic on the 3380 is not 0 volts down level to +5 volts up level.

Signals from the HDA may have to be examined with a scope differentially, to see the true condition of the signal.

Scope the nets involved with the failure and compare them with the same nets on a working device. Quite often the difference of signal level or signal shapes can be observed on the scope without regard to a sync point.

EC History of Help Section

EC HISTORY OF P/N 4519946			
EC Number	Date Of EC	EC Number	Date Of EC
475245	14Nov86	475248	25Apr88
475246	21Jul87		
475247	11Sep87		

Notes:

3380-JK and 3380-DE Differences

There are many differences between the 3380-DE and 3380-JK. While the machines may look very similar, the reader is cautioned not to use these sense data descriptions in place of the 3380-DE Sense description text and not to use 3380-DE manuals to resolve 3380-JK problems.

Sense Data Introduction

The following discussion assumes that you have read the HELP section.

A 3380-JK subsystem needs an operating system with error recovery procedures (ERP) for error handling and recovery.

Errors in a 3380-JK subsystem are reported to the operating system as sense data records. Each record contains 24 or 32 bytes in one of ten different formats. When 3380-JK is attached to a 3880 Storage Control it uses a 24 byte sense format. When 3380-JK is attached to 3990 Storage Control, it has a 32 byte format. These additional bytes are used by the 3990 subsystem to perform subsystem error recovery actions.

Byte 7, bits 0-3, of each sense record, identify the format type of the sense record. Bits 4-7 of byte 7 is the message code of the format.

Only seven of the ten formats are used to report 3380-JK status. The remaining three formats are used to report Storage Control status only.

The formats for reporting 3380-JK status are:

- Format 0 — System checks and programming errors. This format has no 3380-JK hardware checks. It only contains storage control microcode detected errors.
- Format 1 — Device check 2 errors and servomechanism errors except for Read/Write checks.
- Format 4 — Data checks
- Format 5 — Not logged with 3380-JK
- Format 6 — Usage statistics and Control Unit overrun error statistics. This format has no 3380-JK hardware checks.
- Format 7 — Controller check 1 errors
- Format 8 — Controller check 2 and device check 1 errors
- Format 9 — Device check 2 read/write errors and Storage Control detected device seek errors.

Note: *Check 1 faults interfere with communications and cannot be reported through the normal communication path. Check 2 faults are faults outside the communications path and can be reported through the normal communication path.*

Format 0 gives messages to the operator of the system connected at the time of the error. If byte 1, bit 3 is on, and byte 7 is equal to hex 01 or hex 02, a 3380-JK message is indicated. Any other conditions indicate 3880 or system messages.

Formats 2 and 3 usually indicate storage control errors and are not described in this SENSE section. For more information about format 0 and for information about formats 2 and 3, see the storage control maintenance library.

For byte and bit meaning summaries by format, see the following pages in this section.

Format 1 see SENSE-4
Format 4 see SENSE-14
Format 5 see SENSE-22
Format 6 see SENSE-29
Format 7 see SENSE-31
Format 8 see SENSE-40

Format 9 see SENSE-50

The 3380-JK diagnostics also generate error bytes that have the same bit assignments and names as the error bytes collected in sense data. References are made to the SENSE section for bit identification.

Symptom Code Assignments by Sense Format

The first character of the symptom code identifies the format of the sense data. The maintenance package developers, in order to ensure that the CE would not be confused by similar symptom codes for the different models of the 3380, assigned the following codes:

1XXX for Format 1 of 3380 Stage 1 and 2
4XYY for Format 4 of 3380-JK (except 49XX)
49XX for Format 4 of 3380 Stage 1 and 2, and DE
5X5X for Format 5 of 3380 Stage 1 and 2, and DE
60XX for Format 1 of 3380 Stage 1 and 2
61XX for Format 8 of 3380 Stage 1 and 2
7XXX for Format 7 of 3380 Stage 1 and 2
8XXX for Format 8 of 3380 Stage 1 and 2
AXXX for Format 1 of 3380-DE
BXXX for Format 7 of 3380-DE
CXXX for Format 8 of 3380-DE
9XXX for Formats 1 and 9 of 3380-JK
DXXX for Format 7 of 3380-JK
EXXX for Format 8 of 3380-JK

The remaining symptom codes, 0XXX, 2XXX, 3XXX and 6(2-9)XX, belong to the storage control's sense data.

Format, Byte, and Bit Table Headings

The 3380-JK sense data descriptions are assembled in the following tabular form for quick identification of each of the sense bits.

(1)**Fmt X - Byte X** (2)**Byte Name** (3)**Reference**

1) The format number and the byte number.

2) The name assigned to the byte.

3) Reference to additional text about the byte as a whole.

(4)**Bit** (5)**N** (6)**Prty** (7)**PSC** (8)**Bit Name** (9)**Reference**

4) Bit number, or with the term Equals, the hexadecimal value of the byte.

5) N is the normal condition of the bit on a 3380-JK that is ready and online. Some bits should be active at the time of each sense collection. They are indicated with a 1. Others should always be inactive and they are indicated with a 0.

6) Priority. The smaller the value of this number, the higher the priority. Because some faults cause symptoms to be propagated, the priority provides the indication of which symptoms should be investigated first. However, do not ignore the other symptoms with higher numbered priorities or symptoms that do not have a priority assignment.

7) Primary Symptom Code. The symptom code that would be generated if this symptom and only this symptom were active.

8) Name assigned to the bit.

9) Indicates where additional text describing the bit is located.

Format 1

Format 1 is generated when one of the following conditions is encountered:

- Detection of a device equipment check that meets one of the following conditions:

  - Byte 11 is not x'04' or x'00'. (x'04' is Read/Write Check.)

  - Byte 11 is x'00' and the error is not a microcode detected device seek check.

  In this case, Equipment Check (byte 0, bit 3) is set. If the error is detected on an asynchronous operation, byte 2 bit 3 (environmental data present) is also set. Byte 1, bit 0 (permanent error) is set if the internal retries (if performed) are not successful.

- Detection of a permanent device logic seek check. Equipment Check (byte 0, bit 3) and Permanent Error (byte 1, bit 0) are set. The message code in byte 7 may specify a Seek Error. If the error occurred on an asynchronous operation, byte 2, bit 3 (environmental data present) is also set.

- The storage control microcode has detected one of the errors, such as timeout of some device activity, which is normally reported using this format. Equipment check (byte 0, bit 3) is set. These do not include microcode detected seek checks.

- Successfully retried logic seek checks are off loaded if they occurred during error logging mode or forced error logging mode. Environmental Data Present (byte 2, bit 3) is set.

- When Online (byte 19, bit 4) is not active, and either Device Switch Set to Disable (byte 20, bit 5) or Busy (byte 19, bit 6) is active, then Intervention Required (byte 0, bit 1) is set. If Online (byte 19, bit 4) is inactive, and Device Switch Set to Disable (byte 20, bit 5) is inactive, Equipment Check (byte 0, bit 3) is set.

If Friend or Subsystem Log bytes are being examined and a 9F10 symptom code is listed, read the text on ECD-4.

Fmt 1 - Byte 0 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Command Rejected	SENSE-59
1	0	Intervention Required	SENSE-59
2	0	Channel Bus Out Parity	SENSE-59
3	0	Equipment Check	SENSE-59
4	0	Data Check	SENSE-59
5	0	Overrun	SENSE-59
6	0	Unused	

Bit	N	Bit Name
7	0	Unused

Fmt 1 - Byte 1 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Permanent Error	SENSE-60
1	0	Invalid Track Format	SENSE-60
2	0	End of Cylinder	SENSE-60
3	0	Message to Operator	SENSE-60
4	0	No Record Found	SENSE-60
5	0	File Protected	SENSE-60
6	0	Write Inhibited	SENSE-60
7	0	Imprecise Ending	SENSE-60

Fmt 1 - Byte 2 **Unit Check Description** **SENSE-60**

Bit	N	Bit Name	
0	0	Request Write Inhibit	SENSE-60
1	0	Correctable	SENSE-60
2	0	First Error Logged	SENSE-60
3	0	Environmental Data Present	SENSE-61
4	0	Intent Violation	SENSE-61
5	0	Imprecise Ending	SENSE-61
6	0	Write Operation in Progress	SENSE-61
7	0	3880 Model 23 Storage Control	SENSE-61

Fmt 1 - Byte 3 **String ID** **SENSE-61**

This byte identifies the string in which the device resides. The controller is identified by the Path In Use bits of byte 4.

Fmt 1 - Byte 4 **Path and Device Physical Identifier** **SENSE-61**

Bit	Bit Name	
0	Path In Use / Controller Response Bit 0	SENSE-61
1	Path In Use / Controller Response Bit 1	SENSE-61
2	String Address Bit (0 or 1)	SENSE-62
3-7	Device Address Bits (x'00' through x'1F')	SENSE-62

Fmt 1 - Byte 5 **Seek Low Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4

Bit	Bit Name
6	Cylinder 2
7	Cylinder 1

Fmt 1 - Byte 6 **Seek Head and High Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 2048
1	Cylinder 1024
2	Cylinder 512
3	Cylinder 256
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Fmt 1 - Byte 7 **Format and Message** **SENSE-62**

Equals	Prty	PSC	Message	
x'10'	313	9F10	No Message	ECD-4
x'11'	314	9F11	Device Status 1 Not as Expected	ECD-4
x'12'			Not Used	
x'13'	316	9F13	Index Missing	ECD-6
x'14'	317	9F14	Interrupt Not Resettable	ECD-7
x'15'	302	9F15	Device Does Not Respond To Selection	ECD-8
x'16'	318	9F16	Device Check-2 Or Set Sector Incomplete	ECD-10
x'17'			Not Used	
x'18'	320	9F18	Device Status-1 Has an Invalid Combination of Bits	ECD-11
x'19'	321	9F19	Device Not Ready To Do Customer Work	ECD-12
x'1A'			Not Used	
x'1B'	322	9F1B	Missing Device Address Bit At Selection	ECD-13
x'1C'	303	9F1C	Drive Motor Switch Sensed Off	
x'1D'	312	9DXX	Seek Incomplete	ECD-15
x'1E'			Not Used	
x'1F'	319	9F1F	Offset Active Cannot Be Reset	ECD-16

Fmt 1 - Byte 8 **String Features** **SENSE-62**

Bit	N	Bit Name	
0		Dynamic Path Selection Function Installed in Controllers	SENSE-62
1		String Has Four Path Capability	SENSE-62
2		Second CDP Card Installed	SENSE-62
3		Reserved	
4		3380 Model CJ2	
5	0	Always Zero (Controller type definition, set to 0 for 3380-JK)	
6	0	Always Zero (Controller type definition, set to 0 for 3380-JK)	
7	1	3380-JK	SENSE-62

Fmt 1 - Byte 9 with Byte 7 equal to x'11' — **Expected Device Status**

With Message 1, Device Status Not As Expected, Byte 9 will contain the device status expected by the storage control. A comparison with Byte 19, Device Status 1, will provide the reader with the status bit that was not at the expected state at the time of its examination.

Fmt 1 - Byte 9 with Byte 7 equal to x'14' x'15' x'16' x'18' x'1D' or x'1F' — **DDC Bus In**

Byte 9 may contain the DDC Bus In bit configuration at the storage control end of the bus when the storage control recognized that an error occurred.

Because of storage director recovery procedures for Format 1, the contents of this byte cannot be guaranteed.

Fmt 1 - Byte 9 with Byte 7 equal to x'12' x'13' x'19' x'1B' or x'1C' — **Invalid Data**

Byte 9 will contain invalid data.

Fmt 1 - Byte 9 with Byte 7 = x'10' — **End Operation Codes**

Bit 0 = Index
Bit 1 = No sync and no data

The hex codes below (bits 2 through 7) are ORed with the bits above and result in the final contents of the End Op byte.

Bits 2-7 Equals	Prty	PSC	End Operation	
'00'			Operation successfully completed, No Error	
'01'	257	ED01	DDC Command Overrun	ECD-344
'02'		4XXX	Sync Byte Missing - The storage control collects format 4 sense data.	ECD-233
'03'		4XYY	Data Check - The storage control collects format 4 or 5 sense data.	ECD-235
'04'		4XYY	Data Check - With a controller undervoltage condition.	ECD-235
'06'	202	ED06	Invalid Command Code	ECD-346
'07'	203	ED07	DDC Data Overrun	ECD-348
'08'		ED08	HAR Modifier Overrun On Set HAR Oriented	ECD-349
'09'	237	9F15	Device Not Responding to Selection	ECD-8
'0D'		4XYY	No Read Data Found	ECD-237
'0F'			Delta Frequency/Fail to Lock Check	
'10'	245	ED10	Check 2 Detected in Controller	ECD-351
'11'	235	ED11	Device Check-1 on Selection	ECD-353
'12'	258	E8XX	Controller Sequencer Microcode Detected Error	ECD-355
'13'	234	ED13	CDP Hung Due to Late or Missing Device Response	ECD-388
'16'		ED16	Data Check on Start Read/Write	ECD-390

Bits 2-7 Equals	Prty	PSC	End Operation	
'17'	204	ED17	Any Check, but Controller Collected No Status	ECD-391
'18'	205	ED18	Sync Out/In Tag Counts Not Equal	ECD-393
'19'	259	ED19	Device Dropped to Null	ECD-394
'1B'	260	ED1B	Index Found During Defect Skip in HA	ECD-395
'20'			Device Check Active - The storage control collects Format 1 or 9 sense data. (Format 9 when only Byte 11 Bit 5 is active or message 7, A or E.)	ECD-397

Fmt 1 - Byte 10 **Device Power Status** **SENSE-63**

Bit	N	Prty	PSC	Bit Name		
0	0			Motor Start Surge Complete	SENSE-63	
1	0			Unused		
2	0	306	9020	No Air Flow	SENSE-63	ECD-17
3	1			Device Power On Sequence Complete	SENSE-63	
4	1			Spindle Motor Started by Device Sequencer	SENSE-63	
5	1			Spindle Control Bit 0	SENSE-63	
6	1			Motor Brake Latch	SENSE-63	
7	0			Spindle Control Bit 1	SENSE-63	

Fmt 1 - Byte 11 **Device Check-2 Status** **SENSE-63**

Bit	N	Prty	PSC	Bit Name		
0	0	307	9180	Device Sequencer Check	SENSE-63	ECD-18
1	0	308	97XX	Servo Control Check	SENSE-64	ECD-19
2	0	309	9120	Rotational Position Sensing (RPS) Check	SENSE-64	ECD-20
3	0	310	95XX	Checkpoint Check See Checkpoint Log, byte 15 on SENSE-66	SENSE-63	ECD-22
4	0	323	9108	HDA Cable Swap Check	SENSE-64	ECD-23
5	0	402	9104	Read/Write Check	SENSE-64	ECD-448
6	0	304	9102	Power Card Check	SENSE-64	ECD-24
7	0	305	9101	Funnel Parity Check	SENSE-64	ECD-26

Fmt 1 - Byte 12 and 13 **Servo Status-0** **SENSE-64**

SENSE-64'

Byte 12 Bit	Bit Name	
0	Not Used	SENSE-64
1	Self Initiated Busy	SENSE-64
2	Initial Microcode Load In Progress	SENSE-64
3	Initial Microcode Load Complete	SENSE-64
4	Half Track	SENSE-64
5	Servo Write Inhibit	SENSE-65
6	Index	SENSE-65
7	Scale 2 Mode	SENSE-65

"F¹B¹³ - BIT 4 - SERVO INHIBIT" on page SENSE-65'

Byte 13	Bit	Bit Name	
	0	Clock	SENSE-65
	1	DCP Busy	SENSE-65
	2	DCP Error	SENSE-65
	3	DCP Check-2	SENSE-65
	4	Servo Inhibit	SENSE-65
	5	Track Following	SENSE-65
	6	Offset	SENSE-65
	7	Servo to Voltage	SENSE-65

Fmt 1 - Byte 14 **Servo Status-1, First Byte, Version Level** **SENSE-66**

This byte is the first of two bytes that indicate the version level of the Servo Card Microcode.

Fmt 1 - Byte 15 **Device Checkpoint Log** **SENSE-66**

For details see SENSE-66

Fmt 1 - Byte 16 **Servo Status-1, Second Byte, Version Level** **SENSE-66**

This byte is the second of two bytes that indicate the version level of the Servo Card Microcode.

Fmt 1 - Byte 17 and 18 with Byte 12 Bit 2 = 1 **Servo Status-2, Invalid**

These bytes are invalid because the Servo microcode is in the process of an IML indicated by Byte 12 Bit 2 active, Servo Microcode Initial Microcode Load in Progress.

Fmt 1 - Byte 17 and 18 with Byte 12 Bit 2 = 0 **Servo Status-2**

These bytes are the Digital Control Processor (DCP) detected errors. The codes indicate either DCP Servo Inhibit (Errors that are external to the DCP and its busses), or DCP Servo Check-2 errors (Errors that are internal to the DCP and its busses). All errors below x'8000' are DCP Servo Inhibit errors.

Equals	Message
x'0000'	No Error
x'1300'	Motion Command Not Accepted While Busy
x'1400'	Disable Write Inhibit Command Received While Not Offset
x'2000'	Excessive Voltage Required to Park at OD During Rezero or Sweep
x'2100'	Excessive Servo to Voltage, or Servo to Current Loop Errors
x'2300'	Excessive Average VCM Current
x'5100'	Windage Exceeds The Allowable Limit
x'5200'	PES Exceeds The Allowable Limit During Track Following
x'5300'	AGC Is Inactive
x'5400'	Seek Command Received When Not Track Following Or In Offset

Equals	Message
x'5500'	Offset Command Received When Not Track Following Or In Offset
x'5600'	Seek Command Outside The Minimum or Maximum Cylinder
x'5700'	AGC Gain Correction Voltage Reached The Limit During Rezero or Sweep
x'5800'	Excessive Position Estimator Error
x'5900'	Timeout While Executing a Seek, Offset, Sweep, or Rezero
x'5A00'	Unable to Locate Either Guard Band During Rezero
x'5B00'	PES P Has Too Much Offset
x'5C00'	PES Q Has Too Much Offset
x'5D00'	GBID Detected at the Wrong Cylinder (Probably Incorrect Device Model)
x'5E00'	Unable To Move Away From Guard Band Outer Diameter (GBOD)
x'8100'	IML Fails Checksum
x'8300'	Instruction Storage Parity Error
x'8400'	Data Storage Parity Error
x'8500'	Data Bus Parity Error
x'8600'	Time Interval Between Interrupts Is Too Short (DCP Sample Interrupt Signal net)
x'8700'	Illegal Command
x'8800'	Time Interval Between Interrupts Is Too Long
x'FC00'	Multiply Failure In Basic Assurance Test
x'FD00'	Compute Failure In Basic Assurance Test
x'FE00'	Checksum Failure In Basic Assurance Test
x'FF00'	Power On Reset Code Hung

Fmt 1 - Byte 19 **Device Status 1** **SENSE-74**

Bit	N	Bit Name		
0	0	Padding In Progress	SENSE-74	
1		Device Model	SENSE-74	
2	0	Always Zero	SENSE-74	
3	0	Device Error	SENSE-74	ECD-487
4	1	Online	SENSE-75	
5	0	HDA Attention	SENSE-75	
6	0	Device Busy	SENSE-75	
7	0	Locate Interrupt	SENSE-75	

Fmt 1 - Byte 20 **Device Status 2** **SENSE-75**

Bit	N	Prty	PSC	Bit Name		
0	0			Device Logic Disabled	SENSE-75	
1	0			Servo Inhibit	SENSE-75	ECD-229
2	0			Offset Active	SENSE-75	
3	0			Drive Motor Switch Off	SENSE-75	
4	0			Access Mechanism Logic Exchanged	SENSE-75	
5	0			Device Switch Set to Disable	SENSE-75	
6	0	301	9FFF	Device Logic Undervoltage Status	SENSE-75	ECD-230
7	0			Seek Incomplete	SENSE-75	ECD-232

Fmt 1 - Byte 21 **Subsystem or Storage Director Physical ID**

This byte is the Storage Director Physical ID when 3380-JK is attached to a 3880. This byte identifies the attached storage director at the time of this sense collection.

When 3380-JK is attached to 3990, this byte is the low order byte of the Subsystem ID. With the Path In Use bits of byte 4, it identifies the storage director attached at the time of this sense collection.

Fmt 1 - Byte 22 and 23 **Symptom Code**

These bytes are a summary of the error condition indicated in the prior 22 bytes.

Format 1 symptom codes all start with the numeral 9, for example 9XXX.

Fmt 1 - Byte 24 **Flags**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Reserved, set to 0
1	Reserved, set to 0
2	Reserved, set to 0
3	Logging Mode
4&5	Logging Control Bits (with 3990 Only)
0 0	Do Not Log
0 1	Log Unconditionally
1 0	Log First Occurrence of This Retry Sequence
1 1	Log First Occurrence of This Retry Sequence If Permanent Error On This Path
6&7	Operator Message Control
0 0	Send No Message to Operator
0 1	Send Message to Operator Unconditionally
1 0	Send Message to Operator On the First Record for This Retry Sequence
1 1	Send Message to Operator on the First Record for This Retry Sequence if Permanent Error on This Path

Fmt 1 - Byte 25 **Action Code**

This byte identifies the Action Code used by 3990. Refer to the 3990 Maintenance Manuals for the definition of this byte.

Fmt 1 - Byte 26 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Dual Frame Storage Control
1	4 Path Device Level Selection
2	Duplex Pair Volume
3	Secondary Device of a Duplex Pair
4	Sense Presented to Relevant Channel
5	Sense Presented to Relevant Device Number
6	Put Record into System Exception Report
7	Alternate Internal Path Will Be Tried

Fmt 1 - Byte 27 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Twenty-four Byte Capability
1	Device Address Valid in Byte 4
2	Track Address Present in Bytes 29 thru 31
3	Reserved, Set to 0
4	Reserved, set to 0
5	Reserved, set to 0
6	Cluster
7	Storage Path

Fmt 1 - Byte 28 **Message Code**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	ERP, Prepare a SIM Message
1-7	Format of the SIM Message

Fmt 1 - Byte 29 **Seek Cylinder Address High**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Cylinder 2048
5	Cylinder 1024
6	Cylinder 512
7	Cylinder 256

Fmt 1 - Byte 30 **Seek Cylinder Address Low**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 1 - Byte 31 **Seek Head Address**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Format 4

Format 4 is generated when:

- Uncorrectable Data Checks were detected in either the Home Address, count, key, or data areas and retry was unsuccessful.
- Data Checks were detected in either the Home Address, count, key, or data areas that were successfully recovered using subsystem retry with head offset.
- Data Checks were detected in either the Home Address, count, key, or data areas that were successfully recovered (using ECC correction or subsystem retry), and logging mode was active in the storage director. Logging mode is set by a successfully recovered data check threshold counter overflow condition.
- Successfully recovered correctable Data Checks detected while in diagnostic mode. Programs, such as ICKDSF, use a diagnostic mode during their operations to extract error information without allowing the subsystem Error Recovery Procedures to intercede and correct the Correctable Data Checks. This diagnostic mode error data will not normally be displayed.

Fmt 4 - Byte 0 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Command Rejected	SENSE-59
1	0	Intervention Required	SENSE-59
2	0	Channel Bus Out Parity Check	SENSE-59
3	0	Equipment Check	SENSE-59
4	0	Data Check	SENSE-59
5	0	Overrun	SENSE-59
6	0	Unused	
7	0	Unused	

Fmt 4 - Byte 1 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Permanent Error	SENSE-60
1	0	Invalid Track Format	SENSE-60
2	0	End of Cylinder	SENSE-60
3	0	Message to Operator	SENSE-60
4	0	No Record Found	SENSE-60
5	0	File Protected	SENSE-60
6	0	Write Inhibited	SENSE-60
7	0	Imprecise Ending	SENSE-60

Fmt 4 - Byte 2 **Unit Check Description** **SENSE-60**

Bit	N	Bit Name	
0	0	Request Write Inhibit	SENSE-60
1	0	Correctable	SENSE-60
2	0	First Error Logged	SENSE-60
3	0	Environmental Data Present	SENSE-61
4	0	Intent Violation	SENSE-61
5	0	Imprecise Ending	SENSE-61
6	0	Write Operation in Progress	SENSE-61
7	0	3880 Model 23 Storage Control	SENSE-61

Fmt 4 - Byte 3 with Byte 2 Bit 3 = 1 **Retry Count / Records Remaining**

With Environmental Data Present bit set, this byte indicates the number of DASD subsystem retries attempted by the storage control to make the record usable. The data was recovered and the error was temporary.

Byte 1 Bit 0 = 1 & Byte 2 Bit 5 = 1

With the Permanent bit set and with Imprecise Ending bit active, this byte indicates the number of remaining records to be processed in the domain of Locate Record command. The data was not successfully read.

Byte 1 Bit 0 = 1 & Byte 2 Bit 5 = 0

With the Permanent bit set and without Imprecise Ending bit active, this byte is set to zero. The data was not successfully read.

Note: *See byte 14 for the String ID for this format.*

Fmt 4 - Byte 4 **Path and Device Physical Identifier** **SENSE-61**

Bit	Bit Name	
0	Path In Use / Controller Response Bit 0	SENSE-61
1	Path In Use / Controller Response Bit 1	SENSE-61
2	String Address Bit 0 or 1	SENSE-62
3-7	Device Address Bits , x'00' through x'1F'	SENSE-62

Fmt 4 - Byte 5 **Seek Low Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 4 - Byte 6 **Seek Head and High Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 2048
1	Cylinder 1024
2	Cylinder 512
3	Cylinder 256
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Fmt 4 - Byte 7 **Format and Message** **SENSE-62**

Equals	Message
x'40'	Home Address Area, Data Check
x'41'	Count Area, Data Check
x'42'	Key Area, Data Check
x'43'	Data Area, Data Check
x'44'	Home Address Area, No Sync Byte Found
x'45'	Count Area, No Sync Byte Found
x'46'	Key Area, No Sync Byte Found
x'47'	Data Area, No Sync Byte Found

Messages 8 thru F not used by 3380-JK

Fmt 4 - Bytes 8 through 12 **Record ID *** **SENSE-76**

The following bit description scheme, for Bytes 8 through 12, will be correct in most instances, but keep in mind that a program can use many other schemes to identify the record.

Byte 8 Bit	Bit Name
0-3	Unused
4	Cylinder 2048
5	Cylinder 1024
6	Cylinder 512
7	Cylinder 256

Byte 9 Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Byte 10 Bit	Bit Name
0-7	Unused

Byte 11 Bit	Bit Name
0-3	Unused
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Byte 12 Bit	Bit Name
0	Record 128
1	Record 64
2	Record 32
3	Record 16
4	Record 8
5	Record 4
6	Record 2
7	Record 1

Fmt 4 - Byte 13 **Sector Number** **SENSE-76**

This byte is used by the error recovery procedure to determine where it should commence the retry read operation. It indicates the beginning sector on the track that has the error area.

Fmt 4 - Byte 14 **String ID** **SENSE-61**

This byte identifies the string in which the device that had the data check resides. The controller is identified by the Path In Use bits of byte 4.

Fmt 4 - Byte 15 **Head Offset Value** **SENSE-76**

Bit	Bit Name	
0-3	Units of offset	SENSE-76
	'0' No offset applied	SENSE-76
	'1' 1st increment of offset	SENSE-76
	'2' 2nd increment of offset	SENSE-76
	'3' 3rd increment of offset	SENSE-76
	'4' 4th increment of offset	SENSE-76
	'5' 5th increment of offset	SENSE-76
	'6-F' Not Used	SENSE-76
4	Unused	SENSE-76
5	Extra Subsystem Recovery Operation	SENSE-76
6	Unused	SENSE-76
7	Forward Direction	SENSE-76

Fmt 4 - Byte 16 and 17 — **ECC Status Bytes**

Byte 16 Bit	Bit Name	
0	'Sub-Block' Check Byte Error (ICKDSF)	SENSE-77
1	'Block' Check Byte Error (ICKDSF)	SENSE-77
2	Uncorrectable Determined by Block Check Errors	SENSE-77
3	Two or More Second Level Errors in One Phase	SENSE-77
4	128 First-Level Errors Allowed	SENSE-77
5	Second Level Correctable Error Count 4	SENSE-77
6	Second Level Correctable Error Count 2	SENSE-77
7	Second Level Correctable Error Count 1	SENSE-77

Byte 17 Bit	Bit Name	
0	First Level Correctable Error Count 128	SENSE-77
1	First Level Correctable Error Count 64	SENSE-77
2	First Level Correctable Error Count 32	SENSE-77
3	First Level Correctable Error Count 16	SENSE-77
4	First Level Correctable Error Count 8	SENSE-77
5	First Level Correctable Error Count 4	SENSE-77
6	First Level Correctable Error Count 2	SENSE-77
7	First Level Correctable Error Count 1	SENSE-77

Fmt 4 - Bytes 18 - 19 — **Error Displacement**

For 3380-JK, these bytes will contain the displacement of only the first byte in error. 3380-JK devices may have several non-contiguous ECC correctable errors in the same field. This error displacement will locate only the first one.

Fmt 4 - Byte 20 — **Unused**

Fmt 4 - Byte 21 — **Subsystem or Storage Director Physical ID**

This byte is the Storage Director Physical ID when 3380-JK is attached to a 3880. This byte identifies the attached storage director at the time of this sense collection.

When it is attached to 3990, this byte is the low order byte of the Subsystem ID. With the Path In Use bits of byte 4, it identifies the storage director attached at the time of this sense collection.

Fmt 4 - Byte 22 and 23 — **Symptom Code**

The symptom code generated for Format 4 is:

Byte 22 equals Byte 7
Byte 23 equals:

Bit	Bit Name
0&1	Error Correction Process Used
0 0	Recovered without using ECC
0 1	Recovered Using First Level Correction

Bit	Bit Name
1 0	Recovered Using Second Level Correction
1 1	Permanent Error, Not Recovered Using Subsystem Error Recovery
2	Offset Active
3	Always 0
4	Under Voltage Condition Detected in the Device
5	Under Voltage Condition Detected in the Controller
6	Offset Recovery Bypassed In One Direction
7	Loss of Track Following

Fmt 4 - Byte 24 **Flags**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Reserved, set to 0
1	Reserved, set to 0
2	Reserved, set to 0
3	Logging Mode
4&5	Logging Control Bits (with 3990 Only)
0 0	Do Not Log
0 1	Log Unconditionally
1 0	Log First Occurrence of This Retry Sequence
1 1	Log First Occurrence of This Retry Sequence If Permanent Error On This Path
6&7	Operator Message Control
0 0	Send No Message to Operator
0 1	Send Message to Operator Unconditionally
1 0	Send Message to Operator On the First Record for This Retry Sequence
1 1	Send Message to Operator on the First Record for This Retry Sequence if Permanent Error on This Path

Fmt 4 - Byte 25 **Action Code**

This byte identifies the Action Code used by 3990. Refer to the 3990 Maintenance Manuals for the definition of this byte.

Fmt 4 - Byte 26 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Dual Frame Storage Control
1	4 Path Device Level Selection
2	Duplex Pair Volume
3	Secondary Device of a Duplex Pair

Bit	Bit Name
4	Sense Presented to Relevant Channel
5	Sense Presented to Relevant Device Number
6	Put Record into System Exception Report
7	Alternate Internal Path Will Be Tried

Fmt 4 - Byte 27 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Twenty-four Byte Capability
1	Device Address Valid in Byte 4
2	Track Address Present in Bytes 29 thru 31
3	Reserved, Set to 0
4	Reserved, set to 0
5	Reserved, set to 0
6	Cluster
7	Storage Path

Fmt 4 - Byte 28 **Message Code**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	ERP, Prepare a SIM Message
1-7	Format of the SIM Message

Fmt 4 - Byte 29 **Seek Cylinder Address High**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Cylinder 2048
5	Cylinder 1024
6	Cylinder 512
7	Cylinder 256

Fmt 4 - Byte 30 **Seek Cylinder Address Low**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 4 - Byte 31 **Seek Head Address**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Format 5

Format 5 Correctable Data Checks **will not be logged** in LogRec by the error recovery procedures because it is not the format normally used to indicate Correctable Data Checks for 3380-JK. Normally, all Correctable Data Checks will be reported and logged using Format 4.

This format is listed here for those few instances where a diagnostic program displays its results. Normal operations should not use this format to indicate the occurrence of Correctable Data Checks.

Format 5 is generated when:

- Data Checks were detected while reading a Read Multiple Count Key Data command. Format 5 is used to indicate to the Error Recovery Procedure and the user program that it should not continue with the Read Multiple Count Key Data command string because the subsystem will not be able to recover from the multiple Data Checks that have occurred while processing the command. The user program will usually issue individual read commands until the data expected from the Read Multiple command has been read. Each area will be read independently and all necessary error correction will be correctly applied.

- A data check, either ECC correctable or uncorrectable, recovered using Channel Command Retry while in PCI Fetch mode. Both the error displacement and correction patterns are set to zero by the Storage Control.

  This sense record is sent to the system to indicate that the last data received is invalid, and that if it is processing that data, it should commence to reprocess it again after receiving corrected data.

Fmt 5 - Byte 0 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Command Rejected	SENSE-59
1	0	Intervention Required	SENSE-59
2	0	Channel Bus Out Parity Check	SENSE-59
3	0	Equipment Check	SENSE-59
4	0	Data Check	SENSE-59
5	0	Overrun	SENSE-59
6	0	Unused	
7	0	Unused	

Fmt 5 - Byte 1 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Permanent Error	SENSE-60
1	0	Invalid Track Format	SENSE-60
2	0	End of Cylinder	SENSE-60
3	0	Message to Operator	SENSE-60
4	0	No Record Found	SENSE-60
5	0	File Protected	SENSE-60
6	0	Write Inhibited	SENSE-60
7	0	Imprecise Ending	SENSE-60

Fmt 5 - Byte 2 **Unit Check Description** **SENSE-60**

Bit	N	Bit Name	
0	0	Request Write Inhibit	SENSE-60
1	0	Correctable	SENSE-60
2	0	First Error Logged	SENSE-60
3	0	Environmental Data Present	SENSE-61
4	0	Intent Violation	SENSE-61
5	0	Imprecise Ending	SENSE-61
6	0	Write Operation in Progress	SENSE-61
7	0	3880 Model 23 Storage Control	SENSE-61

Fmt 5 - Byte 3 **Not Used**

Fmt 5 - Byte 4 **Path and Device Physical Identifier** **SENSE-61**

Bit	Bit Name	
0	Path In Use / Controller Response Bit 0	SENSE-61
1	Path In Use / Controller Response Bit 1	SENSE-61
2	String Address Bit (0 or 1)	SENSE-62
3-7	Device Address Bits (x'00' through x'1F')	SENSE-62

Fmt 5 - Byte 5 **Seek Low Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 5 - Byte 6 **Seek Head and High Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 2048
1	Cylinder 1024
2	Cylinder 512
3	Cylinder 256
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Fmt 5 - Byte 7 **Format and Message** **SENSE-62**

Equals	Message
x'50'	Home Address Area, Data Check
x'51'	Count Area, Data Check
x'52'	Key Area, Data Check
x'53'	Data Area, Data Check

Messages 4 thru F are not used by 3380-JK

Fmt 5 - Bytes 8 through 12 **Record ID *** **SENSE-76**

Byte 8 Bit	Bit Name
0-3	Unused
4	Cylinder 2048
5	Cylinder 1024
6	Cylinder 512
7	Cylinder 256

Byte 9 Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Byte 10 Bit	Bit Name
0-7	Unused

Byte 11 Bit	Bit Name
0-3	Unused
4	Head Address 8

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* The following bit description scheme, for Bytes 8 through 12, will be correct in most instances, but keep in mind that a customer's program can use another scheme to identify the record.

Byte 11 Bit	Bit Name
5	Head Address 4
6	Head Address 2
7	Head Address 1

Byte 12 Bit	Bit Name
0	Record 128
1	Record 64
2	Record 32
3	Record 16
4	Record 8
5	Record 4
6	Record 2
7	Record 1

Fmt 5 - Byte 13 **Sector Number** **SENSE-76**

This byte is used by the error recovery procedure to determine where it should commence the retry read operation. It indicates the beginning sector of the track that has the error area.

Fmt 5 - Byte 14 **String ID** **SENSE-61**

This byte identifies the string in which the device that had the data check resides. The controller is identified by the Path In Use bits of byte 4.

Fmt 5 - Byte 15 - 17 with Byte 2 Bit 3 = 0 **Restart Displacement**

Refer to the Storage Control Description Manual, Error Recover Procedures, Error Correction Function - Count, Key, and Data Devices for details on how the Storage Control expects the system Error Recovery Procedures to use the data in these three bytes.

Fmt 5 - Bytes 18 - 19 **Error Displacement**

For 3380-JK, these bytes will contain the displacement of only the first byte in error. 3380-JK devices may have several non-contiguous ECC correctable errors in the same field. This error displacement will locate only the first one.

Fmt 5 - Byte 20 - 23 **Error Pattern**

For 3380-JK, these bytes will always be set to zero.

Note: Format 5 sense data does not have symptom code bytes. Only Format 4 data checks have symptom codes.

Fmt 5 - Byte 24 **Flags**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Reserved, set to 0
1	Reserved, set to 0
2	Reserved, set to 0
3	Logging Mode
4&5	Logging Control Bits (with 3990 Only)
0 0	Do Not Log
0 1	Log Unconditionally
1 0	Log First Occurrence of This Retry Sequence
1 1	Log First Occurrence of This Retry Sequence If Permanent Error On This Path
6&7	Operator Message Control
0 0	Send No Message to Operator
0 1	Send Message to Operator Unconditionally
1 0	Send Message to Operator On the First Record for This Retry Sequence
1 1	Send Message to Operator on the First Record for This Retry Sequence if Permanent Error on This Path

Fmt 5 - Byte 25 **Action Code**

This byte identifies the Action Code used by 3990. Refer to the 3990 Maintenance Manuals for the definition of this byte.

Fmt 5 - Byte 26 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Dual Frame Storage Control
1	4 Path Device Level Selection
2	Duplex Pair Volume
3	Secondary Device of a Duplex Pair
4	Sense Presented to Relevant Channel
5	Sense Presented to Relevant Device Number
6	Put Record into System Exception Report
7	Alternate Internal Path Will Be Tried

Fmt 5 - Byte 27 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Twenty-four Byte Capability
1	Device Address Valid in Byte 4
2	Track Address Present in Bytes 29 thru 31
3	Reserved, Set to 0
4	Reserved, set to 0
5	Reserved, set to 0
6	Cluster
7	Storage Path

Fmt 5 - Byte 28 **Message Code**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	ERP, Prepare a SIM Message
1-7	Format of the SIM Message

Fmt 5 - Byte 29 **Seek Cylinder Address High**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Cylinder 2048
5	Cylinder 1024
6	Cylinder 512
7	Cylinder 256

Fmt 5 - Byte 30 **Seek Cylinder Address Low**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 5 - Byte 31 **Seek Head Address**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Format 6

The text format of 3380-JK Format 6 varies dependent on the Storage Control Unit that 3380-JK is attached to. Only the bits that relate to 3380-JK are described in the following text. The Storage Control is identified as either 3880-3 or 3990. For details of the remaining bytes and bits of the format see the Storage Control's documentation.

Format 6 is used by both the storage control and the devices. The following text only relates to those bits that relate to the environmental data of 3380-JK (Byte 2 Bit 3 active).: **Format 6 for 3380-JK is generated when:**

- A Read and Reset Buffered Log command is executed.

  Normally issued with the End Of Day command or when EREP is run.

- Usage/error statistics require off-loading from the storage control due to counter overflow

  The number of bytes read or searched and the number of motion seeks is the only usage data reported by a 3380-JK.

  The EREP DASD String Summary Report totals each of the different counts for the period. The EREP Event History Report shows the format 6 records as MDR (Miscellaneous Data Record) type records.

Fmt 6 - Byte 1 **Unit Check Description**

Bit	N	Bit Name	
0	0	Permanent Error	SENSE-60

Fmt 6 - Byte 2 **Unit Check Description**

Bit	N	Bit Name	
3	1	Environmental Data Present	SENSE-61

Fmt 6 - Byte 3 **String ID** **SENSE-61**

This byte identifies the string to which the device resides. The controller is identified by the Path In Use bits of byte 4.

Fmt 6 - Byte 4 **Path and Device Physical Identifier** **SENSE-61**

Bit	Bit Name	
0	Path In Use / Controller Response Bit 0	SENSE-61
1	Path In Use / Controller Response Bit 1	SENSE-61
2	String Address Bit (0 or 1)	SENSE-62
3-7	Device Address Bits (x'00' through x'1F')	SENSE-62

Fmt 6 - Byte 6 / 3880 **Storage Director Physical ID**

This byte is the Storage Director Physical ID when 3380-JK is attached to a 3880. This byte identifies the attached storage director at the time of this sense collection.

Fmt 6 - Byte 7 **Format and Message** **SENSE-62**

There are no messages in this format for 3380-JK, but bit four of this byte, the high order Message Bit, will always be active to indicate that this is an environmental collection format.

Fmt 6 - Bytes 8 through 11 **Bytes Read or Searched**

Bytes 8 through 11 contain the number of bytes read or searched for the addressed device. (Only Key and Data bytes are counted. Bytes processed during retry are not counted.)

Fmt 6 - Bytes 12 and 13 / 3990 **Number of Motion Seeks**

Bytes 12 and 13 contain the number of seek commands processed by the 3990 storage path, but do not include recalibrate or retried seeks.

Fmt 6 - Bytes 16 and 17 / 3880 **Number of Motion Seeks**

Bytes 16 and 17 contain the number of seek commands processed by the 3880 storage director, but do not include recalibrate or retried seeks.

Format 7

Format 7 is generated when:

- A controller type 1 (check 1) error occurs.
- A path error exists between the storage control and the attached controller.

  If the 3380 Controller Power On/Off switch is switched to Off after the storage control and controller have established initial communication and the storage control attempts to use the path, this format indicates an equipment check error. If use is attempted prior to initial communication and the Controller Power On/Off switch is set to Off, a Condition Code 3 response results. (In other IBM non 3380 DASD products, a disabled interface is always indicated to the system as a Condition Code 3.)

Note: Controller 0 in Format 7 sense data is the controller addressed as zero on the CTL-I attached to the storage director or subsystem identified in byte 21. Controller 1 is the controller addressed as one on that same interface.

Fmt 7 - Byte 0 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Command Rejected	SENSE-59
1	0	Intervention Required	SENSE-59
2	0	Channel Bus Out Parity Check	SENSE-59
3	0	Equipment Check	SENSE-59
4	0	Data Check	SENSE-59
5	0	Overrun	SENSE-59
6	0	Unused	
7	0	Unused	

Fmt 7 - Byte 1 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Permanent Error	SENSE-60
1	0	Invalid Track Format	SENSE-60
2	0	End of Cylinder	SENSE-60
3	0	Message to Operator	SENSE-60
4	0	No Record Found	SENSE-60
5	0	File Protected	SENSE-60
6	0	Write Inhibited	SENSE-60
7	0	Imprecise Ending	SENSE-60

Fmt 7 - Byte 2 **Unit Check Description** **SENSE-60**

Bit	N	Bit Name	
0	0	Request Write Inhibit	SENSE-60
1	0	Correctable	SENSE-60
2	0	First Error Logged	SENSE-60
3	0	Environmental Data Present	SENSE-61
4	0	Intent Violation	SENSE-61
5	0	Imprecise Ending	SENSE-61
6	0	Write Operation in Progress	SENSE-61
7	0	3880 Model 23 Storage Control	SENSE-61

Fmt 7 - Byte 3 **String ID** **SENSE-61**

The storage control suspects this string's controller as being the failing controller. In that there is only one CCA net, the storage control examines Byte 11 CCA bits to determine which String ID to load into this byte. If both controllers CCA bits are active, it uses the String ID of the selected controller. The controller address selected can be determined by the Path In Use bits and the string address in byte 4.

Fmt 7 - Byte 4 **Path and Device Physical Identifier** **SENSE-61**

Bit	Bit Name	
0	Path In Use / Controller Response Bit 0	SENSE-61
1	Path In Use / Controller Response Bit 1	SENSE-61
2	String Address Bit (0 or 1)	SENSE-62
3-7	Device Address Bits (x'00' through x'1F')	SENSE-62

Fmt 7 - Byte 5 **Seek Low Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 7 - Byte 6 **Seek Head and High Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 2048
1	Cylinder 1024
2	Cylinder 512
3	Cylinder 256
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Equals	Prty	PSC	Message	
x'70'			RCC Initiated By a Connection Check Alert	
x'71'	109	DF01	RCC1 Sequence Not Successful	ECD-238
x'72'	101	DF02	RCC1 and RCC2 Sequences Not Successful	ECD-240
x'73'	125	DF03	Invalid Tag In During Selection Sequence	ECD-241
x'74'	132	DF04	Extra RCC Required	ECD-243
x'75'	126	DF05	Invalid DDC Selection Response or Time-out	ECD-244
x'76'	127	DF06	Missing End Operation, Transfer Was Complete	ECD-245
x'77'	128	DF07	Missing End Operation, Transfer Was Incomplete	ECD-247
x'78'	129	DF08	Invalid Tag In for an Immediate Command Sequence	ECD-248
x'79'	130	DF09	Invalid Tag In for an Extended Command Sequence	ECD-250
x'7A'	131	DF0A	Storage Control Microcode Timed Out On Deselection	ECD-251
x'7B'	124	DF0B	No Selection Response After Poll Interrupt	ECD-252
x'7C'	133	DF0C	Controller Fenced, Permanent Path Error	ECD-254
x'7D'	134	DF0D	Controller Not Available on Disconnected Command Chain	ECD-255

Messages E and F Unused

Fmt 7 - Byte 8 **String Features** **SENSE-62**

Byte 8 will contain x'FF' if the data for this byte was not available to the storage control at the time of sense assembly.

Bit	N	Bit Name	
0		Dynamic Path Selection Function Installed in Controllers	SENSE-62
1		String Has Four Path Capability	SENSE-62
2		Second CDP Card Installed	SENSE-62
3		Reserved	
4		3380 Model CJ2	
5	0	Always Zero (Controller type definition, set to 0 for 3380-JK)	
6	0	Always Zero (Controller type definition, set to 0 for 3380-JK)	
7	1	3380-JK	SENSE-62

Fmt 7 - Byte 9 **DDC Bus In**

Byte 9 indicates the selection response received by the storage control and is valid only when Byte 7 indicates message 5. At other times this byte contains the contents of Bus In 1 when the RCC sequence was executed.

Fmt 7 - Byte 10 **Storage Control Data Transfer Error Bits** **SENSE-77**

Bit	N	Prty	PSC	Bit Name		
0	0		DF80	Connection Check Alert	SENSE-77	ECD-256
1	0	123	DF40	Tag-In Check	SENSE-77	ECD-258
2	0	108	DF20	Sync-In Check	SENSE-77	ECD-259
3	0	107	DF10	DDC Bus In Parity Check	SENSE-77	ECD-261
4	0			DDC Tag-In Null Disconnect	SENSE-77	
5	0			DDC Tag-In Sync In or Valid	SENSE-78	
6	0			DDC Tag-In Selected Null	SENSE-78	
7	0			DDC Tag-In End-Op	SENSE-78	

Fmt 7 - Byte 11 **Connection Check Alert and Power Status** **SENSE-78**

Bit	N	Prty	PSC	Bit Name		
0	0		D18X	Controller 0 Connection Check Alert	SENSE-78	ECD-262
1	0		D14X	Controller 1 Connection Check Alert	SENSE-78	ECD-262
2	0		D12X	Controller 0 DPS Unconditional Reserve Release	SENSE-78	ECD-265
3	0		D11X	Controller 1 DPS Unconditional Reserve Release	SENSE-78	ECD-265
4	0			Always 0 for 3380-JK; 3380 - Model A D E, Power On	"F^{7}B^{11} - BITS 4 - FOR 3380-JK, ZERO" on page SENSE-78	
5	0			Always 0 for 3380-JK; 3380 - Model A D E, Power On	"F^{7}B^{11} - BITS 4 - FOR 3380-JK, ZERO" on page SENSE-78	
6	1			Controller 0 3380-JK Power On.	SENSE-78	
7	1			Controller 1 3380-JK Power On.	SENSE-78	

Fmt 7 - Byte 12 **Controller 0 Check-1 Status 1** **SENSE-79**

Bit	N	Prty	PSC	Bit Name		
012				IOC Card Isolation Bits 0,1,2	SENSE-78	
000	0			No Error		
001	0	110	D220	IOC ROS Bit Parity Check (of the Controller Sequencer)		ECD-267
010	0	115	D240	IOC Transfer Clock Check		ECD-269
011	0	111	D260	IOC Detected DDC Bus Out Parity Check		ECD-271
100	0	104	D280	IOC Register Data Bus Parity Check		ECD-273
101	0	112	D2A0	IOC Register 1 Parity Check (CTL-I Bus In)		ECD-274
110	0	113	D2C0	IOC Register 3 Parity Check (CDP Bus Out)		ECD-277
111	0	114	D2E0	IOC Controller Selection Check		ECD-279
3	0	116	D210	DDC Bus Out Parity Check	SENSE-79	ECD-281
4	0	103	D208	Controller Clock Check	SENSE-79	ECD-282
5	0	105	D7XX	Controller Sequencer Check	SENSE-79	ECD-284
6	0	107	D202	DDC Bus In Parity Check	SENSE-79	ECD-285
7	0	106	D201	IOC Card Check-1	SENSE-79	ECD-287

Fmt 7 - Byte 13 **Controller 0 Check-1 Status 2** **SENSE-79**

Bit	N	Prty	PSC	Bit Name		
0	0	117	D380	DDC Tag-Out Sequence Check	SENSE-79	ECD-289
1	0	118	D340	Extended Command, Tag Sequence Check	SENSE-79	ECD-291
2	0	121	D6XX	Controller Sequencer Microcode Detected Check-1	SENSE-80	ECD-292
3	0	119	D310	Controller Gate DDC Drivers Check	SENSE-80	ECD-294
4	0	120	D308	RCC Sequence Check	SENSE-80	ECD-295
5	0			Unused		
6	0			Unused		
7	0			Unused		

Fmt 7 - Byte 14 **Controller 1 Check-1 Status 1** **SENSE-79**

Bit	N	Prty	PSC	Bit Name		
012				IOC Card Isolation Bits 0,1,2	SENSE-79	
000	0			No Error		
001	0	110	D420	IOC ROS Bit Parity Check (of the Controller Sequencer)		ECD-267
010	0	115	D440	IOC Transfer Clock Check		ECD-269
011	0	111	D460	IOC Detected DDC Bus Out Parity Check		ECD-271
100	0	104	D480	IOC Register Data Bus Parity Check		ECD-273
101	0	112	D4A0	IOC Register 1 Parity Check (CTL-I Bus In)		ECD-274
110	0	113	D4C0	IOC Register 3 Parity Check (CDP Bus Out)		ECD-277
111	0	114	D4E0	IOC Controller Selection Check		ECD-279
3	0	116	D410	DDC Bus Out Parity Check	SENSE-79	ECD-281
4	0	103	D408	Controller Clock Check	SENSE-79	ECD-282
5	0	105	D9XX	Controller Sequencer Check	SENSE-79	ECD-284
6	0	107	D402	DDC Bus In Parity Check	SENSE-79	ECD-285
7	0	106	D401	IOC Card Check-1	SENSE-79	ECD-287

Fmt 7 - Byte 15 **Controller 1 Check-1 Status 2** **SENSE-79**

Bit	N	Prty	PSC	Bit Name		
0	0	117	D580	DDC Tag-Out Sequence Check	SENSE-79	ECD-289
1	0	118	D540	Extended Command, Tag Sequence Check	SENSE-79	ECD-291
2	0	121	D8XX	Controller Sequencer Microcode Detected Check-1	SENSE-80	ECD-292
3	0	119	D510	Controller Gate DDC Drivers Check	SENSE-80	ECD-294
4	0	120	D508	RCC Sequence Check	SENSE-80	ECD-295
5	0			Unused		
6	0			Unused		
7	0			Unused		

Fmt 7 - Byte 16 **Controller 0 Sequencer Microcode Detected Errors** **SENSE-80**

For additional details see SENSE-80

Fmt 7 - Byte 17 **Controller 0 RCC Transfer Status** **SENSE-81**

Bit	N	Prty	PSC	Bit Name		
0	1	102	DFFF	Controller Undervoltage	SENSE-81	ECD-407
1&2				Controller Location in String	SENSE-81	
0 0				Controller A1		
0 1				Controller A2		
1 0				Controller A3 in the 4 path connection		
1 1				Controller A4 in the 4 path connection		
3	1			Always 1	SENSE-81	
4	1			Power Sequence Complete	SENSE-81	
5	0			Check 2 Active	SENSE-82	
6	1			Successful Transfer Complete	SENSE-82	
7	0			Always 0	SENSE-82	

Fmt 7 - Byte 18 **Controller 1 Sequencer Microcode Detected Errors** **SENSE-80**

For additional details see SENSE-80

Fmt 7 - Byte 19 **Controller 1 RCC Transfer Status** **SENSE-81**

Bit	N	Prty	PSC	Bit Name		
0	1	102	DFFF	Controller Undervoltage	SENSE-81	ECD-407
1&2				Controller Location in String	SENSE-81	
0 0				Controller A1		
0 1				Controller A2		
1 0				Controller A3 in the 4 path connection		
1 1				Controller A4 in the 4 path connection		
3	1			Always 1	SENSE-81	
4	1			Power Sequence Complete	SENSE-81	
5	0			Check 2 Active	SENSE-82	
6	1			Successful Transfer Complete	SENSE-82	
7	0			Always 0	SENSE-82	

Fmt 7 - Byte 20 with Byte 7 not equal to x'74, 7C, or 7D' — **Unused**

Fmt 7 - Byte 20 with Byte 7 = x'74, 7C, or 7D' — **Initial Error Message**

If the storage control cannot communicate with the controller because of message 4, or C conditions, this byte will contain byte 7 of the initial error data.

If the storage control cannot communicate with the controller because of message D conditions, this byte may not be valid on the first reporting of 7D, but all subsequent 7D's will contain byte 7 of the initial error data.

Fmt 7 - Byte 21 — **Subsystem or Storage Director Physical ID**

This byte is the Storage Director Physical ID when 3380-JK is attached to a 3880. This byte identifies the attached storage director at the time of this sense collection.

When 3380-JK is attached to 3990, this byte is the low order byte of the Subsystem ID. With the Path In Use bits of byte 4, it identifies the storage director attached at the time of this sense collection.

Fmt 7 - Byte 22 and 23 — **Symptom Code**

These bytes are a summary of the error condition indicated in the prior 22 bytes.

Format 7 symptom codes all start with the character D, for example DXXX.

Fmt 7- Byte 24 — **Flags**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Reserved, set to 0
1	Reserved, set to 0
2	Reserved, set to 0
3	Logging Mode
4&5	Logging Control Bits (with 3990 Only)
0 0	Do Not Log
0 1	Log Unconditionally
1 0	Log First Occurrence of This Retry Sequence
1 1	Log First Occurrence of This Retry Sequence If Permanent Error On This Path
6&7	Operator Message Control
0 0	Send No Message to Operator
0 1	Send Message to Operator Unconditionally
1 0	Send Message to Operator On the First Record for This Retry Sequence

Bit	Bit Name
1 1	Send Message to Operator on the First Record for This Retry Sequence if Permanent Error on This Path

Fmt 7- Byte 25 **Action Code**

This byte identifies the Action Code used by 3990. Refer to the 3990 Maintenance Manuals for the definition of this byte.

Fmt 7 - Byte 26 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Dual Frame Storage Control
1	4 Path Device Level Selection
2	Duplex Pair Volume
3	Secondary Device of a Duplex Pair
4	Sense Presented to Relevant Channel
5	Sense Presented to Relevant Device Number
6	Put Record into System Exception Report
7	Alternate Internal Path Will Be Tried

Fmt 7 - Byte 27 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Twenty-four Byte Capability
1	Device Address Valid in Byte 4
2	Track Address Present in Bytes 29 thru 31
3	Reserved, Set to 0
4	Reserved, set to 0
5	Reserved, set to 0
6	Cluster
7	Storage Path

Fmt 7- Byte 28 **Message Code**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	ERP, Prepare a SIM Message
1-7	Format of the SIM Message

Fmt 7- Byte 29 **Seek Cylinder Address High**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Cylinder 2048
5	Cylinder 1024
6	Cylinder 512
7	Cylinder 256

Fmt 7- Byte 30 **Seek Cylinder Address Low**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 7- Byte 31 **Seek Head Address**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Format 8

Format 8 is generated when:
Either a controller check-2 or drive check-1 equipment check occurs.

Fmt 8 - Byte 0 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Command Rejected	SENSE-59
1	0	Intervention Required	SENSE-59
2	0	Channel Bus Out Parity Check	SENSE-59
3	0	Equipment Check	SENSE-59
4	0	Data Check	SENSE-59
5	0	Overrun	SENSE-59
6	0	Unused	
7	0	Unused	

Fmt 8 - Byte 1 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Permanent Error	SENSE-60
1	0	Invalid Track Format	SENSE-60
2	0	End of Cylinder	SENSE-60
3	0	Message to Operator	SENSE-60
4	0	No Record Found	SENSE-60
5	0	File Protected	SENSE-60
6	0	Write Inhibited	SENSE-60
7	0	Imprecise Ending	SENSE-60

Fmt 8 - Byte 2 **Unit Check Description** **SENSE-60**

Bit	N	Bit Name	
0	0	Request Write Inhibit	SENSE-60
1	0	Correctable	SENSE-60
2	0	First Error Logged	SENSE-60
3	0	Environmental Data Present	SENSE-61
4	0	Intent Violation	SENSE-61
5	0	Imprecise Ending	SENSE-61
6	0	Write Operation in Progress	SENSE-61
7	0	3880 Model 23 Storage Control	SENSE-61

Fmt 8 - Byte 3 **String ID** **SENSE-61**

This byte identifies the string in which the controller resides. The controller is identified by the Path In Use bits of byte 4.

Fmt 8 - Byte 4 — **Path and Device Physical Identifier**

Bit	Bit Name	
0	Path In Use / Controller Response Bit 0	SENSE-61
1	Path In Use / Controller Response Bit 1	SENSE-61
2	String Address Bit (0 or 1)	SENSE-62
3-7	Device Address Bits (x'00' through x'1F')	SENSE-62

Fmt 8 - Byte 5 — **Seek Low Cylinder Address** — **SENSE-62**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 8 - Byte 6 — **Seek Head and High Cylinder Address** — **SENSE-62**

Bit	Bit Name
0	Cylinder 2048
1	Cylinder 1024
2	Cylinder 512
3	Cylinder 256
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Fmt 8 - Byte 7 **Format and Message** **SENSE-62**

Equals	Prty	PSC	Message		
x'80'			No Message		
x'81'	248	EF81	Error Correction Code Logic Check	ECD-331	
x'82'			Reserved		
x'83'	253	EDXX	Unexpected End Operation Response Code Received	ECD-332	
x'84'	254	EDXX	End Operation Received With Transfer Count Not Equal To Zero	ECD-333	
x'85'	255	EDXX	End Operation Received With Transfer Count Equal To Zero	ECD-334	
x'86'	249	EF86	DPS Cleanup Checks on Channel or System Reset	ECD-335	
x'87'	250	EF87	DPS Array Cannot Be Initialized	ECD-337	
x'88'	251	EF88	Short Busy Time-out During Device Selection	ECD-339	
x'89'	252	EF89	Controller Failed To Either Set or Reset Long Busy Latch	ECD-340	
x'8A'	256	EF8A	Missing Device Interrupt Detected by the Storage Control While it was Processing an nternal Command Chain	SENSE-91	ECD-343

Messages B through F - Unused

Fmt 8 - Byte 8 **String Features** **SENSE-62**

Byte 8 will contain x'FF' if the data for this byte was not available to the Storage Director at the time of sense assembly.

Bit	N	Bit Name	
0		Dynamic Path Selection Function Installed in Controllers	SENSE-62
1		String Has Four Path Capability	SENSE-62
2		Second CDP Card Installed	SENSE-62
3		Reserved	
4		3380 Model CJ2	
5	0	Always Zero (Controller type definition, set to 0 for 3380-JK)	
6	0	Always Zero (Controller type definition, set to 0 for 3380-JK)	
7	1	3380-JK	SENSE-62

Fmt 8 - Byte 9 with Byte 7 not equal to x'83, 84 or 85' **DDC Bus In**

Byte 9 will contain the DDC Bus In bit configuration at the storage control end of the bus when the storage control recognized that an error occurred.

Fmt 8 - Byte 9 with Byte 10 bit 7 equal to 1, or Byte 7 is equal to x'83, 84 or 85' **End Operation Codes**

Bit 0 = Index
Bit 1 = No Sync and No Data

The hex codes below (bits 2 through 7) are ORed with the bits above and result in the final contents of the End Op byte.

Bits 2-7 Equals	Prty	PSC	End Operation		
'00'			Operation successfully completed, No Error		
'01'	257	ED01	DDC Command Overrun	ECD-344	
'02'		4XYY	Sync Byte Missing - The storage control collects format 4 sense data.	ECD-233	
'03'		4XYY	Data Check - The storage control collects format 4 sense data.	ECD-235	
'04'		4XY4	Data Check - With a controller undervoltage condition.	ECD-235	
'06'	202	ED06	Invalid Command Code	ECD-346	
'07'	203	ED07	DDC Data Overrun	ECD-348	
'08'	261	ED08	HAR Modifier Overrun On Set HAR Oriented	ECD-349	
'09'	237	9F15	Device Not Responding to Selection	ECD-8	
'0D'		4XYY	No Read Data Found	ECD-237	
'10'	245	ED10	Check 2 Detected in Controller	ECD-351	
'11'	235	ED11	Device Check-1 on Selection	ECD-353	
'12'	258	E8XX	Controller Sequencer Microcode Detected Error	ECD-355	SENSE-87
'13'	234	ED13	CDP Hung Due to Late or Missing Device Response	ECD-388	
'16'	214	ED16	Data Check on Start Read/Write	ECD-390	
'17'	204	ED17	Any Check, but Controller Collected No Status	ECD-391	
'18'	205	ED18	Sync Out/In Tag Counts Not Equal	ECD-393	
'19'	259	ED19	Device Dropped to Null	ECD-394	
'1B'	260	ED1B	Index Found During Defect Skip in HA	ECD-395	
'20'			Device Check Active - The storage control collects Format 1 or 9 sense data. (Format 9 when only Byte 11 Bit 5 is active or message 7, A or E.)	ECD-397	

Fmt 8 - Byte 10 **Storage Control Data Transfer Error Bits** **SENSE-77**

Bit	N	Prty	PSC	Bit Name		
0	0			Connection Check Alert	SENSE-77	ECD-256
1	0	239	E04X	Tag-In Check	SENSE-77	ECD-258
2	0	240	E02X	Sync-In Check	SENSE-77	ECD-259
3	0	241	E01X	DDC Bus In Parity Check	SENSE-77	ECD-261
4	0			DDC Tag-In Null Disconnect	SENSE-77	
5	0			DDC Tag-In Sync In or Valid	SENSE-78	
6	0			DDC Tag-In Selected Null	SENSE-78	
7	0			DDC Tag-In End-Op	SENSE-78	

Fmt 8 - Byte 11 **Controller Fault Log A** **SENSE-82**

Bit	N	Prty	PSC	Bit Name		
0	0	219	E180	DHPLO Delta Frequency Check	SENSE-82	ECD-398
1	0	221	E140	DHPLO Non-Drive Check	SENSE-82	ECD-399
2	0	220	E120	Read/Write Data Cable Check	SENSE-82	ECD-401
3	0	236	E110	Data Valid Check	SENSE-82	ECD-402
4	0	217	E108	DHPLO Failed to Lock Check	SENSE-82	ECD-403
5	0	218	E104	DHPLO Multiple Select Check	SENSE-82	ECD-404
6	0	222	E102	No Read Data Check	SENSE-82	ECD-406
7	0	201	EFFF	Controller Undervoltage Test	ECD-407	

Fmt 8 - Byte 12 **Controller Fault Log B** **SENSE-83**

Bit	N	Prty	PSC	Bit Name		
0	0	213	E280	SERDES Control Check	SENSE-83	ECD-408
1	0	214	E240	Clock/SERDES/ECC Card Check	SENSE-83	ECD-409
2	0	238	E220	SERDES Path Check	SENSE-83	ECD-411
3	0			Unused		
4	0			SERDES 2 Card Installed	SENSE-83	
5	0			Unused		
6	0			Unused		
7	0			Unused		

Fmt 8 - Byte 13 **Controller Fault Log C** **SENSE-83**

Bit	N	Prty	PSC	Bit Name		
0	0			Unused		
1	0	251	E340	Controller Sequencer Check-2	SENSE-83	ECD-412
2				Unused (May be either a zero or one.)	SENSE-83	
3	0	206	E310	Multiplexer Input Parity Check	SENSE-83	ECD-413
4	0	212	E308	CDP Register 3 Parity Check	SENSE-83	ECD-414
5	0	215	E304	IOC Card Check-2	SENSE-83	ECD-415
6	0	216	E302	Precompensation Check	SENSE-83	ECD-417
7	0	223	E301	Write Gap 3 Control Check	SENSE-83	ECD-418

Fmt 8 - Byte 14 **Controller Fault Log D** **SENSE-84**

Bit	N	Prty	PSC	Bit Name		
0	0	233	EE80	Device xx00 Check-1	SENSE-84	ECD-419
1	0	233	EE40	Device xx01 Check-1	SENSE-84	ECD-419
2	0	233	EE20	Device xx10 Check-1	SENSE-84	ECD-419
3	0	233	EE10	Device xx11 Check-1	SENSE-84	ECD-419
4 5				Isolation Bits 0 and 1	SENSE-84	ECD-419
0 0	0	232	EEX0	Tie-Break Check		
0 1	0	225	EEX4	Clock Check		
1 0	0	227	EEX8	Port Card Check		
1 1	0	226	EEXC	CDP Interface Check		
6				CDP Port Selection Bit 0 [1]	SENSE-84	ECD-419

Bit	N	Prty	PSC	Bit Name		
7				CDP Port Selection Bit 1 [1]	SENSE-84	ECD-419

Fmt 8 - Byte 15 **Controller Fault Log E** **SENSE-85**

This byte should only indicate errors when a DPS card is installed in the controller.

Bit	N	Prty	PSC	Bit Name		
0	0	242	E580	DPS Array Check	SENSE-85	ECD-421
1	0	243	E540	DPS Internal Check	SENSE-85	ECD-423
2	0	244	E520	DPS Compare Check	SENSE-85	ECD-424
3	0	245	E510	DPS Controller to Controller Connection Check	SENSE-85	ECD-425
4	0	246	E508	DPS Storage Address Register Check	SENSE-85	ECD-426
5	0	247	E504	DPS Internal Register Check	SENSE-85	ECD-427
6	0	248	E502	DPS Alternate Check (Wait/Lock Check)	SENSE-85	ECD-429
7	0			Unused		

Fmt 8 - Byte 16 **Controller Fault Log F** **SENSE-85**

Bit	N	Prty	PSC	Bit Name		
0	0	208	E68X	DTB Bus Out Parity Check	SENSE-85	ECD-430
1	0	209	E64X	DTB Bus In Parity Check	SENSE-85	ECD-431
2	0	210	E62X	DTB Control Check	SENSE-85	ECD-432
3	0	207	E61X	Read/Write Gate DDC Drivers Check	SENSE-86	ECD-433
4	0			String Configuration Switch 1	SENSE-86	
5	0			String Configuration Switch 2	SENSE-86	
6	0			String Configuration Switch 3	SENSE-86	
7	0			String Configuration Switch 4	SENSE-86	

Fmt 8 - Byte 17 **Controller Fault Log G** **SENSE-86**

Bit	N	Prty	PSC	Bit Name		
0	0	230	E78X	Controller to CDP Card Check	SENSE-86	ECD-436
1	0	231	EBXX	Drive to CDP Card Check	SENSE-86	ECD-438
2	0	228	E720	Port Response Check	SENSE-86	ECD-440
3	0	224	EBXX	CDP Active Drivers Check	SENSE-86	ECD-441
4	0	211	EBXX	Selected Device Check-1	SENSE-86	ECD-442
5				Sub String 0 Selected	SENSE-87	
6				Sub String 1 Selected	SENSE-87	
7	0	229	E701	Port Degate Check	SENSE-87	ECD-444

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1 These bits, byte 14, bits 6 and 7 can only be used along with byte 17 bits 5 and 6. See "F[8]B[14] - BITS 6 AND 7 — CDP PORT SELECTION BITS 0, 1" on page SENSE-84.

Fmt 8 - Byte 18 with Byte 9 End Op code equal to 12 **Controller Sequencer Microcode Detected Check 2** **SENSE-87**

Byte 18 displays the sequencer microcode detected Check 2 errors of the Controller, only when Format 8 Byte 9 contains an End Op code of 12. See SENSE-87

Byte 9 End Op code not equal to 12

If the End Op code is not 12 in byte 9, Byte 18 will contain, in most instances, the last DDC Read/Write command from the storage control to the controller prior to the error.

Fmt 8 - Byte 19 **Device Status 1** **SENSE-74**

Bit	N	Bit Name		
0	0	Padding In Progress	SENSE-74	
1		Device Model	SENSE-74	
2	0	Always Zero	SENSE-74	
3	0	Device Error	SENSE-74	ECD-487
4	1	Online	SENSE-75	
5	0	HDA Attention	SENSE-75	
6	0	Device Busy	SENSE-75	
7	0	Locate Interrupt	SENSE-75	

Fmt 8 - Byte 20 **Device Status 2** **SENSE-75**

Bit	N	Prty	PSC	Bit Name		
0	0			Device Logic Disabled	SENSE-75	
1	0			Servo Inhibit	SENSE-75ECD-229	
2	0			Offset Active	SENSE-75	
3	0			Drive Motor Switch Off	SENSE-75	
4	0			Access Mechanism Logic Exchanged	SENSE-75	
5	0			Device Switch Set to Disable	SENSE-75	
6	0	301	9FFF	Logic Voltage Status	SENSE-75	ECD-230
7	0			Seek Incomplete	SENSE-75	ECD-232

Fmt 8 - Byte 21 **Subsystem or Storage Director Physical ID**

This byte is the Storage Director Physical ID when 3380-JK is attached to a 3880. This byte identifies the attached storage director at the time of this sense collection.

When 3380-JK is attached to 3990, this byte is the low order byte of the Subsystem ID. With the Path In Use bits of byte 4, it identifies the storage director attached at the time of this sense collection.

Fmt 8 - Byte 22 and 23 **Symptom Code**

These bytes are a summary of the error condition indicated in the prior 22 bytes.

Format 8 symptom codes all start with the character E, for example EXXX.

Fmt 8 - Byte 24 **Flags**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Reserved, set to 0
1	Reserved, set to 0
2	Reserved, set to 0
3	Logging Mode
4&5	Logging Control Bits (with 3990 Only)
0 0	Do Not Log
0 1	Log Unconditionally
1 0	Log First Occurrence of This Retry Sequence
1 1	Log First Occurrence of This Retry Sequence If Permanent Error On This Path
6&7	Operator Message Control
0 0	Send No Message to Operator
0 1	Send Message to Operator Unconditionally
1 0	Send Message to Operator On the First Record for This Retry Sequence
1 1	Send Message to Operator on the First Record for This Retry Sequence if Permanent Error on This Path

Fmt 8 - Byte 25 **Action Code**

This byte identifies the Action Code used by 3990. Refer to the 3990 Maintenance Manuals for the definition of this byte.

Fmt 8 - Byte 26 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Dual Frame Storage Control
1	4 Path Device Level Selection
2	Duplex Pair Volume
3	Secondary Device of a Duplex Pair
4	Sense Presented to Relevant Channel
5	Sense Presented to Relevant Device Number
6	Put Record into System Exception Report
7	Alternate Internal Path Will Be Tried

Fmt 8 - Byte 27 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Twenty-four Byte Capability
1	Device Address Valid in Byte 4
2	Track Address Present in Bytes 29 thru 31
3	Reserved, Set to 0
4	Reserved, set to 0
5	Reserved, set to 0
6	Cluster
7	Storage Path

Fmt 8 - Byte 28 **Message Code**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	ERP, Prepare a SIM Message
1-7	Format of the SIM Message

Fmt 8 - Byte 29 **Seek Cylinder Address High**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Cylinder 2048
5	Cylinder 1024
6	Cylinder 512
7	Cylinder 256

Fmt 8 - Byte 30 **Seek Cylinder Address Low**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 8 - Byte 31 **Seek Head Address**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Format 9

Format 9 is generated when one of the following conditions is encountered:

- Detection of only a Read/Write Check.

  It is indicated by an active bit 5 only in byte 11. In this case, Equipment Check (byte 0 bit 3) is set. If bit 5 is active along with other bits in byte 11, a Format 1 sense record is generated. If the error is detected on an asynchronous operation, byte 2 bit 3 (environmental data present) is also set. Byte 1, bit 0 (permanent error) is set if the internal retries are not successful.

- Detection of a permanent storage control microcode detected seek check. The message code in byte 7, of x'97', x'9A', or x'9E', will specify the type of seek error. Equipment Check (byte 0, bit 3) and Permanent Error (byte 1, bit 0) are set. If the error occurred on an asynchronous operation, byte 2, bit 3 (environmental data present) is also set.

- Successfully retried microcode seek checks are off loaded if they occurred during error logging mode or forced error logging mode. Environmental Data Present (byte 2, bit 3) is set.

Fmt 9 - Byte 0 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Command Rejected	SENSE-59
1	0	Intervention Required	SENSE-59
2	0	Channel Bus Out Parity	SENSE-59
3	0	Equipment Check	SENSE-59
4	0	Data Check	SENSE-59
5	0	Overrun	SENSE-59
6	0	Unused	
7	0	Unused	

Fmt 9 - Byte 1 **Unit Check Description** **SENSE-59**

Bit	N	Bit Name	
0	0	Permanent Error	SENSE-60
1	0	Invalid Track Format	SENSE-60
2	0	End of Cylinder	SENSE-60
3	0	Message to Operator	SENSE-60
4	0	No Record Found	SENSE-60
5	0	File Protected	SENSE-60
6	0	Write Inhibited	SENSE-60
7	0	Imprecise Ending	SENSE-60

Fmt 9 - Byte 2 **Unit Check Description** **SENSE-60**

Bit	N	Bit Name	
0	0	Request Write Inhibit	SENSE-60
1	0	Correctable	SENSE-60
2	0	First Error Logged	SENSE-60
3	0	Environmental Data Present	SENSE-61
4	0	Intent Violation	SENSE-61
5	0	Imprecise Ending	SENSE-61
6	0	Write Operation in Progress	SENSE-61
7	0	3880 Model 23 Storage Control	SENSE-61

Fmt 9 - Byte 3 **String ID** **SENSE-61**

This byte identifies the string in which the device resides. The controller is identified by the Path In Use bits of byte 4.

Fmt 9 - Byte 4 **Path and Device Physical Identifier** **SENSE-61**

Bit	Bit Name	
0	Path In Use / Controller Response Bit 0	SENSE-61
1	Path In Use / Controller Response Bit 1	SENSE-61
2	String Address Bit (0 or 1)	SENSE-62
3-7	Device Address Bits (x'00' through x'1F')	SENSE-62

Fmt 9 - Byte 5 **Seek Low Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 9 - Byte 6 **Seek Head and High Cylinder Address** **SENSE-62**

Bit	Bit Name
0	Cylinder 2048
1	Cylinder 1024
2	Cylinder 512
3	Cylinder 256
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Equals	Prty	PSC	Message	
x'90'			No Message	
x'91'			Not Used	
x'92'			Not Used	
x'93'			Not Used	
x'94'			Not Used	
x'95'			Not Used	
x'96'			Device Check-2	
x'97'	403	9F97	Head Address Miscompare	ECD-446
x'98'			Not Used	
x'99'			Not Used	
x'9A'	404	9F9A	Track Physical Address Miscompare While Oriented	ECD-447
x'9B'			Not Used	
x'9C'			Not Used	
x'9D'			Not Used	
x'9E'	405	9F9E	Cylinder Address Miscompare	ECD-448
x'9F'			Not used	

Fmt 9 - Byte 8 **String Features** **SENSE-62**

Bit	N	Bit Name	
0		Dynamic Path Selection Function Installed in Controllers	SENSE-62
1		String Has Four Path Capability	SENSE-62
2		Second CDP Card Installed	SENSE-62
3		Reserved	
4		3380 Model CJ2	
5	0	Always Zero (Controller type definition, set to 0 for 3380-JK)	
6	0	Always Zero (Controller type definition, set to 0 for 3380-JK)	
7	1	3380-JK	SENSE-62

Fmt 9 - Byte 9 with Byte 7 not equal to x'90' **DDC Bus In**

Byte 9 may contain the DDC Bus In bit configuration at the storage control end of the bus when the storage control recognized that an error occurred.

Because of storage control recovery procedures for Format 9 the contents of this byte cannot be guaranteed.

Fmt 9 - Byte 9 with Byte 7 = x'90' — **End Operation Codes**

Bit 0 = Index
Bit 1 = No sync and no data

The hex codes below (bits 2 through 7) are ORed with the bits above and result in the final contents of the End Op byte.

Bits 2-7 Equals	Prty	PSC	End Operation		
'00'			Operation successfully completed, No Error		
'01'	257	ED01	DDC Command Overrun	ECD-344	
'02'		4XYY	Sync Byte Missing - The storage control collects format 4 sense data.	ECD-233	
'03'		4XYY	Data Check - The storage control collects format 4 sense data.	ECD-235	
'04'		4XY4	Data Check - With a controller undervoltage condition.	ECD-235	
'06'	202	ED06	Invalid Command Code	ECD-346	
'07'	203	ED07	DDC Data Overrun	ECD-348	
'08'		ED08	HAR Modifier Overrun On Set HAR Oriented	ECD-349	
'09'	237	9F15	Device Not Responding to Selection	ECD-8	
'0D'		4XYY	No Read Data Found	ECD-237	
'10'	245	ED10	Check 2 Detected in Controller	ECD-351	
'11'	235	ED11	Device Check-1 on Selection	ECD-353	
'12'	258	E8XX	Controller Sequencer Microcode Detected Error	ECD-355	SENSE-87
'13'	234	ED13	CDP Hung Due to Late or Missing Device Response	ECD-388	
'16'		ED16	Data Check on Start Read/Write	ECD-390	
'17'	204	ED17	Any Check, but Controller Collected No Status	ECD-391	
'18'	205	ED18	Sync Out/In Tag Counts Not Equal	ECD-393	
'19'	259	ED19	Device Dropped to Null	ECD-394	
'1B'	260	ED1B	Index Found During Defect Skip in HA	ECD-395	
'20'			Device Check Active - The storage control collects Format 1 or 9 sense data. (Format 9 when only Byte 11 Bit 5 is active or message 7, A or E.)	ECD-397	

Fmt 9 - Byte 10 — **Device Power Status** — **SENSE-63**

Bit	N	Prty	PSC	Bit Name		
0	0			Motor Start Surge Complete	SENSE-63	
1	0			Unused		
2	0	908	9020	No Air Flow	SENSE-63	ECD-17
3	1			Device Power On Sequence Complete	SENSE-63	
4	1			Spindle Motor Started by Device Sequencer	SENSE-63	
5	1			Spindle Control Bit 0	SENSE-63	
6	1			Motor Brake Latch	SENSE-63	
7	0			Spindle Control Bit 1	SENSE-63	

Fmt 9 - Byte 11 **Device Check-2 Status** **SENSE-63**

Bit	N	Prty	PSC	Bit Name		
0	0	307	9180	Device Sequencer Check	SENSE-63	ECD-18
1	0	308	97XX	Servo Control Check	SENSE-64	ECD-19
2	0	309	9120	Rotational Position Sensing (RPS) Check	SENSE-64	ECD-20
3	0	310	95XX	Checkpoint Check See Checkpoint Log, byte 15 on SENSE-66	SENSE-63	ECD-22
4	0	323	9108	HDA Cable Swap Check	SENSE-64	ECD-23
5	0	402	9104	Read/Write Check	SENSE-64	ECD-448
6	0	304	9102	Power Card Check	SENSE-64	ECD-24
7	0	305	9101	Funnel Parity Check	SENSE-64	ECD-26

Fmt 9 - Byte 12 **Read/Write Status-1** **SENSE-88**

Bit	N	Prty	PSC	Bit Name		
0	0	424	92XX	FRU Bit 0	SENSE-88	ECD-451
1	0	424	9840	FRU Bit 1	SENSE-88	ECD-451
2	0	407	9220	Redundant Line / Selection Check	SENSE-88	ECD-452
3	0	408	9210	No Read/Write Recovery	SENSE-89	ECD-454
4	0	409	9208	Inhibit Or Reset Active	SENSE-89	ECD-455
5	0	410	9204	Read and Write Check	SENSE-89	ECD-456
6	0	411	9202	HAR Bus Parity Check	SENSE-89	ECD-458
7	0	412	9201	Data Detector Check	SENSE-89	ECD-459

Fmt 9 - Byte 13 **Read/Write Status-2** **SENSE-89**

Bit	N	Prty	PSC	Bit Name		
0	0	406	92XX	Read/Write Channel Check	SENSE-89	ECD-461
1	0	413	9340	Padding Check	SENSE-89	ECD-462
2	0	414	9320	Read/Write Sequence Check	SENSE-89	ECD-465
3	0	415	9310	Index / Cell Check	SENSE-89	ECD-467
4	0	416	9308	Servo Cable Check	SENSE-89	ECD-468
5	0	417	9304	Write Overrun Check	SENSE-90	ECD-469
6	0	418	9302	Read/Write Servomechanism Check	SENSE-90	ECD-470
7	0	419	9301	Head Address Register Parity Check	SENSE-90	ECD-472

Fmt 9 - Byte 14 **Read/Write Status-3** **SENSE-90**

Bit	N	Prty	PSC	Bit Name		
0	0	420	9480	Check Inhibit Check	SENSE-90	ECD-473
1	0	421	9440	Read/Write Channel Status Parity Check	SENSE-90	ECD-474
2	0	422	9420	Read Transmit Check	SENSE-90	ECD-475
3	0	423	9410	Read/Write Control Cable Check	SENSE-90	ECD-477
4	0			Read Transmit Active	SENSE-90	ECD-477
5	0			Write Gate Active	SENSE-90	ECD-478
6	0			Unused		
7				Unused (May be either a zero or one.)	SENSE-90	

Fmt 9 - Byte 15 **Device Checkpoint Log** **SENSE-66**

For details see SENSE-66

Fmt 9 - Bytes 16 and 17 **Track Physical Address Read**

With Byte 7 equal to x'97', '9A', or '9E'

If the message in byte 7 is 7, A, or E, byte 16 contains the high order byte of the head and cylinder address that were read from the disk. Byte 17 will contain the low order byte. For Cylinder Address see bytes 5 and 6 for bit assignments, on SENSE-5.

With any other Byte 7 messages

For any other Format 9 messages, bytes 16 and 17 will be zero.

Fmt 9 - Byte 18 **Read/Write Status 4** **SENSE-90**

Bit	N	Bit Name		
0	0	FRU Bit 0	SENSE-90	ECD-451
1	0	FRU Bit 1	SENSE-90	ECD-451
2	0	Multifunction	SENSE-91	ECD-479
3	0	No Function	SENSE-91	ECD-481
4	0	Arm Electronics Selected	SENSE-91	ECD-482
5	0	Write Mode Verify	SENSE-91	ECD-484
6	0	Arm Electronics Status 2	SENSE-91	ECD-485
7	0	Arm Electronics Status 1	SENSE-91	ECD-485

Fmt 9 - Byte 19 **Device Status 1** **SENSE-74**

Bit	N	Bit Name		
0	0	Padding In Progress	SENSE-74	
1		Device Model	SENSE-74	
2	0	Always Zero	SENSE-74	
3	0	Device Error	SENSE-74	ECD-487
4	1	Online	SENSE-75	
5	0	HDA Attention	SENSE-75	
6	0	Device Busy	SENSE-75	
7	0	Locate Interrupt	SENSE-75	

Fmt 9 - Byte 20 **Device Status 2** **SENSE-75**

Bit	N			Bit Name		
0	0			Device Logic Disabled	SENSE-75	
1	0			Servo Inhibit	SENSE-75	ECD-229
2	0			Offset Active	SENSE-75	
3	0			Drive Motor Switch Off	SENSE-75	
4	0			Access Mechanism Logic Exchanged	SENSE-75	
5	0			Device Switch Set to Disable	SENSE-75	
6	0	301	9FFF	Device Logic Undervoltage Status	SENSE-75	ECD-230
7	0			Seek Incomplete	SENSE-75	ECD-232

Fmt 9 - Byte 21 **Subsystem or Storage Director Physical ID**

This byte is the Storage Director Physical ID when 3380-JK is attached to a 3880. This byte identifies the attached storage director at the time of this sense collection.

When 3380-JK is attached to 3990, this byte is the low order byte of the Subsystem ID. With the Path In Use bits of byte 4, it identifies the storage director attached at the time of this sense collection.

Fmt 9 - Byte 22 and 23 **Symptom Code**

These bytes are a summary of the error condition indicated in the prior 22 bytes.

Format 9 symptom codes all start with the numeral 9, for example 9XXX.

Fmt 9 - Byte 24 **Flags**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Reserved, set to 0
1	Reserved, set to 0
2	Reserved, set to 0
3	Logging Mode
4&5	Logging Control Bits (with 3990 Only)
0 0	Do Not Log
0 1	Log Unconditionally
1 0	Log First Occurrence of This Retry Sequence
1 1	Log First Occurrence of This Retry Sequence If Permanent Error On This Path
6&7	Operator Message Control
0 0	Send No Message to Operator
0 1	Send Message to Operator Unconditionally
1 0	Send Message to Operator On the First Record for This Retry Sequence
1 1	Send Message to Operator on the First Record for This Retry Sequence if Permanent Error on This Path

Fmt 9 - Byte 25 **Action Code**

This byte identifies the Action Code used by 3990. Refer to the 3990 Maintenance Manuals for the definition of this byte.

Fmt 9 - Byte 26 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Dual Frame Storage Control
1	4 Path Device Level Selection
2	Duplex Pair Volume
3	Secondary Device of a Duplex Pair
4	Sense Presented to Relevant Channel
5	Sense Presented to Relevant Device Number
6	Put Record into System Exception Report
7	Alternate Internal Path Will Be Tried

Fmt 9 - Byte 27 **3990 Subsystem Configuration**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	Twenty-four Byte Capability
1	Device Address Valid in Byte 4
2	Track Address Present in Bytes 29 thru 31
3	Reserved, Set to 0
4	Reserved, set to 0
5	Reserved, set to 0
6	Cluster
7	Storage Path

Fmt 9 - Byte 28 **Message Code**

Refer to the 3990 Maintenance Manuals for the definition of the following byte bits.

Bit	Bit Name
0	ERP, Prepare a SIM Message
1-7	Format of the SIM Message

Fmt 9 - Byte 29 **Seek Cylinder Address High**

Bit		Bit Name
0	0	Unused
1	0	Unused
2	0	Unused
3	0	Unused
4		Cylinder 2048
5		Cylinder 1024
6		Cylinder 512
7		Cylinder 256

Fmt 9 - Byte 30 **Seek Cylinder Address Low**

Bit	Bit Name
0	Cylinder 128
1	Cylinder 64
2	Cylinder 32
3	Cylinder 16
4	Cylinder 8
5	Cylinder 4
6	Cylinder 2
7	Cylinder 1

Fmt 9 - Byte 31 **Seek Head Address**

Bit	Bit Name
0	Unused
1	Unused
2	Unused
3	Unused
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

Byte Text Headings

The following abbreviated text form, F^1B^{20} (Format 1 Byte 20), was used to speed eye searches through the text titles.

Unit Check Description, Bytes 0,1,2

Bytes 0, 1, and 2 in all formats are the unit check description. These bytes are generated by the storage director microcode whenever a unit check occurs. They indicate that the operation requested by the operating system cannot be completed. They also indicate the type of error recovery and logging routines required of the operating system by the error.

Unit Check Description, Byte 0

B^0, BIT 0 - COMMAND REJECTED

Bit 0 is set after a channel command to the storage director is rejected. See the appropriate storage control maintenance library for a description of this bit.

B^0, BIT 1 - INTERVENTION REQUIRED

Bit 1 is set after one of the following conditions occurs:

- The addressed device is not physically attached to the system.
- The addressed device is not available because of an initial power-on sequence (purge, motor, start, and warm-up cycles).
- The addressed device is not available because it is in CE mode.
- The addressed device is not available because its Enable/Disable switch is in the Disable position.

B^0, BIT 2 - CHANNEL BUS OUT PARITY CHECK

Bit 2 is set when a channel data parity error is detected by the storage director in data transferred from the channel. See the storage control maintenance library for a description of this bit.

B^0, BIT 3 - EQUIPMENT CHECK

Bit 3 is set by the storage director upon detection of a hardware fault. It requests the operating system to save the first sense data, retry the operation 9 additional times, and log in the error recording data set the first error data with an indication whether the retry was successful (temporary error) or unsuccessful (permanent error).

B^0, BIT 4 - DATA CHECK

Bit 4 is set when a correctable or an uncorrectable data error is detected in information received from the device.

B^0, BIT 5 - OVERRUN

Bit 5 is set after data transfer between the storage director and the channel is not completed in the time permitted by the storage director. See the storage control maintenance library for a description of this bit.

B^0, BIT 6 - UNUSED

B^0, BIT 7 - UNUSED

Unit Check Description, Byte 1

B^1, BIT 0 - PERMANENT ERROR

Bit 0 is set when the storage director error recovery procedures fail to recover from an error, and system retry through that storage director is not desirable

B^1, BIT 1 - INVALID TRACK FORMAT

Bit 1 is set after an attempt is made to write data that exceeds the track capacity. Bit 1 is also set during a read or search operation when the index point is detected in the gap after a count or key field. This bit indicates a programming error or indicates an expected programming condition. See the storage control maintenance library for a description of this bit.

B^1, BIT 2 - END OF CYLINDER

Bit 2 is set after a read multitrack or search multitrack operation continues beyond the last track on the cylinder.

See the storage control maintenance library for a description of this bit.

B^1, BIT 3 - MESSAGE TO OPERATOR

Bit 3 causes the error recovery procedure to print an error message (defined by byte 7) to the system operator. See the storage control maintenance library for further details of this bit.

B^1, BIT 4 - NO RECORD FOUND

Bit 4 is set after the index point at the beginning of the selected logical track is detected twice in the same command chain without an intervening:

- Read operation in the home address (HA) field or in a data field
- Write, sense, or control command

The storage director verifies that the access mechanism is correctly positioned before activating bit 4.

B^1, BIT 5 - FILE PROTECTED

Bit 5 is not used in the 3380-JK See the storage control maintenance library for a description of this bit.

B^1, BIT 6 - WRITE INHIBITED

When bit 6 is active, one of the components on the storage director - controller selection path is set to a read only mode. If the storage director receives a write CCW, it will post a Format 0 Equipment Check with Write Inhibited active. Write Inhibit is set (for data integrity) by the operating system error recovery procedure when it detects a permanent error.

B^1, BIT 7 - IMPRECISE ENDING

Used by storage controls capable of non-synchronous operations. For example, the 3880 with cache memory feature installed uses the bit to indicate an abnormal channel program termination. The active bit indicates that the CCW address is not in sync with the transfer of data from the storage control to the disk. This bit is duplicated in byte 2 bit 5 for compatibility purposes.

Unit Check Description, Byte 2

B^2, BIT 0 - REQUEST WRITE INHIBIT

Bit 0 is set when the Storage Director recognizes that there is a possibility of write operations destroying valid data. It indicates to the operating system ERP that write operations should be inhibited. And, only when attached to 3990, Byte 25 will define the DASD subsystem component to be inhibited.

B^2, BIT 1 - CORRECTABLE (Data Check)

Bit 1 is used only with a Read Multiple Count Key Data command or a Program Control Interrupt fetch. It is set when the data area data check activated in byte 0, bit 4, is determined to be correctable by the storage director.

B^2, BIT 2 - FIRST ERROR LOGGED

Bit 2 is set on the first logged error when an error threshold is exceeded for data, seek, and data checks with offset active.

B^2, BIT 3 - ENVIRONMENTAL DATA PRESENT

Bit 3 indicates that the sense record is for logging information only. This bit is on for data checks and seek checks when the storage director has the device in logging or forced logging mode. The bit is also set when usage data, format 6, is presented by the storage director, after a usage counter overflow.

B^2, BIT 4 - INTENT VIOLATION

Used by storage controls capable of non-synchronous write operations. For example, the 3880 with speed matching buffer feature installed uses the bit to indicate:

- An unsuccessful update write operation was attempted with a record whose size differs from the count area record size parameters.
- An unsuccessful update write operation was attempted to R0 and the data was not 8 bytes in length.
- For examples, see 3880 or 3990 Storage Control Reference Manual.

B^2, BIT 5 - IMPRECISE ENDING

Used by storage controls capable of non-synchronous operations. For example, the 3880 with cache memory feature installed uses the bit to indicate an abnormal channel program termination. The active bit indicates that the CCW address is not in sync with the transfer of data from the storage control to the disk. This bit is duplicated in byte 1 bit 7 for the 3990.

B^2, BIT 6 - WRITE OPERATION IN PROGRESS

Bit 6 indicates to the operating system that a write operation was in progress at the time of the error.

B^2, BIT 7 - 3880 MODEL 23 STORAGE CONTROL

Bit 7 indicates to the operating system that this DASD Subsystem has a 3880 Model 23 for a DASD storage control.

String ID

The data for the String physical ID byte is collected from the selected controller's String ID switches set during installation. The storage director collects the byte with a Sense Controller ID (hex 16) command.

The String physical ID byte is byte 3 of formats 1, 6, 7, 8, and 9. For format 4, byte 14 is the String ID.

Path and Device Physical Identifier, Byte 4

B^4, BITS 0 and 1 - PATH IN USE / CONTROLLER RESPONSE BITS

When connected to 3990, the Path In Use bits, 0 and 1, are set by the storage control indicating the 3990 storage path used. At the 3380-JK Operator panel, the path number will identify the 3380-JK controller for the path.

When connected to 3880-3, these bits, 0 and 1, are the response of a Sense Controller Path, Command 26. They identify the controller connected to the storage director.

Bits 0	1	CONTROLLER RESPONSE
0	0	Controller A1
0	1	Controller A2

EREP will use the bits to complete the identity of the controller with the String ID, when attached to 3880-3. EREP will not use these bits when attached to 3990, it will use Byte 27 bit 6 and 7 to identify the path to the controller. That and the String ID is

used to develop the physical ID to identify the controller path that was used to collect the sense data.

B^4, BIT 2 - String Address Bit

An active bit represents the String Address.1. .It is used by the Storage Director to select the string with the desired controller or device.

B^4, BITS 3 THROUGH 7 - DEVICE ADDRESS BITS

Bits 3 through 7 identify the selected device.

Seek Head and Cylinder Address, Byte 5 and 6

These bytes identify the cylinder and head address last received by the storage director from the operating system for this device. These bytes are used by the storage director to determine the length and direction of the seek instructions sent to the device. At the end of a successful seek operation the device heads should be over the track address indicated in these two bytes.

In Format 6, byte 5 and byte 6 have other meanings. See SENSE-32.

Format and Message, Byte 7

The format-and-message byte is byte 7 of the sense bytes. Byte 7 sense data is generated by the storage director microcode when the storage director receives evidence that a 3380-JK error has occurred.

Bits 0 through 3, the format part of the byte, identify the format of the sense bytes.

Bits 4 through 7, the message part of the byte, identify the kind of evidence the storage director received about the error and indicate what was happening in the subsystem when the error evidence was received.

String Features, Byte 8

F^1,F^7,F^8,F^9B^8 - Bit 0 - DYNAMIC PATH SELECTION FUNCTION INSTALLED IN CONTROLLERS

This status bit indicates that the string's controllers have DPS cards installed.

F^1,F^7,F^8,F^9B^8 - Bit 1 - STRING HAS FOUR PATH CAPABILITY

This status bit indicates that the storage control recognizes this string as having four path capability.

F^1,F^7,F^8,F^9B^8 - Bit 2 -SECOND CDP CARD INSTALLED

A second CDP card is installed to provide 32 device selection capability to this controller.

F^1,F^7,F^8,F^9B^8 - Bit 3 - RESERVED

F^1,F^7,F^8,F^9B^8 - Bit 4 - 3380 MODEL CJ2

F^1,F^7,F^8,F^9B^8 - Bit 5 - ALWAYS ZERO

F^1,F^7,F^8,F^9B^8 - Bit 6 - ALWAYS ZERO

F^1,F^7,F^8,F^9B^8 - Bit 7 - CONTROLLER LOGIC IS 3380-JK

This status bit is provided so that the diagnostics can easily determine the level and/or type of controller logic installed in the machine.

Device Power Status, Byte 10

F^1,F^9B^{10} - Bit 0 - MOTOR START SURGE COMPLETE

Bit 0 indicates that the device sequencer microcode, after detecting the motor contactor closed, has detected AGC active. This indicates that the drive motor has reached a speed where the start surge ac current is reduced almost to run ac current level.

F^1,F^9B^{10} - BIT 1 - UNUSED

F^1,F^9B^{10} - BIT 2 - NO AIR FLOW

Bit 2 is an error condition set if there is no air flow at the exit of the blower assembly. The air flow is sensed by an air driven switch. This switch causes both drives to stop or fail to start, if there is not enough air flow.

F^1,F^9B^{10} - BIT 3 - DEVICE POWER ON SEQUENCE COMPLETE

Bit 3 indicates that the device has completed a normal power-on sequence. The status bit is set after the rezero operation and a warm-up clean cycle.

F^1,F^9B^{10} - BIT 4 - SPINDLE MOTOR STARTED BY DEVICE SEQUENCER

Bit 4 is an indication of the status of the motor run latch. When the bit is on, the motor run latch is on and when the bit is off, the motor run latch is off. When this latch is on, the motor contactor should be picked and the motor running.

F^1,F^9B^{10} - BIT 5 - SPINDLE CONTROL BIT 0

Bit 5 is an indication of the status of the drive motor contactor. When the bit is on, the contactor is picked. When the bit is off, the contactor is not picked.

F^1,F^9B^{10} - BIT 6 - MOTOR BRAKE LATCH

Bit 6 is an indication of the status of the brake latch. When the bit is on, the brake latch is on. When the bit is off, the brake latch is off. When the brake latch is on, the brake relay should be picked, which releases the motor brake.

F^1,F^9B^{10} - BIT 7 - SPINDLE CONTROL BIT 1

Bit 7 is an indication of the status of the motor sequence assembly relay. This relay is also referred to as the soft-start relay. When the bit is off, the relay is not picked. When the bit is on, the relay is picked.

Device Check-2 Status, Byte 11

For Format 1 this byte will have any bit 0 - 4, or 6, or 7. Bit 5 may or may not be on.

For Format 9 this byte will have bits 0 - 4, or 6 or 7, off. Bit 5 may or may not be on. If bit 5 is off, the message in byte 7 will be 7, A, or E.

F^1,F^9B^{11} - BIT 0 - DEVICE SEQUENCER CHECK

Bit 0 is a hardware check. A device sequencer check indicates that one of the error sensors in the device sequencer portion of the Sequencer/Servo/RPS card recognizes an error condition. The sequencer performs the major control function of each actuator and therefore has

9 error checkers to guarantee correct operation. See Checkpoint log, byte 15 on SENSE-66.

F^1,F^9B^{11} - BIT 1 - SERVO CONTROL CHECK

Bit 1 is a hardware check. The checking circuit monitors internal registers in the servo control portion of the Sequencer/Servo/RPS card for correct parity.

F^1,F^9B^{11} - BIT 2 - ROTATIONAL POSITION SENSING (RPS) CHECK

Bit 2 check is a hardware check. The checking circuit monitors those conditions that affect the sensing of the rotational position of the disk with respect to index. The checking circuit also tests for correct parity of the data loaded from the '+ CDP Data Bus Power' bus into the target register.

F^1,F^9B^{11} - BIT 3 - CHECKPOINT CHECK

The checkpoint log register (Byte 15) is loaded at significant points in the execution of sequencer code. A check point log register error occurs when either bad parity occurs in the checkpoint register or when the sequencer forces the check to occur. See Checkpoint log, byte 15 on SENSE-66.

F^1,F^9B^{11} - BIT 4 - HDA CABLE SWAP CHECK

When Bit 4 is active it indicates that cables to the HDA have been exchanged improperly.

F^1,F^9B^{11} - BIT 5 - READ/WRITE CHECK

Bit 5 is an indication that an error latch is on in one of the read/write status registers.

F^1,F^9B^{11} - BIT 6 - POWER CARD CHECK

Bit 6 is an indication of a Power Card Check, which is developed because of No Air Flow to the HDAs or Sequencer Write Bus Parity Check. No Air Flow should also be indicated in format 1, byte 10, bit 2.

F^1,F^9B^{11} - BIT 7 - FUNNEL PARITY CHECK

Data going to the storage director from a device is gated through a funnel in the port card before it is put onto the CDP Bus In. The parity of the data gated into the funnel is checked and a Funnel Parity Check results if the parity is even.

Servo Status - 0, Bytes 12 and 13

F^1B^{12} - BIT 0 - NOT USED

This bit is always 0.

F^1B^{12} - BIT 1 - SELF INITIATED BUSY

Bit 1 active (1) means that the DCP is in the process of resetting internal registers. This bit is usually at 0.

F^1B^{12} - BIT 2 - INITIAL MICROCODE LOAD IN PROGRESS

Bit 2 active (1) means that the DCP microcode load is in the process of being loaded into the DCP RAM. The DCP microcode is stored in the EPROM's located on the PES card. The DCP microcode is loaded into RAM whenever device power-on-reset, Reset Servo Check command, or a Processor Reset command occurs.

F^1B^{12} - BIT 3 - INITIAL MICROCODE LOAD COMPLETE

Bit 3 active (1) means the DCP microcode load has successfully been loaded into the DCP RAM, the DCP self-checks have been completed without error, and the DCP is ready for servo operation.

F^1B^{12} - BIT 4 - HALF TRACK

Bit 4 is active (1) when the servo head is within one half of the track width of the target cylinder, but is not yet track following. After half track has been reached, the servo will then settle on track center. This bit will then go inactive (0), and the track following bit (byte 13, bit 5) will go active (1).

F1B12 - BIT 5 - SERVO WRITE INHIBIT

Bit 5 active (1) means that it is unsafe to do a write operation. Bit 5 will be active for all servo error conditions, and during DCP IML, offset, rezero, and locate (seek) operations.

F1B12 - BIT 6 - INDEX

Bit 6 active (1) means that index occurred during the last servo sample.

F1B12 - BIT 7 - SCALE 2 MODE

Bit 7 active (1) means that the DCP is in the fast (2x mode) sampling mode. While the DCP is moving the actuator, (seeking. for example), the servo error signal, PES P or PES Q, is read and digitized every 112 microseconds (1x mode). When the DCP is in track following mode, the error signal is read and digitized every 56 microseconds, (2x mode).

F1B13 - BIT 0 - CLOCK

The DCP toggles this bit each time it reads the Command Out register, and writes the Servo Status registers. The DCP does these two operations every 112 microseconds. Therefore, the clock bit will change states every 112 microseconds, and may be the only bit that changes between Servo Status updates.

F1B13 - BIT 1 - DCP BUSY

Bit 1 active (1) means that the DCP was executing a command that caused the DCP to change state. Servo commands such as Locate, Rezero, Offset, will cause bit 1 to go active. Commands such as Select Status, or certain diagnostic commands do not cause busy. Busy is also active during IML. When busy is active, the DCP cannot accept another command. If the B-sequencer sends a command to the DCP while busy is active, a Servo Inhibit error will occur.

F1B13 - BIT 2 - DCP ERROR

Bit 2 active (1) means that a DCP error has occurred, and that Servo Status 2 contains an error code that describes the error. Two types of errors will cause this bit to go active: DCP Check-2, and certain Servo Inhibit conditions.

F1B13 - BIT 3 - DCP CHECK-2

Bit 3 active (1) means that an error internal to the DCP or its busses has occurred. Servo operation is impossible and a servo reset is required.

F1B13 - BIT 4 - SERVO INHIBIT

Bit 4 active (1) means that the DCP has inhibited the servo power amplifier preventing any actuator movement. This is a normal condition following a DCP power-on-reset, or if the B-sequencer has issued a servo inhibit command. DCP error bit 2 will not be active for these conditions. Errors external to the DCP can cause a Servo Inhibit, and DCP error bit 2 will be active for these conditions.

F1B13 - BIT 5 - TRACK FOLLOWING

Bit 5 active (1) means that the servo head has settled on the center of the target track, and is servoing on track center. When track following is active, Half Track, (byte 12,bit 4), will be inactive. If there are no error conditions in the DCP, Servo Write Inhibit, (byte 12, bit 5), will be inactive.

F1B13 - BIT 6 - OFFSET

Bit 6 active (1) means that the servo head has reached the desired offset position. Servo Write Inhibit, (byte 12, bit 5), will also go active.

F1B13 - BIT 7 - SERVO TO VOLTAGE

Bit 7 active (1) means that the servo is responding to the requested voice coil voltage or current. This bit may become active before the coil voltage or current has reached its requested value.

Servo Status-1, Bytes 14 and 16

These bytes indicate the version level of the Servo Card Microcode.

Checkpoint Log Byte 15

The checkpoint log is a register in the device sequencer/servo/RPS card. Normally, without any device errors, the device sequencer maintains the checkpoint log. The sequencer changes the value in (or updates) the checkpoint log at specific points in the microcode to record the occurrence of events. This value can indicate either status or error conditions.

The value in the checkpoint log will indicate an error if Checkpoint Check (sense byte 11, bit 3), is active in the device check 2 status byte. Checkpoint check is set by device sequencer microcode.

During servomechanism operations, the device sequencer controls and monitors the operation. If the device sequencer microcode detects an error in the operation, the microcode sets a value in the checkpoint log to identify the error. Depending on the severity of the error, the microcode may branch to a recovery or retry routine, or an error routine to stop operations before damage to data or hardware.

The checkpoint log byte is collected from the device sequencer/servo/RPS card in the selected device in response to the Sense Checkpoint Log (hex 57) command, which comes from the storage director. The command and the response pass through the controller on the feed through path. The checkpoint log byte is contained in EREP format 1, byte 15 and format 9, byte 15.

The text next to each checkpoint value is a simple description of the checkpoint, not a name; therefore it may not match the name in the microcode listing.

Problems within the motor, Motor Start Assembly (MSA), and brake relay area.: The motor control relay, the motor sequence assembly relay, and the brake relay are controlled by the cards in both devices within a drive. If a problem is reported in this area against one device, the failure could be in the opposite device. This should be kept in mind when doing problem determination and running diagnostics.

Checkpoint Log Value Meanings

'XX' indicates checkpoint value is not an error, status only.

'XX'^{2} indicates the number of alternate meanings depending on the operation (in this case: 2)

'XX'-E indicates an error condition. Checkpoint Check, Format 1, Byte 11, Bit 3 = 1.

'XX'^{2}-E indicates an error condition and the number of alternate meanings depending on the operation (in this case: 2)

'XX'-D indicates that this checkpoint is only from a Diagnostic and is not an error.

'XX'-DE indicates that this checkpoint is only from a Diagnostic and is an error.

NOTE; Checkpoints not labeled 'diagnostic only' may occur during diagnostic tests. Checkpoints labeled 'diagnostic only' will not occur during normal operation.

'00'	Hardware Reset of the Checkpoint register.
'01'	Starting purge.

'02'	Purge routine complete.
'03'	Bypassing 4-6 minute perpetual seek timeout test, command active.
'07'	Rearming Safe timer, either in idle or going to idle.
'09'	Check Reset ('43') command complete, no errors.
'0C'	Starting the DCP IML.
'0D'	DCP IML complete without errors.
'10'-E	Index failure during idle. (see error description on ECD-27)
'13'-E	Cell pulse failure during idle routine. (see error description on ECD-29)
'15'-E.	DCP Servo Write Inhibit bit detected inactive during rezero. (see error description on ECD-30)
'16'-E	DCP Servo Write Inhibit or Write Inhibit detected active at the end of the rezero. (see error description on ECD-31)
'17'	Write Inhibit signal is active during a Read/Write operation. (does not set checkpoint check)
'17'-E	Servo Inhibit during a Read/Write operation.
'18'-E	DCP Half Track bit active at the end of the rezero. (see error description on ECD-33)
'19'	Reset command received during the Data Check Recovery.
'1A'-E	DCP found Busy with Not Write Inhibit. (see error description on ECD-34)
'1D'	No Guard Band detected during a Sense Guard Band ('79') command.
'1E'	GBOD detected during a Sense Guard Band ('79') command.
'1F'	GBID detected during a Sense Guard Band ('79') command.
'20'	Power on routine started.
'21'	Set for start and error free ending of the Park and relay tests (Motor, Brake and Soft Start relays) at the beginning of power on.
'22'	Release brake and pick Soft Start relay during power on.
'23'	Pick Soft Start And Motor Run Relays during power on.
'24'	Drop Soft Start relay, keep motor relay picked during power on.
'25'	Decompress, hold Park, almost full speed during power on.
'26'	Check reset complete, no errors during power on.
'27'.	Checking to see if the COMMAND signal from Port card is stuck active.
'28'2	At full speed, reset park during power on.
'29'	Sweep in progress during power on.
'2A'-DE	Checkpoint Freeze detected not active during diagnostic command. ('8B') (see error description on ECD-35)
'2B'	Sweep complete, no errors in warm-up period of power on.
'2C'	Second sweep in progress.
'2D'	Received Power On Retry command.
'2E'	Drive motor switch turned off then on.
'2F'-E	Motor turning without relay being picked during POR. (see error description on ECD-36)
'30'	Power off sequence started with motor running.

'31'-E The actuator moved too far during the safe. (see error description on ECD-37)

'32' Motor slowing during power off.

'33' Brake applied during power off.

'34'-E Either a DCP detected error or the check-2 reset command failed during the safe routine. (see error description on ECD-39)

'39'-E DCP in an error state or wrong command issued during safe routine. (see error description on ECD-40)

'3A'-E Drive motor slowing down or checks active. (see error description on ECD-42)

'3B'-E The DCP either did not take or it did not complete the safe routine. (see error description on ECD-44)

'3F'-E Motor relay stuck active during either a POR or a power off. (see error description on ECD-45)

'41'-E DCP Track Following bit active when not expected during rezero routine. (see error description on ECD-47)

'44'-E DCP detected failure during rezero routine. (see error description on ECD-48)

'45'-E DCP Servo Check 2 bit active during rezero. (see error description on ECD-49)

'46'-E DCP Busy bit detected inactive during rezero. (see error description on ECD-50)

'47'-E Servo Check 2 active prior to issuing rezero command. (see error description on ECD-51)

'48'-E AGC lost during rezero. (see error description on ECD-52)

'49'-E Track Following not acquired at the end of rezero. (see error description on ECD-53)

'4C'-E DCP detected error or it failed to start the rezero command. (see error description on ECD-55)

'4D' EC level from command '8D'x.

'4D'-E DCP Half Track bit not active when expected during rezero routine. (see error description on ECD-56)

'4E' EC Level from command '8D'x.

'4F'-E DCP Busy bit active before issuing rezero command. (see error description on ECD-57)

'50'-E Seek routine took to long. (see error description on ECD-58)

'51' AGC signal detected active during seek.

'52'-E Guard band detected during seek. (see error description on ECD-59)

'53'-E DCP Busy bit not active at the beginning of seek command. (see error description on ECD-61)

'54'[2] Track Following before first settling delay during seek.

'54'[2]-E DCP Error bit detected active during seek. (see error description on ECD-62)

'55'[3] Track Following at the end of first settling delay during seek.

'55'[3]-E DCP detected failure during seek. (see error description on ECD-63)

'55'[3]-D Amount loaded into the Checkpoint register to test the register.

'56'[2] Track Following at the end of second settling delay during seek.

'56'²-E Invalid command in DCP command register for seek routine. (see error description on ECD-64)

'57'² Track Following at the end of third settling delay during seek.

'57'²-E AGC signal inactive during seek. (see error description on ECD-65)

'58'² Track Following at the end of fourth settling delay during seek.

'58'²-E Not track following after forth settling maximum delay during seek routine. (see error description on ECD-66)

'59'-E Both DCP Track Following and DCP Offset bits inactive at beginning of seek routine. (see error description on ECD-67)

'5A'-E DCP Busy bit active either at the beginning or end of the seek. (see error description on ECD-68)

'5B'-E DCP fails to accept seek command or DCP hang condition detected. (see error description on ECD-70)

'5C'-E DCP Busy bit goes inactive during seek. (see error description on ECD-71)

'5D'-E DCP Half Track bit in wrong state during seek. (see error description on ECD-72)

'5E'-E DCP Track Following bit active too soon during seek. (see error description on ECD-73)

'5F'-E Write Inhibit signal or DCP Servo Write Inhibit bit in wrong state during seek routine. (see error description on ECD-74)

'60'-E DCP Offset bit in wrong state during offset. (see error description on ECD-76)

'61' AGC signal detected active during offset.

'62'-E Invalid command in DCP command register for offset. (see error description on ECD-77)

'63'-E DCP Busy bit active before issuing offset command. (see error description on ECD-78)

'64'-E DCP Error bit detected active during offset. (see error description on ECD-79)

'65'-E DCP detected failure during offset. (see error description on ECD-80)

'66'-E DCP fails to accept offset command or DCP hang condition detected. (see error description on ECD-81)

'67'-E DCP Busy bit not active at the beginning of offset command. (see error description on ECD-83)

'68'-E AGC signal inactive during offset. (see error description on ECD-84)

'6A'-E DCP Track following bit in wrong state during offset routine. (see error description on ECD-85)

'6B'-E Offset routine took to long. (see error description on ECD-86)

'6C'-E Write Inhibit signal or DCP Servo Write Inhibit bit in wrong state during offset routine. (see error description on ECD-87)

'6D'-E DCP Track Following and DCP Offset bits both inactive at beginning of offset routine. (see error description on ECD-88)

'6E'-E Write Inhibit signal or DCP Servo Write Inhibit bit active at the end of a zero offset routine. (see error description on ECD-90)

'6F'-E DCP Busy bit active at the end of the offset. (see error description on ECD-91)

'70' Search routine completed, no errors.

'71' Sector search in progress

'72' Targeted sector detected during search.

'73' 'Go around' search started after first Record Ready Interrupt.

'74'-E DCP Error bit detected active during a 'go around' search. (see error description on ECD-92)

'75'-E DCP Servo Check 2 bit detected active during a 'go around' search. (see error description on ECD-94)

'76'-E DCP Busy bit active before issuing search command. (see error description on ECD-95)

'77'-E Record Ready Interrupt is active too long during search routine. (see error description on ECD-96)

'78'-E AGC signal detected inactive during search. (see error description on ECD-97)

'79'-E RPS failed to lock detected during search. (see error description on ECD-98)

'7A'-E RPS Check active during search. (see error description on ECD-99)

'7B'-E Index/Record Ready Interrupt check during search routine. (see error description on ECD-101)

'7C'-E Time between Record Ready Interrupts too short during a search. (see error description on ECD-102)

'7D'-E Time between Record Ready Interrupts to long during a search. (see error description on ECD-103)

'7E' Open Write Ready Window command ('42'x) received during Data Check Recovery.

'7F'-E Servo Check 2 bit active before issuing search command. (see error description on ECD-104)

'80'-E Received a command that does not match the HDA model (Command active - Busy inactive). (see error description on ECD-105)

'82'-E Read/Write Mode active during SAFE. (see error description on ECD-107)

'83'-E Invalid warm-up command.

'84'-E Either an invalid command or parameter was received. (see error description on ECD-108)

'85'-E Received a command that does not match the HDA model (Command active - Busy active). (see error description on ECD-109)

'86'-E Lost Track Following during Data Check Recovery. (see error description on ECD-111)

'87'-E Check-2 reset command ('43'x) fails to reset busy. (see error description on ECD-112)

'88'-E Invalid or illegal command received with the device busy. (see error description on ECD-113)

'89' Set HAR command received during safe.

'8A'-E DCP Sample Interrupt signal out of specification during idle. (see error description on ECD-114)

'8B'-E DCP Sample Interrupt signal not changing states during idle routine. (see error description on ECD-115)

'8C' Safe routine complete, no errors.

'8D'-E Sequencer failed to receive required data from the CDP. (see error description on ECD-116)

'8E'-E Received a command that does not match the HDA model (Command signal inactive). (see error description on ECD-117)

'8F'-E Both guard bands detected, actuator appears to be oscillating. (see error description on ECD-119)

'90' Set HAR command, head parameter transfer complete. Ready for Read/Write operations. change.

'92'-E Command Gate stuck active (see error description on ECD-120)

'A0'-D Error during crash test. (Any failure within the device during this routine will set this Checkpoint)

'A1'-E No air pressure detected before motor start. (see error description on ECD-121)

'A2'-E Motor relay not active during power on or a search routine. (see error description on ECD-122)

'A3'-E. No air pressure detected during power on routine. (see error description on ECD-124)

'A4'-E Motor Switch off after the motor is started during power on routine. (see error description on ECD-125)

'A5'-E Drive Motor Switch momentarily off during search or idle routine. (see error description on ECD-126)

'A6'-E Motor relay active at the beginning of motor start routine. (see error description on ECD-127)

'A7'-E DCP detected error doing a decompress of the motor start. (see error description on ECD-129)

'A8'-E AGC not active with, or motor not running after 20 seconds of motor power on. (see error description on ECD-130)

'A9'-E DCP Command bit active when not expected during compress routine. (see error description on ECD-132)

'AA'-E DCP detected error or timeout during a compress routine. (see error description on ECD-133)

'AB'[2]-D Normal completion code for Diagnostic Command '89'x (Register Wrap Test).

'AC'-E DCP detected error or timeout during a decompress. (see error description on ECD-135)

'AD'-E DCP detected error or hang during the sticky crash stop recovery. (see error description on ECD-136)

'AE'-E DCP timeout during the sticky crash stop recovery.

'AF' Sticky crash stop recovery routine started.

'B0'-E DCP detected error during a seek of crash stop recovery.

'B1'-E DCP detected error after park prior to starting the motor. (see error description on ECD-140)

'B2'-E Motor or Soft Start Thermal or Belt Guard Switch open. (see error description on ECD-141)

'B3'-E No Air pressure detected. (see error description on ECD-143)

'B4'-E Motor Switch off at beginning of power on or during idle. (see error description on ECD-144)

'B5'-E AGC still active with motor off. (see error description on ECD-145)

'B6'-E Drive motor slowing down during idle. (see error description on ECD-146)

'B7'-E DCP detected error or servo failure during power on. (see error description on ECD-148)

'B8'-E Brake test failed at the beginning of power on. (see error description on ECD-150)

'B9'-E Soft Start Relay active when not expected. (see error description on ECD-151)

'BA'-E Soft Start Relay not active at beginning of motor start. (see error description on ECD-152)

'BB'-E Soft Start relay active after at beginning of motor start. (see error description on ECD-154)

'BC'-E DCP detected external error after any sequencer to DCP command. (see error description on ECD-155)

'BD'-E DCP detected internal error after any sequencer to DCP command. (see error description on ECD-156)

'BE'-E DCP hang after any servo command. (see error description on ECD-158)

'BF'-E DCP Command bit active when not expected during decompress. (see error description on ECD-159)

'C0'-E Servo Inhibit active during Data Check Recovery. (see error description on ECD-160)

'C1'-E DCP IML failure. (see error description on ECD-162)

'C2'-E DCP BAT failure. (see error description on ECD-164)

'C3'-E AGC not active 18 seconds after the motor was started. (see error description on ECD-165)

'C4'-E DCP detected failure during the handling of Sweep commands. (see error description on ECD-166)

'C5'-E External Timer from other device not running. (see error description on ECD-168)

'C6'-E Motor Run Relay not active after Soft Start Relay dropped. (see error description on ECD-169)

'C7'-E Sector Compare not found during Data Check Recovery. (see error description on ECD-170)

'C8'-E Offset command not saved prior to Data Check Recovery. (see error description on ECD-171)

'C9'-E Sector Compare stuck on during Data Check Recovery. (see error description on ECD-172)

'CA'-E DCP Busy Detected during Data Check Recovery. (see error description on ECD-174)

'CB'-E RPS Lock inactive during Data Check Recovery. (see error description on ECD-175)

'CC'-E DCP detected checksum error during DCP IML or DCP BAT. (see error description on ECD-176)

'CD'-E Guard Band detected at cylinder 0 during a minus cylinder seek command. (see error description on ECD-178)

'CE'-E Abnormal Termination of Data Check Recovery. (see error description on ECD-179)

'CF'-E GBOD not found after a seek to a minus cylinder. (see error description on ECD-180)

'D1'-E Servo failure during sweep or heat up routines of power on. (see error description on ECD-181)

'D2'-E DCP timeout doing a compress during the motor start routine. (see error description on ECD-183)

'D3'-E DCP timeout failure during sweep. (see error description on ECD-184)

'D4'-E Park failed before starting motor during power on. (see error description on ECD-185)

'D5'-E DCP detected error at the beginning of motor start. (see error description on ECD-187)

'D6'-E Motor sensed off, but still turning at more than 3440 RPM. (see error description on ECD-189)

'D7'-E Unexpected Offset active during Data Check Recovery. (see error description on ECD-190)

'D8'-E Index not found during Data Check Recovery. (see error description on ECD-192)

'D9'-E Device Selected dropped during Data Check Recovery. (see error description on ECD-193)

'DA'-E DCP Error Detected during Data Check Recovery. (see error description on ECD-194)

'DB'-E Unexpected Sector Compare during Data Check Recovery. (see error description on ECD-195)

'DC'-E DCP Check Detected during Data Check Recovery. (see error description on ECD-196)

'DD'-E Command Gate missing during Data Check Recovery. (see error description on ECD-197)

'DF'-E DCP timeout failure during crash stop recovery. (see error description on ECD-198)

'E0'-DE Soft Start Relay active at the beginning of Diagnostic Routine '99'. (see error description on ECD-199)

'E1'2-DE Motor Run Relay active at the beginning of Diagnostic Routine '99'. (see error description on ECD-201)

'E2'-DE Motor Run and Soft Start Relays active at the beginning of Diagnostic Routine '99'. (see error description on ECD-202)

'E3'-DE Drive Motor Switch sensed on at the beginning of Diagnostic Routine '99'. (see error description on ECD-203)

'E4'-DE Soft Start Relay inactive after pick during Diagnostic Routine '99'. (see error description on ECD-205)

'E5'-DE Soft Start Relay active after dropping it during Diagnostic Routine '99'. (see error description on ECD-206)

'E6'-DE Motor relay active after picking brake relay during Diagnostic Routine '99'. (see error description on ECD-207)

'E7'-DE Motor relay inactive after pick during Diagnostic Routine '99'. (see error description on ECD-208)

'E8'-DE Motor relay active after drop during brake relay pick test of Diagnostic Routine '99'. (see error description on ECD-209)

'E9'-DE Motor relay active with the brake applied during Diagnostic Routine '99'. (see error description on ECD-210)

'EA'-DE Motor relay active after drop during motor test of during Diagnostic Routine '99'. (see error description on ECD-212)

'EB'-DE Soft Start Relay active at the end of Diagnostic Routine '99'. (see error description on ECD-213)

'EC'-DE Motor Run Relay active at the end of Diagnostic Routine '99'. (see error description on ECD-214)

'ED'-DE Motor Run and Soft Start Relays active after dropping during Diagnostic Routine '99'. (see error description on ECD-216)

'EE'-DE Drive Motor Switch sensed on at the end of Diagnostic Routine '99'. (see error description on ECD-217)

'EF'-DE Sequencer failed to detect bad parity during diagnostic command '84'. (see error description on ECD-218)

'F1'-E GBOD not detected after park during power off. (see error description on ECD-219)

'F2'-E Drive motor slowing down during sweep. (see error description on ECD-220)

'F3'-E AGC signal stuck active, motor not turning during POR. (see error description on ECD-221)

'F4'-E Motor slowing, AGC active, motor relay not picked during POR. (see error description on ECD-223)

'F5'-E Park failed in SAM power on.

'F6'-E No air pressure detected during idle. (see error description on ECD-225)

'F8'-E Sector compare not detected during a sector search. (see error description on ECD-226)

'F9'-E Unexpected Read/Write mode active. (see error description on ECD-227)

'FC'-E Disable Switch detected active during any search command. (see error description on ECD-228)

'FF'-D Successful completion of Checkpoint Register test. Even though Checkpoint Check is active, this is not an error, since Checkpoint Check active is expected. Diagnostic routine 81, test 05 will run this test.

Device Status 1, Byte 19

$F^{1},F^{8},F^{9}B^{19}$ - BIT 0 - PADDING IN PROGRESS

Bit 0 is a status bit indicating that the device read/write path is performing a padding operation.

$F^{1},F^{8},F^{9}B^{19}$ - Bit 1 - DEVICE MODEL

Bit 1 inactive identifies a Model J HDA.

Bit 1 active identifies a Model K HDA.

$F^{1},F^{8},F^{9}B^{19}$ - BIT 2 - ALWAYS ZERO

$F^{1},F^{8},F^{9}B^{19}$ - BIT 3 - DEVICE ERROR

Bit 3 is set by any one of of four status conditions.

Servo Inhibit

If byte 20 bit 1 is active, then this bit indicates Servo Inhibit. Servo Digital Control Processor (DCP) detects a servo system failure.

Seek Incomplete

If byte 20 bit 7 is active this bit active indicates Seek Incomplete. If Byte 20 bit 7 is active without byte 20 bit 1, a Seek Incomplete condition exists, yet it indicates specifically that the device sequencer timed out waiting for the Servo DCP to complete a seek operation.

Device Check 2 Condition

If any byte 11 bit is active, then this bit indicates an active Check 2 condition.

Set Sector Incomplete

If none of the above bits are active the device microcode has detected a Set Sector Incomplete condition.

F^1,F^8,F^9B^{19} - BIT 4 - ONLINE

Bit 4 is active when the drive power-on sequence is successfully completed and the device is ready to resume normal operations.

F^1,F^8,F^9B^{19} - BIT 5 - HDA ATTENTION

Bit 5 is set when the device sequencer starts a head and disk assembly (HDA) attention interrupt at the completion of the device power-on sequence.

F^1,F^8,F^9B^{19} - BIT 6 - DEVICE BUSY

Bit 6 is set by the device sequencer during any of the following operations:

Seek
Offset
Rezero
Pad in Progress
Search sector
Power On or Power Off

F^1,F^8,F^9B^{19} - BIT 7 - LOCATE INTERRUPT

Bit 7 is set to indicate interrupt for the following operations:

Sector search in progress
Seek/rezero complete
Seek incomplete
Set Sector incomplete
Padding complete

Device Status 2, Byte 20

F^1,F^8,F^9B^{20} - BIT 0 - DEVICE LOGIC DISABLED

Bit 0 is active when the Logic Enable/Disable switch (on the SAM Panel) on the other device of this drive is in the Disable position.

F^1,F^8,F^9B^{20} - BIT 1 - SERVO INHIBIT

Bit 1 is set when the servo system is not track following and loses all orientation.

F^1,F^8,F^9B^{20} - BIT 2 - OFFSET ACTIVE

Bit 2 indicates that the servo circuits are being operated with offset active. The offset process modifies the track following process by moving the heads slightly from the center of the track in the current cylinder.

F^1,F^8,F^9B^{20} - BIT 3 - DRIVE MOTOR SWITCH OFF

Bit 3 indicates that the Drive Motor switch for this drive is in the Off position.

F^1,F^8,F^9B^{20} - BIT 4 - ACCESS MECHANISM LOGIC EXCHANGED

Bit 4 indicates that the cables to the access mechanisms are exchanged between the two devices of this drive.

F^1,F^8,F^9B^{20} - BIT 5 - DEVICE SWITCH SET TO DISABLE

Bit 5 indicates that the operator panel Enable/Disable switch is in the Disable position.

F^1,F^8,F^9,F^9B^{20} - BIT 6 - DEVICE LOGIC VOLTAGE STATUS

Bit 6 indicates that an under-voltage condition has occurred on one of the device logic voltages of +5v, -5v, +15v, or -15v. It is a status condition because a device logic under-voltage condition cannot by itself initiate an equipment check. This bit is gated by device check 2 or device check 1 active.

F^1,F^8,F^9B^{20} - BIT 7 - SEEK INCOMPLETE

Bit 7 indicates that the device sequencer timed out waiting for the Servo DCP to complete a seek operation. It will also set Seek Incomplete if the DCP detects an error during the Seek operation.

Record ID, Bytes 8 through 12

F^4 - BYTES 8 THROUGH 12 - RECORD IDENTIFICATION

Sense bytes 8 through 12 contain the record identification obtained from the count area of the record in which the error occurs.

These bytes contain the data read without correction, therefore, if the message in byte 7 is:

0 (data check in the HA area) or,

1 (data check in the count area) or,

4 (no sync byte found in the HA area) or,

5 (no sync byte found in the count area)

the address data is unreliable. Use bytes 5 and 6 for track address.

Sense byte 12, the record number from the count area, is set to zero if the error occurs in the home address area (Messages 0 and 4). This byte is unreliable after a space count.

Sector Number, Byte 13

F^4 - BYTE 13 - SECTOR NUMBER

Byte 13 contains the sector number of the record in error. It is used by the storage director to reorient to the beginning of the record, for retry, when a data check occurs in a key or data area.

These bytes contain the data read without correction, therefore, if the message is 0 (error in the HA area) or if the message is 1 (error in the count area) the address data is unreliable.

Head Offset Value, Byte 15

F^4 - B^{15} BITS 0 THRU 3 - OFFSET

Bits 0 thru 3 reflect the amount of head offset used to recover from an initially uncorrectable data check. The amount of head offset displacement increases with each level of offset.

The hex value of Bits 0 thru 3 indicate the offset.

- '0' No offset applied
- '1' 1st increment of offset
- '2' 2nd increment of offset
- '3' 3rd increment of offset
- '4' 4th increment of offset
- '5' 5th increment of offset
- '6-F. Not Used

F^4 - B^{15} BIT 4 - UNUSED

F^4 - B^{15} BIT 5 - EXTRA SUBSYSTEM RECOVERY OPERATION

F^4 - B^{15} BIT 6 - UNUSED

F^4 - B^{15} BIT 7 - FORWARD DIRECTION

This bit active indicates that the offset was applied in a forward (increasing) direction.

ECC Status, Bytes 16 and 17, Format 4

F^4 - B^{16} BIT 0 - 'SUB-BLOCK' CHECK BYTE ERROR (ICKDSF)

While this bit and the next, 'Block' Check Byte Error (ICKDSF), contain status information for all Read operations, they provide information specifically for the ICKDSF program analysis. They do not provide any service information to the CE.

F^4 - B^{16} BIT 1 - 'BLOCK' CHECK BYTE ERROR (ICKDSF)

While this bit and bit 0, 'Sub-Block' Check Byte Error (ICKDSF), contain status information for all Read operations, they provide information specifically for the ICKDSF program analysis. They do not provide any service information to the CE.

F^4 - B^{16} BIT 2 - UNCORRECTABLE

The ECC logic determined, with the Sub-Block and Block Check Bytes, that the record read was uncorrectable with the ECC pattern data.

F^4 - B^{16} BIT 3 - TWO OR MORE SECOND LEVEL ERRORS IN ONE PHASE

The ECC logic determined that two or more second level errors in one phase occurred. This is an indication of the quantity of errors detected within the record.

F^4 - B^{16} BIT 4 - 128 FIRST-LEVEL ERRORS ALLOWED.

This bit active indicates the number of first-level errors that the ECC process can manage is 128. It is a measure of the storage capacity of the ECC function. When the bit is off, it indicates that the process can manage only 64.

F^4 - B^{16} BITS 5 THROUGH 7- SECOND LEVEL CORRECTABLE ERROR COUNT

These three bits indicate the number of second level errors in the record. This count, up to seven, along with the first level count is intended for use primarily by IBM Engineering in analyzing uncorrectable data situations. IBM RAS may be able to find some use for both the error counts to monitor a device's performance degradation.

F^4 - B^{17} BITS 0 THROUGH 7 - FIRST LEVEL CORRECTABLE ERROR COUNT

This byte indicates the number of first level errors in the record. This count, up to 128 (only 128 are used), along with the second level count is intended for use primarily by IBM Engineering in analyzing uncorrectable data situations. IBM RAS may be able to find some use for both the error counts to monitor a device's performance degradation.

Storage Control Data Transfer Error Bits, Byte 10

The information in the Storage Control Data Transfer Bits byte is extracted from different storage control registers during the collection of the sense data.

F^7,F^8B^{10} - BIT 0 - CONNECTION CHECK ALERT

Bit 0 indicates a connection check alert. This bit can be on for format 7, but is always off for format 8.

F^7,F^8B^{10} - BIT 1 - TAG-IN CHECK

Bit 1 is set when the storage director detects an invalid tag-in sequence.

F^7,F^8B^{10} - BIT 2 - SYNC-IN CHECK

Bit 2 is set when the storage director detects too many sync in tags during data transfer operations.

F^7,F^8B^{10} - BIT 3 - DDC BUS IN PARITY CHECK

Bit 3 is set if the storage director detects a bus in parity error.

F^7,F^8B^{10} - BIT 4 - DDC TAG-IN NULL DISCONNECT

Bit 4 is set when tag in is in a Null Disconnect condition when the storage director detects an error.

F^7,F^8B^{10} - BIT 5 - DDC TAG-IN SYNC IN or VALID

Bit 5 is set when tag in is in a sync in or valid condition when the storage director detects an error.

F^7,F^8B^{10} - BIT 6 - DDC TAG-IN SELECTED NULL

Bit 6 is set when tag in is in a selected null condition when the storage director detects an error.

F^7,F^8B^{10} - BIT 7 - DDC TAG-IN END OPERATION

Bit 7 is set when tag in is in an end-operation condition when the storage director detects an error.

Connection Check Alert and Power Status, Byte 11

F^7B^{11} - BIT 0 - CONTROLLER 0 CCA

Bit 0 is active if any check 1 error is set in the connection check shift register of the controller addressed as 0.

F^7B^{11} - BIT 1 - CONTROLLER 1 CCA

Bit 1 is active if any check 1 error is set in the connection check shift register of the controller addressed as 1.

F^7B^{11} - BIT 2 - CONTROLLER 0 DPS UNCONDITIONAL RESERVE RELEASE

Bit 2 is active to indicate that the companion controller of this string received an Unconditional Reserve Release command. This status message is not an error indication, but a logged indication of the dynamic path selection (DPS) activity.

F^7B^{11} - BIT 3 - CONTROLLER 1 DPS UNCONDITIONAL RESERVE RELEASE

Bit 3 is active to indicate that the companion controller of this string received an Unconditional Reserve Release command. This status message is not an error indication, but a logged indication of the DPS activity.

F^7B^{11} - BITS 4 - FOR 3380-JK, ZERO

This bit refers to the string addressed as 0. If string 0 is a 3380-JK, this bit is always zero. If it is a 3380 model AA4, AD4, or AE4, this bit means Power On. If the string addressed as 0 is a 3380 model AA4, AD4, or AE4, this bit would be a one, while bit 6 would be zero.

F^7B^{11} - BITS 5 - FOR 3380-JK, ZERO

This bit refers to the string addressed as 1. If string 1 is a 3380-JK, this bit is always zero. If the string addressed 1 is a 3380 model AA4, AD4, or AE4, this bit means Power On. If the string addressed as 1 is a 3380 model AA4, AD4, or AE4, this bit would be a one while bit 7 would be zero.

F^7B^{11} - BIT 6 - CONTROLLER 0 3380-JK POWER ON BIT

For 3380-JK, this bit is the 16th RCC bit transferred from the controller addressed as 0 on the CTL-I interface. The bit should be a 1 if the transfer is successful and the controller is powered on. For 3380 AA4, AD4, AE4, this bit will be 0.

F^7B^{11} - BIT 7 - CONTROLLER 1 3380-JK POWER ON BIT

For 3380-JK, this bit is the 16th RCC bit transferred from the controller addressed as 1 on the CTL-I interface. The bit should be a 1 if the transfer is successful and the controller is powered on. For 3380 AA4, AD4, AE4, this bit will be 0.

Controller 0 or 1 Check-1 Status, Byte 12 or 14

F^7B^{12},B^{14} - BITS 0, 1, AND 2 - INPUT/OUTPUT CONTROL CARD ISOLATION BITS

Bits 0, 1, and 2 are combined to indicate the kind of error detected on the input/output control card.

Bit	0	1	2	
	0	0	1	ROS Bit Parity Check (Controller Sequencer) See ECD-267.
	0	1	0	Transfer Clock Check See ECD-269.
	0	1	1	IOC Detected DDC Bus Out Parity See ECD-271.
	1	0	0	Register Data Bus Parity Check See ECD-273.
	1	0	1	Register 1 Parity Check (CTL-I Bus In) See ECD-274.
	1	1	0	Register 3 Parity Check (CDP Bus Out) See ECD-277.
	1	1	1	Controller Selection Check See ECD-279.

See ECD Index for locations of error descriptions.

F^7B^{12},B^{14} - BIT 3 - DDC BUS OUT PARITY CHECK

Bit 3 is set when the controller detects a bus out parity error from the storage director.

F^7B^{12},B^{14} - BIT 4 - CONTROLLER CLOCK CHECK

Bit 4 is set when missing or extra system clock signals (A through H) occur.

F^7B^{12},B^{14} - BIT 5 - CONTROLLER SEQUENCER CHECK

Bit 5 is set when any error is detected on the controller sequencer card. This check includes read-only storage (ROS) output parity, received clock signals, and received address lines.

F^7B^{12},B^{14} - BIT 6 - DDC BUS IN PARITY CHECK

Bit 6 is set with a Bus In 1 parity check, detected in the controller, when it occurs at any time other than data transfer. (The Set Read/Write command has not been issued.)

F^7B^{12},B^{14} - BIT 7 - INPUT/OUTPUT CONTROL CARD CHECK-1

Bit 7 is set when any one of the following seven checks on the input/output control card is set:

- An output selection check resulting from not having a one-and-only one register address selected
- A multiple input selection
- An in select parity check
- A format parity check
- A parity check from register 2
- A parity check from register 3 (CDP out register) when hardware is in control
- An out select parity check.

Controller 0 or 1 Check-1 Status 2, Byte 13 or 15

F^7B^{13},B^{15} - BIT 0 - DDC TAG-OUT SEQUENCE CHECK

Bit 0 is set when the controller detects an invalid tag-out sequence change from the storage director. The controller detects the changing status of more than one of the tag networks at a time or the change into an invalid sequence state.

F^7B^{13},B^{15} - BIT 1 - EXTENDED COMMAND, TAG SEQUENCE CHECK

Bit 1 is set when a tag out sequence error is detected during an extended command. The following tags set the check:

Bit 0	1	2	TAG
0	0	0	Null
1	0	0	Poll
1	1	0	Hardware Immediate

F^7B^{13},B^{15} - BIT 2 - CONTROLLER SEQUENCER MICROCODE DETECTED CHECK 1

Bit 2 is set by the controller sequencer microcode when the code detects an error condition.

The check conditions detected are in byte 16 or 18.

F^7B^{13},B^{15} - BIT 3 - CONTROLLER GATE DDC DRIVERS CHECK

Bit 3 is set when the DDC bidirectional buses are not set at bus out 0 and bus in 1 during command transfer times.

F^7B^{13},B^{15} - BIT 4 - RCC SEQUENCE CHECK

Bit 4 is set when the data received by an RCC sequence can be invalid. The data becomes invalid because a clock pulse from the storage director was not properly detected and used by the controller.

F^7B^{13},B^{15} - BITS 5 - 7 ALWAYS ZERO

Controller Sequencer Microcode Detected Check 1 Errors, Bytes 16 and 18

Format 7, Bytes 16 and 18 contain the Sequencer Microcode Detected Check 1 error description bytes for Controller 0 and 1.

The sequencer microcode, upon detecting a Controller Check 1 condition, sets an error description byte into Register '1F' and Controller Sequencer Microcode Detected Check-1, byte 13 or 15, bit 2. The subsequent RCC sequence will collect the contents of Register '1F' for the storage control to place in the Format 7 sense data.

If byte 13 or 15, bit 2 is not active, the contents of Register '1F' contains a non-error state description code. This code indicates the routine the microcode is in or its state. The codes are within the following list.

00 End of RCC sequence, Hang Reset sequence about to start. This is not a failure.

02 Controller Sequencer And/Or IOC Register Failure. (see error description on ECD-298)

04 Controller Sequencer Counter Failed (see error description on ECD-299)

08 This value indicates a successful forced Check-1 microdiagnostic to the MD. This is not a failure.

0A Internal Logic Check-Out successfully completed after either the Controller Power Up sequence or the Hang Reset sequence. This is not a failure; this is the normal operating state.

0C Hang Reset Sequence Completed, Start of the Internal Logic Check-Out. This is not a failure.

0E Start of Controller Power On Reset Routine. This is not a failure.

10 Controller Command active with a DPS Command on the DDC Bus Out lines. (see error description on ECD-301)

12 Controller Command, DPS Command or Selected stuck active. (see error description on ECD-303)

14 Diagnostic, Invalid Diagnostic Command or Subcommand Received. (see error description on ECD-305)

15 Diagnostic, Invalid Extended Subcommand Received. (see error description on ECD-306)

18 During Timeout Routine, 'Allow Selection' detected Off, with 'Device Selected' detected On. (see error description on ECD-307)

1A During Timeout Routine, the DDC Tag Out lines are in the Selected Null state with the CDP Tag In lines in the Valid state. There are no Controller Check-2's active. (see error description on ECD-309)

20 Controller Command active without the DDC Tag Out lines being in a Command Gate state. (see error description on ECD-311)

22 DPS Command active with a Non-DPS Command on the DDC Bus Out lines. (see error description on ECD-313)

32 Reset Allegiance, at the beginning either the Device Selected latch was active or the CDP Tag In lines were not in the Null state. (see error description on ECD-314)

34 Reset Allegiance, Invalid Device Address Received from the Storage Control. (Bits 1, 2 or 3 not 0's) (see error description on ECD-316)

36 During either the Timeout Routine or while executing the Sense Fault Log Command, the DDC Tag Out lines are detected in an invalid state. (see error description on ECD-318)

70 Invalid Tag State on the DDC Tag Out lines. (see error description on ECD-320)

72 Internal '1D' Register Failure. (see error description on ECD-321)

74 Invalid Command on the DDC Bus Out Lines. (see error description on ECD-323)

76 Diagnostic, Invalid Command on the DDC Bus Out Lines. (see error description on ECD-324)

78 Diagnostic, Invalid Tag State on the DDC Tag Out lines. (see error description on ECD-326)

CE During Device Power On, Controller Failed to Take Control. (see error description on ECD-327)

Controller 0 or 1 RCC Transfer Status, Bytes 17 and 19

F^7B^{17},B^{19} - BIT 0 - CONTROLLER UNDERVOLTAGE STATUS

Bit 0 is reset to zero when the logic detects an undervoltage condition and a controller check 1 is active.

F^7B^{17},B^{19} - BITS 1 and 2 - CONTROLLER LOCATION IN THE STRING

Bits 1 and 2 identify the controller reporting the RCC Data.

Bits 1	2	Controller
0	0	Path 0 Controller (Controller A1)
0	1	Path 1 Controller (Controller A2)
1	0	Path 2 Controller (Controller A3)
1	1	Path 3 Controller (Controller A4)

F^7B^{17},B^{19} - BIT 3 - ALWAYS 1

These bits are always 1 on a correctly operating machine. Power problems can cause these bits to be incorrectly set on the controller sequencer card.

F^7B^{17},B^{19} - BIT 4 - POWER SEQUENCE COMPLETE

Bit 4 indicates that the power-on sequence of the controller completed.

F^7B^{17},B^{19} - BIT 5 - CHECK 2 ACTIVE

Bit 5 indicates that the controller currently has a CHECK 2 active.

F^7B^{17},B^{19} - BIT 6 - SUCCESSFUL TRANSFER COMPLETE

Bit 6 indicates that the controller successfully transferred its RCC latched errors to the storage director.

F^7B^{17},B^{19} - BIT 7 - ALWAYS 0

Controller Fault Log A, Byte 11

The information for the controller fault log bytes is collected as responses to the Sense Fault Log (hex 10) command. The Sense Fault Log command collects all seven controller fault log bytes (A through G) and then resets the controller check-2 latches. The fault log byte values are ignored by the storage director if the byte on the 'DDC bus in' lines is not validated by a Valid tag in. The storage director substitutes hex FF for the fault log byte value if the Valid tag is missing.

The controller fault log A byte is in byte 11 of EREP format 8.

F^8B^{11} - BIT 0 - DHPLO DELTA FREQUENCY CHECK

Bit 0 is set when the frequency of the voltage controlled oscillator exceeds its specified limits during a write operation.

F^8B^{11} - BIT 1 - DHPLO NON-DRIVE CHECK

Bit 1 is set when the data handling phase-locked oscillator (DHPLO) card detects a missing servo/PLO clock input signal from the selected device on the DHPLO card.

F^8B^{11} - BIT 2 - READ/WRITE DATA CABLE CHECK

Bit 23 indicates a defect to the differential R/W Data lines between the Read/Write Channel card in the device and the DHPLO card in the controller occurred.

F^8B^{11} - BIT 3 - DATA VALID CHECK

This bit is active if logic determines that the write data contains invalid 2/7 encoded data. It indicates that a write transition has not occurred within expected limits.

F^8B^{11} - BIT 4 - DHPLO FAILED TO LOCK CHECK

Bit 4 is set when the DHPLO fails to lock to the servo PLO. Missing or extra servo clock pulses are detected on the DHPLO card.

F^8B^{11} - BIT 5 - DHPLO MULTIPLE SELECT CHECK

Bit 5 is set when both of the data handling phase-locked oscillator (DHPLO) control lines, Servo and Lock PLO to Data, are active at the same time on the DHPLO card.

F^8B^{11} - BIT 6 - NO READ DATA CHECK

If no Read Data is received for about four byte times, this check is set.

F^8B^{11} - BIT 7 - CONTROLLER UNDERVOLTAGE STATUS

This bit is set to one when the circuits detect an undervoltage condition and a Controller Check-2 is active.

Controller Fault Log B, Byte 12

F^8B^{12} - BIT 0 - SERDES CONTROL CHECK

This bit active indicates that one of the following checks occurred.

- Select Check on the IOC card
- A SERDES Control Check on the Clock/SERDES/ECC card
- An ECC Control Check on the Clock/SERDES/ECC card

F^8B^{12} - BIT 1 - CLOCK/SERDES/ECC CARD CHECK

This bit active indicates that one of the following checks occurred.

- An Encoder/Decoder Check on the Clock/SERDES/ECC card
- A SERDES Shift Check on the Clock/SERDES/ECC card
- An ECC Data Parity Check on the Clock/SERDES/ECC card

F^8B^{12} - BIT 2 - SERDES PATH CHECK

This bit active indicates that one of the following checks occurred.

- A SERDES Load Check on the Clock/SERDES/ECC card
- A Serial Data Check on the Clock/SERDES/ECC card
- A Write Data Parity Check on the Clock/SERDES/ECC card

F^8B^{12} - BIT 3 - UNUSED

F^8B^{12} - BIT 4 - SERDES TWO CARD INSTALLED

This bit active indicates that there is a SERDES Two card installed in this controller. Controllers may or may not have this card installed. The bit is used by the maintenance package to generate valid FRU lists.

F^8B^{12} - BITS 5 thru 7 - UNUSED

Controller Fault Log C, Byte 13

F^8B^{13} - BIT 0 - UNUSED

F^8B^{13} - BIT 1 - CONTROLLER SEQUENCER CHECK-2

Bit 1 is set when the logic detects a parity error when Register 1F is used to report Controller microcode detected errors.

F^8B^{13} - BIT 2 - UNUSED

Bit 2 is unused, but it may be either a zero or a one.

F^8B^{13} - BIT 3 - MULTIPLEXER INPUT PARITY CHECK

Bit 3 is set when a multiplexer parity error occurs on the Input/Output control card.

F^8B^{13} - BIT 4 - CDP REGISTER 3 PARITY CHECK

Bit 4 on indicates that a parity check is detected on the CDP bus out register.

F^8B^{13} - BIT 5 - INPUT/OUTPUT CONTROL CARD CHECK-2

Bit 5 is set when one of the registers on the input/output control card has a parity check.

F^8B^{13} - BIT 6 - PRECOMPENSATION CHECK

Bit 6 is set when a comparison of the precompensation control signals fails.

F^8B^{13} - BIT 7 - WRITE GAP 3 CONTROL CHECK

Bit 7 is set when the parity of the control lines to the gap 3 logic is incorrect.

Controller Fault Log D, Byte 14

F^8B^{14} - BITS 0 THROUGH 3 — DEVICE CHECK 1

An active bit (any one) in any of these four bit positions indicates a device check-1 condition was detected by a device on the CDP in use. The position of the bit indicates the low-order two bits of the device address of the device (or devices) that detected a check-1.

Each device on a port is assigned a CDP data bus bit line for reporting device check-1 errors during the collecting of fault log D.

Bits 0 through 5 are collected from the device. Bits 6 and 7 are collected from the controller.

The failing port, when a Sense Error Log command is issued by the storage director, is indicated by fault log D (Byte 14) bits 6 and 7 and fault log G (Byte 17) bits 5 and 6.

See "F^8B^{14} - BITS 6 AND 7 — CDP PORT SELECTION BITS 0, 1"

F^8B^{14} - BITS 4 AND 5 — ISOLATION BITS 0, 1

Bits 4 and 5 indicates the check that set the Device Check 1.

The following figure shows how bits 4 and 5 are used to identify the check that set the Device Check 1.

Bit 4	*Bit 5*	*Check that set the Device Check 1*
0	0	Tie-Break Check
0	1	Clock Check
1	0	Port Card Check
1	1	CDP Interface Check

F^8B^{14} - BITS 6 AND 7 — CDP PORT SELECTION BITS 0, 1

Bits 6 and 7 indicates the port in use only when one of the following Fault Log G (Byte17) errors occur:

Bit 1. Drive to CDP Card Check
Bit 2. Port Response Check
Bit 3. CDP Active Drivers
Bit 4. Selected Device Check-1

The following figure shows how bits 6 and 7 identify the port in use. Byte 17 Bit 5 active indicates ports 0 thru 3 in use, while Byte 17 Bit 6 active indicates ports 4 thru 7 in use.

Fault Log D Sense Byte 14 - Bits - 0 1 2 3 6 7	*Fault Log G Byte 17 - Bits - 5 6*	*Device*	*Port In Use*
1 - - - 0 0	1 0	00	0
- 1 - - 0 0	1 0	01	0
- - 1 - 0 0	1 0	02	0
- - - 1 0 0	1 0	03	0
1 - - - 0 1	1 0	04	1
- 1 - - 0 1	1 0	05	1
- - 1 - 0 1	1 0	06	1
- - - 1 0 1	1 0	07	1
1 - - - 1 0	1 0	08	2
- 1 - - 1 0	1 0	09	2
- - 1 - 1 0	1 0	0A	2
- - - 1 1 0	1 0	0B	2
1 - - - 1 1	1 0	0C	3
- 1 - - 1 1	1 0	0D	3
- - 1 - 1 1	1 0	0E	3
- - - 1 1 1	1 0	0F	3
1 - - - 0 0	0 1	10	4
- 1 - - 0 0	0 1	11	4
- - 1 - 0 0	0 1	12	4
- - - 1 0 0	0 1	13	4
1 - - - 0 1	0 1	14	5
- 1 - - 0 1	0 1	15	5
- - 1 - 0 1	0 1	16	5
- - - 1 0 1	0 1	17	5
1 - - - 1 0	0 1	18	6
- 1 - - 1 0	0 1	19	6
- - 1 - 1 0	0 1	1A	6
- - - 1 1 0	0 1	1B	6
1 - - - 1 1	0 1	1C	7
- 1 - - 1 1	0 1	1D	7
- - 1 - 1 1	0 1	1E	7
- - - 1 1 1	0 1	1F	7

Controller Fault Log E, Byte 15

This byte should be all zero when attached to a 3990, or this is a 3380 Model CJ2. If this byte contains a bit when attached to 3990, or this is a 3380 Model CJ2, the fault is in the error collection logic because the DPS cards, that use this fault log, should not be installed in the controllers.

The controller fault log E byte is in byte 15 of EREP format 8. Ignore this byte if it contains hex FF.

F^8B^{15} - BIT 0 - DPS ARRAY CHECK

The DPS Array Check indicates that the DPS logic detected an array parity error or an array read or write control error on the controlling side of the DPS function.

F^8B^{15} - BIT 1 - DPS INTERNAL CHECK

An error has been detected on one or more of the internal busses or control lines within the DPS card of the controller which reported the error.

F^8B^{15} - BIT 2 - DPS COMPARE CHECK

When data is read from the DPS storage array, it is concurrently read from both controller DPS halves for comparison to ensure the integrity of the data in the arrays. The compare is performed by the primary DPS half. The Check indicates that the comparison was not equal.

F^8B^{15} - BIT 3 - DPS CONTROLLER-to-CONTROLLER CONNECTION CHECK

This indicates that the controlled side of the DPS logic has detected an error during communication between the two halves. If this failure occurs singularly, the culprit is most likely the other DPS card.

F^8B^{15} - BIT 4 - DPS STORAGE ADDRESS REGISTER CHECK (SAR Check)

A DPS storage address register check indicates that an address parity or selection error was sensed while addressing the DPS storage array during a DPS array read or write operation.

F^8B^{15} - BIT 5 - DPS INTERNAL REGISTER CHECK

An error has been detected on the output of the DDC Bus Out register or an illegal state has been detected on the DDC Tag Out register.

F^8B^{15} - BIT 6 - DPS ALTERNATE CHECK (WAIT/LOCK CHECK)

An error was detected by the primary DPS half. The error may be caused by an internal failure of the primary DPS half or a failure of the CCC interface between the two DPS halves. Bit 1 on indicates a parity error on either of the internal DPS buses.

F^8B^{15} - BIT 7 - UNUSED

Controller Fault Log F, Byte 16

F^8B^{16} - BIT 0 - DTB BUS OUT PARITY CHECK

Bit 0 is set when the DDC/DTB card detects a parity error on either bus 0 or bus 1 while handling write data.

F^8B^{16} - BIT 1 - DTB BUS IN PARITY CHECK

Bit 1 is set when the DDC/DTB card senses a parity error on the read data received from the clock/SERDES/ECC card.

F^{8}B^{16} - BIT 2 - DTB CONTROL CHECK

Bit 2 is set when there is a hardware failure on the DDC/DTB card. Possible failure is:

- Selection of more than one or none of the data transfer multiplexer registers

F^{8}B^{16} - BIT 3 - READ/WRITE GATE DDC DRIVERS CHECK

Bit 3 is set when the driver/receiver logic detects a gating error on the DDC data buses during a read or write operation.

F^{8}B^{16} - BITS 4 Thru 7 - STRING CONFIGURATION

Bits 4 thru 7 indicate the number of units in the string. The configuration of the string is set into the String Configuration switches 1 thru 4 manually by the installing CE. The configuration information is used by the operating system, the diagnostics, and the error message software. An active bit 4 indicates its associated String Configuration Switch 1 is set to On.

In the following tables, A is an A-unit and B is a B-unit. For example, the string ABB, is a single A-unit with two B-units.

Two Path Configurations

Byte 8 Bit 1, String Has a Four Path Capability is inactive indicating a two path configuration. Bits 4 and 5 are valid while Bits 6 and 7 are undefined in the two path configuration.

4,5	Configuration
00	A Unit only (Addressed as 00-03)
01	AB or BA (Addressed as 00-07)
10	ABB or BBA (Addressed as 00-0B)
11	ABBB or BBBA (Addressed as 00-0F)

Four Path Configurations

Bits 4 thru 7 are all used with a four path configuration. With Byte 8 Bit 1 active, Bits 6 and 7 are recognized.

Bits 4 and 5 are assigned to the substring addressed as 00-0F.

45	Configuration
00	A Unit (Addressed as 00-03)
01	AB or BA (Addressed as 00-07)
10	ABB or BBA (Addressed as 00-0B)
11	ABBB or BBBA (Addressed as 00-0F)

Bits 6 and 7 are assigned to the substring addressed as 10-1F.

67	Configuration
00	A Unit (Addressed as 10-13)
01	AB or BA (Addressed as 10-17)
10	ABB or BBA (Addressed as 10-1B)
11	ABBB or BBBA (Addressed as 10-1F)

Controller Fault Log G, Byte 17

F^{8}B^{17} - BIT 0 - CONTROLLER TO CDP CARD CHECK

This bit active indicates an error was detected in the CDP interface logic and the most likely area of the fault is within the controller logic.

F^{8}B^{17} - BIT 1 - DRIVE TO CDP CARD CHECK

This bit active indicates an error was detected in the CDP interface logic and the most likely area of the fault is within the device logic.

F^{8}B^{17} - BIT 2 - PORT RESPONSE CHECK

The CDP check logic, with a port selected, detected another port with active tags.

F^{8}B^{17} - BIT 3 - CDP ACTIVE DRIVERS

Bit 3 is set when the device incorrectly gates the CDP bidirectional data bus during a device selection or a command transfer.

F^{8}B^{17} - BIT 4 - SELECTED DEVICE CHECK-1

Bit 4 is set when a Device Check-1 occurs on the selected device. The check is sensed on the CDP card.

F^{8}B^{17} - BIT 5 - SUBSTRING 0 SELECTED

This status bit indicates Substring 0, or Ports 0 thru 3 and devices 00 thru 0F, identified by Byte 14 Bits 6 and 7, was selected by the CDP logic.

F^{8}B^{17} - BIT 6 - SUBSTRING 1 SELECTED

This status bit indicates Substring 1, or Ports 4 thru 7 and devices 10 thru 1F, identified by Byte 14 Bits 6 and 7, was selected by the CDP logic.

F^{8}B^{17} - BIT 7 - PORT DEGATE CHECK

One of the CDP ports indicates 'Degated'.

Controller Sequencer Microcode Detected Check 2 Errors, Byte 18

Byte 18 displays the sequencer microcode detected Check 2 errors of the Controller, only when Format 8 Byte 9 contains an End Op code of 12.

The controller microcode, upon detecting an error condition will set an End Op code of 12, (Controller Sequencer Detected Error). The storage director, on sensing the error condition End Op, issues a Sense Fault Logs command. The subsequent operation collects the error for the Format 8 sense data.

If the End Op code is not 12 in byte 9, Byte 18 will contain, in most instances, the last DDC Read/Write command from the storage director to the controller prior to the error.

Note: *The second entry is the undervoltage detected in the controller error. For example, 01 is Index Not Active when Expected, and 81 is Index Not Active when Expected with undervoltage detected in the controller.*

01	81	Index Not Active when Expected (see error description on ECD-356)
02	82	Index Active when Not Expected (see error description on ECD-358)
03	83	Cell Pulse Not Active when Expected (see error description on ECD-360)
04	84	Cell Pulse Active when Not Expected (see error description on ECD-362)
05	85	Searched Cell, Cell Pulse Off (see error description on ECD-364)
06	86	Address Mark or Index Not Active When Expected (see error description on ECD-366)
07	87	Orientated Not Active When Tested (see error description on ECD-368)
10	90	First Byte Ready Active When Not Expected (see error description on ECD-369)
14	94	Address Mark Active When Not Expected (see error description on ECD-371)
15	95	Diagnostic, Lock PLO To Servo Not Active When Expected (see error description on ECD-373)
17	97	Write ASRP Active When Not Expected (see error description on ECD-374)
18	98	Lock PLO To DATA Not Active When Expected (see error description on ECD-376)
19	99	Any Check and Any Check Duplicated Mismatched (see error description on ECD-377)
20	A0	CDP Tag in at Valid, Expected Selected Null (see error description on ECD-378)

21 A1 In Reset Allegiance Command, The Device Returned an Incorrect Address. (see error description on ECD-379)

22 A2 CDP Tag In was not at Selected Null, it is now at Selected Null. (see error description on ECD-381)

51 D1 Data Check Recovery Routine, Expected Device Checkpoint 'CE' Occurred too Soon. (see error description on ECD-382)

52 D2 Data Check Recovery Routine, Expected Device Checkpoint 'CE' or '7X' Received. (see error description on ECD-382)

53 D3 Data Check Recovery Routine, Expected Device Checkpoint '19' or '0X' Received. In Response to CMD 13, Expected Drive Checkpoint of 19 or 0X. (see error description on ECD-382)

55 D5 Data Check Recovery Routine, Expected Device Checkpoint '0X' Occurred to Soon. (see error description on ECD-382)

56 D6 Data Check Recovery Routine, Pad-In-Progress Active When Not Expected. (see error description on ECD-383)

57 D7 Data Check Recovery Routine, Expected Device Checkpoint '0X' Failed to Occur. (see error description on ECD-382)

58 D8 Data Check Recovery Routine, Device Checkpoint of '7X' is Still Active When Not Expected. (see error description on ECD-382)

70 F0 Diagnostic, Start/Run CDP Timeout Bit Not Active When Expected (see error description on ECD-384)

71 F1 Diagnostic, Controller Command Bit Not Active When Expected. (see error description on ECD-384)

72 F2 Diagnostic, DPS Command Bit Active When Not Expected. (see error description on ECD-384)

73 F3 Diagnostic, Allow Selection Bit Active When Not Expected. (see error description on ECD-384)

74 F4 Diagnostic, Device Selected Bit Active When Not Expected. (see error description on ECD-384)

75 F5 Diagnostic, Start/Run CDP Timeout Bit Active When Not Expected (see error description on ECD-384)

76 F6 Diagnostic, Controller Command Bit Active When Not Expected. (see error description on ECD-384)

77 F7 Diagnostic, Sequencer Counter Failure. (see error description on ECD-387)

78 F8 Diagnostic, Unexpected Failure During The Running of Sub-Routine 'E0' of Diagnostic '80'. (see error description on ECD-384)

Read/Write Status-1, Byte 12

F^9B^{12} - BITS 0 and 1 - FRU BITS

FRU bits 0 and 1 indicate the general area of the error as shown in the table below.

Bit 0	Bit 1	FRU Location
0	0	Normal (no error)
0	1	R/W channel board
1	0	B board
1	1	Read cable error

F⁹B¹² - BIT 2 - REDUNDANT LINE / SELECTION CHECK

Control lines going from the read/write control card to the read/write channel board are duplicated. Circuits in the read/write channel board check for both lines and a redundancy check results if one line is there without the other.

F⁹B¹² - BIT 3 - NO READ/WRITE RECOVERY

During write mode, conditions are monitored by the read/write channel board that would indicate a problem with selecting and using an arm in the HDA. Bit 3 indicates that an Arm Electronics error has been detected during a write operation.

F⁹B¹² - BIT 4 - INHIBIT OR RESET ACTIVE

Bit 4 is not an error condition. It is an indication that either drive check reset or drive check inhibit has been detected by the read/write channel board.

F⁹B¹² - BIT 5 - READ AND WRITE CHECK

Bit 5 indicates that while read transmit is active, (indicating a read operation is in progress) write gate is active, (indicating a write operation is in progress). A read and a write operation should not occur at the same time.

F⁹B¹² - BIT 6 - HAR BUS PARITY CHECK

The 15 available heads in the HDA are selected using 'HAR bus bits 4-7'. The HAR bus P bit is used to maintain odd parity when the HAR bits are sent to the read/write channel board from the read/write control card. HAR bus parity check is set if even parity is detected on the 'HAR bus bits 4-7 + P'.

F⁹B¹² - BIT 7 - DATA DETECTOR CHECK

Bit 7 indicates that any one of four error conditions checked for by the read/write board is present. The four errors are:

Read cable error
Write cable error
Read status error
Select status error

Read/Write Status-2, Byte 13

F⁹B¹³ - BIT 0 - READ/WRITE CHANNEL CHECK

Bit 0 indicates that an error has been detected by the read/write channel board. The bit is set if either Read/Write Status 1 (Byte 12) or Read/Write Status 4 (byte 18) Bit 0 or 1 is equal to 1.

F⁹B¹³ - BIT 1 - PADDING CHECK

During the pad to index operation, pad control circuits use three latches which are stepped with Primary Write Gate, CDP Bus Bit 3, Index and RPS Clock T-0 lines. Bit 1 indicates that the padding sequence latches have stepped incorrectly or one of the controlling lines has failed.

F⁹B¹³ - BIT 2 - READ/WRITE SEQUENCE CHECK

During read and write operations, 'CDP bus bits 4-7' are decoded by the read/write control card into six control lines. These lines are used to control the functions of the read/write channel board. The control lines are monitored for correct sequence during read and write operations and sequence check results if an invalid sequence is detected.

F⁹B¹³ - BIT 3 - INDEX / CELL CHECK

Bit 3 indicates that either the cell bit count was incorrect or an Index pulse error occurred. The two index pulses are compared in length, and if they are not equal this error is set.

F^9B^{13} - BIT 4 - SERVO CABLE CHECK

Bit 4 indicates that the impedance of the servo cable is not balanced. This usually is caused by a cable fault or a fault in the associated drivers and receivers.

F^9B^{13} - BIT 5 - WRITE OVERRUN CHECK

Bit 5 indicates that index was passed while write gate was active. It can also indicate that there is a failure in the check circuit hardware.

F^9B^{13} - BIT 6 - READ/WRITE SERVOMECHANISM CHECK

Bit 6 indicates that the servo mechanism was not correctly following the track during a read or write operation.

F^9B^{13} - BIT 7 - HEAD ADDRESS REGISTER PARITY CHECK

Bit 7 indicates that the head address register, located in the read/write control card has even parity during R/W mode select.

Read/Write Status-3, Byte 14

F^9B^{14} - BIT 0 - CHECK INHIBIT CHECK

Bit 0 indicates that either Check Inhibit is active in the read/write channel board and it should not be, or it is inactive and it should be active. Check Inhibit is activated when control lines to the read/write channel board are changed to prevent false errors.

F^9B^{14} - BIT 1 - READ/WRITE CHANNEL STATUS PARITY CHECK

Bit 1 indicates that the data from the read/write channel board which is latched in the read/write control card, has even parity.

F^9B^{14} - BIT 2 - READ TRANSMIT CHECK

Bit 2 is a multipurpose check. It means that any one of four check conditions has occurred. The checks are Read Transmit check, Read Transmit Counter check, Write Mode Verify check, and Select check. The first two errors have to do with the 'read transmit' control line being set and the fourth error has to do with device selection errors.

F^9B^{14} - BIT 3 - READ/WRITE CONTROL CABLE CHECK

Bit 3 indicates the possibility that the read/write control cable from the 'B' board to the read/write channel board is disconnected.

F^9B^{14} - BIT 4 - READ TRANSMIT ACTIVE

Bit 4 is a status bit to indicate if Read Transmit was active at the time of the error.

F^9B^{14} - BIT 5 - WRITE GATE ACTIVE

Bit 5 is a status bit to indicate if Write Gate was active at the time of the error.

F^9B^{14} - BIT 6 - UNUSED

F^9B^{14} - BIT 7 - UNUSED

Bit 7 is unused, but it may be either a zero or a one.

Read/Write Status 4, Byte 18

F^9B^{18} - BITS 0 AND 1 - FRU BITS

FRU Bits 0 and 1 indicate the general area of the error as shown in the table below.

Bit 0	Bit 1	FRU Location
0	0	Normal (no error)
0	1	R/W channel board
1	0	B board
1	1	Read cable error

F^{9}B^{13} - BIT 2 - MULTIFUNCTION

Bit 2 indicates the status of the arm electronics. If bit 2 is active, then more than one arm has been selected.

F^{9}B^{18} - BIT 3 - NO FUNCTION

Bit 3 indicates the status of the arm electronics. If bit 3 is active, then no arm has been selected.

F^{9}B^{18} - BIT 4 - ARM ELECTRONICS SELECTED

Bit 4 indicates the status of the arm electronics. If bit 4 is active, then an arm has been selected.

F^{9}B^{18} - BIT 5 - WRITE MODE VERIFY

Bit 5 indicates the status of the arm electronics. If bit 5 is active, an arm is actually in write mode.

F^{9}B^{18} - BITS 6 AND & 7 - ARM ELECTRONICS STATUS 2 AND 1

Bits 6 and 7 change status as the operational modes change between standby, read, write, and back to standby. In write mode both bits should be active. In standby or read mode, both bits should be inactive.

Format 8, Message A

Missing Device Interrupt Detected by the Storage Control While it was Processing an Internal Command Chain

When a storage control, with a Dual Copy Feature, communicates with a device with an internal CCW command chain, it disconnects at times. While it is waiting for the expected interrupt from the device it may time out. The storage control then selects the device and collects its sense data. If it collects error data, it will present that data in the correct format. If it does not find an error with the device, it will post this message A.

EC History of Sense Section

EC HISTORY OF P/N 4519948			
EC Number	Date Of EC	EC Number	Date Of EC
475245	14Nov86	475248	25Apr88
475246	21Jul87		
475247	11Sep87		

Notes:

About This Section

The OPER section is for the person who desires to know theory about the 3380-JK.

The OPER section emphasizes similarities between operations. Similar operations are grouped, and their common characteristics are described. Thereafter, only the differences between the operations are described.

Because most of the information in the OPER section is theory, the OPER section does not contain procedures for the reader to perform. The only direct benefit one can expect from reading the OPER section is better understanding of the operations of the 3380-JK.

The OPER section is not intended to be used as introductory material. The OPER section is intended to be used by experienced people who have completed the CE training course on the 3380-JK.

P/N 4519952 129 Sides EC 475248 25Apr88

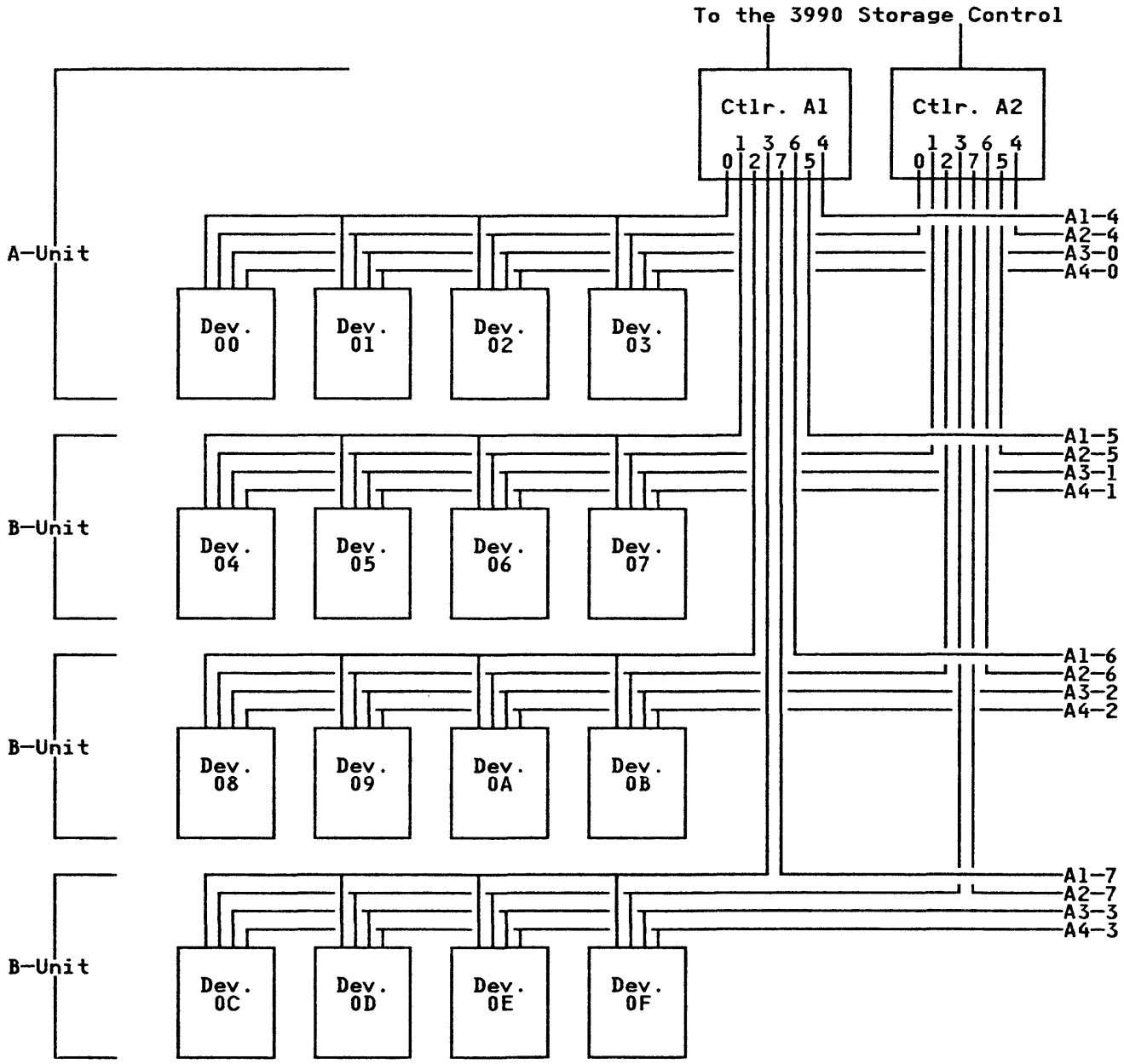


Figure 1. First Half of a Full Four-Path Configuration

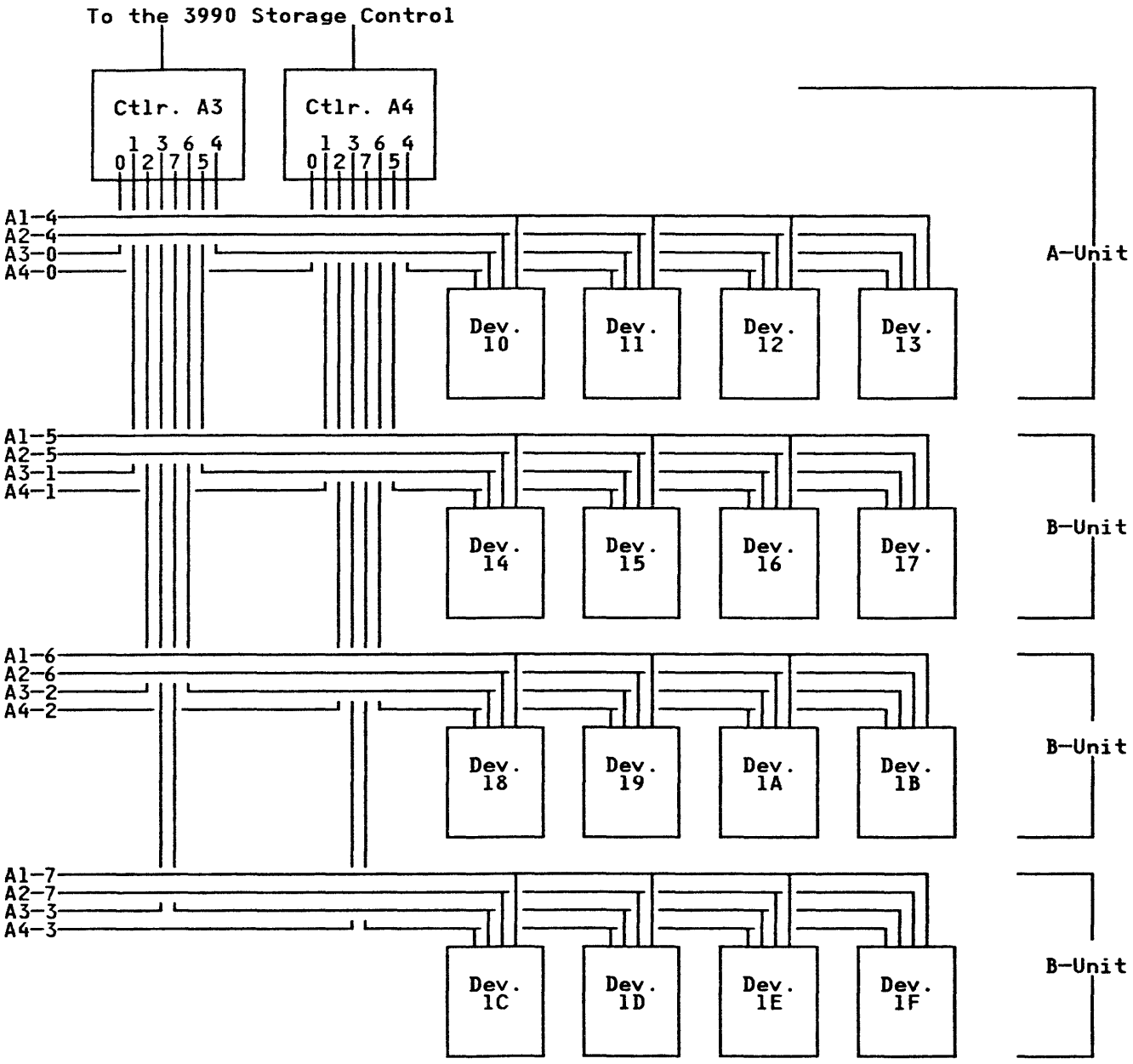


Figure 2. Second Half of a Full Four-Path Configuration

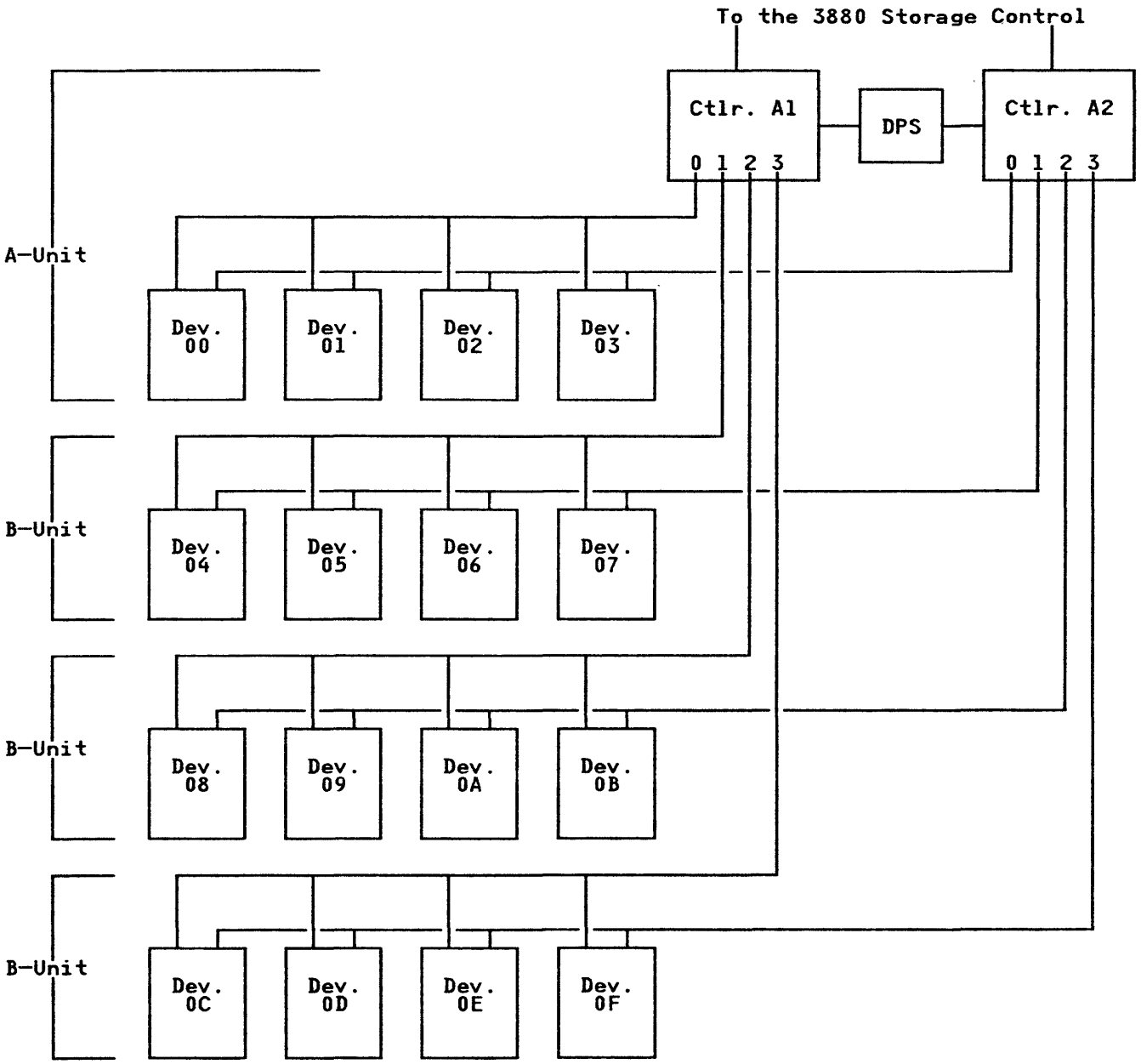


Figure 3. Two-Path Configuration

Introduction

An IBM 3380-JK Direct Access Storage string contains one A unit and may contain up to three B units, when running two-path. Two-path may be run when attached to either a 3880 or 3990.

An IBM 3380-JK Direct Access Storage string contains two A units and may contain up to six B units, when running four-path. Four-path may only be run when attached to a 3990.

An A unit contains two controllers and two drives.

Each B unit contains two drives but no controllers.

Every drive contains two separate access mechanisms in a single head and disk assembly (HDA). Each access mechanism has exclusive access to data surfaces on the disks.

Each 3380-JK string connects to two storage directors in IBM 3880's or to two or four storage paths in IBM 3990's, which connects to the system channel. The storage directors in the 3880 or storage paths in the 3990 contains a microprogram that is needed for communicating with the 3380-JK string.

When running two-path both controllers have access to each access mechanism through paths that are exclusive. When running four-path four controllers have access to each access mechanism through paths that are exclusive. The Dynamic Path Selection circuits, in the 3380-JK, (only when attached to a 3880) and the Shared Control Array, in the 3990. are needed to coordinate device access between controllers. This is done to prevent the controllers from interfering in each other's operations with the devices.

The figures on pages OPER-4 and OPER-2 show a full 2-Path string configuration. The figures show the four paths from each controller for communications between the controller and the devices. Each path serves two drives or four devices.

The figures on pages OPER-2 and OPER-3 show a full 4-Path string configuration. The figures show the eight paths from each controller for communications between the controller and the devices. Each path serves two drives or four devices.

Physical Parts

A Logic

The A board contains the controller cards. The cards for both controllers are contained in the same A board. The A board also contains the DPS cards unless attached to a 3990.

B Logic

The B board contains cards for the four devices in the unit.

HDA

Each drive has an HDA associated with it. The HDA in the front of the unit is named the front HDA and is associated with the cards in the left half of the B board.

The HDA in the rear of the unit is named the rear HDA. It is associated with the cards in the right half of the B board.

Each HDA contains two access mechanisms, one on the left and one on the right of the HDA as one faces the pulley side of the HDA. These locations lead to the description of the four devices in a unit as the front left device, the front right device, the rear left device, and the rear right device.

Read/Write Channel

The cards that are mounted on the HDAs are called read/write channel boards. One of these read/write channel boards is associated with each device (two with each HDA). The read/write channel boards have C board designations.

Power Supplies

Two power supplies one on top of the other, one for each controller, are located in the lower front of the A units. These power supplies can be powered on and off individually.

A single power supply in the rear of the unit serves both drives (all four devices). The power from the drive power supply passes through a single access mechanism control panel, which permits power to be removed from device cards in the B and C boards without powering off the complete drive.

Tailgate

The tailgate connectors and the operator panel are located in the front of the unit. The DDC Interface (CTL-I) and Power Sequencing cables from the storage control and/or the other string connect to the tailgate.

Operator Panel

The operator panel contains:

- A Unit Emergency switch and AC Power-On indicator
- Two Controller switches and Ready indicators
- 16 Actuator switches and Ready indicators

The switches and indicators on the operator panel are described in the INTRO section in the Product Service Guide (PSG).

Air System

One air system in each unit supplies the filtered air that cleans and cools the inside of the HDAs. The air system supplies air that has passed through three progressively fine filters to a plenum for distribution to the two HDAs. The pressure in the HDAs keeps contaminants in the ambient air out of the HDAs.

Controller Functions

The controller performs the following functions:

- Communicates with a storage control
- Communicates with the devices
- Generates clock signals (synchronized and nonsynchronized)
- Presents interrupt status to the storage control
- Controls the flow of data and control signals in response to selection and commands
- Controls the read/write processes and processes read/write data
- Supplies error correction information for read errors
- Performs error checking and supplies status information to the storage control
- Provides a means for running diagnostics.

Communications between the storage control and the controller are through the control interface. These communications include:

- Polls and interrupt information
- Commands, command parameters, and responses to commands (status)
- Data
- Selection and deselection sequences

See OPER-13 for a description of the control interface.

Communications between a controller and a device are through the device interface. These communications include the same kinds of information as through the control interface with the addition of read/write control and drive power control.

During polls, the controller uses all four device interface ports to communicate with all the devices in the string.

During selection, the controller uses only one device interface port to select one of the four devices connected to the port.

For device commands and responses and for read/write control, the controller communicates with only the selected device.

See OPER-15 for a description of the device interface.

The controller generates a clock ring (8 separate clock steps) used to control circuit operations. During read operations, the clock ring is synchronized to the read data from the disk. During write operations, the clock ring is synchronized to information from the servo surface.

Interrupts permit the subsystem to start an operation in one device, and then disconnect from that device to service another device. When the started operation is completed, the device generates an interrupt signal to request service. The controller assembles interrupt information from all the devices in a string during polling and presents the interrupt information to a storage control.

The controller contains circuits that perform a partial decode of the commands from the storage control. If the command is a device command or a Dynamic Path Selection (DPS) command, these circuits control the internal paths for signals through the controller so that the controller sequencer is not controlling the operation. (The DPS feature is only installed in a 3380-JK that is attached to a 3880 storage control unit.) Commands and responses are exchanged directly between the storage control and the device (or DPS function). The controller sequencer monitors the operation, checking for error conditions, but having no control over the process.

If the command is a controller command or an extended command (read/write operations), the controller sequencer receives control of the operation, supplying control for circuits and guiding the flow of information in the controller.

See OPER-22 for a simplified description of the controller sequencer and the ways it controls an operation.

During read/write operations, the storage control, the controller, and a device are all involved.

The controller receives commands and write data from the storage control and receives rotational position information (index and cell boundary) and read data from the device.

The controller's part of read/write operations is controlled by the controller sequencer. The controller's part includes the following:

- Receiving and processing commands (extended commands) from the storage control
- Getting and maintaining orientation to the track format
- Supplying control signals for the read/write circuits in the device
- Requesting and receiving parallel write data from the storage control
- Serializing the write data, encoding it, and sending it to the device
- Receiving serial read data from the device
- Decoding the serial read data, deserializing it, and sending the read data to the storage control
- Recognizing status and reporting to the storage control at the end of each operation

For read error correction, the controller contains Error Correction Code (ECC) circuits, which process read and write data under the control of the controller sequencer. During write operations, the data bytes are processed in sub-blocks that are 96 bytes long. The ECC circuits generate a 6-byte error correction code for the 96 bytes, which is written on the disk immediately following the sub-block of data. The ECC circuits also process all the data that is written, to generate a separate 6-byte block error correction code. These 6-bytes are written behind the error correction code bytes for the last sub-block.

During read operations, each byte of data read is processed again to generate the 6-byte sub-block error correction codes and the final 6-byte block ECC. This time, the ECC's generated during the read operation are compared with the ECC bytes that were read with the data. If all the codes compare equally, the read operation is correct. If any were not equal, the result of the comparison and the location are used by the ECC circuits to control another process, which generates 274 bytes that is used by the storage control to correct the read error if it is correctable.

Device Functions

The device performs the following functions:

- Communicates with the controller
- Positions the access mechanism in response to commands
- Performs rotational position sensing and identifies index and cell boundaries
- Reads and writes data and control information on the disks
- Generates interrupt signals

Communications between the device and a controller are through the device interface. These communications include:

- Interrupt information during polls
- Commands, command parameters, and responses to commands (status)
- Selection and deselection sequences
- Read/write control and status
- Data
- Drive power control

See OPER-15 for a description of the device interface.

The access mechanism is put in position by a voice-coil motor, which operates by the interaction of the magnetic fields around a voice coil and a permanent magnet. The amount of current in the voice-coil controls the force, and the direction of the current determines the direction of the force.

The amount and direction of the voice-coil current is based on digital control signals, analog feedback signals, and analog signals read from the servo surface.

Alignment of the read/write heads to a cylinder is accomplished through the alignment of the servo head to a track on the servo surface.

Rotational position sensing circuits process digital information read from the servo surface to generate the 'index' signal and to identify cell boundaries. Index and cell boundary information is supplied to the controller through the device interface during read/write operations.

During read and write operations, the data streams into, or out of, the device. No clocks are used in the device for moving the data. Control signals are developed in the device to ensure protection of customer data and to control the read/write circuits in the device. These control signals are based on signals received from the controller through the device interface.

After the last record on a track, the drive can perform drive padding, which writes pad characters in the remainder of the track.

Drive padding is started by the controller when an End Read/Write command is received from the storage control while padding from the controller is in progress. After drive padding is initiated, the device supplies all the signals needed for controlling the operation to completion, and the controller can disconnect from the device. Drive padding stops after the index is recognized.

Devices generate an interrupt signal for any of the following reasons:

- Completion of the drive-motor power-on sequence, online and ready for access-positioning commands and read/write operations
- Not busy after being busy while selection was attempted
- Completion of a servo operation (seek, offset, or rezero), either normally or with an error
- Specified sector is under the read/write heads

The device sequencer provides the basic controls for the drive-motor power-on sequence in response to a command from the controller. When the sequence is successfully completed, the device sequencer sets the latch that generates the interrupt signal.

The device sequencer issues commands to the Digital Control Processor (DCP), which controls the access mechanism positioning operations, in response to commands from the storage control unit. When the access positioning operation is terminated, either successfully or with an error, the device sequencer sets a latch that generates the interrupt signal.

The device sequencer controls the start of a sector search operation and then monitors the operation until it is completed. Sector search operations are initiated by commands from the storage control. A command parameter identifies a sector number (0 through 221) as the target sector. When the target sector is under the read/write heads, the device generates an interrupt signal. The intent is that the target precedes data enough to allow the storage control to analyze interrupt information collected during a poll and select the interrupting device in time to issue the commands to access the data.

If the sector search operation fails to locate the target sector, the device sequencer sets a latch that generates the interrupt signal and also indicates the incomplete status of the operation.

If the device is selected while the drive is busy, such as while drive padding is in progress, circuits in the device are conditioned so that when the busy condition ends, a latch is set. The output from this latch causes an interrupt signal to notify the storage control (through a poll) that the device is free to accommodate commands.

To determine the cause of an interrupt, the storage control issues a Sense Device Status 1 command and decodes the status byte returned by the device.

See the SENSE section for a description of the device status 1 bits (format 1, byte 19).

DPS Functions (Optional)

The Dynamic path selection (DPS) feature is used to coordinate the access by the two controllers to any device in the string.

The DPS feature is only installed within a 3380-JK that is attached to a 3880 storage control unit. The Shared Control Array (in the 3990) provides the same function when attached to a 3990.

The functions in the string remain under the control of the storage controls, which receive their instructions through channel commands. The purpose of the DPS circuits is to supply and maintain storage for information about each device in the string so that the information is immediately available to both storage controls. The following kinds of information are maintained.

- The current position of the access mechanism for each device
- Path associations between storage control channels
- Path authorization for each device
- Owed Device End information for each device
- Pack Change Interrupt information for each device
- Reservation information about each device

The DPS circuits are contained in two cards that are exactly the same. A DPS card is physically contained in each of the controllers. Each DPS card contains a storage array that supplies storage for the device information. The information in the arrays is written or read during DPS command sequences, which are controlled by the storage controls.

Whenever information is written to one of the storage arrays, it is written to both storage arrays, no matter which storage control started the operation.

When information is read, it is read from both arrays and compared to ensure accuracy.

When first powered on, the DPS arrays must be initialized with device and channel information. This information is supplied through a storage control by one of the systems connected to the storage control. The storage control formats the device and channel information and sends the information to the DPS circuits as data for a write array operation. Thereafter, the information is dynamically updated.

If one of the controllers is powered off, which also powers-off the associated DPS card, the other DPS array contains all the information needed about the devices to continue normal operation. When power is restored, the storage control sends a command to copy the information in the updated array into the array that had been powered off, therefore ensuring the same information in both arrays.

Most changes in the information stored in the DPS arrays are through DPS commands.

The only times that the DPS circuits are involved in an operation other than through DPS commands is during device selection sequences.

During device selection sequences, the DPS circuits control the first responses sent to the storage control on the control interface. The DPS circuits analyze the selection address, generate the response byte, and control the tag-in response.

During device selection, the DPS circuits also analyze the information in the array and DPS registers to determine the availability of the device. This information is also returned to a storage control in the responses. If the device is available, the DPS circuits let the selection of the device continue.

To perform the DPS operations, the DPS circuits:

- Communicate with the storage control through controller circuits and the control interface
- Communicate with the DPS circuits associated with the other controller in the unit
- Respond to DPS commands
- Participate in selection sequences and generate the first responses during device selection

For communicating with the storage control, the DPS circuits receive outbound signals directly, after the signals have been powered by circuits in the DDC/DTB card. (The outbound signals are those on the DDC byte 0 bus and the DDC tag out bus.) The inbound signals from the DPS circuits to the storage control involve the feedthrough path in the controller.

For communications between two DPS cards, a group of lines known as the controller-to-controller connection is used. These lines connect the two DPS cards directly, and the lines are bidirectional.

The words primary and alternate in a DPS context have the following meanings. Primary describes the DPS card that receives the command from the storage control or that is more directly involved in device selection. Alternate describes the other DPS card, the one associated with the other controller.

The DPS commands are all immediate commands.

Control Interface

The control interface (CTL-I) that connects the storage control to the 3380-J/K controller is the control-to-device controller (DDC) interface.

All 24 signals in the DDC interface are differentially driven. Twenty-three of the 24 signals are grouped into four buses:

- DDC bus out/bus in byte 0 (bits 0 through 7, and parity)
- DDC bus out/bus in byte 1 (bits 0 through 7, and parity)
- DDC tag out (bits 0 through 2)
- DDC tag in (bits 0 and 1)

The remaining signal, 'connection check alert' (CCA), is an inbound signal. The 'CCA' line is used to notify the storage control when the controller recognizes a check 1 error. Check 1 errors interfere with normal communications between the storage control and the controller.

The mode of operation in the DDC interface determines the direction of the signals on the DDC bus in/bus out (bidirectional) buses as shown in the following table.

Bus Byte	Control Mode	Transfer Mode (Write)	(Read)
0	outbound	outbound	inbound
1	inbound	outbound	inbound

In control mode, the byte 0 bus carries commands and modifiers to the controller, and the byte 1 bus carries responses to the storage control.

In transfer mode, the byte 0 and byte 1 buses are driven in the same direction to transfer two bytes of data concurrently.

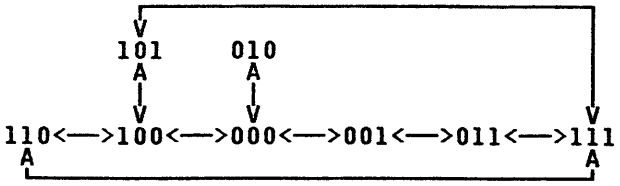
The control interface is always in control mode except during the transfer of data (for read/write operations) or during the transfer of error correction bytes (following read errors).

DDC Tag Out (Bits 0, 1, and 2)

The status of the three tag out bits combine to define a tag as shown in the following table.

TAGS	TAG OUT BITS 0	1	2
Null Disconnect	0	0	0
Select or Sync Out	0	0	1
Request Connection Check 1	0	1	0
Selected Null	0	1	1
Poll	1	0	0
Request Connection Check 2	1	0	1
Hardware Immediate	1	1	0
Command Gate	1	1	1

In normal DDC tag sequences, only one tag bit changes for each tag change. The following figure shows valid changes.



The following paragraphs describe the meanings of the tags.

Null Disconnect (000)

The Null Disconnect tag out indicates to the controller that it (the controller) and any device should be disconnected.

Select or Sync Out (001)

The Select tag out validates a selection address on DDC byte 0 bus during a selection sequence.

After selection, the Sync Out tag validates a command modifier on byte 0 (while the DDC is in control mode).

During transfer mode, the Sync Out tag has two meanings. Sync Out acknowledges the receipt of two bytes of read data during read operations, and Sync Out validates two bytes of write data during write operations.

Request Connection Check 1 (010)

The Request Connection Check 1 (RCC1) tag is set by a storage control to collect controller status when normal communications between the storage control and the controller do not work.

(The RCC1 tag is used both when the storage control detects the error and when the controller sends the 'CCA' signal.)

Selected Null (011)

The Selected Null tag out is the default tag while the storage control is logically connected to a controller.

Poll (100)

The Poll tag out validates the controller address and poll number on the DDC byte 0 bus and indicates the start of a polling operation to the addressed controller.

Request Connection Check 2 (101)

The Request Connection Check 2 (RCC2) tag is set by the storage control to collect controller status if an invalid response was received for a RCC1 sequence.

Hardware Immediate (110)

The Hardware Immediate tag out is set by the storage control to restore the DDC driver circuits in a controller to operational status.

The drivers in the controller are inhibited during the RCC1 and RCC2 sequences. This condition, called "fenced", isolates the controller so that it cannot send any responses (tags or data) to the storage control in the normal way. The Hardware Immediate tag resets the fenced condition.

Command Gate (111)

The Command Gate tag validates a command code on the DDC byte 0 bus while the DDC interface is in control mode.

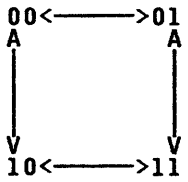
When the interface is in transfer mode, the Command Gate tag signals the controller to prepare to end the data transfer. The storage control sends the Command Gate tag instead of the Sync Out tag when only seven more transfers are needed to complete the data transfer in progress.

DDC Tag In (Bits 0 and 1)

The status of both tag in bits combine to define a tag as shown in the following table.

TAGS	TAG IN BITS 0	1
Null Disconnected	0	0
Valid or Sync In	0	1
Selected Null	1	1
End Op	1	0

In normal DDC tag sequences, only one tag bit changes for each tag change. The valid DDC tag in changes are shown in the following figure.



The following paragraphs describe the meanings of the tags.

Null Disconnected (00)

The Null Disconnected tag in indicates that the controller is not selected.

Valid or Sync In (01)

The Valid tag in validates a response (on the DDC byte 1 bus) to a command or to selection during control mode.

While the DDC interface is in transfer mode, a Sync In tag requests two bytes of data from the storage control for write operations or validates two bytes of data on the DDC byte 0 and byte 1 buses during read operations.

Selected Null (11)

The Selected Null tag in indicates that the controller is selected.

End Op (10)

The End Op tag in indicates that the current operation (for an immediate command) cannot be correctly completed because of an error. The End Op tag validates an end op code on DDC byte 1 bus. The end op code indicates the cause of the error.

In the tag sequence for extended commands, the End Op tag indicates the end of the commanded function and validates the end op code on the DDC byte 1 bus. The end op code indicates successful completion of the commanded function or identifies the cause of an error.

The End Op tag is valid only in control mode.

See the SENSE section for the meanings of the end-op codes.

Device Interface

The device interface connects the controller to the devices. This interface is divided into two parts, control and read/write data. The control part is used in polls, in selection, for communicating commands and responses, and for control and status during read/write operations. The read/write data part carries serial read/write data between the device and the controller and carries the servo clock signal to the controller.

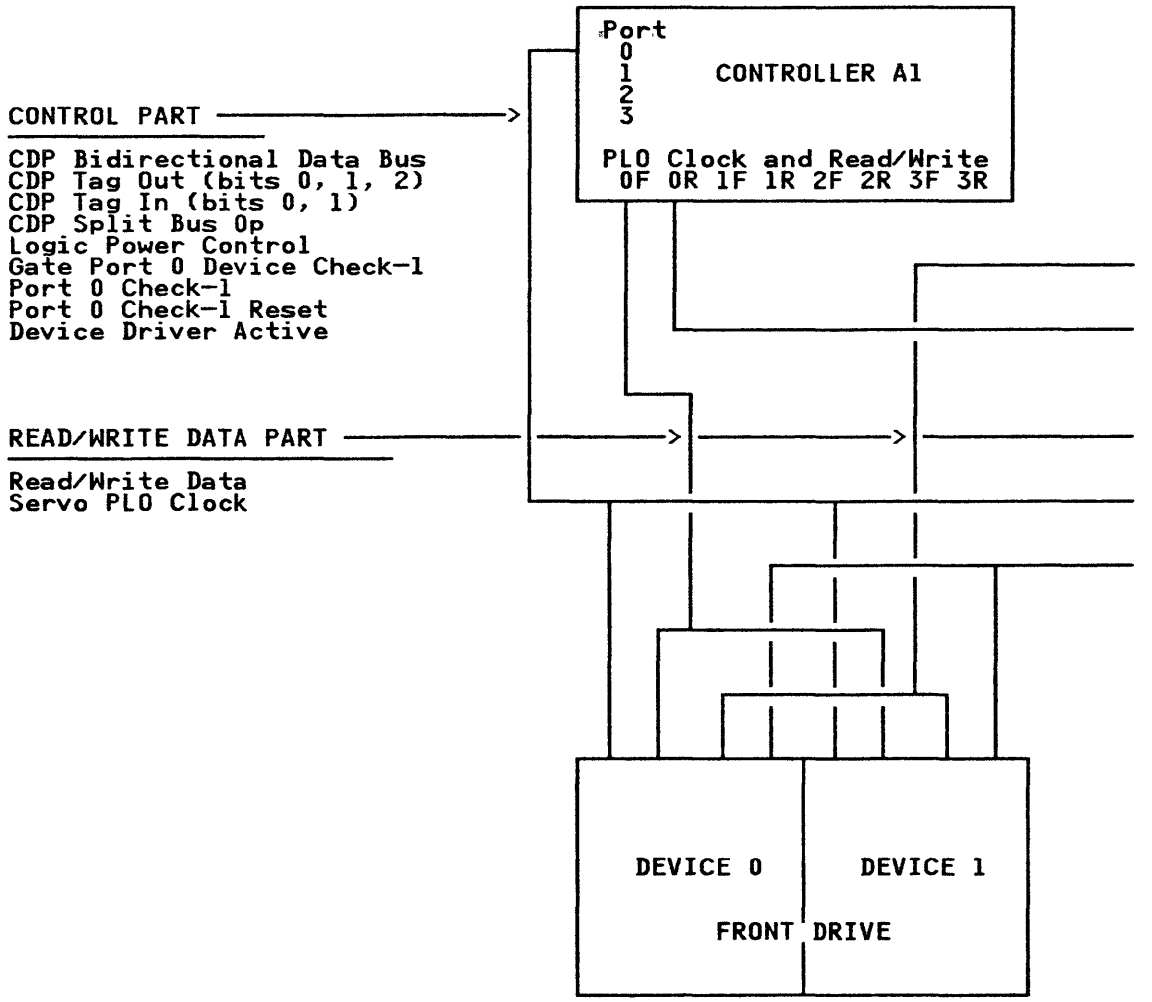
Each controller has four or eight ports (2-Path or 4-Path) for the control part of the device interface. In a full string, each port connects the controller to four devices (two drives). Each controller has a set of these ports, which are not shared by the controllers.

The read/write data part of the device interface has a separate set of signal lines for each drive, and each drive has a set of these lines for each controller. The two devices in a drive share these signal lines to the controllers.

The following table shows the port and the read/write data connection for each device in a string.

Dev	Port	R/W Data Connect	HDA Side	Unit	Config Path
0	0	0 Front	Left	A1/2	2/4
1	0	0 Front	Right	A1/2	2/4
2	0	0 Rear	Left	A1/2	2/4
3	0	0 Rear	Right	A1/2	2/4
4	1	1 Front	Left	1st B	2/4
5	1	1 Front	Right	1st B	2/4
6	1	1 Rear	Left	1st B	2/4
7	1	1 Rear	Right	1st B	2/4
8	2	2 Front	Left	2nd B	2/4
9	2	2 Front	Right	2nd B	2/4
A	2	2 Rear	Left	2nd B	2/4
B	2	2 Rear	Right	2nd B	2/4
C	3	3 Front	Left	3rd B	2/4
D	3	3 Front	Right	3rd B	2/4
E	3	3 Rear	Left	3rd B	2/4
F	3	3 Rear	Right	3rd B	2/4
10	4	4 Front	Left	A3/4	4
11	4	4 Front	Right	A3/4	4
12	4	4 Rear	Left	A3/4	4
13	4	4 Rear	Right	A3/4	4
14	5	5 Front	Left	4th B	4
15	5	5 Front	Right	4th B	4
16	5	5 Rear	Left	4th B	4
17	5	5 Rear	Right	4th B	4
18	6	6 Front	Left	5th B	4
19	6	6 Front	Right	5th B	4
1A	6	6 Rear	Left	5th B	4
1B	6	6 Rear	Right	5th B	4
1C	7	7 Front	Left	6th B	4
1D	7	7 Front	Right	6th B	4
1E	7	7 Rear	Left	6th B	4
1F	7	7 Rear	Right	6th B	4

Figure 4. Device Connections for Port and Read/Write Data



This figure shows the device inter—

Figure 5. Device Connections to Port and Read Write Data

Controller Port Signals

The cable from a controller port to a device carries 20 signals:

- 9 bidirectional signals
- 7 outbound signals
- 4 inbound signals

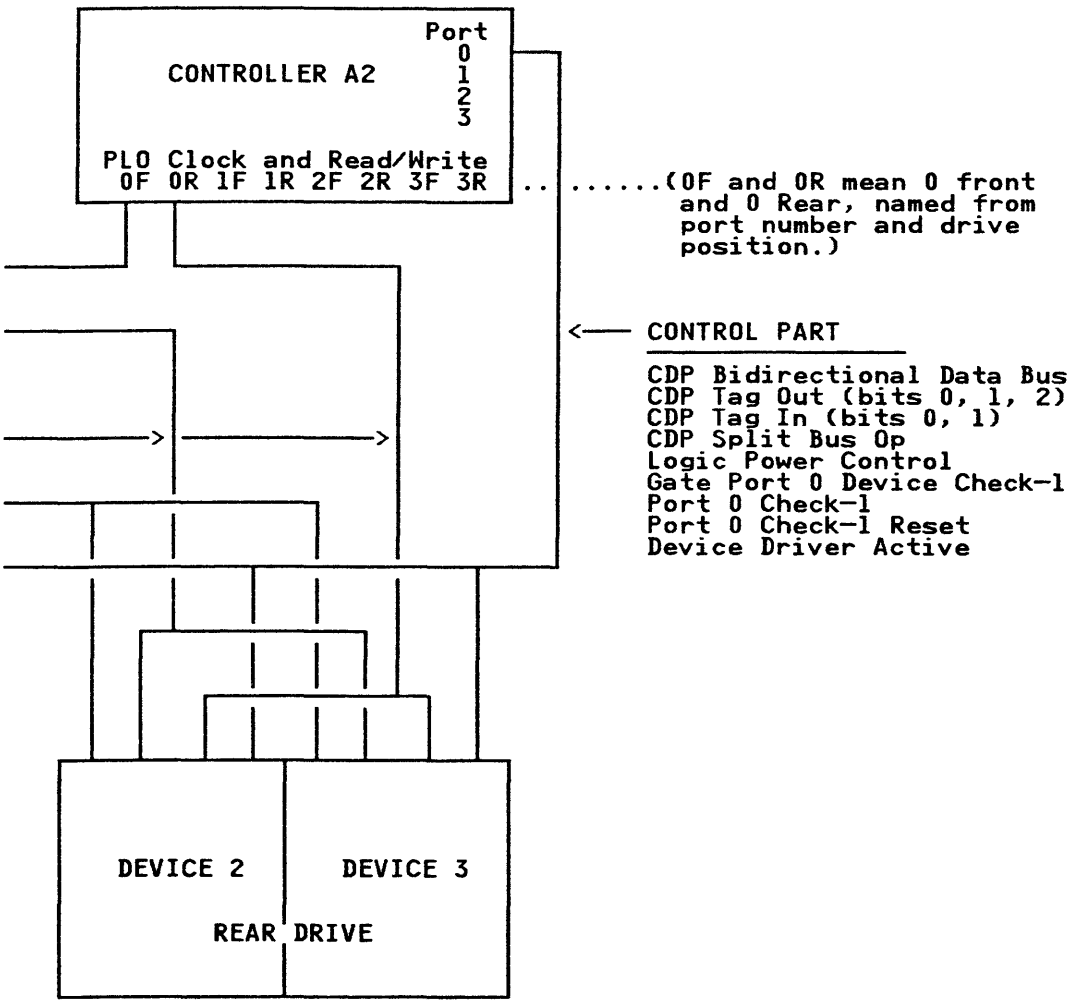
The nine bidirectional signals are the CDP bidirectional data bus, which contains bits 0 through 7 and a parity bit.

The seven outbound signals are:

- CDP tag out (bits 0, 1, and 2)
- CDP split bus op
- Logic power control
- Gate port x device check-1
- Port x check-1 reset

The four inbound signals are:

- CDP tag in (bits 0 and 1)



face for devices 0 through 3. (2-Path)

- Port check-1
- Device driver active

CDP Bidirectional Data Bus

The CDP bidirectional data bus operates in two modes, normal mode, during which all the signals in the bus go in the same direction (either inbound or outbound), and split bus mode, during which the bus is divided so that some signals are inbound and the others are outbound at the same time.

In normal mode, the bus is used to communicate selection addresses, command codes and parameters, and responses to both commands and selection between the controller and the device.

Split bus mode is used while the subsystem is in extended mode (during read/write operations). Split bus mode divides the bus and dedicates bits 0, 1, and 2 for inbound signals to the controller and dedicates bits 3 through 7 for outbound signals for controlling the read/write circuits in the device cards. (The parity bit is not used in split bus mode.)

During polls, the CDP bidirectional data bus operates in a modified normal mode. All signals are inbound from the devices. Each device connected to a port has control of a dedicated line so that the interrupt status of all the devices can be examined by the controller.

CDP Tag Out (Bits 0, 1, and 2)

The status of the three tag out lines combine to define a tag as shown in the following table.

Tags (out)	Tag Out Bits 0 1 2
Null Disconnect	0 0 0
Select or Sync Out	0 0 1
Selected Null	0 1 1
Poll	1 0 0
Command Gate	1 1 1

In CDP tag out sequences, only one tag out bit changes status for a tag change. Valid changes are shown in the following figure.

```
100<—>000<—>001<—>011<—>111
```

The following paragraphs describe the meanings of the tags.

Null Disconnect (000)

The Null Disconnect tag out signals the selected device to disconnect. This is the tag that shows no activity on the port.

Select or Sync Out (001)

The Select tag out validates the select address on the CDP bidirectional data bus during a device selection sequence.

After the device is selected, the tag (Sync Out) validates a parameter on the CDP bidirectional data bus during a command sequence.

The Sync Out tag also is an intermediate step between Select Null and Null Disconnect in a deselection sequence.

Selected Null (011)

The Selected Null tag is the default tag out while the controller and a device are logically connected.

Poll (100)

The Poll tag out requests interrupt status from the devices on the port. Each device has a dedicated line in the CDP bidirectional data bus for reporting an interrupt.

Command Gate (111)

The Command Gate tag out validates a command code on the CDP bidirectional data bus.

CDP Split Bus Op

The 'CDP split bus op' line is activated by the controller while the subsystem is in extended mode (during read/write operations) to put the CDP bidirectional data bus in split bus mode.

While the 'CDP split bus op' line is active, bits 0 through 2 of the CDP bidirectional data bus are dedicated for inbound status from the device, and bits 3 through 7 of the CDP bidirectional data bus are dedicated for outbound control signals to the device.

Bit 0 is used to report index to the controller. See OPER-30 for index information.

Bit 1 is used to report cell boundaries (see OPER-26 for information).

Bit 2 is used to indicate that drive padding is in progress.

Bits 3 through 7 are used for controlling the device read/write functions during read/write operations. See OPER-34 for more information.

Logic Power Control

The 'logic power control' line is activated by the controller to start the power-on sequence in the devices connected to the port. The controller maintains this line active until the controller is powered off.

When the 'logic power control' line is deactivated, the drive starts a power-off sequence.

Gate Port x Device Check-1

The 'gate port x device check-1' line is activated by the controller to enable the devices on the port to return check-1 status. A check-1 from a device indicates that an error that interferes with normal communications between the controller and the device was detected by the device logic.

Port x Check-1 Reset

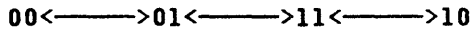
The 'port x check-1 reset' line is activated by the controller to reset check-1 latches in the devices attached to the port.

CDP Tag In (Bits 0 and 1)

The status of the tag-in bits combine to indicate a tag as shown in the following table.

Tags (in)	Tag In Bits 0 1
Null	0 0
Sync In or Valid	0 1
Selected Null	1 1
End Op	1 0

In CDP tag in sequences, only one tag in bit changes status for a tag in change. Valid changes are shown in the following figure.



The following paragraphs describe the meaning of the inbound tags.

Null (00)

The Null tag in indicates that no device on the port is selected and that none of the devices on the port is activating an interrupt status signal during a poll.

Sync In or Valid (01)

The Valid tag validates a response on the CDP bidirectional data bus. Response bytes are sent to the controller by the selected device during some command sequences and during selection.

The Sync In tag acknowledges the receipt of a command or parameter when no response is sent to the controller on the CDP bidirectional data bus.

Selected Null (11)

The Selected Null tag indicates that a device is selected. This tag is the default tag while the device remains selected.

End Op (10)

The End Op tag in is activated by the device to indicate a check-2 error has been detected.

When the CDP bidirectional data bus is in normal mode, an End Op tag is sent to the controller instead of a Sync In or Valid tag during a tag sequence. (The error condition is not reported until a command sequence is in progress.)

When the CDP bidirectional data bus is in split bus mode (during read/write operations), the End Op tag is sent immediately when the check-2 error is detected.

Some of the device check-2 errors are:

- Sequencer checks
- Servo control checks
- RPS (rotational position sensing) checks
- Checkpoint checks
- Read/write checks
- Power checks

Port Check 1

The 'port check-1' line is activated by the device to report an error that affects normal communications on the control part of the device interface. Only the selected device can report a check-1 error.

Device Driver Active

The 'device driver active' line is activated by the device to indicate to the controller that a response (inbound) to a command or to selection is on the CDP bidirectional data bus.

While the 'device driver active' line is active, the CDP data bus drivers in the controller are inhibited.

Read/Write Data and Servo Clock Signals

The connection between a drive and the read/write data port that is dedicated to the drive carries two differential signals, 'read/write data', and 'servo PLO clock'. Separate lines are provided between each controller and each drive. The lines between a controller and a drive are shared by the two devices in the drive. (See the figure on OPER-16.)

During read operations, one pair of lines carries serial read data from the selected device to the selecting controller. During write operations, the same pair of lines carries the serial write data to the selected device.

The 'servo PLO clock' signal from the selected device is on the other pair of lines during both read operations and write operations. The 'servo PLO clock' signal is supplied to the controller for synchronizing the controller clock during write operations.

Controller—to—Controller Connection

The controller-to-controller connection provides paths for communications and control between the two DPS cards in a 3380-J/K A-unit that is being used in a 2-Path configuration to 3380 storage controls. This communication between the DPS cards permits the primary/alternate relationship between those cards during DPS functions.

Line Descriptions

Because both DPS cards are the primary side (at different times), and because data moves in both directions between the DPS cards, most of the lines in the controller-to-controller connection are bidirectional. The exceptions are noted in the line descriptions that follow.

(The lines in this interface are shown on the diagrams for the DPS cards in the LRM.)

- CCC Stg Adr Reg (Bits 0 through 10, P)

This storage address register bus is controlled by the primary DPS card and is used to provide the 11-bit address to the alternate DPS card for array access operations.

- CCC Data (Bits 0 through 7, P)

The data bus is used for transferring data bytes between the primary and alternate DPS cards. The direction of the data depends on the operation. For example, during a copy alternate array command, the data is supplied by the alternate card; and during a write DPS array command, data is received by the alternate card.

- CCC Command (Bits 0, 1, 2, P)

This bus is controlled by the primary DPS card to specify the kind of operation in the alternate DPS card. The operation is encoded on the bus.

- CCC Array Buffer Reset

This line resets the array output latches in the alternate DPS card.

- CCC A1 Control Request and - CCC A2 Control Request

These two lines are activated by the respective DPS cards to request control of the controller-to-controller connection and to establish the primary and alternate relationship between the two DPS cards.

When a DPS card receives a command, it activates its 'control request' line. If the other DPS card is not in an operation, the card that requested control becomes primary. The primary DPS card keeps its request line active until the DPS operation is completed.

- CCC Wait 1, - CCC Wait 2, and - CCC Wait 3

These lines contain the encoded response from the alternate side during array and lock operations.

- CCC Reset A2 Control

This line is used to give control of the controller-to-controller connection (and primary status) to the DPS card with controller 1 when both DPS cards activate their control request lines at the same time.

The '- CCC reset A2 control' line can be activated by either of the DPS cards. Both cards test for the simultaneous activation of the '- CCC A2 control request' and '- CCC A1 control request' lines. If the test in either card indicates a *tie* condition, the '- CCC reset A2 control' line is activated.

+ CCC Array Initialized

The '+ CCC array initialized' line is activated by the alternate DPS card if the array in that card is initialized.

- CCC Error

The '- CCC error' line is activated by the alternate DPS card if an error is detected in that card during a DPS operation.

+ CCC Power Sequence Complete

The '+ CCC power sequence complete' line is activated to indicate that the drives in the string have been powered on. Either DPS card can activate this line.

+ CCC A1 Power On and + CCC A2 Power On

These lines are activated when the respective controllers have logic power. The '+ CCC A1 power on' line is activated from the DPS card with controller A1, and the '+ CCC A2 power on' line is activated from the DPS card with controller A2.

- CCC Clock 1, - CCC Clock 3, and - CCC Clock 3

These three lines are used to validate the data on the CCC data bus during array and lock operations.

Controller Path Control

The controller sequencer microcode, located on the Controller Sequencer card directs the flow of information in the controller during the execution of all immediate controller and extended commands. The microcode is a set of microinstructions that are stored in the Read-Only Storage (32K x 24 bits) modules on the card. These instructions control the register circuits and the bus between the register on both the Controller Sequencer card and the input/output control (IOCC) card.

Basically, the sequencer controls by selecting the source and the destination of information on the register data bus. Selection of both the source and destination are caused by the same microinstruction.

When the microcode is not controlling functions of the controller, such as during dynamic path selection (DPS) commands and device commands, the sequencer executes instructions to monitor status in the controller. (The controller sequencer monitors by performing bit tests on selected bytes) At this time, communication between the storage control and the DPS circuits or the selected device is through the feedthrough paths, which do not use the Register Data Bus.

The process by which the sequencer takes control of the controller functions for immediate controller commands is described in the following paragraphs.

Circuits in the IOCC card are designed to detect a DDC tag out change from a Selected Null (011) state to the Command Gate (111) state. At this time the IOCC card performs a partial decode of the command code on the DDC Bus Out Byte 0 bus. When the command is an immediate command for the controller, the circuits activates the 'controller command' bit in a register that the sequencer can test. The controller sequencer frequently tests the status of the 'controller command' bit while performing the monitor function.

When the microcode detects the 'controller command' bit active, it branches to an instruction that activates the 'seq controls DDC/CDP' register bit. With this bit active, the feedthrough paths are disabled, and the DDC tag in lines, CDP tag out lines, CDP data bus (outbound), and the DDC Bus In Byte 1 bus are all controlled by the controller sequencer through the register data bus.

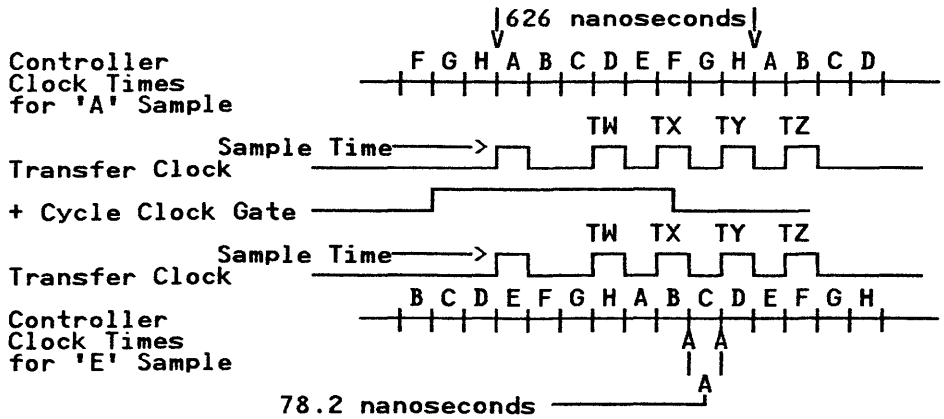
Transfer Clock and Feedthrough Path Control

The transfer clock is used to maintain order during the transfer of information on the feedthrough paths in the controller.

The feedthrough paths permit the exchange of information between the Director-to-Device Controller (DDC) Interface and the Controller-to-Device Port (CDP) Interface during selection sequences and during device command tag sequences. The feedthrough paths are also used to connect the DDC Interface to the Dynamic Path Selection (DPS) circuits during DPS operations. (If installed) During these times, the controller sequencer is monitoring the status of the controller and is not controlling the controller end of the interfaces. However, if an error is detected by circuits in the controller, the controller sequencer microcode takes control to prepare an end-op code, which identifies the error condition, and then controls the tag-in response to the storage control.

The circuits for the transfer clock are contained on the Input/Output Control Card (IOCC). When activated, these circuits generate a cycle of four clock pulses: TW, TX, TY, and TZ. The basic timings for the transfer clock are supplied by the controller clock ring, on the Clock/Serdes/ECC card. (+ System Clock A-H) The duration of the controller clock pulse and the duration of a transfer clock pulse are the same (approximately 78.2 nanoseconds).

A transfer clock cycle starts if the '+ cycle clock gate' signal, an internal only signal on the IOCC card, is active during either of two sample times. (The status of the '+ cycle clock gate' signal is sampled at A-clock time and at E-clock time) The '+ cycle clock gate' signal is activated by changes on the DDC Tag Out lines and by changes on the Tag In lines from the DPS circuits or from the devices.



Tag changes are recognized through the comparison of the status of the tag lines with the status of the corresponding bits in tag registers. The tag registers are updated to the status of the tag lines during the transfer clock cycle that results from the tag change.

After a transfer clock cycle starts (at either A-clock time or E-clock time), the '+ cycle clock gate' signal must remain active until TW-clock time in the transfer clock cycle to continue the cycle. If the signal is inactive between the start of the cycle and the time for the TW clock, the cycle is cancelled. This prevents transient signals and noise from causing transfers on the feedthrough paths.

The feedthrough paths are used during polls, during selection, and during immediate commands. The controls that are needed for the feedthrough paths involve, in addition to the transfer clock signals, a complex relationship of signals in the IOCC card. Most of these are not described in this section, but several of the major signals are described in the following paragraphs.

The 'controller command' signal (internal to the IOCC card) is the output of a latch that is set at TW-clock time in a transfer clock cycle if the tag out on the DDC is Command Gate, the command is an immediate controller command, and the controller is selected. The 'controller command' signal remains active until the latch is reset either by a Null tag out on the DDC or by the sequencer-operation complete bit is activated by the sequencer microcode. This bit is activated at the end of the execution of a controller immediate command.

The 'controller command' signal is tested by the controller sequencer while the microcode is monitoring controller status and is not in control. If the signal is found active, the controller sequencer takes control of controller functions and activates the '+ seq controls DDC/CDP' line (this is also an IOCC internal only signal), which remains active while the sequencer is in control.

The '- DPS command' signal is the output from a latch on the IOCC card and is set by either of two ways. The latch is set at TW-clock time in the transfer clock cycle if the tag out state of the DDC interface is at Command Gate, the tag register indicates that it was at the Selected Null state, the command is a DPS command, and the controller is selected. The latch is also set at TW-clock time during initial selection if the DPS card is present, the controller address part of the selection address is correct, it is not a controller-only selection, the tag out state of the DDC interface is at Select, the tag register indicates that it was at the Null state, and the '+ seq controls DDC/CDP' signal is not active.

The latch that activates the '- DPS command' line is reset by any of the four sets of conditions that follow:

- The DDC tag out lines are at the Null state and the tag register also indicates the Null state.
- The '+ seq controls DDC/CDP' line is active.
- The '+ DPS op complete' signal is active at TZ-clock time. (The '+ DPS op complete' signal is activated by circuits in the DPS card when the DPS function is completed)

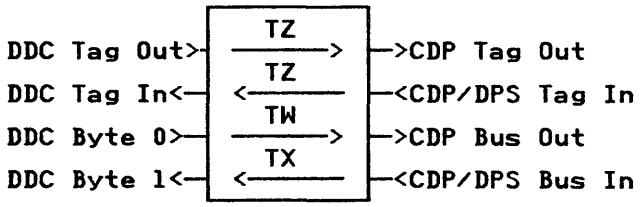
- The tag out state of the DDC interface is at Command Gate, the command is not a DPS command, the controller is selected, and it is TW time in a transfer clock cycle.

While the '- DPS command' line is active, the DPS circuits are enabled, and the feedthrough paths are used to connect the inbound bytes and tags from the DPS circuits to the DDC byte 1 bus and the DDC tag in lines.

When the controller sequencer is not in control (the '+ seq controls DDC/CDP' line is not active) and the '- DPS command' line is not active, the feedthrough paths are available for communications between the storage control and the selected device for device commands.

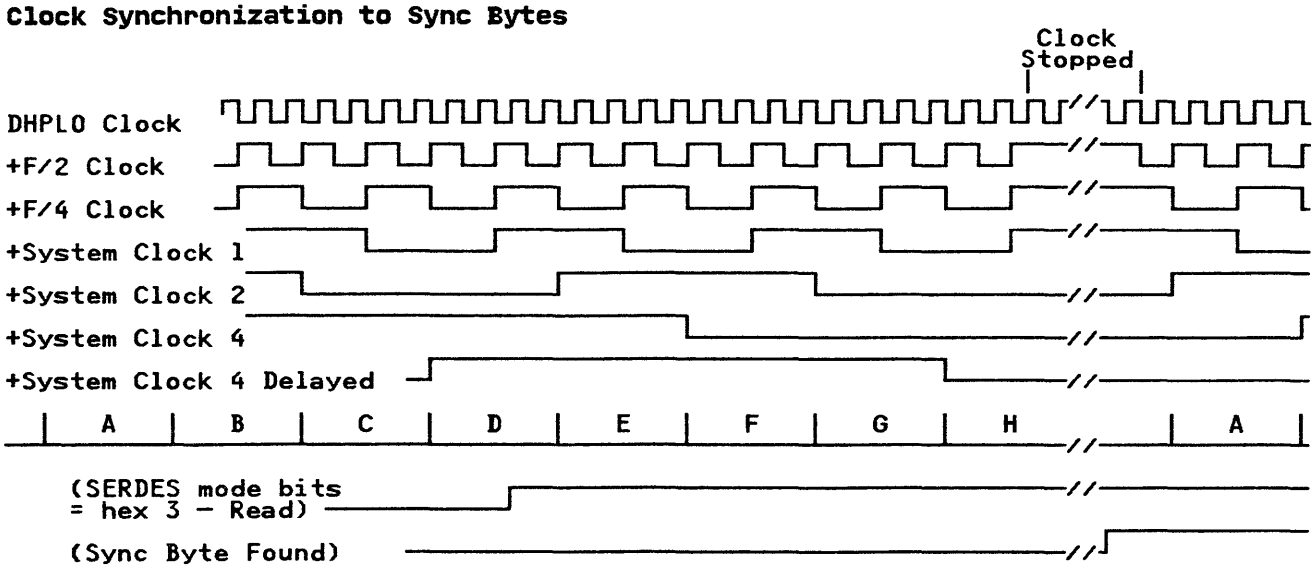
During the tag sequence for device commands from the storage control , the following transfers occur in the feedthrough paths:

- For DDC tag out changes to Command Gate, the byte on the DDC byte 0 bus transfers to the CDP data bus (outbound) at TW time, and the DDC tag out transfers to the CDP tag out at TZ time.
- For DDC tag out changes to Selected Null, the DDC tag out transfers to the CDP tag out at TZ time.
- For DDC tag out changes to Sync Out, the byte on the DDC byte 0 bus transfers to the CDP data bus (outbound) at TW time, and the DDC tag out transfers to the CDP tag out at TZ time.
- For CDP tag in changes to Valid or Sync In, the byte on the CDP data bus transfers to the DDC byte 1 bus at TW time, and the CDP tag in transfers to the DDC tag in at TY time.
- For CDP tag in changes to Selected Null, the CDP tag in transfers to the DDC tag in at TY time.



Controller Clock

Clock Synchronization to Sync Bytes



Clock Sync to Sync Byte

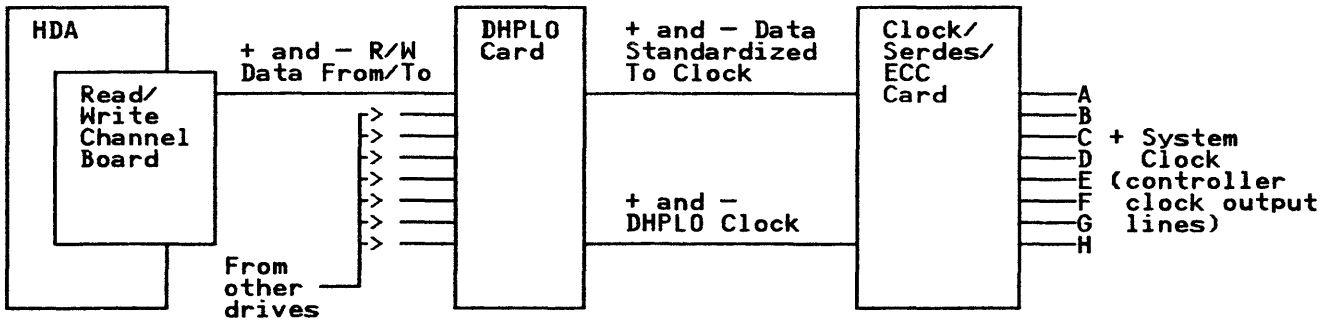


Figure 6. Schematic for Clock Synchronization to Sync Bytes

The controller clock is based on frequency division of the data-handling phase-locked oscillator (DHPLO) clock signal.

The DHPLO clock operates in three modes: asynchronous, synchronized to read data, and synchronized to servo phase-locked oscillator. Both synchronous modes synchronize the DHPLO clock to the speed of the disk.

The frequency of the DHPLO clock is approximately 48 MHz in all three modes. Selection of the modes of operation is controlled by the controller sequencer. During write operations, the DHPLO clock is synchronized to the servo phase-locked oscillator, which is synchronized to the signal from the servo surface. While data is being read, the DHPLO clock is synchronized to the data read by the selected read/write head.

Each of the eight steps (A through H) in the controller clock ring contains four DHPLO clock cycles. (The duration of each step is approximately 83.3 nanoseconds. The period of a complete ring is approximately 666.6 nanoseconds.)

For read/write operations, the clock ring is synchronized to events. To synchronize the clock ring to an event, the controller sequencer activates signals to stop the clock ring. The ring stops only during H-clock time and remains in H-clock time until the ring is restarted.

To synchronize the clock ring for read operations, the clock is restarted by sync bytes. To synchronize the clock ring for write operations, the clock ring is restarted at the cell boundary.

While waiting for sync bytes to be recognized, the clock ring also starts if the ring was stopped for 2 leading edge of cell pulses.

The clock ring also starts if a clock check is recognized or if either the '-extended pwr on reset/index' or '-trap check-1' input lines to the Clock/Serdes/ECC card is active.

Clock Sync to Cell Boundary

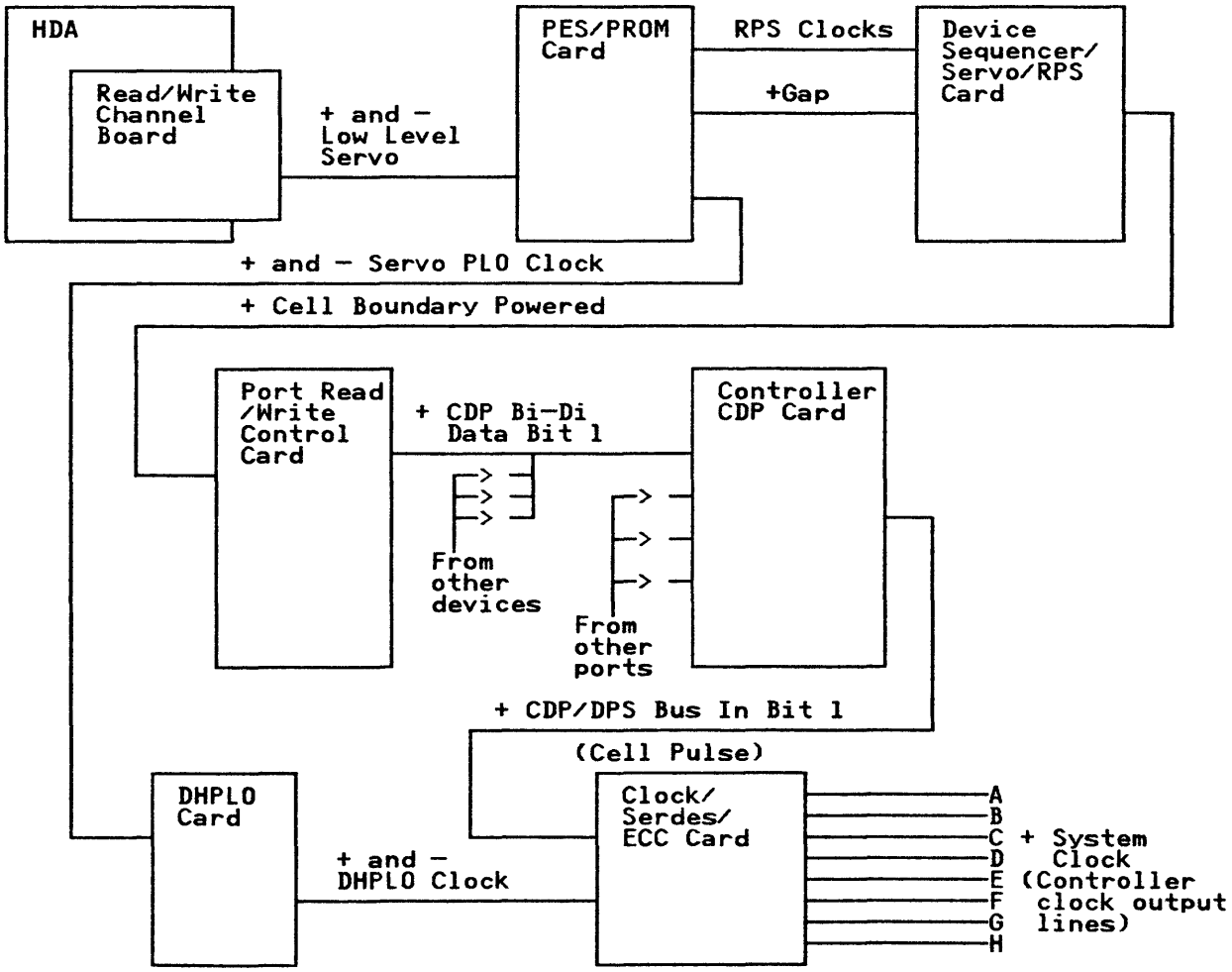
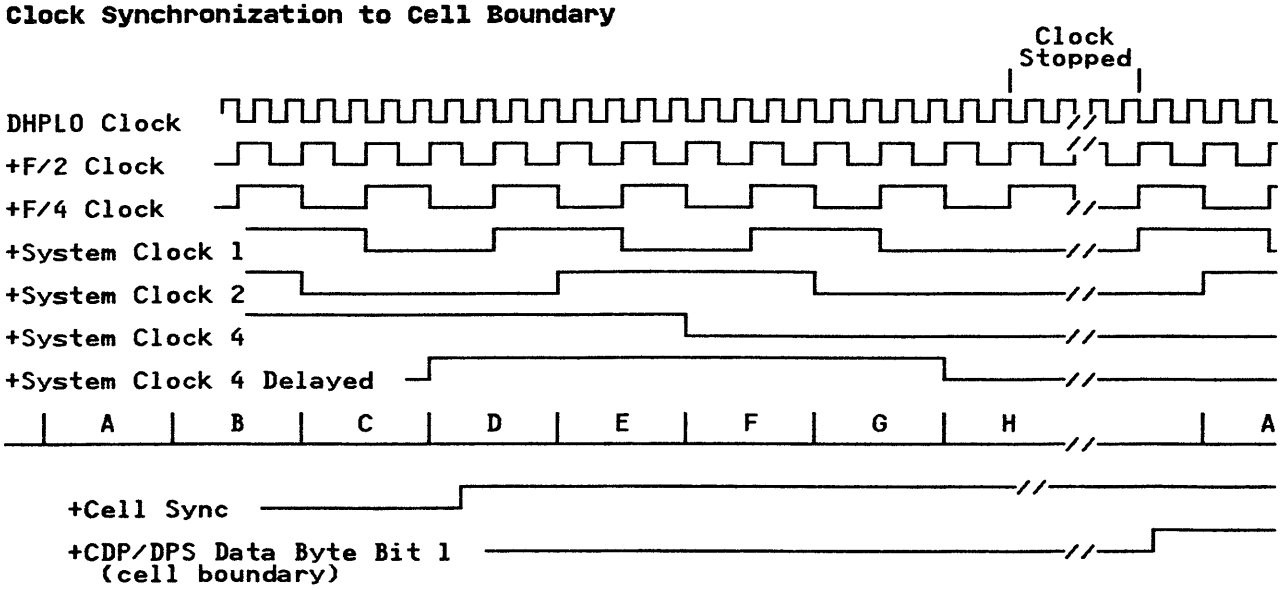


Figure 7. Schematic for Clock Synchronization to a Cell Boundary

Clock Synchronization to Cell Boundary



The system clock (controller clock) is synchronized to the sync byte pattern to align the controller sequencer and the circuits that move read data with the start of data. The sync byte pattern immediately precedes data.

To synchronize the clock to the sync byte pattern, the controller sequencer sets the ECC mode control bits and the SERDES mode bits to hex 2 and hex 3 respectively, which stops the clock ring during H-clock time. The clock ring remains stopped (normally) until the sync byte pattern is recognized in the encoded serial data read from the disk.

This page shows the path for read data, which is analyzed by the sync-byte-found circuits and is also used as the frequency reference for the data-handling phase-locked oscillator (DHPLO) while data is read. The system clock (controller clock) is synchronized to a cell boundary as a part of achieving orientation after index is detected.

To synchronize the clock to a cell boundary, the controller stops the clock ring by activating the '+ cell sync' line, which stops the ring during H-clock time. The clock ring starts again at the next cell boundary.

This page shows the paths for the signal that starts the clock ring and the paths for the signals used to synchronize the data-handling phase-locked oscillator (DHPLO). The DHPLO is synchronized to the 'servo PLO clock' signals from the selected device during clock synchronization to cell boundaries and during write operations.

While the DHPLO is synchronized to the 'servo PLO clock' signals, the '- lock PLO to servo' line, which is controlled by the controller sequencer, is active.

The Device

The ultimate job of the device is to store data and produce it upon request. The device accomplishes its ultimate job by storing customer data on ferrous oxide coated disks, using magnetic heads. The device consists of the following:

- Device Logic
- Device Sequencer Microcode
- Head Disk Assembly (HDA)
- Power Supplies

With the exception of the device power supplies, the above parts of the device will be explained in the following pages. For information on the device power supplies see the PWR (power) section of the Maintenance Information Manual (MIM).

Device Logic

The device logic contains all the device and drive circuitry. This circuitry is located on logic cards installed in the 'B' board. The exceptions are the Power Amplifier card and the R/W Channel Board. The following is a list of device logic cards:

- Sequencer/Servo/RPS
- Port R/W Control
- PES/PROM
- Common Power
- Power Amplifier
- R/W Channel Board

Sequencer/Servo/RPS card

The device Sequecer/Servo/RPS card contains the following:

The Device Sequencer

The device sequencer is a microprocessor, with a limited arithmetic and logic unit, whose function is to monitor and control the operations of the device. The instructions (the device sequencer microcode), for the sequencer, are contained in Erasable Programmable Read Only Memory (EPROM) modules. These memory modules are located on the PES/PROM card. All decisions for the sequencer have been designed in advance.

To accomplish the control part of its job, the device sequencer issues commands to the servo system, the port and the common power circuits. This is done by activating bits on a bus or in an output register, followed by the activation of a control line. The receiving part of the device (example: common power card) acts upon the active bits when the proper control line is active.

The monitoring part of the device sequencer's job is done by sensing the contents of its input registers at predetermined times. Selected signals, from various parts of the device, control contents of these registers. The active or inactive bits in the registers determines the next sequencer instruction.

Both the controling and the monitoring of the device is done under the total control of the device sequencer microcode. For more information see "Device Sequencer Microcode" on page OPER-38.

The Digital Servo System (Digital Control Processor)

The Digital Servo System consists of the Digital Control Processor (DCP), a ten Mhz oscillator, 2K (by 27 bits wide) of Random Access Memory (RAM), the Analog Conversion Circuits (ACC) and the Position Error Sensing (PES) circuits. The PES circuits (PES/PROM card) are the only circuits that are not located on the Sequencer/Servo/RPS card. The DCP is the microprocessor that controls the servomechanism through the Power Amplifier via the ACC circuits. The DCP's function is to position the actuator in response to commands received from the device sequencer.

The device sequencer issues the servo commands, with their parameters, in response to device commands received from the storage control. The

command and its parameters are loaded in the Servo Command Register, which is located in the sequencer. Using the contents of this register, the DCP calculates the required control output (digital) to move the access mechanism to the desired position. These digital signals are converted to an analog signal by the Analog Conversion Circuits (ACC). The analog signal is then applied to the Power Amplifier which drives the Voice Coil Motor (VCM).

Feedback from the HDA is in the form of the two PES signals from the PES/PROM card (PES P and PES Q). These Position Error Signals provide the DCP with a way to keep track of where the heads are located. The ACC circuits are used to digitize the PES signals for the DCP.

The DCP returns status, to the sequencer, by loading three status registers every 112 microseconds. These registers are named Servo Status 0, 1 and 2, and are located in the sequencer. This memory is accessible to both the sequencer and the DCP.

To become operational, the DCP has to go through an Initial Microcode Load (IML), that is controlled by the device sequencer. The sequencer first IMLs the DCP with BAT (Basic Assurance Test) code and commands the DCP to execute this BAT. After successful completion of the BAT, the sequencer will IML the DCP with functional servo code. The IML code for both models (J and K) is located in the Erasable Programmable Read Only Memory (EPROM), on the PES/PROM card. The device sequencer senses the HDA ID signals, from the HDA, to determine which code load to use. Once the correct load is determined, the DCP is IML'ed across the ROS Out (0 to 23) bus from the PES/PROM card. When the device sequencer microcode has determined that the IML has been successful, it will issue the necessary commands to start the DCP. The failure of any one of the following:

1. Any IML process
2. The BAT
3. A successful start of the functional code

results in the sequencer aborting the operation in process, reporting an interrupt with a device check-2 condition and posting an appropriate Check Point Check. The DCP is IML'ed during a power on operation and before every Rezero operation.

The Rotational Position Sensing (RPS) Circuits

The Rotational position sensing (RPS) circuits on the Sequencer/Servo/RPS card perform the following function:

- Identifying the start and end of tracks (Index)
- Generates cell boundaries
- Reporting when the disks have reached the position specified in a Sector Search command

The index signal identifies the start and end of tracks. This is one of the two events that can lead to orientation. The recognition of index time and the generation of the index signal are described on OPER-30.

The '+ cell boundary powered' signal, is generated by the RPS circuits from the '+ gap' and 'RPS clocks' signals. These signals are created by the PES/PROM card from the digital information stored in the 'gaps' on the servo surface. See Servo Surface on page OPER-49 for more information. The '+ cell boundary powered' signal, as its name implies, indicates cell boundaries. The signal is synchronized to the speed of the disks and alternates polarity every 5.3 microseconds (approximately). The change from inactive to active on the '+ cell boundary powered' signal indicates the cell boundaries. (Thus, the time between cell boundaries is approximately 10.6 microseconds) Cell boundaries are also part of the orientation process.

The '+ record ready interrupt' signal, from the RPS circuits, is part of the process for reporting that the disks have reached a specified position. This RPS function is described on this page, but because it is more easily understood when the reason for the function is understood, the reason is explained first.

The Sector Search command permits the storage control to specify a rotational position (relative to index) such that, when the specified position on the disks is at the read/write heads, an interrupt signal is generated in the device.

The interrupt signal has to occur in advance of a desired record so that the storage control has time to collect the interrupt status during a poll, select the device, determine the cause of the interrupt, send a Start Read/Write command to go into extended mode, and get oriented before the desired record reaches the read/write heads.

The way that a rotational position is specified is with a sector number, which is calculated by the storage control.

The disks are radially divided into 222 sectors. There are no sector marks or IDs on the disks. The sector boundaries are determined by the contents of counters in the device Sequencer/Servo/RPS card that are locked to Index. Each sector contains seven cells. Sector 0 contains cells 0 through 6. One is added to the sector counter at the end of cell 6, and the next seven cells (7 through 13) are included in sector 1.

This process continues until the sector counter contains 221 (decimal), which is the sector counter's contents while cells 1547 through 1553 pass under the read/write heads.

The sector counter is used for only two purposes. It is used to determine when index is expected (as a part of error checking). The contents of the sector counter are also compared with the contents of the target register, which is loaded with the number of the sector in which an interrupt is wanted by the storage control.

When the contents of the sector counter and the target register are the same, the '+ record ready interrupt' signal is activated. This signal remains active for two full sectors, or for approximately 148.4 microseconds.

The 'record ready interrupt' signal is sent to the Port R/W Control card, where it sets bit 7 in the device status 1 register. The signal also arms the interrupt circuits on the port card. When the next poll is received the Port R/W Control card will activate its device identifier bit. The storage control will then address the device and issue a sense device status 1 command, causing bit 7 to be detected active.

Index Detection

Index identifies the start and end of tracks. The recognition of index is based on a decode of the bit sequence from the digital part of the signal read from the servo surface.

The '- gap' signal from the PES/PROM card carries the serial digital information to the shift register and decoding circuits on the Sequencer/Servo/RPS card. When the shift register contains hex FAD, which occurs only once each revolution of the disk, the decoder circuits recognize the index. Index occurs approximately 2.6 microseconds into cell 1553.

Counters in the device Sequencer/Servo/RPS card are used to validate index. One of the counters counts clock pulses. (Two of these pulses occur during each cell). The counter counts to 13 and resets to zero. With each reset, 1 is added to another counter. This counter counts sectors, which contain seven cells. (The disk is divided into 222 sectors). When the clock pulse counter contents is 13 (decimal) and the sector counter contents is 221 (decimal), index is expected. When the decoder circuits recognize index while index is expected, the '+ index 1 powered' and '+ index 2' signals are activated. These signals remain active for approximately 21.2 microseconds. The two index signals are sent to the Port R/W Control card.

While the 'CDP split bus op' line (in the device interface) is active, the Port R/W Control card gates the index signal on bit 0 of the CDP bidirectional data bus, to the controller CDP card.

On the CDP card, bit 0 is used to control bit 0 of the CDP/DPS Bus In bus to the IOCC card. On the IOCC card it is gated into a sequencer register. The controller sequencer microcode reads the contents of this register across the Register Data Bus. When index (bit 0) is detected active, the microcode branches. One of the instructions prepares an end op code that is sent to the storage control indicating that an index has been detected.

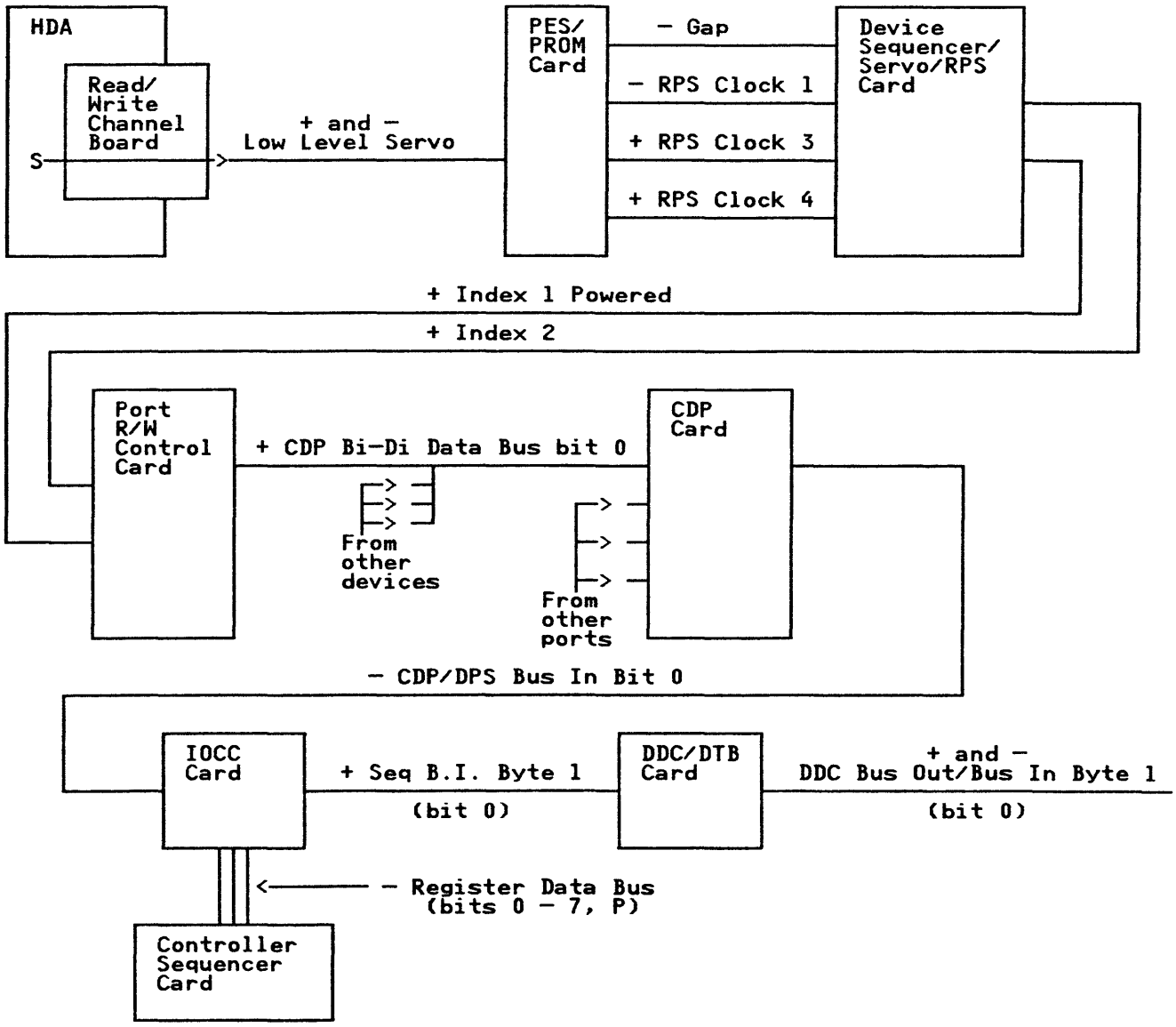


Figure 8. Index Detection

Port R/W Control card

The Port R/W Control card contains circuitry for two functions that have been on separate logic cards in the previous models of the 3380. The port control and the read/write control functions are explained in the following paragraphs.

The port control function provides the following to the device:

- Four independent Controller-Device-Port (CDP) communications paths, one for each controller.
- Proper device selection (device selection is determined by plug location)
- Checking and reporting circuitry, to insure that an error is reported when more then one controller attempts to select the device at the same time.
- Circuitry that will reset the selection circuits when the special command of unconditional selection is received.

- Interrupt circuits for device interrupts, device check-1's and device check-2's.

- Processes most 5X, 74 and 75 status sense commands by activating gate signals to the other parts of the device and sending the resulting status bytes to the controller.

- Enables command handling by gating the command, its parameters and the activation of the command signal to the device sequencer.

- Device check-1 detection and reporting circuitry. (Clock check is detected by the Common Power card and reported to the port circuitry)

- Device check-1 reset circuitry.

- All Path-Interrupt-Table circuitry.

- Sends the Index signal, Cell signal and Padding mode signals to the controller when the CDP interface is in split bus mode.

- Activates the customer ready light if the device is on line and none of the following conditions exists:

    1. An active port check-1
    2. An active clock check-1
    3. An active device check-2
    4. Servo inhibit is active
    5. Write inhibit is active

The primary function of the read/write control logic is to provide the controller, that selected the device, a way to communicate with the R/W Channel Board. Using signals coming across the CDP interface from the controller and information within the device, the read/write control logic is able to raise the signals to R/W Channel Board that will cause either a read or a write operation. For more information on the relationship between the CDP interface, R/W Channel Board and the read/write control logic see "Read/Write Channel Board" on page OPER-34.

While doing its primary function, the read/write control logic also provides error detection, collection and reporting. Most of the error detection circuitry is active all the time, but its primary job is to detect read/write failures during read/write operations. Error collection and reporting is done through the four R/W status registers.

The Port R/W Control card also contains circuits that generate the signals to continue write controls to the R/W Channel board for drive padding after the end of control through the CDP data bus. This is a combined operation for both the port function and the read/write control function within the card. Device padding is initiated, by the controller sequencer, if an End Read/Write command is received, from the storage control, before the end of the track is detected, during a format write. Format write require pads to be written from the end of data until the index (end of track). The pad control and pad write sequence circuits in the Port R/W Control card are activated when the controller sequencer activates the CDP bus bit 3, (set padding) while the '- write gate' lines are active. The Port R/W Control card circuits retain control of the R/W Channel board until the next index is detected.

PES/PROM card

The PES/PROM card consists of the Position Error Sensing (PES) circuits, (part of the servo system) the Erasable Programmable Read Only Memory (EPROM - used by the device sequencer) and the device's under voltage detection circuits.

The device sequencer microcode and the Digital Control Processor (DCP) microcode (for all models) is stored in the EPROM memory. The device sequencer addresses this memory using the '+ SAR 0-7' lines and the '+ ISAR 0-7' lines. The PES/PROM card, using the storage address register lines, gates the data out of memory, over the '+ ROS out 0-23' lines.

The PES circuits are used to amplify and demodulate the burst servo signal from the servo surface in the HDA. ('+ and - Low Level Servo' lines) Demodulating the burst signal provides the servo system with the following:

- The Primary and Quadrature Position Error signals ('+ PES P and + PES Q) for servo position control.

    The relationship between the 'PES P' and 'PES Q' signals identifies, to the DCP, the position of

the servomechanism relative to the four track types. (see OPER-49 for more information) When the servomechanism is solidly in one position, both signals are at some constant DC value. When the mechanism moves the servo head over the servo surface, both signals change. The amount of change is relative to the movement. The DCP, in the Sequencer/Servo/RPS card, uses these signals to determine the location of the servomechanism during a seek. (how many cylinders have been crossed) The DCP's track following circuits also use these signals to determine when the mechanism is track following.

- The write reference clock for data writing synchronization.

  The '+ and - Low Level Servo' signals also supply drive for the clock circuits in the PES/PROM card. The clock circuits generate a servo clock signal that is sent to the oscillator in the controller DHPLO card. The frequency of the servo clock, approximately 12 MHz, is locked to the speed of the disk. This is the clock that is used to serialize the data from the storage control during a write operation.

- Generates a signal for quick off track detection.

  The PES/PROM card monitors the Position Error Signals (PES P and Q) to provide the '- Burst Write Inhibit' signal to the Digital Control Processor (DCP) and the internal PES circuits. The DCP has circuits that are monitoring the position of the servomechanism also, but its detection circuits can not work as fast as the burst inhibit circuits.

- Provides the 'Gap' and 'RPS Clock' signals for cell generation, index and guard band detection.

  These signals are provided to the Sequencer/Servo/RPS card. See "The Rotational Position Sensing (RPS) Circuits" on page OPER-29 for more information.

The PES/PROM card also provides under-voltage detection for the device. These under-voltage detection circuits monitor the + 5VDC, - 5VDC, + 15VDC and - 15VDC power supplies. For more information on how the under voltage condition is reported see OPER-119.

The PES/PROM card activates the '- Power Amp Inhibit' signal and the '- Power Amp Inhibit TTL' signal when it detects an under voltage condition. The TTL signal sets bit 1 in the Device Status 2 register, (Servo Inhibit bit) on the Port R/W Control card. This signal is also used to notify the DCP and device sequencer that there is a problem. The '- Power Amp Inhibit' signal, as its name implies, inhibits the Power Amplification card from driving the servomechanism.

Common Power card

The Common Power card should be called a drive card instead of a device card. Some of the circuits on this card are shared between both devices on the same drive. The following is a list of functions that is provided by this card:

1. Controls the initial power on (shared)

   The Common Power card controls power on reset (multi signals) to both devices. Starts the clocks 8 milliseconds after power on and drops the power on reset signals 2 milliseconds later.

2. Supplies the device clocks (shared) '+ A-H Clock' signals

3. Provides drive relay control (shared)

   The Common Power card controls the picking and dropping of the drive motor relay, the soft-start relay (MSA) and the brake relay.

4. Provides relay position sensing, either picked or dropped (shared)

5. Provides switch position sensing, either on or off

   The drive motor switch sensing is the only switch that is shared between devices, the other switch (disable) is device dependent.

6. Provides error checking and reporting for the following failures:

   a. Internal clock circuitry failure (shared)

b. Detects a 'no air flow' condition (shared)

c. Detects a 'motor thermal' condition (shared)

d. Checks that the power amp cable is plugged correctly (shared)

e. Parity checks the '+ sequencer write bus' lines for both devices

The Common Power card requires both device sequencers to activate their release brake bit, which is the first step of drive motor power on sequence. Therefore, both sequencers must be functional to power on the drive motor.

To control the drive motor power on sequence, both device sequencers activate bits in their power register (located on the Common Power card) for each step. The device sequencer activates the desired bits on the '+ sequencer write bus' lines and then brings up the '+ load power control reg' signal to set the bits into its power register. As the relays are picked and dropped during the sequence, their state is reported to the Sequencer/Servo/RPS card (both devices) by activating and deactivating signal lines. (example: '+ sense soft-start latch' signal is active when the MSA relay is picked)

Power Amplifier card

The Power Amplifier card converts the '+ and - power amp drive' signals from the Sequencer/Servo/RPS card to drive the servomechanism in the desired direction and the desired speed. The desired direction and speed is determined by the Digital Control Process (DCP), which activates the power amp signals through the Analog Conversion Circuits (ACC). The Power Amp card reports back the amount of current and voltage that is being applied to the DCP, by activating the following analog signals: '+ VCM current signal' and '+ VCM voltage signal'.

Read/Write Channel Board

The Read/Write Channel Board, during either a read or write operation controls the head circuitry that is doing the operation.

During a read, the R/W Channel Board accepts the data signal from the Arm Electronics (AE) circuits. The data signal passes through a select amplifier, which amplifies and filters the signal from only the select head. After going through an AGC (Automatic Gain Circuit) circuit, the data signal is converted to a digital signal and sent to the DHPLO card in the selecting controller.

During a write operation, the R/W Channel Board receives pulse data from the Clock/Serdes/ECC card in the controller. The frequency of the data is then divided by two and sent to the selected AE circuitry. During either a read or write operation the Read/Write Channel Board does the following:

1. Decodes the HAR bits (Head Address Register) for arm and head selection.
2. Provides parity checking for the HAR bits received from the Port R/W Control card.
3. Checks the sequence validity of the control lines received from the Port R/W Control card.
4. Provides internal circuitry checking for the channel board and the Arm Electronics circuits.
5. Reports not only errors but its status to the Port R/W Control card.

The controller sequencer, through the CDP interface, supplies the signals that control the selected Read/Write Channel Board during all read and write operations. These signals are the outbound lines of the + CDP Bi-Di Data bus, (bits 3 through 7) when the bus is in split bus mode. The CDP interface is in split bus mode when the '+ CDP split bus op' signal is activated from the controller. In split bus mode, bits 0 through 2 of the CDP interface are dedicated as inbound signals from the selected device.

The following is a list of the outbound bits (3 through 7) and their definitions during read/write operations:

CDP BIT	MEANING DURING READ	MEANING DURING WRITE
3	Not Used	Set Padding
4	Not Used	Safety Inhibit
5	Read Mode Enable	Write Select
6	Not Used	Write Gate
7	AM Search Enable	Safety Inhibit

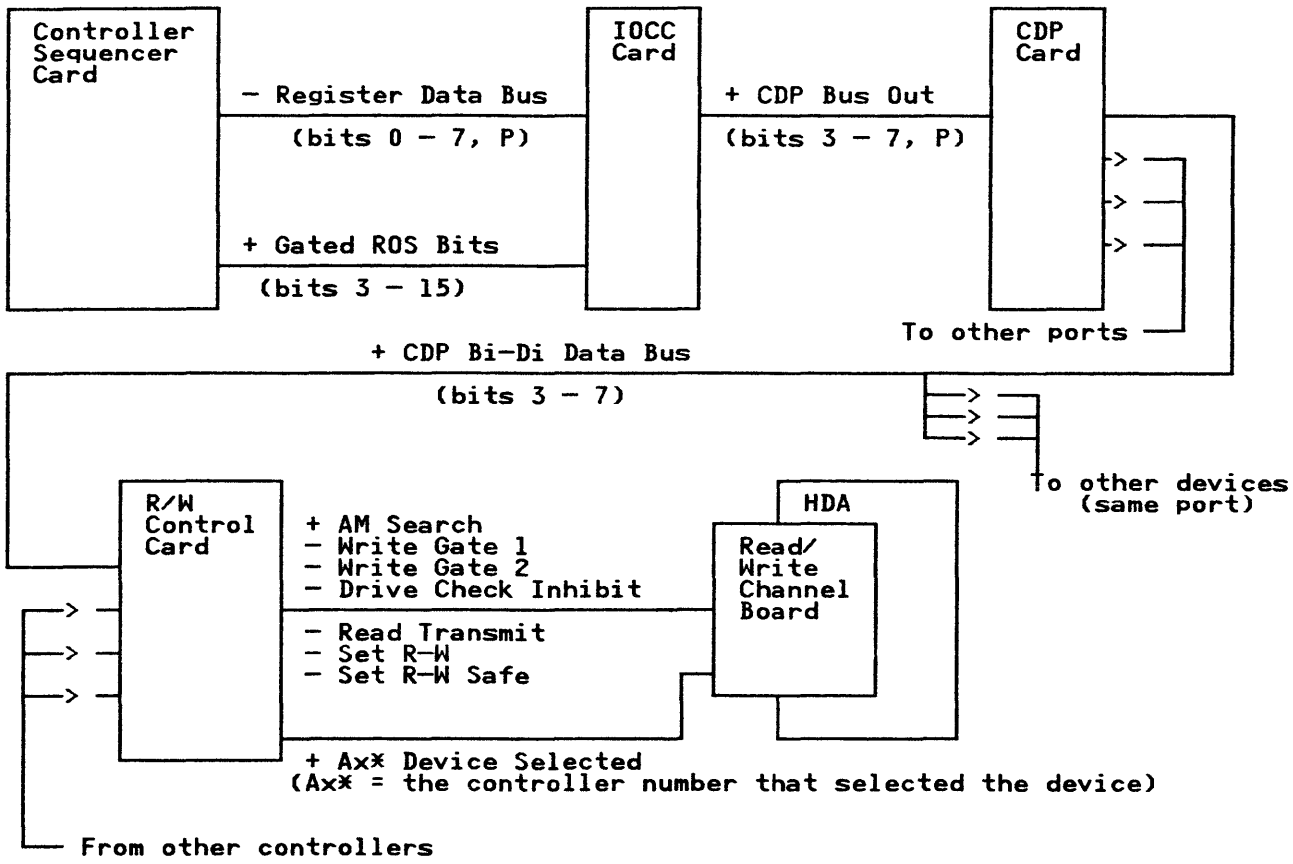


Figure 9. Read/Write Channel Board Controls

For the Read/Write channel board, the source of write data and the destination for read data (which controller) is determined by the status of the '+ Ax device selected' signals from the Port R/W Control card. (x = controller number) There are four signals, one for each controller. The active signal designates which controller selected the device and which R/W PLO cable the R/W Channel Board will use.

Circuits in the Port R/W Control card decode the CDP data bus bits and activate the read/write control lines to the R/W Channel board. (The read/write control lines to the R/W Channel board are immediately deactivated if any error is recognized) The following figures show the relationship between the CDP data bus bits and the read/write control lines to the R/W Channel board, during both a read and a write operation.

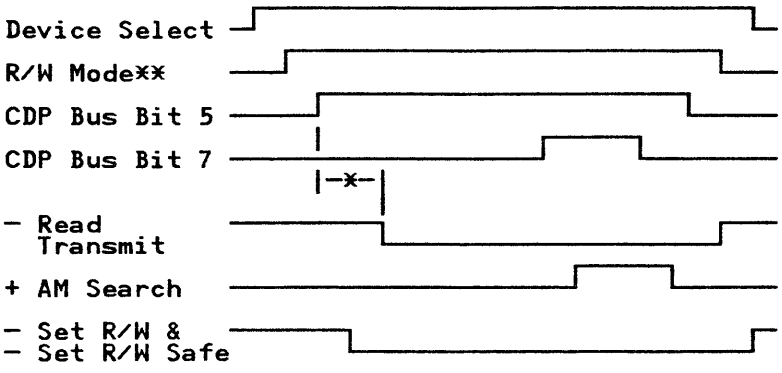


Figure 10. Read Timing Chart

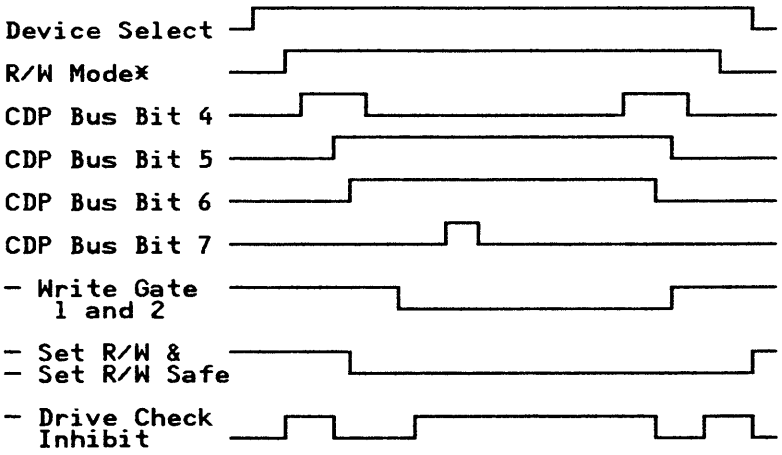


Figure 11. Write Timing Chart

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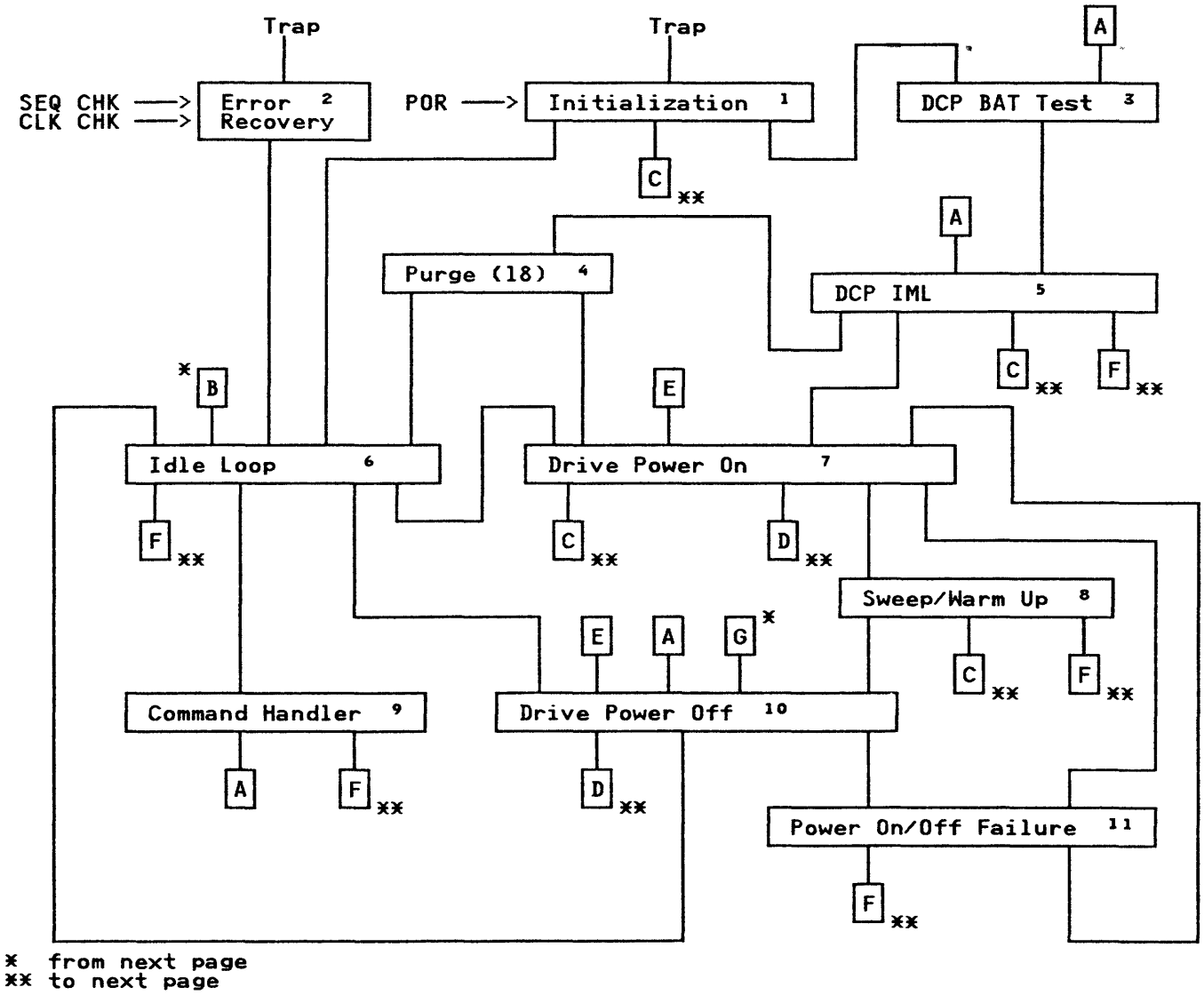

Figure 12. Device Sequencer Microcode Flow (cont. on next page)

Device Sequencer Microcode

The device sequencer (see OPER-28) executes instructions in microcode to command and monitor the digital servo system and drive-motor power-on and power-off sequences. The microcode is located in the Erasable Programmable Read Only Memory (EPROM) on the PES/PROM card. The memory is addressed using SAR and ISAR bus and the microcode is read out to the device sequencer (Sequencer/Servo/RPS card) across the ROS Out bus.

The device sequencer microcode is organized into modules that are named by the functions that are performed by the routines contained within the modules. The modules and the module-to-module flow of the device sequencer microcode are shown in the figures on pages OPER-38 and OPER-39.

The initialization module **[1]** is entered through an address trap. This trap address is the microcode address that the device sequencer is forced to by a Power-On Reset (POR). The routines within the initialization module do the following:

1. Initialize the device sequencer's registers
2. Reset all device check-2 latches
3. Set the busy latch for the device

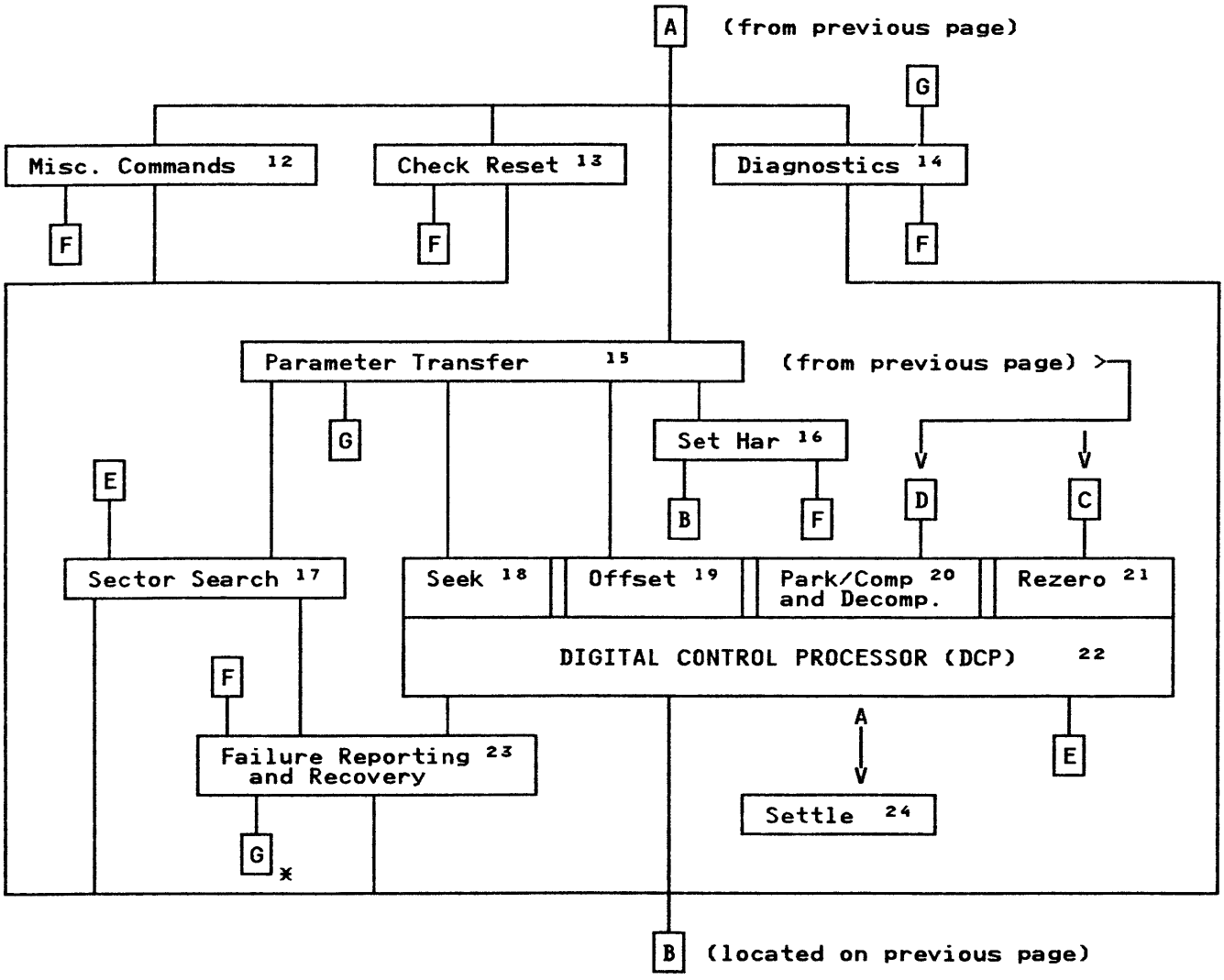

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Figure 13. Device Sequencer Microcode Flow (cont. from previous page)

4. The device sequencer tests the status of the drive motor. If the drive motor is running, the device sequencer branches to the Rezero module **[21]**. If the drive motor is not running, the device sequencer branches to the DCP BAT test module **[3]**.

The error recovery module **[2]** is entered by a trap address. This entry address is forced when a device sequencer check or a clock check occurs. During the execution of this module, the device sequencer attempts to initiate an interrupt to compensate for a missing interrupt. (The condition used to cause the interrupt is a seek incomplete) After setting seek incomplete, the sequencer initializes registers, activates servo inhibit and then branches to the idle loop module **[6]**.

The Digital Control Processor (DCP) Bat test module **[3]**, is entered from either the initialization module (after a POR) or from the command handler module **[9]**, where a rezero command (4C) had to be received. The storage control issues a rezero command after it has collected all sense data for a device check-2 or check-1 failure and after it has issued a reset device check command.

The Basic Assurance Test (BAT), as its name implies, is a basic test of the DCP internal circuitry and memory. When this test fails, the device sequencer reports the failure and continues on to the DCP IML.

In the purge module**[4]**, the device sequencer goes into a timer loop for 18 seconds, this is to permit the air system to clean the HDA. During the 18 seconds, the sequencer tests the status of the drive motor switch. If the drive motor switch is turned off and remains off until the end of the purge cycle, the devices sequencer resets the busy latch and branches to the idle loop module **[6]**. If the switch remains on throughout the cycle, the sequencer branches to the drive power on module **[7]**.

The Digital Control Processor (DCP) Initial Microcode Load (IML) module **[5]** is used to load the microcode that the DCP uses to do its job (control the servo system). The entry to this module is either from the DCP Bat module or from the command handler module after it has received a drive power on command (40). The device sequencer exits from this module to the following:

1. Successful load after initialization - Exit purge module **[4]**.
2. Successful load after receiving a drive power on command - Exit drive power on module **[7]**.
3. Successful load after receiving a rezero command - Exit rezero module **[21]**.
4. Unsuccessful load any situation - Exit failure reporting and recovery module **[23]**. (part of the recovery will be to try the IML again)

The first step of the IML is for the device sequencer to sense the HDA ID signals from the HDA. These signals identify the model of the 3380-JK (J or K), which in turn identifies which DCP microcode load to use. The sequencer then takes control of the DCP's Random Access Memory (RAM) and loads the DCP's microcode from the PES/PROM card. When the sequencer is satisfied that the load was successful, it gives the DCP a starting address and executes the load.

The idle loop module **[6]** contains two test loop routines, the 'motor on loop' and the 'motor off loop'. During the 'motor on loop', the device sequencer tests the status of the following:

1. Drive motor switch
2. Drive air pressure switch
3. Enable/disable switch
4. The spinning speed of the HDA
5. The clock used by the DCP circuits
6. Verify that neither guard band can be detected
7. Drive motor thermal

The 'motor off loop' tests the status of the following:

1. The clock used by the DCP circuits
2. The spinning speed of the HDA (should be stopped)
3. Drive motor switch

The ending status of each of these tests determines what the device sequencer does next. The correct status results in the sequencer moving on to the next test, the wrong status is reported (checkpoint check) and the correct action is taken if an action is necessary. An example where an action is required, is when both guard bands are being detected, one after the other. This indicates that the servo mechanism is oscillating back and forth. Action taken; inhibit the power amplifier by activating servo inhibit.

The device sequencer enters the idle loop from the other modules when they have completed their job and there is nothing to do. This does not mean that the device is not doing anything. The device could be reading or writing a complete track, the microcode was involved getting everything set up to do it but does nothing during the actual read or write. Just about every module has an exit to the idle loop.

The only exits out of the idle loop are the following:

1. The '+ command' signal, from the Port R/W Control card is active. (this signal is active when command gate is active on the CDP interface, indicating that there is a command for the device) - Exit command handler module **[9]**.
2. The drive motor switch is detected in the on position - Exit drive power on module **[7]**.
3. An error condition that could cause damage to the device - Exit drive power off module **[10]**.
4. Any failure - Exit failure reporting and recovery modules **[23]** (in the case where the failure could cause damage to the device, the sequencer sets up the condition for reporting the failure before exiting to the drive power down module)

[7] The routines in the drive power on module control and monitor the drive motor power on

sequence. During the drive motor power on sequence, the device sequencer does the following:

- Issue the necessary commands to the DCP to position the read/write heads in the landing zone. (park) - park/compress and decompress module **[20]**.

- Have the DCP cause a compress process, this moves the actuator to the crash stop bumpers. - park/compress and decompress module **[20]**

- Energizes the brake solenoid by picking the brake relay, this will disengage the brake. This is done through the Common Power card, both device sequencers must request the picking of the brake relay before the power card will do it.

- Pick the soft-start relay (in the MSA) through the Common Power card.

- Pick the motor run relay through the Common Power card.

- Drop the soft-start relay (in the MSA) through the Common Power card.

- Issue the necessary commands to the DCP to do a decompress. (By this time the heads are flying) park/compress and decompress module **[20]**

- Exit to the sweep/warm up module

Throughout this module, the device sequencer performs many tests to verify that the sequence is progressing safely and correctly. If an error is detected, the device sequencer branches to the drive power off module **[10]**, if needed, or straight to the power on/off failure module **[11]**.

In the sweep/warm up module**[8]**, the device sequencer directs the device through two sweeps and a warm up delay. The device sequencer accomplishes a sweep (also known as a clean process) by issuing a sweep command to the Digital Control Processor (DCP). During the clean process, the heads move from the outer guard band to the inner guard band in a series of one-cylinder seeks. The process cleans the disks before long motion seeks are attempted and permits some temperature stabilization after a period with drive motor power off. The 3380-JK does two sweeps and then delays for more temperature stabilization, for total of just over three minutes.

Throughout the sweep/warm up module, the device sequencer is monitoring for failures. The DCP is doing all the servomechanism control and will report servo failures to the sequencer. The device sequencer monitors for these and for failures in the air and motor system. When the sweep/warm up module detects failures it will branch to the drive power off module **[10]**, (if needed) or go straight to the failure reporting and recovery module **[23]**. Again, the deciding factor is whether the detected failure will do damage to the device. When the module is completed without errors, the device sequencer branches to the rezero module **[21]**.

[9] The command handler module contains a routine that tests the command code for validity. If the command is not valid, the device sequencer branches to the failure reporting and recovery module **[23]**. If the command is valid, the device sequencer branches to a routine that accommodates the command. See OPER-94 for general information about device commands.

The drive power off module **[10]** contains routines that control and monitor the drive motor power off sequence. Entry to the module is from the following:

1. Idle loop module **[6]** - The drive motor switch is detected in the off position.
2. Command handler module **[9]** - A drive power off command (4F) has been received.
3. Failure reporting and recovery module **[23]** - A failure that could do damage to the device has been detected.

During the drive motor power off sequence, the device sequencer causes the following to occur:

- Issue the necessary commands to the DCP to position the read/write head in the landing zone. (park) - park/compress and decompress module **[20]**.

- Drop the motor run relay through the Common Power card and permit the drive motor to coast for 40 seconds.

- De-energize the brake solenoid by dropping the brake relay, this will apply the brake.

- Issue the necessary commands, to the DCP, to remove all drive to the power amplifier.

If the drive motor power off sequence is completed without errors, the device sequencer branches to the idle loop module **[6]**. If an error is detected, it branches to the power on/off failure module **[11]**.

The power on/off failure module **[11]** is entered either from the drive power on module **[7]** or the drive power off module **[10]**, when a failure is detected. Within this module are tests that determine whether the drive motor should be stopped or allowed to run. This depends on whether device damage will result from the failure.

The miscellaneous command module **[12]** is used by the device sequencer to handle the following commands: reset interrupt (4A) command and the load path interrupt table (4D) command.

The check reset module **[13]** is used to handle the check-2 reset (43) command. The device sequence resets all check-2 reset latches on the Sequencer/Servo/RPS card (not the DCP, it is reset by being IML'ed when the rezero command is received) and then it activates bit 7 of the '+ sequencer write bus' with the '+ sequencer move format' signal. This causes the rest of the device logic to reset their check-2 circuits.

The diagnostics module **[14]** , as its name implies, is used to for the special diagnostic commands.

The parameter transfer module **[15]** is used by the device sequencer for all commands that will have parameters on the CDP interface after the command. This module does not execute the commands, it provides the sequence needed to handle the parameter. This module, after correctly handling the command parameter, causes the device status 1 register to be sent inbound on the CDP interface. The commands that require a parameter are as follows: all seek commands, all search commands, the set HAR command, the offset command and some diagnostic commands.

The set head address register (HAR) module **[16]** is used to execute the set HAR (63) command.

The sector search module **[17]** is entered directly from the parameter transfer module **[15]** to accommodate a sector search (62) command. When the command is a seek, sector search and verify no guard band (46 or 49) or a start offset and sector search (6E), the sector search module is entered after the servomechanism movement is completed and the servo is track following. In the sector search module, the device hardware does the comparing and activating of the record ready interrupt signal to the port card. The device sequencer, after setting the target register and activating the hardware, monitors for errors.

The seek, offset and rezero modules **[18]**, **[19]** and **[21]**are no longer true modules. They do nothing except issue the necessary servo commands to the Digital Control Processor (DCP) and monitor for errors. If there is an error within the DCP circuits or within the servo system, the DCP reports it to the sequencer.

When the DCP notifies the sequencer that the servomechanism is at the desired location, it branches to the settle module **[24]**. This again is not to do the settle (the DCP controls the servo and reports when it has acquired track following) but to verify that track following was acquired within specifications.

The park/compress and decompress module **[20]** is different from the actuator movement commands because when they are completed the servomechanism will not be track following. There is a DCP command that will cause a park to be done but there are none for compress and decompress. The device sequencer accomplishes these functions by issuing three servo to voltage commands to the DCP. These three commands cause the compress or decompress to be done in three increments.

The Digital Control Processor (DCP) module **[22]** is used by the device sequencer to handle the servo commands to the DCP, to verify that the DCP is functional and to monitor for any DCP detected failures. To accomplish this, the device sequencer does the following:

1. Monitors that the DCP's clock bit is changing states every 112 microseconds. This verifies that the DCP is functional before a command has been issued.

2. Issue the servo command with parameters (if needed)
3. Verify that the DCP has accepted the command, the DCP command line has been deactivated.
4. Monitor the DCP error bit indicators for an indication that the DCP detected a servo failure.
5. Time the servo operation and compare it against the time it should take to do the operation.

The Failure reporting and recovery module **[23]** is not a stand alone module. This module is spread out through all the modules in the device sequencer's microcode. Each failure recovery is handled differently but all failure reporting is done the same way. To report a device sequencer microcode detected failure, the sequencer stores a checkpoint value in the checkpoint log and then activates bit 3 (checkpoint check) in the device check-2 status byte. The checkpoint value in log is sent in bound on the CDP interface when the sense checkpoint log status (57) command is received. The value in the checkpoint log describes the failure and when it happened to the system collecting sense data.

What is done for failure recovery is determined by what the failure is, what the device was doing at the time of the failure and what damage this failure can do to the device. The recovery could go from 'do nothing' to power off the drive. (other examples: Servo inhibit, seek incomplete, write inhibit)

The settle module **[24]** is entered, by the device sequencer, after an actuator movement has been done by the servo system but track following has not been acquired. The sequencer does not issue any command during this module, it just times how long the servo system takes to acquire track following. When the DCP activates the track following bit, the device sequencer causes a seek complete interrupt to sent in bound to the system.

Head Disk Assembly

The head and disk assembly (HDA) contains the heads and disks for two devices: a left device and a right device. Each part contains an access mechanism.

Access Mechanism

Each access mechanism positions 16 movable heads concurrently over eight disk surfaces. Each head has exclusive access to its part of the disk surface. Fifteen of the movable heads are read/write heads for data. The remaining head, the servo head, is for reading the servo surface.

An access mechanism is positioned via a voice-coil motor (VCM), which relies on the interaction between the magnetic fields around the voice coil and a permanent magnet.

Motor Start Assembly (MSA) - Soft-Start

The MSA reduces the starting torque of the drive motor so that if a read/write head is stuck to a disk surface, the stuck head is more gently pulled loose from the surface during drive motor start-up.

The MSA contains a relay and three large resistors. The relay, which is the soft-start relay, is controlled by the Common Power card. The normally closed points of the soft-start relay form shunts for the large resistors. When the relay is energized. the resistors are in series with the windings of the three-phase drive motor, reducing the current through the motor windings (and reducing drive motor torque). The reduced torque causes a slower start-up of the disks. When the relay is de-energized, the resistors are eliminated from the drive-motor circuit.

Both device sequencers must issue the soft-start relay pick command, to the Common Power card, to start the drive motor power on sequence. The drive motor relay is picked after the soft-start relay has been picked. The drive motor runs with reduced torque for approximately 900 milliseconds. Then the sequencer releases the soft-start relay, restoring the drive motor to full power.

The location of the MSA is shown in the LOC section (see the index).

The soft-start relay and the resistors are shown on YA/YB200.

Head Addressing

For read/write operations, one of the 15 read/write heads in the selected device is selected by an address in the head address register (in the Port Read/Write Control card). The half-byte addresses used for the read/write heads are shown on the heads in Figure 14. The physical arm and head numbers in the HDA are shown in the following chart.

Address (in hex)	Selected Arm and Head
0	Arm 1, head 1
1	Arm 1, head 4
2	Arm 1, head 3
3	Arm 1, head 2
4	Arm 4, head 1
5	Arm 4, head 4
6	Arm 4, head 3
7	Arm 4, head 2
8	Arm 3, head 1
9	Arm 3, head 4
A	Arm 3, head 3
B	Arm 3, head 2
C	Arm 2, head 1
D	Arm 2, head 4
E	Arm 2, head 3

The servo head is head 2 of arm 2 (address F).

HDA Drive Motor Braking

A mechanical brake on the drive motor stops the Head Disk Assembly (HDA) spindle during an HDA drive motor power-off sequence. The brake stopping time is approximately 45 seconds (coast = 40 seconds; apply brake to 0 rpm is approximately 5 seconds). See the PWR section in the Maintenance Information Manual (MIM) for detail of the HDA drive motor power-off sequence. When power is lost, the drive brake is applied by the return spring.

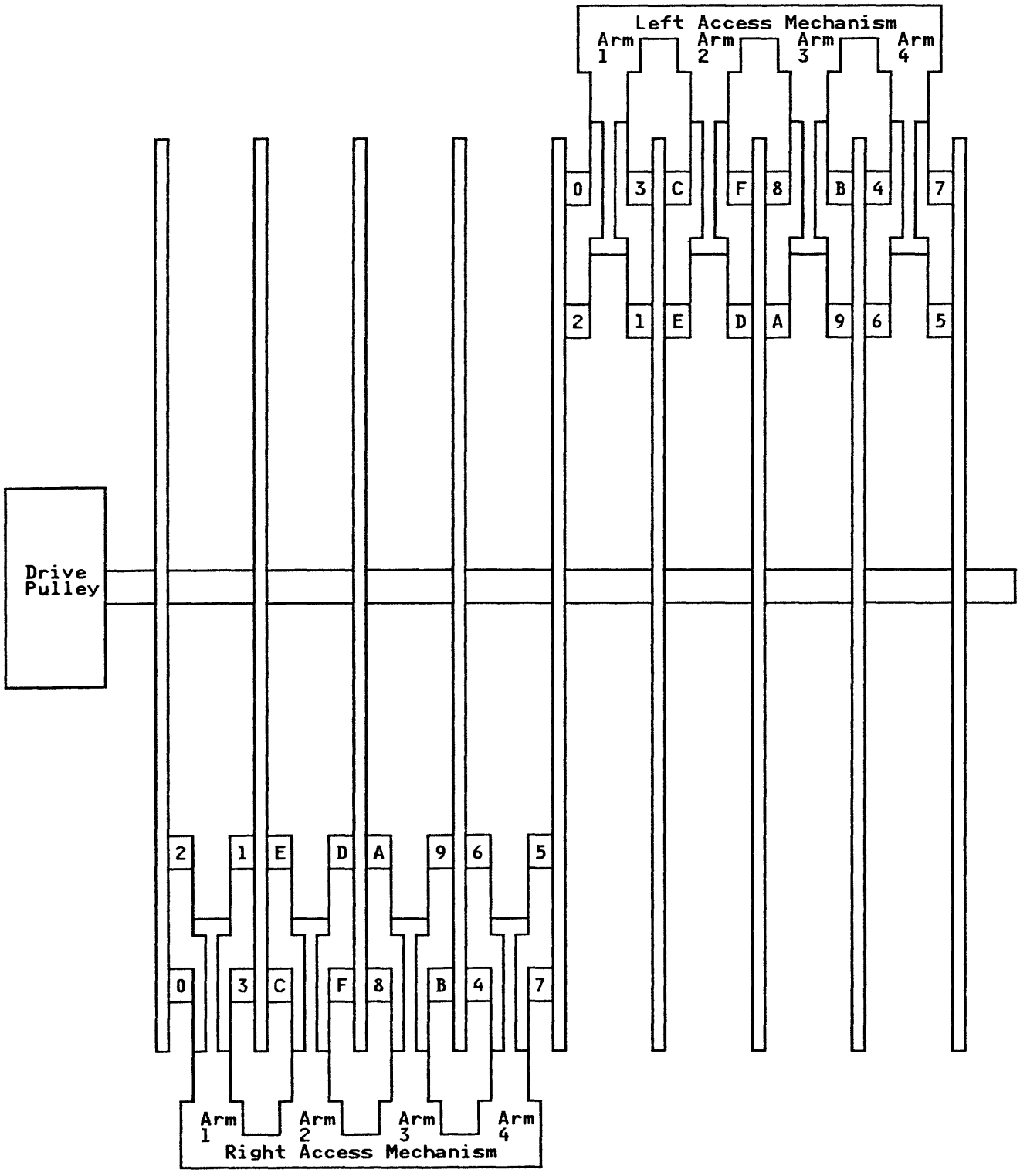


Figure 14. Arms, Heads, and Disks in the HDA

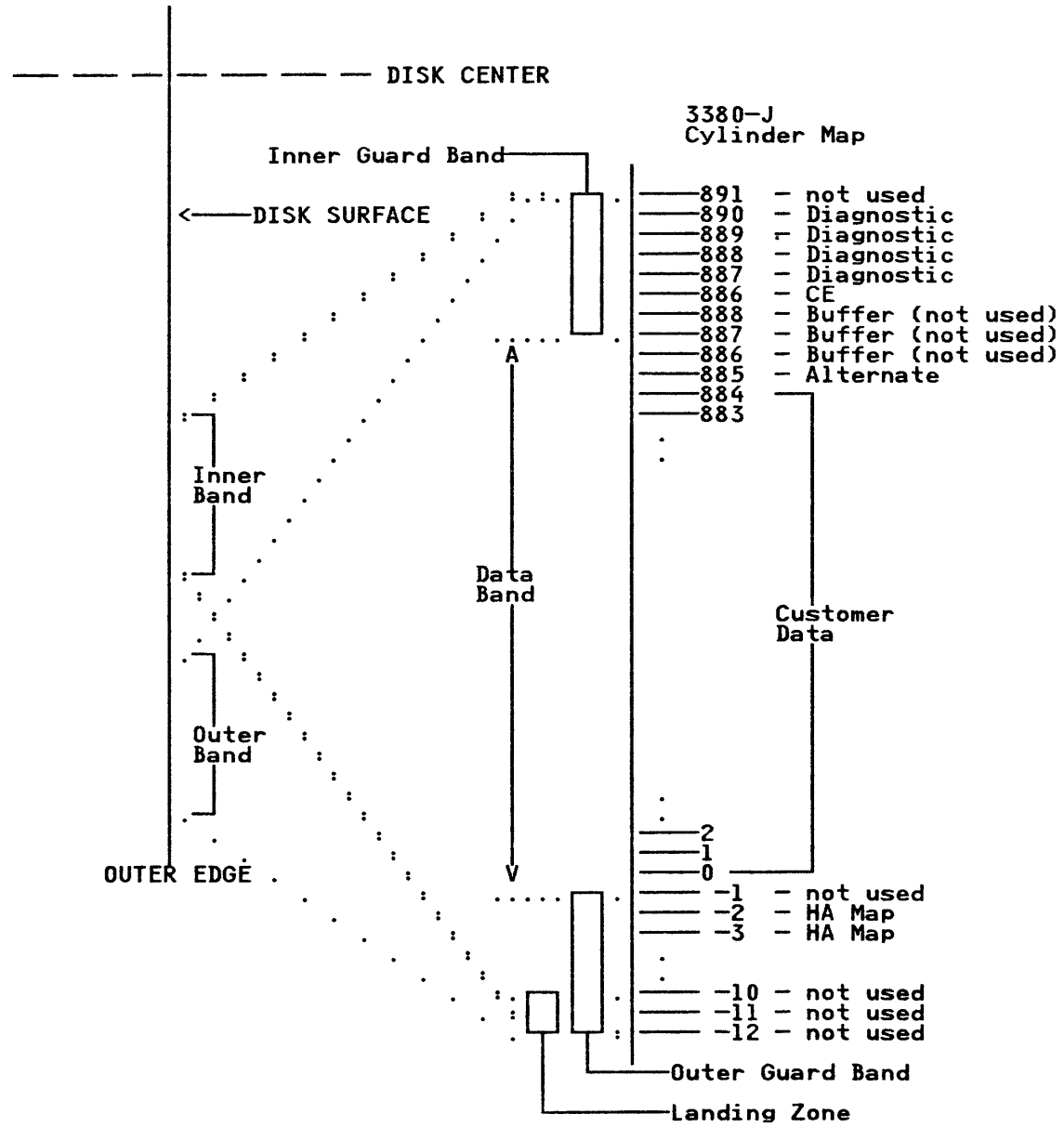


Figure 15. 3380-J Cylinder Map

Disk Surface Organization

Each disk surface accessed by movable heads contains two bands, an outer band and an inner band. An outer head is always over a part of the outer band, and an inner head is always over a corresponding part of the inner band. The outer and inner bands each contain the following parts:

- A take-off zone — where the heads are positioned when the disks start to move during the drive motor power-on sequence
- A landing zone — where the heads are positioned when disk motion stops
- An outer guard band — from the start of the band to the data band
- The data band — which contains all the customer tracks
- An inner guard band — inward from the last track in the data band

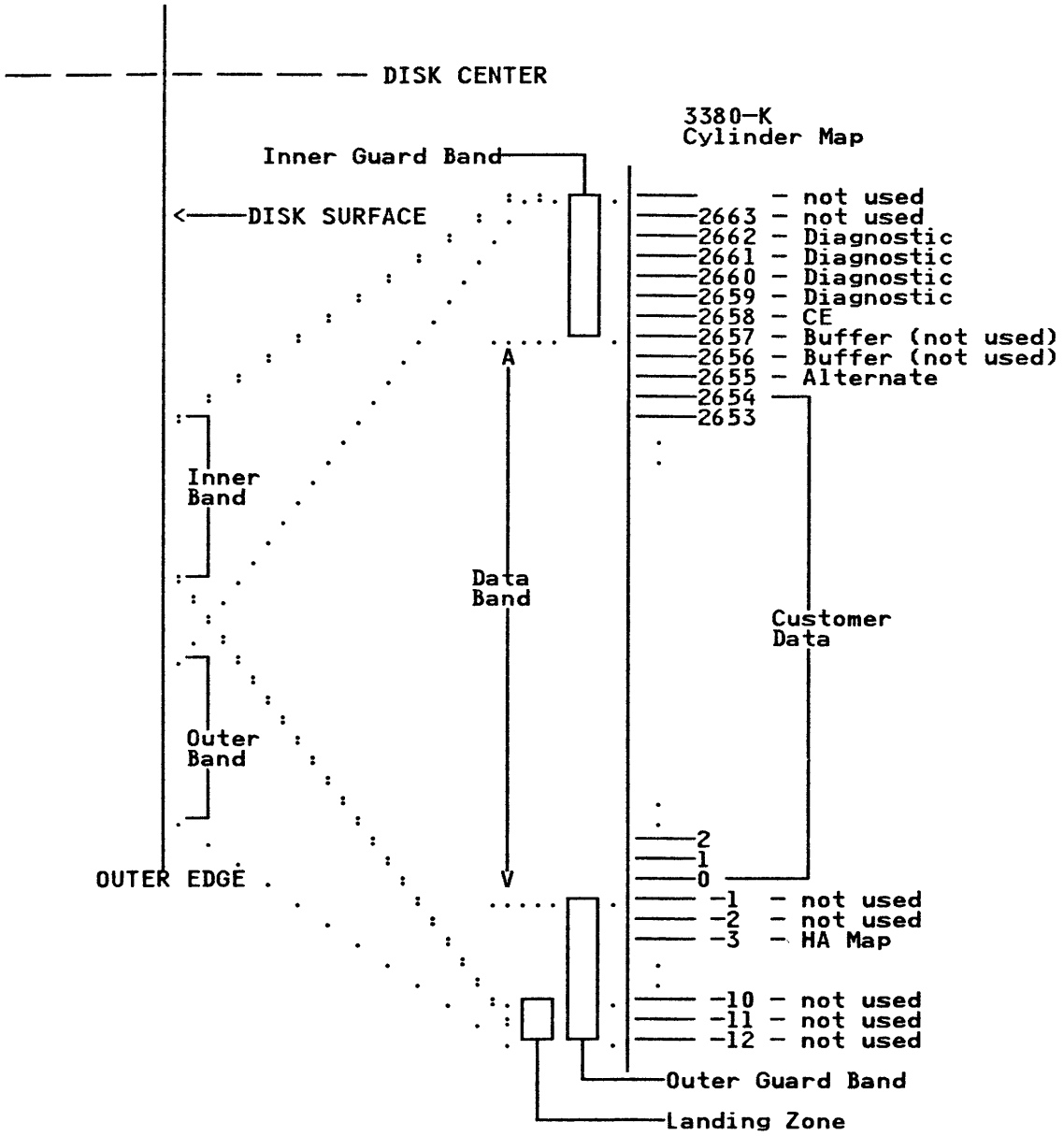


Figure 16. 3380-K Cylinder Map

- A tolerance zone — between the inner guard band and the inner limit of travel

The landing zone is determined by the outer crash stop.

The take-off zone is reached when the crash stop pad is compressed (when voice coil current is increased above normal current levels to press against the crash stop).

The inner limit of travel is determined by the inner crash stop.

The 3380-J HDAs contain 885 (0 through 884) customer cylinders. The 3380-K HDAs contain 2655 (0 through 2654) customer cylinders. For more track or cylinder information, see the following Cylinder Map figures.

The diagnostic cylinders shown in these figures are accessible through the diagnostic routines only.

The buffer cylinders, which are in 3380-JK, ensure that the last customer cylinder is not in a guard band and that the CE cylinder is well into the inner

guard band. The cylinder numbers of the buffer cylinders are duplicates of the cylinder numbers for the CE cylinder and the first two diagnostic cylinders. The tracks on the buffer cylinders are flagged defective without alternates assigned.

Access Mechanism Positioning — Servo Operations

The processes for positioning the access mechanism are controlled by the Digital Control Processor (DCP). The DCP reacts to commands issued by the device sequencer in response to device commands received from storage control.

The access mechanism positioning processes are:

- Park
- Compress
- Sweep
- Rezero
- Seek
- Track follow
- Offset

The park process moves the access mechanism toward the outer crash stop. This is part of the drive motor power-on and power-off sequences and is also used if certain errors occur.

The compress process pushes the access mechanism against the outer crash stop to change the location of the heads for take-off from the location used for landing. This process is used in the drive motor power-on sequence.

The sweep (clean) process moves the heads twice across the disk surfaces a track at a time. The purpose is to dislodge any loose particles from the surface during the drive motor power-on sequence. (The inner edge of the heads are designed to deflect particles on the surface of the disks.)

The rezero process moves the access mechanism from any position to the inner guard band, then to a cylinder in the outer guard band, and finally to cylinder 0. During a rezero operation, the access mechanism moves approximately 2 inches per second.

The seek process moves the access mechanism rapidly in a specified direction for a specified number of cylinders. The parameters for the command that causes the seek process identifies the targeted cylinder. The acceleration and velocity of the access mechanism depends on the distance remaining to be traveled in the seek operation.

The track follow process keeps the access mechanism positioned with the heads over the center of the tracks in the current cylinder. Track follow is used during write operations and during normal read operations. This process normally continues until another access mechanism positioning process is needed.

The offset process modifies the track follow process by moving the heads slightly from the center of the tracks in the current cylinder. The movement is in a specified direction for a specified distance. Both the direction and the distance are specified by parameters for a command. Offsets are used during read retries for data checks.

Servo Control

The read/write heads are positioned by a voice-coil motor that is part of a servomechanism. The servomechanism operates in both velocity and position modes, depending on the operation in progress. In velocity mode, the servomechanism attempts to move according to a velocity reference. In position mode, the servomechanism attempts to follow a position reference. For operations that require the read/write heads to follow a track (remain in the current cylinder) the servomechanism operates in position mode. When the read/write heads are required to move from one cylinder to another location, the servomechanism operates in velocity mode. The mode of operation and the circuits that support each mode of operation are controlled by the Digital Control Processor (DCP).

To provide such control, the DCP monitors the status of the servo circuits while executing the servo commands from the device sequencer. The active components for the servo system are contained in only three cards, the PES/PROM card, the Power Amplifier card and the Sequencer/Servo/RPS card. The R/W Channel Board does not contain an active servo component, but it does provide a path for the low level servo signals between the HDA and the cable that connects it to the 'B' board.

The basic input signal to the servo circuits are the signals from the servo head, which reads the servo surface in the HDA. (Each HDA contains two servo surfaces; one for each device)

Servo Surface

The servo surface, which is written at the factory, is written with a pattern such that the data, when read, contains both digital and analog information.

The digital part is written such that a change in the position of the servo head does not change the amplitude of the signal read from the digital part of the servo pattern. The digital part of the information is used to generate index pulses and guard band identification and to synchronize the circuits that process the analog part of the signal.

The analog part of the signal read from the servo surface changes in amplitude as the access mechanism moves. The analog information is processed to indicate the position of the servomechanism relative to track centers (or cylinder centers).

The smallest part of complete servo information (containing a sync pattern and enough analog information to have meaning) is called a servo burst. More than 3100 servo bursts are contained in a single track. In a single track, the same analog information is repeated. The servo surface pattern repeats every four tracks and identifies four servo track types, type 0, type 1, type 2, and type 3.

The servo surface is the outer band of the front surface of the third disk from the front for the right access mechanism, and the outer band of the front surface of the seventh disk from the front for the left access mechanism. The servo surface is associated with head 2 of arm 2 (or head F). See head F in Figure 14 on page OPER-44.

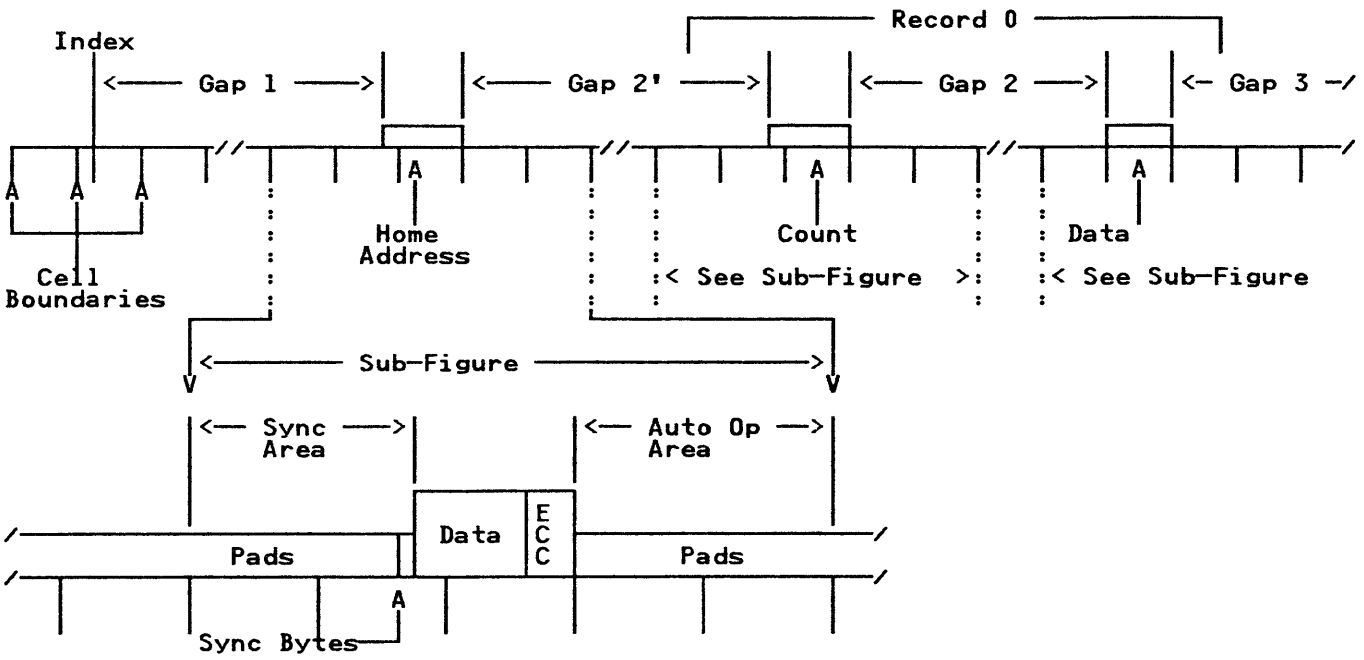


Figure 17. Track Organization (Part 1 of 2)

Track Format

A full track contains 1554 cells (0-1553). Each cell has room for 34 bytes of information. Index indicates the start of a track and identifies cell 0, the cell in which index occurs.

The track format shown on this page and the next page is typical for count, key, and data records. For count and data records (no key), eliminate the key area and the preceding gap.

In the format shown, every information or data area ends at a cell boundary, and the gaps separate the information or data areas.

Gaps

The gaps, which are included in the track format to accommodate the time needed by the system, are generally filled with pad characters (hex FF). The exception is the address mark, shown after record 0 in Part 2 of 2 of the Track Organization figure. An address mark contains a special pattern that indicates the start of a record (record 1 through record n).

Each gap has a defined length:

Gap 1 — 15.75 cells

Gap 2 — 7.00 cells

Gap 2′ — 7.75 cells

Gap 3 — 6.75 cells

If a defect exists in a gap, the gap is extended. Gap 1 is extended six cells for each defect (maximum of three). The other gaps are extended three cells for each defect (maximum of seven).

Home Address and Count Areas

The home address (HA) and the count areas each contain 40 bytes of information, including 6 bytes of sub block and 6 bytes of block Error Checking and Correction (ECC) code. The HA contains track information, such as the track address (cylinder and head) and defect skipping information. The count areas contain the same kind of information as the HA does, with the length of the associated key and data and the record number included.

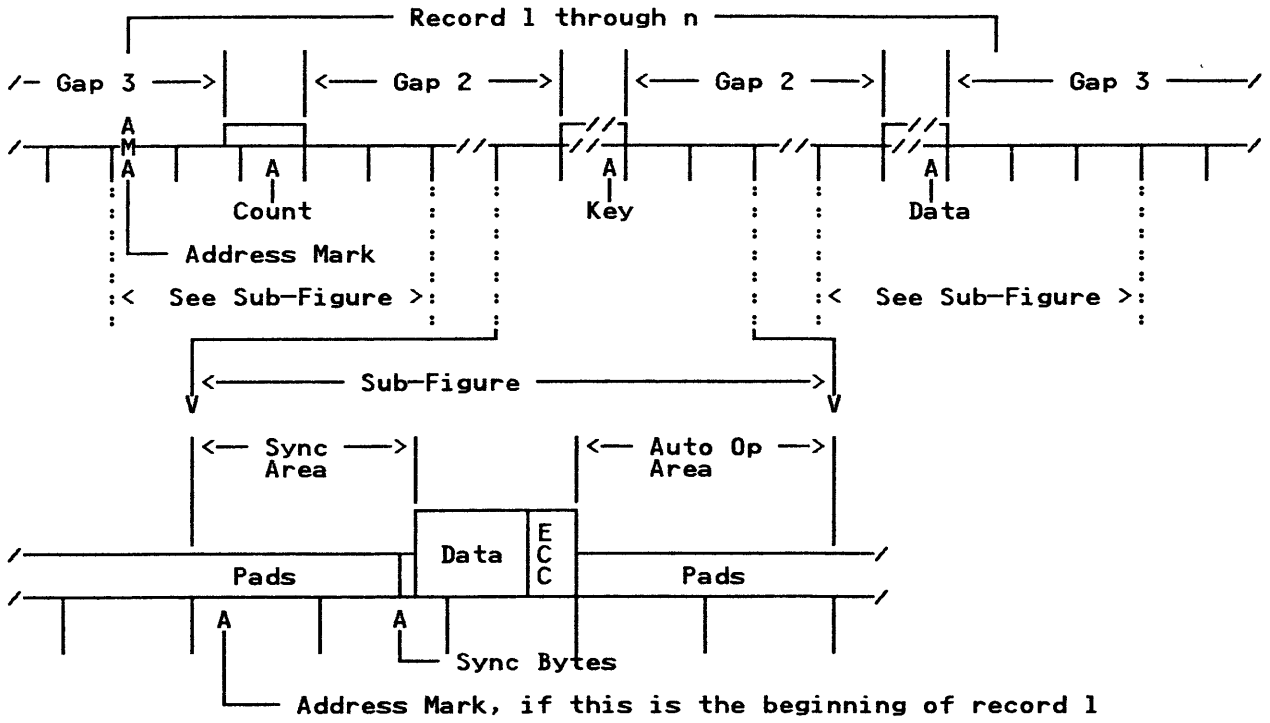


Figure 18. Track Organization (Part 2 of 2)

The format of the bytes in both the HA and the count areas is the same. See OPER-52 for the format.

Key and Data Areas

Key areas and data areas always start at cell boundaries. The number of cells occupied by a key or data area depends upon the amount of data involved.

The maximum length of a key is 255 bytes. With 6 sub block ECC bytes added every 96 bytes of information and 12 bytes of ECC at the end. This is for a total of 279 bytes of information can be contained in a key area. Nine cells are needed to contain 279 bytes, and nine cells have a capacity of 306 bytes. The 27-byte difference is occupied by fill characters, which are supplied by the storage control.

The key area contains an index that points to specific data in the data area when under programming system control. The key area length and data are specified by the customer when not under programming system control.

The data area in record 0 is always one cell long, if present. Record 0 contains information for the operating system. If record 0 is not needed, the space can be used for record 1.

The data area in record 1 through record n is like the key areas. Any part of a cell not occupied by either data or ECC bytes contains fill characters that are supplied by the storage control.

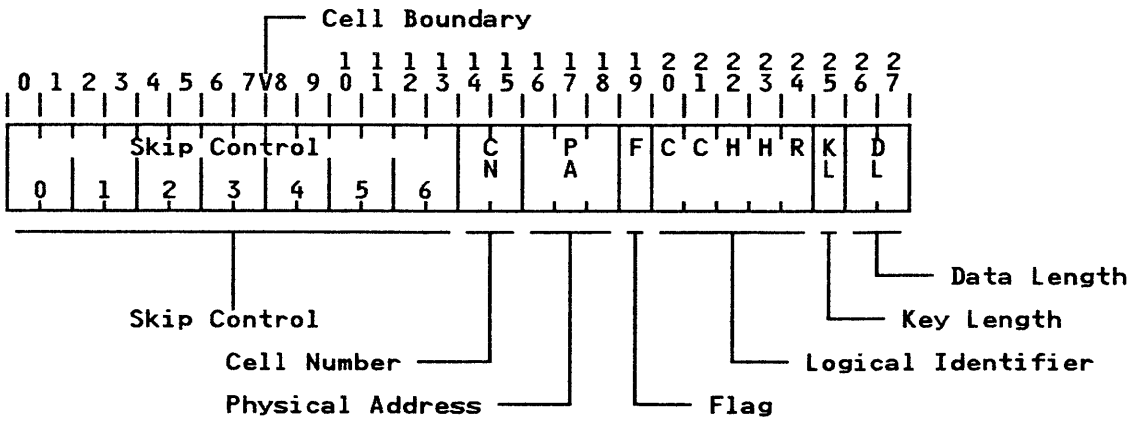


Figure 19. Home Address and Count Area Format

Home Address and Count Area Detail

The home address area and the count areas contain the following:

- Skip control
- Cell number
- Physical address
- Flag
- Logical identifier
- Key length
- Data length

Skip Control

The skip control bytes contain information concerning the location of failures on a track. Each failure causes a skip over a three-cell section of track. A maximum of seven failures are permitted on a track.

The skip control field is 14 bytes long.

Cell Number

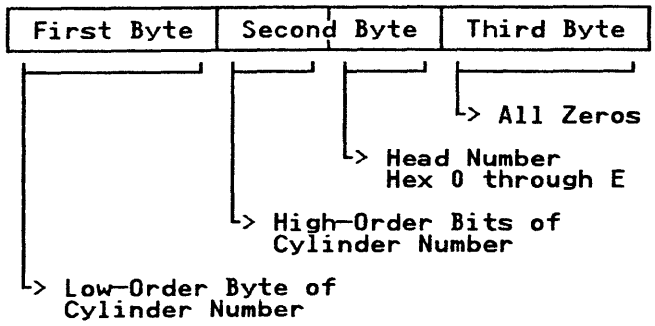
The cell number bytes contain the number of the cell that immediately precedes the two cells in which this home address area (or count area) is located.

The cell number is two bytes long.

Physical Address

The physical address bytes contain the cylinder number and the head number of the physical track. The physical address is used by the subsystem; the logical identifier is used by the system.

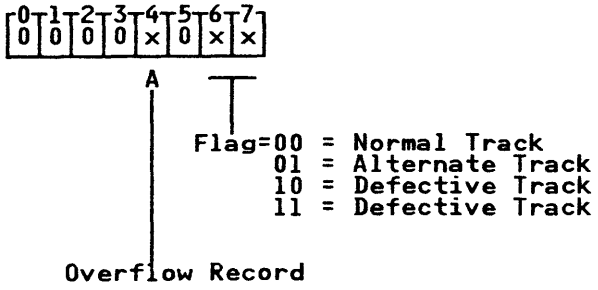
The physical address is three bytes long.



Example: 76 2E 00 = Cylinder '276' hex, head 'E' hex.

Flag

The flag byte contains the status of this track.



Logical Identifier

The logical identifier contains five bytes (CCHHR).

CC = cylinder number

HH = head number

R = record number

The logical identifier bytes contain the same cylinder number and head number that are contained in the physical address bytes. In a Home Address (HA), the record number byte is not used. In the count areas, the record number byte contains the record number (0, 1, through n). The logical identifier is used by the system; the physical address is used by the subsystem.

Key Length

The key length byte contains the length, in bytes, of the key area in a record. This length does not include any fill bytes that follow the key. The value in the key byte in the home address is zero. When the value in the key byte is zero, the key area does not exist.

Data Length

The data length bytes contain the length, in bytes, of the data area in a record. This length does not include any fill bytes that follow the data. The data bytes field is not used in an HA. When the value is 0 (in other than home address record count fields), a one-cell data area exists containing 20 bytes of padding followed by 12 bytes of error correction code.

The data length field is two bytes long.

Track Format Processing

Track format is processed by a series of extended commands from the storage control, which responds to channel commands from the system.

The chain of processes associated with track format is basically continuous. Each command specifies a collection of processes that start and end mostly at cell boundaries. The number of cells spanned by the processes depends upon the command and the amount of data transferred.

Commands that include the transfer of data affect the process for one full cell before the data and usually for two cells following the data area.

In the two cells following the data area, the controller sends End Op to the storage control (indicating the end of the operation), and the storage control sends the next command to the controller. The new command takes control of the processes for the cell following the cell in which the command is received.

The area preceding the data area is the sync area, and the two cells that follow the data area are called the auto-op area.

For the next four topics, use the figure that is titled 'Track Organization (Part 1 and 2), that starts on page OPER-50.

Sync Area

The sync area precedes the data. The sync area provides the time during read operations to synchronize the oscillator that drives the system clock (controller clock). The last two bytes of a sync area are always a special pattern that contains a sync byte. The sync byte is recognized by controller circuits and used to start the clock ring at the start of data during read operations.

Auto-Op Area

The two cells following the last data cell are the auto-op area. The commanded function is completed before the read/write head enters the auto-op area. The auto-op area provides the time needed for indicating the end of the commanded function (with an End Op tag) and for the storage control to send the next command.

The areas identified as data (or data and fill) are processed in transfer mode.

ECC Area

The Error-Checking and Correction (ECC) area is always 12 bytes long, 6 sub block and 6 block ECC bytes, and is always in the last cell of the field. If the field is over 96 bytes long, then there will also be 6 bytes of sub block ECC data for every 96 bytes of information. These 6 bytes will not be located in the ECC area but after each of the 96 bytes they are formulated from.

If a key or data field (for record 1 through record N) is not completed within the area controlled by a single command because of a defect in the disk, the ECC area is omitted from the format that precedes the defect. The defective area in the disk is skipped, and another command completes the field after the defect. The commands used to complete a key or data field after a defect is skipped are Write, Write P, Clock, Erase P or R P, and Read. The read and write commands used do not reset the ECC circuits before data is read or written. This continues the ECC calculation from the start of the field.

Gaps

As shown in the Track Organization figure (page OPER-50), the areas that are processed by commands that transfer data extend into the gaps. The remaining parts of the gaps are processed by commands that do not transfer data. These parts of the gaps are processed by pad commands and space commands.

Because pad and space commands do not transfer data, the areas controlled by these commands are not subdivided. The functions (End-Op and the next command), which occur in the auto-op area for data commands, occur in the last two cells controlled by the pad or space commands.

Command Transfers During Track Processing

As described on OPER-83 (Extended Commands), control mode tag sequences on the director-to-device controller (DDC) interface are interlocked. The storage control can send commands only while the tag in is End Op. The controller can change the DDC tag in from End Op to Selected Null only if the tag out is Command Gate. The storage control can change the tag out from Command Gate to Selected Null only if the tag in is Selected Null. And the controller can change the tag in from Selected Null to End Op only if the tag out is Selected Null.

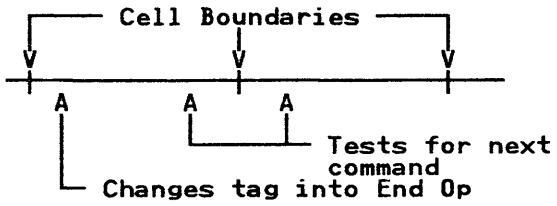
Track processing involves a series of extended commands. The first command, which achieves orientation, is a non-oriented command. All remaining commands for continued processing of the track are oriented commands.

To maintain orientation through consecutive commands, each command must be received by the controller within a critical amount of time. The process for each *next* command must start when the process caused by the preceding command stops.

When the controller is oriented, the time for command transfers is during the time the

read/write heads are in the auto-op area (for commands that use data transfer modes, or in the last two cells of an area processed by pad or space commands). During these times, the controller changes the tag in to End Op to indicate the completion of the current operation. Then, the controller sequencer branches to a common routine that tests for the next command.

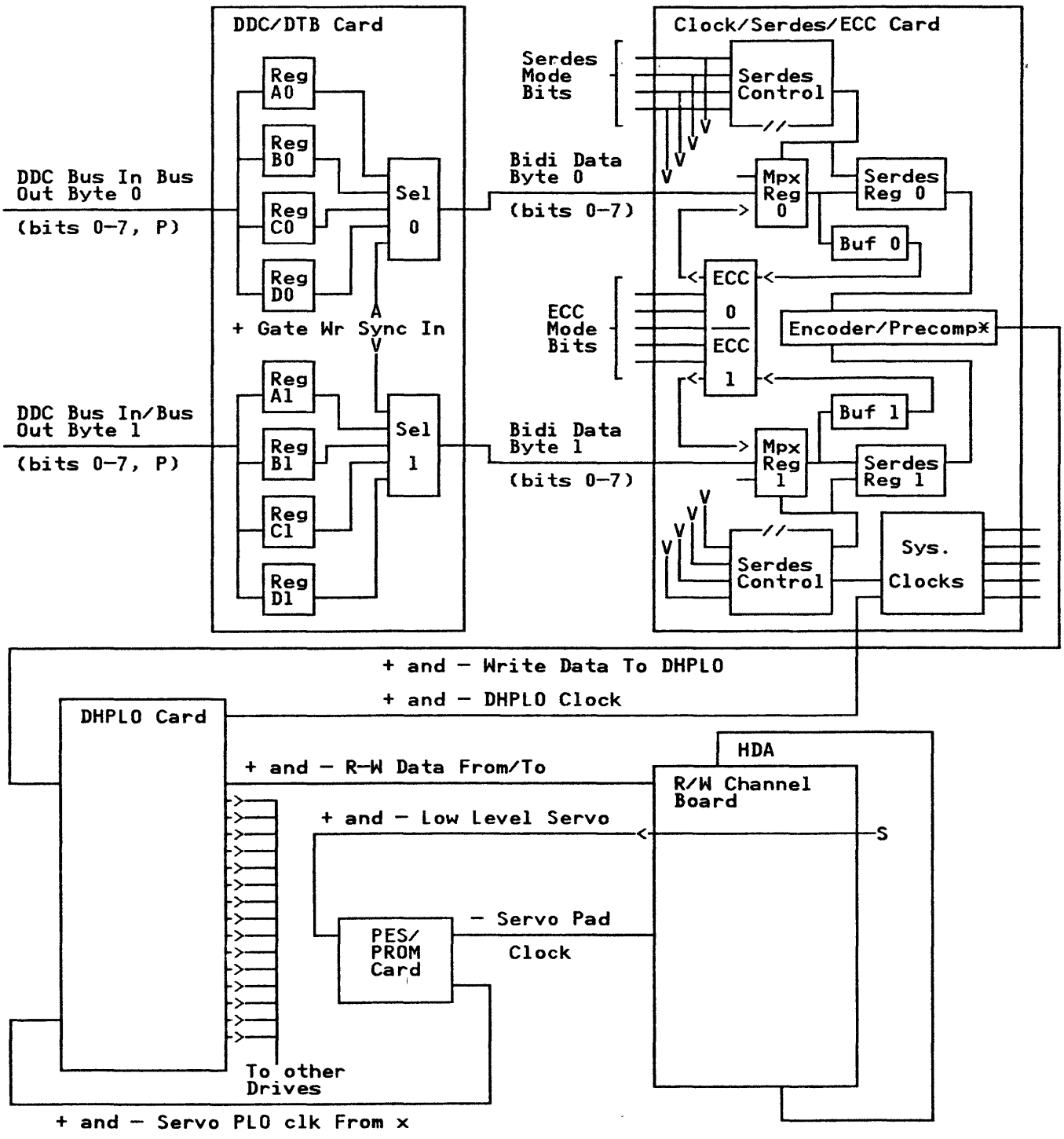
The following figure shows the actions of the controller sequencer relative to the two-cell auto-op (or the last two cells of an area processed by Pad 2 through 15 and Space 2 through 15 commands).



If the tag out on the DDC interface is Command Gate when the controller sequencer tests for a command, the sequencer immediately branches to a routine for the new command. The new command takes effect at the cell boundary following the test.

The only commands the storage control must send in time to be recognized by the first test are commands that write or erase the count area for a record 1 through record n field. All other oriented commands are acted upon as if they were received during the cell following the one in which the End Op for the preceding command occurs.

When the new command is received by the first test (during the same cell in which End Op occurs) and the command is for writing or erasing the count area for a record 1 through n kind of field, the auto-op area ends one cell earlier than usual, and the new command takes effect at the cell boundary. The number of cells affected by pad or space commands is also shortened by one cell when a command is received in time for the first test. (This occurs only in gap 3)



* See OPER-109 for descriptions of the encoder and precomp circuits.

Figure 20. Write Paths

Write Paths

The previous page shows the write paths for:

- Drive padding
- Pads
- Address marks
- Sync bytes
- Data and fill
- ECC bytes

The controls for each of the write paths, except drive padding, are the Serdes mode bits and the ECC mode bits. The Serdes and ECC mode bits are set by the controller sequencer.

Drive Padding

Drive padding is initiated by the controller during the execution of an End Read/Write command received while doing a format write. A format write requires that pad characters be written from the end of data to the end of the track. (Index)

To start drive padding, the controller sequencer activates bit 3 in the CDP data bus while the write control signals to the R/W Channel board in the device are active. (See OPER-34 for more on the R/W Channel board control signals.) During drive padding, the output signal (- Servo Pad Clock signal) from an oscillator in the PES/PROM card is used as write data. Each plus shift of the signal produces a transition on the disk, covering any data previously written on that part of the surface.

Drive padding stops at the detection of the next index pulse.

pads

Pad characters are supplied by the controller while the Serdes mode bits are hex 5. (Write Pad) This mode forces all 1 bits into Serdes registers 0 and 1, producing the hex FF pad characters.

Address Marks

An address mark is written while the Serdes mode bits equal hex F. (Write Address Mark) An address mark occupies the space of four bytes on the disk and is written with only two transitions total in the four bytes (one at the start of the second byte, and the other in the middle of the third byte).

Sync Bytes

The sync byte pattern is gated into multiplex registers 0 and 1, from the DDC/DTB card, while the Serdes mode bits equal hex 6. (Write Sync Byte) The sync byte pattern always follows pad characters and precedes the first byte of data.

Data and Fill

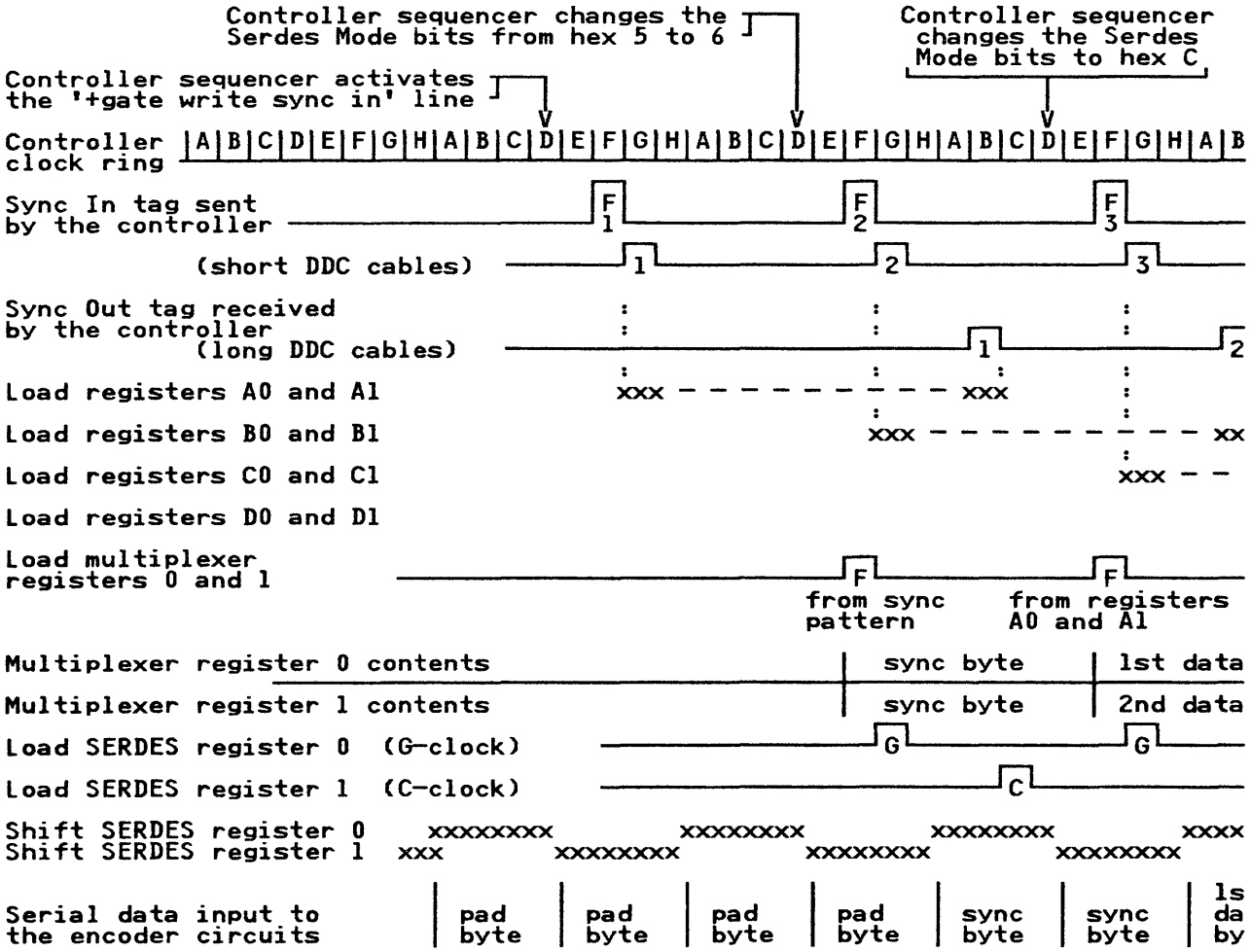
Data and fill characters are received by the controller from the storage control in data transfer mode. While the Serdes mode bits equal hex C, (Write Data From DTB) the bytes from the storage control are gated to multiplex registers 0 and 1 from registers A0, B0, C0, and D0 for byte 0 and from registers A1, B1, C1, and D1 for byte 1.

ECC Bytes

The 6 or 12 ECC bytes are written while the Serdes mode bits equal hex A (Write ECC) and the ECC mode bits equal a hex 3 or a hex 4. (Write Sub-Block ECC or Write Sub-Block and Block ECC) The ECC bytes are gated from the ECC circuits to the multiplex registers 0 and 1.

While the data and fill is written, the ECC control mode bits are equal hex 2, (Write Data) which causes the ECC circuits to process the data and fill bytes to generate the ECC bytes.

Write Data Transfer (first half)

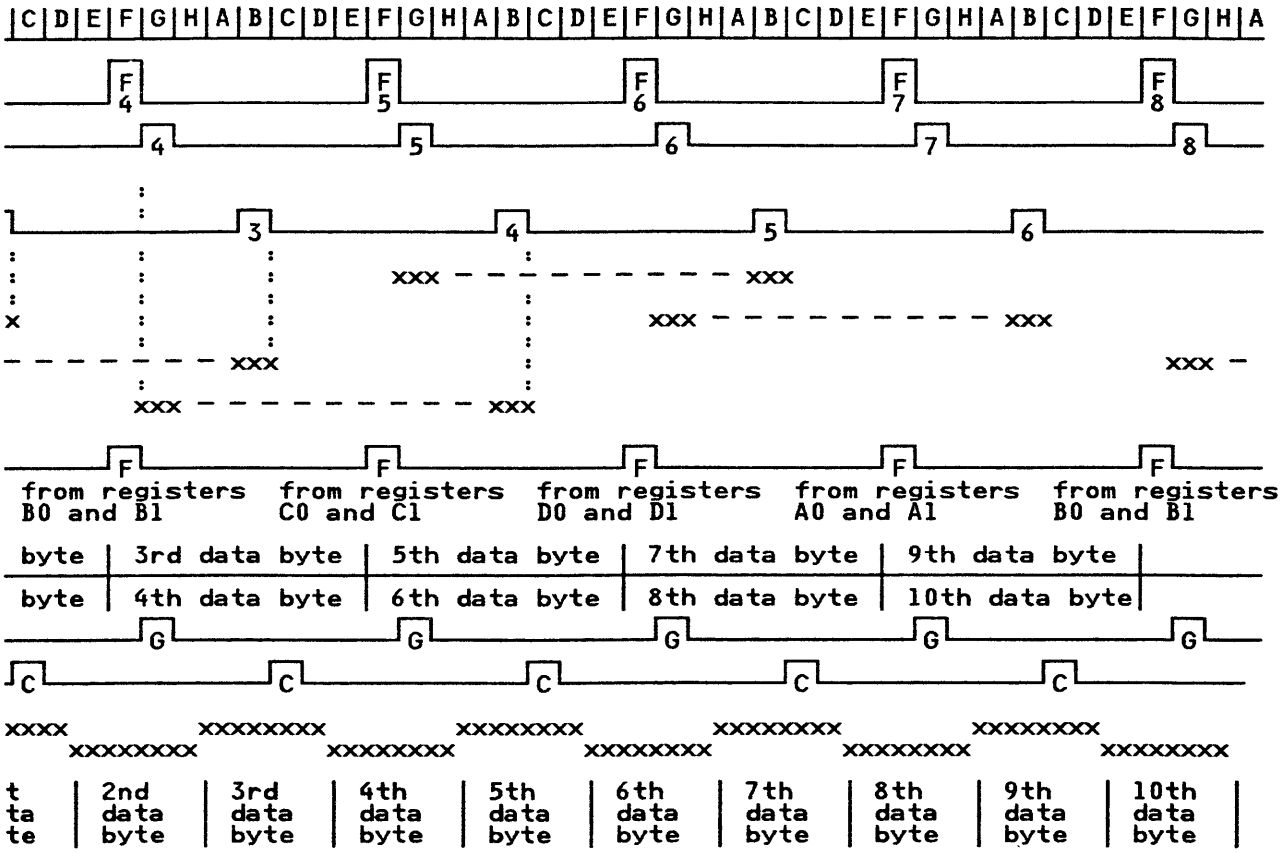


The write data transfer process moves data and fill characters, two bytes at a time, from the storage control to the controller.

During write data transfers, the DDC interface is in transfer mode, and both the byte 0 and byte 1 buses carry outbound signals. Each pair of bytes is transferred with a Sync In and Sync Out tag sequence on the DDC interface. Each Sync In tag requests two bytes of data from the storage control. Each Sync Out (response) validates two bytes of data on the DDC byte 0 and 1 buses.

The write data transfer process is started and stopped by the controller sequencer, which stays in step with the track format by executing 16 instructions in each cell. The storage control, which maintains the transfer byte counter, indicates that only 12 more bytes remain to be transferred by responding to the Sync In tag from the controller with a Command Gate tag out instead of the usual Sync Out tag. The Command Gate tag (occurring while the DDC interface is in transfer mode) sets a latch that the controller sequencer tests twice each cell. When the sequencer tests the status of the latch and finds the latch set, the sequencer branches to a series of instructions that permit only as many Sync In tags to be sent to the storage control as are needed to complete the transfer.

Write Data Transfer (second half)

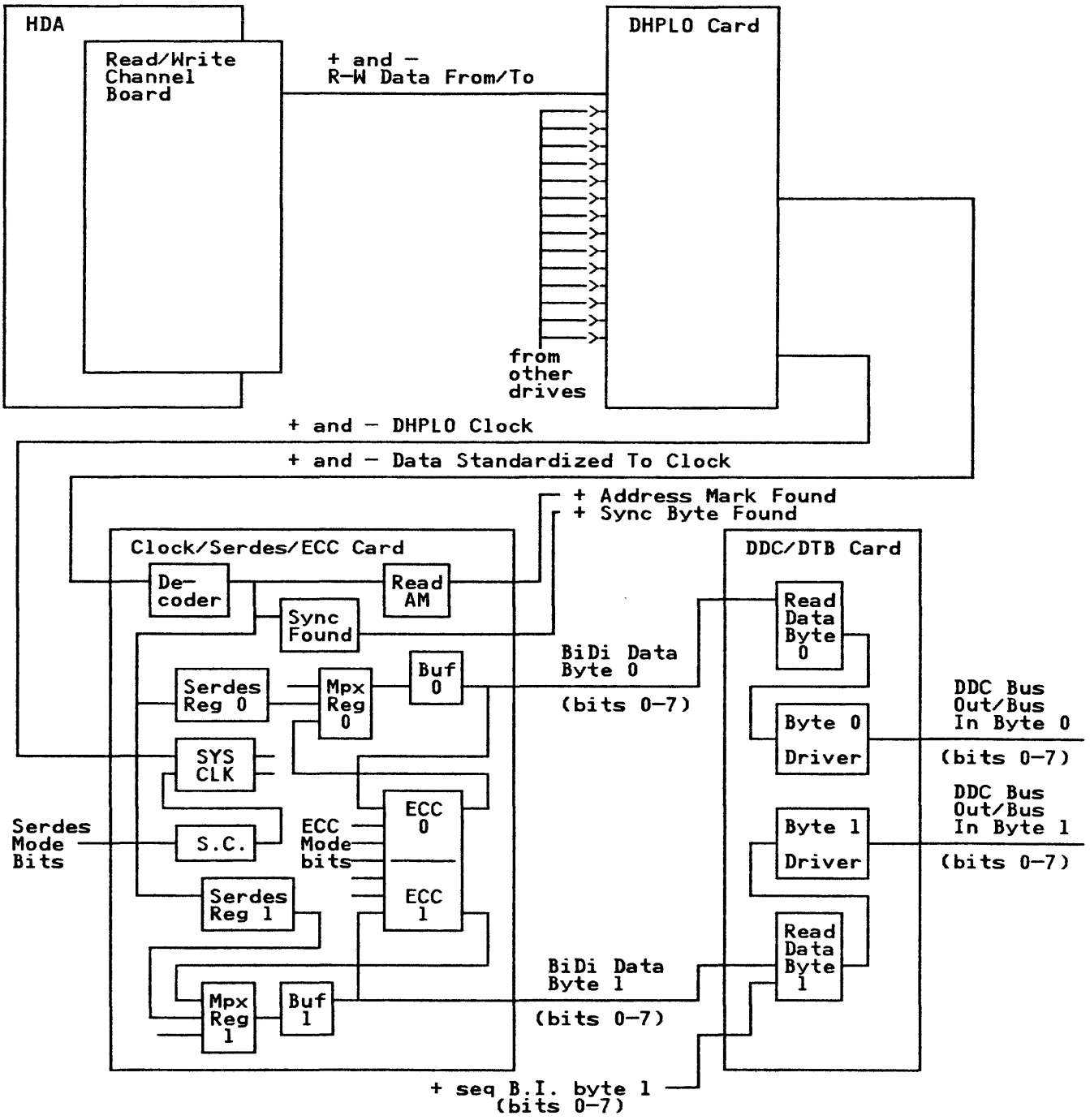


To start the write data transfer process, the controller sequencer activates the '+ gate write sync in' line. While this line is active, the controller changes the DDC tag in from Selected Null (11) to Sync In (01) for the duration of F-clock time. To stop the write data transfer process, the controller sequencer deactivates the '+ gate write sync in' line.

The figure on this and the previous page shows the start of a write data transfer for a write operation. Notice that the first Sync In tag occurs approximately two-and-one-half clock rings before the first byte of data starts into the encoder circuit. Notice too that the Sync Out tag timings are shown twice in the figure, once for short control interface cables and once for long interface cables. The delay between the time that the pulse occurs for short and long cables is because of propagation delay. It takes time for the Sync In tag to reach the storage control, and it takes time for the Sync Out tag to reach the controller.

As shown in the figure on this page, the controller sequencer controls the action of the Serdes circuits by changing the Serdes mode bits. This selects the source of data for the Serdes circuits and controls the Serdes circuits operations. (See the figure on OPER-64)

Read Paths



This page shows the read paths for:

- Recognizing address marks
- Recognizing sync bytes
- Reading data and fill
- Reading ECC bytes from the disk
- Transferring ECC correction bytes to the storage control

Recognizing Address Marks

To search for address marks, the controller sequencer activates the '+ read address mark' line. While the line is active, circuits for reading an address mark are enabled in the Clock/Serdes/ECC card. When the enabled circuits recognize an address mark, the circuits activate the '+ address mark found' line, which the controller sequencer frequently tests during an address mark search.

During an address mark search, the Serdes mode bits equal hex 0, (reset) which keeps the Serdes circuits reset.

Recognizing Sync Bytes

Sync bytes immediately precede the first data byte. To correctly align the clock ring and the controller sequencer instructions with data, the controller sequencer sets the Serdes mode bits to hex 3, which is the read mode, and sets the ECC mode control bits to hex 2, which is the write data mode. Together, these two modes stop the system clock ring at H time (see OPER-25). The clock normally starts again when circuits in the Clock/Serdes/ECC card activate the '+ sync byte found' signal. The circuits activate the '+ sync byte found' signal when the pattern of the read data in the shift register is decoded as the sync byte pattern. The '+ sync byte found' signal remains active until the controller sequencer changes the Serdes mode bits from hex 3.

Reading Data and Fill

Data and fill characters are sent to the storage control in data transfer mode. After the clock ring has been started by the '+ sync byte found' signal, the decoded serial bit stream from the selected read/write head is shifted into deserializing circuits in the Clock/Serdes/ECC card. The first eight bits into one Serdes register and the next eight bits into another Serdes register. When a Serdes register is full, the assembled byte is loaded in a multiplexer register while the other Serdes register is filling. While data and fill characters are read, the ECC mode control bits equal hex 5, (read data) and the Serdes mode bits equal hex 3 (read).

Reading ECC Bytes From The Disk

The read path for reading the Error-Checking and Correction (ECC) bytes from the disk is exactly the same as for data and fill characters except that these ECC bytes are not sent to the storage control.

For reading the ECC bytes from the disk, the ECC mode control bits equal either a hex 6 (Read Sub-Block ECC) or hex 7, (Read Sub-Block and Block ECC) and the Serdes mode bits equal hex 3 (read). The ECC bytes read from the disk are compared with the ECC bytes generated during the reading of the data and fill characters.

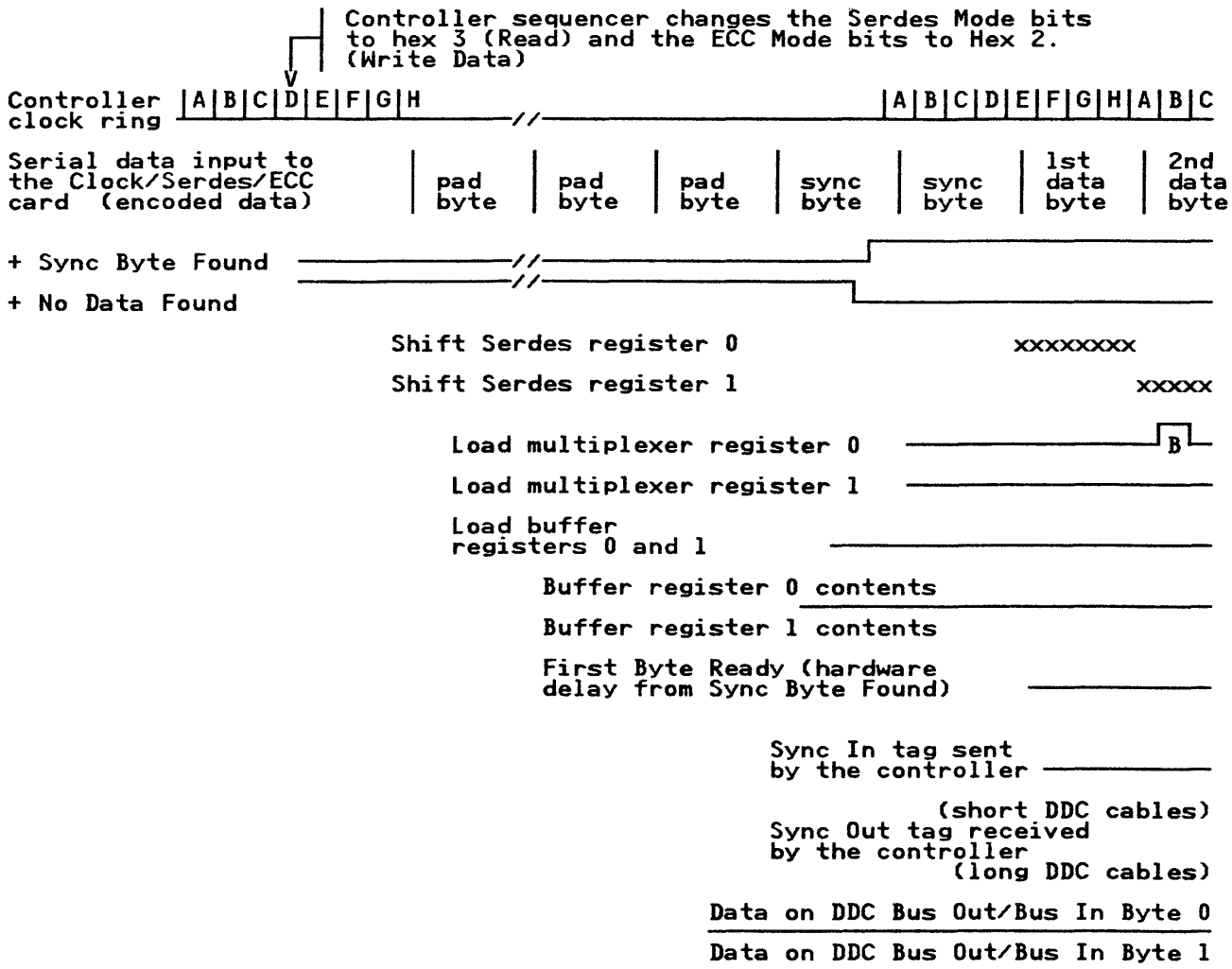
Transferring ECC Correction Bytes

After a read error, which is detected through the unequal compare of the ECC bytes from the disk with the ECC bytes generated during the reading of data and fill, the storage control requests correction data by issuing a Sense ECC Bytes (hex E2) command to the controller.

During the execution of the command, the 274 bytes of ECC correction data is generated in the ECC circuits, loaded into the multiplexer registers, and sent to the storage control (two bytes at a time) in transfer mode.

While the ECC correction bytes are being transferred, the ECC mode control bits equal hex A, (Transfer Correction Data) and the Serdes mode bits equal hex 3 (read).

Read Data Transfer (First Half)

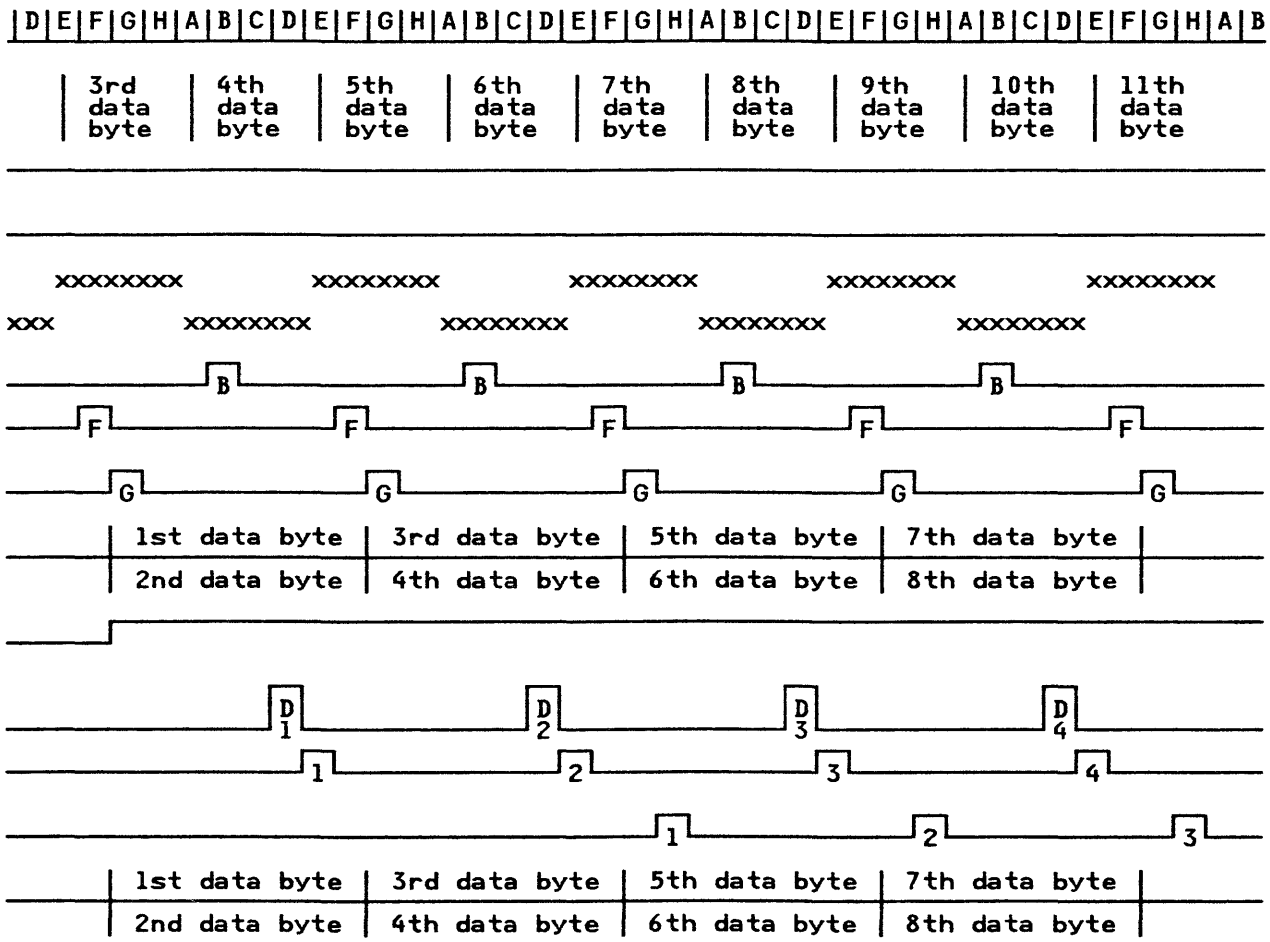


The read data transfer process moves data and fill characters (and ECC correction bytes), two bytes at a time, from the controller to the storage control.

During read data transfers, the DDC interface is in data transfer mode, and both the DDC byte 0 and DDC byte 1 buses carry inbound signals. Each pair of bytes is transferred with a Sync In and Sync Out tag sequence on the DDC interface. Each Sync In validates two bytes of data on the DDC byte 0 and 1 buses. Each Sync out (response) acknowledges the receipt of two bytes of data.

The figure on this and the next page shows the sequence at the start of a read data transfer for read data (not for ECC correction byte transfers). As shown, the controller sequencer starts the process by setting the Serdes mode bits and the ECC mode bits to hex 3 (Read) and hex 2 (Write Data) respectively. This prepares the Serdes circuits to receive the serial read data for deserializing, but also stops the clock ring, which is used to synchronize the system clock and the sequencer microcode to the data. The Serdes circuits remain idle until the clock ring is started by the '+ sync byte found' signal. (See Recognizing Sync Bytes on OPER-61.)

Read Data Transfer (Second Half)



The Clock/Serdes/ECC card contains a shift register and several decoder circuits that are used to recognize the sync byte pattern. Before the sync byte pattern is fully in the shift register, one of the decoder circuits resets a 'no-data-found' latch, deactivating the '+ no data found' signal. When the sync byte is fully in the shift register, the other decoder circuit activates the '+ sync byte found' signal.

The '+ first byte ready' signal is activated at G-clock time of the second clock ring after the '+ sync byte found' signal was activated. By then, the first two data bytes are ready to be sent to the storage control. The '+ first byte ready' signal combines with the decode of the Serdes mode bits at hex 3 to activate the '- read data or corr' signal. (from the clock/Serdes/ECC card to the DDC/DTB card) While the '- read data or corr' signal is active, data is gated through the DDC/DTB card to the DDC byte 0 and 1 buses, and the Tag In change to Sync In is enabled.

(During the transfer of ECC correction bytes, the '- read data or corr' signal is activated by the decode of the ECC mode bits at a hex A - Transfer Correction Data.)

The controller sequencer prepares to stop the read data transfer process (for read data, not ECC correction byte transfers) when the sequencer tests the '+ stop/delta freq check' signal and finds it active. The '+ stop/delta freq check' signal is

activated when the Command Gate Tag Out is received as a Sync In response.

Serdes Mode and ECC Mode Bits

The Serdes mode bits control the functions of the serdes (serializer/deserializer) circuits in the Clock/Serdes/ECC card and the source of data to the serdes circuits.

The ECC (Error-Checking and Correction) mode bits control the functions of the ECC circuits and the destination of data from the ECC circuits.

During read and write operations, and during the calculation and transfer of ECC correction bytes, the status of the Serdes mode bits and the ECC mode control bits must change in specific sequences. These sequences are not described in the OPER section because the Serdes mode bits and the ECC mode control bits are controlled completely by the controller sequencer through microcode.

Serdes Mode Bits

The status of the Serdes mode bits is decoded to control the mode of operation of the serdes circuits and to select the source of the data for the operation. The following paragraphs describe the effects of the decode of the valid Serdes mode bit combinations.

Serdes Mode Bits = Hex 0 (Reset)

While the Serdes Mode bits equal hex 0, the Serdes circuits are reset. This mode conditions the circuits before the start of read and write operations.

Serdes Mode Bits = Hex 3 (Read)

While the Serdes mode bits equal hex 3, the serdes circuits are conditioned to deserialize. Serial read data from the decoded circuits in the Clock/Serdes/ECC card is deserialized, and the parallel output from the serdes circuits is available to the multiplexer registers. See OPER-60 for more information on the effect of the Serdes mode bits during read operations.

Serdes Mode Bits = Hex 5 (Write Pad)

While the Serdes mode bits equal hex 5, the serial output lines from the Serdes circuits are held to all ones, which supplies hex FF or pad characters to the encoder circuits. These pad character are only used for the GAP areas of the track format.

Serdes Mode Bits = Hex 6 (Write Sync Byte)

While the Serdes mode bits equal hex 6, the serdes circuits are conditioned to serialize. The 2-byte sync pattern (in parallel from the DDC/DTB card) is serialized and supplied to the encoder circuits (see OPER-57).

Serdes Mode Bits = Hex 9 (Resync)

While the Serdes mode bits equal hex 9, the Serdes circuits are conditioned to serialize. Input bytes to the serdes circuits are inhibited so that the serial output is all zeros. This serdes mode is used at the end of all data write operations. As a result, two bytes of zeroes are written immediately following the last ECC byte (or immediately following the last data or fill byte if the ECC bytes are not written). The two bytes of zeros are located in the first two bytes in the auto-op area.

Serdes Mode Bits = Hex A (Write ECC)

While the Serdes mode bits equal hex A, the Serdes circuits are conditioned to serialize. The source of the parallel input bytes for the Serdes circuits are the ECC circuits (see OPER-57).

Serdes Mode Bits = Hex C (Write Data From DXB)

While the Serdes Mode bits equal hex C, the serdes circuits are conditioned to serialize. The source of data for the serdes circuits is the storage control. The data and fill characters from the storage control are transferred to the controller in data transfer mode. See OPER-57 for the write path, and see OPER-60 for information on write data transfers.

Serdes Mode Bits = Hex F (Write Address Mark)

While the Serdes mode bits equal hex F, the serdes circuits are conditioned the same as for hex 5, which supplies pad characters to the encoder circuits. (See OPER-57). The address mark circuits (also shown on OPER-57) are activated while the Serdes Mode bits equal hex F. The address mark circuits inhibit the flow of serial data through the pre-comp circuits to the DHPLO card to produce the address mark.

ECC Functions

The ECC circuits are used during read and write operations to provide a way to check the accuracy of the read/write process and to supply a way to correct some data errors in the process.

During write operations, the data and fill characters transferred from the storage control are processed, in 96 byte sub-blocks, by the ECC circuits in the Clock/Serdes/ECC card to calculate a 6-byte sub-block ECC code. At the same time, all the data is being processed to calculate a 6-byte block ECC code. The 6-byte sub-block ECC code is written on the disk at the end of each sub-block. The block ECC bytes are written on the disk at the end of the sub-block ECC bytes for the last sub-block of data.

During read operations, the data and fill characters read from the disk are processed to generate the same sub-block and block ECC bytes as during write operations. When the 6-bytes of ECC code are read at the end of each of the sub-blocks, they are compared with the 6-bytes of ECC code calculated during the reading of the sub-block. The same is done for the block ECC bytes.

The write and read data processes were accurate if the ECC bytes read and those calculated are exactly the same.

If the calculated and read sub-block ECC bytes are not the same (byte for byte), the difference and the location is saved, in the ECC RAM storage, until all the data has been read (there may be more then one sub-block failure or a block failure). The ECC circuits also check whether the error occurred in the data part or the ECC part of the operation. If, at the end of reading data, a data error was detected, the ECC circuits activates the '+ ECC Data Check' signal. (The controller sequencer microcode tests the status of the '+ ECC Data Check' signal to determine the which end-op code to send at the end of the operation.) The end-op code that indicates a data check is either a hex 03 or hex 04. The hex 04 end-op, is a data check with a controller under voltage condition.

To attempt to correct the error in the data, the storage control issues a Sense ECC Bytes (hex E2) command to the controller. During the execution of this command, the ECC circuits process the error information and send all 256 bytes of RAM storage to the storage control in transfer mode. The storage control then processes the error information and corrects the correctable data checks in the data that is stored in its full track buffer. The corrected data is then sent to the host processor.

ECC Mode Bits

The status of the ECC mode bits is decoded to control the mode of operation of the ECC circuits. The effects of the valid combinations of bits are described in the following paragraphs.

ECC Mode Bits = Hex 0 (Reset)

When the ECC mode bits equal hex 1, the ECC circuits are reset, this prepares the circuits for read and write operations.

ECC Mode Bits = Hex 1 (Idle)

While the ECC mode bits equal hex 1, the ECC circuits are conditioned to do nothing, just hold all calculation at the position they are in. Idle may occur due to defect skipping or interleaving. The values of the calculated ECC bytes don't change during the idle.

ECC Mode Bits = Hex 2 (Write Data)

While the ECC mode bits equal hex 2, the ECC circuits are conditioned to receive the data and fill character bytes, from storage control, (write data transfer) and to process these bytes to calculate the sub-block and block ECC data.

ECC Mode Bits = Hex 3 (Write Sub-Block ECC)

While the ECC mode bits equal hex 3, the ECC circuits are conditioned to transfer the sub-block ECC bytes to the serdes registers to be written on the disk. These ECC bytes are written behind the sub-block of data that was just written from storage control.

ECC Mode Bits = Hex 4 (Write Sub-Block and Block ECC)

While the ECC mode bits equal hex 4, the ECC circuits are conditioned to transfer the sub-block and block ECC bytes to the serdes registers to be written on the disk. These ECC bytes are written behind the last sub-block of data that is received from storage control.

ECC Mode Bits = Hex 5 (Read Data)

While the ECC mode bits equal hex 5, the ECC circuits are conditioned to receive the data and fill character bytes, from the selected device, (read data transfer) and to process these bytes to calculate the sub-block and block ECC data.

ECC Mode Bits = Hex 6 (Read Sub-Block ECC)

The ECC mode bits are changed to a hex 6 immediately after the last byte of data is read in from a sub-block (not the last sub-block). This sets up the ECC circuits to read the sub-block ECC bytes and prevents them from being sent to the storage control.

ECC Mode Bits = Hex 7 (Read Sub-Block and Block ECC)

The ECC mode bits are changed to a hex 7 immediately after the last byte of data is read in from the last sub-block of data. This sets up the ECC circuits to read the sub-block ECC bytes and the block ECC bytes, preventing them from being sent to the storage control.

ECC Mode Bits = Hex 8 (Initialize RAM)

While the ECC mode bits equal hex 8, the ECC circuits are conditioned to initialize the 256 byte ECC Ram storage. This is done during the power on sequence, error recovery and after a read in preparation for the next operation.

ECC Mode Bits = Hex 9 (Correction Generation)

The ECC mode bits are set to a hex 9 if, after the last sub-block has been read, there has been a sub-block data check (does not have to be the last sub-block). This causes the ECC circuits to go through the correction generation routine. This routine prepares the ECC correction data that will be sent to the storage control when it issues the Sense ECC command.

ECC Mode Bits = Hex A (Transfer Correction Data)

While the ECC mode bits equal hex A, the ECC circuits are conditioned to send 256 bytes of error correction data to the storage control.

ECC Mode Bits = Hex C (Transfer Correction Data - ICKDSF)

ECC mode bits equal to a hex C is the same as ECC mode bits equal to a hex A, when ICKDSF is being used. This is to facilitate a more indepth data check report.

ECC Mode Bits = Hex D (Correction Generation - ICKDSF)

ECC mode bits equal to a hex D is the same as ECC mode bits equal to a hex 9, when ICKDSF is being used. This is to facilitate a more indepth data check report.

ECC Mode Bits = Hex E (Read Sub-Block ECC - ICKDSF)

ECC mode bits equal to a hex E is the same as ECC mode bits equal to a hex 6, when ICKDSF is being used. This is to facilitate a more indepth data check report.

ECC Mode Bits = Hex F (Read Sub-Block and Block ECC - ICKDSF)

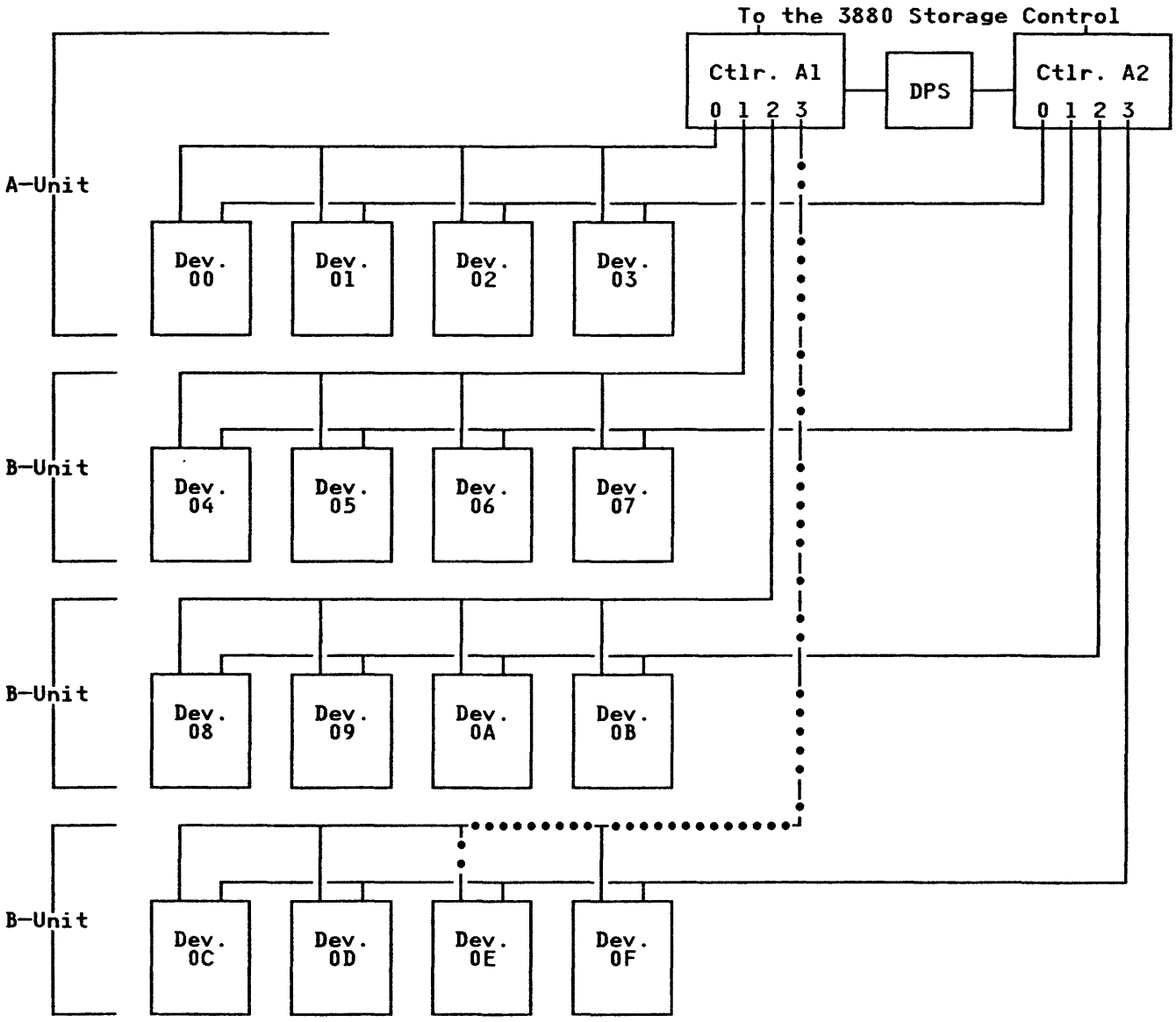
ECC mode bits equal to a hex F is the same as ECC mode bits equal to a hex 7, when ICKDSF is being used. This is to facilitate a more indepth data check report.

Selection — De-Selection — Polls

The device selection process connects the storage control, a controller, and a device (through the controller) such that commands from the storage control can be executed by the selected controller and/or device. While the controller and device are selected, the controller limits outbound communications to only one port in the device interface, and only the selected device on the port is enabled to respond.

The controller-only selection process connects the storage control and the controller such that the controller can execute commands from the storage control, but no port in the device interface is selected and no device is enabled to respond.

In the following figure, the dotted lines represent the communications paths that are in use while device E is selected in a string with dynamic path selection (DPS). (2 -Path configuration attached to a 3880). While one controller is connected to device E, the other controller can be used to select any other device in the string. The selection processes are described relative to the tag sequences.

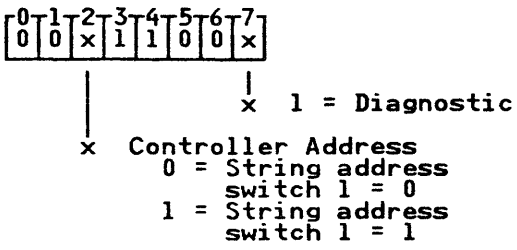


Controller-Only Selection

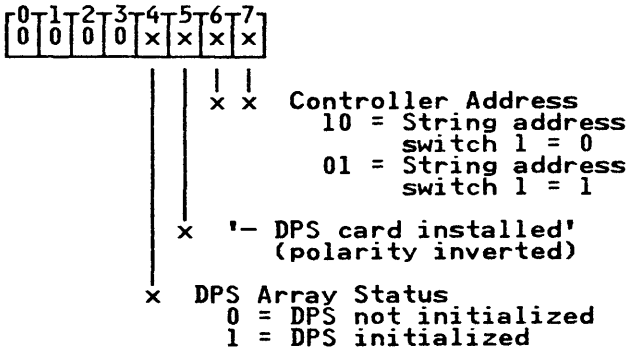
The following figure shows the tag sequence for controller-only selection. The comment numbers in the figure identify comments on page OPER-68. Keys **[A]** and **[B]** represent the formats of bytes transferred during selection. Bit positions not identified by an X in these figures are usually zeros.

Controlled by the Storage Control		Controlled by the Controller		
Control Interface				
DDC Tag Out	DDC Byte 0	DDC Byte 1	DDC Tag In	Comment Number
(000)			(00)	1
	[A]			2
001				3
		[B]		4
			01	5
011				6
			11	7
(011)			(11)	8

[A] Selection Address



[B] Initial Response



Comments for Controller Only Selection

1. Status before selection.

2. Storage control sets the selection address on DDC byte 0. Circuits in the DDC/DTB card compare bit 2 in the selection address with switch 1 of the String Address Switches. Switch 1 controls the '- ctr I adr 0/+ ctr I adr 1' signal to the IOCC card. (a down level for string 0 and an up level for string 1) When bit 2 and switch 1 are the same, the circuits activate the '+ controller adr valid' signal (the following sequence continues for the addressed controller).

3. Storage control changes tag out to Select. The following conditions are then detected by the IOCC card:

   a. The DDC tag out lines are changed from Null to Select
   b. The '+ controller adr valid' line is active
   c. The '+ seq controls DDC/CDP' line is inactive
   d. Selection address bits 3 and 4 are active.

   These concurrent conditions cause the CDP tag out lines to change to Null (000) on all ports and the controller selected latch to be set, activating the '+ selected' line.

4. At 'TX' time in the transfer clock cycle, the selection response byte is set in register 01 (in the IOCC card) and sent in on DDC byte 1. Bits 0 through 3 in the response byte are from bits 0 through 3 on the CDP data bus for port 0 and have no meaning to the storage control. Bits 4 through 7 are the status of the following lines.

   Bit 4 '+ primary array initialized'
   Bit 5 '- DPS card installed' (polarity inverted)
   Bit 6 '- ctr I adr 0/+ ctr I adr 1' (polarity inverted)
   Bit 7 '- ctr I adr 0/+ ctr I adr 1'

5. Valid Tag In is forced.

6. The storage control sends Select Null.

7. The Controller returns Selected Null.

8. Status after selection.

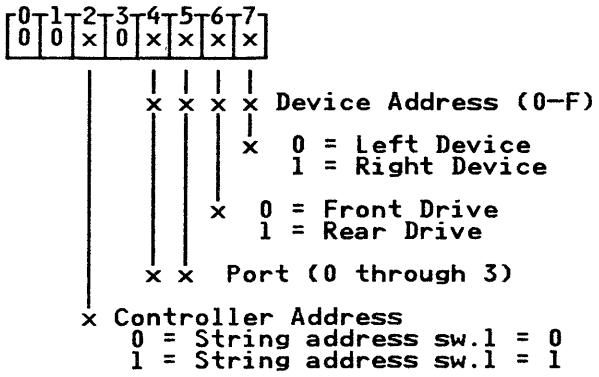
Device Selection With DPS

The following figure shows the tag sequence for a device selection on a 3380-JK with the DPS card installed. A 3380-JK with the DPS feature is only installed in a 2-Path configuration (single CDP card) to a 3880 0 storage control. The comment numbers in the figure are identified on page OPER-70.

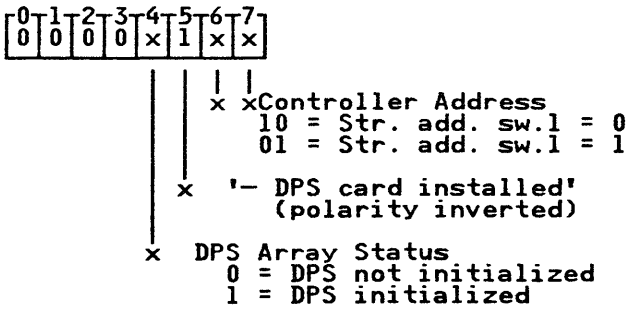
The comments describe some of the actions that occur in the tag sequence. The keys **[A]** through **[F]** represent the formats of bytes transferred during selection. Bit positions not identified by an 'X' in these figures are usually zeros.

Controlled by the Storage Control		Controlled by the Controller		Device Controlled			
Control Interface				Device Interface			
DDC Tag Out	DDC Byte 0	DDC Byte 1	DDC Tag In	CDP Tag Out	CDP Data Bus	CDP Tag In	Comment Number
(000)			(00)	(100)			1
	[A]						2
001				000		00	3
					[A]		4
		[B]					5
			01				6
011							7
			11				8
	[C]						9
001							10
		[D]					11
			01				12
011							13
			11				14
	hex 00						15
001							16
				001			17
					[E]		18
						01	19
		[F]					20
			01				21
011							22
				011			23
						11	24
			11				25
(011)			(11)	(011)		(11)	26

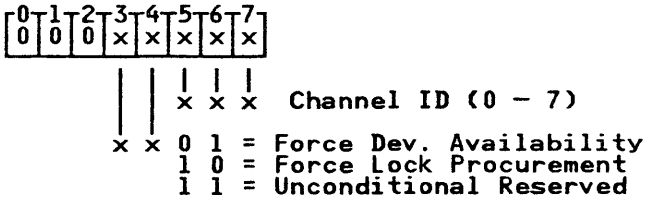
[A] Selection Address



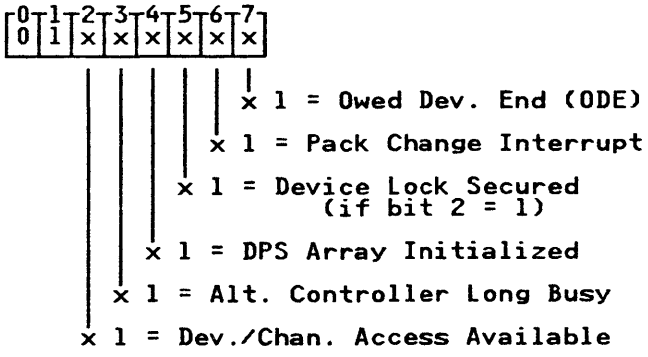
[B] Initial Response



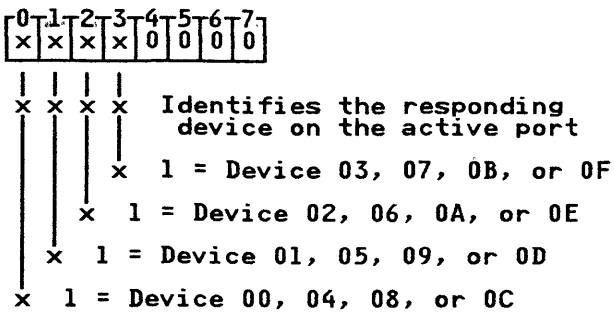
[C] Channel Address



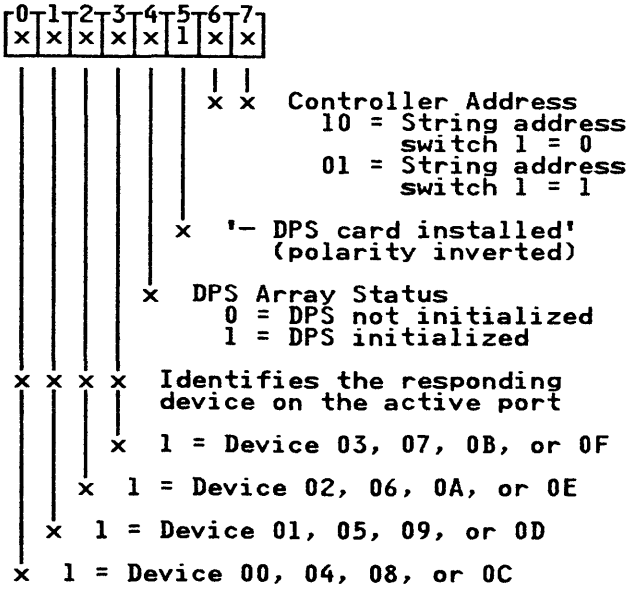
[D] DPS Response



[E] Device Response



[F] Controller Response



Comments for Device Selection with DPS

1. Status before selection (Device interface in poll condition).

2. The storage control sets selection of the address on DDC Bus Out Byte 0.

   Circuits in the DDC/DTB card compare the status of bit 2 in the selection address with the status of the String Address Switch 1, which controls the state of the '- ctr l adr 0/+ ctr l adr 1 signal. This signal is in the down state for string 0 and in the up state for string 1. If the state of the bit and the switch match, the circuits activate the '+ controller adr valid' signal (and the following sequence continues only for the addressed controller).

3. The following conditions are then detected by the IOCC card:

   a. The DDC Tag Out lines change from the Null state to the Select state
   b. The '+ controller adr valid' signal is active
   c. The '+ seq controls DDC/CDP' signal is not active
   d. Bit 3 in the selection address is not active
   e. The '- DPS card installed' signal is active

   These concurrent conditions cause the following:

   a. The CDP tag out lines change to the Null state
   b. The '- DPS command' signal becomes active
   c. The Controller selected latch is set, activating the '+ selected' signal

4. With the '+ controller adr valid' and the '+ selected' signals both active and the DDC Tag Out lines in the Select state, the selection address is gated onto the CDP Bus Out lines at TW time. The CDP card does nothing with the selection address at this time.

5. Circuits in the IOCC card load an initial selection response into register 01 and then onto DDC Bus In Byte 1 bus to the storage control. Bits 4 through 7, of the response, are the status of the following lines.

   Bit 4 = '+ primary array initialized'
   Bit 5 = '- DPS card installed' (polarity inverted)
   Bit 6 = '- ctr l adr 0/+ ctr l adr 1 (polarity inverted)
   Bit 7 = '- ctr l adr 0/+ ctr l adr 1

6. The DPS card stores the selection address from DDC byte 0, and then sends a Valid to the Tag In circuits. The Valid is transferred to the DDC Tag In lines via the feedthrough path at TZ time in the transfer clock cycle.

   The storage control checks the response byte and (for this example) finds that the response is as expected; the correct controller responded, DPS is present, and the DPS array is initialized (meaning that the storage in the DPS card was loaded with information about the subsystem since the most recent power-on reset).

7. The storage control continues the sequence by changing the state of the DDC Tag Out lines to Selected Null.

8. The DPS card returns Selected Null, which transfers to the DDC Tag In lines at TZ time in the transfer clock cycle.

9. The storage control sends the channel address byte.

10. The data on the DDC Bus Out Byte 0 bus is validated by the storage control when it changes the DDC Tag Out lines to the Sync Out state.

    The DPS card, after receiving the channel address, checks the availability of the device to the identified channel. If the requested device is available and not in use through by the other controller, the DPS card activates bit 5 in the DPS response byte. This response also indicates whether a device end interrupt or a pack change interrupt is owed to the channel. The DPS card validates the response with a Valid Tag In.

11. The response byte is loaded in register 01 (in the IOCC card) at TX time in the transfer clock cycle.

12. The Valid Tag In transfers to the DDC at TZ time in the transfer clock cycle.

13. The storage control continues the sequence by changing the DDC Tag Out lines back to the Selected Null state.

14. The DPS card returns Selected Null, which transfers to the DDC Tag In lines at TZ time in the transfer clock cycle.

15. Because the response indicated that the requested device is available, the storage control puts hex 00 on the DDC Bus Out Byte 0.

16. The data on the DDC Bus Out Byte 0 bus is again validated by the storage control when it changes the DDC Tag Out lines to the Sync Out state.

The DPS card activates the '+ DPS op complete' signal, which causes the activation of the '+ allow selection' signal and the deactivation of the '- DPS command' signal. The transfer of the byte on DDC Bus Out Byte 0 to the CDP Bus Out lines is inhibited, the CDP bus still has the selection address on it. The Select state on the DDC Tag Out lines is transferred to the CDP Tag Out lines at TZ time in the transfer clock cycle.

17. When the Select is detected by the CDP card, the following occurs:

    a. Using bits 4 and 5 in the selection address, the CDP card activates the selected port.
    b. The selection address is gated onto the selected ports '+ CDP bi-di data bus.
    c. The '+ CDP Tag Out bits' lines are changed to the Select state.
    d. Circuits in the Port R/W Control cards (in the devices connected to the selected port) compare the states of bits 6 and 7 in the selection address with the status of the "hard wired" address bits on the device's logic board. The device where both comparisons are equal and it is not already selected, the Port R/W Control card activates the '- device selected' signal.

18. The selected device generates a selection response that identifies which device has responded on the selected port (bits 0 through 3). This response is sent to the controller on the CDP bi-di data bus. The '+ device driver active' line is activated by the Port R/W Control card to inhibit the CDP bi-di data bus drivers in the controller during the inbound response.

19. The Port R/W Control card changes the state of the CDP Tag In lines to Valid.

20. The Valid Tag In from the device and the active '+ allow selection' signal sets the device selected latch on the IOCC card. This latch can be tested by the controller sequencer and it also enables circuits in the IOCC card to recognize an End Op (10) tag in from a device as an error.

    At TX time, in the transfer clock cycle, circuits in the IOCC card load bits 0 through 3, from the response byte on the CDP data bus, into bits 0 through 3 of register 01. The circuits concurrently load the status of the following lines into bits 4 through 7 of register 01:

    Bit 4 = '+ primary array initialized'
    Bit 5 = '- DPS card installed' (polarity inverted)
    Bit 6 = '- ctr l adr 0/+ ctr l adr 1 (polarity inverted)
    Bit 7 = '- ctr l adr 0/+ ctr l adr 1

    The contents of register 01 are gated on to DDC Bus In Byte 1.

21. The state of the CDP Tag In lines (Valid) is then gated on to the DDC Tag In lines, at TZ time in the transfer clock cycle.

22. The storage control responds to the Valid and the controller response byte, by changing the state of the DDC Tag Out lines to Selected Null.

23. The Selected Null state is transferred to the CDP Tag Out lines at TZ time in the transfer clock cycle (feedthrough path).

24. Upon detection of the Selected Null, the selected device deactivates the '+ device driver active' signal, enabling the CDP data bus drivers in the controller again. The device also changes the CDP Tag In lines to the Selected Null state.

25. The state of the CDP Tag In lines are transferred to the DDC Tag In lines via the feedthrough path at TZ time in the transfer clock cycle.

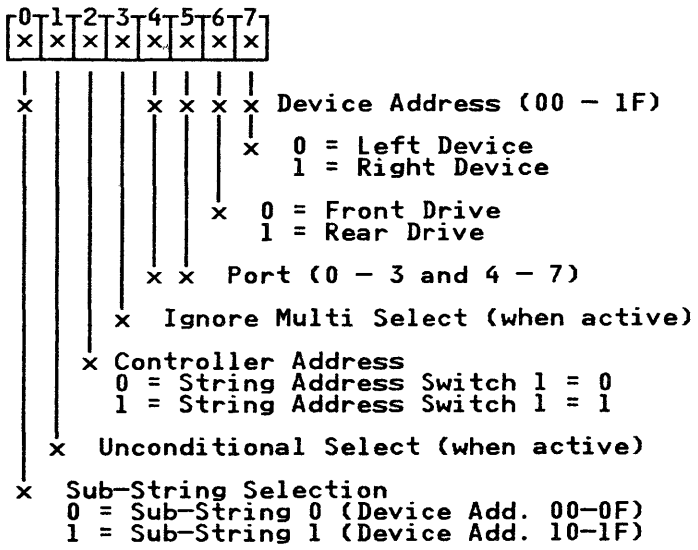
26. Status after device selection.

Device Selection Without DPS

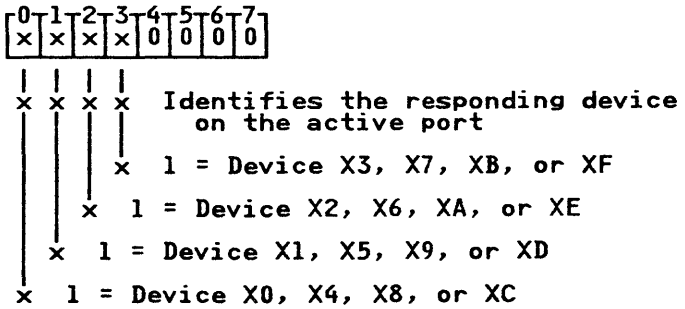
The following figure shows the tag sequence for device selection when the DPS card is not installed (Both 2-Path and 4-Path configuration, attached to a 3990 storage control). The comment numbers in the figure identify comments on OPER-73. The comments describe some of the actions that occur in the tag sequence. The keys **[A]** through **[C]** represent the formats of bytes transferred during selection. Bit positions not identified by an X in these figures are usually zeros.

Controlled by the Storage Control	Controlled by the Controller			Controlled by the Device			
Control Interface				Device Interface			
DDC Tag Out	DDC Byte 0	DDC Byte 1	DDC Tag In	CDP Tag Out	CDP Data Bus	CDP Tag In	Comment Number
(000)			(00)	(100)			1
	[A]						2
001				000		00	3
					[A]		4
				001			5
					[B]		6
						01	7
		[C]					8
			01				9
011							10
				011			11
						11	12
			11				13
(011)			(11)	(011)		(11)	14

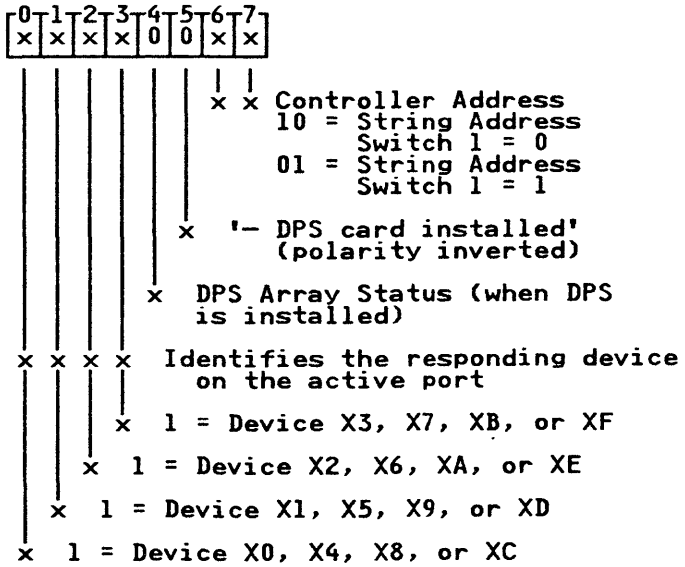
[A] Selection Address



[B] Device Response



[C] Controller Response



Comments for Device Selection Without DPS

1. Status before selection (Device interface in poll condition).

2. The storage control sets selection of the address on DDC Bus Out Byte 0.

   Circuits in the DDC/DTB card compare the status of bit 2 in the selection address with the status of the String Address Switch 1, which controls the state of the '- ctr l adr 0/+ ctr l adr 1' signal. This signal is in the down state for string 0 and in the up state for string 1. If the state of the bit and the switch match, the circuits activate the '+ controller adr valid' signal (and the following sequence continues only for the addressed controller).

3. The following conditions are then detected by the IOCC card:

   a. The DDC Tag Out lines change from the Null state to the Select state
   b. The '+ controller adr valid' signal is active
   c. The '+ seq controls DDC/CDP' signal is not active
   d. Bit 3 in the selection address is not active
   e. The '- DPS card installed' signal is not active

   These concurrent conditions cause the following:

   a. The CDP Tag Out lines change to the Null state
   b. The '+ allow selection' signal is activated
   c. The Controller selected latch is set, activating the '+ selected' signal

4. With the '+ controller adr valid' signal and the '+ selected' signal both active and the DDC Tag Out lines in a Select state, the selection address transfers onto the CDP Bus Out lines at TW time in the transfer clock cycle.

5. The Select Tag Out state is transferred to the CDP Tag Out lines at TZ time in the transfer clock cycle. This Tag Out change causes the following:

   a. In a 4-Path configuration (two CDP cards), the state of bit 0 in the selection address

selects which CDP card uses the selection address. Bit 0 being inactive (0) selects the CDP card that handles ports 0 through 3. In the active state (1) the CDP card that handles ports 4 through 7 is selected. In a 2-Path configuration (one CDP card), bit 0 will be inactive (0).

b. Using bits 4 and 5 in the selection address, the CDP card activates the selected port.
c. The selection address is gated onto the selected ports '+ CDP bi-di data bus.
d. The '+ CDP Tag Out bits' lines are changed to the Select state.
e. Circuits in the Port R/W Control cards (in the devices connected to the selected port) compare the states of bits 6 and 7 in the selection address with the status of the "hard wired" address bits on the device's logic board. The device where both comparisons are equal and it is not already selected, the Port R/W Control card activates the '- device selected' signal.

6. The selected device generates a selection response that identifies which device has responded on the selected port (bits 0 through 3). This response is sent to the controller on the CDP bi-di data bus. The '+ device driver active' line is activated by the Port R/W Control card to inhibit the CDP bi-di data bus drivers in the controller during the inbound response.

7. The Port R/W Control card changes the state of the CDP Tag In lines to Valid.

8. The Valid Tag In from the device and the active '+ allow selection' signal sets the device selected latch on the IOCC card. This latch can be tested by the controller sequencer and it also enables circuits in the IOCC card to recognize an End Op (10) Tag In from a device as an error.

   At TX time, in the transfer clock cycle, circuits in the IOCC card load bits 0 through 3, from the response byte on the CDP data bus, into bits 0 through 3 of register 01. The circuits concurrently load the status of the following lines into bits 4 through 7 of register 01:

   Bit 4 = '+ primary array initialized' (will be inactive)
   Bit 5 = '- DPS card installed' (will be inactive)
   (polarity inverted)
   Bit 6 = '- ctr l adr 0/+ ctr l adr 1
   (polarity inverted)
   Bit 7 = '- ctr l adr 0/+ ctr l adr 1

   The contents of register 01 are gated on to DDC Bus In Byte 1.

9. The state of the CDP Tag In lines (Valid) is then gated on to the DDC Tag In lines, at TZ time in the transfer clock cycle.

10. The storage control responds to the Valid and the controller response byte, by changing the state of the DDC Tag Out lines to Selected Null.

11. The Selected Null state is transferred to the CDP Tag Out lines at TZ time in the transfer clock cycle (feedthrough path).

12. Upon detection of the Selected Null, the selected device deactivates the '+ device driver active' signal, enabling the CDP data bus drivers in the controller again. The device also changes the CDP Tag In lines to the Selected Null state.

13. The state of the CDP Tag In lines are transferred to the DDC Tag In lines via the feedthrough path at TZ time in the transfer clock cycle.

14. Status after device selection.

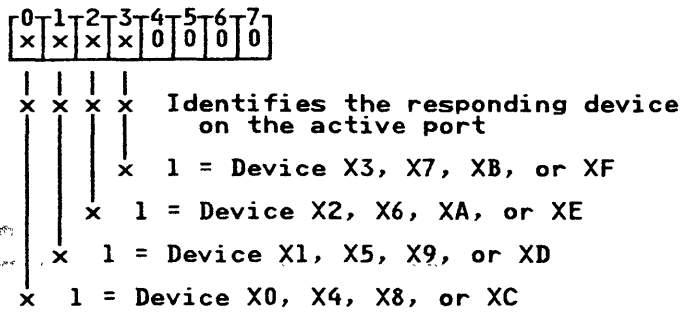
Device De-Selection

The following figure shows the tag sequence for device de-selection. The comment numbers in the figure identify comments on page OPER-77. The comments describe some of the actions that occur in the tag sequence.

Key **[A]** represents the format of the byte that is transferred during de-selection. Bit positions not identified by an X in these figures are usually zeros.

Controlled by the Storage Control		Controlled by the Controller			Controlled by the Device		
Control Interface				Device Interface			
DDC Tag Out	DDC Byte 0	DDC Byte 1	DDC Tag In	CDP Tag Out	CDP Data Bus	CDP Tag In	Comment Number
(011)			(11)	(011)		(11)	1
001							2
							3
				001			4
					[A]		5
						01	6
		[A]					7
			01				8
000				000			9
			00	100			10
(000)			(00)	(100)			11

[A] Device Response



Comments for Device De-Selection

1. Status before de-selection.

2. Storage control changes the state of the DDC Tag Out lines to Sync Out.

3. The byte on DDC byte 0 transfers on the feedthrough path, at TW time of the transfer clock cycle, to the CDP Bus Out bus.

4. The DDC Tag Out state is transferred to the CDP Tag Out lines at TZ time of the transfer clock cycle.

5. The Port R/W Control card in the selected device prepares the device response, which is sent in on the CDP bi-di data bus. The response is based on which device on the 'B' board is selected. The location of the Port R/W Control card determines which bit is activated within the response byte.

   Bit 0 = Front Left Device
   Bit 1 = Front Right Device
   Bit 2 = Rear Left Device
   Bit 3 = Rear Right Device

   The '+ device driver active' line is activated by the Port R/W control card to inhibit the CDP data bus drivers in the controller during the inbound response.

6. The selected device changes the state of the CDP Tag In lines to a Valid.

7. The response byte is transferred on the feedthrough path at TW time to the DDC Bus In Byte 1.

8. The Valid tag is transferred on the feedthrough path to the DDC Tag In lines at TZ time of the transfer clock cycle.

9. The storage control changes the DDC Tag Out lines to the Null Disconnect state. A Null Disconnect tag out state causes the following actions in the controller:

   a. The controller selected latch is reset, deactivating the '+ selected' signal.

   b. The CDP Tag Out lines changes to the Null Disconnect, resetting the '+ device selected' signal in the Port R/W Control card of the selected device.

10. At the next TZ time in the transfer clock cycle, the following changes occur:

    a. The '+ allow selection' signal is deactivated.

    b. The device selected signal (internal to the IOCC card) is deactivated.

    c. The CDP Tag Out lines are forced to the Poll state on all ports.

    d. The Null Disconnected tag is returned to the storage control.

11. Status after de-selection.

Polls

Polling is initiated by the storage control to collect interrupt status. A complete polling sequence for the 3380-JK contains twelve poll cycles, permitting the collection of status from two strings of up to 32 devices.

Each poll cycle is identified by a poll code, which identifies the controller (string 0 or 1) and assigns meaning to the collected information.

During polling, the controller identified by the poll code formats the response bits in a byte that is sent to the storage control on the DDC byte 1 bus. The controller is identified by the high-order half-byte of the poll code, and the status that is wanted is identified by the low-order half-byte.

Figure 5 on OPER-79 shows the poll codes for the twelve poll cycles. Figure 5 also identifies the information collected during each poll cycle. Figures 1, 2, 3, and 4, located in front of figure 5, identifies the format and bit meaning for the responses. It should be understood that an active interrupt from a device does not identify the cause of the interrupt in the device. To determine the cause of an interrupt, the storage control analyzes the response to a Sense Device Status 1 command.

Use the the following OPER pages for more information about Polls:

- OPER-80 - The normal tag sequence for a poll cycle.
- OPER-81 - A description of the functions of the CDP card (in the controller) during poll cycles.
- OPER-81 - A short description of the device functions relative to polls.
- OPER-82 - A list of causes for interrupts from the devices.

A Poll tag out on the device interface is a normal default condition from a controller on device interface ports that are not in use with a selected device (or selecting one). However, a device in use through one controller does not respond to the Poll tag from the controller on the other device interface.

Figure 1. Response to Hex x1, x3, xB, xD Poll Code

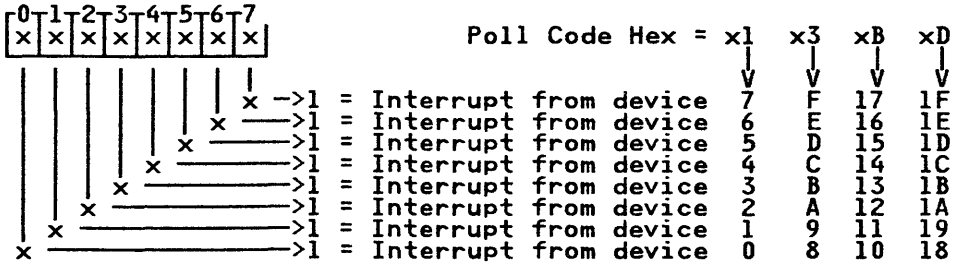


Figure 2. Response to Hex x5 Poll Code - 2 Path with DPS Installed

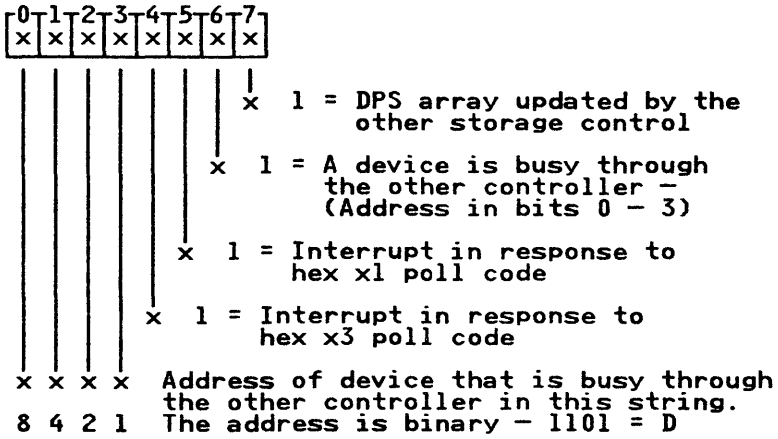


Figure 3. Response to Hex x5 Poll Code — 2 Path without DPS and 4 Path

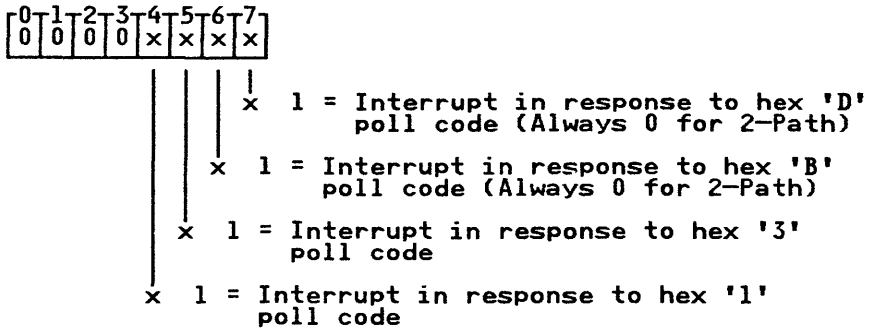


Figure 4. Response to Hex x7 Poll Code

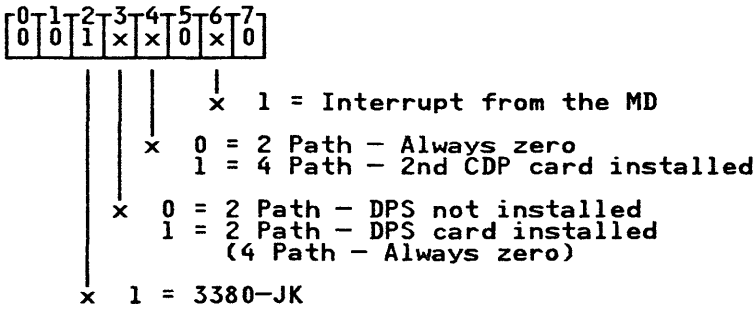


Figure 5. Poll Codes and the Status Collected

Poll Code (In Hex)	2-Path With DPS card installed	2-Path without DPS installed	4-Path
x1	Interrupt status from Devices 0 through 7 (See figure 1)	Interrupt status from Devices 0 through 7 (See figure 1)	Interrupt status from Device 0 through 7 (See figure 1)
x3	Interrupt status from devices 8 through F (See figure 1)	Interrupt status from devices 8 through F (See figure 1)	Interrupt status from devices 8 through F (See figure 1)
xB	Not Used	Not Used	Interrupt status from devices 10 through 17 (See figure 1)
xD	Not Used	Not Used	Interrupt status from devices 18 through 1F (See figure 1)
x5	Device busy, DPS array status and summary interrupt status - all devices (See figure 2)	Summary interrupt status for devices 00 through 0F (See figure 3)	Summary interrupt status for devices 00 through 1F (See figure 3)
x7 A	MD interrupt status (See figure 4)	MD interrupt status (See figure 4)	MD interrupt status (See figure 4)

x = 0 = String '0' controller
2 = String '1' controller

Poll Cycle Tag Sequence

The following chart shows the tag sequence that occurs during a poll cycle. The events occur in order from the top of the chart toward the bottom. The comments describe some of the actions that occur in the tag sequence.

Poll Tag Sequence Chart

Controlled by the Storage Control		Controlled by the Controller			
				Device Interface	
Control Interface					
DDC Tag Out	DDC Byte 0	DDC Byte 1	DDC Tag In	CDP Tag Out	Comment Number
(000)			(00)	(100)	1
	Poll Code				2
					3
100					4
					5
		Response Byte	01		6
000					7
			00		8
(000)			(00)	(100)	9

The following are comments that accompany the tag sequence shown on the above, Poll Tag Sequence Chart. The numbers relate to the steps in the tag sequence.

1. Status before a poll cycle.

2. The storage control sends the poll code. Figure 5 on OPER-79 shows the twelve poll codes that are used in a complete poll sequence.

3. Circuits in the DDC/DTB card (in the controllers) compare the status of bit 2 in the poll code with the state of switch 1 of the String Address Switches. Switch 1 controls the state of the '- ctr l adr 0/+ ctr l adr 1' signal to the IOCC card. String 0 will have the switch in the 'close' position and the signal at the down (minus) level. String 1 will have the switch in the 'open' position and the signal at the up (plus) level. If the status of poll code bit 2 and the state of string address switch 1 are the same, the DDC/DTB circuits activate the '+ controller adr valid' line, to the IOCC card.

4. The storage control changes the tag to Poll (100).

5. The input conditions that are detected by the IOCC card at this time are as follows:

   - The DDC Tag out change, from a Null Disconnect to a Poll.

- The '+ controller adr valid' line active from the DDC/DTB card.

- The 'seq controls DDC/CDP' bit has not been activated by sequencer.

- Bit 7 in the poll code = 1.

With the above conditions and at TX time in the transfer clock cycle, the poll code, on DDC Bus byte 0, is sent to the CDP card over the CDP Bus Out lines. At the same time, the Controller selected latch sets, activating the '+ selected' signal.

6. At TY time in the transfer clock cycle, the following events occur:

   - The response byte, from the CDP card, is loaded into register 01, in the IOCC card, and then transferred onto the DDC Bus In Byte 1, to the storage control.

   - The DDC Tag In lines are forced to a Valid (01) state.

7. The storage control responds by changing the DDC Tag Out lines to a Null Disconnect state.

8. The Null Disconnect Tag Out resets the controller selected latch, deactivating the '+ selected' signal. A Null Disconnected (00) Tag In is returned to the storage control.

9. Status after the poll cycle.

CDP Card Functions During Poll Cycles

During polls, the CDP card (in the controller) collects and formats the response byte. To perform these functions, circuits in the CDP card:

- Decode the Poll tag on the '+ CDP Tag Out 0, 1 and 2' lines. These lines come from DDC interface, through the feedthrough circuitry on the IOCC card.

- Decode the Poll code on the '+ CDP Bus Out' lines. Again, these come from the DDC interface, through the feedthrough circuitry on the IOCC card.

The Poll code, on the CDP Bus Out lines, identifies the following:

Normal Poll

1. The CDP card containing the selected group of devices (4-Path).
2. The two ports within the selected CDP card.
3. The response that is put together from the + CDP Bidirectional Data 0, 1, 2, and 3 lines from the two selected ports.

Summary Poll

1. No card or port selection is required. The response uses both cards (if installed) and all ports.
2. The summary poll response reports the following:
   a. All active interrupts by port pairs (examples: 0 and 1, 2 and 3, 6 and 7)
   b. **(DPS installed only)** If a device is selected by the other controller; its address is identified (this is done by monitoring the the '+ alternate device adr 0 through 3' and the '+ alternate device busy' signals - from the DPS card).
   c. **(DPS installed only)** The DPS array status ('+ alert' signal)

MD Poll

1. No card or port selection is required, the response comes from the CDP with the low numbered ports (0 through 3).
2. The MD poll response reports whether the '+ maint dev interrupt request' signal is active from the MD Adapter card. On a 2-Path configuration, it will report whether the DPS card is installed. On a 4-Path configuration, the CDP card reports whether the 2nd CDP card is installed.

Device Functions During Polls

While the tag out to a device is in the Poll (100) state, the device Port R/W Control card reports the device interrupt status to the controller.

For reporting interrupt status, during polls, each device is assigned a line in the CDP data bus. The line is assigned by where the Port R/W Control card is located in the device ('B') board.

The interrupt status for every device is sent to the controllers on a different line, as shown in the following table:

	CDP Bi-Di Data Bus Bit →								
Port >	0	1	2	3	4	5	6	7	V
Devices > 0	0	4	8	C	10	14	18	1C	0
1	1	5	9	D	11	15	19	1D	1
2	2	6	A	E	12	16	1A	1E	2
3	3	7	B	F	13	17	1B	1F	3

For example, the chart shows that the interrupt status for device B is sent to the controllers on CDP data bit 3 of port 2.

When an interrupt signal is active, the Port R/W Control card activates the CDP bidirectional data bit line. The Tag In lines also change to the Valid state when an interrupt signal is active, but the Tag In lines, on the device interface, are not used in the collection of poll data.

Device Interrupts

The interrupt sent to the controller and reported to the storage control during the poll cycles can be caused by any of the following conditions:

- A seek operation, a rezero operation, or an offset operation (all previously started) has completed without errors.
- A seek operation, a rezero operation, or an offset operation was ended with an error.
- The drive motor power-on sequence has completed.
- A search sector operation was ended with an error.
- The desired sector (target sector) has been found in a sector search operation.
- Selection was attempted while the device was busy and it is now not busy.

3380-JK Commands

The figure on page OPER-83 contains all the commands for the 3380-JK from either the 3880 or the 3990 Storage Control. The commands are listed in command-code order.

The series of commands from the storage control to the 3380-JK is controlled by the storage control microcode, which is accommodating commands from the channel. There are two basic types of commands received from the storage control:

- Immediate commands
- Extended commands

For immediate commands, the director-to-device controller (DDC) interface remains in control mode while the command is processed. The tag sequence continues until the process ends. An End Op (Tag In) occurs only to indicate an error.

For extended commands, the DDC interface can change from control mode to transfer mode while the command is processed. When the process is completed, the DDC interface reenters control mode, and an End Op (Tag In) is generated to indicate the end of the process.

The End Op tag validates an end op code (inbound on the DDC byte 1 bus). For immediate commands, the end op code identifies the error. For extended commands, the end op code indicates either good or error status.

Immediate commands and extended commands are easily recognized by the status of bit 0 in the command code. See the following table:

Type of Command	***Command Byte 0 1 2 3 4 5 6 7***
Immediate	0 x x x x x x x
Extended	1 x x x x x x x

(x = do not care)

Extended commands are only valid while the subsystem is in extended mode.

Two commands change the mode. The Start Read/Write command changes the mode from immediate mode to extended mode. An End Read/Write command returns from extended mode to immediate mode.

Immediate Commands

Immediate commands are divided into device commands, Dynamic Path Selection (DPS) commands, and controller commands. These three kinds of commands can be recognized by the status of certain bits in the command code.

Type of Immediate Command	***Command Byte 0 1 2 3 4 5 6 7***
Device	0 1 x x x x x x
DPS	0 0 x x 1 x x x
Controller	0 0 x x 0 x x x

(x = do not care)

For more information on immediate commands, see the following:

- Device Commands OPER-94.
- DPS Commands OPER-101.
- Controller Commands OPER-91.

Extended Commands

Extended commands are only valid when the controller is in extended mode. While the controller is in extended mode, the controller sequencer directs the controller functions. The controller sequencer also directs the read/write actions of the drive.

The controller enters extended mode during the last part of the execution of a Start Read/Write command. A Start Read/Write command is issued by the storage control after device selection is completed and after the access mechanism is positioned to the correct cylinder for a read operation. The controller must return to immediate mode before the position of the access mechanism can be changed. While the controller is in extended mode, the CDP tags (both out and in) are normally at Selected Null (011 and 11) and the 'CDP split bus op' line is active. While the 'CDP split bus op' line is active, CDP data bus bits 0 through 2 are dedicated as inbound status lines,

Command Code In Hex	Command Name
08[1]	Copy Alternate DPS Array
09[1]	Terminate DPS Control
0A[1]	Inhibit DPS Device Lock Reset
0B[1]	Alert Processing Macro
10[2]	Sense Fault Log
11[2]	Sense Features
12[2]	Sense Storage Facility Config.
14[2]	Sense MD Data
15[2]	Sense EC Level
16[2]	Sense SF ID
17[2]	Sense Check-2 Register
18[1]	Sense DPS Status
19[1]	Read Alternate DPS Lock Status
1A[1]	Disconnected Chain Cleanup Macro
1B[1]	End CCW Cleanup Macro
1C[1]	Read Device Parameters Macro
20[2]	DDC Bus Out Diagnostic
22[2]	Start Read/Write
24[2]	Set MD Data Byte 1
25[2]	Set MD Data Byte 2
26[2]	Sense Controller Path
28[1]	Write DPS Array
2A[1]	Reset DPS Locks
2C[1]	Write Device Parameters Macro
30[2]	Wrap Bus
31[2]	Diagnostic Command
33[2]	Reset Allegiance
34[2]	Desel. Device & Reset Controller
38[1]	Read DPS Array
3A[1]	Set DPS Locks
3C[1]	Set Under Mask
3D[1]	Reset Under Mask
40[3]	Start Spindle Power On
43[3]	Reset Device Checks
44[3]	Seek and Verify No Guard Band (Model J)
46[3]	Seek, Sector Search and Verify No Guard Band (Model J)
48[3]	Seek and verify No Guard Band (Model K)
49[3]	Seek, Sector Search and Verify No Guard Band (Model K)
4A[3]	Reset Interrupts
4C[3]	Start Rezero
4D[3]	Load Path Interrupt Table
4F[3]	Start Spindle Power Off
50[3]	Sense Device Status 1
51[3]	Sense Power Status
52[3]	Gate Servo Status & Bump Pointer
53[3]	Sense Read/Write Status 1
54[3]	Sense Read/Write Status 2
55[3]	Sense Device Checks
56[3]	Sense Read/Write Status 3
57[3]	Sense Device Checkpoint Log
58[3]	Sense Device Status 2
59[3]	Seek Cylinder minus 3
5C[3]	Read HAR
5D[3]	Gate Servo Sta. & Reset Pointer
5E[3]	Controller CDP Parity Check Test
5F[3]	Force A Device Check 1
62[3]	Sector Search
63[3]	Set HAR
69[3]	Seek Cylinder minus 2
6A[3]	Seek Cylinder minus 4
6C[3]	Start Offset
6E[3]	Start Offset and Sector Search
70[3]	Start Diag. & Spec. Command Mode
71[3]	Select Servo Status 1 or 2
72[3]	Set Register Pointer

Command Code In Hex	Command Name
74[3]	Sense Read/Write Status 4
75[3]	Sense Path Interrupt Table
76[3]	Arm Device Interrupt
78[3]	Seek to Anywhere
79[3]	Sense GBOD or GBID
7A[3]	Seek to Anywhere & Sector Search
80[4]	Read
81[4]	Read 34 Bytes With No ECC
88[4]	Read - R*
89[4]	Read - A, R*
8C[4]	Read - L, R*
8E[4]	Read - H, L, R*
8F[4]	Read - O, L, R*
90[4]	Space From Index
91[4]	Space n Blocks of 16 Cells
92[4]	Space - 2
93[4]	Space - 3
94[4]	Space - 4
95[4]	Space - 5
96[4]	Space - 6
97[4]	Space - 7
98[4]	Space - 8
99[4]	Space - 9
9A[4]	Space - 10
9B[4]	Space - 11
9C[4]	Space - 12
9D[4]	Space - 13
9E[4]	Space - 14
9F[4]	Space - 15
A0[4]	Clock
A4[4]	Clock - L*
A7[4]	Clock - O, L*
C0[4]	Write
C1[4]	Write 34 Bytes With No ECC
C2[4]	Write - P
C3[4]	Format Write, 34 Bytes, No ECC and Auto Pad
C8[4]	Write - R*
CA[4]	Write - R, P*
CB[4]	Write - A, R, P*
CE[4]	Write - L, R, P*
D0[4]	Pad From Index
D1[4]	Pad To Index
D2[4]	Pad - 2
D3[4]	Pad - 3
D4[4]	Pad - 4
D5[4]	Pad - 5
D6[4]	Pad - 6
D7[4]	Pad - 7
D8[4]	Pad - 8
D9[4]	Pad - 9
DA[4]	Pad - 10
DB[4]	Pad - 11
DC[4]	Pad - 12
DD[4]	Pad - 13
DE[4]	Pad - 14
DF[4]	Pad - 15
E0[4]	Set HAR Oriented
E1[4]	End Read/Write
E2[4]	Sense ECC Bytes
E3[4]	Time Delay
E4[4]	Extended Diagnostic
E5[4]	End Read/Write Diagnostic
EC[4]	Set Diagnostic Read Mode
ED[4]	Modify Read Clip Level
F2[4]	Erase - P*
F6[4]	Erase - L, P*
FA[4]	Erase - R, P*
FE[4]	Erase - L, R, P*

* A = Address Mark
L = Long Sync
P = Pad Sync Area
H = Home Address
R = Reset ECC
O = Record Zero

[1] = DPS Command, [2] = Controller Command, [3] = Device Command, [4] = Extended Command

Figure 21. 3380-JK Commands

and CDP data bus bits 3 through 7 are dedicated as outbound control lines.

While the controller is in extended mode, the DDC interface operates in two modes, control mode and transfer mode. The interface is in control mode except when read or write data is being transferred or when the ECC correction bytes are being transferred to the storage control after a read error. During these transfers, the DDC interface is in transfer mode.

In control mode, the controller reports the status of a completed operation by sending an end-op code to the storage control on the DDC byte 1 bus and changing the DDC Tag In from Selected Null (11) to End Op (10). The controller normally maintains the DDC Tag In at End Op until the storage control sends the next command on DDC byte 0 and changes the DDC Tag Out from Selected Null (011) to Command Gate (111). When the Tag Out is Command Gate, the controller can change the DDC tag in from End Op (10) to Selected Null (11). With the Tag In at Selected Null, the storage control changes the DDC Tag Out from Command Gate (111) to Selected Null (011).

Both DDC tags (out and in) must be Selected Null when the DDC interface changes from control mode to transfer mode. When the DDC interface is in transfer mode, the direction of the DDC byte 0 and 1 buses is the same, both outbound for write operations and both inbound for read operations and ECC correction byte transfers. Two bytes are transferred simultaneously.

Each two-byte transfer over the DDC interface is validated by a tag sequence. (This tag sequence is not interlocked -- that is, a tag change in one direction does not have to be followed by a tag change in the other direction before another tag change can occur)

The controller starts the tag sequence in transfer mode by changing the DDC Tag In from Selected Null (11) to Sync In (01) and back to Selected Null. During write operations, each Sync In tag is a request for two bytes of data. During read operations, each Sync In tag validates two bytes of data on the DDC byte 0 and 1 buses.

The storage control responds to the Sync In tags from the controller. To respond, the storage control changes the DDC Tag Out from Selected Null (011) to Sync Out (001) and back to Selected Null. During write operations, each Sync Out tag validates two bytes of data outbound on the DDC byte 0 and 1 buses. During read operations, each Sync Out tag acknowledges the receipt of two bytes of data. When data is read from (or written to) the disk, the controller must be oriented; that is, the controller sequencer must be in step with the format of the track under the selected read/write head.

Orientation results from the recognition of either of two events: index or address mark. To get oriented, the controller sequencer (in response to a command) stops the controller clock ring several instructions after the event (index or address mark) is recognized. The next controller sequencer instruction is delayed until the clock ring is started by hardware. If the clock ring was stopped when the sequencer recognized index, the clock ring is started by the next cell boundary. If the clock ring stopped after an address mark, the clock ring starts when sync byte is found.

Orientation is maintained by the controller sequencer, which executes 16 instructions during each cell. Orientation is also maintained by the storage control, which issues the commands to accommodate the format of the track. While the subsystem is oriented, the system clock (controller clock) is synchronized to the speed of the disk (via signals from the servo surface or via the read data). Because the controller sequencer is in step with the track format, the sequencer initiates data transfers in transfer mode.

Although the controller sequencer remains in step with the track format, the storage control indicates when the controller sequencer must stop the transfer. (The storage control receives the lengths of the key or data area as part of the information in the count fields for each record. The length of a count field is fixed.)

The storage control calculates a transfer length that is usually longer than the data. The transfer length includes all the bytes from the first data byte through the last byte. The Error-Checking and Correction (ECC) bytes are not counted or sent to the storage control at the time of the data transfer.

The storage control decreases the transfer length by two bytes for each Sync In received in transfer mode. When 14 bytes remain to be transferred, the storage control responds to the Sync In with a Command Gate Tag Out. The Command Gate Tag Out received during transfer mode sets a stop latch in the controller. The controller sequencer tests the status of the stop latch twice each cell in transfer mode. When the stop latch is found set, the sequencer prepares to end transfer mode (prepares to stop sending Sync In tags) and gets ready for the next process.

The figure on page OPER-86 identifies the extended commands. The figure also indicates which commands are oriented commands and non-oriented commands. The oriented commands are valid only when the controller is oriented. The commands with an X in both the oriented and non-oriented columns are valid in either condition. The other extended commands are valid only when the controller is not oriented to the track format.

See OPER-50 for information on track format.

See OPER-13 for a description of the control (DDC) interface.

See OPER-54 for more information about control mode tag sequences for extended commands.

See OPER-58 and OPER-62 for details on transfer mode.

Read Commands

All read commands except one are oriented commands. The exception (Read-A,R) can be either oriented or non-oriented and can be used to orient the subsystem to the track format.

All read commands transfer the data that is read to the storage control in transfer mode. The data is also processed by the Error Checking and Correction (ECC) circuits to build the 6-byte sub-block and the 6-byte block ECC codes. The sub-block and block error checking and correction codes are compared with the same ECC bytes read from the disk to ensure valid data. The status of the read operation is reported via the end-op code, which signals the end of the operation.

The first byte of data is always immediately preceded by a two-byte sync byte pattern. During the read command process, the controller sequencer stops the clock ring, waiting for the sync byte pattern to be read. When the sync byte is read, the clock ring starts again. The next information available from the read/write head is the first byte of data.

As each pair of bytes is assembled, the bytes are sent to the storage control in transfer mode. The storage control initiates the end of transfer mode by responding to the Sync In (Tag In) with a Command Gate (Tag Out) when only 14 bytes are needed to complete the field.

The Read-A,R command can be used to achieve orientation. During the execution of the Read-A,R command, the controller sequencer tests for an address mark and also tests for index. If an address mark is found before index occurs, the count field immediately following the address mark is read. If index occurs before an address mark is found, the Tag In is changed to End Op (with index indicated in the end-op code on DDC byte 1). The controller sequencer then executes routines for the Space From Index command instead of reading a count field. (See OPER-88 for a description of the Space From Index command.)

The Read-H,L,R command, which reads the home address record, provides automatic skipping of defects. During the execution of this command, the controller clock is stopped waiting for the sync byte pattern. If the sync byte pattern is not found, the clock ring is started one cell later. The controller sequencer counts five more cells and again attempts to find the sync byte pattern. In all, the Read-H,L,R command tries to read the home address record up to four times, producing up to three 6-cell defect skips in the process.

See OPER-60 for the read paths.

See OPER-34 for the read/write controls for the read/write channel board.

Command Name	Command Code in Hex	Non-Oriented Command	Oriented Command	Execution Includes Transfer Mode	Outbound Parameters	Response Bytes
Read	80		X	X	–	Data (Variable)
Read 34 Bytes With No ECC	81		X	X	–	Data (34)
Read-R	88		X	X	–	Data (Variable)
Read-A,R	89	X	X	X	–	–
Read-L,R	8C		X	X	–	Data (40)
Read-H,L,R	8E		X	X	–	Data (40)
Read-O,L,R	8F		X	X	–	Data (40)
Space From Index	90	X			–	–
Space n Blocks of 16 Cells	91		X		Number of Blocks	–
Space 2	92		X		–	–
Space 3	93		X		–	–
Space 4	94		X		–	–
Space 5	95		X		–	–
Space 6	96		X		–	–
Space 7	97		X		–	–
Space 8	98		X		–	–
Space 9	99		X		–	–
Space 10	9A		X		–	–
Space 11	9B		X		–	–
Space 12	9C		X		–	–
Space 13	9D		X		–	–
Space 14	9E		X		–	–
Space 15	9F		X		–	–
Clock	A0		X	X	Data (Variable)	–
Clock-L	A4		X	X	Data (Variable)	–
Clock-O,L	A7		X	X	Data (Variable)	–
Write	C0		X	X	Data (Variable)	–
Write 34 Bytes With No ECC	C1		X	X	Data (34)	–
Write-P	C2		X	X	Data (Variable)	–
Format Write, 34 Bytes, No ECC and Auto Pad	C3		X	X	Data (34)	–
Write-R	C8		X	X	Data (Variable)	–
Write-R,P	CA		X	X	Data (Variable)	–
Write-A,R,P	CB		X	X	Data (40)	–
Write-L,R,P	CE		X	X	Data (40)	–
Pad From Index	D0	X			–	–
Pad To Index	D1		X		–	–
Pad 2	D2		X		–	–
Pad 3	D3		X		–	–
Pad 4	D4		X		–	–
Pad 5	D5		X		–	–
Pad 6	D6		X		–	–
Pad 7	D7		X		–	–
Pad 8	D8		X		–	–
Pad 9	D9		X		–	–
Pad 10	DA		X		–	–
Pad 11	DB		X		–	–
Pad 12	DC		X		–	–
Pad 13	DD		X		–	–
Pad 14	DE		X		–	–
Pad 15	DF		X		–	–
Set Head Address Oriented	E0		X		Head Address (1)	–
End Read/Write	E1	X	X		–	–
Sense ECC Bytes	E2	X			–	ECC Data (274)
Time Delay	E3	X			–	–
Extended Diagnostic	E4	X	X		Diag. Modifier	–
End Read/Write Diagnostic	E5	X	X		–	–
Set Diagnostic Read Mode	EC	X	X		–	–
Modify Read – Clip Level	ED		X	X	–	–
Erase-P	F2		X	X	–	–
Erase-L,P	F6		X	X	–	–
Erase-R,P	FA		X	X	–	–
Erase-L,R,P	FE		X	X	–	–

Figure 22. Extended Commands

Write, Clock, and Erase Commands

The processes caused by write, clock, and erase commands are similar. All three kinds of commands:

- are oriented commands
- change from control mode to transfer mode for data transfer

The basic differences between the processes for these commands are what is done with the data that is received from the storage control.

Write commands cause the data to be written on the disk. The data is also processed by the ECC circuits to build the 6-byte sub-block and 6-byte block Error-Checking and Correction (ECC) bytes.

Clock commands cause nothing to be written on the disk. The Sync In/Sync Out tag sequence occurs the same as for write commands, but the data is not processed by the ECC circuits or sent to the access mechanism.

Erase commands write pad characters instead of the transferred data. Pad characters are also written in the ECC areas.

See OPER-57 for the write paths.

See OPER-26 for clock synchronization during write operations.

See OPER-34 for the read/write controls for the read/write channel board.

Pad Commands and Space Commands

Pad commands and space commands are similar in that they are used to build and process gaps. The execution of these commands does not include the use of transfer mode.

The major differences during the execution of pad commands and space commands are the serdes controls and the controls for the Read/Write Channel board. During the execution of pad commands, the controller sequencer sets the write controls for the Read/Write Channel board and sets the serdes mode bits to supply pad characters from the serdes circuits.

During the execution of space commands, the controller sequencer sets read controls for the Read/Write Channel board and sets the serdes mode bits to keep the serdes circuits reset.

All pad commands except one and all space commands except one are oriented commands, which are valid only while the controller is oriented to the track format. The non-oriented pad and space commands are Pad From Index (Hex D0) and Space From Index (Hex 90).

Pad from Index and Space from Index Commands

These two commands are used to achieve orientation to index. Both commands process the first eight cells of the track (including the cell in which index occurs).

The following describes the sequence of events for both Pad From Index and Space From Index commands.

1. Index occurs and is recognized by the controller sequencer (see OPER-30).
2. The controller sequencer reports index to the storage control via an End Op tag (see OPER-30). The End Op tag in is retained, but the controller sequencer does not check the status of the DDC Tag Out lines for a Command Gate tag until the end of the seventh cell.
3. The controller clock is synchronized to the second cell boundary after index occurs (see OPER-26).
4. The controller sequencer tests the status of the DDC Tag Out lines for a Command Gate Tag Out. The next command is expected during the eighth cell of the track.

Pad to Index Command

The Pad To Index command (Hex D1) has no counterpart space command. The Pad To Index command is an oriented command that writes pad characters (supplied by the serdes circuits in the controller) until index occurs. When index occurs, the controller sequencer:

1. Continues pad controls to the end of the cell in which index occurred, and then changes the Read/Write Channel board controls from write to read.

2. Reports index to the storage control via an End Op Tag In with an end op code on the DDC byte 1 bus.

3. Synchronizes the controller clock to a cell boundary (see OPER-26).

4. Tests the status of the DDC Tag Out lines for a Command Gate tag at the end of the seventh cell and during the eighth cell (The next oriented command is expected during the eighth cell of the track process).

Pad 2 Through 15 Commands and Space 2 Through 15 Commands

These commands are all oriented commands. The pad commands cause pad characters (supplied by the controller) to be written in the number of cells specified by the command name. Similarly, the space commands space past the number of cells specified by the command name.

The controller sequencer reports the completion of these pad and space operations by activating the End Op Tag In during the next-to-last cell affected by the command. For example, during the execution of a Space 5 command, the controller sequencer changes the Tag In from Selected Null to End Op early in the fourth cell.

The padding or spacing continues through the remaining cells as specified by the command. In the Space 5 example, spacing continues through the fifth cell.

Set Head Address Oriented Command

The Set Head Address Oriented (Hex E0) command can be executed by the controller only if the controller is oriented and only if the subsystem is spacing, not padding. During spacing, the Read/Write Channel board controls (via the CDP data bus in split bus mode) are set for reading, but the serdes circuits are reset.

During the execution of the Set Head Address Oriented command, the controller deactivates the '+ CDP split bus op' line in the device interface to send a Set Head Address Register (Hex 63) command to the selected device. After the device command is completed, the controller activates the '+ CDP split bus op' line and resumes spacing.

The tag sequence for this command is different from that described on OPER-83 for extended commands. The tag sequence for the Set Head Address Oriented command involves the storage control, the controller, and the device. Timing is critical, and the controller sequencer maintains interlocked tag sequences with both the storage control and the device. The complete process occurs in the time of four cells, after which the controller sequencer enters a two-cell long routine, during which the End Op tag is sent and the next command is expected. (See OPER-54 for more information on command transfers during processing)

The figure on page OPER-90 shows the tag sequence for a Set Head Address Oriented command. The events occur in order from the top toward the bottom of the figure. The figure includes all the tag changes that occur between the End Op tag for the preceding command until the End Op tag for the Set Head Address Oriented command.

Controlled by the Storage Control	Controlled by the Controller					Controlled by the Device		
Control Interface				Device Interface				
DDC Tag Out	DDC Byte 0	DDC Byte 1	DDC Tag In	Split Bus Op	CDP Tag Out	CDP Data Bus	CDP Tag In	Comments
(011)		(00)	(10)	active	(011)		(11)	Good End Op - Ready for next command.
	E0							Command Code for Set Head Address Oriented
111								Command Gate Tag Out-DDC
			11					Selected Null Tag In-DDC
								Controller phases out the controls to the R/W Channel board.
				deac-tivate				Deactivates the '+ CDP Split Bus Op' signal
011						63 (out)		Controller Sequencer originates the Set Head Address Register Command to the device.
					111			Command Tag Out-CDP
			01					Controller sends Sync In (ready for Parameter)
	Head Addr						01	Head address from the storage control
001								Sync Out tag validates the parameter
					011			Selected Null Tag Out-CDP
						Head Addr (out)		Sequencer moves head address parameter from the DDC to the CDP bus.
			11		001			Sync Out tag validates the parameter.
011							01	Sequencer prepares the Precompensation circuits for the new address.
					011			Selected Null Tag Out-CDP
							11	Selected Null returned by the device.
						00 (out)		Preparation for changing to split bus mode.
				Acti-vate				Return to split bus mode on the CDP.
		00 End Op Code	10					Sequencer returns the R/W Channel board controls to the space function. End of command indicated by End Op tag.
(011)		(00)	(10)	active	(011)		(11)	Ready for next command.

Figure 23. Tag Sequence for a Set Head Address Oriented Command

End Read/Write Command

The End Read/Write (Hex E1) command causes a change from extended mode to immediate mode. The End Read/Write command can be executed when the controller is either oriented or non-oriented.

If the End Read/Write command is received while the controller is padding (writing pad characters), drive padding is initiated during the command execution.

Sense ECC Bytes (Hex E2)

The sense ECC bytes command is used to collect the 274 bytes of error correction data from the controller during read error correction (see ECC Functions on OPER-65).

During this command, the controller sequencer changes the ECC mode control bits to generate the error correction data from the error syndrome. Then the controller sequencer executes a routine that causes the transfer of the error correction data to the storage control (see Transferring ECC Correction Bytes on OPER-61).

The ECC correction data is transferred to the storage control in transfer mode. The Sync In/Sync Out tag sequence transfers the 274 bytes (two at a time), and the start and stop of the transfer are directly controlled by the controller sequencer.

Time Delay (Hex E3)

The time delay command causes a delay of approximately 80 microseconds.

Extended Diagnostic (Hex E4)

The extended diagnostic command is used to test the operation of error detection circuits. The extended diagnostic command is used only in diagnostic mode and is not used during normal operations.

Immediate Controller Commands

During the execution of immediate controller commands, controller functions are directed by the controller sequencer.

Immediate commands for controllers can be received by only the selected controller.

Except for one command, the tag sequences for immediate controller commands all normally start and end with both tags (in and out) on the control interface (DDC) at Selected Null. The exception occurs with the Start Read/Write command, which usually is used to change the mode from immediate mode to extended mode. When the Start Read/Write command tag sequence ends (in extended mode), the DDC Tag Out is Selected Null and the Tag In is End Op. The same conditions can precede the start of a Start Read/Write command because that command can occur while the subsystem is in extended mode (if not oriented). All other immediate controller commands are valid only if the subsystem is in immediate mode.

For information about how the controller sequencer takes control for immediate controller commands, see OPER-22. (If the subsystem is in extended mode, the controller sequencer is already in control)

The immediate commands for controllers are listed in the figure on page OPER-91. The figure identifies the outbound parameters for these commands and it also identifies the response bytes.

Command Descriptions

The following paragraphs contain short descriptions of the immediate controller commands from the storage control.

Sense Fault Log (Hex 10)

The Sense Error Log command is used to collect check-2 status from the controller and check-1 status from the devices on the selected port. During this command, the controller sends seven response bytes (fault logs A through G) to the storage control.

Command Code (In Hex)	Command Name	Outbound Parameters	Response Bytes
10	Sense Fault Log	-	7 Fault Logs (A through G)
11	Sense Features	-	1 Feature Byte
12	Sense Storage Facility Conf.	-	1 Configuration Byte
14	Sense MD Data	-	1 MD Data Byte
15	Sense EC Level	-	2 Sequencer EC Level Bytes
16	Sense Storage Facility ID	-	1 Physical ID Byte
17	Sense Check-2 Register	-	1 Checkpoint Byte
20	DDC Bus Out Diagnostic	10 Test Patterns	-
22	Start Read/Write	1 Head Address	-
24	Set Md Data Byte 1	1 MD Data Byte	-
25	Set Md Data Byte 2	1 MD Data Byte	-
26	Sense Controller Path	-	1 Controlling Path ID
30	Wrap Bus	Test Data Byte	Test Data Byte
31	Diagnostic Command	Command Modifier	-
33	Reset Allegiance	Device Address	-

Figure 24. Immediate Controller Commands

The Sense Error Log command also resets the controller check-2 circuits and the port check-1 circuits after the status is collected.

Sense Features (Hex 11)

The Sense Features command is used to determine the device dependent information. The bits in the response byte have the following meanings:

Bit	Bit Function
0	DPS Function Installed
1	Storage Facility Configured for Four Path
2	Second CDP card Installed
3	0 (Reserved)
4	0 (Reserved)
5	0 (Reserved)
6	0 (Reserved)
7	1 3380-JK

Sense Storage Facility Configuration (Hex 12)

The Sense Storage Facility Configuration command is used for determining the number of units attached to the controller. This command collects the configuration data by reading the controller configuration switches. Bits 4 and 5 indicate the number of B units attached to the CDP card that handles ports 0 through 3. Bits 6 and 7 indicate the number of B units attached to the CDP card that handles ports 4 through 7.

Sense MD Data (Hex 14)

The Sense MD Data command is used to collect a byte of data (supplied by the MD) from the MD adapter card. This command also resets MD interrupt bit, which is set when the MD sends a byte of data to the MD adapter card.

Sense EC Level (Hex 15)

The Sense EC Level command causes the two byte controller sequencer microcode EC level to be sent to the storage control.

Sense Storage Facility ID (Hex 16)

The Sense Storage Facility ID command collects a byte containing the physical ID of the storage sub-system. The physical ID is set in switches during installation.

Sense Check-2 Register (Hex 17)

The Sense Check-2 Register command is used to collect the controller sequencer checkpoint byte. For more information about this checkpoint byte, see the SENSE section.

DDC Bus Out Diagnostic (Hex 20)

This command verifies that the controller correctly receives the DDC Bus Out (byte 0) from the storage control. The controller compares a series of 10 1-byte patterns with the 10 consecutive bytes received from the storage control. The expected patterns are:

Pattern 01 = Hex 00
Pattern 02 = Hex 01
Pattern 03 = Hex 02
Pattern 04 = Hex 04
Pattern 05 = Hex 08
Pattern 06 = Hex 10
Pattern 07 = Hex 20
Pattern 08 = Hex 40
Pattern 09 = Hex 80
Pattern 10 = Hex FF

If the expected pattern and the pattern received are not the same, the controller responds with an End Op tag.

This command is used only during diagnostics and is not part of normal operations.

Start Read/Write (Hex 22)

The Start Read/Write command changes the mode of operation from immediate mode to extended mode. During the start read/write command tag sequence, the controller sequencer sends a set head-address register command to the selected device.

The Start Read/Write command is the only immediate controller command that can be received by a controller while in extended mode.

Set MD Data Byte 1 (Hex 24) and Set MD Data Byte 2 (Hex 25)

The Set MD Data Byte 1 and 2 commands are used to store data for the MD in the MD adapter card. The execution of these commands is exactly the same. The first command (of two) stores the high-order byte in a two-byte register. The second command stores the low-order byte in the two-byte register and sets the adapter-loaded bit, which can be tested by the MD.

Sense Controller Path (Hex 26)

In response to this command, one byte is returned to the storage control indicating the controller path. Bits 0 through 5 are all 'zeros' (unused), bits 6 and 7 indicates controller A1 through A4.

Wrap Bus (Hex 30)

The Wrap Bus command is used to test the byte 1 bus in the control interface (DDC). This command wraps the byte out on DDC byte 0 back in on DDC byte 1.

Diagnostic Command (Hex 31)

The Diagnostic command is used to exercise and to verify the operation of error detection circuits. The test is specified by a modifier (outbound parameter).

This command is used only during diagnostics and is not part of normal operations.

The following modifiers are valid for this command:

Hex C0 - Controller Reset
Hex C1 - Diagnostic Extended Command Mode
Hex C2 - Force PLO No Device Check
Hex C3 - Force Multi-Select Check
Hex D0 - Force Sequencer Check-1 (Word 0)
Hex D1 - Force Sequencer Check-1 (Word 1)
Hex D2 - Force Sequencer Check-1 (Word 2)
Hex D3 - Controller Sequencer Check
Hex D4 - BIDI Bus 1 Parity Check 1
Hex D5 - Sequencer Forced Check 1
Hex D6 - Register Data Bus Parity Check

Hex D7 - Register Data Bus Parity Check
Hex E0 - Register 13 Status Test
Hex E1 - Counter Test
Hex E2 - Port Select - Extended Mode
Hex F0 - Set/Reset Split Bus Mode
Hex F1 - Lock PLO To Servo - Selected

Reset Allegiance (Hex 33)

This command is issued when only the controller is selected. It frees the addressed device, indicated by the one byte parameter, even if that device is selected through another controller. If the device was selected, a check is generated in the controller through which the device was selected. Only one device is freed with each issuance of the command.

The meanings of the bits in the outbound parameter are as follows:

Bit	Bit Function
0	Device Address Bit 16*
1	0 (Unused)
2	0 (Unused)
3	0 (Unused)
4	Device Address Bit 8
5	Device Address Bit 4
6	Device Address Bit 2
7	Device Address Bit 1

* 0 = Devices 00 through 0F
  1 = Devices 10 through 1F

Device Commands

Device commands are all immediate commands.

Most device commands originate in the storage control. During device commands from the storage control, communications between the storage control and the device is through the feedthrough paths in the controller.

Although most device commands are from the storage control, the controller originates some. The controller issues Start Spindle Power On command and the Reset Device Checks command during the initial power-on sequence. The controller also issues the Set Head Address Register command during the execution of the Start Read/Write command (an immediate controller command) and during the execution of the Set Head Address Oriented command (an extended command).

Device commands are received by only the selected device. All device command sequences start with the Tag In lines at Selected Null tag (11). Correctly completed device command tag sequences also end with the Tag In at Selected Null.

See OPER-83 for general information about 3380-JK command and their immediate commands.

See OPER-22 for information on the feedthrough paths in the controller.

See OPER-13 and OPER-15 for descriptions of the control interface and the device interface.

Device Command Types

Device commands are divided into two types - those that involve the device sequencer, and those that do not involve the device sequencer.

During device commands that do not involve the device sequencer, device check 2 errors are ignored by the circuits that generate the Tag In responses. Commands of this type are for collecting status from the device. No errors are recognized and the device is not automatically deselected. (No End-Op tag is sent, and the sequence ends with the Tag In from the device at Selected Null.)

In contrast, all device commands that involve the device sequencer (with three exceptions, mentioned in the beginning paragraphs) are accepted by the device if (and only if) there are no device check 2 errors both before and during the command. Any device check 2 error results in an End-Op tag.

Some device commands that involve the device sequencer initiate functions that are completed after the end of the command sequence. The functions started by these commands can be completed while the device is no longer selected. The completion of these functions is generally indicated to the storage control through interrupts during polls.

Command Code (In Hex)	Command Name	Outbound Parameters	Response Bytes
40	Start Spindle Power On	-	-
43	Reset Device Checks	-	-
44	Seek and Verify No Guard Band (Model J)	2 - DCP Seek Code and Cylinder Address	1 - Device Status 1
46	Seek, Sector Search and Verify No Guard Band (MOD J)	3 - Same as '44' with Sector Address Added	1 - Device Status 1
48	Seek and Verify No Guard Band (Model K)	2 - DCP Seek Code and Cylinder Address	1 - Device Status 1
49	Seek, Sector Search and Verify No Guard Band (MOD K)	3 - Same as '48' with Sector Address Added	1 - Device Status 1
4A	Reset Interrupts	-	-
4C	Start Rezero	-	-
4D	Load Path Interrupt Table	1 - PIT Register Byte	-
4F	Start Spindle Power Off	1 - 'B0'	-
50	Sense Device Status 1	-	1 - Device Status 1
51	Sense Power Status	-	1 - Power Status
52	Gate Servo Status and Bump Pointer	-	1 - Servo Status
53	Sense Read/Write Status 1	-	1 - R/W Status 1
54	Sense Read/Write Status 2	-	1 - R/W Status 2
55	Sense Device Checks	-	1 - Device Check 2
56	Sense Read/Write Status 3	-	1 - R/W Status 3
57	Sense Device Checkpoint Log	-	1 - Checkpoint Log
58	Sense Device Status 2	-	1 - Device Status 2
59	Seek Cylinder minus 3	-	-
5C	Read Home Address Register	-	1 - Head Address
5D	Gate Servo Status and Reset Pointer	-	1 - Servo Status 0
5E	Controller CDP Parity Test	-	-
5F	Force Device Check 1	-	-
62	Sector Search	1 - Sector Address	1 - Device Status 1
63	Set Head Address Register	1 - Head Address	-
69	Seek Cylinder minus 2	-	-
6A	Seek Cylinder minus 4	-	-
6C	Start Offset	2 - DCP Offset Code and amount of offset	1 - Device Status 1
6E	Start Offset and Sector Search	3 - Same as '6C' with Sector Address Added	1 - Device Status 1
71	Select Servo Status 1 or 2	2 - Reg. Select and Servo RAM address	-
72	Set Register Pointer	1 - Register Address	-
74	Sense Read/Write Status 4	-	1 - R/W Status 4
75	Sense Path Interrupt Table	-	1 - PIT Register Byte
76	Arm Device Interrupt	2 - '89' '00'	1 - Device Status 1
78	Seek To Anywhere	2 - DCP Seek Code and Cylinder Address	1 - Device Status 1
79	Sense GBOD or GBID	-	-
7A	Seek To Anywhere and Sector Search	3 - Same as '78' with Sector Address Added	1 - Device Status 1

Figure 25. Device Commands

The above figure contains a list of the device commands. The figure identifies the commands that require outbound parameters and those commands that send a response inbound. It also identifies what those parameters and responses will contain.

Command Descriptions

The following contains a short description for each of the device commands.

Start Spindle Power On (Hex 40)

The Start Spindle Power-on command is used to power on the drive motor and to position the read/write heads in a known position (cylinder zero).

The command starts a sequence that contains the following servo processes.

- Park
- Compress
- Sweep/Warm Up (Clean)
- Rezero

- Track follow

The device sequencer accomplishes all these servo processes by issuing servo commands to the Digital Control Processor (DCP). The Park process insures that the read/write heads are positioned in the Outside Diameter Guard Band (GBOD) to prevent them from landing on data if a power failure should occur.

The compress process pushes the access mechanism against the outer crash stop to change the location of the heads for take-off from the location used for landing.

The Sweep/Warm Up (also known as the Clean process) process moves the heads twice across the disk surfaces a track at a time. The purpose is to dislodge any loose particles from the surface during the drive-motor power-on sequence. (The inner edge of the heads are designed to deflect particles on the surface of the disks) At the end of the two sweeps the sequencer enters a time delay for further warm up. This allows for the required temperature stabilization.

The rezero process moves the access mechanism from any position to the inner guard band, then to the -3 cylinder in the outer guard band, and finally to cylinder 0. During a rezero operation, the DCP does some required circuit calibration. Actuator movement is about two inches per second.

The track follow process keeps the access mechanism positioned with the heads over the center of the tracks in the current cylinder. Track follow is used during normal Read and write operations. Track follow normally continues until another access mechanism positioning process is needed.

During the spindle power on sequence, the device sequencer tests the status of specific lines to determine that the air system is good. It also senses the Servo Status register to verify that the servo processes are progressing correctly.

When the read/write heads are in cylinder zero (at the end of the sequence), the device sequencer activates the online and attention bits (in the device status 1 byte). The attention bit causes an interrupt.

Reset Device Checks (Hex 43)

The Reset Device Checks command resets the check-2 error latches in the selected device.

During this command, the device sequencer loads the byte (Hex 43) on the CDP data bus in the target register (in the device sequencer/servo/RPS card) and causes the rest of the device logic to reset all check 2 circuits. Then the device sequencer loads hex 43 in the head address register (in the port read/write control card).

Seek and Verify No Guard Band - Model J (Hex 44)

Seek and Verify No Guard Band - Model K (Hex 48)

These commands prepare the device for a seek operation. The only difference between them is that the hex '44' command is for a model J and the hex '48' is for a model K.

During the command, the device sequencer loads the first outbound parameter from the CDP data bus into the DCP command high register; the second outbound parameter into the DCP command low register. The device sequencer then gates the device status 1 response byte to the storage control and branches to the DCP execution routine.

Together, the first and second parameters indicate the DCP seek command code and the cylinder number that the actuator is to be moved to. The meanings of the bits in the outbound parameters are as follows:

Parameter Byte 1		**Parameter Byte 2**	
Bit	Bit Function	Bit	Bit Function
0	0*	0	Cylinder Add. 128
1	1*	1	Cylinder Add. 64
2	1*	2	Cylinder Add. 32
3	1*	3	Cylinder Add. 16
4	0 (Unused)	4	Cylinder Add. 8
5	0 (Unused)	5	Cylinder Add. 4
6	Cylinder Add. 512	6	Cylinder Add. 2
7	Cylinder Add. 256	7	Cylinder Add. 1

* This value is the DCP command code for a Seek.

At the destination cylinder, a test is made to ensure that the read/write heads are not in a guard band area. None of the customer cylinders are in a guard band area.

Receipt of these commands with offset active will result in the command being performed and the offset being reset.

The response byte returned to the storage control is the device status 1 byte.

The completion of a seek operation (either correct or with an error) causes an interrupt.

Seek, Sector Search and Verify No Guard Band - Model J (Hex 46)

Seek, Sector Search and Verify No Guard Band - Model K (Hex 49)

These command are the same as the hex '44' and the hex '48' commands with a sector search (Hex '62' command) at the end of the seek process. Again, as with the '44' and '48' commands, the hex '46' command is for a model J and the hex '49' is for a Model K.

There are three outbound parameters for these commands. The first two bytes indicate the DCP seek command code and the cylinder number that the actuator is to be moved to (see the figure that is with the hex '44' and the hex '48' commands). The third parameter byte indicates the desired sector address (see the figure that is with the hex '62' command).

At the destination cylinder, a test is made to ensure that the read/write heads are not in a guard band area. None of the customer cylinders are in a guard band area. Once the sequencer has determined that the read/write heads are not sitting in a guard band, it branches to the sector search routine.

Receipt of these commands with offset active will result in the command being performed and the offset being reset.

The response byte returned to the storage control is the device status 1 byte.

The completion of the sector search (either correct or with an error) causes an interrupt.

Reset Interrupts (Hex 4A)

The Reset Interrupts command is used to reset any active interrupt latches in the selected device.

Start Rezero (Hex 4C)

This command causes the Digital Control Processor (DCP) to calibrate its Cylinder Address Register (CAR) by moving the actuator until the transition from the data band to the Guard Band is detected, and then moving the actuator to cylinder 'zero'. This command also resets the servo circuitry and reloads the servo microcode (DCP IML). It is the only means (other than power on reset) of resetting a Servo Check 2 condition.

The completion of the rezero operation (either correct or with an error) causes an interrupt.

Load Path Interrupt Table (PIT) (Hex 4D)

This command is used to load the one parameter byte into the PIT register. Bits 0 through 3 are the only bits used by the Path Interrupt Table. Bit 0 for the A1 controller, bit 1 for the A2, bit 2 for the A3 and bit 3 for the A4 controller (for example: bit 3 bit active allows interrupts from this device to the A4 controller).

Start Spindle Power Off (Hex 4F)

This command is used to initiate the drive motor power off sequence. It must be issued within one millisecond to both devices sharing the same spindle. Receipt of this command causes the device to present busy, park the actuator and enter the power off sequence. Hex 'B0' is the only parameter that is sent outbound to the device and it is the complement of the command code. This is used to validate the the command.

Sense Device Status 1 (Hex 50)

The Sense Device Status 1 command is used to collect status information from the selected device. For more information about this status byte, see page SENSE-74 in the Sense Section.

Sense Power Status (Hex 51)

The Sense Power Status command is used to collect status information from the selected device. For more information about this status byte, see page SENSE-63 in the Sense Section.

Gate Servo Status and Bump Pointer (Hex 52)

This command causes the sequencer circuits to send, to the storage control, the contents of the Internal Sequencer register that is being pointed to by the register address counter. (Six of these Sequencer Registers contain DCP Servo Status information). Once the status byte has been read, the register address counter is bumped by one to point to the next servo status register.

Sense Read/Write Status 1 (Hex 53)

The Sense Read/Write Status 1 command is used to collect status from the selected device. For more information about this status byte, see page SENSE-88 in the Sense Section.

Sense Read/Write Status 2 (Hex 54)

The Sense Read/Write Status 2 command is used to collect status from the selected device. For more information about this status byte, see page SENSE-89 in the Sense Section.

Sense Device Check (Hex 55)

The Sense Device Check command is used to collect status from the selected device. For more information about this status byte, see page SENSE-63 in the Sense Section.

Sense Read/Write Status 3 (Hex 56)

The Sense Read/Write Status 3 command is used to collect status from the selected device. For more information about this status byte, see page SENSE-90 in the Sense Section.

Sense Checkpoint Log (Hex 57)

The Sense Checkpoint Log command is used to collect the contents of the checkpoint log register from the device sequencer/servo/RPS card. The contents of the checkpoint register is periodically updated by the device sequencer to indicate what has occurred. This byte could either describe a normal operation or a device sequencer microcode detected failure.

When an error condition is first recognized by the device sequencer (instead of hardware check circuits). the device sequencer loads a specific value into the checkpoint register to identify the cause of the error.

When the contents of the Checkpoint log represents a failure, the checkpoint check bit (bit 3) in the Device Check 2 Status byte is activated.

For the definitions of the values that are placed in the checkpoint log see page SENSE-66 in the Sense Section.

Sense Device Status 2 (Hex 58)

The Sense Device Status 2 command is used to collect status information from the selected device. For more information about this status byte, see page SENSE-75 in the Sense Section.

Seek Cylinder -3 (Hex 59)

This command is used to position the read/write heads three cylinders behind cylinder 0 (toward the outer edge of the disks) for accessing the back-up tracks for home address records. (That position is cylinder -3 for 3380-J and 2668 for 3380-K, it is DCP cylinder 61 on both models)

Read Head Address Register (HAR) (Hex 5C)

The Read Head Address Register command is used to verify that HAR has been correctly loaded (this is a diagnostic command and is not used for normal operations).

Gate Servo Status and Reset Pointer (Hex 5D)

This command resets the contents of the register address counter to a hex '01'. It then sends, to the storage control, the contents of the servo status register that is located at address '00' (Servo Status 0 register - low). For more information about this status byte, see page SENSE-65 in the Sense Section.

Controller CDP Parity Test (Hex 5E)

This command sends even parity on the CDP bidirectional data bus from the device. The error is detected by the controller (this is a diagnostic command and is not used for normal operations).

Force Device Check 1 (Hex 5F)

This command tests the device circuits for detecting and reporting CDP parity checks. A CDP parity check detected by the device is a device check-1 (this is a diagnostic command and is not used for normal operations).

Start Sector Search (Hex 62)

This command loads the Sector Target register of the selected device with a sector address and initiates a sector search. Any of the 222 sectors (sector address 0 through 221) of a cylinder can be found. The sector compare circuits provide a record ready interrupt when the target sector has been reached.

The meanings of the bits in the outbound parameter are as follows:

Bit	Bit Function
0	Sector Address Bit 128
1	Sector Address Bit 64
2	Sector Address Bit 32
3	Sector Address Bit 16
4	Sector Address Bit 8
5	Sector Address Bit 4
6	Sector Address Bit 2
7	Sector Address Bit 1

The response byte returned to the storage control is the device status 1 byte.

The completion of a sector search (either correct or with an error) causes an interrupt.

Set Head Address Register (Hex 63)

The Set Head Address Register command is used to select the read/write head for read and write operations.

During this command, the arm and head addresses are contained in a single outbound parameter, which is loaded into the head address register in the Port R/W Control card (from the CDP data bus).

The meanings of the bit positions in the outbound parameter and in the head address register are as follows:

Bit	Bit Function
0	Unused
1	Unused
2	Unused
3	Unused
4	Head Address Bit 8
5	Head Address Bit 4
6	Head Address Bit 2
7	Head Address Bit 1

Seek Cylinder -2 (Hex 69)

This command is used to position the read/write heads two cylinders behind cylinder 0 (toward the outer edge of the disks) for accessing the back-up tracks for home address records (that position is cylinder -2 for 3380-J and 2667 for 3380-K, DCP cylinder 62 for both models).

Seek Cylinder -4 (Hex 6A)

This command is used to position the read/write heads four cylinders behind cylinder 0 (toward the outer edge of the disks) for accessing the back-up tracks for home address records. (That position is cylinder -4 for 3380-J and 2669 for 3380-K, DCP cylinder 60 for both models)

Start Offset (Hex 6C)

The Start Offset command prepares the device for an offset operation, which moves the heads a specified distance from track center in a specified direction. Offsets are used during read retries in an attempt to improve reading.

During the command, the device sequencer loads the first outbound parameter from the CDP data bus into the DCP Command High register and the second outbound parameter into the DCP Command Low register. The device sequencer gates the response byte (device status 1) to the storage control before it has the DCP execute the offset command. The meanings of the bits in the outbound parameters are as follows:

Parameter Byte 1		Parameter Byte 2	
Bit	Bit Function	Bit	Bit Function
0	1*	0	Offset Bit 8
1	0*	1	Offset Bit 7
2	0*	2	Offset Bit 6
3	1*	3	Offset Bit 5
4	Offset Bit 12**	4	Offset Bit 4
5	Offset Bit 11	5	Offset Bit 3
6	Offset Bit 10	6	Offset Bit 2
7	Offset Bit 9	7	Offset Bit 1

* This value is the DCP command code for an Offset.
** = 0 = Plus Offset
1 = Minus Offset

When the offset operation is completed (either correctly or with an error), an interrupt signal is generated. When there is an offset condition, the Dev Stat 2, Bit 2 is set and writing is inhibited. When the offset condition is cleared, the Dev Stat 2, Bit 2 is cleared and writing is allowed. Any seek or rezero operation resets the offset condition.

Start Offset and Sector Search (Hex 6E)

The Start Offset and Sector Search command combines the offset operation and sector search operation. The parameters needed for both operations (first two are for the offset and the third is for the sector search) are transferred and loaded into the respective registers, and the response byte (device status 1) is sent to the storage control before either operation is actually started. Then the offset operation is performed. If that operation is completed without an error, the interrupt that normally occurs at the end of an offset operation is bypassed, and the device sequencer proceeds with the sector search operation. An interrupt is generated when the sector identified by the contents of the target register is found.

Select Servo Status 1 or 2 (Hex 71)

This command is used to select servo status information from the servo data RAM and put it in the Servo Status 1 register or the Servo Status 2 register. The two outbound parameters contain the DCP command code Servo Status, the register select bits and Servo Address RAM bits. (This is a diagnostic command and will not be used during normal operations.)

Set Register Pointer (Hex 72)

This command is used to set a register pointer in the register address counter register prior to the execution of the Gate Servo Status and Bump Pointer (Hex '52') command.This is done in order to retrieve the contents of a specific register when that command is issued.

Sense Read/Write Status 4 (Hex 74)

The Sense Read/Write Status 4 command is used to collect status from the selected device. For more information about this status byte, see page SENSE-90 in the Sense Section.

Sense Path Interrupt Table (PIT) (Hex 75)

This command is used to sense the contents of the Path Interrupt Table (PIT) register. One response byte is returned to the storage control containing this information.

Arm Device Interrupt (Hex 76)

This command is used to generate a Seek Complete Interrupt from the selected device without causing the actuator to move.

Seek To Anywhere (Hex 78)

This command is identical to the Seek and Verify No Guard Band (Hex '48') command except that there is no guard band restrictions. (This allows seeks into the guard band area.) See the above mentioned command for more information.

Sense GBOD or GBID (Hex 79)

This command is used to test for the presence of the Outside Diameter Guard Band (GBOD) or the Inside Diameter Guard Band (GBID). The device sequencer samples the GBOD and GBID signals, from the DCP, and reports the findings to the storage control by the value it places into the checkpoint log.

Seek To Anywhere and Sector Search (Hex 7A)

This command is identical to the Seek, Sector Search and Verify No Guard Band (Hex '49') command except that there is no guard band restriction. (This allows seeks into the guard band area). See the above-mentioned command for more information.

DPS Commands

All DPS (Dynamic Path Selection) commands are immediate commands.

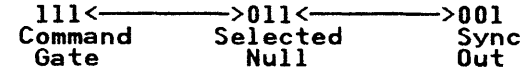
During DPS commands, like all other immediate commands, the control interface (DDC)remains in control mode.

The function caused by a DPS command is always completed during the tag sequence for the command.

In the start of each DPS command tag sequence, circuits in the IOCC card activate the '- DPS command' line, which enables the DPS card to respond. The '- DPS command' line remains active throughout the tag sequence and is deactivated by any of the following events:

- Command Gate on the DDC Tag Out lines, from the storage control, without a DPS command code on the DDC byte 0 bus.
- Null Disconnect on the DDC Tag Out lines from the storage control (controller deselected).
- The 'seq controls DDC/CDP' latch is set (the controller sequencer is in control).
- The '+ DPS op complete' line is active. (Activated by the DPS card in response to a Terminate DPS Control command or during device selection).

During DPS command tag sequences, the Tag Out from the storage control can change as shown in the following figure.



A Tag Out change from Selected Null to Command Gate ends a current DPS command tag sequence and indicates the start of another immediate command.

During DPS command tag sequences, the Tag In signals from the DPS card alternate between the Sync In or Valid (01) state and the Selected Null (11) state.

The DPS card cannot send an End Op Tag In. If a check-2 error is detected, the controller sequencer takes control to prepare the end op code and to send the End Op Tag In.

Command Descriptions

The following paragraphs contain short descriptions of the DPS commands from the storage control. The DPS commands are also listed in the figure on page OPER-101. The figure identifies those commands that involve outbound parameters and those for which the DPS card supplies defined response bytes.

Copy Alternate Array (Hex 08)

The Copy Alternate Array command is used to initialize an array in one DPS card from the updated information in the array in the other DPS card. The card that receives the data is the one that receives the command. At the end of the command, the information in both arrays is exactly the same.

Command Code (In Hex)	Command Name	Outbound Parameters	Response Bytes
08	Copy Alternate DPS Array	–	–
09	Terminate DPS Control	–	–
0A	Inhibit DPS Device Lock Reset	–	–
0B	Alert Process Macro	(Variable)	(Variable)
18	Sense DPS Status	–	DPS Status Byte
19	Read Alternate DPS Lock Status	–	Lock Status Byte
1A	Disconnected Chain Cleanup	–	Availability Byte
1B	End CCW Cleanup Macro	–	Availability Byte
1C	Read Device Parameters Macro	–	Data
28	Write DPS Array	Address (2) and Data	Data Returned
2A	Reset DPS Locks	Reset Pattern	–
2C	Write Device Parameters Macro	Data	Data Returned
38	Read DPS Array	Address (2)	Data
3A	Set DPS Locks	Pattern	Status
3C	Set Under Mask	Address (2) and Masks	Updated Data
3D	Reset Under Mask	Address (2) and Masks	Updated Data

Figure 26. DPS Commands

Terminate DPS Control (Hex 09)

This command is given at the conclusion of a DPS command sequence, when the storage control wishes to transfer control of the DDC from the DPS hardware to the sequencer in the controller. The Terminate DPS Control command activates the '+ DPS op complete' line, which then deactivates the '- DPS command' line. When that line is inactive, the DPS circuits deactivate the '+ DPS op complete' line.

Inhibit Device Lock Reset (Hex 0A)

The Inhibit Path Lock Reset command is used to keep the current path busy status for the path after deselection. An example of when this command could be used is when a read retry is pending after a read error. The path busy status prevents the use of the port by the controller in the string, keeping the collection of interrupt information from that port possible.

If deselection is not preceded by this command, the path is available to the other controller after deselection. The effect of this command is cancelled by the next device selection that uses the port.

Alert Processing Macro (Hex 0B)

The Alert Processing Macro command is used to update device information in one storage control after that storage control receives an Array Updated interrupt. An Array Updated interrupt indicates that device information in the DPS arrays has been updated by the other storage control to which the string is attached.

During the Alert Processing Macro command, command modifiers and responses are exchanged between the storage control and the DPS card to identify the extent of the updated information in the arrays. Then the updated information is read from the arrays to update the control store in the storage control.

Sense DPS Status (Hex 18)

The Sense DPS Status command is used to collect one byte of status information from the primary DPS card. (The primary card is the one that received the command. The alternate card is the one associated with the other controller.)

The meanings of the bits in the response byte from the DPS card are:

Bit	Bit Function
0	Primary Long Busy Indicator
1	0 = A1 Controller 1 = A2 Controller
2	DPS Installed
3	Primary Array Initialized
4	Alternate Array Initialized
5	0 (Unused)
6	Primary Array Data Lock 1 Set
7	Primary Array Data Lock 1 Set

The array lock indicators are program indicators that are set and reset by commands from the storage control. These indicators have no effect on other circuits in the DPS card.

Read Alternate DPS Lock Status (Hex 19)

The Read Alternate DPS Lock Status command collects status for the alternate DPS card (the one with the other controller) from the primary DPS card. The status is collected by the primary card from the alternate card through the controller-to-controller connection.

The meanings of the bits in the response byte sent to the storage control are:

Bit	Bit Function
0	Array Updated
1	Alternate Device Busy
2	Array Lock 1 Indicator
3	Array Lock 2 Indicator
4	Path Lock 0
5	Path Lock 1
6	Path Lock 2
7	Path Lock 3

The array lock indicators are programming indicators that do not affect other DPS circuits. The array lock indicators are set and reset by commands.

The path lock bits indicate that the controller-to-device port is currently in use by that controller or is reserved for use by that controller.

Disconnected Chain Cleanup (Hex 1A)

The Disconnected Chain Cleanup command is used to prepare for a disconnected chain of channel command words. For example, after a seek operation is started in a device, the storage control can deselect the device and perform work with another device. When the seek operation is completed, the device activates an interrupt signal (which is collected during polling) to indicate the completed seek operation. To prevent the other storage control from starting an operation with that device before the storage control that started the chain has selected the device again, the storage control that issued the seek issues a disconnected chain cleanup command before deselecting the device. The Disconnected Chain Cleanup command changes certain device information in the array so that the device is not available to the other storage control.

After the information in the array is changed, the DPS card sends an availability byte to the storage control (with Valid Tag In). The active bit in the byte identifies the channel to which the device is available for completing the chain.

Information changed in an array is changed in both the primary and alternate arrays.

End Of CCW Cleanup Macro (Hex 1B)

The End Of CCW Cleanup command is used to prepare the DPS circuits and the arrays before deselecting a device after a chain of channel command words is completed.

After the information in the arrays is changed, the DPS card sends an availability byte to the storage control (with Valid Tag In). The active bits in the byte identify the channels to which the device is now available.

Read Device Parameters Macro (Hex 1C)

The Read Device Parameters command is used to read the information in the arrays for the currently selected device. The starting address of the information in the arrays for that device is generated by circuits in the DPS card. For each Sync Out tag from the storage control, the byte specified by the address is read from the array and sent to the storage control on DDC byte 1 (with Valid Tag In). Then circuits in the DPS card add 1 to the address to prepare for reading the next byte.

The storage control ends the sequence by starting another command (by changing the Tag Out to Command Gate).

Write DPS Array (Hex 28)

The Write DPS Array command is used to update information in both the primary and alternate arrays. The address in the arrays for the first byte of data is supplied by the storage control in the first two outbound parameters. Bits 4 through 7 of the first parameter become bits 0 through 3 of the 12-bit address. Bits 0 through 7 of the second parameter become bits 4 through 11 in the address. The third and following parameters are data, which is stored in the arrays.

When the third parameter is validated by a Sync Out tag, the byte is written in both the primary and alternate arrays. Then the DPS circuits add 1 to the address and send the byte (just written) to the storage control on DDC byte 1.

The sequence ends when the storage control starts the next command.

Reset DPS Locks (Hex 2A)

The Reset DPS Locks command is used to control the status of latches in the DPS cards. The latches are set and reset according to the active bits in the outbound parameter from the storage control.

The bits in the parameter have the following meanings: (Inactive bit positions cause no action.)

Bit	Bit Function
0	Set Array Update Notification to the Alternate DPS card
1	Reset Array Update Notification from the Alternate DPS card
2	Reset Array Lock 1 Indicator
3	Reset Array Lock 2 Indicator
4	0 (Reserved)
5	Reset Primary Long Busy Indicator
6	Reset Primary Array Initialized
7	0 (Unused)

If the array updated latch is set, the DPS card activates an interrupt signal that is collected during polls.

The array lock indicators are program indicators that are used by the storage control program. These indicators do not affect other DPS circuits.

If the array initialized latch is not set, it indicates that the array does not contain good information and device selection is not permitted.

Write Device Parameters Macro (Hex 2C)

The Write Device Parameters command is used to store new information in both the primary and alternate arrays for the currently selected device. The starting address is generated in the DPS card. Each Sync Out tag from the storage control validates a byte of device information. After the current byte is stored, the DPS card adds 1 to the address to prepare for the next byte. The DPS card also sends the byte (just written) back to the storage control on DDC byte 1.

The sequence ends when the storage control starts another command.

Read DPS Array (Hex 38)

The Read DPS Array command permits the storage control that issues the command to collect any or all the information that is stored in the arrays.

The storage control sends two outbound parameters, which provide the starting address for the operation. Bits 4 through 7 in the first parameter become address bits 0 through 3 of the 12-bit address. Bits 0 through 7 in the second parameter represent address bits 4 through 11.

For each Sync Out tag (from the storage control) that follows, the DPS cards (both primary and alternate) read the addressed byte in the arrays.

The data is compared for accuracy and sent to the storage control by the primary DPS card. The DPS card then adds 1 to the address to prepare for the next Sync Out tag.

The sequence ends when the storage control starts another command.

Set DPS Locks (Hex 3A)

The Set DPS Locks command is used to control the status of latches in the DPS cards. The latches are set according to the bits that are active in the outbound parameter from the storage control. Inactive bits in the parameter cause no action.

The active bits in the parameter are the same as the Sense DPS Status (Hex 18). (See the parameter byte on page OPER-102 for the bit definitions.)

If the array initialized latch is set, it indicates that the array contains good information and device selection operations are permitted.

The array lock indicators are program indicators that are used by the storage control program. These indicators have no affect on the operation of other DPS circuits.

After the specified latches are set, the DPS card sends a response byte to the storage control. In that response, only bit 5 is defined. Bit 5 is active if at least one array lock was specified and was set.

Set Under Mask (Hex 3C)

The Set Under Mask command is used to set specified bits in the array without affecting the status of other bits in the same byte.

The storage control supplies a starting address in the first two outbound parameters. Bits 4 through 7 in the first parameter become bits 0 through 3 in the address. Bits 0 through 7 in the second parameter become address bits 4 through 11.

The third and following parameters from the storage control are masks, which are validated by Sync Out tags the same as the address parameters. As each mask is received by the DPS card, the addressed byte is read from the arrays (both primary and alternate). The byte read is logically ORed, bit-for-bit, with the mask byte to produce a result byte. The result byte then replaces the byte read from the arrays (stored at the same address) and is sent to the storage control on DDC byte 1. The DPS card also adds 1 to the address to prepare for the next mask byte.

(In the Set Under Mask command, any 1-bit in a mask ensures a 1-bit in the corresponding position in the result byte. A 0-bit in a mask causes no change.)

The tag sequence for this command ends when the storage control starts another command.

Reset Under Mask (Hex 3D)

The Reset Under Mask command is used to reset specified bits in the arrays without affecting the status of other bits in the same byte.

The storage control supplies a starting address in the first two outbound parameters. Bits 4 through 7 in the first parameter become bits 0 through 3 in the address. Bits 0 through 7 in the second parameter become address bits 4 through 11.

The third and following parameters from the storage control are masks, which are validated by Sync Out tags the same as the address parameters. As each mask is received by the DPS card, the addressed byte is read from the arrays (both primary and alternate). The byte read is logically ANDed, bit-for-bit, with the mask byte to produce a result byte. The result byte then replaces the byte read from the arrays (stored at the same address) and is sent to the storage control on DDC byte 1. The DPS card also adds 1 to the address to prepare for the next mask byte.

(In the Reset Under Mask command, any 0-bit in a mask ensures a 0-bit in the corresponding position in the result byte. A 1-bit in a mask causes no change.)

The tag sequence for this command ends when the storage control starts another command.

The Controller

A controller consists of sequencer microcode, power supplies and controller logic. The logic is broken down into three types; Control logic, Data Handling logic, and optionally, Dynamic Path Selection (DPS) arrays and controls. Some of the controller logic cards perform both the control and data handling functions. The control logic does the following:

1. Communicates with the storage control
2. Communicates with the devices
3. Presents interrupts to the storage control
4. Controls the power to the device logic
5. Controls the power to the drive motors
6. detects and isolate faults

The Data Handling logic does the following:

1. Synchronizes the controller's timing with the data
2. Serializes and de-serializes the data
3. Encodes and Decodes the data
4. Detects data errors and produces correction information
5. Transfers the data to and from the HDA

The DPS feature will only be installed on 3380-JK's that are attached to a 3880 storage control unit.

The DPS circuits are responsible for maintaining the information necessary to make the 'time-sharing' of the devices within a string by two storage controls orderly. Whenever a storage control desires to select a device, the DPS circuits step in and verify that the device is available and not in use by the alternate controller. This is by the primary DPS circuits communicating with the alternate DPS circuits in the other controller. This communication is done across the Controller-to-Controller Connection (CCC) bus. For more information about the DPS function and the CCC bus, see pages OPER-11 and OPER-20.

With the exception of the controller power supplies and DPS circuits, (which has been already discussed) the controller logic will be described in the following paragraphs. For information on the power supplies see the PWR (power) section of the Maintenance Information Manual (MIM).

Controller Logic

The controller logic (circuitry) is located on logic cards installed in the 'A' board. (An 'A' board holds two complete and independent controllers.)

DDC/DTB card

The primary function of the DDC (Director-to-Device Controller) circuits on the DDC/DTB card are to receive and drive the DDC interface for the controller. These circuits, when receiving, convert the differential from the storage control to a digital signal for the controller. When sending, it converts the controller digital signals to the differential used on the DDC interface.

The primary function of the DTB (Data Transfer Buffer) circuits during a write operation are to receive from the DDC circuits, buffer (up to 8 bytes, 4 bytes for DDC Byte 0 and 4 bytes for DDC Byte 1) and send to the Clock/Serdes/ECC card the data from the storage control. During a read operation these circuits receive the data from the Clock/Serdes/ECC card and send to the storage control through the DDC driver circuits.

The following error checking is provided by both circuit functions:

- Checks DDC Bus Out bytes 0 and 1 for correct parity during a write operation.
- Checks for an overrun or underrun condition during a write. An overrun is where the storage control is suppling data faster then the serdes circuits can handle it. The underrun is the opposite problem, serdes requesting data when none is available from the storage control.
- Checks both the Read Data Byte 0 register and the Byte 1 register for correct parity during a read operation. These registers are used as a two byte buffer between the Clock/Serdes/ECC card and the DDC drivers.
- Checks DDC Bus In byte 1 (from the IOCC card) for correct parity when the DDC interface is in control mode.

This card also performs a very unique function for the controller when a controller check 1 failure is detected. The DDC/DTB circuits, not only detect a few check 1 failures themselves but they provide the following for the controller:

1. Log all check 1's that are detected by the rest of the controller hardware and the microcode.
2. Take over control of the controller during the check 1 sequence. (The controller sequencer is trapped to address x'000' and the system clocks are stopped when a check 1 is detected.)
3. Report to the storage control that a controller check 1 failure has been detected. (Activates Connection Check Alert lines to the storage control.)
4. Causes the Request Connection Check (RCC) bits to be presented to the storage control during the RCC sequence.
5. Resets the controller during the Hardware Immediate sequence.

On the DDC/DTB card are the controller string address switches, that are set by the CE during installation. Address circuitry on the card, along with these switches, provide address validation for the controller during all selection and polls sequences.

IOCC card

The IOCC (Input/Output Control Card) contains all but three (those are located on the sequencer card) of the controller sequencer's input and output registers. See the Sequencer card for more information about the uses of the input/output registers, this is located on page OPER-107.

The IOCC card also contains the control circuits which monitor the DDC and the CDP tags and commands. These circuits determine the correct control point for various operations. This control point can be the controller sequencer microcode, the DPS circuits or a device.

For a better understanding of what a control point is, here is an example: The IOCC card monitors the DDC Tag Out lines and DDC Bus Out Byte 0 lines from the DDC/DTB card. When the tag lines are in a Command Gate state with a DPS command code on the Bus Out lines, the IOCC card activates the '- DPS command' line. The CDP card uses this signal to select where inbound data is coming from. In this case, from the DPS card.

The IOCC card also provides the Feedthrough circuitry and transfer clock. For more information about these circuits, see page OPER-22

CDP card

The CDP card circuits' main function is to provide the means for connecting the controller to the devices. The CDP's driver/receiver circuits are used by the controller to communicate with the devices across the CDP (Controller Device Port) interface. See page OPER-16 for more information about this interface and its functions. Each CDP card within a controller is capable of handling four ports. Each port has four devices attached to it. In a 4 Path configuration, each controller has 2 CDP cards that will handle up to 32 devices.

The following is a list of functions the CDP card provides the controller:

1. A path and control for information from the DPS card to the IOCC card (only when the 3380-JK is attached to a 3880 storage control)
2. Poll control
3. Assembly of the response information during Summary and Normal Polls
4. Port selection control
5. Gating the data from the selected CDP interface to the IOCC card
6. Error detection and reporting
   a. Checking the response for the device during initial selection
   b. Checking of the CDP interface during Split Bus Mode
   c. Reporting of Port and Device Check 1 conditions
   d. CDP Tag Sequence and Parity checking
   e. Checking for responses from un-selected ports and devices

Sequencer card

The Sequencer card contains the controller sequencer, a microprocessor with no arithmetic and logic unit, whose function is to monitor all and control some of the operations of the controller. The instructions (the controller sequencer microcode), for the sequencer, are contained in Read Only Storage (ROS) modules. The ROS storage are 32K by 24 bits wide and are located within the Sequencer card. All decisions for the sequencer have been designed in advance.

To accomplish the control part of its job, the controller sequencer activates bits within output

registers located on the IOCC card. Activating these bits causes external control signals to be sent to the rest of the controller hardware. An example of the sequencer using the output registers to control the controller: Activating bit 0 in Register 07 (Drive Logic Power Control Register) causes the IOCC card to activate the '+ logic power control 0' line. All devices on port 0 do a power on when this signal is active.

The monitoring part of the controller sequencer's job is done by sensing the contents of the input registers which are also located on the IOCC card. The contents of these registers are controlled by signal lines from the controller hardware circuits.

Depending on the operation, the sequencer is either in complete control using both the output and input registers or it is monitoring, just using the input registers. During both types of operations, the sequencer monitors the controller for errors. When an error is detected (other then controller check 1's), the sequencer takes control and handles the reporting of the failure and its sense bytes.

The Sequencer card also contains the logic that generates the Power On Reset (POR), Extended Power On Reset (EPOR) and the Special EPOR signals. The Power Surge Complete relay is controlled by signals that are generated within the Sequencer card.

DHPLO card

The functions of the DHPLO (Data Handling Phase Locking Oscillator) card are threefold:

- Write Operation Clock

  The DHPLO supplies a clock to the controller's Clock/Serdes/ECC card whose frequency is synchronous to the selected device's spindle speed. This is done by locking the frequency of its oscillator to the servo signal from the selected device. Since the clock is synchronous to the selected device's spindle speed, the data is always written at a constant transition density. Review the write path figure on page OPER-56.

- Read Operation Clock

  Again the DHPLO card supplies the Clock/Serdes/ECC card with a clock signal. This time the frequency of the oscillator is locked to the data being read from the selected device's HDA. This gives the clock a fixed phase relationship to the data, giving the system a better chance of an error free read operation. Review the read path figure on page OPER-60.

- Attachment Clock

  A free running frequency (within specifications) clock is supplied to the controller when not in a read or write operation.

To select the correct read/write servo PLO cable to apply to the frequency control circuits. the DHPLO card uses the port select bits from the IOCC card. The controller sequencer activates the 'lock to servo' signal when it wants the DHPLO to lock to the servo signal and the 'lock to data' signal during a read operation. The DHPLO handles up to eight ports (4 path)

Clock/Serdes/ECC card

(see the Clock/Serdes/ECC cards in the figures on page OPER-56 and OPER-60)

The primary function of the Clock/Serdes/ECC card is to provide data to and from the devices. Data received (during a write) from the storage control through the DDC/DTB card is serialized, encoded, synchronized to the device and then sent to the selected device through the DHPLO card. Before the data is serialized it is used to generate error checking and correction bytes, which are also stored on the HDA of the selected device. Data received (during a read) from the device through the DHPLO card is decoded, de-serialized, ECC verified and sent to the storage control through the DDC/DTB card.

Clocking pulses that are received from the DHPLO card are used to generate system clock signals that are used throughout the controller for for every function. These clocks are also used to synchronize the controller's hardware circuits and microcode to the selected device. During a write, the synchronization is to the device's servo signal. During a read, it is to the data itself.

The clock and serdes circuits perform their functions under the control of the controller sequencer. The sequencer maintains this control using the Serdes Mode bits. Review page OPER-64 for more information on the mode bits.

The following paragraphs are on some of the unique circuits within the Clock/Serdes/ECC card.

Encoder/Decoder Circuits

(see OPER-56) The encoder converts the serial bit stream from the two Serdes registers into a special code for writing on the disks. The conversion is not bit-for-bit, but operates on groups of bits. In the encoded output, consecutive one-bits are separated by at least two and not more than seven zero-bits.

The rate of input to the encoder is approximately 24 megabits per second. The rate of output is approximately 48 megabits per second.

Only the one bits produce a transition on the disk.

The decoder circuits, during a read operation, convert the data from the HDA that was encoded by the encoder circuits. The output of the decoder is sent to the two Serdes registers and to the sync byte and address mark detection circuits.

Precomp Circuits

(see OPER-56) These circuits compensate for the affect that adjacent transitions on a disk have on each other. Transitions tend to repel transitions.

To compensate for the physical shift that occurs when transitions (bits) occur close together, the data is loaded serially in a shift register. This shift register has enough positions so that it contains data that has already been sent to the DHPLO (Data Handling Phase Locked Oscillator) card, the current data bit, and the data that will be sent to the DHPLO card. The data being sent to the DHPLO card always passes through a very short delay. The status of past bits and future bit (in the shift register) combine to select the delay for the current data bit to cause the bit to be earlier or later.

As a result, the physical placement of the transitions is such that the bits can be read correctly.

The precompensation circuits are used to change the delay for bit times during write operations for the inner band read/write heads. During write operations in the outer bands, the bit delay is constant.

ECC Circuits

The error checking and correction circuits are used during read and write operations to provide a way to check the accuracy of data operations and to supply a way to correct some data errors within the subsystem during the read process. Review page OPER-65 for more information on the function of the ECC circuits.

The ECC circuits perform their functions under the control of the controller sequencer. The sequencer maintains this control using the ECC Mode bits. Review page OPER-64 for more information on the mode bits.

MD Adapter card

The MD adapter card permits communication between the CE's maintenance device and the selected storage control to which the 3380-JK is attached. This communication is accomplished the storage control polling the maintenance device as it would any other device. The MD Adapter card also has circuits that will collect sense bytes in parallel with the storage control.

Controller Sequencer Microcode

The microcode provides the instructions that the controller sequencer uses to direct and monitor the functions of the controller. The controller sequencer microcode is organized into modules (routines) that are named by the functions performed during their execution. The modules themselves are divided into two modes; those that are executed when the controller is in immediate mode and those that are executed when the controller is in extended mode.

Immediate mode modules are as follows:

1. The Device Power On module - The microcode is trapped to this routine by a power on reset. Before powering on the devices, the microcode determines if it is within the controller with the highest priority (A1 then A2 etc). When it is the highest priority controller, the microcode takes control of providing the signals to the devices that causes them to power on. Once the devices are powered on, the sequencer attempts to select each device, and if able, issues a Start Spindle Power On command to the selected device. During this routine, the microcode also initializes and tests all of its input and output registers and resets the serdes, ECC and controller check circuits.

2. The CCA and Unfenced Initialization module - The microcode is again trapped to this routine but by the RCC sequence this time. (See page OPER-113 for more information about the RCC sequence) During the execution of this routine, the microcode initializes and tests it's registers and resets the serdes, ECC and controller check circuits.

   Both the Device Power On module and the CCA and Unfenced Initialization module drop into the Unselected Wait Loop module when they have completed without failure.

3. The Unselected Wait Loop module and the Selected Wait Loop module - These modules are both used when the microcode is not directing a controller function. The Unselected Wait Loop is used while the controller is not selected and is not involved in a poll. When a device is selected, this module causes the DHPLO oscillator to lock to that device's signal before dropping into the Selected Wait Loop.

   The Selected Wait Loop module contains microcode that tests for the presence of commands. If an immediate controller command is received from the storage control, the sequencer branches to the Command Decoder and Handler module. If the storage control sends a device or a DPS command, the sequencer remains in the selected wait loop and monitors the exchange of information between the storage control and the device or DPS circuits. If a controller check 2 occurs or if a response from either the device or the DPS circuits is overdue, the controller sequencer takes control of its end of the DDC interface and branches to the Exception Handler module.

4. The Command Decoder and Handler module - This module has a series of routines that decode and execute the controller immediate command that has been received. (See page OPER-91 for more information on Controller Immediate Commands.)

5. The Exception Handler module - The microcode tests for the cause of the error condition and prepares an end op code to identify the cause. The sequencer then sends the end op code to the storage control on the DDC Bus In Byte 1 bus and validates the end op code with an End Op tag state.

If, while in the Command Decoder and Handler module, the Start Read/Write command is decoded, the sequencer changes to the extended mode and the microcode enters the Extended Un-oriented Command Decoder module. This module contains microcode routines that;

- Send an End-Op Tag In (which is needed by the storage control before the next Command Gate Tag Out can be sent).
- Test for a Command Gate Tag Out.
- Decode the command code when a Command Gate Tag Out is found.
- Branch to the module for any extended unoriented command decoded, or prepare an end-op code if an extended unoriented command is not decoded.

The commands that can be processed that do not lead to orientation are End Read/Write, Sense ECC Bytes, and Time Delay. These commands are described under the heading of 'Extended Commands' on page OPER-83. The End Read/Write command does one other important thing to the sequencer; it drops it back into the immediate mode. The extended unoriented commands that lead to orientation are Space From Index, Pad From Index, and Read-A,R commands, which are also described under the 'Extended Commands' heading. During these commands, the controller sequencer branches from module to module as the operation progresses.

For example, during the execution of a Pad From Index command, the controller sequencer first executes microcode in the space and pad from index commands module. In that module, the sequencer sets up controls for the Read/Write Channel board and for the Serdes circuits and then waits for index to occur. When index does occurs, the sequencer waits for the index signal to end, then prepares an end-op code and sends an End-Op tag to report the index to the storage control. (See page OPER-30 for more information on how the sequencer detects the index signal from the selected device.) Next, the microcode starts padding (by activating the 'write gate' lines to the Read/Write Channel board), and then stops the clock ring to achieve orientation and clock synchronization to the next cell boundary. (See OPER-26) After the clock starts at the cell boundary, the sequencer is blocked into 16-step groups. (Each group corresponds with a cell) When finished, the microcode enters the space and pads command module. In this module, the controller sequencer counts to the end of the current cell and for four more cells. Then, the sequencer branches to the auto-op processing module.

In the auto-op processing module, the controller sequencer tests for the next command. When the Command Gate Tag Out is recognized, the microcode branches immediately to a module that contains the microcode for the new command code.

The read commands, write commands, clock commands. and erase commands all involve data transfers between the controller and the storage control. During the execution of each of these commands, the controller normally executes routines from four modules.

The first module used is one of the start-up modules (Read, Clock, or Write/Erase) in which the operation is set up and the data transfer is started. The sequencer then branches to the data transfer module. The microcode in the data transfer module monitors the transfer of data and tests twice in each cell for a stop signal (DDC Tag Out lines changed to the Command Gate state) When the stop signal is found, the controller sequencer branches to the correct stop module. (Read/Clock, Write or Erase) These modules control the ending of the commanded function. The time that the stop signal is found active during the execution of read commands and write commands determines the next part of the operation.

When the commanded function ends without errors, the controller sequencer branches to the auto-op processing module. In this module, the microcode sends the End-Op Tag In to indicate the completion of the commanded function and tests for the next command.

Failure Detection and Reporting

The 3380-JK detects data errors and hardware faults which affect normal machine operation. This detection is achieved using both hardware fault detection circuits and microcode self checking routines. In addition, the storage control that the 3380-JK is attached to is expected to detect certain faults that occur both within the 3380, and on the DDC interface.

Most hardware failures that occur within the 3380 result in a hardware check latch being set. Other failures are detected by the microcode operating within the controller, device or the digital servo (Digital Control Processor - DCP). These microcode routines control the functions of the hardware and constantly test for correct operation. While these two methods of error detection are highly effective, there are certain error conditions that cannot be detected within the 3380.

The storage control has the responsibility to provide an additional level of error detection using both hardware and microcode checking. See page OPER-120 for more information about this level of detection.

Errors that are detected within the 3380 are presented to the storage control by either raising the Connection Check Alert (CCA) lines or by presenting a non-zero End Op response code. The 3380-JK raises the CCA lines when a controller check 1 failure has been detected. A non-zero End Op response code indicates that the controller sequencer microcode has detected a controller check 2 condition. The bits in the non-zero End Op response code have the following meanings:

Bit	Bit Definition
0	Index Found

1 No Sync Byte and No Data Found
2 Check Condition Bit*
3 Check Condition Bit*
4 Message Bit Value 8
5 Message Bit Value 4
6 Message Bit Value 2
7 Message Bit Value 1

* See the next chart.

Bit 2	Bit 3	Check Conditions
0	0	DDC Errors, Data Checks, and Device Time-outs on Selection
0	1	Controller Check 2s (Device Check 1s also)
1	0	Device Check 2s
1	1	Not Used

The controller check 2 failure may be detected by either the hardware error detection circuits or by the microcode itself. A Device Check 1 failure is considered a controller check 2. All subsystem failures are presented to the system by the storage control.

Once the storage control recognizes that a error condition exists, it has to do the following:

- Categorize the failure (determine the which format to use to present the failure)
- Collect the appropriate sense information for the failure
- Generate a two byte Fault Symptom Code - FSC - (this code attempts to summarize the error condition)
- Present the FSC and the sense information to the system

If during the execution of a DDC command, multiple error conditions exist at any level of detection such that a decision must be made as to which error to present to the system, the storage control uses the following priority:

1. Equipment Checks
    a. Storage Control Check 2 errors (including BIDI Bus 0 or Tag Out faults)
    b. Controller Check 1 errors
    c. Controller Check 2 errors (including BIDI Bus 1 or Tag In faults) or Device Check 1 errors
    d. Device Check 2 errors (excluding Seek Checks)
2. Seek Checks
3. Data Checks

Failure detection and reporting will be explained in six sections, they are as follows:

- Controller Check 1
- Controller Check 2 or Device Check 1
- Device Check 2
- Data Checks
- Under Voltage Detection
- Storage Control Detected Failures

Controller Check 1 Errors

A Controller Check 1 error is defined as follows:

- Any condition detected by the hardware or microcode that makes it impossible to guarantee the integrity of the communication link across the DDC interface. The hardware detection circuits or the microcode can be located in either the 3380-JK or the storage control. Some of the failures are operation dependent; what is a controller check 1 condition when the DDC interface is in control mode will be a controller check 2 failure during data transfer mode.

The controller sequencer microcode and the controller logic (except the DPS, DHPLO and CDP cards) detect controller check 1 failures. The microcode and hardware circuits report the failures to the DDC/DTB card by activating a check 1 signal line that defines the type error. The microcode also stores a failure description byte in a register within the sequencer card that is later sent to the storage control.

The check 1 lines activate a Connection Check Shift Register (CCSR) latch (each signal line has their own latch). The CCSR is a 16-bit shift register on the DDC/DTB card, the purpose of which is to store any check 1 and report it to the storage control. A check 1 signal line being active also activates the Connection Check Alert (CCA) latch in the CCSR register. The setting of this latch causes the DDC/DTB card to activate four signal lines, they are:

- 'Trap Check 1' - Traps the sequencer microcode address register to address '000'.
- 'Check 1/RCC' - Stops the system clocks on Clock/Serdes/ECC card. (This will prevent the microcode from doing any instructions.)
- 'CCA Latch' - causes the DPS card to isolate itself from the DPS card in the other controller.
- DDC Conn Check Alert - Notifies the storage control of the controller check 1 condition.

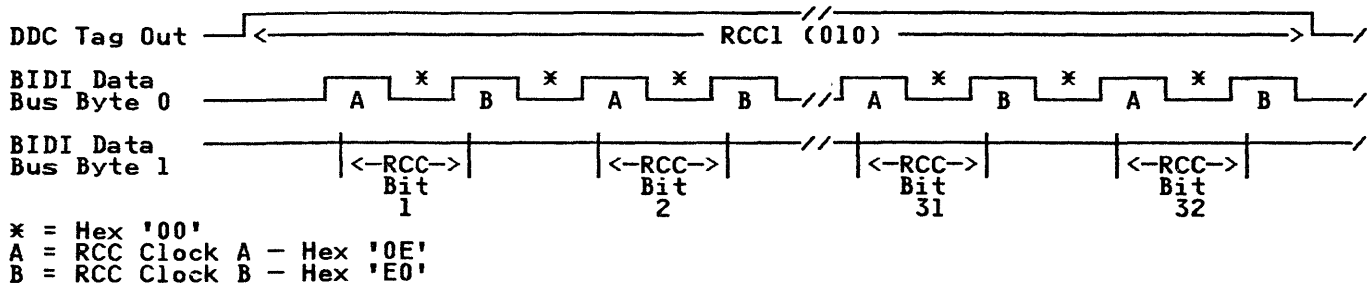
Request Connection Check (RCC) Sequence

Check conditions that cannot be communicated across the DDC.interface by normal sense commands (controller check 1), must still recover from the controller's error latches for fault isolation and recovery purposes. The Request Connection Check Sequences (RCC1 and RCC2) provide a means of scanning out these latches when normal DDC communication is suspect.

An active CCA line indicates (to the storage control) that a least one controller has detected a controller check 1 failure. The storage control then initiate the RCC sequence to both controllers, not knowing which controller activated the CCA line. There is no difference between RCC1 sequence and the RCC2 sequence except the tag state that starts the sequence. RCC2 is used when an RCC1 sequence has failed. The Request Connection Check sequence is as follows: (Review the figure on page OPER-113 for more information)

- The storage control changes the DDC Tag Out lines to either RCC1 (010) or RCC2 (101) and the BIDI Data Bus Byte 0 bus hex '00'.
- All controllers on that DDC interface decode the Tag Out lines, causing them to de-gate all inputs to BIDI Data Bus Byte 1 bus, de-gate all error circuitry that could change the state of the CCSR register. This is done in order to preserve all initial check conditions.
- The storage control changes the BIDI Data Bus Byte 0 to RCC Clock A (hex '0E).
- The decode of the RCC Clock A shifts the check 1 bits from the CCSR primary latch to the CCSR secondary latch in both controllers. This places the first bit on BIDI Data Bus Byte 1. The controllers use their string address switches (either 0 or 1) to determine which BIDI Data Bus Byte 1 bit (Bit 0 for string 0 and bit 1 for string 1) to gate its Check 1 bits onto.
- The storage control changes the BIDI Data Bus Byte 0 to hex '00' and then to RCC Clock B (hex 'E0') to shift the second check bit from the secondary latch to the next primary latch.
- The BIDI Data Bus Byte 0 is then returned to hex '00' and then to RCC Clock A.
- The decode of RCC Clock A shifts the second CCSR bit onto the BIDI Data Bus Byte 1.
- The Third and succeeding bits of the controller CCSR register are shifted onto the BIDI Data Bus Byte 1 in the same manner.
- When all 16 bits of the CCSR have been sent to the storage control, the input to the BIDI Data Bus is shifted from the CCSR to registers in the sequencer card. During the shift an active bit is sent to the storage control. This bit (bit 16), along with bit 15 (always 0 for a 3380-JK) identifies that the RCC sequence is coming from a 3380-JK.
- Using the same clocking sequence (RCC Clock A - Hex '00' - RCC Clock B - Hex '00') the register that contains the failure description byte used by the microcode is read out (8 bytes, 17 through 24).
- The last 8 bits (25 through 32) come from different places within the sequencer (see OPER-114 for more information on what each of the RCC bits represent).

All RCC sequences transfer 33 bits; bit 32 must equal one and bit 32 must equal zero to verify that the controller is transferring data. All other bits depend on the RCC format as specified in the two RCC Format indicator bits. When the RCC sequence is complete, both controllers in a fenced condition. (see page OPER-125 for more information on controller fencing)



Hardware Immediate Sequence

Unlike the RCC sequence (not selective), the Hardware Immediate Sequence only goes to the selected controller. This is to allow a selective reset (leaves a controller with problems fenced). Before the sequence can be started, the DDC Tag Out and the DDC TAG In must be in the Null state. The Hardware Immediate sequence is as follows:

- The command modifier byte (all zero's except bit 2 which indicates which string)is placed on the BIDI Data Bus Byte 0 bus.
- The storage control changes the state of the DDC TAG Out lines to the Poll state (100). (This is to maintain tag sequence validity.)
- The storage control then changes it to the Hardware Immediate state (110).
- The DDC/DTB circuits decode the TAG Out lines, it activates and deactivates lines that reset check 1 latches, allows the system clocks to run and the microcode start to do instructions from address '000'. The circuits also un-fences its DDC drivers and changes the DDC Tag In to the Sync In or Valid (01) state.
- To maintain tag sequence validity, the storage control changes the DDC Tag Out lines to the Poll state.
- The controller changes the TAG In lines to the Null state.
- The last step of the sequence is when the storage control changes the DDC Tag Out to the Null state.

Request Connection Check Bits (0 through 32)

See the figure on page OPER-114 for a break down of the 33 bits sent to the storage control during a RCC sequence.

0 A V | 1 A V | 2 A V = IOC Card Isolation Bits

0 A V	1 A V	2 A V	Description
0	0	1	IOC ROS Bit Parity Check
0	1	0	IOC Transfer Clock Check
0	1	1	IOC Detected DDC Bus Out Parity Check
1	0	0	IOC Register Data Bus Parity Check
1	0	1	IOC Register 1 Parity Check
1	1	0	IOC Register 3 Parity Check
1	1	1	IOC Controller Selection Check

Figure 28. IOC Card Isolation Bits

RCC Bit	Description	Format 7 Sense Byte for Controller '0'	Format 7 Sense Byte for Controller '1'	Sense Bit
0	This Controllers CCA latch was set.	11–0[1]	11–1[1]	1
1	The alternate Controller's DPS received an Unconditional Reserve command	11–2[2]	11–3[2]	2
2 3 4	IOC Card Isolation Bit '0'* IOC Card Isolation Bit '1'* IOC Card Isolation Bit '2'*	12 12 12	14 14 14	0 1 2
5	DDC Bus Out Parity Check (Byte 0)	12	14	3
6	Controller Clock Check	12	14	4
7	Controller Sequencer Check	12	14	5
8	DDC Bus In Parity Check (Byte 1)	12	14	6
9	IOCC Card Check	12	14	7
10	DDC Tag Out Sequence Check	13	15	0
11	Extended Command, Tag Sequence Check	13	15	1
12	Controller Seq. Microcode Detected Check	13	15	2
13	Controller Gate DDC Drivers Check	13	15	3
14	RCC Sequence Check	13	15	4
15 16	RCC Format Indicator Bits (15 and 16 = 01 = 3380–JK)	NONE NONE	NONE NONE	
17 to 24	The Controller Sequencer Microcode Detected Check–1 Description Byte**	16	18	0 to 7
25	Controller Under–Voltage	17	19	0
26 27	Controller Location – 00 = A1, 01 = A2, 10 = A3 and 11 = A4	NONE NONE	NONE NONE	
28	Always '1'	NONE	NONE	
29	The Power Sequence Complete bit is set	17	19	4
30	Controller Check–2 Active	17	19	5
31	Successful Transfer Complete (Always '1')	17	19	6
32	Stop Bit (Always '0')	17	19	7

* The IOC Card Isolation Bit combinations are explained in the chart on page OPER–114.
** The Controller Sequencer Microcode Detected Check–1 Description Bytes are defined on page SENSE–80.

Figure 27. RCC bits

Controller Check 2 and Device Check 1 Errors

A controller check 2 failure is any controller failure that does not qualify as a controller check 1 (a failure that indicates that the normal DDC communication path is not functioning correctly). Some DDC interface failures that are controller check 1s when the interface is in control mode, are controller check 2s during data transfer mode (example: DDC Bus In Parity Check). The controller hardware circuits, microcode and the storage control's hardware and microcode can detect controller check 2 failures. A device check 1 failure is reported as controller check 2 condition.

Controller Check 2

All the logic cards, in the controller, have circuitry for detecting controller check 2 failures. To report a failure, the card circuitry sets a fault log latch (all controller cards have a one byte wide fault log, each latch within the log indicates a different failure) and then activates the '+ act check 2' signal. This signal is dot OR'ed with the same signal from all the other cards, and sent to the IOCC card. Within the IOCC card, the active check 2 signal sets a register bit that is detected by the sequencer microcode. The microcode sends an end op response code to the storage control that indicates that a controller check 2 has been detected.

To collect sense data for the controller check 2 condition, the storage control issues the Sense Fault Log command to the controller. The controller causes the fault logs within the logic cards to be read out to the storage control, one log at a time (fault log A through G). The CDP card has two faults logs; one for its own circuitry failures and one for the device check 1 failures. At the end of the sense fault log microcode routine, the sequencer causes the IOCC card to activate the check 2 reset signals and the port check 1 reset signal. These signals reset the error collection circuits (fault logs).

The controller sequencer microcode, during its normal operation, can detect controller check 2 failures. When one is detected, the microcode sets a value into a register that describes the failure and then sends the storage control a check 2 end op code (hex '12' controller sequencer microcode detected error). The storage control issues the Sense Check 2 Register command, which causes the contents of that register to be sent inbound. A lot of these failures are index and cell detection by the sequencer.

Device Check 1

A device check 1 is any failure that brings the integrity of the CDP (Controller Device Port) interface under suspicion. These errors fall into two categories, they are:

1. CDP Check

   Failures that are common to a CDP interface, such as CDP parity check, Tag Out sequence check and Selection check (a second controller tries to select an already selected device). These errors indicate a broken interface and affect only one controller. (This type of failure is only reported if the device is selected across the failing interface.)

2. Port Check

   Failure in the device logic that are common to all controllers. Examples: CDP data in parity check, funnel selection check, funnel parity check and Clock check. A port check 1 condition will reset the customer's ready light; a CDP check will not.

All device check 1's are detected by the Port R/W Control card with the exception of the Clock check. This check is detected by the Common Power card which reports the failure to both devices on the drive. The port card handles the reporting of device check 1 failure to the controller for the device.

An active '+ port check 1' signal informs the controller that the selected device has a device check 1 condition. (The CDP card sets a fault log latch and activates the active check 2 signal.) This signal can only be activated by the selected device. During the collection of the fault logs in the controller, the sequencer will active the '+ gate port device check 1' signal. This will let an unselected device, with an active device check 1 condition, report it (only then, if it is on the same port with the selected device).

At the end of the fault log collection, the controller not only activate the check 2 reset signal but the '+ port check 1 reset' signal also. This signal is used to reset the check circuits.

Device Check 2 Errors

A Device check 2 error is any device failure that does not indicate a possible CDP communication failure (Device check 1). These failures are detected by the device's hardware or microcode. There are 8 types of device check 2 errors, as indicated by the device check 2 status byte; they are: (See the ECD section for a more detailed explanation of each of these checks.)

1. Device Sequencer Check
2. Servo Control Check
3. Rotational Position Sensing (RPS) Check
4. Checkpoint Check
5. HDA Cable Swap Check
6. Read/Write Check
7. Power Card Check
8. Funnel Parity Check

All of these failures, with the exception of the Checkpoint Check and Servo Control Check are detected only by hardware circuits on the logic cards. The Checkpoint Checks are the failures that are detected by device sequencer microcode. The Servo Control Checks are failures that are detected by Digital Control Processor (DCP) sequencer hardware that monitors the operation of the SEQ-DCP interface. When the DCP microcode detects a failure, a value that represents the failure is stored into a checkpoint register within the sequencer card. The type and time of the failure determines what else the sequencer or DCP microcode will do to report and recover. Examples of options that are open to the sequencer: Set Seek Incomplete, Activate Servo inhibit, activate the Power Amp Inhibit signal.

The one thing all device check 2 errors do is activate signal lines to the port circuitry on the Port R/W Control card (example: '- act RPS check'). Each one of these lines sets a bit in the device check 2 status register and causes the setting of the device error bit in the device status 1 register.

If the device error bit is set, when the device was selected, the Port R/W Control card changes the CDP Tag In lines to an End Op. The controller detects the tag change and takes control, sending the storage control an end op code indicating a device check 2 (hex '20'). If the device was not selected, but owed the storage control an interrupt, (example: seek complete) the device would present an interrupt on the next poll. The storage control then selects the device and issues the Sense Device Status 1 command to determine what caused the interrupt. If the device was not selected and it did not owe an interrupt, the failure reporting would wait until the next selection. Once the storage control detects that a device check 2 condition is active (either receiving an end op or detecting the device error bit active in the device status 1 byte), it will issue the necessary sense commands to generate format 1 or 9 sense bytes.

The Port R/W Control card handle most of the sense commands by decoding the command and activating a corresponding gate signal (example: '+ gate checkpoint reg'). These gate signals cause the check circuits to send the requested sense bytes to the port hardware. The Port R/W Control card sends the sense bytes to the storage control. Once the storage control has collected all the sense bytes, it issues the Reset Device Checks command.

Data Checks Errors

A Data Check is an error condition that is detected by the controller logic during a read operation. It indicates that the data that was read from the selected device is not correct. A Data Check is presented to the storage control by one of the following End Op response codes:

- End Op Response Code Hex '02' (Sync Byte Missing But Data Found)

  The controller logic (Clock/Serdes/ECC card) was unable to detect a Sync Byte. However, there was an indication that some data was found on the track. This error can occur during the reading of the Home Address, Count, Key or Data areas. (During a read the sync byte is used to synchronize the controller's clocks and microcode to the data from the selected device.)

- End Op Response Code Hex '03' (Data Check)

The Error Correction Code (ECC) bytes generated during a read operation did not agree with those that were generated when the data was written (no controller under-voltage condition exists).

- End Op Response Code Hex '04' (Data Check with under-voltage condition)

  This is the same failure as End Op Response code hex '03' but there was a controller under-voltage indication at the time of the failure. Review page OPER-118 for more information on the detection and reporting of a controller under-voltage condition.

- End Op Response Code Hex '0D' (No Read Data)

  The controller logic (DHPLO card) sensed no read data for a period of 1200 nanoseconds when read data should have been present. This condition is treated as a Data Check that is uncorrectable on an initial read.

Data Check Recovery and Reporting Procedures

When the storage control receives a Data Check indication (a data check end op code) from the 3380-JK, it issues a Sense ECC Bytes (hex 'E2') command to the appropriate controller, assembles the data check sense bytes (if needed) and enters the Read Retry sequence. The type of data check determines the recovery; the three types of data checks are as follows:

1. Successfully Recovered Without Using ECC (Temporary)

   During the Read Retry sequence the data was successfully read without detecting a data check. The successful reading could be due to simply rereading the data or due to a head offset operation performed as part of the Read Retry sequence.

   Every temporary data check that is recovered using an offset routine will be reported to the Environmental Recording Data Sets (ERDS). The data checks that are read successfully by just doing a read retry are not sent to the ERDS unless the device has reached data check threshold and is in logging mode.

2. Successful Recovery Using ECC (Correctable)

   The storage control was able to correct the data using Error Correction Code (ECC) correction. The data may have been correctable on the first read, or may have become correctable during the Read Retry sequence.

   The data checks that are correctable on the first read or any read where offset is not active will not sent to the ERDS unless the device has reached data check threshold and is in logging mode. All data checks that become correctable using an offset routine will be reported to the Environmental Recording Data Sets (ERDS).

3. Unrecoverable Data Checks (Permanent)

   The Data could not be successfully read using and of the read retry procedures, i.e. ECC or head offset.

   All permanent data checks are reported with there sense bytes to the ERDS.

Under-Voltage Detection

The 3380-JK under voltage detection circuitry provides an early warning indication of voltages that are marginally low. Certain controller and device logic board voltages are monitored. Detecting an under voltage indication does not cause a failure to be reported. When an error occurs, other than the under voltage indication, the under voltage will be reported with the error.

Controller Under-Voltage Detection and Reporting

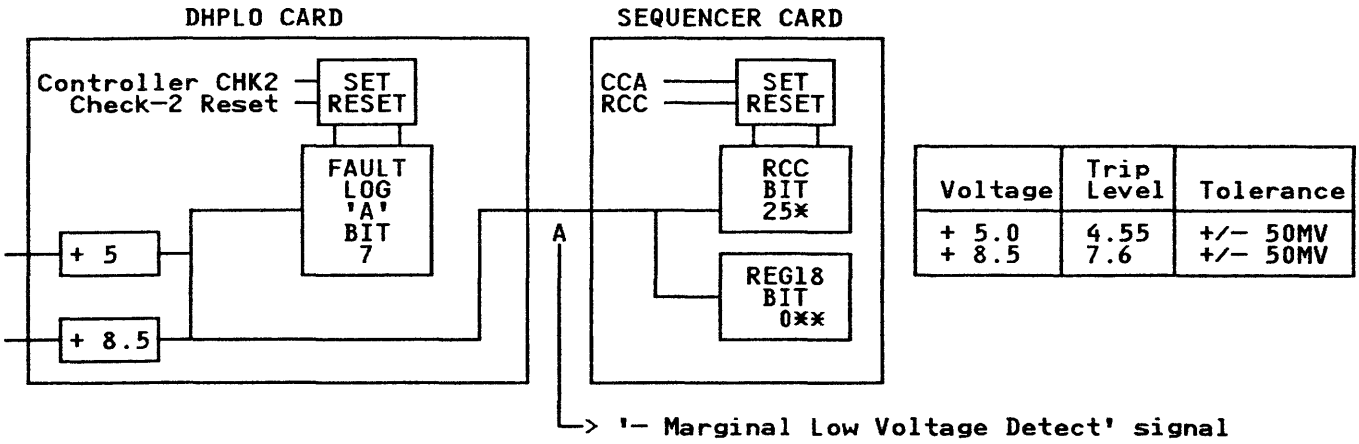
On the controller logic board, the +8.5 VDC and the +5 VDC are monitored by the under voltage detection circuits. The +5 VDC is the one found on the D03 pins of the logic board, not the +5 VDC Special or the +5/24 VDC. The controller under voltage detection circuits are located on the DHPLO card. When the circuits detect an under voltage condition, they activate the - Marginal Low Voltage Detect Signal.

A controller under voltage condition is reported to the storage control with all Controller Check-2 failures (format 8) and all Controller Check-1

failures (format 7). The fault symptom code generator, within the storage control, generates a unique FSC for each format when it receives an under voltage indication.

During format 7 sense byte collection, the Request Connection Check (RCC) bit 25 indicates whether the under voltage signal was active at the time the check 1 failure was detected. This bit controls sense byte 17 bit 0 for controller 0 and sense byte 19 bit 0 for controller 1. The normal state for the sense bit is active (1), a low voltage indication is the inactive (0) state.

All controller Check-2 failures, except 'Controller Sequencer Microcode Detected Error' (End OP 12), report an active under voltage signal by setting Fault Log 'A' bit 7 (format 8 sense byte 11 bit 7). The Controller Sequencer Microcode Detected Error's report the low voltage indication by setting bit 0 active in the failure description byte that is sent to the storage control with the End OP 12 (Sense byte 18).



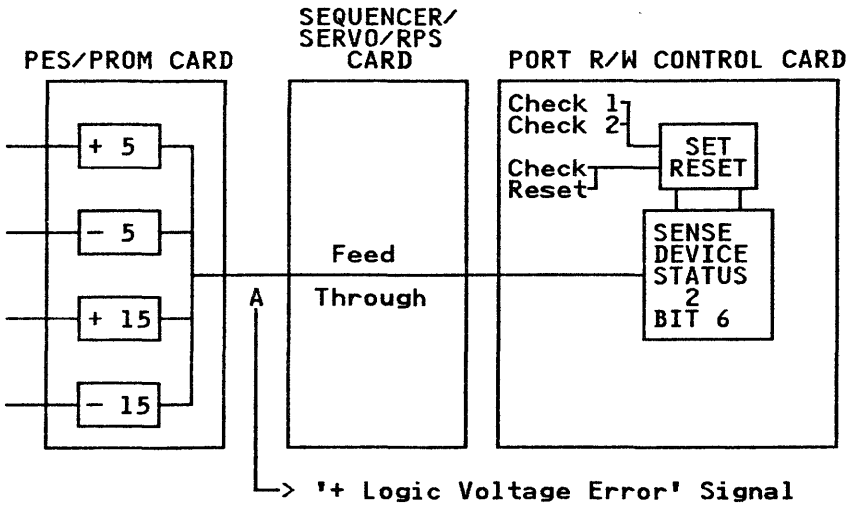
Voltage	Trip Level	Tolerance
+ 5.0	4.55	+/- 50MV
+ 8.5	7.6	+/- 50MV

* The low voltage indication is active when this bit is set to the zero state.
** Register 18 bit 0 is not latched, it's state follows the input signal. This bit allows the microcode to monitor the low voltage signal.

Device Under-Voltage Detection and Reporting

On the device logic board, the +5 VDC, the -5 VDC, the +15 VDC and the -15 VDC are monitored by the under voltage detection circuits. The device under voltage detection circuits are located on the PES/PROM card. When the circuits detect an under voltage condition, they activate the + Logic Voltage Error signal. The low voltage indication signal controls the state of bit 6 in the Device Status 2 Register on the Port R/W Control card. The register is not latched until another device failure is detected.

A device under voltage condition is reported to the storage control with all Device Check-2 failures (format 1 and 9) and all Device Check-1 failures (format 8 - Controller Check-2). Again, as with the controller under voltage, the fault symptom code generator sends the system a unique under voltage FSC for each format. The storage control detects the device under voltage when it issues the Sense Device Status 2 command while collecting failure sense data.



Voltage	Trip Level	Tolerance
+/- 5.0	4.55	+/- 50MV
+/- 15.0	13.5	+/- 300MV

When the under voltage condition is detected and reported, the maintenance analysis procedures (MAPs) will first do the under voltage analysis. Any other error condition will be ignored until the under voltage problem is corrected. The diagnostic routines are designed to sample the under voltage status bits over a fixed period of time, and a common Isolation Code is created if the under voltage bits are active. Just as in the case of the Fault Symptom Code MAPs, the IC MAPs are designed to correct the under voltage condition before analyzing any other error conditions.

Both the controller and device under voltage detection circuits cannot detect a missing voltage.

Storage Control Detected Failures

Storage control detected failures, as with device or controller reported failures, are detected by both the hardware and the microcode. Some of the hardware detected failures are as follows: Bad parity on the DDC Data Bus In lines, Invalid tag sequences on the DDC Tag In lines, Wrong Sync In counts at the end of data transfer. Some of the microcode detected failures are as follows: Head or cylinder address miscompare, a bit stuck active in all sense bytes received, no response from selection after a poll (see the ECD section for more information about these failures). The storage control will report these using the format that is indicated by the type of failure and the operation that was in progress at the time of failure.

Miscellaneous

Subsystem Paths

The 3380-JK direct access storage string can be configured in two path arrangements: 2-path and 4-path. The purpose of 2-path and 4-path configurations is to provide improved path availability and performance of the subsystem over previous configurations.

In order to better understand what is involved in these path configurations, it is necessary to define the subsystem elements that form a 2-path and 4-path string. (Review the figure on page OPER-121 for a better understanding of the definitions that follow.)

The 3990 Storage Control elements that are important to achieve an understanding of path configurations are as follows: the storage cluster, the storage director, the storage path and the shared control array. In the 3380-JK the important elements are the controllers.

A storage cluster is a power and service region containing two independent data paths, and either one multipath storage director or two single-path storage directors. Each storage cluster includes a shared control array and a support facility.

A storage director (SD) is a logical entity consisting of one or more physical storage paths in the same storage cluster.

In 2-path strings the storage paths are defined as single-path storage directors. Single path storage directors are the same as 3880 storage directors.

Each single-path storage director provides a host-addressable path to the 3380-JK.

In 4-path strings the storage clusters are defined as two multi-path storage directors. The multi-path storage director provides host-addressable multi-path access to the 3380-JK. Through one storage director address, the multi-path storage selects either storage path in the cluster for data transfer operations.

A storage path (SP) controls data transfer operations between the channel and the 3380-JK.

The shared control array (SCA) contains status information about the storage paths and devices in both storage clusters. In a 3880 subsystem, this information was kept in the Dynamic Path Selection (DPS) array of the 3380 controller. The shared control array allows the storage director to get the device status and reconnection data faster because it is already resident in the storage control.: In a 2-path string, the shared control arrays are logically divided. One half contains information about the storage paths and the devices in its own cluster and the other half contains the same type of information about the other cluster. Sharing information in this way ensures that data is accessible through a second path in the event of a failure in the first path. In a 4-path string, the shared control array is a single logical array shared by all storage paths.

The support facility is a service processor that provides IML capability and maintenance features such as maintaining storage cluster errors, soft copy MAPS.

The 3380-JK Controller has different capabilities from previous models of 3380 DASD. In a 2-path configuration the 3380-JK is essentially the same as the 3380 D/E, but in a 4-path configuration a number of changes have been made. The 4-path controller is logically and physically connected so that two 2-path controllers (a total of 4 controllers) can communicate with each others devices. To accomplish this the DPS array has been moved to the 3990 and four additional CDP ports have been added to the controller function.

2-Path and 4-Path Configurations.

A 2-path string consists of two single-path storage directors and the devices attached to those storage directors. A 2-path string can transfer data to or from any two devices within the string, including both devices on a head disk assembly (HDA).

A 4-path subsystem consists of two multi-path storage directors and 3380-JK devices attached to those storage directors. In a 4-path subsystem, the storage cluster becomes the storage director and allocates the storage paths for data transfer operations, independent of host processor program control. A 4-path string permits concurrent data transfer with any four devices within a string, including those of the same HDA.

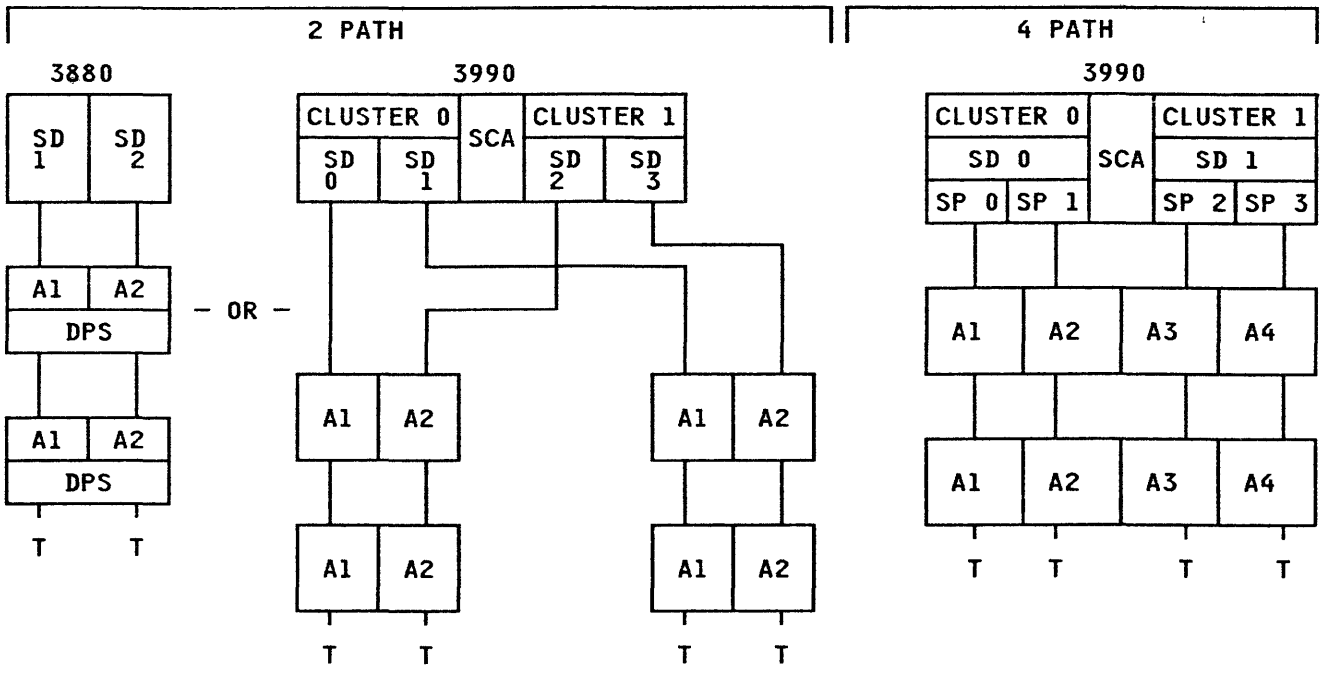


Figure 29. 2 Path and Simple 4 Path Configurations

The figure on page OPER-121 shows the 3380-JK in a 2 path configuration with a 3880 and a 3990. The figure also shows a very simple 4-path configuration. (See the Install section for more complicated 4-path and mixed configurations.)

The 2-path example, using a 3880, could have any 3380 model attached to it. Any device on either string can be accessed by either storage director.

The 2-path subsystem example, using a 3990 storage control unit, has two storage clusters. Each storage cluster has two single path storage directors and a shared control array. The four strings of attached DASD could either be 3380-JK and/or 3380 D/E and/or 3380 Standards (stage 2). A device in any string can be accessed by either storage cluster through the appropriate single path storage director.

The 4-path subsystem example is the simplest of the 4-path configurations. Each of these storage clusters has one multi-path storage director controlling two storage paths. The two strings of attached DASD can only be 3380-JK's (up to 64 devices). A device in either string can be accessed by either storage cluster through either of its storage paths and the storage paths of the other cluster.

Quiesce and Resume Commands

The Quiesce and Resume commands are a function of the 3990 Storage Control Unit, but because it is used to service the 3380-JK subsystem a short explanation follows.

The Quiesce command allows a Customer Engineer to service a part of a 2-path or 4-path 3990/3380-JK subsystem. By issuing the appropriate Quiesce command a fence can be set blocking the host processor from using the indicated element of the subsystem. The following is a list of subsystem elements that a Quiesce command can be issued against:

- Storage Cluster
- Storage Path
- Device

All Quiesce commands are entered at the 3990 Storage Facility (SF) keyboard. The SF, after receiving the Quiesce command, will send a message to all host processors that are connected on an enabled storage control channel interface. For a Quiesce Storage Cluster, Quiesce Device or a 2-path Quiesce Storage Path, the 'Request Quiesce' message is sent; it will indicate which element of the subsystem the request is for.

When 5 minutes has passed or all hosts have responded, the SF will generate a response, to the CE, giving the results. If all hosts report that the channel paths (cluster or 2-path storage path) or the device have been varied off line, the SF will indicate that the request was successful.

The Quiesce Storage Path command (4-path only), will remove the path for service without issuing a request. An 'Inform Storage Path Quiesce' message will be sent to all the host processors, but no operator action is required. The Quiesce Storage path command will only work when the other storage path within the cluster is fully functional (no fences at any level).

The command which allows the CE to service the 3380-JK controller or the CTL-I (DDC) interface is the Quiesce Storage Path command. Once the Service Facility (SF) has reported that the storage path (SP) was ready to be serviced, the CE can work/install on any controller(s) on the CTL-interface or the interface itself. The storage path, DDC interface and controllers are fenced from all host processors at this time.

After the repair/install action is completed, the CE enters the Resume command at the SF keyboard. The Resume command, like the Quiesce, is a request used for the storage cluster, storage path (2-path) and device. For the storage path (4-path) it is again a notification, not a request. The process in both cases will be handled the same as the Quiesce command.

A storage path that has been fenced for service by the Quiesce Storage Path command, (4-path only) can not be put back into normal service using the normal system vary commands. The CE must enter the Resume command into the Service Facility keyboard.

Unconditional Reserve Release and Reset Allegiance

The Unconditional Reserve Release command and the Reset Allegiance command are used when the operating system needs to break through to a busy or reserved device. This is a device that could not be accessed through normal selection. This is a very drastic error recovery procedure and should not be attempted without the system programmers concurrence.

The Unconditional Reserve Release command is used only on 3380-JK controllers that have the Dynamic Path Selection (DPS) feature installed. The DPS feature is installed when the 3380-JK is attached to a 3880 Storage Control Unit.

An unconditional reserve is accomplished during the selection sequence, at channel address time. (See page OPER-69 for more information about device selection with DPS installed.) Bit 3 (Force Lock Procurement) and bit 4 (Force Device Availability), of the channel address byte, being active is an unconditional reserve command to the DPS circuitry. Bit 3 forces the device lock to be available, even if it is currently held by the alternate controller. Bit 4 forces the device to be available to the selecting channel without regard to the indication in the DPS array.

The alternate controller detects the unconditional reserve command across the Controller to Controller Connection data bus, between DPS cards. The alternate controller notifies its storage control of the command by setting a controller check 1 condition, with the unconditional reserve RCC bit active.

The Reset Allegiance command is used only on 3380-JK controllers that are attached to the 3990 Storage Control units. The Reset Allegiance (33) command is a controller only command that is issued to the controller with a modifier byte identifying the device. The controller sequencer microcode branches to the reset allegiance routine when the command is decoded. The routine starts out by selecting the device, using a selection address byte with the reset allegiance bit (bit 1) active. The device will honor this selection whether it was already selected or not. The controller sequencer microcode will deselect the device and then select the device again to verify the selection operation. The controller sequencer microcode will then deselect the device and report its success to the storage control. If another controller had that device selected when the reset allegiance command was received, an error will be generated to that controller.

System Write Inhibit and Storage Control Fencing

Write inhibit and fencing basically do the same function; they partition off a component within a DASD subsystem that is failing. Partitioning off a component (device, path or cluster) prevents the host processors from using that component. Write inhibit is a function of the system Error Recovery Procedures and is used on both the 3880 and 3990 storage control units. Controller Interface fencing is also used by both storage controls and it has been in use since the beginning of 3380s. Subsystem initiated fencing is only active when a 3380-JK is attached to a 3990 storage control unit in a 4-Path configuration. Both types of fencing are controlled by the storage control unit, where the write inhibit is controlled by the host systems.

System Write Inhibit

Write Inhibit is a condition set for the purpose of protecting existing customer data from a data path failure which could cause the data to be written in error. The Write Inhibit state is initiated by the system Error Recovery Procedures (ERP) in response to a request by the Storage Control unit when it recognizes specific errors detected within a data path component. The path components are the channel, the storage control and the controller.

An explanation of the error recovery procedure which sets Write Inhibit will help you to better understand their use on the 3380-JK.

Whenever any logic fault occurs, the storage control collects the error data to generate a Fault Symptom Code (FSC) and sense bytes. The storage control then signals the system with a Unit Check. The system will issue a Sense command and choose an error recovery procedure based on the unique configuration of sense bits in bytes 0, 1 and 2. In this example, it would be an equipment check.

The ERP saves the first sense data record and then performs ten retries of the failing Channel Command Word (CCW) on the initial failing path. If, by the tenth retry, a successful recovery was not made, and if in the initial sense or during any of the retries, byte 2, bit 6 became active (Write Operation in Progress), the ERP will attempt to identify the portion of the path that failed with the initial sense data and block that path to any future write operations. In addition, the ERP will, even if the Write Operation in Progress was never active, upon detection of an error in the serial data path in the subsystem, block that path to future write operations.

To initiate the write inhibit, the ERP will issue the Diagnostic Control command X'F3', with the subcommand Inhibit Write X'02' and a subcommand modifier byte which specifies the failing data path component; the subcommand modifier bytes are as follows:

1. A hex '20' subcommand modifier byte is sent, if the error format for the 3380-JK was one of the following:

    a. A format 7 with the Write in Progress bit active.
    b. A format 8 with the Write in Progress bit active, except when the FSC is equal to an ED11 (Device Check-1 on selection).
    c. A format 8 without Write in Progress bit active and one of the following:
        - Byte 12 bit 0 active (SERDES CONTROL CHECK).
        - Byte 12 bit 1 active (CLOCK/SERDES/ECC/CARD CHECK).
        - Byte 12 bit 2 active (SERDES PATH CHECK).
        - The FSC equals an ED07 or ED87 (DDC OVERRUN).
        - The FSC equals an EF81 (ECC LOGIC CHECK).

    A modifier of 20 blocks all future write operations through the failing controller. However, in a 4-path 3990 storage control, the condition known as FENCING will bypass the initial storage path and the controller prior to the tenth retry unless, the alternate storage path had previously been fenced for that particular device. This will severely limit the number of times that you see the write inhibit condition as compared to previous models of storage control units. The 3990 is only capable of setting a fencing condition when configured for a 4-path subsystem, a 2-path 3990 subsystem and the 3880 do not have the fencing capability.

2. A hex '40' subcommand modifier byte is sent when the failure indicates that all future write operations through a failing channel should be blocked.

3. A hex '80' subcommand modifier byte is sent when the failure indicates that all future write operations through a failing storage control should be blocked.

A console message, (similar to the following) indicates to the operator, the component of the path that is inhibited by the ERP:

IEA467E PATH (CUU,X) WRITE INHIBITED CONTROLLER FOR ALL WRITE OPERATIONS

If alternate paths are available, which will most likely be the case on a 3990/3380-JK subsystem, the ERP continues the recovery effort. ERP will retry each alternate path to the device ten times. If an alternate path fails, the ERP will again use the above algorithm. If an alternate path is successful, the ERP will issue the following console message for each path that failed:

IEA466I PATH (CUU,X) PERMANENT I/O ERROR (24 sense bytes)

In addition, every path that failed will be varied offline and the following console message will be issued:

IEA469E PATH (CUU,X) HAS BEEN VARIED OFFLINE

The Error Recovery Procedures will never vary off the last path to the device.

If all paths fail, the ERP will issue the following console message:

IEA0001 (CUU,X) PERMANENT I/O ERROR (24 sense bytes)

If the host processor or other host processors attached to the device, (using their own paths) attempt to perform a write operation on the device when the channel path, storage control path, or controller path has been Write Inhibited, the storage control will respond with a unit check. The first two sense bytes will be as follows:

Byte 0 bit 3 active (Equipment Check),
Byte 1 bit 6 active (Write Inhibited).

The host processor's ERP, upon recognition of this pattern, will not retry on the same path. The Error Recovery Procedures will retry it on another path and issue the following console message:

IEA468I WRITE INHIBITED PATH (CUU,X) ENCOUNTERED

In addition, ERP will log a permanent error OBR record using the sense data it received.

Write Inhibit status is reset by either an IML, of the storage control, or by using the ICKDSF control command ALLOWRITE.

Control Interface Fencing

A controller must be fenced when an operation to it causes a permanent controller check 1. When fenced, a controller cannot respond to a storage control unit. Control interface fencing is an operation that results in a failing controller being partitioned off from its DDC interface. This is done to prevent, the failing controller, from interfering with the operation of a second controller on the same interface. To accomplish this, the DDC signal drivers in both controllers are disabled by the storage control with a Request Connection Check Sequence (RCC1 or RCC2). The storage control then issues a Hardware Immediate Sequence to the non-failing controller to restore its signal drivers to normal.

- See page OPER-113 for more information about the RCC sequence.
- See page OPER-114 for more information about the Hardware Immediate Sequence.

The failing controller will remain fenced until restored by either a Hardware Immediate sequence or a power on reset. A Hardware Immediate sequence will be issued whenever a host processor issues a SIO to a device within the fenced controller.

Subsystem Initiated Fencing

Subsystem initiated fencing automatically removes failing components from a DASD 4-Path 3990/3380-JK subsystem. This is done by altering the selection path to a device. In addition, fencing ensures that all available subsystem paths are tried before the system Error Recovery Procedures (ERP) retry activities cause a write inhibit to be issued because of a permanent error. Subsystem fencing also permits better identification of the failing hardware or media in console messages and EREP reports.

The subsystem fencing that is initiated by a 3990 4-path storage path (SP) and its functional microcode has three levels of fencing that are possible. They are as follows:

- Storage Cluster
- Storage Path
- Device

(See page OPER-120 for the definition of a storage cluster and path)

Each level of fencing has a set of threshold counters. Each counter acts as an 8-position shift register, with the most recent event always deleting the oldest event. Microcode determines if three error events occurred after each entry. When three errors are detected in the counter, a process is started that can result in a permanent subsystem fence by the storage control to a storage cluster, storage path or device.

Storage Path to Device Fencing microcode has a counter for each device in the subsystem. These counters are initially used to determine if more than 3 errors occur during the time eight SIOS are issued to the device. If the three errors occur, the storage path applies a temporary device fence that forces the multipath storage director to use the other storage path in that storage cluster for the next selection path to the device.

When a temporary fence is set, the device 3/8 counter in the alternate storage path is modified, by that storage path's microcode, to four errors in 32 SIOs (4/32 counters) mode. If the SP detects four errors prior to 32 SIOs the SP determines that the problem is in the device and not in the path and does not continue the process to set a permanent fence. If however, the alternate path completes 32 SIOs prior to experiencing four errors, the SP determines that there is a pathing problem. A message is sent to the support facility describing the setting of the temporary fence. Upon receipt of the message, the support facility (SF) checks the number of temporary device fences applied to a device attached to the storage path in the last hour to determine if it should set a permanent fence. By including time in the test, a permanent fence is never set by the accumulation of random temporary errors.

The following examples show how a storage path uses the device counters to fence a failing component of a 4-path subsystem.

In attempting to select device 1A, a controller check 2 error is detected. For this example, the device selection path from the channel is through multipath storage director (SD) 1 and storage path (SP) 2 of storage cluster 1, controller A3, and then device 1A of 3380-JK 4-path string. (Use the 4-Path figure on page OPER-121 for reference.) The failing component is controller A3.

A unit check is presented to the channel, in response to the first error, the host processor initiates a system error recovery procedure (ERP) of ten retries of the same CCW string. This is done on the same channel, in an effort by the ERPs to recover from the error. With the second retry, three errors will have occurred before eight successful SIOs have been completed on the selection path. The third error overflows the counter and the storage path sets a temporary fence against the existing selection path. Storage path 2 signals storage path 3 to modify the device 1A counter to 4 failures in 32 SIOs mode. With the next retry, the multipath storage director will use the alternate path to device 1A through storage path 3.

At this point in this example, storage path 3 is now successfully communicating with device 1A through controller A4 and experiences no failures. It will successfully complete the next ERP retry, in addition to the next 32 SIOs through any channel on the multipath storage director to the device. With the overflow of the 32 count, the device counters are reset and modes are reset to the 3 in 8 mode in both storage path 2 and storage path 3. The temporary fence is also removed from storage

path 2. When the support facility receives the temporary fence message from storage path 2, it steps the device counter and performs a test to determine if too many temporary fences were set over a set period of time. When the count is exceeded, and the system has an alternate path to the device available, the support facility instructs storage path 2 to set a permanent fence only for device 1A. As additional device selections fail when selected through storage path 2, they too will eventually have permanent fences set for them. The final result has controller A3 permanently fenced off to all device selections.

In the example, device 1A selections continue to fail with each use of storage path 2, yet it was successful when using storage path 3. When the support facility error threshold for device 1A is exceeded and before it sets a permanent fence, it must verify that all the host processors attached to the subsystem have a remaining unfenced path to device 1A. When the support facility has completed the alternate path verification, it issues a command to storage path 2 to set a permanent fence for device 1A.

In the following example, the failure will be in device 1A instead of controller A3, a different series of events will occur.

In response to the first device error, the system ERP's will initiate ten retries using the same CCW string. The third error will overflow the counter causing storage path 2 to signal multipath storage director 1 to set a temporary fence against the existing selection path. Storage path 2 also signals storage path 3 to modify device 1A's counter to 4 failures in 32 SIOs mode. Storage path 3 is unsuccessful in the next four system ERP retries in communicating with device 1A through controller A4. With the overflow of the error count of 4, device counters in both storage paths are reset and modes are set to the 3 in 8 mode. The temporary fence is also removed from storage path 2. When the support facility receives the temporary fence, and the reset of the temporary fence by 4 additional errors from storage path 3, it steps the device counter each time and perform the rate test.

At this point in this example, the initial selection, plus two ERP retries have occurred by using storage path 2, storage path 2 is fenced, the next four retries occur by using storage path 3, the temporary fence is removed from storage path 2, and the seventh through the ninth ERP retries are performed by using storage path 2. Storage path 2 again signals storage path 3 and the support facility of the fence. Storage path 3 is used for the tenth retry.

The system ERP, having exhausted the retries down one channel path, then attempts to find an alternate channel and subsystem path to device 1A. In this example, it is assumed that the host processor has a channel to multipath storage director 0 in storage cluster 0. The ERP, in finding this path, starts ten retries. The series of events through this storage cluster is exactly the same as the previous cluster. After 10 unsuccessful retries through the alternate path, ERP sends a console message and a record to LOGREC indicating that device 1A had a permanent I/O error. At this point, no subsystem fencing conditions would have been met.

To continue the example, the next system job to use the device will overflow the device counter, this allows a permanent fences to occur. The support facility ensures that at least one unfenced path exists to the device after a permanent fence command is issued.

A New System Message is posted to the system operator after it has been determined that a device should have a permanent fence. The support facility creates a format 0 fault symptom code from which the console message, similar to the following, is sent to the operator:

IEA473I VVVVV fenced from SP X
CUU/SSID.P-SS.C-DD

VVVVV volume id that failed.
X is the Storage Path fenced - sense byte 27, bits 6 and 7.
CUU is the physical address.
SSID is the Subsystem Identifier - sense byte 20 and 21.
P is the Storage Path - sense byte 27, bits 6 and 7.
SS is the string ID - sense byte 3.
X is the controller path - sense byte 4, bits 0 and 1.
DD is the device number - sense byte 4, bits 3 thru 7.

System/Operator Action: None. The subsystem attempts to recover the operation by using an alternate path.

Reset of Subsystem Fencing is accomplished by doing one of the following:

- A specific DEVICE on a specific storage path can be reset by the use of the support facility.
- An IMPL of the storage path.
- A warm start by pushing the 3990 restart button.
- By the using the ICKDSF control command CLEARFENCE.
- A temporary device fence will be reset every time the other storage path, in the multipath storage director, reports either 32 successful SIO's or 4 errors while trying to use the device.

It is important to remember that a reset of the fencing state should only be attempted upon completion of a repair action as directed by the 3990/3380-JK maintenance packages.

EC History of Operation Section

EC HISTORY OF P/N 4519952			
EC Number	Date Of EC	EC Number	Date Of EC
475245	14Nov86	475248	25Apr88
475246	21Jul87		
475247	11Sep87		

Notes:

Introduction

The 3380-JK diagnostic program package contains many individual diagnostic routines operated under a common control program and invoked through use of the Maintenance Device (MD).

Each diagnostic routine is identified by an ID of two hex digits. Each routine can be run independently, and some routines can be linked together to run in sequence. Some routines are divided into tests.

The diagnostic control program and all diagnostic routines are executed on the attached storage control (not in the 3380-JK). The control program normally resides in control storage. The diagnostic routines are loaded into control storage from the storage control IML device as the routines are needed during diagnostic operation. If a routine or test cannot be contained within the available control storage, it may be divided into several sections (overlay loads) which are loaded from the IML device as needed. You should be aware that the IML device may operate continuously during diagnostic routine execution.

In addition to the diagnostic routines, a special diagnostic function is provided to test the connection between the MD, the specified controller, and the storage control. This function is the MD Connection Test, which is run by the controller sequencer. The MD Connection Test is normally used only if trouble is suspected in the connection between the MD, the controller, and the storage control.

Instructions for running the MD Connection Test are contained in the Product Service Guide (PSG). No routine ID is assigned to the MD Connection Test, and it cannot be run under the Diagnostic Aids option. A brief description of the MD Connection Test is included in this section on DIAG-6.

Diagnostic Routine Operating Procedures

Diagnostic routines are always run under control of the MD. See the PSG for basic MD operating procedures.

Diagnostic routines may be run either by selecting option 1 (Run Diagnostics) or option D (Diagnostic Aids) from the main MD option selection menu.

If option 1 is used, diagnostic operation is controlled by the MD. Prompting messages request information when it is needed. See the PSG for more information about running diagnostics under option 1.

The Diagnostic Aids option allows you more control of the diagnostic routines but requires that you more fully understand the routine's operation and control parameters. Any routine may be run using the Diagnostic Aids option, and you have full control of routine execution. But if you enter inappropriate control parameters for the routine being run, some very misleading results can occur.

Controller Selection

When the MD requests that a controller be selected, enter 1, 2, 3, or 4 to select the controller (A1, A2, A3, or A4) to be used. Once a controller is selected the MD will continue to use that controller as a default until another controller is selected.

Warning: If routine 90 (DPS Tests) is run, both controllers must be used. For this routine only, the controller that you select will be the master controller (see routine 90 description). Routine 90 starts first on the slave controller, and then runs on the master controller.

Routine Selection

When the MD requests selection of a routine, enter the two hex-digit routine ID of the diagnostic routine to be run. The following routine IDs can be selected.

80	Controller Tests
81	Device Logic Tests
82	Servo Tests
83	Read/Write Data Transfer Tests
84	Read/Write Function Tests
85	Seek Exerciser
8A	Incremental Seek Exerciser
90*	DPS Tests
91	Home Address Scan
93*	DDC Tests
96	Device Status Test
97	Sense Utility
98	Error Log Search
99	Motor Start Test
9C	CE Track Repair
9D*	DPS Array Display/Dump Utility
9E*	Diagnostic Microcode Patch
9F	Set/Reset/Sense CE Mode
C0*	3380-JK Model A04, AA4 Controller Tests (3880 Maintenance Package Support)
D3*	3380-JK Model A04, AA4 DDC Tests (3880 Maintenance Package Support)

Selection of a routine is always required. If a routine ID is not specified, the MD provides the last routine ID specified by the user as a default value. The default value is initially 80. To use the default value, press the enter key in response to the prompting message.

Warning: Although any of the above routines may be selected, routines 91, 93, 96, 97, 98, 99, 9D, 9E, 9F, C0, and D3 provide special purpose functions and may produce confusing results if run under the Diagnostic Aids option. Refer to individual routine descriptions for additional information.

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* Note: These routines are available only when attached to a 3880 control unit.

Device Selection

When the MD requests that a device be selected, determine if the routine being run requires use of a device. If so, enter the hex address (00 to 0F) of the device to be tested. Routines 81, 82, 83, 84, 85, 8A, 91, 97, 99, and 9C all require that a device be selected.

If the routine does not require use of a device, press the enter key without entering a device address. Routines 80, 90, 93, 96, 98, 9D, 9E, 9F, C0, and D3 do not require device selection but can be run even if a device is selected.

Once a device is selected, the MD continues to use that device address as a default value until a different routine is selected. When a new routine is selected, the default is reset to no device selection. To use the default value, press the enter key in response to the prompting message.

Warning: An attempt to run a diagnostic routine for a device without specifying a device for selection causes an error. The error message that results does not mention that this error can be caused by user failure to specify a device. It is the user's responsibility to ensure that a device is selected when running a device test under the Diagnostic Aids option.

Warning: A device specified for selection must be in CE mode. Failure to set CE mode for the selected device results in IC 1101. Use main option 0 to set or reset CE mode as required.

Parameters

Each diagnostic routine has default parameter values that are correct for the routine so that the entry of control parameters is not usually required. However, in special cases, the user may want to enter parameters to provide some unusual diagnostic function.

When the MD requests that parameters be entered, press the Enter key to use the default parameter values, or enter all of the parameters and then press the enter key.

Each parameter is two hex digits. Up to 16 parameters (numbered 0 to F) may be entered consecutively with no spaces between successive parameters. If more than one parameter is keyed, then all the parameters used by the routine must be keyed before the Enter key is pressed. (Remaining default parameter values are ignored after the second parameter is entered.)

The number of parameters required and the meaning of each parameter (except for parameter 0) varies depending on the routine being run.

The first parameter (parameter 0) is the 'run control' parameter. Parameter 0 provides control functions that are the same for all routines. Some of the run control functions are not appropriate for some of the routines and can cause unexpected results. See the descriptions of the routines for restrictions on the selection of the run control parameter.

The control functions provided by parameter 0 are:

00	Allow Routine Linking, No Loop, Halt On Error
01	Allow Routine Linking, No Loop, Bypass Error Halt
02	Allow Routine Linking, Loop, Halt On Error
03	Allow Routine Linking, Loop, Bypass Error Halt
04	Inhibit Routine Linking, No Loop, Halt On Error
05	Inhibit Routine Linking, No Loop, Bypass Error Halt
06	Inhibit Routine Linking, Loop, Halt On Error
07	Inhibit Routine Linking, Loop, Bypass Error Halt
08 to 0F	Same as 00 to 07
18 to FF	Invalid

The 'Allow Routine Linking' function allows routine 80 to link to routine 96 or allows routines 81 through 85 to link and run in sequence.

If the 'Inhibit Routine Linking' function is selected, or if any routine other than 80 through 85 is selected, only the selected routine is run.

The 'Loop' function causes the selected routine (or linked series of routines) to be repeated. The 'Loop' function in combination with the 'Allow Routine Linking' function causes routines 81 through 85 to repeatedly run in sequence.

If the 'No Loop' function is used, the selected routine or linked series of routines run only once.

The 'Bypass Error Halt' function allows routine execution to continue after an error is detected. This function may be used in combination with the 'Loop' function to create a scope loop.

If the 'Halt On Error' function is selected, routine execution stops and an error message is displayed when an error is detected.

If only the first parameter (Parameter 0) is entered, the default values built into the routine being run are used for the remaining parameters. This permits the user to specify only the "run control" parameter if desired. If more than one parameter is entered, then all parameters applicable to the routine being run should be entered. If too few parameters are entered, the MD supplies 00 for the remaining parameters. If too many parameters are entered, the excess parameters are ignored. The meaning of parameter entries 1 through F varies depending on the routine being run. Refer to the individual routine description for the routine being run for a description of the parameters applicable to that routine.

After parameters have been entered, the MD uses those parameters as default values until a different routine is selected. When a new routine is selected, the default parameter values are reset to the built-in default values for the new routine.

Warning: Entry of parameter values that are incorrect or inappropriate for the routine being run can cause some very confusing or misleading results. See the description for the routine being run for the parameters applicable to that routine.

Routine Linking

Diagnostic routines are normally run individually under the Diagnostic Aids option. However, routines 81 through 85 can be linked to automatically run in sequence. If automatic routine linking is desired, then the appropriate run control parameter must be entered as described in the preceding section. If no parameters are entered, then only the selected routine is run.

Warning: When routine linking is allowed, dynamic messages (described in following sections) cannot be displayed by the MD because linking can occur too fast to be detected by the MD. Therefore, the MD cannot provide any indication as to which of the linked routines is currently running.

Routine Looping

If no parameters are entered, the MD asks if the selected routine is to be looped. If the routine is looped, it is repeated indefinitely until stopped either by the user or by an error halt. If the routine is not looped, it is run only once.

If parameters are entered, the routine looping function is controlled by the run control parameter.

Bypassing Error Halts

When an error condition is detected, or when an executing diagnostic routine has information that is to be transmitted to the MD, the routine normally halts and the MD displays a message. It is sometimes desirable to bypass these halts and allow the routine to continue running.

If no parameters are entered but the user indicates that the routine is to be looped, the MD asks if error halts are to be bypassed.

If parameters are entered, the error halt function is controlled by the run control parameter.

When an error halt is bypassed, the executing routine attempts to recover from the error condition and to continue normal operation. If recovery is successful (or not required), the routine continues normal execution and might run to normal completion. If recovery is unsuccessful, the routine continues to attempt recovery until an attempt is successful or the routine is stopped by the user.

Warning: Error conditions that can cause machine damage and those from which recovery is impossible cannot be bypassed. If such a condition is detected, the error halt occurs.

Stopping Routine Execution

A routine that is in execution may be stopped by the user by pressing any MD key. The routine may then be subsequently restarted from the point of interruption by pressing the enter key.

Diagnostic Error Messages

A diagnostic error message consists of a two byte Isolation Code (IC) and up to fifteen bytes (numbered 1 to F) of additional information.

Diagnostic error messages are used to report error conditions and are also used to transmit many other types of information to the MD. Thus, when diagnostic routines are run under the Diagnostic Aids option, diagnostic error message displays may sometimes occur even though no error has been detected. In fact, some routines normally end with an error message display. See the IC Descriptions in this section for meanings of the isolation codes and the meanings of the bytes displayed with the isolation codes.

Dynamic Message Displays

An executing diagnostic routine may sometimes send an error message to the MD, then automatically continue running. This occurs when an error is detected with error halts bypassed and sometimes occurs during normal routine execution. When this occurs, the IC appears in the "Routine Running" message being displayed by the MD. The 15 additional error bytes are not displayed in this case.

Normal Routine Completion

When a routine runs to normal completion, the MD displays a 'Routine Ended' message. The user may then choose to repeat execution of the same routine or may return to the option selection procedure to perform other diagnostic functions.

MD Connection Test

The MD Connection Test checks the paths between the MD, the controller, and the storage director. The test is divided into three parts that run in sequence. These parts cannot be run separately.

The MD Connection Test requires a dedicated controller. Customer operations cannot be run concurrently with the MD Connection Test through the controller being tested. Before the test is run, each path that uses the controller being tested must be varied off-line for all devices to each system. Devices need not be in CE mode for the test.

The MD Connection Test can be selected by menu. MD Main Menu Option 1 produces the Diagnostic Menu. Option 4 of the Diagnostic Menu selects the

MD Connection Test. The MD Connection Test is also available from any diagnostic during which the MD detects a communications error between the MD and the storage director. Messages from the MD provide instructions.

Parameters

No parameters are needed and no parameters can be used with the MD Connection Test.

Test Description

The first part of the MD Connection Test verifies circuits and paths in the MDA card and in the controller. Several patterns of data are exchanged between the MDA card and the controller sequencer card. Data sent by the MD is returned by the controller sequencer and verified by the MD. (The 'fault log bus' and the 'register data bus' are checked by this part of the test.)

The second part of the MD Connection Test checks more of the controller circuits. Special commands are sent to the controller sequencer to exercise hardware controlled by the controller sequencer.

The third part of the MD Connection Test checks the communications path between the controller and the storage director (which is part of a control unit). In this part of the test, the controller sequencer (instead of hardware) has control of the controller during initial selection from the storage director.

CTL-I Tests

The &sara. diagnostic supervisor supports a special CTL-I test function that allows a Support Facility (SF) application to test the CTL-I using a much simpler sequence of diagnostic control commands and responses than is used by the MD. This special diagnostic function is called the "CTL-I Tests" and is normally used only if a failure occurs that prevents use of the MD.

No routine ID is assigned to the CTL-I Tests. These tests are intended for use only by an SF application. They cannot be run from an MD and are not available when the &sara. is attached to a 3880 control unit.

To invoke the CTL-I Tests, the SF application sends the diagnostic control command 'FF00'X or 'FF01'X to the diagnostic supervisor. The last digit of this command specifies the controller (0 or 1) to be used during the test.

On completion of the CTL-I Tests, the diagnostic supervisor sends a response from two to sixteen bytes in length to the SF. The first two bytes of this response contain an isolation code (IC) and the remaining bytes contain additional information about any detected error. An IC of '00CF'x indicates that no errors were detected.

The CTL-I Tests consist of 8 individual tests that are always run in sequence.

Test 01 - RCC1 Test

Test 01 checks the RCC1 and Partition On (Hang Reset) functions. If an error is detected, an RCC2 sequence is used to verify test results. A failure in test 01 indicates that the RCC1 sequence failed but the RCC2 sequence operated correctly.

Test 02 - RCC2 Test

Test 02 checks the RCC2 and Partition On (Hang Reset) functions. If an error is detected, an RCC1 sequence is used to verify test results. A failure in test 02 indicates that the RCC2 sequence failed but the RCC1 sequence operated correctly.

Test 03 - RCC Test Analysis

Test 03 performs no test functions but completes the analysis of results from tests 01 and 02. A failure in test 03 indicates that errors were detected after both RCC1 and RCC2 sequences.

Test 04 - Bus Out Test

Test 04 uses the RCC1 sequence with several combinations of RCC clock codes to test individual lines on CTL-I bus out.

Test 05 - Poll Test

Test 05 checks CTL-I tag in responses to a poll sequence.

Test 06 - Force Connection Check Alert (CCA)

Test 06 uses an invalid CTL-I tag out sequence to force a Connection Check Alert (CCA)

Test 07 - Bus Out to Bus In Wrap Test

Test 07 uses a series of diagnostic commands to wrap CTL-I bus out to bus in through the controller.

Test 08 - Data Transfer Test

Test 08 uses a series of diagnostic commands to simulate a write operation. This tests the CTL-I at a high data transfer rate.

IC Descriptions

Errors that are detected by the diagnostic routines (or by the MD) are identified by isolation codes (ICs). ICs are generated by the MD based on the source of the error and the error indication received from the diagnostic routines. IC numbers contain four hex digits and conform to the following general rules:

- If the IC is 0001 through 00FF, it identifies an MD detected error.
- If the IC is 11xx, it is common to all routines.
- If the IC is 80xx or higher, it is unique to the routine indicated by the first byte of the IC.

On this and following pages, the ICs are briefly described. The meanings assigned to the error bytes in the MD display for each IC are indicated.

Several MD displays contain the error bytes. The formats are similar. The following figure shows the positions of the error bytes in a typical MD display.

```
* DIAGNOSTIC AIDS *
RTN=**       IC=****
EB=11 2233 4455 6677
 8899 AABB CCDD EEFF
```

Value	Meaning
11	Error Byte 1
22	Error Byte 2
33	Error Byte 3
44	Error Byte 4
55	Error Byte 5
66	Error Byte 6
77	Error Byte 7
88	Error Byte 8
99	Error Byte 9
AA	Error Byte A
BB	Error Byte B
CC	Error Byte C
DD	Error Byte D
EE	Error Byte E
FF	Error Byte F

Some error conditions require that additional DDC operations be performed after error detection to collect the data needed for the error display on the MD. If another error should occur while the needed data is being collected, the collection process is immediately terminated. The IC for the original

error condition is displayed, and those error bytes that were not collected are shown as containing hex FF.

IC 0001 = The MD detected an error condition while attempting to transmit information to the 3380-JK MD adapter. This indicates a problem with the MD, the 3380-JK controller, or attaching cables.

Byte	Name	Reference
1-F	Not Used.	

IC 0002 = The MD was not able to set or sense an MD interrupt. This indicates a problem in the 3380-JK controller.

Byte	Name	Reference
1-F	Not Used.	

IC 0003 = The MD received an invalid response. The MD transmitted control information to the attached storage control and received a response, but the response was invalid. This usually indicates that an invalid operating procedure was used in running a diagnostic routine.

Byte	Name	Reference
1-F	Not Used.	

IC 0004 = A required diagnostic routine was not found on the storage control IML device diskette. Either the wrong diskette is installed in the storage control or the diskette is defective.

Byte	Name	Reference
1-F	Not Used.	

IC 0005 = The MD received an invalid response. The MD transmitted control information to the attached storage control and received a response, but the response was invalid. This usually indicates that an invalid operating procedure was used in running a diagnostic routine.

Byte	Name	Reference
1-F	Not Used.	

IC 0006 = Diagnostic execution was abnormally terminated. The attaching storage control indicated that diagnostic execution was abnormally terminated. This could have been caused by a system reset, contention with another MD on some other part of the system, or a storage control error condition.

Byte	Name	Reference
1-F	Not Used.	

IC 0007 = Diagnostic execution was abnormally terminated. The attaching storage control indicated that diagnostic execution was abnormally terminated because of contention with another MD on some other part of the system.

Byte	Name	Reference
1-F	Not Used.	

IC 0008 = A storage control IML device error was detected while trying to load a diagnostic routine. This indicates either a defective diskette installed in the storage control or a storage control error.

Byte	Name	Reference
1-F	Not Used.	

IC 0009 = The MD detected an error condition while attempting to open the MD adapter port. This indicates a problem with the MD, the 3380-JK controller, or attaching cables.

Byte	Name	Reference
1-F	Not Used.	

IC 0010 = The MD received an invalid response. The MD transmitted control information to the attaching storage control and received a response, but the response was invalid. This usually indicates that an invalid operating procedure was used in running a diagnostic routine.

Byte	Name	Reference
1-F	Not Used.	

IC 002x = The MD detected an error condition while running the MD Connection Tests. This indicates a problem with the MD, the 3380-JK controller, or attaching cables.

Byte	Name	Reference
1-F	Not Used.	

IC 1100 = String Configuration Bytes Data

Byte	Name	Reference
1	Controller Selection Response	
2	Features Byte ('11' hex command)	
3	Configuration Byte ('12' hex command)	
4	String ID ('16' hex command)	
5	Controller Path ('26' hex command)	
6	Unused ('00' hex)	
7	SDID (3880 SDI Reg) or SSID (3380 Model CJ2 SSID 20)	
8	Control Unit Type (See below)	
9	Fault Log B	
A	Storage Path ('00' hex - '03' hex)	
B	Reserved	
C	Reserved	
D	Reserved	
E	Reserved	
F	Reserved	
	Control Unit Type Codes	
	'00' hex - 3880	
	'05' hex - 3990 Model 2	
	'06' hex - 3990 Model 3	
	'0F' hex - 3380 Model CJ2	
	'10' hex - 3990 Model 1	

IC 1101 = The device being tested is not in CE mode.

Byte	Name	Reference
1	Device Address of Device Being Tested	
	Value Range — Meaning	
	00 through 0F — Device (00 through 0F) with Controller 0	
	20 through 2F — Device (00 through 0F) with Controller 1	
	80 through 8F — Device (10 through 1F) with Controller 0	
	A0 through AF — Device (10 through 1F) with Controller 1	
2-F	Not Used.	

IC 1110 = Unexpected Controller Check-1. Either an unexpected Connection Check Alert (CCA) occurred or an expected RCC bit was not on after a forced Controller Check-1. In either case, the detected error condition was not expected by the diagnostic routine.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Selection Address for Controller/Device Tested	DIAG-69
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	RCC Bits 0-7 for String 0	DIAG-70
9	RCC Bits 8-15 for String 0	DIAG-71
A	RCC Bits 17-24 for String 0	DIAG-71
B	RCC Bits 25-32 for String 0	DIAG-71
C	RCC Bits 0-7 for String 1	DIAG-70
D	RCC Bits 8-15 for String 1	DIAG-71
E	RCC Bits 17-24 for String 1	DIAG-71
F	RCC Bits 25-32 for String 1	DIAG-71

IC 1111 = Tag In Sequence Check (3880 DTI Bit 1 = 1). The storage control detected an invalid transition on DDC Tag In. Both DDC Tag In bits changed state at the same time.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Selection Address of Controller/Device Tested	DIAG-69
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	RCC Bits 0-7 for String 0	DIAG-70
9	RCC Bits 8-15 for String 0	DIAG-71
A	RCC Bits 17-24 for String 0	DIAG-71
B	RCC Bits 25-32 for String 0	DIAG-71
C	RCC Bits 0-7 for String 1	DIAG-70
D	RCC Bits 8-15 for String 1	DIAG-71
E	RCC Bits 17-24 for String 1	DIAG-71
F	RCC Bits 25-32 for String 1	DIAG-71

IC 1112 = Storage Control Check. The storage control detected a condition that indicates incorrect DDC operation other than as defined for IC 1110 or IC 1111. The specific conditions that may be detected are dependent on the type of storage control being used.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Storage Control Check Indicators	DIAG-72
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	RCC Bits 0-7 for String 0	DIAG-70
9	RCC Bits 8-15 for String 0	DIAG-71
A	RCC Bits 17-24 for String 0	DIAG-71
B	RCC Bits 25-32 for String 0	DIAG-71
C	RCC Bits 0-7 for String 1	DIAG-70
D	RCC Bits 8-15 for String 1	DIAG-71
E	RCC Bits 17-24 for String 1	DIAG-71
F	RCC Bits 25-32 for String 1	DIAG-71

IC 1113 = Timeout waiting for Tag In response. An expected DDC tag in response failed to occur and no specific error condition was indicated. The controller completely failed to respond to a DDC tag out change.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Selection Address of Controller/Device Tested	DIAG-69
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	RCC Bits 0-7 for String 0	DIAG-70
9	RCC Bits 8-15 for String 0	DIAG-71
A	RCC Bits 17-24 for String 0	DIAG-71
B	RCC Bits 25-32 for String 0	DIAG-71
C	RCC Bits 0-7 for String 1	DIAG-70
D	RCC Bits 8-15 for String 1	DIAG-71
E	RCC Bits 17-24 for String 1	DIAG-71
F	RCC Bits 25-32 for String 1	DIAG-71

IC 1114 = Expected CCA failed to occur. The diagnostic routine attempted to force a controller check-1 but no CCA occurred.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Selection Address of Controller/Device Tested	DIAG-69
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	RCC Bits 0-7 for String 0	DIAG-70
9	RCC Bits 8-15 for String 0	DIAG-71
A	RCC Bits 17-24 for String 0	DIAG-71
B	RCC Bits 25-32 for String 0	DIAG-71
C	RCC Bits 0-7 for String 1	DIAG-70

Byte	Name	Reference
D	RCC Bits 8-15 for String 1	DIAG-71
E	RCC Bits 17-24 for String 1	DIAG-71
F	RCC Bits 25-32 for String 1	DIAG-71

IC 1120 = Unexpected Controller Check-2 or Device Check-1. An end op occurred on the control interface with an end op code other than as defined for ICs 1130, 1140, or 1150. This condition was either completely unexpected or an expected error indicator was not on after a forced error. In either case, the detected error condition was not expected by the diagnostic routine.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Not Used	
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	Controller Fault Log A	SENSE-82
9	Controller Fault Log B	SENSE-83
A	Controller Fault Log C	SENSE-83
B	Controller Fault Log D	SENSE-84
C	Controller Fault Log E	SENSE-85
D	Controller Fault Log F	SENSE-85
E	Controller Sequencer Microcode Detected Check-2 Code	SENSE-87
F	Controller Fault Log G	SENSE-86

IC 1121 = Read or Write Operation Terminated by End Op Before Completion of Data Transfer. The End Op Code was as expected.

Byte	Name	Reference
1-F	The same as for IC 1120	

IC 1122 = Bus In not as expected during a DDC sequence other than as defined for IC 1132.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Incorrect Bus In Bit(s)	
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	Controller Fault Log A	SENSE-82
9	Controller Fault Log B	SENSE-83
A	Controller Fault Log C	SENSE-83
B	Controller Fault Log D	SENSE-84
C	Controller Fault Log E	SENSE-85
D	Controller Fault Log F	SENSE-85
E	Controller Sequencer Microcode Detected Check-2 Code	SENSE-87
F	Controller Fault Log G	SENSE-86

IC 1124 = Expected Controller Check-2 or Device Check-1 failed to occur. The diagnostic attempted to force a controller check-2 or a device check-1 error, but no end op response occurred on the control interface.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Not Used	
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	Controller Fault Log A	SENSE-82
9	Controller Fault Log B	SENSE-83
A	Controller Fault Log C	SENSE-83
B	Controller Fault Log D	SENSE-84
C	Controller Fault Log E	SENSE-85
D	Controller Fault Log F	SENSE-85
E	Controller Sequencer Microcode Detected Check-2 Code	SENSE-87
F	Controller Fault Log G	SENSE-86

IC 1130 = Unexpected Device Check-2. An End Op tag in occurred on the control interface. The end op code contained binary xx10xxxx. This condition was either completely unexpected or an expected error indicator was not on after a forced error. In either case, the detected error condition was not expected by the diagnostic routine.: The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Not Used	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 1131 = Unexpected Device Check-2 indicated in Device Status 1. This condition was either completely unexpected or an expected error indicator was not on after a forced error. In either case, the detected error condition was not expected by the diagnostic routine.: The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Last command executed other than a sense command	
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Incorrect Bus In Bit(s)	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 1132 = Bus In not as expected during a polling sequence or during a device sense (hex 5x) command sequence.: The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Last command executed other than a sense command	
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Incorrect Bus In Bit(s)	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 1134 = Expected Device Check-2 failed to occur. The diagnostic attempted to force a device check-2 error but no End Op tag in response occurred.*:* The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68

Byte	Name	Reference
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Not Used	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 1140 = Data Check End Op. An end op response occurred on control interface. The end op code was either hex 02, hex 03, or hex 0D. This condition should only occur during a read data transfer.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Not Used	
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8-9	Track Physical Address (PA)	DIAG-72
A-F	Not Used	

IC 1150 = Unexpected End Op Code. An end op response occurred on DDC tag in with binary xx000000 contained in the end op code on DDC bus in. Either the end op response was completely unexpected or some other end op code was expected.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Incorrect End Op Code Bit(s)	
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8-9	Track Physical Address (PA)	DIAG-72
A-F	Not Used	

IC 1160 = Physical Address (PA) miscompare. Seek error or incorrect PA bytes in home address or count field.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3-7	Not Used	
8-9	Track Physical Address (PA) Expected	DIAG-72
A-B	PA read from track	DIAG-72
C-F	Not Used	

IC 117F = String being tested is not a 3380-JK string.

Byte	Name	Reference
1-F	Not Used	

IC 8081 = DDC bus out error. An end op response occurred during execution of an Execute DDC Bus Out Diagnostic (hex 20) command.

Byte	Name	Reference
1	Test number	DIAG-68
2-3	Error bit map, hex 20 command Bit 0 = End op response to hex 80 modifier Bit 1 = End op response to hex 40 modifier Bit 2 = End op response to hex 20 modifier Bit 3 = End op response to hex 10 modifier Bit 4 = End op response to hex 08 modifier Bit 5 = End op response to hex 04 modifier Bit 6 = End op response to hex 02 modifier Bit 7 = End op response to hex 01 modifier Bit 8 = End op response to hex 00 modifier Bit 9 = End op response to hex FF modifier Bits 10-15 Not used	
4-F	Not Used	

IC 8082 = DDC wrap error. An incorrect bus in response occurred during execution of a Test DDC Byte 1 (hex 30) command.

Byte	Name	Reference
1	Test number	DIAG-68
2-3	Error bit map, hex 30 command Bit 0 = Incorrect bus in response to hex 80 modifier Bit 1 = Incorrect bus in response to hex 40 modifier Bit 2 = Incorrect bus in response to hex 20 modifier Bit 3 = Incorrect bus in response to hex 10 modifier Bit 4 = Incorrect bus in response to hex 08 modifier Bit 5 = Incorrect bus in response to hex 04 modifier Bit 6 = Incorrect bus in response to hex 02 modifier Bit 7 = Incorrect bus in response to hex 01 modifier Bit 8 = Incorrect bus in response to hex 00 modifier Bit 9 = Incorrect bus in response to hex FF modifier Bits 10-15 Not used	
4	Bus in response to hex 80 modifier (hex 30 command)	
5	Bus in response to hex 40 modifier (hex 30 command)	
6	Bus in response to hex 20 modifier (hex 30 command)	

Byte	Name	Reference
7	Bus in response to hex 10 modifier (hex 30 command)	
8	Bus in response to hex 08 modifier (hex 30 command)	
9	Bus in response to hex 04 modifier (hex 30 command)	
A	Bus in response to hex 02 modifier (hex 30 command)	
B	Bus in response to hex 01 modifier (hex 30 command)	
C	Bus in response to hex 00 modifier (hex 30 command)	
D	Bus in response to hex FF modifier (hex 30 command)	
E-F	Not used	

IC 8083 = Incorrect RCC data with no CCA active. RCC bits 0 and 32 should be off (0). RCC bits 15 and 31 should be on (1).

Byte	Name	Reference
1	Test Number	DIAG-68
2	RCC Sequence Status 01 = RCC1 sequence failed 02 = RCC2 sequence failed	
3-6	Not Used	
7	Selection Address of Controller/Device Tested	DIAG-69
8	RCC Bits 0-7 for String 0	DIAG-70
9	RCC Bits 8-15 for String 0	DIAG-71
A	RCC Bits 17-24 for String 0	DIAG-71
B	RCC Bits 25-32 for String 0	DIAG-71
C	RCC Bits 0-7 for String 1	DIAG-70
D	RCC Bits 8-15 for String 1	DIAG-71
E	RCC Bits 17-24 for String 1	DIAG-71
F	RCC Bits 25-32 for String 1	DIAG-71

IC 8086 = Force Tag Sequence Check (RCC bit 10) Failed. The connection check alert line did not activate when the diagnostic attempted to force a tag sequence check.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Selection Address for Controller/Device Tested	DIAG-69
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	RCC Bits 0-7 for String 0	DIAG-70
9	RCC Bits 8-15 for String 0	DIAG-71
A	RCC Bits 17-24 for String 0	DIAG-71
B	RCC Bits 25-32 for String 0	DIAG-71
C	RCC Bits 0-7 for String 1	DIAG-70
D	RCC Bits 8-15 for String 1	DIAG-71
E	RCC Bits 17-24 for String 1	DIAG-71
F	RCC Bits 25-32 for String 1	DIAG-71

IC 8087 = Force Connection Check Alert Attempted. A Connection Check Alert (CCA) occurred, but RCC bit 0 was off indicating that the CCA was from the other string (not the string being tested).

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Selection Address for Controller/Device Tested	DIAG-69
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	RCC Bits 0-7 for String 0	DIAG-70
9	RCC Bits 8-15 for String 0	DIAG-71
A	RCC Bits 17-24 for String 0	DIAG-71
B	RCC Bits 25-32 for String 0	DIAG-71
C	RCC Bits 0-7 for String 1	DIAG-70
D	RCC Bits 8-15 for String 1	DIAG-71
E	RCC Bits 17-24 for String 1	DIAG-71
F	RCC Bits 25-32 for String 1	DIAG-71

IC 8089 = Controller Undervoltage Detected

Byte	Name	Reference
1	Test number	
2-F	Not Used	

IC 8092 = Controller Fault Log Not As Expected.

Byte	Name	Reference
1	Test number (hex 08, 09, 0A, 0C, 0D, or 11)	
2	Incorrect controller fault log A bits	
3	Incorrect controller fault log B bits	
4	Incorrect controller fault log C bits	
5	Incorrect controller fault log D bits	
6	Incorrect controller fault log E bits	
7	Incorrect controller fault log F bits	
8	Controller Fault Log A	SENSE-82
9	Controller Fault Log B	SENSE-83
A	Controller Fault Log C	SENSE-83
B	Controller Fault Log D	SENSE-84
C	Controller Fault Log E	SENSE-85
D	Controller Fault Log F	SENSE-85
E	Incorrect controller fault log G bits	
F	Controller Fault Log G	SENSE-86

IC 8093 = ECC Data Not As Expected.

Byte	Name	Reference
1	Test number	
2	Diagnistic Read Subcommand	
3-F	Not Used	

IC 8180 = Port Select Error.

Byte	Name	Reference
1	Test number	
2	Controller Fault Log D (Port 0 or 4)	SENSE-84
3	Response to hex 00 wrap data (Port 0 or 4)	
4	Response to hex FF wrap data (Port 0 or 4)	
5	Controller Fault Log D (Port 1 or 5)	SENSE-84
6	Response to hex 00 wrap data (Port 1 or 5)	
7	Response to hex FF wrap data (Port 1 or 5)	
8	Controller Fault Log D (Port 2 or 6)	SENSE-84
9	Response to hex 00 wrap data (Port 2 or 6)	
A	Response to hex FF wrap data (Port 2 or 6)	
B	Controller Fault Log D (Port 3 or 7)	SENSE-84
C	Response to hex 00 wrap data (Port 3 or 7)	
D	Response to hex FF wrap data (Port 3 or 7)	
E	Controller Fault Log G (first failing port)	SENSE-85
F	Bit Significant Error Flags. Bit 0 = Port 0 failed, Bit 1 = Port 1..., etc.	

IC 8181 = Port Wrap Error.

Byte	Name	Reference
1	Test number	
2	Controller Fault Log D (Port 0 or 4)	SENSE-84
3	Response to hex 00 wrap data (Port 0 or 4)	
4	Response to hex FF wrap data (Port 0 or 4)	
5	Controller Fault Log D (Port 1 or 5)	SENSE-84
6	Response to hex 00 wrap data (Port 1 or 5)	
7	Response to hex FF wrap data (Port 1 or 5)	
8	Controller Fault Log D (Port 2 or 6)	SENSE-84
9	Response to hex 00 wrap data (Port 2 or 6)	
A	Response to hex FF wrap data (Port 2 or 6)	
B	Controller Fault Log D (Port 3 or 7)	SENSE-84
C	Response to hex 00 wrap data (Port 3 or 7)	
D	Response to hex FF wrap data (Port 3 or 7)	
E	Controller Fault Log G (first failing port)	SENSE-85
F	Bit Significant Error Flags. Bit 0 = Port 0 failed, Bit 1 = Port 1..., etc.	

IC 8182 = Device check on in Controller Fault Log D after Diagnostic Read Controller Fault Log D command.

Byte	Name	Reference
1	Test Number	DIAG-68
2-7	Not Used	
8	Controller Fault Log A	SENSE-82
9	Controller Fault Log B	SENSE-83
A	Controller Fault Log C	SENSE-83
B	Controller Fault Log D	SENSE-84
C	Controller Fault Log E	SENSE-85
D	Controller Fault Log F	SENSE-85
E	Not Used	
F	Controller Fault Log G	SENSE-85

IC 8183 = Unexpected controller check-2 or device check-1 on first attempt at device selection.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Not used	
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	Controller Fault Log A	SENSE-82
9	Controller Fault Log B	SENSE-83
A	Controller Fault Log C	SENSE-83
B	Controller Fault Log D	SENSE-84
C	Controller Fault Log E	SENSE-85
D	Controller Fault Log F	SENSE-85
E	Controller sequencer microcode detected check-2 code	SENSE-87
F	Controller Fault Log G	SENSE-85

IC 8184 = Device Power Status Incorrect.

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Device Power Status from device being tested	SENSE-63
7	Device Power Status from other device in the drive	
8	Checkpoint Log from device being tested	SENSE-66
9	Checkpoint Log from other device in the drive	
A	Device Check-2 Status from device being tested	SENSE-63
B	Device Check-2 Status from other device in the drive	
C-F	Not Used	

IC 8185 = Device Check-1 During Port Select

Byte	Name	Reference
1	Test Number	DIAG-68
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Bit Significant Error Flag (bit 0 = port 0 failed, bit 1 = port 1 failed, etc.)	
7	Tag Out (DTO) and Tag In Decoded (DTI)	DIAG-69
8	Controller Fault Log A	SENSE-82
9	Controller Fault Log B	SENSE-83
A	Controller Fault Log C	SENSE-83
B	Controller Fault Log D	SENSE-84
C	Controller Fault Log E	SENSE-85
D	Controller Fault Log F	SENSE-85
E	Controller Sequencer Microcode Detected Check-2 Code	SENSE-87
F	Controller Fault Log G	SENSE-86

IC 8189 = Device Undervoltage Detected

Byte	Name	Reference
1	Test number	
2-F	Not Used	

IC 8192 = Unable to force PLO No Drive check (Fault Log A, bit 5)

Byte	Name	Reference
1	Test number	
2-7	Not Used	
8	Controller Fault Log A	SENSE-82
9	Controller Fault Log B	SENSE-83
A	Controller Fault Log C	SENSE-83
B	Controller Fault Log D	SENSE-84
C	Controller Fault Log E	SENSE-85
D	Controller Fault Log F	SENSE-85
E	Incorrect controller fault log G bits	
F	Controller Fault Log G	SENSE-86

IC 8199 = Failed to force Read/Write Check

Byte	Name	Reference
1	Test Number	DIAG-68
2-6	Not Used	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1	SENSE-88
B	Read/Write Status 2	SENSE-89
C	Read/Write Status 3	SENSE-90
D	Read/Write Status 4	SENSE-90
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 8292 = Sector times too short. The sector interrupt time was less than the minimum time allowed.

Byte	Name	Reference
1	Test Number	DIAG-68
2-F	Not Used	

IC 8381 = One or more data checks occurred during the execution of routine 83. Error bytes 2 through B contain bit significant head maps for the CE and diagnostic cylinders showing the heads that were in use at the time of failure. The first 15 bits in each head map are numbered 0 through E, left to right, and correspond to heads 0 through E. The rightmost bit is not used. A bit being on (1) indicates that a data check occurred while reading using that head.

Byte	Name	Reference
1	Test number	
2-3	Bit significant head map for the CE cylinder	
4-5	Bit significant head map for the first diagnostic cylinder	
6-7	Bit significant head map for the second diagnostic cylinder	
8-9	Bit significant head map for the third diagnostic cylinder	

Byte	Name	Reference
A-B	Bit significant head map for the fourth diagnostic cylinder	
C-D	Total number of data checks	
E	Model designation. Hex 1D for 3380-J. Hex 1F for 3380-K.	
F	Not Used	

IC 8AB0 = Invalid parameter entry. See the routine 8A description for additional information.

Byte	Name	Reference
1-F	Parameter entries 1 through 15	

IC 8AB2 = A seek operation ended with 'seek incomplete' status and the checkpoint log contained a value other than hex 58.: The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1	Test Number	DIAG-68
2-6	Not used	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 8AB3 = An unexpected checkpoint log value was obtained following a seek operation.: The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1	Test Number	DIAG-68
2-6	Not used	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 8AFF = Normal end of routine 8A. After each seek performed by routine 8A the device checkpoint log is sensed. The checkpoint value obtained indicates the settling time required at the end of the access motion. These checkpoint values range from hex 54 to 58 with the lowest value indicating the best machine performance. Thus, the counter values provided in the error message bytes provide an indication of access performance.

Byte	Name	Reference
1	Not used	
2-3	Number of seeks that ended with checkpoint 54	
4-5	Number of seeks that ended with checkpoint 55	
6-7	Number of seeks that ended with checkpoint 56	
8-9	Number of seeks that ended with checkpoint 57	
A-B	Number of seeks that ended with checkpoint 58 and 'seek complete' status	
C-D	Number of seeks that ended with checkpoint 58 and 'seek incomplete' status	
E-F	Total number of seeks performed	

IC 90F0 = The master controller lost contact with the slave during execution of routine 90. This usually indicates that routine 90 was stopped on the slave side by a storage control error or by system activity. The condition may have been caused by a system reset on the slave side or by extremely heavy system activity. This condition rarely indicates an 3380-JK failure.

Byte	Name	Reference
1-F	Not Used	

IC 9180 = Data Check Detected During Home Address Scan

Byte	Name	Reference
1	Command Code	DIAG-68
2	End Op Code	
3-4	Track Physical Address	DIAG-72
5	Number of data checks on this track	
6-F	Not Used	

IC 91F0 = Invalid Parameter Entry. See the routine 91 description.

Byte	Name	Reference
1-F	Not Used	

IC 93XX = Stop during routine 93. See MAP-001, entry D in the MIM.

IC 9699 = Normal end of routine 96. Error bytes 1 through F contain string configuration and device status information.

Byte	Name
1	Substring ID (0 or 1)
2-5	Not Used
6-7	Device type indicators. The four hex digits, left to right, indicate the device type for boxes 1 to 4 as follows: D = 3380-J.

Byte	Name
	F = 3380-K. 0 = Box not installed or unable to determine type
8-F	Device status indicators. The 16 hex digits, left to right, indicate the status of devices 0 to F as follows: 0 = All tests successful. Device is operational. 1 = Unable to select (device is busy). 2 = Equipment check. 3 = Data check. 4 = Intervention required. 5 = "Servo Busy" condition. F = Box not installed **Note:** *Status codes 0, 1 and 5 indicate that the device is probably usable. Codes 2 through 4 indicate that the device is probably not usable.*

IC 9790 = Controller Check-1 Status. Normal end of routine 97.

Byte	Name	Reference
1-7	Not Used	
8	RCC Bits 0-7 for String 0	DIAG-70
9	RCC Bits 8-15 for String 0	DIAG-71
A	RCC Bits 17-24 for String 0	DIAG-71
B	RCC Bits 25-32 for String 0	DIAG-71
C	RCC Bits 0-7 for String 1	DIAG-70
D	RCC Bits 8-15 for String 1	DIAG-71
E	RCC Bits 17-24 for String 1	DIAG-71
F	RCC Bits 25-32 for String 1	DIAG-71

IC 97A0 = Controller Check-2 and Device Check-1 Status. Normal end of routine 97.

Byte	Name	Reference
1-7	Not Used	
8	Controller Fault Log A	SENSE-82
9	Controller Fault Log B	SENSE-83
A	Controller Fault Log C	SENSE-83
B	Controller Fault Log D	SENSE-84
C	Controller Fault Log E	SENSE-85
D	Controller Fault Log F	SENSE-85
E	Controller Sequencer Microcode Detected Check-2 Code	SENSE-87
F	Controller Fault Log G	SENSE-86

IC 97B0 = Device Status. Normal end of routine 97.*:* The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1-6	Not Used	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64

Byte	Name	Reference
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 98F1 = Error log entry found. The error bytes contain sense bytes 0 through 11 from the error log. Restart the routine to get sense bytes 12 through 23 (see IC 98F2).

Byte	Name	Reference
1	Error record number (hex 01-20)	
2	Sense byte 0	
3	Sense byte 1	
4	Sense byte 2	
5	Sense byte 3	
6	Sense byte 4	
7	Sense byte 5	
8	Sense byte 6	
9	Sense byte 7	
A	Sense byte 8	
B	Sense byte 9	
C	Sense byte 10	
D	Sense byte 11	
E	Not Used	
F	Not Used	

IC 98F2 = Error log entry found. The error bytes contain sense bytes 12 through 23 from the error log. Restart the routine to continue the error log search.

Byte	Name	Reference
1	Counter (number of times this error occurred)	
2	Sense byte 12	
3	Sense byte 13	
4	Sense byte 14	
5	Sense byte 15	
6	Sense byte 16	
7	Sense byte 17	
8	Sense byte 18	
9	Sense byte 19	
A	Sense byte 20	
B	Sense byte 21	
C	Sense byte 22	
D	Sense byte 23	
E-F	Time Stamp - .1 hours/increment (not used if attached to 3880 control unit)	

IC 98FF = The contents of the device error log area in the storage control are invalid. Use main option E, Error Log Reset, to reset the error log. Resetting the error log restores the error logging function.

Byte	Name	Reference
1-F	Not Used	

IC 9980 = The left device was not disabled. Possible incorrect routine operating procedure.

Byte	Name	Reference
1	Test Number	DIAG-58
2-F	Not Used	

IC 9981 = The right device was not disabled. Possible incorrect routine operating procedure.

Byte	Name	Reference
1	Test Number	DIAG-58
2-F	Not Used	

IC 9982 = The left device was not enabled. Possible incorrect routine operating procedure.

Byte	Name	Reference
1	Test Number	DIAG-58
2-F	Not Used	

IC 9983 = The right device was not enabled. Possible incorrect routine operating procedure.

Byte	Name	Reference
1	Test Number	DIAG-58
2-F	Not Used	

IC 9984 = Unexpected device check-2 on the left device.: The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1	Test Number	DIAG-58
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Not Used	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 9985 = Unexpected device check-2 on the right device.: The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1	Test Number	DIAG-58
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Not Used	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 9986 = Unexpected device check-2 on the left device.

Byte	Name	Reference
1	Test Number	DIAG-58
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Device Power Status (left device)	SENSE-63
7	Device Power Status (right device)	SENSE-63
8	Checkpoint Log (left device)	SENSE-66
9	Checkpoint Log (right device)	SENSE-66
A	Device Check-2 Status (left device)	SENSE-63
B	Device Check-2 Status (right device)	SENSE-63
C-F	Not Used	

IC 9987 = Unexpected device check-2 on the right device.

Byte	Name	Reference
1	Test Number	DIAG-58
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Device Power Status (left device)	SENSE-63
7	Device Power Status (right device)	SENSE-63
8	Checkpoint Log (left device)	SENSE-66
9	Checkpoint Log (right device)	SENSE-66
A	Device Check-2 Status (left device)	SENSE-63
B	Device Check-2 Status (right device)	SENSE-63
C-F	Not Used	

IC 9988 = Timeout waiting for busy bit (in device status 1) to go inactive following motor start.: The meanings of bytes A through D depend on the status of bit 5 in byte E (device check-2 status) for this isolation code.

Byte	Name	Reference
1	Test Number	DIAG-58
2	Command Code	DIAG-68
3	Modifier Count	DIAG-68
4	Bus Out (DBO)	DIAG-68
5	Bus In (DBI)	DIAG-68
6	Not Used	
7	Device Power Status	SENSE-63
8	Device Status 1	SENSE-74
9	Device Status 2	SENSE-75
A	Read/Write Status 1 (if byte E = hex 04)	SENSE-88
A	Servo Status 0, bits 0-7 (if byte E not = hex 04)	SENSE-64
B	Read/Write Status 2 (if byte E = hex 04)	SENSE-89
B	Servo Status 0, bits 8-15 (if byte E not = hex 04)	SENSE-64
C	Read/Write Status 3 (if byte E = hex 04)	SENSE-90
C	Servo Status 2, bits 0-7 (if byte E not = hex 04)	SENSE-9
D	Read/Write Status 4 (if byte E = hex 04)	SENSE-90
D	Servo Status 2, bits 8-15 (if byte E not = hex 04)	SENSE-9
E	Device Check-2 Status	SENSE-63
F	Checkpoint Log	SENSE-66

IC 9989 = Either one or both devices failed to become ready after 3 minutes.

Byte	Name	Reference
1	Test Number	DIAG-58
2-F	Not Used	

IC 9991 = Normal end of test 1. See routine 99 description.

Byte	Name	Reference
1	Test Number	DIAG-58
2-F	Not Used	

IC 9992 = Normal end of test 2. See routine 99 description.

Byte	Name	Reference
1	Test Number	DIAG-58
2-F	Not Used	

IC 9993 = Normal end of test 3. See routine 99 description.

Byte	Name	Reference
1	Test Number	DIAG-58
2-F	Not Used	

IC 9994 = Normal end of test 4. See routine 99 description.

Byte	Name	Reference
1	Test Number	DIAG-58
2-F	Not Used	

IC 9CFF = Normal End of Routine 9C

Byte	Name	Reference
1	Not Used	
2-F	The 14 skip control bytes written in the home address.	

IC 9C80 = Either invalid parameters were entered when running routine 9C or no parameters were entered at all. See the routine 9C description.

Byte	Name	Reference
1-F	Not Used	

IC 9DA0 = DPS array data display. Bytes 8 through F contain 8 bytes read from the the DPS array starting at that address shown in bytes 2 and 3. Continue routine execution (by pressing the Enter key on the MD) to read the next 8 bytes from the array. The routine ends after the last array bytes have been displayed.

Byte	Name	Reference
1	Test Number	DIAG-68
2-3	DPS Array Address	DIAG-63
4-7	Not Used	
8-F	DPS Array Data	

IC 9DF0 = Unable to dump the DPS array to the trace area because a trace is in progress. Either use appropriate storage control facilities to stop the trace or use Routine 98 to reset and restart the error logging function. (Starting error logging stops the trace function.) Then use Routine 9D to dump the DPS array.

Byte	Name	Reference
1-F	Not Used	

IC 9E80 = Invalid Parameters specified for the diagnostic microcode patch routine. The error bytes show what was entered for the parameters.

Byte	Name	Reference
1	Parameter 1	
2	Parameter 2	
3	Parameter 3	
4	Parameter 4	
5	Parameter 5	
6	Parameter 6	
7	Parameter 7	
8	Parameter 8	
9	Parameter 9	
A	Parameter 10	
B	Parameter 11	
C	Parameter 12	
D	Parameter 13	
E	Parameter 14	
F	Parameter 15	

IC 9FFF = Normal ending condition for Routine 9F (Set/Reset CE Mode).

Byte	Name
1-4	Bit positions 00 to 1F (left to right) represent device addresses 00 to 1F. A bit being on (1) indicates that the corresponding device is in CE mode. For example, if error message bytes 1 through 4 contain 02800184, then devices 06, 08, 17, and 1D are in CE mode.
5	Bit positions 0 and 1 (left to right) represent 3380-JK strings 0 and 1. A bit being on (1) indicates that the corresponding string is write inhibited. Bit positions 2 through 5 are not used. Bit 6 On indicates that the reset fence function is available and Bit 7 On indicates that the reset write inhibit function is available.
6	Bit positions 0 to 7 (left to right) represent storage control channel interfaces A through H. A bit being on (1) indicates that the corresponding channel interface is write inhibited.
7	Not Used
8-B	Bit positions 00 to 1F (left to right) represent device addresses 00 to 1F. A bit being on (1) indicates that the corresponding device is fenced.
C	Bit position 0 On (1) indicates that the entire storage path is fenced.
D	Bit positions 0 to 7 (left to right) represent storage control channel interfaces A through H. A bit being On indicates that the corresponding channel interface is fenced.
E	The information contained in bytes 1 through 13 is not valid for all types of control units. Byte 14, bits 0 through 7 indicate which fields contain valid information as follows: Bit 0 - Bytes 1 through 4 are valid Bit 1 - Byte 5 is valid Bit 2 - Byte 6 is valid Bit 3 - Not used Bit 4 - Bytes 8 through 11 are valid Bit 5 - Byte 12 is valid Bit 6 - Byte 13 is valid Bit 7 - Not used
F	Not used

IC D3XX = Stop during routine D3. See MAP-001, entry AK in the MIM.

CTL-I Test IC Descriptions

The following CTL-I Test IC descriptions are listed in numerical sequence. Additional error message bytes are numbered 1 through F and are listed following each IC description.

FF82 = CTL-I wrap error. An incorrect bus in response to a command modifier occurred during execution of a CTL-I wrap test command (command code hex 30).

Byte	Name	Reference
1	Test Number	
2-3	Error bit map, hex 30 command	
	Bit 0 = Incorrect bus in response to hex 80 modifier	
	Bit 1 = Incorrect bus in response to hex 40 modifier	
	Bit 2 = Incorrect bus in response to hex 20 modifier	
	Bit 3 = Incorrect bus in response to hex 10 modifier	
	Bit 4 = Incorrect bus in response to hex 08 modifier	
	Bit 5 = Incorrect bus in response to hex 04 modifier	
	Bit 6 = Incorrect bus in response to hex 02 modifier	
	Bit 7 = Incorrect bus in response to hex 01 modifier	
	Bit 8 = Incorrect bus in response to hex 00 modifier	
	Bit 9 = Incorrect bus in response to hex FF modifier	
4	Bus in response to hex 80 modifier (hex 30 command)	
5	Bus in response to hex 40 modifier (hex 30 command)	
6	Bus in response to hex 20 modifier (hex 30 command)	
7	Bus in response to hex 10 modifier (hex 30 command)	
8	Bus in response to hex 08 modifier (hex 30 command)	
9	Bus in response to hex 04 modifier (hex 30 command)	
A	Bus in response to hex 02 modifier (hex 30 command)	
B	Bus in response to hex 01 modifier (hex 30 command)	
C	Bus in response to hex 01 modifier (hex 30 command)	
D	Bus in response to hex 00 modifier (hex 30 command)	
E-F	Not used	

FF88 = CCA, tag in, or bus in line active after an RCC sequence.

Byte	Name	Reference
1	Test Number	
2-3	Not Used	
4	Bus In	
5	Tag Out (DTO) and Tag In Decoded (DTI)	
6	RCC Bits 0-7 for string 0	
7	RCC Bits 8-15 for string 0	
8	RCC Bits 17-24 for string 0	
9	RCC Bits 25-32 for string 0	
A	RCC Bits 0-7 for string 1	
B	RCC Bits 8-15 for string 1	
C	RCC Bits 17-24 for string 1	
D	RCC Bits 25-32 for string 1	
E-F	Not Used	

FF89 = RCC sequence failed, stop bits (31-32) incorrect

Byte	Name	Reference
1	Test Number	
2-3	Not Used	
4	Bus In	
5	Tag Out (DTO) and Tag In Decoded (DTI)	
6	RCC Bits 0-7 for string 0	
7	RCC Bits 8-15 for string 0	
8	RCC Bits 17-24 for string 0	
9	RCC Bits 25-32 for string 0	
A	RCC Bits 0-7 for string 1	
B	RCC Bits 8-15 for string 1	
C	RCC Bits 17-24 for string 1	
D	RCC Bits 25-32 for string 1	
E-F	Not Used	

FF8A = RCC sequence failed to fence controller

Byte	Name	Reference
1	Test Number	
2-3	Not Used	
4	Bus In	
5	Tag Out (DTO) and Tag In Decoded (DTI)	
6	RCC Bits 0-7 for string 0	
7	RCC Bits 8-15 for string 0	
8	RCC Bits 17-24 for string 0	
9	RCC Bits 25-32 for string 0	
A	RCC Bits 0-7 for string 1	
B	RCC Bits 8-15 for string 1	
C	RCC Bits 17-24 for string 1	
D	RCC Bits 25-32 for string 1	
E-F	Not Used	

FF8B = CCA, tag in, or bus in line active after a partition on (hang reset) sequence.

Byte	Name	Reference
1	Test Number	
2-3	Not Used	
4	Bus In	
5	Tag Out (DTO) and Tag In Decoded (DTI)	
6	RCC Bits 0-7 for string 0	
7	RCC Bits 8-15 for string 0	
8	RCC Bits 17-24 for string 0	
9	RCC Bits 25-32 for string 0	
A	RCC Bits 0-7 for string 1	
B	RCC Bits 8-15 for string 1	
C	RCC Bits 17-24 for string 1	
D	RCC Bits 25-32 for string 1	

Byte	Name	Reference
E-F	Not Used	

FF8C = Bus out test (test 4) failed. One or more bus out lines is inoperative.

Byte	Name	Reference
1	Test Number	
2	Bit map indicating failing bus out lines.	
3-F	Not Used	

FF90 = Unexpected Controller Check-1. An unexpected Connection Check Alert (CCA) occurred.

Byte	Name	Reference
1	Test Number	
2	Command Code	
3	Modifier Count	
4	Selection Address for controller under test	
5	Tag Out (DTO) and Tag In Decoded (DTI)	
6	RCC Bits 0-7 for string 0	
7	RCC Bits 8-15 for string 0	
8	RCC Bits 17-24 for string 0	
9	RCC Bits 25-32 for string 0	
A	RCC Bits 0-7 for string 1	
B	RCC Bits 8-15 for string 1	
C	RCC Bits 17-24 for string 1	
D	RCC Bits 25-32 for string 1	
E-F	Not Used	

FF91 = Tag In Sequence Check. The storage control detected an invalid transition on CTL-I Tag In. Both CTL-I Tag In bits changed state at the same time.

Byte	Name	Reference
1	Test Number	
2	Command Code	
3	Modifier Count	
4	Selection Address for controller under test	
5	Tag Out (DTO) and Tag In Decoded (DTI)	
6	RCC Bits 0-7 for string 0	
7	RCC Bits 8-15 for string 0	
8	RCC Bits 17-24 for string 0	
9	RCC Bits 25-32 for string 0	
A	RCC Bits 0-7 for string 1	
B	RCC Bits 8-15 for string 1	
C	RCC Bits 17-24 for string 1	
D	RCC Bits 25-32 for string 1	
E-F	Not Used	

FF92 = Storage Control Check. The storage control detected a condition that indicates incorrect CTL-I operation other than as defined for FF90 or FF91.

Byte	Name	Reference
1	Test Number	
2	Command Code	
3	Modifier Count	
4	Bit 2 = Bus in parity check Bit 5 = Sync in check	
5	Tag Out (DTO) and Tag In Decoded (DTI)	
6	RCC Bits 0-7 for string 0	
7	RCC Bits 8-15 for string 0	
8	RCC Bits 17-24 for string 0	
9	RCC Bits 25-32 for string 0	
A	RCC Bits 0-7 for string 1	
B	RCC Bits 8-15 for string 1	
C	RCC Bits 17-24 for string 1	
D	RCC Bits 25-32 for string 1	
E-F	Not Used	

FF93 = Timeout waiting for Tag In response. An expected CTL-I Tag In response failed to occur and no specific error condition was indicated. The controller completely failed to respond to a CTL-I Tag Out change.

Byte	Name	Reference
1	Test Number	
2	Command Code	
3	Modifier Count	
4	Selection Address for controller under test	
5	Tag Out (DTO) and Tag In Decoded (DTI)	
6	RCC Bits 0-7 for string 0	
7	RCC Bits 8-15 for string 0	
8	RCC Bits 17-24 for string 0	
9	RCC Bits 25-32 for string 0	
A	RCC Bits 0-7 for string 1	
B	RCC Bits 8-15 for string 1	
C	RCC Bits 17-24 for string 1	
D	RCC Bits 25-32 for string 1	
E-F	Not Used	

FF94 = Expected CCA failed to occur. The diagnostic attempted to force a Controller Check-1 but no CCA occurred.

Byte	Name	Reference
1	Test Number	
2	Command Code	
3	Modifier Count	
4	Selection Address for controller under test	
5	Tag Out (DTO) and Tag In Decoded (DTI)	

Byte	Name	Reference
6	RCC Bits 0-7 for string 0	
7	RCC Bits 8-15 for string 0	
8	RCC Bits 17-24 for string 0	
9	RCC Bits 25-32 for string 0	
A	RCC Bits 0-7 for string 1	
B	RCC Bits 8-15 for string 1	
C	RCC Bits 17-24 for string 1	
D	RCC Bits 25-32 for string 1	
E-F	Not Used	

FFA0 = Unexpected Controller Check-2. An unexpected End Op response occurred on CTL-I Tag In.

Byte	Name	Reference
1	Test Number	
2	Command Code	
3	Modifier Count	
4	Bus In (End Op Code)	
5	Tag Out (DTO) and Tag In Decoded (DTI)	
6	Fault Log A	
7	Fault Log B	
8	Fault Log C	
9	Fault Log D	
A	Fault Log E	
B	Fault Log F	
C	Controller Sequencer Microcode Detected Check-2 Code	
D-F	Not Used	

Routine 80 - Controller Tests

Routine 80 tests controller functions only. It does not perform device selection and does not require that any device be in CE mode. Routine 80 includes tests of controller error checking functions as well as checks for normal controller operation. A partial test for normal DPS operation is also included.

Routine 80 contains 17 tests (numbered 01 to 11 hex) which are normally run in sequence. A parameter entry provides for user selection of a specific test to be looped. The number of the failing test appears in the first error byte of any isolation code generated by this routine.

Note: *The test number for test 08 may appear in error messages as any hex value from 08 to 38. Refer to the description of test 08.*

Parameters

Two parameter entries are applicable to this routine as follows:

Parameter 0 is the run control parameter, which is described on DIAG-3. Any valid run control value can be used with this routine.

Parameter 1 specifies a test to be looped. If this parameter contains a valid test number (hex 01 to 11), then the indicated test loops indefinitely after all preceding tests have been successfully run. If this parameter does not contain a valid test number, then each test runs only once. The default value for this parameter is 00 (run all tests).

Tests

The following tests are contained in routine 80:

Test 01 - DDC Bus Out Test

Test 01 uses command code hex 20 (DDC Bus Out Test) to check DDC bus out.

Test 02 - DDC Wrap Test

Test 02 uses command code hex 30 (DDC Wrap Test) to wrap DDC bus out to bus in. The command is repeated 10 times using 10 different command modifiers. The command modifiers used are hex 00, 80, 40, 20, 10, 08, 04, 02, 01, and FF.

Test 03 - Controller Sequencer Tests

Test 03 uses command code hex 31 (Diagnostic Command) to test controller functions. The diagnostic command modifiers (subcommands) used are:

C0 (Reset Serdes/ECC Hardware),
E0 (Controller Reg 13 Status Test), and
E1 (Counter and Controller Exercise)

Test 04 - Force Controller Check-1 Errors

Test 04 checks RCC1 and RCC2 sequence functions then uses command code hex 31 (Diagnostic Command) to force controller check-1 conditions.

Test 05 - Force Tag Sequence Check (RCC bit 10)

This test forces a tag sequence check three times by causing the following invalid DDC tag out transitions:

1. Null Disconnect to Selected Null
2. Selected Null to Null Disconnect
3. RCC1 to Selected Null

Test 06 - Write Data Transfer Test

This test uses command code hex 31 (Diagnostic Command) with command modifier (subcommand) hex C1 to place the controller in an extended read/write mode. The extended diagnostic subcommand A2 (write data) is then used to start a write data transfer from the storage control to the controller. No device is selected, so the data is not actually written to any device. The write data transfer consists of 4096 2-byte wide data transfers (8192 bytes total).

Test 07 - Write Data Transfer With Incorrect Bus Out Parity

Test 07 performs the same functions as test 08 except that write data is placed on DDC bus out with incorrect parity. This should cause a controller check-2 condition (end op code = 10 hex) with a 'DXB Bus Out Parity Check' (bit 0) indicated in fault log byte F.

Test 08 - Write Data, Read ECC

Test 08 uses diagnostic commands to simulate a write operation and read the controller generated ECC bytes. This checks ECC byte generation.

Test 09 - Force Data Check

Test 09 uses diagnostic commands to simulate a read operation with an error in the data read. This should cause a data check.

Test 0A - ECC Tests

Test 0A uses diagnostic commands to simulate several read operations using different lengths and with several different types of errors in the data and ECC bytes. This tests the ability of the controller to correctly detect data errors.

Test 0B - Force Controller Check-2 Errors (Fault Log F)

Test 0B uses diagnostic commands to test Fault Log F, bits 0, 1, and 2.

Test 0C - Force Controller Check-2 Errors (Fault Log B)

Test 0B uses diagnostic commands to test Fault Log B, bits 0, 1, and 2.

Test 0D - Force PLO No Drive Check

Test 0D uses command code hex 31 (Diagnostic Command) with modifier C2 Hex to force a PLO No Drive Check (Fault Log A Bit 1). controller check-2 conditions.

Test 0E - DPS Preliminary Checkout.

This test performs a partial test of the ability to sense both the primary and alternate DPS status and to set and reset DPS locks.

Test 0F - DPS Diagnostic Array Test.

This test checks the ability to read and write in the diagnostic communication area in the DPS array using the read/write array DPS commands.

Test 10 - DPS Set/Reset Under Mask Test.

This test checks the ability to read and write in the diagnostic communication area in the DPS array using the set/reset under mask DPS commands.

Test 11 - DPS Checker Test.

This test uses the DPS set locks command to force a controller check-2 with all DPS error indicators (bits 0-6) on in fault log E.

Routine 81 - Device Logic Tests

Routine 81 tests controller and device logic for device selection. It tests device and controller error checking on the CDP interface.

Routine 81 contains 9 tests that run in sequence.

Parameters

Routine 81 uses two parameters. The first parameter is the run control parameter, which is described on DIAG-3. The second parameter identifies a test to be looped.

If the second parameter is a test number (hex 01 through hex 09), the specified test is looped after all the lower numbered tests have been run. If the parameter is hex 00 (default) or any value other than a test number, all tests are run in numerical sequence and the routine ends after the last test.

Test Descriptions

The tests in routine 81 are described in the following paragraphs.

Test 01 - Port Selection and CDP Wrap Test

This test selects a port without selecting a device. It verifies that the correct port is selected and that no checks are set. CDP wrap tests are then performed to verify the CDP bidirectional data bus. The two data patterns used are hex 00 and hex FF. Four passes through the test (or eight if 4-path) are needed to test all CDP ports. The fault log bytes and other status are saved and included in the error bytes.

Test 02 - Device Selection Test

Test 02 performs and verifies device selection, and then forces device check 1 errors.

Test 03 - Sense Power Status Test

Test 03 checks the status of the drive motor and tests the Sense Device Checks command.

Test 04 - Register Checkers Test

Test 04 causes parity checks on the target register and the head address register to verify checker operation. Then, the test resets the checks to verify checker reset operation.

Test 05 - CDP Register Wrap Test

Test 05 checks the CDP bus moving data in both directions. Checkers tested by this test are:

- CDP register check
- CDP/DPS bus parity check
- Checkpoint check

Test 06 - Force Multi-Select Check

Test 06 uses command code Hex 31 with subcommand Hex C3 to force a multi-select check (Fault Log A, Bit 5).

Test 07 - Target Register Test

This test loads the target register with various patterns and checks for errors in that function. Errors associated with the target register cause an RPS check. Test 04 was able to set the RPS check indicator.

Test 08 - Head Address Register (HAR) Test

Test 08 checks the head address register by loading it with various patterns. The CDP is set to split-bus mode to enable the HAR checker. Errors in the head address register are indicated by a HAR parity check, which was verified to be settable by test 04.

Test 09 - Device Status Test

Test 09 verifies correct device status before linking to tests that need correct status reporting for operation. The device undervoltage indicator is also checked.

Routine 82 - Servo Tests

Routine 82 tests servomechanism functions. It performs device selection and requires that the device be in CE mode.

Routine 82 contains four tests (01 through 05), which are normally run in sequence. The number of the failing test appears in the first error byte for the isolation codes generated by this routine.

Parameters

Routine 82 uses two parameters. The first parameter is the run control parameter, which is described on DIAG-3. The second parameter identifies a test to be looped.

If the second parameter is a test number (hex 01 through hex 04), the specified test is looped after all the lower numbered tests have been run. If the parameter is hex 00 (default) or any value other than a test number, all tests are run in numerical sequence and the routine ends after the last test.

Test Descriptions

The five tests in routine 82 are described in the following paragraphs.

Test 01 - Multiple Cylinder Seek

This test performs a rezero operation followed by a series of seek operations.

Test 02 - Offset Verification

This test performs a rezero operation followed by a series of offset operations to verify that offset status is correctly set and sensed.

Test 03 - Set Sector and Generate Interrupt

This test performs valid and invalid sector search operations to test the sector search function and the associated error detectors and status indicators.

Test 04 - Force HDA Attention

This test uses a special diagnostic command to rezero the actuator and force an HDA attention interrupt.

Test 05 - Lock PLO To Servo

This test locks the DHPLO to the 'servo PLO clock' signal from the selected device.

Routine 83 - Read/Write Data Transfer Tests

This routine contains three tests:

- Test 01 reads the home addresses on all the CE and diagnostic cylinders, re-writes those home addresses that are found to be off track center, and checks the data check rate in the home address areas.
- Test 02 writes a full track of data (several records) on each of the CE and diagnostic tracks, reads each track several times after each write, and checks the data check rate for each track.
- Test 03 performs the same functions as test 02 except that the total data check rate, across all tracks, is measured.

If an acceptable data check rate is exceeded in any test, IC 8381 is used to report the tracks on which data checks occurred that contributed to the failure. See the description of IC 8381 for additional information.

Parameters

Six parameters are used with routine 83.

Parameter 0 is the run control parameter, which is described on DIAG-3. Any run control functions can be used with routine 83. If routine linking is allowed, routine 83 links to routine 84.

Parameter 1 specifies the number of times each track is to be written. The default value for the parameter is 03.

Parameter 2 specifies the number of times each track is to be read after each write. The default value for this parameter is 03.

Parameter 3 specifies the number of data checks to be allowed per track in test 2. The default value for this parameter is 0A.

Parameter 4 specifies the total number of data checks to be allowed in test 3. The default value for this parameter is 14 hex for a 3380-J or 28 hex for a 3380-K.

Parameter 5 specifies the length of each record, in cells, to be written in tests 2 and 3. The default value for this parameter is 1F hex.

Routine 84 - Read/Write Function Tests

Routine 84 tests device read functions, write functions, clocking functions, erase functions, padding and error checking functions. It contains 10 tests (numbered 01 to 0A hex), which are normally run in sequence.

The number of the failing test appears in the first error message byte of any error message generated by routine 84.

Parameters

Only the run control parameter is applicable to routine 84.

Parameter 0 is the run control parameter. All of the normal run control functions are applicable to this routine. The run control parameter values are described on DIAG-3. If routine linking is specified, routine 84 links to routine 85.

Test Descriptions

The following tests are contained in routine 84:

Test 01 - Seek To CE Cylinder

This test seeks to the CE cylinder (hex 376 for 3380-J, and hex A62 for 3380-K.)

Test 02 - Format Track

This test reads home address then writes a standard record 0 followed by two eight byte records (records 1 and 2). This is the track format required by subsequent tests in this routine. After record 2 has been written, drive padding to index is checked.

Test 03 - Clock Command Test

This test reads home address, clocks over records 0 and 1, then reads the record 2 count field to verify that track orientation was retained during the clocking operation.

Test 04 - Address Mark Search Test

This test reads home address then performs an address mark search and reads the count field found. Failure to detect an address mark is an error.

Test 05 - Erase Commands Test

This test reads home address and record 0, uses the erase commands to erase record 1 count and data fields, and then uses drive padding to erase record 2. The home address is read again and an address mark search is performed to verify that both record 1 and record 2 have been erased.

Test 06 - Write Overrun Check Test

This test reads home address, spaces to within 6 cells of index, pads three cells, and then uses the extended diagnostic command (hex E4) with a hex B0 modifier to force a write overrun check.

Test 07 - Reserved

Test 08 - Pad Check Test

This test reads home address and then uses the extended diagnostic command (hex E4) with hex modifiers B3, 19, and 80 to force a pad check.

Test 09 - Read/Write Sequence Check Test

This test reads home address and then uses the extended diagnostic command (hex E4) with hex modifiers B3, 0F, and 80 to force a read/write sequence check.

Test 0A - Read/Write Sequence Check Test

This test reads home address and then uses the extended diagnostic command (hex E4) with hex modifiers B3, 0D, and 80 to force a read/write sequence check.

Routine 85 - Seek Exerciser

Routine 85 provides a high speed exercise of the device access mechanism. The routine starts by rezeroing the access and seeking to a starting cylinder location. The routine then seeks outward in fixed increments a fixed number of times and seeks back to the starting cylinder using the same seek increment. Access position is verified at the outermost and innermost cylinders by reading the home address using head 0.

In normal (default) operation, the routine is repeated 10 times using 10 different seek patterns.

Parameters

Seven parameter entries are applicable to this routine as follows:

Parameter 0 is the run control parameter, which is described on DIAG-3. Any valid run control functions can be used with this routine. If the routine is looped, the initial steps (rezero and seek to the starting cylinder position) are repeated only when required to recover from an error condition.

Parameters 1 and 2 specify the starting cylinder address in hex (0xxx). The entry of an invalid cylinder address causes the use of the 10 default seek patterns.

Parameters 3 and 4 specify the seek increment to be used (in hex). Entry of an invalid (too large) seek increment causes the routine to end without performing any seeks except the seek to the starting cylinder.

Parameters 5 and 6 specify the number of forward seeks, from the starting cylinder, to be performed (in hex). After the specified number of forward seeks have been performed, the same number of reverse seeks are performed to get back to the starting cylinder. If an invalid (too large) number of forward seeks is specified, the routine reduces these parameters to the largest acceptable value.

Routine 8A - Incremental Seek Exerciser

Routine 8A provides a high speed exercise of the device access mechanism. The routine consists of two tests (01 and 02) which are always run in sequence.

Each of the two tests executes an incremental seek pattern as defined by parameters. The seek pattern for test 01 is defined by parameters 1 through 6, and the pattern for test 02 is defined by parameters 7 through 12. In each test, a seek is performed to a specified starting cylinder. Then seeks are performed in specified increments until a specified ending cylinder is reached. The two tests are sequentially repeated the number of times specified by parameter 13.

Access position may be periodically verified by reading home address. The points at which the home address is read and the head to be used are defined by parameter entries 14 and 15.

On initial entry to this routine, a rezero operation is performed to establish a known access position. The rezero operation is not subsequently repeated, even if the routine is looped, except when required for recovering from a device check or physical address miscompare condition.

Routine 8A normally ends with IC 8AFF (see IC description) unless looping is specified in the run control parameter. If looping is specified, this ending message is bypassed.

Parameters

Sixteen parameters are applicable to this routine.

Parameter 0 is the run control parameter, which is described on DIAG-3. Any valid run control value can be used with this routine.

Parameters 1 and 2 specify the starting cylinder address for test 01. See the notes at the end of this description.

Parameters 3 and 4 specify the ending cylinder address for test 01. See the notes at the end of this description.

Parameters 5 and 6 specify the seek increment (length of each seek) for test 01. See the notes at the end of this description.

Parameters 7 and 8 specify the starting cylinder address for test 02. See the notes at the end of this description.

Parameters 9 and 10 specify the ending cylinder address for test 02. See the notes at the end of this description.

Parameters 11 and 12 specify the seek increment (length of each seek) for test 02. See the notes at the end of this description.

Parameter 13 specifies the number of times, in hex, that the test sequence (tests 01 and 02) is to be repeated. The valid range is hex 00 to FF, meaning that the test sequence is to be run from 1 to 256 times. See the notes at the end of this description.

Parameter 14 specifies when home address is to be read for verifying access mechanism position.

Value	Meaning
00	Do not read HA at all.
01	Read HA only at starting cylinders.
02	Read HA only at ending cylinders.
03	Read HA only at starting and ending cylinders.
04-FF	Read HA after every seek.

Parameter 15 specifies the head to be used when reading the home address. Valid range is hex 00 through 0E. Entry of an invalid head address results in IC 8AB0.

> **Note:** *If the routine is not being looped, a maximum of 65535 seeks are performed before the routine ends with IC 8AFF. This prevents overflow of the counters that are displayed for IC 8AFF.*

Valid cylinder address range, in hex, is from 0000 to 0375 for a 3380-J, and from 0000 to 0A5F for a 3380-K. The special value FFFF indicates that the largest valid value for the device being tested is to be used. Entry of an invalid (too large) cylinder address causes IC 8AB0.

Valid seek increment range is from 0000 to 0xxx where xxx is the difference, in hex, between the starting and ending cylinders. The special value FFFF indicates that the largest valid value for the specified starting and ending cylinders is to be used. Entry of an invalid (too large) seek increment causes IC 8AB0.

If the starting and ending cylinder addresses are the same or if the specified seek increment is 0000, then only the seek to the specified starting cylinder is performed.

If the difference between the starting and ending cylinders is not an exact multiple of the seek increment, then either the starting or ending (whichever is larger) cylinder address is decreased to meet this criteria.

Default hex values for parameters 1 through 15 are 0000FFFF0001FFFF00000001000300. This causes the routine to seek, one cylinder at a time, from cylinder 0000 to the highest valid cylinder address and back to cylinder 0000. The test sequence is run only once. The home address is read using head 0 at the starting and ending cylinders only.

Routine 90 - DPS Test

Note: Routine 90 is available only when attached to a 3880 control unit.

Routine 90 tests controller Dynamic Path Selection (DPS) functions. The routine consists of 10 tests (numbered in hex 01 to 0A) that are normally run in sequence.

This routine requires use of both controllers. The routine is started first on one controller then on the other. The first controller is called the 'slave' and the second is called the 'master'.

When routine 90 is run under the Diagnostic Aids option, the controller selected by the user becomes the master controller. The other controller is therefore started first and becomes the slave.

When routine 90 is started on either controller, tests 01 through 04 perform a partial test of DPS operation, then test 05 checks the content of a reserved area in the DPS array to determine if routine 90 is running on the other controller. The result of test 05 determines whether that controller is to be master or slave.

After the master/slave relationship has been established, all control of the routine is from the master side and all error information is supplied from the master side.

Because tests 06 through 0A run on both controllers, an indication as to which controller detected an error is sometimes useful. To provide such an indication, these tests are numbered 86 through 8A on the slave side only. (The test numbers are in error byte 1 for some isolation codes.)

Parameters

Two parameters are applicable to routine 90.

Parameter 0 is the run control parameter, which is described on DIAG-3. All normal run control functions are applicable to this routine.

Parameter 1 specifies a test to be looped. If this parameter contains a valid test number (hex 01 to 0A), that test loops indefinitely after all preceding tests have been successfully run. If this parameter does not contain a valid test number, each test runs only once. The default value for this parameter is 00 (run all tests).

Test Descriptions

The following tests are contained in routing 90:

Test 01 - Preliminary Checkout

This test performs a partial test of the ability to sense both the primary and alternate DPS status and to set and reset DPS locks.

Test 02 - Diagnostic Array Test

This test tests the ability to write and read in the diagnostic communication area of the DPS array using the write and read DPS array commands.

Test 03 - Set/Reset Under Mask

Test 03 performs the same functions as test 02 except that the set and reset under mask commands are used to modify the content of the DPS array.

Test 04 - DPS Checker Checks

Test 04 forces all DPS hardware checkers on and checks for correct DPS error indications in the controller fault log.

Test 05 - Master/Slave Determination

Test 05 determines whether the controller being tested is to perform the functions of master or slave for subsequent tests.

Test 06 - Master/Slave Synchronization

Test 06 checks the ability to establish and maintain synchronization between the master and slave portions of a test.

Test 07 - Set/Reset Status

Test 07 checks the ability to set, reset, and sense the array updated latches, the array locks, and the array initialized latches.

Test 08 - Array Initialization

Test 08 checks that the DPS array initialized indicators are on and performs a partial test of the array copy function.

Test 09 - Main Array Test

Test 09 checks the ability to write and read in all areas of the DPS array.

Test 0A - Device Busy Test

Test 0A checks for correct device busy indication on selection and polling sequences and in alternate DPS status.

Routine 91 - Home Address Scan

Routine 91 can be used to read the home address from any track. It is used to determine if a track has a valid readable home address. This routine is normally run under main option 1 (Run Diagnostics). It may be run in Diagnostic Aids mode but there is usually no advantage in doing so.

Parameters

Six parameters are applicable to this routine.

Parameter 0 is the run control parameter, which is described on DIAG-3. Any valid run control value can be used with this routine.

Parameters 1 and 2 contain the address of the first track to be read in normal physical address form (see note below).

Parameters 3 and 4 contain the address of the last track to be read in normal physical address form (see note below).

Parameter 5 specifies the number of times each track is to be read. This parameter is entered in the form xy, where x is the minimum number of times the track is to be read and y is the minimum number of times the track is to be read if a data check occurs while reading the track. The default value for this parameter is 22 hex.

Note: *See DIAG-72 for a description of physical address form. Parameters 1 and 2 must contain a track address that is lower than that contained in parameters 3 and 4 except for the special values*

listed below. Entry of invalid parameter values will result in IC 91F0. Special values that are allowed for parameters 1 through 4 are as follows:

```
0000FFFF - Read all normal customer tracks. (default values)
CECExxxx - Read all CE and diagnostic tracks.
AAAAxxxx - Read all home address MAP tracks.
```

Routine 93 - DDC Tests

Note: Routine 93 is available only when attached to a 3880 control unit. Routine 93 tests the DDC (control interface) from the storage director. Routine 93 is normally run with the MD attached to the 3880. Isolation codes produced by this routine are not included in the IC Descriptions. Any error detected by this routine indicates a problem with the DDC that should be isolated through the use of MAP-1, Entry D in the MIM.

Routine 93 does not require a device in CE mode.

Parameters

Routine 93 uses only one parameter, the run control parameter, which is described on DIAG-3.

Routine 96 - Device Status Test

Routine 96 is used to obtain string configuration and device status information. It is not a comprehensive test of machine operation, but does provide a quick indication as to which devices are probably usable and which are not.

This routine selects devices 0 through F, one at a time, and attempts to read the home address on the track in the current cylinder. The routine does not interfere with system use of the devices being tested. The devices need not be in CE mode and no device need be selected when running this routine under the Diagnostic Aids option.

This routine normally ends with IC 9699. See the IC 9699 description for more information.

Parameters

Routine 96 uses only one parameter, the run control parameter, which is described on DIAG-3. No other parameters should be entered. Because the purpose of this routine is to present configuration and status information, the routine should not normally be looped and error halts should not be bypassed.

Routine 97 - Sense Utility

This routine collects and displays status from the 3380-JK. Three classes of status can be collected:

- Controller check-1 status
- Controller check-2 and device check-1 status
- Device status

If device status is to be collected, the device address must be specified during the selection of routine 97. If no device is specified, only the controller is selected. Routine 97 normally ends with IC 9790, 97A0, or 97B0.

Parameters

Two parameters are applicable to routine 97.

Parameter 0 is the run control parameter, which is described on DIAG-3. Any valid run control value can be used, but error stops should not be bypassed if the status is to be observed.

Parameter 1 determines the status to be collected. Hex 01 collects controller check-1 status, which is collected through an RCC sequence.

If parameter 1 is hex 02, controller check-2 and device check-1 status is collected. This status is collected through the Sense Fault Log command.

If parameter 1 is any value other than hex 01 or hex 02, device status is collected through the device sense commands.

The default for parameter 1 is 00, which specifies the collection of device status.

Routine 98 - Error Log Search

Routine 98 is used to search the error log contained in the attached storage control. The error log contains sense information for up to 16 checks that were reported to the attaching host system for each string. Criteria from parameters determine which checks are logged.

The error log is not intended as a replacement or a supplement to EREP data. The error log is intended to provide error data when no sense data can be obtained, such as when the fault is on the system pack or a paging pack.

Routine 98 searches the error log based on search arguments provided through parameters. The search arguments identify the symptom codes and the devices to be included in the search. Devices can be identified in the 'local string' and in the 'other string'. (The 'local string' is the 3380-JK string to which the MD is attached. The 'other string' is the other 3380-JK string that connects to the same storage director as the string to which the MD is

attached.) When a matching entry is found in the error log, the sense bytes from that entry are displayed.

Error log searches with routine 98 are normally run through the selection of main menu option 2 (Error Log Function). Error log searches can be performed in Diagnostic Aids mode. When run in Diagnostic Aids mode, error log information is reported as error halts (with isolation codes).

Isolation code 98F1 indicates that an error log entry that matches the search arguments was found. The error bytes for isolation code 98F1 contains the first 12 of the 24 bytes of sense data for the matching error log entry. IC 98F1 is followed by IC 98F2 with the remaining 12 bytes of sense data. (See the IC descriptions in this section for more information.)

Continuing routine execution after a 'Match Found' display causes the routine to continue searching the error log for the next log entry that matches the search arguments. Normal completion of the routine indicates that the entire error log has been searched.

Routine 98 may also be used in Diagnostic Aids mode to reset (erase and restart) the error log. However, using main option 2 is simpler.

Parameters

Up to fifteen parameters are used for routine 98. The number of parameters used depends on the function specified by parameters 1 and 2.

Parameter 0 is the run control parameter, which is described on DIAG-3. Any valid value can be specified for parameter 0, but error halts should not be bypassed.

Parameters 1 and 2 specify the function to be performed. The three functions are:

- Erase log and restart logging
- Set mask
- Search and display

See the headings with those function names.

Erase Log and Restart Logging

To erase the log and to restart logging, parameters 1 and 2 must contain 0101 (hex). Parameters 3 through 10 need not be entered.

Set Mask

The Set Mask function changes the criteria for logging. To activate this function, parameters 1 and 2 must be 0303 (hex). Parameters 3 through 8 specify masks that are applied to sense records to determine whether a record is to be logged or bypassed.

Parameters 3, 4, and 5 are are used as a mask for the Unit Check Description bytes (bytes 0 through 2) in the sense records. This mask is logically ANDed with the Unit Check Description bytes as the first test for logging. If the result from the AND is 0 (no 1-bits match), the record is bypassed (not logged). If the result from the AND is 1, a second test is applied to the sense record.

The second test involves a mask specified by parameters 7 and 8. Parameter 6 is ignored. Parameters 7 and 8 form a bit significant mask for sense format. The high-order bit of parameter 7 represents format 0, and the low-order bit of parameter 8 represents format F (if there were one). When the format of the record corresponds to a 1-bit in the mask, the record is logged.

If the mask is changed, the default mask for routine 98 can be restored by entering 03031000004180 (hex) for parameters 1 through 8. The 100000 mask for the Unit Check Description bytes specifies that logged records should be equipment checks. The 4180 for parameters 7 and 8 specifies that only formats 1, 7, and 8 qualify for logging.

Search and Display

If parameters 1 and 2 contain any value other than 0101, or 0303 (hex), the search criteria are specified in parameters 3 through 14.

Parameters 3 through 6 contain a bit significant mask indicating the device addresses on the "other string" to be included in the error log search. Bits are numbered 00 to 1F. left to right, and correspond to device addresses 00 to 1F. A bit being on (1) indicates that error log entries for that device are to be included in the search. A bit being off (0) indicates that log entries for that device are to be skipped.

Parameters 7 through 10 have the same meaning as parameters 3 through 6 except that parameters 7 through 10 apply to devices in the string to which the MD is attached.

Parameters 11, 12, 13, and 14 define the symptom code(s) to be searched for. In searching the error log, routine 98 retrieves a symptom code (SC) from the log, performs a logical AND of the SC with the two bytes from parameters 13 and 14, and then compares that result with the two bytes from parameters 11 and 12. If these are equal, an isolation code is generated to display the log entry. If the compared values are not equal, the search continues with the next log entry.

The following are examples of routine 98 parameter entries:

Parameters 00000000000000104000000000000000 (hex) cause routine 98 to search for any log entry for devices 03 and 09 on the 'local string'.

Parameters 00020200000000800000000B075FFFF (hex) cause routine 98 to search the error log for SC B075 for device 00 on the 'local string'.

Parameters 00020200000000FFFFFFFFA000F000 (hex) cause routine 98 to search the error log for SC Axxx (any SC beginning with A) for any device on the 'local string'.

Parameters 040202FFFFFFFFFFFFFFFF00000000 (hex) cause routine 98 to search for any log entry applicable any device on either string. This is the default that is used if no parameters are entered.

Routine 99 - Motor Start Test

Routine 99 tests the device power-on and motor start functions. Routine 99 should be used for fault isolation only if routine 81 detects a possible motor-start problem.

Routine 99 is normally run by the MD as part of option 6 (Motor Test) of the Diagnostic Menu. In diagnostic option 6, the MD displays instructions to the user. Routine 99 starts with the drive motor off, exercises power relays, and, if successful, allows a full power on of the drive.

Warning: The following special operating procedures must be used to run this routine in Diagnostic Aids mode. If any IC other than those listed in this procedure occurs in Diagnostic Aids mode, the routine cannot be continued. It must be restarted with step 2.

1. Place both devices in the drive in CE mode. (This routine requires that the drive motor be stopped and started.)

2. Place the drive 'Motor Power' switch in the 'Off' position. and wait for the drive motor to come to a complete halt.

3. Place both left and right 'Logic Enable/Disable' switches in the 'Disable' position.

4. Run routine 99. Either of the two drive addresses may be selected. Do not enter parameters and do not loop the routine or bypass error halts.

5. When IC 9991 appears, indicating the successful completion of the first test, perform the following steps.

   a. Power off both devices in the drive being tested. See the CARR section for power procedures.

   b. Power on the left device.

   c. Move the left 'Logic Enable/Disable' switch to the 'Enable' position.

   d. Wait at least 20 seconds, and press Enter on the MD to restart the routine.

6. When IC 9992 appears, indicating the successful completion of the second test, perform the following.

a. Move the left 'Logic Enable/Disable' switch back to the 'Disable' position.

b. Power off the left device.

c. Power on the right device.

d. Move the right 'Logic Enable/Disable' switch to the 'Enable' position.

e. Wait at least 20 seconds, and press Enter on the MD to restart the routine.

7. When IC 9993 indicates successful completion of the third test, perform the following.

   a. Move the right 'Logic Enable/Disable' switch back to the 'Disable' position.

   b. Power on the left device.

   c. Move the drive 'Motor Power' switch to the 'On' position.

   d. Move both the left and right 'Logic Enable/Disable' switches back to the 'Enable' position.

   e. Wait at least 20 seconds, and press Enter on the MD to restart the routine.

8. When IC 9994 indicates successful completion of the fourth test, press Enter on the MD to restart the routine. The routine then waits approximately 3 minutes for both devices to become ready. Normal completion of the routine indicates that both devices are ready.

Error Byte 1

For any IC generated by routine 99, error byte 1 (test number) is in the form nx where n is the test number (1, 2, 3, or 4) and x is 0 if the left device failed or 1 if the right device failed.

Parameters

Use the defaults. Enter no parameters. Only the run control parameter (parameter 0) is applicable to this routine. Because of the special operating procedures required, this routine should not be looped and error halts should not be bypassed.

Test Descriptions

The tests in routine 99 are described in the following paragraphs.

Test 01 - Set-up Verification

This test verifies that both of the devices in the drive are disabled (logic switches are in the disable position). During the test, selection of the devices is attempted. If the devices are disabled (as they should be), the storage director receives an '09' end-op code from the controller when device selection is attempted. If both devices are disabled and no error occurs, IC 9991 is generated. If one of the devices is not disabled, another isolation code is generated to indicate the error, IC 9980 for the left device, or IC 9981 for the right device.

Test 02 - Left Device Test

Test 02 tests drive-motor and brake controls for the left device. The left device must be enabled and the right device must be disabled and powered off.

The left device is selected, and the Start Spindle Power Sequence Test command is used to exercise the brake solenoid and to sense relay lines. Device status is checked.

That sequence is performed 16 times, and if no errors are detected, IC 9992 is generated to indicate correct completion of the test.

Test 03 - Right Device Test

Test 03 tests drive-motor and brake controls for the right device. The right device must be enabled and the left device must be disabled and powered off.

The right device is selected, and the Start Spindle Power Sequence Test command is used to exercise the brake solenoid and to sense relay lines. Device status is checked.

That sequence is performed 16 times, and if no errors are detected, IC 9993 is generated to indicate correct completion of the test.

Test 04 - Drive Power-On

Test 04 powers on the drive motor. Both devices must be enabled (logic switches in the enable position).

The left device is selected and the Start Spindle Power On (hex 40) command is issued. Then the left device is de-selected. The right device is selected, and the Start Spindle Power On command is issued. The right device is then de-selected.

Approximately one minute elapses, and the left device is selected and tested for errors. Then, the left device is de-selected, the right device is selected, and the right device is tested for errors.

If no error was detected, IC 9994 indicates successful completion of that part of the test.

If the Enter key is pressed, the test continues until both devices are 'ready', until an error is detected, or until approximately 15 minutes has elapsed. 'Ready' is indicated when both the On-line and Attention bits (bits 4 and 5) are on in the Device Status-1 responses from the devices.

Routine 9C - CE Track Repair

Routine 9C can be used to perform a surface analysis on any track in the CE cylinder or in the four diagnostic cylinders. After the surface analysis, routine 9C rewrites the home address record with new skip control information to skip any defects that were found on the track.

This routine should be used to restore a CE track when an excessive number of data checks indicate that the track may have developed a surface defect. This routine should not be run when any hardware problem other than disk surface defects is suspected.

Routine 9C performs surface analysis on only one track at a time. Parameters must be entered to specify the track to be analyzed.

During the execution of this routine, the location of the read/write heads is verified as follows. The first attempt to verify is with the lowest numbered head that is not associated with the track specified for analysis. If reading is performed without errors, and the physical address read is the same as the physical address expected, then the location of the read/write heads is considered verified.

If an error is detected, verification is attempted with the next read/write head that is not associated with the track specified for analysis. Again, if the read operation produces no data checks, and the physical address read is as expected, the location is verified. Again, if an error is detected, verification is attempted with the next read/write head.

Parameters

Five parameters are applicable to this routine.

Parameter 0 is the run control parameter, which is described on DIAG-3. Any valid run control value can be specified for this routine, but routine 9C does not link to any routine, and error stops should not be bypassed. A run control value of hex 04 should normally be used.

Parameters 1 and 2 specify the physical address (PA) of the track to be analyzed. The physical address must be entered in standard PA form and must specify a track in the CE cylinder or in a diagnostic cylinder. Entry of an invalid physical address results in IC 9C80. This IC cannot be bypassed.

Note: *Standard form for a physical address is xxyz where xx is the last two hex digits of the cylinder address, y is the first hex digit of the cylinder address, and z is the head address in hex.*

Note: *Routine 9C normally ends with IC 9CFF.*

The correct values for parameters 1 and 2 are shown in the following table, in which the head address (z) is in hex.

Cylinders	3380-J	3380-K
CE Cylinder	763z hex	62Az hex
1st Diagnostic Cylinder	773z hex	63Az hex
2nd Diagnostic Cylinder	783z hex	64Az hex
3rd Diagnostic Cylinder	793z hex	65Az hex
4th Diagnostic Cylinder	7A3z hex	66Az hex

Figure 1. Values for Parameters 1 and 2..

Default values for parameters 1 and 2 are hex 0000. Use of the default parameters causes the routine to end with IC 9C80.

Parameter 3 specifies the number of times each cell is to be written during surface analysis. The default value for this parameter is 0A.

Parameter 4 specifies the number of read errors required to indicate that a cell is defective. The default value for this parameter is 01.

Routine 9D - DPS Array Display/Dump Utility

Note: Routine 9D is available only when attached to a 3880 control unit.

Routine 9D is to be used under the direction of product engineering. It may be used either to display the contents of the DPS array at the MD or to dump the contents of the array to the trace area in the storage director control store.

If the display option is used, the routine halts with IC 9DA0 to display the array address and content. See the description of IC 9DA0 for instructions and for the error byte assignments.

If the dump option is used, the contents of the DPS array are dumped to the trace area in the storage director control store. A system level program or a storage control MD function is required to retrieve this information from the storage director control store. The 3380-JK maintenance package does not contain any facility for displaying the contents of the storage control trace area.

> **Note:** *The trace area in control store is used for several mutually exclusive functions. It may contain trace information, DPS array data (from this routine), or error log information. Dumping the DPS array to the trace area stops all error logging functions until the error log is reset and restarted with routine 98.*

Parameters

Three parameter entries are applicable to routine 9D.

Parameter 0 is the run control parameter, which is described on DIAG-3. Any valid run control value can be used, but a value of hex 04 should normally be used.

Parameters 1 and 2 control the function to be performed. If parameters 1 and 2 are hex FFFF, the contents of the DPS array are dumped to the storage control trace area. If parameters 1 and 2 are any value other than hex FFFF, the display function is performed, and parameters 1 and 2 are used in the generation of the starting address of the array data to be displayed.

(Valid addresses for array data are hex 0000 through 07FF. Each display of data from the array shows eight bytes of data and the address of the first of those eight bytes.)

To determine the starting address to be used for the display, routine 9D logically ANDs parameters 1 and 2 with hex 07F8. The result obtained is used for the starting address. This ensures that a valid address is generated from any parameter values and that the display always begins on an 8 byte boundary.

It is not the purpose of this document to describe the array data, which is dependent on the functional microcode and on the type of storage control to which the 3380-JK is attached. The following information about typical array data addresses is provided to help in the collection of data for product engineering.

Address Range	Contents
000-01F	Device 0 dynamic path association (DPA) field.
020-021	Device 0 dynamic availability (AVL) field.
022-023	Device 0 owed device end (ODE) field.
024-025	Device 0 pack change (PCH) field.
026-027	Device 0 reservation (RSV) field.
028-03F	Device 0 parameters.
040-07F	Device 1 fields (DPA, AVL, ODE, PCH, RSV, and parameters)
080-0BF	Device 2 fields (DPA, AVL, ODE, PCH, RSV, and parameters)
0C0-0FF	Device 3 fields (DPA, AVL, ODE, PCH, RSV, and parameters)
100-13F	Device 4 fields (DPA, AVL, ODE, PCH, RSV, and parameters)
140-17F	Device 5 fields (DPA, AVL, ODE, PCH, RSV, and parameters)
180-1BF	Device 6 fields (DPA, AVL, ODE, PCH, RSV, and parameters)
1C0-1FF	Device 7 fields (DPA, AVL, ODE, PCH, RSV, and parameters)
200-23F	Device 8 fields (DPA, AVL, ODE, PCH, RSV, and parameters)
240-27F	Device 9 fields (DPA, AVL, ODE, PCH, RSV, and parameters)
280-2BF	Device A fields (DPA, AVL, ODE, PCH, RSV, and parameters)
2C0-2FF	Device B fields (DPA, AVL, ODE, PCH, RSV, and parameters)
300-33F	Device C fields (DPA, AVL, ODE, PCH, RSV, and parameters)

Figure 2 (Part 1 of 2). DPS Array Address Table

Address Range	Contents
340-37F	Device D fields (DPA, AVL, ODE, PCH, RSV, and parameters)
380-3BF	Device E fields (DPA, AVL, ODE, PCH, RSV, and parameters)
3C0-3FF	Device F fields (DPA, AVL, ODE, PCH, RSV, and parameters)
400-4E5	Reserved
4E6-4E7	CE mode indicators.
4E8-4EF	Reserved
4F0-4FF	Diagnostic communications area.
500-5FF	Reserved
600-601	Vector left (VCL) or block update indicator left (BUL).
602-603	Reserved
604-605	Vector right (VCR) or block update indicator right (BUR).
606-607	Reserved
608-609	Disconnected chain indicator (DCC) field.
60A-60B	Reserved
60C-60D	Primed device end (PDE)
60E-60F	Reserved
610-611	Channel mode of operation (CMO) field.
612-6FF	Reserved
700-7FF	Path group ID (PID)

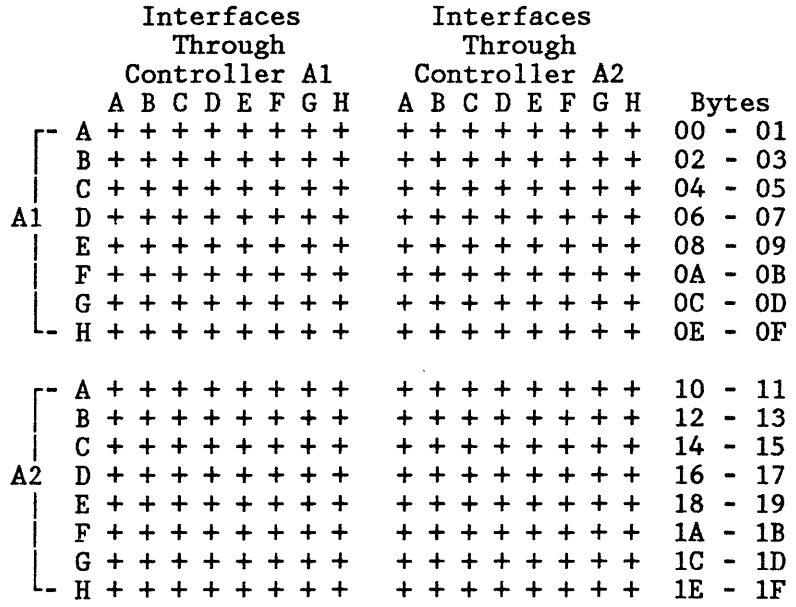
Figure 2 (Part 2 of 2). DPS Array Address Table

The default parameters for this routine are 040000, which initiates the display of array data starting at array address 0000 (hex).

Field Organization

The following paragraphs describe the organization of most of the fields that are named in the array address table.

Each DPA field contains 32 bytes of information about the associations between the channel interfaces at the storage directors with respect to the device. The DPA field is divided into 16 subfields, one for each of the possible channel interfaces (eight channel interfaces to a storage director through each of the two controllers). The bits in each subfield represent the 16 possible interfaces as shown below.



The AVL, ODE, PCH, RSV, and CMO fields are all 2-byte fields that contain bit-significant information about the channel interfaces. Bits 0 through 7 in the fields represent channel interfaces A through H at the storage director through controller A1. Bits 8 through F represent the interfaces through controller A2.

The CE mode field, the VCL or BUL field, the VCR or BUR field, and the DCC field are all 2-byte fields that contain bit-significant information relative to the devices in the string. The bits (0 through F) represent the devices (0 through F).

> **Note:** *For more information about the data from the DPS arrays, see the PDA pages in the maintenance support manual (MSM) for the IBM 3880 Storage Control.*

Routine 9E - Patch Diagnostic Microcode

Note: Routine 9E is available only when attached to a 3880 control unit.

This routine allows you to put patches in the diagnostic patch area and to reset patches previously installed by this routine.

Parameters

Up to 16 parameters may be entered.

Parameter 0 is the run control parameter, which is described on DIAG-3. This routine does not link to any other routine, and error stops should not be bypassed.

Parameter 1 specifies the function to be performed -- either to install patches or to reset previously installed patches. Hex FF specifies the reset function. Any value other than hex FF specifies the patch function. (If the reset function is specified in parameter 1, parameters 2 through 15 can be omitted.)

Parameters 2 through 15 contain information for the patches to be applied. The process for generating patches is intentionally not described because patches should not be casually constructed. To protect against errors in keying patch information, some validity checking is performed if the patch function is specified. If the patch information is found invalid, the routine ends with IC 9E80.

The default for parameters 1 through 15 is all zeros, which is invalid for patch information and causes IC 9E80.

Routine 9F - Set/Reset/Sense CE Mode

This routine is used to set devices in CE mode, to reset devices from CE mode, or to determine which devices are in CE mode. This routine is normally run through use of main option 0 or R0 to set, reset, or sense CE mode. It may, however, also be run under the Diagnostic Aids option. No device should be selected when running this routine under the Diagnostic Aids option.

This routine normally ends with IC 9FFF. Error bytes 1 through 4 contain the bit significant addresses for the devices that are in CE mode. Error bytes 5 and 6 indicate which strings or channels (if any) are write inhibited. See the description of IC 9FFF.

Parameters

Six parameter are applicable to this routine.

Parameter 0 is the run control parameter, which is described on DIAG-3. All run control functions are applicable to this routine, but because the routine normally ends with an error halt, routine looping is possible only if error halts are bypassed. Routine 9F does not link to other routines.

Parameter 1 specifies the function to be performed. An 01 (hex) indicates that CE mode is to be set for the devices indicated in parameters 2 and 3. An 02 (hex) indicates that CE mode is to be reset for the devices indicated in parameters 2 and 3. An 03 (hex) performs the same function as 02 (hex) except that all fence and write inhibit conditions are also reset if possible. An FF (hex) indicates that CE mode is to be set for the devices indicated in parameters 2 and 3 and reset for all other device addresses. All other values specify that CE mode is to be sensed only.

Parameters 2 through 5 specify which devices are to be set in CE mode or reset from CE mode. These parameters are applicable only if parameter 1 contains hex 01, 02, 03, or FF. Parameters 2 through 5 are bit significant, left to right, with each bit corresponding to a device address, 00 through 1F. A

bit being on indicates that the function specified in parameter 1 is to be performed for the corresponding device.

Default values for parameters 1 through 5 are hex 0000000000. Use of default parameters causes the routine to sense CE mode only.

Routine C0 - Controller Test

Note: Routine C0 is available only when attached to a 3880 control unit.

Routine C0 is provided to support the storage control maintenance package. It is invoked by the MD during storage control diagnostics to test the connection from the storage control to the 3380-JK.

Routine C0 is intended only for use by the storage control maintenance package. It usually produces no useful results if run in diagnostic aids mode. Isolation codes generated by this routine have no significance and are not included in the IC Descriptions. Any error detected by this routine indicates a problem with the controller that should be isolated through routine 80.

Parameters

Only the run control parameter (parameter 0) is applicable to this routine. No other parameters should be entered. The run control parameter values are described on DIAG-3.

Routine D3 - DDC Tests

Note: Routine D3 is available only when attached to a 3880 control unit.

Routine D3 is provided to support the storage control maintenance package. It is invoked by the MD during storage control diagnostics to test the connection from the storage control to the 3380-JK.

Routine D3 is intended only for use by the storage control maintenance package. It usually produces no useful results if run in diagnostic aids mode. Isolation codes generated by this routine have no significance and are not described in the IC Descriptions. Any error detected by this routine indicates a problem with the DDC that should be isolated through routine 93.

Parameters

Only the run control parameter (parameter 0) is applicable to this routine. No other parameters should be entered. The run control parameter values are described on DIAG-3.

References

This page and those that follow contain references that are identified in the error-byte tables for the isolation codes.

Test Number

For routines that contain more than one test, this byte is usually the number of the test. For routines that contain only one test, this byte might contain a diagnostic checkpoint number. See the descriptions of the routines for more definite meanings for this byte.

Command Code

The command code byte contains the hex value of the command that was last sent out on the control interface (on the DDC) when the detected error occurred. If the error occurred during selection or immediately after selection, the value in the command code byte is hex 00.

Modifier Count

The modifier count byte is set to hex 00 at the start of each selection sequence and at the start of each command sequence. Thereafter, one is added to the count for each parameter or modifier that is transferred during the sequence.

Bus Out (DBO)

The bus out byte is collected from the storage director when the storage director recognizes that an error has occurred. (The storage director detects some errors directly, but other errors that are detected by the controller or by the device must be reported to the storage director.)

Bus In (DBI)

The bus in byte is collected from the storage director when the storage director recognizes that an error has occurred. (The storage director detects some errors directly, but other errors that are detected by the controller or by the device must be reported to the storage director.)

When the storage director receives evidence in an end op code that an error has occurred, the end-op code is collected in the bus in byte. See the Tag Out and Tag In Decoded byte (described on this page) to determine that an end-op occurred. Find 'DDC Bus In' in the index of the ECM for End-Op code descriptions. (The descriptions are in the SENSE section.)

Tag Out and Tag In Decoded

This byte contains the status of the outbound and inbound tags on the control interface (DDC tags). The bit meanings are as follows:

Bit 0 = DTI Bit 0 (CCA)

0 = CCA line not active
1 = CCA line active

Bits 1-3 = DTO Bits 0-2 (Tag Out)

000 = Null Disconnect
001 = Select or Sync Out
010 = RCC 1
011 = Selected Null
100 = Poll
101 = RCC 2
110 = Hardware Immediate
111 = Command Gate

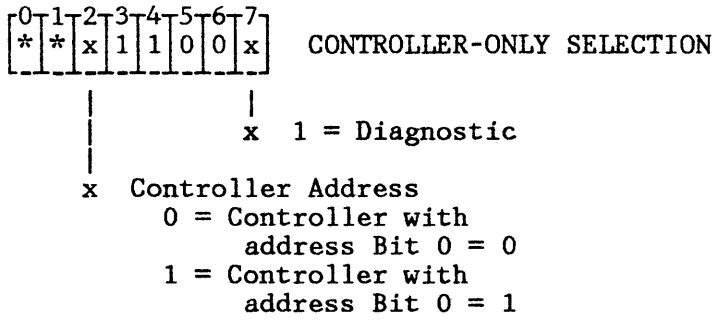
Bits 4-7 = DTI Bits 4-7 (Tag In Decoded)

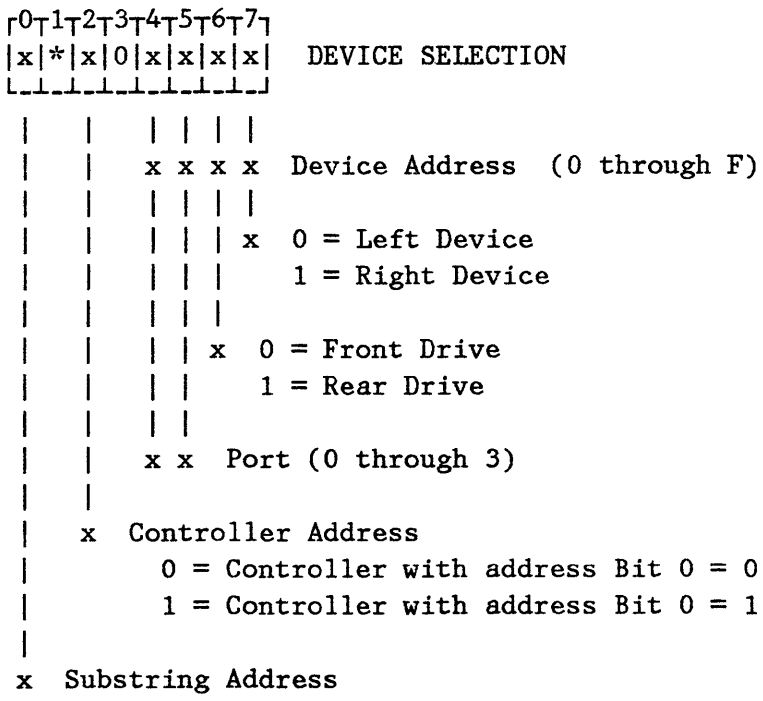
Bit 4 = Null Disconnect
Bit 5 = Valid or Sync In
Bit 6 = Selected Null
Bit 7 = End Op

If bit 7 is on, the end-op code is in the Bus In byte (described on this page).

Selection Address for Controller/Device Tested

This byte contains the address that was used to select the controller and/or device that was selected when the error was detected. The bit meanings are described in the following figures.





Note: *Bit 1 in the selection address bytes can be either one or zero in the selection address bytes. This bit position is used by the diagnostic code for temporary storage and has no meaning in the selection address.*

Request Connection Check Bits 0 through 7

The following figure indicates the meanings of the RCC bits. For more information about the RCC bits, see the SENSE section in the ECM.

Bit	Meaning
0	Controller x CCA (Sense format 7, byte 11, bit 0 or 1)
1	DPS x Unconditional Reserve (Sense format 7, byte 11, bit 2 or 3)
2-4	IOC1 Card Isolation Bits (Sense format 7, byte 12 or 14, bits 0-2)
5	DDC Bus Out Parity Check (Sense format 7, byte 12 or 14, bit 3)
6	Clock Check (controller) (Sense format 7, byte 12 or 14, bit 4)
7	Sequencer Check (controller) (Sense format 7, byte 12 or 14, bit 5)

Request Connection Check Bits 8 through 15

The following figure indicates the meanings of these RCC bits. For more information about the RCC bits, see the SENSE section in the ECM.

expand.

Bit	Meaning
8	DDC Bus In Parity Check (Sense format 7, byte 12 or 14, bit 6)
9	IOC2 Card Check-1 (Sense format 7, byte 12 or 14, bit 7)
10	Tag-Out Sequence Check (DDC) (Sense format 7, byte 13 or 15, bit 0)
11	Extended Mode Tag Check (Sense format 7, byte 13 or 15, bit 1)
12	Sequencer Detected Check (Sense format 7, byte 13 or 15, bit 2)
13	DDC Bus Floating (Sense format 7, byte 13 or 15, bit 3)
14	RCC Sequence Check (Sense format 7, byte 13 or 15, bit 4)
15	Controller x Power On (Sense format 7, byte 11, bit 4 or 5)

Note: *There are 33 bits (0 through 32) that are collected during an RCC sequence. Bit 16 is not included in the bytes shown on this page.*

Request Connection Check Bits 17 through 24

The following figure indicates the meanings of the these RCC bits. For more information about the RCC bits, see the SENSE section in the ECM.

expand.

Bit	Meaning
17-24	Controller Sequencer Detected Check-1 Code (Sense format 7, byte 16 or 18) See 'Register 1F' in the INDEX of the Error Condition Manual (ECM).

Request Connection Check Bits 25 through 32

The following figure indicates the meanings of the the RCC bits. For more information about the RCC bits, see the SENSE section in the ECM.

expand.

Bit	Meaning
25	Register Data Bus Parity Check (Sense format 7, byte 17 or 19, bit 0)
26	Always 1 (Not used)
27	Always 1 (Not used)
28	Always 1 (Not used)
29	Power On Complete (Sense format 7, byte 17 or 19, bit 4)
30	Check-2 Active (controller) (Sense format 7, byte 17 or 19, bit 5)

Bit	Meaning
31	Successful Transfer (Sense format 7, byte 17 or 19, bit 6)
32	Always 0 (Sense format 7, byte 17 or 19, bit 7)

Storage Control Check Indicators

These indicators are named as shown in the following chart. Bits 2 and 5 are used in 3380-JK sense records.

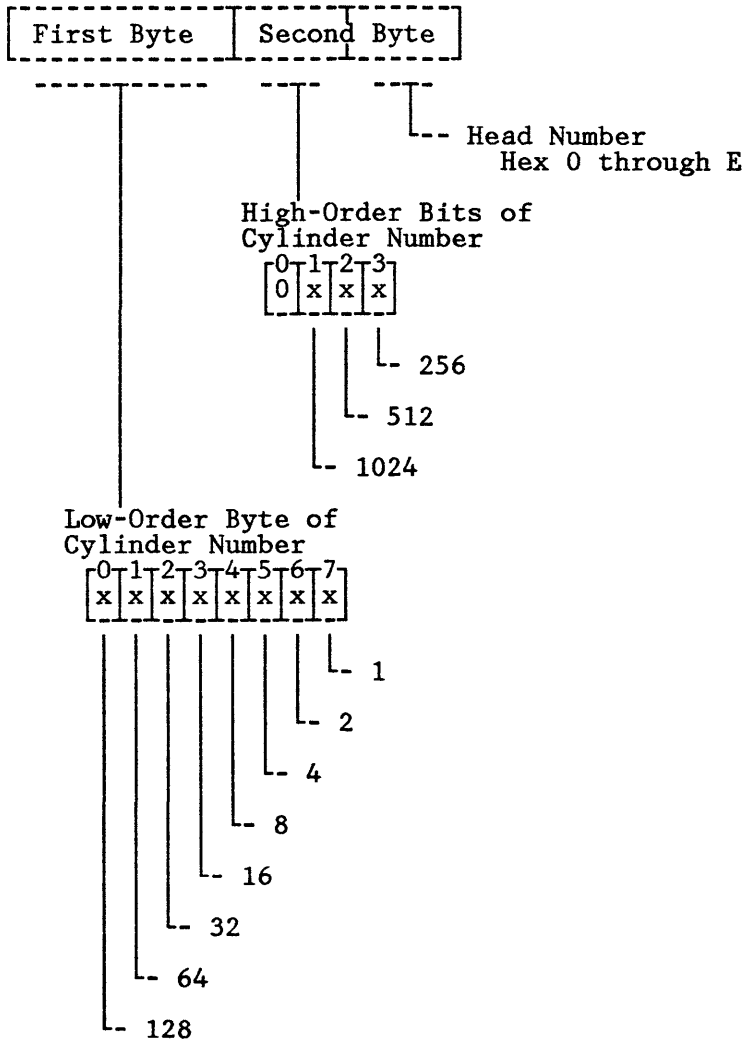
Bit	Meaning
0	Reserved
1	Reserved
2	Control Interface Check (Sense format 7 or 8, byte 10, bit 3)
3	Reserved
4	Reserved
5	Control Interface Sync In Check (Sense format 7 or 8, byte 10, bit 2.)
6	Reserved
7	Reserved

Incorrect Bus In Bits

Each active bit (1) in this byte identifies a bit position in the bus-in byte that did not have the expected status.

Track Physical Address

The track physical address bytes contain the cylinder number and the head number of the physical track.



The ranges of the cylinder addresses are shown in Figure 3 and Figure 4. Notice that the order of the hexadecimal characters in the tables is different from the order in the bytes shown above. The order in the bytes shown above is the same as that for bytes 5 and 6 in sense data (EREP).

Cylinder Types	Decimal	Hexadecimal
Customer Cylinders	0 - 884	000 - 374
Alternate Cylinder	885	375
Buffer Cylinders	886 - 888	See note.
CE Cylinder	886	376
Diagnostic Cylinders	887 - 890	377 - 37A
HA Map Cylinders	-3	FFD

Figure 3. 3380-J Cylinder Address Ranges

Cylinder Types	Decimal	Hexadecimal
Customer Cylinders	0 - 2654	000 - A5E
Alternate Cylinder	2654	A5F
Buffer Cylinders	2656 - 2657	See note
CE Cylinder	2658	A62
Diagnostic Cylinders	2659 - 2662	A63 - A66
HA Map Cylinders	2667 - 2669	A6B - A6D

Figure 4. 3380-K Cylinder Address Ranges

Note: *The buffer cylinders are not accessible.*

EC History of Diagnostic Section

EC HISTORY OF P/N 4519954			
EC Number	Date Of EC	EC Number	Date Of EC
475245	14Nov86	475248	25Apr88
475246	21Jul87		
475247	11Sep87		

Notes:

A

A unit OPER-5
access mechanism positioning OPER-48
  clean process OPER-48
  compress process OPER-48
  offset process OPER-48
  park process OPER-48
  rezero process OPER-48
address marks
  reading and recognizing OPER-60
  writing OPER-57
analysis with multiple ECDs HELP-18
analyze format of sense data HELP-11
area HELP-3

B

B unit OPER-5
bands
  data bands OPER-46
    inner OPER-46
    outer OPER-46
  guard bands OPER-46
    inner OPER-46
    outer OPER-46
brake, drive motor OPER-44
buffer cylinders OPER-46
byte text headings SENSE-59

C

CDP card function during polling OPER-81
CDP interface
  See device interface
CE cylinders OPER-46
cells OPER-29, OPER-50
checkpoint log byte 15 SENSE-66
clock synchronization
  to cell boundary OPER-26
  to sync byte OPER-25
command transfers during track processing OPER-54
commands OPER-83
connection check alert and power status, byte 11 SENSE-78
control interface OPER-13
  control mode OPER-13
  line descriptions OPER-13
  transfer mode OPER-13
controller fault log A, byte 11 SENSE-82
controller fault log B, byte 12 SENSE-83
controller fault log C, byte 13 SENSE-83
controller fault log D, byte 14 SENSE-84
controller fault log E, byte 15 SENSE-85
controller fault log F, byte 16 SENSE-85
controller fault log G, byte 17 SENSE-86
controller functions OPER-7
controller path control OPER-22
  controller sequencer function OPER-22
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