Original Equipment Manufacturers' Information

IBM 7631 File Control

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PREFACE

The information in this manual will assist designers of accessory equipment for IBM 7631 File Control Models 1, 2, 3, 4, and 5 and IBM 1301 Disk Storage Models 1 and 2. Additional details about the operation and use of these units in integrated data processing systems may be obtained from the local IBM Sales Office. If additional technical information is needed, customer engineering manuals are available from the local IBM Sales Office.

Descriptions and data in this manual are subject to engineering development modification.

Address comments regarding the contents of this publication to:
IBM Corporation, Customer Manuals, Dept. 298, PO Box 390, Poughkeepsie, N.Y.

CONTENTS

High-speed magnetic disk storage provides large external storage capacity to supplement internal core storage of a computer system. The IBM 1301 Disk Storage and its associated IBM 7631 File Control provide large storage capacity, fast access time to data recorded on the disks, and the ability to handle fixed or variable length records.

MAGNETIC DISK RECORDING

The magnetic disk is a thin metal disk coated on both sides with magnetic recording material. Twenty-five disks are mounted on a vertical shaft, with a small separation between the disks to provide space for the movement of read-write assemblies. The shaft revolves, spinning the disks at a maximum of 1790 revolutions per minute.

Data are stored as magnetized spots in concentric tracks on each surface of the disk (Figure 1). There are 250 tracks for the storing of data on each surface. The tracks are accessible for reading and writing by positioning the read-write heads between the spinning disks.

ACCESS MECHANISM

The read-write heads are mounted on an access mechanism which has 24 arms arranged like teeth on a comb (Figure 2). The arms move horizontally between the disks. (No vertical motion is involved.) Two read-write heads are mounted on each arm. One of the heads services the bottom surface of the upper disk while the other head services the top surface of the lower disk. Thus, it is possible to read or write on either side of a disk.

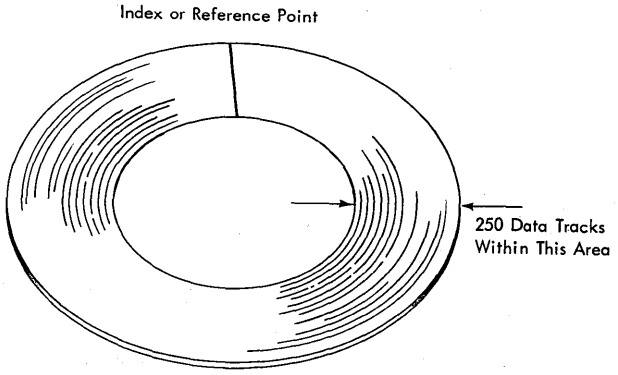


Figure 1. Magnetically Coated Disk

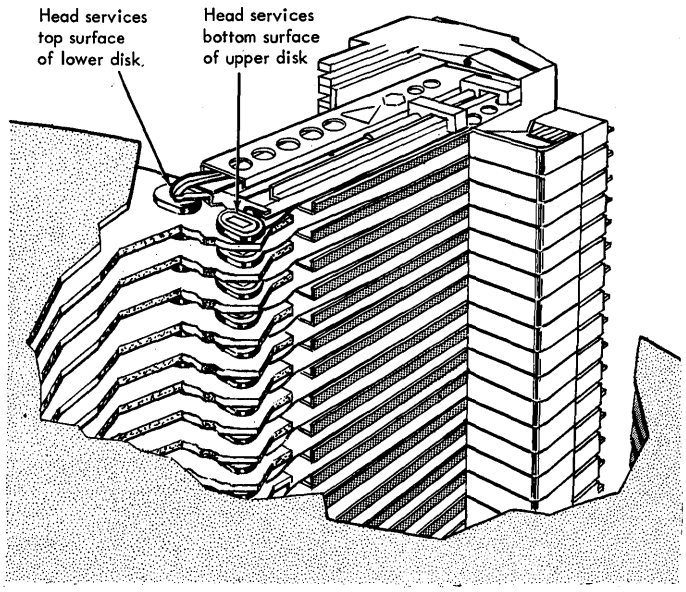


Figure 2. Head Arrangement

The magnetic disk data surface can be used repetitively. Each time new information is stored on a track, old information on the track is erased as the new information is recorded. The recorded data may be read as often as desired and will remain recorded in the tracks of a disk until it is written over.

Disk storage, like trays of cards or magnetic tape, provides external storage capacity to supplement internal core storage of a computer. Disk storage has a major advantage, however, in that all records contained in the 1301 are program-addressable, providing random access to any record or group of records, that is, faster access to any record.

Although the total number of character positions of the track is fixed, the number of records and the number of characters per record can be arranged to suit the needs of the using system. Thus, data can be stored on the track in any convenient arrangement within track limitations. Addresses must be provided to identify the track and the individual records to the computer. Also, space must be provided in the form of gaps to separate address and record areas, as well as to separate records in the record areas.

A format track is used to provide a means of defining and monitoring the address, record, and gap areas for the data tracks. In the 1301, one format track monitors 40 associated data tracks. The format track can be written and rewritten to describe the desired data track format as often as required to suit the needs of the user.

A disk storage module is comprised of the stack of 25 magnetic disks and its associated access mechanism.

Of the 25 disks, 20 disks (40 surfaces) are used to store data; of the other ten surfaces, six are used as alternate surfaces, one is a format surface, and one is a clock surface (Figure 3). The other two are not used. Each of the data storage surfaces and the format surface contains 250 concentric tracks that are accessible for reading and writing.

Read-write heads are mounted on the 24 arms of the access mechanism that moves the arms horizontally between the disks (Figure 4). No vertical motion is involved. Two read-write heads are mounted on each arm. One of the heads services the bottom face of the disk above the arm and the other head services the upper face of the disk below the arm.

The read-write heads on the 24 access arms are aligned one above the other and are mechanically moved in parallel to one of the 250 cylinder positions of the module. When the access mechanism is positioned at a specific cylinder, 40 data tracks of information are available without any further motion of the access mechanism. Only electronic head switching is necessary to select a particular track in the cylinder. With the cylinder mode optional feature, it is possible to read or write a cylinder or part of a cylinder of tracks in one operation.

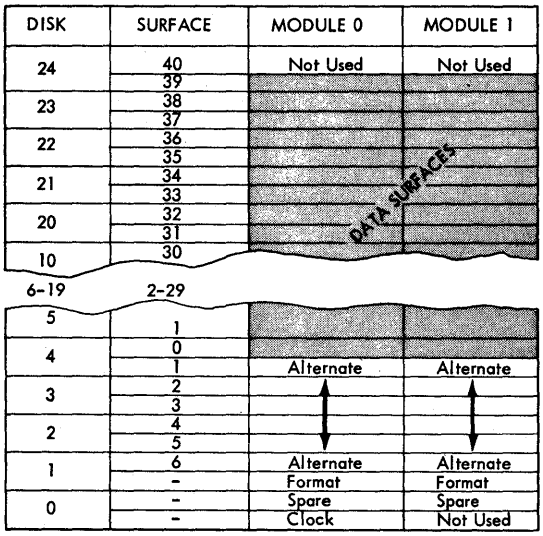


Figure 3. Disk Surface Orientation

ACCESS MOTION TIME

The time required for the access mechanism to move from one cylinder to another is related to the distance the arm moves, within certain machine defined limits. To calculate the time required, consider the 250 cylinders of a module organized into five areas of 50 cylinders per area (Figure 5). Also consider each area of cylinders further divided into six sections. Access motion time for any one access is as follows:

1. To move the access arm within a section of any one area requires 50 milliseconds.
2. To move the access arm from one section to another section of an area requires 120 milliseconds.
3. To move the access arm from one area to another area (crossing an area boundary) requires 180 milliseconds.

For example, to move the access arm from track 0000 to 1960 requires 120 milliseconds of access

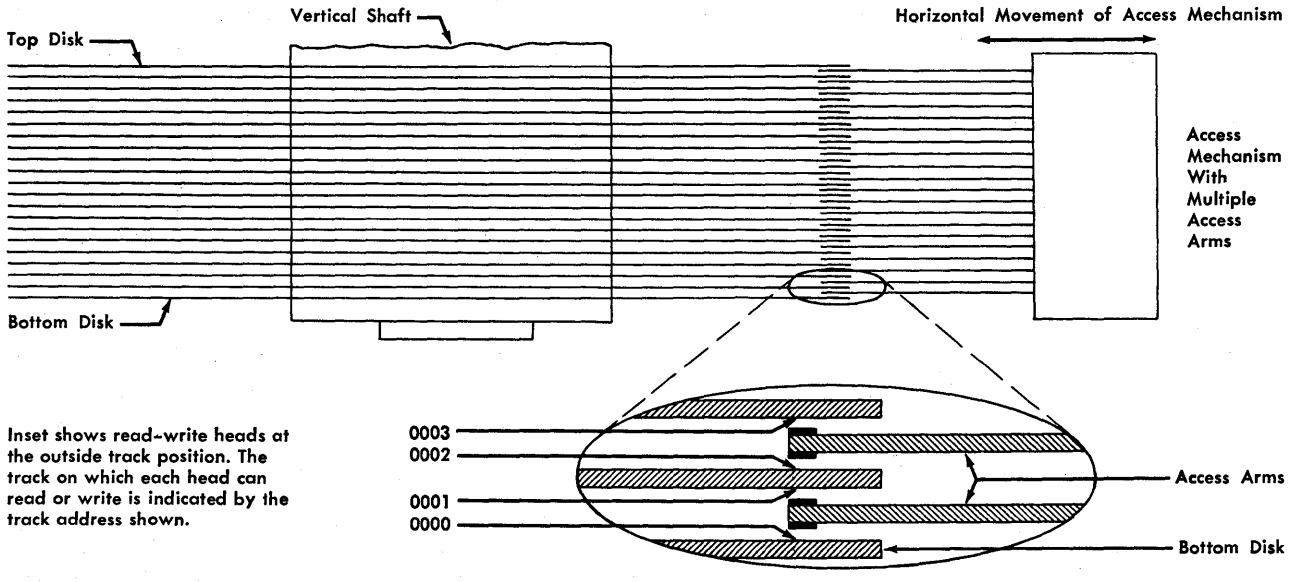


Figure 4. Module and Access Mechanism

motion time. To move the access arm from track 1960 to 2000 requires 180 milliseconds.

CYLINDER RECORDING

Since the heads and disk tracks are mechanically aligned one above the other, the vertical alignment of the tracks can be considered as a cylinder of tracks (Figure 6). Thus, with the access mechanism placed in any one of the 250 cylinders, 40 tracks of data are available without further access motion; only electronic head switching is necessary.

The tracks are numbered sequentially, from the bottom to the top of the cylinder (corresponding to the 40 heads, 00 to 39), starting at the outermost cylinder (000) to the innermost cylinder (249). Thus with large storage areas for reference tables, the data can be conveniently stored in a cylinder of tracks or in a number of adjacent cylinders. This technique reduces access time to a minimum.

The cylinder arrangement of tracks also permits the optional feature -- the cylinder mode of operation -- to read or write a cylinder of tracks, or part of a cylinder, in one operation.

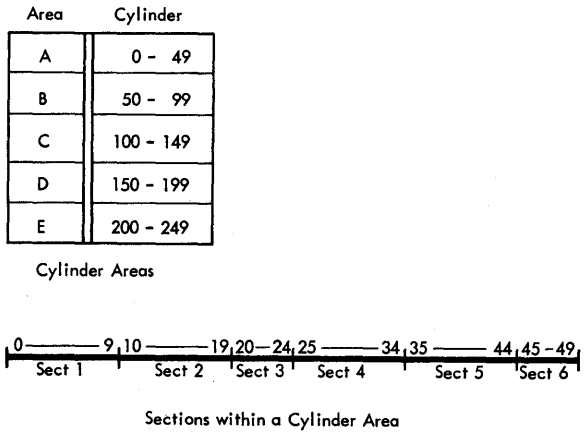


Figure 5. Access Motion Areas and Sections

DATA TRACK

The basic fixed recording area of the 1301 is the data track. The physical make-up of the track limits it to a specific overall recording capacity. The overall storage capacity of all data tracks are equal. The entire recording area cannot be used to store data, however, as a number of character positions must be set aside to provide a means of identifying the track to the using system, or a home address (HA). To provide random access to any record on the track, additional character positions must be used for each record on the track, or a record address (RA). Additional character positions are required for gaps (G) to separate addresses and records. Since the tracks are circular, an index point (I) must be used to indicate the beginning or the end of the track. Therefore, each of the 10,000 data tracks must have an index point, one home address, a record address for each record stored on the track, and the necessary gaps to separate the address and the records (Figure 7).

Index Point

The index point of the track is the reference point of the track; that is, it indicates both the beginning and the end of the track. The index point is used by the file control in conjunction with its various modes of operation.

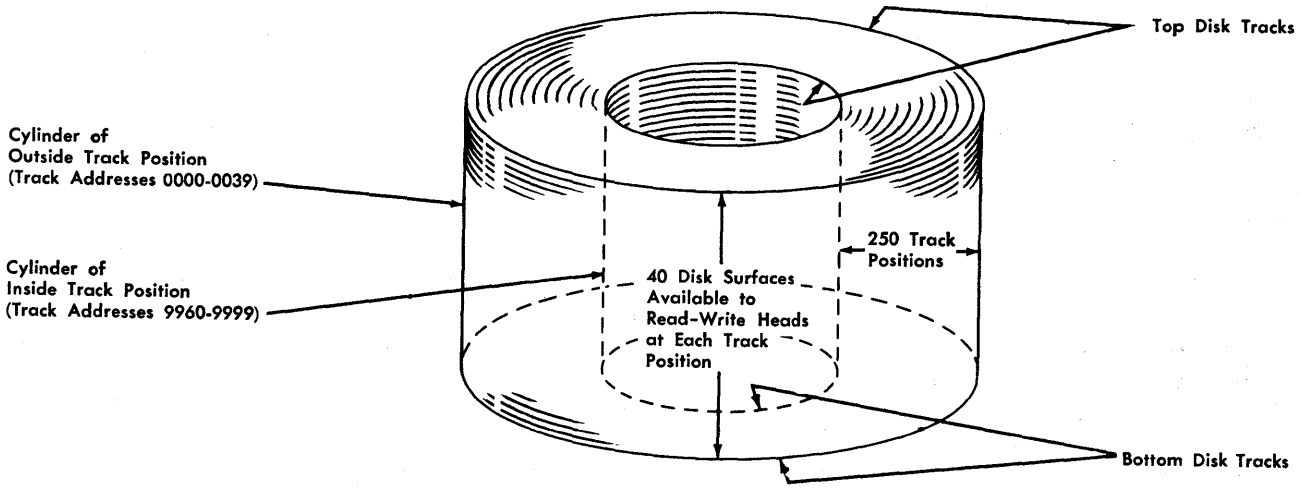


Figure 6. Track Cylinders

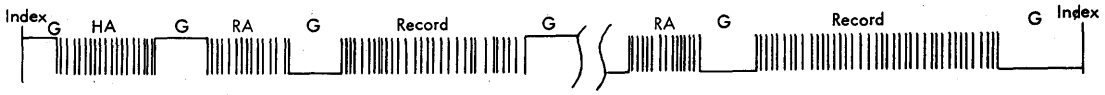


Figure 7. Track Layout

Home Address (HA)

There is one home address for each of the 10,000 tracks. The home address follows the index point and consists of two parts called home address one (HA1) and home address two (HA2).

HA1

The HA1 portion of the home address is the track number. HA1 is prerecorded; it cannot be written by the customer. The track number is a four-digit number (0000-9999), that indicates the physical location of the track within the module. The tracks are numbered sequentially beginning at the lowest track of the outermost cylinder (track number 0000). Continuing up through the cylinder, 0000-0039 represents the 40 data tracks of the outermost cylinder. The numbers continue with the lowest track of the adjacent cylinder, track number 0040, up the cylinder to track number 0079. Continuing through each of the cylinders in a like manner, the last track number (9999) is the top track of the innermost cylinder. With this method of numbering, adjacent tracks on the same disk always differ by 40. This provides a means of determining the track number for any track within any cylinder by the simple formula: Given the head number and the cylinder number, the track number is the product of the cylinder number and 40, plus the head number. For example, for cylinder number 241 and head number 20 the track number is: 241 X 40 = 9640; 9640 + 20 = 9660.

Also, with the track number known, the cylinder number and head number can be determined by dividing the track number by 40. The quotient is the cylinder number and the remainder is the head number. For example, given the track number 0590, 0590 ÷ 40 = 014 with a remainder of 30. Thus, the cylinder number is 014 and the head number is 30.

HA2

The second portion of the home address (HA2) is called the home address identifier. This portion of the address further identifies the track to the using system. HA2 is written by the user and consists of two or more characters that can be numeric, alphabetic, or special characters, depending on the requirements of the using system. Two characters are required for HA2. Even though only two characters are compared during address verification operations, additional characters can be used as a convenience for fixed word length systems.

HA2 can be written to serve any convenient purpose. For example, it can be used as a coded file protect device or it can be used to identify or tag a category of records, such as receipts, withdrawals, payments, inventory, etc.

Record Address (RA)

The record address consists of six or more characters that can be numeric, alphabetic, or special characters. It is used to identify the individual record on the track to the using system. A record address is assigned and written by the user to fit any convenient addressing system. It requires no relationship to the home address of the track where it is written, since an address is transmitted to the file control for each functional order. The home address used for seek orders, and the record address used in the prepare-to-verify (single record) order, need not be related in any way.

The record address normally consists of six characters and, even though the first four (high-order positions) can be alphabetic or special characters, depending on the system, only the numeric bit positions of these characters are compared during address verification operations. All bits of the fifth and sixth characters are compared during address verification.

Gap (G)

To distinguish between addresses and records, gaps are written between address and record areas. The gaps contain check characters and internal synchronization information required for proper machine operation.

Data are read and written on a track in six-bit or eight-bit characters or "bytes" serially by bit and serially by character. The eight-bit mode permits the use of packed format feature (packing two four-bit digits into one eight-bit character) on the 1301 by any system using that feature.

Since there are 250 tracks on each of the 40 disk storage surfaces in a module, 10,000 addressable data tracks are available in each module.

TRACK CAPACITY (7000 SYSTEMS)

Each track on a disk has 2840 six-bit or 2205 eight-bit character positions available for recording information. However, this will vary depending upon the system involved and is exclusive of HA1 and all associated gaps. Character positions necessary for home address 2, the record addresses, and gaps must be considered, however, in determining the number of character positions available for the records. In general, the track area available for record storage is the total track capacity less the character positions necessary for addresses and gaps.

TRACK CAPACITY (1410 SYSTEMS)

Each data track of the disk has a capacity of 2,840 six-bit or 2,205 eight-bit character positions for recording information and is exclusive of HA1 and all associated gaps. These figures have been adjusted to compensate for the character positions used in the prerecorded home address 1 and the gaps for the home address. To determine the number of character positions available for record storage, the character positions required for HA2, the record addresses, and the gaps must be considered. With HA2 representing the number of characters in the home address identifier, N representing the number of records on the track, L representing the number of characters per record, RA representing the number of record address characters (assumed to be the same for each record address), and 32 representing the number of character positions required for record address gaps, track capacity used can be determined by the following formulas:

For the six-bit mode:

HA2+N (L+RA+32) = 2,840 or less.

For the eight-bit mode:

HA2+N (L+RA+32) = 2,205 or less.

With HA2 equal to two character positions, RA equal to six characters positions, and L of constant length, the formulas can be reduced to:

For the six-bit mode:

N = 2838/(L+38) records per track.

For the eight-bit mode:

N = 2203/(L+38) records per track.

For a number of variable length records within the same track, the calculations require the summation of a series of quantities representing the number of records and their length or

$N_1(L_1+38) + N_2(L_2+38) + \ldots\ldots$

$N_n(L_n+38) = 2838$ (six-bit mode)

$N_1(L_1+38) + N_2(L_2+38) + \ldots\ldots$

$N_n(L_n+38) = 2203$ (eight-bit mode)

N_1 is the number of records of L_1 length in the track, N_2 is the number of records of L_2 length, etc.

The number of records per track for different record lengths (80 to 2800) and the number of character positions remaining that can be used as desired by the program are shown in Figure 8. To calculate the size of record that can be placed in the remainder of a track, assuming that the same size record address is to be used, subtract 38 from the remainder.

FORMAT TRACK

The advanced characteristics of the 1301 permit flexibility in establishing how the disk storage space is to be allocated, organized, and addressed. This concept of disk storage use makes possible a wide variety of storage formats to meet the needs of many varied applications. The concept also requires that the user organize the disk storage in some particular format prior to its use as a data storage device. These activities can be likened to the wiring of a control panel for unit record machines, to the housekeeping preparations for a program, or to masking a storage area for future use. For clarity of understanding disk storage, it is important that the operations required for establishing disk storage format should not be confused with the operations related to the use of disk storage.

Before any data can be written on or read from a data track within a cylinder, a format track for that cylinder must be written. The 250 format tracks, one for each cylinder, are located on one of the additional disk surfaces not used for data.

The function of the format track is to control the use of the data tracks of a cylinder. Once a format track has been written, it establishes the location, character size, and mode of reading or writing which can take place in the home address area, the record address areas, the record areas, and certain gap areas. Data to be written on or read from each data track of a cylinder must conform to the format established by the format track for that cylinder.

The layout and writing of the format track is under the complete control of the user. Once written, however, the format for a cylinder of tracks remains fixed until the format track is rewritten.

Characters per Record	Six-Bit Mode N (Records)	Six-Bit Mode Remainder	Eight-Bit Mode N (Records)	Eight-Bit Mode Remainder
80	24	6	18	79
100	20	78	15	133
200	11	220	9	61
300	8	134	6	175
400	6	210	5	113
500	5	148	4	51
1000	2	762	2	127
2165	1	635	1	0
2800	1	0	---	---

Figure 8. Records per Track for Various Record Sizes

PLANNING THE FORMAT TRACK

The control characters used to write a format track must first be organized in core storage as a record (format control record). The write format track instruction transfers the core storage format control record to the 7631 File Control. It is converted to a special bit configuration for machine control purposes and is written on the addressed format track. Since the format track defines, in machine form, the control action previously defined in the core storage format control record, explanation of how the data tracks of a cylinder are defined will be made in terms of the core storage format control record.

Four different characters, BCD 1, 2, 3, and 4 are used to compose a format control record in core storage. The BCD characters 1 and 2 are used to define areas of the data track which will be handling data in a six-bit mode. The BCD characters 3 and 4 are used to define areas of the data track which will be handling data in an eight-bit mode. It should be noted that certain areas of the format track are used for machine control and data checking purposes. These areas must be unconditionally provided for in the core storage format control record.

A typical core storage layout of a format control record in both the six-bit and eight-bit mode is shown in Figure 9.

Track Identification Area

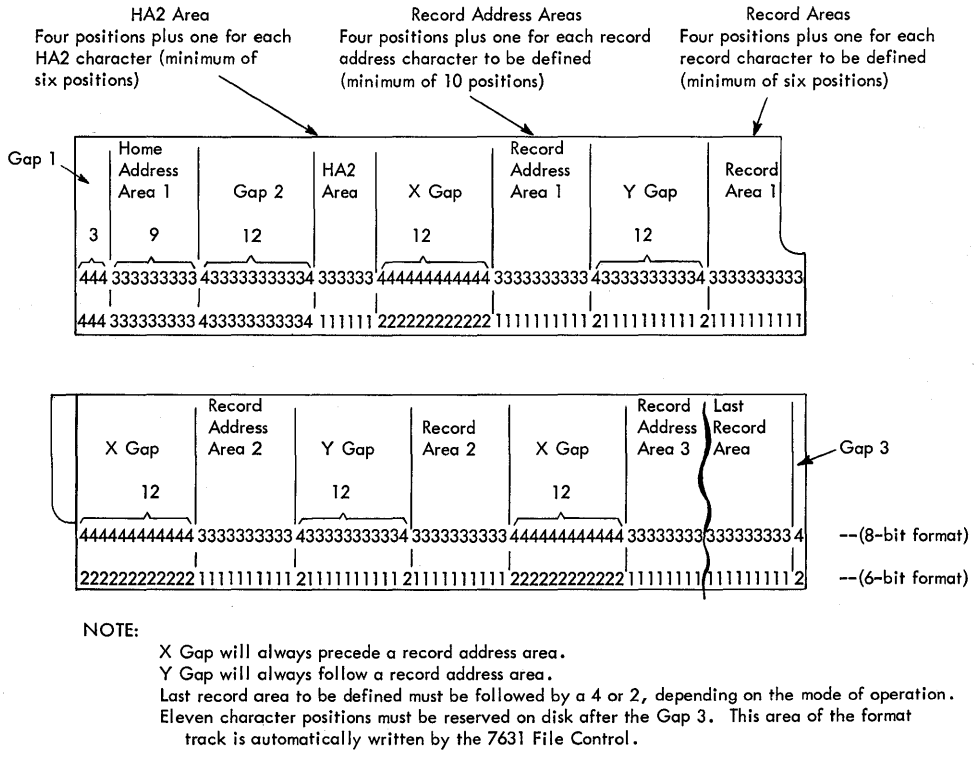
The track identification area consists of Gap 1, HA1, and Gap 2. It is always written to indicate the eight-bit mode and is the same for all format control records. Gap 1 consists of three 4's; HA1 is nine 3's; Gap 2 is a 4 followed by ten 3's and a 4. From this point, the remaining area of the format control record must indicate either a six-bit or eight-bit mode of operation. It cannot be a combination of the two modes.

Home Address 2 Area (HA2)

The format of the home address 2 (HA2) area must provide for four more character positions than the number of characters to be used for HA2. For example, if HA2 is to be a two-character home address identifier (minimum size), six BCD characters (1 or 3) must be used.

X Gap Area

An X gap area must precede every record address area of the format control record. This gap is indicated by 12 BCD characters (either 2's or 4's depending on the mode of operation).



NOTE:
X Gap will always precede a record address area.
Y Gap will always follow a record address area.
Last record area to be defined must be followed by a 4 or 2, depending on the mode of operation.
Eleven character positions must be reserved on disk after the Gap 3. This area of the format track is automatically written by the 7631 File Control.

Figure 9. Organization of Core Storage Control Record

Record Address Area

This area must provide for four more character positions than the number of characters to be used for the record address. For example, if a record address is to be six digits in length, then ten BCD 1's or 3's must be used in the format control record to define the record address area. Because a record address must have a minimum of six character positions, the record address area of the format control record must provide for a minimum of ten character positions.

Y Gap Area

A Y gap area must follow every record address area of the format track record. This gap is made up of one BCD 2 or 4, followed by ten BCD 1's or 3's and a BCD 2 or 4.

Record Area

This area must provide for four more BCD character positions than the characters required in the disk record. For example, for an 80-character record, 84 BCD 1's or 3's must be provided in the format control record. Data records can be a minimum of two characters in length. Therefore, the format control record must contain a minimum of six BCD characters. From this point the sequence of the areas to be established in the format data record is an X gap, record address area, Y gap, record area, etc., until the last record area.

Gap 3 Area

Gap 3 is a one-character gap that follows the last record area of the format track. Gap 3 is indicated in the format control record by a BCD 2 or 4, depending upon the mode of operation to be used.

NOTE: Although the format track does not need to be completely formatted for use, it does require that at least 11 character positions be reserved (not used) following the Gap 3 area of the format track. This area will be written automatically by the 7631.

TIMING CONSIDERATIONS

The disk rotation speed of 1790 revolutions per minute, combined with the data recording method, makes possible a maximum rate of 70,000 or 90,000 characters per second. An entire cylinder (112,000 characters) can be read in approximately 1360 milliseconds. A whole module (28,000,000 characters) can be read in less than seven minutes. These rates include access motion time and rotational delay time, and are significant to timing estimates for such operations as file maintenance, audit trail preparation, and disk scheduling searching, where large volumes of data can be used in the same sequence in which the data are arranged in disk storage.

When reading or writing a series of tracks, system time of 350 microseconds is provided at the end of the track to permit verification of the home address (HA) of the next track to be processed. This allotted time permits the verification of the HA immediately following the end of the previously processed track instead of waiting for a disk revolution (33 milliseconds) to reposition the HA for verification.

In establishing job times for programs that make reference to individual records or groups of records in disk storage, the disk storage reference cycle is considered. A disk storage reference cycle includes the time required to complete all the disk storage operations for a particular processing operation. A typical disk storage reference cycle (move mode), assuming a random distribution of records within the disk storage module, is shown in Figure 10.

If the records in disk storage are arranged in such a way that no access motion time is required (all records for the job stored in the same cylinder), the total disk storage reference cycle time is reduced to 88 milliseconds (Figure 10). Thus, the distribution of records within disk storage affects total job time.

Access motion time within specific groups of ten adjacent cylinders is 50 milliseconds. Access motion time within specific groups of 50 adjacent cylinders is 120 milliseconds. To compute average data access time (the time required to seek a particular data record or track in disk storage), add 17 milliseconds average rotational delay time to access motion time.

Access motion time between cylinders in a disk storage module is shown in Figure 11.

NOTE: Numbers shown in the above chart are track numbers of the lowest numbered track in each cylinder and are the "cylinder addresses." Examples:

160 ms	Average access motion time	0
17 ms	Average rotational delay time	17
3 ms	Read (using a 270 character record)	3
31 ms	Available processing time before the record can be written back	31
3 ms	Write	3
31 ms	Elapsed rotation time before a WRITE DISK CHECK instruction can be executed	31
3 ms	WRITE DISK CHECK	3
248 ms	Total Disk Storage Reference Cycle Time	88

Figure 10. Disk Storage Reference Cycle Comparison

Group 1, Block 1, contains ten cylinders (0000-0360) and 400 tracks (0000-0399); Group 3, Block 1, contains five cylinders (0800-0960) and 200 tracks (0900-0999).

Access motion time is calculated as follows: Movement between cylinders in the same group in a block is 50 milliseconds. Movement between cylinders not in the same group in a block requires: 120 milliseconds when within any one of the five blocks (examples, between cylinders 0000 and 0400, 0000 and 1960), 180 milliseconds when between any of the five blocks (examples, between cylinders 1960 and 2000, 0000 and 9960).

To approximate average access motion time for a job (assuming a random distribution of records):

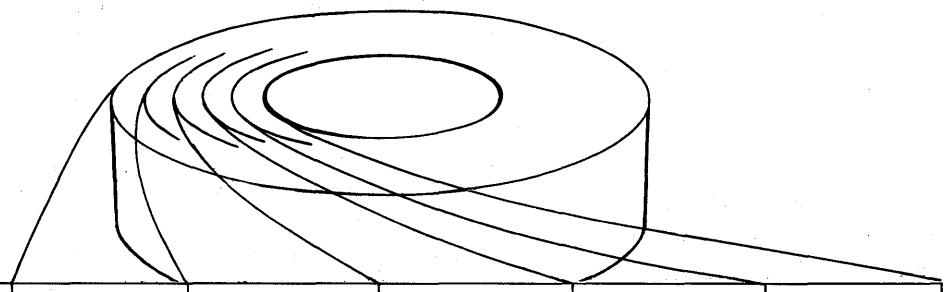
1. Determine the numbers of the cylinders to be used.
2. Select a used cylinder in the block that contains the most cylinders used.
3. From that cylinder:

a. Count the number of cylinders used in the same group and multiply this count by 50 ms.

b. Count the remaining number of cylinders used in the same block and multiply this count by 120 ms.

c. Count the remaining number of other cylinders used in the disk storage unit and multiply this count by 180 ms.

d. Divide the sum of a, b, and c, above, by the total number of cylinders used.



Group 1	0000-0360	2000-2360	4000-4360	6000-6360	8000-8360
Group 2	0400-0760	2400-2760	4400-4760	6400-6760	8400-8760
Group 3	0800-0960	2800-2960	4800-4960	6800-6960	8800-8960
Group 4	1000-1360	3000-3360	5000-5360	7000-7360	9000-9360
Group 5	1400-1760	3400-3760	5400-5760	7400-7760	9400-9760
Group 6	1800-1960	3800-3960	5800-5960	7800-7960	9800-9960
	BLOCK 1	BLOCK 2	BLOCK 3	BLOCK 4	BLOCK 5
	0000-1960	2000-3960	4000-5960	6000-7960	8000-9960

NOTE: Numbers shown in the above chart are track numbers of the lowest numbered track in each cylinder and are the "cylinder addresses."

Examples: Group 1, Block 1 contains 10 cylinders (0000-0360) and 400 tracks (0000-0399);
Group 3, Block 1 contains 5 cylinders (0800-0960) and 200 tracks (0800-0999).

Access Motion Time is calculated as follows:

Movement between cylinders in the same group in a block is 50 milliseconds;

Movement between cylinders not in the same group in a block requires:

120 Milliseconds when within any one of the 5 blocks.

Examples, between cylinders 0000 and 0400; 0000 and 1960;

180 Milliseconds when between any of the 5 blocks.

Examples, between cylinders 1960 and 2000; 0000 and 9960.

To approximate average access motion time for a specific job (assuming a random distribution of records):

1. Determine the numbers of the cylinders to be used.
2. Select a used cylinder in the block that contains the most cylinders used.
3. From that cylinder:

A. Count the number of cylinders used in the same group and multiply this count by 50 ms,

B. Count the remaining number of cylinders used in the same block and multiply this count by 120 ms,

C. Count the remaining number of other cylinders used in the disk storage unit and multiply this count by 180 ms,

D. Divide the sum of A, B, and C by the total number of cylinders used.

Figure 11. Access Motion Time

The IBM 7631 File Control is used to control the operation of up to five IBM 1301 Disk Storage units. It contains electronic circuitry for performing the following functions:

1. Transferring of addresses from the computer to the 1301.
2. Notifying the computer when a 1301 file seek has been completed.
3. Searching the file tracks for the particular record addressed by the computer.
4. Obtaining assembled data from the computer system and sending it to the IBM 1301 in a serial by bit manner during a write operation.
5. Accepting serial data from the IBM 1301 Disk Storage during a read operation and assembling it into characters for transmission to the computer systems.
6. Providing status information to the computer system, on command.

The IBM 7631 File Control may be used with any IBM Data Processing System that uses the IBM 1301 Disk Storage; however, different models of the 7631 are required depending on the computer system involved. The different models and their system or systems assignments are:

Model 1 - For disk storage use with a single IBM 1410 system

Model 2 - For disk storage use with a single IBM 7040, 7044, 7070, 7074, 7080, 7090 or 7094 system

Model 3 - For shared disk storage use by an IBM 7000 system (as listed above) and an IBM 1410 system

Model 4 - For shared disk storage use by two IBM 7000 systems (as listed above).

Model 5 - For shared disk storage use by two IBM 1410 systems.

A maximum of five IBM 1301 Disk Storage units may be used per system or combination of systems with a maximum of two IBM 7631 File Controls connected to the five disk storage units.

Because of basic operational and design differences between the IBM 7000 and IBM 1410 systems, two types of programming and systems connecting lines are used. The operational information and line functions for computer to 7631-1301 operations are separately provided in this manual. Additionally, 7631-1301 operations in specific IBM Data Processing Systems are available in the following IBM references.

System	Reference Form No.
1410	A22-6670
7040/44	A22-6649
7070/74	G22-6594
7080	G22-6604
7090	A22-6528
7094	A22-6703

The functions performed by the 7631 and 1301 and the using 7000 systems data channels are based on the execution of commands, orders and instructions.

FILE CONTROL OPERATIONS WITH 7000 SERIES SYSTEMS

Commands

The 7631 uses four commands relating to disk storage operation: read, write, sense, and control. (A command is defined as system-coded information, decoded by a system data channel and executed by the file control, to perform a specific function.) The four commands executed by the 7631 are:

Read Command: A command that sets up the necessary control circuitry in the connecting data channel to permit information stored in the disk storage to be read and transmitted to the computer system, through the file control.

Write Command: A command that sets up the control circuitry in the connecting data channel to permit information to be transmitted from the computer system, through the file control, to the disk storage, and to write upon a designated disk track.

Sense Command: A command which causes transmission of status information from the file control to the computer system to indicate the status of the disk storage unit or units and the file control. Status conditions such as error and unusual conditions as well as attention conditions are affected by the sense command.

Control Command: A command which is used to transmit orders to the file control. (An order is defined as control coded information that is decoded and executed by the file control to perform a specific function.) Orders are transmitted to the file control in the same manner as data are normally transmitted. The file control recognizes the information as an order and sets up the necessary decoding and execution circuitry to process the order. Transmission of orders to the file control as a result of the command is the same for all computer systems using the 7631 File Control, although they may be initiated by a different method.

Orders

Orders normally consist of a two-digit operation code and eight characters to define addresses. When

address information is not required, the order consists of the operation code only. The make-up of the order is shown in Figure 12.

Orders are transmitted from the computer's data channel as BCD characters over the write bus. The 7631 File Control accepts the digit portion of the first eight characters of the order (operation code, access and module number, and the first four positions of the address) and all bits in the ninth and tenth characters of the order.

Operation Code: A two-digit code that specifies the operation to be performed. This portion of the order is always numeric. The operation code is all that is required for the following orders: no operation, six-bit mode, eight-bit mode, and release.

Access and Module Number: These two positions of the order, which are always numeric, specify the module in which the operation will take place.

Record or Home Address: This portion of the order gives the home or record address, depending on the type of operation that is to take place.

The 7631 File Control will decode and execute any of 13 orders transmitted from the computer by the control command. The 7631 decodes the transmitted order, accepts address information, performs the designated function, and then transmits an end signal or unusual end signal to the computer. In the case of a seek order, the file control sends the end signal after decoding the order. It then performs the seek and, at the completion of the seek operation, sends an attention signal to the computer.

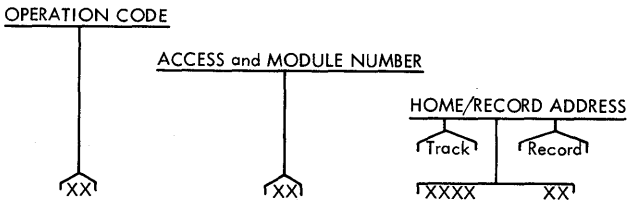


Figure 12. Order Format

Order	Mnemonic Code	Numeric Code
No Operation	DNOP	00
Release	DREL	04
Eight-Bit Mode	DEBM	08
Six-Bit Mode	DSBM	09
Seek	DSEK	80
Prepare to Verify, Single Record	DVSR	82
Prepare to Write, Format	DWRF	83
Prepare to Verify, Track with No Addresses	DVTN	84
Prepare to Verify, Cylinder Operation (Optional Feature)	DVCY	85
Prepare to Write Check	DWRC	86
Set Access Inoperative	DSAI	87
Prepare to Verify, Track with Addresses	DVTA	88
Prepare to Verify, Home Address	DVHA	89

Figure 13. Table of Orders

Orders requiring the two-digit operation code only are: no operation, release, six-bit mode, and eight-bit mode. The orders, with their mnemonic code and their numeric operation code, are shown in Figure 13.

Operation Signals

Signals are generated to provide a communication link between the file control and the computer. The signals generated to indicate that a specific condition exists, are:

Attention: Indicates that a previously given seek operation has successfully positioned the access mechanism at the specified location and selected the desired head.

End: Indicates the successful completion of an operation. This signal can indicate the successful transmission of an order to the file control or it can indicate the successful completion of a read or write operation.

Unusual End: Always indicates an unsuccessful operation. This signal can indicate that an error has been sensed during a read or write operation, or when any other check condition has occurred, or it might indicate that an unsuccessful attempt to transmit data has occurred.

Stop: Indicates that the computer has sensed the end of a read or write field.

Status Data

Status data are set in bit form for each read, write, and control operation performed by the file control and are available to the computer by means of the sense command. The status data should be called for by the computer before the initiation of the next read, write, or control command. (The initiation of the next command resets all error indications of the status data.) The attention bit for the addressed module is also reset.

The make-up of the status data transmitted to the data channel of the using system is shown in Figure 14.

Status character 0 summarizes the type of check or condition. Characters 1 and 2 give the type of check encountered during the operation and the mode of operation; character 3 gives the different unusual conditions; and characters 4, 5, and 6 give the attention indications. Characters 7, 8, and 9 are reserved.

Status Char	Bit No.	BCD Bit	Assignment	Comment
0	3	A	Reserved	
	5	4	Program Check	Summary
	6	2	Data Check	Byte
	7	1	Exceptional Condition	
1	3	A	Invalid Sequence	
	5	4	Invalid Code	Program
	6	2	Format Check	Check
	7	1	No Record Found	
2	3	A	Invalid Address	
	5	4	Response Check	Data Check
	6	2	Data Compare Check	
	7	1	Parity or Check Char Code Check	
3	3	A	Access Inoperative	
	5	4	Access Not Ready	Exceptional
	6	2	Disk Storage Circuit Check	Condition
	7	1	File Control Circuit Check	
4	3	A	Reserved	
	5	4	Six-Bit Mode	Data Mode
	6	2	Reserved	
	7	1	Reserved	
5	3	A	Module 0	
	5	4	Module 1 (Disk Only)	
	6	2	Module 2	Attention
	7	1	Module 3 (Disk Only)	
6	3	A	Module 4	
	5	4	Module 5 (Disk Only)	
	6	2	Module 6	Attention
	7	1	Module 7 (Disk Only)	
7	3	A	Module 8	
	5	4	Module 9 (Disk Only)	
	6	2	Reserved	Attention
	7	1	Reserved	
8,9			Reserved	

Figure 14. Status Data Bit Assignment

File Control Checks

The 7631 File Control checks for twelve individual error conditions that are possible in the operation of disk storage. The sensing of any one of these conditions causes an unusual end signal to be sent to the computer. Their position in the status word is shown in the Appendix.

Parity or Character Check: The 7631 is an odd-parity machine. As characters are transferred from the computer, the bit count of each is checked. If an even number is detected, this check bit, as well as the summary data check bit, will be set into the status data. The character code check is made by generating three check characters for each address and record as bits are read from the disk surface during a read operation. These newly generated characters are then compared bit by bit with those previously generated and recorded in the gap following each address and each record during the write operation. Failure to compare will indicate the occurrence of an error.

Response Check: The response check indicates that a character was not received by the 7631 within the allotted time. Response check can only occur as a result of a read or write operation.

Data Compare Check: Data compare check can occur only during a write check operation. The condition indicates that a compare error was detected somewhere during write check. During a write check operation data are read from the disk surface and compared bit by bit with those transferred from the computer.

Format Check: The format check occurs during either format write or a write check of a format track. The cause may be either an illegal code (any but a BCD 1, 2, 3, or 4) or because a stop signal was not sent to the file control prior to sensing the index point.

No Record Found: The no-record-found indication occurs if the file control fails to locate the track address that was issued to it on a prepare-to-verify order.

Invalid Sequence: The invalid sequence condition can occur during write operations in two ways, namely, when a write command is received by the file control without a preceding and properly executed prepare-to-verify or prepare-to-write format order. In the second case, invalid sequence occurs when a write check order is preceded by other than a prepare-to-verify order, prepare-to-write format order, and properly executed write command. When reading, a prepare-to-verify is the only legal order than can precede a read command.

Invalid Code: The invalid-code indication occurs when the file control is given an order that cannot be performed.

Access Inoperative: This indication occurs when the access mechanism fails to respond to a seek order. The access may be mechanically out of order or may not exist.

Access Not Ready: The access-not-ready indication shows that the addressed access is in motion from some prior seek order.

Disk Storage Circuit Check: This check indicates a circuit failure in the 1301 Disk Storage.

File Control Circuit Check: This check occurs due to malfunctioning of the gap detection circuit, address comparison circuit, or the check character code generator in the file control, the format skew detector circuit, or the basic timing rings of the 7631.

Invalid Address: Invalid address is set by an invalid configuration of bits sent to the 1301.

FUNCTIONAL DESCRIPTION OF LINES -- 7000 SERIES SYSTEM/7631

The lines are divided functionally into five groups. Generally speaking, any signal must be maintained until its response is provided by the receiving unit. See Figure 15.

Initiation of Operation (Five Lines)

The operation is initiated by one of the four commands, namely read, write, control, and sense and their common response (command response). Both read and sense commands establish transfer of information from the 7631 to the computer. Read is associated with the transfer of data while sense is associated with the transfer of status of the 7631. Both write and control commands establish transfer of information from the computer to the 7631. Write is associated with transfer of data while control is associated with the transfer of housekeeping orders to the 7631. Commands are sequentially executed over the interface. An operation associated with any of the four commands must be properly terminated prior to issuance of the next command.

Information Transfer (20 Lines)

Information is transmitted over the read bus and the write bus on the demand and response basis. Demand is indicated by service request and response by service response. Information is transferred parallel by byte. The byte may be up to eight data bits in size.

Termination of Operation (Four Lines)

An operation may be terminated by either the computer or the 7631. The computer accomplishes this by the stop signal. The 7631 indicates successful completion with end signal and abnormal completion by unusual end signal. In either case the computer responds with end response. The cause of unusual end may be determined by analysis of the status information obtained by means of a subsequent sense command.

Asynchronous Signaling (Two Lines)

The 7631 can present an asynchronous signal to the computer by means of an attention signal. An attention signal indicates to the computer that a change in status in the 7631 has occurred which requires attention. This signal may come at any time whether or not one of the command operations is in process. The computer signals to the 7631 the recognition of attention by sending attention response.

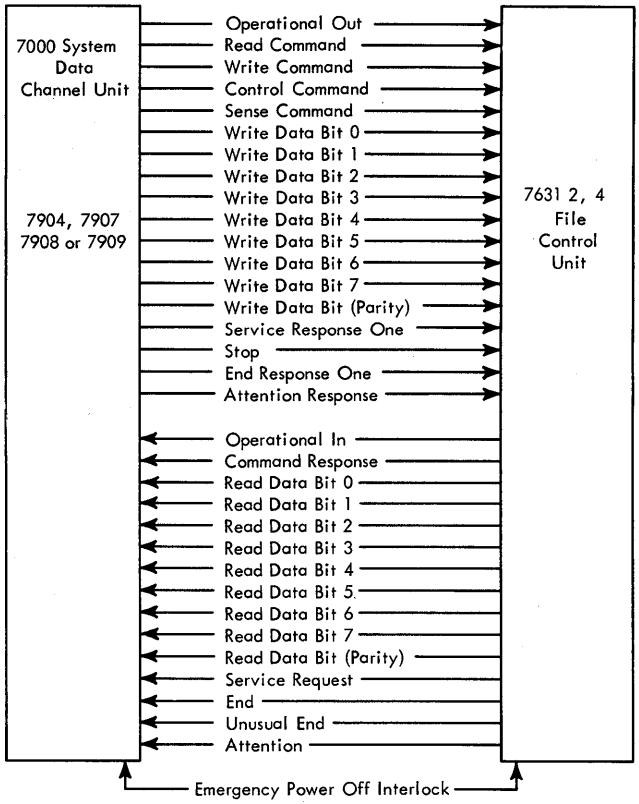


Figure 15. Operating Lines - IBM 7000 Series Data Processing Systems to/from IBM 7631-2 and 4

Interlocks (Two Lines) -- Non Power

In addition to the logical interlocks (signal and response) mentioned above, the computer and 7631 are interlocked by means of operational-in and operational-out. Each line reflects the operational state of the unit at its driver end.

ORGANIZATION OF INFORMATION

Information on the read bus and the write bus is arranged so that bit position 0 of a bus always carries the highest order bit, with bits in descending order being assigned to bit positions of the bus string in the computer or 7631, the bit-from-bit position 0 of a byte always adjoins the bit-from bit position 7 of the preceding byte. As a result, a message consisting of several bytes always appears as bus bit positions 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2, etc.

When a byte is transmitted over the connecting lines that consists of less than eight bits, the bits must be placed in the highest-numbered continuous bit positions of the bus. Thus, when a computer or 7631 transmits only the six bits of the BCD code over the lines, bit B is placed in bit position 2 of the bus, bit A in bit position 3, etc., and bit 1 is placed in position 7. When the computer or 7631 places information on or receives information from only four lines of a bus, it must use bit positions 4, 5, 6, and 7. Any unused lines of the read or write bus must include the low-numbered bit positions of the bus, i.e., bit position 0 and bit positions adjacent to it. The parity bit of any byte must always appear in the parity bit position. Unused lines must always present logical zeros to the receiving end.

DESCRIPTION OF SIGNAL LINES FROM COMPUTER TO 7631

Operational Out

The operational out line is used for interlocking purposes. The lines from the computer are significant only when the operational out line is up.

The down-state of the operational out signal is used to reset the 7631. Any down-state of sufficient duration to cause a response from the terminator circuit provides the reset. The meaning of the reset is defined by the 7631. To insure a proper reset, the operational out line must remain down for at least 6 usec.

READ COMMAND

The read command line is used to signal the 7631 to cause the next block to be read into the computer. The read command signal, as well as all other command signals, is loop checked by the command response line.

The read command signal must not be initiated unless command response is down, and unless stop and end response are either down or are dropped at the time read command is raised. The read command signal must remain up until the rise of command response. It must fall before the rise of end response.

Write Command

The write command line is used to signal the 7631 to proceed with writing a block of data. Loop checking and signal timing specifications are the same as for read command.

Control Command

The control command line is used to signal the 7631 that it must accept information from the computer over the write bus and must perform the operation encoded in this information. Examples are: seek, prepare to write format, etc. Loop checking and signal timing specifications are the same as the read command.

Sense Command

The sense command line is used to signal the 1301 to send status information to the computer over the read bus. The information sent depends on the definition of the sense data word. Loop checking and signal timing specifications are the same as for read command.

Write Bus

The write bus is used for sending both data and control information to the 7631. It consists of nine lines -- eight data lines plus one line for odd parity. Not all of these lines need be used.

Data must be valid on the write bus from the rise of service response until the fall of service request.

The assignment of bit positions on the nine lines on the write bus is as follows:

Line Name	Assignment A	Assignment B	
Parity Bit	Bit C - BCD	Parity	
Bus Bit Position 0	Unused - BCD	Bit 8	
Bus Bit Position 1	Word Mark	Bit 4	First
Bus Bit Position 2	Bit B - BCD	Bit 2	Numeric
Bus Bit Position 3	Bit A - BCD	Bit 1	Character
Bus Bit Position 4	Bit 8 - BCD	Bit 8	
Bus Bit Position 5	Bit 4 - BCD	Bit 4	Second
Bus Bit Position 6	Bit 2 - BCD	Bit 2	Numeric
Bus Bit Position 7	Bit 1 - BCD	Bit 1	Character

Service Response

The service response line is used to signal the 7631 in recognition of a signal on the service request line. Service response indicates to the 7631 that the computer is transmitting or has received information on the data busses.

During write and control operations, the rise of service response indicates that data is available on the write bus. The rise of service response is delayed sufficiently to insure that it does not precede data when measured at the cable connectors at the computer under worst-case skew conditions. Skew that is caused within cables and 7631 circuitry is accommodated by the 7631. Within the above skew

limitations, data must be valid from the rise of service response until the fall of service request. During read and sense operations, service response must rise when the computer has accepted the information on the read bus.

The service response signal must rise before the fall of service request. In the case of cyclic devices, service response must rise before the fall of service request by a time period specified by the 7631. If service response rises too late, the 7631 recognizes the overrun condition.

The service response signal must remain up until the fall of service request. It falls after the fall of service request.

Stop

The stop line is used to signal the 7631 that the computer has recognized the end of a record or operation. If the 7631 recognizes the end of operation first and generates an end or unusual end signal, no stop signal occurs.

Upon receipt of the stop signal, the 7631 proceeds to its normal ending point. No further service request is sent and no further service response is expected. To complete the ending procedure, the 7631 sends an end or unusual end signal at the proper time and receives in return an end response from the computer.

The stop signal may rise any time when the command response line is up except when both service request and service response lines are also up. If stop is issued when service request is up, it replaces service response, in which case read and sense operations data on the read bus is not accepted.

The stop signal must remain up until the fall of command response. It must fall when or before a new command signal is sent to the 7631.

End Response

The end response line is used to signal the 7631 in recognition of a signal on the end or unusual end lines. The end response signal restores the 7631 to the conditions necessary for accepting a new command.

The end response signal must remain up until the fall of both command response and end or unusual end. It must fall when or before a new command signal is sent to the 7631.

Attention Response

The attention response line is used to signal the 7631 in recognition of a signal on the attention line. The attention response signal causes the fall of the attention line.

The attention response signal must remain up until the fall of attention and must fall after the fall of attention.

DESCRIPTION OF SIGNAL LINES FROM 7631 TO COMPUTER

Operational In

The operational in line is used for interlocking purposes. During operation the lines from the 7631 are significant only when the operational in line is up. When the operational in line is down, the 7631 normally will not respond to any signal from the computer.

Read Bus

The read bus is used for sending both data and sense information to the computer. It consists of nine lines -- eight data lines plus one line for odd parity. All of these lines need not be used.

Data must be valid on the read bus from the rise of service request until the rise of service response.

The assignment of bit positions on the nine lines of the read bus is the same as on the write bus.

Command Response

The command response line is used to signal the computer in recognition of a signal on any of the four command lines. It indicates the ability of the 7631 to initiate the command.

The command response signal will rise within 6 usec of the rise of any of the four commands. If, because of skew, stop or end response from the preceding operation overlap the command, command response cannot rise until stop and end response are down and it will not fall during the execution of the command. It will fall within 6 usec of the rise of end response.

Service Request

The service request line is used to signal the computer when the 7631 wants to transmit or receive a byte of information.

During read and sense operations, service request rises when information is available on the read bus and service response is down. The rise of service request must be delayed to guarantee that it does not precede data when measured at the cable connectors at the computer under worst-case skew conditions. Skew that is caused within computer circuitry must be accommodated by the computer. Within the above skew limitations, data must be valid

until the rise of service response. During write and control operations, service request rises when or before information is required on the write bus and service response is down.

The service request signal must fall after the rise of service response. During read and sense operations, service request must fall within 6 usec of the rise of service response.

When the next cycle time is reached, in the case of cyclic devices, and service response has not occurred, the 7631 must drop service request and must recognize an overrun condition. The minimum interval between the rise of service response and the fall of service request is part of the 7631 specifications.

End

The end line is used to signal the computer that the 7631 has recognized the normal ending of an operation. If any abnormality such as data check, program check, end of file, or cancel condition has occurred, the end signal is not used and an unusual end signal is given instead.

The end signal cannot rise until service response for the last service request has been received. The end line must stay up until end response is received from the computer. It must fall within 6 usec of the rise of end response.

The 7631 gives an end signal after every normal operation. The computer may or may not have previously given a stop signal. In any case, the computer gives an end response signal after receiving an end signal from the 7631.

Unusual End

The unusual end line is used to signal the computer that the operation being executed has resulted in an unusual condition and has been terminated. This signal is a summary of all unusual conditions such as data check, program check, end of file, out of material, or cancel. If an unusual end signal occurs, the end signal is not given. The computer therefore sees end or unusual end, but not both.

The unusual end signal must stay up until end response is received from the computer. It must fall within 6 usec of the rise of end response. No further service request may be sent after unusual end rises.

The computer may or may not have given a stop signal before the 7631 signals unusual end. In any case, the computer gives an end response after receiving an unusual end signal from the 7631.

Attention

The attention line is used to signal the computer that an access mechanism has come to rest.

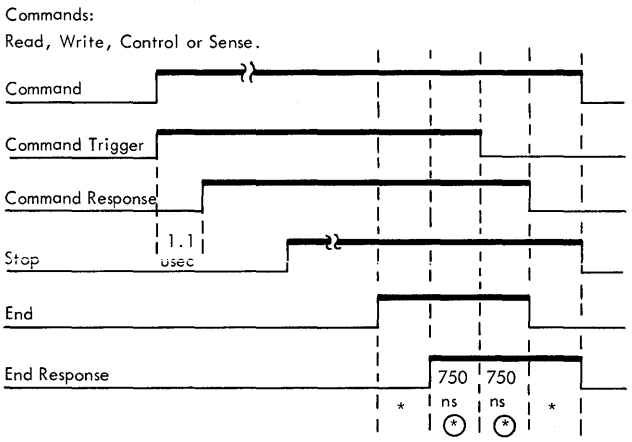
The attention signal can rise at any time except when attention response is up. It must stay up until the 7631 receives an attention response from the computer. Attention must fall within 6 usec of the rise of attention response.

Turning off the attention signal generally does not reset the conditions which caused the indication. The conditions are available for transmission to the computer on a sense command.

TIMING OF LINES -- 7631 IN 7000 SERIES OPERATION

Commands

Read, Write, Control or Sense:



⊛ Timings shown are maximum. They are measured from the time a signal rises on the interface cable until the 7631 brings up its responding signal on the interface cable.

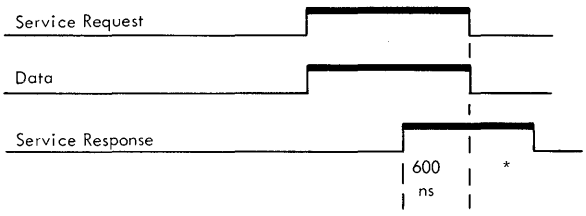
* Timings are a Computer function. The length of these timings has no effect on 7631 operation.

1. Get command from computer.
2. Command will not be initiated unless command response, end, and stop are down.
3. Command response will rise no later than 1.1 microseconds after the command is initiated.
4. If stop is issued, the 7631 will proceed to its normal ending point.
5. The rise of end causes the 7631 to detach itself from the I-O device and signals end to the computer.
6. The rise of end response causes the command to be reset.
7. Command going down causes command response and end to be reset.
8. The fall of end should cause end response and stop to fall.

Service request and response:

1. Service response must be down for service request to rise.
2. Service response is the system acknowledgment of service request.
3. Service request falling causes service response to fall.
4. A service response must rise within 7.3 microseconds after the rise of service request or an overrun condition will be indicated.
5. Timings shown are maximum.

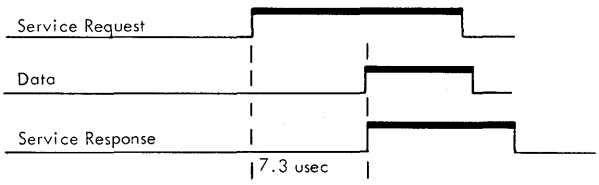
Read or Sense:



* Timing is a computer function.

1. Service request rises when data is available on the bus.
2. Rise of service response indicates that data has been accepted by the computer.
3. Service response rising causes service request to fall.

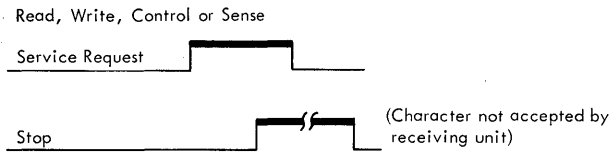
Write or Control:



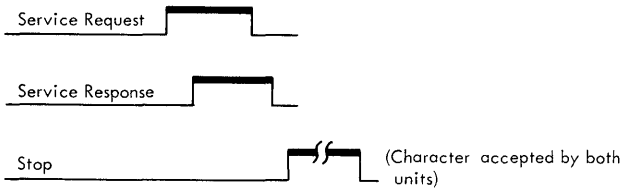
1. Service request rises when data is requested in the 7631.
2. Rise of service response indicates data is available on the bus.

Stop

Read, Write, Control or Sense:

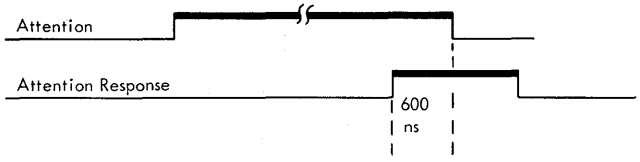


1. Stop is issued when service request is up.



1. Stop is issued when both service request and service response are down.

Attention



Timings shown are maximum.

1. Attention may rise any time except when attention response is up.
2. Attention holds up until attention response rises.

OPERATIONAL CHARACTERISTICS

Data handling (reading and writing) can be handled in five different modes:

Home Address Operation: Comparing the physical home address (HA1) followed by transfer of the home address identifier (HA2) plus all addresses and records on a given track.

Single Record Operation: Comparing a record address followed by transfer of the associated single record only.

Track Operation: Comparing the entire home address (HA1 and HA2) followed by transfer of all record addresses and records on a single track.

Track Without Addresses: Comparing the entire home address requested, followed by transfer of all records contained in the remainder of the track.

Cylinder Operation: Optional feature -- comparing the entire home address of a particular track in a cylinder followed by transfer of all records contained in that track and all succeeding tracks of higher address within that cylinder.

CONTROL COMMANDS

The 7631 File Control executes thirteen particular orders under the control command. The orders, standardized at a common length of either ten or two digits, are transmitted to the file control over the write bus in response to service requests by the file control. The first two command digits comprise the operation code and the remaining digits provide the necessary address information. Six-bit mode, eight-bit mode, no-op and release are orders which require no address information and consequently are of two digits in length. The remaining orders demand ten digits. The file control decodes the command, accepts the address information, performs the designated function, and transmits an end signal to the processing system upon completion.

During execution of the control function, the file control performs various checking operations. It performs a parity check on op codes and address information, confirms that a valid op code has been accepted, and verifies disk storage ready and operative lines. If any check conditions are present, the control operation is immediately terminated and an unusual end signal is sent to the using system.

Seek (DSEK)

The seek order transmitted to the file control includes the address of the access unit and cylinder-head location to which the access is to be moved. The file control selects the particular access mechanism, encodes the cylinder-head digits into the file's track and head code and sends the address to the 1301. An end signal is then issued and the file control is available for further operations while the access moves to the requested address.

The end of the seek order does not signify that the access has reached its proper position nor that it necessarily will, as there is a possibility of the file going to memory address. It means only that the file control has sent an address to the selected access and that no error conditions were encountered.

Set Access Inoperative (DSAI)

This order is sent to the file control accompanied by the address of a particular access mechanism. The file control sets the inoperative relay in the access and issues a normal end signal to the system. The set access inoperative signal from the adapter to the 1301 Disk Storage will be issued regardless of the level of the ready line.

Prepare to Verify Orders

The PV order specifies the manner in which a subsequent read or write command is to be performed, provides an address for subsequent verification, selects the desired module and access and, with the exception of DVSR, selects the addressed head. An end signal indicates that the PV order and associated address have been accepted by the file control and that no check conditions have been encountered. The read or write which follows a PV order initiates a search for the particular record address.

Prepare to Verify -- Single Record Operation: The DVSR order prepares the file control to read or write one particular record in a track. The record address is supplied for subsequent verification. The head that is selected for the DVSR was determined during a previous seek or PV order.

Prepare to Verify Track Operation (DVTA): The DVTA order prepares the file control to read or write record addresses and records on a particular track. The home address of the track is supplied for subsequent verification.

Prepare to Verify Track Without Addresses (DVTN): The DVTN order prepares the file control to read or write only records on a particular track. The home address of the track is supplied for subsequent verification.

Prepare to Verify -- Cylinder (DVCY): The DVCY order prepares the file control to read or write only records in a particular cylinder. The home address of the track within the cylinder at which it is desired to start the operation is supplied for subsequent verification.

Prepare to Verify Home Address Operation (DVHA): The DVHA order prepares the file control to read or write an entire track of data and addresses including the home address identifier. The physical track and head address must be supplied for subsequent verification. For execution of the DVHA order the HAO switch must be on. If this switch has not been activated the DVHA order is not decoded and an invalid code check condition is issued. If the HAO CE switch is on during DVHA the ninth digit of this control order is scanned for flag information and on the succeeding write or read a flag surface is selected if flag bits have been found. The HAO CE switch removes the address compare cycle.

Prepare to Write Format (DWRF): The DWRF order sets up format writing. The address used for verification when writing a format track must be the physical address of any track located in the cylinder to be formatted. For execution of the DWRF order the format switch must be on. To write the format on a virgin file, which contains no physical addresses, the HAO CE switch may be activated, which will bypass address verification.

Prepare to Write Check (DWRC): The prepare to write check order is issued to the 7631 prior to checking a written format or data area. The write check operation is performed in the 7631 by requesting information from the system while reading information from the disks and comparing the two streams of data in a bit-by-bit fashion.

The normal sequence of commands involving a write check could be prepare to verify, write, prepare to write check, and write. The 7631 retains the mode used by the previous write operation and applies it to the second write. For example, a DVSR write sequence would be followed by a prepare to write check and write command. The 7631 retains the necessary SRO condition from the DVSR order and executes write check in that mode.

The write check requires an address that must agree with the address that was issued on the previous prepare to verify. The same information should also be provided during the write check operation that was transferred on the original write.

During the actual check of the format, the 7631 performs a check on its format gap detector circuits to insure that they are kept within specified tolerances. A gap detector failure will cause the file adapter circuit check to be set.

A write check on a home address operation requires the HA switch be on.

The write check order ends when the op code and the address have been successfully loaded into the 7631. Execution of the operation occurs when the following write command is issued.

Six-Bit Mode

This order causes the 7631 to operate in six-bit mode. The character rate of the file control is determined by the character rate of the attached storage unit with a maximum rate of 110 KC.

Eight-Bit Mode

This order causes the file control to operate in eight-bit mode.

No-Op

The no-op order is accepted by the 7631 as a programming convenience. No function is performed by the file control under a no-op order.

Release

The release order has meaning only on the 7631 Models 3 and 4. The order causes the 7631 to make both of its channel interfaces assume an available status.

SENSE

The sense command is used to bring status information from the adapter to the system. The status word contains ten four-bit bytes of error and attention status information. The first four bytes contain error status information. The first byte is the summary byte. The succeeding three bytes represent particular error conditions that occurred on the instruction immediately preceding the sense operation. The fifth byte contains a bit designating data mode and bits reserved for future optional features. The last five bytes indicate those accesses which were ordered to seek and have come to rest but have not yet been utilized in a subsequent command. A chart of the status word and its sequence of transmission is given in the

Appendix. An end signal is issued after transmission to the system of the last status byte.

ATTENTION

The attention signal from the file control to the system is activated when an attention status sign signal is received from a particular access. Attention remains up until attention response is transmitted from the system. If several seek orders are issued by the system, attention will be sent from the file control each time one of the accesses comes to rest, provided each attention is recognized by an attention response before the subsequent attention condition arises. The system can determine the access responsible for the attention signal by analysis of the status word (see Appendix) received in answer to a sense command. In Model 4 attention is transmitted to both systems regardless of availability status.

WRITE

A write command must always have been preceded by a prepare-to-verify order. A write that is not preceded by a PV order will be terminated by an unusual end signal with no transmission of data.

Format Write Operation

The necessary steps for format write operation are: the format switch must be on, a prepare-to-write format order must be received by the file control and normally terminated, and a write command must be subsequently received.

During the format write operation the 7631 will legally accept only four different characters, namely, BCD 1, BCD 2, BCD 3, and BCD 4. Respectively, the four characters cause the 7631 to write on the format track a seven-bit character of all ones, a seven-bit character of all zeros, a nine-bit character of all ones, and a nine-bit character of all zeros. These characters are used to construct a format as shown in the Appendix, Figure 27. The figure shows the reference timing from which the 7631 operates. The format track that is given as an example would result in a data track such as that shown at the bottom of the illustration.

The format areas A, B, C, D, E, F, and G are uniquely associated with the home address that is recorded at the start of each data track. The areas H, J, K, L are associated with the record address. The areas M, N, P, and Q are associated with the data. The areas A, B, C, D, E, associated with home address, must be written using the BCD 3 and BCD 4 characters.

Format areas that are associated with the record portion of the home address, as well as those associated with record addresses (i.e., H, J, K, L) and with data (i.e., M, N, P, Q) are written using the appropriate six-bit or eight-bit data characters that agree with the six- or eight-bit mode in which the data is to be written.

Prior to area A the file control automatically generates a burst of ones between early and late index marks. The burst of ones is written to set the sensitivity of the format read amplifier on any ensuing read or write.

Each of the format track writing areas is described below:

Area A: Three characters mandatory length. The BCD 4 character must be used for causing it to be written.

Area B: Length of nine characters. The BCD 3 character must be used for writing the area. The length permits the four-character physical address portion of the home address and its flag bits to be written. Only the physical address portion of the home address is used for verification on a subsequent home address or format operation.

Area C: Must be one character long. BCD 4 is the one character used to write this area.

Area D: Mandatory length of ten characters of ones; must be written by means of the BCD 3 character.

Area E: Must be one character of zeros. The system must send a BCD 4 to the 7631 to have it written.

Area F: Minimum length of six characters. Either the BCD 1 or BCD 3 is used for this area depending on the desired bit mode for the particular data tracks. This area permits the home address identifier to be written. The minimum home address identifier must contain two characters. For word-oriented systems, the length of the home address can be increased to any value. The physical address portion and the first two characters of the record portion of the home address are compared for a track operation or cylinder operation. Any further characters in the home address are ignored internally by the 7631. However, on a read home address operation, the 7631 will return all of the home address characters to the system in their original order and form.

Area G: Mandatory length of twelve characters. Either the BCD 2 or BCD 4 should be used to write this area. The length of this area is dictated by a combination of file control and disk storage

considerations. The file control considerations are that the actual last character of the home address that is written is placed two characters beyond the finish of the format home address area. The cyclic check characters for the home address are placed beyond the last character of home address and demand four characters of space.

Area H: Minimum length of ten characters. Either the BCD 1 or BCD 3 is used for writing this area. Area H can be varied in length in the same manner as area F to achieve record addresses of a convenient word size. To cause an RA length of n characters, area H should be n + 4 characters long.

Area J: Must be one character long. Either the BCD 2 or BCD 4 should be used to write this area.

Area K: Mandatory length of ten characters of ones; should be written by means of either the BCD 1 or BCD 3 character.

Area L: Must be one character of zeros. The system should send either a BCD 2 or BCD 4 to the 7631 to have it written.

Area M: Minimum length of six characters. The length of M is determined from the length of the record that is to be recorded under the control of M. For a record of two characters long, M is equal to 2 +4 characters. Either the BCD 1 or the BCD 3 may be used for recording area M depending on whether six-bit or eight-bit characters are to be recorded in the corresponding record areas of the data tracks. All of the records in a cylinder can be either in six-bit mode or in eight-bit mode but not in a mixture of the two modes.

Area N: Mandatory length of twelve characters; must be written with either the BCD 2 or BCD 4. The BCD 2 should be used if all records of the cylinder are to be recorded in six-bit mode. The BCD 4 is used where the cylinder is assigned for eight-bit data.

Area P: Must be only one character in length. The area may be written using either the BCD 2 or BCD 4. The area N can be seen after the first record area in Figure 15. If a track is to have multiple records each record is followed by an area N except the last record which is followed by a single character of zeros and then the filler characters.

Area Q: Minimum length of eleven characters. This area is written under the internal control of the 7631. The control is passed over to the 7631 from the program by use of the stop signal from the computer. After receiving the stop signal, the 7631 writes one bits until it senses the early index signal, after which it continues writing for three more characters. The 7631 checks the filler area to assure that the length is equal to or greater than the minimum length. A format check indication results if the filler does not cover sufficient space.

Write Home Address Operation

The conditions necessary for a WR-HAO are: the HAO switch must be on, a prepare-to-verify home address operation order must be issued to the file control, and the write command must follow. The file control compares the physical address portion of the home address on the particular track and begins the write operation at the beginning of the HA 2 area. At that time, under internal control, the file control writes five bytes of AGC ones followed by one byte of zeros and then begins to request bytes from the processor. The first byte must be the home address identifier of the particular track. The home address identifier must be a minimum of two characters. If desired, this area may be formatted to match the word length of the processor. The number of bytes requested by the 7631 for the HA identifier is determined by the number of ones that were previously written on the format. All characters of the HA identifier after the second are non-significant and will not be a part of address compare.

WR-HAO continues with the file control detecting the gap between the HA2 and the first record address. On detection of the gap, the file control ceases service requesting, completes recording of characters already requested, and writes the three-digit check character.

At the record address, five bytes of AGC ones are automatically written, followed by a gap of zeros. Record address bytes are now requested from the processor and written in the record address area. The gap of zeros following the record address area signals the end of the record address area. The file control detects ensuing gaps, writes AGC bits, and obtains data from the processor in all record address areas and record areas. While writing address and record areas the file control simultaneously generates a check character to be placed at the end of each area. This check character is a cyclic code for error detection. Its detection capabilities are explained under checking section. One character beyond the check character of the last record on a track, the file control initiates a burst of ones which are written until WR-HAO is terminated when the file control senses index. At this time the file control issues a normal end signal if no errors have

occurred during the operation, or an unusual end signal if a data check error has been detected.

If a stop signal is issued by the processor during a WR-HAO operation, the file control continues processing any data already received, fills in the rest of the record area in which it was writing with blanks, generates the check character, and fills with blanks any formatted address or record areas remaining on the track. End is signalled at the normal termination time of the operation.

For all other write operations, if a stop is issued the file control continues processing any data already received, fills in the rest of the record area in which it was writing with blanks, generates the check character, and then issues a normal end.

If the HAO CE switch is on during a WR-HAO operation, address verification is bypassed and the 7631 begins writing AGC bits at the early index point until one character before the actual recording of the physical home address. At this time, the file control begins to request bytes from the processor. The first five bytes shall constitute the physical home address and flag byte. On detecting the gap following HA1, the file control ceases service requesting, completes recording of characters already requested, and writes the three-digit check character. The remainder of the operation is identical with normal WR-HAO operation.

Write Track Operation

Conditions necessary for a WR-TRO are a DVTA order followed by write. Under control of the DVTA the file control searches the data track for a home address and compares this address, bit by bit, against the address that was previously issued with the DVTA command. If the home address fails to compare, the file control issues an immediate unusual end signal and indicates in its status word a no-record-found bit. Upon a successful home address compare the file control will cause the write amplifier to be activated in the 1301 prior to the first record address area and will write the first AGC ones which must precede the record address.

Transfer of record address proceeds in the usual service request-service response manner. The file control continues writing the AGC prior to each information area, filling the information area with data requested from the computer, which includes both records and addresses. The file control also supplies the check characters to be written at the end of each area. When the last check character area is reached, a normal end signal will be issued to the processor providing no error conditions have been detected. Otherwise, unusual end results.

Write Single Track Operation

Conditions necessary for the WR-SRO are that a prepare-to-verify-single-record operation order be issued to the file control and that a write command follow. On a single record operation, the file control squelches the AGC voltage in the file frame, then permits the read amplifiers sufficient time to regain proper sensitivity. The record address area is recognized in the file control by sensing the end of a long gap in the format. Upon finding a record address area, the file control reads off the address contained in the area and compares it bit by bit with the address previously supplied to the adapter during DVSR. If the address does not compare, the file control continues searching succeeding address areas and comparing the address contained in each. If the file control passes the index point twice without comparing the address, and no flag bits are sensed, it will register the no-record-found status bit and issue an unusual end signal to the processor without transmission of data. Upon an address compare true, the file control will cause the 1301 to write over the record immediately following the compared address. Data is furnished by the system in response to a series of service requests. The file control automatically transmits the cyclic code check characters at the end of the record area as defined by the format track.

If a stop signal is received at a midpoint in the record area, the file control will continue to write the record, writing blanks (with sync bits) until the end of the formatted area is reached. After the check character is recorded, a normal end signal is issued to the system unless a data check has occurred, in which case, unusual end would result.

Write Track Without Addresses

The conditions necessary for a WR-TWA are that a DVTN order be followed by a write command. The address received with the DVTN order is compared with the home address transmitted from the 1301. If the home address fails to compare, the no-record-found bit is registered and an unusual end signal is issued to the system. If address compares true, the file control skips over the first address area into the record area and writes the record. The file control continues skipping addresses and writing the records until the end of the last record area is sensed. A normal end signal is issued to the system providing no error conditions occur during data transfer. In the event of a parity error, the operation will be terminated at the end of the record in which the error was detected and unusual end issued. This condition also holds true for CYO operation.

Write Cylinder

Operation in the cylinder mode is an optional feature of the 7631. A cylinder mode write is set up by having the processor send a prepare-to-verify cylinder operation order to the file control. The address issued with the order is the home address of the track on which the operation is to start. The home address is compared bit by bit in the 7631 after the write is received.

On a compare equal, the data transfer operation begins with all of the records on the addressed track being written and with the record addresses ignored in the same manner as a track-without-addresses operation. However, rather than causing an end signal when the last record of the track has been processed, the 7631 sends a new head address to the 1301 and writing continues. The head address sent to the 1301 is one address higher than the previous head address. By indexing one head address on each disk revolution the 7631 continues writing until the cylinder of information has been processed. The end signal is generated in the 7631 when the highest-order head of the cylinder has been operated on. No wrap-around feature is included in CYO to cause operation to begin again at the low-order head after the high-order head has completed its writing.

NOTE: On all the write operations that have been described, it has been assumed that a previous seek control order has selected the proper cylinder.

Write Check Operation

Each of the write operations has a companion write check operation which is optional and under program control. The operation requires that a write check order be preceded by a successful PV-write sequence and followed by a write command. The file control will compare the data recorded in the addressed record bit by bit with the write data from the system. End of WR-CKO is the same as in a true write. A compare error during write check will set the data compare check bit.

During a write check operation on a format track the format gap detector circuits in the 7631 are checked to determine whether or not they are within their specified tolerance. A file adapter circuit check is noted if the circuits do not meet specifications.

On receiving a stop signal the file control continues comparing data already received, and then continues until end-of-the-present-record area and issues a normal end signal. The stop signal must be issued at the same time with respect to the data field as in the preceding write instruction.

Flag Byte

A flag byte is set up by a customer engineer when it is determined that a track is unusable for data recording. The three low-order bits of the flag byte are used to designate one of the six spare disk surfaces provided for alternate usage. The flag byte is located in the fifth character position of the physical address portion of the home address. Upon sensing these bits during an address compare operation (record search part of read or write), the file control automatically transfers the new head address (that of the spare surface) to the file, and execution of read or write proceeds without any reference to program.

Table of Flag Codes

B5	B6	B7	Flag Surface
0	0	1	1
0	1	0	2
1	0	0	3
1	0	1	4
1	1	0	5
1	1	1	6

READ

Read Home Address Operation

The RD-HAO requires that a DVHA order be issued to the file control and that a read command follow. The RD-HAO is analogous to the WR-HAO. The most useful application of the RD-HAO is to recover tracks of information after a major mechanical change involving disk restacking and actuator replacement. The RD-HAO does not depend on the format track for recognition of data and address areas. With this operation and assuming that a proper gap is provided between late index and the beginning of the home address area, the processor can restore a file to normal operation after a major mechanical change. The file control compares the physical address portion of the home address and begins reading with the home address identifier. All address and record data of the track are read. The termination of the RD-HAO occurs when the adapter senses the early index. At that time either a normal or unusual end signal is issued, depending on the state of the data check. The processor may terminate the operation earlier by issuing a stop. Upon receipt of stop, the file control will terminate data transmission and internally complete reading of the record on which it was operating at the time of the stop. At the end of the particular record, the file control will send either a normal or unusual end signal, depending on the state of data check.

If the HAO-CE switch is on during RD-HAO, address verification is bypassed and reading begins with the physical home address.

Read Track Operation

Conditions necessary for the RD-TRO operation are that a DVTA order be issued to the file control followed by a read command. The file control begins the operation by comparing the home address which accompanied the DVTA order against the recorded home address on the selected track. A failure to compare will cause no record found to be set in the status word and causes an unusual end signal to be issued to the system. A successful compare permits the file control to begin reading at the first record address area. The record address is read out in its entirety and sent to the system followed by the record and then the next address and record, etc. The operation terminates when the file control senses that it has completed comparing the check characters of the last record of a track. Normal end or unusual end is contingent upon the state of data check. A stop signal prior to the logical end of DVTA will cause the file control to stop data transmission and to transmit an end signal at the end of the record on which it is operating at the moment.

Read Single Record Operation

The read SRO requires the completion of a DVSR order and read command. As with write SRO, the read SRO has no predetermined starting point on the disk; that is, when the instruction is received by the adapter it squelches and sets the AGC voltages in the file and immediately begins searching for a record address. Upon finding one, the adapter does a bit-by-bit address comparison. A failure to compare causes the adapter to continue searching on the next record address. No record found is registered if the adapter passes the early index point twice in its search for a particular record. Upon obtaining an address compare true the adapter causes the record immediately following that address to be read and the data to be sent to the system. The adapter verifies the legality of the check character at the end of the record and sends the normal or unusual end signal at that time. A stop signal prior to the logical end of DVSR will cause the file control to stop data transmission and to transmit an end signal at the end of the record.

Read Track Without Addresses

The read TWA operation requires that a DVTN and a read instruction, in that order, be executed. The file control waits for the home address area before beginning to compare the address supplied with the prepare-to-verify order against the recorded home address. A compare failure causes the file control to register no record found in the status word. If the address compares successfully, the file control carries out the read TWA operation by skipping over the first record address and reading the first record. The operation continues with addresses ignored by the file control and only record data being sent to the system. The operation ends when the 7631 finishes the last record of the track, at which time the appropriate end signal is issued. An early end signal may occur due to system stop signal or the occurrence of a data check. In that case, the adapter finishes the record on which it is operating and issues a normal or unusual end signal as the case may be. This condition also holds true for CYO.

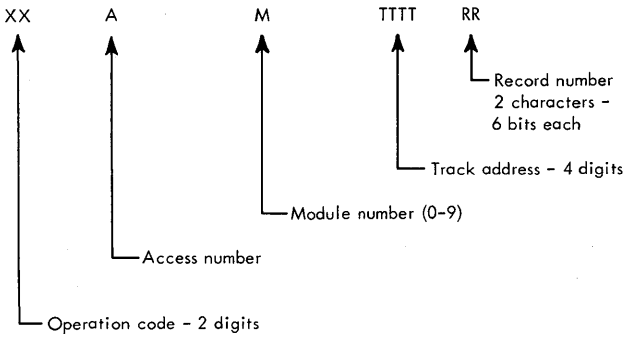
Read Cylinder Operation

A cylinder mode read is set up by having the processor send a prepare-to-verify cylinder operation order to the file control. The address issued with the order is the home address of the track on which the operation is to start. The home address is compared bit by bit in the 7631 after the read is received.

On a compare equal, the data transfer operation begins with all of the records on the addressed track being read and with the record addresses ignored in the same manner as in track-without-addresses operation. However, rather than causing an end signal when the last record of the track has been processed, the 7631 sends a new head address to the 1301 and reading continues. The head address sent to the 1301 is one address higher than the previous head address. By indexing one head address on each disk revolution the 7631 continues reading until the cylinder of information has been processed. The end signal is generated in the 7631 when the highest-order head of the cylinder has been operated on.

ADDRESS COMPARING

In general, an address in the 7631 is composed of six numeric digits followed by two alpha-numeric six-bit characters. For a control command, the 7631 receives two digits which define the order (or operation code) followed by the above mentioned address. The control order format follows:



Access (A) and module (M) digits are decoded in the 7631 and the decoded outputs select a particular access control in the disk storage. Access-module combinations which interrogate non-existent address locations result in an access-inoperative indication. This occurs since the 7631 can not differentiate between an access with its power off and a completely non-existent access location. During an address compare the access-module digits are not a part of the comparison. Bit-by-bit comparison is made on the remaining digits of the address. On the four track digits only the numeric portion of the digit is compared. The zone bits do not enter into the comparison. In a record address the four track digits need not reflect physical track locations. However, in a home address the track number recorded must agree completely with physical location. The last two characters of the address are alpha-numeric and not limited to purely numerics as in the case of track digits. The 7631 compares both the numeric and the zone portions of the record identifiers. The home-address-identifier characters are useful in some program applications, particularly for multiprogramming.

INSTRUCTION TIMES

Ten-digit control orders require 148 microseconds in six-bit mode and 190 microseconds in eight-bit mode. Two-digit control orders demand 55 microseconds in six-bit mode and 75 microseconds in eight-bit mode. A sense command requires 123 microseconds in six-bit mode and 158 microseconds in eight-bit mode.

Read and write commands vary in time duration depending on the length of record (for single-record operations) and rotational coincidence of starting points. A cylinder operation involving all 40 tracks within a cylinder will take 1.353 seconds, providing no tracks are flagged. Flagging could add a maximum of .396 seconds.

Service requests to the computer will occur cyclicly at a minimum average period of 11.1 microseconds in six-bit mode and 14.2 microseconds in eight-bit mode. However, the minimum time between any two characters can be 10.7 microseconds in six-bit mode and 13.8 microseconds in eight-bit mode.

FUNCTIONAL DESCRIPTION OF LINES -- 1410 SYSTEM TO IBM 7631

The lines are divided functionally into four groups: control lines, operation code bus lines, data lines, and status condition lines. See Figure 16.

Control Lines

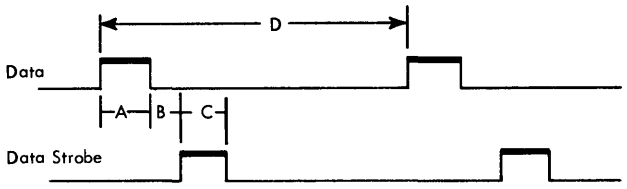
File Op originates in the 1410 system and indicates the beginning of an instruction to be carried out with the 7631. The 1411 will drop file op after the rise of end op. The trailing edge of the file op signal indicates that end of op may be dropped.

File Start Gate originates in the system. The line has a dual function. It is first used during an address transfer cycle to indicate that the 1411 has address data ready for transfer to the 7631. For this purpose the line must assume the active level at the time address data is put on the data bus to the 7631. The pulse may be as short as .5 usec, or may exist until the finish of the address transfer. However, file start gate must be inactive prior to the rise of end of address transfer.

The second function of the file start gate is to indicate the beginning of a read or write operation. For this function the file start gate must assume the active level following a properly executed address transfer cycle. The line may be active for 0.5 microseconds or may exist until the fall of file op.

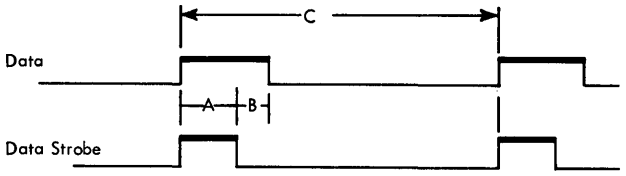
Data Strobe originates in the 7631 and is used to synchronize data transfers in either direction across the 1411/7631 lines. During a data or address transfer from the 1411 to the 7631 the line has the following timing characteristics. The data strobe pulse width is 1.58 to 1.65 microseconds. The period between leading edges of two successive data strobes is 11.06 to 11.60 microseconds during a fetch operation. During a read operation when data is transferred to the 1411, the duration of data strobe becomes 1.58 microseconds to 3.48 microseconds and the period becomes 10.66 microseconds to 12.0 microseconds. The timing relationship between data strobe and data is shown in the illustration following. The specified times between cycles refer to move mode only.

Relationship between data strobe and data:
Write or Address Transfer (Time in usec.)



$1.48 \leq A \leq 1.65$ $\quad 1.58 \leq C \leq 1.65$
$.79 \leq B \leq .825$ $\quad 11.06 \leq D \leq 11.55$

Read (Time in usec.)



$1.18 \leq A \leq 2.06$
$.79 \leq B \leq 3.71$
$10.66 \leq C \leq 11.96$

End of Address Transfer originates in the 7631 and indicates that the 7631 has completed an errorless

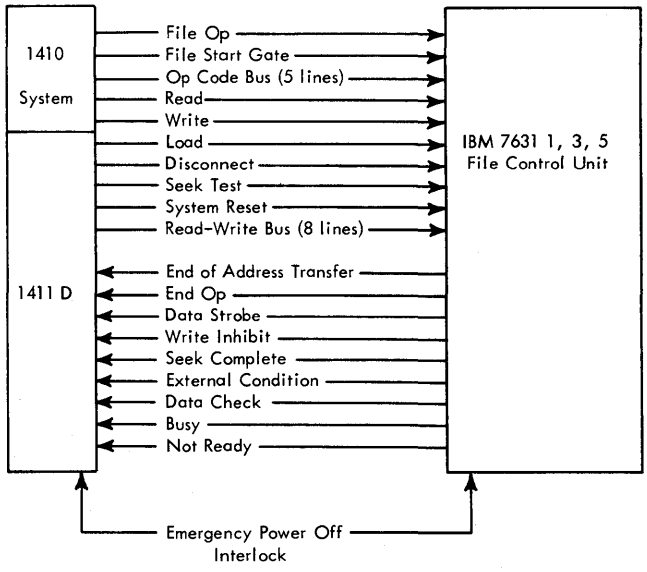


Figure 16. Operating Lines - IBM 1410 Data Processing System to/from IBM 7631 1, 3, and 5

address load cycle and that a read or write cycle is to follow. End of address transfer will remain up until file start gate is reactivated.

End of Op originates in the 7631 and indicates the end of an operation. End of op will rise at the end of an address transfer cycle if:

1. A seek, a set access inop, a release, or a block seek complete is being performed.
2. Any error occurs during the address transfer cycle.
3. A disconnect or a seek test is given by the 1411 during an address transfer cycle.

During a read or write operation, end of op is raised either when the 7631 logically completes the operation or when a condition is encountered that makes completion impossible. The end of op drops when file op from the 1411 is dropped.

System Reset originates in the 1411. A complete reset of the 7631 is accomplished with this line; however, the 1301 is not affected. Any existing attention status or seek operation in process at the 1301 is not affected by the system reset. The only condition placed on the execution of the reset is that on a dual 7631 the 7631 must be available to the channel that issues the system reset.

Seek Complete originates in the 7631. In a 7631 Model 1 the seek complete is the OR combination of all the attention status lines from the individual access control units. In order for the 7631 Model 3 to issue a seek complete to a channel, the 7631 must be available to that channel and the channel's block interrupt latch must be inactive. The status of a latch in the 7631 determines which system receives the seek complete. This latch is alternately set and reset by system 1 and system 2, respectively, as they process the interrupt and release the 7631.

Operation in this case would proceed as follows: System 1 issues seek and then release. System 2 issues seek, then release. The release of system 2 causes all interrupts to be sent to system 1. If the access mechanism addressed by system 1 is first to complete its motion, system 1 completes its read or write and then issues a release. The remaining interrupt is now sent to system 2. If the access associated with system 2 is first to complete its motion, the interrupt is issued to system 1 as before; however, the interrupt routine finds that the seek complete was meant for system 2. System 1 issues a release that sends the interrupt to system 2 for processing.

Write Inhibit originates in the 7631. This line is at +S level when active and -S when inactive. It is activated by a switch on the control console of the 7631 and sets the no transfer status in the 1411. A write instruction carried out with write inhibit on is executed completely in the 7631 except that no write data is written on the file and none of the data on the file is erased.

Read and Write originate in the 1411. The lines are active prior to the end of address transfer but they are not sampled into the 7631 until the file start signal following end of address transfer. The read or write fall following end of op.

Disconnect originates in the 1411. The disconnect informs the 7631 that the end of the allocated memory field has been reached for the file instruction. During an address transfer the 7631 will send one more data strobe to the 1411 after the disconnect is received. During a write operation the 7631 will send one more data strobe to the 1411 after the disconnect is received if the disconnect does not coincide with the last character transmitted for a given operation. During a read, the disconnect signal stops data strobes from the 7631 but does not stop the operation until the 7631 reaches a logical stopping point. The disconnect should be brought up from the 1411 not more than four microseconds after the last legitimate data strobe while reading or while writing. Disconnect should not fall until the 7631 has issued end of op.

Load originates in the 1411. The line must be active prior to the end of address transfer signal and should last throughout the rest of the instruction. The line causes the 7631 to operate in the eight-bit mode and to thereby accept the word mark as a valid bit for transmission. An absence of the load line indicates the move mode.

Operation Code Bus

The operation code bus originates in the 1411. It consists of four-bit lines plus an odd-redundancy parity bit. This bus is decoded into an operation during an address transfer cycle. This bus must be active prior to the first file start gate following a file op and last at least until end of address transfer or end of op, whichever occurs first. If the code sent on the bus is an invalid one for the 7631 or if the check bit is incorrect, the 7631 will send "external condition" to the 1411 at the end of the address load cycle.

The following codes are interpreted by the 7631:

Operation	Code C 8 4 2 1	Numeric Code
Seek	1 1 1 0 1	0
Single Record	0 0 0 0 1	1
Full Track without Addresses	0 0 0 1 0	2
Write Check	1 0 0 1 1	3
Block Seek Complete	0 0 1 0 0	4
Home Address Operation	1 0 1 0 1	5
Full Track with Addresses	1 0 1 1 0	6
Write Format Track	0 0 1 1 1	7
Set Access Inoperative	0 1 0 0 0	8
Release	1 1 0 0 1	9
Cylinder Operation	0 1 0 1 1	@

Data Lines

The data lines are broken into the read bus and the write bus. Each bus has eight lines which are called:

1411	7631
Check Bit	Parity Bit
Word Mark Bit	Bit 1
B	Bit 2
A	Bit 3
8	Bit 4
4	Bit 5
2	Bit 6
1	Bit 7

The write bus originates in the 1411 and must abide by the one timing restriction that a new character should be on the bus 7.9 microseconds after a data strobe.

The read bus originates in the 7631 and has valid data on it for as little as 1.77 microseconds to as much as 2.68 microseconds. The data must be sampled by the 1411 during the period of valid data. The relationship between data and data strobe is shown under data strobe.

Seek Test

This line originates in the computer. It is active prior to file start gate and will cause an end op after the address transfer is complete. It falls following end op from the 7631.

Status Condition

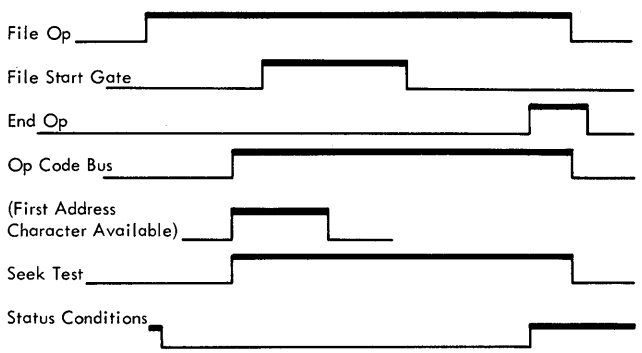
The status condition lines show error status, power-on status, and availability status of the 7631. During a data or address transfer operation the lines should be sampled at the end of op. Any other sampling of the status conditions should be done no sooner than 10 microseconds after the start of file op. The particular status conditions used are: data check, ready, busy, and external condition. The causes of the status conditions are:

STATUS CONDITIONS

Check Definitions	Status Conditions
Invalid Sequence	Data Check
Response Check	Data Check
Parity Check	Data Check
Cyclic Code Check	Data Check
Data Compare Check	Data Check
Format Character Check	Data Check
Access in Motion	Busy
Interface Not Available	Busy
7631 Power Off	Not Ready
Access Inoperative	Not Ready
Home Address Switch Check	Not Ready
Wrong Length Format	External Condition
No Record Found	External Condition
Write Check without Mode Setting	External Condition
File Frame Circuit Check	External Condition
File Adapter Circut Check	External Condition

7631/1410 TIMINGS

Timings for Seek Set Access Inoperative, Seek Test, Block Seek Complete, and Release



1. File op rises and remains up throughout the operation. If file op drops, the operation is terminated immediately.

2. File start gate rises. The timing is a system function; however, the earliest time that the 7631 will recognize the signal is 22.4 microseconds. If the file start gate is up prior to the earliest timing, it will ignore the signal until it is ready to accept it. If the file start gate is issued later than the 22.4 microsecond timing, the 7631 latches up and waits for the signal until it arrives. The maximum length of the file start gate pulse is 44 microseconds.

3. End op is sent to the system 114 microseconds after the file start gate. Before the end op uses the address, characters are transferred from the system to the 7631 according to the data transfer timings.

4. File op drops as a result of end op. The timing is a system function.

5. End op drops 1.2 microseconds after file op drops.

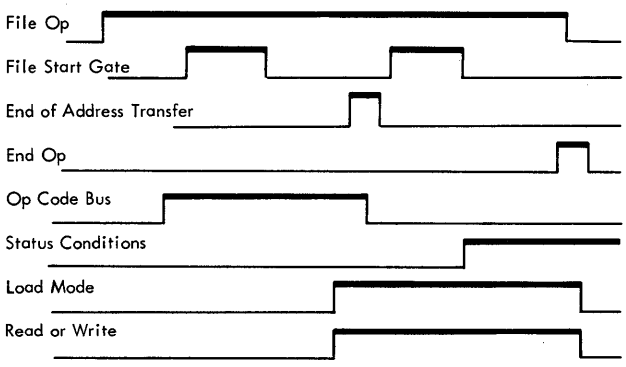
6. The op code on the op code bus must remain active prior to file start gate until after end op rises.

7. If a seek test is to be performed, the seek test line must be up prior to file start gate and must remain active until after end op.

8. The first character of address data must be on the write data bus prior to file start gate. All following characters abide by data transfer timings.

9. Status conditions are available to the system at end op. They remain on until the following file op.

Read or Write Operation



1. File op rises and remains active until end op.

2. File start gate initiates the address transfer cycle. The timing is the same as for seek.

3. The op code bus timing is the same as seek.

4. If status conditions occur during the address transfer cycle, an end op is sent 114 microseconds after file start gate and no further processing takes place. If no status conditions occur during the address transfer cycle, the end of address transfer cycle signal is sent 116 microseconds after the file start gate. The end of address transfer signal is 14.4 microseconds long.

5. After end of address transfer drops, the 7631 looks for file start gate to rise again. The timing of the rise of the second file start gate is a system function.

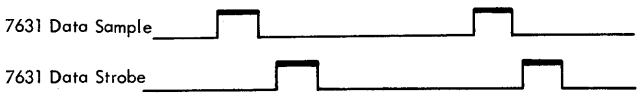
6. The load mode line must precede the second file start gate and fall after end op if the operation is to be performed in load mode.

7. Read or write rise must precede the second file start gate rise and fall after end op.

8. If status conditions occur during the read or write operation, the conditions will be available at end op and will remain active until the next file op.

Data Transfer Timings

Write or Address Transfer Cycle:



1. Data sample is between 1.58 and 1.65 microseconds long. It occurs within a minimum period of 11.1 microseconds.

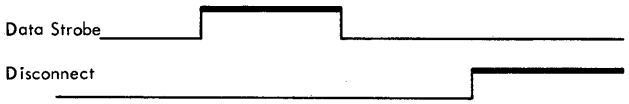
2. Data strobe indicates to the system that the 7631 has accepted a character and that the next character should be made available. Data strobe rises between .79 and .83 microseconds after the fall of the 7631 data sample. The data strobe varies in width from 1.58 to 1.65 microseconds.

Read

1. Data is available on the read data bus for 1.8 to 2.65 microseconds.

2. Data strobe rises when data is available. The pulse is 2.8 to 3.71 microseconds long. The minimum period of data strobe is 10.66 microseconds.

Disconnect



Disconnect rises as the result of a data strobe. Disconnect cannot preceed the data strobe. It must rise no later than 4.0 microseconds after the rise of data strobe.

FUNCTIONS, 1410 SYSTEM/7631 FILE CONTROL

The functions performed by the 7631 File Control for the 1410 Data Processing System depends on the contents of the disk storage instruction. The various parts of the disk storage instruction and their functions follows:

Operation Code (1410)

Disk storage operations are initiated by a move (M) or load (L) operation-type instruction. The move instruction specifies that data are to be read or written in the six-bit mode. The load instruction designates eight-bit mode. See Figure 17.

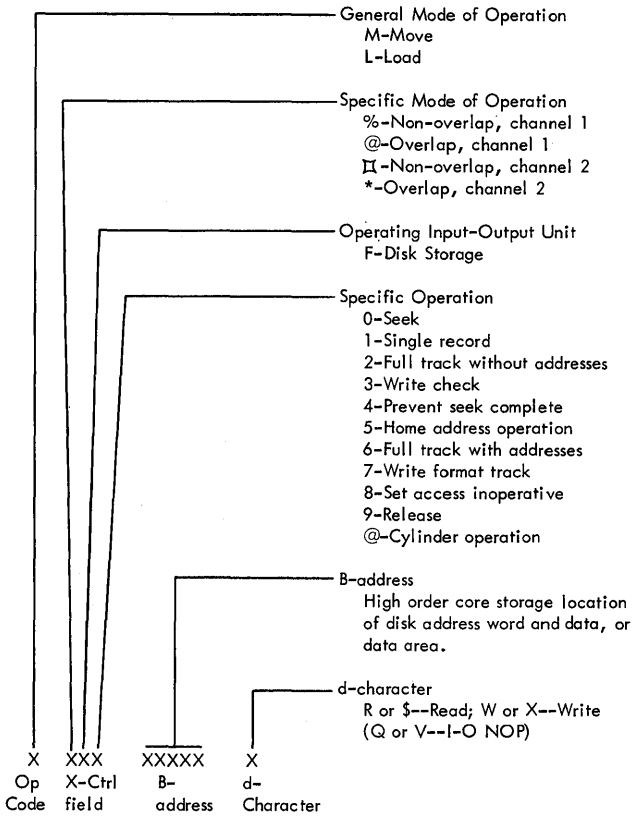


Figure 17. Disk Storage Operation Code Format

NOTE: Data written using a move mode instruction must be read with a move mode instruction. Also data written using a load mode instruction must be read with a load mode instruction. This insures the proper coding relationship between data in core storage and disk storage.

X Control Field

The high-order character of the X-control field specifies which data transmission channel is to be used and the overlap or non-overlap status of the operation.

The second character (F) specifies 1301 Disk Storage as the active input or output device for this operation.

The low order position specifies which operation is to be performed.

0-Seek
1-Single Record
2-Full Track without Addresses
3-Write Check
4-Prevent Seek Complete
5-Home Address Operation
6-Full Track with Addresses
7-Write Format
8-Set Access Inoperative
9-Release
@-Cylinder Operation

B-Address

The B-address portion of the instruction addresses either group-mark-word-mark or the high-order position of an eight-character data field in core storage, depending on the operation to be performed. The data field (disk address word) is sent to the 7631 (Figure 18); it specifies the access mechanism, a module number and a track address in the module except for the single record operation. Description of the disk address word for the single record operation will be made with the description of single record operation.

The high-order position of the disk address word specifies the access mechanism. Because there is only one access mechanism per module, the access mechanism address is always zero. Modules are numbered from 0 through 9, depending upon a fixed assigned number for each module. The module to be used is indicated in the second position of the disk address word. The next four positions (HA1 part) are used to address a specific track in the module (0000-9999). The last two character positions (HA2 part) are used for the home address identifier characters. A group mark with word mark must appear in the core storage position to the immediate right of the disk address word. The disk address word, illustrated in Figure 18, addresses access mechanism 0, module 2, and track 7860AA.

Data to be written on disk follows the associated disk address word in core storage. Also, data read from disk is placed in core storage following its associated disk address word. A group mark with word mark must appear in the core storage position to the immediate right of the last character of the core storage data field to be written or the data area to be used to receive data from disk (Figure 19). The location of a disk address word and its related data field or data area is determined by the user.

The disk address word must be eight characters in length to establish a valid length for disk address words. In some operations not all of the characters of the disk address word are essential to the

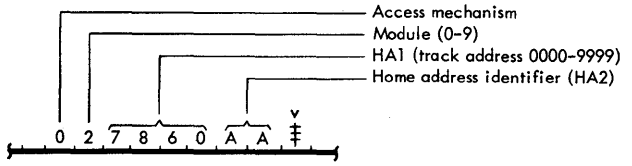


Figure 18. Core Storage Disk Address Word

operation. Portions which are not essential (not verified) may consist of any valid characters. However, characters not verified are parity checked.

Figure 20 shows those operations which use a disk address word, the characters that are verified, and the characters that are not verified. Character positions not verified are indicated by the symbol ▨.

d-Character

This portion of the instruction specifies whether a read operation (R or $), a write operation (W or X), or an I-O no-op (Q or V) is to take place. Read or write instructions defining the limit of a core storage field or area by a group mark with word mark use the R or W d-character, respectively.

Read or write instructions which define the limit of a core storage field or area by the end-of-storage indication use the $ or X d-characters, respectively. Explanation of instructions in this manual will assume the use of only the R or W d-character for reading or writing operations. The Q or V d-characters used with the I-O no-op will be explained in the discussion of this operation.

Instructions using the $ or X d-character cannot be overlapped.

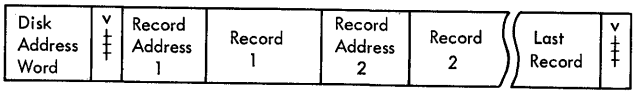


Figure 19. Core Storage Layout - Read or Write Full Track with Address

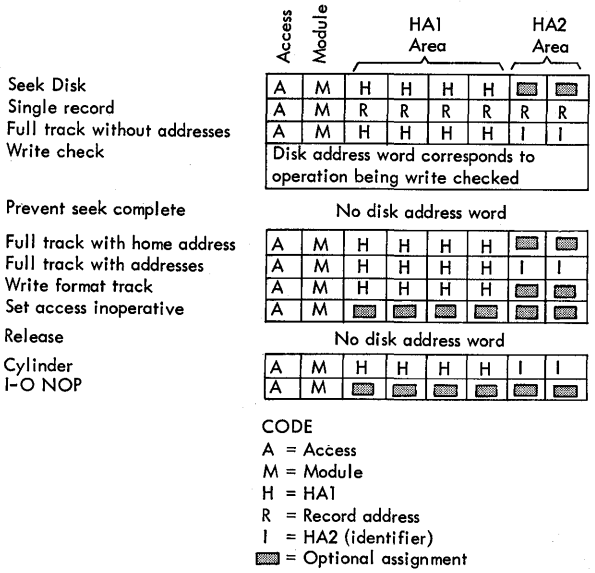


Figure 20. Disk Address Word Format

INSTRUCTION HANDLING, 1410/7631

An instruction intended for the 7631 causes the file op line to be activated. Under a given file op the 7631 performs an address transfer cycle and then, if required, the actual read or write cycle.

During the address transfer cycle the 7631 decodes the instruction to be performed from an op code bus. All instructions with the exception of release and block seek complete cause the 7631 to request eight characters of address data. While the address data are being transmitted the 7631 performs various checking operations. It checks the parity of each address character, confirms that a valid op code has been accepted, and verifies disk storage ready and operative lines. If any check conditions are present, the operation ends after the address data have been transmitted.

The read or write cycle will immediately follow the address load cycle if the decoded instruction requires it and if no unusual condition has arisen during the address transfer.

HEAD SELECT UNDER AN ADDRESS TRANSFER CYCLE

In all data address transfer cycles except during a single record operation, the 7631 transfers a head address to the 1301. (Data address transfer cycles here mean that the eight characters of address are transmitted.) This permits operation on the various tracks of the cylinder without intervening seeks. However, if single record operations are to be performed on various tracks of the cylinder, seeks must be performed to select the proper head prior to each of the single record operations. This procedure is necessary because record addresses are scrambled whereas home addresses reflect the physical locations of the various tracks.

OPERATIONS REQUIRING ONLY ADDRESS TRANSFER CYCLES

Seek

The eight characters transmitted under a seek instruction describe the access unit, module, and track to be located. The 7631 selects the particular access mechanism, encodes the cylinder-head digits into the 1301's track and head code, and sends the address to the 1301. An end op signal is then issued to the 1411 and the 7631 is available for further operations while the access moves to the addressed track. If errors have occurred, one or more of the error status lines will be present at this time. If an error occurs before the seventh character of the eight-character address is received, the access will not be instructed to move.

Set Access Inoperative

The set access inoperative instruction causes the addressed access to be removed from system usage. Any instruction sent to the access at a later time will show not ready at the end of the address transfer cycle and no read or write cycle will take place. The address associated with the set access inoperative instruction has only the module and access digits as significant characters. The set inoperative signal from the 7631 to the 1301 is issued without regard to prior ready or operative status of the access.

Release

The release instruction has significance only with the dual models of the 7631. Operation proceeds in the following manner. The 7631 is normally reset to a state where both systems are available. When an instruction is issued to the 7631 over one line set, then the other line set is no longer available and the busy line is raised on the unavilable 1410. The 7631 remains associated with the one channel until a release instruction is sent from that channel. There is no programming method available for the "locked out" computer to break in on the operation.

The release operation is performed by bringing up file op and the code for release. The 7631 sends an end of op without transfer of data. The release instruction will be decoded on a Model 1 but it has no significance.

Block Seek Complete

This instruction has significance only with the dual models of the 7631. When a block seek complete is decoded, the system giving it will not receive any subsequent seek complete when an access arm comes to rest. The above condition is reset by that same system giving a seek instruction.

The block seek complete instruction is performed by bringing up file op and the code for this operation. The 7631 sends an end of op without transfer of data. The block seek complete instruction will be decoded on a Model 1 but it has no significance.

Seek Test (I-O No-Op)

The seek test operation is operative only on models of the 7631 that are attached to the 1410 with priority processing feature. It is achieved by inserting a Q or a V in the d-modifier position of the 1410 instruction word. The operation is used on these 1410 versions as the method for a program to interrogate the attention status of the access mechanisms of the system. The operation proceeds as follows: When the system issues a seek, the access mechanism moves to the selected track and raises its attention status line to the control unit. The 7631 sends a seek complete signal to the 1411 when any of the attention status signals are up. An attention status drops when the particular access mechanism associated with it is selected for another operation. If only one access mechanism is instructed to seek, when the seek complete appears at the 1411 a read or write operation can immediately be issued to the particular access mechanism. By the beginning of read or write, the attention status and the seek complete signal will be dropped. When multiple seeks are issued, the seek complete signal at the 1411 indicates only that one of the accesses has assumed attention status. The 1410 must then issue a seek test to each of the access mechanisms in turn. The 7631 sends a select ACU signal to each of the access mechanisms as it is selected for the seek test and samples the ready and operative status. A busy indication to the 1411 will show that the access is still in motion. Otherwise, the access may be used for reading or writing.

The seek test to the 7631 must always be accompanied by an operation code such as single record, track without address, seek, etc. If a seek test is given an end of op will be sent to the 1411 at the end of the address transfer. This method can therefore be used to set up an operation code, without actually reading or writing, so that a write check can be given under the next file op.

If a seek test accompanies a seek operation, the addressed arm is selected but the 7631 will not instruct that arm to move. In addition, an existing prepare-to-verify mode will not be reset. This makes it possible to interject seek tests without disturbing an existing prepare-to-verify mode.

OPERATIONS REQUIRING ADDRESS TRANSFER AND READ OR WRITE CYCLES

Write Single Address

This operation in the 7631 is initiated by file op. After performing internal setup procedures, the eight characters of address are received and the 7631 performs the various checks as just previously described. If no unusual conditions have occurred, the 7631 sends a signal-end of address transfer to the 1411.

The write line from the 1411 is then sampled into the 7631 and the write cycle proceeds. The 7631 squelches the read amplifier AGC voltage and then sets it to a proper level. The search for the particular record address follows immediately. No time is used waiting for the index point before attempting to compare the addresses. The 7631 notes the passing of the index while searching for the particular record address and signals no record found if the index comes up a second time. In the event of a bad track detected in the file array, the 7631 reads out the flag bits and transfers them to the file frame. The search for the record then continues on the alternate surface. In this particular case it could take as long as three disk revolutions before the 7631 issues external condition if the record does not exist on the particular track.

Normally, the 7631 gets an address comparison on the proper record address and begins to operate on the record following the address comparison. The 7631 first causes an AGC burst to be written and then begins to sample the data from the 1411. Each character from the system is parity checked and if it should be in error, the error condition is noted while data transfer continues. The error condition is transferred to the 1411 at the end of the record. The 7631 generates a cyclic code check burst while writing and records the burst after the last character as defined by the format track.

During the writing of the record, if the 1411 should send a disconnect, the 7631 stops data transfer and records characters on the disk consisting of a sync bit and zero data bits. These blank characters are recorded until the end of the formatted record area where the check burst is placed and end of op is issued.

Write Track

The write track operation is initiated by file op. The address transfer to the 7631 is handled in the same manner as previously described under write single record. The 7631 must wait for the index point to pass under the heads before the track operation can begin. The read amplifiers in the file frame are adjusted during the index time; then a comparison is made between the home address recorded on the track and the address that has been stored in the 7631. The comparison that is made includes both the physical address portion and the home address identifier portion of the home address. While attempt- to compare the home address, the 7631 examines the flag area. If flag bits are present, a transfer to the

alternate surface is performed and the home address comparison is attempted on the alternate surface. If the address comparison is successful, the 7631 begins to send data strobes to the system during the first record address area of the track. The 7631 receives data until the area is filled and then the cyclic code check characters are placed behind the address. The 7631 fills in the necessary gaps and the AGC bits before beginning data transfer again at the record area. The operation continues with the 7631 filling each of the address and data areas with information from the system.

The track operation normally terminates in one of two ways. Either the 1411 issues a disconnect or the 7631 senses that it has completed writing the last record of the track. If a disconnect is issued, the 7631 stops writing and sends an end of op after the check characters have been placed behind the particular record or address being written at the time of the disconnect. If disconnect occurs in the middle of an address or data area the remainder of the area is written with blank characters. When the end of op is sent to the computer, the status byte will indicate whether errors have occurred during the track writing but no indication is given as to which record is in error.

Write Track Without Addresses

This operation is similar to the write track operation except that record address areas are not disturbed during the track without addresses operation. The 7631 compares the entire home address during either of the track operations. After a successful comparison, the 7631 begins receiving data for the first record area following the home address. The record address areas are passed over without notice as each of the record areas is written.

The ending of the write track without addresses differs from write track with addresses. If the 7631 senses a parity error in any character of data during a track without addresses op, the 7631 issues an end of op at the end of the particular record where the invalid character was recorded and indicates the error in the status byte. In the event of disconnect, the procedure is to write blanks in the remainder of the particular record that is being written and to issue end of op.

Write Home Address

In order to perform either a read or write home address operation, the home address switch on the operator's panel of the 7631 must be set to the active position. Failure to set the switch will result in the sending of an end of op to the 1411 at the end of the address transfer cycle and the recording of the not ready condition. With the HA switch in its proper position, the write home address operation begins with a comparison of the physical portion of the home address only. The home address identifier from the system does not have to agree with the recorded HAI. If the physical home address coincides, then the write operation begins at the home address identifier.

The 7631 receives new home address identifier characters from the system and records them in their position between the physical address and the first record address. The 7631 continues to receive data for the rest of the track, filling in address and record areas.

Data transmission may end in either of two ways. The 7631 senses the end of the last record on the track, or the 1411 issues a disconnect which causes the 7631 to terminate data transmission immediately. One character beyond the check character of the last record on the track, the 7631 initiates a burst of ones which are written until the index point is sensed. At this time end of op is sent to the 1411.

If the HAO-CE switch is on during a write home address operation, address verification is bypassed and the 7631 begins writing AGC bits at the index point until one character before the actual recording of the physical home address, at which time the 7631 begins receiving data from the 1411. The first five characters shall constitute the physical home address and flag byte. On detecting the gap following HA1, the 7631 stops data transmission and writes the three-digit check character. The remainder of the operation is identical with the normal write home address operation.

Write Format

The write format instruction requires an address transfer prior to the actual writing on the format track. The address included with this instruction must be the home address of one of the tracks controlled by the format that is to be changed. The compare made in this case is performed on the physical address only. If the HAO switch on the 7631 CE panel is on during a write format op, the address comparison is bypassed and writing proceeds.

One other restriction is placed on the format write op, namely, the key-lock for the particular module must be in the format write position. The key-lock is located in the file frame.

The actual writing of the format begins one revolution after the address comparison is completed. The format write operation must be in move mode. During the format write operation the 7631 accepts only the BCD 1, BCD 2, BCD 3, and BCD 4 characters.

Should any character be received other than these four, the 7631 will set data check of the status conditions and terminate the operation with end of op.

Respectively, the four characters cause the 7631 to write on the format track a seven-bit character of all ones, a seven-bit character of all zeros, a nine-bit character of all ones, and a nine-bit character of all zeros. These characters are used to construct a format as shown in the Appendix.

The format areas, A, B, C, D, E, F, and G are uniquely associated with the home address that is recorded at the start of each data track. The areas H, J, K, and L are associated with the record address. The areas M, N, P, and Q are associated with the data. The areas A, B, C, D, and E, associated with home address, must be written using the BCD 3 and BCD 4 characters. This is necessary because the physical portion of the home address is indelible in the sense that the customer has no access to it and that it will remain constant for all using systems. The format areas which control address areas must be written in such a manner as to guarantee proper alignment between the format and address areas.

Format areas associated with the record portion of the home address, as well as those associated with record addresses (H, J, K, L) and with data (M, N, P, Q), are written using the appropriate six-bit or eight-bit data characters that agree with the move or load mode in which the data is to be written.

Prior to the area A, the file control automatically generates a burst of ones between early and late index marks. The index points are shown in Figure 27. The burst of ones is written to set the sensitivity of the format read amplifier on any ensuing read or write.

A description of the format track writing areas is as follows:

Area A: Three characters mandatory length. The BCD 4 character should be used for writing this area. If the area is less than the specified three characters, the recoverability of data can not be guaranteed after a major mechanical change involving disk restacking and actuation replacement.

Area B: Length of nine characters. The BCD 3 character should be used for writing the area. The length permits the four-character physical address portion of the home address and its flag bits to be written. Only the physical address portion of the home address is used for verification on a subsequent home address or format operation.

Area C: Must be one character long. The one character used to write this area is a BCD 4.

Area D: Mandatory length of ten characters of ones. It should be written by means of the BCD 3 character.

Area E: Must be one character of zeros. The system should send a BCD 4 to the 7631 to have it written.

Area F: Minimum length of six characters. Either the BCD 1 or BCD 3 is used for this area depending on the desired bit mode for the particular data cylinder. The BCD 1 is used when the entire cylinder is to be written in move mode. The BCD 3 is used for a cylinder in load mode. This area permits the home address identifier to be written. The minimum home address identifier must contain two characters. For word-oriented systems, the length of the home address identifier can be increased to any value. The physical address portion and the first two characters of the home address identifier are compared for a track operation or cylinder operation. Any other characters in the home address are internally ignored by the 7631. However, on a read home address operation the 7631 will return all of the home address characters to the system in their original order and form.

Area G: Mandatory length of twelve characters. Either the BCD 2 or BCD 4 should be used to write this area. The minimum length of this area is dictated by a combination of file control and disk storage considerations. The file control considerations are that the actual last character of the home address that is written is placed two characters beyond the finish of the format home address area F. The cyclic check characters for the home address are placed beyond the last character of home address and demand four characters of space. The 1301 specification demands that a time interval as long as six characters be provided for the noise caused by a write driver being started or stopped. Any attempts to write the area G other than the length given above will result in marginal operation of the file and possible failure to read data correctly.

Area H: Minimum length of ten characters. Either the BCD 1 or BCD 3 is used for writing this area. Area H can be varied in length in the same manner as area F to achieve record addresses of a convenient word size. To cause an RA length of n characters, area H should be n + 4 characters long.

Area J: Must be one character long. Either the BCD 2 or BCD 4 should be used to write this area.

Area K: Mandatory length of ten characters of ones. It should be written by means of either the BCD 1 or BCD 3 character.

Area L: Must be one character of zeros. The system should send either a BCD 2 or BCD 4 to the 7631 to have it written.

Area M: Minimum length of six characters. The length of M is determined from the length of the record that is to be recorded under the control of M. For a record of x characters, M is equal to x + 4 characters. Either the BCD 1 or the BCD 3 may be used for recording area M, depending on whether six-bit or eight-bit characters are to be recorded in the corresponding record areas of the data tracks. All of the records in a cylinder can be either in six-bit mode or in eight-bit mode but not in a mixture of the two modes.

Area N: Mandatory length of twelve characters. It must be written with either the BCD 2 or BCD 4 characters. The BCD 2 should be used if all records of the cylinder are recorded in six-bit mode. The BCD 4 is used where the cylinder is assigned for eight-bit data.

Area P: Must be only one character in length. The area may be written using either the BCD 2 or BCD 4 characters. Area P is used only after the last record of a track. Area N can be seen after the first record area (Figure 27). If a track is to have multiple records, each record is followed by an area N, except the last record, which is followed by a single character of zeros and then the filler characters.

Area Q: Minimum length of eleven characters. This area is written under the internal control of the 7631. Control is passed over to the 7631 from the program by use of the disconnect signal over the 1411/7631 interface. After receiving the disconnect signal, the 7631 writes one bits until it senses the early index signal and then continues writing for three more characters. The 7631 checks the filler area to assure that the length is equal to or greater than the minimum length. An external condition indication results if the filler does not cover sufficient space.

Read Single Record

The read single record operation requires an address transfer prior to the start of the record read. The address is that of a particular record on the track. Since no head switching is caused during the address transfer, the particular cylinder and head must be selected prior to the read single record operation. The address search begins after the AGC squelch and set are completed. The adapter does a bit-by-bit comparison on each record address until an address compare true is obtained. If the index point is passed twice in the course of the search, then an external condition is noted. The actual reading of a record is performed following a successful address comparison. The 7631 sends the data characters to the system, verifies the legality of the check characters following the record, and sends an end of op to the 1411. A disconnect during the operation will not stop the 7631 from finishing the record and checking the check burst; however, data transfer is suspended after the disconnect.

Read Track

The address sent with the read track instruction is a home address. Both the physical address and the home address identifier must compare before the operation begins. A failure to compare will cause an external condition indication to be given along with an end of op. A successful compare permits the 7631 to begin reading at the first record address area. The address is read out and sent to the system, followed by the first record, and then the second address and the second record, etc. The operation terminates when the adapter senses that it has completed comparing the check characters of the last record of the track. The end of op is then issued. A failure in comparing a check burst is signaled to the system at the end of op. Disconnect causes end of op at the finish of the address or record area in process at the time of disconnect.

Read Track Without Addresses

The read track without addresses operation proceeds in the same manner as the read track except that the record addresses are ignored as they are encountered and the record data only is transmitted to the system. If a disconnect is issued, the end of op occurs after the record in which disconnect was received. A check character compare failure is signaled by an end of op at the finish of the record in error. In this event, data check will be present.

Read Home Address

The read home address operation requires only that the physical portion of the home address be compared successfully and that the home address switch on the 7631 operator panel be in the home address operation setting. The most useful application of the read HAO is to recover tracks of information after a major mechanical change involving disk restacking and actuator replacement. The read home address operation does not depend on the format track for recognition of data and address areas. With this operation, and assuming that a proper gap is

provided between late index and the beginning of the home address area, the processor can restore a file to normal operation after a major mechanical change. The 7631 compares the physical address portion of the home address and begins reading at the home address identifier digits. All address and record data of the track are read. A disconnect will suspend data transmission and the operation will terminate with end op at the end of the data area being read. Should a compare failure occur on any check character of the track, a data check will accompany the end of op.

Write Check

The write check instruction is used to perform a bit-by-bit comparison of the data written on the disk with the same data retransmitted across the 1411/7631 interface. Each of the write modes has an associated write check operation which is optional and under program control. The mode may be set up by a previous read or write operation or an errorless seek test with a mode setting. The 7631 retains the mode information from the write operation or seek test, either single record, track operation, etc. The write check op is accompanied by an address which should agree with the address used for the write op. The 7631 locates the address and compares the recorded data against the same write data strobed in from the system. Any compare error will cause a data compare check indication.

During a write check operation on a format track, the format gap detector circuits in the 7631 are checked to determine whether or not they are within their specified tolerance. An external condition is noted if the circuits are not within tolerance. When a disconnect is issued during a write check operation, the 7631 will discontinue data transmission and comparison. The disconnect signal must be issued at the same time with respect to the data field as in the preceding write instruction. The 7631 proceeds to the logical stopping point for the particular mode setting before issuing end op.

Cylinder Operation

Cylinder operation of the 1301 is an optional feature. With the addition of the option, an entire cylinder of records may be written or read. One of the forty home addresses in the cylinder is received during the address transfer cycle. The 7631 compares the entire home address against the recorded home address and begins data transfer if the address comparison is successful. All of the records of addressed track are either read or written as the instruction dictates. When the last record of the track is completed the 7631 determines the next higher head location of the cylinder, sends the head number to the file, and continues to operate on the records as they pass by the head. Operation continues on the records only until the 7631 notes the end of the cylinder. The end of op is then issued. In the event of any data error during a cylinder operation, the 7631 sends the end of op at the finish of the record containing the error. If a disconnect is issued during a write cylinder operation, the 7631 fills out the data area on which it is operating with blank characters and then issues end of op. During a read, the disconnect causes an end of op after the record that was in process at the time of disconnect.

No address comparisons are made after the initial compare of the home address.

ALTERNATE SURFACE FLAGGING

Except for the format track, the disk surfaces of the 1301 may not be completely defect free. The surface defects may render a portion of the data track useless. Alternate surfaces are provided in the 1301 for usage as switchable replacements for the defective data surfaces. When a track is identified as defective, it is necessary to have a customer engineer assign an alternate surface and to mark the defective track with flag bits which cause switching to the alternate surface. In order to write the flag bits the CE will need access to the system and will have to turn on the HAO switch on the CE panel. With this switch on, he must perform a write home address on the defective surface. Under this operation, the flag bits are written in the fifth character of HA1. The alternate surface must then be selected so that the physical home address of the defective surface may be recorded. This is done by placing the code for the alternate surface in the seventh character of the address transmitted under the address transfer cycle. The HAO switch on the 7631 CE panel must be in the on position to perform the alternate surface operation.

While doing any address search, the 7631 inspects the flag bits as the physical portion of the home address is passed. Upon sensing the bits, the 7631 automatically transfers the new head address to the file and execution of the read or write proceeds without reference to the system program.

STATUS CONDITIONS

The 7631 is cognizant of four status conditions, namely, data check, busy, not ready, and external condition.

An error of the data-check type is considered only a nuisance and, in most cases, an operation is carried out to its normal logical finish before notifying

the program of the condition. The check conditions grouped under external condition are all of a serious nature and cause an immediate stoppage of 7631 operation at the time that they are encountered. The busy and not ready class of errors have no particular stopping time that is applicable to the entire class.

DATA CHECK

Parity Check: The 7631 File Control is an odd-parity machine. As bytes are transferred from the processor the bit count of each is checked. If an even number is detected the data check condition is set.

Cyclic Code Check: The cyclic code check is made by generating code characters for each address and record as bits are streamed off the disk surface during a read operation. These newly-generated characters are then compared bit-by-bit with those previously recorded during the write operation. Failure to compare will indicate the occurrence of a single-bit error, double-bit error, triple-bit error, or other odd-redundancy error, or any burst of errors in which the first and last bits in error are physically located within a 15-bit cell. Any type of error not specifically provided for above has a probability of 1 in 65,536 of passing undetected.

Data Compare Check: Data compare check can be set only during a write check operation. The condition indicates that a compare error was detected somewhere during write check. Data is streamed off the disk surface and compared bit-by-bit with that transferred from the processor. This condition falls under data check.

Format Character Check: During a format write or format check operation only four characters are considered legal by the 7631. These characters are: BCD 1, BCD 2, BCD 3, and BCD 4. Any character transmitted over the interface other than one of the four will cause data check. This error will result in an immediate end of op.

Except for a track without addresses operation or a cylinder operation, and as noted above, a data check does not stop data transmission to or from the system and the end of op is issued at the normal termination time of the operation. During a read or write TWA or CYO, data transfer ceases at the end of the record in which the check condition occurred and an end of op is then issued.

Invalid Address: If the selected access arm of a 1301 is situated at a CE track when a customer program enters a read or write cycle, an invalid address condition is registered and will cause a data check to the 1411. This error will result in an immediate end of op.

BUSY

A busy condition precludes any further processing of an instruction.

Access in Motion: The 7631 senses an access in motion by means of a line from the access. No operation can be performed with a moving actuator nor can the address to which it is heading be changed once motion begins.

System Not Available: In a dual system 7631, the busy condition is indicated to the "locked out" channel while the 7631 is tied up with the other channel. The busy condition remains in a DC on state until the 7631 is released and the lines are restored to available status.

NOT READY

7631 Power Off: The 7631 normally sends the ready condition across the interface to the 1411. The absence of ready is then interpreted as not ready in the 1411. By defining the communication in this manner, a not ready may be sensed at the 1411 when the 7631 has power off and thus cannot send ready.

Access Inoperative: This indication exists when the file control fails to receive an access operative signal from an addressed access control unit. The access may be mechanically out of order or possibly non-existent.

Home Address Switch Check: If a home address operation is attempted without a proper setting of the home address switch on the 7631 operator's panel, a not ready indication is given.

EXTERNAL CONDITION

Wrong Length Format: This condition arises if an attempt is made to format for a greater number of characters than the track will hold. The 7631 senses too few filler characters after the disconnect signal.

No Record Found: The no record found condition occurs if the 7631 fails to locate the address that was issued to it during the address transfer cycle. In single-record mode the 7631 must pass index twice before noting no record found. On all other operations the indication can be given as soon as an attempt to compare the home address fails.

Write Check without Mode Setting: A write check may only follow a read or write operation on an errorless seek test with a mode-setting operation code. A write check under any other circumstances will cause an external condition.

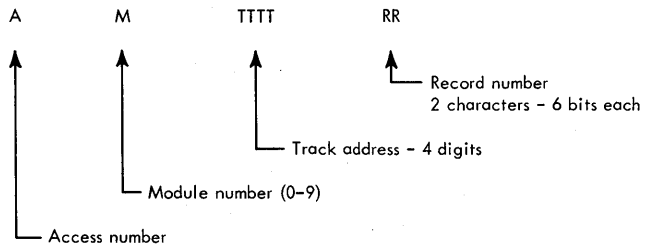
File Frame Circuit Check: The file frame circuit indicates a circuit failure in the 1301 file storage. The particular conditions that could cause this are write driver failures or a failure of the access operative or ready lines from the 1301 to the file control.

File Control Circuit Check: The causes of this indication are a gap detection circuit functioning out of tolerance during a write check of a format track or a failure of either the address-comparison circuitry or the cyclic code generator in the file control. The address comparison circuits are automatically checked just prior to comparing any address. The cyclic code generator is automatically checked just prior to writing either addresses or record data.

Invalid Op Code: This error is registered when the 7631 senses that the code transmitted on the op code bus has an improper parity bit or could not be performed by the 7631.

ADDRESS COMPARING

In general, an address in the 7631 is composed of six numeric digits followed by two alpha-numeric six-bit characters. The address format is as follows:



Access (A) and module (M) digits are decoded in the 7631 and the decoded outputs select a particular access control unit in the disk storage. Access module combinations which interrogate non-existent address locations result in an access inoperative indication. This occurs because the 7631 cannot differentiate between an access with its power off and a completely non-existent access location. During an address compare, the access-module digits are not a part of the comparison. Bit-by-bit comparison is made on the remaining digits of the address. On the four-track digits, only the numeric portion of the digit is compared. The zone bits do not enter into the comparison. In a record address, the four-track digits need not reflect physical track locations. However, in a home address, the track number recorded must agree completely with physical location. The last two characters of the address are alpha-numeric and not limited to purely numerics as in the case of track digits. The 7631 compares both the numeric and the zone portions of the record identifiers and the home address identifier. The home address identifier characters are useful in some program applications, particularly for multi-programming.

INSTRUCTION TIMES

Read and write commands vary in time duration depending on the length of record (for single record operations) and rotational coincidence of starting points. Address transfer cycles, which precede read or write commands are in six-bit mode and require 160 usec. A cylinder operation involving all 40 tracks within a cylinder will take 1.3 seconds, provided no tracks are flagged. Flagging could add a maximum of .207 second.

Data strobes to the processor will occur cyclicly at a minimum average period of 11.1 microseconds in six-bit mode and 14.2 microseconds in eight-bit mode. However, the minimum time between any two characters can be 10.7 microseconds in move mode and 13.8 microseconds in load mode.

The control panel of the 7631 is primarily intended for maintenance simulation purposes. The panel is mounted on the right front cover of the frame. It has an exposed section, and a hidden section intended for customer engineering usage. Indicator lights on the exposed section reflect the status of data and controls within the 7631. Operator switches are located in a light-and-switch assembly above the indicator lights. See Figure 21. The CE section of the panel is covered and contains switches for simulation of data, commands and responses from the channel, and responses from the files. See Figure 22.

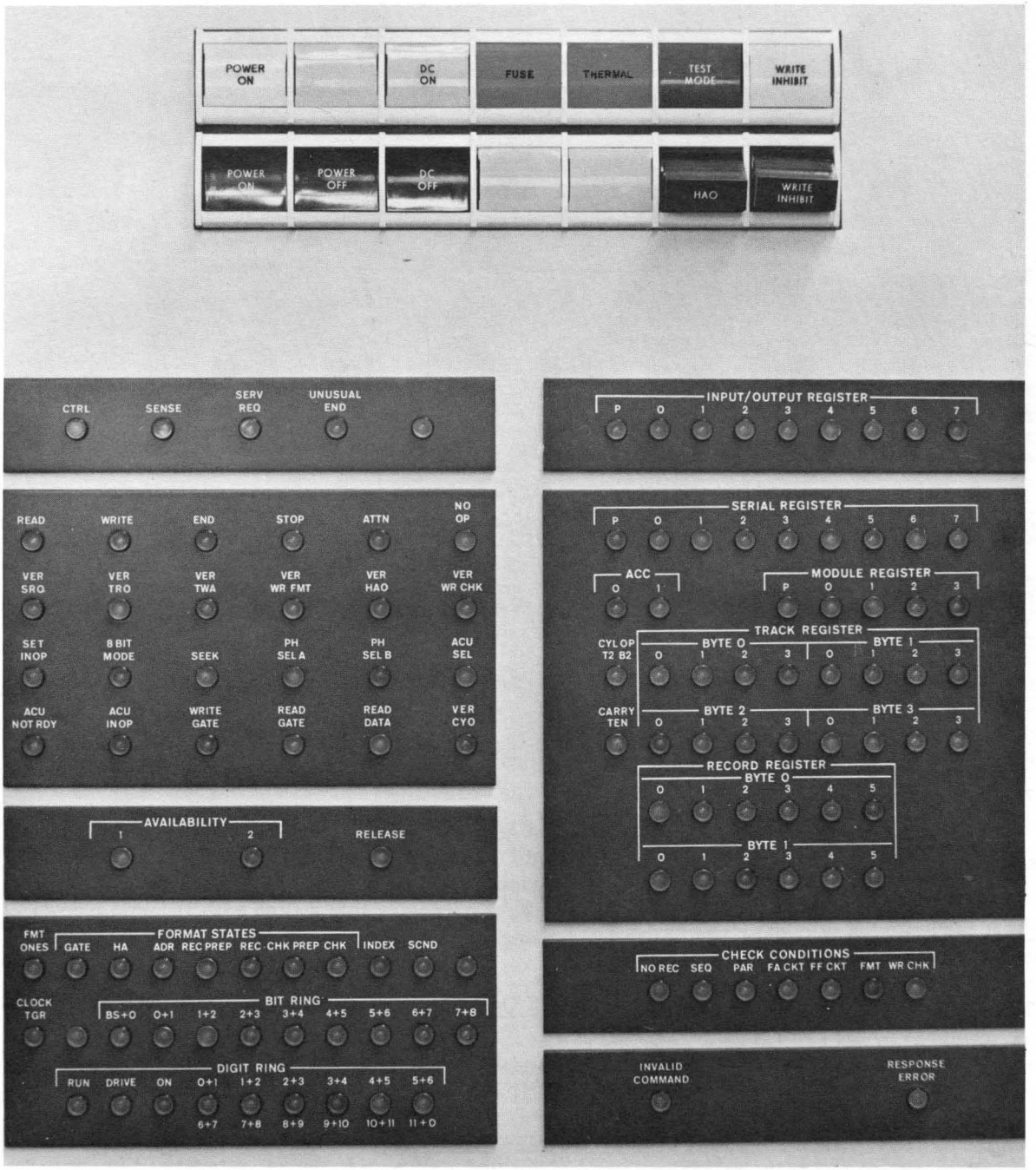


Figure 21. IBM 7631 Model 3 Operator Panel

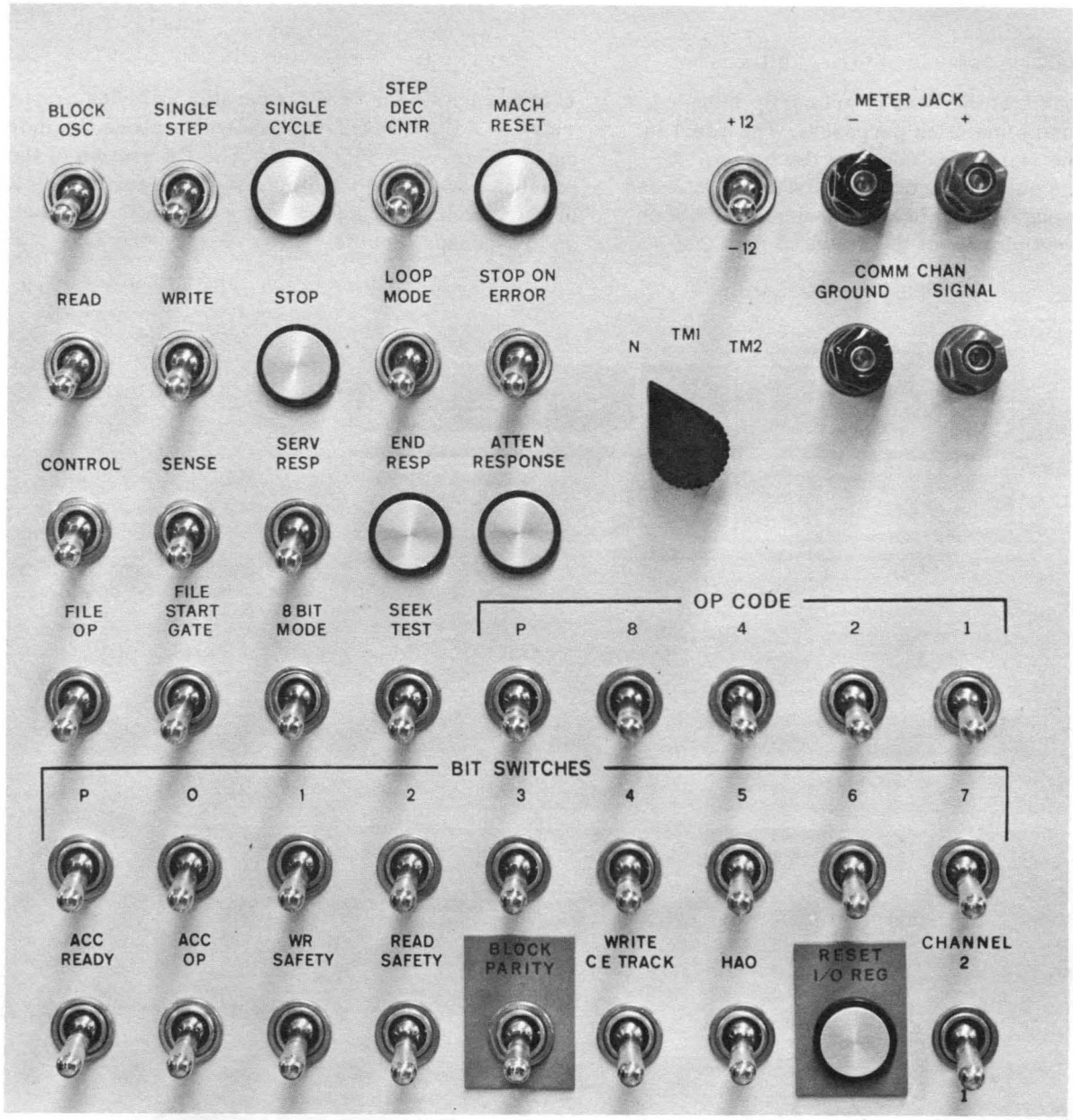


Figure 22. IBM 7631 Model 3 Customer Engineer Panel

OPERATOR'S SWITCH AND LIGHT PANEL

Power On Switch: Depressing this switch causes the following to occur:

1. Apply +12 and -12 volts DC to the IBM 7631.
2. Apply DC voltages to the IBM 1301's if they are set in the CE remote power control.
3. The blower motor in the 7631 to rotate.
4. Sequence AC power to the drive motors and hydraulic power supplies on all 1301 units, one at a time, connected to the 7631. When AC power of the first 1301 is sequenced up, the sequencing of the power to the second 1301 will start. This continues until AC power is sequenced up on all 1301 units connected to the 7631.
5. Depressing this switch with DC power down brings up DC power on the 7631 and 1301.

DC On Light goes on when DC power is on the 7631.

Power On Light goes on when AC power is on in the 7631 and the 1301 in the remote status.

Power Off Switch removes DC and AC power from the 7631 and 1301 except the 24 volts AC. The 24 volts AC power is removed from the 7631 when the power

plug is removed from the wall receptacle or when the main line circuit breaker is thrown off.

HAO Switch allows the execution of the home address operation.

Write Inhibit Switch allows the file control to simulate writing without actually writing on a 1301 file unit.

Write Inhibit Light is on when the write inhibit switch is in the on position.

Test Mode Light is on when the rotary switch on the CE panel is in TM1 or TM2 position.

DC Off Switch causes DC power to be removed from the 7631 and all connected 1301's in the remote status.

Thermal Light indicates that the thermal switch control caused DC power to be removed from the machine. It also lights if the logic gate temperature exceeds 115°F.

Fuse Light indicates that the tripping of AC circuit breaker CB 2 caused DC power to be removed from the machine. The blowing or removal of either of the 1.6 ampere blower fuses stops the blower motor.

NOTE: The 208/24 volt transformer (TB5) is fused with 0.5 ampere slow-blow fuses. When the file control is off-line, power cannot be brought up unless plugs (IBM P/N 553298) are in the two right-hand emergency interlock receptacles on the tailgate.

CUSTOMER ENGINEERING TEST PANEL AND MACHINE INDICATING LAMPS (FIGURE 22)

Block Oscillator Switch prevents the oscillator from driving the bit ring. This switch is activated to drive the bit ring with the single step or single cycle switch.

Single Step Switch allows the bit ring to advance one-half bit each time the single step switch is activated up or down. At the end of each bit ring cycle the digit ring advances one digit if the digit ring run lamp is on. At the end of a control or sense operation the digit ring resets to its initial condition.

Single Cycle Switch causes the machine to advance through a complete cycle of the bit ring and advance the digit ring one digit if the digit ring run lamp is on. At the end of a control or sense operation the digit ring resets to its initial condition.

Rotary Switch in the TM2 position simulates the computer and file lines to the file control. The TM2 position is used to test the file control by itself. This switch in the TM1 position allows simulation of the computer lines to the file control. The TM1 position is used to test the file control with a file. The switch in the normal position is for operation of the file control with a computer and a file. All the CE panel switches except mach reset, write CE track, and HAO must be in the normal position when the CE panel rotary switch is in the N position.

Step Decimal Counter Switch (STEP DEC CNTR): (This switch is used on machines with the CYO operation.) Activating this switch allows single stepping of track registers T2 and T3 until the number 39 is indicated on the CE panel. The CE panel rotary switch must be in the TM1 or TM2 position and the block oscillator switch must be activated. Each flip of the single step switch advances the counter one step.

Machine Reset causes all triggers in the file control to be reset to their initial condition. If the file control is in eight-bit mode, it will change to the six-bit mode.

Read Switch allows reading to be executed in the following modes: home address (HAO), track without addresses (TWA), single record operation (SRO), track operation (TRO), and cylinder operation (CYO)--optional feature.

Write Switch allows writing to be executed in the following modes: home address (HAO), track without addresses (TWA), single record (SRO), track (TRO), CYO (optional feature), and format (the format operation can be performed, but a valid format cannot be written without a system).

Stop Switch terminates the data flow in the file control and turns on the stop lamp. The CE panel rotary switch must be in the TM1 or TM2 position.

Loop Mode Switch allows continuous repetitions of the read or write functions. The CE panel rotary switch must be in the TM1 position.

Stop On Error causes the file control to stop when a check condition occurs. The CE panel rotary switch must be in the TM1 or TM2 position.

Control Switch - (Used on 7631 Models 2, 3, and 4) turns on the control trigger and lamp. The CE panel rotary switch must be in the TM1 or 2 position. The

control switch allows manual operation of all the orders under the control command.

Sense Switch - (Used on 7631 Models 2, 3, and 4) turns on the sense trigger and lamp. The CE panel rotary switch must be in the TM1 or TM2 position. The sense switch allows the data of the ten four-bit bytes of error and attention information to transfer from the status latches to the serial register and then to the input/output register.

Service Response Switch - (Used on 7631 Models 2, 3, and 4) simulates the computer service response. This switch allows the resetting of the service request trigger and lamp. The CE panel rotary switch must be in the TM1 or TM2 position. The service response switch, when the rotary switch is in TM1 position, allows the gating of write data through the file control.

End Response Switch - (Used on 7631 Models 2, 3, and 4) resets the four basic command triggers of read, write, control and sense, the end trigger, and the unusual end trigger. The CE panel rotary switch must be in the TM1 or TM2 position.

Attention Response Switch - (Used on 7631 Models 2, 3, and 4) resets the attention 1 and 2 triggers and the attention lamp. The CE panel rotary switch must be in the TM1 or TM2 position.

Bit Switches activated on the 7631 Models 2, 3, and 4, turns on their respective input register trigger and lamp. The zero-bit switch is not used on 7631 Models 1 and 5. These switches activated on 7631 Model 1 cause its respective serial register trigger and lamp to turn on. The CE panel rotary switch must be in the TM1 or TM2 position.

Write CE Track Switch allows writing on a 1301 inner or outer CE track if the access is located at either of these tracks.

HAO Switch allows reading or writing the physical home address, home address identifier, record addresses and records of the selected head and track with the operator panel HAO switch activated.

Channel 2 Switch - (Used on 7631 Models 1 and 3) allows the file op switch to simulate file operation one. This switch, when transferred, allows the file op switch to simulate file operation two. On 7631 Model 3, the Channel 2 switch must be in Channel 2 position for the file op, file gate start, eight-bit mode, seek test, and op code switches to be active.

The CE panel rotary switch must be in the TM1 or TM2 position.

File Operation Switch - (Used on 7631 Models 1 and 3) with Channel 2 switch in the normal position (7631 Model 1 only) turns on the control trigger and permits the available 1 lamp to turn on. In 7631 Model 3 this switch activated, with Channel 2 switch transferred, allows the available 2 lamp to turn on. The CE panel rotary switch must be in the TM1 or TM2 position for the above conditions.

File Start Gate Switch - (Used on 7631 Models 1 and 3) simulates system 1 or 2, sending the file start gate line to the file control. This switch, used in conjunction with the file op switches, allows completion of the control instructions. The CE panel rotary switch must be in the TM1 or TM2 position. The Channel 2 switch must be in the Channel 2 position for 7631 Model 3.

Eight-Bit Mode Switch - (Used on 7631 Models 1 and 3) causes reading and writing in the eight-bit mode. The eight-bit mode lamp turns on. The CE panel rotary switch must be in the TM1 or TM2 position. The Channel 2 switch must be in the Channel 2 position for 7631 Model 3.

Seek Test Switch - (Used on 7631 Models 1 and 3) simulates a system CPU to file seek test. This switch, used in conjunction with a seek operation, prevents the file access mechanism from moving, turns on the end op trigger and prevents the VER SRO, VER TRO, VER TWA, and VER HAO triggers from being reset. The CE panel rotary switch must be in the TM1 or 2 position. The Channel 2 switch must be in the Channel 2 position for 7631 Model 3.

Op Code Switches - (Used on 7631 Models 1 and 3) allows the proper control operation trigger to turn on. The file start and control triggers must be on and the CE panel rotary switch must be in the TM1 or TM2 position. The Channel 2 switch must be in the Channel 2 position for 7631 Model 3.

+12 and -12 Volt Switch: This switch in the -12 position causes -12 volts to appear at the (-) meter jack and ground to appear at the (+) meter jack. This switch in the +12 position causes ground to appear at the (-) meter jack and +12 volts to appear at the (+) meter jack.

COMMUNICATION CHANNEL JACKS

Ground always appears at the ground test jack. A sync signal sent from the file appears at the signal jack. A check condition causes the unusual end lamp to turn on.

Parity Check: An even number of bits in a byte received by the file control from the computer turns on the parity (PAR) lamp.

Cyclic Code Check: During reading or write check operation, failure to compare check characters for each address and record that were previously written turns on the parity lamp.

Response Check - (Used on 7631 Models 1 and 3): During reading or writing, if a service response is not received within 12 microseconds after a service request in the eight-bit mode, the response error lamp turns on. In the six-bit mode a service response should be received within 8.8 microseconds or the response error lamp turns on.

Data Compare Check: A compare error during a write check operation turns on the WR CHK ERR lamp.

Format Check: During a format write or format check operation any character except BCD 1, BCD 2, BCD 3, and BCD 4 causes the format (FMT) lamp to turn on. The format lamp also turns on if a stop is not sent to the file control 11 characters prior to an early index during these two format operations.

No Record Found: The no record (NO REC) lamp turns on if the file control fails to locate the address issued on the previous control operation.

Access Ready Switch simulates file ready signal from a file. If this switch is activated before the monitor trigger is turned on during a control, read or write operation, the file frame circuit check (FF CKT) lamp turns on. If this switch is activated after the monitor trigger is on, the ACU not ready check cannot occur. The CE panel rotary switch must be in the TM2 position.

Access Operative Switch simulates an access operative line from a file. If this switch is activated after the monitor trigger is on, the ACU not ready check cannot occur. The CE panel rotary switch must be in the TM2 position.

Write Safety Switch simulates the write safety line from a file. The read safety switch activated, with the monitor trigger on when writing, should turn on the file frame circuit check lamp (FF CKT). If the monitor trigger is on prior to both read safety and write safety switches when writing, the FF CKT lamp should turn on. The FF CKT lamp should not turn on when writing with the write safety, access ready, and access operative switches active. The CE Panel rotary switch must be in the TM2 position.

Read Safety Switch simulates the read safety switches line from a file. The write safety switch activated, with the monitor trigger on when reading, should turn on the FF CKT lamp. If the monitor trigger is on prior to both read safety and write safety switches when reading, the FF CKT lamp should turn on. The FF CKT lamp should not turn on when reading with the read safety, access ready, and access operative switches activated. The CE panel rotary switch must be in the TM2 position.

Invalid Sequence - (Used on 7631 Models 2, 3, and 4): The sequence (SEQ) lamp turns on if a write operation is not preceded by a properly executed prepare to verify or prepare to write format order. This lamp also turns on if a prepare to verify order does not precede reading.

Invalid Code: An illegal control order issued to the file control turns on the invalid command lamp.

Access Inoperative: If the file control fails to receive an access operative signal from an addressed access control unit the ACU in op lamp turns on.

Access Not Ready: If the addressed access is in motion from a prior seek order the ACU not ready lamp turns on.

Home Address Check: If a home address operation is attempted without the operator's panel HAO switch activated, the not ready trigger turns on (used on 7631 Models 1 and 3).

File Frame Circuit Check: The FF CKT lamp turns on under the following conditions:

1. Read amplifier failure
2. Write driver failure
3. Access operative line failure from the file to the file control before or after ACU select.
4. A failure of a write operation due to a signal from the format skew detector circuit of the 7631.
5. Ready line failure from the file to the file control before ACU select.

File Adapter Circuit Check: The FA CKT lamp turns on under the following conditions:

1. Out of tolerance gap detection circuit during a write check of a format track.
2. Failure of the address comparison circuitry.
3. Failure of the cyclic code generator.
4. Failure of the format skew detector circuit.
5. Failure of the basic timing rings of the 7631.

APPENDIX

PHYSICAL SPECIFICATIONS

NOTE: Physical specifications are identical for each model of the IBM 7631 File Control, therefore only one value is stated for all models and should be interpreted as applying to all models.

Power Requirement

Power -- Single phase, 3-wire, 60 cycle, 208/230 volts.
Frequency Regulation -- 60 cycle, plus or minus 1/2 cycle.
Voltage Regulation -- Plus or minus 10%, including maximum transient measured at receptacle.

Heat and Power

KVA (60 cycle) -- 1.5
BTU/hr. -- 3550
Power Connectors -- Size -- 30 amp, 250 volts, single phase, 3-wire. Machine end -- Russell & Stoll P/N 3750. Service receptacle -- Russell & Stoll P/N 3933.

Environment

Temperature -- 65° to 90° F.
Humidity -- 10% to 80% R.H.

Dimensions

Weight -- 500 lbs.
Size -- Front 38 inches
Side 32 inches
Height 70 inches

Clearances

Front -- 42 inches; Rear -- 36 inches; Left -- 30 inches; Right -- 30 inches

NOTE: The left side should not be placed adjacent to any non-movable unit or object as access to the left side is occasionally required to service cables.

Grounding

The 1301 Disk Storage is equipped with radio interference control circuitry and requires a good wired earth or building ground. Total resistance of the ground circuit should not exceed 3 ohms. For proper operation, all components of the system or systems to which the 1301 is attached must have the same ground reference. Conduit is not a satisfactory grounding means.

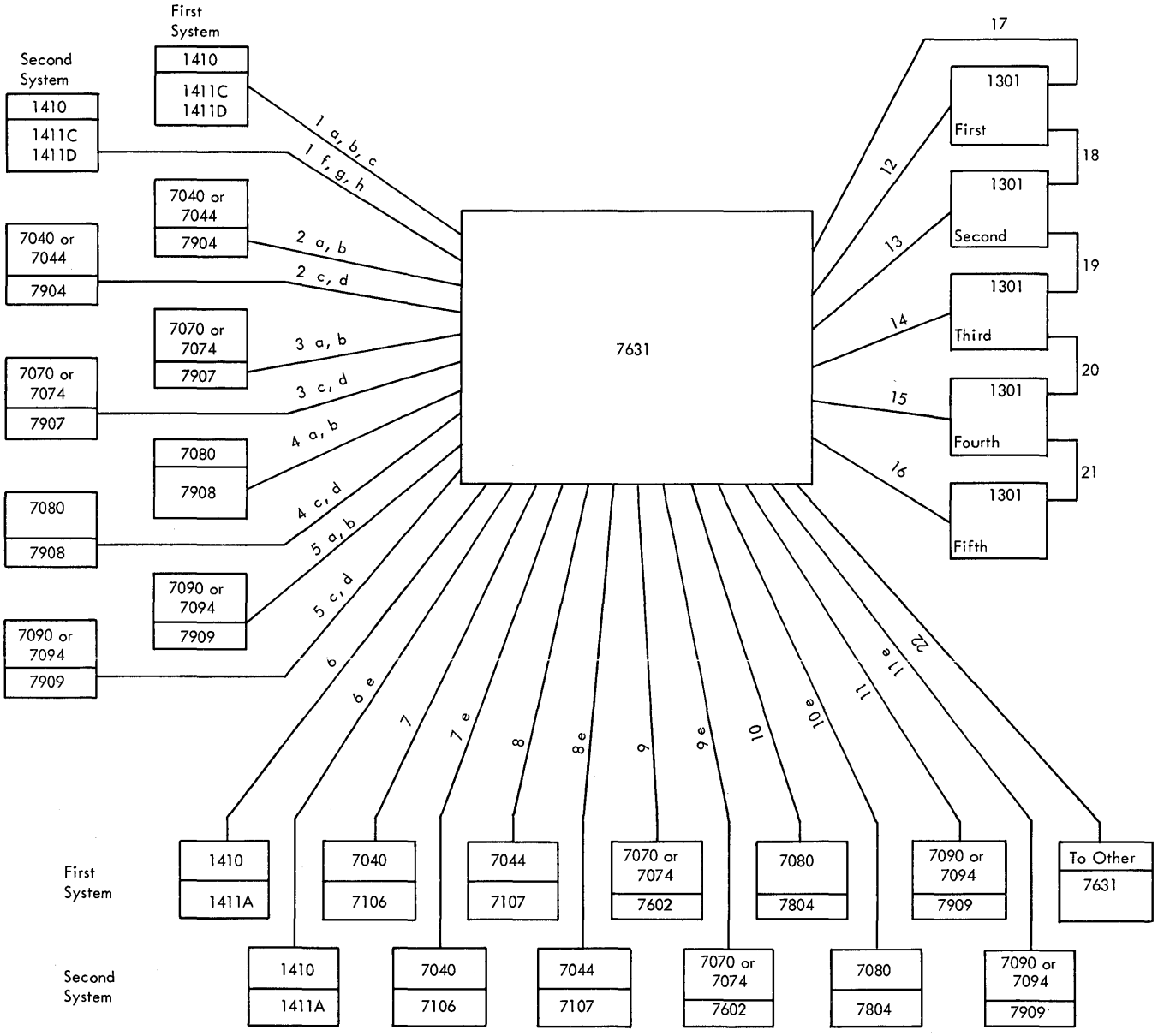


Figure 23. Cable Routings - All Systems

Cable No.	Routing	IBM Part Number[2]	Max. Length in Feet	Notes
1a, b, c/f, g, h	7631 to 1411D	553343	50	
2a, b, c, d	7631 to 7904	587330	50	
3a, b, c, d	7631 to 7907	587330	55	
4a, b, c, d	7631 to 7908	587330	50	
5a, b, c, d	7631 to 7909	587330	50	
6 & 6e	7631 to 1411A	352303	100	
7 & 7e	7631 to 7106	352303	50	
8 & 8e	7631 to 7107	352303	100	
9 & 9e	7631 to 7602	352303	100	
10 & 10e	7631 to 7804	352303	100	
11 & 11e	7631 to 7909	352303	100	
12	7631 to 1301 (1st)	587387	150	
13	7631 to 1301 (2nd)	587387	150	
14	7631 to 1301 (3rd)	587387	150	
15	7631 to 1301 (4th)	587387	150	
16	7631 to 1301 (5th)	587387	150	
17a, b	7631 to 1301 (1st)	553379		1
18a, b	1301 to 1301	553379		1
19a, b	1301 to 1301	553379		1
20a, b	1301 to 1301	553379		1
21a, b	1301 to 1301	553379		1
22	7631 to Other 7631 Unit	352303	100	

1. The maximum total length of these cables in series from 7631 to the last 1301 is 150 feet.
2. Cables listed must be ordered through IBM Sales Representative and will be ordered by appropriate cable key number. Cable part numbers are listed above for design information only.

CABLES AND TERMINATORS

IBM Part Number	Description	Computer End Connectors and Terminals (IBM P/N)	
553343	16-pair twisted wire cable	216076 (1 pos) 216083 (8 pos)	Terminals molded to connector block
587330	20-conductor (20 signal leads and 20 shield leads) 92-ohm coaxial cable	591000	P/N 596224 or 598041 (See Note 1)
352303*	3-pair stranded wire cable	523269	523267
587387	16-conductor (16 signal leads and 16 shield leads) 92-ohm coaxial cable	Not applicable	
553379	16-pair twisted wire cable	Not applicable	

Note 1: The terminal to be used depends on the wire gage/quantity of wires to be terminated per terminal:

IBM P/N 596224 - use with 2-20 gage wires or
2-22 gage wires or
1-16 gage wire or
1-18 gage wire or
1-26 gage wire (requires P/N 596230-stuffer)

IBM P/N 598041 - use with 1-20 gage wire or
1-22 gage wire or
1-24 gage wire

*Emergency Power-Off Cabling

Safety regulations require that the power to all systems components located in a room be turned off by an emergency power-off switch located in a convenient place (normally the computer system console). If a room has more than one computer system, the emergency power-off switch for each system should be able to remove power from the entire room configuration.

Each component is connected in series to other components. When an emergency power-off switch is pressed, a power-control relay in the first unit is released, dropping power and breaking the circuit to the next unit. Each unit in turn has its control circuit broken and power removed.

	1411D Termination Locations						7631			
Drivers/ Terminators	Chan E Signal	TW	Chan F Signal	TW	Lines to Computer	Drivers/ Terminators	System 1 Signal	TW	System 2 Signal	TW
DED -C	U01B	A	U06B	A	Operation Code - C Bit	DEE -C	L-09-02	01	U-13-02	01
DED -C	U01D	C	U06D	C	Operation Code - 8 Bit	DEE -C	L-09-04	03	U-13-04	03
DED -C	U01F	E	U06F	E	Operation Code - 4 Bit	DEE -C	L-09-06	05	U-13-06	05
DED -C	U01H	G	U06H	G	Operation Code - 2 Bit	DEE -C	L-09-08	07	U-13-08	07
DED -C	U01K	J	U06K	J	Operation Code - 1 Bit	DEE -C	L-09-10	09	U-13-10	09
DED -C	U01M	L	U06M	L	Read	DEE -C	L-09-12	11	U-13-12	11
DED -C	U01P	N	U06P	N	Write	DEE -C	L-09-14	13	U-13-14	13
DED -C	U01R	Q	U06R	Q	Load	DEE -C	L-09-16	15	U-13-16	15
DED -C	U02B	A	U04B	A	File Op	DEE -C	L-09-18	17	U-13-18	17
DED -C	U02H	G	U04H	G	Disconnect	DEE -C	L-09-24	23	U-13-24	23
DED -C	L27B	A	U07B	A	Write Data - WM Bit	DEE -C	U-09-02	01	L-13-02	01
DED -C	L27D	C	U07D	C	Write Data - C Bit	DEE -C	U-09-04	03	L-13-04	03
DED -C	L27F	E	U07F	E	Write Data - B Bit	DEE -C	U-09-06	05	L-13-06	05
DED -C	L27H	G	U07H	G	Write Data - A Bit	DEE -C	U-09-08	07	L-13-08	07
DED -C	L27K	J	U07K	J	Write Data - 8 Bit	DEE -C	U-09-10	09	L-13-10	09
DED -C	L27M	L	U07M	L	Write Data - 4 Bit	DEE -C	U-09-12	11	L-13-12	11
DED -C	L27P	N	U07P	N	Write Data - 2 Bit	DEE -C	U-09-14	13	L-13-14	13
DED -C	L27R	Q	U07R	Q	Write Data - 1 Bit	DEE -C	U-09-16	15	L-13-16	15
DED -C	U03B	A	U08B	A	Seek Test	DEE -C	U-11-02	01	L-11-02	01
DED -C	U03H	G	U08H	G	File Start Gate	DEE -C	U-11-08	07	L-11-08	07
DED -C	U03M	L	U08M	L	System Reset	DEE -C	U-11-12	11	L-11-12	11
DFZ -C	U02D	C	U04D	C	End of Address Transfer	DED -C	L-09-20	19	L-13-20	19
DGA -C	U02F	C	U04F	E	End Operation	DED -C	L-09-22	21	L-13-22	21
DGA -C	U02K	J	U04K	J	Ready	DED -C	L-09-26	25	L-13-26	25
DGA -C	U02M	L	U04M	L	Busy	DED -C	L-09-28	27	L-13-28	27
DGA -C	U02P	N	U04P	N	Data Check	DED -C	L-09-30	29	L-13-30	29
DGA -C	U02R	Q	U04R	Q	External Condition	DED -C	L-09-32	31	L-13-32	31
DGA -C	L28B	A	U05B	A	Read - WM Bit	DED -C	U-09-18	17	L-13-18	17
DGA -C	L28D	C	U05D	C	Read - C Bit	DED -C	U-09-20	19	L-13-20	19
DGA -C	L28F	E	U05F	E	Read - B Bit	DED -C	U-09-22	21	L-13-22	21
DGA -C	L28H	G	U05H	G	Read - A Bit	DED -C	U-09-24	23	L-13-24	23
DGA -C	L28K	J	U05K	J	Read - 8 Bit	DED -C	U-09-26	25	L-13-26	25
DGA -C	L28M	L	U05M	L	Read - 4 Bit	DED -C	U-09-28	27	L-13-28	27
DGA -C	L28P	N	U05P	N	Read - 2 Bit	DED -C	U-09-30	29	L-13-30	29
DGA -C	L28R	Q	U05R	Q	Read - 1 Bit	DED -C	U-09-32	31	L-13-32	31
DGA -C	U03D	C	U08D	C	Data Strobe	DED -C	U-11-04	03	L-11-04	03
DFZ -C	U03F	E	U08F	E	Seek Complete	DED -C	U-11-06	05	L-11-06	05
DAC -S	U03P	N	—	—	Write Inhibit	DEW -S	U-11-14	13	L-11-14	13
DAW -S	—	—	U08P	N	Write Inhibit	DEW -S	U-11-14	13	L-11-14	13
Emergency Power Off Interlock			1411D				C3		C2	

7000 Series System to and from 7631 Models 2, 3, and 4

Lines	7000 Series System 1 To/From 7631-2, -3, -4 Drivers/ Terminators	Termination Location Signal	Shield	7000 Series System 2 To/From 7631-4 Drivers/ Terminators	Termination Location Signal	Shield
Operational Out	DEE -C	L-09-02	01	TBH -C	L-13-02	01
Read Command	DEE -C	L-09-04	03	DEE -C	L-13-04	03
Write Command	DEE -C	L-09-06	05	DEE -C	L-13-06	05
Control Command	DEE -C	L-09-08	07	DEE -C	L-13-08	07
Sense Command	DEE -C	L-09-10	09	DEE -C	L-13-10	09
Write Data Bit 0	TBH -C	L-09-14	13	TBH -C	L-13-14	13
Write Data Bit 1	TBH -C	L-09-16	15	TBH -C	L-13-16	15
Write Data Bit 2	TBH -C	L-09-18	17	TBH -C	L-13-18	17
Write Data Bit 3	TBH -C	L-09-20	19	TBH -C	L-13-20	19
Write Data Bit 4	TBH -C	L-09-22	21	TBH -C	L-13-22	21
Write Data Bit 5	TBH -C	L-09-24	23	TBH -C	L-13-24	23
Write Data Bit 6	TBH -C	L-09-26	25	TBH -C	L-13-26	25
Write Data Bit 7	TBH -C	L-09-28	27	TBH -C	L-13-28	27
Write Data Bit Parity	TBH -C	L-09-12	11	TBH -C	L-13-12	11
Service Response	DEE -C	L-09-30	29	TBH -C	L-13-30	29
Stop	DEE -C	L-09-32	31	TBH -C	L-13-32	31
End Response	DEE -C	L-09-34	33	TBH -C	L-13-34	33
Attention Response	DEE -C	L-09-36	35	TBH -C	L-13-36	35
Operational In	DED -C	U-09-02	01	DED -C	U-13-02	01
Command Response	DED -C	U-09-40	39	DED -C	U-13-40	39
Read Data Bit 0	DED -C	U-09-14	13	DED -C	U-13-14	13
Read Data Bit 1	DED -C	U-09-16	15	DED -C	U-13-16	15
Read Data Bit 2	DED -C	U-09-18	17	DED -C	U-13-18	17
Read Data Bit 3	DED -C	U-09-20	19	DED -C	U-13-20	19
Read Data Bit 4	DED -C	U-09-22	21	DED -C	U-13-22	21
Read Data Bit 5	DED -C	U-09-24	23	DED -C	U-13-24	23
Read Data Bit 6	DED -C	U-09-26	25	DED -C	U-13-26	25
Read Data Bit 7	DED -C	U-09-28	27	DED -C	U-13-28	27
Read Data Bit Parity	DED -C	U-09-12	11	DED -C	U-13-12	11
Service Request	DED -C	U-09-30	29	DED -C	U-13-30	29
End	DED -C	U-09-32	31	DEC -C	U-13-32	31
Unusual End	DED -C	U-09-38	37	DED -C	U-13-38	37
Attention	DED -C	U-09-36	35	DED -C	U-13-36	35
Emergency Power Off Interlock		C3			C2	

IBM 7631 to and from IBM 1301

7631 Term	Shield/ TW	Terminator/ Driver	Line Name	Driver/ Terminator	1301 Term	Shield/ TW
U-03-22	21	TBH -C	Format Read Data (FF1)	DED -C	11D22	21
U-03-18	17	TBH -C	Read Data (FF1)	DED -C	11D18	17
U-01-02	01	TDB -C	Access Ready	TAB -C	05D02	01
U-01-18	17	TDB -C	Early Index	TAB -C	05D18	17
U-01-20	19	TDB -C	Late Index	TAB -C	05D20	19
U-01-08	07	TDB -C	Write Safety	TAB -C	05D08	07
U-01-06	05	TDB -C	Read Safety	TAB -C	05D06	05

7631 Term	Shield/ TW	Terminator/ Driver	Line Name	Driver/ Terminator	1301 Term	Shield/ TW
U-03-02	01	TBH -C	Access 0 Module 0 (FF1)	TDB -C	11D02	01
U-03-04	03	TBH -C	Access 0 Module 1 (FF1)	TDB -C	11D04	03
L-03-24	23	TDB -C	Communication Channel to FCU	TAB -C	07D24	23
U-01-04	03	TDB -C	Access Operative	TAB -C	05D04	03
U-01-22	21	TDB -C	CE Track	TAB -C	05D22	21
L-03-16	15	--- C	30 vdc	--- C	07D16	--
U-03-24	23	TES -C	Clock A (FF1)	TES -C	11D24	23
U-03-28	27	TES -C	Clock B (FF1)	TES -C	11D28	27

FF1 = File Frame 1 only

7631 Models 1, 2, 3, 4, and 5 to IBM 1301

7631 Term	Shield TW	Driver	Line Name	Terminator	Location	Shield TW
L-01-08	07	TAB	T0 B0	TDB	09DB8	07
L-01-06	05	TAB	T0 B1	TDB	09D06	05
L-01-04	03	TAB	T0 B2	TDB	09D04	03
L-01-02	01	TAB	T0 B3	TDB	09D02	01
L-01-16	15	TAB	T1 B0	TDB	09D16	15
L-01-14	13	TAB	T1 B1	TDB	09D14	13
L-01-12	11	TAB	T1 B2	TDB	09D12	11
L-01-10	09	TAB	T1 B3	TDB	09D10	09
L-01-24	23	TAB	T2 B0	TDB	09D24	23
L-01-22	21	TAB	T2 B1	TDB	09D22	21
L-01-20	19	TAB	T2 B2	TDB	09D20	19
L-01-18	17	TAB	T2 B3	TDB	09D18	17
L-01-32	31	TAB	T3 B0	TDB	09D32	31
L-01-30	29	TAB	T3 B1	TDB	09D30	29
L-01-28	27	TAB	T3 B2	TDB	09D28	27
L-01-26	25	TAB	T3 B3	TDB	09D26	25
U-03-30	29	TAB	Module 0 (FF1)	TDB	11D30	29
U-03-32	31	TAB	Module 1 (FF1)	TDB	11D32	31
U-03-20	19	DED	Write Data (FF1)	DFZ	11D20	19
L-03-02	01	TAB	Access Zero	TDB	07D02	01
U-01-12	11	TAB	Access Register (Set Track)	TDB	05D12	11
U-01-14	13	TAB	Access Register (Set Head)	TDB	05D14	13
L-03-28	27	TAB	Data AGC (Squelch)	TDB	07D28	27
L-03-30	29	TAB	Store Format	TDB	07D30	29
L-03-32	31	TAB	Write Gate	TDB	07D32	31
L-03-18	17	TAB	Flag 1	TDB	07D18	17
L-03-20	19	TAB	Flag 2	TDB	07D20	19
L-03-22	21	TAB	Flag 3	TDB	07D22	21
U-01-16	15	TAB	Head Select	TDB	05D16	15
U-01-24	23	TAB	Set Access Inoperative	TDB	05D24	23
U-01-26	25	TAB	Communication Chan from FCU	TDB	05D26	25
U-01-30	29	---	24 vac Common	---	05D30	29
L-03-06	05	---	Power On	---	07D06	05
L-03-12	11	---	Emergency Off	---	07D12	11
L-03-14	13	---	Power Sequence Common	---	07D15	--
L-03-10	09	---	DC Power Set	---	07D10	09
U-01-28	27	---	Start-Stop Sequence	---	05D28	27

Drivers from 7000 Series Data Channels to 7631

7040-7044		7070-7074			7080		7090-7094		
Driver/ Sym	Terminal Location 7904-1	Driver/ Channel 1 Ext 1	Ext 2/Sym	Terminal Location 7907 Channel 1 Extender 1	Driver/ Sym	Terminal Location 7908 Chan 40	Driver/ Sym	Terminal Location 7909	Lines From Computer
DQJ -C	L-01-02	TCN	TCN -C	H-13C-02	SZT -C	U-05-02	DED -C	L-01-02	Operational Out
UCL -C	L-01-04	TCN	TCN -C	H-13C-04	SZX -C	U-05-04	DED -C	L-01-04	Read Command
UCL -C	L-01-06	TCN	TCN -C	H-13C-06	SZX -C	U-05-06	DED -C	L-01-06	Write Command
UCL -C	L-01-08	TCN	TCN -C	H-13C-08	SZX -C	U-05-08	DED -C	L-01-08	Control Command
UCL -C	L-01-10	TCN	TCN -C	H-13C-10	SZX -C	U-05-10	DED -C	L-01-10	Sense Command
UCL -C	-------	TCN	SHM -C	H-13C-14	SYB -C	U-05-14	DED -C	L-01-14	Write Data Bit 0
UCL -C	-------	TCN	SHM -C	H-13C-16	SYB -C	U-05-16	DED -C	L-01-16	Write Data Bit 1
UCL -C	L-01-18	TCN	SHM -C	H-13C-18	SYB -C	U-05-18	DED -C	L-01-18	Write Data Bit 2
UCL -C	L-01-20	TCN	SHM -C	H-13C-20	SYB -C	U-05-20	DED -C	L-01-20	Write Data Bit 3
UCL -C	L-01-22	TCN	SHM -C	H-13C-22	SYB -C	U-05-22	DED -C	L-01-22	Write Data Bit 4
UCL -C	L-01-24	TCN	SHM -C	H-13C-24	SYB -C	U-05-24	DED -C	L-01-24	Write Data Bit 5
UCL -C	L-01-26	TCN	SHM -C	H-13C-26	SYB -C	U-05-26	DED -C	L-01-26	Write Data Bit 6
UCL -C	L-01-28	TCN	SHM -C	H-13C-28	SYB -C	U-05-28	DED -C	L-01-28	Write Data Bit 7
UCL -C	L-01-12	TCN	SHM -C	H-13C-12	SYB -C	U-05-12	DED -C	L-01-12	Write Data Bit Parity
UCL -C	L-01-30	TCN	SHM -C	H-13C-30	SYB -C	U-05-30	DED -C	L-01-30	Service Response
UCL -C	L-01-32	TCN	TCN -C	H-13C-32	UAP -C	U-05-32	DED -C	L-01-32	Stop
UCL -C	L-01-34	TCN	SHM -C	H-13C-34	SZU -C	U-05-34	DED -C	L-01-34	End Response
UCL -C	L-01-36	TCN	TCN -C	H-13C-36	UAB -C	U-05-36	DED -C	L-01-36	Attention Response

Terminators at 7631 from 7000 Series Data Channels

7040-7044		7070-7074			7080		7090-7094		
Terminator Sym	Terminal Location 7904	Terminator Ext 1	Ext 2/Sym	Terminal Location 7907 Chan 1 Extender 1	Terminator Sym	Terminal Location 7908 Chan 40	Terminator Sym	Terminal Location 7909	Lines to Computer
UCH -C	L-05-02	TDL	TDL -C	H-09C-02	SZT -C	U-01-02	DEE -C	U-01-02	Operational In
UCH -C	L-05-40	SHU	SHU -C	H-09C-40	SZZ -C	U-01-40	DEE -C	U-01-40	Command Response
UCG -C	-------	SHU	SHU -C	H-09C-14	SYK -C	U-01-14	DEE -C	U-01-14	Read Data Bit 0
UCG -C	-------	SHU	SHU -C	H-09C-16	SYK -C	U-01-16	DEE -C	U-01-16	Read Data Bit 1
UCG -C	L-05-18	SHU	SHU -C	H-09C-18	SYK -C	U-01-18	DEE -C	U-01-18	Read Data Bit 2
UCG -C	L-05-20	SHU	SHU -C	H-09C-20	SYK -C	U-01-20	DEE -C	U-01-20	Read Data Bit 3
UCG -C	L-05-22	SHU	SHU -C	H-09C-22	SYK -C	U-01-22	DEE -C	U-01-22	Read Data Bit 4
UCG -C	L-05-24	SHU	SHU -C	H-09C-24	SYK -C	U-01-24	DEE -C	U-01-24	Read Data Bit 5
UCG -C	L-05-26	SHU	SHU -C	H-09C-26	SYK -C	U-01-26	DEE -C	U-01-26	Read Data Bit 6
UCG -C	L-05-28	SHU	SHU -C	H-09C-28	SYK -C	U-01-28	DEE -C	U-01-28	Read Data Bit 7
UCG -C	L-05-12	SHU	SHU -C	H-09C-12	SYK -C	U-01-12	DEE -C	U-01-12	Read Data Bit Parity
UCH -C	L-05-30	SHU	SHU -C	H-09C-30	UAF -C	U-01-30	DEE -C	U-01-30	Service Request
UCH -C	L-05-32	SHU	SHU -C	H-09C-32	SZU -C	U-01-32	DEE -C	U-01-32	End
UCH -C	L-05-38	SHU	SHU -C	H-09C-38	SZU -C	U-01-38	DEE -C	U-01-38	Unusual End
UCH -C	L-05-36	TDL	TDM -C	H-09C-36	UAB -C	U-01-36	DEE -C	U-01-36	Attention
7106 (7040) 7107 (7044)				7602		7804		7909	Emergency Power Off Interlock

Cabling Notes

7040-7044 System: The 7904-2 contains two channels. Identical cabling and block terminations are used for channel 1 in the 7904-2 as in the 7904-1. Channel 2 in the 7904-2 uses terminal blocks 45L and 49L, respectively. The terminal position on each block remains the same regardless of model or channel.

7070-7074: The 7070 and 7074 systems have a capacity of four channels, with two channel extenders per channel. The terminal blocks used on the 7907 are:

		To 7631	From 7631
Channel 1	Extender 2	H 21 C	H 17 C
Channel 2	Extender 1	H 01 C	H 01 B
Channel 2	Extender 2	H 05 C	H 05 B
Channel 3	Extender 1	H 21 A	H 17 A
Channel 3	Extender 2	H 29 A	H 25 A
Channel 4	Extender 1	H 05 A	H 01 A
Channel 4	Extender 2	H 13 A	H 09 A

The individual terminal position on each block remains the same regardless of channel or extender designation.

7080: The IBM 7908 has a capacity of six channels, two high-speed channels (channel numbers 40 and 41) and four low-speed channels (channel numbers 44, 45, 46, 47). The following terminal blocks are assigned in addition to the listed channel 40.

	From 7631	To 7631
Channel 41	U 09	U 13
Channel 44	U 17	U 21
Channel 45	U 25	U 29
Channel 46	U 33	U 37
Channel 47	U 41	U 45

The individual terminal position on each block remains the same regardless of channel designation.

All driver/terminator circuits are the same for each respective line for both high- and low-speed channels with the exception of read data bit parity, which uses circuit SZS on the low-speed channels. Additionally, due to circuit packaging, the printed wire card codes differ between the low-speed and high-speed channels as follows:

	High-Speed Channel	Low-Speed Channel
Service Response	SYB	UAK
Stop	UAP	UAK
Read Data Bits (All)	SYK	SZS
Service Request	UAF	UAY

7090-7094: The 7090 and 7094 systems provide a data channel switch optional feature for the assignment of a second 7631 to the 7090-7094 system. The second 7631 is connected to the 7909 at terminal block locations U 05 (from 7631) and L 05 (to 7631). The individual terminal positions remain the same for the second 7631.

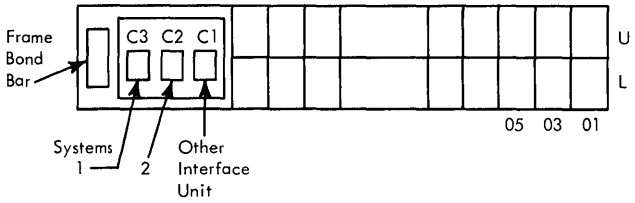


Figure 24. IBM 7631 Terminal Block Locations

7631 Model Number	Cable Number	Connector Position 1st System	Connector Position 2nd System
I	1a 1b 1c	U-11 U-09 L-09	------ ------ ------
II	2a,3a,4a,5a 2b,3b,4b,5b	L-09 U-09	------ ------
III	1f 1g 1h 2a,3a,4a,5a 2b,3b,4b,5b	------ ------ ------ L-09 U-09	U-15 L-13 U-13 ------ ------
IV	2a,3a,4a,5a 2c,3c,4c,5c 2b,3b,4b,5b 2d,3d,4d,5d	L-09 ------ U-09 ------	------ L-13 ------ U-13
V	1a, - 1f 1b - 1g 1c - 1h	U-11 U-09 L-09	L-11 L-13 U-13

Figure 25. IBM 7631 Cable Connector Chart

Cable Numbers	Channel	Unit	Connector Frame	Position Level	Block
1a or 1f	E	1411	D	U	03
1b or 1g	E	1411	C	L	27
		1411	C	L	28
1c or 1h	E	1411	D	U	01
		1411	D	U	02
1a or 1f	F	1411	D	U	08
1b or 1g	F	1411	D	U	07
		1411	D	U	05
1c or 1h	F	1411	D	U	06
		1411	D	U	04

Figure 26. IBM 1410 Cable Connector Chart

FILE CONTROL STATUS WORD

Error Status

Byte Number	Read Bus Position	Assignment	Comment
	0		
	1		
	2		
	3	Operator Intervention Req'd	Summary
0	4		Byte
	5	Program check	
	6	Data Check	
	7	Exceptional Condition	
	0		
	1		
	3	Invalid Sequence	Program Check
1	4		
	5	Invalid Code	Program Check
	6	Format Check	Program Check
	7	No Record Found	Program Check
	0		
	1		
	2		
	3	Invalid Address	Program Check
2	4		
	5	Response Check	Data Check
	6	Data Compare Check	Data Check
	7	Parity or Cyclic Code Check	Data Check
	0		
	1		
	2		
	3	Access Inoperative	Excep Cond
3	4		
	5	Access Not Ready	Excep Cond
	6	File Frame Circuit Check	Excep Cond
	7	File Adapter Circuit Check	Excep Cond

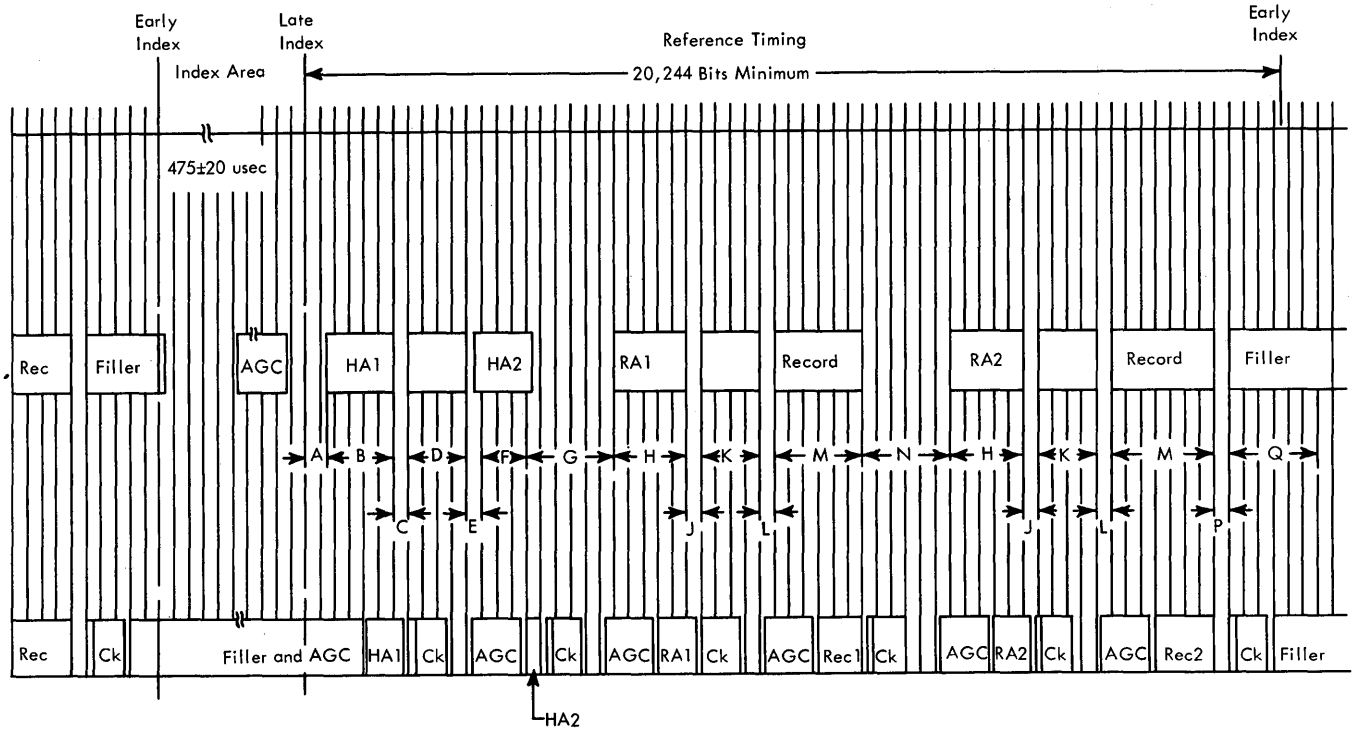
Optional Features

Byte Number	Read Bus Position	Assignment	Comment
	0		
	1		
	2		
	3	Channel Interrupt	Optional
4	4		
	5	Six-Bit Mode	Data Mode
	6	Unassigned	
	7	Unassigned	

Attention Status

Byte Number	Read Bus Position	Assignment	Comment
	0		
	1		
	2		
	3	Access 0, Module 0	Attention
5	4		
	5	Access 0, Module 1	Attention
	6	Access 0, Module 2	Attention
	7	Access 0, Module 3	Attention
	0		
	1		
	2		
	3	Access 0, Module 4	Attention
6	4		
	5	Access 0, Module 5	Attention
	6	Access 0, Module 6	Attention
	7	Access 0, Module 7	Attention
	0		
	1		
	2		
	3	Access 0, Module 8	Attention
7	4		
	5	Access 0, Module 9	Attention
	6		
	7		
	0		
	1		
	2		
	3		
8	4		
	5		
	6		
	7		
	0		
	1		
	2		
	3		
9	4		
	5		
	6		
	7		

FORMAT TRACK



AGC - Automatic Gain Control Burst of "One" Bits
RA - Record Address
HA - Home Address
Rec - Record
Ck - Check Characters
HA1 - Physical Track and Head Address Portion of Home Address
HA2 - Home Address Identifier

Scale: 2 Characters per Graduation

Figure 27. Format Track Layout

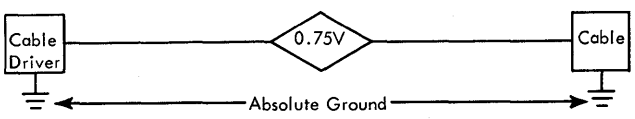
DESIGN CONSIDERATIONS FOR CABLE DRIVERS AND TERMINATORS

1. Cable drivers must be able to drive up to a maximum of 100 feet of coaxial cable and 50 feet of twisted wire cable.

2. A power-off condition at either end of the cable between the computer and the IBM 7631 must not cause any electrical damage.

3. Shorts of cable pins to ground must not be destructive.

4. Ground shift plus line drop between the cable driver and the cable terminator is 0.75 volts. This 0.75 volts should be considered as a voltage generator existing internally in the cable.



5. Cable termination must be between 90 and 100 ohms.

6. With an input to the terminator disconnected, an "up" level must be present at the input and must not exceed +2.35 volts. The "up level" is the off state.

7. With an input to the terminator going from the down to the up level, the terminator must be designed to switch at a level equal to or less than +0.65 volts.

8. In the up level, the cable driver appears as a current source. The terminator must be capable of accepting 0.1 ma. DC leakage.

9. The cable driver output, in the up level, should have the characteristics of a high impedance current source. It must not be greater than 0.1 ma. at its output. In worst case condition, the cable driver must be capable of seeing the following load:

10. The minimum signal pulse duration to a terminator coming from the computer must be 0.5 usec.
11. The pulse repetition rate must be between 0 and 625 KC.
12. The output of the cable driver must be capable of meeting the following worst case condition:

-c lines (down level, on state)	-1.12 volts at 31.6 ma.	
-s lines (down level, on state)	Minimum -6.87 volts at 4.4 ma	Maximum -12.48 volts

"M" in schematics = Marginal.
12M can be varied ±1.5 volts in 7631.

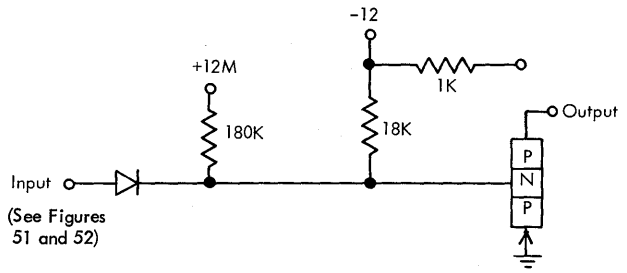


Figure 30. Terminator (TDB)

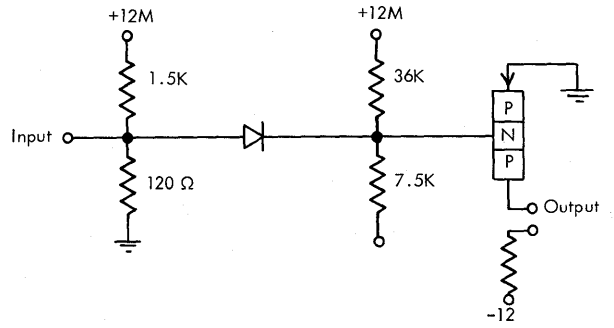


Figure 31. Terminator (DEE)

CIRCUITS -- DRIVERS AND TERMINATORS

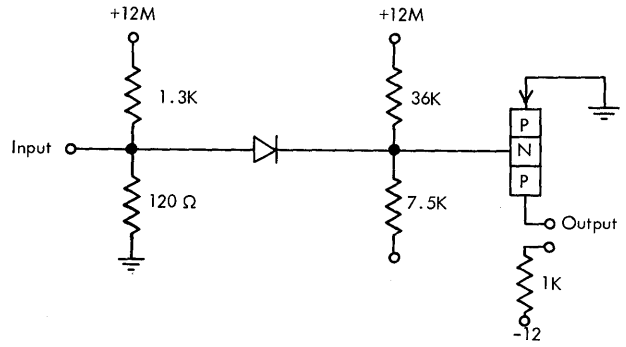


Figure 28. Terminator (TBH)

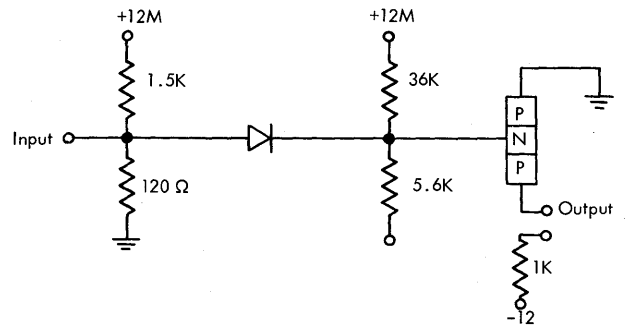


Figure 29. Terminator (TDM)

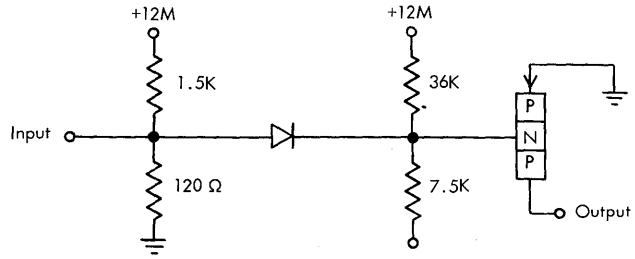


Figure 32. Terminator (DGA)

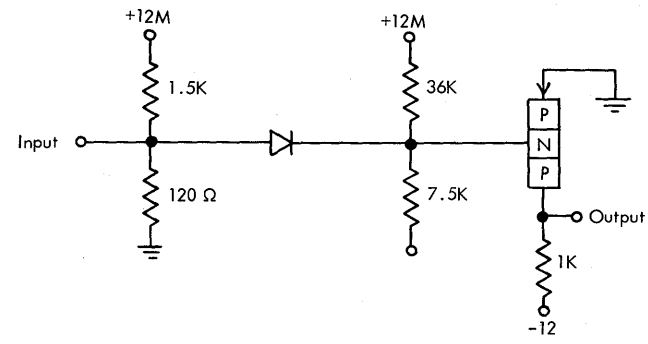


Figure 33. Terminator (DFZ)

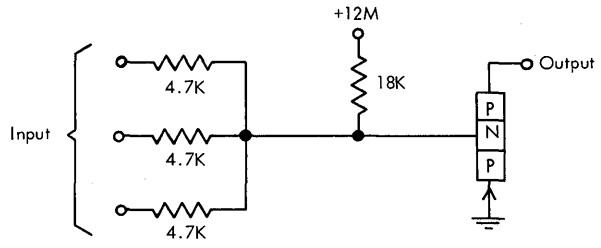


Figure 34. Terminator (DAW)

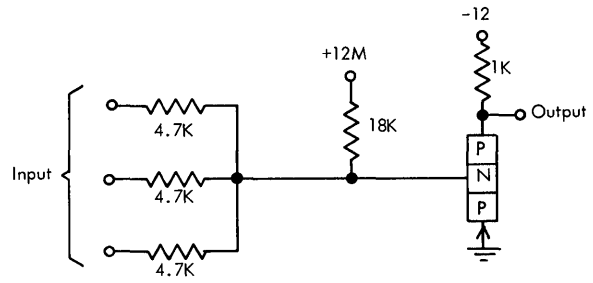


Figure 35. Terminator (DAC)

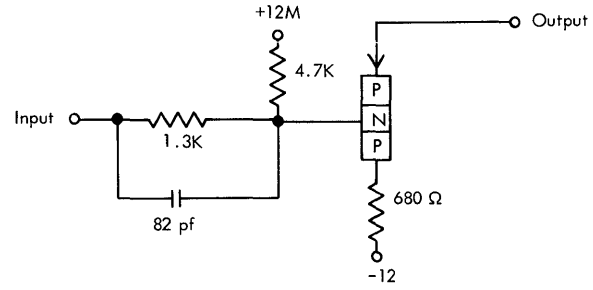


Figure 36. Driver (DED)

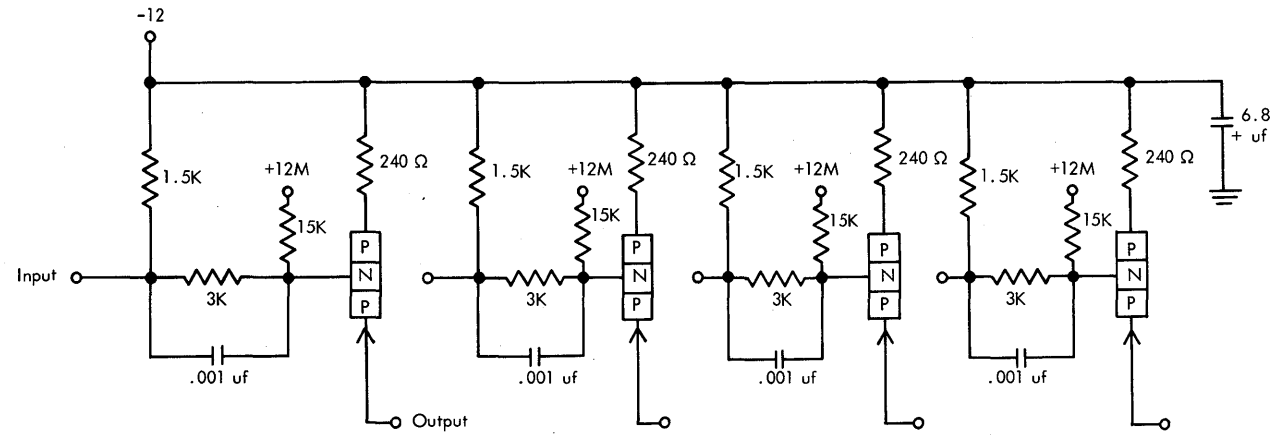


Figure 39. Line Driver - Dispersed Load (TAB)

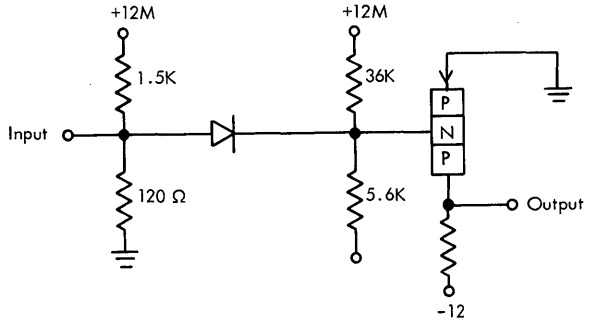


Figure 37. Terminator (TDL)

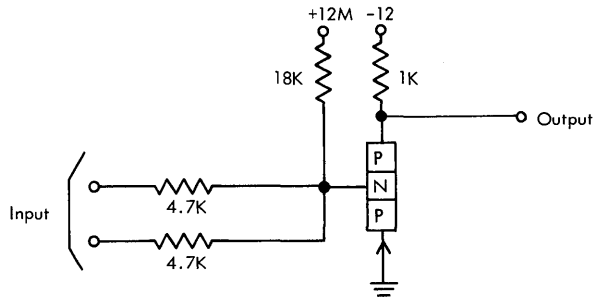


Figure 38. Terminator (DEW)

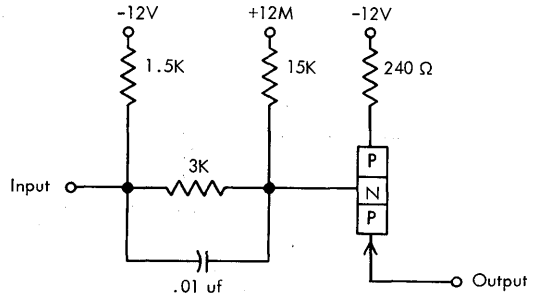


Figure 40. Line Driver (SHM)

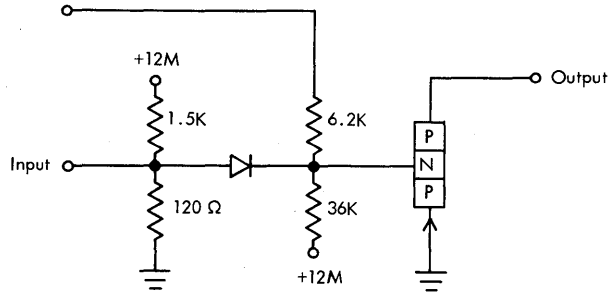


Figure 41. Terminator (SHU)

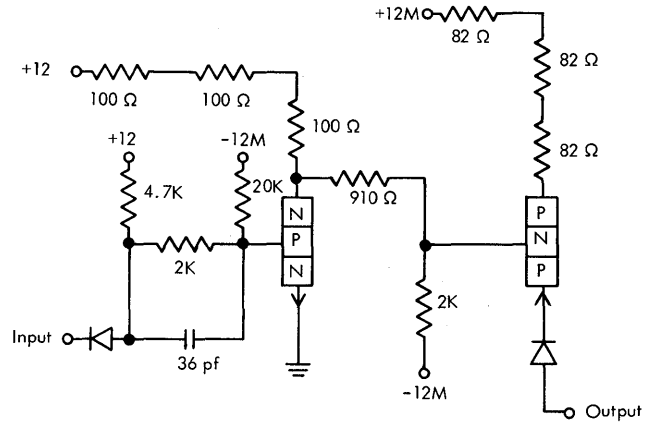


Figure 42. Driver (DQJ)

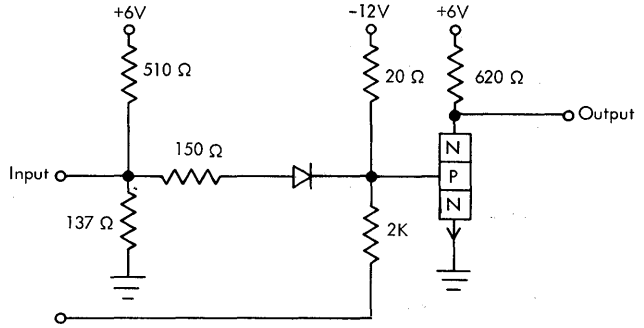


Figure 43. Line Terminator (UAB)

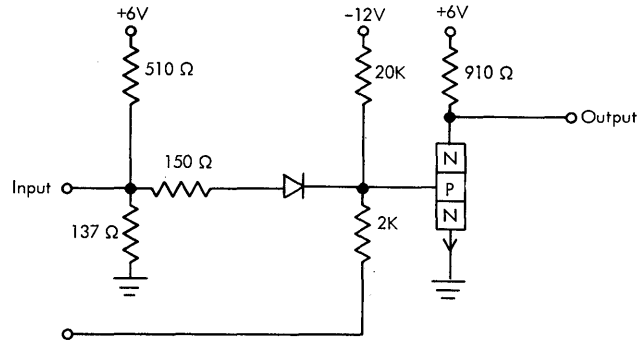


Figure 44. Line Terminator (SZS)

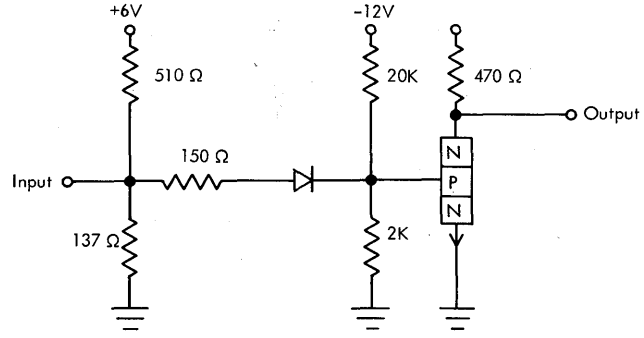


Figure 45. Line Terminator (SYK, UAF, SZU, UAY, SZZ)

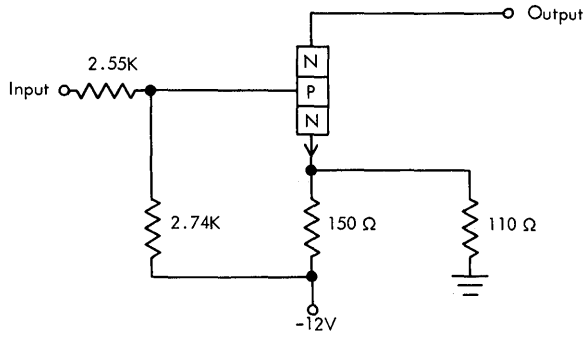


Figure 46. Line Driver (SZX, UAD, SYB, SZT, UAK)

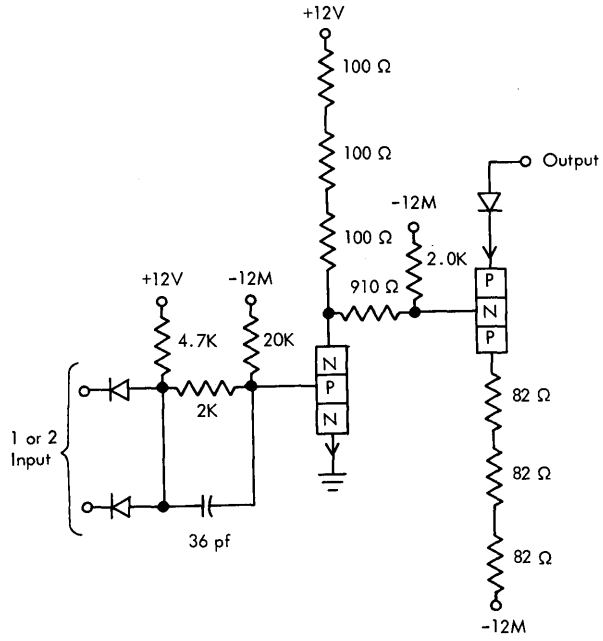


Figure 47. Driver (UCL)

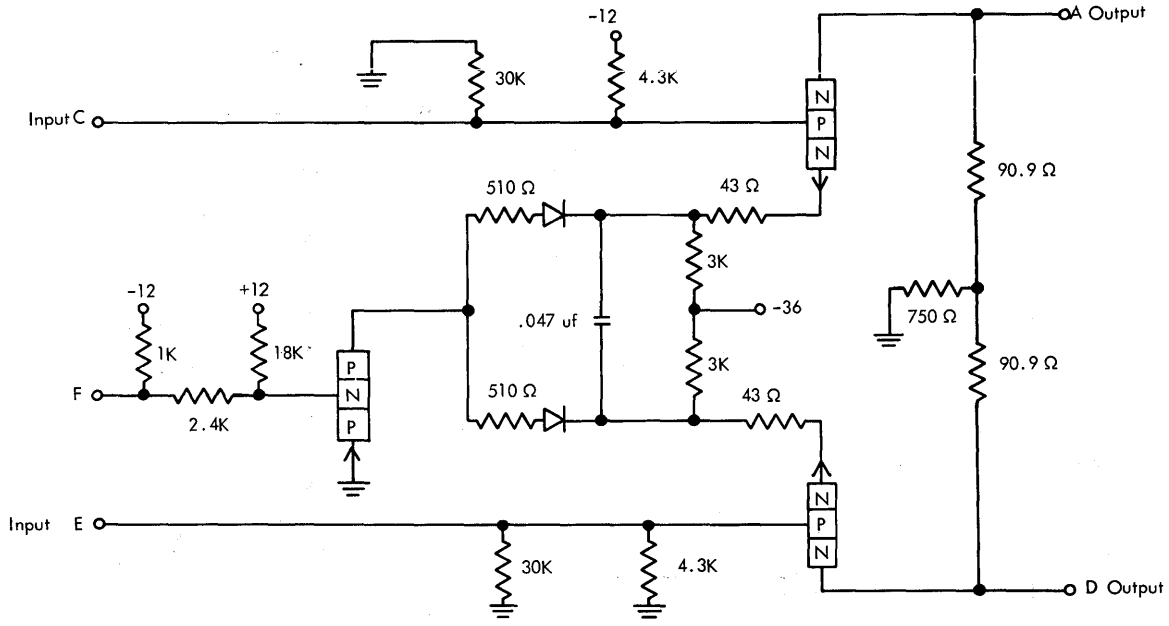


Figure 48. Line Driver (TEJ)

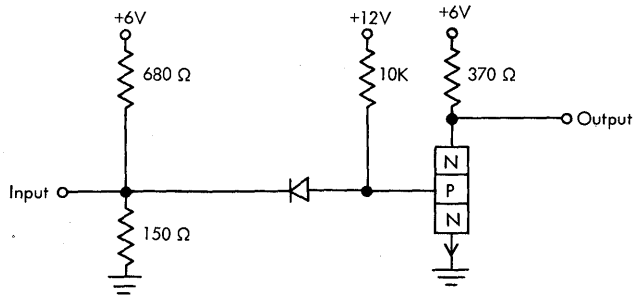


Figure 49. Terminator (UCG, UCH)

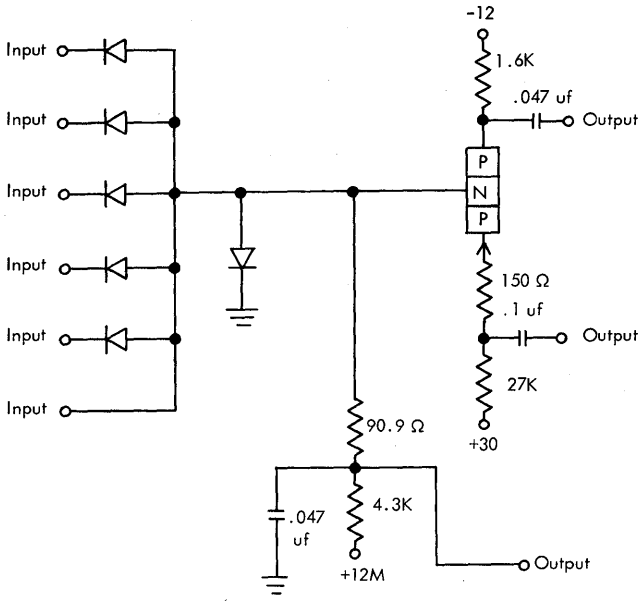


Figure 51. Terminator (TES)

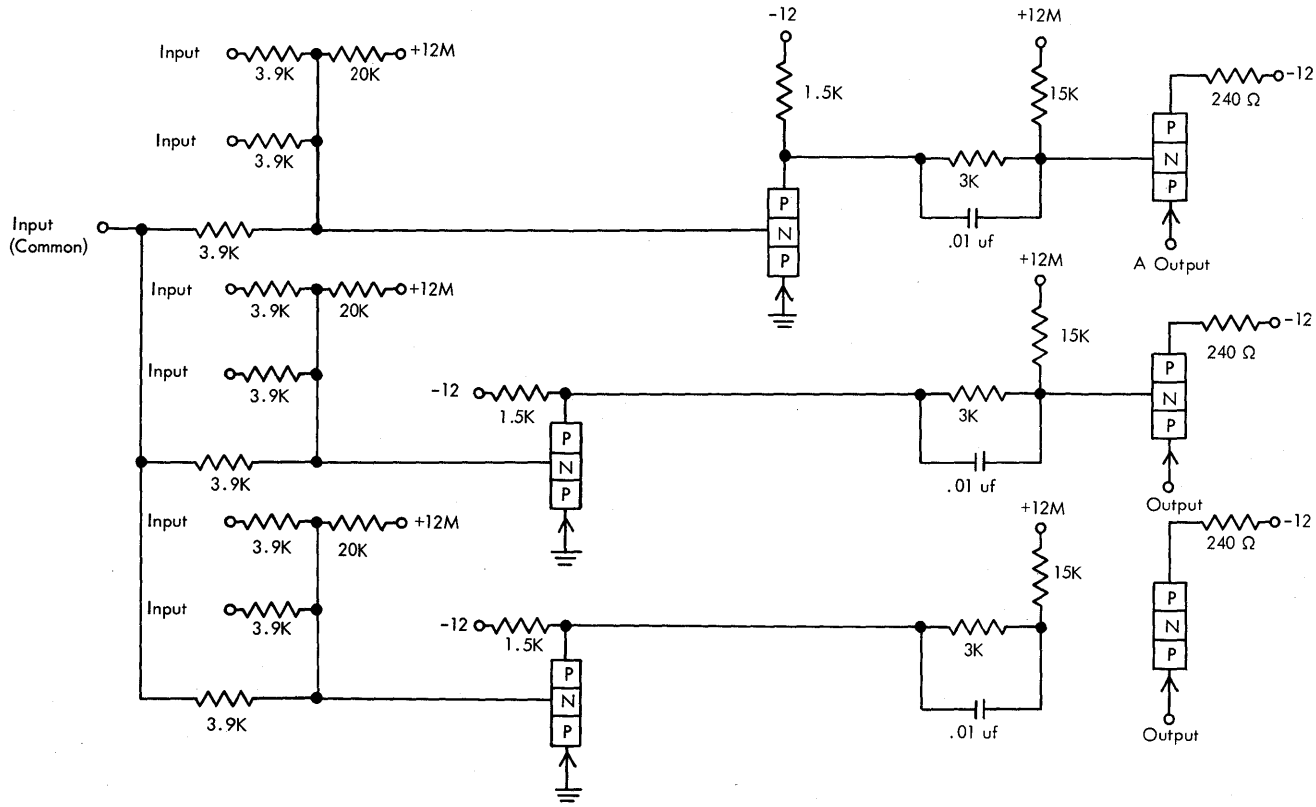


Figure 50. Line Driver (TCN)

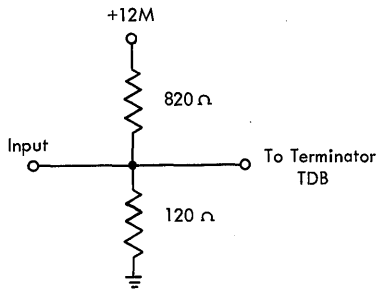


Figure 51. End of Line Terminator (TCK)

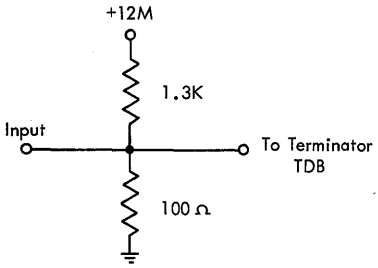


Figure 52. End of Line Terminator (TAC)

2/63:3M-H-68

A22-6725

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IBM

International Business Machines Corporation
Data Processing Division
112 East Post Road, White Plains, New York