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IBM Series/1
Synchronous Data Link Control
Communications Feature
Description

Preface

This publication describes the Synchronous Data Link Control Communications Feature. The reader should be an experienced Series/1 assembler-language programmer who writes, maintains, and debugs machine-level-language programs. The reader should also be familiar with binary and hexadecimal numbering systems, and stored-program concepts.

The subject matter is presented in two chapters and three appendices:

- Chapter 1 introduces the synchronous data link control communications feature.

- Chapter 2 describes the Series/1 machine-level language that the processor uses to transfer data to and from the attachment. It also describes attachment operation as related to Series/1 interface (command/interrupts), link protocol, and jumperable options.

- Appendix A contains a summary of the commands, device control blocks (DCB), cycle-steal status words, and condition codes associated with the attachment feature.

- Appendix B describes the operator self-test to be used to verify attachment operation.

- Appendix C shows an example of adapter initialization.

Prerequisite Publications

- *IBM Series/1 Principles of Operation*, GA34-0152.

- Refer to *IBM Series/1 Graphic Bibliography*, GA34-0055, for the name and order number of the appropriate feature description manual for your processor.

Related Publications

- *IBM Series/1 System Selection Guide*, GA34-0143.

- *IBM Series/1 Customer Site Preparation Manual*, GA34-0050.

- *IBM Series/1 Pocket Digest*, GX34-0104.

- *IBM Synchronous Data Link Control General Information*, GA27-3093.

- *Data Communication-HDLC Procedures-Frame Structure*, IS 3309

- *Data Communication-HDLC Procedures-Elements of Procedures*, DIS 4335 and Amendments

Contents

Chapter 1. Introduction

This chapter provides an overview of the IBM Series/1 Synchronous Data Link Control Feature.

The single-line control feature provides circuitry for one half-duplex communication line that can process bit rates of up to 19.2K bits per second (bps). The synchronous data link control (SDLC) feature operates as a primary station or a secondary station but provides no initial program load (IPL) capability. This attachment also supports High-Level Data Link Control (HDLC).

The SDLC feature controls the serial transfer of data to and from remote terminals or host systems by using modems and communication line facilities. The SDLC feature allows a Series/1 processor to communicate with telecommunication equipment or other processors with compatible adapters. The following communication characteristics apply to the SDLC feature:

- Data transmission uses SDLC procedures.

- The feature can communicate with host systems or terminals using Extended Binary Coded Decimal Interchange Code (EBCDIC), American Standard Code for Information Interchange (ASCII), or any other 8-bit data code.

- The attachment is a single-line, medium-speed, half-duplex device that can operate on switched or nonswitched lines. However, two attachment cards may be used together, one as a transmitter the other as a receiver, to operate in a duplex environment. The two attachments must be installed in consecutive I/O card slots in the processor enclosure or I/O expansion unit.

- Bit rates of up to 19.2K bps with external clocking.

- It can be used as a primary or secondary station or as a combined station, if two attachments are used.

- Internal clocking is available with bit rates of 600 bps or 1,200 bps.

- Nonreturn-to-zero-inverted (NRZI) coding is used with internal clocking.

- Nonreturn-to-zero (NRZ) coding or NRZI coding can be used with external clocking.

- Installing a jumper on the attachment card provides answer-tone.

- The attachment does not support station address field extensions or control field extensions.

Configurations

The SDLC feature is on a single card that can be installed in any I/O card socket in the processor enclosure or in an I/O expansion unit; a single attachment card provides a single-line, half-duplex configuration.

Two of these attachments are required to support duplex point-to-point service, and/or interconnection with an X.25 network. If the line is connected to a duplex modem the attachment still operates in half-duplex mode. The request to send jumper should be installed when the SDLC feature is connected to a duplex modem.

Connections to the modem and the indicator panel are made through top-card connectors.

Note: The SDLC Single-Line Control feature is referred to as the attachment.

Interfaces

An EIA[1]RS232-C and CCITT[2] V.24 interface is provided. The interface drives or ends an external modem or data set.

The communication feature can communicate with remote stations over private lines, leased common-carrier facilities, or switched voice-grade common-carrier lines, or it can be directly connected to a remote station.

Some modems disconnect automatically when the communication feature's DTR signal is deactivated. This signal can be deactivated by issuing a Start command, with a disable operation specified in the device control block, or by using the communications indicator panel.

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[1]   Electronic Industries Association
[2]   The International Telegraph and Telephone Consultative Committee.

Data Links

The communication line can operate with one of the following types of data links:

- Point-to-point nonswitched
- Point-to-point switched
- Multipoint nonswitched
- Direct connect

Point-to-Point Nonswitched

A point-to-point nonswitched data link consists of a local station connected to a single remote station. Such a line is nonswitched because there is a permanent connection between the local station and the remote station through their respective modems.

```
┌─────────┐        ┌─────────┐        ┌─────────┐        ┌─────────┐
│ Local   │        │         │        │         │        │ Remote  │
│ station │────────│ Modem   │────────│ Modem   │────────│ station │
│         │        │         │        │         │        │         │
└─────────┘        └─────────┘        └─────────┘        └─────────┘
```

Point-to-Point Switched

A point-to-point switched data link consists of a local station connected to one of several remote stations after a link has been established between the local station and the remote station. The connection is maintained only for the duration of the communication.

```
                                    ┌─────────┐        ┌─────────┐
                                    │         │        │ Remote  │
                                    │ Modem   │────────│ station │
                                    │         │        │         │
                                    └─────────┘        └─────────┘

┌─────────┐        ┌─────────┐      ┌─────────┐        ┌─────────┐
│ Local   │        │         │      │         │        │ Remote  │
│ station │────────│ Modem   │╴╴╴╴╴╴│ Modem   │────────│ station │
│         │        │         │      │         │        │         │
└─────────┘        └─────────┘      └─────────┘        └─────────┘

                                    ┌─────────┐        ┌─────────┐
                                    │         │        │ Remote  │
                                    │ Modem   │────────│ station │
                                    │         │        │         │
                                    └─────────┘        └─────────┘
```
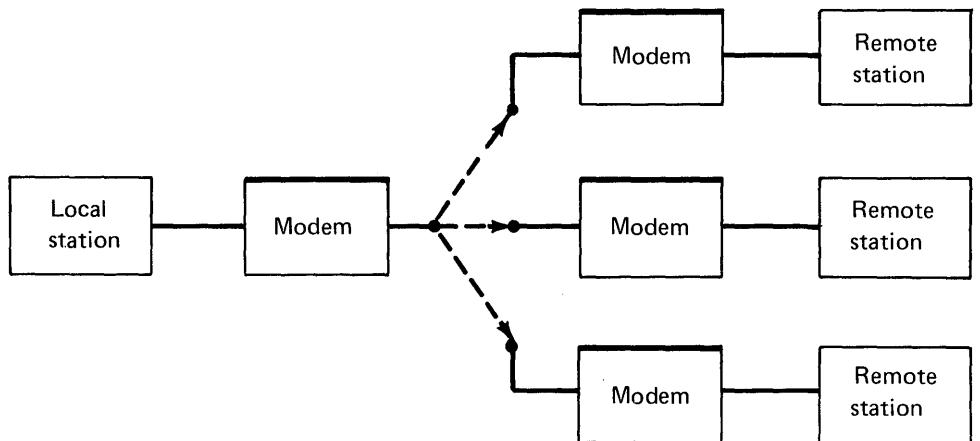
Multipoint Nonswitched

A multipoint nonswitched data link consists of a primary station connected to several secondary stations through their respective modems. The primary station polls the secondary stations, using unique station addresses. Only the addressed station can respond to the poll.

```
                                              ┌─────────┐       ┌───────────┐
                                              │  Modem  │───────│ Tributary │
                                              │         │       │ station   │
                                              └─────────┘       └───────────┘
┌─────────┐     ┌─────────┐                   ┌─────────┐       ┌───────────┐
│ Control │─────│  Modem  │─────●─────────────│  Modem  │───────│ Tributary │
│ station │     │         │                   │         │       │ station   │
└─────────┘     └─────────┘                   └─────────┘       └───────────┘
                                              ┌─────────┐       ┌───────────┐
                                              │  Modem  │───────│ Tributary │
                                              │         │       │ station   │
                                              └─────────┘       └───────────┘
```
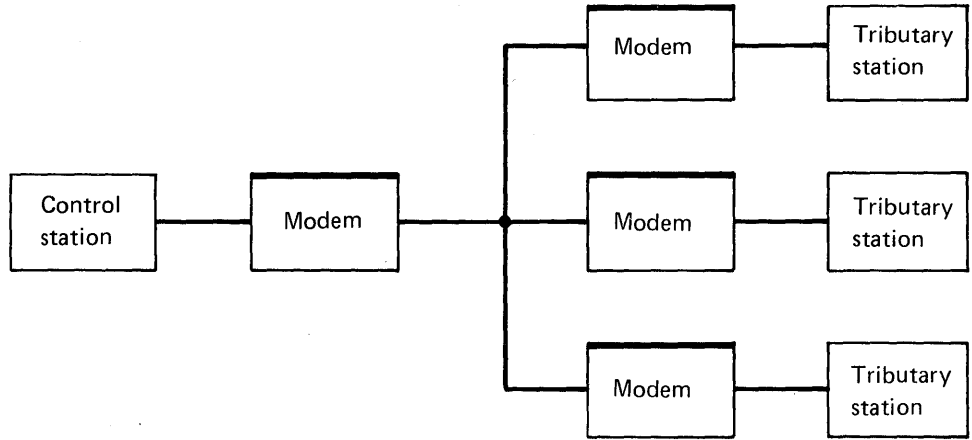
Direct Connect

A direct-connect data link consists of two stations connected using an EIA RS232-C, CCITT V.24 connection.

```
┌─────────┐     ┌─────────┐
│ Local   │─────│ Remote  │
│ station │     │ station │
└─────────┘     └─────────┘
```
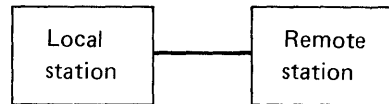
Station Options

Primary and Secondary Stations

Using SDLC, the primary station transmits commands and receives responses while the secondary station receives the commands and transmits responses. The secondary station does not transmit until polled by the primary station.

Combined Stations

Two stations can be connected by a duplex point-to-point line. A combined station transmits both commands and responses and receives both commands and responses from its counterpart combined station.

Establishing a Switched-Line Data Link

Initiating a Call

1. Load the program and make sure that the DTR signal is active.

2. Place the modem in talk mode.

3. Dial the remote station. The operator of the remote station will answer your call, or you will hear a high-pitched tone indicating that the remote modem is in auto-answer mode. If you talk to the operator, request that the remote modem be placed in data mode (or equivalent).

4. Place your modem in data mode (or equivalent) and hang up the receiver.

Answering a Call

1. When you are called, lift the receiver and talk to the operator of the other system.

2. Make sure that the program is loaded and the DTR signal is active.

3. Put your modem in data mode (or equivalent) before the caller puts the calling modem in data mode, and hang up the receiver.

Chapter 2. Operations

Operating Modes

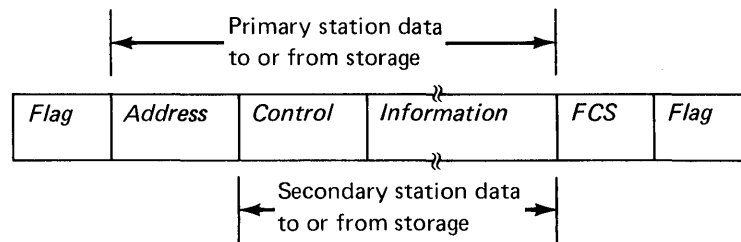The attachment can operate in any of the following modes:

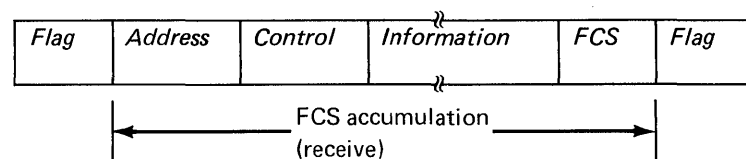- Monitor mode
- Receive mode
- Transmit mode

Monitor Mode

The attachment is placed in monitor mode by a receive operation. While in this mode, the attachment constantly monitors the line for a flag character. If the attachment operates as a primary station, it immediately goes into receive mode upon recognizing a flag character. If the attachment operates as a secondary station, it checks the address following the flag. If the address is its own (or the broadcast address), the attachment goes into receive mode. If the address is not the address of the attachment, the attachment remains in monitor mode.

Receive Mode

If the attachment is operating as a primary station, data transfers to main storage, beginning with the A-field. When the attachment is operating as a secondary station in receive mode, data transfers to main storage beginning with the C-field. If the attachment is operating as a secondary station, the attachment automatically checks the received address to determine if the frame is intended for this station. If the frame is intended for this station, the attachment transfers the data to storage (beginning with the C-field).

```
        |<------- Primary station data ------->|
        |        to or from storage            |
 _____
|      |         |         |  ~          |       |      |
| Flag | Address | Control | Information  |  FCS  | Flag |
|_____|_____|_____|_____~_____|_____|_____|
                      |<---- Secondary station data --->|
                      |   to or from storage            |
```

The accumulation of frame-check sequences starts with the address and includes the frame-check sequence received.

```
 _____
|      |         |         |  ~          |       |      |
| Flag | Address | Control | Information  |  FCS  | Flag |
|_____|_____|_____|_____~_____|_____|_____|
            |<--------- FCS accumulation --------->|
            |            (receive)                 |
```

Transmit Mode

This mode is established when a Transmit command has been issued by the program. The frame-check sequence begins with the first character to be transmitted after the beginning flag character and continues until the byte count, device control block (DCB) word 6, is 0.

Flag	Address	Control	Information	FCS	Flag

FCS accumulation (transmit)
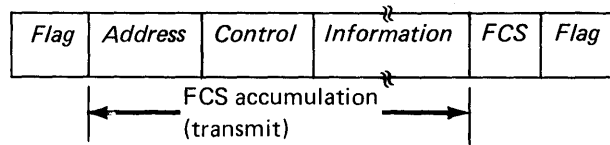
The frame-check sequence is then automatically transmitted, followed by a flag character. If the attachment is operating as a primary station, the address of the receiver comes from storage. If the attachment is operating as a secondary station, the hardware provides the A-field of the frame.

Transmission Codes

The SDLC attachment allows data communication using any 8-bit data code including EBCDIC or ASCII.

Control Characters

Two levels of information grouping are included in SDLC procedures. The basic level, called a frame, is checked for transmission errors by the attachment. The frame is the vehicle for every command, every response, and all information transmitted using SDLC procedures.

Frame starts;
transmission
checking begins

Frame ends;
transmission check
is complete

All control and information
data is sent in one or more
frames
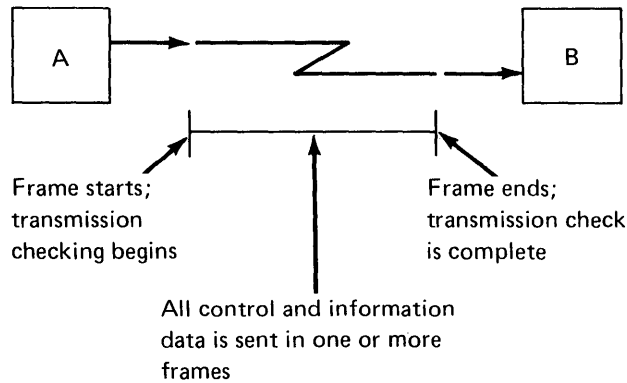
The higher level of grouping, a frame sequence, is checked by the program for missing or duplicated frames. At a station that transmits sequenced frames, the program counts and numbers each sequenced frame; this count is called Ns. At a station receiving sequenced frames, the program counts each error-free sequenced frame that it receives; this count is called Nr.

Primary   Secondary

Nr count   Ns count   ┌─────┐   ┌─────┐   Nr count   Ns count
   0   0   │ A │ ────────────▶ ───〜─── ──▶ │ B │   0   0
   0   1   └─────┘   └─────┘   1   0
   0   2   Ns   Ns   2   0
   0   3   Frames ┌─0─┬─1─┬─2─┬─3─┬─4─┬─5─┬─6─┐   3   0
   0   4   └───┴───┴───┴───┴───┴───┴─▲─┘   4   0
   0   5   │   5   0
   0   6   Poll (command   6   0
  [1] next [7]   ┌─────┐   to respond) ┌─────┐   [7] next [1]
                        │ A │ ◀────── ───〜─── ◀────── │ B │
                        └─────┘   └─────┘

                                           Ns 0
                                          ┌┤ ├ ◀──── Nr=7
                                          └─┘   Final (response)

If B responds with Nr =:   Then A may send, on request, Ns frames:
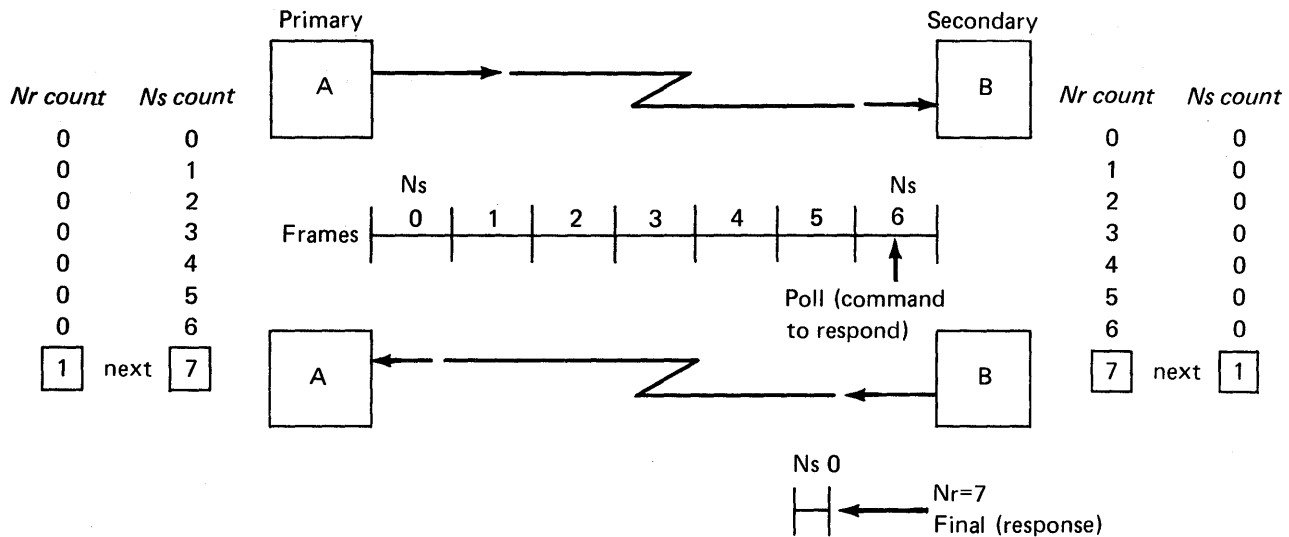
7 (as above, all frames check OK)   7, 0, 1, 2, 3, 4, 5 (continue)
6 (frame 6 discarded because of error)   6, 7, 0, 1, 2, 3, 4 (retransmit and continue)
5 (error on frame 5; 5 and 6 discarded)   5, 6, 7, 0, 1, 2, 3 (retransmit and continue)
4 (error on frame 4; 4–6 discarded)   4, 5, 6, 7, 0, 1, 2 (retransmit and continue)
3 (error on frame 3; 3–6 discarded)   3, 4, 5, 6, 7, 0, 1 (retransmit and continue)
2 (error on frame 2; 2–6 discarded)   2, 3, 4, 5, 6, 7, 0 (retransmit and continue)
1 (error on frame 1; 1–6 discarded)   1, 2, 3, 4, 5, 6, 7 (retransmit and continue)
0 (error on frame 0; no frames accepted)   0, 1, 2, 3, 4, 5, 6 (retransmit)

Note: Shaded frames are retransmitted.

The program advances the Nr count when a frame is checked and found to be error
free. Nr then becomes the count of the next expected frame and should agree with
the next incoming Ns count. If the incoming Ns does not agree with Nr, the frame
is out of sequence and the count Nr does not advance. Out-of-sequence frames
may be rejected or saved at the option of the program. The receiving station does
accept the incoming Nr count (confirmation) if the out-of-sequence frame is
otherwise error free.

The counting capacity for Nr or Ns is 8, using the digits 0 through 7. These counts
can wrap around. For example, 7 is followed by 0. Up to seven frames can be sent
before the receiver reports its Nr count to the transmitter, some or all of the frames
may need repeating. The reported Nr count is the sequence number of the next
frame that the receiving station expects to receive; therefore, if the count is not the
same at a checkpoint as the transmitter's next sequence number, some of the
frames sent must be repeated.

The Nr and Ns counts of both stations are initialized to 0 at the discretion of the
primary station. At other times, the counts advance as sequenced frames are sent
and received.

Data Flow

Each character occupies a byte position in storage. Transfers to and from storage are two bytes at a time, except that the first and last transfers may move only one byte if specified by the data address or byte count.

Transmit

Transmission data is fetched from storage two characters at a time. The high-order byte holds the first character to be sent and the low-order byte holds the next character. After a character has been transferred into the serializer/deserializer; it is transmitted over the line serially, low-order bit first. The following figure illustrates the data flow.
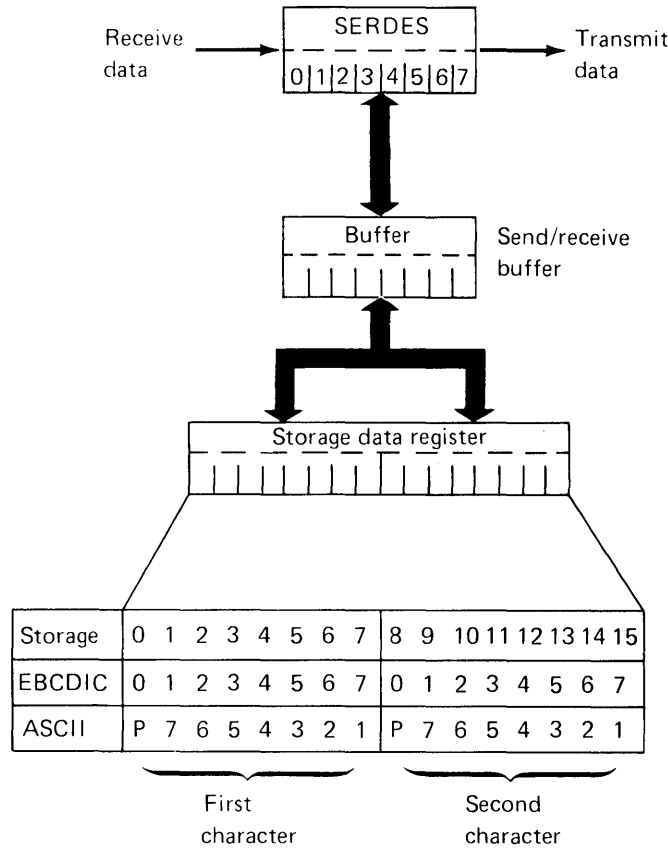
```
                    ┌──────────────────┐
  Receive  ──────▶  │     SERDES       │  ──────▶  Transmit
  data               ├──────────────────┤            data
                     │0│1│2│3│4│5│6│7│
                     └────────▲─────────┘
                              │
                     ┌────────▼─────────┐
                     │     Buffer       │   Send/receive
                     ├──────────────────┤   buffer
                     │ │ │ │ │ │ │ │ │
                     └────────▲─────────┘
                              │
              ┌───────────────┴───────────────┐
              ▼                                ▼
        ┌───────────────────────────────────────┐
        │         Storage data register         │
        ├───────────────────────────────────────┤
        │ │ │ │ │ │ │ │ │ │ │ │ │ │ │ │ │ │
        └───────────────────────────────────────┘
```

Storage	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
EBCDIC	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
ASCII	P	7	6	5	4	3	2	1	P	7	6	5	4	3	2	1

First character   Second character

Figure 1.   SDLC attachment data flow

Note: If the data address (DCB word 7) is odd, only one character is fetched from storage on the first data transfer.

Receive

The first bit received is transferred into the low-order bit position of a byte, the second bit received is transferred into the next higher bit position, and so on, until a character is assembled. The first character received is loaded into the high-order byte of the storage data register, and the next character is loaded in the low-order byte. The attachment provides buffering for four bytes of data. This allows the attachment to recognize an ending flag without putting the frame-check sequence into storage. Data is written into main storage without any code translation.

Note: If the data address (DCB word 7) is odd, only one character is sent to storage on the first data transfer.

Frame Format

All active communication regulated by SDLC procedures has a format called a frame. Each frame is enclosed in flags.

Starting from the beginning flag as a reference point, eight consecutive binary bits are dedicated to the address (A) of the secondary station. The next eight consecutive bits contain the control (C) information, which can be a command or response. At least 16 more bits are transmitted after the C-field before the ending flag is sent. These 16 bits [the frame-check sequence (FCS)] contain the transmission checking information; therefore, the internal structure of any valid frame must consist of at least 32 consecutive binary bits.

Any information (I) field is sent following the C-field and preceding the frame-check sequence field. The I-field is not restricted in format or content. In a frame with an I-field, the maximum length is not restricted by procedures.

The transmission check at the receiver is complete when the ending flag is recognized. The receiving attachment separates the I-field from frame-check sequence information when the ending flag is received, and does not put the frame-check sequence into storage.

Flag

Two flags, the beginning flag and the ending flag, enclose the SDLC frame. The beginning flag serves as a reference for the position of the A- and C-fields and begins transmission error checking; the ending flag completes the check for transmission errors. Both beginning and ending flags have the binary configuration 01111110. The bit orientation of SDLC allows the flag to be recognized at any time. A flag can be followed by a frame or by another flag.
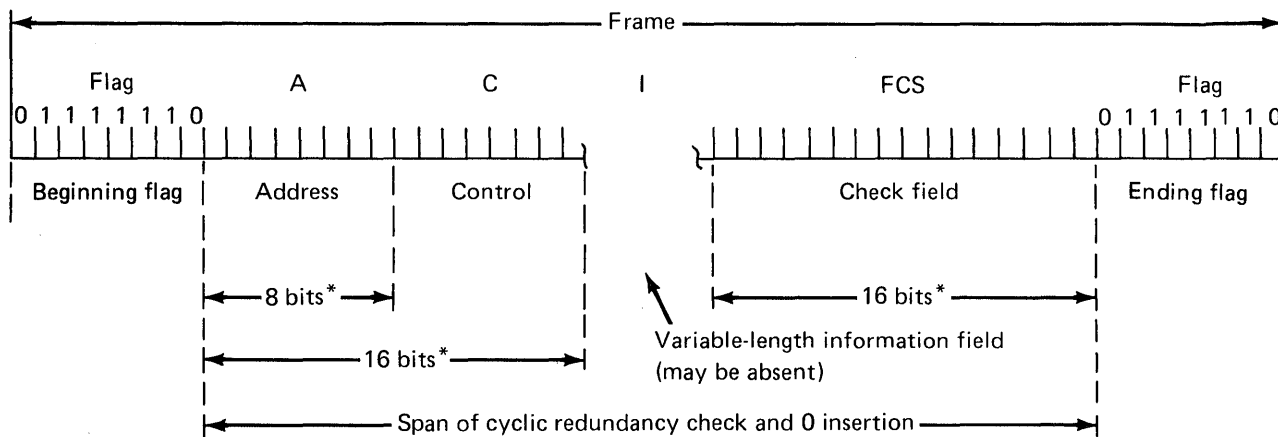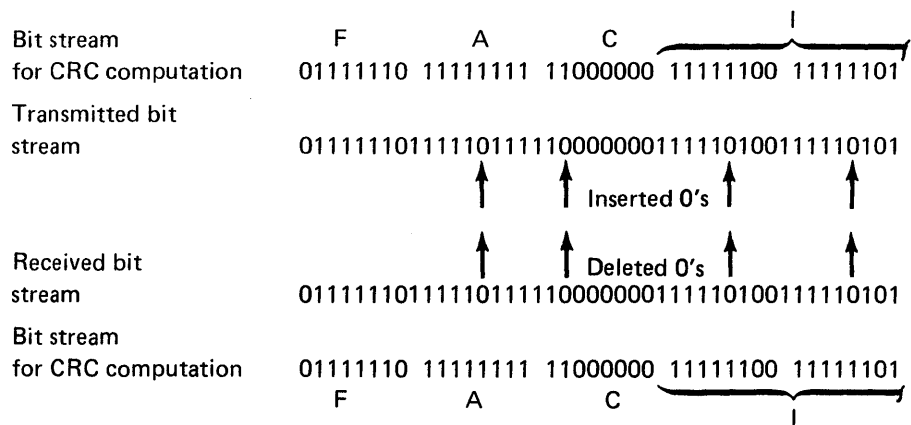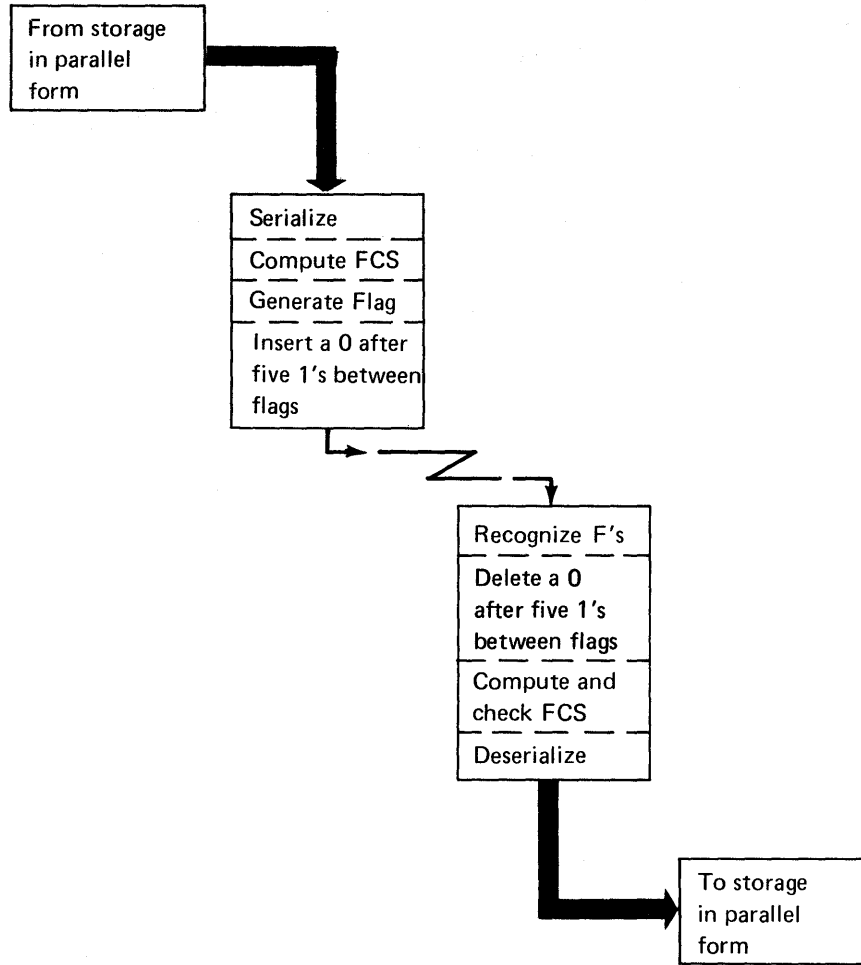

*Excluding inserted 0's.

Frame Format

Zero Insertion

A frame begins with a flag and contains only non-flag bit patterns. (The frame ends at the next flag.) This characteristic does not restrict the contents of a frame, because SDLC procedures require that a binary 0 be inserted by the transmitted station after any succession of five contiguous 1s within the frame. No pattern of 01111110 (flag) is transmitted by chance. After testing for flag recognition, the receiver removes any 0s that follows a received succession of five contiguous 1s. The attachment automatically provides 0 insertion and deletion. Inserted and removed 0s are not included in the transmission error check. (A one that follows five 1s is not removed.)

Note: When NRZI transmission coding is used, 0 insertion eliminates the possibility of prolonged, transitionless periods in the active state. NRZI transmission allows the transmit data line to change states when a logical zero is transmitted.

From storage in parallel form

Serialize

Compute FCS

Generate Flag

Insert a 0 after five 1's between flags

Recognize F's

Delete a 0 after five 1's between flags

Compute and check FCS

Deserialize

To storage in parallel form

Bit stream for CRC computation

F	A	C	I
01111110	11111111	11000000	11111100 11111101

Transmitted bit stream

011111101111101111100000000111101001111110101

Inserted 0's

Received bit stream

011111101111101111100000000111101001111110101

Deleted 0's

Bit stream for CRC computation

01111110	11111111	11000000	11111100	11111101
F	A	C	I	

Data Link Control Functions and 0 Insertion/Deletion

Active State

A series of contiguous flags is transmitted by a station to maintain bit synchronization and to maintain the data link in an active state. A series of flags can also be used to hold the authority to transmit, on half-duplex links, provided that the P/F bit is not sent and to avoid time-outs at the linked stations.

Note: NRZI transmission recording and zero insertion is used only in the active state of the data link.

Address Field

The primary station manages a data link by issuing commands to the secondary stations that recognize their address in the A-field of a received frame.

A primary station can address all secondaries by sending an *all 1's* address (hex FF). A secondary station may receive a common address or its individual address. However, when a secondary station sends any response, its individual address is used.
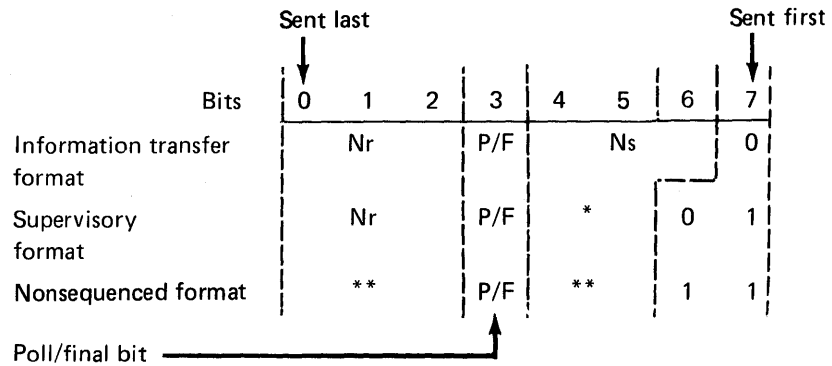
Balanced Operation

When the two-attachment duplex mode is used to support CCITT RECOMMEN-DATION X.25 for LAP (Link Access Procedure) and LAPB (Link Access Procedure, Balanced Mode), the address field is used as follows:

	Frame address (hexadecimal)	
	DTE to DCE*	DCE* to DTE
Command frame	01	03
Response frame	03	01

*Data Circuit Terminating Equipment

Control Field and the Poll/Final (P/F) Bit

The C-field contains, within its eight binary digits, the capability to encode the commands and responses required to control a data link. The C-field has three formats, as shown here:

	Sent last							Sent first
Bits	0	1	2	3	4	5	6	7
Information transfer format		Nr		P/F		Ns		0
Supervisory format		Nr		P/F		*	0	1
Nonsequenced format		**		P/F		**	1	1

Poll/final bit → (bit 3)

*Codes for supervisory commands/responses
**Codes for nonsequenced commands/responses

(Software controls the commands and responses to correspond to the link-level protocol used.)

Each C-field contains the format identifier and poll/final bits. The codes for the C-field commands and responses are shown here:

| Format (see note)	Sent last ↓	Binary configuration	Sent first ↓	Acronym	Command	Response	I-field prohibited	Resets Nr and Ns	Confirms frames through Nr-1	Defining characteristics
NS	000	P/F	0011	U1	X	X				Command or response that requires unnumbered information
	000	F	0111	RIM		X	X			Initialization needed; expect SIM
	000	P	0111	SIM	X		X	X		Set initialization mode; the using system prescribes the procedures
	100	P	0011	SNRM	X		X	X		Set normal response mode; transmit on command
	000	F	1111	DM		X	X			This station is offline
	010	P	0011	DISC	X		X			Do not transmit or receive information
	011	F	0011	NSA		X	X			Acknowledge NS commands
	100	F	0111	FRMR		X				Invalid frame received; must receive SNRM, DISC, or SIM
	101	P/F	1111	XID	X	X				System identification in I-field
	001	P/F	0011	NSP	X		X			Response optional if no P-bit
	111	P/F	0011	TEST	X	X				Check pattern in I-field
S	Nr	P/F	0001	RR	X	X	X		X	Ready to receive
	Nr	P/F	0101	RNR	X	X	X		X	Not ready to receive
	Nr	P/F	1001	REJ	X	X	X		X	Transmit or retransmit, starting with frame Nr
I	Nr	P/F	Ns 0	I	X	X			X	Sequenced I-frame

Note: NS = nonsequenced, S = supervisory, I - information.

During half-duplex operation the poll/final (P/F) bit is the send-receive control. A poll bit is sent to a secondary station to authorize transmission; a final bit is returned by the secondary station in response to the poll bit. (Do not confuse the final bit with the F (flag) frame delimiter pattern.) Normally, only one poll bit is outstanding (unanswered by a final bit) on a data link. For half-duplex operation, a poll/final bit detected ON ends the receive operation at the conclusion of the frame in progress. During duplex operation, the attachment can ignore the P/F bit and continue to receive.

Information Transfer Format

A C-field in the information transfer format is a part of each sequenced frame transmitted over a data link. It contains the poll-final bit and the Nr and Ns counts.

Stations transmitting information-transfer frames request configuration by sending the Ns count; they confirm by sending the Nr count.
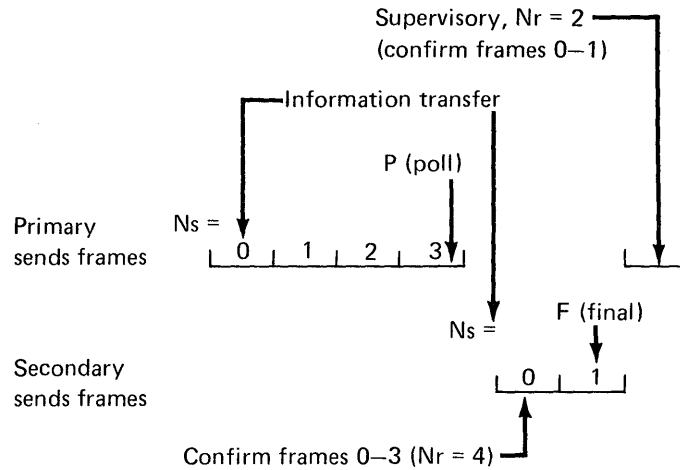
Supervisory Format

The supervisory format is an adjunct to the information transfer format. Frames containing a C-field of the supervisory format convey ready or busy conditions and can be used to report sequence errors (thus requesting retransmission). Such frames may be interspersed with frames having a C-field of the information transfer format. Whether or not a primary station has information data to transmit, it may use a frame having a C-field of the supervisory format to poll a secondary station. A secondary station can use the supervisory format to respond to a request for confirmation. Frames with a supervisory format C-field are not counted in the Nr or Ns counts.

Nonsequenced Format

Command and response frames having a C-field of this format are used for data link management. Data link management includes activating and initializing secondary stations, controlling the response mode of secondary station, and reporting of procedural errors (not recoverable by retransmission). Information data may also be transmitted, using a frame with a C-field of the nonsequenced format. Frames with a nonsequenced format C-field are not counted in the Nr or Ns counts.

Information Field

The information field (I-field) contains data that is moved, by using the data link, from place to place. The I-field is unrestricted in format and content; its contents are not apparent to the components of data link control.

An I-field is normally included with every frame having a C-field of the information-transfer format. These information-transfer frames are the only ones that are sequenced.

Provisions for an I-field in frames with a non-sequenced format C-field exists but are unprotected by sequence checking.

Frame Check Sequence Field

The frame-check sequence field, also called block check characters (BCC), contains 16 binary digits. It follows the I-field if there is one, the C-field if not, and immediately precedes the ending flag.

The transmitting SDLC attachment performs the computation and sends the resulting frame-check sequence value. The receiving SDLC attachment performs a similar computation and checks its results; it discards an incorrect frame and does not advance the Nr count.

Synchronization

The SDLC attachment receives timing signals from the modem, which establishes and maintains bit synchronization. When the attachment starts to transmit, it automatically transmits a flag character that establishes frame and byte synchronization.

Some modems, to operate properly, may require NRZI-coded data and/or pad characters. Bits 9 and 12 of the DCB control word can be used to satisfy particular modem requirements.

If internal clocking is used, the attachment operates in NRZI mode and automatically sends two pad characters (hex 00) prior to sending the beginning flag. This causes 16 bit transitions to take place before the flag character is sent.

Timers

The attachment has two programmable timers. Each timer can count up to 27 seconds, in 106 millisecond increments. Bits 0 through 7 of DCB word 1 control the first timer; bits 8 through 15 control the second timer.

Timer 1

Timer 1 can be used in the following ways:

Idle detect timer: If a receive operation is specified, the attachment runs timer 1 for the duration specified by bits 0 through 7 of DCB word 1. When timer 1 times out, the attachment begins checking the line for an idle condition. If it detects an idle condition it presents an exception-interrupt request.

If it detects a flag character while timer 1 is running, it immediately begins checking for an idle condition and stops timer 1. If the attachment detects an idle condition from the time timer 1 stops until the receive operation ends, it presents an exception-interrupt request.

If the program assigns a value of 0 to timer 1, the attachment does not check for an idle condition.

Note: An idle condition is 15 contiguous 1s on the line.

Data set ready time-out: During an enable terminal operation, a time-out occurs if data set ready (DSR) is not returned by the modem within the specified time. If the condition of the rate select line is changed during the enable terminal operation, set the timer value that allows the modem enough time to equalize. Consult the manual for the modem being used to determine equalization time. A timer value of zero indicates that no time-out will be reported.

Disable data terminal ready time-out: During a disable terminal operation, a time-out occurs if DSR is not deactivated within the specified time. A timer value of zero indicates that no time-out will be reported.

Clear to send time-out: During a transmit operation, a modem interface error occurs if clear to send (CTS) is not returned by the modem within the specified time. A timer value of zero indicates that no time-out will be reported.

Program delay: When the operation is not an enable terminal, disable terminal, receive, or transmit operation, timer 1 can be used by the program for timing purposes.

Note: When using a program delay, timer 2 must not be in use when performing a hold-line-active function after a transmit operation.

Timer 2

Timer 2 is used in two ways:

Nonproductive receive time-out: This time-out is used only during receive operations. Its purpose is to limit the total nonproductive receiving time for a total receive operation. A total receive operation can be a single receive operation or a chain of receive operations started by a single Operate I/O instruction. When chaining receive operations, the value for timer 2 is taken from each DCB in the chain. The timer runs anytime that the attachment is not receiving flags or frames. When timer 2 times out, the attachment presents an exception interrupt request. When the timer is set to 0, no time-out occurs.

Hold-line-active timer: When timer 2 is used in conjunction with a transmit operation with bit 15 on in the DCB control word, the attachment transmits flag characters for the duration of the time specified by bits 8 through 15 of DCB word 1, or until another transmit operation begins. When the timer is set to 0, no time-out occurs, and the attachment transmits continuous flags until another transmit operation begins.

Commands

The Operate I/O instruction points to the immediate device control block (IDCB) that contains one of the following commands:

- Prepare
- Halt I/O
- Device Reset
- Read ID
- Start Diagnostic 1
- Start Diagnostic 2
- Start
- Start Cycle-Steal Status

The programmer must ensure that the program always tests the operate I/O condition codes following an Operate I/O instruction.

Programming note: Since two attachments are required to support duplex operation, commands must be issued to both cards as required.

Note: See Appendix C for an example of an adapter initialization.

Prepare

The Prepare command is used to control the interrupt parameters of the addressed device. The data word contains the level and I-bit. The device always accepts and executes a Prepare command, even if it is busy or has an interrupt request pending from a previous command. The IDCB for the Prepare command has the following format:

IDCB (immediate device control block)

Command field	Device address field
0 1 1 0 0 0 0 0	0 X X X X X X X
0 7	8 15
60	00—7F

Immediate data field		
0's	Level	I
16	26 27 30	31

Level: This 4-bit field specifies the priority interrupt level assigned to the device. The binary value of bits 27–30 indicates priority levels of 0–3.

Example

Bits 27–30	Level
0000	0
0001	1
0010	2
0011	3

I-Bit: This bit determines whether the device is allowed to present interrupt requests. An I-bit set to 1 means that the device can request to interrupt; if it is set to 0 it means that the device cannot interrupt.
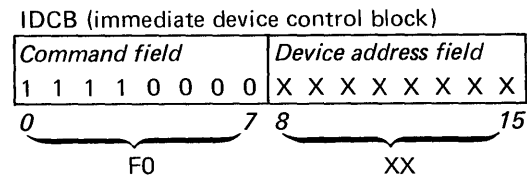
The attachment stores the level data and presents it to the processor each time the attachment presents an interrupt request. The prepare information (level and I-bit) is reset by a system reset or a power-on reset.

The Prepare command causes an interrupt request only when the attachment is not prepared (I-bit set to 0) and has an interrupt request pending upon receipt of a Prepare with the I-bit set to 1.

A successful Prepare command always causes the attachment to respond with satisfactory (CC7).
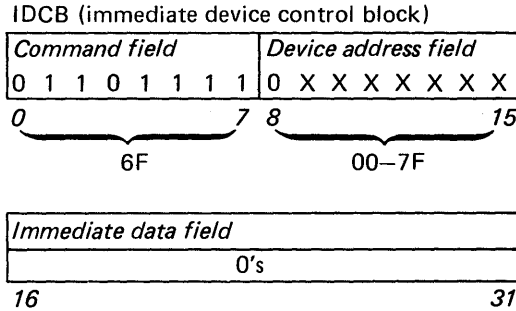
Halt I/O

This command halts all I/O activity on the I/O channel. The reset functions in the attachment are the same as the ones carried out for a Device Reset.

IDCB (immediate device control block)

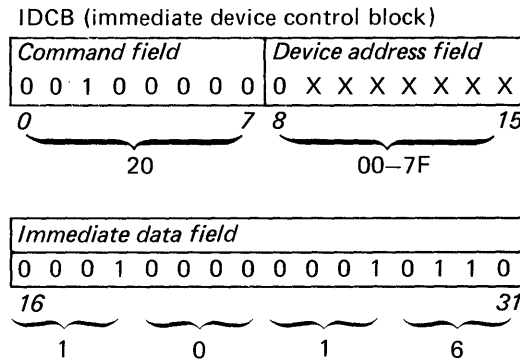| Command field	Device address field
1 1 1 1 0 0 0 0	X X X X X X X X
0 7	8 15
FO	XX

Device Reset

The Device Reset command resets the addressed device. Any pending interrupt requests are cleared. Prepared level, I-bit, residual address, and data terminal ready (DTR) are not reset by this command. The Device Reset command has the following format:

IDCB (immediate device control block)

Command field	Device address field
0 1 1 0 1 1 1 1	0 X X X X X X X
0 7	8 15
6F	00–7F

Immediate data field
0's
16   31

A Device Reset command issued to the attachment causes the attachment to become busy while the reset functions are carried out. The amount of time that the attachment is busy is a function of the microcode program. The attachment presents a busy after reset (CC2) if an Operate I/O follows a Device Reset too closely.
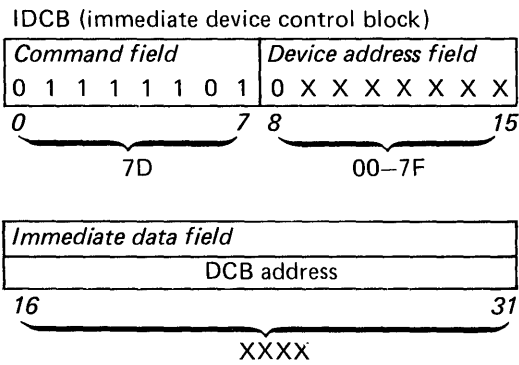
Read ID

The Read ID command transfers the attachment's identification (ID) word from the attachment to the immediate data field of the IDCB. The ID word of the SDLC attachment is shown below as it appears in the immediate data field of the IDCB:
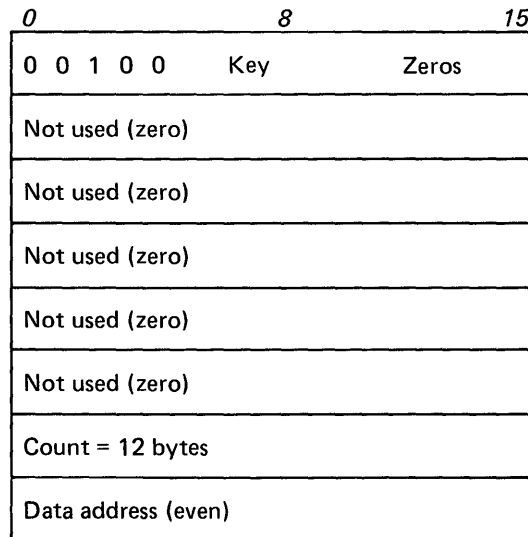
IDCB (immediate device control block)

Command field	Device address field
0 0 1 0 0 0 0 0	0 X X X X X X X
0 7	8 15
20	00–7F

Immediate data field
0 0 0 1 0 0 0 0 0 0 0 1 0 1 1 0
16   31
1   0   1   6

Start Diagnostic 1

The format of the IDCB for this command is:

IDCB (immediate device control block)

Command field	Device address field
0 1 1 1 1 1 0 1	0 X X X X X X X

0   7 8   15

7D   00–7F

Immediate data field
DCB address

16   31

XXXX

The format of the DCB for the Start Diagnostic 1 command follows:

0   8   15

0 0 1 0 0   Key   Zeros
Not used (zero)
Not used (zero)
Not used (zero)
Not used (zero)
Not used (zero)
Count = 12 bytes
Data address (even)

The byte count for this operation must be 12 (hex 000C) and the data address must be even; otherwise, a DCB specification check occurs. The DCB control word should be hex 2000.

The Start Diagnostic 1 command causes the following four tests to be performed in the attachment:

Register test: Upon recognition of the Start Diagnostic 1 command, and before fetching the DCB, all registers accessible to the microcontroller are tested. If the test finds an error, the attachment halts and proceeds no further. If the test does not find an error, the attachment fetches the DCB and proceeds with test 2.

Checksum test: The read-only storage modules in the attachment have a checksum built into them when they are made. This test reads each location in read only storage and calculates a check sum for each module.

It then transfers the built-in and calculated checksums to storage as follows:

Data word 0 = Built-in check sum read only storage module 1
Data word 1 = Calculated check sum read only storage module 1
       (inverted)
Data word 2 = Built-in check sum read only storage module 2
Data word 3 = Calculated check sum read only storage module 2
       (inverted)

Function test: This test checks various circuits and latches in the attachment. The results are then placed in data word 4 in storage. The bits in data word 4 have the following significance:

Bit	Meaning
0	DTR active
1	DSR active
2	Not used
3	Not used
4	NRZ transmit tested successfully*
5	Not used
6	NRZI transmit tested successfully
7	Not used
8	Flag latch tested successfully
9	Abort latch tested successfully
10	Idle latch tested successfully
11	Buffer service latch tested successfully
12	Overrun latch tested successfully
13	Zero bit insert tested successfully
14	Transmit clock active
15	Receive clock active

*NRZ is not tested if the internal clock jumper is installed.

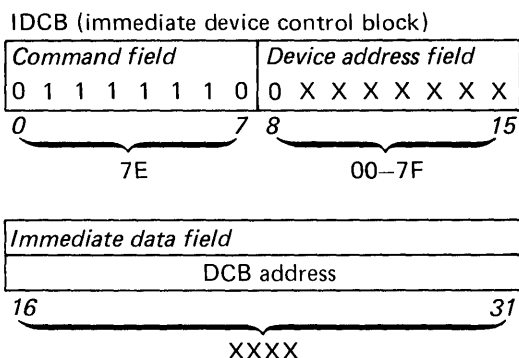The following table shows the correct contents of data word 4 for various configurations:

	With internal clocking	Without internal clocking*
Leased-line or switched-line with modem enable	C2FF	CAFC CAFD CAFE CAFF
Switched-line with modem disabled	82FF	8AFC 8AFD 8AFE 8AFF

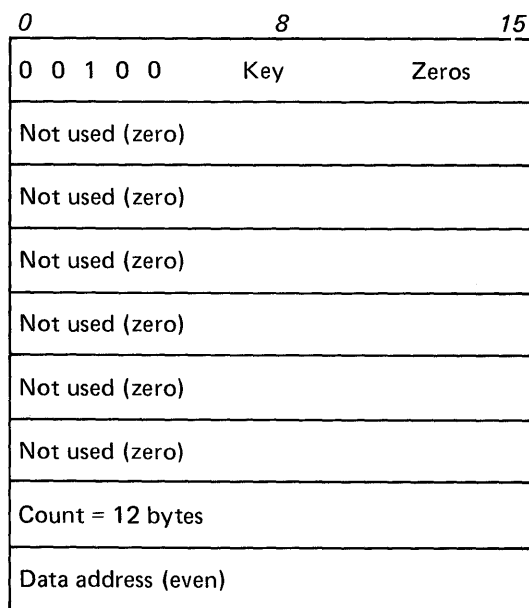*State of bits 14 and 15 depends on state of modem clocks.

Byte transfer test: The attachment loads the value in the DISPLAY/FUNCTION SELECT switches of the communication indicator panel into both bytes of the attachment's storage data register. If an indicator panel is not connected to the attachment, the value is 0. The attachment then attempts to transer only the high-order byte of The storage data register to data word 5 in storage. The low-order bytes of data word 5 in storage remain unchanged. The program makes data word 5 equal to FFFF before issuing the Start Diagnostic 1 command to verify the correct byte transfer.

Start Diagnostic 2

The Start Diagnostic 2 command is used by diagnostic programs to perform the same tests as the Start Diagnostic 1 command, with the addition of a data wrap test during test 3 (see "Start Diagnostic 1"). The format of the IDCB for this command is:

IDCB (immediate device control block)

Command field	Device address field
0 1 1 1 1 1 1 0	0 X X X X X X X

0 _____ 7 8 _____ 15

7E   00–7F

Immediate data field
DCB address

16 _____ 31

XXXX

The format of the DCB for the Start Diagnostic 2 command follows:

0   8   15

0 0 1 0 0	Key	Zeros
Not used (zero)		
Not used (zero)		
Not used (zero)		
Not used (zero)		
Not used (zero)		
Not used (zero)		
Count = 12 bytes		
Data address (even)		

The byte count for this operation must be 12 (hex 000C) and the data address must be even; otherwise, a DCB specification check is presented. The DCB control word should be hex 2000. For this command to operate properly, the attachment must be disconnected from the modem, and a wrap connector must be plugged into the modem end of the cable that goes from the attachment to the modem.

The bits in data word 4 have the following meanings for the Start Diagnostic 2 command:

Bit	Meaning
0	DTR active
1	DSR active
2	RTS active
3	CTS active
4	NRZ transmit tested successfully (see Note)
5	NRZ receive tested successfully (see Note)
6	NRZI transmit tested successfully
7	NRZI receive tested successfully
8	Flag latch tested successfully
9	Abort latch tested successfully
10	Idle latch tested successfully
11	Buffer service latch tested successfully
12	Overrun latch tested successfully
13	Zero bit insert tested successfully
14	Transmit clock active
15	Receive clock active

Note: NRZ is not tested if the internal clock jumper is installed.

If the attachment supplies internal clocking, data word 4 should equal F3FF. If the modem supplies clocking, data word 4 should equal FFFC.
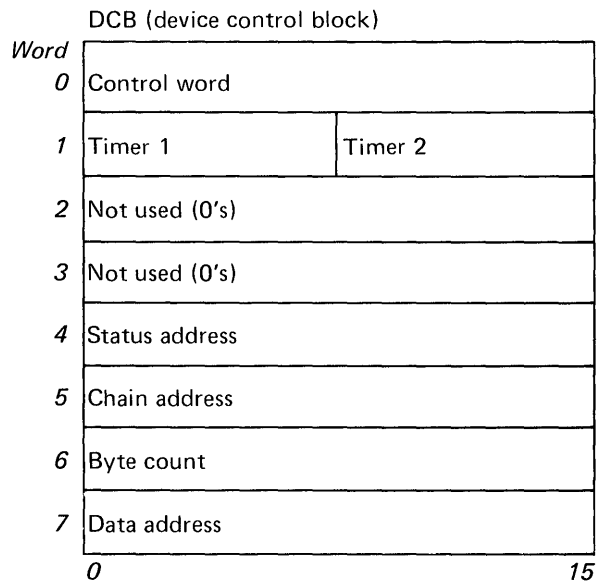
Start

The Start command transfers the address of a DCB to the attachment. When the Start command is accepted, the attachment fetches the DCB from the main storage address specified in the immediate data field of the IDCB and begins carrying out the operation.

IDCB (immediate device control block)

Command field	Device address field
0 1 1 1 0 0 0 0	0 X X X X X X X

0   7   8   15

      70   00—FF

Immediate data field
DCB address

16   31
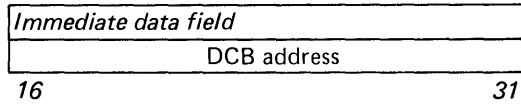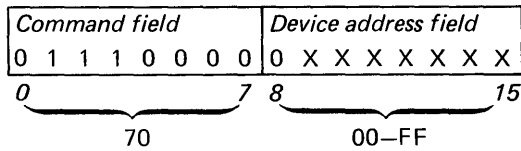
The format of the DCB for a Start command follows:

DCB (device control block)

Word		
0	Control word	
1	Timer 1	Timer 2
2	Not used (0's)	
3	Not used (0's)	
4	Status address	
5	Chain address	
6	Byte count	
7	Data address	

0   15

The DCB address transferred to the attachment through the IDCB points to word 0 of the DCB and must be even. If the DCB address is odd, the attachment sets interrupt status byte bit 1 (delayed command reject) to 1 and ends the operation with an exception interrupt request (CC2).

DCB Word 0 – Control

Bit 0 – Chaining Flag: If this bit is set to 1, the next DCB in the chain is fetched after the successful completion of the current DCB operation. If this bit is set to 0 and the operation is successfully completed, the attachment presents a device-end interrupt request.

Bit 1: Not used and must be set to 0.

Bit 2 – Input Flag: Indicates the direction of data transfer relative to processor storage. If bit 2 is set to 1, data is transferred from the attachment to the processor. If bit 2 is set to 0, data is transferred from the processor to the attachment. For a Start command, a receive operation is specified by bit 2 being set to 1.

Receive operation - This operation allows the attachment to begin transferring received data to the processor after synchronization is established.

The ending conditions for a receive operation are dependent on the following factors:

- The setting of the chaining flag (bit 0)
- The setting of the SE bit (bit 4)
- The condition of the poll-final bit in the current frame
- Whether any errors occurred in the frame
- Half-duplex or duplex operation

The attachment has the ability to interrupt (break receive chain) or continue to receive. The interrupt can be used in half-duplex operation and the continue receive function is available for duplex operation.

There are two general types of errors: suppressible and nonsuppressible. Nonsuppressible errors always cause an exception interrupt request (CC2). All errors except the following four are nonsuppressible.

- Overrun
- Aborted frame
- Incorrect length record
- Block check error

The action taken when a suppressible error occurs depends upon the setting of the SE bit. If the SE bit is set to 0, the attachment presents an exception interrupt (CC2) and posts the cause of the error in the interrupt status byte or cycle-steal status words. If the SE bit is set to 1, the attachment posts the error in the in the residual status block and either presents a device and interrupt request (CC3) with interrupt information byte bit 0 set to 1, or chains to the next DCB.

Bits 0 through 7 of DCB word 1 can be used in conjunction with the receive operation to specify a time after which the attachment begins checking the line for an idle condition. If an idle condition is detected, the attachment sets bit 5 to 1 in cycle-steal status word 2 and bit 0 to 1 in the interrupt status byte, and presents an exception interrupt request.

Bits 8 through 15 of DCB word 1 can be used in together with the receive operation to specify the nonproductive receive time-out period.

Bit 3: Not used and must be set to 0.

Bit 4 - Suppress Exception: This bit is used with receive operations only. When this bit is set to 1, the attachment stores two words of information into the residual status block at the end of the operation, beginning at the address specified in the status address (DCB word 4). The first word contains the residual byte count. The second word contains the residual status flags. See the description of DCB word 4 (status address) for more information about the residual status block.

Bits 5-7 - Cycle-Steal Address Key: A 3-bit key presented to the processor by the attachment during data transfers so that the processor knows if the attachment is authorized to access certain blocks of main storage.

Bit 8 - Half-Rate: The attachment only recognizes this bit during the enable terminal operation—and then only if DSR is set to 1. This bit causes the modem to operate at one-half of its normal bit rate (if the modem is equipped to do so). If internal clocking is being used, this bit selects the 600-bps bit rate. If changing bit rates, timer 1 (bits 0 through 7 of DCB word 1) should be set to allow enough time for the modem to equalize when using modem clocking. Change rates if timer 1 is set to 0, regardless of whether internal clocking or modem clocking is being used.

Bit 9 - NRZI Coding: This bit causes the attachment to use and recognize NRZI coding. When the internal clocking feature is used, NRZI is automatic and this bit is ignored.

Bit 10 - Enable Terminal Operation: This bit causes the attachment to activate the DTR line. A device-end interrupt request occurs or a chaining operation begins 50 milliseconds after the modem activates DSR.

Timer 1 can be used together with this operation to limit the time the attachment waits for DSR to become active. If DSR does not become active within the specified time, the attachment resets DTR and presents an exception interrupt request with bit 0 set to 1 in the interrupt status byte and bit 4 set to 1 in status word 2.

For manual answer or manual call sequences, this bit must be used to switch DTR on before entering data mode. On leased lines, DTR can be set to 1.

Programming Consideration: When the modem presents a ring indication, the attachment presents an attention interrupt request (CC4) and waits 50 milliseconds for the program to perform an enable terminal operation. If after this time the program has not enabled DTR, the attachment presents another attention interrupt request (provided that the ring indication is still active).

Note: If DSR is not returned and a time-out occurs, the attachment resets the DTR line.

Bit 11 - Disable Terminal Operation: This bit causes the attachment to deactivate the DTR line and disconnect from a switched network. Timer 1 can be used together with this operation to limit the time that the attachment allows for DSR to become deactivated. If DSR does not deactivate within the specified time, an exception interrupt request occurs with bit 0 set to 1 in the ISB and bit 4 set to 1 in status word 2. A device-end interrupt request occurs or a chaining operation begins 200 milliseconds after the attachment detects that the DSR line has been deactivated.

Bit 12 - Control/Pad: If set to 1 in transmit mode (bit 2 set to 0, bit 14 set to 1) and bit 12 is set to 1, the attachment automatically transmits two pad characters before transmitting the first flag character of the first frame. For NRZ, the pad character is hex 55; for NRZI, the pad character is hex 00.

If in receive mode (bit 2 set to 1, bit 14 set to 0) bit 12 is used to control the presentation of device end interrupt.

```
bit 12 - 0 — Final bit 0   (In received frame) do not present device end interrupt (unless
        |              |       end of chain reached) and stay in receive mode.
        |              |__1    Present device end interrupt and drop out of receive mode.
        |__1 — Ignore final bit (in received frame) and stay in receive mode (unless end of
              chain).
```

Note: This facilitates duplex operation when using two attachments.

Bit 13 - Secondary or Primary: This bit determines whether the attachment operates as a secondary or a primary station. If bit 13 is set to 1, the station is a primary station; if bit 13 is set to 0, the station is a secondary station. On a receive operation, the attachment examines the address portion of a received frame only if the attachment is being used as a secondary station. On a transmit operation, the attachment begins its own address only when it is operating as a secondary station.

Bit 14 - Transmit Operation: The attachment begins this operation by activating request-to-send (RTS), and then waiting for clear-to-send (CTS) to become active. Upon receiving CTS, the attachment transmits the beginning flag character and starts transmitting the data. When the byte count is reduced to 0, the attachment automatically transmits the frame-check sequence and the ending flag character. One DCB causes one frame to be transmitted.

If bit 0 (the chaining flag) is set to 1, the attachment fetches the next DCB and starts the next frame. If bit 15 (hold line active) is set to 0 and the attachment is unable unable to fetch the chained-to DCB in time to cause the next frame to immediately follow the preceding frame, the attachment deactivates transmit mode and the transmission line goes into an idle condition. The next DCB is then treated as a normal transmit operation. Bit 15 can be used to eliminate the possibility of the line idling between frames.

If bit 0 and bit 15 are set to 0 and the modem delay jumper is installed, the attachment automatically transmits trailing pad characters (hex FF) for 2 milliseconds after the ending flag character. The attachment then exits transmit mode and resets RTS.

Bit 15 - Hold Line Active: Used in conjunction with bit 14 (transmit operation). If bit 15 is set to 1, when the byte count goes to 0, the attachment stays in transmit mode and transmits flag characters until another operation begins or until the time specified in timer 2 passes. If the program sets timer 2 to 0, then the attachment remains in transmit mode and transmits flags until another operation begins.

		Conditions		Results				
	Chn bit	SE bit	P/F bit	Int CC	IIB bit 0	Chain occurs	Post resid- ual status	EOC bit *
No errors	0	0	0	3	0	no	no	n/a
	0	0	1	3	0	no	no	n/a
	0	1	0	3	0	no	yes	1
	0	1	1	3	0	no	yes	1
	1	0	0	n/a	n/a	yes	no	n/a
	1	0	1	2	**	no	no	n/a
	1	1	0	n/a	n/a	yes	yes	0
	1	1	1	3	0	no	yes	1
Suppressible errors	0	0	0	2	**	no	no	n/a
	0	0	1	2	**	no	no	n/1
	0	1	0	3	1	no	yes	1
	0	1	1	3	1	no	yes	1
	1	0	0	2	**	no	no	n/a
	1	0	1	2	**	no	no	n/a
	1	1	0	n/a	n/a	yes	yes	0
	1	1	1	3	1	no	yes	1

*See "Status Address" for a description of this bit.

**When condition code 2 is reported, the IIB is called the ISB and bit 0 has a different meaning. See "Interrupt Status Byte" for a description of ISB bits.

DCB Word 1 - Timer 1/Timer 2

The value specified in bits 0–7 of this word determine the value set in timer 1 of the attachment.

The value specified in bits 8–15 of this word determine the value set in timer 2 of the attachment.

DCB Words 2 - 3

Not used.

DCB Word 4 - Status Address

DCB word 4 contains the processor storage location of the first word of the residual status block. If DCB word 0, bit 4 (suppress exception) is set to 1, a residual status block is stored in processor storage after every DCB fetch, regardless of whether an error occurred. Suppress exception (DCB word 0, bit 4) is used only for receive operations. If bit 4 of the control word is set to 1 and the attachment detects any of the conditions that set residual status flags, an exception-interrupt request does not occur. Instead, the attachment automatically stores two words of information into the residual status block and monitors the line, looking for an ending flag character. When the ending flag is detected, the attachment presents a normal device-end interrupt request or begins a chaining operation. The first word stored in the residual status block is the residual byte count; the second word contains the residual status flags.

Residual Status Flags: The second word of the residual status block contains the residual status flags. The bits have the following meanings:

Bit 0 - End-of-Chain: This bit indicates that no further chaining will take place and is usually a result of the attachment receiving a frame in which the poll-final bit is set to 1. This bit also set to 1 if the SE bit is set to 1 and the chaining flag is set to 0.

Bits 1-7: Not used.

Bit 8 - Overrun: This condition occurs during a receive operation if the attachment is unable to transfer the contents of the storage data register to the processor before it is time to load another word of data into the storage data register.

Bit 9 - Abort: This condition occurs during a receive operation if the attachment detects an abort condition. An abort condition is eight contiguous 1-bits received after the beginning of a frame.

Bit 10 - Long Frame: This bit indicates that the byte count is 0 and the current frame has not ended. The attachment continues to monitor the receive line until the end of the frame; however, any data received after the byte count reaches 0 is lost.

Bit 11 - Block Check Error: The frame check sequence received is incorrect.

Bits 12-14: Not used and must is set to 0.

Bit 15 - No Exception: This bit indicates either of two conditions. The first condition is that the frame is the correct length and error free. The second condition is that the attachment received an error free but short frame. To determine which condition caused this bit to be set, examine the residual byte count. If the residual byte count is not 0, a short frame was received.

DCB Word 5 – Chaining Address

The chaining address contains the processor storage address of the next DCB and is used when chaining is indicated (bit 0 of control word is set to 1). The chaining address must be even. If the address is odd, the attachment sets interrupt status byte bit 3 to 1 and ends the operation.
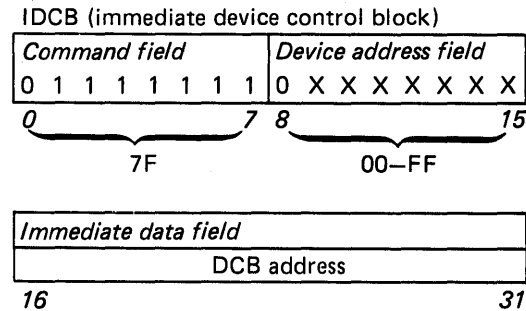
DCB Word 6 – Byte Count

This 16-bit word contains the number of bytes to be transferred during the operation specified in the current DCB control word.
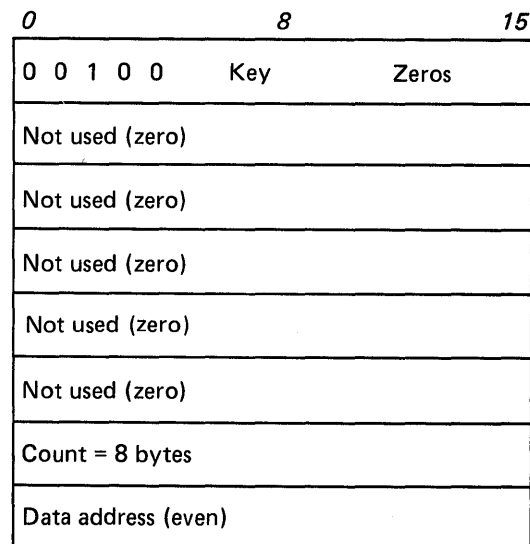
DCB Word 7 – Data Address

This is the address in processor storage where data transfer starts.

Start Cycle-Steal Status

The Start Cycle-Steal Status command causes the attachment to transfer status information (about the previous cycle-steal operation) to the processor. The attachment provides four words of cycle-steal status information. The byte count specified in word 7 of the DCB must be 8.

IDCB (immediate device control block)

Command field	Device address field
0 1 1 1 1 1 1 1	0 X X X X X X X
0 7	8 15
7F	00–FF

Immediate data field
DCB address

16   31

The format of the DCB for a Start Cycle-Steal Status command follows:

0   8   15

0 0 1 0 0   Key   Zeros
Not used (zero)
Not used (zero)
Not used (zero)
Not used (zero)
Not used (zero)
Count = 8 bytes
Data address (even)

The data address (word 7) must be on a word boundary (bit 15 set to 0) or an exception interrupt request (CC2) occurs with a DCB specification check (bit 3) set to 1 in the interrupt status byte. The attachment ignores bits 0, 4, and 8 through 15 of the control word, and DCB words 1 through 5. The byte count must be 8, and the data address must be an even address. Four words are transferred into main storage, starting at the data address contained in DCB word 7.

When a cycle-steal data transfer is ended by an exception condition, bit 0 of the interrupt status byte may be set to 1. If interrupt status byte, bit 0 is set to 1, further information regarding the cause of the exception condition can be obtained by executing a Start Cycle-Steal Status command.

Status Word 0

Word 0 contains the main storage address of the last attempted cycle-steal transfer. This residual address may be a data address, DCB address, or status address. The following chart shows which type of address the residual address can be for various error conditions. Where more than one possibility is shown, the program must decide which type of address cycle-steal status word 0 contains.

Error condition	Residual Address DCB address	Residual Address Status address	Residual Address Data address
Delayed command reject	N/A	N/A	N/A
Incorrect-length record		*	X
DCB specification check	*		
Storage data check	X		X
Invalid storage address	X	X	X
Protect check	X	X	X
Interface data check	X	X	X
Overrun		X	X
Time-out	X		X
Modem interface error	X		X
Block check error	X		X
Abort		X	X
Idle or inactivity detected	X		X
Nonproductive receive	X		X

Status Word 1

Word 1 contains the residual byte count. This is the byte count remaining when an operation ends due to an error.

Status Word 2

Words 2 and 3 are the only words required for attachment or interface error analysis.

Bit 0 - Overrun: During a receive operation, this condition occurs if the attachment is unable to transfer the contents of the storage data register to processor storage before it is time to reload the register. During a transmit operation, an overrun occurs if the attachment is unable to reload the storage data register in time to keep a steady stream of data going out on the line.

Bit 1 - Abort: During a receive operation, this bit is set to 1 if the attachment receives eight consecutive 1-bits (no 0-bits insertion) within a normal frame. This indicates that the transmitting station decided to end the frame prematurely. This condition is recoverable by the program. If the condition occurs frequently, contact the remote location to determine if the program is aborting frames.

Bit 2 - Long Frame: This condition indicates that the byte count decremented to 0 and no ending flag was received. If using the SE bit, adjust buffer size and DCB byte count to accommodate more data. If not using the SE bit, contact the remote location and determine the exact byte count necessary.

Bit 3 - Block Check Error: In receive operation only, the attachment sets this bit to 1 if the frame check sequence received by the attachment is incorrect. The probable cause is a line error. The program may request retransmission for recovery.

Bit 4 - Time-Out: The attachment sets this bit to 1 if a DSR time-out or a Disable DTR time-out occurs. This is an attachment to modem handshaking problem during an enable or disable command. Increase value of timer 1 to allow DSR to become either active or inactive (depending upon operation requested).

Bit 5 - Idle Detected: This error occurs if the attachment detects an idle condition after timer 1 times out during a receive operation The attachment expected to receive a frame and the line went idle. Increase timer 1 value or notify remote location that turnaround is too slow.

Bit 6 - Nonproductive Receive Time-Out: Indicates that a nonproductive receive time-out occurred. The remote station is not transmitting frames soon enough after being polled within the limits specified in timer 2. The condition can occur at a line break or on a long frame.

If it occurs frequently, contact remote station to resolve problem.

Bit 7 - Modem Interface Error: The attachment sets this bit to 1 under the following conditions:

- DSR is not active when either a transmit or receive operation is initiated.
- DTR, DSR, RTS, or CTS is lost during a transmit operation.
- DTR or DSR is lost during a receive operation.
- On a transmit operation, timer 1 times out before CTS is activated by the modem.
- CTS on for more than 100 milliseconds while RTS is off at the beginning of a transmit operation.

Examine status word 3 bits 0 through 3 for an error condition. Adjust timer value, if necessary, and retry.

Bits 8-12: Not used and are set to 0s.

Bit 13 - Business Machine Clock: This bit indicates that the internal clocking jumper is installed.

Bit 14 - Generate Answer-tone: This bit indicates that the answer-tone jumper is installed in the attachment. The attachment provides a 3-second answer tone when a ring is detected.

Bit 15 - Modem Delay: Some modems require that RTS remain active for a time after the attachment transmits the ending flag. When this jumper is installed, the attachment maintains RTS in the active condition and transmits trailing pad characters for 2-milliseconds after sending the ending flag.

Status Word 3

Bit 0 - Data Terminal Ready: An outbound signal from the attachment to the modem signifying that remote station is ready to communicate. It expects data-set-ready (bit 1) from the modem. DTR is set by the DTR enable type DCBs.

Bit 1 - Data Set Ready: This is either an inbound signal to the attachment from the modem in response to DTR (bit 0) or an indication of power-on from a leased-line modem. If the DSR is set to 1, then install the DTR jumper on the attachment.

Bit 2 - Request-to-Send: This bit indicates an outbound signal from the attachment to the modem requesting that the modem prepare for data transmission. It expects a CTS (bit 3) return from the modem. Some duplex modems always signal CTS as a power-on indication. In this case, the RTS jumper on the attachment should be installed.

Bit 3 - Clear-to-Send: An inbound signal to the attachment from the modem indicating the modem is ready to transmit data.

Bit 4 - Ring Indicator: An inbound signal to the attachment indicating the modem has detected a ring condition on the line.

Bit 5 - Half-Rate Selected: An outbound signal from the attachment to the modem requesting the modem to operate at half its normal bit rate. If internal clocking is used, this line causes the attachment to provide clocking at 600 bps.

Bit 6 - Transmit Mode Latch: This bit does not interface to the modem. It indicates that the attachment hardware is set up to transmit.

Bit 7: Not used.

Bits 8-15 - Secondary Station Address: These bits contain the secondary station address of the attachment, as designated by jumpers on the attachment card.

Condition Codes and Status Information

Operate I/O Instruction Condition Codes

Only the following bit combinations are valid:

Prepare command	0110	0000
Device Reset command	0110	1111
Start command	0111	XXXX
Read ID command	0010	0000
Halt I/O command	1111	0000
Write command	010X	XXXX

X   The attachment does not detect these bits during the Operate I/O instruction.

*   The SDLC attachment cannot process a Write command; however, it does accept the command. When the Operate I/O instruction is issued, the attachment reports delayed command reject by using an exception interrupt request with ISB bit 1 set to 1.

The SDLC feature may present a variety of Operate I/O condition codes. These are shown below for each type of Operate I/O command with a recommended program recovery or terminate procedure (notify user).

CC value	Even	Carry	Overflow	Meaning
0	0	0	0	Not attached
1	0	0	1	Busy
2	0	1	0	Busy after reset
3	0	1	1	Command reject
4	1	0	0	Intervention required
5	1	0	1	Interface data check
6	1	1	0	Controller busy
7	1	1	1	Satisfactory

Interrupt Condition Codes

Interrupt condition code 4 (attention) indicates that the ring indicator line from the modem is active. Condition codes 6 and 7 indicate that the ring indicator line is active in conjunction with another interrupt-causing condition.

CC value	Even	Carry	Overflow	Meaning
0	0	0	0	Controller end (not reported)
1	0	0	1	PCI (not reported)
2	0	1	0	Exception
3	0	1	1	Device end
4	1	0	0	Attention
5	1	0	1	Attention and PCI (not reported)
6	1	1	0	Attention and exception
7	1	1	1	Attention and device end

Interrupts can occur only after acceptance of the following commands:

- Prepare
- Start
- Start Cycle-Steal Status
- Start Diagnostic 1
- Start Diagnostic 2

Status

Interrupt Information Byte

When the attachment presents an interrupt request to the processor, the interrupt information byte is used to record information that cannot be indicated to the program by the condition codes. If interrupt information bytes bit 0 are set to 1 when condition code 3 is reported, the SE bit was set to 1 for the previous receive operation and a suppressible error occurred. When interrupt condition code 2 or 6 is reported, the interrupt information byte has a fixed format called the interrupt status byte.

The processor detects the interrupt status byte in bits 0 through 7 of the interrupt ID word. The format of the interrupt status byte follows:

Bit 0 - Device Dependent Status Available: If this bit is set to 1, additional status is available through the Start Cycle-Steal Status command. A discussion of this status was previously described in this chapter.

Bit 1 - Delayed Command Reject: This bit is set to 1 under the following conditions:

- The command field of the IDCB contains an invalid function or modifier bit combination.
- The immediate data field of the IDCB contains an odd DCB address.

Bit 2 - Incorrect Record Length: This error is reported only during receive operations and only when bit 4 of the DCB control word is set to 0. Incorrect record length indicates that the attachment detected a mismatch between the byte count and the frame length or that the poll-final bit was on in the frame just received (when chaining).

A Start Cycle-Steal Status command may be issued to obtain the residual byte count and the address of the last attempted data transfer.

Bit 3 - DCB Specification Check: This bit is set to 1 if one of the following conditions occurs:

- The DCB contains an odd address in the chaining address (word 5).
- The byte count field (DCB word 6) contains a value other than 8, it applies only to Start Cycle- Steal Status commands.
- The data address (DCB word 7) contains an odd address, it applies only to Start Cycle-Steal Status, Start Diagnostic 1 or Start Diagnostic 2 commands.
- The status address (DCB word 4) contains an odd address - applies only to receive operations when the SE bit is set to 1.
- The byte count (DCB word 6) is set to 0 for either a transmit operation or a receive operation.
- Bit 2 of the DCB control word is not set to 1 for a Start Cycle-Steal Status, Start Diagnostic 1 or Start Diagnostic 2 command.
- More than one operation is specified in the control word (word 0) of the DCB.
- Bit 3 of DCB word 0 is set to 1.
- Bit 1 of DCB word 0 is set to 1.
- The byte count field (DCB word 6) contains a value other than 12 (applies only to Start Diagnostic 1 or Start Diagnostic 2 commands).

Bit 4 - Storage Data Check: This bit is set to 1 during cycle-steal output (storage to attachment) operations only. It indicates that the storage location accessed during the current output cycle contains incorrect parity. The parity in main storage is not corrected. The attachment ends the operation.

Bit 5 - Invalid Storage Address: This bit is set to 1 if an address presented by the attachment during a cycle-steal to or from storage exceeds the storage size of the system. The attachment ends the operation.

Bit 6 - Protect Check: This bit is set to 1 if the attachment attempts to store data into a storage location without the correct cycle-steal address key.

Bit 7 - Interface Data Check: This bit is set to 1 if a parity error is detected on the interface during a cycle-steal data transfer. The condition can be detected by the channel or the attachment. In either case, the operation is ended and an exception interrupt request is presented to the processor.

Status After Reset

There are several methods of resetting some or all of the circuits in the attachment. They are:

Reset	Action
Power-on reset	All attachment components are reset to 0.
System reset	All attachment components (except DTR, half-rate, and the residual address) are reset to 0.
Halt I/O command	All attachment components (except DTR, prepared level, I-bit, half-rate, residual address, residual byte count, and residual DCB information) are reset to 0 by this command.
Device Reset command	This command resets the same component as the Halt I/O command.

Jumper Options

Installing jumpers on the feature card allows selection of of the following options:

Internal Clocking: With this jumper installed, the attachment provides clocking at 600 bps or 1,200 bps (selectable by programming).

Generate Answer-tone: With this jumper installed, the attachment provides a 3-second answer tone after the modem activates DSR in response to the attachment activating DTR. This jumper should not be installed if the modem provides an answer-tone.

Request-to-Send: If this jumper is installed, the attachment maintains RTS in an active condition. This eliminates modem turnaround delay when using a duplex modem. This option must always be selected when using a modem that always keeps CTS active.

Data Terminal Ready: If this jumper is installed, the attachment maintains DTR in an active condition. This option must not be selected for switched-line operation; it must be selected when using a modem that always keeps DSR active.

Modem Delay: Some modems can lose the last character at the end of a transmit operation. If this jumper is installed, the attachment keeps the transmit data line in a marking condition for 2 milliseconds after sending the last character to the modem and before resetting RTS. This prevents the last character from being lost.

Secondary Station Address: If the attachment is to be used as a secondary station, the station address is assigned by installing jumpers that correspond to bits of the address.

Note: For cable information, see the maintenance logic diagrams and the *Customer Site Preparation Manual*, GA34-0550.

Communications Indicator Panel

This optional panel can display various conditions and registers in the attachment. In addition, the DTR line to the modem can be reset from this panel.
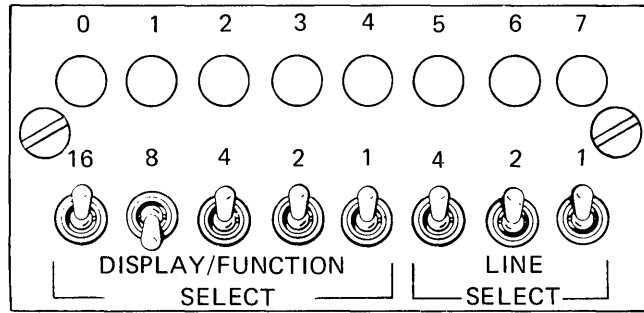
LINE SELECT Switches

The three LINE-SELECT switches are used only with multiple-line communication devices. The SDLC attachment does not use these switches.

DISPLAY/FUNCTION SELECT Switches

The DISPLAY/FUNCTION SELECT switches determine what information is displayed in the indicator panel. The following two charts show valid switch settings and the information that is displayed in the indicator panel.

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
00000	0-7	High-order byte of DCB word 0 (control word)
00001	0-7	Low-order byte of DCB word 0 (control word)
00010	0-7	High-order byte of DCB word 5 (chain address)
00011	0-7	Low-order byte of DCB word 5 (chain address)
00100	0-7	High-order byte of DCB word 6 (byte count)
00101	0-7	Low-order byte of DCB word 6 (byte count)
00110	0-7	High-order byte of DCB word 7 (data address)
00111	0-7	Low-order byte of DCB word 7 (data address)
01000	0-7	Low-order byte of word 1 of the Residual Status Block
01001	0-7	Interrupt status byte (ISB)
01010	0-7	High-order byte cycle-steal status word 2
01011	0-7	High-order byte of DCB word 4 (status address)
01100	0-7	Low-order byte of DCB word 4 (status address)
01101	0-7	SDLC control 0 Flag detected 1 Buffer service request 2 Idle detect 3 Abort detect 4 Overrun 5 Business machine clock selected 6 Attachment generated answer-tone 7 Modem delay selected
01110	0-7	Secondary station address
10100	0-7	Low-order byte of DCB word 1 (timer 2)
10101	0-7	High-order byte of DCB word 1 (timer 1)
11100	0-7	Lamp test
11101	0-7	Modem status 0 Data terminal ready 1 Data set ready 2 Request to send 3 Clear to send 4 Ring indicator 5 Half-rate select 6 Transmit mode 7 Receive mode
11110*		Enable for DTR reset
11111*		Reset DTR

Figure 2. Indicator panel information - SDLC feature

* To reset DTR, the switches must first be set to 11110, then to 11111. This prevents resetting DTR unintentionally.

Note: The indicator panel functions in one of three manners during the period of time where the attachment is monitoring for the initial flag in receive mode:

1. Display all settings as indicated in table.

2. Locked out display.

3. Display all settings when the NPR and idle timers are not used, otherwise locked out.

This function is dependent on the hardware level.

Error Recovery

Error recovery for the Synchronous Data Link Control Communications is as follows:

1. Inspect the Operate I/O condition code and use the following chart:

Operate I/O command	Operate I/O CC	Recommended action
Read ID	0	Terminate; device not attached
	1,2,4,6	Terminate; hardware error
	3	Terminate; examine IDCB function
	5	Retry; terminate if problem persists
	7	Satisfactory
Prepare	0,1,2,4,6	Terminate
	3	Terminate; examine IDCB function
	5	Retry; if problem persists, abort
	7	Satisfactory
Device Reset	0	Terminate; device not attached
	1,2,4,6	Terminate
	3	Examine IDCB function; if OK, abort
	7	Satisfactory
Start, Start Cycle-Steal status, Start Diagnostic 1 and 2	0	Device not attached: terminate
	1	Device reset; retry; If trouble persists, terminate
	2	Retry; if trouble persists, terminate
	3	Examine function in IDCB; if correct, terminate
	4	Terminate
	5	Retry; if trouble persists, terminate
	6	Terminate
	7	Satisfactory

2. Inspect the interrupt condition code.

- If the interrupt condition code is 3, end.
- If the interrupt condition code is a 2, use the following chart.

Interrupt status byte (hex)	Recommended action
80	Issue a Start Cycle-Steal Status command; examine bits to determine further action.
40	Examine IDCB for invalid function modifier or odd DCB address; correct error condition and retry.
20	Occurs during a receive operation; indicates byte count reduced to 0 and no ending flag was detected, or ending flag was detected and byte count was not reduced to 0; adjust receive data buffer size and byte count and retry; this error can occur only when the control word bit 4 is set to 0.
10	Indicates DCB being processed has an odd chain address (word 5); a start cycle-steal status DCB has a byte count other than 8 or an odd address; a transmit or receive DCB has a byte count of zero; the I/O bit of the DCB control word is incorrect; a diagnostic-type DCB has incorrect byte count or odd data address; correct the error and retry.
08	Storage data check; retry operation; if error persists, end.
04	Invalid storage address; correct program and retry.
02	Protect check; verify the protect key and retry.
01	Interface data check; retry once and end if the error persists.

Appendix A. SDLC Reference Summary

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,2,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,5,6,7
7D	Start Diagnostic 1	0,1,2,5,6,7
7E	Start Diagnostic 2	0,1,2,5,6,7
7F	Start Cycle-Steal Status	0,1,2,5,6,7

Device Control Block (DCB)

DCB (device control block)

Word		
0	Control word	
1	Timer 1	Timer 2
2	Not used (0's)	
3	Not used (0's)	
4	Status address	
5	Chain address	
6	Byte count	
7	Data address	

0   15

Control Word

Bit	Meaning
0	Chaining flag
1	Not used - zero
2	Input flag
3	Not used - zero
4	Suppress exception (SE)
5,6,7	Cycle-steal address key
8	Half rate
9	NRZI coding
10	Enable terminal
11	Disable terminal
12	Pad (leading)/control
13	Secondary/primary
14	Transmit operation
15	Hold line active (HLA)

Cycle-Steal Status Words

Word 0

Bit	Meaning
1-15	Residual address

Word 1

Bit	Meaning
1-15	Residual byte count

Word 2

Bit	Meaning
0	Overrun
1	End
2	Long frame
3	Block check error
4	Timeout
5	Idle detected
6	Nonproductive receive timeout
7	Modem interface error
8-12	Not used - zero
13	Business machine clock selected
14	Answer-tone jumper installed
15	Modem delay jumper installed

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request-to-send
3	Clear-to-send
4	Ring indicator
5	Half rate selected
6	Transmit mode latch
7	Not used - zero
8-15	Secondary station address

Residual Status Block

Word 0

Bit	Meaning
0-15	Residual byte count

Word 1

Bit	Meaning
0	End-of-chain (EOC)
1-7	Not used - zero
8	Overrun
9	End
10	Long frame
11	Block check error
12-14	Not used - zero
15	No exception (NE)

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents
2,6	Cycle-steal interrupt status byte
3	Bit 0 suppressed exception, bits 1-7 zero
4,7	Always zero

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

* Zero for a device attached to a 4952 or 4953 processor.

Appendix B. Communications Operator's Self-Test Procedure

The communication adapter operator self-test program needs a minimum system configuration of:

Series/1 processor with 16K storage, a diskette drive feature 4964 or 4962 model 2, a programmer console feature 5650, and one communication adapter feature 2090.

1. Remove power, disconnect the modem cable at the modem and connect the wrap connector at the modem end of the cable as follows:

Modem cable part number	Wrap connector part number
1632208	2704136
1632919	*
919422	**

*Do not disconnect the modem cable but place the switch in the cable extension part number 2722052 in the test position.

**Do not disconnect the modem cable but place the switch in the cable extension part number 919423 in the test position.

2. Insert the basic diskette.

3. Press the load button on the programmer console.

4. If the system has only a programmer console, go to step 10.

5. Wait for the input/output device (as configured in the diagnostic diskette) to print the following message:

RDY

ENTER

6. Begin the operator self-test program be entering B3CEF on the input/output device.

7. The output device will then print:

ENTER DEVICE ADDRESS AND LOOP COUNT

ENTER

8. Enter FDAXX (where DA=device address and XX=loop count in hexadecimal).

    Example:

    F1801 (DA=18, loop count=01).

9. Wait for one of the following messages to appear then take the appropriate operator action:

Message:

DEVICE ADDRESS ERROR

REENTER DEVICE ADDRESS AND LOOP COUNT

ENTER

Operator action:

Verify that the device address is correct and call the service organization or return to step 8.

Message:

TEST WAS SUCCESSFUL

Operator action:

None, self-explanatory.

Message:

THE TEST FAILED, CALL THE SERVICE ORGANIZATION

Operator action:

Verify that the cable and wrap connector have the correct part numbers and call the service organization or return to step 8.

After the loop count has been exhausted, the program returns to step 7. At this time, you may run the test again or end the program by returning the system to the operating state. (Steps 10 through 16 of this procedure are for systems with only a programmer's console.)

Note: The running time for feature 2090 per pass is 12 seconds:

10. Wait for hex 3800 in the lights of the programmer console.
11. Press the data buffer button and enter 000B, then press the console interrupt button. Press the data buffer button again and enter 3CEF, then press the console interrupt button twice.
12. Wait for 3CE1 on the lights of the programmer console.
13. Press data buffer and enter 001F, then press the console interrupt button.
14. Press the data buffer and enter DAXX (where DA=device address and XX=loop count). Press the console interrupt button twice.

15. Wait for one of the following values to appear in the lights of the programmer console.

Value in lights	Operator action
3CE2 (Device address error)	Verify the address is correct and call the service organization or go to step 1.
3CE3 (Test successful)	Self-explanatory
3CE4 (The test failed, call the service organization	Verify that the cable wrapped is the correct one and call the service organization or return to step 11.

16. Press the data buffer button, enter 0006 and depress the console interrupt button twice. Wait for the lights to indicate 3CE1 and proceed to step 12 to run the test again, if desired, or return the system to the operating state.

Appendix C. SDLC Adapter Initialization
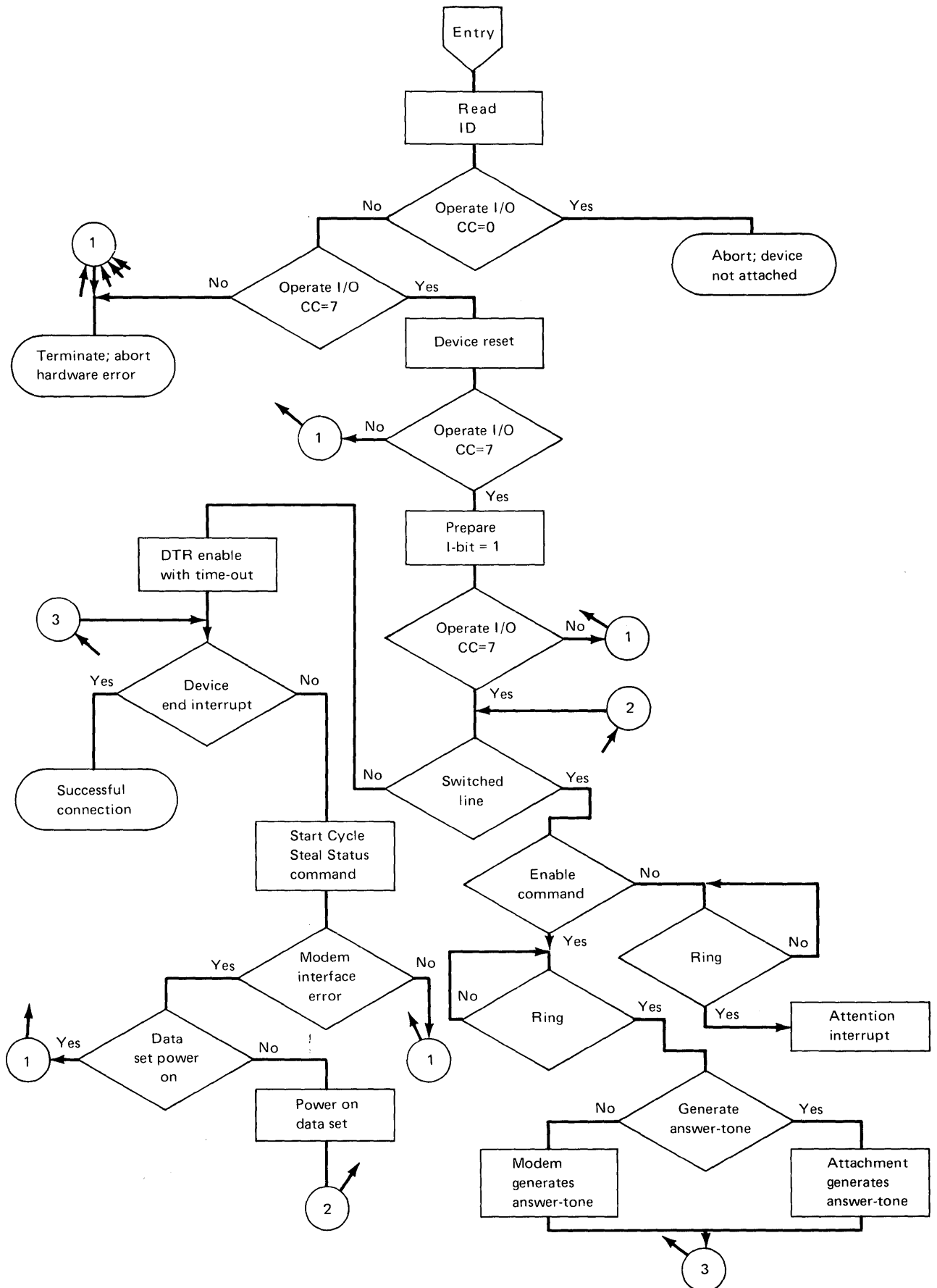
Appendix D. Transmission Codes

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/correspondence
0	00	0000 0000	NUL	NUL	NUL		
1	01	0001	SOH	SOH	NUL	space	space
2	02	0010	STX	STX		1	1,]
3	03	0011	ETX	ETX	@		
4	04	0100	PF	EOT		2	2
5	05	0101	HT	ENQ	space		
6	06	0110	LC	ACK			
7	07	0111	DEL	BEL		3	3
8	08	1000		BS		4	5
9	09	1001	RLF	HT			
10	0A	1010	SMM	LF	P (even parity)		
11	0B	1011	VT	VT	P (odd parity)	5	7
12	0C·	1100	FF	FF	0 (even parity)		
13	0D	1101	CR	CR	0 (odd parity)	6	6
14	0E	1110	SO	SO		7	8
15	0F	1111	SI	SI			
16	10	0001 0000	DLE	DLE		8	4
17	11	0001	DC1	DC1			
18	12	0010	DC2	DC2	H (even parity)		
19	13	0011	TM	DC3	H (odd parity)	9	0
20	14	0100	RES	DC4	((even parity)		
21	15	0101	NL	NAK	((odd parity)	0	z
22	16	0110	BS	SYN		Ⓓ (EOA)	Ⓓ (EOA),9
23	17	0111	IL	ETB			
24	18	1000	CAN	CAN			
25	19	1001	EM	EM			
26	1A	1010	CC	SUB			
27	1B	1011	CU1	ESC	X		
28	1C	1100	IFS	FS		uppercase	uppercase
29	1D	1101	IGS	GS	8		= ^
30	1E	1110	IRS	RS			
31	1F	1111	IUS	US		Ⓒ (EOT)	Ⓒ (EOT)
32	20	0010 0000	DS	space	EOT	@	t
33	21	0001	SOS	!	EOT		
34	22	0010	FS	"	D (even parity)		
35	23	0011		#	D (odd parity)	/	x
36	24	0100	BYP	$	S (even parity)		
37	25	0101	LF	%	S (odd parity)	s	n
38	26	0110	ETB	&		t	u
39	27	0111	ESC	'			
40	28	1000		(			
41	29	1001		)		u	e
42	2A	1010	SM	*		v	d
43	2B	1011	CU2	+	T		
44	2C	1100		,		w	k
45	2D	1101	ENQ	-	4		
46	2E	1110	ACK	.			
47	2F	1111	BEL	/		x	c
48	30	0011 0000		0	forms feed		
49	31	0001		1	forms feed	y	l
50	32	0010	SYN	2		z	h
51	33	0011		3	L		
52	34	0100	PN	4			
53	35	0101	RS	5	,		
54	36	0110	UC	6			

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/correspondence
55	37	0011 0111	EOT	7		Ⓢ (SOA),comma	b
56	38	1000		8			
57	39	1001		9			
58	3A	1010		:	\ (even parity)		
59	3B	1011	CU3	;	\ (odd parity)	index	index
60	3C	1100	DC4	<	< (even parity)		
61	3D	1101	NAK	=	< (odd parity)	Ⓑ (EOB)	
62	3E	1110		>			
63	3F	1111	SUB	?			
64	40	0100 0000	space	@		Ⓝ ,-	!
65	41	0001		A	EOA		
66	42	0010		B	B (even parity)		
67	43	0011		C	B (odd parity)	i	m
68	44	0100		D	" (even parity)		
69	45	0101		E	" (odd parity)	k	
70	46	0110		F		l	v
71	47	0111		G			
72	48	1000		H			
73	49	1001		I		m	'
74	4A	1010	¢	J		n	r
75	4B	1011	.	K	R		
76	4C	1100	<	L		o	i
77	4D	1101	(	M	2		
78	4E	1110	+	N			
79	4F	1111	]	O		p	a
80	50	0101 0000	&	P	line feed		
81	51	0001		Q	line feed	q	o
82	52	0010		R		r	s
83	53	0011		S	J		
84	54	0100		T			
85	55	0101		U	*		
86	56	0110		V			
87	57	0111		W		$	w
88	58	1000		X			
89	59	1001		Y			
90	5A	1010	!	Z	Z (even parity)		
91	5B	1011	$	[	Z (odd parity)	CRLF	CRLF
92	5C	1100	*	\	: (even parity)		
93	5D	1101	)	]	: (odd parity)	backspace	backspace
94	5E	1110	;	Λ		idle	idle
95	5F	1111	¬	_			
96	60	0110 0000	-	`	ACK		
97	61	0001	/	a		&	j
98	62	0010		b		a	g
99	63	0011		c	F		
100	64	0100		d		b	
101	65	0101		e	&		
102	66	0110		f			
103	67	0111		g		c	f
104	68	1000		h		d	p
105	69	1001		i			
106	6A	1010	¦	j	V (even parity)		
107	6B	1011	,	k	V (odd parity)	e	
108	6C	1100	%	l	6 (even parity)		
109	6D	1101	_	m	6 (odd parity)	f	q
110	6E	1110	>	n		g	comma
111	6F	1111	?	o			
112	70	0111 0000		p		h	/
113	71	0001		q	shift out		
114	72	0010		r	N (even parity)		

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/correspondence
115	73	0011		s	N (odd parity)	i	y
116	74	0100		t	. (even parity)		
117	75	0111 0101		u	. (odd parity)		
118	76	0110		v		Ⓨ ,period	
119	77	0111		w			
120	78	1000		x			
121	79	1001		v			
122	7A	1010	:	z		horiz tab	tab
123	7B	1011	#	{	↑		
124	7C	1100	@	|		lowercase	lowercase
125	7D	1101	'	}	>		
126	7E	1110	=	~			
127	7F	1111	"	DEL		delete	
128	80	1000 0000					
129	81	0001	a		SOM	space	space
130	82	0010	b		A (even parity)	=	±,[
131	83	0011	c		A (odd parity)		
132	84	0100	d		! (even parity)	<	@
133	85	0101	e		! (odd parity		
134	86	0110	f				
135	87	0111	g			;	#
136	88	1000	h		X-ON	:	%
137	89	1001	i				
138	8A	1010					
139	8B	1011			Q	%	&
140	8C	1100					
141	8D	1101			1	'	¢
142	8E	1110				>	*
143	8F	1111					
144	90	1001 0000			horiz tab	*	$
145	91	0001	j		horiz tab		
146	92	0010	k				
147	93	0011	l		I	(	)
148	94	0100	m				
149	95	0101	n		)	)	Z
150	96	0110	o			Ⓓ (EOA),"	(
151	97	0111	p				
152	98	1000	q				
153	99	1001	r				
154	9A	1010			Y (even parity)		
155	9B	1011			Y (odd parity)		
156	9C	1100			9 (even parity)	uppercase	uppercase
157	9D	1101			9 (odd parity)		
158	9E	1110					
159	9F	1111				Ⓒ (EOT)	Ⓒ (EOT)
160	A0	1010 0000			WRU (even)	¢	T
161	A1	0001	~		WRU (odd)		
162	A2	0010	s				
163	A3	0011	t		E	?	X
164	A4	0100	u				
165	A5	0101	v		%	S	N
166	A6	0110	w			T	U
167	A7	0111	x				
168	A8	1000	y				
169	A9	1001	z			U	E
170	AA	1010			U (even parity)	V	D
171	AB	1011			U (odd parity)		
172	AC	1100			5 (even parity)	W	K

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/ correspondence
173	AD	1101			5 (odd parity)		
174	AE	1110					
175	AF	1111				X	C
176	B0	1011 0000					
177	B1	0001			return	Y	L
178	B2	0010			M (even parity)	Z	H
179	B3	1011 0011			M (odd parity)		
180	B4	0100			- (even parity)		
181	B5	0101			- (odd parity)		
182	B6	0110					
183	B7	0111				Ⓢ (SOA), |	B
184	B8	1000					
185	B9	1001					
186	BA	1010					
187	BB	1011			]	index	index
188	BC	1100					
189	BD	1101			=	Ⓑ (EOB)	
190	BE	1110					
191	BF	1111					
192	C0	1100 0000	{		EOM (even)	Ⓝ ,—	
193	C1	0001	A		EOM (odd)		
194	C2	0010	B				
195	C3	0011	C		C	J	M
196	C4	0100	D				
197	C5	0101	E		#	K	
198	C6	0110	F			L	V
199	C7	0111	G				
200	C8	1000	H				
201	C9	1001	I		X-OFF	M	"
202	CA	1010			S (even parity)	N	R
203	CB	1011			S (odd parity)		
204	CC	1100	ʃ		3 (even parity)	O	I
205	CD	1101			3 (odd parity)		
206	CE	1110	⊤				
207	CF	1111				P	A
208	D0	1101 0000	}				
209	D1	0001	J		vertical tab	Q	O
210	D2	0010	K		K (even parity)	R	S
211	D3	0011	L		K (odd parity)		
212	D4	0100	M		+ (even parity)		
213	D5	0101	N		+ (odd parity)		
214	D6	0110	O				
215	D7	0111	P			!	W
216	D8	1000	Q				
217	D9	1001	R				
218	DA	1010					
219	DB	1011			[	CRLF	CRLF
220	DC	1100					
221	DD	1101			;	backspace	backspace
222	DE	1110				idle	idle
223	DF	1111			PAD		
224	E0	1110 0000	\				
225	E1	0001			bell	+	J
226	E2	0010	S		G (even parity)	A	G
227	E3	0011	T		G (odd parity)		
228	E4	0100	U		, (even parity)	B	+
229	E5	0101	V		, (odd parity)		
230	E6	0110	W				

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/correspondence
231	E7	0111	X			C	F
232	E8	1000	Y			D	P
233	E9	1001	Z				
234	EA	1010					
235	EB	1011			W	E	
236	EC	1100					
237	ED	1101			7	F	Q
238	EE	1110				G	comma
239	EF	1111					
240	F0	1111 0000	0		shift in (even)	H	?
241	F1	0001	1		shift in (odd)		
242	F2	0010	2				
243	F3	0011	3		O	I	Y
244	F4	0100	4				
245	F5	0101	5		/		
246	F6	0110	6			Ⓨ , ⌐	—
247	F7	0111	7				
248	F8	1000	8				
249	F9	1001	9				
250	FA	1010	LVM		⟵ (even parity)	horiz tab	tab
251	FB	1011			⟵ (odd parity)		
252	FC	1100			? (even parity)	lowercase	lowercase
253	FD	1101			? (odd parity)		
254	FE	1110					
255	FF	1111			delete / rub out	delete	

Note: When used with the BSCA, the software must maintain parity in bits 0–7 of each byte.

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Communications Feature Description

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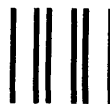
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