IBM

Series/1

GA34-0246-0

File No. S1-09

IBM Series/1
Feature-Programmable Multiline Communications Feature
Description

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Feature-Programmable Multiline Communications Feature
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First Edition (May 1983)

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Preface

This publication describes the Series/1 Feature-Programmable Multiline Communications Feature. The reader should be an experienced Series/1 assembler language programmer who writes, maintains, and debugs machine-level language programs. The reader should also be familiar with binary and hexadecimal numbering systems and stored-program concepts.

The subject matter is presented in two chapters and two appendices:

- Chapter 1 introduces the feature-programmable multiline communications feature.
- Chapter 2 describes the Series/1 machine-level language that the processor uses to transfer data to and from the attachment and devices that connect to the communications line.
- Appendix A contains a summary of the commands, device control blocks (DCBs), cycle-steal status words, and condition codes associated with the attachment feature.
- Appendix B lists the control and data characters used by the attachment feature.

Prerequisite Publications

- *IBM Series/1 Principles of Operation*, GA34-0152.
- Refer to *IBM Series/1 Graphic Bibliography*, GA34-0055, for the name and order number of the appropriate feature description manual for your processor.

Related Publications

- *IBM Series/1 System Selection Guide*, GA34-0143
- *IBM Series/1 Customer Site Preparation Manual*, GA34-0050
- *IBM Series/1 Pocket Digest*, GX34-0104

Contents

Chapter 1. Introduction

This chapter provides an overview of the Feature-Programmable Multiline Communication feature which uses asynchronous or synchronous transmission, depending on which of these options is programmed. Up to eight lines can operate at 7,200 bits per second (bps) or at combinations of different speeds.

The programmable multiline attachment controller is designed to provide control circuitry for one or two programmable 4-line adapter features. The programmable multiline attachment contains hardware and a microprocessor to service the 4-line adapters.

Each line of the multiline communication feature is programmable. The serial transfer of data to and from remote terminals or host systems is described in this chapter. The following communication characteristics apply:

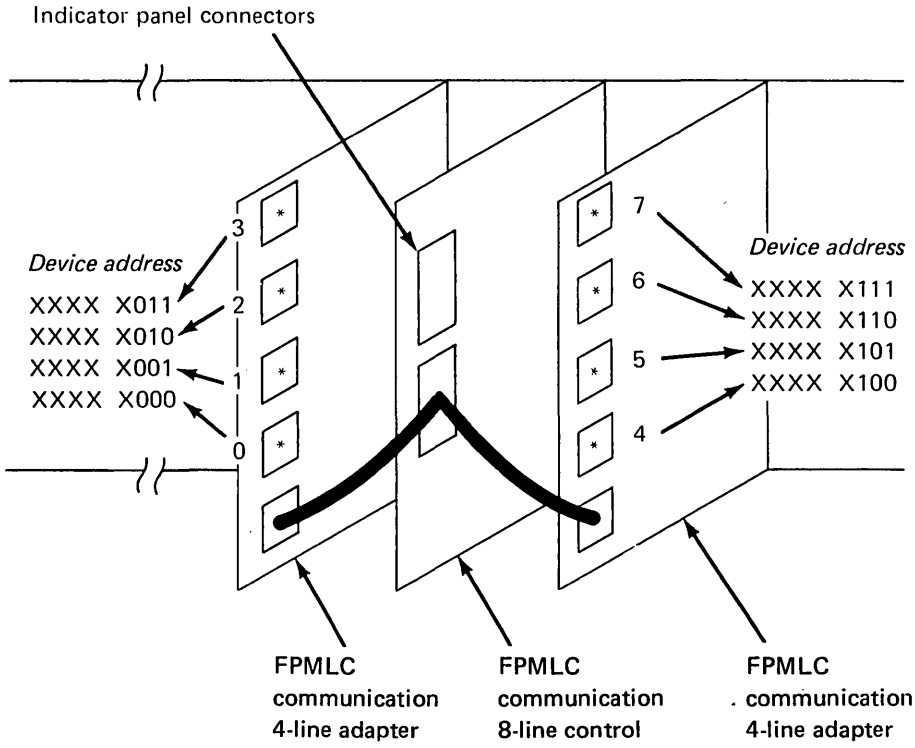
- Data transmission is serial-by-bit, using either asynchronous (start-stop) or synchronous methods of character transmission.
- The feature can communicate with different terminals/systems using ASCII or any transmission code with 5, 6, 7, or 8 bits per character.
- The program defines line control characters.
- The bit rate can range from 37.5 to 1,200 bps, or from 300 to 19,200 bps. Aggregate throughput is 64,000 bps (based on a 12-bit character).
- Multipoint control is provided in which the program can recognize secondary station addresses in a multipoint network.
- The feature provides answer-tone generation and break character recognition.
- Internal and external (modem) clocking capability (asynchronous only).
- Block check character reception for one or two characters is provided.
- Parity generation and checking can be specified as odd, even, or no parity.
- The stop bit length can be either 1 or 2 characters.
- Synchronous operation can have either 1 or 2 synchronization characters.
- Up to seven different change-of-direction (COD) characters can be recognized.
- Echoplex capability.
- Current loop (20 milliampere) capability or EIA RS232C or CCITT V.24 Interface.
- Expanded mode provides for the following attachment operations:
  - — Continuous Receive
  - — Continuous echoplex
  - — Attention interrupt
  - — With the following character recognition and detection
    - Two-character COD
    - Two-character longitudinal redundancy check (LRC)
    - Extended COD with block check capability.

Configurations

The programmable communication control feature has a multiline configuration and provides control for up to eight lines. This configuration contains either two or

three feature cards: two cards for one to four lines, and three cards for five to eight lines.

Note: When referring to the Feature-Programmable 8-Line Communications Control and one or two Feature-Programmable 4-Line Communication Adapters the term attachment is used.



*Modem interface connectors

Note: XXXX = basic device address

Note: See "Jumper Options" for additional information.

Each line operates in a half-duplex mode (unless expanded mode is selected) and can be connected to a duplex modem to avoid excessive modem turnaround. If a line is connected to a duplex modem, the attachment still operates in half-duplex mode. However, the request-to-send jumper on the feature card should be installed.

Interfaces

An EIA[1]RS232-C and CCITT[2] V.24 interface is provided for each line. The interface directly drives or ends an external modem. The Feature-Programmable Multiline Communication feature also provides local attachment capabilities using a 20-milliampere current loop.

The attachment can communicate with remote stations over private lines, leased common-carrier facilities, or switched voice-grade common-carrier lines. It also can be directly connected to remote stations.

Some modems disconnect automatically when the communication feature's DTR signal is deactivated. To deactivate this signal, issue a Start command, with a disable operation specified in the device control block, or use the communications indicator panel.

1 Electronic Industries Association
2 The International Telegraph and Telephone Consultative Committee.

Data Links

Each communication line can operate with one of the following types of data links:

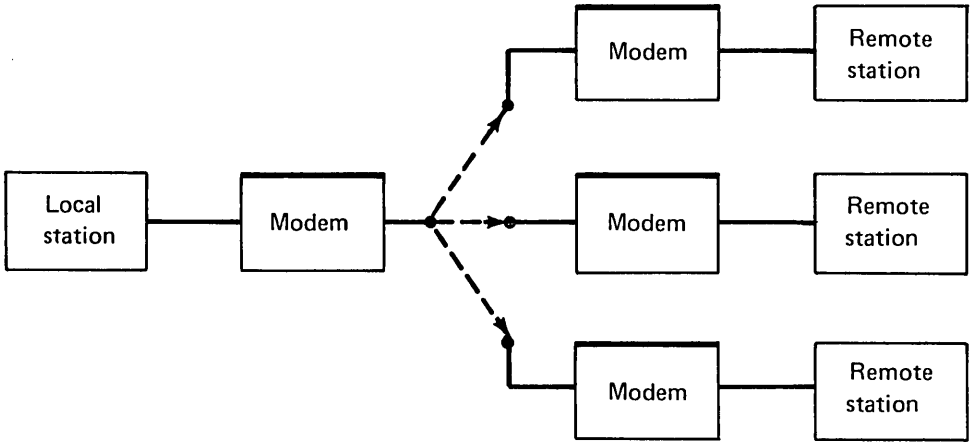
- Point-to-point nonswitched
- Point-to-point switched
- Multipoint nonswitched
- Direct connect

Point-to-Point Nonswitched

A point-to-point nonswitched data link consists of a local station connected to a single remote station. Such a line is nonswitched because of a permanent connection between the local station and the remote station through their respective modems.

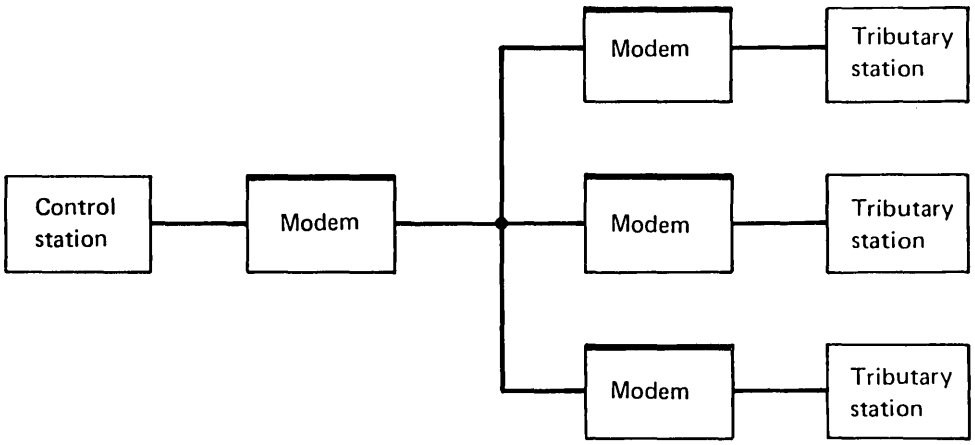
Point-to-Point Switched

A point-to-point switched data link consists of a local station connected to one of several remote stations after a link has been established between the local station and the remote station. The connection is maintained only for the duration of the communication.



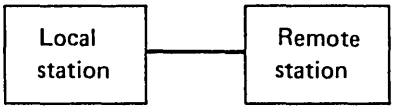
Multipoint Nonwsitched

A multipoint nonswitched data link consists of a primary station connected to several secondary stations through their respective modems. The primary station polls the secondary stations, using unique station addresses. Only the addressed station responds to the poll.



Direct Connect

A direct-connect data link consists of two stations connected using an EIA RS232-C, CCITT V.24, or current loop connection.



Establishing a Switched-Line Data Link

Initiating a Call

1. Load the program and make sure that the DTR signal is active.
2. Place the modem in talk mode.
3. Dial the remote station. The operator of the remote station will answer your call, or you will hear a high-pitched tone indicating that the remote modem is in auto-answer mode. If you talk to the operator, request that the remote modem be placed in data mode (or equivalent).
4. Place your modem in data mode (or equivalent) and hang up the receiver.

Answering a Call

1. Lift the receiver and talk to the operator of the other system.
2. Make sure that the program is loaded and the DTR signal is active.
3. Put your modem in data mode (or equivalent) before the caller puts the calling modem in data mode, and hang up the receiver.

Chapter 2. Operations

Transmission Codes

In asynchronous operation, the attachment supports transmission codes with 5, 6, 7, or 8 bits per character plus parity and one or two stop bits. The adapter always adds a start bit. In synchronous operation, the attachment supports any transmission code with 5, 6, 7, or 8 bits per character plus parity and one or two synchronization characters. (When two synchronization characters are used, they may be the same character or different characters.) The attachment operates either with no parity bit or with an additional bit for even or odd parity checking.

Any code that meets the preceeding requirements may be used at the programmer's discretion.

Receive/Transmit Mode

In normal receive mode, when the set control or set mode operations have been used to initialize the adapter, the following conditions are in effect:

- Seven change-of-direction (COD) characters are operable. Two of the CODs can be conditioned, by command, to receive a single character block check character.
- The receive with echoplex functions of the attachment are directly controlled by the Series/1 program using the defined start command operations. In this operating mode, the attachment receives data **only** when device control block (DCB) receive or DCB transmit with prereceive operations are being processed.

In normal receive mode, the attachment recognizes any one of the seven characters defined in the set mode/set control DCB and treats them as COD characters. When any one of the defined characters is received, the attachment presents a device end interrupt request or begins a DCB command chaining operation except when an incorrect length record is detected. All received characters are placed in storage.

In expanded mode (more information about expanded mode is described under "Data Reception" later in this chapter) the two-character COD causes the adapter to interpret the COD table in conjunction with a delineating character to determine an ending sequence. The user-specified delineating character is the first character received and the second character will be any of the seven programmable characters in the COD table. If two delineating characters are received consecutively followed by a character in the COD table, reception continues until a single delineating character followed by a COD is detected. Typically, the delineating character would be a DLE or ESC character.

In transmit mode, there is no control character comparison. All ending conditions must be controlled by byte count. When the byte count is reduced to 0, a device-end interrupt request or chaining occurs.

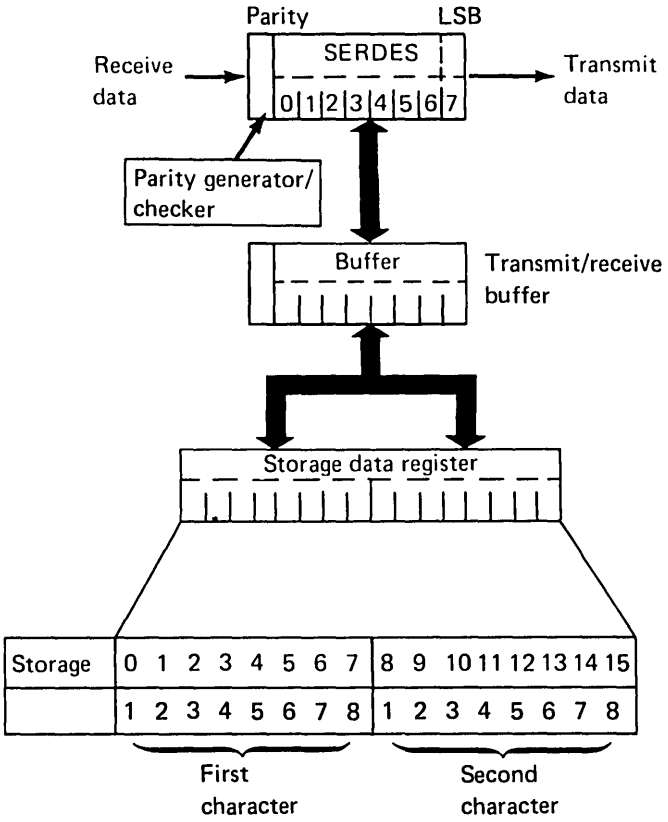
Note: See DCB description under "Start."

Data Flow

Valid data is placed in storage as it is received. If parity checking is requested, the data is checked for odd or even parity, and then the parity bit is removed from the data character. Data received with incorrect parity is placed in storage as hex 00. The data may be placed in storage exactly as received by placing the DISPLAY/FUNCTION SELECT switches on the communication indicator panel (if installed) to 11110. This applies to any and all lines.

In expanded mode, the inhibit zero insertion affects the adapter error procedure when a bad parity character is received (assumes parity check enabled). Normal adapter operation is to replace the bad parity character with a binary zero character. When this mode is enabled, the adapter does not zero the character but provides the character as it was received (incorrect data parity) with the parity bit removed.

Data is transmitted as it comes from storage; therefore, data must be organized in the exact bit configuration required by the code being used and in the sequence in which it is to be transmitted. Illustrated below is the attachment's storage data register and the bits in storage.



Note: The attachment transmits by sending out the low order bit of the byte first. The received characters are stored in the same manner; that is, the first bit received is the low order bit of the byte. If the character is less than 8 bits, it must be right justified. If the data address (DCB word 7) is odd, only one character is moved in or out of storage on the first data transfer.

Line Error Checking

The attachment checks for line errors through programmed parity checking. The DCB in set mode format specifies even, odd, or no parity. If even or odd parity is specified, the parity bit is generated by the adapter in transmit mode and checked by the adapter in receive mode.

Note: If the set control DCB is processed, no parity is specified.

Asynchronous operation requires that one or two stop bits (as defined in the set mode/set control DCB) be transmitted with each character. The attachment checks each received character for only one stop bit.

Timers

The **attachment** has two programmable timers (timer 1 and timer 2). Each timer is controlled by a 16-bit word in the DCB. Both timer values are reduced independently at a rate of 3.33 milliseconds per count. The maximum time that either timer can count is 218.2 seconds. The timers use a count (hex FFFF to 0000). When the count reaches 0000, the attachment begins or ends an operation. The timers are used with various operations defined in the control word of the DCB; these operations are listed below.

Timer 1

- Receive time-out (see "Receive with Time-Out" under "Operations" later in this chapter)
- Generate answer tone or break
- Transmit delay
  - — Slows down turnaround (pretransmit delay)
  - — Allows last character to exit modem before deactivating request to send (posttransmit delay)
- Carrier detect time-out

Timer 2

- Program delay
- Clear to send time-out
- Data set ready time-out
- Ring indicator time-out
- Data terminal ready disable delay

For detailed information about the use of the timers with particular operations, see the description of the operations.

Commands

The program begins all communication operations by issuing an Operate I/O instruction.

The Operate I/O instruction points to the immediate device control block (IDCB), which contains one of the following commands:

- Prepare
- Halt I/O
- Device Reset
- Read ID
- Write Data
- Start Control
- Start Diagnostic 1
- Start Diagnostic 2
- Start
- Start Cycle-Steal Status

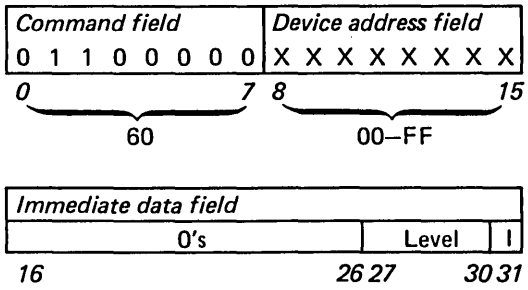
The programmer's must ensure that the program always tests the Operate I/O condition codes following an Operate I/O instruction.

Also, the programmer should exercise care in modifying the DCB words before an interrupt request signifying the end of the operation. All of the DCBs might not have been fetched because the attachment is slower that the Series/1 processor.

Prepare

The Prepare command is used to control the interrupt parameters of the addressed device. The data word contains the priority level and I-bit. The IDCB for the Prepare command has the following format:

IDCB (immediate device control block)



Level: This four-bit field specifies the priority interrupt level assigned to the device. Bits 27-30 indicate priority levels.

Example

Bits 27-30	Level
0000	0
0001	1
0010	2
0011	3

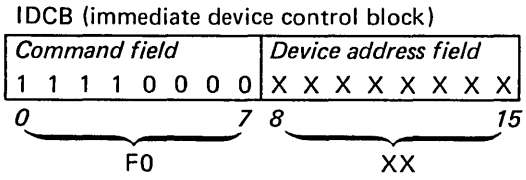
A Prepare command issued to any device on this attachment gives all of the devices in the attachment the same priority interrupt level. The I-bit information applies only to the specific device addressed.

I-Bit: This bit determines if the device is allowed to present interrupt requests. An I-bit value of 1 allows requests; a value of 0 prevents requests.

The prepared attachment stores the level data and presents it to the processor each time an enabled device presents an interrupt request. This data is reset during a system reset or a power-on reset, or is changed by the successful process of another Prepare command issued to the attachment. The Prepare command causes an interrupt request to be presented if one was pending on the device and the I-bit is set to 1. On a multiline attachment, the device returns an operate I/O condition code 1 to this command if it has an interrupt request pending, and the I-bit in the IDCB is set to 0.

Halt I/O

The Halt I/O command halts all I/O activity on the I/O channel. Any pending interrupt requests, including controller end (CC0), are cleared. Except for the fact that the I-bits and priority level do not change, this instruction performs the same function as a system reset. The format of the IDCB for this command follows:

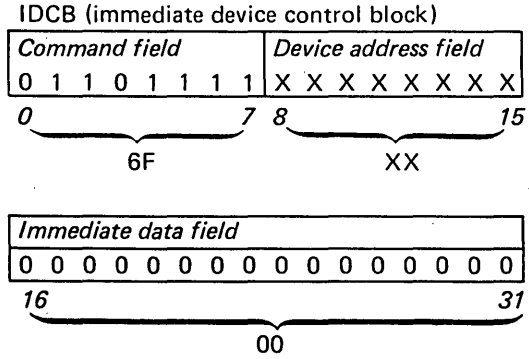


Device Reset

The Device Reset command resets the addressed device and clears any pending interrupt requests (except controller end). The following are not affected:

- Line control characters
- Bit rate constant
- Number of data bits specified by the DCB
- DTR line
- Controller end interrupt

(See "Status After Resets" later in this chapter.) The IDCB for the Device Reset command has the following format:



A Device Reset command issued to the attachment causes the attachment to become busy while the reset functions are being performed. A controller busy (CC6) is reported if a Start command follows a Device Reset or another Start command too closely. When the attachment is capable of accepting another command, a controller end interrupt request (CC0) is presented by the base address of the multiline attachment (line 0) at which time the program should reissue the Start command.

Read ID

The Read ID command puts the attachment's identification (ID) word into the IDCB's immediate data field. The ID word contains physical information about the attachment that can be used to tabulate the system's configuration. The Read ID command is generally used in diagnostic programming. The format of the IDCB for this command follows:

IDCB (immediate device control block)

Command field	*Device address field*
0 0 1 0 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
20	XX

Immediate data field
Identification word
16 ... *31*

Two-line	2116
Four-line	2216
Six-line	2316
Eight-line	2016

Note: If the controller card has jumpers installed for addresses that are not valid, the controller responds to commands as though the 4-line adapter card was present; therefore, the ID of the controller should match the number of attachment lines present to prevent errors. For example, an ID of 2016 or 2316 defines a controller with two 4-line attachments. If there is only one 4-line attachment present, the ID is 2216 or 2116.

Reference CE binder MLD sheet SC xxxx for controller card jumper layout.

Write Data

This command is provided as a way to process character by character operation in the expanded operating mode to provide programmed echoplex. DTR, DSR, RTS, CTS must be active when this command is issued.

This command is similar to a Transmit End Start command except there is no DCB associated with this command. Data is transferred to the attachment in the IDCB. Chaining, pre and posttransmit delays, and modem control operations are not supported. The addressed device is Device Busy until a Device End or Exception Interrupt is presented notifying the program that the adapter is capable of accepting more data.

The Write Data IDCB has the following format:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 0 1 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
50	00–7F

Immediate data field	
Data	0
16 ... *23*	*24* ... *31*

Start Control

The Start Control command is used for the following operations:

- Write attachment storage
- Read attachment storage
- Start trace
- Trace dump
- Set expanded mode

Note: See description of DCB see "Start."

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
7C	XX

Immediate data field
DCB address
16 ... *31*

Issuing this command can cause the attachment to become inoperable, if certain conditions/parameters are not adhered to. If this happens, the attachment can only be restored to operation by switching power off and then on again.

The data address (DCB word 7) must always be even. Otherwise, the attachment ends the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte is set to 1.

Write Attachment Storage: The DCB format for this operation follows:

Word	DCB (device control block)
0	Control word–0X00
1	Not used
2	Not used
3	Not used
4	Not used
5	Chain address–not used
6	Byte count–must be 432 (hex 1B0)
7	Data address–must be even

This operation begins if DCB word 0 bit 2 is set to 0 and the byte count is 432. Starting at the address specified in DCB word 7, the attachment cycle-steals 432 bytes of data from processor storage into storage associated with the attachment. A device end interrupt request is presented when the cycle-stealing is completed. The 432 bytes of data transferred is used by IBM Engineering to make functional changes in the attachment.

If DCB word 0 bit 2 is set to 0 and the byte count is not 432, the attachment ends the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte is set to 1.

Read Attachment Storage: The DCB format for this operation follows.

Word	DCB (device control block)
0	Control word–2X00
1	Not used
2	Not used
3	Not used
4	Not used
5	Chain address–not used
6	Byte count–must be 1024 (hex 0400)
7	Data address–must be even

This operation begins if DCB word 0 bit 2 is set to 1 and the byte count is 1024. Starting at the address specified in DCB word 7, the attachment cycle-steals 1024

bytes of data from the attachment into storage. A device end interrupt request is presented when the cycle-stealing is completed.

If DCB word 0 bit 2 is set to 1 and the byte count is not 1024, the attachment ends the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte is set to 1.

Start Trace: The DCB format for this operation follows.

DCB (device control block)

Word	
0	Control word—0000
1	Not used
2	Bit-dependent (see description below)
3	Not used
4	Not used
5	Chain address—not used
6	Byte count—must be 0
7	Data address—not used

This operation begins if DCB word 0 bit 2 is set to 0 and the byte count is 0. An array is generated in attachment storage to provide the following information about the last seven DCBs issued to a single address (only one address can be traced at a time):

- The DCB control words
- The DCB addresses
- The interrupt status byte and interrupt condition codes
- The cycle-steal status word 1s information

Data shifts through this array and is traced for predefined error conditions. These conditions are defined in DCB word 2 by having one or several bits set to 1.

The bits and their meanings follow:

Bit	Meaning
0	Overrun
1	Time-out
2	Log all status word 1 errors (all other bits must be off)
3	DCB reject
4	Not used
5	Parity error
6	Break detected
7	Stop bit error
8	Not used
9	Modem interface error
10-11	Not used
12	Error during prereceive/adapter buffer full
13-14	Not used
15	Adapter buffer not empty

After an error condition is detected, the trace operation stops and information about the last seven DCBs is available to the operator when the trace dump operation is performed. The trace operation also stops when DCB word 2 is set to 0 or when any interrupt status byte except A0 or 80 is presented.

Trace Dump: The DCB format for this operation follows:

DCB (device control block)

Word	
0	Control word—2X00
1	Not used
2	Not used
3	Not used
4	Not used
5	Chain address—must be even
6	Byte count—must be 64 (hex 0040)
7	Data address—must be even

This operation begins if DCB word 0 equals 2X00 and the byte count is 64. Data for error analysis is dumped from an array in storage to the data address specified in DCB word 7 and is made available to the operator through an output device.

This data is the following information about the last seven DCBs issued to a single address:

- The DCB control words
- The DCB addresses
- The interrupt status byte and interrupt condition codes
- The status word 1 information

This data also includes status words 0 and 2 for the last DCB if the trace operation stops due to an error detected.

Note: The field containing the interrupt status byte and interrupt condition codes for the last DCB is followed by FFFF; the field containing status word 1 for the last DCB is followed by FFFF.

The field containing the interrupt status byte and interrupt condition code for the last DCB is followed by 0000; the field containing status word 1 for the last DCB is followed by 0000.

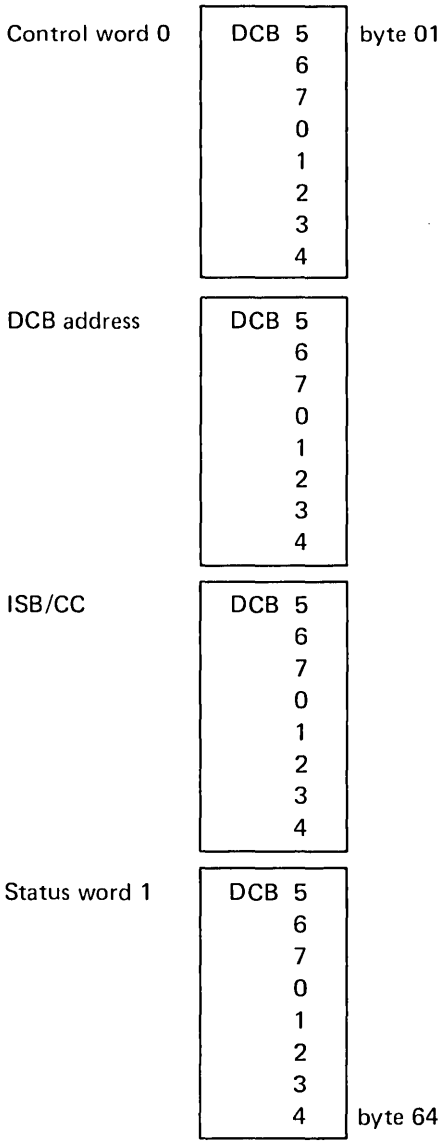
The interrupt status byte and interrupt condition codes are presented in the following format:

Interrupt status byte	Reset indicator	Condition code

The condition codes and their meanings follow:

Condition code	**Meaning**
00	No interrupt returned
02	Exception interrupt returned
03	Device end interrupt returned
F0	Operation ended by reset
F2	Exception interrupt returned followed by reset
F3	Device end interrupt returned followed by reset

The trace dump storage array appears in storage as follows:



Trace dump storage array

The trace dump printout is as follows:

	DCB5	*DCB6*	*DCB7*	*DCB0*	*DCB1*	*DCB2*	*DCB3*	*DCB4*
Control word 0			2004	SW0				
DCB address			XXXX	SW2				
ISB/CC			8002	FFFF				
Status word 1			8000	FFFF				

DCBs without errors — Failing DCB — DCBs without errors

- SW0 – Status word 0 for failing DCB
- SW2 – Status word 2 for failing DCB
- FFFF – Indicates that trace has stopped on preset error condition (**Note:** 0000 indicates that trace is still running)

Set Expanded Mode: To enable and disable the expanded operating mode the Start Control command is used.

The IDCB has the following format:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
7C	XX

Immediate data field
DCB address
16 ... 31

DCB Format

```
Word      0    0 0 0 1
          1    Not used
          2    Not used
          3    X field Y field
          4    Not used
          5    Not used
          6    Must be zero
          7    Not used

X-field   =    Delineating Character used in Two Character Change of
               Direction Mode.  Bit 10 of the Y field must be on to
               activate the mode.

Y-field   =    Bit 08 = priority DCB fetch
               Bit 09 = two-character LRC mode
               Bit 10 = two-character COD mode
               Bit 11 = inhibit zero insert mode
               Bit 12 = 4 CODs with LRC mode
               Bit 13 = continuous echoplex mode
               Bit 14 = attention interrupt mode
               Bit 15 = continuous receive mode
```

Note: See "Operations" for a description of the modes listed in the Y field.

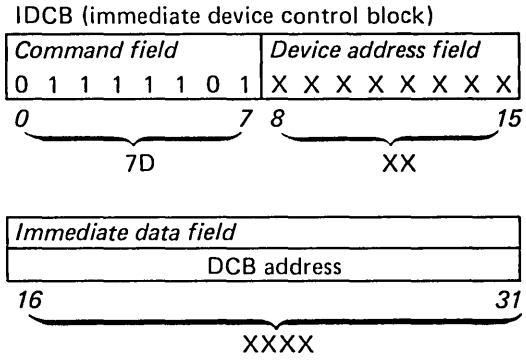
These modes are stored in a bit significant manner; a 0 disables the mode and a 1 enables the mode.

These extensions are applicable on a per line basis within the Feature-Programmable Multiline adapter. The various adapter modes of operation can be used together. However, certain combinations of modes such as continuous echoplex without continuous receive or attention interrupt without continuous receive are illogical.

(Device Reset, System Reset, Halt I/O resets the expanded mode of operation.)

Start Diagnostic 1

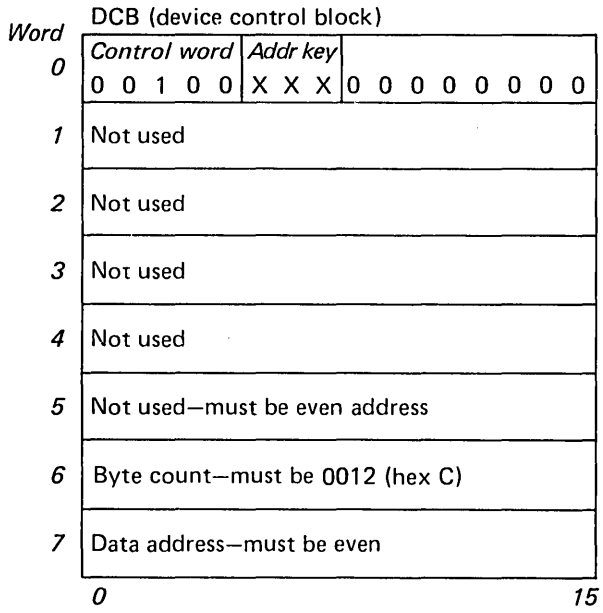
The format of the IDCB for this command follows:



When a Start Diagnostic 1 command is issued to the attachment, the following sequence of operations takes place:

1. The DCB is fetched.
2. A test of the attachment registers is processed. When one or more registers identifies an error, the attachment enters a wait state and no interrupt request is presented.
3. A read only storage check sum is calculated and the results are stored at the data address specified in the DCB.

Note: When the attachment recognizes Start Diagnostic 1, it dedicates itself to processing that command and no operations should be pending at other addresses controlled by this attachment.



Descriptions of the Start Diagnostic 1 DCB words follow:

Word 0

Bits 0-1: Must be set to 0.

Bit 2: Must be set to 1.

Bits 3-4: Must be set to 0.

Bits 5-7: Storage protect key.

Bits 8-15: Set to 0 to preclude future code obsolescence.

Words 1-5

Not used.

Word 6 - Byte Count

This word must contain a count of 12 (hexadecimal C). Otherwise, the attachment ends the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte is set to 1.

Word 7 - Data Address

This word must contain an even address. Otherwise, the attachment ends the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte is set to 1.

This word specifies the starting address for the attachment to cycle-steal the following words into storage:

- Word 1 - Stored checksum of read only storage 1
- Word 2 - Calculated checksum of read only storage 1 (inverted)
- Word 3 - Stored checksum of read only storage 2
- Word 4 - Calculated checksum of read only storage 2 (inverted)
- Word 5 - Stored checksum of read only storage 3
- Word 6 - Calculated checksum of read only storage 3 (inverted)

Start Diagnostic 2

The Start Diagnostic 2 command can be issued to any device without disturbing the normal function of other devices.

The IDCB for this command is shown below:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 1 0	X X X X X X X X
0 7	*8* *15*
7E	00–7F

Immediate data field
DCB address
16 *31*
XXXX

When a Start Diagnostic 2 command is issued to the attachment, various operations as defined in the DCB are processed. These operations are ended with a device end interrupt request after the attachment cycle-steals the Start Diagnostic 2 words into storage. The operations and words are described below.

This command provides both external and internal wrap capability. The external wrap requires an external wrap connector; the internal wrap does not affect the transmit or receive lines.

Note: Before a Start Diagnostic 2 command can be issued, a Set Mode or Set Control command must be issued; otherwise, results are be unpredictable. If external clocking is available, it may be used with this command. Internal clocks not exceeding 300 bps may be used for diagnostic purposes in synchronous mode. DTR and RTS are reset following the completion of this command (if not jumpered on).

DCB (device control block)

Word		
0	*Control word* 0 0 1 0 0	*Addr key* X X X	0 0 0 0 0 0 0 0
1	Not used	
2	Not used	
3	Not used	
4	Not used	
5	Not used—must be even address	
6	Byte count—must be 0006	
7	Data address—must be even	
	0	*15*

DCB Word 0 - Control

The bit descriptions for this word are given below.

Bits 0-1: Must be set to 0.

Bit 2: Must be set to 1.

Bits 3-4: Must be set to 0.

Bits 5-7 - Cycle-Steal Address Key: Storage protect key.

Bit 8: If the data terminal ready (DTR) jumper is not installed and this bit is set to 1, DTR is deactivated for the length of the command.

Bit 9: If the request to send (RTS) jumper is not installed and this bit is set to 1, the RTS is deactivated for the length of the command.

Bit 10: The adapter activates echoplex when this bit is set to 1. The echoplex latch is reset after Start Diagnostic 2 is processed.

Bit 11: Not used and must be set to 0.

Bit 12: The attachment places a space condition on the transmit line when this bit is set to 1. If odd parity is selected, bit 12 (parity error) of diagnostic word 1 is set to 1. If asynchronous mode is selected, bit 9 (break detect) and bit 10 (framing error) of the returned diagnostic data word equal 1. Diagnostic data word 0 is 0000 for 5-, 6-, 7-, and 8-bit character lengths.

Bit 13: Not used and must equal 0.

Bit 14: An internal wrap test is performed when this bit is set to 1. The transmit data line to the modem remains at a mark level and no data is transmitted off the card. The receive data line is not examined and does not affect the test.

Bit 15: Not used and must equal 0.

DCB Words 1-5

Not used.

DCB Word 6 - Byte Count

This word must contain a count of 6. Otherwise, the attachment ends the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte is set to 1.

DCB Word 7 - Data Address

This word must contain an even address. Otherwise, the attachment ends the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte is set to 1.

This word specifies the starting address for the attachment to cycle steal the diagnostic data words into storage.

Diagnostic Data Words

The diagnostic data words are used in conjunction with the maintenance package.

Word 0

This word is defined by the character length of the selected transmission code as shown in the chart that follows.

Character length (bits)	*Word 0 description* *Start Diagnostic 2 DCB word 0, bit 12, equals 0*	*Word 0 description* *Start Diagnostic 2 DCB word 0, bit 12, equals 1*
5	150A	0000
6	152A	0000
7	552A	0000
8	55AA	0000

Word 1

The bit descriptions are:

Bit 0 - Data Terminal Ready: Set to 1 if DTR jumper is installed or if bit 8 of the DCB control word 0 is set to 0. DTR is reset following the command execution.

Bit 1 - Data Set Ready: Set as follows:

- Set to 1 if external wrap connector is used.
- Set to 1 if a leased line modem is used and powered on.
- Set to 1 if the IBM Current Interface Cable is installed and the current interface is wired.
- Set to 0 or 1 if a switched line modem is used.
- Set to 0 if no cable is installed.
- Set to 0 if bit 8 of DCB control word 0 is set to 1.

Bit 2 - Request To Send: Set to 1 if the request to send (RTS) jumper is installed or if bit 9 of DCB control word 0 is set to 0.

Bit 3 - Clear To Send: Set to 0 or 1 for the same conditions as bit 1 (data set ready), as described previously.

Bit 4 - External Clocks: Set to 1 if the bit rate constant in the DCB for the Set Control or Set Mode command is set to 00.

Bit 5 - Carrier Detect: Set to 1 if the carrier detect jumper is installed or the external wrap connector is used and control word 0 bit 9 is set to 0. This bit is set to 0 or 1 if connected to a modem.

Bit 6 - Echoplex: Set to 1 if bit 10 of control word 0 is set to 1.

Bit 7 - Receive Data Lead: Can be set to 0 or 1.

Bit 8 - Ring: Set to 0.

Bit 9 - Sync/Break Detect: Set to 1 for all operations in synchronous mode and those in which bit 12 of DCB control word 0 is set to 1 in asynchronous mode.

Bit 10 - Framing Error: Set to 1 if bit 12 of DCB control word 0 is set to 1 in asynchronous mode.

Bit 11 - Overrun: Set to 0.

Bit 12 - Parity Error: Set to 1 if bit 12 of DCB control word 0 is set to 1 and odd parity is specified in set mode.

Bit 13 - Transmit Empty: Set to 1.

Bit 14 - Receive Ready: Set to 1.

Bit 15 - Transmit Ready: Set to 1.

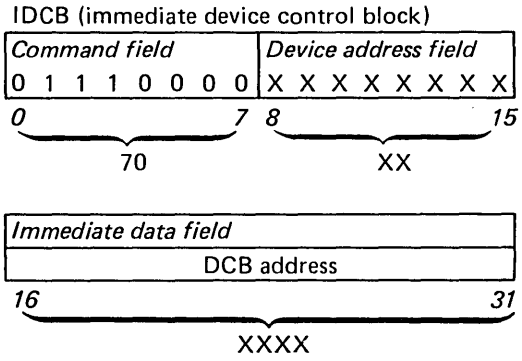
Word 2

This word is used to test the attachment's ability to cycle steal bytes of data into storage. Bits 0-7 are the bit rate constant and the only data byte to be placed in storage. If this byte transfer fails, hex FF is placed in bits 8 through 15; if the transfer is successful, bits 8 through 15 are unchanged.

Note: Before executing a Start Diagnostic 2 command, bits 8 through 15 of word 2 in storage should be equal too a value other than hex FF so that the program can determine if the byte transfer failed. After Start Diagnostic 2 is completed, DTR is reset unless it is set to 1.

Start

The Start command begins a cycle-steal operation in the addressed device. The format of the IDCB for the Start command follows:



The DCB is an eight-word area in storage that describes the specific parameters of the cycle-steal operation. Its storage address is assigned by the program and must be even. When this address is transferred to the attachment, it points to word 0. If the DCB address is odd, the attachment sets interrupt status byte bit 1 (delayed command reject) to 1 and ends the operation with an exception interrupt request. The general format for a DCB Start command follows.

DCB (device control block)

Word	
0	Control word
1	Not used
2	Timer 1
3	Timer 2
4	Not used
5	Chain address—must be even
6	Byte count
7	Data address

The formats for the individual start commands (Start, Start Cycle-Steal Status, Start Diagnostic, and Start Control) are described under "Commands," earlier in this chapter.

The general format for a DCB specifying asynchronous set mode or set control operation follows:

DCB (device control block)

Word		
0	Control word	
1	Bit-rate constant	Line-control character
2	Line-control character	Line-control character
3	Line-control character	Line-control character
4	Line-control character	Line-control character
5	Chain address	
6	Byte count	
7	Data address	

0 *7* *8* *15*

The general format for a DCB specifying synchronous set mode operation (synchronous mode only) follows:

DCB (device control block)

Word		
0	Control word	
1	00	Line-control character
2	Line-control character	Line-control character
3	Line-control character	Line-control character
4	Line control character	Line-control character
5	Chain address	
6	Quantity of synchronization characters	
7	Address of synchronization characters	
	0 7 8 15	

A description of the eight DCB words follows.

DCB Word 0 - Control

This 16-bit word prescribes the operation to be performed.

Bit 0 - Chaining Flag: If this bit is set to 1, the attachment fetches the next DCB in the chain after completing the current DCB operation if there are no exception interrupt conditions.

Bit 1 - Program Controlled Interrupt (PCI) Request: If this bit is set to 1, the attachment presents a PCI request at the completion of the DCB fetch and places DCB word 3 bits 8 through 15 in the interrupt information byte. Data transfers associated with the DCB can begin if the PCI request is pending. If the PCI request is pending when the attachment encounters the next interrupt causing condition, the device discards the PCI condition replaced with the new interrupt condition. This bit is recognized only during transmit and receive operations. If it is set to 1 in any other type of operation, bit 3 of the interrupt status byte (DCB specification check) is set to 1 and the operation ends with an exception interrupt request.

Bit 2 - Input Flag: Indicates to the attachment the direction of data transfer. It is set to 1 when data is transferred from the attachment to the processor; it sets 0 when data is transferred from the processor to the attachment.

Bits 3-4: Not used and must be set to 0; otherwise, bit 3 of the interrupt status byte (DCB specification bit) is set equal to 1 and the operation ends with an exception interrupt request.

Bits 5-7 - Cycle-Steal Address Key: This key is presented by the attachment during data transfers. It is used to ascertain storage access authorization.

Bits 8-15 - Operation Modifier: When bit 8 is set to 1, the operation specified in bits 9 through 15 of the DCB control word is performed in set mode. The attachment decodes bits 9 through 15 to determine which of the following operations should be performed.

Bits								Operation
8	9	10	11	12	13	14	15	
0	0	0	0	0	0	0	0	Transmit
0	0	0	0	0	0	0	1	Transmit end
0	0	0	1	0	0	0	1	Transmit end with prereceive
0	0	0	0	0	0	1	0	Transmit allow break
0	0	0	0	0	0	1	1	Transmit end allow break
0	0	0	1	0	0	1	1	Transmit end allow break with prereceive
0	0	0	0	0	1	0	0	Receive
0	0	0	0	0	1	0	1	Receive with time-out
0	0	0	1	0	1	0	0	Receive with block check character
0	0	0	1	0	1	0	1	Receive with time-out and block check character
0	0	1	0	0	1	0	0	Receive with echoplex
0	0	1	0	0	1	0	1	Receive time-out and echoplex
0	0	1	1	0	1	0	0	Receive with echoplex and block check character
0	0	1	1	0	1	0	1	Receive with echoplex, time-out, and block check charac
0	1	0	0	0	1	0	0	Receive transparent
0	1	0	0	0	1	0	1	Receive transparent with time-out
0	1	1	0	0	1	0	0	Receive transparent with echoplex
0	1	1	0	0	1	0	1	Receive transparent with echoplex and time-out
0	1	1	1	0	1	0	0	Read adapter buffer
0	0	0	0	0	1	1	0	Ring monitor
0	0	0	0	0	1	1	1	Ring monitor with time-out
0	0	0	0	1	0	0	0	DTR enable
0	0	0	0	1	0	0	1	DTR enable with time-out
0	0	0	0	1	0	1	0	DTR enable with answer tone
0	0	0	0	1	0	1	1	DTR enable with time-out and answer tone
0	0	0	0	1	1	0	0	DTR disable
0	0	0	1	1	1	0	1	Set control
0	0	0	0	1	1	1	0	Program delay
0	0	0	0	1	1	1	1	Reset
0	0	0	0	1	1	0	1	DCB specification check
1	X	X	X	X	X	X	X	Set mode

Data Transmission

Transmit

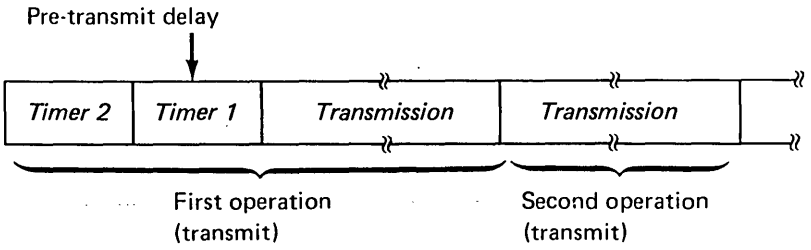
The transmit operation is used when another transmit type operation follows immediately.

The attachment begins this operation by sending request-to-send (RTS) to the modem and starting timer 2. The attachment then waits for clear-to-send (CTS) from the modem. When the attachment receives CTS, it resets timer 2, starts timer 1, and waits for timer 1 to time out. When timer 1 times out, the attachment begins cycle-stealing data from storage and transmitting the data to the remote station. The delay provided by timer 1, in this case, is called pretransmit delay; its purpose is to allow the receiving station enough time to set up to receive data and to allow time for the modem and communication lines to stabilize.

Timer 2 should be set to a value high enough to allow turnaround on a half-duplex teleprocessing link. If timer 2 is not correctly defined by the program, an exception interrupt request (CC2) occurs. If the interrupt status byte bit 0 is set to 1, status word 1 of the attachment has a modem interface error (bit 9 set to 1) indicating that RTS was active and that CTS was not returned by the modem within the time limits of timer 2.

The attachment presents a device end interrupt request or begins a DCB command chaining operation when the byte count goes to 0. The attachment stays in transmit mode and leaves RTS active at the end of this operation. This allows continuity from one transmit type operation to another without sending another RTS and waiting for CTS.

When chaining a series of transmit type operations, timer 2 is used only in the first operation; timer 1 provides a pretransmit delay in the first operation only.

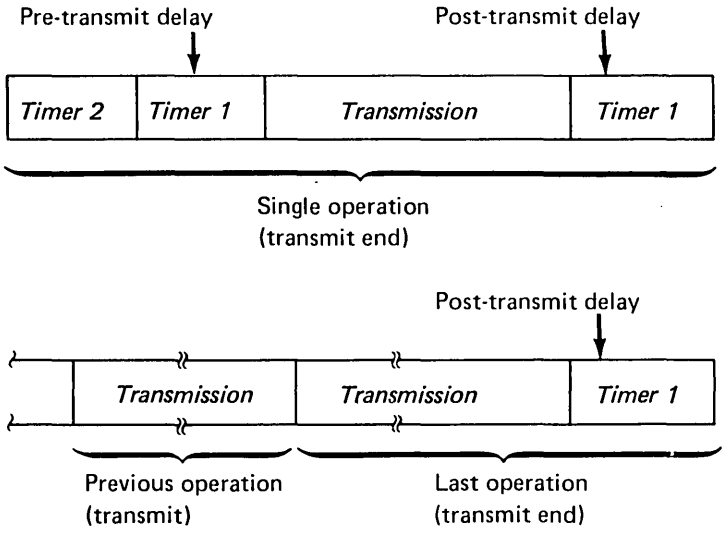


Timer 1 should be set for a pretransmit delay of approximately 9 milliseconds when the receiving station is a program controlled device and is directly connected or is connected through a duplex modem. Timers 1 and 2 should always be activated to prevent excessive turnaround and noise.

Note: Line control characters are not examined. In synchronous operation, leading pad characters and synchronization characters are not inserted by the attachment except in two situations. When data is not placed into the data stream as quickly as the attachment expects it, the attachment may insert synchronization characters into the data stream as follows:

- Between characters within a block of data
- Between blocks of data within the data stream when the blocks result from chained transmit operations

Transmit End: This operation is used to transmit the last block of data in a chain of transmit type operations or when only one block is being transmitted. An example of the use of this operation is shown below.



This operation is the same as the transmit operation, except that the attachment exits transmit mode and starts timer 1 after the last character is sent to the modem. When timer 1 times out, the attachment resets its RTS (if RTS is **not** set to 1). This delay allows the last character to leave the modem before the attachment resets request to send. The timer 1 delay at the end of this operation is called posttransmit delay. Note that timer 1 is used twice in this operation (pretransmit and posttransmit delays) if this operation is not part of two or more transmit type operations.

Transmit End With Pre-receive: This operation is the same as the transmit end operation, except that there is no posttransmit delay and, when prereceive time starts, incoming data is saved during the chaining process. Pre-receive time starts after the last character has been transmitted and a posttransmit delay is not used. Data can be received immediately; however, this operation must be chained to a receive type command or an exception interrupt will occur. Interrupt status byte bit 3 (DCB specification check) is set to 1. To ensure data integrity during line turnaround, a direct connection or a four-wire interface must be used.

Transmit Allow Break: This operation is the same as the transmit operation, except that it allows the receiving station to stop the transmission. To do this, the receiving station breaks the line by driving its transmit line to a space condition for at least 150 milliseconds plus two character times. If the attachment detects this condition, it presents an exception interrupt request with bit 0 of the interrupt status byte set to 1 and transmit mode is reset. Status word 1 bit 6 sets 1 to indicate the break.

Transmit End Allow Break: This operation is the same as the transmit end operation, except that this operation allows the receiving station to stop the transmission. To do this, the receiving station breaks the line for at least 150 milliseconds plus two character times. If the attachment detects this condition, it resets transmit mode and RTS and presents an exception interrupt request with bit 0 of the interrupt status byte set to 1. The attachment does not reset RTS if the jumper is installed.

Transmit End Allow Break With Pre-receive: This operation is the same as the transmit end with prereceive operation and transmit end allow break operation combined. The same restrictions stated under "Transmit End With Pre-receive" apply to this command.

Data Reception

Normal receive mode (selected by using the set control or set mode operations) provides the following:

- ACCA compatibility
- Half duplex operation
- 7 COD characters, 1 block check character, and 2 of the CODs can be conditioned by command to receive a single block check character
- Command driven reception, with echoplex capabilities

In the normal receive mode, the attachment receives data **only** when a DCB receive or DCB transmit with prereceive operation is being processed. When no receive DCB or transmit DCB is being processed, the attachment assumes that no data is present to be received. This assumption is correct when dealing with a half-duplex device. When a device operates in duplex mode, data can be present almost anytime.

Expanded Mode

To expand the attachment capabilities, additional operations are defined using the Set Expand Mode command. (See "Set Expanded Mode" in the commands section of this chapter.)

Expanded mode provides the following operations:

- Continuous receive mode
- Attention interrupt mode
- Continuous echoplex mode
- Extended character recognition/ detection consisting of the following:
  - — Two character COD
  - — Inhibit zero insert mode
  - — Two character block check mode
  - — 4 CODs with LRC mode

Continuous Receive Mode: In the normal receive mode, the adapter receives data **only** when a DCB Receive or DCB transmit with prereceive command is being processed by the adapter. When no receive DCB is in process or a transmit DCB is being processed, the attachment assumes that no data is present to be received. This assumption is correct when dealing with a half-duplex device. When a device operates in duplex mode, however, data can be present at almost anytime due to operator action or device operation. To handle this situation, a new mode (continuous receive mode) of operation has been defined. DTR, DSR, and DCD must be active before entering this mode of operation.

1. If a receive DCB is in process, the character is be handled in normal fashion; that is, it is compared with the COD character table and the receive either continued or ended based on normal operation.
2. If no DCB is active or a nonreceive DCB is active, the adapter stores the character within the adapter's 15-byte buffer (one character per byte) and awaits the processing of the next DCB receive. The adapter continues to buffer these characters on a first-in first-out (FIFO) basis. When the next

receive DCB is processed by the adapter, the buffer contents are processed as part of the operation just as if the buffer data was being received from the line. It will be transparent to the program whether the data from the receive came from the buffer or the actual line. If the adapter receives more characters than it can hold in the line buffer, the next DCB ends with a unique error condition of FIFO full (status word 1, bit 12).

Note that the COD processing is simply an alert condition for lines operating in asynchronous mode (TTY); that is, the reception of the COD character does not necessarily mean a true end of message condition, but could simply be a special character within a message. In synchronous mode operations, after a COD has been received, the attachment resets synchronization and begins the resynchronization process again. Set Mode Set Control, or DCB Reset commands clear the adapter of any stored input data.

Attention Interrupt Mode: Attention interrupt mode is an operating mode used only in conjunction with continuous receive mode. When activated in the adapter, attention interrupt mode causes received characters to be processed by the adapter concurrent with other adapter operations. In this mode, when a character is received and a DCB is not in process, it is presented to the Series/1 using an attention interrupt with the received character in the IIB (interrupt information byte). The following special situations are dependent on the Attention Interrupt Mode: Attention interrupts are presented only if a Transmit Type command or no command is active. DTR and DSR must be active. The ATTN interrupt is not associated with any active command.

1. If a transmit allow break command is active and a character is received which is in the COD table, the adapter ends the Transmit Allow Break command (after processing the current transmit character) and presents interrupt status with the residual address of the last character transmitted available to the system. If a COD character is received before the transmit allow break command and is interrupt pending in the channel, the transmit command is not stopped.
2. If an error occurs, an attention with exception (CC=6) is presented with an ISB equal to 80, and no further attention interrupts are presented until a read adapter buffer operation followed by a read cycle-steal status is processed by the adapter. Attention interrupts resume if the FIFO buffer is empty (bit 15 of status word 1) following a Start Cycle-Steal Status command. If a transmit type command is ended by the error, a Start Cycle-Steal Status command should be issued, then a Read Adapter Buffer command followed by another Start Cycle-Steal Status command. The first Start Cycle-Steal Status command is used to obtain the residual address of the transmitted data. The read Adapter buffer operation is used to clear out all previously held data and the second Start Cycle-Steal Status command reenables attention interrupts. If the adapters buffer is not empty, and bit 15 of status word 1 is set to 1, another read adapter buffer operation is required followed by a Start Cycle-Steal Status command.

Continous Echoplex Mode: Continuous echoplex provides the capability to use the echoplex function with continuous receive in a half-duplex operation between the adapter and the Series/1. During read with echoplex operation, characters received from the terminal are automatically transmitted back to the terminal for display. When continuous receive mode is in operation and continuous echoplex is specified, any characters received without a pending read operation are saved and echoed to the terminal. During a transmit operation any characters received are **not** held in the line buffer and **not** echoed to the terminal. Continuous echoplex is

intended for situations where the device requires echoplex but no CPU logic is needed to process the data characters for echo.

Expanded Character Recognition/Detection

Two-Character COD Mode: Two-character COD causes the adapter to interpret the COD table in conjunction with a delineating character to determine an ending sequence. The user-specified delineating character is the first character received and the second character will be any of the seven programmable characters in the COD table. If two delineating characters are received consecutively followed by a character in the COD table, reception continues until a single delineating character followed by a COD is detected. Typically, the delineating character would be a DLE or ESC character.

Inhibit Zero Insert Mode: Inhibit zero insert mode, when enabled, causes the attachment to place a received character with incorrect parity into storage as it was received. If inhibit zero insert mode is not enabled, the attachment places 0's into storage when characters are received with incorrect parity.

Two Character Block Check Mode: Two character block check causes the adapter to process the Read with block check command such that two block check (LRC) characters following a COD are placed into the user's buffer within Series/1 storage. Similar to the conventional mode of LRC reception (single character), no check is made of the data received as a block check.

Four CODs with LRC Mode: 4 CODs with LRC causes the adapter to receive one additional character following COD recognition utilizing four specifiable COD characters. When a Receive with Block Check command is issued and COD 4, 5, 6, or 7 is received and interpreted from the COD table, one additional character is placed in Series/1 storage following the COD character.

DCB Priority Fetch Mode: Causes the DCB Scan function in the microcode to fetch the entire DCB for the address with the priority bit set before checking for activity on other addresses. Provides faster response for high priority address. Overall response is degraded as more priority bits are set.

Normal Receive

This operation allows the attachment to begin cycle-stealing data into storage when the attachment begins receiving valid data (the correct start bit or synchronization characters must be recognized). If the carrier detect jumper is not installed, carrier detect from the modem must be active before the attachment can begin transferring data to storage. When any of the defined characters are received, the attachment presents an interrupt request, as shown in the chart:

Receive termination chart

Input conditions				Receive termination		
Error condition*	Chain flag	Byte count = 0	COD received	CC	ISB/IIB	Comment
No	No	No	Yes	2	A0	
No	No	Yes	No	2	20	
No	No	Yes	Yes	3	00	
No	Yes	No	Yes	2	A0	No chain
No	Yes	Yes	No	–	–	Chain to next DCB
No	Yes	Yes	Yes	–	–	Chain to next DCB
Yes	No	No	Yes	2	A0	
Yes	No	Yes	No	2	A0	
Yes	No	Yes	Yes	2	80	
Yes	Yes	No	Yes	2	A0	No chain
Yes	Yes	Yes	No	2	A0	No chain
Yes	Yes	Yes	Yes	2	80	No chain

*Parity error exception interrupt occurs at the completion of the operation for the present DCB. All other exception interrupts are presented upon detection.

If the attachment detects a parity error while receiving data, it places hex 00 into storage instead of the incorrect character and continues receiving data until the ending condition occurs (COD received). The attachment then presents an exception interrupt request. If the indicator panel is connected to the attachment and the DISPLAY/FUNCTION SELECT switches are set to 11110, the attachment places the incorrect character into storage and continues receiving data.

A device end interrupt request is presented when a COD character is recognized. After character synchronization is established, all characters, including any synchronization characters, are placed into storage.

When the attachment recognizes a receive operation, a timer is not used, and the carrier detect jumper is not installed, the attachment waits for an indefinite length of time for carrier detect to become active before beginning the receive operation.

When the attachment recognizes a receive operation, a timer is used, and the carrier detect jumper is not installed, the attachment waits for the length of time specified in timer 1 for carrier detect to become active before beginning the receive operation. If carrier detect does not become active within the specified time, the attachment ends the operation with an exception interrupt request and word 1 bit 9 (modem interface error) in the start cycle-steal status operation's DCB is set to 1.

When the carrier detect jumper is installed, a carrier detect signal is returned to the attachment and the signal from the modem is not checked.

When DCB word 0 bit 0 (chaining flag) is set to 0, the byte count reaches 0, and no COD is received:

- An exception interrupt request is presented
- Interrupt status byte bit 2 (incorrect length record) is set to 1

Receive With Time-Out: This operation is the same as the receive operation, except that the attachment uses timer 1 to limit the time it will wait for the first character. It also limits the time that the attachment waits between characters. Failure to

receive a character within this time results in an exception interrupt request with interrupt status byte bit 0 set to to 1 and status word 1 bit 1 (time-out) set to 1. If the carrier detect jumper is not installed, the attachment waits the length of time specified by timer 1 for carrier detect to become active. If carrier detect does not become active within the specified time, the attachment presents an exception interrupt request and posts modem interface error (bit 9) in cycle-steal status word 1.

Receive With Block Check Character: This operation is the same as the receive operation except that the attachment waits for one character after detecting either the COD6 or COD7 character specified in the DCB format of a Set Control or Set Mode command. The block check character is not checked by the adapter but is placed in storage. Parity, if set, is checked on the block check character.

Receive With Time-Out and Block Check Character: This operation is the same as the receive with block check character operation except that timer 1 is used to limit the time the attachment waits for carrier detect to become active, to receive the first character, or between characters. If the attachment does not receive a character or a block check character after a COD6 or COD7 character, an exception interrupt request is presented with interrupt status byte bit 0 set to to 1.

Receive With Echoplex: This operation is the same as the receive operation except that all data transmitted from the sending station is returned to the sending station on the sending station's receive line. A duplex interface is required.

Receive With Time-Out and Echoplex: This operation is the same as the receive with echoplex operation except that timer 1 is used to limit the time that the attachment waits to receive a character, the time between characters, and the time waiting for carrier detect to become active. If the attachment does not receive a character or carrier detect within the specified time, an exception interrupt request is presented with interrupt status byte bit 0 set to 1.

Receive With Block Check Character and Echoplex: This operation is the same as the receive with block check character operation except that data is immediately transmitted back to the sending station.

Receive With Echoplex, Time-Out, and Block Check Character: This operation is the same as the receive with time out and block check character operation except that data is immediately transmitted back to the sending station.

Receive Transparent: This operation is the same as receive, except that the COD characters are not recognized and this operation ends when the byte count reaches 0, with an interrupt CC3 or when it processes a chain.

Receive Transparent With Time-Out: This operation is the same as the receive transparent operation except that timer 1 limits one of the following:

- The time that the attachment waits for carrier detect to become active or to receive a character
- The time between characters when more than one character is being received

Receive Transparent With Echoplex: This operation is the same as the receive transparent operation except that all data transmitted from the sending station returns to the sending station on the sending station's receive line.

Receive Transparent With Echoplex and Time-Out: This operation is the same as the receive transparent with echoplex operation except that timer 1 limits one of the following:

- The time that the attachment waits for carrier detect to become active or to receive a character
- The time between characters when more than one character is being received

Notes:

1. When carrier detect jumper is not installed and the attachment recognizes any receive operation without timer, the attachment, before going into receive mode, waits for an indefinite period of time for carrier detect signal from the modem to become active.
2. When carrier detect jumper is not installed and the attachment recognizes any receive with time-out command, before going into receive mode, the attachment waits for the carrier detect signal from the modem to become active within the period of time specified in timer 1 (DCB word 2). If at the end of timer 1 value, the carrier detect signal from the modem has not become active, then the attachment ends the operation with an exception interrupt and modem interface error bit (bit 9) set in cycle-steal status word two.
3. When the carrier detect jumper is installed, carrier detect is permanently returned to the attachment and the signal from the modem is not checked.

Read Adapter Buffer: This operation is used with the expanded mode commands. When processed, any data saved in the adapter buffer is cycle stolen into Series/1 storage. This command must be issued if an interrupt CC6 is presented or if bit 15 of word 1 of the Start Cycle-Steal Status command is active. The first byte placed into storage represents a byte count of the characters received error free but not reported by way of CC4. Following the byte count are the receive characters. Up to 16 (hexadecimal 10) bytes may be placed into storage.

Line Control

Ring Monitor: This operation allows the attachment to monitor the ring indicator line from the modem. Unless this is a chained operation, the attachment presents a device end interrupt request to the processor when ring indicator is active for more than 100 milliseconds.

Ring Monitor With Time-Out: This operation is the same as the ring monitor operation except that timer 2 limits the length of time that the attachment waits for a ring condition. If a time-out occurs, an exception interrupt request is presented, interrupt status byte bit 0 is set to 1, and bit 1 (time-out) is set in cycle-steal status word 1.

DTR Enable: This operation sends DTR to the modem; the modem responds by activating DSR. Unless this is a chained operation, the attachment presents an interrupt request to the processor when DSR becomes active.

To ensure the validity of DSR, the minimum processing time of this operation is 100 milliseconds.

Note: DTR is normally set to 1 for leased lines.

DTR Enable With Time-Out: This operation is the same as the DTR enable operation except that timer 2 limits the length of time the attachment waits for DSR. If a time-out occurs before the DSR becomes active DTR is disabled, an exception interrupt request is presented to the processor, the interrupt status byte bit 0 is set to 1, and bit 9 (modem interface error) is set in cycle-steal status word 1. To ensure the validity of DSR, the minimum processing time of this operation is 100 milliseconds.

DTR Enable With Answer Tone: This operation is the same as the DTR enable operation except that an answer tone or space is placed on the transmission line for the period specified in timer 1 when data set ready is activated. After the time-out occurs, an interrupt request is presented to the processor or chaining begins. To ensure the validity of DSR, the minimum execution time of this operation is 100 milliseconds. Timer 1 should be set to approximately 3 seconds (refer to the modem manual for an exact setting).

DTR Enable With Answer tone and Time-Out: This operation is the same as the DTR enable with answer tone operation except that timer 2 limits the length of time the attachment waits for DSR. If a time-out occurs before the DSR becomes active, DTR is disabled, an exception interrupt request is presented to the processor, interrupt status byte bit 0 is set to 1, and status word 1, bit 9 (modem interface error) is set in cycle steal status word 1. To ensure the validity of DSR, the minimum execution time of this operation is 100 milliseconds.

DTR Disable: This operation is used in a switched network to deactivate DTR and disconnect the attachment from the network. Timer 2, which should be set for at least 5 seconds, starts when DTR is deactivated. Unless this is a chained operation, the attachment presents a device and interrupt request to the processor when a time-out occurs. If DTR or DSR is not deactivated within the time specified by timer 2, an exception interrupt is presented to the processor, interrupt status byte bit 0 is set to 1 and cycle-steal status word 1 bit 9 is set to 1. DTR cannot be deactivated if the jumper is installed.

Set Control: This operation provides compatibility with the Asynchronous Communications (ACC) features, and it places the attachment in asynchronous mode and COD characters are defined in the DCB for a Set Control command. The data length is eight bits, there is no parity specified, and there are two stop bits. The above conditions are effective until a new set control or set mode is activated, or a power-on reset occurs.

Note: The attachment's mode of operation is designated by either set control or set mode operation.

Program Delay: This operation starts timer 2. Unless this is a chained operation, the attachment presents a device end interrupt request to the processor when a time-out occurs.

Reset: This operation resets all information in an addressed device except Prepare command information, DTR, set control information, or set mode information. Unless this is a chained operation, a device end interrupt request is presented to the processor when all of the designated information is reset.

Set Mode: This operation places the attachment in either asynchronous or synchronous operation. The format of bits 8 through 15 for both modes are shown here:

Bit	*Value*	*Meaning*	
8	1	Set mode	
9	0	Asynchronous operation	
	1	Synchronous operation	
10,11	00	5 bits per character	
	01	6 bits per character	
	10	7 bits per character	
	11	8 bits per character	
		Asynchronous	**Synchronous**
12,13	00	Invalid	SYN-SYN is recognized/generated
	01	One stop bit	Invalid
	10	Reserved	SYN is recognized/generated
	11	Two stop bits	Invalid
14	0	Odd parity	
	1	Even parity	
15	0	Parity disabled	
	1	Parity enabled	

Note: Any invalid configuration causes an exception interrupt request with ISB bit 3 (DCB specification check) equal to 1.

In asynchronous mode, external clocks must be provided when DCB word 1 bits 0 through 7 (bit rate constant) equal 00.

In synchronous mode, external clocks must be provided and DCB word 1 bits 0 through 7 (bit rate constant) must equal 00. The number of synchronization characters specified by bits 12 and 13 must equal the byte count in the DCB of a set mode (synchronous) operation and must reside at an even byte boundary; otherwise, a DCB specified check is presented to the processor. The location of the synchronization characters must be specified by DCB word 7 (data address). If two synchronization characters are used, they can be different characters.

Bit Rate

Any line on the adapter can be programmed for data transmission at a rate between 37.5 and 19,200 bps. (See limitations below.) If the rate is between 37.5 and 1200 bps, install the low range jumper; if the rate is between 300 and 19,200 bps, install the high range jumper. Specify the exact bit rate (bit rate constant) in the program. The constant is the high order byte of DCB word 1 and is stored in the attachment during a set control/set mode operation.

The programmable eight-line controller is limited to the following:

- A maximum aggregate throughput rate of 64,000 bps (at 12 bits per character), 56,000 if doing a trace operation
- A maximum of one four-line adapter if the bit rate of 19,200 bps is selected for any line synchronous operation
- When continuous receive mode is selected with buffered duplex devices, the bit rate used to determine controller loading should be twice the stated bit rate of the line.

Example: Determine the bit-rate constant for 150 bps.

$$\text{Constant} = \frac{9600}{\text{bps}} - 1$$

Round off to the nearest whole number and convert to hexadecimal

$$\frac{9600}{150} - 1 = 63 \text{ (decimal)} = 3F \text{ (hexadecimal)}$$

Therefore, the hex constant supplied by the program in conjunction with the set control/set mode operation would be 3F.

The bit rate constant for high range operation is determined by the following formula:

$$\text{Constant} = \frac{76800}{\text{bps}} - 1$$

Round off to the nearest whole number and convert to hexadecimal.

Example: Determine the bit rate constant for 1,200 bps (with high-speed jumper installed).

$$\frac{76800}{1200} - 1 = 63 \text{ (decimal)} = 3F \text{ (hexadecimal)}$$

Therefore, the hex constant supplied by the program in conjunction with the set control/set mode operation would be 3F.

There are some bit rates in the ranges shown previously that are incompatible with the attachment. The difference between the bit rate of the attachment and the bit rate of the attached terminal must not exceed 1.5 percent. To determine the difference (in percent) use one of the following methods. An example follows method 2.

Method 1: For attachments that have the low speed jumper installed.

1. Divide the terminal's bit rate into 9,600 and round the answer to the nearest whole number.
2. Multiply the above answer by 0.000104166. This gives the attachment's bit time.
3. Determine the terminal's bit time by taking the reciprocal of the terminal's bit rate.
4. Divide the smaller of the bit times by the larger of the bit times.
5. Subtract the answer from 1.
6. Multiply this answer by 100.

This gives the percentage of difference between the bit rate of the terminal and the actual bit rate of the attachment for a given constant.

Method 2: For attachments that have the high-speed jumper installed. Compute the difference in the same manner as method 1, making the following substitutions:

1. Substitute the number 76,800 for 9,600.
2. Substitute the number 0.0000130208 for 0.000104166.

Example: Determine the difference between the bit rate of the attachment and the bit rate of a terminal that operates at 134.5 bps.

```
Step 1  9600   = 71.37 = 71
        134.5

Step 2  0.000104166
        X          71
        0.007395786 = attachment's bit time

Step 3      1   = 0.007434944 = terminal's bit-time
        134.5

Step 4  (1  0.007395786)  100 = 0.53%
          0.007434944
```

The aggregate throughput rate can be determined by performing the following calculation:

$$\sum_{x=0}^{7} \left[\frac{12B_x}{C_x}\right] \quad \text{or the summation of}$$

$$\left[\frac{12 \cdot B_0}{C_0}\right] + \left[\frac{12 \cdot B_1}{C_1}\right] + \left[\frac{12 \cdot B_2}{C_2}\right] + \left[\frac{12 \cdot B_3}{C_3}\right] +$$
$$\left[\frac{12 \cdot B_4}{C_4}\right] + \left[\frac{12 \cdot B_5}{C_5}\right] + \left[\frac{12 \cdot B_6}{C_6}\right] + \left[\frac{12 \cdot B_7}{C_7}\right]$$

Where:

B=bit rate (see note)

C=character length of line x (character length is equal to the sum of all bits in the character: start, data, parity, and stop).

For example, in a configuration, five lines with the following characteristics are desired:

- Two asynchronous lines at 9600 bps, each having a start bit, five data bits, one parity bit, and one stop bit
- Two asynchronous lines at 2400 bps, each having a start bit, eight data bits, no parity, and two stop bits
- One synchronous line at 9600 bps, having eight data bits and one parity bit

$$\left[\frac{12\ (9600)}{8}\right] + \left[\frac{12\ (9600)}{8}\right] + \left[\frac{12\ (2400)}{11}\right] + \left[\frac{12\ (2400)}{11}\right] + \left[\frac{12\ (9600)}{9}\right] = 46{,}836$$

Because 46,836 bps is less than 64,000 bps, the above configuration is valid.

Note: The **actual** bit rate multiplied by 2 should be used for buffered terminals using continuous receive mode.

Control Characters

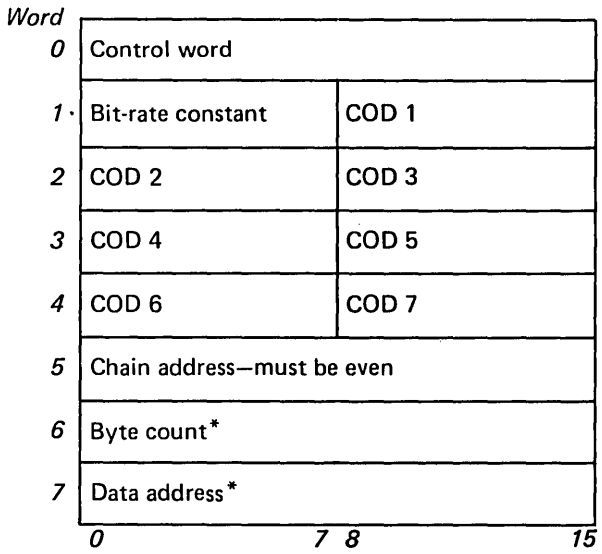
Each remote terminal may require different line control characters, each line of the adapter provides programmable line control characters. For example, a program could specify the same COD character in each of the seven COD positions in a set control or set mode DCB, which would allow 255 possible character configurations or 256 possible character configurations that could be received in an 8-bit code using the receive transparent command. The attachment recognizes up to seven different COD characters. These control characters are specified in the DCB in either the set mode or set control format.

Reception of any of the seven COD characters causes the attachment to end the current receive operation in one of the following conditions:

- Device end interrupt request
- Exception interrupt request
- Chained operation

Note: The programmer must ensure that all COD characters (COD1 to COD7) are defined in the set control/set mode DCB.

These COD characters are transferred to the attachment by the DCB. The DCB format follows:



*Used for synchronous operation
DCB for a set-control/set-mode operation

DCB Word 5 - Chaining Address

The chaining address word (DCB word 5) contains the processor storage address of the next DCB when chaining is indicated. The chaining address must be even; otherwise, the attachment sets interrupt status byte bit 3 to 1 and ends the operation with an exception interrupt request.

DCB Word 6 - Byte Count

The 16-bit byte count word (DCB word 6) contains an unsigned integer that is the byte count for this data transfer.

DCB Word 7 - Data Address

The data address word (DCB word 7) contains the storage address of the first data transfer for the operation being performed.

Start Cycle-Steal Status

The Start Cycle-Steal Status command begins a cycle-steal operation in the addressed device to retrieve status information about the previous cycle-steal operation. The format of the IDCB for this command follows:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 1 1	X X X X X X X X
0 ... *7*	*8* ... *15*
7F	XX

Immediate data field
DCB address
16 ... *31*
XXXX

This command does not allow a chaining operation. The byte count in word 6 must be set to 6 and the data address (word 7) must be on a word boundary (bit 15 is set to 0) or an exception interrupt (CC2) occurs with DCB bit 3 (specification check) in the interrupt status byte set to 1.

See "Cycle-Steal Status Words" later in this chapter for a description of the information transferred to storage by this command.

DCB (device control block)

Word		
0	*Ctrl word* 0 0 1 0 0	*Addr key* X X X	0 0 0 0 0 0 0 0
1	Not used		
2	Not used		
3	Not used		
4	Not used		
5	Not used		
6	Byte count—must be 0006		
7	Data address—must be even		

Three words of status information are available by using the Start Cycle-Steal Status command. This information is available regardless of the setting of ISB bit 0.

Three words (six bytes) of status information are transferred into main storage starting at the data address contained in DCB word 7. Status words 1 and 2 are the only words required for analysis of attachment or terminal link errors.

Status Word 0

Word 0 contains the main storage address of the last attempted cycle-steal data transfer. This residual address may be either a data or DCB address. The value of the residual address must be examined to determine if it is a data address or a DCB address. When reporting a DCB address, the attachment reports the address of the low order byte of the last DCB word that the attachment attempted to fetch.

Status Word 1

Bit 0 - Overrun: During a receive operation, this bit is set to 1 if the attachment is not able to transfer data to storage before the storage data register is needed for new data.

Bit 1 - Time-Out: Set to 1 if:

- During a receive with time out operation, no data is received within the limits established by timer 1.
- During a ring enable with time out operation, ring indicator is not received from the modem within the limits of timer 2.

For error recovery, increase the timer 2 value during a ring enable with time-out. If a ring signal was not received within the limits of timer 2, increase the value of timer 2 and retry.

Bit 2: Not used.

Bit 3 - DCB Reject: Set to 1 under either of the following conditions:

- A transmit type operation is attempted when the attachment is in receive mode.
- A receive type operation is attempted when the attachment is in transmit mode.

Bit 4: Not used.

Bit 5 - VRC Error: The parity of a received character was incorrect. The exception interrupt request is presented at the end of the message.

A special character (hex 00) is placed in main storage when any incorrect data is detected. If communications indicator panel is installed and the DISPLAY/FUNCTION SELECT switches are set to 11110, the received character is placed in storage without any modifications to the character. For expanded mode, inhibit zero insertion affects the adapter error procedure when a bad parity character is received (assumes parity check enabled). Normal adapter operation is to replace the bad parity character with a binary 0 character. When this mode is enabled, the adapter does not zero the character, but provides the character as it was received (incorrect data parity). The interrupt request does not occur until a COD is detected, or the byte count is reduced to 0 and the chain bit is set to 0.

For error recovery, the program should transmit a negative acknowledgement and retry.

Bit 6 - Break: During a transmit allow break, transmit end allow break, or transmit end allow break with prereceive operation, a break condition was detected. The attachment ends the operation and resets transmit mode and RTS (if RTS is not wired on). For error recovery, the program can then issue either a receive command or continue transmitting. During continuous receive mode, break detect will not be presented.

Bit 7 - Stop-Bit Error: A character was received with a stop bit missing. The exception interrupt request occurs as soon as the error is detected.

For error recovery, the program should transmit a negative acknowledgement and retry.

Bit 8: Not used.

Bit 9 - Modem Interface Error: Conditions that cause this error are:

- DSR is not activated from the modem within the predetermined time after a TR enable with time-out operation begins.
- CTS is not activated from the modem within the time specified by timer 2 during any transmit or DTR enable with answer tone operation.
- DTR or DSR are not active at the beginning of a transmit or a receive operation.
- CTS is active for more than 1 second while RTS is inactive at the beginning of a transmit operation. (If CTS is permanently returned, RTS must be wired on.)
- DTR or DSR is lost during a transmit or receive operation.
- RTS or CTS is lost during a transmit or answer tone operation.
- Carrier detect becomes inactive during a receive operation if the carrier detect jumper is not installed.
- Carrier detect is not received during a receive with time-out operation if the carrier detect jumper is not installed.

If a modem interface error is reported, for error recovery, the programmer should examine status word 2 and retry. If DTR is set to 1, the attachment expects DSR to be to set 1; if RTS is set to 1, the attachment expects CTS to be set to 1.

Bits 10-11: Not used.

Bit 12 - Error During Pre-receive, Adapter Buffer Full: Set to 1 when an error is detected during an operation with prereceive. Set to 1 if operating in expanded mode with continuous receive and the adapter buffer is full.

Bits 13-14: Not used and must be set to 0.

Bit 15: Reflects the status of the adapter buffer. If this bit is set to 1, a read adapter buffer operation followed by another Start Cycle-Steal Status command must be issued to reset any error conditions and enable attention interrupts.

Note: More than one error may be reported in status word 1. An example is a VRC error with an overrun, time-out, modem interface error, or error during prereceive.

Word 2

Bit 0 - Data Terminal Ready: A signal from the attachment to the modem that indicates whether DTR was active at the time the Start Cycle-Steal Status command was issued. It expects a DSR (bit 1) response from the modem.

DTR is set by the DTR enable type DCBs.

Bit 1 - Data Set Ready: A signal to the attachment from the modem. It is either in response to DTR (bit 0) or is a power on indication from a leased line modem.

If DSR is always set to 1, install the DTR jumper on the attachment.

Bit 2 - Request to Send: An outbound signal from the attachment to the modem when the attachment wishes to transmit. Expect a CTS (bit 3) returned from the modem.

Some duplex modems always signal CTS as a power on indication; in this case, the RTS jumper on the attachment must be installed.

Bit 3 - Clear to Send: An inbound signal to the attachment from the modem in response to RTS (bit 2) signal.

Bit 4 - External Clocks: Set to 1 if the bit-rate constant in the DCB for a set mode/set control operation is set to 00, indicating modem clocking is being used.

Bit 5 - Carrier Detect: Set to 0 or 1 when the attachment is connected to a modem and the carrier detect jumper is installed.

Bit 6 - Echoplex: Set to 1 if the attachment is in echoplex mode.

Bit 7 - Receive Data Lead: May be set to 0 or 1.

Bits 8-15 - Indicator Panel: Designates the communications indicator panel DISPLAY/FUNCTION SELECT switch settings.

Interrupt Status Byte

When the attachment presents an exception interrupt request (along with an interrupt condition code of 2 or 6) to the processor, the interrupt status byte is used to record status that cannot be indicated to the program by the condition codes. The attachment presents the interrupt status byte to the processor as bits 0 through 7 of the interrupt ID word.

The bits and their meanings follow.

Bit 0 - Device Dependent Status Available: If this bit is set to 1, additional status is available by using the Start Cycle Steal Status command (described later in this chapter). This bit may be set to 1 in conjunction with bit 2 (incorrect length record).

Bit 1 - Delayed Command Reject: Set to 1 for any of the following conditions:

- The IDCB contains an odd DCB address.
- The IDCB contains an invalid function modifier.
- The IDCB is for a command that performs a write operation.

Bit 2 - Incorrect Length Record: Can be reported during all receive operations except the receive transparent operation. If ISB bit 0 is set to 0 and bit 2 is set to 1, the byte count has gone to 0 and the attachment has not received a COD character. If ISB bits 0 and 2 are set to 1, the attachment received a COD character and the byte count was not 0.

Bit 3 - DCB Specification Check: Set to 1 under any of the following conditions:

- The DCB contains an odd chaining address (DCB word 5).
- The byte count (DCB word 6) contains a value other than 6 for a Start Cycle-Steal Status command.
- The data address (DCB word 7) contains an odd address for the following: a Start Cycle-Steal Status, Start Control, or Start Diagnostic command (the chaining bit must be set to 0 for these commands).
- The byte count for a transmit or receive operation is 0.
- Bit 2 of the DCB control word (word 0) is not set appropriately for the operation.
- The byte count of a Start Diagnostic 1 command is not set to 12.
- The byte count of a Start Diagnostic 2 command is not set to 6.
- Bit 2 of the control word for a Start Control command is set to 1 and the byte count is not set to hex 0400 or hex 0040.
- Bit 2 of the control word for a Start Control command is set to 0 and the byte count is not set to hex 01B0 or hex 0000.
- The PCI bit is on for other than transmit or receive type operations.

Bit 4 - Storage Data Check: Set to 1 during cycle-steal output operations only. It indicates that the storage location accessed during the current output cycle contained incorrect parity. The parity in main storage is not corrected. The attachment ends the operation.

Bit 5 - Invalid Storage Address: Set to 1 if the storage address presented by the attachment for data or DCB access exceeds the storage size of the system. The attachment ends the operation.

Bit 6 - Protect Check: Set to 1 if the attachment attempted to access a storage location without the correct cycle-steal address key. The attachment ends the operation.

Bit 7 - Interface Data Check: Set to 1 if a parity error was detected on the Series/1 interface during a cycle-steal data transfer. The condition can be detected by the processor I/O channel or the attachment. In either case, the operation is ended and an exception interrupt request is presented to the processor.

0	1	2	3	4	5	6	7
Device-dependent status available	Delayed command reject	Incorrect-length record	DCB specification check	Storage data check	Invalid storage address	Protect check	Interface data check

Interrupt Information Byte (IIB)

When the attachment presents an interrupt, the IIB is used to record additional information. If the CC equals 3 (CC3) the IIB=0000. If the CC equals 4 (CC4) and expanded mode is being used, the IIB equals the character received.

Status After Resets

There are several methods of resetting some or all of the circuits in the attachment. The resets and their effects are shown in the chart:

	Power-on reset	*System reset*	*Halt I/O*	*Device reset*	*DCB command reset*	*Indicator panel reset*
DTR with jumper	On	On	On	On	On	On
DTR without jumper	Off	-	-	-	-	Off
RTS with jumper	On	On	On	On	On	On
RTS without jumper	Off	Off	Off	Off	Off	Off
Interrupt level	Off	Off	-	-	-	-
I-bit	Off	Off	-	-	-	-
Set control	*	-	-	-	-	-
Pending interrupts	Off	Off	Off	Off	-	-
Residual address	**	-	-	-	-	-
Echoplex	Off	Off	Off	Off	Off	-
Trace	Off	***	***	***	-	-
Expanded mode	Off	Off	Off	Off	-	-

*Defaults to 8 data bits, 2 stop bits, no parity, internal clock.
**Reset to 0000.
***Does not disable the trace; logs the reset, if enabled.
- Does not change.

Error Recovery

Operate I/O Condition Codes

This attachment may present a variety of operate I/O condition codes. The codes for each type of Operate I/O command with a recommended program recovery or end procedure are given following the programmable multiline operate I/O condition codes chart.

There will be only one controller end interrupt request when multiple controller busy operate I/O condition codes are presented; consequently, the program should queue the controller busy condition codes and clear (post) the controller end interrupt condition code to all controller busy codes received.

Note: Under certain conditions, it is possible that more than one controller end interrupt request is presented. If no busy condition is found upon examining the controller busy queue, disregard the interrupt request.

Programmable multiline Operate I/O condition codes

CC	Even	Carry	Overflow	Meaning
0	0	0	0	Not attached
1	0	0	1	Busy
2	0	1	0	Not reported by this attachment
3	0	1	1	Command reject
4	1	0	0	Not reported by this attachment
5	1	0	1	Interface data check
6	1	1	0	Controller busy (see Note)
7	1	1	1	Satisfactory

Note: Reported when the controller is busy servicing a previous Operate I/O instruction; a subsequent controller end interrupt request will occur (interrupt condition code 0).

The following table shows recommended error recovery or end procedures for operate I/O error conditions:

Operate I/O command	*Controller busy for next Operate I/O*	*Operate I/O CC*	*Recommended action*
Read ID	No	0	End; device not attached
		1,2,4,6	End; hardware error
		3	End; examine IDCB function
		5	Retry; end if problem persists
		7	Satisfactory
Prepare	No	0	End; device not attached
			Examine bit 15 (I-bit of the IDCB); if bit 15 equals 1, end; if bit 15 equals 0, correct program
		2,4,6	End
		3	End; examine IDCB function
		5	Retry; end if problem persists
		7	Satisfactory
Halt I/O	No	0,1,2,3,4,5,6	End
	7	Satisfactory	
Device Reset	Yes	0	End; device not attached
		1,2,4,6	End
		3	Examine IDCB function; if OK, end
		5	Retry; if trouble persists, end
		7	Satisfactory
Write Data	Yes	0	End; device not attached
		1	Retry after device end if the device is busy or device reset, retry. If trouble persists, end.
		2	End
		3	Examine IDCB, if correct, end
		4	End
		5	Retry; if trouble persists, end
		6	Retry after controller end interrupt
		7	Satisfactory
Start Start Cycle Steal Status, Start Diagnostics 1 and 2, Start Control	Yes	0	Device not attached; end
		1	Retry after device end if device is busy or device reset then retry; if problem persists, end
		2	End
		3	Examine function in IDCB; if correct, end
		4	End
		5	Retry; if trouble persists, end
		6	Retry after controller end interrupt
		7	Satisfactory

Interrupt Condition Codes

Interrupt requests can only occur for the feature - programmable multiline attachment following the acceptance of the following commands:

- Prepare (This command is not an interrupting command. An interrupt request can occur when the device is unprepared and an interrupt request is pending. This command is issued with the I-bit equal to 1.)
- Write Data
- Start
- Start Cycle-Steal Status
- Start Diagnostic 1
- Start Diagnostic 2
- Start Control

The only interrupt codes presented by the attachment are 0, 1, 2, 3, 4, and 6. If an interrupt condition code 2 or 6 is reported, the program should examine the ISB and issue a Start Cycle-Steal Status command (if the ISB bit 0 is active)

Programmable multiline interrupt condition codes

CC	Even	Carry	Overflow	Meaning
0	0	0	0	Controller end (see Note)
1	0	0	1	PCI
2	0	1	0	Exception
3	0	1	1	Device end
4	1	0	0	Attention*
5	1	0	1	Attention and PCI*
6	1	1	0	Attention with exception*
7	1	1	1	Attention and device end

*These interrupts do not end any pending commands.

Note: The controller presents the device address of line 0.

The following chart shows the recommended actions for various combinations of condition codes and interrupt status byte values. (The interrupt status byte bit meanings are included for your convenience.)

Interrupt status byte

Bit	Name
0	Device dependent status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage check
5	Invalid storage address
6	Protection check
7	Interface data check

Interrupt CC	*ISB (hex)*	*Recommended action*
0	-	Retry Operate I/O commands queued with controller busy operate I/O condition code.
2	A0	Normal ending operation to a receive DCB if a COD was detected prior to reducing the byte count to 0. Perform a Start Cycle-Steal Status command to obtain residual address.
2	80	Issue a Start Cycle-Steal Status command; examine bits to determine further action.
2	40	Examine IDCB for invalid function modifier or odd DCB address; correct error condition; retry.
2	20	Occurs during a receive operation and indicates that the byte count reduced to 0 and no COD character was detected. Increase the receive data buffer size and byte count and retry.
2	10	Indicates that the DCB being processed had one or more of the following errors: an odd chaining address (word 5); a Start Cycle-Steal Status DCB had a byte count other than 6 or an odd address; a transmit or receive DCB had a byte count of 0; the I/O bit of the DCB control word is incorrect; a diagnostic type DCB had incorrect byte count or odd data address; a Start Control command to an attachment with the I/O bit in the control word set to 1 did not have a byte count of hex 400 or hex 040, or, if the I/O bit equals 0, had an odd data address. Correct the error and retry.
2	08	Storage data check; retry operation; if error persists, end.
2	04	Invalid storage address; correct program and retry.
2	02	Protect check; verify the protect key and retry. This error can only occur on a Series/1 processor that has the storage protection feature.
2	01	Interface data check; retry once; if the error persists, end.
4 *	XX	Attention interrupt, used in expanded mode with ISB/IIB equal to the character received.
6 *	80	Attention with exception, always indicates that the expanded mode of operation (attention interrupt) detected an error on receive. This interrupt does not end any outstanding I/O commands.

* Unsolicited

Jumper Options

Reference CE binder MLD sheet SC xxxx for controller card jumper layout.

On this attachment, the base device address must have the following:

- The device addresses must be sequential.
- The first device address must have bits 13, 14, and 15 equal to 0.

The following options can be selected by installing jumpers on the 4-line feature card. Reference CE binder MLD sheet SC xxxx for 4-line adapter card jumper layout.

Request to Send

There are four RTS jumpers on the card - one for each line. If the jumper is installed, the attachment maintains RTS in an active condition for that line. This eliminates modem turnaround when using a duplex interface. This option must be selected when using a modem that always keeps CTS active.

Data Terminal Ready

There are four DTR jumpers on the card - one for each line. If the jumper is installed, the attachment maintains DTR in an active condition for that line. To enable disconnecting from a switched network, this option should not be selected for switched line operation.

Bit-Rate Jumpers

There are four sets (one low range and one high range) of jumpers for the card, one for each line. Either high range or low range must be selected for each line, but not both.

With the low range jumper installed, speeds between 37.5 and 1,200 bps can be selected by programming; with the high-speed jumper installed, speeds between 300 and 19,200 bps can be selected by programming.

Carrier Detect

There are four carrier detect jumpers on the card - one for each line. Some modems offer the ability to check the quality of the received signal. When the signal is of acceptable quality, the modem generates carrier detect. If the received signal starts to deteriorate, the modem notifies the attachment by deactivating carrier detect.

Carrier detect is a function of the remote site when RTS and CTS are active. A loss of carrier detect may be caused by the local modem, open lines, the remote modem, or the remote station not being in transmit mode.

If the carrier detect jumper is not installed on the attachment card, the attachment waits for carrier detect from the modem at the beginning of a receive type operation. If carrier detect does not become active within the time specified by timer 1, or if it becomes inactive during the receive operation, the attachment presents an exception interrupt request to the processor and activates modem interface error. Carrier detect also informs the user that the remote station has RTS active.

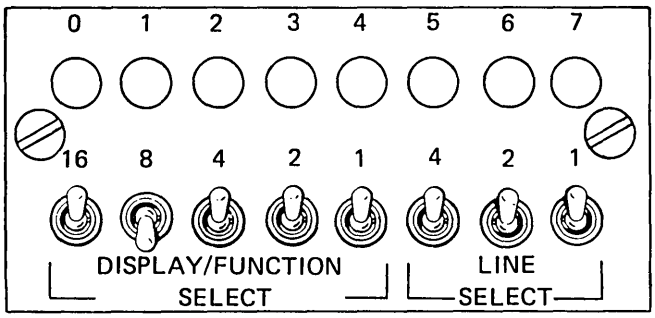
Line Interface Circuits

There are two types of line interface circuit jumpers: an EIA RS-232C/CCITTV24 interface and a 20-milliampere current loop interface. One or the other of the options must be selected for each line, but not both.

Communications Indicator Panel

This optional panel is a valuable aid to program debugging and machine trouble-shooting.

The communications indicator panel displays various conditions and registers in the attachment. In addition, the DTR line(s) to the modem(s) can be reset from the indicator panel. One setting of the DISPLAY/FUNCTION SELECT switches causes any incorrect data that is received to be placed in storage as is.



LINE SELECT Switches

The three LINE SWITCHES switches are used to select a particular line. A line is selected by setting the last three bits of its device address, in binary form, into the LINE SELECT switches.

DISPLAY/FUNCTION SELECT Switches

The DISPLAY/FUNCTION select switches determine what information is displayed on the panel. Following is a list of switch settings and the information that is displayed on the panel.

DISPLAY/ FUNCTION SELECT	*Lamps*	*Information*
00000	0-7	High order byte of the DCB control word
00001	0-7	Low order byte of the DCB control word
00010	0-7	Bit-rate constant
00011	0-7	Line-control character 1
00100	0-7	Line-control character 2
00101	0-7	Line-control character 3
00110	0-7	Line-control character 4
00111	0-7	Line-control character 5
01000	0-7	Line-control character 6
01001	0-7	Line-control character 7
01010	0-7	Bits 0-7 of the chain address
01011	0-7	Bits 8-15 of the chain address
01100	0-7	Bits 0-7 of the byte count
01101	0-7	Bits 8-15 of the byte count
01110	0-7	Bits 0-7 of the data address
01111	0-7	Bits 8-15 of the data address
10000	0-7	Bits 0-7 of timer 2
10001	0-7	Bits 8-15 of timer 2
10010	0-7	Bits 0-7 of timer 1
10011	0-7	Bits 8-15 of timer 1
10100	0-4	Base device addresses
	5	Interrupt condition code (LSR even)
	6	Interrupt condition code (LSR carry)
	7	Interrupt condition code (LSR overflow)
10101	0-7	Engineering use
10110	0	Overrun
	1	Time-out
	2	Not used
	3	DCB reject
	4	Not used
	5	Parity error - VCR
	6	Break detected
	7	Stop bit error

DISPLAY/ FUNCTION SELECT	*Lamps*	*Information*
10111	0	Engineering use
	1	Modem interface error
	2-3	Engineering use
	4	Error during prereceive/adapter buffer full
	5-6	Engineering use
	7	Adapter buffer not empty
11000	0-7	Engineering use
11001	0	Data terminal ready
	1	Data set ready
	2	Request to send
	3	Clear-to-send
	4	External clocks
	5	Carrier detect
	6	Echoplex
	7	Receive line (on=mark)
11010	0-7	Engineering use
11011	0-7	Set mode or set control (bits 8-15 in the control word)
11100	0-7	Lamp test
11101	0-7	Interrupt status byte
11110	0-7	Place data into storage as is. Inhibit 00 insert.
11111 *	0	Data terminal ready
	1	Data set ready
	2	Request to send
	3	Clear-to-send
	4	External clocks
	5	Carrier detect
	6	Echoplex
	7	Receive

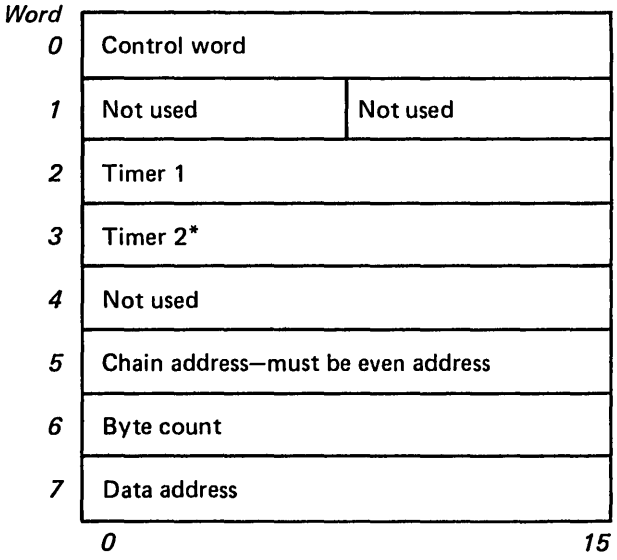
* Resets DTR + RTS if not jumpered on.

Appendix A. Multi-Line Attachment Reference Summary

I/O Commands

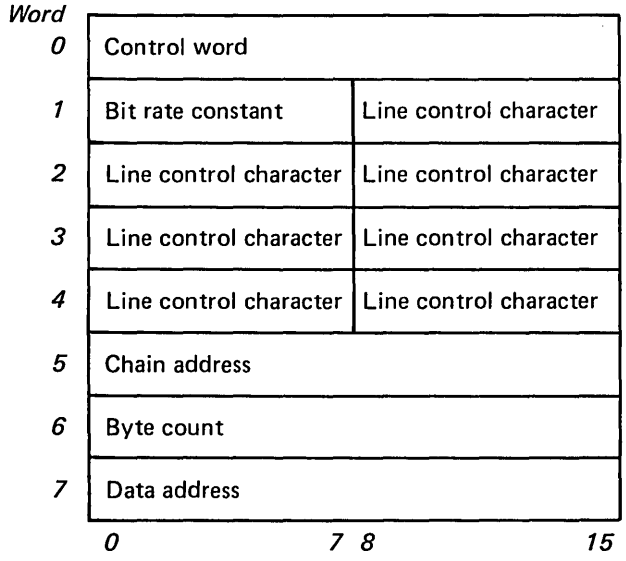
Hex	*Command*	*I/O instruction CCs reported*
	Read ID	0, 5, 7
0	Prepare	0, 1, 5, 7
6F	Device Reset	0, 7
70	Start	0, 1, 5, 6, 7
7C	Start Control	0, 1, 5, 6, 7
7D	Start Diagnostic 1	0, 1, 5, 6, 7
E	Start Diagnostic 2	0, 1, 5, 6, 7
F		Start Cycle-Steal Status 0, 1, 5, 6, 7

Device Control Block (DCB) — General Format



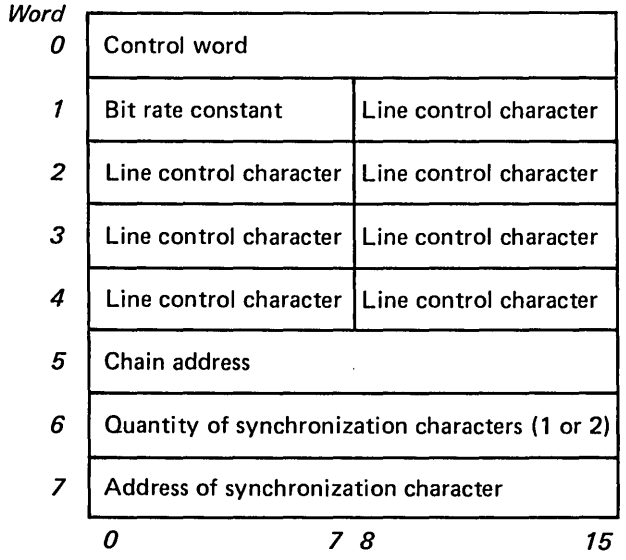
*Dual function word. In transmit, it contains Timer 2 and PCI information. In receive, it contains only PCI information.

Device Control Block (DCB) — Set Mode and Set Control (Asynchronous)



Device Control Block (DCB) — Set Mode (Synchronous)

Set Mode (Synchronous)



ntrol Word

Bit	Meaning
0	Chaining flag
1	Program-controlled interrupt
2	Input flag
3–4	Not used—zeros
5–7	Cycle-steal address key
8–15	Operation

00000000	Transmit
00000001	Transmit end
00010001	Transmit end with pre-receive
00000010	Transmit allow break
00000011	Transmit end allow break
00010011	Transmit end allow break with pre-receive
00000100	Receive
00000101	Receive with time-out
00010100	Receive with block check character
00010101	Receive with time-out and block check character
00100100	Receive with echo-plex
00100101	Receive with time-out and echo-plex
00110100	Receive with echo-plex and block check character
00110101	Receive with echo-plex, time-out, and block check character
01000100	Receive transparent
01000101	Receive transparent with timer
01100100	Receive transparent with echo-plex
01100101	Receive transparent with echo-plex and timer
00000110	Ring monitor
00000111	Ring monitor with time-out
00001000	Data terminal ready (DTR) enable
00001001	Data enable with time-out
00001010	DTR enable with answertone
00001011	DTR enable with answertone and time-out
00001100	DTR disable
00011101	Set control*
00001110	Program delay
00001111	Reset
00001101	Not supported. If issued, ISB bit 3 (DCB specification check) is set equal to 1.

*The attachment is placed in asynchronous mode with 8 data bits, no parity, and 2 stop bits.

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0	Overrun
1	Time-out
2	Not used
3	DCB reject
4	Not used
5	Parity error detected on receive
6	Break
7	Stop bit error
8	Not used
9	Modem interface error
10–11	Not used — zeros
12	Error during pre-receive
13–15	Not used — zeros

Word 2

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request-to-send
3	Clear-to-send
4	External clocks
5	Data carrier detect
6	Echo-plex
7	Receive data lead (when set to 1, equals the mark state)
8–15	Indicator panel setting

Interrupt Condition Codes Reported

CC0,CC1, CC2, CC3

Interrupt Information Byte (IIB)

Condition code	IIB contents
0, 3	Always zero
1	Program-controlled interrupt identifier
2	Cycle-steal interrupt status byte

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor.

Appendix B. Communications Operator's Self-Test Procedure

The communication adapters operator self-test program needs a minimum system configuration of:

- a Series/1 processor with 16K storage
- a diskette drive feature 4964 or 4962 model 2
- a programmer console feature 5650, and
- a one communication adapter feature 2095/2096.

1. Remove power, disconnect the modem cable at the modem and connect the wrap connector at the modem end of the cable as follows:

Modem cable part number	Wrap connector part number
1632208	2704136
1632211	1633811
1632919	*

*Do not disconnect the modem cable but place the switch in the cable extension part number 2722052 in the test position.

2. Insert the basic diskette.
3. Press the load button on the programmer console.
4. If the system has only a programmer console go to step 10.
5. Wait for the input/output device (as configured in the diagnostic diskette) to print the following message:

   RDY

   ENTER
6. Begin the operator self-test program be entering B3CEF on the input/output device.
7. The output device will then print:

   ENTER DEVICE ADDRESS AND LOOP COUNT

   ENTER
8. Enter FDAXX (where DA=device address and XX=loop count in hexadecimal).

   Example:

   F1801 (DA=18, loop count=01).

9. Wait for one of the following messages to appear then take the appropriate operator action:

   Message:

   DEVICE ADDRESS ERROR

   REENTER DEVICE ADDRESS AND LOOP COUNT

   ENTER

   Operator action:

   Verify that the device address is correct and call the service organization or return to step 8.

   Message:

   TEST WAS SUCCESSFUL

   Operator action:

   None, self-explanatory.

   Message:

   THE TEST FAILED, CALL THE SERVICE ORGANIZATION

   Operator action:

   Verify that the cable and wrap connector have the correct part numbers and call the service organization or return to step 8.

   After the loop count has been exhausted, the program returns to step 7. At this time, you may run the test again or end the program by returning the system to the operating state. (Steps 10 through 16 of this procedure are for systems with only a programmer's console.)

   Note: The running time for each feature per pass is as follows:

Feature	Time
2091/2092	8 seconds

10. Wait for a hexadecimal 3800 in the lights of the programmer console.
11. Insert the SIO/communications diskette.
12. Press the data buffer button and enter 000B, then press the console interrupt button. Press the data buffer button again and enter 3CEF, then press the console interrupt button twice.
13. Wait for 3CE1 on the lights of the programmer console.
14. Press data buffer and enter 001F, then depress the console interrupt button.
15. Press the data buffer and enter DAXX (where DA=device address and XX=loop count). Press the console interrupt button twice.

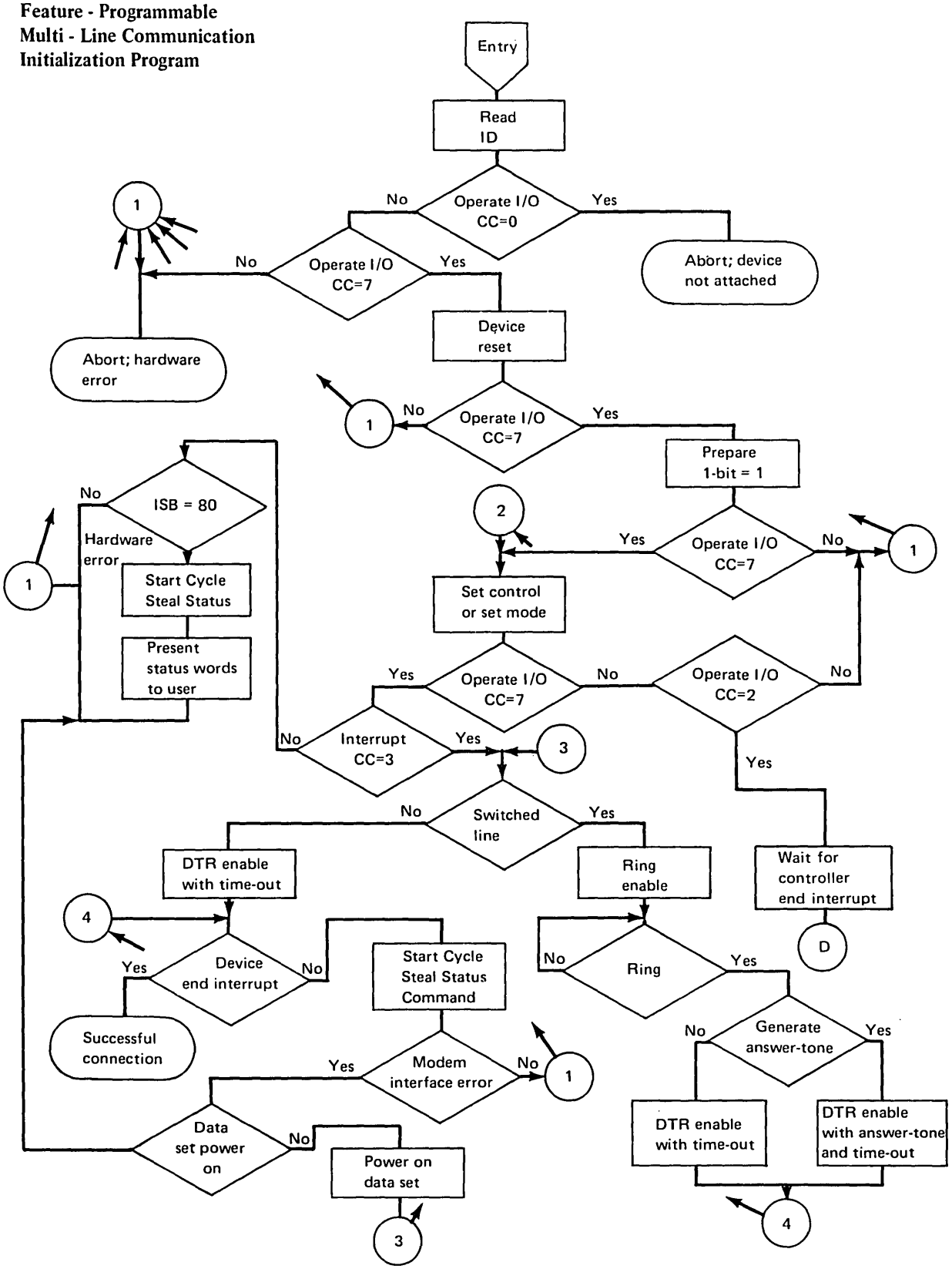
16. Wait for one of the following values to appear in the lights of the programmer console.

Value in lights	Operator action
3CE2 (Device address error)	Verify the address is correct and call the service organization or go to step 1.
3CE3 (Test successful)	Self-explanatory
3CE4 (The test failed, call the service organization	Verify that the cable wrapped in the correct one and call the service organization or return to step 11.

17. Press the data buffer button, enter 0006, and press the console interrupt button twice. Wait for the lights to indicate 3CE1 and proceed to step 13 to run the test again, if desired, or return the system to the operating state.

Appendix C. Multiline Adapter Initialization Program

Feature - Programmable
Multi - Line Communication
Initialization Program



Appendix D. Transmission Codes

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/ correspondence
0	00	0000 0000	NUL	NUL	NUL		
1	01	0001	SOH	SOH	NUL	space	space
2	02	0010	STX	STX		1	1,]
3	03	0011	ETX	ETX	@		
4	04	0100	PF	EOT		2	2
5	05	0101	HT	ENQ	space		
6	06	0110	LC	ACK			
7	07	0111	DEL	BEL		3	3
8	08	1000		BS		4	5
9	09	1001	RLF	HT			
10	0A	1010	SMM	LF	P (even parity)		
11	0B	1011	VT	VT	P (odd parity)	5	7
12	0C	1100	FF	FF	0 (even parity)		
13	0D	1101	CR	CR	0 (odd parity)	6	6
14	0E	1110	SO	SO		7	8
15	0F	1111	SI	SI			
16	10	0001 0000	DLE	DLE		8	4
17	11	0001	DC1	DC1			
18	12	0010	DC2	DC2	H (even parity)		
19	13	0011	TM	DC3	H (odd parity)	9	0
20	14	0100	RES	DC4	((even parity)		
21	15	0101	NL	NAK	((odd parity)	0	z
22	16	0110	BS	SYN		Ⓓ (EOA)	Ⓓ (EOA),9
23	17	0111	IL	ETB			
24	18	1000	CAN	CAN			
25	19	1001	EM	EM			
26	1A	1010	CC	SUB			
27	1B	1011	CU1	ESC	X		
28	1C	1100	IFS	FS		uppercase	uppercase
29	1D	1101	IGS	GS	8		= ^
30	1E	1110	IRS	RS			
31	1F	1111	IUS	US		Ⓒ (EOT)	Ⓒ (EOT)
32	20	0010 0000	DS	space		@	t
33	21	0001	SOS	!	EOT		
34	22	0010	FS	"	D (even parity)		
35	23	0011		#	D (odd parity)	/	x
36	24	0100	BYP	$	S (even parity)		
37	25	0101	LF	%	S (odd parity)	s	n
38	26	0110	ETB	&		t	u
39	27	0111	ESC	'			
40	28	1000		(			
41	29	1001		)		u	e
42	2A	1010	SM	*		v	d
43	2B	1011	CU2	+	T		
44	2C	1100		,		w	k
45	2D	1101	ENQ	-	4		
46	2E	1110	ACK	.			
47	2F	1111	BEL	/		x	c
48	30	0011 0000		0	forms feed		
49	31	0001		1	forms feed	y	l
50	32	0010	SYN	2		z	h
51	33	0011		3	L		
52	34	0100	PN	4			
53	35	0101	RS	5	,		
54	36	0110	UC	6			

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data interchange	PTTC/EBCD	PTTC/ correspondence
55	37	0011 0111	EOT	7		Ⓢ (SOA),comma	b
56	38	1000		8			
57	39	1001		9			
58	3A	1010		:	\ (even parity)		
59	3B	1011	CU3	;	\ (odd parity)	index	index
60	3C	1100	DC4	<	< (even parity)		
61	3D	1101	NAK	=	< (odd parity)	Ⓑ (EOB)	
62	3E	1110		>			
63	3F	1111	SUB	?			
64	40	0100 0000	space	@		Ⓝ	!
65	41	0001		A	EOA		
66	42	0010		B	B (even parity)		
67	43	0011		C	B (odd parity)	i	m
68	44	0100		D	" (even parity)		
69	45	0101		E	" (odd parity)	k	
70	46	0110		F		l	v
71	47	0111		G			
72	48	1000		H			
73	49	1001		I		m	'
74	4A	1010	¢	J		n	r
75	4B	1011	.	K	R		
76	4C	1100	<	L		o	i
77	4D	1101	(	M	2		
78	4E	1110	+	N			
79	4F	1111	]	O		p	a
80	50	0101 0000	&	P	line feed		
81	51	0001		Q	line feed	q	o
82	52	0010		R		r	s
83	53	0011		S	J		
84	54	0100		T			
85	55	0101		U	*		
86	56	0110		V			
87	57	0111		W		$	w
88	58	1000		X			
89	59	1001		Y			
90	5A	1010	!	Z	Z (even parity)		
91	5B	1011	$	[	Z (odd parity)	CRLF	CRLF
92	5C	1100	*	\	: (even parity)		
93	5D	1101	)	]	: (odd parity)	backspace	backspace
94	5E	1110	;	Λ		idle	idle
95	5F	1111	¬	—			
96	60	0110 0000	-		ACK		
97	61	0001	/	a		&	j
98	62	0010		b		a	g
99	63	0011		c	F		
100	64	0100		d		b	
101	65	0101		e	&		
102	66	0110		f			
103	67	0111		g		c	f
104	68	1000		h		d	p
105	69	1001		i			
106	6A	1010	¦	J	V (even parity)		
107	6B	1011	,	k	V (odd parity)	e	
108	6C	1100	%	l	6 (even parity)		
109	6D	1101	—	m	6 (odd parity)	f	q
110	6E	1110	>	n		g	comma
111	6F	1111	?	o			
112	70	0111 0000		p		h	/
113	71	0001		q	shift out		
114	72	0010		r	N (even parity)		

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/ correspondence
115	73	0011		s	N (odd parity)	i	y
116	74	0100		t	. (even parity)		
117	75	0111 0101		u	. (odd parity)		
118	76	0110		v		Ⓨ ,period	
119	77	0111		w			
120	78	1000		x			
121	79	1001		v			
122	7A	1010	:	z		horiz tab	tab
123	7B	1011	#	{	↑		
124	7C	1100	@	|		lowercase	lowercase
125	7D	1101	'	}	>		
126	7E	1110	=	~			
127	7F	1111	"	DEL		delete	
128	80	1000 0000					
129	81	0001	a		SOM	space	space
130	82	0010	b		A (even parity)	=	±,[
131	83	0011	c		A (odd parity)		
132	84	0100	d		! (even parity)	<	@
133	85	0101	e		! (odd parity		
134	86	0110	f				
135	87	0111	g			;	#
136	88	1000	h		X-ON	:	%
137	89	1001	i				
138	8A	1010					
139	8B	1011			Q	%	&
140	8C	1100					
141	8D	1101			1	'	¢
142	8E	1110				>	*
143	8F	1111					
144	90	1001 0000			horiz tab	*	$
145	91	0001	j		horiz tab		
146	92	0010	k				
147	93	0011	l		I	(	)
148	94	0100	m				
149	95	0101	n		)	)	Z
150	96	0110	o			Ⓓ (EOA),"	(
151	97	0111	p				
152	98	1000	q				
153	99	1001	r				
154	9A	1010			Y (even parity)		
155	9B	1011			Y (odd parity)		
156	9C	1100			9 (even parity)	uppercase	uppercase
157	9D	1101			9 (odd parity)		
158	9E	1110					
159	9F	1111				Ⓒ (EOT)	Ⓒ (EOT)
160	A0	1010 0000			WRU (even)	¢	T
161	A1	0001	~		WRU (odd)		
162	A2	0010	s				
163	A3	0011	t		E	?	X
164	A4	0100	u				
165	A5	0101	v		%	S	N
166	A6	0110	w			T	U
167	A7	0111	x				
168	A8	1000	y				
169	A9	1001	z			U	E
170	AA	1010			U (even parity)	V	D
171	AB	1011			U (odd parity)		
172	AC	1100			5 (even parity)	W	K

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/ correspondence
173	AD	1101			5 (odd parity)		
174	AE	1110					
175	AF	1111				X	C
176	B0	1011 0000					
177	B1	0001			return	Y	L
178	B2	0010			M (even parity)	Z	H
179	B3	1011 0011			M (odd parity)		
180	B4	0100			- (even parity)		
181	B5	0101			- (odd parity)		
182	B6	0110					
183	B7	0111				Ⓢ (SOA), |	B
184	B8	1000					
185	B9	1001					
186	BA	1010					
187	BB	1011			]	index	index
188	BC	1100					
189	BD	1101			=	Ⓑ (EOB)	
190	BE	1110					
191	BF	1111					
192	C0	1100 0000	{		EOM (even)	Ⓝ –	
193	C1	0001	A		EOM (odd)		
194	C2	0010	B				
195	C3	0011	C		C	J	M
196	C4	0100	D				
197	C5	0101	E		#	K	
198	C6	0110	F			L	V
199	C7	0111	G				
200	C8	1000	H				
201	C9	1001	I		X-OFF	M	"
202	CA	1010			S (even parity)	N	R
203	CB	1011			S (odd parity)		
204	CC	1100	ʃ		3 (even parity)	O	I
205	CD	1101			3 (odd parity)		
206	CE	1110	ʏ				
207	CF	1111				P	A
208	D0	1101 0000	}				
209	D1	0001	J		vertical tab	Q	O
210	D2	0010	K		K (even parity)	R	S
211	D3	0011	L		K (odd parity)		
212	D4	0100	M		+ (even parity)		
213	D5	0101	N		+ (odd parity)		
214	D6	0110	O				
215	D7	0111	P			!	W
216	D8	1000	Q				
217	D9	1001	R				
218	DA	1010					
219	DB	1011			[	CRLF	CRLF
220	DC	1100					
221	DD	1101			;	backspace	backspace
222	DE	1110				idle	idle
223	DF	1111			PAD		
224	E0	1110 0000	\				
225	E1	0001			bell	+	J
226	E2	0010	S		G (even parity)	A	G
227	E3	0011	T		G (odd parity)		
228	E4	0100	U		, (even parity)	B	+
229	E5	0101	V		, (odd parity)		
230	E6	0110	W				

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/ correspondence
231	E7	0111	X			C	F
232	E8	1000	Y			D	P
233	E9	1001	Z				
234	EA	1010					
235	EB	1011			W	E	
236	EC	1100					
237	ED	1101			7	F	Q
238	EE	1110				G	comma
239	EF	1111					
240	F0	1111 0000	0		shift in (even)	H	?
241	F1	0001	1		shift in (odd)		
242	F2	0010	2				
243	F3	0011	3		O	I	Y
244	F4	0100	4				
245	F5	0101	5		/		
246	F6	0110	6			Ⓨ , ¬	—
247	F7	0111	7				
248	F8	1000	8				
249	F9	1001	9				
250	FA	1010	LVM		⇐ (even parity)	horiz tab	tab
251	FB	1011			⇐ (odd parity)		
252	FC	1100			? (even parity)	lowercase	lowercase
253	FD	1101			? (odd parity)		
254	FE	1110					
255	FF	1111			delete / rub out	delete	

Note: When used with the BSCA, the software must maintain parity in bits 0–7 of each byte.

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