IMSAI

SIO 2

SIO 2 Board

FUNCTIONAL DESCRIPTION

The SIO Board provides a serial input/output capability for the IMSAI 8080 System. It contains two serial I/O ports, providing two complete RS232 full duplex data lines with all control signals. Data lines for both channels are provided in RS 232, TTL Level and current loop formats. Asynchronous or synchronous lines utilizing full or half duplex can be run with this board at any rate up to 9600 baud in the Asynchronous mode and 56,000 baud in the Synchronous mode.

The SIO Board may be jumper-selected to respond either to input and output instructions from the IMSAI 8080 System or to memory reference instructions for memory-mapped I/O.

Operation of the board requires 16 I/O port or address locations, which are selected by address bits 0 through 3. When the board is used with input and output instructions, address bits 4 through 7 form the remainder of the board address and are jumper selectable. When the board is used as memory-mapped I/O, the lower byte of address is jumper selected exactly the same as an I/O port address and the upper byte of address is hex FE or octal 376.

The SIO Board is structured around a pair of Intel 8251 USART (Universal Synchronous-Asynchronous Receiver-Transmitter) devices.

The 8251 chips provide for extensive program control of the input/output functions including the RS232 Control Line and sync character selection in the Synchronous mode and error condition sense and recovery. The board provides interrupt generation for received characters, empty transmitter buffers, and sync characters detected with provision for jumper selecting the priority of the interrupt. The interrupt works in conjunction with the Priority Interrupt/ Clock board (PIC-8).

All functions may also be program controlled so that the full capability of the board is available to the machine without the use of interrupts. All RS232 level drivers and receivers necessary for two complete RS232 lines are included on the board.

Control lines included are DSR, DTR, RTS, CTS, and Carrier Detect. RS232 level drivers and receivers are also provided for receive and transmit clocks for use in Synchronous Mode. Jumper options permit the SIO board to be used either as the receiving (terminal) end of an RS232 line, or as the originating (computer) end.

Jumper options are available so that the two serial I/O ports may be used together so that the control lines are connected together on the two ports and the data lines are received and originated by the 8251 USARTS.

This configuration permits breaking an existing RS232 line and inserting the IMSAI 8080 System between the ends so that the control signals pass straight through and the IMSAI 8080 System intercepts, processes, and retransmits the data. This configuration is extremely useful where format adaptation or other changes must be made to data travelling on RS232 Systems.

Jumper-selectable baud rates are provided on the board for standard asynchronous and synchronous rates up to 9600 baud asynchronous and up to 38,400 baud synchronous. Other rates may be obtained through the use of the SIOC board which contains a jumper-programmable divider which mounts directly onto the SIO Board.

The two output connectors on the top of the board are designed to use the 3M flat cable system to connect directly to 25 pin EIA connectors so that no hand wiring is required to either receive or originate an RS232 line.

TTL and current loop serial input and output are connected to unused pins on the input/output connector. TTL levels are available on the connector for DTR, DATAIN, and DATAOUT, to provide maximum flexibility and utility. A current source is available on the connector for use with current loops. Current loop driving is done through opto-isolators for complete isolation of current loop lines.

Integrated circuit power regulation is provided with high quality tantalum and disc ceramic by-pass capacitors. The board is made on G10-type, 1/16 inch laminate with contact fingers gold-plated over nickel for reliable contact and long life. The remainder of the circuitry is tin-plated for good appearance and reliable solder connections.

Plated through-holes eliminate the need for any circuit jumpers. All jumper options are provided in 16 pin dual in-line package patterns so that jumpers may be installed on headers plugged into IC sockets for convenient and quick changing.

SIO THEORY OF OPERATION

To enable the SIO board, it must be properly addressed. In the I/O port addressed mode, address bits A4 through A7 are jumpered to the 74LS30 (8 input NAND) in C8. The status bits SINP and SOUT are NORed, this intermediate value inverted, and applied (via jumper on D6) to another of the NAND inputs. Remaining NAND inputs in this mode are jumpered (via D6) to a +5 volt level. Thus, when the selected address appears on A4-A7, and the MPU sends a SINP or SOUT pulse, the NAND output goes low and the board is enabled. See schematic.

In the memory-mapped I/O mode, the jumpering in socket C7 still selects an address. The high-order address is interpreted in another 8 input NAND (D8), and hard-wired to respond to the hex value FE. The jumper in socket D6 should be wired to put the inverted output of D8 into an input of C8, and the NORed output of the status bits SINP and SOUT directly connected to the (C8) NAND's input.

The +5 volt tie line jumper in D6 should not be connected for memory-mapped I/O. In this mode, when the corrected high and low order bits are on A4 through A15, and the MPU does not send a SINP or SOUT pulse, the board is enabled. See Diagram.

The SIO board has a bi-directional data bus on the board which connects to the 8251 chips and to the input and output portion of the SIO board control port. The bi-directional bus is connected to the DATA IN and DATA OUT busses on the IMSAI 8080 back plane through 8216 bi-directional bus driver chips. The board enable signal selects these bi-directional bus driving chips and the processor's data bus in signal (DBIN) is used to determine the direction of driving of the bi-directional chips.

8T97's are used to gate the control port data on the bi-directional data bus on the board. They are enabled by the DBIN strobe from the processor and address bit 3.

The 4 output bits of the control port on the SIO board are latched into the 74177 which is clocked by a combination of board enable and address bit 3 and the write strobe either from the processor or from the front panel.

The 8251 chips are selected by address bits 1 and 2, respectively, with address bit 0 determining whether the chip is in control or data mode. The read and write strobes are supplied to complete the control, enabling the chip to read data or write data onto the bi-directional data bus on the board.

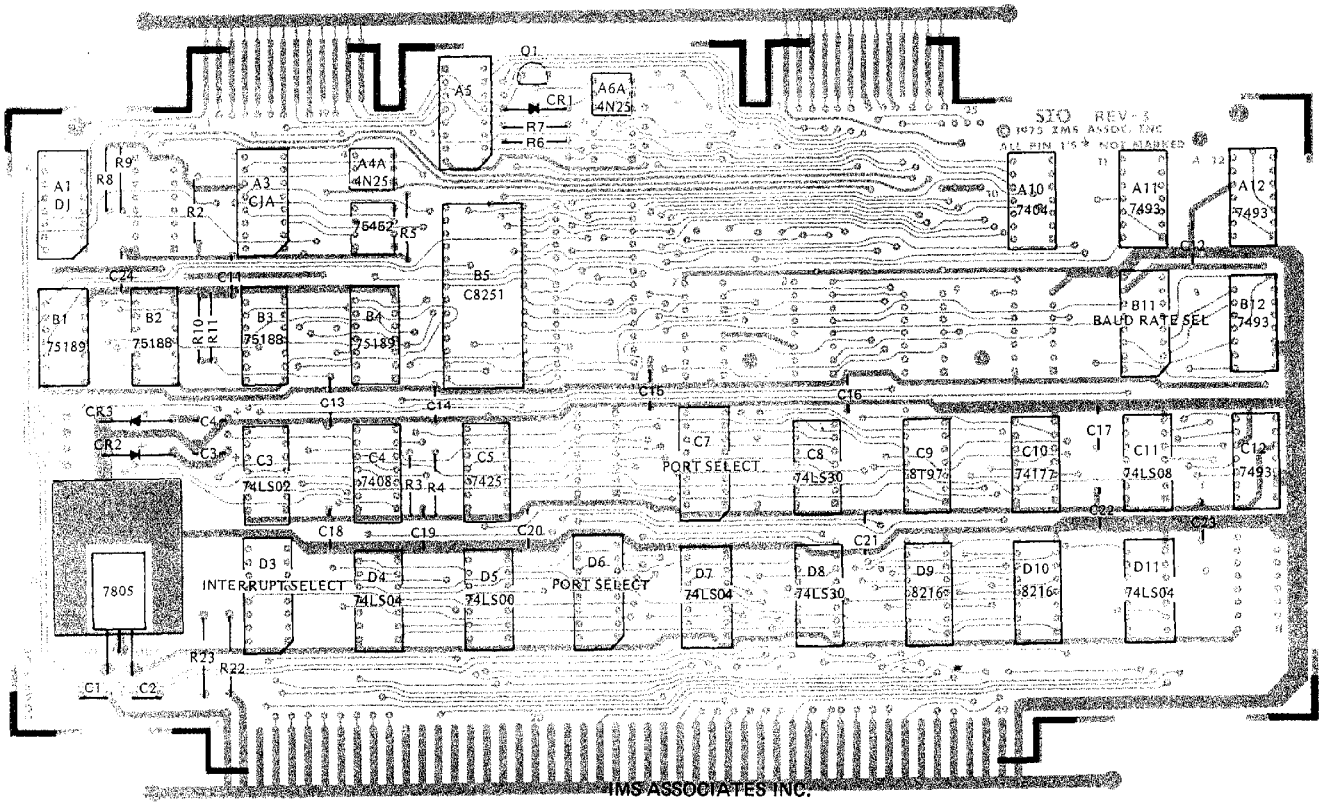
The four control lines desired for interrupt generation are ORed through 7425 and the resultant value supplied to an interrupt select jumper socket (D3). The 7425 OR gate may be disabled by two of the output port bits (IEA or IEB) when interrupts are not desired.

The two megacycle system clock phase II is divided to provide the standard baud rates for jumper selection to channel A and B. It is first divided by 13 through the use of a 7493 with external gating. This produces a rate extremely close to 16 times 9600 baud.

Further division of two are made by 7493's to provide most of the other standard baud rates. 110 baud for a standard teletype is achieved by a divide by 11 from the 2400 baud line which is then divided by 2 to create a symmetrical output and supplied to the jumper socket for 110 baud.

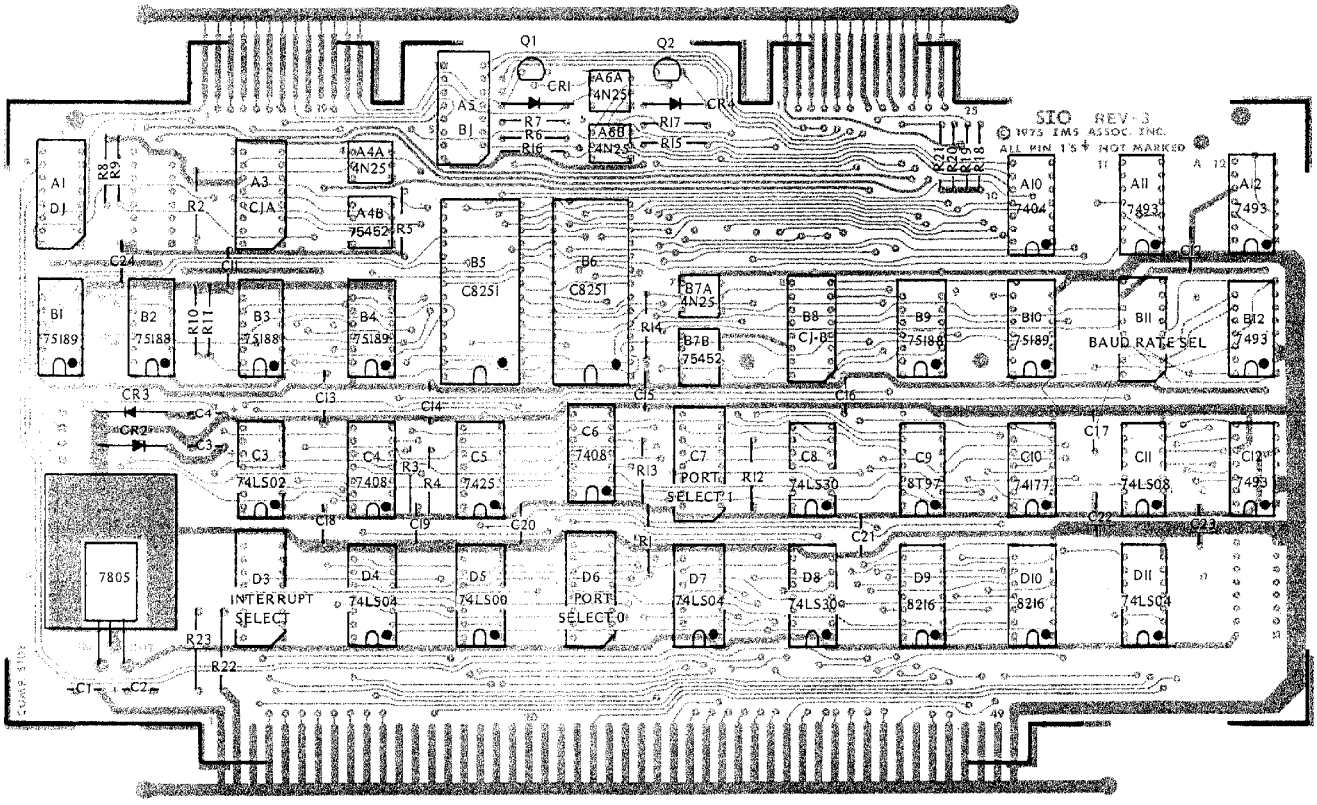
The phase II clock, +5 volts and ground are also supplied to the data rate select socket for use by the SIOC board which connects to the SIO board through the data rate select socket (B11) to provide a jumper-selectable baud rate generator for special rates.

The data and control outputs of the 8251 chips are driven or received through 1488 or 1489 TTL to RS232 level converters as appropriate to the functions. The TTL levels for data and control are driven through open-collector peripheral drivers and a 220 ohm pull-up to +5 volts. The current loop input and output are driven through opto-isolators and are designed to work adequately with either 20 or 60 miliampere current loops.



IMS ASSOCIATES INC.
ASSEMBLY DIAGRAM
SIO 2-1 REV 3 2/76

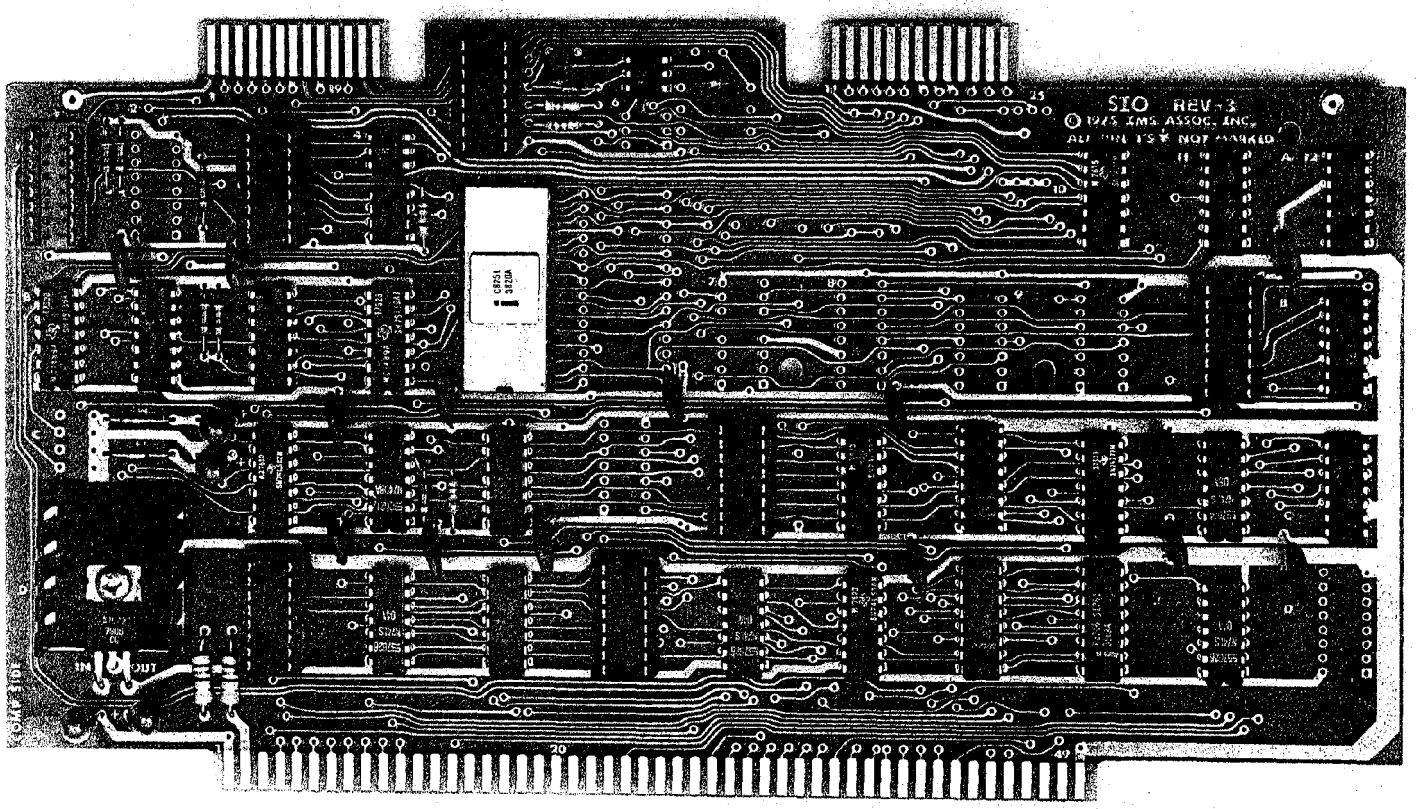
5/18/76



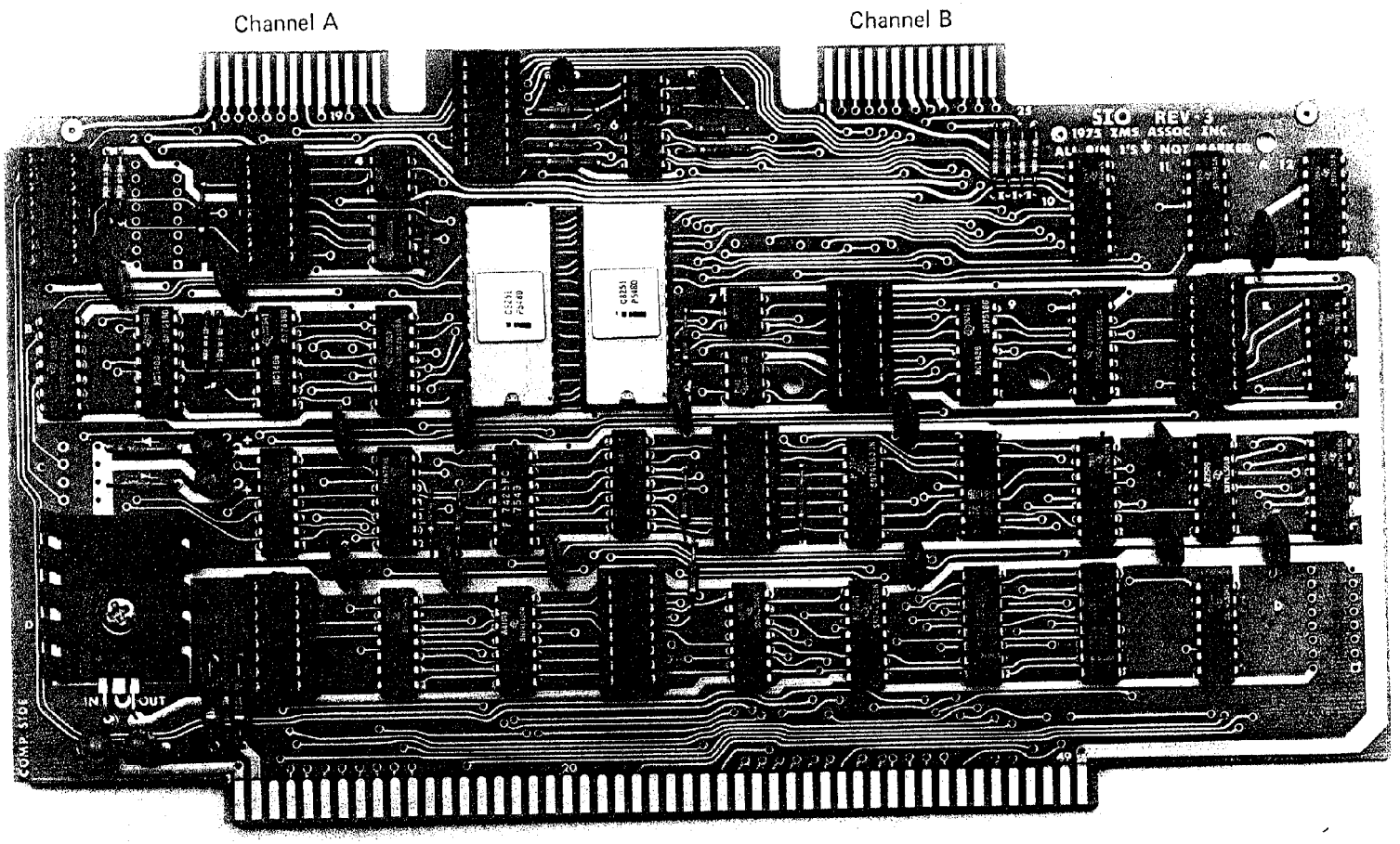
IMS Associates Inc.

ASSEMBLY DIAGRAM

SIO 2-2 REV 3 2/76



SIO 2–1 REV 3



SIO 2-2 REV. 3

BOARD: SIO 2

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Solder	15-0000001	5'	
Heat Sink	16-0100002	1	Thermalloy/6106B-14
Screw	20-3402001	1	6-32x3/8" Phillips Pan Head Machine
Nut	21-3120001	1	6-32 Hex Nut
Lockwasher	21-3350001	1	#6 Internal Star Lockwasher
Header	23-0400001	7	16 Pin IC Header
Socket	23-0800001	7	16 Pin Solder Tail Socket
Socket	23-0800003	1	28 Pin Solder Tail Socket
Resistor	30-2560462	2	56 Ohm, ½ Watt/green. blue, black
Resistor	30-3220362	3	220 Ohm, ¼ Watt/red, red, brown
Resistor	30-3470362	4	470 Ohm, ¼ Watt/yellow, violet, brown
Resistor	30-4100362	4	1K Ohm, ¼ Watt/brown, black, red
Resistor	30-4470362	1	4.7K Ohm, ¼ Watt/yellow, violet, red
Capacitor	32-2010010	14	.1uF Disk Ceramic
Capacitor	32-2233070	4	33-25 Tantalum Capacitor (or 22-25)
Diode	35-1000006	1	1N914 Zener Diode
Diode	35-1000009	2	1N4742 Zener Diode
Transistor	35-2000002	1	2N3904 Transistor
Isolator	36-0042501	1	Opto Isolator/4N25
8T97	36-0089701	1	Hex Tri-State Buffer/N8T97B
74LS00	36-074002	1	Quad 2 Input NAND(Low Power Schottky)/ SN74LS00N
74LS02	36-0740202	1	Quad 2 Input NOR (LPS)/SN74LS02N

SIO 2-1 Rev. 3
Parts List

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
7404	36-0740401	1	Hex Inverter/SN7404N
74LS04	36-0740402	3	Hex Inverter (LPS)/SN74LS04A
7408	36-0740801	1	Quad 2 Input AND/SN7408N
74LS08	36-0740802	1	Quad 2 Input AND (LPS)/SN74LS08N
7425	36-0742501	1	Dual 4 Input NOR with Strobe/SN7425N
74LS30	36-0743002	2	8 Input NAND (LPS)/SN74LS30N
7493	36-0749301	4	4 Bit Binary Counter/SN7493N
7805	36-0780501	1	5V Positive Voltage Regulator/MC7805CP
8216	36-0821601	2	Bi-Directional Bus Driver/D8216/S1261
8251	36-0825101	1	Programmable Comminication Interface/ C8251
74177	36-7417701	1	4 Bit Binary Counter, 35MHz/SN74177N
75188	36-7518801	2	RD 232 Driver/SN74188
74189	36-7418901	2	RS 232 Receiver/SN75189A
75452	36-7545201	1	Dual Peripheral Driver/SN75452BD
PC Board	92-0000018	1	SIO Rev. 3

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Solder	15-0000001	5'	
Heat Sink	16-0100002	1	Thermalloy /6106B-14
Screw	20-3402001	1	6-32x3/8" Phillips Pan Head Machine
Nut	21-3120001	1	6-32 Hex Nut
Lockwasher	21-3350001	1	#6 Internal Star Lockwasher
Header	23-0400001	8	16 Pin IC Header
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Socket	23-0800003	2	28 Pin Solder Tail Socket
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Resistor	30-4100362	7	1K Ohm, ¼ Watt/brown, black, red
Resistor	30-4470362	2	4.7K Ohm, ¼ Watt/yellow, violet, red
Capacitor	32-2010010	14	.1uF Disk Ceramic
Capacitor	32-2233070	4	33-25 Tantalum Capacitor (or 22-25)
Diode	35-1000006	2	1N914 Zener Diode
Diode	35-1000009	2	1N4742 Zener Diode
Transistor	35-2000002	2	2N3904 Transistor
Isolator	36-0042501	4	Opto Isolator/4N25
8T97	36-0089701	1	Hex Tri-State Buffer/N8T97B
74LS00	36-0740002	1	Quad 2 Input NAND (Low Power Schottky)/ SN74LS00N
74LS02	36-0740202	1	Quad 2 Input NOR (LPS)/SN74LS02N

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74LS04	36-0740402	3	Hex Inverter (LPS)/SN74LS04A
7408	36-0740801	2	Quad 2 Input AND/SN7408N
74LS08	36-0740802	1	Quad 2 Input AND (LPS)/SN74LS08N
7425	36-0742501	1	Dual 4 Input NOR with Strobe/SN7425N
74LS30	36-0743002	2	8 Input NAND (LPS)/SN74LS30N
7493	36-0749301	4	4 Bit Binary Counter/SN7493N
7805	36-0780501	1	5V Positive Voltage Regulator/MC7805CP
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Resistor	30-4470362	1	4.7K Ohm, ¼ Watt/yellow, violet, red
Socket	23-0800001	1	16 Pin Solder Tail Socket
Socket	23-0800003	1	28 Pin Solder Tail Socket
Solder	15-0000001	5'	

SIO Assembly Instructions

1) Unpack your board and check all parts against the parts list enclosed in the package.

2) If gold contacts on the edge connector appear to be corroded, use pencil eraser to remove any oxidation. NOTE: Do not use Scotchbright or any abrasive material as it will remove the gold plating.

RESISTOR INSTALLATION

3) Insert and solder the two 56 ohm ½ watt resistors (green/blue/black) at locations R22 and R23 as shown on the Assembly Diagram.

4) Insert and solder the six 220 ohm ¼ watt resistors (red/red/brown) at locations R4 through R6, R12, R15, and R16 as shown on the Assembly Diagram for SIO 2-2; or the three 220 ohm ¼ watt resistors (red/red/brown) R4 through R6 for SIO 2-1.

5) Insert and solder the eight 470 ohm ¼ watt resistors (yellow/violet/brown) at locations R8 through R11 and R18 through R21 for SIO 2-2; the four 470 ohm ¼ watt resistors (yellow/violet/brown) at locations R8 through R11 for SIO 2-1 as shown on the Assembly Diagrams.

6) Insert and solder the 1K ohm ¼ watt resistors (brown/black/red at locations R1 through R3, R13, and R14 for SIO 2-2; the 4 1K ohm ¼ watt resistors R2, R3, R13 and R14 for SIO 2-1 as shown on the Assembly Diagrams. The remaining two 1K ohm resistors for the SIO 2-2 board are used as jumper selects on A3 and B8. See User Guide section.

7) Insert and solder the two 4.7K ohm ¼ watt resistors (yellow/violet/red) at locations R7 and R17 shown on the SIO 2-2 Assembly Diagram; one 4.7K ohm ¼ watt resistor at location R7 as shown on the SIO 2-1 Assembly Diagram.

IC INSTALLATION

All Pin 1's are toward the lower right hand edge of the PC board and the 100 pin connector.

8) Insert and solder the one 74LS00 at location D5.

9) Insert and solder the one 74LS00 at locaiton D5.

10) Insert and solder the one 74LS02 at location C3.

11) Insert and solder the one 7404 at location A10.

12) Insert and solder the three 74LS04's at locations D4, D7, and D11.

13) Insert and solder the two 7408's at locations C4 and C6 on SIO 2-2; or the one 7408 at location C4 on SIO 2-1.

14) Insert and solder the one 74LS08 at location C11.

15) Insert and solder the one 7425 at location C5.

16) Insert and solder the two 74LS20's at locations C3 and D8.

17) Insert and solder the four 7493's at locations A11, A12, B12, and C12.

18) Insert and solder the one 74177 at location C9.

19) Insert and solder the three 75188's at locations B2, B3, and B9 on SIO 2-2; or the two 75188's at locations B2 and B3 on SIO 2-1.

20) Insert and solder the three 75189's at locations B1, B4, and B10 on SIO 2-2; or the two 75189's at locations B1 and B4.

21) Insert and solder the two 75452's at locations A4B and B7B on SIO 2-2; or the one 75452's at location A4B on SIO 2-1.

22) Insert and solder the two 8216's at locations D9 and D10.

23) Insert and solder the two 28 pin solder tail sockets at locations B5 and B6 on SIO 2-2; or the one 28 pin solder tail socket at location B5.

24) Insert and solder the four 4N25's at locations A4A, A6A, A6B, and B7A for SIO 2-2; or the two 4N25's at locations A4A and A6A for SIO 2-1.

25) Insert the one 8T97 at location C9.

DISCRETE COMPONENT INSTALLATION

26) Insert and solder the fourteen .1 uf disk capacitors at locations C11 through C24 as shown on the Assembly Diagram.

27) Insert and solder the four 33 uf tantalum capacitors at locations C1 through C4 as shown on the Assembly Diagram. NOTE: Observe polarity (+ to +) as shown on the board.

28) Insert and solder the two 1N914 zener diodes at locations CR1 and CR4 as shown on the Assembly Diagram.

29) Insert and solder the two 1N742 zener diodes at locations CR2 and CR3 as shown on the Assembly Diagram.

30) Insert and solder the two 2N3904 transistors at locations Q1 and Q2 as shown on the Assembly Diagram for SIO 2-2; or the one 2N3904 transistor at location Q1 as shown on the Assembly Diagram for SIO 2-1.

31) Insert and solder the eight 16 pin sockets at locations A1, A3, A5, B8, B11, D3, and D6 for SIO 2-2; or the seven 16 pin sockets at locations A1, A3, A5, B11, D3, and D6 for SIO 2-1 as shown on the Assembly Diagram.

REGULATOR AND HEAT SINK INSTALLATION

32) Before installing the heat sink and regulator, bend the 7805 regulator leads at 90 degree angles to facilitate mounting of the heat sink.

33) Insert the #6 screw through the 7805 regulator and heat sink on the component side of the board and attach through the lockwasher and nut on the circuit side of the board. Tighten the screw carefully to insure proper alignment of the heat sink to prevent shorting to adjacent traces Solder in the 7805 leads.

34) Finally, the 8251 chips should be inserted in their sockets with Pin 1 down toward the 100 pin edge connector at the bottom of the board. Addressing and baud rate jumpers should be installed and other option jumpers installed as required. The board is ready for use.

USER GUIDE

The IMSAI SIO Board provides 2 independent channels of serial data input and output. Utilizing the Intel 8251 USART devices, the SIO Board provides 2 channels of RS232, TTL, and current loop data lines with complete control signals.

The SIO Board also includes all logic necessary to control the 8251 devices from the IMSAI 8080 Back Plane.

For reference information on the programming and operation of the 8251 chip, the user should refer to the Intel 8080 Microcomputer Systems User's Manual.

The User's Guide is intended to cover the information beyond that contained in the Intel Data Book necessary to make full use of the SIO board.

Both the memory-mapped and jumper-wired I/O configurations use the lower 4 bits of the address bytes (A1 through A3) to select and control the board's functions. Bit 4 through 7 of the board address (A4 - A7) are jumper-selected as described on another page. If the board is jumper-selected to run as an input and output port type board, then A0 - A7 form a complete address. If the board is jumper-selected to respond to memory-mapped I/O, then A0 - A7 form the lower byte of address and the upper byte of address is hex FF or octal 376.

Address bits 1 and 2 select serial I/O channel A or channel B respectively. That is, when address bit 1 (A1) is high, serial I/O channel A is enabled. When address bit 2 (A2) is on, serial I/O channel B is enabled.

Address bit 0 determines whether the I/O channel selected will respond to the current byte as a control byte or a data byte. If address bit 0 is a 1, the control functions are selected, and if address bit 0 is a 0, the byte is assumed to be data. Thus, to write a control byte into serial I/O channel A, the lower 4 bits of address would normally contain hex 3 or octal 03, while the normal address

SIO BOARD ADDRESSING

Address Bit	Function	
0	C/$\overline{D}$ on 8251's	1 = CONTROL 0 = DATA
1	SELECT CHANNEL A	1 = SELECT
2	SELECT CHANNEL B	1 = SELECT
3	SELECT CONTROL I/O	1 = SELECT
4		
5	CARD ADDRESS	
6	Jumperable to any one of 16 addresses	
7		

This byte is I/O port address to run SIO card from INP & OUT instructions.

If SIO card is to be run from memory reference instructions (memory mapped I/O), the above byte is the low order address byte; the high order address byte is FE_{hex} (376_{octal}) (1111 1110 binary)

SIO CONTROL I/O BIT DEFINITIONS

Bit	Input Byte	Output Byte
0	always 1	Interrupt Enable chan. A
1	always 1	Carrier Detect chan. A
2	Carrier Detect chan. A	non - functional
3	Clear To Send chan. A	non - functional
4	always 1	Interrupt Enable chan. B
5	always 1	Carrier Detect chan B
6	Carrier Detect chan. B	non - functional
7	Clear To Send chan. B	non - functional

Carrier detects need option jumper to select originate/receive

Interrupts occur on TxRDY, TxEMTY, RxRDY, and SYNDET

TxRDY and RxRDY interrupts are removed if the respective functions (transmit and receive) are disabled by software command byte. TxEMTY interrupt is removed only by filling transmit buffer with a byte. This may be done while the transmit function is disabled .if desie

for channel B control bytes would be hex 5 or octal 05. Address bit 3 (A3) selects the board control I/O port. When address bit 3 (A3) is high, the control port will be enabled. Thus, when use is being made of the control port, the lower 4 bits of address would normally be hex 8 or octal 10.

The control I/O byte selected by address bit 3 is divided into the upper 4 bits and the lower 4 bits. The lower 4 bits, 0 through 3, serve the channel A serial I/O circuit. The upper four bits, 4 through 7, serve the second I/O channel B functions. Bits 0 and 4, for channel A and B respectively, control the interrupt enable separately for each channel. When this bit is a 1, the interrupts are enabled and the processor will receive and interrupt whenever any one of the following 4 lines are active: the transmitter ready line, the transmitter empty line, the receiver ready line, and the sync detect line.

If bits 0 or 4 (as appropriate to channel A or B) are made 0, then no interrupts will be generated from the affected channel. Bits 1 and 5 serve channel A and B, respectively, to output the carrier detect signal. This is operative only when the jumper in jumper socket BJ has selected the board to act as the originator of the carrier detect line.

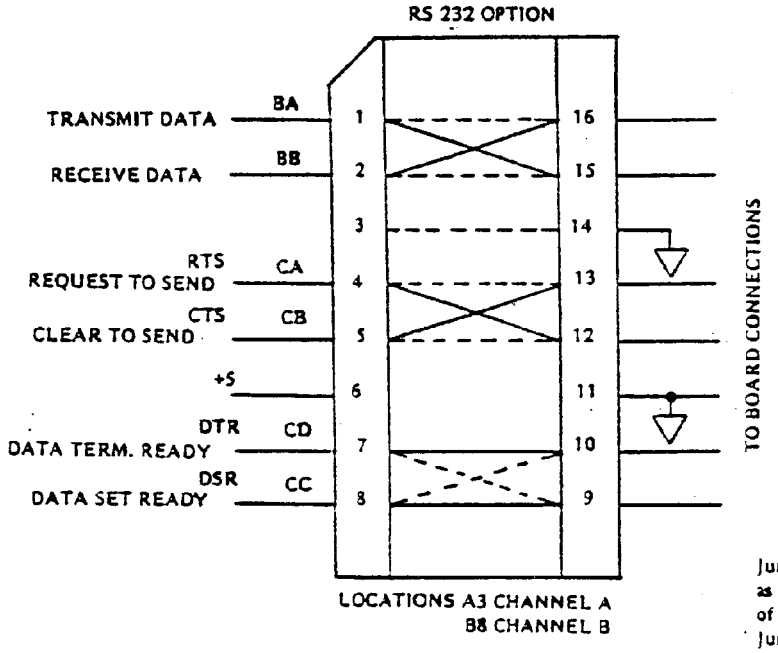
Bits 2, 3, and 6, and 7 are not functional in the output mode for the SIO control byte. When an input is read from the SIO control byte, bits 0, 1, 4 and 5 are not functional. These 4 bits will always be read as a 1.

Bits 2 and 6 read the condition of the carrier detect receiver for channels A and B, respectively. The signal is operative only when jumper socket BJ is jumpered to read the condition of the carrier detect line.

Bits 3 and 7 serve channel A and B, respectively, to read the condition of the clear-to-send (CTS) control signal. This is provided because it is not possible to read the condition of CTS through programmed input from the 8251.

SIO BOARD I/O PIN DEFINITIONS

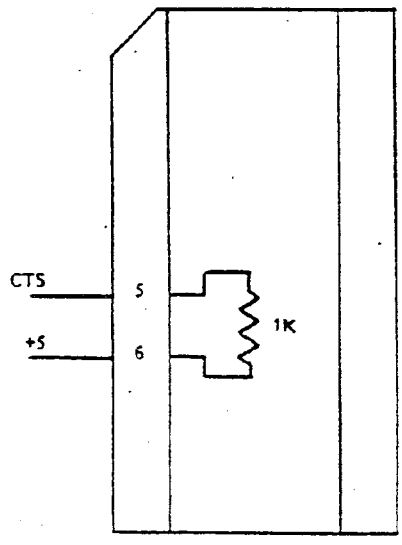
EIA 25 pin connector	26 pin edge connector	RS232 LEVELS	TTL LEVELS	CURRENT LOOP
1	1	AA chassis ground		
2	3	BA Trans. Data		
3	5	BB Rec. Data		
4	7	CA Req. to Send		
5	9	CB Clr. to Send		
6	11	CC Data Set Rdy.		
7	13	AB signal ground		
8	15	CF Carrier Det.		
9	17	+ V		+ V + Current Source
10	19			
11	21			In Loop +
12	23			Out Loop +
13	25			Out Loop −
14	2		$\overline{\text{Data Term. Rdy.}}$	
15	4	DB Trans. Clk.		
16	6		$\overline{\text{Data Set Rdy.}}$	
17	8	DD Rec. Clk.		
18	10		$\overline{\text{Data Out}}$	
19	12		$\overline{\text{Data In}}$	
20	14	CD Data Term. Rdy.		
21	16			Current sink 1
22	18			
23	20			Current sink 2
24	22			
25	24			In Loop −



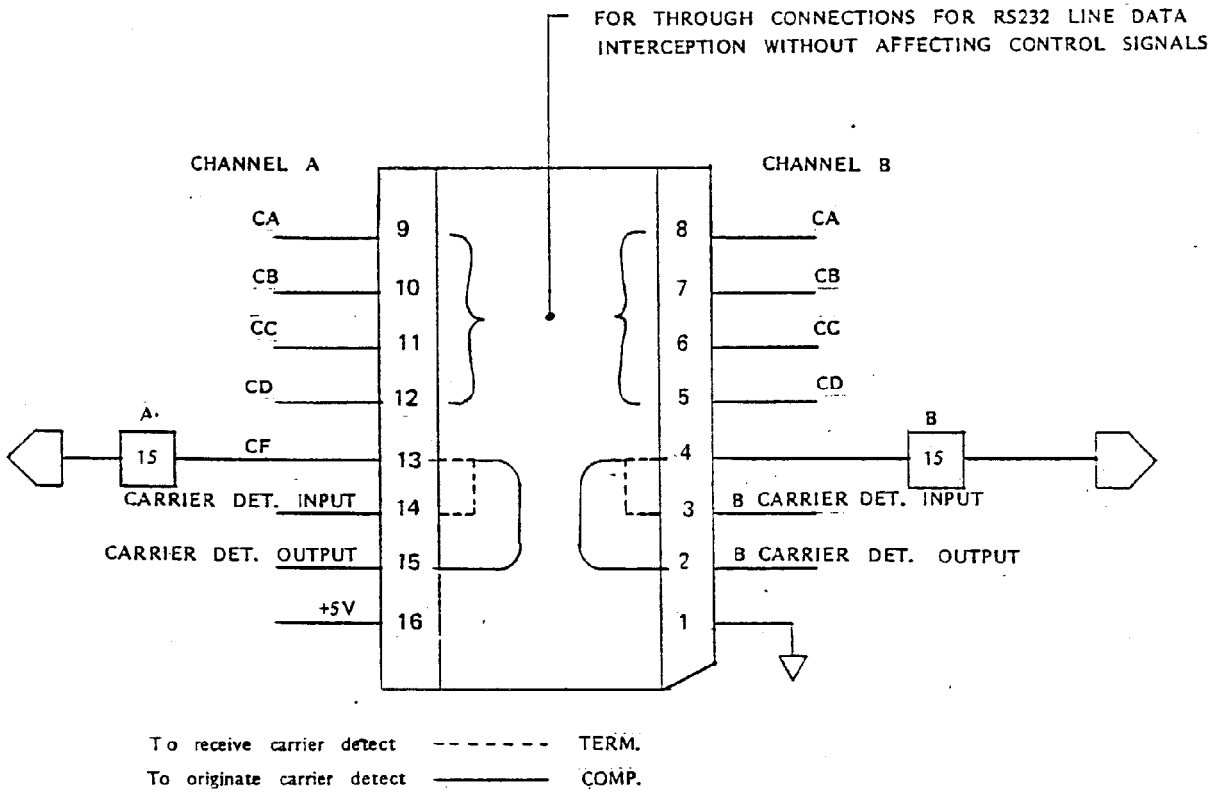
Jumpers shown for connection as terminal or computer end of an RS232 line.
Jumper connection 3 to 14 is always to be made.

TERMINAL ——

COMPUTER ——

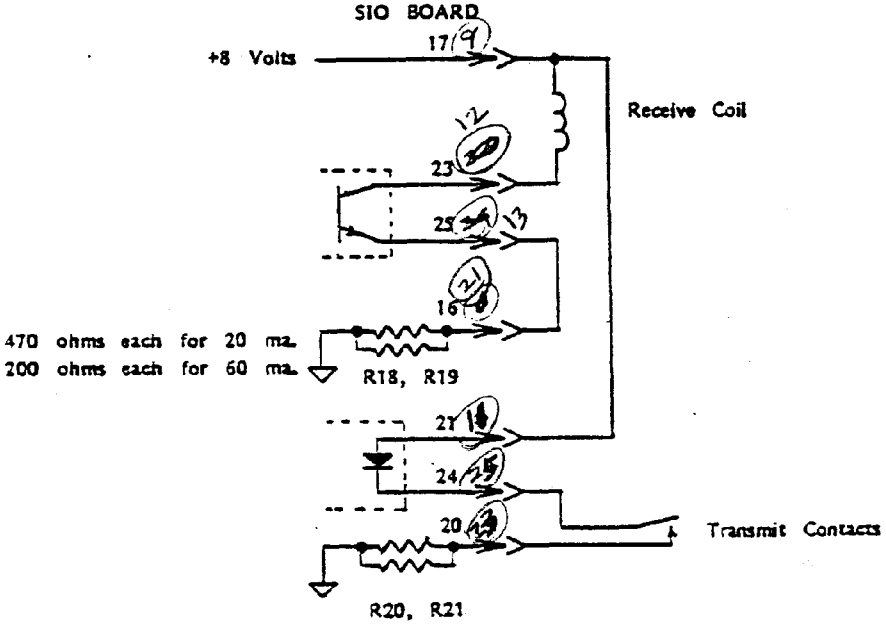


SIO RS232 INTERCHANNEL CONTROL JUMPERS and CARRIER DETECT

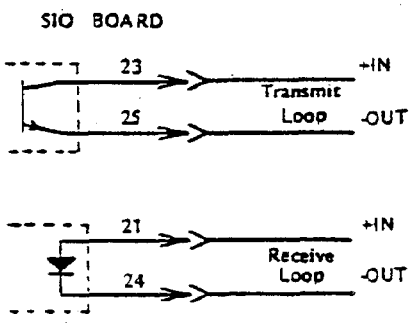


CURRENT LOOP CONNECTIONS

WITH CURRENT SOURCE



WITHOUT CURRENT SOURCE



The TTL output levels are driven by a 75452 dual peripheral driver, with open collector outputs, and a 220 ohm pull-up to +5 volts. The TTL data inputs drive 1TTL input load and a 1K pull-up to +5 volts.

When the TTL inputs are not being used, they should be left open or held high so as not to affect data input from other sources.

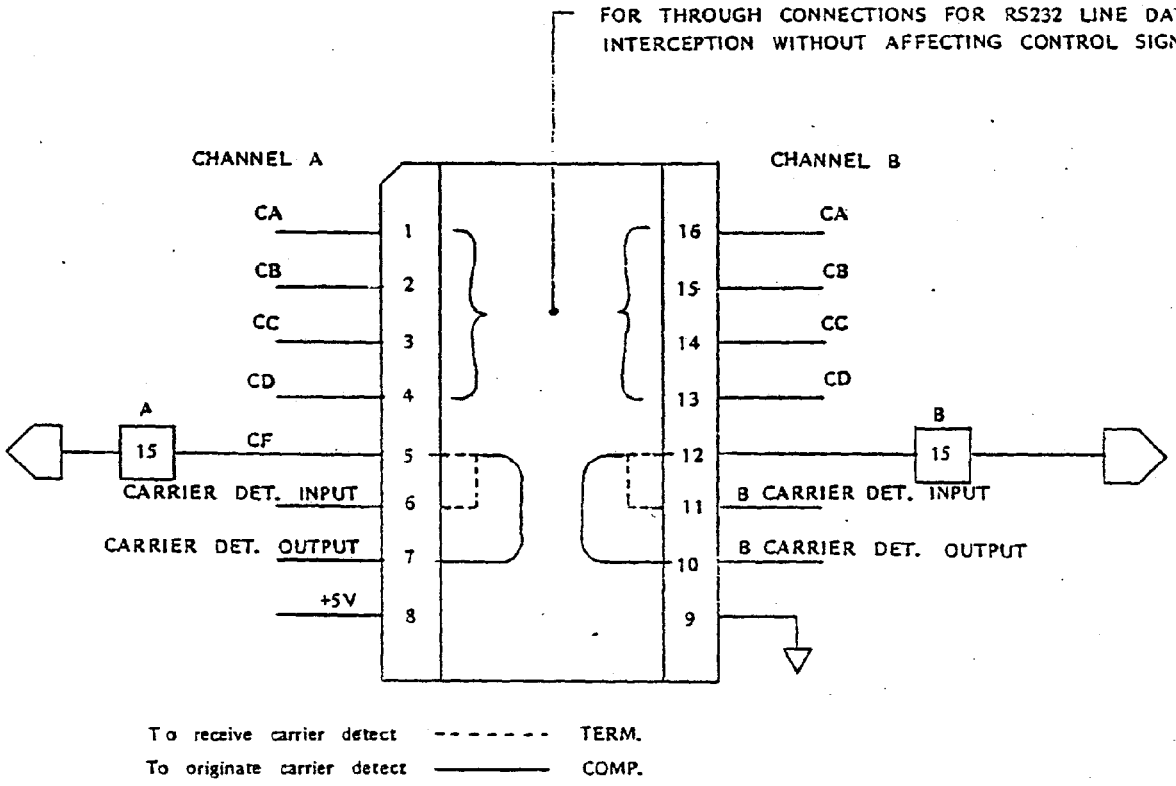
The TTL Data Input line must be left open and not held high when the current loop inputs are used. The current loop input drives opto-isolators and will respond to either 20 or 30 milliamperes. In applications where a significant reverse voltage may be experienced, such as when inductive circuits (i.e., relays) are coupled to the data line, a protective diode should be put across the line such that any reverse voltage spikes will cause the diode to conduct and thus protect the LED in the opto-isolator from too large a reverse voltage.

The current loop output is switched by an isolated transistor through an opto-isolator and is provided with a transient-shunting diode across the output transistor so that it may be used to drive relays without risk of damage to the output circuit. Typical wiring connections are diagramed on another page, both with and without the current source being used.

Setting the baud rate for serial I/O channels A and B is done on the jumper select socket RJ in position B11. The baud rates designated on the detailed sheet for rate select are correct when the 8251 is programmed for a 16X asynchronous clock rate and a 1X synchronous clock rate.

The details of selecting the desired baud rates are located on the schematic.

SIO RS232 INTERCHANNEL CONTROL JUMPERS and CARRIER DETECT



Jumper CJ-A or CJ-B

The jumper selection socket in A3 serves serial I/O channel A and the jumper selection socket in B8 serves serial I/O circuit B. Their functions are the same for their respective channels. The function of this jumper socket is to permit the serial I/O port RS232 levels to be wired so as to either serve as the terminal end of a 232 line or the computer end of a 232 line with no special cable wiring required off the Serial I/O board.

With pins 1, 2, 4, 5, 7 and 8 wired directly across the jumper socket as shown in the diagram for the terminal end, the function of the lines correspond one to one with the names of the RS232 control lines referred to in the 8251 specifications.

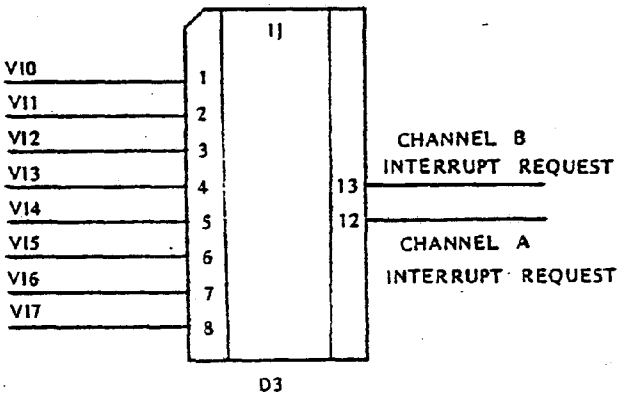
The inputs and outputs are arranged as appropriate for the SIO board to serve as the terminal end of an RS232 line. Should it be desired for the SIO board to serve as the computer end of a standard RS232 line, use jumpers connected as shown in the diagram. The 3 pairs of lines are reversed so that TRANSMIT DATA is now driving what is received data for the terminal and RECEIVE DATA is receiving what is transmit data from the terminal, and similarly, REQUEST TO SEND and CLEAR TO SEND are reversed and DATA SET READY and DATA TERMINAL READY are reversed.

Ground and +5 volts are available on the socket for providing permanent mark or space levels to any of the control lines if CLEAR TO SEND is not driven by an external source. It should be wired to pin 6 to provide a constant enable for the transmitter section of the USART.

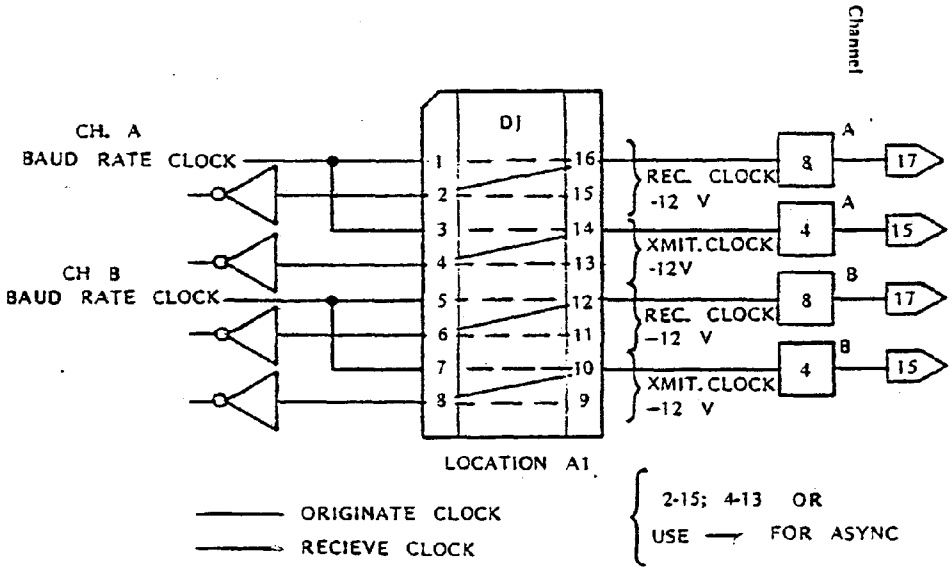
Jumper Socket BJ

Socket BJ serves both to determine whether CARRIER DETECT is being originated or received by the SIO board. It is also used to jumper the control lines between channel A and channel B for applications where the control lines are desired to be passed through and data intercepted and

SIO INTERRUPT SELECT SOCKET



SIO 232 CLOCKS JUMPER OPTIONS



Program 8251 for x16 for asynchronous operation,
x1 for synchronous.

handled. The four primary control lines for both channel A and channel B appear in this jumper socket, and can be jumper-wired straight across as desired.

It should be remembered that only one source should be driving an RS232 line at a time. If the control lines are jumpered straight across so that the modem and data terminal are driving the lines, then appropriate jumpers in jumper socket locations A3 or B8 should be removed so that the SIO board will not be attempting to drive these lines at the same time. If it is desired to detect the DATA TERMINAL READY line, then a jumper needs to be placed as shown between pins 5 and 6 for channel A, or between pins 11 and 12 for channel B.

If it is desired to originate the CARRIER DETECT line, a jumper should be placed instead between pins 5 and 7 for channel A, for 10 and 12 for channel B.

Ground and +5 volts are available in this jumper socket for providing a permanent mark or space level to any of these control lines.

The interrupt line from channel A and channel B both appear on the interrupt select socket in position D3. All 8 of the IMSAI 8080 system priority interrupt lines on the back plane, also appear on the interrupt select socket. A jumper may be placed between the appropriate channel's interrupt line and any one of the priority interrupt system lines to provide an interrupt of the desired priority.

Jumper Location DJ, Located in A1

The jumper select socket in A1 provides facilities for originating and receiving clock signals for receive or transmit for use in the synchronous mode of communication. One-half of the socket controls lines for Channel A and the other half is dedicated to Channel B. Pins 1, 2, 3, 4, and 13, 14, 15 and 16 serve the channel A jumper functions. The remainder of the pins have the identical function for Channel B.

When it is desired to originate the clock signal the pins for that channel should be jumpered straight across, as shown in the diagram, so that the clock signal from the SIO board is driven through converters to RS232 levels onto the DD and DB lines.

The inputs to the data clock receive circuits are tied to -12 volts to provide an inactive output to the OR-gate supplying the receive clock to the USART chip.

When it is desired instead to receive the clock from the RS232 cable, then these jumpers are removed and the RS232 lines DD and DB are jumpered to the input of the clock-receive circuits as shown in the diagram.

When this is done, the data rate select socket for the appropriate channel must be jumpered so that the clock line from this jumper select socket is held at ground or low in order to avoid interference between the onboard clock circuit and the incoming clock from the RS232 line.

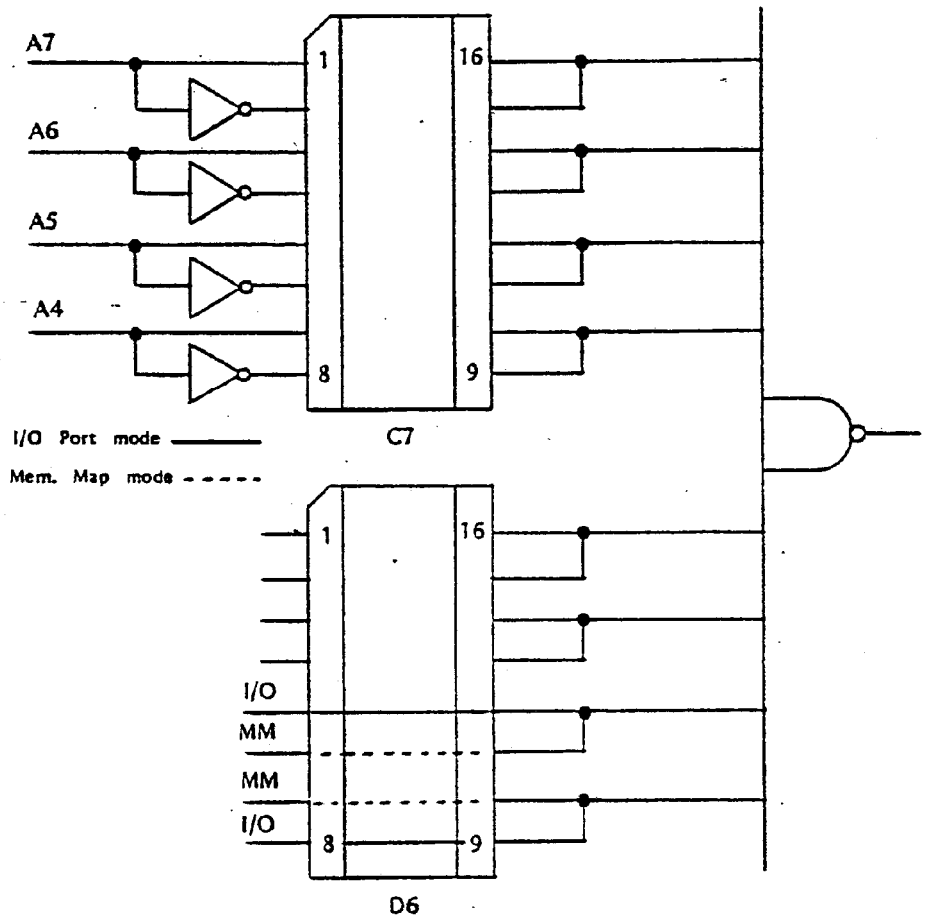
Data Rate Select Socket

The jumper socket in position B11 provides for selecting different baud rates for both Channel A and Channel B from the set of standard rates provided by the SIO board. The pin numbers and baud rates are indicated in the diagram.

The clock lines for Channel A and Channel B are completely independent and may be jumpered to the same rate or different rates.

When the chip is being used in the synchronous mode, the chip is running at a 1X clock rate rather than 16 X rate as in the asynchronous mode. Thus, the baud rates are 16 times as great for the same jumper location when used in the synchronous mode.

Board Address Selection Jumper Sockets



The board address is selected by jumpers or a DIP switch in locations C7 and D6. There are two cases for which this board may be jumpered: 1) to respond to input/output instructions and 2) to respond to memory access instructions. The case of input/output instructions will be treated first.

In selection location D6 pins 8 and 9 must be jumpered together and pins 5 and 12 must be jumpered together. The user must jumper socket C7 so when the desired I/O Port Address appears on the Address lines, the inputs to the NAND gate from bits A4 through A7 are high. If, for instance, address bit 6 is desired to be a 0 when the board responds, then pins 4 and 13 would be jumpered together. If address bit A6 was desired to be a 1, then

either pins 3 and 14 may be jumpered together or 3 and 13 may be jumpered together, since 13 and 14 are tied to the common address selection input.

It is suggested, however, that when jumpers are being used, pins 3 and 13 be connected together to provide an easy visual indication of whether the address bit is a 1 or a 0. since that will correspond to whether the jumpers are slanted or straight across the jumper socket. Pins 13 and 14 were tied together so that an 8 position DIP switch can be inserted in this location and used to select the address. Address bits 4, 5, and 7 are jumpered in a similar manner on position C7.

See the diagram on the previous page for pin numbers for each address bit.

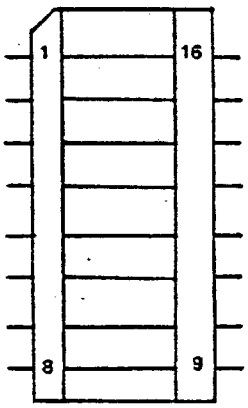
If it is desired to use the board in a memory-mapped I/O capacity, then in position D6 the jumpers between pins 8 and 9 and 5 and 12 must be removed and two jumpers inserted between pins 7 and 10 and between 6 and 11. The remaining jumpers for bits 4 through 7 function exactly the same and affect the lower eight bits of the memory address. The upper eight bits of the address will always be all ones, that is hex FE or octal 376.

When used as a memory-mapped I/O board, all instructions that normally affect the memory will operate on the I/O ports. For example, an increment memory instruction would read the data from the addressed input port, increment that data by one and output it on the same address output port.

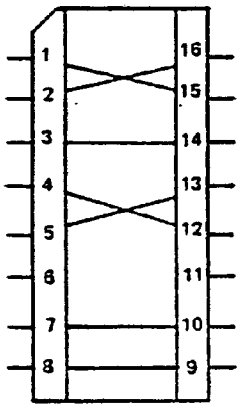
Example Jumpers -

To use the SIO Board in its simplest form, non-interrupted input/output instruction controlled, create jumpers as shown.

A1

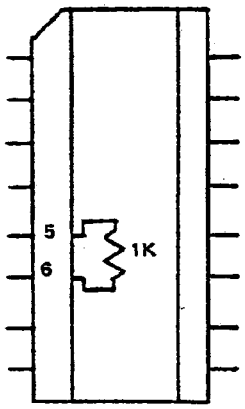


RS232 or Current Loop



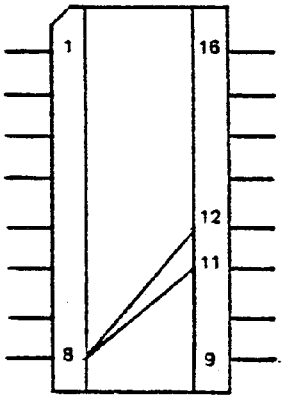
RS232

A3 (B8)

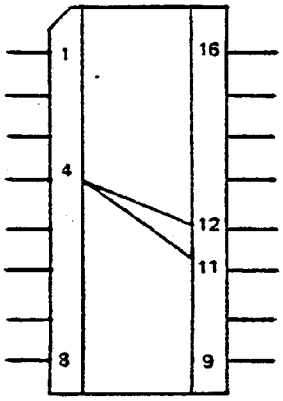


Current Loop

B11

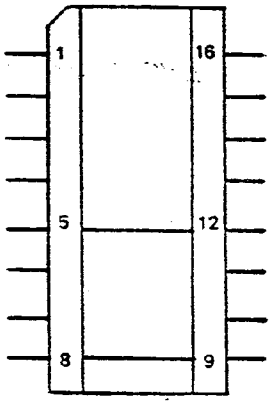


110 BAUD

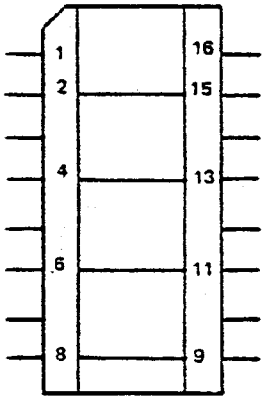


1200 BAUD

D6



C7



Select appropriate address-
Shown is 0- as required by SCS

Sample sequence to set up SIO for teletype and echo from keyboard to printer:

Format used is 2 stop bits, no parity, and 7 data bits. Reset IMSAI 8080 before running. Address and constants are in hexadecimal.

```
LIST
0010      MVI A,0CAH          MODE BYTE
0020      OUT 03
0030      MVI A,27H           COMMAND BYTE
0040      OUT 03
0050 LOOP IN 03               READ CHAN A STATUS
0060       ANI 02             MASK OUT ALL BUT RECEIVER READY
0070       JZ LOOP            IF NOT READY LOOP
0080       IN 02              READ CHAR
0090       OUT 02             WRITE CHAR
0100       JMP LOOP
```

```
ASSM 3700

3700 3E CA       0010      MVI A,0CAH          MODE BYTE
3702 D3 03       0020      OUT 03
3704 3E 27       0030      MVI A,27H           COMMAND BYTE
3706 D3 03       0040      OUT 03
3708 DB 03       0050 LOOP IN 03               READ CHAN A STATUS
370A E6 02       0060       ANI 02             MASK OUT ALL BUT RECEIV
370C CA 08 37    0070       JZ LOOP            IF NOT READY LOOP
370F DB 02       0080       IN 02              READ CHAR
3711 D3 02       0090       OUT 02             WRITE CHAR
3713 C3 08 37    0100       JMP LOOP
```

IMSAI

SIOC

SIOC BOARD

FUNCTIONAL DESCRIPTION

The IMSAI SIOC Board is a small optional board used with the Serial Interface (SIO Board). The SIOC provides user selection of any USART clock frequency from 15 Hz to 56 KHz.

The generated clock frequency is determined by a binary value set in two 16-pin jumper sockets. An additional jumper socket allows selection of either the SIOC or the standard SIO USART clocks to channels A and/or B.

Physically, the SIOC Board measures 5.2 X 2.2", and piggy-back mounts to a standard SIO Board. Mounting hardware and decoupling capacitors are provided with the SIOC Board.

SIOC BOARD

THEORY OF OPERATION

The SIOC board is a modulo -N clock divider, where N is user selectable. The SIOC divides down the 2MHz 8080 $\emptyset_2$ clock to a rate appropriate for the 8251 USART devices.

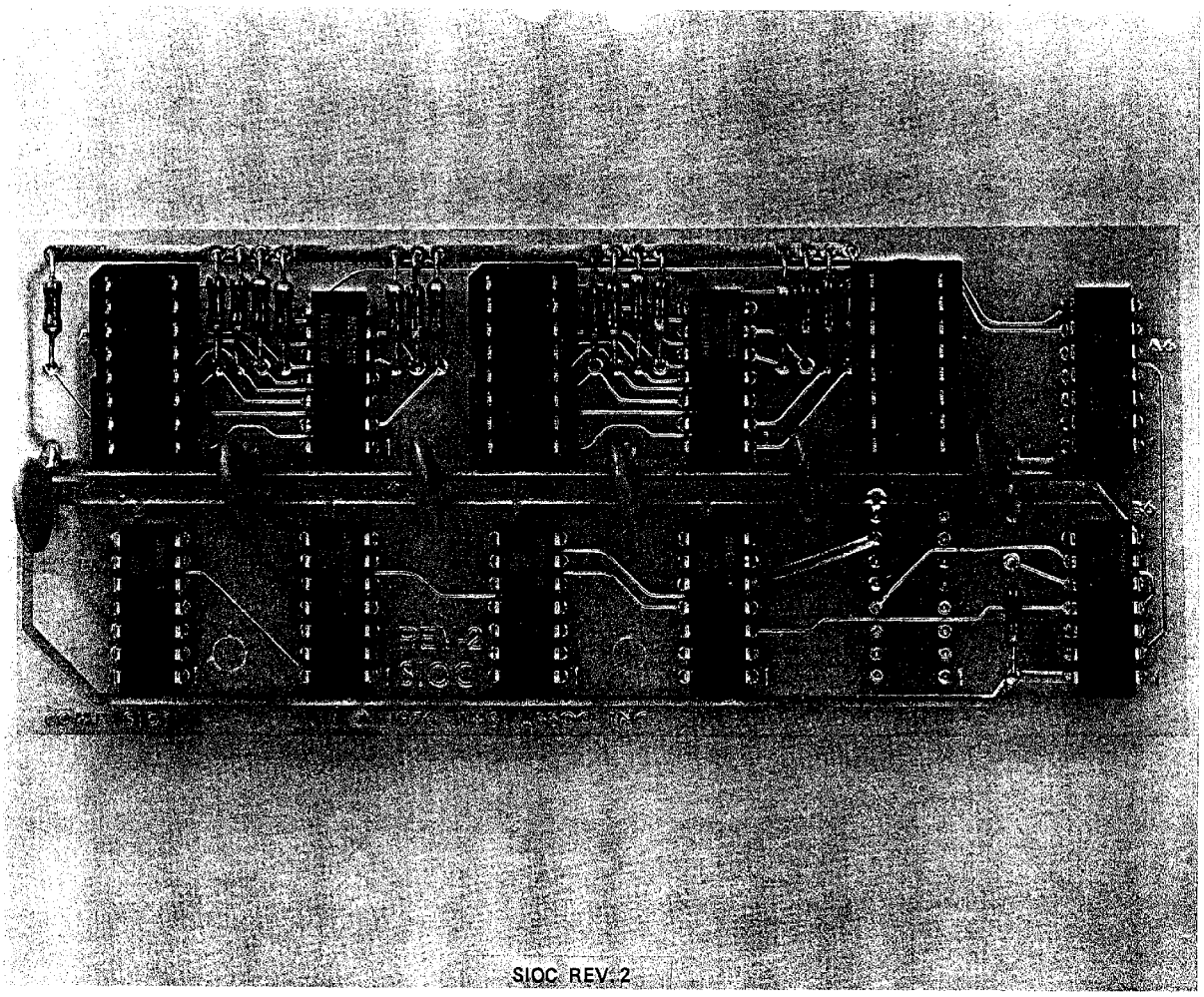
The four 7493 counters are arranged as a 16 bit ripple counter, clocked by the $\emptyset_2$ clock. Jumper sockets, A1 and A3 are jumpered so that when the selected binary value N (where N is selected to produce a desired final clock rate) is reached by the counter, the counter is reset. The 7430's and 7402 create the reset signal, while the 7474 is used to gate the reset pulse and create a symmetrical square wave output.

The final outclock frequency can be determined by:

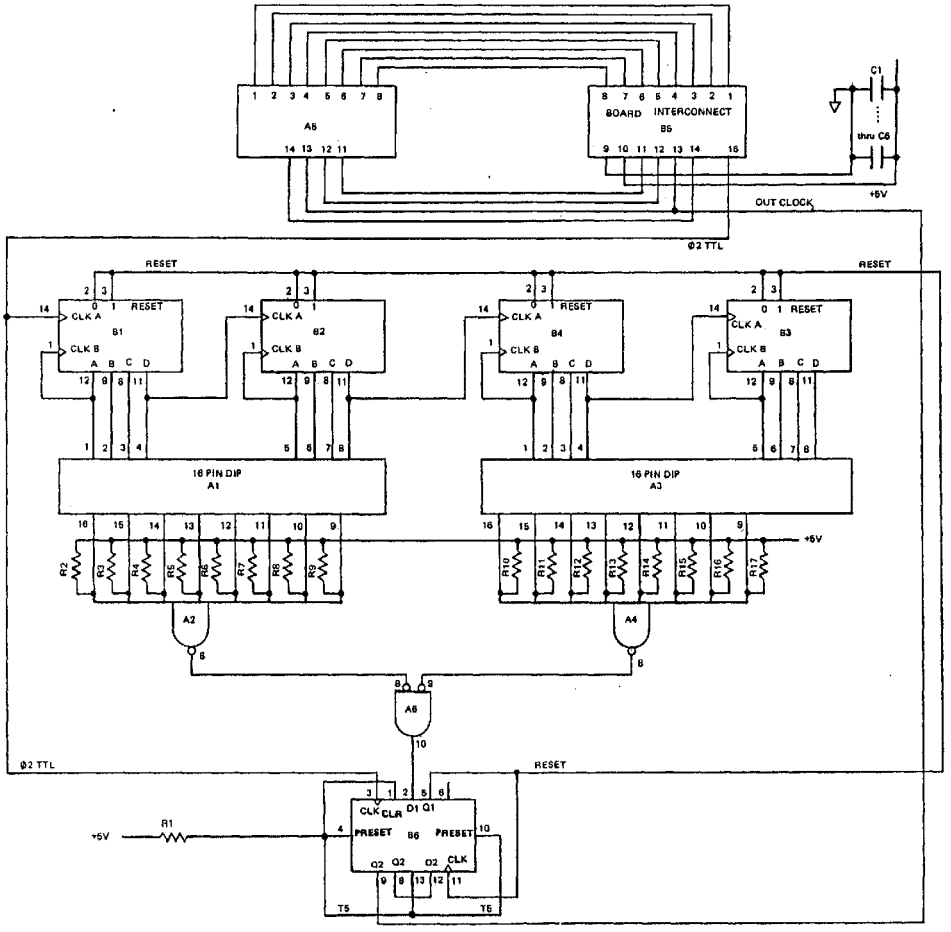
$$\text{Outclock (Hz)} = \frac{1}{2} \cdot \frac{2 \times 10^6 \text{ Hz}}{N}$$

Where N is the binary value in jumpers A1 and A3, and the factor of 1/2 is the result of the final ÷ 2 for the symmetrical output.

Decoupling capacitors are provided to eliminate the high frequency noise generated by the digital currents.



SIOC REV. 2



A1, A3, A5	16 PIN HEADER SOCKET
A2, A4	7430
A6	7402
B1, B2, B3, B4	7493
B5	16 PIN BOARD INTERCONNECT
B6	7474
C1 thru C6	.1 mF
R1 thru R17	1K ¼W

IMS ASSOCIATES,
SCHEMATIC DIAG
SIOC REV 2 4/

BOARD: SIOC

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Solder	15-0000001	5'	
Washers	21-3390001	3	#6 Fiber Washers
Screw	20-3702001	3	6-32x3/4" Phillips Pan Head Machine
Nut	21-3120001	3	#6 Hex Nut
Spacer	21-3600002	#6, 7/16" Spacer	
Socket	23-0800001	3	16 Pin Solder Tail Socket
Connector	23-0400009	1	16 Pin Board Interconnection
Header	23-0400001	3	16 Pin Integrated Circuit Header
Resistor	30-4100362	17	1K Ohm, ¼ Watt/brown, black, red
Capacitor	32-3010010	6	.1uF Disk Ceramic Capacitor
7402	36-0740201	1	Quad 2 Input NOR/SN7402N
7430	36-0743001	2	8 Input NAND/SN7430N
7474	36-0747401	1	Dual D Flip-Flop (Preset & Clear)/ SN7474N
7493	36-0749301	4	4 Bit Binary Counter/SN7493AN
PC Board	92-0000019	1	SIOC Rev. 2

ASSEMBLY INSTRUCTIONS

1) Unpack your board and check all parts against the parts list enclosed in the package.

2) If gold contacts on the edge connector appear to be corroded, use pencil eraser to remove any oxidation. NOTE: Do not use Scotchbright or any abrasive material as it will remove the gold plating.

3) Insert and solder each of the seventeen 1K Ohm, ¼ Watt resistors at locations R1 through R17 as shown on the Assembly Diagram.

IC INSTALLATION

NOTE: All IC's and 16 pin IC sockets orient pin 1 as indicated by the number 1 etched on the board.

4) Insert and solder one 7402 IC at location A6 as shown on the Assembly Diagram.

5) Insert and solder each of the two 7430 IC's at locations A2 and A4 as shown on the Assembly Diagram

6) Insert and solder one 7474 IC at location B6 as shown on the Assembly Diagram.

7) Insert and solder each of the four 7493 IC's at locations B1 through B4 as shown on the Assembly Diagram.

DISCRETE COMPONENTS INSTALLATION

8) Insert and solder each of the three 16 pin IC sockets at locations A1, A3, and A5 as shown in the Assembly Diagram. Plug in the three 16 pin headers.

9) Insert and solder each of the six .1uF disk capacitors at locations C1 through C6 as shown on the Assembly Diagram.

10) Insert and solder on the circuit side of the board one 16 pin board interconnection header B5 as shown on the Assembly Diagram (dotted lines).

ASSEMBLY INSTRUCTIONS (cont.)

TO MOUNT SIOC ONTO SIO BOARD

The SIOC mounting is accomplished by placing the fiber washers into each of the three holes in the SIOC on the component side and each of the three holes in the SIO board on the circuit side. Then insert the #6 screws through the fiber washer and spacers into the fiber washer of the SIO board. Plug in the board interconnect header during alignment before tightening screws.

SIOC BOARD

USERS GUIDE

The SIOC board allows the selection of any USART clock rate between 15 Hz and 56 KHz, allowing data transfer rates of .23 baud to 56K baud.

Designed to piggyback mount on the SIO board, the SIOC allows the user to select either the standard clock rates provided by the SIO board or the user-generated SIOC rate.

The SIOC may be easily mounted on the front of the SIO board, or the user may save one card slot by mounting the SIOC on the back of the SIO, and inserting the combination in the last slot of the mother board. To mount the SIOC on the back of the SIO board, the board rate select socket (B-11) must be soldered to the back of the SIO board, and the SIOC's binary divisor and clock jumper sockets should be mounted on the back of the SIOC board.

Jumper socket A-5 allows the selection of 8251 clock rates. Either the SIO standard rates or the SIOC generated rates may be jumpered to channels A or B. This jumper is arranged identically with B11 on the SIO board.

	9	8	110 A
	10	7	150 A
Chan. B Clk	11	6	300 A
Chan. A Clk	12	5	600 A
SIOC OUTCLK	13	4	1200 A
75 A	14	3	2400 A
	15	2	4800 A
$\emptyset_2$	16	1	9600 A

As with socket B11 on the SIO board, jumpers should be placed to connect the appropriate clock to the proper channel clock input.

To select a binary divisor, determine the desired USART clock rate, remembering that this rate may be 1, 16 or 64 times the desired final baud rate, as program selected by the mode byte output to the USART.

The binary divisor, N, can be determined by

$$N = \frac{1}{2} \cdot \frac{2 \times 10^6 \text{ Hz}}{\text{Clock Hz}}$$

This value should be converted to binary, and the jumpers (or switches) in A1 and A3 set so that the NAND input for every bit that should be a 1 is connected to the output bit of the counter. All other inputs (i.e., those desired to be a zero) should be left unconnected and pulled high. The selected clock rate will be on pin 13 of A5.

For example, to generate a 45 baud data rate for channel A (with a X16 USART clock), and to use channel B for a 1200 baud data rate, do as follows:

$$45 \text{ Hz} \times 16 = 720 \text{ Hz (Desired clock rate)}$$

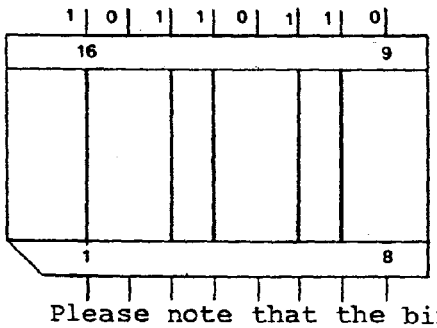
$$N = \frac{1}{2} \cdot \frac{2 \times 10^6 \text{ Hz}}{720 \text{ Hz}}$$

$$N = 1389_{10} \qquad N = 10101101101_2$$

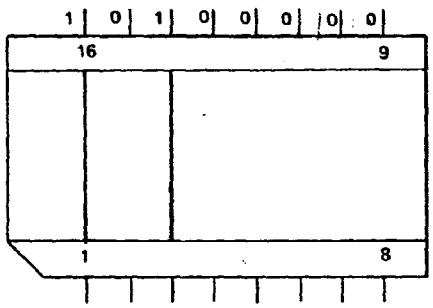
(to convert a decimal number to binary, see the attached note)

The jumpers should be jumpered as:

A1



A3



Please note that the binary number appears as:

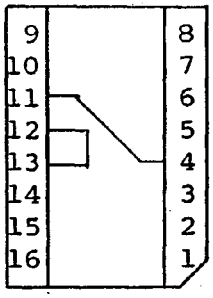
A1

1	2	3	4	5	6	7	8
1	0	1	1	0	1	1	0
LSB							

A3

1	2	3	4	5	6	7	8
1	0	1	0	0	0	0	0
							MSB

Jumper socket A5 as:



Chan. B.
Chan. A
SIOC OUTCLK

1200 A

Decimal to binary number conversion:

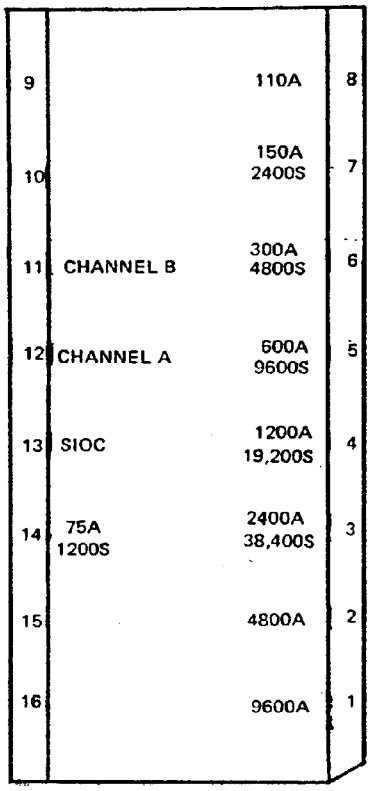
The simplest method to convert a number to binary is to divide it repeatedly by 2, recording the remainder for each step.

To convert the value 1389_{10} to binary,

Value	Value/2	Remainder	
1389	694	1	LSB (Least Significant Bit)
694	347	0	
347	173	1	
173	86	1	
86	43	0	
43	21	1	
21	10	1	
10	5	0	
5	2	1	
2	1	0	
1	0	1	MSB (Most Significant Bit)

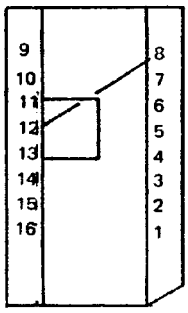
Note that the answer appears LSB first, thus, $1389_{10} = 10101101101_2$

Check: 1 + 4 + 8 + 32 + 64 + 256 + 1024 = 1389



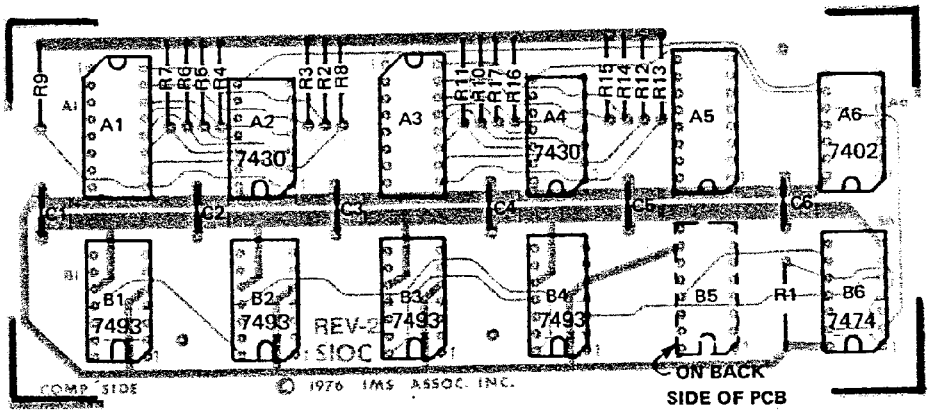
SOCKET POSITON A5

ASYNCHRONOUS RATES INDICATED "A"
ASSUME x16 CLOCK SELECTED IN 8251
SYNCHRONOUS RATES INDICATED BY "S"



EXAMPLE SHOWING CHANNEL A SET TO 110 BAUD
FOR A TELETYPE, AND CHANNEL B SET TO A
NON-STANDARD RATE SET BY SIOC JUMPERS IN A[illegible] A3

SIOC BAUD RATE SELECT JUMPERS



16 PIN BOARD
INTERCONNECT

IMS ASSOCIATES, INC.
ASSEMBLY DIAGRAM
SIOC REV 2 4/76