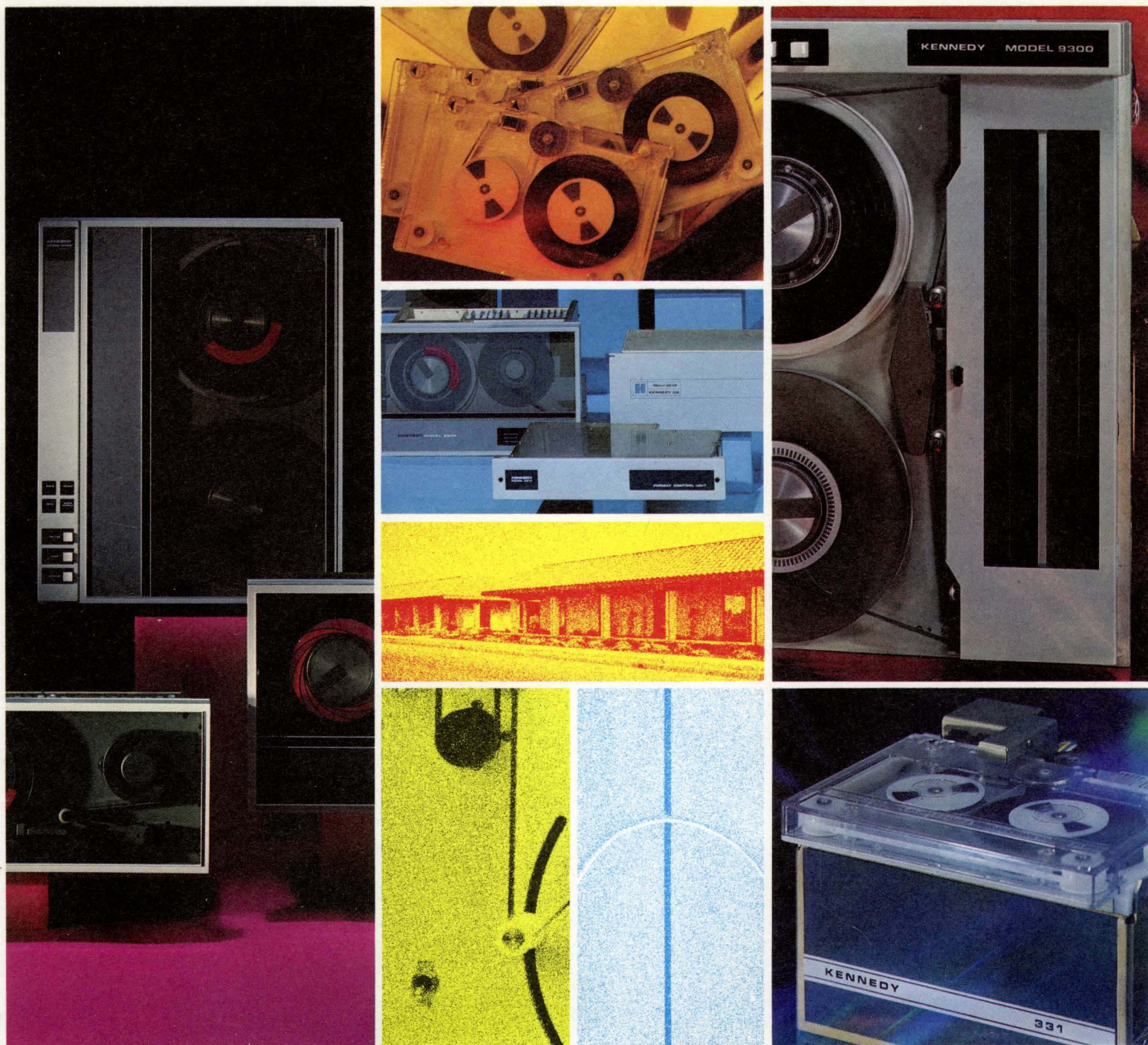


KENNEDY CO.

**Model 9800**  
**Digital Tape Transport**





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**SECTION I**  
**APPLICATION DATA**



## SECTION I

## APPLICATION DATA

## 1.1 INTRODUCTION

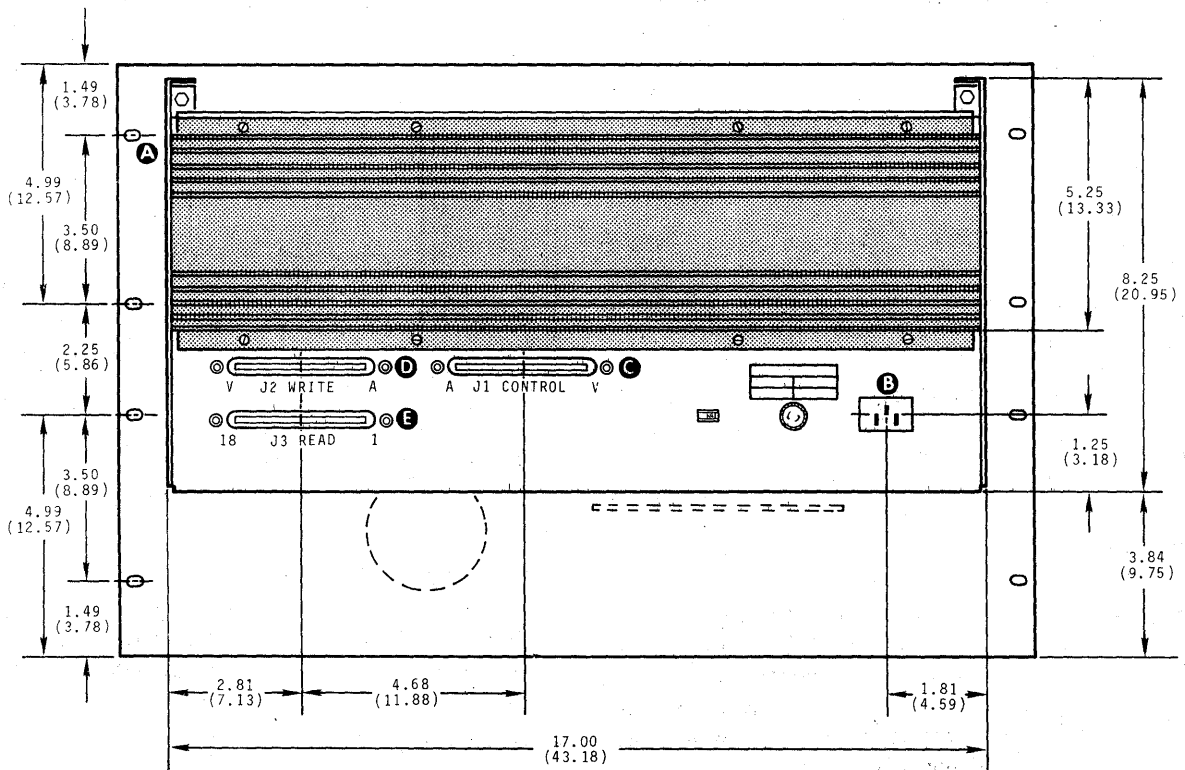
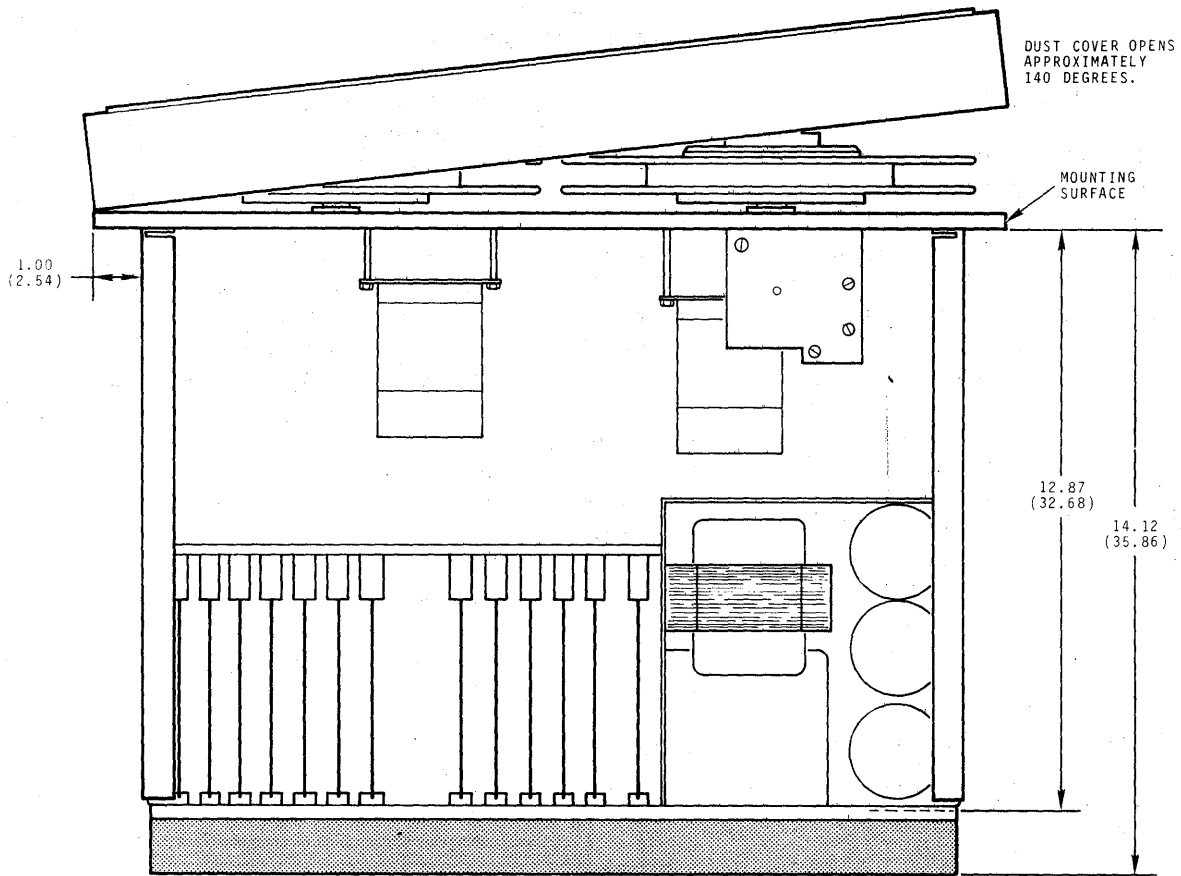
The Kennedy Model 9800 is a synchronous digital magnetic tape unit that with proper external formatting control is capable of reading and writing IBM compatible tapes, and is used in applications requiring high reliability at moderate tape speeds. Typical applications include operation with mini-computers, high speed data collection systems, and computer peripherals.

The Model 9800 is equipped with the electronics necessary for reading and writing tapes and for controlling the tape motion. The head specifications and the mechanical and electrical tolerances of the Model 9800 meet the requirements for IBM compatibility. However, the formatting electronics, parity generator, cyclic redundancy check character (CRCC) generator, gap control, etc., are not included and must be provided by the tape control and formatter

## 1.2 ELECTRICAL AND MECHANICAL SPECIFICATIONS

Tape (computer grade)	Erase head . . . . . Full width
Width . . . . . 0.5 inch (1.27 cm)	
Thickness . . . . . 1.5 mil (0.038 mm)	Load point and end of tape reflective strip detection . . . . . Photoelectric (IBM compatible)
Tension . . . . . 8.0 ounces (227 gm)	
Reel diameter . . . . to 8.5 inches (21.53 cm)	Broken tape detection . . . . . Photoelectric
Capacity . . . . . 1200 feet (360m)	
Reel hub . . . . . 3.69 inches (9.37 cm) dia per IBM standards	
	Dimensions (see Figure 1-1)
Reel braking . . . . . Dynamic	Transport mounting (horizontal) . . . . .
Recording mode (IBM compatible) . . . . NRZ1	. . . Standard 19-inch (48.26 cm) RETMA rack
Tape drive . . . . . Single capstan	Height . . . . . 12.5 inches (31.75 cm)
Tape speed . . . . 10-25 ips (25.4-63.5 cm/sec)	Width . . . . . 19.0 inches (48.26 cm)
	Depth (from mounting surface) . . . . .
Instantaneous speed variation . . . . . $\pm 3\%$	. . . . . 13.37 inches (33.96 cm)
Long term speed variation . . . . . $\pm 1\%$	Depth (overall) . . . . 15.87 inches (40.31 cm)
Start/stop displacement 0.1875 inch (0.476 cm)	Weight (transport only) . 45 pounds (20.25 kg)
Start/stop time @ 12.5 ips . . . . . 30 ms	Shipping weight . . . . . 60 pounds (27.00 kg)
Rewind speed . . . . . 120 ips (3.05m) (nominal)	
	Operating environment
Magnetic head assembly	Ambient temperature . . . . . $+2^{\circ}$ to $+50^{\circ}$ C
(Write to read gap displacement)	Relative humidity (noncondensing) . 15% to 95%
Dual gap seven-track read after write . . . . .	Altitude . . . . . to 30,000 feet (9120m)
. . . . . 0.30 inch (0.76 cm)	
Dual gap nine-track read after write . . . . .	
. . . . . 0.15 inch (0.38 cm)	Power requirements . . . . . 115/230 vac
Interchannel displacement error .. (measured with IBM master skew tape PN 432362)	50 to 500 Hz, single phase
Write (maximum) . . . . 150 $\mu$ inches (3.8 $\mu$ m)	Volt amps nominal . . . . . 200
Read (maximum) . . . . 150 $\mu$ inches (3.8 $\mu$ m)	Volt amps maximum . . . . . 300

**Table 1-1. Model 9800 Series Tape Transport Electrical and Mechanical Specifications**

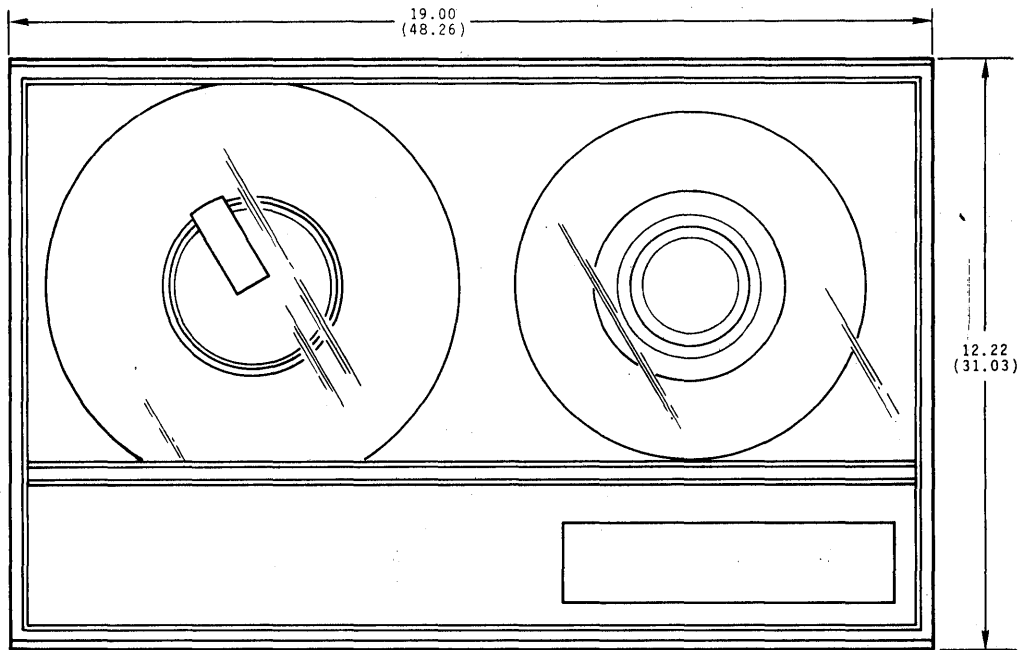


**B** INPUT POWER CONNECTOR  
(POWER CABLE 125-0068-001  
SUPPLIED WITH UNIT)

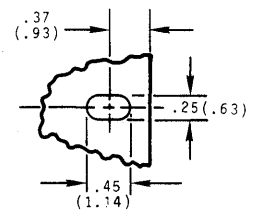
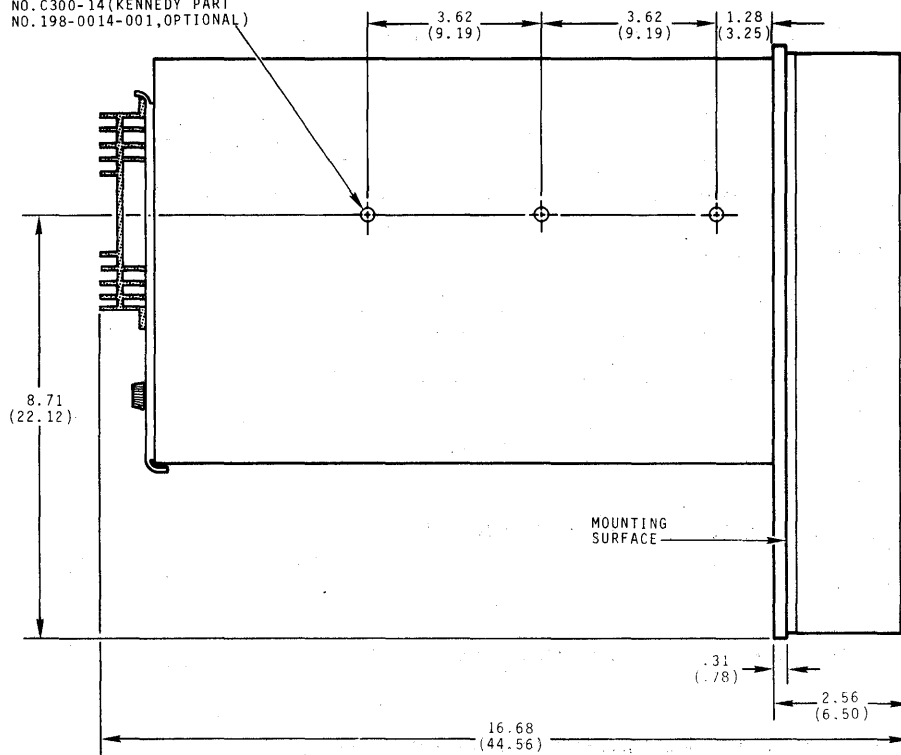
**C** P1 CONTROL CONNECTOR  
MATING CONNECTOR PART  
NUMBER 121-0096-036.

**D** P2 WRITE CONNECTOR  
MATING CONNECTOR PART  
NUMBER 121-0096-036

**E** P3 READ CONNECTOR  
MATING CONNECTOR PART  
NUMBER 121-0096-036



MOUNTING HOLES ARE FOR  
ZERO NONTILT TYPE SLIDE  
NO. C300-14 (KENNEDY PART  
NO. 198-0014-001, OPTIONAL)



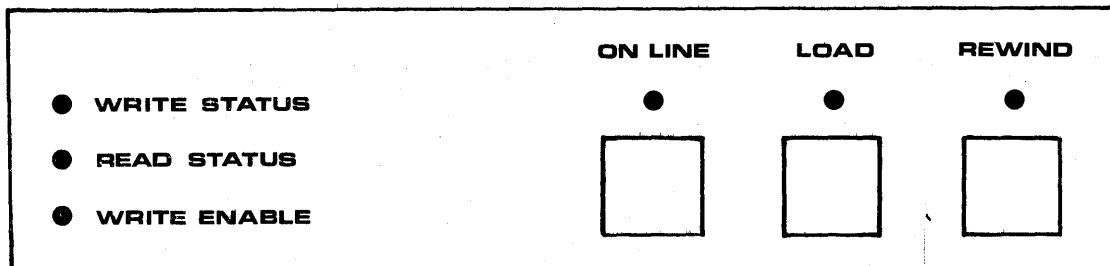
DETAIL A  
TYPICAL SLOT  
PATTERN

NOTE: DIMENSIONS SHOWN ARE IN  
INCHES. DIMENSIONS IN PARENTHESES  
ARE IN CENTIMETERS.

**Figure 1-1.**  
**Outline and Installation Drawing,**  
**Model 9800**



### 1.3 CONTROLS AND INDICATORS



#### ON LINE PUSHBUTTON/INDICATOR

A momentary pushbutton, which functions as alternate action. When first activated the tape unit is placed in an on-line condition; when the tape unit is on line it can be remotely selected and will be ready if tape is loaded to or past the load point. When activated again it takes the unit off line. The LED indicator is illuminated in the on-line condition. A short time lag is built in between closure and action to prevent accidental operation.

#### LOAD PUSHBUTTON/INDICATOR

The momentary pushbutton activates the reel servos (tensions tape) and starts the load sequence. The LED indicator is illuminated when the reel servos are activated and tape is tensioned.

#### REWIND PUSHBUTTON/INDICATOR

The momentary pushbutton activates a rewind operation. This control is enabled only when tape is tensioned and unit is off line. The LED indicator is illuminated during either a local or remote rewind operation.

#### WRITE STATUS INDICATOR

Indicator is illuminated whenever tape unit is on line, selected, and write status is selected.

#### READ STATUS INDICATOR

Illuminated when tape unit is on line, selected, and read selected.

#### WRITE ENABLE INDICATOR

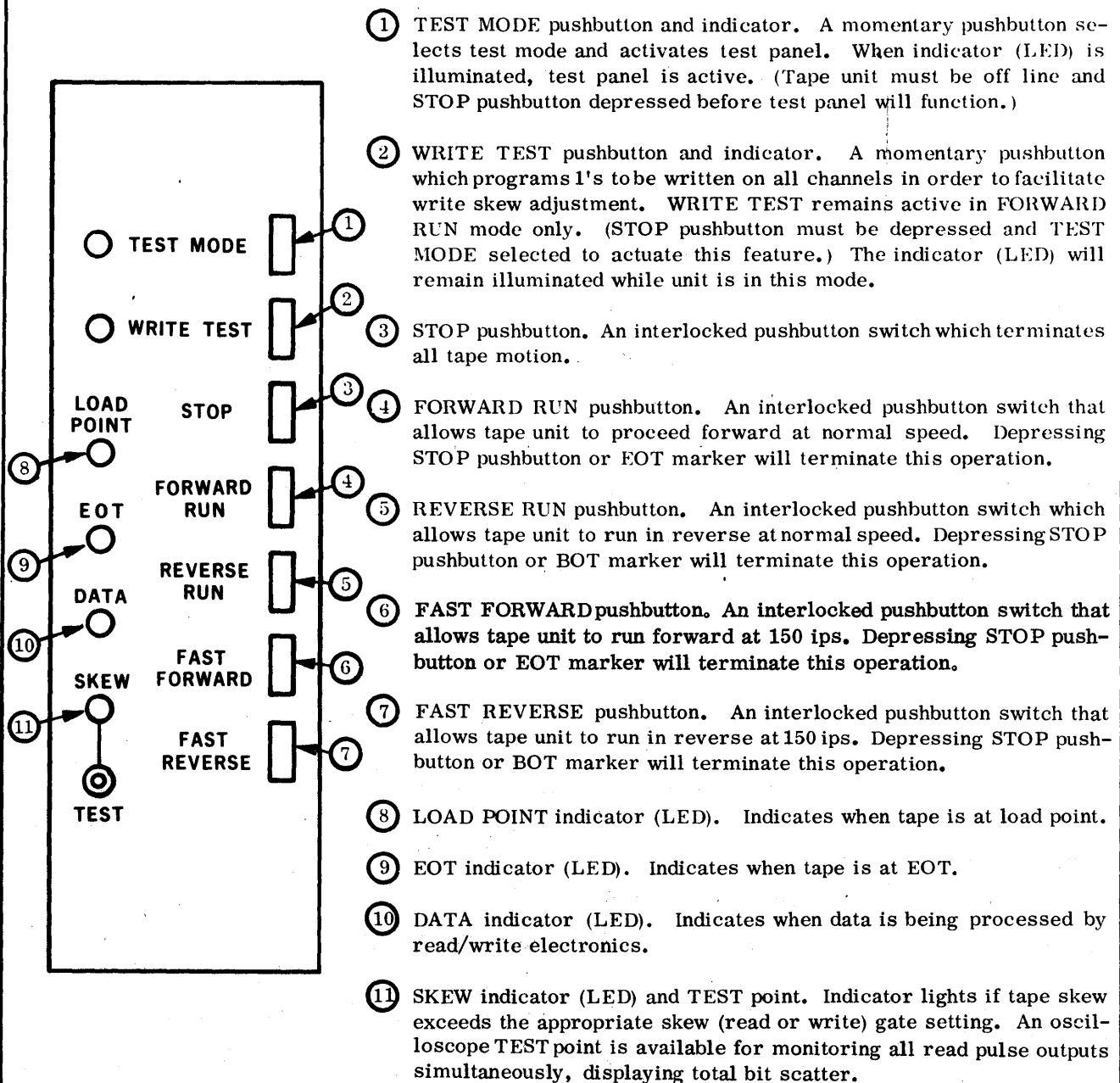
Illuminated whenever a reel with a write enable ring is mounted on the supply (file) hub.

LOAD and REWIND pushbuttons are disabled when the tape unit is on line.

**Figure 1-2. Controls and Indicators**

### Note

Tape transport must be off line and STOP pushbutton depressed before test panel can become functional.



- ① TEST MODE pushbutton and indicator. A momentary pushbutton selects test mode and activates test panel. When indicator (LED) is illuminated, test panel is active. (Tape unit must be off line and STOP pushbutton depressed before test panel will function.)
- ② WRITE TEST pushbutton and indicator. A momentary pushbutton which programs 1's to be written on all channels in order to facilitate write skew adjustment. WRITE TEST remains active in FORWARD RUN mode only. (STOP pushbutton must be depressed and TEST MODE selected to actuate this feature.) The indicator (LED) will remain illuminated while unit is in this mode.
- ③ STOP pushbutton. An interlocked pushbutton switch which terminates all tape motion.
- ④ FORWARD RUN pushbutton. An interlocked pushbutton switch that allows tape unit to proceed forward at normal speed. Depressing STOP pushbutton or EOT marker will terminate this operation.
- ⑤ REVERSE RUN pushbutton. An interlocked pushbutton switch which allows tape unit to run in reverse at normal speed. Depressing STOP pushbutton or BOT marker will terminate this operation.
- ⑥ FAST FORWARD pushbutton. An interlocked pushbutton switch that allows tape unit to run forward at 150 ips. Depressing STOP pushbutton or EOT marker will terminate this operation.
- ⑦ FAST REVERSE pushbutton. An interlocked pushbutton switch that allows tape unit to run in reverse at 150 ips. Depressing STOP pushbutton or BOT marker will terminate this operation.
- ⑧ LOAD POINT indicator (LED). Indicates when tape is at load point.
- ⑨ EOT indicator (LED). Indicates when tape is at EOT.
- ⑩ DATA indicator (LED). Indicates when data is being processed by read/write electronics.
- ⑪ SKEW indicator (LED) and TEST point. Indicator lights if tape skew exceeds the appropriate skew (read or write) gate setting. An oscilloscope TEST point is available for monitoring all read pulse outputs simultaneously, displaying total bit scatter.

Figure 1-3. Test Panel Controls and Indicators (Optional)

## 1.4 INTERFACE CONNECTIONS

The interface connectors on the Model 9800 are designed for twisted pair inputs and outputs. For each active pin there is a ground pin. The mating interface connectors, three 36-pin edge connectors (PN 121-0096) are supplied with the tape unit.

## 1.5 INTERFACE SIGNAL CHARACTERISTICS

The tape unit responds to zero true inputs and provides zero true outputs. Each signal input is terminated in such a manner as to provide matching for twisted pair cables. See Figure 1-4. Each output line is driven with an open collector driver. For best results the typical interfacing circuit configurations shown in Figure 1-5 should be used. The recommended twisted pair cable will reduce the magnitude of intercable crosstalk. Unless otherwise specified all wires should be 24 AWG minimum, with a minimum insulation thickness of 0.1 inch. Each pair should have not less than one twist per inch and the input-output cables should not exceed 20 feet in length.

## 1.6 INPUT SIGNAL DESCRIPTION

The input receiver circuits, due to zero true current sinking logic design, will interpret a disconnected wire or removal of power at the transmitter as a logic 0 or false condition. The logic 1 or true state requires 25 ma current sink with less than 0.4v.

The logic 0 or false state will be 3v due to the input matching resistors (see Figure 1-4). The recommended input pulse width is 2 microseconds. The rise and fall times for pulses and levels must be less than 0.5 microsecond. Each input is enabled when the tape transport is on line and selected.

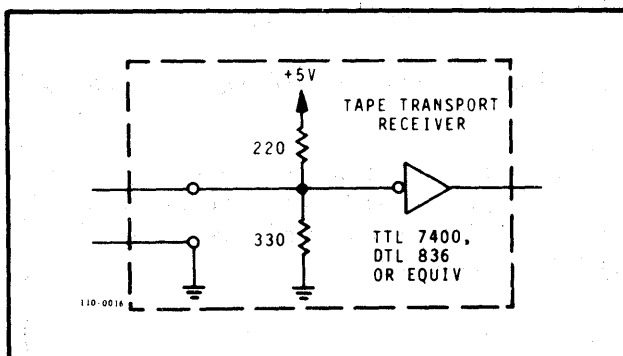


Figure 1-4. Typical Receiver Circuit

## 1.7 OUTPUT SIGNAL DESCRIPTION

Each output line is driven with an open collector current sinking logic driver which is capable of sinking up to 40 ma in the true state. All outputs are disabled (false) when the tape unit is not on line and selected.

## 1.8 TAPE MOTION COMMANDS

For maximum interface convenience, Model 9800 is configured to control tape motion and direction using the SYNCHRONOUS FORWARD command and SYNCHRONOUS REVERSE command. The tape transport capstan servo accelerates the tape to the required speed with a linear ramp. The tape is also decelerated to a stop with a linear ramp. Start and stop occurs within the interrecord gaps. The ramp time is 30 ms for 12.5 ips and varies inversely with tape speed. The amount of tape travel during the ramp up or ramp down is always 0.1875 inch.

These two factors are to be taken into consideration when writing and gapping. A delay is required before writing to insure that tape is up to speed and to allow read after write. Timing diagrams for pertinent commands to provide properly formatted tapes are shown in Figures 1-6 through 1-8.

Figure 1-6 shows the timing requirements for writing a block in a read after write system (dual gap head) in the write mode with read occurring immediately after writing. Figure 1-7 shows the timing requirements for reading a block on a read after write system in the forward direction. Figure 1-8 shows the timing requirements for reading a block on a read after write system in the reverse direction.

## 1.9 INTERFACE INPUT SIGNALS

All commands from and to the input/output connector are preconditioned by loading the machine and placing it on line using the front panel controls. The next commands set up the recorder.

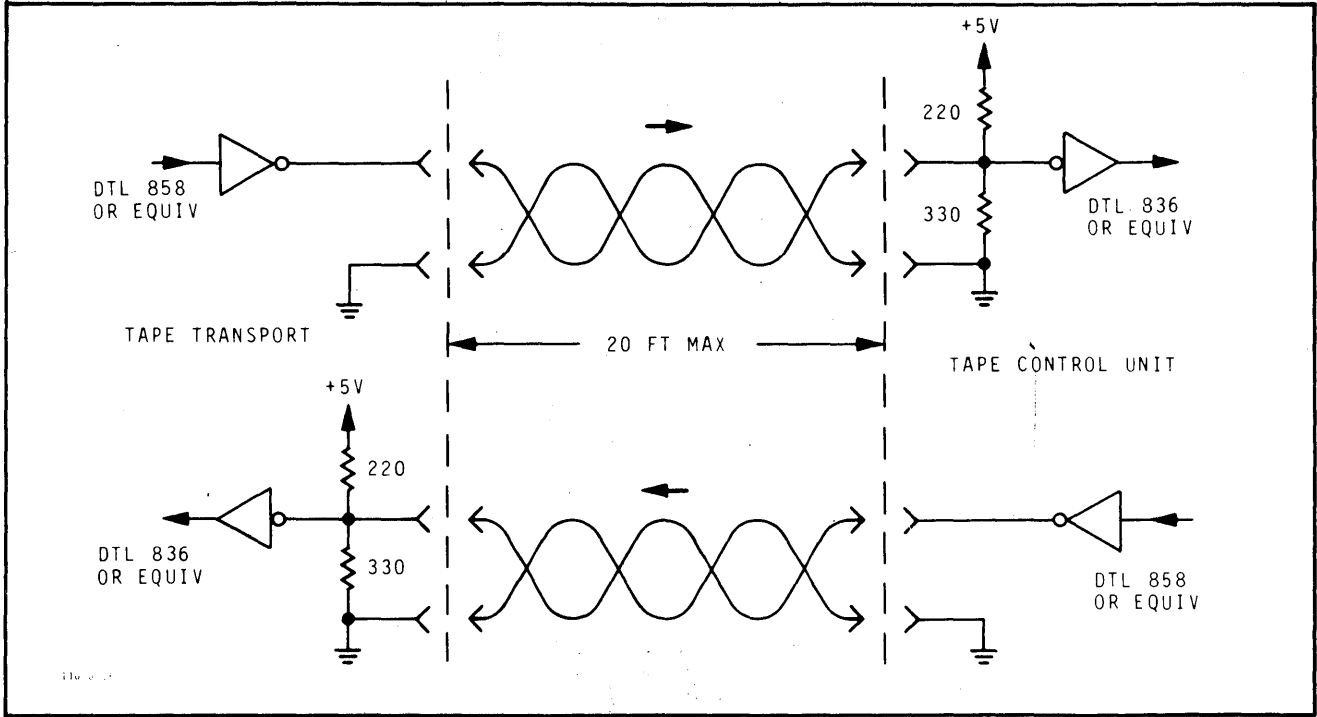
### 1.9.1 SETUP COMMANDS

#### TRANSPORT SELECT

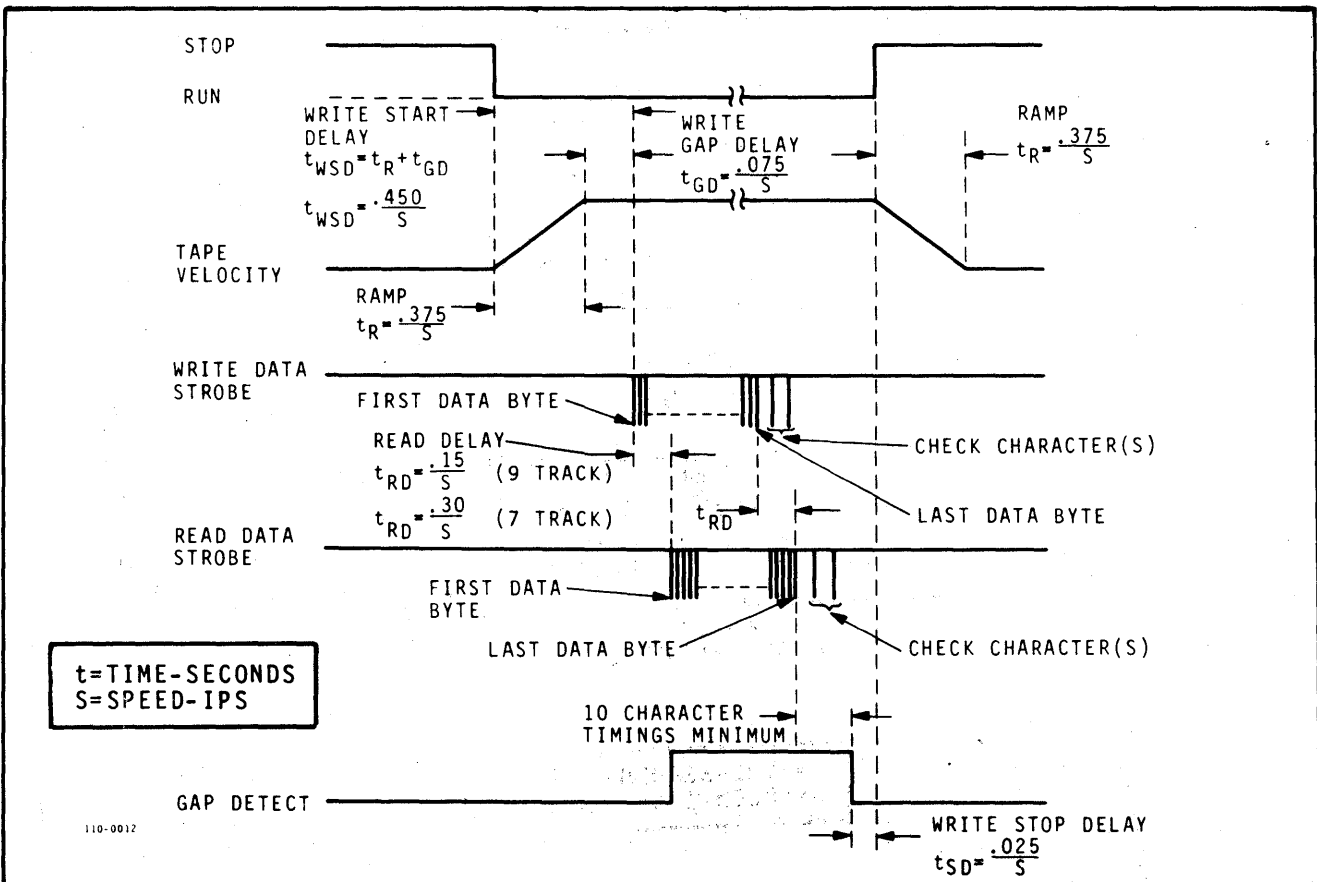
SLT Level P1-J

A level that when true enables all the interface drivers and receivers in the transport, thus connecting the transport to the controller. Transport must also be on line, and SLT must be true for entire write sequence (until tape motion stops). The SLT level may be removed to disconnect the machine from the system. The machine will remain in the last condition established by SWS.

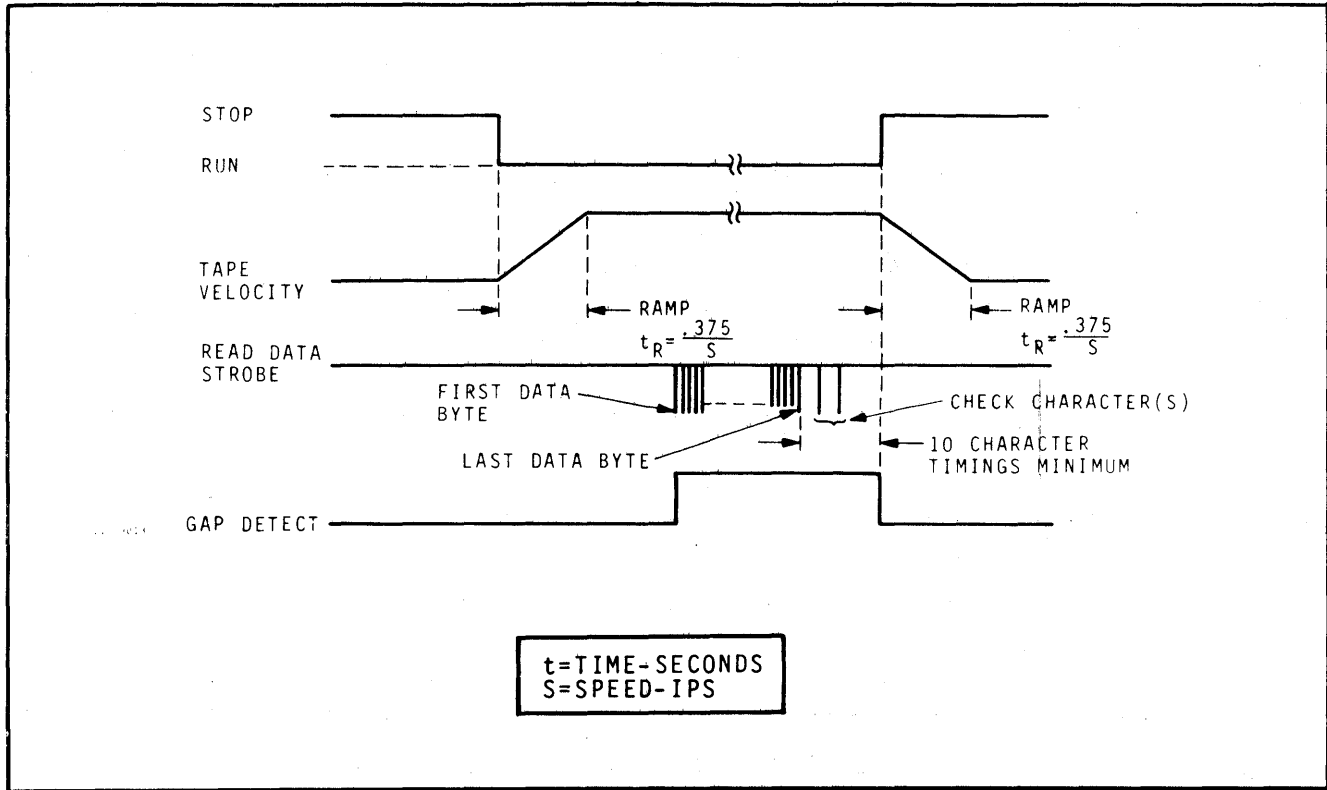




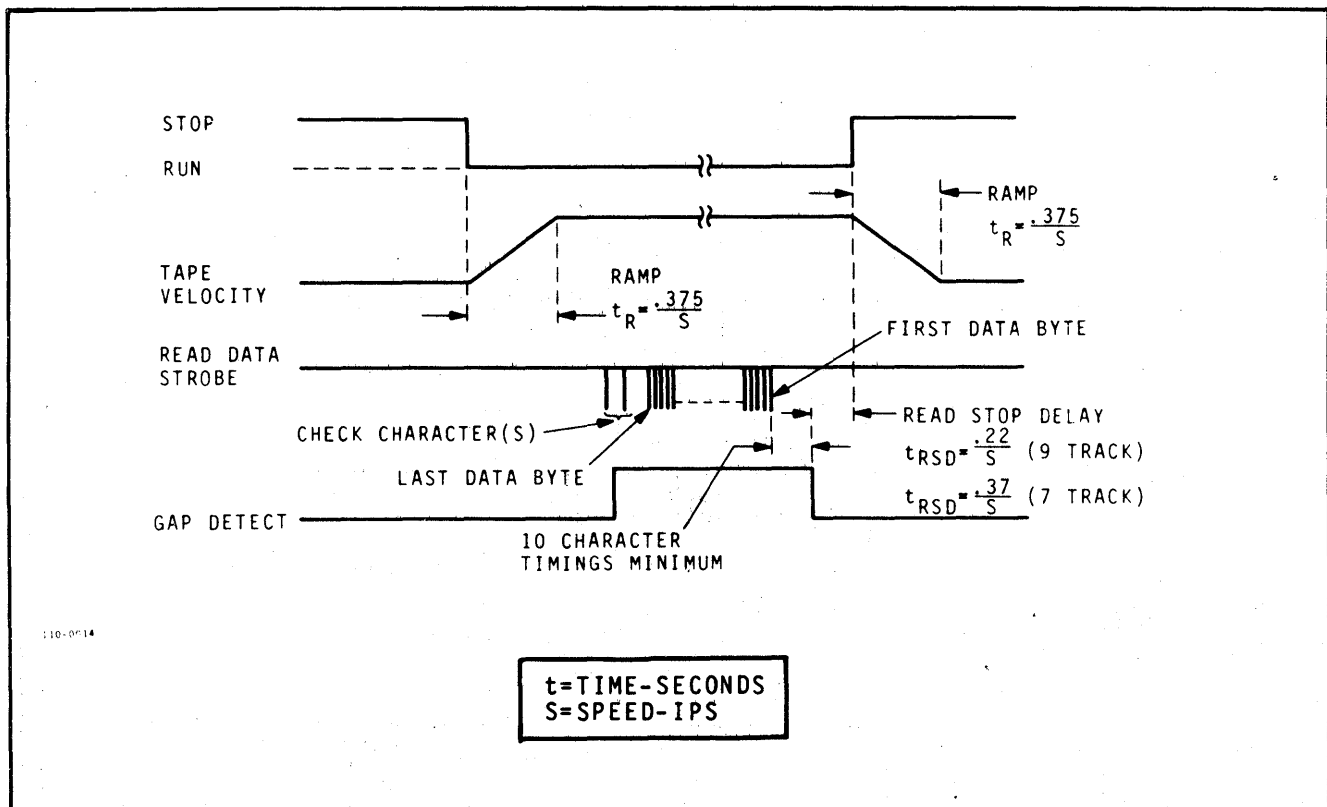
**Figure 1-5. Typical Interface Configuration**



**Figure 1-6. Read after Write Tape Transport Write Start and Stop Delays**



**Figure 1-7. Read after Write Tape Transport Reading Forward**



**Figure 1-8. Read after Write Tape Transport Reading in Reverse**

**DATA DENSITY SELECT**

(Dual Density only)

DDS Level P1-D

Used when the TRANSPORT DENSITY SELECT switch is in the remote position. When true, this level selects the high read density (dual density).

**1.9.2 TAPE MOTION COMMANDS****OVERWRITE (optional)**

OVW Level P1-B

A level that when true conditions appropriate circuitry in the transport to allow updating (rewriting) of a selected record. The transport must be in the write mode of operation to utilize the OVW feature.

**SYNCHRONOUS FORWARD COMMAND**

SFC Level P1-C

A level that when true, and the transport is ready and on line, causes tape to move forward at the specified speed. When the level goes false, tape motion ramps down and ceases.

**SYNCHRONOUS REVERSE COMMAND**

SRC Level P1-E

A level that when true, and the transport is ready and on line, causes tape to move in a reverse direction at the specified speed. When the level goes false, tape motion ceases. If the load point marker is detected during an SRC, the SRC will be terminated. If an SRC is given when the tape is at load point, it will be ignored.

**REWIND COMMAND**

RWC Pulse P1-H

A pulse input will rewind the tape past the load point and stop. The transport will then initiate a load forward sequence and return the tape to the load point marker. This input will be accepted only if the load point output is false. The transport may be taken off line while rewind is still in process. Rewind will continue normally.

**1.9.3 WRITE COMMANDS****SET WRITE STATUS**

SWS Level P1-K

A level that must be true at the leading edge of an SFC (or RUN and FWD) when the write mode of operation is required, and must remain true for a minimum of 10  $\mu$ sec after the leading edge of the SFC (or RUN and FWD). SWS is sampled at the leading

edge of the SFC or SRC (or RUN and FWD), toggling the read/write flip-flop to the appropriate state. Internal interlocks in the 9800/9700 will prevent writing in the reverse direction, when the write enable ring is missing, when the tape unit is off line, when loading to a load point, and during a rewind.

**WRITE DATA INPUTS**

<u>Nine Track</u>		<u>Seven Track</u>		
WDP		WDC		P2-I
WD0				P2-M
WD1				P2-N
WD2		WDB		P2-P
WD3		WDA		P2-R
WD4		WDS		P2-S
WD5		WD4		P2-T
WD6		WD2		P2-U
WD7		WD1		P2-V

Nine lines for nine-track operation, seven lines for seven-track operation. These are levels that if true at WDS time will result in a flux transition being recorded on tape (transport is in the write mode). Data inputs must have settled 0.5  $\mu$ sec before the leading edge of the WDS pulse and must remain quiescent 0.5  $\mu$ sec beyond the trailing edge of the WDS pulse. The CRCC is written by providing the correct data character together with a WDS four character times after the last data character of the record.

The LRCC is written using the WARS signal. The LRCC can also be written by providing the correct data character together with a WDS. If the LRCC is written (DATA-WDS) in this manner a WARS should be given one character time after the LRCC to insure proper IRG erasure in case of data input error.

**WRITE DATA STROBE**

WDS Pulse P2-A

A pulse of 2  $\mu$ sec nominal width for each character to be written. Writing occurs on the leading edge of the WDS. WDS may be a 1  $\mu$ sec minimum, 3  $\mu$ sec maximum pulse. Data inputs must have settled for at least 0.5  $\mu$ sec before the leading edge of WDS and remain quiescent for at least 0.5  $\mu$ sec beyond the trailing edge.

**WRITE AMPLIFIER RESET**

WARS Pulse P2-C

A pulse of 2  $\mu$ sec nominal width that, when true, resets the write amplifier circuits on the leading edge. The purpose of this line is to enable writing of the longitudinal redundancy check character (LRCC) at the end of a record. This insures that all tracks are properly erased in an interrecord gap (IRG).



In a seven-track system, the leading edge of the WARS pulse should be four character times after the leading edge of the WDS associated with the last data character in the block. In a nine-track system, the leading edge of the WARS pulse should be eight character times after the leading edge of the WDS associated with the last data character in the block (four character times after the CRCC is written).

#### 1.9.4 READ COMMANDS

A read after write machine will always have read selected. When write is selected (SWS) the data just written will be read back using a high threshold level on the read amplifiers. When SWS is false the normal threshold is applied to the read amplifiers.

#### **AUTOMATIC CLIPPING LEVEL DISABLE**

ACLD Level P3-6

When true this level overrides the automatic clipping level electronics and holds the read electronics in the normal clipping level.

#### 1.9.5 SHUTDOWN COMMANDS

The use of a given magnetic tape unit may be terminated by an OFF LINE command. Once this command is given the tape unit may be returned to an interface command only by operating the front panel ON LINE switch.

#### **OFF LINE COMMAND**

OFFC Pulse P1-L

A level or pulse (minimum width 2  $\mu$ sec) that resets the on-line flip-flop to the zero state, placing the transport under manual control. It is gated only by SELECT in the transport logic, allowing an OFFC to be given while a rewind is in progress. An OFFC should be separated from a rewind command by at least 2  $\mu$ sec.

### 1.10 INTERFACE OUTPUT SIGNALS

All output signals are enabled only when the tape transport is on line and selected.

#### 1.10.1 STATUS OUTPUTS

#### **ON LINE**

ONL Level P1-M

A level that is true when the on-line flip-flop is set. When true, the transport is under remote control. When false, the transport is under local control.

#### **TRANSPORT READY**

RDY Level P1-T

A level that is true when the tape transport is on tape; that is, when the initial load sequence is complete and the transport is not rewinding. When true, the transport is ready to receive a remote command.

#### **HIGH DENSITY INDICATOR**

(Dual Density only)

HDI Level P1-F

A level that is true only when the high-density mode of operation is selected.

#### **FILE PROTECT**

FPT Level P1-P

A level that is true when a reel of tape without a write-enable ring is mounted on the transport supply (or file) hub.

#### **WRITE ENABLE**

WEN Level P1-S

A level that is true when a reel of tape with a write-enable ring is mounted on the transport supply (or file) hub. Opposite of file protect.

#### **LOAD POINT**

LDP Level P1-R

A level that is true when the load point marker is under the photosensor and the transport is not rewinding. After receipt of an SFC the signal will remain true until the load point marker leaves the photosense area. (Circuitry using this output should not use the transitions to and from the true state.)

#### **TAPE RUNNING**

RNG Level P1-V

This is a level that is true when tape is being moved under capstan control and remains true until tape motion has ceased. (Includes forward, reverse, and rewind tape motion.)

#### **END OF TAPE**

EOT Level P1-U

A level that is true for the duration of the EOT marker. (Circuitry using this output should not use the transitions to and from the true state.)

#### **REWINDING**

RWD Level P1-N

A level that is true only when the transport is engaged in a rewind operation or returning to the load point. (Goes true approximately 5  $\mu$ sec after a rewind command is given.)

### 1.10.2 READ OUTPUTS

Read outputs are present at all times in tape units when a dual gap head is used (read after write). The high threshold level is selected internally when SWS is selected. In a read/write tape unit (single gap head) read outputs are inhibited when SWS is true.

#### READ DATA STROBE

RDS                      Pulse                                      P3-B

A pulse of 2  $\mu$ sec minimum width for each data character read from tape. Although the average time between two read data strobes is

$$\tau_1 \text{ (sec)} = \frac{1}{s \cdot d}$$

where

s = tape speed in inches per second  
d = density characters per inch

the minimum time between consecutive read data strobes is less than this figure due to skew and bit crowding effects. A guaranteed safe value for the minimum time is  $1/2 \tau_1$ .

#### READ GAP DETECT

RGAP                      Level                                      P3-N

A level that is true approximately nine character spacings after the last data byte (five character spacings on seven-channel), and remains true until the first data byte of the subsequent data block. Note: This level will be true whenever tape motion is at rest.

### READ DATA LEVEL

<u>Nine Track</u>	<u>Seven Track</u>	
RDP	RDC	P3-1
RD0		P3-3
RD1		P3-4
RD2	RDB	P3-8
RD3	RDA	P3-9
RD4	RD8	P3-14
RD5	RD4	P3-15
RD6	RD2	P3-17
RD7	RD1	P3-18

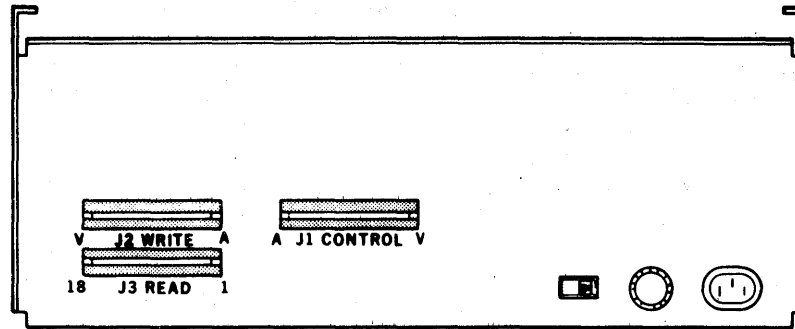
Nine lines, nine track; seven lines, seven track. Nine (or seven) staticisers are provided, which act as a one-stage read deskewing buffer. Each output is a level that changes to the appropriate state approximately 1  $\mu$ sec before the read data strobe and remains in that state until 1  $\mu$ sec before the next read data strobe. Data lines return to false condition in the IRG when tape motion stops regardless of the last character read.

It is recommended that read data strobes and the read gap detect be ignored during the first read or write operation from load point for  $\tau_2$  msec after the load point output goes false, where  $\tau_2 = 1000/s$  (s = speed of tape unit).

The read gap in a read after write tape unit is downstream from the write gap. Thus when the write gap is initially energized the read gap may detect a flux change depending on the initial state of magnetism on the tape.

### 1.11 SUMMARY OF INTERFACE CHARACTERISTICS

Figure 1-9 shows the location of connectors and pin numbers with signal names.



← INPUT  
→ OUTPUT

### WRITE CONNECTOR J2

ACTIVE	GROUND	SIGNAL	MNEMONIC
A	1	← WRITE DATA STROBE	WDS
B	2	← N.C.	
C	3	← WRITE AMPLIFIER RESET	WARS
D	4	← NOT USED	
E	5	← NOT USED	
F	6	← NOT USED	
H	7	← NOT USED	
J	8	← NOT USED	
K	9	← NOT USED	
L	10	← WRITE DATA CHANNEL P	WDP
M	11	← WRITE DATA CHANNEL 0	WDO
N	12	← WRITE DATA CHANNEL 1	WD1
P	13	← WRITE DATA CHANNEL 2	WD2
R	14	← WRITE DATA CHANNEL 3	WD3
S	15	← WRITE DATA CHANNEL 4	WD4
T	16	← WRITE DATA CHANNEL 5	WD5
U	17	← WRITE DATA CHANNEL 6	WD6
V	18	← WRITE DATA CHANNEL 7	WD7

### CONTROL CONNECTOR J1

ACTIVE	GROUND	SIGNAL	MNEMONIC
A	1	← SPARE	
B	2	← OVERWRITE	OVW
C	3	← SYNCHRONOUS FORWARD	SFC
D	4	← DATA DENSITY SELECT	DDS
E	5	← SYNCHRONOUS REVERSE	SRC
F	6	← DATA DENSITY INDICATOR	DDI
H	7	← REWIND COMMAND	RWC
J	8	← SELECT	SLT
K	9	← SET WRITE STATUS	SWS
L	10	← OFF LINE COMMAND	OFFC
M	11	← ON LINE	ONL
N	12	← REWINDING	RWD
P	13	← FILE PROTECT	FPT
R	14	← LOAD POINT	LP
S	15	← WRITE ENABLE	WEN
T	16	← TRANSPORT READY	RDY
U	17	← END OF TAPE	EOT
V	18	← TAPE RUNNING	RNG

### READ CONNECTOR J3

ACTIVE	GROUND	SIGNAL	MNEMONIC
1	A	→ READ DATA CHANNEL P	RDP
2	B	→ READ DATA STROBE	RDS
3	C	→ READ DATA CHANNEL 0	RDO
4	D	→ READ DATA CHANNEL 1	RD1
5	E	→ NOT USED	
6	F	→ AUTO DISABLE	
7	H	→ NOT USED	
8	J	→ READ DATA CHANNEL 2	RD2
9	K	→ READ DATA CHANNEL 3	RD3
10	L	→ NOT USED	
11	M	→ NOT USED	
12	N	→ GAP DETECT	
13	P	→ NOT USED	
14	R	→ READ DATA CHANNEL 4	RD4
15	S	→ READ DATA CHANNEL 5	RD5
16	T	→ NOT USED	
17	U	→ READ DATA CHANNEL 6	RD6
18	V	→ READ DATA CHANNEL 7	RD7

Figure 1-8. Summary of Interface Characteristics



**SECTION II**  
**INSTALLATION AND OPERATION**

## SECTION II

### INSTALLATION AND OPERATION

#### 2.1 INSTALLATION

##### 2.1.1 INSPECTION

Prior to installation, inspect thoroughly for foreign material that may have become lodged in the tension arms, reel hubs, and other moving parts.

##### 2.1.2 MOUNTING

Physical dimensions and outline of the tape transport are shown in Figure 1-1. The transport requires 12.22 inches vertical mounting space on the standard 19 inch rack. Transports in a system configuration should be arranged to require less than 20 feet of cabling between the Format Control Unit and the furthest tape unit.

##### 2.1.3 SERVICE ACCESS

Access to the plug-in cards, the power supply, and the control electronics is available from the top of the unit. The voltage regulator and the servo power assembly are mounted on the inside of the heatsink on the rear of the transport. The voltage selection switch, fuse, power connector, and interface connectors are also accessible from the rear of the unit. For servicing electronics, test points are provided by standoff pins on circuit boards and are identified by upper case letters near each test point.

##### 2.1.4 INTERCABLING

Installation of the tape transport requires fabrication of interconnection cables between the Format Control Unit and the tape transport. Three 36-pin cable connectors that mate with the connectors on the units are supplied with the system.

The connector pin assignments are shown in Figure 1-9. Twisted pair cabling should be used to reduce intercable crosstalk. All wires should be 24 AWG, minimum, with a minimum insulation thickness of 0.01 inch. Each pair should have no less than one twist per inch, and maximum cable length should not exceed 20 feet.

##### 2.1.5 POWER CONNECTIONS

**CAUTION**

Before connecting the unit to the power source, make certain the line voltage selector switch, near power connector

on rear flange, is set to correct voltage (115 or 230 VAC) and that proper fuse has been installed (3A 3AG for 115 VAC, 1.5A 3AG for 230 VAC).

A detachable power cord is supplied with the tape unit. The power cord is 7.5 feet long and has a NEMA three-prong (two power, one chassis ground) plug for connection to the power source.

##### 2.1.6 TERMINATION OF INPUT LINES

Terminator cards are provided to terminate input lines for minimum reflection. When machines are used singly or in a radial interface, terminators remain in place.

In a daisychain installation of two or more machines, terminators are removed from all machines except the machine at the greatest distance from the interface.

#### 2.2 OPERATION

##### 2.2.1 INTERFACE

Before placing the unit in operation, make certain that the interface connection procedures outlined in Section I have been performed.

##### 2.2.2 CONTROLS AND INDICATORS

Paragraph 1.3 lists the controls and indicators for the tape transport and describes the functions of each. The optional test panel controls are shown in Figure 1.3.

##### 2.2.3 PRELIMINARY PROCEDURES

Before placing the unit in operation, proceed as follows:

- a. Clean the tape transport read/write head, capstan, and idlers to prevent degradation of magnetic tapes.
- b. Check for correct setting of line voltage selector switch on rear flange, and make sure that correct fuse is installed (paragraph 2.1.5).
- c. Set primary power switch on control panel to ON.

### 2.2.4 TAPE THREADING

To thread the tape on the transport, proceed as follows:

- a. Raise the latch of the quick-release hub and place the tape file reel to be used on the supply hub (Figure 2-1) with the write-enable ring side next to the transport deck.
- b. Hold the reel flush against the hub flange and secure it by pressing the hub latch down.
- c. Thread the tape along the path as shown by the threading diagram (Figure 2-1).
- d. Holding the end of the tape with a finger, wrap a few turns counterclockwise around the takeup hub.

### 2.2.5 TAPE LOADING

Pressing the LOAD pushbutton energizes the reel servos and initiates a load sequence. Tape advances to the load point marker and stops.

If for some reason the load point marker is already past the sensor as, for example, in restoring power after a shutdown, tape will continue to move. Under these conditions, press REWIND and tape will rewind to load point.

Once pressed, the LOAD switch is illuminated and is inactive until power has been turned off or tape is removed from the machine.

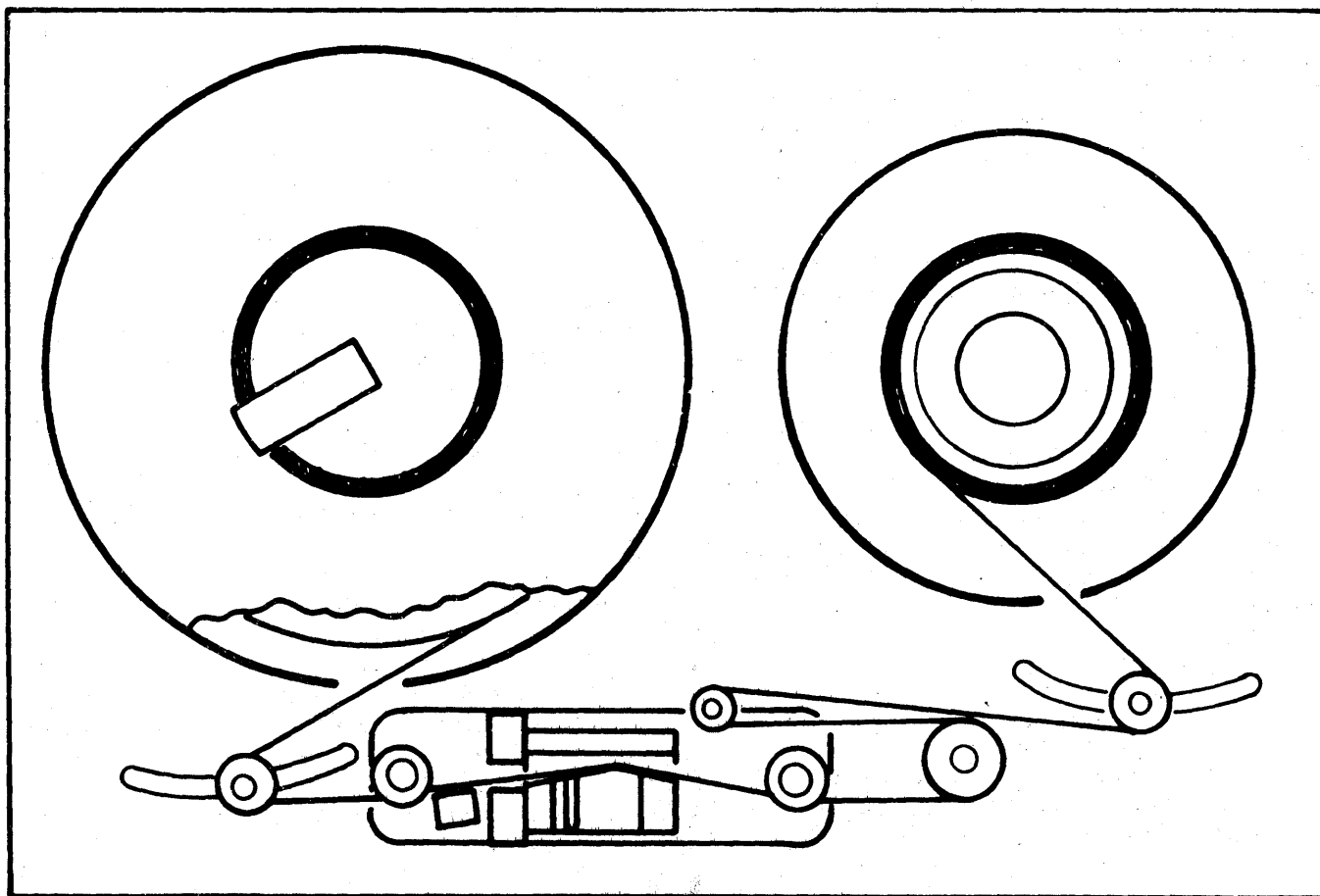
### 2.2.6 PLACING TAPE UNIT ON LINE

After the tape is properly threaded and has been loaded and brought to the load point, press the ON LINE pushbutton and check that the ON LINE indicator illuminates. (LOAD and REWIND pushbuttons are disabled when the tape unit is on line.) On-line status enables the tape unit to be remotely selected and to perform all normal operations under remote control.

### 2.2.7 TAPE UNLOADING AND REWIND

Provision is made in the 9000-series transports for rewinding a tape to the load point under remote control. However, this operation may also be performed manually. Proceed as follows.

- a. If the ON LINE indicator is illuminated, press the ON LINE pushbutton. Check that the indicator extinguishes when pressure is removed.
- b. Press the REWIND pushbutton. The tape will now rewind to the load point marker.



**Figure 2-1. Tape Threading Diagram**

- c. After the tape has been positioned at the load point under remote or local control, press the REWIND pushbutton to rewind the tape past the load point to the physical beginning of the tape.

#### NOTE

The rewind sequence cannot be stopped until the tape has rewound either to the load point or until tension is lost at the physical beginning of the tape.

#### 2.2.8 POWER SHUTDOWN

A tape transport should not be turned off when tape is loaded and is past the load point marker. Kennedy 9000-series transports are designed to prevent physical damage to the tape in the event of power failure,

and to minimize operator error which could destroy recorded data. In the event of power failure during tape unit operation, manually wind the tape forward several feet before restoring power. When power has been restored, press the LOAD pushbutton, then the REWIND pushbutton. This will rewind the tape to the load point. If desired, the tape can then be advanced to the data block nearest the point at which the power failure occurred, by initiating the appropriate control commands.

Although it is possible to develop procedures which would allow power shutdown between files or record blocks on a tape, this is not recommended. Where data files are short, it is preferable to use smaller tape reels.

**SECTION III**  
**THEORY OF OPERATION**

## SECTION III

### THEORY OF OPERATION

#### 3.1 INTRODUCTION

This section describes the tape transport on a functional basis. The description applies to the standard model using the 800 cpi NRZ1 data electronics and covers all tape speeds. Models using the 1600 cpi phase encoded electronics, the dual density 800/1600 cpi electronics, or the seven-track NRZ1 electronics include a different set of data electronics, and these are described in special supplements that accompany the standard manual.

Each circuit card schematic is preceded by a detailed circuit description that explains the operation of the card on the component level. The description offered in this section is more in the nature of a block diagram description, and divides the transport into three main functional subsections — control logic, servo system, and data electronics.

#### 3.2 CONTROL LOGIC

##### 3.2.1 INTRODUCTION

The control logic section of the tape transport generates the appropriate internal tape motion commands in response to input commands from the transport interface, the main pushbutton panel, and from the test panel pushbuttons. The control electronics receive these commands and generate transport motion if all internal interlocks are satisfied. In addition, the control electronics return the transport status outputs to the interface and illuminate the respective indicators on the main panel and on the test panel.

Five plug-in circuit cards constitute the control section logic: Control Terminator Type 3841, Pushbutton Control Type 3843, Ramp Generator Type 3645, and Sensor Amplifier/Driver Type 3844. The modules are housed in the card cage assembly and plug into the master board. Figure 3-1 is a simplified block diagram of the control logic, showing the signal flow between the control modules. As can be seen, the input signals from the interface are supplied, after being terminated on the Control Terminator module, to the Control Interface module, where these signals are acknowledged if certain interlocks are satisfied. The motion commands are then supplied to the Pushbutton Control module. This card also includes the interlocks for the main panel pushbuttons and for the test panel pushbuttons. If the

interlocks are satisfied, the Pushbutton Control module encodes all tape motion commands onto three command lines: RUN NORMAL (RNN1), RUN FAST (RNFST1), and REVERSE SELECT (RVS1). The three command lines are then supplied to the Ramp Generator module which produces accurate analog voltage output. The output of the Ramp Generator is then supplied to the Capstan Servo Amplifier module in the servo system, described below. The voltage output of the Ramp Generator in conjunction with the feedback from the capstan tachometer is used to energize the capstan motor and to advance the tape in the desired speed and direction. The Ramp Generator provides linear ramp-ups to speed and linear ramp-downs to standstill in order to minimize the stress on the tape and maintain accurate speeds.

The Sensor Amplifier/Driver module receives the inputs from the file protect switch, the load point sensor, end of tape sensor, and broken tape sensor. These signals are amplified and supplied to the other modules in the control section where they provide the inputs to the interlocks. The Sensor Amplifier/Driver module also contains the drivers for the front panel indicators, the driver for the file protect solenoid, and the write and erase head drivers.

##### 3.2.2 CONTROL LOGIC OPERATION DURING A WRITE SEQUENCE

A write operation will be used as an example to demonstrate the interaction of the different components of the control logic. The whole operation is described, showing the flow of commands and the required control interlocks.

The main pushbutton panel is used to prepare the transport for operation. After the power is turned on and the tape is properly threaded, the front panel LOAD pushbutton is pressed. This sets the LOAD flip-flop on the Pushbutton Control modules, generating a RUN NORMAL RNN1 true to the Ramp Generator card. The Ramp Generator outputs a linear ramp voltage to the Capstan Servo Amplifier card, initiating forward tape motion at normal running speed. The Ramp Generator also supplies TAPE RUNNING status true through the Interface Control card to the transport interface. When the load point reflector marker is detected by the respective photo cell, the signal is amplified by the Sensor Amplifier/Driver card and is supplied as LOAD POINT DETECT

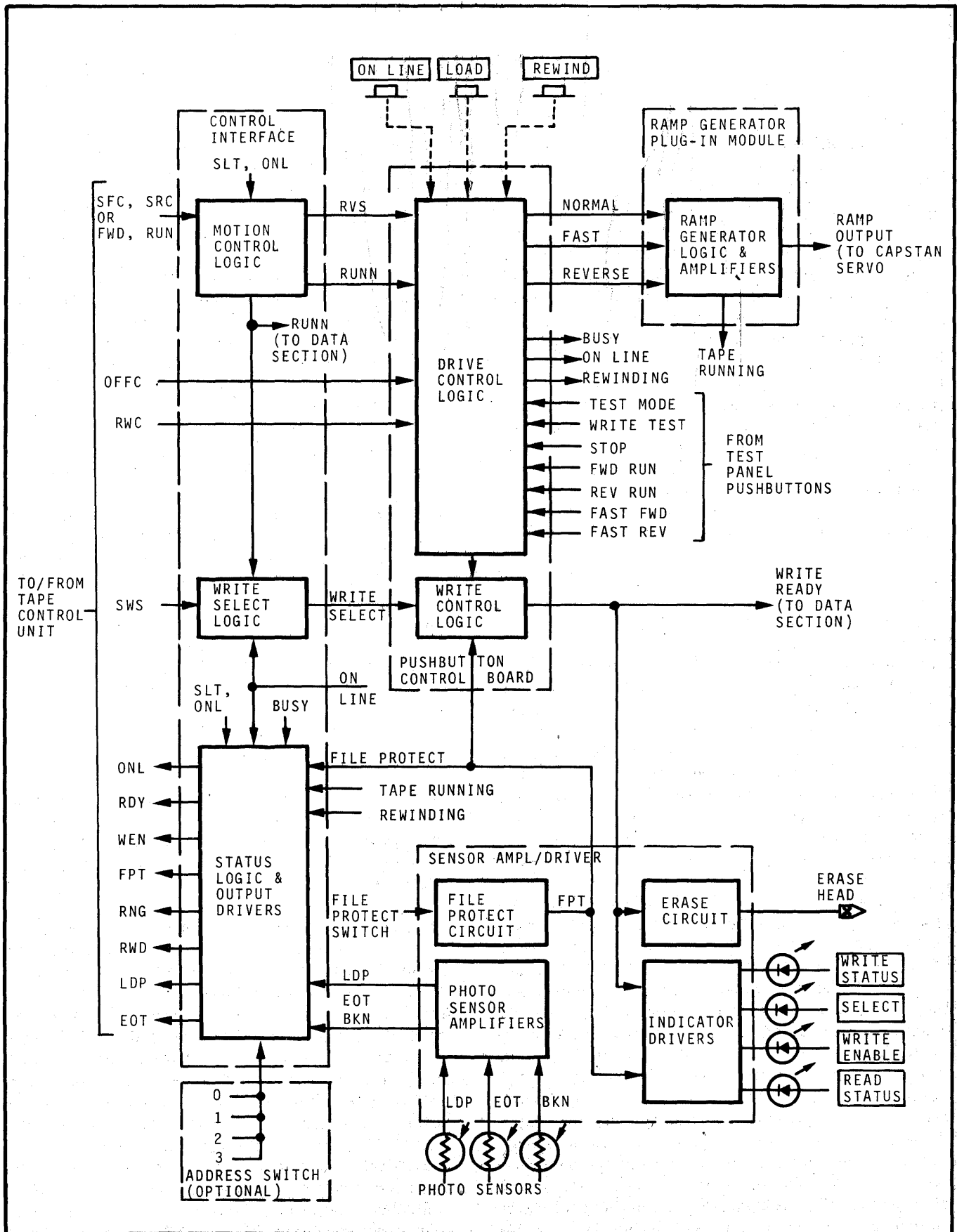


Figure 3-1. Control Logic Block Diagram



(LP) true to the Pushbutton Control module. LOAD POINT true sets the ON TAPE flip-flop to the true condition which terminates the synchronous forward motion by setting RUN NORMAL RNN1 false. The tape is stopped at load point and is properly loaded. Pressing the front panel ON LINE pushbutton now places the transport on line, preparing the transport to respond to interface commands once it is selected by the interface. When the transport is selected (input line SELECT going true) the transport can accept commands from the interface and return the transport status outputs back to the interface. At this time the transport status lines would be in the states shown in Table 3-1.

In addition to the status lines, the front panel ON LINE and SELECT indicators are illuminated, as is the WRITE ENABLE indicator if the supply reel contains a write enable ring.

If the write operation is to be initiated, the interface now supplies SET WRITE STATUS level true and then a SYNCHRONOUS FORWARD COMMAND. The SET WRITE STATUS (SWS) level is sampled on the leading edge of the SYNCHRONOUS FORWARD COMMAND. If the level is true this sets a flip-flop on the Interface Control module and generates WRITE SELECT WSEL true. WRITE SELECT is supplied to the Pushbutton Control module where it generates WRITE READY true provided that FILE PROTECT is false (supplied from the Sensor Amplifier/Driver module), BUSY is false (this signal is generated on the Pushbutton Control and is true whenever the transport is searching for load point and is rewinding), and no reverse command is given. These interlocks ensure that the transport writes data on tape only when the tape is properly loaded, the reel has a write enable ring, and the tape is moving forward at normal running speed. WRITE READY true is supplied to the Sensor Amplifier/Driver module where it turns on write and erase head current drivers and illuminates the WRITE indicator on the front panel. WRITE READY and SELECT 1 (combining ON LINE true and SELECT true) are also supplied to the data electronics card cage where they enable the write and read amplifier stages.

When the tape is properly loaded and not rewinding and WRITE READY is false, a read operation is selected and the Sensor Amplifier/Driver module illuminates the front panel READ indicator.

If WRITE READY does go true the interface supplies the properly formatted data to be written on tape. The write operation can be interrupted in case of broken tape; when the BROKEN TAPE signal is supplied from the Sensor Amplifier/Driver module, all

servos are disabled immediately. Note that an END OF TAPE indication does not terminate a write operation, but leaves it up to the interface to do so. When the write operation is terminated by the interface, the tape is rewound to load point when the interface issues a REWIND COMMAND. Note that the tape cannot be rewound past the load point by a command from the interface. In order to rewind the tape off the takeup reel the transport must be taken off line, either through an interface command or by pressing the front panel ON LINE pushbutton again. Once the transport is off line the front panel REWIND pushbutton can be activated to rewind the tape completely off the takeup reel.

### 3.2.3 TEST PANEL (optional)

The test panel provides a means of exercising, testing, and adjusting the tape transport while it is off line, eliminating the need for a separate test fixture or for the use of valuable computer time. The test panel can initiate forward and reverse tape motions at either normal or high tape speeds. It can also initiate a write test, generating a crystal controlled all-1 test pattern on tape. The test panel also provides indicators for load point, end of tape, and data available. An additional indicator monitors excessive skew, and is used in the aligning of the read/write head when using an 800 cpi skewmaster tape. When the head is properly aligned and the data is written on tape properly the SKEW indicator is extinguished.

The controls and interlocks for the test panel are located on the Pushbutton Control card. The skew detect network is located on the Delay Timing module in the read logic section of the transport. The test panel becomes operational only when the transport is OFF LINE, with the test panel STOP pushbutton depressed. If these conditions are satisfied the test panel pushbuttons are enabled when the TEST MODE pushbutton is pressed.

### 3.2.4 CONTROL LOGIC ADJUSTMENTS

The Kennedy tape transport requires very few adjustments. These are preset in the factory and should not be changed unless there is a very strong reason to believe that they are required. The following adjustments are made on the control logic modules:

<u>Adjustment</u>	<u>Location</u>
Normal running speed	Ramp Generator
Ramp-up time	Ramp Generator
Ramp-down time	Ramp Generator
End of Tape/Beginning of	
Tape sensor adjustment	Sensor/Amplifier Driver

STATUS LINE	STATE	POINT OF ORIGIN
ON LINE	true	Supplied from the load point flip-flop on the Pushbutton Control module, routed through the Interface Control module.
TRANSPORT READY	true	This signal, generated on the Interface Control module, combines BUSY false (meaning the transport is loaded and not rewinding or searching for load point) and SELECT 1 true (meaning the transport is ON LINE and SELECT is true).
TAPE RUNNING	false	This signal goes true on the Ramp Generator when tape motion is initiated.
REWINDING	false	At this time the Rewind flip-flop on the Pushbutton Control module is in the cleared state.
FILE PROTECT		This signal is true if the reel of tape mounted on the supply hub does not contain a write enable ring. It is false if the reel does contain the ring and is available for writing. The signal originates on the Sensor Amplifier/Driver module.
LOAD POINT	true	Since the tape is at load point the Sensor Amplifier/Driver supplies this signal true. When LOAD POINT is true the transport does not acknowledge a REWIND command or a SYNCHRONOUS REVERSE COMMAND from the interface, but must be taken off line and re-wound off tape by using the front panel pushbutton.
WRITE ENABLE		This signal is equivalent to the inverse of the FILE PROTECT signal and is true whenever the other is false; e.g., whenever the supply reel contains a write enable ring. The signal originates on the Interface Control module.
END OF TAPE	false	This signal goes true only when the end of tape reflective marker is detected by the respective photosensor. The signal is supplied to the Sensor Amplifier/Driver module.

**Table 3-1. Transport Status**

The adjustment procedures are outlined in the maintenance section of the manual and in the circuit descriptions of the individual schematics.

### 3.3 SERVO SYSTEM

#### 3.3.1 INTRODUCTION

The transport servo system consists of the electronics and electromechanical components that are required to advance the tape past the magnetic head at accurately controlled speeds while maintaining constant tape tension. The servo system includes two subsections — the capstan servo system, whose function is to drive the tape at accurately controlled speed, and the reel servo system that maintains

constant tape tension. High performance servos are required to drive the reel motors and the capstan drive motor. Considerable power is required, resulting in substantial heat dissipation. This requires the use of heatsinks which are mounted for optimum cooling. All servo components are modular in nature and may be replaced with minimum effort.

#### 3.3.2 REEL SERVOS

Two identical reel servos are employed for the supply and the takeup reels. A block diagram is shown in Figure 3-2. Each reel servo includes a spring loaded buffer arm, a magnetic position sensor coupled to the buffer arm shaft, a servo amplifier, located on the Servo Preamplifier Type 4306 module, power

transistors located on the chassis heatsink, and a high power dc motor. The dc motors operate from  $\pm 24$  volt supplies capable of providing up to 30 amperes peak output current.

The tape tension is maintained by the interaction of the spring loaded buffer arms, the capstan, and the respective reel motors. The magnetic position sensors, called magpots, produce a corrective voltage whenever the buffer arms swing away from the center of their arcs. Each magpot consists of an oscillator circuit, a stationary transformer with a rotating flux linkage, and a discriminator circuit. When the respective buffer arm is in the center of its arc the rotating flux linkage coupled to the buffer arm shaft is adjusted so that the oscillator induces equal voltages into the two stationary secondary coils of the transformer. When equal voltage is induced to both coils the voltage of each cancels out and the total output of the position sensor is 0 volt. When the buffer arm swings away from the center of its arc the rotating flux linkage induces more voltage into one of the secondary coils than the other, generating either positive or negative corrective voltage to the amplifier circuit of the respective reel, located on the Servo Preamplifier Type 4306 module. The magpot corrective voltage is then summed with the modified output of the capstan tachometer to produce the energizing output for the reel motors. The effect of the modified tachometer output is to speed up the response of the reel motors to the capstan motion, to compensate for the lag in the magpot output to tape motion.

The relative effect of the modified tachometer output on the reel motor response is adjusted by a potentiometer located on the Servo Preamplifier module. The adjustment minimizes the buffer arm travel during the ramp-ups to normal running speed by optimizing the interaction of the magpot corrective voltage and the capstan tachometer voltage. Reducing the buffer arm travel prevents the arms from bottoming and ensures accurate ramp speeds.

The summed magpot and modified tachometer voltages are amplified on the Servo Preamplifier module. The amplified output is then supplied to power transistors located on the chassis heatsink whose output energizes the reel motor. The reel motor then produces the proper torque to return the buffer arm to the center of its arc, where the magpot position sensor output is again reduced to zero.

### 3.3.3 CAPSTAN SERVO

The single capstan drive motor is part of a high performance velocity servo system. In addition to the

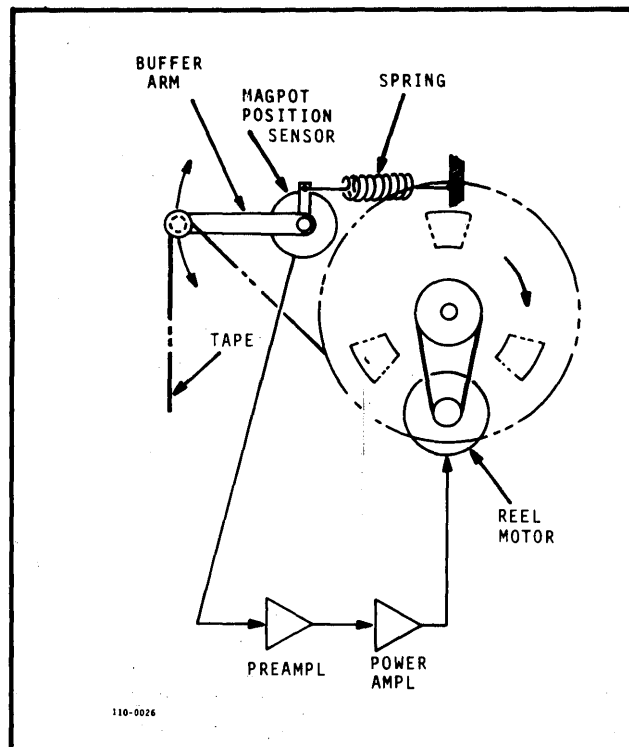


Figure 3-3. Reel Servo System

motor the capstan servo system includes a dc tachometer, coupled to the capstan motor shaft, and the capstan amplifier, located on the Servo Preamplifier Type 4306 module. The linear analog ramp voltage produced by the Ramp Generator card (in the control logic section) is supplied to the Servo Preamplifier module where it is compared with the feedback supplied from the capstan tachometer. Any resulting difference is amplified and is supplied to the capstan power transistors, located on the chassis heatsink. The output of the power transistors energizes the capstan motor, advancing tape at accurately controlled speeds.

### 3.3.4 SERVO SYSTEM ADJUSTMENTS

The following adjustments are preset in the factory and should not be changed unless there is a strong reason to believe that they are required. The adjustment procedures are outlined in the maintenance section of the manual and in the circuit descriptions of the particular schematics.

<u>Adjustment</u>	<u>Location</u>
Capstan servo offset (to prevent capstan creep)	Type 4306 Servo Preamplifier
Buffer arm position	Type 4210 Magpot
Buffer arm travel	Type 4306 Servo Preamplifier

### 3.4 DATA SECTION

#### 3.4.1 INTRODUCTION

The data section includes read and write amplifiers and interface cards providing output drivers and timing controls. Block diagrams are shown in Figures 3-3 and 3-4.

The data section consists of eight circuit cards that plug into the master board. These include a Timing Delay module, a Read Amplifier/Clipping Control card, a pair of Quad Read Amplifier modules, a Four Channel Write Amplifier card, a Five Channel Write Amplifier card, and a Data Terminator card.

#### 3.4.2 WRITE ELECTRONICS

A write amplifier channel is provided for each tape channel. Four such channels and the circuitry common to all write amplifiers are contained on Write Amplifier Type 3848, and the five remaining write amplifier stages are located on Write Amplifier Type 3849. These cards plug into the master board, from which the necessary head connections are made. Two of the channels on Write Amplifier Type 3848 are not used in seven-track operation.

Each write amplifier channel consists of an input buffer, a digitally adjustable deskewing circuit, a clocked flip-flop, and a head driver. The skew characteristics of each read/write head are tested at the factory and the write amplifier switches are set to compensate for the skew, using channel P as the fixed reference channel. Normally the write skew switch settings should never be changed. When a new head is installed the factory furnishes a tag displaying the new deskew switch settings required to compensate for the characteristics of the new head.

The write electronics section also includes the write data strobe buffer which clocks the write amplifier flip-flops, and a write amplifier reset circuit to clear all write amplifier flip-flops. The write amplifier reset is used to write the longitudinal redundancy check character. During a write test mode, initiated by the test panel with the recorder off line, the write electronics generates an all-1 test pattern on tape derived from a crystal controlled reference frequency  $F_R$ , supplied from the Delay Timing module in the read electronics. The test pattern can be used to test the write deskewing, as well as the other functions of the data electronics.

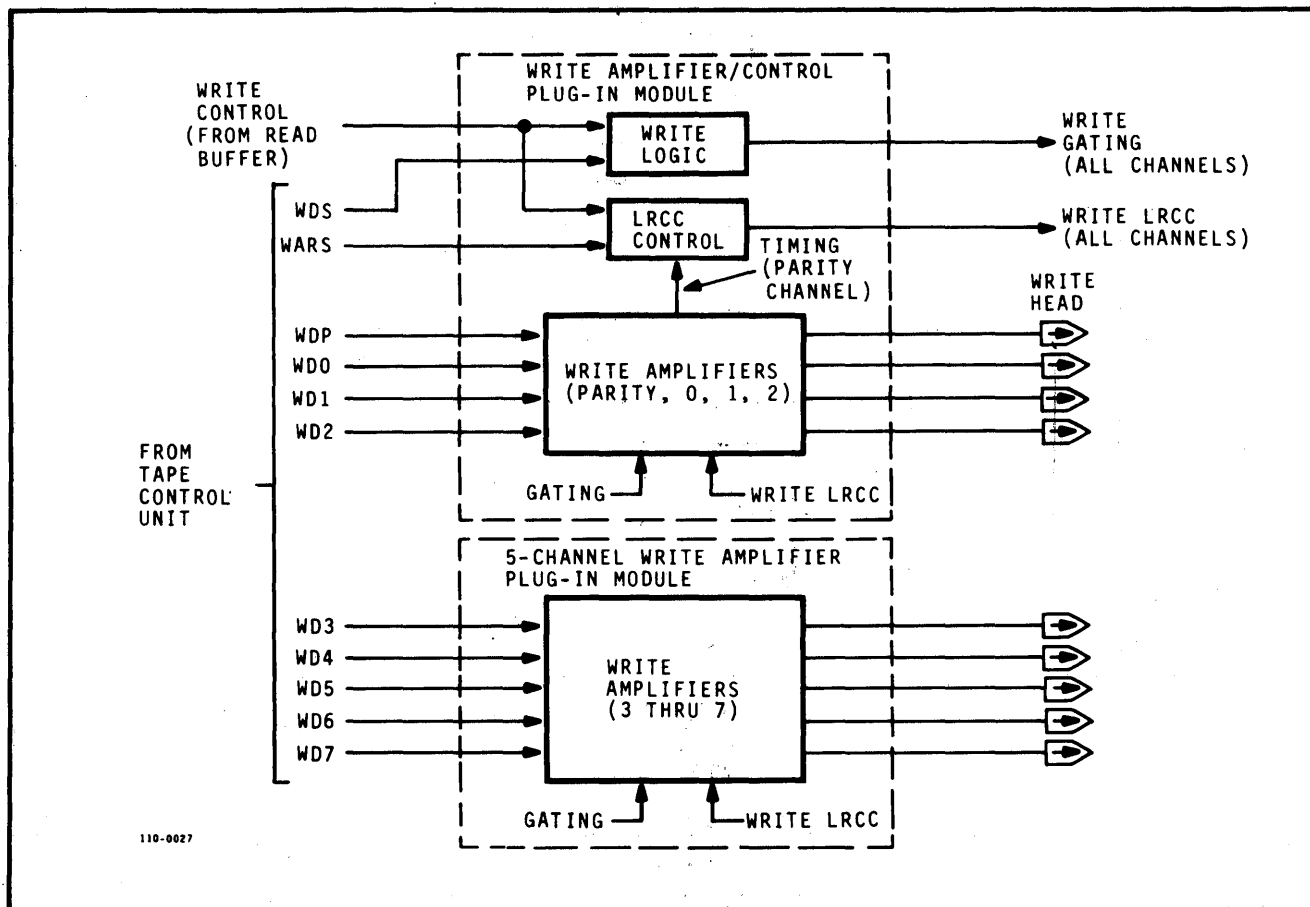
#### 3.4.3 READ ELECTRONICS

The function of the read electronics is to convert the data recovered from the tape into digitized wave forms, deskew it and supply it to the interface with its respective read clock. The read electronics also detect the interrecord gap and excessive skew. The components comprising the read section include the magnetic read head, the Read Pre-amplifier module, Delay Timing module, Read Amplifier/Clipping Control module, and a pair of Quad Read Amplifier modules. Figure 3-4 is a functional block diagram of the read section, showing the general signal flow between the cards. A detailed circuit description of each circuit card accompanies the schematic of the card.

The low level analog signals, on the order of tens of millivolts, are supplied from the read head to the Read Pre-amplifier module where they are linearly amplified to an output voltage (adjusted by a potentiometer for each read pre-amplifier stage) of approximately 9 volts peak to peak in 800 cpi NRZ1 read operation. The amplified analog signals are then supplied to the nine read amplifier stages, eight of which are located on the Quad Read Amplifier modules while that of channel P is located on the Read Amplifier/Clipping Control module. Each Read Amplifier stage includes a peak detection circuit, a filtering network, an output data register, and a pulse generator.

The analog signals from the pre-amplifier are detected only when they exceed the positive or negative clipping levels provided by the Read Amplifier/Clipping Control module. They are then rectified and peak detected, with the resulting digitized waveforms containing negative-going transitions corresponding to the peaks of the input analog signals, e.g., one bits in the NRZ1 code. The digitized waveforms are supplied to a filtering network which eliminates spurious pulses between transitions. The data of each channel is then stored in a register and generates a PULSE OUT to the Delay Timing module. Following the skew delay the Delay Timing card supplies a DATA TRANSFER output to clock the data registers of all nine channels simultaneously, supplying the data character to the interface.

When an error is detected, and the transport is commanded by the interface to reread a block, the read amplifier/clipping levels are switched automatically by the Read Amplifier/Clipping Control module to maximize the recoverability of marginally recorded data. The clipping levels are kept normal on the first reread; on the second reread are switched to lower levels in order to recover possible partial



**Figure 3-3. Write Data Section**

dropouts. If the block is still in error and a third reread is commanded the clipping levels are switched to higher levels to eliminate possible baseline spikes. During read-after-write operations higher clipping levels are used.

The Delay Timing module contains circuitry common to all nine channels. It includes a crystal controlled oscillator and divider network which produces the synchronous clocks used in the skew delay network, the data strobe generation, the gap detect network, and are also supplied to the Write Amplifier Type 3848 module to generate the write test pattern. The crystal controlled clocks ensure high precision in the performance of all data synchronized functions.

#### 3.4.4 DATA SECTION ADJUSTMENTS

These adjustments are preset at the factory and should not be changed unless there is a strong reason to believe that a readjustment is required. The adjustment procedures are outlined in the maintenance section of the manuals and in the circuit descriptions of the individual schematics.

<u>Adjustment</u>	<u>Location</u>
Read preamplifier amplitude	Type 3631 Read Preamplifier
Skew alignment	Read/write head, write amplifiers

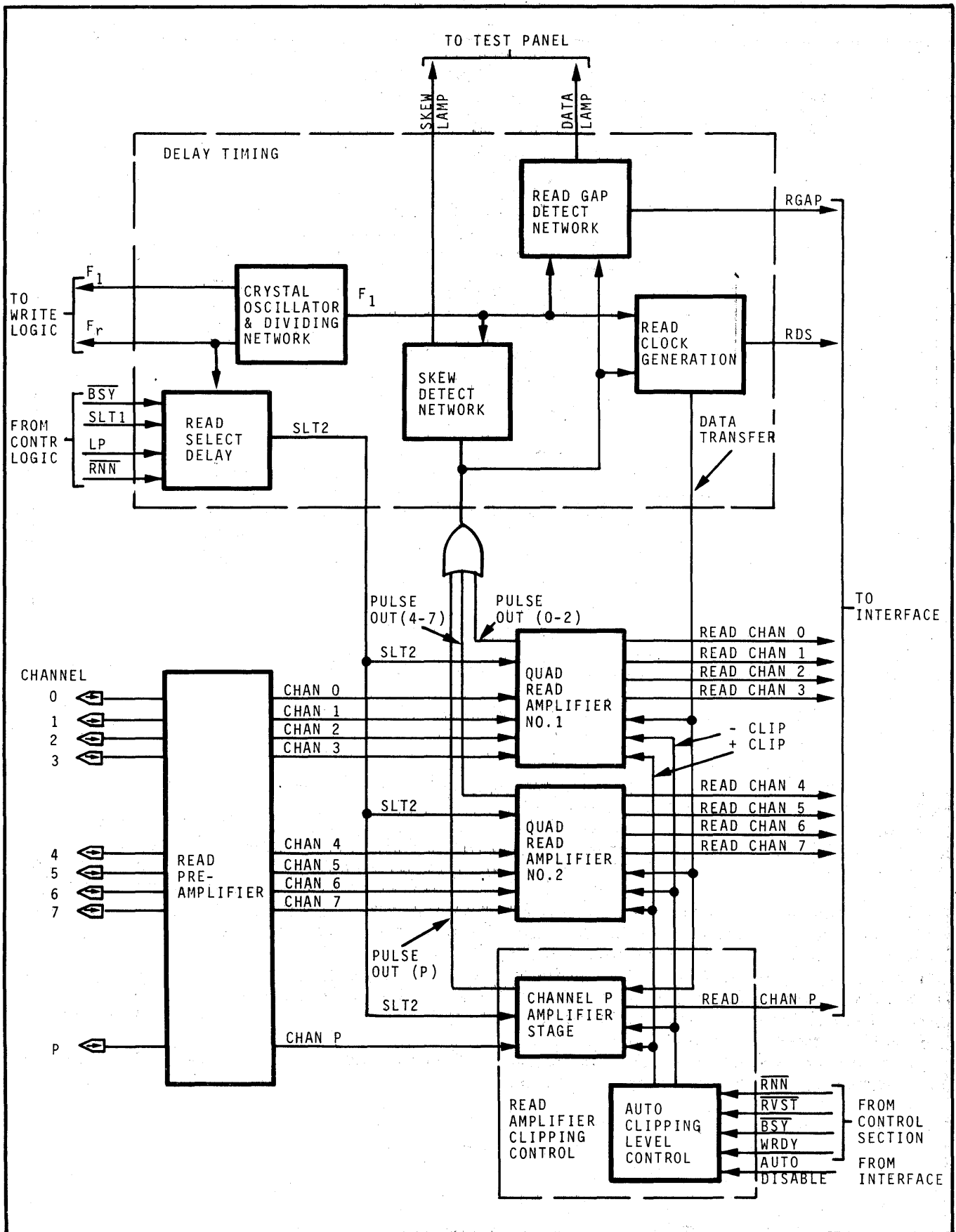


Figure 3-4. Read Data Section

**SECTION IV**  
**MAINTENANCE INSTRUCTIONS**



## SECTION IV

### MAINTENANCE INSTRUCTIONS

#### 4.1 GENERAL

Kennedy Company tape transports are highly reliable precision instruments which will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The units require very few adjustments and these should not be performed unless there is strong reason to believe they are required. All electrical adjustments are preset at the factory and should not require readjustment except after long periods of time.

#### 4.2 PREVENTIVE MAINTENANCE

To assure continuing trouble-free operation a preventive maintenance schedule should be kept. The items involved are few and simple but very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport so a rigid schedule applying to all machines is difficult to define. The recommended periods below apply to units in constant operation in ordinary environments. They should be modified if experience shows other periods are more suitable.

##### 4.2.1 DAILY CHECK

Visually check the machine for cleanliness and obvious misadjustment. If items in the tape path show evidence of dirt or oxide accumulation, clean thoroughly.

##### 4.2.2 CLEANING

All items in the tape path must be kept scrupulously clean. This is particularly true of the head and guides. The inside of the dust cover must not be allowed to accumulate dirt since transfer to the tape will cause malfunction.

In cleaning it is important to be thorough yet gentle and to avoid certain dangerous practices.

##### 4.2.2.1 Head Cleaning

Oxide or dirt accumulations on the head surfaces are removed using a mild organic solvent and a swab. Q tips are convenient for this use but must be used

with caution. Be sure the wooden portion does not contact head surfaces. Figure 4-1 shows access to the head by lifting the face shield.

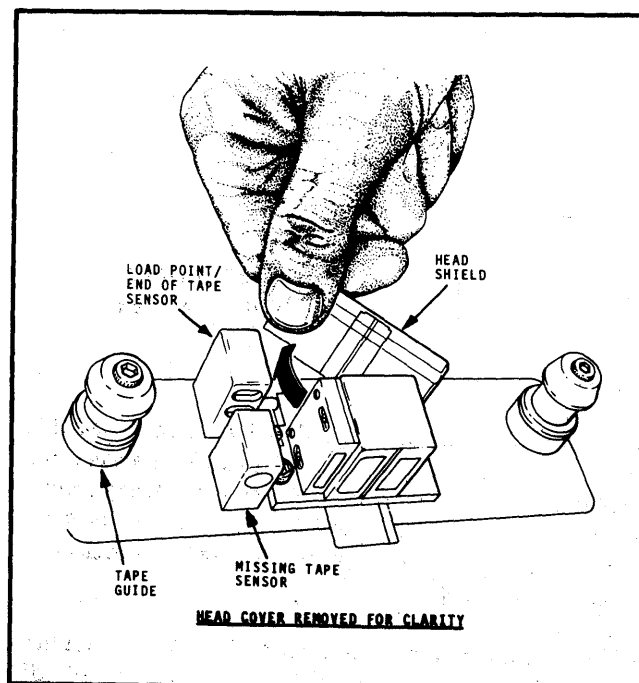
An ideal solvent is 1,1,1 trichloroethane contained in Kennedy K21 maintenance kit. However, others such as isopropyl alcohol will do.

- DO NOT USE - acetone or lacquer thinner  
 - aerosol spray cans  
 - rubbing alcohol

Do not use an excess of any solvent, and be extremely careful not to allow solvent to penetrate ball bearings of tension rollers, capstan motor, etc., since it will destroy their lubrication.

##### 4.2.2.2 Tape Path Cleaning

Other items in the tape path should be cleaned at the same time as the magnetic head. These include:



**Figure 4-1. Opening of Head Shield.**

Tension rollers  
Tape guides  
Capstan  
Tape cleaner surface

The techniques are similar to those outlined above for head cleaning.

#### 4.2.2.3 Other Cleaning

For removing accumulations of dust inside the dust cover or elsewhere in the unit, use of a vacuum cleaner is recommended. Compressed air may be used if caution is exercised to avoid blowing dirt into bearings. Antistatic cleaners are available for cleaning the plexiglass dust cover window.

#### 4.2.3 VISUAL CHECK

Check visually to determine if all appears to be right with the machine. It is helpful to run tape forward and reverse observing smooth tape motion, proper tension arm operation, etc. It is well to remember that if things look right they probably are right, and the converse.

#### 4.3 ROUTINE ADJUSTMENT

There are no routine adjustments. Need for adjustment will be manifest if malfunction occurs. Under normal circumstances adjustment will be more likely to cause trouble than prevent it.

#### 4.4 LUBRICATION

No bearing lubrication is required. All bearings are lubricated for life and introduction of oil may destroy their lubrication.

#### 4.5 WEAR

Magnetic tape is an abrasive and in time wear will be noted on items over which the oxide surface slides.

##### 4.5.1 HEAD WEAR

Head wear is generally signaled by an increase in error rate. Confirmation is a sizable increase in output voltage, measured at the preamplifier, from the read head. When the head becomes worn it must be replaced. Head replacement procedure is outlined in paragraph 4.8.1.

Worn heads usually can be resurfaced at least once if returned to the factory. This is more economical than replacement with a new head. Consult Section V for details of head return.

##### 4.5.2 GUIDE WEAR

Guides wear principally at the point of contact with the front guide surface. Although guides are hard anodized with a coating equivalent to sapphire, in time grooves will appear. Since guides are symmetrical it is only necessary to loosen the guide mounting screw, rotate the guide, and tighten to present an unworn surface to the tape.

##### 4.5.3 REEL HUBS

Quick release hubs are adjustable to assure a firm clamping action. They are designed to make it impossible to mount a reel in a wrong or cocked position. If the locking action should become weak, the hub may be adjusted by tightening the nut at the rear end of the hub shaft. O ring clamps used in the hub may tend to hang up after long periods of use. This can be corrected as follows:

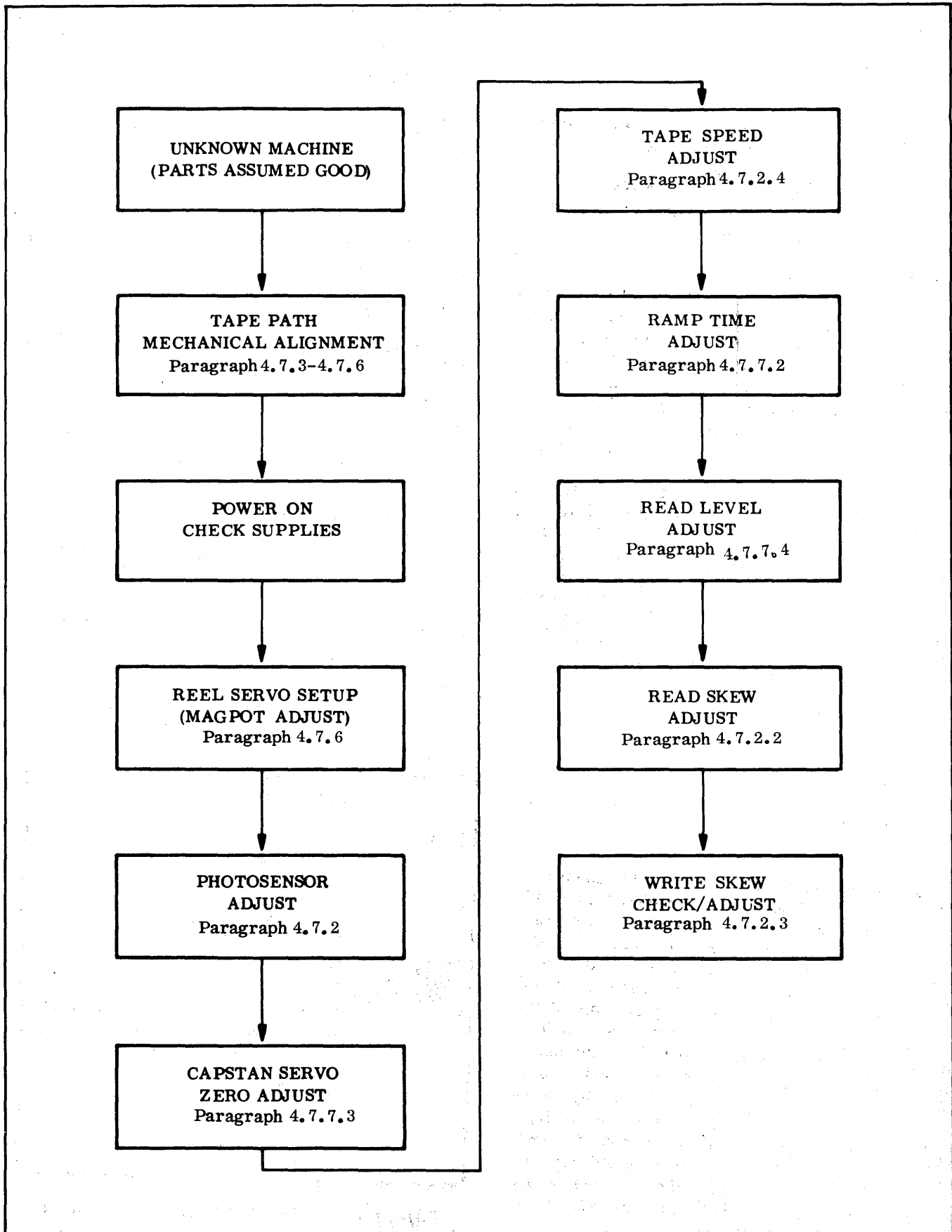
- a. Remove O ring from hub.
- b. Clean thoroughly with mild solvent.
- c. Lubricate ring with silicone grease. Wipe off as thoroughly as possible, leaving a light lubricating film.
- d. Snap O ring back in place.

#### 4.6 PERIODIC INSPECTION

At regular intervals, approximately every two months, it is advisable to make a more thorough check of machine operating parameters. This will insure that no progressive degradation will go unnoticed. Of great assistance in making these checks is the test panel (standard equipment on Model 9000, optional with Models 9700 and 9800) which allows control of tape motion off line for test purposes and provides certain useful indicators and test signals as well. The test panel connector plugs into a connector on the control electronics. It does not require that interface cables be disconnected. Using the test panel or other appropriate means, the following should be checked periodically.

Tape speed  
Ramp times  
Ramp level  
Skew  
Photosensor adjustment  
Servo zero adjustment

The suggested adjustment sequence is shown in Table 4-1.



**Table 4-1. Adjustment Sequence**

## 4.7 CHECKS and ADJUSTMENTS

### 4.7.1 TEST PANEL (optional)

All adjustments described below are preset at the factory and should not be performed unless there is a strong reason to believe they are required. When the adjustments have to be performed it is recommended that the test panel be used. The test panel provides a flexible means of exercising the tape deck off-line without requiring computer time. It can initiate tape motion in normal and high speeds, in forward and reverse directions, as required for the particular adjustment. In addition, it includes a skew indicator to monitor excessive skew that should be used in the head alignment procedure described below, and a write test mode that automatically generates an all-1 test pattern on tape. The test panel also includes load point, end of tape, and data available indicators. The test panel pushbuttons and indicators are described on page 1-4 of the manual.

In order to use the test panel the transport must be off line and the test panel STOP pushbutton must be depressed. The recorder is then placed under test panel control by depressing the TEST MODE pushbutton. If all interlocks are satisfied the TEST MODE indicator is then illuminated and the other pushbuttons on the test panel become active. Any tape motion can then be commanded by the respective pushbutton and can be terminated by the STOP pushbutton.

### 4.7.2 SKEW ADJUSTMENT

#### 4.7.2.1 Introduction

The skew adjustment on this model is simplified considerably by the use of the test panel. The SKEW light on the test panel indicates excessive skew when illuminated, while the adjacent skew test point supplies the wire-OR'd pulse outputs of all the read amplifier stages, displaying the entire range of bit scatter. When excessive skew is detected, follow the skew adjustment procedure outlined below. Normally only the read skew adjustment should be made, since the write amplifiers are digitally deskewed in the factory, using the write amplifier switches to control the write skew delay. The switch settings should never have to be changed under normal use. When the magnetic head needs replacement, the factory supplied head is accompanied by a tag displaying the new write amplifier switch positions required to match the new head characteristics.

#### 4.7.2.2 Read Skew Adjustment

- Mount a master skew tape on the supply hub.
- Adjust skew adjusting screw (Figure 4-2) in the head mounting plate until the skew lamp is extinguished. Alternately an oscilloscope probe may be connected to the test panel skew test point, displaying the wire-OR'd read peaks. The read skew should then be adjusted until minimum peak scatter is detected.

#### 4.7.2.3 Write Skew Adjustment

As mentioned above, this adjustment is made in the factory and normally should not be changed. Should a readjustment be required, follow these steps:

- Place the write amplifier card containing the channel to be adjusted on an extender.
- Mount a blank reel of tape on the supply hub, and advance to load point.
- Connect channel 1 of a dual channel oscilloscope to test point P(C) on the read pre-amplifier card.

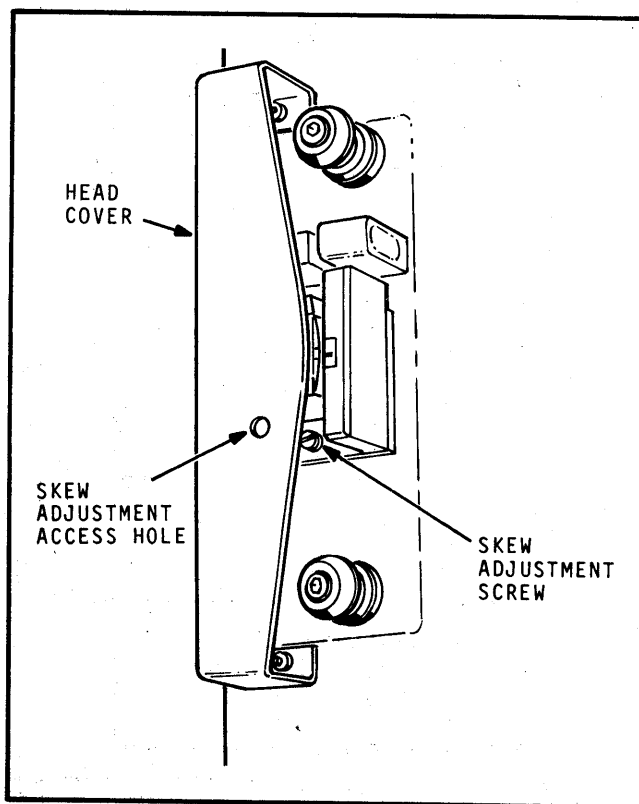


Figure 4-2. Head Skew Adjustment

- d. Connect scope probe channel 2 to test point channel 7(1) of the read preamplifier. Select added sweep, synchronizing on channel 1 only, positive slope trigger (Figure 4-4).
- e. Place recorder in the write test mode by first pressing the TEST MODE pushbutton on the test panel, and then the WRITE TEST pushbutton. The recorder will then write consecutive all 1's pattern.
- f. Adjust the channel 7 switches on the write amplifier card (see Figure 4-3) until the channel P and channel 7 traces coincide.
- g. Repeat the above steps for the remaining channels, leaving the scope probe on channel P as the reference channel.
- h. Recheck the read skew following the procedure outlined in the preceding paragraph.

#### 4.7.2.4 Tape Speed Check

With master skew tape mounted and scope connected (paragraph 4.7.2.2), check tape speed by measuring the time of one sine wave period, or the time between corresponding points in the sine wave. In NRZ1 recording this time is equal to two bit periods.

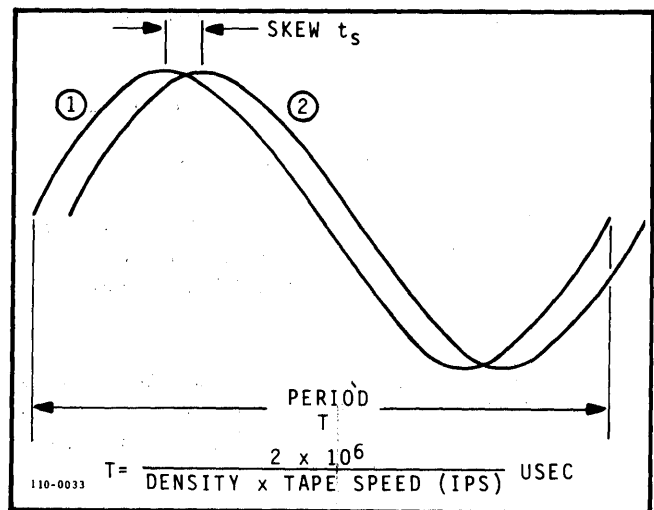


Figure 4-4. Skew Adjustment Waveforms

Measured time in microseconds should be

$$t = \frac{2 \times 10^6}{\text{density} \times \text{tape speed (ips)}} \mu\text{sec}$$

#### 4.7.3 TAPE PATH CHECKS

It is important to maintain a correct tape path at all times. Items influencing tape path are: tension arm roller guides, tape guides, and direction-reversing idler. All must be correctly set for satisfactory operation. To check tape path, proceed as follows:

- a. Observe that tape enters both reels without touching reel flanges.
- b. Depress the spring-loaded (inside) portion of the top tape guide. Tape should have a slight tendency to follow the guide.
- c. Operate the transport in alternate forward and reverse direction, moving about 1 foot of tape. The tape should stay centered on direction-reversing idler in both directions.
- d. If these checks indicate need for adjustment, the following procedure should be used.

#### 4.7.4 TAPE PATH ADJUSTMENTS

##### 4.7.4.1 Tension Arm Roller Guide

(Symptom: Tape touches reel flange.)

- a. Be sure reel installed is not warped.

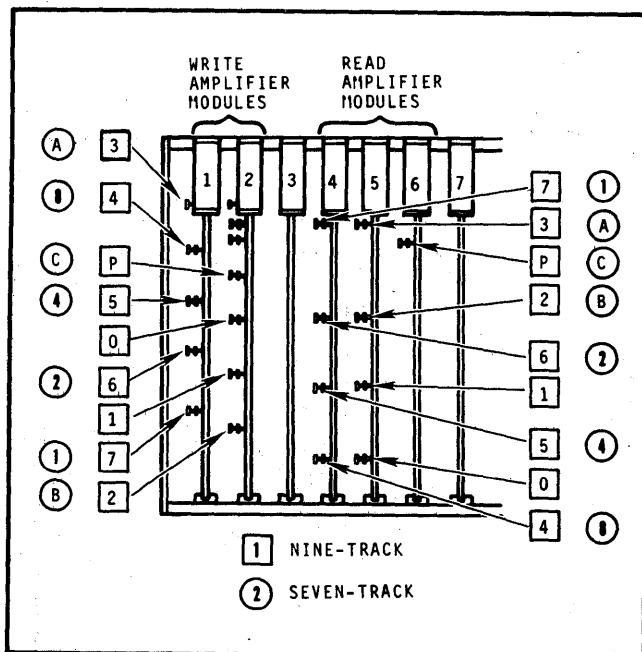


Figure 4-3. Write and Read Amplifier Channel Locations

- b. Remove tension arm roller guide nearest reel.
- c. Insert a 4 inch rod of 0.187 inch diameter ground stock in place of the roller guide shaft and thread tape over the rod.
- d. Run tape forward continuously. Hold the end of the rod and loosen lock screw (A, Figure 4-5). This will allow the rod to be angularly adjusted.
- e. Adjust the position of the rod so that tape is guided into the center of the reel without touching reel flanges. Tighten lock screw.
- f. Remove rod and replace roller guide (B). Do not change setting established in step e. Roller guide height should be set so tape is in center of reel. On most decks the tape edge should be set to 0.434 inch from the painted surface, a measurement that can easily be made with the tape height gauge included in the K21 maintenance kit. In recorders with cast decks this measurement cannot be made, and tape height should simply be adjusted to center of reel. The roller height adjustment on all decks should be made as follows:
  - (1) Pull roller guide outward so tape nearly touches the outside edge of the reel.
  - (2) Partially tighten roller guide retaining screw (C) until the roller guide shaft cannot be moved by hand.

- (3) Using the adjustment nut and washer (D), (No. 10 flat washer and 10-32 nut should be used), move the roller guide inward until the tape is at the center of the reel (0.434 inch on most decks).
- (4) Lock the roller guide retaining screw (C); remove adjustment nut and washer.

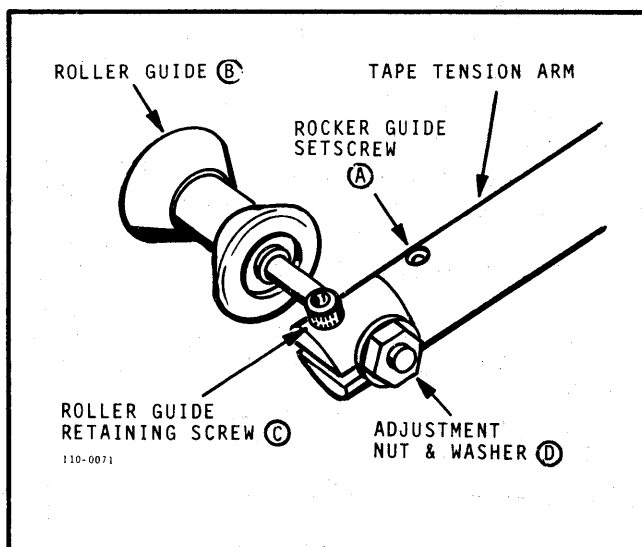
#### 4.7.4.2 Direction-Reversing Idler

(Symptom: Tape moves back and forth on direction-reversing idler when run alternately forward and reverse.)

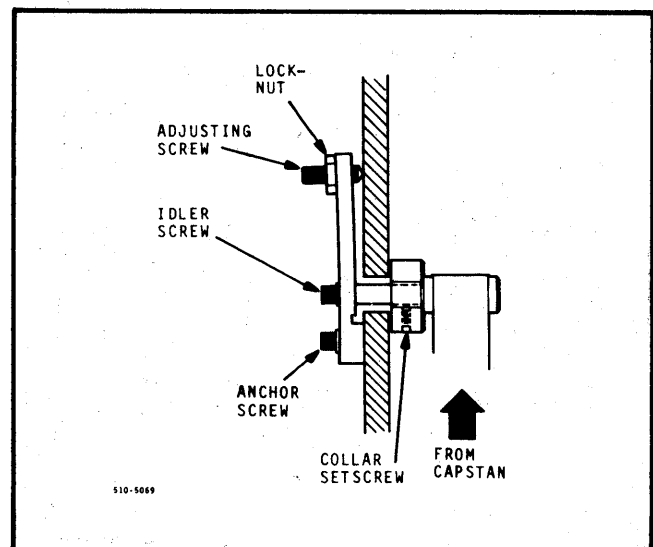
- a. Loosen locknut on idler adjusting screw (see Figure 4-6).
- b. Loosen setscrew in idler collar.
- c. Run tape alternately forward and reverse.
- d. Tighten locknut and idler collar.

#### 4.7.5 TAPE TENSION CHECK

- a. Turn power off and remove tape from machine.
- b. Using a spring scale, measure return force of tension arm at the approximate center of its arc. Force should be  $16 \pm 2$  ounces ( $450 \pm 55$  grams) corresponding to tape tension of  $8 \pm 1$  ounces ( $225 \pm 27$  grams).



**Figure 4-5. Roller Guide Adjustment**



**Figure 4-6. Idler Adjustment**

## NOTE

Spring anchor adjustment can be varied to produce small corrections. If a large correction is required, tension arm spring should be replaced.

- c. To adjust spring tension, loosen anchor lug nut slightly and adjust anchor for correct reading on spring scale.

## 4.7.6 TENSION ARM POSITION CHECK

When the transport is at rest with a tape loaded, the tension arms should be located in the approximate center of their respective arcs. If the arms drift away from their proper position they may hit the end of their arcs when the tape ramps up to running speed. The magpot position sensors, coupled to the buffer arms as shown in Figure 4-7, control the position of the arms. When the tension arms drift away from their proper position the magpots should be adjusted as follows:

Magpot Adjustment

The magpot should be adjusted so that when the respective tension arm is in the center of its arc the

corrective voltage output by the magpot is 0 volt. When the arm swings away from the center of its arc the voltage put out by the magpot should be either positive or negative, depending on the position of the arm. The adjustment procedure is as follows:

- a. Turn the transport power on.
- b. Remove the shell from the magpot to be adjusted (as shown in Figure 4-7).
- c. Loosen the transformer linkage retaining screw (point A on Figure 4-7) so linkage can be turned on the tension arm shaft.
- d. Connect an oscilloscope probe to the magpot output. A convenient point is resistor R8 (point B on Figure 4-7).
- e. Move the tension arm to the approximate center of its arc and turn the linkage on the tension arm shaft so that the output voltage of the oscillator (measured at R8) is 0 volt.
- f. Ascertain that when tension arm is in the rest position (under spring pull only) the output voltage of the magpot is between -5

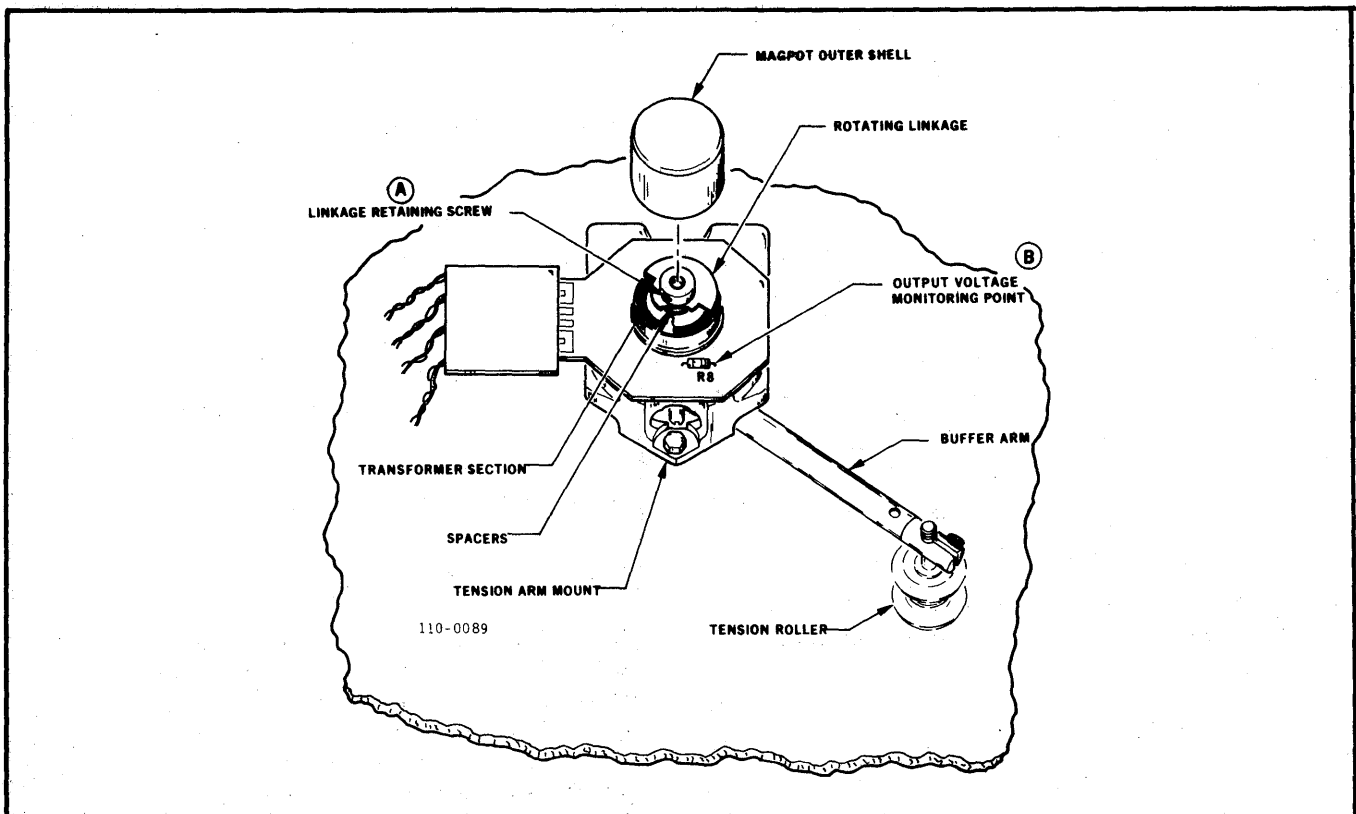


Figure 4-7. Magpot Position Sensor



and -6 volts. When the buffer arm is at the other extreme of its arc the magpot output voltage should be between +5 and +6 volts. Though the total output voltage swing of the magpot is not critical, it should be between 10 and 12 volts. This amplitude is determined by the distance of the rotating linkage from the stationary transformer section and is permanently fixed in the factory by using plastic spacers. The amplitude swing can be readjusted by moving the rotating flux linkage toward the stationary transformer section to increase the amplitude or away from the stationary section to decrease the amplitude.

- g. After adjusting the rotating linkage position lock the linkage retaining screw and replace the magpot outer shell. It is recommended that the retaining screw be secured with Loctite.

#### 4.7.7 ELECTRICAL ADJUSTMENTS

##### 4.7.7.1 Introduction

The electrical adjustments outlined below are also conveniently located on the circuit descriptions of the individual circuit boards on which the adjustments are performed.

##### 4.7.7.2 Control Section Adjustments

###### Speed Adjustment

The tape speed adjustment is performed on the Ramp Generator card as described in paragraph 4.4.2.4.

###### Ramp Time Adjustments

The ramp time adjustments are also performed on the Ramp Generator module. The stop and start ramps should be adjusted according to the formula

$$\text{ramp time} = \frac{0.375 \text{ millisecond}}{\text{transport speed}}$$

Consequently in transports with synchronous running speeds of 25 inches per second the start and stop ramps should each be

$$\frac{0.375}{25} = 15 \text{ milliseconds}$$

and the ramp time varies inversely with speed. The adjustment procedure is as follows:

- a. Arrange the input signals to the tape transport to start and stop the transport repeatedly. The rate must be such as to allow full ramp time.
- b. Adjust start ramp potentiometer R3 on the Ramp Generator card for the required time, observing the ramp output at test point A of the Ramp Generator. The ramp start time is measured from 0 volt to the maximum output voltage.
- c. Adjust the stop ramp potentiometer R4 for the required time. The stop ramp time is measured from maximum volts to 0 volt.

##### Beginning of Tape, End of Tape Sensor Adjustment

This adjustment is performed on the Sensor Amplifier/Driver Type 3844 module. The adjustment becomes necessary if the Beginning of Tape or End of Tape markers are not detected by their respective sensors. To adjust the sensors, turn potentiometer R16 on the Sensor Amplifier/Driver card until the voltage between test points E and F on that card measures 0 volt.

##### 4.7.7.3 Servo System Adjustments

###### Capstan Creep Adjustment

This adjustment is performed on the Servo Preamplifier Type 4306 when capstan creep is observed during standstill. To adjust, follow these steps:

- a. Connect oscilloscope to observe voltage at the amplifier output. A convenient point is output pin X.
- b. With transport on line and loaded but in a stopped condition, adjust R56 so that a straight-line trace is produced. Use 0.5v/cm scale on oscilloscope.
- c. Observe that capstan does not rotate.

###### Buffer Arm Travel Adjustment

This adjustment is performed on the Servo Preamplifier Type 4306 module, and is required when the buffer arms exhibit excessive travel during ramp-ups to running speed. In that case potentiometer R57 or R58 on the Servo Preamplifier Type 4306 should be adjusted to minimize buffer arm travel during the ramps, preventing the arm from bottoming and overshooting. To adjust, follow these steps:

- a. Load a full reel of tape on the supply reel.
- b. With the transport off line, press the test panel TEST MODE pushbutton, placing the transport under the test panel control.
- c. Alternately press the FORWARD RUN and then the REVERSE RUN pushbuttons on the test panel, initiating synchronous forward and reverse tape motions.
- d. Adjust potentiometer R57 until the travel of the SUPPLY buffer arm is at a minimum during ramp-ups and ramp-downs.
- e. Repeat the above procedure for the TAKEUP Servo Preamplifier, adjusting R58.

#### 4.7.7.4 Data Section Adjustments

The data read/write deskewing adjustments are described in paragraph 4.7.2 of this section. The only other adjustment required is the output voltage adjustment of the read preamplifier stages. This adjustment should be made after the transport speed has been checked and, if necessary, adjusted (see paragraph 4.7.2.4). The output voltage of each read preamplifier stage should then be adjusted, using the potentiometer associated with that stage, until the output voltage is 9 volts peak to peak in 800 cpi operation.

### 4.8 PARTS REPLACEMENT

Over extended periods replacement of certain parts may be required. While disassembly and assembly are for the most part obvious upon inspection, the following information will simplify repair procedures for certain parts.

#### 4.8.1 HEAD REPLACEMENT

- a. Unplug head and remove screws holding head connectors to deck.
- b. Remove head cover.
- c. Remove head mounting screw.
- d. Pass connectors through hole provided in the deck.

#### NOTE

Do not remove head from head mounting plate. Replacement heads are furnished with mounting.

- e. Replace head and connectors. Make certain adjusting screw is aligned with hole provided on the deck.
- f. For procedures to deskew head and adjust write amplifiers, follow procedures given earlier in this section.

#### 4.8.2 CAPSTAN MOTOR REPLACEMENT

- a. Unplug motor.
- b. Remove capstan locking screw.
- c. Pull capstan off shaft. (This requires the use of a special puller available from the factory on purchase or loan.)
- d. Remove four motor mounting screws and motor.
- e. Replace the motor, being careful to orient motor mounting so that the motor brush holders do not strike the control card cage.
- f. Replace capstan and tighten capstan lock-screws.

#### 4.8.3 REEL MOTOR REPLACEMENT

- a. Disconnect terminal block from cable.
- b. Remove four motor mounting nuts and reel motor.
- c. Replace motor.
- d. Adjust belt tension so that when belt is squeezed in the center about 1/4 inch (6.3 mm) deflection occurs.

#### 4.8.4 TENSION MAGPOT REPLACEMENT

- a. Remove buffer arm roller guide.
- b. Unplug magpot cable.
- c. Remove spring from anchor.
- d. Remove two mounting screws to free the magpot assembly.

#### NOTE

Replacement magpot assemblies are supplied prealigned. If position alignment is required see paragraph 4.4.6.

- e. Install replacement assembly.
- f. Check tape path. If adjustment is needed see paragraph 4.7.4.

#### 4.8.5 VOLTAGE REGULATOR/SERVO POWER ASSEMBLY REPLACEMENT

- a. Remove eight mounting screws.
- b. Unplug molex connectors from the master board.
- c. Plug in replacement unit and reassemble.

#### 4.9 TEST PANEL USE

The test panel, standard equipment in Model 9000, is packaged in a box and supplied as Model 9900 for use with Model 9700/9800 transports (see Figure 4-8). Its use is identical in all transports.

A diagrammatic representation of the controls and indicators, together with brief descriptions of their purpose, is given in Figure 4-9. It will be noted that the box allows tape to be moved in either direction, normal speed or fast speed. Motion is interlocked to prevent running off reels at either end. Additionally, the 9900 allows writing an all ones pattern on the tape and provides indicators for skew, data, load point, and EOT.

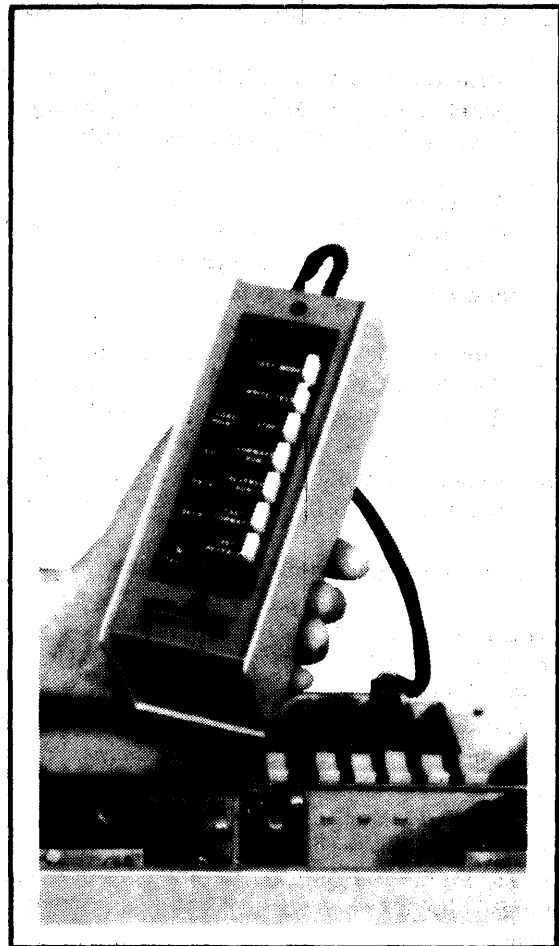
The test panel is intended to be used in checking the machine when off line or, for that matter, when completely isolated from the operating system. The controls provided are useful under these circumstances but under normal operation they would be confusing and invite possible operator error. For this reason the panel is accessible only by opening a sliding cover on Model 9800.

Because of the special nature of phase encoded and dual density transports, use of the test panel is slightly modified. The above discussion applies to NRZI only. Test panel use with other units is discussed in portions of the manual applicable to these types.

##### 4.9.1 OPERATION

The test panel becomes operational only in test mode, selected by pressing the alternate action TEST MODE pushbutton. For the TEST MODE button to be operational the machine must be:

- a. Off line
- b. STOP must be depressed



**Figure 4-8. Test Panel Installation**

Test mode is terminated by either:

- a. Pressing alternate action TEST MODE button
- b. Pressing ON LINE pushbutton

A characteristic of Series 9000 electronics is that when LOAD is pressed the machine feeds forward to load point. If tape is already wound on the machine and the load point marker has been passed, search will continue to end of tape unless REWIND is pressed. This characteristic is sometimes troublesome when servicing the machine. Under these circumstances, pressing TEST MODE will terminate search and induce an ON TAPE status in the control electronics. If ON LINE is subsequently pressed, the ON TAPE status is retained. This feature can be adapted to allow power turn-off while tape is loaded.

When using tape motion pushbuttons the STOP button should be pressed between changes in motion speed or direction. No harm will result if this is not done, but on occasion switch bounce will cause the command not to be recognized and the last motion signaled will be retained.

#### 4.9.2 SKEW INDICATOR

An LED indicator is provided which flashes if skew is being encountered. Logic in the data section detects skew to two different criteria and lights the indicator. The skew gate in the NRZI read electronics is normally open for 50 percent of one character time (see discussion of read electronics). If pulses fall outside the skew gate they trigger the indicator. In test mode the skew gate is narrowed to 5/32 of a character time. An all ones pattern on a properly adjusted machine should fall inside the shortened gate. A tape with random data suffers from pulse crowding effects and will not, in general, fall inside the gate. Thus in test mode the skew indicator is valid for an all ones data pattern only. In normal operation it is valid for all data patterns.

#### 4.9.3 DATA INDICATOR

The DATA INDICATOR is illuminated when the tape being read has data written on it of a level sufficient to activate the read electronics. It of course blinks when reading gapped data.

#### 4.9.4 LOAD POINT INDICATOR

This LED lights when load point is sensed.

#### 4.9.5 EOT INDICATOR

EOT is indicated when the end of tape marker is sensed in the forward direction and remains true until it is passed in the reverse direction. All indicators operate whether or not test mode is selected.

**SECTION V**  
**PARTS IDENTIFICATION**

## SECTION V

### PARTS IDENTIFICATION

#### 5.1 SPARE PARTS ORDERING INFORMATION

This section describes the replaceable parts in your tape unit which are available only from Kennedy Company. Many parts of the unit are common commercial parts which can be obtained directly from the manufacturer.

The serial number and part number of the tape unit are the keys to numerous engineering details applying to your unit. These numbers are located on the serial number tag located on the rear panel of the unit. When ordering spare parts, accessories, or tools, always specify the serial number and part number of your unit.

Changes to Kennedy units are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. If a part you have ordered has been replaced by a new part, a Kennedy representative will contact you concerning any change in part number.

All parts orders should be addressed directly to Kennedy Company, Parts Order Department, 540 West Woodbury Road, Altadena, Ca 91001, telephone (213) 798-0953, TWX 910-588-3751.

#### 5.2 IN-WARRANTY REPAIR PARTS ORDERING INFORMATION

Repair parts for in-warranty units are made available on an exchange basis through the Kennedy Company Customer Engineering Department.

The serial number and part number of the tape unit are necessary in order to insure shipment of the proper replacement parts.

All inquiries should be directed to Kennedy Company, Customer Engineering Department, 540 West Woodbury Road, Altadena, Ca 91001, telephone (213) 798-0953, TWX 910-588-3751.

#### 5.3 EXPORT ORDERS

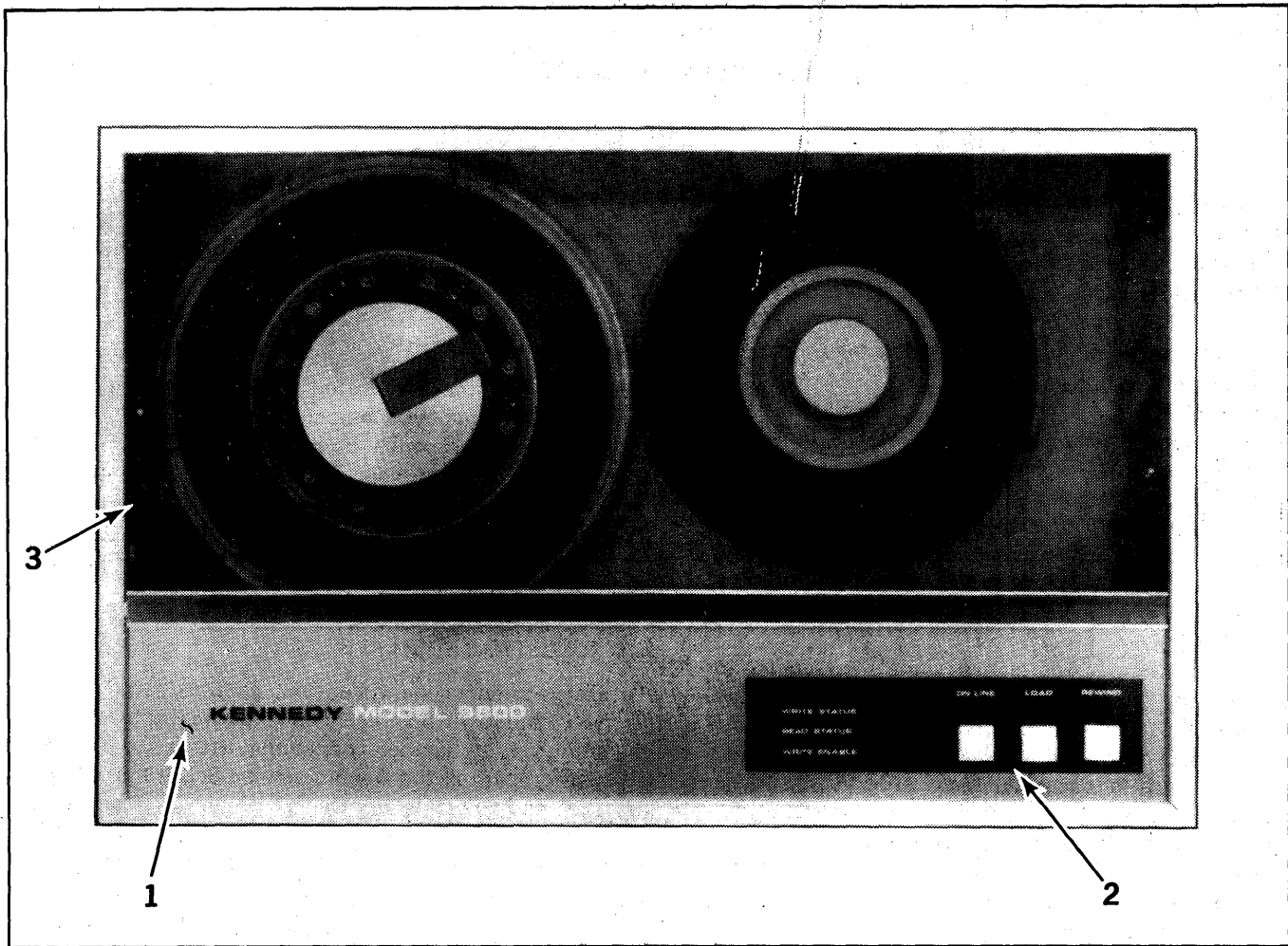
Customers outside the United States and Canada are served by Kennedy Company international sales agents. All correspondence regarding your tape unit should be directed to your sales agent. If you prefer, correspondence may be addressed directly to Kennedy Company, Parts Order Department, 540 West Woodbury Road, Altadena, Ca 91001, TWX 910-588-3751, cable KENNEDYCO.

#### 5.4 ILLUSTRATED PARTS LIST

To assist in parts identification, an illustrated parts list is included with references to photographs of the machine. Part numbers beginning with an 8 or 198 are listed again in the Recommended Spare Parts List at the end of this section. Kennedy Company recommends that these parts be ordered as spares to minimize machine downtime due to equipment failure. Certain parts on this list have no quantity indicated. We recommend ordering one of each such parts for remote installations where parts delivery is time consuming.

#### 5.5 FIELD KITS

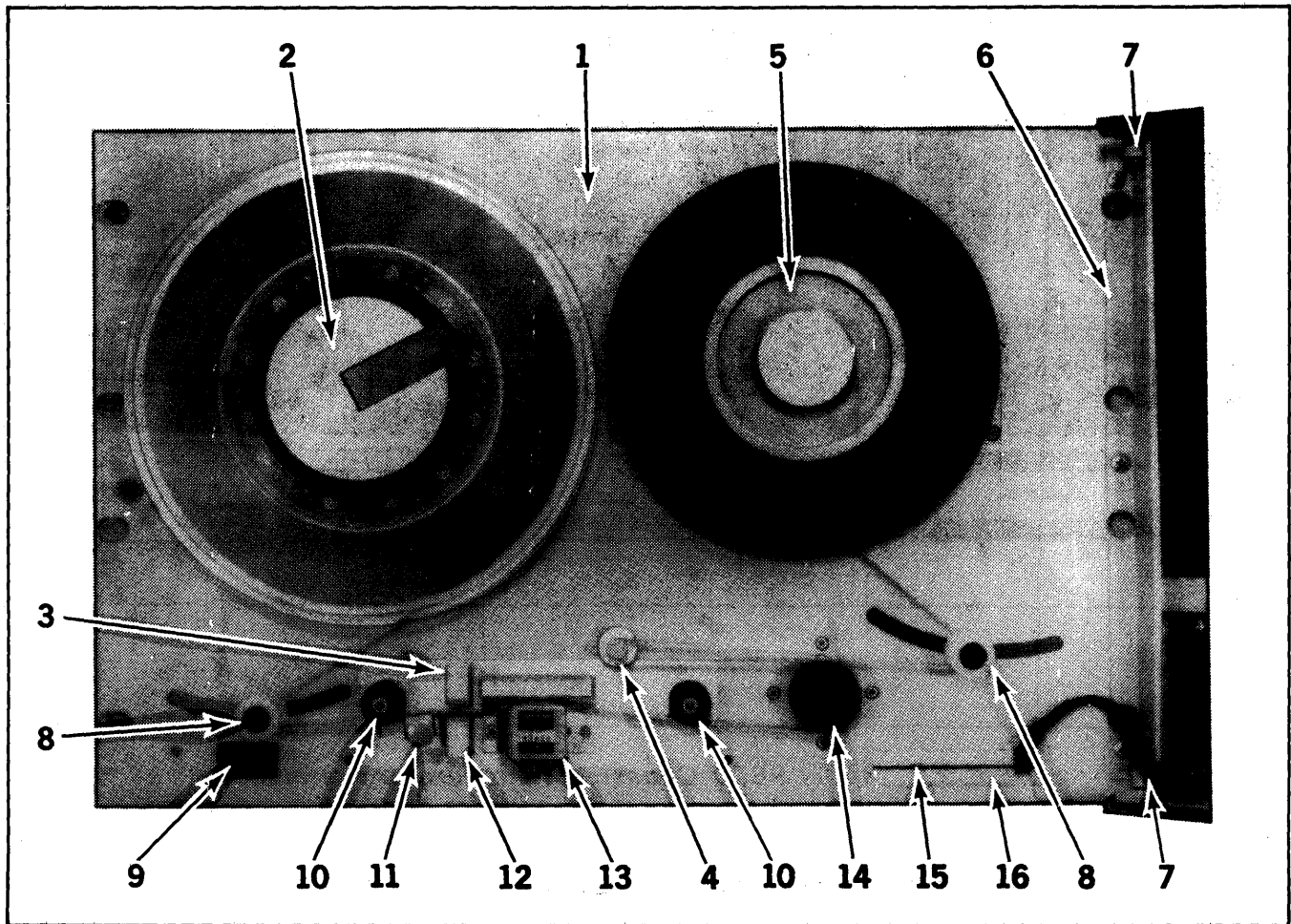
Some replacement components may be supplied in the form of repair or field change kits. The repair kits contain parts that are matched or assembled and adjusted at the factory because of complexity or to aid the field technician. The components ordered as field kits either by correspondence with Kennedy service engineers or by direct order will be supplied with complete installation instructions. The change kits are intended for standard or special options not originally included in the unit.



**Figure 5-1. Model 9800 Chassis: Front View (Dust Cover Closed)**

**ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-1**

<u>Item No.</u>	<u>Part No.</u>	<u>Description</u>
5-1-1	190-3373-004	Dust Cover Assy (includes control panel)
5-1-2	890-3371-004	Control Panel Assy
5-1-3	191-2915-001	Door Latch
5-1-3	128-0003-002	Door Catch
Not shown	198-0014-001	Slide Set

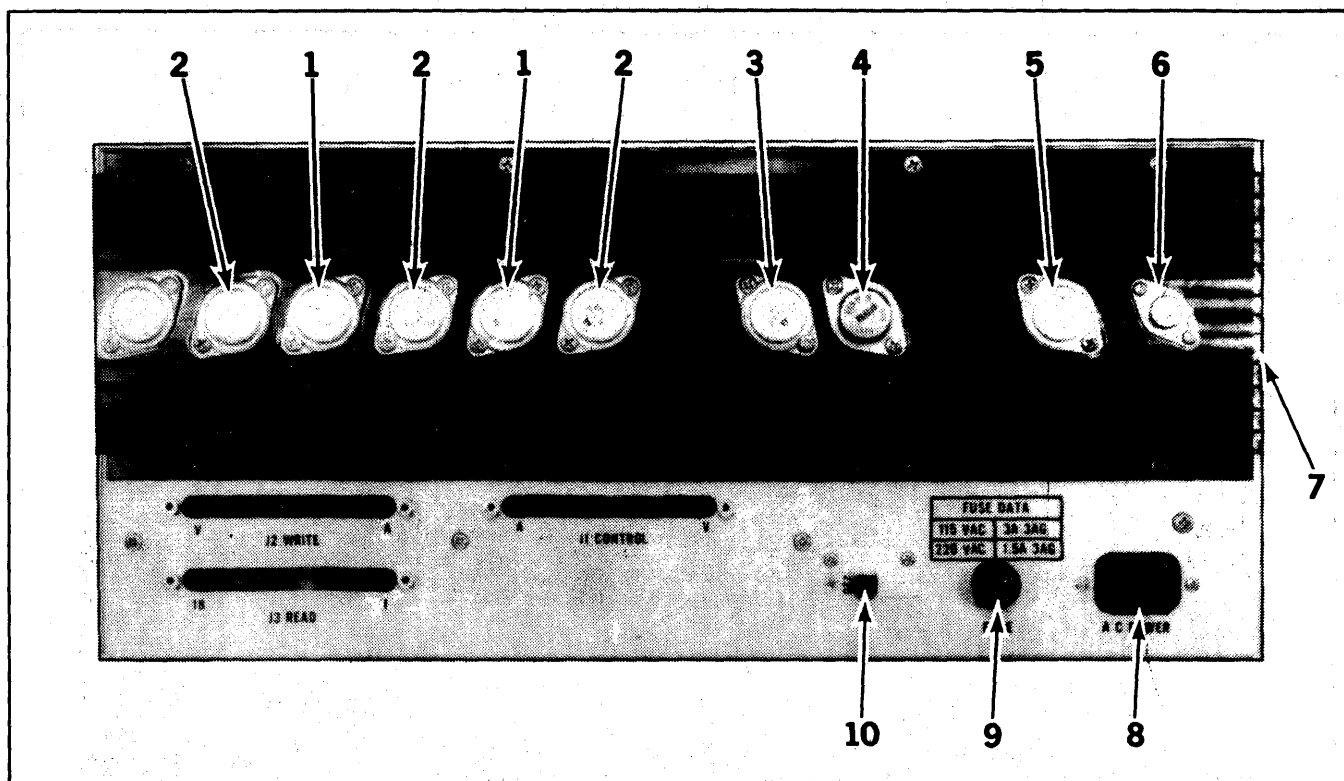


**Figure 5-2. Model 9800 Chassis: Front View (Dust Cover Open)**

**ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-2**

<u>Item no.</u>	<u>Part No.</u>	<u>Description</u>
5-2-1	190-3955-002	Deck Assy
5-2-2	890-2744-001	Quick Release Hub
5-2-2	198-0010-001	Hub Bearing Assy
5-2-2	825-0030-006	O-Ring
5-2-2	828-0090-001	Spring Washer
5-2-3	890-1138-001	Load Point/EOT Photosensor Assy
5-2-4	890-2627-001	Idler Assy
5-2-5	890-2772-002	Takeup Hub Assy
5-2-6	291-2964-005	Dust Cover Mount
5-2-7	191-2966-001	Hinge Pin
5-2-8	890-2647-002	Tension Roller Guide Assy
5-2-9	851-0038-001	Power Switch
5-2-10	890-1509-001	Split Tape Guide Assy
5-2-11	190-2747-001	Tape Cleaner Assy
5-2-12	890-1139-001	Broken Tape Photosensor Assy
5-2-13	198-2399-010	Head and Head Mounting Assy, 9 Track Read and Write
5-2-13	198-2399-003	Head and Head Mounting Assy, 7 Track Read and Write
5-2-14	890-2605-001	Capstan

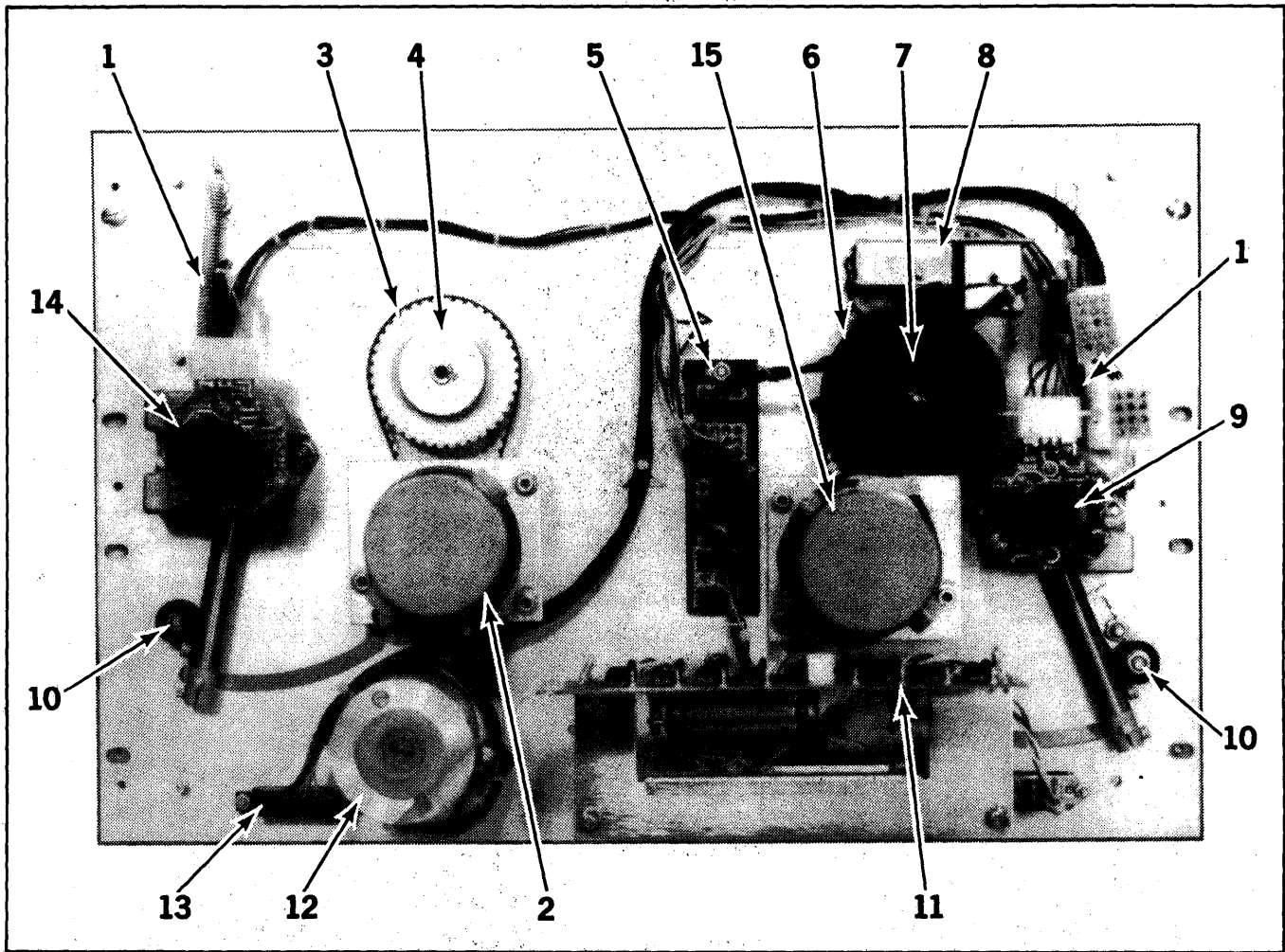




**Figure 5-3. Model 9800 Chassis: Rear View (Assembled)**

**ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-3**

<u>ITEM</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
5-3-1	148-0122-001	Power Transistor, Type MJ802 Motorola
5-3-2	148-0121-001	Power Transistor, Type MJ4502 Motorola
5-3-3	148-0102-003	Power Transistor, Type MJ900 Motorola
5-3-4	148-0102-004	Power Transistor, Type MJ1000 Motorola
5-3-5	148-0053-001	Power Transistor, Type 2N3055
5-3-6	148-0075-001	Power Transistor, Type 2N4910
5-3-7	890-4352-001	Voltage Regulator PC Board
5-3-7	890-4441-001	Regulator and Servo Assembly
5-3-8	127-0003-001	Power Receptacle
5-3-9	151-0802-001	Fuseholder
5-3-9	851-0133-030	Fuse, 3 AG, 3A (115 vac operation) (box of 5)
5-3-9	851-0133-015	Fuse, 3 AG, 1.5A (220 vac operation) (box of 5)
5-3-10	851-5001-103	Switch, 115/220 vac



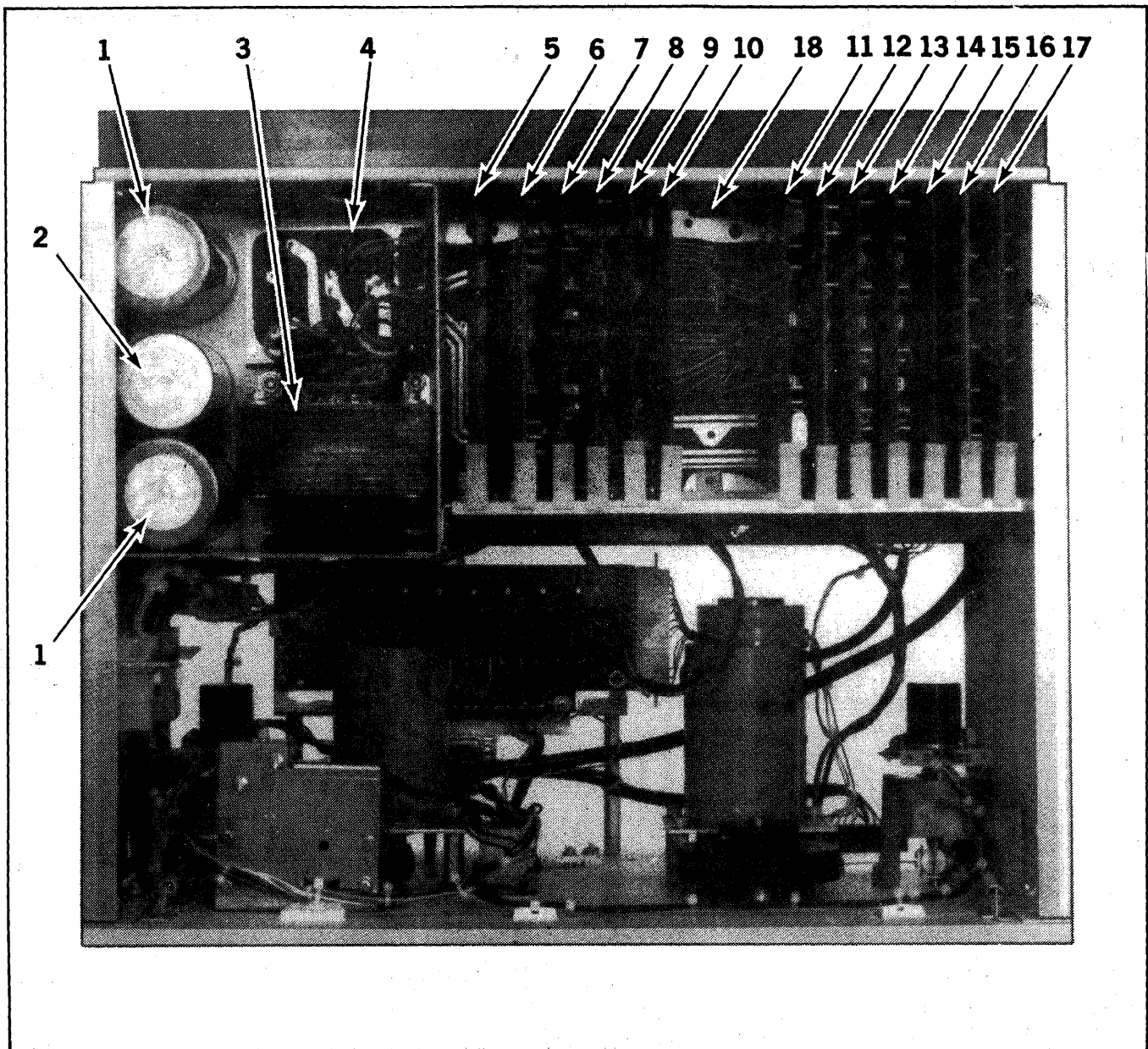
**Figure 5-4. Model 9800 Chassis: Rear View (Power Supply Removed)**

**ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-4**

<u>ITEM</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>	<u>NOTE</u>
5-4-1	825-0017-003	Extension Spring	
5-4-2	890-4438-002	Takeup Reel Motor Assembly, 16 Tooth	2
5-4-3	825-0004-002	Takeup Reel Drive Belt	
5-4-4	191-0805-001	Takeup Reel Drive Pulley	
5-4-5	890-4013-001	Connector PC Board Assembly	
5-4-6	825-0004-003	Supply Reel Drive Belt	
5-4-7	191-2643-001	Supply Reel Drive Pulley	
5-4-8	890-2641-001	File Protect Switch Assembly	
5-4-9	198-0009-011	Supply Reel Magpot Sensor	
5-4-9	890-4210-002	Magpot PC Board Assembly	
5-4-9	891-4198-001	Cover	
5-4-10	828-0067-001	Recessed Bumper	
5-4-11	890-3631-xxx	Read Preamplifier Assembly	1
5-4-12	890-2484-004	Capstan Motor Assembly	
5-4-13	121-0145-004	20 Pin Connector	
5-4-14	198-0009-012	Takeup Reel Magpot Sensor Assembly, complete	
5-4-14	890-4210-002	Magpot PC Board	
5-4-14	891-4198-001	Cover	
5-4-15	890-4438-001	Supply Reel Motor Assembly, 14 Tooth	

NOTE 1: Refer to dash number stamped on circuit board to determine complete part number.

NOTE 2: In 37.5 ips machines, the takeup reel motor is numbered 890-4438-002. The supply reel motor is still numbered 890-4438-001 in 37.5 ips units.



*Figure 5-5. Model 9800 Tape Transport: Top View*

**ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-5**

<u>ITEM</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
5-5-1	815-3625-199	Capacitor, Aluminum, Electrolytic, 19K mfd, 25 vdc
5-5-2	815-3610-449	Capacitor, Electrolytic, 44K mfd, 10 vdc
5-5-3	890-4474-001	Power Transformer Assembly
5-5-10	190-3841-001	Control Terminator PC Board
5-5-15	190-3860-001	Data Terminator PC Board
5-5-5 thru 5-5-17		For part number, see Recommended Spare Parts List (5-5-10 and 5-5-15 listed above)

## RECOMMENDED SPARE PARTS LIST

<u>Item No.</u>	<u>Part No.</u>	<u>Description</u>	<u>Qty.</u>	<u>Notes</u>
5-1-2	890-3371-004	Control Panel Assy	1	
5-2-2	198-0010-001	Hub Bearing Assy	1	
5-2-3	890-1138-001	Load Point/EOT Photosensor Assy	1	
5-2-4	890-2627-001	Idler Assy	1	
5-2-8	890-2647-002	Tension Roller Guide Assy	1	
5-2-10	851-0038-001	Power Switch	1	
5-2-12	890-1139-001	Broken Tape Photosensor Assy	1	
5-2-13	198-2399-010	Head and Head Mounting Assy, 9 Track RAW	1	
5-2-13	198-2399-003	Head and Head Mounting Assy, 7 Track RAW	1	
5-2-14	890-2605-001	Capstan	1	
5-3-7	890-4441-001	Regulator and Servo Assy, complete	1	
5-3-9	851-0133-030	Fuse, 3AG, 3A (115 vac use, box of 5)	1	
5-3-9	851-0133-015	Fuse, 3AG, 1.5A (220 vac use, box of 5)	1	
5-3-10	851-5001-103	Switch, 115/220 vac	1	
5-4-1	825-0017-003	Extension Spring	2	
5-4-2	890-4438-002	Reel Motor Assy	1	2
5-4-3	825-0004-002	Takeup Reel Drive Belt	1	
5-4-5	890-4013-001	Connector PC Board Assy	1	
5-4-6	825-0004-003	Supply Reel Drive Belt	1	
5-4-8	890-2641-001	File Protect Switch Assy	1	
5-4-9	198-0009-011	Supply Reel Magpot Sensor, complete	1	
5-4-9	890-4210-002	Magpot PC Board Assy	1	
5-4-11	890-3631-xxx	Read Preamplifier Assy	1	
5-4-12	890-2484-004	Capstan Motor Assy	1	
5-4-14	198-0009-012	Takeup Reel Magpot Sensor Assy, complete	1	
5-4-14	890-4210-002	Magpot PC Board Assy	1	
5-4-15	890-4438-001	Supply Reel Motor Assy, 14 tooth	1	
5-5-1	815-3625-199	Capacitor, Electrolytic, 19K mfd, 25 vdc	1	
5-5-2	815-3610-449	Capacitor, Electrolytic, 44K mfd, 10 vdc	1	
5-5-3	890-4474-001	Power Transformer Assy	1	1
5-5-5	890-4306-xxx	Servo Preamplifier PC Board	1	1
5-5-6	890-3844-xxx	Sensor Amplifier/Driver PC Board	1	1
5-5-7	890-3645-xxx	Ramp Generator PC Board	1	1
5-5-8	890-3843-xxx	Pushbutton Control PC Board	1	1
5-5-9	890-3842-xxx	Interface Control PC Board	1	1

## NOTES

- 1: PC board dash number will vary depending upon machine specifications. Refer to the circuit board identification card in the machine or check the PC board for a stamped dash number.
- 2: In 37.5 ips machines, the supply and takeup reel motors are both numbered 890-4438-001.

**RECOMMENDED SPARE PARTS LIST**

(Continued)

<u>Item No.</u>	<u>Part No.</u>	<u>Description</u>	<u>Qty</u>	<u>Notes</u>
5-5-11	890-3845-xxx	Delay Timing PC Board	1	1
5-5-11	890-4118-xxx	7 Track Delay Timing PC Board	1	1
5-5-11	890-4365-xxx	Dual Density Control PC Board (dual density models)	1	1
5-5-11	890-4209-xxx	Read Control Logic	1	1
5-5-12	890-4179-xxx	Read Amplifier/Clipping Level Control	1	1
5-5-12	890-4188-xxx	Read Amplifier/Clipping Level Control (1600 cpi models)	1	1
5-5-12	890-4367-xxx	Replaced by:		
	890-6367-xxx	Dual P Channel Clipping Control (dual density models)	1	1
5-5-13	890-4178-xxx	Quad Read Amplifier PC Board	1	1
5-5-13	890-4139-xxx	Quad PE Read Detector (PE models)	1	1
5-5-13	890-4385-xxx	Replaced by:		
	890-6385-xxx	Quad Read Amplifier (dual density models)	1	1
5-5-14	890-4178-xxx	Quad Read Amplifier PC Board	1	1
5-5-14	890-4139-xxx	Quad PE Read Detector (PE models)	1	1
5-5-14	890-4385-xxx	Quad Read Amplifier PC Board (dual density models)	1	1
5-5-16	890-3848-xxx	Four Channel Write Amplifier PC Board	1	1
5-5-16	890-4207-xxx	Four Channel PE Write Amplifier (PE models)	1	1
5-5-16	890-4366-xxx	Four Channel Write Amplifier (dual density models)	1	1
5-5-17	890-3849-xxx	Five Channel Write Amplifier	1	1
5-5-17	890-4208-xxx	Five Channel PE Write Amplifier (PE models)	1	1
5-5-17	890-4368-xxx	Five Channel Write Amplifier (dual density models)	1	1
5-5-18	890-4206-xxx	Masterboard	1	
5-5-18	890-4509-001	Masterboard (dual density models)	1	
Not shown	825-0068-001	Power Cord	1	
Not shown	821-9000-003	Power Cord (230 vac or dc power)	1	
Not shown	198-0103-001	Brush Replacement Kit, Capstan Motor Tachometer	1	
Not shown	198-0075-001	Brush Replacement Kit, Reel Motor (4 brushes)	1	
Not shown	198-0100-001	Hub Repair Kit	1	2
Not shown	198-0014-002	24" Rack Slide Set		
Not shown	198-0014-001	18" Rack Slide Set		

**NOTES**

1. PC board dash number will vary depending upon machine specifications. Refer to the circuit board identification card in the machine or check the PC board for a stamped dash number.
2. Hub repair kit contains items subject to wear; i.e., O ring, reel drive latch, and thrust washer.

**SECTION VI**  
**WIRING AND SCHEMATIC DIAGRAMS**

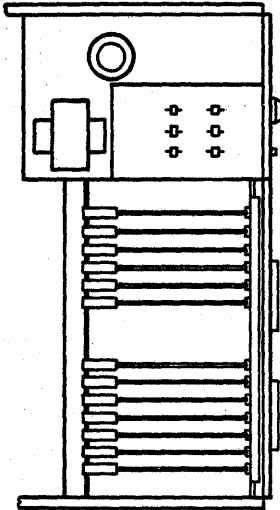
## SECTION VI

### WIRING AND SCHEMATIC DIAGRAMS

This section contains the wiring diagrams, schematic diagrams, and circuit descriptions for the individual circuit cards used in the transport. The schematics are arranged by functional group as shown below.

Electronics symbols used in the drawings conform to MIL-STD-15. Abbreviations conform to MIL-STD-12 unless otherwise specified. Logic diagrams conform to MIL-STD-806C.

Overall	Power Supply
Control Electronics	<ul style="list-style-type: none"> <li>Control Terminator</li> <li>Interface Control</li> <li>Tape Motion Controls, including Pushbutton Control, Main Control Panel, and Test Panel</li> <li>Ramp Generator</li> <li>Sensor Amplifier/Driver</li> <li>Connector Board</li> </ul>
Servo System	<ul style="list-style-type: none"> <li>Servo Preamplifier</li> <li>Magpot Tension Arm Position Sensor</li> </ul>
Read Electronics	<ul style="list-style-type: none"> <li>Data Terminator</li> <li>Read Preamplifier</li> <li>Read Control Logic, including Nine Track Delay Timing Seven Track Delay Timing</li> <li>Quad Read Amplifier</li> <li>Read Amplifier/Clipping Control</li> </ul>
Write Electronics	<ul style="list-style-type: none"> <li>Write Amplifier, Section A</li> <li>Write Amplifier, Section B</li> </ul>



2 4 6 8 10 12  
1 3 5 7 9 11 13

CIRCUIT CARD IDENTIFICATION		
LOC	TYPE	FUNCTION
READ/WRITE SECTION		
1	3849-001	5 CHANNEL HEAD DRIVER
2	3848-001	4 CHANNEL HEAD DRIVER
3	3860-001	DATA TERMINATOR
4	4178-001	QUAD READ AMPLIFIER
5	4178-001	QUAD READ AMPLIFIER
6	4179-001	P CHANNEL/CLIPPING
7	3845-001	DELAY TIMING
CONTROL SECTION		
8	3841-001	CONTROL TERMINATOR
9	3842-001	INTERFACE CONTROL
10	3843-001	PUSHBUTTON CONTROL
11	3645-001	RAMP GENERATOR
12	3844-001	SENSOR AMPLIFIER/DRIVER
13	4306-001	SERVO PREAMPLIFIER

MODEL	PART NO.	INTERFACE
9832	192-9832-094	STD
SPEED	DENSITY	TRACKS
25 IPS	800 CPI	9
MODIFICATIONS		
512 BUFFER		



## NOTES TO SCHEMATIC SECTION

Certain conventions have been observed in preparing schematics for this manual:

1. Resistor values are given in ohms. If wattage is unspecified the resistor may be either 1/4 or 1/2 watt.
2. Capacitor values may be given in picofarads or microfarads. Those values for which neither designation is provided are assumed to be obvious from circuit function. Filter capacitors on certain supply lines do not have logic significance. In general, they are not shown on schematics. On PC board silkscreens they are designated as CF.
3. Normally, IC power connections are on pins 14 (+5v) and 7 (ground) for 14 pin packages, and 16 (+5v) and 8 (ground) for 16 pin packages. Some ICs — 7476, 7492, 7493 for example — have power connections on pin 5 (+5v) and pin 10 (ground). Operational amplifiers in the 8 pin package have power connections on pin 4 (-Vcc) and pin 7 (+Vcc). Power connections are not shown unless they are nonstandard.
4. Where multiple inputs are tied together only one pin may be designated on the schematic.
5. Unused inputs that are tied high are not normally indicated unless the connection has logic significance.
6. From and to designations are intended to describe inputs and outputs only. The same signal may be connected to several other points not shown on a particular drawing.
7. Abbreviations used in from and to designations are as follows:

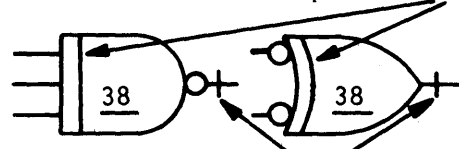
CI	Control Interface
PBC	Pushbutton Control
RG	Ramp Generator
SA	Sensor Amplifier/Driver
DT	Delay Timing
RA/CL	Read Amplifier/Clipping Level
RA	Quad Read Amplifier
WA1	Four Channel Write Amplifier
WA2	Five Channel Write Amplifier

8. Positive logic is shown for all internal connections. Interface connections are zero true but the bar is omitted.
9. Integrated circuit symbols contain a circuit designator that corresponds to the number silk-screened onto the circuit module above an underlined number representing the IC type.

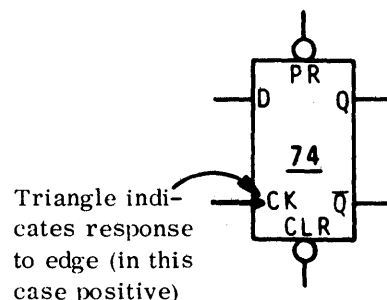
The IC type number is abbreviated and omits the portions of the manufacturer's type number pertaining to case and vendor identification. Further, since the TTL 7400 series makes up most of the circuitry, the 74 is omitted on these. Thus a 00 designation indicates a 7400 quad two input NAND gate. T.I.'s complete part number is SN7400N. In multifunctional units in close proximity to each other the type designation may be omitted. The type designation may appear outside the symbol if the symbol is too small.

Military Standard 806C is the base for logic symbols. Additional conventions are shown below.

Line indicates buffer or power driver



Line indicates open collector

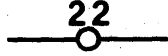


10. Semiconductor types on schematics may be replaced by their functional equivalents. If not indicated, diodes are 1N914, NPN transistors are 2N2714, and PNP transistors are MPS6517.
11. Unless otherwise specified, light emitting diodes are FLV102 or equivalent.

12. Module connector pins are shown as



where no further connection is shown on the schematic, and as



when there is a connection shown.

13. Where an input is represented by an arrow instead of a complete line, the input source is designated. Where outputs are so shown their destinations may not be shown.
14. Some schematics of modules include certain external elements which aid in understanding the

circuit function. In this case all the connections to the element may not be shown in the interest of clarity.

- 15.



designates a test point provided on the module. Letters proceed from top to bottom of card with the ground test point, if present, as the bottommost terminal.

16. Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double sided socket is used. These are the designations on the socket. When a single sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on the etch. Letters follow the 22 pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.

## MODEL 9800 POWER SUPPLY

### CIRCUIT DESCRIPTION

Power supply in Model 9800 produces the unregulated and regulated voltages required by motors and electronics.

#### PRIMARY POWER

Primary power is switchable to allow either 115v or 220v mains. Frequency is not critical and may be from 48 Hz to 500 Hz. 220 volt mains predominate in Europe, hence this selection of voltages. A simple modification allows 230v operation if required. For 115v operation the two 115v primary windings of  $T_1$  are connected in parallel by S2. For 220v operation a 105v tap on primary winding 2 is connected in series with primary 1. Modification for 230v operation requires removal of the violet wire and installation of a jumper from S2-6 to S2-3.

#### SECONDARY POWER

Transformer secondary voltages are rectified to produce nominal unregulated voltages of  $\pm 24v$  ( $\pm 26v$  under light load) and  $+8v$ .  $\pm 24v$  regulated is supplied to motor drive circuits and provides sources from which  $\pm 10v$  regulated is produced.  $+8v$  is the source for a high efficiency  $+5v$  regulator.

#### +10 VOLT REGULATOR

Pass transistor Q3 is fed from  $+24v$  and its base is driven by a monolithic regulator IC2. Voltage output is determined by R8 and R9. Q7 and Q8 control power supply tracking when powering down. As  $+24v$  drops owing to discharge of C1, Q8 cuts off at approximately 13 volts on the  $+24v$  line. When this happens Q7 is

turned on shorting out R9 and dropping the regulator reference voltage to zero. The  $+10v$  output is cut off and drops to zero. Since  $+10v$  is the reference for  $-10v$ ,  $-10v$  also drops to zero. This action occurs before the  $+5v$  supply has dropped sufficiently to cause indeterminate logic states; turn-off transient motions are prevented.

#### -10 VOLT REGULATOR

The  $-10v$  supply is regulated by pass transistor Q4 driven by Q6. Its reference is  $+10v$  as determined by R13, R14. In this way the two regulated voltages are made to track or retain a constant relationship to each other.

#### +5 VOLT REGULATOR

An integrated circuit regulator IC1 controls  $+5v$  output in conjunction with pass transistor Q1 and driver Q2. Output voltage is set by R4, R5. An inset on the schematic shows the internal circuitry of IC1, IC2. It will be noted that it consists of a differential amplifier with built-in zener reference together with facilities for short circuit protection. Q2 assures that sufficient base drive is available for Q1.

#### SHORT CIRCUIT PROTECTION

Drop through series resistors, for example R10 in the  $-10v$  supply, provides short circuit protection. If the drop across R10 exceeds approximately 0.6v, Q5 is turned on connecting Q4 base to emitter and cutting off Q4. This corresponds to approximately 1.5 amperes under short circuit conditions. Similar circuits are provided in IC1 and IC2.

## TYPE 3842 INTERFACE CONTROL

### CIRCUIT DESCRIPTION

This module contains a set of receivers for the interface control commands:

SYNCHRONOUS FORWARD SFC  
 SYNCHRONOUS REVERSE SRC  
 OVERWRITE OVW  
 REWIND RWC  
 SELECT SLT  
 SET WRITE STATUS SWS  
 OFF LINE OFFC

It also contains drivers that return the recorder status outputs to the interface:

ON LINE ONL  
 REWINDING RWDG  
 FILE PROTECT FPT  
 LOAD POINT LP  
 WRITE ENABLE WEN  
 READY RDY  
 END OF TAPE EOT  
 TAPE RUNNING TNG

Certain controls and delays are also provided to ensure proper tape motion and transport operation.

#### TAPE MOTION CONTROLS

The motion control commands from the interface, SFC and SRC, are translated on this card into the internal motion commands of the transport — RUN NORMAL  $\overline{RNN}$ , FORWARD  $\overline{FWD}$ , and REVERSE  $\overline{RVS}$ . These internal motion commands are supplied to the Pushbutton Control module, where they are combined with commands supplied from the transport pushbuttons and internal interlocks to generate the commands that initiate actual tape motion on the Ramp Generator module.

On this module SFC and SRC are supplied to an interlocking network that ensures that the tape comes to a stop before its direction of motion is reversed. The interlocking network includes flip-flop IC1-3, edge circuits IC2-6 and IC2-8, NAND gate IC3-6, and interlocking flip-flop IC3-10. Whenever flip-flop IC1 changes states due to a change in the direction of motion, for example from a reverse command SRC to a forward command SFC, its output generates a pulse through the edge circuits consisting of inverters IC2 and the associated capacitors. The pulse is gated through IC3-6 to the set input of interlocking

flip-flop IC3-10. The flip-flop can be set only if TAPE RUNNING  $\overline{TNG}$  is true, indicating that the tape is still moving. In this case  $\overline{TNG}$  low at input pin W is inverted by IC18-12 and supplies a high input to the clear of IC3. The flip-flop can then be set by the pulse on its set input, its 0 output going low. The 0 output of IC3 then inhibits the RUN NORMAL gate IC15 at pin 2, setting RUN NORMAL  $\overline{RNN}$  false. After the tape has ramped down to a stop, TAPE RUNNING  $\overline{TNG}$  goes false, clearing interlocking flip-flop IC3, whose output then enables the RUN NORMAL gate. RUN NORMAL  $\overline{RNN}$  then goes true if the following conditions are satisfied: SELECT SLT1 is true, indicating that the transport is on line and selected by the interface; BUSY  $\overline{BSY}$  is false, indicating the transport is not rewinding or searching for load point; and SRC command is not given at load point. (This would activate NAND gate IC15-8 and would disable the RUN NORMAL gate at IC15-1.) If the above conditions are satisfied, RUN NORMAL  $\overline{RNN}$  goes true at output pin V, and is supplied to the Pushbutton Control module where it initiates tape motion at the normal running speed. The direction of motion is determined by the state of flip-flop IC1. If a forward command SFC has been given, the flip-flop is set and its 1-output enables NAND gate IC14-8, provided that SLT1 is true and  $\overline{BSY}$  is false. This generates FORWARD  $\overline{FWD}$  true at output pin U. If a reverse command SRC has been given, flip-flop IC1 is cleared and enables NAND gate IC14-6, generating REVERSE  $\overline{RVS}$  true, providing SLT1 is true,  $\overline{BSY}$  is false, and LOAD POINT LP is false. No interface reverse command is acknowledged by the transport when the load point is detected.

#### WRITE SELECT

During a write operation the interface supplies SET WRITE STATUS SWS true at pin K; SWS is inverted by IC9-4 and is supplied to the D input of flip-flop IC7. The flip-flop is toggled provided that the transport is selected and on line, after NOR gate IC1-11 is activated by a synchronous motion command. This would activate NAND gate IC1-8 and trigger one-shot IC4-1, generating a 2  $\mu$ sec pulse. On the trailing edge of the pulse the  $\overline{Q}$  output of the one-shot toggles IC7-3, the Q output of the flip-flop going high and activating NAND gate IC10-11, generating WRITE SELECT WSEL true at output pin H. During an overwrite operation OVERWRITE OVW true is inverted by IC18-8 and sets the D input of flip-flop IC7-12

high. On the trailing edge of the pulse generated by one-shot IC4-4 the flip-flop is set and enables NAND gate IC8-12. One-shot IC4-4 also direct-sets flip-flop IC11, whose Q output enables the overwrite gate at IC8-9. If write status is true, the gate is enabled at IC8-13 and it is kept activated as long as a synchronous motion command is activating NAND gate IC1-8. IC8-8 then goes low and supplies  $\overline{WSEL}$  for the duration of the motion command only. When a WRITE AMPLIFIER RESET pulse is given at pin P, it toggles flip-flop IC11 to the cleared state and disables the overwrite gate.

#### REWIND FLIP-FLOP

When a REWIND COMMAND RWC is given by the interface, it sets the rewind flip-flop IC5-3, provided that the transport is selected, on line, and not at load point. The 1-output of the flip-flop then goes high, generating REWINDING RWDG true to the interface, and a rewind command  $\overline{RWCI}$  through an edge circuit consisting of inverter IC6-6, NAND gate IC6-8, and capacitor C5.  $\overline{RWCI}$  is supplied to the Pushbutton Control module. The flip-flop is cleared when the tape returns to and stops at load point, or when BROKEN TAPE BKN is detected.

#### END OF TAPE

An end of tape indication is set when the EOT marker is encountered in forward direction and remains set

until the marker is passed in the reverse direction.

A true EOT signal at pin Z if machine status is  $\overline{RWDG}$  (IC10-5, 8) and  $\overline{RVS}$  (IC14-6) causes IC11 to be preset by IC19-8. An EOT status is then signaled at the interface by IC16-3.

Upon passing the EOT marker in the reverse direction IC13-3 is high and the EOT signal clocks IC11 clear on the trailing edge of the EOT signal dropping the EOT signal at the interface. IC11 is preset to the clear state by BKN signal at pin X.

#### OUTPUT STATUS

Most status gates on this module are preconditioned by SELECT and ON LINE being true; consequently, the transport returns status indications only when it is selected and on line. The READY status is generated when BUSY  $\overline{BSY}$  supplied from the Pushbutton Control module is false and the transport is not rewinding. The LOAD POINT output is also preconditioned by the rewinding status being false. The only status gate not preconditioned is the rewind via the REWIND pushbutton. If the pushbutton is used to rewind, that status is made available to the interface without being selected and on line.

## TYPE 4842 INTERFACE PC BOARD

### CIRCUIT DESCRIPTION

This board contains receivers and gating circuits for developing tape transport commands from incoming controller commands. It also contains line drivers for outputting tape transport status commands to the controller. In addition, type D flip-flop IC10 outputs EBDIS/, the Erase Bar Disable signal required during tape editing.

#### Tape Motion Control Circuitry

SFC, SRC, FAST tape motion commands from the controller are translated into internal tape transport motion commands RNN/, RNF/ and RVS/ by quad 2x1 multiplexer IC15. These internal commands are supplied to the Pushbutton Control module where they are combined with commands from the transport pushbuttons and the internal interlocks to develop the actual tape motion commands issued to the transport's Ramp Generator PC board.

SRC, SFC and FAST are supplied to an interlocking network on this PC board to insure that tape motion ceases prior to accepting a new direction command. The interlock network consists of a high frequency sampling oscillator (IC11 and related components), and a directional interlock flip-flop (IC14 and related components) to select and generate the appropriate RUN NORMAL, RUN FAST and REVERSE signals required by the transport. The oscillator monitors the state of TNG/ (Turning) signal. This signal disables oscillator output when the capstan is turning and enables oscillator output when tape and capstan motion ceases.

Table 1 indicates the controller inputs and interface board outputs required to initiate a given tape motion.

To generate RNN true for forward tape motion, SFC (Synchronous Forward Command) from the controller must be true. This is supplied to the D input of interlock flip-flop IC14 and pin 3 of multiplexer IC15. After capstan motion ceases, TNG/ goes false, enabling the high frequency oscillator at IC11, pin 3 to clock out Q high at IC14-5. This is applied to multiplexer IC15-1 to select its B inputs. Since SFC

high is applied to the 1B input of the multiplexer, the output at IC15-4 goes high. This is inverted low at inverter IC16-11 to produce RNN/ (Run Normal) true at pin V.

Should the Synchronous Reverse Command (SRC) be issued to the transport, it will not be able to produce a RVS/ transport command until capstan rotation ceases. SRC true is gated with LP/ false to enable IC6-6. IC6-6 high is applied to inputs 1A and 2A of the multiplexer. After tape motion stops, TNG/ false enables the sampling oscillator, clocking the Q output of IC15-5 low, since SFC would now be low false after inversion at IC14. IC15-1 of the multiplexer goes low, selecting the A multiplexer inputs. IC15-4 again goes high to issue RNN/ true at pin V IC15-7 also goes high and is inverted low at IC16-3 to produce RVS/ true.

Fast forward tape motion does not require a stopped tape, if a direction change is not required since the requisite RNN true is routed back to pin 11 of the multiplexer IC and output whenever the A inputs are selected by IC14-5 low. IC15-9 goes high at this point, making NAND gate IC16-10 high. FAST true from the interface will enable IC16, which outputs RNF/ true at pin U. RNN/ at pin V will also be true as required by the ramp generator for fast forward tape motion. When the End of Tape mark is reached, EOT/, connected to pin 10 of the multiplexer, will go low true, causing IC15-9 to go low to disable a run fast operation (now being interpreted as normal run).

Fast reverse tape operation is initiated by generating RNN/ true, RNF/ true and RVS/ true. Thus, the controller must issue SRC true and FAST true. After capstan rotation ceases and TNG/ goes false, Q low is clocked out of IC14-5, selecting the B multiplexer inputs. Then RNN/, RNF/ and RVS/ at pins V, U and T all go low true.

Tape motion will be disabled whenever BSY true or SLT/ false signals are issued. This would disable NAND gate IC3-6, resulting in a high false STROBE signal at IC15-15, which disables all multiplexer outputs.

<u>Tape Mode</u>		<u>Controller Command</u>	<u>Interface PCB Output</u>
Forward	=	SFC true	RNN/true
Reverse	=	SRC true	RNN/true + RVS/true
Fast Forward	=	SFC true + FAST true	RNN/true + RNF/true
Fast Reverse	=	SRC true + FAST true	RNN/true + RNF/true + RVS/true

Table 1

### Write Select

Control of the write amplifier is performed by SWS (Set Write Status), OVW (Overwrite) and internally generated WARS1 (Write After Read Strobe) signals which generate WSEL/ (Write Select) and EBDIS/ (Erase Bar Disable). WSEL/ and EBDIS/ are output to the sensor amplifier and pushbutton control cards.

A sampling scheme is employed to permit the interface to issue tape motion and WSEL commands simultaneously. RNN/ true and RNN true are delayed 16 and 8 usec respectively by RC networks R8/C1 and R9/C2 prior to being applied to Schmitt trigger NAND gate IC13. As a result, IC13-8 outputs an approximate 8 usec low clockpulse to the sampling flip-flops and the preset of IC8. Thus the write commands are sampled 15 to 20 usec after the leading edges of the tape motion commands, allowing the controller to output tape motion and write amplifier commands simultaneously.

Set Write Status (SWS) true is loaded into the D input at IC10-12 from 15 to 20 usec after RNN goes true. SWS high true and EBDIS high false are applied to AND/OR inverter IC9 at pins 9,10 and 11, producing WSEL/ true at IC9-8. OVW will be false during a normal write operation.

Note that WSEL/ is not reset on termination of a motion command; instead it is only sampled at the beginning of a motion command. This avoids potential glitches from being written while writing consecutive blocks, since the write amplifier is not being constantly turned on and off during this operation.

### Overwrite

Overwriting or editing is performed by backspacing over the block to be rewritten to determine its exact length then presenting OVW true and SWS true concurrent with the beginning of a run command. This sets the Q outputs at IC10-9 low false and IC10-5 true. Reset flip-flop IC8-9 is also set high true. AND/OR inverter 9 is enabled, outputting WSEL/ true for the duration of the overwrite operation. Note that Erase Bar Disable (EBDIS/) true is output to the sensor amplifier from pin 18 during an overwrite operation which disables (turns off) the upstream erase bar.

After a block is written in NRZI format, WARS goes true at the write amplifier to produce an LRC character; then WARS1 true is issued to the interface, toggling IC8-9 false to disable Write Select and turn off the write current before writing can continue into the next data block.

### Rewind and Unload

The rewind status flip-flop is a SR flip-flop IC7 and related circuitry. A Rewind Command (RWC) is accepted whenever the tape is not at load point (LP false). IC7-8,2 go high, causing RWDG true status signal to be output to the interface through driver IC5-6. Simultaneously a 5 usec RWC1/ true pulse is

output from Schmitt trigger NAND gate IC11-11. RWC1 is output to the Pushbutton Control PC board to set the REWIND flip-flop. The pushbutton control card then issues a RWDG1 true level which is applied to IC7-10 to keep the rewind status flip-flop set.

When the tape rewinds to loadpoint (LP true) and capstan motion ceases (TNG/ true), or a broken tape is detected (BKN true), the rewind status flip-flop is cleared. IC7-11,12 goes high, which is applied to AND gate IC6-12. If the unit is selected, online, and not busy, IC6 and IC13 will be enabled to return a RDY true status signal to inform the interface that the transport is ready for the next data and/or tape motion command.

During an unload operation, the tape is slowly rewound off the takeup reel. To accomplish this, UNLD/ true is issued from the controller. UNLD/ true is inverted high at IC4-12; then gated with SLT SLT and ONL, or just UNLD/ itself. (This is determined by the strapping of ST1/ST2: See table on schematic.) The high output at IC6-8 is inverted low by IC4, then used to set unload flip-flop IC8 at pin 4. IC8-5 high is gated at IC11 with IC7-11,12 high, which indicates the transport is not rewinding. IC11-6 outputs UNLOAD/ true for vacuum column 9100/9300 transports. Strap ST5 is connected on interface PC boards used in 9100/9300 transports to output UNLOAD/ true to the Sequence Control PC board through pin 7.

With strap ST3 installed, RVS and RNN/ true signals are output to the Pushbutton Control PC board on 9000/9700 transport through pins V and T. A BKN true status signal will clear both the rewind status and unload flip-flops, when the tape completely unloads.

Diodes CR3/CR4 at pins 10 and 12 cause UNLD/ true from the interface to initiate a rewind operation if the tape was not already at load point. The tape drive will also be taken offline (OFFC true). RC network R21/C7 delays SLT and ONL true signals 4 to 6 usec to insure correct timing during this combination unload-rewind-offline operation.

### EOT Flip-Flop

IC14 is the EOT flip-flop which outputs EOT1 high true status signal to the Pushbutton Control PC board whenever the EOT tab has been detected. EOT true also is gated with SLT and ONL true at IC1, then returned to the interface via pin U as EOT. EOT low false trailing edge from the Sensor Amplifier clears IC14 by clocking the flip-flop if and only if a reverse motion command is initiated. (EOT is delayed by R10/C3 for TTL timing considerations.) EOT1 at IC14-8 now goes false. Load Point true or Broken Tape true, which are applied to preset pin 10, will also clear the EOT flip-flop.

### Status Gates

All status gates on this PC board are preconditioned by SLT and ONL being true. The gating of these signals is self-explanatory.

## MODEL 9000 SERIES TAPE MOTION CONTROLS

### CIRCUIT DESCRIPTION

The circuitry used to carry out the motion commands issued by the interface or by the pushbutton panels, both the main control panel and the test panel, is located on Pushbutton Control Type 3843 module. This module generates the motion command lines RUN NORMAL RNN1, RUN FAST RNF1, and REVERSE RVS1, which are supplied to the ramp generator module to initiate actual tape motion.

#### FRONT PANEL PUSHBUTTON CONTROLS

The LOAD, ON LINE, and REWIND pushbuttons, situated on the main control panel, are connected to respective flip-flops on the Pushbutton Control Card Type 3843. When the LOAD pushbutton is activated, it grounds the input to inverter IC12-1, setting the LOAD flip-flop consisting of NOR gate IC13-6 and inverter IC12-1. Once the LOAD flip-flop is set IC13-6 goes low, is inverted by IC12-4 and removes the direct-clear from the ON LINE flip-flop IC10-3. Thus the ON LINE flip-flop can be set only after the transport has been loaded. When the ON LINE pushbutton is activated the first time, it toggles IC10-1 to the set, or ON LINE, position, the outputs of the flip-flops generating ONL and  $\overline{\text{ONL}}$  true. Inverters IC12-8 and IC12-10 are connected as a protective flip-flop on the clock input to IC10-1. Once the ON LINE flip-flop has been set, ONL true is inverted twice by IC9 setting the common of the REWIND pushbutton on the control panel high, disabling that pushbutton. The ON LINE flip-flop can be cleared by pressing the front panel pushbutton a second time, or by an interface OFF LINE COMMAND OFFC1, supplied from the interface control module.

The REWIND pushbutton can be activated only when the transport is off line. When activated the REWIND pushbutton sets the flip-flop consisting of gates IC8-8 and IC8-6, provided that the transport is loaded at the time (LOAD true at IC8-13) and test mode is not selected (IC7-8 high). Consequently the transport cannot be rewound by the pushbutton during test mode, or when on line, or when LOAD is false. When the transport is on line the rewind flip-flop can be alternately set by interface REWIND COMMAND  $\overline{\text{RWC1}}$ , supplied from the interface control module. The output of the rewind flip-flop, REWINDING  $\overline{\text{RWDG1}}$ , activates NOR gates IC15-8 and IC14-6, generating RNF1 and RVS1 true to the ramp generator module, initiating a fast reverse motion to load point. When load point is detected the photosensor

amp driver module supplies the load point pulse at input pin H of the pushbutton control module, clearing the rewind flip-flop.

An additional flip-flop, IC1-6, is used to locate the tape position. Before the tape is loaded, the flip-flop is cleared by LOAD false at IC10-8. When the transport is loaded the direct-clear is removed and NAND gate IC14-11 is enabled. Since the on tape flip-flop is still cleared, its  $\overline{\text{Q}}$  output high activates NAND gate IC14-8, generating a RUN NORMAL RNN1 at output pin Y, advancing the tape to load point. When the load point marker is detected, LP true at input pin 21 from the photosensor module is gated through IC16-3 and direct-sets flip-flop IC10-7 to the ON TAPE state, terminating the tape motion. Similarly, when load point is detected during reverse tape motion, the ON TAPE flip-flop is toggled by NAND gate IC16-11 to the clear state, initiating forward tape motion back to load point.

#### BUSY

This module generates a BUSY output when the tape is not loaded, when it is advancing to load point, or when the transport is off line and not in test mode. In any of these cases NOR gate IC4-8 is activated and supplies  $\overline{\text{BSY}}$  true to the interface control module.

#### WRITE READY

WRITE READY true is generated in two different cases: when the interface supplies WRITE SELECT true and the transport is not in test mode ( $\overline{\text{TM}}$  false), or when the transport is in the write test mode and flip-flop IC6-14 is set. In either case NOR gate IC1-8 is activated, enabling NAND gate IC4-5. The gate is activated provided that BUSY  $\overline{\text{BSY}}$  is false, FILE PROTECT  $\overline{\text{FPT}}$  is false, and the transport is not in reverse motion (RVS1 is false). IC4-3 then goes low, is inverted by IC5-12 and generates WRDY true at output pin J to Write Amplifier Type 3848.

#### TEST PANEL CONTROL

In order to activate the test panel the transport must be off line, and the test panel STOP pushbutton must be depressed. In that case the TEST MODE pushbutton on the test panel can be activated, setting the flip-flop consisting of inverters IC11-8 and IC11-10, which in turn toggles the test mode flip-flop IC6-6



to the test mode state, generating  $TM$  and  $\overline{TM}$  true. The test mode flip-flop is direct-cleared when the transport is placed on line, or when the TEST MODE pushbutton is activated a second time. After the test mode flip-flop has been set the other test panel pushbuttons are enabled. The WRITE TEST pushbutton may then be activated, setting the protective flip-flop consisting of inverters IC11-4 and IC11-6, which in turn toggles the write test flip-flop IC6-1 to the write test mode, provided that forward motion is selected. The  $\overline{Q}$  output of the write test flip-flop then activates NOR gate IC1-8, in turn activating the write ready gate IC5-3, provided that FILE PROTECT FPT, REVERSE RVS1, and BUSY  $\overline{BSY}$  are all false. In that case WRITE READY WRDY true is generated at output pin J to the write amplifier module, where it enables the write data strobe circuitry. During the write test the write amplifiers generate consecutive all-1 characters which may be used to adjust the skew.

Additional test panel pushbuttons are FORWARD RUN, a normal forward run button, FAST FORWARD, a high speed forward button, REVERSE and

FAST REVERSE buttons. The reverse motion buttons can be activated only if the on tape flip-flop IC10 is set and the tape is not at load point, activating NAND gate IC3-3, which in turn activates NAND gate IC7-6 (when the test mode flip-flop is set) and setting the common of the reverse buttons low. The forward motion commands are terminated when either the STOP pushbutton is activated, clearing the test mode flip-flop, or end of tape is detected, in which case EOT1 true is inverted by IC17-4, disabling NAND gate IC7-3, and setting the common of both forward motion buttons high. Similarly the reverse motion can be terminated by activating the STOP pushbutton, which terminates all test mode operations, or when load point is detected, in which case LP true is inverted by IC17-3 and disables NAND gates IC3-3 and IC7-6, setting the common of the reverse buttons high. The pushbutton control module also drives the test panel indicators, lighting the data lamp when any data is being processed by the write/read electronics, illuminating the skew indicator when the skew is out of adjustment, illuminating the EOT indicator when the transport is at end of tape, and illuminating the LOAD POINT indicator when the transport is at the beginning of tape.

## TYPE 4843 AUTO POWER RESTART PC BOARD

### CIRCUIT DESCRIPTION

### (OPTIONAL PC BOARD)

#### Introduction

When incorporated in any of the Kennedy Model 9000, 9100, 9300, 9700, 9800, or 9832 recorders, the type 4843 Pushbutton Control module allows use of several factory optional features. These functions are determined by optional straps and the use of components in the APR field. Not all functions and/or combinations of such are available with every 9000 series recorder. Refer to schematic 401-4843-001 and the dash number of your particular 4843 module for features that have been incorporated and tested at the time your unit was built. Due to the interaction of several of these options the user is advised to consult the factory in writing if he desires to incorporate any additional optional features through field modification. Failure to do so invites the possibility of voiding the warranty of the particular recorder involved.

The major optional features along with suggested usage are outlined below. (Reference is made to schematic 401-4843-001.)

#### ON TAPE (OT)

Determined by the placement of option strap 1. If this option is specified at the time of factory order, the operator cannot place the tape unit on line until a reel of tape is loaded and positioned at or past the BOT tab.

#### ONLINE LOCK (ONLL)

Determined by the placement of option strap 2. When specified at the time of factory order, this feature prevents the operator from manually taking the tape unit off line via the front panel switch, unless the tape controller has allowed him to do so. This signal is not normally gated with select and is an input signal line on interface connector J1-A.

#### FAST (FST)

Determined by diode CR2 and a special control interface module. When specified at the time of factory order, this feature allows interface control of high speed forward and high speed reverse motion of tape. It is used in conjunction with the Synchronous Forward, Synchronous Reverse, and the optional Fast line at the control interface connector of the deck. High speed forward and reverse commands will be accepted when the tape is on line and selected. The high speed reverse command will be implemented at any time when tape is positioned past the BOT tab and the high speed forward command will be carried out only when tape is positioned at or between the BOT and EOT tabs (past EOT, a fast forward

command will cause tape to advance at the normal synchronous forward speed). Note: This feature should be used only for purposes of high speed search, as writing cannot be done at high speeds.

#### AUTO POWER RESTART (APR)

Determined by the configuration of components in the APR field and external assemblies (in some models) driven by this module. When specified at the time of factory order, this option will protect the tape unit against "brownout" and will automatically power up, load, and set the deck on line under certain conditions. With the standard APR option this circuitry continually monitors the line voltage and whether the tape unit is on line or off line. If the external line voltage falls below a minimum value required by the tape deck, this option will force the deck into an off-line state along with issuing a BROKEN TAPE command (i.e., the reel and capstan servos will be disabled and any write current is inhibited). When the input power level returns to an acceptable value, the APR circuitry will do one of two things, depending on whether the deck was on line before the power fell: (1) nothing, if the deck was in an off-line state, or (2) load, advance tape several inches and place the deck on line if it was previously in an on-line state. Additionally, if APR circuitry is used in the Model 9832 buffer, it will issue an INITIALIZE signal (i.e., clear the buffer memory) when power is returned.

#### OPTIONAL LOAD ON LINE FEATURE

A factory variation (to be specified at time of order) of the standard APR option is the LOAD ON LINE (LOL) feature. If specified, this allows the user, through a control interface signal, to load and place the tape deck on line. The LOL signal is acknowledged only after external power has dropped and returned to an acceptable level and the deck is in an unloaded state. If the LOL feature is used, it is the user's responsibility to provide a TTL logic low-going pulse (minimal pulse duration 500 milliseconds) after power is returned to an acceptable level. The LOL signal is not gated with SELECT and appears as an input signal on interface connector J1A.

#### SUGGESTED USAGE OF APR FEATURE

The standard APR circuitry is activated only when the deck is placed on line and is deactivated when the deck is placed off line. (In the case of the LOL variation, circuitry is activated only when power has failed and then returned when the deck is in an unloaded state.) Thus, when manually loading a reel of tape on the deck, the APR feature is transparent to the operator and only comes into play when

external power has failed with the tape deck in an on-line state. The tape deck must be mounted in a vertical position to avoid spilling of tape in the case of power failure. Proper positioning of commands after the APR circuitry has repowered the deck depends on the particular mode of operation and should be determined by the application. If a rewind was in process at the time of power failure, the tape may stop and become repositioned up to 5 feet before load point. For proper operation in this case, tape should be spaced forward 6 feet and then rewound. For any other mode of operation, it is suggested that a REWIND command be issued immediately after an APR power-up. The LOL signal is not gated with SELECT and appears as an input signal on interface connector J1A.

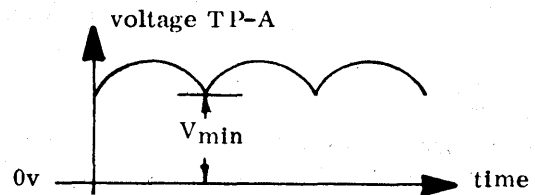
The APR circuitry is designed to operate under conditions of power failure external to the tape deck. Power failure simulations made via the front panel power switch do not come under the above category since this power switch is located between an input power RFI filter and the power transformer.

#### AUTO POWER RESTART ADJUSTMENT

Normal field adjustment of the Auto Power Restart board is not required unless a new APR board is placed in a machine or an existing board has been refurbished. If this is the case, the following field procedure is recommended:

1. Power up machine and adjust R18 fully CW.
2. Monitor TP-A and TP-B with a scope. TP-B is a logic level and will be high. TP-A is the

preregulated +5 vdc and will appear on the scope as illustrated below:



3. Adjust the input power voltage to the machine so that the value of  $V_{min}$  (as shown above) equals the value stated on schematic 401-4843-001 of the APR PC board.

4. Turn R18 CCW until the voltage appearing at TP-B goes low.

#### APR OPERATION IN MODELS 9100/9300

APR operation in these vacuum column tape transports is identical to the above description with the following exceptions:

- a) Manual and power failure initiated load sequences take approximately twice as long due to the increased tape tensioning time required to prevent oversized tape loops from forming in the vacuum columns during a power failure.
- b) The manual and APR load sequences are now as follows: Tension Tape; Load Columns, Search forward to load point; if load point is not found after a given time out period, rewind to load point; then place unit online.

## TYPE 3194/3645 RAMP GENERATOR

### CIRCUIT DESCRIPTION

The ramp generator produces the proper analog signal inputs to the capstan servo system to control the direction and velocity of tape motion. The outputs are voltages that rise and fall linearly at controlled rates to highly stable levels. These analog signals are controlled by digital logic outputs from the control section. Waveforms produced are shown with the schematic.

Two similar ramp generator circuits are provided: one for normal speed operation and one for high speed operation. IC4 is an operational amplifier in the RUN NORMAL SPEED circuit. The amplifier output is normally saturated in the negative direction. When its positive input at pin 5 is high, the output saturates at +10 volts. This occurs when the RUN NORMAL input sets flip-flop IC7. IC4 feeds FETs Q1, Q2 which are connected in a constant-current circuit. The magnitude of current flow in the circuit is controlled by R3 and R4. R3 controls current in the positive-going direction, or start ramp, while R4 controls the negative-going stop ramp.

Since C1 is charged by a constant current, its voltage rises linearly until clamped by CR1 to a value one diode drop below +5 volts. Q3 is an emitter follower whose output rises to a value of +5 volts, since the emitter can rise one diode drop higher than the base. When the input from IC7 to IC4 drops, the voltage fed to Q1, Q2 goes to -10 volts and C1 is discharged linearly until clamped by the base-collector diode of Q3. Since Q3 base goes one diode drop negative, and the emitter is at zero, a positive-going ramp has been generated.

The ramp voltage output from Q3 is fed to the FET switches Q4 and Q5. If forward direction has been selected, Q4 is on and Q5 is off. The ramp is then amplified by unity gain operational amplifier IC3, without inversion, and appears as a positive-going ramp at test point A. If reverse is selected, Q5 is on and Q4 is off. The ramp is then fed to the inverting input of IC3 and appears as a negative-going ramp at test point A. Forward/reverse selection is controlled by flip-flop IC6 and Q9, Q10.

Ramp amplitude and, therefore, tape speed is controlled by normal speed control R14 and output summing resistor R15. The fast forward and reverse ramps are produced by a similar circuit involving amplifiers IC1 and IC2. However, since rewind

speed and ramp time need not be precisely controlled, resistors are used instead of FETs to charge and discharge C4 and produce an approximate 0.5 sec rise/fall time. CR9 and CR10 isolate the ramp output from any small offsets that may be present in IC2. Rewind speed is controlled by summing resistor R16. Operational amplifier IC5 at zero ramp output has a slight bias produced by R37 and R38, keeping its output negative. When the ramp rises above the bias, IC5 switches to positive output, indicating that the tape is running. This output is used to gate off the input circuits through IC10 and IC9. Flip-flops IC7 and IC8 may be reset by run normal or run fast inputs going false, but cannot be set again until the tape comes to a stop. This prevents damage from illegal commands and reduces timing requirements.

Type 3645 Ramp Generator includes an additional flip-flop, IC11-8, whose function is to enable consecutive RUN NORMAL commands to be received without requiring the tape to ramp down to a stop following each normal speed operation. Following a RUN FAST command, however, flip-flop IC11 is set by IC8, inhibiting any RUN NORMAL commands until the tape comes to a stop, at which point IC9-6 clears IC11-9, and the 0 output at IC11-8 enables IC7-2.

### ADJUSTMENT PROCEDURE

Start/stop time adjustment:

- a. Arrange input signals to the tape transport to start and stop machine. Rate must be such as to allow full ramp time.
- b. Adjust start ramp (R3) for required time, observing with oscilloscope at test point A.
- c. Adjust stop ramp (R4) for required time. Time is measured from maximum volts to zero volts.

Speed adjustment:

- a. Using a master skew tape, drive the transport in a forward direction at normal speed.
- b. Observe data rate at read amplifiers and adjust R14 for correct timing.

## TYPE 3844 SENSOR AMPLIFIER DRIVER

### CIRCUIT DESCRIPTION

This module responds to signals from photoresistive cells which sense load point and end of tape reflective strips, and broken tape. In addition, this module contains the file protect circuitry, the write and the erase head drives.

#### BOT, EOT, AND BKN SENSOR AMPLIFIERS

The load point sensor amplifier and the end of tape sensor amplifier operate interdependently to detect the load point and the end of tape markers. The active components in detecting EOT and load point are two operational amplifiers, IC6 and IC8, and two transistors, Q1 and Q2, in conjunction with associated components. Transistors Q1 and Q2 act as current sources; potentiometer R16 is used to adjust the transistor base currents to equalize the voltage at the inputs of IC8, the load point sensor amplifier, and IC6, the end of tape sensor amplifier. Resistors R18, R19, R20, and R21 are used to bias the amplifiers' inputs when plain tape is in front of the photo sensors. When either the load point marker or the end of tape marker is detected, the resistance of the respective photoresistive cell is lowered by approximately 60 percent of its unilluminated value. Each cell is returned to +10 volts, and a 30 percent change in its resistance, causing a 30 percent change in the input potential, will be sufficient to switch the output of the respective operational amplifier. Resistors R17 and R22 serve as feedback loops for noise protection. Thus when load point is detected, the load point sensor output as input pin Y of this module saturates IC8, causing its output to go high, and is inverted twice by IC7 to generate LOAD POINT LDP true at output pin 19 to the Pushbutton Control module. The output of inverter IC7-8 is also supplied to an edge circuit which produces a 1  $\mu$ sec pulse on the trailing edge of LDP. This pulse is output at pin 8 to the Pushbutton Control module. The EOT sensor amplifier operates in the same manner, generating a high output when the EOT marker is detected, and supplying EOT true at output pin X to the Pushbutton Control and Control Interface modules.

When the broken tape photoresistive cell is illuminated the resistance of the cell is reduced enough for the +10 volts to turn on transistor Q3. The collector of the transistor goes to ground, generating BROKEN TAPE BKN true at output pin 18. When  $\overline{\text{LOAD}}$  is high at input pin U the output of IC4-8 is low. This causes the collector of Q3 to be low through diode CR3 and

the BKN output will be true at output pin 18. Also when power is initially turned on capacitor C9 will cause the BKN output to be high which presets the LOAD flip-flop on the Interface Control module.

#### FILE PROTECT CIRCUITS

The file protect switch output is supplied to this module at input pin T. When a reel is loaded without a write enable ring, the switch contact remains grounded; the switch input at pin T is inverted by IC2-6 and enables NAND gate IC4-13. The gate is activated when BKN is true before the transport is loaded. Whenever the LOAD pushbutton has not been energized, IC4-8 low grounds the clear input of flip-flop IC4-1 through diode CR14. IC4-2 then issues FILE PROTECT  $\overline{\text{FPT}}$  true at output pin 9 to the Interface Control card, while the 0 output of IC4 high is inverted by IC2-8 to turn off transistor Q5, disabling the file protect solenoid output at pin P.

When a reel with a write enable ring is used, the file protect switch is opened, setting input pin T high and enabling NAND gate IC2-13. Again the gate can be activated only when BKN is high, before the transport is loaded. The output of the gate then goes low to set flip-flop IC4-5; the flip-flop can be set only after  $\overline{\text{LOAD}}$  has gone false. This provision is made to ensure that the write mode can be selected only at the time tape is first loaded. Once flip-flop IC4 is set, its 1 output issues  $\overline{\text{FPT}}$  false, and after being inverted by IC1-10 lights the WRITE ENABLE LAMP through output pin H. The 0 output of the flip-flop low is inverted by IC2-8 and turns on transistor Q5, activating the file protect solenoid through pin P. The file protect solenoid then draws in the switch pin, and the transport is ready for the write operation.

#### WRITE, ERASE DRIVES

When the file protect switch is grounded, it also turns off transistor Q7, in turn shutting off the current at the base of Q8. This cuts off the write head and erase head drive currents supplied by transistor Q8. In order for the write and erase drives to be turned on, the file protect switch must be opened and WRITE READY must be true at input pin 2. This will activate NAND gate IC2-3, causing op amp IC3 to turn off transistor Q9, in turn enabling transistor Q8 to turn on and supply the write and erase head drives at pins 22 and J.

The zener diode into the base of Q7 detects when power is being dropped. This turns off Q7 early enough in the power down sequence to turn on Q9 and remove the head voltage supplied by Q8. This avoids putting unwanted remnants on tape during a power failure.

## TYPE 4306 SERVO PREAMPLIFIER

### CIRCUIT DESCRIPTION

#### (25 IPS Models and Lower)

This module contains the capstan servo and reel servo amplifier stages. The following paragraphs describe their operation.

#### CAPSTAN SERVO AMPLIFIER STAGE

The capstan servo amplifier portion of this module is a part of a velocity servo system which produces accurately controlled capstan speeds with linear ramp-ups and ramp-downs. The analog linear signal supplied from the Ramp Generator module is input at pin N of this module and is summed with the output of the DC tachometer coupled to the capstan motor shaft. Tachometer output is supplied at pin P of this module. Any difference between the two voltages is amplified by operational amplifier IC5. The amplification of IC5 is controlled by two negative feedback loops, one supplied directly from the output of IC5 through resistors R39, R40 and capacitor C9, and the other from the capstan motor through resistor R71. The zero offset of the amplifier is adjusted by potentiometer R56 to eliminate capstan creep during standstill as described below.

The output of amplifier IC5 is supplied to a pair of complementary driver stages, including transistors Q11, Q12, Q17, and Q18. The output of these stages is supplied to a pair of power transistors located on the heatsink servo power assembly, at the rear of the unit. The power transistors' output then energizes the capstan motor, advancing tape at accurately controlled speeds.

#### REEL SERVO AMPLIFIERS

Takeup and supply reel servos are provided to maintain tape tension at a constant value. Three main components are included: magpot position sensor, reel servo amplifier, and reel motor.

The magpot position sensor measures tape tension by the position of a spring loaded buffer arm. At the approximate center of the arc, sensor output is zero. As the buffer arm moves off center, a positive or negative voltage is produced which is proportional to the error. This error voltage is summed with the modified capstan tachometer signal and is amplified to energize the respective reel motor, producing sufficient torque to return the buffer arm to the center of its arc. Only the takeup amplifier stage will be described below; the operation of the supply amplifier stage is identical.

The takeup magpot signal is supplied at pin F of this module. The magpot corrective voltage is fed through R9 and AC coupling C3 and R8 to the inverting input of operational amplifier IC1. In order to speed up the response of the reel servo in higher speed machines, the output of the tachometer capstan motor is summed with the magpot corrective voltage through summing resistor R10. The tachometer signal is modified by the network, which includes operational amplifiers IC6 and IC7, to reduce the tachometer's effect during high speed operations. The response of the reel servos to capstan acceleration is only critical during ramp-ups to normal running speed. During high speed operations, however, the ramp times are very long (approximately 0.5 sec) and the tachometer signal is very large. Consequently, the signal is modified so that up to approximately 40 ips it increases linearly, but at speeds exceeding 40 ips it decreases, reducing its effect.

Potentiometer R58 controls the effect of the modified tachometer signal on takeup reel response. This potentiometer is adjusted to reduce the buffer arm travel to a minimum, optimizing the reel response to both the capstan motion and to the buffer arm position. The adjustment is described below.

The output of the reel servo amplifier on this module is supplied to a pair of power transistors located on the servo power assembly on the heatsink at the rear of the unit. The output of the power transistors energizes the respective reel motor, returning the buffer arms to their proper locations as described above.

#### SERVO ADJUSTMENTS

##### Capstan Zero Offset

This adjustment becomes necessary when capstan creep is detected during standstill. To adjust follow these steps:

- a. Connect an oscilloscope probe to monitor the voltage at output pin X, measuring the output of the capstan servo amplifier stage.
- b. With the transport ON LINE and loaded but in a stopped condition, adjust potentiometer R56 so that a straight-line trace is produced. Use the 0.5v/cm scale on the oscilloscope.
- c. Observe that the capstan does not rotate.

### Buffer Arm Travel

Potentiometers R57 (supply arm) and R58 (takeup arm) are adjusted on this card to minimize the respective buffer arm travel, preventing arm bottoming and overshooting. The adjustment procedure is as follows:

- a. Load a full reel of tape on the supply reel.
- b. With the transport off line, press the test panel TEST MODE pushbutton.
- c. Press the FORWARD RUN and REVERSE RUN pushbuttons alternately, initiating synchronous forward and reverse tape motions. (A remote tape control unit may be used if the test panel is not available.)
- d. Adjust potentiometer R57 on this module until the travel of the SUPPLY buffer arm is at minimum during the ramp-ups and ramp-downs.
- e. Repeat the above steps for the TAKEUP arm, adjusting potentiometer R58.
- f. If a test box or computer diagnostic program is available this adjustment can be more easily performed doing a write/backspace/write, using a very long data block length (16K if available). Adjust for minimum arm travel. When adjusting supply servo arm response (R57) all the tape should be on the supply reel. When adjusting the response of the takeup servo arm at R58, all the tape should be on this takeup reel at EOT.



## TYPE 4606 SERVO PREAMPLIFIER

### CIRCUIT DESCRIPTION

#### (37.5 IPS Models and Higher)

This module contains the capstan servo and reel servo amplifier stages. The following paragraphs describe their operation.

#### CAPSTAN SERVO AMPLIFIER STAGE

The capstan servo amplifier portion of this module is a part of a velocity servo system which produces accurately controlled capstan speeds with linear ramp-ups and ramp-downs. The analog linear signal supplied from the Ramp Generator module is input at pin N of this module and is summed with the output of the DC tachometer coupled to the capstan motor shaft. Tachometer output is supplied at pin P of this module. Any difference between the two voltages is amplified by operational amplifier IC5. The amplification of IC5 is controlled by two negative feedback loops, one supplied directly from the output of IC5 through resistors R39, R40 and capacitor C9, and the other from the capstan motor through resistor R71. The zero offset of the amplifier is adjusted by potentiometer R56 to eliminate capstan creep during standstill as described below.

The output of amplifier IC5 is supplied to a pair of complementary driver stages, including transistors Q11, Q12, Q17, and Q18. The output of these stages is supplied to a pair of power transistors located on the heatsink servo power assembly, at the rear of the unit. The power transistors' output then energizes the capstan motor, advancing tape at accurately controlled speeds.

#### REEL SERVO AMPLIFIERS

Takeup and supply reel servos are provided to maintain tape tension at a constant value. Three main components are included: magpot position sensor, reel servo amplifier, and reel motor.

The magpot position sensor measures tape tension by the position of a spring loaded buffer arm. At the approximate center of the arc, sensor output is zero. As the buffer arm moves off center, a positive or negative voltage is produced which is proportional to the error. This error voltage is summed with the modified capstan tachometer signal and is amplified to energize the respective reel motor, producing sufficient torque to return the buffer arm to the center of its arc. Only the takeup amplifier stage will be described below; the operation of the supply amplifier stage is identical.

The takeup magpot signal is supplied at pin F of this module. The magpot corrective voltage is fed through R9 and AC coupling C3 and R8 to the inverting input of operational amplifier IC1. In order to speed up the response of the reel servo in higher speed machines, the output of the tachometer capstan motor is summed with the magpot corrective voltage through summing resistor R10. The tachometer signal is modified by the network, which includes operational amplifiers IC6 and IC7, to reduce the tachometer's effect during high speed operations. The response of the reel servos to capstan acceleration is only critical during ramp-ups to normal running speed. During high speed operations, however, the ramp times are very long (approximately 0.5 sec) and the tachometer signal is very large. Consequently, the signal is modified so that up to approximately 40 ips it increases linearly, but at speeds exceeding 40 ips it decreases, reducing its effect.

Potentiometer R58 controls the effect of the modified tachometer signal on takeup reel response. This potentiometer is adjusted to reduce the buffer arm travel to a minimum, optimizing the reel response to both the capstan motion and to the buffer arm position. The adjustment is described below.

The output of the reel servo amplifier on this module is supplied to a pair of power transistors located on the servo power assembly on the heatsink at the rear of the unit. The output of the power transistors energizes the respective reel motor, returning the buffer arms to their proper locations as described above.

#### SERVO ADJUSTMENTS

##### Capstan Zero Offset

This adjustment becomes necessary when capstan creep is detected during standstill. To adjust follow these steps:

- a. Connect an oscilloscope probe to monitor the voltage at output pin X, measuring the output of the capstan servo amplifier stage.
- b. With the transport ON LINE and loaded but in a stopped condition, adjust potentiometer R56 so that a straight-line trace is produced. Use the 0.5v/cm scale on the oscilloscope.
- c. Observe that the capstan does not rotate.

### Buffer Arm Travel

Potentiometers R57 (supply arm) and R58 (takeup arm) are adjusted on this card to minimize the respective buffer arm travel, preventing arm bottoming and overshooting. The adjustment procedure is as follows:

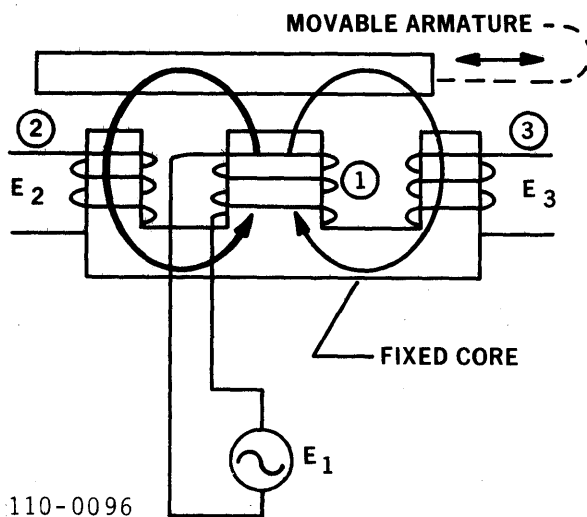
- a. Load a full reel of tape on the supply reel.
- b. With the transport off line, press the test panel TEST MODE pushbutton.
- c. Press the FORWARD RUN and REVERSE RUN pushbuttons alternately, initiating synchronous forward and reverse tape motions. (A remote tape control unit may be used if the test panel is not available.)
- d. Adjust potentiometer R57 on this module until the travel of the SUPPLY buffer arm is at minimum during the ramp-ups and ramp-downs.
- e. Repeat the above steps for the TAKEUP arm, adjusting potentiometer R58.
- f. If a test box or computer diagnostic program is available this adjustment can be more easily performed doing a write/backspace/write, using a very long data block length (16K if available). Adjust for minimum arm travel. When adjusting supply servo arm response (R57) all the tape should be on the supply reel. When adjusting the response of the takeup servo arm at R58, all the tape should be on this takeup reel at EOT.

## TYPE 4210 MAGPOT TENSION ARM POSITION SENSOR

### CIRCUIT DESCRIPTION

In the reel servo system it is necessary to produce an analog signal representing tension arm position. The signal must be zero at the nominal resting position of the tension arms and should linearly represent angular deviations from the center of arm travel by positive and negative voltages. A common method utilizes lamps, photocells, and a shutter to produce the required voltage. This method suffers from the mortality of lamps and the relatively slow response of photocells.

The magpot operates as a differential transformer, an example of which is shown below.



110-0096

Magnetic flux produced by current in winding (1) will produce voltages  $E_2$  and  $E_3$  in the other windings. If the armature is symmetrically located with respect to (2) and (3), flux in the two windings will be equal, and since they have the same number of turns,  $E_2 = E_3$ . If the armature is displaced as shown,  $E_2 > E_3$  since the flux coupling  $E_3$  has been reduced. Displacement in the opposite direction produces  $E_3 > E_2$ . Displacement from center then is represented by  $E_0 = E_2 - E_3$ . In the configuration shown this relation is linear only for very small displacements because area relations are not linear.

The magpot is an adaptation of the above scheme in that there are three windings on a magnetic core. The core in this case is a ferrite pot core while the armature is half a pot core. The windings (2) and (3) are around legs of the pot core while (1) is around

the center portion common to the two legs. Winding (1) is energized by a high frequency oscillator (approximately 200 kHz). The magpot is in balance and  $E_2 = E_3$  when the armature couples equally to the two legs. As the armature is rotated the area available for magnetic flux increases linearly for one leg and decreases linearly for the other leg. Thus the difference in induced voltages is a linear representation of angular movement.

The 200 kHz oscillator is a Hartley circuit comprising Q1, C1, C2, R1, R2. It produces a 40 volt ptp sine wave across the primary winding.

The two secondary windings are connected in series and their voltages are rectified by CR1, CR2. The two rectified voltages are subtracted and referenced to ground. Thus the input to IC1 operational amplifier is a dc voltage equal to  $E_2 - E_3$ . This voltage is null when  $E_2 = E_3$  and is positive or negative depending upon which is larger. Secondary voltages induced are at all times large enough to overcome the diode drops in CR1, CR2.

DC output of the rectifier circuit is amplified by IC1 and fed from the output to the appropriate reel servo amplifier.

Voltage output for a given angular deflection depends upon coupling between the fixed core and armature at that setting. The gain relations are such that a spacing of 0.030 inch between core and armature results in  $\pm 5v$  output for full arm travel. Spacing is established by two 0.015 inch thick plastic spacer washers on the shaft.

#### Adjustment Procedure

If adjustment should be required:

1. Remove tape from machine.
2. Place a short length of tape in front of broken tape sensor.
3. Turn power on, press LOAD. Reels will rotate.
4. Hold tension arm in approximate center of arc. Reel rotation should stop.
5. If reel continues to rotate loosen setscrew holding the armature to the tension arm shaft.

6. Rotate armature until reel hub motion ceases. Press firmly against the fixed core to maintain core to armature spacing.
7. Tighten setscrew.
8. Move arm to limits of travel and observe directions of reel hub rotation. There are two null positions  $180^{\circ}$  apart. The sense of the output is reversed for one null causing hub rotation to be wrong. If this null has been chosen, loosen setscrew, rotate armature  $180^{\circ}$ , and repeat.
9. Check output at pin 4 using a voltmeter. Total output swing should be between 10 and 12 volts ( $\pm 5$ v nominal).

## TYPE 3631 READ PREAMPLIFIER

### CIRCUIT DESCRIPTION

Read Preamplifier Type 3631 includes nine identical amplifier stages which accept the analog signals from the read head winding and supply the amplified outputs to the read amplifier modules. In seven-track recorders the channel 0 and 1 stages are left out.

The 0 channel amplifier stage is shown in the schematic; the other channels are identical. The amplifier stage consists of high gain operational amplifier IC1 and negative feedback including resistors R2, R3, R4, R5, and capacitor C2. The input head signal is filtered by resistor R1 and capacitor C1, and is supplied to the noninverting input of IC1. The negative

feedback network controls the output amplitude and response.

In NRZ only tape units, potentiometer R4, located in the feedback network, is adjusted so that the amplified analog output at test point A is 9 volts peak to peak while writing 800 flux reversals per inch. In phase encoded only tape units, potentiometer R4 is adjusted for 5 volts peak to peak output while writing 3200 flux reversals per inch. In dual density tape units, potentiometer R4 is adjusted for 9 volts peak to peak output while writing 800 flux reversals per inch.

## TYPE 3845 DELAY TIMING MODULE

### CIRCUIT DESCRIPTION

This module contains the crystal oscillator and dividing network which produce the synchronous clocks used by the read and write electronics. In addition, this module includes the read data strobe generation network, a read skew delay counter, the gap detect network, and the SELECT 2 circuitry. These functions are discussed in detail below.

#### CRYSTAL CONTROLLED OSCILLATOR AND DIVIDING NETWORK

The oscillator consists of crystal Y1 used in a feedback loop between two inverter sections of IC5. The oscillator output is supplied to a dividing network which provides the synchronous clocks used in the transport. The dividing network includes divide by 2 and 8 counter IC2, flip-flops IC1, and divide by 16 counter IC4. The clocks generated by the network are a function of tape speed and a series of switches is provided to divide the master oscillator frequency according to the tape speed of the particular transport. The switch positions for the different tape speeds are tabulated on the schematic diagram. The clocks output by the network are  $f_1$ , a square wave at 32 times the character frequency, and  $f_r$ , a square wave at the character frequency.

#### SKREW CHECK COUNTER AND READ DATA STROBE GENERATION

The wire-OR'd peak pulses supplied from the read amplifier stages are input at pin R of this module, and after being inverted by IC14 are supplied to NAND gate IC14-10. At this time the Q output of flip-flop IC15-3 is high, enabling IC14-9, and the peak pulses are gated through IC14-8 to the direct-clear input of flip-flop IC15-13. During each data character the pulse of the leading channel direct-clears flip-flop IC15-13, setting the  $\bar{Q}$  output high to enable the skew counter, divide-by-16 IC16. The counter is clocked by  $f_1$  at 32 times the data frequency. During a test mode, TEST MODE true at input pin H (from the pushbutton control module) direct-sets the skew counter to the count of 11. The counter then counts from 11 to 16, at which point its  $Q_d$  output toggles flip-flop IC15-12, locking itself. The skew tolerance is restricted to the period of the count; any peak coming in after the skew counter has set flip-flop IC15 would cause a skew indication, as explained below. Once IC15 flip-flop has been toggled to the set state, its  $\bar{Q}$  output goes low and toggles flip-flop

IC12-12. The  $\bar{Q}$  output of IC12-2 goes low, is inverted by IC10-12 and supplies DATA TRANSFER true to the read amplifier module, shifting the data to the output buffer on those modules. The next  $f_1$  pulse after DATA TRANSFER toggles the second IC12 flip-flop to the set state; the  $\bar{Q}$  output of IC12-6 goes low, is inverted twice by two IC10 inverters and is output as the READ DATA STROBE RDS at output pin A to the interface. IC12-6 low also direct-clears the first IC12 flip-flop; consequently the next  $f_1$  pulse also toggles the second IC12 flip-flop to the cleared state and terminates the data strobe. Should the skew tolerance be exceeded and a pulse arrive after flip-flop IC15 has been set, the lagging pulse will direct-clear IC15-13 again and enable NAND gate IC13-12. The gate is activated when IC12-5 goes high and fires the skew one-shot IC11-4, illuminating the skew lamp on the test panel. During a normal write mode the skew tolerance is increased, as WRITE READY true and TEST MODE false activate NAND gate IC14-6 and direct-set the skew counter to the count of four. This increases the skew tolerance from the five counts used during the test mode to 12 counts. During the read only mode both WRDY and TEST MODE are false, and the skew tolerance count is increased to 16, or half a character space.

#### GAP DETECT COUNTER

The gap detect counter consists of two divide-by-16 counters in tandem: IC6 and IC7. It is clocked by  $f_1$  at 32 times the data frequency. After each data pulse flip-flop IC15-13 is direct-cleared, its  $\bar{Q}$  output goes high and resets the gap counter. After the skew delay IC15 is set again and the gap counter is enabled. Following the last data character of a record, the gap counter is not reset immediately but keeps counting. When it reaches the count of 32, one character time after the last data character of the block, the  $Q_b$  output of IC7 activates NAND gate IC9-13. IC9-11 goes low and direct-clears flip-flop IC8-13. The Q output of the flip-flop in turn direct-sets the gap detect flip-flop IC15-10, generating GAP DETECT true at output pin H to the interface, provided that the transport is selected and on line (SLT1 true). The Q output of IC8-3 low also activates NOR gate IC9-1, keeping the counter enabled and counting while the check characters are being read; otherwise the LRC and CRC characters will have reset the gap counter, signifying end of gap. When the gap counter reaches

the count of 256 it toggles flip-flop IC8-9, enabling NAND gate IC9-10. Thirty-two counts later, equivalent to the tenth character space of the interrecord gap, IC9-8 goes low and toggles flip-flop IC8-12 to the set state. The Q output of the flip-flop goes high and activates NAND gate IC9-4, so that the gap counter will clear when the next data character is detected (IC15-2 high).

#### SELECT 2 GENERATION

SELECT 2 is used to enable the output data gates on the read amplifier modules. SLT2 is generated by combining BUSY  $\overline{\text{BSY}}$  false, LOAD POINT LP false,

SELECT 1 SLT1 true, and RUN NORMAL  $\overline{\text{RNN}}$  true. Once  $\overline{\text{RNN}}$  goes true, initiating synchronous tape motion, a delay count consisting of divide-by-16 counters IC18 and IC19 is enabled. The counters are advanced by data frequency clock  $f_r$ . On the count of 128 the  $Q_d$  output of IC19 goes high and activates NAND gate IC20 if all the requirements mentioned above are met. IC20-8 goes low, is inverted by IC20-6, and generates SLT2 true at output pin L to the read amplifiers. The purpose of the SLT2 delay is to disable the output data gates during the tape ramp-up. When IC19-11 goes high IC17-8 goes low preventing further clocks to the counter. The counter is reset to the count of zero when RUN NORMAL  $\overline{\text{RNN}}$  goes high.

## TYPE 4118 DELAY TIMING MODULE

### CIRCUIT DESCRIPTION

This module contains the crystal oscillator and dividing network which produce the synchronous clocks used by the read and write electronics. In addition, this module includes the read data strobe generation network, a read skew check counter, the gap detect network, and the SELECT 2 circuitry. These functions are discussed in detail below.

#### CRYSTAL CONTROLLED OSCILLATOR AND DIVIDING NETWORK

The oscillator consists of crystal Y1 used in a feedback loop between two inverter sections of IC11. The oscillator output is supplied to a dividing network which provides the synchronous clocks used in the transport. The dividing network includes divide by 2 and 8 counter IC3, and divide by 16 counter IC12. The clocks generated by the network are a function of tape speed and a series of switches is provided to divide the master oscillator frequency according to the tape speed of the particular transport. The switch positions for the different tape speeds are tabulated on the schematic diagram. The clocks output by the network are  $f_1$ , a square wave at 32 times the character frequency, and  $f_r$ , a square wave at the character frequency.

#### SKEW CHECK COUNTER AND READ DATA STROBE GENERATION

The wire-OR'd peak pulses supplied from the read amplifier stages are input at pin R of this module. After being inverted by IC15 they are supplied to IC15-10. At this time the Q output of flip-flop IC16-3 is high, enabling IC15-9, and the peak pulses are gated through IC15-8 to the direct-clear input of flip-flop IC16-13. During each data character the pulse of the leading channel direct-clears flip-flop IC16-13, setting the  $\bar{Q}$  output high to enable the skew counter, divide-by-16 IC17. The counter is clocked by  $f_1$  at 32 times the data frequency. During a test mode, TEST MODE true at input pin H (from the pushbutton control module) direct-sets skew counter IC17 to the count of 11. The counter then counts from 11 to 16, at which point its  $Q_d$  output toggles flip-flop IC16-12, locking itself. The skew tolerance is restricted to the period of the count; any peak coming in after the skew counter has set flip-flop IC16 would cause a skew indication, as explained below. Once the IC16 flip-flop has been toggled to the set state, its  $\bar{Q}$  output goes low and toggles flip-flop

IC14-12. The Q output at IC14-2 goes low, is inverted by IC12-12 and supplies DATA TRANSFER true to the read amplifier module, shifting the data to the output buffer on those modules. The next  $f_1$  pulse after DATA TRANSFER toggles the second IC14 flip-flop to the set state; the  $\bar{Q}$  output of IC14-6 goes low, is inverted twice by two IC12 inverters and is output as the READ DATA STROBE RDS at output pin A to the interface. IC14-6 low also direct-clears the first IC14 flip-flop; consequently the next  $f_1$  pulse also toggles the second IC14 flip-flop to the cleared state and terminates the data strobe. Should the skew tolerance be exceeded and a pulse arrive after flip-flop IC16 has been set, the lagging pulse will direct-clear IC16-13 again. The gate is activated when IC14-5 goes high and fires the skew one-shot IC11-4, illuminating the skew lamp on the test panel. During a normal write mode the skew tolerance is increased, as WRITE READY true and TEST MODE false activate NAND gate IC15-6 and direct-set the skew counter to the count of four. This increases the skew tolerance from the five counts used during the test mode to 12 counts. During the read only mode both WRDY and TEST MODE are false, and the skew tolerance count is increased to 16, or half a character space.

#### GAP DETECT COUNTER

The gap detect counter consists of two divide-by-16 counters in tandem: IC8 and IC9. It is clocked by  $f_1$  at 32 times the data frequency. After each data pulse flip-flop IC16-13 is direct-cleared, its  $\bar{Q}$  output goes high and resets the gap counter. The skew delay IC16 is reset and the gap counter is enabled. Following the last data character of a record, the gap counter is not reset immediately but keeps counting. When it reaches the count of 32, one character time after the last data character of the block, the  $Q_b$  output of IC9 activates NAND gate IC11-13. IC11-11 goes low and direct-clears flip-flop IC10-13. The Q output of the flip-flop in turn direct-clears the gap detect flip-flop IC16-10, generating GAP DETECT true at output pin H to the interface, provided that the transport is selected and on line (SLT1 true). The Q output of IC10-3 low also activates NOR gate IC18-10, keeping the counter enabled and counting while the check characters are being read. Otherwise the LRC and CRC characters will have reset the gap counter, signifying end of gap. When the gap counter reaches



the count of 256 it toggles flip-flop IC10-9, enabling NAND gate IC11-3. Sixty-four counts later, equivalent to the tenth character space of the interrecord gap, IC10-8 is activated and toggles flip-flop IC12-12 to the set state. The Q output of the flip-flop goes high and activates NAND gate IC18-4, clearing the gap counter, and keeping it cleared until the first character of the next block is read.

#### SELECT 2 GENERATION

SLT2 Delay disables the output data gates during tape ramp-up. SELECT 2 is used to enable the output

data gates on the read amplifier modules. SLT2 is generated by combining BUSY  $\overline{\text{BSY}}$  false, LOAD POINT LP false, SELECT 1 SLT1 true, and RUN NORMAL  $\overline{\text{RNN}}$  true. Once  $\overline{\text{RNN}}$  goes true, initiating synchronous tape motion, a delay counter consisting of divide-by-16 counter IC20 and IC21 is enabled. The counter is advanced by data frequency clock  $f_r$ . On the count of 128 the  $Q_d$  output of IC21 goes high and activates NAND gate IC22 if all the requirements mentioned above are met. IC22-8 goes low, is inverted by IC12-6, and generates SLT2 true at output pin L to the read amplifiers. The purpose of the SLT2 delay is to disable the output data gates during the tape ramp-up.

## TYPE 4178 QUAD READ AMPLIFIER

### CIRCUIT DESCRIPTION

Quad Read Amplifier Type 4178 accepts amplified head signals from the head preamplifier module and supplies decoded and deskewed data outputs to the interface. Each module contains four amplifier stages, and each recorder contains two of these modules. The channel P amplifier stage is located on Read Amplifier/Clipping Control module. The operation of the channel A amplifier stage is explained in the following paragraphs. The other amplifier stages operate identically.

The amplified analog signal is supplied from the read preamplifier at input pin E. The signal is filtered through R1, C1; the negative half waves are routed through diode CR1 while the positive half waves are routed through CR2. CR1 and CR2 are back biased respectively by the negative and positive clipping levels, supplied from the Read Amplifier/Clipping Control Module, to eliminate spurious baseline pulses. The negative half waves are then differentiated by C4 and R6 and are input at the inverting input of operational amplifier IC1. At the leading edge of the negative analog half wave the differentiated output of C4 and R6 swings negative, crossing zero at the peak of the analog signal and then going positive until the trailing edge of the analog signal. Normally the op amp output is low, since the non-inverting input of IC1 is negatively biased through R7 and R9. When the leading edge of the differentiated signal exceeds the input threshold, the output of the amplifier swings positive. The amplifier output returns to 0v at the zero crossover of the differentiated signal, corresponding to the peak of the input analog signal. A similar transition occurs for the positive half wave, since it is input at the noninverting input of the amplifier. Consequently the amplifier output goes high and returns low for each 1 character, with the negative-going transition occurring at the analog peak. The output of the amplifier is limited by diodes CR3 and CR4 and is inverted by NAND gate

IC2-3. IC2-3 output is supplied to a filtering network consisting of C6, R11, R12, and CR5, whose output is in turn supplied to the Schmitt trigger input of one-shot IC3. The output of IC2-3 is normally high, and the voltage at the input of IC3-5 is at 3.3v. When the output of IC1 swings positive, IC2-3 goes low and capacitor C6 discharges through R12 with a slow time constant, approximately 5  $\mu$ sec at 25 ips. The voltage is clamped at 0v by diode CR5. When the output of IC1 goes low again at the peak of the analog input, IC2-3 goes high and C6 charges with a much faster time constant, approximately 300 nsec. When C6 charges up to 1.8v, one-shot IC3 triggers, generating a 300 nsec pulse. The  $\bar{Q}$  output of the one-shot is connected back to IC2-2, disabling the gate and preventing the one-shot from being retriggered by spurious pulses on the input.

The positive pulse generated by the Q output of IC3 is inverted by IC2-11 and is output as PULSE OUT at pin V. The pulses of all the amplifier stages are wire-OR'd and supplied to the Delay Timing module where they are used for read deskewing and read data strobe generation. The  $\bar{Q}$  output of one-shot IC3 direct-sets flip-flop IC4-4, the data storage register. The Q output of IC4-5 sets the D input of the output register IC4-12 high. A skew delay time is provided for all channels to be read after the leading data pulse is detected. DATA TRANSFER (supplied from the Delay Timing module) toggles the output register flip-flops of all channels simultaneously after the allowed skew delay time, outputting the deskewed, decoded data to NAND gate IC2-9 and, on its trailing edge, clears the first stage of IC4. The gate is enabled by SELECT 2 true, supplied from the Delay Timing module at input pin S. IC2-8 supplies the output data at pin Z to the interface. The length of the skew delay time is varied depending on the operation being performed. This is described in the Delay Timing module circuit description.

## TYPE 4179 READ AMPLIFIER CLIPPING CONTROL

### CIRCUIT DESCRIPTION

This module contains the P channel read amplifier stages and the read amplifier clipping level control. The operation of the P channel amplifier is explained in the circuit description of the Quad Read Amplifier module, and the read amplifier clipping level control is explained below.

The read amplifier clipping control provides four clipping levels to the read amplifier: normal, low, high, and very high. When an error is detected during a read operation the transport may be commanded by the tape control unit to backspace over the erroneous block to reread it. The clipping level is kept at a normal level during the first reread. If a second reread is commanded, the clipping level is switched from normal to a lower clipping level, to compensate for a possible partial dropout. If a third reread is initiated, the clipping level is switched to a higher than normal level to eliminate possible baseline noise spikes. During a read after write operation the normal and high clipping levels are combined to supply a still higher clipping level which is not used during a read operation. The switching of the clipping levels is explained in detail below.

The initial state of the circuitry will be both IC10 flip-flops set and both IC11 flip-flops clear. This is established by  $\overline{\text{BUSY}} \overline{\text{BSY}}$  at pin Y true when tape is initially loaded or rewound. Since the first command from load point is always a run forward command,  $\text{RUN NORMAL } \overline{\text{RNN}}$  at pin H true and  $\text{REVERSE SELECT } \overline{\text{RVS1}}$  at pin W false cause IC8-8 to be low clearing IC9 flip-flop. The IC10 flip-flops remain in the set state when clocked by IC9-3 high. The circuitry remains in the states just described until a reverse command is given to the tape unit. When  $\overline{\text{RNN}}$  and  $\overline{\text{RVS1}}$  are true IC8-6 goes low direct-clearing the IC10 flip-flops which causes IC10-8 to go high removing the direct-clear from the IC11 counter flip-flops. Also IC8-6 low sets IC9 flip-flop which makes IC9-6 low; IC11-12 toggles causing IC11-3 to go high putting the counter in the "01" state. The clipping level does not change because the IC12, IC13 gating described in the next paragraph establishes the same clipping level. The circuitry will now remain in this state until a forward command is given. The next forward command causes IC8-8 to go low clearing IC9 flip-flop and toggling IC10-5 high. At this point two things could happen: The tape unit will be commanded to go forward to continue reading the next data block, or to backspace if the interface decides

to reread the data block. If the tape unit is commanded to go forward to continue reading, then IC8-8 low makes IC9-3 high causing IC10-8 to go low which direct-clears the IC11 counter to its initial state. If instead the tape unit is commanded to go in reverse IC11-12 goes low toggling the IC11 counter to its next state. This establishes the next clipping level in the sequence. The IC10 flip-flops are cleared as described above. The IC11 counter will continue to toggle every time the tape unit is commanded to backspace after being commanded to go forward once. Two forward commands in succession will reset the IC11 counter by setting IC10-8 low, and reading continues at the normal clipping level.

The clipping levels established by the IC11 counter through IC12 and IC13 are as follows: (a) 00 and 01 cause IC13-6 and IC13-11 to be low and IC13-3 to be high establishing the normal read clipping level; (b) 10 causes IC13-6 and IC13-3 to be low and IC13-11 to be high establishing the low clipping level; (c) 11 causes IC13-3 and IC13-11 to be low and IC13-6 to be high establishing the high read clipping level.

During a read after write operation  $\text{WRITE READY}$  at input pin J is inverted by IC7-12 and disables the automatic clipping level control by direct-setting IC10 flip-flops, keeping the IC11 counter direct-cleared. At the same time  $\text{WRDY}$  true activates NOR gate IC13-4, enabling the higher clipping level, while the Q output of IC11-5 low enables the normal clipping level. Thus the normal and high clipping levels are combined to generate a still higher clipping level used during read after write only.

The automatic clipping level control is also disabled when the interface supplies  $\text{AUTO DISABLE}$  true at input pin N, or when  $\text{BUSY } \overline{\text{BSY}}$  is true at input pin Y of the module. In either case NOR gate IC7-6 is high, and direct-sets the IC10 flip-flops which in turn keep the reread counter IC11 cleared.

Operational amplifier IC6 is connected with negative feedback through R26, establishing its gain at a value determined by the ratio of the input resistance to +10v switched by IC13 to the value of R26 (22K).

Capacitor C10 acts as an integrator slowing the response of IC6 to a change in input, which avoids coupling enough signal through C4 and C5 into IC1 to cause a spurious output. IC5 is connected as an

inverter outputting an equal but opposite polarity voltage to that voltage at IC6-10. The negative clipping level voltage (TPD) and positive clipping level voltage (TPC) are then applied to each read amplifier

through a resistor dividing network to backbias diodes CR1 and CR2. This establishes the amplitude of analog input from the read preamplifier required for IC1 to switch and thus detect data.

## TYPE 3848 WRITE AMPLIFIERS

### CIRCUIT DESCRIPTION

This module generates the internal write data strobe and contains the write amplifier stages for four of the data channels — channel P through channel 2. These are explained in detail below.

#### WRITE DATA STROBE GENERATION

The Write Data Strobe WDS is input from the interface at pin N and is supplied to an edge circuit consisting of inverters IC5 and IC6, capacitor C8, and NAND gate IC6-8. If Write Ready WRDY and Select SLT1 are true at input pins 12 and 13 of IC6, the gate transmits a short pulse on the leading edge of each input WDS. The pulse is gated through NOR gate IC5-6 and triggers one-shot IC1-1 on its trailing edge. The Q output of the one-shot supplies a positive 0.5  $\mu$ sec pulse which is gated through NAND gate IC7-3, provided that the transport is not in a test mode. The pulse then enables the write NAND gates IC11 and IC15, gating the input write data to the write amplifier stages. It is also supplied as WDS1 to Type 3849 Write Amplifier module. When IC1-13 generates the write strobe, its  $\bar{Q}$  output triggers the second IC1 one-shot, which in turn inhibits IC6 for a 3.5  $\mu$ sec duration, inhibiting any pulses during that time.

If the transport is in test mode, TM true at pin K enables NAND gates IC5-2 and IC7-10, 12 while disabling NAND gate IC7-2. If Write Ready WRDY is true, crystal controlled data frequency  $f_r$ , supplied from the Delay Timing module, is gated through NAND gate IC5-12 and NOR gate IC5-6 to generate the test mode strobes. These are gated through the two IC7 NAND gates and direct-clear the write amplifier flip-flops on this module and on the other Write Amplifier module, writing the all-1 characters of the test mode.

#### WRITE AMPLIFIER STAGES

The data inputs are supplied from the data terminator card at pins R, S, T, and U, are inverted and then strobed through NAND gates IC11 and IC15 by the write data strobe WDS1, generated at test point B. The write channels are then supplied to the amplifier stages, each consisting of a divide-by-16 counter, a pair of flip-flops, and a pair of drivers. The amplifier stages are digitally deskewable, where the delay of channels 0 through 7 is adjusted to coincide with that of the reference channel, channel P, when read back.

The delay of channel P is permanently set to the count of eight, equivalent to a quarter character delay, by counter IC8. Whenever the input data is 1, the WDS pulse is gated through IC11-8 and direct-clears flip-flop IC9-13. The  $\bar{Q}$  output of the flip-flop goes high, removing the direct-clear from the IC8 counter. The counter is then clocked by  $f_1$  at 32 times the data frequency until the count of eight, at which point the  $Q_d$  output of the counter goes low and toggles IC9 flip-flop to the set state. The  $\bar{Q}$  output of IC9 then goes low, locking the counter and toggling the output flip-flop IC9-9. During the next 1 character the same process is repeated with the output flip-flop IC9-9 toggling to the opposite state. When a 0 is input, the input NAND gate IC11-8 does not transmit the write data strobe, and consequently the write amplifier flip-flops are not toggled. The outputs of flip-flop IC9-5, 6 are then supplied to a pair of drivers IC10 which energize the write head, reversing the flux for each 1 while remaining unchanged for each 0, as required for NRZ1.

The operation of the amplifier stages of the eight other channels is identical to that of channel P, except that their delay is digitally adjustable. Four switches are connected to the parallel inputs of the skew delay counters of the eight channels, as shown for data channel 0. The skew of each channel can be measured and adjusted during the write test mode, which writes all 1's characters, by observing the analog outputs at the Type 3631 Read Preamplifier module.

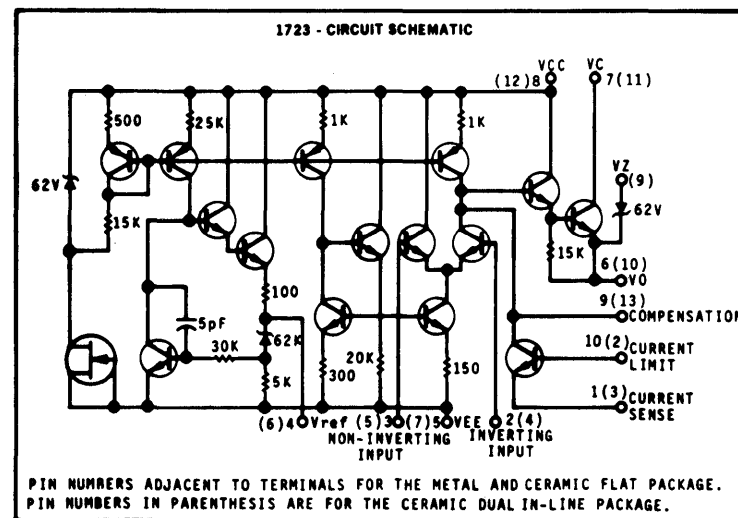
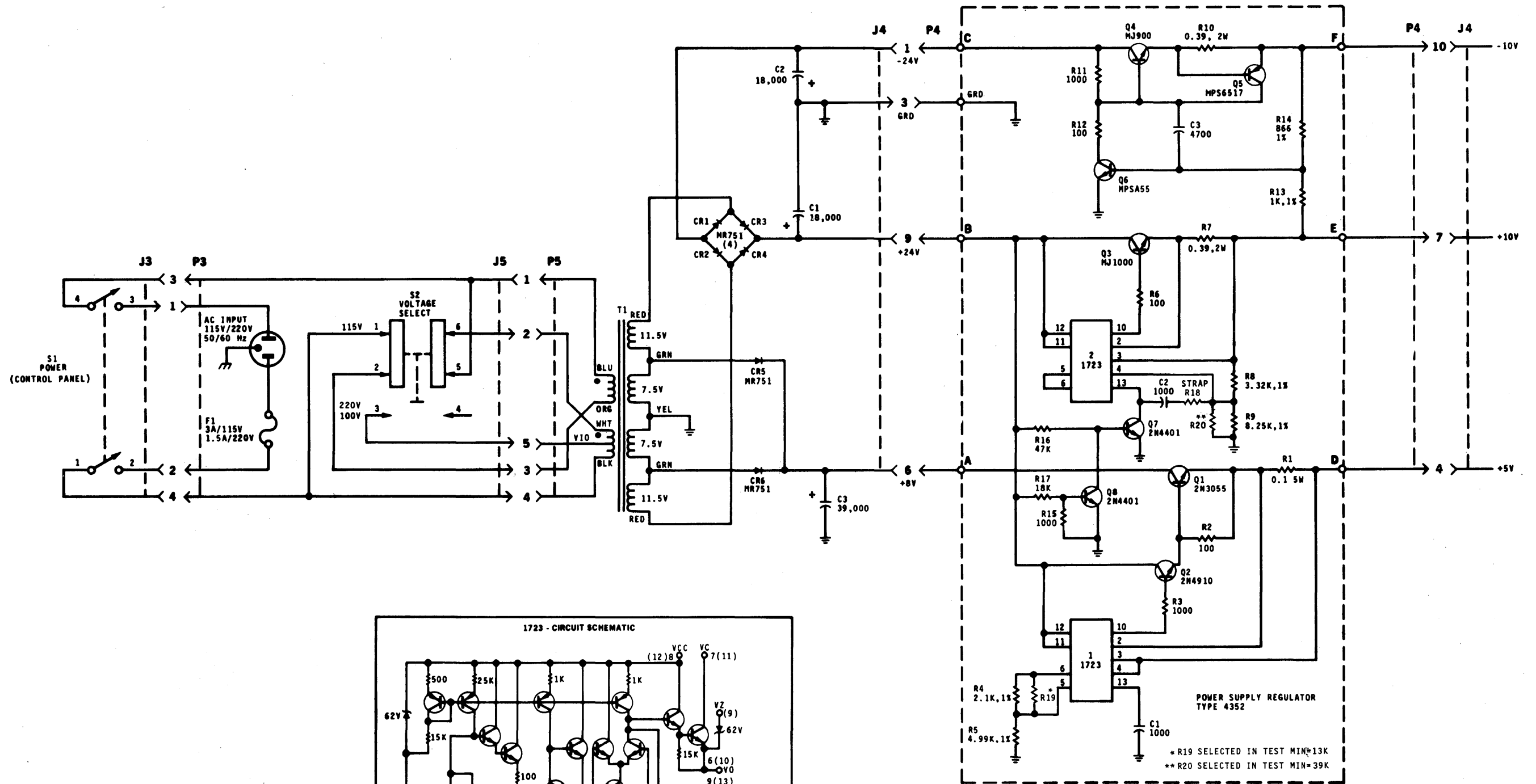
Trigger channel 1 of a dual trace oscilloscope on the P channel so that one peak is easily observed. With channel 2 of the oscilloscope, observe the preamplifier channel that is to be checked or adjusted. Set the switches on the write amplifier channel so that the peaks of the two observed channels coincide. A small amount of jitter will be seen on the channel being adjusted due to tape recorder dynamics. Repeat the observations for all eight channels leaving the P channel as the reference.

Opening the switches reduces the count while closing them increases it. Thus when the switches are all opened the counter is direct-set to 16, gating the data character to the output without any delay. When the switches are all closed the skew counter is set at 0 and the character will be delayed 16 counts, or a quarter of a character time behind channel P.

**WARS**

The Write Amplifier Reset pulse  $\overline{\text{WARS}}$  is input at pin P from the data terminator card, and is gated through NAND gate IC2-3, provided that Select 1 is true, to set flip-flop IC2-12. The 1 output of the flip-flop goes high, removing the direct-clear from shift register IC3. The register is then clocked by  $f_1$  at 32 times the data frequency. On the seventh

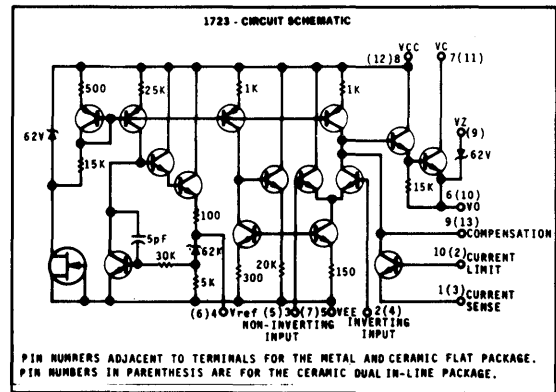
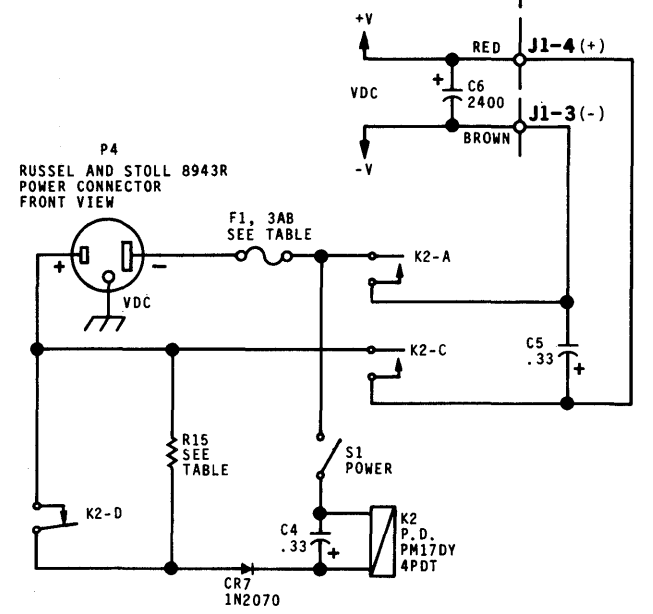
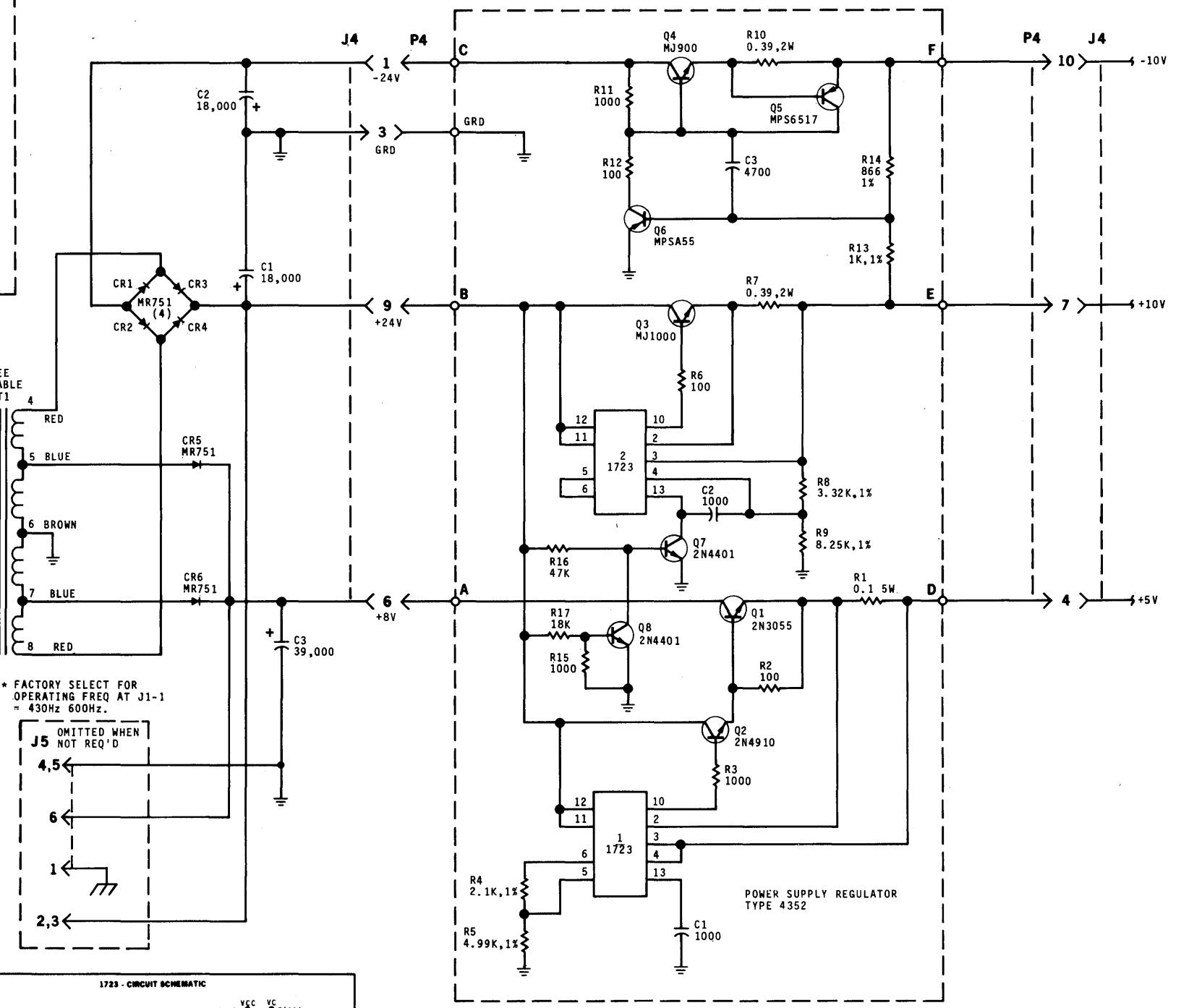
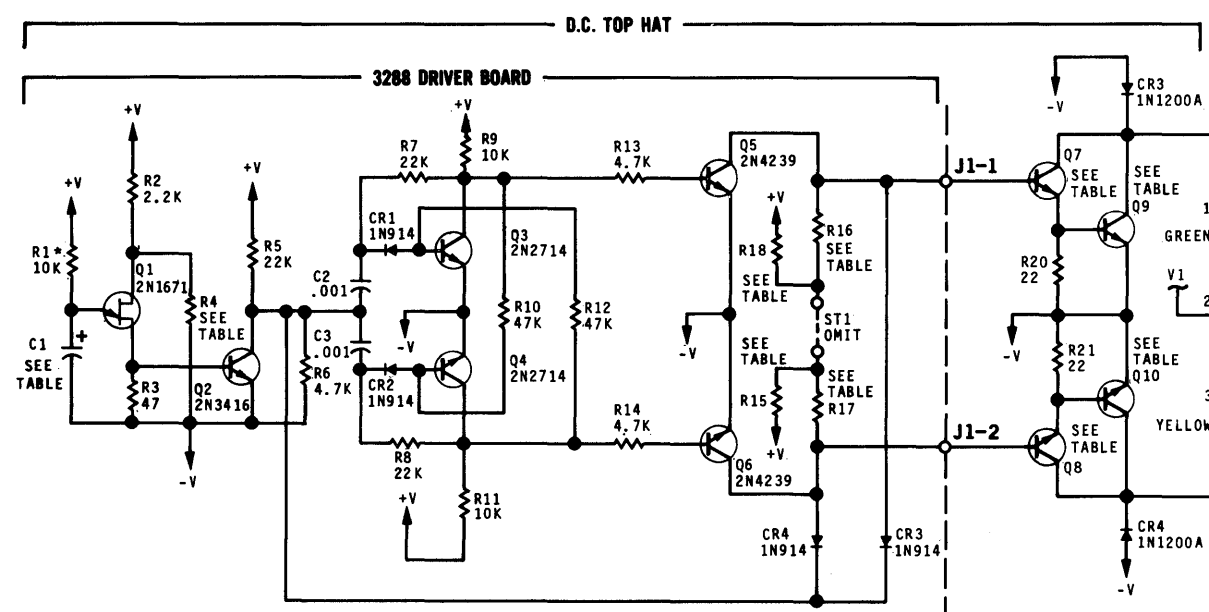
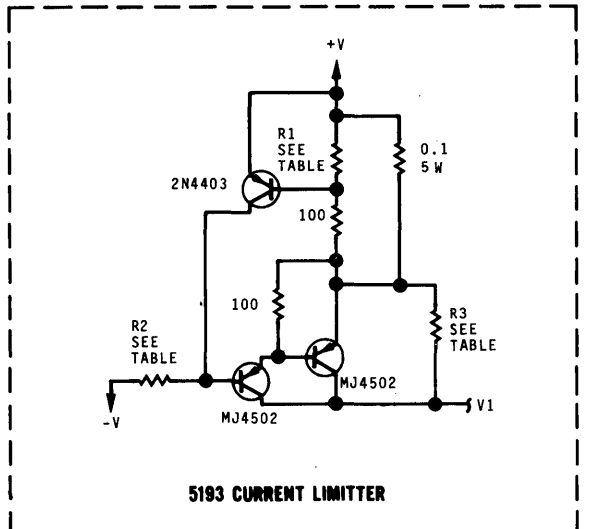
pulse, the  $Q_g$  output of the register goes high and is inverted by IC4-8 to issue  $\overline{\text{WARSI}}$ , resetting the write amplifier flip-flops on this module.  $\overline{\text{WARSI}}$  is also output at pin H to Type 3849 Write Amplifier where it resets the flip-flops of the other amplifier stages. On the eighth pulse to the register the  $Q_h$  output goes high and is inverted by IC4-11, clearing flip-flop IC2 and locking itself until the next  $\overline{\text{WARS}}$  is issued by the interface.



- NOTES:
1. LINE VOLTAGE SELECTION AS SHOWN IS 115/220V, 48-500Hz
  2. TO WIRE FOR 100 VAC OPERATION:  
 MOVE S2-2 (BLK) TO J5-4  
 " S2-3 (VIO) TO S2-4  
 " S2-5 (WHT) TO J5-2
  3. TO WIRE FOR 230VAC OPERATION:  
 CONNECT J5-2 (WHT) TO J5-3 (ORG);  
 J5-5 (VIO) UNUSED

**Power Supply,  
Model 9700/9800**

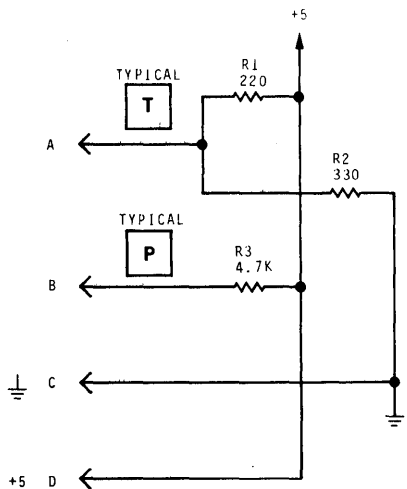
3288 DASH NO	-224F	-228F	-248C	-260B
INPUT D.C. VOLTAGE ±10%	24VDC	28VDC	48VDC	60VDC
R15, R16, R17, R18	120 5W	150 5W	500 5W	2.2K
R4	OMIT	OMIT	2.2K	2.2K
C1	.22	.22	.47	.47
REFERENCE				
Q7, Q8,	MJ802	MJ802	2N3442	MJ410
Q9, Q10	MJ802	MJ802	2N6340	2N6341
F1	15A	15A	7.5A	7.5A
T1	156-4561	156-3909	156-3626	
R15	100 3W	150 3W	400 10W	400 10
5193 DASH NO.	-002A	-002A	-001A	
R1, 1/2W	33	33	100	
R2, 5W	500	500	3.5K	
R3, 5W	1	1	3	



NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

**D.C. Power Supply,  
Model 9700/9800,  
Schematic Diagram**





TYPICAL  
T

TYPICAL  
P

E ← T

F ← T

J ← T

L ← T

M ← OMIT

N ← T

P ← T

R ← P

S ← P

T ← P

U ← P

V ← P

W ← P

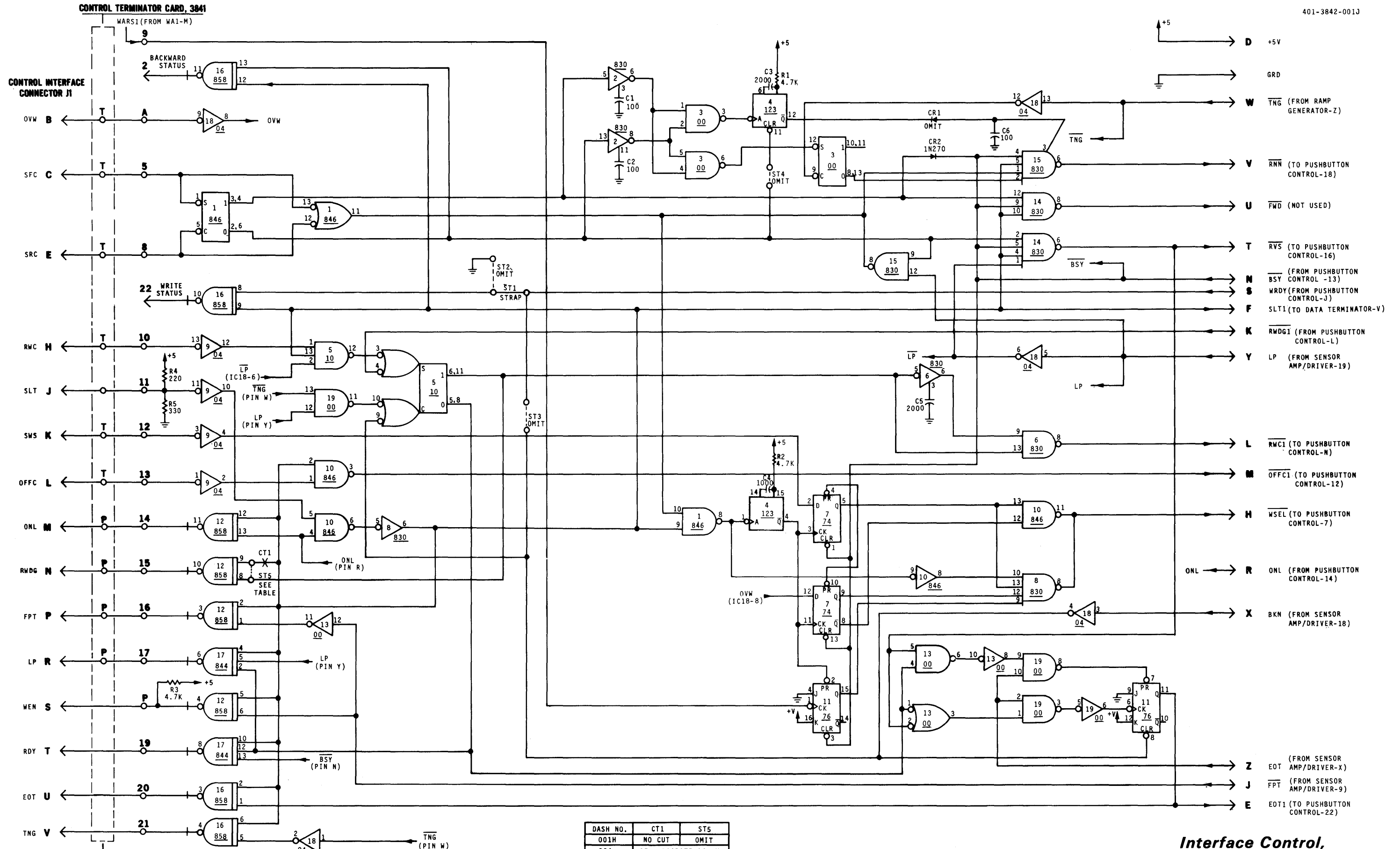
X ← P

Y ← P

Z ← P

NOTE: FOR CIRCUIT CONVENTIONS USED,  
SEE NOTES TO SCHEMATIC SECTION.

**Control Terminator,  
Type 3841-001C,  
Schematic Diagram**

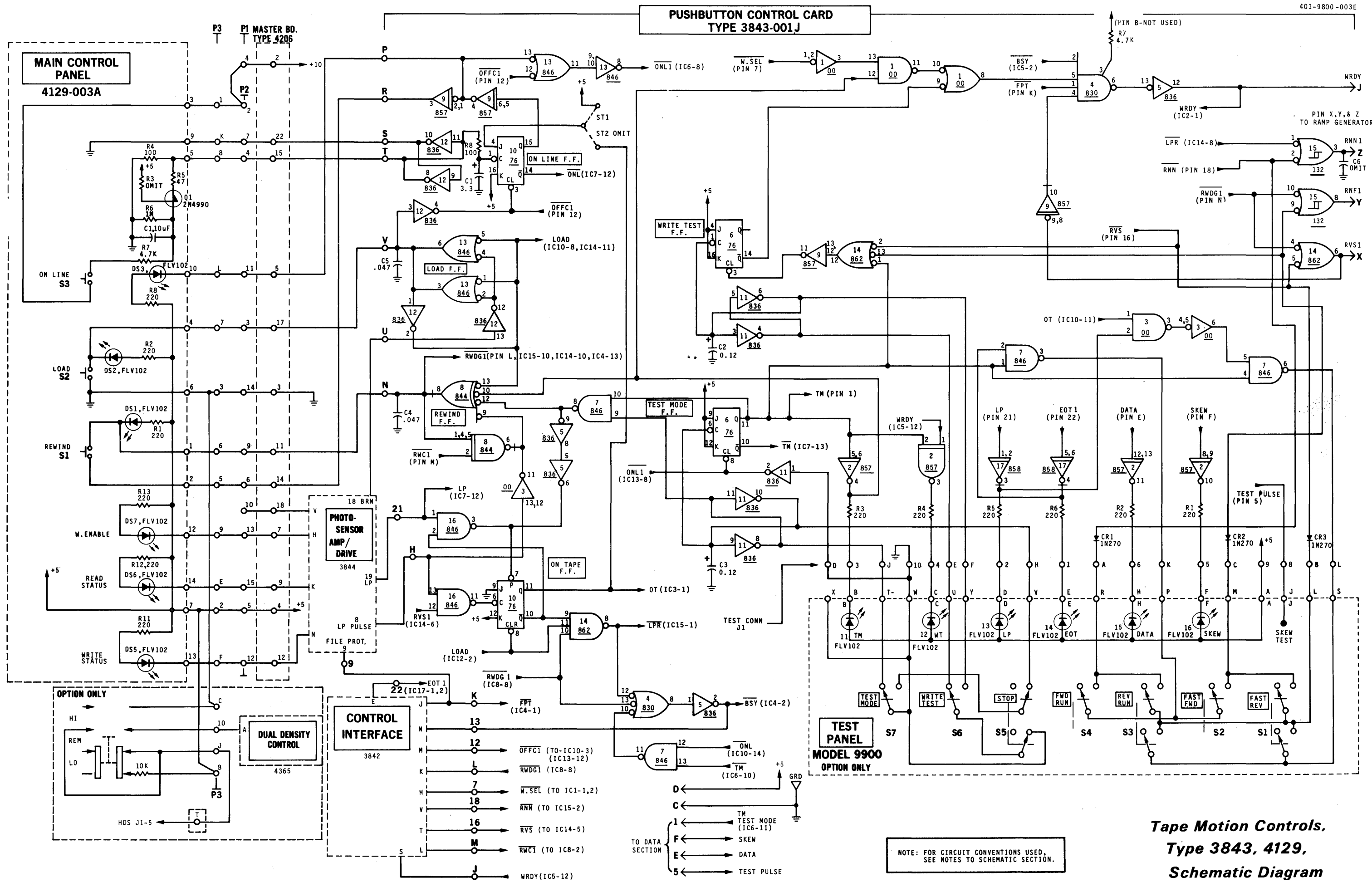


CONTROL TERMINATOR CARD HAS TERMINATORS (T) 220-330 OHM AND PULL-UPS (P) 4.7K AS SHOWN

DASH NO.	CT1	ST5
001H	NO CUT	OMIT
004	SEE SEPARATE SCHEM.	
005	SEE SEPARATE SCHEM.	
006A	CUT	STRAP

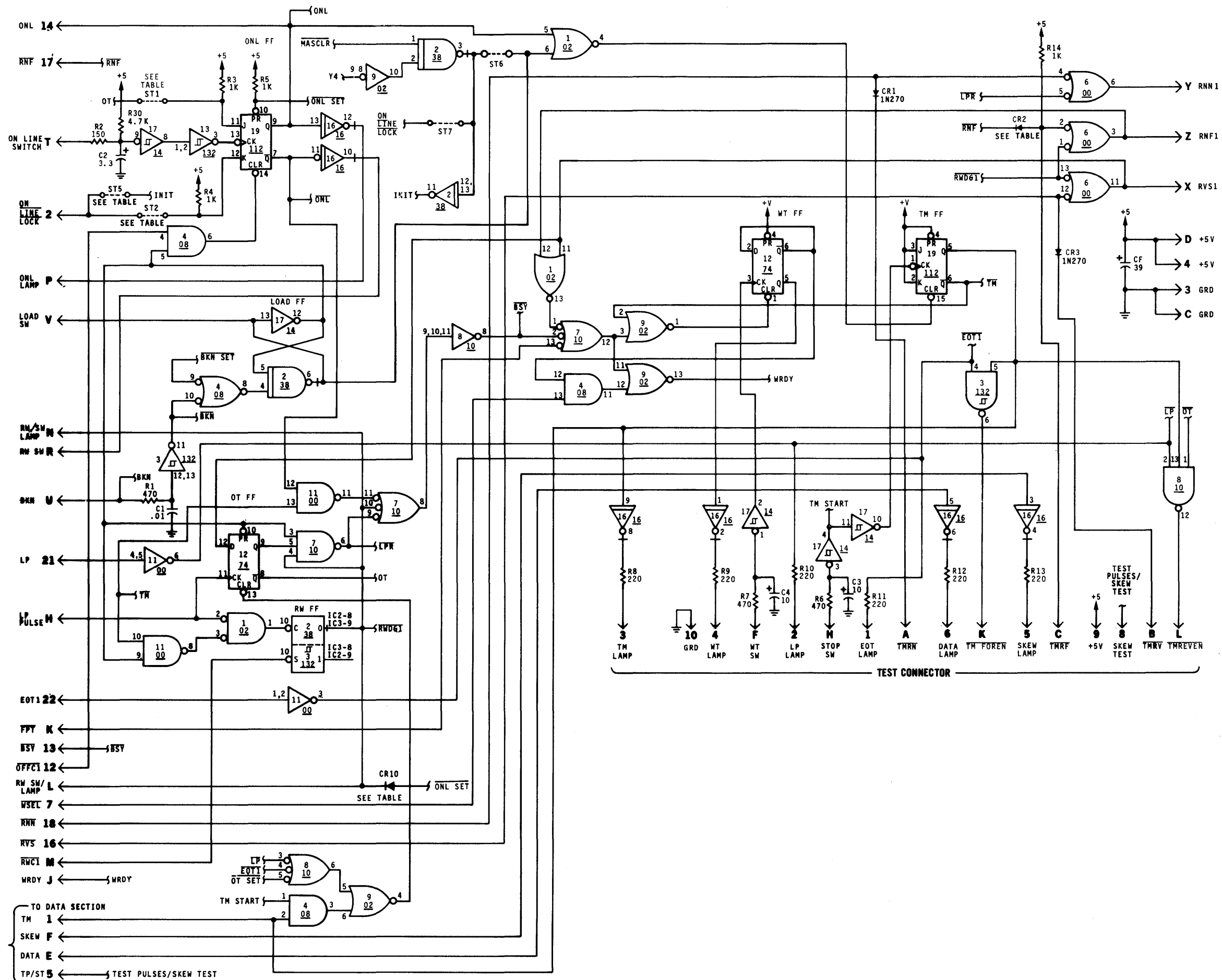
**Interface Control,  
Type 3842,  
Schematic Diagram**





NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Tape Motion Controls, Type 3843, 4129, Schematic Diagram



APR Pushbutton Control  
 Type 4843,  
 Schematic Diagram  
 Sheet 1 of 2

STATE	FUNCTION	NEXT (JUMP)	JUMP CONDITION
0	BKN SET	1 (0)	HAS CLR
1	BKN SET	2 (0)	HAS CLR
2		3	
3		4	
4		F (7)	LOL
5		6	
6		7	
7		8	
8	LDSET	9	
9	LDSET	A	
A	OTSET	B	
B	OTSET	C	
C	ONLSET	D	
D	ONLSET	E	
E	ENABLE	E (0)	HAS CLR
F	ENABLE	F (0)	BKN

X TABLE

DASH NO.	-0YZ	-1YZ	-2YZ	-3YZ	-4YZ	-5YZ	-6YZ	-7YZ	-8YZ
SPEED(IPS)	-	10	12.5	15	18.75	25	37.5	45	75+
R25	OMIT	180K	150K	100K	82K	68K	47K	39K	2.2M

Y TABLE

DASH NO.	-X0Z	-X1Z	-X2Z	-X3Z	-X4Z	-X5Z	-X6Z	-X7Z	-X8Z
FIRST USED ON	9000	9100/9300	9000/9700/9800		9832		9700/9800	9100/9300	9100/9300
FUNCTION	STD	LOL	LOL	AUTO	LOL	AUTO	AUTO RW	AUTO	AUTO / OT
APR CIRCUIT		●	●	●	●	●	●	●	●
ST3, RELAY K1				●	●	●	●	●	●
ST4			●	●	●	●	●	●	●
ST5				●	●	●	●	●	●
ST6	●		●	●	●	●	●	●	●
ST7		●						●	●
ST8	●		●	●	●	●	●	●	●
ST9		●						●	●
DIODE CR10							1N270		

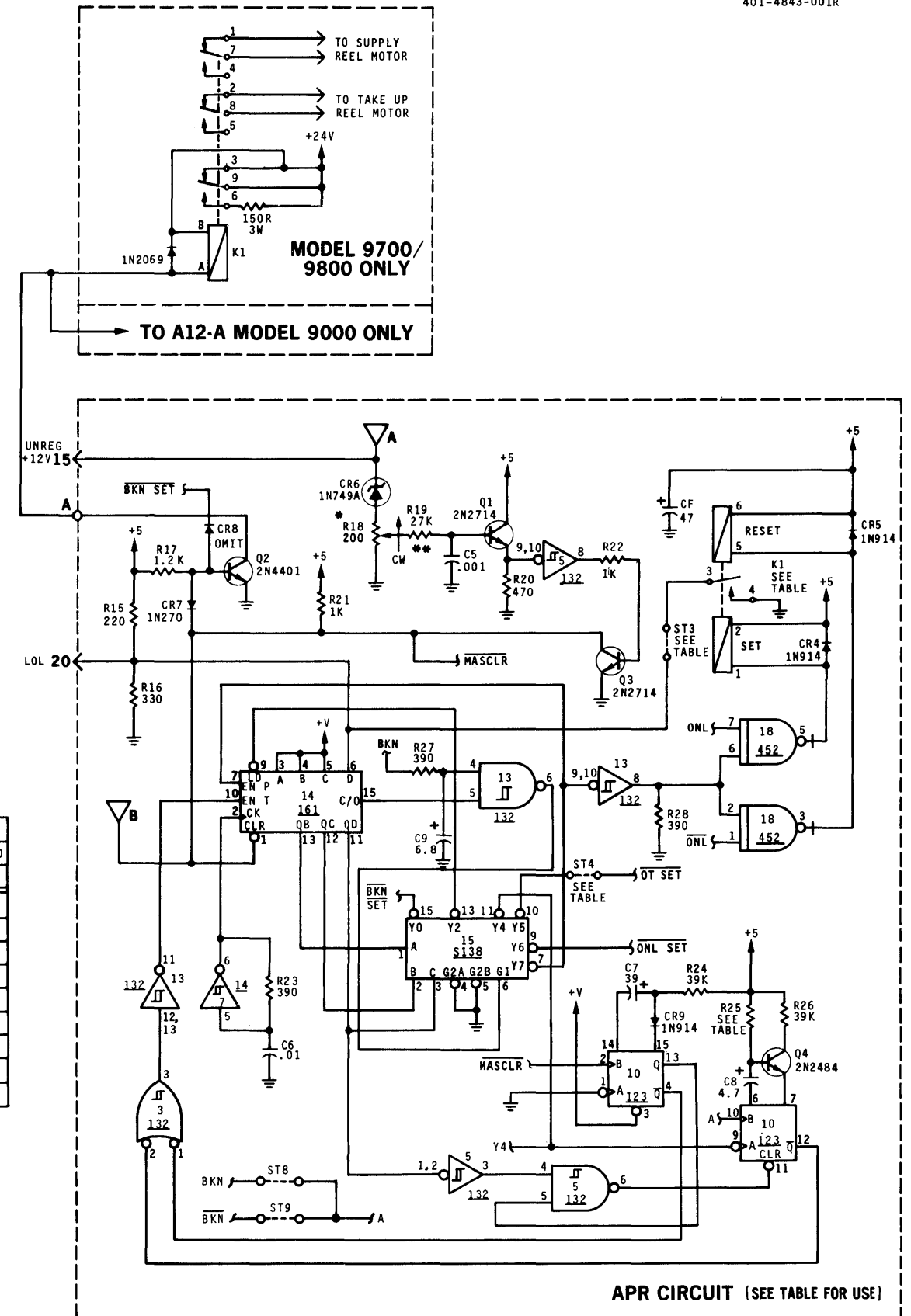
Z TABLE

DASH NO.	-XY1	-XY2	-XY3	-XY4	-XY5	-XY6	-XY7	-XY8
FUNCTION	STD	OT	ONLL	OT/ONLL	FAST	OT/FAST	ONLL/FAST	OT/ONLL/FAST
ST1 (OT)		●		●		●		●
ST2 (ONLL)			●	●			●	●
CR2 (FAST)					1N270	1N270	1N270	1N270

●=USED

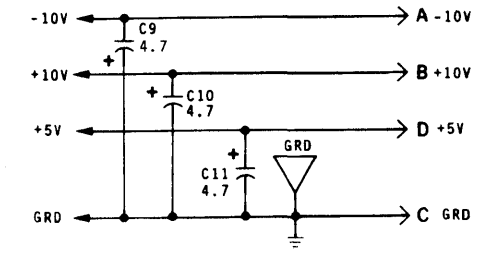
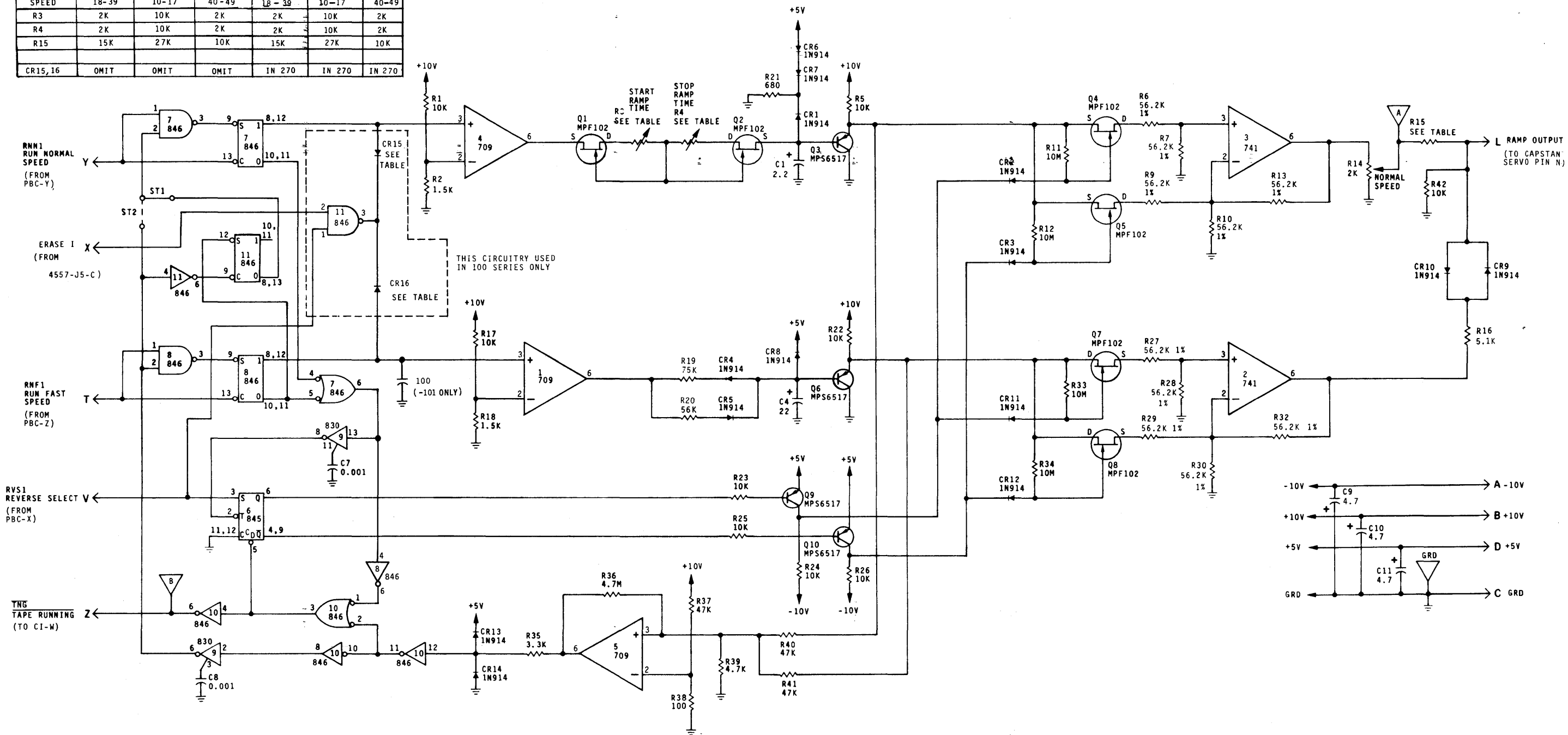
\*ADJUST R18 SUCH THAT SIGNAL AT TEST POINT B GOES LOW WHEN VOLTAGE FALLS BELOW 6.25 ±.15V MIN AT TEST POINT A (NOTE SCHMITT ACTION OF IC5-3)  
\*\*FACTORY SELECT

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

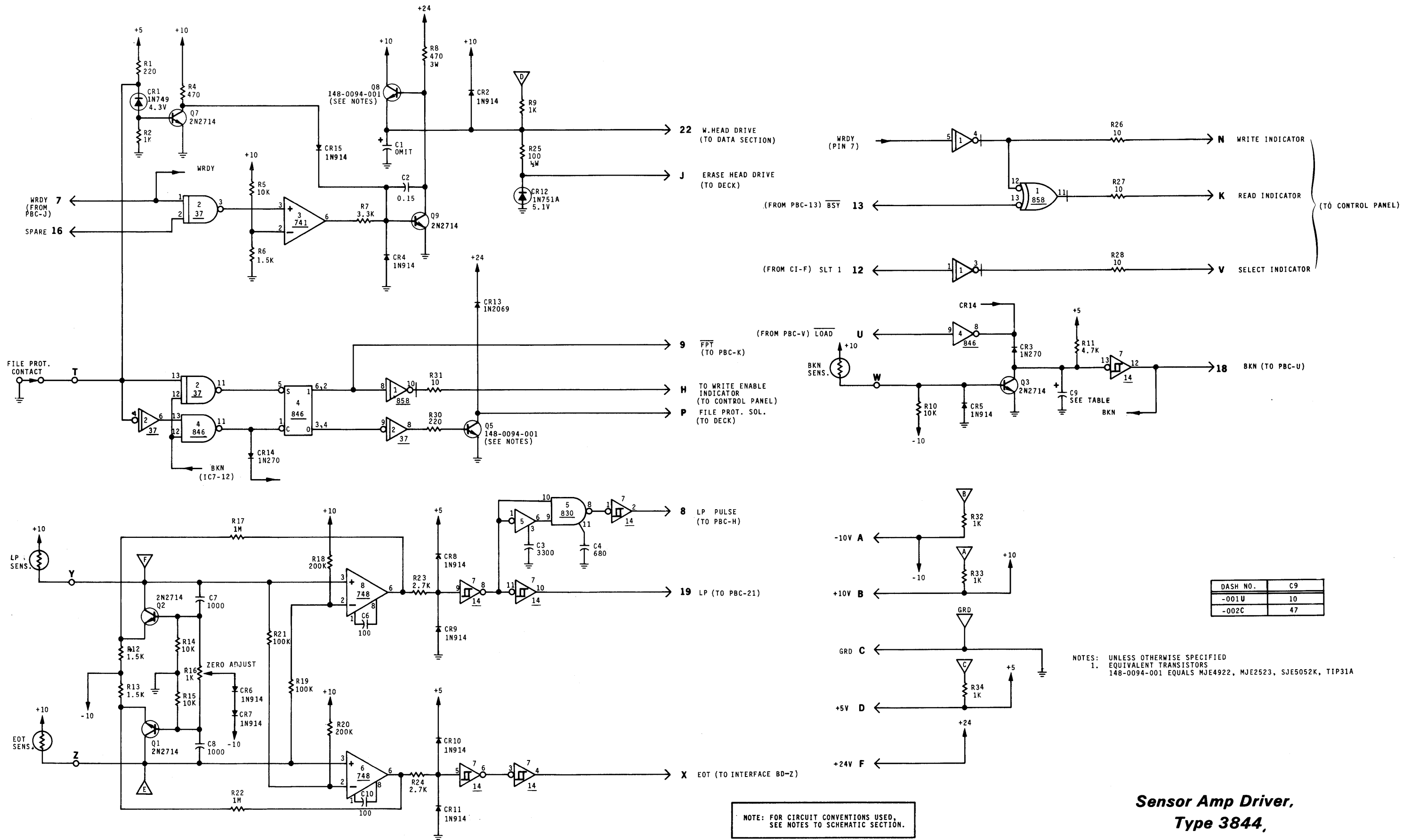


**APR Pushbutton Control,  
Type 4843,  
Schematic Diagram  
Sheet 2 of 2**

DASH NO.	001E	002E	010F	101B	102A	110A
SPEED	18-39	10-17	40-49	18-39	10-17	40-49
R3	2K	10K	2K	2K	10K	2K
R4	2K	10K	2K	2K	10K	2K
R15	15K	27K	10K	15K	27K	10K
CR15,16	OMIT	OMIT	OMIT	IN 270	IN 270	IN 270



Ramp Generator, Type 3645  
Schematic Diagram

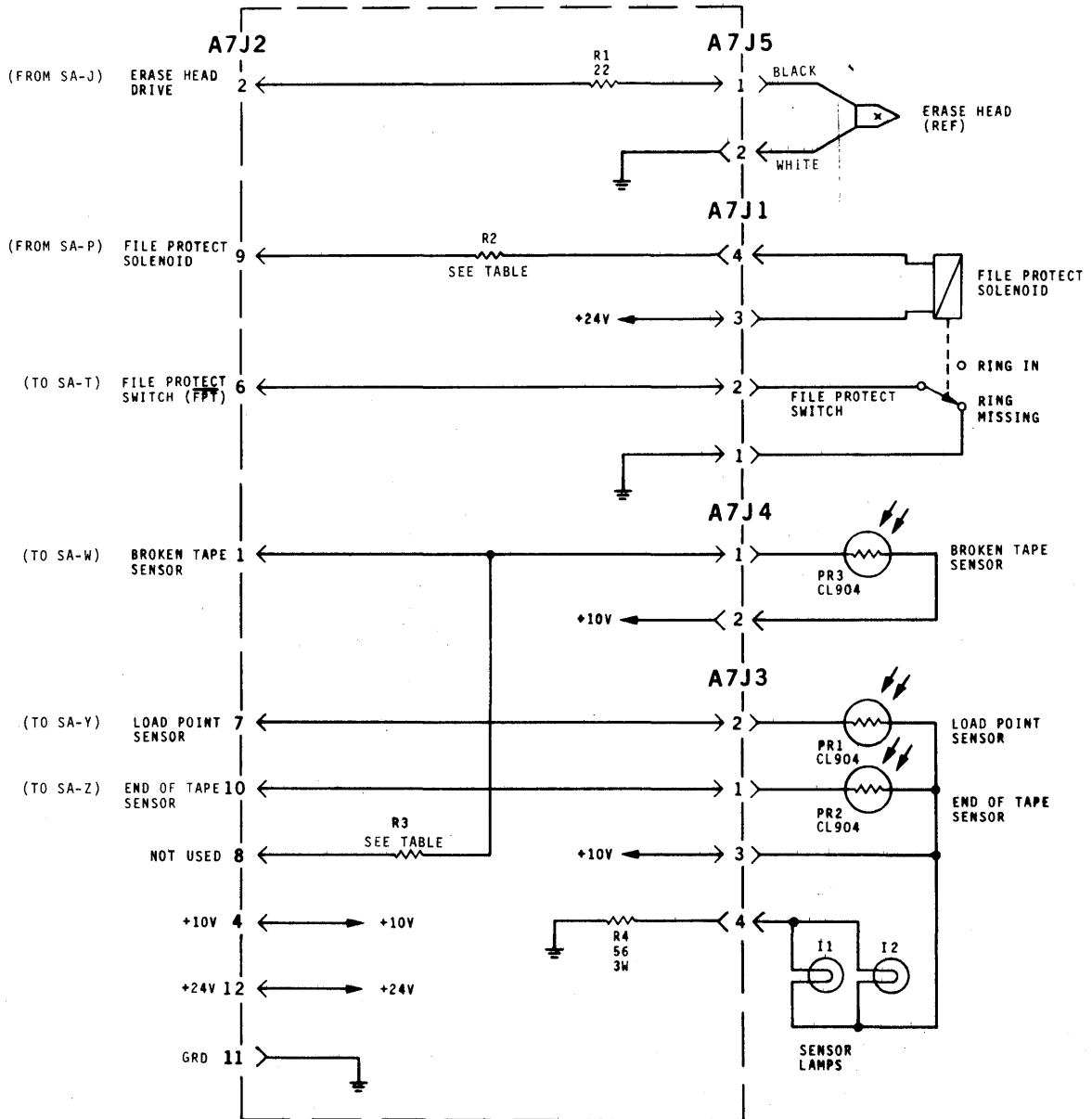


DASH NO.	C9
-001U	10
-002C	47

NOTES: UNLESS OTHERWISE SPECIFIED  
1. EQUIVALENT TRANSISTORS  
148-0094-001 EQUALS MJE4922, MJE2523, SJE5052K, TIP31A

**Sensor Amp Driver,  
Type 3844,  
Schematic Diagram**

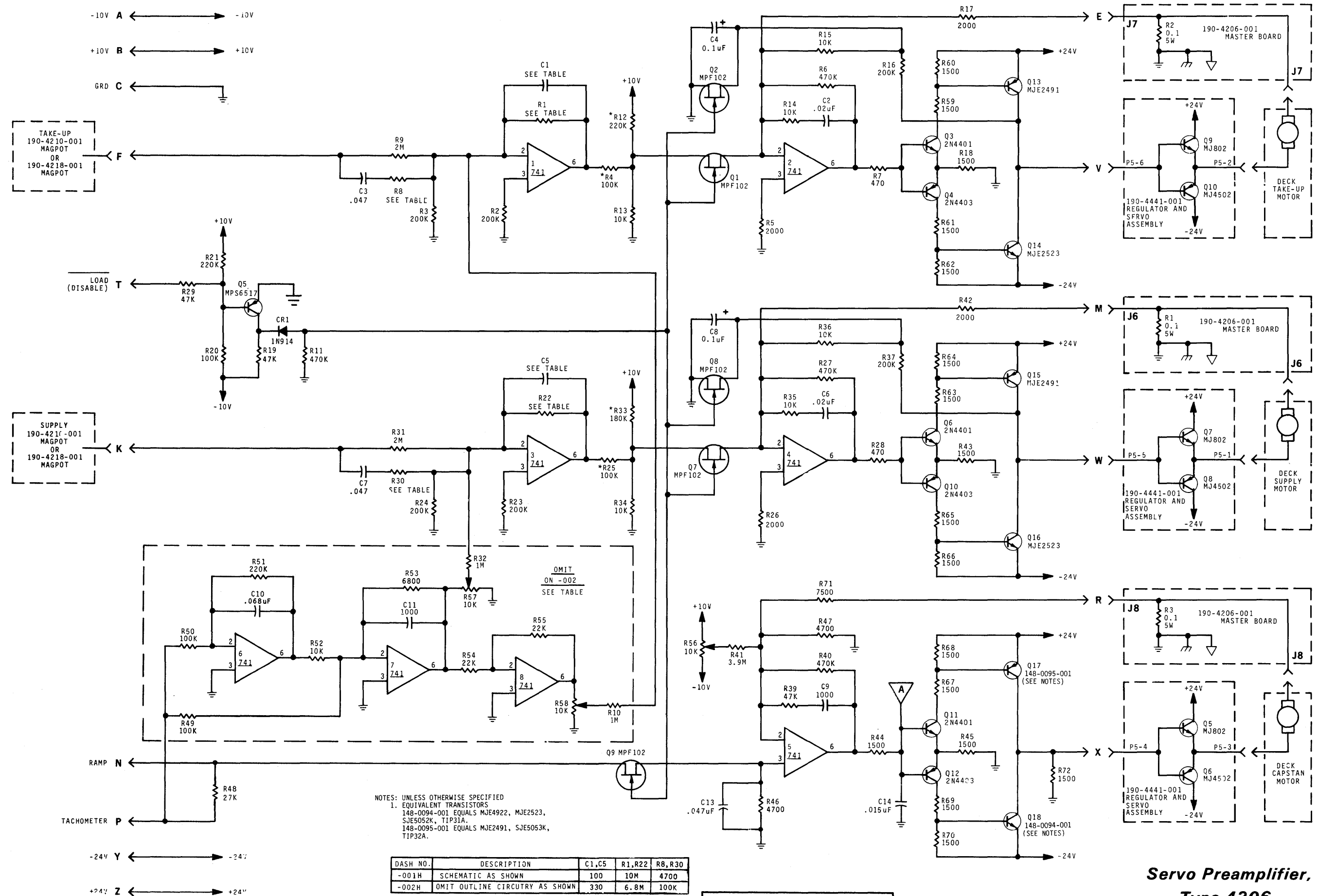




DASH NO.	R2	R3
001C	STRAP	2.2K
002B	15, 3W	2.2K
003A	STRAP	OMIT

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

**Connector Board, Type 4013  
Schematic Diagram**

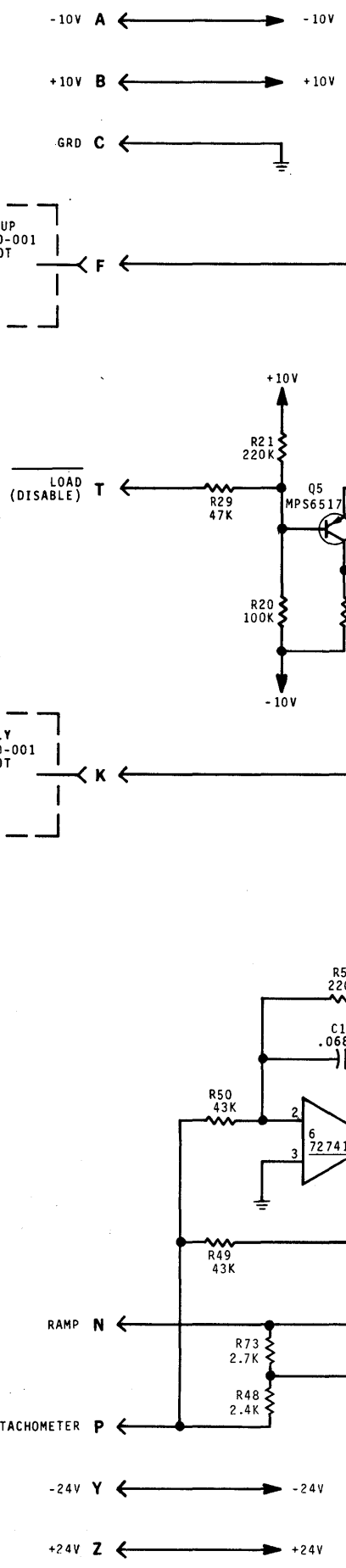
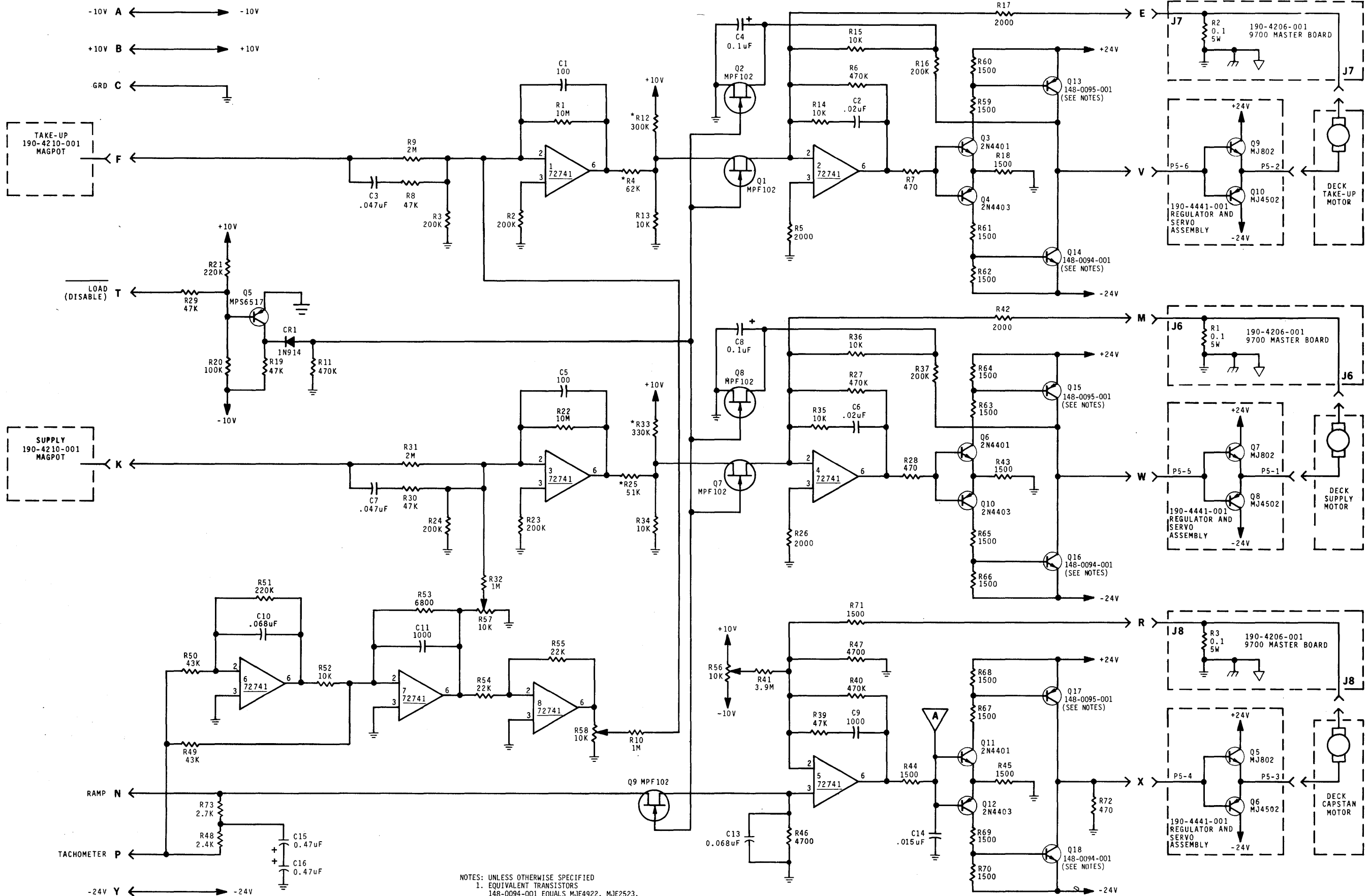


NOTES: UNLESS OTHERWISE SPECIFIED  
 1. EQUIVALENT TRANSISTORS  
 148-0094-001 EQUALS MJE4922, MJE2523,  
 SJE5052K, TIP31A,  
 148-0095-001 EQUALS MJE2491, SJE5053K,  
 TIP32A.

DASH NO.	DESCRIPTION	C1,C5	R1,R22	R8,R30
-001H	SCHEMATIC AS SHOWN	100	10M	4700
-002H	OMIT OUTLINE CIRCUITRY AS SHOWN	330	6.8M	100K

NOTE: FOR CIRCUIT CONVENTIONS USED,  
 SEE NOTES TO SCHEMATIC SECTION.

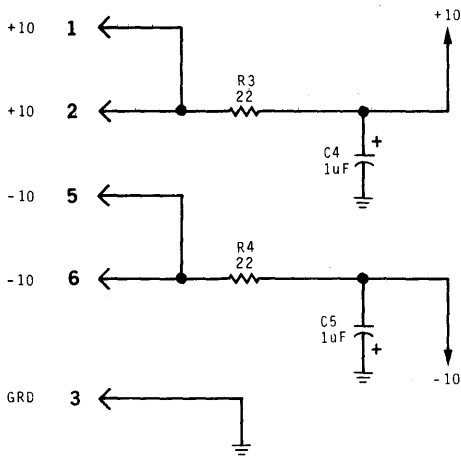
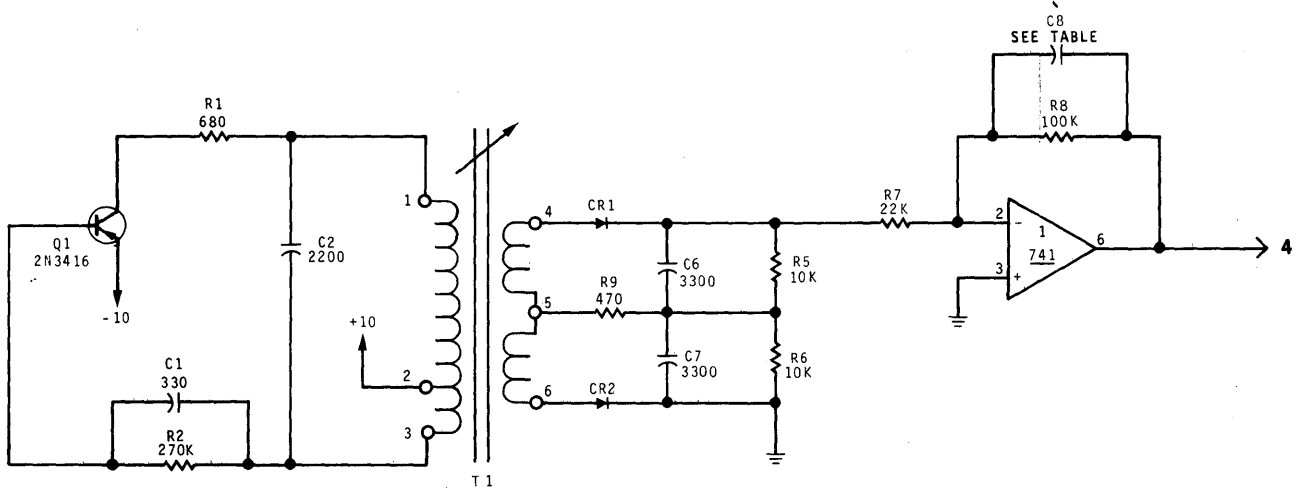
**Servo Preamplifier,  
 Type 4306,  
 Schematic Diagram**



NOTES: UNLESS OTHERWISE SPECIFIED  
 1. EQUIVALENT TRANSISTORS  
 148-0094-001 EQUALS MJE4922, MJE2523,  
 SJE5052K, TIP31A.  
 148-0095-001 EQUALS MJE2491, SJE5053K,  
 TIP32A.

NOTE: FOR CIRCUIT CONVENTIONS USED,  
 SEE NOTES TO SCHEMATIC SECTION.

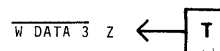
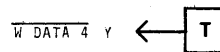
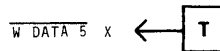
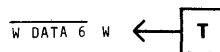
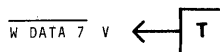
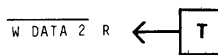
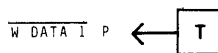
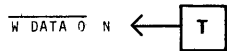
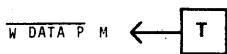
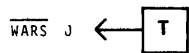
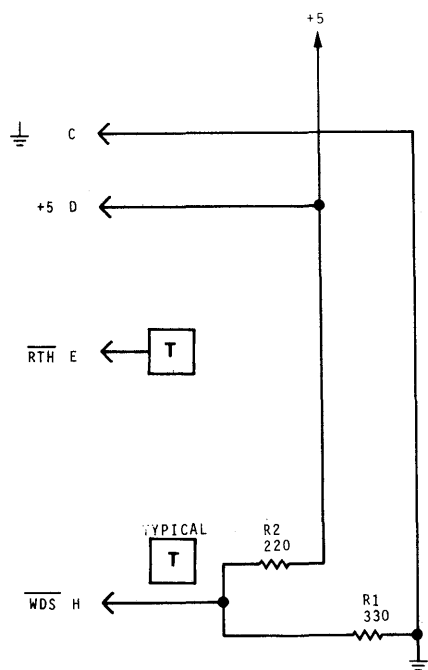
**Servo Pre-amplifier,  
 Type 4606-001C,  
 Schematic Diagram**



UNLESS OTHERWISE SPECIFIED:  
 - RESISTOR VALUES ARE IN OHMS ±5%  
 - CAPACITOR VALUES ARE IN PICOFARADS ±5%  
 - NPN TRANSISTORS ARE 2N2714  
 - PNP TRANSISTORS ARE MPS6517  
 - DIODES ARE 1N914  
 - IC ARE TTL, 7400 SERIES  
 - NUMBER IN LOGIC SYMBOL IS REFERENCE DESIGNATOR, UNDERLINED NUMBER IS IC TYPE. (IF 7400 SERIES, 74 IS OMITTED)  
 - IC PIN 7 IS CONNECTED TO GROUND  
 - IC PIN 14 IS CONNECTED TO +5V  
 - UNUSED INPUTS OF IC MAY BE TIED TOGETHER OR TO +5V THROUGH RESISTOR (+V)  
 - (\*) DENOTES FACTORY SELECTED VALUE. TYPICAL VALUE IS SHOWN  
 - FILTER CAPACITORS ARE NOT SHOWN BUT ARE IDENTIFIED BY CF ON PC BOARD

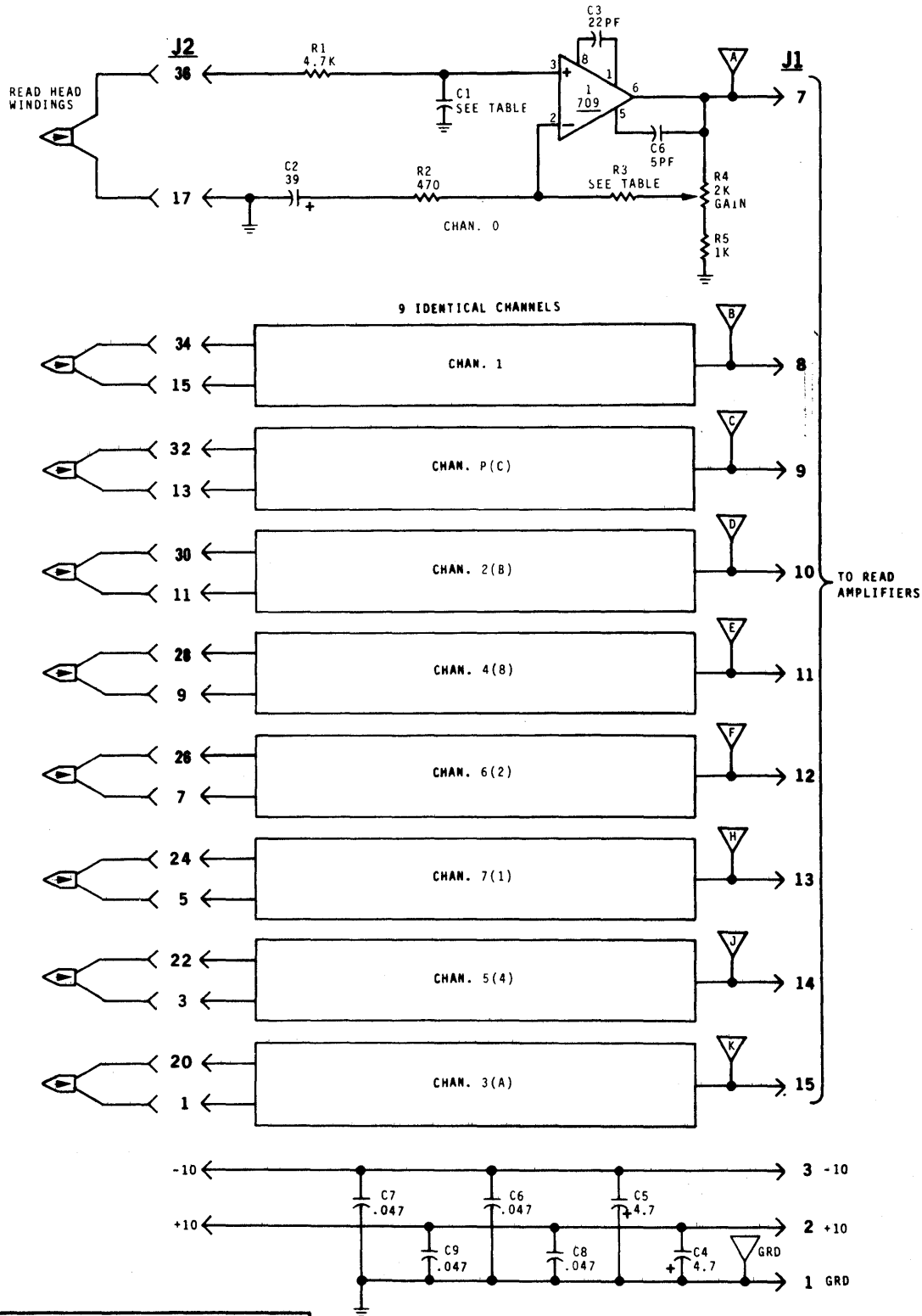
DASH NO.	MODELS	C8
-001C	ALL OTHERS	.033uF
-002A	9800/9801	.01uF

**Magpot,  
 Type 4210  
 Schematic Diagram**



NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

**Data Terminator,  
Type 3860-001B,  
Schematic Diagram**

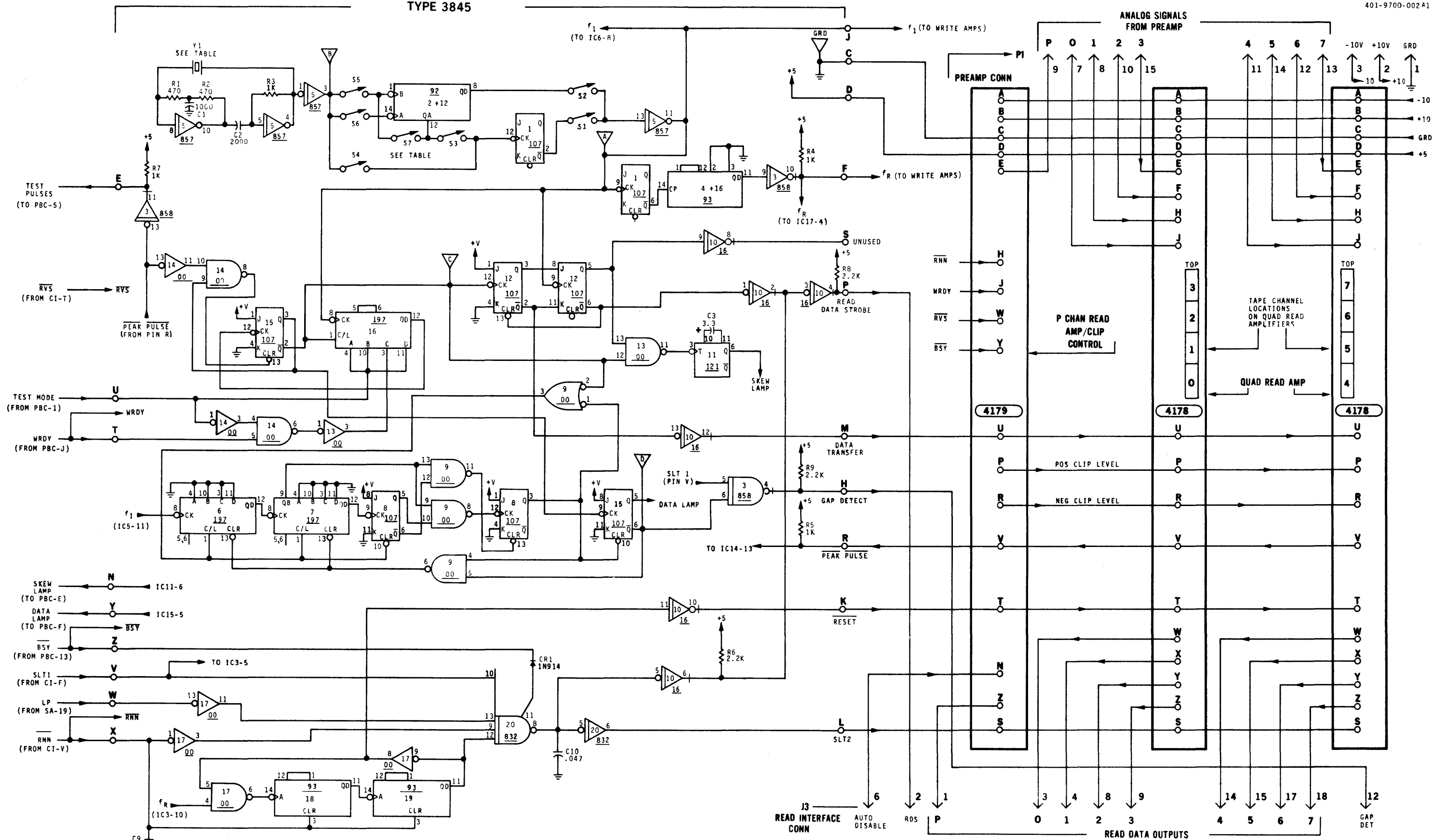


NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

DASH NO.	-001D	-002E	-004E	-005E	-006E	-003A
SPEED	9 TRACK	20-30IPS	30-40IPS	15-20IPS	10-15IPS	75IPS
	7 TRACK	15-20IPS	20-30IPS	10-15IPS		
R3	150K	110K	220K	300K	68K	82K
C1	470PF	330PF	680PF	1000PF	68PF	270PF

**Read Preamplifier,  
Type 3631,  
Schematic Diagram**

DELAY TIMING CARD  
TYPE 3845



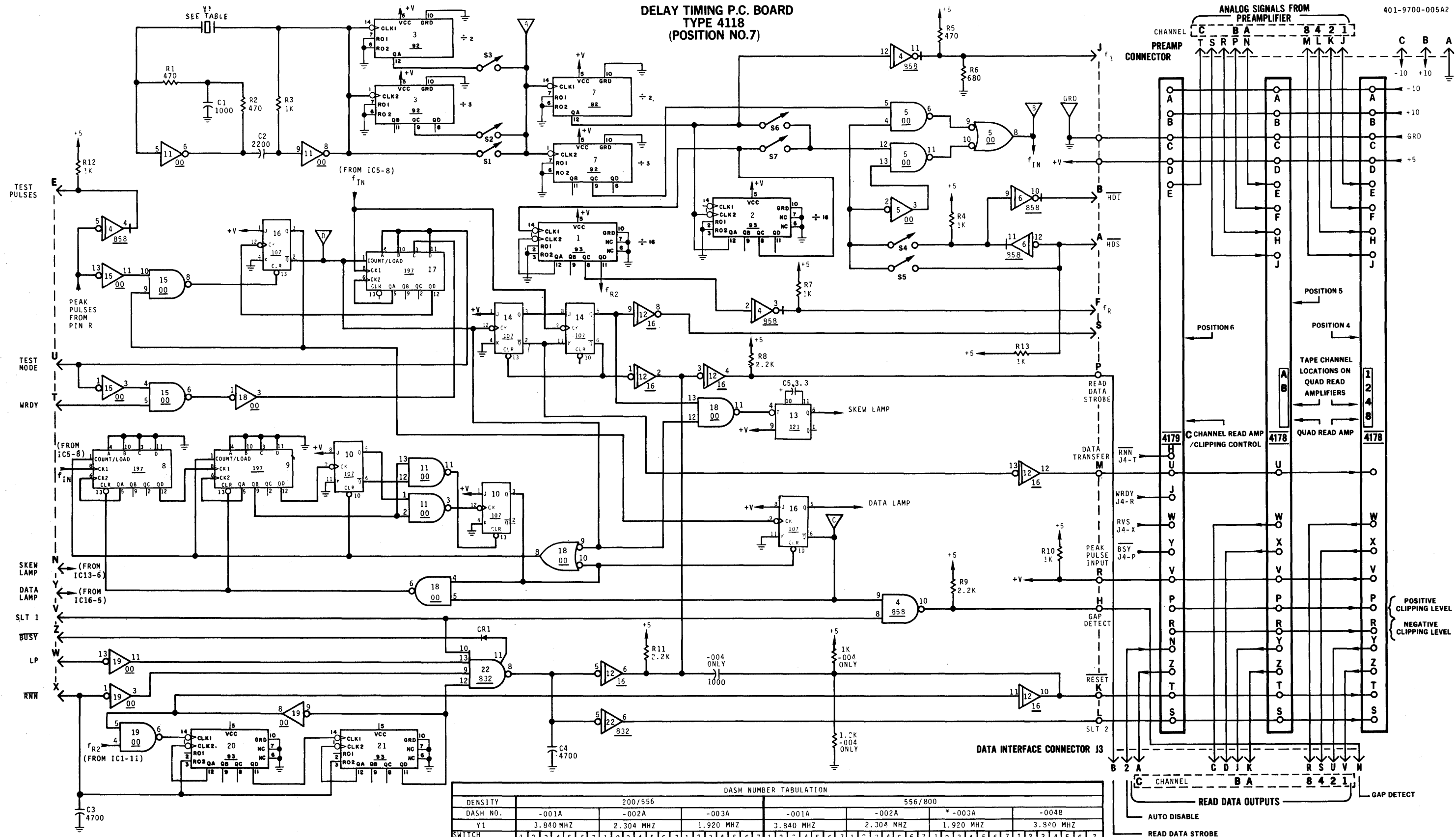
DASH NO.	-001A	-002A	-004A	-005A	SWITCH POSITION									
	1	2	3	4	5	6	7	8	9					
SPEED IPS	75.00		30.00		•	•	•	•	•	•	•	•	•	•
	37.50	45.00	15.00	18.75	•	•	•	•	•	•	•	•	•	•
	25.00		10.00		•	•	•	•	•	•	•	•	•	•
	12.50		5.00		•	•	•	•	•	•	•	•	•	•
Y1	3.84MHz	4.608MHz	1.336MHz	1.92MHz										

NOTE: FOR CIRCUIT CONVENTIONS USED,  
SEE NOTES TO SCHEMATIC SECTION.

9 Track Read Control Logic,  
Schematic Diagram

**DELAY TIMING P.C. BOARD  
TYPE 4118  
(POSITION NO.7)**

401-9700-005A2



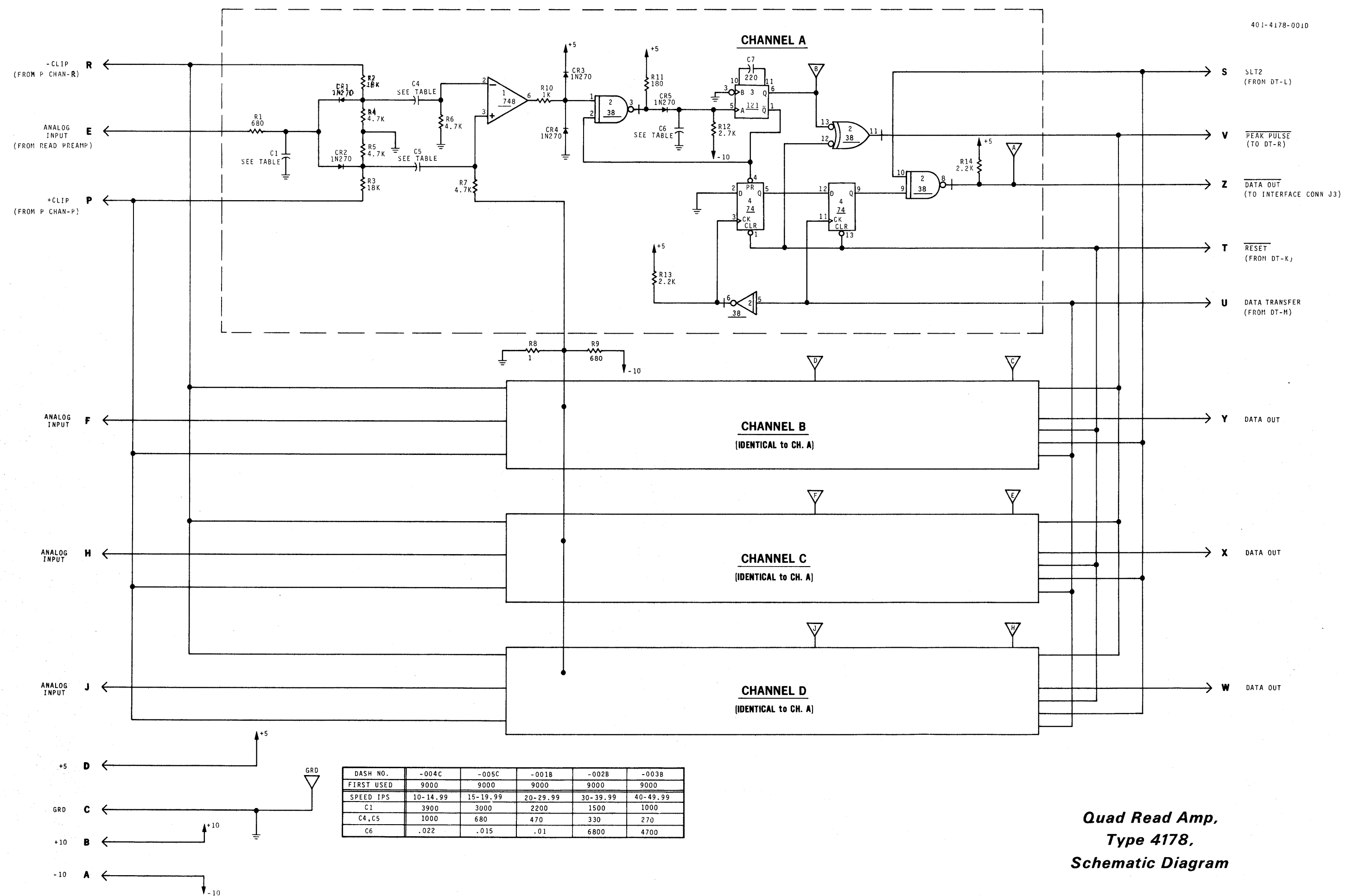
NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

		DASH NUMBER TABULATION																											
		200/556							556/800																				
DENSITY		-001A							-002A																				
DASH NO.		-001A							-002A																				
Y1		3.840 MHZ							2.304 MHZ																				
SWITCH POSITION		1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4	5	6	7
SPEED (IPS)	12.50																												
	15.00																												
	19.75																												
	25.00																												
	37.50																												
	45.00																												
75.00																													

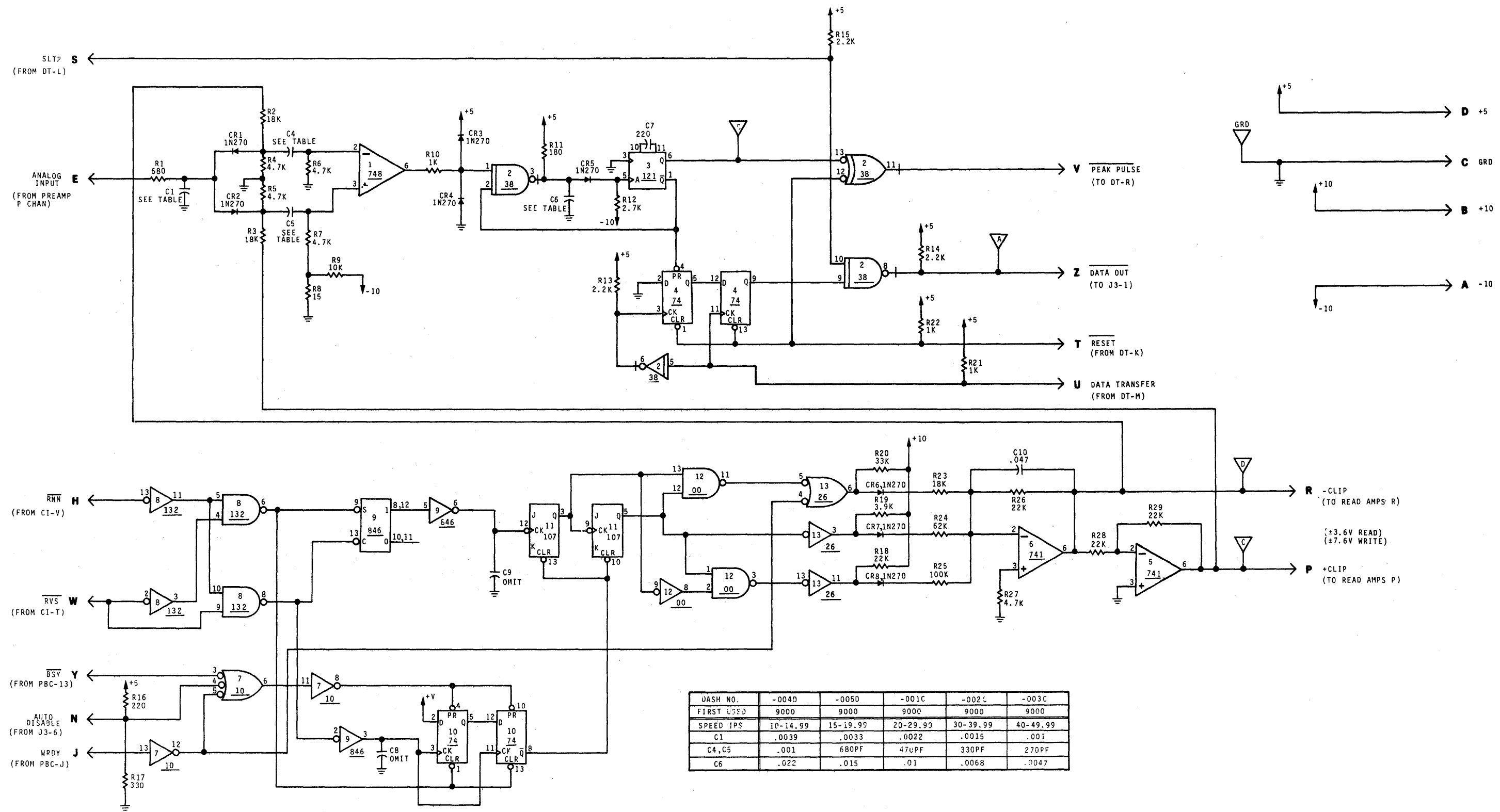
● INDICATES CLOSED POSITION OF SWITCH  
\* 2. DASH -103 TO USE SAME SWITCHING ARRANGEMENT AS -003.

**7 Track Read Control Logic,  
Schematic Diagram**

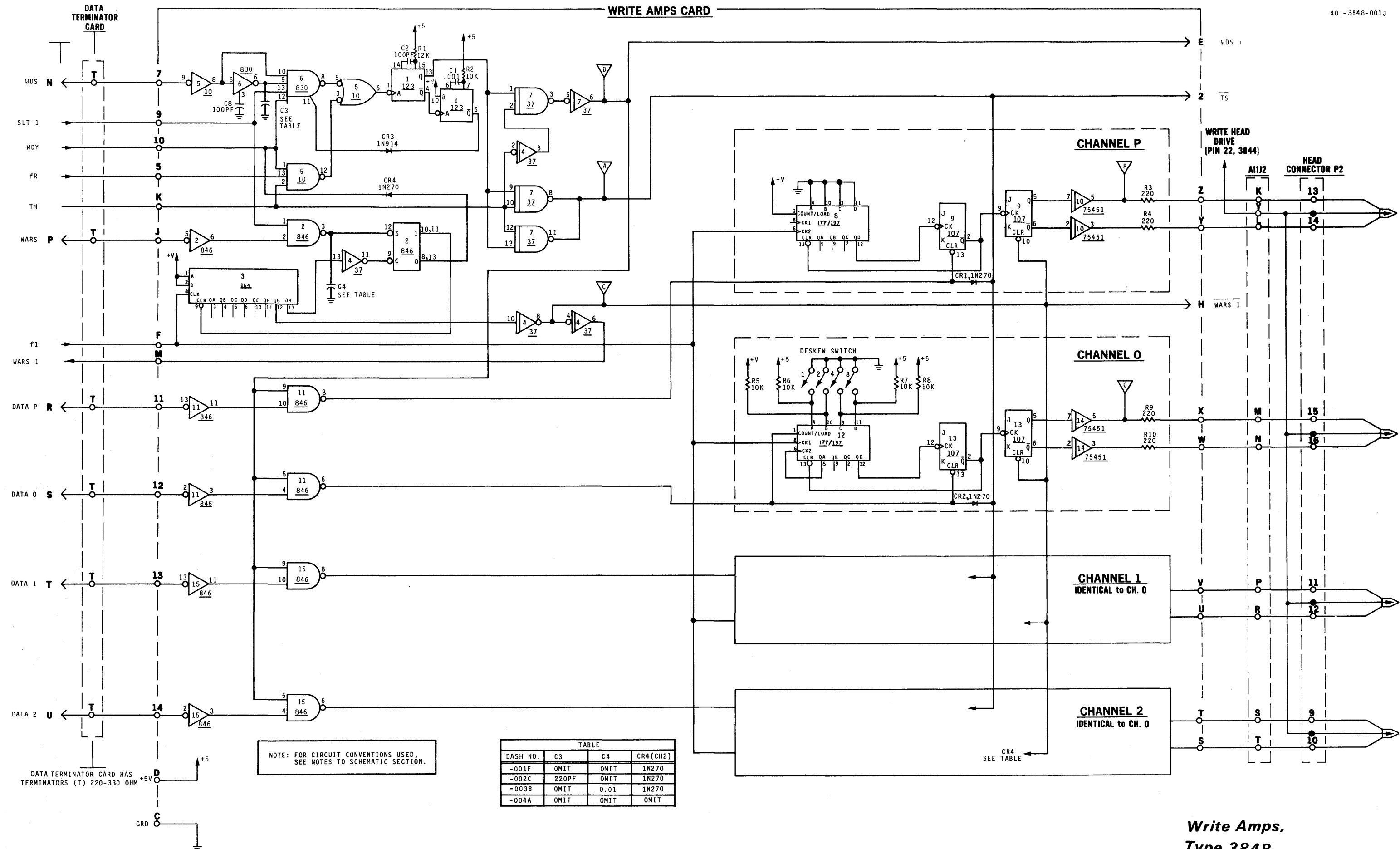




**Quad Read Amp,  
Type 4178,  
Schematic Diagram**



**Read Amp/Clipping Level Control,  
Type 4179,  
Schematic Diagram**



NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

TABLE			
DASH NO.	C3	C4	CR4 (CH2)
-001F	OMIT	OMIT	1N270
-002C	220PF	OMIT	1N270
-003B	OMIT	0.01	1N270
-004A	OMIT	OMIT	OMIT

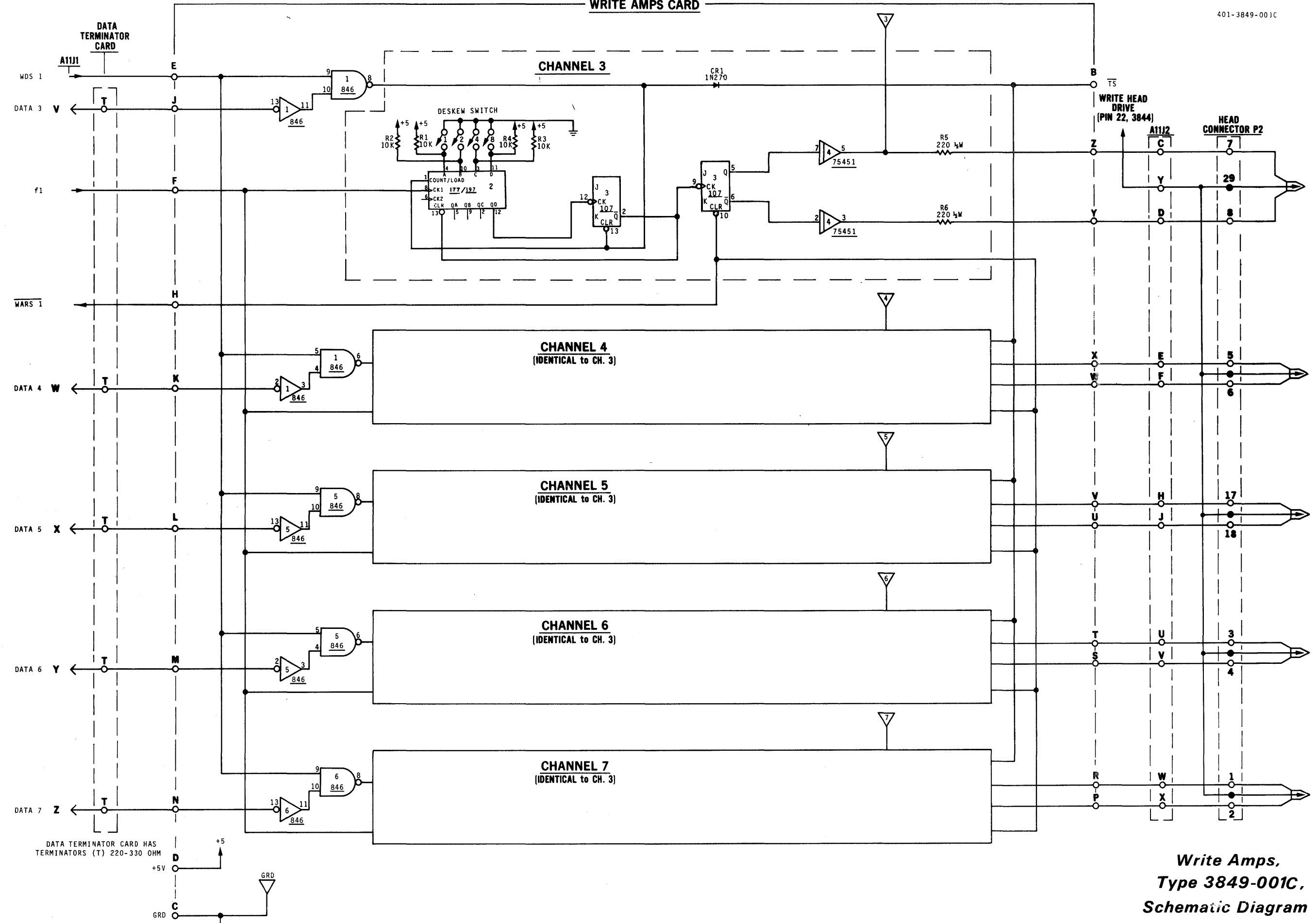
DATA TERMINATOR CARD HAS TERMINATORS (T) 220-330 OHM

CR4 SEE TABLE

**Write Amps,  
Type 3848,  
Schematic Diagram**

WRITE AMPS CARD

401-3849-001C



Write Amps, Type 3849-001C, Schematic Diagram

**SECTION VII**  
**GENERAL INFORMATION AND APPENDIX**

## DIGITAL RECORDING ON MAGNETIC TAPE USING NRZ1 CONVENTIONS AND FORMAT

### 1.1 INTRODUCTION

There are many recording techniques that may be employed to record digital information onto magnetic tape. Some of these are: non-return-to-zero (NRZ), return-to-zero, phase-encoded, Manchester coding, and NRZ1. Of these methods the NRZ1, non-return-to-zero change at logic 1, has been most widely accepted for recording parallel data onto multitrack recorders. This method has been used by IBM and other computer manufacturers for many years, and packing densities, formats, and mechanical dimensions have been fairly well standardized by usage throughout the industry.

#### 1.1.1 IBM COMPATIBLE

The term IBM compatible, or more specifically IBM compatible 2400 series, is found frequently in specifications of tape units manufactured by companies other than IBM. This means that a tape written on a machine that is IBM compatible can be successfully entered into an IBM computer utilizing the IBM 2400 series of magnetic tape units. The converse, of course, is also true. Tapes written on an IBM 2400 can be read on IBM compatible tape units equipped with the read function.

This common denominator between systems is important, for often it is the only common point between computer systems and data acquisition systems. The parameters that ensure this compatibility relate to track width, number of tracks, position of the tracks on the width of the tape, form of check characters, spacing of check characters from data, length of interblock gaps, length of file gaps, and the character used to identify a file gap, as well as the mechanical dimensions of reels and hubs. This note describes these factors for the IBM compatible NRZ1 method of recording.

#### 1.1.2 ADVANTAGES OF NRZ1 RECORDING METHOD

In the NRZ1 method of recording, current is flowing in one direction in the magnetic head at all times it is writing. This factor makes it possible to record over old data, erasing the old data as the recording is taking place. Head current also flows in a uniform direction during the interrecord gap. This is useful when it is necessary to rewrite a record or skip a

bad area of tape found on re-read and allows the head current to be turned on again in a known direction without causing unwanted spikes.

Another advantage of the NRZ1 system is that the electronics for writing and reading are simpler than those required for other recording techniques, such as phase encoding.

A disadvantage of the NRZ1 system is that it is not self-clocking and is useful only where multiple track recording is employed. A further restriction is that in order to derive a clock from the multiple tracks, at least one of the tracks must have a one in it for each byte or character recorded. This last factor is ensured when a parity check is employed and the parity is odd. If even parity is used, then of course the all-zero character must be declared invalid and not used during the block.

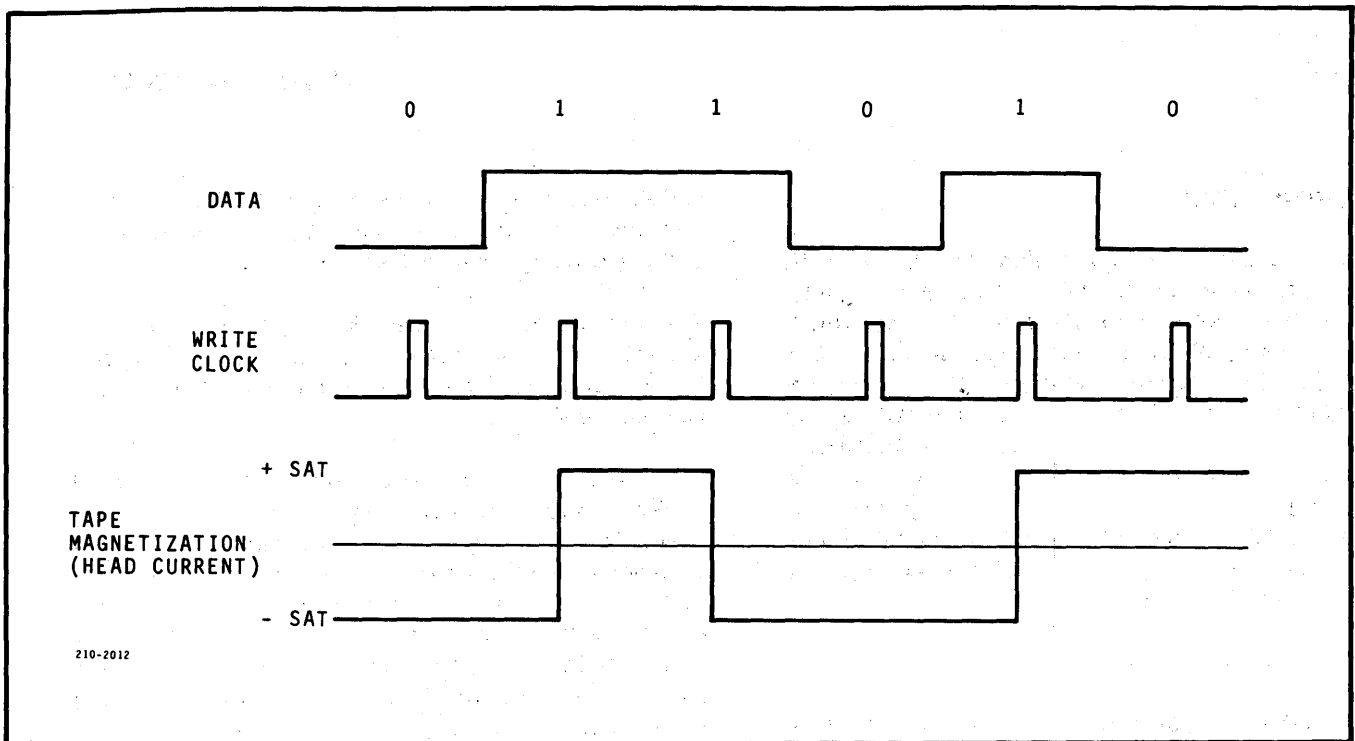
### 1.2 WRITING NRZ1 TAPES

To record digital data on magnetic tape, it is necessary to magnetize the tape discretely to indicate binary ones and zeros. In the NRZ1 method, current is flowing in the head at all times the magnetic tape unit is in the write mode. As long as the head current does not change, the data will be written such that it will be interpreted as zeros. When a transition occurs between saturation magnetism (plus and minus) on the tape, this will be interpreted as a one. Figure 1-1 shows typical waveforms for data recorded on tape in the pattern 011010. The data is entered together with write clocks as shown, with a write clock for each bit recorded. With tape in continuous motion, a flux pattern corresponding to the tape magnetization will appear on the tape as shown.

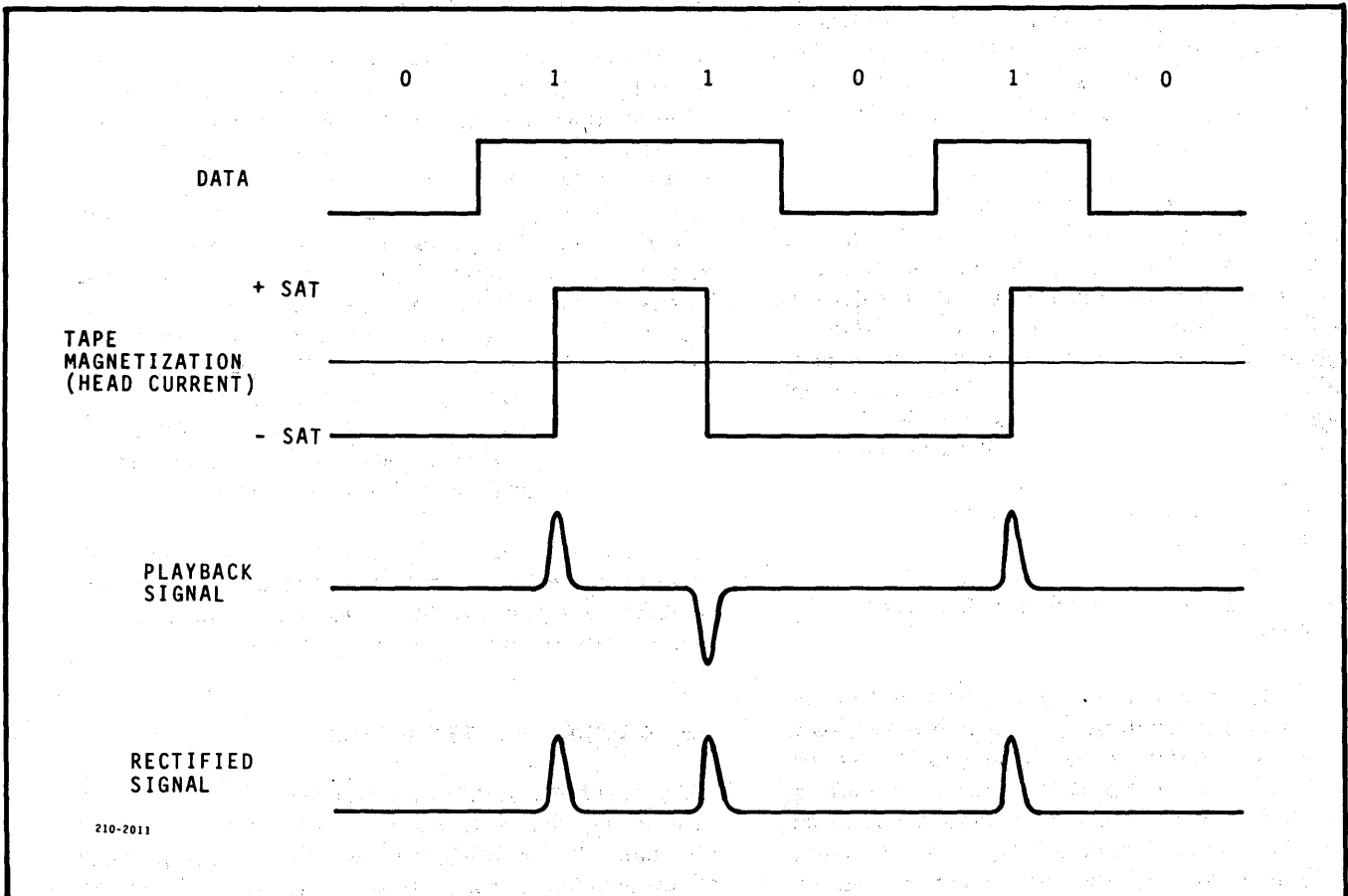
NRZ1 recording is implemented by driving current through the head winding in a direction determined by a flip-flop that toggles for each one, gated in by coincidence between data and a write clock.

### 1.3 READING NRZ1 RECORDINGS

To recover the data written in NRZ1 format, the tape is moved at a constant velocity past the gap in the head. Refer to Figure 1-2. If the same pattern shown above is present on the tape, the head voltage



**Figure 1-1 NRZ1 Waveforms - Writing**



**Figure 1-2. NRZ1 Waveforms - Reading**

will look like the playback signal since the voltage induced in the head is the differential of the flux pattern on the tape. The characteristic half sine wave results from the fact that the gap on the head has a finite width.

The pattern shown is typical of what would be seen with 200 bits per inch (bpi) recording. As the recording density increases, the mechanical dimensions of the head remain the same, resulting in the same waveform but with the individual waves crowded close together. This ultimately presents a limit beyond which this type of recording is useful with state-of-the-art tapes and magnetic heads. Recording of 800bpi seems to be a practical limit and is the maximum density utilized in present-day systems.

The playback signal is then rectified and, as can be seen from the figures, a pulse is present for every one recorded and the base line remains stationary for all zeros recorded. Note, however, that it is not practical to derive an accurate clock from the signal on the basis of a single-track recording. However, since this is a multiple track system and employs a parity generator, a data bit will be found on one of the multiple tracks for each character written, assuming that an all-zeros character is not employed in conjunction with even parity.

Considering the above factors, a typical read amplifier consists of an analog amplifier, a rectifier, a peak detector, suitable logic to create a clock, and an output buffer stage to enable interfacing to the customer's unit.

### 1.3.1 SKEW AND GAP SCATTER

Another major factor that limits the design of an NRZ1 multiple track system is that heads are not perfect because of gap scatter and head mounting to decks is not perfect causing skew. Both these factors have the same effect in that the signals from all the tracks do not occur perfectly in unison. The problem is minimal if the same head and deck are used for reading and writing a given tape, but since interchangeability of tapes between machines is mandatory provisions must be made to cancel out these effects. The allowable tolerances in head manufacture have practical limits and are typically in the  $\pm 50$  microinch region for high quality heads. Fixed heads without adjustment are practical with 200 bpi and 556 bpi recording, but 800 bpi recording requires adjustments.

All Kennedy recorders are equipped with the necessary deskewing adjustment to enable operation and

assure compatibility with other magnetic tape units. These adjustments take the following form.

#### 1.3.1.1 Read Head Alignment

The read head is adjusted so that its gaps are perpendicular to the direction of tape motion using an IBM skewmaster tape. A mechanical adjustment is provided consisting of a spring loaded mounting plate working against a fine pitch adjusting screw. (On incremental and some low density machines this adjustment is either not required or is made by shimming tape guides.)

#### 1.3.1.2 Read Electronic Deskew Register

All Kennedy read amplifiers are provided with a deskewing register. This register allows a total skew of 50 percent for all reasons including write head gap scatter, dynamic read skew, read head misalignment, and speed variation in writing or reading.

#### 1.3.1.3 Write Electronic Deskewing (continuous tape units only)

The mechanical relationship between the read gap and the write gap is fixed in any given read after write head. Since the read head is adjusted perpendicular to tape motion (paragraph 1.3.1.1), the write time for each channel may be delayed selectively so that a character is written on the tape perpendicular to tape motion. In Kennedy continuous tape units a fixed delay is inserted for one channel and individual delays are provided for the remaining channels. This arrangement allows each channel to be adjusted in exact relationship to the fixed channel and allows adjustment for skew and gap scatter as well.

## 1.4 TAPE FORMATS

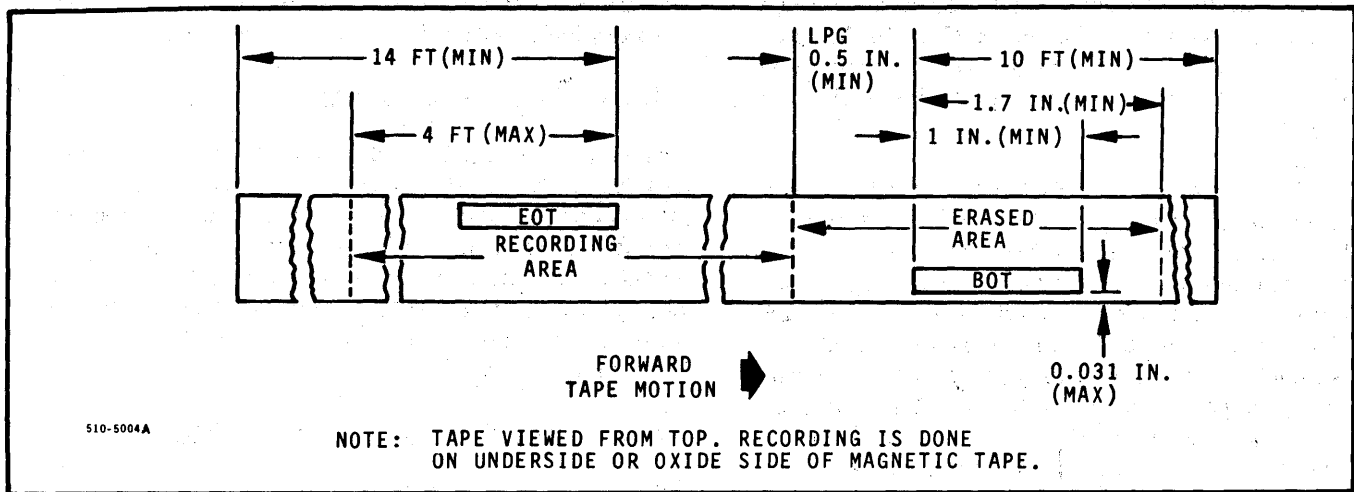
There are other factors that affect compatibility in addition to density and recording method:

- a. Tape markers
- b. Gaps
- c. Check characters
- d. Codes

### 1.4.1 TAPE MARKERS

When recording on magnetic tape, care must be taken to avoid physical handling and damage to the recorded surface. A portion of tape — at least 10 feet — at each end is reserved for threading and loading and is not used for storing data. To define the recorded area, pressure sensitive reflective markers are applied to the nonoxide side of the tape as shown in Figure 1-3.





**Figure 1-3. Tape Markers**

These markers are sensed optically and define the recorded area in a standardized manner.

The BOT marker signal is used internally to define the load point or starting of recording. The EOT marker signal is not used internally but is available to the interface as an end of tape warning signal and should be used by the unit interfaced to the magnetic units to terminate recording within the next 4 feet of tape.

#### 1.4.2 GAPS

Tape reading can only take place reliably when tape is moving at a known speed across the head. To allow tape to start and stop while the computer manipulates data, a section of tape with no data is provided between records or blocks of data and at the beginning and end of tape. This section is recorded with the head current turned on in the direction defined as erased and results in a constant flux in a predetermined direction which is independent of tape speed or motion. The direction of current in the heads defining the erased condition is also controlled to be uniform in all recorders. On readback this flux is constant as the tape accelerates and decelerates. Since a change in flux is required for the read head to sense data, no signal occurs and orderly starts and stops may be made.

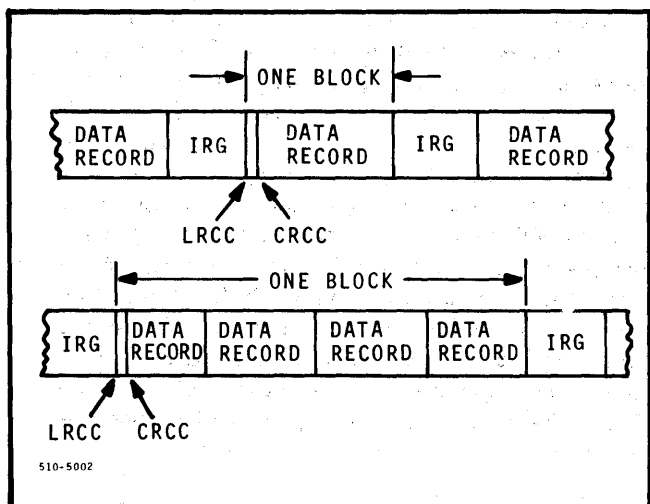
Mechanical limitations preclude instantaneous starts and stops, and a distance of tape must be reserved, conditioned by the requirements of the "worst case" machines, to use the standards. While high speed units (IBM 2400 series) set the length of the gaps, Kennedy recorders utilize the full gap length to advantage by providing controlled acceleration and deceleration, resulting in minimum stresses to the tape.

##### 1.4.2.1 Beginning of Tape Gap

An erased section of tape is required surrounding the BOT marker. This serves as a defined area within which data recording or reading can start. To comply with IBM specifications this section extends a minimum of 1.7 inches ahead of the trailing edge of the BOT marker and extends a minimum of 0.5 inch past the trailing edge of the BOT marker. In nearly all systems (including IBM) this erased section totals about 3.5 inches (Figure 1-3).

##### 1.4.2.2 Interrecord Gaps

Interrecord gaps are areas, without data, placed between data blocks or records as shown in Figure 1-4. The length of the gap is 0.75 inch minimum for seven-track systems and 0.60 inch minimum for nine-track



**Figure 1-4. Interrecord Gaps**

systems. The maximum length is not critical. The USA Standard Institute specifies the maximum length at 25 feet.

If records are short it can be seen that a large portion of the tape is used for interrecord gaps. In many cases computers are programmed to handle records in batches as shown in Figure 1-4. In this case the IRG and check characters are inserted on a block basis.

Figure 1-5 shows the format of the file mark for seven- and nine-track tapes. The distinguishing feature of the block is the fact that it is a single specific character record with a check character. The erased gap itself is nearly always used but IBM standards state that it is optional.

#### 1.4.3 CHECK CHARACTERS

The NRZ1 format provides for both vertical and horizontal parity checks. In the nine-track system an additional check called the cyclic redundancy check character is used. Refer to Figures 1-6 and 1-7 for the location of the check characters.

The check characters define to a very high level of confidence that a block that is read is accurate.

#### 1.4.3.1 Vertical Parity

Seven-track and nine-track systems use six and eight tracks respectively for recording data. The remaining track is redundant and carries the parity information. When the data is written on tape, a parity generator senses the input data and determines if the number of bits in the byte is odd or even. It outputs a "1" or a "0" to the redundant track to make the count odd if odd parity is selected, or even if even parity is selected.

On readback a similar circuit can be used to count the number of bits in each byte and determine if the count is odd or even. Depending on which is defined as correct, it signals the error line if the count is wrong. Thus each byte is checked. However, if an even number of bits is dropped the test will not result in an error signal, so an additional check called longitudinal parity is employed.

Odd or even parity may be selected on seven-track recorders. Nine-track recorders are always odd parity.

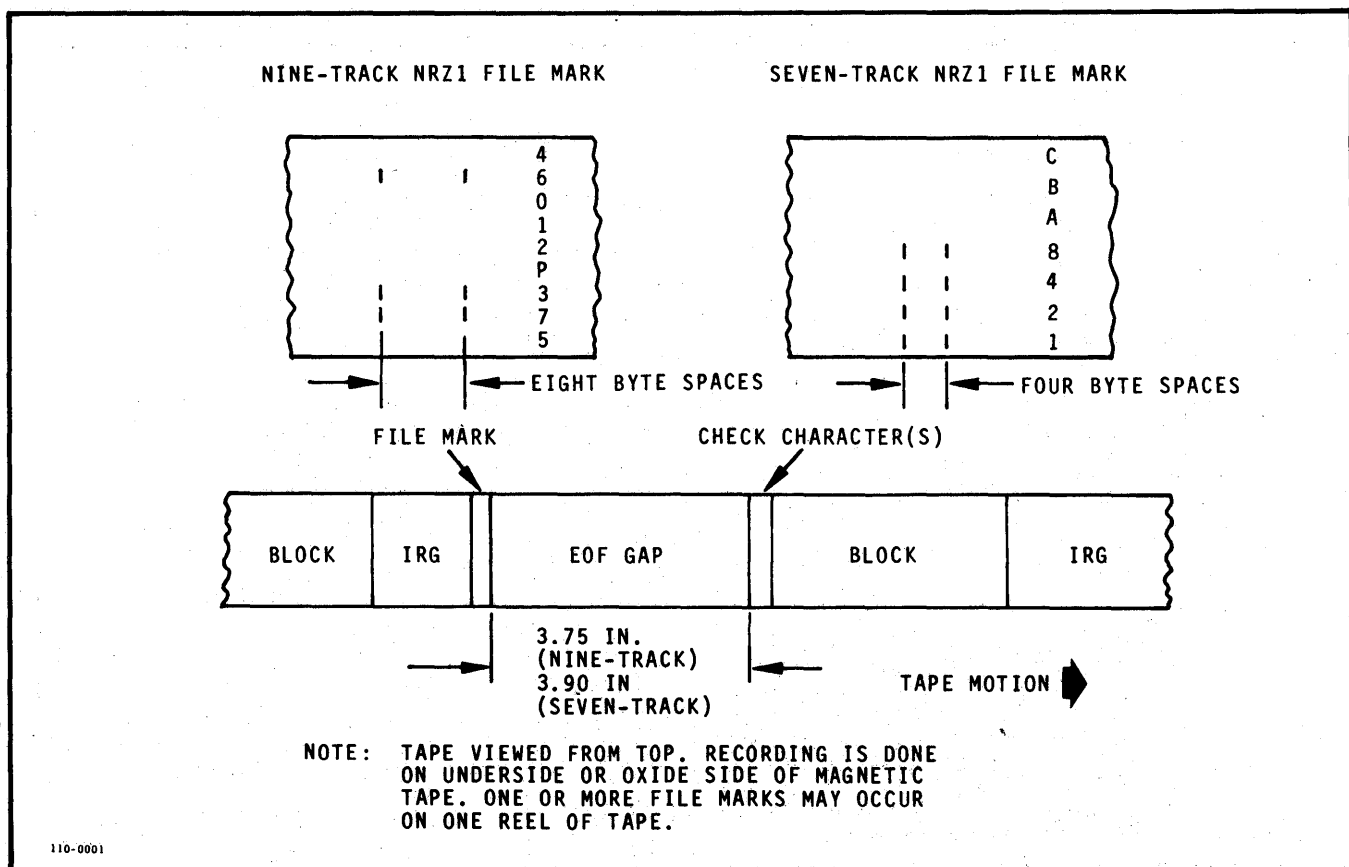
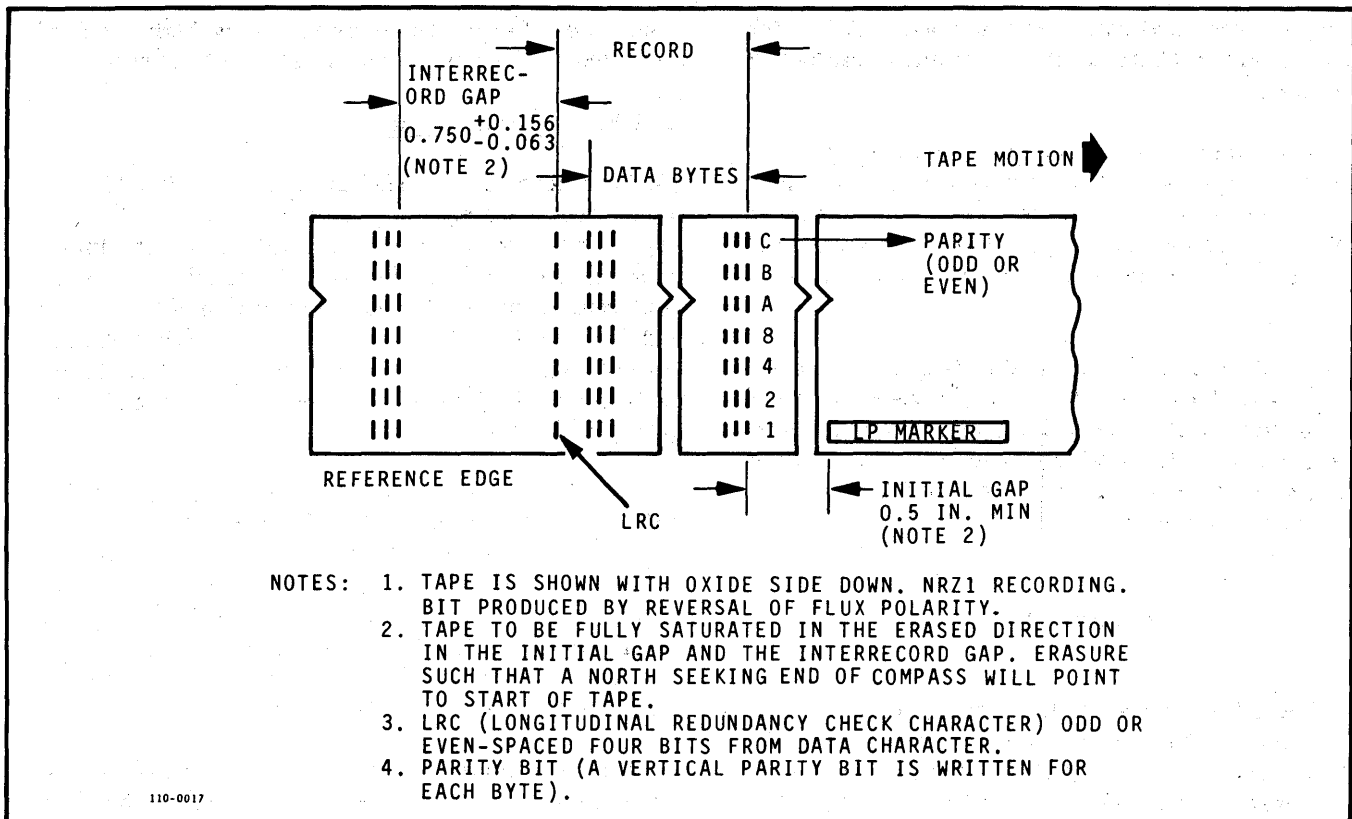
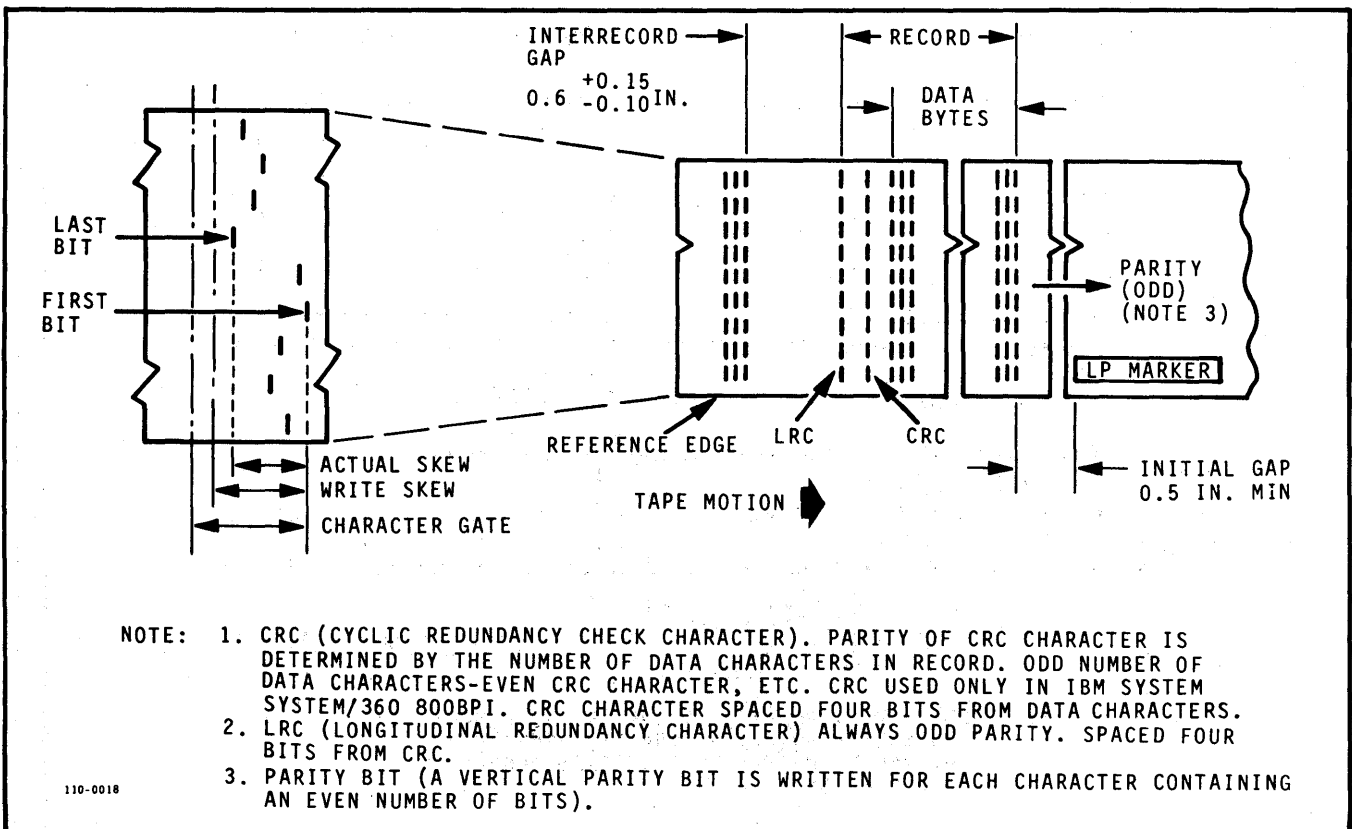


Figure 1-5. NRZ1 File Marks



**Figure 1-6. Data Format - Seven Track**



**Figure 1-7. Data Format - Nine Track**

### 1.4.3.2 Longitudinal Parity

A longitudinal redundancy check character is written at the end of each block. It is separated from the end of each block as shown in Figure 1-8. This character is made up on a per-track basis. The number of 1's recorded in a given track of a block is counted and a "1" is written in the track as the LRCC if the count was odd, and, therefore, the number of 1's recorded in each track becomes even for any given block. On readback this is checked and an error is detected if the count is odd in any track. The possibility of not detecting an erroneous block still exists if an even number of bits in a given track of a block is dropped. However, when this test is combined with the vertical parity test the probability of not detecting an error is reduced.

### 1.4.3.3 Cyclic Redundancy Check Character (CRCC)

In the nine-track system another check character must be written. This character is derived with relatively complex logic, the result of which, in combination with the LRCC and vertical parity information, enables a computer to determine in which track a dropout occurred. If the dropout occurred in only one track in the given block, the computer can then nullify that track and generate the information in that track from the data in the remaining tracks, which includes the parity track.

This check character follows the last data byte by four cell positions, as shown in Figure 1-8.

### 1.4.3.4 Codes

The recorder will accept and read back any code set applied (six-bit for seven-track, eight-bit for nine-track). The only restriction is that the 000000 character in a seven-track system using even parity must not be used. This is a blank position or missing character, and most IBM systems will register an error condition if it is found in a block.

Two code sets are shown in Figure 1-9. These are the graphic symbols portion of the codes used by IBM for nine-track and seven-track systems. They are shown for reference only. Systems may use different code structures when they are programmed for them.

In the seven-track system the 000000 character may be converted to the 001010 character by use of the

"BCD 0 to 10" option which is available for most Kennedy recorders. This senses the 000000 character on the data lines in conjunction with a write clock and converts it internally to record the IBM character for the number 0 (001010).

### 1.4.4 SUMMARY OF FORMAT

A summary of the above factors is shown in Figure 1-6 for seven-track data format and Figure 1-7 for nine-track data format. Record blocks and tape markers are shown in Figure 1-10.

### 1.4.5 REFERENCES

Additional information may be found in the following publications:

- a. IBM 2400-Series Magnetic Tape Units Original Equipment Manufacturers' Information, IBM Form 226862-4
- b. USA Standard Recorded Magnetic Tape for Information Interchange (800 cpi, NRZ1), United States of America Standards Institute, 10 East 40th Street, New York 10016

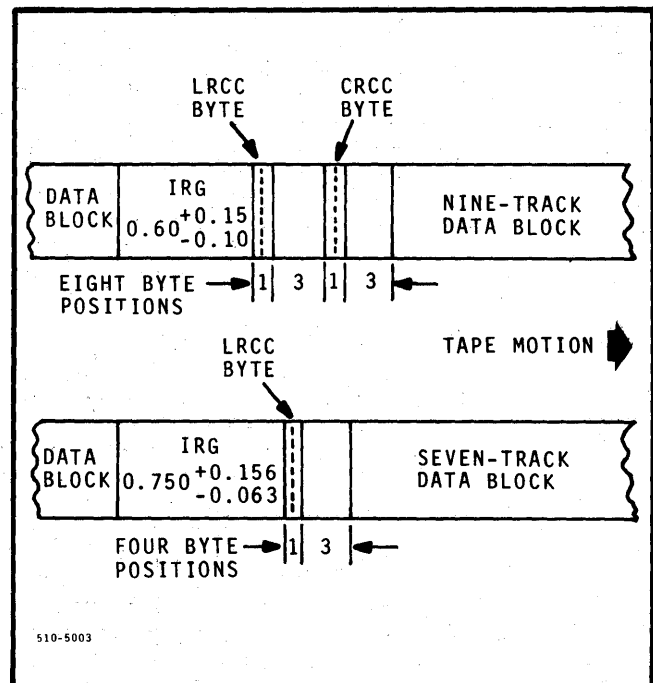
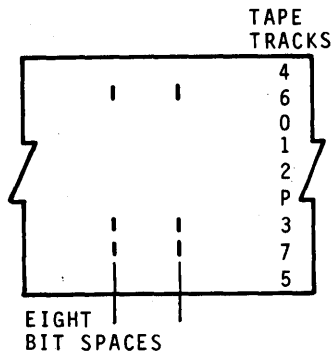


Figure 1-8. Check Characters

COLLATING SEQUENCE	GRAPHICS		EXTENDED BINARY CODED DECIMAL INTERCHANGE CODE (EBCDIC)							BINARY CODED DECIMAL INTERCHANGE CODE (BCD)						
	8 Bit	BCD	0	1	2	3	4	5	6	7	B	A	8	4	2	1
00	blank	blank	0	1	0	0	0	0	0	0	0	0	0	0	0	0
01	.	.	0	1	0	0	1	0	1	1	1	1	0	1	1	1
02	←	⌘	0	1	0	0	1	1	0	0	1	1	1	1	0	0
03	(	(	0	1	0	0	1	1	0	1	1	1	1	0	1	1
04	+	<	0	1	0	0	1	1	1	0	1	1	1	1	1	0
05	GM	GM	0	1	0	0	1	1	1	1	1	1	1	1	1	1
06	&	&+	0	1	0	1	0	0	0	0	1	1	0	0	0	0
07	\$	\$	0	1	0	1	1	0	1	1	1	0	1	0	1	1
08	*	*	0	1	0	1	1	1	0	0	1	0	1	1	0	0
09	)	)	0	1	0	1	1	1	0	1	1	0	1	1	0	1
10	;	;	0	1	0	1	1	1	1	0	1	0	1	1	1	0
11	MC	MC	0	1	0	1	1	1	1	1	1	0	1	1	1	1
12	-	-	0	1	1	0	0	0	0	0	1	0	0	0	0	0
13	/	/	0	1	1	0	0	0	0	1	0	1	0	0	0	1
14	,	,	0	1	1	0	1	0	1	1	0	1	1	0	1	1
15	%	% (	0	1	1	0	1	1	0	0	0	1	1	1	0	0
16	WS	WS	0	1	1	0	1	1	0	1	0	1	1	1	0	1
17	↑	\	0	1	1	0	1	1	1	0	0	1	1	1	1	0
18	SM	SM	0	1	1	0	1	1	1	1	0	1	1	1	1	1
19	⌘	⌘	0	1	1	1	1	0	1	0	0	1	0	0	0	0
20	#	#=	0	1	1	1	1	0	1	1	0	0	1	0	1	1
21	@	@'	0	1	1	1	1	1	0	0	0	0	1	1	0	0
22	▽	:	0	1	1	1	1	1	0	1	0	0	1	1	0	1
23	=	>	0	1	1	1	1	1	1	0	0	0	1	1	1	0
24	TM	TM	0	1	1	1	1	1	1	1	0	0	1	1	1	1
25	ø	ø	1	1	0	0	0	0	0	0	1	1	1	0	1	0
26	A	A	1	1	0	0	0	0	0	1	1	1	0	0	0	1
27	B	B	1	1	0	0	0	0	1	0	1	1	0	0	1	0
28	C	C	1	1	0	0	0	0	1	1	1	1	0	0	1	1
29	D	D	1	1	0	0	0	1	0	0	1	1	0	1	0	0
30	E	E	1	1	0	0	0	1	0	1	1	1	0	1	0	1
31	F	F	1	1	0	0	0	1	1	0	1	1	0	1	1	0
32	G	G	1	1	0	0	0	1	1	1	1	1	0	1	1	1
33	H	H	1	1	0	0	1	0	0	0	1	1	1	0	0	0
34	I	I	1	1	0	0	1	0	0	1	1	1	1	0	0	1
35	ø	ø	1	1	0	1	0	0	0	0	1	0	1	0	1	0
36	J	J	1	1	0	1	0	0	0	1	1	0	0	0	0	1
37	K	K	1	1	0	1	0	0	1	0	1	0	0	0	1	0
38	L	L	1	1	0	1	0	0	1	1	1	0	0	0	1	1
39	M	M	1	1	0	1	0	1	0	0	1	0	0	1	0	0
40	N	N	1	1	0	1	0	1	0	1	1	0	0	1	0	1
41	O	O	1	1	0	1	0	1	1	0	1	0	0	1	1	0
42	P	P	1	1	0	1	0	1	1	1	1	0	0	1	1	1
43	Q	Q	1	1	0	1	1	0	0	0	1	0	1	0	0	0
44	R	R	1	1	0	1	1	0	0	1	1	0	1	0	0	1
45	RM	RM	1	1	1	0	0	0	0	0	0	1	1	0	1	0
46	S	S	1	1	1	0	0	0	1	0	0	1	0	0	1	0
47	T	T	1	1	1	0	0	0	1	1	0	1	0	0	1	1
48	U	U	1	1	1	0	0	1	0	0	0	1	0	1	0	0
49	V	V	1	1	1	0	0	1	0	1	0	1	0	1	0	1
50	W	W	1	1	1	0	0	1	1	0	0	1	0	1	1	0
51	X	X	1	1	1	0	0	1	1	1	0	1	0	1	1	1
52	Y	Y	1	1	1	0	1	0	0	0	0	1	1	0	0	0
53	Z	Z	1	1	1	0	1	0	0	1	0	1	1	0	0	1
54	0	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
55	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	1
56	2	2	1	1	1	1	0	0	1	0	0	0	0	0	1	0
57	3	3	1	1	1	1	0	0	1	1	0	0	0	0	1	1
58	4	4	1	1	1	1	0	1	0	0	0	0	0	1	0	0
59	5	5	1	1	1	1	0	1	0	1	0	0	0	1	0	1
60	6	6	1	1	1	1	0	1	1	0	0	0	0	1	1	0
61	7	7	1	1	1	1	0	1	1	1	0	0	0	1	1	1
62	8	8	1	1	1	1	1	0	0	0	0	0	1	0	0	0
63	9	9	1	1	1	1	1	0	0	1	0	0	1	0	0	1

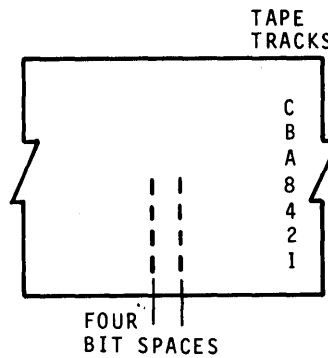
Figure 1-9. Typical IBM Codes

**NINE-TRACK NRZ1 TAPE MARK**

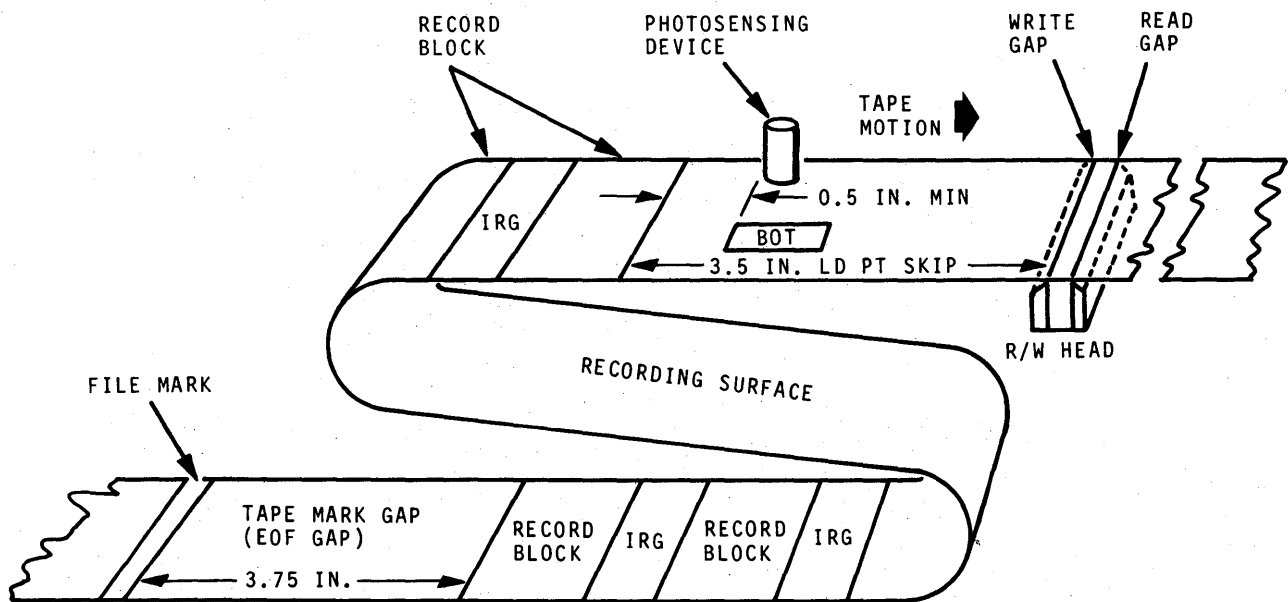


A NINE-TRACK NRZ1 TAPE MARK IS A SPECIAL CONTROL BLOCK THAT CONSISTS OF A CHARACTER WITH 1-BITS IN DATA TRACKS 3, 6, AND 7, AND AN IDENTICAL LRC CHARACTER EIGHT BIT SPACES FROM IT. NO CRC CHARACTER IS WRITTEN. ALTHOUGH THE TAPE MARK IS PRECEDED BY APPROXIMATELY 3.75 INCHES OF ERASED TAPE, THIS GAP IS NOT A REQUIREMENT.

**SEVEN-TRACK NRZ1 TAPE MARK**



A SEVEN-TRACK NRZ1 TAPE MARK IS A SPECIAL CONTROL BLOCK THAT CONSISTS OF A CHARACTER WITH 1-BITS IN A DATA TRACKS 8, 4, 2, AND 1, AND AN IDENTICAL LRC CHARACTER FOUR BIT SPACES FROM IT. ALTHOUGH THE TAPE MARK IS PRECEDED BY APPROXIMATELY 3.90 INCHES OF ERASED TAPE, THIS GAP IS NOT A REQUIREMENT.



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**Figure 1-10. Record Blocks and Tape Marks**

## PHASE ENCODED RECORDING

### Introduction

For many years, NRZ1 recording has been used in most computer tape systems. Density has increased from 200 cpi to 556 cpi and 800 cpi in the quest to increase data storage capability of tape and to achieve higher data rates.

With higher densities mechanical tolerances become more and more critical, however, and 800 cpi is probably the practical limit for NRZ1 recording. If

higher densities were to be achieved, a new recording method was required.

Phase encoding was chosen. Its advantages were well known from use of similar systems on drums and specialized tape drives. In computer use, tape density of 1600 cpi was selected, and a tape format was established first by IBM and later adopted by ANSI as a proposed American national standard.

Figure 1 shows graphically the effect of density on tape storage capacity as a function of block length.

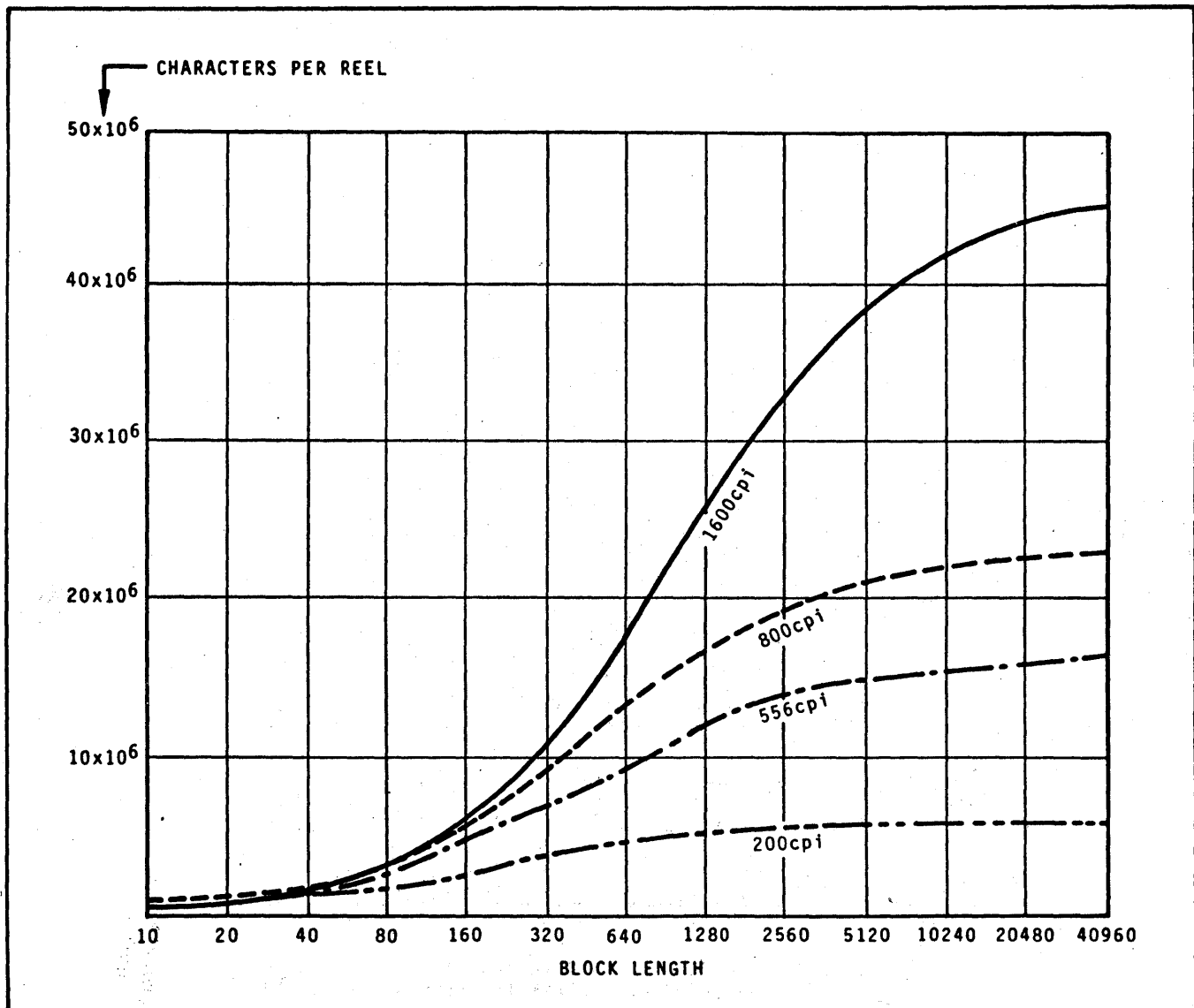


Figure 1. Comparison of Packing Density, Phase Encoded and NRZ1 Formats

### Phase Encoded Recording

Each of the nine tracks on a PE tape is recorded in such a manner as to allow recovery of a track clock plus the data. This removes the requirement for close skew alignment as in NRZ1 recording, since clocked data can be assembled in a register to remove the effects of skew.

Saturation recording is used. Tape is dc erased with a polarity such that the rim end of the tape becomes a north seeking pole. A one bit is defined as a flux reversal to the reference polarity. A zero bit is defined as a flux reversal toward the opposite polarity. A "phase flux reversal" is written at the nominal midpoint between successive ones or successive zeros to establish proper polarity.

Figure 2 shows the resulting pattern of reversals on tape. It will be seen that the recording results in two bit densities being recorded, 1600 flux reversals per inch (frpi) and 3200 frpi. Phase shift of these two frequency components is of the utmost importance for decoding after playback.

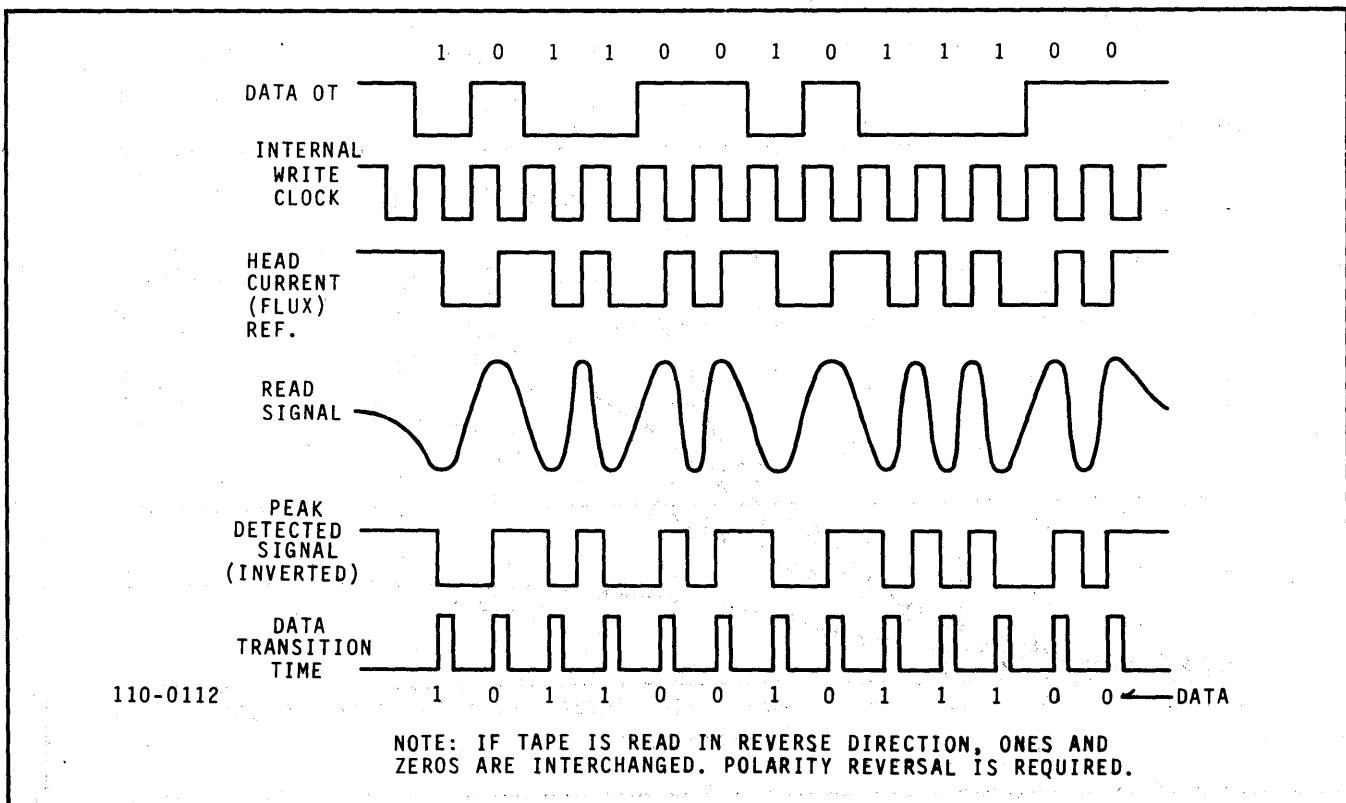
Figure 3 is a logic diagram of a write amplifier that generates the required waveforms.

### Tape Format

For IBM compatibility, tapes must be written in the proper format. This includes conventions on gap-lengths and special marks on tape. These have been chosen to ensure compatibility with nine-track 800 cpi NRZ1 on the same transport but with different electronics.

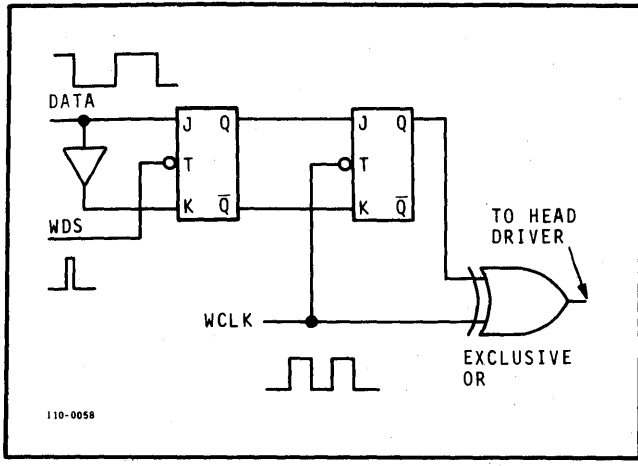
### PE Format Requirement

- a. Identification burst. A burst of recording in track 4 (P channel) only starting a minimum of 1.7 inches before the load point marker and extending past load point, but ending at least 0.5 inch before the first data block. Used to identify PE tapes.
- b. Initial gap. A gap of at least 3 inches between the load point marker and the beginning of the first data block.
- c. Preamble. A burst of 40 zero characters in each track followed by a character containing ones in each track.
- d. Data. Nine tracks, channel assignments same as 800 cpi.



**Figure 2. Phase Encoded Waveforms**





**Figure 3. Write Amplifier Logic**

- e. Postamble. An all ones character followed by 40 all zero characters.
- f. Interrecord gap. A gap 0.6 inch long nominal (0.5 inch minimum, 25 feet maximum) erased in the reference direction.
- g. Tape marks. Tape marks are special control blocks used to identify portions of the tape. As opposed to NRZ1 format which has only one tape mark, there are eight possible marks in PE format. Tape mark blocks may be from 64 to 256 characters in length and are recorded in the format shown in Table 1.

Reflective Strips

Load point and end-of-tape reflective strips are attached to the tape in the same positions and with the same meaning as in NRZ1 recording.

Check Characters

All PE tapes are written with odd vertical parity. There are no LRC or CRC characters in the PE system. They are not needed since the location of the track in error can be easily detected through the coding system.

Reading Phase Encoded Tapes

Reading methods for PE tapes differ, naturally, from NRZ1 methods. Following is a general discussion of means employed to extract recorded information. More specific circuit descriptions will be found in instruction manuals for Kennedy Company PE units.

Amplified head signal waveforms are shown in Figure 4 for a typical data block. Preamble and postamble are easily identified at the beginning and end of the block. Purpose of the preamble is to allow synchronization with the signal by a phase-locked oscillator before data begins. It is written at 3200 frpi (all zeros).

Because of tape and head response limitations, the high frequency components are of lower amplitude than the low frequency components.

Differentiation of the amplified signal is performed in read electronics. Signal is then crossover detected, and digitized. A new signal envelope detector is used to detect "dropouts" in order to precisely determine defective parts of tape. Up to three characters may be lost at the beginning of the block and some noise can be seen at the end of the block (after the last zero) for up to two characters time.

Two conditions should be met before signals are recognized as valid data: (a) Signals must be present in all tracks; (b) a number of zeros (approximately 25) must be followed by an all ones character preamble detected).

Once detected, the preamble combination of all ones must be treated as a valid character. All zeros is not a valid character unless the single track dropout line is active.

One phase-locked oscillator and associated electronics is recommended for better tolerance to tape deck

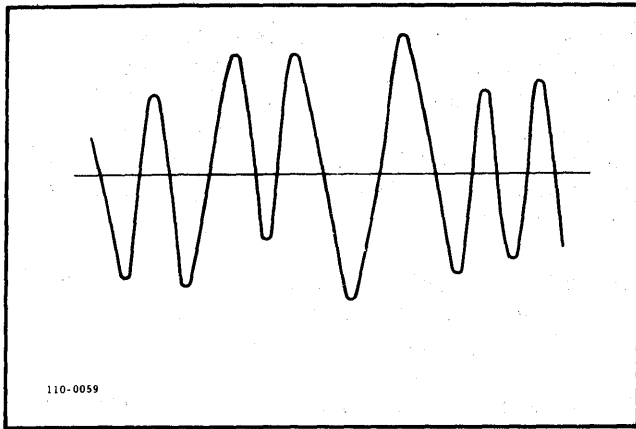
TRACK	CHANNEL	1	2	3	4	5	6	7*	8
1	5	X	-	X	-	X	-	X	-
2	7	X	X	X	X	X	X	X	X
3	3	-	-	-	-	-	-	-	-
4	P	-	X	X	-	-	X	X	-
5	2	X	X	X	X	X	X	X	X
6	1	-	-	-	-	-	-	-	-
7	0	-	-	-	X	X	X	X	-
8	6	X	X	X	X	X	X	X	X
9	4	-	-	-	-	-	-	-	-

- dc erased 110-0113

x recorded at 3200 frpi

\* most frequently used combination

**Table 1. Tape Mark Combinations**



**Figure 4. Read Signal**

speed variation and write data timing. Two detectors, a one detector and a zero detector, are used to develop data. If, in the required time, neither detector has an output, a single track dropout is signaled and data correction ensues.

Each read channel has three output lines: one, zero, clock. These three lines are fed to a four-stage

shift register controlled by an up-down counter. Upon entering the shift register, the 1 or 0 bit is shifted to the right to occupy the last open shift register cell. As data characters are read out, the shift register contents are shifted to the right. This allows up to four characters of skew. An error is posted if the skew register overflows.

Since single track dropouts are detected on a per bit basis and since the track in error is known, the character in the SR output stage can be corrected. This is done by reconstructing the missing bit by placing the remaining bits in a parity generator and adjusting the missing bit so that odd parity is achieved. If more than one track drops out, a multiple track error condition is flagged. In this case correction is not possible.

It can be seen from the preceding discussion that some complexity is required in the PE read electronics. If possible, it is desirable to share read electronics among several tape units as in Kennedy System 9000. If a customer wishes to build his own PE electronics, licenses are available to use Kennedy Company designs, thereby saving a considerable amount of engineering time.

## **Warranty**

Kennedy Company products are warranted to be free from defects in materials and workmanship for a period of one year.

Kennedy Company reserves the right to inspect any defective parts or material to determine damage and cause of failure.

This warranty does not apply to any Kennedy equipment that has been subject to neglect, misuse, improper installation and maintenance, or accident.

Liability under warranty is limited to no charge repair of defective units when equipment is shipped prepaid to factory or authorized service center after authorization from Kennedy Company to make such return.

Kennedy Company is continually striving to provide improved performance, value and reliability in their products, and reserves the right to make these improvements without being obligated to retrofit delivered equipment.

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