XT-4000E

Product Specification
and
OEM Manual

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WARRANTY

Maxtor warrants the XT-4000E Family of disk drives against defects in materials and workmanship for a period of twelve months, for the original purchaser. Direct any questions regarding the warranty to your **Maxtor** Sales Representative. **Maxtor** maintains Customer Service Centers for the repair/reconditioning of all **Maxtor** products. Direct all requests for repair to the **Maxtor** Service Center in your area. This assures you of the fastest possible service.

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PREFACE

Maxtor reserves the right to make changes and/or improvements to its products without incurring any obligation to incorporate such changes or improvements in units previously sold or shipped.

Maxtor publishes descriptive Brochures and Data Sheets, an OEM Manual, and a Quick Reference Guide for each product line. In addition, important changes to a product are conveyed in the form of a Technical Bulletin sent to all product customers of record. Changes that affect the content of any manual are covered by publishing addendum or revisions to the affected manual.

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1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The XT-4000E™ Family disk drives are high capacity, high performance random access storage devices using from five to eight nonremovable 5¼-inch disks as storage media. Each disk surface employs one moveable head to access 1,224 data tracks. The total unformatted capacity of the drive ranges from 179 to 385 megabytes.

The drive incorporates the Enhanced Small Device Interface (ESDI) high performance 5¼-inch standard. Among the resultant benefits are a 10 megabit per second transfer rate, status and configuration reporting across the interface, and nonreturn to zero (NRZ) data transfer.

Low cost and high performance are achieved through the use of a rotary voice coil actuator and a closed loop servo system using a dedicated servo surface. The innovative MAXTORQ™ rotary voice coil actuator provides an average access time of 16 milliseconds, typical, for the eight-disk model (14 milliseconds, typical, for the five-disk model). Track-to-track access time is 2.5 milliseconds for all models. This level of performance is usually achieved only with larger, higher powered, linear actuators. The closed loop servo system and dedicated servo surface combine to allow state of the art recording densities (1,070 tracks per inch, and 14,043 flux changes per inch) in a 5¼-inch package.

High capacity is achieved through a balanced combination of high areal recording density, run-length limited (RLL) data encoding techniques, and high density packaging techniques. **Maxtor's** advanced MAXPAK™ electronic packaging techniques use surface mount devices to allow all electronic circuitry to fit on one printed circuit board (PCB). Advanced 3380 Whitney-type flexures allow closer spacing of disks, and therefore allow a higher number of disks in a 5¼-inch package. **Maxtor's** unique integrated drive motor/spindle design allows a deeper head/disk assembly (HDA) casting than conventional designs, thus permitting more disks to be used.

The electrical interface is compatible with the industry standards established by the ESDI committee. The same basic drive/HDA is also available with a Small Computer System Interface (SCSI). The drive size and mounting conform to the industry standard 5¼-inch floppy and Winchester disk drives, and the drive uses the same direct current (DC) voltages and connectors. No AC power is required.

1.2 DRIVE FEATURES

The key features of the drive are as follows:

- storage capacity of 179 to 385 megabytes unformatted
- same physical size and mounting as standard floppy disk drives
- same control and data cabling as ST506/412 interface drives
- same DC voltages as standard floppy disk drives
- no AC voltage required
- rotary voice coil actuator and closed loop servo system for fast, accurate head positioning
- microprocessor-controlled servo for fast access time, high reliability, and high density functional packaging
- 10.0 megabit per second transfer rate
- ESDI interface
- track capacity of 20,940 bytes, unformatted
- thin film metallic media for higher bit density and resolution plus improved durability
- single PCB for improved reliability
- automatic actuator lock
- brushless DC spindle motor inside disk hub
- microprocessor-controlled spindle motor for precision speed control (±0.1%) under all load conditions
- dynamic braking during power down cycle
- user selectable hard or soft sectors
- synchronization of spindle motors for parallel data transfer of multiple drives

2.0 PRODUCT SPECIFICATIONS

This section lists all specifications for the XT-4000E Family disk drives.

2.1 PERFORMANCE SPECIFICATIONS

Table 1, Performance Specifications, lists the performance specifications for the drive.

	XT-4170E	XT-4380E
Capacity, Unformatted		
Per Drive (Mbytes)	179.45	384.53
Per Surface (Mbytes)	25.64	25.64
Per Track (bytes) (minimum)	20,940	20,940
Capacity, Formatted (512 bytes/sector)		
Per Drive (Mbytes)	157.93	338.4
Per Surface (Mbytes)	22.56	22.56
Per Track (Mbytes)	18,432	18,432
Sector/Track	36	36
Transfer Rate, Mbits/Sec	10.0	10.0
Typical Seek Time, msec*		
Average	14	16
Track-to-Track	2.5	2.5
Full Stroke	27	29
Max Seek Time, msec*		
Average	16	18
Track-to-Track	3	3
Full Stroke	34	34

* Includes Settling

Table 1
Performance Specifications

2.2 FUNCTIONAL SPECIFICATIONS

Table 2, Functional Specifications, lists the functional specifications for the drive.

	XT-4170E	XT-4380E
Rotational Speed (rpm) *	3,600	3,600
Average Latency	8.33	8.33
Recording Density (bpi)	21,064	21,064
Flux Density (fci)	14,043	14,043
Track Density (tpi)	1,070	1,070
Cylinders	1,224	1,224
Tracks	8568	18,360
Sectors (36 sectors/track)	308,448	660,960
Data Heads	7	15
Servo Heads	1	1
Disks	5	8

*Accurate to ± 0.1%

Table 2
Functional Specifications

2.3 PHYSICAL DIMENSIONS

Table 3, Physical Dimensions, lists the physical dimensions of the drive.

HEIGHT	= 3.25 in. (82.55 mm)
WIDTH	= 5.75 in. (146.05 mm)
DEPTH	= 8.20 in. (208.28 mm)
WEIGHT	= 7.1 lb (3.2 kg)
SHIPPING WEIGHT	= 9.3 lb (4.2 kg)
HEAT DISSIPATION	= 27 W Typical, 35 W Max.

Table 3
Physical Dimensions

2.4 ENVIRONMENTAL LIMITS

Table 4, Environmental Limits, lists the environmental limits of the drive.

	OPERATING	NONOPERATING
AMBIENT TEMPERATURE	50° F to 122° F (10° C to 50° C)	-40° F to 140° F (-40° C to 60° C)
MAXIMUM TEMPERATURE GRADIENT	18° F/hr (10° C/hr), Below Condensation	18° F/hr (10° C/hr), Below Condensation
RELATIVE HUMIDITY	8 to 80% Noncondensing with Max Gradient of 10% /hr	8 to 80% Noncondensing with Max Gradient of 10% /hr
MAXIMUM ELEVATION	10,000 ft	-1,000 ft to 40,000 ft
VIBRATION (INPUTS TO FRAME OF DRIVE)	All axes, 5-25 Hz, 0.006 in. P-P 25-500 Hz, 0.20 G Peak Acceleration	All axes, 5-31 hz, 0.02 inches P-P 31-500 Hz, 1.0 G Peak Acceleration
SHOCK (INPUTS TO FRAME OF DRIVE)	2 G with 11 msec Pulse Width, Half Sine Wave, (all axes)	20 G With 11 msec Pulse Width, Half Sine Wave, (all axes)

Table 4
Environmental Limits

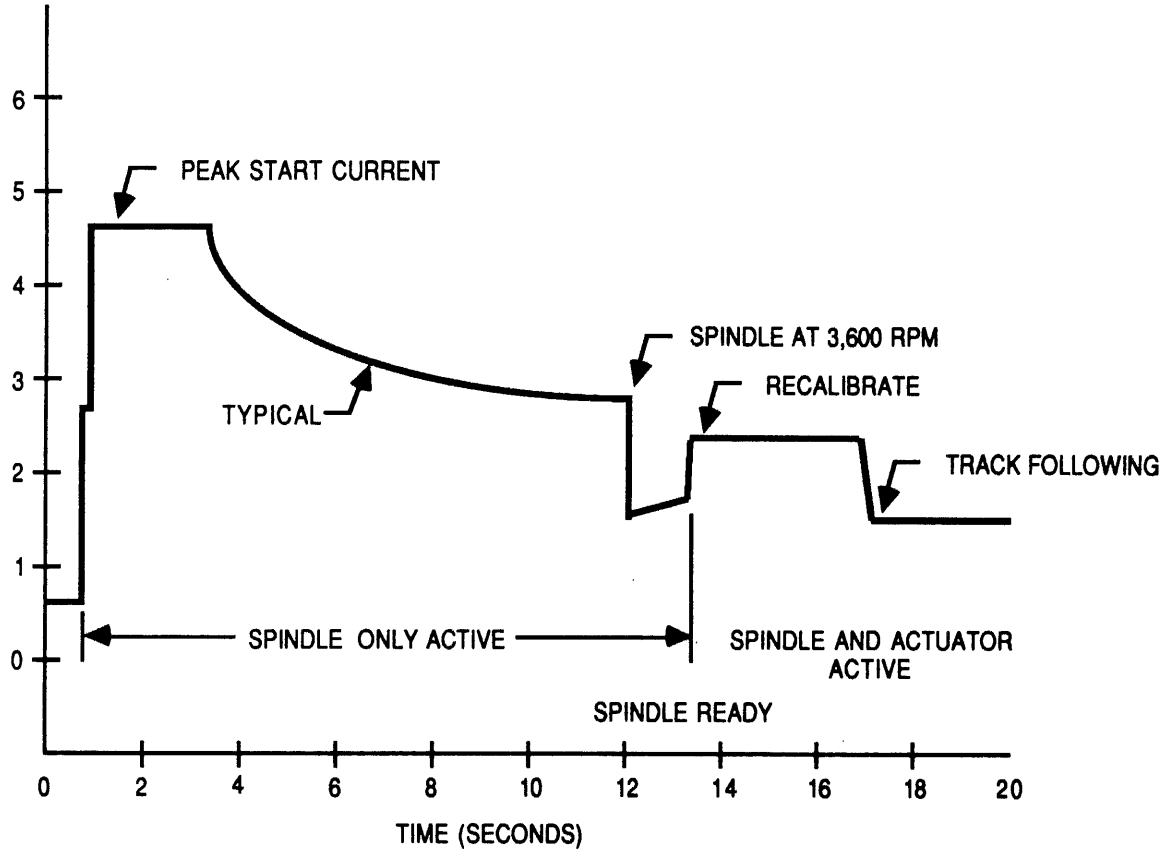
2.5 DC POWER REQUIREMENTS

Table 5, DC Power Requirements, lists the DC power requirements of the drive.

VOLTAGE (NOMINAL)	+12 V DC	+5 V DC
Regulation	±5%	±5%
Current (Typical)	1.5 A	1.7 A
Current (Maximum)	4.5 A *	1.9 A
Ripple (Maximum, P-P)	120 mV	50 mV

* Potential Current Surge for 1st 100 to 200 µsec to Charge Capacitors Dependent on Power Supply at Power On

Table 5
DC Power Requirements



NOTE: WHEN A FULL-LENGTH SEEK IS DONE, ONE ADDITIONAL AMP IS REQUIRED FOR A DURATION OF 15 MILLISECONDS

Figure 1
Typical 12 Volt Current Power Up Cycle

2.6 RELIABILITY SPECIFICATIONS

Table 6, Reliability Specifications, lists the reliability specifications for the drive.

MTBF	30,000 POH, Typical Usage
PM	Not Required
MTTR	30 Minutes
COMPONENT DESIGN LIFE	5 Years

Table 6
Reliability Specifications

2.7 ERROR RATES

Table 7, Error Rates, lists the error rate specifications for the drive.

SOFT READ ERRORS	10 per 10^{11} Bits Read
HARD READ ERRORS*	10 per 10^{13} Bits Read
SEEK ERRORS	10 per 10^{7} Seeks

*Not Recoverable Within 16 Retries

Table 7
Error Rates

2.6 STANDARDS AND REGULATIONS

The **Maxtor** XT-4000E Family disk drives satisfy the following standards and regulations:

UNDERWRITERS LABORATORIES (UL) = United States safety; UL 478, Standard for Safety, Electronic Processing Units and Systems.

CANADIAN STANDARDS ASSOCIATION (CSA) = Canadian safety; CSA C22.2 No. 220, 1986, Information Processing and Business Equipment (Consumer and Commercial Products).

VERBAND DEUTSCHER ELECTROTECHNIKER (VDE) = German safety; VDE 0806/8.81, Safety of Office Appliances and Business Equipment.

INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC) = International safety commission; IEC 950 (formerly 380), Safety of Information Technology Equipment.

FEDERAL COMMUNICATIONS COMMISSION (FCC) = United States radiation emissions; Part 15, Subpart J, Class B Consumer Computing Devices.

CAUTION: *Connections between equipment must be made with shielded cables, and a shielded power cord must me used to connect AC power to the unit.*

CAUTION: *This equipment generates and uses radio frequency energy, and may cause interference to radio and television reception if not installed and used in strict accordance with the instructions in this manual and in XT-4000S Service Manual.*

The drive has been tested and found to comply with the limits for a Class B computing device, in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against radio and television reception interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference using one or more of the following measures:

- reorient the receiving antenna
- reorient the computer with respect to the receiver
- move the computer away from the receiver
- plug the computer into a different outlet, so that the computer and receiver are on different branch circuits

If necessary, consult the dealer, or an experience radio/television technician, for additional suggestions. You may find the FCC booklet *How to Identify and Resolve Radio TV Interference Problems* helpful. This booklet is available from the United States Government Printing Office, Washington, D.C., 20402, stock number 004-000-00345-4.

Maxtor is not responsible for any radio or television interference caused by unauthorized modifications to the drive. It is the responsibility of the user to correct such interference.

3.0 FUNCTIONAL CHARACTERISTICS

The XT-4000E Family disk drive consists of read/write and control electronics, read/write heads, a servo head, a head positioning actuator, media, and an air filtration system. The components perform the following functions:

- interpret and generate control signals
- position the heads over the desired track
- read and write data
- provide a contamination-free environment

3.1 READ/WRITE AND CONTROL ELECTRONICS

Drive electronics are packaged on a single PCB. This board, which includes two microprocessors, performs the following functions:

- reading/writing of data
- index detection
- head positioning
- head selection
- drive selection
- fault detection
- voice coil actuator drive circuitry
- track zero detection
- recalibration to track zero on power up
- track position counter
- power and speed control for spindle drive motor
- braking for spindle drive motor
- drive up-to-speed indication circuit
- monitoring for write fault conditions
- control of all internal timing
- generation of seek complete signals
- RLL encoding/decoding
- data separation
- address mark detection (soft sector)
- sector detection (hard sector)
- spindle synchronization

3.2 DRIVE MECHANISM

A brushless DC drive motor, contained within the spindle hub, rotates the spindle at 3,600 revolutions per minute. The spindle is direct driven, with no belt or pulleys being used. Dynamic braking is used to quickly stop the spindle motor when power is removed. The HDA is shock mounted to minimize transmission of vibration through the chassis or frame.

3.3 AIR FILTRATION SYSTEM

The disks and read/write heads are assembled in an ultra clean-air environment and then sealed within the module. The module contains an internal absolute filter, mounted inside the casting, to provide constant internal air filtration (see Figure 2, Air Filtration System). A second filter, located on top of the base casting, permits pressure equalization between internal and ambient air.

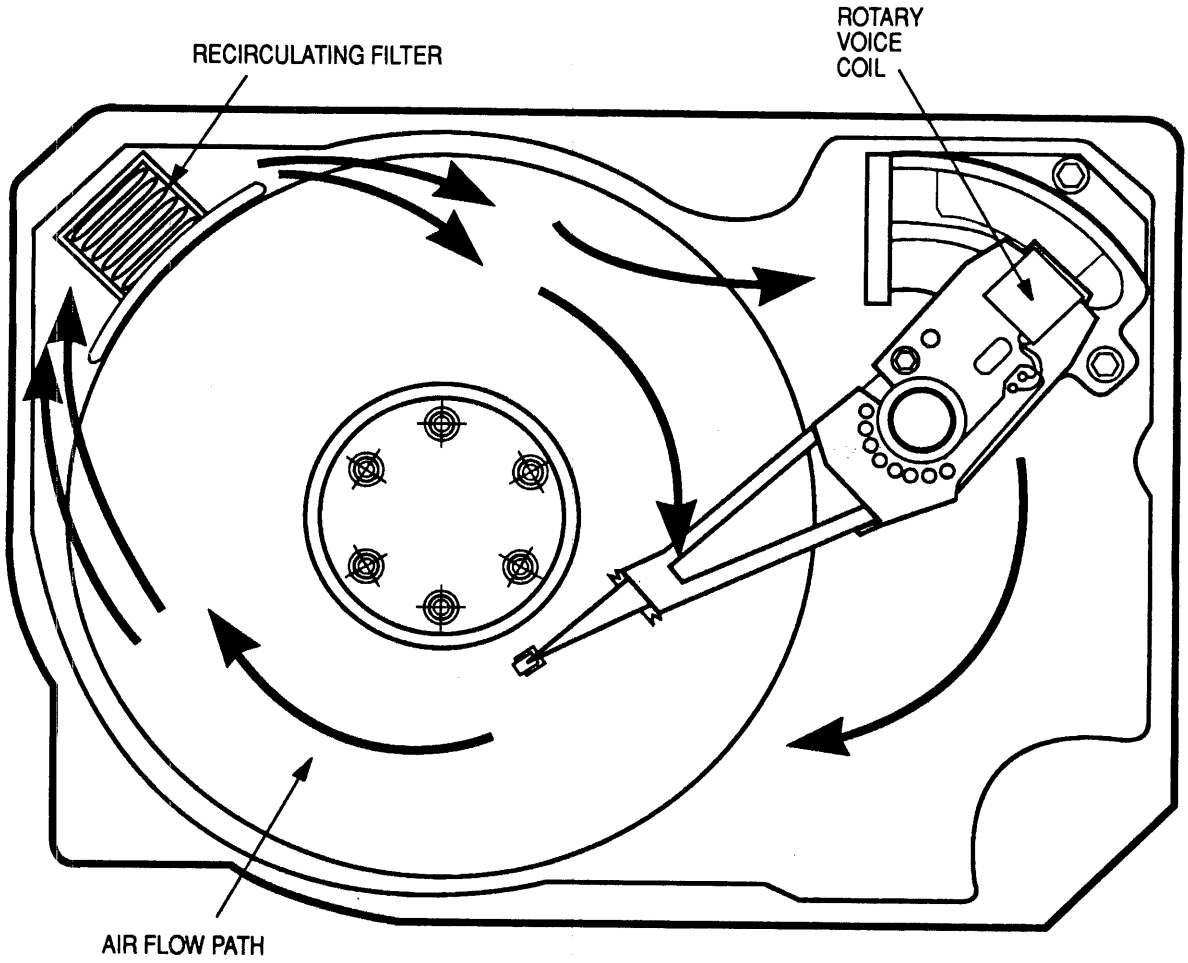


Figure 2
Air Filtration System

3.4 POSITIONING MECHANISM

The read/write heads are mounted on a head arm assembly, which is then mounted to a ball bearing supported shaft. The voice coil, an integral part of the head/arm assembly, lies inside the magnet housing when installed in the drive. Current from the power amplifier, controlled by the servo system, causes a magnetic field in the voice coil which either aids or opposes the field around the permanent magnets. This reaction causes the voice coil to move within the magnetic field. Since the head arm assemblies are mounted on the voice coil, the voice coil movement is translated through the pivot point directly to the heads, and positions the head over the desired cylinder. See Figure 3, Head Positioning System.

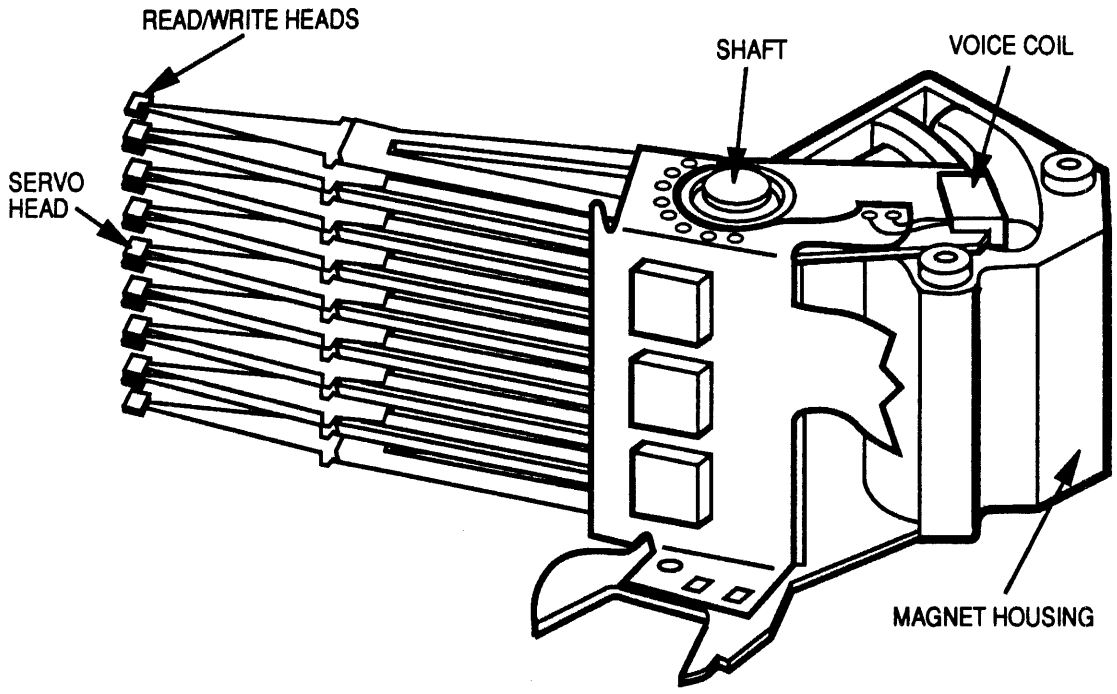


Figure 3
Head Positioning System

Actuator movement is controlled by the servo feedback signal from the servo head. The servo head is located on the lower surface of the fourth disk from the top, where servo information is prewritten at the factory. This servo information is used as a control signal for the actuator to provide track-crossing signals during a seek operation, track-following signals during on cylinder operation, and timing information, such as index, sector pulses (hard sector), and servo clock.

3.5 READ/WRITE HEADS AND DISKS

The drive employs thin film heads and Whitney-type flexures. This configuration of sliders and flexures provides improved aerodynamic stability, superior head/disk compliance, and a higher frequency response than conventional ferrite heads.

The medium uses thin metallic film deposited on 130 millimeter diameter aluminum substrates. The metallic surface, together with the low load force/low mass Whitney-type heads, permit highly reliable contact start/stop operation. The metallic recording film yields high amplitude signals, and very high resolution performance compared to conventional oxide coated media. The metallic medium also provides a highly abrasion-

resistant surface, decreasing the potential for damage caused by shipping shock and vibration.

Data on each of the data surfaces is read by one of fifteen read/write heads, each of which accesses 1,224 tracks. There is one surface dedicated to servo information in each drive.

4.0 THEORY OF OPERATION

The drive PCB assembly provides four major functions, 1) spindle motor control; 2) actuator control for head/positioning; 3) the read and write data channel; and 4) ESDI hardware and protocol implementation. In addition, power conditioning and monitoring is provided. Figure 4, General Block Diagram, shows the organization of these functions and the major subsections of each. The following paragraphs describe each of these in more detail.

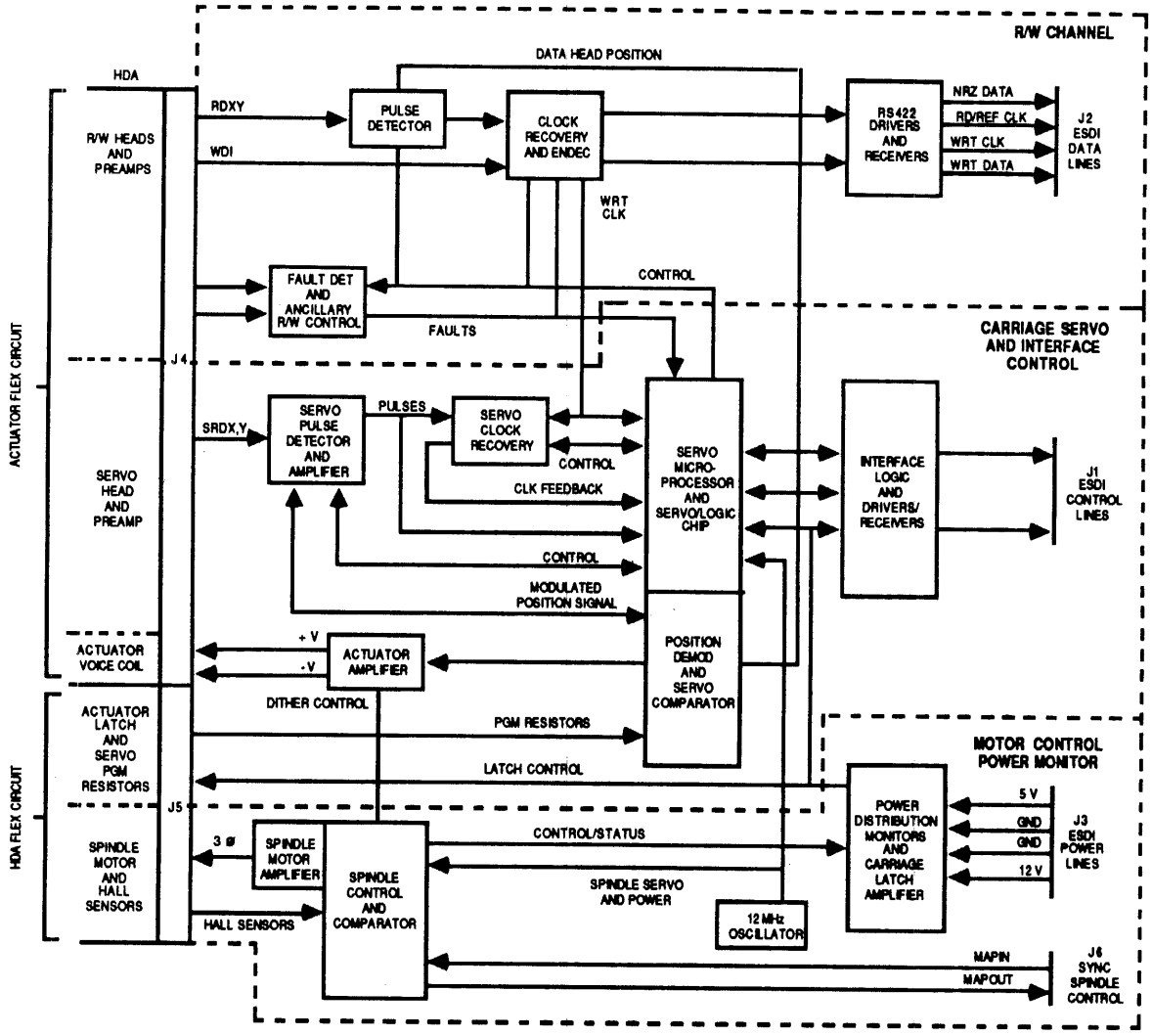


Figure 4
General Block Diagram

4.1 SPINDLE MOTOR CONTROL

The spindle motor in the drive uses a three-phase delta-wound brushless DC motor located inside the hub. Commutation is determined by three hall effect sensors which are mounted on a flex circuit at the bottom of the casting. These hall effect sensors sense magnets under the spindle motor.

4.1.1 Hardware Configuration

Figure 5, Spindle Control Hardware, presents a component block diagram of the spindle system. The hardware provides the functions described below. The Z8 microcontroller is the central element in this diagram, serving to coordinate, direct, and control all of the activity of the spindle.

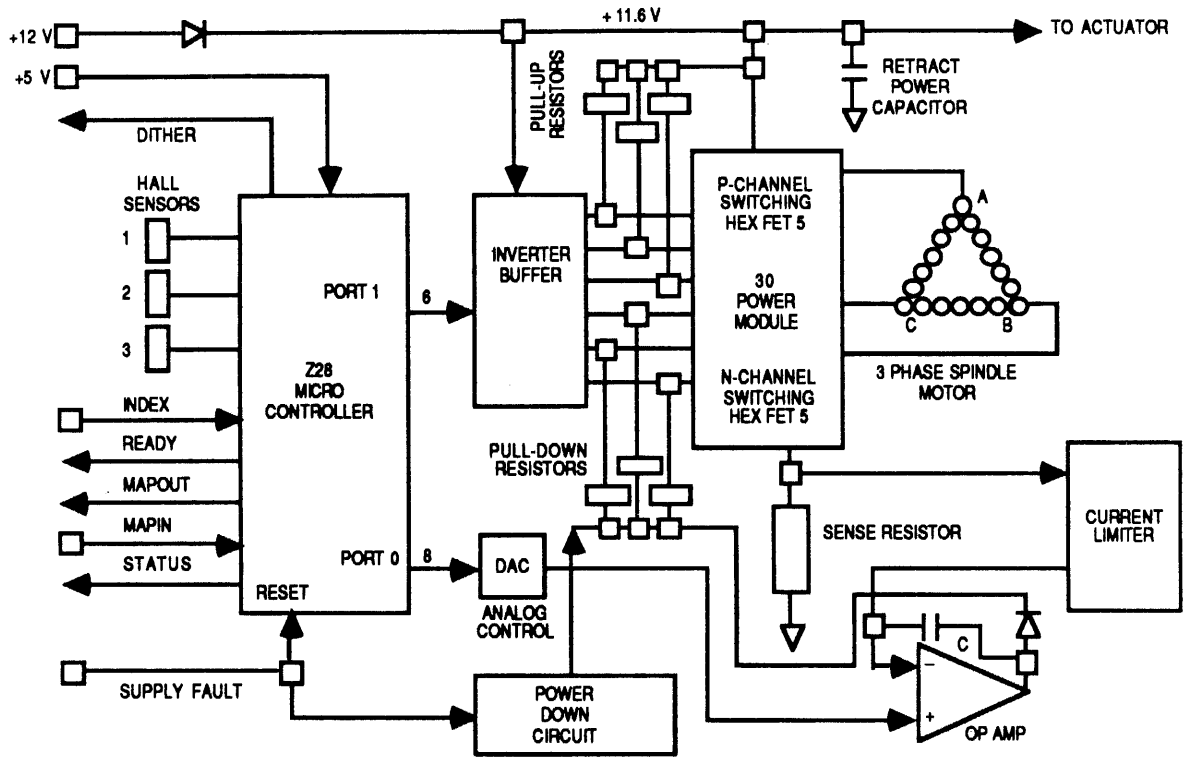


Figure 5
Spindle Control Hardware

The output of the hall sensors is mapped by the Z8 microcontroller into a three phase commutation sequence. This sequence continuously commutates the in-the-hub four-pole three phase spindle drive motor through the three phase H-bridge power module (six power transistors). The current through the motor is monitored by the voltage across the 0.1 ohm sense resistor. Current control is obtained by comparing the sense voltage with the digital analog converter (DAC) output at a high gain op-amp, and then closing the analog control loop through the (lower) power transistors; an integrating capacitor around the op-amp stabilizes the loop. The net effect of this loop is to desensitize the circuit to variations in the power transistor parameters.

Additional analog circuitry shown in Figure 5, Spindle Control Hardware, provides current limiting of the motor current, and provides graceful shutdown (homing of the actuator and dynamic braking of the spindle) in the event of loss of power, or if the spindle motor is turned off by a STOP command in remote mode.

4.1.2 Spindle Modes of Operation

Figure 6, Spindle Control Flow Chart, is a diagrammatic description of the in-line/real-time microcontroller diagnostics for the spindle control system.

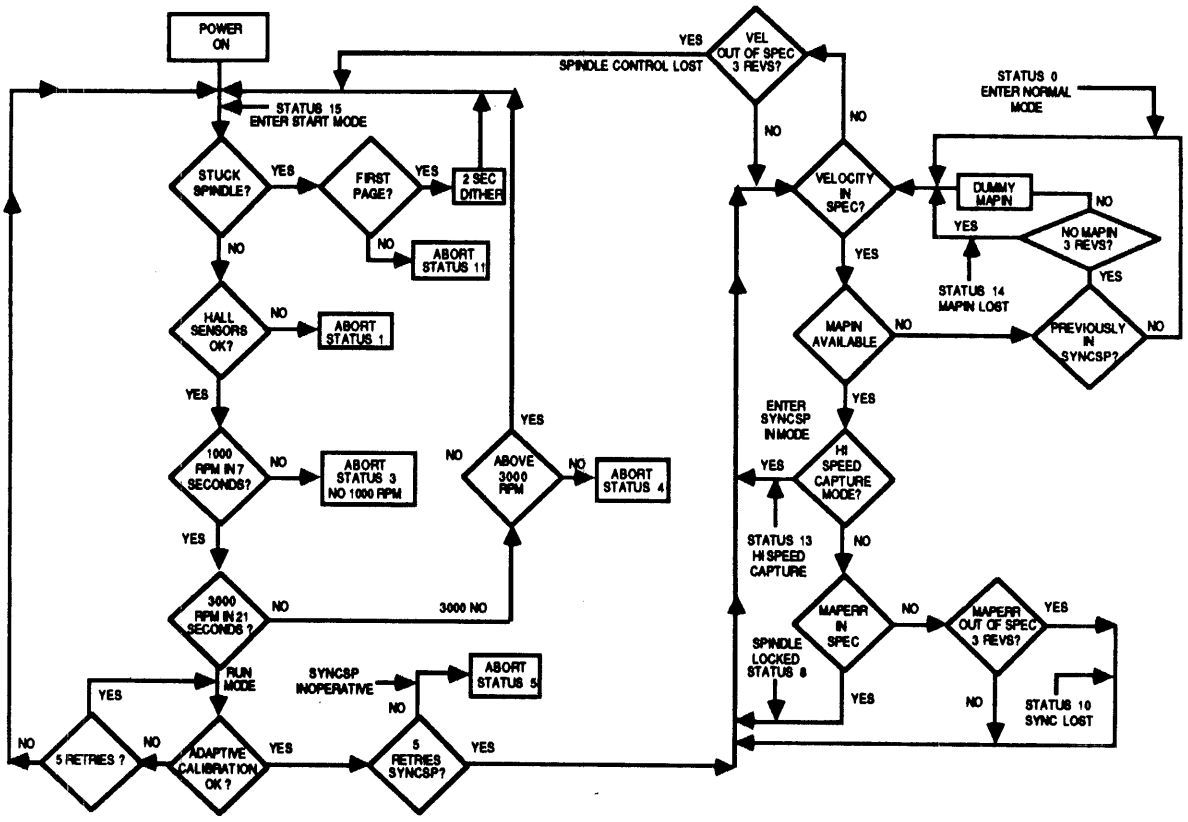


Figure 6
Spindle Control Flow Chart

The flowchart describes the sequence of microcontroller activity required during each of the spindle modes of operation; this sequence provides a detailed overview of the diverse control and auxiliary functions of the spindle. The sequence, programmed as algorithms in the microcontroller, provides three basic modes of operation for the drive: START mode, RUN mode, and SYNCSP (synchronous spindle) mode.

START Mode: At power up with the spindle at rest, full current (limited to 4.0 amps) is applied to the spindle motor. Progressive diagnostic and timing checks are performed to detect a spindle drive malfunction and to take corrective action as follows:

- Detect a Stalled Spindle Motor
  The hall sensors are tested for (commutation) motion. If one second elapses without motion, either a "stuck" spindle or a power module failure is indicated; actuator dither is invoked to free up the spindle, and STATUS 2 is posted. At the end of two seconds of dither, motion is checked again and if not detected, STATUS 2 is posted and the spindle aborts (powers down).

- Detect a Hall Sensor Failure
  The states of the hall sensors are continuously checked at commutation until velocity lock on. If an illegal state occurs in two consecutive revolutions, STATUS 1 is posted and the spindle aborts.

- Check 1,000 revolutions per minute at 7 Seconds
  The commutation is timed for 1,000 revolutions per minute to occur within 7 seconds. If 1,000 revolutions per minute do not occur, this indicates excessive drag forces from the head or bearings, or a motor/driver failure; STATUS 3 is posted and the spindle aborts.

- Check 3,000 revolutions per minute at 21 Seconds:
  The commutation is timed for 3,000 revolutions per minute to occur within 21 seconds. If above 3,000 revolutions per minute, the spindle tries to achieve 3,600 revolutions per minute; in contrast to the stalled spindle motor and 1,000 revolutions per minute in 7 seconds checks, a sufficient back electromotive force from the motor has reduced the voltage overhead across the drivers in the power module such that the reduced power dissipation of the drivers allows multiple retries. (A RETRY is performed beyond this point for any return into the START mode.)

RUN Mode: Upon entering RUN mode, the microcontroller sequentially enters a) an adaptive routine to compute the quiescent drag force of the bearing/disks and to compute the dynamic system constant from the DAC input to motor velocity; b) an electronic commutation routine; and c) a velocity lock-on-routine (in thirty revolutions) to insure (monitored) velocity operation of 3,600 revolutions per minute ±0.1%. The system is then given a STATUS 0 identification of normal mode operation. If a failure occurs at any point between a) and c), the system goes into RETRY mode (into START mode) and is monitored for five successive failures without velocity lock-on before ABORT.

At velocity lock-on, a READY signal is posted to the interface microcontroller to signal that the spindle is at recording velocity (3,600 revolutions per minute).

A feature of the drive is the capability of synchronous spindle operation (spindle locked operation) in which INDEX lock is achieved between a master drive and up to forty eight slave drives. This feature allows serial data streams to operate in parallel and thereby multiplies the system data transfer rate (drive-to-host computer) by the number of slave drives.

When the drive is in RUN mode, the code of the microcontroller provides two simultaneous functions: 1) generation of a MAPOUT (master pulse out); and 2) search for a MAPIN (master pulse in). Normal operation implies the lack of a MAPIN pulse, and while in this mode, the drive defaults to a master drive designation.

If a MAPIN pulse is detected, the drive is posted with a slave drive designation (MAPIN available) and the drive goes into SYNCSP mode.

SYNCSP Mode: Upon detection of MAPIN by the microcontroller, the slave drive enters a high-speed CAPTURE mode to bring the MAPIN pulse to the MAP (master pulse) window. Normal velocity control is in effect during this operation (NORMAL mode).

As MAPIN approaches the outer boundaries of the MAP window, a velocity adjustment is made to the slave drive to return the drive to normal velocity prior to entering the MAP window and subsequent phase lock. Within the MAP window, bounds are tested for velocity error and phase error. When the two are within their tolerance zones, the system switches to a phase controlled configuration, wherein the slave drive is locked to the MAPIN pulse, and synchronous spindle operation (spindle locked) STATUS 8 is posted.

In the SYNCSP mode, the velocity and phase error are constantly monitored to assure velocity and INDEX phase tolerances as follows:

velocity: 3,600 revolutions per minute ±0.1%
master INDEX/slave INDEX lock ±40 microseconds

If the SYNCSP lock error (MAPERR) is out of tolerance (STATUS 10), the system reverts to CAPTURE mode. If the velocity is out of tolerance (spindle control lost), RETRIES are performed via START mode (recalibration of the adaptive loop) and if SYNCSP is not achieved (with MAPIN available), a SYNCSP inoperative condition error (STATUS 10) is posted and the system attempts operation in NORMAL mode.

4.2 ACTUATOR CONTROL

This section describes the servo system used in the XT-4000E Family disk drives. The same servo system is used for both models, with small modifications made to accommodate the different number of heads unique to each model. Two functions are provided, precision track following, and carriage motion to specific tracks in response to in-

terface commands. Typical track-to-track and average access times are 14 milliseconds for the XT-4170E and 16 milliseconds for the XT-4380E.

A dedicated servo surface and quadrature servo pattern is used. This servo incorporates evolutionary and detail improvements over prior generations of **Maxtor** servos.

The level of electronics integration is very high. Three custom analog integrated circuits, an actuator driver integrated circuit, and a standard cell servo logic chip (SLC), are used to implement the servo functions. In addition, the servo uses a microcontroller, which is shared with the drive interfacing function.

4.2.1 Servo Pattern

The servo pattern consists of 3,808 servo frames per track with twenty-two servo clock intervals per frame. This yields a 228 kilohertz frame rate for the system. Four dibit pulses encode the quadrature position information, and one pulse each is used for synchronization and data (see Figure 7, Servo Pattern and Read-Back Signal I). When the data pulse is present, the frame has a logical "1" value. When the pulse is not present, the frame has a logical "0" value. This serial pulse stream is decoded in 16-bit words, with parity, and is used to encode the absolute track address, index, and configuration data used by the drive and the servo. Thus, the words are repeated 238 times per revolution for a word rate of 14.3 kilowords per second. The synchronization pulse, which follows the data pulse, is present in every frame and is used to synchronize to the servo pattern. The first pair of position pulses, A and B, are used for positioning on even numbered data tracks. The second pair of pulses, C and D, are used for positioning on odd numbered tracks.

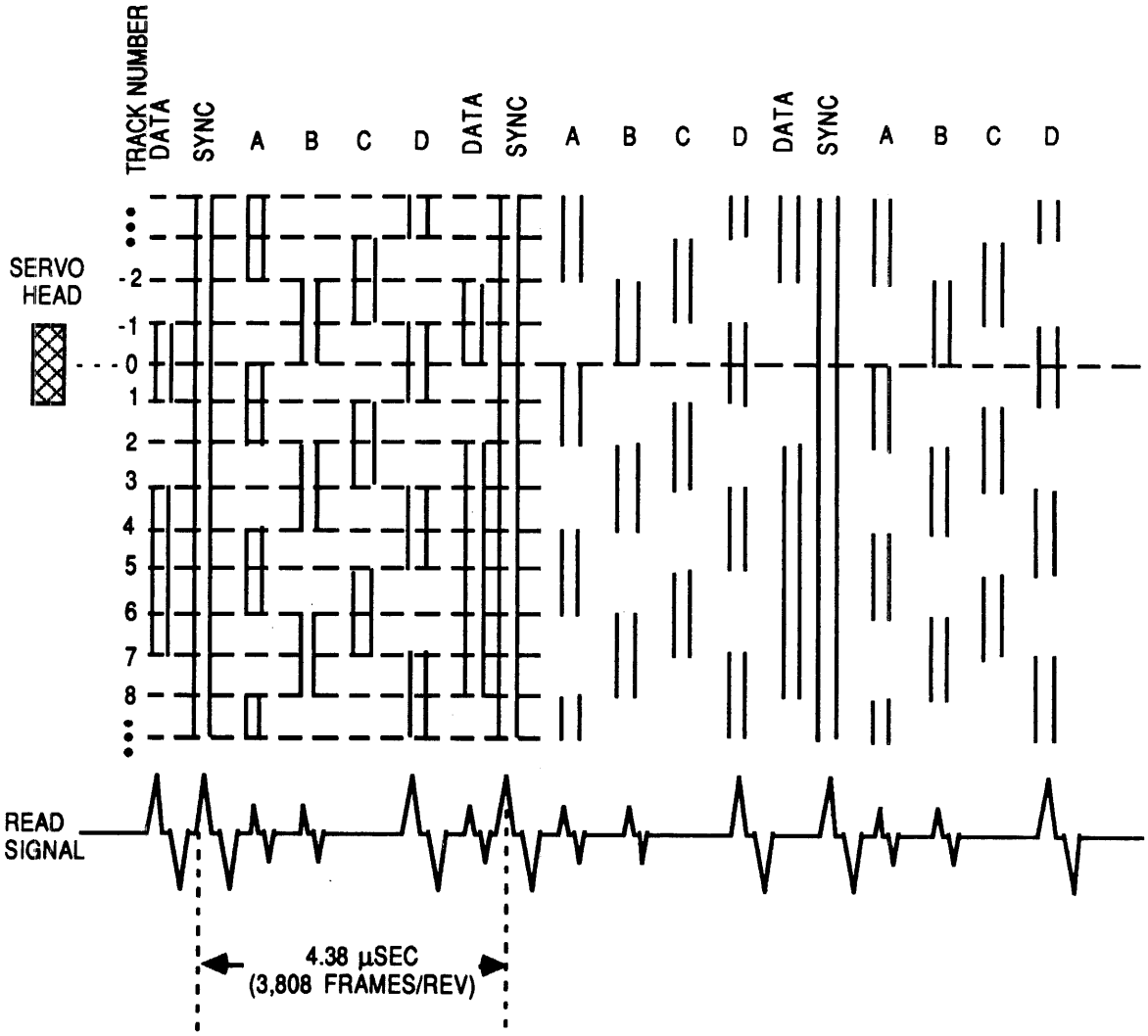


Figure 7
Servo Pattern and Read-Back Signal I

4.2.2 Block Description

Refer to Figure 8, Servo System, and Figure 9, Main Servo Loop, when reading the following descriptions.

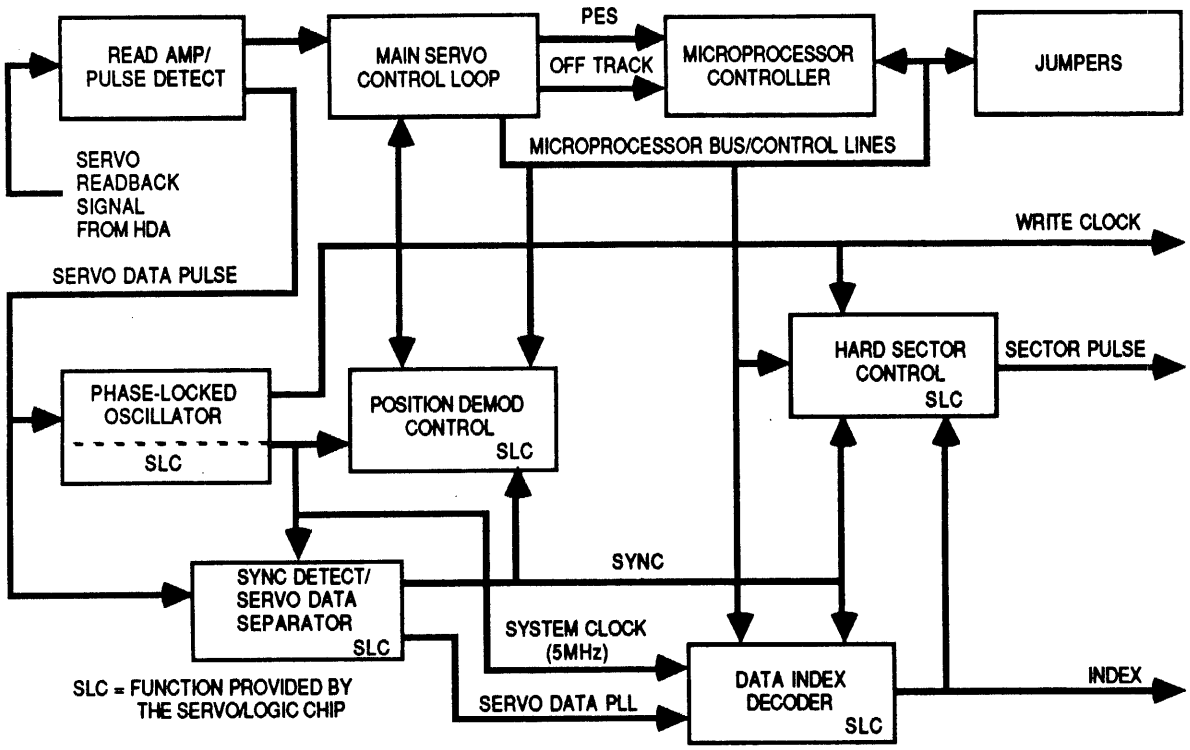


Figure 8
Servo System

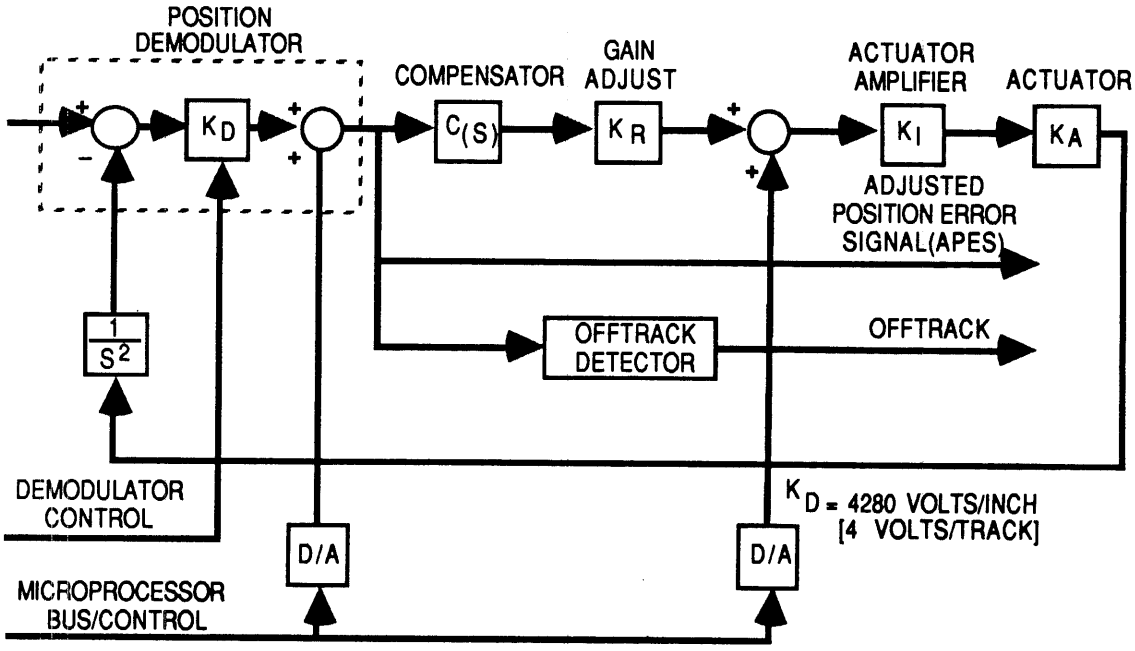


Figure 9
Main Servo Control Loop

A READ AMPLIFIER/PULSE DETECTOR

The read amplifier and pulse detector provides automatic gain control (AGC) a buffer amplifier for the servo filter and a pulse detector for the dibit pulses. The raw servo signal from the preamplifier enters the read amplifier and is applied to the AGC amplifier. The AGC loop is closed through the position demodulator. The amplified and normalized servo signal then passes through a filter for noise reduction and then on to the pulse detector and peak detector.

The pulse detector detects the zero crossing between the positive and negative going portions of the dibit pulses. The digital output of this detector is used to decode data pulses and issued as the input for the phase-locked oscillator. The peak detector samples the peak values of the position pulses and establishes a reference baseline from which to measure these peak values. The discharge current of the peak detector is switchable to allow the use of a long time constant (peak hold) during servoing, and a shorter time constant which is used to facilitate lock up of the AGC loop at power on.

B PHASE-LOCKED OSCILLATOR

The phase-locked oscillator (PLO) harmonically locks to the incoming pulse stream from the pulse detector. During synchronization the oscillator locks in phase and frequency mode to a reference clock generated in the SLC. Also, in the SLC, the oscillator output is divided and used to generate the 5 megahertz master clock from which timing gates are derived. This clock is divided again to provide the 2.5 megahertz feedback clock for the PLO. The fundamental oscillator output frequency is 20 megahertz.

Since the PLO output is synchronized with the physical rotation of the disk stack, it is used as the write clock and as the clock for the sector counter for hard sector mode operation.

C SYNCHRONIZATION DETECTOR AND SERVO DATA SEPARATOR

The synchronization detector and servo data separator in the SLC detect the data and synchronization transitions, which are the first two dipulses present in each servo frame. The extracted synchronous transitions are used to create the absolute frame reference for synchronizing the servo frame and for decoding servo position information. Capability is provided for tolerating servo surface defects which may cause missing synchronization pulses. The serial data stream of data pulse transitions is used to verify lock by virtue of its limited run length of zeros when proper lock is in effect. Parity of the data words is also checked. The microprocessor constantly monitors synchronization and data and initiates relocking the PLO and reinitializing the servo if synchronization is lost.

D DATA AND INDEX DECODER

The data and index decoder in the SLC is a 16-bit shift register whose contents are read every sixteen frames. If all the frames are valid the word is passed on to other logic in the SLC and then to the microprocessor controller. Index is delineated by a preindex and index word sequence. Absolute track information is also encoded with redundancy. The absolute track information is constantly monitored to verify that the servo is positioned on the correct track. In addition to index and track coding, the guard bands contain configuration data which is used to configure a given PCB for a given HDA. In this way, the same PCB may be used for a family of products. Configuration data includes the number of data tracks and heads, the servowriter version and drive capacity, and the dynamic constants to be used when seeking.

E HARD SECTOR CONTROL

The hard sector capability of the drive is provided by a programmable counter in the SLC. This counter is clocked by the PLO and is synchronized with index. User defined jumpers on the PCB are used to set the desired number of bytes per sector. Alternatively, the desired number of bytes per sector may be set via the drive interface. The microprocessor either reads the jumpers or receives the interface command, and in turn sets the decode logic for the proper sector size. The sector pulses are very accurately timed to data since the sector clock is locked to disk rotation.

F POSITION DEMODULATOR CONTROL

Timing windows are created in the SLC to gate the synchronization pulses, data pulses, and servo position dipulses. The servo master clock derived from the PLO divides each servo frame into twenty-two equal segments, and is used as the reference for generating these gates. A nominal disk rotation speed of 3,600 and 3,808 frames per revolution results in a 5 megahertz servo master clock.

The synchronization pulse is used to align the gates to the servo frames. The gate generated for synchronization is used to verify lock to synchronization. If lock is lost, synchronization pulses stop appearing in the proper synchronization window and a relock process is initiated by the microprocessor. The gate generated for data pulses is used to decode servo data. When no transition is detected in the window, the frame has a logical "0" value, and when a data transition does occur in the window, the frame has a logical "1" value.

The four gates generated for the four position dipulses (A, B, C, and D) are used to switch the peak detectors in the position demodulator from a tracking mode to a hold mode, providing position information to the control system.

G MAIN SERVO CONTROL LOOP

The peak-detected A, B, C, and D dipulses are used to create the locking edges for the position loop. Difference signals corresponding to A-B, B-A, C-D, and D-C are synthesized and used for servoing on the appropriate data tracks.

With the quadrature pattern, track zero uses A-B, track one uses C-D, track two uses B-A, and track three uses D-C. This pattern is repeated every fourth track so that tracks zero, four, eight, twelve, etc., use A-B for generating the position error signal.

Digital to analog converters in the SLC are controlled by the microprocessor. During SEEKs, position and velocity control trajectories are calculated by the microprocessor

and output to the servo control loops via these DAC's. These trajectories are calculated based on the configuration data which is read at power up. The configuration data contains the dynamic constants which are used in calculating the SEEK trajectories.

During track following, the position error is monitored by hardware to obtain fast response to shut down the write current should an off track condition occur during a write operation.

H MICROPROCESSOR CONTROLLER

The servo microprocessor exercises supervisory control over the servo during track following mode, and active control while seeking. In addition to the servo function, the microprocessor performs interface control functions per ESDI specifications.

The various peripherals, such as the SLC and configuration jumpers, are memory mapped. The microprocessor makes use of registers inside the SLC for drive status, control, seek current DAC output, position offset current DAC output, track address, servo data words, and peripheral control via output port pins in the SLC.

The microprocessor also controls the recalibration sequence when power is first applied to the drive. When the drive is jumpered to enable starting and stopping the spindle motor via the interface, the microprocessor controls the reset line to the spindle control microprocessor. The status of the spindle control microprocessor is monitored by the servo microprocessor to determine status and detect any error conditions in the system. Such status information is then available to the host through the drive interface.

The servo microprocessor also controls the actuator latch and releases the actuator when the spindle is locked to the proper speed. After power is removed from the drive, or a spindle stop command is received from the interface, the actuator driver pushes the headstack into the landing zone and the latch is enabled. This action takes place while the spindle is still spinning and before dynamic braking begins.

I JUMPERS

Two classes of servo jumpers are used in the drive. The first class includes factory jumpers which configure the PCB to work properly for the particular model of drive on which it is installed. These jumpers program the number of heads, the data transfer rate, and the synchronization field required by the data separator. The microprocessor reads these jumpers and performs accordingly.

The second class of jumpers comprises user selectable jumpers. These jumpers are for setting a hard or soft sectored mode of operation, selecting the sector size in hard sector

mode, enabling or disabling the ability to set the hard sector size through the drive interface, and enabling or disabling automatic spinup.

4.3 READ/WRITE CHANNEL

The read/write channel is described in the following paragraphs.

4.3.1 HDA Flex Circuit Interface

A description of the HDA flex circuit interface, including the preamplifier integrated circuit, power, head selection, the READ signal, and the WRITE mode and write unsafe, follow.

A PREAMPLIFIER INTEGRATED CIRCUIT

The preamplifier/write driver that is used on the flex circuit is the SSI 521 integrated circuit. This is a thin film head compatible circuit capable of interfacing with up to six heads. There are three SSI 521 chips used on the flex circuit so that a maximum number (fifteen) of heads for a drive can be selected.

B POWER

Power is supplied from the main drive PCB through the flex circuit connector, J4. The voltage requirements are Vcc = +5 volts, Vdd = +12 volts.

C HEAD SELECTION

The head selection circuitry starts at the ESDI interface connector, J1. There are four head select lines used at the ESDI interface (Figure 10, Head and Drive Selection).

-Headselect 2^0
-Headselect 2^1
-Headselect 2^2
-Headselect 2^3

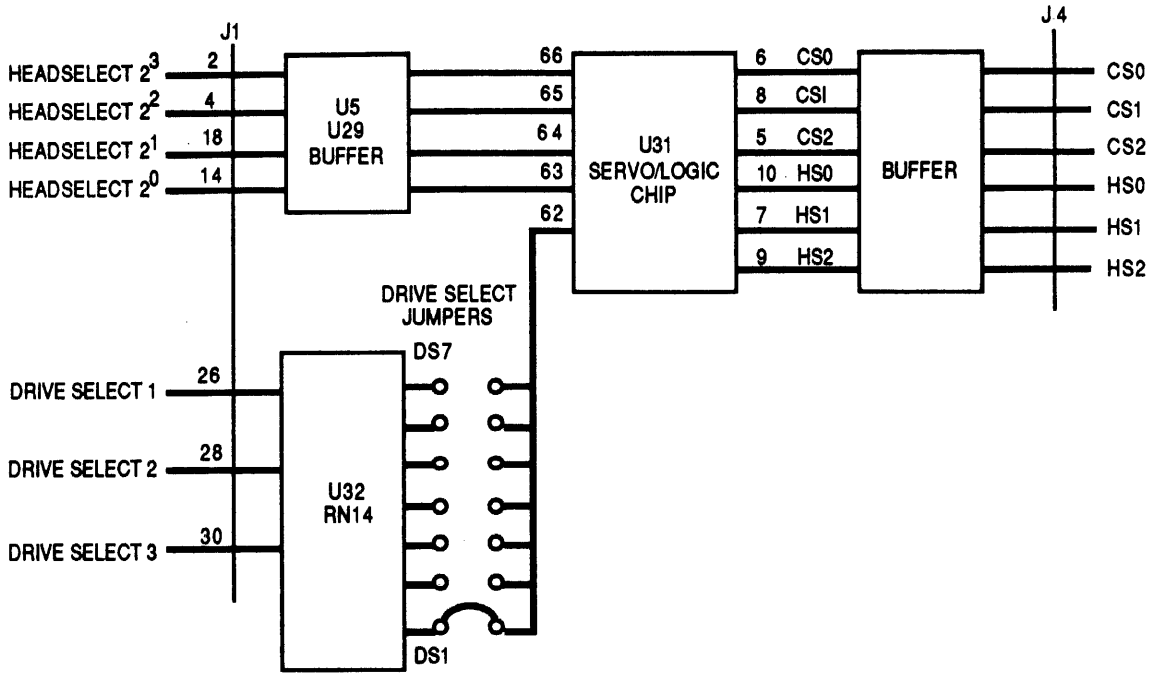


Figure 10
Head and Drive Selection

These are then encoded by the SLC into three chip select lines and three head select lines that are used by the flex circuit. These lines are listed below (also, see Figure 11, Preamplifier Head Selection and Read-Back Signal).

CS0*
CS1*
CS2*
HS0
HS1
HS2

* Negative true

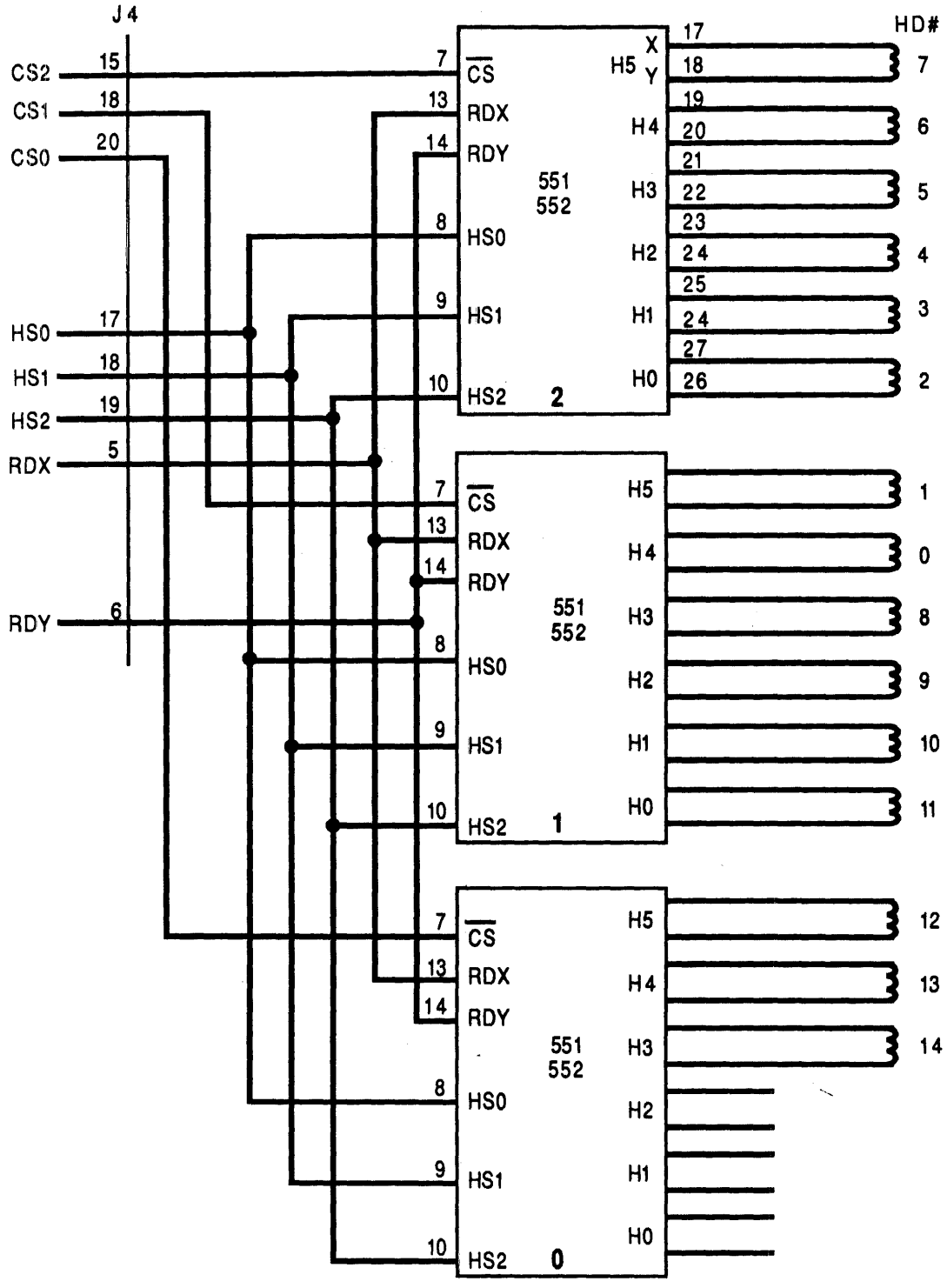


Figure 11
Preamplifier Head Selection and Read-Back Signal

The encoding for the heads is listed in Figure 12, Head Selection Map. Also shown is the mapping of the heads within the HDA.

HD	CS2	CS1	CS0	HS2	HS1	HS0
0	1	0	1	1	0	0
1	1	0	1	1	0	1
2	0	1	1	0	0	0
3	0	1	1	0	0	1
4	0	1	1	0	1	0
5	0	1	1	0	1	1
6	0	1	1	1	0	0
7	0	1	1	1	0	1
8	1	0	1	0	1	1
9	1	0	1	0	1	0
10	1	0	1	0	0	1
11	1	0	1	0	0	0
12	1	1	0	1	0	1
13	1	1	0	1	0	0
14	1	1	0	0	1	1

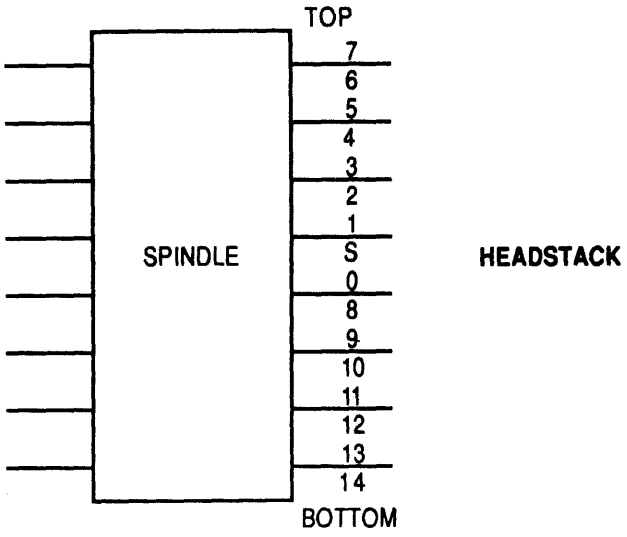


Figure 12
Head Selection Map

D READ SIGNAL

The amplified read-back signal is output from the flex on the RDX (read data x) line. RDY (read data y) lines are shown in Figure 12, Head Selection Map. The nominal gain from the head input, HnX and HnY (where n is the head number), of the preamplifier to the RDX and RDY outputs is 100.

E WRITE MODE AND WRITE UNSAFE

Write data is sent by the main PCB to the flex circuit via the WDI (write data input) pin on J4. A negative transition on the WDI line changes the direction of the write current in the SSI 521, causing a data transition to be written. (The SSI 521 integrated circuit has a divide-by-two flip-flop internally in the write data path). Write current is selected by three programming resistors on the main PCB, one resistor per SSI 521.

The WUS (write unsafe output) is normally HIGH (unsafe) when in READ or IDLE mode. When a WRITE mode is initiated, WUS goes low after a period of up to 1 microsecond; this indicates a safe condition when in WRITE mode. An unsafe condition exists if any of the following occur:

- the WDI frequency is too low
- there is no write current
- the device is in READ mode
- the chip is disabled

4.3.2 Pulse Detector

The primary function of the pulse detector is to detect "legitimate" peaks of the read-back signal from the head, disk, and preamplifier. A legitimate peak corresponds to a written flux transition on the disk. Other undesired peaks can be caused by noise. The pulse detector must detect these legitimate peaks while preserving the timing associated with them. Each peak is represented by the presence of a narrow pulse on the +ENDATA (encoded data) line, with timing information in the leading edge. This pulse stream, representing encoded data, is ultimately time synchronized by the PLL data separator so that it can be decoded by the encoder/decoder (ENDEC).

The pulse (or peak) detection function is implemented with an 8464 pulse detector integrated circuit.

The following functions are used to achieve the primary purpose of this circuitry as stated above.

NOTE: *Differential signals are denoted by pin pairs.*

A SIGNAL AMPLIFICATION USING AGC

Figure 14, Pulse Detector, shows the preamplified head signal as the input to a gain-controlled amplifier in the 8464 pulse detector. AGC is used to maintain a constant, predetermined signal level at the input to the hysteresis comparator in the 8464 (pins twenty-one and twenty-two).

This is important because a DC voltage level on the SET HYSTERESIS line (pin three) programs a comparator hysteresis which is intended to be a fixed percentage of the average zero-to-peak signal amplitude at the comparator input.

This hysteresis comparator provides the means to amplitude-qualify signal peaks as legitimate. This is illustrated below, in Section 4.3.2 C, Pulse Qualification/Peak Detection.

A gain-control signal for the first amplifier stage is derived from the signal at pins twenty-one and twenty-two by full-wave rectifying that signal, filtering it by means of the AGC capacitor on pin sixteen, and comparing it to a reference level, VREF (voltage reference), at pin four. The VREF thus determines the signal amplitude at pins twenty-one and twenty-two, while the DC level on pin three, SET HYSTERESIS, determines the amplitude qualification level for peak detection. The discharge circuit connected to pin sixteen allows AGC discharge current to flow only when pulses are present at +ENDATA, thereby allowing the graceful detection of address marks without perturbing the AGC loop.

B SIGNAL FILTERING

The amplified read-back signal at pins eighteen and nineteen is processed by a 6.5 megahertz Bessel filter before being input to the differentiator input (pins two and twenty-three). An additional 8 megahertz Bessel filter is placed before the hysteresis comparator (pins twenty-one and twenty-two) to compensate for the additional group delay in the differentiator, as well as some internal delay within the system.

The differentiator network is a two pole Bessel configuration.

C PULSE QUALIFICATION/PEAK DETECTION

Figure 13, Peak Detection, shows pertinent wave forms which are referenced to the pulse detector integrated circuit. The gate channel input signal (to the hysteresis comparator) is shown with the SET HYSTERESIS level on pin three. This is essentially the same wave form that is input to the time channel differentiator stage at pins two and twenty-three. The time differentiated version of this wave form has zero crossings that represent the peaks of the input wave form. These zero crossings are detected by a level comparator which triggers a bidirectional one-shot. The resulting pulses at pins

twelve and thirteen thus have leading edges which carry the timing information of the signal peaks.

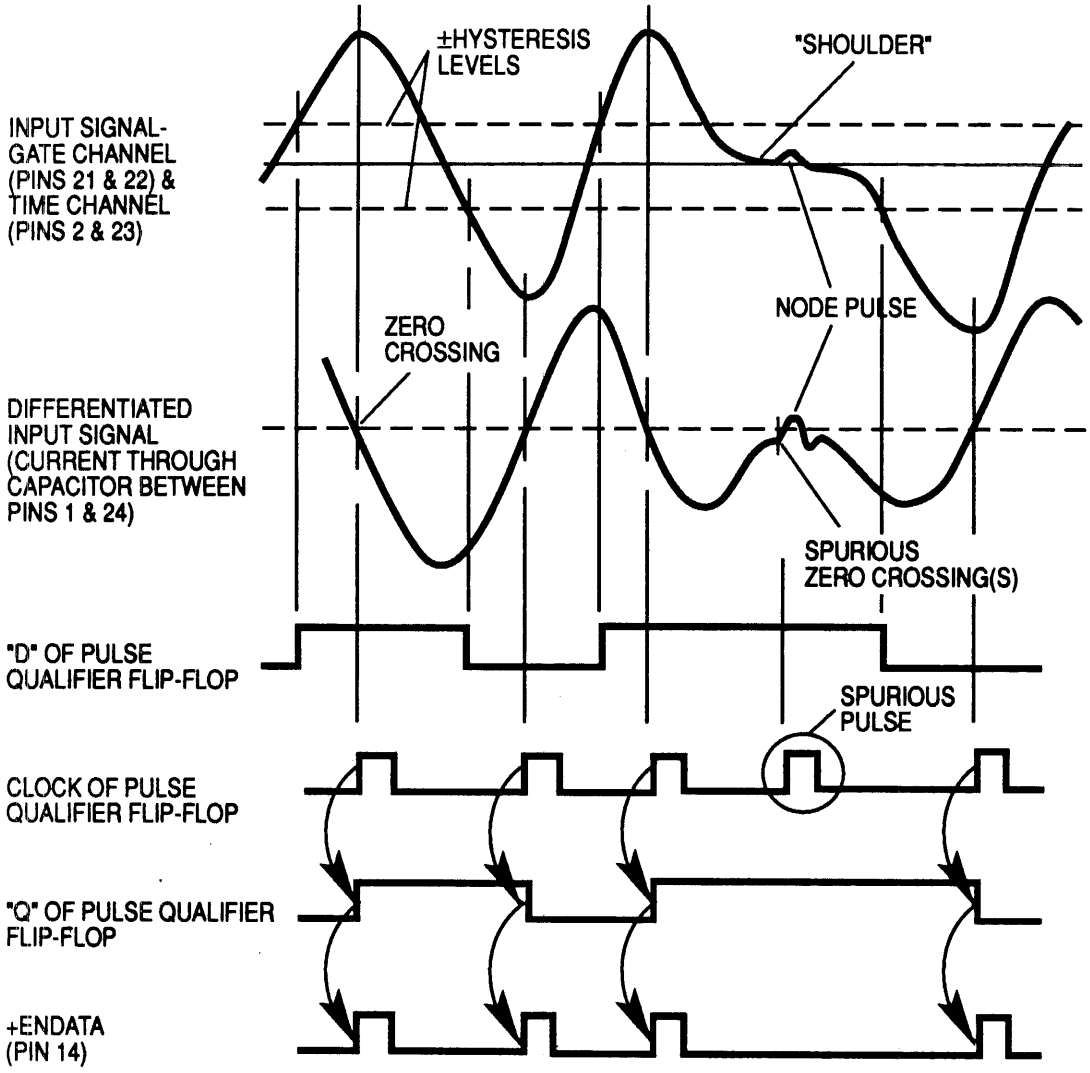


Figure 13
Peak Detection

These clocks toggle the pulse-qualifier flip-flop in the 8464 only if the AMPLITUDE QUALIFICATION signal at pin fifteen (D of the flip-flop) has changed state since the last clock was received. Every flip-flop toggle produces a pulse on pin fourteen (+ENDATA) whose leading edge retains the timing of the corresponding signal peak.

Note that the flip-flop D changes state, and thus qualifies the next flip-flop clock only if the gate channel input signal exceeds the preset hysteresis level.

Note that "shoulders" on the differentiator input produce "droop" on the differentiated output which can generate spurious zero crossing. Figure 13, Peak Detection, illustrates the pulse amplitude qualification.

D WRITE-TO-READ AND HEAD SWITCH RECOVERY

Referring to Figure 14, Pulse Detector, the drive uses a -SQUELCH command, derived in the SLC, which is related to the system WRITE command in the following manner:

- when WRITE is true, -SQUELCH is true (low) and pin eleven is held high, which puts the 8464 in WRITE mode. The 8464 reacts by lowering its internal input impedance at pins eighteen and nineteen, and maintaining the AGC voltage at pin sixteen

- when WRITE is false, -SQUELCH remains true for 5 microseconds and then becomes false. This maintains the reduced input impedance across pins six and seven for the 5 microseconds by virtue of the 8464's internal circuit, as well as an external circuit shown as "squelch net"

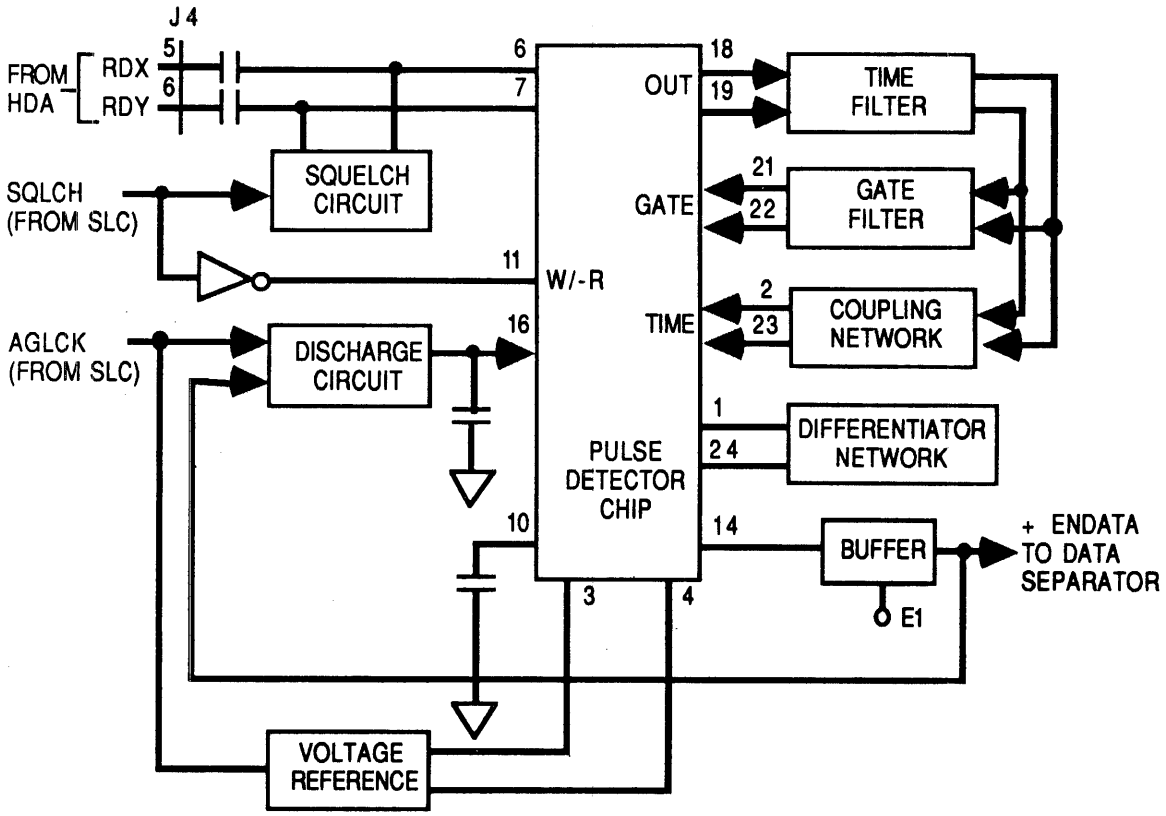


Figure 14
Pulse Detector

When a head switch occurs, -SQUELCH becomes true for 5 microseconds with the same result as described above.

The reduced input impedance during squelch permits the input coupling capacitors to pins six and seven to discharge more quickly after any new DC offset voltage which may be the result of write-to-read mode switching or head switching. If these capacitors are not discharged by the time the next read data comes along, the resulting pin six and seven differential input voltage hinders a read operation.

4.3.3 Clock Recovery and Decoding

The clock recovery and data standardization functions are provided by the DP8459 integrated circuit which receives +ENDATA from the pulse detector. Decoding is provided by the DP8463B ENDEC integrated circuit according to the rules of (2, 7) 1/2 code. Figure 15, ENDEC/Data Separator, READ Mode, illustrates the system in READ mode. The

additional logic in the read gate synchronization block and the data resynchronizer ensures that the data separator/ENDEC combination meets all ESDI specifications.

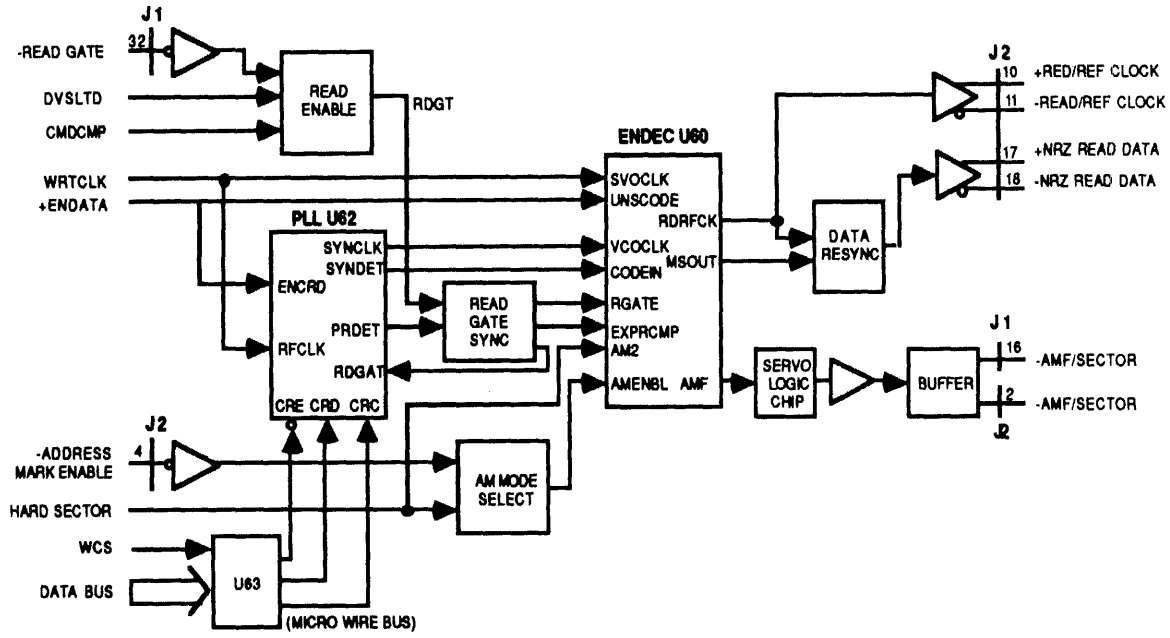


Figure 15
ENDEC/Data Separator READ Mode

A DATA SEPARATOR

The data separator uses a phase-lock loop (PLL) to recover the write clock information from the encoded data stream, +ENDATA. It operates in three modes under control of the read gate synchronization circuits. When not reading or writing (IDLE mode), or when in WRITE mode, the data separator is locked to the write clock from the servo PLL, and operates in a wide band width, phase/frequency mode. This insures proper PLL lock-up, both for phase and frequency. When READ GATE is asserted, RDGAT to the data separator becomes true at the same time, beginning a lock-up sequence; the voltage controlled oscillator (VCO) in the data separator stops and then restarts synchronously with the incoming data stream on +ENDATA, and the phase detector goes into phase only mode. Stopping and restarting the VCO ensures that a relatively low initial phase error occurs so that the lock-up time is well below the time allotted by the 11-byte preamble field. After preamble is detected in the data separator, PRDET becomes true, which reduces the loop gain so that the band width is reduced. Additionally, the PRDET signal is sent to the read gate synchronization logic. The data standardizer in the data separator uses the recovered clock to decide if a +ENDATA pulse has occurred in each window.

The window is nominally 50 nanoseconds wide for 10 megabits per second NRZ data rate. The data standardizer then resynchronizes +ENDATA to the recovered clock, using the window constraint, and sends synchronous data and synchronization clock to the ENDEC.

When -READ GATE becomes false, the RDGAT to the data separator is delayed for about seven write clock periods. This ensures that stopping the VCO does not interfere with the READ/REF clock switch over. The VCO is stopped and then restarted synchronously with write clock to ensure minimal initial phase error. The data separator locks to the write clock in phase/frequency mode and wide band width. After power up, the data separator is initialized through U63 and the microwire bus (National trade mark) on the data separator. This establishes the window centering for the data standardizer in the data separator.

B ENDEC, READ MODE

After the read gate synchronization logic receives a preamble-detected signal from the PLL, along with READ GATE true, it issues RGATE to the ENDEC. The ENDEC then switches the READ/REF clock output from the reference clock (servo PLL write clock) to the PLL derived read clock, with no more than two clock periods missing, and no glitches allowed at the switch over point. Additionally, the read gate synchronization logic sends EXPRCMP to the ENDEC after approximately 500 nanoseconds from the leading edge of RGATE. At this point, the ENDEC has acquired code framing and can decode the (2,7) 1/2 encoded data to NRZ data. The NRZ data at the MSOUT output on the ENDEC is then reclocked with the data resynchronizer before going to the line driver. The RDR-FCK output of the ENDEC is also sent to another line driver which then goes to the ESDI interface. When READ GATE becomes false, RGATE and EXPRCMP to the ENDEC both become false at the same time, but RDGAT to the data separator is delayed for about seven write clock periods. This is to ensure that a proper switch over occurs on the READ/REF clock output of the ENDEC. The switch over from the read clock to the reference clock (write clock) occurs at the same time that -READ GATE (or RGATE at the ENDEC) becomes false.

4.3.4 Write Path and Encoding

Figure 16, Write Path, details the write path. The ENDEC receives NRZ data from the line receivers and encodes it to (2,7) 1/2 code according to the encoding rules, using write clock as the master clock.

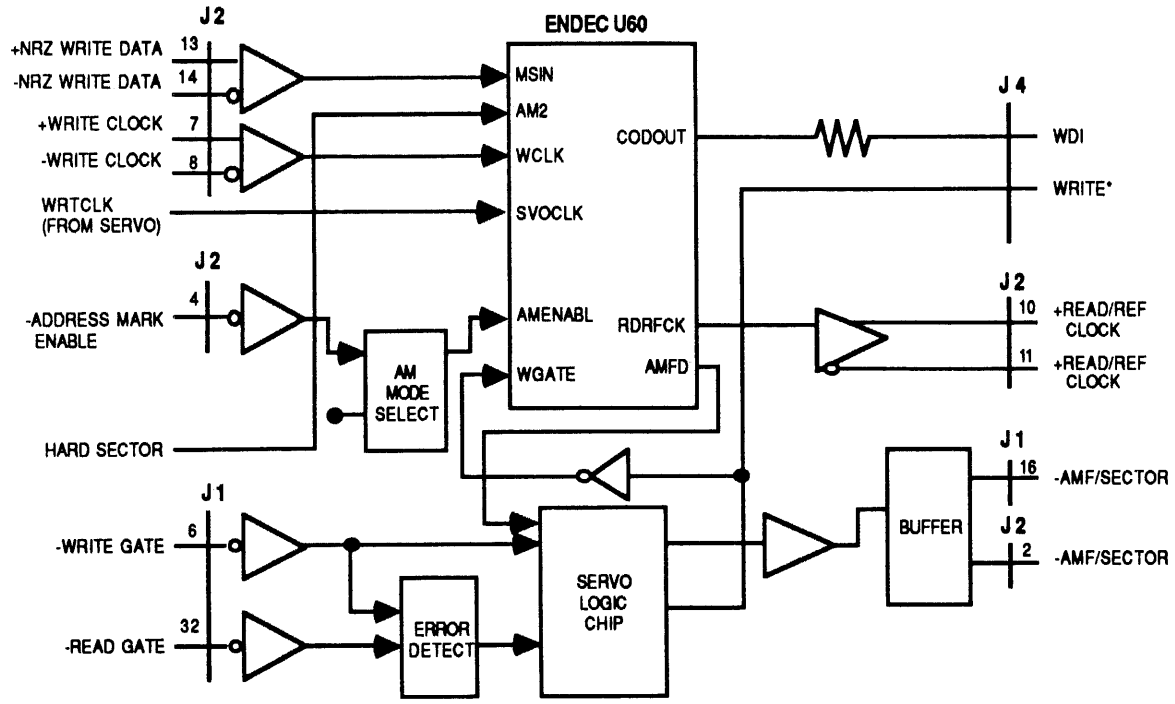


Figure 16
Write Path

A SOFT SECTOR WRITE

When the drive is configured for soft sector operation (JP31 installed), address marks are written on the drive through the -AME (address mark enable) line along with -WRITE GATE. An address mark is a dc erased portion of the track of 3 bytes. When the controller initiates a WRITE in soft sector mode, the -WRITE GATE input becomes true and -AME is enabled at the time an address mark is to be written. The ENDEC does not send pulses out on the WDI lines during this time so that the dc erased mark is written on the disk.

B HARD SECTOR WRITE

When the drive is configured for hard sector operation (JP31 removed), address marks are not written on the disk and the start of a sector is indicated by the drive with the sector mark output. The number of sectors per track is selected by jumpers, or can be configured through the interface if the drive is jumpered for this option. -WRITE GATE again initiates a write operation.

C ENCODING DATA

The NRZ WRITE DATA and WRITE CLOCK from the controller are received by the line receivers on the drive, and are converted to TTL levels before being sent to the ENDEC. The ENDEC then encodes the NRZ data to (2,7) 1/2 code that is sent out of the COD-OUT output of the ENDEC. This then goes to the WDI input of the flex circuit.

D ENCODING RULES

The ENDEC, when in WRITE mode, encodes the NRZ write data using (2, 7) 1/2 encoding rules. The NRZ code is encoded to meet the desired run constraints of no fewer than two, and no more than seven, encoded zeros written between transitions. By doing this, any long runs of NRZ zeros are encoded such that transitions are present for the clock regeneration circuitry (the data separator PLL).

If the code did not place a bound on the longest period between transitions, as with the NRZ data, the data separator would not have any data to lock to, resulting in the data separator losing synchronization over a period of time. Most importantly, the (2, 7) 1/2 code has properties which improve the performance of the read channel.

The period of time between transitions for various (2, 7) 1/2 code lengths can be determined by the following:

(N) $T = (Td/2)(N+1)$ $n = 2, 3, 4, 5, 6, 7$

Where: $N = n + 1$
Td = NRZ data clock period

10 Mbps
Td = 100.00 nanoseconds

(3) T = 150 nanoseconds
(4) T = 200 nanoseconds
(8) T = 400 nanoseconds

For the (2, 7) 1/2 code, (3) T is the shortest period that can be written, also known as Tmin, and (8) T is the longest period that can be written, also known as Tmax.

4.3.5 Address Mark Detection

When a drive has been formatted in soft sector mode, address marks are used to establish the start of sectors. An address mark is a 3-byte dc erased gap written on the track. Interface signals tell the drive to search for an address mark by making -AME true, along

with -DRIVE SELECT. These interface commands are then converted to AME and are sent to the ENDEC input AMENBL. This starts an address mark search within the ENDEC. When the ENDEC detects an address mark, it sends out AMF (address mark found). This signal is then sent out to the SLC which, in turn, sends it to a buffer and then to the interface as -AMF/SECTOR. The SLC controls which signal is sent to the -AMF/SECTOR, depending on whether the drive is jumpered for soft sector (-AMF is output) or hard sector (-SECTOR is output).

After the controller receives the -AMF signal, the controller sets -AME to false. When -AME becomes false, the AMF signal to the SLC becomes false. The address mark has been detected and the controller turns on -READ GATE to the interface. -READ GATE is conditioned, along with -DRIVE SELECT and CMDCMP (command complete), before it is input to the read gate synchronizing block as RDGT. The read process then starts as described above.

5.0 FUNCTIONAL OPERATION

5.1 POWER UP SEQUENCE

DC power (+5 volt and +12 volt) may be supplied to the drive in any order, but +12 volts DC is required to start the spindle motor. The motor power up is controlled by the status of jumper JP6 on the drive electronics PCB assembly. (The location and function of all PCB jumpers are shown in Figure 46, Drive Jumper Options, and Table 26, Jumper Selections.)

If jumper JP6 is open, the spindle power up sequencing is initiated by the issuance of the START MOTOR CONTROL command.

When the spindle reaches full speed, the actuator lock automatically disengages and the heads then recalibrate to track zero. Upon a successful recalibration, READY and COMMAND COMPLETE status signals are true. The unit does not perform any read, write, or seek functions until READY is true. (If after starting, 1,000 revolutions per minute is not reached in ten seconds, an automatic shutdown procedure is initiated; power to the spindle motor is shut off and the drive does not become READY.)

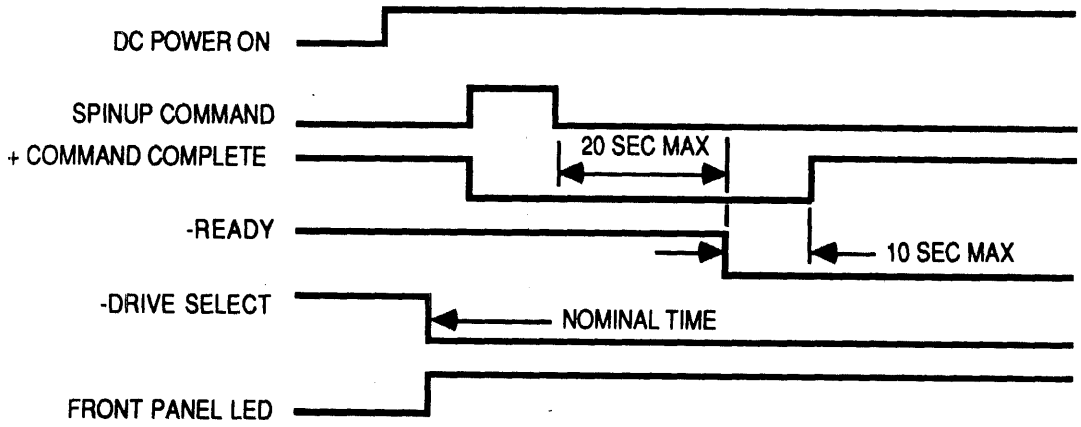


Figure 17
Power Up Sequence (Jumper JP6 Open)

If jumper JP6 is installed, the spindle power up sequencing is initiated by the application of DC power. (When shipped, the JP6 jumper is installed.)

5.2 DRIVE SELECTION

Drive selection occurs when the controller places the address of the drive to be selected on the three drive select lines. See Figure 18, Drive Select Circuit. Only the selected drive responds to the input signals, and only that drive's output signals are then gated to the controller. The details of setting the drive selection jumper are covered in Section 9.1, Drive Address Selection Jumper.

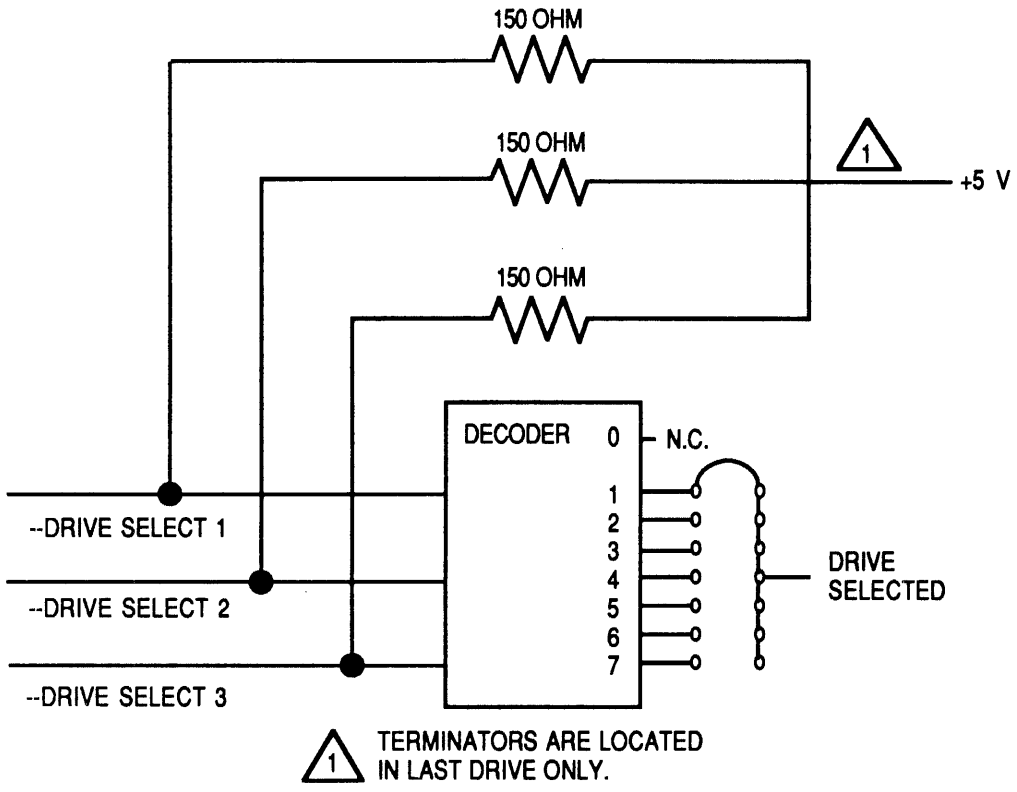


Figure 18
Drive Select Circuit

DRIVE SELECTED	DRIVE SELECT 3	DRIVE SELECT 2	DRIVE SELECT 1
None	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table 8
Drive Selection Matrix

5.3 DRIVE TERMINATION

If more than one **Maxtor** drive is used in a system, the terminator packs (RN13 and RN14) must be removed in all but the last drive in the string. Figure 46, Drive Jumper Options, shows the location of RN13 and RN14.

6.0 ELECTRICAL INTERFACE

The interface to the drive can be divided into four separate categories, each of which is physically separated:

- control signals
- data signals
- DC power
- auxiliary signals

All control lines are digital (open collector transistor-transistor logic (TTL)), and either provide signals to the drive (input) or signals to the host (output) via interface connection J1/P1. The data transfer signals are differential and provide data either to (write) or from (read) the drive via J2/P2.

Figure 19, Control Cable J1/P1 Signals, Table 9, Control Cable J1/P1 Pin Assignments, Figure 20, Data Cable J2/P2 Signals, and Table 10, Data Cable J2/P2 Pin Assignments, show connector pin assignments and interconnection of cabling between the host controller and drives.

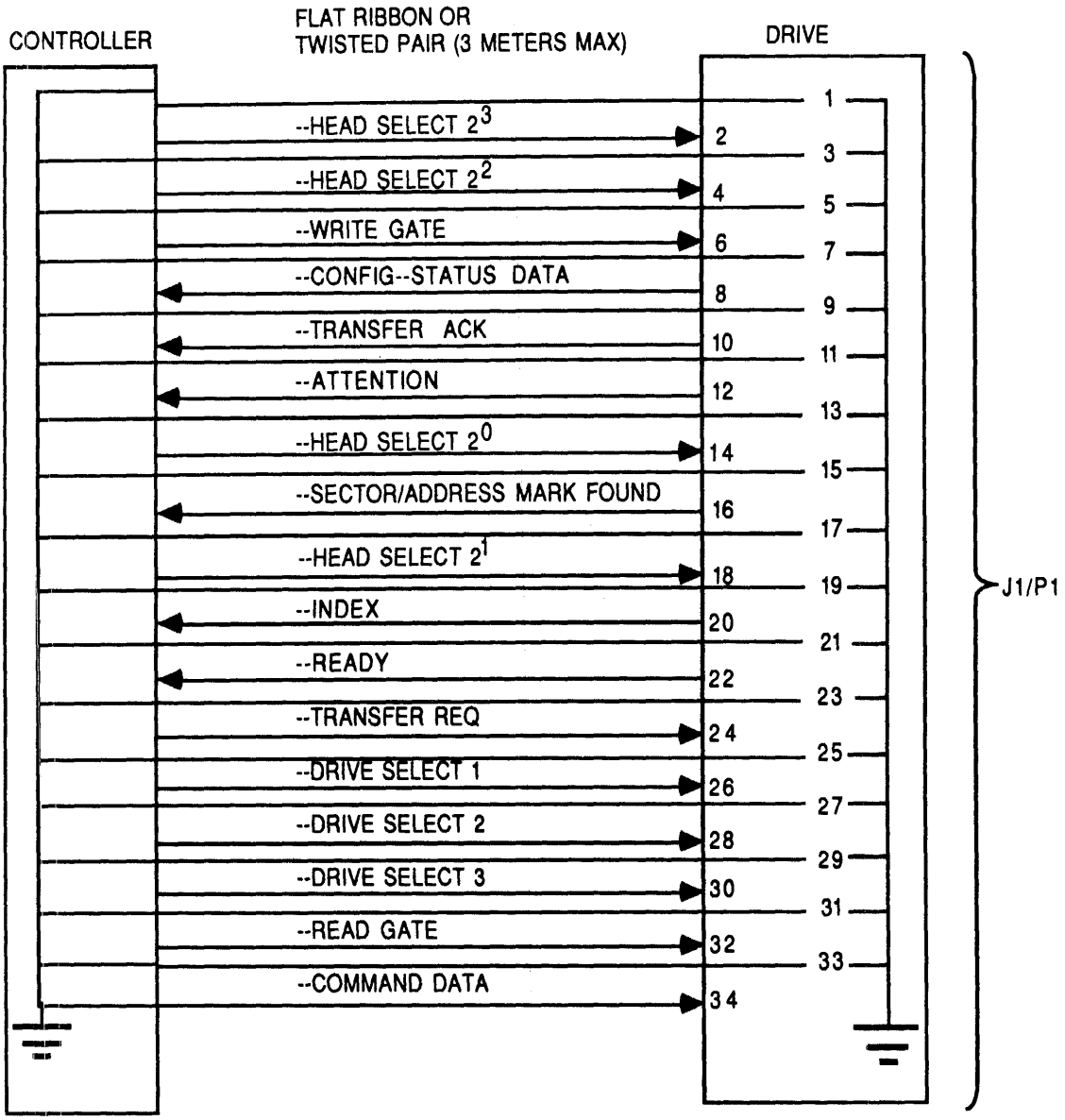


Figure 19
Control Cable J1/P1 Signals

SIGNAL NAME	SIGNAL PIN	GROUND PIN
--HEAD SELECT 2^3	2	1
--HEAD SELECT 2^2	4	3
--WRITE GATE	6	5
--CONFIG-STATUS DATA	8	7
--TRANSFER ACK	10	9
--ATTENTION	12	11
--HEAD SELECT 2^0	14	13
--SECTOR/ADDRESS MARK FOUND	16	15
--HEAD SELECT 2^1	18	17
--INDEX	20	19
--READY	22	21
--TRANSFER REQ	24	23
--DRIVE SELECT 1	26	25
--DRIVE SELECT 2	28	27
--DRIVE SELECT 3	30	29
--READ GATE	32	31
--COMMAND DATA	34	33

Table 9
Control Cable J1/P1 Pin Assignments

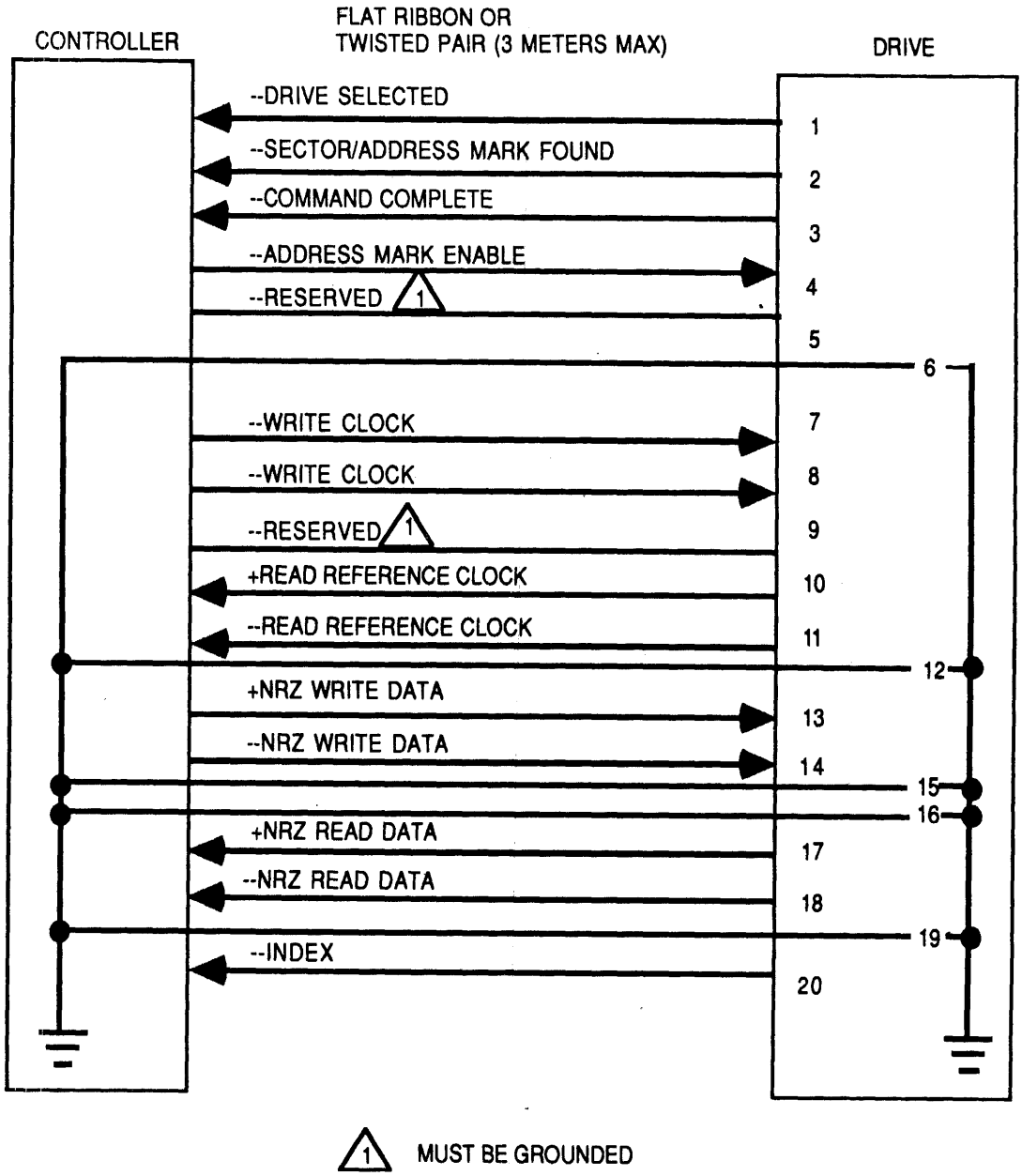
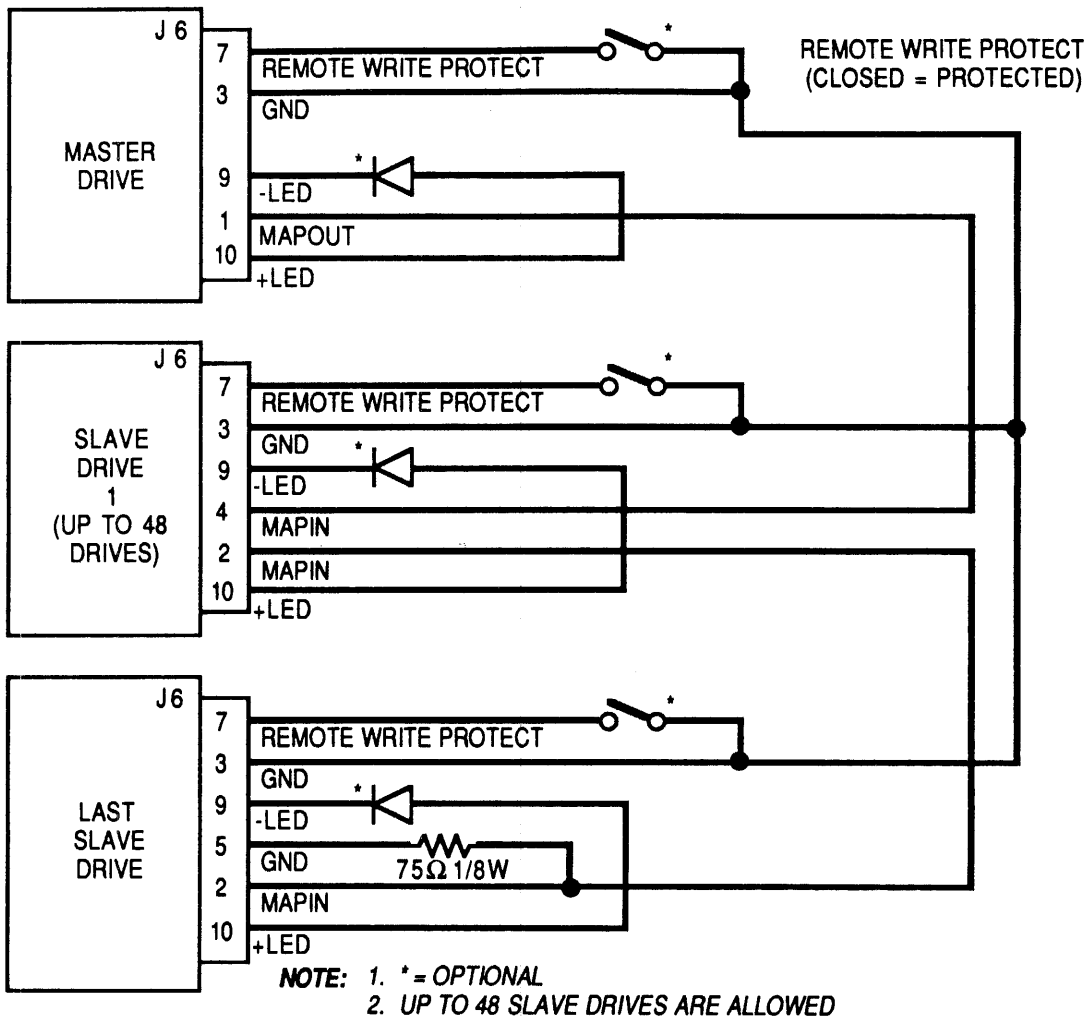


Figure 20
Data Cable J2/P2 Signals

SIGNAL NAME	SIGNAL PIN	GROUND PIN
--DRIVE SELECTED	1	
-SECTOR/ADDRESS MARK FOUND (not gated w/drive select)	2	
--COMMAND COMPLETE	3	
--ADDRESS MARK ENABLE (not gated w/drive select)	4	
--Reserved	5	6
--WRITE CLOCK	7/8	
--Reserved	9	
--READ/REF CLOCK	10/11	12
--NRZ WRITE DATA	13/14	15/16
--NRZ READ DATA	17/18	19
--INDEX (not gated w/drive select)	20	

Table 10
Data Cable J2/P2 Pin Assignments

Figure 21, Typical Auxiliary Cable and Spindle Synchronization Connection, and Table 11, Auxiliary Cable (J6) Pin Assignments, show connector pin assignments, and interconnection of cabling between drives, for the auxiliary signals.



NOTE: *1. * = OPTIONAL*
2. UP TO 48 SLAVE DRIVES ARE ALLOWED
3. THE MAXIMUM LED CURRENT IS 40 mA
4. THE TERMINATOR IS APPLIED AT THE DRIVE CONNECTOR FARTHEST FROM THE MASTER DRIVE

Figure 21
Typical Auxiliary Cable and Spindle Synchronization Connection

SIGNAL NAME	PIN
MAPOUT	1
MAPIN	2
GND	3
MAPIN	4
GND	5
KEY (N.C.)	6
- REMOTE WRITE PROTECT	7
	8
- LED	9
+ LED	10

Table 11
Auxiliary Cable (J6) Pin Assignments

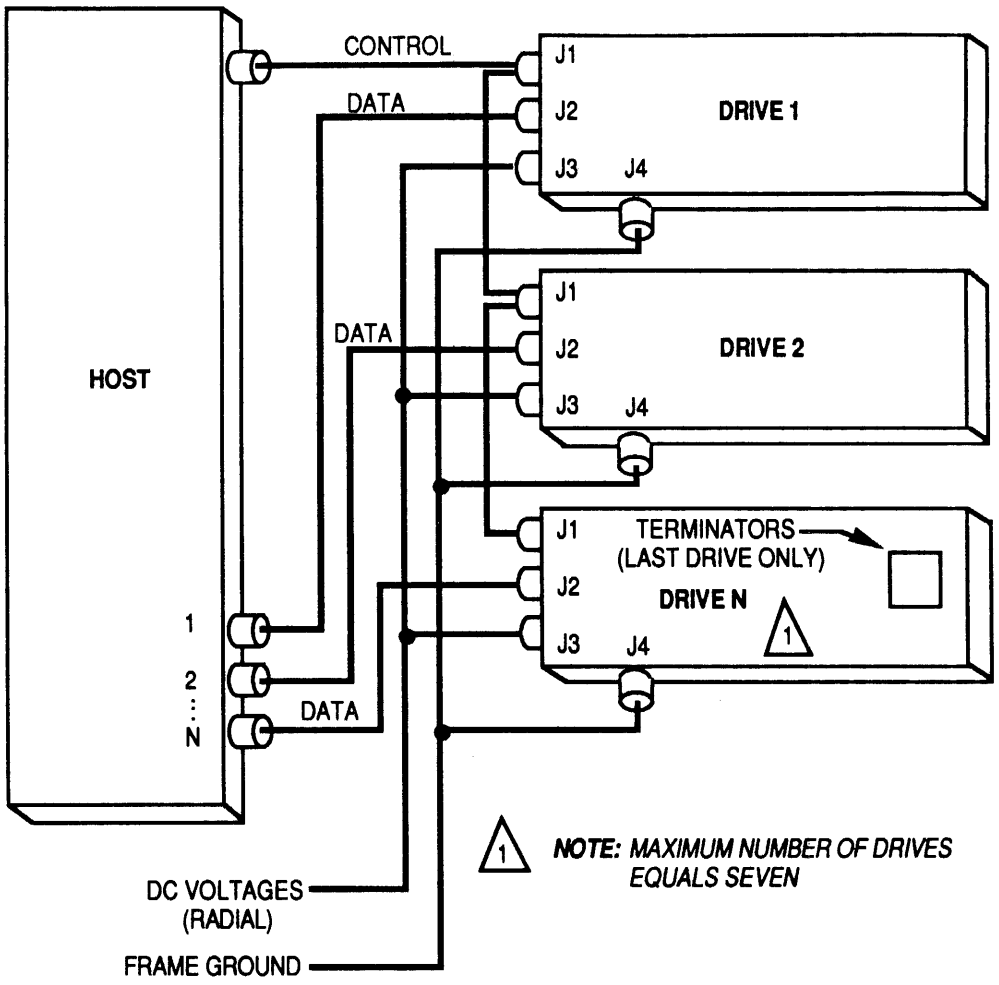


Figure 22
Typical Multidrive Connection

6.1 CONTROL INPUT LINES

The control input signals are one of two types: those to be multiplexed in a multidrive system, and those intended to do the multiplexing. The signals to be multiplexed are WRITE GATE, TRANSFER REQ, and COMMAND DATA. The signals which do the multiplexing are DRIVE SELECT 1, DRIVE SELECT 2, and DRIVE SELECT 3.

The input lines have the following electrical specifications (see Figure 23, Control Signals, Driver/Receiver Combination, for the recommended circuit):

TRUE: 0.0 V DC to 0.4 V DC @ 1 = -48 mA (max)

FALSE: 2.5 V DC to 5.25 V DC @ 0 = +250 µA (open collector)

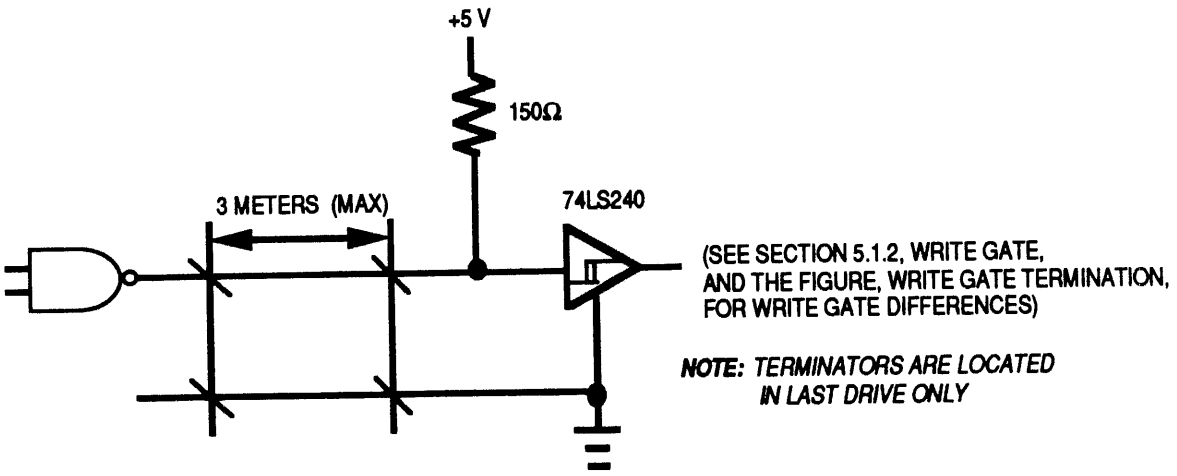


Figure 23
Control Signals, Driver/Receiver Combination

6.1.1 HEAD SELECT 2^0, 2^1, 2^2, and 2^3

The four HEAD SELECT lines allow selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. Data heads are numbered and addressed continuously from zero through the maximum head number. When all HEAD SELECT lines are high (inactive), head zero is selected.

Addressing more heads than contained in the drive results in a write fault when attempting to perform a write operation.

A 150 ohm terminator pack allows for line termination.

6.1.2 WRITE GATE

The active state of this signal, or low level, enables write data to be written on the disk.

The HI to LO transition of this signal creates a write splice and initiates the writing of the data phase-locked oscillator (PLO) synchronization field by the drive. See Figure 24, Soft Sector Address Mark, WRITE GATE, PLO Synchronous Format Timing. When for-

matting, WRITE GATE should be deactivated for 2 bit times minimum between the address area and the data area, to alert the drive to the beginning of the data PLO synchronization field.

***NOTE**: The controller must send zeros during the writing of a PLO synchronization field.*

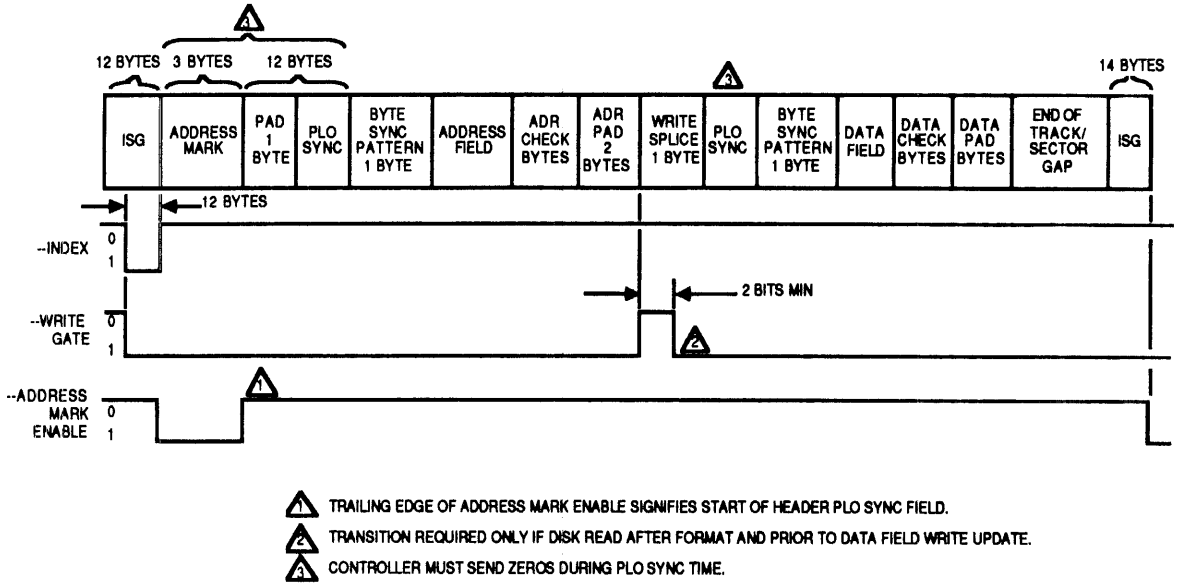
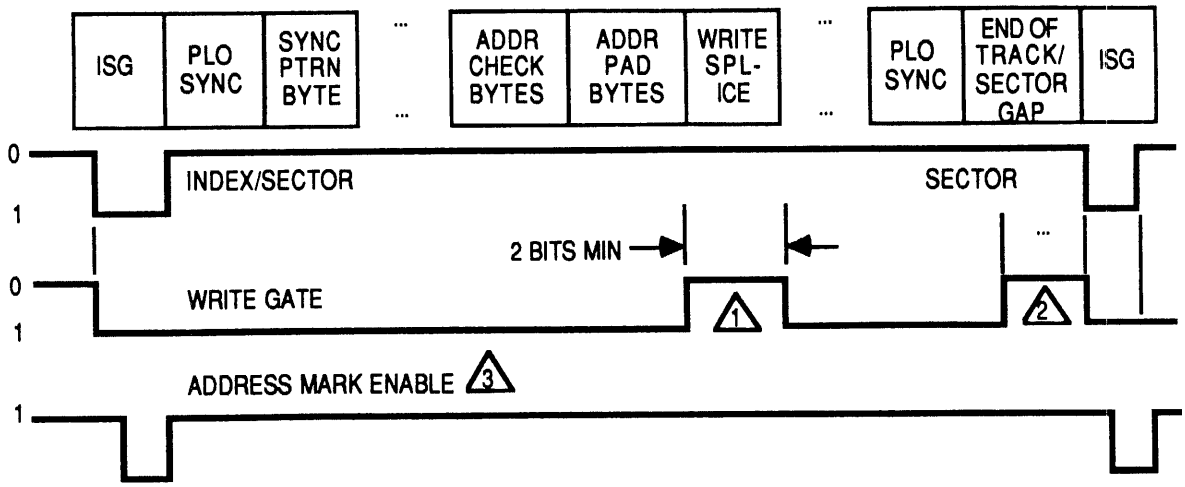


Figure 24
Soft Sector Address Mark, WRITE GATE, PLO Synchronous Format Timing

An alternate format timing in hard sector mode, using the ADDRESS MARK ENABLE signal, is shown in Figure 25, Hard Sector WRITE GATE, PLO Synchronous Format Timing, Using ADDRESS MARK ENABLE.



1. TRANSITION REQUIRED ONLY IF DISK IS READ AFTER FORMAT AND PRIOR TO DATA FIELD WRITE UPDATE

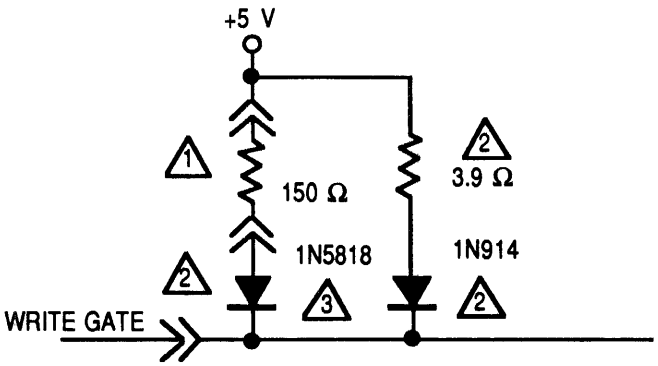
2. CONTROLLER MUST REINITIALIZE TIMING WITH EACH SECTOR RELATIVE TO SECTOR PULSE (NEED NOT NEGATE WRITE GATE)

3. TRAILING EDGE OF ADDRESS MARK ENABLE (1 to 0) SIGNIFIES START OF HEADER PLO SYNC FIELD. DRIVE DOES NOT WRITE ADDRESS MARK ON DISK MEDIUM.

NOTE: *THE USE OF ADDRESS MARK ENABLE ALLOWS WRITING OF AN ADDRESS AREA WITHOUT A WRITE SPLICE IN THE PRECEDING GAP.*

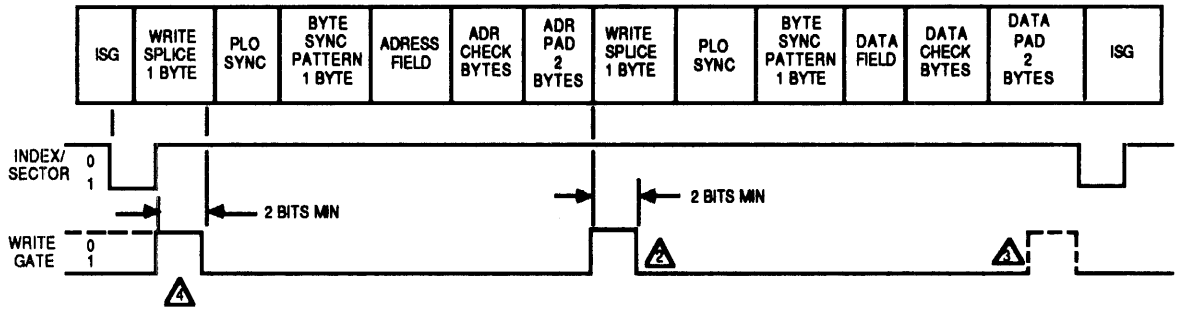
Figure 25
Hard Sector WRITE GATE, PLO Synchronous Format Timing, Using ADDRESS MARK ENABLE

This line is protected from terminator power loss by implementation of the circuit shown in Figure 26, WRITE GATE Termination.



1. PART OF THE TERMINATOR IN THE LAST DRIVE OF THE DAISY CHAIN.
2. PERMANENTLY LOCATED IN THE DRIVE.
3. OR EQUIVALENT PART.

Figure 26
WRITE GATE Termination



1. TRAILING EDGE OF ADDRESS MARK ENABLE (1 TO 0) SIGNIFIES START OF HEADER PLO SYNCHRONIZATION FIELD. DRIVE DOES NOT WRITE ADDRESS MARK ON DISK MEDIUM.
2. TRANSITION REQUIRED ONLY IF DISK IS READ AFTER FORMAT AND PRIOR TO DATA FIELD WRITE UPDATE.
3. CONTROLLER MUST REINITIALIZE TIMING WITH EACH SECTOR PULSE (NEED NOT NEGATE WRITE GATE).
4. LEADING EDGE OF WRITE GATE (0 TO 1) DEFINES A WRITE SPLICE AND START OF A PLO SYNCHRONIZATION FIELD.

Figure 27
Hard Sector WRITE GATE, PLO Synchronous Format Timing

6.1.3 READ GATE

The active state of this signal, or low level, enables data to be read from the disk. This signal should be activated only during a PLO synchronization field and at least 10 bytes prior to the ID, or data synchronization bytes. The PLO synchronization field length is 11 bytes and is indicated by the response to the REQUEST PLO SYNC FIELD LENGTH command. Read gate must be deactivated when passing over a write splice area.

A 150 ohm terminator pack allows for line termination.

6.1.4 COMMAND DATA

When presenting a command, sixteen information bits of serial data, plus parity, are presented on this line. This data is to be controlled by the handshake protocol with signals TRANSFER REQ and TRANSFER ACK (see Figure 33, Typical Serial Operation(s)). Upon receipt of this serial data, the drive performs the required function, as specified by the bit configuration. Data is transmitted most significant byte first. See Table 12, COMMAND DATA Definition, for the meaning of the various bit combinations. See Figure 28, One Bit Transfer Timing—To Drive, for timing. Odd parity must be maintained. (The number of bits set to one in a command, including parity, must be odd.)

No communications should be attempted unless the COMMAND COMPLETE line is true.

Reading and writing are inhibited during the execution of commands.

NOTE: *The COMMAND DATA line must be at a logic zero when not in use.*

A 150 ohm resistor pack allows for line termination.

CMD FUNCTION BIT 15 14 13 12	CMD FUNCTION DEFINITION	CMD MODIFIER APPLICABLE (BITS 11-8)	CMD PARAMETER APPLICABLE (BITS 11-0)	STATUS CONFIGURATION DATA RETURNED TO CONTROLLER
0 0 0 0	Seek	No	Yes	No
0 0 0 1	Recalibrate	No	No	No
0 0 1 0	Request Status	Yes	No	Yes
0 0 1 1	Request Configuration	Yes	No	Yes
0 1 0 0	Reserved	-	-	-
0 1 0 1	Control	Yes	No	No
0 1 1 0	Reserved	-	-	-
0 1 1 1	Track Offset	Yes	No	No
1 0 0 0	Initiate Diagnostics	No	No	No
1 0 0 1	Set Byte per Sector	No	Yes	No
1 0 1 0	Reserved	-	-	-
1 0 1 1	Reserved	-	-	-
1 1 0 0	Reserved	-	-	-
1 1 0 1	Reserved	-	-	-
1 1 1 0	Reserved	-	-	-
1 1 1 1	Reserved	-	-	-

NOTES: 1. All unused or not applicable lower order bits must be zero.
2. Any reserved or command function received is treated as an invalid command.

Table 12
COMMAND DATA Definition

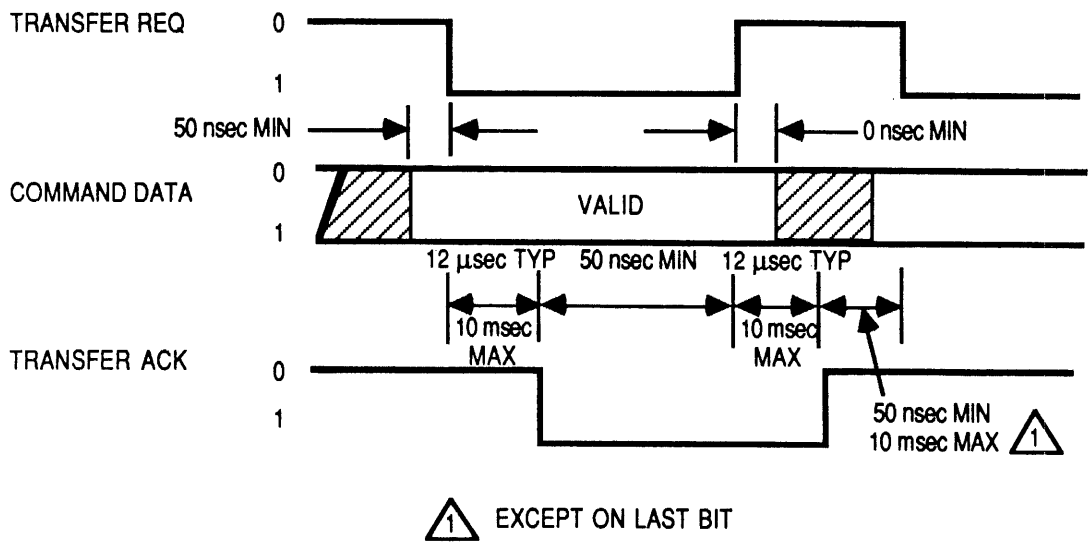


Figure 28
One Bit Transfer Timing—To Drive

See Figure 29, COMMAND DATA Word Structure, for a diagram of the COMMAND DATA bytes.

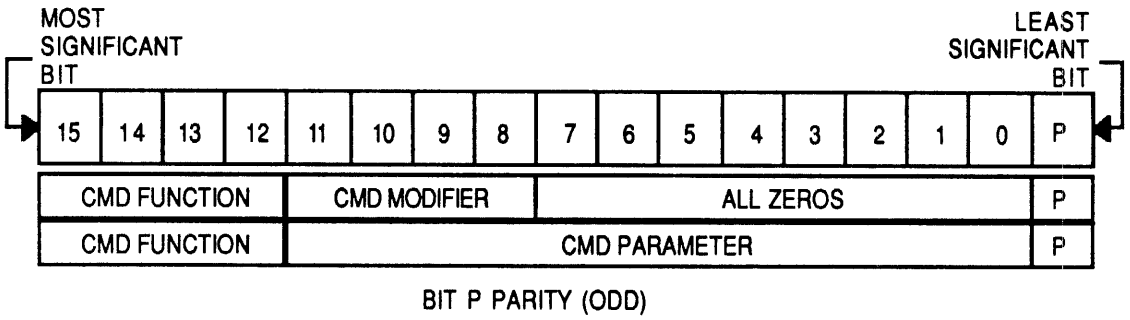


Figure 29
COMMAND DATA Word Structure

SEEK (0000): This command causes the drive to seek to the cylinder indicated in bits eleven through zero. A SEEK command restores track offsets to zero.

RECALIBRATE (0001): This command causes the actuator to return to cylinder 0000. A RECALIBRATE command restores track offsets to zero.

REQUEST STATUS (0010): This command causes the drive to send 16 bits (see Table 16, TRACK OFFSET Command Modifier Bits) of standard status information to the controller, as determined by the command modifier bits.

When the command modifier bits (11-8) of the REQUEST STATUS command are 0000, the drive responds with 16 bits of standard status. See Table 13, REQUEST STATUS Modifier Bits. Bits fifteen through twelve of this status are defined as state bits which do not cause ATTENTION to be asserted. Bits eleven through zero of this status are fault, or change of status, bits that cause ATTENTION to be asserted each time one is set.

When the command modifier bits (11-8) of the REQUEST STATUS command are 0001 through 0111, the drive responds with the vendor unique status. The number of vendor unique status words is specified by the configuration data.

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	Request Standard Status
0	X	X	X	Request Vendor Unique Status
1	X	X	X	Reserved

Table 13
REQUEST STATUS Modifier Bits

REQUEST CONFIGURATION (0011): This command causes the drive to send 16 bits of configuration data to the controller. The specific configuration requested is specified by bits eleven through eight of the command, as shown in Table 14, REQUEST CONFIGURATION Modifier Bits. Furthermore, the drive responds to the subscripted command, REQUEST FOR CONFIGURATION with Are synchronized spindles configured? (0011 0000 0000 0001). The response is 1000 0000 0000 0000 (Yes) or 0000 0000 0000 0000 (No).

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	General Configuration of Drive and Format
0	0	0	1	Number of Cylinders
0	0	1	0	Reserved
0	0	1	1	Number of Heads
0	1	0	0	Minimum Unformatted Bytes per Track
0	1	0	1	Number of Unformatted Bytes per Sector (hard sector)
0	1	1	0	Number of Sectors per Track (hard sector)
0	1	1	1	Minimum Bytes in ISG Field
1	0	0	0	Minimum Bytes per PLO Synchronization Field
1	0	0	1	Number of Words of Vendor Unique Status Available
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table 14
REQUEST CONFIGURATION Modifier Bits

CONTROL (0101): This command causes the control operations specified by bits eleven through eight to be performed as described in Table 15, CONTROL Command Modifier Bits.

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	Reset Interface Attention and Standard Status
0	0	0	1	Reserved
0	0	1	0	Stop Motor (when jumper J6 not installed)
0	0	1	1	Start Motor (when jumper J6 not installed)
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	X	X	X	Reserved

Table 15
CONTROL Command Modifier Bits

TRACK OFFSET (0111): This command causes the drive to perform a track offset in the direction and amount specified by bits eleven through eight, as outlined in Table 16,

TRACK OFFSET Command Modifier Bits. Each offset value is 5% of the track width. SEEK and RECALIBRATE commands restore track offsets to zero.

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	Restore Offset to Zero
0	0	0	1	Restore Offset to Zero
0	0	1	0	Positive Offset One
0	0	1	1	Negative Offset One
0	1	0	0	Positive Offset Two
0	1	0	1	Negative Offset Two
0	1	1	0	Positive Offset Three
0	1	1	1	Negative Offset Three
1	X	X	X	Reserved

Table 16
TRACK OFFSET Command Modifier Bits

INITIATE DIAGNOSTICS (1000): This command causes the drive to perform 10,000 random seeks as a diagnostic aid. Successful completion of the diagnostics is indicated by COMMAND COMPLETE with no ATTENTION.

SET UNFORMATTED BYTES PER SECTOR (1001): This optional command causes the drive to set the number of unformatted bytes per sector indicated in bits eleven through zero (if implemented). This command is valid only if the drive is configured in the hard sectored mode and jumper JP30 is installed.

6.1.5 TRANSFER REQ

This line functions as a handshake signal, in conjunction with TRANSFER ACK, during command and configuration/status transfers. See Figure 28, One Bit Transfer Timing—To Drive, and Figure 30, One Bit Transfer Timing—From Drive, for timing. The transfer speed (one complete handshake) takes typically 11.76 microseconds per bit. Longer times may be experienced depending on the overhead experienced at the controller.

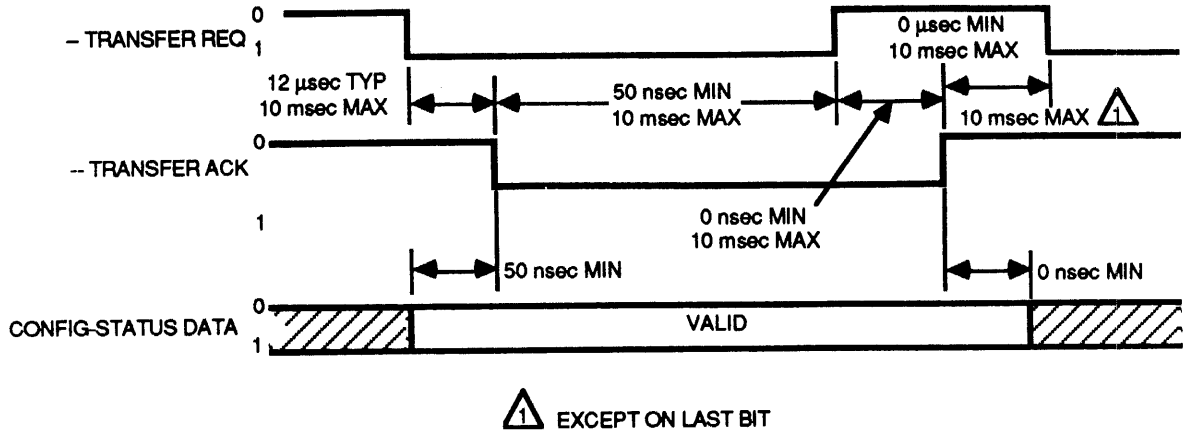


Figure 30
One Bit Transfer Timing—From Drive

6.1.6 ADDRESS MARK ENABLE

A **SOFT SECTOR MODE ONLY**

This signal, when active with WRITE GATE, causes an address mark to be written. ADDRESS MARK ENABLE is active for 24 bit times. See Figure 31, Write Address Mark Timing.

ADDRESS MARK ENABLE, when active without WRITE GATE or READ GATE, causes a search for address marks.

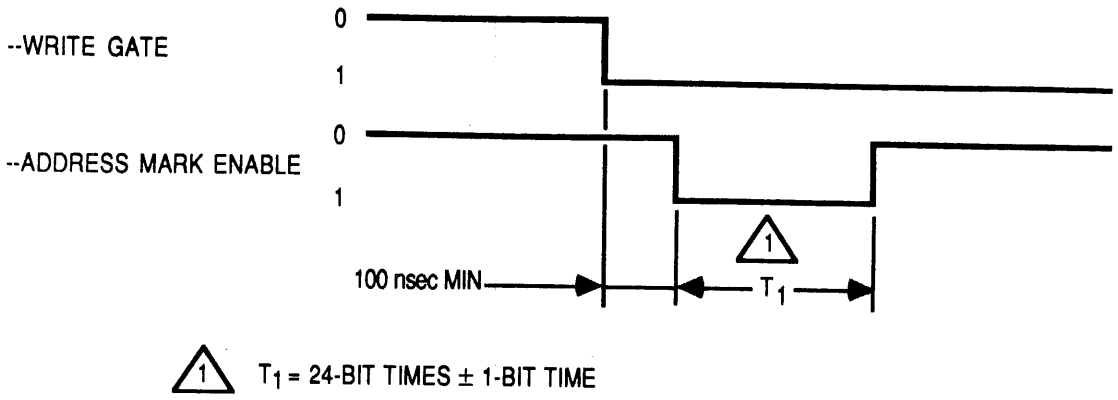


Figure 31
Write Address Mark Timing

B **HARD AND SOFT SECTOR MODES**

If WRITE GATE is true, the LO to HI transition, or deassertion of ADDRESS MARK ENABLE, causes the drive to begin writing the ID PLO synchronization field. See Figure 24, Soft Sector Address Mark, WRITE GATE, PLO Synchronous Format Timing. The controller must send zeros during the writing of the PLO synchronization field.

A 150 ohm terminator pack allows for line termination.

6.2 CONTROL OUTPUT LINES

The output control signals are driven with an open collector output stage capable of sinking a maximum of 48 milliamps at low level, or true state, with maximum voltage of 0.4 volts, measured at the driver. When the line driver is in the high level, or false state, the driver transistor is off and collector leakage current is a maximum of 250 microamps.

All J1 output lines are enabled by the drive select decoder.

Figure 23, Control Signals, Driver/Receiver Combination, shows the recommended circuit.

6.2.1 DRIVE SELECTED

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive. The DRIVE SELECTED line is driven by a TTL open collector driver,

as shown in Figure 23, Control Signals, Driver/Receiver Combination. This signal goes active only when the drive is selected, as defined in Section 5.2, Drive Selection. The DRIVE SELECT lines at J1/P1 are activated by the host system.

6.2.2 READY

This signal indicates that the spindle is up to speed. This interface signal, when true, together with COMMAND COMPLETE, indicates that the drive is ready to read, write, or seek. When the line is false, all writing and seeking is inhibited.

6.2.3 CONFIG-STATUS DATA

The drive presents serial data on this line upon request from the controller. See Figure 33, Typical Serial Operation(s), for typical operation. CONFIG-STATUS serial data is presented to the interface and transferred using the handshake protocol with signals TRANSFER REQ and TRANSFER ACK; see Figure 30, One bit Transfer Timing—From Drive. Once initiated, 16 bits, plus parity, are transmitted, most significant byte first. Odd parity is maintained.

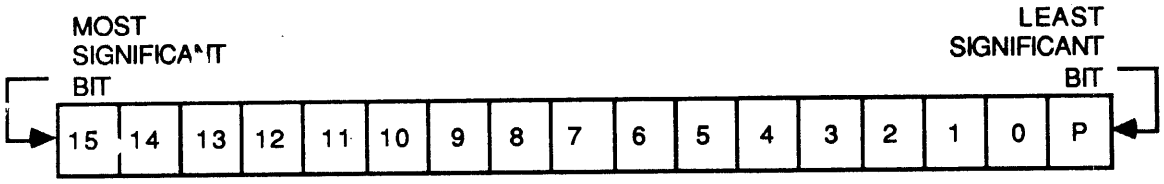
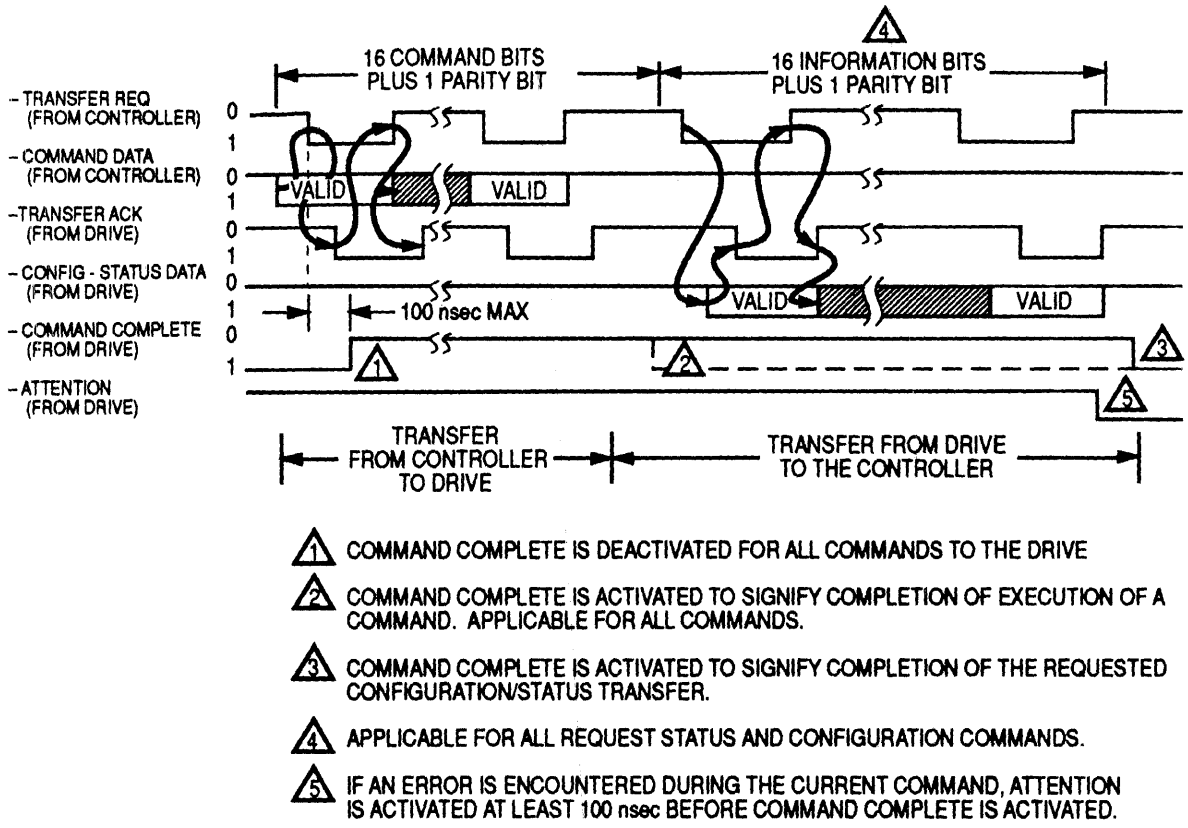


Figure 32
CONFIG-STATUS DATA Word Structure



1. COMMAND COMPLETE IS DEACTIVATED FOR ALL COMMANDS TO THE DRIVE
2. COMMAND COMPLETE IS ACTIVATED TO SIGNIFY COMPLETION OF EXECUTION OF A COMMAND. APPLICABLE FOR ALL COMMANDS.
3. COMMAND COMPLETE IS ACTIVATED TO SIGNIFY COMPLETION OF THE REQUESTED CONFIGURATION/STATUS TRANSFER.
4. APPLICABLE FOR ALL REQUEST STATUS AND CONFIGURATION COMMANDS.
5. IF AN ERROR IS ENCOUNTERED DURING THE CURRENT COMMAND, ATTENTION IS ACTIVATED AT LEAST 100 nsec BEFORE COMMAND COMPLETE IS ACTIVATED.

Figure 33
Typical Serial Operation(s)

In response to the REQUEST STATUS command, 16 bits of status information is returned to the controller. Odd parity is maintained.

If the command modifier bits (eleven through eight) are 0000, the standard status information is returned (see Table 17, Standard Status Response Bits).

BIT POSITION	BIT VALUE	FUNCTION
15	0	Reserved
14	0	Reserved
13	0	Reserved
12	C	Write Protected, Fixed Medium
11	C	Spindle Synchronized (multiple spindles)
10	0	Reserved
9	C	Spindle Motor Stopped by STOP Command
8	C	POWER ON RESET Conditions Exist
7	C	COMMAND DATA Parity Fault
6	C	Interface Fault
5	C	Invalid or Unimplemented Command Fault
4	C	SEEK Fault
3	C	WRITE GATE with TRACK OFFSET Fault
2	C	Vendor Unique Status Available
1	C	WRITE Fault
0	0	Reserved

C = Condition Dependent

Table 17
Standard Status Response Bits

Bits fifteen through twelve of the status are defined as state bits, which do not cause ATTENTION to be asserted. Bits eleven through zero are fault, or change of status, bits which cause ATTENTION to be asserted.

Conditions that can cause WRITE FAULT are:

- write current in a head without WRITE GATE active or no write current with WRITE GATE active and the drive selected
- writing before a COMMAND COMPLETE signal is received
- writing while the head is off track
- having DC voltages grossly out of tolerance
- having WRITE GATE active to a write protected drive
- having nonzero data during a PLO synchronization field write
- simultaneously activating READ GATE and WRITE GATE

If the command modifier bits (eleven through eight) are used, the vendor unique status information shown in Table 18, Vendor Unique Status Response Bits.

BIT POSTION	BIT VALUE	FUNCTION
15	C	Motor Status
14	C	
13	C	
12	C	
11	C	Motor Synchronization
10	C	Unable to Read Configuration Data
9	C	SEEK Calibration Failure
8	C	Head Offset Out of Tolerance
7	C	Multiple Preamplifiers Selected
6	C	WRITE GATE without COMMAND COMPLETE
5	C	WRITE GATE without Offtrack
4	C	Write to Protected Drive
3	C	Preamplifier Write Unsafe
2	C	READ GATE Before AMF
1	C	Nonzero Data During PLO Write
0	C	Simultaneous READ and WRITE GATE

C = Condition Dependent WORD 1

BIT POSTION	BIT VALUE	FUNCTION
15	0	Reserved
14	1	XT-4000E
13	C	SEEK Calibration Error Code
12	C	SEEK Calibration Error Code
11	C	Number of Heads
10	C	
9	C	
8	C	
7	C	Servo Writer Version
6	C	
5	C	
4	C	
3	C	
2	C	
1	C	
0	C	

C = Condition Dependent WORD 2

Table 18
Vendor Unique Status Response Bits

BIT POSITION				FUNCTION
15	14	13	12	
BIT VALUES				
0	0	0	0	Normal Run Mode
0	0	0	1	Bad Spindle Position Sensor
0	0	1	0	Reserved
0	0	1	1	Excessive Time to 1,000 rpm
0	1	0	0	Excessive Time to 3,000 rpm
0	1	0	1	Cannot Lock to Speed
0	1	1	0	Abnormal Accel/Decel Condition at Start
0	1	1	1	Motor Running at Wrong Speed
1	0	0	0	Normal Run Mode with Locked Spindle, Synchronized Feature Active
1	0	0	1	Locked Spindle Feature Active Spindle Not Synchronized
1	0	1	0	Locked Spindle Synchronization Lost
1	0	1	1	Spindle Stuck
1	1	0	0	Reserved
1	1	0	1	Locked Spindle Sync Up Mode Active
1	1	1	0	Locked Spindle Feature Active, but No MAPIN Pulse Provided for Synchronization
1	1	1	1	Reserved

Table 19
Motor Status

The SEEK calibration error portion of word two is only valid with bit nine of word one set. With this bit set, the error code is interpreted as in Table 20, SEEK Calibration Error Code.

BIT POSITION		FUNCTION
13	12	
BIT VALUES		
0	0	SEEK Error During Calibration
0	1	SEEK Calibration Time Excessive
1	0	Torque Profile Error
1	1	Head Calibration Error

Table 20
SEEK Calibration Error Code

BIT POSITION	BIT VALUE	FUNCTION
15	0	Magnetic Disk Drive
14	0	End of Track/Sector Gap
13	1	Track Offset Option Available
12	0	Reserved
11	0	Reserved
10	0	Reserved
9	1	Transfer Rate > 5 MHz or ≤ 10 MHz
8	0	Reserved
7	0	Reserved
6	1	Fixed Drive
5	P	Spindle Motor Control Option Implemented
4	0	Reserved
3	1	RLL Encoded (not MFM)
2	P	Soft Sectored (address mark)
1	P	Hard Sectored (sector mark)
0	1	Spindle Synchronization Subscripted Configuration Supported

P = Programmable

Table 21
General Configuration Response Bits

The motor status portion of word one of the vendor unique response is translated as in Table 22, Specific Configuration Response Bits.

COMMAND MODIFIER BITS				CONFIGURATION RESPONSE	VALUE
11	10	9	8		
0	0	0	1	Number of Cylinders, Fixed	1,224
0	0	1	0	Number of Cylinders, Removable	0
0	0	1	1	Number of Heads, Bits 7-0	7 or 15
0	1	0	0	Minimum Unformatted Bytes per Track	20,940
0	1	0	1	Number of Unformatted Bytes per Sector (hard sector)	P
0	1	1	0	Number of Sectors per Track (hard sector)	P
0	1	1	1	Minimum Bytes in ISG Field (not including intersector speed tolerance)	-
				Bits 15-8: ISG Types After Index	12
				Bits 7-0: Bytes per ISG Field	14
1	0	0	0	Minimum Bytes per PLO Synchronization Field	
				Bits 7-0: Bytes per PLO Synchronization Field	11
1	0	0	1	Number of Words of Vendor Unique Status Available	2
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Reserved	
1	1	0	1	Reserved	
1	1	1	0	Reserved	
1	1	1	1	Reserved	

P = Programmable

Table 22
Specific Configuration Response Bits

6.2.4 TRANSFER ACK

This signal functions as a handshake signal, along with TRANSFER REQ, during command and configuration-status transfers. See Figure 28, One Bit Transfer Timing—To Drive, and Figure 30, One Bit Transfer Timing—From Drive.

6.2.5 ATTENTION

This output is asserted when the drive wants the controller to request its standard status. Generally, this is a result of a fault condition or a change of status. Writing is inhibited when ATTENTION is asserted. ATTENTION is deactivated by the reset interface attention command modifier, under the CONTROL command (see Section 6.1.4, COMMAND DATA).

6.2.6 INDEX

This pulse is provided by the drive once each revolution to indicate the beginning of a track. Normally, this signal is high and makes the transition to low to indicate INDEX. Only the transition at the leading edge of the signal is reciprocal of the rotational speed (see Figure 34, INDEX Timing). This signal is available on the command cable J1/P1 (gated) and on the data cable J2/P2 (ungated).

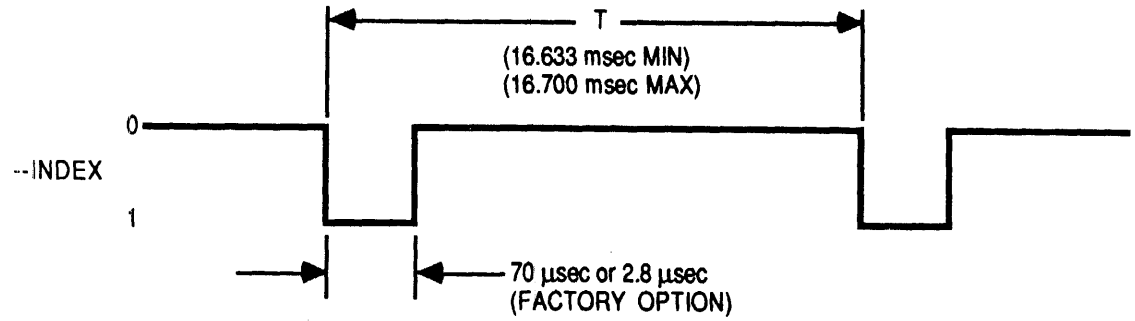
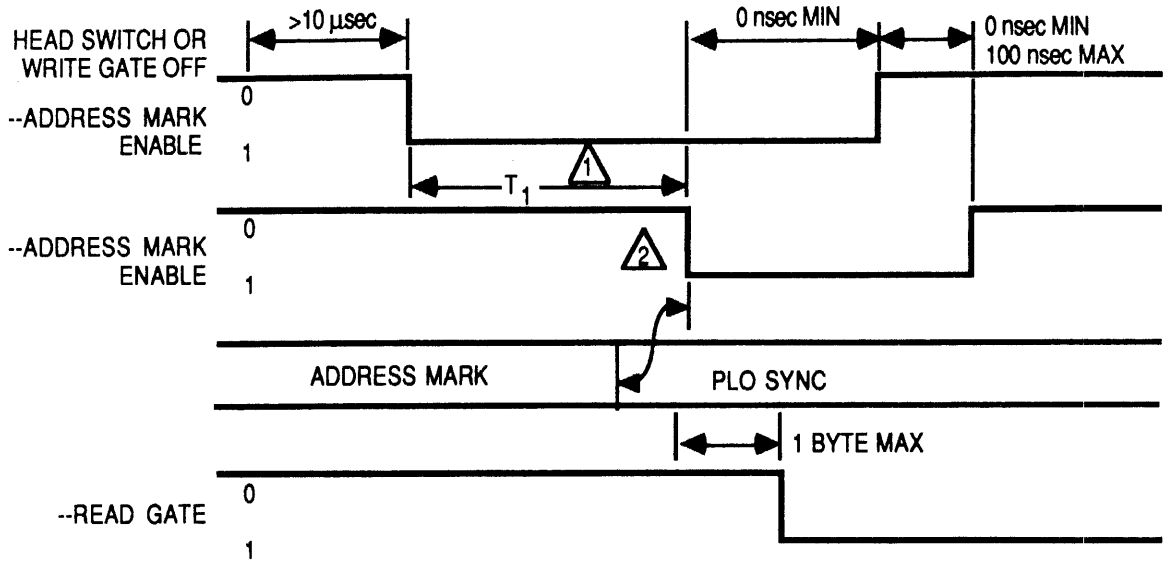


Figure 34
INDEX Timing

6.2.7 ADDRESS MARK FOUND (Soft Sector)

This signal indicates the detection of the end of an address mark. See Figure 35, Read Address Mark Timing (Hard Sector), for timing.



1 T_1 = 16 BIT TIMES MINIMUM

2 LEADING EDGE INDICATES THE LOCATION OF THE END OF AN ADDRESS MARK

Figure 35
Read Address Mark Timing (Hard Sector)

6.2.8 SECTOR MARK (Hard Sector)

This optional interface signal indicates the start of a sector. No short sectors are allowed. The leading edge of the asserted sector pulse is the only edge that is accurately controlled. The INDEX pulse indicates sector zero. See Figure 36, Sector Pulse Timing (Hard Sector).

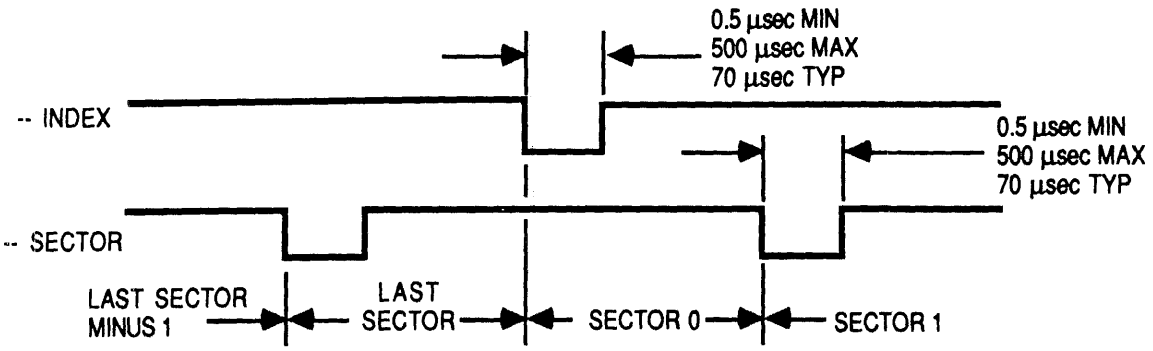


Figure 36
Sector Pulse Timing (Hard Sector)

6.2.9 COMMAND COMPLETE

COMMAND COMPLETE is a status line provided at the J2/P2 connector. This is an ungated output from the drive, which allows the host to monitor the drive's COMMAND COMPLETE status during overlapped commands, without selecting the drive. This signal line goes false in the following cases:

- a recalibration sequence is initiated (by drive logic) at power on if the read/write heads are not over track zero
- the signal line goes false upon receipt of the first COMMAND DATA bit. COMMAND COMPLETE stays false during the entire command sequence

This signal is driven by an open collector driver, as shown in Figure 23, Control Signals, Driver/Receiver Combination.

6.3 SPINDLE SYNCHRONIZATION CONTROL OPTION

This feature allows up to forty-eight drives to synchronize the angular position of their spindles such that their INDEX signals line up to within +20 microseconds of the leading edge of the INDEX signal on the master drive. In the absence of a MAPIN signal, the drive synchronizes to its internal clock. The drive indexes lead the leading edge of MAPIN by 215 milliseconds (typical). The MAPIN signal is derived from either an external 60 hertz signal, or from the MAPOUT signal available on J6 from one drive defined as the master drive.

MAPOUT is a TTL signal at 60 hertz with a pulse width of 20 microseconds.

The light-emitting diode (LED) output on J6 is an optional drive selected signal that is available for use in systems that cannot use the LED on the faceplate.

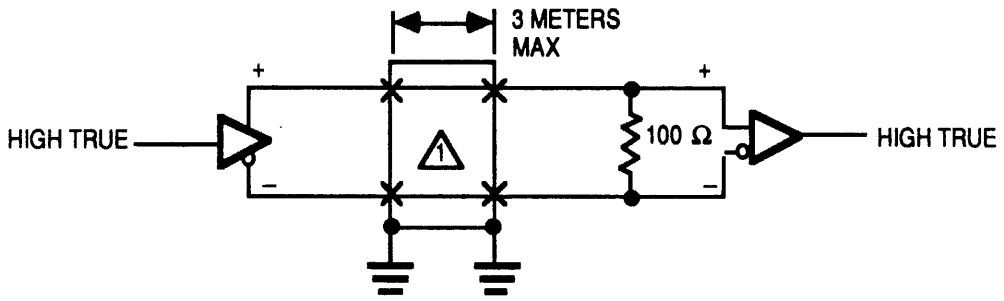
The remote write protect input allows the drive to be write protected via the J6 connector. The active state of this signal, or low level, prohibits data from being written to the drive.

See Figure 21, Typical Auxiliary Cable and Spindle Synchronization Connection, for a typical configuration.

6.4 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host system are differential, and are not multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Four pairs of balanced signals are used for the transfer of data and clock: NRZ WRITE DATA, NRZ READ DATA, WRITE CLOCK, and READ/REFERENCE CLOCK. Figure 37, Data Line Driver/Receiver Combination, illustrates the recommended driver/receiver circuit.



Z = 105 Ω FLAT RIBBON OR TWISTED PAIR
ANY DRIVER AND RECEIVER WHICH COMPLIES WITH
EIA STANDARD RS-422 MEETS THESE REQUIREMENTS.

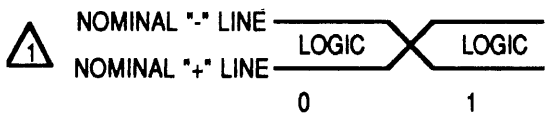


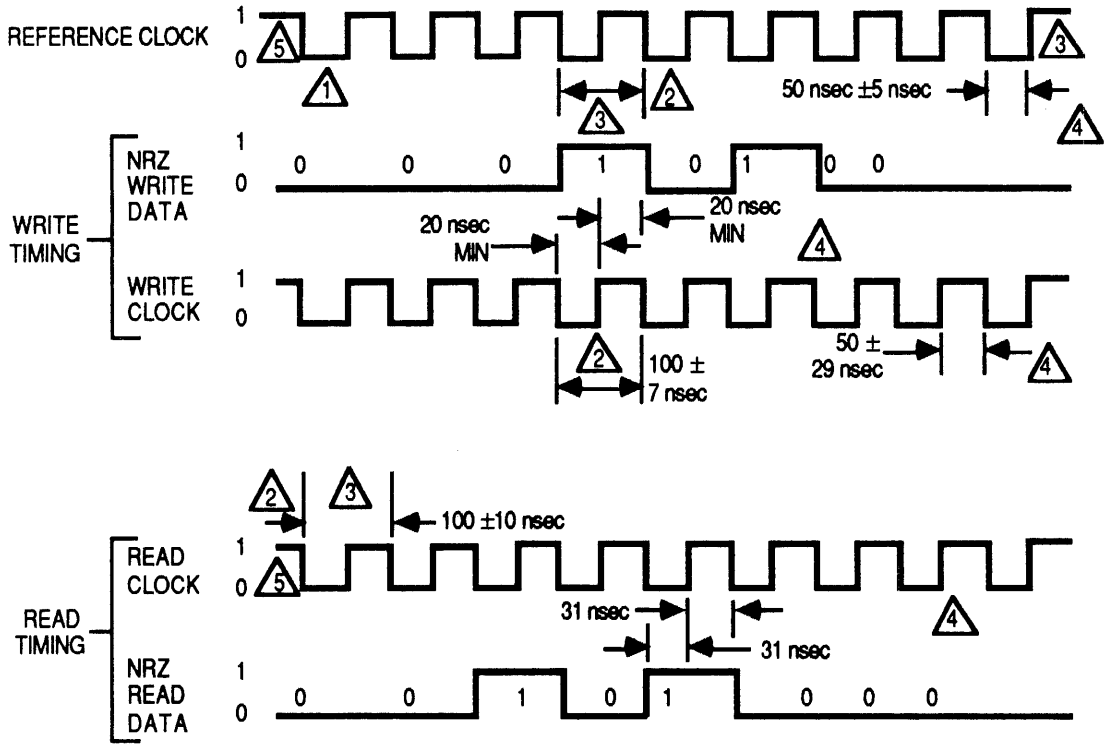
Figure 37
Data Line Driver/Receiver Combination

6.4.1 NRZ READ DATA

The data recovered by reading a prerecorded track is transmitted to the host system via the differential pair of NRZ READ DATA lines. This data is clocked by the READ CLOCK signal. See Figure 38, NRZ READ/WRITE DATA Timings, for timing. These lines are held at a zero level until PLO synchronization has been obtained and data is valid.

6.4.2 NRZ WRITE DATA

This is a differential pair that defines the data to be written on the track. This data is clocked by the WRITE CLOCK signal. See Figure 38, NRZ READ/WRITE DATA Timings, for timing. These lines must be held at a zero level during the writing of PLO synchronization.



1. ALL TIMES IN nsec MEASURED AT I/O CONNECTOR OF THE DRIVE.
2. SIMILAR PERIOD SYMMETRY IS IN ± 4 nsec BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.
3. EXCEPT DURING A HEAD CHANGE OR PLO SYNCHRONIZATION THE CLOCK VARIANCES FOR SPINDLE SPEED AND CIRCUIT TOLERANCES DO NOT VARY MORE THAN +0% TO -.2%. PHASE RELATIONSHIP BETWEEN REFERENCE CLOCK AND NRZ WRITE DATA OR WRITE CLOCK IS NOT DEFINED.
4. TIMING APPLICABLE DURING READING OR WRITING.
5. REFERENCE CLOCK IS VALID WHEN READ GATE IS INACTIVE. READ CLOCK IS VALID WHEN READ GATE IS ACTIVE AND PLO SYNCHRONIZATION HAS BEEN ESTABLISHED.

NOTE: *SEE THE FIGURE, DATA LINE DRIVER/RECEIVER COMBINATION, FOR DEFINITION OF 0 AND 1 ON THESE DIFFERENT SIGNAL LINES.*

Figure 38
NRZ READ/WRITE DATA Timings

6.4.3 READ/REFERENCE CLOCK

The timing diagram as shown in Figure 38, NRZ READ/WRITE DATA Timings, depicts the necessary sequence of events, with associated timing restrictions, for proper read/write operation of the drive. The REFERENCE CLOCK signal from the drive determines the

data transfer rate. The transitions from REFERENCE CLOCK to READ CLOCK must be performed without glitches. Two missing clock cycles are permissible.

The REFERENCE CLOCK rate is 10.0 + 0.10% megahertz.

The READ CLOCK rate is 10.0 + 0.30% megahertz.

6.4.4 WRITE CLOCK

WRITE CLOCK is provided by the controller and must be at the bit data transfer rate. This clock frequency is dictated by the READ/REFERENCE CLOCK during the write operation. See Figure 38, NRZ READ/WRITE DATA Timings, for timing.

WRITE CLOCK need not be continuously supplied to the drive. WRITE CLOCK should be supplied before beginning a write operation and must last for the duration of the write operation.

7.0 PHYSICAL INTERFACE

The electrical interface between the drive and the host controller is via four connectors:

- J1 - control signals (multiplexed)
- J2 - read/write signals (radial)
- J3 - DC power input
- J4 - frame ground

Jumper J6 is the spindle synchronization connector and is connected to the drives using this option.

Refer to Figure 26, Interface Connector Physical Location, for connector locations.

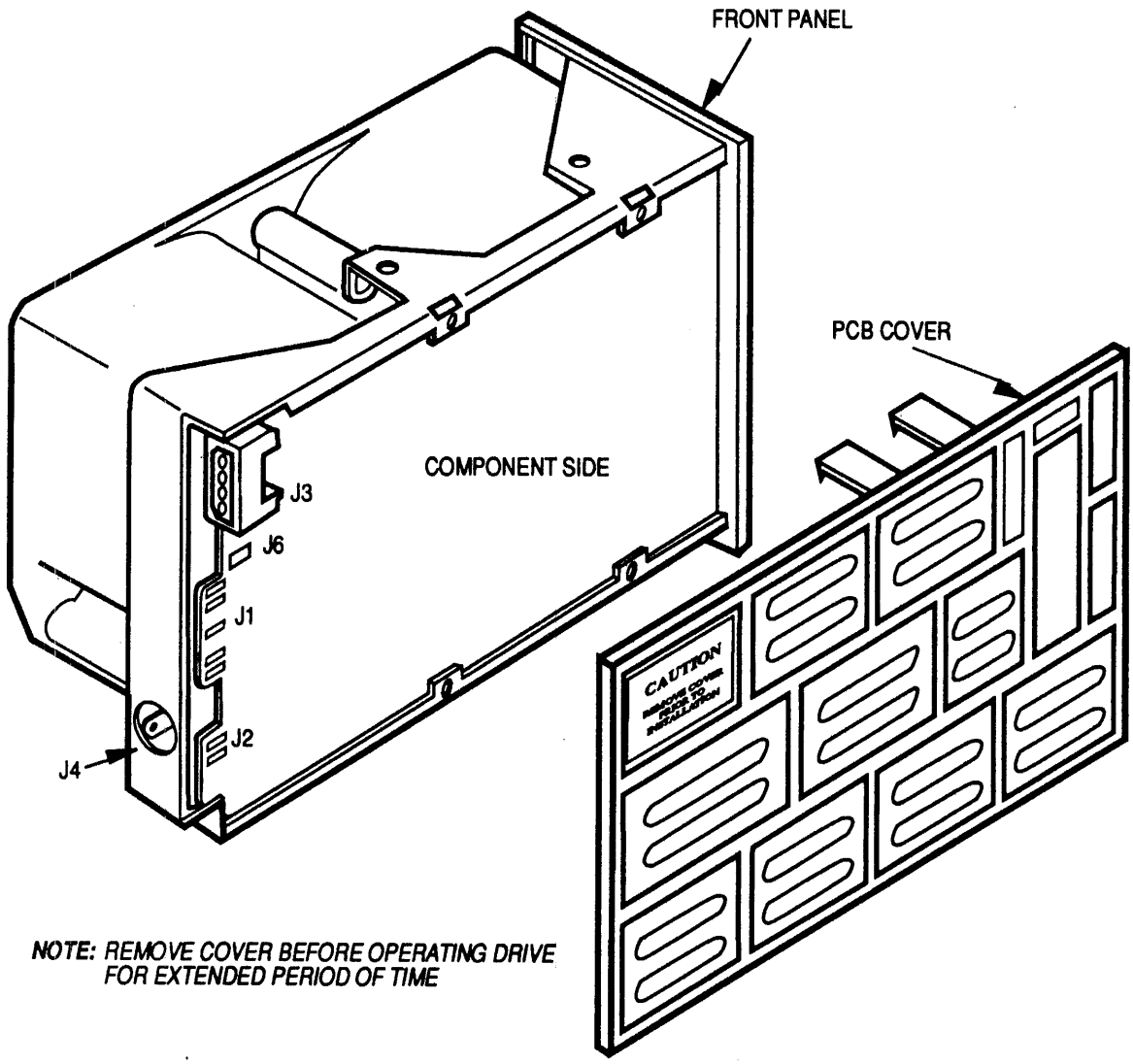


Figure 39
Interface Connector Physical Location

7.1 J1/P1 CONNECTOR

Connection to J1 is via a thirty-four-pin PCB edge connector. The dimensions for this connector are shown in Figure 40, J1 Connector Dimensions. The pins are numbered one through thirty-four, with the even pins located on the component side of the PCB. Pin two is located on the end of the PCB connector closest to the DC power connector J3/P3. A key slot is provided between pins four and six. The recommended mating connector for P1 is AMP ribbon connector part number 88373-3, or equivalent.

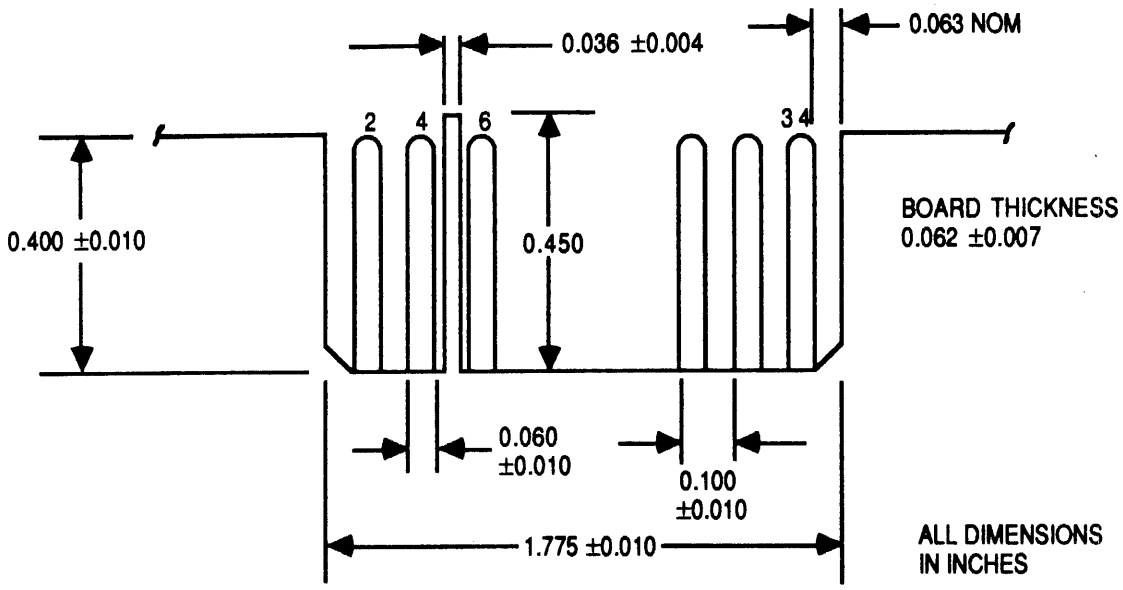


Figure 40
J1 Connector Dimensions

7.2 J2/P2 CONNECTOR

Connection of J2 is via a twenty-pin PCB edge connector. The dimensions for the connector are shown in Figure 41, J2 Connector Dimensions. The pins are numbered one through twenty, with the even pins located on the component side of the PCB. The recommended mating connector for P2 is AMP ribbon connector, part number 88373-6. A key slot is provided between pins four and six.

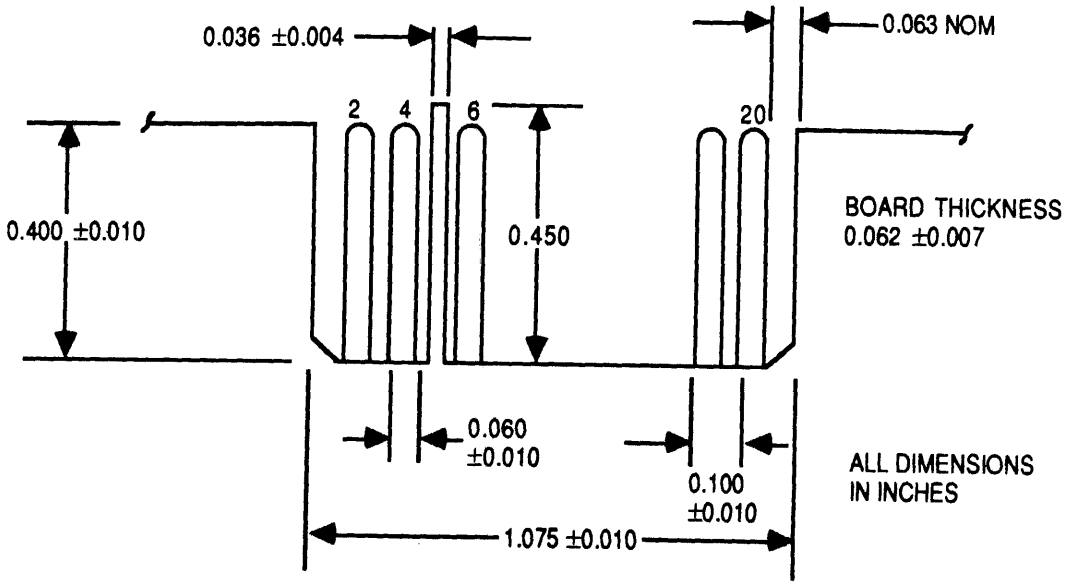


Figure 41
J2 Connector Dimensions

7.3 J3/P3 CONNECTOR

The DC power connector (J3), Figure 42, J3 Connector (Drive PCB, Solder Side), is a four-pin AMP MATE-N-LOCK connector, part number 350543-1, mounted on the solder side of the PCB. The recommended mating connector (P3) is AMP part number 1-480424-0, using AMP pins part number 350078-4 (strip) or part number 61173-4 (loose piece). J3 pins are numbered as shown in Figure 42.

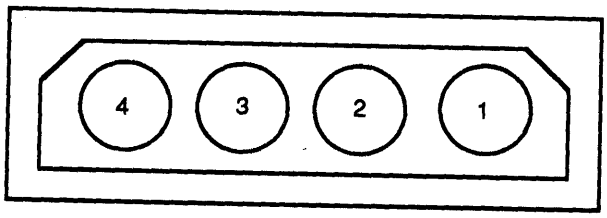


Figure 42
J3 Connector (Drive PCB Solder Side)

J3 CONNECTOR
PIN 4 +5 VOLTS DC ±5% PIN 3 +5 VOLT RETURN
PIN 1 +12 VOLTS DC ±5% * PIN 2 +12 VOLT RETURN

* ±10% AT POWER ON OR SEEKING

Table 23
Power Connector (J3) Requirements

7.4 J4/P4 Frame Ground Connector

The frame ground connection is a Faston-type connection, AMP part number 61761-2. The recommended mating connector is AMP 62187-1. If wire is used, the hole in J4 accommodates a wire size of 18 AWG maximum.

7.5 J6/P6 Auxiliary Connector

The auxiliary connector is a Berg 68451-121 ten-pin connector. The mating connector is a 3M 3473-6010. See Table 24, J6 Auxiliary Signal Cable Pin Assignments, for pin assignments.

SIGNAL NAME	PIN
MAPOUT	1
MAPIN	2
GND	3
MAPIN	4
GND	5
KEY (N.C.)	6
- REMOTE WRITE PROTECT	7
	8
- LED	9
+ LED	10

Table 24
J6 Auxiliary Signal Cable Pin Assignments

8.0 PHYSICAL SPECIFICATIONS

This section describes the mechanical and mounting recommendations for the XT-4000E Family disk drives.

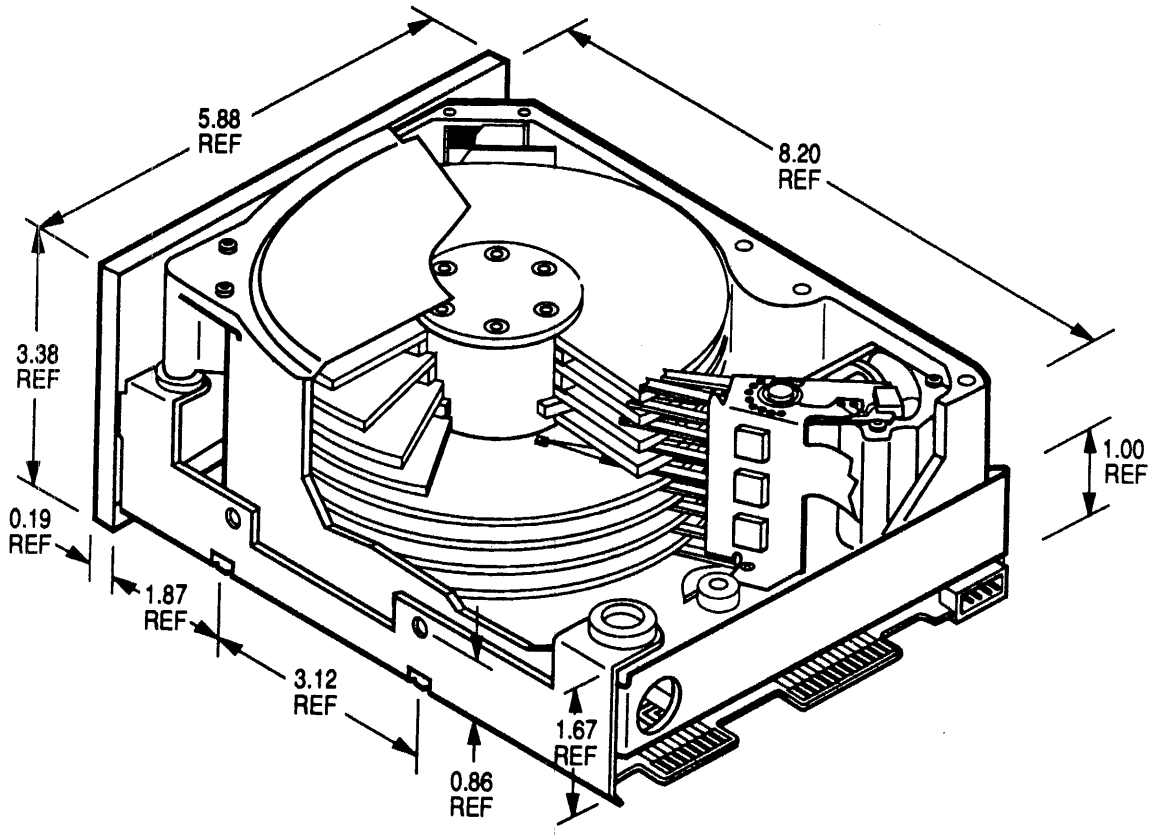
8.1 MOUNTING ORIENTATION

The drive may be mounted in any orientation. In any final mounting configuration, insure that the operation of the three shock mounts, which isolate the base casting from the frame are not restricted. Certain switching power supplies may emanate electrical noise which degrades the specified read error rate. For best results, it is suggested that the drive be oriented so that the PCB assembly is not adjacent to these noise sources.

8.2 MOUNTING HOLES

Eight mounting holes, four on the bottom and two on each side, are provided for mounting the drive into an enclosure. The size and location of these holes, shown in Figure 43, Mechanical Outline and Mounting Hole Locations, are identical to industry standard floppy drives.

CAUTION: *The casting is very close to the frame mounting holes in some locations. Mounting screw lengths must be chosen such that no more than 0.125 inches of the screw is available to enter the frame mounting hole. The torque applied to the mounting screws should be at least 9 inch-pounds; but to avoid stripping the threads, the maximum torque applied should not exceed 12 inch-pounds.*



REF = REFERENCE. FOR EXACT MEASUREMENTS SEE FIGURE 8, MECHANICAL OUTLINE, BOTTOM AND SIDE VIEWS.

Figure 43
Mechanical Outline and Mounting Hole Locations

8.3 PHYSICAL DIMENSIONS

Overall height, width, and depth, along with other key dimensions, are shown in Figure 43, Mechanical Outline and Mounting Hole Locations, and Figure 44, Mechanical Outline, Bottom and Side Views.

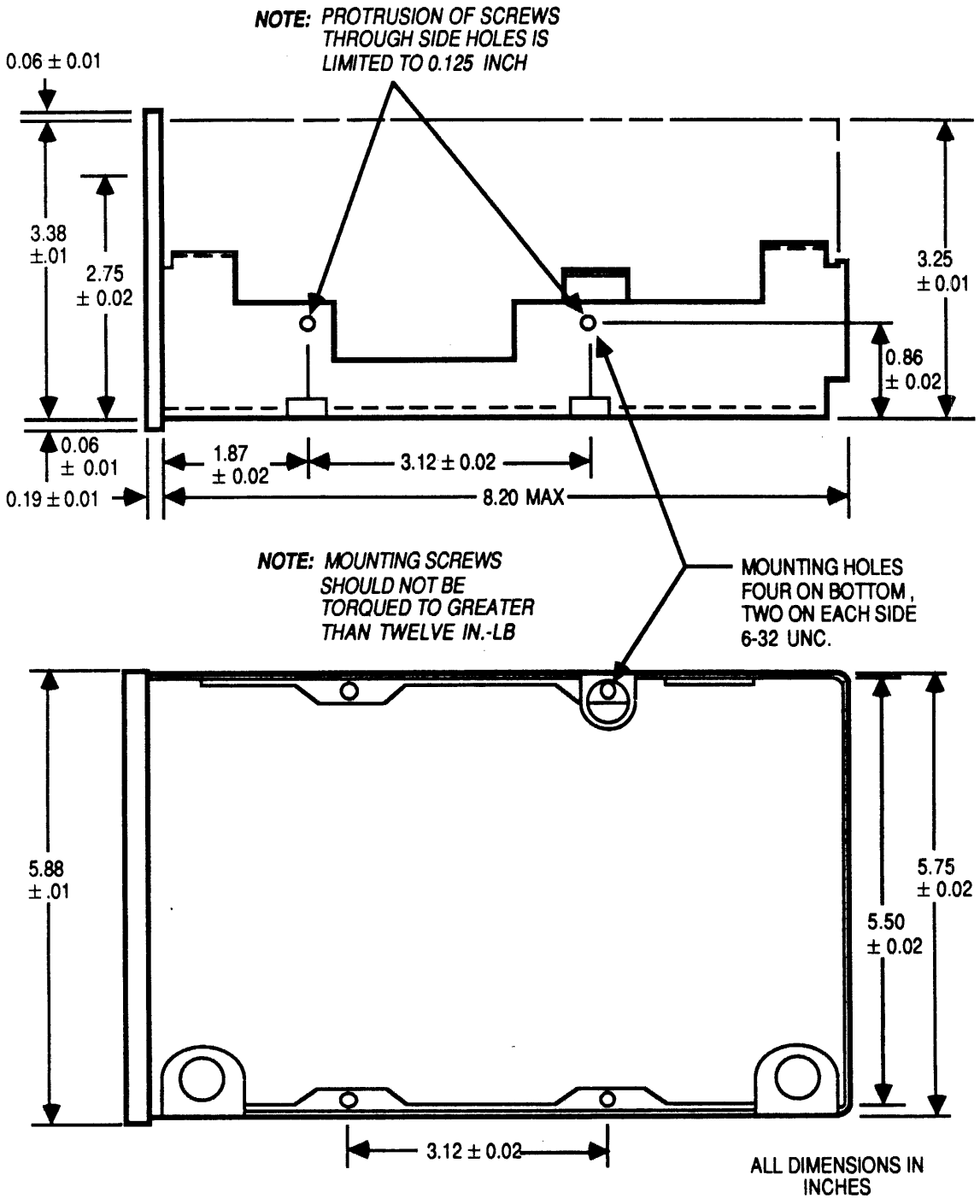


Figure 44
Mechanical Outline, Bottom and Side Views

8.4 SHIPPING REQUIREMENTS

At power down the heads are automatically positioned over the nondata, dedicated landing zone on each disk surface. The automatic shipping lock solenoid is also engaged at this time. **Maxtor** ships the drive in single- and multipack shipping containers.

8.5 REMOVABLE FACEPLATE

The faceplate may be removed in installations that require it. Remove the two C-clips and unplug the LED cable from the PCB. See Figure 45, Removable Faceplate.

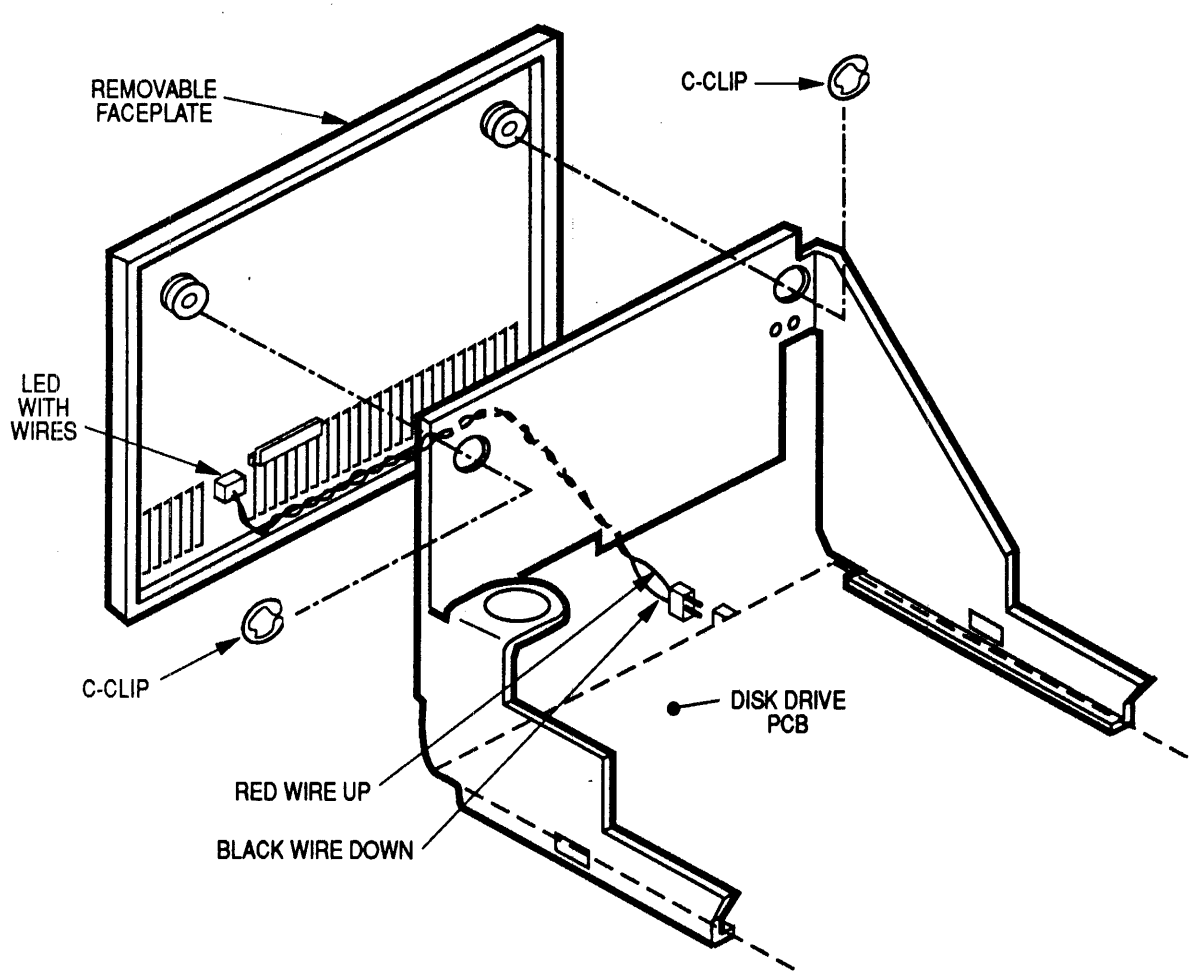


Figure 45
Removable Faceplate

9.0 PCB JUMPER OPTIONS

9.1 DRIVE ADDRESS SELECTION JUMPER

In multidrive configurations, it is necessary to configure each drive with a unique address. A maximum of seven drives are permitted per single host controller. The address for the drive is determined by installing the jumper plug in the appropriate jumper location (Figure 46, Drive Jumper Options). Table 25, Drive Select Jumpers, shows the drive selection jumpers. As shipped from the factory, the drive is configured as logical unit number one. Removing the jumper entirely is equivalent to a "no select."

DRIVE SELECT NUMBER	JUMPER INSTALLED
1	DS1
2	DS2
3	DS3
4	DS4
5	DS5
6	DS6
7	DS7

Table 25
Drive Select Jumpers

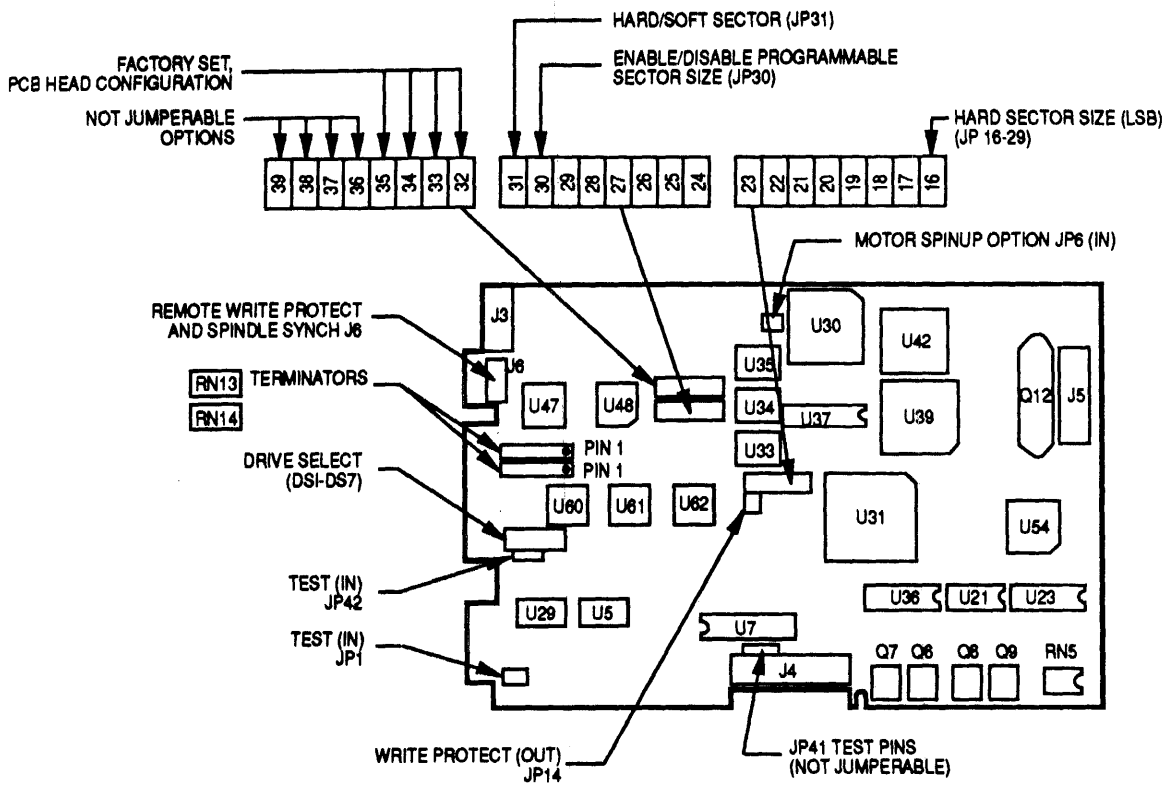


Figure 46
Drive Jumper Options

JUMPER	DESCRIPTION
JP1 (in) JP6 (in)	Used for Manufacturing Testing In = Motor Spinup Option Disabled Out = Remote Motor Spinup Option Enabled
DS1-DS7 (DS1 in) JP14 (out)	Drive Select In = Write Protected Out = No Write Protection
JP16-JP29	Unformatted Hard Sector Size in Bytes Jumpers, LSB = JP16, MSB = JP29 (refer to Table 30, Customer Selectable Jumpers)
JP30	In = Enables Programming of the Hard Sector Size Through the Interface Out = Disable this Function
JP31	In = Soft Sector Mode Out = Hard Sector Mode
JP32-35	PCB Head Configuration
JP41	Test Connection, Not a Jumperable Option
JP42 (in)	Used for Manufacturing Testing
NOTE: *JP4, JP5, JP15, JP36, JP37, JP38, JP39, JP40, JP41 ARE NOT JUMPERABLE OPTIONS. THE ONLY CUSTOMER CONFIGURABLE OPTIONS ARE JP16-JP29, JP30, JP31, DS1-DS7, JP6, AND JP14.*	

Table 26
Jumper Selections

9.2 DATA HEAD SELECTION JUMPERS (JP32-JP36)

Jumpers have been provided to allow the number of usable data heads to be selected. In order for the drive to respond correctly to the request configuration command - number of heads, these jumpers are set at the factory to correspond with the model of the drive. Table 27, Data Head Number Selection Jumpers, shows the various configuration options.

DRIVE MODEL	NUMBER OF DATA HEADS	JUMPER CONFIGURATION			
		JP 32	JP 33	JP 34	JP 35
XT-4170E	7	In	In	In	Out
XT-4380E	15	In	In	In	In

Table 27
Data Head Number Selection Jumpers

9.3 WRITE PROTECT SELECTION JUMPER (JP14)

Jumper JP14 is the write protect jumper. When the jumper is present (installed), the drive is write-protected and can only be read; no writing may take place. The drive does not have this jumper installed when it is shipped from the factory.

9.4 OPTION FOR SEQUENTIAL SPINDLE MOTOR SPINUP JUMPER (JP6)

The spindle motor spinup jumper (JP6) allows a string of drives to be started sequentially by the controller. When the jumper is present (installed), the drive automatically spins up as soon as power is applied. If JP6 is removed, the drive is started by issuing the appropriate command from the controller. As shipped from the factory, jumper JP6 is installed.

9.5 TEST JUMPERS (JP1, JP41, JP42)

These jumpers provide access to certain test signals. The specific signals and the normal factory settings are shown in Table 28, Test Pin Jumpers.

JUMPER	FACTORY SETTING	NOTES ON FUNCTION
JP1	In	Write Data
JP41	N/A	Test Pins, Not Jumperable
JP42	In	Write Gate

Table 28
Test Pin Jumpers

9.6 HARD SECTOR CONFIGURATION JUMPERS (JP16-29)

Jumper JP31 selects the mode of operation. Jumper JP31 installed configures the drive as a soft sector drive; removed, it configures the drive as a hard sectored drive.

Jumpers JP16 through JP29 allow the user to configure the drive's hard sector size. The sector size can range from a minimum of 123 to a maximum of 10,470 bytes per sector, with 1 byte granularity.

The hard sector configuration jumpers are encoded in a binary fashion, with JP16 being the least significant byte, and JP29 being the most significant byte. An installed jumper equates to a one.

Jumper JP30, if installed, enables setting the hard sector size over the ESDI interface.

JUMPER	# BYTES/SECTOR
J16	1
J17	2
J18	4
J19	8
J20	16
J21	32
J22	64
J23	128
J24	256
J25	512
J26	1,024
J27	2,048
J28	4,096
J29	8,192

Example: 36 Sectors Desired

1. $\frac{20,940 \text{ Bytes/Track}}{36 \text{ Sectors}} = 581$ Bytes/Sector
2. Install Jumpers J25, J22, J18, +J16
   Number Bytes/Sector = 512 + 64 + 4 + 1 = 581

Table 29
Customer Selectable Jumpers

10.0 MEDIUM DEFECTS AND ERRORS

Defects on the medium surface are identified on both a paper defect map and a defect map, written on the drive according to the ESDI format rules. These defect maps indicate the head number, track number, and number of bytes from index for each defect.

The maximum allowable number of defects per drive does not exceed an average of fifty per disk surface. Cylinder zero is certified to be defect-free.

The maximum number of encoded (NRZ) defects per drive is listed in Table 30, Maximum Number of Defects.

DRIVE MODEL	NO. OF DISKS	NUMBER OF DATA SURFACES	MAXIMUM NO. OF DEFECTS
XT-4170E	5	7	140
XT-4380E	8	15	300

Table 30
Maximum Number of Defects

As shipped, the disk drive contains two copies of the defect map, written on different locations on the disks.

One complete defect list resides on sector zero of cylinder 1,223. An identical copy is located on sector zero of cylinder 1,215. This allows for redundancy should an error occur on cylinder 1,223. Sector zero of any surface contains the defects for that surface. The format for the data field portion (see Figure 47, Defect List Format) of this sector is 256 bytes, with 2 bytes of cyclic redundancy check (CRC) ($x^{16} + x^{12} + x^5 + 1$).

Defect locations are identified by fields 5 bytes long. Other byte definitions are shown in Figure 47, Defect List Format. Byte count is the number of bytes from INDEX.

The location of the start of the actual defect may vary from the location specified on the defect list by up to + 1 byte due to the rotational speed tolerance of the drive motor.

The end of the defect list for each surface is indicated by 5 bytes of ones in the defect location field, or the end of the sector.

The CRC check bytes should be used, if that capability exists, but may be ignored if multiple reads are a more desirable approach.

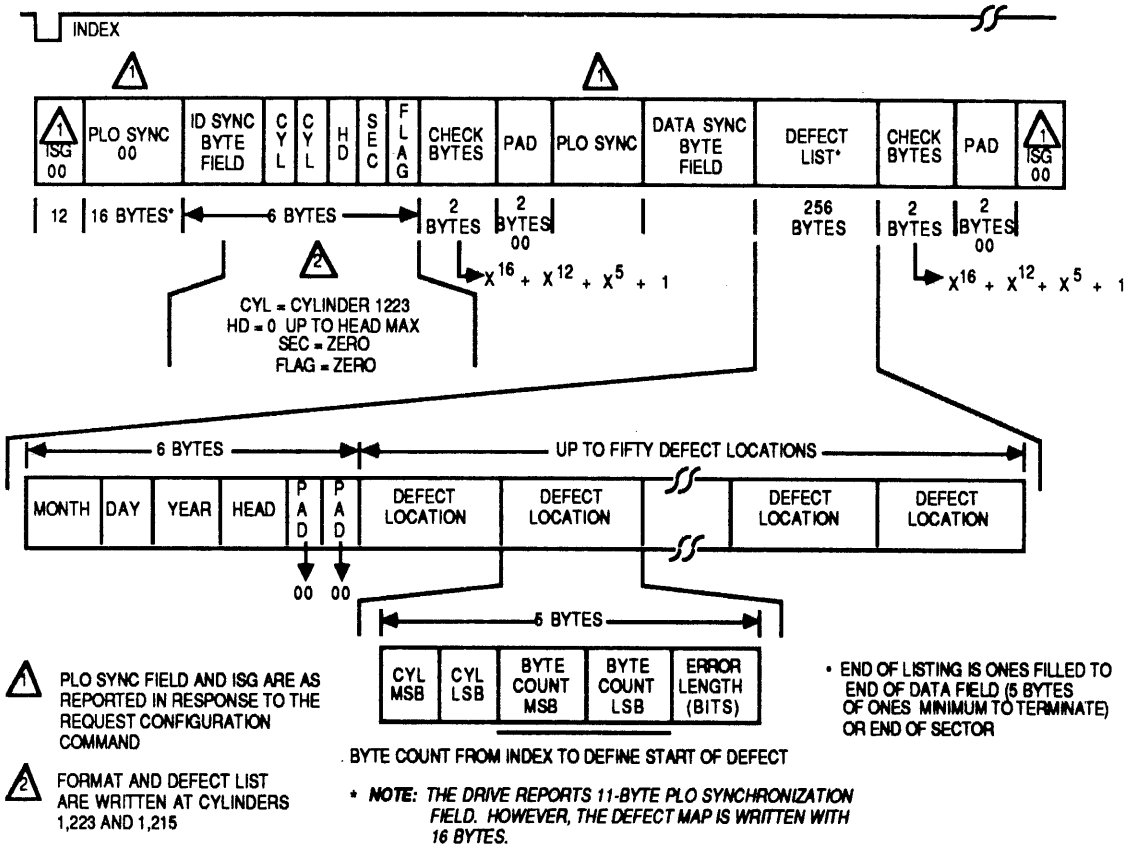


Figure 47
Defect List Format

APPENDIX: UNITS OF MEASURE

Abbreviation	Meaning
A/m	amps per meter
AWG	average wire gauge
bpi	bits per inch
dBA	decibel, a-weighted
fci	flux changes per inch
g	gram
Gbyte	gigabyte
Hz	hertz
mA	milliamp
µA	microamp
Mbit	megabit
Mbyte	megabyte
µm	micrometer
msec	millisecond
µsec	microsecond
nsec	nanosecond
Oe	oersted
RH	relative humidity
rpm	revolutions per minute
tpi	tracks per inch
xxB	binary values
xxh	hexadecimal values

GLOSSARY

3RDPTY. Third party

ACK. Acknowledge

ADR. Address

AGC. Automatic gain control

AM. Address mark

AM2. Address mode two

AME. Address mark enable

AMENBL. Address mark enable (to U60)

AMF. Address mark found

AMFD. Address mark found (from U60)

ANSC. American National Standards Committee

ANSI. American National Standards Institute

ASSERT. A signal driven to the true state.

ASYNC. Asynchronous

BIT. Binary digit

BYTE. Eight consecutive binary digits

CLK. Clock

CMD. Command

CMDCMP. Command complete

CODEIN. Code input

CODOUT. Code output

CRC. Control register clock, or cyclic redundancy check

CRD. Control register data

CRE. Control register enable

CSA. Canadian Standards Association

D/A. Digital-to-analog

DAC. Digital analog converter

DB (7-0, P). Eight data-bit signals, plus a parity-bit signal, that form a DATA BUS.

DC. Direct current

DEMOD. Demodulator

DET. Determination

DMA. Direct memory access

DTE. Disable transfer on error

DVSLTD. Device select

ECC. Error correction code

ECL. Emitter-coupled logic

EEC. Enable early connection

EIA. Electrical Industry Association

ENCRD. Encoded read data

ENDATA. Encoded data

ENDEC. Encoder/decoder

EPROM. Erasable programmable read only memory

ESDI. Enhanced Small Device Interface

EXPRCMP. External preamble complete

FCC. Federal Communication Commission

FIRMWARE. Computer programs encoded permanently into a ROM

FW. Firmware

G. Constant of gravitation

GND. Ground

HARD ERROR. An error due to faulty equipment, transmission techniques, recording media, etc.

HDA. Head/disk assembly

HEX. Hexadecimal

HNX, HNY. Head (zero through five) input x, head (zero through five) input y

HW. Hardware

I/O. Input and/or output

ISG. Inter-sector gap

ISO. International Standardization Organization

LBA. Logical block address

LED. Light-emitting diode

LSB. Least significant bit

MAP. Master pulse

MAPERR. Master pulse error

MAPIN. Master pulse in

MAPOUT. Master pulse out

µC. Microcomputer

µCOMPUTER. Microcomputer

MSB. Most significant bit

MSIN. Message in

MTBF. Mean time between failures

MTTR. Mean time to repair

N.C. No connection

NEGATE. A signal driven to the false state

NOM. Nominal

NRZ. Nonreturn to zero

OEM. Original equipment manufacturer

ONE. True signal value

P-P. Peak to peak

P/N. Part number

PARITY. A method of checking the accuracy of binary numbers

PC. Polycarbonate

PCB. Printed-circuit board

PCF. Page control field

PES. Position error signal

PLL. Phase-locked loop

PLO. Phase-locked oscillator

PM. Preventive maintenance

PMI. Partial medium indicator

POH. Power On hours

PRDET. Preamble detected

PREAMP. Preamplifier

PROM. Programmable read only memory

PTRN. Pattern

QUAL. Qualification

R/W. Read and/or write (heads)

RAM. Random-access memory

RD/REF CLK. Read/reference clock

RDGAT. Read gate (to U262)

RDGT. Read gate

RDRFCK. Read/reference clock

RDX,Y. Read data x, read data y

REF. Reference

RESERVED. Bits, bytes, fields and code values that are set aside for future standardization.

REVS. Revolutions

RFCLK. Reference clock

RGATE. Read gate (to U60)

RLL. Run-length limited

ROM. Read-only memory

RSRV. Reserved

SCSI. Small Computer Systems Interface

SLC. Servo/logic chip

SPEC. Specification

SRDX,Y. Servo read data x, servo read data y

STD. Standard

SVOCLK. Servo clock

SW. Software

SYNC. Synchronization, synchronous

SYNCLK. Synchronized clock

SYNCSP. Synchronous spindle

SYNDET. Synchronized data

TBD. To be determined. Values which are not defined as of the date this manual is published.

TLA. Top level assembly

TTL. Transistor-transistor logic

TYP. Typical

UL. Underwriter's Laboratories, Inc.

UNC. Unified National Coarse

UNF. Unified National Fine

UNSCODE. Unsynchronized code

VCO. Voltage controlled oscillator

VCOCLK. VCO clock

VDE. Verband Deutscher Electrotechniker

VEL. Velocity

VENDOR UNIQUE. The bits, fields, or code values that are vendor specific.

VREF. Voltage reference

WCLK. Write clock (to U60 from interface)

WCS. Write current select

WDI. Write data input

WGATE. Write gate (to U60)

WRITE*. -WRITE to preamplifier chip

WRT. Write

WRTCLK. Write clock

WUS. Write unsafe output

XFER. Transfer

ZERO. False signal code