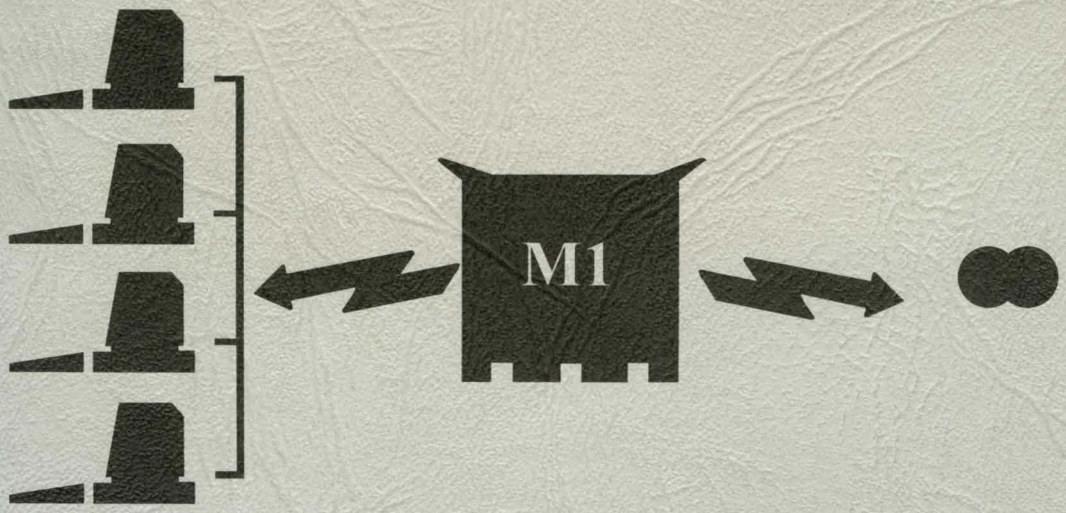
SBC M1 SERIES

SINGLE BOARD COMPUTER

User Guide



Mentec

0. FIRST EDITION

M1 Single Board Computer
User Guide
Version 1.0

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Mentec Limited
Mentec House,Dun Laoghaire Industrial Estate
Dun Laoghaire
Co. Dublin
Ireland

Telephone: *353-1-2059797*
Fax: *353-1-2059798*

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PREFACE
AUDIENCE

This document is intended for two specific types of user. Firstly, the engineer who needs to configure and install the SBC M1 Single Board Computer. Secondly, the programmer who wants to write applications software for the module. An overview of the architecture is given, but the document is not intended as a tutorial on PDP-11's.

ORGANISATION

Configuration, programming and installation details are divided among the chapters as follows:

CHAPTER 1: PRODUCT OVERVIEW

Chapter 1 describes the main functions and features of the SBC M1

CHAPTER 2: SPECIFICATIONS

Chapter 2 gives a quantitative description of the features of the SBC M1.

CHAPTER 3: UNPACKING AND INSTALLATION

Chapter 3 outlines the steps a user must follow in order to successfully unpack and install the module.

CHAPTER 4: HARDWARE CONFIGURATION

Chapter 4 explains how the user can alter the hardware configuration of the SBC M1.

CHAPTER 5: SELECTABLE SOFTWARE CONFIGURATION

Chapter 5 describes the functionality and operation of the SBC M1 software.

CHAPTER 6: SYSTEM ARCHITECTURE

Chapter 6 gives an overview of the architecture of the SBC M1 module. It describes how the PDP-11 architecture is implemented on the SBC M1.

CHAPTER 7: SERIAL I/O INTERFACE

Chapter 7 details the architecture, programming and cables of the serial-line sub-system.

APPENDIX A: BACKPLANE PIN UTILISATION

Appendix A lists the Q-Bus signals and indicates their positions on the module.

APPENDIX B: OP CODES & TRAPS

Appendix B contains a list of PDP-11 OP Codes.

APPENDIX C: I/O PAGE MEMORY MAP

Appendix C contains a memory map of the I/O page for the SBC M1.

APPENDIX D: DEVICE MNEMONICS

Appendix D contains the device mnemonics as used in the boot prompts.

RELATED DOCUMENTS

The following Digital Equipment Corporation publications provide additional information on DEC PDP-11. DCJ11 User Guide, Micro PDP-11 Hand Book and the Micro PDP-11 Interface Hand Book

1 PRODUCT OVERVIEW

1.1 INTRODUCTION

The SBC M1 module is a high performance ASIC based PDP11 quad height QBUS card. The module contains 1 to 4Mb of RAM, four DLV11J compatible serial lines and 32 Kb of FLASH EPROM, and a 50Hz, 60Hz, 800Hz or BEVENT real-time clock. The SBC M1 also interfaces to the 22-bit Q-BUS and supports block mode DMA.

1.2 PROCESSOR

The M1 is a high performance PDP-11 similar in functionality to previous Mentec PDP11 CPU's. PDP11 instructions are implemented in "Microcode" a micro programmed subsystem based on an ASIC implementation. The Console ODT function is also performed in the M1's Microcode.

1.3 MEMORY

The module contains 1Mb/2Mb/3Mb/4Mb of Q-bus non-parity SRAM. The Module's SRAM is accessible by other system devices over the Q-bus using DMA.

1.4 LSI-BUS INTERFACE

The module interfaces to the extended LSI-11 bus and can address up to 4 MB of main memory and communicate with other bus devices, disk controllers or asynchronous serial line multiplexers. The 22-bit extended LSI-11 bus is completely downward compatible with the standard 18-bit LSI-11 bus.

1.5 SERIAL LINES

Contained on the module are four independent, full-duplex, asynchronous serial line units (SLUs) which are software compatible with the DLV11J Q-bus module. Channel number 3 is configurable as the system console. The interface transmits and receives data from the peripheral device over EIA lines, which support data leads only. The four independent lines are contained within a single FPGA chip.

1.6 LINE TIME CLOCK

The line time clock on the module is used by software systems to control events, such as operating system scheduling, software interrupts and system time.

1.7 BOOTSTRAPS

There are a number of primary bootstraps available on the module, which facilitate the loading of secondary bootstraps from storage devices, such as tape and disk drives.

1.8 INTERRUPTS

An interrupt allows the current code being executed by the processor to be suspended, while the requesting device is serviced. The interrupt source may be from either the LSI-11 bus or the SBC M1 processor. The interrupt facility of the LSI-11 bus, supported by the module, allows any I/O device to temporarily suspend the current program execution and divert the processor operation to service the requesting device.

1. 9 LED DISPLAY

The LED display indicates the power up status and operating status of the module i.e. is there power on the module, have all power-up diagnostics been passed, is the module in console ODT or executing software.

2. SPECIFICATION

2. 1 PHYSICAL

Height - 25 mm.
Length - 214 mm.
Width - 265 mm.
Weight - 426 g.

2. 2 POWER REQUIREMENTS

Power Supply - +5.0 V +10%/-5% 7A (typical).
+12V +/- 5% 2A (max.).

NOTE: **The M1 does not use 12V it only supplies it to the Berg headers for use by external devices.**

2. 3 ENVIRONMENTAL

2. 3 .1 TEMPERATURE

Storage - -10 to 60 Degrees C.
Operating - 0 to 50 Degrees C.

NOTE: **The module should be brought into operating conditions and allowed to stabilise before commencing operation.**

2. 3 .2 AIRFLOW

Operating - Adequate airflow must be provided to limit the inlet to outlet temperature rise across the module to 5 Degrees C when the inlet temperature is 35 Degrees C.

NOTE: **These are design limits. Lower temperature limits will serve to increase the life of the product.**

2. 3 .3 ENVIRONMENT

Operating Air must be non-caustic.

2. 3 .4 RELATIVE HUMIDITY

Storage - 10% to 90% (no condensation).
Operating - 10% to 90% (no condensation).

2. 4 CONNECTORS AND CABLES

Connectors: AMP 2x5 pin male
J3 to J6: RS232 Null Modem - DEC BC20N-05
Cables: [2x5 pin AMP female to RS-232C female (25-way Cannon D-type)].

3. UNPACKING AND INSTALLATION

3. 1 INTRODUCTION

This chapter explains how to unpack and install the SBC M1 module. It is advisable to leave the module in the factory configuration until its operation has been verified.

3. 2 UNPACKING

The following four steps outline how the SBC M1 should be unpacked. (If there is visible damage to the shipping carton then the module should be unpacked in the presence of the delivering carriers agent).

WARNING STATIC ELECTRICITY CAN DAMAGE COMPONENTS ON THE MODULE. PROPER PRECAUTIONS SHOULD BE TAKEN DURING ANY OPERATION WHICH INVOLVES HANDLING THE BOARD.

1). Ensure that an anti-static wrist-strap is being worn.

2). Lay the shipping carton on a flat surface and open out the flap.

3). Remove the module from the anti-static bubble-wrap. Allow a moment for any static to leak away to ground and then remove the module from the anti-static bag.

4). Inspect the module for damage.

If the module is damaged then no installation or repair should be undertaken. If the delivering carriers agent was not present during the unpacking then an insurance inspection claim should be called for. If the board is to be repaired then it should be returned to the distributor.

3. 3 INSTALLATION

3. 3 .1 Introduction

This section details the installation of the SBC M1. Bus connections and user connections are described. Full details of the LED display on the front of the module are also given since monitoring these is the first step in verifying the correct operation of the module.

3. 3 .2 Bus Connections

The following must be verified before the module is installed in the backplane:

1). The backplane is a correct Q-Bus AB-AB or AB-CD backplane.

2). +5Vdc and +12Vdc are available at the correct points on the backplane Module damage will result if user power is incorrectly bussed (ref AppendixA).

3). There is adequate power reserve for the module and any other Q- Bus modules which are to be inserted in the backplane.

4). The backplane is adequately cooled and there is sufficient airflow.

5). The board is configured as required. It is advisable to leave the module in the factory configuration until its operation has been verified.

WARNING MODULE DAMAGE WILL RESULT IF THE BOARD IS REMOVED FROM THE BACKPLANE WITH POWER APPLIED.

The SBC M1 may now be installed as follows.

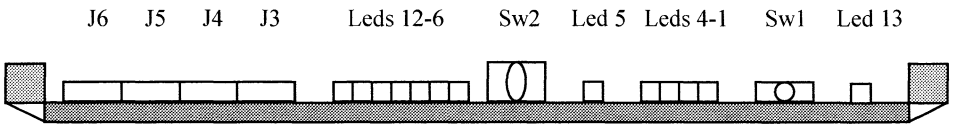
1).Place the module in the backplane in the first most slot. The other cards should then be placed in the following slots. Ensure that grant continuity is maintained for all the NPR modules. The respective backplane documentation should give details.

2).Apply power to the backplane and observe diagnostic LEDs for correct operation.

3. 4 USER CONNECTION

The serial communications with the SBC M1 is by means of four AMP ten-way connectors on the front of the module (refer to figure 4.1). A suitable DEC cable is BC20N-05 (5 foot EIA RS-232C null modem cable). For initial module verification a single cable should be connected to J6.

3. 5 DIAGNOSTIC LEDs AND POWER-UP



Led Indicators:

1.	Led 1	WCS Load 1	Red
2.	Led 2	WCS Load 2	Red
3.	Led 3	WCS Load 3	Red
4.	Led 4	WCS Load 4	Red
5.	Led 5	FP Indicator	Red
6.	Led 6	12V	Green
7.	Led 7	BDCOK	Green
8.	Led 8	Run	Green
9.	Led 9	ODT	Red
10.	Led 10	Console	Red
11.	Led 11	Memory	Red
12.	Led 12	CPU	Red
13.	Led 13	i960 Reset	Red

Hardware Setup Switch SW1 operates as per manual page 4-1
M1 Board Power Up Indicators:

Rotary Switch SW2 operates as per manual page 4-3

On power up the M1 SBC differs from The M11 SBC in the following manner. The banner message,

```
Loading Microcode v1.*
1    2    3    4    5
```

is replaced by the extinguishing of six LED indicators in the following sequence,

LED 13 extinguishes followed by Led 5. Then LED's 1,2,3,4 illuminate together and extinguish singularly in the sequence 1, 2, 3, 4. LED's 6 through 12 should be consistent with the SBCM11 LED indicators as described in Table 3.1 at the end of this chapter. This sequence of events indicates a correct power up procedure of the M1 SBC.

The LED display (6 through 12) on the front of the module should be observed while the power is being switched on. When power is applied, two bus signals, BDCOK-H and BPOK-H, are asserted. These signals indicate that the correct DC power and AC line power levels are available. The M1 then proceeds to execute a power-up diagnostic routine, which test the CPU, MEMORY and CONSOLE. When each diagnostic is passed the corresponding diagnostic LED is turned off. The action taken by the M1 at this point depends on the value of the power-up configuration register. If the module is in factory configuration, it will commence executing the boot code resident in the module's FLASH EPROMS.

TABLE 3-1 STATUS LED DESCRIPTION

Led	Colour	Description
6	Red	CPU Test. Cleared on power-up if internal CPU diagnostic is passed.
7	Red	Memory Test. Cleared on power-up if CPU receives a reply from memory at address 0 and no reply from memory at address 17777700 octal
8	Red	Console Test. Cleared on power-up if CPU receives a reply from console DLART at address 17777560 octal
9	Red	Processor in ODT. Set if processor is running console ODT.
10	Green	Processor Running. Set if the processor is executing code.
11	Green	Power. This LED indicates the status of the signal BDCOK-H on the Q-bus. BDCOK-H is a PSU generated signal that is asserted when there is sufficient DC voltage available to sustain reliable system operation.
12	Green	Communications Power. Set if fuse F1 and +/- 12V are operating correctly.

4. SELECTABLE HARDWARE CONFIGURATION

4.1 INTRODUCTION

Module hardware configuration is by means of selecting switch positions and component values, as described in this chapter, and by means of firmware which is user programmable through the console as described in chapter 5.

4. 1 .1 Bus Grant Continuity Jumpers

To confirm the installation of the grant jumpers on the module identify the back-plane and refer to table 4-1 for jumper configuration. Jumpers are located at W1 and W2.

NOTE:- Jumpers are installed in module on leaving factory.

TABLE 4-1 BUS GRANT CONTINUITY

Backplane	Bus Type	Jumpers
H9270 (4 slot)	**Q/Q**	**in**
H9275 (9 slot)	**Q22/Q22**	**in**
H9273 (4 slot)	**Q/CD**	**out**
H9276 (9 slot)	**Q22/CD**	**out**

4. 1 .2 Fuse

If the current drawn by all external device powered via the modules communications connectors (J3 – J6) exceeds 2 amps, the modules fuse (F1) will have to be replaced. LED 12 will be extinguished if the fuse has blown or +/- 12V has failed. Replace the fuse with one of the same specification.

4. 1 .3 Factory Hardware Default Switch

This switch allows the user to force the module's PROGRAMMABLE HARDWARE CONFIGURATION to factory standard. Switch, SW1 is usually set such that the module's configuration is loaded from the EPROM on power-up (Refer to section 5.5.5.1 for details on factory default).

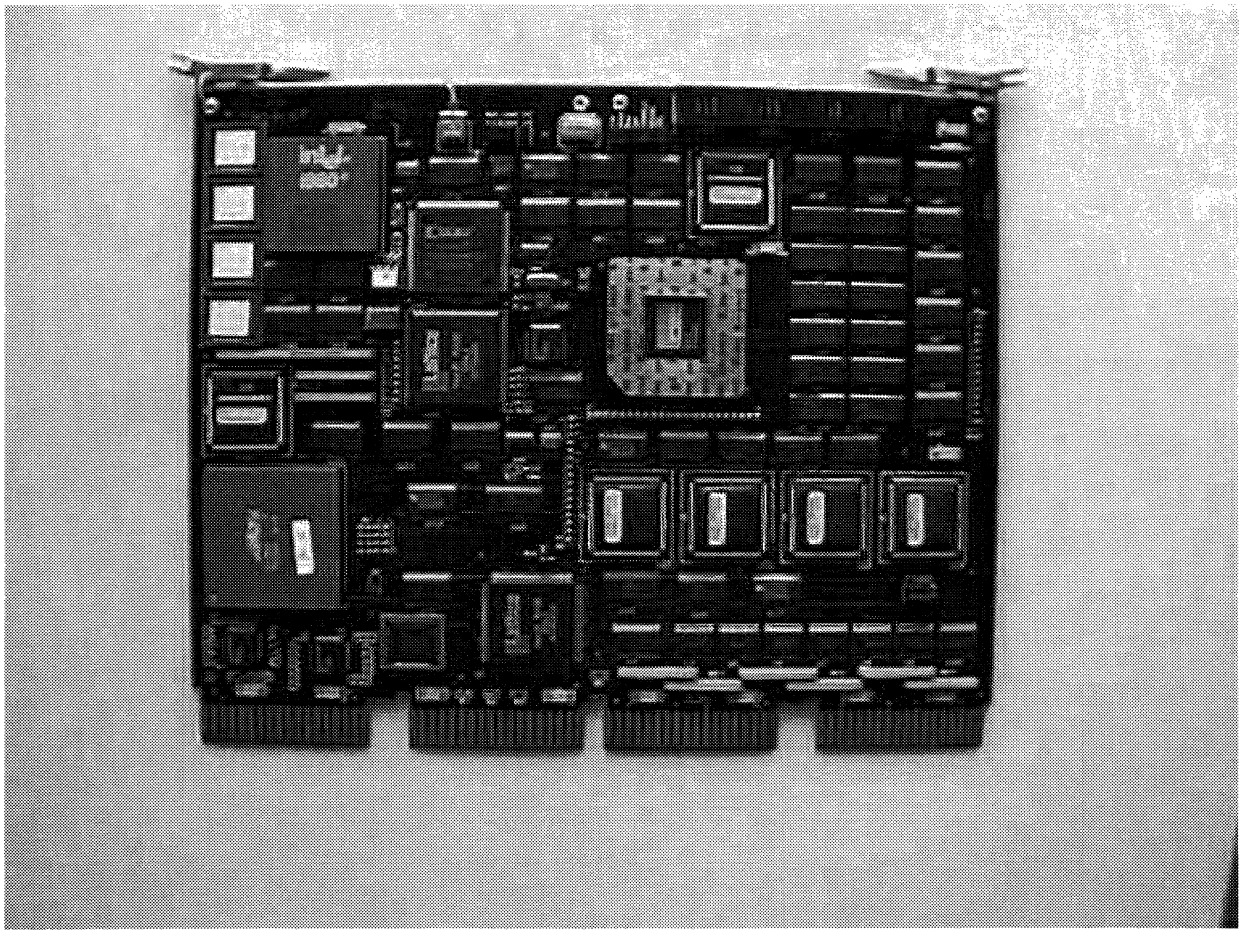


Figure 4.1 SBC M1 Layout

4.1 4 Rotary Baud Rate Default Switch

Switch SW2 provides a hardware over ride switch for the baud rate on the console serial line. This switch effectively over rides the baud rate selected in the Hardware Setup Menu. Table 4-3 provides details of the Rotary Baud Rate switch settings.

TABLE 4-3 ROTARY BAUD RATE SETTINGS

Position	Baud rate
0 to 7	As per Hardware Setup Menu
8	38400 Baud
9	19200 Baud
A	9600 Baud
B	4800 Baud
C	2400 Baud
D	1200 Baud
E	600 Baud
F	300 Baud

5. PROGRAMMABLE MODULE CONFIGURATION

5.1 INTRODUCTION

This chapter is a guide for the boot/diagnostic and module configuration software. It describes the functionality and basic operation of the software. In addition some of the internal functioning of the software is described.

The bootstrap and diagnostic firmware is contained in one FLASH EPROM on the SBC M1. The EPROM is used both by the power-up circuitry and the boot/diagnostic software to retain setup information.

5.2 FUNCTIONAL OVERVIEW

The bootstrap/diagnostic EPROM provides a set of diagnostics, bootstraps for standard devices, and configuration software for the board. The boot software can operate in two modes viz:

Automatic Mode: - The bootstrap attempts to boot in sequence from a pre-configured list of devices.

Dialogue Mode: - The user enters commands directly to configure or boot the system.

Dialogue mode is entered when an non-configured board is booted, when an automatic bootstrap fails, or when <CTRL/C> is entered during the execution of diagnostics or an auto-boot sequence. Therefore if a board is setup for automatic boot, with power-up testing disabled, it may be necessary to unload or disable all devices in the automatic boot list to gain access to the dialogue boot.

5. 3 OPERATIONAL OVERVIEW

The boot code supports both ANSI standard video terminals and dumb terminals. ANSI standard terminals use cursor position escape sequences whereas dumb terminals allow only standard ASCII control characters.

Both upper and lower case may be used interchangeably in all responses to the boot/ diagnostic code. Lowercase is converted to and echoed as uppercase.

As the SBC M1 does not have a display register, failures early in testing i.e. before the functionality of the console sub-system are established, are signalled by the processor halting with a failure code in R0.

The Failure codes are as follows:

0 - bootPROM window 0, window number invalid.
1 - bootPROM window 1, window number invalid.
2 - bootPROM window 0, checksum invalid.
3 - bootPROM window 1, checksum invalid.
4 - Low 64kB memory failure.
5 - bootPROM window number invalid, not window 0 or 1.
6 - bootPROM window checksum invalid, not window 0 or 1.
7 - Processor Trap to memory location 4 octal.
10 - Processor Trap to memory location 10 octal.
11 - Data parity error detected, trap location 114 octal.

5. 4 AUTOMATIC BOOT MODE

Automatic boot mode is selected using the "Setup Option" in dialogue mode. In this mode the bootstrap will run processor and memory diagnostics and then attempt to boot the system from one or a series of devices. These devices may be selected using the "BOOT Option" also in dialogue mode. The diagnostics run during boot are configurable from the setup menu as described in section 5.5.5.

5. 5 DIALOGUE MODE

Dialogue mode is intended for use in reconfiguring the system. The following is the initial dialogue mode menu:

```
BOOT -    BOOT FROM A SPECIFIC DEVICE.

HELP   -  PROVIDE A SUMMARY OF COMMANDS.

LIST   -  LIST BOOTSTRAPS PROVIDED.

MAP    -  DISPLAY A MAP OF ADDRESS SPACE.

SETUP  -  CONFIGURE THE SBC M1.

TEST   -  ENTER A CONTINUOUS TEST MODE.
```

To invoke the required option, enter the associated command and a <CR>.

Note: - 'TEST' assumes that the hardware setup information is valid.

5. 5 .1 BOOT - Boot from a specific device

To enter this option the user inputs "B<CR>" at the main menu and the SBC M1 responds with the prompt "BOOT>". The BOOT function invokes the SBC M1 device specific bootstrap to load a primary bootstrap from the selected boot device. The user must enter the boot device mnemonic and device unit number followed by "<CR>". The device number is only required in instances when more than one device of a certain type is resident in the system. Note the default device number is "0" e.g. to select a second RL02 drive the user enters DL1 followed by <CR>.

When the software has been loaded from the device, control is relinquished to the primary bootstrap, which normally proceeds to load a secondary bootstrap and then a possible tertiary bootstrap. Success of this operation is usually indicated by a "linefeed" at the console. The devices and the mnemonics that are supported by the SBC M1 are listed in table 5-1.

TABLE 5-1 SUPPORTED DEVICES

Mnemonic	Device
DB	RM03 emulation
DD	TU58
DL	RL01/02
DU	MSCP
DX	RX01
DY	RX02
EE	CONCENTRATOR
MS	TK25/TSV05
MU	TK50
XQ	DEQNA (Decnet boot)
NL	Delay for devices to come ready

5. 5 .2 HELP - Provide a summary of commands

This option redisplays the MAIN MENU and is selected by entering "H<CR>" at the above menu. This option is useful when the console is a dumb terminal and it is required to recall the available commands.

5. 5 .3 LIST - List bootstraps provided

This option lists the mnemonics and corresponding devices that the SBC M1 module can boot from as shown in table 5-1 above. This option is selected by entering "L<CR>" at the MAIN MENU. <CR> returns the user to the main menu.

5. 5 .4 MAP - Display a map of address space

When this option is selected the SBC M1 reads all locations in the 4Mb address space (0 to 17777777 octal), starting at location 0 and working upwards through the memory address space and then proceeding into the I/O address space. The SBC M1 continues reading until a location fails to reply at which stage it outputs the address it started from and the address of the last location that replied. This procedure is carried out until the complete address range has been read.

This operation reports all contiguous memory blocks and I/O device registers which respond to read commands in the system. The I/O space occupies the top 8 Kbytes of the total 4 Mbytes address space.

This option is selected by entering "M<CR>" at the MAIN MENU. <CR> returns the user back to the main menu.

For listing of fixed I/O page registers refer to Appendix C.

5. 5 .5 SETUP - Configure the SBC M1

Setup mode allows the configuration of both the SBC M1 hardware and of the boot/diagnostic operation. Alterations to Software Setup take effect immediately, however they must be saved for retention. Hardware alterations only take effect if SW1 is in position “B” on power up. SW1 is used to force the module into factory hardware configuration (position 'A') or load hardware configuration from FLASH EPROM (position 'B'). Software configuration is reset to factory default by selecting option 4 of the Setup Menu.

The initial setup mode menu is shown below:

```
          SETUP MENU

     1  MODIFY HARDWARE SETUP

     2  MODIFY SOFTWARE SETUP

     3  SAVE MODIFIED SETUP

     4  INITIALIZE TO FACTORY SETUP

     5  CONFIGURE AUTOBOOT LIST

     6  CONFIGURE DEVICE TRANSLATIONS

     7  EXIT SETUP

     To select an option, enter the associated number and press
<CR>.
```

The first two options may be used to obtain a listing of the current setup. No changes are saved to the FLASH EPROM until a save is performed.

5.5.5.1 Modify Hardware Setup

This option is selected by entering "1<CR>" at the "SETUP MENU". The following menu is then displayed indicating the configurable hardware. The various options for each hardware element are described below. "<CR>" returns the user to the "SETUP MENU".

Note that SW1 is only used to temporarily force the module to factory hardware configuration. Changes to the setup may be made with SW1 in either position but only take effect when SW1 is in position “B” and the board is powered up.

NOTE : Any devices which will conflict with the module's factory setups must be removed from the system when the module is being restored to default settings.

To alter a specific hardware element the user enters the corresponding number from the menu followed by <CR>. The menu below shows the factory hardware configuration for the SBC M1 module:

```
1    Base address of DLV11J emulation .      176500
2    Base vector of DLV11J emulation. .      300
3    Serial line 0 baud rate. . . . . .      9600
4    Serial line 1 baud rate. . . . . .      9600
5    Serial line 2 baud rate. . . . . .      9600
6    Serial line 3 baud rate. . . . . .      9600
7    On-board console . . . . . .            Enabled
8    On-board LTC . . . . . .                60 HZ
9    On-board bootPROM. . . . . .            Enabled
10   Power-Up mode. . . . . .                173000
11   Power-Up address . . . . . .            000000
12   On-board parity CSR address. . . .      172100
13   Halt option. . . . . .                  Cleared
14   On board parity enable . . . . . .      Enabled
15   Console Halt enable . . . . . .         Enabled
16   Memory timeout select . . . . . .       24uS
```

Note 1 :- **In order for a modification to the hardware configuration to take effect the configuration must be saved and the system turned off and on as the information is loaded only during initialisation.**

Note 2 :- **Refer to section 5.5.5.4. Restore Factory Hardware Configuration for details on how to reset the SBC M11 module to factory hardware configuration.**

The SBC M1 has four on-board serial lines that emulate the functionality of a DLV11J. The first 8 options in the hardware setup menu allow the user to configure most of the characteristics of this emulation. The serial (DL) lines do not support parity generation or the generation of more than one stop bit.

1. DLV11J Base Address

A DL module consists of four serial lines. Each serial line has four registers and as a result, the address space for the DL module requires sixteen contiguous locations. Therefore the base address for the DL module must increment in 40 octal bytes or 16 decimal words in the range 160000 octal to 177740 octal.

NOTE:- **That the I/O page addresses for these serial lines will occupy range of 30 octal if the on-board console is enabled and 40octal if it is disabled.**

2. DLV11J Base Vector

Similarly the four interrupt vector addresses for use with the serial lines must be contiguous. The base interrupt vector for the DL lines is selectable in the range 0 to 340 octal. Note that bits [0:4] of the interrupt base address are always set to 0. The default base address is 300.

Note:- The vectors for these serial lines will occupy a range of 30 octal if the on-board console is enabled and 40 octal if it is disabled.

3 - 6. Serial Line Baud Rate.

The baud rate for each of the four serial lines may be individually configured to any of 300, 600, 1200, 2400, 4800, 9600, 19200 or 38400 baud. When this option is selected, the user enters the number of the required baud rate as displayed on the screen followed by <CR>.

7. On-Board Console

If this option is selected the CSR address for SLU3 is 177560 octal and the vector is 60 octal irrespective of the addresses assigned to the other serial lines. When using on-board console the base address for the DL module must be either 176500 octal, 176540 octal or 177500 octal . A warning is given on saving the setup if one of the above is not selected as the base address due to the configuration not being DLV11J compatible.

8. Line Time Clock

The on-board clock source may be configured as a 50, 60 or 800 Hz clock or the bus signal BEVENT can be used. The source is selected by entering the required option number as displayed on the screen followed by <CR>.

9. On-Board BootPROM

This option allows the BootPROM to be disabled. If this option is used the hardware setup is still loaded from the FLASH EPROM when the system is initialised. The setup bypass switch SW1 must be used to regain access to the on-board FLASH EPROM to allow any further changes to be made to the on-board firmware. Note that the PCR resident at 177520 octal is also disabled if the on board BootPROM is disabled.

10. Power-up Mode

There are four power-up modes which can be selected by entering one of the options from table 5-2 below.

TABLE 5-2 POWER-UP MODE OPTIONS

0	Trap through location 24 octal
1	Enter console ODT
2	Power-up to location 173000 octal
3	Power-up to the user specified power-up address

11. Power-up Address

The user may configure the most significant 7 bits of the power-up address. In order for this address to apply, power-up mode option 3 must be selected. The address is entered as a sixteen bit octal number followed by <CR>. Note that the MMU is turned off on power-up and as a result the SBC M1 module has a sixteen bit address range.

12. On-Board Parity CSR Address

The parity CSR on the SBC M11 module allows program control of certain memory parity functions and contains diagnostic information if a parity error occurs in the on-board memory system. The on-board memory CSR may be assigned one of the word addresses in the range 172100 octal to 172136 octal which allows for sixteen memory CSR's. Since the on-board memory starts at location 0, the CSR is assigned as default the first address in this range. Additional Q-bus memory cards will have their parity CSR's in ascending order following their base address.

The user is prompted for an address in the range indicated above and the address is entered as a sixteen bit octal number followed by <CR>.

13. Halt Option

Indicates how a HALT instruction is executed in KERNEL mode. If clear the processor enters console ODT. If set the processor traps through location 4 and sets bit 7 of the CPU error register. This is selected by entering the required option as displayed on the screen followed by <CR>.

14. On-board Parity Enable

This option allows the generation of parity interrupts and aborts to be enabled/disabled. If disabled, the error is still logged in the parity CSR. The disabling of aborts is not recommended except for special applications.

15. Console Halt Enable

This option allows the user to configure whether or not the system will halt on receipt of a break from the console.

16. Memory Timeout Select

This option allows selection of memory timeout periods of 12.5us or 25 us. It should be set to 25 us if older Q-Bus devices cause bus timeouts at 12.5 us.

The following lists the module's factory hardware configuration:

1).	Serial Line Base address -	17776500 octal
2).	Serial Line Vector address -	300 octal.
3).	Serial Line Baud Rate -	9600.
4).	Serial Line Baud Rate -	9600.
5).	Serial Line Baud Rate -	9600.
6).	Serial Line Baud Rate -	9600.
7).	Onboard Console -	Enabled.
8).	Line Time Clock Frequency -	60Hz.
9).	BootPROM -	Enabled.
10).	Power-up Mode-	173000 octal.
11)	User Power up Address -	000000
12).	Parity CSR address -	17772100 octal.
13)	Halt option -	Cleared
14)	On Board Parity -	Enabled
15)	Console Halt Enable -	Enabled
16)	Memory Timeout Select -	24 us

5.5.5.2 Modify Software Setup

This allows the configuration of power-up action, console type, diagnostics run at power-up, and non-standard device CSR assignments. When the software setups are modified they take effect immediately, however a save operation must be implemented to retain them. The displayed menu with the factory configured option settings is as shown below:

```
1 BOOT OPTION. . . . . .Dialogue
2 AUTOBOOT LOOP/EXIT OPTION. . . .Loop
3 CONSOLE TYPE . . . . . .DUMB
4 DISABLE ALL DIAGNOSTICS. . . . .NO
5 ENABLE EXTENDED TESTING. . . . .NO
6 ENABLE LINE TIME CLOCK . . . . .Disabled
7 ALLOW NON-STANDARD BOOT BLOCK. .Disabled

To select an option, enter the required number followed by <CR>.
```

1. Boot Option

This allows the user to determine whether the SBC M1 will power-up in dialogue mode where the main menu is displayed or attempt to boot from devices listed in the auto-boot configuration table (refer to section 5.5.5.5).

2. Console Type

With this option the user may determine the type of terminal with which the system is to interact. If ANSI mode is selected (Option 1) the bootstrap will use ANSI escape sequences for cursor positioning. Option 0 should be selected if the console terminal does not support ANSI escape sequences or is a hard-copy terminal. Factory default is dumb mode.

Note : VT100 terminals support ANSI escape sequences.

3. Disable All Diagnostics

Board diagnostics are executed at power-up. These diagnostics are intended to provide confidence in the operation of the board and are not for fault isolation.

The following tests are performed

- Low memory 0-64 K.
- Existence and operation of I/O page registers.
- Basic CPU functionality - All GP registers etc.
- BootPROM checksums and PCR.
- MMU.
- Console SLU.
- Memory parity register.
- Basic memory test.

If the user requires no diagnostic tests to be performed the option "1" should be selected followed by <CR>. However, it is recommended that these tests be kept enabled.

4. Enable Extended Testing

When selected, this option provides an extended memory test, which is run in conjunction with the standard diagnostics. This test verifies the integrity of all available system memory and the existence and operation of the fixed I/O page registers. (Refer to Table 5-3).

TABLE 5-3 FIXED I/O PAGE REGISTERS

Address	Register
172200 to 172376	Page address and page descriptor registers
172516	MMR3
173000 to 173776	BootPROMs
177546	Line time clock
177560 to 177566	Console registers
177520	Page control register
177572 to 177576	Memory management registers
177600 to 177676	Page address and page descriptor registers
177744	Memory system error register
177746	Cache control register
177750	Maintenance register
177752	HIT/MISS register
177766	CPU Error register
177772	Program interrupt request
177776	Processor status word

5. Enable Line Time Clock

This option allows the user to enable the line time clock on the SBC M1. The line time clock interrupts at PR6 while the bootstrap executes at PR7, therefore all LTC interrupts are ignored. When control is relinquished to the primary bootblock it must cater for LTC interrupts either by executing at or above PR6, disabling the LTC or providing an interrupt service routine at the LTC vector 100 octal.

Note: **DEC operating systems primary bootstraps execute at PR0, therefore the LTC must be disabled on booting these systems.**

6. Allow Non-standard Boot Block

When the standard boot block option is enabled, primary code is checked to ensure that the first instruction is NOP (240 octal). If this test fails an error message is displayed to indicate that the media cannot be booted. If the non-standard boot block option (option 1) is selected, this test is dispensed with and control is passed unconditionally to the primary bootstrap.

5.5.5.3 Save Modified Setup

This option must be selected in order to save any hardware or software modifications to the board. When selected, a message "SAVE IN PROGRESS PLEASE WAIT" is displayed after which control is returned to the setup menu. Software alterations take effect immediately. Modifications to hardware only take effect if the module has been powered-up again with SW1 in position 'B'.

5.5.5.4 Initialise To Factory Setup

The SBC M1 Programmable Hardware and Software configuration is restored to factory setting when this option is invoked. In order for this configuration to be retained on power-up it must be saved by selecting option 3 from the "SETUP MENU".

5.5.5.5 Configure Autoboot List

The user may configure a list of up to six devices in the order in which it is desired to attempt to boot them. If the list has not been configured all entries are shown as unused and the user is prompted to modify the list. The configuration menu is as shown below in table 5-4.

TABLE 5-4 AUTOBOOT CONFIGURATION

	DEVICE	LOWEST UNIT	HIGHEST UNIT
1	DU	0	10
2	DL	0	2
3	Unused		
4	Unused		
5	Unused		
6	Unused		

In order to delete a device from the list it should be selected and <CR> alone entered as the response to the prompt for the device mnemonic.

Note : There is a NL mnemonic which may be used as the first device to provide a delay for some peripherals to come online after power up. The use of this device is not normally necessary. If needed it should be configured with a highest unit number of 0. The lowest unit number should be configured to specify the delay required. A unit number of 1 provides approximately 0.75 seconds delay (dependent on clock frequency) and a unit number of 30 provides 24 * 0.75 seconds delay (Note unit numbers are octal). It may also be useful to use this device to allow users to enter <CTRL/C> before a real auto-boot is entered.

5.5.5.6 Configure Device Translations

The boot software may be configured to allow for non-standard CSR addresses by use of the device translation table. This table contains a list by mnemonic of device types with the lowest and highest unit numbers to which the entry applies and the corresponding CSR address. When booting the software initially scans this table and if an entry is found corresponding to the device from which it is attempting to boot the CSR in the table is used, otherwise the default standard CSR is used. Only 6 entries are allowed in the table and the menu is similar to the auto-boot configuration.

TABLE 5-5 DEVICE TRANSLATION TABLE

DEVICE	LOWEST UNIT	HIGHEST UNIT	CSR
1 DU	0	10	172150
2 DL	0	2	174400
3 Unused			
4 Unused			
5 Unused			
6 Unused			

To select a specific device, enter the appropriate device number followed by <CR>.To exit from this option, enter <CR>.

Note : The bootstrap device table contains an entry for the maximum number of devices per controller, if no entries for a mnemonic exist in the device translation table the unit number entered by a user is validated to be in the range 0 to n-1. If an entry exists in the device translation table for the unit number entered it is validated against the range given in the table entry.

As each device translation table entry is assumed to correspond to one controller with one CSR the lowest unit number in the table entry is subtracted from the unit number entered to give the device number within the controller before it is passed to the device specific bootstrap.The one slight exception to the above rule is that the standard bootstrap table supports 4 MS units as there are 4 sequentially assigned fixed CSRs in the I/O page.

5.5.5.7 Exit Setup

Select this option to return to main menu.

5.5.6 Test - Enter A Continuous Test Mode.

In this mode it is assumed that the SBC M1 module is in a valid hardware configuration. Diagnostics are continuously executed until <CTRL C> is entered by the user. At this point control is returned to the main menu on completion of the current diagnostic.

5. 6 BOOTPROM MAPPING

The FLASH EPROM is mapped using a page control register at location 17777520 octal. The PCR functions as two separate halves. The low byte is used as bits 8 to 14 of the EPROM address for addresses in the range 173000 to 173377 and the high byte as bits 8 to 14 of the EPROM address for addresses in the range 173400 to 173777.

Bits 8 to 14 of the PCR provide a total of 128 windows of 256 bytes each. Of these 128 (0-127) are used to map the EPROM and one (127) is used to map the setup data. The setup data is byte wide with the least significant byte being valid. This provides 128 bytes of EPROM and 31.75 K bytes of BootPROM. The first 8 bytes of setup data are reserved for hardware configuration. These bytes are read by the SBC M1 power-up circuitry unless the configuration bypass switch (SW1) is on. The definition of these bytes is hardware defined and they must contain a valid configuration.

5. 7 USAGE OF BOOTPROM WINDOWS

Windows 0 and 1 are allocated for use by the code, which relocates the remaining code to RAM. These two windows relocate the contents of all of the remaining windows. The format of the remaining windows is such that the first word contains the load address i.e. the address at which the code is to be loaded. In order to provide a degree of testability the last 2 bytes of each window in the BootPROMs are reserved locations for diagnostic purposes. Byte 377 octal is the window number, this is used to test the functioning of the PCR. Byte 376 octal is an exclusive-OR checksum to validate the integrity of the EPROMS.

As the setup data is mapped to the low byte only, the checksum is in byte 376 octal as normal and no block number is provided. The overheads in the windows mean that the effective window size is 252 bytes. As two windows are allocated for code relocation to RAM the effective upper limit on the actual code size for the main code is 124x252 = 31248 bytes or just over 30 Kb. The physically resident setup data and Boot Code are in one 29F010 device but the Boot Code is in hardware protected sectors and appears to be 16 Bits wide to the software.

5. 8 CODE OVERVIEW

The operation of the boot software proceeds as follows:

1). A test is performed on low memory.

2). The basic trap vectors are set up.

3). 16 bit memory space is tested.

4). The EPROM code is transferred to RAM.

5). Control is transferred to the code in RAM.

6). If boot is selected the requested bootstrap is searched for and if found, it is invoked.

7). If the boot block is valid or the non standard boot block format is enabled control is passed to the boot block.

This method of operation requires that the first one or two windows of the Boot Code contain code specifically written for execution in those windows to perform basic testing and relocate the remaining code. The remaining code is transferred to RAM at address 10000 and control is transferred to this. The setup data cannot be relocated in the same manner as the remaining code as only the low byte is valid and it has a different format. It is therefore specifically unpacked into a formatted area of RAM.

5. 9 DEVELOPMENT UTILITIES

A utility program is used to process a number of RT11 load-able absolute binary files to a HEX ASCII PROM file. The boot code is developed and tested in RAM under RT11. It is transferred to VAX/VMS by using the VMS EXCHANGE utility. The Mentec PROM FORMAT utility is then used to format the code. This utility program is written in VAX FORTRAN.

6. SYSTEM ARCHITECTURE

6.1 INTRODUCTION

This chapter describes the architecture of the SBC M1 with special reference to how the M1 interfaces with other system components.

6.2 PROCESSOR MODES

There are three processor modes - Kernel, Supervisor and User. Each one has a different degree of control over the operation of the M1. They are chosen by setting bits 14 and 15 in the Processor Status Word (PSW). The existence of different processor modes allows security to be implemented in a multi-programming environment. For example, WAIT, RESET and HALT statements can only be executed in Kernel mode. Certain bits in the PSW may only be written to in Kernel mode. (Refer to section 6.4.1.1). Thus, non-privileged users are kept from having too much control over the system.

6.3 GENERAL PURPOSE REGISTERS

The M1 has sixteen general purpose registers. These registers do not reside in the address space. Twelve of the registers are true general purpose registers. These are arranged as two sets, R0 to R5 and R0' to R5'. Only one of these sets is available to the user at any one time. The choice is made by setting bit 11 in the Processor Status Word. These registers may be used as accumulators or as base or index registers for memory addressing. The existence of two sets means that fast context switching is possible. There are three registers used as stack pointers - one for each of the operating modes. Thus there is a kernel stack pointer (KSP), a supervisor stack pointer (SSP) and a user stack pointer (USP). The mode is chosen by setting bits 14,15 in the PSW and the stack pointer is then referred to as register R6.

The stack moves downwards in memory when items are pushed on to it. The stacks can be used to provide linkage information when the processor modes are switched. The M1 provides hardware stack protection for the Kernel stack. Yellow and Red stack traps are described in table 6-3. The final register is the program counter (instruction pointer). It is incremented by two every time a word is fetched from memory. It is accessed as register R7. R7 may also be used as a base or index registers for addressing. This has the effect of extending the power of the addressing modes.

6.4 SPECIAL PUROSE REGISTERS

As well as the general purpose registers the SBC M1 module implements a set of special purpose registers. These registers are used by the user to set some of the operational features of the system or by the system to provide status information to the user.

There are four sub-divisions of special purpose registers. These are the internal registers, System registers, External Registers and Power-up Register. They all differ from the General Purpose Registers in that they have addresses in the 4K words of memory reserved for I/O addresses (the I/O Page).

6.4.1 Internal Registers

The Internal Registers are so named because they are implemented in the logic of the M1 itself. Unlike the General Purpose Registers, however, the user accesses them by addressing locations in the I/O page. Table 6-1 lists the internal registers. The Processor Status Word and CPU Error Register are described here. Descriptions of the other registers are reserved until the relevant sections of the architecture are being described.

TABLE 6-1 INTERNAL REGISTERS

Abbrv.	Register	Address
PSW	Processor Status Word	17777776_8
PIRQ	Program Interupt Request Register	17777772_8
CPUERR	CPU Error Register	17777766_8
HMR	Hit /Miss Register	17777752_8
-	Memory Management Registers	*
-	Floating Point Registers	**

* Refer to Appendix C.
** Floating Point Registers do not have addresses they are referenced using special instructions.

6.4.1.1 Processor Status Word

The Processor Status Word (PSW) contains information about current processor staus. It also contains information about the result of the current instruction. By writing to it the user can provide the M1 with information about how it is to run. Figure 6-1 gives a schematic of the PSW. Table 6-2 explains each bit in detail.

TABLE 6-2 PROCESSOR STATUS WORD

Bit	Name	Description
15:14	Current Mode (R/W)	The Status Of these bits indicate the current processor mode as follows: Bits 15 14 — Mode 0 0 — Kernel 0 1 — Supervisor 1 0 — N/A 1 1 — User
13:12	Previous Mode (R/W)	These bits indicate the previous processor mode and have the same meanings as bits 15 and 14.
11	Register Set (R/W)	If Bit 11 is 0 then R0-R5 are used. If Bit 11 is 1 then R0'-R5' are used.
10:09	Unused (Read Only)	These bits are unused and read back as 0's
08	Reserved	
07:05	Priority	These bits are read as a 3 bit binary number with bit 5 as the Least Significant Bit. An interrupt needs a priority greater than this number before it can interupt the processor.

TABLE 6-2 Contd. PROCESSOR STAUS WORD

Bit	Name	Description
04	Trace Trap	If this bit is set then the processor traps to location 14 at the end of the instruction currently being executed. The bit may not be set directly - it must be set via an RTI or RTT instruction.
03	N (Read Only)	This bit is set if the result of the previous operation was negative.
02	Z (Read Only)	This bit is set if the result of the previous operation was 0.
01	V (Read Only)	This bit is set if the previous operation resulted in an arithmetic overflow.
00	C (Read Only)	This bit is set if the Most Significant Bit of the result of the previous operation was carried.

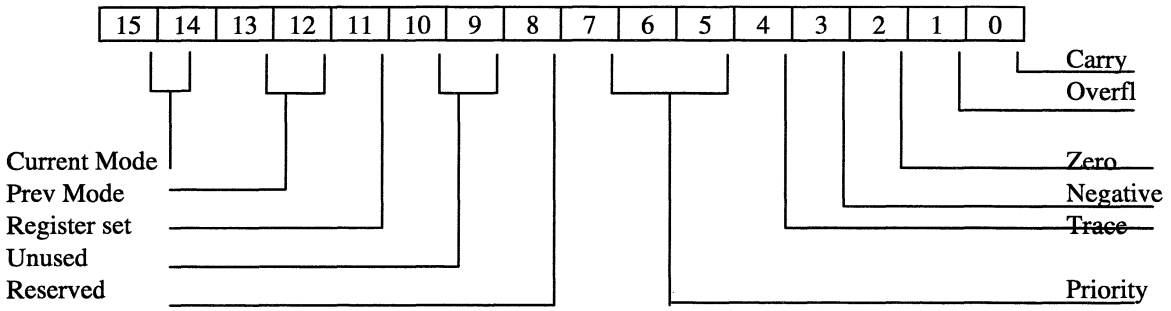


Figure 6.1 Processor Status Word.

6.4.1.2 The CPU Error Register

The M1 traps to location 4 when a CPU error occurs. The CPU error register is used to log the nature of the error. Only bits [7:2] of the CPU error register are used all of the other bits return 0's when read. The CPU error register is summarised in Table 6-3 and Figure 6.2.

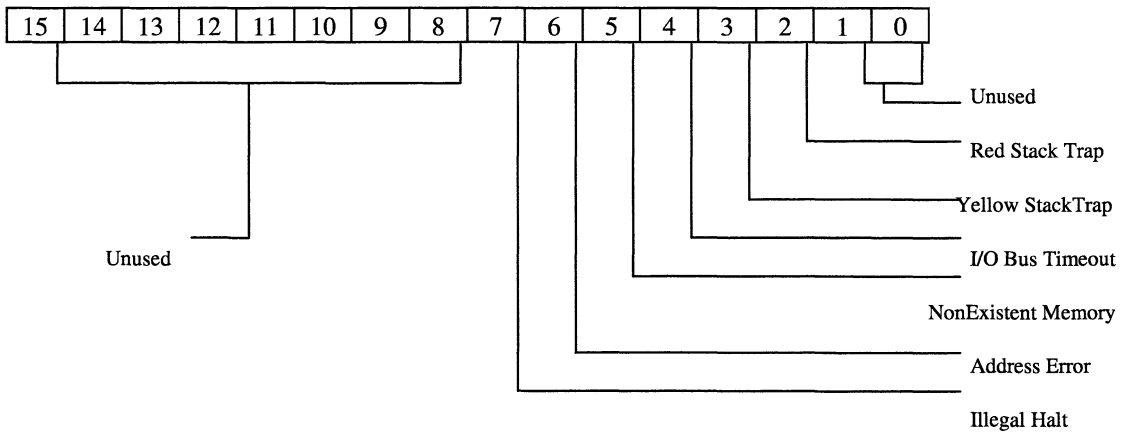


Figure 6.2 CPU Error Register.

TABLE 6-3 CPU ERROR REGISTER

Bit	Name	Description
15:08	Unused	Return 0's when read.
07	Illegal HALT	A HALT instruction is illegal if executed in user or supervisor mode. A trap 4 will occur and this bit will be set. A HALT will cause this sequence of events in all three modes if bit 3 in the power-up configuration register is set.
06	Address Error	A trap to 4 will occur if an attempt is made to address a word with an odd address or if an attempt is made to fetch an address from an internal register. Bit 6 in the CPU error register is set in these instances.
05	Non-Existent Memory	An attempted access to a memory location which does not exist will cause a trap to 4. Bit 5 of the CPU Error Register is set. If the location is in the I/O page then bit 4 is set instead.
04	I/O Bus Timeout	If a non-existent location is in the I/O page then bit 6 is set.
03	Yellow Stack Trap	Set when a yellow zone stack trap occurs i.e. when a Kernel stack reference has a virtual address of less than octal 400
02	Red Stack Trap	If a Kernel stack abort occurrs during an interrupt, trap or abort sequence then a red stack trap is flagged and locations 0 and 2 are used as an emergency stack, vectoring through location 4.
01:00	Unused	Return 0's when read.

6.4.2 System Registers

The registers classed as system registers have addresses in the range 17777740$_8$ to 17777750$_8$. The SBC M1 has three system registers; the Maintenance Register, the Memory Error Register, and the Cache Control Register. Table 6-4 gives the addresses of these registers.

The Cache Control Register, the Memory Error Register and Hit Miss Register are implemented for compatibility and have no effect on system operation and are not described further.

Some operating systems check for the existence of the Maintenance Register and this is the main reason for its inclusion. The Maintenance Register is described in section 6.4.2.1.

6.4.2.1 The Maintenance Register

The Maintenance Register (MR) has the same bit definitions as the Power-up and Configuration Register. The latter is equivalent to the DCJ11's external register and is described in section 6.4.4.

TABLE 6-4 SYSTEM REGISTERS

Abbrv.	Register	Address
MR	Maintenance Register	17777750$_8$
MER	Memory Error Register	17777744$_8$
CCR	Cache Control Register	17777746$_8$

6.4.3 The External Registers

These are the Line-Time Clock Register, The Parity Control and Status Register (PCSR) and the Page Control Register (PCR). Table 6-5 lists the external registers.

TABLE 6-5 EXTERNAL REGISTERS

Abbrv.	Register	Address
LTC	Line-Time Clock Register	17777546$_8$
PCSR	Parity Control and Status Register.	177721XX$_8$
PCR	Page Control Register	17777520$_8$

6.4.4 The Power-Up Register

As part of the M1 power-up diagnostic routine it reads the Power-Up register using a unique instruction. Table 6-6 describes the information relayed to the

TABLE 6-6 POWER-UP REGISTER

Bit	Name	Description
15:09	Boot Address	These bits represent the address from which the M1 is to start executing boot code, bits 00:08 of the address are always logic zero.
08	Unused	This bit is unused on the M1
07	-	Reserved for future use.
06:04	Processor Type	These bits are read by operating systems to determine the processor type. (Maintenance Register)
03	Halt Option	This bit determines the action to be taken by the M1 on receipt of a halt instruction : 0 - Enter Console ODT 1 - Trap Through Location 4.

TABLE 6-6 contd. POWER-UP REGISTER

Bit	Name	Description
2:1	Power-up mode	The M1 uses these bits on power-up to determine which of the following actions is to be taken Bits: 2 1 — Mode 0 0 - Trap through location 24_8 0 1 - Enter console ODT 1 0 - Power-up to 173000_8 1 1 - Power-up to user specified address bits 15:09
0	POK	This bit is asserted by on-board logic to inform the M1 that the system power is at an acceptable level.

The Maintenance Register, which can be read by the user, will display the same information as the power-up mode register except that bits 09:15 are read back as logic zero ,since they are used by operating systems to determine the hardware configuration of the system.

6.4.5 The Program Interrupt Request Register

The Program Interrupt Request Register (PIRQ) can interrupt the processor at any one of the seven levels of interrupt priority. An interrupt will occur if one of the bits [15,9] in the PIRQ is set. The PIRQ has two sets of read only bits which hold the binary value of the priority. The vector for a trap instigated by the PIRQ is 240.

Table 6-7 describes each bit in the PIRQ. Figure 6.3 shows the PIRQ in schematic form.

TABLE 6-7 PROGRAM INTERRUPT REQUEST REGISTER

Bit	Name	Description
15:9	PIR7 to PIR1 (R/W)	When bit 15 is set, an interrupt with priority level of 7 is requested. Bits 14 down to 9 are used to request an interrupt with priority level 6 and so on down to a priority of 1.
7:5	- Read only	Contains the binary value of the highest program interrupt pending.
3:1	- Read Only	These bits hold the same information as bits 7:5.

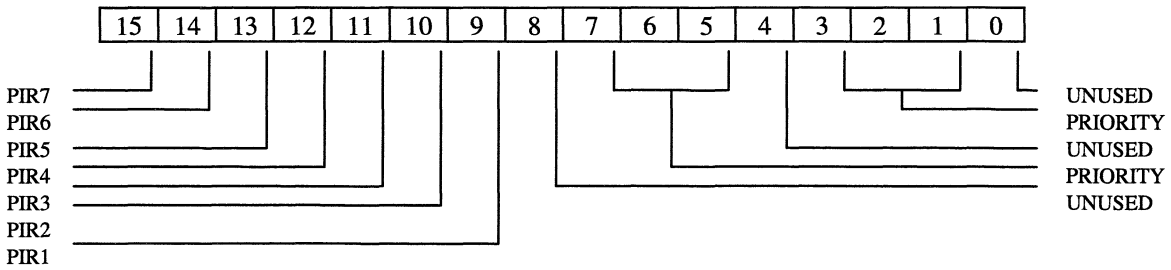


Figure 6.3 Program Interrupt Request Register.

6.5 MEMORY MANAGEMENT

NOTE: Refer to Appendix C, Table C-6 for addresses of Memory Management Registers.

The M1 is a sixteen-bit machine. This basically limits the virtual address space to 64k bytes. The M1 Memory Management Unit (MMU) allows the effective memory to be expanded. The MMU maps a sixteen bit virtual address space (64 Kb) to a twenty-two-bit physical address space (4 Mb) using a paging system. The user can decide where each page is to reside in physical memory by writing to registers in the MMU. The only restriction on the mapping of virtual addresses to physical memory is that they should start at locations which are multiples of 64 bytes.

6.5.1 Active Page Registers

The user decides where the pages are to be mapped by writing to the Active Page Registers. The MMU maintains one of these registers for each page that it maps. Each one consists of two sixteen-bit registers, the Page Address Register (PAR) and the Page Descriptor Register (PDR).

Each processor mode can map eight pages. This gives twenty-four Active Page Registers. If the Instruction/Data space mode of operation is enabled (Refer to Table 6-10), then these twenty-four pairs are used to map to the instruction Space and a further twenty-four are available to map to the Data Space. The Instruction/Data space mode of operation is described in section 6.5.4.

6.5.1.1 Page Address Register

This register contains the block number in physical memory to which the page is to be mapped.

6.5.1.2 Page Descriptor Register

The PDR allows the user to set some of the features of the mapped page. It is described in Table 6-8 and Figure 6.4.

TABLE 6-8 PAGE DESCRIPTOR REGISTER

Bit	R/W	Description
15	R/W	If this bit is set then reference to this page will bypass cache. No effect on M1.
14:08	R/W	The length of the page in blocks is contained in bits 14:8. An attempt to access data in a longer page will lead to a page length abort.
07	R	Reserved for future use.
06	R	If this bit is set then the page has been written to since the last time its PAR or PDR was modified.
05:04	R	Reserved for future use.
03	R/W	This bit indicates in which direction the page expands. When set to a 1 the page will expand downwards.
02:01	R/W	Access Control Field. These bits represent a code: 00 Non Resident - Abort all. 01 Read Only - Abort on write. 10 Unused - Abort all. 11 Read/Write - Full Access.
00	R	Reserved for future use.

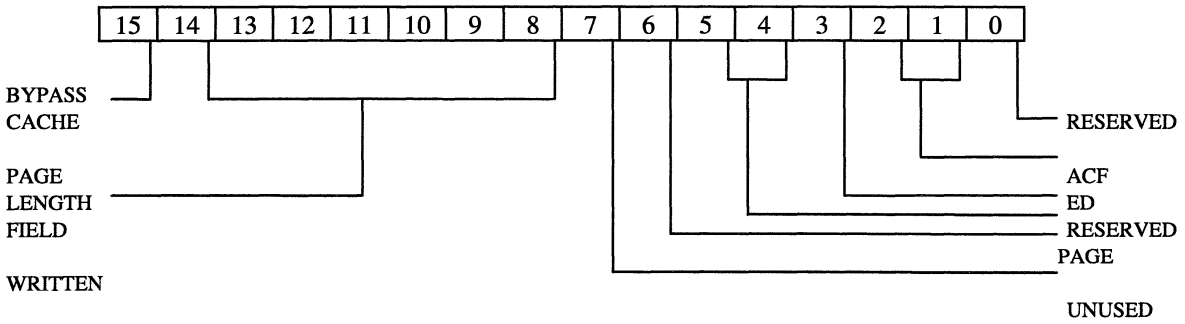


Figure 6.4 Page Descriptor Register.

6.5.2 The Memory Management Registers

The user interacts with the MMU through a series of registers in the I/O page. There are four status and control registers - MMR0-3. These are used to enable and disable the MMU and to decide some other features of its operation.

6.5.2.1 Memory Management Register 0

Memory Management Register 0 gives status and control information for the memory management unit, refer to Figure 6.5 and Table 6-9.

TABLE 6-9 MEMORY MANAGEMENT REGISTER 0

Bit	Access	Description
15	R	If an attempt is made to access a non-resident page then an abort will occur and this bit 15 will be set. When set the contents of MMR1/MMR3 are frozen.
14	R	MMU will abort if program tries to access memory beyond the page length indicated in the PDR. Bit 14 will also be set
13	R	If an attempt is made to access a page which has been set as read only then an abort will occur and bit 13 will be set.
12:07	R	Reserved for future use.
06:05	R	Indicates which processor mode is causing the abort. Code is same as that for PSW.
04	R	I/D Error.
03:01	R	These bits contain the number of the page causing the abort in binary form.
* 00	R/W	This bit must be set if the MMU is to be enabled.

*** NOTE: This bit must be set to 1 if MMU is to be used since the M1 powers up as a sixteen-bit machine.**

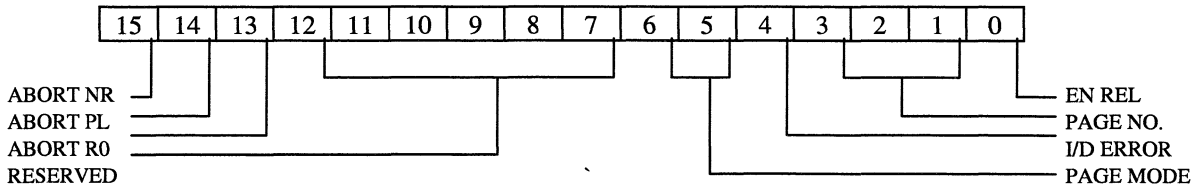


Figure 6.5 Memory Management Register 0.

6.5.2.2 Memory Management Register 1

If a memory management trap occurs then Memory Management Register 1 (MMR1) records any changes to the general purpose registers. Figure 6.6 gives the format of the register. The register number is given in binary form. The amount by which the register has changed is given in 2's complement format.

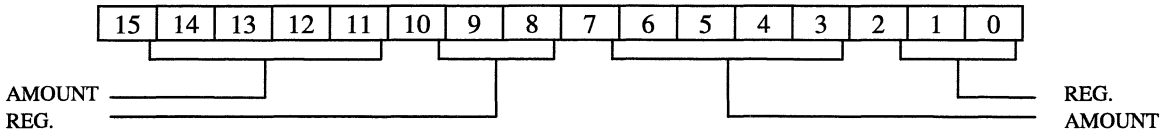


Figure 6.6 Memory Management Register 1.

6.5.2.3 Memory Management Register 2

Memory Management Register 2 (MMR2) holds the virtual address of the instruction which is currently being fetched.

6.5.2.4 Memory Management Register 3

Memory Management Register 3 (MMR3) gives further status and control information. It is summarised in Figure 6.7 and Table 6-10.

TABLE 6-10 MEMORY MANAGEMENT REGISTER 3

Bit	Description
15:06	Reserved for future use - always read back as 0.
05	Unused
04	If this bit is 0 when the MMU is enabled then 18-bit mapping is used. To enable 22-bit mapping the bit should be set to a 1.
03	Enable CSM instruction.
02	Enable Kernel Data Space
01	Enable Supervisor Data Space
00	Enable User Data Space

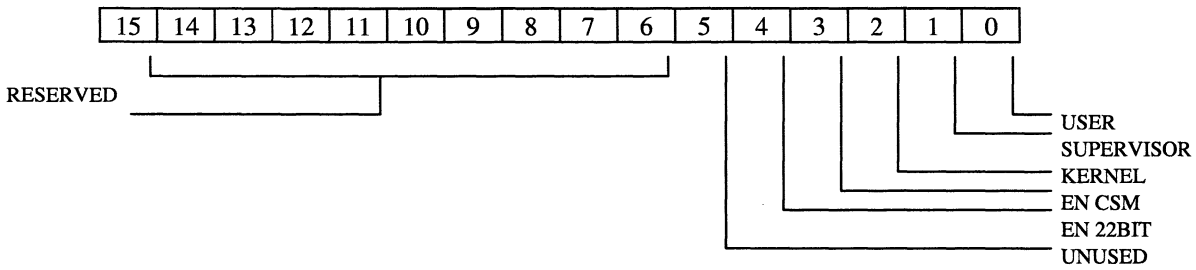


Figure 6.7 Memory Management Register 3.

6.5.3 *Mapping from Virtual to Physical Memory*

The mapping procedure is now considered. The MMU contains a PAR for every page that it maps. The three most significant bits in the virtual address are used to choose between the pages. The number in the PAR must be shifted six bits to the left to give the address in physical memory to which the page is to be mapped. The sixteen Least Significant Bits of the virtual address are used as the displacement within the page. The mapping procedure is summarised in Figure 6.8.

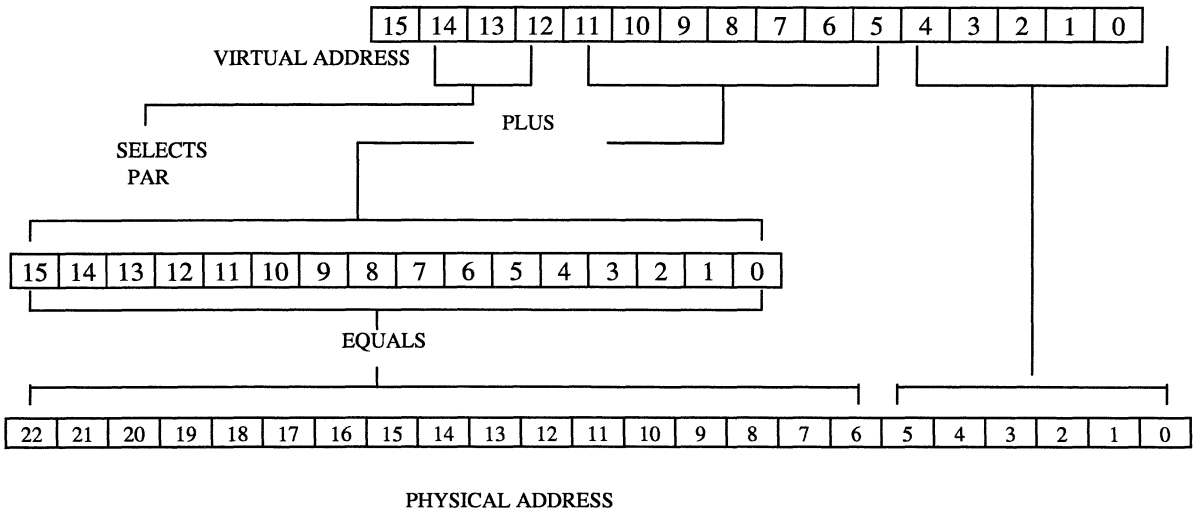


Figure 6.8 Virtual To Physical Address Mapping.

6.5.4 *Instruction and Data Space*

The Instruction/Data space mode of operation can be enabled through the memory management registers. In this mode of operation, the user has access to sixteen pages instead of the normal eight. Eight of the pages are reserved for data and eight are reserved for instructions.

6.6 SBC M1 MEMORIES

The SBC M1 memories are as follows

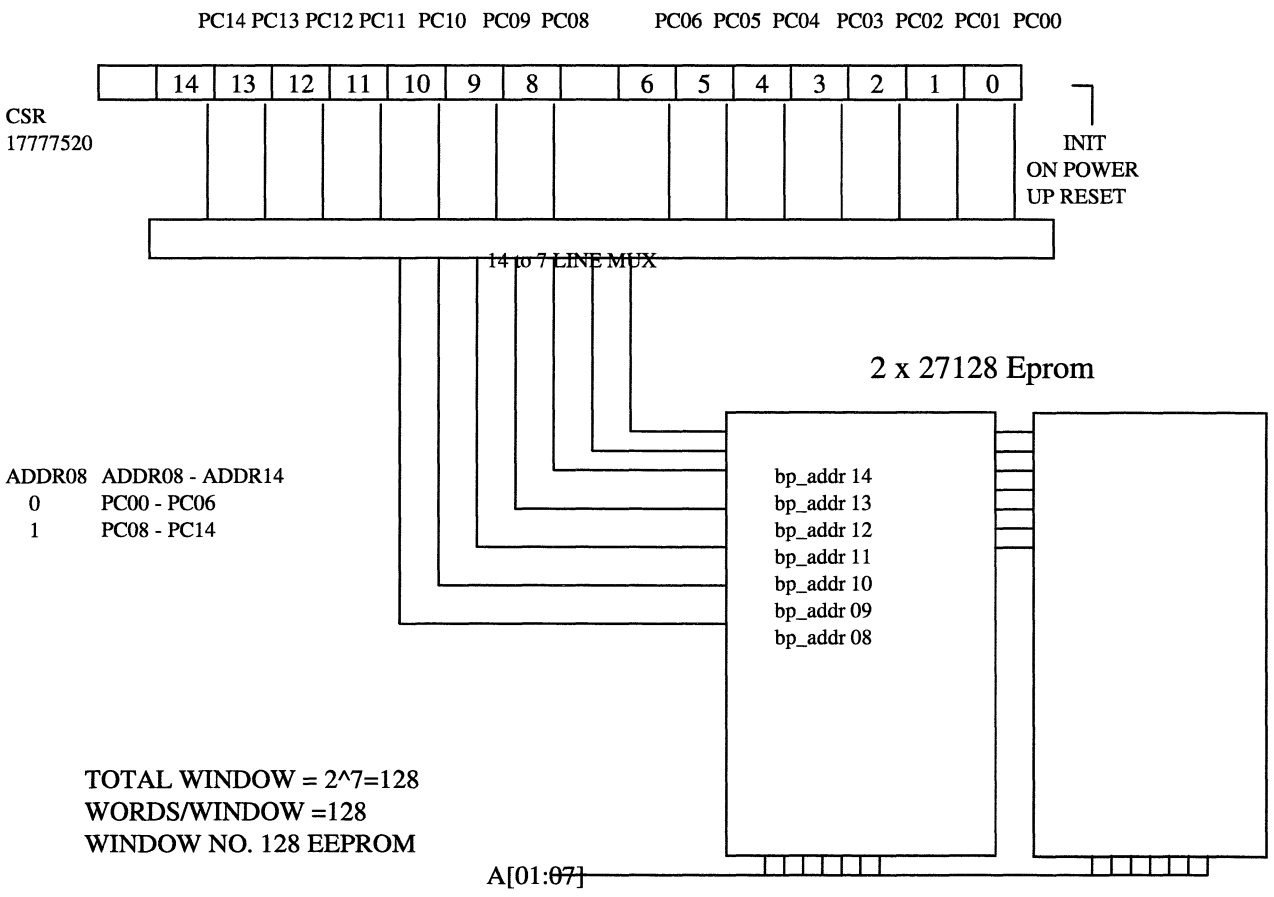
1 - Main Memory SRAM 4 M/Bytes
2 - Eprom (Boot Code user setups)

6.6.1 Main Memory

The main memory system on the SBC M1 is 4 MegaByte of non-Parity SRAMS.

6.6.2 BootProm

The SBC M1 module permits 32K bytes of BootPROM to be accessed. through the 1/2K byte window in the I/O page (17773000_8 to 17773776_8) using the Page Control Register. (refer to section 6.9).



TOTAL BOOT CODE SPACE 128 WORDS X 127 WINDOWS = 31.75KBYTES.
TOTAL EEPROM ADDR. SPACE 128 BYTES X 1 = 128 BYTES.

Figure 6.9

6.7 EPROM STORAGE AND USE

The first 6 bytes of SETUP are reserved for hardware configuration. These bytes are read by the SBC M1 power-up circuitry unless the configuration bypass switch SW1 is on. The definition of these bytes is hardware defined and they must contain a valid configuration. The remaining 122 bytes are software defined.

6.8 PROGRAM CONTROL OF THE LINE-TIME CLOCK

The line-time clock function is controlled through the LTC register, addressable at location 17777546_8. Bits <15:7,5:0> are not used and are always read as logical zeroes. Writing to these bits has no effect on the CSR. Bit <6> is used to control line time clock interrupts. It must be set to 1 to enable clock interrupts. This is done by writing 100_8 to the register. Note that the bit is cleared on power-up. It will also be cleared by a RESET instruction. The line-time clock is a read/write register. There are four clock sources available for the LTC, refer to section 5.5.5.1 on how to select a source.

6.9 PAGE CONTROL REGISTER FOR BOOTPROMS

The EPROM and EEPROM are mapped using a page control register at location 17777520_8. The register format and ROM address calculation are shown in figure 6.9.

The PCR functions as two separate halves. The low byte is used as bits 8 to 14 of the EPROM address for addresses in the range 173000_8 to 173377_8 and the high byte as bits 8 to 14 of the EPROM address for addresses in the range 173400_8 to 173777_8.

The 7 bits of the PCR provide a total of 128 windows at 256 bytes each. Of these 127 (0-126) are used to map the EPROM and one (127) is used to map the EEPROM. The EEPROM is byte wide with the least significant byte being valid. This provides 128 bytes of EEPROM and 31.75K bytes of EPROM.

6.10 PARITY MEMORY CONTROL AND STATUS BIT ASSIGNMENT

The CSR allows program control of certain memory parity functions and contains diagnostic information if a memory parity error has occurred. The address of the CSR is assigned from one of the 16 selectable addresses using the configuration option in the boot software. The CSR should be assigned the first address when off-board memory parity CSRs exist. The order of CSR address assignment should follow the order of the addressing of the memory modules. Bits <15,2,0> are reset on power-up or BUS INIT. This signal is asserted on power-up and in response to RESET instruction. The CSR assignments are listed in Table 6-13 and shown in Figure 6.12.

TABLE 6-13 PARITY CONTROL REGISTER

Bit	Description
Bits 1,3,4,12,13	These bits are not used and are always read as logical zeroes. Writing into these bits has no effect on the CSR.
Bit 0	Parity Error Enable - If a parity error occurs on a DATI or DATIO(B) cycle to memory and bit 0 is set, then a parity abort trap occurs to location 114_8. This is a read/write bit reset to zero on power-up or BUS INIT.
Bit 2	Write Wrong Parity - If this bit 2 is set = 1 and a DATO or DATOB cycle to memory occurs, wrong parity data is written into the parity RAMs. Bit 2 can be used to check the parity error logic as well as failed address information in the CSR.

TABLE 6-11 contd. PARITY CONTROL REGISTER

Bit	Description
Bit 5-11	Error Address Bits - If a parity error occurs on a DATI or DATIO(B) cycle, then A11-A17 are stored in CSR bits <5:11> and bits A18-A21 are latched. CSR bit <14>=0 allows the logic to pass A11-A17 to the processor. The program then sets CSR bit <14> = 1. This enables A18-A21 to be read from CSR bits 05-08. The parity error addresses locate the parity error to 1K segment of memory. These are read/write bits and are not reset to zero via power up or BUS INIT. If a second parity error is encountered the new failed address is stored in the CSR.
Bit 14	Extended CSR Read Enable Supra for use of this bit.
Bit 15	Parity Error - If bit 15 is set this indicates that a parity error has occurred. The bit mimics the Parity Led. The indicator provides visual indication of a parity error. This bit is a read/write bit. It is reset to zero via a power-up or BUS INIT and remains set unless rewritten or initialised.

PER	EXCSR	0	0	A17	A16	A15	A14 A21	A13 A20	A12 A19	A11 A18	0	0	WTWRP	0	PERENB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6.12 Parity CSR Bit Allocation.

7.4 SERIAL LINE REGISTERS

The serial line registers are now described in tabular form. Figures 7.3(a) to 7.3(d) give bit maps for the serial line registers. Tables 7-3 to 7-6 give bit descriptions (For addresses of serial line registers refer to Appendix C).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	rcv act	0	0	0	rcv done	rcv ie	0	0	0	0	0	0

Figure 7.3(a) Receiver Control and Status Register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	oe err	fr err	Par err	rcv brk	0	0	0								
(---------- RECEIVED DATA BUFFER----------)															

Figure 7.3(b) Receiver Data Buffer Register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	xmit rdy	xmit ie						xmit brk

Figure 7.3(c) Transmitter Control and Status Register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0								
(----------TRANSMIT DATA BUFFER----------)															

Figure 7.3(d) Transmitter Data Buffer Register.

TABLE 7-3 RECEIVER CONTROL AND STATUS BIT DESCRIPTION

Bits	Name	Direction	Function
12-15	Not used	Read only	Reserved for future use.
11	Receiver Active (RCV ACT)	Read only	This bit is set to a one by the start bit. It is cleared to a zero on power-up.
08-10	Not used	Read only	Reserved for future use.
07	Receiver done (RCV DONE)	Read only	This bit is set to a one when the byte received is transferred into the RCV data buffer. It is cleared to a zero when the RCV data buffer is read. It is cleared to zero on power-up.
06	Receiver Interrupt Enable (RCV IE)	Read/Write	This bit is set in software to enable RCV IRQ. The interrupt will occur when data has been received ie. when the RCV DONE bit has been set. It can be cleared by software. A power-up or bus reset will clear it.
00-05	Not used	Read only	Reserved for future use

TABLE 7-4 RECEIVER DATA BUFFER BIT DESCRIPTION

Bits	Name	Direction	Function
15	Error (ERR)		There are three errors associated with the use of RBUF - the overrun error the framing error and the parity error. These set this bit as well as bits 14, 13 and 12 respectively.
14	Overrun Error (OR ERR)	Read only	If a new character is placed in the received data buffer before the previous one has been read, this bit is set. Bit 7 of the RCSR (RCV DONE) is cleared by reading the buffer. The bit is cleared when the next character along is moved in. It is cleared on power-up.
13	Framing Error (FR ERR)	Read only	A framing error occurs if the serial line moves a byte into the buffer and is then unable to read a valid stop bit. This renders the character and the one following invalid. The next byte with a valid stop bit will cause the bit to be cleared. The bit is cleared on power-up.

TABLE 7-4 Contd. RECEIVER DATA BUFFER BIT DESCRIPTION

Bits	Name	Direction	Function
12	Not Used	Read only	This bit is reserved
11	Received break (RCV BRK)	Read only	This bit is used to indicate that the serial line has received a break. Cleared on power-up.
08-10	Not used	Read only	Reserved for future use.
00-07	Received data (RCV DATA BUFFER)	Read only	The 8 bits represent a data buffer which contains the last byte that was received. The bits are cleared on power-up.

TABLE 7-5 TRANSMITTER CONTROL AND STATUS DESCRIPTION

Bits	Name	Direction	Function
08-15	Not used	Read only	Reserved for future use.
07	Transmitter ready (XMIT RDY)	Read only	If set this indicates that the current character has been sent. A new byte may be placed in the XMIT data buffer. Writing the byte in the buffer will clear the bit. Cleared on Power-up.
06	Transmitter interrupt enable (XMIT IE)	Read/write	This bit can be set by software and enables XMIT IRQ The signal can be cleared under program control, by power-up and by bus reset.
01-05	None		Bits have no use on SBC-M1.

TABLE 7-5 Contd. TRANSMITTER CONTROL AND STATUS DESCRIPTION

Bits	Name	Direction	Function
00	Transmit Break (XMIT BRK)	Read/write	Used under program control to start communication with external devices. When the bit is set high Serial Out will be held low. The bit can be cleared by software. A power-up or bus reset will also reset it.

TABLE 7-6 TRANSMITTER DATA BUFFER BIT DESCRIPTIONS

Bits	Name	Direction	Function
08-15	Not used	Read only	Reserved for future use.
00-07	Transmit data buffer (XMIT DATA BUFFER)	Read/write	These 8 bits represent a data buffer which cont-ains the next byte to be transmitted. Writing a byte to this buffer causes the XMIT RDY bit in the XCSR to be cleared. Power-up will clear these bits

7.5 SERIAL LINE CABLES AND CONNECTORS

Each serial line interfaces to the outside world through a 2*5 pin AMP connector. The positions of these connectors are shown in Figure 4.1. Figure 7.4 shows the AMP connector pin numbers. The relevant signal connections are outlined in Table 7-7.

Most of the cables which are necessary for serial communications with peripheral devices are available from Digital Equipment Corporation. For example,

BC20N-05	A 5 foot RS-232 null modem cable
BC20M-50	A 50 foot RS-422, RS-423 cable

TABLE 7-7 SLU CONNECTOR PIN DESIGNATIONS

Pin	Designation
1	NC
2	GND
3	TX DATA+
4	GND
5	GND
6	INDEX KEY (no pin)
7	NC
8	RCV DATA+
9	GND
10	+12V (fused)

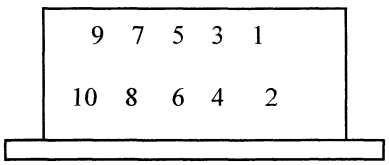


Figure 7.4 AMP Connector front view

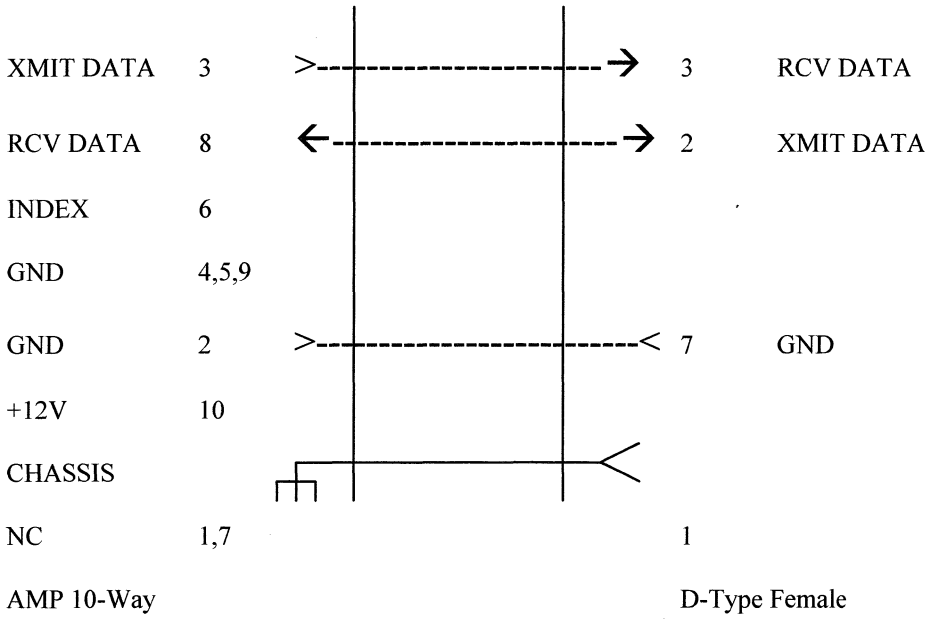


Figure 7.5 Null Modem Cable

7.5.2 User Cable Construction

This section outlines the factors which must be taken into consideration when designing a cable for use with the RS-232 standard.

To connect the SBC M1 module to RS-232-C terminal an AMP 2*5 female connector and a D-type male/female RS-232 connector is required.

A loopback to connect the inverted input of the differential receivers to ground is necessary. Pin 7 (Receive Data-) is normally connected to pin 9 (Ground). For the SBC M1 to communicate correctly with the terminal it is necessary to connect transmit data outputs to receive data inputs on the terminal and vice versa, i.e. the cable must be constructed as a null modem. Figure 7.4 and table 7-7 show where the relevant signals are on the AMP connector. Table 7-8 shows the signals on the D-type connector.

Pin 3 on the SBC M1 (Transmit Data+) should be connected to pin 3 on the D-type connector (RS-232 Received Data). Pin 8 on the SBC M1 (Received Data +) should be connected to pin 2 of the D-type connector (RS-232 Transmitted Data). Common the ground signals at each end by connecting Pin2 on the SBC M1 (Ground) to pin 7 on the D-type connector (RS-232 Signal Ground/Common Return). Lastly, a shield connection is made from the chassis containing the SBC M1 to pin 1 on the D-type connector (Protective Ground). The cable length limitations of RS-232 should not be neglected in designing the cable. These are shown in Table 7-1.

If the cable is to be used to join two SBC M1's or between one SBC M1 and a DL type device then two AMP female connectors are used and Table 7-5 is used to determine which pins should be connected to give a null modem configuration.

The following AMP/DEC parts will be needed if cables are being constructed:

1. Cable Receptacle:	AMP PN 87133-5	DEC PN 12-14268-02
2. Locking Clip:	AMP PN 87124-1	DEC PN 12-14267-00
3. Key Pin (pin 6)	AMP PN 87179-1	DEC PN 12-15418-00

TABLE 7-6 D-TYPE CONNECTOR PIN DESIGNATIONS

PIN	SIGNAL
1	Protective Ground
2	Transmitted Data
3	Received Data
7	Common Return/Signal Ground

Appendix A BACKPLANE PIN UTILISATION

TABLE A-1 COMPONENT SIDE (Side1)

Backplane Pin	SBC M1 Signal Function	LSI-11 Bus Signal Name
AA1	BIRQ5 L	BIRQ5 L
AB1	BIRQ6 L	BIRQ6 L
AC1	BDAL16 L	BDAL16 L
AD1	BDAL17 L	BDAL17 L
AE1	Not connected	SSPARE 1
AF1	SRUN	SRUN
AH1	Not connected	SSPARE 3
AJ1	GND	GND
AK1	NNot connected	MSPAREA
AL1	Not connected	MSPAREB
AM1	GND	GND
AN1	BDMR L	BDMR L
AP1	BHALT	BHALT
AR1	BREF L	BREF L
AS1	Not Connected	+5B
AT1	GND	GND
AU1	Not connected	PSPARE 1
AV1	Not Connected	+5B
BA1	BBDCOK H	BDCOK H
BB1	BPOK H	BPOK H
BC1	BDAL18 L	BDAL18 L
BD1	BDAL19 L	BDAL19 L
BE1	BDAL20 L	BDAL20 L
BF1	BDAL21 L	BDAL21 L
BH1	Not connected	SSPARE8
BJ1	GND	GND
BK1	Not connected	MSPAREB
BL1	Not connected	MSPAREB
BM1	GND	GND
BN1	BSACK L	BSACK L
BP1	BIRQ7 L	BIRQ7 L
BR1	BEVNT L	BEVNT L
BS1	Not Connected	+12B
BT1	GND	GND
BU1	Not connected	PSPARE2
BV1	+5V	+5V

TABLE A-1 Contd. COMPONENT SIDE (Side2)

Backplane Pin	SBC M1 Signal Function	LSI-11 Bus Signal Name
AA2	+5 V	+5 V
AB2	Not connected	-12 V
AC2	GND	GND
AD2	+12 V	+12 V
AE2	BDOUT L	BDOUT L
AF2	BRPLY L	BRPLY L
AH2	BDIN L	BDIN L
AJ2	BSYNC L	BSYNC L
AK2	BWTBT L	BWTBT L
AL2	BIRQ4 L	BIRQ4 L
AM2	Not connected	BIAKI L
AN2	BIAKO L	BIAKO L
AP2	BBS7 L	BBS7 L
AR2	Not connected	BDMGI L
AS2	BDMGO L	BDMGO L
AT2	BINIT L	BINIT L
AU2	BDAL0 L	BDAL0 L
AV2	BDAL1 L	BDAL1 L
BA2	+5 V	+5 V
BC2	GND	GND
BD2	Not connected	+12 V
BE2	BDAL2 L	BDAL2 L
BF2	BDAL3 L	BDAL3 L
BH2	BDAL4 L	BDAL4 L
BJ2	BDAL5 L	BDAL5 L
BL2	BDAL7 L	BDAL7 L
BM2	BDAL8 L	BDAL8 L
BN2	BDAL9 L	BDAL9 L
LP2	BDAL10 L	BDAL10 L
BR2	BDAL11 L	BDAL11 L
BS2	BDAL12 L	BDAL12 L
BT2	BDAL13 L	BDAL13 L
BU2	BDAL14 L	BDAL14 L
BV2	BDAL15 L	BDAL15

NOTE: **The following pins on the C and D sections of the backplane edge connector are also used:**

CA2, DA2 +5V power CT1, CC2, DT1, DC2 GND
CM2, CN2 BIAKI L, BIAKO L (linked) CR2, CS2
BDMGI L, BDMGO L (linked)

Appendix B NUMERICAL OP CODE LISTINGS

TABLE B-1 NUMERICAL OP CODES

OP Code	Mnemonic	OP Code	Mnemonic
00 00 00	Halt	00 4R DD	JSR
00 00 01	Wait		
00 00 02	RTI		
00 00 03	BPT	00 50 DD	CLR
00 00 04	IOT	00 51 DD	COM
00 00 05	Reset	00 52 DD	INC
00 00 06	RTT	00 53 DD	DEC
00 00 07	MFPT	00 54 DD	NEG
00 00 77	Unused	00 55 DD	ADC
		00 56 DD	SBC
		00 57 DD	TST
00 01 DD	JMP		
00 02 OR	RTS		
		00 60 DD	ROR
		00 61 DD	ROL
00 02 10		00 62 DD	ASR
to	Unused	00 63 DD	ASL
00 02 27		00 64 NN	MARK
		00 65 SS	MFPI
		00 66 DD	MTPI
00 02 3N	SPL	00 67 DD	SXT
00 02 40	NOP		
		00 70 00	
00 02 41		to	Unused
to	Cond Codes	00 77 77	
00 02 77			
		01 SS DD	MOV
00 03 DD	SWAB	02 SS DD	CMP
		03 SS DD	BIT
		04 SS DD	BIC
00 04 XXX	BR	05 SS DD	BIS
00 10 XXX	BNE	06 SS DD	ADD
00 14 XXX	BEQ		
00 20 XXX	BGE		
00 24 XXX	BLT		
00 30 XXX	BGT		
00 34 XXX	BLE		

TABLE B-1 contd. NUMERICAL OP CODES

OP Code	Mnemonic	OP Code	Mnemonic
07 0R SS	MUL	10 50 DD	CLRB
07 1R SS	DIV	10 51 DD	COMB
07 2R SS	ASH	10 52 DD	INCB
07 3R SS	ASHC	10 53 DD	DECB
07 4R DD	XOR	10 54 DD	NEGB
07 5R RR	MOVR	10 55 DD	ADCB
		10 56 DD	SBCB
10 65 SS	MFPD	10 57 DD	TSTB
10 67 DD	MFPS		
00 00 07	MFPT		
10 66 DD	MTPD		
10 64 SS	MTPS	10 60 DD	RORB
		10 61 DD	ROLB
		10 62 DD	ASRB
07 50 40		10 63 DD	ASLB
to	Unused		
07 67 77			
		10 64 00	
		to	Unused
07 7R NN	SOB	10 64 77	
10 00 XXX	BPL		
10 04 XXX	BMI	10 67 00	
10 10 XXX	BHI	to	Unused
10 14 XXX	BLOS	10 77 77	
10 20 XXX	BVC		
10 24 XXX	BVS		
10 30 XXX	BCC,BHIS		
10 34 XXX	BCS, BLO		
		11 SS DD	MOVB
10 40 00		12 SS DD	CMPB
to	EMT	13 SS DD	BITB
10 43 77		14 SS DD	BICB
		16 SS DD	SUB
10 44 00			
to	TRAP		
10 47 77		00 70 DD	CSM
		00 72 DD	TSTSET
		00 73 DD	WRTLCK

TABLE B-1 contd. NUMERICAL OP CODES

OP Code	Mnemonic	OP Code	Mnemonic
1706 fdst	ABSD	171 (AC) fsrc	MULD
1706 fdst	ABSF	171 (AC) fsrc	MULF
172 (AC) fsrc	ADDD	1707 fdst	NEGD
172 (AC) fsrc	ADDF	1707 fdst	NEGE
170000	CFCC	170011	SETD
1704 fdst	CLRD	170001	SETF
1704 fdst	CLRF	170002	SETI
173 (AC+4)	CMPD	170012	SETL
173 (AC+4)	CMPF	176 (AC) fdst	STCDF
174 (AC+4)	DIVD	176 (AC) fdst	STCDI
174 (AC+4)	DIVF	176 (AC) fdst	STCDL
177 (AC+4)	LDCDF	176 (AC) fdst	STCFD
177 (AC+4)	LDCFD	175 (AC+4)	STCFI
177 (AC) src	LDCID	175 (AC+4)	STCFL
177 (AC) src	LDCIF	174 (AC) fdst	STD
177 (AC) src	LDCLD	175 (AC) dst	STEXP
177 (AC) src	LDCLF	174 (AC) fdst	STF
172 (AC+4)	LDD	1702 dst	STFPD
176 (AC+4)	LDEXP	1703 dst	STST
172 (AC+4)	LDF	173 (AC) fsrc	SUBD
1701 src	LDFPS	173 (AC) fsrc	SUBF
171 (AC+4)	MODD	1705 fdst	TSTD
171 (AC+4)	MODF	1705 fdst	TSTF

INTERRUPTS ASYNCHRONOUS & SYNCHRONOUS

TABLE B-2 INTERRUPTS

Interrupt	Vector Address
Address error (CPU error register, bit 6)	4
Red stack trap (CPU error register, bit 2)	4
Yellow stack trap (CPU error register, bit 3)	4
Timeout/nonexistent memory (CPU error register bits 4-5)	4
Parity error (Parity, Abort)	114
Memory management violation (MMR0, 13-15)	250
Trace (T bit) Trap (PSW, bit 4)	14
Power fail (PWRF)	24
FP exception (FPE)	244
EVENT/LTC	100
PIR 1 (PIRQ, bit 9)	240
PIR 2 (PIRQ, bit 10)	240
PIR 3 (PIRQ, bit 11)	240
PIR 4 (PIRQ, bit 12)	240
PIR 5 (PIRQ, bit 13)	240
PIR 6 (PIRQ, bit 14)	240
PIR 7 (PIRQ, bit 15)	240

Appendix C I/O PAGE MEMORY MAP

TABLE C-1 SERIAL LINE FACTORY ADDRESSES

Address	Register	Vector	Channel
17776500	RCSR		
17776502	RBUF	300	
17776504	XCSR		Channel 0
17776506	XBUF	304	
17776510	RCSR		
17776512	RBUF	310	
17776514	XCSR		Channel 1
17776516	XBUF	314	
17776520	RCSR		
17776522	RBUF	320	
17776524	XCSR		Channel 2
17776526	XBUF	324	
17777560	RCSR		
17777562	RBUF	60	
17777564	XCSR		Channel 3
17777566	XBUF	64	

TABLE C-2 INTERNAL REGISTERS

Abbrv.	Register	Address
PSW	Processor Status Word	17777776
PIRQ	Program Interrupt Request	17777772
CPUERR	CPU Error Register	17777766
HMR	Hit/Miss Register	17777752

TABLE C-3 SYSTEM REGISTERS

Abbrv.	Register	Address
MR	Maintenance Register	17777750
MER	Memory Error Register	17777744
CCR	Cache Control Register	17777746

TABLE C-4 EXTERNAL REGISTERS

Abbrv.	Register	Address
LTC	Line-Time Clock Register	17777546
PCSR	Parity memory Control and Status Register	17772100

TABLE C-5 BOOT CODE LOCATIONS

Section	Address Ranges
Window 0-127	17773000 to 17773776

TABLE C-6 MEMORY MANAGEMENT REGISTERS

Abbrv.	Name	Address
MMR0	Memory Management Register0	17777572
MMR1	Memory Management Register 1	17777574
MMR2	Memory Management Register 2	17777576
MMR3	Memory Management Register 3	17772516
-	Kernel Data Page PAR7 to PAR0	17772376 to 17772360
-	Kernel Instruction PARs	17772356 to 17772340
-	Kernel Data PDRs	17772336 to 17772320
-	Kernel Instruction PDRs	17772316 to 17772300
-	Supervisor Data PARs	17772276 to 17772260
-	Supervisor Instruction PARs	17772256 to 17772240
-	Supervisor Data PDRs	17772236 to 17772220
-	Supervisor Instruction PDRs	17772216 to 17772200
-	User Data PARs	17777676 to 17777660
-	User Instruction PARs	17777656 to 17777640
-	User Data PDRs	17777636 to 17777620
-	User Instruction PDRs	17777616 to 17777600

Appendix D DEVICE MNEMONICS

TABLE D-1 DEVICE MNEMONICS

Mnemonic	Device	Address
DX01	Floppy	17777170
DY	RX02 Floppy	17777170
DL	RL01, RL02 Removable Disk	17774400
DU	MSCP Devices	17772150
DM	RK06/RK07 Removable Disk	17777440
DB	RM03 Removable Disk	17776700
MS	TS11, TK25, TSV05,TU80	17772522
MT	TS03, TU10, TE10	17772522
DD	TU58 Tape Cartridge	17776500
MU	TK50 Tape Cartridge	17774500
XQ	DEQNA (DECNET boot)	17774440

Mentec Limited

Mentec House,
Dun Laoghaire Industrial Estate,
Co. Dublin, Ireland.
Tel: 353-1-2059797
Fax: 353-1-2059798