TM20001600
PART 2

# OPERATION AND MAINTENANCE INSTRUCTION MANUAL FOR 1600 SERIES COMPUTERS (LOGIC DIAGRAMS)




Microdata™

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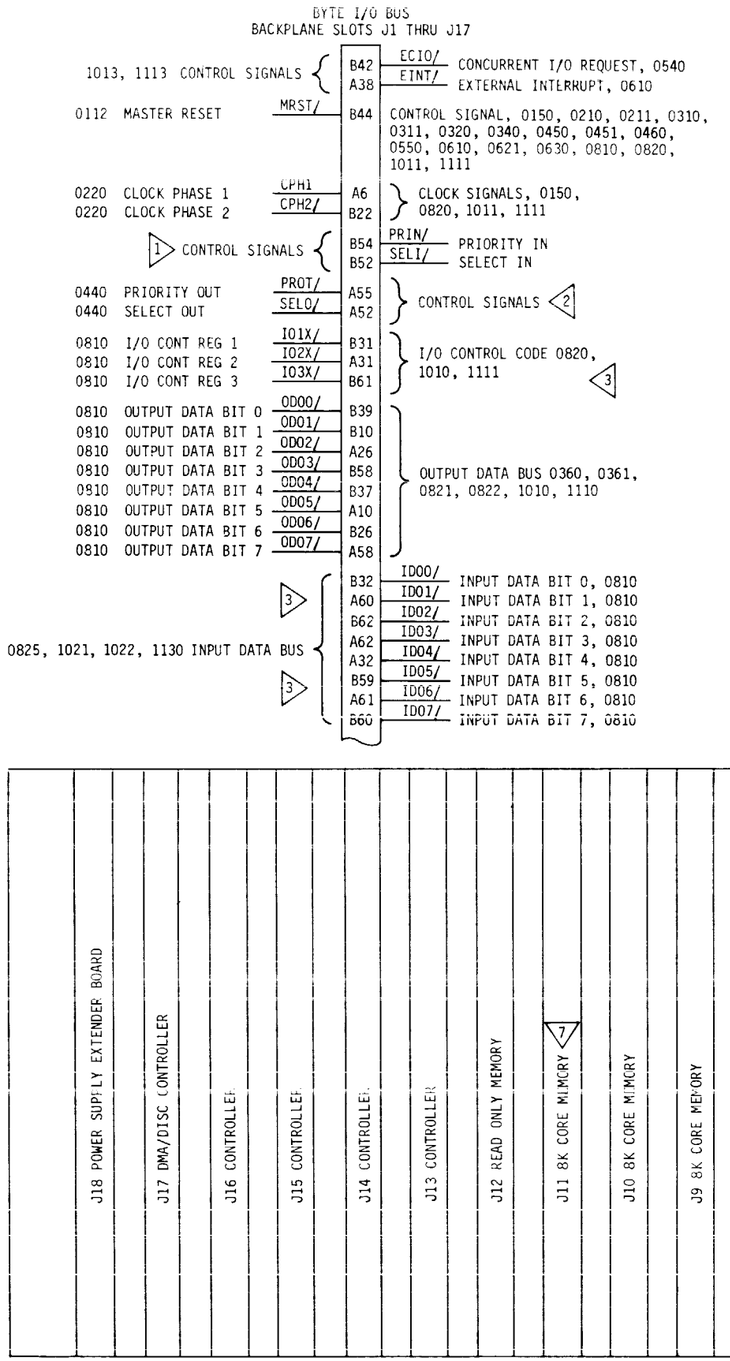
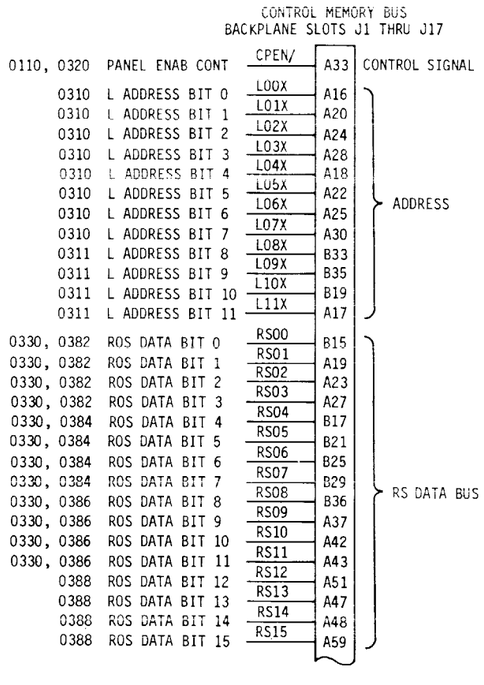
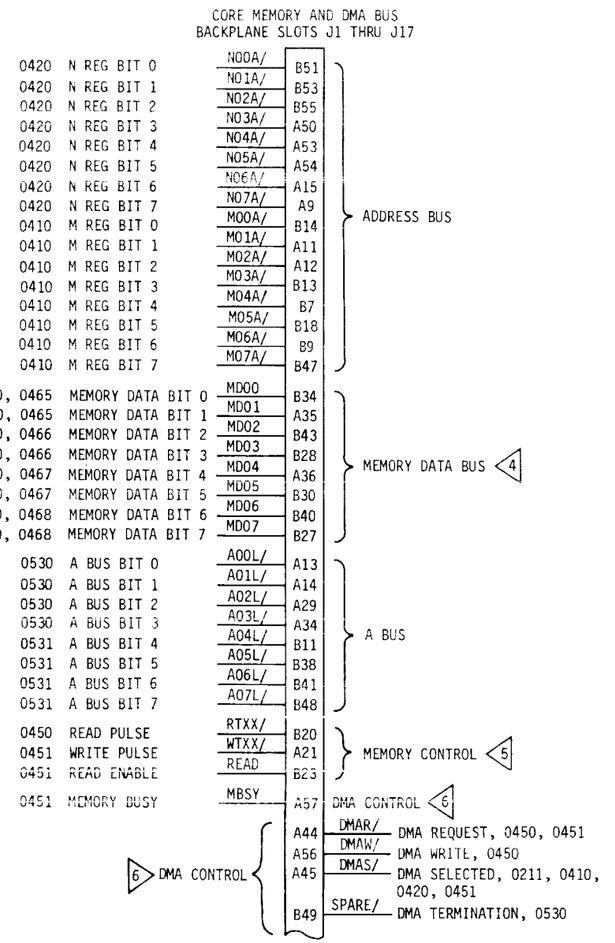
# LIST OF ILLUSTRATIONS

# INTERCONNECTION DIAGRAM



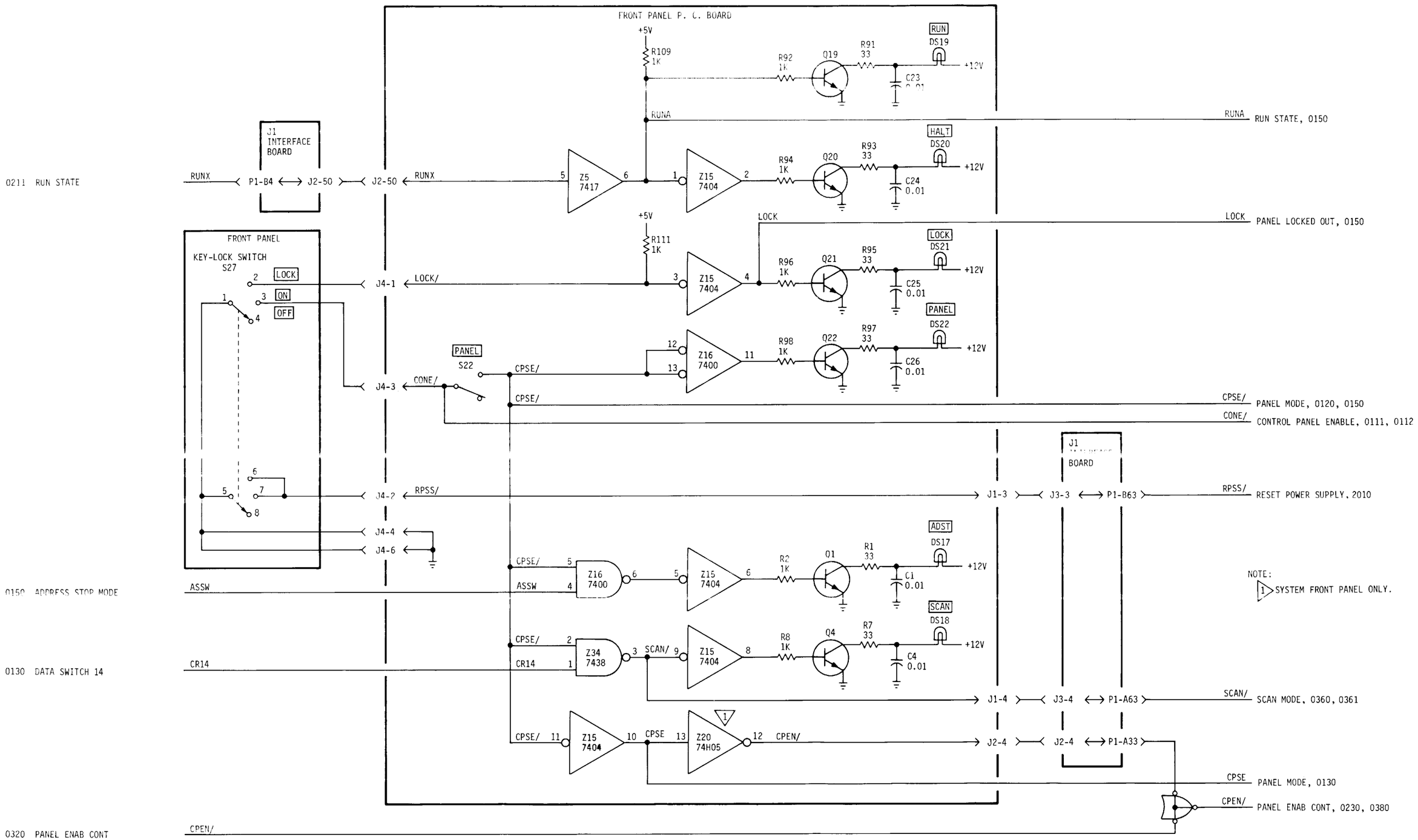




NOTES:

1. NOT ON J1, J2 AND J3; PINS B54 AND B52.
2. NOT ON J1, J2 AND J17; PINS A55 AND A52.
3. NOT ON J2; PINS B61, A60, B62, A62, B59, A61 AND B60.
4. NOT ON J1 AND J2; PINS B34, A35, B43, B28, A36, B30, B40 AND B27.
5. NOT ON J1, J12 THRU J17; PINS B20 AND A21.
6. NOT ON J1; PINS B23, A57, A44, A56, A45.
7. MEMORY SHOWN AS 64K. IF LESS THAN 64K, THE ROM, DMA, AND CONTROLLERS MUST BE MOVED TO SLOTS ADJACENT TO THE LAST MEMORY BOARD.
8. CONTROLLER PRIORITY SEQUENCE:

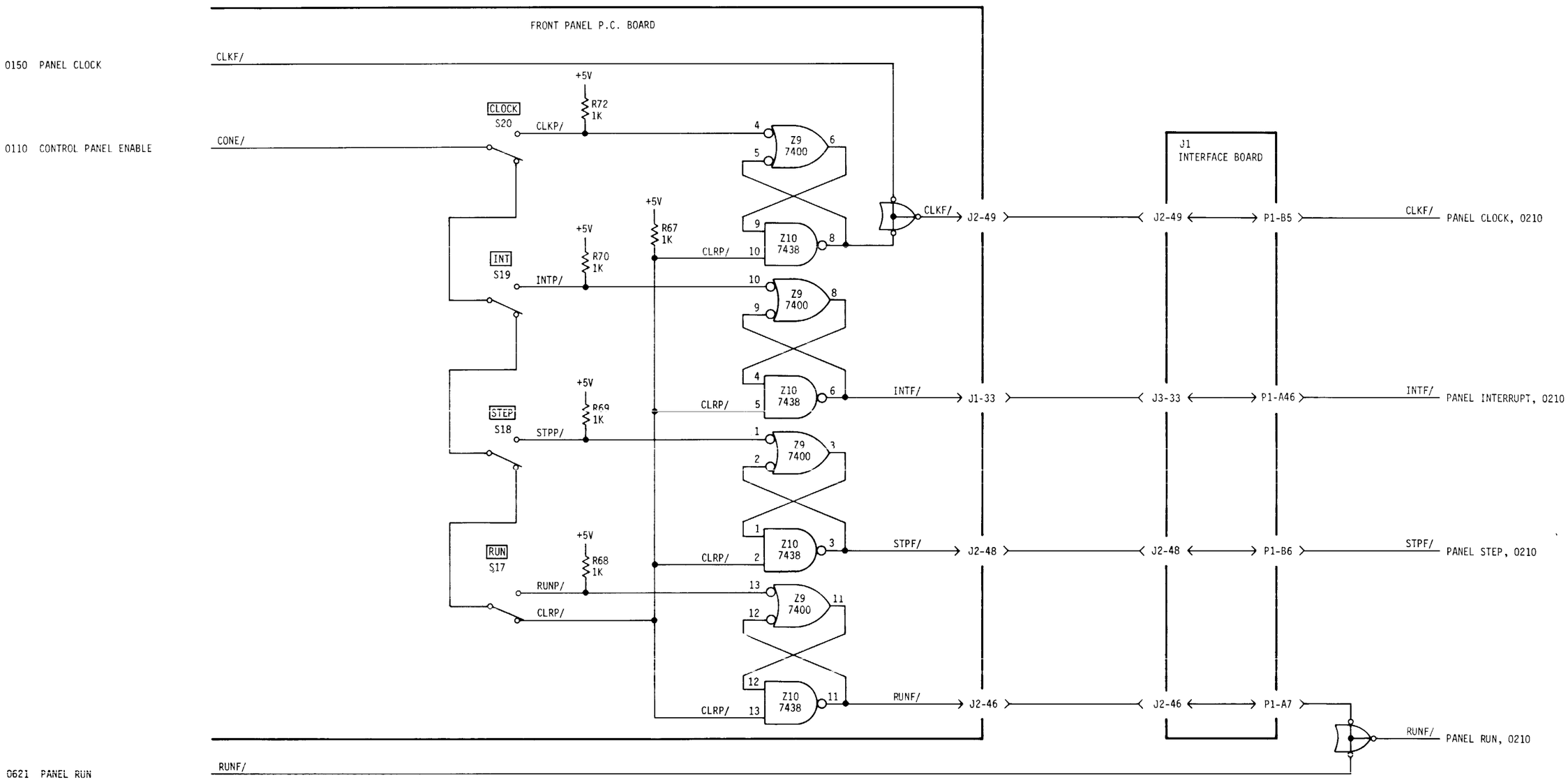
| | |
|---|---|
| | EIGHT CHANNEL CONTROLLER |
| J13 | FOUR CHANNEL CONTROLLER |
| J14 | 2400 BAUD CONTROLLER |
| J15 | MAGNETIC TAPE UNIT CONTROLLER (TWO SLOTS) |
| J16 | PAPER TAPE CONTROLLER |
| | CARD READER CONTROLLER |
| | LINE PRINTER CONTROLLER |




FRONT PANEL CONTROL INDICATORS

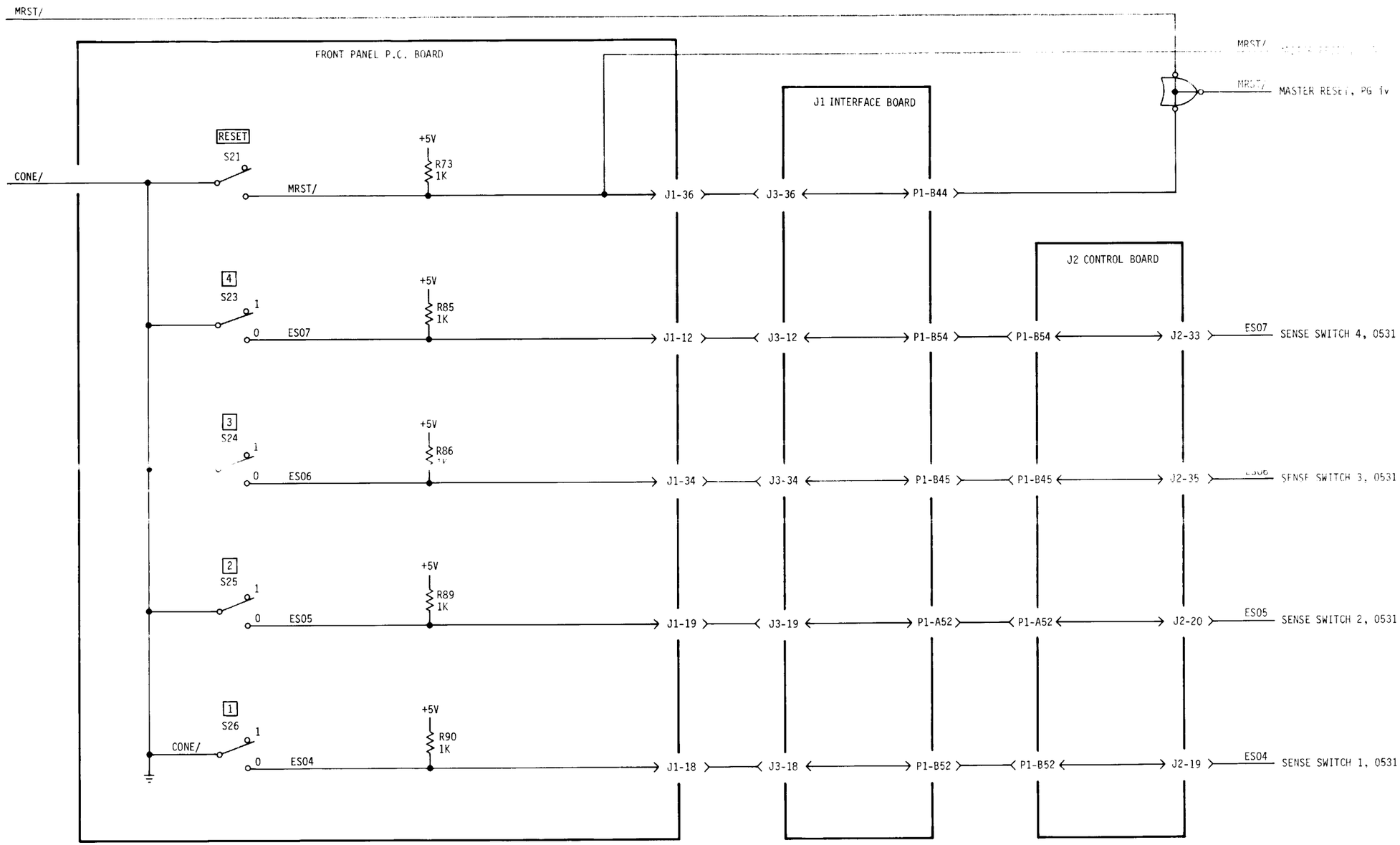
FRONT PANEL P.C. BOARD AND J1 INTERFACE BOARD 0110

# FRONT PANEL CONTROL SWITCHES



0621 MASTER RESET

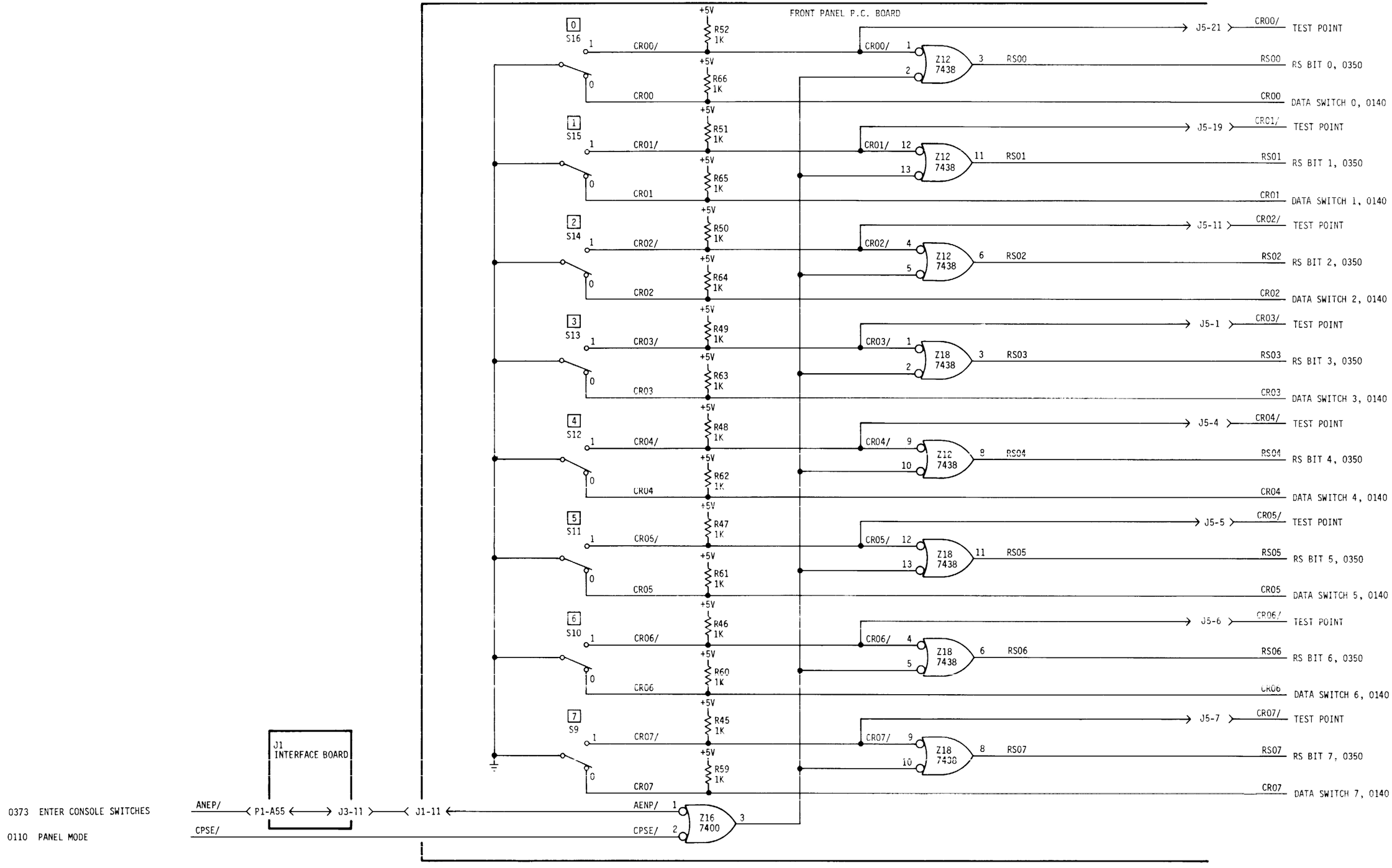
0110 CONTROL PANEL ENABLE

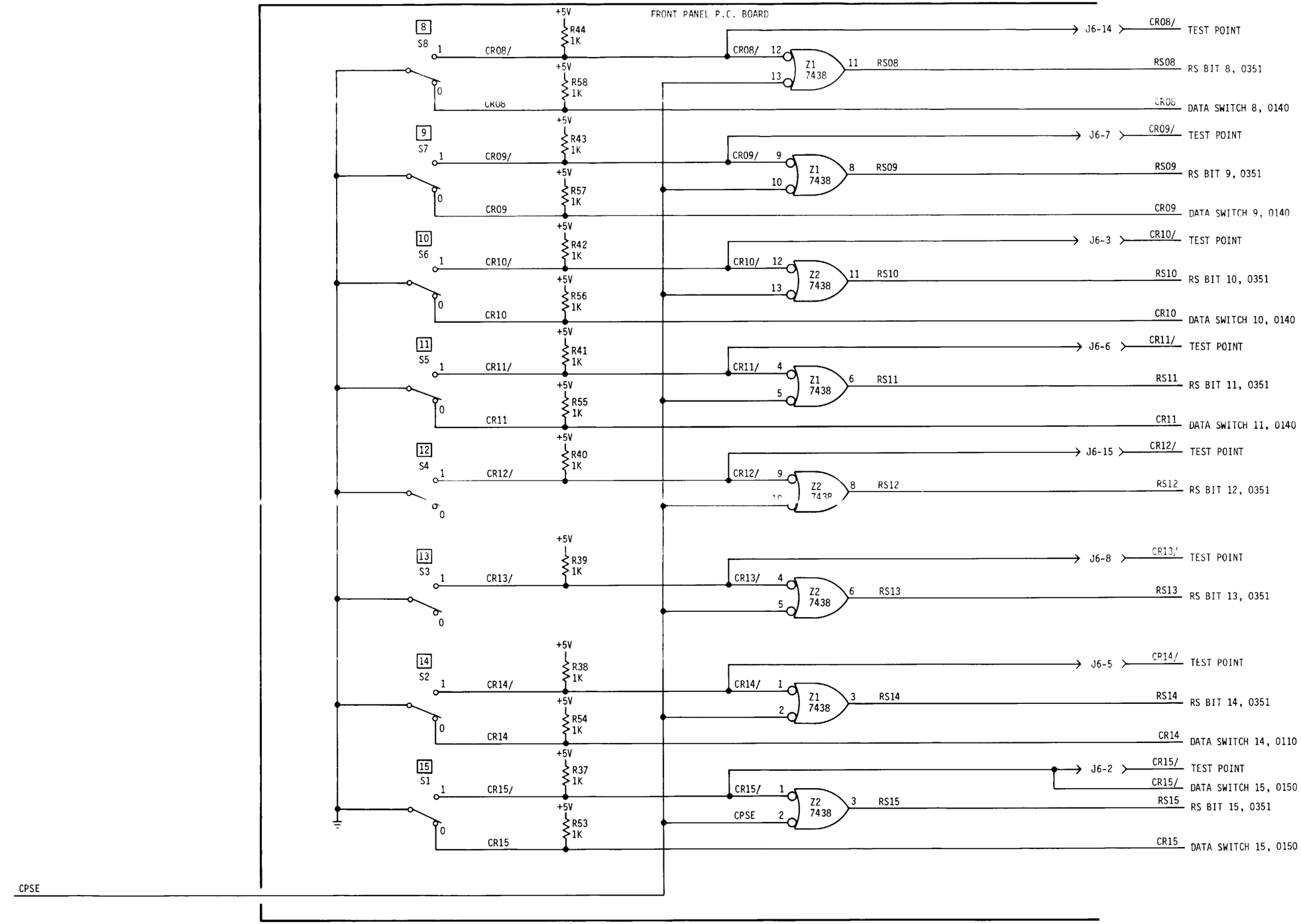



SENSE SWITCHES AND MASTER RESET

FRONT PANEL P.C. BOARD, J1 INTERFACE BOARD
AND J2 CONTROL BOARD
0112

## LOWER DATA SWITCHES

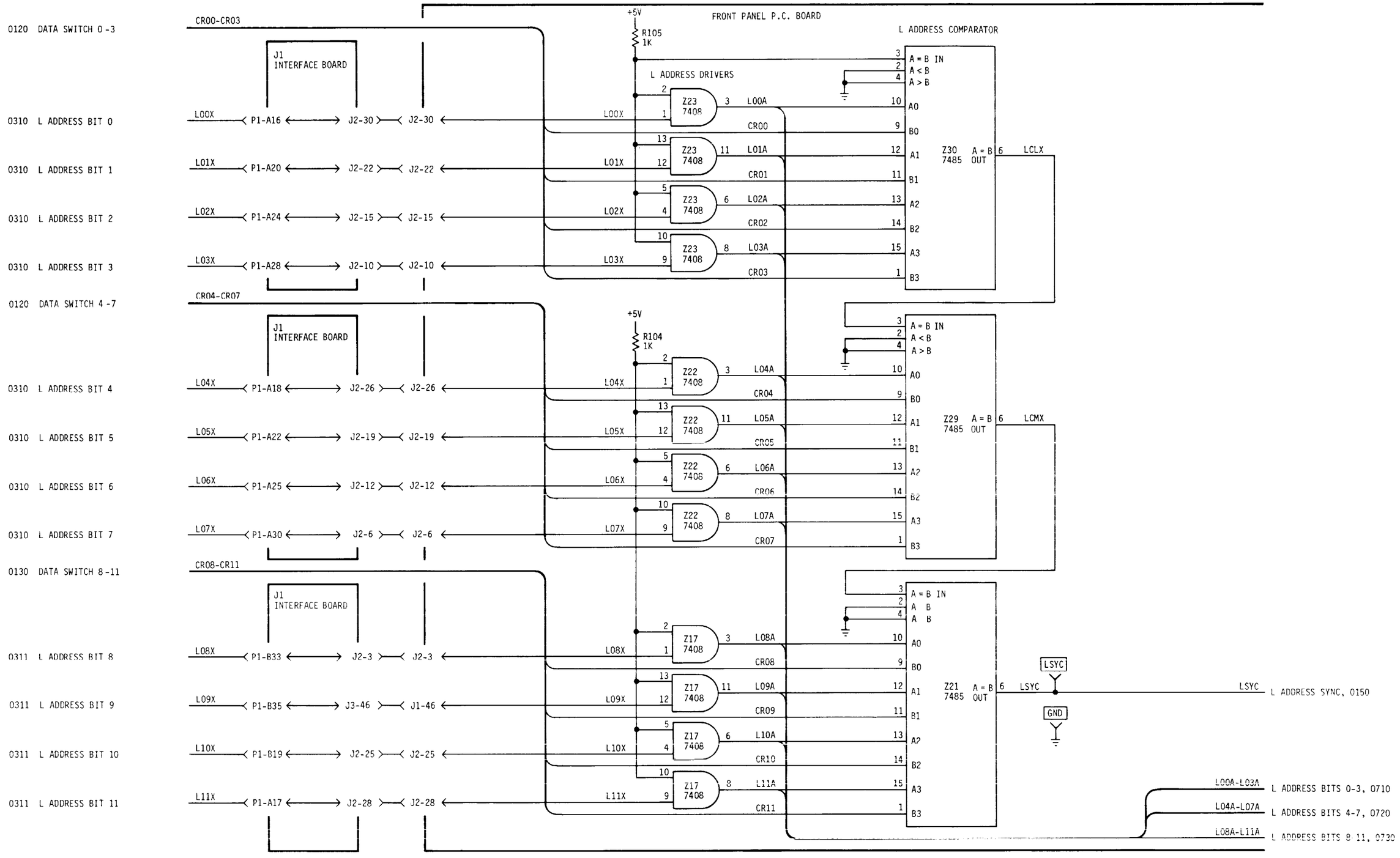


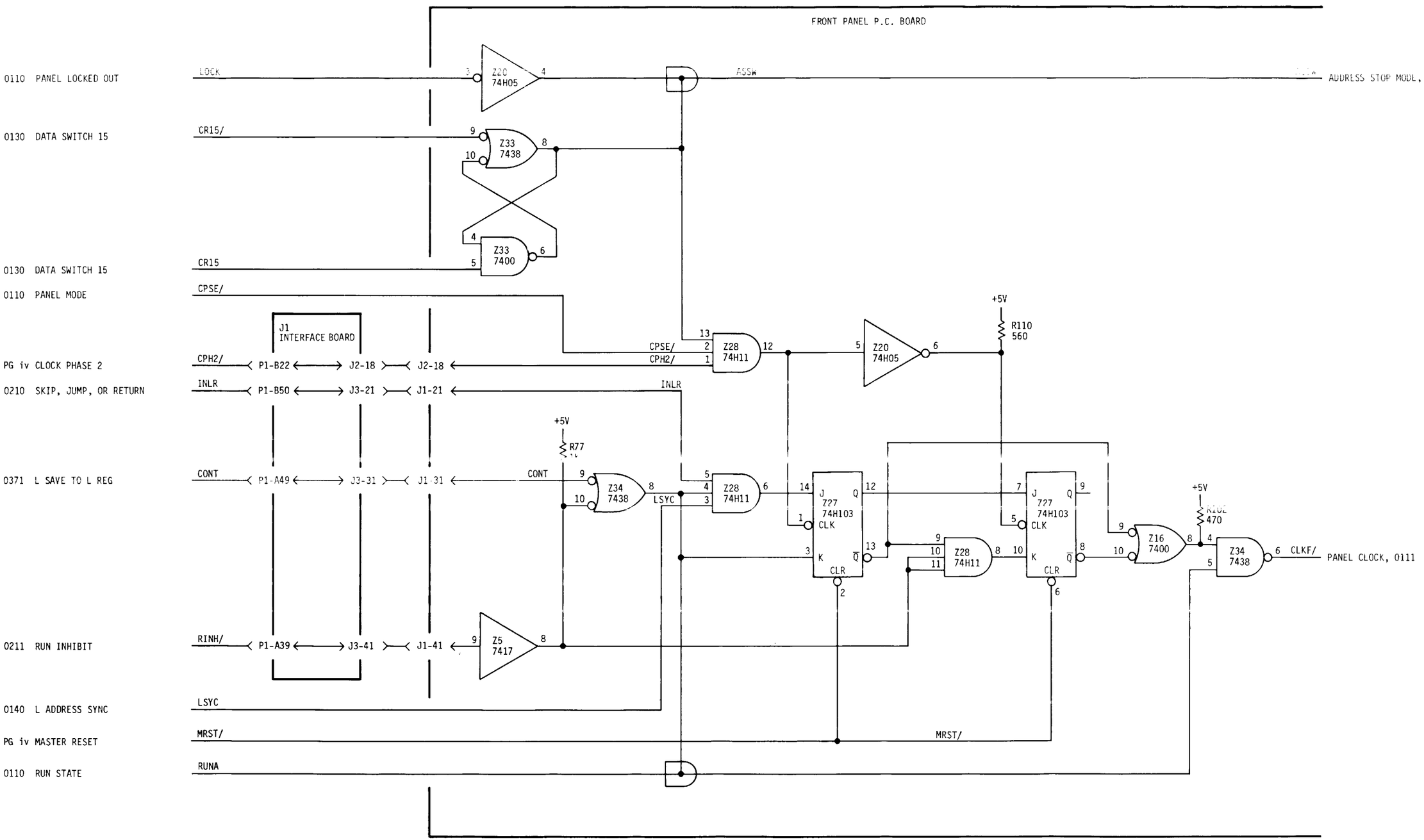



UPPER DATA SWITCHES

FRONT PANEL P.C. BOARD
0130

# L ADDRESS DRIVERS AND COMPARATOR






ADDRESS STOP LOGIC

FRONT PANEL P.C. BOARD
AND J1 INTERFACE BOARD
0150

0210 PANEL RUN SET

0230 5-MHZ CLOCK PHASE 2

0230 RUN & INHIBIT CONTROL CLOCK

0211 CLOCK STOP

PG iv MASTER RESET

0373 ENTER INTERNAL STATUS

0230 DATA CLOCK

0111 PANEL RUN

0111 PANEL STEP

0111 PANEL INTERRUPT

0210 SWITCH SYNC

0210 SWITCH SYNC 2

0211 RUN STATE

0111 PANEL CLOCK

0211 RUN STATE

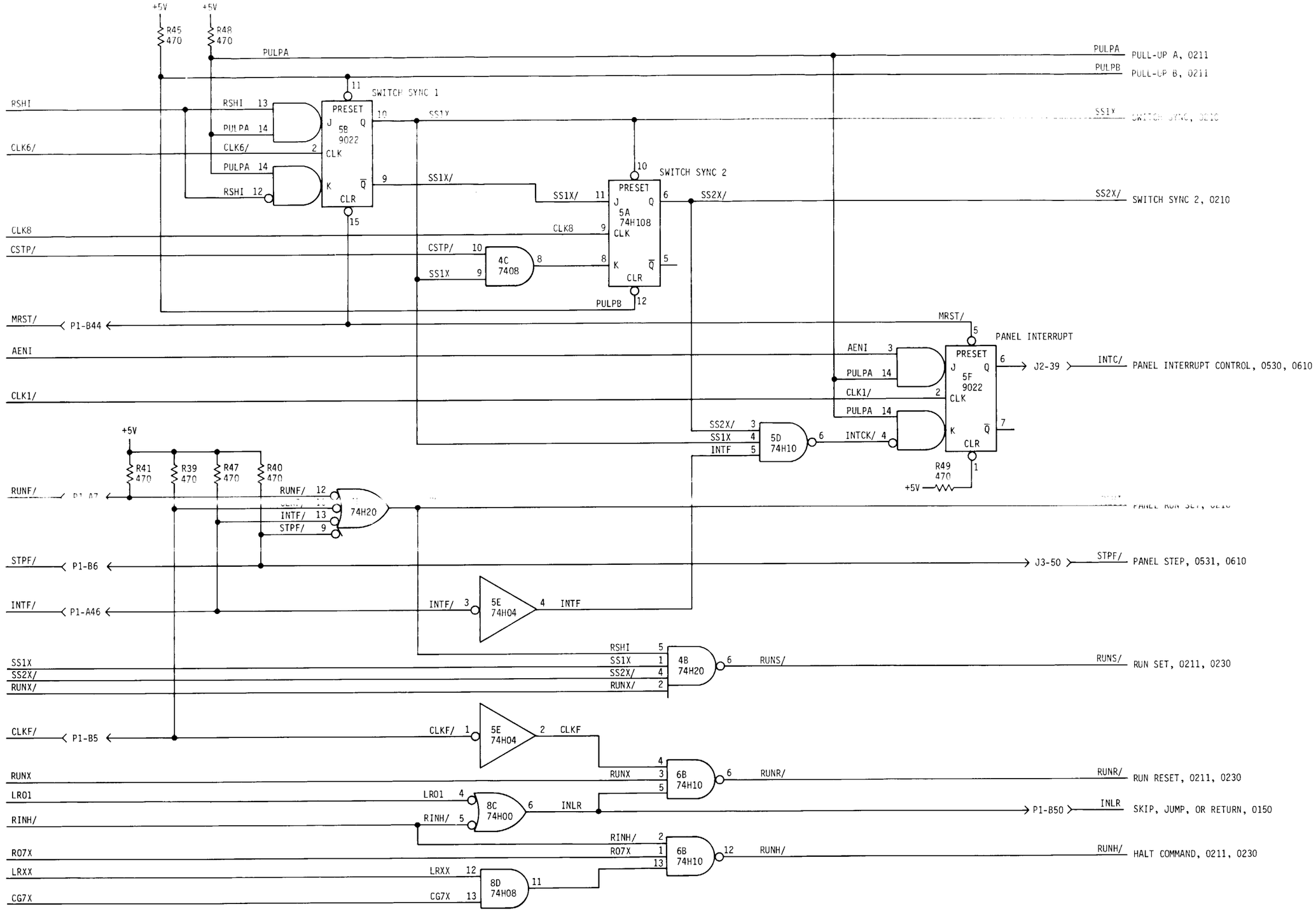
0372 JUMP

0211 RUN INHIBIT

0361 R REG BIT 7

0370 LOAD LITERAL

0371 LOAD SEVEN




RUN AND INHIBIT CONTROL 1

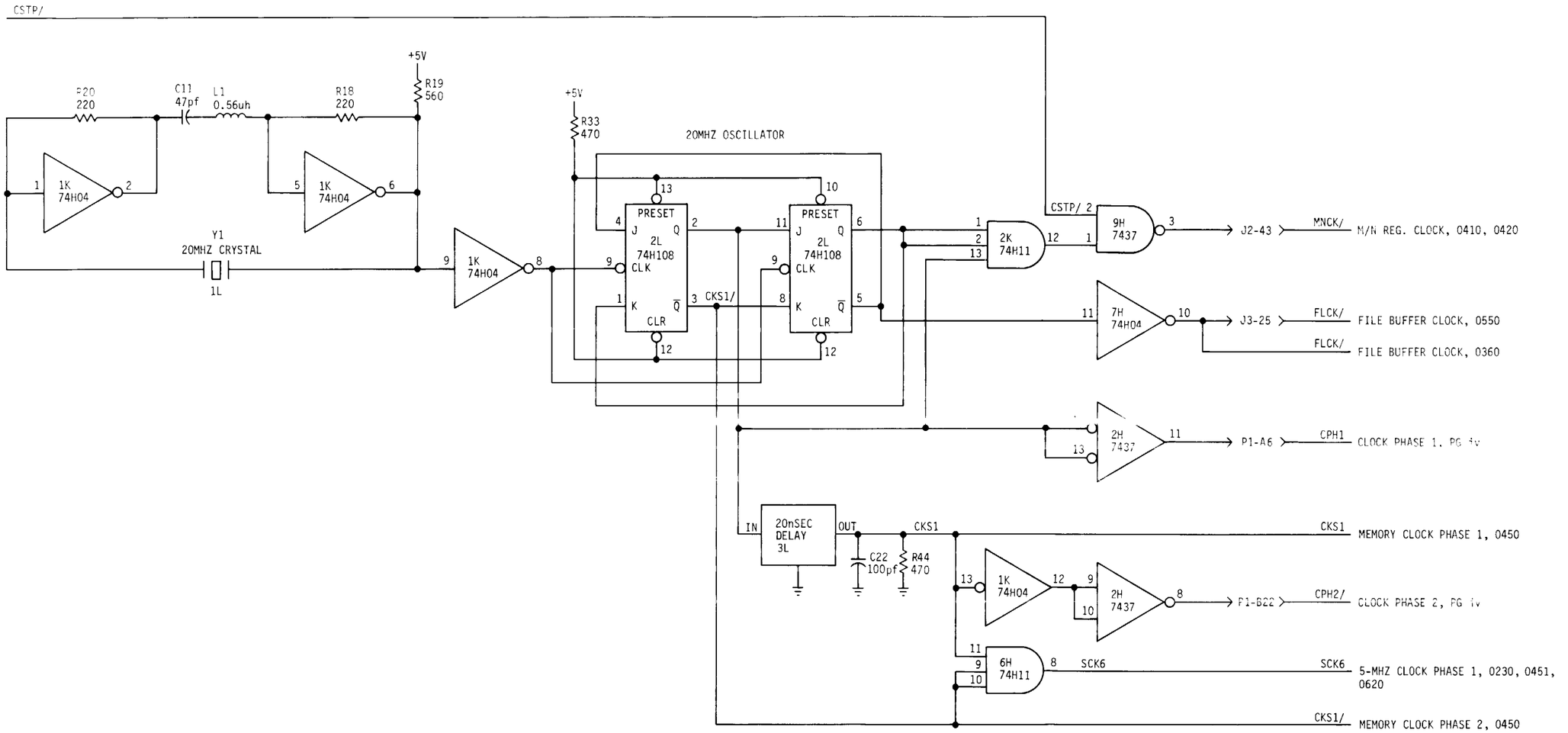
J2 CONTROL BOARD
0210

# RUN AND INHIBIT CONTROL 2

PG iv MASTER RESET
0210 RUN RESET
0210 HALT COMMAND
0230 5-MHZ CLOCK PHASE 2
0210 PULL-UP A
0210 RUN SET
0210 PULL-UP B
0230 RUN & INHIBIT CONTROL CLOCK
0372 JUMP
0370 COMPARE FILE
0520 HIGH-ORDER BIT CARRY
0370 TNXX/ TEST IF NOT ZERO
0570 A BUS ZERO DECODE
0370 TZXX/ TEST IF ZERO
0211 CLOCK STOP
0370 MEMORY READ OR WRITE
0451 MEMORY STOP
0372 M TO M REG SELECT
0451 MEMORY BUSY INTERNAL
PG iv DMA SELECTED
0374 I REG TRANSFER TO B BUS
0451 MEMORY DATA NOT AVAILABLE

MRST/ ← P1-B44
RUNR/
RUNH/
7F 74H00
CLK6/
PULPA
RUNS/
PULPB
CLK8
LRO1/
CPXX
CRY7 ← J3-49
TNXX/
AZO7/
TZXX/
CSTP/
MYXX
MSTP
MNRX
MBYI
DMAS/ ← P1-A45
BTXR ← J2-31
MDNA
TMCE
5B 9022 PRESET J Q CLK K Q CLR
5A 74H108 PRESET J Q CLK K Q CLR
6J 76H20
6K 74H00
6L 74H04
7C 7438
1J 7408
2J 74H11
+5V
R51 220
RUNX/ → RUNX/ RUN STATE, 0210, 0630
RUNX → P1-B4 → RUNX RUN STATE, 0210, 0230, 0620
RUNX → RUNX RUN STATE, 0110
8C 74H00
7C 7438 → CSTP/ CLOCK STOP, 0211, 0630
RINH/ → P1-A39 → RINH/ RUN INHIBIT, 0150
RINH/ RUN INHIBIT, 0210, 0230, 0372
7H 74H04
2H 7437 → P1-A41 → CSTP/ CLOCK STOP, 0320
CSTP CLOCK STOP, 0230
CSTP/ CLOCK STOP, 0210, 0220, 0330, 0360, 0372, 0450
TMCE TM CLOCK ENABLE, 0230

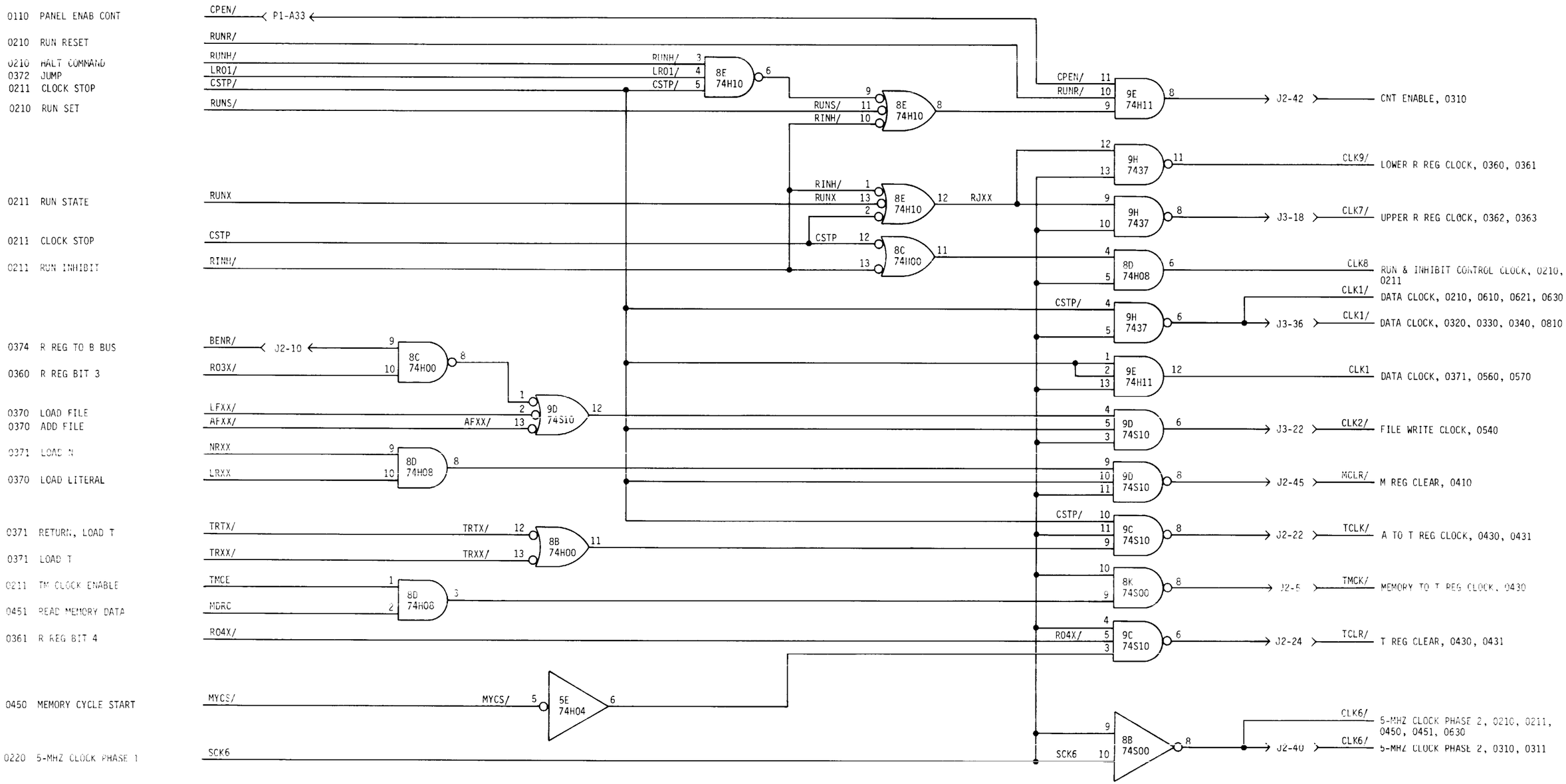
0211 CLOCK STOP

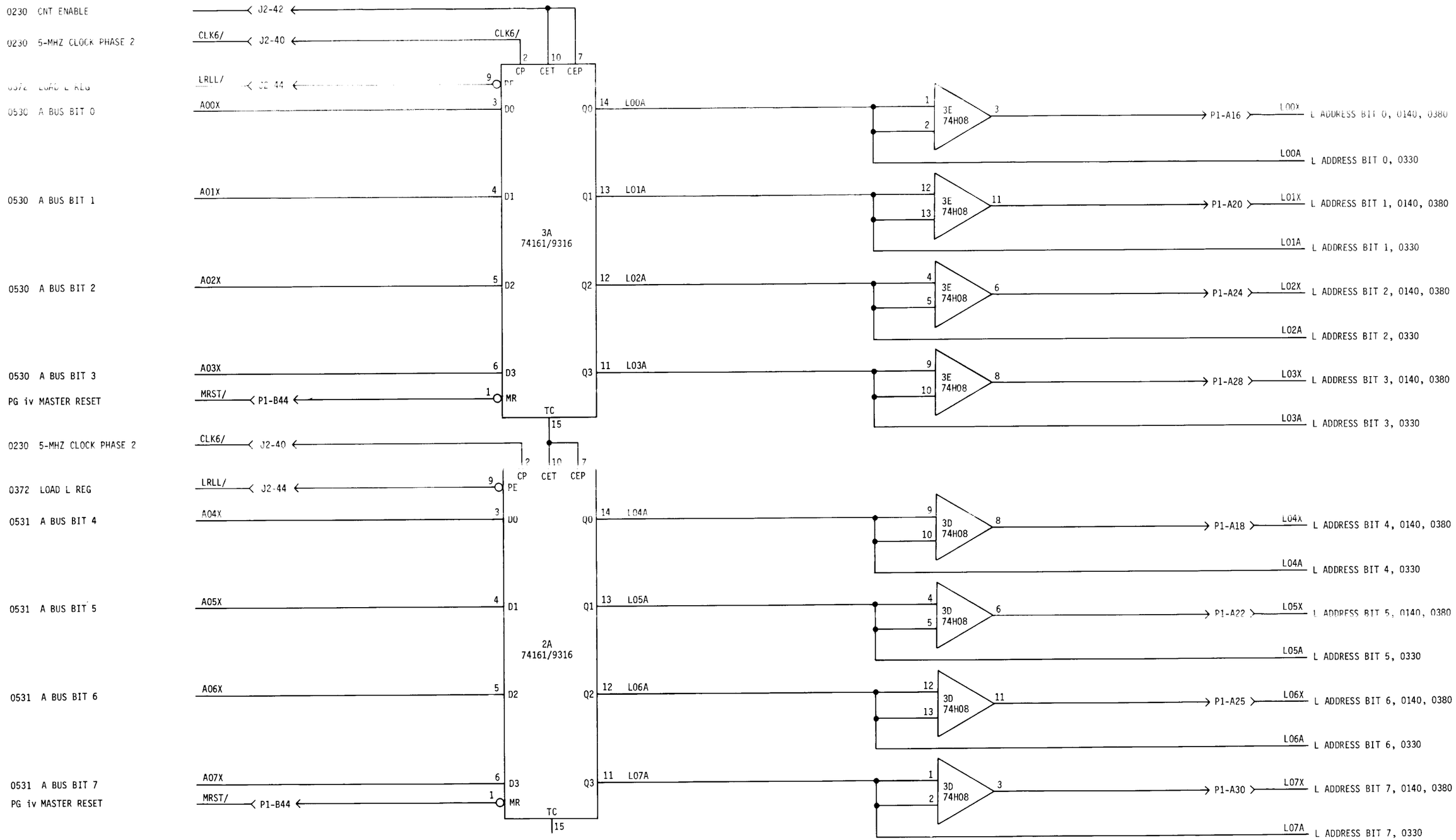



CLOCK GENERATOR

J2 CONTROL BOARD
0220

# CLOCK GATES

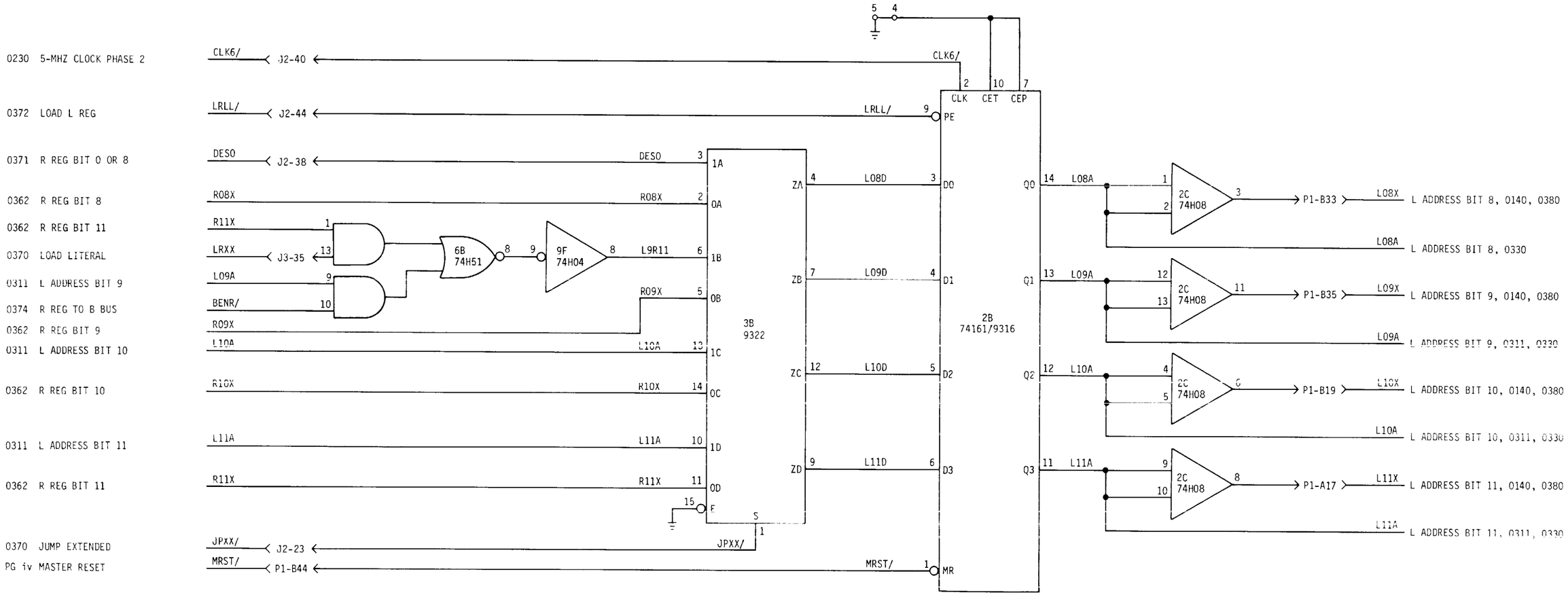

0110 PANEL ENAB CONT
0210 RUN RESET
0210 HALT COMMAND
0372 JUMP
0211 CLOCK STOP
0210 RUN SET
0211 RUN STATE
0211 CLOCK STOP
0211 RUN INHIBIT
0374 R REG TO B BUS
0360 R REG BIT 3
0370 LOAD FILE
0370 ADD FILE
0371 LOAD N
0370 LOAD LITERAL
0371 RETURN, LOAD T
0371 LOAD T
0211 TM CLOCK ENABLE
0451 READ MEMORY DATA
0361 R REG BIT 4
0450 MEMORY CYCLE START
0220 5-MHZ CLOCK PHASE 1
CPEN/
P1-A33
RUNR/
RUNH/
LRO1/
CSTP/
RUNS/
RUNX
CSTP
RINH/
BENR/
J2-10
RO3X/
LFXX/
AFXX/
NRXX
LRXX
TRTX/
TRXX/
TMCE
MDRC
RO4X/
MYCS/
SCK6
8E 74H10
8C 74H00
8D 74H08
9D 74S10
8B 74H00
5E 74H04
9E 74H11
9H 7437
8K 74S00
9C 74S10
RJXX
J2-42
CNT ENABLE, 0310
CLK9/
LOWER R REG CLOCK, 0360, 0361
J3-18
CLK7/
UPPER R REG CLOCK, 0362, 0363
CLK8
RUN & INHIBIT CONTROL CLOCK, 0210, 0211
CLK1/
DATA CLOCK, 0210, 0610, 0621, 0630
J3-36
DATA CLOCK, 0320, 0330, 0340, 0810
CLK1
DATA CLOCK, 0371, 0560, 0570
J3-22
CLK2/
FILE WRITE CLOCK, 0540
J2-45
MCLR/
M REG CLEAR, 0410
J2-22
TCLK/
A TO T REG CLOCK, 0430, 0431
J2-5
TMCK/
MEMORY TO T REG CLOCK, 0430
J2-24
TCLR/
T REG CLEAR, 0430, 0431
CLK6/
5-MHZ CLOCK PHASE 2, 0210, 0211, 0450, 0451, 0630
J2-40
5-MHZ CLOCK PHASE 2, 0310, 0311

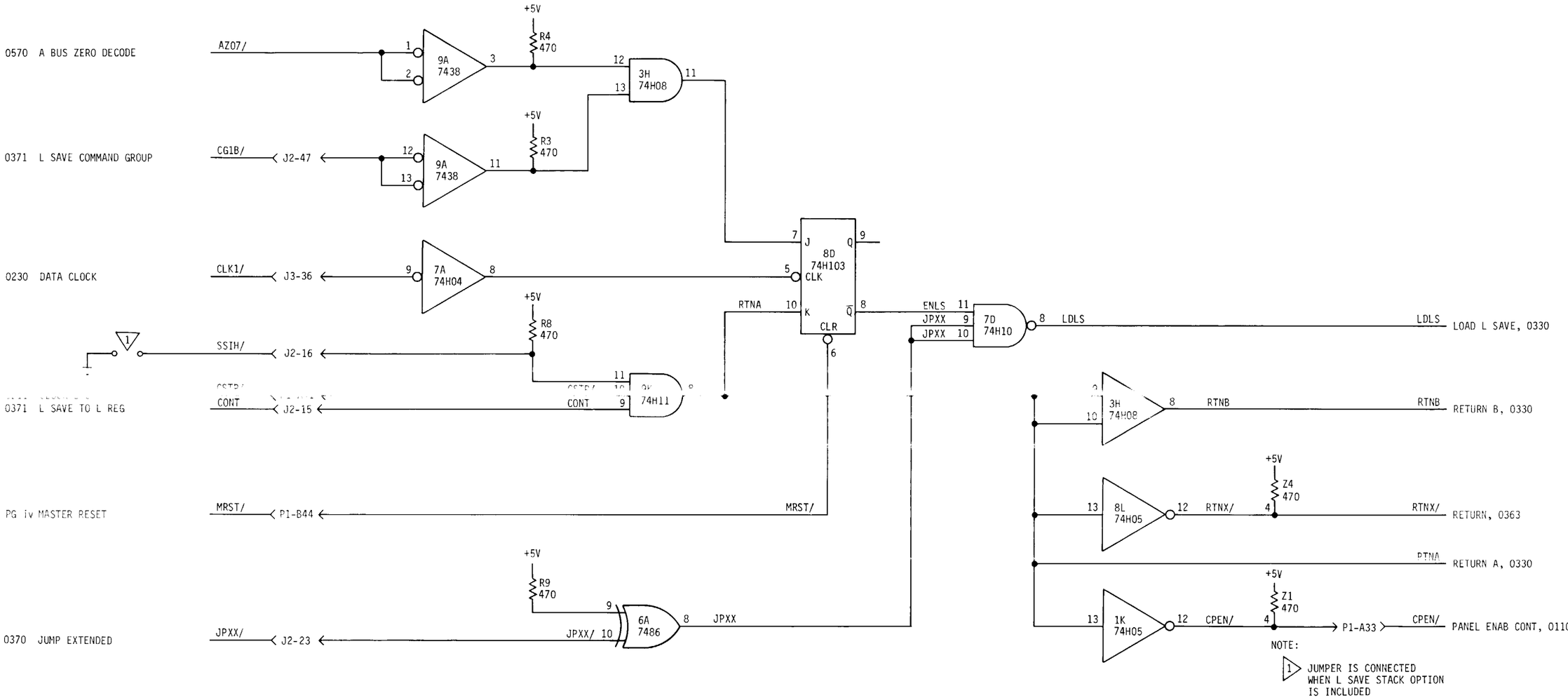



L REGISTER BITS 0-7

J3 DATA BOARD
0310

# L REGISTER BITS 8-11






L SAVE CONTROL

J3 DATA BOARD
0320

# L SAVE REGISTER

0320 RETURN B

0310 L ADDRESS BIT 0

0310 L ADDRESS BIT 1

0310 L ADDRESS BIT 2

0310 L ADDRESS BIT 3

0230 DATA CLOCK

0320 LOAD L SAVE

0550 PULL-UP 1

0310 L ADDRESS BIT 4

0310 L ADDRESS BIT 5

0310 L ADDRESS BIT 6

0310 L ADDRESS BIT 7

0230 DATA CLOCK

0320 LOAD L SAVE

0550 PULL-UP 1

0311 L ADDRESS BIT 8

0311 L ADDRESS BIT 9

0311 L ADDRESS BIT 10

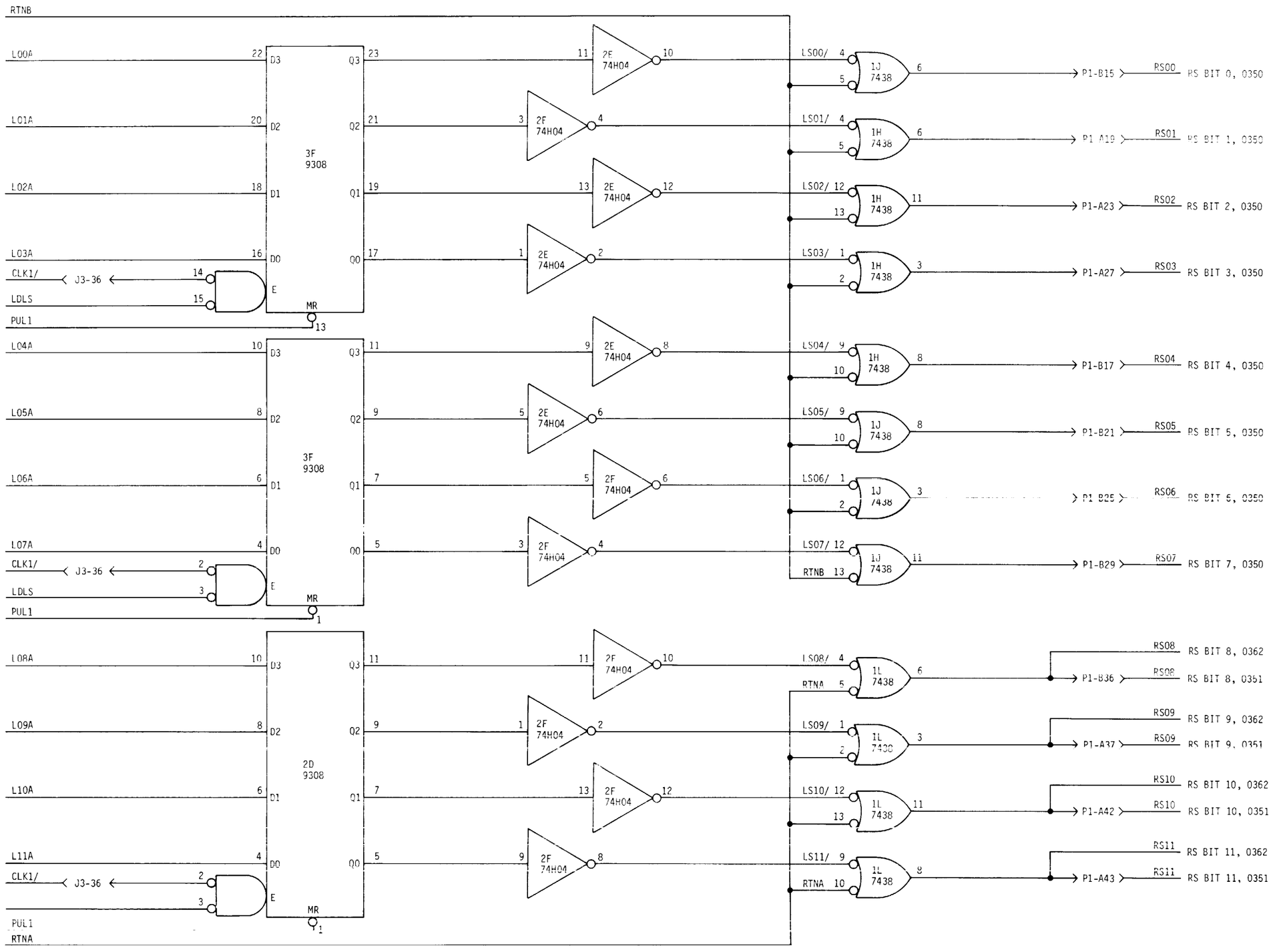
0311 L ADDRESS BIT 11

0230 DATA CLOCK

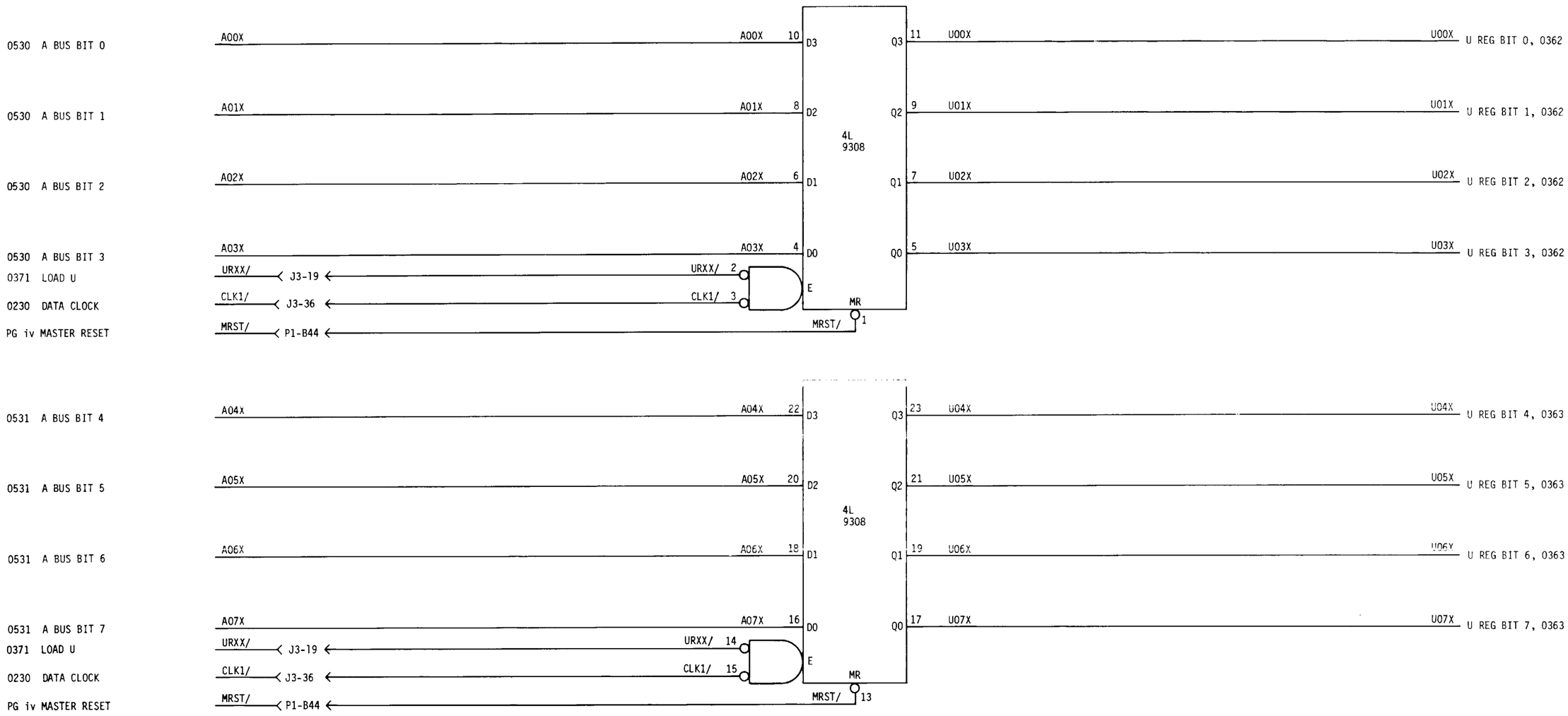
0320 LOAD L SAVE

0550 PULL-UP 1

0320 RETURN A




RS BIT 0, 0350
RS BIT 1, 0350
RS BIT 2, 0350
RS BIT 3, 0350
RS BIT 4, 0350
RS BIT 5, 0350
RS BIT 6, 0350
RS BIT 7, 0350
RS BIT 8, 0362
RS BIT 8, 0351
RS BIT 9, 0362
RS BIT 9, 0351
RS BIT 10, 0362
RS BIT 10, 0351
RS BIT 11, 0362
RS BIT 11, 0351




U REGISTER

J3 DATA BOARD
0340

# RS BUS AND DRIVERS

0382 ROS DATA BIT 0
0330 RS BIT 0

0382 ROS DATA BIT 1
0330 RS BIT 1

0382 ROS DATA BIT 2
0330 RS BIT 2

0382 ROS DATA BIT 3
0330 RS BIT 3

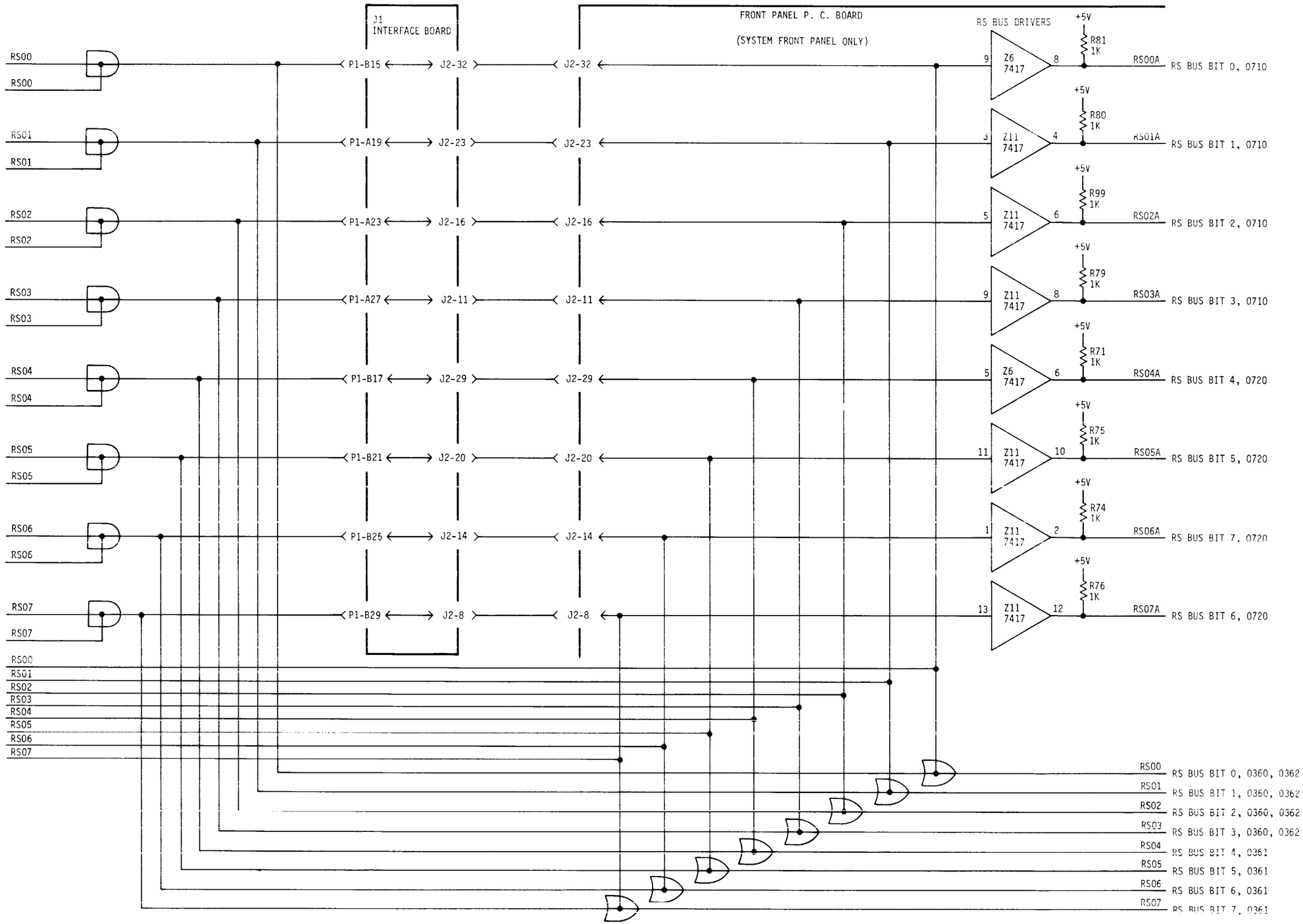
0384 ROS DATA BIT 4
0330 RS BIT 4

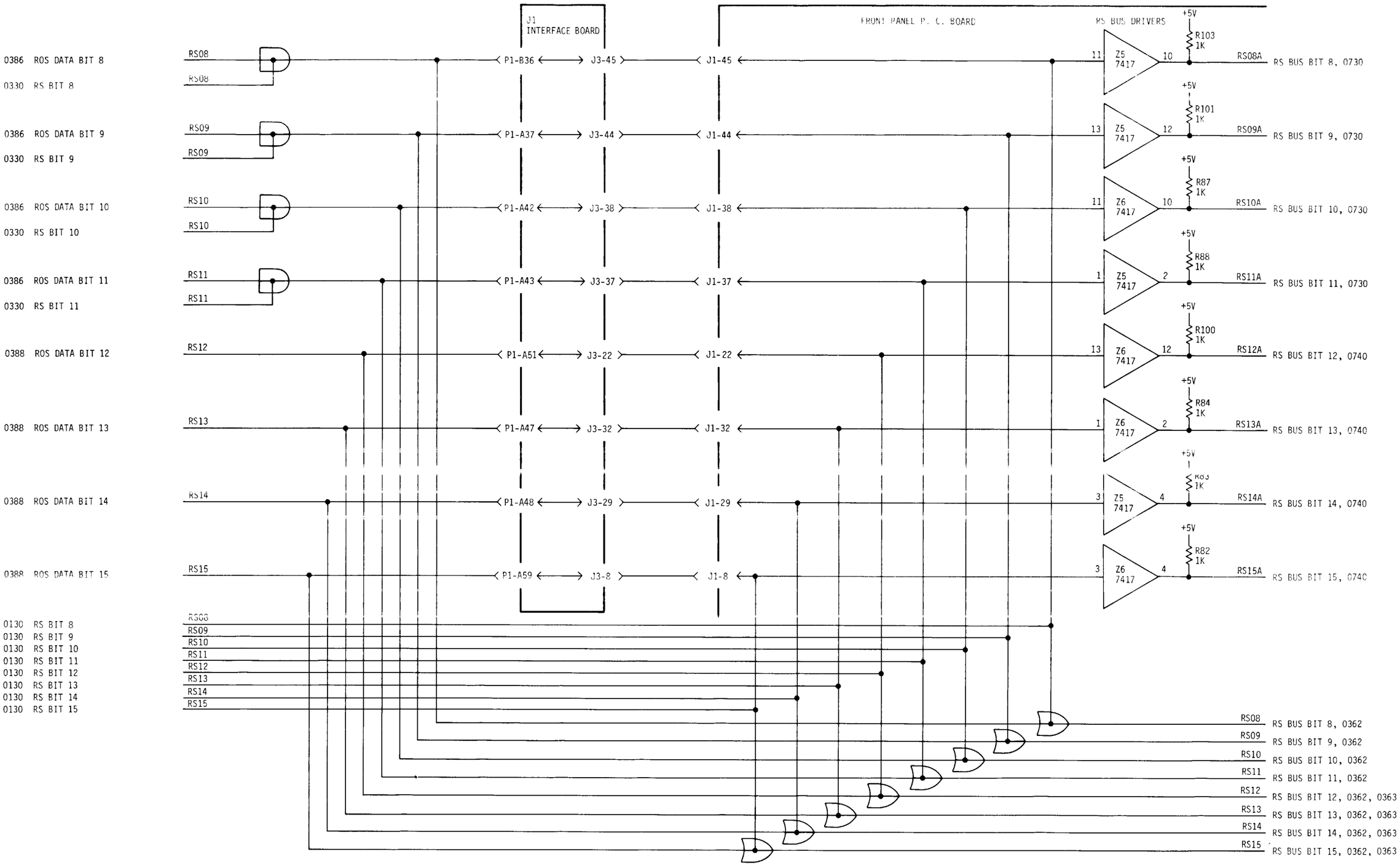
0384 ROS DATA BIT 5
0330 RS BIT 5

0384 ROS DATA BIT 6
0330 RS BIT 6

0384 ROS DATA BIT 7
0330 RS BIT 7

0120 RS BIT 0
0120 RS BIT 1
0120 RS BIT 2
0120 RS BIT 3
0120 RS BIT 4
0120 RS BIT 5
0120 RS BIT 6
0120 RS BIT 7





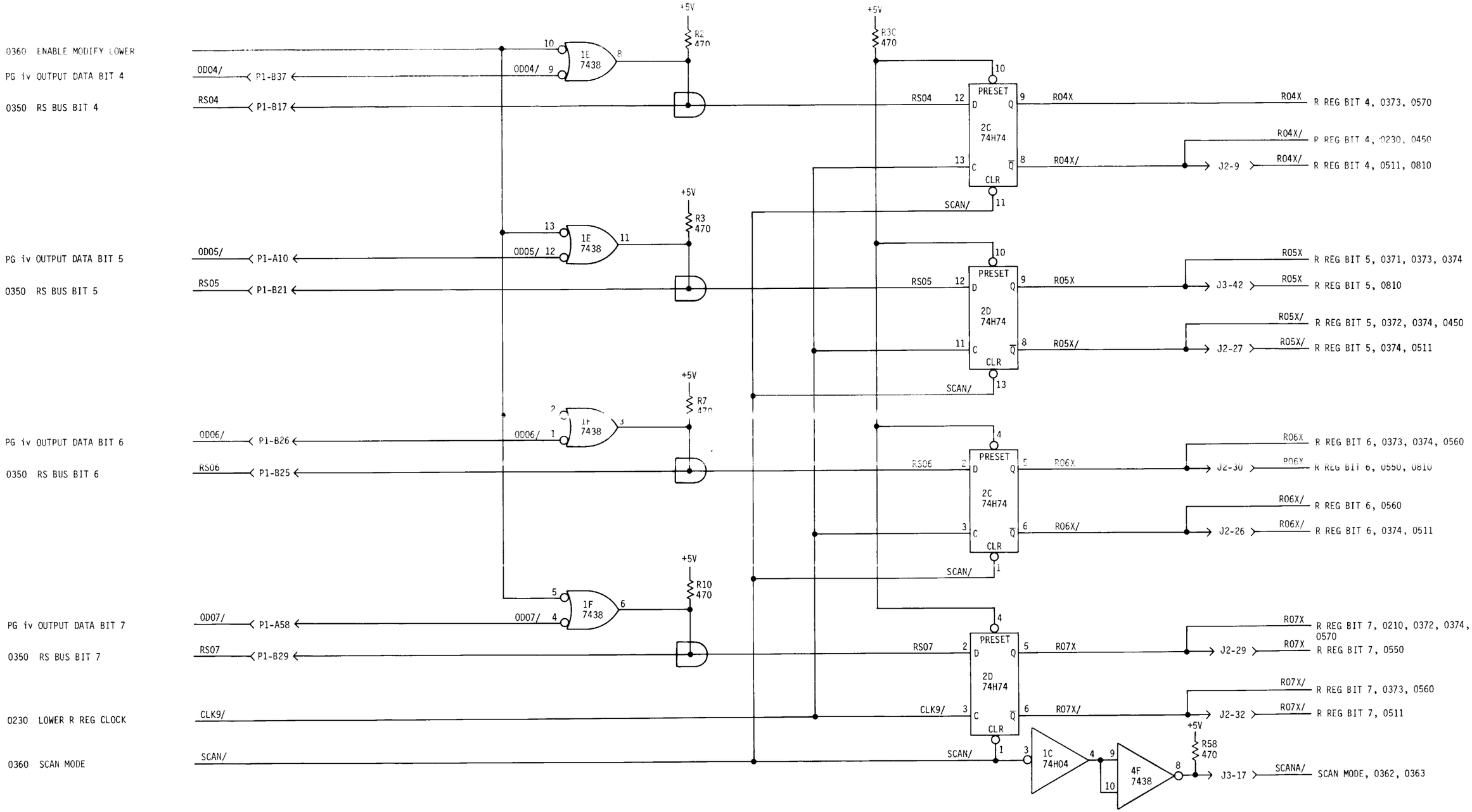

RS BUS AND DRIVERS

FRONT PANEL P.C. BOARD
0351

# LOWER R REGISTER BITS 0-3

0220 FILE BUFFER CLOCK
0211 CLOCK STOP
0371 MODIFY LOWER COMMAND
PG iv OUTPUT DATA BIT 0
0350 RS BUS BIT 0
PG iv OUTPUT DATA BIT 1
0350 RS BUS BIT 1
PG iv OUTPUT DATA BIT 2
0350 RS BUS BIT 2
PG iv OUTPUT DATA BIT 3
0350 RS BUS BIT 3
0230 LOWER R REG CLOCK
0110 SCAN MODE

FLCK/
CSTP/
6H 74H11
ENABLE MODIFY LOWER, 0361
JUXX/
5H 74H04
+5V
R31 470
R32 470
R28 470
R6 470
R29 470
R8 470
1E 7438
1F 7438
OD00/
OD01/
OD02/
OD03/
P1-B39
P1-B10
P1-A26
P1-B58
RS00
RS01
RS02
RS03
P1-B15
P1-A19
P1-A23
P1-A27
PRESET
CLR
2E 74H74
2F 74H74
R00X
R00X/
R01X
R01X/
R02X
R02X/
R03X
R03X/
SCAN/
R REG BIT 0, 0371
R REG BIT 0, 0560
R REG BIT 0, 0510
R REG BIT 1, 0371
R REG BIT 1, 0560
R REG BIT 1, 0510
R REG BIT 2, 0371
R REG BIT 2, 0560
R REG BIT 2, 0510
R REG BIT 3, 0230
R REG BIT 3, 0510
SCAN MODE, 0361
J3-37
J3-39
J3-41
J3-43
CLK9/
P1-A68




LOWER R REGISTER BITS 4-7

J2 CONTROL BOARD
0361

# UPPER R REGISTER BITS 8-11

0361 SCAN MODE
0330 RS BIT 8
0351 RS BUS BIT 8
0340 U REG BIT 0
0230 UPPER R REG CLOCK
0330 RS BIT 9
0351 RS BUS BIT 9
0340 U REG BIT 1
0330 RS BIT 10
0351 RS BUS BIT 10
0340 U REG BIT 2
0330 RS BIT 11
0351 RS BUS BIT 11
0340 U REG BIT 3
0351 RS BUS BIT 12
0351 RS BUS BIT 13
0351 RS BUS BIT 14
0350 RS BUS BIT 0
0350 RS BUS BIT 1
0350 RS BUS BIT 2
0351 RS BUS BIT 15

J3 DATA BOARD

SCANA/ J3-17
RS08 P1-B36
U00X
CLK7/ J3-18
RS09 P1-A37
U01X
RS10 P1-A42
U02X
RS11 P1-A43
U03X

+5V Z3 470 RS08
+5V Z3 470 RS09
+5V Z3 470 RS10
+5V Z3 470 RS11

RENU ENABLE U REG, 0363

1 13 2H 74H51 8
U00X 9
RENU 10

+5V R1 470
CLK7/

10 PRESET 12 D Q 9 R08X/ R REG BIT 8, 0550
4H 74H74
11 C Q 8 J3-7 R08X R REG BIT 8, 0371
CLR R08X R REG BIT 8, 0311, 0540
13

2 3 2H 74H51 6
U01X 4
5

4 PRESET 2 D Q 5 R09X/ R REG BIT 9, 0550
4H 74H74
3 C Q 6 J3-5 R09X R REG BIT 9, 0371
CLR R09X R REG BIT 9, 0311, 0540
1

1 13 2J 74H51 8
U02X 9
10

10 PRESET 12 D Q 9 R10X/ R REG BIT 10, 0550
3J 74H74
11 C Q 8 J3-8 R10X R REG BIT 10, 0371
CLR R10X R REG BIT 10, 0311, 0540
13

2 3 2J 74H51 6
U03X 4
RENU 5

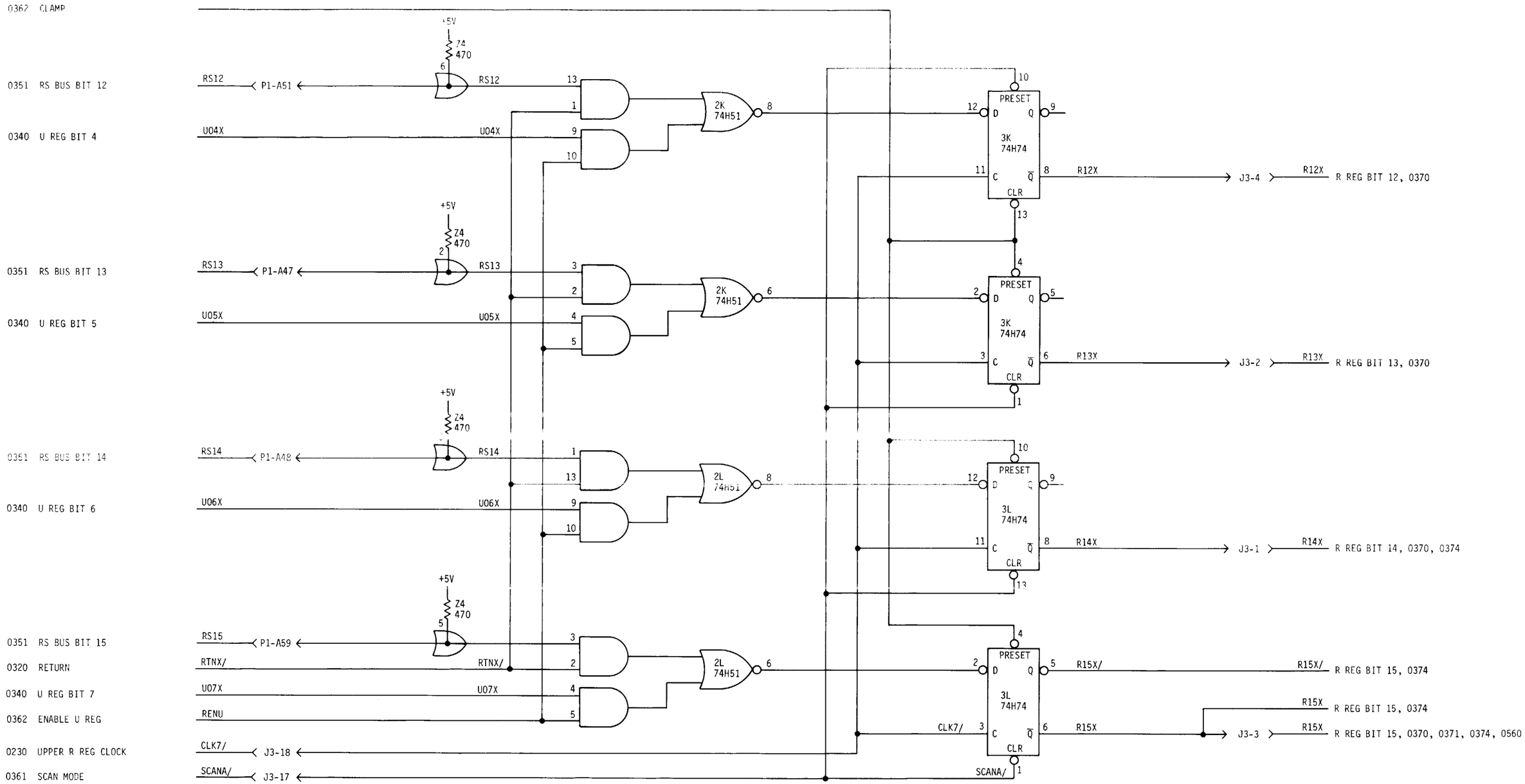
4 PRESET 2 D Q 5 R11X/ R REG BIT 11, 0550
3J 74H74
3 C Q 6 J3-6 R11X R REG BIT 11, 0371
CLR R11X R REG BIT 11, 0311, 0540
1

CLAMP, 0363

J2 CONTROL BOARD

RS12 P1-A51 RS12 10 9
RS13 P1-A47 RS13 6 5 4
RS14 P1-A48 RS14 13 1
RS00 P1-B15 2
RS01 P1-A19 5
RS02 P1-A23 4
RS15 P1-A59 1
3H 74H20 6

U REGISTER ENABLE
3J 74H53 8
J2 15 J3 15




UPPER R REGISTER BITS 12-15

J3 DATA BOARD
0363

# OP CODE DECODER

0363 R REG BIT 12 — R12X — J3-4 — R12X 23 — A0
0363 R REG BIT 13 — R13X — J3-2 — R13X 22 — A1
0363 R REG BIT 14 — R14X — J3-1 — R14X 21 — A2
0363 R REG BIT 15 — R15X — J3-3 — R15X 20 — A3

9L 74154

| | | | |
|---|---|---|---|
| 0 | 1 | JPXX/ | P1-B27 → JPXX/ NOT USED; JPXX/ JUMP EXTENDED, 0372; J2-23 → JPXX/ JUMP EXTENDED, 0311, 0320, 0374 |
| 1 | 2 | LRXX/ | LRXX/ LOAD LITERAL, 0371, 0372 |
| 2 | 3 | LFXX/ | LFXX/ LOAD FILE, 0230, 0372 |
| 3 | 4 | AFXX/ | AFXX/ ADD FILE, 0230 |
| 4 | 5 | TZXX/ | TZXX/ TEST IF ZERO, 0211, 0372 |
| 5 | 6 | TNXX/ | TNXX/ TEST IF NOT ZERO, 0211, 0372 |
| 6 | 7 | CPXX/ | CPXX/ COMPARE FILE, 0560 |
| 7 | 8 | IOXX/ | IOXX/ OP CODE 7, 0371, 0372, 0570; J2-21 → IOXX/ OP CODE 7, 0374 |
| 8 | 9 | ADXX/ | ADXX/ ADD COMMAND, 0372, 0560 |
| 9 | 10 | SBXX/ | SBXX/ SUBTRACT COMMAND, 0372, 0374, 0560; J3-29 → SBXX/ SUBTRACT COMMAND, 0810 |
| A | 11 | MYXX/ | MYXX/ MEMORY READ OR WRITE, 0372, 0374, 0560, 0570; J2-25 → MYXX/ MEMORY READ OR WRITE, 0374 |
| B | 13 | CYXX/ | CYXX/ COPY, 0372 |
| C | 14 | ORXX/ | ORXX/ OR COMMAND, 0372; J3-11 → ORXX/ OR COMMAND, 0520 |
| D | 15 | XRXX/ | J3-10 → XRXX/ EXCLUSIVE OR COMMAND, 0520 |
| E | 16 | ANXX/ | ANXX/ AND WITH FILE, 0372 |
| F | 17 | SHXX/ | SHXX/ SHIFT FILE, 0560 |

18, 19 → E

JPXX/ → 9K 74H04 (1→2) → JPXX → JPXX JUMP EXTENDED, 0371

LRXX/ → 9K 74H04 (13→12) → J3-35 → LRXX LOAD LITERAL, 0311; LRXX LOAD LITERAL, 0210, 0230, 0371, 0610, 0630

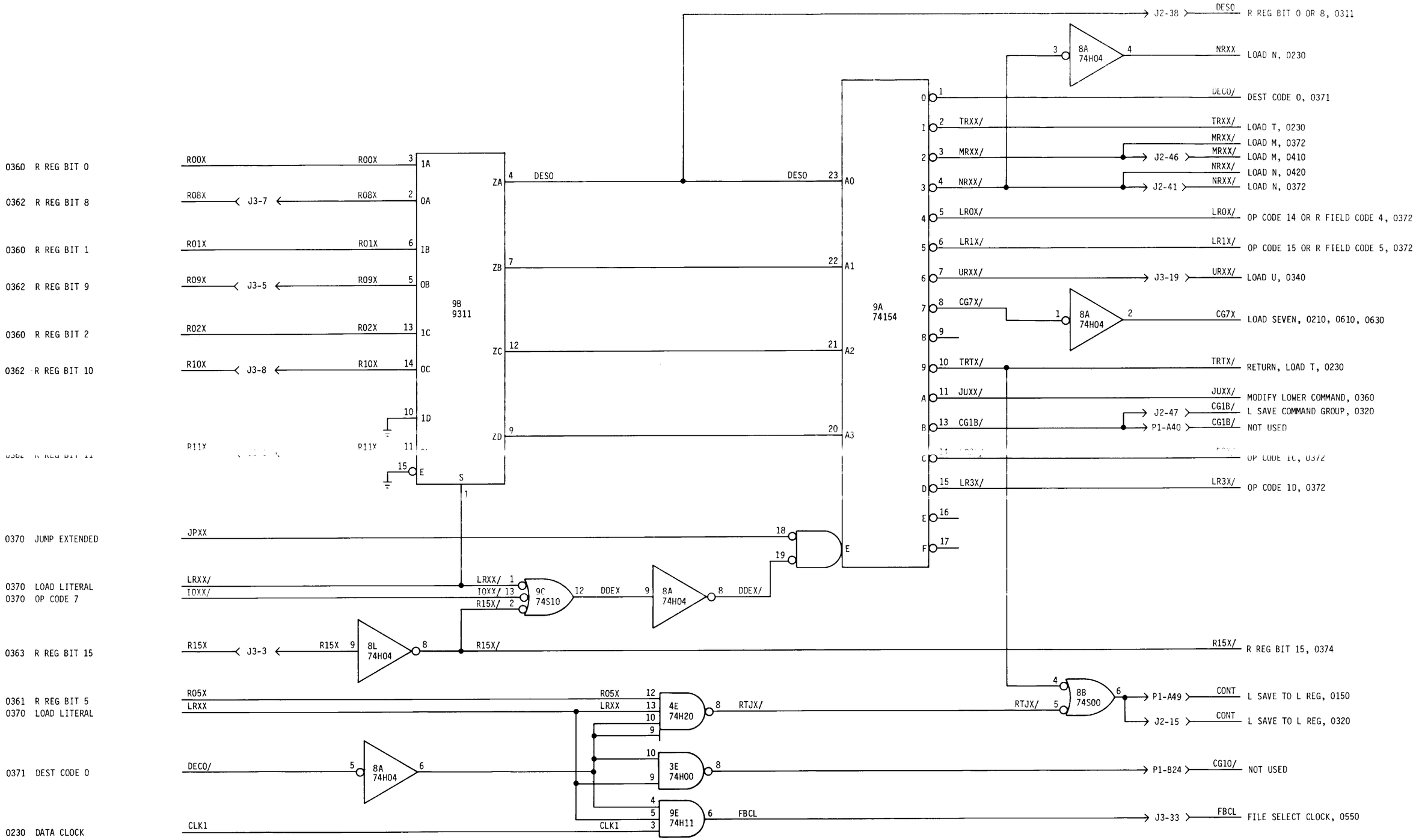
CPXX/ → 9K 74H04 (11→10) → CPXX → CPXX COMPARE FILE, 0211

IOXX/ → 8L 74H04 (5→6) → IOXX OP CODE 7, 0372, 0373

SBXX/ → 9K 74H04 (3→4) → SBXX SUBTRACT COMMAND, 0374, 0560

MYXX/ → 8L 74H04 (3→4) → MYXX MEMORY READ OR WRITE, 0211, 0374, 0450, 0560

SHXX/ → 9K 74H04 (5→6) → SHXX → J2-49 → SHXX SHIFT FILE, 0570; SHXX SHIFT FILE, 0372, 0373, 0560




DESTINATION DECODER

J2 CONTROL BOARD
0371

# SECOND-LEVEL COMMAND DECODES

0211 RUN INHIBIT
0211 CLOCK STOP

RINH/
CSTP/

RINH/ 9
10
11
6B 74H10
8 LRLL/

J2-44 > LRLL/ LOAD L REG, 0310, 0311

0371 OP CODE 1D
0371 OP CODE 1C
0371 OP CODE 15 OR R FIELD CODE 5
0371 OP CODE 14 OR R FIELD CODE 4
0370 JUMP EXTENDED

LR3X/
LR2X/
LR1X/
LROX/
JPXX/

LR3X/ 12
11
LR2X/ 6
LR1X/ 5
4
LROX/ 3
JPXX/ 2
1
7A 74H20
8 LRO1

13 8A 74H04 12 > LRO1/ JUMP, 0211, 0230

LRO1 JUMP, 0210

0370 LOAD FILE
0370 LOAD LITERAL
0370 COPY

LFXX/
LRXX/
CYXX/

13
LFXX/ 12
LRXX/ 10
CYXX/ 9
9J 74H20
8 FINH

J3-45 > FINH FILE INHIBIT, 0550

0361 R REG BIT 5
0370 OP CODE 7

RO5X/
IOXX/

RO5X/ 4
IOXX/ 5
2H 7437
6

J3-28 > IDHT SEL UNCOMP INPUT DATA, 0810

0370 SHIFT FILE

SHXX

RO5X/ 9
SHXX 10
5K 74H00
8 SHLX/

9 6L 74H04 8 > SHLX SHIFT LEFT, 0560

J3-12 > SHLX/ SHIFT LEFT, 0520

0374 OP CODE C, D, E OR F
0370 OR COMMAND

LSGX/
ORXX/

IOXX/ 1
LSGX/ 2
ORXX/ 12
13
8J 74H30
8

11 8L 74H04 10 > J2-48 > ADDX OP CODES 0-3, 6, 8-B, 05/0

0370 AND WITH FILE
0370 TEST IF NOT ZERO
0370 TEST IF ZERO

ANXX/
TNXX/
TZXX/

EXIO 6
ANXX/ 3
TNXX/ 4
TZXX/ 5

4
5
2
1
9J 74H20
6

9 9K 74H04 8 > J3-21 > ANDX/ LOGICAL AND, 0520

0370 OP CODE 7
0361 R REG BIT 7

IOXX
RO7X

IOXX 5
RO7X 4
8K 74S00
6 EXIO

J2-37 > EXIO EXTERNAL I/O COMMAND, 0810

0370 ADD COMMAND
0370 SUBTRACT COMMAND
0370 MEMORY READ OR WRITE
0370 COPY

ADXX/
SBXX/
MYXX/
CYXX/

ADXX/ 1
SBXX/ 4
MYXX/ 5
CYXX/ 2
7J 74H22
6

+5V
R53 470

9 7H 74H04 8 > J2-7 > TONY/ OP CODES 8-B, 0374

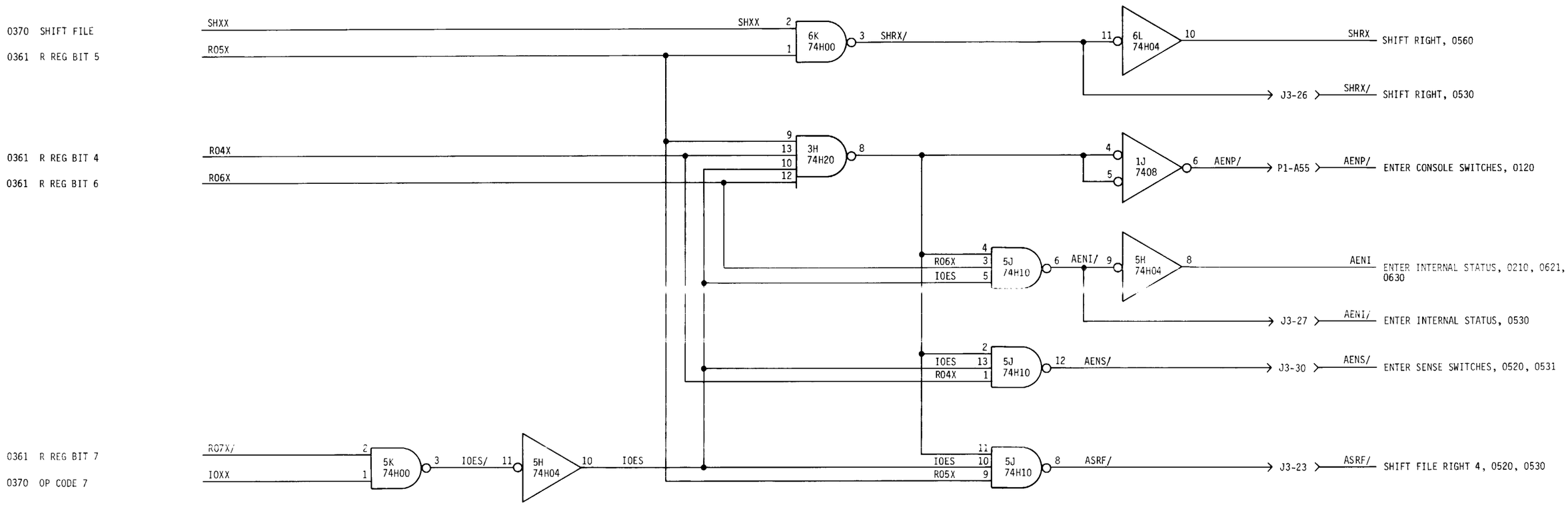
0371 LOAD N
0371 LOAD M

NRXX/
MRXX/

NRXX/ 2
MRXX/ 1
8B 74S00
3 MNRX

11 8A 74H04 10 > MNRX/ M OR N REG SELECT, 0560

MNRX M OR N REG SELECT, 0211, 0560




A BUS DATA SELECT DECODES

J2 CONTROL BOARD
0373

# B BUS DATA SELECT DECODES

J2 CONTROL BOARD

0361 R REG BIT 7
0361 R REG BIT 6
0363 R REG BIT 14
0363 R REG BIT 15

R07X
R06X
R14X
R15X
4C 7408
8K 74S00
MYDX
LSGX/
J3-1
J3-3

MYDX — CODE 01 IN C FIELD BITS 7 AND 6, 0560
LSGX/ — OP CODE C, D, E OR F, 0372

8L 74H04

0370 SUBTRACT COMMAND

SBXX/
R15X
8K 74S00
BNTP1/

0370 MEMORY READ OR WRITE
0361 R REG BIT 5
0374 INPUT DATA TO B BUS

MYXX/
R05X
BENI
J2-28

R06X
8H 74H53
J2-12
J3 DATA BOARD
BNTP — SEL UNCOMP T REG TO B BUS, 0510, 0511

6A 7486
BTXR — T REG TRANSFER TO B BUS, 0211

0370 MEMORY READ OR WRITE

MYXX
7H 74H04
7F 74H00
BNTM1
SBXX
8F 74H53
J2-6
BNTM — SEL COMP T REG TO B BUS, 0510, 0511

0370 SUBTRACT COMMAND

SBXX
BNTM2

0361 R REG BIT 5
0363 R REG BIT 15

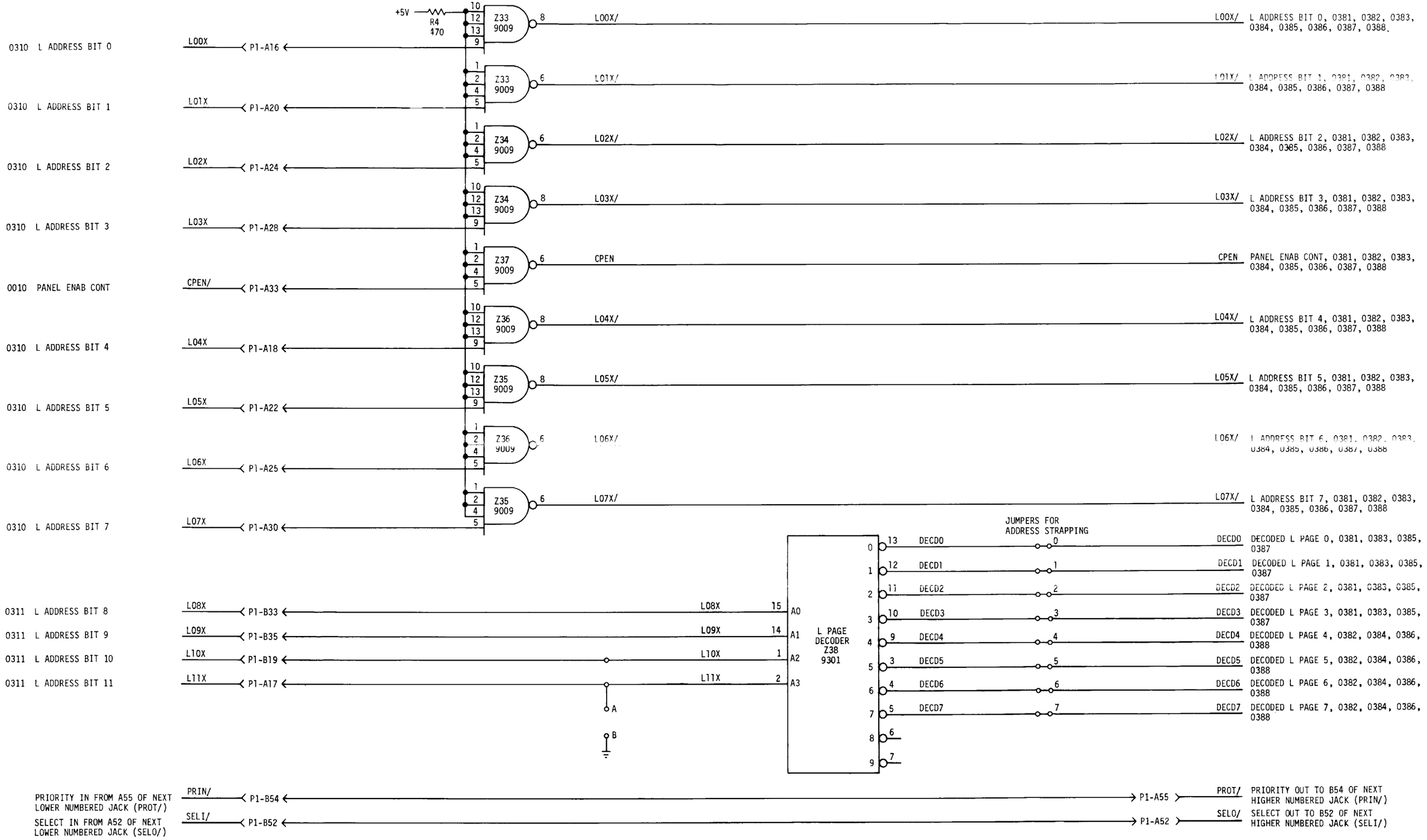
R05X/
R15X/

0370 JUMP EXTENDED
0371 R REG BIT 10
0370 OP CODE 7
0361 R REG BIT 5
0361 R REG BIT 6
0372 OP CODES 8-B

JPXX/
IOXX/
R05X/
R06X/
TONY/
J2-23
J2-21
J2-27
J2-26
J2-7
7F 74H20
6A 7486
7D 74H10
BEIA
7E 74H00
BENR — R REG TO B BUS, 0510, 0511
BENR/ — R REG TO B BUS, 0230
BENR/ — R REG TO B BUS, 0311, 0570
6B 74H51
BENI — INPUT DATA TO B BUS, 0374
BENI — INPUT DATA TO B BUS, 0510, 0511

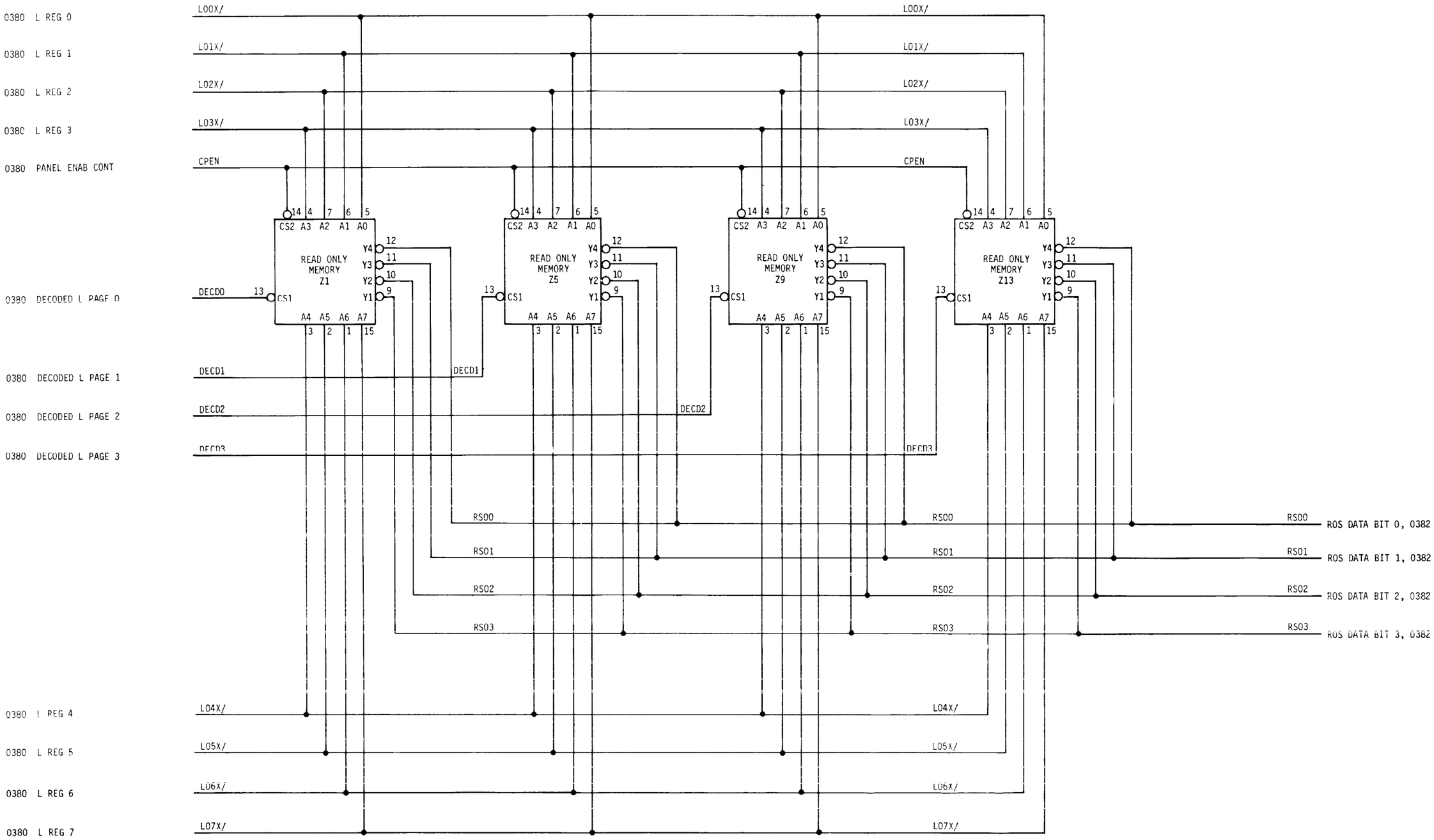
0363 R REG BIT 15
0370 MEMORY READ OR WRITE
0810 I/O CONT REG 3

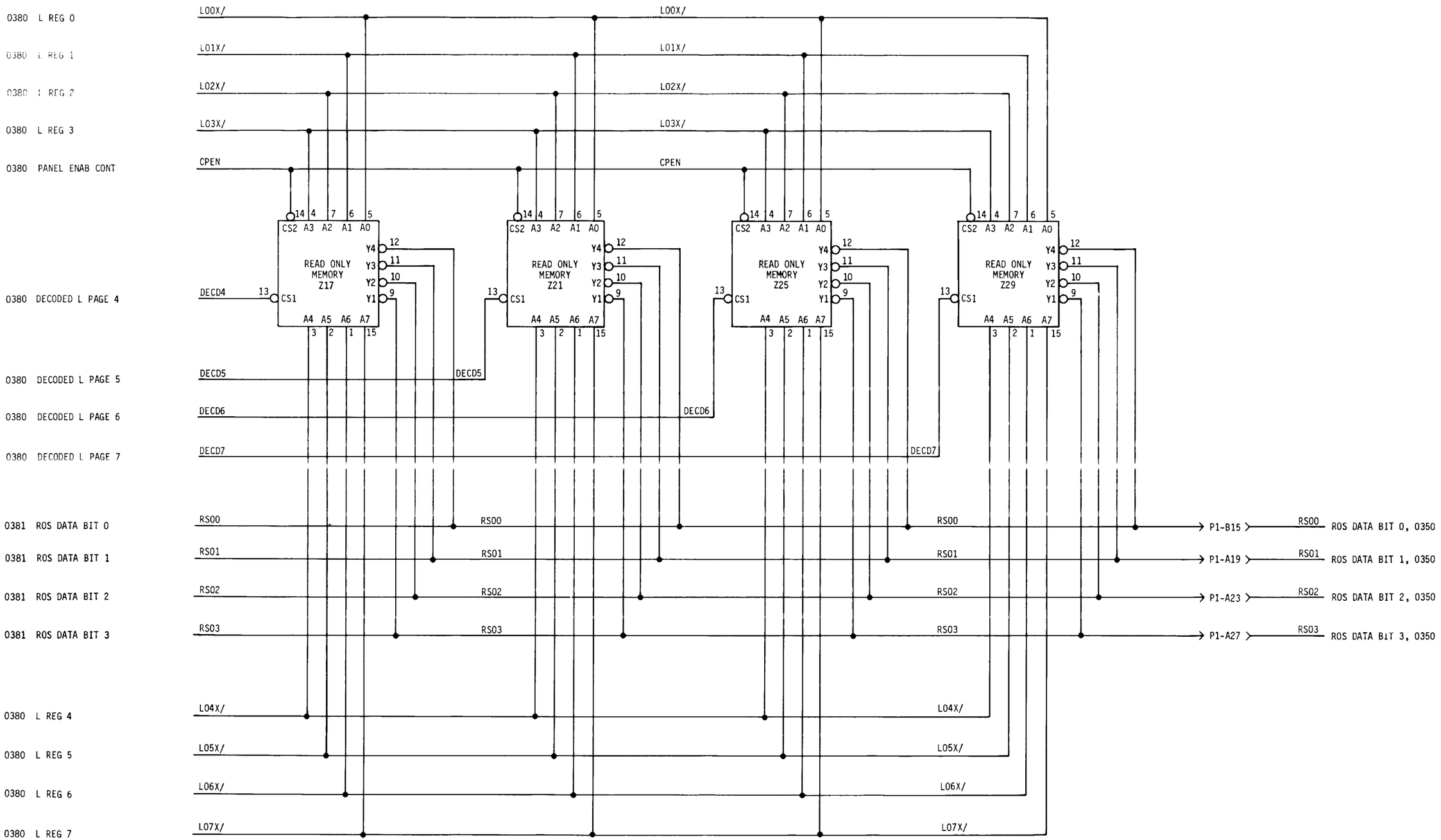
R15X
MYXX/
IO3X/
J2-25




READ ONLY MEMORY CONTROL

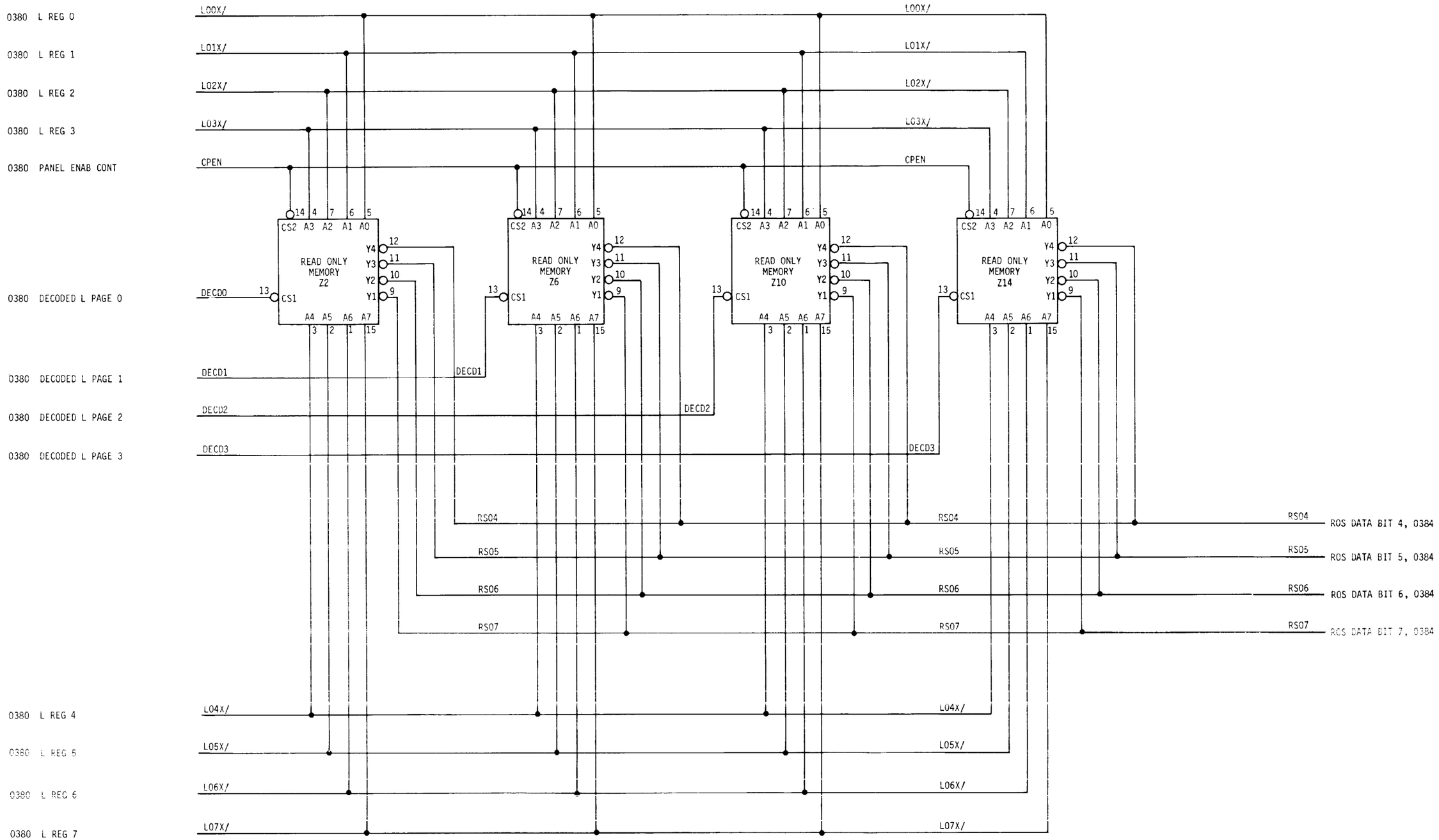
READ ONLY MEMORY BOARD
0380


0380 L REG 0
0380 L REG 1
0380 L REG 2
0380 L REG 3
0380 PANEL ENAB CONT
0380 DECODED L PAGE 0
0380 DECODED L PAGE 1
0380 DECODED L PAGE 2
0380 DECODED L PAGE 3
0380 L REG 4
0380 L REG 5
0380 L REG 6
0380 L REG 7
L00X/
L01X/
L02X/
L03X/
CPEN
DECD0
DECD1
DECD2
DECD3
L04X/
L05X/
L06X/
L07X/
RS00
RS01
RS02
RS03
CS2 A3 A2 A1 A0
A4 A5 A6 A7
CS1
Y4 Y3 Y2 Y1
READ ONLY MEMORY Z1
READ ONLY MEMORY Z5
READ ONLY MEMORY Z9
READ ONLY MEMORY Z13
ROS DATA BIT 0, 0382
ROS DATA BIT 1, 0382
ROS DATA BIT 2, 0382
ROS DATA BIT 3, 0382

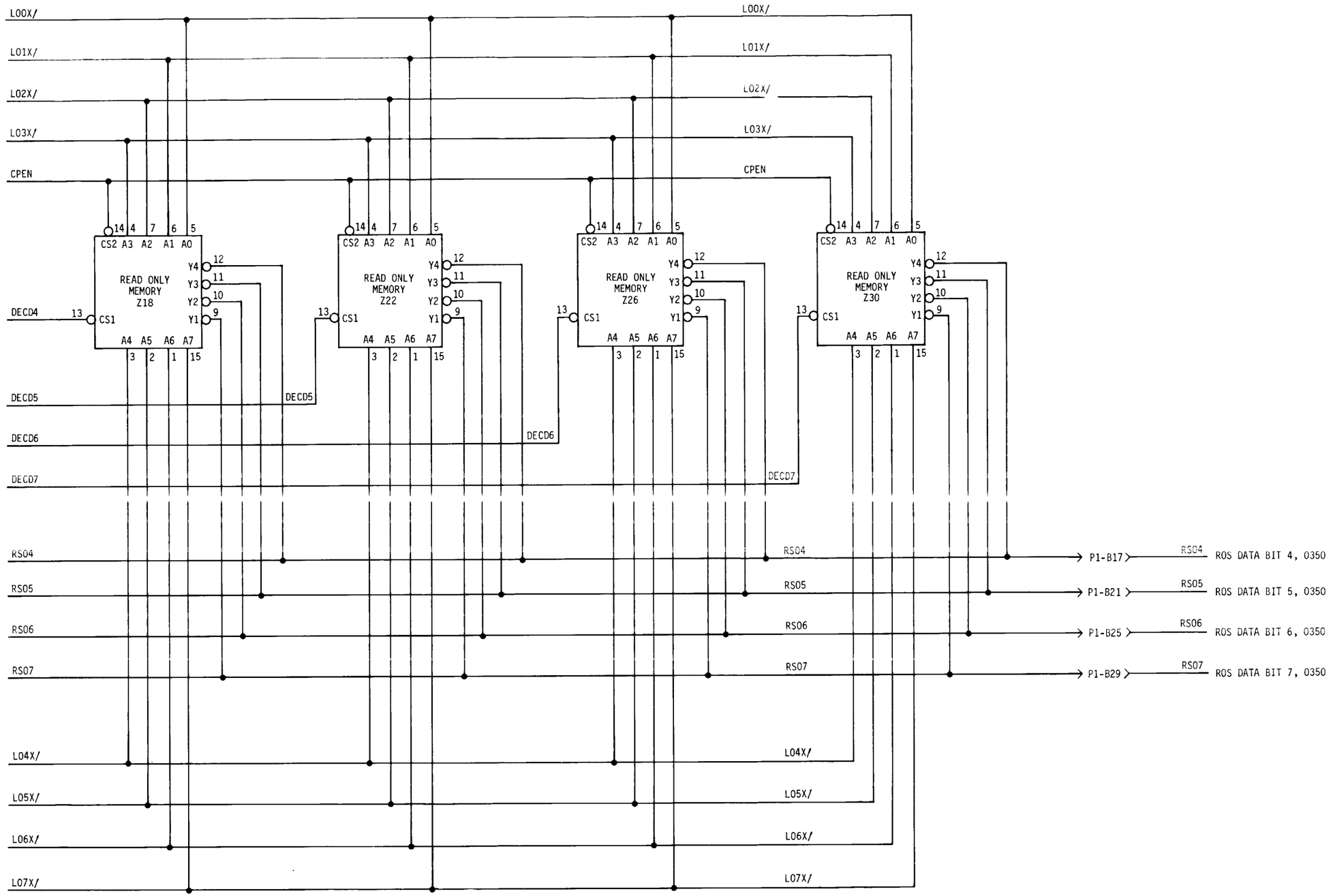



READ ONLY MEMORY BITS 17, 21, 25, 29

READ ONLY MEMORY BOARD
0382


0380 L REG 0
0380 L REG 1
0380 L REG 2
0380 L REG 3
0380 PANEL ENAB CONT
0380 DECODED L PAGE 0
0380 DECODED L PAGE 1
0380 DECODED L PAGE 2
0380 DECODED L PAGE 3
0380 L REG 4
0380 L REG 5
0380 L REG 6
0380 L REG 7
L00X/
L01X/
L02X/
L03X/
CPEN
DECD0
DECD1
DECD2
DECD3
L04X/
L05X/
L06X/
L07X/
CS2 A3 A2 A1 A0
CS1
A4 A5 A6 A7
Y4 Y3 Y2 Y1
READ ONLY MEMORY Z2
READ ONLY MEMORY Z6
READ ONLY MEMORY Z10
READ ONLY MEMORY Z14
RS04
RS05
RS06
RS07
ROS DATA BIT 4, 0384
ROS DATA BIT 5, 0384
ROS DATA BIT 6, 0384
ROS DATA BIT 7, 0384

0380 L REG 0
0380 L REG 1
0380 L REG 2
0380 L REG 3
0380 PANEL ENAB CONT
0380 DECODED L PAGE 4
0380 DECODED L PAGE 5
0380 DECODED L PAGE 6
0380 DECODED L PAGE 7
0383 ROS DATA BIT 4
0383 ROS DATA BIT 5
0383 ROS DATA BIT 6
0383 ROS DATA BIT 7
0380 L REG 4
0380 L REG 5
0380 L REG 6
0380 L REG 7




READ ONLY MEMORY BITS 18, 22, 26, 30

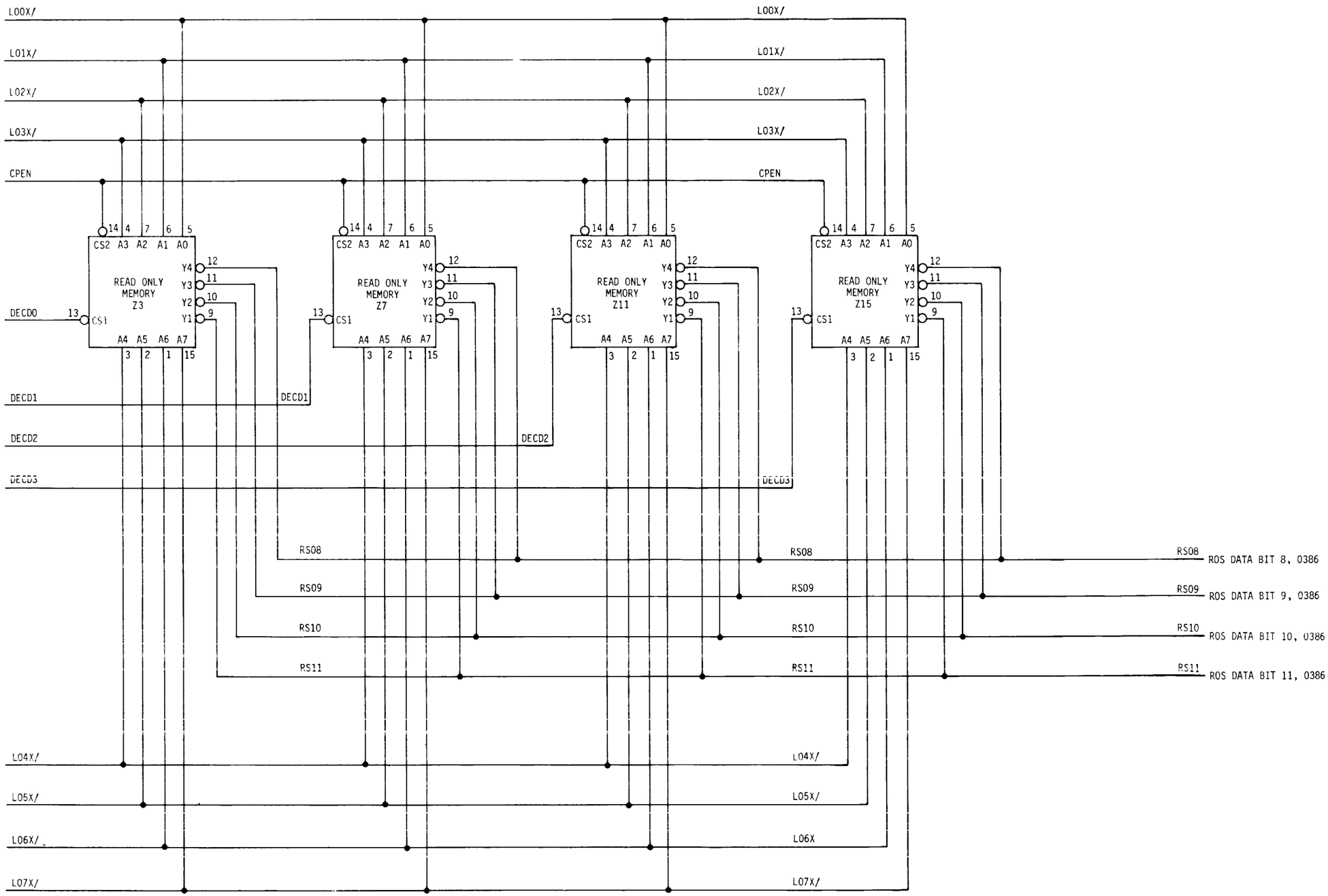
READ ONLY MEMORY BOARD
0384

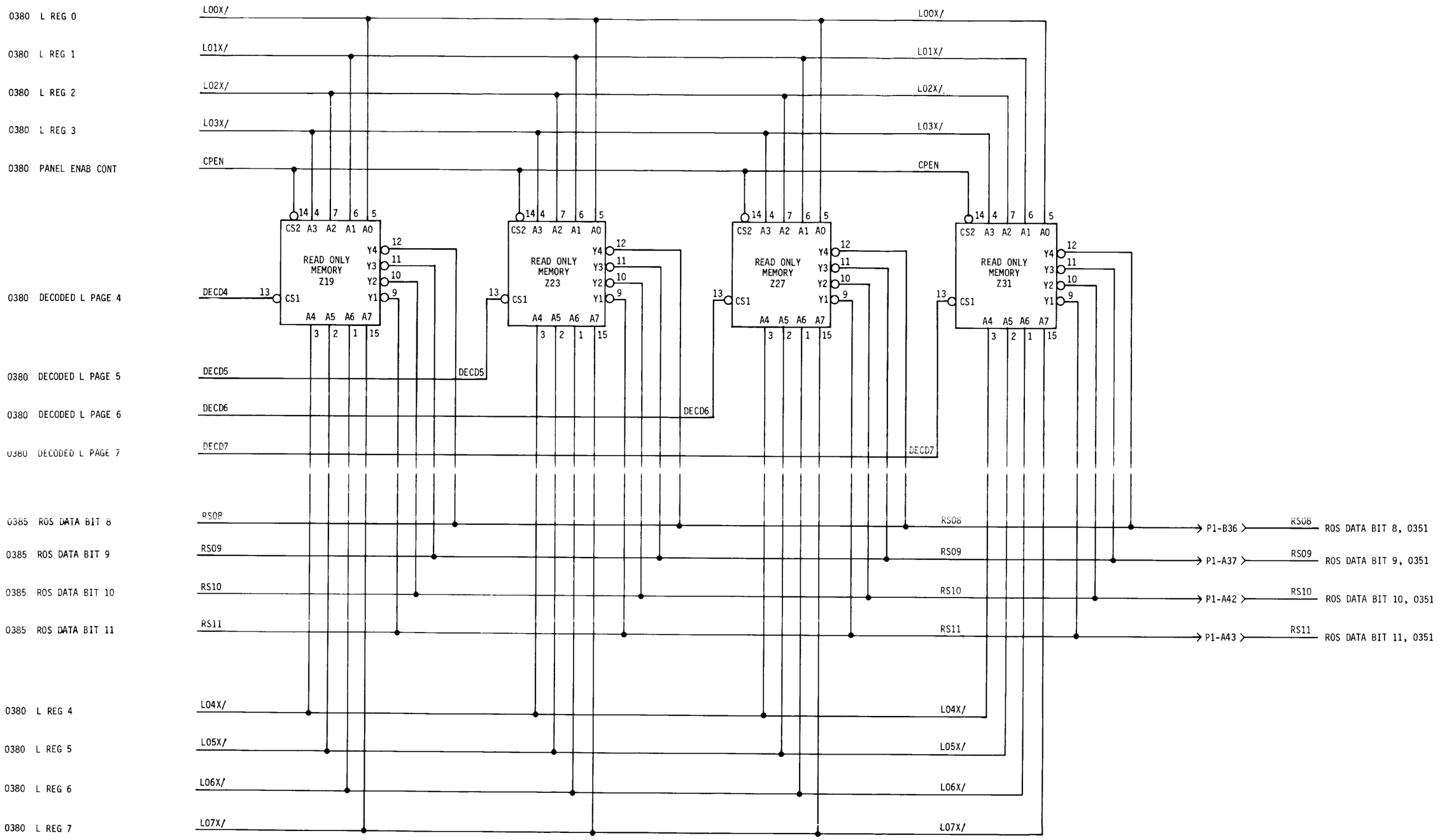
# READ ONLY MEMORY BITS 3, 7, 11, 15

0380 L REG 0
0380 L REG 1
0380 L REG 2
0380 L REG 3
0380 PANEL ENAB CONT

0380 DECODED L PAGE 0
0380 DECODED L PAGE 1
0380 DECODED L PAGE 2
0380 DECODED L PAGE 3

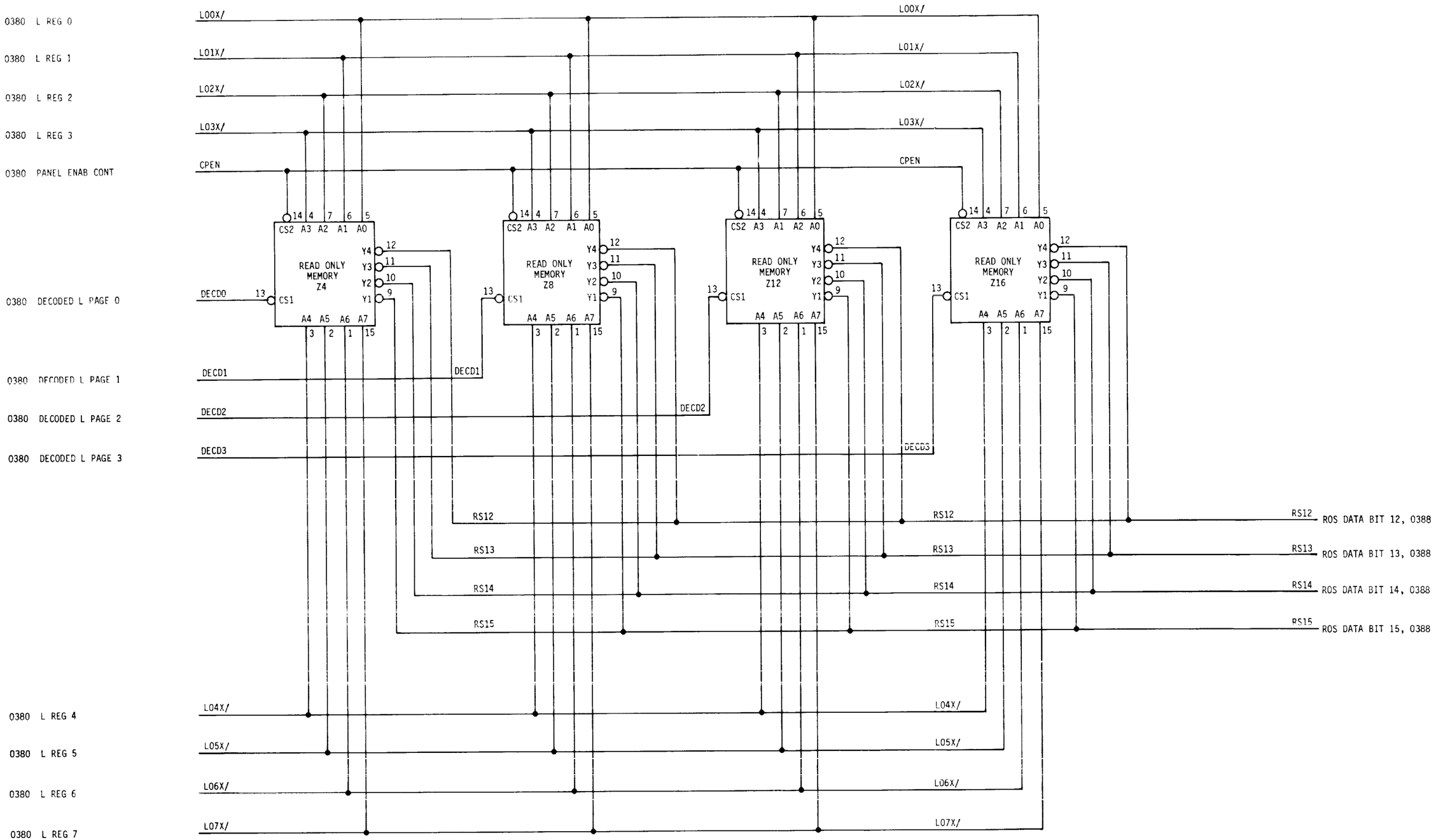
0380 L REG 4
0380 L REG 5
0380 L REG 6
0380 L REG 7

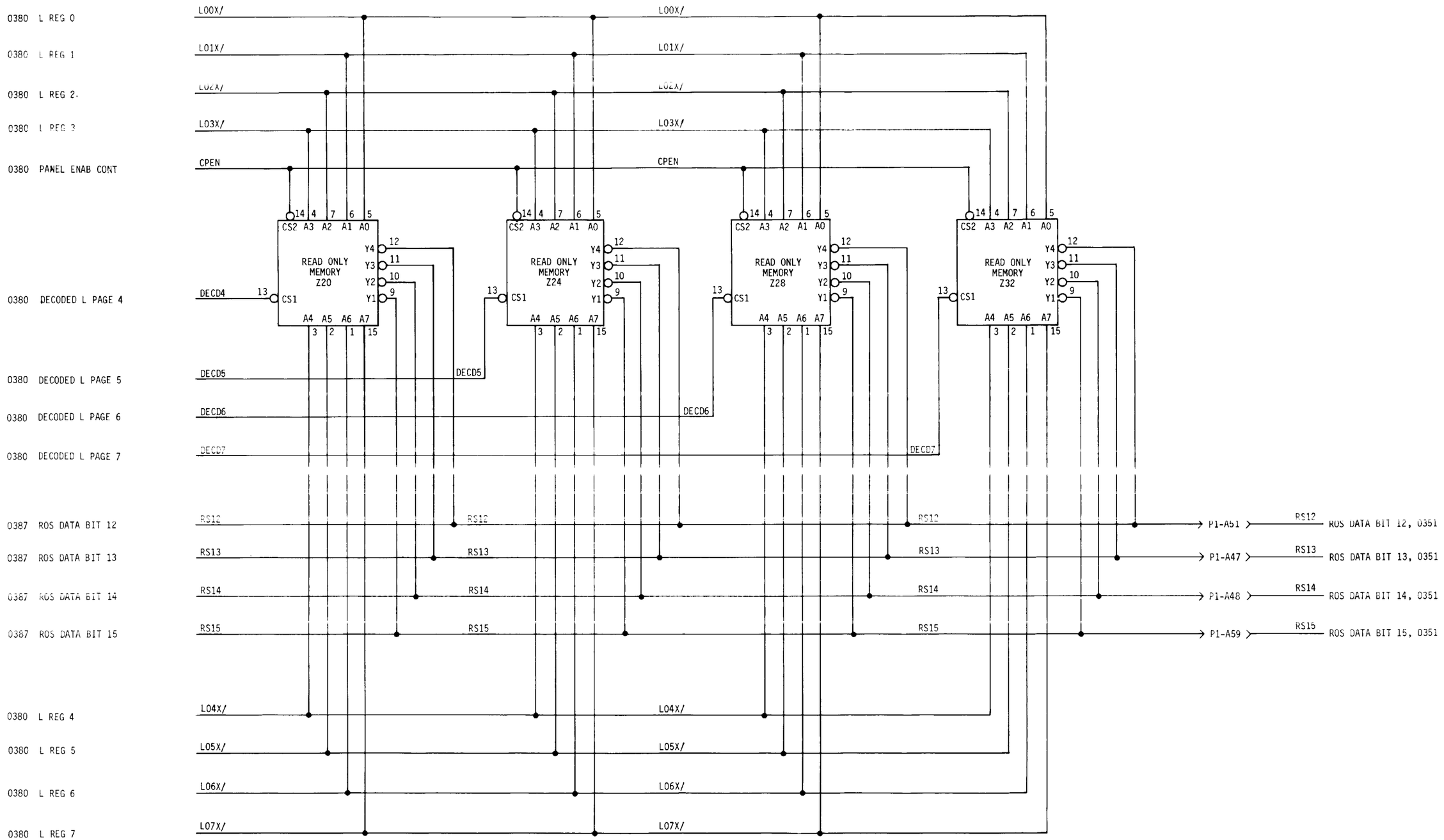





READ ONLY MEMORY BITS 19, 23, 27, 31

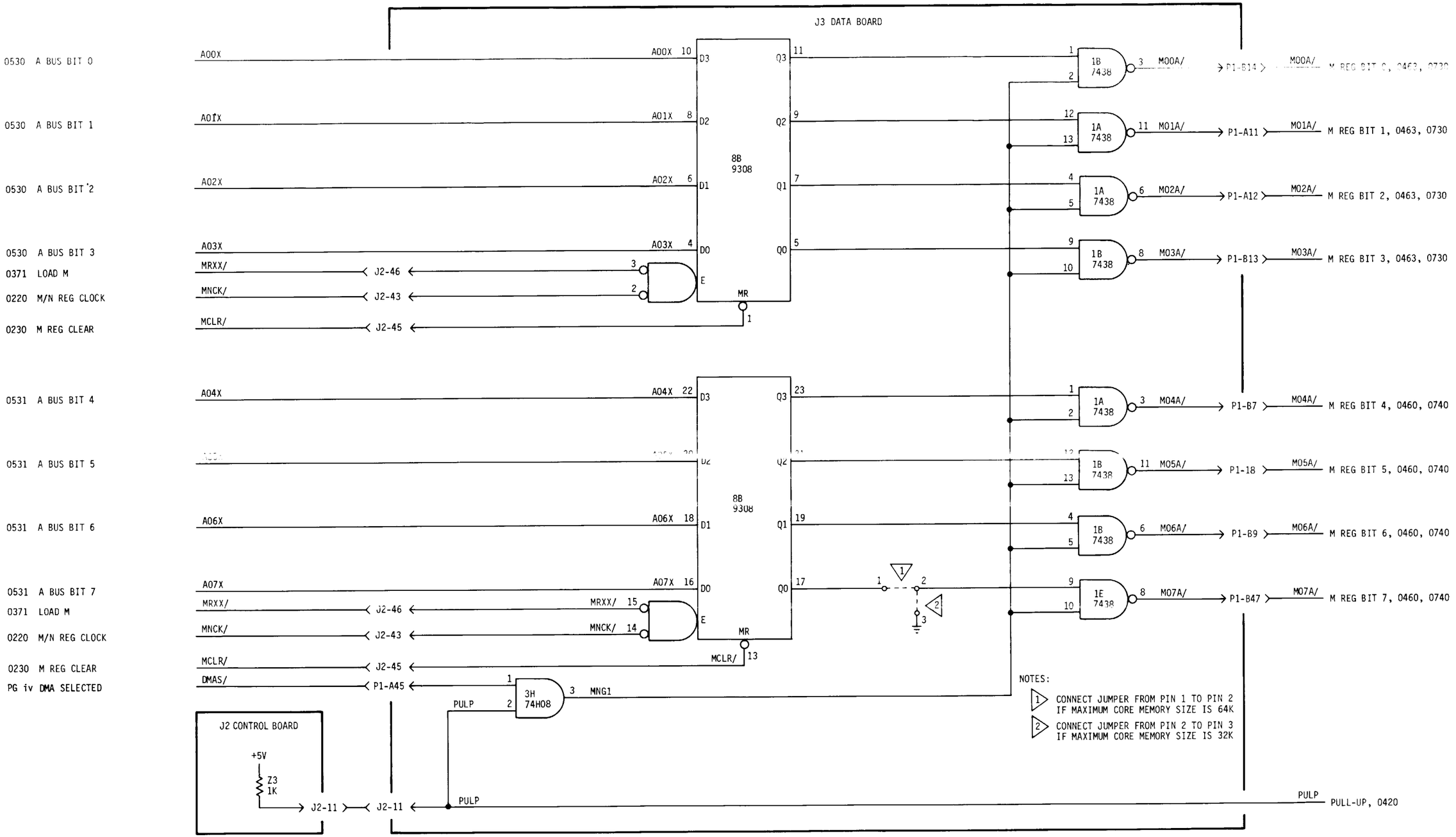
READ ONLY MEMORY BOARD
0386


0380 L REG 0
0380 L REG 1
0380 L REG 2
0380 L REG 3
0380 PANEL ENAB CONT
0380 DECODED L PAGE 0
0380 DECODED L PAGE 1
0380 DECODED L PAGE 2
0380 DECODED L PAGE 3
0380 L REG 4
0380 L REG 5
0380 L REG 6
0380 L REG 7
L00X/
L01X/
L02X/
L03X/
CPEN
L04X/
L05X/
L06X/
L07X/
DECD0
DECD1
DECD2
DECD3
READ ONLY MEMORY Z4
READ ONLY MEMORY Z8
READ ONLY MEMORY Z12
READ ONLY MEMORY Z16
CS2 A3 A2 A1 A0
CS1
A4 A5 A6 A7
Y4 Y3 Y2 Y1
RS12
RS13
RS14
RS15
RS12 ROS DATA BIT 12, 0388
RS13 ROS DATA BIT 13, 0388
RS14 ROS DATA BIT 14, 0388
RS15 ROS DATA BIT 15, 0388




READ ONLY MEMORY BITS 20, 24, 28, 32

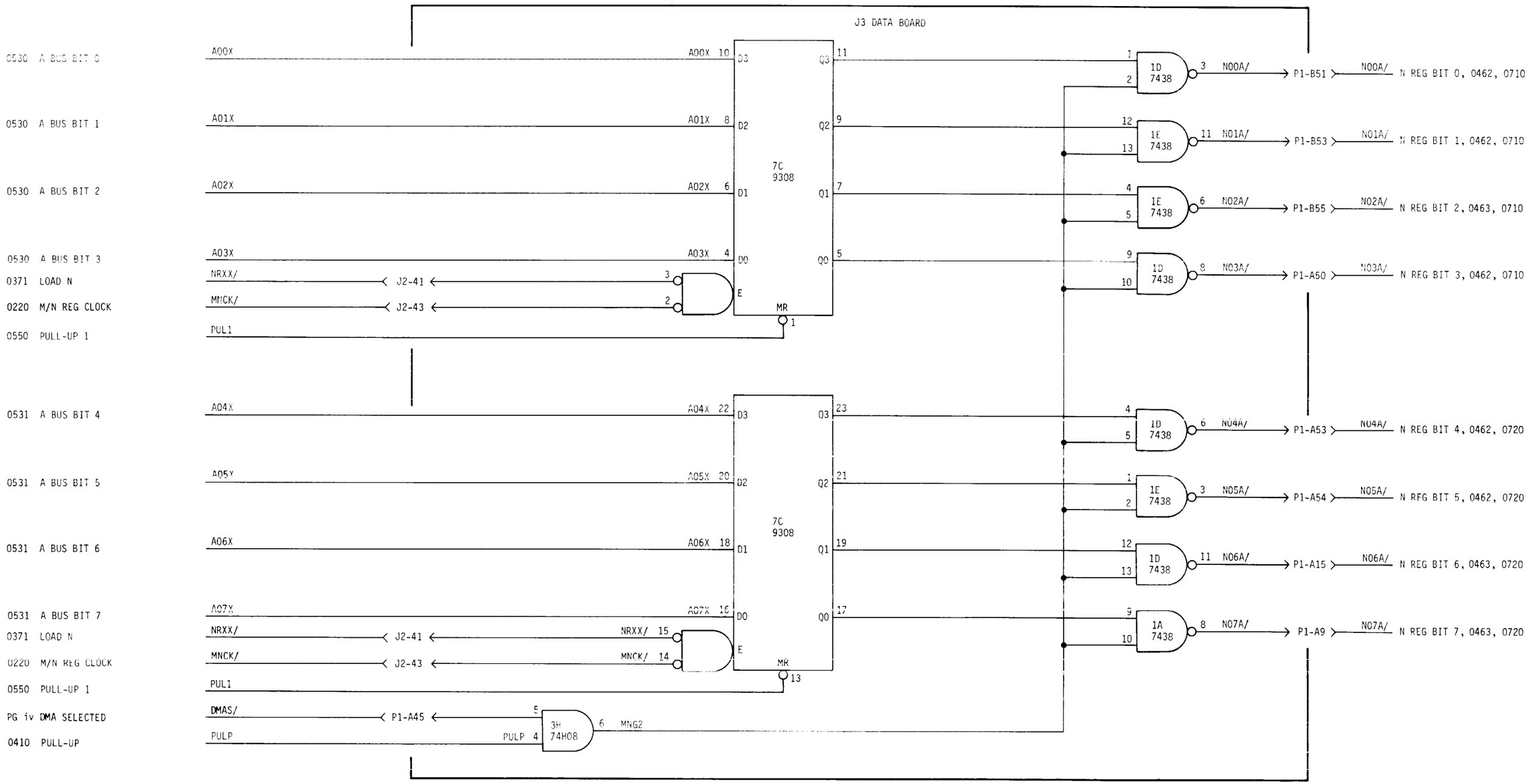
READ ONLY MEMORY BOARD
0388

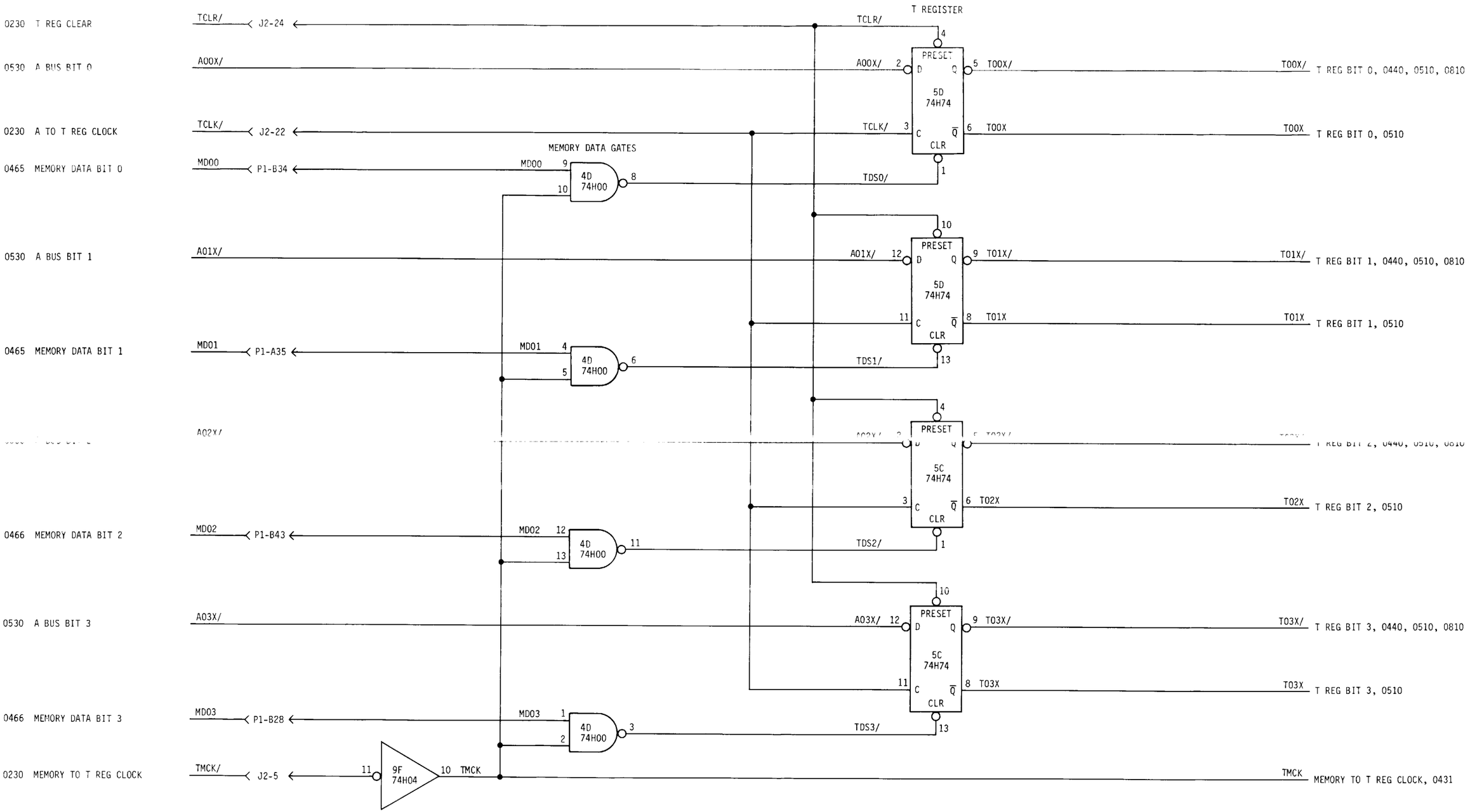



M REGISTER

J2 CONTROL BOARD
AND J3 DATA BOARD
0410

# N REGISTER

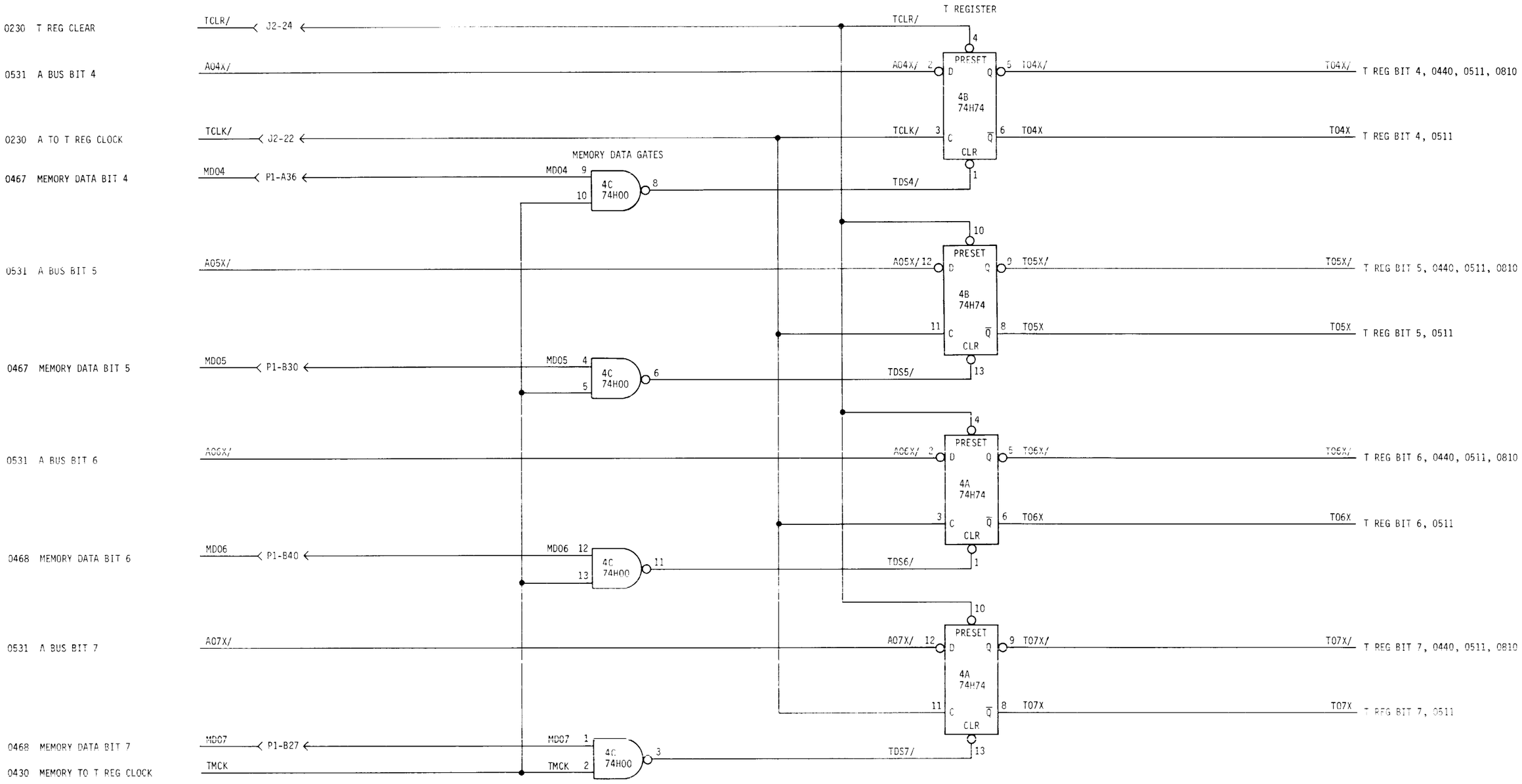

J3 DATA BOARD
0530 A BUS BIT 0
0530 A BUS BIT 1
0530 A BUS BIT 2
0530 A BUS BIT 3
0371 LOAD N
0220 M/N REG CLOCK
0550 PULL-UP 1
0531 A BUS BIT 4
0531 A BUS BIT 5
0531 A BUS BIT 6
0531 A BUS BIT 7
0371 LOAD N
0220 M/N REG CLOCK
0550 PULL-UP 1
PG iv DMA SELECTED
0410 PULL-UP
A00X
A01X
A02X
A03X
A04X
A05X
A06X
A07X
NRXX/
MNCK/
PUL1
J2-41
J2-43
7C 9308
D3
D2
D1
D0
Q3
Q2
Q1
Q0
E
MR
1D 7438
1E 7438
1A 7438
N00A/
N01A/
N02A/
N03A/
N04A/
N05A/
N06A/
N07A/
P1-B51
P1-B53
P1-B55
P1-A50
P1-A53
P1-A54
P1-A15
P1-A9
N REG BIT 0, 0462, 0710
N REG BIT 1, 0462, 0710
N REG BIT 2, 0463, 0710
N REG BIT 3, 0462, 0710
N REG BIT 4, 0462, 0720
N REG BIT 5, 0462, 0720
N REG BIT 6, 0463, 0720
N REG BIT 7, 0463, 0720
DMAS/
PULP
P1-A45
3H 74H08
MNG2

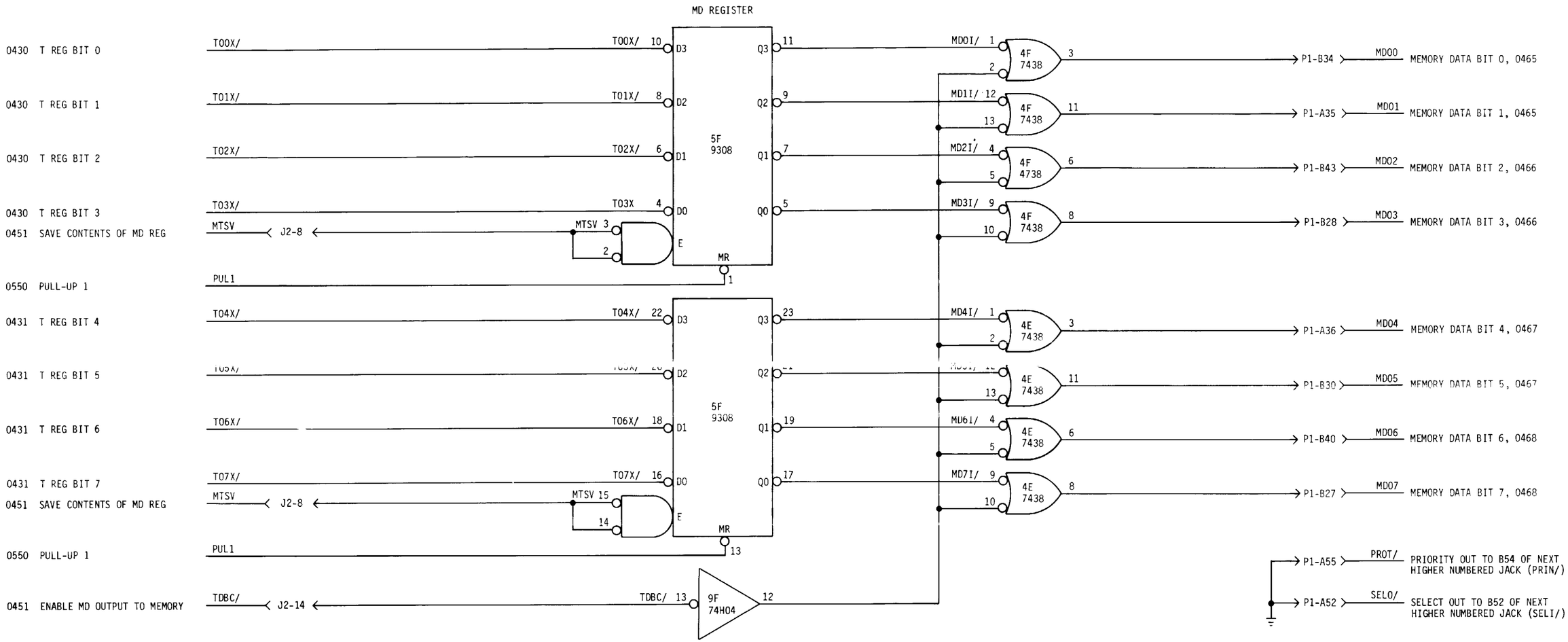



MEMORY DATA GATES AND T REGISTER BITS 0-3

J3 DATA BOARD
0430

# MEMORY DATA GATES AND T REGISTER BITS 4-7






MEMORY DATA (MD) REGISTER, PRIORITY/SELECT

J3 DATA BOARD
0440

# MEMORY CONTROL 1

PG iv MASTER RESET

0220 MEMORY CLOCK PHASE 1
0220 MEMORY CLOCK PHASE 2
0451 WRITE INHIBIT 0 S

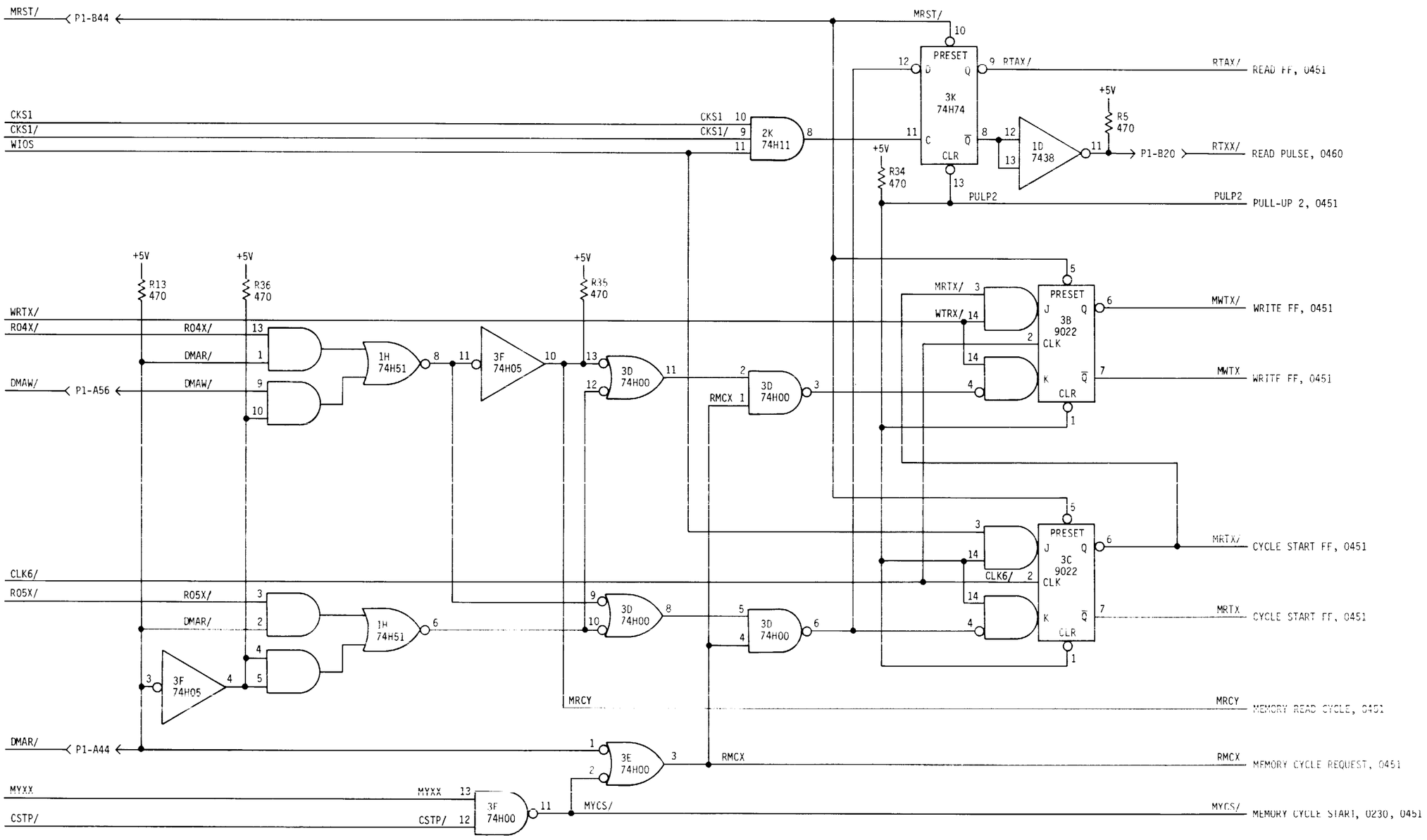
0451 WRITE PULSE INTERNAL
0361 R REG BIT 4

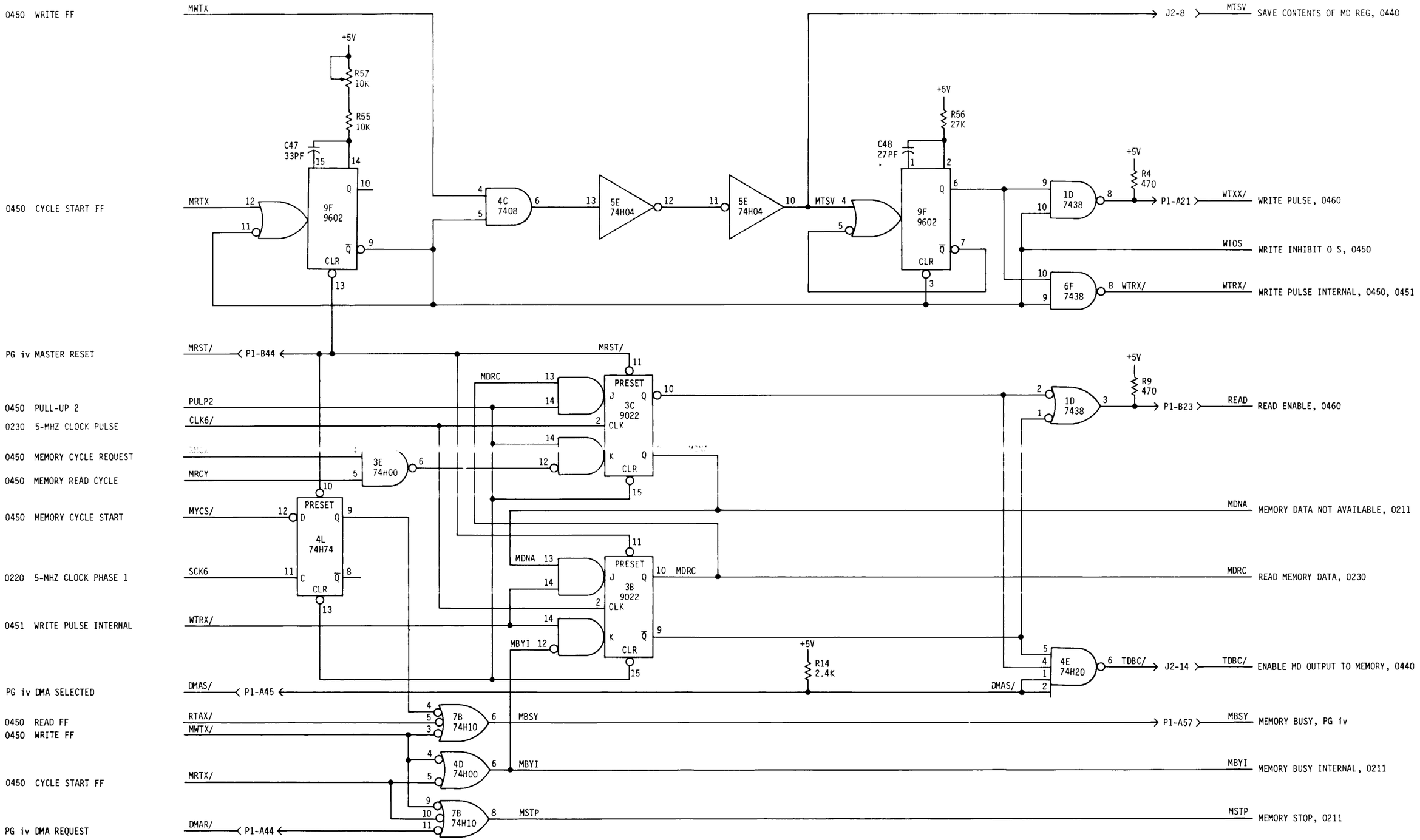
PG iv DMA WRITE

0230 5-MHZ CLOCK PHASE 2
0361 R REG BIT 5

PG iv DMA REQUEST

0370 MEMORY READ OR WRITE
0211 CLOCK STOP






MEMORY CONTROL 2

J2 CONTROL BOARD
0451

# MEMORY TIMING AND CONTROL

PG iv MASTER RESET

0450 READ PULSE

0410 M REG BIT 7

3 MEMORY SELECT 3

0410 M REG BIT 6

PG iv M REG BIT 6

3 MEMORY SELECT 2

0410 M REG BIT 5

PG iv M REG BIT 5

3 MEMORY SELECT 1

0451 WRITE PULSE

NOTES:

1. R2 AND R16 SELECTED FOR 345 ηSEC OUTPUT AT PIN 7 OR 9.
2. C10 MAY BE ADDED IN TEST.
3. PINS B12, B16, and B45 ARE CONNECTED AS SHOWN IN THE CHART BELOW

| MEMORY SIZE | | 8K | 16K | 24K | 32K | 40K | 48K | 56K | 64K |
|---|---|---|---|---|---|---|---|---|---|
| | SLOT | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 |
| SIGNAL | PIN | | | | | | | | |
| MS1 | B12 | N/C | GRD | N/C | GRD | N/C | GRD | N/C | GRD |
| MS2 | B16 | N/C | N/C | GRD | GRD | N/C | N/C | GRD | GRD |
| MS3 | B45 | N/C | N/C | N/C | N/C | GRD | GRD | GRD | GRD |

MRST/ P1-B44

RTXX/ P1-B20

MO7A/ P1-B47

MS3 P1-B45

MO6A/ P1-B9

MO6A/

MS2 P1-B16

MO5A/ P1-B18

MO5A/

MS1 P1-B12

WTXX/ P1-A21

R142 1K, R144 1K, R145 470, R146 4.7K, +5V

Z6 8242, Z4 74H11 (8 MEN), MOS

C4 100pf, R1 10K, R2

Z2 9602 (345 ηSEC) — RTXX/, YRXX

C5 100pf, R15 10K, R16

Z2 9602 (345 ηSEC) — WTXX/, YWXX

YRXX/, YWXX/, MRST/, MEN

Z7 74H11 → EDEC/ ENABLE DECODER, 0462, 0463, 0540

Z7 74411

Z7 74H11 → DCTO/ DRIVE CURRENT TURN-OFF, 0461

YRXX/ Y READ PULSE, 0461

YWXX/ Y WRITE PULSE, 0461

YWXX

Z5 9322 (RAS, YRXX/, YWXX/, MEN, YWXX)

7a → $\bar{O}$ROW/ X WRITE/READ PULSE, 0461

7b → OR$\bar{O}$W/ X READ/WRITE PULSE, 0461

7c → $\bar{O}$RAS READ AMP STROBE UPPER STACK, 0465, 0466, 0467, 0468

7d → ORAS READ AMP STROBE LOWER STACK, 0465, 0466, 0467, 0468

Z1 9602 (≈ 200 ηSEC) — 6 MCLR, MCLR/, MCLR

R39 10K, C9 47pf, R47 10K

C10, R40 4.7K

Z1 9602 (50-70 ηSEC) — 10 RAS, RAS/

Z3 9016 → IOTO INHIBIT CURRENT TURN-OFF, 0464

Z3 9016 → MCLR/ MEMORY LATCH CLEAR, 0465, 0466, 0467, 0468

Z4 74H11 → $\bar{O}$.WT WRITE LOWER STACK, 0465, 0466, 0467, 0468

Z4 74H11 → O.WT WRITE UPPER STACK, 0465, 0466, 0467, 0468

M04A

0410 M REG BIT 4

PG iv M REG BIT 4

M04A/ P1-B7

Z3 9016

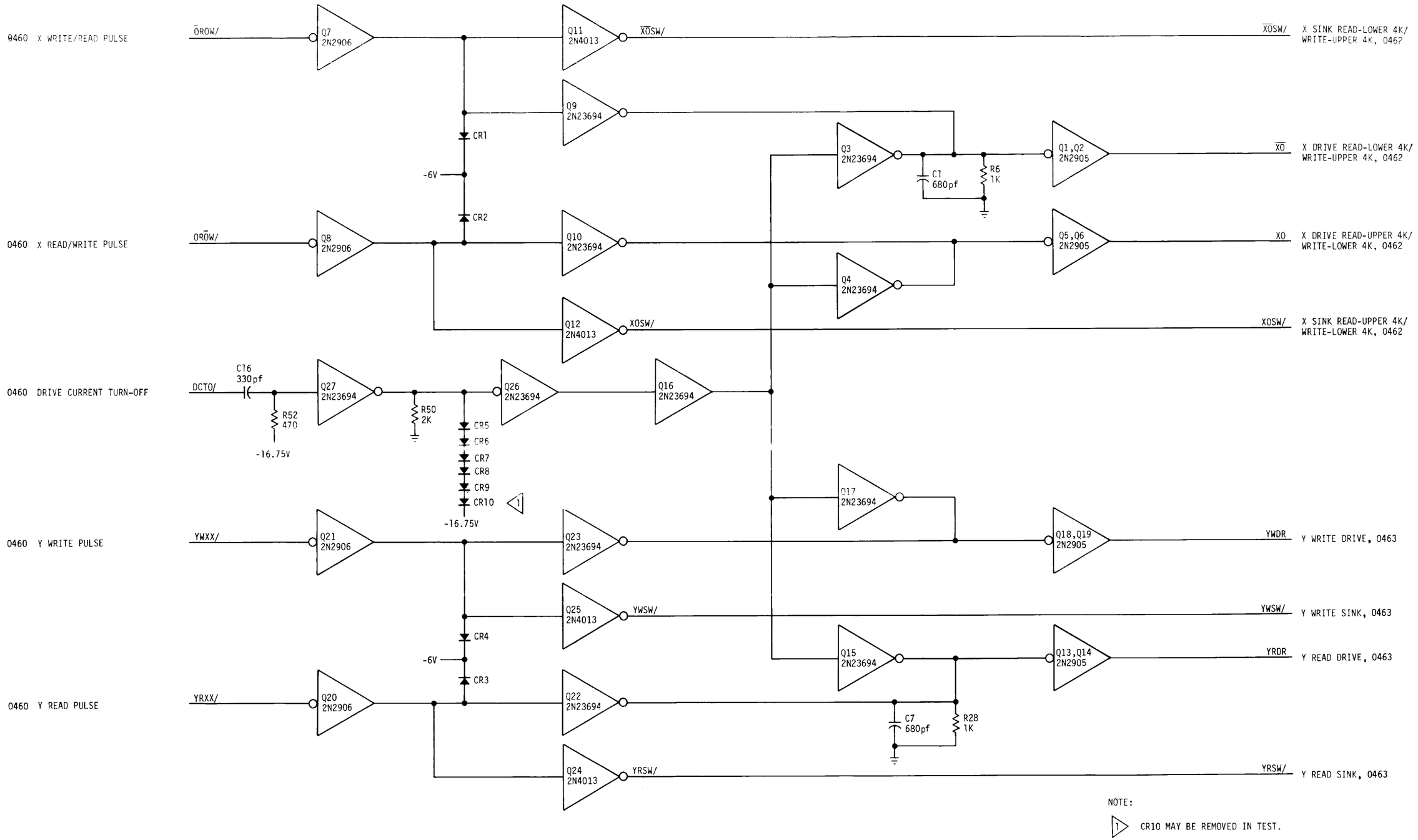
0451 READ ENABLE

READ P1-B23

MEN, READ

Z7 9002

Z3 9016 → MSAR MEMORY SELECT AND READ, 0465, 0466, 0467, 0468




MEMORY DRIVE CIRCUITS

# X SELECT BITS 0-7

0461 X DRIVE READ-UPPER 4K/ WRITE-LOWER 4K

0420 N REG BIT 0

PG iv N REG BIT 0

0420 N REG BIT 1

PG iv N REG BIT 1

0420 N REG BIT 2

PG iv N REG BIT 2

0460 ENABLE DECODER

0461 X SINK READ-LOWER 4K/ WRITE-UPPER 4K

0461 X SINK READ-UPPER 4K/ WRITE-LOWER 4K

0420 N REG BIT 5

PG iv N REG BIT 5

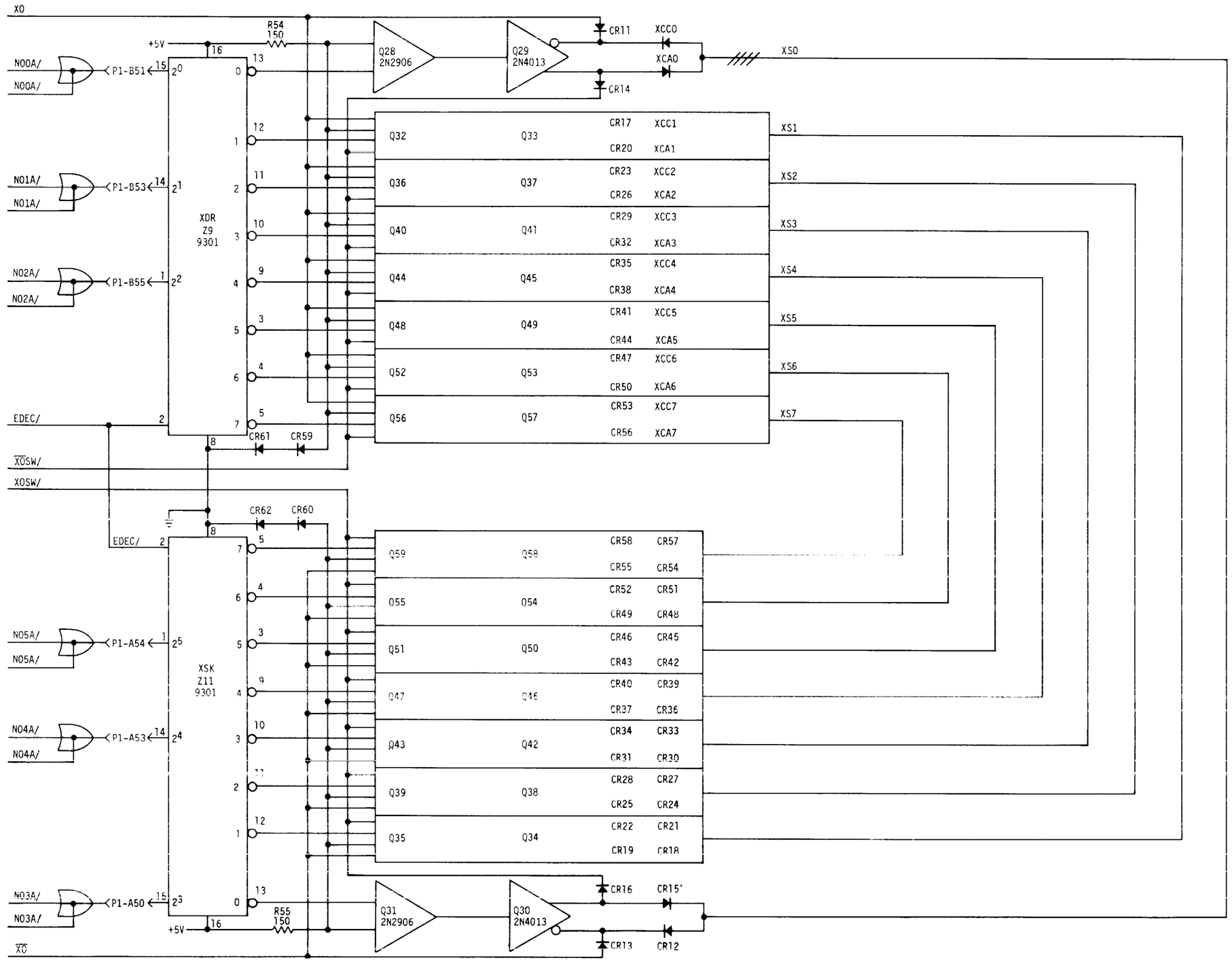
0420 N REG BIT 4

PG iv N REG BIT 4

0420 N REG BIT 3

PG iv N REG BIT 3

0461 X DRIVE READ-LOWER 4K/ WRITE-UPPER 4K



0461 Y WRITE DRIVE

0420 N REG BIT 6

PG iv N REG BIT 6

0420 N REG BIT 7

PG iv N REG BIT 7

0410 M REG BIT 0

PG iv M REG BIT 0

0460 ENABLE DECODER

0461 Y READ SINK

0461 Y WRITE SINK

0410 M REG BIT 3

PG iv M REG BIT 3

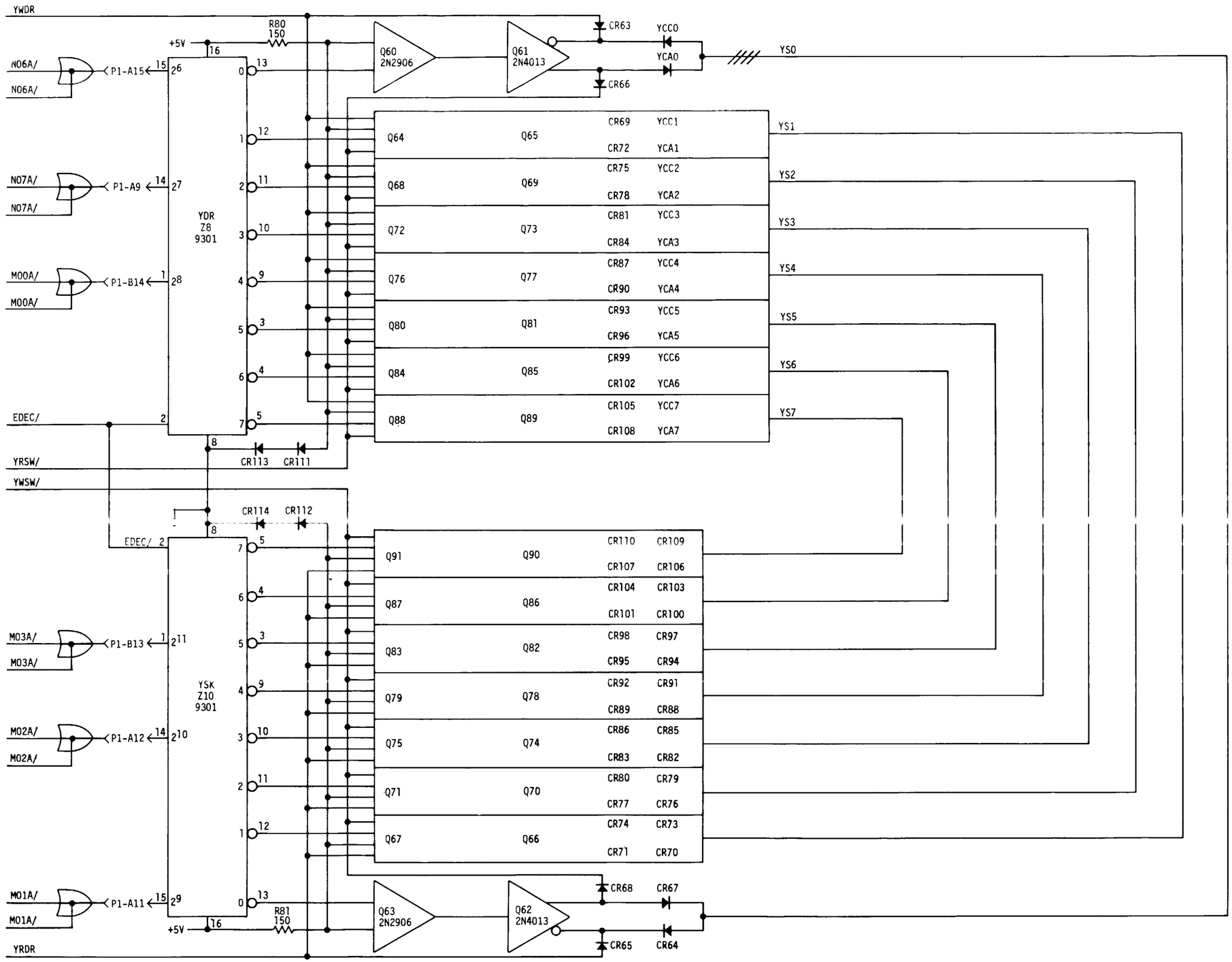
0410 M REG BIT 2

PG iv M REG BIT 2

0410 M REG BIT 1

PG iv M REG BIT 1

0461 Y READ DRIVE




Y SELECT BITS 0-7

# PRIORITY/SELECT, MEMORY CLAMP AND POWER

PRIORITY IN FROM A55 OF NEXT LOWER NUMBERED JACK (PROT/)

PRIN/ P1-B54

P1-A55 PROT/ PRIORITY OUT TO B54 OF NEXT HIGHER NUMBERED JACK (PRIN/)

SELECT IN FROM A52 OF NEXT LOWER NUMBERED JACK (SELO/)

SELI/ P1-B52

P1-A52 SELO/ SELECT OUT TO B52 OF NEXT HIGHER NUMBERED JACK (SELI/)

+5V

VTH P1-B61

R136 511

GROUND: P1-A1, P1-A2, P1-A64, P1-A65

R137 2

C31 22

C32 22

C33 22

C58 22

C56 22

+V REF

CR164 5.1V

CR165

C20 47

C34 0.01

C35 0.01

-V REF

Q110 2N2905

-5V

R133 1K

R134 1K

R135 68

-16.75V

-16.75V

C19 330 pf

C55 220 pf

R108 470

R109 470

0460 INHIBIT CURRENT TURN-OFF

ICTO

Q92,Q93 2N4013

ICTO/ INHIBIT CURRENT TURN-OFF, 0465, 0466, 0467, 0468

+5 VOLTS: P1-B1, P1-B2, P1-B64, P1-B65

C13 22 C14 22 C17 0.01 C18 0.10 C21 0.01 C22 0.01 C36 4.7 C37 4.7 C38 0.01 C39 0.01 C46 0.01 C47 0.01 C52 4.7 C53 4.7 C48 0.01 C49 0.01 C50 0.01 C51 0.01

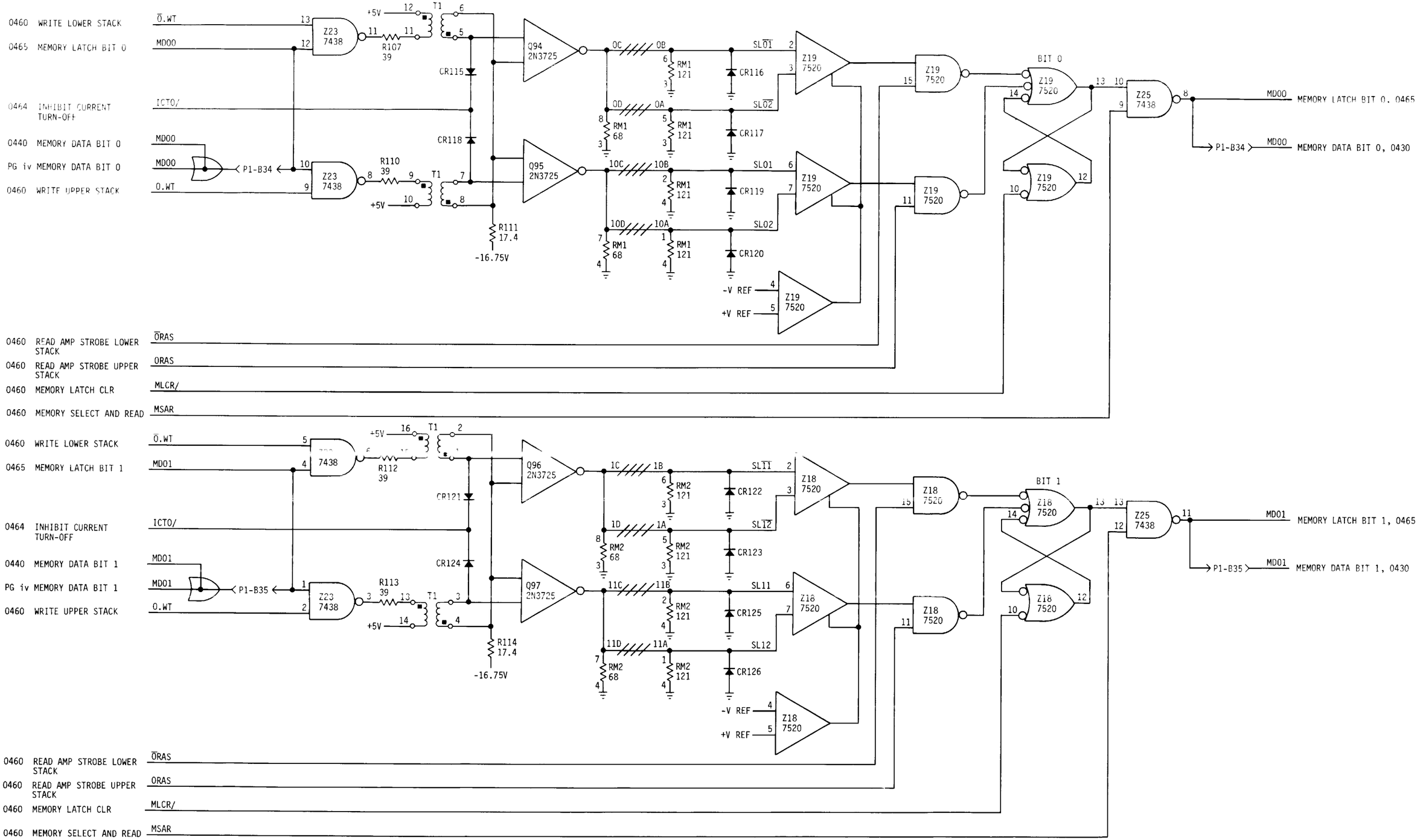
+5V

-V REF

C40 22 C41 22 C42 22 C43 22 C44 22 C45 22 C57 22 C2 22 C12 22 C54 0.01 C6 0.01 C11 0.01

-16.75V

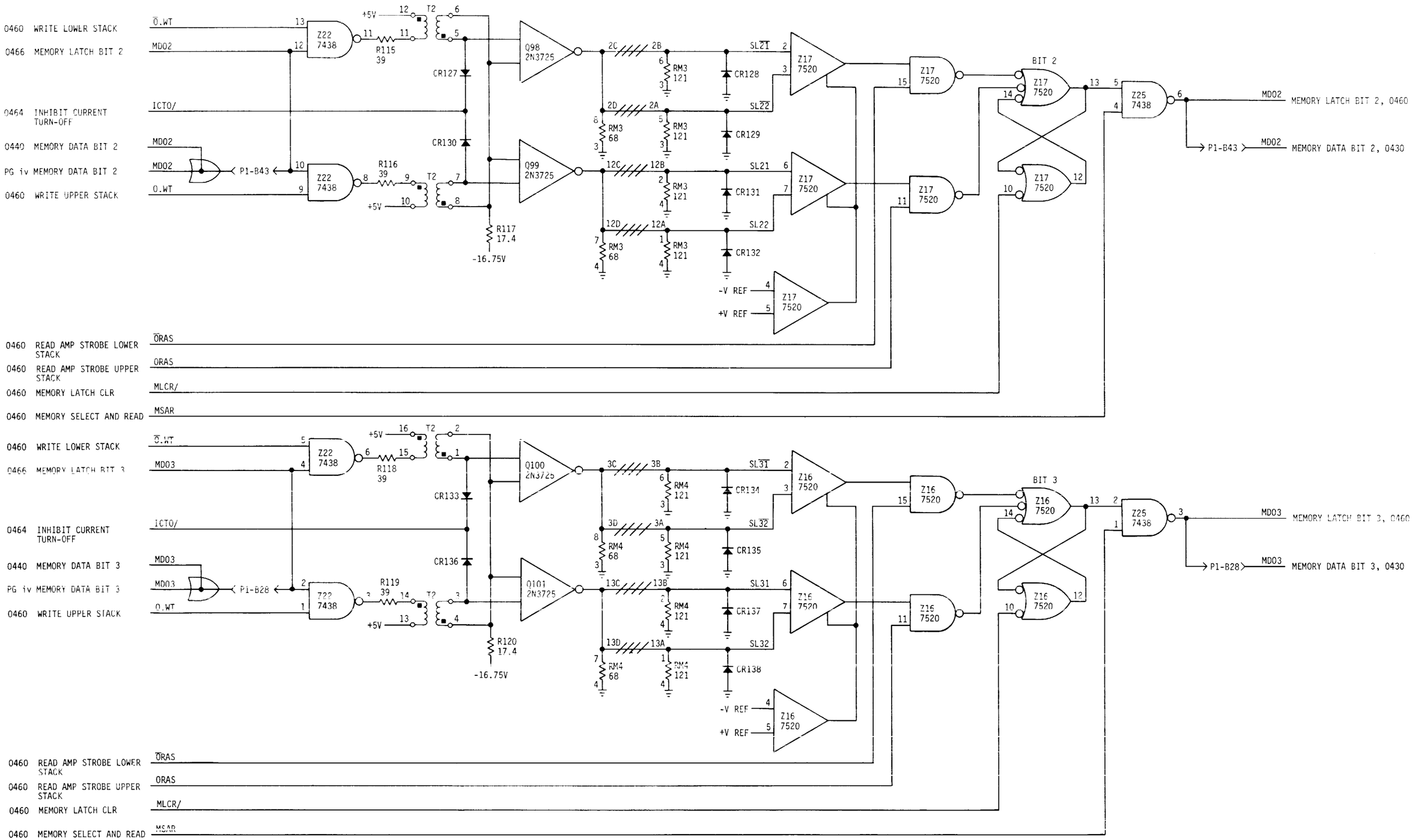
-16.75 VOLTS: P1-B3, P1-A4, P1-A63, P1-B63

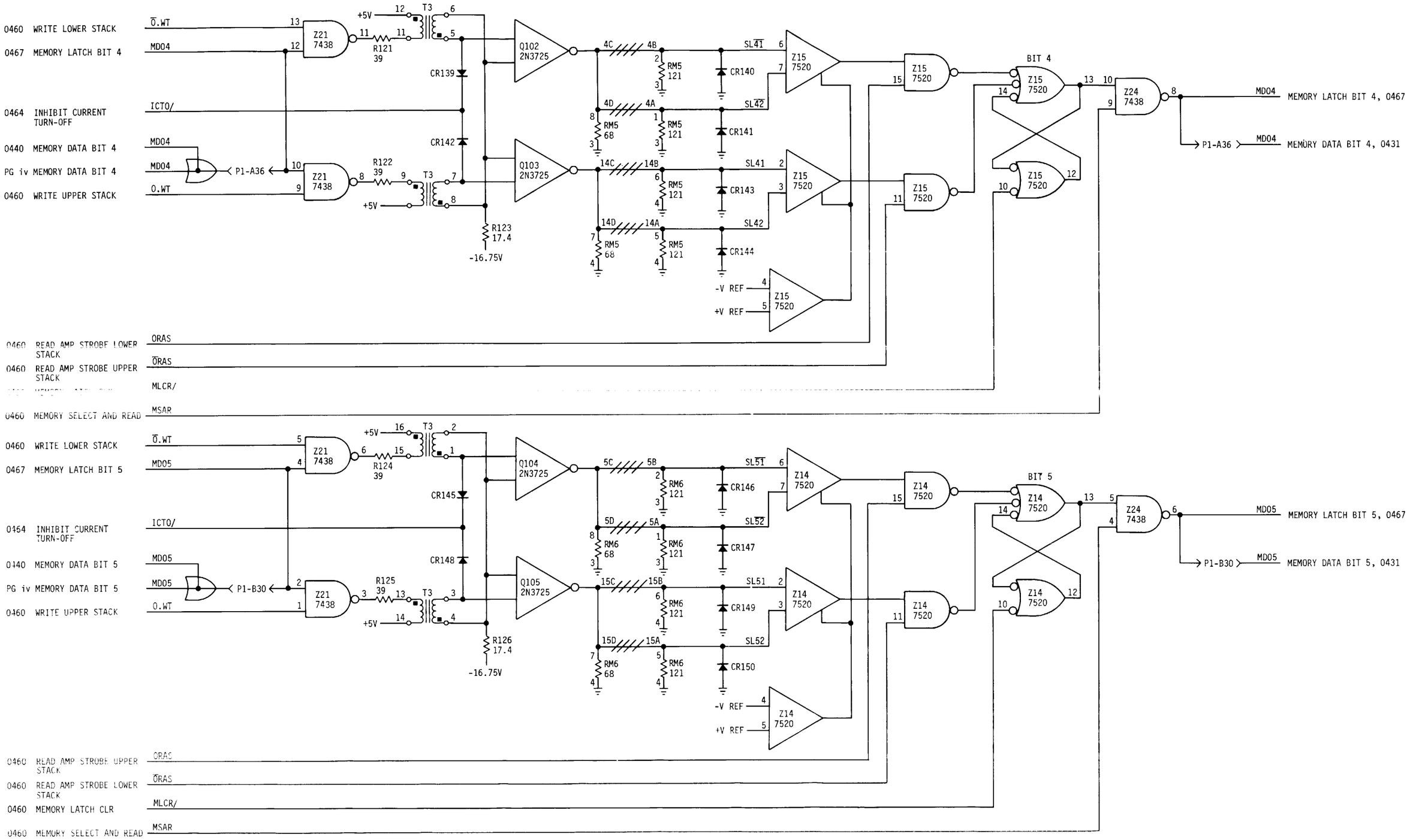



MEMORY READ/WRITE BITS 0 AND 1

CORE MEMORY
0465

# MEMORY READ/WRITE BITS 2 AND 3






MEMORY READ/WRITE BITS 4 AND 5

CORE MEMORY
0467

# MEMORY READ/WRITE BITS 6 AND 7

0460 WRITE LOWER STACK
0468 MEMORY LATCH BIT 6
0464 INHIBIT CURRENT TURN-OFF
0440 MEMORY DATA BIT 6
PG iv MEMORY DATA BIT 6
0460 WRITE UPPER STACK

$\overline{0}$.WT
MD06
ICTO/
MD06
MD06
0.WT

Z20 7438
R127 39
R128 39
+5V
T4
CR151
CR154
Q106 2N3725
Q107 2N3725
R129 17.4
-16.75V
P1-B40

6C 6B 6D 6A 16C 16B 16D 16A
RM7 121
RM7 68
CR152 CR153 CR155 CR156
SL$\overline{61}$ SL$\overline{62}$ SL61 SL62
Z13 7520
-V REF
+V REF

0460 READ AMP STROBE LOWER STACK
0460 READ AMP STROBE UPPER STACK
0460 MEMORY LATCH CLR
0460 MEMORY SELECT AND READ

$\overline{0}$RAS
0RAS
MLCR/
MSAR

BIT 6
Z24 7438
MD06 MEMORY LATCH BIT 6, 0468
P1-B40 MD06 MEMORY DATA BIT 6, 0431

0460 WRITE LOWER STACK
0468 MEMORY LATCH BIT 7
0464 INHIBIT CURRENT TURN-OFF
0440 MEMORY DATA BIT 7
PG iv MEMORY DATA BIT 7
0460 WRITE UPPER STACK

$\overline{0}$.WT
MD07
ICTO/
MD07
MD07
0.WT

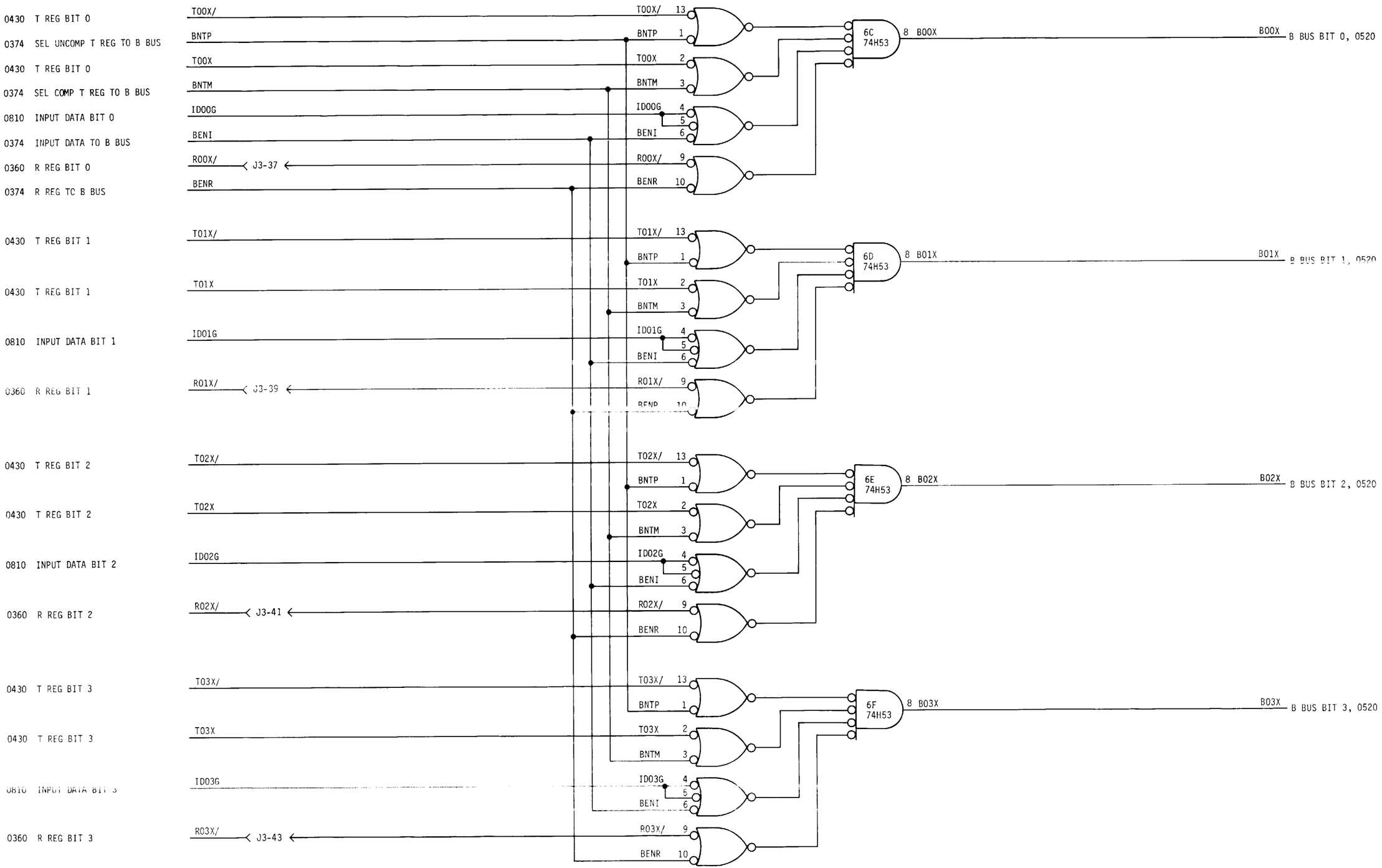
Z20 7438
R130 39
R131 39
+5V
T4
CR157
CR160
Q108 2N3725
Q109 2N3725
R132 17.4
-16.75V
P1-B27

7C 7B 7D 7A 17C 17B 17D 17A
RM8 121
RM8 68
CR158 CR159 CR161 CR162
SL$\overline{71}$ SL$\overline{72}$ SL71 SL72
Z12 7520
-V REF
+V REF

0460 READ AMP STROBE UPPER STACK
0460 READ AMP STROBE LOWER STACK
0460 MEMORY LATCH CLR
0460 MEMORY SELECT AND READ

0RAS
$\overline{0}$RAS
MLCR/
MSAR

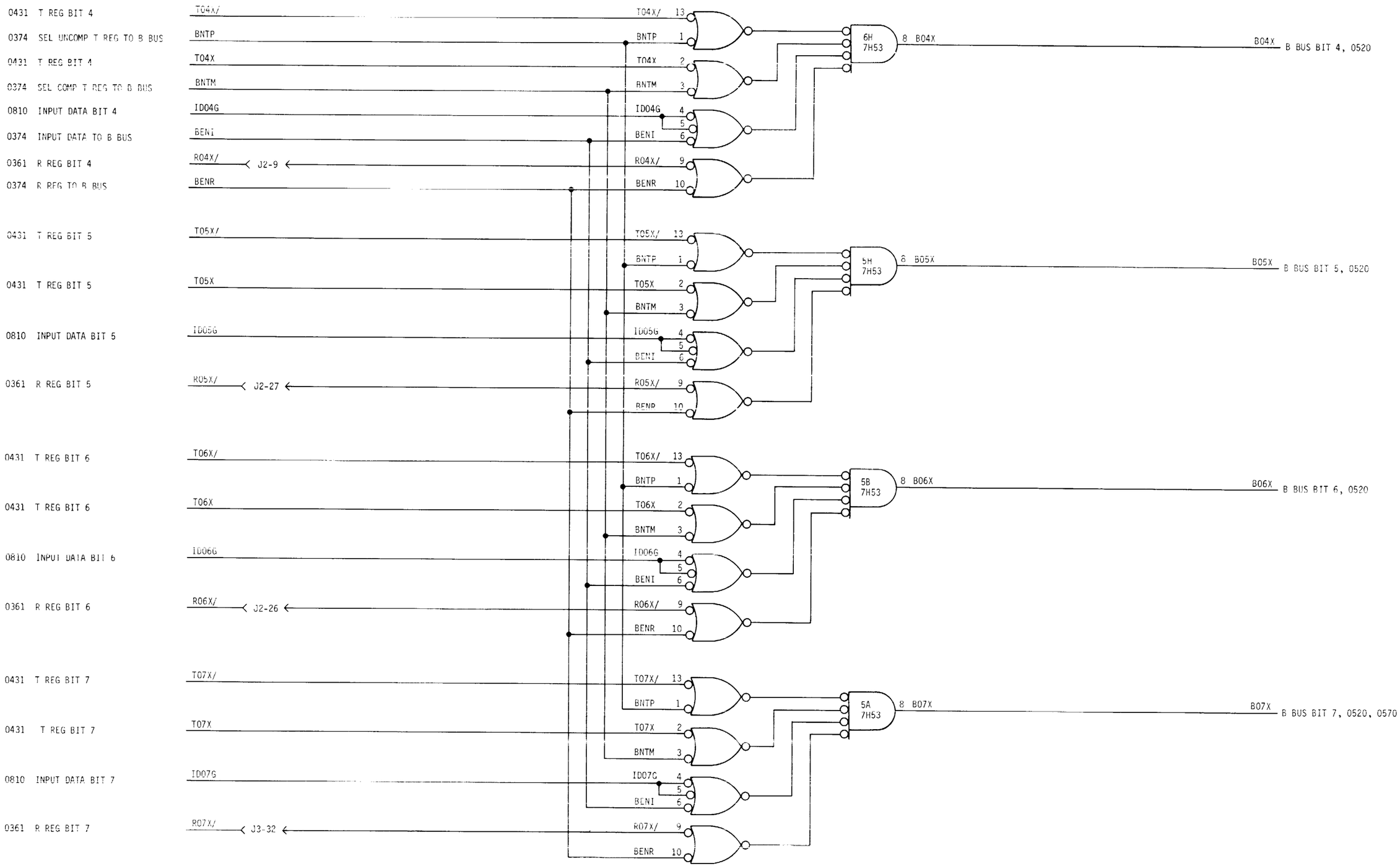
BIT 7
Z24 7438
MD07 MEMORY LATCH BIT 7, 0468
P1-B27 MD07 MEMORY DATA BIT 7, 0431




B BUS MULTIPLEXER BITS 0-3

J3 DATA BOARD
0510

# B BUS MULTIPLEXER BITS 4-7



0560 INITIAL CARRY

0550 FILE BIT 0

0510 B BUS BIT 0

0550 FILE BIT 1

0510 B BUS BIT 1

0550 FILE BIT 2

0510 B BUS BIT 2

0550 FILE BIT 3

0510 B BUS BIT 3

0550 FILE BIT 4

0511 B BUS BIT 4

0550 FILE BIT 5

0511 B BUS BIT 5

0550 FILE BIT 6

0511 B BUS BIT 6

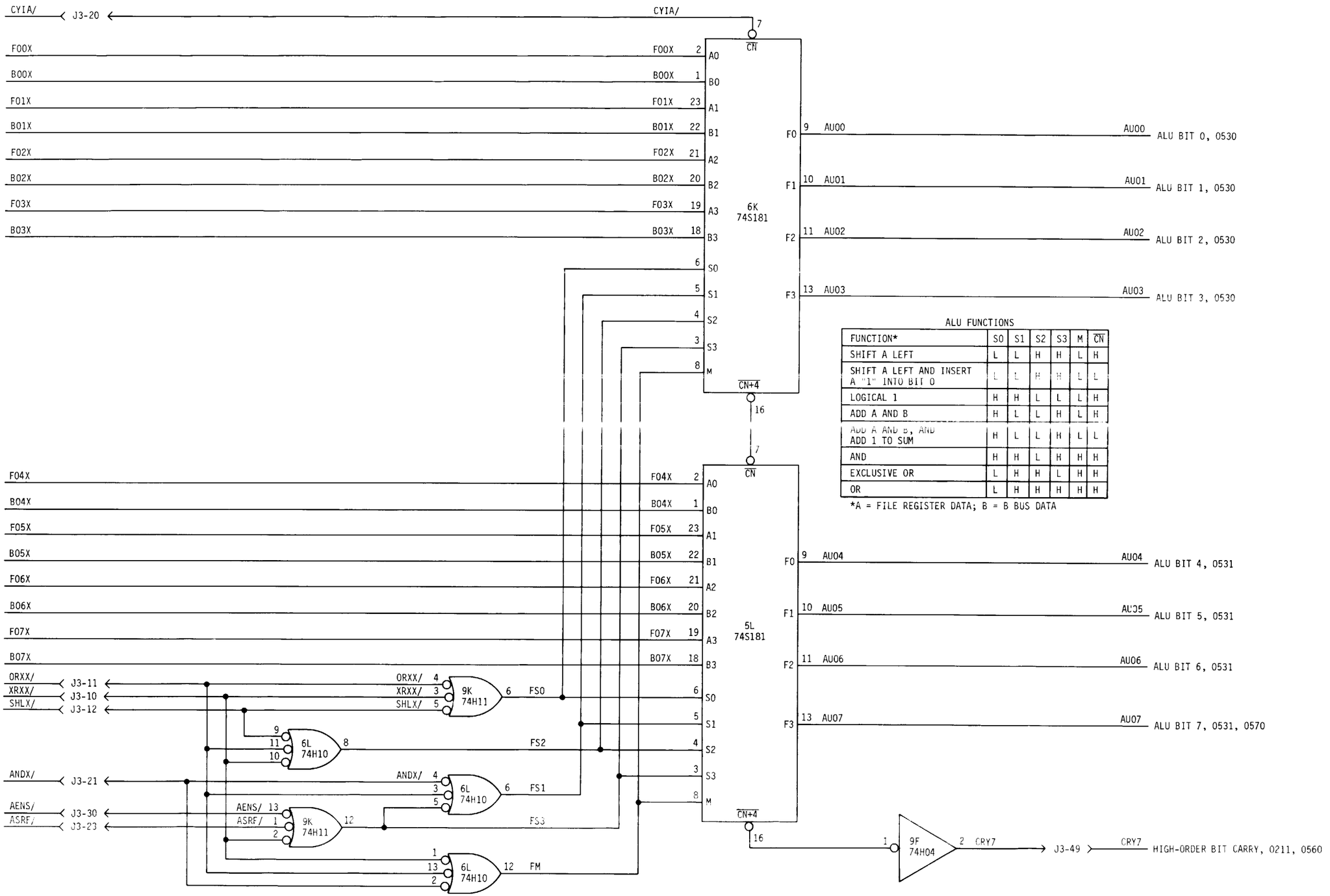
0550 FILE BIT 7

0511 B BUS BIT 7

0370 OR COMMAND
0370 EXCLUSIVE OR COMMAND
0372 SHIFT LEFT

0372 LOGICAL AND

0373 ENTER SENSE SWITCHES
0373 SHIFT FILE RIGHT 4




ALU FUNCTIONS

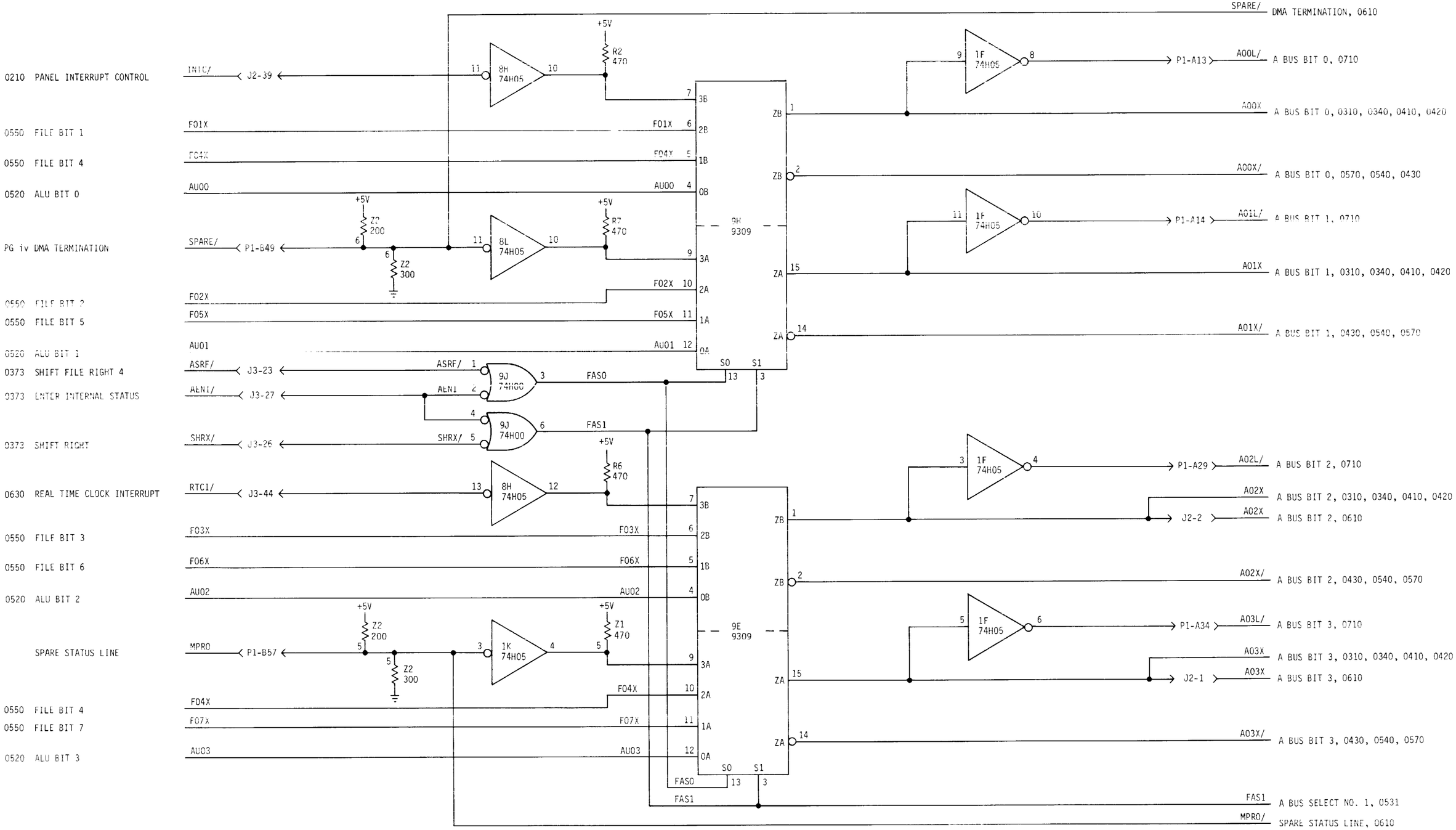
| FUNCTION* | S0 | S1 | S2 | S3 | M | $\overline{CN}$ |
|---|---|---|---|---|---|---|
| SHIFT A LEFT | L | L | H | H | L | H |
| SHIFT A LEFT AND INSERT A "1" INTO BIT 0 | L | L | H | H | L | L |
| LOGICAL 1 | H | H | L | L | L | H |
| ADD A AND B | H | L | L | H | L | H |
| ADD A AND B, AND ADD 1 TO SUM | H | L | L | H | L | L |
| AND | H | H | L | H | H | H |
| EXCLUSIVE OR | L | H | H | L | H | H |
| OR | L | H | H | H | H | H |

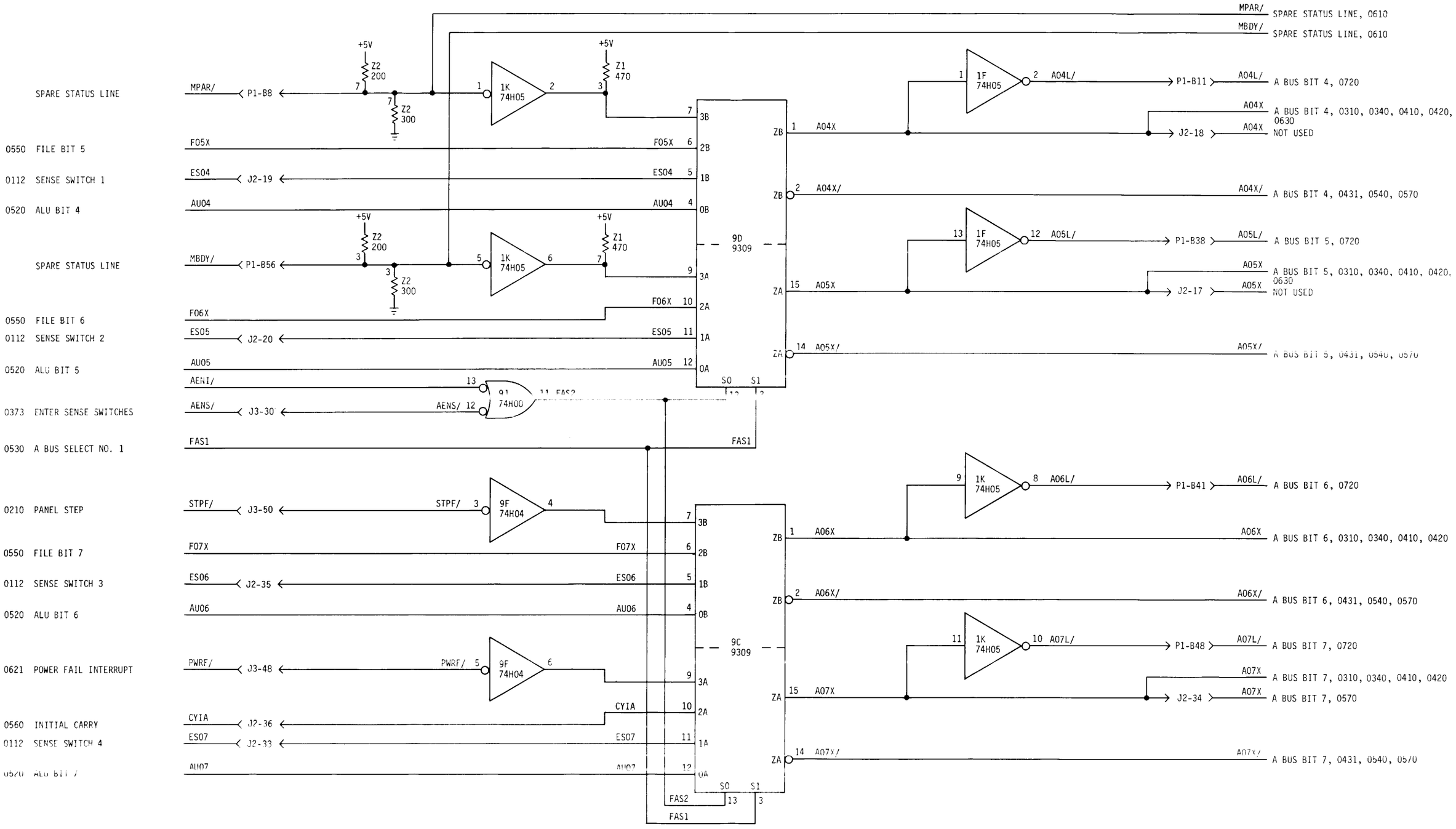
*A = FILE REGISTER DATA; B = B BUS DATA

ARITHMETIC/LOGIC UNIT

J3 DATA BOARD
0520

# A BUS MULTIPLEXER BITS 0-3






A BUS MULTIPLEXER BITS 4-7

J3 DATA BOARD
0531

# FILE REGISTERS AND FILE ZERO FLAGS

0550 SELECT SECONDARY FILE
0362 R REG BIT 8-11
0530 A BUS BIT 0-3
0531 A BUS BIT 4-7

0550 SELECT PRIMARY FILE
0230 FILE WRITE CLOCK

0570 OVERFLOW CONDITION

0570 NEGATIVE CONDITION

0570 ZERO CONDITION

PG iv CONCURRENT I/O REQUEST

0610 INTERNAL STATUS INTERRUPT

SPARE STATUS LINE

NOT USED

0610 EXT INTERRUPT REQUEST

0550 SELECT FILE ZERO

J3 DATA BOARD

FBS2/

R08X-R11X

A00X/-A03X/

A04X/-A07X/

FBS1/

CLK2/ ← J3-22

CC0X/ ← J2-3

CC1X/ ← J3-31

CC2X/ ← J2-4

ECIO/ ← P1 B42

INTL/

IRPY/ ← P1-B50

TTIN/
OR
STOV/ ← P1-B46 ↔ J3-46 ← J3-46

INTR/ ← J3-47

FAZO

+5V

Z11 200

Z11 300

J2
CONTROL BOARD

FILE ZERO FLAGS

8E 7438 — CC0X/ → F00Z
8E 7438 — CC1X/ → F01Z
8E 7438 — CC2X/ → F02Z
8E 7438 → F03Z
8F 7438 → F04Z
8F 7438 → F05Z
8F 7438 → F06Z
8F 7438 → F07Z

PRIMARY FILE

7K P3101A: R08X, R09X, R10X, R11X, A00X/, A01X/, A02X/, A03X/, FBS1/, CLK2/ → F00P, F01P, F02P, F03P

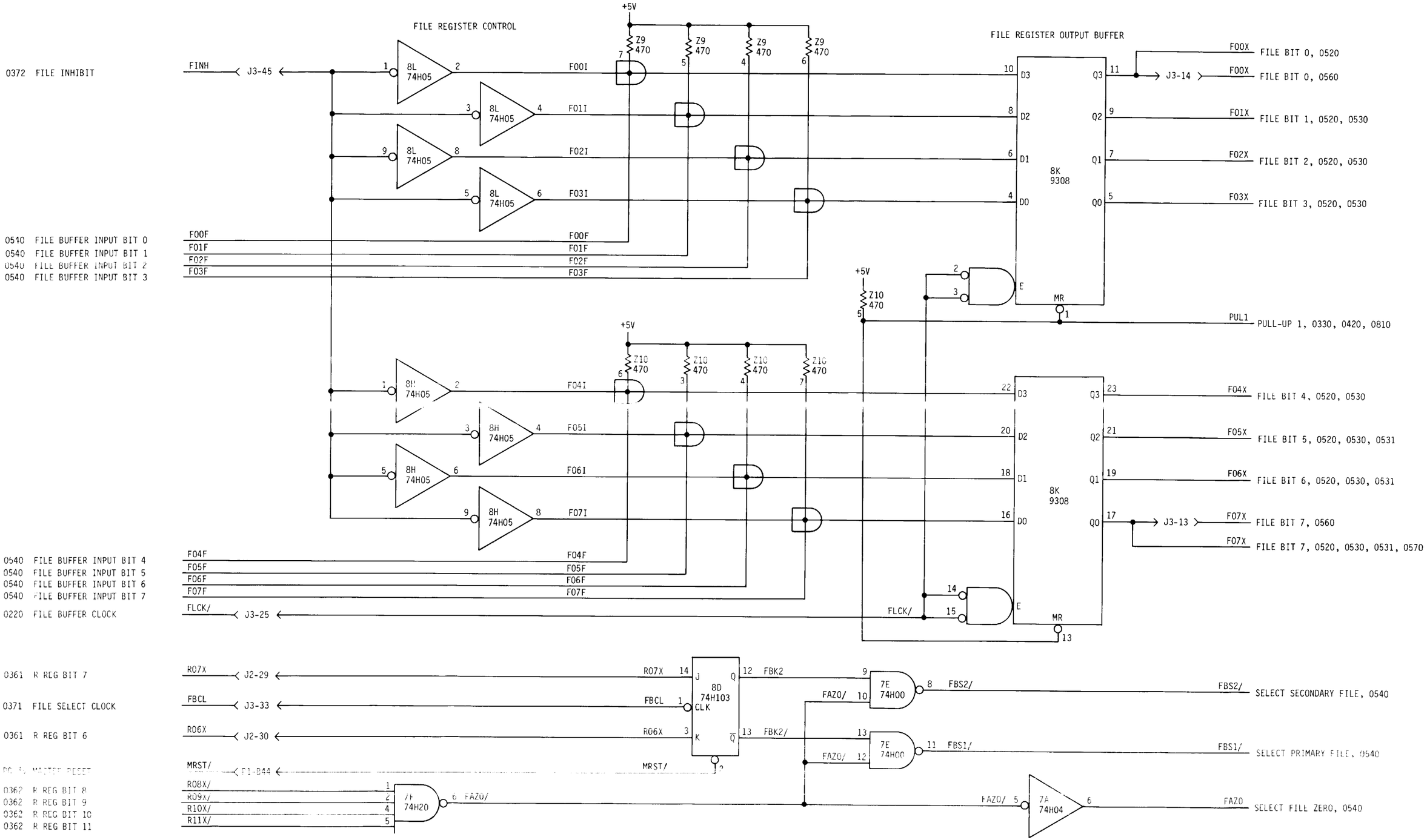
7J P3101A: R08X, R09X, R10X, R11X, A04X/, A05X/, A06X/, A07X/, FBS1/, CLK2/ → F04P, F05P, F06P, F07P

SECONDARY FILE

7L P3101A: R08X, R09X, R10X, R11X, A00X/, A01X/, A02X/, A03X/, FBS2/, CLK2/ → F00S, F01S, F02S, F03S

7H P3101A: R08X, R09X, R10X, R11X, A04X/, A05X/, A06X/, A07X/, FBS2/, CLK2/ → F04S, F05S, F06S, F07S

F00F FILE BUFFER INPUT BIT 0, 0550
F01F FILE BUFFER INPUT BIT 1, 0550
F02F FILE BUFFER INPUT BIT 2, 0550
F03F FILE BUFFER INPUT BIT 3, 0550
F04F FILE BUFFER INPUT BIT 4, 0550
F05F FILE BUFFER INPUT BIT 5, 0550
F06F FILE BUFFER INPUT BIT 6, 0550
F07F FILE BUFFER INPUT BIT 7, 0550




FILE REGISTER CONTROL AND FILE REGISTER OUTPUT BUFFER

# LINK REGISTER AND INITIAL CARRY LOGIC

0550 FILE BIT 7
0372 SHIFT LEFT
0550 FILE BIT 0
0373 SHIFT RIGHT
0370 SHIFT FILE
0520 HIGH-ORDER BIT CARRY
0370 SHIFT FILE

0370 ADD COMMAND
0370 COMPARE FILE
0370 SUBTRACT COMMAND
0372 M OR N REG SELECT

0230 DATA CLOCK

0570 CLAMP
0372 M OR N REG SELECT

0370 SUBTRACT COMMAND
0361 R REG BIT 6
0361 R REG BIT 7

0370 MEMORY READ OR WRITE
0361 R REG BIT 6

0370 MEMORY READ OR WRITE
0361 R REG BIT 7

0363 R REG BIT 15
0560 SEL LINK BIT

0374 CODE 01 IN C FIELD BITS 7 AND 6

0360 R REG BIT 0
0360 R REG BIT 1
0360 R REG BIT 2

LINK REGISTER

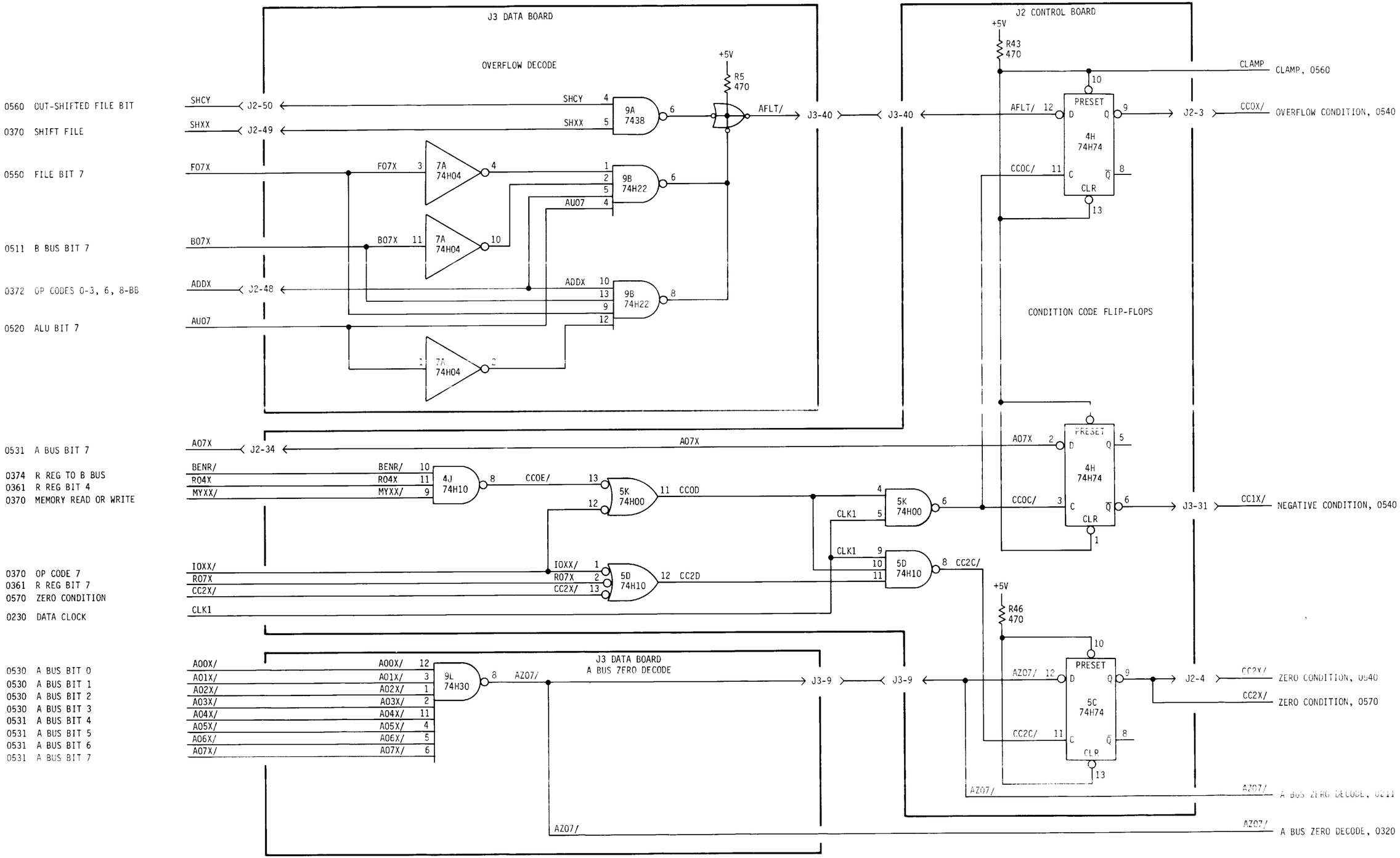
FO7X ← J3-13
SHLX
FOOX ← J3-14
SHRX
SHXX
CRY7 ← J3-49
SHXX/
ADXX/
CPXX/
SBYY/
MNRX/
CLK1
CLAMP
MNRX
SBXX
RO6X/
RO7X/
MYXX/
RO6X
MYXX
RO7X
R15X
LINK
MYDX
RO0X/
RO1X
RO2X/

5L 74H51
6L 74H04
SHCY → J2-50 → SHCY — OUT-SHIFTED FILE BIT, 0570
5L 74H51
6J 74H20
SACS
4J 74H10
ARITH LINK
4K 74H74 (PRESET, D, Q, CLR)
ARTL/ → P1-B62 — ARTL/ — NOT USED
+5V
R42 220
4F 7438
7H 74H04
LINK → SEL LINK BIT, 0560
P1-B61 — LINK/ — NOT USED
P1-B60 — MALK/ — NOT USED
P1-A60 — MNRX/ — NOT USED
P1-A61 — EALC — NOT USED
P1-A62 — SACS — NOT USED
MEMORY LINK
4K 74H74 (PRESET, D, Q, CLR)
4J 74H10
ARTC/
4F 7438
7K 74H22
7L 74H22
7L 74H22
7K 74H22
7J 74H22
6H 74H11

INITIAL CARRY LOGIC

+5V
R54 470
CYIA/ 13
8L 74H04
CYIA → J2-36 — CYIA — INITIAL CARRY, 0531
J3-20 — CYIA/ — INITIAL CARRY, 0520

NOTE:
1. JUMPER CONNECTIONS FOR SEPARATE MEMORY AND ARITHMETIC LINK IS SHOWN. FOR COMBINED MEMORY AND ARITHMETIC LINK, PAD 1 IS JUMPERED TO PAD 2, AND PAD 5 IS JUMPERED TO PAD 6, AND JUMPERS BETWEEN PADS 2 and 3, AND BETWEEN PADS 4 AND 6 ARE REMOVED. WHEN EXTERNAL MEMORY/ARITHMETIC LINK SWITCH IS INCLUDED JUMPERS BETWEEN PADS 2 AND 3 AND BETWEEN PADS 4 AND 6 ARE REMOVED.




OVERFLOW DECODE, A BUS ZERO DECODE AND CONDITION CODE FLIP-FLOPS

J2 CONTROL BOARD
AND J3 DATA BOARD
0570

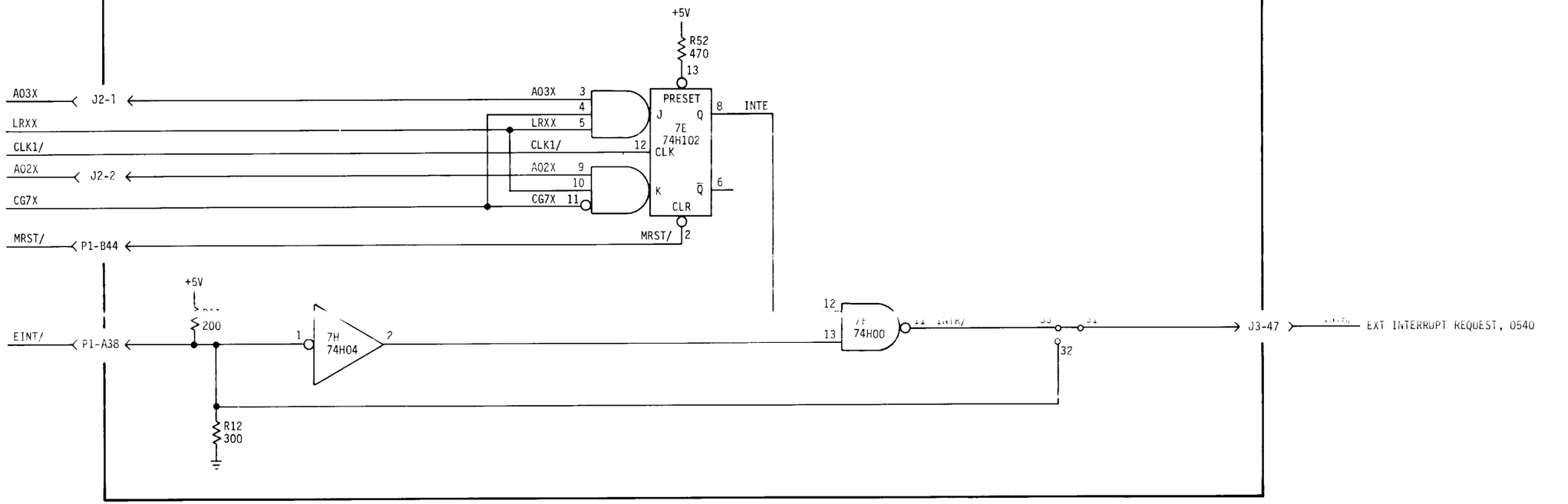
J2 CONTROL BOARD

EXTERNAL INTERRUPT CONTROL

0530 A BUS BIT 3
0370 LOAD LITERAL
0230 DATA CLOCK
0530 A BUS BIT 2
0371 LOAD SEVEN

PG iv MASTER RESET

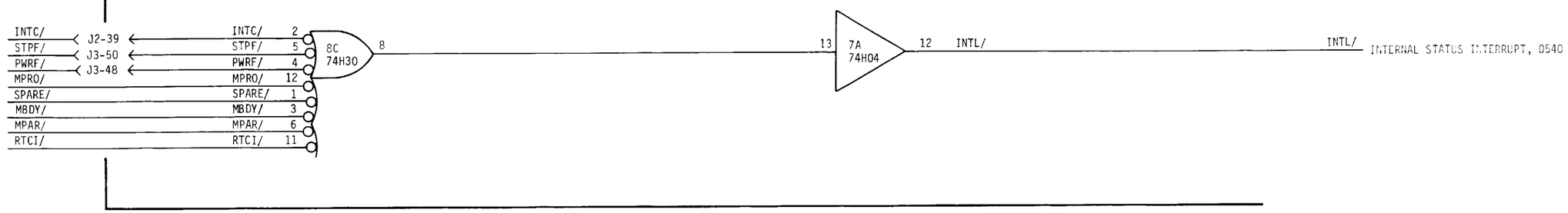
PG iv EXTERNAL INTERRUPT




J3 DATA BOARD

INTERNAL STATUS INTERRUPT CONTROL

0210 PANEL INTERRUPT CONTROL
0210 PANEL STEP
0621 POWER FAIL INTERRUPT
0530 SPARE STATUS LINE
0530 DMA TERMINATION
0531 SPARE STATUS LINE
0531 SPARE STATUS LINE
0630 REAL TIME CLOCK INTERRUPT




INTERNAL AND EXTERNAL INTERRUPTS

J2 CONTROL BOARD
AND J3 DATA BOARD
0610

# POWER FAIL 1

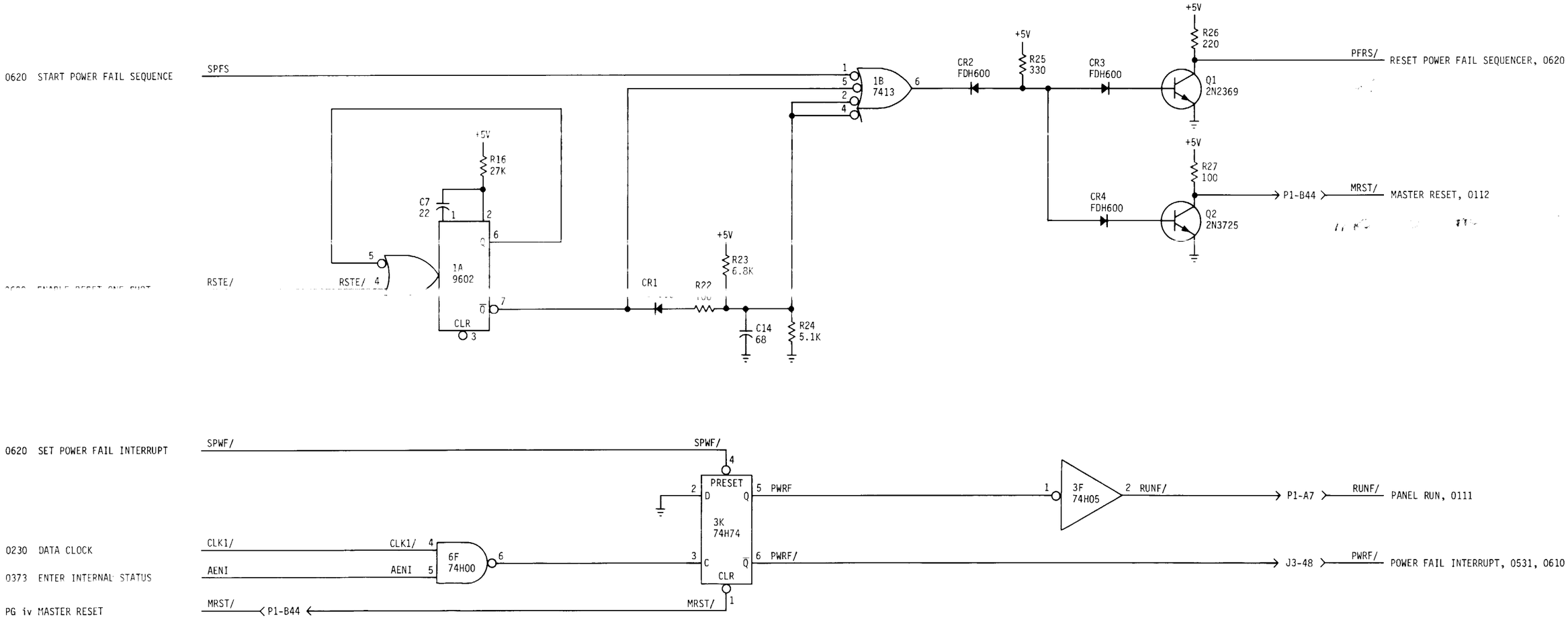
0620 POWER FAIL STATE 0
0621 RESET POWER FAIL SEQUENCER
0220 5-MHZ CLOCK PHASE 1
0620 POWER FAIL STATE 2
0620 POWER FAIL STATE 1
0620 POWER FAIL STATE 3
2010 POWER FAILURE DETECT
0211 RUN STATE
0211 RUN STATE
0620 POWER FAIL STATE 4
0620 POWER FAIL STATE 0

PFS0
PFRS/
SCK6
PFS2
PFS1
PFS3
PWRD/ P1-A3
RUNX/
RUNX
PFS4
PFS0

3A 74164 (A, B, CLK, CLR, QA–QH)
4D 74H00
1C 74H04
2A 74H05
R21 470
2B 7438
R15 47K
C6 0.025
1A 9602
R1 100
1B 9602
C9 1.5
C8 0.1
1C 74H04
1D 7438
4D 74H00

PFS1 POWER FAIL STATE 1, 0620
PFS2 POWER FAIL STATE 2, 0620
PFS3 POWER FAIL STATE 3, 0620
PFS4 POWER FAIL STATE 4, 0620
PFS0 POWER FAIL STATE 0, 0620
SPWF/ SET POWER FAIL INTERRUPT, 0621
RSTE/ ENABLE RESET ONE-SHOT, 0621
SPFS START POWER FAIL SEQUENCE, 0621

R38 470
R37 470
R17 470


0620 START POWER FAIL SEQUENCE
SPFS
1B
7413
CR2
FDH600
+5V
R25
330
CR3
FDH600
+5V
R26
220
PFRS/
RESET POWER FAIL SEQUENCER, 0620
Q1
2N2369
+5V
R27
100
CR4
FDH600
P1-B44
MRST/
MASTER RESET, 0112
Q2
2N3725
+5V
R16
27K
C7
22
1A
9602
RSTE/
RSTE/
CLR
CR1
+5V
R23
6.8K
C14
68
R24
5.1K
0620 SET POWER FAIL INTERRUPT
SPWF/
SPWF/
PRESET
D
Q
3K
74H74
CLR
PWRF
3F
74H05
RUNF/
P1-A7
RUNF/
PANEL RUN, 0111
0230 DATA CLOCK
0373 ENTER INTERNAL STATUS
CLK1/
AENI
6F
74H00
PWRF/
J3-48
PWRF/
POWER FAIL INTERRUPT, 0531, 0610
PG iv MASTER RESET
MRST/
P1-B44
MRST/

# REAL TIME CLOCK

PG iv MASTER RESET

0373 ENTER INTERNAL STATUS

0211 CLOCK STOP

0630 LOAD RTC

0630 RESET INTERRUPT

0230 5-MHZ CLOCK PHASE 2

PG iv MASTER RESET

0531 A BUS BIT 5

0371 LOAD SEVEN

0370 LOAD LITERAL

0230 DATA CLOCK

0531 A BUS BIT 4

PG iv MASTER RESET

MRST/ ← P1-B44

AENI

CSTP/

RTCW/

RTCK/

2J 74H11

6A 9022 — PRESET, CLR

RTC1/ → J3-44 → RTCI/ REAL TIME CLOCK INTERRUPT, 0530, 0610

R50 470

+5V

Z2 1K

6A 9022

RTCC

CLK6/

MRST/ ← P1-B44

6C 74161 — LD, CLK, CET, CEP, A, B, C, D, CLR, QA, QB, QC, QD, CARRY

Z1 1K

6D 74161

RTC1

Z3 1K

6E 74161

RTC2

NOTE:
JUMPER CONNECTIONS SHOWN ARE FOR A REAL TIME CLOCK INTERRUPT RATE OF 1 KHz

Z2 1K

A05X ← J2 17

CG7X

LRXX

CLK1/

7D 74H102 — PRESET, CLR

A04X ← J2-18

MRSI/ ← P1-B44

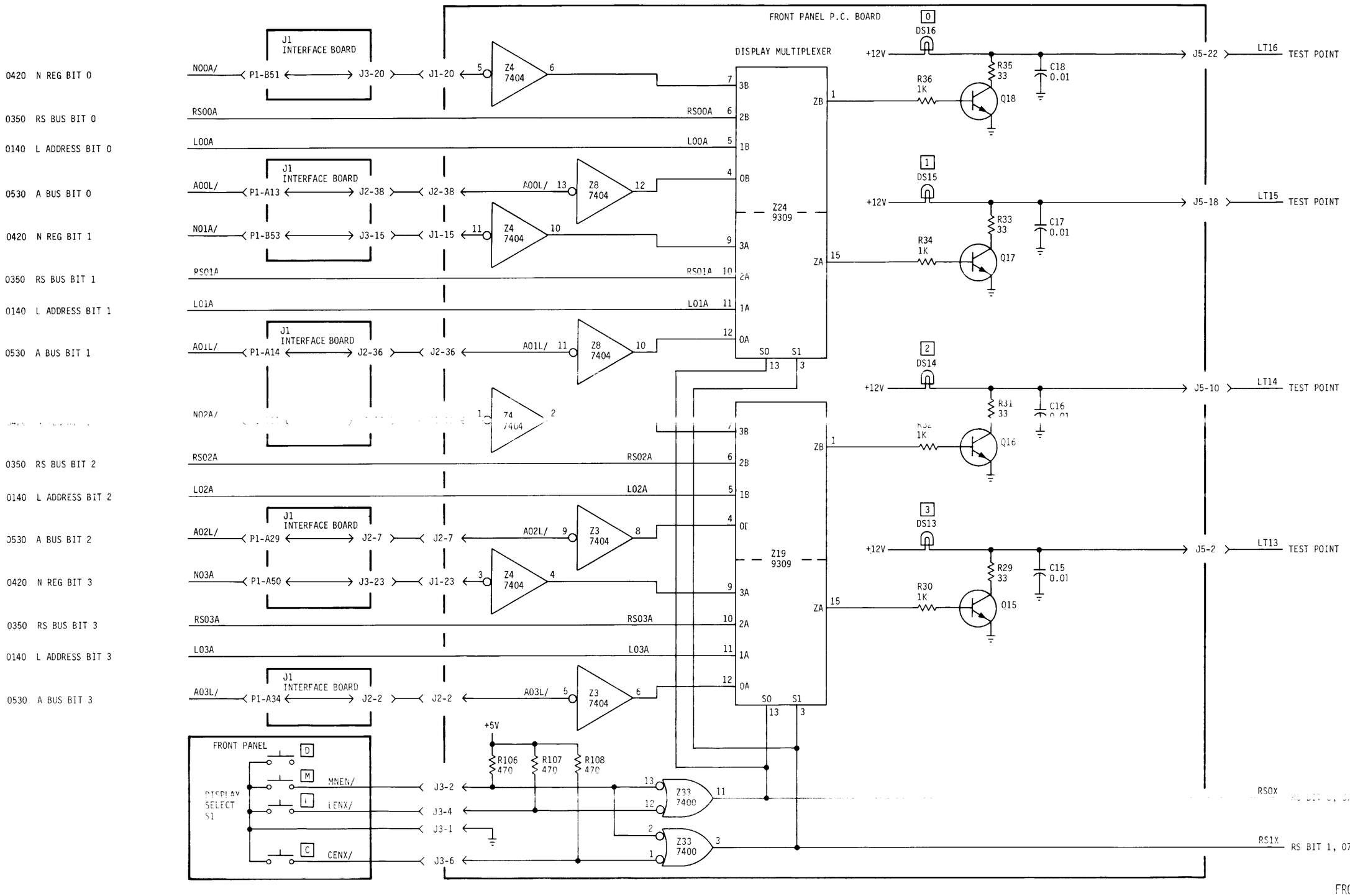
RTC3

5H 74H04

6F 74H00

RTCW/ LOAD RTC, 0630

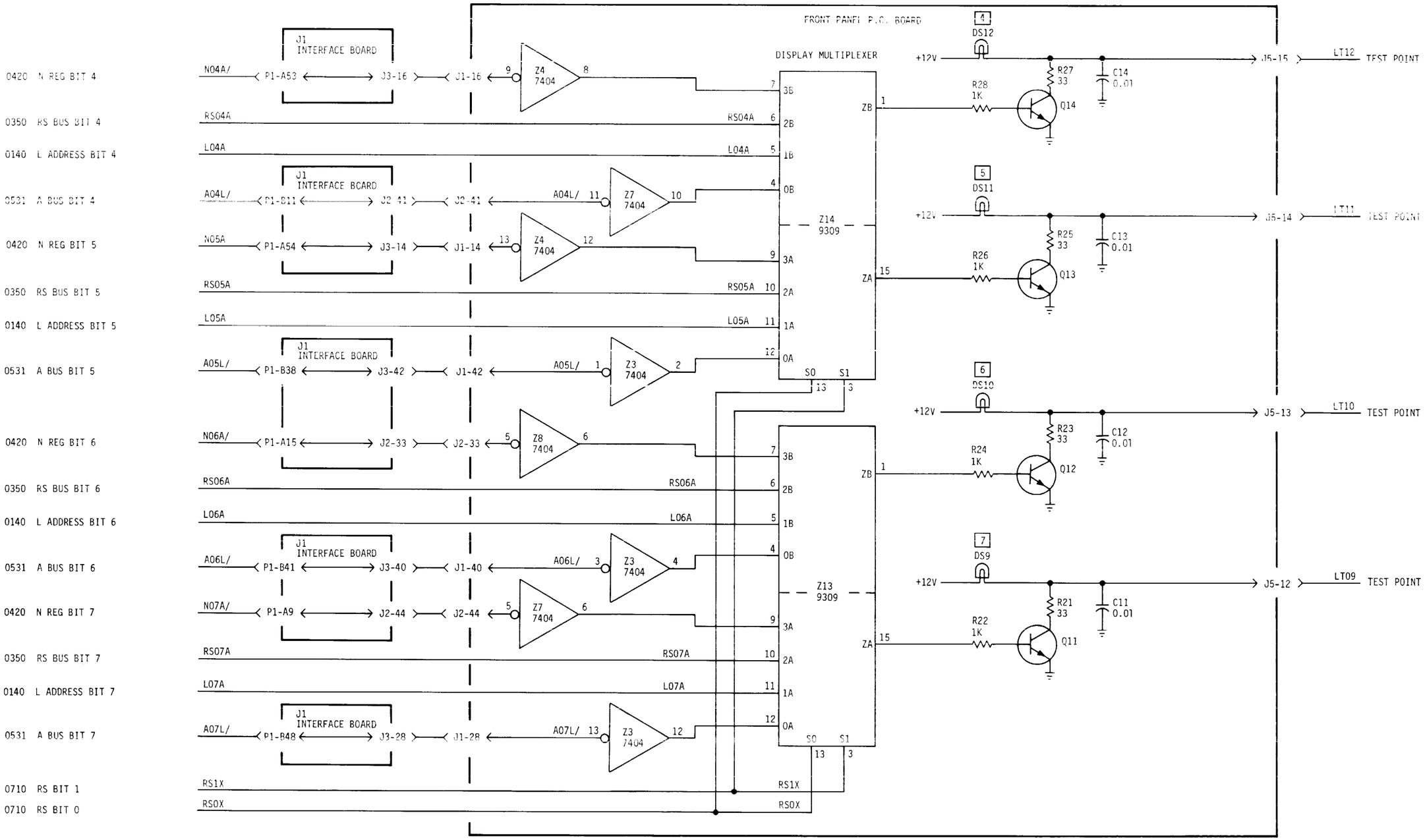
RTCK/ RESET INTERRUPT, 0630

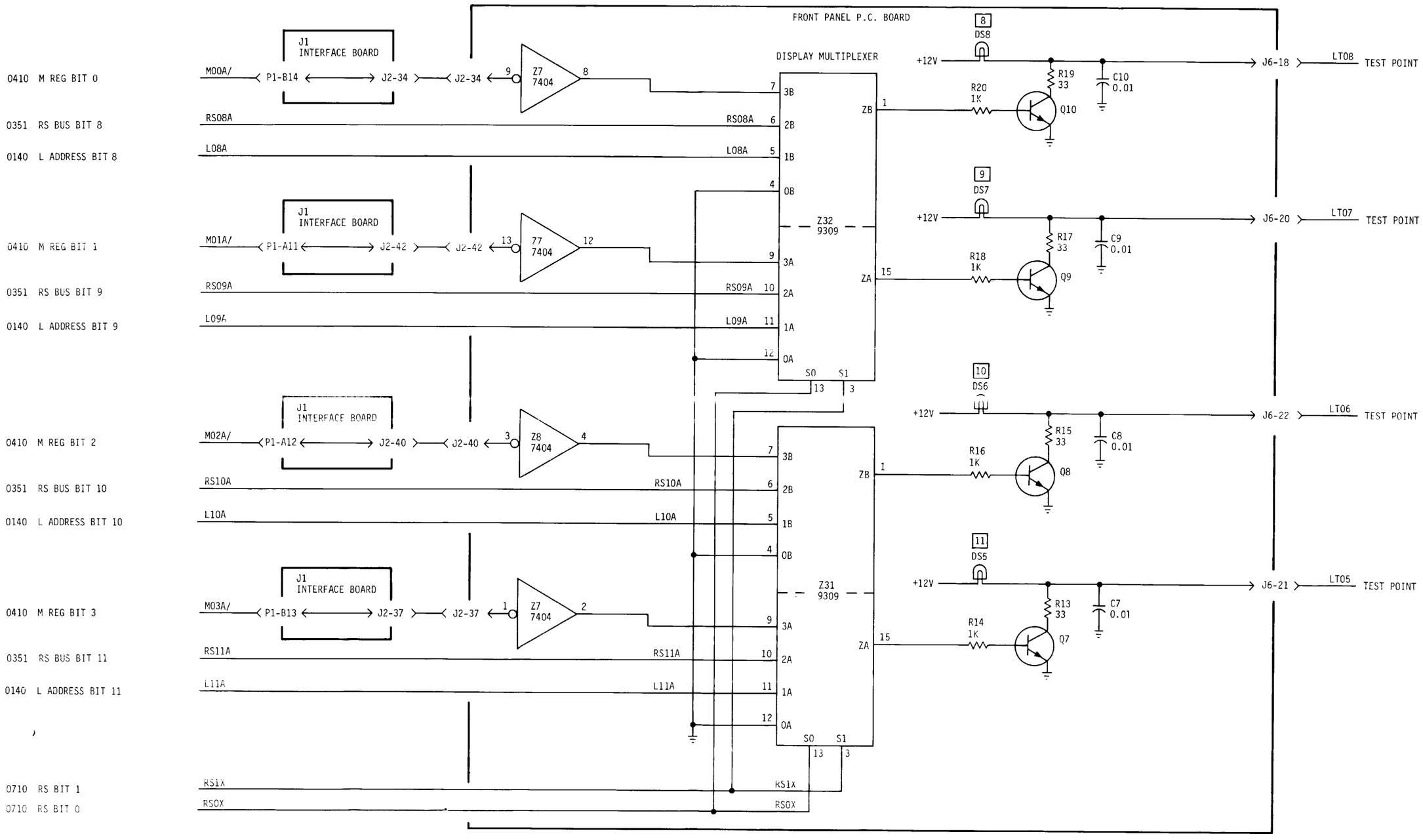



FRONT PANEL DISPLAY INDICATORS BITS 0-3

FRONT PANEL P.C. BOARD
AND J1 INTERFACE BOARD
0710

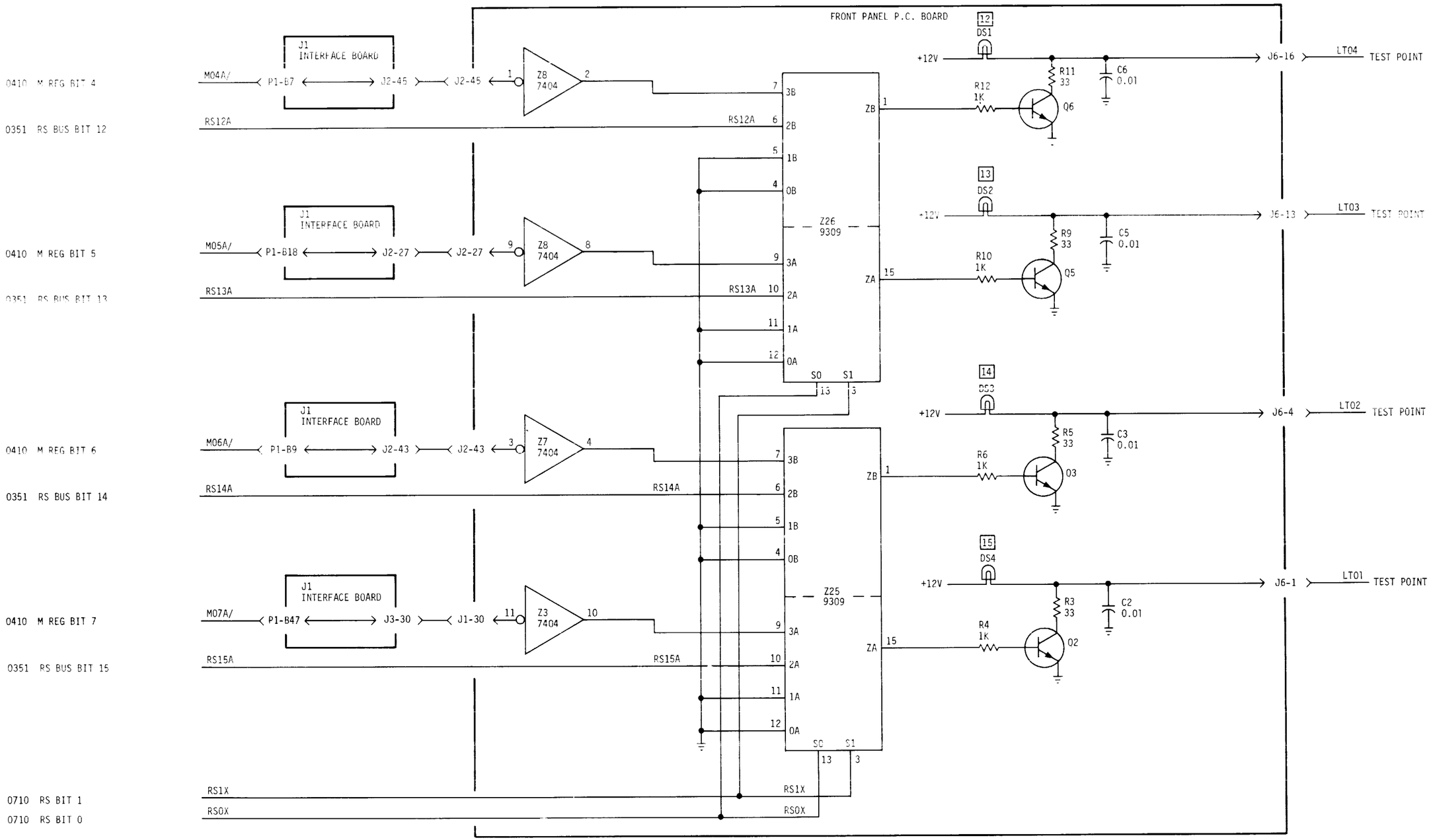
# FRONT PANEL DISPLAY INDICATORS BITS 4-7






FRONT PANEL DISPLAY INDICATORS BITS 8-11

# FRONT PANEL DISPLAY INDICATORS BITS 12-15



PG iv INPUT DATA BIT 0

PG iv INPUT DATA BIT 1

PG iv INPUT DATA BIT 2

PG iv INPUT DATA BIT 3

PG iv INPUT DATA BIT 4

PG iv INPUT DATA BIT 5

PG iv INPUT DATA BIT 6

PG iv INPUT DATA BIT 7

0372 SEL UNCOMP INPUT DATA

0370 SUBTRACT COMMAND

0430 T REG BIT 0 - 3

0431 T REG BIT 4 - 7

0810 SAVE CONTENTS OF OD REG

0550 PULL-UP 1

0361 R REG BIT 4

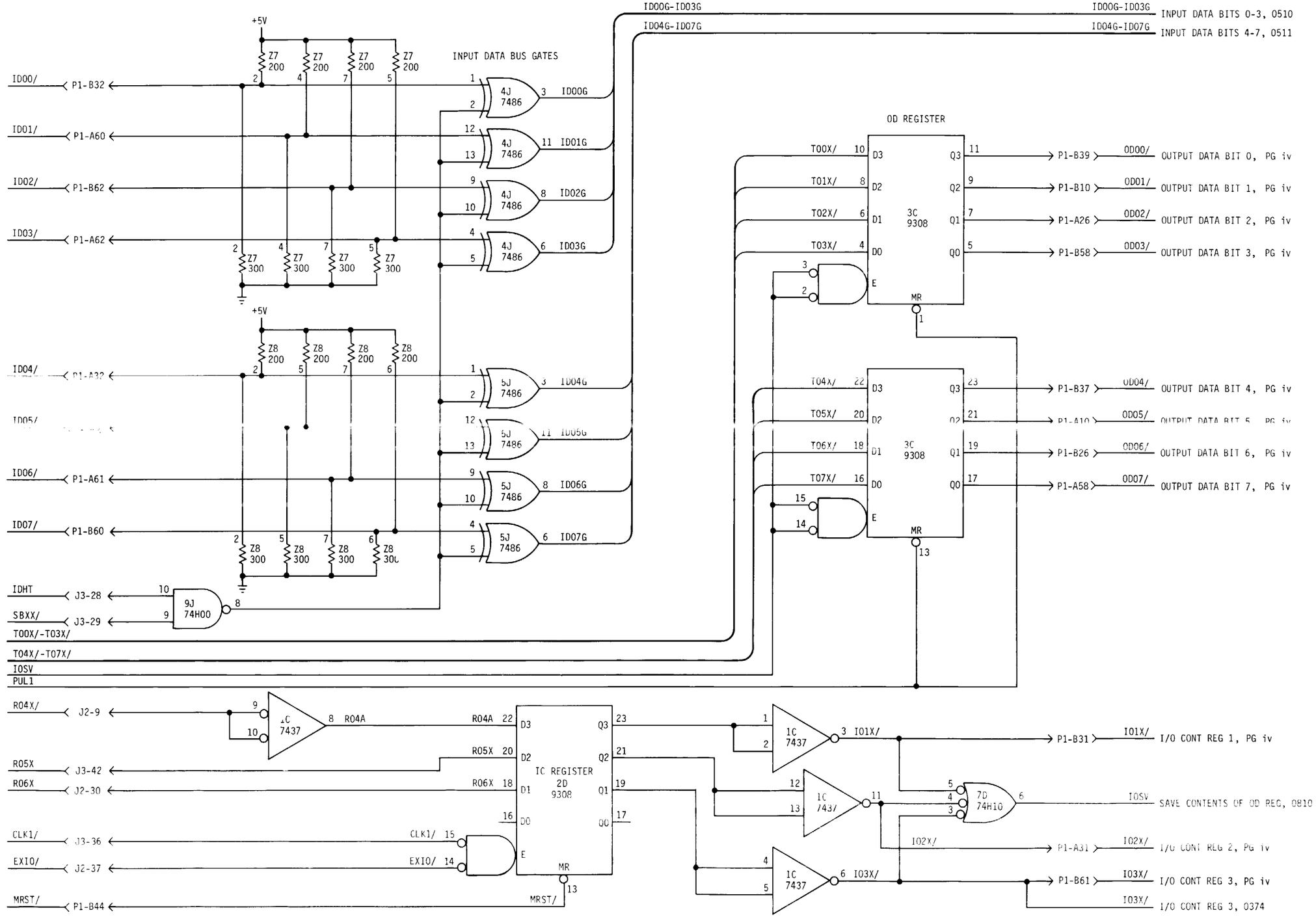
0361 R REG BIT 5

0361 R REG BIT 6

0230 DATA CLOCK

0372 EXTERNAL I/O COMMAND

PG iv MASTER RESET




INPUT DATA BUS GATES, IC REGISTER AND OD REGISTER

INPUT DATA BITS 0-3, 0510

INPUT DATA BITS 4-7, 0511

OUTPUT DATA BIT 0, PG iv

OUTPUT DATA BIT 1, PG iv

OUTPUT DATA BIT 2, PG iv

OUTPUT DATA BIT 3, PG iv

OUTPUT DATA BIT 4, PG iv

OUTPUT DATA BIT 5, PG iv

OUTPUT DATA BIT 6, PG iv

OUTPUT DATA BIT 7, PG iv

I/O CONT REG 1, PG iv

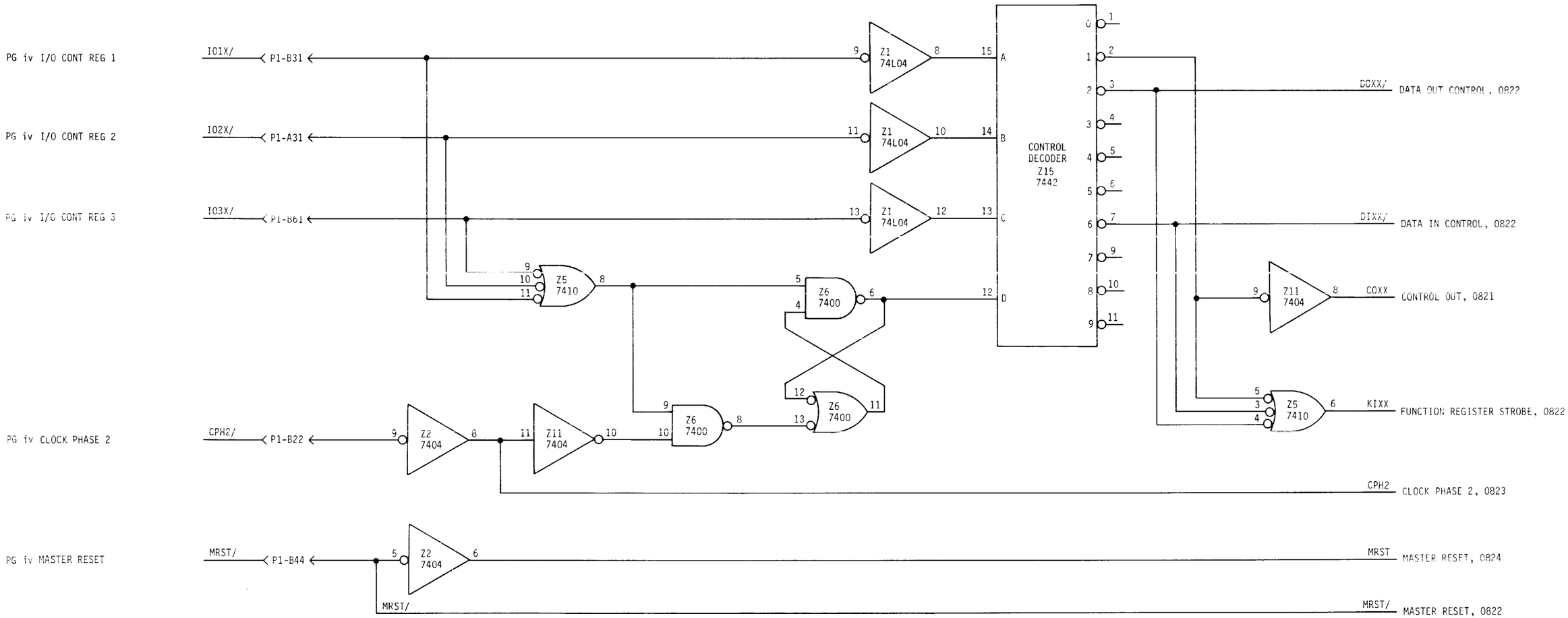
SAVE CONTENTS OF OD REG, 0810

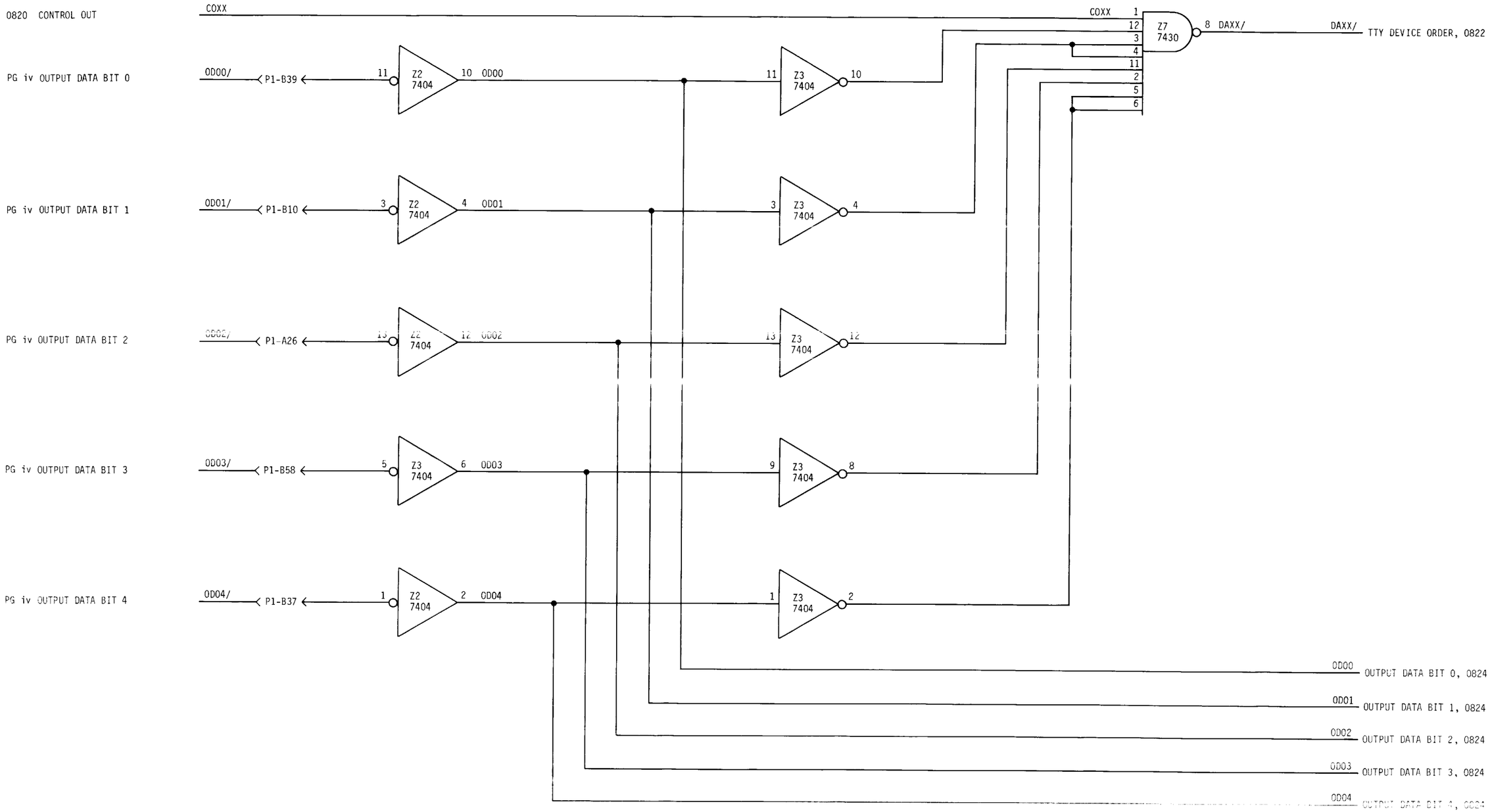
I/O CONT REG 2, PG iv

I/O CONT REG 3, PG iv

I/O CONT REG 3, 0374

J3 DATA BOARD
0810

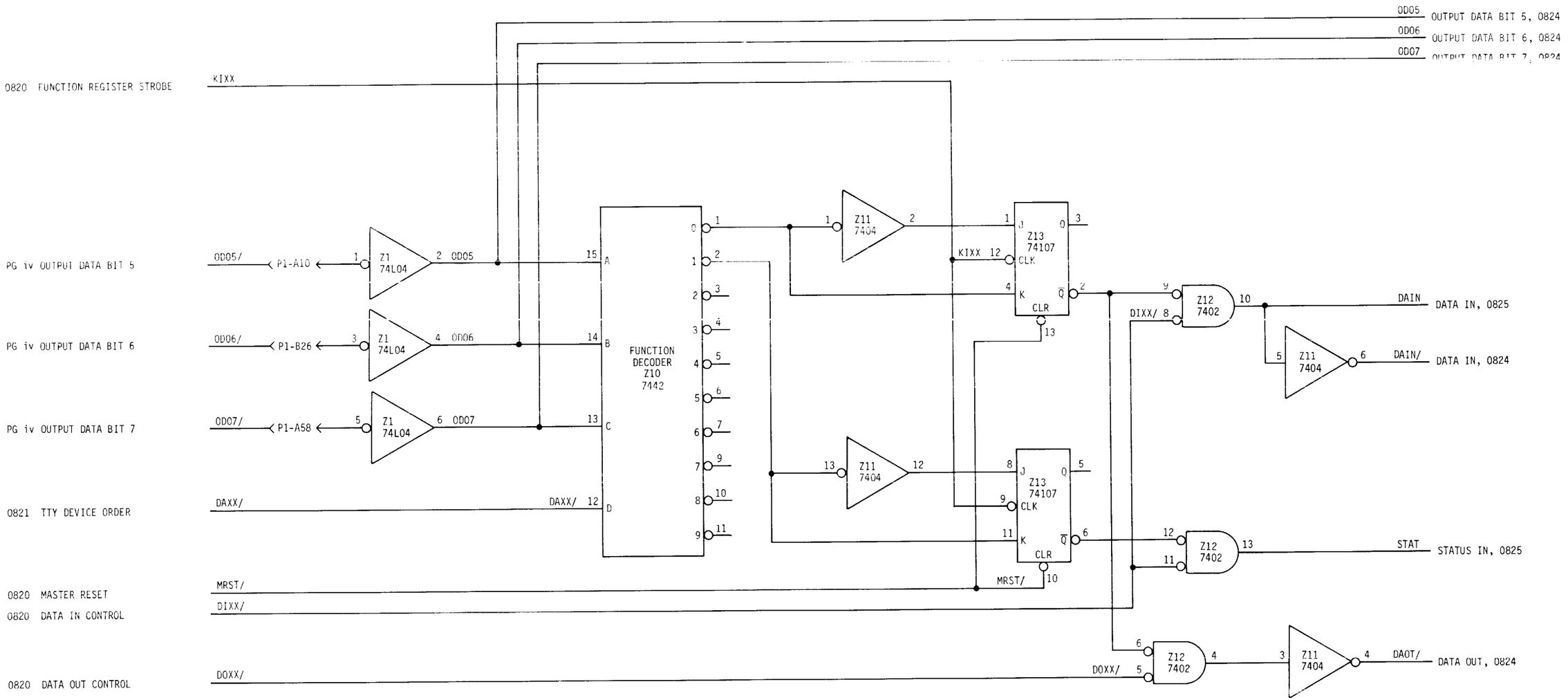

PG iv I/O CONT REG 1
IO1X/
P1-B31
PG iv I/O CONT REG 2
IO2X/
P1-A31
PG iv I/O CONT REG 3
IO3X/
P1-B61
Z1 74L04
Z5 7410
Z6 7400
CONTROL DECODER Z15 7442
DOXX/
DATA OUT CONTROL, 0822
DIXX/
DATA IN CONTROL, 0822
Z11 7404
COXX
CONTROL OUT, 0821
KIXX
FUNCTION REGISTER STROBE, 0822
PG iv CLOCK PHASE 2
CPH2/
P1-B22
Z2 7404
CPH2
CLOCK PHASE 2, 0823
PG iv MASTER RESET
MRST/
P1-B44
MRST
MASTER RESET, 0824
MRST/
MASTER RESET, 0822

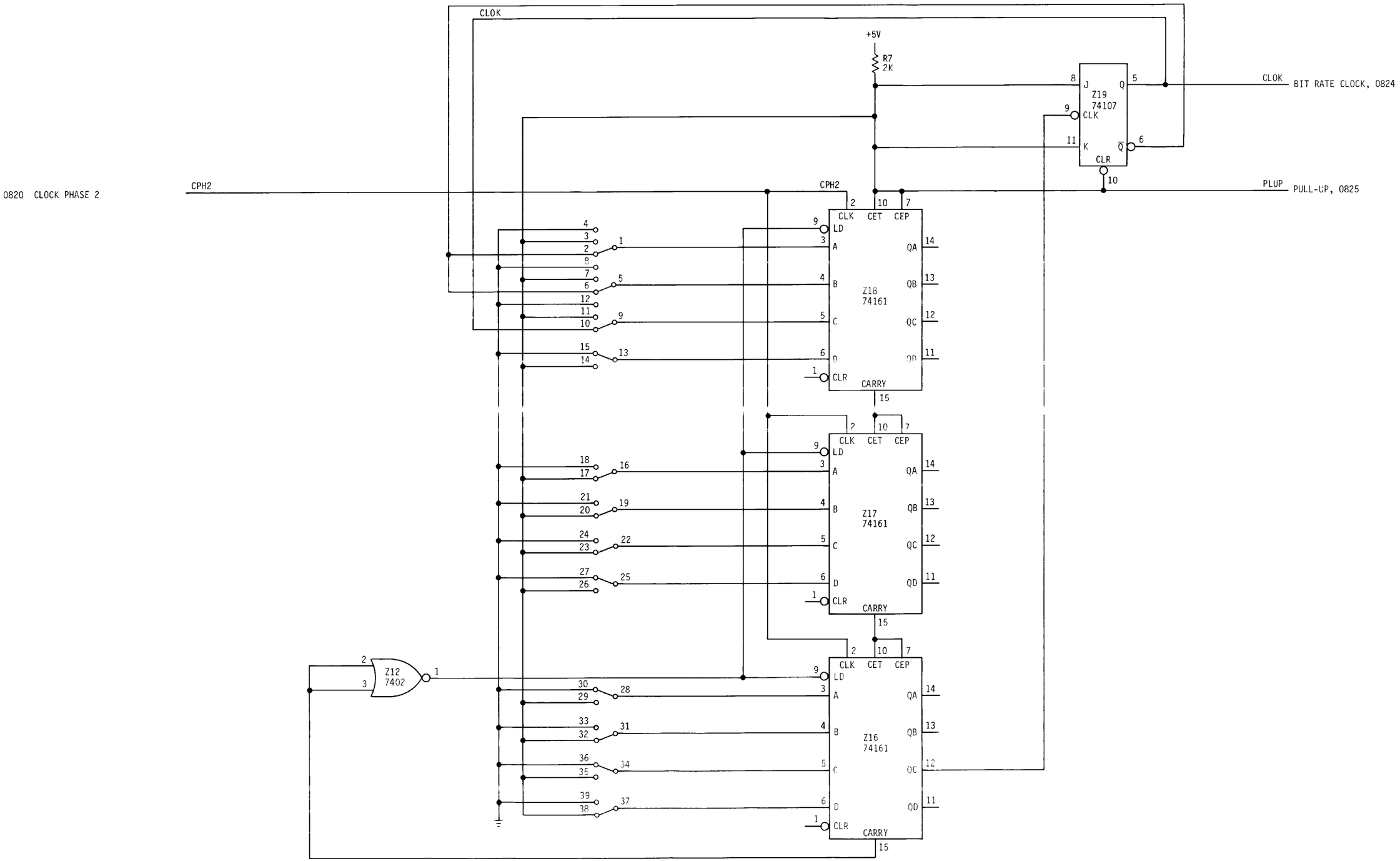



TTY CONTROLLER - ADDRESS DECODER

J1 INTERFACE BOARD
0821

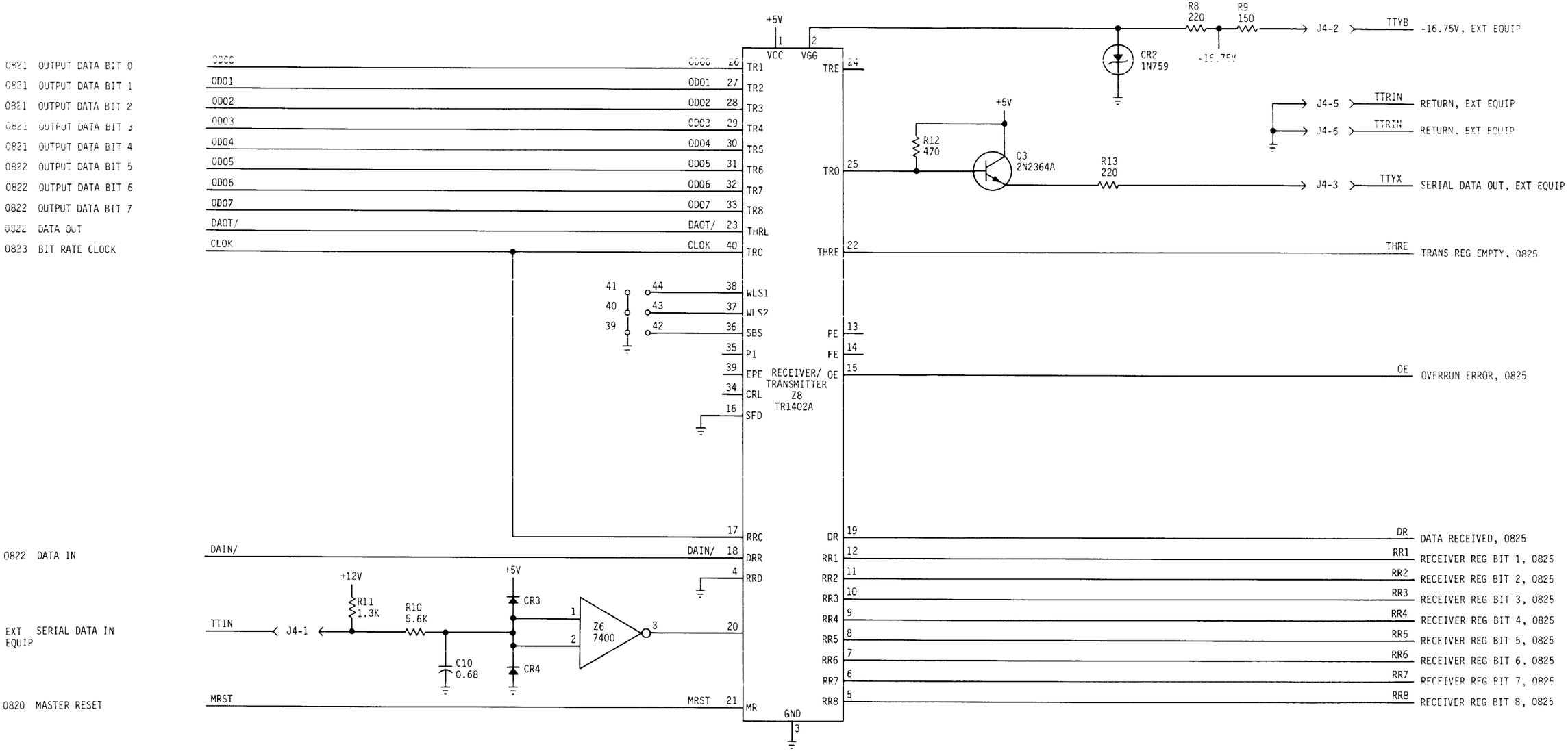
# TTY CONTROLLER - FUNCTION DECODER

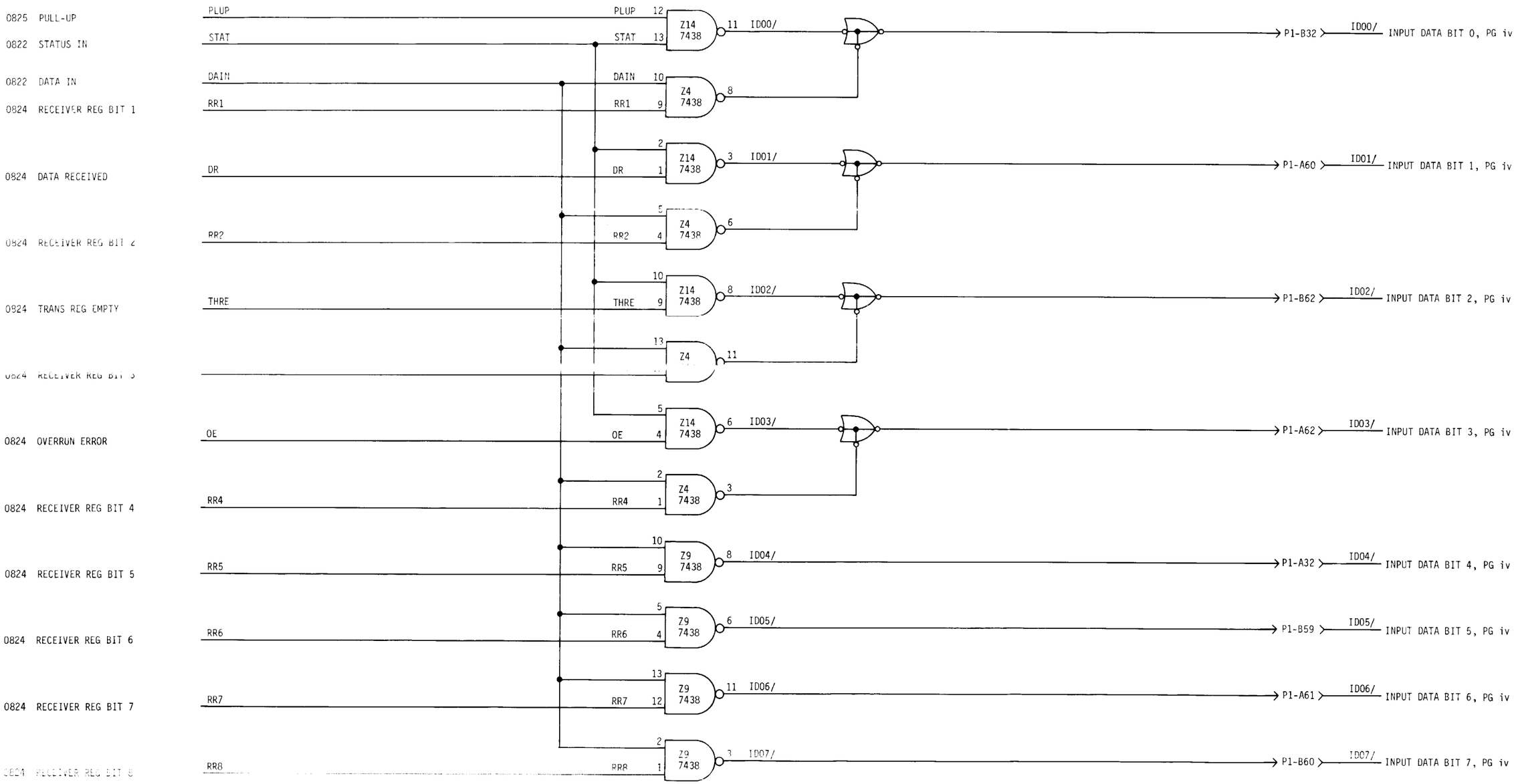





TTY CONTROLLER - BIT RATE CLOCK GENERATOR

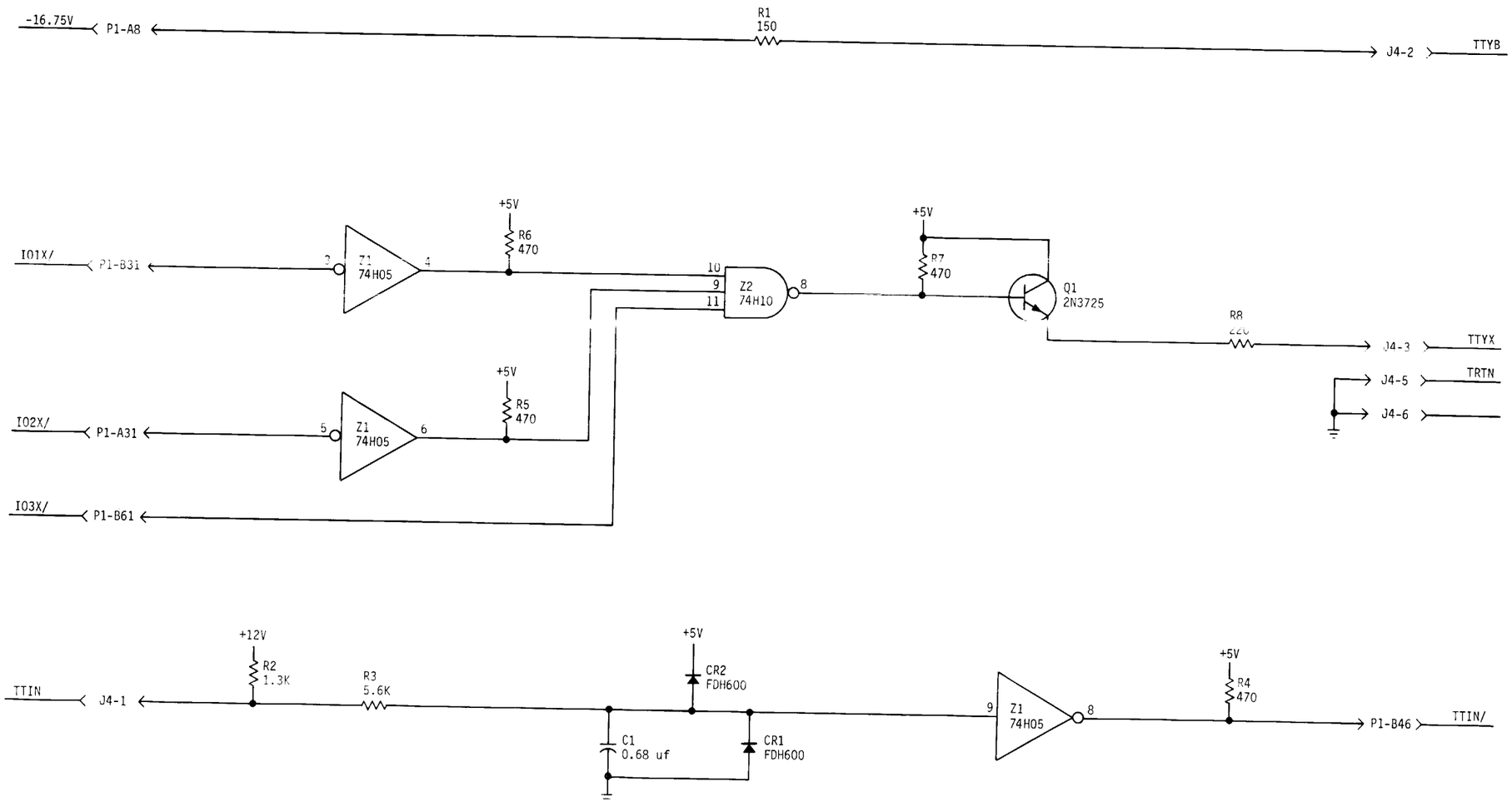
J1 INTERFACE BOARD
0823


0821 OUTPUT DATA BIT 0
0821 OUTPUT DATA BIT 1
0821 OUTPUT DATA BIT 2
0821 OUTPUT DATA BIT 3
0821 OUTPUT DATA BIT 4
0822 OUTPUT DATA BIT 5
0822 OUTPUT DATA BIT 6
0822 OUTPUT DATA BIT 7
0822 DATA OUT
0823 BIT RATE CLOCK
ODO0
ODO1
ODO2
ODO3
ODO4
ODO5
ODO6
ODO7
DAOT/
CLOK
+5V
VCC
VGG
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
THRL
TRC
TRE
TRO
THRE
WLS1
WLS2
SBS
P1
EPE
CRL
SFD
PE
FE
OE
RECEIVER/ TRANSMITTER Z8 TR1402A
R8 220
R9 150
-16.75V
CR2 1N759
J4-2
TTYB
-16.75V, EXT EQUIP
J4-5
J4-6
TTRIN
RETURN, EXT EQUIP
R12 470
Q3 2N2364A
R13 220
J4-3
TTYX
SERIAL DATA OUT, EXT EQUIP
THRE
TRANS REG EMPTY, 0825
OE
OVERRUN ERROR, 0825
0822 DATA IN
DAIN/
RRC
DRR
RRD
DAIN/
DR
RR1
RR2
RR3
RR4
RR5
RR6
RR7
RR8
DATA RECEIVED, 0825
RECEIVER REG BIT 1, 0825
RECEIVER REG BIT 2, 0825
RECEIVER REG BIT 3, 0825
RECEIVER REG BIT 4, 0825
RECEIVER REG BIT 5, 0825
RECEIVER REG BIT 6, 0825
RECEIVER REG BIT 7, 0825
RECEIVER REG BIT 8, 0825
EXT SERIAL DATA IN EQUIP
TTIN
J4-1
+12V
R11 1.3K
R10 5.6K
C10 0.68
CR3
CR4
Z6 7400
0820 MASTER RESET
MRST
MR
GND

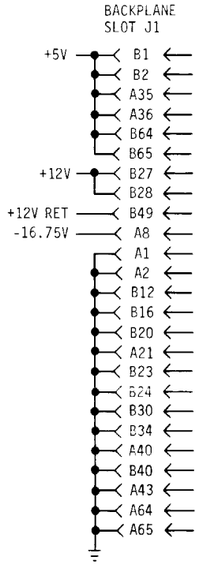


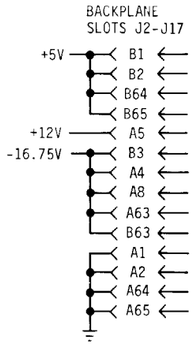

TTY CONTROLLER - INPUT DATA GATES

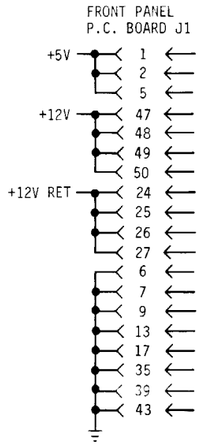
J1 INTERFACE BOARD
0825

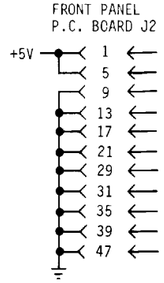


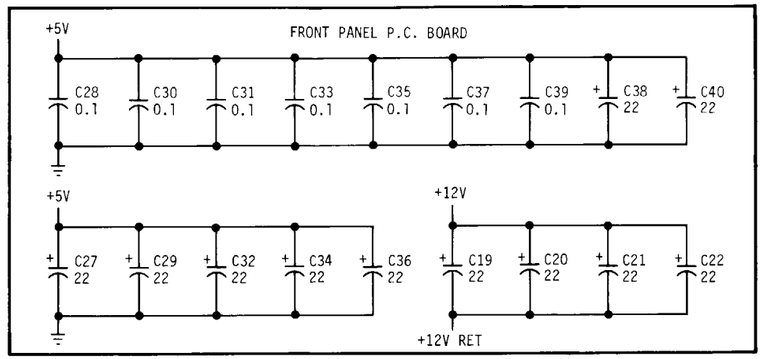

SERIAL TTY INTERFACE

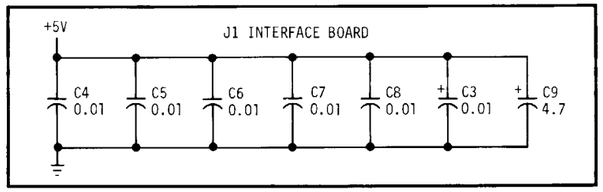


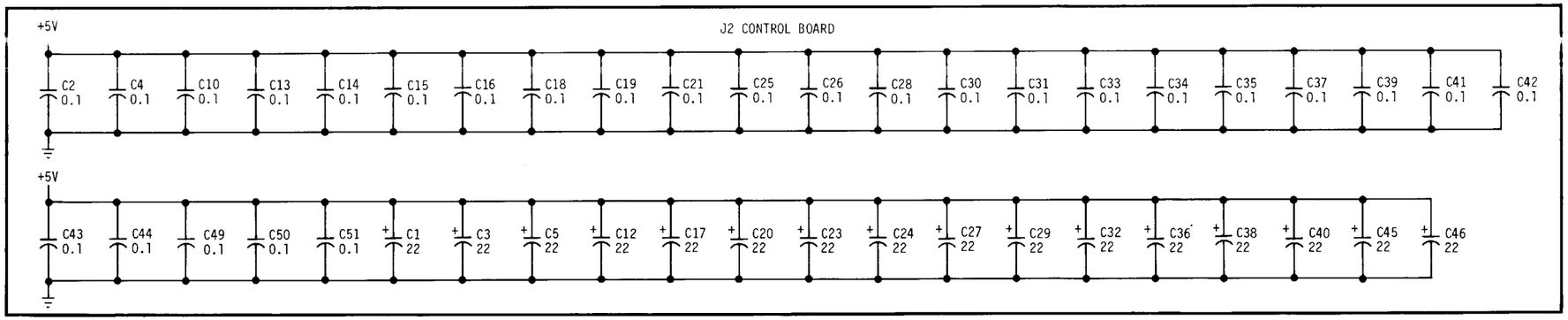



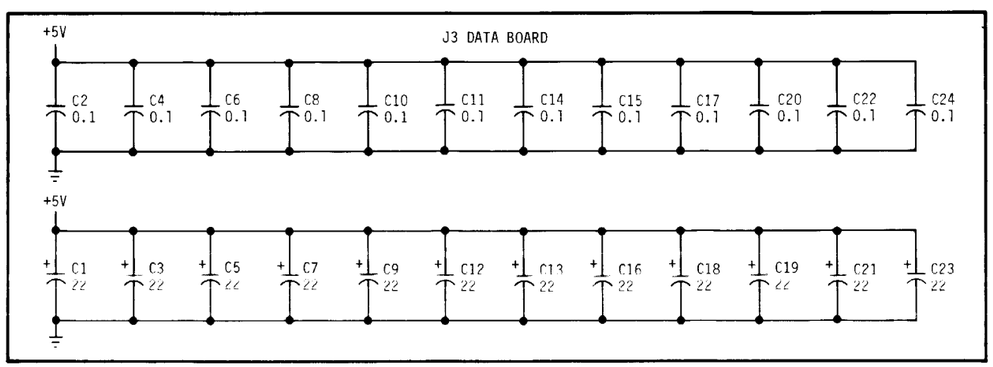



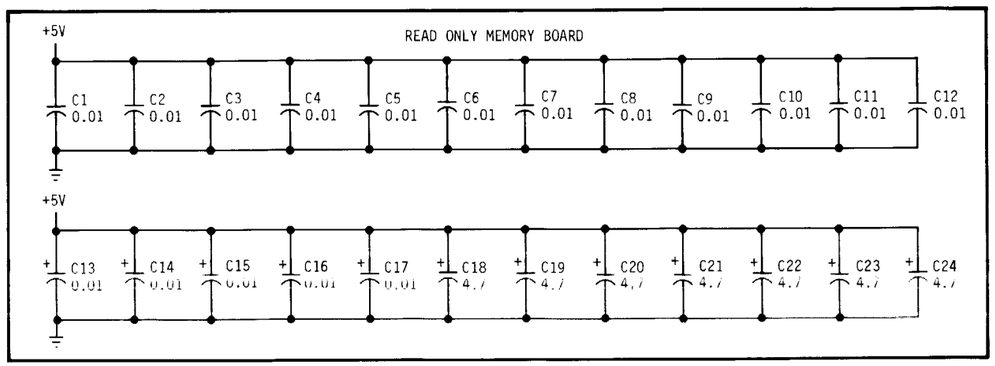




POWER DISTRIBUTION

# POWER SUPPLY CIRCUIT

2010
POWER SUPPLY AND
I18 EXTENDER BOARD

POWER SUPPLY

0110 RESET POWER SUPPLY
RPSS/ P1-A65
0110 RESET POWER SUPPLY
RPSS/ P1-B65
POWER SUPPLY EXTENDER BOARD

TB1
K1
CR8 1N4005
T2
CR7 1N4720
C11 100 MF
TAP
TB2
F1 5A
PWR S1
OFF
ON
B1 4500A
M
AC INPUT 115 OR 230V RMS 50/60HZ
HOT
NEUT
J1
S2
TB3

T1 7383A
CR5 1N1200A
C5 1
CR6 1N1200A
C1 13000
CR1 1N1183
L1
C6 1
CR2 1N1183
C2 130000
R10 100
CR3 1N1200A
C7 1
CR4 1N1200A
R12 0.05
C3 25000
R11 400

Q1 2N3055
R1 0.45
Q7 2N3055
R8 0.22
Q2 2N3055
R2 0.22
Q3 2N3055
R3 0.22
Q4 2N3055
R4 0.22
Q5 2N3055
C9 0.33
Q8 2N3055
R9 0.33
Q6 2N3055
R5 0.33
REGULATOR BOARD A1 (2020)
REGULATOR BOARD A1 (2020)
REGULATOR BOARD A1 (2020)
C4 1
SCR1 C20U

FAILURE DETECTION BOARD A2 (2030)

REMOTE S3

POWER SUPPLY EXTENDER BOARD
P1-B64 — NOT USED
+12V ±5%
0V
+5V ±2%
0V
-16.75V ±2%
P1-A1 PWRD/ POWER FAILURE DETECT, 0620
P1-B1 PWRD/ POWER FAILURE DETECT, 0620

+12 VOLTS
A6, A7, B6, B7

GROUND
A13 - A22, B13 - B22, A50 - A59, B50 - B59

+5 VOLTS
A26 - A46, B26 - B46

-16.75V
A3, A4, B3, B4, A9, A10, B9, B10, A61 - A63, B61 - B63

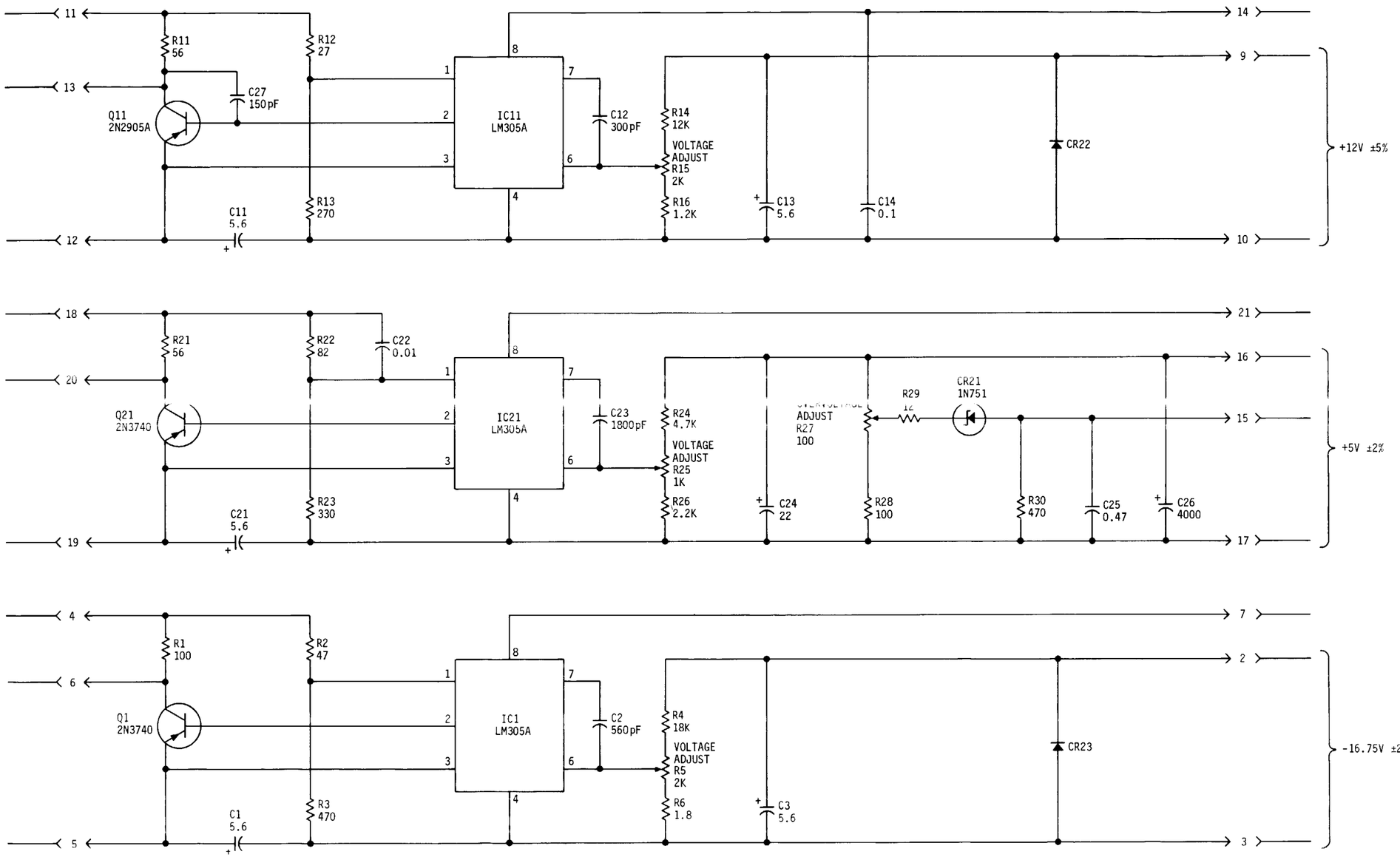
NOTE:

1 FOR 105VAC OPERATION:
JUMPER TB2-1 TO TB2-2
JUMPER TB2-5 TO TB2-6
CONNECT TAP TO TB2-6

FOR 115VAC OPERATION:
JUMPER TB2-1 TO TB2-2
JUMPER TB2-3 TO TB2-4
CONNECT TAP TO TB2-4

FOR 210VAC OPERATION:
JUMPER TB2-2 TO TB2-5
CONNECT TAP TO TB2-6
JUMPER T2-2 TO T2-3
CONNECT T2-1 TO S1-3
CONNECT T2-4 TO TB2-1
CHANGE F1 TO 2.5 AMP

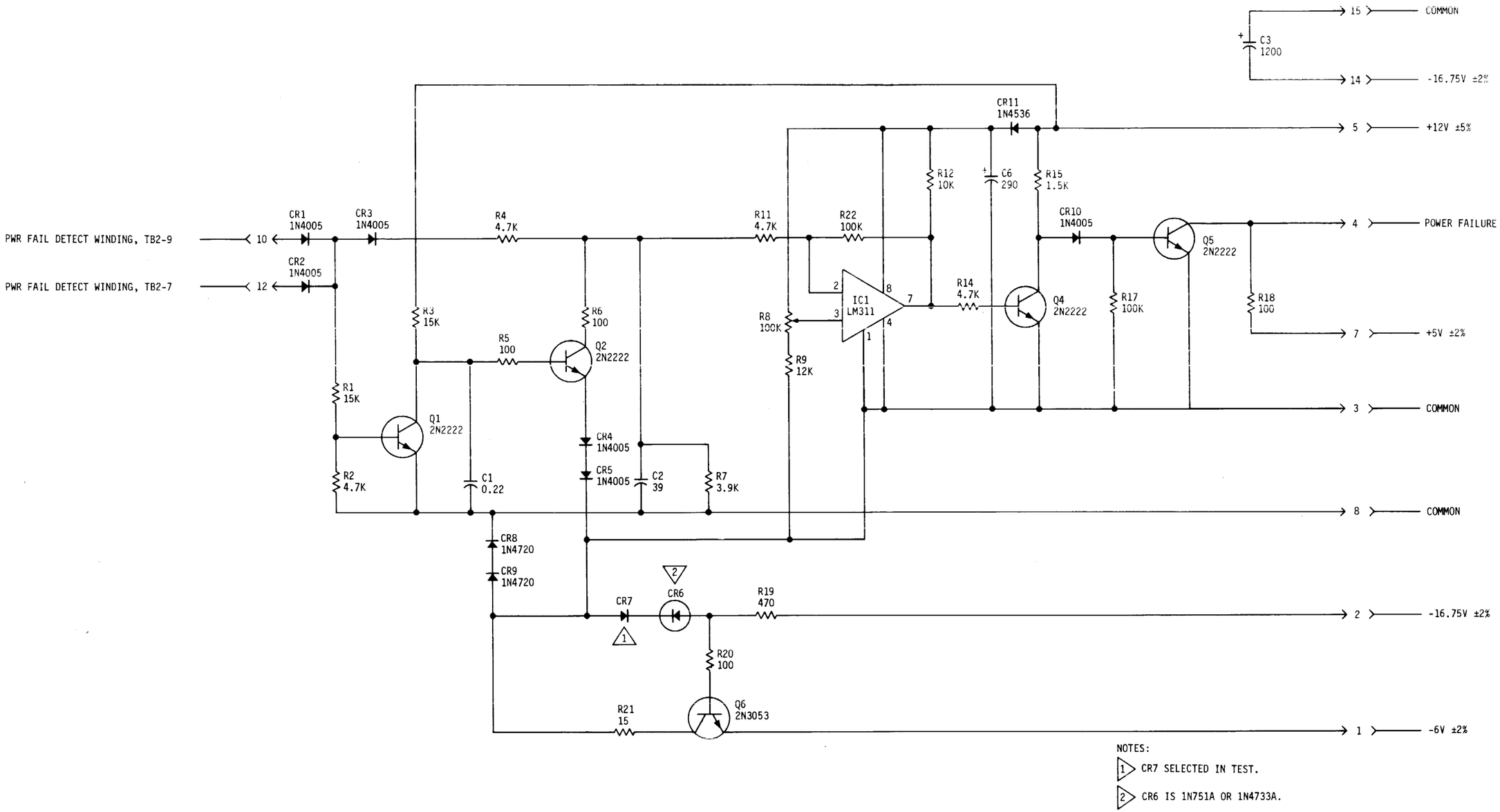
FOR 230VAC OPERATION:
JUMPER TB2-2 TO TB2-3
CONNECT TAP TO TB2-4
JUMPER T2-2 TO T2-3
CONNECT T2-1 TO S1-3
CONNECT T2-4 TO TB2-1
CHANGE F1 TO 2.5 AMP




REGULATOR CIRCUITS

J2 REGULATOR BOARD A1
2020

# FAILURE DETECTION CIRCUIT




NOTES:

1. CR7 SELECTED IN TEST.
2. CR6 IS 1N751A OR 1N4733A.