Single-Supply Applications of CMOS MICRODACs

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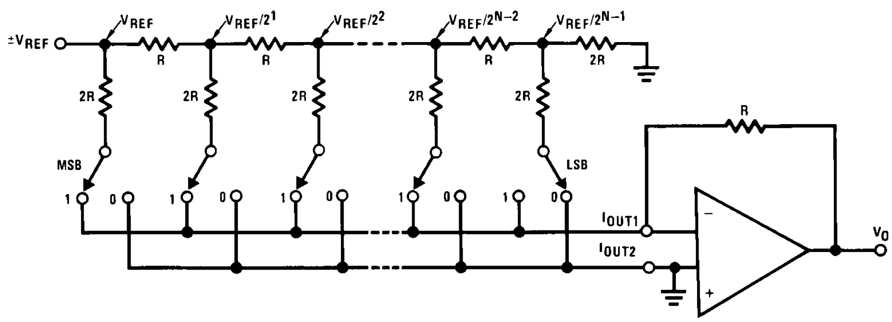
CMOS data acquisition and conversion products are becoming the ideal choice for microprocessor controlled analog systems. The use of CMOS allows the addition of more digital logic functionality on to the same die as the analog circuitry to minimize external parts requirements. The inherently low power consumption is also a big factor for battery operation and low heat generation in large scale systems.

National's MICRODAC™ family of 8, 10 and 12-bit D to A converters all feature on-chip data latches to permit direct interface to 8 or 16-bit data busses. These devices were designed to provide the most versatility from an analog standpoint. By utilizing a current switching R-2R ladder network *(Figure 1),* the applied reference voltage can be either a stable DC voltage or an AC voltage within the wide range of ±10V. However, output linearity requires that the two current output terminals be biased to 0V. This is accomplished by using an external op amp to serve as a current-to-voltage converter. Negative feedback via the feedback resistor included in the DAC keeps the I_{OUT1} terminal at a virtual ground potential. A drawback to this technique is that the output amplifier inverts and outputs a voltage of the opposite polarity of the applied reference. This then requires the output amplifier to have a negative supply voltage if the reference were positive. To operate with only a single-supply by biasing the ground pin of the DAC and the inputs of the op amp to ½ the supply does not work, as the digital inputs are no longer TTL compatible.

All hope is not lost, however, if single-supply operation is essential. By taking a somewhat backwards view of the DAC ladder network, only a single positive supply is necessary. In *Figure 2* the R-2R ladder network is used to switch voltages rather than currents.[1] By applying the reference to the normal current output terminal (I_{OUT1}) and grounding I_{OUT2} the voltage at the reference terminal will be a fraction of the reference voltage and a function of the applied digital input code.

There are two important considerations when using this voltage-switching approach. The applied reference voltage must be positive since there are internal parasitic diodes from the I_{OUT} terminals to ground which would turn on if the reference were to be negative. This, of course, is of no concern with single-supply applications. There is also a dependence of converter linearity and gain error on the voltage difference between the DAC's V_{CC} supply and the applied reference voltage. This is a result of the voltage drive requirement of the CMOS ladder switches. To ensure that all of the switches can turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) an 8-bit DAC should not have a reference greater than 5V and the V_{CC} supply should be at least 9V more positive than the reference. This would keep linearity and gain error degradation less than 0.1%. A 10-bit DAC is a bit more stringent. For a 0.005% or less error degradation, the reference should be less than 3 V_{DC} and V_{CC} should be 10V more positive. The typical effects of bringing V_{REF} and V_{CC} closer together,



N = Number of bits of resolution

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FIGURE 1. The Standard Current-Switching R-2R Ladder Network

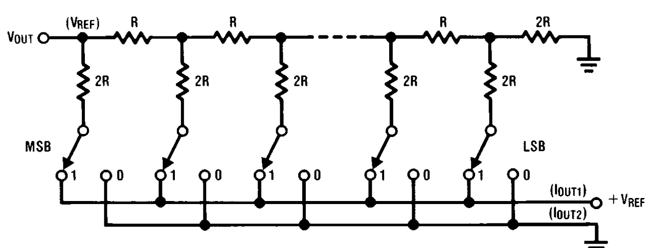

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FIGURE 2. Operating the Ladder "Backwards" to Serve as a Voltage-Switching Network

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as well as temperature performance, are shown graphically in *Figure 3* for the 8-bit DAC0830 series.

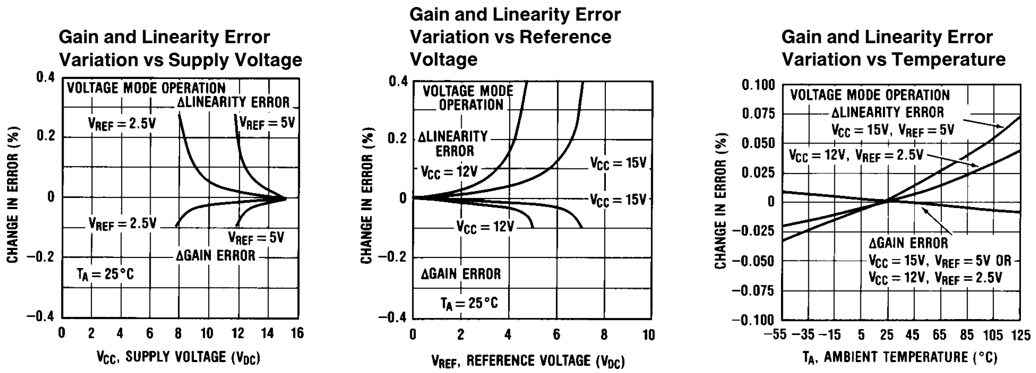
Since the output is now a voltage rather than a current, an output op amp is not necessarily required, but the DAC's output impedance is fairly high (equal to its specified reference input resistance of 10k to 20k), so an op amp may be required for buffering purposes. *Figure 4* shows a single-supply DAC with an output amplifier providing buffering and gain for a more useful 0V to 10V output from a 2.5V reference. The LM336 reference diode is biased through the internal feedback resistor between the I_{OUT1} pin and the R_{fb} pin. The zero-code output voltage is limited by the lower output saturation voltage of the LM358 op amp. The 2k pull-down load resistor helps to reduce this voltage to 10 mV or ¼ of an output LSB. Even with a 15V DAC supply, the digital inputs remain T^2L compatible.

Closer inspection of *Figure 2* shows that both I_{OUT1} and I_{OUT2} drive the ladder network in an identical manner. Each leg is connected to either I_{OUT1} or I_{OUT2} as controlled by the logic state of each digital input. If each I_{OUT} terminal is biased to separate reference potentials, the circuit of *Figure 5* results. This is a single-supply DAC with an adjustable zero-code output offset voltage and adjustable output span to reserve the full resolution of the DAC for a range of voltages other than 0V to full-scale. An important point to note is that for an all ones code applied, only the voltage at I_{OUT1} is connected to the ladder and sets the output to 255/256 times the voltage of I_{OUT1}. With an all zeros code applied, only the voltage at I_{OUT2} drives the ladder, setting the output to 255/256 times this voltage. This non-interaction of the two inputs at the end-points makes calibration a breeze. The incremental analog output steps are automatically set to $(V_{MAX} - V_{MIN})/256$.

The buffers at the two reference inputs in *Figure 5* isolate the code-dependent resistance to ground at I_{OUT1} and I_{OUT2} from the resistive string used to set V_{MAX} an V_{MIN}. The output responds in accordance to the following expression.

(1) $V_{OUT} = D/256\ (V_{MAX} - V_{MIN}) + 255/256\ V_{MIN}$

Where D is the decimal equivalent of the 8-bit binary control word.



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Note: For these curves, V_{REF} is the voltage applied to the I_{OUT1} terminal and I_{OUT2} is grounded.

FIGURE 3. The Effects of Bringing the V_{CC} Supply and V_{REF} Closer Together and Temperature Performance Using the DAC in the Voltage-Switching Mode

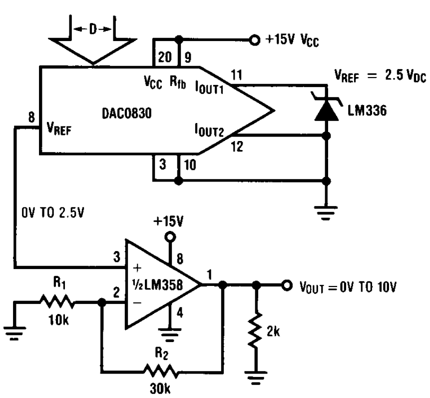

FIGURE 4. Obtaining 0V to 10V Output from a 2.5V Reference

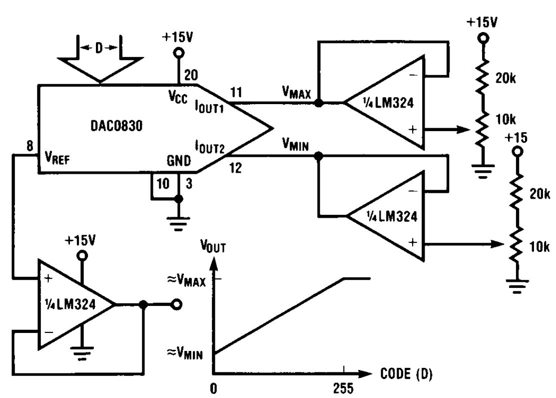

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FIGURE 5. A Single-Supply DAC with Level Shift and Span Adjustable Output

A common requirement of single-supply systems is that the outputs of signal-conditioning amplifiers must be DC biased, typically to ½ of the V_{CC} supply, to provide maximum unclipped AC signal swing. The circuit of *Figure 6* shows how this dual-input voltage-switching DAC configuration can allow the digital input code to control the attenuation of an AC signal without significantly affecting the DC biasing level. If the voltage at I_{OUT2} is set to the DC level of the voltage at I_{OUT1}, then the term in equation (1) which is controlled by the digital input code, D, reduces to just the AC signal at I_{OUT1}. The DC level at the output is 255/256 times the DC level at the input.

The circuit of *Figure 7* combines the advantages of low power consumption of the CMOS MICRODACs together with the non-interactive zero and full-scale adjustability of this voltage-switching technique. This circuit is an isolated 4 mA-20 mA current loop controller where the DAC sets the amount of current that flows through the loop, yet receives its own power from the very same loop.

Digital control and isolation are provided by a single optoisolator and a CMOS counter. The controlling processor must generate a clock and keep track of the number of clock pulses issued to the circuit to know what the loop current is at any time. On power-up the counter is reset to all zeros to give the processor a starting point, as well as to inherently provide a calibration point. When calibrating, potentiometer P1 would be set for the zero-code loop current of 4 mA. The processor would then issue exactly 255 clock pulses to the opto-isolator. Potentiometer P2 can then adjust the full-scale current value to 19.92 mA. If one more clock pulse is issued, the DAC input code returns to all zeros and the previously set value of 4 mA will flow, as this setting was unaffected by the full-scale adjustment.

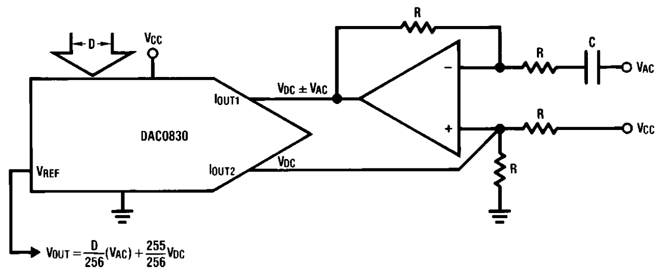

FIGURE 6. Single-Supply DAC where the Digital Input Word Affects the Attenuation of an AC Signal without Significantly Altering its DC Biasing Level

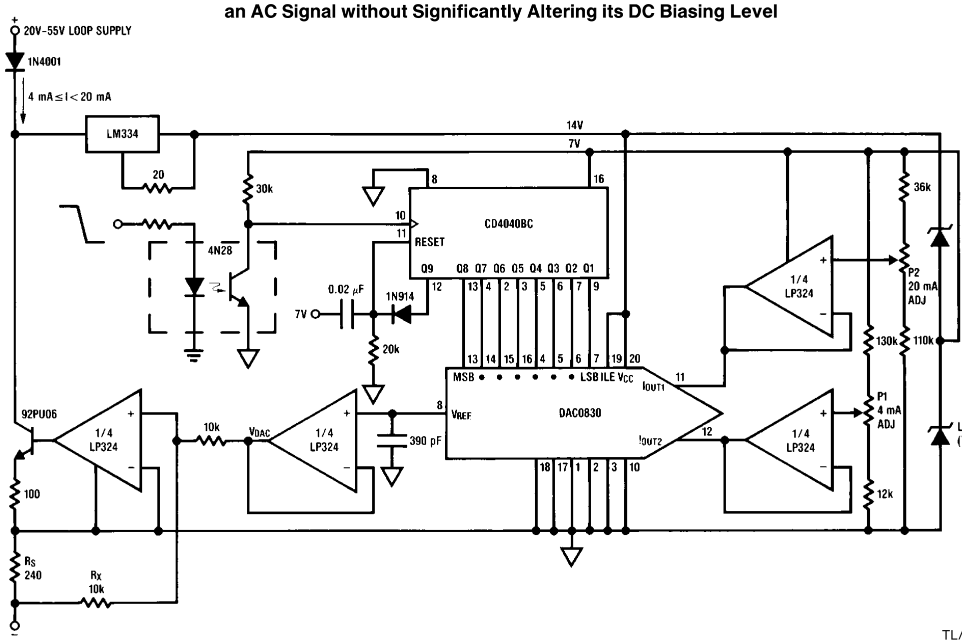

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FIGURE 7. Easily Calibrated, Isolated 4 mA-20 mA Current Loop Controller

The NPN emitter-follower will conduct whatever level of current necessary to keep the voltage across resistor R_S equal to the voltage across resistor R_X. This voltage is equal to the output voltage at the V_{REF} pin of the DAC which can be determined from equation (1). The actual loop current is:

(2) $I_{LOOP} = V_{DAC}(1/R_S + 1/R_X)$

The second LM329 reference diode is used to bias the DAC V_{CC} supply higher than the voltages at I_{OUT1} and I_{OUT2} to preserve linearity.

Finally, what if a D to A function is required, but only a single 5V supply is available and minimal supply current is a primary concern (battery powered instrumentation is a good example)? The voltage-switching techniques previously described are not suitable because not enough voltage is available to properly bias the DAC. A CMOS DAC is still attractive for its low supply current requirements and if it can be operated in the standard current switching configuration, a single 5V supply is sufficient. But how about the voltage inversion and the requirement for negative supply potential?

By taking advantage of an age-old technique of clocking a diode-capacitor network connected as a DC to DC voltage inverter, a low current negative supply can be generated. In the circuit of *Figure 8,* 2 diodes and 2 capacitors are clocked by a CMOS Schmitt trigger oscillator and connected in such a fashion as to generate a −3.8V supply potential. This negative supply is used only to bias a low current LM385-2.5V reference diode to provide the DAC with a stable negative reference. Now the inversion of the output current-to-voltage converter will generate a positive output ranging from 0V to 2.5V as a function of the digital input code.

The amount of ripple that may appear at the reference input is a function of the dynamic impedance of the LM385, the clock frequency and the size of the switching capacitors. For the component values shown, the clock frequency is approximately 1 kHz and the ripple on the reference is 7 mV peak to peak. This ripple is cleanly filtered by the bypass cap around the feedback resistor of the output amplifier. The output op amp is part of a new low power quad, the LP324, which is ideal for its ability to common-mode to ground on the inputs and swing very close to ground at its output. If an extra CMOS Schmitt inverter is not readily available, the oscillator function can be implemented with another of the amplifiers in the op amp package. The total supply current of this single-supply DAC is on the order of 1.5 mA with no output load.

With this technique even the 12-bit DAC1230 can be used with no linearity degradation which would be apparent in the voltage-switching techniques.

REFERENCE

1. Sevastopoulos, N.; Cecil, J.; and Fredericksen, T., *"An Unusual Circuit Configuration Improves CMOS-MDAC Performance",* EDN Magazine, March 5, 1979, pg. 77.

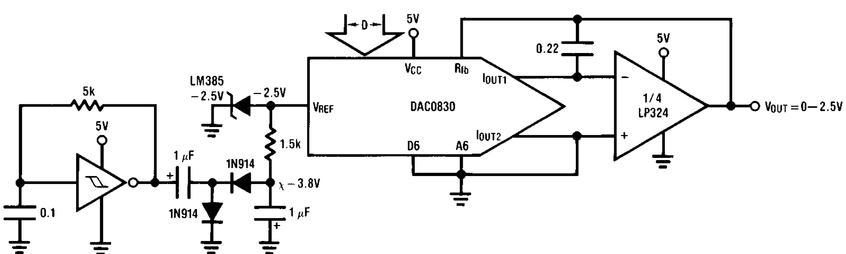

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FIGURE 8. Single 5V Supply, 8-Bit CMOS DAC

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