# The BIPLAN™ DP8342/DP8343 Biphase Local Area Network

National Semiconductor
Application Note 496
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## THE BIPLAN

The BIPLAN is a star local area network designed to demonstrate the capabilities of National Semiconductor's DP8342/43 transmitter/encoder and receiver/decoder chips. These chips are eight bit versions of the DP8340/41 ten bit parts designed to conform to the IBM 3270 protocol. These eight bit devices are ideal for general purpose high speed serial communication. They enable communication at any data rate up to 3.5 megabits/sec over a variety of transmission media with a minimum of external components and easily interface to an eight bit data bus. These devices automatically provide line conditioning, manchester encoding and error checking minimizing transmission errors while enhancing noise immunity and reliability.

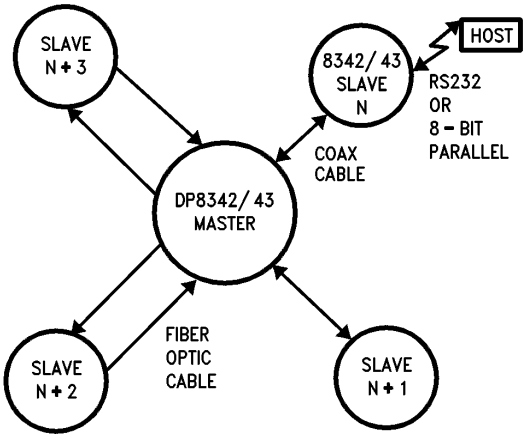


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**FIGURE 1**

The LAN system described here is a star network (see *Figure 1* ) supporting up to 256 nodes with either fiber-optic links or coax links or both (simultaneously) at distances up to 2 miles and a data rate of 3.5 megabits/sec.

To demonstrate this LAN system, a PC board has been developed which can be configured as a master or a slave (the slave hardware is a subset of the master hardware). As a master, the board will support 8 fiber-optic slaves and four coax slaves and can be expanded to support up to 128 fiber-optic slaves and 128 coax slaves simultaneously (see *Figure 2* ). The network interface will communicate with its host either serially (RS-232) or through an eight bit parallel port (multibus). Some features of the network system include:

— 3.5 Megabits/sec data rate
— Distance between slaves—2 miles for coax
— Simultaneous support for 128 fiber-optic slaves and 128 coax slaves
— Protocol insures data integrity—All transfers acknowledged
— 1–254 byte transfers, up to four 254 byte pages per data packet
— 1 kbyte transmit and receive buffers.

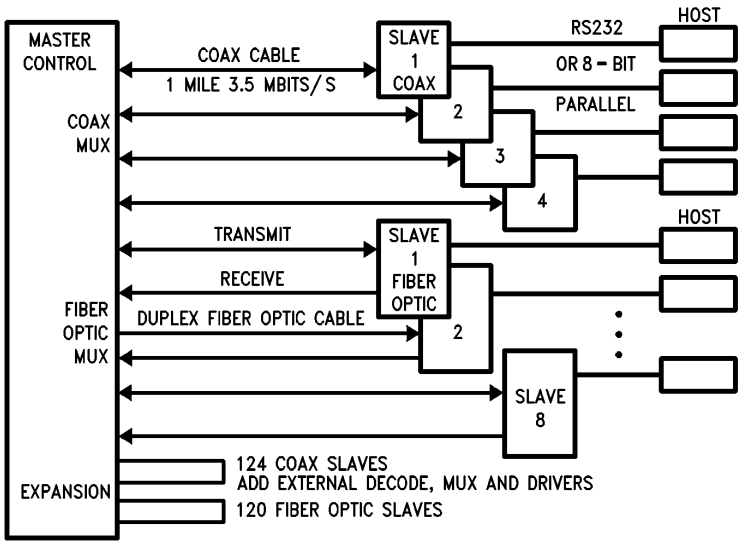


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**FIGURE 2. Master/Slave Network Configuration**

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## NETWORK PROTOCOL

The central node controls access to the network and is therefore termed ''master'' and satellite nodes are ''slaves'' since they provide no network control. The master polls each slave sequentially to offer access to the network. Since the master polls one slave at a time and no slave may transmit unless polled, there is no possibililty of contention. If a slave is not ready to transmit data, it responds to a poll with an ''auto-response'' and the master polls the next slave (see *Figure 3* ). Both the poll and the auto-response (AR) are a single byte transmission with all zero data bits (message types will be discussed in detail later). A disabled or disconnected slave will cause the master to time out and poll the next slave.

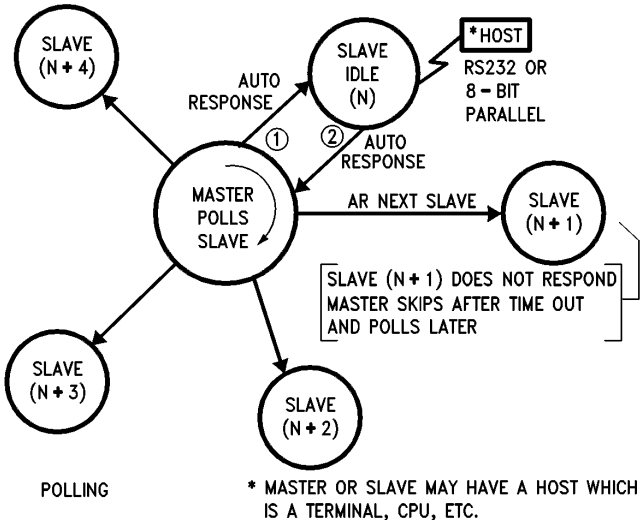


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**FIGURE 3**

If a slave is ready to transmit, it responds to a poll with a ''request to transmit'' indicating the number of pages to be transmitted and a destination address. The master sends this ''request to transmit'' to the destination slave. If the destination slave is not ready to receive data, it sends a ''no-permission to transmit'' and the master sends it to the source slave deferring data transfer until the destination is ready to receive it (see *Figure 4* ). This pre-interrogation prevents wasted data transfers thus improving system throughput. It also allows each node to prepare its DMA circuitry to transfer a block of data.

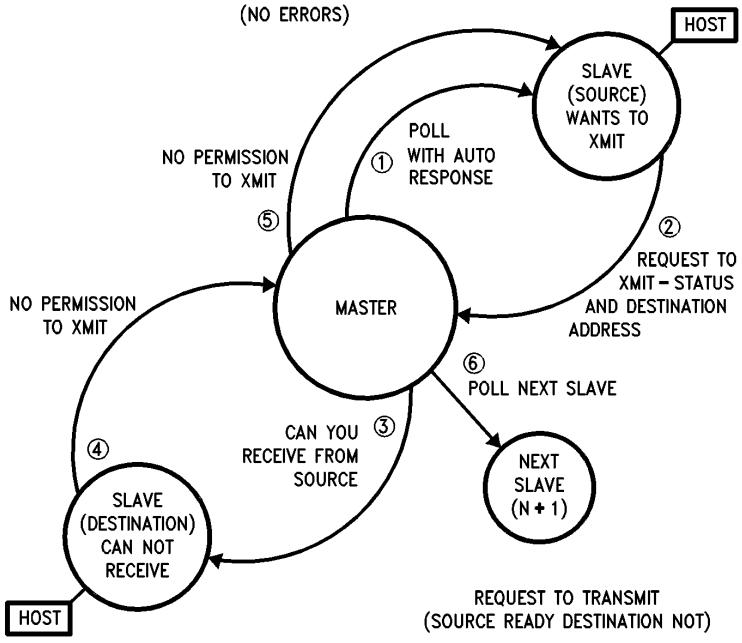


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**FIGURE 4**

In the case where the destination slave is ready to receive data, it sends a ''permission to transmit'' and prepares to receive data. The master, on receiving this ''permission to transmit'' sends it to the source slave and prepares for a transparent transfer of data from source slave to destination slave. The source transmits data and if it reaches the destination without error, the destination slave sends an acknowledge byte. The data/acknowledge cycle continues until the last page of data is transferred. At this point the destination slave sends a special acknowledge called an EOT (''end of transmission'') terminating the communication sequence and releasing the master to poll the next slave (see *Figure 5*).

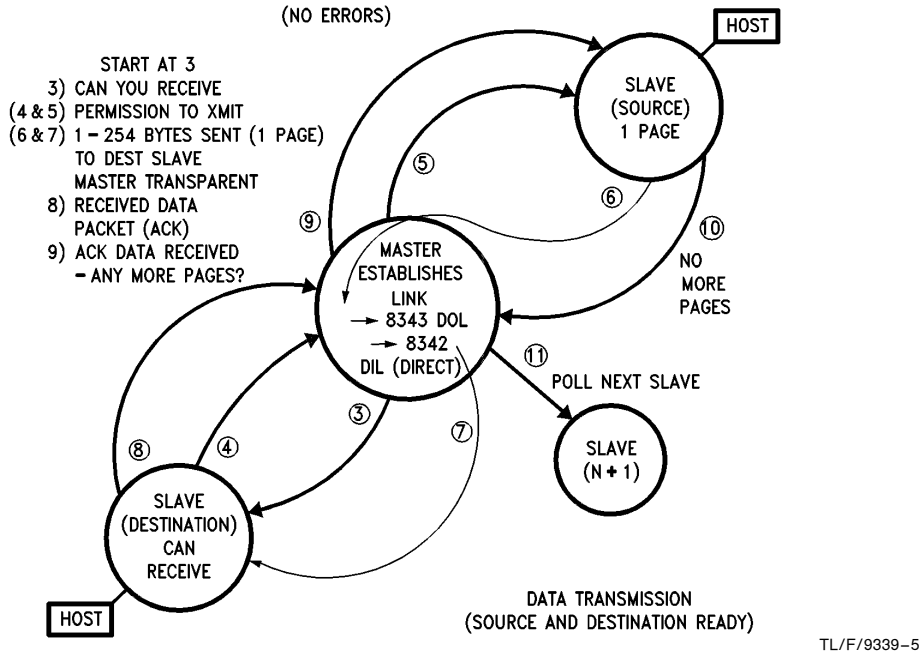


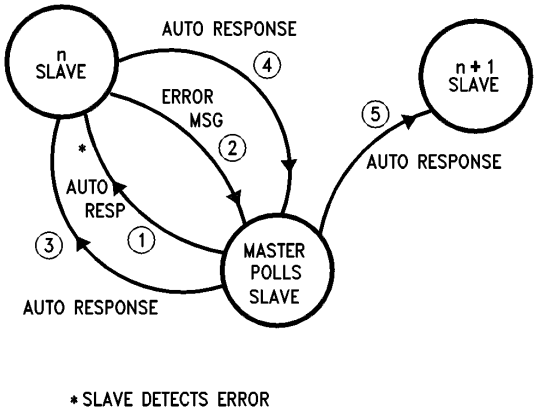

**FIGURE 5**

**ERROR HANDLING**

Recovery from transmission error is handled in the following way. If any node (either master or slave) detects an error while receiving any message from the network (data or control), it sends an error message to the sending node. On receiving an error message, a node retransmits its last message (examples are shown in *Figure 6* ). This may continue to a limit of five retransmission attempts per communication sequence. An error message is simply the error flag register of the DP8343 receiver indicating the type of error that occurred. The receiver provides the following types of internal error checking:

— Data overflow
— Parity error
— Transmit check
— Invalid ending sequence
— Loss of mid-bit transition
— New starting sequence before read
— Receiver disabled while active

**Error on Poll**




*SLAVE DETECTS ERROR

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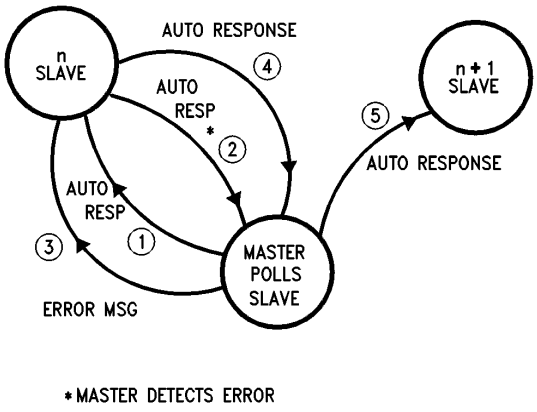
**Error on Auto Response**




*MASTER DETECTS ERROR

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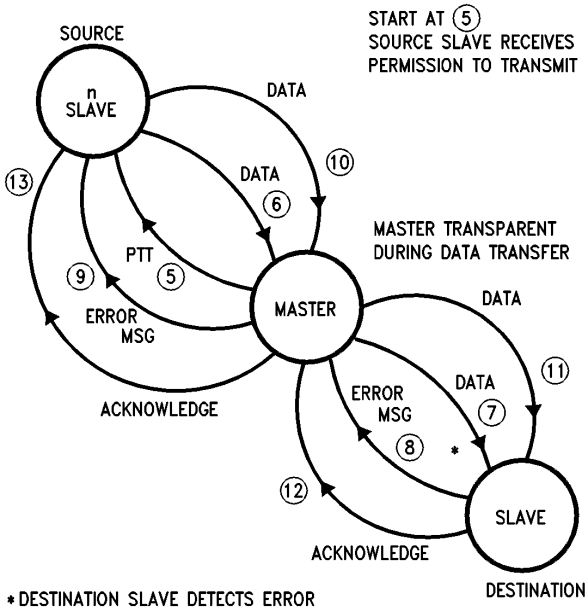
**Error on Data Transfer**




*DESTINATION SLAVE DETECTS ERROR

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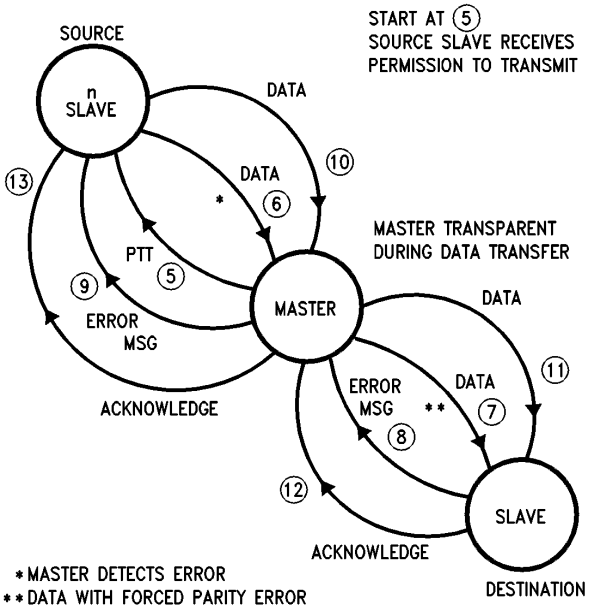
**FIGURE 6**

An exception to this rule is during a transparent data transfer (from source slave through transparent master to destination slave), if the master detects an error, it will not send an error message to the source slave. Instead, the master forces a parity error on the next data byte causing the destination to detect a parity error in the data. The destination slave sends an error message to the master and the master then sends the error message to the source slave which reattempts the data transfer (see *Figure 7* ). This method of forcing a parity error at the master informs the destination slave of the error condition immediately without having to compare byte counts and enables quicker recovery.

The complete network protocol is summarized by the flow chart in *Figure 8*.




*MASTER DETECTS ERROR
**DATA WITH FORCED PARITY ERROR

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**FIGURE 7. Error on Data Transfer**

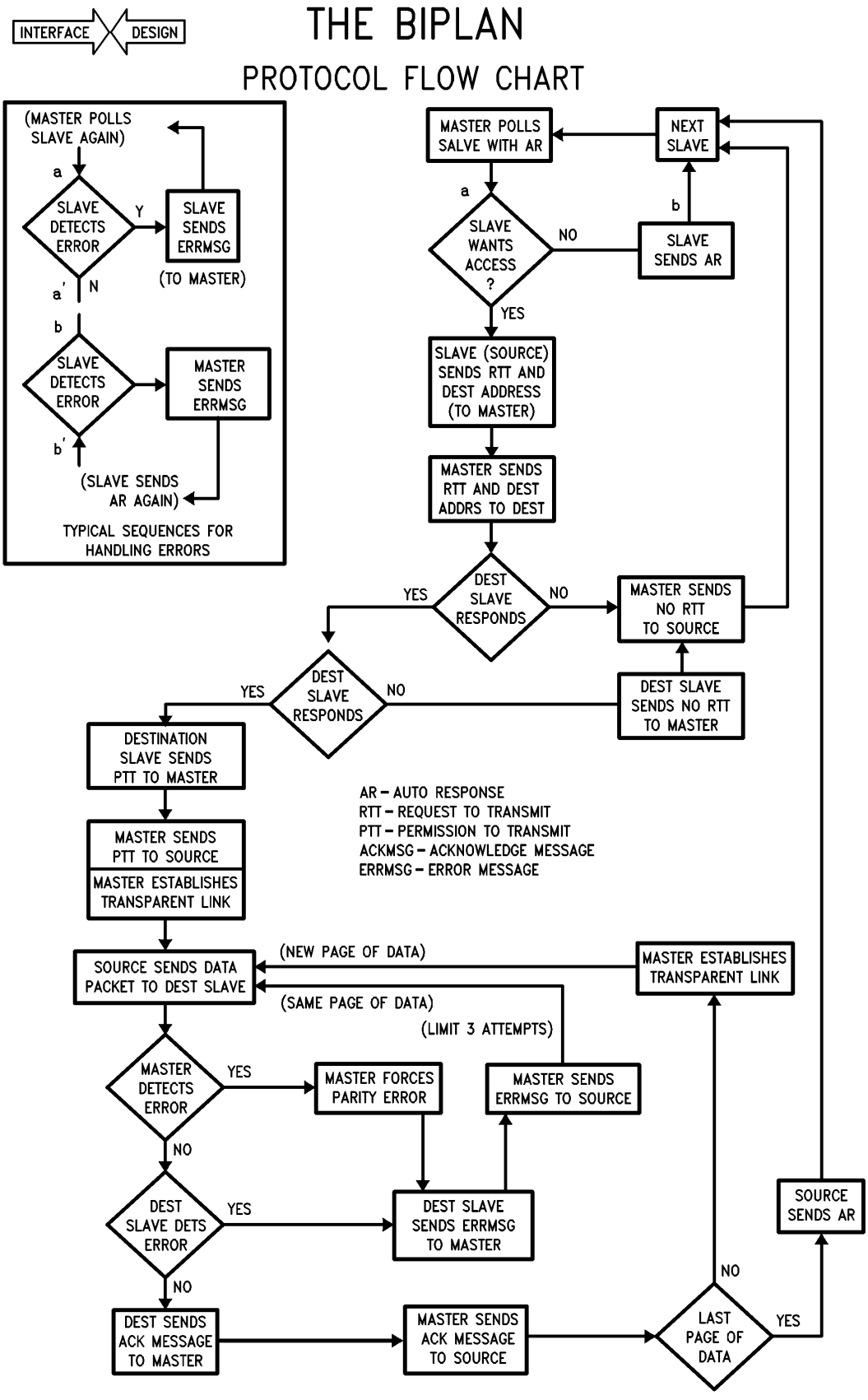


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**FIGURE 8. BIPLAN15B**

## MESSAGE TYPES

There are two major types of messages on the network: control messages and data messages. Control messages are one or two bytes in length and include the following types: poll, auto-response, request to transmit, permission to transmit, acknowledge and error message (see *Figure 9* ). Data messages are 3 to 256 bytes in length and include 1 to 254 bytes of data. Once a node is granted access to the network, it is allowed to transmit up to 4 such data messages (or pages) so that any number of data bytes from 1 to 1016 bytes (4 pages) can be transferred per access. All messages, data as well as control, begin with a status byte as defined in *Figure 9.*

Data communication rates including overhead for the protocol are shown in *Figure 10*. Note that the effective data rate is optimum for large data packets as the overhead becomes a less significant portion of the total time for the data transfer.

**Data Communication Rates Source Slave to Destination Slave**

**Neglecting Cable Propagation Delays**
**(RG 62/AU Coax = 1.2 ns/ft = 3.6 ns/meter)**

| First Page | | Next Two to Four Pages | |
|---|---|---|---|
| **No. of Bytes** | **Time ($\mu$s)** | **No. of Bytes** | **Time ($\mu$s)** |
| 1 | 260 | 1 | 115 |
| 10 | 286 | 10 | 143 |
| 100 | 550 | 100 | 400 |
| 254 | 1000 | 254 | 840 |

Total Time for Transfer of: 1 Page (254 Bytes)—1000 $\mu$s
2 Pages (508 Bytes)—1840 $\mu$s
3 Pages (762 Bytes)—2680 $\mu$s
4 Pages (1016 Bytes)—3520 $\mu$s or
2.3 Mbits/sec

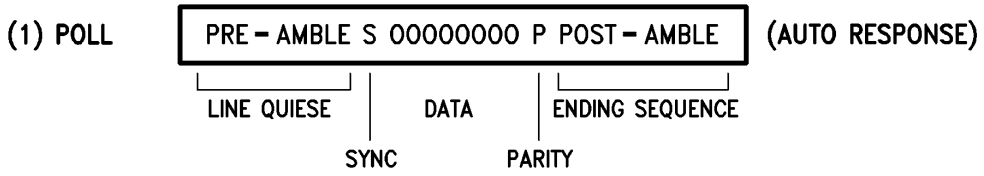
**LATENCY**

No Network Traffic—(40)(N)$\mu$s

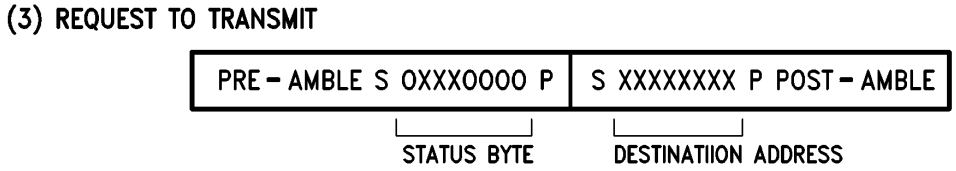
(N) is the number of slaves on the network

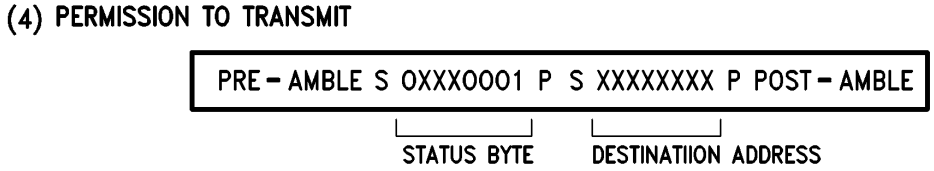
**FIGURE 10**

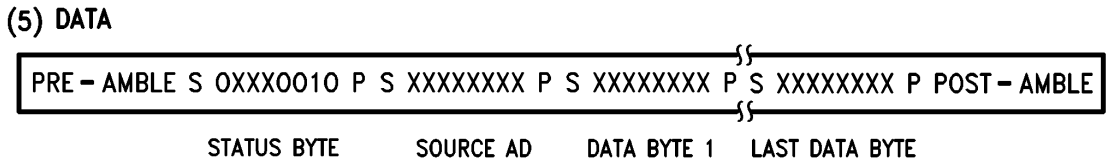
# THE BIPLAN
## MESSAGE TYPES




(2) SLAVE RESPONSE TO POLL (NOT REQUESTING ACCESS)
SAME (AUTO RESPONSE)





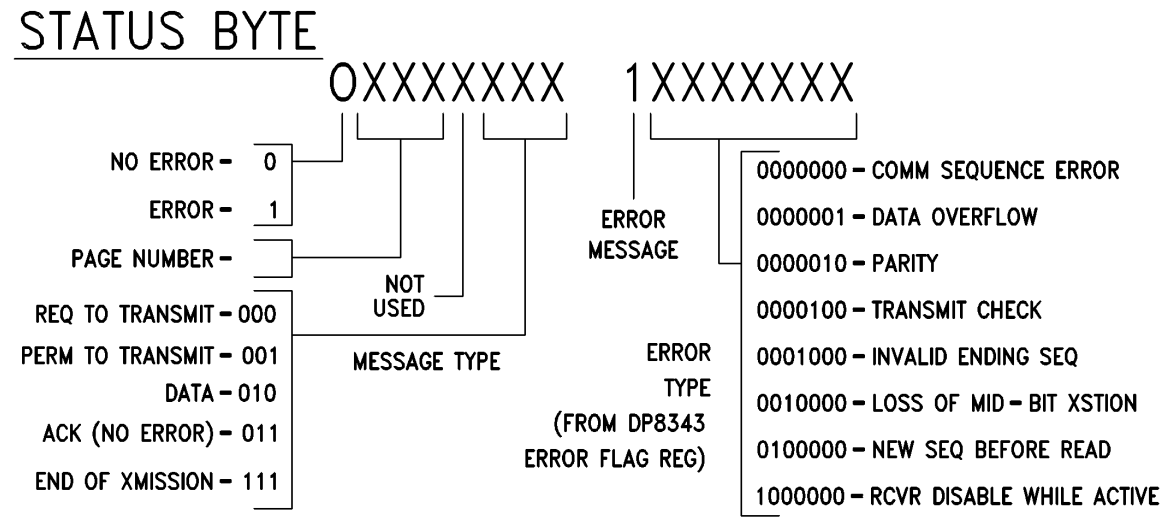



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**FIGURE 9. BIPLAN17**

## DESCRIPTION OF HARDWARE

A block diagram of the network interface showing the major functional elements and the bus structure is shown in *Figure 11*. This represents both the master and the slave except the master contains additional circuitry for multiplexing and de-multiplexing the biphase signal. The CPU (NSC800) provides the intelligence necessary to communicate with the host (8-bit parallel or RS-232 serial) and to implement the network protocol. The DP8342/43 transmitter and receiver both have 2 byte buffers so the CPU can transmit and receive one or two bytes at any time without critical timing requirements. However, the CPU is too slow to accommodate the 350 kbytes/sec data rate during multi-byte (more than 2) transfers. A DMA state-machine controls the transfer of these fast multi-byte messages. Thus, the CPU handles all the control transfers on the network (all 1 or 2 bytes) but the high-speed data must be transferred (to or from the DP8342/43) using direct-memory-access.

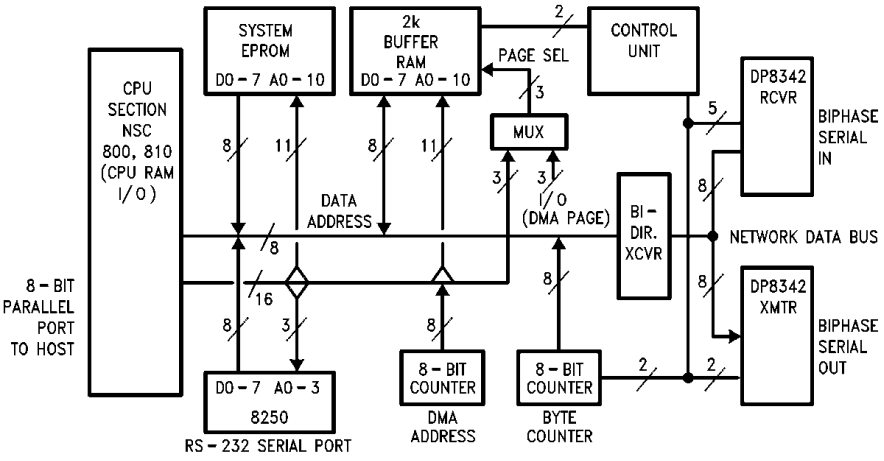


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**FIGURE 11. Network Interface Bus Structure (Slave)**

The state-machine controlling the DMA sequences consists of EPROMS and latches. The CPU commands the state machine using two I/O pins called ''receive request'' and ''transmit request''. A 2 kbyte buffer stores transmit and receive data and is segmented in to eight pages of 256 bytes each. Four pages are allocated for transmit data and four for receive data. When a node has been granted permission to transmit, the CPU loads the appropriate page, loads the DMA counters and asserts ''transmit request''. Similarly, if a node has granted permission to transmit, it prepares to receive data by loading the appropriate page, initializing the DMA counters and asserting ''receive request''. The master may assert both ''receive request'' and ''transmit request'' simultaneously to effect a ''repeat request'' (transparent mode where data from the receiver is loaded directly to the transmitter). *Figure 12* shows the control signals involved in the DMA sequences including those required to handshake with the transmitter and receiver.

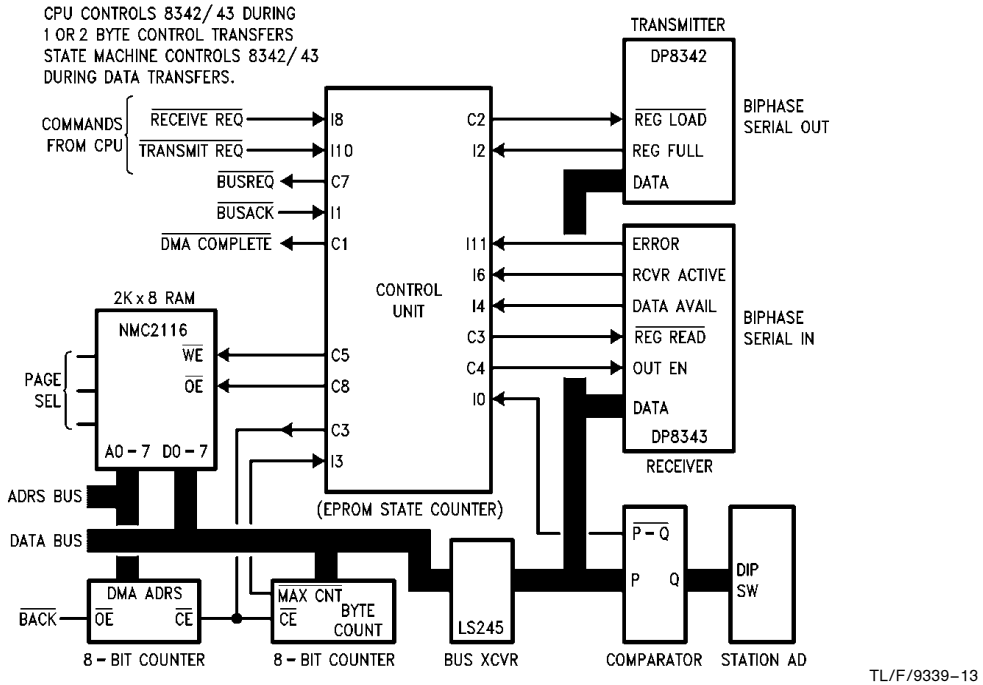


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**FIGURE 12. DMA Section**

An EPROM implementation was selected for the state machine in the interest of flexibility and to keep its operation as lucid as possible. The state machine has three main functions: transmit data (DMA read), receive data (DMA write) and repeat data. *Figure 13* is the state diagram showing how it accomplishes these functions. *Figures 14, 15* and *16* show how the state machine handshakes with the DP8342/43 in getting data on and off the bus.

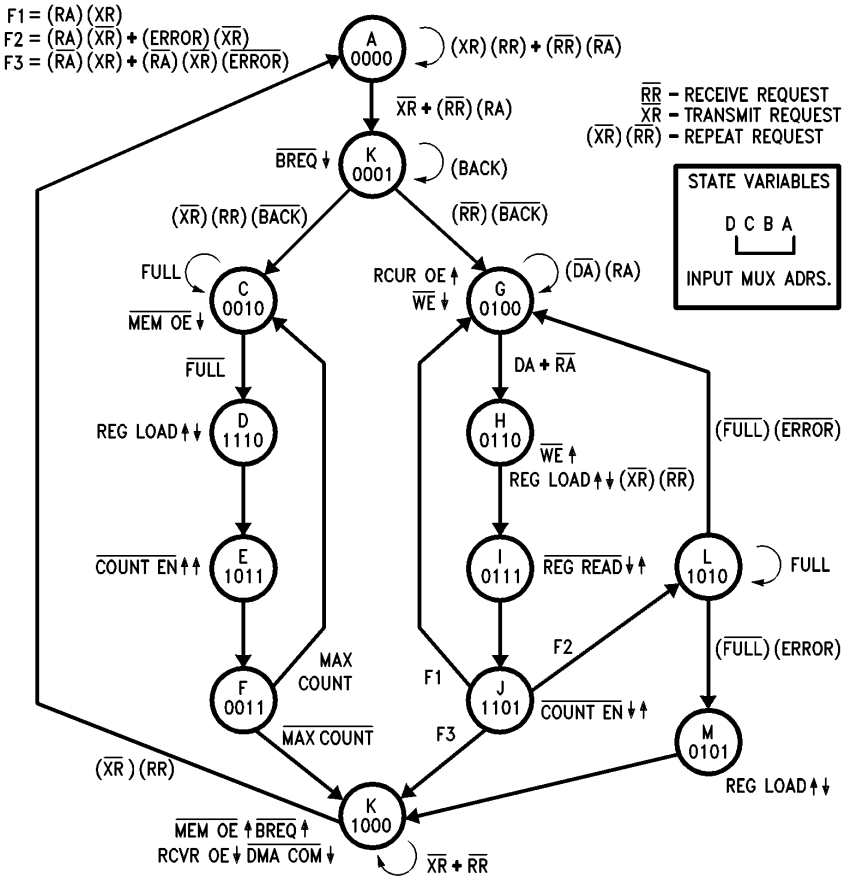


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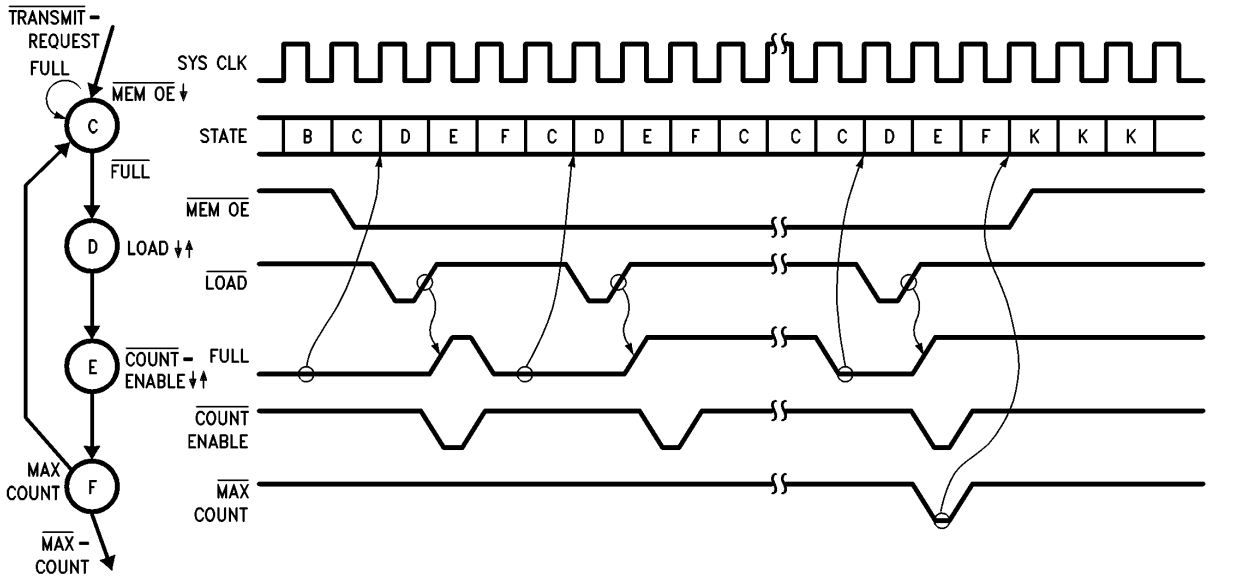
**FIGURE 13. Control Unit State Diagram**

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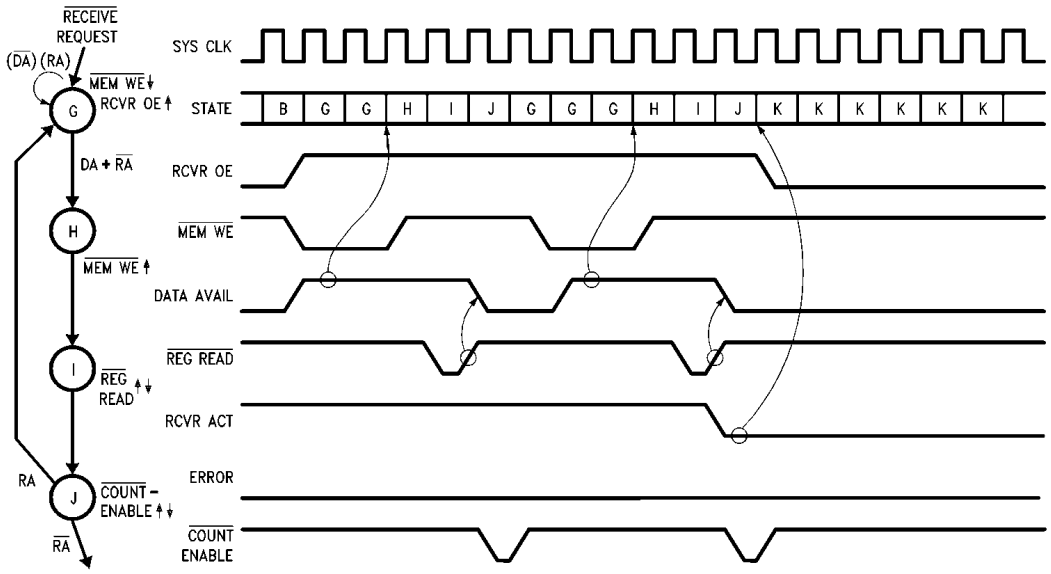
TRANSMIT REQUEST (FROM CPU) INITIATES DATA TRANSMIT SEQUENCE. CONTROLLER WAITS (IN STATE C) UNTIL REG FULL IS LOW BEFORE DOING EACH REG LOAD (IN STATE D). MAX COUNT TERMINATES THE SEQUENCE.

**FIGURE 14. DMA Transmit Timing (Read from Memory)**

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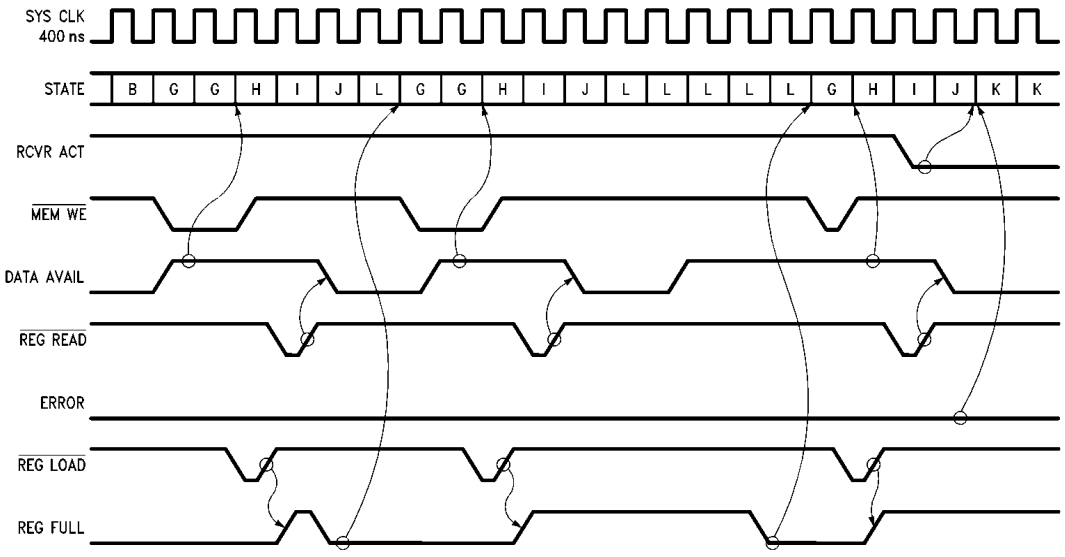
RECEIVER ACTIVE (RA) INITIATES DMA WRITE SEQUENCE ONLY IF REC REQ (RR) IS LOW. FOR EACH WRITE CYCLE, WRITE EN IS KEPT LOW UNTIL DATA AVAIL (DA) GOES HIGH. THIS SIGNIFIES THAT VALID RECEIVE DATA IS ON THE BUS AND THE WRITE CYCLE IS COMPLETED.

**FIGURE 15. DMA Receive Timing (Write to Memory)**

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REPEAT SEQUENCE IS INITIATED ON RECEIVER ACTIVE IF BOTH REC REQ AND XMT REQ ARE LOW. FOR THE FIRST BYTE, THE CONTROLLER WAITS (IN STATE G) FOR DATA AVAILABLE BEFORE DOING A LOAD. FOR SUBSEQUENT BYTES, THE CONTROLLER WAITS (IN STATE L) FOR REGISTER FULL TO GO LOW THEN WAITS FOR DATA AVAILABLE BEFORE DOING EACH LOAD.

**FIGURE 16. Repeat Timing (Master Transparent Mode)**

**MASTER MULTIPLEXING/DE-MULTIPLEXING**

The network master must communicate with multiple slaves so that some method of multiplexing and de-multiplexing the high-speed biphase signals is necessary. For receiving data we must accommodate analog signals from the coaxial links and TTL signals from the fiber-optic receivers. This is easy since the DP8343 receiver has both TTL and analog inputs and an internal mux to select the input. A TTL multiplexer was used to select one of eight fiber-optic channels (expandable off board to 128 channels). For the coax channels, instead of using line receivers and then multiplexing the TTL signals, an analog mux was used to select one of four coax channels (also expandable to 128 channels). This method allows us to take advantage of the excellent input characteristics of the line receiver within the DP8343 receiver and minimizes the number of external components (see *Figure 17* ). For transmitting data, the master must select one of eight fiber-optic drivers or one of four coaxial line drivers. *Figure 18* shows how this is done.

The hardware has been designed for maximum flexibility and to provide a friendly environment for developing communication software. What has been implemented in the present system is the first two layers of the ISO/OSI model of local area networks (the physical layer and the data link layer). That is, the system provides the transfer of data from one station to another assembling frames and handling transmission errors. There is sufficient bandwidth remaining on the network interface CPU to implement any host system interface.

**BIPLAN23**

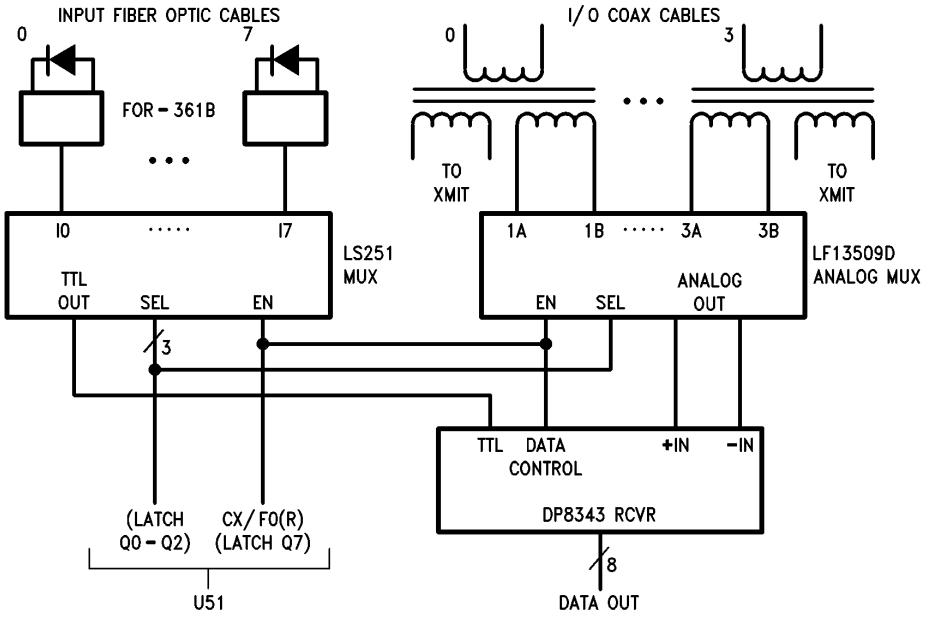


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**FIGURE 17. Receiving Mux (Master)**

**BIPLAN24**

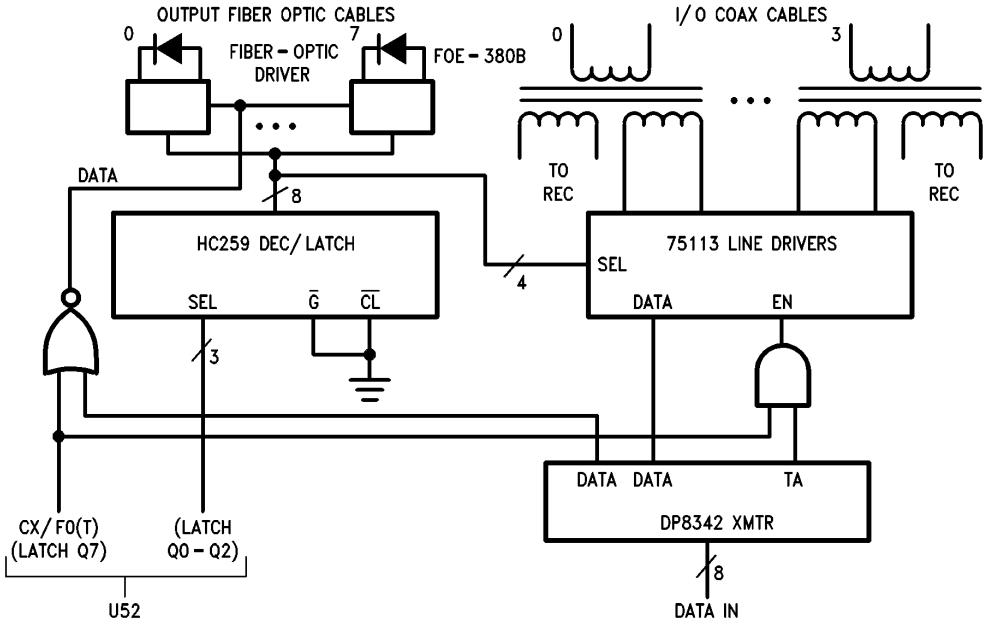


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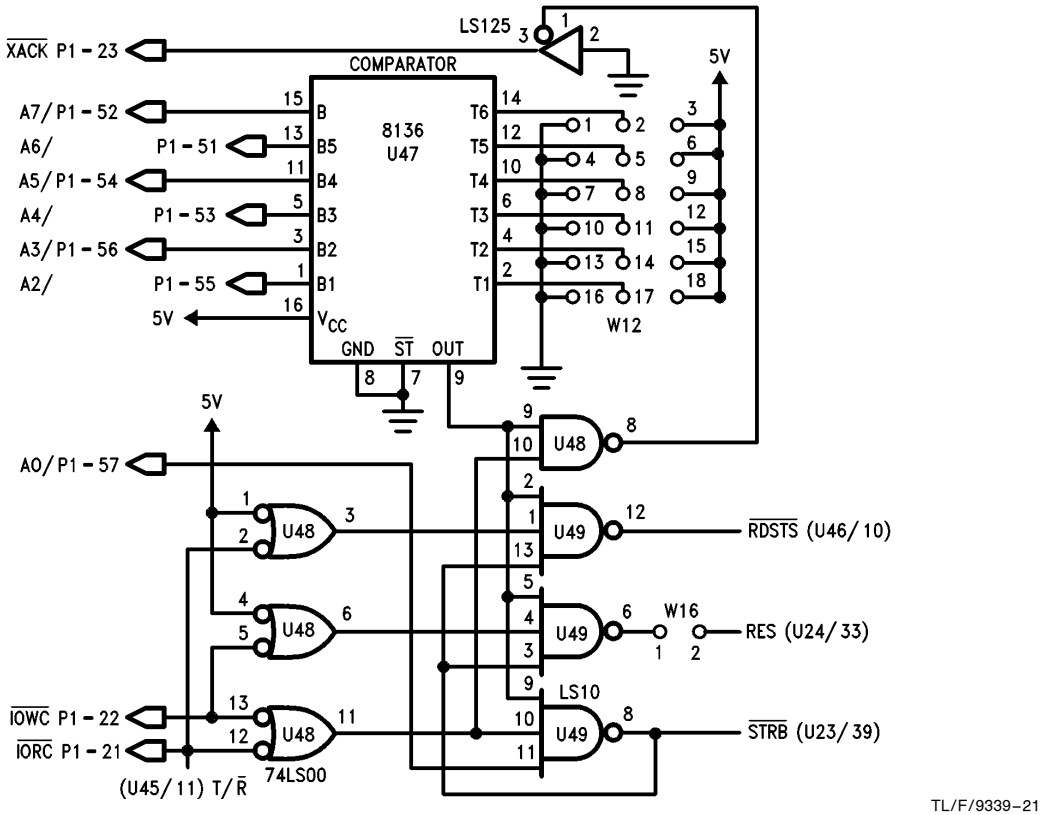
**FIGURE 18. Transmitter Select (Master)**

**THE BIPLAN DP8342/DP8343 BIPHASE LOCAL AREA NETWORK**

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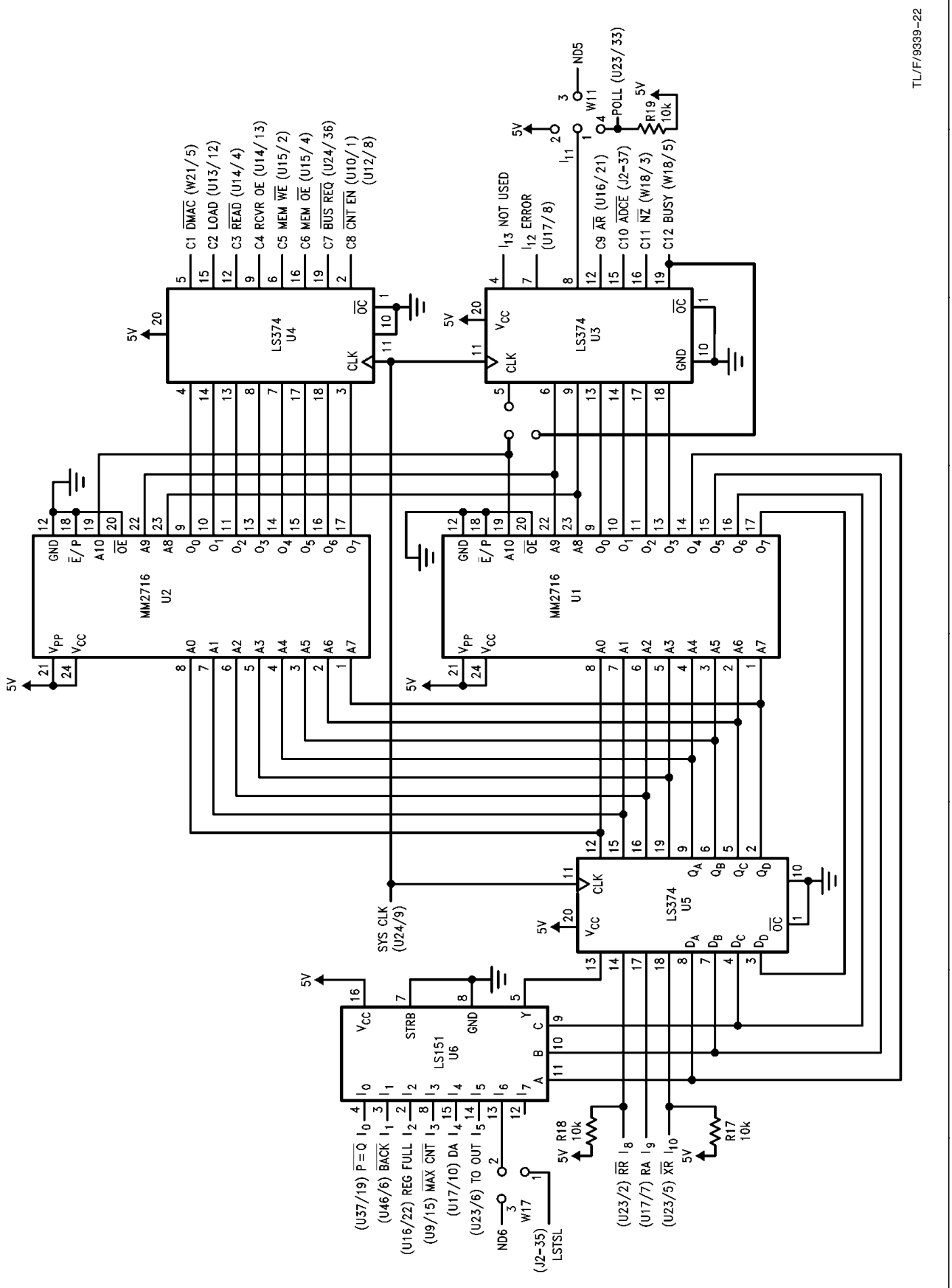
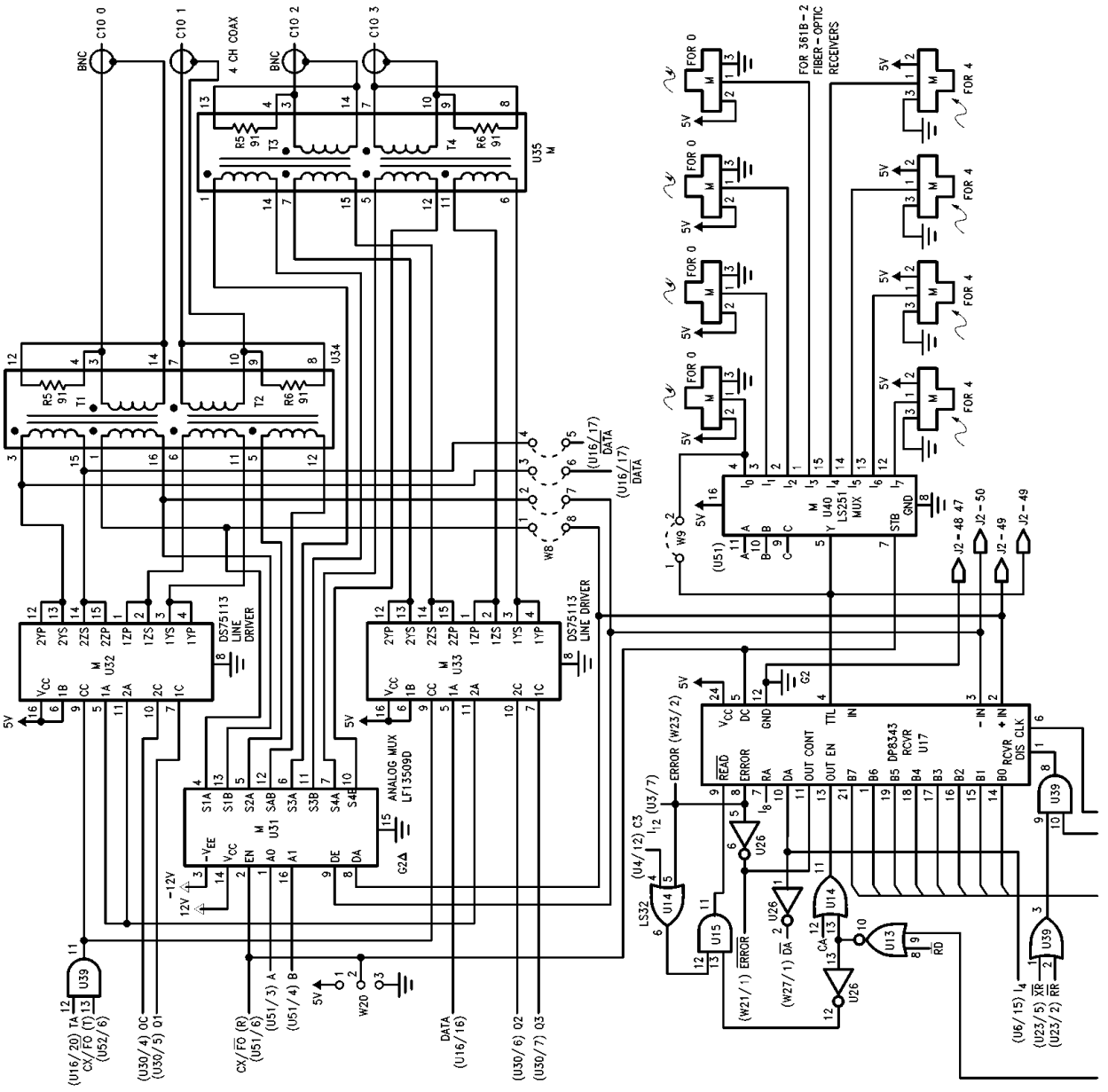

TL/F/9339–22
LS374 U4
LS374 U3
LS374 U5
MM2716 U2
MM2716 U1
LS151 U6
C1 DMAC (W21/5)
C2 LOAD (U13/12)
C3 READ (U14/4)
C4 RCVR OE (U14/13)
C5 MEM WE (U15/2)
C6 MEM OE (U15/4)
C7 BUS REQ (U24/36)
C8 CNT EN (U10/1) (U12/8)
I13 NOT USED
I12 ERROR (U17/8)
C9 AR (U16/21)
C10 ADCE (J2-37)
C11 NZ (W18/3)
C12 BUSY (W18/5)
ND5
W11
POLL (U23/33)
R19 10k
SYS CLK (U24/9)
(U37/19) P=Q I0
(U46/6) BACK I1
(U16/22) REG FULL I2
(U9/15) MAX CNT I3
(U17/10) DA I4
(U23/6) TO OUT I5
ND6
W17
(J2-35) LSTSL
R18 10k
R17 10k
(U23/2) RR I8
(U17/7) RA I9
(U23/5) XR I10

## THE BIPLAN DP8342/DP8343 BIPHASE LOCAL AREA NETWORK



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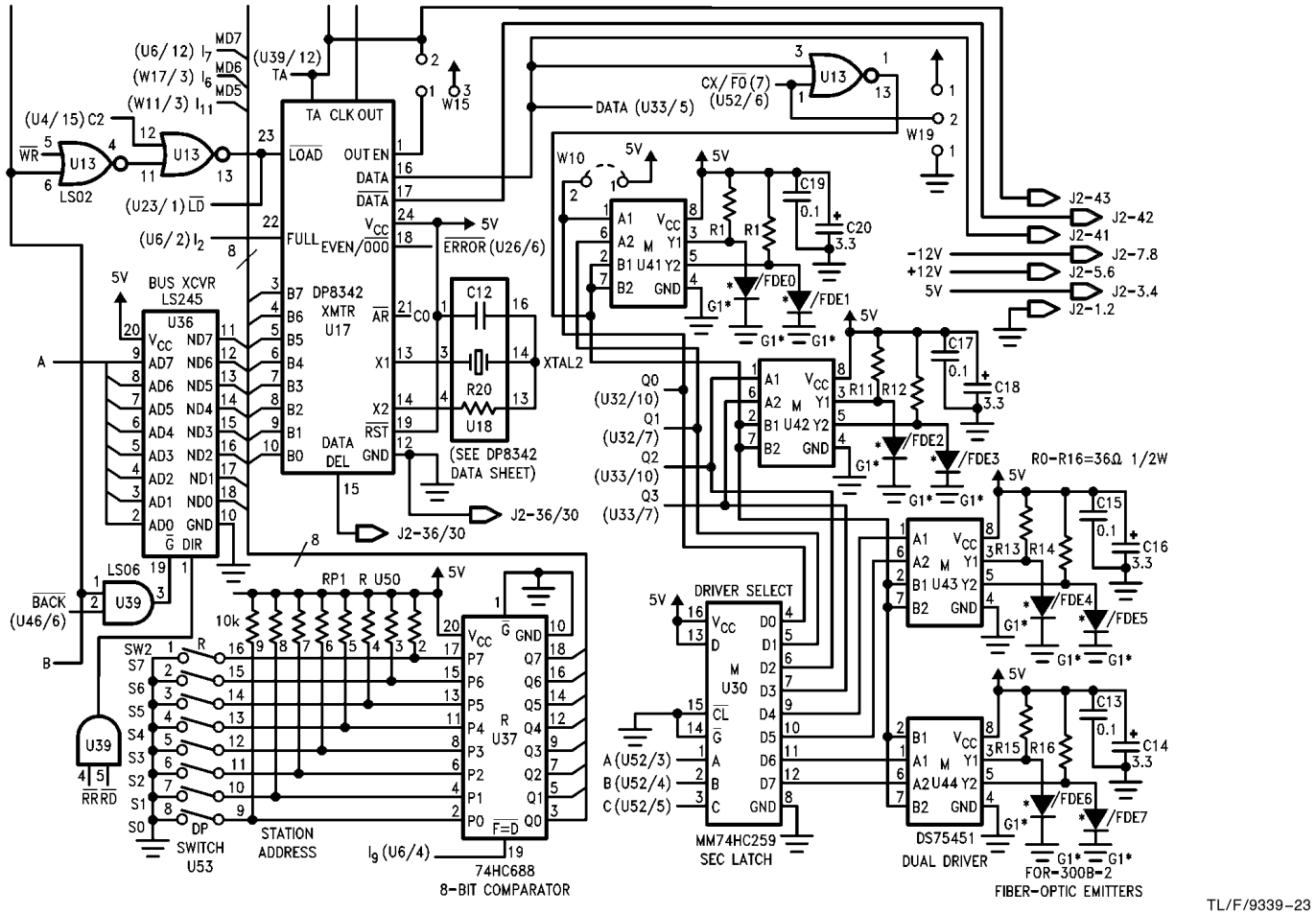


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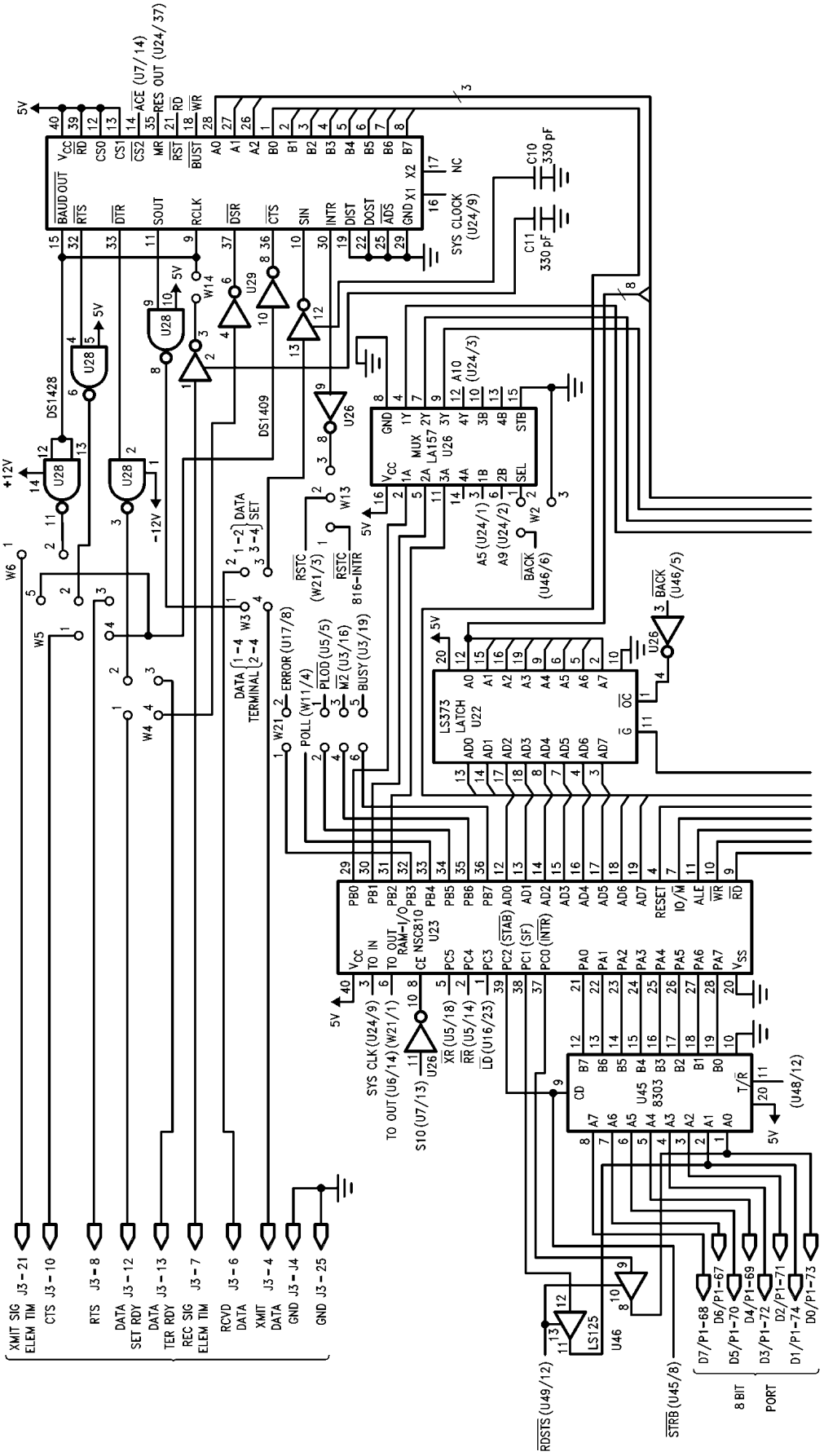
**Notes:**

*—01 IS A SEPARATE GROUND BUS FROM U41–U44 TO EDGE (P1)
**—V1 IS A SEPARATE $V_{CC}$ BUS FROM U41–U44 TO EDGE (P1)
Δ—G2 IS ANOTHER GROUND BUS FROM U31 AND U17 TO EDGE (P1)
M—FOR MASTER SYSTEM ONLY.
R—FOR RING SYSTEM ONLY.

**THE BIPLAN DP8342/DP8343 BIPHASE LOCAL AREA NETWORK**

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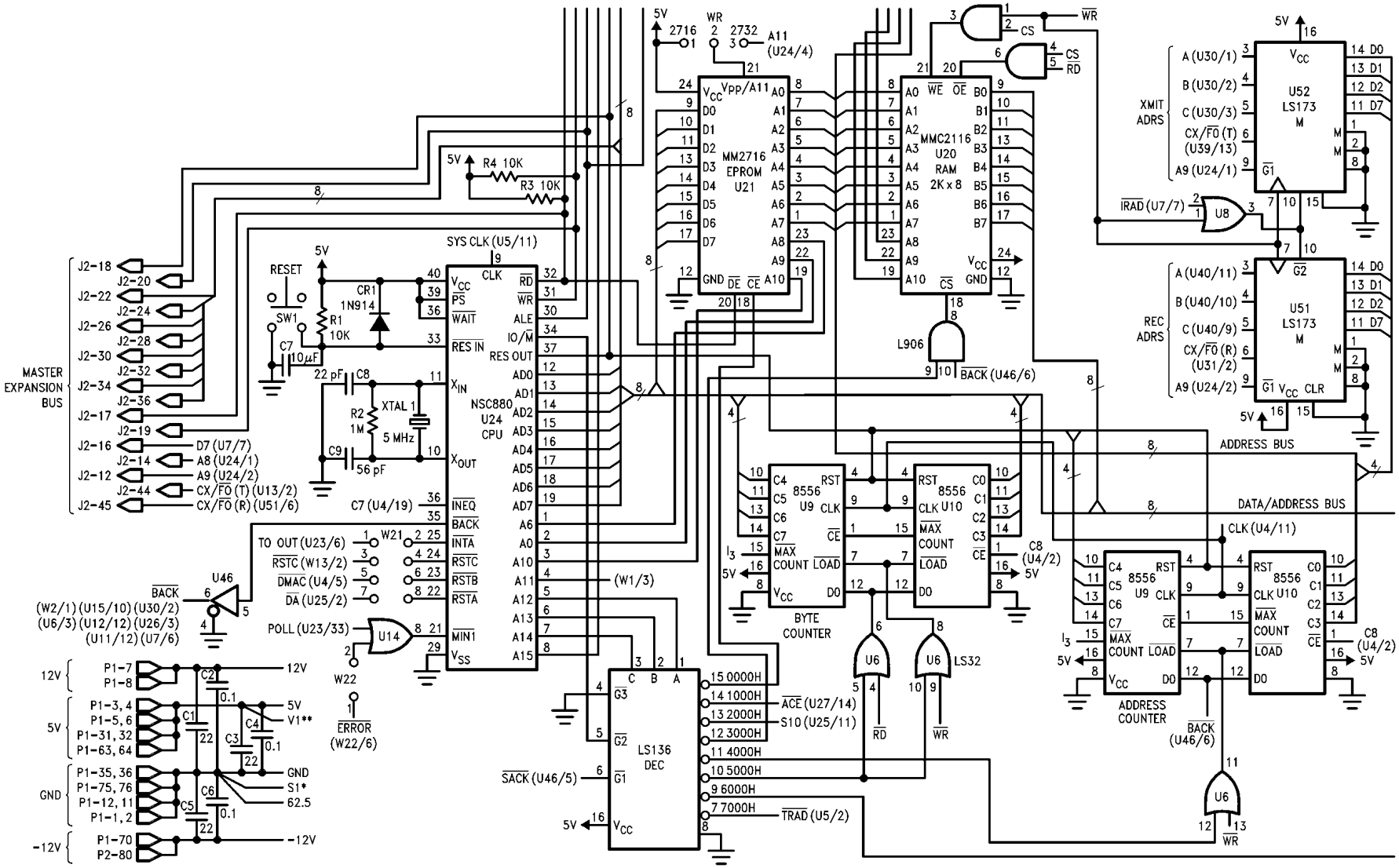


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**Notes:**

*—G1 IS A SEPARATE GROUND BUS FROM U41–U44 TO EDGE (P1)

**—V1 IS A SEPARATE $V_{CC}$ BUS FROM U41–U44 TO EDGE (P1)

Δ—G2 IS ANOTHER GROUND BUS FROM U31 AND U17 TO EDGE (P1)

M—FOR MASTER SYSTEM ONLY.

R—FOR RING SYSTEM ONLY.

**THE BIPLAN**
**Biphase Local Area Network**
**PARTS LIST**

| Device | Type | Device | Type |
|---|---|---|---|
| U1, U2 | MM2716Q | FOE 0–FOE 7 (M) | FOE–380B |
| U3, U4, U5 | DM74LS374 | FOR 0–FOR 7 (M) | FOR-361B |
| U6 | DM74LS151 | | |
| U7 | DM74LS138 | | |
| U8, U14 | DM74LS32 | R1, R3, R4, R17–R19 | 10K |
| U9–U12 | DM8556 | R2 | 1M |
| U13 | DM74LS02 | R5–R8 | 91 |
| U15, U39 | DM74LS08 | R9–R16 (M) | 36Ω ½W |
| U16 | DP8342 | R20 | 120 |
| U17 | DP8343 | RP1 (R) | 10K x 8 |
| U20 | NMC2116N-25L | | |
| U21 | MM2716/2732 | | |
| U22 | DM74LS373 | C1, C3, C5 | 22 μF, 20V |
| U23 | NSC810 | C13, C15, C17, C19 | 0.1 μF |
| U24 | NSC800 | C7 | 10 μF, 10V |
| U26 | DM74LS04 | C8 | 22 pF |
| U27 (S) | INS8250A | C9 | 56 pF |
| U28 (S) | DS1488 | C10, C11 | 330 pF |
| U29 (S) | DS1489 | C12 | 15 pF |
| U30 (M) | MM74HC259 | C14, C16, C18, C20 | 3.3 μf, 10V |
| U31 (M) | LF13509 | | |
| U32–U33 (M) | DS75113 | | |
| U36 | DM74LS245 | SW1 | Push Button SW |
| U37 (R) | MM74HC688 | SW2 | 8 Wide Dip SW |
| U38 | DM74LS157 | | |
| U40 (M) | DM74LS251 | XTAL1 | CPU OSC (5 MHz) |
| U41–U44 (M) | DS75451 | XTAL2 | *Bi-Phase OSC (287 MHz) |
| U45 (P) | DM8303 | | |
| U46 | DM74LS125 | T1–T4 | *Pulse Transformers |
| U47 (P) | DM8136 | | |
| U48 (P) | DM74LS00 | | |
| U49 (P) | DM74LS10 | | |
| U51, U52 (M) | DM74LS173 | | |

**Notes:**

(M)—Master Only

(R)—Ring Configuration Only

(S)—Serial (RS-232) Link to Host

(P)—8-Bit Parallel Link to Host

*(See DP8342 Data Sheet)

## DP8342/DP8343 HIGH SPEED INTERFACE FOR REMOTE DATA ACQUISITION
## CONTINUOUS CONVERSION AND TRANSMIT 16-CHANNEL UNIDIRECTIONAL A/D SYSTEM APPLICATION

** T1 and T2 pulse transformers Pulse Eng. 5762 or Technitrol 11LHA

**Note 1:** $V_{REF} = 5\ V_{DC}$ for this application.

**Note 2:** Crystal manufacturer Midland Ross Net Unit—See data sheet for spec.

**Note 3:** Optional $V_{REF}$ circuit.

**Note 4:** GND inputs of unused gates.

| | 5 $V_{DC}$ Pin | GND Pin |
|---|---|---|
| DP8342 | 24 | 12 |
| DP8343 | 24 | 12 |
| MM74C374 | 20 | 10 |
| DM74LS74 | 14 | 7 |
| MM74C00 | 14 | 7 |
| MM74C93 | 4 | 11 |
| DM74LS00 | 14 | 7 |
| MM74HC04 | 14 | 7 |

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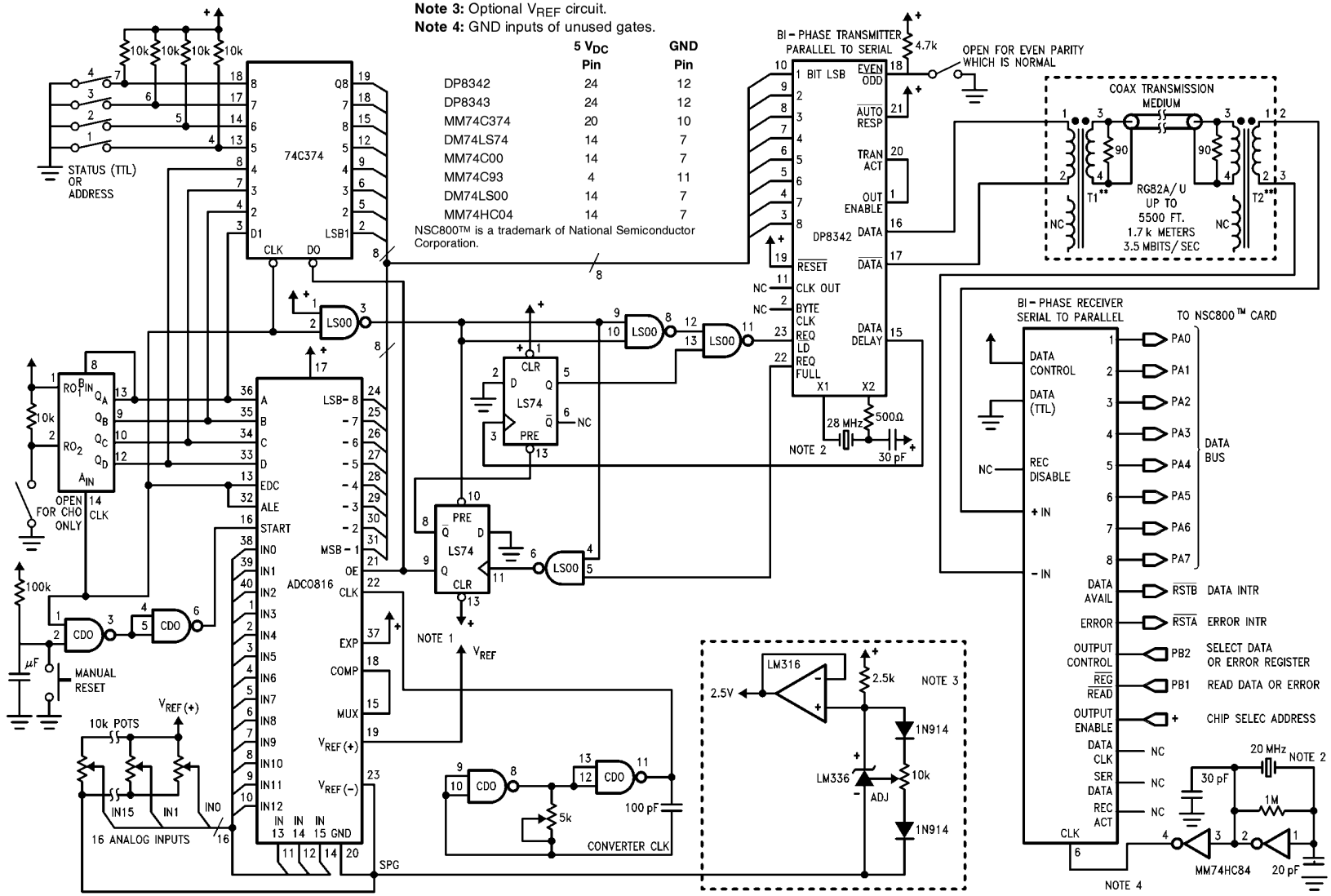


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