32-Bit Bus Master Ethernet Interface for the 68030 (Using the Macintosh SE/30)

National Semiconductor
Application Note 691
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OVERVIEW

National Semiconductor's SE/30 Ethernet adapter provides a high performance, 32-bit, bus master network connection for Apple's 68030 based compact Macintosh computer. This design is based around National Semiconductor's Systems Oriented Network Interface Controller (SONIC™, DP83932), which interfaces directly to the extension slot of the SE/30. The SE/30 design also serves as a model for designing the SONIC onto the mother board of a 68030 based system, since the SE/30's one expansion slot is essentially a direct connection to the Motorola 68030.

A block diagram of the adapter can be seen in *Figure 1*. The SE/30 Ethernet adapter operates synchronously with the 16 MHz SE/30 mother board and accesses the necessary transmit and receive buffers directly in the system's main memory, via 16 MHz 3 cycle asynchronous DMA operations. At this rate, the bus utilization for the buffering of a single packet is approximately 6% of the total bus bandwidth.

In addition to it's high performance DMA, the SONIC also has an on board Ethernet Manchester Encoder/Decoder (ENDEC), which allows the SONIC to communicate directly with any AUI interface. In fact, the SE/30 board has the capability to be connected to a network through either thin wire (10Base2) or AUI drop cable (10Base5) Ethernet.

It is also worth mentioning that the SE/30 adapter supports the use of Macintosh Nubus Slot Manager features, such as interrupt handling, with an on board Slot Manager PROM. This does not cause the board to incur any extra cost, since some type of PROM must already be used to store the adapter's Ethernet address.

FEATURES

- 32-bit bus master system interface
- Asynchronous high speed 3 cycle DMA
- 100% on card address filtering, via the SONIC's on board Content Addressable Memory (CAM)
- Minimal number of components
- Supports both AUI cable and thin wire Ethernet
- Optimal placement of receive and transmit data and descriptors in system memory
- Supports Macintosh Slot Manager
- Portable to 68030 mother board designs

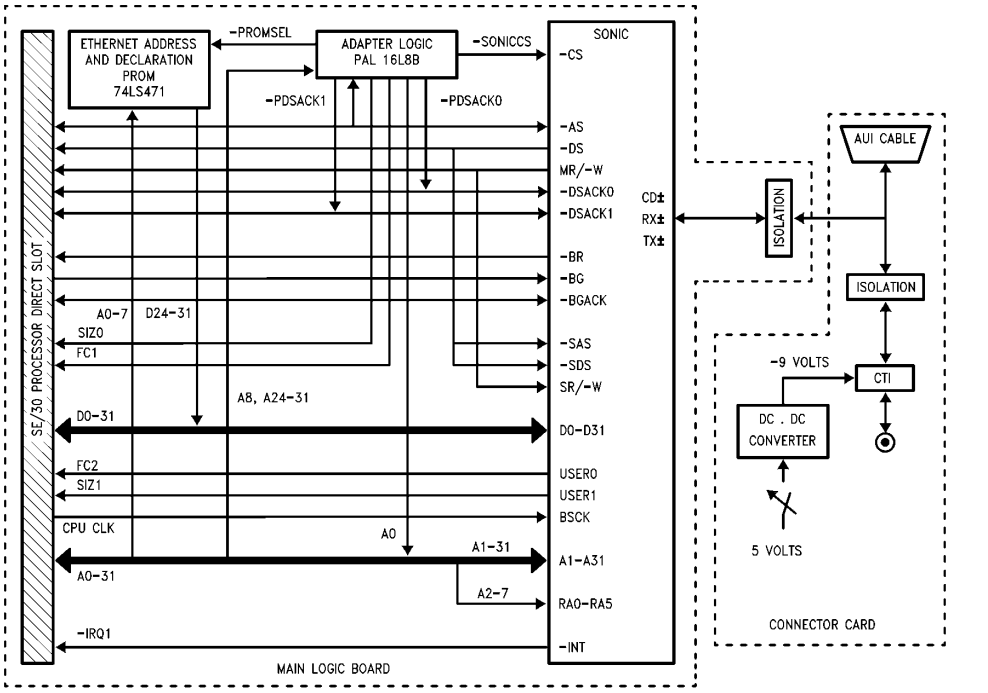

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FIGURE 1. Adapter Block Diagram

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FUNCTIONAL OVERVIEW

System Interface

The Macintosh SE/30 provides a single 32-bit expansion slot, which basically consists of the control, data, and address signals of the mother board's CPU, the 68030. In addition to these signals, the expansion slot also provides Nubus compatible interrupt lines, so that Slot Manager software can be incorporated, if a Slot Manager PROM is placed on the card. Hence, the hardware interface between the SE/30 and the Ethernet adapter is essentially a 68030 bus interface, while the driver software interface is similar to that of a Macintosh II Nubus adapter. This solution is optimally achieved through the use of National Semiconductor's SONIC, whose 32-bit data and address buses and control signals interface directly to those of the Motorola 68030.

The SE/30 Ethernet adapter operates in both a slave and master mode. When operating in a bus master mode, the SE/30 Ethernet adapter arbitrates with the host system for control of the SE/30 bus and proceeds to operate as a 32-bit DMA engine between the system memory and the network. A block diagram of this interface can be found in *Figure 1*. The bus master mode of operation allows for the use of system memory, instead of on card RAM, for the buffering of transmit and receive data and their descriptors. Master operation is facilitated by the SONIC, which is at the heart of this adapter's design. The SONIC provides the complete implementation of the IEEE 802.3 specification from the AUI interface through the MAC layer, as well as performs a direct system interface to the 68030. In fact, when interfacing to the SE/30 backplane, the SONIC carries out 16 MHz 3 cycle asynchronous DMA, which is fully synchronous with the 16 MHz mother board of the SE/30. This enables the SE/30 adapter to operate on the bus in the same fashion as the 68030 and utilize only 6% of the bus bandwidth, during an Ethernet reception or transmission. The bus master design provides for the highest possible throughput between the system and the network, while at the same time requiring only a minimum of parts to implement.

When the adapter is a slave, the host system accesses either the Slot Manager PROM or the SONIC's registers. All slave operations are done via memory reads and writes, since both the PROM and the SONIC registers are mapped into system memory. The slave architecture is depicted in the adapter block diagram *(Figure 1)*. While in the slave mode, the SONIC once again provides a direct interface to the SE/30. The only necessary interface logic is the address decode for the SONIC chip select (-SONICCS). At this point, it is worth noting that the slave address strobe (-SAS) of the SONIC is connected to the data strobe (-DS) of the SE/30 instead of the SE/30's address strobe (-AS). This is due to the operation of the SE/30 backplane and will be further discussed in the design section of this document. However, it is important to remember that in interfacing directly to a 68030 CPU the SONIC's -SAS would be connected directly to the 68030's -AS.

Network Interface

With respect to the adapter's physical layer design, both AUI drop cable Ethernet and thin wire Ethernet are supported. The SE/30 adapter consists of two boards, the main logic board, which contains the SONIC, and the connector card which provides for the AUI and thin wire network connections. The connector card, whose block diagram is shown in *Figure 2*, contains a 15-pin AUI drop cable connector for standard drop cable Ethernet implementations, as well as a thin wire Ethernet connection via the National Semiconductor coaxial transceiver interface (CTI, DP8392).

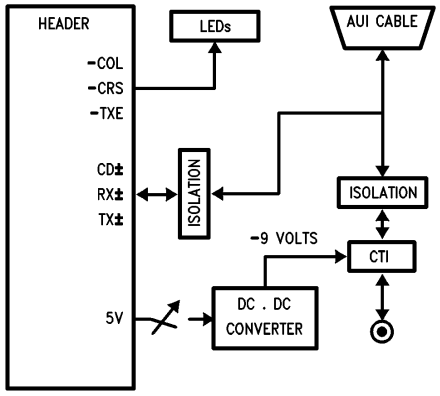

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FIGURE 2. Connector Card Block Diagram

Either of these network connections can be chosen through the use of a single jumper. In either case, the AUI signals (RX±, TX±, and CD±) are sent back to the main logic board, where the SONIC resides. These signals are interfaced to the ENDEC portion of the SONIC, which provides for communication between the AUI interface and the non-return to zero (NRZ) signals (RXD, TXD, and COL) of the Media Access Control (MAC) module of the SONIC. It should be noted that the integrated ENDEC module of the SONIC alleviates the need for an external Ethernet Manchester encoder/docoder, such as National's CMOS Serial Network Interface (CMOS SNI, DP83910).

BOARD ARCHITECTURE AND DESIGN

Memory Map

As stated previously, the SE/30 adapter is completely mapped into the addressable memory space of the SE/30. A diagram of the memory map can be found in *Figure 3*. The board is mapped into the memory locations F9FFFFFF through F9000000. Locations F9FFFFFF through F9FFFF00 contain the Ethernet address and declaration PROM. This region contains the adapter's Ethernet address as well as the declaration data that is necessary for the adapter's interrupt service routine to take advantage of the Slot Manager features, which are provided by the SE/30 operating system.

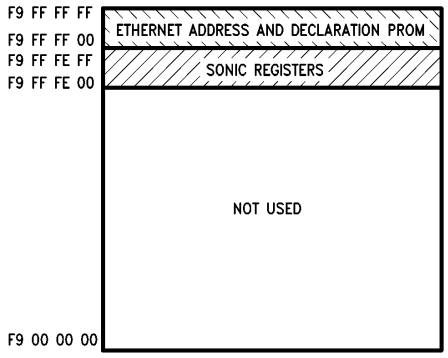

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FIGURE 3. SE/30 Adapter's Memory Map

The SE/30 specification states that this declaration data begin at memory location F9FFFFFF, if the adapter's interrupt is generated on the system's IRQ 1 interrupt line. This is the case with the SE/30 adapter. The six byte Ethernet address immediately follows the Slot Manager software in the PROM. It should be noted that the data in the PROM is all byte addressable. In addition to the declaration information, the SONIC registers are also mapped into memory. These registers are mapped into locations F9FFFFE0 through F9FFFEFF. The SONIC's registers are mapped as 32-bit addressable quantities, in spite of the fact that internally all SONIC registers are only 16 bits wide. This is due to the fact that the SONIC will always respond as a 32-bit port, since it is programmed to operate in 32-bit mode.

Slave Operation

When operating as a slave, the Ethernet adapter appears as a block of memory to the host system. In slave mode, either the SONIC or PROM can be accessed. Timing diagrams for slave accesses appear in *Figures 4–6*. In the case of accessing the PROM *(Figure 4)*, the 68030 will issue a byte read command. The adapter logic will decode address lines 8 and 24 through 31 and recognize the fact that the SE/30 adapter's PROM is being selected. Once the 68030 asserts its address strobe, the logic will issue an enable signal to the PROM (-PROMSEL) and assert the cycle acknowledge signals (-PDSACK0 and -PDSACK1) back to the 68030, in order to indicate the adapter's acknowledgement of a byte access. In parallel with the logic's operation, the PROM will decode the address it is being given (A0–A7) and begin to source data after receiving the -PROMSEL signal. Finally, the 68030 will then finish the read cycle, at which point the adapter logic will then deassert -PROMSEL, -PDSACK0, and -PDSACK1.

As seen in *Figures 5* and *6*, slave accesses to the SONIC are completely compatible with the bus of the 68030 processor. The only deviation is the connection of -SAS to the 68030's -DS instead of -AS. This is due to the fact that during slave writes a glitch may occur on the memory read/write line (MR/-W) of the SE/30 backplane, while -AS is being asserted. This is fatal, since the SONIC latches the value of the slave read/write line (SR/-W, which is connected to MR/-W) with the falling edge of -SAS. The connection of the 68030's -DS to -SAS solves this problem. It should also be noted that the SONIC is mapped into memory as a 32-bit peripheral and will respond accordingly. However, only the lower 16 data lines (D0–D15) will be valid inputs and outputs during slave accesses.

A 32-bit mapping was selected, since the SONIC is programmed to operate in 32-bit mode, which causes the SONIC to respond with the acknowledge signals of a 32-bit port (-DSACK0 = 0 and -DSACK1 = 0). The only adapter logic necessary to facilitate this interface is the decode of address lines 8 and 24 through 31, along with the address strobe (-AS), to generate a chip select signal to the SONIC (-SONICCS). When accessing the SONIC registers, the 68030 will perform either a 32-bit read or a 32-bit write. Once -SONICCS is asserted the SONIC will respond with the acknowledge signals (-DSACK0 and -DSACK1) and appropriately source or sink data. The deassertion of -DS by the 68030 signals the end of the cycle and causes the SONIC to deassert -DSACK0 and -DSACK1 and terminate the slave cycle.

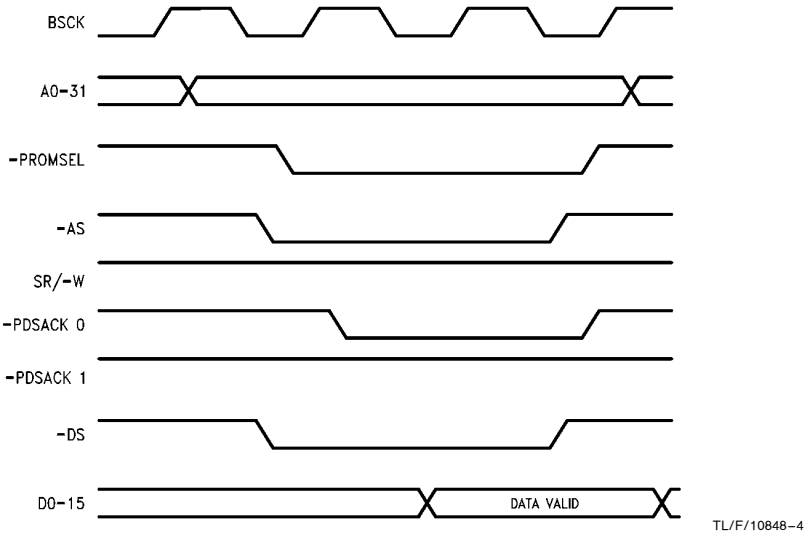

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FIGURE 4. PROM Read

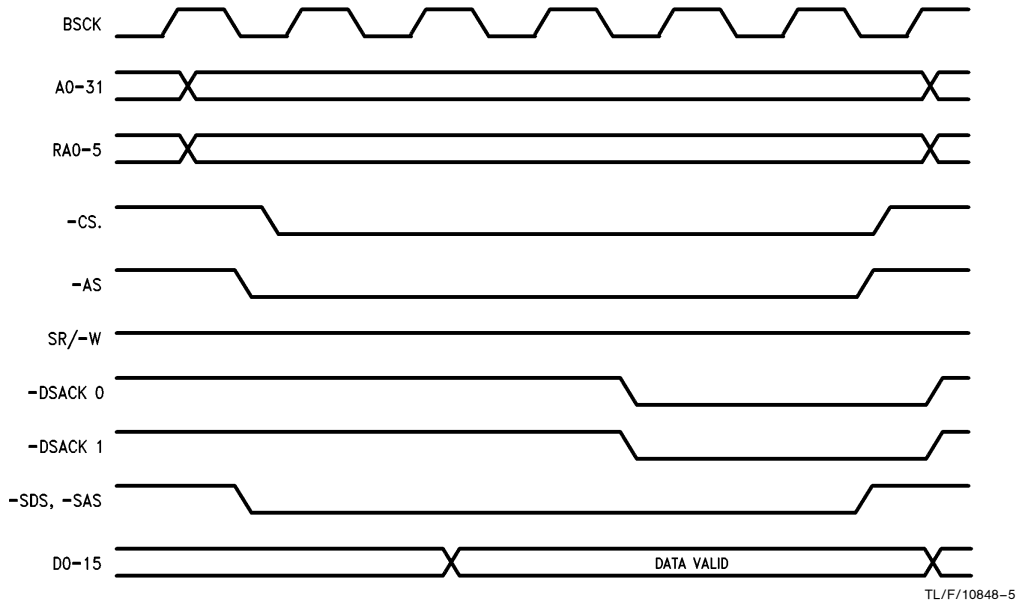

FIGURE 5. SONIC Slave Read

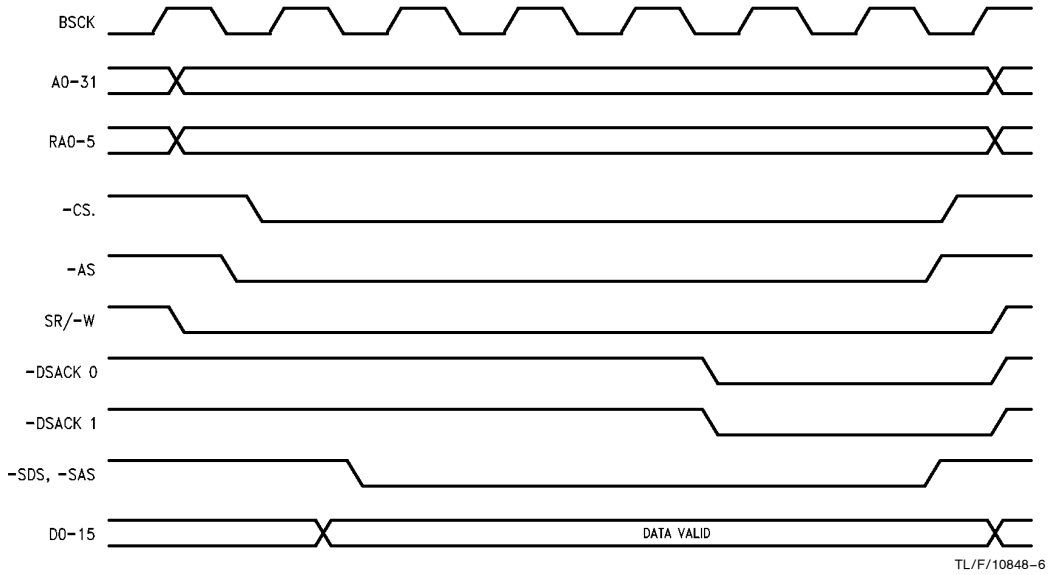

FIGURE 6. SONIC Slave Write

Master Operation

As stated previously, the SE/30 Ethernet adapter contains no local memory. All Ethernet data and descriptors are stored in system memory, which is accessed directly by the adapter. More specifically, the system memory is accessed directly by the SONIC, which interfaces directly to the 68030 mother board bus of the SE/30. When a master DMA access is required, the SE/30 adapter will arbitrate for the SE/30 system bus. This arbitration is performed by the SONIC, which connects directly to the bus arbitration signals of the 68030. This is depicted in the adapter block diagram *(Figure 1)*. A timing diagram of the arbitration cycle can be found in *Figure 7*. When the SONIC initiates a request for the system bus, it asserts the bus request signal (-BR) and waits for the bus grant signal (-BG) to be returned by the system. Once the bus grant signal is received, the SONIC will take ownership of the bus by asserting the open collector bus grant acknowledge signal (-BGACK), when the host system's -AS, -DSACK0, -DSACK1, and -BGACK are all deasserted. Once -BGACK is asserted, the SONIC removes the bus request signal.

After acquiring the bus the SE/30 adapter will begin to perform 16 MHz 3 cycle asynchronous DMA on the system bus. This function is also facilitated by the SONIC, whose direct 68030 interface allows the SE/30 adapter to operate on this bus with virtually no interface logic. As seen in *Figure 1*, the bus interface signals on the SONIC are attached directly to those of the SE/30 backplane.

Timing diagrams of the adapter's master read and master write cycles appear in *Figures 8* and *9*. The only external interface logic required is for the generation of Function Code bit 1 (FC1), SIZ0, and address line 0 (A0). These lines are not provided directly by the SONIC, but are formulated in the adapter logic. All three signals are driven low upon the SONIC's assertion of -BGACK. It should also be noted that Function Code bits 0 and 2 (FC0 and FC2) and the SIZ1 signal are also not provided directly by the SONIC. However, these signals require no extra logic. The FC0 signal is tied high through a backplane resistor and requires no board connection, since the SONIC should only access memory areas which correspond to function codes with the least significant bit set high. These areas are user data space (FC2, FC1, FC0 = 001) and supervisor data space (FC2, FC1, FC0 = 101).

The FC2 and SIZ1 signals are not defined on the SONIC, but they can be generated by using the user 0 and user 1 pins. The user 0 and 1 outputs can be programmed by the programmable output bits (PO0 and PO1) in the SONIC's data configuration register (DCR). The output timing for these signals corresponds to the timing for the SONIC's address lines, which is the correct timing for both FC2 and SIZ1. By programming PO0 with a 0 or 1, the adapter can be made to access either the user data space or supervisor data space of the SE/30's system memory. In order to provide the correct SIZ1 signal for 32-bit operation the PO1 bit should be programmed to a 0.

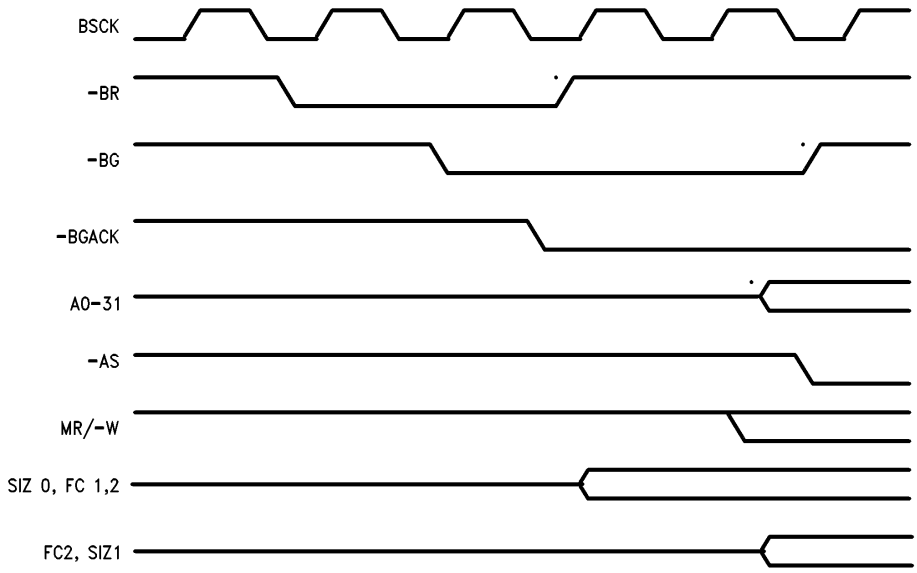

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FIGURE 7. SONIC Master Arbitration

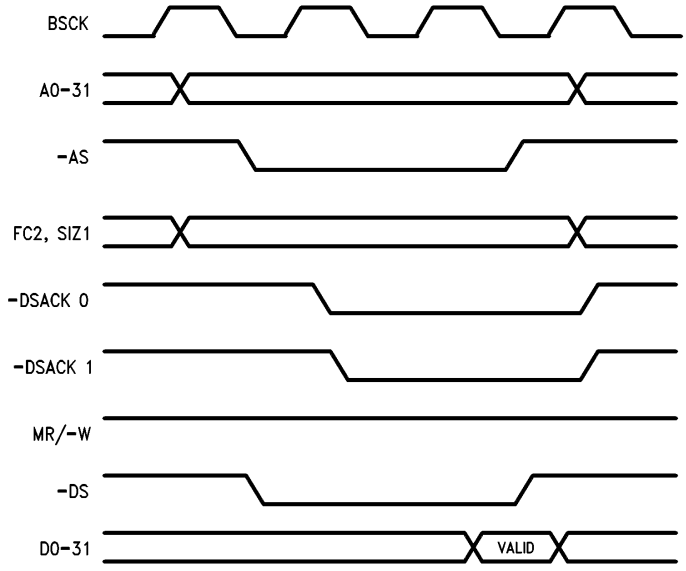

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FIGURE 8. Master Read

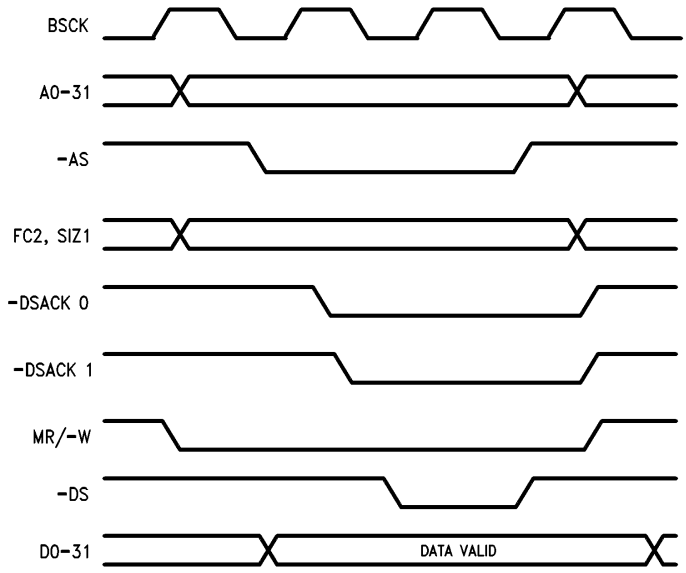

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FIGURE 9. Master Write

Physical Layer

The physical layer interface for the SE/30 adapter resides on the connector card, which attaches to the back of the SE/30. The connector board is linked to the main logic board through a ribbon cable that attaches to a 20-pin header on the main logic board (J2) and another 20-pin header on the connector board (J3). These two headers can be seen on the adapter schematics, which appear at the end of the manual of this application note. The adapter can be used in either a thin wire or standard drop cable Ethernet environment. When the adapter is used in a thin wire Ethernet application, jumper 3 (JB3) must have the jumper covering both posts. This enables the DC-to-DC converter to receive a 5V input from the SE/30 backplane and convert this to a −9V output, which is required by National Semiconductor's Coaxial Transceiver Interface (CTI, DP8392). The CTI provides an interface between the 10 MHz Manchester encoded coax cable and the 10 MHz Manchester encoded differential signals of the SONIC's ENDEC. In the case of a standard drop cable Ethernet application, JB3 is left uncovered so that the CTI will not receive power. This allows the signals of the SONIC's ENDEC to pass directly to the AUI cable, via the 15-pin AUI connector. In examining the schematic of the physical layer design, it can be seen that there is a pulse transformer at the AUI side of the CTI. This is placed here to isolate the CTI from the SONIC's ENDEC signals, when the AUI drop cable connection is being employed. This transformer also provides the IEEE 802.3 specified isolation between the coax and the differential AUI signals, when thin wire Ethernet is being used. It is also necessary to provide a termination for the 78Ω AUI cable's differential receive and collision pair (RX± and CD±). This is the reason for the 39Ω -1% resistors and 0.01 μF capacitors that are shown in the schematic.

Since the ENDEC resides within the SONIC, two components of the physical layer design are located on the main logic board, which can be seen on the schematics. First, each one of the transmit pairs (TX+ and TX−) requires a 270Ω non-precision pull down resistor (R1 and R2) to complete the internal source follower amplifiers that drive these signals. Second, there is an isolation transformer (T1) placed between the differential signals of the SONIC's ENDEC and the header for the ribbon cable. This isolation is necessary to guarantee that the SONIC meets the IEEE 802.3 fail safe specification of a 16V DC level appearing on the AUI cable's differential signals. The external isolation is necessary, due to the fact that in the powered down state the CMOS process, in which the SONIC is manufactured, may not be able to withstand this voltage.

The final feature of the physical layer design is the diagnostic LEDs. The yellow LED indicates that the ENDEC carrier sense signal (CRS) is asserted. An inverted version of CRS drives this LED. The green LED indicates that a transmission is in progress, and the red LED indicates the presence of a collision. The transmission LED and collision LED are driven by inversions of the SONIC's transmit enable (TXE) and collision output (COL) signals, respectively. The signals for the LEDs are supplied from the main logic board, via the ribbon cable that connects the two boards.

ADAPTER LOGIC EQUATIONS

The following is the set of logic equations that are necessary to implement the adapter logic block found in *Figure 1*. As shown in the schematics, this logic can be implemented in a single 16L8B PAL.

Inputs

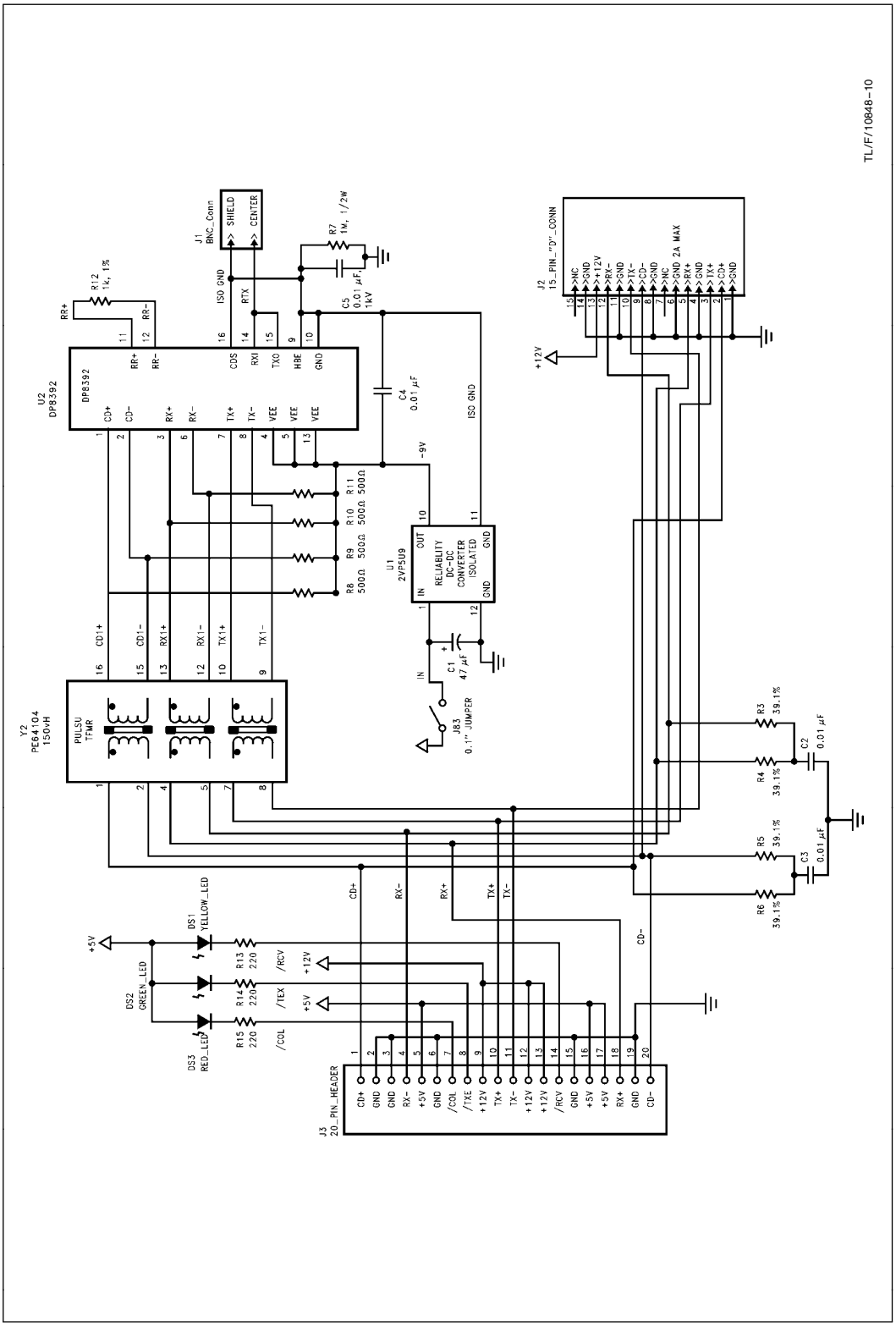
A31, A30, A29	Pin	1, 2, 3
A28, A27, A26	Pin	4, 5, 6
A25, A24, A8	Pin	7, 8, 9
AS, BGACK	Pin	11, 13

Outputs

A0	Pin	12; Address line 0 (TRI-STATE)
SIZ0	Pin	14; 68030 SIZ0 signal (TRI-STATE)
FC1	Pin	15; 68030 Function Code 1 signal (TRI-STATE)
PDSACK1	Pin	16; PROM cycle acknowledgement (TRI-STATE)
PDSACK0	Pin	17; PROM cycle acknowledgement (TRI-STATE)
-PROMSEL	Pin	18; PROM chip select
-SONICCS	Pin	19; SONIC chip select

Equation:

A0 = 0
SIZ0 = 0
FC1 = 0
PDSACK0 = 0
PDSACK1 = 1
ENABLE A0 = -BGACK
ENABLE SIZ0 = -BGACK
ENABLE FC1 = -BGACK
ENABLE PDSACK0 = A31*A30*A29*A28*A27*-A26*-A25*A24*A8*-AS
ENABLE PDSACK1 = A31*A30*A29*A28*A27*-A26*-A25*A24*A8*-AS
SONICCS = A31*A30*A29*A28*A27*-A26*-A25*A24*-A8*-AS
PROMSEL = A31*A30*A29*A28*A27*-A26*-A25*A24*A8*-AS


TL/F/10848–10
J1
BNC_Conn
>> SHIELD
>> CENTER
ISO GND
R7
1M, 1/2W
C5
0.01 µF
1kV
R12
1k, 1%
RR+
RR–
U2
DP8392
CD+
CD–
RX+
RX–
TX+
TX–
VEE
CDS
RXI
TXO
HBE
GND
C4
0.01 µF
–9V
ISO GND
R8
500Ω
R9
500Ω
R10
500Ω
R11
500Ω
U1
2VP5U9
RELIABILITY
DC-DC
CONVERTER
ISOLATED
IN
OUT
GND
C1
47 µF
J3
0.1" JUMPER
Y2
PE64104
1500VH
PULSU
TFMR
CD1+
CD1–
RX1+
RX1–
TX1+
TX1–
J2
15_PIN_"D"_CONN
>NC
>GND
>+12V
>RX–
>GND
>TX–
>CD–
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>NC
>GND 2A MAX
>RX+
>GND
>TX+
>CD+
>GND
+12V
R3
39.1%
R4
39.1%
R5
39.1%
R6
39.1%
C2
0.01 µF
C3
0.01 µF
+5V
DS1
YELLOW_LED
DS2
GREEN_LED
DS3
RED_LED
R13
220
R14
220
R15
220
/RCV
/TEX
/COL
J3
20_PIN_HEADER
CD+
GND
GND
RX–
+5V
GND
/COL
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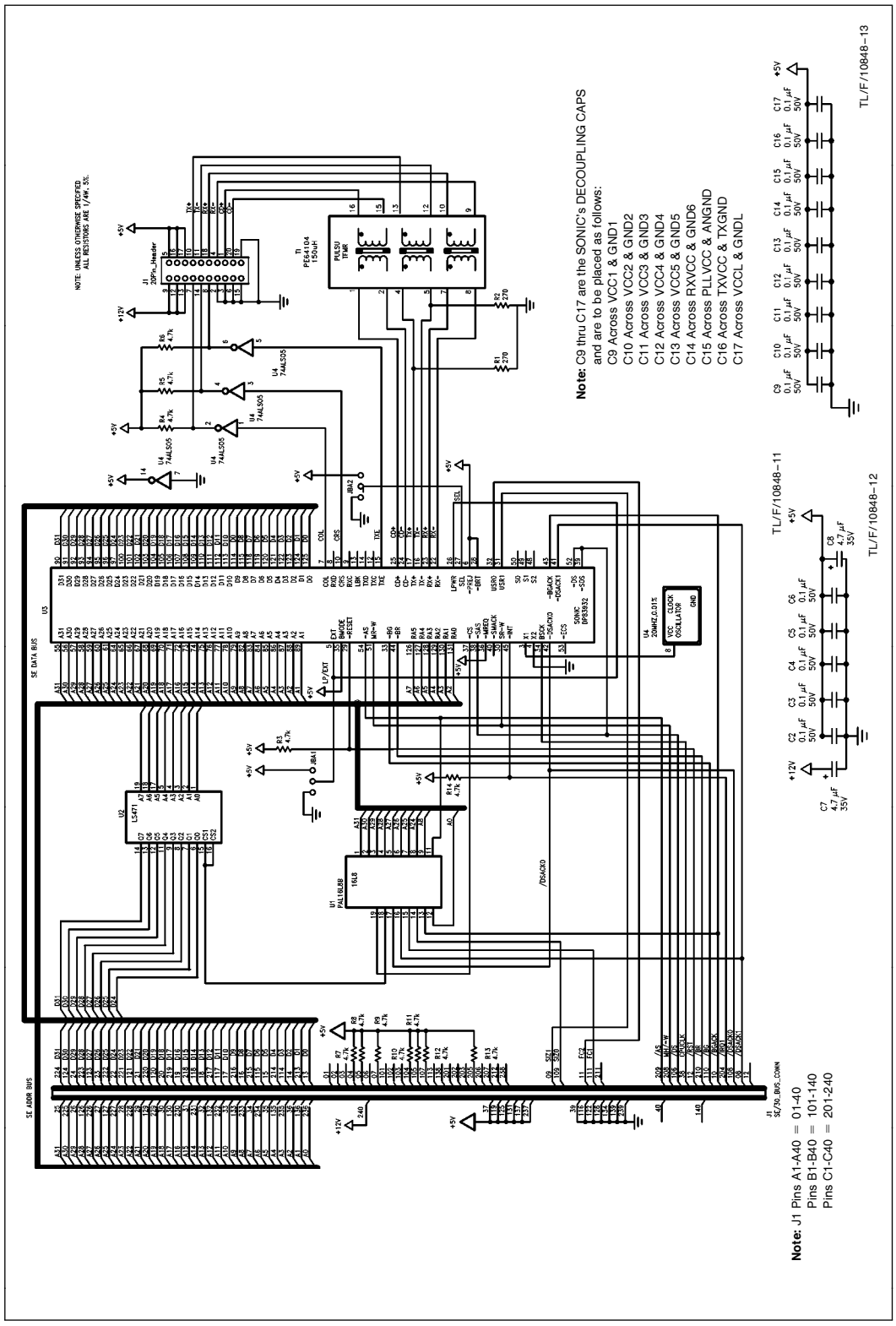
GND
+5V
+5V
RX+
GND
CD–


Note: C9 thru C17 are the SONIC's DECOUPLING CAPS and are to be placed as follows:
C9 Across VCC1 & GND1
C10 Across VCC2 & GND2
C11 Across VCC3 & GND3
C12 Across VCC4 & GND4
C13 Across VCC5 & GND5
C14 Across RXVCC & GND6
C15 Across PLLVCC & ANGND
C16 Across TXVCC & TXGND
C17 Across VCCL & GNDL
Note: J1 Pins A1-A40 = 01-40
Pins B1-B40 = 101-140
Pins C1-C40 = 201-240
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TL/F/10848–12
TL/F/10848–13

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