DP83932EB-EISA SONIC™ EISA Bus Master Ethernet Adapter

National Semiconductor
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INTRODUCTION

The purpose of this application note is to describe the implementation of an EISA bus master Ethernet interface solution using National Semiconductor's DP83932 System Oriented Network Interface Controller (SONIC™) and PLX Technology's EISA9032 EISA Bus Master Interface chip.

This solution takes the form of a high performance 32-bit network interface adapter card which on one side plugs into an EISA bus slot and on the other supports two media connection options, Attachment Unit Interface (AUI) and Thin wire Ethernet.

The board easily interfaces to the EISA bus with few external components. This application note assumes the reader is familiar with National Semiconductor's DP83932 SONIC™ Ethernet controller, PLX Technology's EISA9032 EISA interface chip and the EISA bus specification.

This document will first give a hardware functional description of the card, followed by an overview of EISA covering topics such as system configuration, I/O access, multiple bus masters and bus protocol, and ending with a description of the master and slave interfaces of the Ethernet board.

HARDWARE FUNCTIONAL OVERVIEW

The main function of this adapter card is to transfer Ethernet packet data to/from the CPU's system memory as a high speed 32-bit bus master during LAN transmissions and receptions at the maximum EISA burst rate of 33 Mbytes/s.

A 32-bit bus master architecture, in which the SONIC Ethernet controller can gain ownership of the EISA bus and transfer data directly into system memory with no on-board CPU or buffer RAM has been chosen for this design to maximize data throughput while not adding any extra memory cost or intelligence on the card. In addition the inherent packet buffer management features of SONIC are utilized by driver software to facilitate optimum performance. The card has a typical (calculated) bus occupancy of $\leq$10% for full Ethernet traffic (10 Mb/s).

The block diagram of this board is shown in *Figure 1.* The design can be broken down into 3 sections: slave interface, bus master interface, and physical media interface.

The slave interface enables the EISA host CPU to gain access to the following devices on the adapter card:

1. 32 x 8 PROM which contains the card's Ethernet node ID, and the card's EISA ID.
2. An optional 256k x 8 boot EPROM which can contain a program which enables a diskless CPU to boot up across the network.
3. The SONIC Ethernet controller internal registers.
4. The EISA9032 EISA interface chip configuration registers.

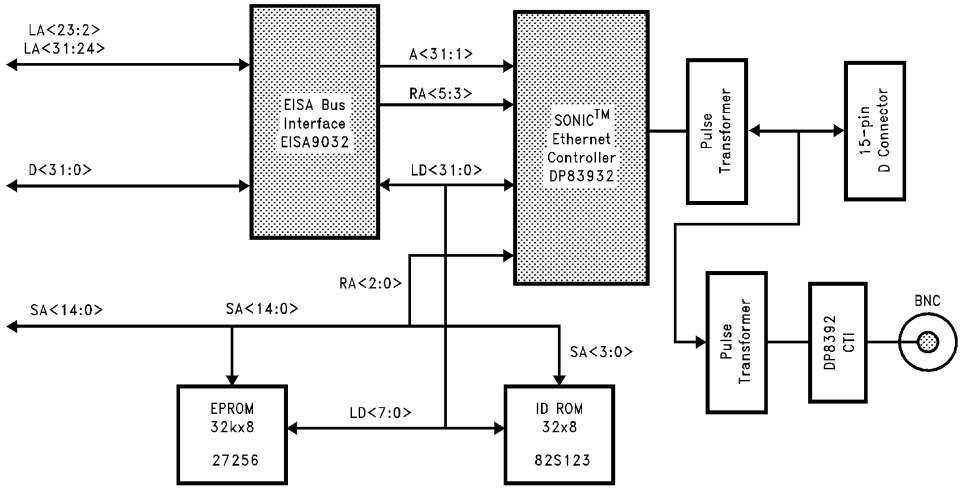

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FIGURE 1. SONIC EISA Ethernet Adapter Card Block Diagram

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The master interface enables the SONIC Ethernet controller to read and write to the system memory on the EISA bus using the EISA9032 interface chip. The EISA9032 interface chip converts the Ethernet controller's arbitration and cycle control signals to the EISA bus timing and protocol.

The physical interface enables the SONIC Ethernet controller to transmit and receive data over a 10BASE5 thick wire Ethernet interface or the 10BASE2 thin wire interface using National Semiconductor DP8392 Coaxial Interface Transceiver CTI.

Transmission

The sequence of events for Ethernet transmissions is as follows:

The host CPU writes the packet data into the system's memory Transmit Buffer Area (TBA). It then writes descriptor information (packet data pointers, packet size, etc.) into the system memory transmit descriptor area (TDA). Next it loads a SONIC register with a pointer to the TDA and issues a transmit command by writing to the SONIC's command register.

The SONIC responds by first reading the TDA descriptor information from system memory. It then loads the packet data from the system memory TBA into its internal FIFO in bursts and transmits this data onto the network. At the end of the transmission the SONIC will write transmit status information into the system's memory TDA.

Reception

The sequence of events for Ethernet receptions is as follows:

Data is loaded from the Ethernet cable into the SONIC's internal FIFO. When a programmable threshold is reached in the FIFO, the SONIC will write the packet data into the system memory's Receive Buffer Area (RBA).

Once a complete packet has been loaded into memory the SONIC will write descriptor information about the reception into the system memory's Receive Descriptor Area (RDA).

Note that all buffer and descriptor areas are set up by the host CPU in system memory prior to any packet transmission and reception.

EISA OVERVIEW

EISA was developed in 1989 by a consortium of 9 PC manufacturers in an attempt to create a higher performance 32-bit bus architecture that is backwards compatible with the PC-AT® based industry Standard Architecture (ISA) created in 1984.

This section gives an overview of the Extended Industry Standard Architecture EISA and describes the Ethernet adapter's implementation of its interface. First, the bus features are described, then various facets of bus operation are described, including addressing, arbitration, configuration, and the bus protocol.

Bus Features

- 64 kBytes of I/O space; Slot specific I/O access
- 32-bit non multiplexed address data bus supporting a 4 GByte address range
- Multiple bus masters using a centralized arbitration scheme supporting preemption
- Synchronous protocol (8.3 MHz clock) supporting standard (2 bus clock per cycle) or burst (1 bus clock per cycle) mode which can achieve a data transfer rate of 33 MB/s
- Cycle translation performed by the system board enables a 32-bit or 16-bit EISA or ISA master to interface with any one of 5 different slaves (EISA 32/16 burst/16 non burst, ISA 16/8 bit)
- Shareable interrupts; Programmable level or edge trigger
- Automatic configuration by means of an on-board product identification ROM. Manufacturers provide a configuration file to be used at system configuration time to assign system resources.

I/O ACCESSES AND ADDRESSING

EISA supports slot specific I/O access. Since EISA is backwards compatible with ISA addressing, how EISA partitions address space is relatively complex. Next follows a description of how addressing is implemented and how backwards compatibility with ISA limits each EISA slot I/O space to 1 kByte.

EISA supports 16-bit wide I/O addresses providing a total I/O address range of 64k. This is divided into 16 slots, each having 4k allocated to them. This is shown in *Figure 2.*

The top 4 bits of the address LA15:12 define the slot number and the remaining 12 bits LA11:0 provide a 4k address range per slot.

To provide backwards compatibility with ISA, some of this address range must be lost. This is because ISA supports 10-bit wide I/O addresses, resulting in a total I/O space range of 1 kByte. The first 256 bytes (000H–0FFH) of this 1k is allocated to the system board, and the remaining 768 bytes (100H–3FFH) can be used by ISA expansion boards.

This means ISA expansion boards only need to decode addresses 9–0 and therefore will recognize the address range 100H–3FFH (256 to 1k) in every 1k block of the 64k EISA I/O space. That is, all addresses in the top 768 bytes of every 1k block are aliased to the ISA expansion board I/O space (100H–3FFH).

Therefore EISA expansion boards cannot use these addresses and are limited to the bottom 256 locations of every 1k block of I/O space (the ISA system board only uses 256 locations in the first 1k of I/O space). As each slot covers a 4k range in the 64k I/O space, each slot will be able to use 4 blocks of 256 locations (1k). These are z000H–z0FFH, z400H–z4FFH, z800H–z8FFH and zC00H–zCFFH, as shown in the center column of *Figure 2.* EISA devices must only recognize addresses with bits 8 and 9 low (bottom 256 bytes of every 1k block).

ISA supports another slot specific signal AEN which is driven high to all slots by the system whenever a DMA cycle is in progress, to prevent I/O devices from decoding the I/O address on the bus.

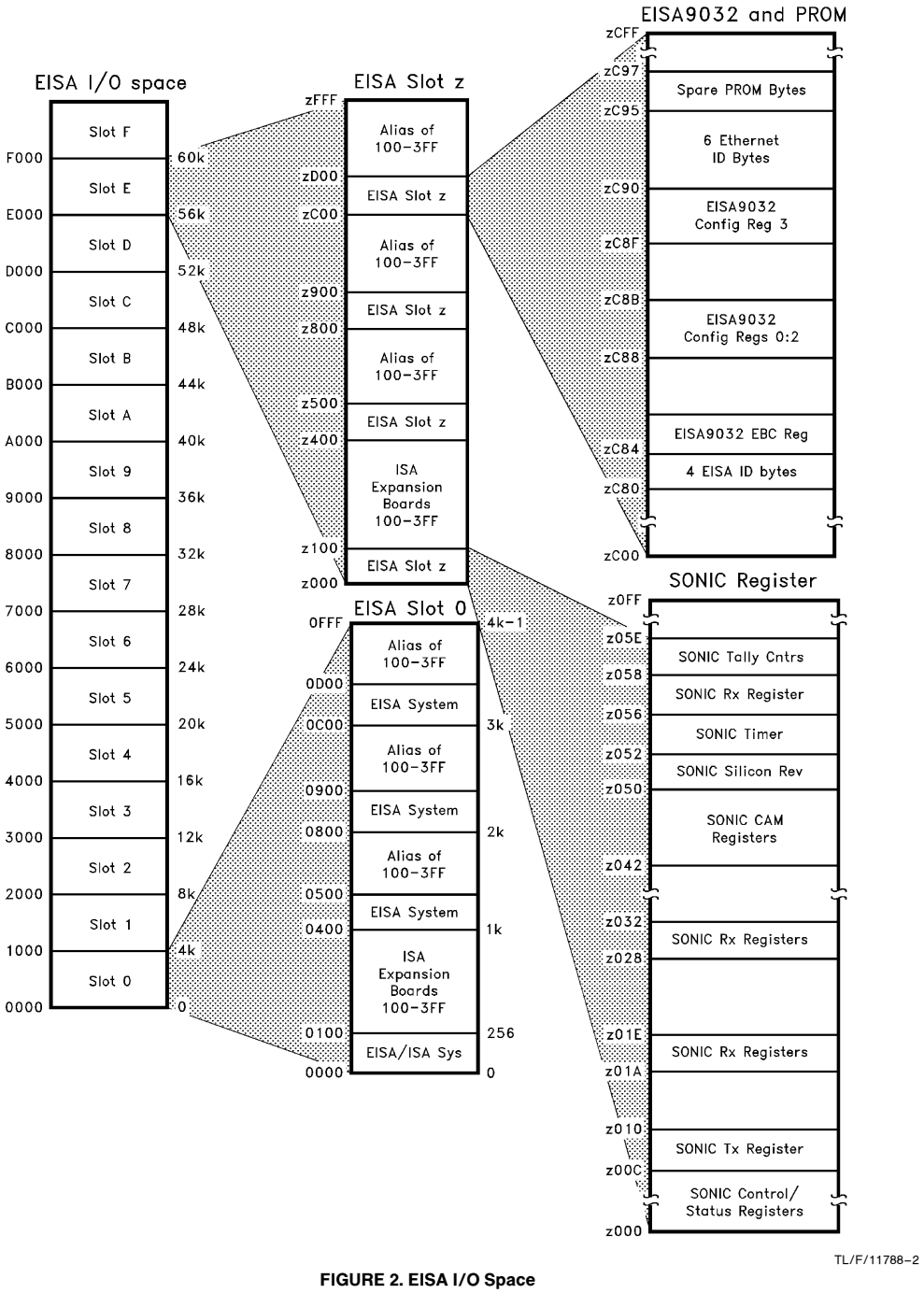

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FIGURE 2. EISA I/O Space

In EISA systems, the EISA controller decodes the top four bits of the I/O address LA15:12 (slot number) and only drives AEN active low to the particular slot being accessed. This relieves each slot from having to decode the slot address.

Therefore, EISA devices only need to decode address bits 8 and 9 both low and AEN low to prevent conflict with ISA devices or other EISA slots. This decoding enables the EISA device to use the bottom 256 bytes of its slot address space. The other three 256 byte blocks in its 4k I/O slot space will be aliased to the bottom 256 bytes. To make use of the other three 256 byte blocks and increase its I/O range to 1k, the EISA device must decode address bits 10 and 11.

The SONIC Ethernet adapter card supports 1k of slot specific I/O space decoding (see right column of *Figure 2*). Addresses 0 to 05EH in the first 256 byte block access the SONIC registers.

Addresses 80H to 83H in the last 256 byte block (C00H–CFFH) access the 4 EISA product IDs in the adapter card's PROM. Addresses 90H–97H in the last 256 byte block access the 6 Ethernet ID bytes (plus 2 spare bytes) in the adapter card's PROM. Addresses 84H, 88H to 8BH and 8FH in the last 256 byte block access EISA9032 configuration registers.

PLX's EISA9032 interface chip provides a configuration register bit which enables ISA I/O addressing to be used so that software drivers which used ISA addressing can be used with minor modifications. This board design does not support this configuration, as jumpers would be required to store the I/O base address into the configuration register at power up.

EISA BUS ARBITRATION AND BUS LATENCY

EISA provides centralized arbitration control to allow bus sharing between CPU, DMA controller, refresh controller and bus masters. Each master has a slot specific memory request (MRQx) and memory acknowledge (MAKx) signal.

If a request is received by the arbitration controller, it will preempt the device currently using the bus who must then release the bus within 64 EISA Bus Clocks (BCKs) (8 μs). Therefore a master on the bus can calculate the maximum bus latency (bus request to bus acknowledge delay) it may have to withstand.

EISA supports a three way rotating arbitration priority scheme between refresh, DMA and either the CPU or bus master. The CPU and bus masters maintain a two way rotating arbitration within the original 3 way rotation. For example, if there are two masters and all devices are requesting the bus, this will be the bus acknowledge sequence DMA/ refresh/ CPU/ DMA/ refresh/ Master1/ DMA/ refresh/ CPU/ DMA/ refresh/ Master2. Therefore the worst case bus latency for a bus master with n masters in the system is:

$$(\text{DMA} \times 2n) + (\text{refresh} \times 2n) + (\text{CPU} \times n) + (\text{master} \times (n-1)) =$$

$$5.8\ \mu s \times 2n + 1.3\ \mu s \times 2n + 9 \times n + 10.6 \times (n-1) = (33.8 \times n - 10.6)\mu s$$

Therefore for 8 masters = 259.8 μs

Note that raising the priority level of a master does not reduce this figure as all other masters must be serviced before the current master can use the bus again. The EISA bus only supports fairness scheme.

The SONIC Ethernet controller will request the bus whenever enough network data has entered its internal FIFO to cross a programmable threshold. The FIFO depth is 32 bytes and the minimum threshold that can be set in the FIFO is 4 bytes. Network data (10 MBits/s) will arrive at 1 byte every 800 ns, therefore the SONIC must acquire the bus before a further 28 bytes arrive into its FIFO, otherwise the FIFO will overflow and the packet will have to be retransmitted. This provides a bus latency of 22.4 μs.

SYSTEM CONFIGURATION

EISA provides a mechanism for automatic configuration of expansion boards. This eliminates the jumpers required by ISA adapters for board configuration.

The board manufacturer must provide a 4 byte product ID in a PROM which can be read at I/O locations zC80–zC83 and a configuration file with a file name matching the product ID.

At start up the EISA system will read the above I/O locations for every slot and compare the product IDs with what it had stored in non-volatile memory during the last system configuration.

If the system finds a mismatch, the system will need to be reconfigured by running a configuration utility which is provided by each EISA system manufacturer. This utility will look for a configuration file with a name matching the product ID of the board to be installed. The configuration file which is provided by the expansion board manufacturer, contains a list of resources the board is able to use (like interrupt lines for example). The configuration utility will choose which resources to allocate to the board so that it does not conflict with other boards and store the information in non volatile memory.

The board's driver can then read this non volatile memory and program the board so that it will use the resources allocated to it.

The first two bytes of the product ID (locations 0zC80 and 0zC81) contain a compressed representation of the manufacturer's code. The next two bytes (locations 0zC82–3) contain the product number and revision number. Please refer to the EISA specification for details on how these values are derived.

If the expansion board is modified so that it requires a new configuration file, both the product number and revision number must be modified. If it does not require a new configuration file, just the revision number can be changed.

EISA BUS PROTOCOL

EISA supports two types of read or write cycles, standard cycles and burst cycles. A burst sequence always starts with a standard cycle. Standard cycles are executed in 2 bus clocks per transfer, whereas burst cycles are executed in 1 bus clock per transfer.

The EISA9032 supports burst read transfers at 25 MHz. At 33 MHz the EISA9032 supports burst read and write transfers. All access to descriptor and resource areas (RRA, RDA and TDA) are executed as standard cycles.

Next follows a description of the standard cycle protocol, how it is converted to a burst cycle sequence, and a brief description of how the EISA9032 interface chip supports these cycles.

For a standard cycle, (see *Figure 3*), once the master has gained control of the bus with the MRQx and MAKx handshake, it initiates a cycle by driving the address and M-IO signals on the falling edge of the clock (0 to 1 clock transition). On the next rising edge of the clock it drives START for 1 clock period, W/R and BE<3:0> (1 to 2 transition). On the next rising edge of the clock (3 to 4 transition) the system board asserts CMD until the end of the cycle.

The slave, after decoding the address, will drive EX32 active if it can support 32-bit transfers. The master samples this signal on the next rising edge of the clock (3 to 4 transition). If EX32 is not asserted the master will TRI-STATE® its BE<3:0> to enable the system board to perform data size translation. Once the system board has completed the translation it asserts EX32, enabling the master to complete the cycle.

The master then samples the EXRDY line from the slave on the next falling edge of the clock (4 to 5 transition). If it is not asserted the master will insert wait states until EXRDY is asserted. The master can also drive a new address for the next cycle on that same clock edge.

On the next rising edge of the clock (5-6 for a single standard cycle, or 5-2 for back to back standard cycles, or 5-4 for burst cycles) the master or slave will latch the data depending on whether it is a read or write cycle, in this way completing a single standard cycle.

Figure 4 shows an example of a typical slave access, a SONIC register read.

A burst sequence, (see *Figures 5* and *6*), always starts with a standard cycle which is the protocol described above. If the master wishes to perform a burst of cycles, it will sample the SLBURST signal from the slave during the 3 to 4 clock transition of the initial standard cycle. If the slave has asserted this signal indicating it supports burst cycles, the master will drive MSBURST active which the slave will sample on the last clock edge of the standard cycle (5 to 4 transition).

MSBURST asserted informs the slave that the next cycle is a burst cycle which can be completed in 1 bus clock. The slave will continue to sample MSBURST on every 5-4 clock transition and respond to burst transfers until MSBURST is deasserted. The master or slave will latch the data on the 5-4 clock transition of every transfer depending on whether it is a read or write cycle.

The EISA specification places some restrictions on the use of burst cycles:

1. No I/O cycles
2. No ISA devices
3. No mixed read and write cycles
4. Address lines LA31:10 must remain constant (no crossing of a 1k memory page boundary)

LA9:2 and BE<3:0> can change within a burst, that is addresses don't need to be sequential, and cycle translation and wait states are still supported.

Address Pipelining

Note that the EISA protocol requires pipelined addresses, that is the master must provide a new address half a clock before the data is ready to be latched for the previous cycle if it wants to perform back to back transfers. This is something the SONIC Ethernet controller does not support directly.

For standard cycles this is not a problem as, at the end of a cycle, the EISA9032 interface chip will assert ready to the SONIC, wait for a new address strobe from the SONIC and after driving the new SONIC address on the EISA bus for half a clock, assert the START signal indicating the beginning of a new cycle. This introduces 2 idle bus clock cycles between consecutive standard cycles.

For burst cycles the interface logic must provide a new address during the 4 to 5 clock transition of the previous cycle, as there is no new START signal to indicate when the new address is asserted. This is supported by the EISA9032 interface chip by automatically loading the first address of a burst into an 8-bit counter during the initial standard cycle and incrementing the counter on every 4 to 5 clock transition.

An 8-bit counter for address bits LA9:2 is sufficient, as address lines LA31:10 must remain constant throughout a burst cycle (must not cross a 1k page). The EISA9032 interface chip has a mechanism for detecting when the SONIC address is crossing a 1k page (it detects addresses ending in 3FCH) and will terminate the burst and initiate a new transfer.

Note that because the EISA9032 is using a counter, this means the interface logic only supports bursts to sequential addresses. This is not a problem as burst cycles are only used for the receive and transmit buffer areas which are always addressed sequentially by the SONIC.

Note also that the EISA9032 interface chip starts a cycle in a burst (by driving a new address on the bus and maintaining MSBURST active) before the SONIC has even asserted Address Strobe. This means the interface logic will always do one extra bus cycle at the end of a burst. For read cycles, the software driver must ensure that the end of the TBA is not contiguous to an area of memory that cannot be read. For write cycles, the software driver must ensure that EOBC (End Of Buffer Word Count) in the RBA (Receive Buffer Area) is set at least 2 words larger than the size of the biggest packet that can be received. This means that the SONIC will not use the last two words of an RBA.

SLAVE INTERFACE OPERATION

The SONIC Ethernet adapter card supports an EISA slave interface to enable the host CPU to access the following devices on the card.

SONIC Registers

The SONIC contains 64 sixteen bit wide registers. Read and write access to 30 of those registers enables the software driver to control and monitor packet transmission and reception. A further 18 registers are used internally by the SONIC. Users may monitor these registers. The last 16 registers (EISA I/O addresses z060H–z07FH) are for test use only. Users must not access these registers. (See *Figure 2* EISA I/O space.)

32-Byte PROM

The adapter card's ''EISA product ID'' and ''Ethernet address'' are stored in a 32 x 8 PROM. PROM addresses A0:3 come directly from the EISA bus, but address A4 is generated by the EISA9032 interface chip as the ''EISA ID'' signal. For EISA I/O addresses 80H–8FH, EISA ID = 1 (EISA

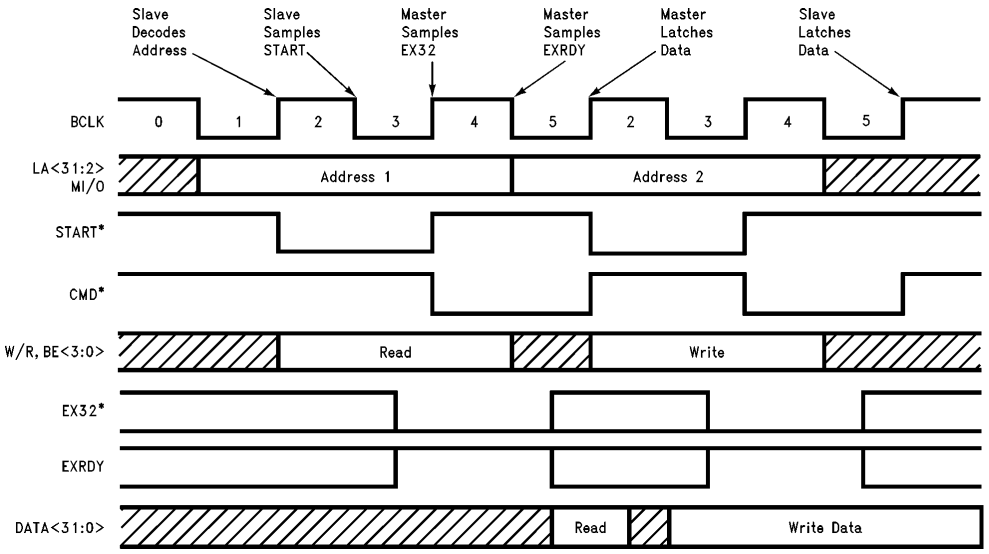

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FIGURE 3. EISA Standard Cycle

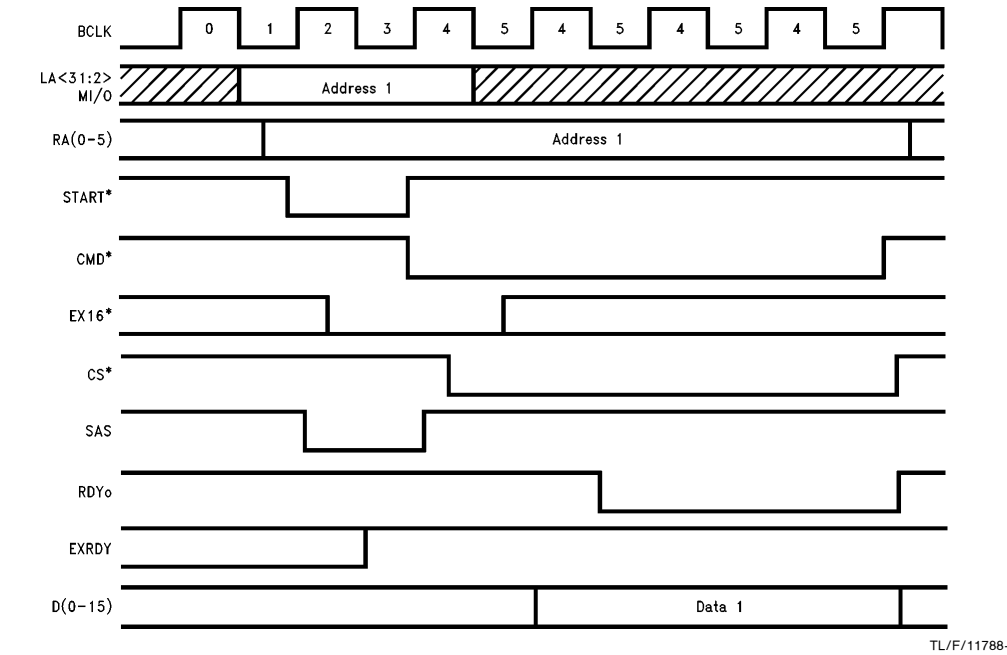

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FIGURE 4. SONIC Register Read Cycle

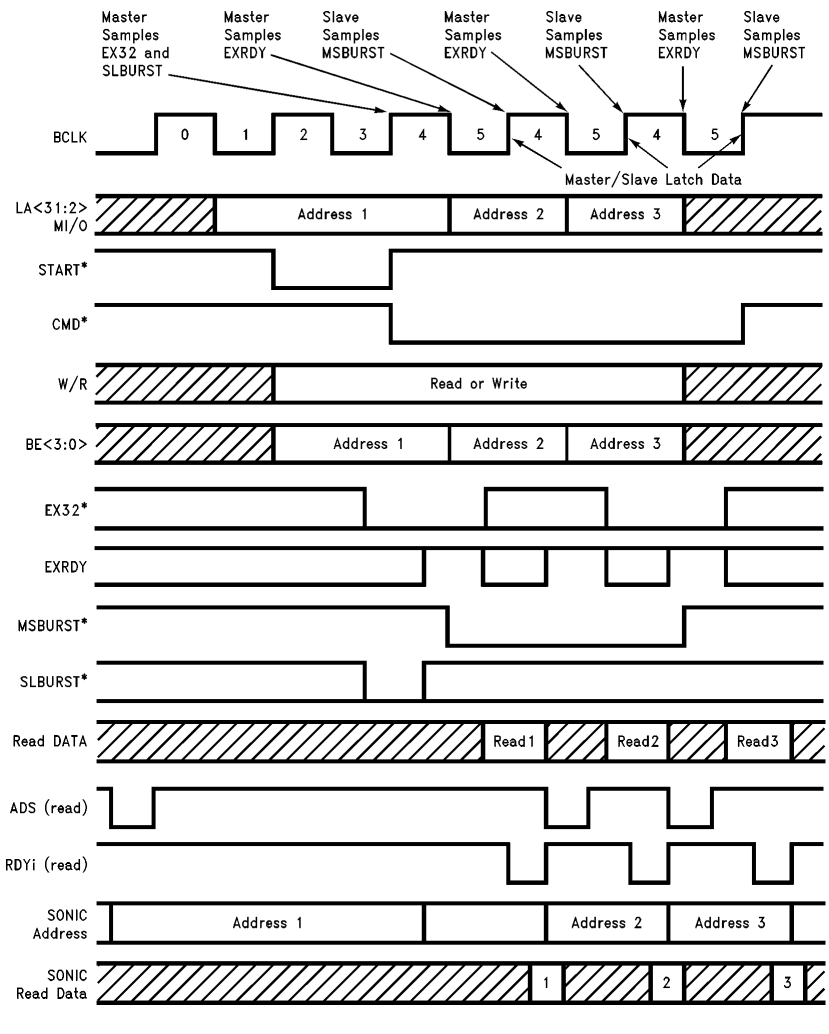

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FIGURE 5. EISA Read Burst Cycle

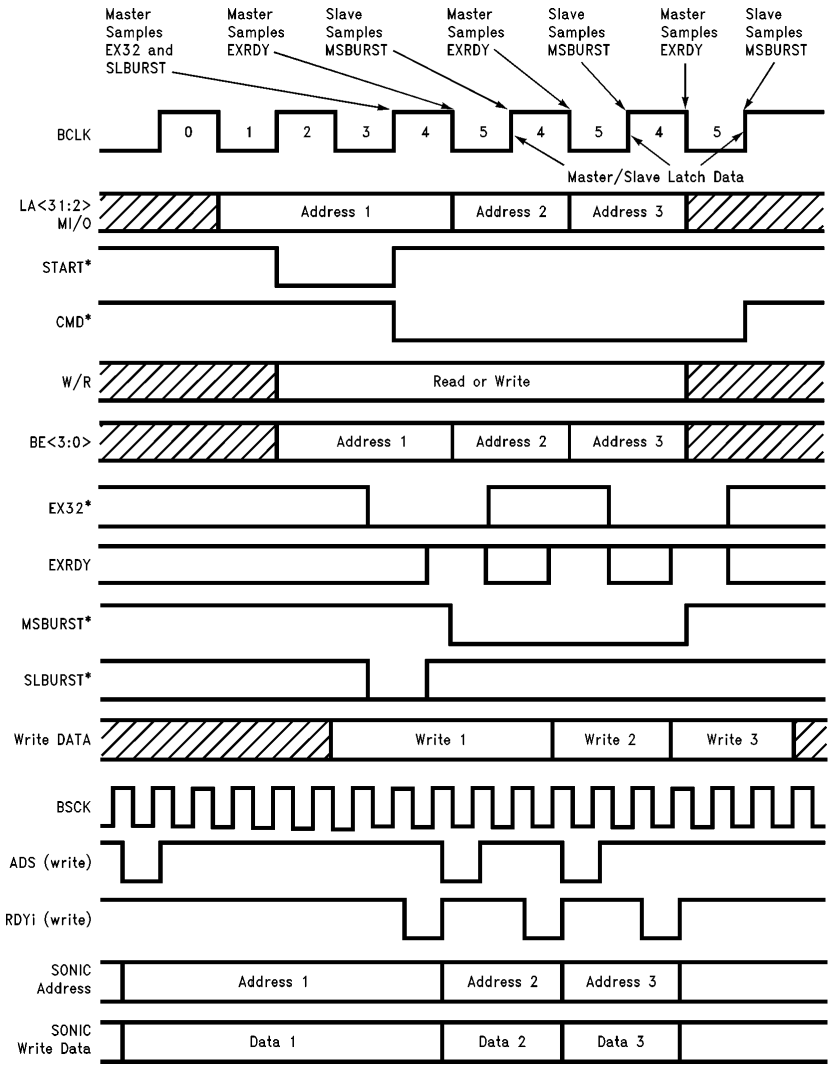

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FIGURE 6. EISA Write Burst Cycle

product ID bytes) and for EISA I/O addresses 90H–97H, EISA ID = 0 (Ethernet ID bytes). This means the EISA9032 chip maps EISA I/O addresses 80H–84H to PROM addresses 10H–14H and EISA addresses 90H–97H to 0H–7H. (Refer to *Figure 2* for I/O map.)

This mapping requires the PROM to be programmed as per *Figure 7.* The first 6 byte locations of this PROM contain the unique physical address assigned to each Ethernet board. These reside on EISA I/O addresses zC90–zC95. The next 2 bytes of the PROM are not used. The following 4 bytes (PROM address 10H–13H) contain the EISA product ID, that is a compressed representation of the manufacturers code, product number and revision number. These 4 bytes reside in EISA I/O space zC80–zC83. The remaining 12 PROM byte locations are not used.

EISA9032 Bus Interface Configuration Registers

These registers reside in EISA I/O space zC84H and zC88H–zC8BH.

When configuring the card, the configuration utility program displays a screen enabling the user to select a number of options. The network software driver will then set up the EISA9032 configuration registers according to the values selected by the configuration utility and the user.

Table I lists the configuration options programmable in the EISA9032 registers (also refer to the EISA9032 data sheet).

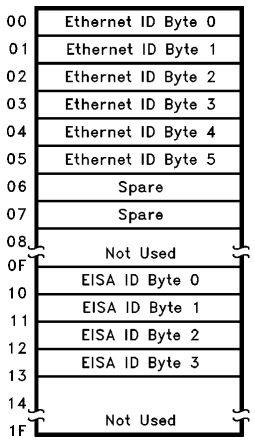

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FIGURE 7. Ethernet/EISA ID PROM

TABLE I. EISA 9032 Configuration Options

Configuration	Options	Selection (Default)
Expansion Board Enable	Enable/Disable	(Enable)
Interrupt Type	Edge/Level Triggered	User Selects
Interrupt Number	EISA IRQ 5, 9, 10, 11	EISA Config. Utility Selects
Preempt Time	55/23 EISA Bus Clocks	User Selects (23)
Bus Master Data Size	32/16 Bits	(32)
Slave I/O Data Size	32/16 Bits	(16)
I/O Addressing	ISA/Slot Specific	Slot Specific
ISA I/O Range		Not Used
BIOS EPROM Size	Disable/8k/16k/32k	
BIOS EPROM Address Range		EISA Config. Utility Selects
SONIC Register Port Address		Not Used
Burst Transfer Enable	Enable/Disable	(Enable)
Local Software Reset	Resets EISA9032	
800 ns Bus Release Timer	Enable/Disable	User Selects (Disable)
USR0 ACT/OWN	Accept/Reject Own Packet	User Selects (Accept)
USR1 Thin/Thick	Thin/Thick Ethernet	User Selects (Thin)
USR2		Not Used
USR3		Not Used

A number of these options are selected by the EISA configuration Utility program. During configuration the Utility program will read the configuration file generated by the board manufacturer which lists the options the card can support and write its selection into non-volatile memory. The board's software driver will then read this memory and write the selections into the EISA9032 configuration registers. These options include interrupt request lines and BIOS EPROM memory address range.

Another set of options can be selected by the user but should not be changed from their default values on this board. These include Bus Master Data Size = 32 bits, Slave I/O Data Size = 16 bits, I/O Addressing = Slot specific (See I/O Accesses and addressing), Expansion Board Enable = Enable, BIOS EPROM Size = 32k and burst transfer enable = enable. This last option can be used to disable burst transfers so that all the card's master cycles are executed as standard cycles.

A last set of options are system or software dependent and should be selected by the user. These include Interrupt Type (Edge/Level). Level triggered interrupts enable several masters to share an interrupt line. Preempt time of 23 or 55 EISA Bus clocks. This is the number of clocks the SONIC Ethernet card will stay on the EISA bus after the memory acknowledge signal has been deasserted by the arbitrator. Accept/Reject own packet. If in reject mode, the EISA9032 will drive the packet reject input of the SONIC whenever the SONIC is transmitting a packet. Thin/Thick Ethernet will select either Thin or Thick Ethernet by turning the −9V DC-DC converter output to the Coaxial Transceiver Interface on or off.

32k x 8 BIOS EPROM

The optional 32k x 8 EPROM design can be added if the user wishes to provide software to boot up the EISA PC from the network. The boot ROM code is simply a special driver that is executed when the EISA PC is initializing, and causes the PC's Operating System to be loaded in from a network server rather than from the EISA PC's hard disk. This software is not provided by National. It can be created by obtaining Novell's Boot ROM developer's kit, or Microsoft's NDDK (Network Device Driver Kit) and following their programming information.

The PROM resides in memory space in the range 0C0000H–0DFFFFH. Its exact location within this range is selected by the EISA configuration utility during board configuration. The card only decodes addresses 17–23.

The Ethernet adapter board supports 6 different types of slave cycle EPROM read, ROM read, SONIC registers read and write, and EISA9032 configuration registers read and write cycles.

Slave Cycle

EISA slave cycles are initiated by the host CPU driving the 16-bit I/O address or the 24-bit EPROM memory address on the bus and the M-IO signal on the falling edge of the clock, and driving START active with W/R and BE<3:0> on the next rising edge of the clock. The EISA9032 interface chip will decode the address and drive EX16* low if the CPU is accessing the SONIC registers or its internal registers. It will then drive EXRDY inactive if it needs to insert wait states until the device accessed is ready to provide or accept the data. Bus transfers to the EISA 9032 configuration registers or the ROM (35 ns access time) are completed with no wait states. Bus transfers to the EPROM (250 ns access time) are completed with two clock cycle wait states and bus transfers to the SONIC will be wait stated until the SONIC asserts RDYo indicating it has completed the transfer.

MASTER INTERFACE DESCRIPTION

The card's main function is to transfer Ethernet packet data from the host's CPU system memory to the Ethernet cable during packet transmission, and from the Ethernet cable to the system memory during packet reception.

The SONIC Ethernet controller's bus master capabilities and buffer management scheme enable it to perform this function using the on board PLX EISA9032 interface chip with no CPU involvement.

Whenever a packet transmission has been requested by the software driver writing to the transmit bit in the command register of the SONIC, or a packet reception is taking place on the Ethernet cable, the SONIC needs to execute read and write cycles on the EISA bus to access descriptor or resource pointer areas in system memory (RDA, TDA, RRA) and to transfer packet data between its internal 32 byte FIFO and buffer areas in system memory (RBA, TBA).

The SONIC initiates a master bus cycle by driving its bus request signal HOLD to the EISA9032 interface chip, who will in turn assert MREQx on the EISA bus. Once the system EISA arbitration controller grants the bus by asserting MAKx, the EISA9032 acknowledges the SONIC by driving HLDA so it can start executing a bus cycle. That is the arbitration phase of the bus transfer.

The SONIC then drives the address and status lines to define which area of memory it wishes to access (RRA, RBA, RDA, TDA, TBA) and qualifies them with address strobe ADS. The EISA9032 loads the lower 8 bits of the address A9:2 into its internal counter and initiates a standard cycle on the bus. If during this cycle the interface chip encounters the following conditions, it will drive MSBURST active to initiate a burst cycle following the standard cycle. The conditions are that the SONIC status lines indicate an access to the RBA or TBA, the slave has asserted EX32 indicating it supports 32-bit transfers, the slave has asserted SLBURST indicating it supports burst transfers, the SONIC address does not end in 3FCH (indicating a 1k page crossing) and burst mode was enabled during the adapter card's configuration. The EISA9032 will drive RDYi back to the SONIC at the end of every burst cycle.

Note that EISA burst cycles are completed in one EISA clock, whereas SONIC cycles are completed in 3 SONIC bus clocks (asynchronous mode). Therefore for the SONIC to support EISA burst mode it must be run at three times the EISA bus clock speed (25 MHz).

If any of the above conditions were not met, the EISA9032 will assert RDYi to the SONIC and wait for a new address strobe before initiating a new standard cycle on the bus.

DP83932EB-EISA PERFORMANCE

Packet throughput is an important consideration in developing an Ethernet adapter. However, bench-marking of throughput may not tell the whole network performance story. In spite of this, *Figure 8* attempts to compare the performance of this SONIC implementation to other EISA implementations.

In *Figure 8* two tests are shown using NetWare 3.1, and Novell's Perform2 v2.3 performance utility. In both graphs the read/write performance in two configurations using a 4096 byte record size. Both tests use a single 33 MHz 486 server. In *Figure 8a* a single 12 MHz 286 client was used, and in *Figure 8b* 10 8 MHz 286 clients were used.

As can be seen from this *Figure*, the performance of the DP83932EB-EISA card surpasses other popular implementations.

MORE INFORMATION

For more information regarding the EISA9032, and manufacturing information for the Evaluation board contact:

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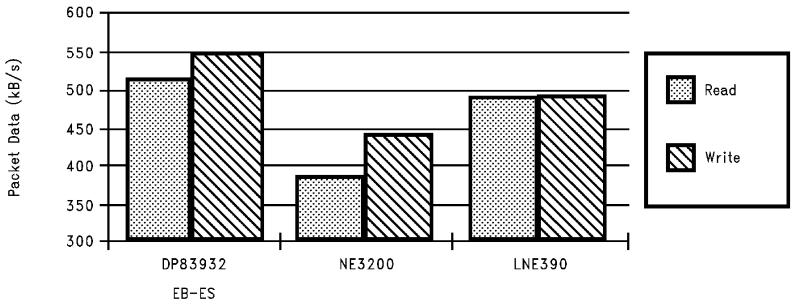

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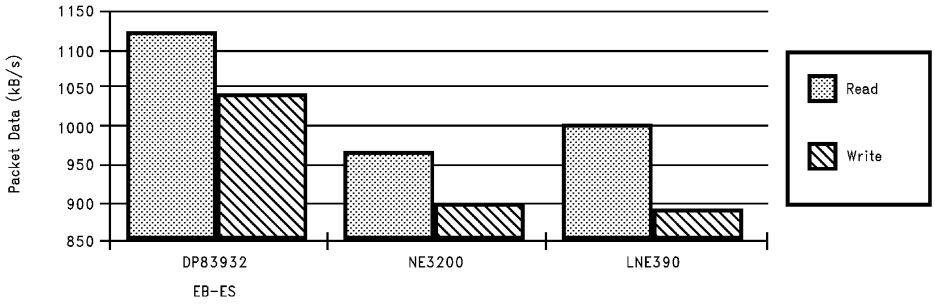
(a). Single Workstation Performance



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(b). Ten Workstation Performance

FIGURE 8. Network Performance Comparison for Single and 10 Workstation LANs

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