Change the Battery on any DP857X Family Member Using Software without Losing Time

National Semiconductor
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This application note describes a method for changing the battery on any of the DP857X family members while power is applied. The method involves use of the test mode. The clock remains running so that no time is lost.

THE PROBLEM

Your in the battery backed mode and the low battery bit has turned on (logic Hi). The battery needs to be changed but you don't want to lose time or have to re-initialize the clock.

THE SOLUTION

Assuming that the clock is still running (start/stop bit in the Real Time Mode Register = '1'), do the following sequence:

1. Write a '1' to bit D7 of the Periodic Flag Register (PFR). Now you are in the Test Mode.
2. Write '1' to bit D7 of the Test Register (address Hex 1F in page 0), all other bits are '0'. This action disables the OSC FAIL bit.
3. Write a '1' to bit D6 of the PFR. This action changes the RTC from battery backed mode to single supply mode.
4. Now the battery can be changed. If the change takes place within a half minute or so, the V_{BB} pin can be left floating for that time. If the battery is soldered in such that many minutes will occur, then temporarily connect V_{BB} to ground until the new battery is ready for installation.
5. After the battery is connected, to return to battery backed mode:

   5.1 Write '0' to all bit positions of the Test Register (address Hex 1F in page 0).

   5.2 Write '0' to bits D6 and D7 of the PFR. This write returns the chip to the battery backed mode.

WHY CAN'T I SWITCH FROM BATTERY BACKED TO SINGLE SUPPLY UNDER NORMAL OPERATION?

Steps 1 thru 4 need to be done because a ''glitch'' can occur in the oscillator fail circuitry when switching from battery backed mode to single supply mode. This glitch can momentarily cause an OSC FAIL condition which stops the clock and sets the OSC FAIL bit (D6 in the PFR). The reason for entering the test mode is that this is the only way the OSC FAIL bit can be disabled.

HOW THE GLITCH OCCURS

In battery backed mode, the oscillator fail circuitry is powered by an internal voltage follower referenced to V_{BB}. When the single supply mode is selected, this voltage follower is disabled and the oscillator fail circuitry instantaneously sees the V_{CC} voltage. Bench tests indicate that the magnitude of the change is what causes the glitch, thus stopping the clock. If the difference between V_{BB} and V_{CC} is reduced, then the clock does not stop.

Example: If V_{BB} is 2.5V and V_{CC} is 5.0V then the clock continues running if you switch from battery backed mode to single supply mode. However, if V_{BB} is 2V and V_{CC} is 5V then the clock will stop when you switch from battery backed mode to single supply mode.

TEST CONDITIONS

Bench tests were made using a PC-AT® 386/33 MHz. The DP8570 was interfaced to the PC using the circuit shown in *Figure 1*.

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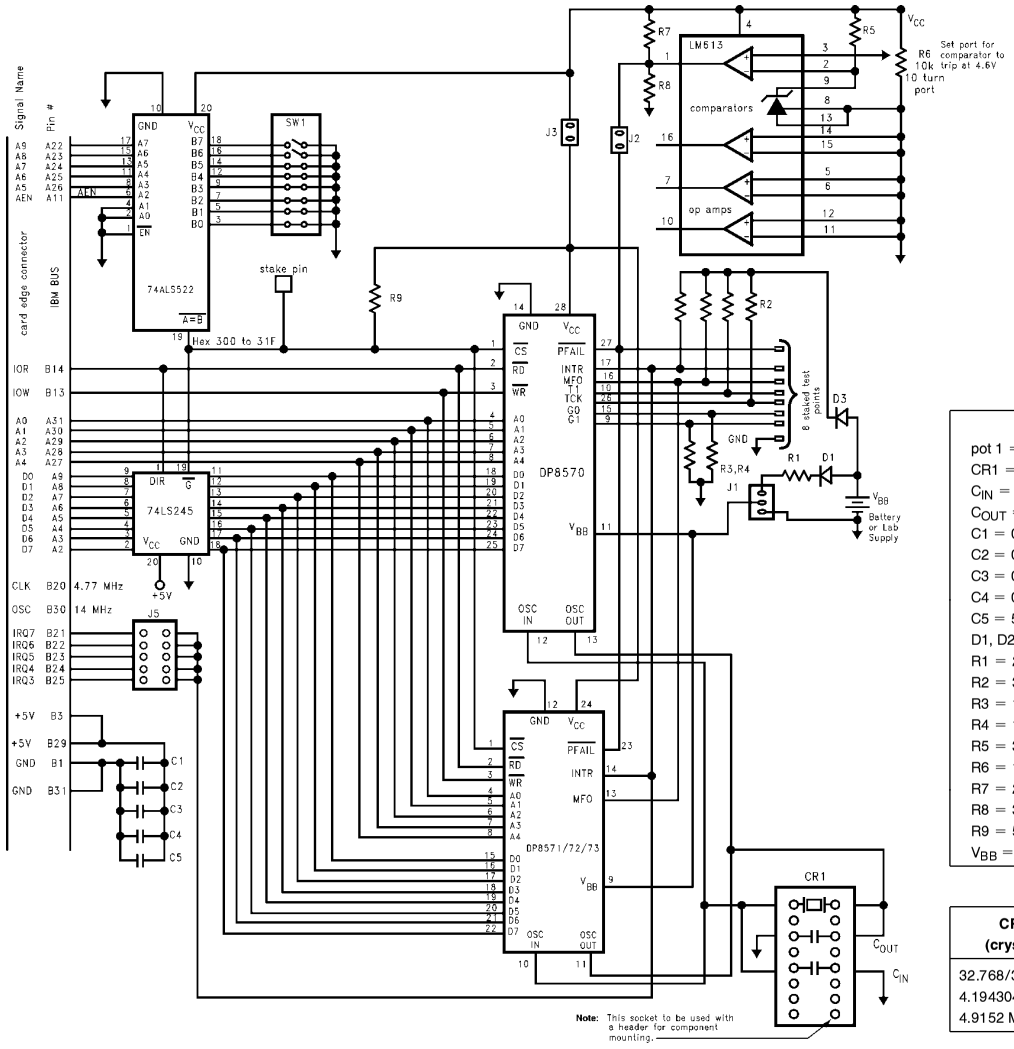


Component and Placement List

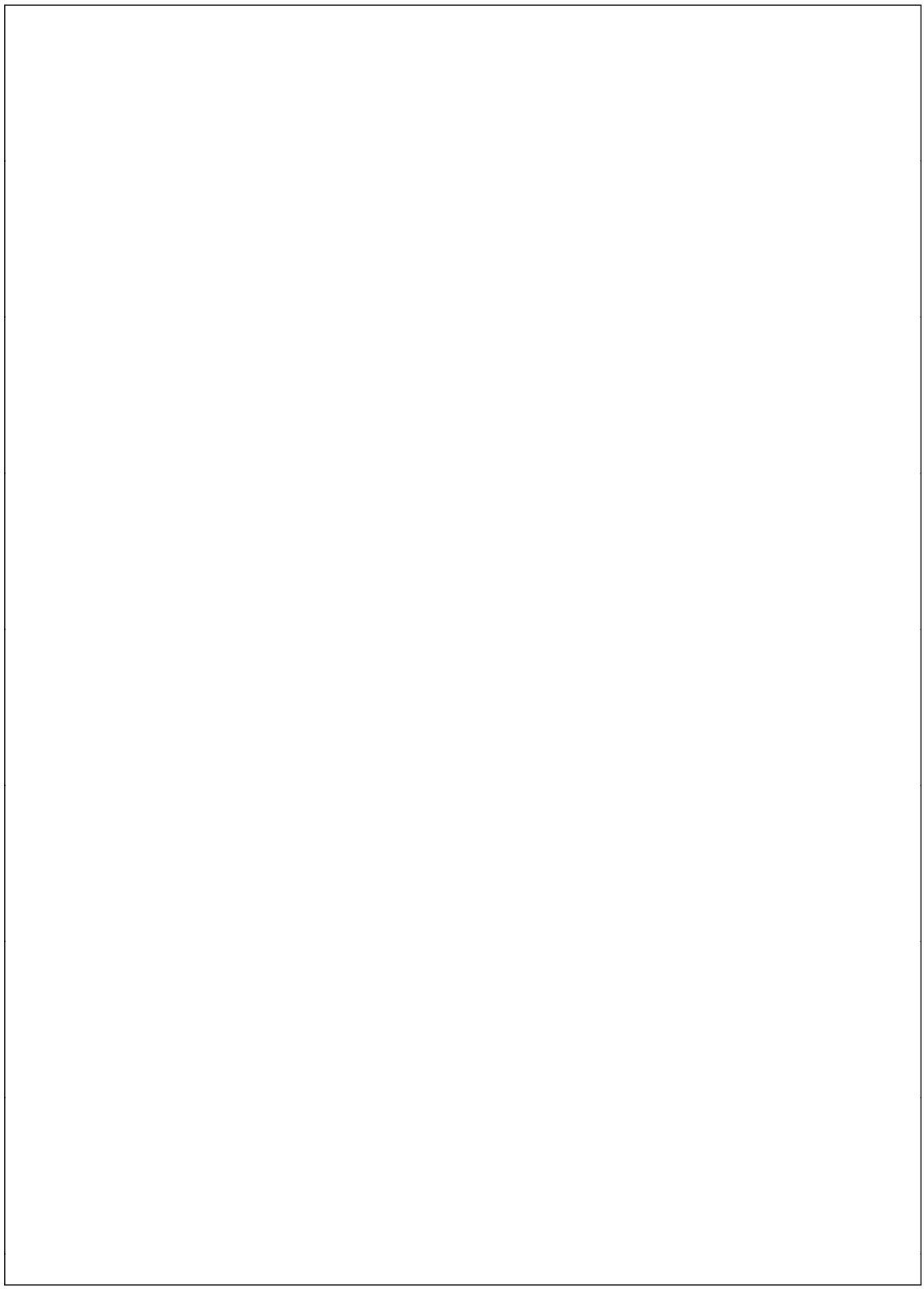
pot 1 = 10 kΩ
CR1 = see Table I
C_{IN} = see Table I
C_{OUT} = see Table I
C1 = 0.047 μF ceramic placed at U1
C2 = 0.047 μF ceramic placed at U2
C3 = 0.047 μF ceramic placed at U3
C4 = 0.047 μF ceramic placed at U4
C5 = 5.6 μF solid tantalum placed at card edge
D1, D2, D3 = 1N914 or 1N4001 or 1N4933
R1 = 2.7 kΩ
R2 = 3.9 kΩ
R3 = 10 kΩ
R4 = 10 kΩ
R5 = 3.3 kΩ
R6 = 10 turn 10 kΩ
R7 = 20 kΩ
R8 = 39 kΩ
R9 = 5 kΩ
V_{BB} = 3.0V to 3.4V Lithium battery (coin cell)

Table I

CR1 (crystal)	C_{IN} (pF)	C_{OUT} (pF)
32.768/32.0 kHz	15	47
4.194304 MHz	36	68
4.9152 MHz	36	68

TL/F/11848–1

FIGURE 1. General Purpose Interface to IBM® PC-XT® or PC-AT® for Experiments



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