Layout Guidelines for an Ethernet Adapter Using the DP83907 AT/LANTIC™ II

National Semiconductor
Application Note 973
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OVERVIEW

This application outlines board layout and design considerations when using the DP83907.

Board Design and Layout

In a multi-layer PCB with good ground and power planes, there should be little risk of noise problems due to layout. When designing a two-layer board special care is needed. The DP83907 drives 16 data lines (SD0-15) with fast high-current drivers that will cause ground bounce if proper care in not taken in laying out the VCC and GND lines. Ground routing should be arranged in a grid to ensure good return current paths between the DP83907 and all the ISA bus ground connections. Analog and Digital VCC and GND lines should not overlap to prevent crosstalk noise.

1.0 Crystal and Oscillator Design

Care should be taken when connecting a crystal. Stray capacitance (e.g., from PC board traces and plated-through holes around X1 and X2 pins) can shift the crystal's frequency out of range, causing the transmitted frequency to exceed the 0.01% tolerance specified by the IEEE. The crystal or oscillator layout should locate all components close to the X1 and X2 pins and should use short traces to avoid excess capacitance and inductance. When using a standard size crystal the crystal should be laid flat with power planes voided in that area, When using a low-profile crystal this is not necessary.

1.1 Decoupling for the DP83907

The DP83907 is composed of multiple functional blocks. The analog and digital functional blocks should be run on separate power rails.

Since the power supply pins on the DP83907 are all connected to the same 5V/0V supply in the ISA connector, noise from other slots in the system will be coupled to the power supply pins on the DP83907. This problem is particularly serious in two-layer boards having no separate power or ground planes. To minimize the impact, the DP83907 should be run on separate V_{CC} and ground traces whenever possible. These traces should join near the PC ISA bus connector and be properly filtered.

The first area which requires attention is the switching on the DP83907's System Data (SD) bus. This bus provides high current drive, TRI-STATE®, fast rise and fall times and is a major noise contributor. The V_{CC} pins which provide power to SD bus drivers and the GND pins which are the return path should be carefully decoupled to reduce the noise. In order to reduce noise the power supply pins and the ground pins on the DP83907 should be decoupled by 0.1 μF and 1000 pF capacitors, with the capacitors connected as close as possible to the chip and the plane.

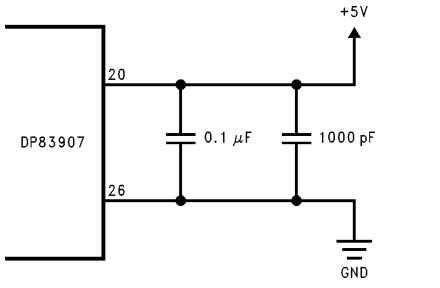

FIGURE 1. Power and Ground Decoupling

This should be done on all the V_{CC} and GND pairs which are pins 20–23, 26–27, 48–49, 35–32, 70–75, 103–100, 109–110. Exceptions are analog V_{CC} and GND pins 40 and 41 which have different decoupling requirements and are discussed in Section 1.2.

The rest of the GND pins except for pin 41 (AGND) should be directly connected to the ground plane.

The second area where care must be taken is in isolation of ''quiet'' output and input signals from ''noisy'' output signals. In this regard, the SD outputs should be a minimum of a double space away from ANY other signal trace, preferably with a ground island in between. Similarly, the IRQ traces should be kept isolated from other signals.

Additionally, care must be taken to prevent fast control signals (IOCHRDY, IO16) causing crosstalk on sensitive inputs. To this end, IO16 must be separated by a double space from input signals (SA0, SA1 . . .). In the case of IOCHRDY, the ground pin supplying IOCHRDY (pin 14) must be connected through a ferrite bead (26Z @ 100 MHz) and IOCHRDY must be separated from AEN by at LEAST a double space, preferably with an isolation ground island placed in between. This island should connect to 0V only at the edge connector.

These layout considerations have been taken into account in the latest DP83907EB-AT board design. Manufacturers must follow these recommendations in their design to avoid possible noise related problems.

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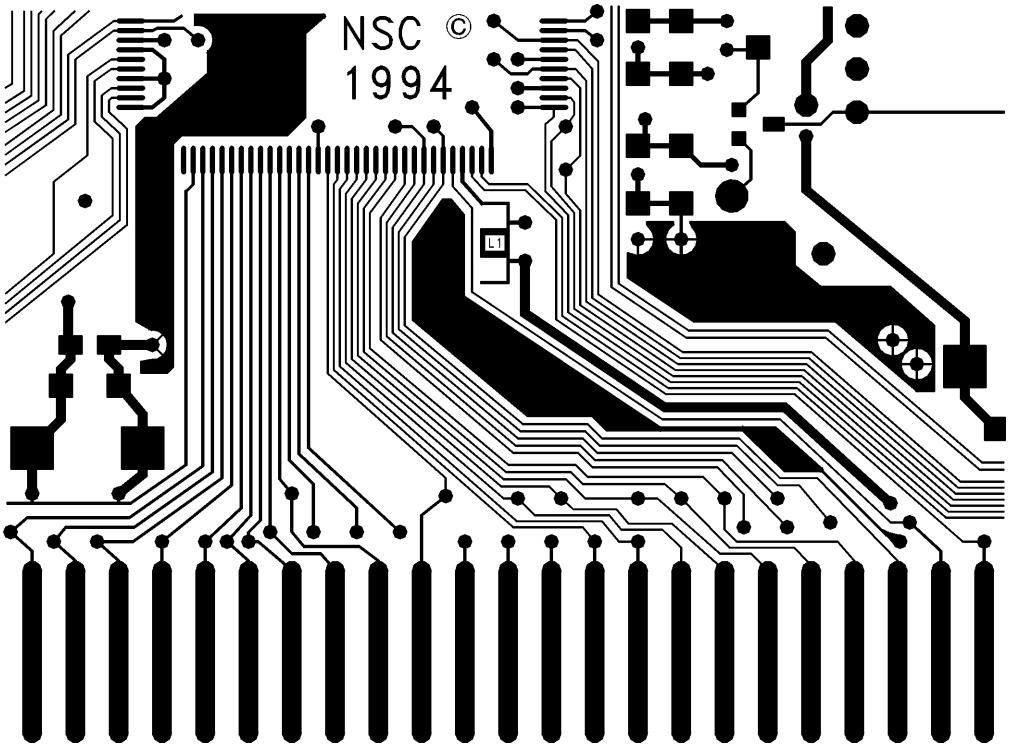

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FIGURE 2. Signal Isolation Detail View

1.2 PLL Power Supply Noise

In order to improve the performance of the PLL, a single pole filter should be used on the PLL power supply pin. This is shown on *Figure 3*.

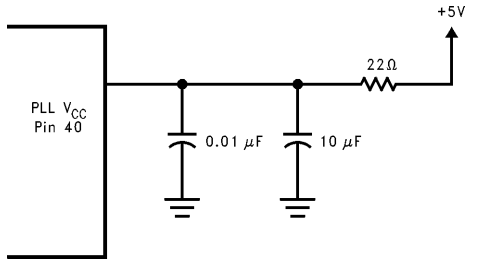

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FIGURE 3. PLL V_{CC} Noise Filter

1.3 PC ISA Bus Interface

Decoupling of noise from the ISA Bus power supply is achieved using 0.1 μF, 100 pF and 22 μF capacitors (used to filter out lower frequency noise in the order of a few kHz). All these three capacitors are placed near the ISA bus connector. This is done for both power supplies of the ISA bus.

Care should also be taken to place the DP83907 as close to the edge connector as possible, with the aim of keeping the ground tracks to a minimum length.

1.4 Attachment Unit Interface

The AUI signals are differential signals. Each pair of these differential signals should be routed in adjacent channels. The traces should go as straight as possible and avoid forming loops to minimize the potential of magnetic coupling. It is not necessary to void the power plane under them.

1.5 Twisted Pair Interface

The transmit signals should be of the same length and as close as possible.These signals are TXOD+, TXOD−, TXO+ and TXO−.

The receive signals should also be of the same length and as close as possible.

The transmit and receive signals should be kept away from each other.

The resistors should be directly tied between the RTX and REQ pins to TPVCC or TPGND.

1.6 Coaxial Transceiver Interface (CTI)

The Coax Transceiver Interface (DP8392CN) should be placed very close to the BNC connector. This will allow the TXO/RXI trace to be short and straight. The area under these traces should be voided of all other signal and power planes (as shown in *Figure 4*) in order to meet the IEEE 802.3 input capacitance requirements. The BNC connector on the evaluation board is a standard part, however, ''quiet'' connectors are readily available for better noise figures and FCC qualification. The CTI requires an area of copper for heat dissipation. This is also shown in *Figure 4* and is documented in the DP8392C data sheet. The ground shield of the BNC connector and coax cable are resistively and capacitively decoupled to chassis ground. There is a chassis ground strip on each layer of the board. This is connected to the chassis of the PC through the 15-pin AUI connector's metal body. Chassis ground is then capacitively decoupled to digital ground through capacitors. The chassis ground trace along the front of the board forms a ''shield'' so that noise is not emitted into or received from the environment.

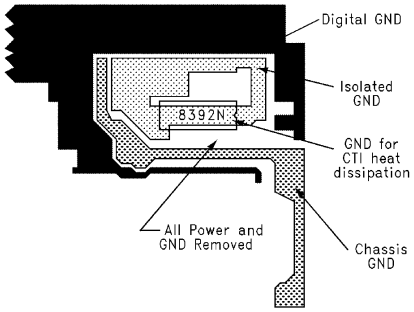

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FIGURE 4. DP83907EB-AT CTI Layout Diagram

1.7 FCC Considerations

For applications requiring FCC class B certification it is strongly recommended that the existing BNC connector be replaced with a *filtered* BNC connector and capacitors C45 and C54 removed.

A filtered BNC connector similar to p/n 413515 from AMP incorporated or p/n 456-117 from Amphenol Corp. (or equivalent) will suffice.

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998