Understanding and Eliminating EMI in Microcontroller Applications

National Semiconductor
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1.0 ABSTRACT

In today's world, with increasing numbers of both fixed and mobile electronic devices, electromagnetic compatibility (EMC) is becoming a critical issue. Disastrous, if not annoying, results occur if a system, subsystem or component interferes with another through electromagnetic means. The EMC problem is first explained, and then the basic theory is presented with an explanation on how to use it to control an EMC problem during the initial design phase. The methods that some silicon manufacturers are using to control EMC and how these changes affect our systems will be examined. A total system (automobile radio) will be examined in detail to prove the effectiveness of a EMC reduced COP8™ (8-bit microcontroller). Overall design guidelines will also be given so that the designer can minimize EMI *before it becomes a problem*.

2.0 INTRODUCTION AND BACKGROUND

Electromagnetic Interference with Powered Wheelchairs

August 26, 1994

FDA is receiving inquiries about reports that electromagnetic interference (EMI) can cause some power-driven wheelchairs and scooters to move unexpectedly. The agency has investigated this matter and determined that EMI can cause unexpected movement in some power-driven wheelchairs when they are turned on. Not all brands and models of power wheelchairs and scooters have this problem. Some have greater immunity levels than others that may protect against EMI. Common sources of EMI include cellular phones, CB radios, TV and radio stations, amateur (HAM) radios and police, fire and ambulance radios.

After receiving reports of problems, FDA tested sample wheelchairs and scooters in its laboratories and obtained information from manufacturers and users about possible EMI-related incidents. As a result of its review, the agency last May asked wheelchair manufacturers to take steps to protect powered wheelchair users from the potential hazards of EMI. FDA required all firms to clearly label wheelchairs and scooters with the immunity level, or else state that the immunity level is not known. It also required them to label wheelchairs and scooters to warn users of the potential hazards of EMI. The agency also asked manufacturers to:

1. *Establish a minimum recommended immunity level of 20V per meter for all new motorized wheelchairs and scooters. This would provide a reasonable degree of protection against the more common sources of EMI.*
2. *Undertake an educational campaign to inform users and those who care for them about the risks of EMI and ways to avoid it; and*
3. *Solicit reports of possible EMI incidents and continue to monitor the full scope of the problem.*

FDA first learned of a possible problem with motorized wheelchairs from a complaint in June 1992. As a result, the agency began testing sample wheelchairs in its laboratories. Those tests, on several brands of power-driven wheelchairs and scooters, revealed that most—but not all—of those sampled were susceptible to interference at various radio frequencies. In some tests, the brakes released. In others, the wheels moved uncontrollably. Sometimes both occurred at once. The extent to which this happens in actual use is not known. In early 1993, FDA began inspecting facilities of all domestic and foreign motorized wheelchair and scooter manufacturers to gather information on the problem. The agency reviewed warranty and complaint files and looked at any manufacturing practices that could contribute to this type of problem. The inspections revealed numerous complaints about erratic, unintentional wheelchair movement, sometimes resulting in injuries. It is unclear, however, exactly what caused the chairs to move in those cases. In addition to EMI, unexpected movement can be caused by failure of an electronic component or by user error.

In May 1993, FDA sent letters to all U.S. manufacturers asking them to provide any information they had about possible problems with radio wave interference, including complaints, reports of injuries and studies on power-driven wheelchairs. In July 1993, the agency alerted consumer groups that represent wheelchair users about the possible problem and requested similar information. An estimated 10,000 motorized wheelchairs and 50,000 motorized scooters are sold annually in this country.

—FDA Report, August 1994

The control and minimization of EMC is a technology that is, out of necessity, growing rapidly. Manufacturers and regulatory agencies have made efforts to control this problem but the issue of meeting these ever tightening specifications is left to the system designer. EMC can no longer be a fix, designed in at the last moment, but must be a directed effort between the circuit designer, layout engineer, software engineer and purchaser. This paper will examine what can be done to reduce the chance of having a product fail EMC approval.

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2.1 The EMC World Map

Before jumping into the midst of the EMC design methods used, it is best to gain an understanding of the problem situation and review or learn applicable electromagnetic (EM) theory. To begin, look at what I call the map of the EMC world, Table I. The EMC problem is between an emission culprit and susceptible victim which are coupled through a means, either radiation through space or conducted through wires *(Figure 1)*. We can map out the EMC problem cases with columns headed by radiation and conduction, and rows headed by emission and susceptibility, to get four cases abbreviated as RE, CE, RS, CS.

TABLE I. ElectroMagnetic Compatibility Map

	Radiation	Conduction
Emission	RE	CE
Susceptibility	RS	CS

2.2 What Designers Do Upon A Discovery of an EMC Problem

Typically, the first time system designers realize that they have a RE problem is after the prototype system has been built and evaluated. Instead of being close to market release they now find themselves applying costly and often ineffective patches and going back into redesign. The steps outlined in Table II are what a typical person does at this point. First reaction is to make the printed circuit board (PCB) trace length short or to upgrade to a higher cost PCB with a full ground plane. Although most system companies have experienced and good layout design rules for their PCBs, enforcing these rules is sometimes difficult to do as more and more components are being packed into smaller packages on a smaller board. Layout is often subcontracted and the designer may not have the necessary experience and motivation, cost reduction is the goal. Next, filters (RC, RL, or ferrite beads) are added in hopes that this may fix the problem. Also, the crystal frequency may be reduced by about 2x to run the system clock at a slower rate. Software may have to be rewritten to compensate for this new time base. Software can be redone to toggle the outputs less frequently. Shielding is added or the PCB is put into an electrically out of the way place (like hiding a monster in the basement). Having exhausted their design tricks, the designers now search other semiconductor suppliers to find a quieter part. Finally, when all the time and money runs out with EMC qualification failing, the decision is made not to market the product and everyone loses business.

It is from this examination that we can understand that EMC design issues have to be considered properly at the beginning of the design cycle, in order to reduce complex design changes which must be done at the completion of the project if EMC testing is failing.

TABLE II. List of Designer Efforts to Reduce EMI Emissions

Method	Complexity	Cost	Time
1. Revise PCB Layout	Medium	Low	High
2. Add Components (Filters)	Medium	Medium	Medium
3. Change Crystal Frequency	High	Low	High
4. Rewrite Software	High	Low	High
5. Add Shielding	Low	High	Low
6. Relocate PCB	Low	Low	Low
7. Change IC Supplier	High	Medium	Medium
8. Fail EMC Qualification—Don't Sell Product	High	High	High

3.0 DESCRIPTION OF NOISE

3.1 ElectroMagnetic Interference

EMI is a form of electrical-noise pollution. Consider the time when an electric drill or some other power tool jammed a nearby radio with buzzing or crackling noise. At times it got so bad that it prevented you from listening to the radio while the tool was in use. Or the ignition of an automobile idling outside your house caused interference to your TV picture making lines across the screen or even losing sync altogether making the picture flip. These examples are annoying but are not catastrophic.

More serious, how about a sudden loss in telephone communication caused by electrical interference or noise while you are negotiating an important business deal? Now EMI can be economically damaging.

The results of EMI incidents can be even further reaching than these examples. Aircraft navigation errors resulting from EMI or interruption of air traffic controller service and may be even computer memory loss due to noise, could cause two aircraft to collide resulting in the loss of lives and property.

These were just a few instances to help identify the results of EMI in a familiar context. To help understand an EMI situation, the problem can be divided into three areas. They are the source, the victim, and the coupling path. Secondary categories involve the coupling path itself. If the source and victim are separated by space with no hard wire connection, then the coupling path may be a radiated path and we are dealing with radiated noise. If the source and victim are connected together through wires, cables, or connectors, then the coupling path may be a conducted path and we are dealing with conducted noise. It is possible for both types of noise to exist at the same time.

3.2 ElectroMagnetic Compatibility

EMI or electrical noise is of world wide concern. Governmental agencies and certain industry bodies have issued specifications with which all electrical, electromechanical, and electronic equipment must comply. These specifications and limitations are an attempt to ensure that proper EMC techniques are followed by manufacturers during the design and fabrication of their products. When these techniques are properly applied, the product can then operate and perform with other equipment in a common environment so that no degradation of performance exists due to internally or externally conducted or radiated electromagnetic emissions. This is defined as ElectroMagnetic Compatibility or EMC.

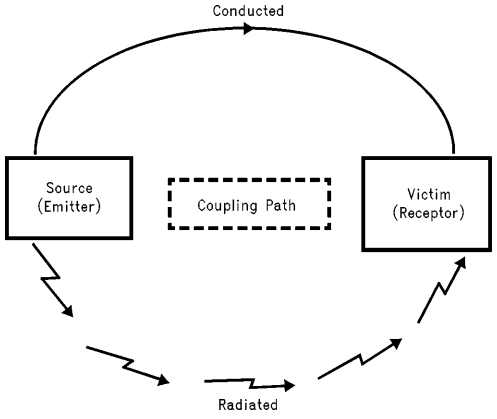

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FIGURE 1. EMI Situation

3.3 Inter-System EMI

For the purpose of this paper, when the source of noise is a module, board, or system and the victim is a different and separate module, board, or system under the design or control of a different person, it will be considered an inter-system interference situation. Examples of inter-system interference situations could be a Personal Computer interfering with the operation of a TV or an anti-lock brake module in a car causing interference in the radio. This type of interference is more difficult to contain because, as mentioned earlier, the systems are generally not designed by a single person. However, design methods and control techniques used to contain the intra-system form of EMI, which are almost always under the control of a single user, will inherently help reduce the inter-system noise.

This paper will address problems and solutions in the area of intra-system noise. Intra-system interference situations occur when the sources, victims, and coupling paths are entirely within one system, module or PCB. Systems may provide emissions that are conducted out of power lines or be susceptible to emissions conducted through them. Systems may radiate emissions through space in addition to being susceptible to radiated noise. Noise conducted out antenna leads turns into radiated noise. By the same token, radiated noise picked up by the antenna is turned into conducted noise within the system. A perfect example is a PCB ground loop, which makes an excellent antenna. The system itself is capable of degrading its own performance due to its own internal generation of conducted and radiated noise and its susceptibility to it.

Some results of EMI within a system: Noise on power lines causing false triggering of logic circuits, rapidly changing signals causing ''glitches'' on adjacent steady state signal lines (crosstalk) causing erratic operation, multiple simultaneously switching logic outputs propagating ground bounce noise throughout system, etc.

3.4 Coupling Paths

The modes of coupling an emitter source to a receptor victim can become very complicated. Remember, each EMI situation can be classified into two categories of coupling, conducted and radiated. Coupling can also result from a combination of paths. Noise can be conducted from an emitter to a point of radiation at the source antenna, then picked up at the receptor antenna by induction, and re-conducted to the victim. A further complication that multiple coupling paths presents is that it makes it difficult to determine if eliminating a suspected path has actually done any good. If two or more paths contribute equally to the problem, eliminating only one path may provide little apparent improvement.

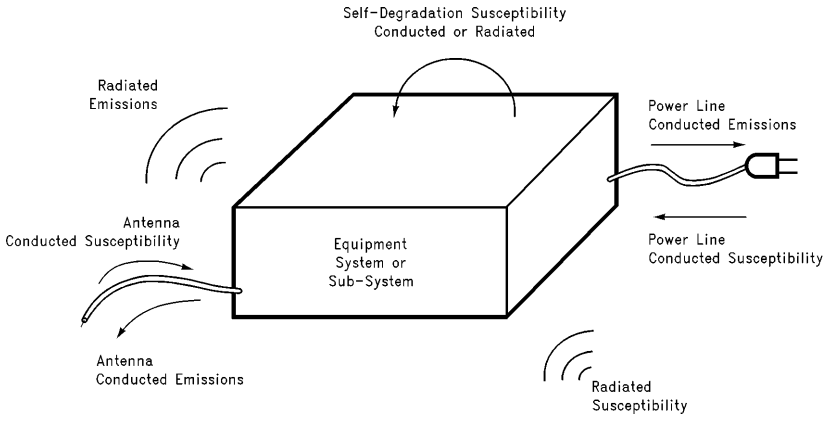

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FIGURE 2. Intra-System EMI Manifestations

3.5 Conducted Interference

In order to discuss the various ways in which EMI can couple from one system to another, it is necessary to define a few terms. There are two varieties of conducted interference which concern us. The first variety is differential-mode interference. That is an interference signal that appears between the input terminals of a circuit. The other variety of conducted interference is called common-mode interference. A common-mode interference signal appears between each input terminal and a third point, the common-mode reference. That reference may be the equipment chassis, an earth ground, or some other point.

Let's look at each type of interference individually. In *Figure 3* we show a simple circuit consisting of a signal source, V_S, and a load, R_L. In *Figure 4* we show what happens when differential-mode interference is introduced into the circuit by an outside source. As is shown, an interference voltage, V_D, appears between the two input terminals, and an interference current, I_D, flows in the circuit. The result is noise at the load. If, for instance, the load is a logic gate in a computer, and the amplitude of V_D is sufficiently high, it is possible for the gate to incorrectly change states.

Figure 5 shows what happens when a ground loop is added to our circuit. Ground loops, which are undesirable current paths through a grounded body (such as a chassis), are usually caused by poor design or by the failure of some component. In the presence of an interference source, common-mode currents, I_C, and a common-mode voltage, V_C, can develop, with the ground loop acting as the common-mode reference. The common-mode current flows on both input lines, and has the same instantaneous polarity and direction (the current and voltage are in phase), and returns through the common-mode reference. The common-mode voltage between each input and the common-mode reference is identical.

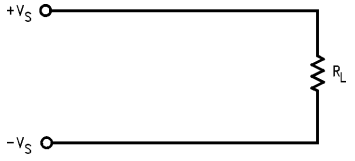

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FIGURE 3. Simple Circuit

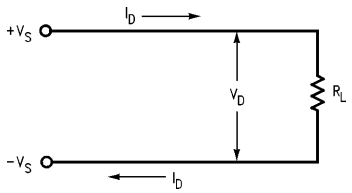

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FIGURE 4. Differential-Mode Interference

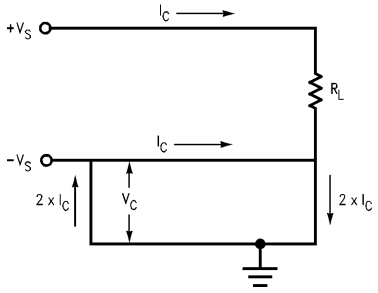

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FIGURE 5. Common-Mode Interference

3.6 Radiated Interference

Radiated coupling itself can take place in one of several ways. Some of those include field-to-cable coupling, cable-to-cable coupling, and common-mode impedance coupling. Let's look at those types of coupling one at a time.

The principle behind field-to-cable coupling is the same as that behind the receiving antenna. That is, when a conductor is placed in a time-varying electromagnetic field, a current is induced in that conductor. That is shown in *Figure 6*. In this figure, we see a signal source, V_S, driving a load, R_L. Nearby there is a current carrying wire (or other conductor). Surrounding the wire is an electromagnetic field induced by the current flowing in the wire. The circuit acts like a loop antenna in the presence of this field. As such, an interference current, I_N, and an interference voltage, V_N, are induced in the circuit. The magnitude of the induced interference signal is roughly proportional to the magnitude of the incoming field, the frequency of the incoming field, the size of the loop, and the impedance of the loop.

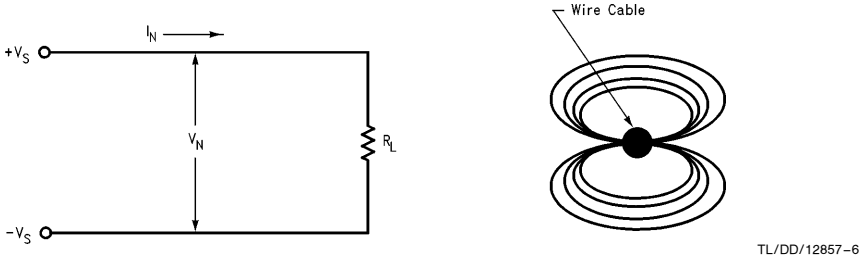

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FIGURE 6. Field-to-Cable Coupling

Cable-to-cable coupling occurs when two wires or cables are run close to each other. *Figure 7* shows how cable-to-cable coupling works. *Figure 7a* shows two lengths of cable (or other conductors) that are running side-by-side. Because any two conducting bodies have capacitance between them, called stray capacitance, a time-varying signal in one wire can couple via that capacitance into the other wire. That is referred to as capacitive coupling. This stray capacitance, as shown in *Figure 7c* makes the two cables behave as if there were a coupling capacitor between them.

Another mechanism of cable-to-cable coupling is mutual inductance. Any wire carrying a time-varying current will develop a magnetic field around it. If a second conductor is placed near enough to that wire, that magnetic field will induce a similar current in the second conductor. That type of coupling is called inductive coupling. Mutual inductance, as shown in *Figure 7b,* makes the cables behave as if a poorly wound transformer were connected between them.

In cable-to-cable coupling, either or both of those mechanisms may be responsible for the existence of an interference condition. Though there is no physical connection between the two cables, the properties we have just described make it possible for the signal on one cable to be coupled to the other. These effects, when combined are known as the transmission line effect and have been studied and described thoroughly in other texts.

The basic transmission line equations are derived for distributed parameters R (series resistance), G (shunt conductance), L (series inductance), and C (shunt capacitance), all defined per unit length of line.

Either or both of the above-mentioned properties cause the cables to be electromagnetically coupled such that a time-varying signal present on one will cause a portion of that signal to appear on the other. The ''efficiency'' of the coupling increases with frequency and inversely with the distance between the two cables. One example of cable-to-cable coupling is telephone ''crosstalk'', in which several phone conversations can be overheard at once. The term crosstalk is now commonly used to describe all types of cable-to-cable coupling.

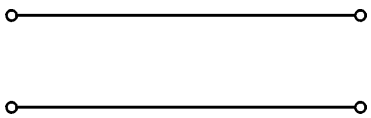

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FIGURE 7a. Parallel Conductors

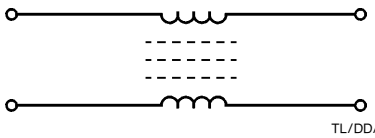

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FIGURE 7b. Inductive Coupling

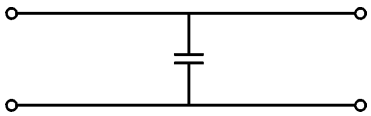

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FIGURE 7c. Capacitive Coupling

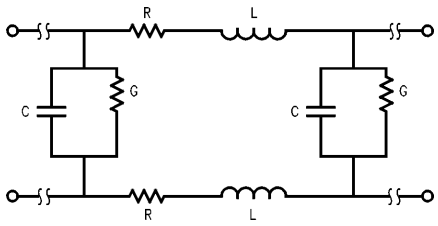

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FIGURE 7d. Transmission Line Model

Common-mode impedance coupling occurs when two circuits share a common bus or wire. In *Figure 8* we show a circuit that is susceptible to that type of coupling. In that figure a TL092 op-amp and a 555 timer share a common return or ground. Since any conductor (including a PCB trace) is not ideal, that ground will have a non-zero impedance, Z. Because of that, the current, I, from pin 1 of the 555 will cause a noise voltage, V_N, to develop; that voltage is equal to I x Z. That noise voltage will appear in series with the input to the op-amp. If that voltage is of sufficient amplitude, a noise condition will result.

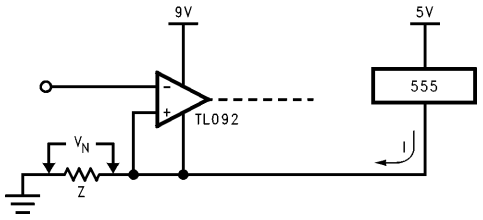

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FIGURE 8. Common-Mode Impedance Coupling

While not all inclusive, these coupling paths account for, perhaps, 98% of all intra-system EMI situations.

4.0 SOURCE OF NOISE

We will look at sources of EMI which involve components that may conduct or radiate electromagnetic energy. These sources, (component emitters), are different from the equipment and subsystems we have been talking about. Component emitters are sources of EMI which emanate from a single element rather than a combination of components such as was previously described. Actually, these component emitters require energy and connecting wires from other sources to function. Therefore, they are not true sources of EMI, but are EMI transducers. They convert electrical energy to electromagnetic noise.

4.1 Cables and Connectors

The three main concerns regarding the EMI role of cables are conceptualized in *Figure 9.* They act as (1) radiated emission antennae, (2) radiated susceptibility antennae, and (3) cable-to-cable or crosstalk couplers. Usually, whatever is done to harden a cable against radiated emission will also work in reverse for controlling EMI radiated susceptibility. The reason for this is usually, when differential-mode radiated emission or susceptibility is the failure mode, twisting leads and shielding cables reduces EMI. If the failure mechanism is due to common-mode currents circulating in the cable, twisting leads has essentially no effect on the rela-

tionship between each conductor and the common-mode reference. Cable shields may help or aggravate EMI depending upon the value of the transfer impedance of the cable shield. Transfer impedance is a figure of merit of the quality of cable shield performance defined as the ratio of coupled voltage to surface current in Ω/meter. A good cable shield will have a low transfer impedance. The effectiveness of the shield also depends on whether or not the shield is terminated and, if so, how it is terminated.

Connectors usually are needed to terminate cables. When no cable shields or connector filters or absorbers are used, connectors play essentially no role in controlling EMI. The influence of connector types, however, can play a major role in the control of EMI above a few MHz. This applies especially when connectors must terminate a cable shield and/or contain lossy ferrites or filter-pins.

Connectors and cables should be viewed as a system to cost-effectively control EMI rather than to consider the role of each separately, even though each offers specific interference control opportunities.

4.2 Components

Under conditions of forward bias, a semiconductor stores a certain amount of charge in the depletion region. If the diode is then reverse-biased, it conducts heavily in the reverse direction until all of the stored charge has been removed as shown in *Figure 10*. The duration, amplitude, and configuration of the recovery-time pulse (also called switching time or period) is a function of the diode characteristics and circuit parameters. These current spikes generate a broad spectrum of conducted transient emissions. Diodes with mechanical imperfections may generate noise when physically agitated. Such diodes may not cause trouble if used in a vibration-free environment.

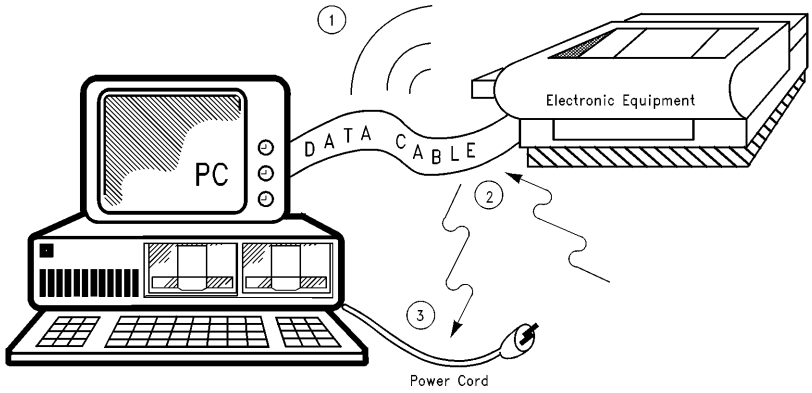

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FIGURE 9. Cables and Connectors

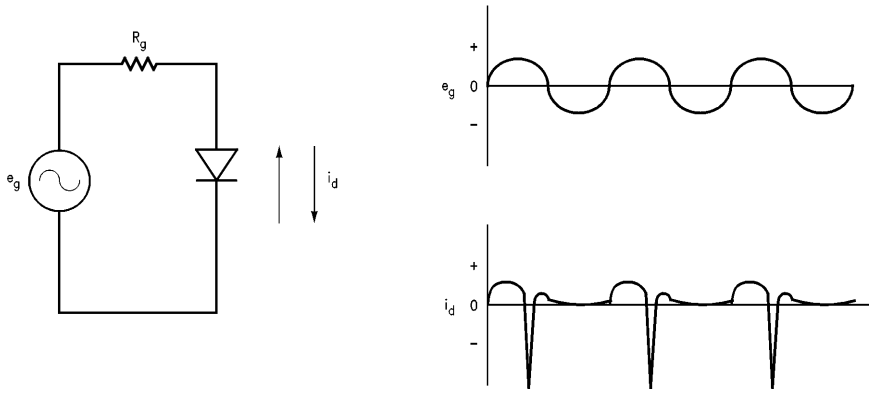

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FIGURE 10. Diode Recovery Periods and Spikes

4.3 Power Supply Noise

Power-supply spiking is perhaps the most important contributor to system noise. When any element switches logic states, it generates a current spike that produces a voltage transient. If these transients become too large, they can cause logic errors because the supply voltage drop upsets internal logic, or because a supply spike on one circuit's output feeds an extraneous noise voltage into the next device's input.

With CMOS logic in its quiescent state, essentially no current flows between V_{CC} and ground. But when an internal gate or an output buffer switches state, a momentary current flows from V_{CC} to ground. The switching transient caused by an unloaded output changing state typically equals 20 mA peak. Using the circuit shown in *Figure 11,* you can measure and display these switching transients under different load conditions.

Figure 12a shows the current and voltage spikes resulting from switching a single unloaded ($C_L = 0$ in *Figure 11*) NAND gate. These current spikes, seen at the switching edges of the signal on V_{IN}, increase when the output is loaded. *Figures 12b, 12c,* and *12d* show the switching transients when the load capacitance, C_L, is 15 pF, 50 pF, and 100 pF, respectively. The large amount of ringing results from the test circuit's transmission line effects. This ringing occurs partly because the CMOS gate switches from a very high impedance to a very low one and back again. Even for medium-size loads, load capacitance current becomes a major current contributor.

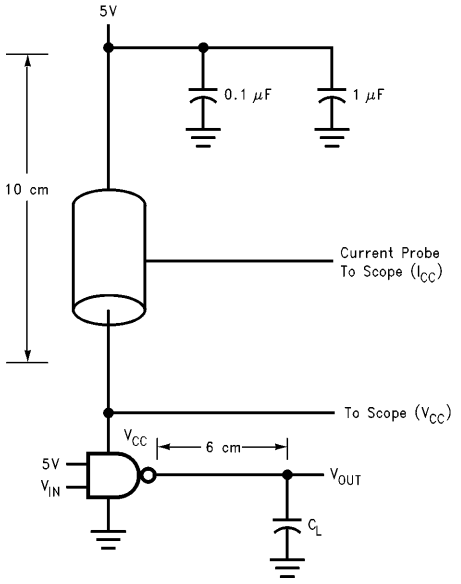

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FIGURE 11. Test Circuit

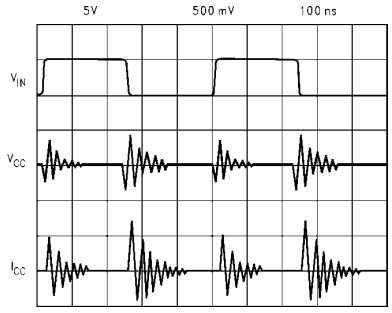

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FIGURE 12a. V_{IN}, V_{CC}, I_{CC} for $C_L = 0$ pF

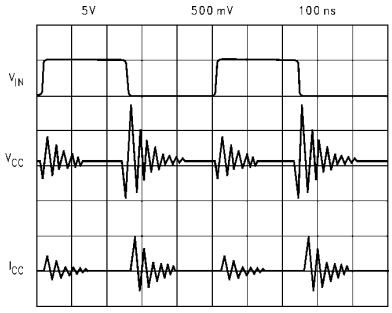

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FIGURE 12b. V_{IN}, V_{CC}, I_{CC} for $C_L = 15$ pF

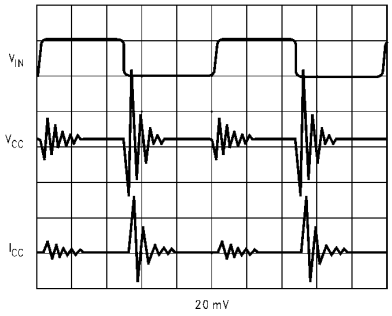

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FIGURE 12c. V_{IN}, V_{CC}, I_{CC} for $C_L = 50$ pF

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FIGURE 12d. V_{IN}, V_{CC}, I_{CC} for $C_L = 100$ pF

Although on standard CMOS logic internal gates generate current spikes when switching, the bulk of a spike's current comes from output circuit transitions. *Figure 13* shows the I_{CC} current for a NAND gate, as shown in the test circuit, with one input switching and the other at ground resulting in no output transitions. Note the very small power-supply glitches provoked by the input-circuit transitions.

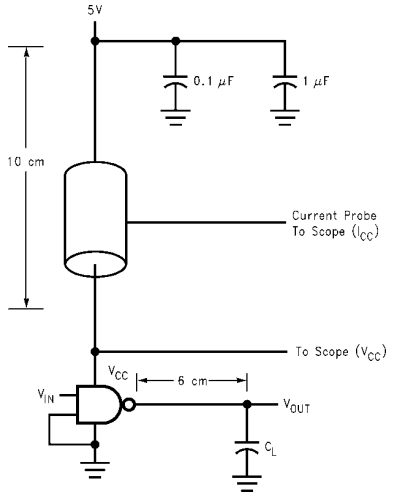

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FIGURE 13a. Test Circuit

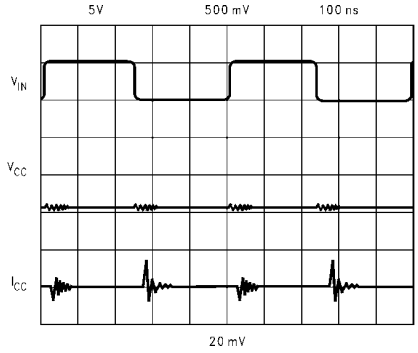

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FIGURE 13b. V_{IN}, V_{CC}, I_{CC}

4.4 High Speed CMOS Logic Switching

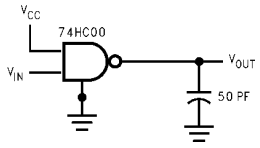
The magnitude of noise which can be tolerated in a system relates directly to the worst case noise immunity specified for the logic family. Noise immunity can be described as a device's ability to prevent noise on its input from being transferred to its output. It is the difference between the worst case output levels (V_{OH} and V_{OL}) of the driving circuit and the worst case input voltage requirements (V_{IH} and V_{IL}, respectively) of the receiving circuit.

Using Table III as a guide, it can be seen that for TTL (LS or ALS) devices the worst case noise immunity is typically 700 mV for the high logic level and 300 mV for the low logic level. For HCMOS devices the worst case noise immunity is typically 1.75V for high logic levels and 800 mV for low logic levels. AC high speed CMOS logic families have noise immunity of 1.75V for high logic levels and 1.25V for low logic levels. ACT CMOS logic families have noise immunity of 2.9V for high logic levels and 700 mV for low logic levels.

TABLE III. Logic Family Comparisons

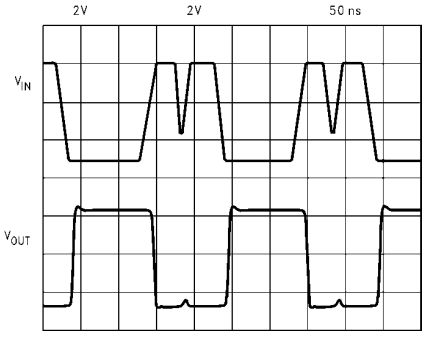
Characteristic	Symbol	LS/ALS/TTL	HCMOS	AC	ACT
Input Voltage (Limits)	V_{IH} (Min)	2.0V	3.15V	3.15V	2.0V
	V_{IL} (Max)	0.8V	0.9V	1.35V	0.8V
Output Voltage (Limits)	V_{OH} (Min)	2.7V	$V_{CC}-0.1V$	$V_{CC}-0.1V$	$V_{CC}-0.1V$
	V_{OL} (Max)	0.5V	0.1V	0.1V	0.1V

To illustrate noise margin and immunity, *Figures 14b* and *14c* show the output that results when you apply several types of simulated noise to a 74HC00's input, *Figure 14a*. Typically, even 2V or more input noise produces little change in the output. The top trace shows noise present on the input logic level signal and the bottom trace shows resultant noise induced on the output logic level signal.



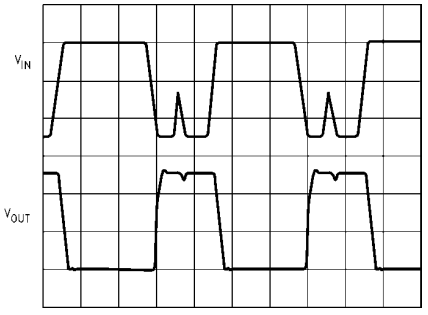
TL/DD/12857–23

FIGURE 14a. Test Circuit



TL/DD/12857–24

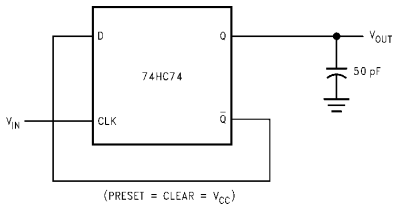
FIGURE 14b. V_{IN}, V_{OUT}



TL/DD/12857–25

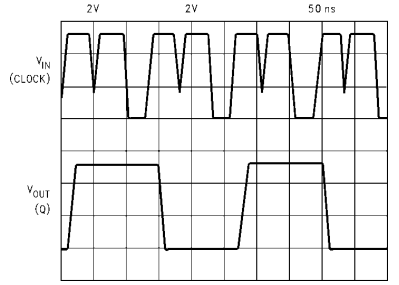
FIGURE 14c. V_{IN}, V_{OUT}

Figure 15b shows how noise affects 74HC74's clock input. Again, no logic errors occur with 2V or more of noise on the clock input.



TL/DD/12857–21

FIGURE 15a. Test Circuit



TL/DD/12857–22

FIGURE 15b. V_{IN}, V_{OUT}

When using high speed CMOS, even with its greater noise immunity, crosstalk, induced supply noise and noise transients become factors. Higher speeds allow the device to respond more quickly to externally induced noise transients and accentuate the parasitic interconnection inductances and capacitances that increase self-induced noise and crosstalk.

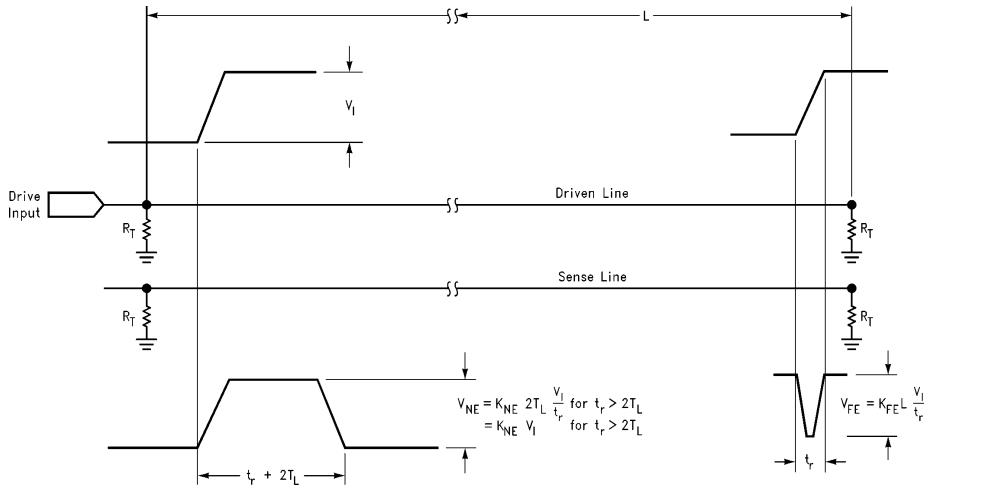
4.5 Signal Crosstalk

The problem of crosstalk, and how to deal with it, is becoming more important as system performance and board densities increase. Our discussion on cable-to-cable coupling described crosstalk as appearing due to the distributed capacitive coupling and the distributed inductive coupling between two signal lines. When crosstalk is measured on an undriven sense line next to a driven line (both terminated at their characteristic impedances), the near end crosstalk and the far end crosstalk have quite distinct features, as shown in *Figure 16.* It should be noted that the near end component reduces to zero at the far end and vice versa. At any point in between, the crosstalk is a fractional sum of the near and far end crosstalk waveforms as shown in the figure. It also can be noted that the far end crosstalk can have either polarity whereas the near end crosstalk always has the same polarity as the signal causing it.

The amplitude of the noise generated on the undriven sense line is directly related to the edge rates of the signal on the driven line. The amplitude is also directly related to the proximity of the two lines. This is factored into the coupling constants K_{NE} and K_{FE} by terms that include the distributed capacitance per unit length, the distributed inductance per unit length, and the length of the line. The lead-to-lead capacitance and mutual inductance thus created causes ''noise'' voltages to appear when adjacent signal paths switch.

Several useful observations that apply to a general case can then be made:

- The crosstalk always scales with the signal amplitude V_I.
- Absolute crosstalk amplitude is proportional to slew rate V_I/t_r not just $1/t_r$.
- Far end crosstalk width is always t_r.
- For $t_r << 2\ T_L$, where t_r is the transition time of the signal on the driven line and T_L is the propagation or bus delay down the line, the near end crosstalk amplitude, V_{NE}, expressed as a fraction of signal amplitude, V_I, is K_{NE} which is a function of physical layout only.
- The high the value of ''t_r'' (slower transition times) the lower the percentage of crosstalk (relative to signal amplitude).



TL/DD/12857–26

FIGURE 16. Crosstalk

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than about three times the propagation delay of the line. Significant transmission line properties may be exhibited, for example, where devices having edge rates of 3 ns (or less) are used to drive traces of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

4.6 Signal Interconnects

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{OE}, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_O and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{OE} and t_{pde} can be calculated with:

$$Z_{OE} = \frac{Z_o}{\sqrt{1 + C_t/C_l}}$$

$$t_{pde} = t_{pd}\sqrt{1 + C_t/C_l}$$

where C_i = intrinsic line capacitance

C_t = additional capacitance due to gate loading.

These formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. As was mentioned earlier, lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signal quality on all of the lines.

4.7 Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bond wires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced. One of these parasitic electrical characteristics is the inductance found in all leadframe materials.

Figure 17 shows a simple circuit model for a CMOS device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

The three waveforms shown represent how ground bounce is generated. The top waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, and the inductors L1 and L3, and C_L, the load capacitance. In order to change the output from a HIGH to a LOW, current must flow to discharge the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = -C_L{*}(dV/dt)$]. This current, as it changes, causes a voltage to be generated across the inductances in the circuit. The formula for the voltage across an inductor is $V = L(dI/dt)$. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{GB} = L1{*}(dI/dt)$]. This induced voltage creates what is known as ground bounce.

Because the inductor is between the external system ground and the internal device ground, the induced voltage causes the internal ground to be at a different potential than the external ground. This shift in potential causes the device inputs and outputs to behave differently than expected because they are referenced to the internal device ground, while the devices which are either driving into the inputs or being driven by the outputs are referenced to the their own device ground. External to the device, ground bounce causes input thresholds to shift and output levels to change.

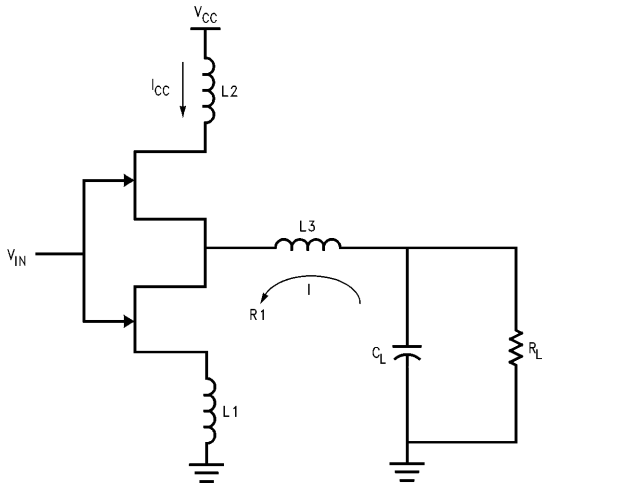


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FIGURE 17a. Test Circuit for Ground Bounce

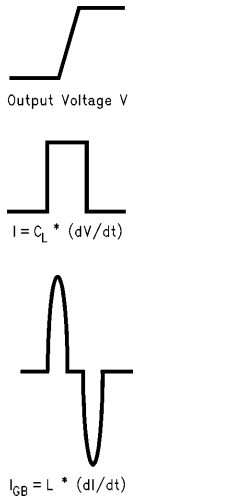

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FIGURE 17b. V_{IN}, V_{CC}, I_{CC}

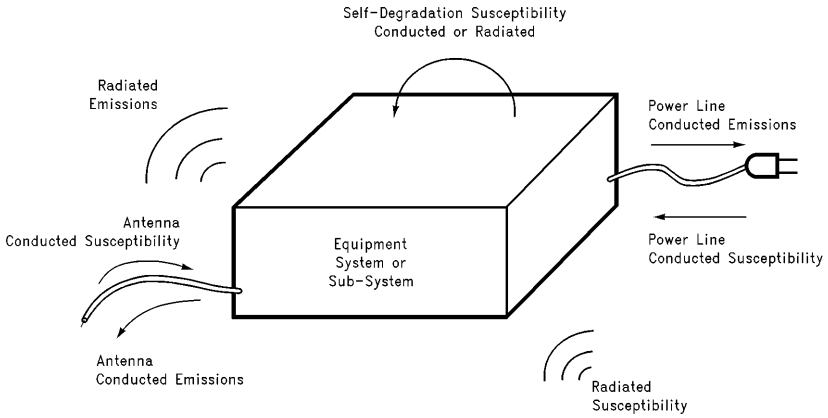

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FIGURE 18. Intra-System EMI Manifestations

Although this discussion is limited to ground bounce generated during HIGH-to-LOW transitions, it should be noted that the ground bounce is also generated during LOW-to-HIGH transitions. This ground bounce though, has a much smaller amplitude and therefore does not present the same concern.

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60 pF–70 pF, increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load itself. Moving the load away from the output also reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away due to effectively lower L1 and L3.
- Voltage: lowering V_{CC} reduces ground bounce.

Ground bounce produces several symptoms:

- Altered device states.
- Propagation delay degradation.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.

5.0 NOISE SUPPRESSION TECHNIQUES

EMI control techniques involve both hardware implementations/methods and procedures. They may also be divided into intra-system and inter-system EMI control. Our major concern in this paper is intra-system EMI control, however, an overview of each may be appropriate at this time.

Figure 18 illustrates the basic elements of concern in an intra-system EMI problem. The test specimen may be a single box, an equipment, subsystem or system (an ensemble of boxes with interconnecting cables). From a strictly nearsighted or selfish point-of-view, the only EMI concern would appear to be degradation of performance due to self jamming such as suggested at the top of the figure. While this might be the primary emphasis, the potential problems associated with either (1) susceptibility to outside conducted and/or radiated emissions or (2) tendency to pollute the outside world from its own undesired emissions, come under the primary classification of intra-system EMI. Corresponding EMI-control techniques, however, address themselves to both self-jamming and emission/susceptibility in accordance with applicable EMI specifications. The techniques that will be discussed include filtering, shielding, wiring and grounding.

Inter-system EMI distinguishes itself by interference between two or more discrete and separate systems or platforms which are frequently under independent user control. Culprit emissions and/or susceptibility situations are divided into two classes: (1) antenna entry/exit and (2) back-door entry/exit. More than 95% of inter-system EMI problems involve the antenna entry/exit route of EMI. We can group inter-system EMI-control techniques by four fundamental categories: frequency management, time management, location management and direction management.

The first step in determining a solution is to identify the problem as either inter-system or intra-system EMI. Generally, if the specimen has an antenna and the problem develops from what exits or enters the antenna from another specimen or ambient, then the problem is identified as inter-system EMI. Otherwise, it is intra-system EMI which we will discuss now.

5.1 Intra-System EMI Control Techniques

5.1.1 Shielding

Shielding is used to reduce the amount of electromagnetic radiation reaching a sensitive victim circuit. Shields are made of metal and work on the principle that electromagnetic fields are reflected and/or attenuated by a metal surface. Different types of shielding are needed for different types of fields. Thus, the type of metal used in the shield and the shield's construction must be considered carefully if the shield is to function properly. The ideal shield has no holes or voids and, in order to accommodate cooling vents, buttons, lamps and access panels, special meshes and ''EMI-hardened'' components are needed.

TABLE IV. Effective Shielding for Different Materials

Shielding Material	Surface Resistance (Ω/square)	Shielding Effectiveness dB		
		At 10 MHz	At 100 MHz	At 1 GHz
Arc-Sprayed Zinc	0.002	106	92	98
Silver Acrylic Paint	0.004	67	93	97
Silver Deposition	0.05	57	82	89
Silver Epoxy Paint	0.1	59	81	87
Nickel Composite	3.0	35	47	57
Carbon Composite	10.0	27	35	41
Wire Screen (0.64 mm Grid)	N.A.	86	66	48

Effectiveness of shielding materials with 25 μm thickness and for frequencies for which the largest dimension of the shielding plate is less than a quarter of a wavelength.

Once a printed-circuit board design has been optimized for minimal EMI, residual interference can be further reduced if the board is placed in a shielded enclosure. A box's shielding effectiveness depends on three main factors: its skin, the control of radiation leakage through the box's apertures or open areas (like cooling holes) and the use of filters or shields at interconnection points depending on shield grounding.

A box skin is typically fabricated from sheet metal or metallized plastic. Normally sheet metal skin that is 1 mm thick is more than adequate; it may have a shielding effectiveness of more than 100 dB throughout the high-frequency spectrum from 1 MHz to 20 GHz. Conductive coatings on plastic boxes are another matter. Table IV shows that at 10 MHz the shielding effectiveness can be as low as 27 dB if a carbon composite (cheap) is used, or it can run as high as 106 dB for zinc sprayed on plastic by an electric arc process (expensive). Plastic filled materials or composites having either conductive powder, flakes, or filament are also used in box shielding; they have an effectiveness similar to that of metallized plastics.

In many cases shielding effectiveness of at least 40 dB is required of plastic housings for microcontroller-based equipment to reduce printed-circuit board radiation to a level that meets FCC regulations in the United States or those of the VDE in Europe. Such skin shielding is easy to achieve. The problem is aperture leakage. The larger the aperture, the greater its radiation leakage because the shield's natural attenuation has been reduced. On the other hand, multiple small holes matching the same area as the single large aperture can attain the same amount of cooling with little or no loss of attenuation.

5.1.2 Filtering

Filters are used to eliminate conducted interference on cables and wires, and can be installed at either the source or the victim. *Figure 19* shows an AC power-line filter. The values of the components are not critical; as a guide, the capacitors can be between 0.01 and 0.001 μF, and the inductors are nominally 6.3 μH. Capacitor C1 is designed to shunt any high-frequency differential-mode currents before they can enter the equipment to be protected. Capacitors C2 and C3 are included to shunt any common-mode currents to ground. The inductors, L1 and L2, are called common-mode chokes, and are placed in the circuit to impede any common-mode currents.

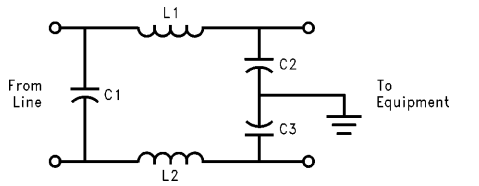

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FIGURE 19. Filtering

5.1.3 Wiring

Now that the equipment in each box can be successfully designed to combat EMI emission and susceptibility separately, the boxes may be connected together to form a system. Here the input and output cables and, to a lesser extent, the power cable form an ''antenna farm'' that greatly threatens the overall electromagnetic compatibility of the system. Most field remedies for EMI problems focus on the coupling paths created by the wiring that interconnects systems. By this time most changes to the individual equipment circuits are out of the question.

Let us address five coupling paths that are encountered in typical systems comprised of two or more pieces of equipment connected by cables. These should adequately cover most EMI susceptibility problems. They are:

- common ground impedance coupling—a conducting path in which a common impedance is shared between an undesired emission source and the receptor.
- common-mode, radiated field-to-cable coupling—electromagnetic fields penetrate a loop formed by two pieces of equipment, a cable connecting them, and a ground plane.
- differential-mode, radiated field-to-cable coupling—the electromagnetic fields penetrate a loop formed by two pieces of equipment and an interconnecting transmission line or cable.
- crosstalk coupling—signals in one transmission line or cable are capacitively or inductively coupled into another transmission line.
- conductive path—through power lines feeding the equipment.

The first coupling path is formed when two pieces of equipment are connected to the same ground conductor at different points, an arrangement that normally produces a volt-

age difference between the two points. If possible, connecting both pieces of equipment to a single-point ground eliminates this voltage. Another remedy is to increase the high frequency impedance along a loop that includes the path between the ground connections of the two boxes. Examples include the isolation of printed-circuit boards from their cabinet or case, the use of a shielded isolation transformer in the signal path, or the insertion of an inductor between one or both boxes and the ground conductor. The use of balanced circuits, differential line drivers and receivers, and absorbing ferrite beads and rods on the interconnecting cable can further reduce currents produced by this undesirable coupling path.

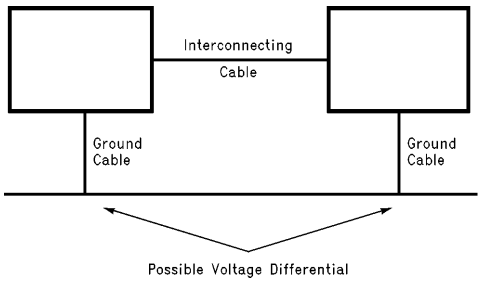

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FIGURE 20. Common Ground Impedance Coupling

A balanced circuit is configured so its two output signal leads are electrically symmetrical with respect to ground, as the signal increases on one output, the signal on the other decreases. Differential line drivers produce a signal that is electrically symmetrical with respect to ground from a single-ended circuit in which only one lead is changing with respect to ground. Ferrite beads, threaded over electrical conductors, substantially attenuate electromagnetic interference by turning radio-frequency energy into heat, which is dissipated in them.

In the second coupling path, a radiated electromagnetic field is converted into a common-mode voltage in the ground plane loop containing the interconnect cable and both boxes. This voltage may be reduced if the loop area is trimmed.

Ferrite beads and ferrite filtered connectors applied to the interconnecting cable can help reduce common mode currents.

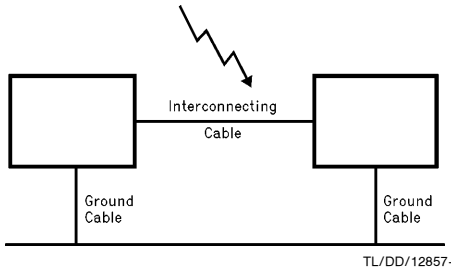

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FIGURE 21. Common-Mode, Radiated Field-to-Cable Coupling

The third coupling path produces a differential-mode voltage that appears across the input terminals of the EMI receptor. One way of controlling this is to cancel or block the pickup of differential-mode radiation. In a balanced transmission line, this is done by use of twisted-wire pairs and a shielded cable.

For crosstalk, the fourth coupling path, the reduction of capacitive coupling, can be achieved by the implementation of at least one of these steps:

- Reducing the spacing between wire pairs in either or both of the transmission lines.
- Increasing the separation between the two transmission lines.
- Reducing the frequency of operation of the source, if possible.
- Adding a cable shield over either or both transmission lines.
- Twisting the source's or receptor's wire pairs.
- Twisting both wire pairs in opposite directions.

The fifth coupling path conductively produces both common-mode and differential-mode noise pollution on the power mains. Among several remedies that can suppress the EMI there are filters and isolation transformers.

There are only about 50 common practical remedies that can be used in most EMI situations. Of these, about 10 suffice in 80 percent of the situations. Most engineers are aware of at least some of these remedies—for example, twisting wires to reduce radiation pickup.

In order to attack the EMI problem, one can make use of the information contained in Tables V and VI. First, decide what coupling path has the worst EMI interference problem. From the 11 most common coupling paths listed at the top of the table, find the problem coupling path. Using the numbers found in that table entry, locate the recommended remedy or remedies from the 12 common EMI fixes identified at the bottom of the table. This procedure should be repeated until all significant coupling paths have been properly controlled and the design goal has been met.

TABLE V. Electromagnetic Interference Coupling Paths

Problem	Solution (See Table VI)
Radiated Field to Interconnecting Cable (Common-Mode)	2, 7, 8, 9, 11
Radiated Field to Interconnecting Cable (Differential-Mode)	2, 5, 6
Interconnecting Cable to Radiated Field (Common-Mode)	1, 3, 9, 11
Interconnecting Cable to Radiated Field (Differential-Mode)	1, 3, 5, 6, 7
Cable-to-Cable Crosstalk	1, 2, 3, 4, 5, 6, 10, 11
Radiated Field to Box	12, 13
Box to Radiated Field	12, 13
Box-to-Box Radiation	12, 13
Box-to-Box Conduction	1, 2, 7, 8, 9
Power Mains to Box Conduction	4, 11
Box to Power Mains Conduction	4, 11
Electromagnetic Interference Coupling Paths	4

TABLE VI. Electromagnetic Interference Fixes

Solution	Complexity	Cost
1. Insert Filter in Signal Source	Low	Medium
2. Insert Filter in Signal Receptor	Low	Medium
3. Insert Filter in Power Source	Low	Medium
4. Insert Filter in Power Receptor	Low	Medium
5. Twist Wire Pair	Low	Low
6. Shield Cable	Low	Medium
7. Use Balanced Circuits	Medium	Medium
8. Install Differential Line Drivers and Receivers	Medium	Medium
9. Float Printed Circuit Board(s)	Medium	Medium
10. Separate Wire Pair	Low	Medium
11. Use Ferrite Beads	Low	Medium
12. Use a Multilayer Instead of a Single Layer Printed Circuit Board(s)	Medium	High

5.2 Inter-System EMI-Control Techniques

There are many EMI controls that may be carried out to enhance the chances of inter-system EMC. They can be grouped into four categories which we will discuss briefly. The following discussion is not intended to be complete but merely provide an overview of some EMI control techniques available to the inter-system designer and user.

5.2.1 Frequency Management

Frequency management suggests both transmitter emission control and improvement of receptors against spurious responses. The object is to design and operationally maintain transmitters so that they occupy the least frequency spectrum possible in order to help control electromagnetic pollution. For example, this implies that long pulse rise and fall times should be used. Quite often one of the most convenient, economic and rapid solutions to an EMI problem in the field, is to change frequency of either the victim receiver or the culprit source.

5.2.2 Time Management

In those applications where information is passed between systems, a possible time management technique could be utilized where the amount of information transferred is kept to a minimum. This should reduce the amount of time that the receptor is susceptible to any EMI. In communication protocols, for example, essential data could be transmitted in short bursts or control information could be encoded into fewer bits.

5.2.3 Location Management

Location management refers to EMI control by the selection of location of the potential victim receptor with respect to all other emitters in the environment. In this regard, separation distance between transmitters and receivers is one of the most significant forms of control since interfering source emissions are reduced greatly with the distance between them. The relative position of potentially interfering transmitters to the victim receiver are also significant. If the emitting source and victim receiver are shielded by obstacles, the degree of interference would be substantially reduced.

5.2.4 Direction Management

Direction management refers to the technique of EMI control by gainfully using the direction and attitude of arrival of electromagnetic signals with respect to the potential victim's receiving antennae.

6.0 SILICON CHANGES

If we examine the modes of EMI emissions and the methods of suppression that were described, on standard CMOS silicon the techniques are exactly the same for what occurs on a PCB. What silicon design engineers at National Semiconductor's Embedded Technologies Division noticed, was that a majority of the EMI emitted from a controller or processor is caused by the transient I_{CC} current flowing in the loop formed from the bypass capacitor to the V_{CC} pin and out of the GND pin. When this current was measured by inserting a 1Ω resistor in this path, a 40 mA (10 ns) current spike was revealed at every clock edge (repetition rate = 2x clock frequency). This occurred even when outputs were toggling or tristated, and instructions that were being executed had very little impact on the magnitude or duration of the spike.

6.1 Chip Problems

Let's note the four items that produce higher amplitude and frequency fundamental and harmonics: large amplitude change, fast rise time or fall time, high repetition rate and finally large pulse width (a 50% duty cycle). Table VII lists these.

TABLE VII. IC Chip Problems

1. Large Amplitude Change
2. Fast Rise or Fall Time
3. High Repetition Rate
4. Large Pulse Width (i.e. 50% Duty Cycle).

As a rule, the waveforms di/dt (rate of change of current) and dv/dt (rate of change of voltage) must be kept to a minimum. If a silicon design engineer could shape both current and voltage waveforms around the device, these problems would be solved. If we look at the current and voltage problems separately, we can solve them both and decrease radiated emissions by more than 20 dB.

But, what about the antennae responsible for radiation? This is where packaging technology comes into the picture. The loop size of a typical system is approximately greater

than 90% PCB trace dimensions plus IC package dimensions and less than 10% IC chip dimensions, which both factor into the antenna gain. Therefore the IC package design should obey several rules, see Table VIII. First a ground pin (current return) adjacent to each power pin will minimize the loop sizes and simplify layout of decoupling circuits. Also an output pin which sources or sinks a large and frequent di/dt (for example crystal or clock pins) should also be adjacent to the power/ground pin pair to keep its current loops small. It helps to have small package dimensions. A last point is that sharing of a common power/ground should be limited to prevent their voltage from bouncing due to the total Ldi/dt + iR. This bouncing is conducted to inputs sharing the common power/ground which in several cases are susceptible since their V_{IH} and V_{IL} trip points are referenced to it. The bouncing is conducted through non-tristated outputs sharing this common power/ground and is passed on outside the IC as additional conducted and radiated emissions from bouncing V_{OH} or V_{OL} levels.

TABLE VIII. Package and PCB Traces form Loop or Whip Antennae which Radiate

1. Ground pin (current return) not adjacent to power pin). Pair should be together.
2. Power/Ground pair not adjacent to output pin (especially crystal of clock pins).
3. Too much sharing of common power/ground having voltage bounce due to its total Ldi/dt+iR. a. Conducted emissions to susceptible I/O b. Radiated emissions from susceptible I/O.
4. Large package dimensions.

6.2 Silicon Design Changes

National's design goal was to reshape the IC pin current waveforms from their original values as follows: I_{CC} pulses to 3X rise time, 0.2X amplitude and 5X width; I_{OL} and I_{OH} pulses to 10X rise time. A second goal is to provide separate power and ground bus systems on-chip for each of the following groups: Chip digital logic, Chip I/O buffers, and if present a chip A/D converter (or other analog intensive sections). This is an extension of proper IC packaging pinout covered earlier to prevent conducted emissions to susceptible circuitry.

Inspection of these goals leads us to divide the chip into separate areas which we named the nucleus, the perimeter and the A/D. Also the partitioning of the nucleus (containing the digital logic functions) and the perimeter (containing digital I/O, oscillator and comparator functions) allows use of an on-chip device to choke the nucleus' I_{CC} current, thereby wave shaping the I_{CC}. The I_{CC} choke, however, causes the nucleus V_{CC} voltage to dip by 0.5V to 1V at each clock edge. These V_{CC} voltage swings will be confined to within the chip's nucleus where the circuitry (digital logic) is tolerant and no significant radiation antennae exist.

On-chip level shifting circuitry is inserted as interface between the nucleus and the perimeter. It permits the nucleus to operate at a lower V_{CC} than the perimeter. This permits the nucleus V_{CC} to come through the on-chip I_{CC} choke emerging as a bouncing V_{CC}.

In general, outputs toggle much less frequently than the clock. This rate is limited by software execution rates. However, for the case of a clock or address/data bus outputs this may not be the case. Looking at time domain EMI instead of frequency domain EMI (which may have some time averaging) may motivate one to take action and reduce EMI from the chip's output drivers. CMOS output drivers turn on fast, in about 1 ns. This causes 2 problems. The first is called ''shoot through'' current which flows from DV_{CC} to DGND when both the pull up and the pull down drivers are on and the output load is small. The second is due to output current magnitude increasing to maximum in about 1 ns when the output changes state. Both problems are solved by using fast turn off, gradual turn on device drivers.

Figure 22 illustrates, in block diagram form, how the chip is partitioned for EMC. Note that the level shifter block is multichannel, and most channels need dedicated level shifting devices in one direction only as shown. The power/ground pads named DV_{CC} (Driver V_{CC}), LV_{CC} (Logic V_{CC}), V_{CC} (a global V_{CC} to most of the chip), GND (a global GND to most of the chip) and DGND (driver ground) are all available. To minimize package pin count, DV_{CC} and LV_{CC} can be bonded to the same pin, GND and DGND can be bonded to the same pin, and the V_{CC} pad is not bonded. A higher pin count package is used to bring out each pad to a separate pin to allow study of the several packaging options. The V_{CC} pad is not bonded when utilizing the on-chip I_{CC} choke to prevent RE (radiated emissions) from V_{CC} bounce.

Three operating modes can be evaluated with GND and DGND pads always connected together to 0V. The first mode applies 5V to DV_{CC}, LV_{CC} and V_{CC} to check the RE improvements due to gradual turn on outputs alone. The second mode applies 5V to DV_{CC} and LV_{CC} where V_{CC} floats as a test point. This checks the RE improvements due to gradual turn on and I_{CC} choking. The third mode applies 5V to DV_{CC} and 3V to V_{CC} and LV_{CC} to check the RE improvement in this mode which actually requires a V_{CC} additional package pin.

TABLE IX. Results of Various Pinout Configurations

Chip Pads	Configuration A	Configuration B	Configuration C
DV_{CC}	5V	5V	5V
LV_{CC}	5V	5V	3V
V_{CC}	5V	Test Point	3V
GND	0	0	0
DGND	0	0	0
EMI	Baseline	−20 dB	−6 dB
Clock Speed	10 MHz	>5 MHz	4 MHz

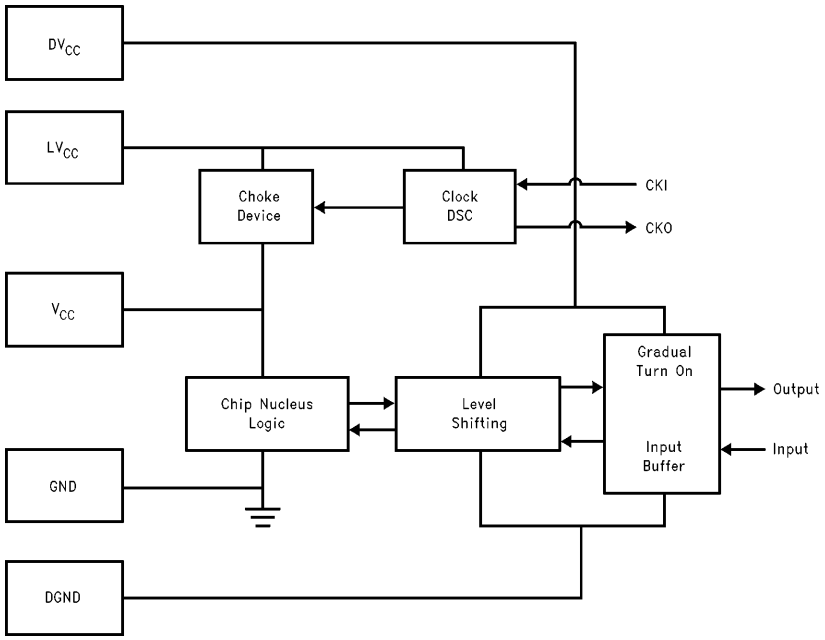

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FIGURE 22. Block Diagram of EMC Circuitry

6.3 Packaging Changes

Recalling our IC packaging rules for EMC, and upon reviewing the packaging pitfalls (Table VIII), one can now appreciate an IC package build sheet *(Figure 23)* that illustrates how to bond out and pin out the five power/ground pads on the die. As advised, power pins having current return ground pins adjacent are LV_{CC} and GND, V_{CC} and GND; but DV_{CC} and DGND are not adjacent. This is permitted since DV_{CC} current is returned via output high pins (not DGND), also DGND current is sourced via output low pins. Therefore placing DV_{CC} adjacent to DGND does not contribute to small area current loops. Note that CKI, CKO, LV_{CC}, and GND are all adjacent pins for the sake of clustering the oscillator external tank circuit into the smallest current loop area. Since the oscillator is supplied through LV_{CC} and GND, added benefit of running both oscillator and nucleus at 3V is possible if one were to choose defeating the on-chip choke by shorting LV_{CC} to V_{CC} in the choke block.

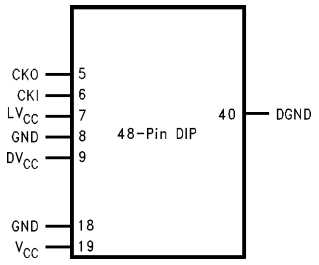

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FIGURE 23. EMC Pinout

6.4 Results of IC Circuit Changes

Simulations give an idea of the expected improvement from addition of the I_{CC} choke on the silicon. *Figure 24a* shows actual I_{CC} as measured by a series resistance during switching transients. Simulation of an equivalent circuit with the addition of the choke predicts a decrease of I_{CC} from about 37 mA to less than 4 mA.

This decrease of 10x would imply a 20 dB improvement in gross emissions.

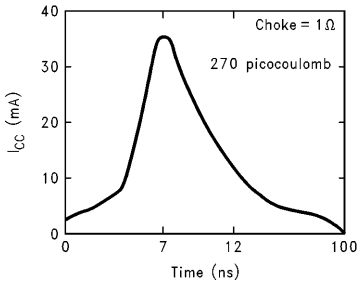

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FIGURE 24a. Original I_{CC}

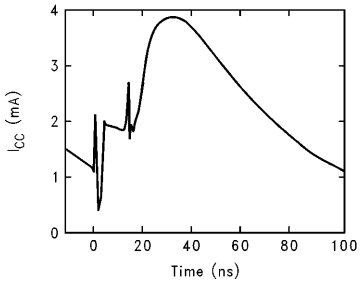

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FIGURE 24b. I_{CC} with Improvements

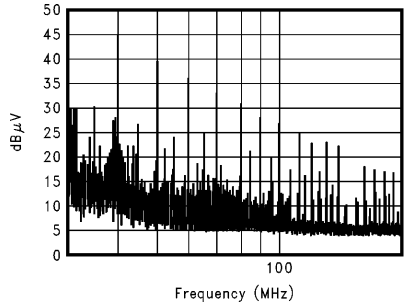

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FIGURE 25a. Emissions without V_{CC} Choke

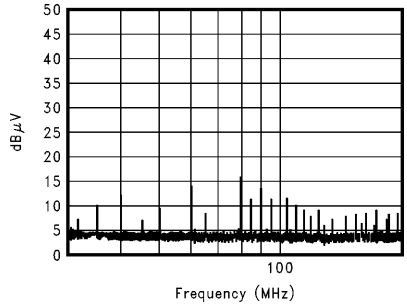

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FIGURE 25b. Emissions with Addition of V_{CC} Choke

Test results in *Figure 26* show emissions of 45 dBμV reduced to less than 20 dBμV on the same device. Unchoked tests were performed using the bonding options previously discussed.

Figure 25 gives the predicted performance degradation from implementing gradual turn-on outputs. High to low transition time propagation delays are doubled and low to high transitions are slowed by about 50%. Remember, though, that propagation delays for an embedded microcontroller are usually of minimal concern since control is based on levels or edges of individual signals or on timing which is under software control. Software control is slow enough that the change in hardware timing is probably negligible.

An indication of the type of emission reduction resulting from the implementation of gradual turn-on can be seen if you look at the baselines of the plots of *Figure 26.* Changes of the outputs occur at low frequency with large amplitude, fast rise time current spikes. The low frequency of the signal keeps the harmonic close together and makes the emissions appear broadband. The fast rise time maintains a higher level of emissions to a higher frequency.

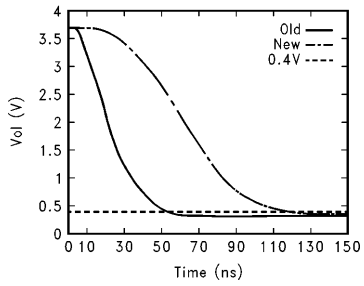

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FIGURE 26a. V_{OL}

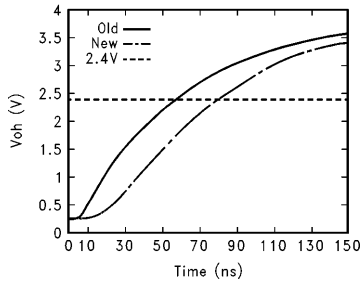

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FIGURE 26b. V_{OH}

7.0 SYSTEM PERFORMANCE USING EMI REDUCED PARTS

We have discussed in previous sections that we can reduce EMI by proper board design and by the selection of low EMI devices. We will now investigate whether EMI reduced parts are worth it. The goal of this testing is to determine the relative electromagnetic emissions from various production options of the COP8 microcontroller. Since most people use OTPs to qualify their end product for emissions approval, both OTPs and ROMmed devices will be tested. The options chosen were:

1. COP8788EGMH (OTP) part used for development and Prototype approval
2. COP888EK (masked ROM) part used for final production (EMI reduced)
3. COP8788GG (OTP) part used for development and Prototype approval
4. COP888GG (masked ROM) part used for final production (EMI reduced)

7.1 Test Procedure

These tests were performed in two ways:

1. Two DIP parts, a COP888EK and a COP888EGMH OTP device, were programmed for use as the main processor in an automotive radio and the relative performance of the radio was measured for each device. The measure of performance chosen was Usable Sensitivity. This is defined as the minimum input required at the antenna in order to achieve a predetermined signal to noise ratio (SNR) at the speaker. In this case the input was chosen to be a 22 kHz deviation of a frequency modulated signal within the US commercial FM radio broadcast band. The signal to noise criterion used was 30 dB.
2. Two other devices, a COP888GG and a COP87M88GG OTP, were placed in a common two sided PCB in a TEM cell and were programmed to run a standard EMI test program included in National's first silicon engineering code. Load capacitors of 10 pF and 4.7 kΩ pull-up resistors used on the eight pins of Port L. The port was programmed to count in a binary manner with the least significant bit changing state every 100 μs. (*Figure 27* illustrates the board layout.) Four AA batteries were attached to the board and the supply voltage was regulated with a Zener diode.

   Emissions were measured with the TEM cell on a Tektronix Model 2754P Spectrum Analyzer over the range of DC to 750 MHz.

7.2 Radio Results

Worst case useable sensitivity is improved by about 17 dB (25 dBμV to 8 dBμV) by the change from the COP888EGMH OTP to the mask programmed COP888EK. Of course not all frequencies show this improvement, but there is some increased sensitivity throughout the spectrum. Note that two local radio stations (at 105.7 MHz and 106.5 MHz) were received even without an external antenna.

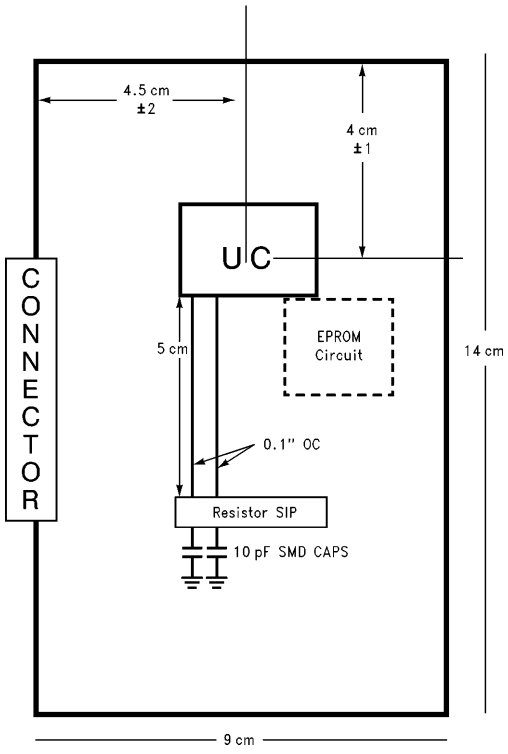

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FIGURE 27. PCB Layout for EMI Testing

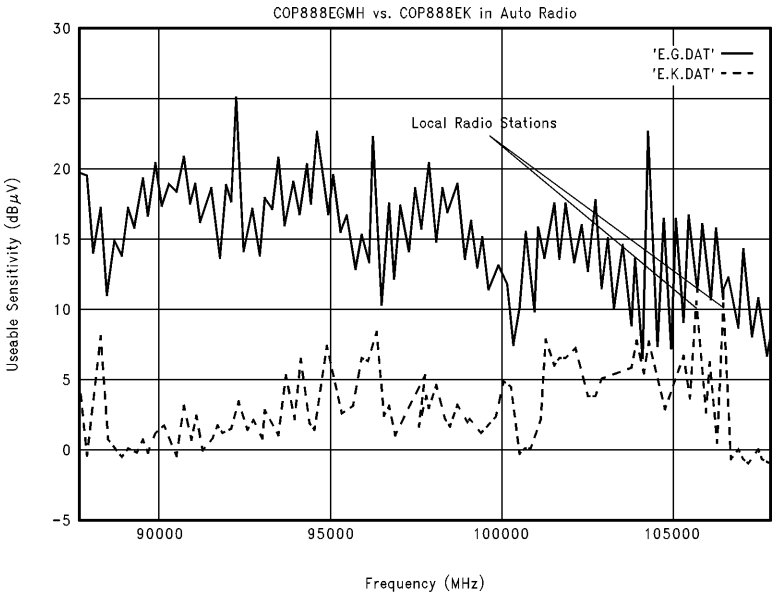

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FIGURE 28. Usable Sensitivity Comparison

7.3 EMI Board Results

Except for the fundamental oscillator frequency of approximately 5 MHz, emissions are down at least 10 dB on the monolithic masked device over the multichip OTP device. Emissions beyond 100 MHz are practically eliminated.

Much more noticeable is the reduction of spectral density in the noise. Off harmonic noise is not noticeable.

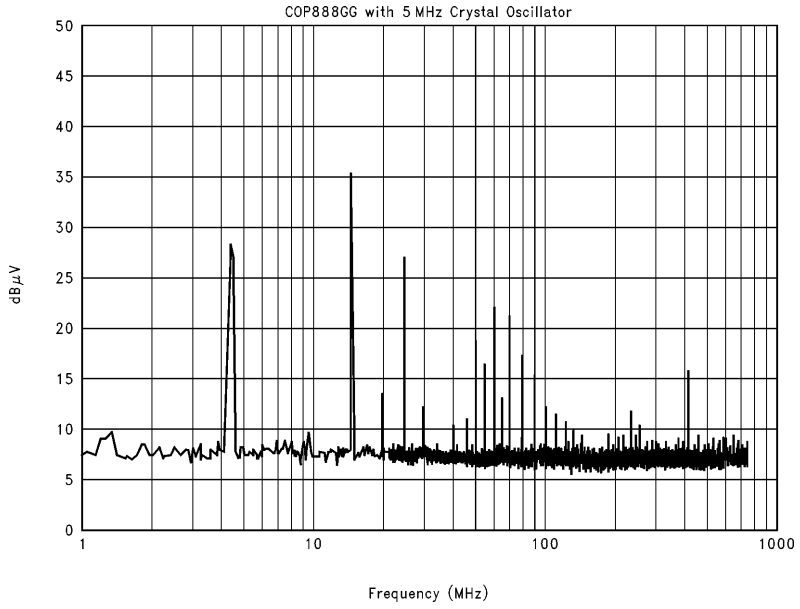

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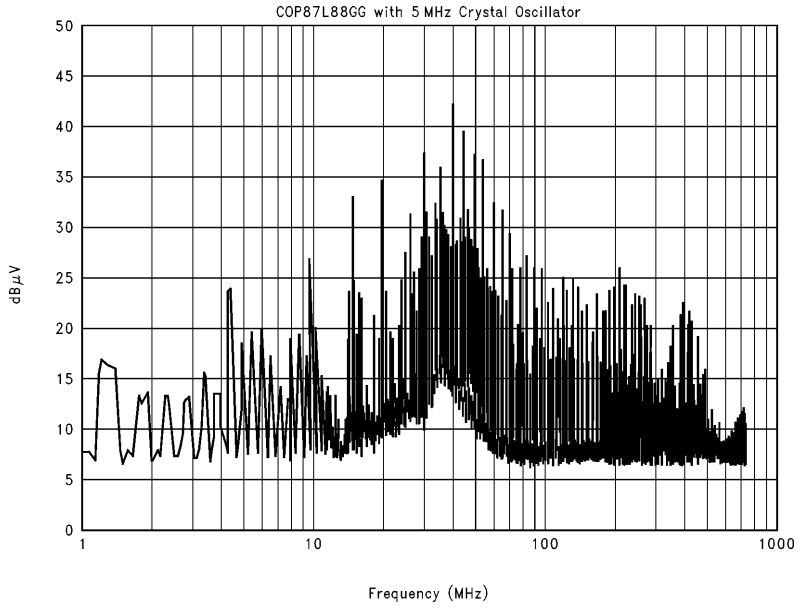
FIGURE 29. COP888GG with 5 MHz Crystal Oscillator



TL/DD/12857–44

FIGURE 30. COP87L88GG with 5 MHz Crystal Oscillator

7.4 Conclusions

Radiated Emissions do not come from a device, but from a board. Devices have some control over the emissions because they generate the noise which is radiated. The equation normally used to predict emission from a system is:

$$|E|_{Max} = \frac{1.32 \times 10^{-3} \times I \times A \times Freq^2}{D} \times \left[1 + \left(\frac{\lambda}{2\pi D}\right)^2\right]^{1/2}$$

where,

$|E|_{Max}$ is the maximum E-field in the plane of the loop in $\mu V/m$

$|$ is the current amplitude, at the frequency of interest, in milliamps

A is the loop area is cm2

λ is the wavelength at the frequency of interest

D is the observation distance in meters

Freq is the frequency in MHz

and the perimeter of the loop $P << \lambda$

When applied to a chip, the area is very small and current is relatively low compared to current consumption in a typical system, thus the emissions are low.

8.0 DESIGN GUIDELINES

The growth of concern over electromagnetic compatibility (EMC) in electronic systems continues to rise in the years since the FCC proclaimed that there shall be no more pollution of the electromagnetic spectrum. Still, designers have not yet fully come to grips with a major source and victim of electromagnetic interference—the PCB. The most critical stage for addressing EMI is during the circuit board design. Numerous tales of woe can be recounted about the eleventh hour attempt at solving an EMI problem by retrofit because EMC was given no attention during design. This retrofit ultimately costs much more than design stage EMC, holds up production and generally makes managers unhappy. With these facts in mind, let's address electromagnetic compatibility considerations in PCB design.

8.1 Logic Selection

Logic selection can ultimately dictate how much attention must be given to EMC in the total circuit design. The first guideline should be: use the slowest speed logic that will do the job. Logic speed refers to transition times of output signals and gate responses to input signals. Many emissions and susceptibility problems can be minimized if a slow speed logic is used. For example, a square wave clock or signal pulse with a 3 ns rise time generates radio frequency (100 MHz and higher) energy that is gated about on the PCB. It also means that the logic can respond to comparable radio frequency energy if it gets onto the boards.

The type of logic to be used is normally an early design decision, so that control of edge speeds and, hence, emissions and susceptibiity is made early. Of course, other factors such as required system performance, speed, and timing considerations must enter into this decision. If possible, design the circuit with as slow speed logic as possible. The use of slow speed logic, however, does not guarantee that EMC will exist when the circuit is built; so proper EMC techniques should still be implemented consistently during the remainder of the circuit design.

8.2 Component Layout

Component layout is the second stage in PCB design. Schematics tell little or nothing about how systems will perform once the board is etched, stuffed, and powered. A circuit schematic is useful to the design engineer, but an experienced EMC engineer refers to the PCB when trouble-shooting. By controlling the board layout in the design stage, the designer realizes two benefits: (1) a decrease in EMI problems when the circuit or system is sent for EMI or quality assurance testing; and (2) the number of EMI coupling paths is reduced, saving troubleshooting time and effort later on.

Some layout guidelines for arranging components according to logic speed, frequency, and function are shown in *Figure 31.* These guidelines are very general. A particular circuit is likely to require a combination and/or trade-offs of these arrangements. Isolation of the I/O from digital circuitry is important where emissions or susceptibility may be a problem. For the case of emissions, a frequently encountered coupling path involves digital energy coupling through I/O circuitry and signal traces onto I/O cables and wires, where the latter subsequently radiate. When susceptibility is a problem, it is common for the EMI energy to couple from I/O circuits onto sensitive digital lines, even though the I/O lines may be ''opto-coupled'' or otherwise supposedly isolated. In both situations, the solution often lies in the proper electrical and physical isolation of analog and low speed digital lines from high speed circuits. When high speed signals are designed to leave the board, the reduction of EMI is usually performed via shielding of I/O cables and is not considered here.

Therefore, a major guideline in layout out boards is to isolate the I/O circuitry from the high speed logic. This method applies even if the logic is being clocked at ''only'' a few MHz. Often, the fundamental frequency is of marginal interest, with the harmonics generated from switching edges of the clock being the biggest emission culprits. Internal system input/output PCB circuitry should be mounted as close to the edge connector as possible and capacitive filtering of these lines may be necessary to reduce EMI on the lines.

High speed logic components should be grouped together. Digital interface circuitry and I/O circuitry should be physically isolated from each other and routed on separate connectors, if possible as shown in *Figure 27d.*

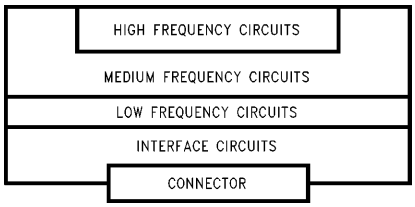


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FIGURE 31a. Board Layout

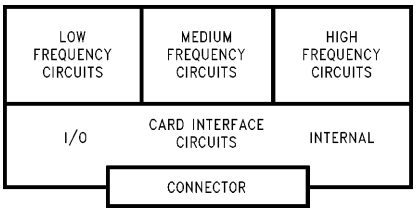

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FIGURE 31b. Board Layout

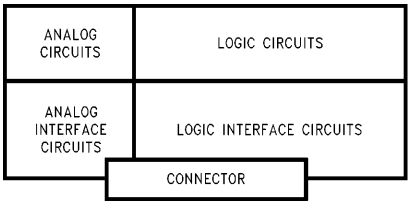

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FIGURE 31c. Board Layout

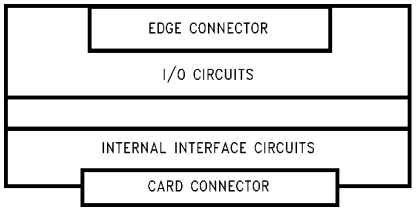

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FIGURE 31d. Board Layout

8.3 Power Supply Bussing

Power supply bussing is the next major concern in the design phase. Isolated digital and analog power supplies must be used when mixing analog and digital circuitry on a board. The design preferably should provide for separate power supply distribution for both the analog and digital circuitry. Single point common grounding of analog and digital power supplies should be performed at one point and one point only—usually at the motherboard power supply input for multi-card designs, or at the power supply input edge connector on a single card system. The fundamental feature of good power supply bussing, however, is low impedance and good decoupling over a large range of frequencies. A low impedance distribution system requires two design features: (1) proper power supply and return trace layout and (2) proper use of decoupling capacitors.

An exception to the rule of analog and digital ground separation applies in the case of high speed interface between analog and digital portions. If possible, the ground plane should be continuous under these interface traces to improve the proximity of the return trace and thus minimize the size of the loop.

At high frequencies, PCB traces and the power supply busses ($+V_{CC}$ and 0V) are viewed as transmission lines with associated characteristic impedance, Z_O, as modeled in *Figure 28.* The goal of the designer is to maximize the capacitance between the lines and minimize the self-inductance, thus creating a low Z_O. Table X, shows the characteristic impedance of various two-trace configurations as a function of trace width, W, and trace separation, h.

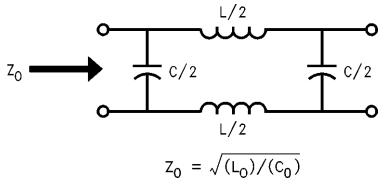

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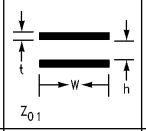
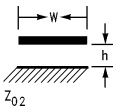
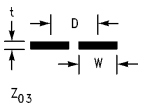
FIGURE 32. Transmission Line Modelling of PCB Traces

TABLE X. Characteristic Impedance of Different Conductor Pairs

			
W/h or D/W	**Parallel Strips**	**Strips Over Ground Plane**	**Strips Side by Side**
0.5	377	377	N/A
0.6	281	281	N/A
0.7	241	241	N/A
0.8	211	211	N/A
0.9	187	187	N/A
1.0	169	169	0
1.1	153	153	25
1.2	140	140	34
1.5	112	112	53
1.7	99	99	62
2.0	84	84	73
2.5	67	67	87
3.0	56	56	98
3.5	48	48	107
4.0	42	42	114
5.0	34	34	127
6.0	28	28	137
7.0	24	24	146
8.0	21	21	153
9.0	19	19	160
10.0	17	17	166
12.0	14	14	176
15.0	11.2	11.2	188
20.0	8.4	8.4	204
25.0	6.7	6.7	217
30.0	5.6	5.6	227
40.0	4.2	4.2	243
50.0	3.4	3.4	255

Any one of the three configurations may be viewed as a possible method of routing power supply (or signal) traces. The most important feature of this table is the noticeable difference in impedance between the parallel strips and strip over ground plane compared with the side-by-side configurations.

As an example of the amount of voltage that can be generated across the impedance of a power bus, consider TTL logic which pulls a current of approximately 16 mA from a supply that has a 25Ω bus impedance (this assumes no decoupling present). The transient voltage is approximately dV = 0.016 x 25Ω = 400 mV, which is equal to the noise immunity level of the TTL logic. A 25Ω (or higher) impedance is not uncommon in many designs where the supply and return traces are routed on the same side of the board in a side-by-side fashion. In fact, it is not uncommon to find situations where the power supply and return traces are routed quite a distance from each other, thereby increasing the overall impedance of the distribution system and the size of the loop antenna. This is obviously a poor layout.

Power and ground planes offer the lowest overall impedance. The use of these planes leads the designer closer to a multi-layer board. At the very least, it is recommended that all open areas on the PCB be ''landfilled'' with an interconnected 0V reference plane so that ground impedance is minimized. This landfill technique may be ineffective, however if minimum width traces connect the filled areas.

Multi-layer boards offer a considerable reduction in power supply impedance, as well as other benefits. Extending the table we just saw, the impedance of a multi-layer power/ground plane bus grows very small (on the order of an Ω or less), assuming a W/h ratio greater than 100. Multi-layer board designs also pay dividends in terms of greatly reduced EMI, and they provide close control of line impedances where impedance matching is important. In addition,

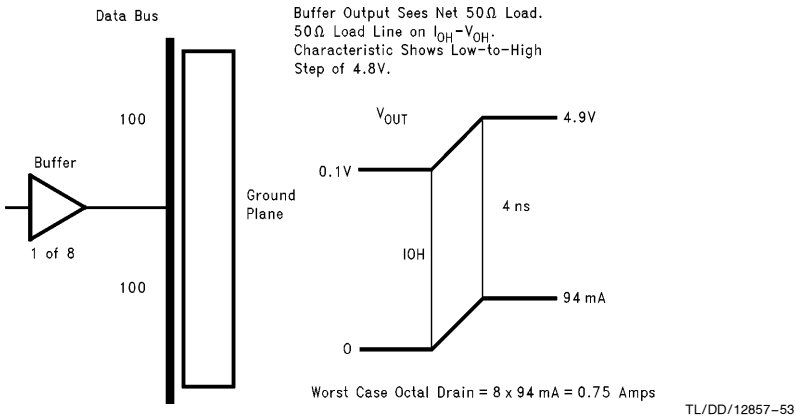


FIGURE 33. Decoupling Example

shielding benefits can be realized. For high-density, high-speed logic applications, the use of a multi-layer board is almost mandatory. The problem with multi-layer boards is the increased cost of design and fabrication and increased difficulty in board repair.

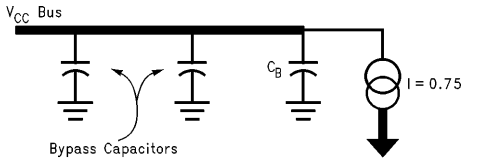
8.4 Decoupling

High-speed CMOS has special decoupling and PCB layout requirements. Adhering to these requirements will ensure that maximum advantage is gained with CMOS devices in system performance and EMC performance.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to a HIGH value. This power is necessary to charge the load capacitance or drive a line impedance.

For most power distribution networks, the typical impedance can be between 50Ω and 100Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{CC} at the part. This droop limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example presented in *Figure 29* used to help calculate the amount of decoupling necessary. This circuit utilizes an octal buffer driving a 100Ω bus from a point somewhere in the middle.

Being in the middle of the bus, the driver will see two 100Ω loads in parallel, or an effective impedance of 50Ω. To switch the line from rail to rail, a drive of 94 mA is needed (4.8V/50Ω) and more than 75 mA wil be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will be to lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current demands. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necesssary values for decoupling capacitors can be calculated with the formula given in *Figure 30*.



Specify V_{CC} Droop = 0.1V max during switching time of 4 ns

Q = CV charge on capacitor

I = C dV/dt

C = I dt/dV = 750 mA × 4 ns/0.1V = 0.030 μF

Select C_B = 0.047 μF or greater

FIGURE 34. Decoupling Example

In this example, if the V_{CC} droop is to be kept below 0.1V and the edge rate equals 4 ns, we can calculate the value of the decoupling capacitor by use of the charge on a capacitor equation: Q = CV. The capacitor must supply the high demand current during the transition period and is represented by I = C(dV/dt). Rearranging this somewhat yields C = I(dt/dV).

Now, I = 750 mA assuming all 8 outputs switch simultaneously for worst case conditions, dt = switching period or 4 ns, and dV is the specified V_{CC} droop of 0.1V. This yields a calculated value of 0.030 μF for the decoupling capacitor. So, a selection of 0.047 μF or greater should be sufficient.

Higher gate count devices, e.g. microcontrollers, with high internal edge rates present additional decoupling problems. Capacitors often suffer from parasitic series inductive effects at high frequency. In fact, a poorly selected capacitor can become almost entirely inductive at high frequency. This can be counteracted by paralleling additional capacitors of lower value and corresponding higher self-resonant frequency. Of course the lower value capacitor should be placed closer to the chip to reduce the size of the resultant current loop.

Inductors or ferrite beads connected in series between the capacitors can help to minimize noise currents and voltages from reaching the rest of the circuit.

It is good practice to distribute decoupling capacitors evenly throughout the logic on the board, placing at least one capacitor for every package as close to the power and ground pins as possible. The parasitic inductance in the capacitor leads can be greatly reduced or eliminated by the use of surface mount chip capacitors soldered directly onto the board at the appropriate locations. Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using Z5U dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

8.5 Proper Signal Trace Layout

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

For those situations where lines must run parallel, as in address and data buses, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing.

There are several termination schemes which may be used. They are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations increase DC power consumption.

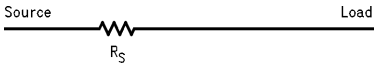
Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula:

$$V_W = \frac{V_{CC} \times Z_{OE}}{Z_{OE} + R_S + Z_S}$$

where R_S is the series Resistor

Z_S is the output impedance of the driver

Z_{OE} is the equivalent line impedance



TL/DD/12857–55

FIGURE 35a. Series Termination

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance (Z_{OE}). The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

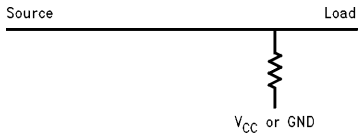


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FIGURE 35b. Parallel Termination

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground depending on which bus the resistor is connected to. While this feature is not desirable for driving CMOS inputs because the trip levels are typically $V_{CC}/2$, it can be useful for driving TTL inputs where level shifting is desirable in order to interface with CMOS devices.

AC parallel terminations work well for applications where the increase in bus delays caused by series terminations are undesirable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin terminations are not generally recommended due to their power consumption. Like parallel terminations, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally be independent of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that output lines with Thevenin terminations should not be left floating since this will cause the undriven input levels to float between V_{CC} and ground, increasing power consumption.

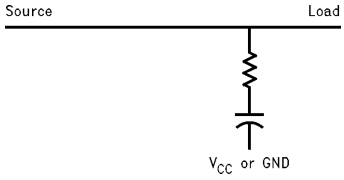

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FIGURE 36a. AC Parallel Termination

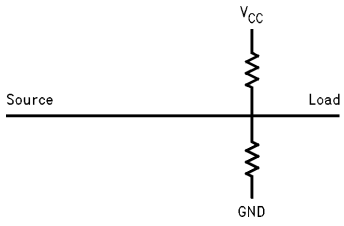

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FIGURE 36b. Thevenin Termination

8.6 Ground Bounce

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

- First, use caution when driving asynchronous TTL-level inputs from CMOS outputs. Ground bounce glitches may cause spurious inputs that will alter the state of non-clocked logic.
- Second, caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Choose package outputs that are as close to the ground pin as possible to drive asynchronous TTL-level inputs.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

8.7 Components

The interference effect by rectifier diodes, typically found in power supply sections of PCBs, can be minimized by one or more of the following measures:

- Placing a bypass capacitor in parallel with each rectifier diode
- Placing a resistor in series with each rectifier diode
- Placing an R-F bypass capacitor to ground from one or both sides of each rectifier diode
- Operating the rectifier diodes well below their rated current capability

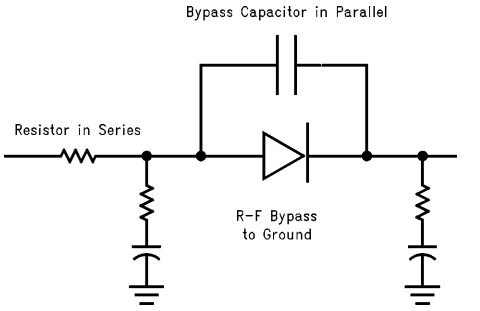

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FIGURE 37a. RF Filtering of Diode

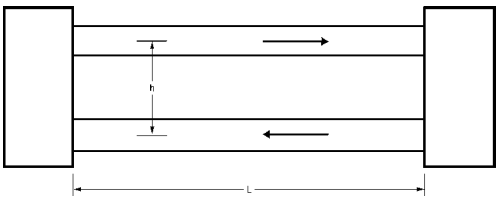

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FIGURE 37b. Connectors and Cables

8.8 Cables and Connectors

Several options are available to reduce EMI from a typical ribbon cable used to interconnect pieces of equipment. These include:

- Reduce spacing between conductors (h in *Figure 37*) by reducing the size of wires used and reducing the insulation thickness. (This could have a negative impact on crosstalk within the cable.)
- Join alternate signal returns together at the connectors at each end of the cable.
- Twist parallel wire pairs in ribbon cables.
- Shield ribbon cable with metal foil cover (superior to braid).
- Replace discrete ribbon cable with stripline flexprint cable.

In the case of joining alternate signal returns, wire N is carrying the signal current, I_N, whereas its mates, N − 1 and N + 1 wires are each carrying one half of the return currents, $I_N - 1$ and $I_N + 1$, respectively. Thus, radiation from pair N and N − 1 is out of phase with radiation from pair N and N + 1 and will tend to cancel. In practice, however, the net radiation is reduced by 20 dB–30 dB with 30 dB being a good default value.

The opposite of this is to conserve signal returns by only using one, or two, wires to service N data lines in a ribbon cable. For data lines farther from the return line, the differential mode radiation becomes so great that this cable tends to maximize EMI radiation. Another disadvantage of this approach is poor impedance control in the resulting transmission line. This could result in distortion of pulses and causes reflections, especially for high-speed logic, and common return impedance noise in this single ground wire.

Ideally, connectors should have negligible resistance for obvious reasons other than EMI control. They should provide for foolproof alignment to minimize the possibility of contact damage over time and use which would increase the resistance and be prone to vibration and shock. The required force should be adequate to provide good mating between contacts which will insure low resistance, but should be minimized to limit likelihood of damage. Connectors should mate with little friction to minimize the effects of continual disconnections and connections increasing the contact resistance with use as the contacts wear out. A contamination free design should be used to avoid corrosion and oxidation increasing resistance and susceptibility to shock and vibration causing intermittent contact.

8.9 Special Considerations with Development Tools

The following set of guidelines have been compiled from the experiences of the applications team at Embedded Technologies Division at National Semiconductor. They should be considered additional techniques and guidelines to be followed concurrently with the standard ones already presented. Some are general and some may be specific to development systems use.

Ground bounce prevention and minimization techniques presented in this paper should be strictly adhered to when using ‘373 type transparent latches on any controller’s external address/data bus. Multiple simultaneously switching outputs could produce ground bounce significant enough to

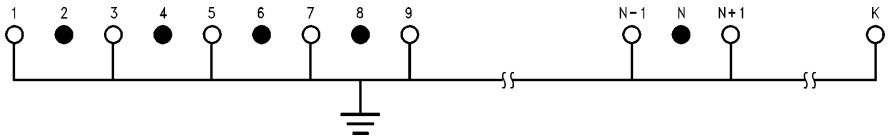

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FIGURE 38a. Alternating Signal Return Minimizes Radiation

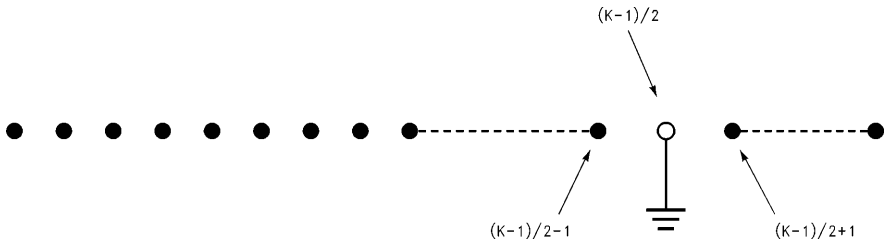

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FIGURE 38b. Single Signal Return Maximizes Radiation

cause false latching. Observe good EMI planning by locating the latches as close to the controller as possible. The use of multi-layer PCBs with good ground planes and following appropriate layout techniques is also essential, especially if emulation will be done at frequencies above 10 MHz. With the foregoing discussions about ''antenna farms'', radiated noise and ideal connector characteristics, it becomes obvious that wire-wrap boards and the use of IC sockets is absolutely out of the question. The concern here is not so much EMI affecting the outside world but EMI strangling the operation of the module itself.

The inputs to the buffers in a '244 type octal buffer package are placed adjacent or side-by-side outputs of other buffers in the package. This configuration would tend to maximize the crosstalk or noise coupling from the inputs to the outputs. On the other hand, the buffer inputs in a '544 type package are on one side of the package and the outputs are on the other. The use of these package types in high speed designs can facilitate board layout to help reduce the effects of crosstalk.

Use extra heavy ground wires between emulator and target board. Rely on the ground returns in the emulator cable for reduction of differential-mode noise radiated from the cable but heavy-duty help is required for reducing power line impedance in the integrated development system.

Unused controller inputs, most importantly any external interrupts and RDY, must be tied to V_{CC} (or GND) directly or through a pull-up (or pull-down) resistor. This not only tends to reduce power consumption, but will avoid noise problems triggering an unwanted action.

In order to reduce the effects of noise generated by high speed signal changes, a sort of Frequency Management technique might be applied. If possible, develop application hardware and software at a slower crystal operating frequency. If ringing, crosstalk, or other combination of radiated and conducted noise problems exists, the result may be to move the problem from one point in the affected signal waveform to a different point. Thus, apparent ''noise glitches'' that caused a latch to erroneously trigger when the input data was still changing, may now come at a time when they are non-destructive such as at a point when the input data is now stable.

Some applications require driving the controller clock input, CKI, with an external signal. Most emulator tools are all clocked using a crystal network with the controller so that the generation of the system timing is contained on the tool itself. Consequently, there is no connection between the emulator cable connector on the tool and the CKI pin at the controller. However, when the emulator cable is now inserted into the target board, the target board's clock signal traveling along the cable couples noise onto adjacent signal lines causing symptoms pointing to an apparent failure of the emulator tool. The recommendation is to disable the clock drive to the CKI pin at the controller pad on the target board whenever the emulator tool is connected. The emulator tools supply the system clock so there is no need for the clock on the target and signal crosstalk on the emulator cable can be greatly reduced with minimal implementation. If one insists that the emulator tool and the target be synchronous, then bring the clock signal from the target to the emulator tool external to the emulator cable via twisted wire pair or coax cable. Remove the clock drive connection to CKI at the target to prevent the signal from entering the cable. Finally, remove crystal components on the emulator tool to prevent problems with the signal.

Connecting boards and modules together to make a totally unique system in which EMC was practiced is necessary to ensure little problem with the environment. But, connecting an emulator tool makes it an entirely new and unique system, both in physical and electrical properties. Treat the emulator tool as part of the system during the design phase and development phase.

9.0 SUMMARY

The design and construction of an electromagnetically compatible PCB does not necessarily require a big change in current practices. On the contrary, the implementation of EMC principles during the design process can fit in with the ongoing design. When EMC is designed into the board, the requirements to shield circuitry, cables, and enclosures, as well as other costly eleventh hour surprises, will be drastically reduced or even eliminated. Without EMC in the design stage, production can be held up and the cost of the project increases.

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