High Speed BUS LVDS Clock Distribution Using the DS92CK16 Clock Distribution Device

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INTRODUCTION

The high data rates in today's systems require extremely low skew clock distribution at a destination on a backplane logic card. Many systems also require a local clock to be distributed across a backplane. Therefore, creating a local distribution of clock signals with low-skew as well as providing a high-speed clock capable of driving a backplane is a must.

The DS92CK16 was designed with the above criteria in mind. The DS92CK16 supports clocks up to 125 MHz, and provides six local copies of a clock that can be input from a BLVDS bus (Bus LVDS) or from an on-board LVCMOS/LVTTL device. The DS92CK16 can also be used to drive a local clock onto the Bus LVDS backplane while providing six local LVTTL copies of the source clock. The block diagram of the device is shown in *Figure 1*.

The DS92CK16 provides the following features:

- Typical clock skew of 30 ps between 6 single-ended CMOS outputs.
- Low Duty Cycle Distortion — 100 ps typical in the Receiver path and 330 ps in the Driver path
- Jam Capability — Force the 6 clock outputs to the logic 'high' state
- 70 mV receiver thresholds for extra noise margins

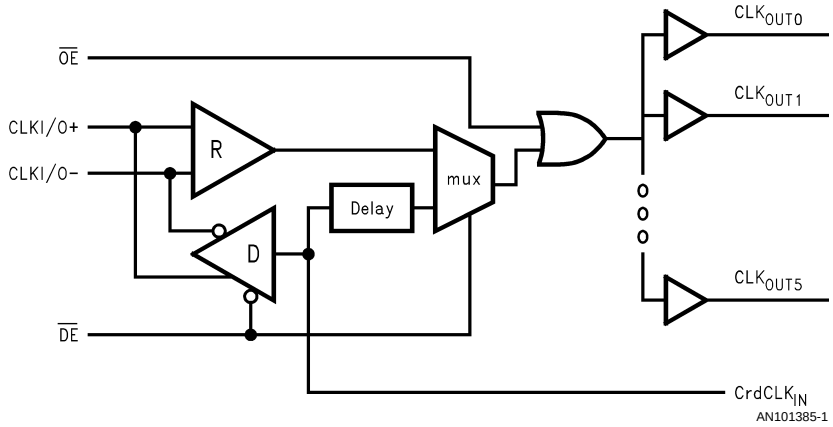


FIGURE 1. Block Diagram of DS92CK16

OPERATION MODES

The DS92CK16 supports four modes of operation:

1. **BUS LVDS Input to Distributed Clock Outputs**

   With $\overline{OE}$ Low and $\overline{DE}$ High, the transceiver is in the bus-input mode. Using the CLKI/O pins as LVDS inputs, 6 copies of this signal are presented at the CLK_{OUT} pins as single-ended signals. These six outputs have gradual turn on/off (GTO) circuits which minimize switching noise. In this mode, the $C_{RD}CLK_{IN}$ pin is ignored as an input. The $\overline{OE}$ and $\overline{DE}$ pins have weak current sources to V_{CC}. If these pins are left open circuit, the CLK_{OUT} pins will be "High" and the CLKI/O pins will be TRI-STATE®.

2. **Local Clock in (LVTTL) to BUS LVDS Output**

   With $\overline{OE}$ High and $\overline{DE}$ Low, the transceiver becomes a bus driver. A 3V singled ended LVCMOS/LVTTL signal is input on the $C_{RD}CLK_{IN}$ pin. This signal is translated to a BLVDS signal at the CLKI/O pins capable of driving a 75Ω T-line, terminated at both ends. The six CLK_{OUT} signals are forced to the Logic High state.

3. **Local Clock in (LVTTL) to BUS LVDS Backplane Drive with Local Loopback**

   With $\overline{OE}$ Low and $\overline{DE}$ Low, six copies of the $C_{RD}CLK_{IN}$ signal are output on the CLK_{OUT} pins, as well as a BUS LVDS signal on the CLKI/O pins.

4. **Forced Failsafe Mode**

   With $\overline{OE}$ and $\overline{DE}$ High, all CLK_{OUT} are forced High, and CLKI/O pins are TRI-STATE. $C_{RD}CLK_{IN}$ and CLKI/O are ignored as inputs.

TYPICAL APPLICATIONS

The DS92CK16 may be used in Point-to-Point, Multi-drop, or in multi-point clock distribution applications. These configurations are shown in *Figures 2, 3, 4.* For simplicity, the DS92CK16 is shown as a driver block or receiver block.

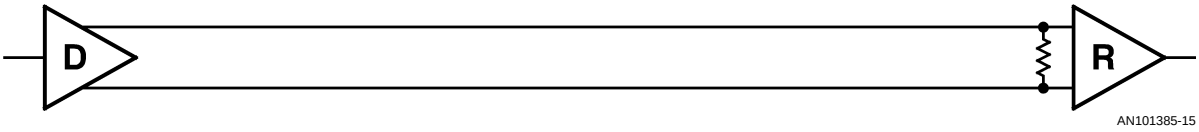


FIGURE 2. Common Bus Configuration: Point-to-Point

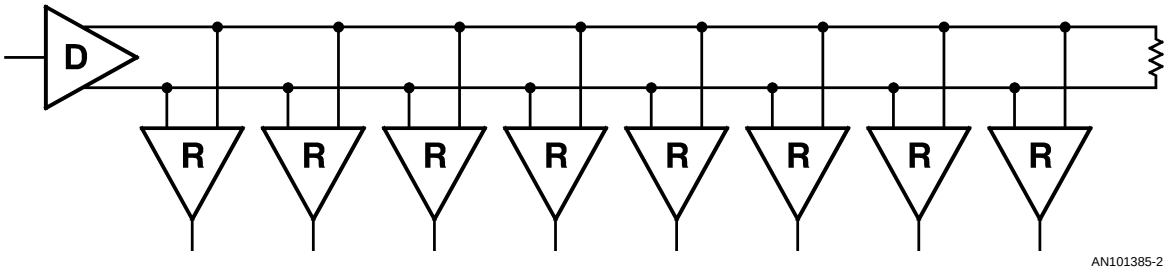


FIGURE 3. Common Bus Configuration: Multi-Drop

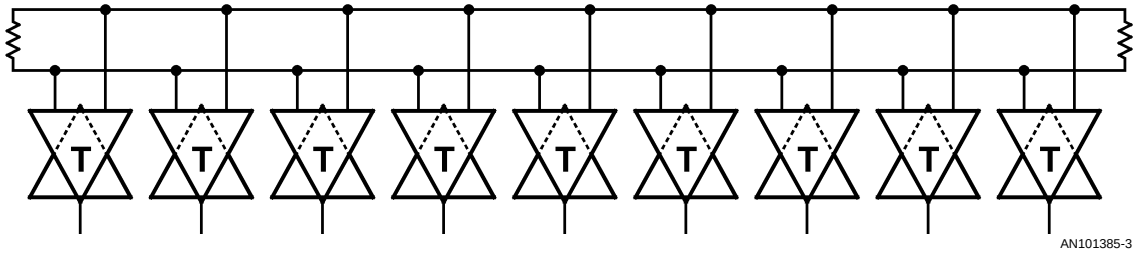


FIGURE 4. Common Bus Configuration: Multi-Point

BUS TERMINATION

For Multi-drop applications 1 or 2 resistors will be required depending upon the location of the driver. If there is only one clock source (driving node) and the configuration is similar to *Figure 2* or *Figure 3* then only 1 resistor is needed. If the clock source is located in the center of the bus, or if it can be sourced from any location, then two resistors (one at each end) would be required as shown in *Figure 4*. The termination resistor value should be equal to the effective loaded differential impedance of the line. It is better to err on the high side and create a small positive reflection than to be too low in value thereby reducing received signal voltage and differential noise margins. The resistor value is determined by the application and depends upon line impedance (unloaded), distance between cards, and capacitive loading added by the cards. The value is typically in the 50Ω to 100Ω range. If doubly terminated, the driver sees both resistors in parallel. Thus, the resulting load is 25Ω to 50Ω.

This is also the reason that National's BUS LVDS parts provide about 3X the driver current of standard LVDS drivers. With a 10 mA drive level, impedance below 50Ω can be driven to levels similar to LVDS with its 100Ω load and 3 mA driver. Closely-spaced backplanes reduce the impedance of the backplane below 50Ω. See AN-905 and also the BLVDS White Papers (located on the web at www.national.com/appinfo/lvds) for information on calculating differential impedance based on the trace geometry.

FAILSAFE BIASING

Failsafe is a common concern in multi-driver applications. If a known state is required when all drivers are off, a failsafe bias may be required. The receivers have a minimum amount of internal failsafe biasing, which may need to be boosted in the application (for example, if it has CMOS rail-to-rail signals swinging on adjacent pins in connectors). If this is the case, a pull-up and pull-down resistor should also be used at the site of the terminations as shown in *Figure 5*. These resistors will typically be in the 1 kΩ to 2 kΩ range. A slight positive bias conditions the line when all drivers are off. These resistors should not be reduced too much in value because this will load down the driver and distort the signal swing as shown in *Figure 6*.

Figure 6 simulation configuration consists of a 1.2 kΩ resistor connected from the driver True output to V_{CC}, a 0.8 kΩ resistor connected from driver Inverted output to Ground, and a 37.5Ω resistor connected between the True and Inverted driver outputs. This lumped load represents the biasing scheme shown in *Figure 5*

The magnitude of VOD is altered by the bias current such that in one direction, the bias adds to the VOD and in the other direction the bias subtracts from the VOD. This simulation shows an extreme case, as the pull up and down resistors are near their recommended minimum value (1 kΩ) and this creates a VOD imbalance of 80 mV. The receiver switches at 0V differential, so this impact to VOD does not impact the data. Also, the minimum VOD is still greater than 200 millivolts

The internal failsafe in the DS92LV16 receiver consists of a weak current source to V_{CC} on the "plus" pin and a weak Current sink on the "minus" pin plus a slight internal offset in the differential pair input. This provides a known state if the card is powered up and is removed from the system. With the card's inputs now "open", the internal failsafe biasing locks the outputs into a stable known (High) state.

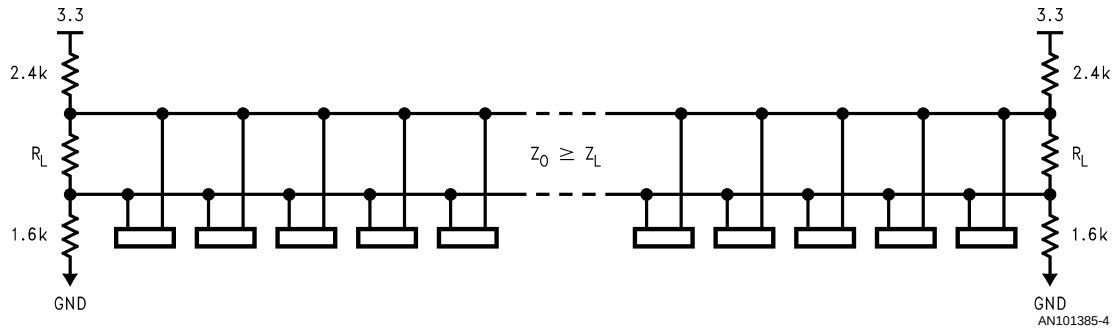


FIGURE 5. Typical Failsafe Biasing Scheme

Failsafe Loading Simulation — DS92CK16
75Ω Bus with 1.2 kΩ Pull Up & 800 Ω Pull Down

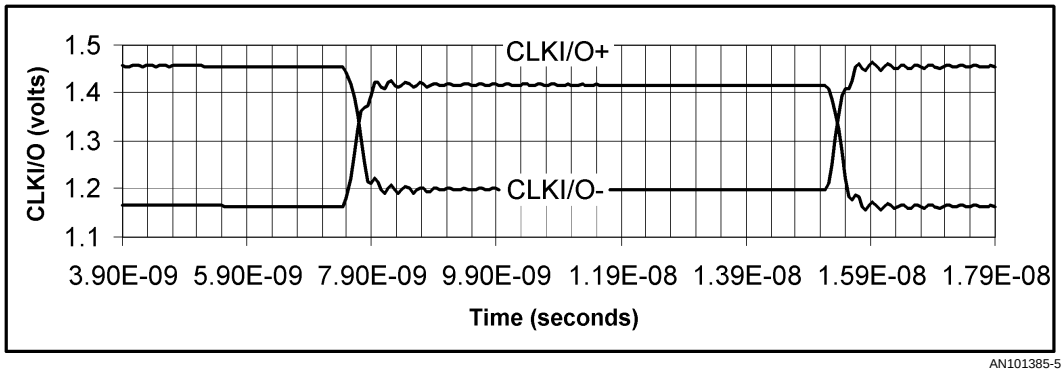


FIGURE 6. Backplane Termination and Failsafe Biasing

General comments about the failsafe biasing resistors are:

- Magnitude of the resistors should be 1 to 2 orders higher than the termination resistor to prevent excessive loading to the driver and waveform distortion.
- Mid-point of the failsafe bias should be close to the offset voltage of the driver (+1.25V) to prevent a large common mode shift from occurring between active and TRI-STATE bus conditions.
- Pull-up and pull-down resistors should be used at both ends of the bus for quickest response.

LIVE INSERTION SUPPORT AND POWER SEQUENCING

Inserting a card into a live bus may be required in applications where system down time must be minimized. This may be accomplished by the use of redundant logic cards and interconnect (systems), or with a system that is fault-tolerant. Bus LVDS provides a robust, fault-tolerant data transmission system that allows the insertion of a card into an active bus. In certain applications, this can eliminate the need for redundant paths altogether, thus reducing system cost. When inserting, it is recommended that the Ground pin makes contact first, then the V_{CC} pin, lastly the BUS LVDS I/O pins. When removing, it is recommended that the I/O pins be disconnected first, then V_{CC} and lastly the Ground pin.

STUBS

The connection of DS92CK16 devices to the backplane forms stubs on the original transmission line, the backplane. The stub extends from the backplane — through the connector — to the device. If the length of this stub becomes long compared to the 'electrical length' of the signal's rise time the stub will begin to act as another transmission line and reflections from the end of the stub back to the backplane become a signal quality issue. The 'electrical length' is the distance the signal travels over a PCB trace in the time period equal to the signal rise time. Various "rules of thumb" have been put forth as to the acceptable ratio of stub length to 'electrical length'. These rules require that the stub length be some fraction of the electrical length; stub length < ⅓ electrical length to stub length < ⅙ electrical length. The purpose of the "rules of thumb" is to provide a threshold at which the stub is considered as a lumped load or as a transmission line. For backplanes the lumped load is required because transmission lines created by long stubs must be terminated and the additional terminations will load the device driving the backplane.

A common recommendation when determining the electrical length of a device's rise time is that the rise time should be projected to 100% of the signal swing from the 20%–80% or 10%–90% value specified in the device datasheet. However, doing so may overstate the rise time if the driving device has GTO outputs, that causes a slow roll-off of the signal edge. For GTO outputs, the 10% to 90% value may be a better choice.

Example 1: Using the typical CLKI/O transition times from the data sheet (0.75 ns for 20% to 80%) and the ¼ rule of thumb we have the following calculations to determine maximum stub length:

First convert this to 0%–100% by dividing by 0.6

Rise (0%–100%) = 0.75/0.6 = 1.25 ns

Now:

l = Tr/D, where:

l = electrical length of the Rise Time in inches

T_r = Rise Time 0% to 100% calculation in picoseconds (ps)

D = Propagation Delay per unit length, ps/inch

(typical PC board trace value is 160 ps/inch)

l = 1250/160 = 7.8 inches

Now divide this by 4 to determine the maximum stub length.

Lumped load stub length < 7.8/4 = 1.95 inches

From this the stub length should not be greater than 2 inches. This calculation uses the ¼ rule, which is on the conservative side. The ⅓ rule is also commonly used. Also, the rise time is the fastest at the driver output. As the signal travels down the backplane or cable the edge will be slowed due to loading and attenuation of high frequencies. Thus the stub length of the receiving locations can be longer since the rise time is slowed at that point. Remember that the stub is the length from the backplane through connectors to the lead of the package.

Figure 7 shows the rise time of the DS92CK16's BLVDS driver under typical load conditions. The smooth signal transitions and also the balance between rise and fall times can be seen from the scope plot. Both the true and inverting outputs are shown.

Note that the scope inputs were attenuated by a factor of 10:1 due to the probing method used. Conditions are: f = 150 MHz, V_{CC} = 3V, T_A = 90˚C, R_L = 37.5Ω, C_L = 15 pF, Output duty cycle is 49.8%.

A first approximation for LVDS drivers is that the outputs behave as constant current sources. As such, one would expect that the VOD across a given R_L would be proportional to the resistor value. While it is correct that the outputs operate in current-mode the VOD is limited and the output current will roll off as the load resistance increases. *Figure 9* shows the VOD of the DS92CK16 with various values of R_L. The typical area of operation is between 25Ω and 120Ω. *Figure 8* shows the single-ended V-I curves and the clamping action that the part provides.

The Bus LVDS outputs of the DS92CK16 are designed to provide closely matched output impedance between the pull-up and pull-down circuits in the operating output voltage range. *Figure 9* shows the V/I curves of the outputs from simulation data. Note the similar slopes of the lines from 1V to 1.6V which indicates balanced outputs.

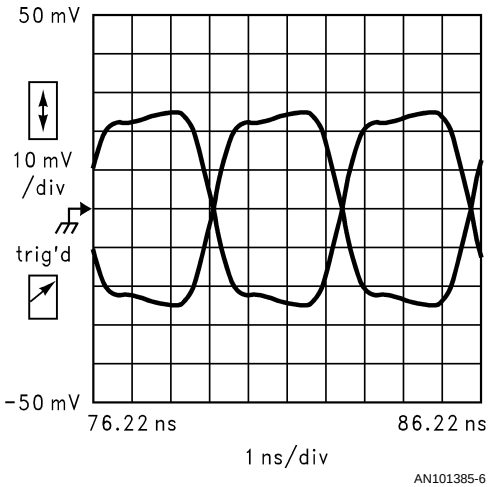


FIGURE 7. Single-Ended Waveforms of CLKI/O Outputs (BUS LVDS)

DS92CK16 Sim of V vs I for CLKI/O High and Low Cases, V_{CC} = 3.3V, T_A = 25˚C

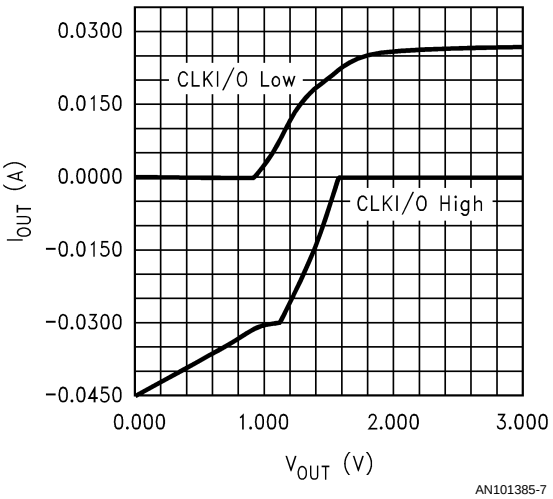


FIGURE 8. Voltage vs Current for CLKI/O Signals (simulation)

DS92CK16 CLKI/O VOD vs R_L, V_{CC} = 3.3V, T_A = 25˚C

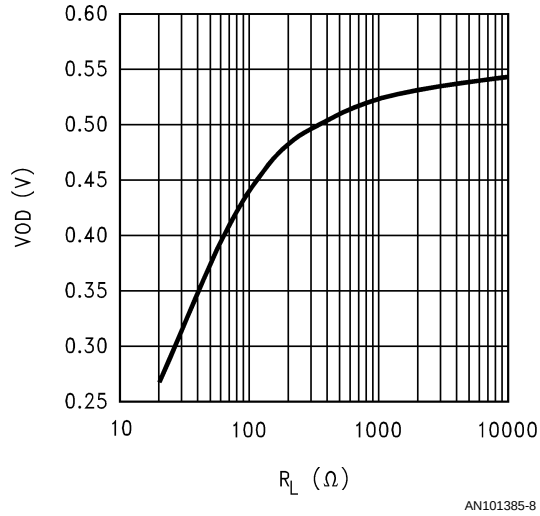


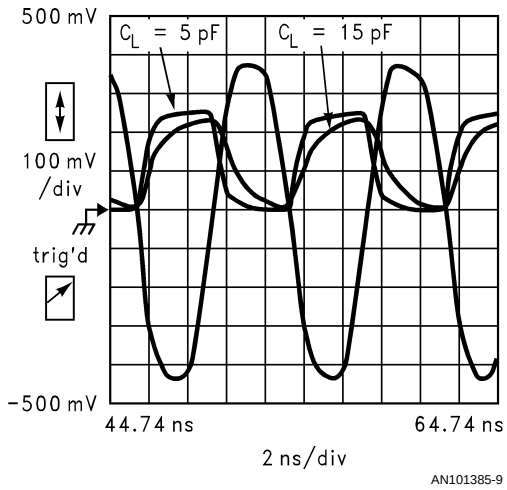
FIGURE 9. VOD vs R_L

RECEIVER OUTPUTS—LOCAL CLOCK DISTRIBUTION

The DS92CK16 employs Gradual Turn On/Off (GTO) circuitry on all CMOS clock outputs (CLK_{OUT} 1-6). The GTO outputs provide less current drive when turning on or off and add current drive during the transition from low-to-high or high-to-low to drive low impedance loads. This results in a rounding of the top/bottom of the transient edges due to the smaller change in current with respect to time (di/dt). The benefit is: less ground bounce, less V_{CC} droop, and longer stub driving than devices with standard CMOS outputs.

The softer edges of the CLK_{OUT} outputs allow for relatively long stubs off of each trace connected to the CLK_{OUT} output. Using the rule 'electrical length' < ¼ stub length and propagation delay per unit length = 160 ps/in., distribution stubs can be about 3.5 inches with a total load of 15 pF.

The duty cycle of the DS92CK16 CLK_{OUT} outputs remains very close to 50% at the maximum frequency of 125 MHz for loads of C_L = 5 pF and C_L = 15 pF. *Figure 10* shows the CLK_{OUT} outputs under the datasheet conditions of 5 pF and 15 pF. Note that the signal was attenuated (10:1) at the scope inputs (R_L = 500Ω). *Table 1* summarizes the V_{OH}, V_{OL}, and Duty Cycle.



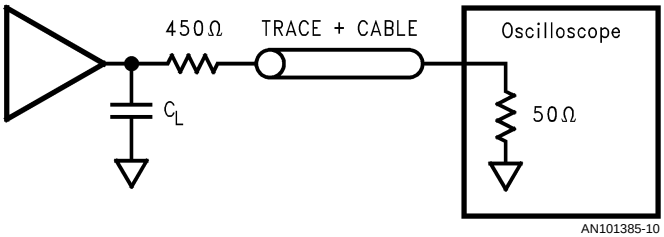


FIGURE 10. CLK_{OUT} vs C_L, R_L = 500Ω, Input = $C_{RD}CLK_{IN}$, Freq = 125 MHz, V_{CC} = 3.0V, T_A = 90˚C

TABLE 1

C_{LOAD} (pF)	V_{MAX} (V)	V_{MIN} (mV)	DC%
5	2.56	4	49.7
15	2.40	0	51.4

Channel to channel skew of the DS92CK16 Receiver outputs is also very well controlled over temperature and V_{CC} operating ranges. *Figures 11, 12* show that the receiver channel to channel skew remains below 40 ps over V_{CC} (3.0V, 3.3V, and 3.6V) for temperatures of 25˚C and 85˚C. This bench sample contains units from three different fabrication runs.

DS92CK16 Ave Skew at 25˚C

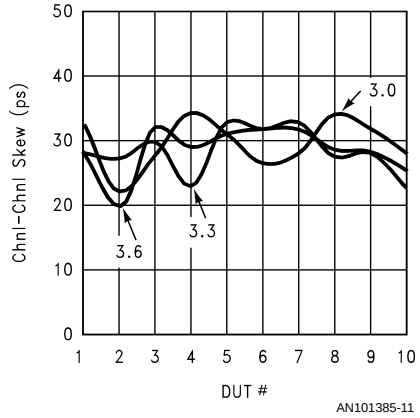


FIGURE 11. Receiver Channel to Channel Skew at 25˚C

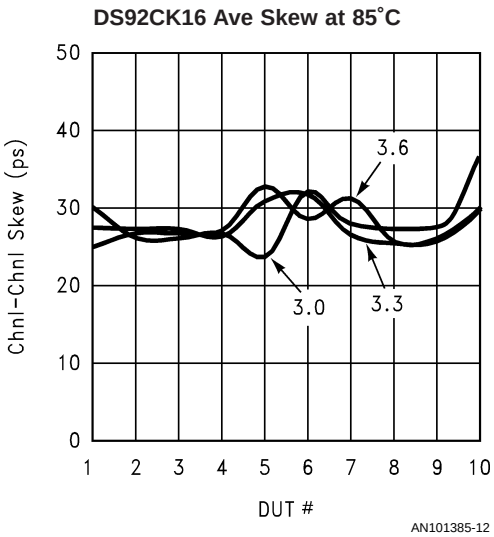


FIGURE 12. Receiver Channel to Channel Skew at 85˚C

POWER DISSIPATION

The DS92CK16 draws very little I_{CC} current when operating due to the nature of its design. *Figure 13* shows that at the maximum operating frequency (125 MHz) the device draws less than 70 mA in the 'receiver' mode. When driving the backplane (*Figure 14*) and the CLK_{OUT} outputs, the I_{CC} current is only increased by about 10 mA (the output drive of the Bus LVDS output).

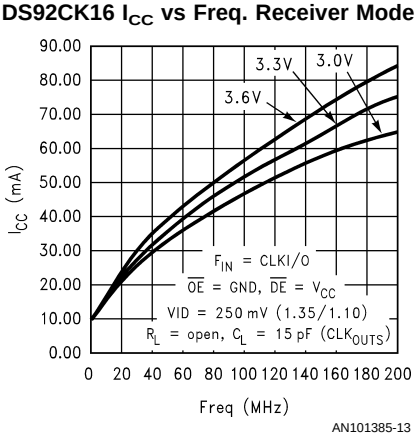


FIGURE 13. Typical I_{CC} vs Frequency. Input is CLKI/O

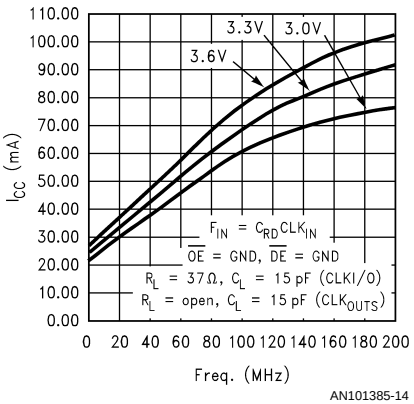


FIGURE 14. I_{CC} vs Frequency with the C_{RD}CLK in as the Input, and CLKI/O, CLK_{OUT} Pins Switching

CONCLUSION

The DS92CK16, BUS LVDS clock distribution device provides a new LVDS based alternative to solving clock distribution problems. It works well in environments requiring up to a 125 MHz clock distribution. It also works well as a differential backplane driver in source synchronous system applications. The very well matched six clock outputs guarantee very low skew and provide a near 50/50 clock duty cycle. The CLKI/O (BUS LVDS) outputs with GTO, allow the use of longer stubs (up to 2 inches) for common multi-point / multi-drop applications.

REFERENCES

National Semiconductor application notes (all available from www.national.com/appinfo/lvds)

AN-108

AN-806

AN-807

AN-808

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