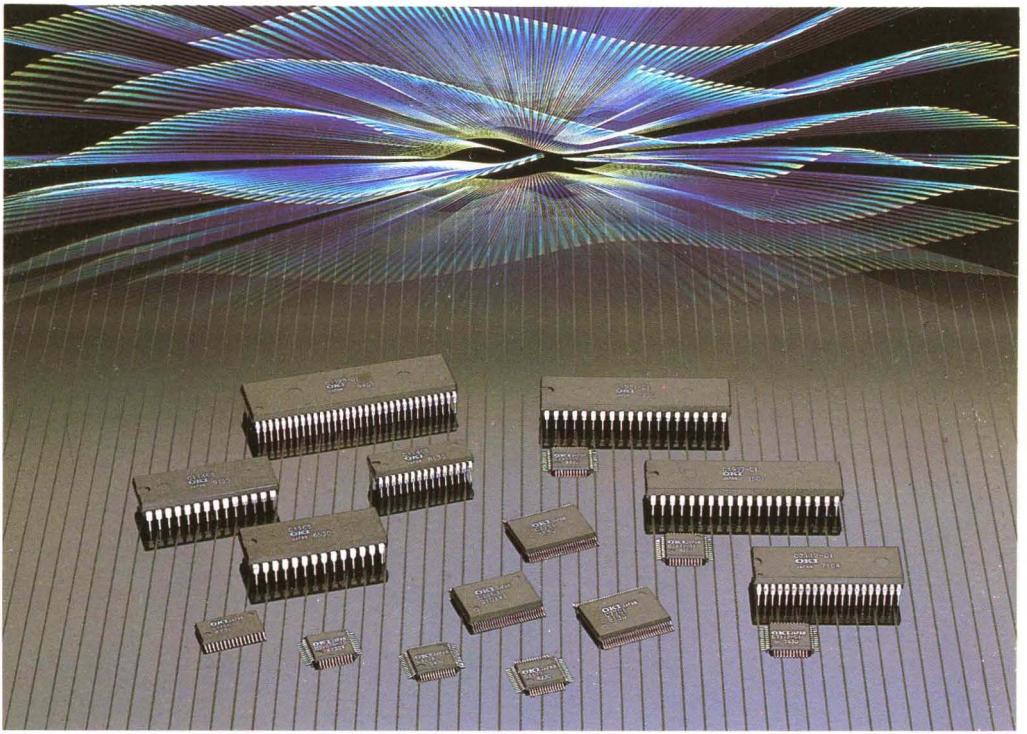
DATA BOOK

OKI

VACUUM FLUORESCENT DRIVER



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VACUUM FLUORESCENT DRIVER DATA BOOK 1989 / 1990

VACUUM FLUORESCENT DISPLAY TUBE DRIVER LINE-UP AND TYPICAL CHARACTERISTICS

PACKAGING

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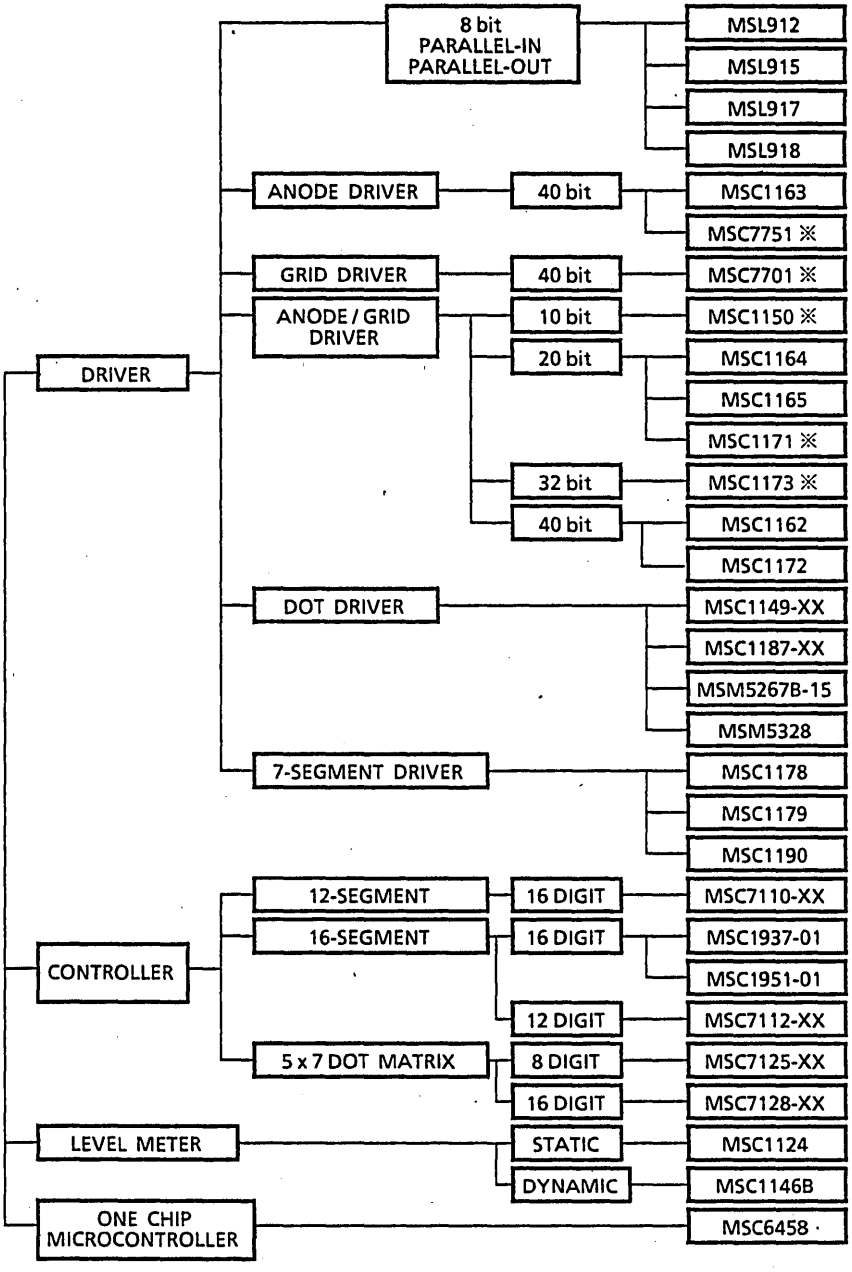
VACUUM FLUORESCENT DISPLAY TUBE DRIVER LINE-UP AND TYPICAL CHARACTERISTICS

VACUUM FLUORESCENT DISPLAY TUBE DRIVER LINE-UP AND TYPICAL CHARACTERISTICS



※ Under development

• DRIVER

DEVICE NAME	TYPE	NUMBER OF OUTPUT	OUTPUT VOLTAGE	OUTPUT CURRENT		OUTPUT CIRCUIT	SHIFT RESISTER	LATCH	REMARKS
				SINK	SOURCE				
MSL912RS	–	8	+30V	–	–40mA	EMITTER FOLLOWER+PULL DOWN	–	–	8 Drivers
MSL915RS	–	8	–60V	–	–40mA	EMITTER FOLLOWER+PULL DOWN	–	–	8 Drivers
MSL917RS	–	8	–80V	–	–90mA	EMITTER FOLLOWER	–	–	8 Drivers
MSL918RS	–	8	+30V	–	–40mA	EMITTER FOLLOWER	–	–	8 Drivers
MSC1149-XX RS/GS	–	Large 8 Small 25	+18V	Large 0.5mA Small 0.5mA	Large -2mA Small -0.8mA	PUSH PULL	34	33	Auto Load Circuit
MSC1150RS	DATA/SCAN	10	+60V	2mA	–25mA	PUSH PULL	10	10	
MSC1162GS	DATA/SCAN	40	+65V	2mA	-40mA	PUSH PULL	40	40	Bi-directional S/R
MSC1163GS	DATA	40	+65V	2mA	-2mA	PUSH PULL	40	40	Bi-directional S/R
MSC1164GS	DATA/SCAN	20	+65V	2mA	–40mA	PUSH PULL	20	20	
MSC1165RS	DATA/SCAN	20	+65V	2mA	–40mA	PUSH PULL	20	20	
MSC1171RS	DATA/SCAN	20	+60V	2mA	–25mA	PUSH PULL	20	20	–
MSC1172GS	DATA/SCAN	40	+70V	2mA	-40mA	PUSH PULL	40	40	Bi-directional S/R
MSC1173RS	DATA/SCAN	32	+60V	2mA	–25mA	PUSH PULL	32	32	
MSC1178/79GS	–	VF 13+7x3 LED 9	+18V	VF 0.1mA LED 20mA	VF -1mA	PUSH PULL (VF) OPEN COLLECTOR (LED)	35	35	7 Segment Decoder Dimming Circuits
MSC1187-XX GS	–	Large 8 Small 25	+18V	Large 0.5mA Small 0.5mA	Large -2mA Small -0.8mA	PUSH PULL (VF)	34	33	MSC1149+ Dimming
MSC1190	–	VF 13+7x3 LED 9	+18V	VF 0.1mA LED 25mA	VF -1mA	PUSH PULL (VF) OPEN COLLECTOR (LED)	35	35	7 Segment Decoder Dimming Circuits
MSC7701GS	SCAN	40	+130V	2mA	-40mA	PUSH PULL	40	40	Bi-directional S/R
MSC7751GS	DATA	40	+200V	2mA	-2mA	PUSH PULL	40	40	Bi-directional S/R
MSM5267B-15RS/GS	–	Large 8 Small 25	+18V	Large 0.5mA Small 0.5mA	Large -6mA Small -1.5mA	PUSH PULL	34	33	
MSM5328RS	–	Large 8 Small 25	+18V	Large 0.5mA Small 0.5mA	Large -3.5mA Small -0.8mA	PUSH PULL	34	33	

• CONTROLLER

DEVICE NAME	TYPE	NUMBER OF OUTPUT	OUTPUT VOLTAGE	OUTPUT CURRENT		OUTPUT CIRCUIT	REMARKS
				SINK	SOURCE		
MSC1937-01 RS/GS	CONTROLLER	GRID 16 SEG 18	-58V	-	GRID -10mA SEG -10mA	EMITER FOLLOWER	16 Segment + Decimal point & Comma Tail 16 Digits Character Generator, Dimming Circuits
MSC1951-01 RS/GS	CONTROLLER	GRID 16 SEG 18	-58V	-	GRID -10mA SEG -10mA	EMITER FOLLOWER	16 Segment + Decimal point & Comma Tail 16 Digits Character Generator, Dimming Circuits
MSC7110-01 RS/GS	CONTROLLER	GRID 16 SEG 12 LED 5	-45V	GRID 0.2mA SEG 0.2mA LED 0.1mA	GRID -40mA SEG -6mA LED -10mA	PUSH PULL	16 Segment 16 Digits Character Generator, Dimming Circuits
MSC7112-01 RS/GS	CONTROLLER	GRID 12 SEG 16 LED 5	-45V	GRID 0.2mA SEG 0.2mA LED 0.1mA	GRID -40mA SEG -6mA LED -10mA	PUSH PULL	16 Segment 16 Digits Character Generator, Dimming Circuits
MSC7125-XX GS	CONTROLLER	GRID 8 SEG 40	+52V	GRID 10μA SEG 10μA	GRID -31mA SEG -0.3mA	PUSH PULL	5 x 7 Dot + 5 Annunciators 8 Digits Character Generator, Dimming Circuits
MSC7128-XX SS	CONTROLLER	GRID 16 SEG 35 CURSOR 1	-60V	GRID 0.1mA SEG 0.1mA CURSOR 0.1mA	GRID -30mA SEG -2mA CURSOR -10mA	PUSH PULL	5 x 7 Dot + Cursor 16 Digits Character Generator, Dimming Circuits

• LEVEL METER

DEVICE NAME	TYPE	NUMBER OF OUTPUT	OUTPUT VOLTAGE	OUTPUT CURRENT		OUTPUT CIRCUIT	REMARKS
				SINK	SOURCE		
MSC1124 RS/GS	2-CH, 12-DOT	SEG 12x2	+37V	SEG 0.1mA	SEG -0.2mA	PUSH PULL	for Static VFD -20 dB~8 dB Peak Hold
MSC1146B RS/GS	2-CH, 15-DOT	GRID 2 SEG 15	-37V	-	GRID -20mA SEG -0.2mA	EMITER FOLLOWER + PULL DOWN	for Dynamic VFD -40 dB~10 dB Peak Hold

• ONE CHIP MICROCONTROLLER

DEVICE NAME	TYPE	NUMBER OF OUTPUT	OUTPUT VOLTAGE	OUTPUT CURRENT		OUTPUT CIRCUIT	REMARKS
				SINK	SOURCE		
MSC6458 SS/GS	4BIT MICROCOMPUTER	12 x 12	+40V	Large 1mA Small 1mA	large -20mA Small -6mA	PUSH PULL	4.3 MHz

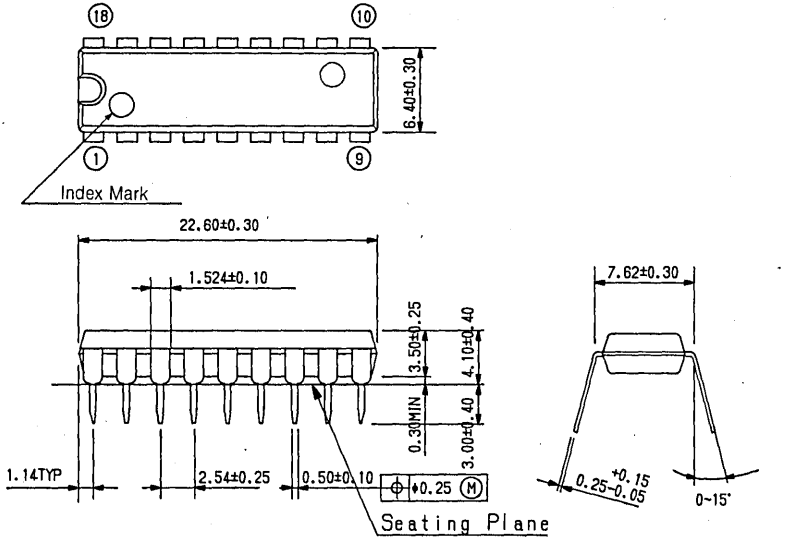
PACKAGING

PACKAGING

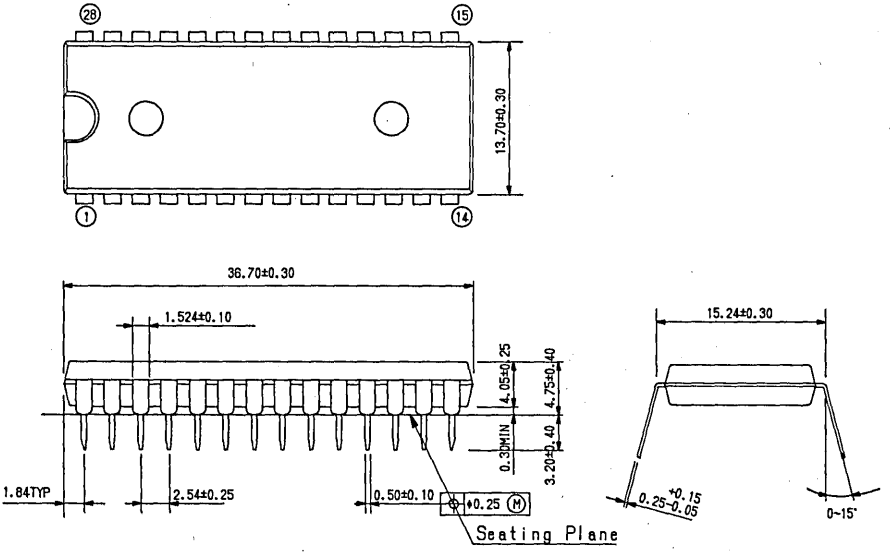
	PRODUCT NAME	NO. OF PINS	PACKAGES						
			BARE CHIP	RS DIP	GS FLAT		JS QFJ	SS SDIP	
					QFP	SOP			
VF DRIVER	MSL912	18		○					
VF DRIVER	MSL915	18		○					
VF DRIVER	MSL917	18		○					
VF DRIVER	MSL918	18		○					
VF DRIVER	MSC1163	60				○			
VF DRIVER	MSC7701	60				○			
VF DRIVER	MSC7751	60				○			
VF DRIVER	MSC1150	18		○					
VF DRIVER	MSC1164	32				○			
VF DRIVER	MSC1165	28		○					
VF DRIVER	MSC1171	28		○					
VF DRIVER	MSC1173	40		○					
VF DRIVER	MSC1162	60				○			
VF DRIVER	MSC1172	60				○			
VF DRIVER	MSC1149-XX	40		○					
		44			○				
VF DRIVER	MSC1187-XX	44			○				
VF DRIVER	MSM5267B-15	40		○					
		44			○		○		
VF DRIVER	MSC5328	40		○					
		44			○		○		
VF DRIVER	MSC1178	56			○				
VF DRIVER	MSC1179	56			○				
VF DRIVER	MSC1190	56			○				
VF CONTROLLER	MSC7110-01	42						○	
		44			○				
VF CONTROLLER	MSC1937-01	40		○					
		44			○				
VF CONTROLLER	MSC1951-01	40		○					
		44			○				
VF CONTROLLER	MMSC7112-01	42						○	
		44			○				
VF CONTROLLER	MSC7125-XX	60			○				
VF CONTROLLER	MSC7128-XX	64						○	
LEVEL METER	MSC1124	40		○					
		44			○				
LEVEL METER	MSC1146B	28		○					
		30						○	
ONECHIP MICRO	MSC6458	64			○			○	

PLASTIC DIP

DIP18-P-300



DIP28-P-600



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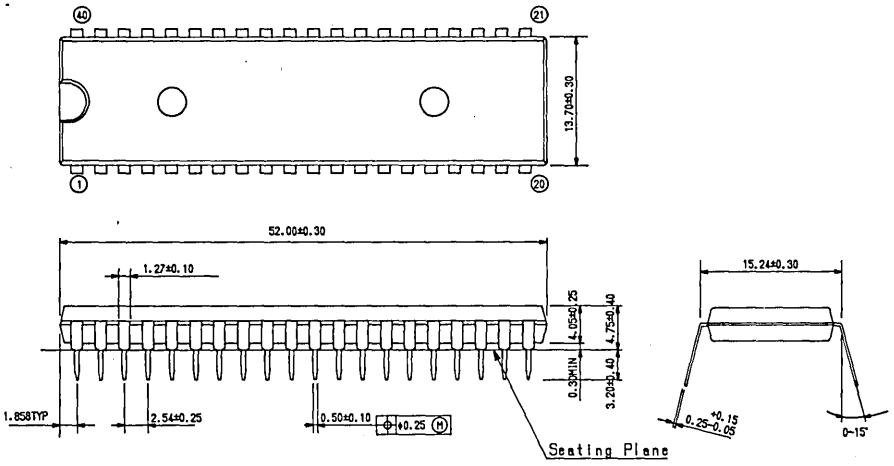

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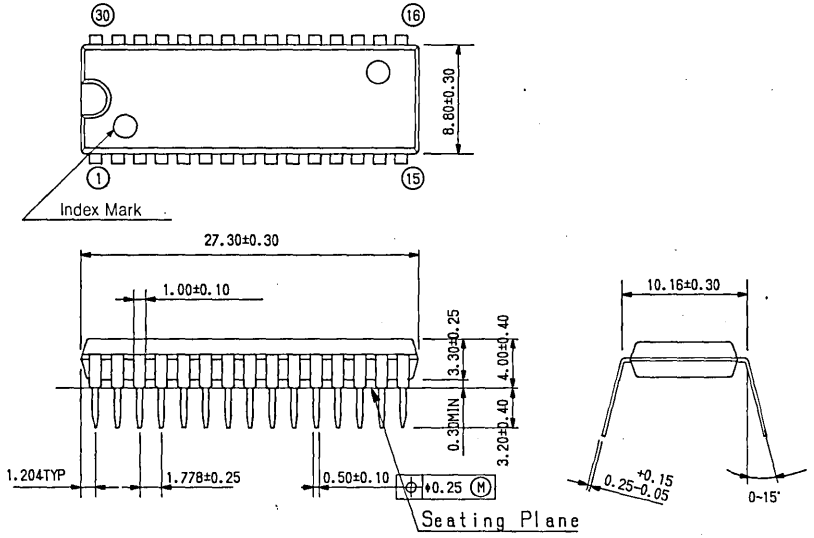

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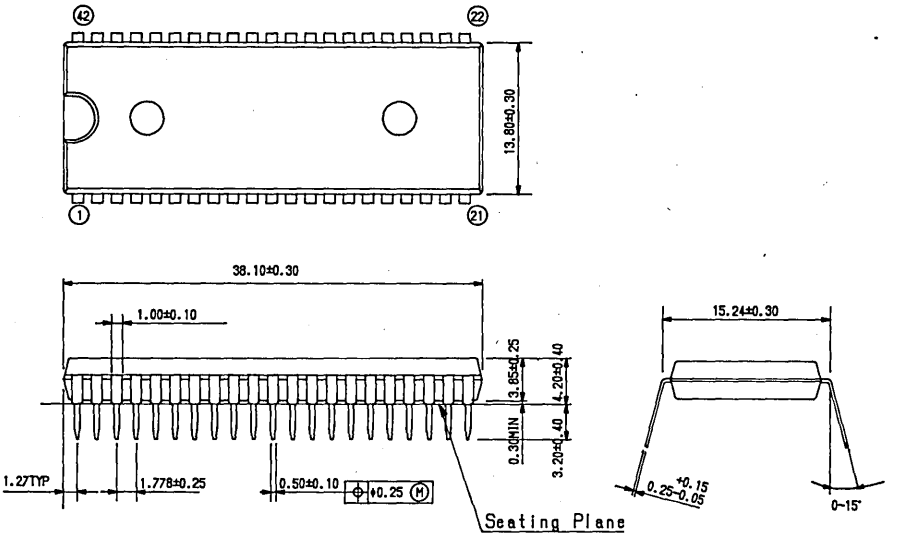
SDIP42-P-600



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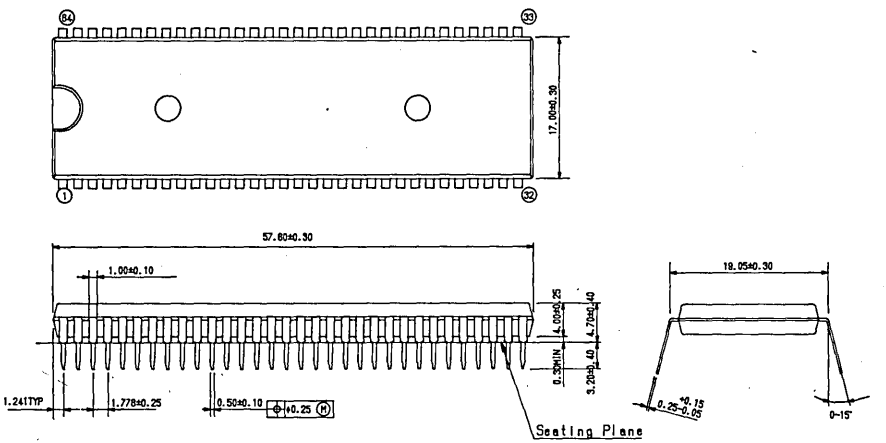

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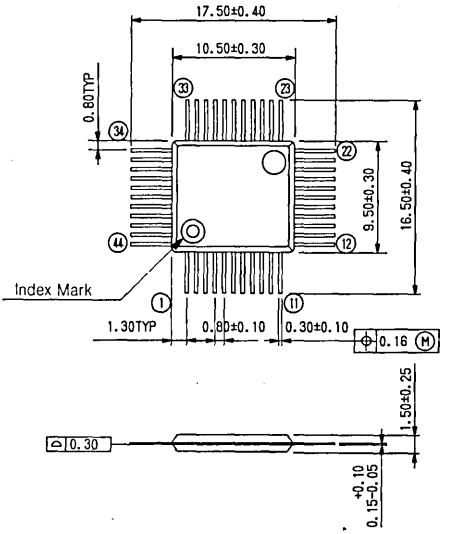

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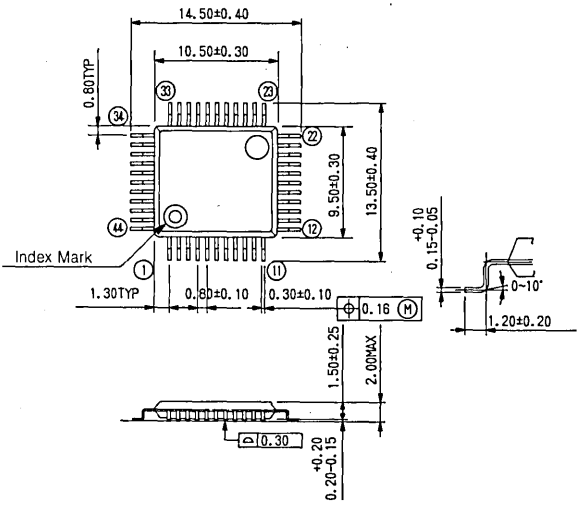

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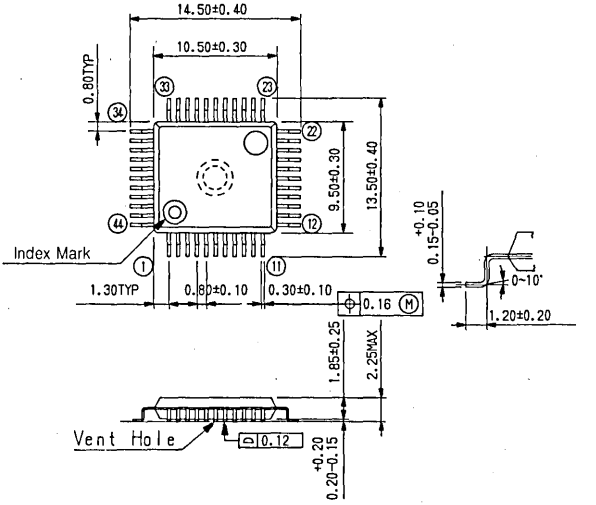

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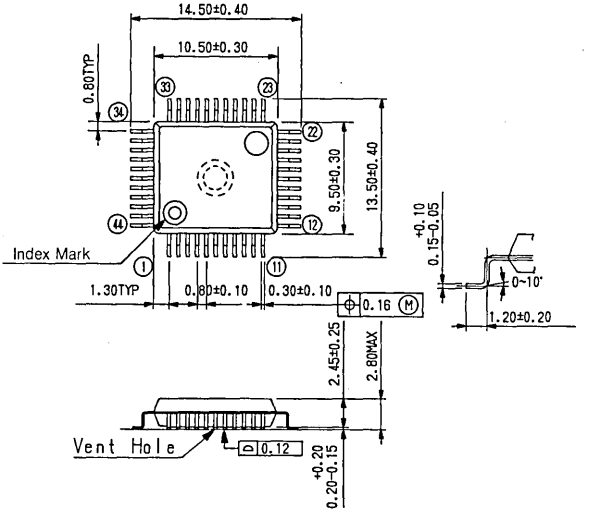

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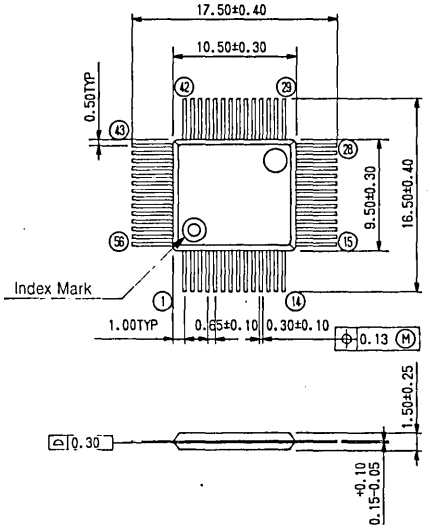

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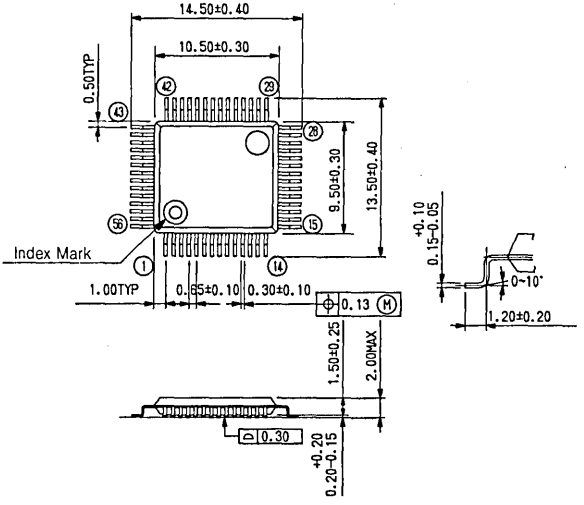

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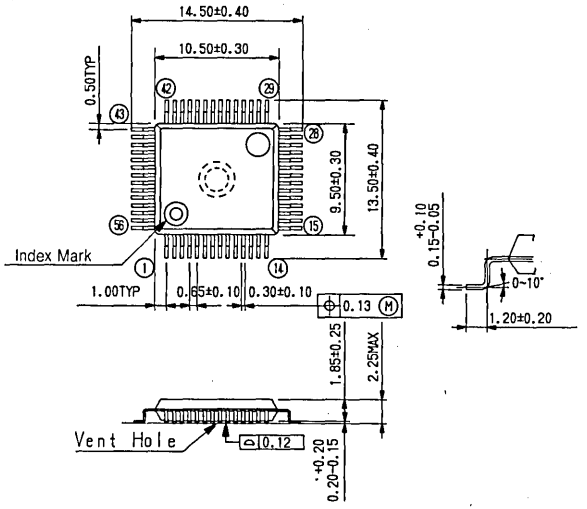

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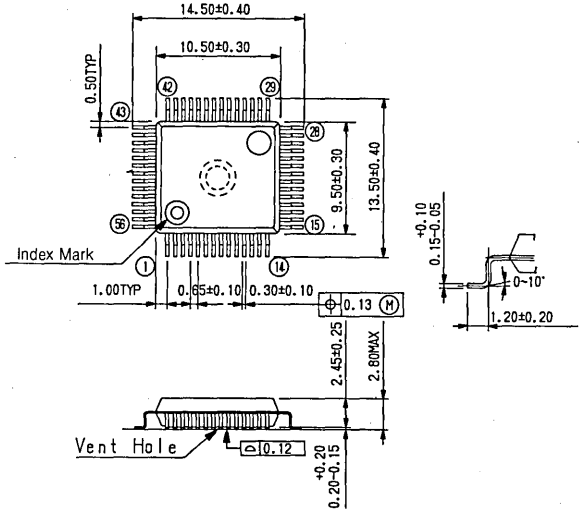

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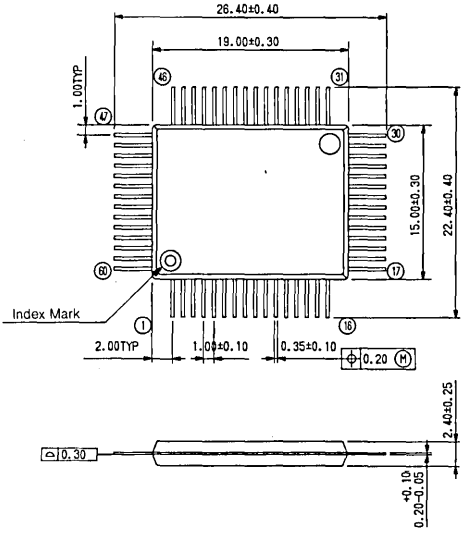

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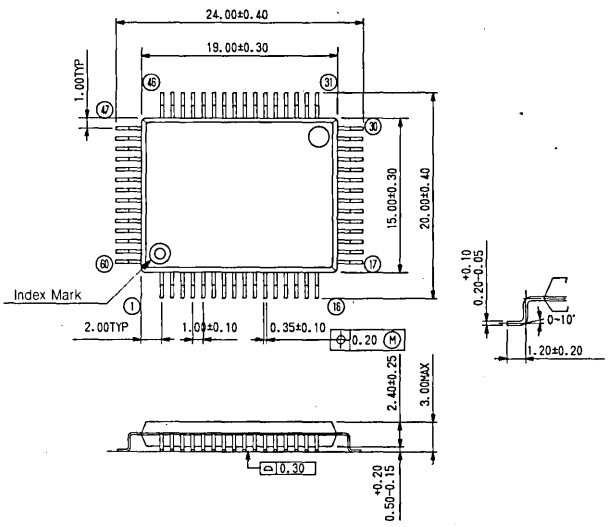

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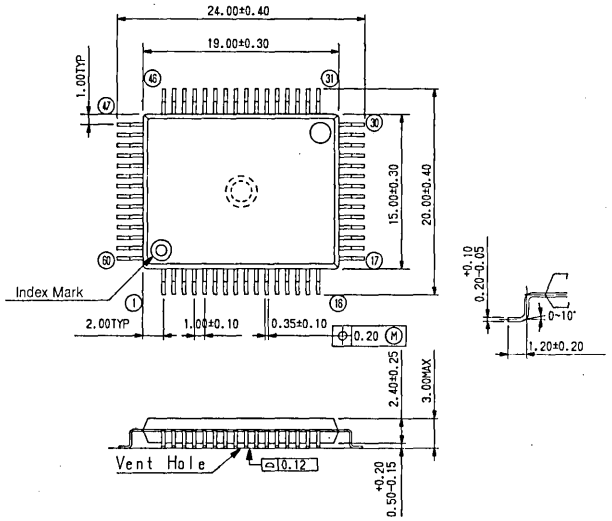

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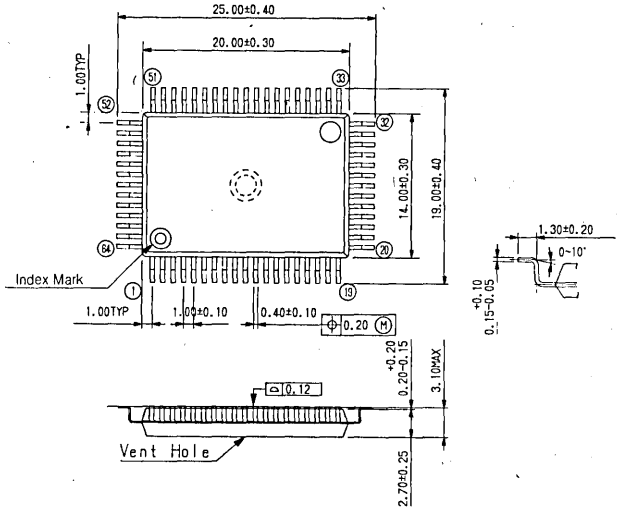

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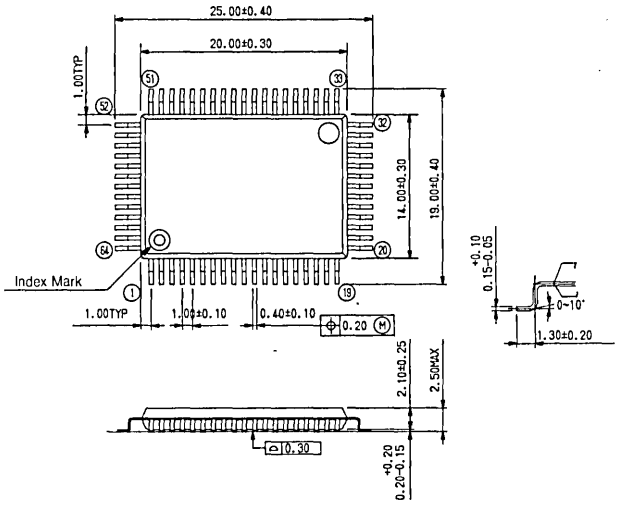

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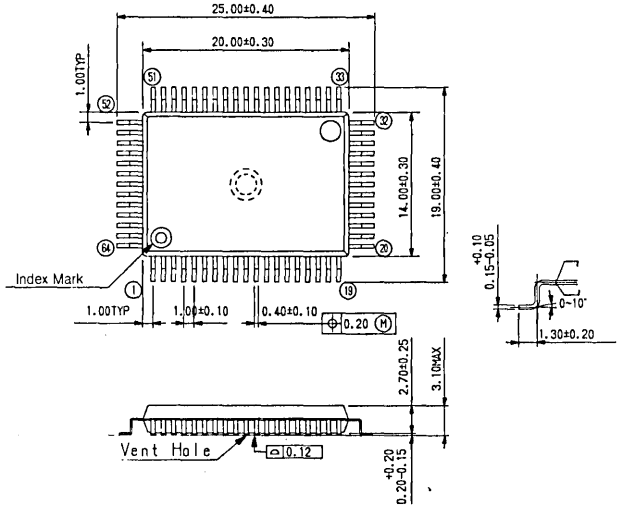

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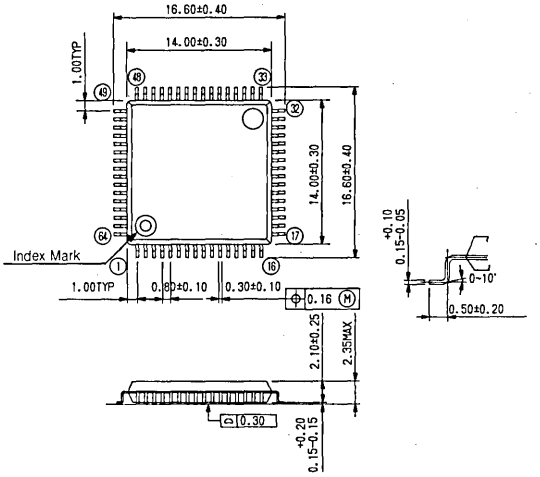
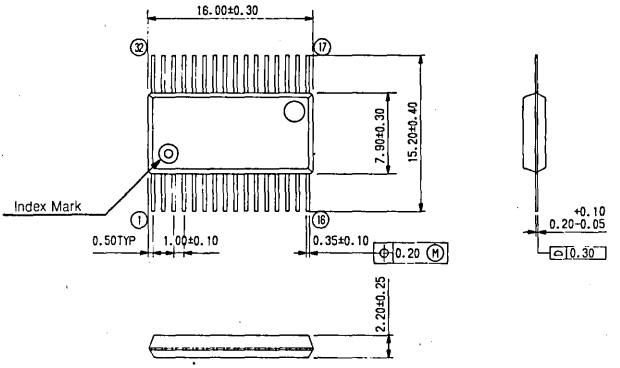


PLASTIC SOP

SSOP32-P



PLASTIC SOP

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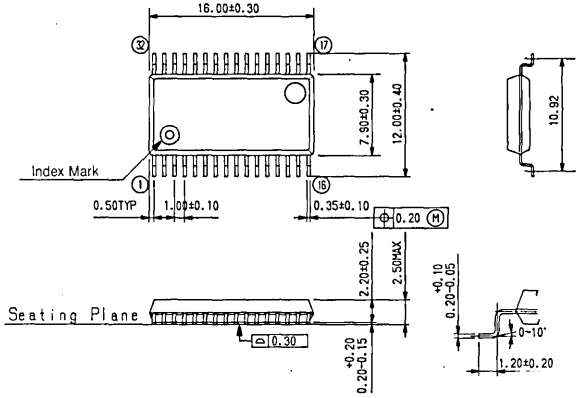

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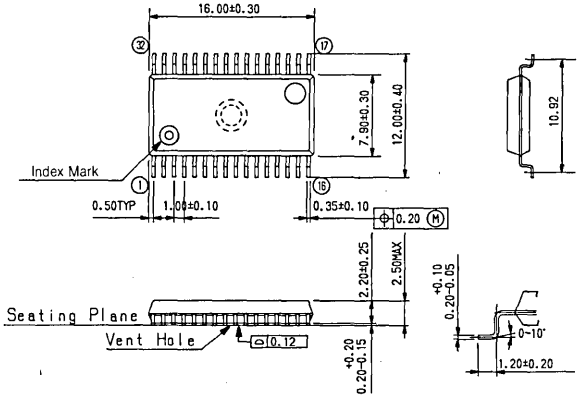

PLASTIC SOP

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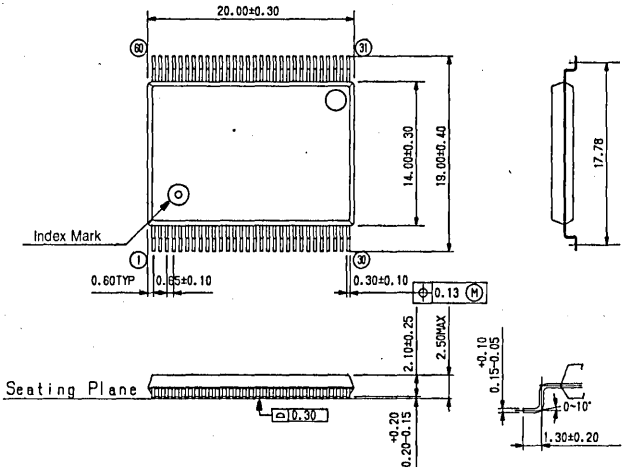

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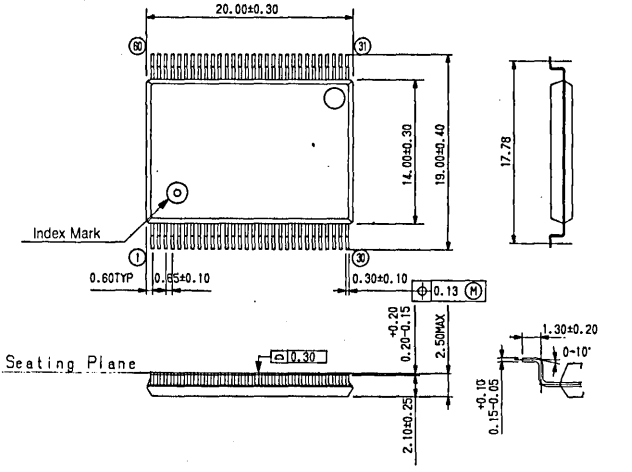
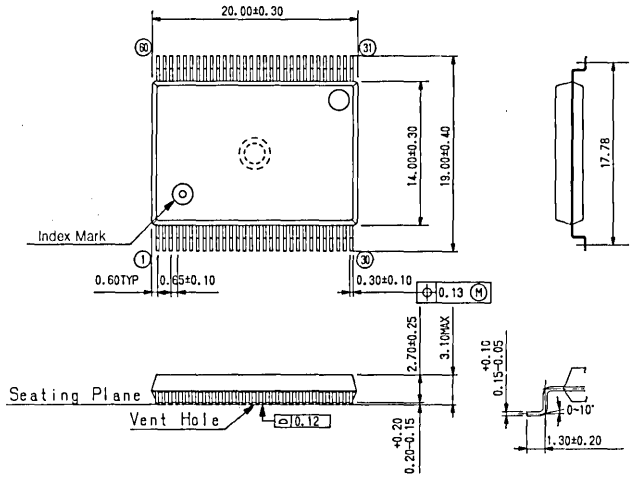


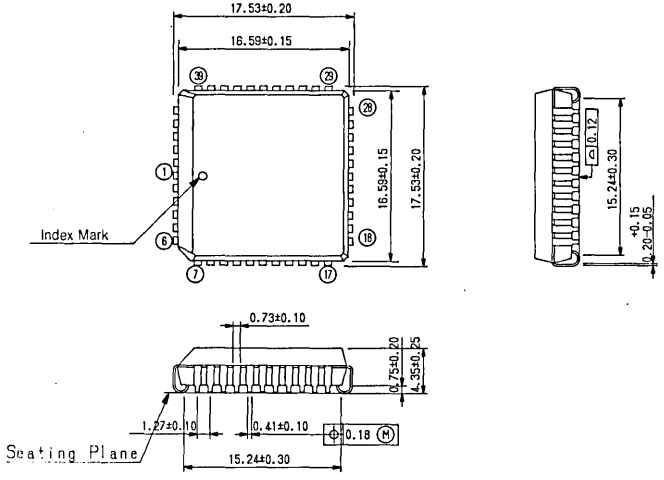
PLASTIC SOP

SSOP60-P-700-V1K



PLASTIC QFJ

QFJ44-P-S650



RELIABILITY INFORMATION

RELIABILITY INFORMATION

1. INTRODUCTION

Semiconductor devices play a leading role in the explosive progress of semiconductor technology. They use some of the most advanced design and manufacturing technology developed to date. With greater integration, diversity and reliability, their applications have expanded enormously. Their use in large scale computers, control equipment, calculators, electronic games and in many other fields has increased at a fast rate.

A failure in electronic banking or telephone switching equipment, for example, could have far reaching effects and can cause incalculable losses. So, the demand, for stable high quality memory devices is strong.

We, at Oki are fully aware of this demand. So we have adopted a comprehensive quality assurance system based on the concept of consistency in development, manufacturing and sales.

With the increasing demand for improvement in function, capability and reliability, we will expand our efforts in the future. Our quality assurance system and the underlying concepts are outlined briefy below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

The quality assurance system employed by Oki can be divided into four major stages: device planning, developmental prototype, production prototype, and mass production. This system is outlined in the following block diagram (Fig. 1).

1) Device planning stage

To manufacture devices that meet market demands and satisfy customer needs, we carefully consider functional and failure rate requirements, utilization form, environment and other conditions. Once we determine the proper type, material and structure, we check the design and manufacturing techniques, and the line processing capacity. Then we prepare the development planning and time schedule.

2) Developmental prototype stage

We determine circuits, pattern design, process settings, assembly techniques and structural requirements during this stage. At the same time, we carry out actual prototype reliability testing.

Since device quality is largely determined during the designing stage, Oki pays careful attention to quality confirmation during this stage.

This is how we do it:

(1) After completion of circuit design (or pattern design), personnel from the design, process technology, production technology, installation technology and reliability departments get together for a thorough review to ensure design quality and to anticipate problems that may occur during mass production. Past experience and know-how guide these discussions.

(2) Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.
Note: TEG (Test Element Group) refers to the device group designed for stability evaluation of MOS transistors, diodes, resistors, capacitors and other circuit component element used in LSI memories.

(3) Prototypes are subjected to repeated reliability and other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Production prototype stage

During this stage, various tests check the reliability and other special features of the production prototype at the mass production factory level. After confirming the quality of a device, we prepare the various standards required for mass production, and then start production. Although reliability and other special tests performed on the production prototype are much the same as those performed on the developmental prototype, the personnel, facilities and production site differ for the two prototypes, necessitating repeated confirmation tests.

4) Mass production

During the mass production stage, careful management of purchased materials, parts and facilities used during the manufacturing process, measuring equipment, manufacturing conditions and environment is necessary to ensure device quality first stipulated during the designing stages. The manufacturing process (including inspection of the completed device) is followed by a lot guarantee inspection to check that the specified quality is maintained under conditions identical to those under which a customer would actually use the device. This lot guarantee inspection is performed in three different forms as shown below.

(1) Group A tests: appearance, labels, dimensions and electrical characteristics inspection

(2) Group B tests: check of durability under thermal and mechanical environmental stresses, and operating life characteristics

(3) Group C tests: performed periodically to check operational life, etc., on a long term basis.

Note: Like the reliability tests, the group B tests conform to the following standards.
MIL-STD-883B, JIS C 7022, EIAJ-IC-121

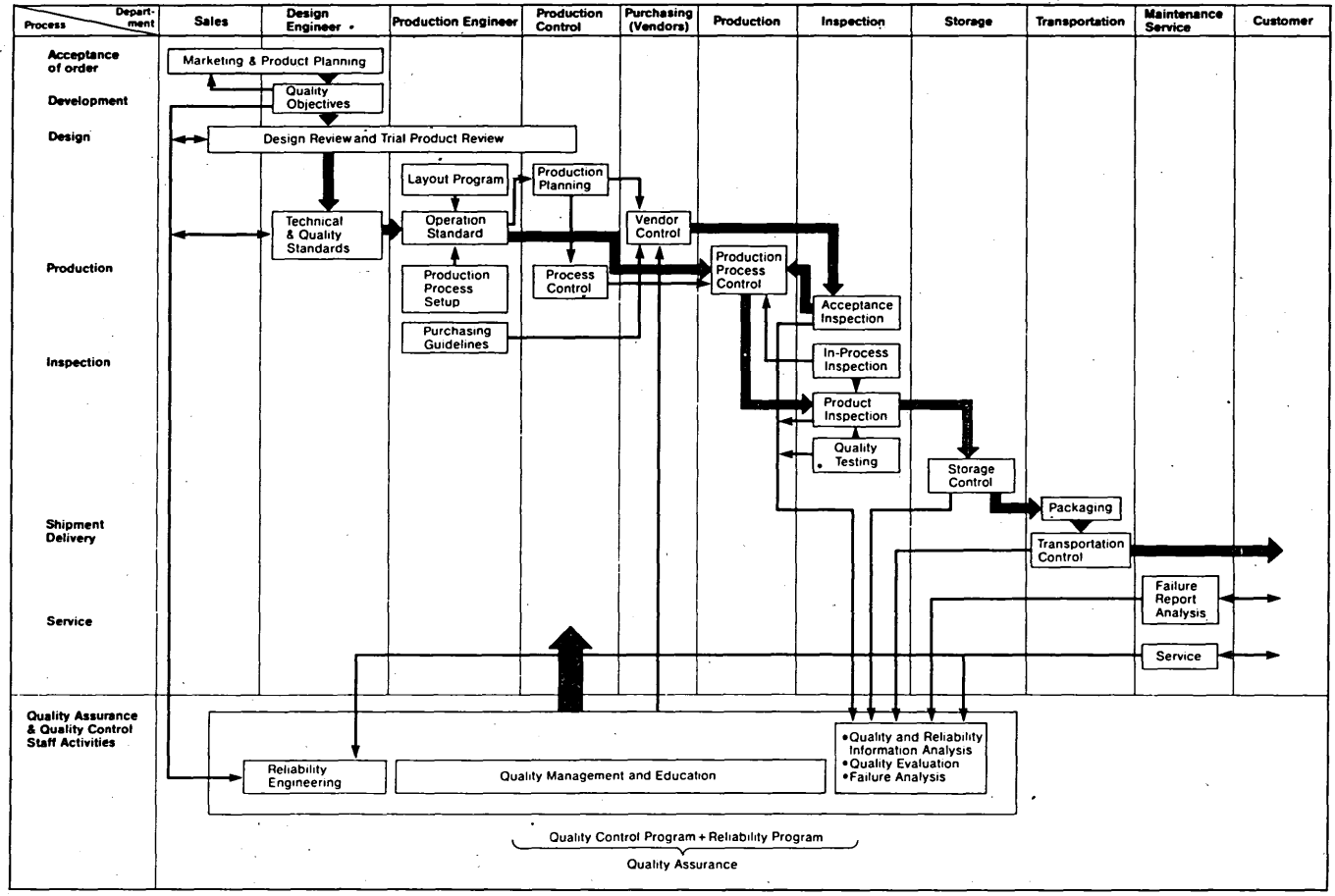


Figure 1 Quality Assurance System

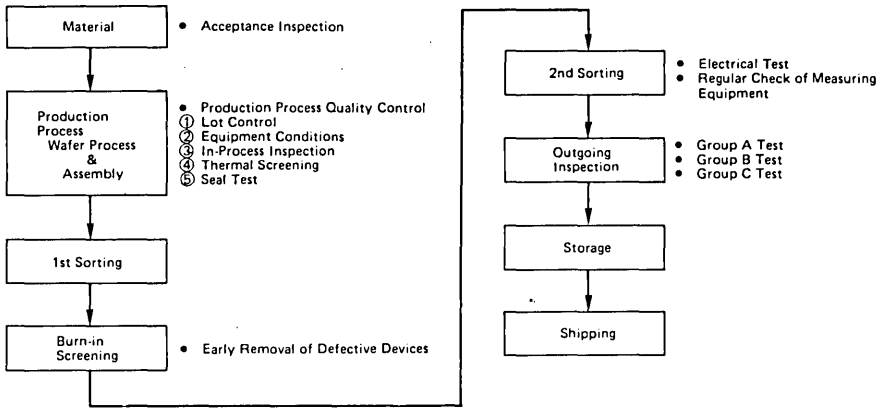


Figure 2 Manufacturing Process

Devices which pass these lot guarantee inspections are stored in a warehouse awaiting shipment to customers. Standards are also set up for handling, storage and transportation during this period, thereby ensuring quality prior to delivery. Figure 2 shows the manufacturing flow of the completed device.

5) At Oki, all devices are subjected to thorough quality checks. If, by chance, a failure does occur after delivery to the customer, defective devices are processed and the problem rectified immediately to minimize the inconvenience to the customer in accordance with the following flowchart.

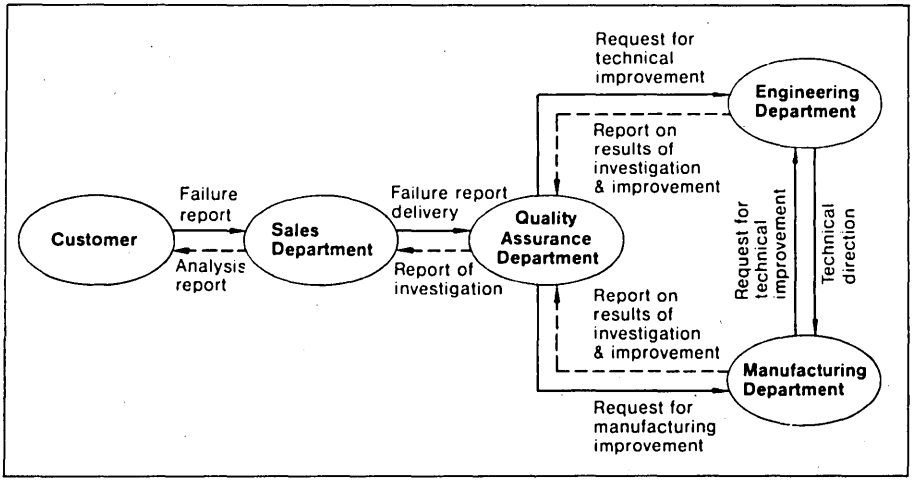
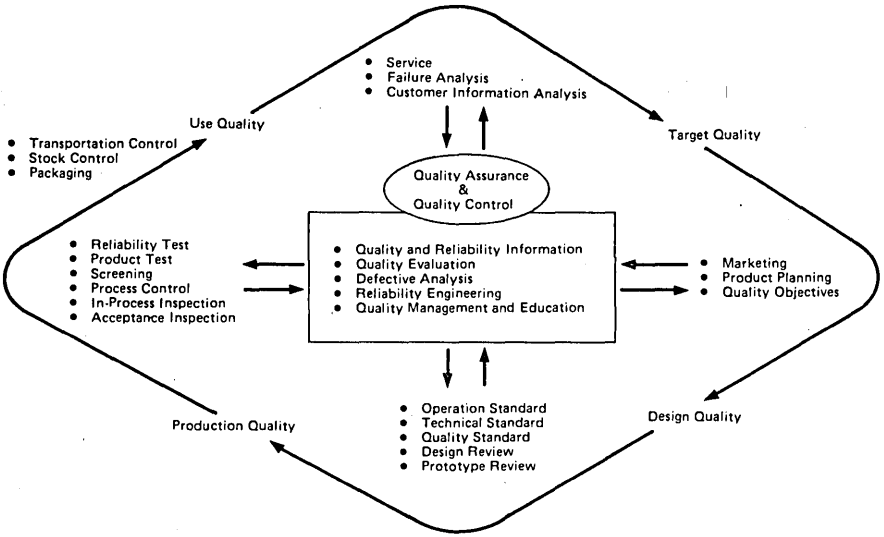


Figure 3 Failure report process



3. EXAMPLE OF RELIABILITY TEST RESULTS

We have outlined the quality assurance system and the underlying concepts employed by Oki. Now, we will give a few examples of the reliability tests performed during the developmental and production prototype stages. All reliability tests performed by Oki conform to the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

Since these reliability tests must determine performance under actual working conditions in a short period of time, they are performed under severe test conditions. For example, the 125°C high temperature continuous operation test performed for 1000 hours is equivalent to testing device life from 2 to 300 years of use at Ta = 40°C.
By repeating these accelerated reliability tests, device quality is checked and defects analyzed. The resulting information is extremely useful in improving the manufacturing processes. Some of the more common defects in LSI elements and their analysis are described on next page.

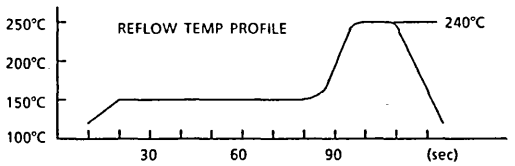
LIFE TEST RESULTS

Test Item	Test Condition	Part Name: MSL915RS — Sample Size (pcs)	MSL915RS — Test Hours or Cycles	MSL915RS — Failures	※ MSM5267B-XXGS-VK — Sample Size (pcs)	※ MSM5267B-XXGS-VK — Test Hours or Cycles	※ MSM5267B-XXGS-VK — Failures	MSC7110SS — Sample Size (pcs)	MSC7110SS — Test Hours or Cycles	MSC7110SS — Failures	※ MSC1162GS-V1K — Sample Size (pcs)	※ MSC1162GS-V1K — Test Hours or Cycles	※ MSC1162GS-V1K — Failures	Referred Standard
	Function	8-BIT PARALLEL-IN PARALLEL-OUT			DOT DRIVER			12-SEGMENT, 16-DIGIT			40-BIT ANODE/GRID DRIVER			
High Temperature Bias Test	Ta = 125°C Bias Condition MSL915RS ..... Note 1 MSM5267B-XXGS-XX .... Note 2 MSC7110SS ..... Note 3 MSC1162GS-V1K ..... Note 4	88	2000 (H)	0	88	2000 (H)	0	88	2000 (H)	0	88	2000 (H)	0	MIL-STD-883C Method 1005
Temperature Humidity Bias Test	Ta = 85°C PH = 85% Bias Condition MSL915RS ..... Note 1 MSM5267B-XXGS-XX .... Note 2 MSC7110SS ..... Note 3 MSC1162GS-V1K ..... Note 4	100	2000 (H)	0	100	2000 (H)	0	100	2000 (H)	0	100	2000 (H)	0	–
High Temperature Storage	Ta = 150°C	22	1000 (H)	0	22	1000 (H)	0	22	1000 (H)	0	22	1000 (H)	0	MIL-STD-883C Method 1008
Temperature Cycling Test	– 65°C ⇄ RT ⇄ 150°C (30 min) (5 min) (30 min)	100	500 (Cy)	0	100	500 (Cy)	0	100	500 (Cy)	0	100	500 (Cy)	0	MIL-STD-883C Method 1010
Pressure Cooker Test	Ta = 121°C RH = 100% 2 atm	50	200 (H)	0	50	200 (H)	0	50	200 (H)	0	50	200 (H)	0	–

- Note 1 (MSL915RS) VI-GND = 7V, V-GND = 60V
- Note 2 (MSM5267B-XXGS-VK) VDD-GND = 18V
- Note 3 (MSC7110SS) VDD-VSS = 5.5V, VDD-VEE = 45V
- Note 4 (MSC1162GS-V1K) VCC-GND = 5.5V, VHV-GND = 65V

※THE PRE DISPOSITION OF EACH SAMPLE

- 85°C 85% 72H STORAGE
- 125°C 16H BAKE
- REFLOW SOLDERING PACKAGE SURFACE TEMP
- LIFE TEST



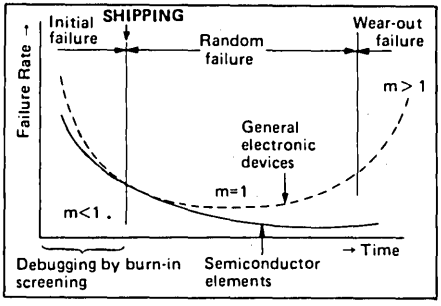
ENVIRONMENTAL TEST RESULTS

Test Item			Part Name	MSL915RS		MSM5267B-XXGS-VK		MSC7110SS		MSC1162GS-V1K		
			Function	8-BIT PARALLEL-IN PARALLEL-OUT		DOT DRIVER		12-SEGMENT, 16-DIGIT		40-BIT ANODE/GRID DRIVER		
			Test Condition	Sample Size (pcs)	Failures	Sample Size (pcs)	Failures	Sample Size (pcs)	Failures	Sample Size (pcs)	Failures	Referred Standard
Thermal Environmental Test	Soldering Heat Test		260°C 10 sec	22	0	22	0	22	0	22	0	MIL-STD-883C Method 2003
	↓ Temperature Cycling Test		−65°C ⇌ RT ⇌ 150°C (30 min) (5 min) (30 min) (20 cycles)									MIL-STD-883C Method 1010
	↓ Thermal Shock Test		100°C ⇌ 0°C (5 min) (5 min) 10 cycles									MIL-STD-883C Method 1011
Other Test	Lead Intgrity	Tensile	18P/42P Dip 500g 10 sec 44P/60P Flat 100g 10 sec	11	0	11	0	11	0	11	0	MIL-STD-883C Method 2004
		Bending	18P/42P Dip 250g 90° 3 times 44P/60P Flat 50g 90° 2 times									
	Solderability		230°C 5 sec	22	0	22	0	22	0	22	0	MIL-STD-883C Method 2003

4. SEMICONDUCTOR MEMORY FAILURES

The life-span characteristics of semiconductor elements in general (not only semiconductor IC devices) is described by the curve shown in the diagram below. Although semiconductor memory failures are similar to those of ordinary integrated circuits, the degree of integration (miniaturization), manufacturing complexity and other circuit element factors influence their incidence.

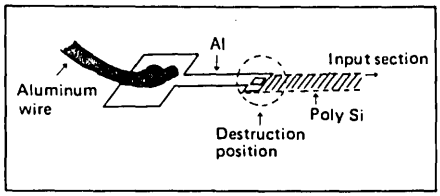
Semiconductor Element Failure Rate Curve



1) Surge Destruction

This is destruction of the input/output stage circuits by external surge currents or static electricity. The accompanying photograph shows a point of contact between aluminum and polysilicon that has been dissolved by a surge current. A hole has formed in the substrate silicon, leading to a short circuit. This kind of failure is traceable in about 30% of defective devices returned to the manufacturer. Despite miniaturization of semiconductor memory component elements (which means the elements themselves are less resistant), these failures usually occur during assembly and other handling operations.

At Oki, all devices are subjected to static electricity intensity tests (under simulated operational conditions) in the development stage to reduce this type of failure. In addition to checking endurance against surge currents, special protective circuits are incorporated in the input and output sections.



2) Oxide Film Insulation Destruction (Pin Holes)

Unlike surge destruction, this kind of failure is caused by manufacturing defects. Local weakened sections are ruptured when subjected to external electrical stress. Although this problem is accentuated by the miniaturization of circuit elements, it can be resolved by maintaining an ultra-clean manufacturing environment and through 100% burn-in screening.

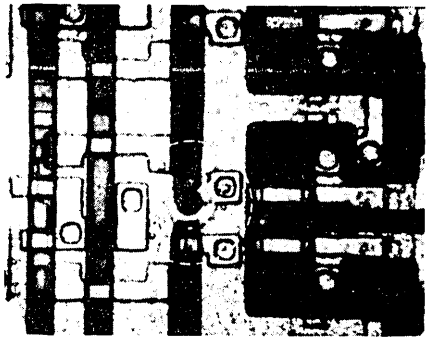
3) Surface Deterioration due to Ionic Impurities

Under some temperature and electric field conditions, charged ionic impurities moving within the oxide film previously resulted in occasional deterioration of silicon surfaces. This problem has been eliminated by new surface stabilization techniques.

4) Photolithographic Defects

Integrated circuits are formed by repeated photographic etching processes. Dust and scratches on the mask (which corresponds to a photographic negative) can cause catastrophic defects. At present, component elements have been reduced in size to the order of 10 cm through miniaturization. However, the size of dust and scratches stays the same. At Oki, a high degree of automation, minimizing human intervention in the process, and unparalleled cleanliness, solves this problem.

Example of surge destruction



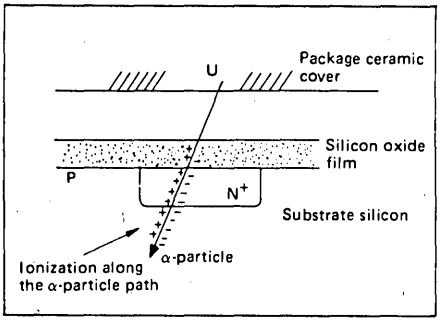
Photolithographic Defect

5) Aluminum Corrosion

Aluminum corrosion is due to electrolytic reactions caused by the presence of water and minute impurities. When aluminum dissolves, lines break. This problem is unique to the plastic capsules now used widely to reduce costs. Oki has carefully studied the possible cause and effect relationship between structure and manufacturing conditions on the one hand, and the generation of aluminum corrosion on the other. Refinements incorporated in Oki LSIs permit superior endurance to even the most severe high humidity conditions.

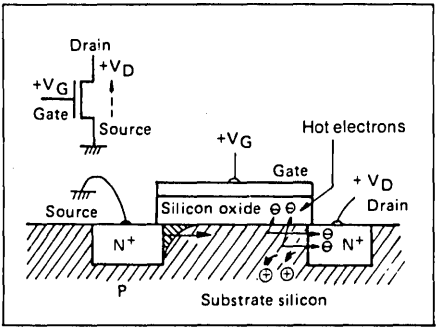
6) Alpha-Particle Soft Failure

This problem occurs when devices are highly miniaturized, such as in 1 megabit RAMs. The inversion of memory cell data by alpha-particle generated by radio-active elements like uranium and thorium (present in minute quantities, measured in ppb) in the ceramic package material causes defects. Since failure is only temporary and normal operation restored quickly, this is referred to as a "soft" failure. At Oki we have eliminated the problem by coating the chip surface of 1 megabit RAMs with a resin which effectively screens out these alpha-particles.



7) Degradation in Performance Characteristics Due to Hot Electrons

With increased miniaturization of circuit elements, internal electric field strength in the channels increases since the applied voltage remains the same at 5V. As a result, electrons flowing in the channels, as shown in the accompanying diagram, tend to enter into the oxide film near the drain, leading to degradation of performance. Although previous low-temperature operation tests have indicated an increase of this failure, we have confirmed by our low-temperature acceleration tests, including checks on test element groups, that no such problem exists in Oki LSIs.



Characteristic deterioration caused by hot electrons

With further progress in the miniaturization of circuit components, failures related to pin hole oxide film destruction and photolithography have increased. To eliminate these defects during manufacturing, Oki has been continually improving its production processes based on reliability tests and information gained from the field. And we subject all devices to high-temperature burn-in screening for 48 to 96 hours to ensure even greater reliability.

DATA SHEETS

Driver

OKI semiconductor
MSL912

8-BIT PARALLEL-IN PARALLEL-OUT

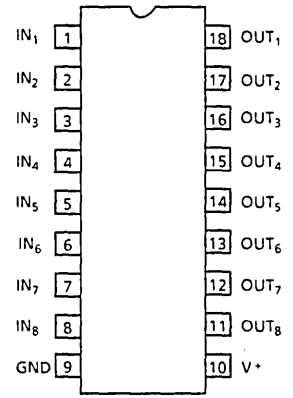
GENERAL DESCRIPTION

The MSL912 is a high voltage vacuum fluorescent display tube driver, which uses positive voltage and contains eight circuits. Each output contains a pull-down resistor, which allows the driver to directly drive the vacuum fluorescent display tube.

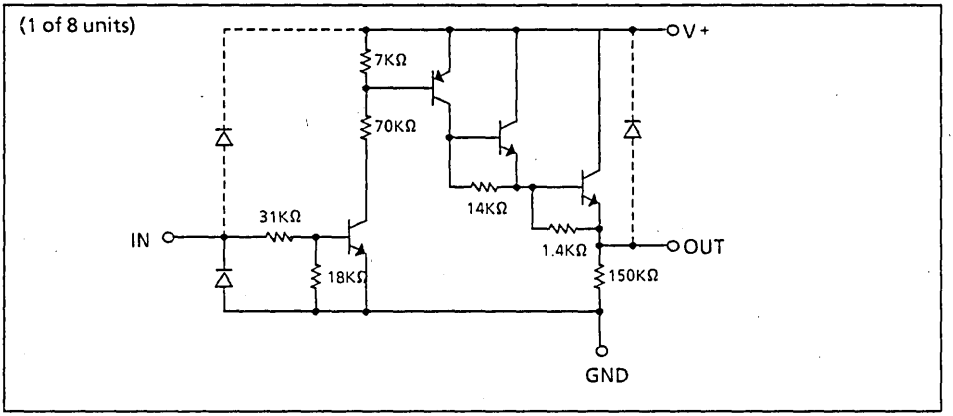
Input may be driven directly by the TTL or CMOS.

PIN CONFIGURATION

(Top View) 18 Lead Plastic DIP



CIRCUIT CONFIGURATION



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V+	Ta = 25 °C	−0.3~35	V
Input voltage	V_I	Ta = 25 °C	−0.5~10	V
Output voltage	Vo	Ta = 25 °C	−0.3~35	V
Output current	Io	Ta = 25 °C, only one circuit ON	+0.6~−45	mA
Storage temperature	Tstg	—	−55~+150	°C

• Recommended Operating Conditions

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V+	—	15~30	V
Input voltage	V_I	—	0~7	V
Output current	Io	Only one circuit ON*	+0.5~−40	mA
		Per circuit when all circuits are ON*	+0.5~−5	mA
		Total output current*	+0.5x8~−40	mA
Operating temperature	Top	—	−30~+75	°C

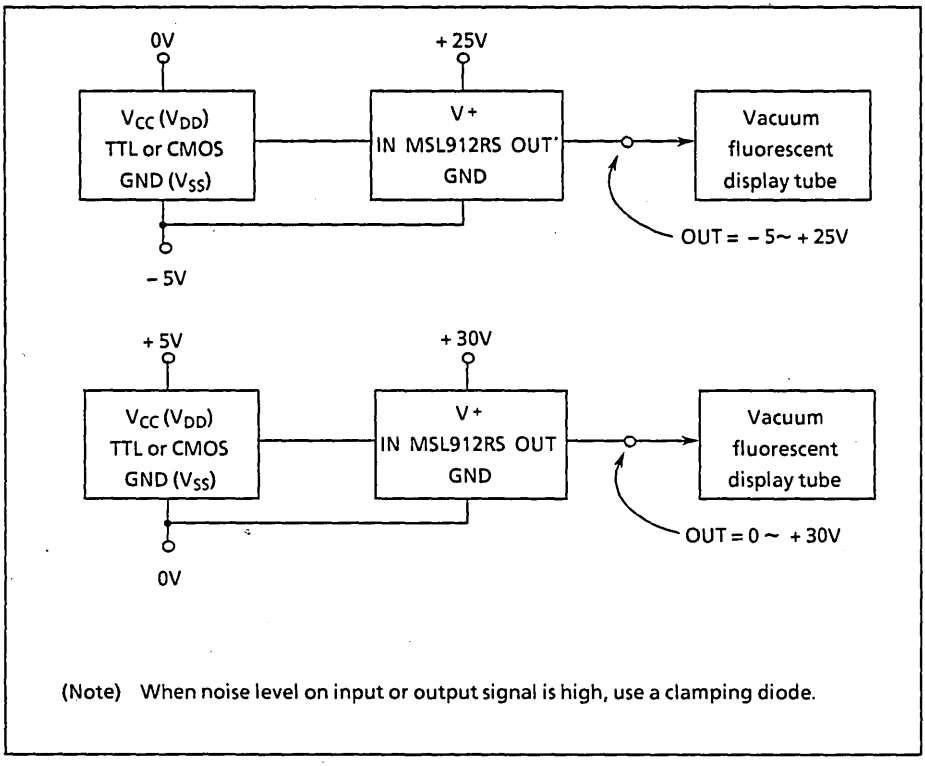
* Duty: 50% max.

• DC Characteristics

(Ta = −30~+75°C, TYP: Ta = 25°C)

Parameter	Symbol	Condition			Specification			Unit
		V+ (V)	V_I(V)	IO(mA)	MIN	TYP	MAX	
High input voltage	V_{IH}	30	—	—	2.5	—	—	V
Low input voltage	V_{IL}	30	—	—	—	—	1.0	V
Low input current	I_{IL}	30	1.0	—	—	20	80	μA
High input current	I_{IH1}	30	2.5	—	—	0.09	0.22	mA
	I_{IH2}	30	7	—	—	0.29	0.7	mA
High output voltage	V_{OH}	30	2.5	−40	27	28.5	—	V
Low output voltage	V_{OL}	30	1.0	0	—	1.0	3.0	V
Supply current	$I_{CC\,OFF}$	30	ALL INPUTS 1.0	0	—	0.04	0.4	mA
	$I_{CC\,ON}$	30	ALL INPUTS 2.5	0	—	12	17	mA
Pull-down resistor	R_{PD}	30	ALL INPUTS 0	Vo = 27V	60	150	270	KΩ

APPLICATION NOTE



(Note) When noise level on input or output signal is high, use a clamping diode.

OKI semiconductor
MSL915

8-BIT PARALLEL-IN PARALLEL-OUT

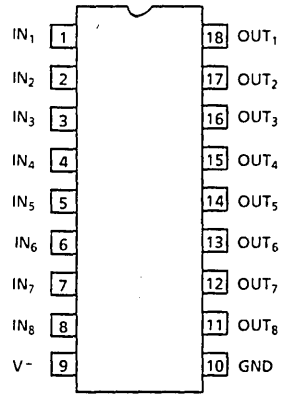
GENERAL DESCRIPTION

The MSL915 is a high voltage vacuum fluorescent display tube driver, which uses negative voltage and contains eight circuits. Each output contains a pull-down resistor, which allows the driver to directly drive the vacuum fluorescent display tube.

Input may be driven directly by the TTL or CMOS.

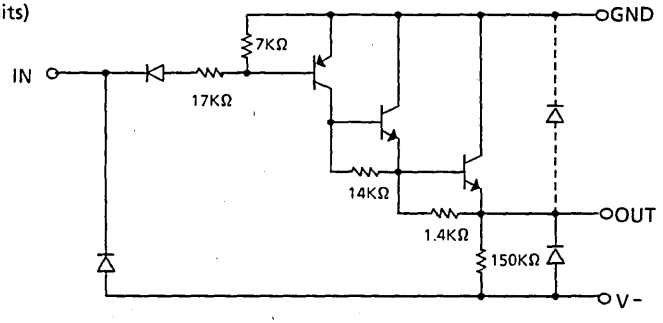
PIN CONFIGURATION

(Top View) 18 Lead Plastic DIP



CIRCUIT CONFIGURATION

(1 of 8 units)



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V-	Ta = 25 °C	GND + 0.3~GND – 65	V
Input voltage	V_I	Ta = 25 °C	GND + 0.5~GND – 10	V
Output voltage	Vo	Ta = 25 °C	GND + 0.3~V- – 0.5	V
Output current	Io	Ta = 25 °C, only one circuit ON	+ 0.9~ – 45	mA
Storage temperature	Tstg	—	– 55~ + 150	°C

• Recommended Operating Conditions

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V-	—	GND – 20~GND – 60	V
Input voltage	V_I	—	GND~GND – 7	V
Output current	Io	Only one circuit ON*	+ 0.8~ – 40	mA
		Per circuit when all circuits are ON*	+ 0.8~ – 5	mA
		Total output current*	+ 0.8x8~ – 40	mA
Operating temperature	Top	—	– 30~ + 75	°C

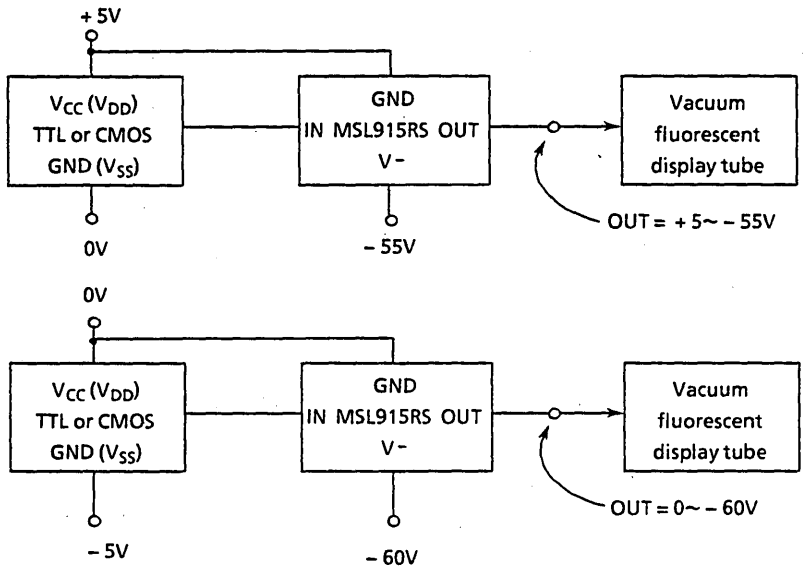
* Duty: 50% max.

• DC Characteristics

(Ta = – 30~ + 75°C, TYP: Ta = 25°C)

Parameter	Symbol	Condition			Specification			Unit
		V-(V)	V_I(V)	IO(mA)	MIN	TYP	MAX	
High input voltage	V_{IH}	– 60	—	—	—	—	– 1.5	V
Low input voltage	V_{IL}	– 60	—	—	– 4	—	—	V
High input current	I_{IH}	– 60	– 1.5	—	—	– 70	– 280	μA
Low input current	I_{IL1}	– 60	– 4	—	—	– 0.23	– 1.2	mA
	I_{IL2}	– 60	– 7	—	—	– 0.58	– 2.6	mA
High output voltage	V_{OH}	– 60	– 4	– 40	—	– 1.5	– 3	V
Low output voltage	V_{OL}	– 60	– 1.5	0	– 55	– 59	—	V
Supply current	$I_{CC\,OFF}$	– 60	ALL INPUTS – 1.5	0	—	0.7	1.3	mA
	$I_{CC\,ON}$	– 60	ALL INPUTS – 4	0	—	6	12	mA
Pull-down resistor	R_{PD}	– 60	ALL INPUTS 0	Vo = – 3V	60	150	270	KΩ

APPLICATION NOTE



(Note) When noise level on input or output signal is high, use a clamping diode.

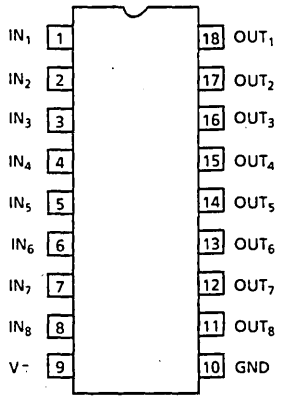
OKI semiconductor
MSL917
8-BIT PARALLEL-IN PARALLEL-OUT

GENERAL DESCRIPTION

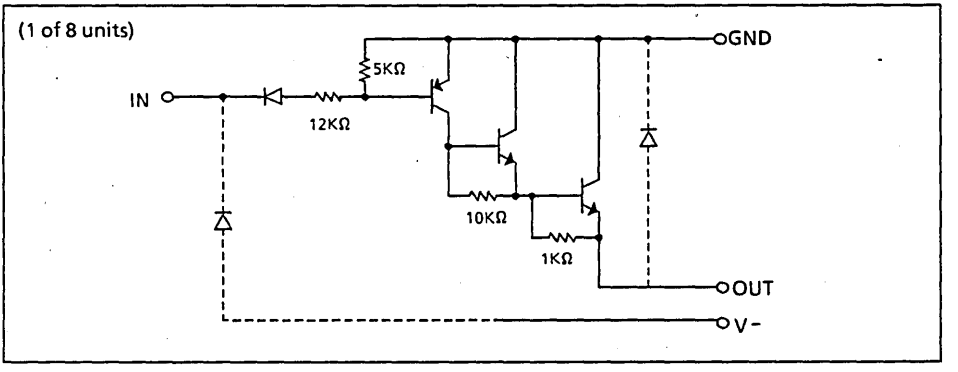
The MSL917 is a high voltage vacuum fluorescent display tube driver, which uses negative voltage and contains eight circuits. Each output does not contain a pull-down resistor, hence it should be connected to an external resistor (about 150KΩ).
Input may be driven directly by the TTL or CMOS. The vacuum fluorescent display tube driver may also be used as a high voltage and current driver.

PIN CONFIGURATION

(Top View) 18 Lead Plastic DIP



CIRCUIT CONFIGURATION



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V-	Ta = 25 °C	GND + 0.3~GND – 85	V
Input voltage	V_I	Ta = 25 °C	GND + 0.5~GND – 10	V
Output voltage	Vo	Ta = 25 °C	GND + 0.3~GND – 85	V
Output current	Io	Ta = 25 °C, only one circuit ON	0~ – 100	mA
Storage temperature	Tstg	—	– 55~ + 150	°C

• Recommended Operating Conditions

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V-	—	GND – 20~GND – 80	V
Input voltage	V_I	—	GND~GND – 7	V
Output current	Io	Only one circuit ON*	0~ – 90	mA
		Per circuit when all circuits are ON*	0~ – 11	mA
		Total output current	0~ – 90	mA
Operating temperature	Top	—	– 30~ + 75	°C

* Duty: 50% max.

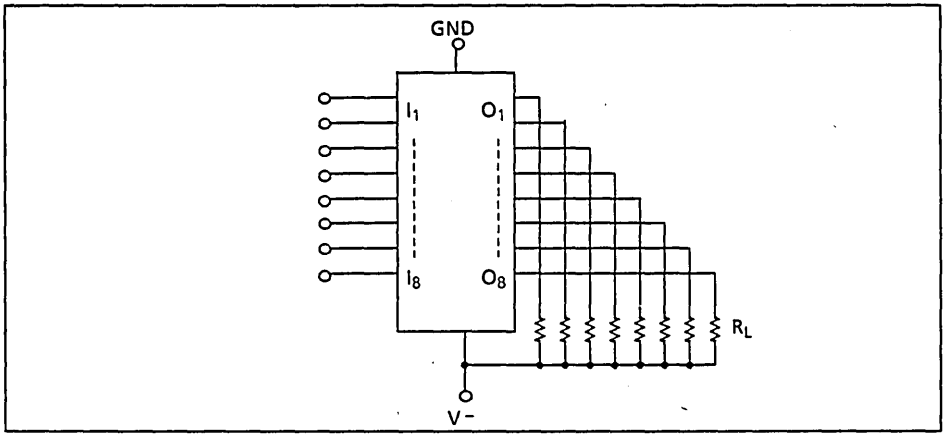
• DC Characteristics

(Ta = – 30~ + 75°C, TYP: Ta = 25°C)

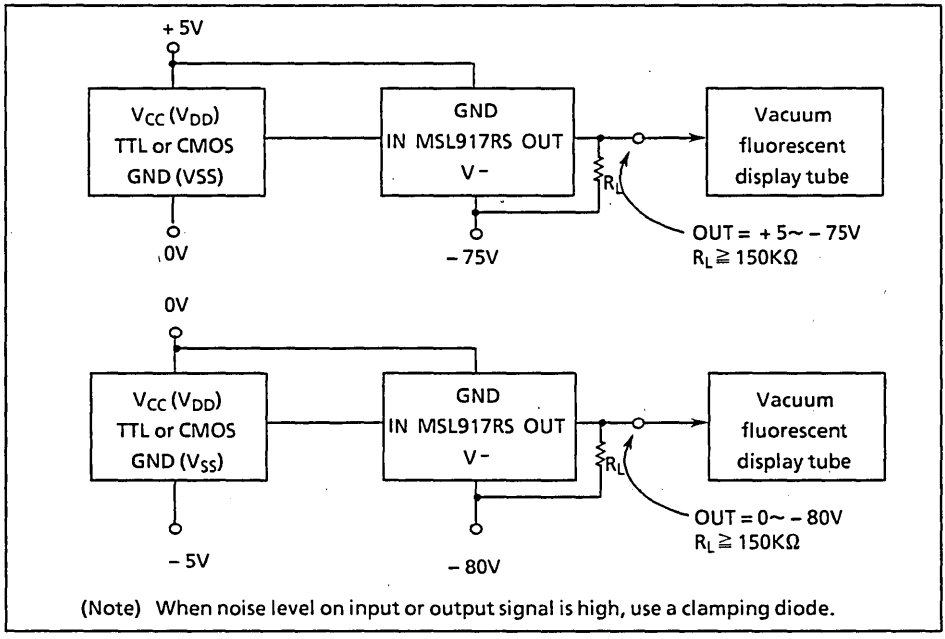
Parameter	Symbol	Condition				Specification			Unit
		V-(V)	V_I(V)	Io(mA)	RL(Ω)	MIN	TYP	MAX	
High input voltage	V_{IH}	– 80	—	—	—	—	—	– 1.5	V
Low input voltage	V_{IL}	– 80	—	—	—	– 4	—	—	V
High input current	I_{IH}	– 80	– 1.5	—	—	—	– 70	– 280	μA
Low input current	I_{IL1}	– 80	– 4	—	—	—	– 0.23	– 1.2	mA
	I_{IL2}	– 80	– 7	—	—	—	– 0.58	– 2.6	mA
High output voltage	V_{OH}	– 80	– 4	– 90	—	—	– 2.0	– 3.0	V
Low output voltage	V_{OL}	– 80	– 1.5	0	*1 150K	– 75	– 79	—	V
Supply current	$I_{CC\,OFF}$	– 80	ALL INPUTS – 1.5	—	*1 150	—	0.7	1.3	mA
	$I_{CC\,ON}$	– 80	ALL INPUTS – 4	—	*1 150K	—	8	14	mA

*1 R_L connection method

R_L CONNECTION METHOD



APPLICATION NOTE



(Note) When noise level on input or output signal is high, use a clamping diode.

OKI semiconductor
MSL918

8-BIT PARALLEL-IN PARALLEL-OUT

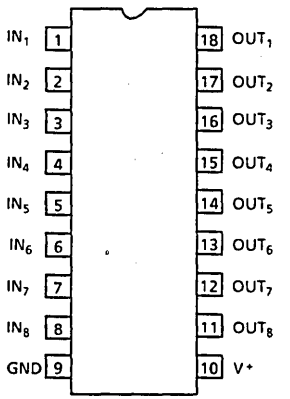
GENERAL DESCRIPTION

The MSL918 is a high voltage vacuum fluorescent display tube driver, which uses positive voltage and contains eight circuits. Each output does not contain a pull-down resistor, hence it should be connected to an external resistor (about 150 KΩ).

Input may be driven directly by the TTL or CMOS. The vacuum fluorescent display tube driver may also be used as a high voltage and current driver.

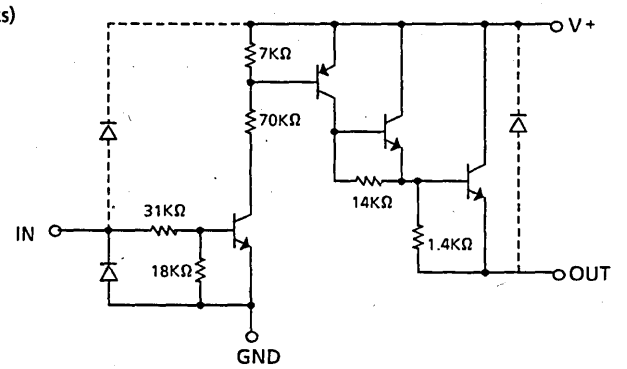
PIN CONFIGURATION

(Top View) 18 Lead Plastic DIP



CIRCUIT CONFIGURATION

(1 of 8 units)



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V+	Ta = 25 °C	−0.3~+35	V
Input voltage	V_I	Ta = 25 °C	−0.5~+10	V
Output voltage	Vo	Ta = 25 °C	−0.3~V+	V
Output current	Io	Ta = 25 °C, only one circuit ON	−45	mA
Storage temperature	Tstg	—	−55~+150	°C

• Recommended Operating Conditions

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V+	—	+15~+30	V
Input voltage	V_I	—	0~+7	V
Output current	Io	Only one circuit ON*	0~−40	mA
		Per circuit when all circuits are ON*	0~−11	mA
		Total output current*	0~−90	mA
Operating temperature	Top	—	−30~+75	°C

* Duty: 50% max.

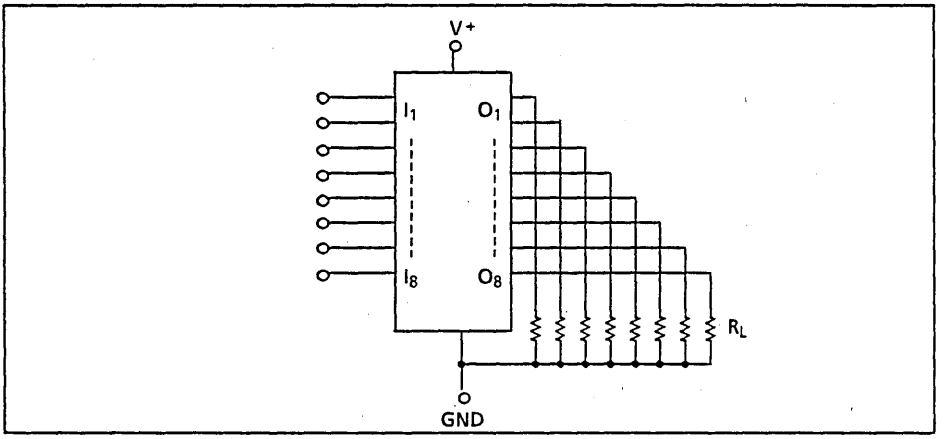
• DC Characteristics

(Ta = −30~+75°C, TYP: Ta = 25°C)

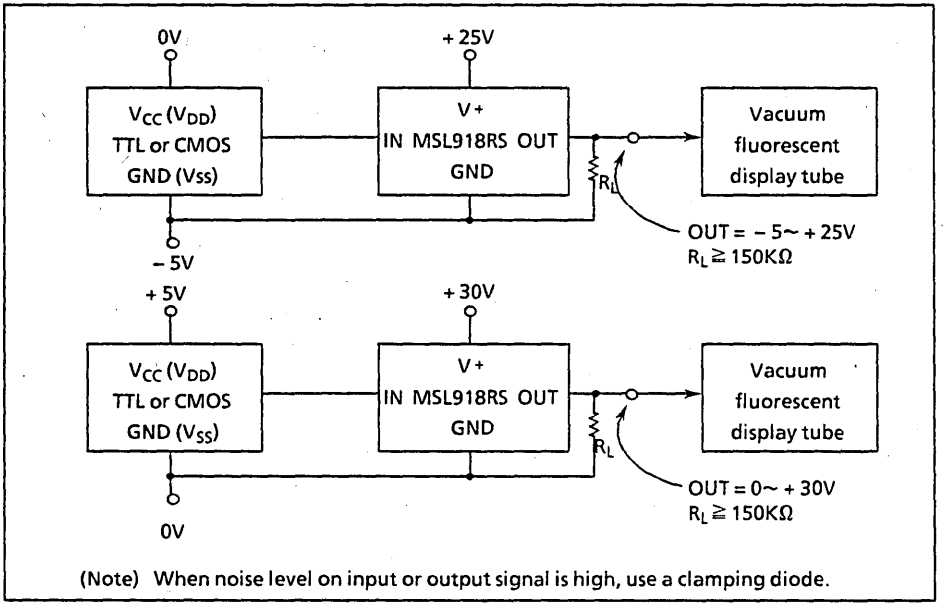
Parameter	Symbol	Condition				Specification			Unit
		V+(V)	V_I(V)	Io(mA)	RL(Ω)	MIN	TYP	MAX	
High input voltage	V_{IH}	+30	—	—	—	2.5	—	—	V
Low input voltage	V_{IL}	+30	—	—	—	—	—	1.0	V
Low input current	I_{IL}	+30	1.0	—	—	—	−20	−80	μA
High input current	I_{IH1}	+30	2.5	—	—	—	—	0.15	mA
	I_{IH2}	+30	7	—	—	—	—	0.5	mA
High output voltage	V_{OH}	+30	2.5	−40	—	27	—	—	V
Low output voltage	V_{OL}	+30	1.0	0	*1 150K	—	—	3.0	V
Supply current	$I_{CC\,OFF}$	+30	ALL INPUTS 1.0	—	*1 150	—	—	0.4	mA
	$I_{CC\,ON}$	+30	ALL INPUTS 2.5	—	*1 150K	—	9.5	14	mA

*1 R_L connection method

R_L CONNECTION METHOD



APPLICATION NOTE



(Note) When noise level on input or output signal is high, use a clamping diode.

OKI semiconductor
MSC1163

40-BIT ANODE DRIVER

GENERAL DESCRIPTION

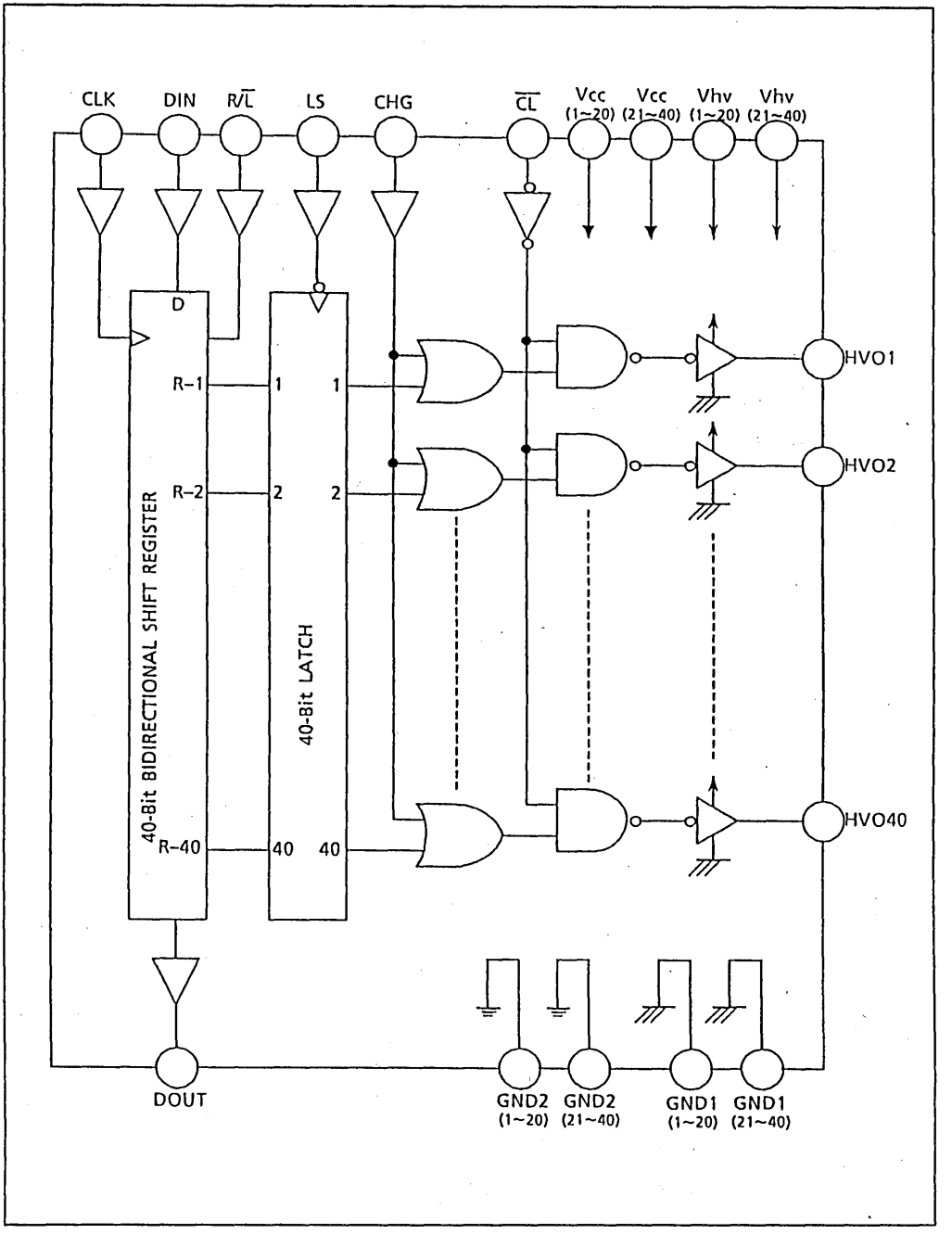
The MSC1163 is a monolithic IC using the Bi-CMOS process for hybridizing CMOS and bipolar transistors on the same chip. The logic portion such as the input stage, shift register and latch is formed by CMOS and the output driver requiring a high withstand voltage is formed by bipoalr transistors.
Since the pin asignment allows single side pattern formation on the printed circuit board, the display unit size can be reduced.
The bidirectional shift register facilitates the pattern design when the deivces are arranged symmetrically with the display as the center axis.

FEATURES

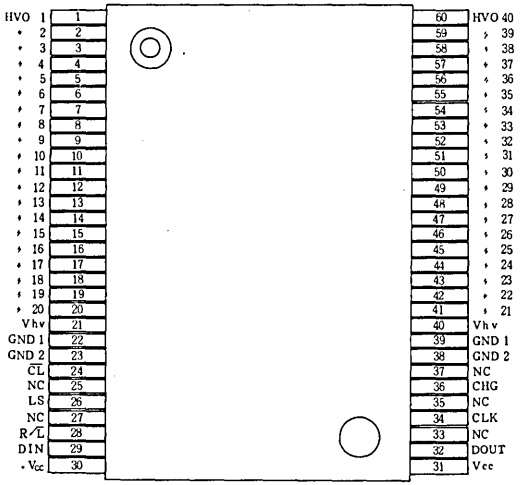
Designed as a VFD anode driver for emitter-follower force output with 40-bit active pull down by built-in 40-bit bidirectional shift register and latch.

- Logic Supply Voltage : Vcc : + 5V
- Driver Supply Voltage : Vhv : + 65V
- Driver Output Current : Iohvh : − 2 mA
  Iohvl : 2 mA
- Built-in 40-Bit latch
- Built-in 40-Bit bidirectional shift register
- Clock frequency : 4 MHz
- 60 pin FLAT Package

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

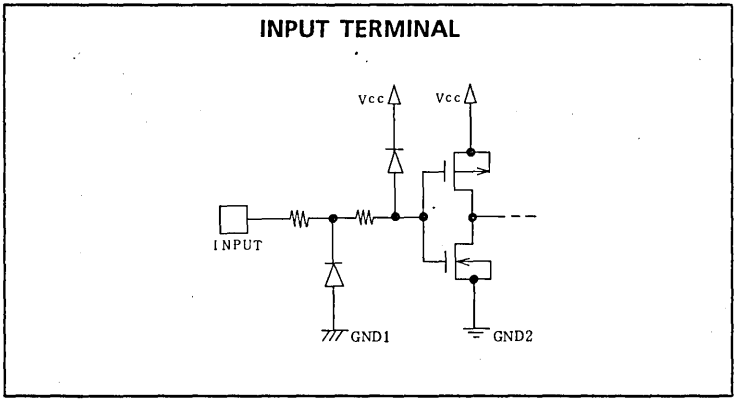


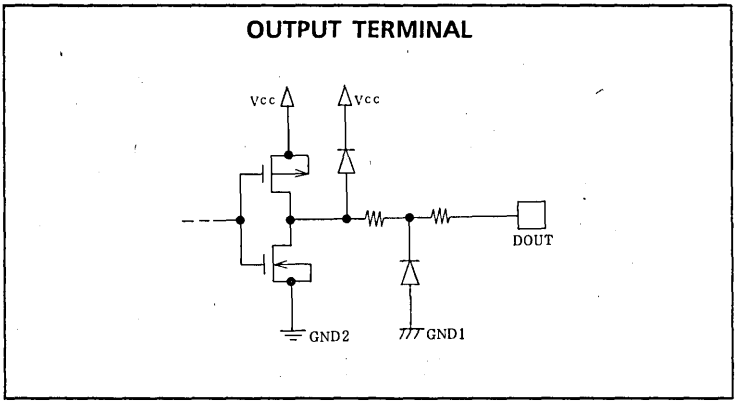
PIN DESCRIPTION

Pin No.	Symbol	Terminal Name	Description
1~20 41~60	HVO1~ HVO40	Driver Output	Driver output terminal, applicable to each bit of shift resistor.
21 40	Vhv	Driver Power Supply	Power supply terminal for driver circuit.
22 39	GND 1	Driver GND	GND pin for driver circuit.
23 38	GND 2	Logic GND	GND pin for the logic circuit. As GND1 and GND2 are not connected inside of the LSI, they need to be connected outside by same wiring.
24	$\overline{CL}$	Clear Input	Clear input pin with pull-up resister. Normally "H" level, in this condition driver output change "H" or "L" according to latch output level. when "L" driver output pins are fixed to "L" and have no relation with latch outputs.
26	LS	Latch Strobe Input	Latch strobe input pin. When LS is "H", information present at the data input is transferred to output. The information is kept latched and the output remains the same, even then LS changes to "L".
28	$R/\overline{L}$	Shift Direction Control	Shift direction control pin with pull-up resistetr. Normally "H", and in this condition, information of Bi-directional SR is shifted to the direction of R-1 from R-40. When this pin is "L", Bi-directional SR shifts information to the direction of R-40 from R-1.

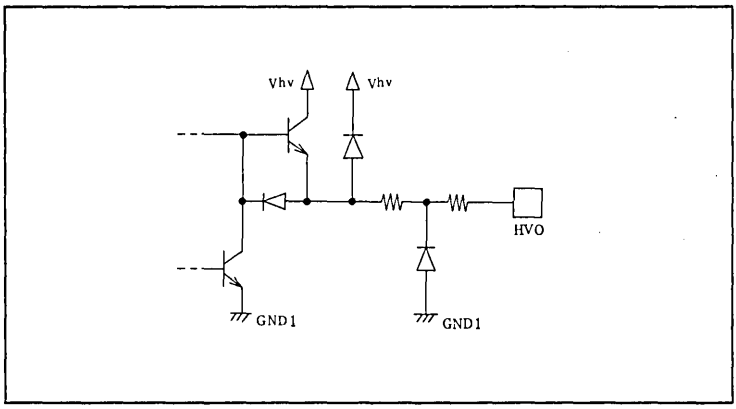
Pin No.	Symbol	Terminal Name	Description
29	DIN	Data Input	Data input pin for bidirectional SR
30 31	V_{CC}	Logic Power Supply	Power supply pin for logic (except driver). V_{CC} should be 4.5V~5.5V.
32	DOUT	Data Output	Serial output pin of bidirectional SR. When $R/\overline{L}$ is "H", D OUT outputs R-40. When $R/\overline{L}$ is "L", D OUT outputs R-1.
34	CLK	Clock Input	Clock input pin. Data of bidirectional SR is shifted from one stage to the next during the positive going clock transition.
36	CHG	Test input	Test input pin with pull-down resister. Normally "L" when CHG is "H" and $\overline{CL}$ is "H" driver outputs are fixed to "H" for test.

SCHEMATIC DIAGRAMS OF LOGIC PORTION INPUT AND OUTPUT TERMIANL CIRCUIT





SCHEMATIC DIAGRAM OF DRIVER OUTPUT TERMINAL CIRCUIT



FUNCTION TABLE

CLK	R/$\overline{L}$	Din	R-1	R-2	R-3	R-4	R-40	Dout
↑	H	H	H	$R1_n$	$R2_n$	$R3_n$	$R39_n$	$R39_n$
↑	H	L	L	RI_n	$R2_n$	$R3_n$	$R39_n$	$R39_n$
↑	L	H	$R2_n$	$R3_n$	$R4_n$	$R5_n$	H	$R2_n$
↑	L	L	$R2_n$	$R3_n$	$R4_n$	$R5_n$	L	$R2_n$

$\overline{CL}$	CHG	LS	R.X	HVO. X
L	X	X	X	L
H	H	X	X	H
H	L	H	H	H
H	L	H	L	L
H	L	L	X	NC

L: Low Level, H: High Level, X: Don't Care, NC: No Change

ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Parameter	Symbol	Condition	Limits	Unit	Note
Logic Supply Voltage	V_{cc}	Applicable to logic supply voltage terminal	− 0.3~ + 6.5	V	1
Driver Supply Voltage	V_{hv}	Applicable to driver supply voltage terminal	Vcc~ + 70	V	1
Input Voltage	V_{in}	Applicable to all input terminal	− 0.3~Vcc + 0.3	V	1
Data Output Voltage	V_{out}	Applicable to all output terminal	− 0.3~Vcc + 0.3	V	1
Driver Driving Frequency	f_{drv}	Duty cycle 50% max	0~ + 15	KHz	–
Power Dissipation	P_d	Ta ≦ 25°C	860 [Derate 6.9 mW/C above 25°C]	mW	–
Attenuation Rate	R_{j-a}	Ta > 25°C	145	°C/W	2
Operating Temperature	T_{op}	Thv ≦ 50V	− 40~ + 85	°C	–
Storage Temperature	T_{stg}	–	− 55~ + 150	°C	–

NOTES: 1) Maximum Supply Voltage for GND

2) Derate 6.9 mW/Ck above 25°C
Refer to the following formula.
$T_j = P \times R_{j-a} + Ta$ (P: Max current consumption)

• Recommended Operating Conditions

Parameter	Symbol	Condition		Min.	Max.	Unit
Logic Supply Voltage	V_{cc}	Applicable to logic supply voltage terminal		4.5	5.5	V
Driver Supply Voltage	V_{hv}	Applicable to driver supply voltage terminal		10	65	V
High Level Input Voltage	V_{ih}	Applicable to all input terminals	V_{cc} = 4.5V	3.6	–	V
			V_{cc} = 5.5V	4.4	–	V
Low Level Input Voltage	V_{il}	Applicable to all output terminals	V_{cc} = 4.5V	–	0.9	V
			V_{cc} = 5.5V	–	1.1	V
Driver High Level Output Current	I_{ohvh}	Applicable to all driver output terminal		–	– 2	mA
Driver Low Level Output Current	I_{ohvl}	Applicable to all driver output terminal		–	2	mA
CLK Frequency	$f\phi$	See timing chart		–	4	MHz
CLK Pulse width	t_{wclk}	See timing chart		75	–	ns
Data in Setup Time	t_{ds}	See timing chart		50	–	ns
Data in Hold Time	t_{dh}	See timing chart		50	–	ns
LS Pulse Width	t_{wls}	See timing chart		80	–	ns
CLK - LS Delay Time	t_{dcl}	See timing chart		50	–	ns
LS - CLK Delay Time	t_{dlc}	See timing chart		0	–	ns
LS - CHG Delay Time	t_{dlcg}	See timing chart		0	–	µs
LS - CL Delay Time	$t_{dl\overline{cl}}$	See timing chart		0	–	µs
CHG Pulse Width	t_{wchg}	See timing chart		2	–	µs
$\overline{CL}$ PUlse width	$t_{w\overline{cl}}$	See timing chart		2	–	µs
Operating Temperature	T_{op}	–		– 40	+ 85	°C

• DC Characteristics

V_{cc} = 5V ± 10%, V_{hv} = 10V~65V, Ta = −40°C to +85°C

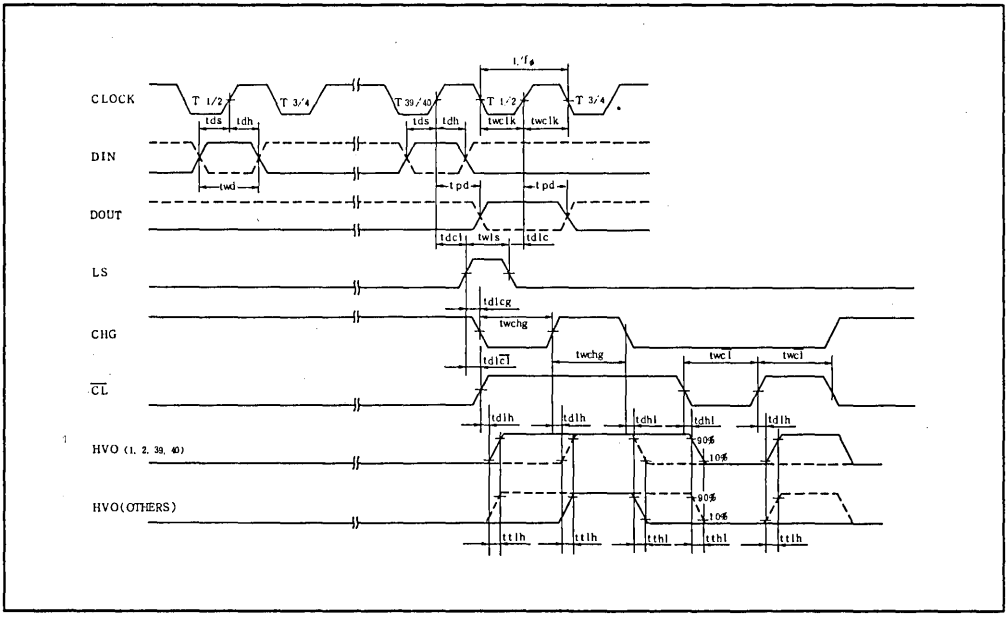
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Logic Standby Current	I_{cc1}	No Load V_{cc} = 5.5V	All Input: Low	–	4.3	6.65	mA
	I_{cc2}		All Input: High, All Driver Output: High, Ta = 25°C	–	0.5	1.0	
Driver Standby Current	I_{hV1}	No Load V_{cc} = 5.5V	All Driver Output: Low	–	–	1	µA
	I_{hV2}		All Driver Output: High, Ta = 25°C	–	2.45	3.8	mA
High Level Input Voltage	V_{ih}		V_{cc} = 4.5V	3.15	–	–	V
			V_{cc} = 5.5V	3.85	–	–	V
Low Level Input Voltage	V_{il}		V_{cc} = 4.5V	–	–	1.35	V
			V_{cc} = 5.5V	–	–	1.65	V
Input Leakage Current	I_{in}	Ta = 25°C		–	–	±1	µA
Input Capacitance	C_{in}	Ta = 25°C		–	15	–	pF
High Level Data Output Voltage	V_{odh1}	Io = −20µA	V_{cc} = 4.5V	4.2	–	–	V
			V_{cc} = 5.5V	5.2	–	–	V
Low Level Data Output Voltage	V_{odl1}	Io = 20µA	V_{cc} = 4.5V	–	–	0.2	V
			V_{cc} = 5.5V	–	–	0.2	V
High Level Data Output Voltage	V_{odh2}	Io = −0.1mA	V_{cc} = 4.5V	3.5	–	–	V
			V_{cc} = 5.5V	4.5	–	–	V
Low Level Data Output Voltage	V_{odl2}	Io = 0.1mA	V_{cc} = 4.5V	–	–	1.1	V
			V_{cc} = 5.5V	–	–	1.1	V
Driver High Level Output Voltage	V_{ohvh}	I_{ohv} = −2mA		Vhv − 3	–	–	V
Driver Low Level Output Voltage	V_{ohvl}	I_{ohv} = 2mA		–	–	3.0	V

• AC Characteristics

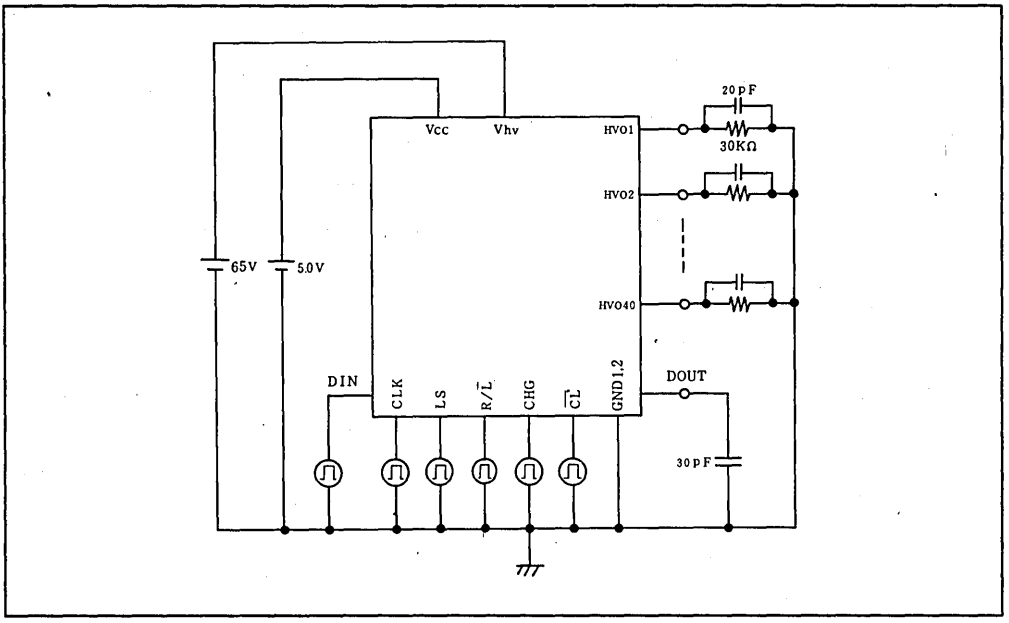
Vcc = 5V, Vhv = 65V, Ta = 25°C

Item	Symbol	Remarks	Min.	Typ.	Max.	Unit
CLK – Dout Delay Time	t_{pd}	See timing chart and test circuit	–	100	150	nS
Delay Time Low – High	t_{dlh}	See timing chart and test circuit	–	0.3	1	µS
Transit Time Low – High	t_{tlh}	See timing chart and test circuit	–	2	5	µS
Delay Time High – Low	t_{dhl}	See timing chart and test circuit	–	0.3	1	µS
Transit Time High – Low	t_{thl}	See timing chart and test circuit	–	2	5	µS

• Timing Chart



TEST CIRCUIT



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OKI semiconductor

MSC7751 (Underdevelopment)

40-Bit ANODE DRIVER

GENERAL DESCRIPTION

The MSC7751 is a monolithic IC using the high withstand voltage driver process for hybridizing CMOS and DMOS transistors on one chip.
The logic portion such as the input stage, shift register and latch is formed by CMOS, and the output driver requiring a high withstand voltage is formed by DMOS transistors.

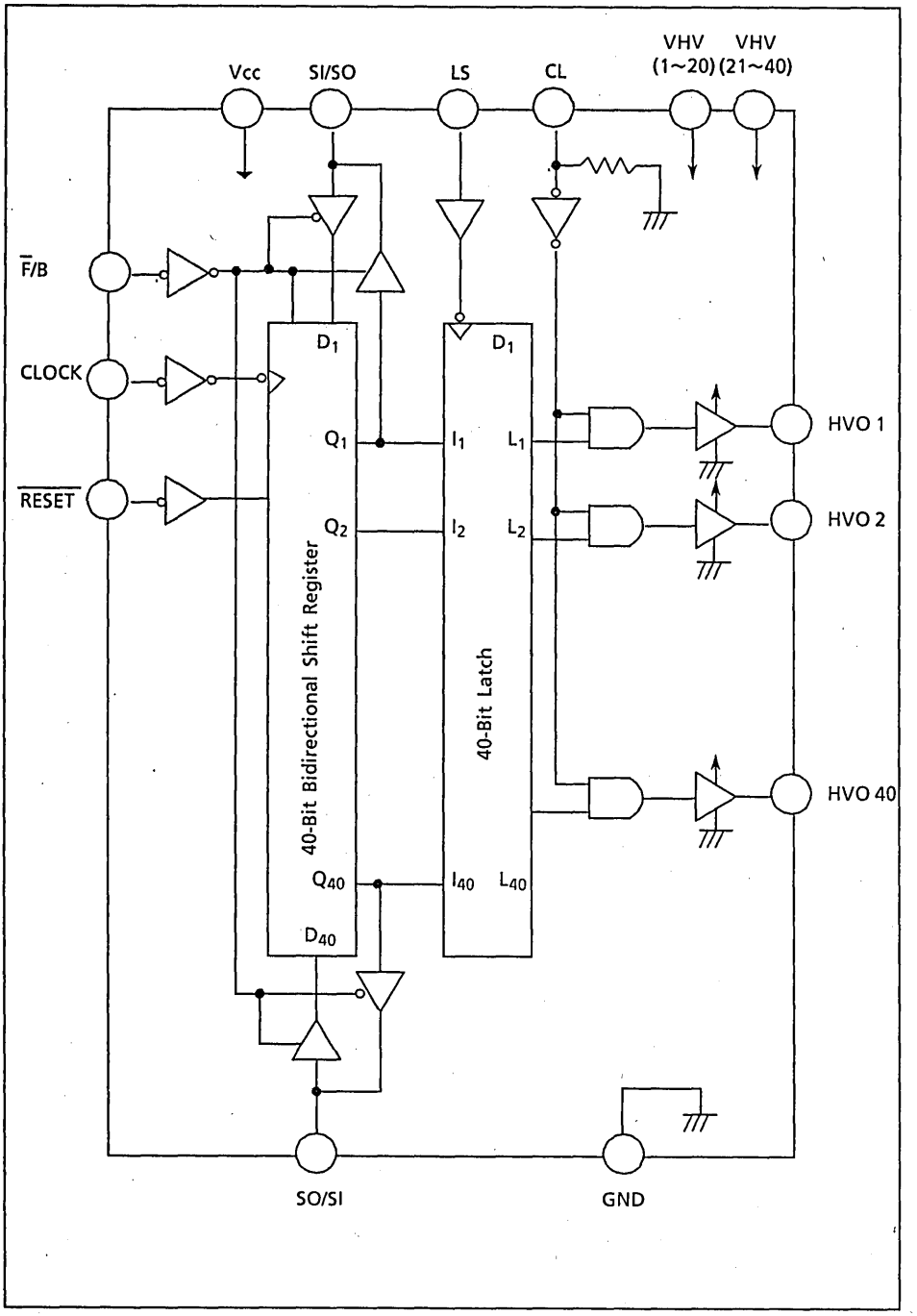
Since the pin assigment allows single side pattern formation on the printed circuit board, the display unit can be reduced.

The bidirectional shift register facilitates the pattern design when the devices are arranged symmetrically with the display at the center axis.

FEATURES

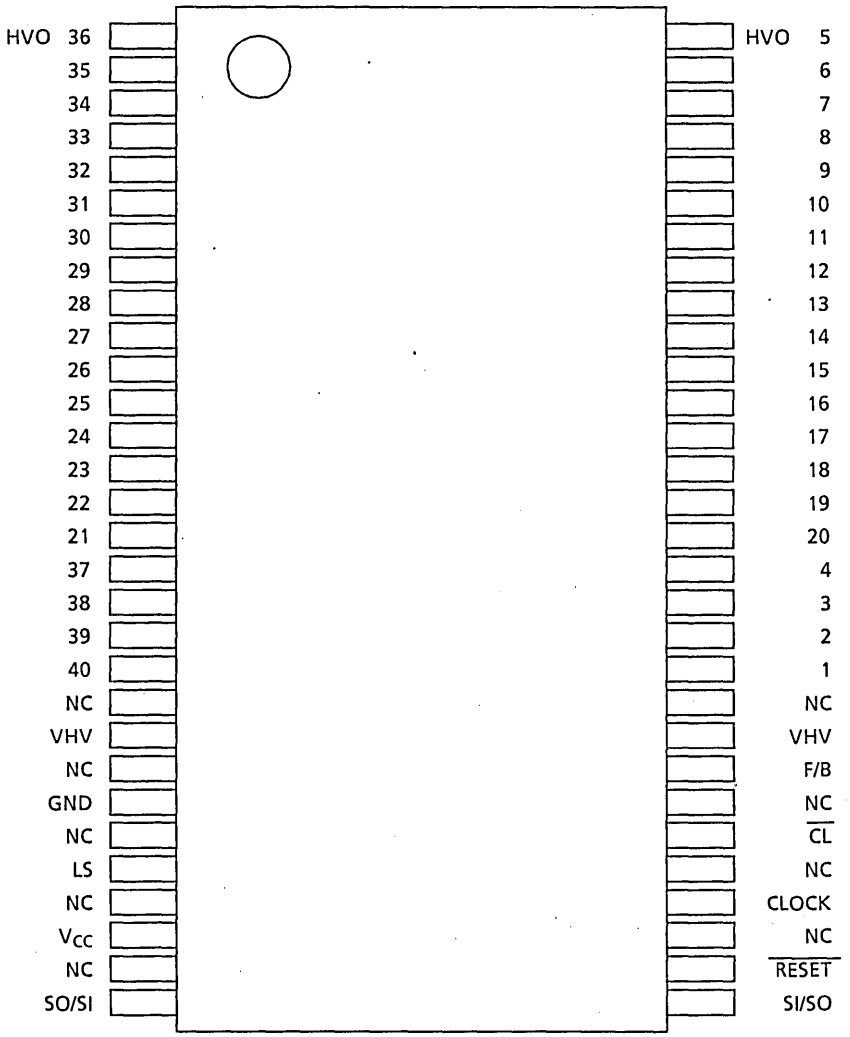
- Logic supply voltage (V_{CC}) : +5 V
- VF driver supply voltage (V_{hv}) : −200 V
- Driver output current
  (I_{ohvh}) : −2 mA (All driver output high)
  (I_{ohvl}) : +2 mA
- Clock frequency : 5.5 MHz
- Built-in 40-bit latch
- Built-in 40-bit bidirectional shift register
- 60 Pin FLAT Package

BLOCK DIAGRAM



PIN CONFDIGURATION

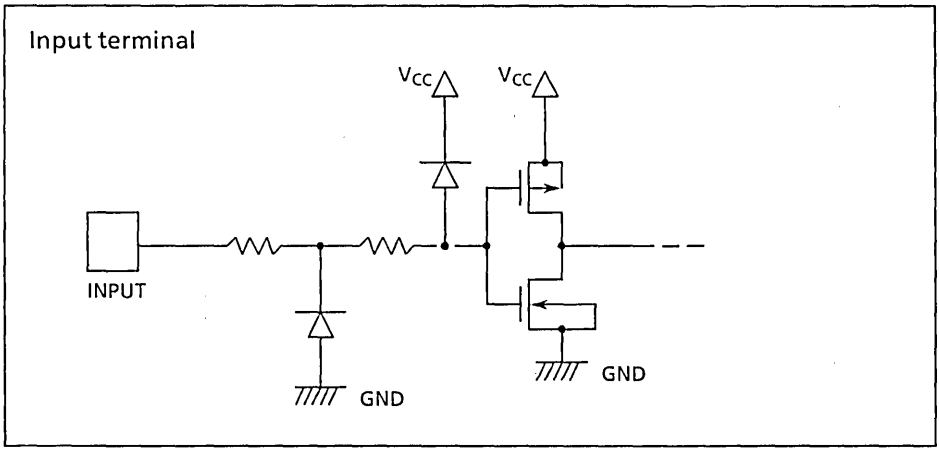
(Top View) 60 Lead Plastic Flat Package

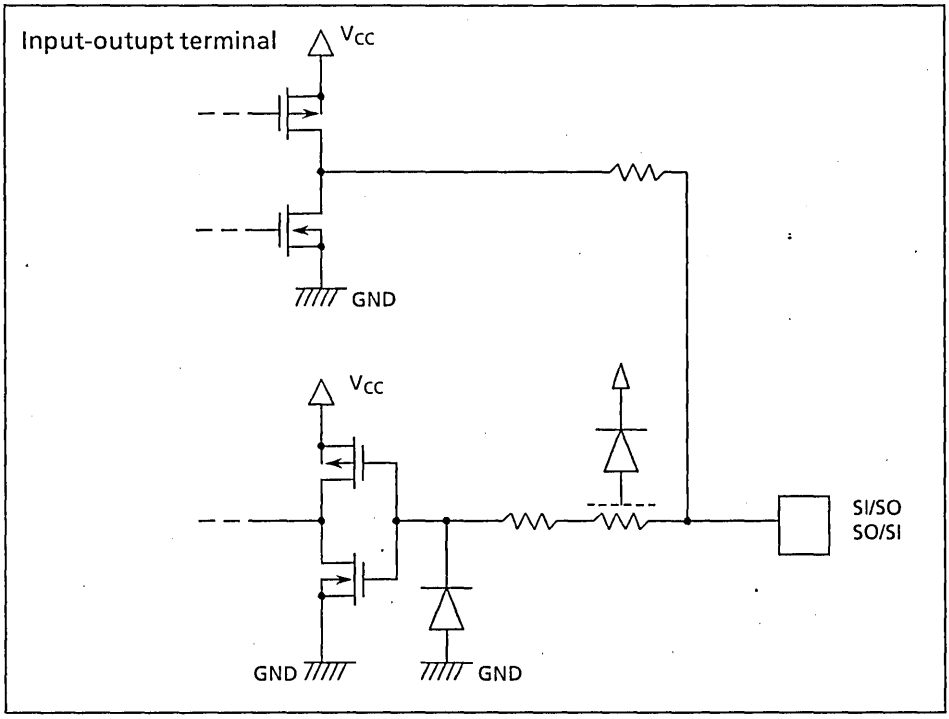


PIN DESCRIPTION

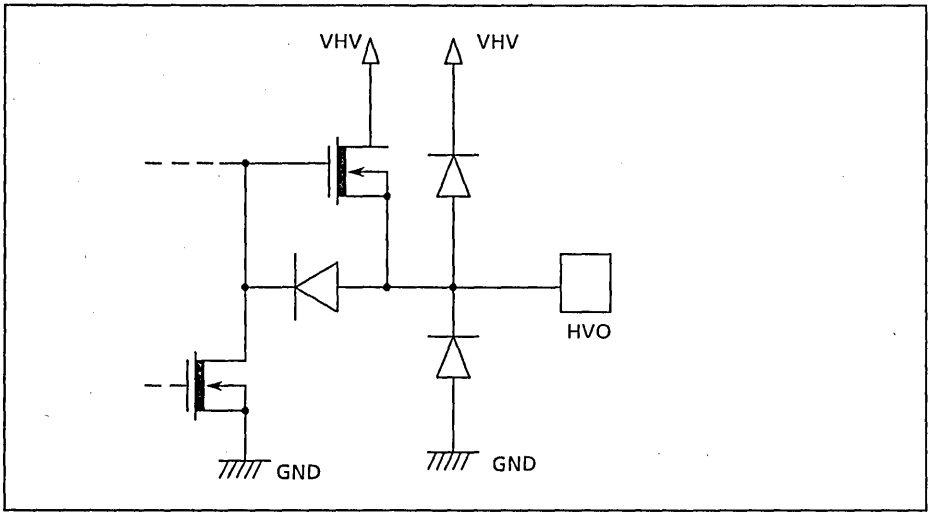
Pin No.	Symbol	Name	Description
1 ⋮ 20, 41 ⋮ 60	HVO 1 ⋮ HVO 40	Driver output	1. Each terminal is a high withstand voltage driver output terminal to drive the anode of the VF display tube, which corresponds to easch bit of the shift register. 2. Each terminal can be directly connected to the anode terminal of the VF display tube.
22, 39	V_{HV}	Driver supply voltage	1. This is a power terminal of the high withstand voltage driver to drive the VF display tube.
28	V_{CC}	Logic supply voltage	2. This is a power terminal of the logic portion.
36	$\overline{CL}$	Clear input	1. This is an input terminal containing a pull-down resistor. 2. The terminal is generally kept High. The driver output, High of Low, is driven by the output of the corresponding latch circuit. 3. When the terminal is Low, the driver outputs are fixed to "Low" regardless of the output of the latch circuit.
26	LS	Latch strobe input	1. When the terminal is High, the latch circuit is slewed, and the output of the shift register is read into the latch circuit. 2. When the terminal is Low, the latch circuit holds the output of the shift register immediately before the terminal is turned Low.
34	CLOCK	Clock input	1. This is a clock terminal of the shift register. The data of the shift register is shifted at the falling edge of a clock pulse.
32	$\overline{RESET}$	Reset input	1. When the terminal is Low, all the data of the shift register is Low. Generally and when not in use, connect the terminal to the V_{CC} terminal.
38	$\overline{F}/B$	Shift direction control input	1. When the terminal is Low, data is shifted from 1 to 40, and Pin 31 is a serial in terminal and Pin 30 is a serial out terminal. 2. When the terminal is High, data is shifted from 40 to 1, and Pin 30 is a serial in terminal and Pin 31 is a serial out terminal.
31	SI/SO	Serial input/serial output	1. When the $\overline{F}/B$ terminal is Low, this terminal is a serial data input terminal. 2. When the $\overline{F}/B$ terminal is High, this terminal is a serial data output terminal.
30	SO/SI	Serial input/serial output	1. When the $\overline{F}/B$ terminal is Low, this terminal is a serial data output terminal. 2. When the $\overline{F}/B$ terminal is High, this terminal is a serial data input terminal.
24	GND	GND	1. This is a grounding (GND) terminal.

SCHEMATIC DIAGRAMS OF LOGIC PORTION INPUT AND OUTPUT TERMINAL CIRCUITS





SCHEMATIC DIAGRAM OF DRIVER OUTPUT TERMINAL CIRCUIT



FUNCTION TABLE

$\overline{\text{RESET}}$	CLK	$\overline{\text{F}}$/B	SI/SO	Q1	Q2	Q3	----	Q39	Q40	SO/SI
L	X	L	X	L	L	L		L	L	L
L	X	H	L	L	L	L		L	L	X
H	↓	L	H	H	Q_{1n}	Q_{2n}		Q_{38n}	Q_{39n}	Q_{39n}
H	↓	L	L	L	Q_{1n}	Q_{2n}		Q_{38n}	Q_{39n}	Q_{39n}
H	↓	H	Q_{2n}	Q_{2n}	Q_{3n}	Q_{4n}		Q_{40n}	H	H
H	↓	H	Q_{2n}	Q_{2n}	Q_{3n}	Q_{4n}		Q_{40n}	L	L

$\overline{\text{CL}}$	LS	Qn	HVOn
L	X	X	L
H	H	H	H
H	H	L	L
H	L	X	NC

L : Low Level, H : High Level
X : Don't Care, NC : No Change

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratingds

Parameter	Symbol	Conditios	Limits	Unit	Note
Logic supply voltage	V_{CC}	Applicable to logic power terminal	− 0.3~6.5	V	1
Driver supply voltage	V_{HV}	Applicable to driver power terminal	V_{CC}~230	V	1
Input voltage	V_{IN}	Applicable to all input teminals	− 0.3~V_{CC} + 0.3	V	1
Data ouptput voltage	Vod	Applicable to data output terminal	− 0.3~V_{CC} + 0.3	V	1
Driver output voltage	Vohv	Applicable to all driver terminals	− 0.3~V_{CC} + 0.3	V	1
Power Dissipation	Pd	Ta≦25°C	860	mW	
Attenuation Rate	Rj-a	Ta>25°C	145	°C/W	2
Operating temperature	Top	V_{HV}≦130V	− 40~ + 85	°C	
Storage temperature	Tstg	———	− 55~ + 150	°C	

Notes : 1. The maximum voltage which can be applied to the GND terminal.

2. Thermal resistance of the package (between junction and atmosphere).
The junction temperature (Tj) expressed by the equation indicated below should not exceed 150°C.
$Tj = P \times Rj - a + Ta$ (P : Maximum power consumption of IC)

• Recommended Operating Conditions

Parameter	Symbol	Conditions		MIN	MAX	Unit
Logic supply voltage	V_{CC}	Applicable to logic power terminal		4.5	5.5	V
Driver supply voltage	V_{HV}	Applicable to driver power terminal		10	200	V
High level input voltage	V_{IH}	Applicable to all input terminals	V_{CC} = 4.5V	3.6	—	V
			V_{CC} = 5.5V	4.4	—	
Low level input voltage	V_{IL}	Applicable to all input terminals	V_{CC} = 4.5V	—	0.9	V
			V_{CC} = 5.5V	—	1.1	
Driver high level output current	I_{OHVH}	Applicable to all driver output terminals		—	− 2	mA
Driver low level output current	I_{OHVL}	Applicable to all driver output terminals		—	2	mA
Clock frequency	fØ	See Timing chart		—	5.5	MHz
Clock pulse width	t_{wclkl}	See Timing chart		70	—	nS
Data setup time	t_{ds}	See Timing chart		20	—	nS
Data hold time	t_{dh}	See Timing chart		45	—	nS
LS pulse width	t_{wls}	See Timing chart		80	—	nS
CLK-LS delay time	t_{dcl}	See Timing chart		45	—	nS
LS-CL delay time	t_{dlcl}	See Timing chart		0	—	nS
CL pulse width	t_{wcl}	See Timing chart		2	—	µS
Operating temperature range	Top	See Timing chart		− 40	+ 85	°C

• DC Characteristics

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Logic supply current	I_{CC1}	No load V_{CC} = 5.5V	All inputs : Low	—	—	50	μA
	I_{CC2}		All inputs : High All driver outputs : High	—	—	200	
Driver supply current	I_{HV1}	No load V_{CC} = 5.5V	All driver outputs : Low	—	—	50	μA
	I_{HV2}		All driver outputs : High	—	2.5	4.0	mA
High level input voltage	V_{IH}	V_{CC} = 4.5V	Applicable to all input terminals	3.15	—	—	V
		V_{CC} = 5.5V		3.85	—	—	V
Low level input voltage	V_{IL}	V_{CC} = 4.5V	Applicable to all input terminals	—	—	1.35	V
		V_{CC} = 5.5V		—	—	1.65	V
Input leak current	I_{ILEEK}	Ta = 25°C	Input terminals except $\overline{CL}$ terminal	—	—	± 1	μA
High level input current	I_{IH}	V_{CC} = 4.5V	Applicable to $\overline{CL}$ terminal	20	50	100	μA
		V_{CC} = 5.5		25	60	200	
Input capacity	C_{IN}	Ta = 25°C		—	15	—	pF
High level data output voltage	V_{ODH}	Io = −0.1mA	V_{CC} = 4.5V	3.5	—	—	V
			V_{CC} = 5.5V	4.5	—	—	
Low level data output voltage	V_{ODL}	Io = ÷0.1mA	V_{CC} = 4.5V	—	—	0.9	V
			V_{CC} = 5.5V	—	—	1.1	
High level driver output voltae	V_{OHVH}	I_{OHV} = −2mA		195	—	—	V
Low level driver output voltae	V_{OHVL}	I_{OHV} = 2mA		—	—	5	V

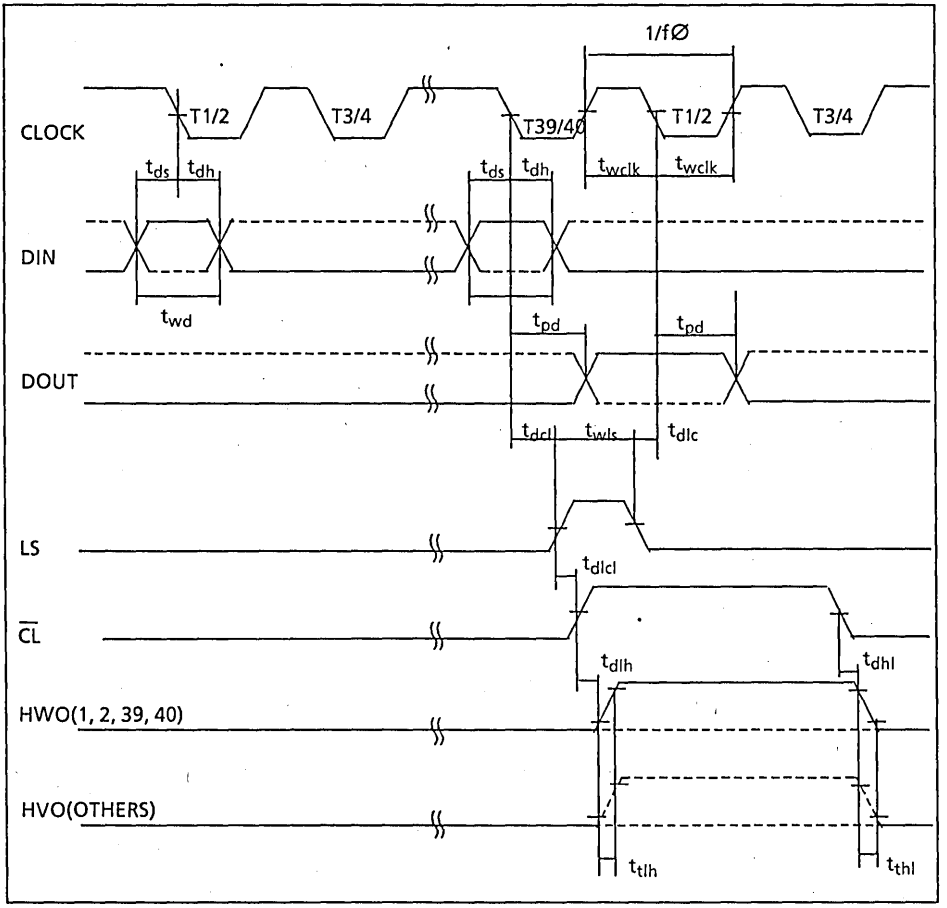
• AC Characteristics

V_{CC} = 5V, V_{HV} = 200V, Ta = 25°C

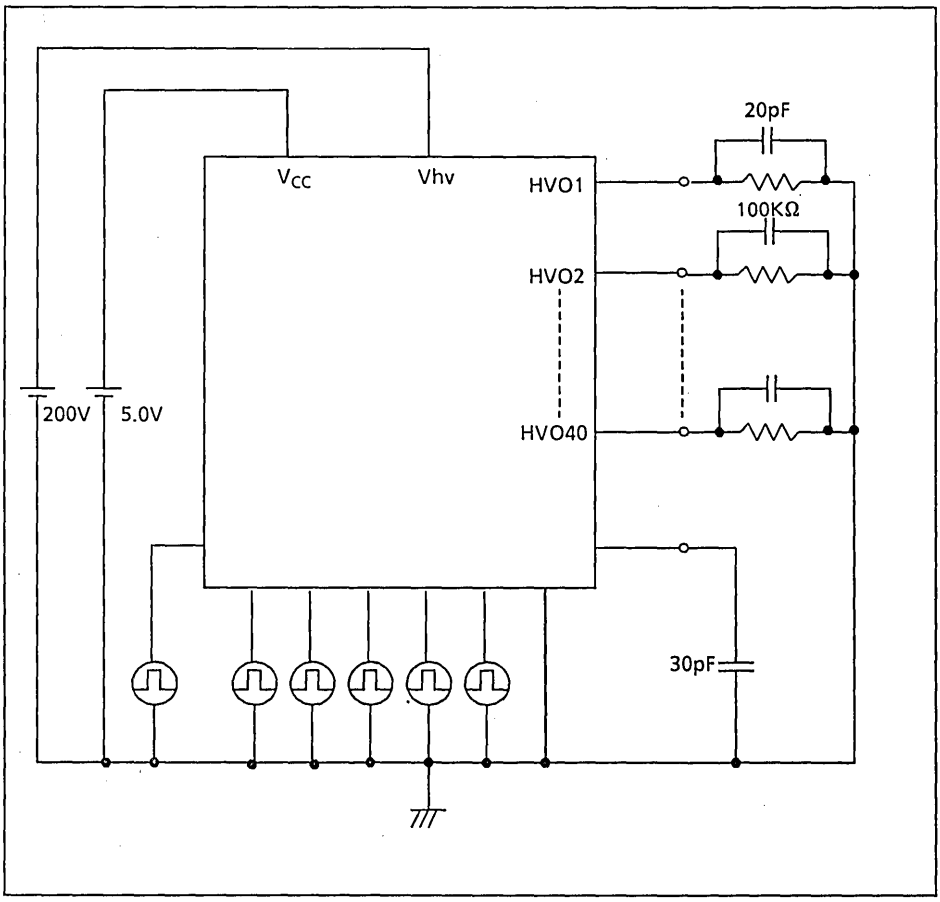
Parameter	Symbol	Conditios	MIN	TYP	MAX	Unit	Note
CLK-DOUT delay time	t_{pd}	See Timing Chart and Test Circuit	—	100	150	nS	4
Delay time : L→H	t_{dlh}	See Timing Chart and Test Circuit	—	0.3	1	µs	5, 6
Transit time : L→H	t_{tlh}	See Timing Chart and Test Circuit	—	2	5	µs	5
Delay time : H→L	t_{dhl}	See Timing Chart and Test Circuit	—	0.3	1	µs	5, 6
Transit time : H→L	t_{thl}	See Timing Chart and Test Circuit	—	2	5	µs	5

Note 4 : Applicable to data output terminal.
Note 5 : Applicable to driver output terminal.
Note 6 : t_{dlh} and T_{dhl} are delay times from $\overline{CL}$ signal.

• Timing Chart



TEST CIRCUIT



OKI semiconductor

MSC7701 (Underdevelopment)

40-BIT GRID DRIVER

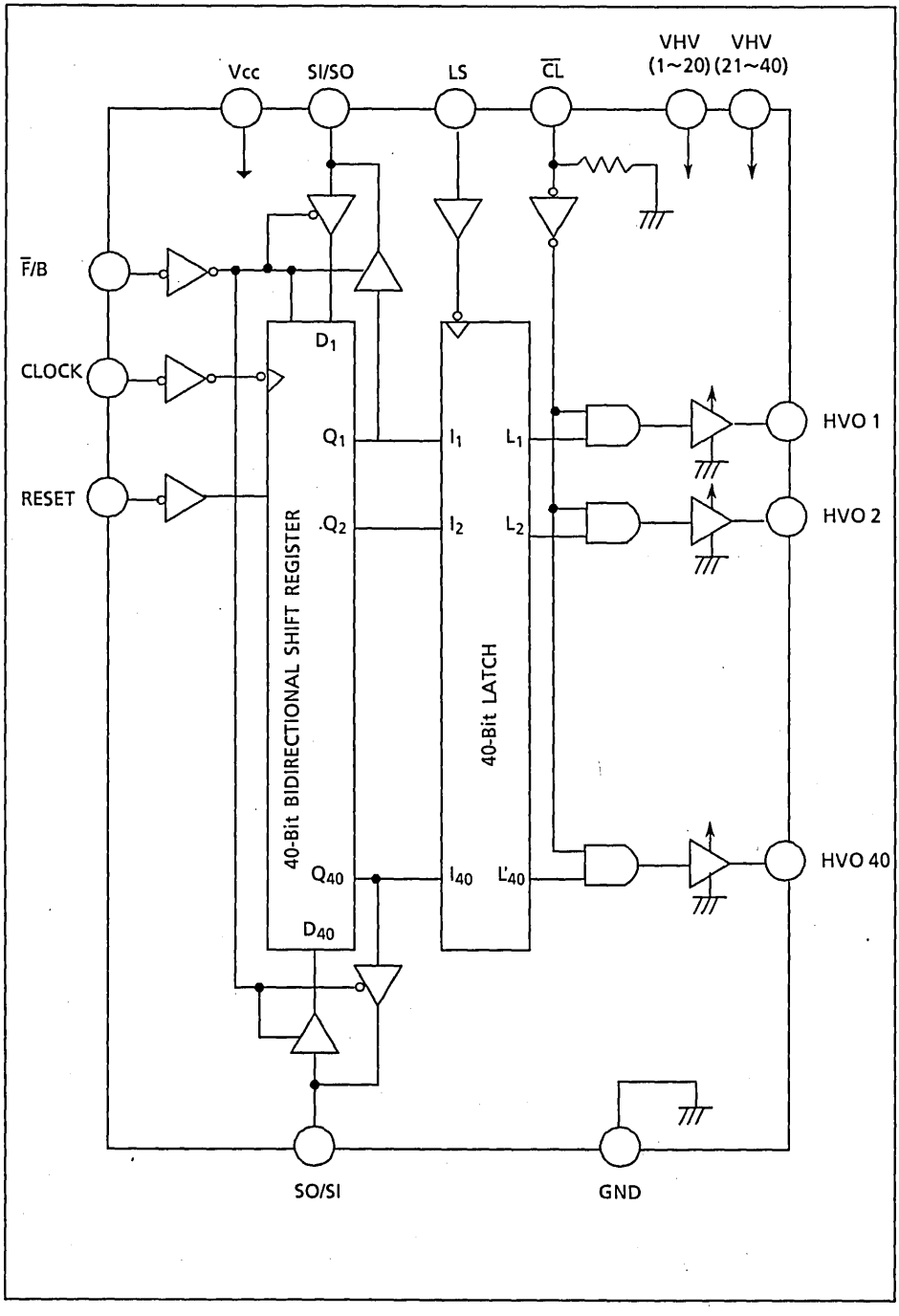
GENERAL DESCRIPTION

The MSC7701 is a monolithic IC using the high withstand voltage driver process for hybridizing CMOS and DMOS transistors on one chip.
The logic portion such as the input stage, shift register and latch is formed by CMOS, and the output driver requiring a high withstand voltage is formed by DMOS transistors.
Since the pin assigment allows single side pattern formation on the printed circuit board, the display unit size can be reduced.
The bidirectional shift register facilitates the pattern design when the devices are arranged symmetrically with the display at the center axis.

FEATURES

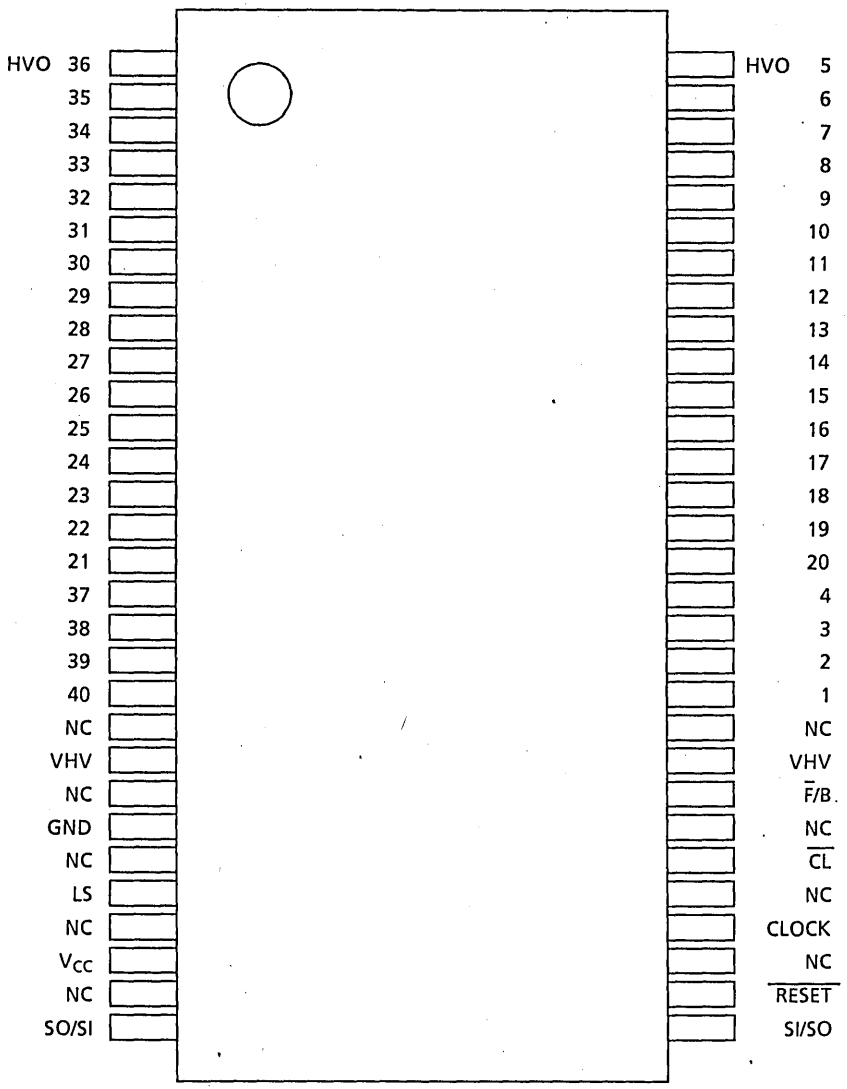
- Logic supply voltage (V_{CC}) : + 5 V
- VF driver supply voltage (V_{hv}) : + 130 V
- VF driver output current
  (I_{ohvh}) : – 40 mA (1 driver output high)
  (I_{ohvl}) : + 2 mA
- Clock frequency : 5.5 MHz
- Built-in 40-Bit latch
- Built-in 40-Bit bidirectional shift register
- 60 Pin FLAT Package

BLOCK DIAGRAM



PIN CONFDIGURATION

(Top View) 60 Lead Plastic Flat Package

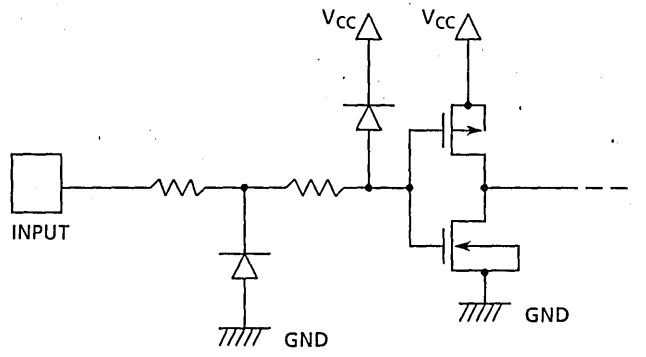


PIN DESCRIPTION

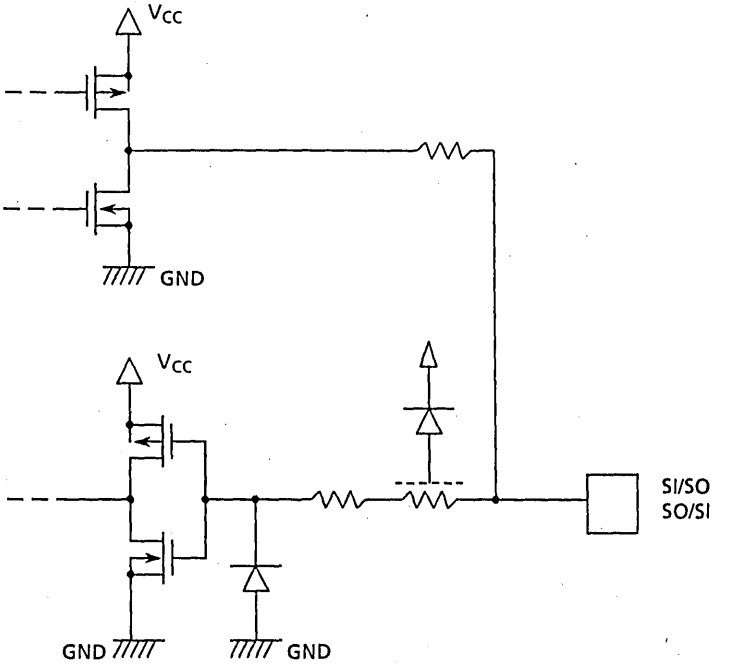
Pin No.	Symbol	Name	Description
1 ⋮ 20 41 ⋮ 60	HVO 1 ⋮ HVO 40	Driver output	1. Each terminal is a high withstand voltage driver output terminal to drive the grid of the VF display tube, which corresponds to each bit of the shift register. 2. Each terminal can be directly connected to the grid terminal of the VF display tube.
22 39	V_{HV}	Driver supply voltage	1. This is a power terminal of the high withstand voltage driver to drive the VF display tuve.
28	V_{CC}	Logic supply voltage	2. This is a power terminal of the logic portion.
36	$\overline{CL}$	Clear input	1. This is an input terminal containing a pull-down resistor. 2. The terminal is generally kept High. The driver output, High or Low, is driven by the output of the corresponding latch circuit. 3. When the terminal is Low, the driver outputs are fixed to "Low" regardless of the output of the latch circuit.
26	LS	Latch strobe input	1. When the terminal is High, the latch circuit is slewed, and the output of the shift register is read into the latch circuit. 2. When the terminal is Low, the latch circuit holds the output of the shift register immediately before the terminal is turned Low.
34	CLOCK	Clock input	1. This is a clock terminal of the shift register. The data of the shift register is shifted at the falling edge of a clock pulse.
32	$\overline{RESET}$	Reset input	1. When the terminal is Low, all the data of the shift register is Low. Generally and when not in use, connect the terminal to the V_{CC} terminal.
38	$\overline{F}$/B	Shift direction control input	1. When the terminal is Low, data is shifted from 1 to 40, and Pin 31 is a serial in terminal and Pin 30 is a serial out terminal. 2. When the terminal is High, data is shifted from 40 to 1, and Pin 30 is a serial in terminal and Pin 31 is a serial out terminal.
31	SI/SO	Serial input/serial output	1. When the $\overline{F}$/B terminal is Low, this terminal is a serial data input terminal. 2. When the $\overline{F}$/B terminal is High, this terminal is a serial data output terminal.
30	SO/SI	Serial output/serial input	1. When the $\overline{F}$/B terminal is Low, this terminal is a serial data output terminal. 2. When the $\overline{F}$/B terminal is High, this terminal is a serial data input terminal.
24	GND	GND	1. This is a grounding (GND) terminal.

SCHEMATIC DIAGRAMS OF LOGIC PORTION INPUT AND OUTPUT TERMINAL CIRCUITS

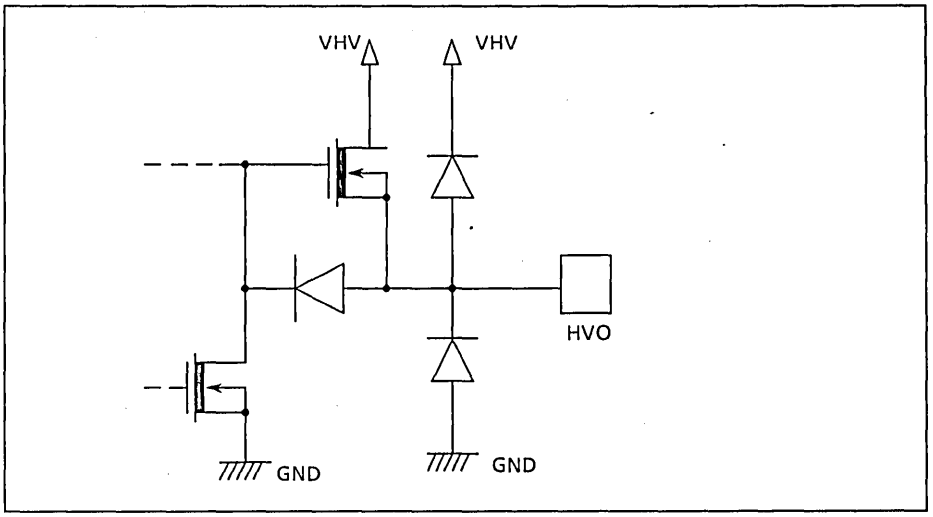
Input terminal



Input -output terminal



SCHEMATIC DIAGRAM OF DRIVER OUTPUT TERMINAL CIRCUIT



FUNCTION TABLE

$\overline{\text{RESET}}$	CLK	$\overline{\text{F/B}}$	SI/SO	Q1	Q2	Q3	----	Q39	Q40	SO/SI
L	X	L	X	L	L	L		L	L	L
L	X	H	L	L	L	L		L	L	X
H	↓	L	H	H	Q_{1n}	Q_{2n}		Q_{38n}	Q_{39n}	Q_{39n}
H	↓	L	L	L	Q_{1n}	Q_{2n}		Q_{38n}	Q_{39n}	Q_{39n}
H	↓	H	Q_{2n}	Q_{2n}	Q_{3n}	Q_{4n}		Q_{40n}	H	H
H	↓	H	Q_{2n}	Q_{2n}	Q_{3n}	Q_{4n}		Q_{40n}	L	L

$\overline{\text{CL}}$	LS	Qn	HVOn
L	X	X	L
H	H	H	H
H	H	L	L
H	L	X	NC

L : Low Level, H : High Level
X : Don't Care, NC : No Change

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditios	Limits	Unit	Note
Logic supply voltage	V_{CC}	Applicable to logic power terminal	− 0.3~6.5	V	1
Driver supply voltage	V_{HV}	Applicable to driver power terminal	V_{CC}~150	V	1
Input voltage	V_{IN}	Applicable to all input teminals	− 0.3~V_{CC} + 0.3	V	1
Data ouptput voltage	Vod	Applicable to data output terminal	− 0.3~V_{CC} + 0.3	V	1
Driver output voltage	Vohv	Applicable to all driver terminals	− 0.3~V_{CC} + 0.3	V	1
Power Dissipation	Pd	Ta≦25°C	860	mW	
Attenuation Rate	Rj-a	Ta>25°C	145	°C/W	2
Operating temperature	Top	VHV≦130V	− 40~ + 85	°C	
Storage temperature	Tstg	———	− 55~ + 150	°C	

Notes : 1. The maximum voltage which can be applied to the GND terminal.

2. Thermal resistance of the package (between junction and atmosphere).
The junction temperature (Tj) expressed by the equation indicated below should not exceed 150°C.
$Tj = P \times Rj - a + Ta$ (P : Maximum power consumption of IC)

• Recommended Operating Conditions

Parameter	Symbol	Conditions		MIN	MAX	Unit
Logic supply voltage	V_{CC}	Applicable to logic power terminal		4.5	5.5	V
Driver supply voltage	V_{HV}	Applicable to logic power terminal		10	130	V
High level input voltage	V_{IH}	Applicable to all input terminals	V_{CC} = 4.5V	3.6	—	V
			V_{CC} = 5.5V	4.4	—	
Low level input voltage	V_{IL}	Applicable to all input terminals	V_{CC} = 4.5V	—	0.9	V
			V_{CC} = 5.5V	—	1.1	
Driver high level output current	I_{OHVH}	1 driver output : High Other driver outputs : Low		—	− 40	mA
Driver low level output current	I_{OHVL}	Applicable to all driver output terminals		—	2	mA
Clock frequency	fØ	See timing chart.		—	5.5	MHz
Clock pulse width	t_{wclkl}	See timing chart.		70	—	nS
Data setup time	t_{ds}	See timing chart.		20	—	nS
Data hold time	t_{dh}	See timing chart.		45	—	nS
LS pulse width	t_{wls}	See timing chart.		80	—	nS
CLK-LS delay time	t_{dcl}	See timing chart.		45	—	nS
LS-CL delay time	t_{dlcl}	See timing chart.		0	—	nS
CL pulse width	t_{wcl}	See timing chart.		2	—	µS
Operating temperature	Top	See timing chart.		− 40	+ 85	°C

• DC Characteristics

V_{CC} = 5V ± 10%, V_{HV} = 110V, Ta = −40°C~ +85°C

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Logic supply current	I_{CC1}	No load V_{CC} = 5.5V	All inputs : Low	—	—	50	µA
	I_{CC2}		All inputs : High 1 driver output : High Other driver outputs : Low	—	—	200	
Driver supply current	I_{HV1}	No load V_{CC} = 5.5V	All driver outputs : Low	—	—	50	µA
	I_{HV2}		1 driver output : High	—	1.1	1.5	mA
High level input voltage	V_{IH}	V_{CC} = 4.5V	Applicable to all input terminals	3.15	—	—	V
		V_{CC} = 5.5V		3.85	—	—	V
Low level input voltage	V_{IL}	V_{CC} = 4.5V	Applicable to all input terminals	—	—	1.35	V
		V_{CC} = 5.5V		—	—	1.65	V
Input leak current	I_{ILEEK}	Ta = 25°C	Input terminals except $\overline{CL}$ terminal	—	—	± 1	µA
High level input current	I_{IH}	V_{CC} = 4.5V	Applicable to $\overline{CL}$ terminal	20	50	100	µA
		V_{CC} = 5.5V		25	60	200	
Input capacitance	C_{IN}	Ta = 25°C		—	15	—	pF
High level data output voltage	V_{ODH}	Io = −0.1mA	V_{CC} = 4.5V	3.5	—	—	V
			V_{CC} = 5.5V	4.5	—	—	
Low level data output voltage	V_{ODL}	Io = −0.1mA	V_{CC} = 4.5V	—	—	0.9	V
			V_{CC} = 5.5V	—	—	1.1	
High level driver output voltae	V_{OHVH}	I_{OHV} = −40mA		106	—	—	V
Low level driver output voltae	V_{OHVL}	I_{OHV} = 2mA		—	—	4	V

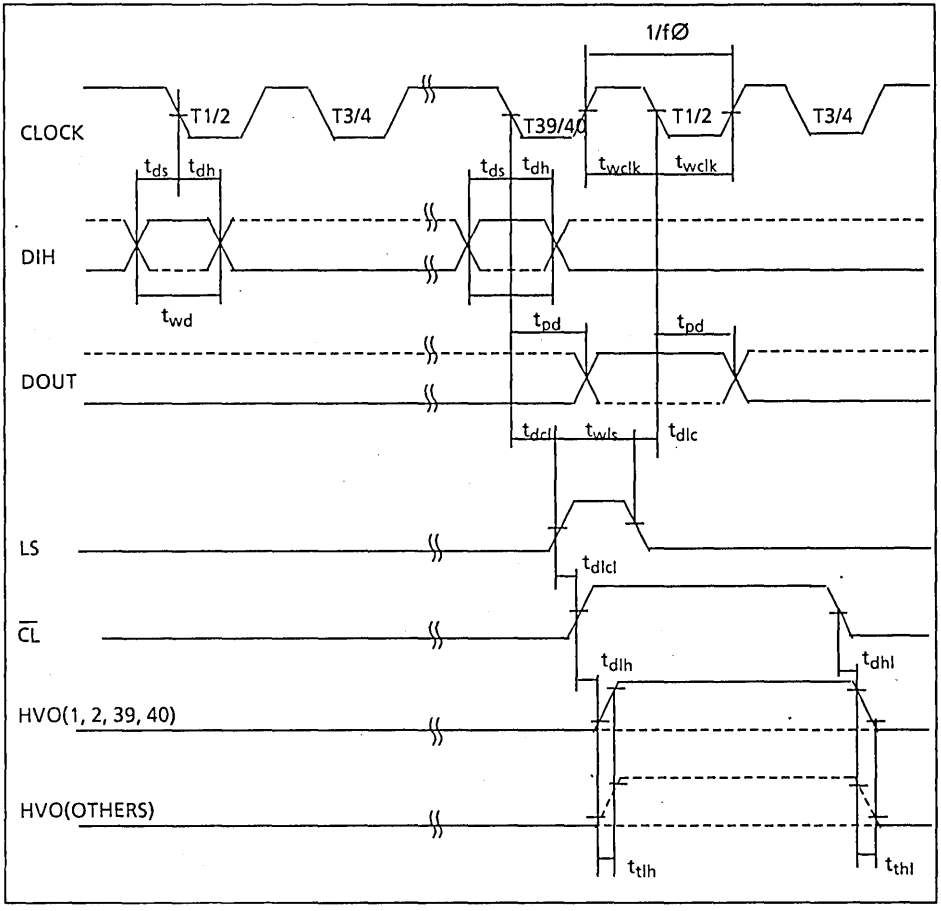
o AC Characteristics

V_{CC} = 5V, V_{HV} = 200V, Ta = 25°C

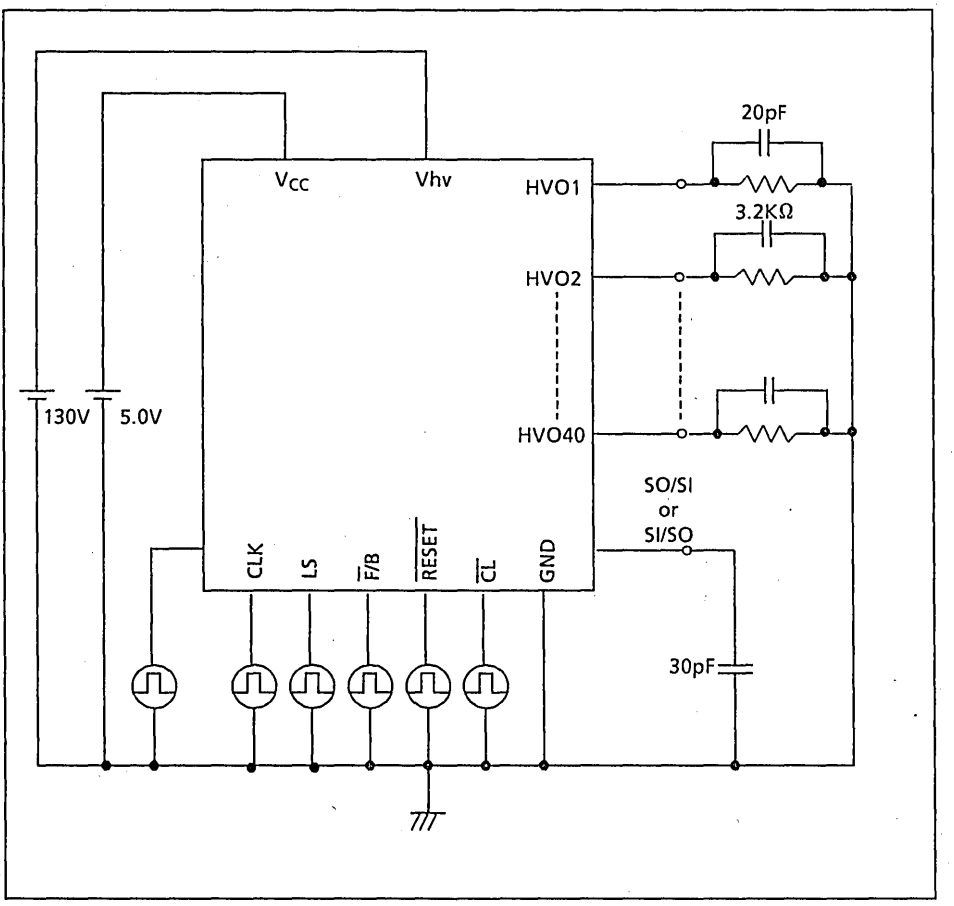
Parameter	Symbol	Conditios	MIN	TYP	MAX	Unit	Note
CLK-DOUT delay time	t_{pd}	See timing chart and test chart.	—	100	150	nS	4
Delay time : L→H	t_{dlh}	See timing chart and test chart.	—	0.3	1	µs	5, 6
Transit time : L→H	t_{tlh}	See timing chart and test chart.	—	2	5	µs	5
Delay time : H→L	t_{dhl}	See timing chart and test chart.	—	0.3	1	µs	5, 6
Transit time : H→L	t_{thl}	See Timing chart and test chart.	—	3	6	µs	5

Note 4 : Applicable to data output terminal.
Note 5 : Applicable to driver output terminal.
Note 6 : t_{dlh} and T_{dhl} are delay times from $\overline{CL}$ signal.

o Timing Chart



TEST CIRCUIT



OKI semiconductor

MSC1150 / MSC1171 / MSC1173 (Underdevelopment)

10-bit/20-bit/32-bit ANODE/GRID DRIVER

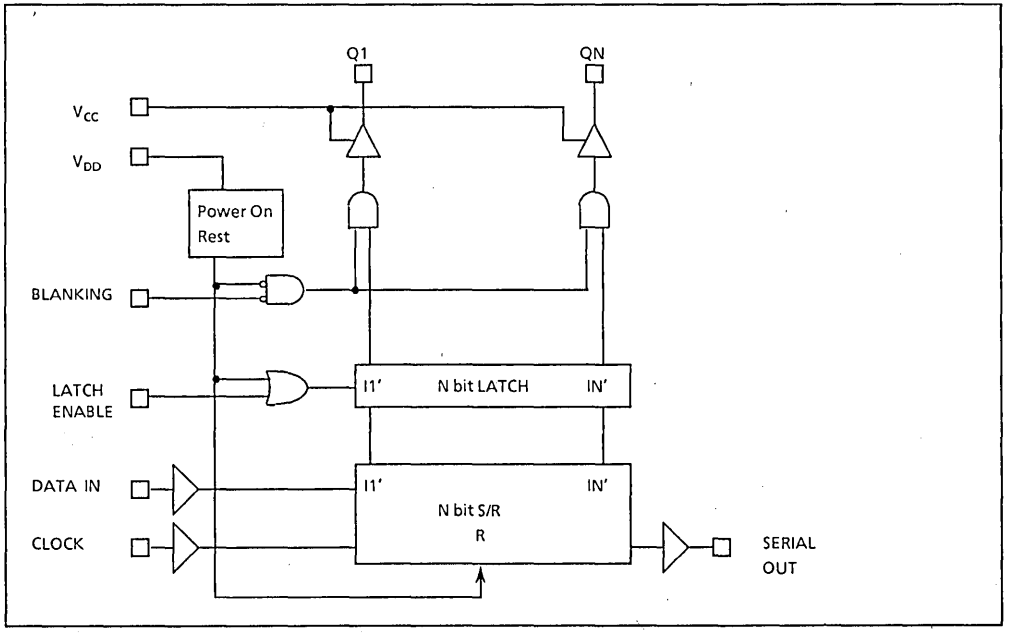
GENERAL DESCRIPTION

The MSC1150/MSC1171/MSC1173 are vacuum fluorescent display tube. ICs which consist of shift registers, latches and VF driver outputs.

FEATURES

- 60-V output Voltage Swing Capability
- 25-mA output Source Current Capability
- Latches on all Driver outputs
- POWER-ON-RESET circuit built in

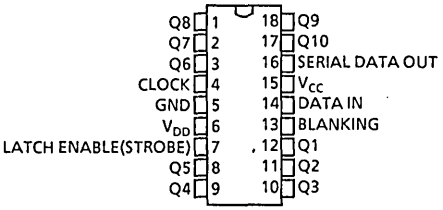
BLOCK DIAGRAM



PIN CONFIGURATION

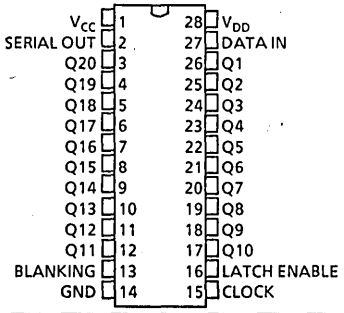
MSC1150RS

DUAL-IN-LINE PACKAGE
(TOP VIEW)



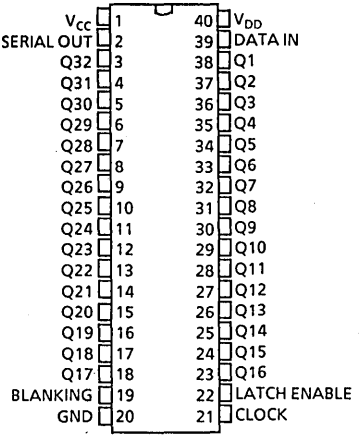
MSC1171RS

DUAL-IN-LINE PACKAGE
(TOP VIEW)



MSC1173RS

DUAL-IN-LINE PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Parameter		Symbol	Limits	Unit
Logic Supply Voltage		Vdd	− 0.3 ~ 6.5	V
Driver Supply Voltage		Vcc	− 0.3 ~ 65	V
Input Voltage		Vin	− 0.3 ~ Vdd + 0.3	V
Maximum Output Current		Io	30	mA
Package Power Dissipation	MSC1173RS	Pd	1300 (Ta = 25°C)	mW
	MSC1171RS		1200 (Ta = 25°C)	mW
	MSC1150RS		1000 (Ta = 25°C)	mW
Operating Temperature		Top	− 40 ~ 85	°C
Storage Temperature		Tstg	− 55 ~ 150	°C

• DC Characteristics

Ta = −40°C to +85°C, Vdd = 4.5V to 5.5V, Vcc = 10V to 60V unless otherwise specified.

Parameter	Symbol	Conditions	Min	Max	Unit
Logic Supply Voltage	Vdd		4.5	5.5	V
Driver Supply Voltage	Vcc		10	60	V
Logic Supply Current	Idd	All Outputs High			
		MSC1150		1	mA
		MSC1171		2	mA
		MSC1173		3	mA
		All Outputs Low			
		MSC1150		4	mA
		MSC1171		6	mA
		MSC1173		7	mA
Driver Supply Current	Icc	All Outpts High (No Load)			
		MSC1150		3	mA
		MSC1171		4	mA
		MSC1173		6	mA
		All Outputs Low		0.1	mA
High Level Input Voltage	Vih		0.7Vdd	—	V
Low Level Input Voltage	Vil		—	0.8	V
High Level Input Current	Iih	Vih = Vdd	—	1	μA
Low Level Input Current	Iil	Vil = Gnd	—	−1	μA
High Level Output Voltage (Q Outputs)	Voh1	Ioh1 = −25mA	Vcc − 3.5	—	V
Low Level Output Voltage (Q Outputs)	Vol1	Iol1 = 1mA	—	3	V
		Iol1 = 200μA	—	1.5	V
High Level Output Voltage (Serial Out)	Voh2	Ioh2 = −20μA	Vdd − 0.5	—	V
Low Level Output Voltage (Serial Out)	Vol2	Iol = 20μA	—	0.8	V

o AC Characteristics

Ta = −40°C to +85°C, Vdd = 4.5V to 5.5V, Vcc = 10V to 60V unless othervise specified.

Parameter	Symbol	Conditions	Min	Max	Unit
Clock Frequency	f (CLOck)	See Figure 1	-	1	MHz
Pulse Duration, Clock High	tw (CKH)	See Figure 1	250	-	nS
Pulse Duration, Clock Low	tw (CKL)	See Figure 1	250	-	nS
Setup Time, Data Before Rising Clock Edge	tsu	See Figure 1	100	-	nS
Hold Time, Data After Rising Clock Edge	th	See Figure 1	100	-	nS
Delay Time, Clock to Serial Out	td	CL = 15pF, See Figure 1	-	600	nS
Delay Time, Colck Rising Edge to Latch Enable High	tCKH-LEH	See Figure 2	200	-	nS
Pulse Duration, Latch Enable High	tw (LEH)	See Figure 2	250	-	nS
Delay Time, High-to-Low Level Q Output	tDHL	from LATCH ENABLE from BLANKING See Figure 2&3, CL = 50PF	-	1.5 1	µS µS
Delay Time, Low-to-High Level Q Output	tDLH	form LATCH ENABLE from BLANKING See Figure 2&3, CL = 50PF	- -	1.5 1	µS µS
TRANSITION TIME, High-to-Low level Q Output	tTHL	CL = 50PF See Figure 3	-	3	µS
TRANSITION TIME, Low-to-High level Q Output	tTLH	CL = 50PF See Figure 3	-	2	µS

- **Timing Chart**

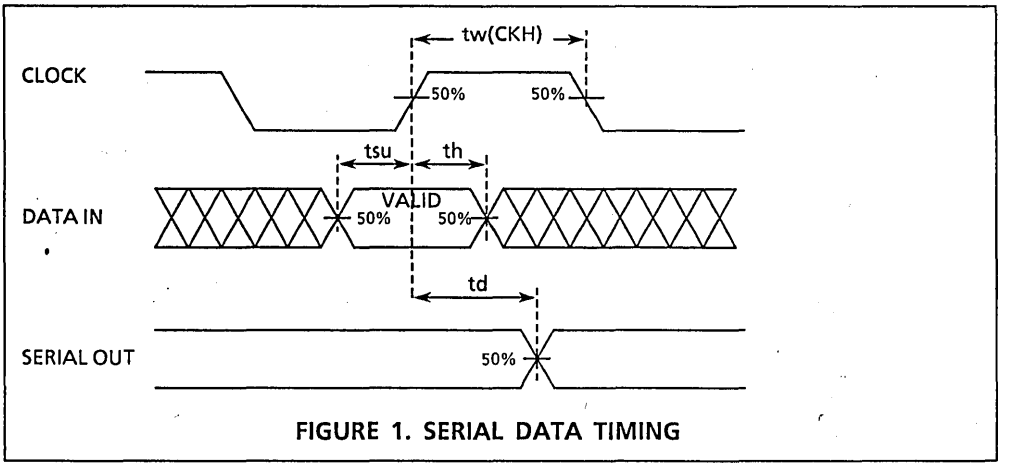


FIGURE 1. SERIAL DATA TIMING

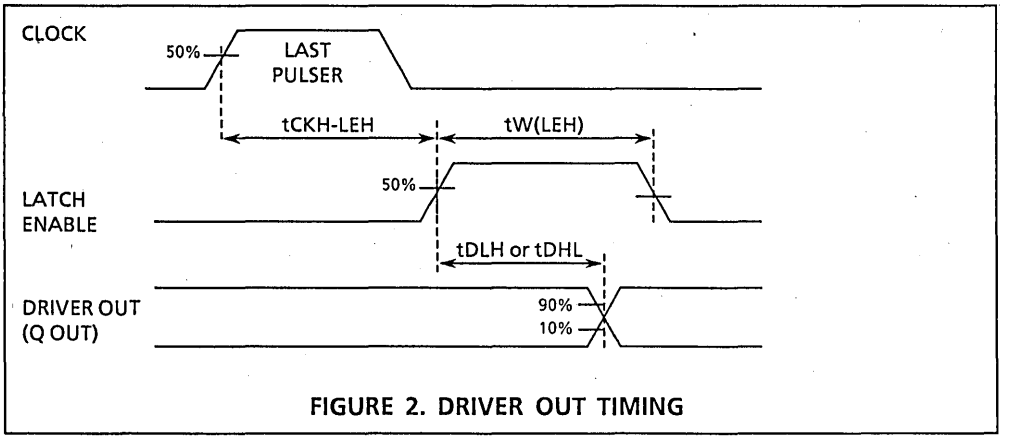


FIGURE 2. DRIVER OUT TIMING

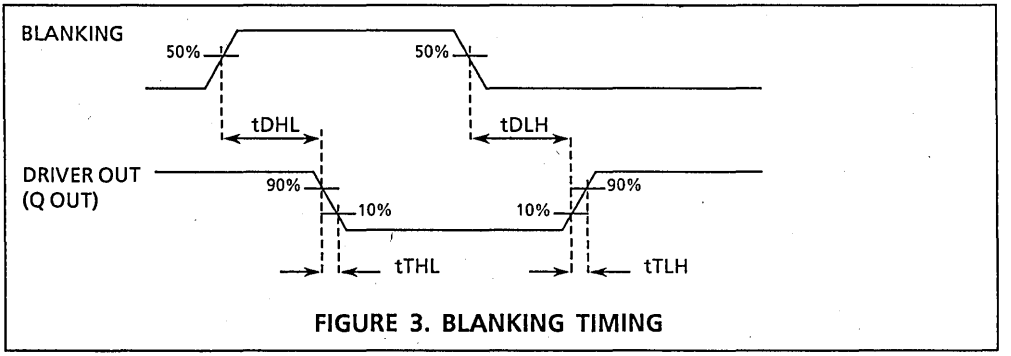


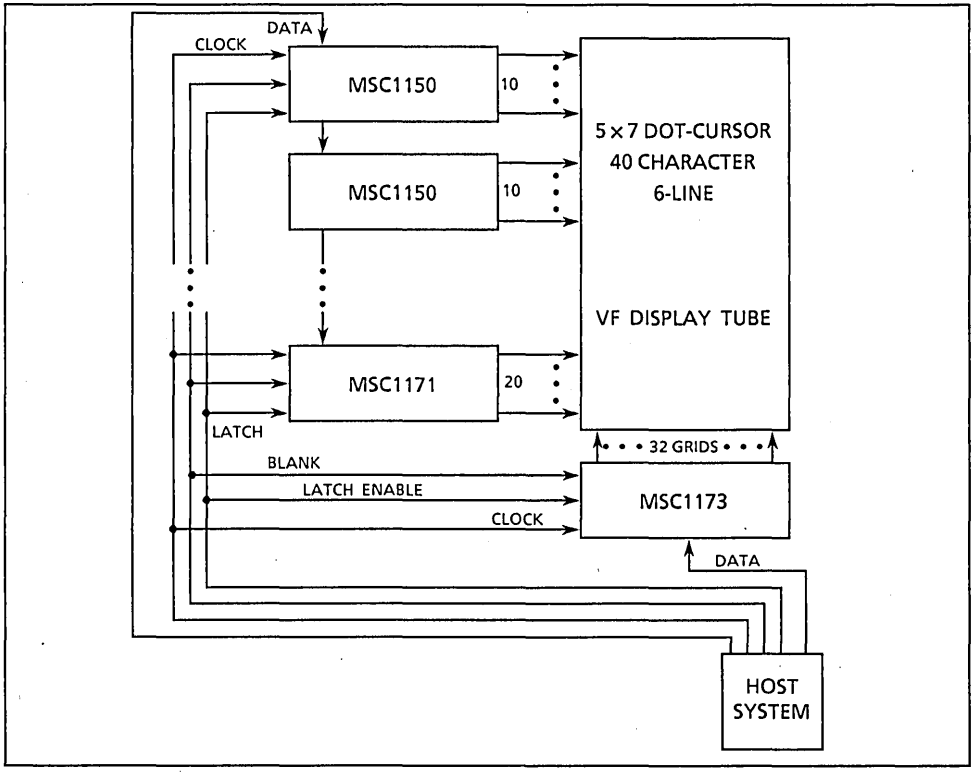
FIGURE 3. BLANKING TIMING

FUNCTION TABLE

Serial Data	Clock	Shift Register Contents I1 I2 . . IN-1 IN	Sarial Data Output	Strobe Input	Latch Contents I1' I2' . . IN-1' IN'	Blacking Input	Output Contents I1 I2 . . IN-1 IN
1	⌐¬	1 R1 . . RN-2 RN-1	RN-1				
0	⌐¬	0 R1 . . RN-2 RN-1	RN-1				
×	¬⌐	R1 R2 . . RN-1 RN	RN		R1 R2 . . RN-1 RN		
		× × . . × ×	×	0	P1 P2 . . PN-1 PN	0	P1 P2 . . PN-1 PN
		P1 P2 . . PN-1 PN	PN	1	× × . . × ×	1	0 0 . . 0 0

0 = Low Logic Level
1 = High Logic Level
× = Irrelevent
P = Present Stats
R = Previous Stats

APPLICATION NOTE



OKI semiconductor
MSC1164

20-BIT ANODE/GRID DRIVER

GENERAL DESCRIPTION

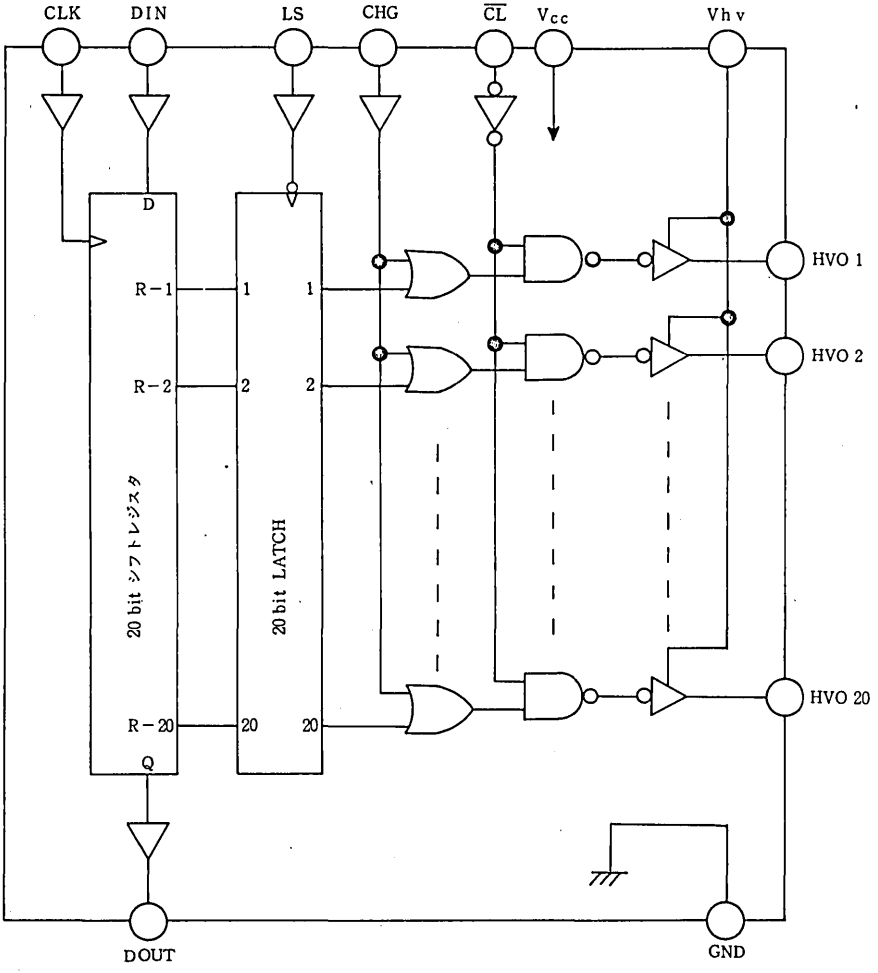
The MSC1164 is a monolithic IC using the Bi-CMOS process for hybridizing CMOS and bipolar transistors on the same chip. The logic portion such as the input stage, shift register and latch is formed by CMOS and the output driver requiring a high withstand voltage is formed by bipoalr transistors.
Since A 32 pins plastic flat package is adopted, the display unit size can be reduced.

FEATURES

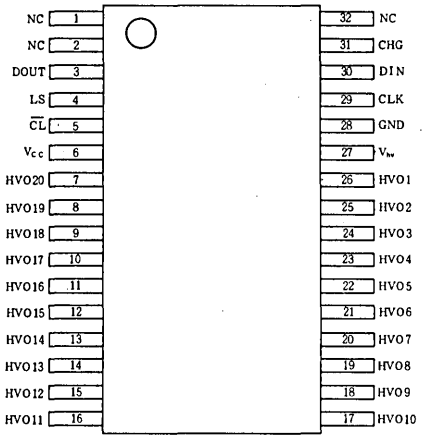
Designed as a VFD grid/anode driver for emitter-follower force output with 20-bit active pull down by built-in 20-bit bidirectional shift register and latch.

- Logic Supply Voltage : Vcc : + 5V
- Driver Supply Voltage : VhV : + 65V
- Driver Output Current : Iohvh : – 40 mA
  Iohvl : 2 mA
- Built-in 20-bit latch
- Built-in 20-bit shift register
- Clock frequency : 4 MHz
- 32 pin FLAT package

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



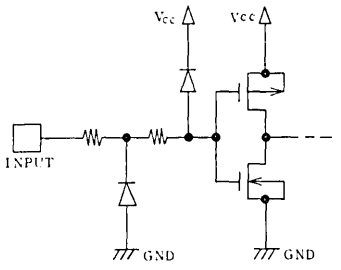
PIN DESCRIPTION

Pin No.	Symbol	Terminal Name	Description
26~7	HVO1~ HVO20	Driver Output	Driver output terminal, applicable to each bit of shift resistor.
27	Vhv	Driver Power Supply	Power supply terminal for driver circuit.
28	GND	Driver GND Logic GND	GND pin for driver circuit. GND pin for the logic circuit.
5	$\overline{CL}$	Clear Input	Clear input pin with pull-up resister. Normally "H" level, in this condition driver output change "H" or "L" according to latch output level. when "L" driver output pins are fixed to "L" and have no relation with latch outputs.
4	LS	Latch Strobe Input	Latch strobe input pin. When LS is "H", information present at the data input is transferred to output. The information is kept latched and the output remains the same, even then LS changes to "L".
30	DIN	Data Input	Data input pin for SR

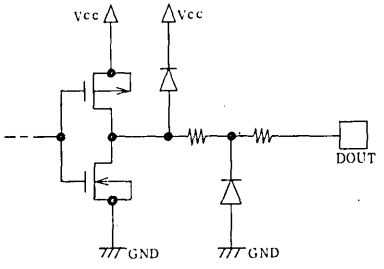
Pin No.	Symbol	Terminal Name	Description
6	V_{CC}	Logic Power Supply	Power supply pin for logic (except driver). V_{CC} should be 4.5V~5.5V.
3	DOUT	Data Output	Serial output pin of SR.
29	CLK	Clock Input	Clock input pin. Data of SR is shifted from one stage to the next during the positive going clock transition.
31	CHG	Test input	Test input pin with pull-down resister. Normally "L" when CHG is "H" and $\overline{CL}$ is "H" driver outputs are fixed to "H" for test.

SCHEMATIC DIAGRAMS OF LOGIC PORTION INPUT AND OUTPUT TERMINAL CIRCUITS

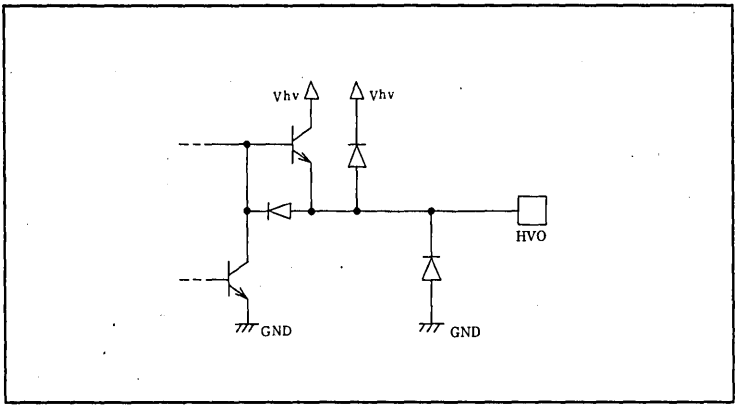
INPUT TERMINAL



OUTPUT TERMINAL



SCHEMATIC DIAGRAM OF DRIVER OUTPUT TERMINAL CIRCUIT



FUNCTION TABLE

CLK	D in	R-1	R-2	R-3	R-4	.....	R-20	Dout
↑	H	H	$R1_n$	$R2_n$	$R3_n$		$R19_n$	$R19_n$
↑	L	L	RI_n	$R2_n$	$R3_n$		$R19_n$	$R19_n$

$\overline{CL}$	CHG	LS	R.X	HVO. X
L	X	X	X	L
H	H	X	X	H
H	L	H	H	H
H	L	H	L	L
H	L	L	X	NC

L: Low Level, H: High Level, X: Don't Care, NC: No Change

ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Item	Symbol	Condition	Limits	Unit	Note
Logic Supply Voltage	V_{cc}	Applicable to logic supply voltage terminal	− 0.3~ + 6.5	V	1
Driver Supply Voltage	V_{hv}	Applicable to driver supply voltage terminal	Vcc~ + 70	V	1
Input Voltage	V_{in}	Applicable to all input terminal	− 0.3~Vcc + 0.3	V	1
Data Output Voltage	V_{out}	Applicable to all output terminal	− 0.3~Vcc + 0.3	V	1
Driver Driving Frequency	f_{drv}	Duty cycle 50% max	0~ + 50	KHz	–
Power Dissipation	P_d	Ta≦25°C	790 [Derate 6.3 mW/C above 25°C]	mW	–
Attenuation Rate	R_{j-a}	Ta≧25°C	158	°C/W	2
Operating Temperature	T_{op}	Thv≦50V	− 40~ + 85	°C	–
Storage Temperature	T_{stg}	–	− 55~ + 150	°C	–

NOTES: 1) Maximum Supply Voltage for GND

2) Derate 6.9 mW/Ck above 25°C
Refer to the following formula.
$T_j = P \times R_{j-a} + Ta$ (P: Max current consumption)

• Recommended Operating Conditions

Item	Symbol	Condition		Min.	Max.	Unit
Logic Supply Voltage	V_{cc}	Applicable to logic supply voltage terminal		4.5	5.5	V
Driver Supply Voltage	V_{hv}	Applicable to driver supply voltage terminal		10	65	V
High Level Input Voltage	V_{ih}	Applicable to all input terminals	V_{cc} = 4.5V	3.6	–	
			V_{cc} = 5.5V	4.4	–	V
Low Level Input Voltage	V_{il}	Applicable to all output terminals	V_{cc} = 4.5V	–	0.9	V
			V_{cc} = 5.5V	–	1.1	V
Driver High Level Output Current	$I_{ohvh\,1}$	1 Output is High at a time		–	– 40	mA
Driver High Level Output Current	$I_{ohvh\,2}$	All driver output are High at a time		–	– 2	mA
Driver Low Level Output Current	I_{ohvl}	Applicable to all driver output terminal		–	2	mA
CLK Frequency	$f\phi$	See timing chart		–	4	MHz
CLK Pulse width	t_{wclk}	See timing chart		75	–	ns
Data in Setup Time	t_{ds}	See timing chart		50	–	ns
Data in Hold Time	t_{dh}	See timing chart		50	–	ns
LS Pulse Width	t_{wls}	See timing chart		80	–	ns
CLK - LS Delay Time	t_{dcl}	See timing chart		50	–	ns
LS - CLK Delay Time	t_{dlc}	See timing chart		0	–	ns
LS - CHG Delay Time	t_{dlcg}	See timing chart		0	–	µs
LS - CL Delay Time	$t_{dl\overline{cl}}$	See timing chart		0	–	µs
CHG Pulse Width	t_{wchg}	See timing chart		2	–	µs
$\overline{CL}$ PUlse width	$t_{w\overline{cl}}$	See timing chart		2	–	µs
Operating Temperature	T_{op}	–		– 40	+ 85	°C

• DC Characteristics

V_{cc} = 5V ± 10%, V_{hv} = 10V~65V, Ta = −40°C to +85°C

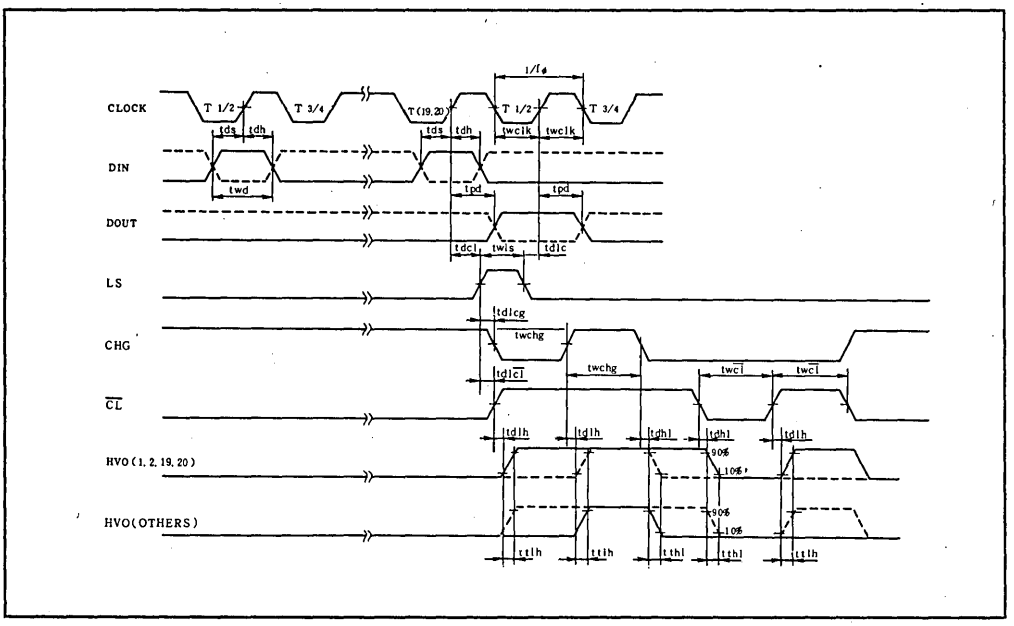
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Logic Standby Current	I_{cc1}	No Load V_{cc} = 5.5V	All Input: Low	–	2.3	3.4	mA
	I_{cc2}		All Input: High, All Driver Output: High, Ta = 25°C	–	0.5	1.0	
Driver Standby Current	I_{hv1}	No Load V_{cc} = 5.5V	All Driver Output: Low	–	–	1	μA
	I_{hv2}		All Driver Output: High, Ta = 25°C	–	1.3	2.0	mA
High Level Input Voltage	V_{ih}		V_{cc} = 4.5V	3.15	–	–	V
			V_{cc} = 5.5V	3.85	–	–	V
Low Level Input Voltage	V_{il}		V_{cc} = 4.5V	–	–	1.35	V
			V_{cc} = 5.5V	–	–	1.65	V
Input Leakage Current	I_{in}	Ta = 25°C		–	–	±1	μA
Input Capacitance	C_{in}	Ta = 25°C		–	15	–	pF
High Level Data Output Voltage	V_{odh1}	Io = −20μA	V_{cc} = 4.5V	4.2	–	–	V
			V_{cc} = 5.5V	5.2	–	–	V
Low Level Data Output Voltage	V_{odl1}	Io = 20μA	V_{cc} = 4.5V	–	–	0.2	V
			V_{cc} = 5.5V	–	–	0.2	V
High Level Data Output Voltage	V_{odh2}	Io = −0.1mA	V_{cc} = 4.5V	3.5	–	–	V
			V_{cc} = 5.5V	4.5	–	–	V
Low Level Data Output Voltage	V_{odl2}	Io = 0.1mA	V_{cc} = 4.5V	–	–	1.1	V
			V_{cc} = 5.5V	–	–	1.1	V
Driver High Level Output Voltage	V_{ohvh}	I_{ohv} = −40mA		Vhv − 4	–	–	V
Driver Low Level Output Voltage	V_{ohvl}	I_{ohv} = 2mA		–	–	3.0	V

• AC Characteristics

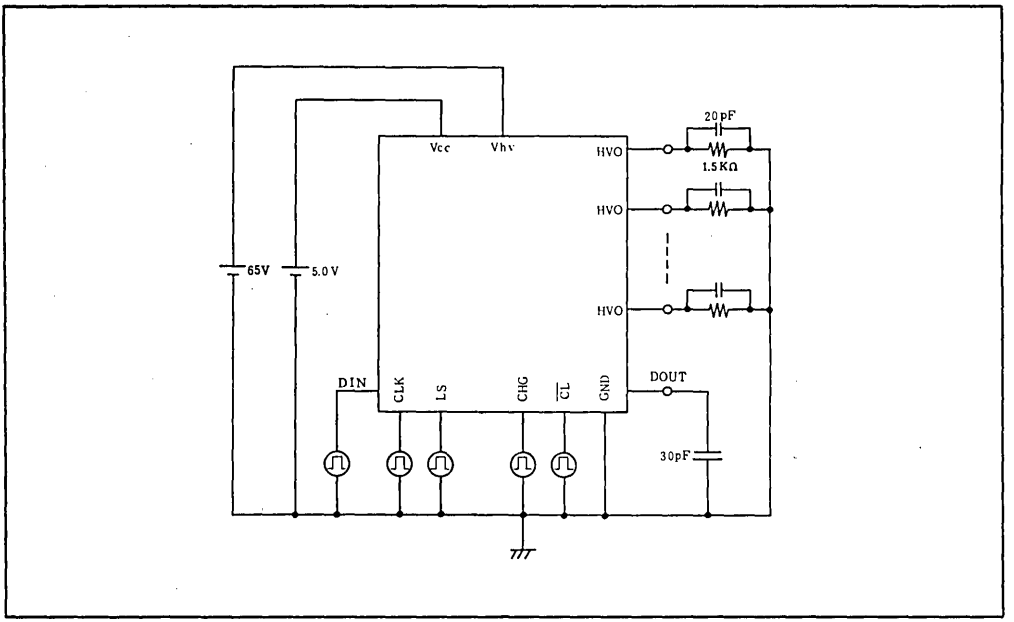
Vcc = 5V, Vhv = 65V, Ta = 25°C

Item	Symbol	Remarks	Min.	Typ.	Max.	Unit
CLK – Dout Delay Time	t_{pd}	See timing chart and test circuit	–	100	150	nS
Delay Time Low – High	t_{dlh}	See timing chart and test circuit	–	0.3	1	µS
Transit Time Low – High	t_{tlh}	See timing chart and test circuit	–	2	5	µS
Delay Time Low – High	t_{dhl}	See timing chart and test circuit	–	0.3	1	µS
Transit Time High – Low	t_{thl}	See timing chart and test circuit	–	2	5	µS

• Timing Chart



TEST CIRCUIT



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OKI semiconductor
MSC1165
20-BIT ANODE/GRID DRIVER

GENERAL DESCRIPTION

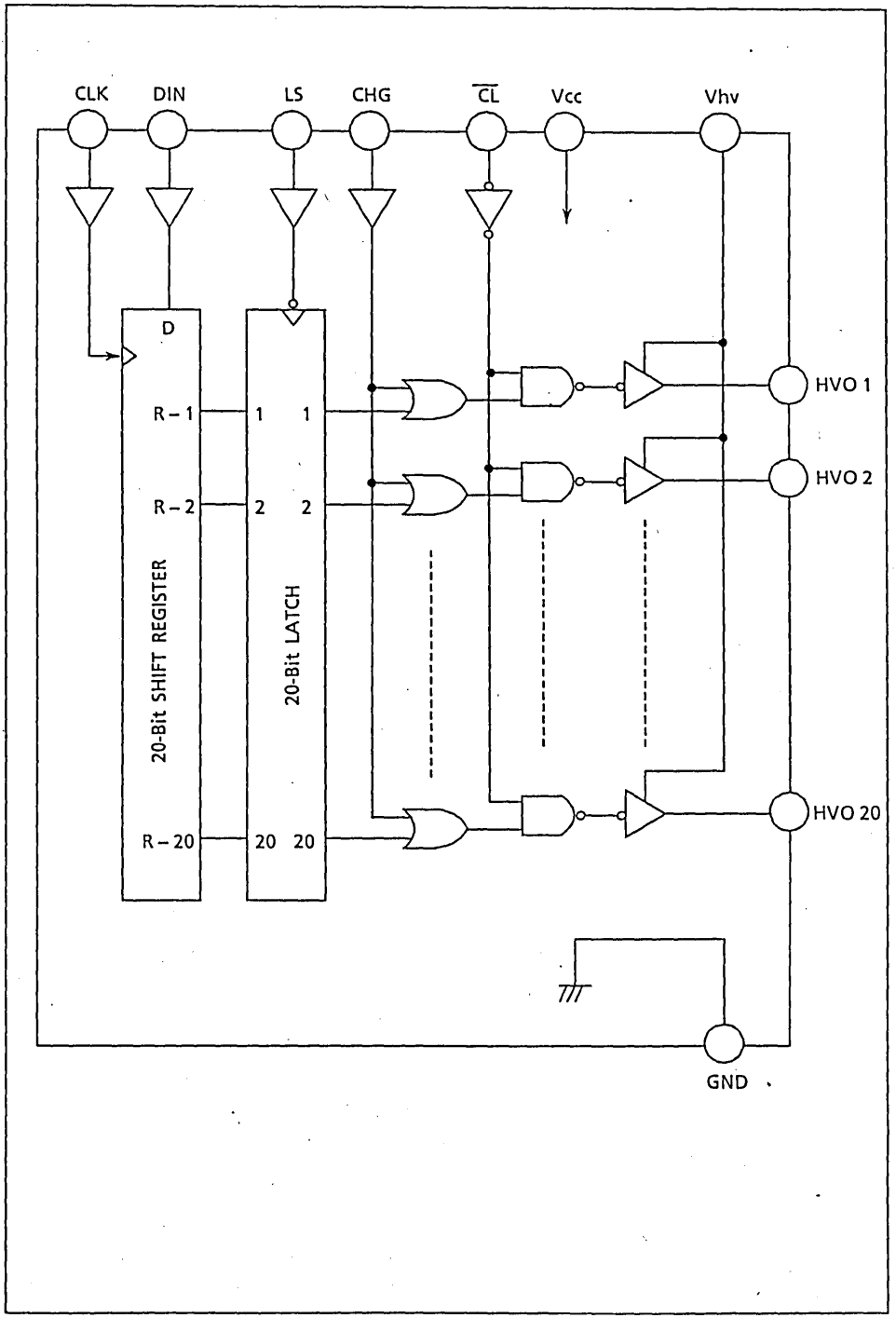
The MSC1165 is a monolithic IC using the Bi-CMOS process for hybridizing CMOS and bipolar transistors on one chip.

The logic portion such as the input stage, shift register and latch is formed by CMOS, and the output driver requiring a high withstand voltage is formed by bipolar transistors.

FEATURES

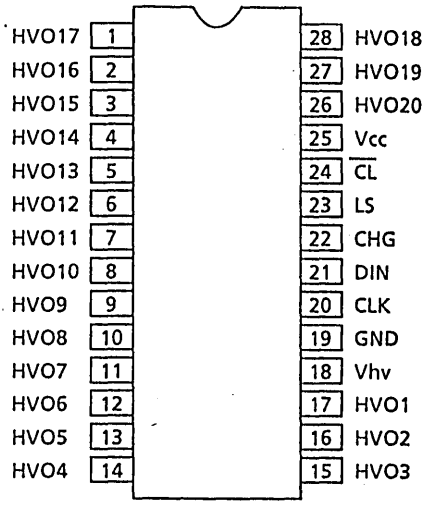
- Logic supply voltage (V_{CC}) : +5 V
- VF driver supply voltage (V_{hv}) : +65 V
- VF driver output current
  (I_{ohvh1}) : −40 mA (1 driver output high)
  (I_{ohvh2}) : −2 mA (All driver output high)
  (I_{ohv1}) : +2 mA
- Clock frequency : 4 MHz
- Built-in 20-bit latch
- Built-in 20-bit shift register
- 28 Pin DIP Package

BLOCK DIAGRAM



PIN CONFIGURATION

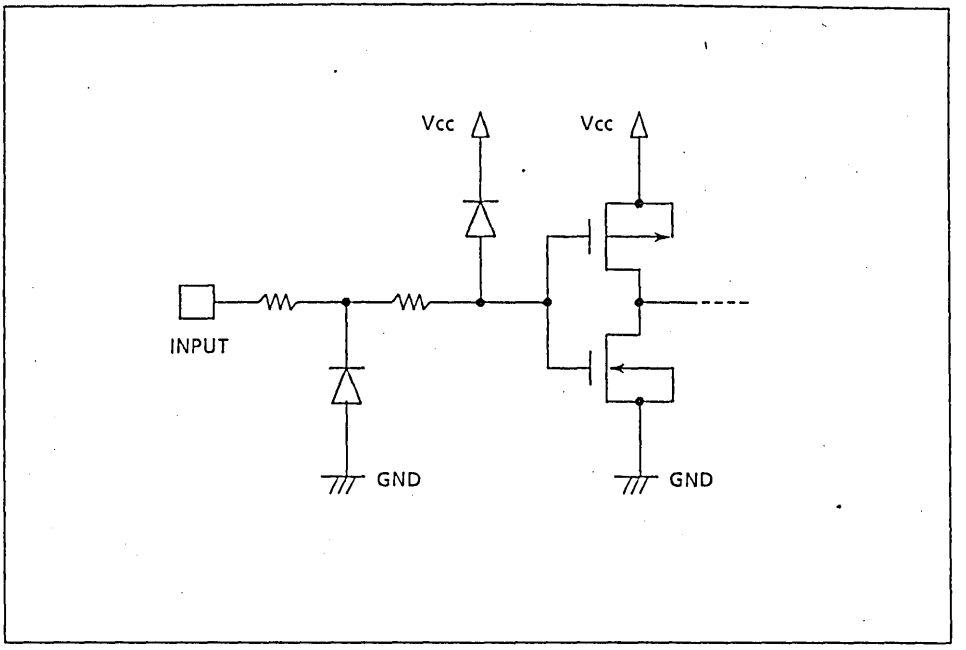
(Top View) 28 Lead Plastic DIP



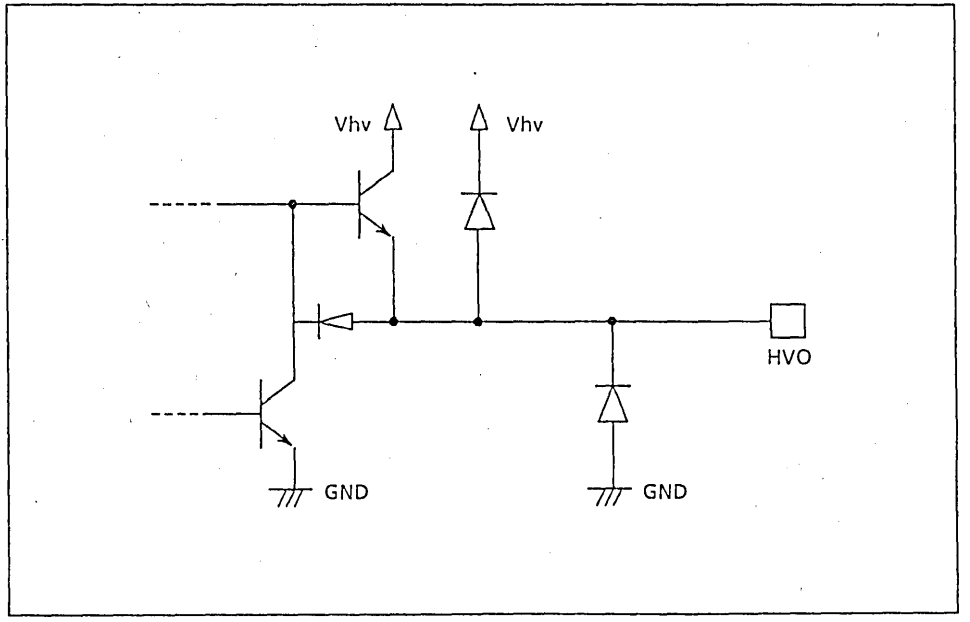
PIN DESCRIPTION

Pin No.	Symbol	Name	Description
17 ⋮ 1 28 ⋮ 26	HVO 01 ⋮ HVO 17 HVO 18 ⋮ HVO 20	Driver output	1. Each terminal is a driver output terminal, which corresponds to each bit of the shift register.
18	Vhv	Driver supply voltage	1. This is a power terminal of the driver circuit.
19	GND	Driver GND LOgic portion GND	1. This is a grounding terminal of the driver circuit, and the logic portion.
24	$\overline{CL}$	Clear input	1. This is an input terminal containing a pull-up resistor. 2. The terminal is generally kept High. The driver output, High of Low, is driven by the output of the corresponding latch circuit. 3. When the terminal is Low, the driver outputs are fixed to "Low" regardless of the output of the latch circuit.
23	LS	Latch strobe input	1. This is an input terminal without a pull-up or pull-down registor. 2. When the terminal is High, the latch circuit is slewed, and the output of the shift register is that of the latch circuit. 3. When the terminal is Low, the latch circuit holds the output of the shift register immediately before the terminal is turned Low.
21	DIN	Data input	1. This is an input terminal of the shift register to input the display data in synchronization wiht a clock pulse. (Positive logic)
25	V_{CC}	Logic supply voltage	1. This is a power terminal of the logic portion (other than the driver circuit).
20	CLK	Clock input	1. This is an input terminal without a pull-up or pull-down resistor 2. The data of the shift register is shifted at the rising edge of a clock pulse.
22	CHG	Test input	1. This is an input terminal containing a pull-down resistor. 2. The terminal is generally kept Low. When the $\overline{CL}$ terminal is High, the driver output, High or Low, is driven by theoutput of the corresponding latch circuit. 3. The terminal is Low and the $\overline{CL}$ terminal is High, the driver output can be fixed to High regardless of the output of the latch circuit.

SCHEMATIC DIAGRAM OF LOGIC PORTION INPUT TERMINAL CIRCUIT



SCHEMATIC DIAGRAM OF DRIVER OUTPUT TERMINAL CIRCUIT



FUNCTION TABLE

CLK	DIN	R-1	R-2	R-3	R-4	R-20
↑	H	H	R1n	R2n	R3n	R19n
↑	L	L	R1n	R2n	R3n	R19n

$\overline{CL}$	CHG	LS	R.X	HVO.X
L	X	X	X	L
H	H	X	X	H
H	L	H	H	H
H	L	H	L	L
H	L	L	X	NC

L: Low Level, H: High, Level, X: Don't Care, NC: No Change

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit	Note
Logic portion supply voltage	V_{CC}	Applicable to logic power terminal	-0.3~6.5	V	1
Driver supply voltage	Vhv	Applicable to driver power terminal	V_{CC}~70	V	1.2
Input voltage	Vin	Applicable to all the input terminals	0.3~V_{CC}+0.3	V	1
Driver drive frequency	fdrv	Duty less than 50%	0~50	kHz	
Power Dissipation	Pd	Ta≦25°C	1020	mW	
Attenuation Rate	Rj-a	Ta>25°C	122	°C/w	2
Operating temperature	Top	Vhv≦50V	-40~+85	°C	
Storage temperature	Tstg	—	-55~+150	°C	

Note 1: The maximum voltage which can be applied t the GND terminal.

Note 2: Thermal resistance of the package (between junction and atmosphere) The junction temperature (Tj) expressed by the equation indicated below should not exceed 150°C.

$Tj = P \times Rj - a + Ta$ (P: Maximum power consumption of IC)

• Recommended Operating Conditions

Parameter	Symbol	Condition		MIN	MAX	Unit
Logic supply voltage	V_{CC}	Applicable to logic power terminal		4.5	5.5	V
Driver supply voltage	V_{hv}	Applicable to driver power terminal		10	65	V
High level input voltage	V_{IH}	Applicable to all input terminals	Vcc = 4.5V	3.6	—	V
			Vcc = 5.5V	4.4	—	V
Low level input voltage	V_{IL}	Applicable to all input terminals	Vcc = 4.5V	—	0.9	V
			Vcc = 5.5V	—	1.1	V
Driver high level output current	IOHVH 1	1 driver output: High Other drive outputs: Low		—	− 40	mA
Driver high level output current	IOHVH 2	All driver output : High		—	− 2	mA
Driver low level output current	IOHVL	Applicable to all driver output terminals		—	2	mA
Clock frequency	fØ	See Timing Chart		—	4	MHz
Clock pulse width	twclk	See Timing Chart		75	—	nS
Data setup time	tds	See Timing Chart		50	—	nS
Data hold time	tdh	See Timing Chart		50	—	nS
LS pulse width	twls	See Timing Chart		80	—	nS
CLK-LS delay time	tdcl	See Timing Chart		50	—	nS
LS-CLK delay time	tdlc	See Timing Chart		0	—	nS
LS-CHG delay time	tdlcg	See Timing Chart		0	—	µS
LS-$\overline{CL}$ delay time	td$\overline{cl}$	See Timing Chart		0	—	µS
CHG pulse width	twchg	See Timing Chart		2	—	µS
$\overline{CL}$ pulse width	tw$\overline{cl}$	See Timing Chart		2	—	µS
Operating temperature range	Top	—		− 40	+ 85	°C

• DC Characteristics

V_{CC} = 5V ± 10%, Vhv = 10V~65V, Ra = − 40°C~85°C

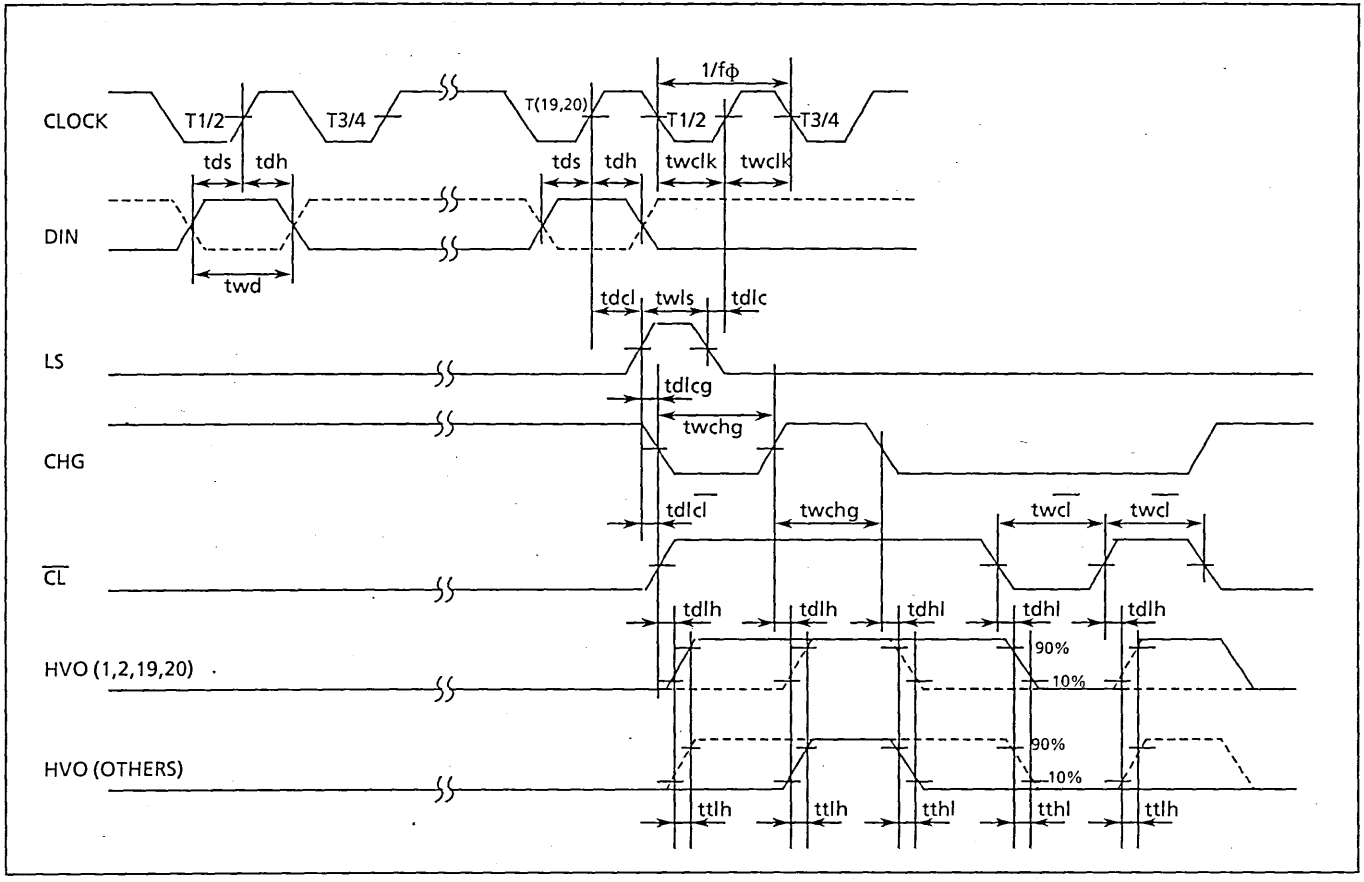
Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
Logic supply current	Icc1	No load V_{CC} = 5.5V	All inputs:Low	—	2.3	3.4	mA
	Icc2		All inputs:High All driver outputs: High Ta = 25°C	—	0.5	1.0	
Driver supply current	Ihv_2	No load V_{CC} = 5.5V	All driver outputs: Low	—	—	50	µA
	Ihv_2		All driver oututs: High Ta = 25°C	—	1.3	2.0	mA
High input voltage	Vih		V_{CC} = 4.5V	3.15	—	—	V
			V_{CC} = 4.5V	3.85	—	—	
Low input voltage	Vil		V_{CC} = 4.5V	—	—	1.35	V
			V_{CC} = 4.5V	—	—	1.65	
Input leak current	V_{OH}	Ta = 25°C		—	—	±1	µA
Input capacity	V_{OL}	Ta = 25°C		—	15	—	pF
High driver output voltage	Vohvh	Iohv = − 40mA		Vhv − 4	—	—	V
Low driver output voltage	Vohvl	Iohv = 2mA		—	—	3.0	V

• AC Characteristics

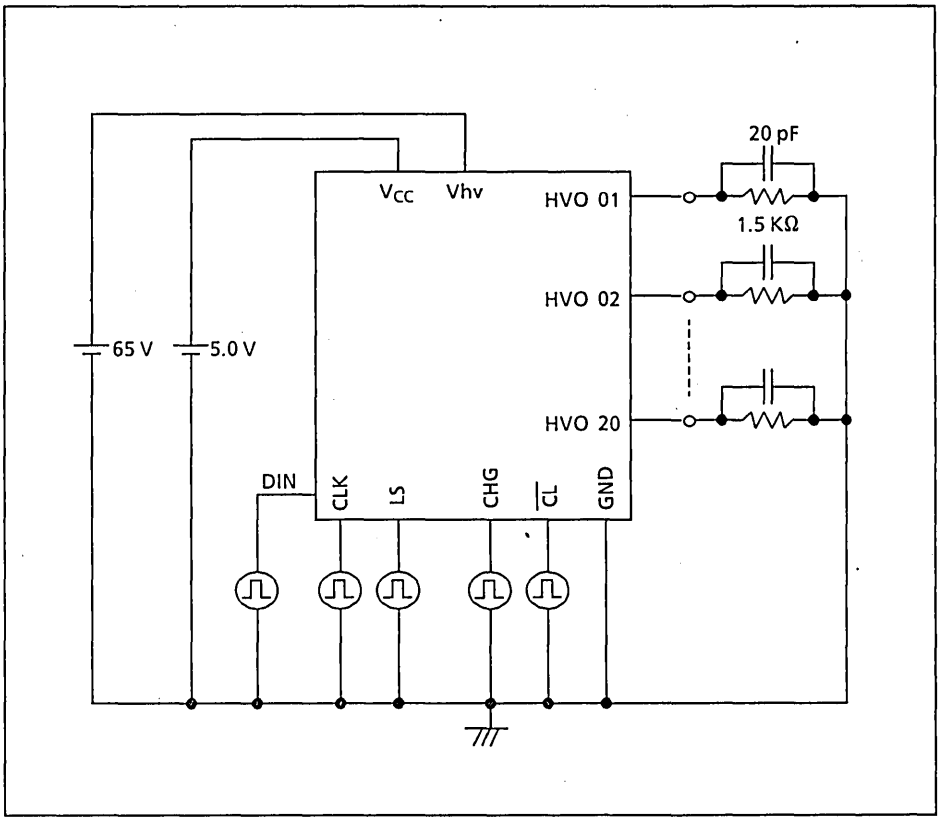
V_{cc} = 5V, Vhv = 65V, Ta = 25°C

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Delay time L - H	tdlh	See Timing Chart and Test circuit.	—	0.3	1	µS
Transit time L - H	ttlh	See Timing Chart and Test circuit.	—	2	5	µS
Delay time H - L	tdhl	See Timing Chart and Test circuit.	—	0.3	1	µS
Transit time H - L	tthl	See Timing Chart and Test circuit.	—	2	5	µS

• Timing Chart



o Test Circuit



OKI semiconductor
MSC1162

40-BIT ANODE/GRID DRIVER

GENERAL DESCRIPTION

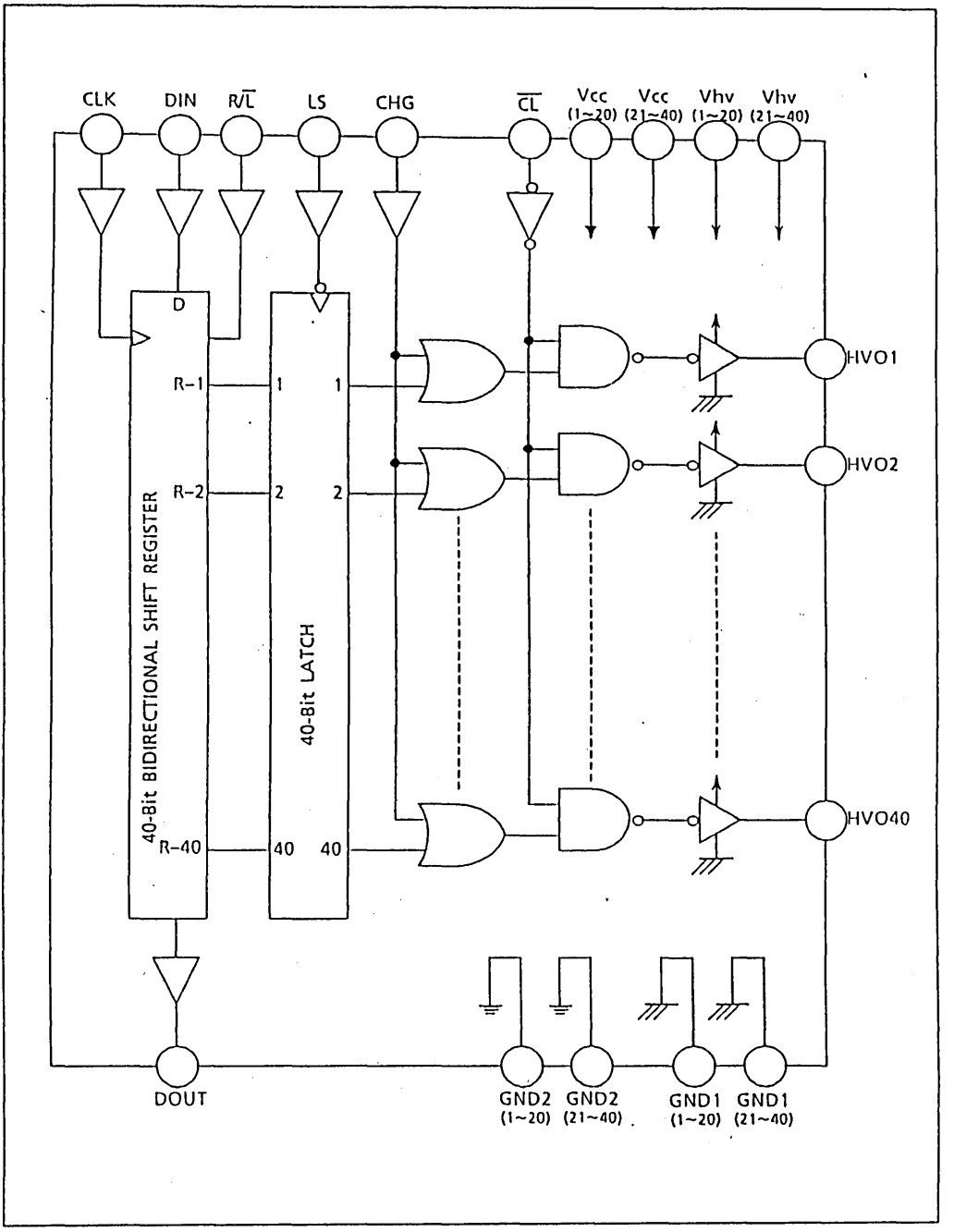
The MSC1162 is a monolithic IC using the Bi-CMOS process for hybridizing CMOS and bipolar transistors on the same chip. The logic portion such as the input stage, shift register and latch is formed by CMOS and the output driver requiring a high withstand voltage is formed by bipoalr transistors.
Since the pin asignment allows single side pattern formation on the printed circuit board, the display unit size can be reduced.
The bidirectional shift register facilitates the pattern design when the deivces are arranged symmetrically with the display as the center axis.

FEATURES

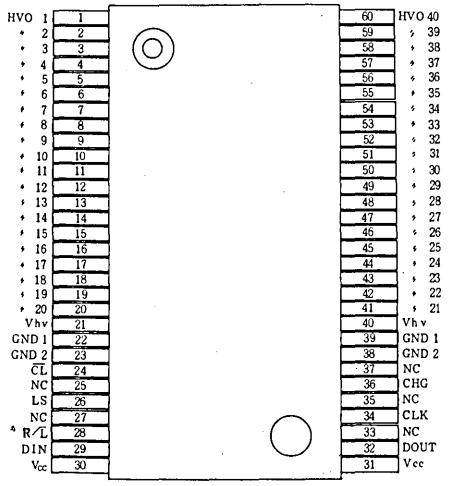
Designed as a VFD grid driver for emitter-follower force output with 40-bit active pull down by built-in 40-bit bidirectional shift register and latch.

- Logic Supply Voltage : Vcc : + 5V
- Driver Supply Voltage : Vhv : + 65V
- Driver Output Current : Iohvh : – 40 mA
  Iohvl : 2 mA
- Built-in 40-Bit latch
- Built-in 40-Bit bidirectional shift register
- Clock frequency : 4 MHz
- 60 pin FLAT Package

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



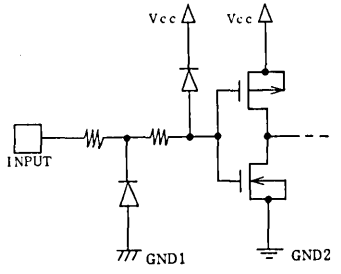
PIN DESCRIPTION

Pin No.	Symbol	Terminal Name	Description
1~20 41~60	HVO1~ HVO40	Driver Output	Driver output terminal, applicable to each bit of shift resistor
21 40	Vhv	Driver Power Supply	Power supply terminal for driver circuit
22 39	GND 1	Driver GND	GND pin for driver circuit
23 38	GND 2	Logic GND	GND pin for the logic circuit. As GND1 and GND2 are not connected inside of the LSI, they need to be connected outside by same wiring.
24	$\overline{CL}$	Clear Input	Clear input pin with pull-up resister. Normally "H" level, in this condition driver output change "H" or "L" according to latch output level. when "L" driver output pins are fixed to "L" and have no relation with latch outputs.
26	LS	Latch Strobe Input	Latch strobe input pin. When LS is "H", information present at the data input is transferred to output. The information is kept latched and the output remains the same, even then LS changes to "L".
28	R/$\overline{L}$	Shift Direction Control	Shift direction control pin with pull-up resistetr. Normally "H", and in this condition, information of Bi-directional SR is shifted to the direction of R-1 from R-40. When this pin is "L", Bi-directional SR shifts information to the direction of R-40 from R-1.

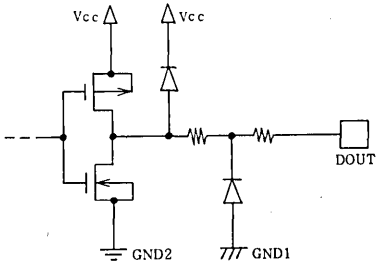
Pin No.	Symbol	Terminal Name	Description
29	DIN	Data Input	Data input pin for bidirectional SR
30 31	V_{cc}	Logic Power Supply	Power supply pin for logic (except driver). V_{cc} should be 4.5V~5.5V.
32	DOUT	Data Output	Serial output pin of bidirectional SR. When R/$\overline{L}$ is "H", D OUT outputs R-40. When R/$\overline{L}$ is "L", D OUT outputs R-1.
34	CLK	Clock Input	Clock input pin. Data of bidirectional SR is shifted from one stage to the next during the positive going clock transition.
36	CHG	Test input	Test input pin with pull-down resister. Normally "L" when CHG is "H" and $\overline{CL}$ is "H" driver outputs are fixed to "H" for test.

SCHEMATIC DIAGRAMS OF LOGIC PORTION INPUT AND OUTPUT TERMINAL CIRCUITS

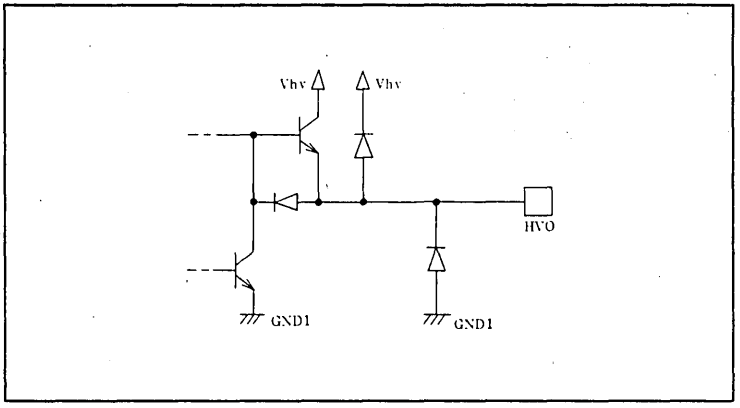
INPUT TERMINAL



OUTPUT TERMINAL



SCHEMATIC DIAGRAM OF DRIVER OUTPUT TERMINAL CIRCUIT



FUNCTION TABLE

CLK	R/$\overline{L}$	D in	R-1	R-2	R-3	R-4	.....	R-40	Dout
↑	H	H	H	$R1_n$	$R2_n$	$R3_n$		$R39_n$	$R39_n$
↑	H	L	L	RI_n	$R2_n$	$R3_n$		$R39_n$	$R39_n$
↑	L	H	$R2_n$	$R3_n$	$R4_n$	$R5_n$		H	$R2_n$
↑	L	L	$R2_n$	$R3_n$	$R4_n$	$R5_n$		L	$R2_n$

$\overline{CL}$	CHG	LS	R.X	HVO. X
L	X	X	X	L
H	H	X	X	H
H	L	H	H	H
H	L	H	L	L
H	L	L	X	NC

L: Low Level, H: High Level, X: Don't Care, NC: No Change

ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Parameter	Symbol	Condition	Limits	Unit	Note
Logic Supply Voltage	V_{cc}	Applicable to logic supply voltage terminal	− 0.3~ + 6.5	V	1
Driver Supply Voltage	V_{hv}	Applicable to driver supply voltage terminal	Vcc~ + 70	V	1
Input Voltage	V_{in}	Applicable to all input terminal	− 0.3~Vcc + 0.3	V	1
Data Output Voltage	V_{out}	Applicable to all output terminal	− 0.3~Vcc + 0.3	V	1
Driver Driving Frequency	f_{drv}	Duty cycle 50% max	0~ + 15	KHz	−
Power Dissipation	P_d	Ta ≦ 25°C	860 [Derate 6.9 mW/C above 25°C]	mW	−
Attenuation Rate	R_{j-a}	Ta > 25°C	145	°C/W	2
Operating Temperature	T_{op}	Thv ≦ 50V	− 40~ + 85	°C	−
Storage Temperature	T_{stg}	—	− 55~ + 150	°C	−

NOTES: 1) Maximum Supply Voltage for GND

2) Derate 6.9 mW/Ck above 25°C
Refer to the following formula.
$T_j = P \times R_{j-a} + Ta$ (P: Max current consumption)

• Recommended Operating Conditions

parameter	Symbol	Condition		Min.	Max.	Unit
Logic Supply Voltage	V_{cc}	Applicable to logic supply voltage terminal		4.5	5.5	V
Driver Supply Voltage	V_{hv}	Applicable to driver supply voltage terminal		10	65	V
High Level Input Voltage	V_{ih}	Applicable to all input terminals	V_{cc} = 4.5V	3.6	–	
			V_{cc} = 5.5V	4.4	–	V
Low Level Input Voltage	V_{il}	Applicable to all output terminals	V_{cc} = 4.5V	–	0.9	V
			V_{cc} = 5.5V	–	1.1	V
Driver High Level Output Current	I_{ohvh}	1 Output is High at a time		–	– 40	mA
Driver Low Level Output Current	I_{ohvl}	Applicable to all driver output terminal		–	2	mA
CLK Frequency	$f\phi$	See timing chart		–	4	MHz
CLK Pulse width	t_{wclk}	See timing chart		75	–	ns
Data in Setup Time	t_{ds}	See timing chart		50	–	ns
Data in Hold Time	t_{dh}	See timing chart		50	–	ns
LS Pulse Width	t_{wls}	See timing chart		80	–	ns
CLK - LS Delay Time	t_{dcl}	See timing chart		50	–	ns
LS - CLK Delay Time	t_{dlc}	See timing chart		0	–	ns
LS - CHG Delay Time	t_{dlcg}	See timing chart		0	–	µs
LS - CL Delay Time	$t_{dl\overline{cl}}$	See timing chart		0	–	µs
CHG Pulse Width	t_{wchg}	See timing chart		2	–	µs
$\overline{CL}$ PUlse width	$t_{w\overline{cl}}$	See timing chart		2	–	µs
Operating Temperature	T_{op}	–		– 40	+ 85	°C

o DC Characteristics

Vcc = 5V ± 10%, Vhv = 10V~65V, Ta = −40°C to +85°C

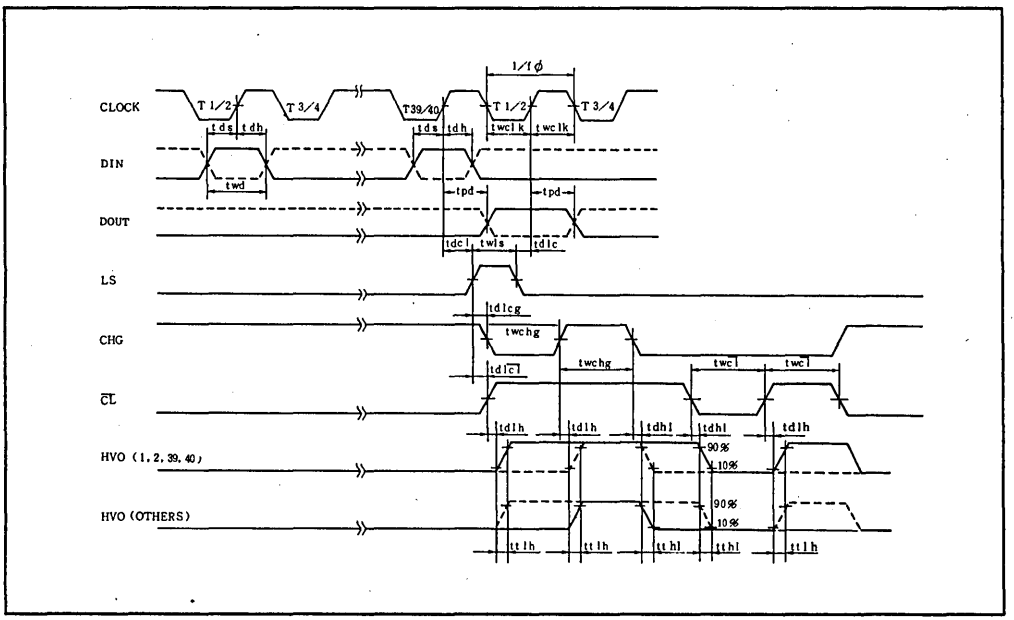
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Logic Standby Current	I_{cc1}	No Load V_{cc} = 5.5V	All Input: Low	–	4.3	6.65	mA
	I_{cc2}		All Input: High, All Driver Output: High, Ta = 25°C	–	0.5	1.0	
Driver Standby Current	I_{hv1}	No Load V_{cc} = 5.5V	All Driver Output: Low	–	–	1	μA
	I_{hv2}		All Driver Output: High, Ta = 25°C	–	2.45	3.8	mA
High Level Input Voltage	V_{ih}		V_{cc} = 4.5V	3.15	–	–	V
			V_{cc} = 5.5V	3.85	–	–	V
Low Level Input Voltage	V_{il}		V_{cc} = 4.5V	–	–	1.35	V
			V_{cc} = 5.5V	–	–	1.65	V
Input Leakage Current	I_{in}	Ta = 25°C		–	–	± 1	μA
Input Capacitance	C_{in}	Ta = 25°C		–	15	–	pF
High Level Data Output Voltage	V_{odh1}	Io = −20μA	V_{cc} = 4.5V	4.2	–	–	V
			V_{cc} = 5.5V	5.2	–	–	V
Low Level Data Output Voltage	V_{odl1}	Io = 20μA	V_{cc} = 4.5V	–	–	0.2	V
			V_{cc} = 5.5V	–	–	0.2	V
High Level Data Output Voltage	V_{odh1}	Io = −0.1mA	V_{cc} = 4.5V	3.5	–	–	V
			V_{cc} = 5.5V	4.5	–	–	V
Low Level Data Output Voltage	V_{odl2}	Io = 0.1mA	V_{cc} = 4.5V	–	–	1.1	V
			V_{cc} = 5.5V	–	–	1.1	V
Driver High Level Output Voltage	V_{ohvh}	I_{ohv} = −40mA		Vhv − 4	–	–	V
Driver Low Level Output Voltage	V_{ohvl}	I_{ohv} = 2mA		–	–	3.0	V

• AC Characteristics

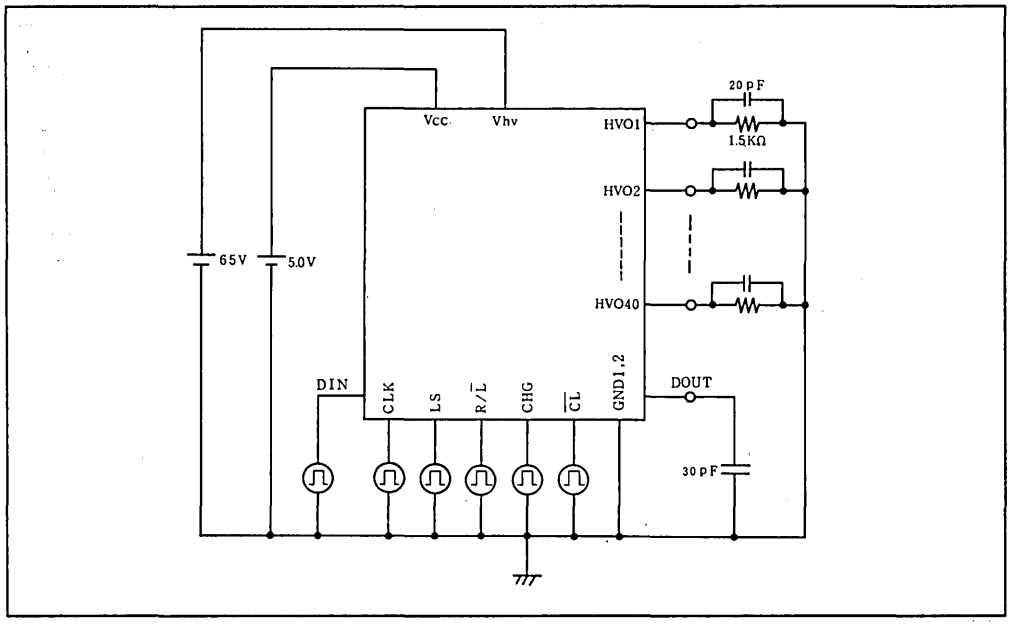
Vcc = 5V, Vhv = 65V, Ta = 25°C

Item	Symbol	Remarks	Min.	Typ.	Max.	Unit
CLK – Dout Delay Time	t_{pd}	See timing chart and test circuit	–	100	150	nS
Delay Time Low – High	t_{dlh}	See timing chart and test circuit	–	0.3	1	µS
Transit Time Low – High	t_{tlh}	See timing chart and test circuit	–	2	5	µS
Delay Time Low – High	t_{dhl}	See timing chart and test circuit	–	0.3	1	µS
Transit Time High – Low	t_{thl}	See timing chart and test circuit	–	2	5	µS

• Timing Chart



TEST CIRCUIT



OKI semiconductor
MSC1172
40-BIT ANODE / GRID DRIVER

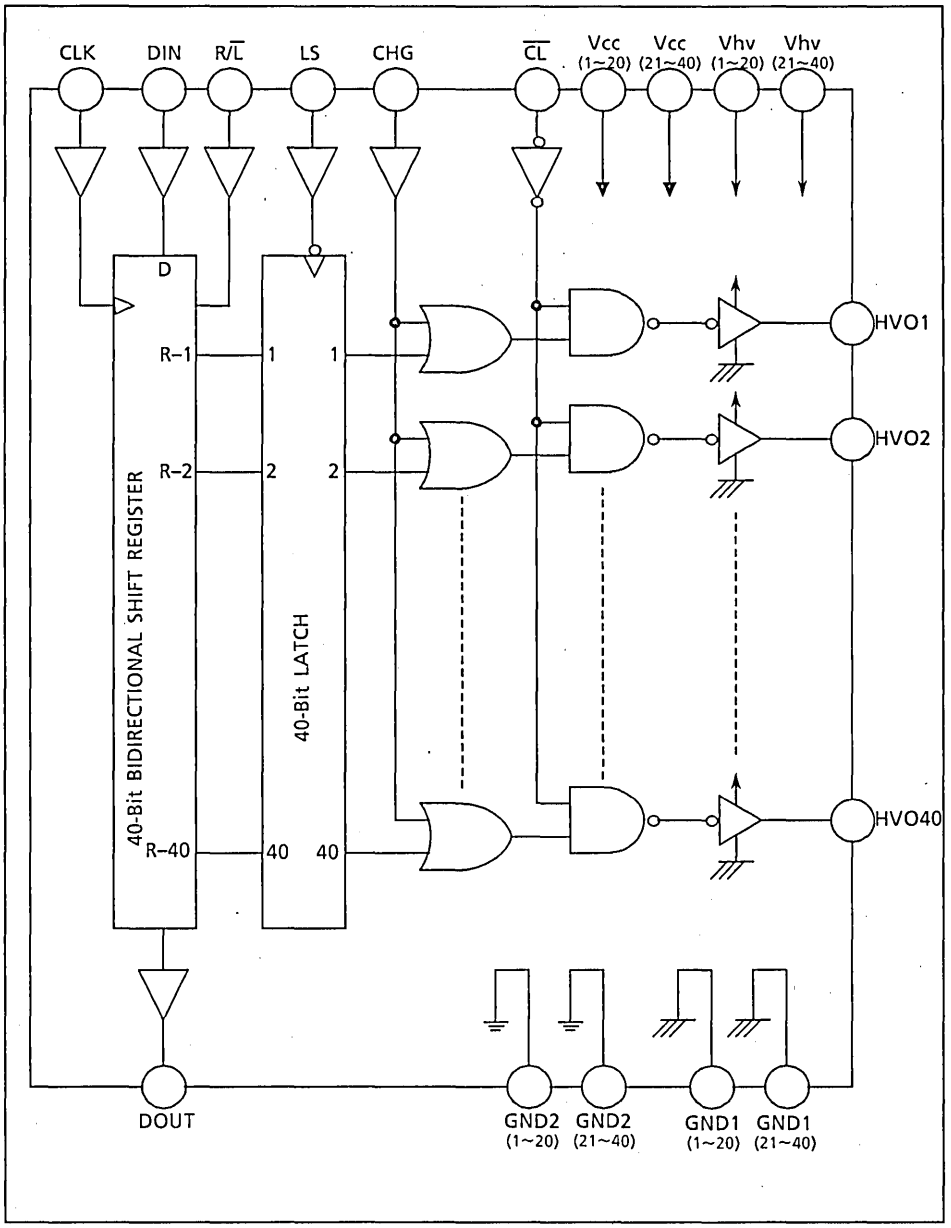
GENERAL DESCRIPTION

The MSC1172 is a monolithic IC using Bi-CMOS process for hybridizing CMOS and bipolar transistors on one chip.
The logic portion such as the input stage, shift register and latch is formed by CMOS, and the output driver requiring a high withstand voltage is formed by bipolar transistors.
Since the pin assigment allows single side pattern formation on the printed circuit board, the display unit size can be reduced.
The bidirectional shift register facilitates the pattern design when the devices are arranged symmetrically with the display at the center axis.

FEATURES

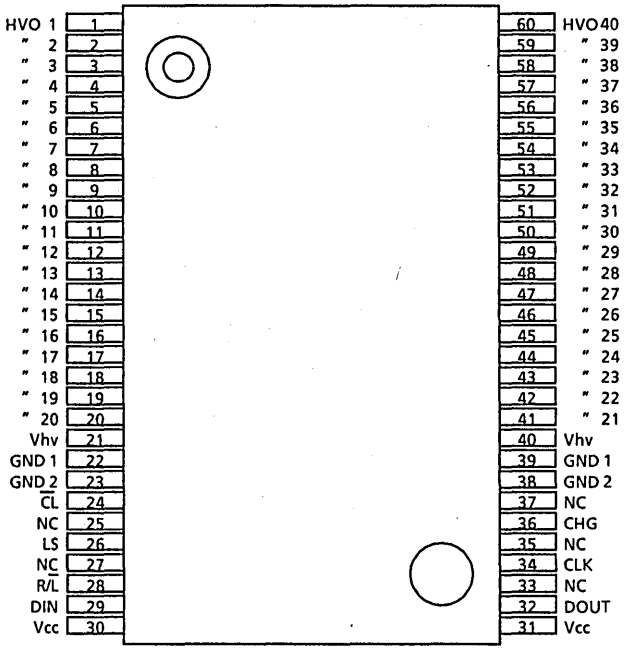
- Logic supply voltage (V_{CC}) : +5 V
- Driver supply voltage (V_{hv}) : +70 V
- Driver output current
  (I_{ohvh1}) : −40 mA (1 driver output high)
  (I_{ohvh2}) : −2 mA (All driver output high)
  (I_{ohvl}) : +2 mA
- Clock frequency : 4 MHz
- Built-in 40-Bit latch
- Built-in 40-Bit bidirectional shift register
- 60 Pin FLAT Package

BLOCK DIAGRAM



PIN CONFIGURATION

(Top View) 60 Lead Plastic Flat Package



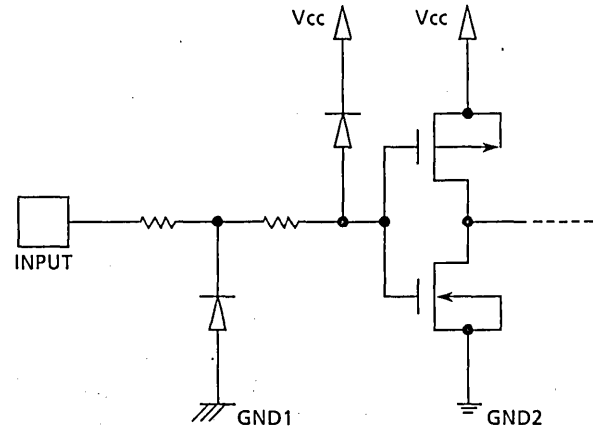
PIN DESCRIPTION

Pin No.	Symbol	Name	Description
1~20 41~60	HV0 1 \ HVO 40	Driver output	1. Each terminal is a driver output terminal, which corresponds to each bit of the shift register. 2. Each terminal can be connected directly to the VF tube grid or anode terminal.
21 41	Vhv	Driver supply voltage	1. This is a power terminal of the driver circuit. 2. Pins 21 and 40 are not connected inside the IC. Connect them outside the IC.
22 39	GND 1	Driver GND	1. This is a grounding terminal of the driver circuit. 2. Pins 22 and 39 are not connected inside the IC. Connect them outside the IC.
23 38	GND 2	Logic GND	1. This is a grounding terminal of the logic portion (other than the driver circuit). 2. Pins 23 and 38 are not connected inside the IC. Connect them outside the IC.
24	$\overline{CL}$	Clear input	1. This is an input terminal containing a pull-up resistor. 2. The terminal is generally kept high. The driver output, High or Low, is driven by the output of the corresponding latch circuit. 3. When the terminal is Low, the driver outputs are fixed to "Low" regardless of the output of the latch circuit.
26	LS	Latch strobe input	1. This is an input terminal without a pull-up or pull-down resistor. 2. When the terminal is High, the latch circuit is slowed, and the output of the shift register is that of the latch circuit. 3. When the terminal is Low, the latch circuit holds the output of the shift register immediately before the terminal is turned Low.
28	R/$\overline{L}$	Shift direction control input	1. This is an input terminal containing a pull-up resistor. 2. This terminal is generally kept High. The bidirectional shift register transfers data from R-1 to R-40. 3. When the terminal is made Low, the bidirectional shift register transfers data from R-40 to R-1.
29	DIN	Data input	1. This is an input terminal without a pull-up or pull-down resistor. 2. The is an input terminal of the shift register to input the display data in synchronization with a clock pulse. (Positive logic)

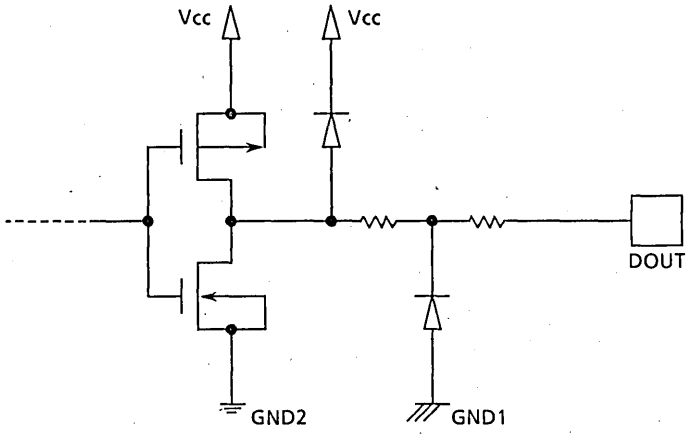
Pin No.	Symbol	Name	Description
30 31	Vcc	Logic supply voltage	1. This is a power terminal of the logic portion (other than the driver circuit). 2. The terminal is used at 4.5 to 5.5 V.
32	DOUT	Data output	1. This is a serial-out output terminal of the shift register. 2. When the R/$\overline{C}$ terminal is High, the terminal outputs the output of the shift register R-40. When the R/$\overline{C}$ terminal is Low, the terminal outputs the output of the shift register R-1.
34	CLK	Clock input	1. This is an input terminal without a pull-up or pull-down resistor. 2. The data of the shift register is shifted at the rising edge of a clock pulse.
36	CHG	Test input	1. This is an input terminal containing a pull-down resistor. 2. The terminal is generally kept Low. When the $\overline{CL}$ terminal is High, the driver output, High or Low, is driven by the output of the corresponding latch circuit. 3. The terminal is Low and the $\overline{CL}$ terminal is High, the driver output can be fixed to "High" regardless of the output of the latch circuit.

SCHEMATIC DIAGRAMS OF LOGIC PORTION INPUT AND OUTPUT TERMINAL CIRCUITS

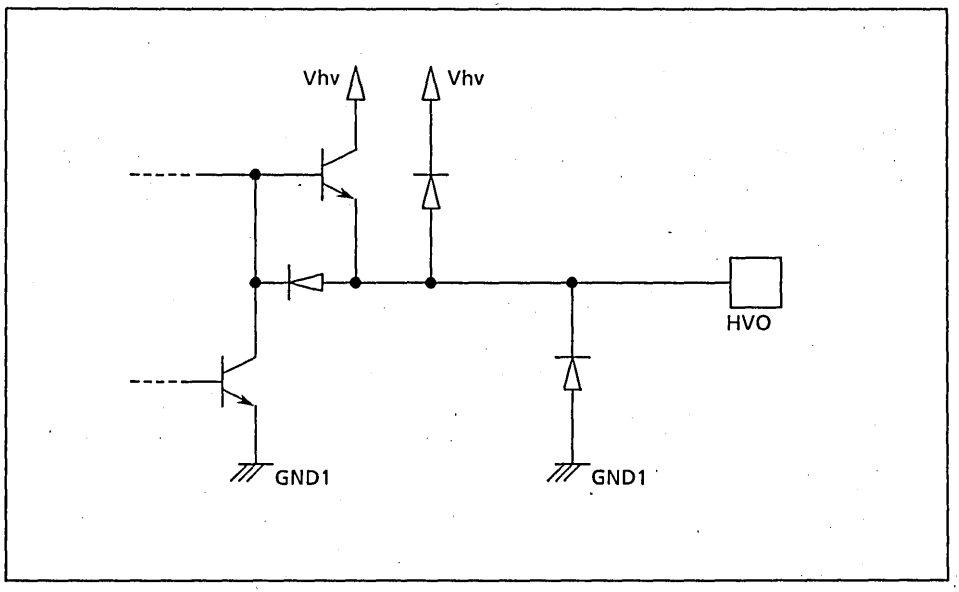
Input terminal



Output terminal



SCHEMATIC DIAGRAM OF DRIVER OUTPUT TERMINAL CIRCUIT



FUNCTION TABLE

CLK	R/$\overline{L}$	DIN	R-1	R-2	R-3	R-4	.....	R-40	DOUT
↗	H	H	H	R1n	R2n	R3n		R39n	R39n
↗	H	L	L	R1n	R2n	R3n		R39n	R39n
↗	L	H	R2n	R3n	R4n	R5n		H	R2n
↗	L	L	R2n	R3n	R4n	R5n		L	R2n

$\overline{CL}$	CHG	LS	R.X	HVO.X
L	X	X	X	L
H	H	X	X	H
H	L	H	H	H
H	L	H	L	L
H	L	L	X	NC

L: Low Level, H: High Level, X: Don't Care, NC: No Change

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limits	Unit	Note
Logic Power Supply	V_{CC}	Applicable to logic power terminal	−0.3~6.5	V	1
Driver Power Supply	V_{HV}	Applicable to driver power terminal	V_{CC}~75	V	1.2
Input voltage	V_{IN}	Applicable to all input terminals	−0.3~V_{CC} + 0.3	V	1
Data output voltage	Vod	Applicable to data output terminal	−0.3~V_{CC} + 0.3	V	1
Driver output voltage	Vohv	Applicable to all driver terminals	−0.3~V_{HV} + 0.3	V	1
Power Dissipation	Pd	Ta≦25°C	860 [Delete 6.9 mw/°C above 25°C]	mW	—
Attenuation Rate	Rj-a	Ta>25°C	145	°C/W	2
Operating temperature	Top	V_{HV}≦70V	−40~+85	°C	—
Storage temperature	Tstg	—	−55~+150	°C	—

Note 1: Maximum Supply Voltage for GND.

Note 2: Delete 6.9 mw/°C above 25°C.
Refer to the following formula.
Tj = P × Rj − a + Ta (P: Maximum power consumption)

• Recommended Operating Conditions

Parameter	Symbol	Condition		MIN	MAX	Unit
Logic supply voltage	V_{CC}	Applicable to logic power terminal		4.5	5.5	V
Driver supply voltage	V_{HV}	Applicable to driver power terminal		10	70	V
High level input voltage	V_{IH}	Applicable to all input terminals	V_{CC} = 4.5V	3.6	—	V
			V_{CC} = 5.5V	4.4	—	
Low level input voltage	V_{IL}	Applicable to all input terminals	V_{CC} = 4.5V	—	0.9	V
			V_{CC} = 5.5V	—	1.1	
Driver high level output current	V_{OHVH1} V_{OHVH2}	Applicable to all driver output terminals	1 output High	—	− 40	mA
			All outpts High	—	− 2	
Driver low level output current	V_{OHVL}	Applicable to all driver output terminals		—	2	mA
Clock frequency	fø	See timing chart		—	4	MHz
Clock pulse width	t_{wclk}	See timing chart		75	—	ns
Data setup time	t_{ds}	See timing chart		50	—	ns
Data hold time	t_{dh}	See timing chart		50	—	ns
LS pulse width	t_{wls}	See timing chart		80	—	ns
CLK-LS delay time	t_{dcl}	See timing chart		50	—	ns
LS-CLK delay time	t_{dlc}	See timing chart		0	—	ns
LS-CHG delay time	t_{dlcg}	See timing chart		0	—	µs
LS-CL delay time	t_{dlcl}	See timing chart		0	—	µs
CHG pulse width	t_{wchg}	See timing chart		2	—	µs
CL pulse width	t_{wcl}	See timing chart		2	—	µs
Operating temperature	t_{op}			− 40	+ 85	°C

• DC Characteristics

V_{CC} = 5V ± 10%, V_{HV} = 10~70V, Ta = −40°C~ +85°C

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Logic supply current	I_{CC1}	No load V_{CC} = 5.5V	All inputs: Low	—	3.98	7.08	μA
	I_{CC2}		All inputs: High All driver outputs: High Ta = 25°C	—	0.5	1.0	
Driver supply current	I_{HV1}	No load V_{CC} = 5.5V	All driver outputs: Low	—	—	1.0	μA
	I_{HV2}		All driver outputs: High Ta = 25°C	—	2.31	4.22	mA
High level input voltage	V_{IH}	V_{CC} = 4.5V	All input terminals	3.15	—	—	V
		V_{CC} = 5.5V		3.85	—	—	V
Low level input voltage	V_{IL}	V_{CC} = 4.5V	All input terminals	—	—	1.35	V
		V_{CC} = 5.5V		—	—	1.65	V
High level input current	I_{IH1}	V_{IN} = V_{CC}	Input terminals except the CHG terminal	—	—	1.0	μA
	I_{IH2}		CHG terminal	10	—	80	
Low level input current	I_{IL1}	V_{IN} = GND	LS, DIN, CLK, CHG terminals	—	—	1.0	μA
	I_{IL2}		$\overline{CL}$, R/$\overline{L}$ terminals	−80	—	−10	
Input capacitance	C_{IN}	Ta = 25°C	All input terminals	—	15	—	pF
High level data output voltage	V_{ODH}	I_O = −0.1mA	V_{CC} = 4.5V	3.5	—	—	V
			V_{CC} = 5.5V	4.5	—	—	
Low level data output voltage	V_{ODL}	I_O = 0.1mA	V_{CC} = 4.5V	—	—	0.9	V
			V_{CC} = 5.5V	—	—	1.1	
High level driver output voltage	V_{OHVH}	I_{OHV} = −40mA		V_{HV} − 40	—	—	V
Low level driver output voltage	V_{OHVL}	I_{OHV} = 2mA		—	—	3.0	V

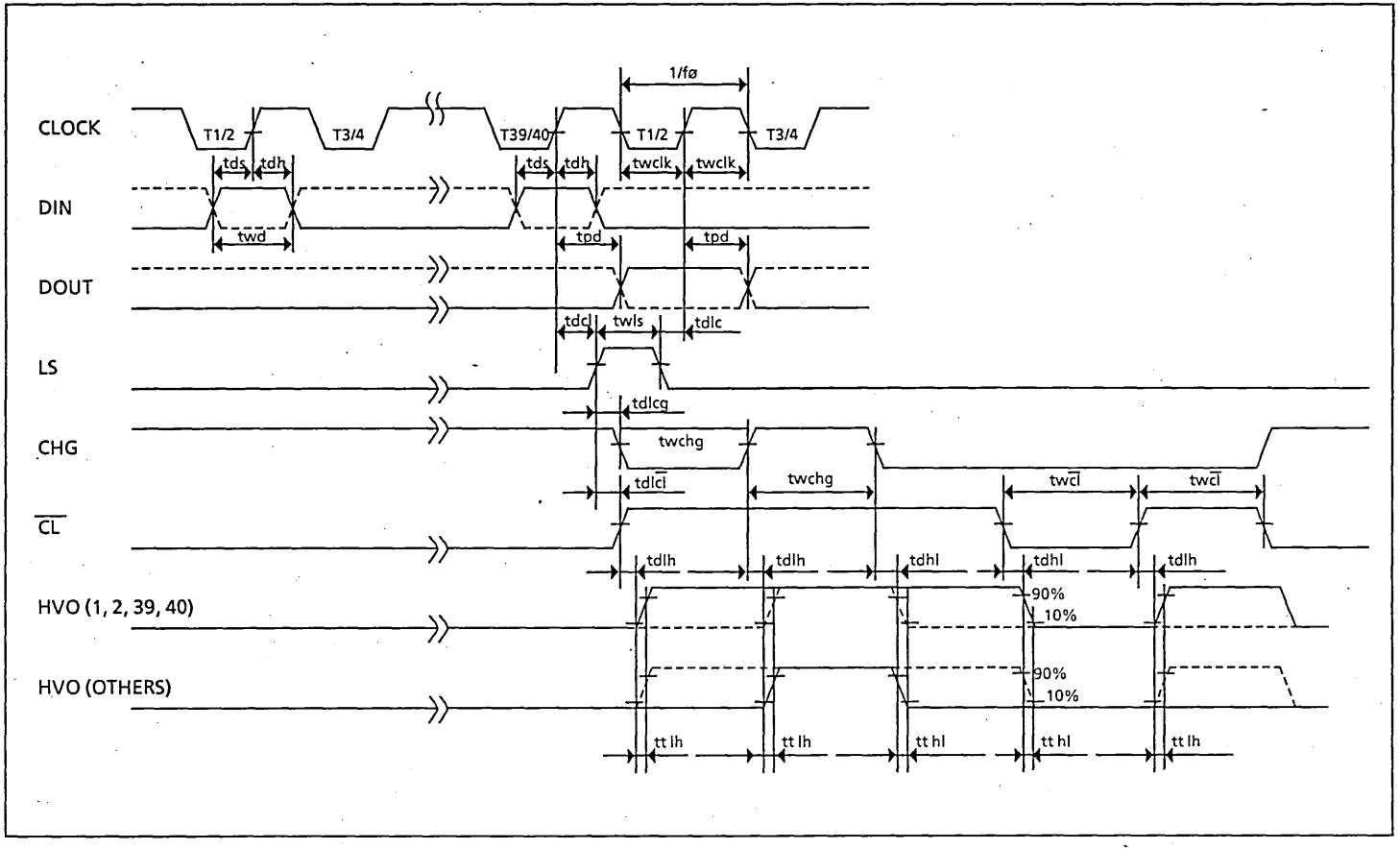
• AC Characteristics

V_{CC} = 5V, V_{HV} = 130V Ta = 25°C

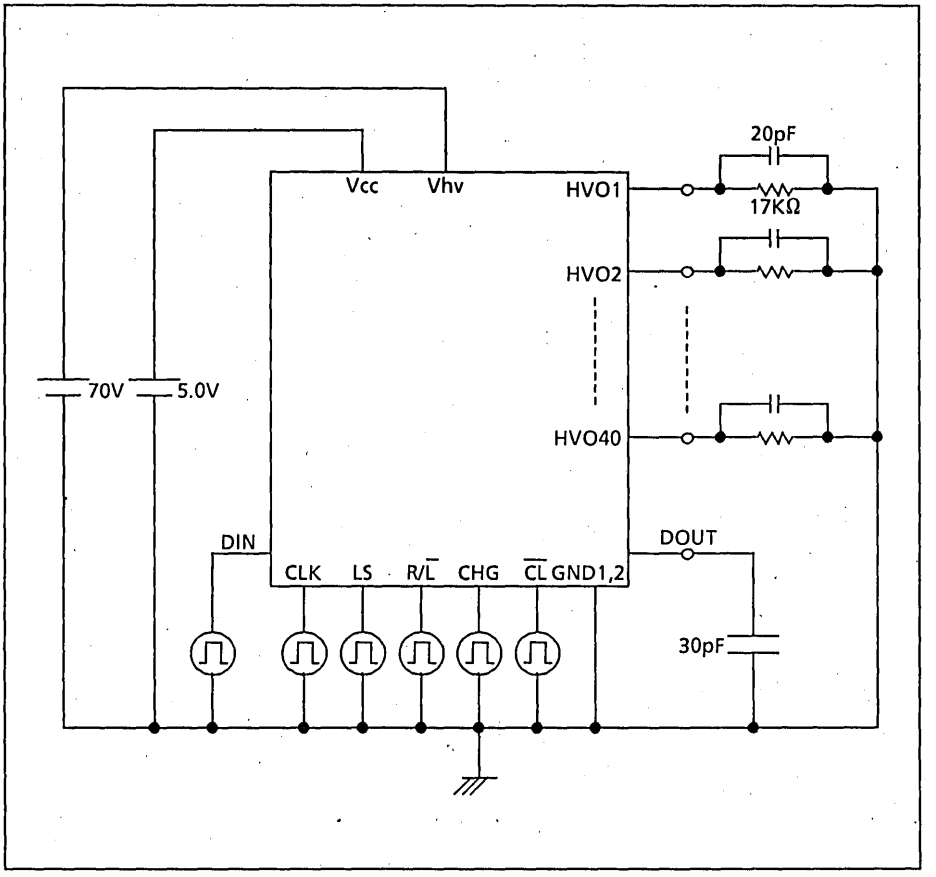
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Note
CLK-DOUT delay time	t_{pd}	See timing chart and test circuit.	—	100	150	ns	4
Delay time: L-H	t_{dlh}	See timing chart and test circuit.	—	0.3	1.0	µs	5.6
Transit time: L-H	t_{tlh}	See timing chart and test circuit.	—	2.0	5.0	µs	5
Delay time: H-L	t_{dhl}	See timing chart and test circuit.	—	0.3	1.0	µs	5.6
Transit time: H-L	t_{thl}	See timing chart and test circuit.	—	2.0	5.0	µs	5

Note 4: Applicable to data output terminal.
Note 5: Applicable to driver output terminal.
Note 6: T_{dlh} and T_{dhl} are delay times from the CL signal.

o Timing Chart



TEST CIRCUIT



OKI semiconductor
MSC1149-XX
DOT DRIVER

GENERAL DESCRIPTION

The MSC1149-XX is a vacuum fluorescent display tube driver IC, which consists of a 34-bit shift register, a 33-bit latch circuit (the 33 bits of the latch circuit correspond to bit 1 to bit 33 of the shift register), and a matrix circuit for latch output and VF driver output.

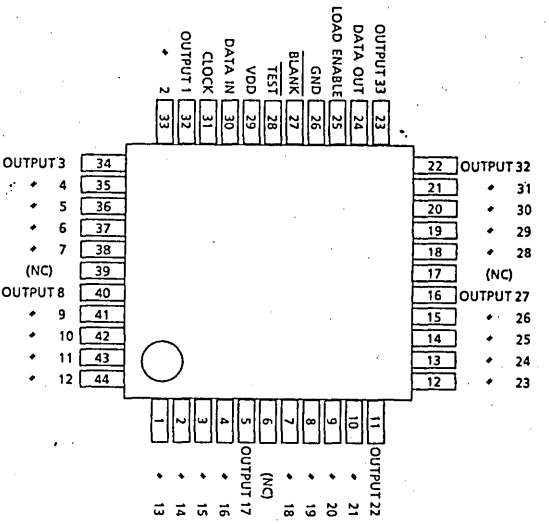
FEATURES

- Power supply voltage: 8V to 18V
- Input: TTL level
- One-to-one correspondence established between latch output and VF driver output by matrix cord
- POWER ON RESET circuit built in
- Latch operation and shift register RESET performed sequentially by LOAD ENABLE signal
  Self load mode generated by connection of LOAD ENABLE terminal and DATA OUT terminal
- Number of bits increased by cascade connection
- VF tube lighting test simplified by all VF outputs on H level via $\overline{\text{TEST}}$ terminal
- 33-bit VF output: – 2 mA for 8 bits, – 0.8 mA for 25 bits Terminal connections

PIN CONFDIGURATION

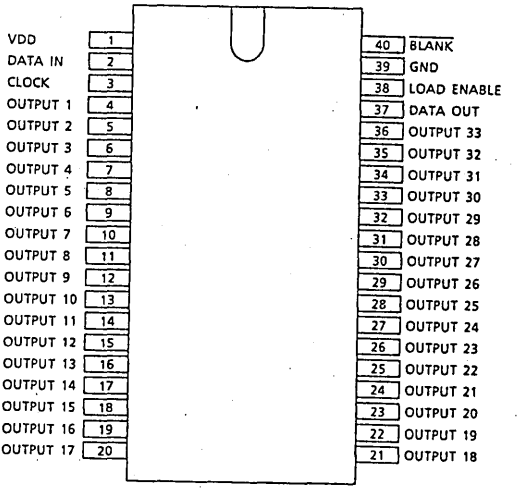
MSC1149-XXGS-VK

(Top View) 44 Lead Plastic Flat Package



MSC1149-XXRS

(Top View) 40 Lead Plastic DIP



PIN DESCRIPTION

(1) DATA IN
This is a serial data input terminal of the 34-stage shift register.

(2) CLOCK
This is a clock input terminal of the shift register to shift an input signal at its leading edge (Low to High).

(3) LOAD ENABLE
This is an input terminal to transfer the data of the shift register to the data latch circuit to hold it. After the data is held, the terminal initializes the data of the shift register. These functions are executed at the leading edge of an input signal.

(4) $\overline{\text{BLANK}}$
This is an input terminal to turn all the OUTPUT terminals OFF (Low), which contains a pull-up resistor.

(5) OUTPUT1 to OUTPUT33
These are output terminals for the VF tube driver. Each terminal outputs data which is transferred from the corresponding bit of the shift register and held in the data latch circuit.

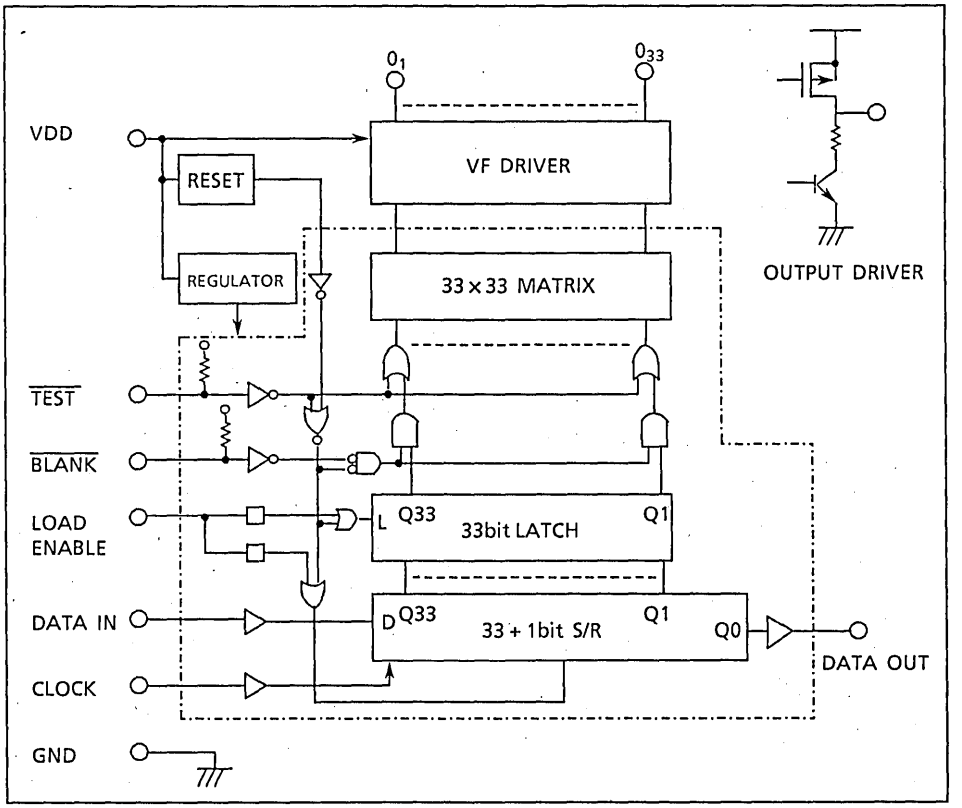
(6) DATA OUT
This is a data output terminal of the shift register to output data on the last stage of the 34-stage shift register.

(7) $\overline{\text{TEST}}$
This is a terminal to turn all the OUTPUT terminals ON (High), which contains a pull-up resistor. The terminal is used for the VF tube lighting test.

(8) V_{DD}
This is a terminal to supply positive potential.

(9) GND
This is a grounding terminal.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit
Power supply voltage	V_{DD}	Ta = 25 °C	− 0.3~2.0	V
Input voltage	V_{IN}	Ta = 25 °C	− 0.3~V_{DD} + 0.3	V
Storage temperature range	Tstg	—	− 65~150	°C

• Operating Conditions

Parameter	Symbol	Range	Unit
Power supply voltage	V_{DD}	8~18	V
Operating temperature range	T_{OP}	− 40~ + 85	°C

• DC Characteristics

V_{DD} = 8~18V Ta = −40~+85°C

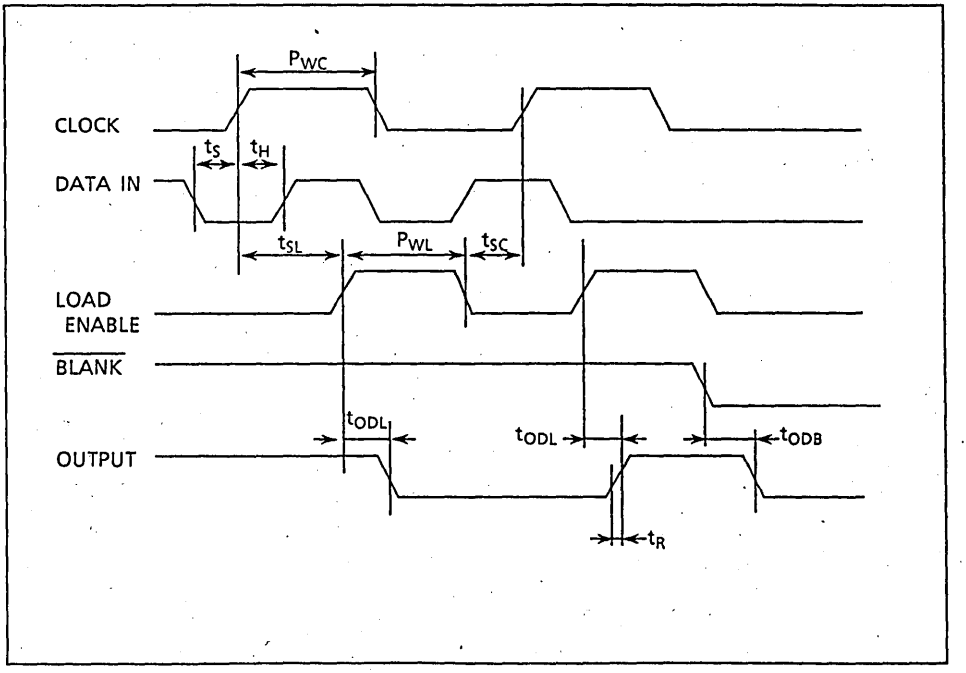
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
High input voltage	V_{IH}	—	3.8	—	6	V
Low input voltage	V_{IL}	—	−0.3	—	0.8	V
High output voltage	V_{OH1}	V_{DD} = 9.5V, I_{OH1} = −2mA OUTPUT14~21	V_{DD} −0.8	—	—	V
High output voltage	V_{OH2}	V_{DD} = 9.5V, I_{OH2} = −0.8mA OUTPUT1~13, 22~33	V_{DD} −0.8	—	—	V
Low output voltage	V_{OL1}	V_{DD} = 9.5V OUTPUT1~33 I_{OL} = 500μA	—	—	2	V
		〃 I_{OL} = 200μA	—	—	1	V
		〃 I_{OL} = 2μA	—	—	0.3	V
High output voltage	V_{OH3}	V_{DD} = 9.5V DATA OUT I_{OH3} = −200μA	4	—	6	V
		〃 No load	4.5	—	6	V
Low output voltage	V_{OL2}	V_{DD} = 9.5V DATA OUT I_{OL} = 200μA	—	—	0.8	μA
High input current	I_{IH1}	CLOCK, DATA IN LOAD V_{IH} = 5.5V	−5	—	5	μA
High input current	I_{IH2}	$\overline{BLANK}$ Ta = 25°C V_{IH} = 5.5V	−20	—	5	μA
Low input current	I_{IL1}	CLOCK, DATA IN LOAD V_{IL} = 0V	−5	—	5	μA
Low input current	I_{IL2}	$\overline{BLANK}$ Ta = 25°C V_{IL} = 0V	−125	—	−10	μA
High input current	I_{IH3}	$\overline{TEST}$ Ta = 25°C V_{IH} = 5.5V	−100	—	5	μA
Low input current	I_{IL3}	$\overline{TEST}$ Ta = 25°C V_{IL} = 0V	−400	—	−20	μA
Operating current	I_{DD}	No load	—	10	15	mA

• AC Characteristics

V_{DD} = 8~18V Ta = −40~+85°C

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Clock frequency	f_C	—	—	—	250	kHz
Clock pulse width	P_{WC}	HIGH pulse	1.3	—	—	µS
Data set up	t_S	—	1	—	—	µS
Data hold time	t_H	—	200	—	—	nS
Load pulse width	P_{WL}	—	1.3	—	—	µS
Output delay time	t_{ODB}	C_L = 100PF BLANK	—	—	7	µS
	t_{ODL}	C_L = 100PF LOAD	—	—	8	µS
Slew rate	t_R	C_L = 100PF 20%~80% of V_{DD}	—	—	5	µS
LOAD ENABLE→CLOCK setup time	t_{SC}	—	2	—	—	µS
CLOCK→LOAD ENABLE setup time	t_{SL}	—	0	—	—	nS

• Timing Chart



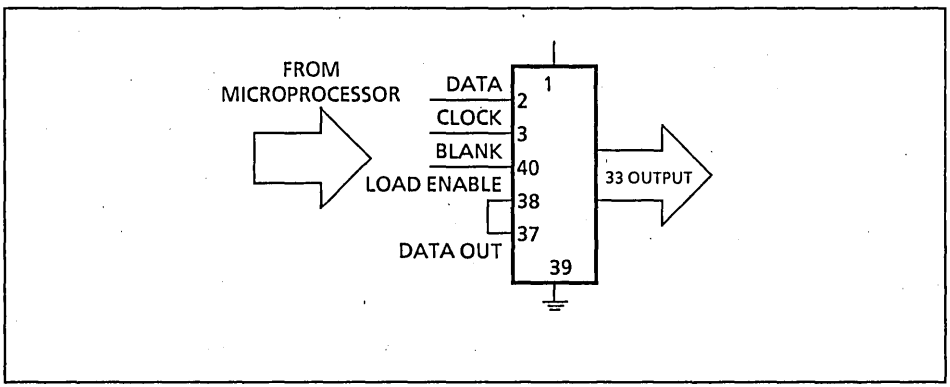
FUNCTIONAL DESCRIPTION

- Shift Register Output Designation

  First data bit read-in is stored in shift register #1, the last data bit read-in is stored in shift register #33. When the shift registers are full, a high voltage level applied to the load enable input will transfer the data from the shift register to the data latch, and then to the output through the 33 x 33 matrix. This matrix determines shift register output designation. the device is mask programmable for the 33 x 33 matrix, thus providing the capability of changing the shift register output designation. The device has 34 shift registers and 33 data latches as shown in the functional block diagram.

- Self-Load Mode

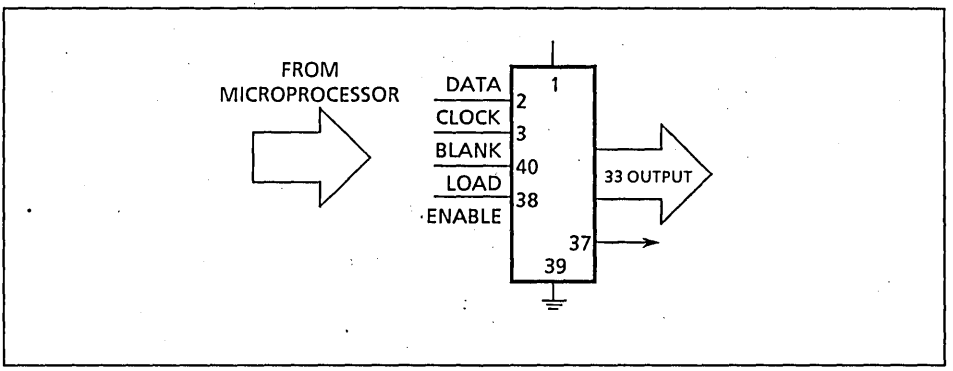
  In this mode data out (pin 4) is connected to load enable (pin 7), and the data word is constructed with 34 bits (including the one self-load bit set to logic 1). At the 34th clock pulse, the data is transferred from the shift register to the data latch and the output drivers through the 33 x 33 matrix. Before the next clock pulse, the registers are zeroed.



- Non-Self-Load Mode

  In this mode, the data out and the load enable pins are not connected, and the load enable input is controlled by an external source. There are two types of operation in this mode.

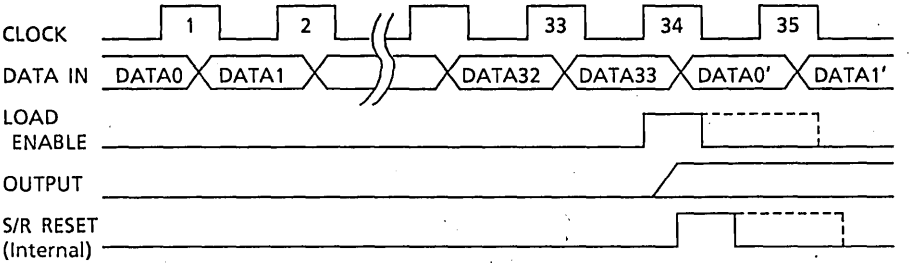
  1. The data word consists of 34 bits (including one self-load bit). To transfer data from the shift registers to the data latch, a high-level voltage is applied to the load enable pin before the rise of the clock pulse following the 34th clock pulse.
  2. The data word consists of 33 bits without the self-load bit. To transfer the data, a high voltage level is applied to the load enable pin before the rise of the 34th clock pulse.



Data load timing example

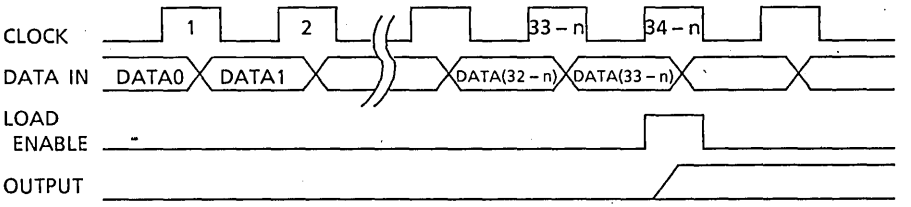
1. LOAD ENABLE singal externally supplied

   1) Bit 1 to Bit 33 used



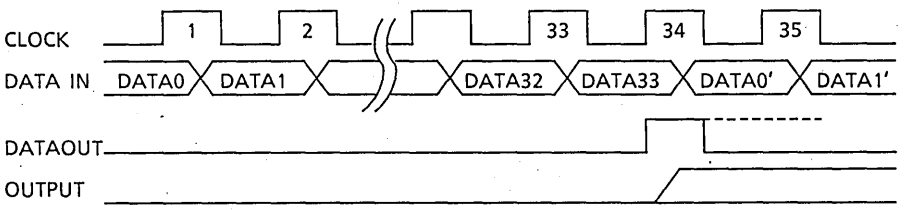
   Notes: 1. The data of DATA0 is negligible.
   2. When the LOAD ENABLE signal is held in the High level state as shown by the dotted line, the shift register is held in the RESET state as shown by the dotted line.

   2) Bit n to Bit 33 used ($1 < n \leqq 33$)



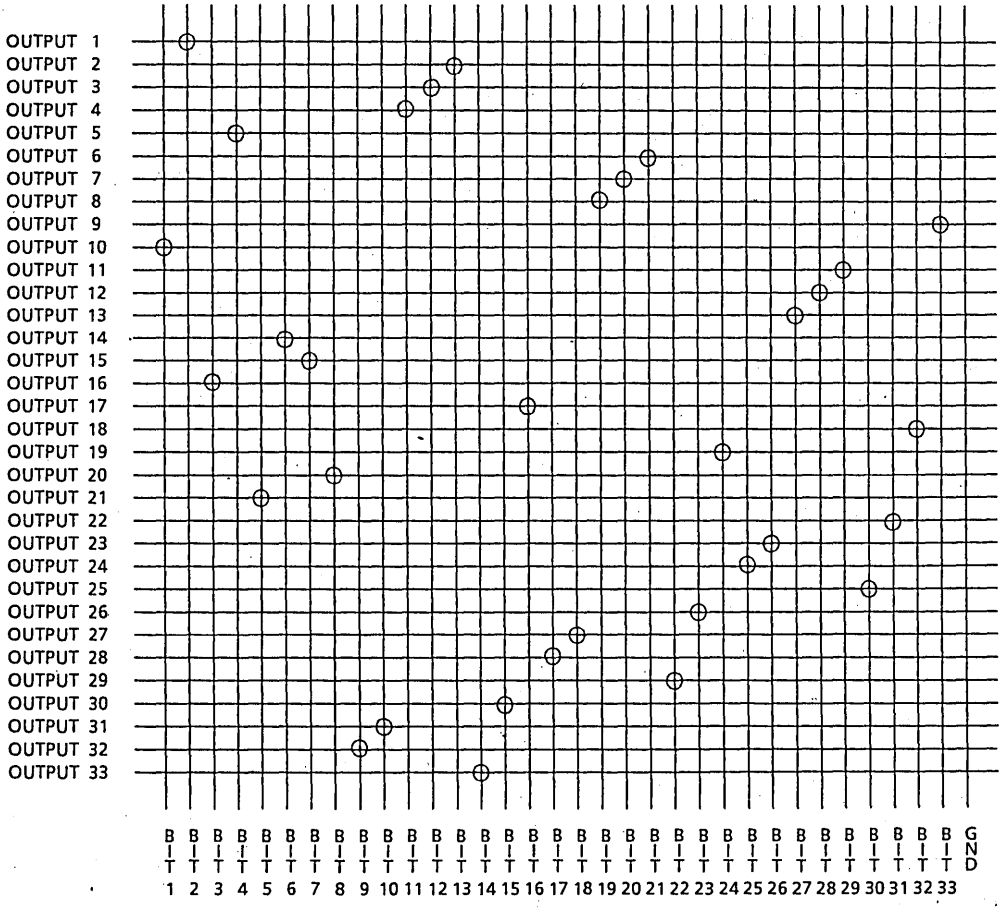
   Notes: 1. The data of DATA0 is the data of Bitn.
   2. The data of Bit1 to Bit(n – 1) goes low.

2. Self LOAD operations (DATA OUT terminal connected to LOAD ENABLE termianl)



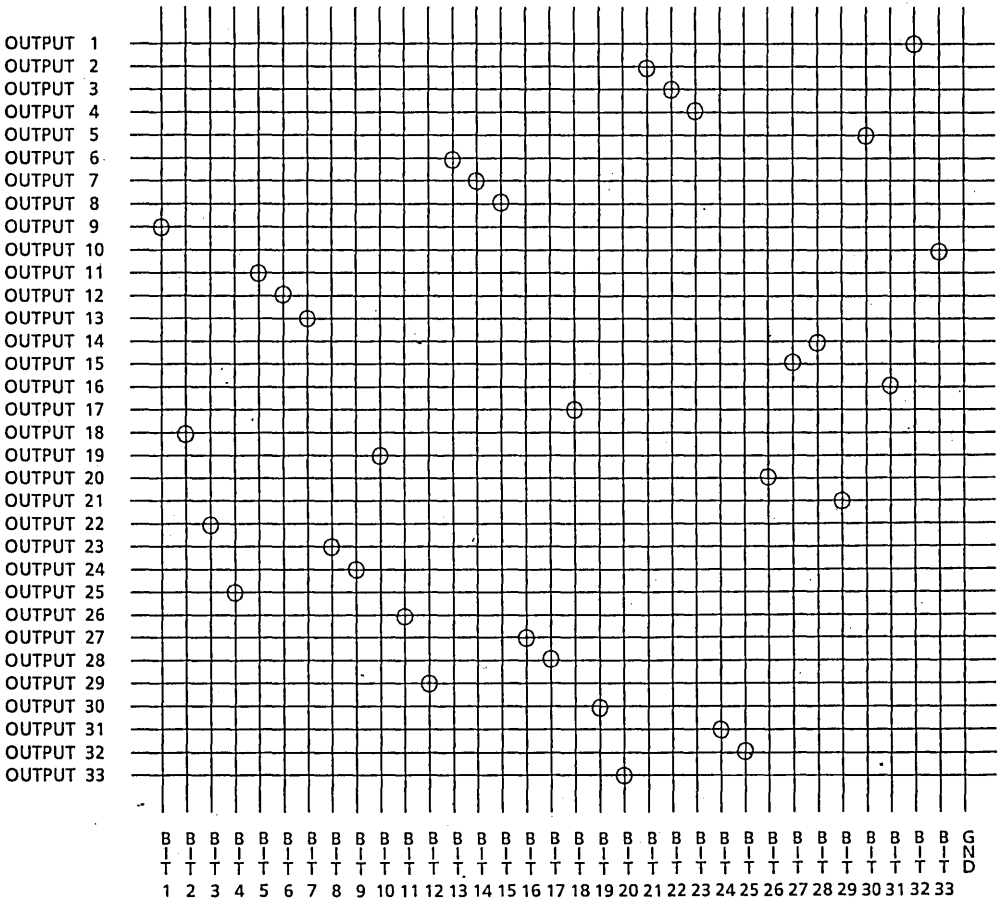
   Notes: 1. Set the data of DATA0 high.
   2. Transfer the data of DATA0 to DATA33 to the shift register.

MSC1149-01 MATRIX
(OUTPUTIN VS LATCH BIT)



PIN NAME	OUT PUT BIT	PIN NAME	OUT PUT BIT	PIN NAME	OUT PUT BIT
OUTPUT 1	BIT 2	OUTPUT 12	BIT 28	OUTPUT 23	BIT 26
OUTPUT 2	BIT 13	OUTPUT 13	BIT 27	OUTPUT 24	BIT 25
OUTPUT 3	BIT 12	OUTPUT 14	BIT 6	OUTPUT 25	BIT 30
OUTPUT 4	BIT 11	OUTPUT 15	BIT 7	OUTPUT 26	BIT 23
OUTPUT 5	BIT 4	OUTPUT 16	BIT 3	OUTPUT 27	BIT 18
OUTPUT 6	BIT 21	OUTPUT 17	BIT 16	OUTPUT 28	BIT 17
OUTPUT 7	BIT 20	OUTPUT 18	BIT 32	OUTPUT 29	BIT 22
OUTPUT 8	BIT 19	OUTPUT 19	BIT 24	OUTPUT 30	BIT 15
OUTPUT 9	BIT 33	OUTPUT 20	BIT 8	OUTPUT 31	BIT 10
OUTPUT 10	BIT 1	OUTPUT 21	BIT 5	OUTPUT 32	BIT 9
OUTPUT 11	BIT 29	OUTPUT 22	BIT 31	OUTPUT 33	BIT 14

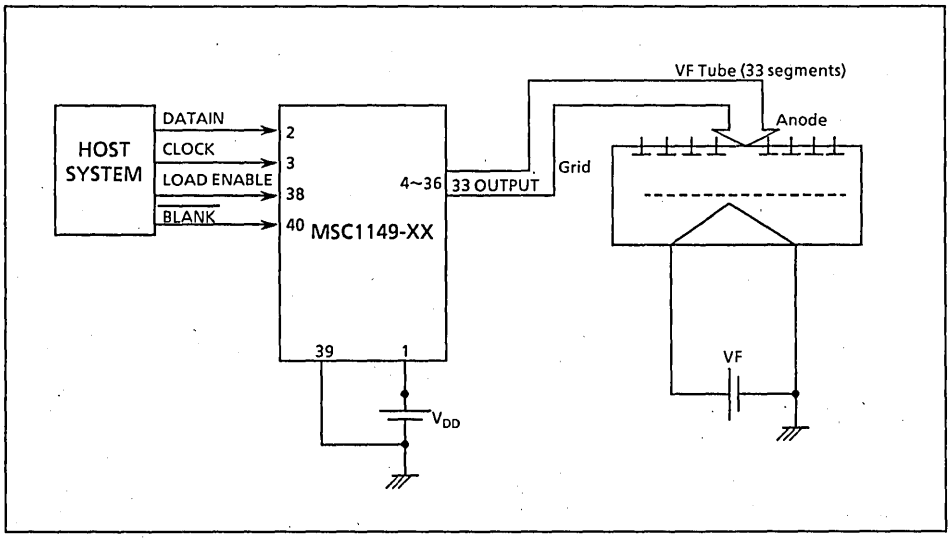
MSC1149-15 MATRIX
(OUTPUTIN VS LATCH BIT)



PIN NAME	OUT PUT BIT	PIN NAME	OUT PUT BIT	PIN NAME	OUT PUT BIT
OUTPUT 1	BIT 32	OUTPUT 12	BIT 6	OUTPUT 23	BIT 8
OUTPUT 2	BIT 21	OUTPUT 13	BIT 7	OUTPUT 24	BIT 9
OUTPUT 3	BIT 22	OUTPUT 14	BIT 28	OUTPUT 25	BIT 4
OUTPUT 4	BIT 23	OUTPUT 15	BIT 27	OUTPUT 26	BIT 11
OUTPUT 5	BIT 30	OUTPUT 16	BIT 31	OUTPUT 27	BIT 16
OUTPUT 6	BIT 13	OUTPUT 17	BIT 18	OUTPUT 28	BIT 17
OUTPUT 7	BIT 14	OUTPUT 18	BIT 2	OUTPUT 29	BIT 12
OUTPUT 8	BIT 15	OUTPUT 19	BIT 10	OUTPUT 30	BIT 19
OUTPUT 9	BIT 1	OUTPUT 20	BIT 26	OUTPUT 31	BIT 24
OUTPUT 10	BIT 33	OUTPUT 21	BIT 29	OUTPUT 32	BIT 25
OUTPUT 11	BIT 5	OUTPUT 22	BIT 3	OUTPUT 33	BIT 20

APPLICATION NOTE

a) Single



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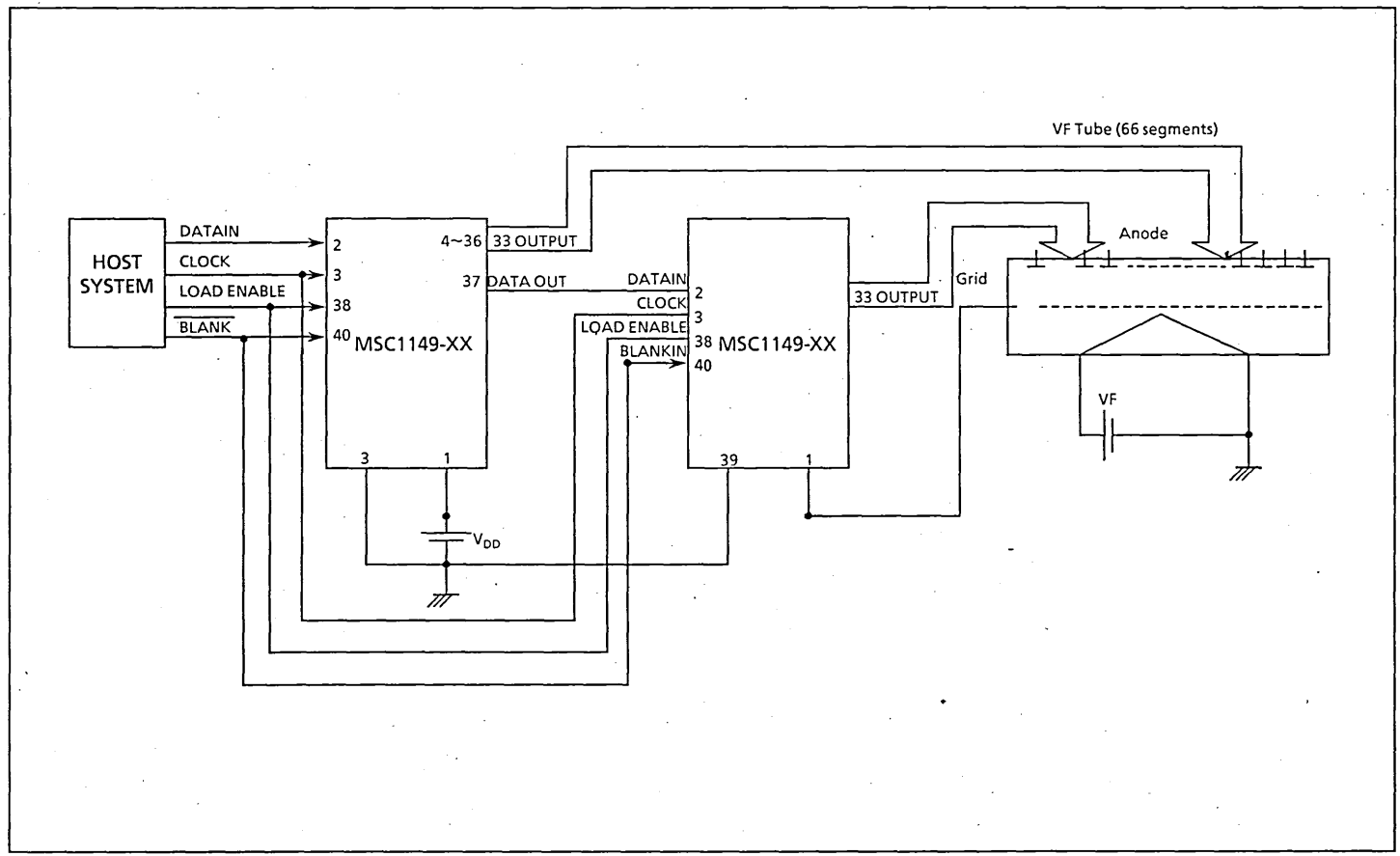
b) Cascading


VF Tube (66 segments)
HOST SYSTEM
DATAIN
CLOCK
LOAD ENABLE
BLANK
2
3
38
40
MSC1149-XX
4~36
33 OUTPUT
37
DATA OUT
DATAIN
CLOCK
LOAD ENABLE
BLANKIN
2
3
38
40
MSC1149-XX
33 OUTPUT
Grid
Anode
VF
3
1
39
1
V_{DD}

OKI semiconductor
MSC1187-XX
DOT DRIVER WITH DIMMING FUNCTION

GENERAL DESCRIPTION

The MSC1187-XX is a vacuum fluorescent display tube driver IC using the Bi-CMOS process for integrating CMOS and bipolar transistors on one chip. The CMOS transistors are used in the logic portion including the input stage (except the VD), shift register, and dimming circuit, and the bipolar transistors are used in the regulator, Vref, comparator, and output drivers.

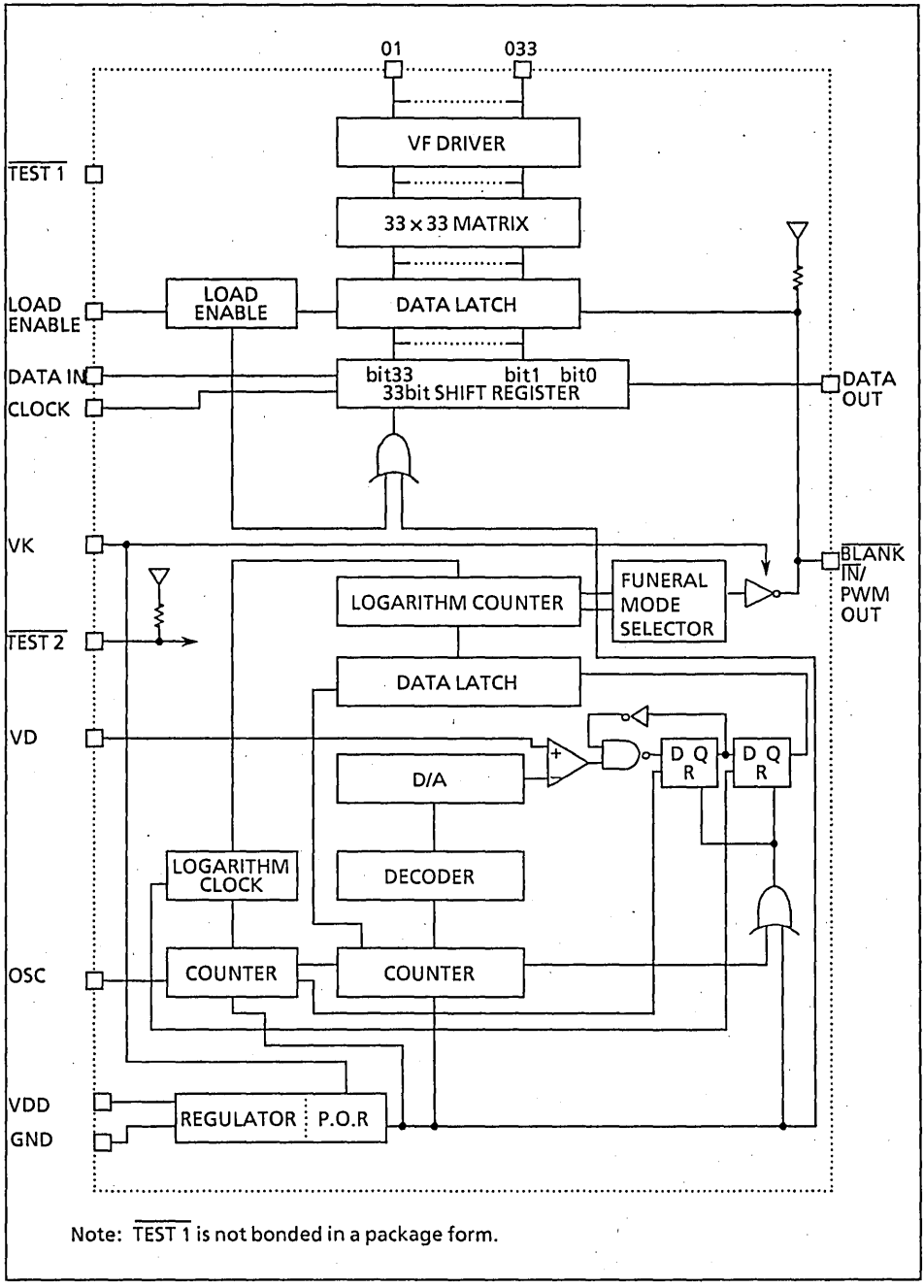
Display data, which is input to the shift register of the MSC1187-XX by DATA IN and CLOCK signals, is transferred to the data latch circuit by a LOAD ENABLE signal and output via the output drivers.

The MSC1187-XX contains a dimming function which accepts an analog voltage to control the duty cycle of the output drivers.

FEATURES

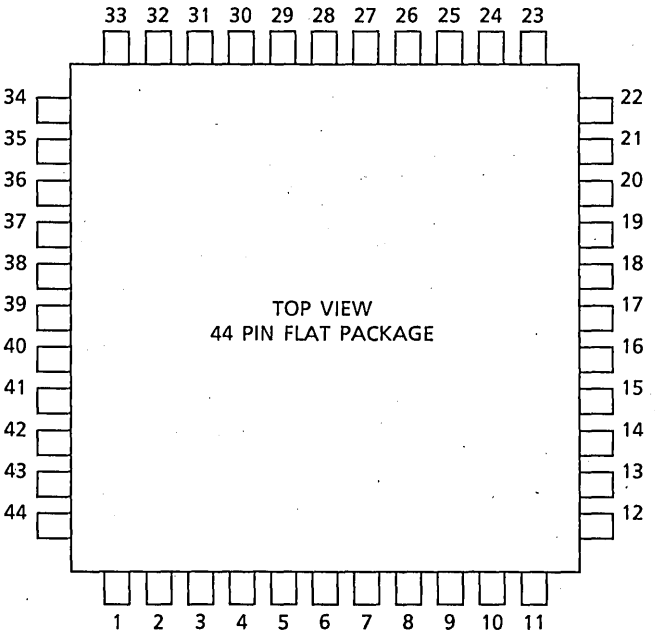
- Supply voltage: 8V to 18V
- Operating temperature range: –40°C to + 85°C
- Up to 52 steps of dimming adjustment, mask-programmable
- Shift register output designation by built-in PLA, mask-programmable
- PWM up to 12.5%, 25% and 50%, mask-programmable
- RC oscillation with external C
- Accepts analog inputs to control dimming.
- 44-pin plastic flat package

BLOCK DIAGRAM



Note: $\overline{\text{TEST 1}}$ is not bonded in a package form.

PIN CONFIGURATION



1	VK input terminal
2	OSC input terminal
3	GND terminal
4	DATA OUT terminal
5	$\overline{\text{BLANK}}$ IN/PWM OUT terminal
6	$\overline{\text{TEST2}}$ input terminal
7	LOAD ENABLE input terminal
8	DATA IN terminal
9	CLOCK input terminal
10	VD input terminal
11	Power supply terminal (8V to 18V)
12	OUTPUT1 terminal
⋮	⋮
44	OUTPUT33 terminal

PIN DESCRIPTION

Terminal No.	Terminal Name	I/O	Function
1	VK	I	This is a dimming function selector terminal. When the terminal is Low, the output duty cycle is 100%. When the terminal is High, the dimming function is performed.
2	OSC	I	This terminal generates an oscillation of 500KHz with an external capacitor of 47pF.
3	GND		This is a GND terminal.
4	DATA OUT	I/O	This terminal outputs the data of bit 0 of the 34-bit shift register. Connecting the terminal to the DATA IN terminal on the next stage provides a cascade connection. Connecting the terminal to the LOAD ENABLE terminal allows the shift register to be latched at the leading edge of the output of the terminal. (Auto load function). In the TEST mode, the terminal functions as an input terminal.
5	$\overline{\text{BLANK IN}}$/ PWM OUT	I/O	When the dimming function is not used, the terminal receives a external BLANK signal and controls the output duty cycle. In the TEST mode, the terminal functions as an output terminal.
6	$\overline{\text{TEST2}}$	I	This terminal is used to select TEST MODE.
7	LOAD ENABLE	I	This is a load signal input terminal to latch the data of the shift register. When the terminal is High, the data of the shift register is loaded into the latch circuit, then the register is reset to 0.
8	DATA IN	I	This is a data input terminal to input data to the shift register. When data is High, the output is ON. When data is Low, the output is OFF.
9	CLOCK	I	This is a shift clock input terminal of the shift register. The shift register operates at the leading edge of a shift clock pulse.
10	VD	I	This is an analog voltage input terminal to input the potential to specify the output duty cycle.
11	VDD		Power supply terminal.
12 ~ 24	OUTPUT1 ~ OUTPUT13	O	These terminals are low current output terminals.
25 ~ 32	OUTPUT14 ~ OUTPUT21	O	These terminals are high current output terminals.
33 ~ 44	OUTPUT22 ~ OUTPUT33	O	These terminals are low current output terminals.

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{DD}	– 0.3 to 20	V
Input Voltage	V_{IN}	– 0.3 to VDD + 0.3	V
Operating Temperature Range	T_{OP}	– 40 to 85	°C
Storage Temperature Range	Tstg	– 65 to 150	°C

• Operating Condition

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		8		18	V
High Level Input Voltage	V_{IH}		3.8		6	V
Low Level Input Voltage	V_{IL}		0		0.8	V
Clock Frequency	fc				250	KHz
OSC Frequency	fosc			512		KHz

• DC CHARACTERISTICS

Ta = −40 to 85°C, V_{DD} = 8 TO 18V unless otherwise noted.
All voltages are referenced to GND.

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
High Level Input Voltage (All Inputs)	V_{IH}		3.8	6.0	V
Low Level Input Voltage (All Inputs)	V_{IL}		0	0.8	V
High Level Input Current (Clock Data In, Load, VK)	I_{IH1}	V_{IH1} = 5.0V	−5	5	μA
High Level Input Current (Blank)	I_{IH2}	V_{IH2} = 5.0V, Ta = 25°C	−20	10	μA
High Level Input Current (Test 2)	I_{IH3}	V_{IH3} = 5.0V, Ta = 25°C	−100	20	μA
Low Level Input Current (Clock, Data In, Load, VK)	I_{IL1}	V_{IL1} = 0V	−5	5	μA
Low Level Input Current (Blank In)	I_{IL2}	V_{IL2} = 0V, Ta = 25°C	−125	−5	μA
Low Level Input Current (Test 2)	I_{IL3}	V_{IL3} = 0V, Ta = 25°C	−700	−100	μA
Input Leak Current (VD)	I_{LI}	V_I = 0~6V	−5	5	μA
High Level Output Voltage (Low Current Driver)	V_{OH1}	V_{DD} = 9.5V, I_{OH1} = −0.8mA	V_{DD} − 0.8	—	V
High Level Output Voltage (High Current Driver)	V_{OH2}	V_{DD} = 9.5V, I_{OH2} = −2mA	V_{DD} − 0.8	—	V
High Level Output Voltage DATA OUT, PWM OUT	V_{OH3}	V_{DD} = 9.5V, I_{OH3} = −200μA Output Open	4 4.5	6 6	V
Low Level Output Voltage (All Drivers)	V_{OL1}	V_{DD} = 9.5V, I_{OL1} = 500μA I_{OL1} = 200μA I_{OL1} = 2μA	— — —	2 1 0.3	V
Low Level Output Voltage DATA OUT, PWM OUT	V_{OL2}	V_{DD} = 9.5V, I_{OL2} = −200μA	—	0.8	V
Supply Current	I_{DD}	NO LOAD		20	mA

• AC CHARACTERISTICS

Ta = – 40 to 85°C, V_{DD} = 8 TO 18V unless otherwise noted.
All voltages are referenced to GND.

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Clock Frequency	fc		—	250	KHz
Clock Pulse Width	PW_C		1.3	—	µS
Data Set-Up Time	ts		1	—	µS
Data Hold Time	t_H		200	—	nS
Load Pulse Width	PW_L		1.3		µS
Output Delay from Blank	to_{DB}	C_L = 100pF	—	7	µS
Output Delay from Load	to_{DL}	C_L = 100pF	—	8	µS
Slew Rate (All Driver)	tr	C_L = 100pF,t = 20% to 80% or 80% to 20% of V_{DD}	—	5	µS

• DIMMING CHARACTERISTICS

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Comparator Offset Voltage	—	—	—	± 10	mV
D/A Output Voltage Error	—	—	—	± 3	%
Reference Voltage Accuracy	Note 1	—	—	± 6	%

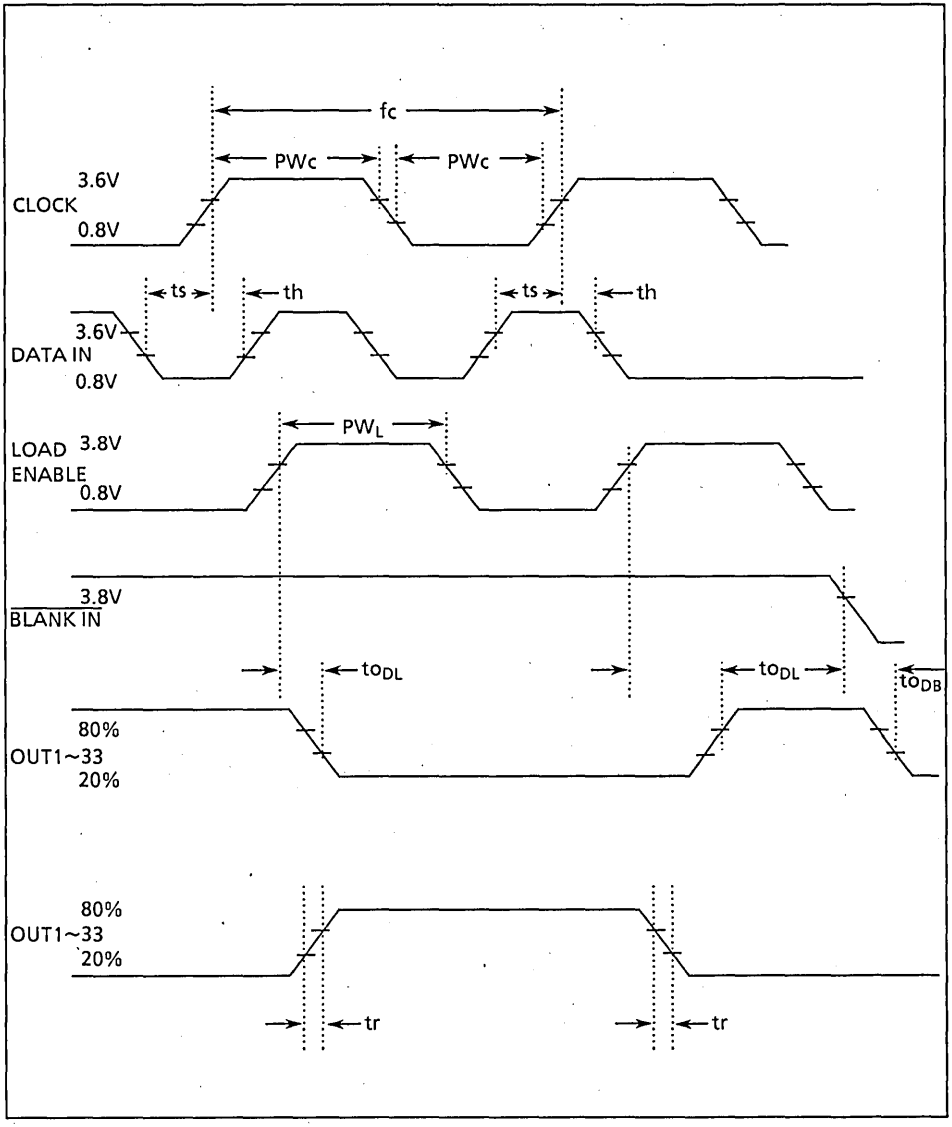
Note 1: Reference Voltage is 6.6V Typical.

AC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Pulse Width Error	No Load, Note 2	—	—	± 100	nsec
PWM OUT Frequency	—	150	250	400	Hz
OSC Frequency	C = 47pF	307.2	512	819.2	KHz

Note 2: Under the ideal condition of DC parameters.

- **Timing Chart**



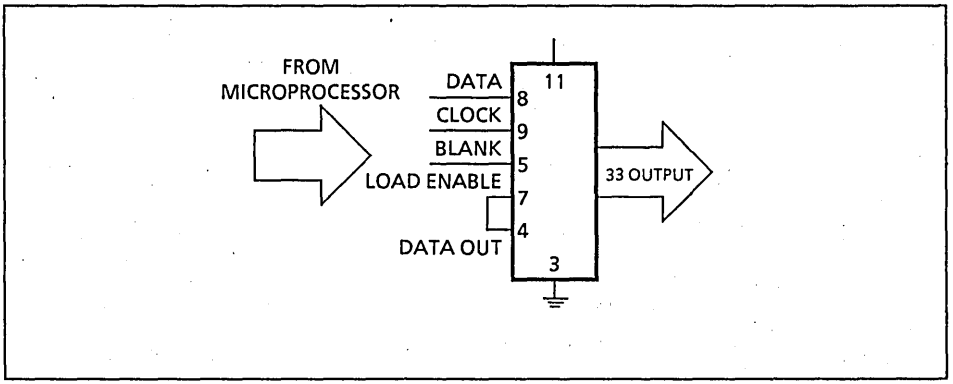
FUNCTIONAL DESCRIPTION

- Shift Register Output Designation

  First data bit read-in is stored in shift register #0, the last data bit read-in is stored in shift register #33. When the shift registers are full, a high voltage level applied to the load enable input will transfer the data from the shift register to the data latch, and then to the output through the 33 x 33 matrix. This matrix determines shift register output designation. the device is mask programmable for the 33 x 33 matrix, thus providing the capability of changing the shift register output designation. The device has 34 shift registers and 33 data latches as shown in the block diagram.

- Self-Load Mode

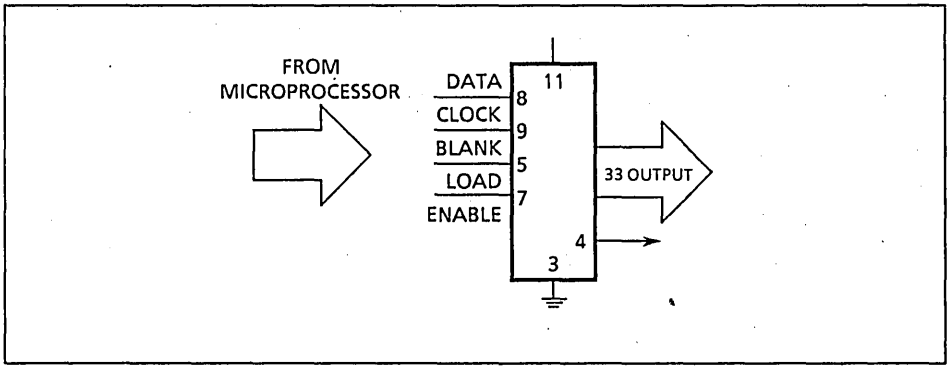
  In this mode data out (pin 4) is connected to load enable (pin 7), and the data word is constructed with 34 bits (including the one self-load bit set to logic 1). At the 34th clock pulse, the data is transferred from the shift register to the data latch and the output drivers through the 33 x 33 matrix. Before the next clock pulse, the registers are zeroed.



- Non-Self-Load Mode

  In this mode, the data out and the load enable pins are not connected, and the load enable input is controlled by an external source. There are two types of operation in this mode.

  1. The data word consists of 34 bits (including one self-load bit). To transfer data from the shift registers to the data latch, a high-level voltage is applied to the load enable pin before the rise of the clock pulse following the 34th clock pulse.
  2. The data word consists of 33 bits without the self-load bit. To transfer the data, a high voltage level is applied to the load enable pin before the rise of the 34th clock pulse.



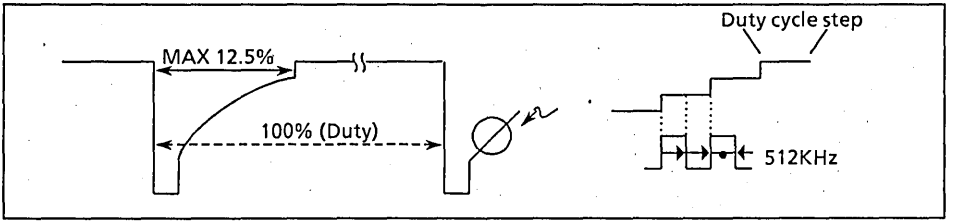
- Dimming function

  When the VK terminal (pin 1) is Low, the BLANK IN/PWM OUT terminal (pin 5) functions as a BLANK signal input terminal, and the output duty cycle is controlled by an external BLANK signal. When the terminal with a built-in pull-up resistor is open, the output duty cycle is 100%.

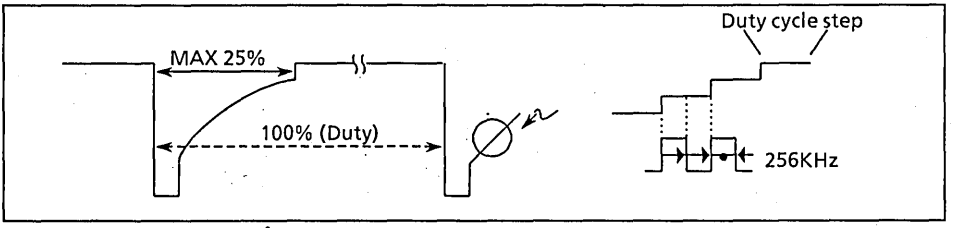
  When the VK terminal is High, the output driver turns ON and OFF repeatedly in the output duty cycle corresponding to the analog voltage which is applied to the VD terminal. The analog voltage vs output duty cycle (dimming curve) is user-programmable under the restrictions indicated below.

1. Select one of the three maximum duty cycles indicated below.

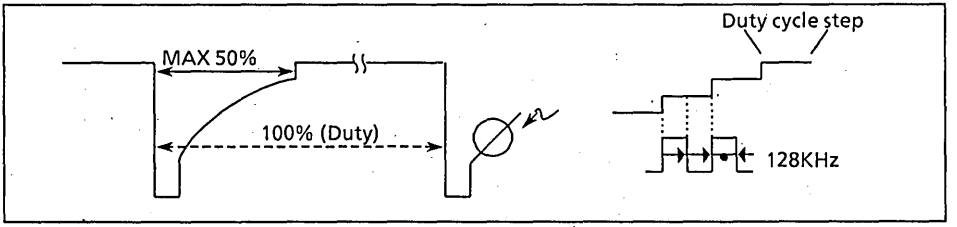
- 12.5%



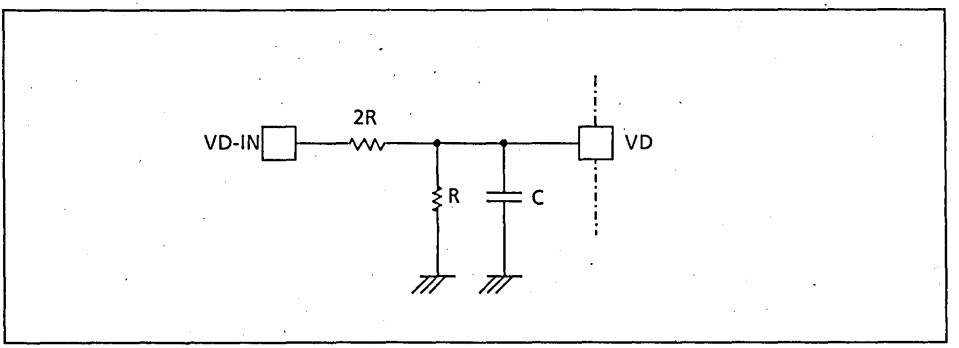
- 25%



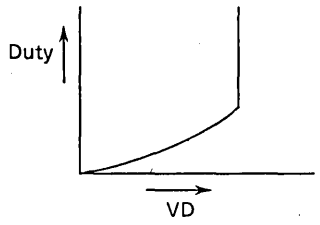
- 50%



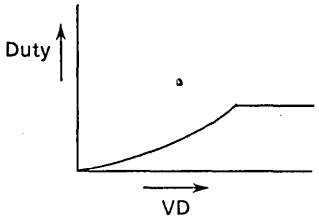
2. The maximum number of duty cycle steps is 52.
3. The VD input voltage should be generally 1/3 VD-IN.



4. Select "Use" or "Non-use" of the funeral mode.



(The funeral mode is used.)



(The funeral mode is not used.)

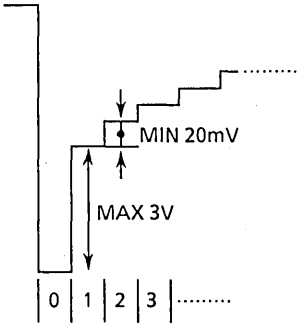
* "Use" or "Non-use" of the funeral mode indicates whether the PWM is set to 100% or not when VD ≧ D/A max. voltage. (When the number of steps is 52 or less, the funeral function is not performed.)

5. Select the initial duty cycle (minimum output width of the PWM when VD = 0V).

Pulse step No.	1	2	3	4	5	6	
Check							
%	0.63	0.68	0.73	0.78	0.83	0.88	(When the maximum duty cycle is 12.5%)
	1.27	1.37	1.46	1.56	1.66	1.76	(When the maximum duty cycle is 25%)
	2.54	2.73	2.93	3.13	3.32	3.52	(When the maximum duty cycle is 50%)

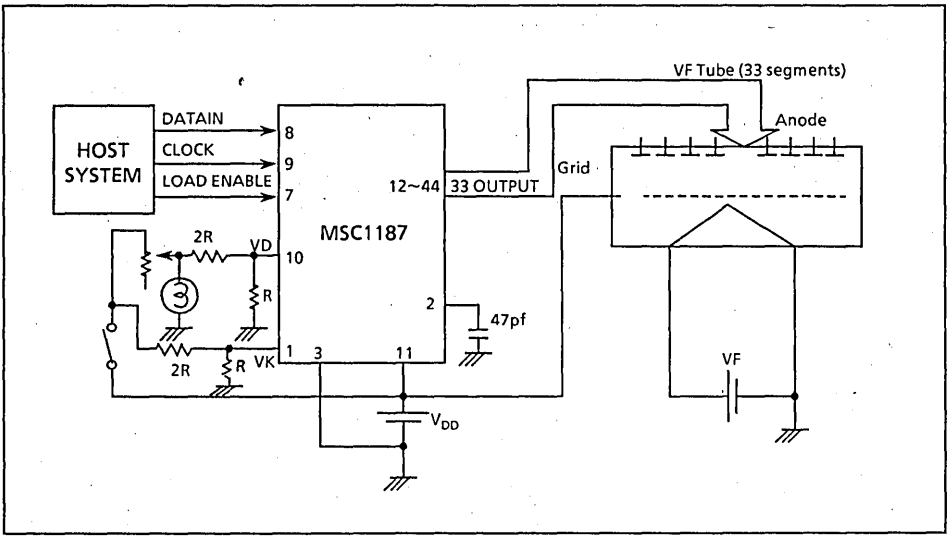
6. The voltage at the maximum step number of the dimming curve should not exceed 5.0V.

7. The minimum voltage at each step of the dimming curve is 20mV. The voltage between pulse step No. 0 and 1 may be programmable from 0V to 3V.

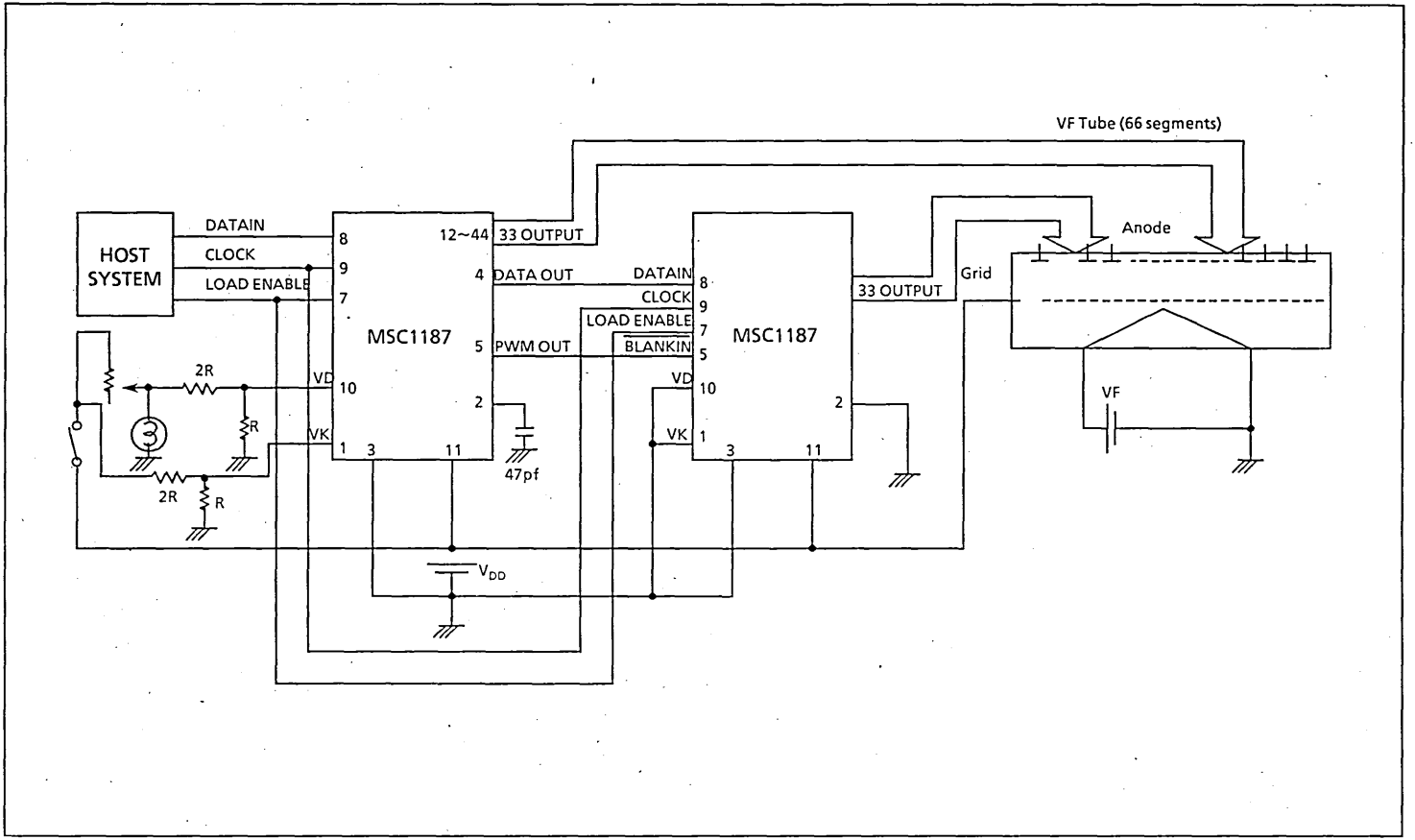


APPLICATION NOTE

a) Single use



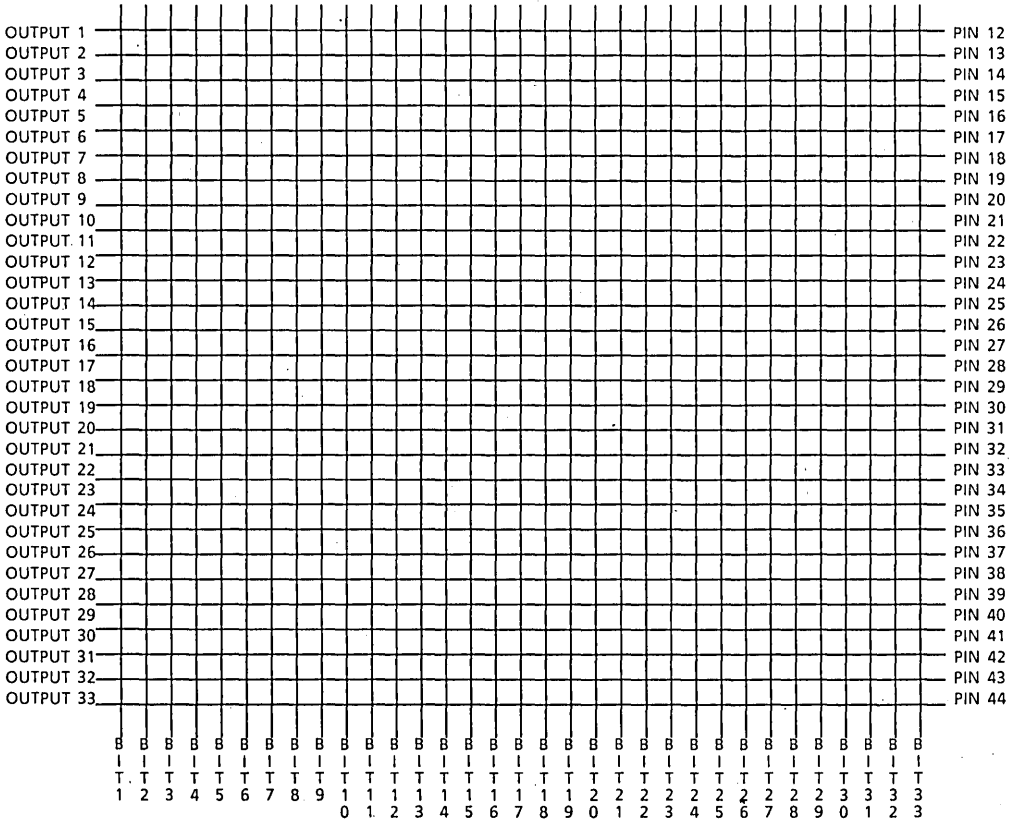
b) Cascading


VF Tube (66 segments)
HOST SYSTEM
DATAIN
CLOCK
LOAD ENABLE
MSC1187
12~44
33 OUTPUT
DATA OUT
PWM OUT
47pf
MSC1187
DATAIN
CLOCK
LOAD ENABLE
BLANKIN
33 OUTPUT
Grid
Anode
VF
2R
R
VD
VK
V_{DD}

Note 1: When placing an order of this IC with OKI, please send the attached dimming curve sheet and PLA code table sheet filled in together with the written order.

Note 2: Values of resistor network connected to VD terminal may be changed after ES evaluation.

MSC1187 - PLA CODE



PIN NAME	OUTPUT BIT	PIN NAME	OUTPUT BIT	PIN NAME	OUTPUT BIT
OUTPUT 1	BIT	OUTPUT 12	BIT	OUTPUT 23	BIT
OUTPUT 2	BIT	OUTPUT 13	BIT	OUTPUT 24	BIT
OUTPUT 3	BIT	OUTPUT 14	BIT	OUTPUT 25	BIT
OUTPUT 4	BIT	OUTPUT 15	BIT	OUTPUT 26	BIT
OUTPUT 5	BIT	OUTPUT 16	BIT	OUTPUT 27	BIT
OUTPUT 6	BIT	OUTPUT 17	BIT	OUTPUT 28	BIT
OUTPUT 7	BIT	OUTPUT 18	BIT	OUTPUT 29	BIT
OUTPUT 8	BIT	OUTPUT 19	BIT	OUTPUT 30	BIT
OUTPUT 9	BIT	OUTPUT 20	BIT	OUTPUT 31	BIT
OUTPUT 10	BIT	OUTPUT 21	BIT	OUTPUT 32	BIT
OUTPUT 11	BIT	OUTPUT 22	BIT	OUTPUT 33	BIT

VD Threshold dimming voltage V.S. PWM duty cycle (Typical Value)

12.5% PWM maximum table

Pulse Step Number	PWM Duty Cycle		Threshold Voltage	Pulse Step Number	PWM Duty Cycle		Threshold Voltage
	Pulse Count	%			Pulse Count	%	
52	256/2048	12.5		26	56/2048	2.73	
51	240/2048	11.7		25	52/2048	2.54	
50	224/2048	10.9		24	48/2048	2.34	
49	208/2048	10.2		23	46/2048	2.25	
48	192/2048	9.38		22	44/2048	2.15	
47	184/2048	8.98		21	42/2048	2.05	
46	176/2048	8.59		20	40/2048	1.95	
45	168/2048	8.20		19	38/2048	1.86	
44	160/2048	7.81		18	36/2048	1.76	
43	152/2048	7.42		17	34/2048	1.66	
42	144/2048	7.03		16	32/2048	1.56	
41	136/2048	6.64		15	30/2048	1.46	
40	128/2048	6.25		14	28/2048	1.37	
39	120/2048	5.86		13	26/2048	1.27	
38	112/2048	5.47		12	24/2048	1.17	
37	104/2048	5.08		11	23/2048	1.12	
36	96/2048	4.69		10	22/2048	1.07	
35	92/2048	4.49		9	21/2048	1.03	
34	88/2048	4.30		8	20/2048	0.98	
33	84/2048	4.10		7	19/2048	0.93	
32	80/2048	3.91		6	18/2048	0.88	
31	76/2048	3.71		5	17/2048	0.83	
30	72/2048	3.52		4	16/2048	0.78	
29	68/2048	3.32		3	15/2048	0.73	
28	64/2048	3.12		2	14/2048	0.68	
27	60/2048	2.93		1	13/2048	0.63	
							0.000

Note: VD input voltage must not exceed the Vref voltage.

VD Threshold dimming voltage V.S. PWM duty cycle (Typical Value)

25% PWM maximum table

Pulse Step Number	PWM Duty Cycle		Threshold Voltage	Pulse Step Number	PWM Duty Cycle		Threshold Voltage
	Pulse Count	%			Pulse Count	%	
52	256/1024	25.0		26	56/1024	5.47	
51	240/1024	23.4		25	52/1024	5.08	
50	224/1024	21.9		24	48/1024	4.69	
49	208/1024	20.3		23	46/1024	4.49	
48	192/1024	18.8		22	44/1024	4.30	
47	184/1024	18.0		21	42/1024	4.10	
46	176/1024	17.2		20	40/1024	3.91	
45	168/1024	16.4		19	38/1024	3.71	
44	160/1024	15.6		18	36/1024	3.52	
43	152/1024	14.8		17	34/1024	3.32	
42	144/1024	14.1		16	32/1024	3.13	
41	136/1024	13.3		15	30/1024	2.93	
40	128/1024	12.5		14	28/1024	2.73	
39	120/1024	11.7		13	26/1024	2.54	
38	112/1024	10.9		12	24/1024	2.34	
37	104/1024	10.2		11	23/1024	2.25	
36	96/1024	9.38		10	22/1024	2.15	
35	92/1024	8.98		9	21/1024	2.05	
34	88/1024	8.59		8	20/1024	1.95	
33	84/1024	8.20		7	19/1024	1.86	
32	80/1024	7.81		6	18/1024	1.76	
31	76/1024	7.42		5	17/1024	1.66	
30	72/1024	7.03		4	16/1024	1.56	
29	68/1024	6.64		3	15/1024	1.46	
28	64/1024	6.25		2	14/1024	1.37	
27	60/1024	5.86		1	13/1024	1.27	0.000

Note: VD input voltage must not exceed the Vref voltage.

VD Threshold dimming voltage V.S. PWM duty cycle (Typical Value)

50% PWM maximum table

Pulse Step Number	PWM Duty Cycle		Threshold Voltage	Pulse Step Number	PWM Duty Cycle		Threshold Voltage
	Pulse Count	%			Pulse Count	%	
52	256/512	50.0		26	56/512	10.9	
51	240/512	46.9		25	52/512	10.2	
50	224/512	43.8		24	48/512	9.38	
49	208/512	40.6		23	46/512	8.98	
48	192/512	37.5		22	44/512	8.59	
47	184/512	35.9		21	42/512	8.20	
46	176/512	34.4		20	40/512	7.81	
45	168/512	32.8		19	38/512	7.42	
44	160/512	31.3		18	36/512	7.03	
43	152/512	29.7		17	34/512	6.64	
42	144/512	28.1		16	32/512	6.25	
41	136/512	26.6		15	30/512	5.86	
40	128/512	25.0		14	28/512	5.47	
39	120/512	23.4		13	26/512	5.08	
38	112/512	21.9		12	24/512	4.69	
37	104/512	20.3		11	23/512	4.49	
36	96/512	18.8		10	22/512	4.30	
35	92/512	18.0		9	21/512	4.10	
34	88/512	17.2		8	20/512	3.91	
33	84/512	16.4		7	19/512	3.71	
32	80/512	15.6		6	18/512	3.52	
31	76/512	14.8		5	17/512	3.32	
30	72/512	14.1		4	16/512	3.13	
29	68/512	13.3		3	15/512	2.93	
28	64/512	12.5		2	14/512	2.73	
27	60/512	11.7		1	13/512	2.54	
							0.000

Note: VD input voltage must not exceed the Vref voltage.

OKI semiconductor
MSM5267B-15
DOT DRIVER

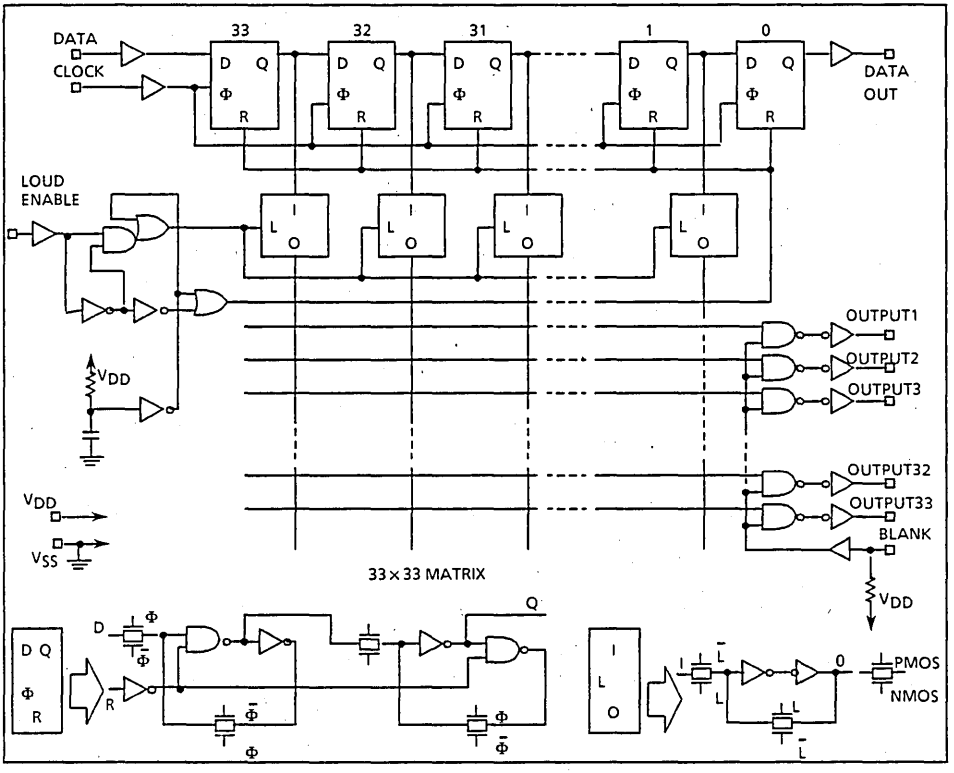
GENERAL DESCRIPTION

The MSM5267B-15 is a CMOS multi-digit display driver and consists of a 34-bit shift register, a 33-bit latch, and a 33-bit VF tube driver.

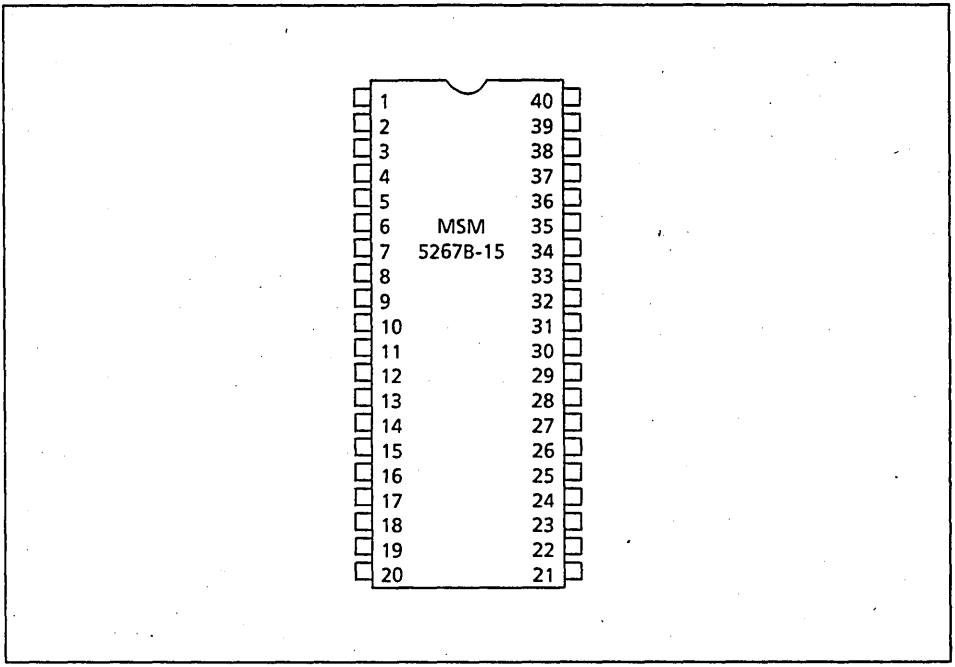
FEATURES

- Complete static operation to ensure stability against noise
- 3 or 4-signal line connection with microcomputers.
- Direct drive of VF tubes (8 outputs of high-current drive, 25 outputs of low-current drive)
- Capability of self-load mode.
- Low power consumption.
- Single power supply and operating voltage range of 8V to 18V

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN#	Pin Name	Comments
1	V_{dd}	Input Positive supply voltage Terminal
2	Data	Input Data Acquisition Terminal
3	Clock	Input Clock Terminal
4	Output 1	Output Shift Register 32
5	Output 2	Output Shift Register 21
6	Out put 3	Output Shift Register 22
7	Output 4	Output Shift Register 23
8	Output 5	Output Shift Register 30
9	Output 6	Output Shift Register 13
10	Output 7	Output Shift Register 14
11	Output 8	Output Shift Register 15
12	Output 9	Output Shift Register 1
13	Output 10	Output Shift Register 33
14	Output 11	Output Shift Register 5

PIN DESCRIPTION

PIN#	Pin Name	Comments
15	Output 12	Output Shift Register 6
16	Output 13	Output Shift Register 7
17	Out put 14	Output Shift Register 28
18	Output 15	Output Shift Register 27
19	Output 16	Output Shift Register 31
20	Output 17	Output Shift Register 18
21	Output 18	Output Shift Register 2
22	Output 19	Output Shift Register 10
23	Output 20	Output Shift Register 26
24	Output 21	Output Shift Register 29
25	Output 22	Output Shift Register 3
26	Output 23	Output Shift Register 8
27	Output 24	Output Shift Register 9
28	Out put 25	Output Shift Register 4
29	Output 26	Output Shift Register 11
30	Output 27	Output Shift Register 16
31	Output 28	Output Shift Register 17
32	Output 29	Output Shift Register 12
33	Output 30	Output Shift Register 19
34	Output 31	Output Shift Register 24
35	Output 32	Output Shift Register 25
36	Output 33	Output Shift Register 20
37	Data Out	Output Data Shift Register
38	Load Enable	Input for Loading Word into Data Latch from Data Shift Register
39	Vss	Ground Potential Terminal
40	Blank	Input for Turning Output Drivers Off

ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Ta = 25°C, Unless otherwise specified

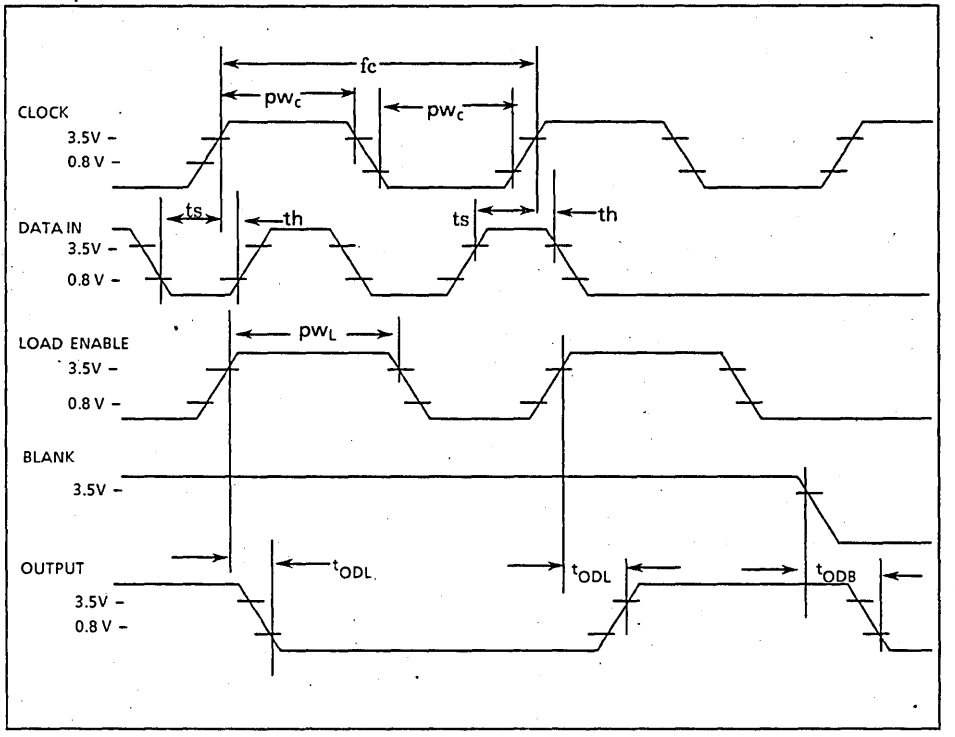
Parameter	Symbol	Condition	Min	Max	Unit
Supply Voltage	V_{DD}	—	– 0.3	20	V
Input Voltage	V_I	—	– 0.3	VDD + 0.3	V
Operating Temp	T_a	—	– 40	85	°C
Storage Temp	T_{st}	—	– 65	150	°C

● AC Characteristics

Ta = −40°C to +85°C, V_{DD} = 8V to 18V Unless otherwise specified

Characteristics	Symbol	Condition	MIN	MAX	Units
Clock Frequency	F_c			160	KHz
Clock Pulse Width	Pw_c	Either positive or negative	2.5		µs
Slew Rate Outputs; (1-33)	t_R	C_L = 100pFt = 20%to80% or 80%to20% of V_{DD} V_{DD} = 8V or V_{DD} = 18V		5	µs
Data Setup Time	t_S		1		µs
Data Hold Time	t_H		200		ns
OUTput Delay from Blank	t_{ODB}	C_L = 100pFV_{DD} = 8V		7	µs
OUTput Delay from Load	t_{ODL}	C_L = 100pFV_{DD} = 8V		8	µs
Power on Reset Slew Rate	PRSR		0.001	10	V / µs
Load Pulse Width	PW_L		1.6		µs

● Timing Chart



• DC Characteristics

Ta = – 40 to 85°C Unless otherwise specified

Characteristic	SYM	Conditions		MIN	MAX	Unit
High Level Input Voltage	V_{IH}	V_{DD} = 8 to 18V		3.5	V_{DD} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{DD} = 8 to 18V		– 0.3	0.8	V
High Input Current (PIN 2, 3, 38)	$I_{IH}1$	V_{DD} = 8to 18V. $V_I = V_{DD}$			1	μA
Low Input Current (PIN 2, 3, 38)	$I_{IL}1$	V_{DD} = 8 to 18V, $V_I = V_{SS}$			– 1	μA
High Input Current (PIN 40)	$I_{IH}2$	V_{DD} = 8 to 18V, V_I = 3.5V		– 5	– 125	μA
Low Input Current (PIN 40)	$I_{IL}2$	V_{DD} = 8 to 18V, V_I = VSS		– 5	– 125	μA
Supply Current	I_{DD}	V_{DD} = 8 to 16V, All Outputs open T_a = – 40°C, 25°C			10	mA
		V_{DD} = 8 to 16V, All Ouputs open T_a = 85°C			7	mA
Low Current Output Drivers (ON) (PIN4 – 16, 25 – 36)	$V_{OH}1$	V_{DD} = 9.5V, I_{OH} = – 1.5mA	Ta = 25°C – 40°C	VDD – 0.3		V
			Ta = 85°C	VDD – 0.5		
Low Current Output Drivers (ON) (PIN 17 – 24)	$V_{OH}2$	V_{DD} = 9.5V, I_{OH} = – 6mA	Ta = 25°C – 40°C	VDD – 0.3		V
			Ta = 85°C	VDD – 0.5		
High Current OutPut Drivers (ON) (PIN 17 – 24)	$V_{OH}2$	V_{DD} = 9.5V, I_{OH} = – 30mA	Ta = 25°C – 40°C	VDD – 2.0		V
			Ta = 85°C	VDD – 2.5		
Output Drivers (OFF) (PIN 4-36)	V_{OL}	V_{DD} = 9.5V, I_{OL} = 1μA / 500μA			V_{SS} + 0.2 /V_{SS} + 5	V
High Voltage Data out (PIN37)	V_{OHD}	V_{DD} = 9.5V, I_{OHD} = – 500μA		VDD – 5		V
Low Voltage Dataout (PIN37)	V_{OLD}	I_{OLD} = 1μA			V_{SS} + 0.4	V

FUNCTIONAL DESCRIPTION

• Data Input

The data pattern (33 bits) supplied to the device through this input controls the output driver state (On or Off).

1. A high level turns the output driver on.
2. A low level turns the output driver off.

- **Clock Input**

  A Positive transition of the clock loads and shifts the data. This input also has a Schmitt trigger which provides 0.3 volts of hysteresis.

- **Blanking Input**

  A low-level voltage at this pin turns the output drivers off; an internal pull up is provided on this pin.

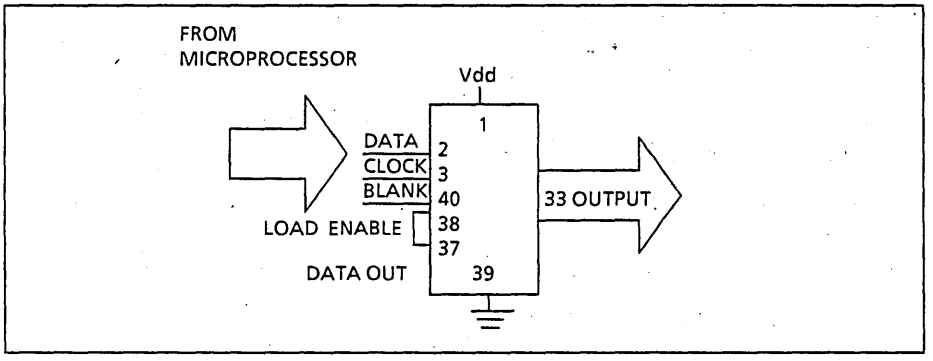
- **Load Enable**

  A high-level at this input transfers the data from the shift register to the data latch, and sets the shift register to zero.

  First data bit read-in is stored in shift register #1, the last data bit read-in is stored in shift register #33. When the shift registers are full, a high Voltage level applied to the load enable input will transfer the data from the shift register to the data latch, and then to the output through the 33 x 33matrix. This matrix determines shift register out put designation. The device is mask programmable for the 33 x 33 matrix, thus providing the capability of changing the shift register output designation. The device has 34 shift registers and 33 data latches as shown in the functional block diagram.
  There are two modes of operation:

- **Self-Load Mode**

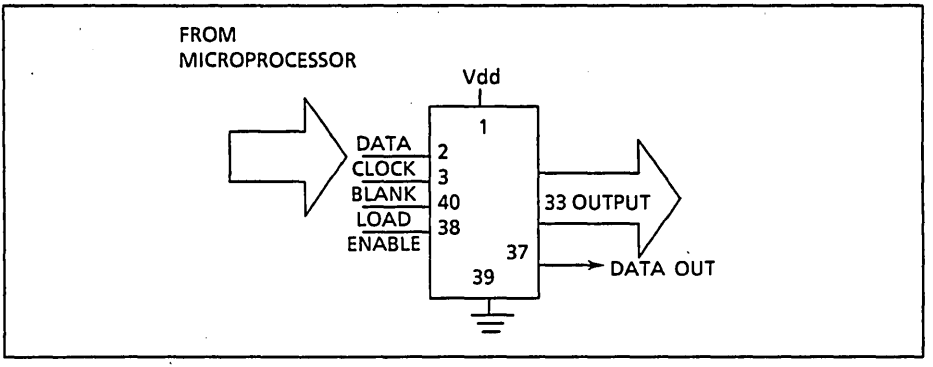
  In this mode Data Out (pin 37) is connected to Load Enable (pin 38), and the data word is constructed with 33 bits (including the one self-load bit set to logic 1). At the 34th clock pulse, the data is transferred from the shift register to the data latch and the output drivers through the 33 x 33matrix. Before the next clock pulse, the registers are zeroed.



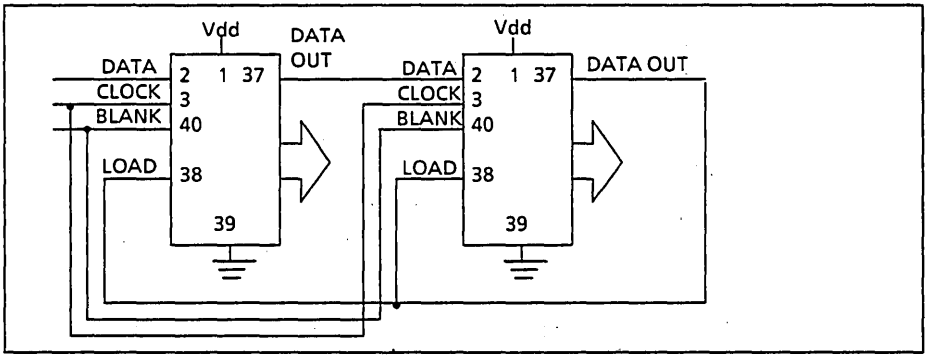
- **Non-Self-Load Mode**

  In this mode, the Data Out and the Load Enable pins are not connected, and the Load Enable input is controlled by an external source. There are two types of operation in this mode.

  1. the data word consists of 34 bits (including one self-load bit). To transfer data from the shift registers to the data latch, a high-level voltage is applied to the Load Enable pin before the rise of the clock pulse following the 34th clock pulse.
  2. The data word consists of 33bits without the self-load bit. To transfer the data, an high voltage level is applied to the Load Enable pin before the rise of the 34th clock pulse.



When the display driver is used in a cascade configuration, a filler bit must be inserted between each group of 33 data bits. The filler bit must be logic 1 when used with the self-loading mode and a logic 0 when used in the non-self-loading mode.



When the cascaded devices are used in self-load mode. the Data Out pin of the last device must be connected to the load enable pin of all devices as shown in the above figure.

When two display drivers are cascaded, sufficient on-chip time delays allow the system to operate within the specification of the device and work in a system.

Up to 10 driver inputs may be connected to the Data Out pin (pin 37) of the last device.

OKI semiconductor
MSM5328
DOT DRIVER

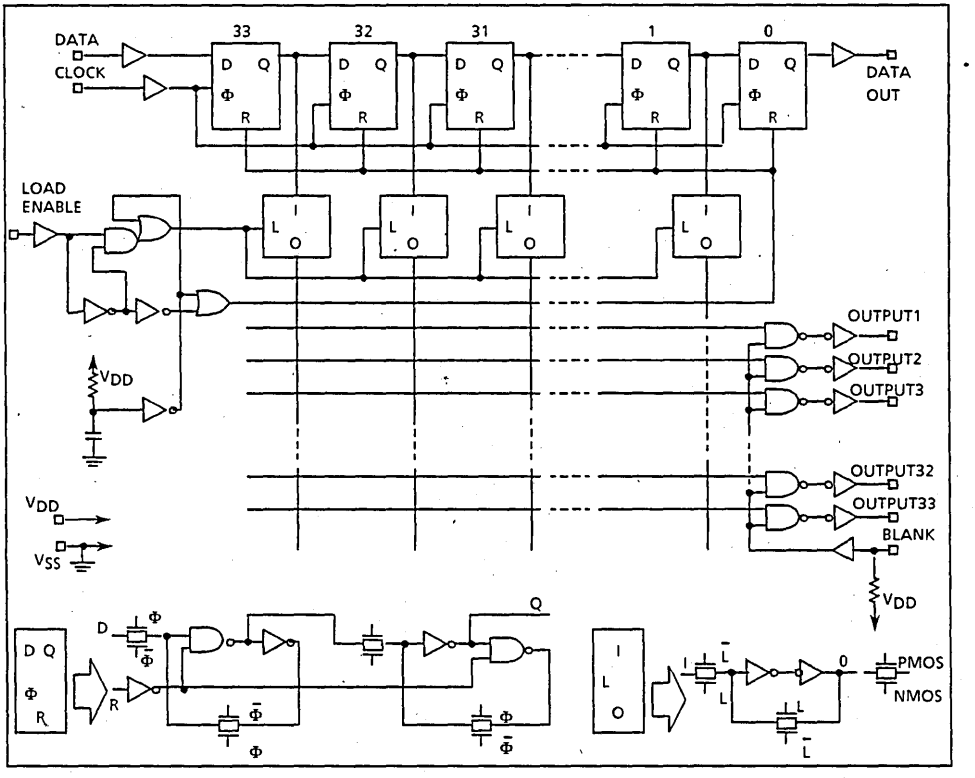
GENERAL DESCRIPTION

The MSM5328RS is a CMOS multi-digit display driver and consists of a 34-bit shift register, a 33-bit latch, and a 33-bit VF tube driver.

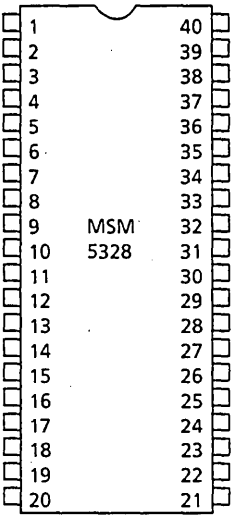
FEATURES

- Complete static operation to ensure stability against noise
- 3 or 4-signal line connection with microcomputers.
- Direct drive of VF tubes (8 outputs of high-current drive, 25 outputs of low-current drive)
- Capability of self-load mode.
- Low power consumption.
- Single power supply and operating voltage range of 8V to 18V

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN#	Pin Name	Comments
1	V_{dd}	Input Positive supply voltage Terminal
2	Data	Input Data Acquisition Terminal
3	Clock	Input Clock Terminal
4	Output 1	Output Shift Register 32
5	Output 2	Output Shift Register 21
6	Out put 3	Output Shift Register 22
7	Output 4	Output Shift Register 23
8	Output 5	Output Shift Register 30
9	Output 6	Output Shift Register 13
10	Output 7	Output Shift Register 14
11	Output 8	Output Shift Register 15
12	Output 9	Output Shift Register 1
13	Output 10	Output Shift Register 33
14	Output 11	Output Shift Register 5

PIN DESCRIPTION

PIN#	Pin Name	Comments
15	Output 12	Output Shift Register 6
16	Output 13	Output Shift Register 7
17	Out put 14	Output Shift Register 28
18	Output 15	Output Shift Register 27
19	Output 16	Output Shift Register 31
20	Output 17	Output Shift Register 18
21	Output 18	Output Shift Register 2
22	Output 19	Output Shift Register 10
23	Output 20	Output Shift Register 26
24	Output 21	Output Shift Register 29
25	Output 22	Output Shift Register 3
26	Output 23	Output Shift Register 8
27	Output 24	Output Shift Register 9
28	Out put 25	Output Shift Register 4
29	Output 26	Output Shift Register 11
30	Output 27	Output Shift Register 16
31	Output 28	Output Shift Register 17
32	Output 29	Output Shift Register 12
33	Output 30	Output Shift Register 19
34	Output 31	Output Shift Register 24
35	Output 32	Output Shift Register 25
36	Output 33	Output Shift Register 20
37	Data Out	Output Data Shift Register
38	Load Enable	Input for Loading Word into Data Latch from Data Shift Register
39	Vss	Ground Potential Terminal
40	Blank	Input for Turning Output Drivers Off

ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Ta = 25°C, Unless otherwise specified

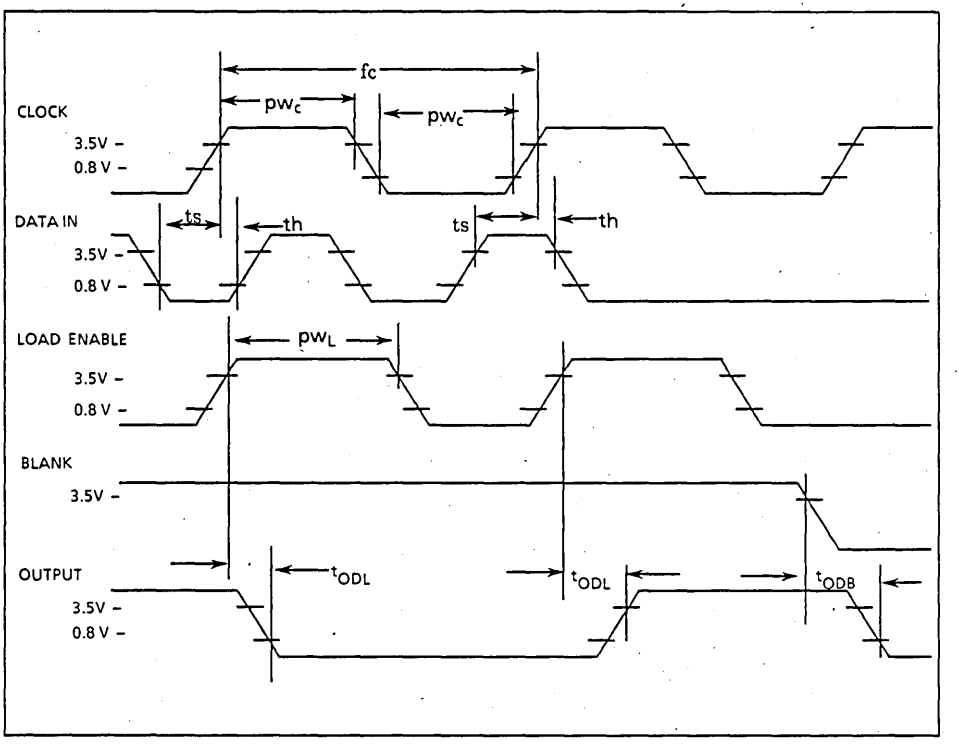
Parameter	Symbol	Condition	Min	Max	Unit
Supply Voltage	V_{DD}	—	− 0.3	20	V
Input Voltage	V_I	—	− 0.3	VDD + 0.3	V
Operating Temp	T_a	—	− 40	85	°C
Storage Temp	T_{st}	—	− 65	150	°C

• AC Characteristics

Ta = −40°C to +85°C, V_{DD} = 8V to 18V Unless otherwise specified

Characteristics	Symbol	Condition	MIN	MAX	Units
Clock Frequency	F_c			160	KHz
Clock Pulse Width	P_{WC}	Either positive or negative	2.5		µs
Slew Rate Outputs; (1-33)	t_R	C_L = 100pFt = 20%to80% or 80%to20% of V_{DD} V_{DD} = 8V or V_{DD} = 18V		5	µs
Data Setup Time	t_S		1		µs
Data Hold Time	t_H		200		ns
OUTput Delay from Blank	t_{ODB}	C_L = 100pFV_{DD} = 8V		7	µs
OUTput Delay from Load	t_{ODL}	C_L = 100pFV_{DD} = 8V		8	µs
Power on Reset Slew Rate	PRSR		0.001	10	V / µs
Load Pulse Width	PW_L		1.6		µs

• Timing Chart



• DC Characteristics

Ta = −40 to 85°C Unless otherwise specified

Characteristic	SYM	Conditions		MIN	MAX	Unit
High Level Input Voltage	V_{IH}	V_{DD} = 8 to 18V		3.5	V_{DD} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{DD} = 8 to 18V		−0.3	0.8	V
High Input Current (PIN 2, 3, 38)	$I_{IH}1$	V_{DD} = 8to 18V. $V_I = V_{DD}$			1	μA
Low Input Current (PIN 2, 3, 38)	$I_{IL}1$	V_{DD} = 8 to 18V, $V_I = V_{SS}$			−1	μA
High Input Current (PIN 40)	$I_{IH}2$	V_{DD} = 8 to 18V, V_I = 3.5V		−5	−125	μA
Low Input Current (PIN 40)	$I_{IL}2$	V_{DD} = 8 to 18V, V_I = VSS		−5	−125	μA
Supply Current	I_{DD}	V_{DD} = 8 to 16V, All Outputs open T_a = −40°C, 25°C			10	mA
		V_{DD} = 8 to 16V, All Ouputs open T_a = 85°C			7	mA
Low Current Output Drivers (ON) (PIN4 − 16, 25 − 36)	$V_{OH}1$	V_{DD} = 9.5V, I_{OH} = −0.8mA	Ta = 25°C − 40°C	V_{DD} − 0.3		V
			Ta = 85°C	V_{DD} − 0.5		
High Current OutPut Drivers (On) (PIN 17 − 24)	$V_{OH}2$	V_{DD} = 9.5V, I_{OH} = −3.5mA	Ta = 25°C − 40°C	V_{DD} − 0.3		V
			Ta = 85°C	V_{DD} − 0.5		
Output Drivers (OFF) (PIN 4-36)	V_{OL}	V_{DD} = 9.5V, I_{OL} = 1μA / 500μA			V_{SS} + 0.2 /V_{SS} + 5	V
High Voltage Data out (PIN37)	V_{OHD}	V_{DD} = 9.5V, I_{OHD} = −500μA		V_{DD} − 5		V
Low Voltage Dataout (PIN37)	V_{OLD}	I_{OLD} = 1μA			V_{SS} + 0.4	V

FUNCTIONAL DESCRIPTION

• Data Input

The data pattern (33 bits) supplied to the device through this input controls the output driver state (On or Off).

1. A high level turns the output driver on.
2. A low level turns the output driver off.

• Clock Input

A Positive transition of the clock loads and shifts the data. This input also has a Schmitt trigger which provides 0.3 volts of hysteresis.

- **Blanking Input**

  A low-level voltage at this pin turns the output drivers off; an internal pull up is provided on this pin.

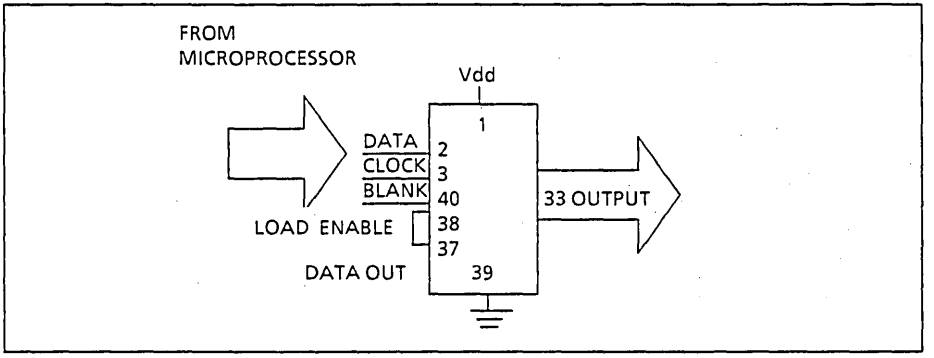
- **Load Enable**

  A high-level at this input transfers the data from the shift register to the data latch, and sets the shift register to zero.

  First data bit read-in is stored in shift register #1, the last data bit read-in is stored in shift register #33. When, the shift registers are full a high Voltage level applied to the load enable input will transfer the data from the shift register to the data latch. The device has 34 shift registers and 33 data latches as shown in the functional block diagram.
  There are two modes of operation:

- **Self-Load Mode**

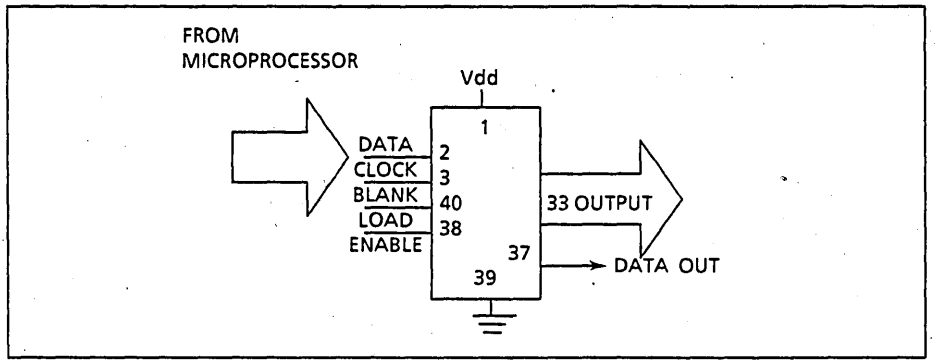
  In this mode Data Out (pin 37) is connected to Load Enable (pin 38), and the data word is constructed with 33 bits (including the one self-load bit set to logic 1). At the 34th clock pulse, the data is transferred from the shift register to the data latch and the output drivers. Before the next clock pulse, the registers are zeroed.



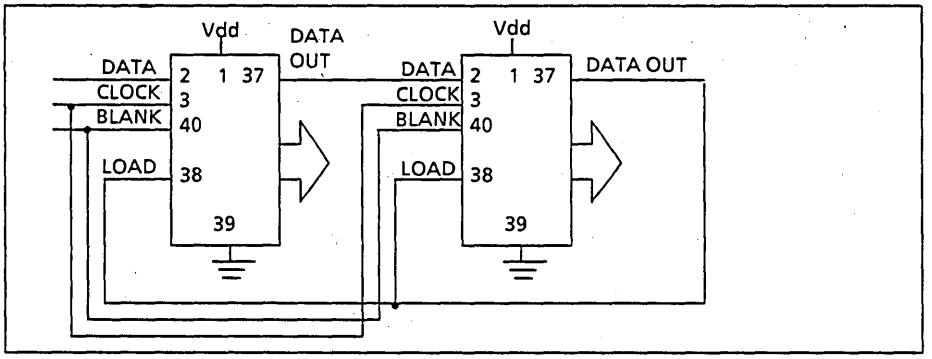
- **Non-Self-Load Mode**

  In this mode, the Data Out and the Load Enable pins are not connected, and the Load Enable input is controlled by an external source. There are two types of operation in this mode.

  1. the data word consists of 34 bits (including one self-load bit). To transfer data from the shift registers to the data latch, a high-level voltage is applied to the Load Enable pin before the rise of the clock pulse following the 34th clock pulse.
  2. The data word consists of 33bits without the self-load bit. To transfer the data, an high voltage level is applied to the Load Enable pin before the rise of the 34th clock pulse.



When the display driver is used in a cascade configuration, a filler bit must be inserted between each group of 33 data bits. The filler bit must be logic 1 when used with the self-loading mode and a logic 0 when used in the non-self-loading mode.



When the cascaded devices are used in self-load mode. the Data Out pin of the last device must be connected to the load enable pin of all devices as shown in the above figure.

When two display drivers are cascaded, sufficient on-chip time delays allow the system to operate within the specification of the device and work in a system.

Up to 10 driver inputs may be connected to the Data Out pin (pin 37) of the last device.

OKI semiconductor
MSC1178 / MSC1179

7-SEGMENT DRIVER

GENERAL DESCRIPTION

The MSC1178/79 is a BiCMOS structure static display driver to directly drive a vacuum fluorescent (VF) display tube. The driver has a structure of a 56-pin flat package, which consists of a 35 bits shift register, latch circuit, 7 segment decoder, VF high voltage driver, LED dot driver, dimming OSC circuit, and dimming control circuit.

The driver is suited to a driver for frequency or clock display of an automobile digital tuning system.

FEATURES

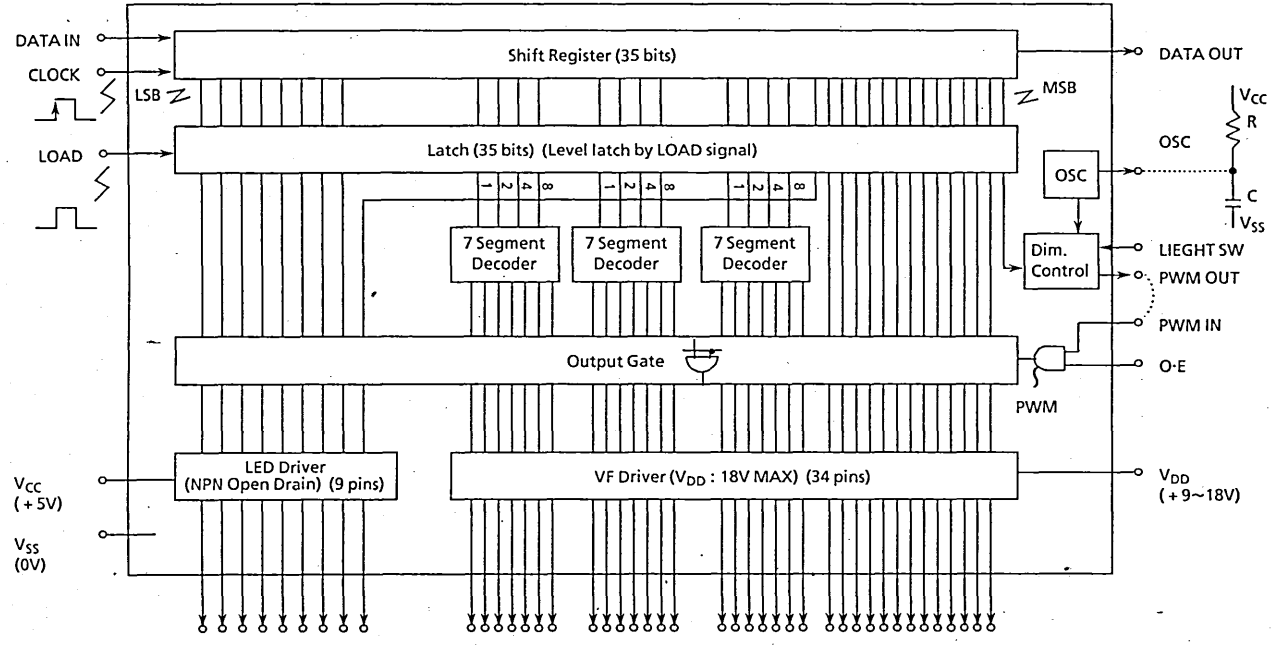
- 56-pin flat package (small)
- 2 supply voltages

  Interface, logic portion, LED driver : V_{CC} = +4.5 to +5.5 V

  VF display driver : V_{DD} = +9 V to +18 V
- VF tube driven by positive voltage (V_{DD} = +18 V MAX)
- VF tube directly connected : No pull down resistor required (CMOS push pull output)
- Dimming oscillation circuit built in (capacitor and resistor externally connected)
- Dimming control circuit built in, with duty (100%, 1/8, or 1/16) selector input terminal (LIGHT-SW). Use the most significant bit (MSB) to select 1/8 or 1/16. L : 1/8, H : 1/16
- With PWM IN input terminal to allow the PWM to continuously control dimming, with external PWM generation circuit
- 3-digit 7 segment output, 13-flag output (I_O = −1 mA TYP)
- 9-LED dot display (I_O = 20 mA MAX)
- Easy control by microprocessor and easy signal line connection (connected by three signal lines, DATA IN, CLOCK, and LOAD)
- 7 display patterns selected by device (The MSC1178GS-K and the MSC1179GS-K differ in the 7 display patterns from each other.)

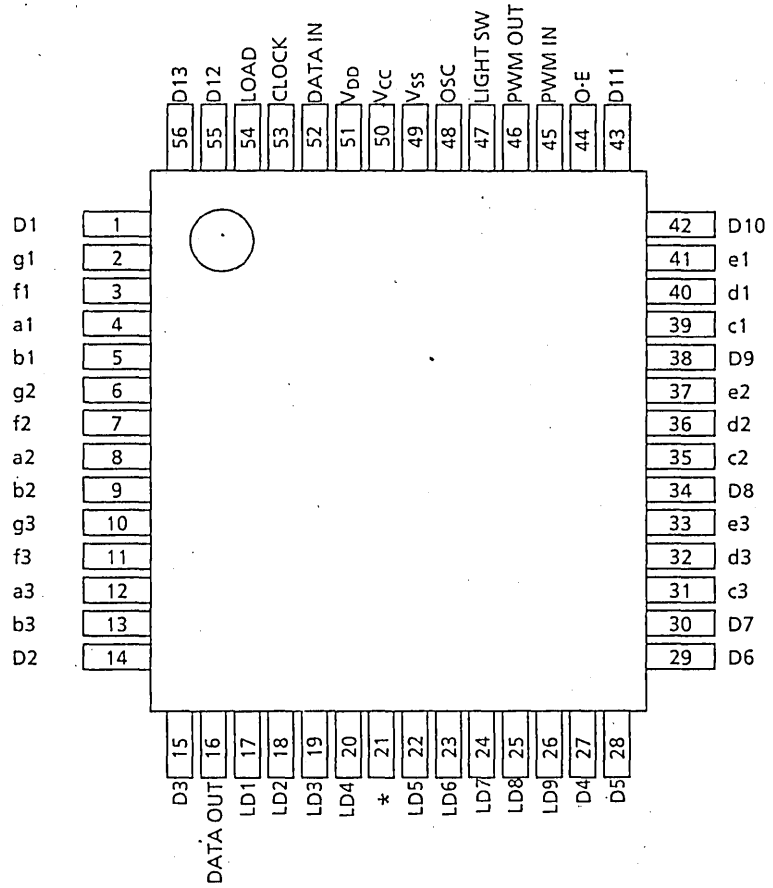
  MSC1178GS-K MSC1179GS-K

BLOCK DIAGRAM



PIN CONFIGURATION

(Top View) 56 Lead Plastic Flat Package



Note: Pin 21 with a * mark is connected to V_{SS}, and cannot be connected to another pin. Pin 21 cannot be used independently as V_{SS} but can be used as V_{SS} reinforcing line.

ELECTRICAL CHARACTERISTICS

- **Absolute maximum ratings**

Parameter	Symbol	Conditions	Limits	Unit
Supply voltage	V_{DD}		−0.3~+19	V
Supply voltage	V_{CC}		−0.3~+6.5	V
Input voltage	V_I	DATA IN, CLOCK, LOAD LIGHT SW, PWMIN, O·E, OSC	−0.3~V_{CC}+0.3	V
Maximum output current	I_{OLD}	LD1~LD9	25	mA
Allowable package loss	P_D		300	mW
Storage temperature	T_{stg}		−55~+150	°C

- **Recommended operating range**

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}		9	12	18	V
Supply voltage	V_{CC}		4.5	5	5.5	V
Input voltage	V_{IH}	DATA IN, CLOCK, LOAD LIGHT SW, PWM IN, O·E	0.7V_{CC}		V_{CC}	V
Input voltage	V_{IL}	DATA IN, CLOCK, LOAD LIGHT SW, PWM IN, O·E	0		0.2V_{CC}	V
Output current	I_{OLD}	LD1~LD9		10	20	mA
Operating temperature	T_{OP}		−40		+85	°C

• DC characteristics

(Unless otherwise specified, V_{CC} = 5V, V_{DD} = 12V, Ta = − 40 to + 85°C)

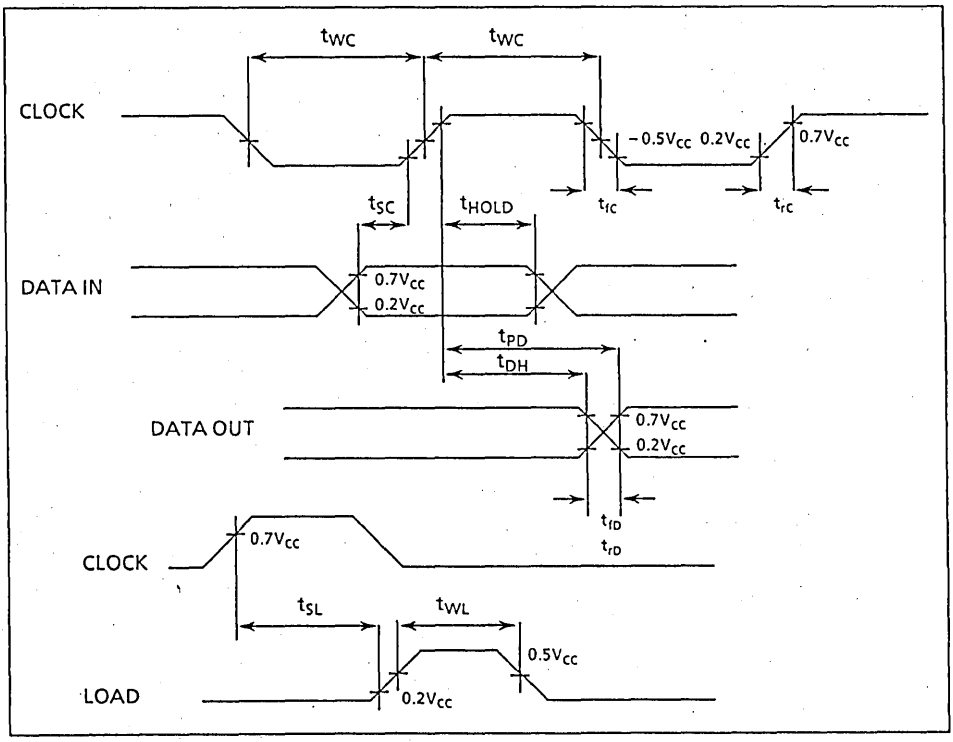
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}		9	12	18	V
Supply voltage	V_{CC}		4.5	5	5.5	V
High level input voltae	V_{IH}	DATA IN, CLOCK, LOAD LIGHT SW, PWM IN, O·E	0.7V_{CC}		V_{CC}	V
Low level input voltage	V_{IL}		0		0.2V_{CC}	V
Input leak	I_{IL1}	DATA IN, CLOCK, LOAD V_{CC} = 5.5V PWM IN, O·E, $V_I = V_{CC}$ or 0V			± 1	µA
High level input leak current	I_{IH}	LIGHT SW V_I = VCC = 5.5V			1	µA
Low level input current	I_{IL2}	V_I = 0V, VCC = 5.0V	− 20	− 68	− 200	µA
High level output voltage	V_{OH1}	DATA OUT, PWM OUT, I_O = − 40µA	4.3	4.9		V
High level output voltage	V_{OH2}	a1~g3, D1~D13, I_O = − 1mA	11.4	11.8		V
Low level output voltage	V_{OL1}	DATA OUT, PWM OUT, I_O = 40µA		0.1	0.4	V
Low level output voltage	V_{OL2}	a1~g3, D1~D13, I_O = 100µA		0.2	0.7	V
Low level output voltage	V_{OL3}	LD1~LD9, I_O = 20mA		0.2	1	V
High level output leak current	I_{TH}	LD1~LD9, $V_O = V_{DD}$ = 18V			10	µA
V_{DD} line supply current	I_{DD1}	PWM IN = O·E = V_{CC}, a1~g3→ character D_1 to D_{13} all high level output, other input terminals at 0V or V_{CC}, output at no load			0.1	mA
	I_{DD2}	O·E = 0V, Other input terminals at 0V or V_{CC}, output at no load			0.1	mA
V_{CC} line supply current	I_{CC1}	OSC = 0V, LIGHT SW = Vcc; Other input terminals at 0V or V_{CC}, output at no load			0.1	mA
	I_{CC2}	R = 51kΩ C = 0.047µF CR oscillaton, LIGHT SW = 0W; Other input terminals at 0V or V_{CC}, output at no load		0.3	1	
	I_{CC3}	OSC = 0V, PWM IN = Vcc O·E = V_{CC}, LD1~9:ON(Low), Other input terminals at 0V or V_{CC}, output at no load		9	20	mA

• AC characteristics

V_{CC} = 5V ± 10%、 Ta = −40~+85°C, C_L = 10PF

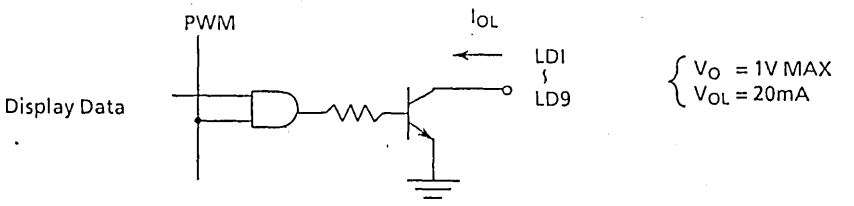
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Maximum clock frequency	f_{CLK}	CLOCK			1	MHz
Minimum clock pulse width	t_{WC}	CLOCK	400			nS
Minimum load pulse width	t_{WL}	LOAD	400			nS
Clock input rise and breaking time	t_{fc} t_{rc}	CLOCK			1	µS
DATA IN→ CLOCK setup time	t_{SC}		200			nS
CLOCK→ DATA IN hold time	t_{HOLD}		100			nS
CLOCK→ DATA OUT propagation delay time	t_{PD}				700	nS
DATA OUT hold time	t_{DH}		150			nS
CLOCK→ LOAD setup time	t_{SL}		500			nS
CR oscillation frequency	f_{OSC}	C = 0.047µF, R = 51kΩ	1	2	4	kHz

• Timing Chart

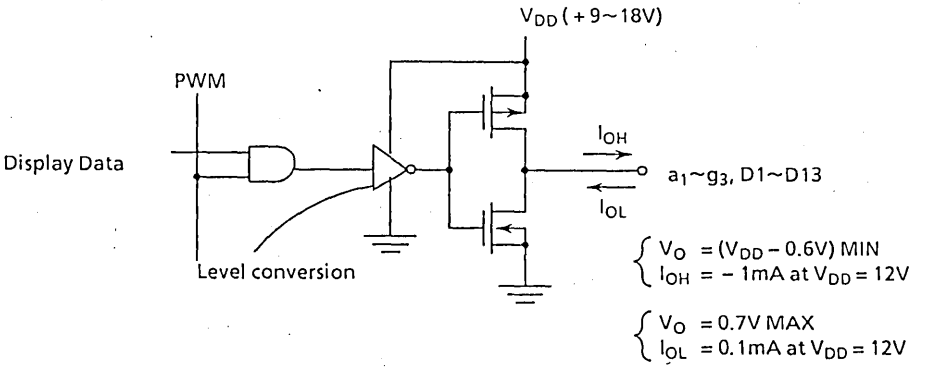


MAJOR SECTIONS EQUIVALENT CIRCUIT

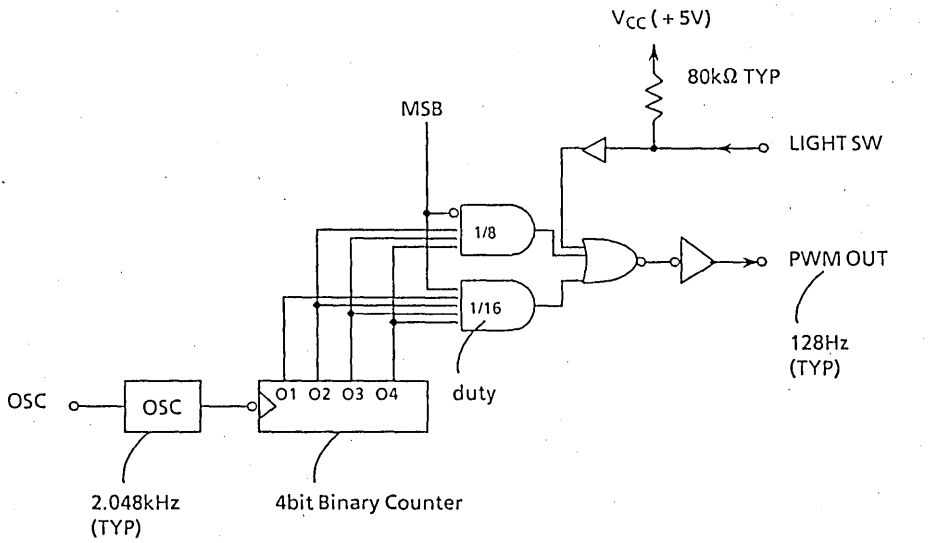
Output Gate & LED Driver



Output Gate & VF Driver



Dim control circuit



DATA DESCRIPTION

(Table a)

No.	Symbol	Function	Output terminal	Description	
1	DIM(MSB)	Dimming control		"0" : 1/8duty, "1" 1/16duty	
2	D13	Flag(VF)	D13	VF driver	"0" : OFF "1" : ON
3	D12		D12		
4	D11		D11		
5	D10		D10		
6	D9		D9		
7	D8		D8		
8	D7		D7		
9	D6		D6		
10	D5		D5		
11	D4		D4		
12	D3		D3		
13	D2		D2		
14	D1		D1		
15	LD9	Flag(LED)	LD9	LED driver	
16 17 18 19	D1-8 D1-4 D1-2 D1-1	7 segment decoder(1st digit)	a1~g1	VF driver	See Table b.
20 21 22 23	D2-8 D2-4 D2-2 D2-1	7 segment decoder(2nd digit)	a2~g2		
24 25 26 27	D3-8 D3-4 D3-2 D3-1	7 segment decoder(3rd digit)	a3~g3		
28	LD8	Flag(LED)	LD8	LED driver	"0" : OFF "1" : ON
29	LD7		LD7		
30	LD6		LD6		
31	LD5		LD5		
32	LD4		LD4		
33	LD3		LD3		
34	LD2		LD2		
35	LD1(LSB)		LD1		

Note : "No." indicates the output number of the shift register. The first bit for data transfer is No. 1.

7 SEGMENT DECODER DISPLAY PATTERN

(Table b)

Input data					Output								Remarks
	8	4	2	1	a	b	c	d	e	f	g	Display pattern	
0	0	0	0	0	1	1	1	1	1	1	0		
1	0	0	0	1	0	1	1	0	0	0	0		
2	0	0	1	0	1	1	0	1	1	0	1		
3	0	0	1	1	1	1	1	1	0	0	1		
4	0	1	0	0	0	1	1	0	0	1	1		
5	0	1	0	1	1	0	1	1	0	1	1		
6	0	1	1	0	1	0	1	1	1	1	1		
7	0	1	1	1	1	1	1	0	0	1	0		MSC1179GS-K:"  "
8	1	0	0	0	1	1	1	1	1	1	1		
9	1	0	0	1	1	1	1	1	0	1	1		
A	1	0	1	0	1	1	1	0	1	1	1		
B	1	0	1	1	0	0	1	1	1	1	1		
C	1	1	0	0	0	0	0	1	1	0	1		
D	1	1	0	1	0	1	1	1	1	0	1		
E	1	1	1	0	1	0	0	1	1	1	1		
F	1	1	1	1	0	0	0	0	0	0	0	Blank	

FUNCTIONAL DESCRIPTION

- **DATA IN, CLOCK, LOAD : Data set input terminals**

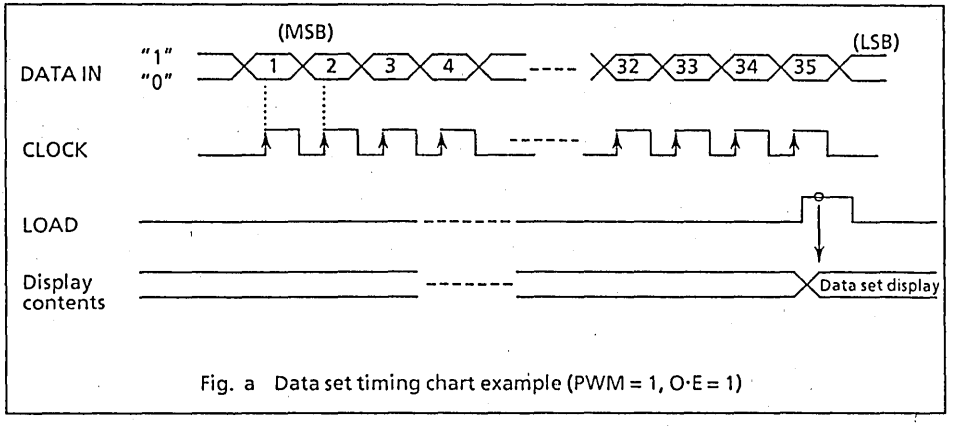


Fig. a Data set timing chart example (PWM = 1, O·E = 1)

DATA IN is a data input terminal, which is read into the internal shift register at the leading edge of the clock input terminal CLOCK.

LOAD is a load input terminal, which loads data of the shift register, data of 35 bits at a time, into the latch circuit. The timing chart above shows that, when a pulse is input to the LOAD terminal after the data of 35 bits is input, the display data is changed to a new one.

- **DATA OUT : Data output terminal**

DATA OUT is a terminal for cascade connection, the output of which is connected to the DATA IN terminal on the next stage.

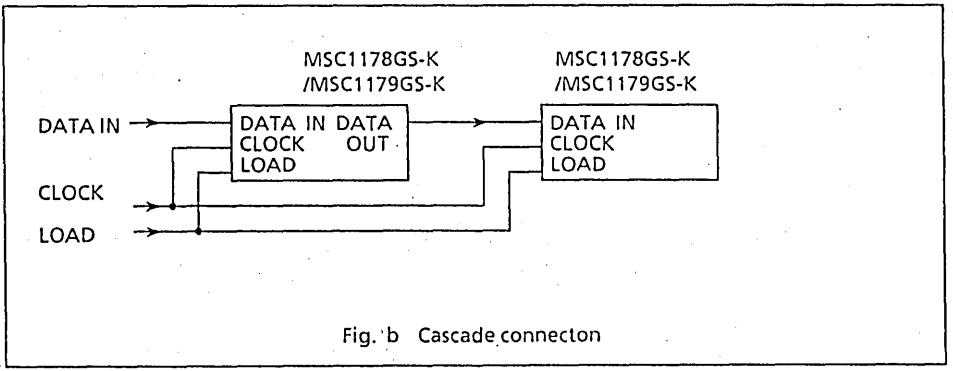


Fig. b Cascade connecton

• OSC : Oscillation terminal

OSC is a capacitor (C) and resistor (R) connection terminal of the oscillation circuit for dimming control. The oscillation frequency depends on the values of the external capacitor (C) and resistor (R).

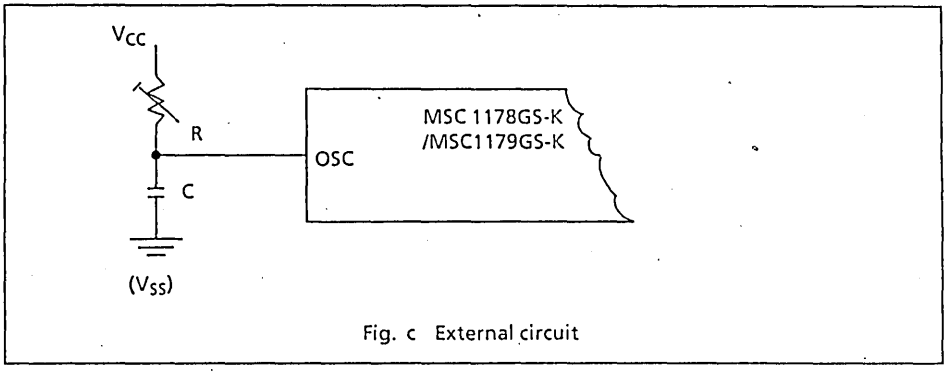


Fig. c External circuit

The value for R should not be less than 30 kΩ. The oscillation frequency f_{OSC} is expressed by the following equation:

$$f_{OSC} = \frac{k}{C \cdot R} \quad (k \fallingdotseq 5)$$

When no oscillation circuit is used (i.e the PWM OUT terminal is not used), connect the OSC terminal to V_{SS}.

• LIGHT SW : Light switch input terminal

LIGHT SW is an input terminal with a pull-up resistor, which controls the PWM OUT output waveform.(See Table c.)

• PWM OUT : PWM output terminal

PWM OUT is a dimming PWM output terminal. When this terminal is connected to the PWM IN input terminal, the display duty ratio can be changed to 1/1, 1/8, or 1/16. Table c is a function table. (Table c)

LIGHT SW input	MSB of data	Display duty ratio
Open or "H"	–	1/1
"L"	0	1/8
"L"	1	1/16

"H" ; V_{CC} level
"L" ; V_{SS} level
– don't care

The frequency of a PWM OUT output signal is $f_{OSC}/16$.

- **PWM IN : PWM input terminal**

PWM IN is a dimming PWM input terminal. If the input is made High when the O·E is High, the display is turned ON. If the input is made Low, the display is turned OFF.

Accondingly, when a signal at 100 to several 100s Hz (the duty ratio is variable) is input to the PWM IN terminal, the display brightness can be continuously controlled.

When the PWM OUT output is connected to the PWM IN terminal, the display duty ratio, as mentioned above, can be changed to one of the three values.

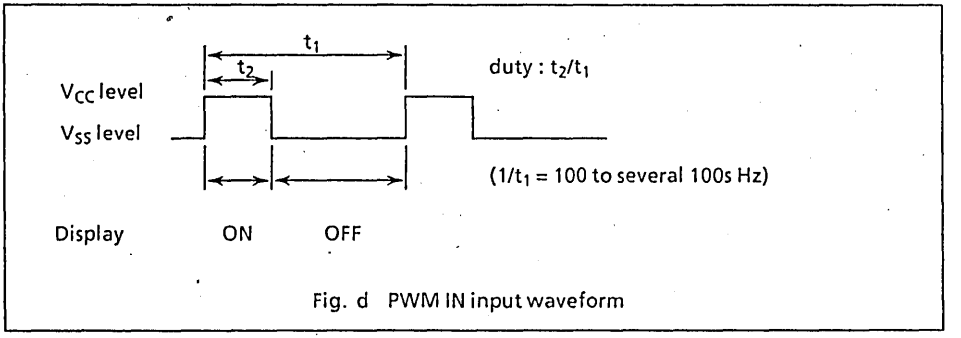


Fig. d PWM IN input waveform

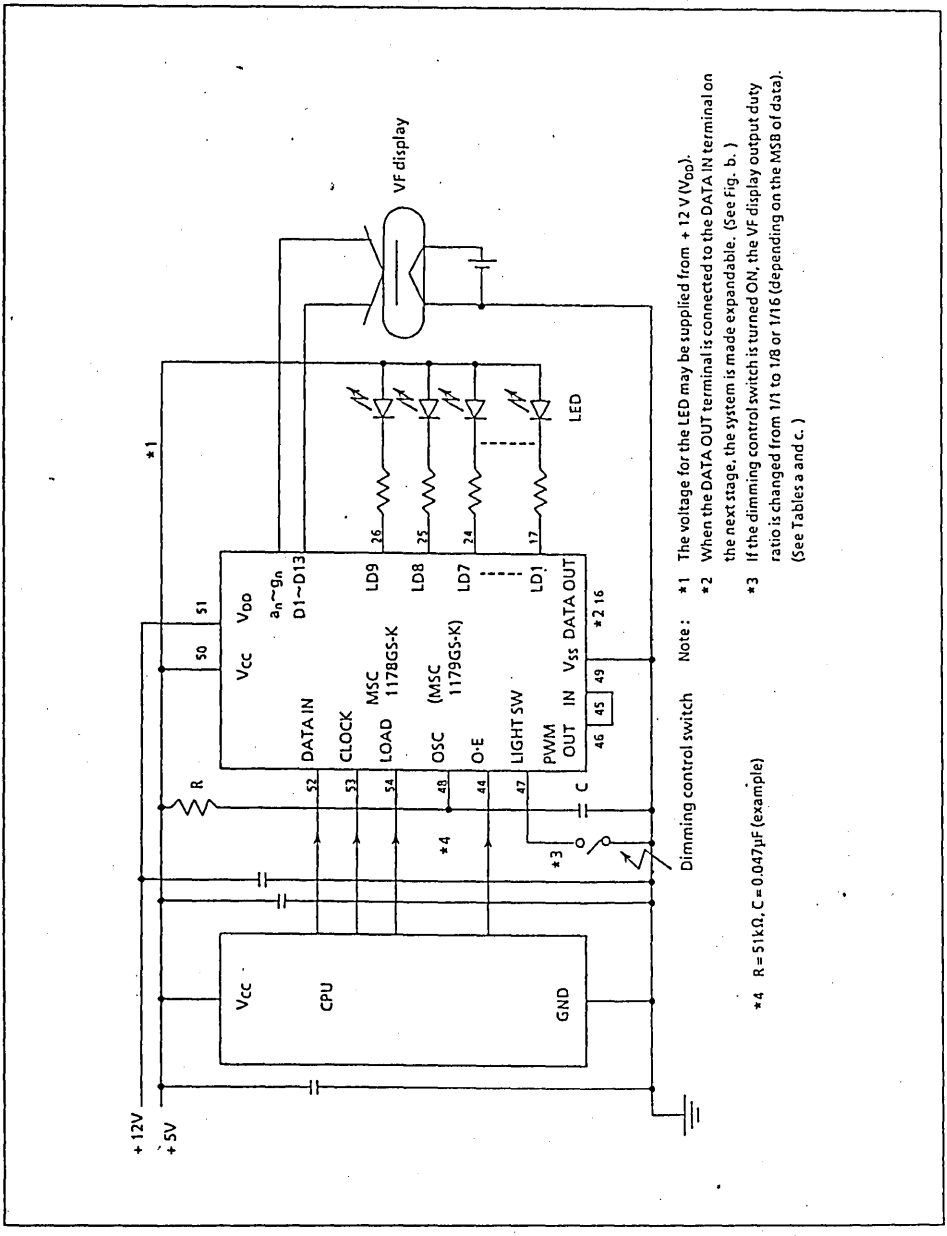
- **O·E : Display output enable input terminal**

When the input is High, the display state is normal. When the input is Low, all displays are turned OFF.

If the O·E is kept Low until the data of the latch circuit is determined when power is turned ON, unnecessary displays can be eliminated.

Two O·E and PWN IN input signals are ANDed in the IC to a PWM signal. The display is ON (normal) when PWM = "1" or OFF when PWM = "0".

APPLICATON NOTE



OKI semiconductor
MSC1190

7-SEGMENT DRIVER

GENERAL DESCRIPTION

The MSC1190GS is a Bi-CMOS structure static display driver to directly drive a vacuum fluorescent (VF) display tube. The driver has a structure of a 56-pin flat package, which consists of a 35-bit shift register, latch circuit, 7 segmemt decoder, VF high voltage driver, LED dot driver, and dimming control circuit.

The driver is suited to a driver for frequency or clock display of an automobile digital tuning system.

FEATURES

- 56-pin flat package
- 2 supply voltages (+ side)

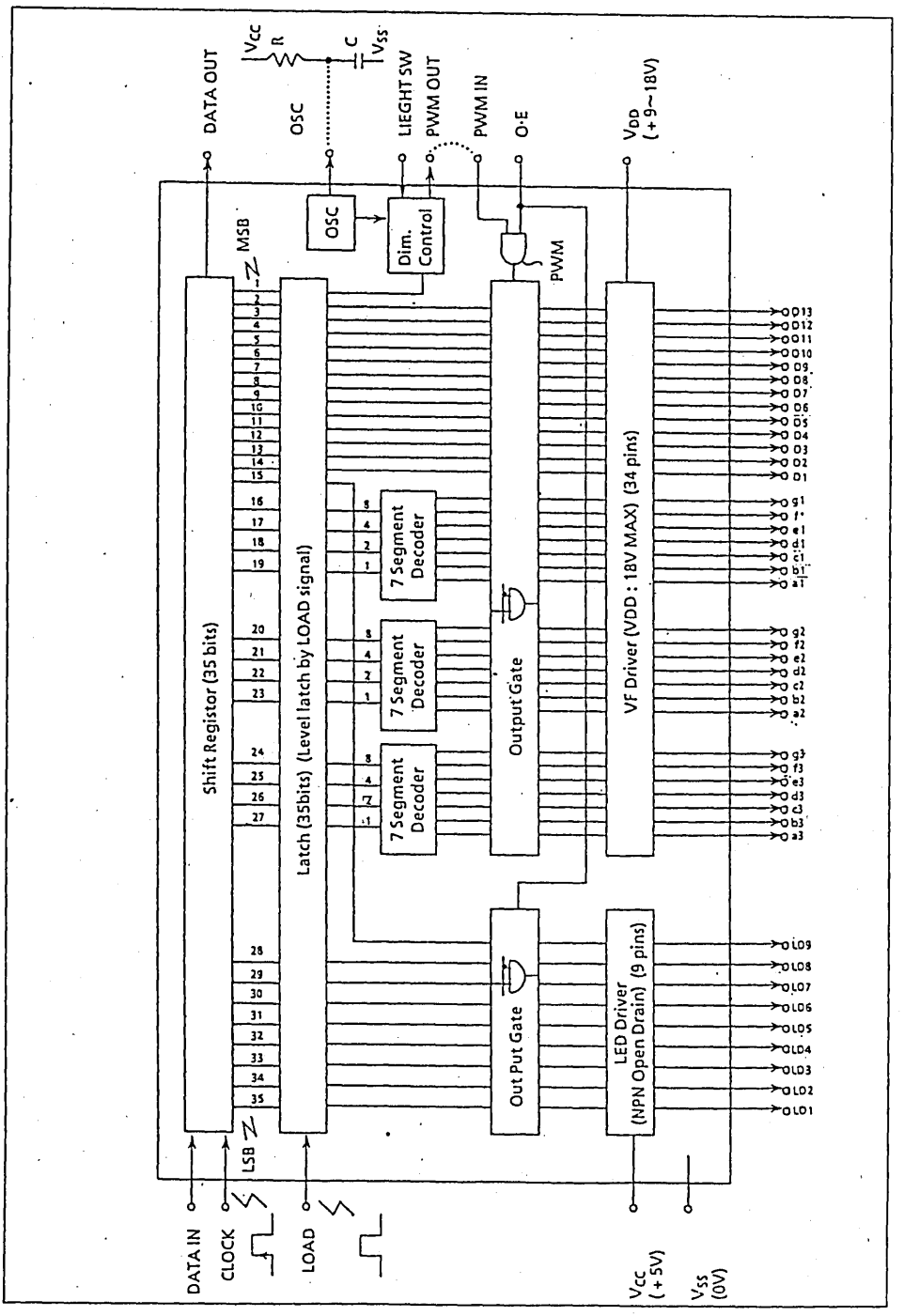
  Interface, logic portion, LED driver : V_{CC} = + 4.5 to + 5.5 V

  VF display driver : V_{DD} = + 9 to + 18V
- VF tube driven by positive voltage (V_{DD} = + $18V_{MAX}$)
- VF tube directly connected without a pull-down resistor

  (CMOS push pull output)
- Dimming oscillation circuit built in (capacitor and resistor externally connected)
- Dimming control circuit built in, with duty (1/1, 1/8, or 1/16) selector input terminal (LIGHT-SW). Use the most significant bit (MSB) to select 1/8 or 1/16.
- With PWM IN input terminal to allow the PWM to continuously control dimming, with external PWM generation circuit (the LED driver is not affected by PWM IN input)
- VF driver : 3-digit 7 segment output, 13 flag outputs

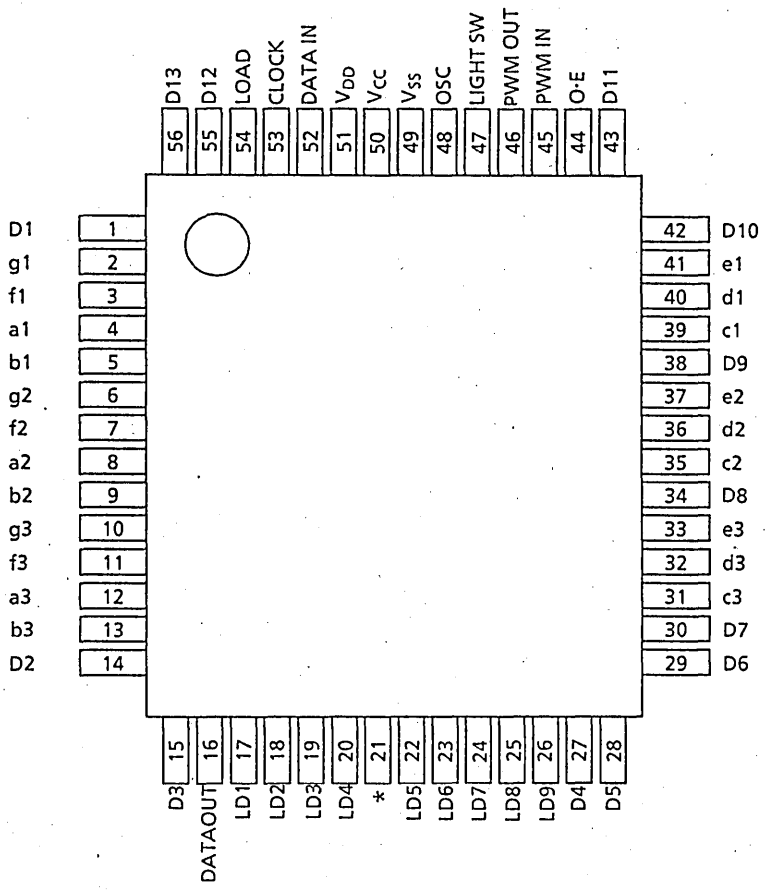
  (I_O = − 1 mA_{TYP})
- LED driver : 9 dot outputs (I_O = $25mA_{MAX}$)
- Easily interfaced with microprocessor (by three inputs of DATA IN, CLOCK, and LOAD)

BLOCK DIAGRAM



PIN CONFDIGURATION

(Top View) 56 Lead Plastic Flat Package



Note: Pin 21 with a * mark is connected to V_{SS}, and cannot be connected to another pin. Pin 21 cannot be used independently as V_{SS} but can be used as a V_{SS} reinforcing line.

ELECTRICAL CHARACTERISTICS

- **Absolute maximum ratings**

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}		−0.3~+19	V
Supply voltage	V_{CC}		−0.3~+6.5	V
Input voltage	V_I	DATA IN, CLOCK, LOAD LIGHT SW, PWMIN, O·E, OSC	−0.3~V_{CC}+0.3	V
Maximum output current	I_{OLD}	LD1~LD9	30	mA
Allowable package loss	P_D		300	mW
Storage temperature	T_{stg}		−55~+150	°C

- **Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}		9	12	18	V
Supply voltage	V_{CC}		4.5	5	5.5	V
Input voltage	V_{IH}	DATA IN, CLOCK, LOAD LIGHT SW, PWMIN, O·E	0.7V_{CC}		V_{CC}	V
Input voltage	V_{IL}	DATA IN, CLOCK, LOAD LIGHT SW, PWMIN, O·E	0		0.2V_{CC}	V
Output current	I_{OLD}	LD1~LD9		15	25	mA
Operating temperature	T_{OP}		−40		+85	°C

• DC characteristics

(Unless otherwise specified, V_{CC} = 5V, V_{DD} = 12V, Ta = − 40 to + 85°C)

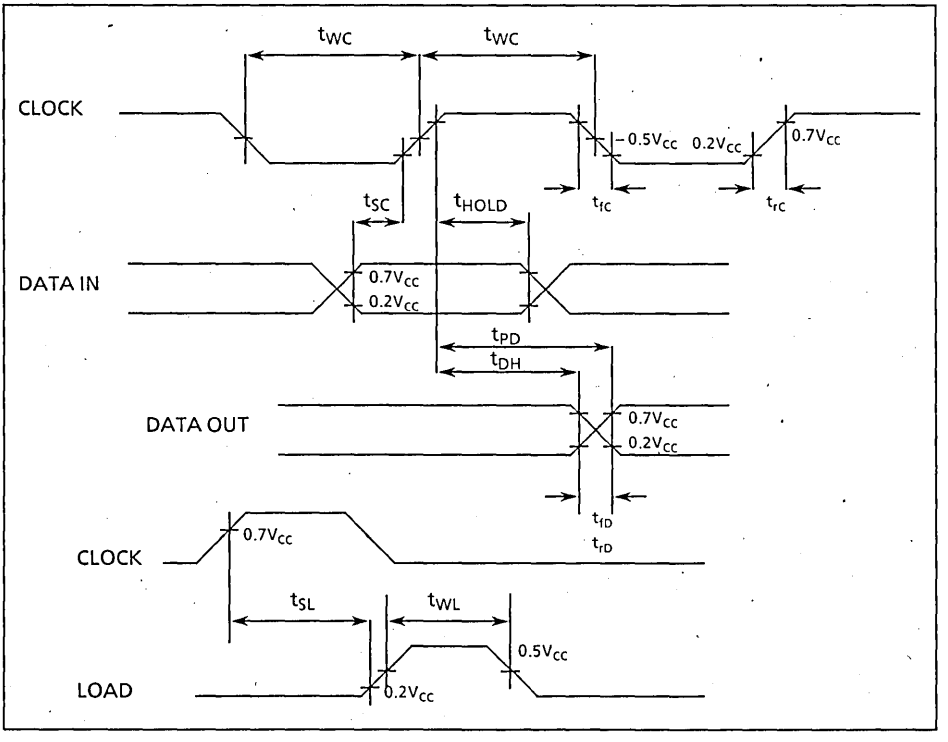
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}		9	12	18	V
Supply voltage	V_{CC}		4.5	5	5.5	V
High level input voltae	V_{IH}	DATA IN, CLOCK, LOAD	0.7V_{CC}		V_{CC}	V
Low level input voltage	V_{IL}	LIGHT SW, PWM IN, O·E	0		0.2V_{CC}	V
Input leak	I_{IL1}	DATA IN, CLOCK, LOAD V_{CC} = 5.5V PWM IN, O·E, V_I = V_{CC} or 0V			± 1	µA
High level input leak current	I_{IH}	LIGHT SW V_I = VCC = 5.5V			1	µA
Low level input current	I_{IL2}	V_I = 0V, VCC = 5.0V	− 20	− 68	− 200	µA
High level output voltage	V_{OH1}	DATA OUT, PWM OUT, I_O = − 40µA	4.3	4.9		V
High level output voltage	V_{OH2}	a1~g3, D1~D13, I_O = − 1mA	11.4	11.8		V
Low level output voltage	V_{OL1}	DATA OUT, PWM OUT, I_O = 40µA		0.1	0.4	V
Low level output voltage	V_{OL2}	a1~g3, D1~D13, I_O = 100µA		0.2	0.7	V
Low level output voltage	V_{OL3}	LD1~LD9, I_O = 25mA		0.25	0.8	V
High level output leak current	I_{TH}	LD1~LD9, V_O = V_{DD} = 18V			10	µA
V_{DD} line supply current	I_{DD1}	PWM IN = O·E = V_{CC}, a1~g3→ character D_1 to D_{13} all high level output, other input terminals at 0 V or V_{CC}, output at no load			0.1	mA
	I_{DD2}	O·E = 0V, Other input terminals at 0 V or V_{CC}, output at no load			0.1	mA
V_{CC} line supply current	I_{CC1}	OSC = 0V, LIGHT SW = VCC, Other input terminals at 0 V or VCC, output at no load			0.1	mA
	I_{CC2}	R = 51kΩ C = 0.047µF CR oscillaton, LIGHT SW = 0W		0.3	1	
	I_{CC3}	OSC = 0V, PWM IN = V_{CC} O·E = VCC, LD1~9:ON(Low), Other input terminals at 0 V or V_{CC}, output at no load		9	20	mA

• AC characteristics

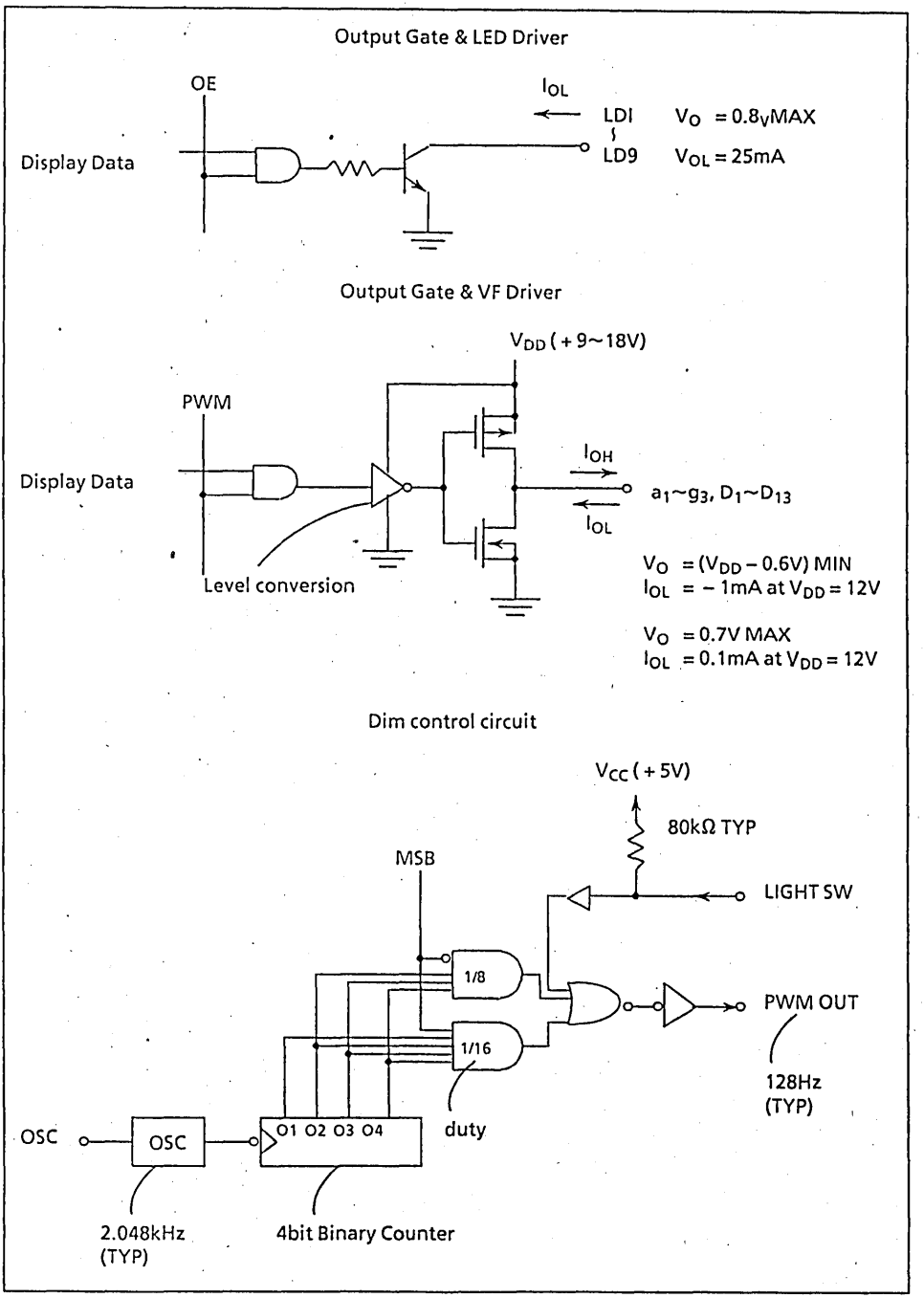
V_{CC} = 5V ± 10%、 Ta = − 40~ + 85°C, C_L = 10PF

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Maximum clock frequency	f_{CLK}	CLOCK			1	MHz
Minimum clock pulse width	t_{WC}	CLOCK	400			nS
Minimum load pulse width	t_{WL}	LOAD	400			nS
Clock input rise and breaking time	t_{fc} t_{rc}	CLOCK			1	µS
DATA IN→ CLOCK setup time	t_{SC}		200			nS
CLOCK→ DATA IN hold time	t_{HOLD}		100			nS
CLOCK→ DATA OUT propagation delay time	t_{PD}				700	nS
DATA OUT hold time	t_{DH}		150			nS
CLOCK→ LOAD setup time	t_{SL}		500			nS
CR Oscillating frequency	f_{OSC}	C = 0.047µF, R = 51kΩ	1	2	4	kHz

TIMING CHART



MAJOR SECTIONS EQUIVALENT CIRCUIT



DATA DESCRIPTION

(Table a)

No.	Symbol	Function	Output terminal	Description	
1	DIM(MSB)	Dimming control		"0" : 1/8duty, "1" 1/16duty	
2	D13	Flag(VF)	D13	VF driver	"0" : OFF "1" : ON
3	D12		D12		
4	D11		D11		
5	D10		D10		
6	D9		D9		
7	D8		D8		
8	D7		D7		
9	D6		D6		
10	D5		D5		
11	D4		D4		
12	D3		D3		
13	D2		D2		
14	D1		D1		
15	LD9	Flag(LED)	LD9	LED driver	
16 17 18 19	D1-8 D1-4 D1-2 D1-1	7 segment decoder(1st digit)	a1~g1	VF driver	See Table b.
20 21 22 23	D2-8 D2-4 D2-2 D2-1	7 segment decoder(2nd digit)	a2~g2		
24 25 26 27	D3-8 D3-4 D3-2 D3-1	7 segment decoder(3rd digit)	a3~g3		
28	LD8	Flag(LED)	LD8	LED driver	"0" : OFF "1" : ON
29	LD7		LD7		
30	LD6		LD6		
31	LD5		LD5		
32	LD4		LD4		
33	LD3		LD3		
34	LD2		LD2		
35	LD1(LSB)		LD1		

Note : "No." indicates the output number of the shift register. The first bit for data transfer is No. 1.

7 SEGMENT DECODER DISPLAY PATTERN

(Table b)

	Input data				Output							
	8	4	2	1	a	b	c	d	e	f	g	Display pattern
0	0	0	0	0	1	1	1	1	1	1	0	
1	0	0	0	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	0	1	1	0	0	1	1	
5	0	1	0	1	1	0	1	1	0	1	1	
6	0	1	1	0	1	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	0	0	1	0	
8	1	0	0	0	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	1	0	1	1	
A	1	0	1	0	1	1	1	0	1	1	1	
B	1	0	1	1	0	0	1	1	1	1	1	
C	1	1	0	0	1	0	0	1	1	1	0	
D	1	1	0	1	0	1	1	1	1	0	1	
E	1	1	1	0	1	0	0	1	1	1	1	
F	1	1	1	1	0	0	0	0	0	0	0	Blank

FUNCTIONAL DESCRIPTION

- DATA IN, CLOCK, LOAD : Data set input terminals

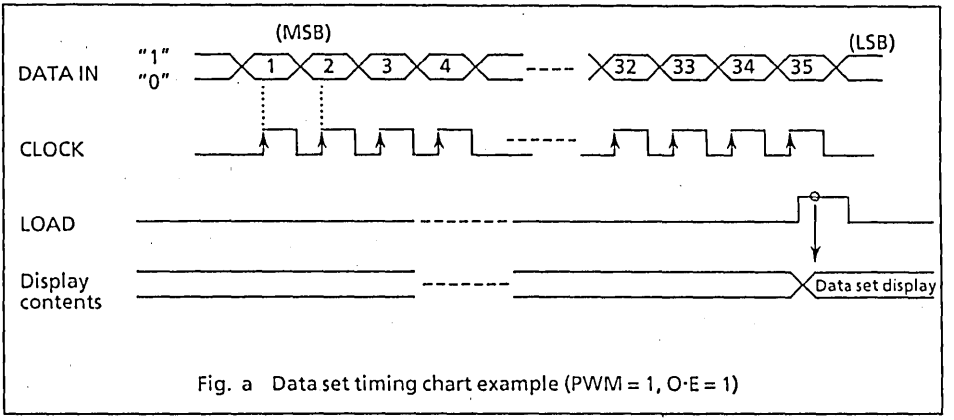


Fig. a Data set timing chart example (PWM = 1, O·E = 1)

DATA IN is a data input terminal, which is read into the internal shift register at the leading edge of the clock input terminal CLOCK.

LOAD is a load input terminal, which loads data of the shift register, data of 35 bits at a time, into the latch circuit. The timing chart above shows that, when a pulse is input to the LOAD terminal after the data of 35 bits is input, the display data is changed to a new one.

- DATA OUT : Data output terminal

DATA OUT is a terminal for cascade connection, the output of which is connected to the DATA IN terminal on the next stage.

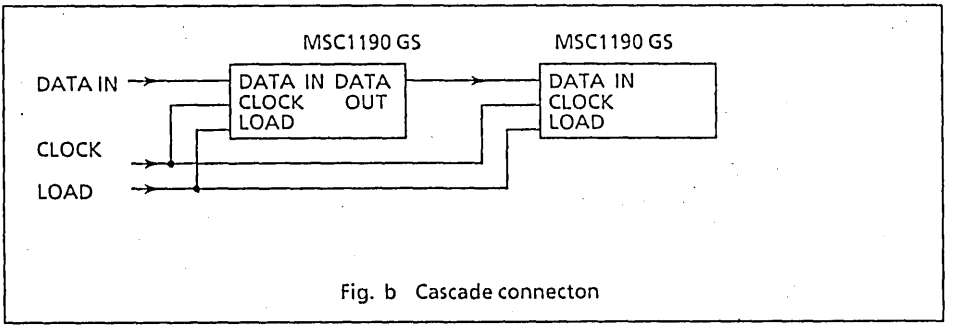


Fig. b Cascade connecton

• OSC : Oscillation terminal

OSC is a capacitor (C) and resistor (R) connection terminal of the oscillation circuit for dimming control. The oscillation frequency depends on the values of the external capacitor (C) and resistor (R).

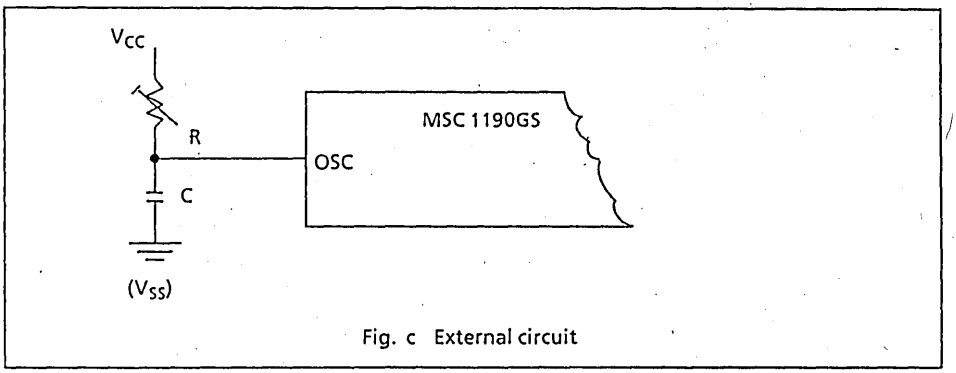


Fig. c External circuit

The value for R should not be less than 30 kΩ. The oscillation frequency f_{OSC} is expressed by the following equaton:

$$f_{OSC} = \frac{k}{C \cdot R} \quad (k \doteqdot 5)$$

When no oscillation circuit is used (i.e the PWM OUT terminal is not used), connect the OSC terminal to V_{SS}.

• LIGHT SW : Light switch input terminal

LIGHT SW is an input terminal with a pull-up resistor, which controls the PWM OUT output waveform.(See Table c.)

• PWM OUT : PWM output terminal

PWM OUT is a dimming PWM output terminal. When this terminal is connected to the PWM IN input terminal, the display duty ratio can be changed to 1/1, 1/8, or 1/16. Table c is a function table. (Table c)

LIGHT SW input	MSB of data	Display duty ratio
Open or "H"	–	1/1
"L"	0	1/8
"L"	1	1/16

"H" ; V_{CC} level
"L" ; V_{SS} level
– don't care

The frequency of a PWM OUT output signal is $f_{OSC}/16$.

• PWM IN : PWM input terminal

PWM IN is a dimming PWM input terminal. If the input is made High when the O·E is High, the VF display is turned ON. If the input is made Low, the display is turned OFF.

Accondingly, when a signal at 100 to several 100s Hz (the duty ratio is variable) is input to the PWM IN terminal, the display brightness can be continuously controlled.

When the PWM OUT output is connected to the PWM IN terminal, the display duty ratio, as mentioned above, can be changed to one of the three values.

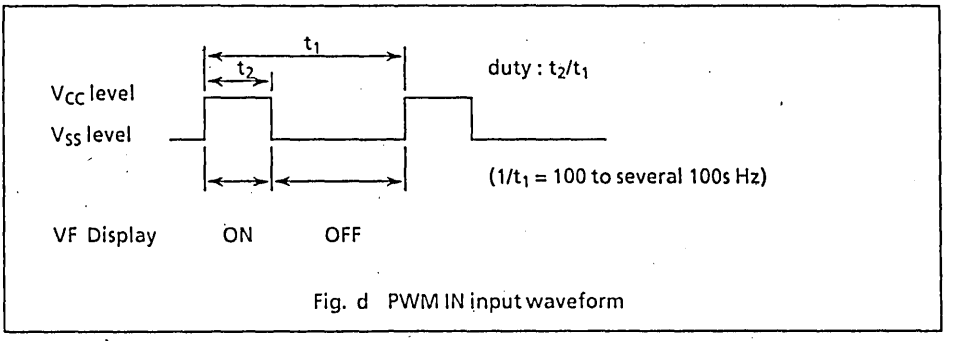


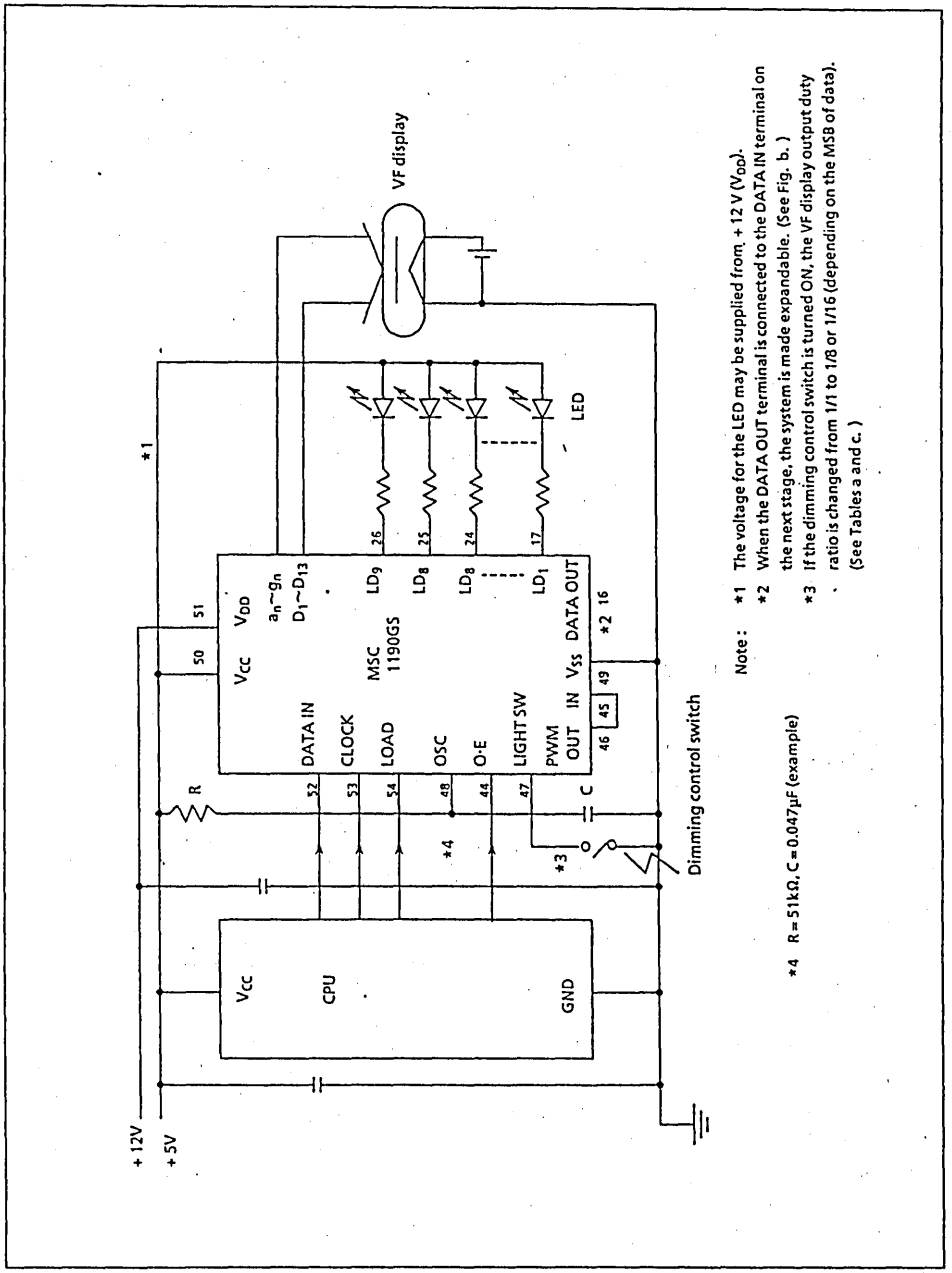
Fig. d PWM IN input waveform

• O·E : Display output enable input terminal

When the input is High, the display state is normal. When the input is Low, all displays are turned OFF.

IF the O·E is kept Low until the data of the latch circuit is determined when power is turned ON, unnecessary displays can be eliminated.

Two O·E and PWN IN input signals are ANDed in the IC to a PWM signal. The VF display is ON (normal) when PWM = "1" or OFF when PWM = "0". The LED display is turned ON or OFF by O·E input but not affected by PWM IN input.



Controller

OKI semiconductor

MSC7110-xx / MSC7112-xx

12-SEGMENT, 16-DIGIT / 16-SEGMENT, 12-DIGIT

GENERAL DESCRIPTION

The MSC7110-xx and MSC7112-xx are general purpose display controllers for vacuum fluorescent display tube.

The MSC7110-xx drives 12-segment bargraph or 7-segment plus comma and decimal point alphanumeric displays with up to 16 display positions, and drives 5 LEDs.

The MSC7112-xx drives 16-segment bargraph, 7-segment plus comma and decimal point or 16-segment alphanumeric displays with up to 12 display positions, and drives 5LEDs.

The controller accepts command and display data input words on a clocked serial input line.

Commands control the on/off duty cycle, starting character position, number of characters to be displayed and display modes (PLA mode, PLA bypass mode and LED mode).

Encoded data words display bargraph position (single segment or increasing length), characters, decimal point, comma and LEDs.

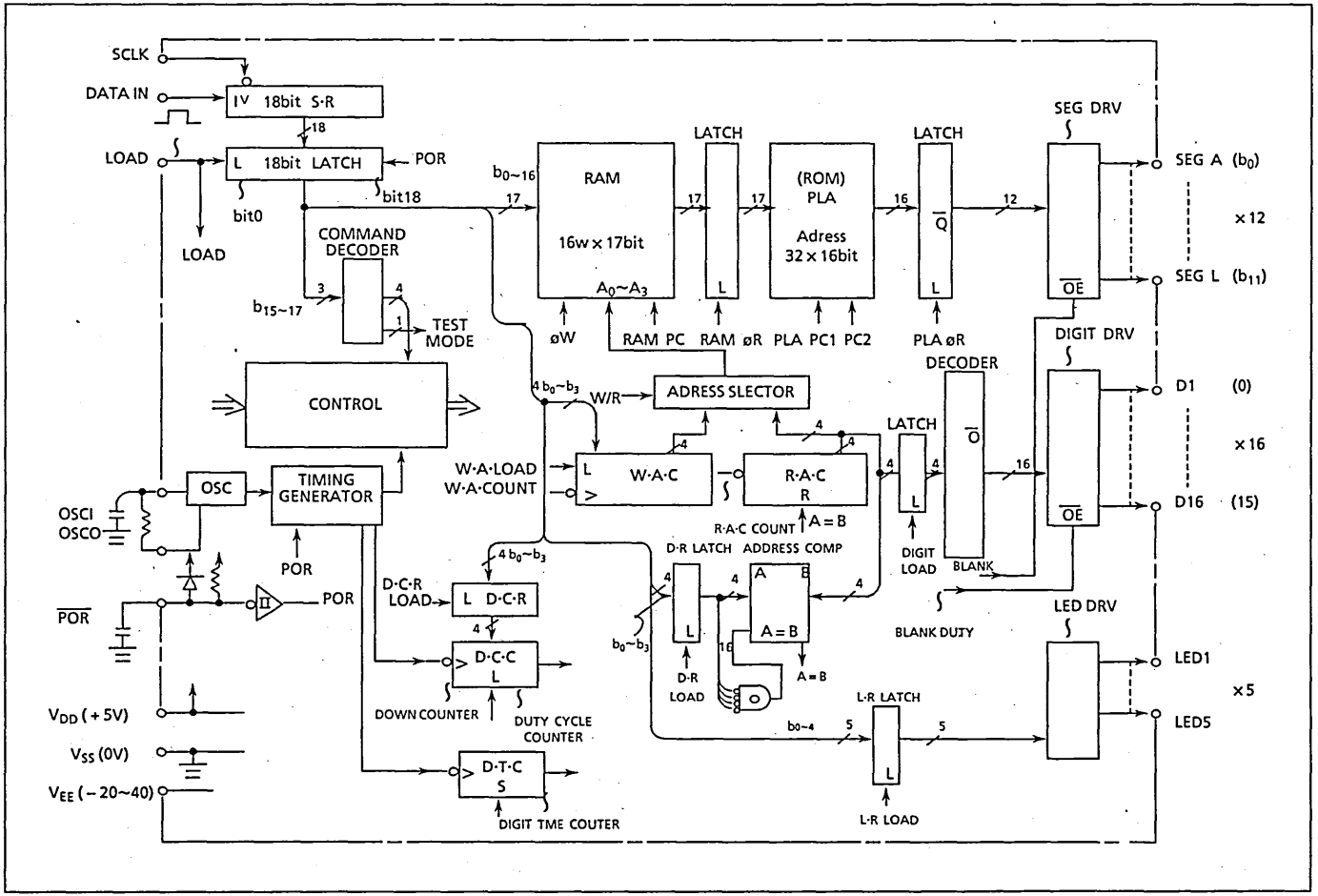
No external drive circuit is required for displays that operate on 40mA of drive current up to 45 volts.

A 32 x 16 bit PLA (ROM) code is programmable.

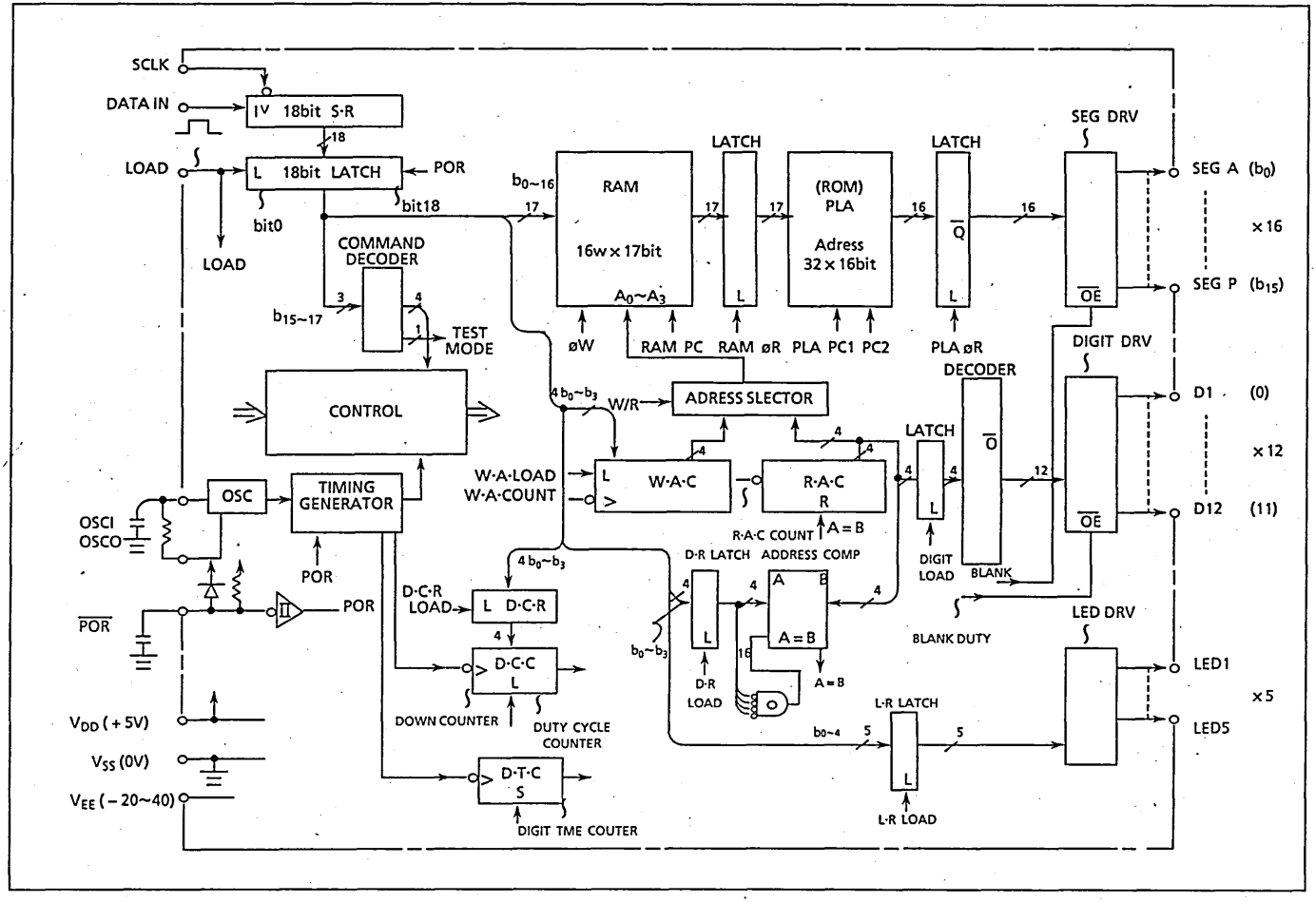
FEATURES

- Logic and LED driver supply voltage (V_{DD}) : +5V
- VF driver supply voltage (V_{EE}) : −40V
- Driver output current
  - VF grid driver (source) : −40mA
  - VF segment driver (source) : −6mA
  - LED driver (source) : −10mA
- Direct drive capability for vacuum fluorescent display
- 12 segment drivers (MSC7110-xx)
  16 segment drivers (MSC7112-xx)
- 16 digit drivers (MSC7110-xx)
  12 digit drivers (MSC7112-xx)
- 5 LED drivers
- Built-in oscillator circuit
- Built-in power-on-reset circuit with external C
- Serial host interface (data in, clock, load)
- Serial data input for 18-bit control and display data words

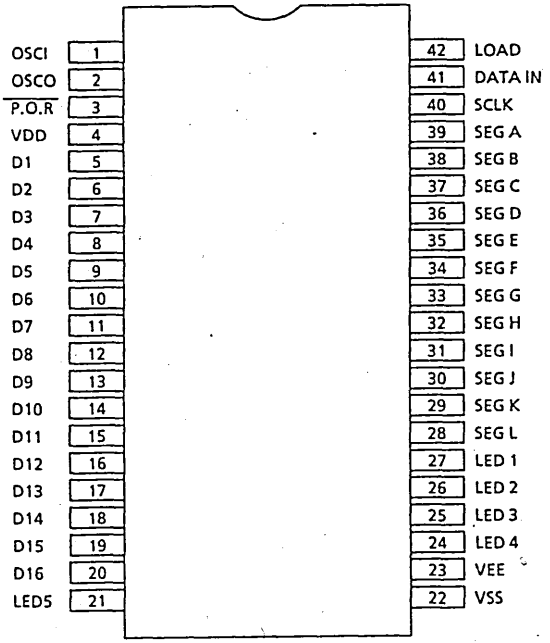
- Command functions
  - On/off duty cycle
  - Starting character position
    - : 1 to 16 (MSC7110-xx)
    - : 1 to 12 (MSC7112-xx)
  - Number of characters
    - : 1 to 16 (MSC7110-xx)
    - : 1 to 12 (MSC7112-xx)
  - 3-display modes
    - PLA mode, PLA bypass mode and LED mode
- 32 x 16 bit PLA provides data decoding to drive
  - 1 to 12 bargraph segments
  - Any 1 of 12 bargraph segment
  - 7-segment plus comma and decimal point alphanumeric characters (MSC7110-xx)
  - 1 to 16 bargraph segment
  - Any 1 of 16 bargraph segment
  - 7-segment plus comma and decimal point alphanumeric characters
  - 14-segment alphanumeric characters (MSC7112-xx)
- The number of character decoded by PLA is 32
- Programmable PLA code
- 42 pin shrink DIP package/44 pin flat pacage


SCLK
DATA IN
18bit S·R
LOAD
18bit LATCH
POR
bit0
bit18
LOAD
COMMAND DECODER
TEST MODE
CONTROL
OSC
TIMING GENERATOR
OSCI
OSCO
POR
VDD (+5V)
VSS (0V)
VEE (−20~40)
RAM
16w×17bit
A0~A3
LATCH
(ROM) PLA
Adress 32×16bit
LATCH
SEG DRV
SEG A (b0)
×12
SEG L (b11)
øW
RAM PC
RAM øR
PLA PC1 PC2
PLA øR
DIGIT DRV
DECODER
D1 (0)
×16
D16 (15)
ADRESS SLECTOR
W/R
W·A·LOAD
W·A·COUNT
W·A·C
R·A·C
R·A·C COUNT
A=B
LATCH
DIGIT LOAD
BLANK
D·R LATCH
ADDRESS COMP
D·C·R LOAD
D·C·R
D·C·C
DOWN COUNTER
DUTY CYCLE COUNTER
D·R LOAD
BLANK DUTY
LED DRV
LED1
×5
LED5
L·R LATCH
L·R LOAD
D·T·C
DIGIT TME COUTER

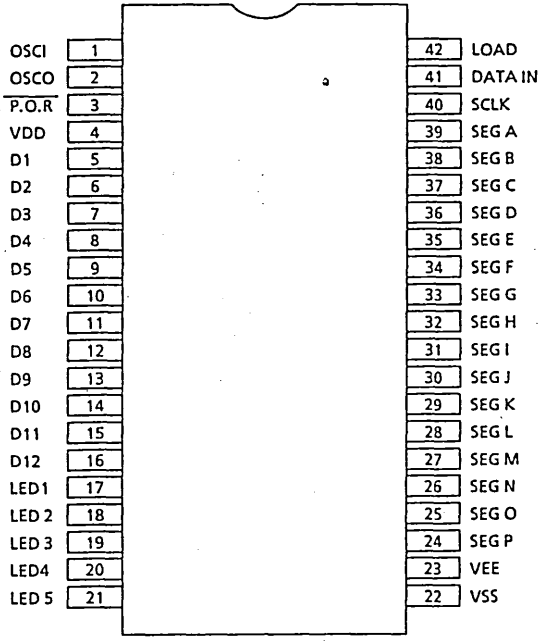
BLOCK DIAGRAM MSC7112-xx



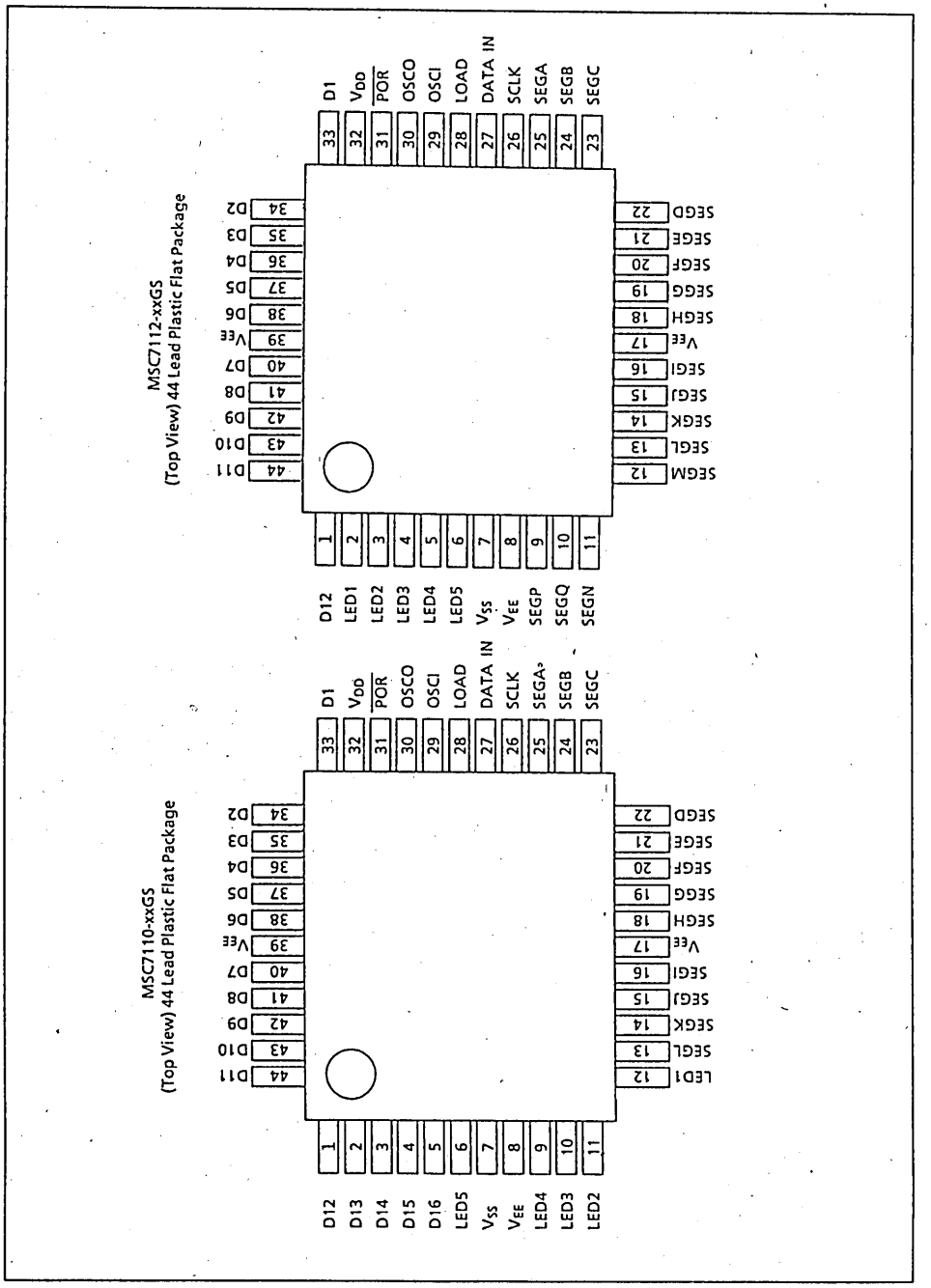
MSC7110-xxSS
(Top View) 42 Lead Plastic Shrink DIP



MSC7112-xxSS
(Top View) 42 Lead Plastic Shrink DIP



PIN CONFIGURATION



PIN DESCRIPTION

Terminal name	No. of terminals	Input, output	Connected to	Function
V_{DD} V_{SS} V_{EE}	1 1 1		Power source	V_{DD}-V_{SS} : Supply voltage for internal logic V_{DD}-V_{EE} : Supply voltage for VF driving circuit logic
DATA IN	1	Input	Microcomputer	Input shift register display data from the MSB (positive logic).
SCLK	1	Input	Microcomputer	Shift clock of the shift register. Data is shifted at the falling edge of SCLK.
LOAD	1	Input	Microcomputer	When the terminal is high, transfer of data from the shift register to the latch occurs.
$\overline{POR}$	1	Input Schmitt with pull-up register and diode		Internal logic reset input when power is turned on. When the terminal is Low, the 18-bit latch, the duty cycle register, the digit register, the LED register and the write/read address register are all reset. And the outputs of SEGA to SEGP (*a), D_1 to D_{12}(*b), and LED_1 to LED_5 are all turned off. When the terminal is connected to an external capacitor, the auto-power-on-reset function can be executed.
OSCI OSCO	1 1	Input Output		When an external resistor and a capacitor are connected, an oscillation circuit is formed. C = 100 pF, r = 47kΩ, f_{OSC} = 235 KHz ± 20%
SEGA~L SEGA~P	12*1 16*2	Output	Anode side of VF display tube	VF display tube driving output. The output is complementary.
D_1~D_{12} D_1~D_{16}	12*2 16*1	Output	Grid side of VF display tube	VF display tube driving output. The output is complementary.
LED1 ~LED5	5	Output	LED	LED driving output. The output is complementary.

*a SEGA to SEGL in case of MSC7110-xx
*b D_1 to D_{16} in case of MSC7110-xx
*1 In case of MSC7110-xx
*2 In case of MSC7112-xx

ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Limits	Unit
Supply voltage (1)	V_{DD}	—	−0.3~+6.5	V
Supply voltage (2)	$V_{DD}-V_{EE}$	—	0~50	V
Input voltage	V_I	—	$-0.3\sim V_{DD}+0.3$	V
Allowable loss	Pd	Ta≧25 °C	~500	mW
Storage temperature	t_{STg}	—	−55~+150	°C
Output current	I_{01}	All SEG output	−10	mA
	I_{02}	All digit output	−60	
	I_{03}	LED1~LED5	−20	

- **Operating Range**

Parameter	Symbol	Conditions	Limits	Unit
Supply voltage (1)	V_{DD}	—	4.5~5.5	V
Supply voltage (2)	$V_{DD}-V_{EE}$	—	25~45	V
Oscillation frequency	f_{OSC}	C=100pF R=47kΩ	235 ±20%	kHz
Operating temperature	T_{OP}	—	−20~+75	°C

• DC Characteristics

($V_{DD} - V_{EE} = 45V$, $V_{DD} = 5V \pm 10\%$, $Ta = -20 \sim +75°C$)

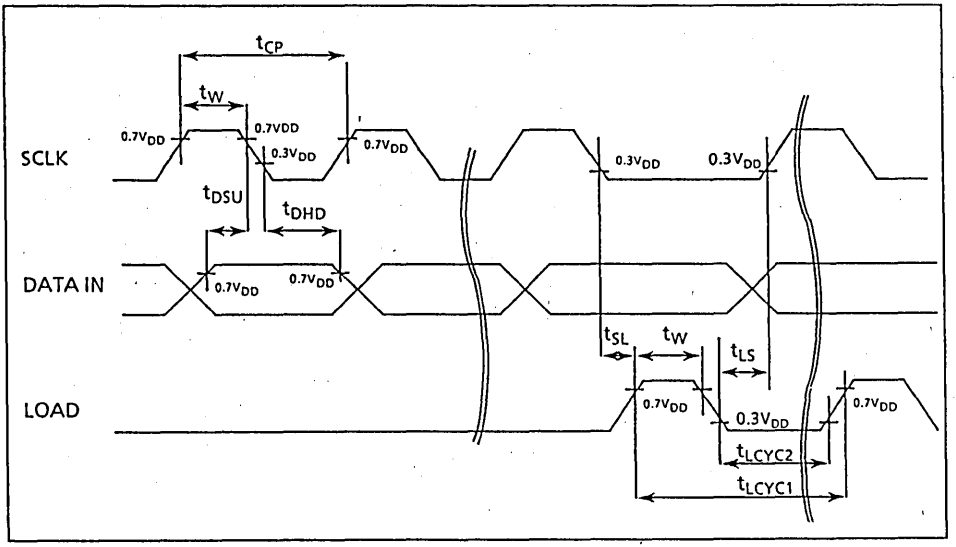
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Terminal
High level input voltage	V_{IH}	—	$0.7V_{DD}$	—	—	V	All input
Low level input voltage	V_{IL}	—	—	—	$0.3V_{DD}$	V	All input
High level input current	I_{IH}	$V_{DD} = 5.5V$ $V_I = V_{DD}$	—	—	1	μA	All input
Low level input current (1)	I_{IL1}	$V_{DD} = 5.5V$ $V_I = 0V$	—	—	−1	μA	All input except $\overline{POR}$
Low level input current (2)	I_{IL2}	$V_{DD} = 5.5V$ $V_I = 0V$	−27	−55	−110	μA	$\overline{POR}$
High level output voltage (1)	V_{OH1}	$V_{DD} = 4.5$ $I_{OH} = -6mA$	$V_{DD} - 2.2$	$V_{DD} - 1.5$	—	V	All SEG output
Low level output voltage (1)	V_{OL1}	$V_{DD} = 4.5$ $I_{OL} = 0.2mA$	—	$V_{EE} + 0.8$	$V_{EE} + 1.3$	V	All SEG output
High level output vltage (2)	V_{OH2}	$V_{DD} = 4.5$ $I_{OH} = -30mA$	$V_{DD} - 2.9$	$V_{DD} - 2.3$	—	V	All digit output
Low level output voltage (2)	V_{OL2}	$V_{DD} = 4.5$ $I_{OL} = 02.mA$	—	$V_{EE} + 0.8$	$V_{EE} + 1.3$	V	All digit output
High level input voltage (3)	V_{OH3}	$V_{DD} = 4.5$ $I_{OH} = -10mA$	$V_{DD} - 1.5$	—	—	V	LED1~ LED5
High level output voltage (3)	V_{OL3}	$V_{DD} = 4.5$ $I_{OL} = 0.1mA$	—	—	0.5	V	LED1~ LED5
Supply current	I_{DD}	$V_{DD} = 5.5V$ No load $f_{OSC} = 245kHz$	—	8.5	15	mA	

- **AC Characteristics**

V_{DD} = 5V ± 10% Ta = – 20~ + 75°C

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCLK cycle time	t_{CP}	—	. 2	—	—	µS
SCLK, LOAD pulse width	t_W	—	1	—	—	µS
Data setup time	t_{DSU}	—	500	—	—	nS
Data hold time	t_{DHD}	—	500	—	—	nS
SCLK-LOAD time	t_{SL}	—	2	—	—	µS
LOAD-SCLK time	t_{LS}	—	2	—	—	µS
LOAD cycle time 1	t_{LCYC1}	f_{OSC} = 245kHz	205	—	—	µS
LOAD cycle time 2	t_{LCYC2}	f_{OSC} = 245kHz	200	—	—	µS

- **Timing Chart**



FUNCTIONAL DESCRIPTION

• LED display

Display data is output to the LED1 to LED5 terminals in correspondence with each bit by executing the L. R LOAD command. Input data uses positive logic. When the data is 1, the LED lights. When the data is 0, the LED goes off.

• VF display (PLA (ROM) used)

Set optional data in the digit register and the duty register, and execute the W. A. C LOAD command to set the display digit position. Execute the PLA (ROM) DISPLAY command to write the display character address (PLA (ROM) address) in the RAM. The write address counter is incremented by one. The write address counter counts sequentially 0, 1, 2, -----, 14, 15, 0, 1, ----- regardless of the value of the digit register.

The segment code (ROM code) corresponding to the PLA (ROM) address is a user option.

• VF display (RAM direct display)

Set optional data in the digit resister and the duty register, and execute the W. A. C LOAD command to set the display digit position. Execute the DATA DISPLAY command to write the b_0 to b_{15} (*1) display data in the RAM. The write address counter is incremented by one. The write address counter counts sequentially 0, 1, 2, -----, 14, 15, 0, 1, ----- regardless of the value of the digit register.

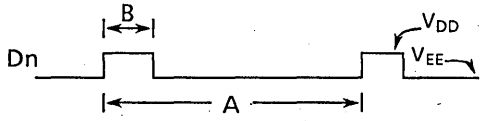
*1 : b_0 to b_{11} display data in case of MSC7110-xx.

• Brightness adjustment

The drightness can be adjusted by using the values of the duty cycle register and the digit register. The value of the duty cycle register changes the pulse width (B) at the D_1 to D_{16} output terminals, and the value of the digit register changes the cycle (A).

The table indicated below gives the relation between the value of the duty cycle register and the duty. When all the values of the duty cycle register are 0 (in the case of 16-digit display), the display is blank.

D. C. R				DUTY	D. C. R				DUTY	D. C. R				DUTY	D. C. R				DUTY
b_3	b_2	b_1	b_0	$\frac{B}{A}$	b_3	b_2	b_1	b_0	$\frac{B}{A}$	b_3	b_2	b_1	b_0	$\frac{B}{A}$	b_3	b_2	b_1	b_0	$\frac{B}{A}$
0	0	0	0	—	0	1	0	0	$\frac{16}{1024}$	1	0	0	0	$\frac{32}{1024}$	1	1	0	0	$\frac{48}{1024}$
0	0	0	1	$\frac{4}{1024}$	0	1	0	1	$\frac{20}{1024}$	1	0	0	1	$\frac{36}{1024}$	1	1	0	1	$\frac{52}{1024}$
0	0	1	0	$\frac{8}{1024}$	0	1	1	0	$\frac{24}{1024}$	1	0	1	0	$\frac{40}{1024}$	1	1	1	0	$\frac{56}{1024}$
0	0	1	1	$\frac{12}{1024}$	0	1	1	1	$\frac{28}{1024}$	1	0	1	1	$\frac{44}{1024}$	1	1	1	1	$\frac{60}{1024}$



$A = 64 \times n = 64 \times 16 = 1024$

n : Number of display digits

• Number of display digits

The number of display digits is set by the digit register. The number of display digits ranges from 1 to 16 (*1). The value of the digit register and the number of digits are as follows :

D. R				Control digit	D. R				Control digit	D. R				Control digit	D. R				Control digit
b_3	b_2	b_1	b_0		b_3	b_2	b_1	b_0		b_3	b_2	b_1	b_0		b_3	b_2	b_1	b_0	
0	0	0	0	*2 D_1~D_{16}	0	1	0	0	D_1~D_4	1	0	0	0	D_1~D_8	1	1	0	0	D_1~D_{12}
0	0	0	1	D_1~D_1	0	1	0	1	D_1~D_5	1	0	0	1	D_1~D_9	1	1	0	1	*2 D_1~D_{13}
0	0	1	0	D_1~D_2	0	1	1	0	D_1~D_6	1	0	1	0	D_1~D_{10}	1	1	1	0	*2 D_1~D_{14}
0	0	1	1	D_1~D_3	0	1	1	1	D_1~D_7	1	0	1	1	D_1~D_{11}	1	1	1	1	*2 D_1~D_{15}

*1 : 1 to 12 digita in the case of the MSC7112-xx
*2 : Ignored in the case of the MSC7112-xx

Command	Function	Input data																	
		MSB b_{17}	b_{16}	b_{15}	b_{14}	b_{13}	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	LSB b_0
DATA DISPLAY	The RAM data is output directly to the SEGA to SEGP terminals. (Positive logic)	0	0	*1 SEGP	*1 SEGO	*2 SEGN	*3 SEGM	SEGL	SEGK	SEGJ	SEGI	SEGH	SEGG	SEGF	SEGE	SEGD	SEGC	SEGB	SEGA
PLA DISPLAY	The RAM data is converted in code by the PLA and output to the SEGA to SEGP terminals. (Positive logic) *2	0	1	×	×	×	×	×	×	×	×	×	×	×	2^4	2^3	2^2	2^1	2^0
L. R LOAD	Display data is set in the LED register and output to the LED1 to LED5 terminals. (Positive logic)	1	0	0	×	×	×	×	×	×	×	×	×	×	LED5	LED4	LED3	LED2	LED1
D. R LOAD	The number of digits is set in the digit register.	1	0	1	0	×	×	×	×	×	×	×	×	×	×	2^3	2^2	2^1	2^0
W. A. CLOAD	The write address is set in the write address counter. (The write position is set.)	1	1	0	×	×	×	×	×	×	×	×	×	×	×	2^3	2^2	2^1	2^0
D. C. R LOAD	The duty value is set in the duty cycle register.	1	1	1	×	×	×	×	×	×	×	×	×	×	×	2^3	2^2	2^1	2^0
TEST LOAD MODE	The TEST mode is set.	1	0	1	1	×	×	×	×	×	×	×	×	×	×	×	×	×	×

*1 : Ignored in case of MSC7110-xx

*2 : Output to the SEGA to SEGL terminals in case of MSC7110-xx

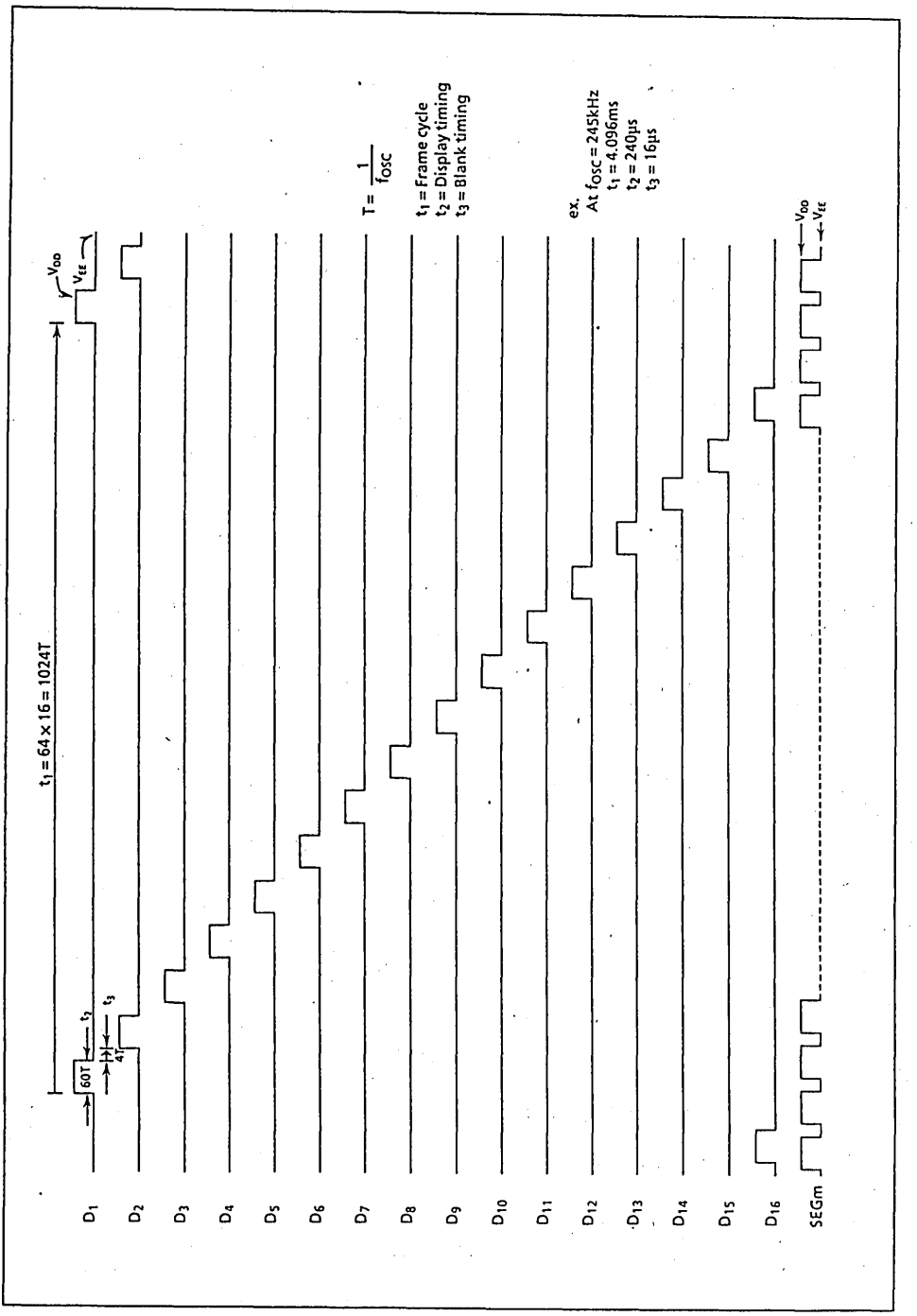
× : Don't Care

Relation between write address and digit output

Write address count	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Corresponding digit output	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	*1 D_{13}	*1 D_{14}	*1 D_{15}	*1 D_{16}

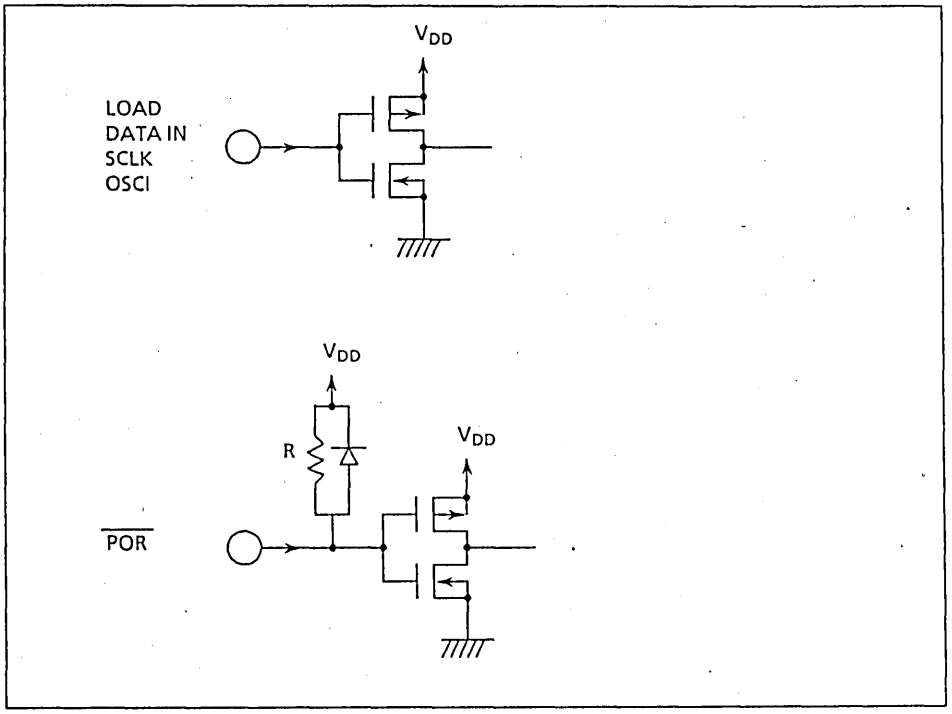
*1 : Ignored in case of MSC7112-xx

- **Digit timing chart (Display 16 digits in length)**

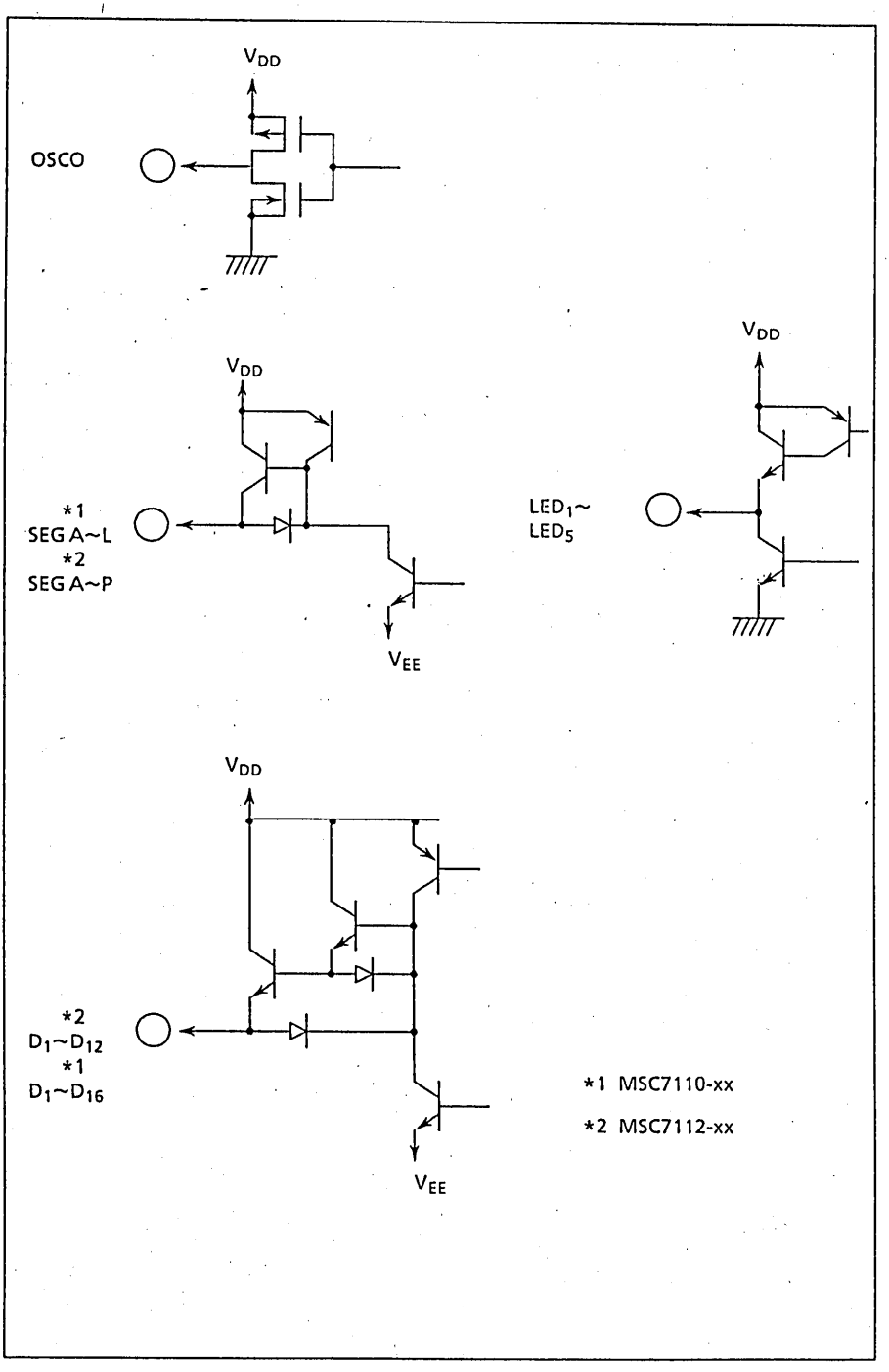


SCHEMATIC DIAGRAMS OF INPUT AND OUTPUT CIRCUIT

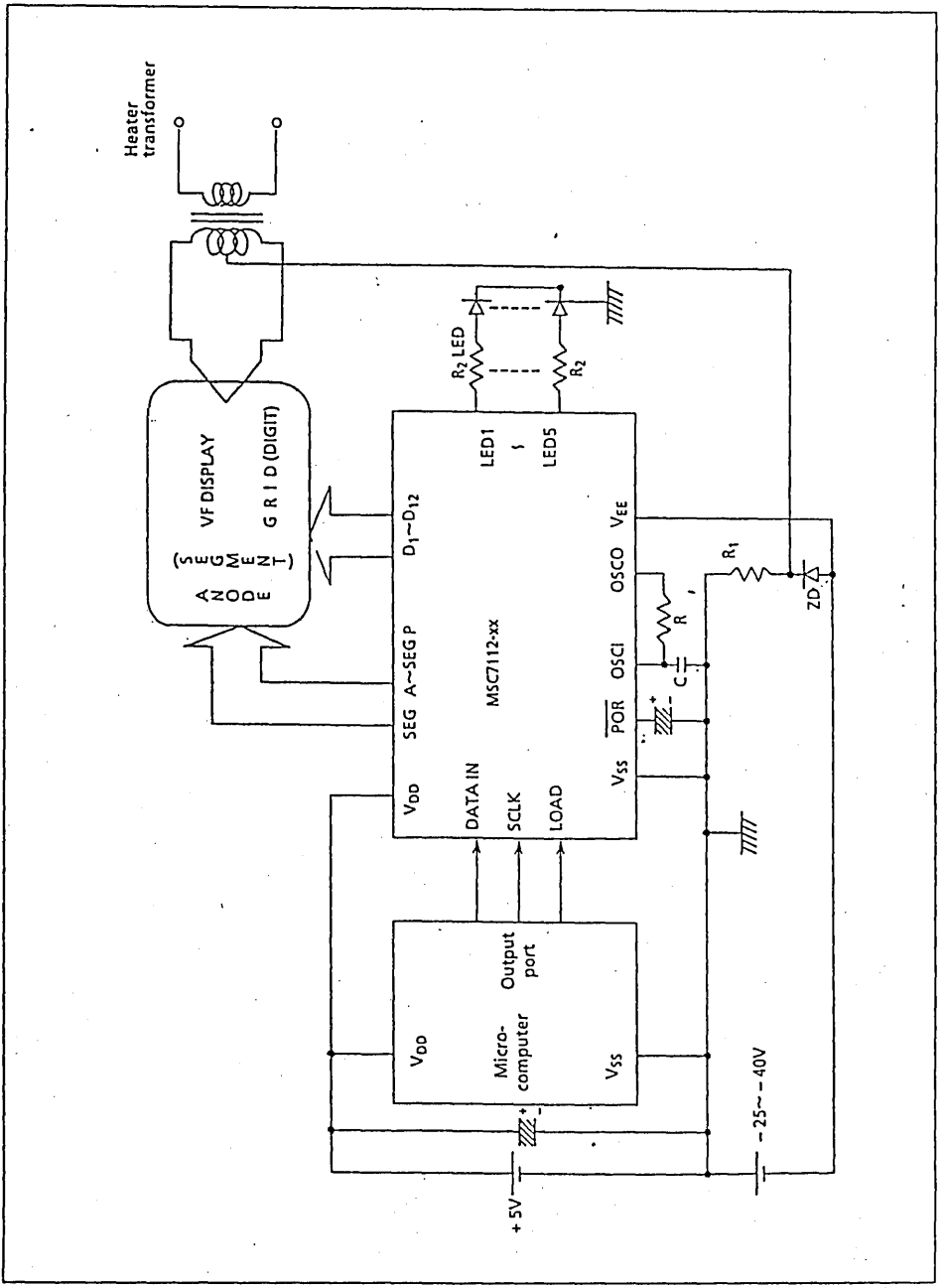
- Input terminal



- **Output terminal**



APPLICATION NOTE (MSM7112-xx)



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OKI semiconductor
MSC1937-01

16-SEGMENT, 16-DIGIT (ALPHANUMERIC)

GENERAL DESCRIPTION

MSC1937-01 is a Bi-COMS alphanumeric display controller designed to interface with either vacuum fluorescent or LED type displays.

MSC1937-01 can drive displays with up to 16 digits with either 14 or 16 segments plus a decimal point and commatail.

MSC1937-01 adopts a serial interface system, which allows data transfer from the CPU of microcomputer only by two signal lines.

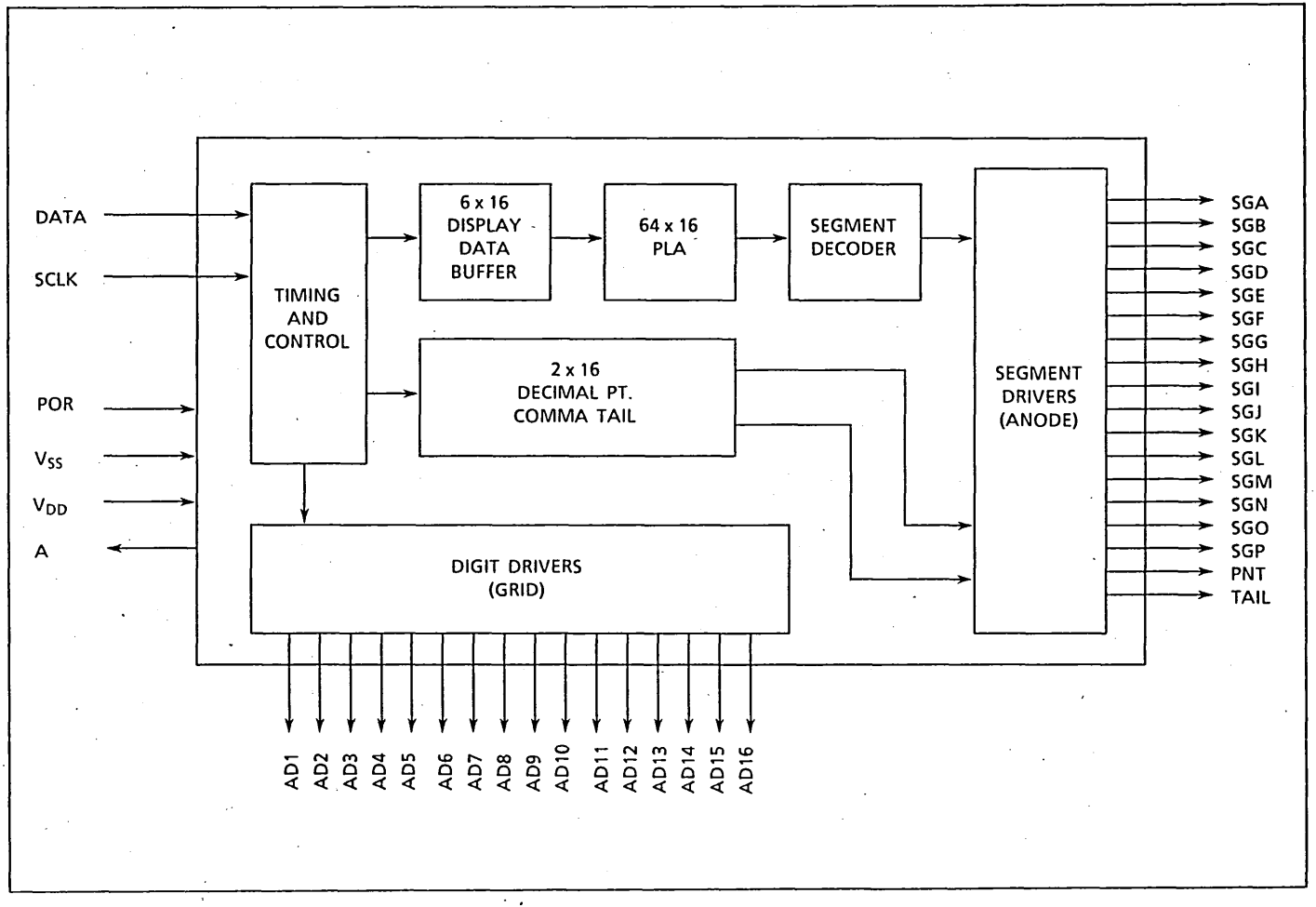
FEATURES

- Provides the interface with the microcomputer by DATA and SCLK.
- Can display up to 16 digits with either 14 or 16 segments plus comma/point.
- The number of display digits is programmable within 16.
- The brightness adjustment is programmable by 1/32 step.
- The display contents can be changed at any digit.
- Built-in PLA (64 types of ASCII characters (capital letters only)).
- Data transfer speed: Up to 66 KHz
- Drive capability

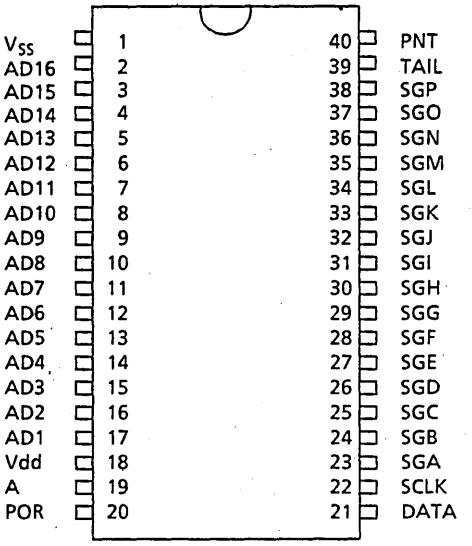
  Current : Up to – 20 mA (Digit)
  – 10 mA (Segment): DIP package
  – 5 mA (Segment): Flat package

  Output voltage : 58V
- Can be used for LED.
- Pin compatible with 10937 manufactured by Rockwell.
- Supply voltage: 5V ± 10%
- 40-pin plastic DIP package and 44-pin flat package

BLOCK DIAGRAM

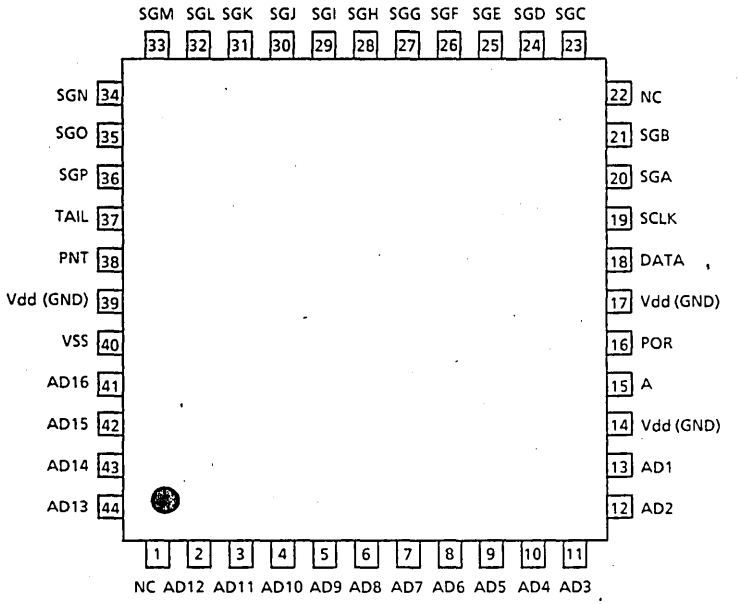


PIN CONFIGURATION



MSC1937-01RS
40 pin DIP PINOUT
(Top View)

PIN NO.	FUNCTION
1	Power supply (+ 5V)
2	Digit output terminal 16
⌇	⌇
17	Digit output terminal 1
18	GND
19	TEST terminal
20	POWER-ON-RESET terminal
21	Data input terminal
22	Shift clock terminal
23	Segment output terminal A
⌇	⌇
38	Segment output terminal P
39	TAIL output terminal
40	POINT output terminal



MSC1937-01GS-K
44 pin QFP PINOUT
(Top View)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	22	No connection
2	Digit output terminal 12	23	Segment output terminal C
⟆	⟆	⟆	⟆
13	Digit output terminal 1	36	Segment output terminal P
14	GND	37	TAIL output terminal
15	TEST terminal	38	POINT output terminal
16	POWER-ON-RESET terminal	39	GND
17	GND	40	Power supply (+ 5V)
18	Data input terminal	41	Digit output terminal 16
19	Shift clock terminal	⟆	⟆
20	Segment output terminal A	44	Digit output terminal 13
21	Segment output terminal B		

PIN DESCRIPTION

Terminal Name	I/O	Function
V_{SS}		Power supply terminal.
V_{dd}		GND terminal.
DATA	I	Input of display data/control data. Input from MSB.
SCLK	I	Shift clock of shift register. Shifts data at the falling edge of SCLK.
POR	I	Power-on-reset input. Input of "H" level into this terminal with the power turned on initializes this IC. The internal state after the initialization is as follows: 1) AD1 to AD16, SGA to SGP, TAIL and PNT output are in the off state. 2) The duty cycle is set to "0". 3) The digit counter value is set to 16 digits. 4) The buffer counter is set to AD1. 5) Terminal "A" is in the output mode.
A	I/O	Usually used as an output mode, and outputs 1/5 of the internal oscillation frequency. In the test mode, operates as an input terminal.
AD16~ AD1	O	Grid output terminal. The output type ia an emitter follower.
SGA~SGP TAIL PNG	O	Segment output terminal. The output type is an emitter follower.

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Item		Symbol	Condition	Unit
Power supply voltage		V_{SS}	− 0.3 to 6.5	V
Input voltage		V_{in}	− 0.3 to V_{SS} + 0.3	V
Output voltage		V_{gg}	V_{SS} + 0.3 to V_{SS} − 58	V
Output current	Digit	I_{load}	− 20	mA
	Segment	I_{load}	− 10 (− 5 *1)	mA
Operating temperature		T_{op}	− 40 to 85	°C
Storage Temperature		T_{stg}	− 55 to 150	°C

*1 In case of flat package

• DC Characteristics (Ta = − 40 to 85°C, V_{SS} = 5V ± 10%)

Parameter		Symbol	Condition	Min	Max	Unit
Power supply voltage		V_{SS}		4.5	5.5	V
Power supply current		I_{SS}	NO LOAD		10.0	mA
Input voltage	"H" level	V_{ih}	DATA, SCLK, POR	3.6	V_{SS} + 0.3	V
	"L" level	V_{il}		0	1	V
Input leak current		I_{il}	DATA, SCLK, POR, VI = V_{SS} or 0V		± 10	µA
Output voltage			V_{SS} = 5V			
"H" output voltage		V_{oh1}	I_{load} = − 10mA (DIGIT STROBES)	3.0		V
"L" output voltage		V_{oh2}	I_{load} = − 10mA (− 5 mA *2) (SEGMENTS)	2.5		V
		V_{ol1}	*3	V_{SS} − 58		V
		V_{ol2}	*3	V_{SS} − 58		V
Output leak current		I_{out}			10	µA

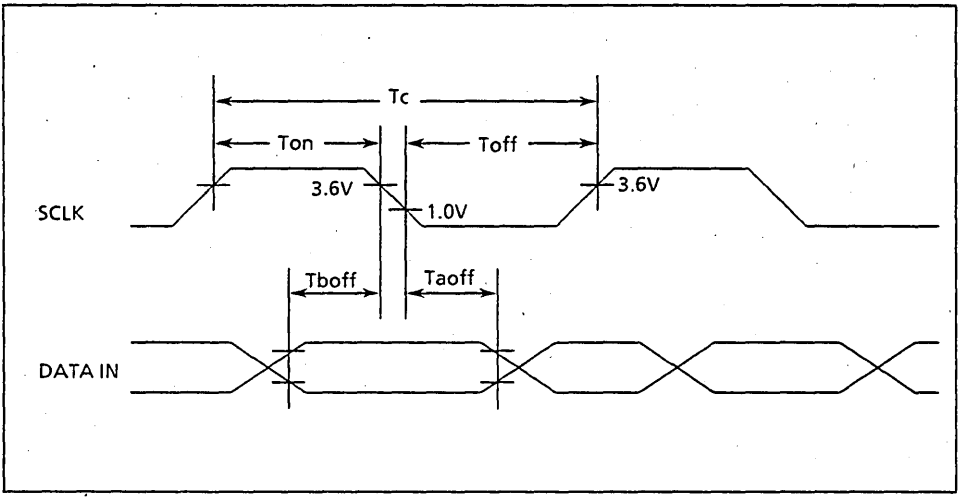
*2 In case of flat package
*3 "L" output voltage depends on the external PULL-DOWN resistor.

• AC Characteristics (Ta = − 40 to 85°C, V_{SS} = 5V ± 10%)

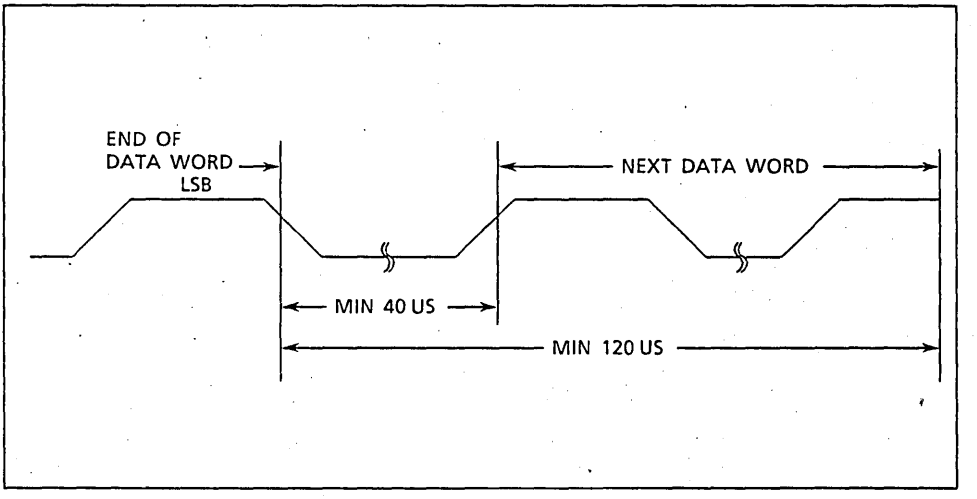
Parameter		Symbol	Condition	Min	Max	Unit
Internal clock frequency		T_{cyc}		58.8	22.1	µs
SCLK	"H" time	T_{on}		1.0	20.0	µs
	"L" time	T_{off}		1.0		µs
Data set up time		T_{boff}		200		ns
Hold time		T_{aoff}		100		ns

- **Timing Chart**

a) SCLK and Data Timing



b) Data Word LSB/MSB Timing



FUNCTIONAL DESCRIPTION

The MSB value of 8-bit serial data determines whether the input data into MSC1937-01 is control data or display data.

• CONTROL DATA

The control data can be input by setting MSB to "1". In addition, a command type and associated data with the command is determined by the bit 6 to bit 0.

Command	Function	MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0
Buffer Pointer Control	Specifies the RAM address.	1	0	1	0	2^3	2^2	2^1	2^0
Digit Counter Control	Sets the number of display digits.	1	1	0	0	2^3	2^2	2^1	2^0
Duty Cycle Control	Sets the duty value.	1	1	1	2^4	2^3	2^2	2^1	2^0
TEST MODE	Sets the test mode.	1	0	0	2^0	X	X	X	X

X: Don't care

a) Buffer Pointer Control

This command changes the display contents only at an arbitrary digit. (The RAM write address is set.)
Adecimal equivallent value of bits 0 - 4 should be set (desired digit number – 2).

(Example) When specifying AD4, the set value is 2 (0010).

Specified digit	Set value of bits 0 to 4	Specified digit	Set value of bits 0 to 4
AD1	15 (1111)	AD9	7 (0111)
AD2	0 (0000)	AD10	8 (1000)
AD3	1 (0001)	AD11	9 (1001)
AD4	2 (0010)	AD12	10 (1010)
AD5	3 (0011)	AD13	11 (1011)
AD6	4 (0100)	AD14	12 (1100)
AD7	5 (0101)	AD15	13 (1101)
AD8	6 (0110)	AD16	14 (1110)

b) Digit Counter Control

This command sets the number of display digits.
Set the desired number of digits in bits 0 to 4.

Number of display digits	Set value of bits 0 to 4	Number of display digits	Set value of bit 0 to 4
1	1 (0001)	9	9 (1001)
2	2 (0010)	10	10 (1010)
3	3 (0011)	11	11 (1011)
4	4 (0100)	12	12 (1100)
5	5 (0101)	13	13 (1101)
6	6 (0110)	14	14 (1110)
7	7 (0111)	15	15 (1111)
8	8 (1000)	16	0 (0000)

c) Duty Cycle Control

This command sets the duty cycle of the driver output. This command allows the brightness to be adjusted by 1/32 step. As shown in Figure 1, the blank type between digits or between the segments is specified by 1 bit time on the hardware. Therefore, the set value ranges from 0 to 31.

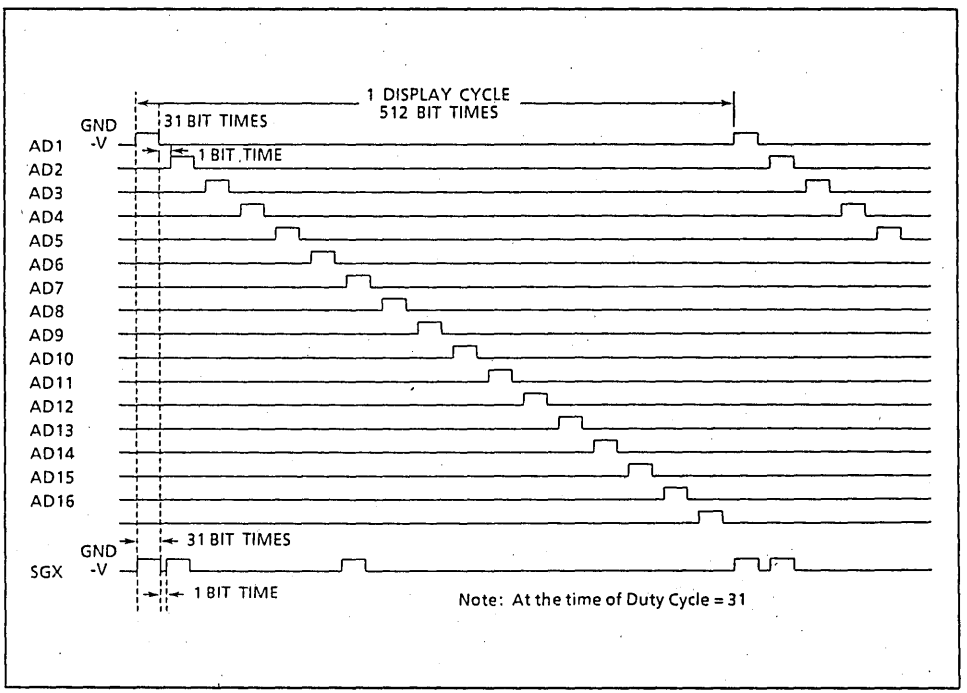


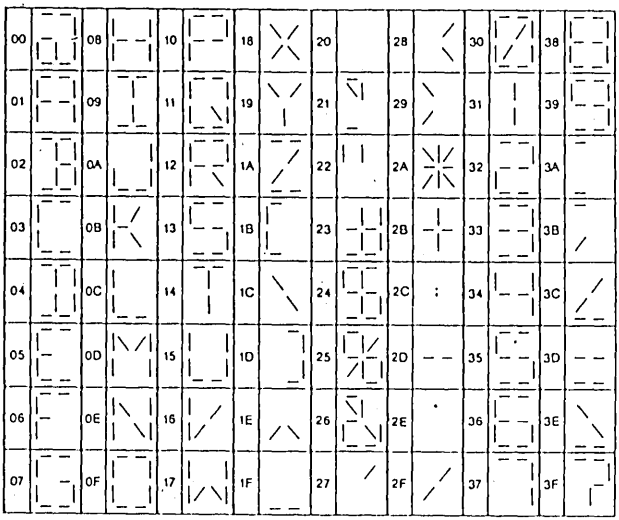
Figure 1 Output timing

d) TEST MODE

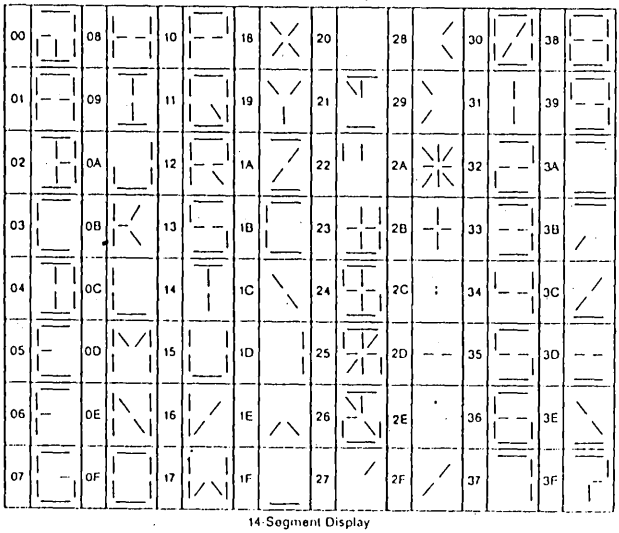
This mode is not a user function, but is used for outgoing inspection.

• DISPLAY DATA

By setting MSB = '0', the display data can be entered. The address of PLA is specified by bit 6 to bit 0 following MSB.
Table-1 provides the PLA code table.



16-Segment Display



14-Segment Display

Table-1 PLA Code Table

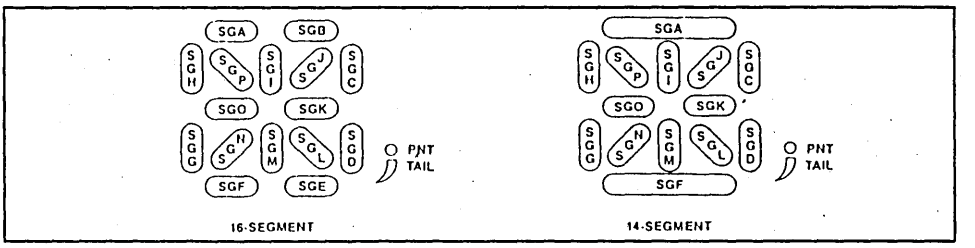
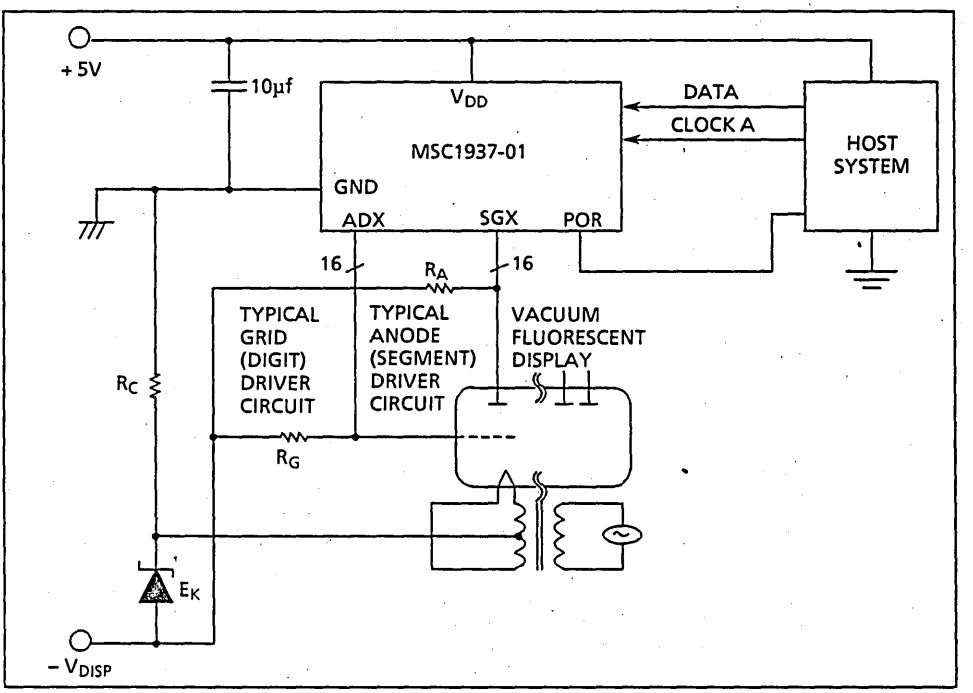


Fig.-1 Segment-Output Assignment

* To set the comma and point, the display data at the display digit is input, then 2C and 2E data are input.

(Note) Only when 2C and 2E data are entered, the write address in the RAM is not automatically incremented. For other data, the address specified by the Buffer Pointer Control command is automatically incremented by one each time the display dadta is input.

APPLICATION NOTE



OKI semiconductor
MSC1951-01

16-SEGMENT, 16-DIGIT (BARGRAPH and NUMERIC)

GENERAL DESCRIPTION

MSC1951-01 is a Bi-CMOS bargraph and alphanumeric display controller designed to interface with either vacuum fluorescent or LED displays.

MSC1951-01 can drive displays with up to 16 positions with either 16 segment bargraph or seven segment plus a decimal point and commatail.

MSC1951-01 adopts a serial interface system, which allows data transfer from the CPU of microcomputer only by two signal lines.

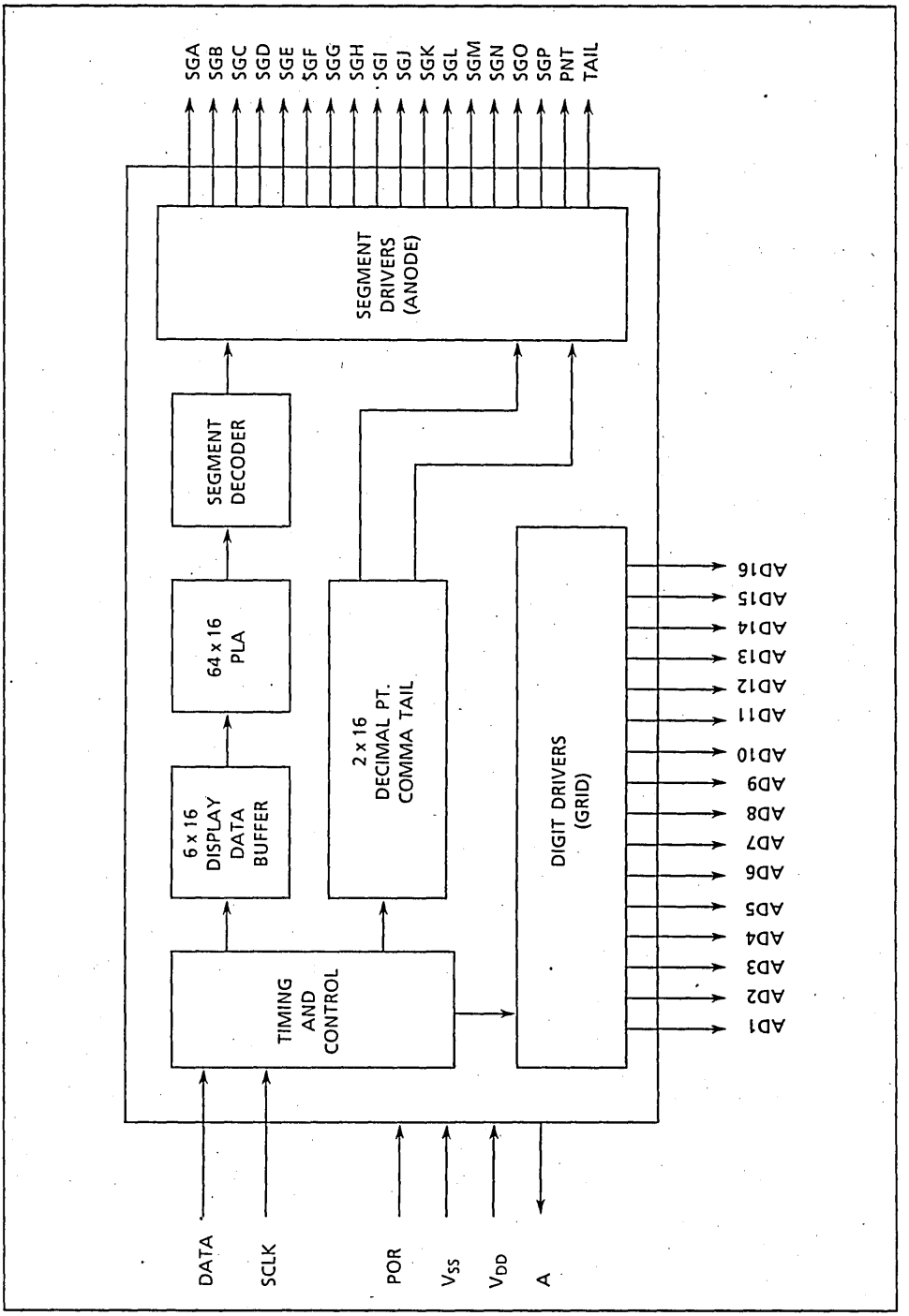
FEATURES

- Provides the interface with the microcomputer by DATA and SCLK.
- Can display up to 16 digits of 7-segment typed characters with comma/point or of 16-segment type bargraph.
- The number of display digits is programmable within 16.
- The brightness adjustment is programmable by 1/32 step.
- The display contents can be changed at any digit.
- Built-in PLA, alphanumeric characters, e.g., 0 to 9, A, C, E, F, P, L (capital letters), b, and d (small letters) can be displayed. In addition, 16-segment dot display and bar display are allowed.
- Data transfer speed: Up to 66 KHz
- Drive capability

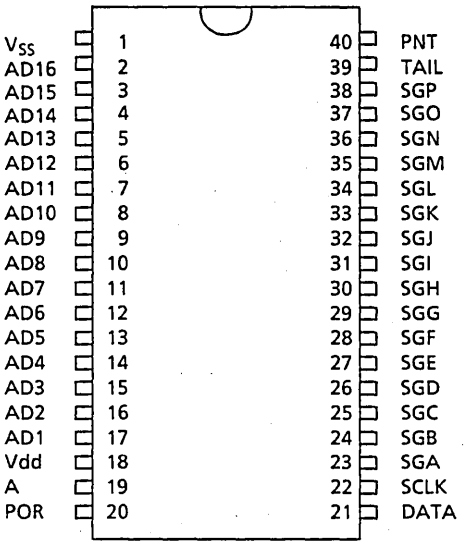
  Current : Up to – 20 mA (Digit)
  – 10 mA (Segment): DIP package
  – 5 mA (Segment): Flat package

  Output voltage : 58V
- Can be used for LED.
- Pin compatible with 10951 manufactured by Rockwell.
- Supply voltage: 5V ± 10%
- 40-pin plastic DIP package and 44-pin flat package

BLOCK DIAGRAM

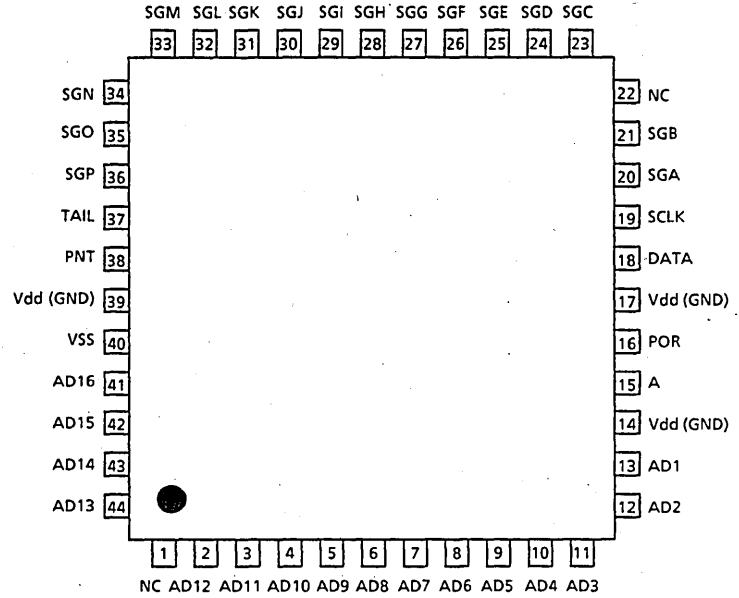


PIN CONFIGURATION



MSC1951-01RS
40 pin DIP PINOUT
(Top View)

PIN NO.	FUNCTION
1	Power supply (+ 5V)
2	Digit output terminal 16
⌇	⌇
17	Digit output terminal 1
18	GND
19	TEST terminal
20	POWER-ON -ESET terminal
21	Data input terminal
22	Shift clock terminal
23	Segment output terminal A
⌇	⌇
38	Segment output terminal P
39	TAIL output terminal
40	POINT output terminal



MSC1951-01GS-K
44 pin QFP PINOUT
(Top View)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	22	No connection
2	Digit output terminal 12	23	Segment output terminal C
⟆	⟆	⟆	⟆
13	Digit output terminal 1	36	Segment output terminal P
14	GND	37	TAIL output terminal
15	TEST terminal	38	POINT output terminal
16	POWER-ON-RESET terminal	39	GND
17	GND	40	Power supply (+ 5V)
18	Data input terminal	41	Digit output terminal 16
19	Shift clock terminal	⟆	⟆
20	Segment output terminal A	44	Digit output terminal 13
21	Segment output terminal B		

PIN DESCRIPTION

Terminal Name	I/O	Function
V_{SS}		Power supply terminal.
V_{dd}		GND terminal.
DATA	I	Input of display data/control data. Input from MSB.
SCLK	I	Shift clock of shift register. Shifts data at the falling edge of SCLK.
POR	I	Power-on-reset input. Input of "H" level into this terminal with the power turned on initializes this IC. The internal state after the initialization is as follows: 1) AD1 to AD16, SGA to SGP, TAIL and PNT output are in the off state. 2) The duty cycle is set to "0". 3) The digit counter value is set to 16 digits. 4) The buffer counter is set to AD1. 5) Terminal "A" is in the output mode.
A	I/O	Usually used as an output mode, and outputs 1/5 of the internal oscillation frequency. In the test mode, operates as an input terminal.
AD16~ AD1	O	Grid output terminal. The output format ia an emitter follower.
SGA~SGP TAIL PNG	O	Segment output terminal. The output format is an emitter follower.

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Item	Symbol	Condition	Unit
Power supply voltage	V_{SS}	− 0.3 to 6.5	V
Input voltage	V_{in}	− 0.3 to V_{SS} + 0.3	V
Output voltage	V_{gg}	V_{SS} + 0.3 to V_{SS} − 58	V
Output current Digit	I_{load}	− 20	mA
Segment	I_{load}	− 10 (− 5 *1)	mA
Operating temperature	T_{op}	− 40 to 85	°C
Storage Temperature	T_{stg}	− 55 to 150	°C

*1 In case of flat package

• DC Characteristics (Ta = − 40 to 85°C, V_{SS} = 5V ± 10%)

Parameter	Symbol	Condition	Min	Max	Unit
Power supply voltage	V_{SS}		4.5	5.5	V
Power supply current	I_{SS}	NO LOAD		10.0	mA
Input voltage "H" level	V_{ih}	DATA, SCLK, POR	3.6	V_{SS} + 0.3	V
"L" level	V_{il}		0	1	V
Input leak current	I_{il}	DATA, SCLK, POR, VI = V_{SS} or 0V		± 10	µA
Output voltage		V_{SS} = 5V			
"H" output voltage	V_{oh1}	I_{load} = − 10mA (DIGIT STROBES)	3.0		V
"L" output voltage	V_{oh2}	I_{load} = − 10mA (− 5 mA *2) (SEGMENTS)	2.5		V
	V_{ol1}	*3	V_{SS} − 58		V
	V_{ol2}	*3	V_{SS} − 58		V
Output leak current	I_{out}			10	µA

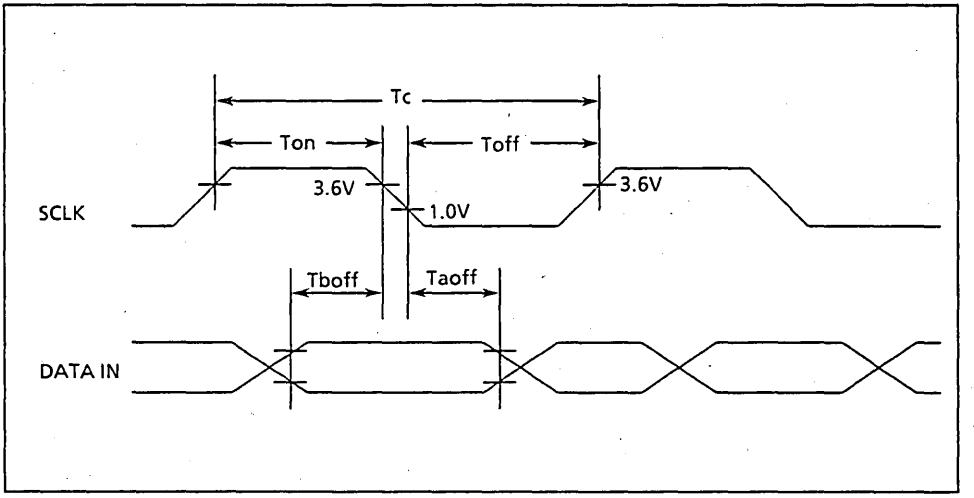
*2 In case of flat package
*3 "L" output voltage depends on the external PULL-DOWN resistor.

• AC Characteristics (Ta = − 40 to 85°C, V_{SS} = 5V ± 10%)

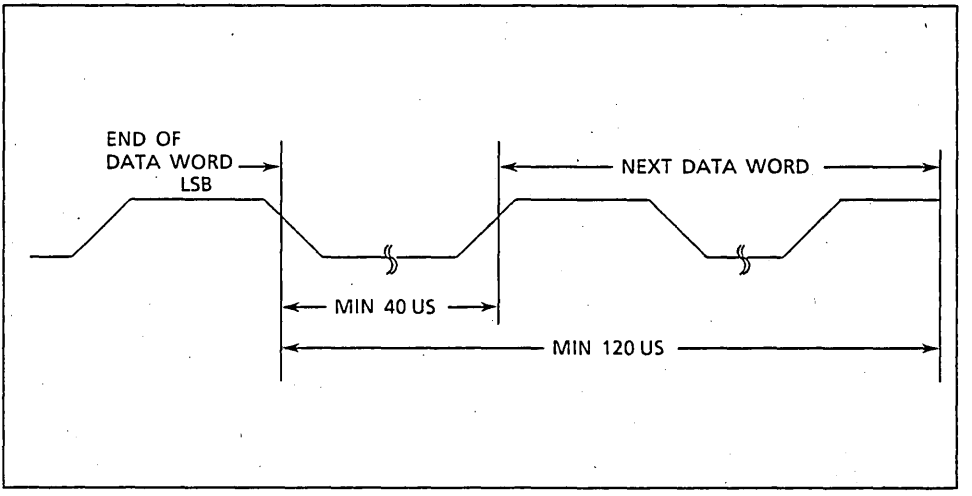
Parameter	Symbol	Condition	Min	Max	Unit
Internal clock frequency	T_{cyc}		58.8	22.1	µs
SCLK "H" time	T_{on}		1.0	20.0	µs
"L" time	T_{off}		1.0		µs
Data set up time	T_{boff}		200		ns
Hold time	T_{aoff}		100		ns

- **Timing chart**

a) SCLK and Data Timing



b) Data Word LSB/MSB Timing



FUNCTIONAL DESCRIPTION

The MSB value of 8-bit serial data determines whether the input data into MSC1951-01 is control data or display data.

• CONTROL DATA

The control data can be input by setting MSB to "1". In addition, a command type is determined by the bit 6 to bit 0 following MSB.

Command	Function	MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0
Buffer Pointer Control	Specifies the RAM address.	1	0	1	0	2^3	2^2	2^1	2^0
Digit Counter Control	Sets the number of display digits.	1	1	0	0	2^3	2^2	2^1	2^0
Duty Cycle Control	Sets the duty value.	1	1	1	2^4	2^3	2^2	2^1	2^0
TEST MODE	Sets the test mode.	1	0	0	2^0	X	X	X	X

X: Don't care

a) Buffer Pointer Control

This command changes the display contents only at an arbitrary digit. (The RAM write address is set.)
To input data into bits 0 to 4, set (desired digit – 2).

(Example) When specifying AD4, the set value is 2 (0010).

Specified digit	Set value of bits 0 to 4	Specified digit	Set value of bits 0 to 4
AD1	15 (1111)	AD9	7 (0111)
AD2	0 (0000)	AD10	8 (1000)
AD3	1 (0001)	AD11	9 (1001)
AD4	2 (0010)	AD12	10 (1010)
AD5	3 (0011)	AD13	11 (1011)
AD6	4 (0100)	AD14	12 (1100)
AD7	5 (0101)	AD15	13 (1101)
AD8	6 (0110)	AD16	14 (1110)

b) Digit Counter Control

This command sets the number of display digits.
Set the desired number of digits in bits 0 to 4.

Number of display digits	Set value of bits 0 to 4	Number of display digits	Set value of bit 0 to 4
1	1 (0001)	9	9 (1001)
2	2 (0010)	10	10 (1010)
3	3 (0011)	11	11 (1011)
4	4 (0100)	12	12 (1100)
5	5 (0101)	13	13 (1101)
6	6 (0110)	14	14 (1110)
7	7 (0111)	15	15 (1111)
8	8 (1000)	16	0 (0000)

c) Duty Cycle Control

This command sets the duty cycle of the driver output. This command allows the brightness to be adjusted by 1/32 step. As shown in Figure 1, the blank type between digits or between the segments is specified by 1 bit time on the hardware. Therefore, the set value ranges from 0 to 31.

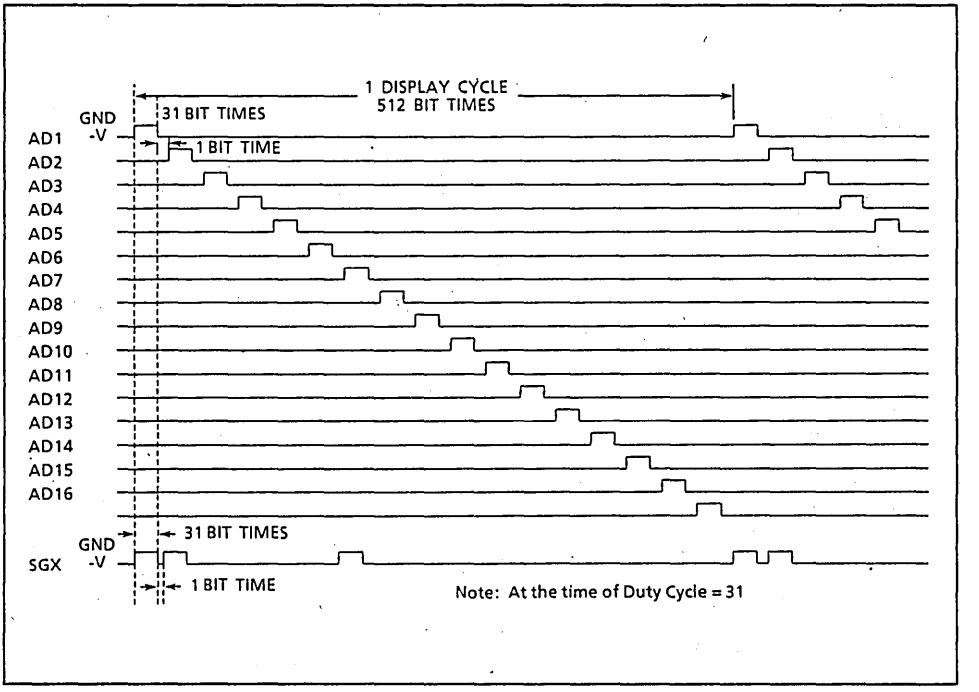


Figure 1 Output timing

d) TEST MODE

This mode is not a user function, but is used for outgoing inspection.

- **DISPLAY DATA**

By setting MSB = '0', the display data can be entered. The address of PLA is specified by bit 6 to bit 0 following MSB.
Table-1 provides the PLA code table.

Input Code								Function	Segment Driver Output Patterns (1 = On)																		
7	6	5	4	3	2	1	0		SGA	SGS	SGC	SGD	SGE	SGF	SGG	SGH	SGI	SGJ	SGK	SGL	SGM	SGN	SGO	SGP	PNT	TAIL	
0	X	0	0	0	0	0	0	Segment A On	1																		Any 1 of 16 Segments
0	X	0	0	0	0	0	1	Segment B On		1																	
0	X	0	0	0	0	1	0	Segment C On			1																
0	X	0	0	0	0	1	1	Segment D On				1															
0	X	0	0	0	1	0	0	Segment E On					1														
0	X	0	0	0	1	0	1	Segment F On						1													
0	X	0	0	0	1	1	0	Segment G On							1												
0	X	0	0	0	1	1	1	Segment H On								1											
0	X	0	0	1	0	0	0	Segment I On									1										
0	X	0	0	1	0	0	1	Segment J On										1									
0	X	0	0	1	0	1	0	Segment K On											1								
0	X	0	0	1	0	1	1	Segment L On												1							
0	X	0	0	1	1	0	0	Segment M On													1						
0	X	0	0	1	1	0	1	Segment N On														1					
0	X	0	0	1	1	1	0	Segment O On															1				
0	X	0	0	1	1	1	1	Segment P On																1			
0	X	0	1	0	0	0	0	Segment A On	1																		Bargraph Codes
0	X	0	1	0	0	0	1	Segment A & B On	1	1																	
0	X	0	1	0	0	1	0	Segment A-C On	1	1	1																
0	X	0	1	0	0	1	1	Segment A-D On	1	1	1	1															
0	X	0	1	0	1	0	0	Segment A-E On	1	1	1	1	1														
0	X	0	1	0	1	0	1	Segment A-F On	1	1	1	1	1	1													
0	X	0	1	0	1	1	0	Segment A-G On	1	1	1	1	1	1	1												
0	X	0	1	0	1	1	1	Segment A-H On	1	1	1	1	1	1	1	1											
0	X	0	1	1	0	0	0	Segment A-I On	1	1	1	1	1	1	1	1	1										1 to 16 Segments
0	X	0	1	1	0	0	1	Segment A-J On	1	1	1	1	1	1	1	1	1	1									
0	X	0	1	1	0	1	0	Segment A-K On	1	1	1	1	1	1	1	1	1	1	1								
0	X	0	1	1	0	1	1	Segment A-L On	1	1	1	1	1	1	1	1	1	1	1	1							
0	X	0	1	1	1	0	0	Segment A-M On	1	1	1	1	1	1	1	1	1	1	1	1	1						
0	X	0	1	1	1	0	1	Segment A-N On	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
0	X	0	1	1	1	1	0	Segment A-O On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
0	X	0	1	1	1	1	1	Segment A-P On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
0	X	1	0	0	0	0	0	Number 0	1	1	1	1	1	1		1	1	1	1	1							Alphanumeric and Special Codes
0	X	1	0	0	0	0	1	Number 1		1	1					1	1	1	1	1							
0	X	1	0	0	0	1	0	Number 2	1	1		1	1		1	1	1	1	1	1							
0	X	1	0	0	0	1	1	Number 3	1	1	1	1			1	1	1	1	1	1							
0	X	1	0	0	1	0	0	Number 4		1	1			1	1	1	1	1	1	1							
0	X	1	0	0	1	0	1	Number 5	1		1	1		1	1	1	1	1	1	1							
0	X	1	0	0	1	1	0	Number 6	1		1	1	1	1	1	1	1	1	1	1							
0	X	1	0	0	1	1	1	Number 7	1	1	1					1	1	1	1	1							
0	X	1	0	1	0	0	0	Number 8	1	1	1	1	1	1	1	1	1	1	1	1							
0	X	1	0	1	0	0	1	Number 9	1	1	1	1		1	1	1	1	1	1	1							
0	X	1	0	1	0	1	0	Letter P	1	1			1	1	1						1	1	1	1			
0	X	1	0	1	0	1	1	Letter L				1	1	1							1	1	1	1			
0	X	1	0	1	1	0	0	Comma								1	1	1	1	1					1*	1*	
0	X	1	0	1	1	0	1	Blank								1	1	1	1	1							
0	X	1	0	1	1	1	0	Decimal													1	1	1	1	1**		
0	X	1	0	1	1	1	1	Blank													1	1	1	1			
0	X	1	1	0	0	0	0	Number 0	1	1	1	1	1	1							1	1	1	1			
0	X	1	1	0	0	0	1	Number 1		1	1										1	1	1	1			
0	X	1	1	0	0	1	0	Number 2	1	1		1	1		1						1	1	1	1			
0	X	1	1	0	0	1	1	Number 3	1	1	1	1			1						1	1	1	1			
0	X	1	1	0	1	0	0	Number 4		1	1			1	1						1	1	1	1			
0	X	1	1	0	1	0	1	Number 5	1		1	1		1	1						1	1	1	1			
0	X	1	1	0	1	1	0	Number 6	1		1	1	1	1	1						1	1	1	1			
0	X	1	1	0	1	1	1	Number 7	1	1	1										1	1	1	1			
0	X	1	1	1	0	0	0	Number 8	1	1	1	1	1	1	1						1	1	1	1			
0	X	1	1	1	0	0	1	Number 9	1	1	1	1		1	1						1	1	1	1			
0	X	1	1	1	0	1	0	Letter A	1	1	1		1	1	1						1	1	1	1			
0	X	1	1	1	0	1	1	Letter B			1	1	1	1	1						1	1	1	1			
0	X	1	1	1	1	0	0	Letter C	1			1	1	1							1	1	1	1		1*	
0	X	1	1	1	1	0	1	Letter D		1	1	1	1		1						1	1	1	1			
0	X	1	1	1	1	1	0	Letter E	1			1	1	1	1						1	1	1	1			
0	X	1	1	1	1	1	1	Letter F	1				1	1	1						1	1	1	1			

Table-1 PLA Code Table

00		08		10		18		20		28		30		38	
01		09		11		19		21		29		31		39	
02		0A		12		1A		22		2A		32		3A	
03		0B		13		1B		23		2B		33		3B	
04		0C		14		1C		24		2C	;	34		3C	
05		0D		15		1D		25		2D		35		3D	
06		0E		16		1E		26		2E		36		3E	
07		0F		17		1F		27		2F		37		3F	

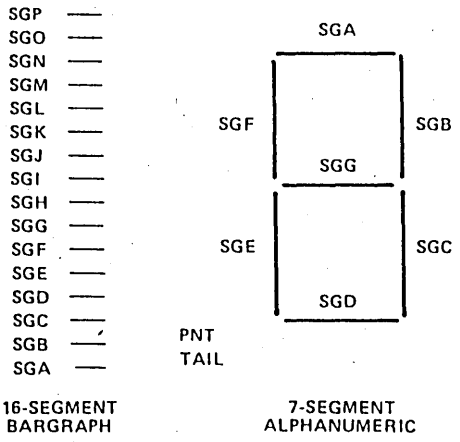


Table-2 PLA Code (At the time of 7-segment display)

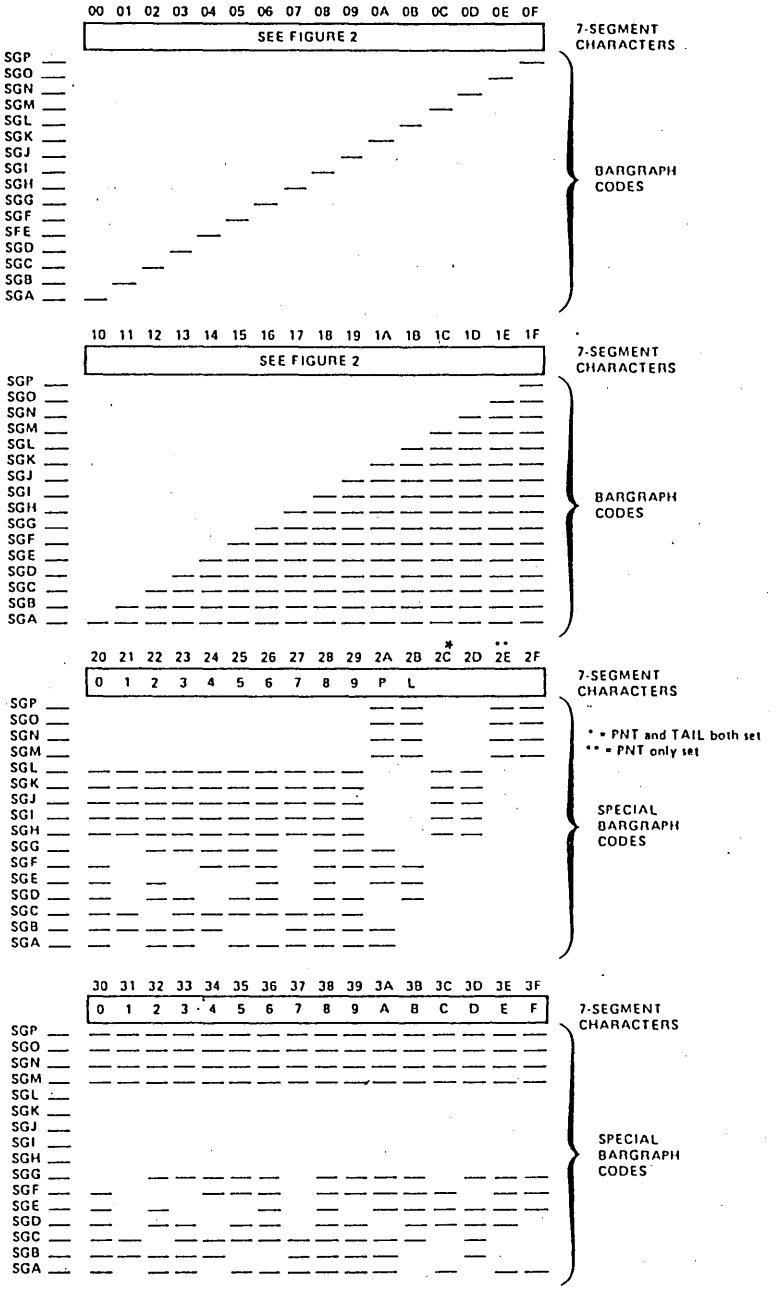
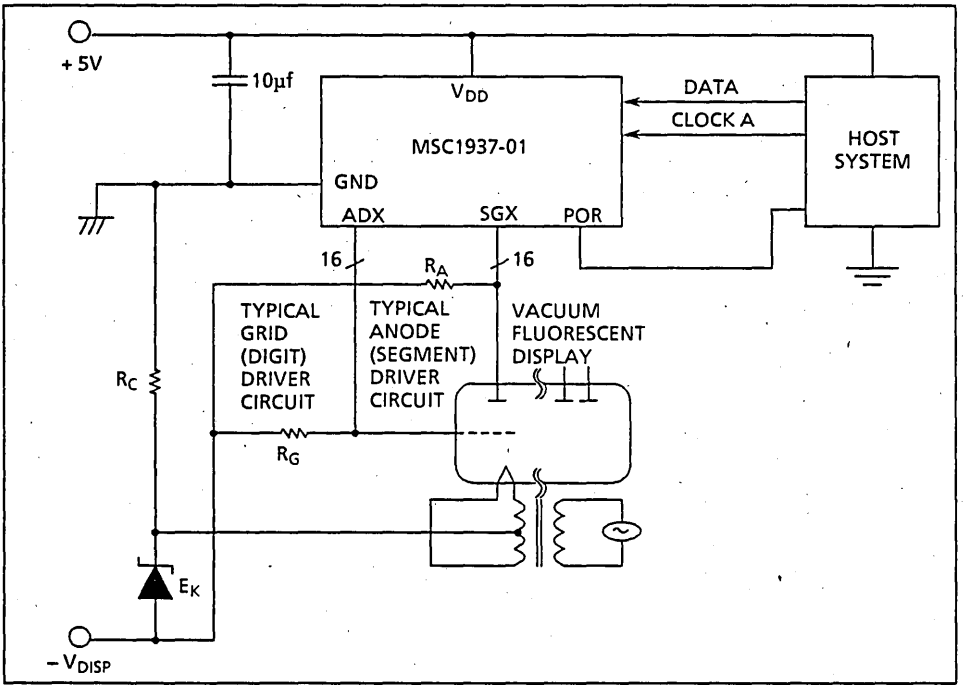


Table-3 PLA Code (At the time of bar display)

* To set the comma and point, the display data at the display digit is input, then 2C and 2E data are input.

(Note) Only when 2C and 2E data are entered, the write address in the RAM is not automatically incremented. For other data, the address specified by the Buffer Pointer Control command is automatically incremented by one each time the display dadta is input.

APPLICATION CIRCUIT



OKI semiconductor
MSC7125-XX

5 x 7 DOT MATRIX, 8-DIGIT

GENERAL DESCRIPTION

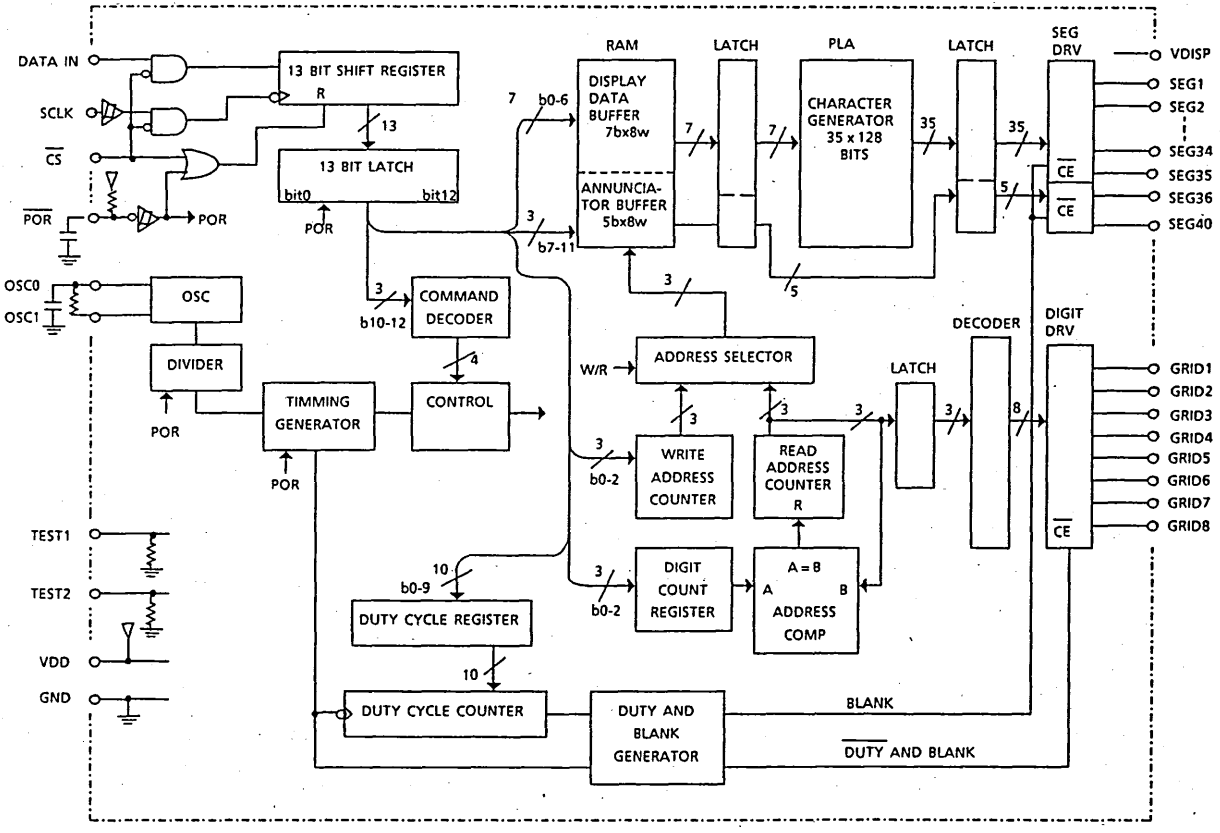
The MSC7125-XX is a BiCMOS dot matrix display controller for vacuum fluorescent display tube.

The MSC7125-XX drives displays with up to 8 grids with 35 anodes (dots) plus 5 annunciators. The controller receives the serial data (command and display data) consisted of 2 bytes (16 bits) on the high to low transition of the clock. The serial data entered into 16-bit shift register via DATA IN terminal is automatically latched after 2 bytes data input is completed. Commands control the on/off duty, starting character position, number of characters to display. An internal PLA-type character generator provides character decoding and dot pattern generation for 128 types of characters.

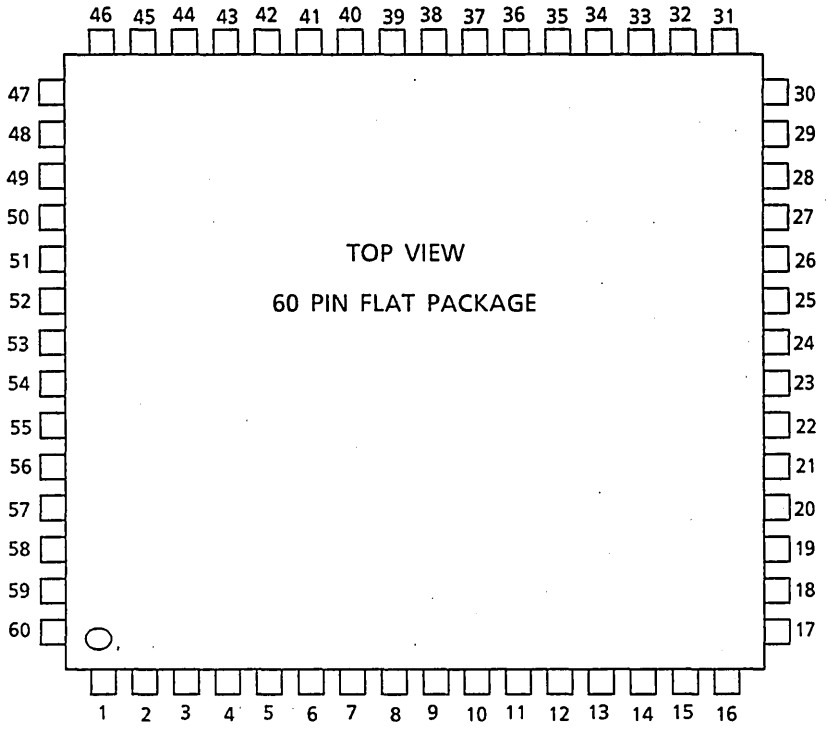
FEATURES

- Operating temperature : – 40°C ~ + 85°C
- Logic supply voltage (V_{DD}) : + 5V ± 10%
- Display voltage : + 50V max
- Driver output current : –31 mA (GRID 1, 8)
  –16 mA (GRID 2–7)
  –4.5 mA (SEG 36–40)
  –0.3 mA (SEG 1–35)
- Data transfer speed : 203KHz max
- Built-in oscillation circuit
- Built-in Power-on-reset circuit with external C
- Serial data input for 2 bytes (16 bits) control and display data
- Command functions : on/off duty cycle (1024 steps)
  starting character position (1 to 8)
  number of characters (1 to 8)
- Built-in PLA-type character generator : 128 types of characters (user programmable)
- 60 pin flat package

BLOCK DIAGRAM



PIN CONFIGURATION



1	V_{DISP}	16	SEG34	31	SEG18	46	SEG4
2	SEG31	17	GRID4	32	SEG17	47	SEG9
3	GRID6	18	GRID3	33	SEG16	48	SEG10
4	GRID5	19	SEG35	34	SEG15	49	SEG36
5	SEG26	20	SEG40	35	SEG14	50	SEG37
6	SEG32	21	SEG25	36	SEG13	51	$\overline{POR}$
7	SEG39	22	CRID2	37	SEG12	52	V_{DD}
8	SEG33	23	GND	38	SEG11	53	OSC1
9	SEG38	24	SEG24	39	SEG1	54	OSC0
10	SEG27	25	GRID1	40	SEG2	55	GND
11	GRID8	26	SEG23	41	SEG5	56	TEST1
12	SEG28	27	SEG22	42	SEG6	57	DATA IN
13	GRID7	28	SEG21	43	SEG7	58	SCLK
14	SEG29	29	SEG20	44	SEG8	59	$\overline{CS}$
15	SEG30	30	SEG19	45	SEG3	60	TEST2

PIN DESCRIPTION

PIN#	PIN NAME	DESCRIPTION	PIN#	PIN NAME	DESCRIPTION
1	VDISP	DISPLAY VOLTAGE	31	SEG18	ANODE18 DRIVER OUTPUT
2	SEG31	ANODE31 DRIVER OUTPUT	32	SEG17	ANODE17 DRIVER OUTPUT
3	GRID6	GRID6 DRIVER OUTPUT	33	SEG16	ANODE16 DRIVER OUTPUT
4	GRID5	GRID5 DRIVER OUTPUT	34	SEG15	ANODE15 DRIVER OUTPUT
5	SEG26	ANODE26 DRIVER OUTPUT	35	SEG14	ANODE14 DRIVER OUTPUT
6	SEG32	ANODE32 DRIVER OUTPUT	36	SEG13	ANODE13 DRIVER OUTPUT
7	SEG39	ANODE39 DRIVER OUTPUT	37	SEG12	ANODE12 DRIVER OUTPUT
8	SEG33	ANODE33 DRIVER OUTPUT	38	SEG11	ANODE11 DRIVER OUTPUT
9	SEG38	ANODE38 DEIVER OUTPUT	39	SEG1	ANODE1 DRIVER OUTPUT
10	SEG27	ANODE27 DRIVER OUTPUT	40	SEG2	ANODE2 DRIVER OUTPUT
11	GRID8	GRID8 DEIVER OUTPUT	41	SEG5	ANODE5 DRIVER OUTPUT
12	SEG28	ANODE28 DRIVER OUTPUT	42	SEG6	ANODE6 DRIVER OUTPUT
13	GRID7	GRID7 DRIVER OUTPUT	43	SEG7	ANODE7 DRIVER OUTPUT
14	SEG29	ANODE29 DRIVER OUTPUT	44	SEG8	ANODE8 DRIVER OUTPUT
15	SEG30	ANODE28 DRIVER OUTPUT	45	SEG3	ANODE3 DRIVER OUTPUT
16	SEG34	ANODE34 DRIVER OUTPUT	46	SEG4	ANODE4 DRIVER OUTPUT
16	GRID4	GRID4 DRIVER OUTPUT	47	SEG9	ANODE9 DRIVER OUTPUT
18	GRID3	GRID3 DRIVER OUTPUT	48	SEG10	ANODE10 DRIVER OUTPUT
19	SEG35	ANODE35 DRIVER OUTPUT	49	SEG36	ANODE36 DRIVER OUTPUT
20	SEG40	ANODE40 DRIVER OUTPUT	50	SEG37	ANODE37 DRIVER OUTPUT
21	SEG25	ANODE25 DRIVER OUTPUT	51	$\overline{\text{POR}}$	POWER-ON-RESET INPUT
22	GRID2	GRID2 DRIVER OUTPUT	52	VDD	LOGIC VOLTAGE
23	GND	POWER & SIGNAL REFERENCE	53	OSC1	RC OSCILLATION
24	SEG24	ANODE24 DRIVER OUTPUT	54	OSC0	RC OSCILLATION
25	GRID1	GRID1 DRIVER OUTPUT	55	GND	POWER & SIGNAL REFERENCE
26	SEG23	ANODE23 DRIVER OUTPUT	56	TEST1	TEST SIGNAL INPUT
27	SEG22	ANODE22 DRIVER OUTPUT	57	DATA IN	SERIAL DATA INPUT
28	SEG21	ANODE21 DRIVER OUTPUT	58	SCLK	SHIFT CLOCK INPUT
29	SEG20	ANODE20 DRIVER OUTPUT	59	$\overline{\text{CS}}$	CHIP SELECT INPUT
30	SEG19	ANODE19 DRIVER OUTPUT	60	TEST2	TEST SIGNAL INPUT

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	− 0.3~6.5	V
Display voltage	V_{DISP}	− 0.3~52	V
Input voltage	V_{IN}	− 0.3~V_{DD} + 0.3	V
Operating temperature range	T_{OP}	− 40~85	°C
Storage temperature range	Tstg	− 65~150	°C

• Operating Condition

Parameter	Symbol	Condition	MIN	TYPE	MAX	Unit
Power supply voltage	V_{DD}		4.5		5.5	V
Display voltage	V_{DISP}		V_{DD} + 2		50	V
High level input voltage	V_{IH}		3.6		VDD	V
Low level input voltage	V_{IL}		0		0.8	V
Clock Frequency	fc				500	KHz
OSC Frequency	fosc	75pf, 4.7KΩ	1	2	4	MHz

• DC Characteristics

Ta = −40~+85°C, V_{DD} = 5V ± 10% unless otherwise noted.
All voltages are referenced to GND.

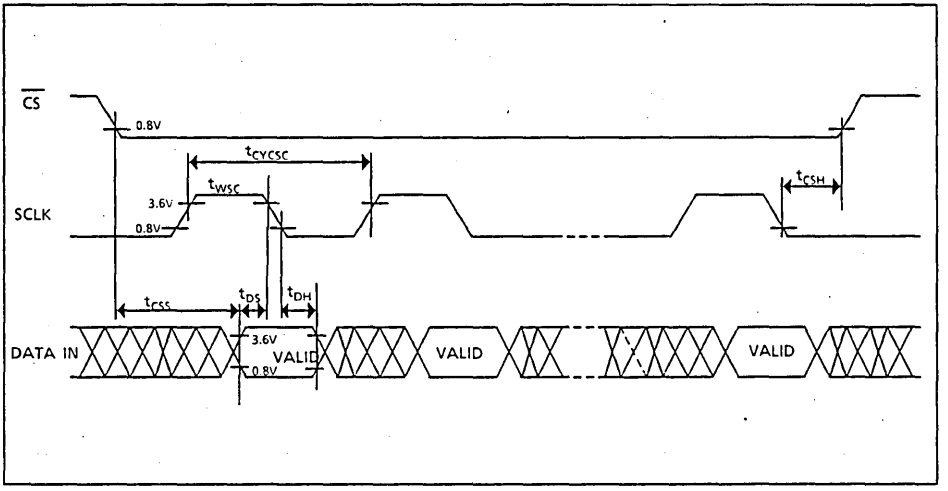
Parameter	Symbol	Condition	MIN	MAX	Unit
High level input voltage (All inputs except OSC0)	V_{IH1}		3.6	—	V
High level input voltage (OSC0)	V_{IH2}		4.2	—	V
Low level input voltage (All input except OSC0)	V_{IL1}		—	0.8	V
Low level input voltage (OSC0)	V_{IL2}		—	0.5	V
High level input current (SCLK, DATA IN, $\overline{CS}$, POR)	I_{IH1}	$V_{IH1} = V_{DD}$	−5	5	μA
High level input current (TEST1, TEST2)	I_{IH2}	$V_{IH2} = V_{DD}$	250	900	μA
High level input current (OSC0)	I_{IH3}	$V_{IH3} = V_{DD}$	−10	10	μA
Low level input current (SCLK, DATA IN, $\overline{CS}$, TEST1, TEST2)	I_{IL1}	V_{IL1} = OV	−5	5	μA
Low level input current ($\overline{POR}$)	I_{IL2}	V_{IL2} = OV	−27	−110	μA
Low level input current (OSC0)	I_{IL3}	V_{IL3} = OV	−10	10	μA
High level output voltage (SEG1-35)	V_{OH1}	I_{OH1} = −0.3mA	V_{DISP}-2.0	—	V
High level output voltage (SEG36-40)	V_{OH2}	I_{OH2} = −4.5mA	V_{DISP}-2.0	—	V
High level output voltage (GRID1, GRID8)	V_{OH3}	I_{OH3} = −31mA	V_{DISP}-2.7	—	V
High level output voltage (GRID2-7)	V_{OH4}	I_{OH4} = −16mA	V_{DISP}-2.7	—	V
Low level output voltage (SEG1-40, GRID1-8)	V_{OL1}	I_{OL1} = 10UA	—	1	V
Logic supply current	I_{DD}	fosc = 2.0MHz, No. load		15	mA
Display supply current	I_{DISP}	No load		10	mA

AC Characteristics

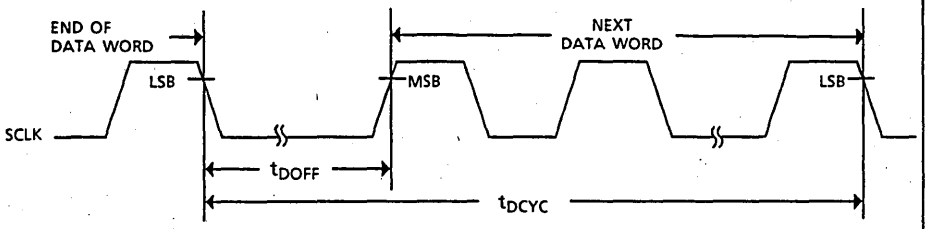
Ta = −40~+85°C, V_{DD} = 5V ± 10% unless otherwise noted.
All voltages are referenced to GND.

Parameter	Symbol	Condition	MIN	MAX	Unit
SCLK cycle time	t_{CYCSC}		—	2	µS
SCLK clock pulse width	t_{WSC}		1	—	µS
Data set-up time	t_{DS}		0.5	—	µS
Data hold time	t_{DH}		0.5	—	µS
$\overline{CS}$ set-up time	t_{CSS}		1	—	µS
$\overline{CS}$ hold time	t_{CSH}		1	—	µS
OSC frequency	f_{OSC}	R = 4.7KΩ, C = 75pf	1	4	MHz

Timing Chart



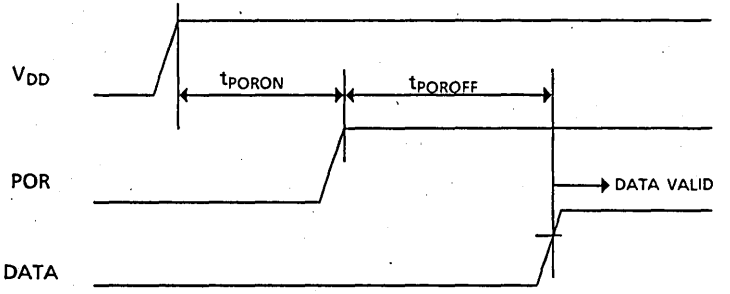
• Data Word LSB/MSB Timing



DATA INPUT OFF TIME t_{DOFF} 32 µSEC min.

DATA INPUT CYCLE t_{DCYC} 64µSEC min.

• Power-on-Reset Timing



OPTION 1
POR signal is generated by RC circuit.

POR ON TIME	t_{PORON}	External 1µF Cap.	250mSEC type
POR OFF TIME	t_{POROFF}		50µSEC min.

* Built-in 100KΩ pull-up resistor.

OPTION 2
POR signal is generated by peripheral circuit or host computer.

POR ON TIME	t_{PORON}	50µSEC min.
POR OFF TIME	t_{POROFF}	50µSEC min.

FUNCTIONAL DESCRIPTION

The data input of MSC7125-XX consists of 2 byte (16 bits) serial data but the 3 bits (bit 15, 14, 13) from MSB are taken as null data. This is because a number of data bis required for MSC7125-XX is 13 bits but 2 bytes construction is used for easy interface with CPU. When the 16-bit data input has been completed, MSC7125-XX generates the load signal automatically and begins execution.

The value of bit 12 of 16-bit serial data determines whether the input data is control data or display data.

• Control Data

When bit 12 is "1", input data is recognized as control data. A type of command and the associated data with the command are extracted from bit 11-0.

TABLE-1 Control data table

16-Bit Serial Input Words																Function
MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0	
X	X	X	1	0	0	X	X	X	X	X	X	X	2^2	2^1	2^0	LOAD BUFFER POINTER (Position of character to be changed)
X	X	X	1	0	1	X	X	X	X	X	X	X	2^2	2^1	2^0	LOAD DIGIT COUNTER (Number of characters to be displayed)
X	X	X	1	1	0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LOAD DUTY CYCLE (On/off and dimming control)
X	X	X	1	1	1	X	X	X	X	X	X	X	X	X	X	ENTER TEST MODE (Not a user function)

Note: X means this bit is "don't care" bit.

a) Load buffer pointer

This command is used to modify individual characters by setting buffer pointer to any digit position. (RAM write address is set)

A decimal equivalent value of bits 0-2 should be (the desired digit number-2).
(Example) In case of GRID 4, the setting value is 2 (010).

TABLE -2 Load buffer pointer codes

Buffer Pointer Value (lower 3 bits)	7	0	1	2	3	4	5	6
Character Controlled By	GRID 1	GRID 2	GRID 3	GRID 4	GRID 5	GRID 6	GRID 7	GRID 8

b) Load digit counter

This command sets the number of display digits.

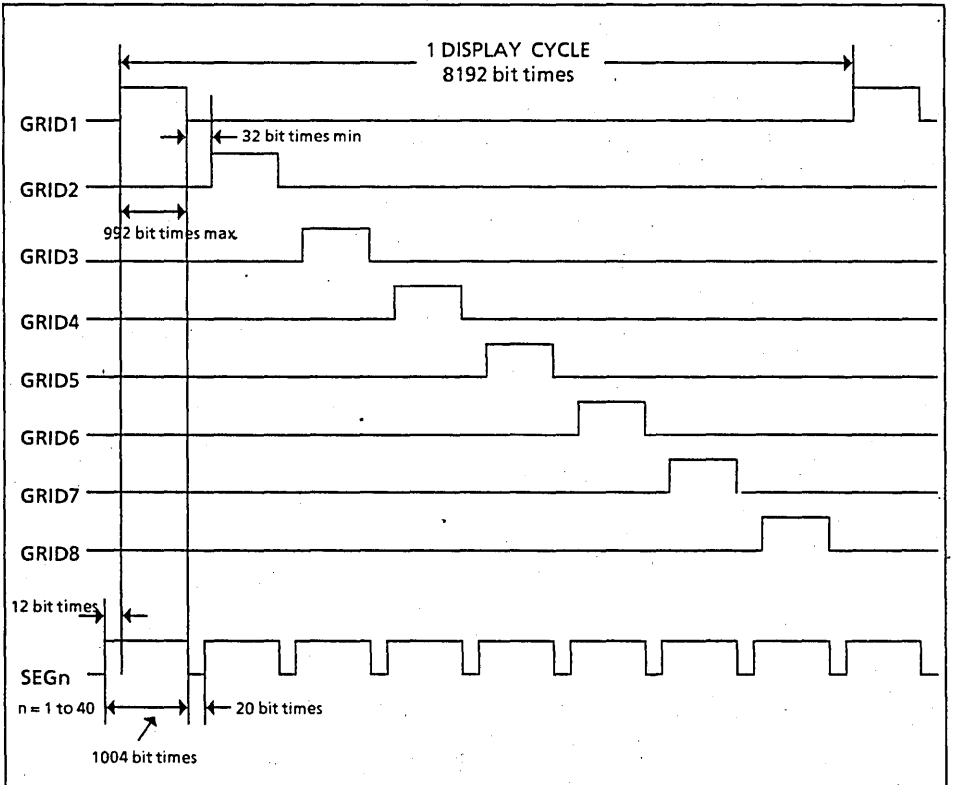
Set the desired digit number in bits 0-2.

TABLE-3 Digit counter control codes

Digit Counter Value (lower 3 bits)	0	1	2	3	4	5	6	7
Number of Digits	8	1	2	3	4	5	6	7

c) Load duty cycle

This command sets the duty cycle of driver output. With this command, 1024 step adjustments of brightness can be done. As shown in Fig.-1, the blank time between the GRIDS is 32 bit times, and between the segments, 20 bit times on the hardware, hence the setting range is 0 ~ 992.



NOTES:
1. TIMING SHOWN IS FOR 8 CHARACTERS WITH DUTY CYCLE OF 992
2. THE DUTY CYCLE CODE CAN MODIFY THE DIGIT ON-TIME FROM 0 TO 992 BIT TIMES.
3. 1 BIT TIME = Tosc (= 1/fosc) = 0.5μS typical

Fig-1 Display timing chart

d) Enter test mode

This mode is used for outgoing inspection and is not a user function.

o Display Data

Display data can be input by setting bit 12 = "0". 5 bits annunciator data are extracted from bits 11 - 7 and PLA address from bits 6 - 0.

Table 4 Display data

16-Bit Serial Input Words																Function
MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0	
X	X	X	0	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	LOAD DISPLAY DATA (Annunciator 5 bits and pla 7 bits)

PLA Code is User Programmable.
The relation between the dots of vacuum fluorescent display tube and Segment output of MSC 7125-XX is as shown in Fig-2.

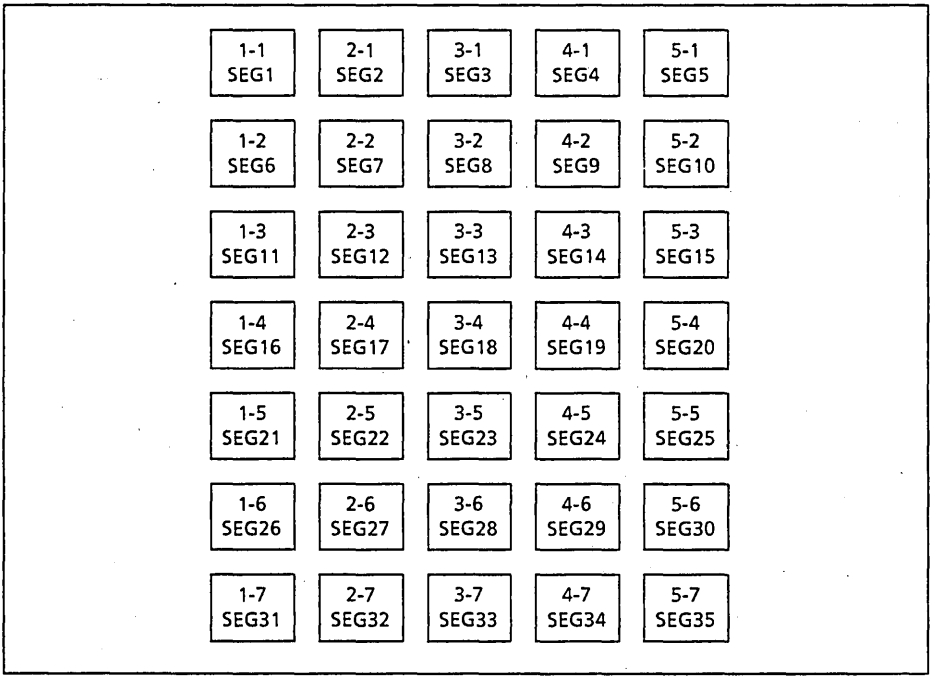


Fig-2 Dot-Segment output assignment

- **Power-On-Reset (POR)**

  The Power -On-Reset initializes the internal circuits when power is applied. The following condition is established after Power-On-Reset.

  a. The segment drivers are in the "L" state.

  b. The grid drivers are in the "L" state.

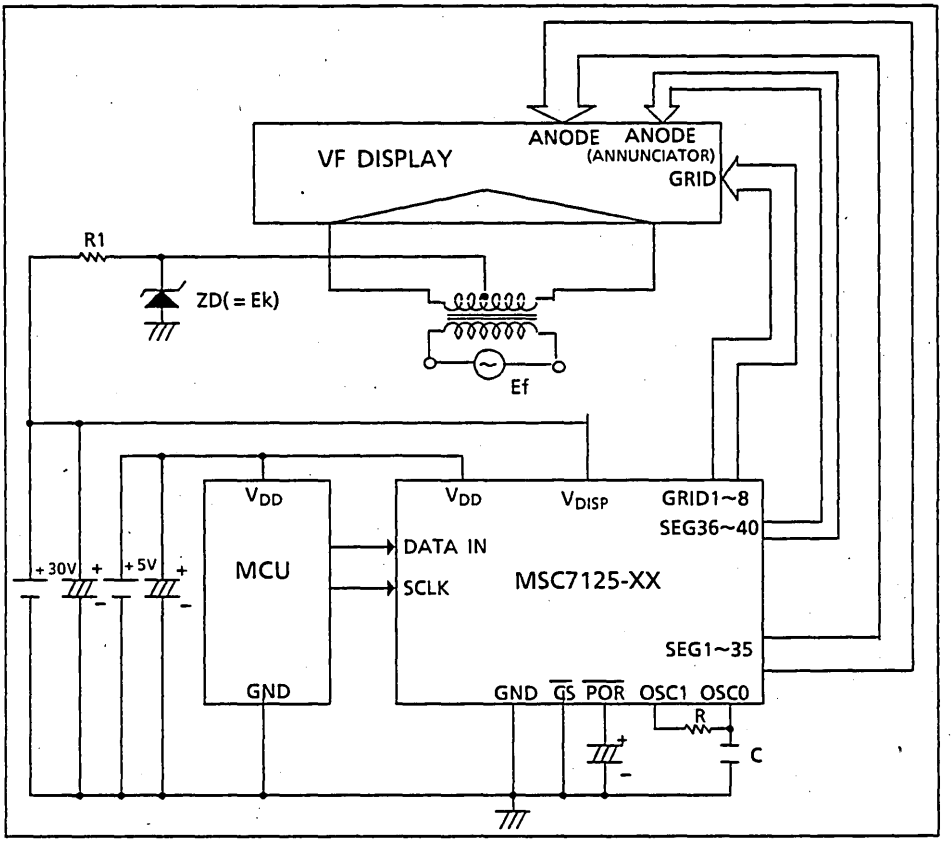
  c. The duty cycle is set to "0".

  d. The digit counter is set to "8".

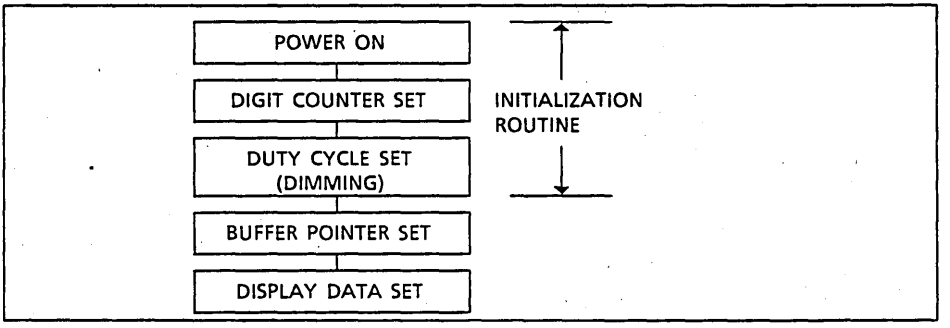
  e. The buffer pointer points to the character controlled by GRID1.

APPLICATION NOTE

a) Application circuit



b) Data set up flow



OKI semiconductor
MSC7128-XX
5 x 7 DOT MATRIX, 16-DIGIT

GENERAL DESCRIPTION

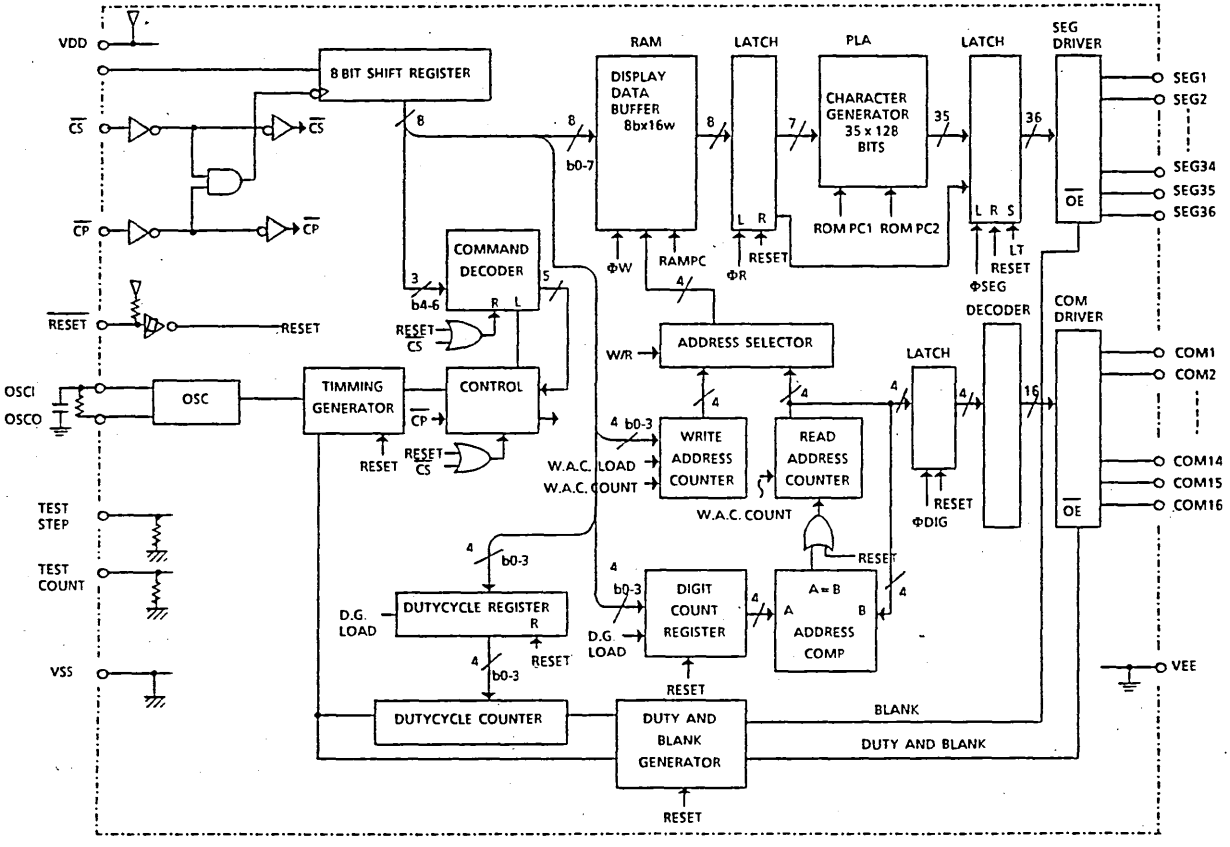
The MSC7128-XX is a general purpose display controllers for vacuum fluorescent display tube.

The MSC7128-XX drives displays with up to 35 anodes (dots) and up to 16 grids (characters) plus a cursor.
The controller accepts command and display data input words on a clocked serial input line.
Commands control the on/off duty cycle, starting character position, number of characters to display and display modes (PLA mode and Lamp Test mode). An internal PLA-type character generator provides character decoding and dot pattern generation for the full 128 characters.
No external drive circuit is required for displays that operate on 30mA of drive current up to 45 volts.
A 35x128-bit PLA (ROM) code is programmable.

FEATURES

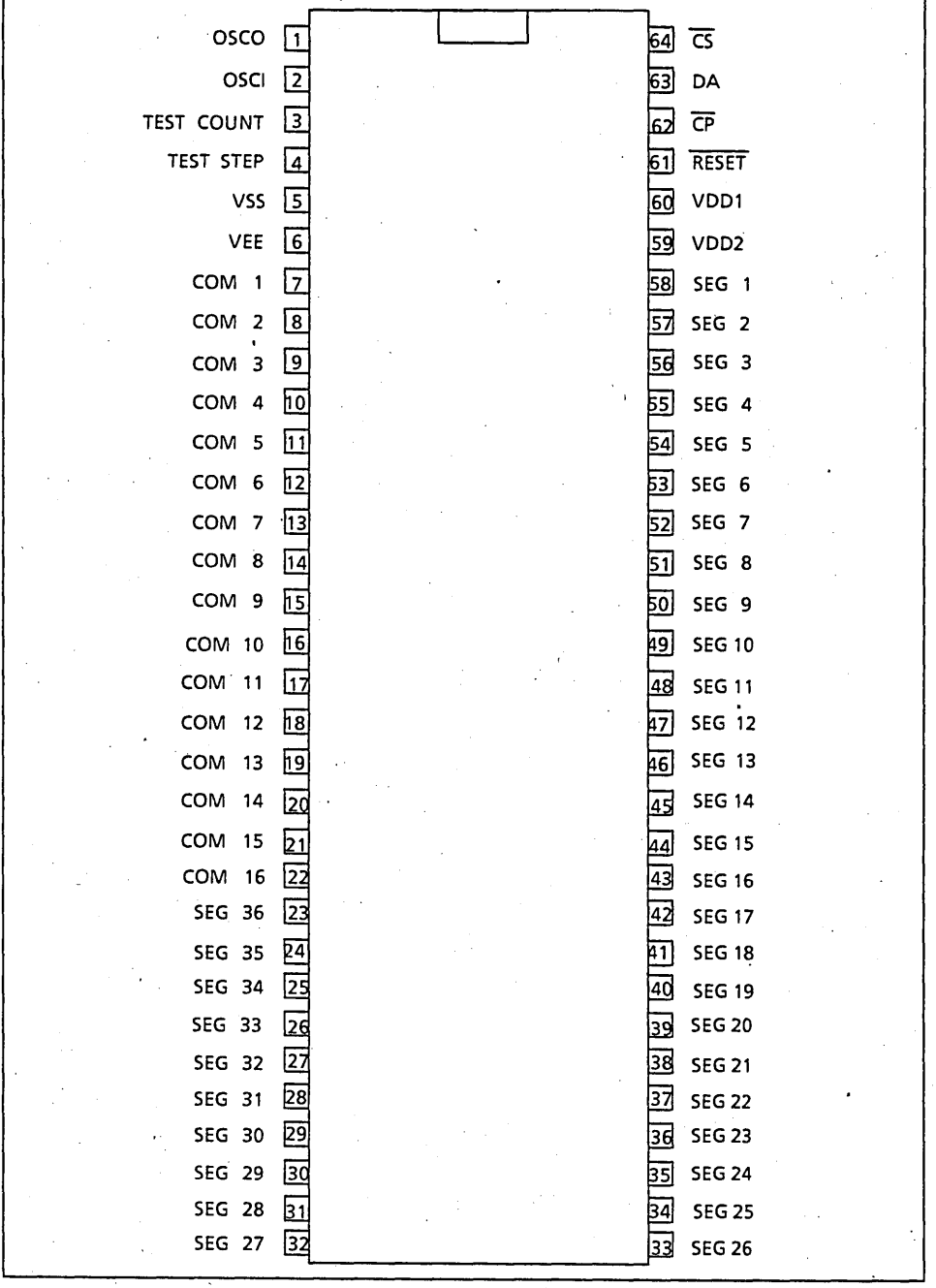
- Logic supply voltage (V_{DD}) : + 5V
- VF driver supply voltage (VEE) : - 55V
- Driver output current
  - VF grid driver (source) : - 30mA
  - VF anode driver (source) : - 2mA
  - VF cursor driver (source) : - 10mA
- Direct drive capability for vacuum fluorescent display
- Built-in oscillation circuit
- Built-in power-on-reset circuit with external C
- Serial host interface (data in, clock, chip select)
- Serial data input for 8-bit control and display data words
- Command functions
  - On/off duty cycle
  - Starting character position : 1 to 16
  - Number of characters : 1 to 16
  - Choice of 2-display modes : PLA mode, and Lamp Test mode
- Built-in 35x128-bit PLA-type character generator
  - Character font : 5x7
  - Number of characters : 128
  - Programmable PLA code
- 64 Pin shrink DIP package

BLOCK DIAGRAM



PIN CONFIGURATION

(Top View) 64 Lead Shrink Dual Inline Package



PIN DESCRIPTION

Pin Name	Pin No.	Input, Output	Connected to	Function
V_{DD1}	60		Power source	$V_{DD1} - V_{SS}$: Inner logic supply voltage $V_{DD2} - V_{EE}$: VF tube driving circuit supply voltage
V_{DD2}	59			
V_{SS}	5			
V_{EE}	6			
DA	63	Input	Microcomputer	Serial data input from LSB (positive logic)
$\overline{CP}$	63	Input	Microcomputer	Shift clock input. Data is shifted at the leading edge of the $\overline{CP}$.
$\overline{CS}$	64	Input	Microcomputer	Chip select input. When the pin is High, the serial data transfer is inhibited.
OSCI	2	Input		CR oscillation, external CR pin. fosc ≒ 250KHz at C = 100pF and R = 47K
OSCO	1	Output		
$\overline{RESET}$	61	Input		Reset input (pull-up resistor built in). When the pin is Low, the internal logic is reset, and the outputs of SBG1 to SBG36 and COM1 to COM16 are Low.
COM 1 ≀ COM16	7 ≀ 22	Output	VF tube grid electrode	VF tube grid electrode driving output. This pin can be connected directly to the VF tube. No pull-down resistor is required. I_{OH} >−30mA
SEG 1 ≀ SEG35	58 ≀ 24	Output	VF tube anode electrode	VF tube 5x7-dot anode electrode driving output. This pin can be connected directly to the VF tube. No pull-down resistor is required. I_{OH} >−2mA
SEG 36	23	Output	VF tube anode electrode	VF tube cursor anode electrode driving output. This pin can be connected directly to the VF tube. No pull-down resistor is required. I_{OH} >−10mA
TEST STEP	4	Input		Test mode setting input (normally open)
TEST COUNT	4	Input		Test clock input (normally open)

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage (1)	$V_{DD} - V_{SS}$		− 0.3~ + 6.5	V
Power supply voltage (2)	$V_{DD} - V_{EE}$		0~ + 65	V
Input voltage	$V_{IH} - V_{SS}$		− 0.3~V_{DD} + 0.3	V
Power dissipation	Pd	Ta≦25°C	~1.0	W
Storage temperature	Tstg		− 55~ + 150	°C
Output current	I_{O1}	COM1 ~ COM16	− 40mA	mA
	I_{O2}	SEG1 ~ SEG35	− 40mA	mA
	I_{O3}	SEG 36	− 40mA	mA

• Recommended Operating Condition

Parameter	Symbol	Condition	MIN	TYPE	MAX	Unit
Power supply voltage (1)	$V_{DD} - V_{SS}$		4.5		5.5	V
Power supply voltage (2)	$V_{DD} - V_{EE}$		10		60	V
High level input voltage	$V_{IH} - V_{SS}$		0.7V_{DD}			V
Low level input voltage	$V_{IL} - V_{SS}$				0.3V_{DD}	V
$\overline{CP}$ Frequency	fcp				500	KHz
OSC Frequency	fosc	100pF, 47KΩ	170	220	270	KHz
Operating temperature	Top		− 20		+ 75	°C

○ DC Characteristics

$V_{DD} - V_{SS} = 5V \pm 10\%$, $V_{DD} - V_{EE} = 60V$, Ta = − 20~ + 75°C

Parameter	Symbol	Condition	MIN	MAX	Unit
High level input voltage	V_{IH}		$0.7V_{DD}$		V
Low level input voltage	V_{IL}			$0.3V_{DD}$	V
High level input current	I_{IH1}	DA, $\overline{CP}$, $\overline{CS}$ $\overline{RESET}$, $\overline{POR}$ $V_{DD} = 5.5V$ $V_{IN} = 5V$	− 5	5	μA
	I_{IH2}	TEST STEP TEST COUNT $V_{DD} = 5.5V$ $V_{IN} = 5V$	0.25	1	mA
Low level input current	I_{IL1}	DA, $\overline{CP}$, $\overline{CS}$ $\overline{POR}$ TEST STEP TEST COUNT $V_{DD} = 5.5V$ $V_{IH} = 0.5V$	− 5	5	μA
	I_{IL2}	$\overline{RESET}$ $V_{DD} = 5.5V$ $V_{IH} = 0.5V$	− 25	− 100	μA
High level output voltage	V_{OH1}	OSC O $I_{OH} = -500\mu A$	$V_{DD} - 0.6$		V
	V_{OH2}	COM1~16 $I_{OH} = -30mA$	$V_{DD} - 4$		V
	V_{OH3}	SEG1~35 $I_{OH} = -2mA$	$V_{DD} - 3$		V
	V_{OH4}	SEG36 $I_{OH} = -10mA$	$V_{DD} - 4$		V
Low level output voltage	V_{OL1}	OSCO $I_{OL} = 500\mu A$		$V_{SS} + 0.6$	V
	V_{OL2}	COM1~16 $I_{OL} = 100\mu A$		$V_{EE} + 3$	V
	V_{OL3}	SEG1~35 $I_{OL} = 100\mu A$		$V_{EE} + 3$	V
	V_{OL4}	SEG36 $I_{OL} = 100\mu A$		$V_{EE} + 3$	V
Supply current	I_{SS1}	All SEGs on, 16-digit display, duty cycle 15/16, no load		15	mA
	I_{SS2}	All SEG s Low, all COMs High		1.5	mA
	I_{EE1}	All SEG s on, 16-digit display, duty cycle 15/16, no load		1.0	mA
	I_{EE2}	All SEGs Low, all COMs High		15	mA

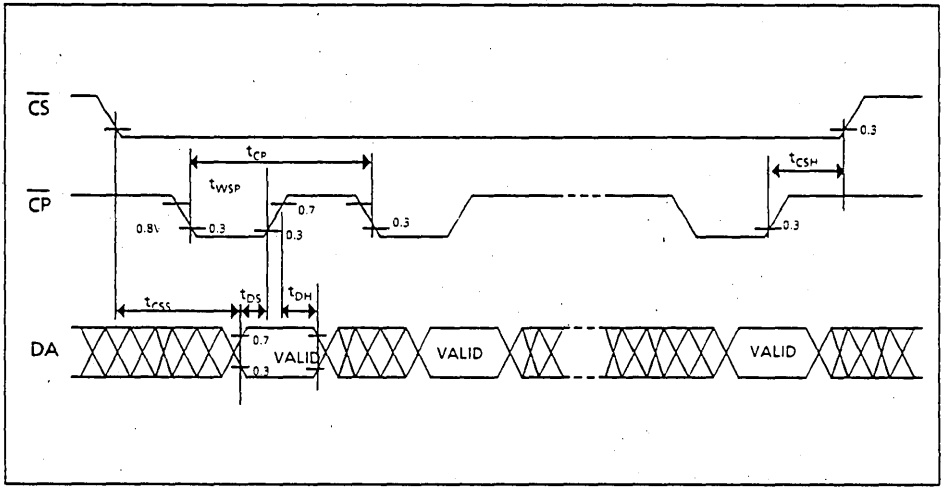
• AC Characteristics

$V_{DD} - V_{SS} = 5V \pm 10\%$, Ta = − 20~ + 75°C

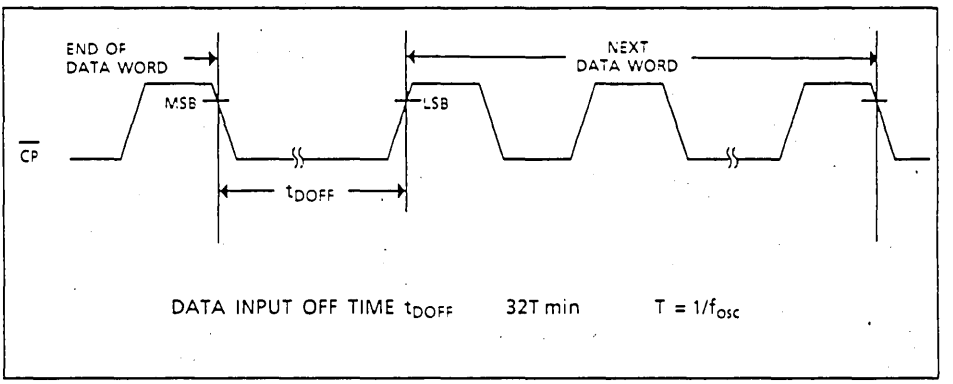
Parameter	Symbol	Condition	MIN	MAX	Unit
$\overline{CP}$ cycle time	t_{CP}		—	2	μS
$\overline{CP}$ pulse width	t_{WCP}		1	—	μS
Data set-up time	t_{DS}		0.5	—	μS
Data hold time	t_{DH}		0.5	—	μS
$\overline{CS}$ set-up time	t_{CSS}		1	—	μS
$\overline{CS}$ hold time	t_{CSH}		32T*	—	S
OSC frequency	f_{osc}	R = 47KΩ, C = 100pF	170	270	KHz

* $T = 1/f_{osc}$

• Data Timing Chart

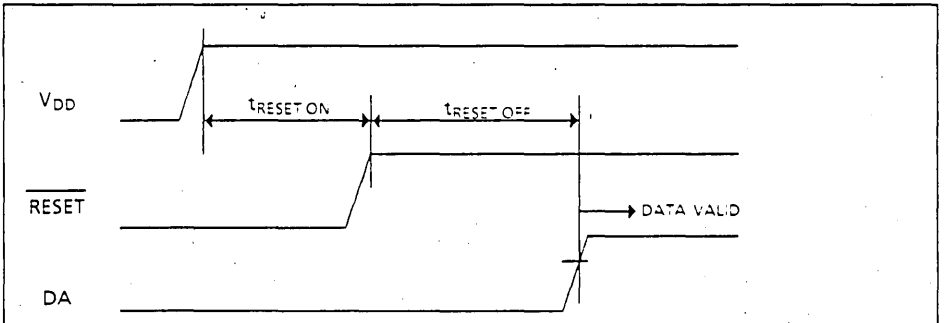


- **Data Word LSB/MSB Timing**



DATA INPUT OFF TIME t_{DOFF} 32T min T = $1/f_{osc}$

- **Reset Timing**



OPTION 1

A capacitor is connected between the $\overline{RESET}$ pin and V_{SS}.

RESET ON TIME	$t_{RESET\,ON}$	250mSEC type
RESET OFF TIME	$t_{RESETOFF}$	50μSEC min.

External capacitor: 1F

- Built-in 100KΩ pull-up resistor.

OPTION 2

A $\overline{RESET}$ signal is externally input.

RESET ON TIME	$t_{RESET\,ON}$	50μSEC min.
RESET OFF TIME	$t_{RESET\,OFF}$	50μSEC min.

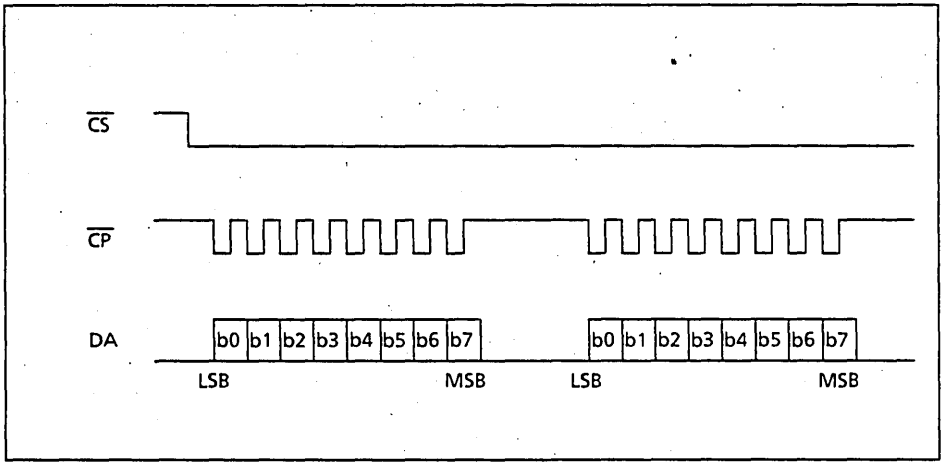
FUNCTIONAL DESCRIPTION

- **Data Transfer Method And Command Write Method**

A display control command or data is written by the 8-bit serial transfer method. The figure below shows the write timing chart. When the $\overline{CS}$ pin is Low, data can be transferred. Data 8 bits in length is input to the DA pin sequentially starting with the LSB. (LSB first)

Data is shifted at the rising edge of a shift clock pulse which is input to the $\overline{CP}$ pin as shown in the figure below. When data 8 bits in length is entered, an inner LOAD signal is automatically generated, and data is written into the registers and RAM. Accordingly, there is no need to input an external LOAD signal.

If the $\overline{CS}$ pin is changed from Low to High, the serial transfer is inhibited, and data, which is entered after the $\overline{CS}$ pin is changed from High to Low, is recognized in units of 8 bits.



○ Command Type

No.	Command	First byte								Second byte							
		b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	Address Set	1	0	0	0	X	X	X	X	X	X	X	X	X_3	X_2	X_1	X_0
1	Character Code Set	1	0	0	1	X	X	X	X	CU	CH_6	CH_5	CH_4	CH_3	CH_2	CH_1	CH_0
2	Display Duty Set	1	0	1	0	X	X	X	X	X	X	X	X	DC_3	DC_2	DC_1	DC_0
3	Number of Display Digits Set	1	0	1	1	X	X	X	X	X	X	X	X	DG_3	DG_2	DG_1	DG_0
4	Lamp Test	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	LT

*1 When character codes are to be continuously transferred, addresses are automatically incremented (internally). Accordingly, neither the Address Set command nor the first byte of the Character Code Set command are required to set the second and following character codes.

*2 X : Don't care

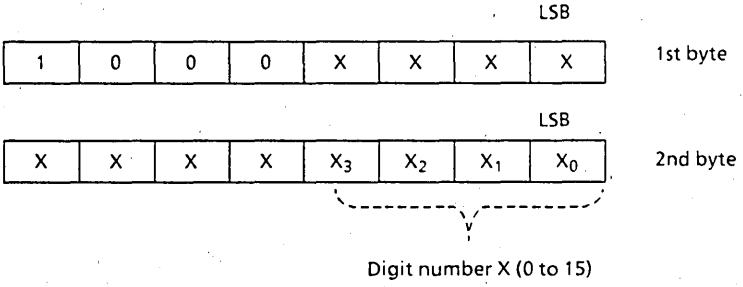
- **Address Set Command**

When the code of a display character is to be set, this command is used to specify the display location (digit number) of the character.

The relation between the digit number X and common outputs COM1 to COM16 is as follows:

X	COM input
0	COM1
1	COM2
⋮	⋮
15	COM16

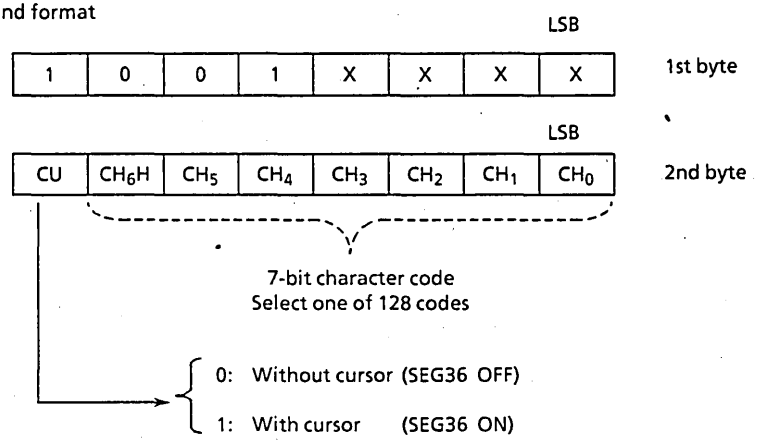
Command format



• Character Code Set Command

This command is used to specify the character to be displayed in the digit place specified by the Address Set command. Bits 0 to 6 of the second byte are used to specify the character code, and bit 7 is used to specify "Yes" or "No" of cursor display.

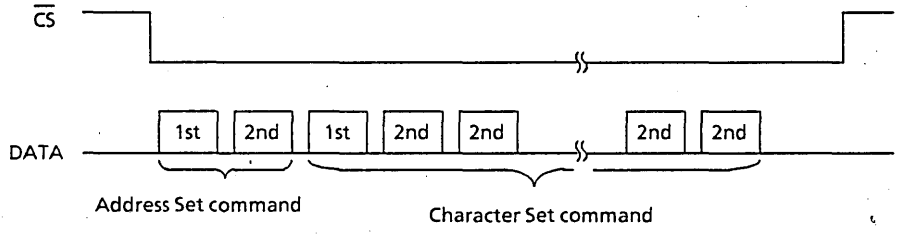
Command format



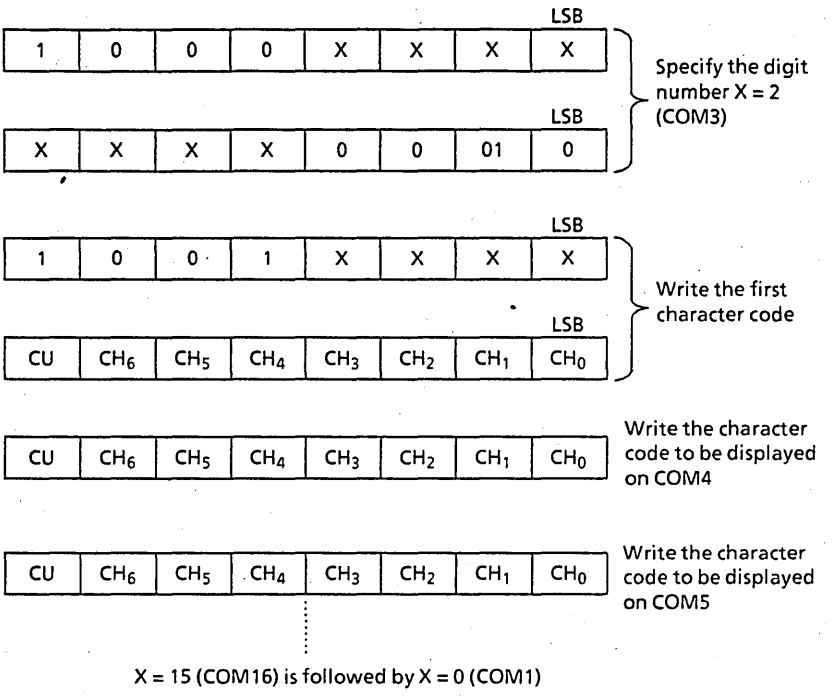
An automatic address increment function is built in. to write multidigit display character codes, just issue the Address Set command. To transfer the second and following digit display character codes, the first byte (operation code) of the Character Code command is not required. Just input the second byte.

When this command is executed, 8-bit data after the second byte, which is provided before the $\overline{CS}$ pin is turned High, is all treated as display character data.

Transfer examples of the Address Set command and the Character Set command



Example 1: The display for COM3 and the following is changed.

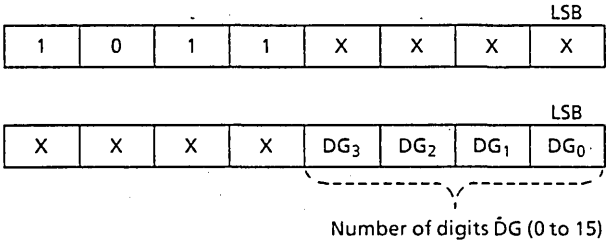


X = 15 (COM16) is followed by X = 0 (COM1)

o Number of Display Digits Set command

This command is used to set the digit count register and the number of display digits. The number of digits to be set ranges from 1 to 16.

Command format



The relation between the value for DG to be set and COM under display control is as follows:

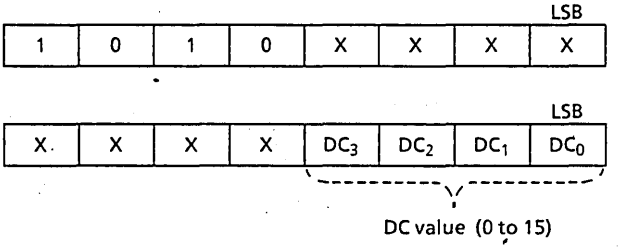
DG	COM displayed	DG	COM displayed
0	$COM_1 \sim COM_{16}$	8	$COM_1 \sim COM_8$
1	COM_1	9	$COM_1 \sim COM_9$
2	$COM_1 \sim COM_2$	10	$COM_1 \sim COM_{10}$
3	$COM_1 \sim COM_3$	11	$COM_1 \sim COM_{11}$
4	$COM_1 \sim COM_4$	12	$COM_1 \sim COM_{12}$
5	$COM_1 \sim COM_5$	13	$COM_1 \sim COM_{13}$
6	$COM_1 \sim COM_6$	14	$COM_1 \sim COM_{14}$
7	$COM_1 \sim COM_7$	15	$COM_1 \sim COM_{15}$

• Display Duty Set command

Assuming the original oscillation cycle as T, the time allocated to 1-digit display is 64 T. The actual display time may be specified as 0 to 60 T in increments of 4T. Assuming the number of display digits as n and the parameter provided by the Display Duty Set command as DC, the resultant display duty cycle ratio is as follows:

$$\frac{4\,(DC)}{64n} = \frac{(DC)}{16n}$$

Command format

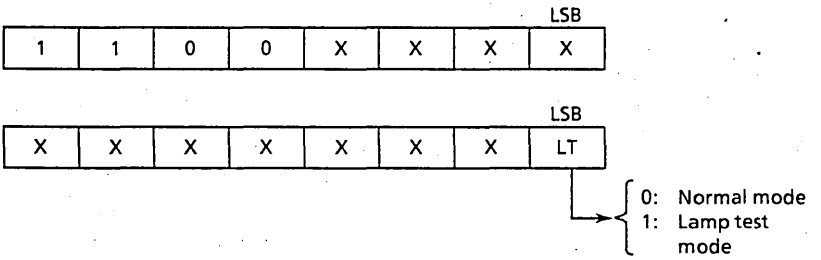


• Lamp Test command

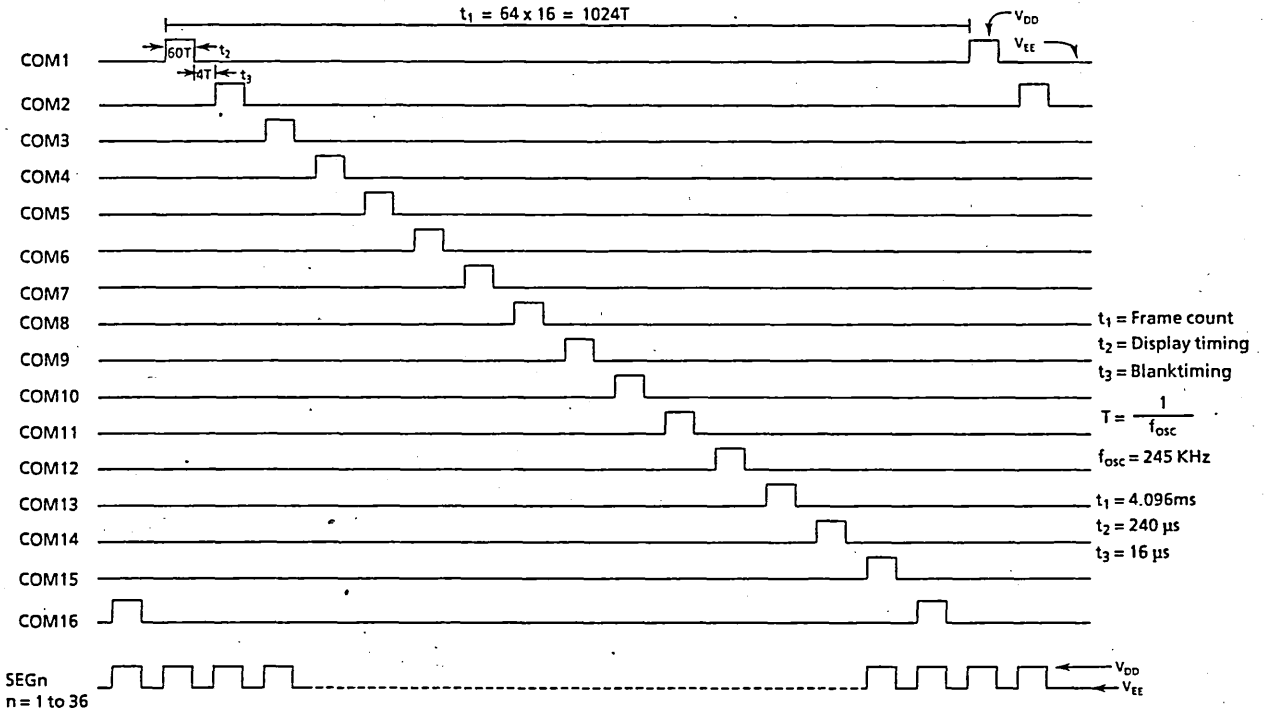
This command is used to set the All-Segment Display mode. If this occurs, the 36 segments for each digit to be displayed are put into the ON state. The number of display digits and the display duty cycle depend on the contents of the digit count register and of the duty register.

The contents of the internal RAM are not affected by this command. When the command is released, the original display appears once again.

Command format



DIGIT TIMING CHART (16-digit display)



POWER ON RESET OPERATION

Operations when the $\overline{\text{RESET}}$ pin is Low are as follows:

a. All segment driver outputs are Low.

b. All grid driver outputs are Low.

c. The number of display digits is set to 16.

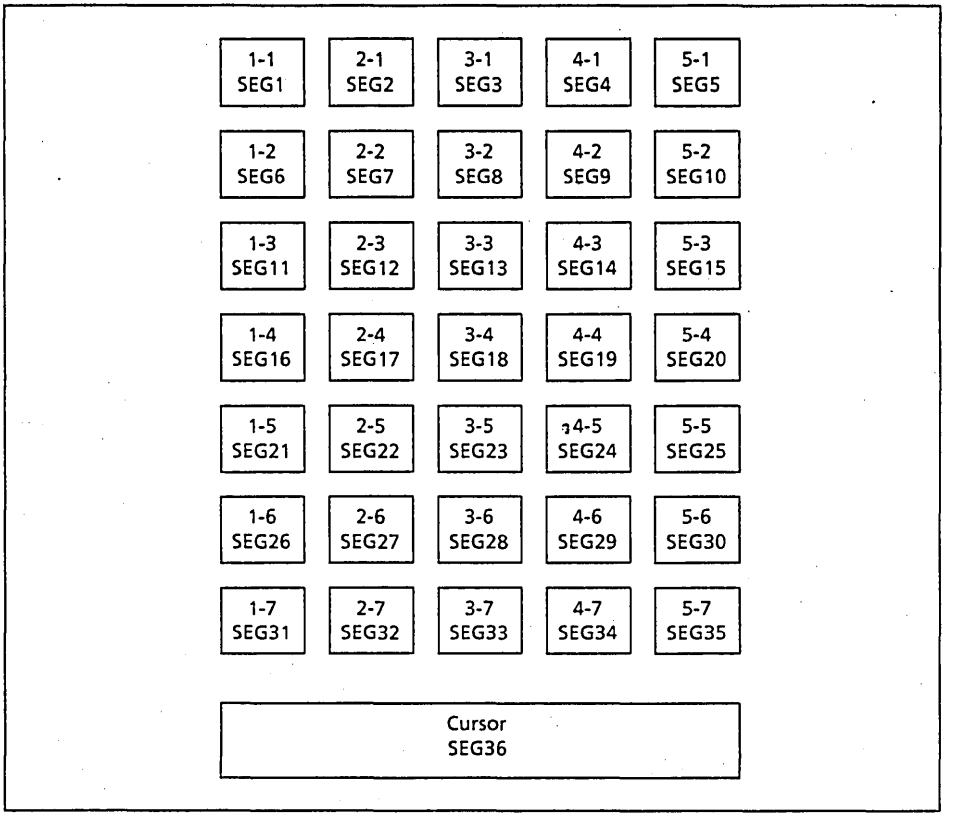
d. The display duty cycle is set to 0.

TEST STEP AND TEST COUNT

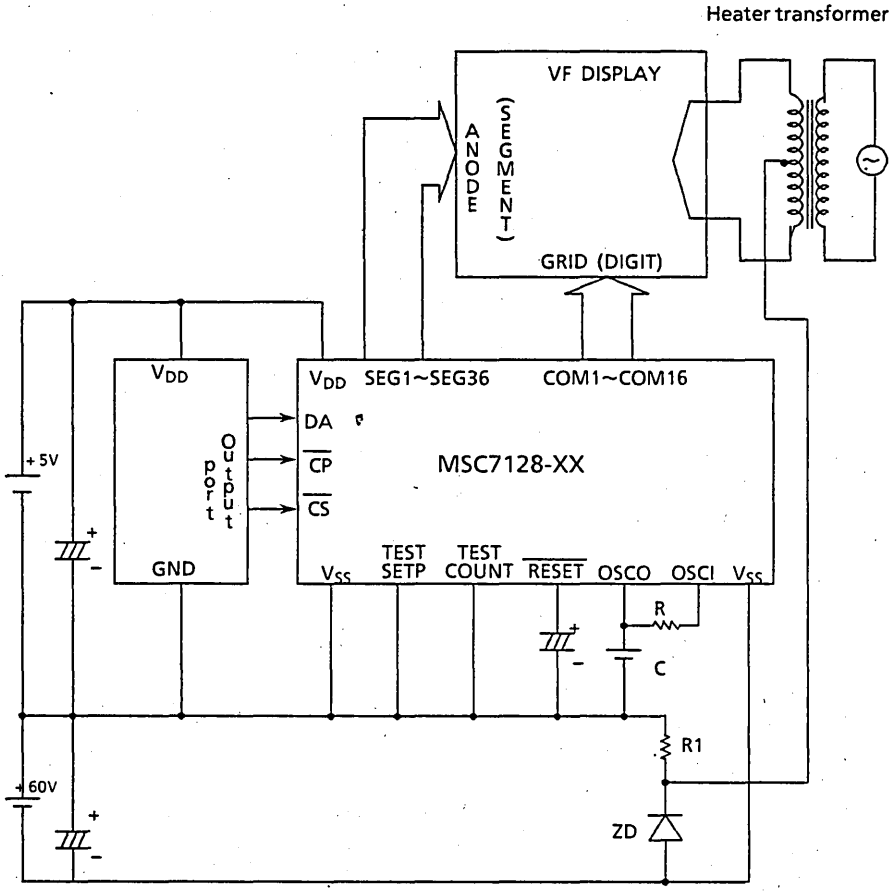
These pins are used for inspection before shipment, and should not be used by the user.

When an IC is mounted, leave them open or connect to V_{SS}. If they are connected to other pins, a malfunction may be caused.

RELATION BETWEEN SEGMENT OUTPUT AND VF TUBE DOTS



APPLICATION NOTE



Level Meter

OKI semiconductor
MSC1124

2-CHANNEL 12-DOT LEVEL METER IC (STATIC)

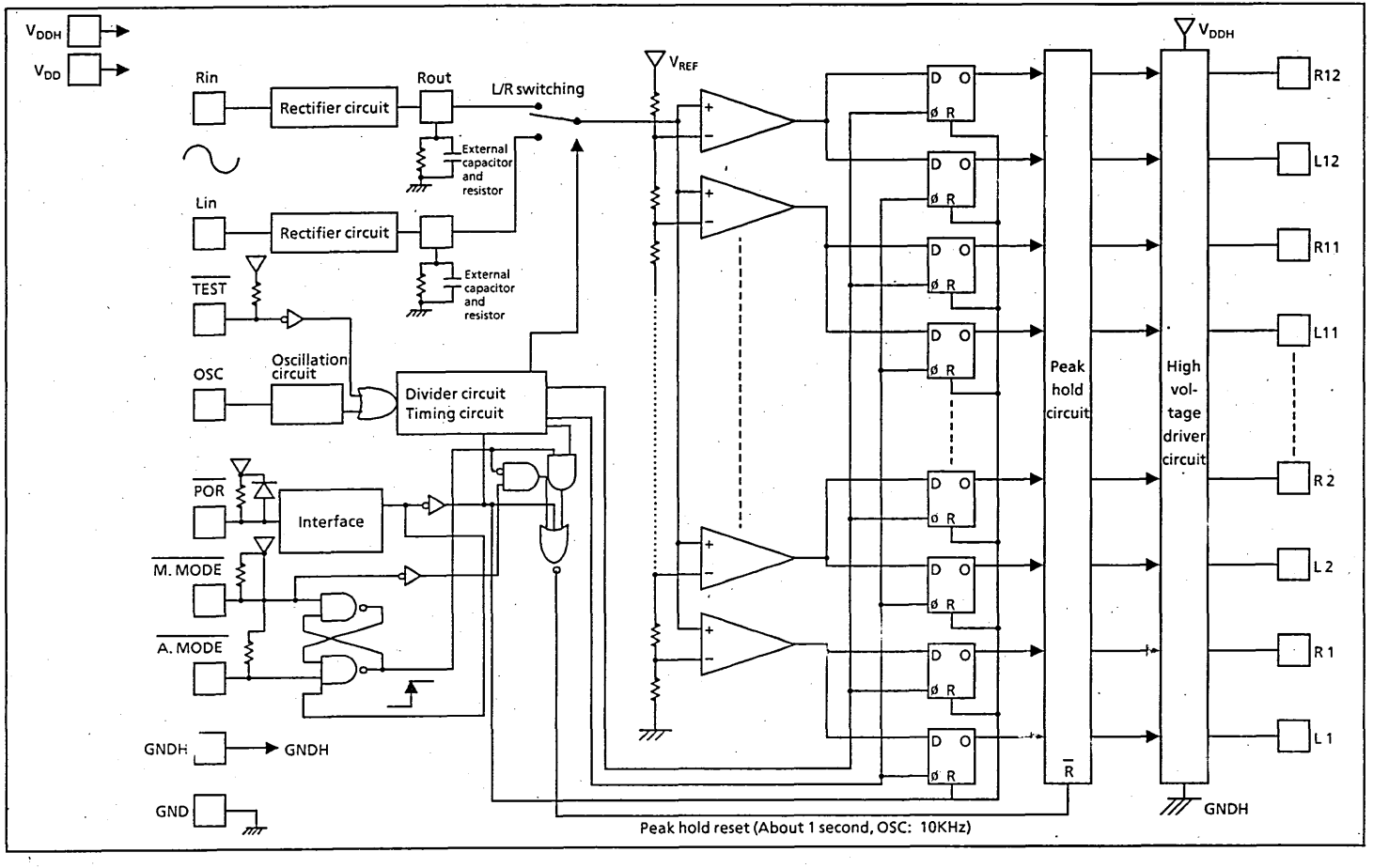
GENERAL DESCRIPTION

The MSC1124 is a static FLT driving audio 2-channel level meter, which can be used for high fidelity VTRs and audio equipment.

FEATURES

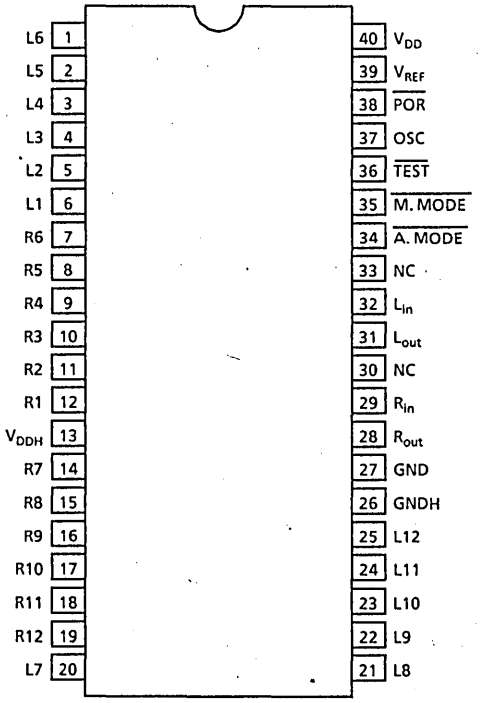
- Direct in put of audio (analogue) signals
- Log compression circuit built in (-20 dB to 8 dB, 12 dots)
- High withstand voltage output, output voltage 35 V, supply voltage 36.5 V
- Peak hold function built in, automatic and manual reset
- Power ON reset circuit built in
- 2-power-source (GND shared) system
- 40-pin plastic DIP, 44-pin V plastic QFP

BLOCK DIAGRAM



PIN CONFIGURATION

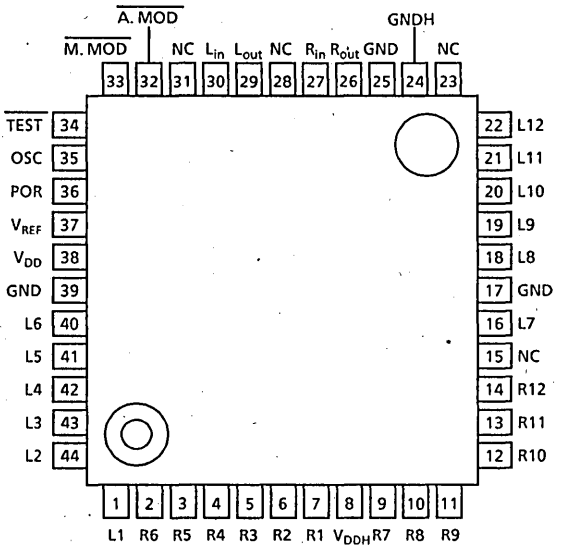
MSC1124
(Top View) 40 Lead Plastic DIP



(This specification may be changed without notice.)

PIN CONFIGURATION

MSC1124
(Top View) 44 Lead Plastic Flat Package



NOTE:

(This specification may be changed without notice.)

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rated value	Unit	Terminal
Supply voltage 1	V_{DD}	Ta = 25°C	− 0.2~7.0	V	V_{DD}, V_{REF}
Supply voltage 2 (Between VCC and VEE)	V_{DDH}	Ta = 25°C	− 0.2~40	V	V_{DDH}
Input voltage	V_{I1}	Ta = 25°C	− 0.2~VDD + 0.2	V	Except Rin and Lin
Input reverse current	I_I	Ta = 25°C VI = − 1.0V	10max	mA	All input pins
Output current	I_{01}	Ta = 25°C, source current	− 10max	mA	R1~R12 L1~L12
Output current	I_{02}	Ta = 25°C, sink current	3max	mA	
Input voltage	V_{I2}	Ta = 25°C	− 0.7~VDD + 0.2	V	Rin, Lin
Allowable loss	P_D	Ta = 25°C	650	mW	
Storage temperature	Ts tg	—	− 50~125	°C	

• Operating Condition

Parameter	Symbol	Conditions	Rated value	Unit	Terminal
Supply voltage 1	V_{DD}	—	4.5~5.5	V	V_{DD}
Supply voltage 2	V_{DDH}	—	8~37	V	V_{DDH}
Operating temperature	Top	—	− 10~70	°C	

• DC Characteristics

(V_{DD} = 5.0V ± 0.5V, Ta = − 10~70°C)

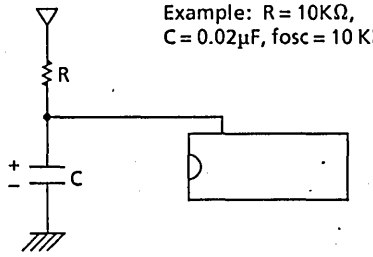
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Terminal
Input bias current	I_{IL1}	V_{IN} = 0V	—	—	± 1	μA	Rin, Lin
Input voltage	V_I	—	—	—	350	mVrms	
High level input voltage	V_{IH1}	—	V_{DD} × 80%	—	—	V	
Low level input voltage	V_{IL}	—	—	—	V_{DD} × 20%	V	$\overline{\text{A. MODE}}$ $\overline{\text{M.MODE}}$ $\overline{\text{P. O. R}}$ $\overline{\text{TEST}}$
High level input current	I_{IH}	$V_I = V_{DD}$	—	—	± 1	μA	
Low level input current	I_{IL2}	V_I = 0V	− 25	− 50	− 100	μA	
High level output voltage	V_{OH}	I_0 = − 0.2mA V_{DDH} = 36.5V	35	—	—	V	R1~R12 L1~L12
Low level output voltage	V_{OL1}	I_0 = 0.1mA V_{DDH} = 36.5V	—	—	2	V	
Low level output voltage	V_{OL2}	I_0 = 0mA V_{DDH} = 40V	—	—	100	mV	R1~R12 L1~L12
Oscillation frequency	f(osc)	R = 10KΩ C = 0.02μF	6	10	14	KHz	OSC
L/R sampling frequency	FLR	—	f(osc) × 1/32				
Peak hold reset timing	p.f	—	f(osc) × 1/8192				
POR release voltage	V_{IH2}	—	4.0	—	—	V	POR, V_{DD}
Supply current 1	I_{DDH}	V_{DDH} = 36.5V No load, all DOTs ON	—	—	15	mA	V_{DDH}
Supply current 2	I_{DD}	V_{DDH} = 36.5V No load, all DOTs OFF	—	—	15	mA	V_{DD}
Supply current 3	I_{DDH} OFF	V_{DDH} = 36.5V No load, all DOTs OFF	—	—	2.2	mA	V_{DDH}

FUNCTIONAL DESCRIPTION

- OSC

This is a C (capacitor) and R (resistor) oscillation connection terminal to specify the R/L sampling switching frequency and the peak hold reset timing.

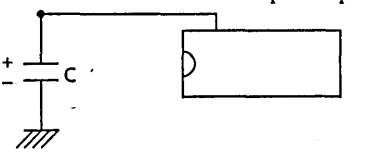
Example: R = 10KΩ,
C = 0.02μF, fosc = 10 KHz



- $\overline{\text{POR}}$

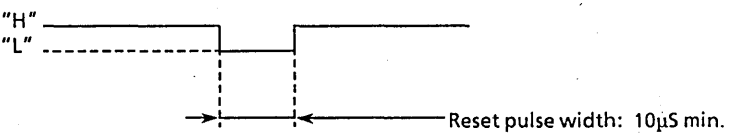
The POR terminal with a capacitor connected is used for power on reset. The reset release threshold voltage is 4.0V max. The built-in pull-up resistor is about 100 KΩ. Select the capacitor value according to the supply voltage at its leading edge.

C = 2.2μF~4.7μF



- $\overline{\text{M, MODE}}$

When this terminal is made Low, the manual peak hold reset mode is set, and the peak hold state is reset. For that purpose, the $\overline{\text{A. MODE}}$ terminal should be kept open.
When only the AUTO mode is to be used, connect the terminal to the V_{DD} terminal.



- $\overline{\text{A. MODE}}$

If this terminal is made Low when M.MODE is selected, the system enters the AUTO mode reset state. The AUTO mode reset timing is fosc x 1/8192.
When only the AUTO mode is to be used, keep the terminal Low. When power is turned on, the AUTO mode is automatically set.

- Rin, Lin

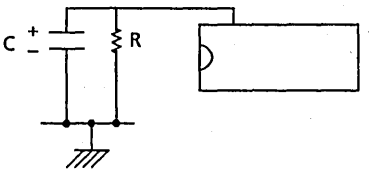
These are an analogue input terminal to input an audio level signal.

Max. 350mVrms

- Rout, Lout

  These are a capacitor (C) and resistor (R) connection terminal to hold the analogue input peak.

  Example: R = 10KΩ, C = 10μF



- R1 to R12, L1 to L12

  These are a FLT dot output terminal

- V_{DDH}

  This is a power terminal for R1 to R12 and L1 to L12.

- GNDH

  This is a GND terminal for R1 to R12 and L1 to L12.

- V_{DD}

  This is an analogue or logic system supply voltage terminal.

- GND

  This is an analogue or logic system grounding terminal.

- $\overline{TEST}$

  This is a measurement input terminal, which is generally to be connected to the VDD terminal.

- V_{REF}

  This is a comparator reference power terminal, which is generally to be connected to the VDD terminal

R/L THRESHOLD VOLTAGE TABLE

(Vref = 5V ± 1%, Ta = 25°C, f = 1 KHz)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Terminal
Threshold voltage 1	C1	The output should be offset. AJD	—	– 20	—	dB	
Threshold voltage 2	C2		– 17	– 15	– 13	dB	
Threshold voltage 3	C3		– 11.5	– 10	– 8.5	dB	
Threshold voltage 4	C4		– 8.0	– 7	– 6.0	dB	
Threshold voltage 5	C5		– 6.0	– 5	– 4.0	dB	
Threshold voltage 6	C6		– 4.0	– 3	– 2.0	dB	
Threshold voltage 7	C7		– 1.5	– 1	– 0.5	dB	
Threshold voltage 8	C8	The output C8 level should be 0 dB.	—	0	—	dB	
Threshold voltage 9	C9		+ 0.5	+ 1	+ 1.5	dB	
Threshold voltage 10	C10		+ 2.0	+ 3	+ 4.0	dB	
Threshold voltage 11	C11		+ 4.0	+ 5	+ 6.0	dB	
Threshold voltage 12	C12		+ 6.5	+ 8	+ 9.5	dB	

When the input is set to – 30 dB, all DOTs are off.

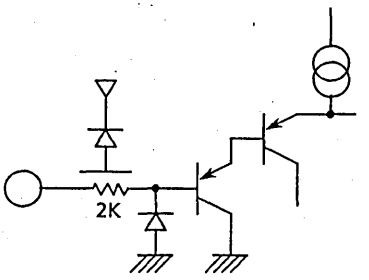
AC INPUT LEVEL VS DC INPUT LEVEL

Threshold voltage	1	2	3	4	5	6	7	8	9	10	11	12
Display [dB]	– 20	– 15	– 10	– 7	– 5	– 3	– 1	0	+ 1	+ 3	+ 5	+ 8
AC input level [mV rms]	11	20	36	51	64	81	102	114	128	161	203	286
DC input level [mV]*	14	26	47	67	84	106	133	149	167	211	265	374

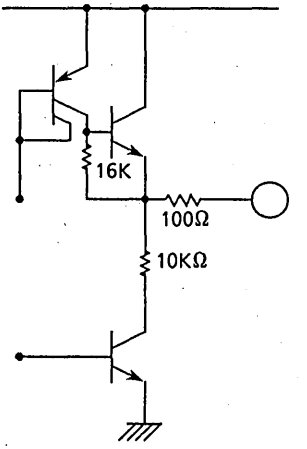
*The values in the table are TYP values.

INPUT/OUTPUT CIRCUIT

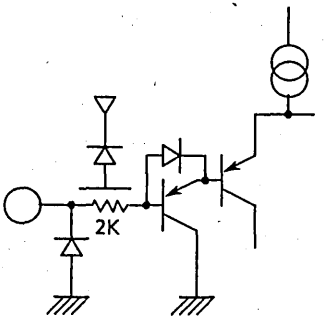
- Rin, Lin



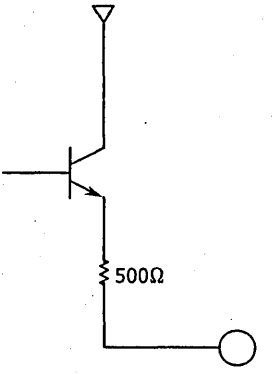
- R1~R12, L1~L12



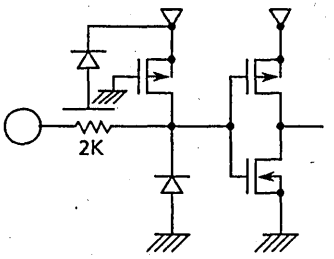
- OSC



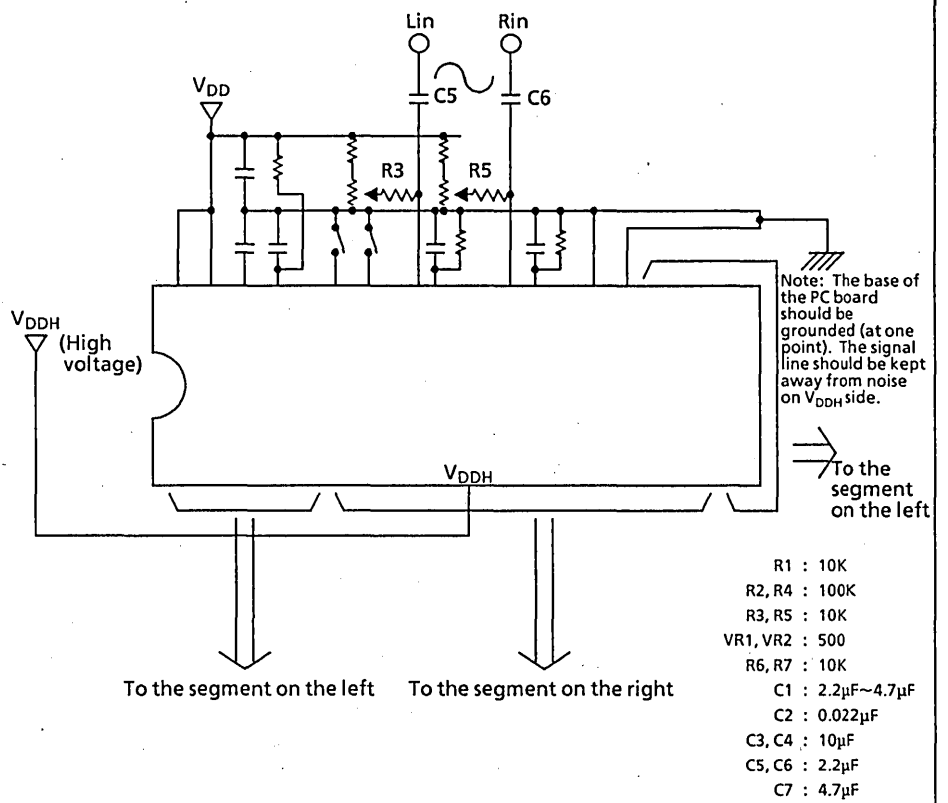
- Lout, Rout



- $\overline{\text{M.MODE}}$ $\overline{\text{A.MODE}}$, $\overline{\text{POR}}$, $\overline{\text{TEST}}$



APPLICATION NOTE



R1 : 10K
R2, R4 : 100K
R3, R5 : 10K
VR1, VR2 : 500
R6, R7 : 10K
C1 : 2.2µF~4.7µF
C2 : 0.022µF
C3, C4 : 10µF
C5, C6 : 2.2µF
C7 : 4.7µF

OKI semiconductor
MSC1146B

2-CHANNEL 15-DOT LEVEL METER IC (DYNAMIC)

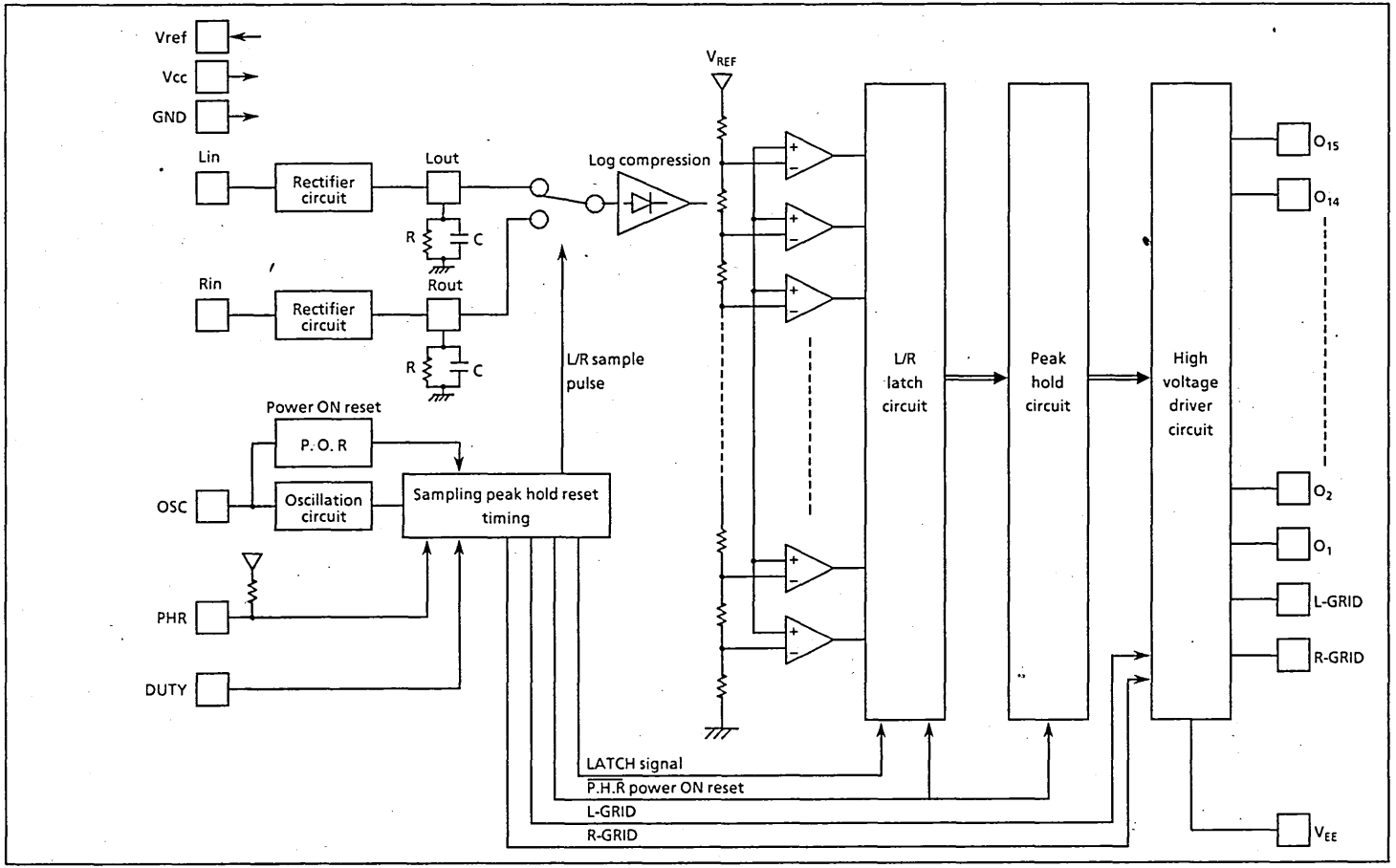
GENERAL DESCRIPTION

The OKI MSC 1146B Bar graph Display Level Meter is a Bi-CMOS LSI general purpose display Level Meter designed to interface with vacuum fluorescent type display.

FEATURES

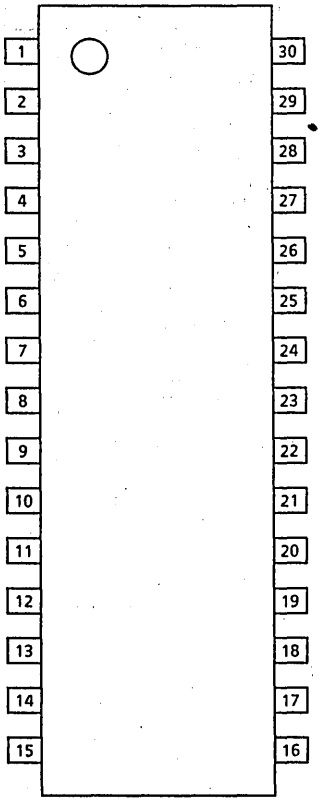
- Direct input of audio signals (AC signals)
- DC input
- Peak hold function provided
- Decibel display by anti-log compression (+ 10 B to – 40dB)
- Power ON reset circuit built in
- FLT direct driving by high withstand voltage process (Pull-down resistor built in)
- Grid driver output duty simply changed by C and R
- 28-pin lead plastic DIP, 30-pin shrink plastic DIP

BLOCK DIAGRAM



PIN CONFIGURATION

30PIN Shrink DIP



1	VCC	11	NC	21	O_6
2	Rin	12	VEE	22	O_7
3	Rout	13	L-Grid	23	O_8
4	GND	14	R-Grid	24	O_9
5	Lin	15	O_1	25	O_{10}
6	Lout	16	O_2	26	O_{11}
7	Vref	17	O_3	27	O_{12}
8	$\overline{PHR}$	18	O_4	28	O_{13}
9	OSC	19	O_5	29	O_{14}
10	DUTY	20	NC	30	O_{15}

(This specification may be changed without notice.)

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rated value	Unit	Terminal
Supply voltage 1	V_{CC}	Ta = 25°C	– 0.2~7.0	V	VCC
Supply voltage 2 (Between VCC and VEE)	V_{EE}	Ta = 25°C	VCC + 0.2~ – 38	V	VEE
Input voltage	V_{I1}	Ta = 25°C	– 0.2~VDD + 0.2	V	Except Rin and Lin
Input reverse current	I_I	Ta = 25°C, V_I = – 1.0V	10MAX	mA	
Output current	I_{01}	Ta = 25°C, source current	– 10MAX	mA	O_1~O_{15}
Output current	I_{02}	Ta = 25°C, source current	– 50	mA	L-Grid, R-Grid
Input voltage	V_{I2}	Ta = 25°C	– 3.0~VDD + 0.2	V	Rin, Lin
Allowable loss	P_{D2}	Ta = 70°C	480	mW	
Storage temperature	Ts tg		– 50~ + 125	°C	

• Operating Condition

Parameter	Symbol	Conditions	Rated value	Unit	Terminal
Supply voltage	V_{CC}		4.5~5.5	V	VCC
Supply voltage	V_{EE}	Between V_{CC} and V_E	– 8~ – 37	V	VEE
Operating temperature	T_{OP}		– 10~ + 70	°C	

• DC Characteristics

Ta = −10~70°C, VCC = 5.0 ± 0.5V

Parameter	Symbol	Conditions	Specifications			Unit	Terminal
			MIN	TYP	MAX		
Input bias current	I_{IL}	Vin = 0V			± 1.0	μA	Rin, Lin
Input voltage	V_I				3.5	VP.P	
High level input voltage	V_{IH1}		VCC × 80%			V	$\overline{PHR}$
Low level input voltage	V_{IL1}				VCC × 20%	V	
High level input current	I_{IH1}				± 1	μA	
Low level input current	I_{IL1}		− 20	− 50	− 100	μA	
High level output voltage	V_{OH1}	I_O = -0.2mA V_{EE} = -36.0V, V_{CC} = 5V	3.5			V	O_1~O_{15}
Low level output voltage	V_{OL1}	I_O = 0mA, V_{EE} = -36.5V (Between VCC and VEE)			200	mV	O_1~O_{15} R-Grid L-Grid
Pull-down resistor	R_O	V_{CC} = 5V, V_{EE} = -36.5V	70	200	500	KΩ	
High level output voltage	V_{OH2}	I_O = -20mA, V_{EE} = -36.5V, V_{CC} = 5V (Between V_{CC} and V_{EE})	2.5			V	R-Grid L-Grid
Oscillation frequency	f_{osc}	R = 10KΩ, C = 0.022μF	6	10	14	KHz	OSC
L/R sampling frequency	f. L/R		fosc × 1/32				
Peak hold reset timing	P.f		fosc × 1/8192				
POR release voltage	V_{IH2}		4.0			V	VCC
Voltage V_{REF}	V_{REF}	V_{CC} = 5V, V_{EE} = -36.5V	− 8	− 5	− 2	V	V_{REF}
Supply current	I_{EE1}	V_{CC} = 5V, V_{EE} = -36.5V DUTY No load, all DOTs ON 1/12			5	mA	V_{EE}
Supply current	I_{EE2}	V_{CC} = 5V, V_{EE} = -36.5V DUTY No load, all DOTs OFF 1/12			5	mA	V_{EE}
Supply current	I_{CC}	V_{CC} = 5V, V_{EE} = -36.5V No load, all DOTs OFF			10	mA	V_{CC}

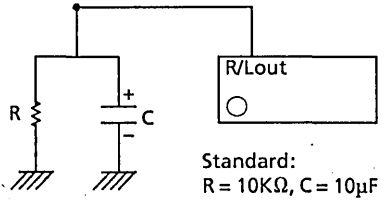
Note: Voltage V_{EE} is a voltage between the V_{CC} and V_{EE} terminals.

FUNCTIONAL DESCRIPTION

VCC: This is an analogue or logic system voltage input terminal.

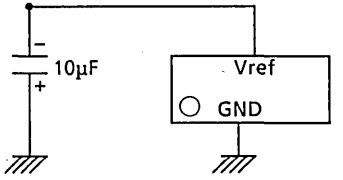
Rin, Lin: These are audio input terminals to directly input an alternating current via a capacitor coupling. Max. 3.5V P.P

Rout, Lout: These terminals rectify an audio alternating current with a capacitor and resistor connected.



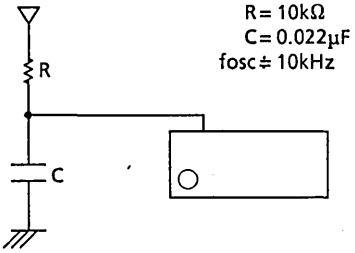
Standard:
R = 10KΩ, C = 10μF

Vref: This is an amplifier built-in voltage output terminal. Connect a capacitor of about 10μF between the GND and Vref terminals.



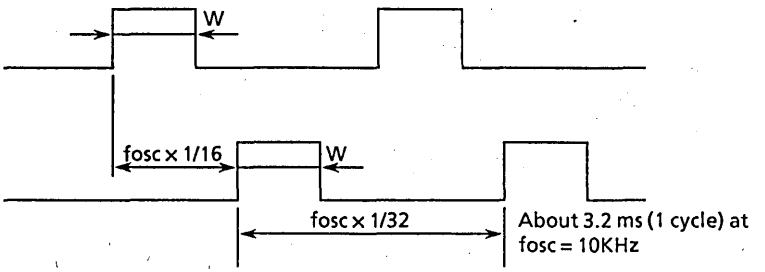
$\overline{\text{P.H.R}}$: This is a peak hold reset terminal. When the terminal is Low, the reset state is fixed. (Peak hold function inhibition state: The peak hold function is performed for an input of − 10 dB or higher.)

OSC: This is a C (capacitor)and R(resistor) oscillation connection terminal to specify the L/R sampling and L/R-Grid switching frequency and the peak hold reset timing.

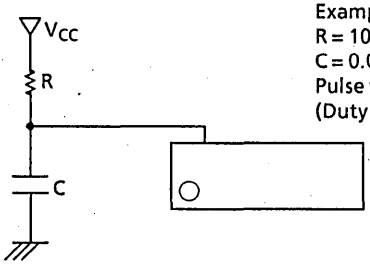


R = 10kΩ
C = 0.022μF
fosc ≒ 10kHz

DUTY: This terminal with a capacitor (C) and a resistor (R) connected is used to adjust the L/R-Grid duty ratio and to change the FLT brightness. When the terminal is fixed Low, the duty ratio is about 1/4.



Wt can be adjusted by C and R. The maximum duty ratio is 1/4.



Example:
R = 10KΩ,
C = 0.046μF,
Pulse width = 270μS
(Duty ratio: About 1/12)

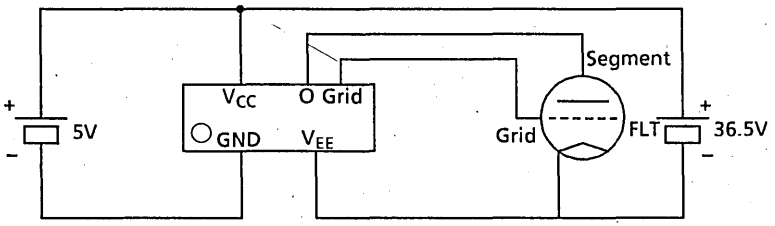
Pulse width calculation method

Wt = 0.587 × C × R(S)

When the value for R is not 10 K, the constant may be slightly changed.

Note: The resistance should not be less than 8K.

VEE: This is a FLT driving supply voltage terminal. The power supply system is as follows:



L/R-Grid: This is a FLT grid driving output terminal. The timing waveform is shown in the illustration for the DUTY terminal. The grid can be directly driven.

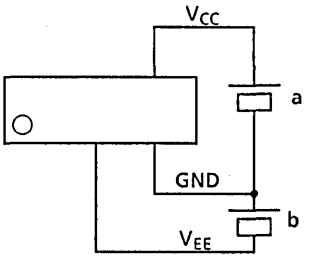
O_1 to O_{15}: These terminals are FLT segment terminal with a pull-down resistor built-in to directly drive the segment.

Note: Precautions for operation

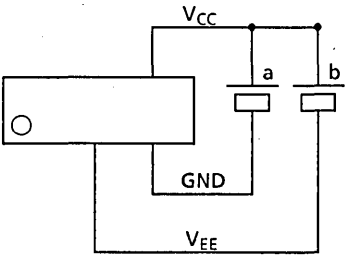
Power ON and OFF sequence

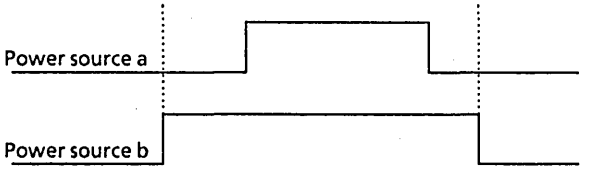
Power connection diagram

1.



2.



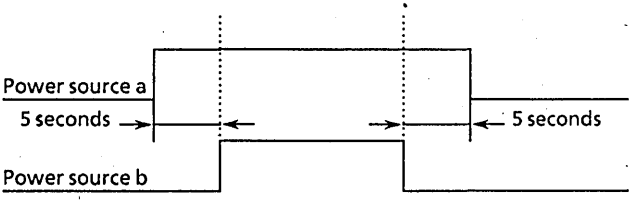


When turning power on, turn the power source b on prior to or simultaneously with the power source a. When turning power off, turn the power source a on prior to or simultaneously with the power source b.

The time difference between a and b should be within 5 seconds as following time chart.

For 5 seconds, a current of 80 to 120mA (VCC = 5V) flows through the power source a.

This is a normal phenomenon. When the power source b is turned on, the system enters the normal state.



THRESHOLD VOLTAGE TABLE

VCC = 5V ± 1%, Ta = 25°C

Parameter	Terminal	Conditions	Specifications			Unit
			MIN	TYP	MAX	
Threshold voltage 1	O_1		9	10	13	dB
Threshold voltage 2	O_2		6	8	9	dB
Threshold voltage 3	O_3		4	5	6	dB
Threshold voltage 4	O_4		1.5	3	4	dB
Threshold voltage 5	O_5		0.5	1	1.5	dB
Threshold voltage 6	O_6	The input should be adjusted to 0 dB.	—	0	—	dB
Threshold voltage 7	O_7		−1.5	−1	−0.5	dB
Threshold voltage 8	O_8		−4	−3	−2	dB
Threshold voltage 9	O_9		−6	−5	−4	dB
Threshold voltage 10	O_{10}		−8.5	−7	−6	dB
Threshold voltage 11	O_{11}		−13	−10	−8.5	dB
Threshold voltage 12	O_{12}		−18	−15	−13	dB
Threshold voltage 13	O_{13}		−25	−20	−18	dB
Threshold voltage 14	O_{14}		−35	−30	−25	dB
Threshold voltage 15	O_{15}	OFF SET should be set to −40 dB.	−45	−40	−35	dB

When the input is set to −60 dB, all DOTs are off. The peak hold function is effective for an input of −10 dB (O_{11}) or higher.

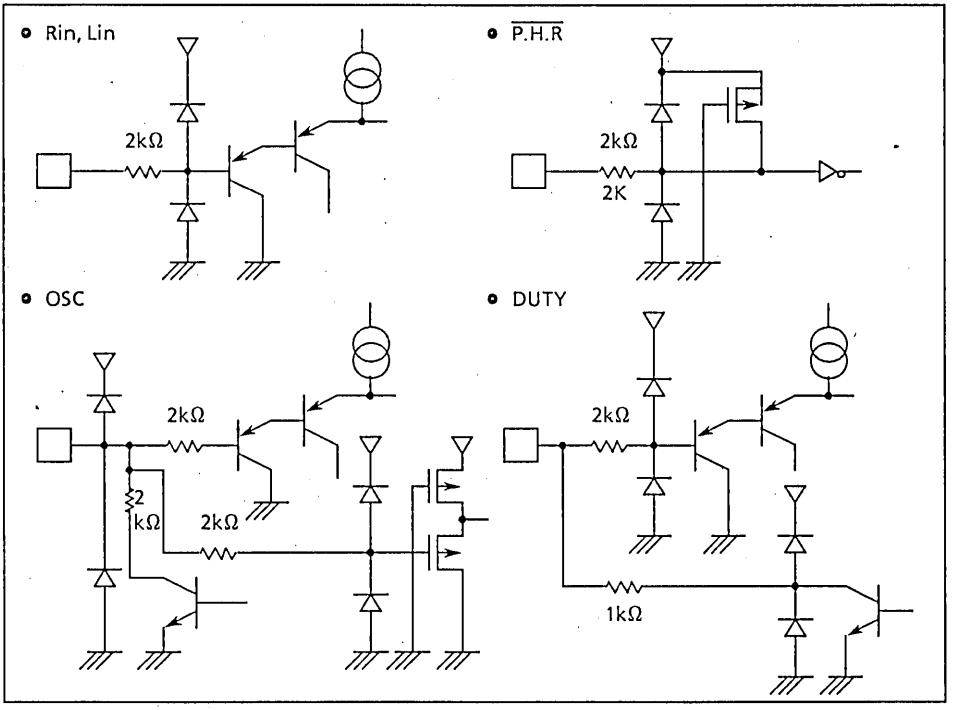
AC INPUT LEVEL VS DC INPUT LEVEL

Threshold voltage	1	2	3	4	5	6	7	8	9	10
Display [dB]	10	8	5	3	1	0	−1	−3	−5	−7
AC input level [mV rms]	782	622	440	349	278	247	221	175	139	110
DC input level [mV]*	1,107	879	622	494	393	350	312	248	197	156

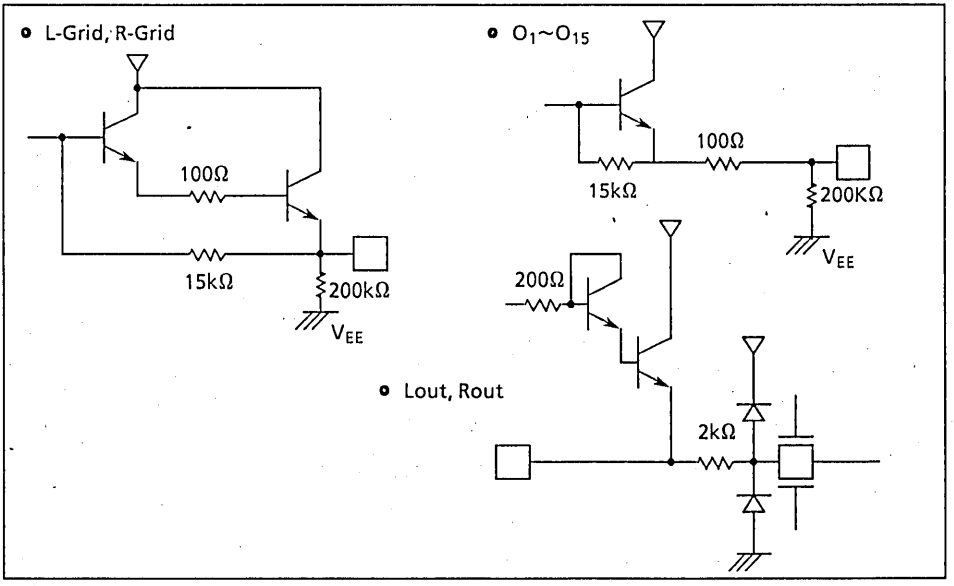
Threshold voltage	11	12	13	14	15
Display [dB]	−10	−15	−20	−30	−40
AC input level [mV rms]	78.5	44.0	24.7	7.85	2.47
DC input level [mV]*	111	62.2	35.0	11.1	3.50

* Input from the Lout or Rout terminal.
The values in the table are TYP values.

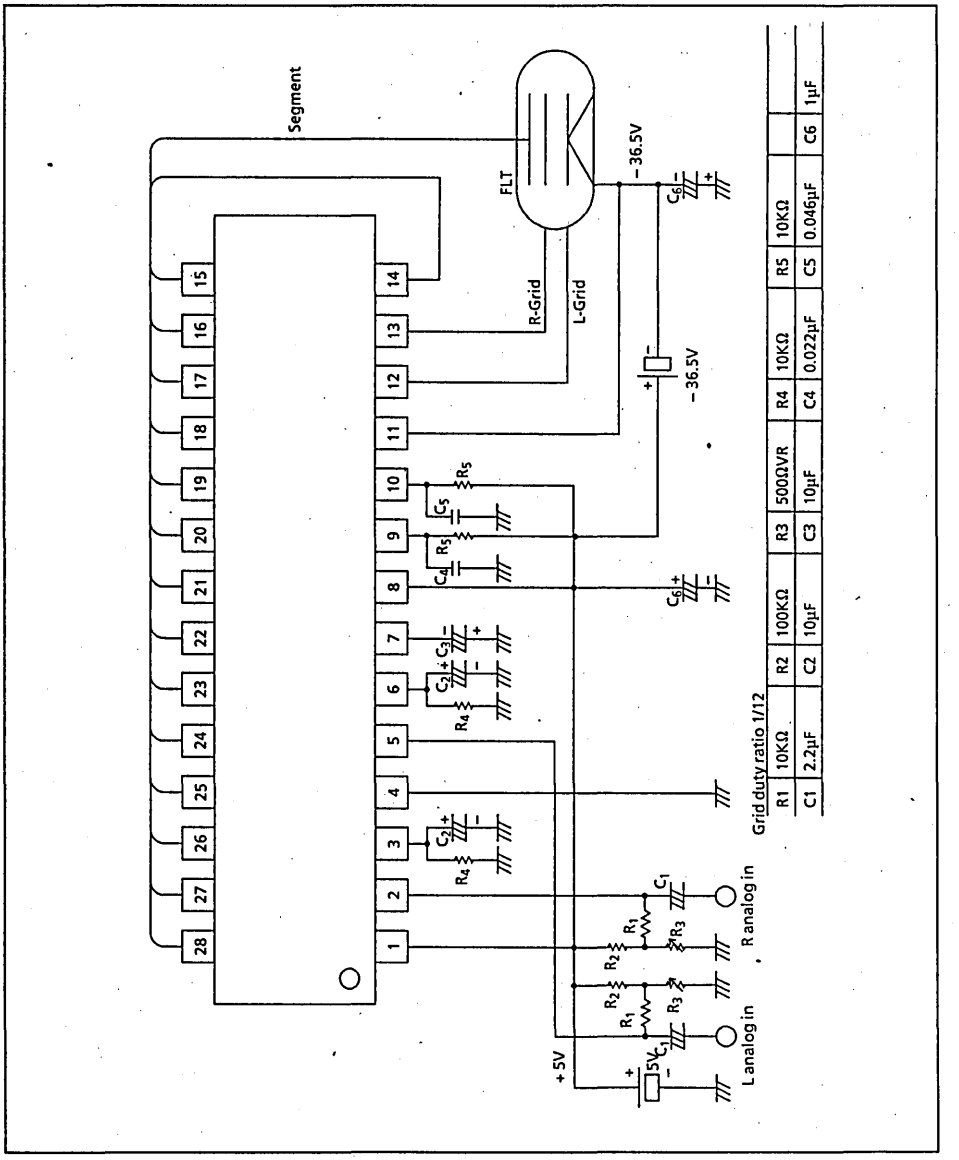
INPUT CIRCUIT



OUTPUT CIRCUIT



APPLICATION NOTE



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One Chip Microcontroller

OKI semiconductor

MSC6458

OKI 4-BIT 1-CHIP MICROCONTROLLER

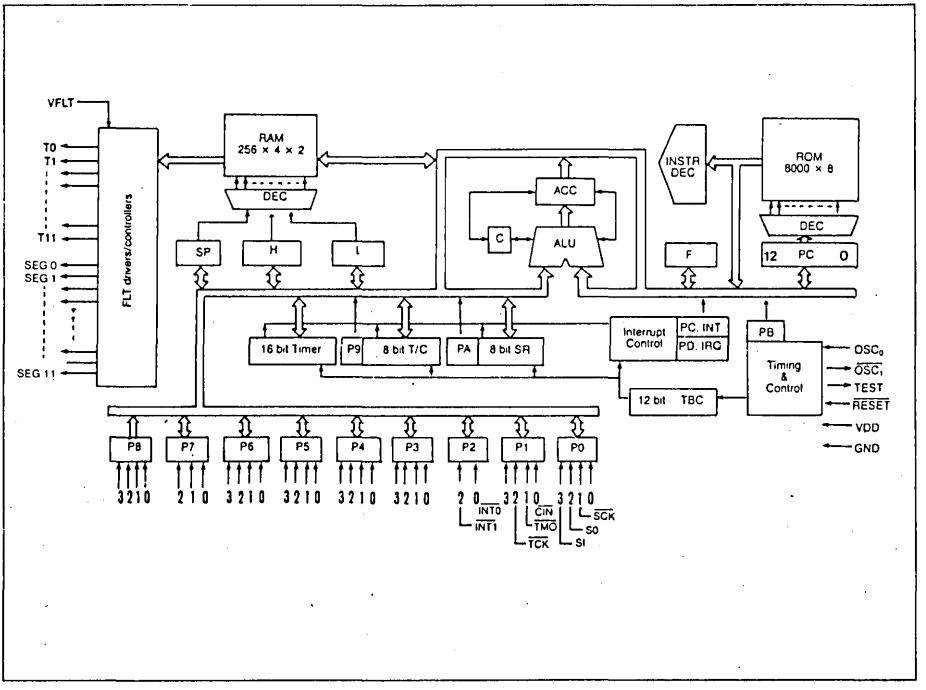
GENERAL DESCRIPTION

The MSC6458 is a high-speed, 4-bit 1-chip microcontroller with built-in FLT drivers/controllers developed to support relatively large control systems.

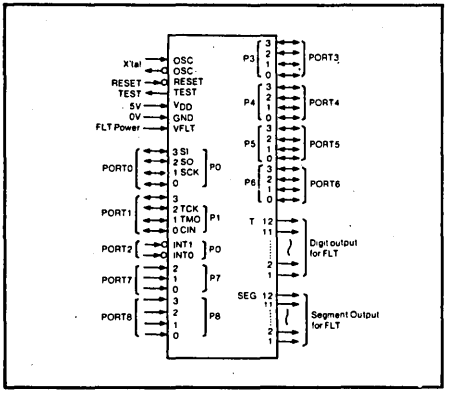
FEATURES

- ROM: 8000 × 8 bits
- RAM: 512 × 4 bits
- Ports: I/O 24 ports (8 having IOL = 20 mA)
  Input 9 (2 also serving as interrupt inputs)
- FLT drivers (Withstand voltage 40V): 12 (IOH = 20mA) 12 (IOH = 6mA)
- LED direct drive available
- Interrupts: 7 lines (2 external, 5 internal)
- Built-in counters: 12 bits, timebase counter
  16 bits, programmable counter
  8 bits, high-speed programmable timer/event counter
- Serial I/O: Built-in 8-bit SIO register
- Oscillation circuit: Crystal or ceramic oscillation
- Number of instructions: 147
- Cycle time: 930 ns (4.3MHz)
- Operating ranges: 4.5 to 5.5V (4.3MHz)
  Voltage: 3.0 to 6.0V (1MHz)
  Temperature: −40 to +85°C
- Power dissipation (typical)
  (display off): 9mA (5V, 4.3MHz)
  2mA (3V, 1MHz)
- Power down: STOP instruction
- Package: 64-pin shrink DIP/64-pin FLAT

BLOCK DIAGRAM

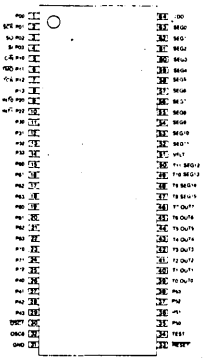


LOGIC SYMBOL



PIN CONFIGURATION (TOP VIEW)

64 PIN PLASTIC SHRINK DIP



PIN DESCRIPTION

Terminal	Input/ Output	Function	When reset
P00 P01/$\overline{SCK}$ P02/SO P03/SI	Input/ Output	I/O port I/O port (also used as serial clock input $\overline{SCK}$) I/O port (also used as serial data output SO) I/O port (also serial data input SI)	"1"
P10/$\overline{CIN}$ P11/$\overline{TMO}$ P12/$\overline{TCK}$ P13	Input/ Output	I/O port (also used as count input $\overline{CIN}$) I/O port (also used as timer output $\overline{TMO}$) I/O port (also used timer clock input $\overline{TCK}$) I/O port	"1"
P20/$\overline{INT0}$ P22/$\overline{INT1}$	Input	Input Port with Latch (falling edge sensitive) also used as interrupt input $\overline{INT0}$ Input Port with Latch ('0' level sensitive) also used as interrupt input $\overline{INT1}$	–
P30 ~ P33	Input/ Output	I/O port	"1"
P60 ~ P63	Input/ Output	I/O port	"0"
P40 ~ P43 P50 ~ P53	Output/ Input	I/O port (I_{OL}=20mA MAX)	"0"
P70 ~ P72 P80 ~ P83	Input	Input port with pull down register Pull down register of P70 ~ P72 can be removed by instruction	
SEG0 ~ SEG11	Output	FLT segment driver (dynamic)	"0"
T11/SEG12 ~ T8/SEG15	Output	FLT segment driver (dynamic)/Timing output	"0"
T7/OUT7 ~ T0/OUT0	Output	FLT segment driver (static)/Timing output	"0"
$\overline{OSC0}$ $\overline{OSC1}$	Input/ Output	Crystal connection terminal for system clock oscillation	–
$\overline{RESET}$	Input	System reset input	–
TEST	Output	Test pin (Open)	–
VFLT	Input	Power supply for FLT driving	–
VDD GND	Input	System Power Supply	–

FUNCTIONAL DESCRIPTION

1. ROM

The ROM, organized in 8 bits, has a maximum capacity of 8000 bytes.

2. RAM

The RAM is organized in 4 bits per word, with a capacity of 512 words.

It is separated into two banks each 256 words long. Bank selection is accomplished via internal ports. The RAM location in the banks is addressed by the H and L registers or by the second byte of each instruction.

3. Ports (24 I/O, 7 input)

The 24 pseudo-bidirectional I/O ports effect or control the exchange of data with external sources. The ports are specified by the L register or by codes contained in instructions. Ports 4 and 5 may draw IOL up to 20mA.

The seven input ports have built-in pulldown resistors. Up to 84 keys can be scanned by assembling them in key matrices with the timing outputs of the FLT drivers (with 12 segments × 12 timings on display; also during automatic display).

4. Interrupt Input Pins (2 terminals)

The $\overline{INT0}$/P20 and $\overline{INT1}$/P22 pins are interrupt input pins. External interrupt request flags of $\overline{INT0}$/P20 pin and $\overline{INT1}$/P22 pin can be set by using interrupt input pins:

$\overline{INT0}$/P20 pin ... positive edge or negative edge input.

$\overline{INT1}$/P22 pin ... "0" level input.

These flags are automatically reset when the appropriate external interrupts occur. These pins are available for use as input ports when not used as interrupt input pins.

5. FLT Drivers/Controllers (Automatic Display)

The FLT drivers have a withstand voltage of 40V in the positive direction from the GND level. They comprise 12 ports that can draw 20mA as IOH (Timing outputs) and 12 ports that can draw 6mA as such (Segment outputs).

A choice of four display modes is supported as listed below. A display RAM area is allocated as part of the RAM space. Data is automatically displayed when transferred to the display RAM. (Two different display frequencies are selectable.) Static output data can be displayed by controlling the FLT drivers by programming.

Display modes (@4.194304 MHz)

(1) 12 Segments × 12 Timings
1/12 duty (85.3/341.3 Hz)

(2) 16 Segments × 8 Timings
1/8 duty (128/512 Hz)

(3) 16 Segments × 4 Timings +4 output*
1/4 duty (256/1024Hz)

(4) 16 Segments+8 output*
Program controlled

*output: static outputs

6. Stack (STACK) and Stack Pointer (SP)

The PC is saved in the stack when an interrupt occurs or a CAL instruction is executed. It is recovered by the execution of an RT instruction.

One fourth of the RAM space (128 words maximum, 32 levels) is available as a stack area. A 4-word RAM area is used for "one" level in the stack.

The stack pointer is an 8-bit up-down counter (the MSB and 2 bits from LSB being fixed at '1') indicating the next stack address to use. It enables the RAM space to be used as a pushdown stack. Data can also be transferred between stack pointer and the H/L registers.

7. Interrupts

Seven interrupt lines are provided for eight sources and eight levels of interrupts as follows (two external inputs):

(1) Display interrupt
Update to timing signals (positive edge)

(2) External interrupt1
Negative edge on the $\overline{INT0}$/P20 pin

(3) External interrupt2
Positive edge on the $\overline{INT0}$/P20 pin

(4) External interrupt3
'0' input on the $\overline{INT1}$/P22 pin

(5) Timebase interrupt
12-Bit timebase counter overflow

(6) Timer interrupt
16-Bit timer and timer register matched signal

(7) Counter interrupt
8-Bit counter and counter register matched signal

(8) Serial/O interrupt
8-Bit shift register shift end signal

8. 12-Bit Timebase Counter

The timebase counter is made up of a 12-bit binary counter. It generates an interrupt request every time it overflows as a result of dividing the OSC0 input 2^{12}.

9. 16-Bit Programmable Timer/Event Counter

Comprising a 16-bit register, a 16-bit binary counter, a comparator circiut, and a control circuit, the programmable timer generates an interrupt request when the register and counter values are matched.

10. 8-Bit High-Speed Programmable Timmer/Event Counter

The high-speed programmable timer/event counter comprises an 8-bit register, an 8-bit binary counter, a comparator circuit, and a control circuit. Starting and stopping the counter can be controlled by instructions. It generates an interrupt request when the register and counter values are matched.

11. 8-Bit Serial I/O

Serial I/O consists of an 8-bit shift register, a 3-bit shift counter, and a control circuit. It is used for serial data input and output. Serial data input and output takes place synchronized with a shift clock, which is selectable between internal and external clocks. The shift counter automatically terminates a data transfer on counting eight shift clock pulses and generates an interrupt request.

12. Registers (Acc, H, L, F)

The accumulator (Acc) is a 4-bit register used to perform data transfers or calculations with the RAM, other registers, ports and so on.

The H and L registers are each a 4-bit register. They transfer data to and from Acc and SP (stack pointer) and address the RAM. The L register is also used to specify ports to use.

The F register is made up of four independent flip-flops. It can be used as a program "flag" or general-purpose register because each of these flip-flops permits set/reset testing and transferring 4-bit parallel data to and from Acc by instructions.

13. Timing Control (TC)

A '0' input on the $\overline{\text{RESET}}$ pin for a certain period initializes internal circuitry and ports.

As the input side of clock pulses, the OSC0 pin accepts clock pulses from an external source. Clock pulses may also be obtained by configuring an oscillation circuit with a crystal oscillator or ceramic resonator connected to OSC0 and $\overline{\text{OSC1}}$.

Load Instructions, etc.

Mnemonic		Code	Bytes	Cycles	Description
LAI	n	90–9F	1	1	A ← n
LLI	n	80–8F	1	1	L ← n
LHI	n	3E · 7n	2	2	H ← n
LHLI	nn	15 · nn	2	2	HL ← nn
LMI	nn	14 · nn	2	2	M (w) ← nn
LAL		21	1	1	A ← L
LLA		2D	1	1	L ← A
LAH		22	1	1	A ← H
LHA		2E	1	1	H ← A
LAM		38	1	1	A ← M
LMA		2F	1	1	M ← A
LAM+		24	1	1	A ← M, L ← L+1, Skip if L = "0"
LAM−		25	1	1	A ← M, L ← L−1, Skip if L = "F"
LMA+		26	1	1	M ← A, L ← L+1, Skip if L = "0"
LMA−		27	1	1	M ← A, L ← L−1, Skip if L = "F"
LAMM	n2	39–3B	1	1	A ← M, H ← H ⊻ n2
LAMD	mm	10 · mm	2	2	A ← Md
LMAD	mm	11 · mm	2	2	Md ← A
X		28	1	1	A ⟷ M
X+		3C	1	1	A ⟷ M, L ← L+1, Skip if L = "0"
X−		2C	1	1	A ⟷ M, L ← L−1, Skip if L = "F"
XM	n2	29–2B	1	1	A ⟷ M, H ← H ⊻ n2
LMT	mm	19 · mm	2	4	M (w) ← T (Md (w), A)
LAF		3E · 54	2	2	A ← F
LFA		3E · 5C	2	2	F ← A
LHLS		3E · 53	2	2	HL ← SP
LSHL		3E · 5B	2	2	SP ← HL
IP		20	1	1	A ← P
OP		23	1	1	P ← A
IPD	p	3D · pD	2	2	A ← Pp
OPD	p	3D · pC	2	2	Pp ← A
OPT		18	1	3	P4, P5 ← T (M (w), A)

Interrupt Control Instructions

Mnemonic	Code	Bytes	Cycles	Description
MEI	3E · 60	2	2	MEIF ← "1"
MDI	3E · 61	2	2	MEIF ← "0"
EIXD	3D · E8	2	2	EIXDF ← "1"
EIXU	3D · E9	2	2	EIXUF ← "1"
EIXL	3D · EA	2	2	EIXLF ← "1"
EIDP	3D · EB	2	2	EIDPF ← "1"
EITB	3D · D8	2	2	EITBF ← "1"
EITM	3D · D9	2	2	EITMF ← "1"
EICT	3D · DA	2	2	EICTF ← "1"
EISR	3D · DB	2	2	EISRF ← "1"
DIXD	3D · E4	2	2	EIXDF ← "0"
DIXU	3D · E5	2	2	EIXUF ← "0"
DIXL	3D · E6	2	2	EIXLF ← "0"
DIDP	3D · E7	2	2	EIDPF ← "0"
DITB	3D · D4	2	2	EITBF ← "0"
DITM	3D · D5	2	2	EITMF ← "0"
DICT	3D · D6	2	2	EICTF ← "0"
DISR	3D · D7	2	2	EISRF ← "0"
TIXD	3D · E0	2	2	Skip if EIXDF = "1"
TIXU	3D · E1	2	2	Skip if EIXUF = "1"
TIXL	3D · E2	2	2	Skip if EIXLF = "1"
TIDP	3D · E3	2	2	Skip if EIDPF = "1"
TITB	3D · D0	2	2	Skip if EITBF = "1"
TITM	3D · D1	2	2	Skip if EITMF = "1"
TICT	3D · D2	2	2	Skip if EICTF = "1"
TISR	3D · D3	2	2	Skip if EISRF = "1"
TQXD	3D · 20	2	2	Skip if IRQXDF = "1"
TQXU	3D · 21	2	2	Skip if IRQXUF = "1"
TQXL	3D · 22	2	2	Skip if IRQXLF = "1"
TQDP	3D · 23	2	2	Skip if IRQDPF = "1"
TQTB	3D · C0	2	2	Skip if IRQTBF = "1"
TQTM	3D · C1	2	2	Skip if IRQTMF = "1"
TQCT	3D · C2	2	2	Skip if IRQCTF = "1"
TQSR	3D · C3	2	2	Skip if IRQSRF = "1"
RQXD	3D · 24	2	2	IRQXDF ← "0"
RQXU	3D · 25	2	2	IRQXUF ← "0"
RQXL	3D · 26	2	2	IRQXLF ← "0"
RQDP	3D · 27	2	2	IRQDPF ← "0"
RQTB	3D · C4	2	2	IRQTBF ← "0"
RQTM	3D · C5	2	2	IRQTMF ← "0"
RQCT	3D · C6	2	2	IRQCTF ← "0"
RQSR	3D · C7	2	2	IRQSRF ← "0"

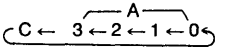
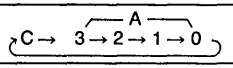
Increment/Decrement Instructions

Mnemonic	Code	Bytes	Cycles	Description
INA	30	1	1	A ← A+1, Skip if A = "0"
INL	31	1	1	L ← L+1, Skip if L = "0"
INH	32	1	1	H ← H+1, Skip if H = "0"
INM	33	1	1	M ← M+1, Skip if M = "0"
DCA	34	1	1	A ← A−1, Skip if A = "F"
DCL	35	1	1	L ← L−1, Skip if L = "F"
DCH	36	1	1	H ← H−1, Skip if H = "F"
DCM	37	1	1	M ← M−1, Skip if M = "F"
INMD mm	12 · mm	2	2	Md ← Md+1, Skip if Md = "0"
DCMD mm	13 · mm	2	2	Md ← Md−1, Skip if Md = "F"

Bit Handling Instructions, etc.

Mnemonic	Code	Bytes	Cycles	Description
TAB n2	54−57	1	1	Skip if A (n2) = "1"
RAB n2	64−67	1	1	A (n2) ← "0"
SAB n2	74−77	1	1	A (n2) ← "1"
TPB n2	50−53	1	1	Skip if P (n2) = "1"
RPB n2	60−63	1	1	P (n2) ← "0"
SPB n2	70−73	1	1	P (n2) ← "1"
TMB n2	58−5B	1	1	Skip if M (n2) = "1"
RMB n2	68−6B	1	1	M (n2) ← "0"
SMB n2	78−7B	1	1	M (n2) ← "1"
TFB n2	5C−5F	1	1	Skip if F (n2) = "1"
RFB n2	6C−6F	1	1	F (n2) ← "0"
SFB n2	7C−7F	1	1	F (n2) ← "1"
TPBD p, n2	3D · p0~3	2	2	Skip if Pp (n2) = "1"
RPBD p, n2	3D · p4~7	2	2	Pp (n2) ← "0"
SPBD p, n2	3D · p8~B	2	2	Pp (n2) ← "1"
TC	09	1	1	Skip if C = "1"
RC	08	1	1	C ← "0"
SC	07	1	1	C ← "1"

Arithmetic Instructions

Mnemonic	Code	Bytes	Cycles	Description
ADCS	01	1	1	C, A ← C+A+M, Skip if C = "1"
ADS	02	1	1	A ← A+M, Skip if Cy = "1"
ADC	03	1	1	C, A ← C+A+M
AIS n	3E · 4n	2	2	A ← A+n, Skip if Cy = "1"
DAA	06	1	1	A ← A+6
DAS	0A	1	1	A ← A+10
AND	0D	1	1	A ← A ∧ M
OR	05	1	1	A ← A ∨ M
EOR	04	1	1	A ← A ⊻ M
CMA	0B	1	1	A ← $\overline{A}$
CIA	0C	1	1	A ← $\overline{A}$+1
RAL	0E	1	1	
RAR	0F	1	1	
CAM	16	1	1	Skip if A = M
CAI n	3E · 0n	2	2	Skip if A = n
CMI n	3E · 1n	2	2	Skip if M = n
CLI n	3E · 2n	2	2	Skip if L = n
CPI p, n	17 · pn	2	2	Skip if Pp = n

Branch Instructions, etc.

Mnemonic	Code	Bytes	Cycles	Description
JCP a6	C0–FF	1	1	PC ← a6
JA	1A	1	2	PC ← (PC ← A) +1
JM	1B	1	2	PC ← (M (w), A)
JP a12	40–4F 00–FF	2	2	PC ← a12
CAL a12	A0–AF 00–FF	2	4	ST ← PC+2, PC ← a12, SP ← SP–4
CZP a	Ba	1	4	ST ← PC+1, PC ← 2a, SP ← SP–4
LJP a13	3F 3F 00–1F 00 FF	3	4	PC ← a13
LCAL a13	3F 3F 80–9F 00 FF	3	4	ST ← PC+3, PC ← a13, SP ← SP–4
RT	1E	1	4	PC ← ST, SP ← SP+4
RTS	1F	1	4	PC ← ST, SP ← SP+4, then Skip

Counter Control Instructions, etc.

Mnemonic	Code	Bytes	Cycles	Description
LCTM	3E · 51	2	2	CTR ← M (w)
LMCT	3E · 59	2	2	M (w) ← CT
ECT	3D · BB	2	2	CTF ← "1" (Counter Start)
DCT	3D · B7	2	2	CTF ← "0" (Counter Stop)
TCT	3D · B3	2	2	Skip if CTF = "1"
LTMM	3E · 50	2	3	TMR ← M (2w)
LMTM	3E · 58	2	3	M (2w) ← TM
LSRM	3E · 52	2	2	SR ← M (w), SC ← "0" SC: Shift Counter
LMSR	3E · 5A	2	2	M (w) ← SR
ESR	3D · BA	2	2	SRF ← "1" (Shift Register Start)
DSR	3D · B6	2	2	SRF ← "0" (Shift Register Stop)
TSR	3D · B2	2	2	Skip if SRF = "1"

CPU Control Instructions, etc.

Mnemonic	Code	Bytes	Cycles	Description
PUSH	1C	1	3	ST ← C, A, H, L, SP ← SP−4
POP	1D	1	3	C, A, H, L ← ST, SP ← SP+4
HALT	3D · B8	2	2	Halt CPU
STOP	3D · B9	2	2	Stop CPU
NOP	00	1	1	No Operation

Explanations of Instruction Symbols

A	: Accumulator (4-bit)
H	: H register (4-bit)
L	: L register (4-bit)
F	: F register (4-bit)
M	: RAM word addressed by the H and L registers
Md	: RAM word addressed by second byte of an instruction code
M (w)	: Two RAM words addressed by the H and L register/H3-0 and L3-1 (8-bit)
Md (w)	: Two RAM words addressed by second byte of an instruction code (8-bit)
M (2w)	: Four RAM words addressed by the H and L register/H3-0 and L3-2 (16-bit)
ST	: Four RAM words (16-bit) allocated as a stack area
SP	: Stack pointer (8-bit)
PC	: Program counter
P	: Port specified by the L register (4-bit)
$\bar{P}p$	: $\bar{P}$ort specified by 4 high-order bits of second byte of an instruction code (4-bit)
CTR	: 8-Bit counter/register
CT	: 8-Bit programmable counter
CTF	: Programmable counter start flag
TMR	: 16-Bit timer/register
TM	: 16-Bit programmable timer
SR	: 8-Bit shift register
SRF	: Shift register start flag
(X, Y)	: ROM address data specified by a11-4 as X and a3-0 as Y (12-bit)
T (X, Y)	: ROM table data specified by a11-4 as X and a3-0 as Y (8-bit)
n	: Immediate data (4-bit)
nn	: Immediate data (8-bit)
n2	: Two low-order bits of an instruction code
(n2)	: Bit specified by the two low-order bits of an instruction code
a	: ROM address data
aX	: ROM address data (X-bit)
mm	: RAM address data (8-bit)
C	: Carry flag
Cy	: Flag indicating a carry in a calculation result

ELECTRIC CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions		Limits	Unit
Supply Voltage	V_{DD}			−0.3 ~ 7	V
Indicated Supply Voltage	V_{FLT}	Ta = 25°C		V_{DD} ~ 45	V
Input Voltage	V_I			−0.3 ~ V_{DD}	V
Input Voltage	V_O	Ta = 25°C	Input/output	−0.3 ~ V_{DD}	V
			Indicated output	−0.3 ~ V_{FLT}	V
"H" Output Current (Indicated Output)	I_{OH}	Per pin	SEG0 ~ SEG1	10	mA
			T0 ~ T11	40	mA
			OUT0 ~ OUT7	* 30	mA
		Output terminal total	SEG0 ~ SEG11	72	mA
			T0 ~ T11	72	mA
"L" Output Current (P4, P5)	I_{OL}	Per terminal		20	mA
		P4 total		40	mA
		P5 total		40	mA
Power Dissipation	P_D	Per package		600	mW
		Per input/output terminal		50	mW
Storage Temperature	Tstg	−		−55 ~ +150	°C

* When timing output is used as static output

• Operating Conditions

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	f (osc) ≦ 4.3MHz	4.5 ~ 5.5	V
		f (osc) ≦ 1MHz	3 ~ 6	V
Indicated Supply Voltage	V_{FLT}	−	10 ~ 40	V
Memory Retension Voltage	V_{DDH}	Oscillation off	2 ~ 6	V
Operating Temperature	Topr	−	−40 ~ +85	°C
(Fan Out (Input/Output Port)	N	MOS Load	15	−
		TTL Load	1	−

• DC Characteristics

(V_{DD} = 5V ±10%, Ta = −40 ~ +85°C)

Parameter	Terminal applied	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	*1	V_{IH}	−	2.4	−	V_{DD}	V
	OSC0, RESET		−	3.8	−	V_{DD}	V
	P7, P8		−	3.4	−	V_{DD}	V
"L" Input Voltage	*2	V_{IL}	−	0	−	0.8	V
	P7, P8		−	0	−	1.6	V
"H" Output Voltage	*3	V_{OH}	IO = −15μA	4.2	−	−	V
	SEG0 ~ SEG11		IO = −6mA	V_{FLT}-2.5	−	−	V
	T0 ~ T11		IO = −20mA	V_{FLT}-3.5	−	−	V
"L" Output Voltage	P0, P1, P3, P6	V_{OL}	IO = 1.6mA		−	0.4	V
	P4, P5		IO = 10mA		−	0.8	V
	OSC1		IO = 15μA		−	0.4	V
	SEG0 ~ SEG11		IO = 1mA		−	1.6	V
	T0 ~ T11		IO = 1mA		−	1.4	V
"H" Input Current	OSC0	I_{IH}	VI = VDD		−	15	μA
	P2, RESET				−	1	μA
	P7(P73=0), P8				−	60	μA
	P7(P73=1)				−	1	μA

Parameter	Terminal applied	Symbol	Conditions	Min.	Typ.	Max.	Unit
"L" Input Current	OSC0	I_{IL}	VI = 0V	–	–	−15	μA
	P2, $\overline{RESET}$			–	–	−30	μA
	P7, P8			–	–	−1	μA
"H" Output Current	P0, P1, P3,	I_{OH}	VO = 2.4V	−0.1	–	–	mA
	P4, P5, P6		VO = 0.4V	–	–	−1.2	mA
Current Consumption		I_{DD}	No load f (osc) = 4.3MHz	–	12	20	mA
Current Consumption (When stop mode condition)		I_{DDS}	No load	–	1	100	μA
			No load V_{DD} = 2V Ta = 25°C	–	0.5	10	μA
Current Consumption (FLT driver section)		I_{FLT}	No load All FLT driver, "L" level	–	2	100	μA

*1. Applied to P0, P1, P2, P3, P4, P5, P6
*2. Applied to P0, P1, P2, P3, P4, P5, P6, OSC0, RESET
*3. Applied to P0, P1, P3, P4, P5, P6, OSC1

• AC Characteristics

(V_{DD} = 5V ±10%, Ta = 40 ~ +85°C)

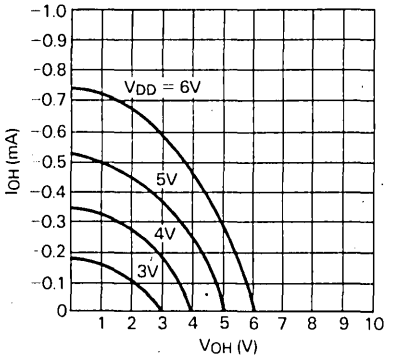
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock (O.S.C $_0$) Pulse Width	$t_{\phi W}$	–	116	–	–	nS
Cycle Time	t_{CY}	–	928	–	–	nS
Input Data Setup Time	t_{DS}	–	120	–	–	nS
Input Data Hold Time	t_{DH}	–	120	–	–	nS
P2 Input Data Pulse Width	t_{DWP2}	Note 1	120	–	–	nS
SR Clock. Pulse Width	t_{DW1}	–	120	–	–	nS
CT Clock. Pulse Width	t_{DW2}	–	2/8t_{CY}+120	–	–	nS
TM Clock. Pulse Width	t_{DW3}	–	t_{CY}+120	–	–	nS
SR Data Setup Time	t_{SS}	–	120	–	–	nS
SR Data Hold Time	t_{SH}	–	120	–	–	nS
SR Clock Invalid Time *	t_{SINH}	–	2/8tcy	–	–	nS
Data Delay Time	t_{DR}	C_L = 15pF	–	–	300	nS
SR Clock Delay Time	t_{SP}	C_L = 15pF	–	–	360	nS
Reset Input. Rise Time	t_{WRS}	Note 2	2tcy	–	–	nS
Segment Output. Rise Time	t_{TLHS}	VFLT = 40V	–	–	3	μSS
Segment Output. Rise Time	t_{THLS}	C_{LD} = 15pF	–	–	1	μS
Timing Output. Rise Time	t_{TLHT}	VFLT = 40V	–	–	3	μS
Timing Output. Rise Time	t_{THLT}	C_{LD} = 15pF	–	–	1	μS

*1. When stop mode is to be released by "L" level input from P20/INT0, it is necessary to keep the pulse width of more than oscillation stability time for OSC_0.
*2. This indicates when OSC_0 oscillation is stabilized. However, when stop mode is released by reset input, the pulse width of more than OSC_0 oscillation stability time as requested.
*3. t_{SINH}: When shift register commands LMSR during shift in operation, its inner part will not change if clock, which inputs P01/SCK during t_{SINH} period, changes.

STANDARD CHARACTERISTICS

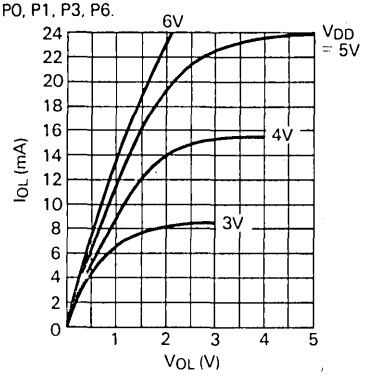
- **"H" Output Current I_{OH} – Output Voltage V_{OH} Characteristics (Ta = 25°C)**

P0, P1, P3, P4, P5, P6

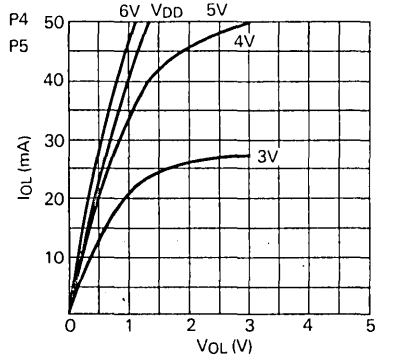


- **"L" Output Current I_{OL}– Output Voltage V_{OL} Characteristics (Ta = 25°C)**

P0, P1, P3, P6.

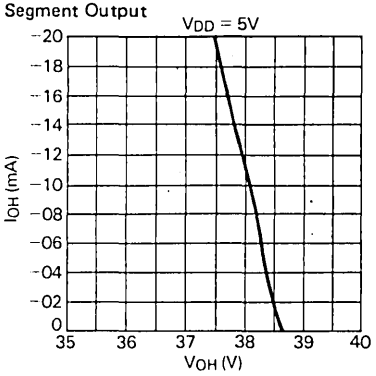


- **"L" Output Current I_{OL}– Output Voltage V_{OL} Characteristics (Ta = 25°)**



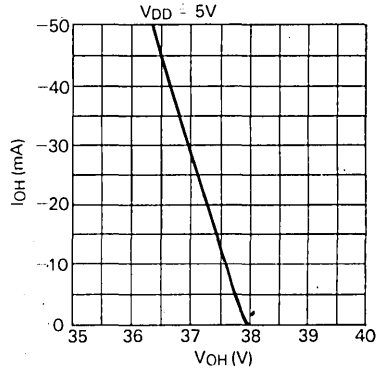
- **"H" Output Current I_{OH}– Output Voltage V_{OH} Characteristics (Ta = 25°C, VFLT = 40V)**

Segment Output



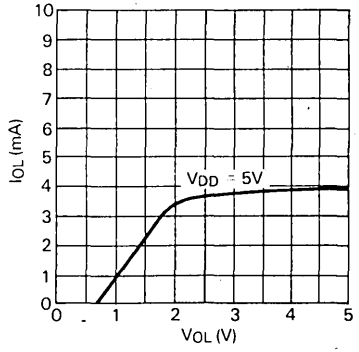
- **"L" Output Current I_{OH}– Output Voltage V_{OL} Characteristics (Ta = 25°C, VFLT = 40V)**

Timing Output



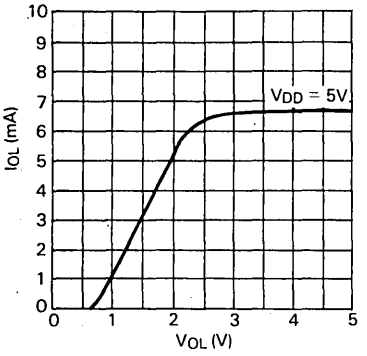
- **"L" Output Current I_{OL}– Output Current V_{OL} Characteristics (Ta = 25°C, VFLT = 40V)**

Segment Output

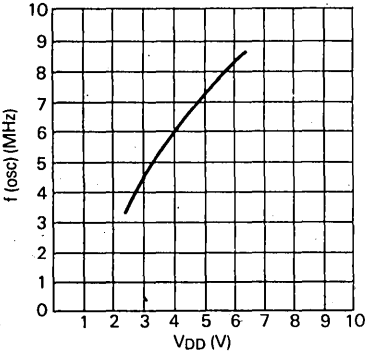


- **"L" Output Current I_{OL} — Output Current V_{OL} Characteristics (Ta = 25°C, VFLT = 40V)**

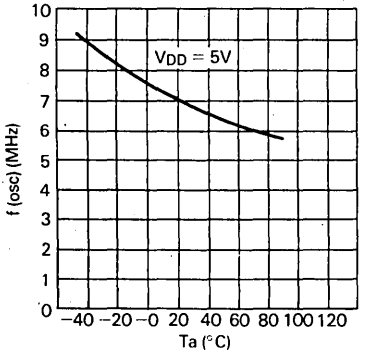
Timing Output



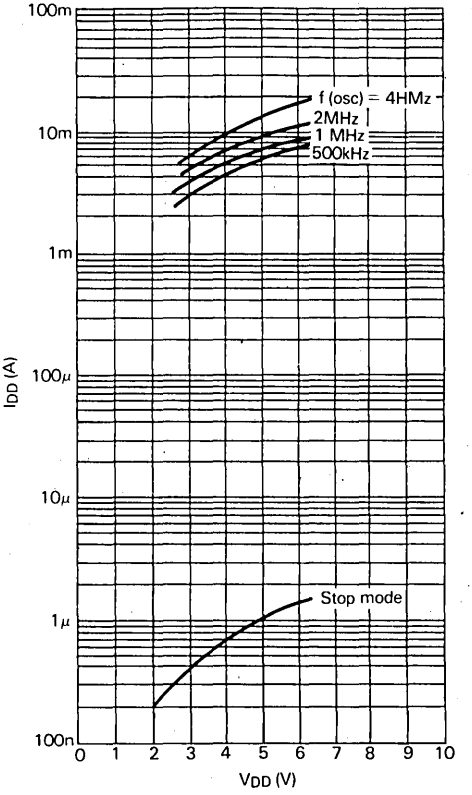
- **Maximum Clock Freqency f(osc) — Supply Voltage V_{DD} Characteristics ($Ta = 25°C, C_L = 15pF$)**



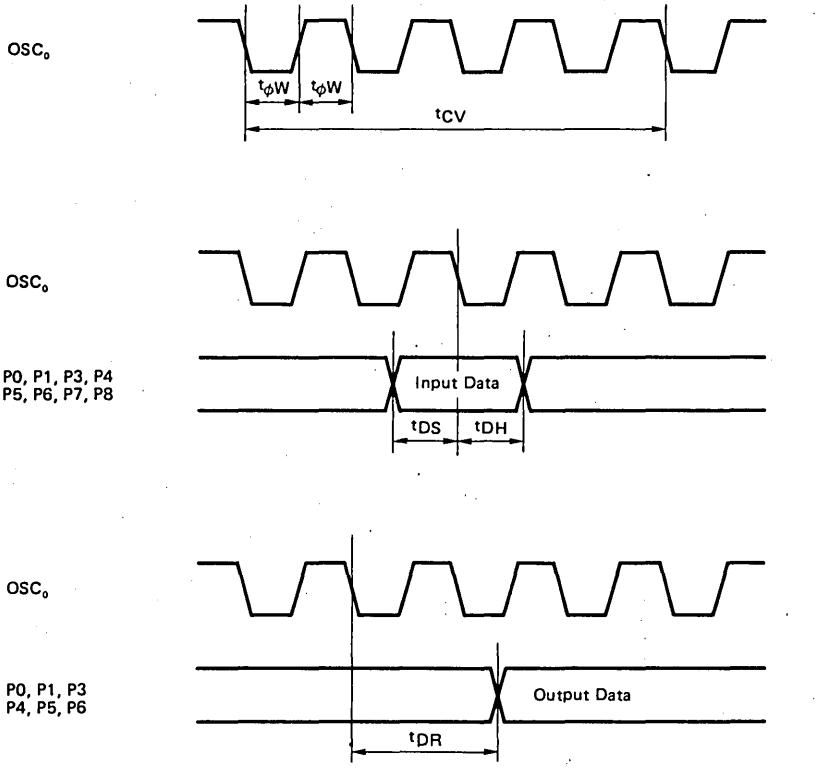
- **Maximum Clock Frequency f(osc) — Ambient Temperature Ta (V_{DD} = 5V, C_L = 15pF)**

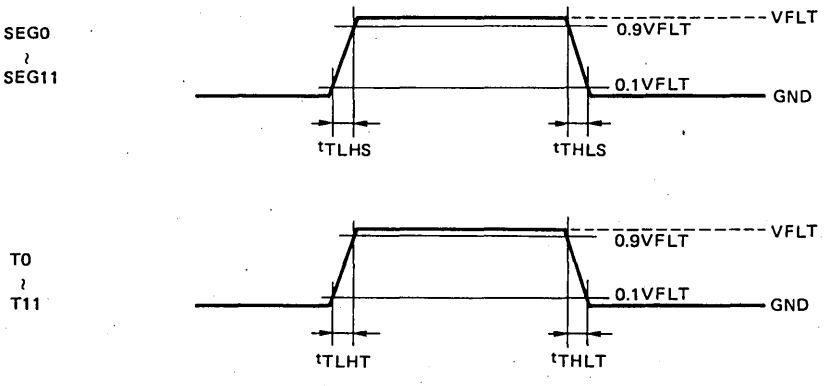


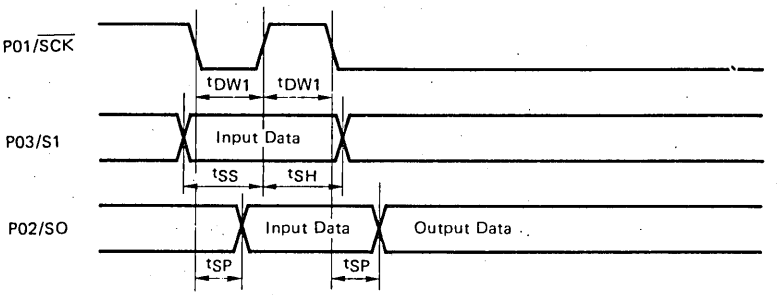
- **Current Consumption I_{DD} — Supply Voltage V_{DD} ($Ta = 25°C$, No load)**

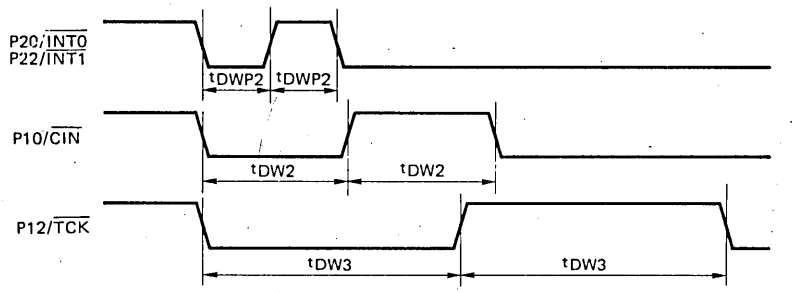


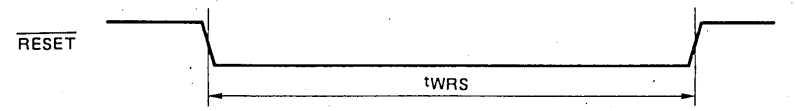
TIMING CHART

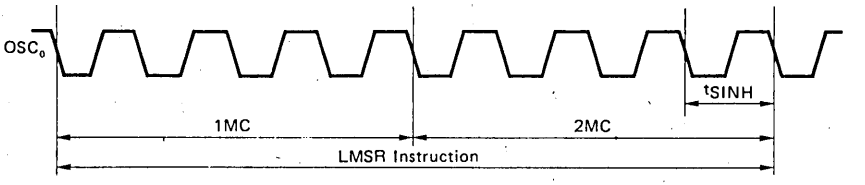





P01/SCK
tDW1
tDW1
P03/S1
Input Data
tSS
tSH
P02/SO
Input Data
Output Data
tSP
tSP


P20/INT0
P22/INT1
tDWP2
tDWP2
P10/CIN
tDW2
tDW2
P12/TCK
tDW3
tDW3


RESET
tWRS


OSC0
tSINH
1MC
2MC
LMSR Instruction

OKI

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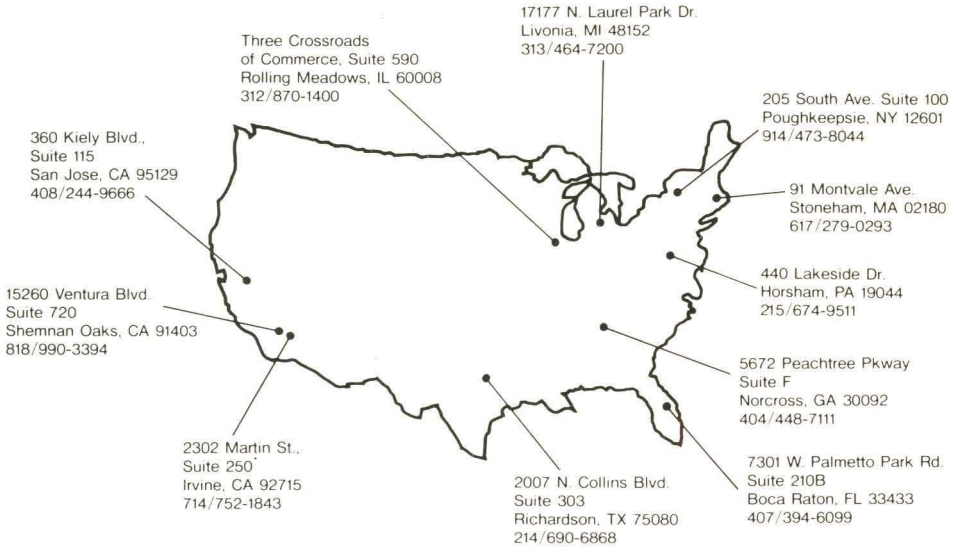
For further information please contact:



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