RM-9465
GRAPHIC DISPLAY SYSTEM
Hardware Reference Manual

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Ramtek

2211 Lawson Lane
Santa Clara, California 95050

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device persuant to subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Ramtek reserves the right to change, without notice, the specifications and materials contained herein. Moreover, Ramtek shall not be responsible for damages caused by erroneous information such as typographical and arithmetic errors.

LIST OF EFFECTIVE PAGES

Changes, deletions, and additions to information in this manual are indicated by bars in the margins or by an asterisk near the page number if the entire page is affected.

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Title	A
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Chapter 1

GENERAL INFORMATION

1.1 INTRODUCTION

The 9465 product line is designed and manufactured by Ramtek Corporation, 2211 Lawson Lane, Santa Clara, California 95050. This hardware reference manual provides a qualified technician with all the information necessary to install, configure, operate, and maintain the 9465.

1.2 HOW TO USE THIS MANUAL

This manual is a single volume reference for the 9465 operator or technician. Chapters and appendices are as follows:

- Chapter 1 - General Information
- Chapter 2 - Installation
- Chapter 3 - Operation
- Chapter 4 - Functional Description
- Chapter 5 - Maintenance
- Chapter 6 - Parts List
- Appendix A - Glossary
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1.2.1 General Information

Chapter 1 gives an overview of the manual, a summary of related documents, safety precautions and warnings, Ramtek service information, and a detailed equipment description.

1.2.2 Installation

Chapter 2 contains receiving and reshipping information and detailed facility requirements. System configuration, turn-on, checkout, and expansion are included.

1.2.3 Operation

Chapter 3 describes and locates 9465 controls and indicators. Instructions include turn-on, operation, and turnoff.

1.2.4 Functional Description

Chapter 4 contains a functional description. Following a discussion of 9465 concepts, functional elements are described and analyzed.

1.2.5 Maintenance

Chapter 5 contains preventive, corrective, removal, and replacement procedures.

1.2.6 Parts List

Chapter 6 contains parts information and ordering procedures.

1.2.7 Glossary

Appendix A lists glossary terms and abbreviations encountered in graphic display systems.

1.2.8 Index

Appendix B lists manual topics referenced to page numbers.

1.3 MANUAL REVISION INFORMATION

Periodically, a change package or a reissued manual is published to stay current with circuit and component improvements as they develop and are tested. This manual has the following revision information:

- List of effective pages
- Request for changes form
- Reader comment form
- Notice of changes (not included in new or reissued manuals)

1.3.1 List of Effective Pages

This is a list of all manual pages referenced to current revision number. Ramtek publishes a list of effective pages each time a manual is issued, reissued, or a change package is issued. Insert the list of effective pages when you add or delete change pages.

1.3.2 Request for Changes Form

If you wish to receive changes, please fill out and mail the self-addressed postcard at the front of this manual. You will then receive change packages as they are published.

1.3.3 Reader Comment Form

Ramtek Technical Publications Department supplies a self-addressed reader comment form to obtain user feedback. Please enter any comments, suggestions, or complaints on the form. Include page, paragraph, figure, or table number as applicable. The reader comment form is inserted after the last manual page.

1.3.4 Notice of Changes

A notice of changes will accompany each change package. Follow the information in the notice when inserting and deleting pages. New or reissued manuals

do not require a notice of changes.

1.4 RELATED DOCUMENTS

Peripherals that connect to the 9465 are documented in separate manuals. Table 1-1 lists peripheral manuals, reference manuals for related Ramtek products, and commercial publications.

The information supplied under date and issue columns was correct when this manual was published. Request the latest issue when ordering.

1.5 SAFETY

This paragraph has important safety information that you should read and understand before installing, operating, or servicing the 9465. Only qualified maintenance technicians should service or adjust internal components. Never reach into the equipment unless someone who can render aid is present.

Throughout this manual you will encounter safety warning and caution notices. A warning alerts you to conditions that could result in personal injury, loss of life, or long-term health impairment. A caution alerts you to conditions that could result in damage to, or destruction of, equipment.

1.5.1 Electrical Safety

The 9465 is equipped with a switching power supply. Therefore, you could encounter high voltage capable of causing death or serious injury; be extremely cautious when servicing equipment with power applied. The following warning is inserted before all hazardous procedural steps.

WARNING

High voltage capable of causing death or serious injury exists when power is applied and internal components are exposed.

Within the 9465, signal ground is isolated from earth ground, but the chassis can develop an electric charge if leakage occurs between the low side of the ac supply and the chassis. This condition can pose a definite health hazard to anyone touching the cabinet. For this reason, you must ground the chassis, via the power cable, to earth ground.

WARNING

To avoid serious injury or death, verify that chassis ground is connected to a good earth ground.

Table 1-1. Related Documents

Title	Date	Issue
Ramtek RM-9460 Software Reference Manual	September 1982	8000081-01A
VAX/VMS RM-9400/RM-9460 Device Driver	1983	8000085-01A
RM-9400 Series Graphics Display System Internal Programming Manual	September 1981	01A
Advanced Micro Devices Bipolar Microprocessor Logic And Interface Data Book	1981	02
Zilog Z80A-CPU	1977	--
RM-9400/9460 Diagnostic and Acceptance Test Operators Manual for VAX/VMS System	October 1983	800088-01
Bit Pad One Users Manual, Summagraphics Corporation		May 1969
Ramtek General Purpose Keyboard Hardware Reference Manual		--
Ramtek GM-850 Series Graphic Monitor Hardware Reference Manual	1980	504615 F
Ramtek General Purpose Interface Manual RM-9000	--	503161
DEC PDP11 Interface Manual	--	8000094-01A
Interdata Interface Manual	--	503173
AN/UYK-7 Interface Manual	--	8000117-01A
HP 21XX Interface Manual	--	504309
Varian 73 Interface Manual	--	503168
Data General Interface Manual	--	503167
2701 PDA Interface Manual	--	503176
Cursor Controller Manual	--	8000129-01A
GC-104 Trackball Manual	--	8000130-01A
DEC LSI-II Interface Manual	--	8000033
GC-105 Lightpen Manual	--	80000018

The 9465 is shipped with a three-conductor power cable and corresponding three-conductor plug. The 120 Vac power plug (NEMA 5-20P) has three prongs; one prong connects to the high side of the ac supply, one prong connects to the low side, and the third, offset, prong connects to ground. At the installation site, the mating power receptacle must have the ground socket tied to a good earth ground. Chapter 2 has additional grounding information.

1.5.2 Fire Safety

Warning systems are available that detect overheating or smoke before a fire becomes apparent. Detection systems designed for installations requiring fire protection or special building construction are listed in the National Fire Protection Association (NFPA) Standard Number 75. To obtain a copy of this standard, write to:

National Fire Protection Association
470 Atlantic Avenue
Boston, Massachusetts 02210

Fire control requirements are normally included in local building codes, and your insurance carrier can recommend appropriate fire control apparatus. Since water based systems can damage electronic equipment, Ramtek recommends carbon dioxide.

1.6 FCC COMPLIANCE

The 9465 complies with FCC requirements for a Class A computing device when installed and operated as directed in this manual. The cabinet front access panel must remain closed when power is applied. During installation, you must tighten the screws that fasten peripheral cables to respective jacks. Likewise, all BNC connectors must mate securely to avoid unwanted radio-frequency interference (RFI).

1.7 RAMTEK SERVICE

Ramtek maintains a complete Field Engineering Department which includes on-site service, depot repair facilities, and a full staff of technical specialists. For special situations or problems that cannot be resolved by our field offices, Ramtek specialists are available for phone consultation, or if necessary, for on-site consultation.

Ramtek maintenance agreements cover complete on-site service including all parts, labor, and expenses for Field Engineer on-site support. If a one-year maintenance agreement is purchased with the 9465, Ramtek will provide on-site installation and checkout in lieu of the 90-day, F.O.B. factory warranty. If installation is purchased with the 9465, we will not only install the hardware, but upgrade the 90-day factory warranty to on-site. On-site service is also available on a time and material basis.

Ramtek maintains a full service depot to repair or exchange modules during or after the warranty period. You must obtain prior approval and a request for material authorization (RMA) number before returning any merchandise to the depot. Parts must be shipped prepaid.

For additional information regarding service offered by Ramtek's Field Engineering Department, call your local Ramtek Office or call Field Engineering, at (408) 988-2211.

1.8 DESCRIPTION

This paragraph describes physical aspects of 9465 components and supplies information about peripherals and accessories. Electrical, functional, and environmental specifications are also described.

1.8.1 Components

Modular 9465 components (table 1-2) simplify maintenance and enhance configuration flexibility. Official Ramtek nomenclature, common names, and part numbers appear in table 1-2.

Table 1-2. 9465 Components

Official Description	Common Name	Part Number
9465 Final Deskside Assembly	Deskside Assembly	509500
Frame Subassembly	Frame Subassembly	509501
Processor PCB	System Processor (Z80)	504047
Processor PCB	System Processor (MC68000)	508217
Serial Link Cursor PCB	Serial Link PCB	504075
MCP 2 PCB	MCP PCB	508221
Sync PCB	Sync PCB	508268
10X12 Memory PCB	Memory PCB	508072*
Video 12 PCB	Video 12 PCB	506407*
Processor Expansion II PCB	Expansion PCB	504907
Video 1 PCB	Video 1 PCB	504079
Video 7 PCB	Video 7 PCB	505955*
Video 8 PCB	Video 8 PCB	505542
Video Load PCB	Video Load PCB	504970
Pixel Formatter PCB	Pixel Formatter PCB	505508
Transform Processor PCB	Transform PCB	506577
Fan Plate Assembly	Fan Plate Assembly	509489
Power Supply (5V/12V)	Power Supply	509484

* Manufactured in an A or B configuration.

A specific 9465 may not have all of these components, and component part numbers may vary depending upon date of manufacture and configuration. Depending upon site power availability, you can order the 9465 in a 120 Vac version or a 220 Vac version.

For some applications, an interface PCB may be desirable. Ramtek manufactures nine interface PCBs (table 1-3). Four interface PCBs install in the 9465: the GPIF, the UYK IF, the Varian IF, and the IBM IF. The other five interface PCBs install in the corresponding host computer.

Peripherals and monitors are listed in table 1-4. Monitors are available for color or monochrome applications. Screen sizes are 13-, 19-, and 25-inches measured diagonally. A "-C" means cabinet mounted; an "-R" means rack mounted. The designation "LP" means long persistence phosphor. Please note that some peripheral options require specific 9465 configurations. Consult your Ramtek sales representative when ordering.

Accessories include miscellaneous hardware items, cables for peripheral devices, and a test extender PCB. Standard peripheral cables are manufactured in 25, 50 or 100 foot lengths. Non-standard length cables are available, subject to factory quotes.

1.8.2 Physical Description

The 9465 (figure 1-1) is a modularized cabinet-enclosed device that processes text, image, or graphics data for display in monochrome or color. A standard 9465 consists of a unibody cabinet made up of a frame subassembly, a fan plate assembly, and printed circuit boards (PCBs). The cabinet has a hinged front access panel and a hinged rear access panel (removed for clarity in figure 1-1).

An identification plate is affixed to the floor of the air intake opening. This plate is printed with the model, operating voltage, operating current, and serial number.

1.8.2.a Frame Subassembly. The frame subassembly (figure 1-2) is formed of sheet metal and supports subassemblies which fasten with screws. Components include

- Input/output (I/O) panel assembly
  - J1 is red video (or monochrome monitor 1)
  - J2 is green video (or monochrome monitor 2)
  - J3 is blue video (or monochrome monitor 3)
  - J4 is one of up to six extra video connectors (J4-J9)
  - J101 is one of up to eight peripheral cable connectors (J101-108)
  - J201 is a host computer cable connector
  - J301 is for future use
- AC panel assembly
- AC bracket assembly
- Rear fan assembly
- Power supply
- Control panel
- Backplane assembly

The I/O panel assembly is a junction point for video cables, peripheral cables, and a host computer cable. Depending upon configuration ordered, this panel can have up to nine BNC connectors and eight 9-pin connectors. Unused positions are either plugged or sealed off with a plate. Cables connect the I/O panel assembly to the PCBs and the backplane assembly.

Table 1-3. Interface PCBs and Cables

Model Number	Description	Prerequisite	Standard Cable Length (ft.)
RM-9465-40	General purpose bidirectional interface. Operation in PIO and DMA modes.		Not provided (mating connector provided)
RM-9465-53A	DEC PDP-11 Series bidirectional interface. Operation in PIO and DMA modes. Uses one SPC slot.	Non-processor grant line at the interface slot for DMA operation	50
RM-9465-54	DEC LSI-11 Series bidirectional Q-bus interface. Operation in QIO and DMA modes.	Non-processor grant line at the interface slot for DMA operation	50
RM-9465-56	Interdata 7/8XX Series bidirectional interface to programmed I/O multiplexer bus or SELCH.	M48-13 compatible card (provided)	50
RM-9465-59	Univac AN/UYK-7 bidirectional interface to NAVY Type B (NTDS FAST) digital data interface (0V, -3V logic levels). Usually a DMA interface. See MIL-Std. 1397 (ships).	Navy Type B NTDS FAST digital data interface (I/O controller)	Not provided (mating connector provided)
RM-9465-61	HP-21MX Series bidirectional PIO/DMA interface.		50
RM-9465-64	Varian 620 and 73 Series bidirectional interface to buffered I/O controller.	Varian (BIOC) buffered I/O controller board (P/N E2832) and priority interrupt module (PIM) Model 620/i-16, and CPU for checkout	15
RM-9465-65A	Data General Nova and Eclipse bidirectional interface	Data General Model 4192 cable in CPU	50
RM-9465-71	IBM 2701 Parallel Data Adapter (PDA) bidirectional interface.		Not provided (special I/F panel provided)

Table 1-4. 9465 Peripherals

Official Description	Common Name	Part Or Model Number
Trackball Cursor Controller	Trackball	GC-104
Lightpen Cursor Controller	Lightpen	GC-105
Joystick Cursor Controller	Joystick	GC-106
Graphic Tablet	Tablet	GC-108
3X Magnification Puck	Puck	GC-PUCK
General Purpose Keyboard	Keyboard	GK-120
Monitor Assembly,CLR,19,P22	Monitor	GM-859-C
Monitor Assembly,CLR,19,P22	Monitor	GM-859-R
Monitor Assembly,CLR,19,LP	Monitor	GM-859-CLP
Monitor Assembly,CLR,19,LP	Monitor	GM-859-RLP
Monitor Assembly,CLR,25,P22	Monitor	GM-865-C
Monitor Assembly,MONO,13,P4	Monitor	GM-873-CP4
Monitor Assembly,MONO,13,P4	Monitor	GM-873-RP4
Monitor Assembly,MONO,19,P4	Monitor	GM-879-CP4
Monitor Assembly,MONO,19,P4	Monitor	GM-879-RP4
Monitor Assembly,MONO,19,P39	Monitor	GM-879-CP39
Monitor Assembly,MONO,19,P39	Monitor	GM-879-RP39

The ac panel assembly holds the main fuse and the power cable assembly. The main fuse protects the 9465 against overloads. The power cable assembly routes ac power to the main fuse and to circuit breaker CB1 on the rear fan assembly.

The ac bracket assembly holds terminal block TB1 and line filter LF1. Line filter LF1 routes ac power from circuit breaker CB1 on the rear fan assembly to TB1. Terminal block TB1 routes ac power to the rear fan assembly fans, the fan plate assembly, and the power supply.

The rear fan assembly holds two rotary fans and circuit breaker CB1. The fans remove hot air from the 9465 cabinet. Circuit breaker CB1 routes ac power from the ac panel assembly to the ac bracket assembly.

The power supply mounts on a hinged power supply mounting bracket which in turn fastens with screws to the frame subassembly.

NOTE

The hinged power supply mounting bracket must remain securely fastened to suppress radio-frequency interference (RFI).

Power supply fuse F1 protects the power supply against overloads. Power supply strapping is factory installed for the customers' specified source

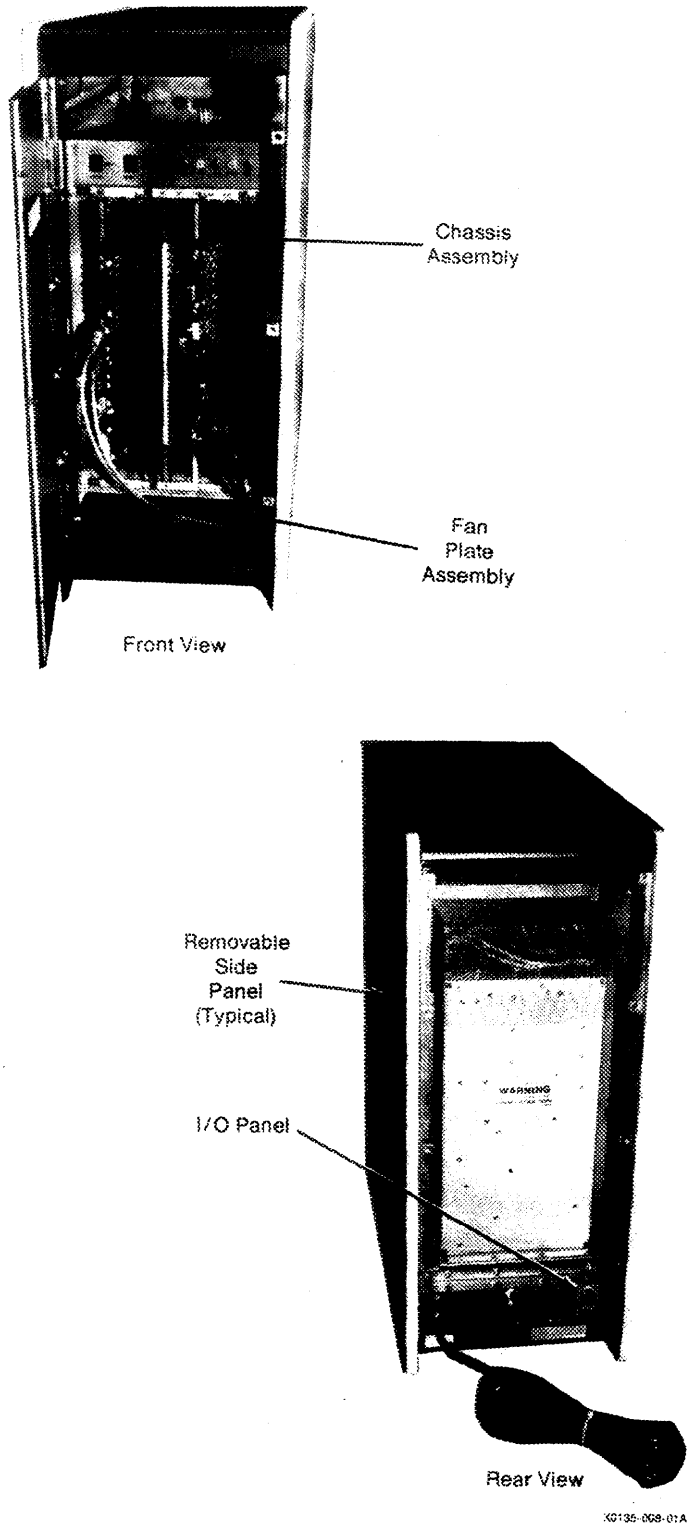


Figure 1-1. 9465

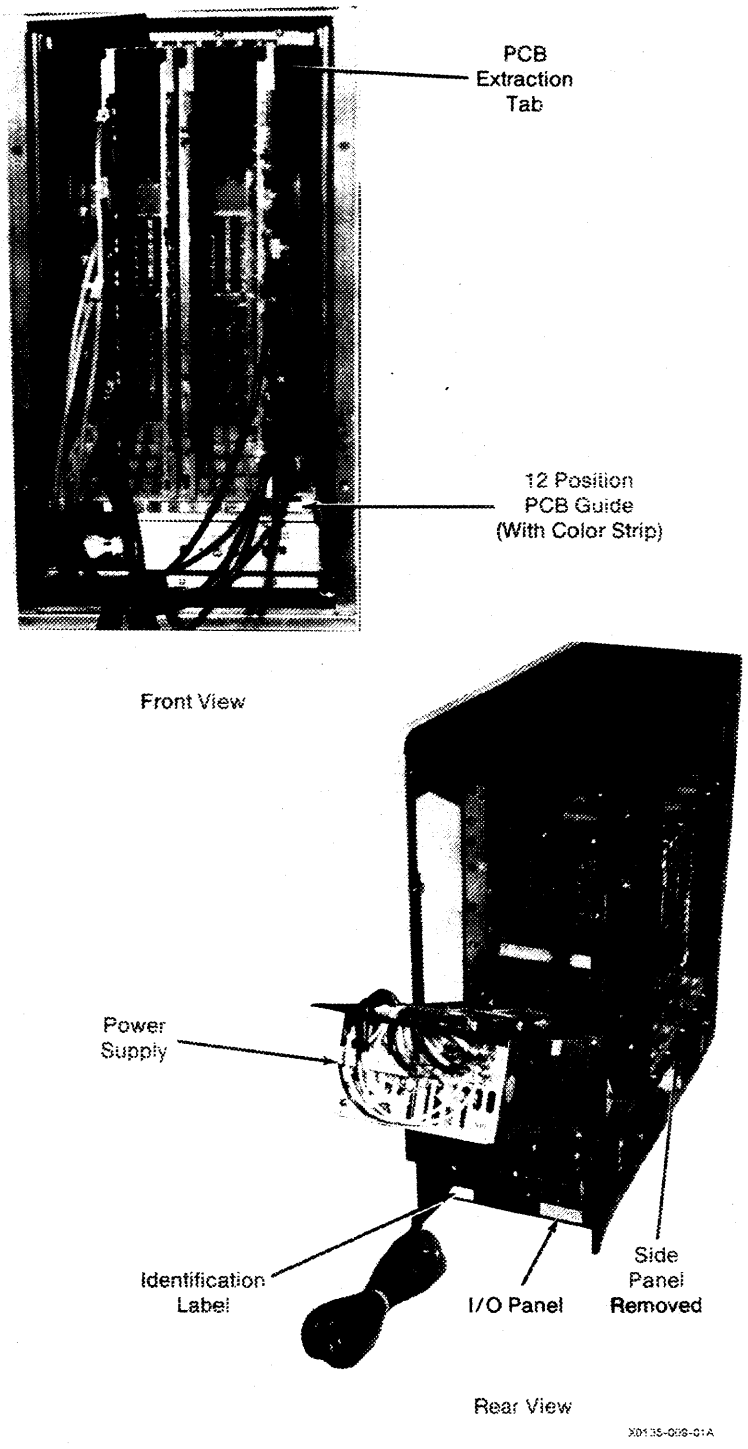


Figure 1-2. Frame Subassembly

voltage. A protective cover (removed for clarity in figure 1-2) fastens to the top of the power supply. Lowering the power supply gives access to the backplane assembly and wiring harnesses.

The control panel holds two controls, five test points, and one indicator. A cable assembly connects the control panel to the backplane assembly.

The backplane assembly is fabricated of 125-mil-thick epoxy glass-laminate, NEMA grade FR-4, with one ounce copper foil. There are six layers of laminate. Each of the 12 backplane assembly positions corresponds to a PCB slot and has two 100-pin connectors. A backplane assembly cover (removed for clarity in figure 1-2) fastens over the top half of the backplane assembly.

1.8.2.b Fan Plate Assembly. The fan plate assembly (figure 1-3) is formed sheet metal that has six rotary fans mounted with screws. Fan operating voltage is routed through 6-position plug P5 that connects at the rear of the frame subassembly. The fan plate is removed from the front. The air intake beneath the fan plate assembly must remain free of obstruction.

1.8.2.c PCBs. The PCBs are alike in size, material, and fabrication technique. Board material is epoxy glass-laminate, 62 mils thick; there are four layers of laminate. One side of a PCB mounts discrete components and integrated circuits. Sockets for the integrated circuits are soldered to the PCB. Discrete components are likewise soldered. Circuit traces are one ounce copper foil. Each PCB has two 100-pin gold-plated contact strips.

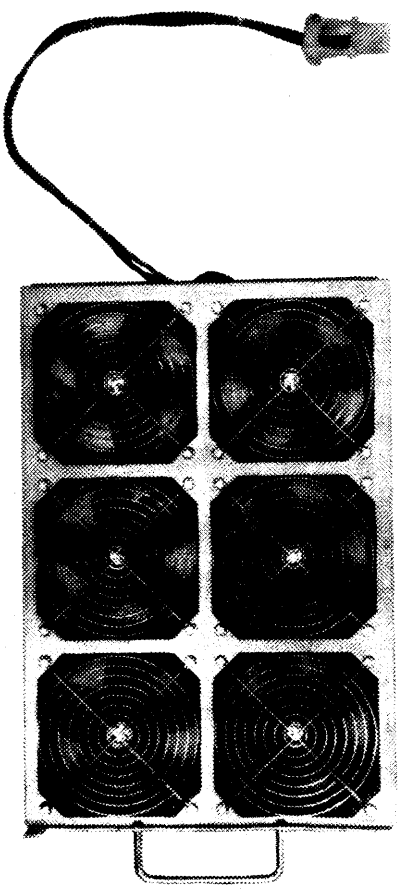
An alphanumeric coordinate grid is etched on the component side of the PCB. Typically, two PCB edges are etched with numerals. These numerals are the row identifiers. Alphabetic characters, aligned perpendicular to the row identifiers, make up the column identifiers. The resulting grid forms the coordinate scheme. Block and logic diagrams refer to component parts by corresponding coordinates; parts lists use the same scheme.

Each PCB has two color-coded PCB extraction tabs. Two adhesive-backed color strips are affixed to 12-position PCB guides on the frame subassembly as an aid during PCB insertion. Color codes are referenced to PCB types in table 1-5.

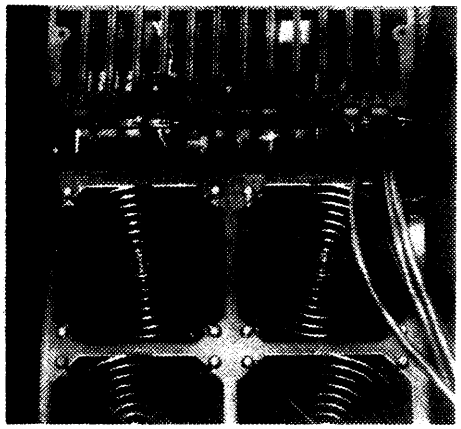
CAUTION

Installing a PCB in the wrong slot can cause severe equipment damage. Refer to chapter 2 for installation instructions.

PCB electrical connectors, light-emitting diode (LED) indicators, test switches and test points are arranged for access from the front of the 9465 cabinet when the PCBs are installed.



Fan Plate Assembly



Connection And Insertion
Into Frame Assembly

X0135-010-01A

Figure 1-3. Fan Plate Assembly

Table 1-5. PCB Color Coding

Color	PCB
Orange	System Processor PCB (Z80 or MC68000)
White	Serial Link, Expansion, Pixel Formatter, or Transform PCB
Green	Sync PCB
Red	MCP PCB
Blue	Memory PCB
Yellow	Video 12, Video 1, Video 7, Video 8, or Transform PCB
Black	Interface PCB (if installed)

Each PCB is marked with a serial number, assembly number and revision level. In some cases, a six-digit option number is affixed to the stiffener. This option number identifies configuration information you may need when contacting Ramtek.

1.8.2.c.1 System processor PCB (Z80). This system processor PCB (figure 1-4) has four jacks (J1-J4), nine LED indicators (LD0-8), and two configuration switches (SW1-2). Functions are as follows:

- J1 - keyboard (not used at present)
- J2 - joystick (not used at present)
- J3 - parallel port or joystick (not used at present)
- J4 - RS232 serial host port (not used at present)
- LD0-7 - system indicators
- LD8 - self test
- SW1 - configuration switch
- SW2 - configuration switch

1.8.2.c.2 System processor PCB (MC68000). This system processor PCB (figure 1-5) has four jacks (J1-4), nine LED indicators (DS1-9), two configuration switches, and five subminiature fuses (F1-5). Functions are as follows:

- J1 - keyboard (not used at present)
- J2 - joystick (not used at present)
- J3 - RS232 serial host port (not used at present)
- J4 - RS232 serial host port (not used at present)
- DS1-8 - system indicators (7-0)
- DS9 - halt
- SW1 - configuration switch
- SW2 - configuration switch

1.8.2.c.3 MCP PCB. The MCP PCB (figure 1-6) has three jacks (J1-3), two LED indicators (DS1-2), and three subminiature fuses (F1-3). Functions are as follows:

- J1 - test
- J2 - test
- J3 - test
- DS1 - self-test
- DS2 - ready

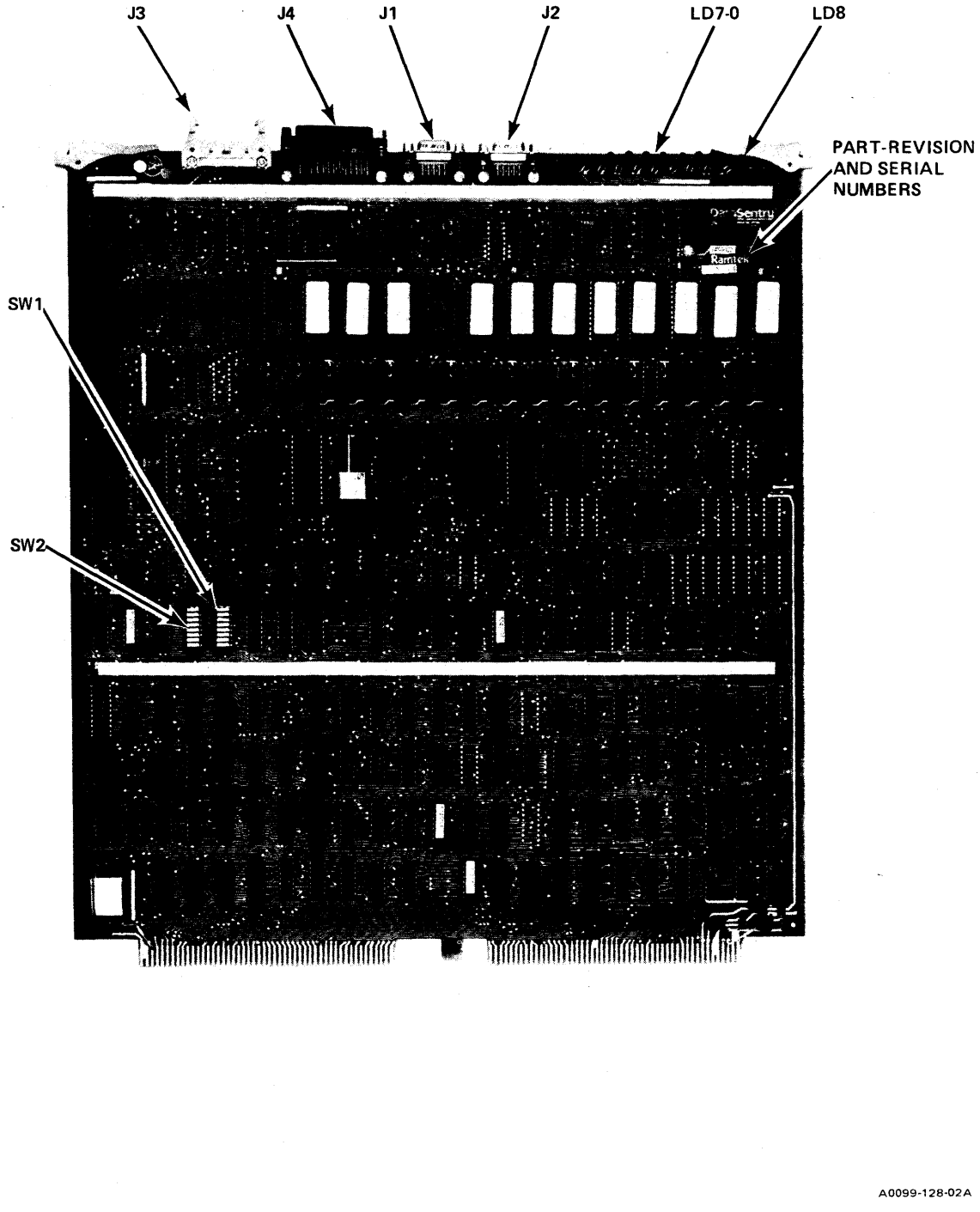


Figure 1-4. System Processor PCB (Z80)

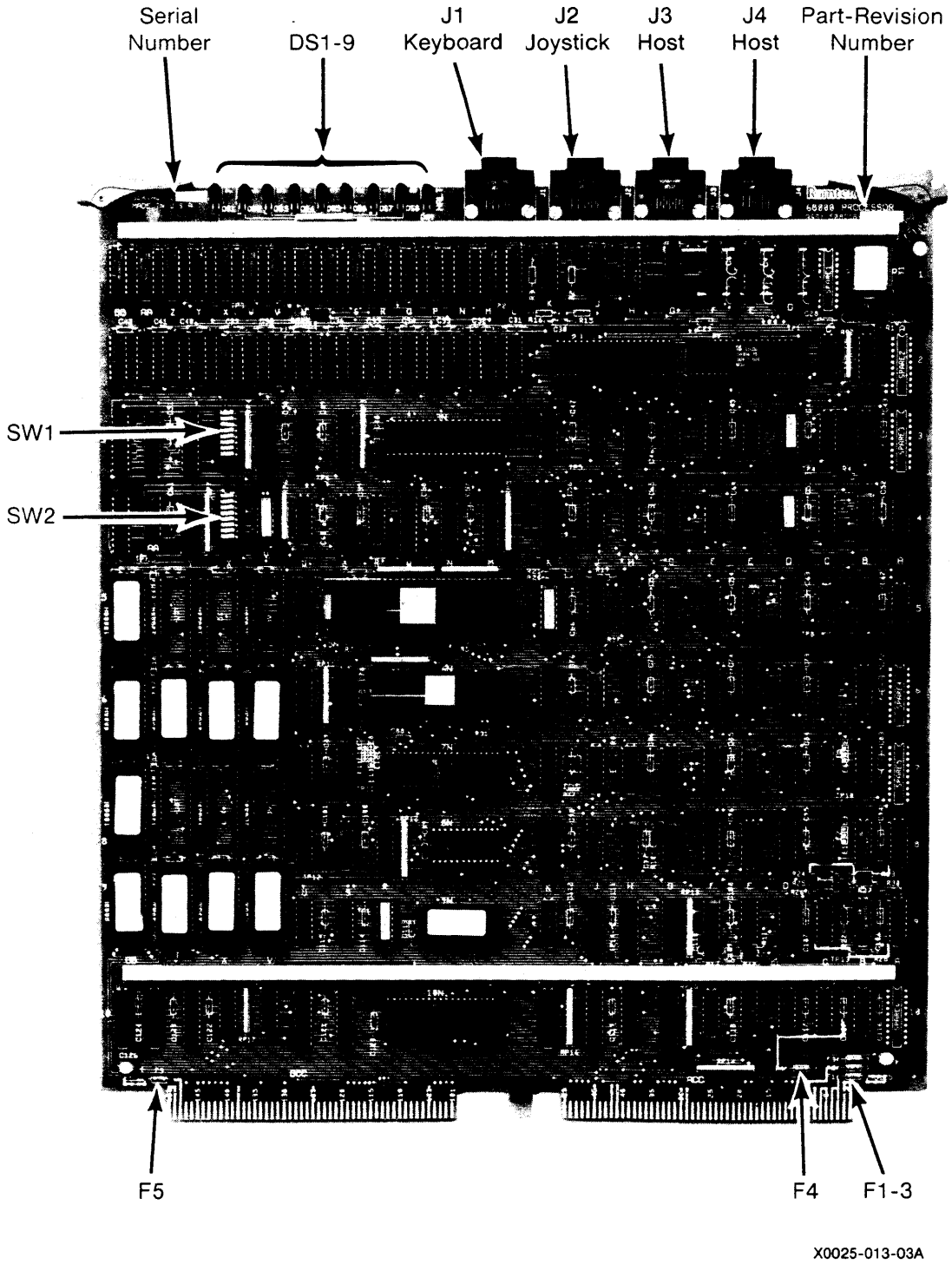


Figure 1-5. System Processor PCB (MC68000)

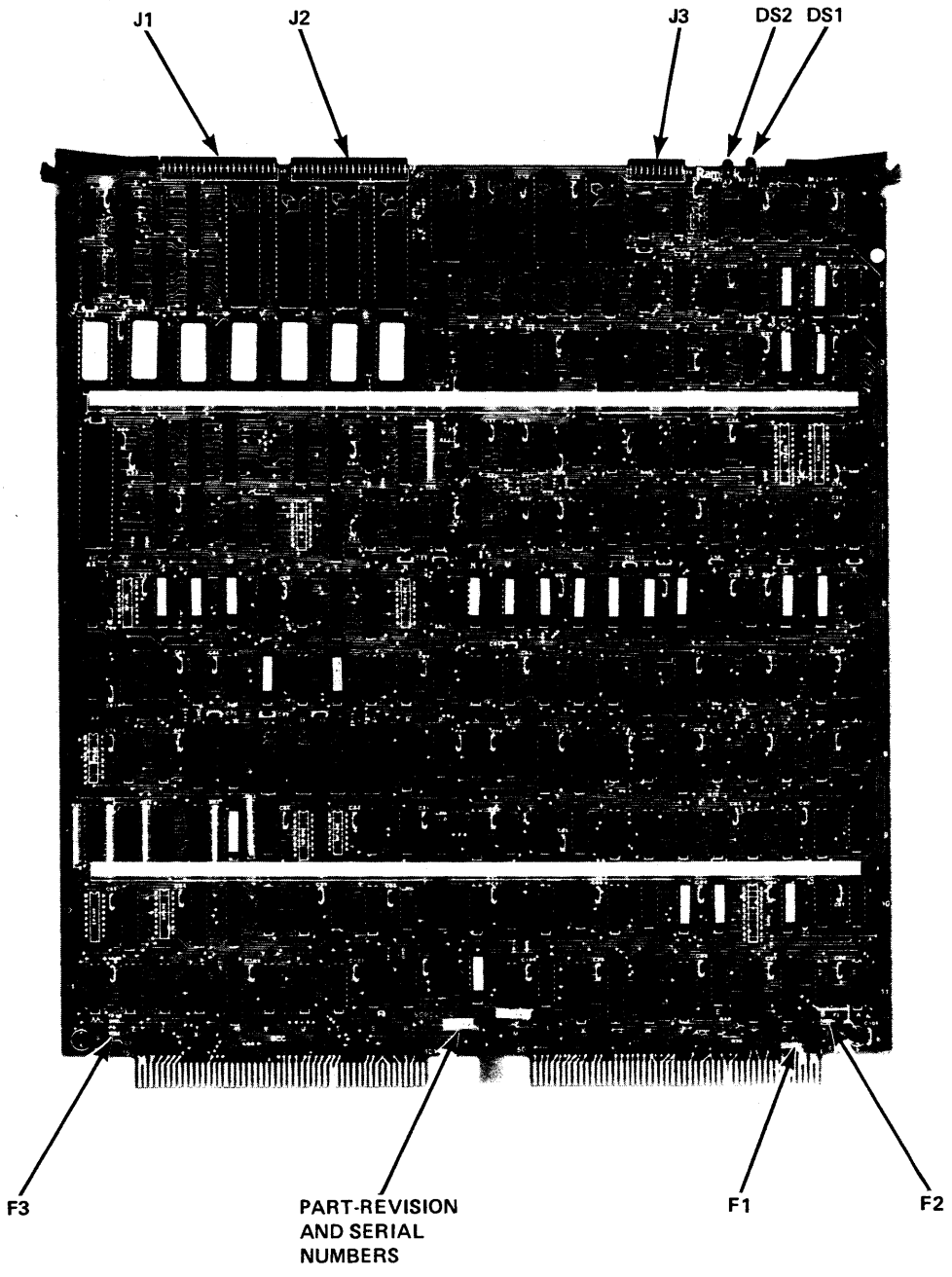


Figure 1-6. MCP PCB

1.8.2.c.4 Memory PCB. The memory PCB (figure 1-7) has three subminiature fuses (F2-4). A metal stiffener fastens to the front edge; other 9465 PCBs lack this device.

1.8.2.c.5 Video 12 PCB. The video 12 PCB (figure 1-8) has five BNC connectors (J1-5), one configuration switch (SW1), and five subminiature fuses (F1-5). Functions are as follows:

- J1 - 8-bit digital-to-analog converter (DAC)
- J2 - text or red
- J3 - text or green
- J4 - text or blue
- J5 - text or hardcopy
- SW1 - blink speed select

This PCB is manufactured in either an A or a B configuration.

1.8.2.c.6 Sync PCB. This PCB (figure 1-9) has 14 test points (TP1-2,TP33, TP3-8,TP 34, and TP9-12), a momentary toggle switch (SW1), and three subminiature fuses (F1, F3, and F5). Functions are as follows:

- TP1 - 7MCQ
- TP2 - 7BQ
- TP33 - ground
- TP3 - THM
- TP4 - TVM
- TP5 - THB
- TP6 - TVB
- TP7 - TCS
- TP8 - TVF
- TP34 - ground
- TP9 - 7EQ
- TP10 - Z80
- TP11 - 7FQ
- TP12 - 7HQ
- SW1 - reset

1.8.2.c.7 Serial link PCB. The serial link PCB (figure 1-10) has eight 9-pin jacks (J1-8), one LED indicator (LD1), five configuration switches (SW1-5), and two subminiature fuses. Functions are as follows:

- J1 - serial port 1 (differential or RS232)
- J2 - serial port 2 (differential or RS232)
- J3 - serial port 3 (differential or RS232)
- J4 - serial port 4 (differential or RS232)
- J5 - serial port 5 (differential or RS232)
- J6 - serial port 6 (differential or RS232)
- J7 - serial port 7 (differential or RS232)
- J8 - serial port 8 (differential or RS232)
- LD1 - self test
- SW1 - keyboard, joystick, graphic tablet, or lightpen select
- SW2 - keyboard, joystick, graphic tablet, or lightpen select
- SW3 - baud rate select (bit 0)

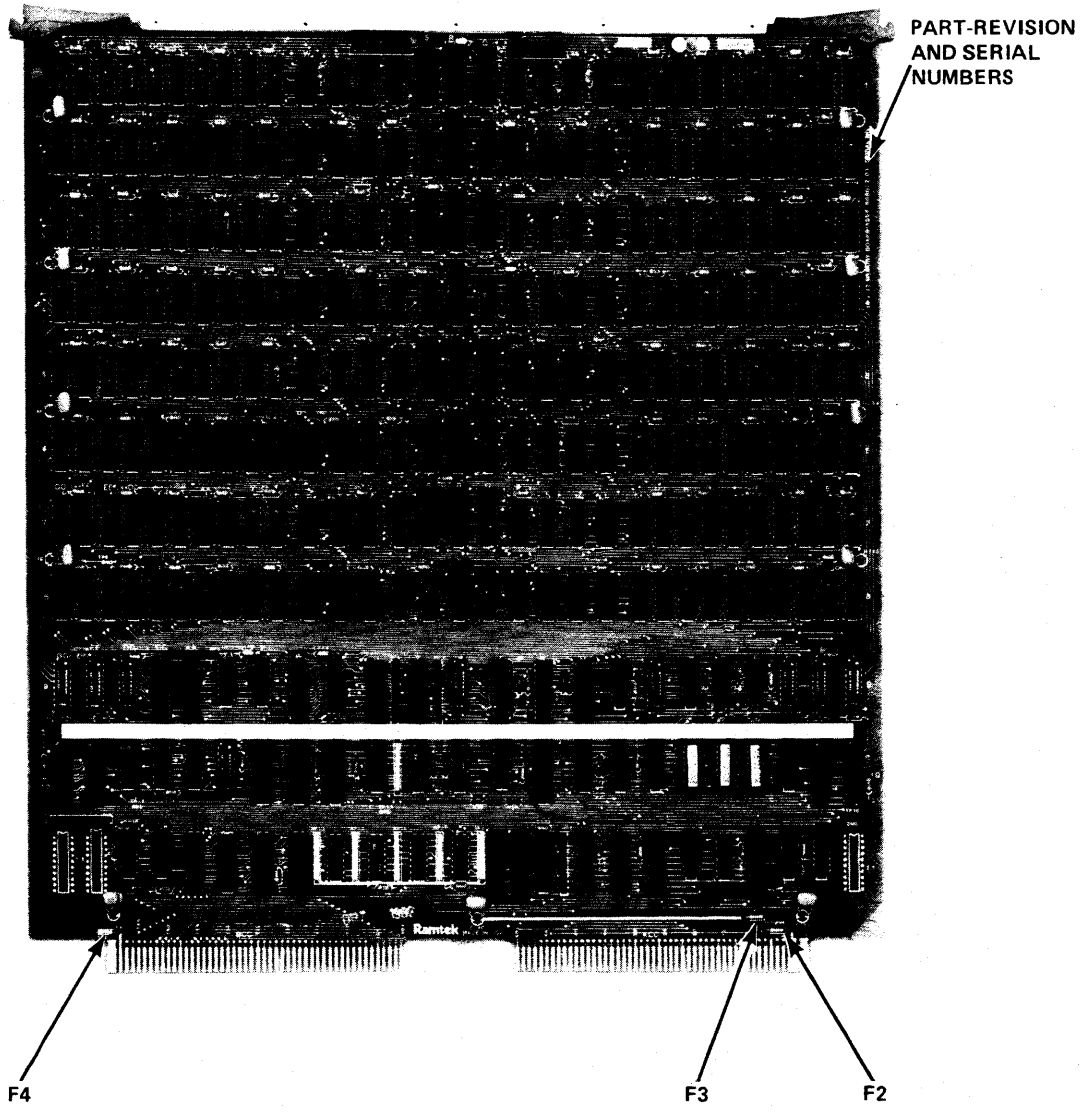


Figure 1-7. Memory PCB

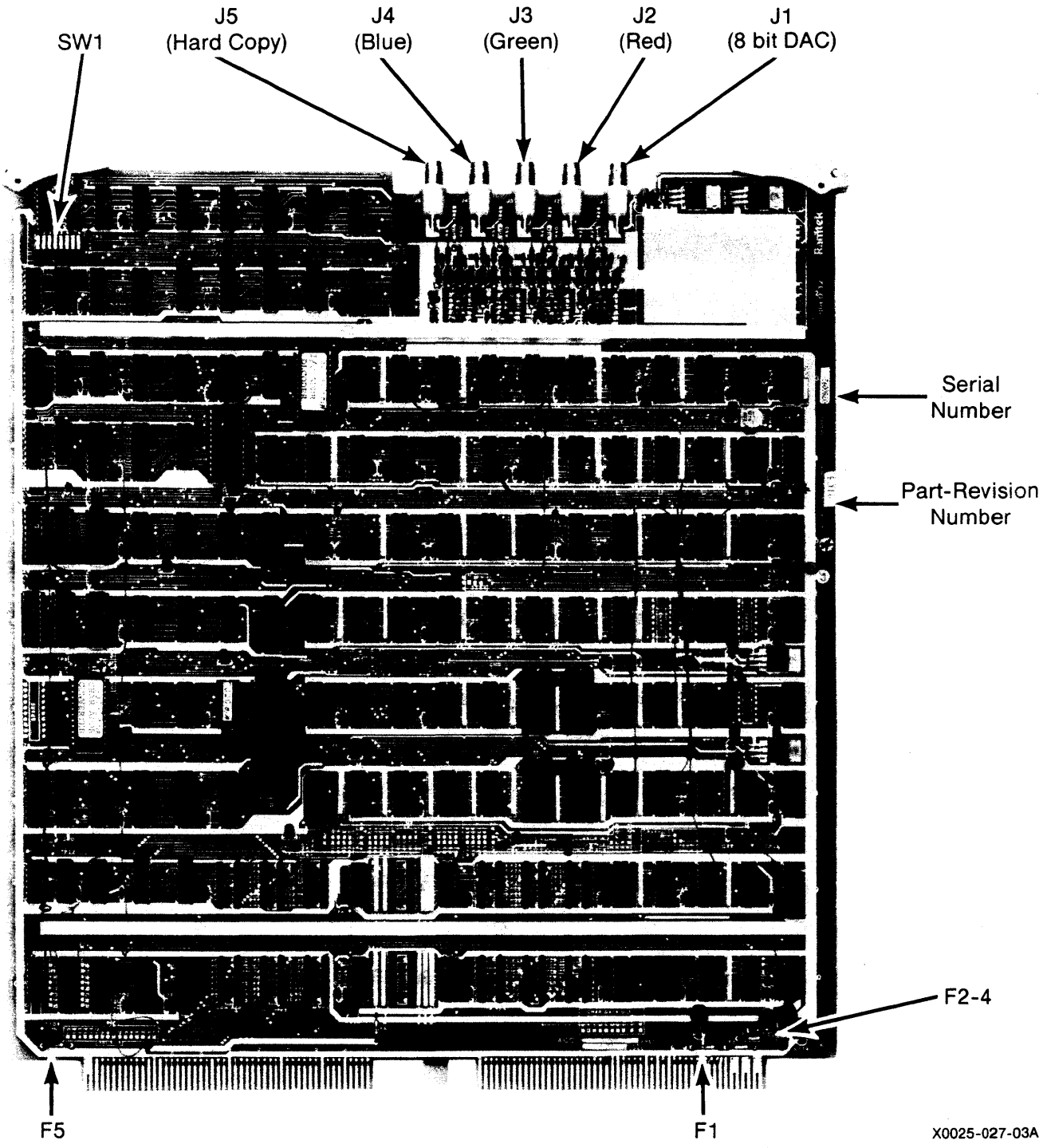


Figure 1-8. Video 12 PCB

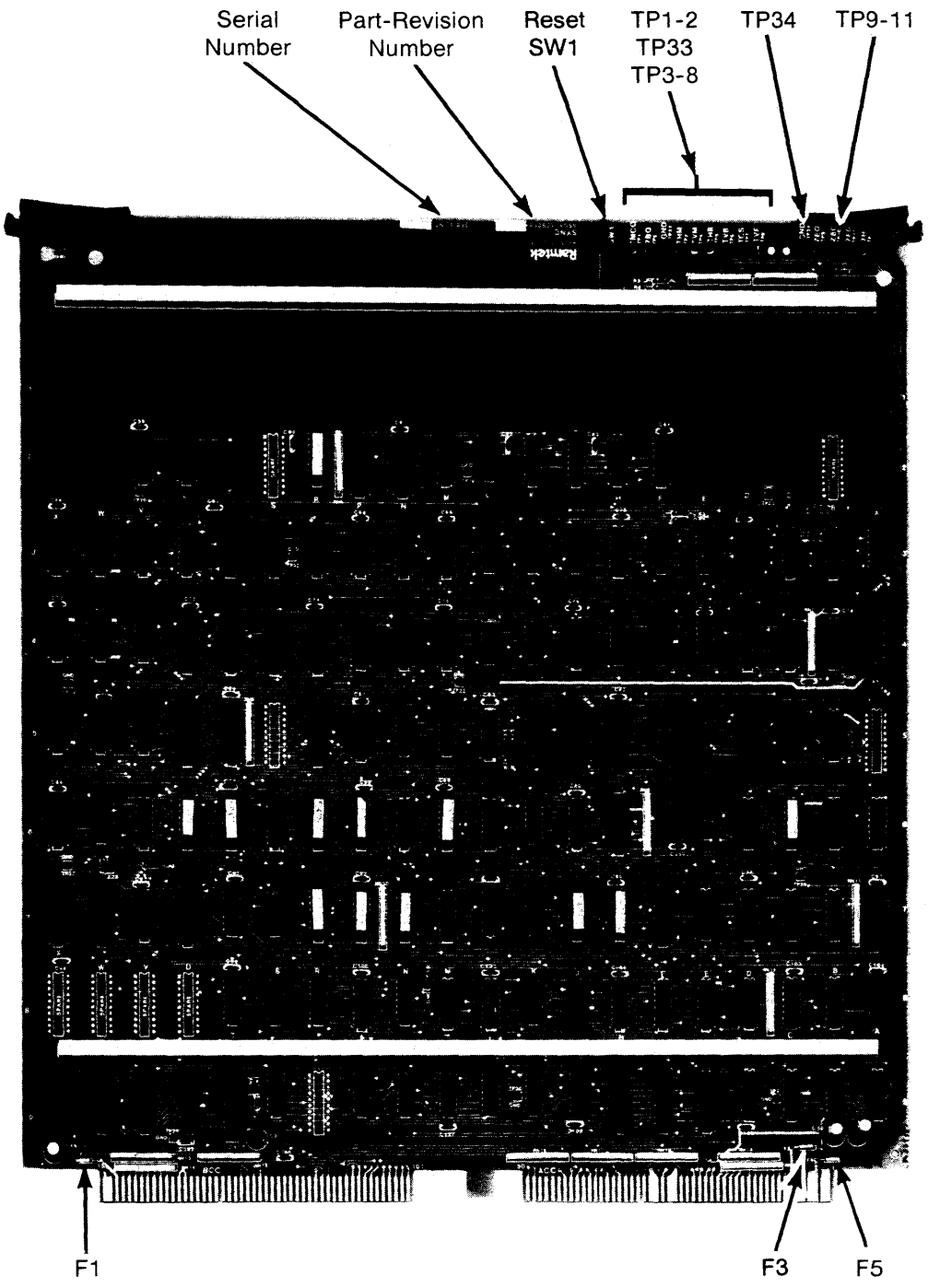


Figure 1-9. Sync PCB

- SW4 - baud rate select (bit 1)
- SW5 - baud rate select (bit 2)

1.8.2.c.8 Expansion PCB. This PCB (figure 1-11) has four jacks (J1-4), and six configuration switches. Functions are as follows:

- J1 - IEEE (not supported)
- J2 - parallel port A or B (not used in 9465)
- J3 - RS232C serial port 1 (not used in 9465)
- J4 - RS232C serial port 2 (not used in 9465)
- SW 6N - RAM ending address
- SW 5P - RAM starting address
- SW 9N - ROM type select and options address range
- SW 10S - ROM starting address
- SW 11P - ROM ending address
- SW 11E - not used

1.8.2.c.9 Video 1 PCB. The video 1 PCB (figure 1-12) has 12 BNC connectors (VOUT0-11) Functions are as follows:

- VOUT0 - video 0
- VOUT1 - video 1
- VOUT2 - video 2
- VOUT3 - video 3
- VOUT4 - video 4
- VOUT5 - video 5
- VOUT6 - video 6
- VOUT7 - video 7
- VOUT8 - video 8
- VOUT9 - video 9
- VOUT10 - video 10
- VOUT11 - video 11

1.8.2.c.10 Video 7 PCB. This PCB (figure 1-13) has eight BNC connectors (J1-8), three LEDs, three DIP switches (SW 11CC, SW 11DD, SW 11P), and five subminiature fuses (F1-5). There are two configurations: A or B. Functions are as follows:

- J1 - red
- J2 - green
- J3 - blue
- J4 - pixel clock
- J5 - composite sync
- J6 - composite blanking
- J7 - vertical drive
- J8 - horizontal drive
- DS1 - +5V
- DS2 - -5V
- DS3 - -12V
- SW 11CC - part of PCB device address select
- SW 11DD - part of PCB device address select
- SW 11P - part of PCB device address select

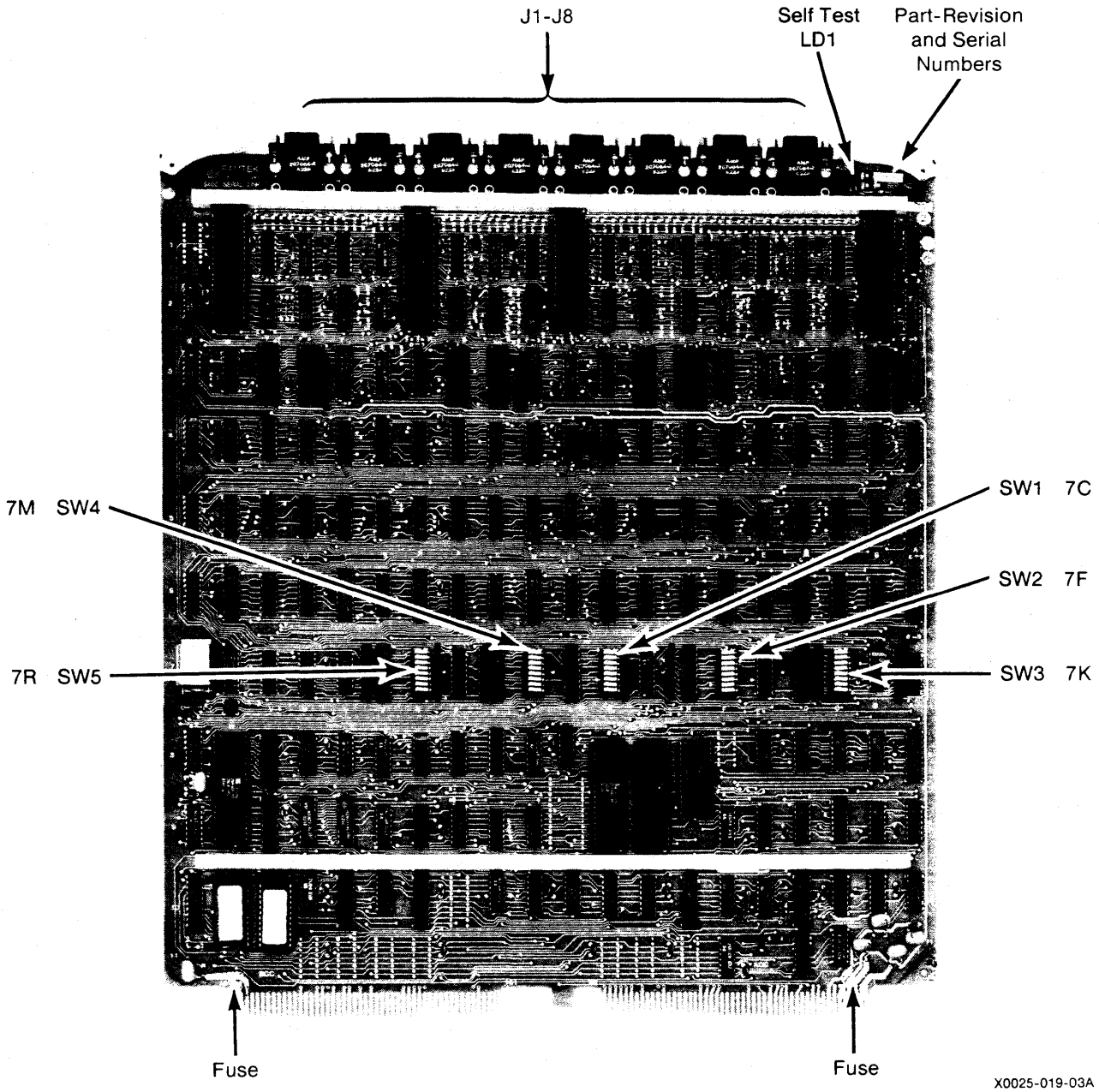


Figure 1-10. Serial Link PCB

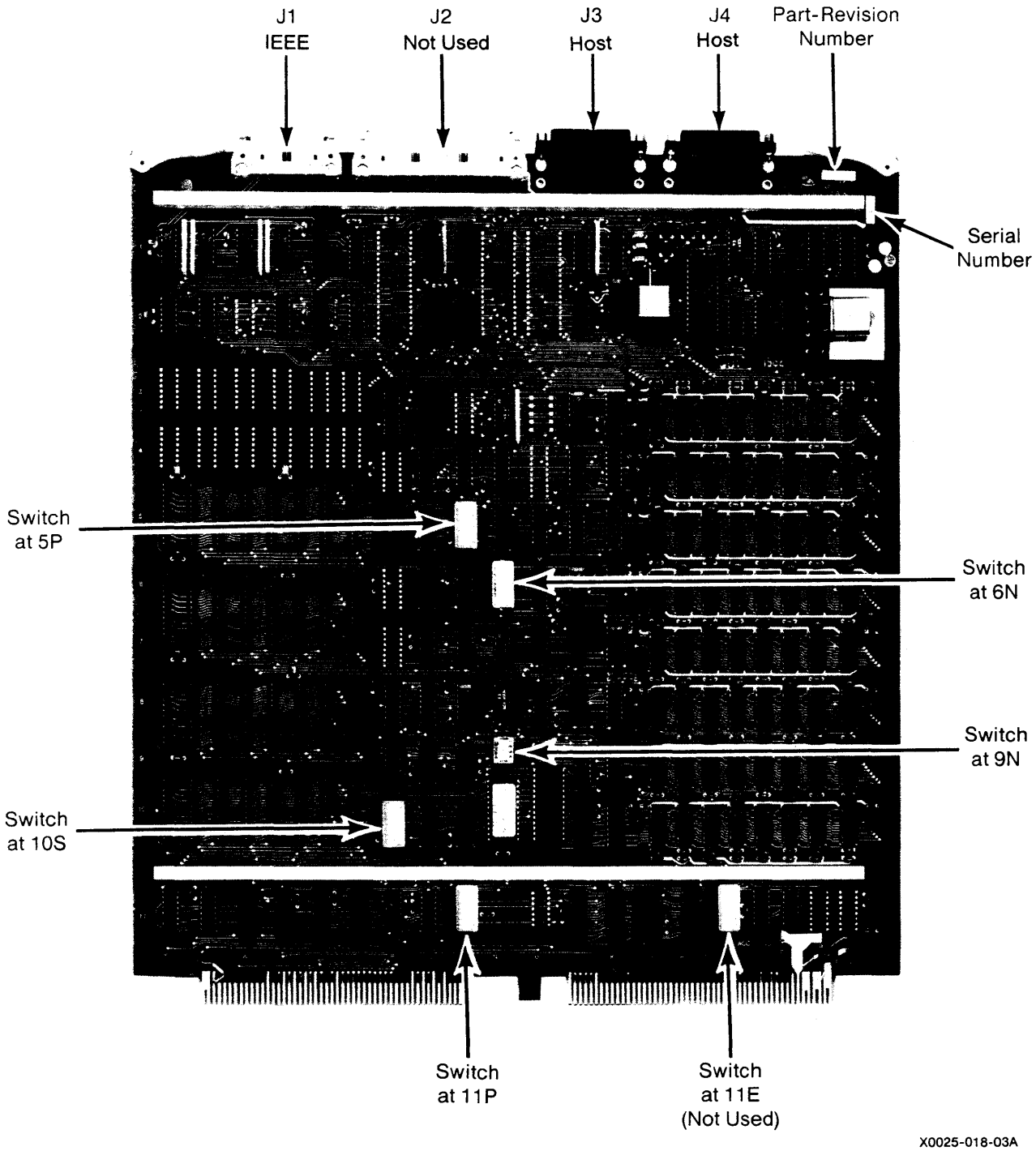


Figure 1-11. Expansion PCB

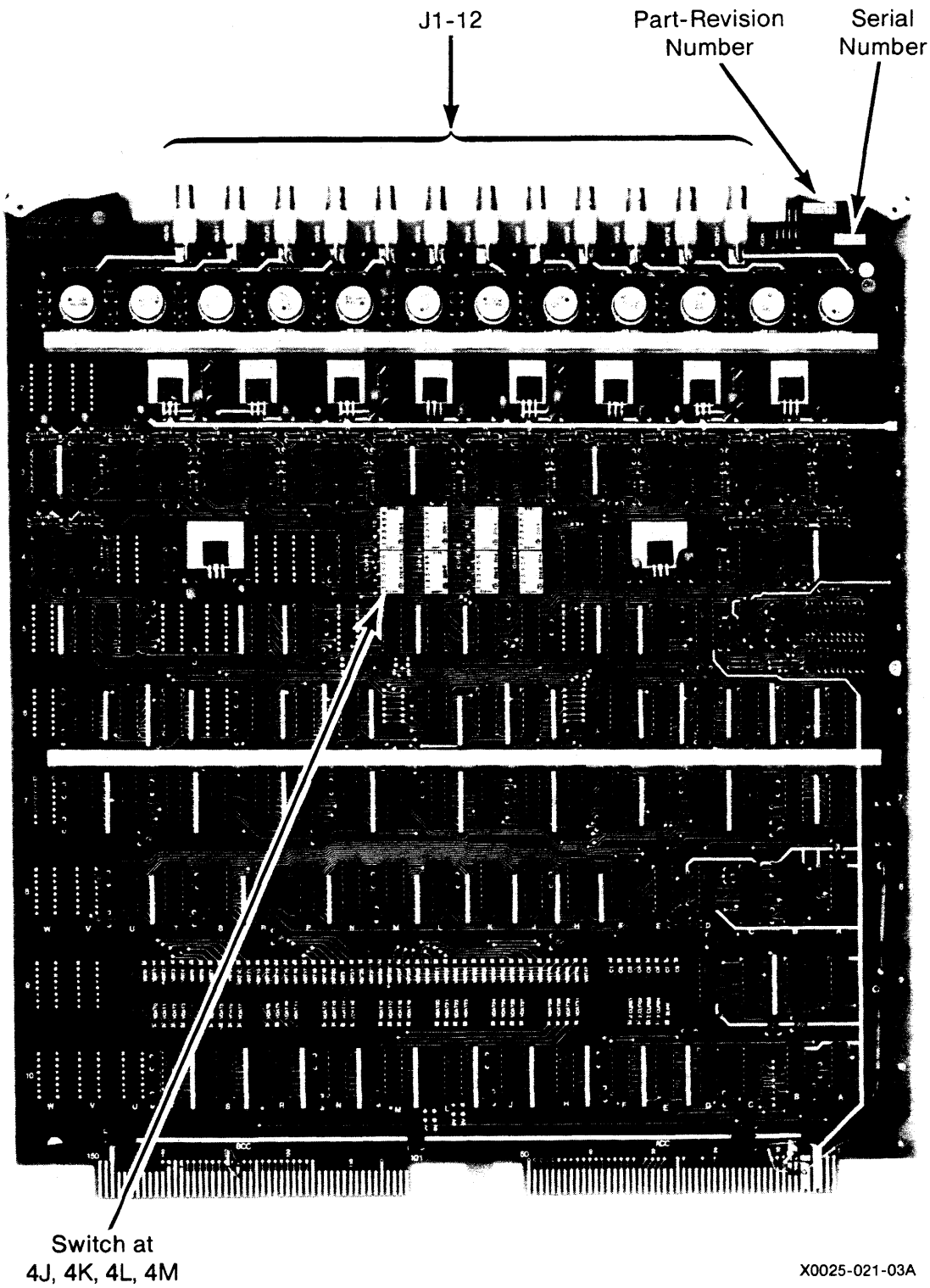


Figure 1-12. Video 1 PCB

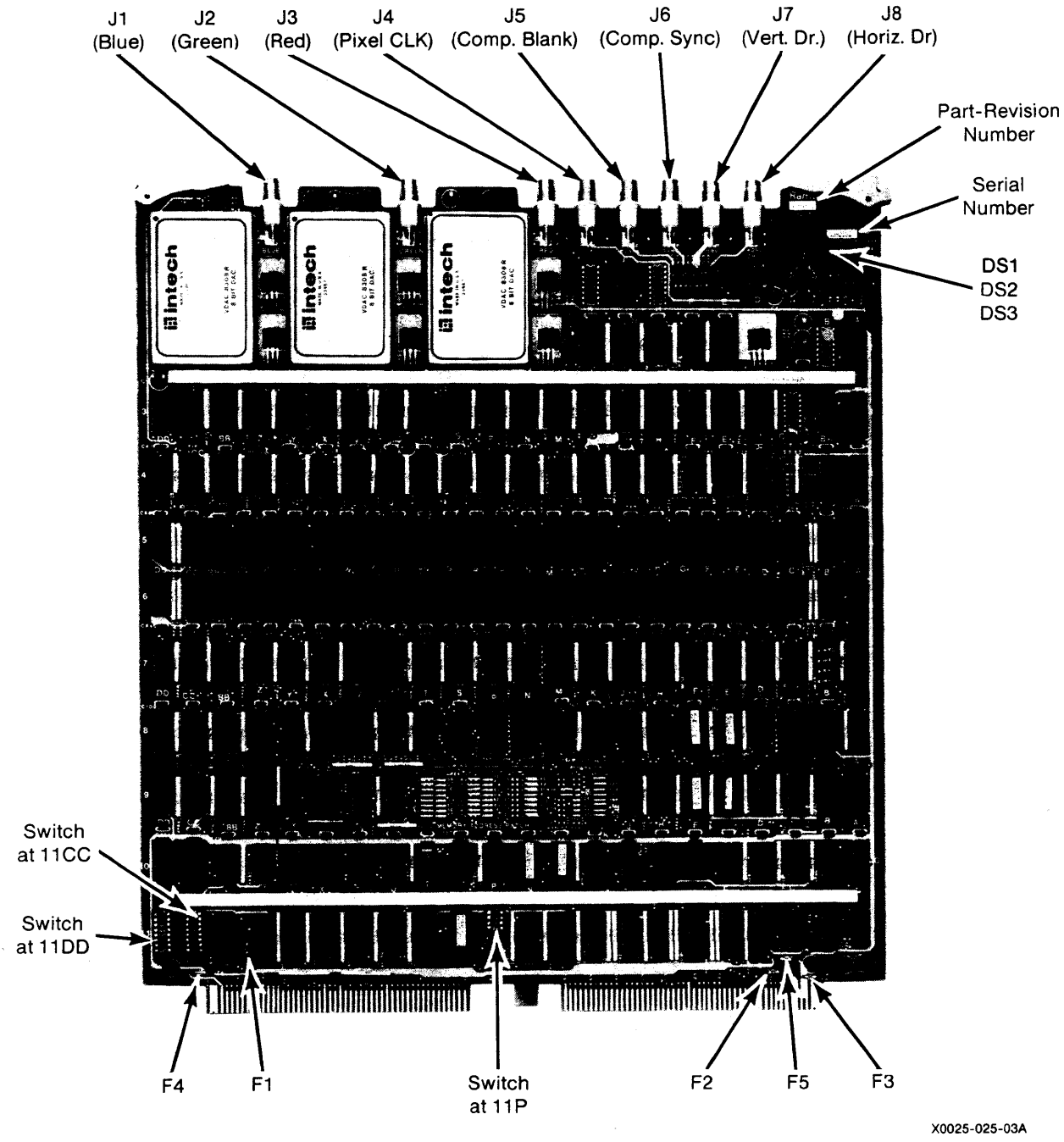


Figure 1-13. Video 7 PCB

1.8.2.c.11 Video 8 PCB. The video 8 PCB (figure 1-14) has 12 jacks (J1-12) and four DIP switches. Functions are as follows:

- J1 - hardcopy display 1
- J2 - blue display 1
- J3 - green display 1
- J4 - red display 1
- J5 - hardcopy display 2
- J6 - blue display 2
- J7 - green display 2
- J8 - red display 2
- J9 - composite sync
- J10 - composite blanking
- J11 - horizontal drive
- J12 - vertical drive
- SW 9S - memory input selection (display 1)
- SW 9H - memory input selection (display 2)
- SW 9B - blink rate and resolution select
- SW 10N - device select

1.8.2.c.12 Video load PCB. The video load PCB (figure 1-15) has 30 resistors. This PCB is only found in 9465 configurations that have a single video 1 PCB installed.

1.8.2.c.13 Pixel formatter PCB. This PCB (figure 1-16) does not have jacks, indicators, switches, or test points. Operating voltage is +5 Vdc and -5 Vdc, unfused on the PCB. No more than one pixel formatter is installed in a 9465.

1.8.2.c.14 Transform PCB. The transform PCB (figure 1-17) has four jacks (J1-4), three switches (SW1, SW2A, and SW2B), three LED indicators (DS1-3), and three subminiature fuses (F1-3). Functions are as follows:

- J1 - test
- J2 - test
- J3 - test
- J4 - transform PCB bus (T-bus)
- SW1 - reset
- SW2A - test address 0-7
- SW2B - test address 8-11
- DS1 - +5V
- DS2 - -5V
- DS3 - idle

1.8.3 Specifications

Electrical, physical, functional, and environmental characteristics of the 9465 configured for domestic installation are specified in table 1-6. Characteristics of peripherals and monitors are documented in separate manuals. Refer to this chapter, "Related Documents."

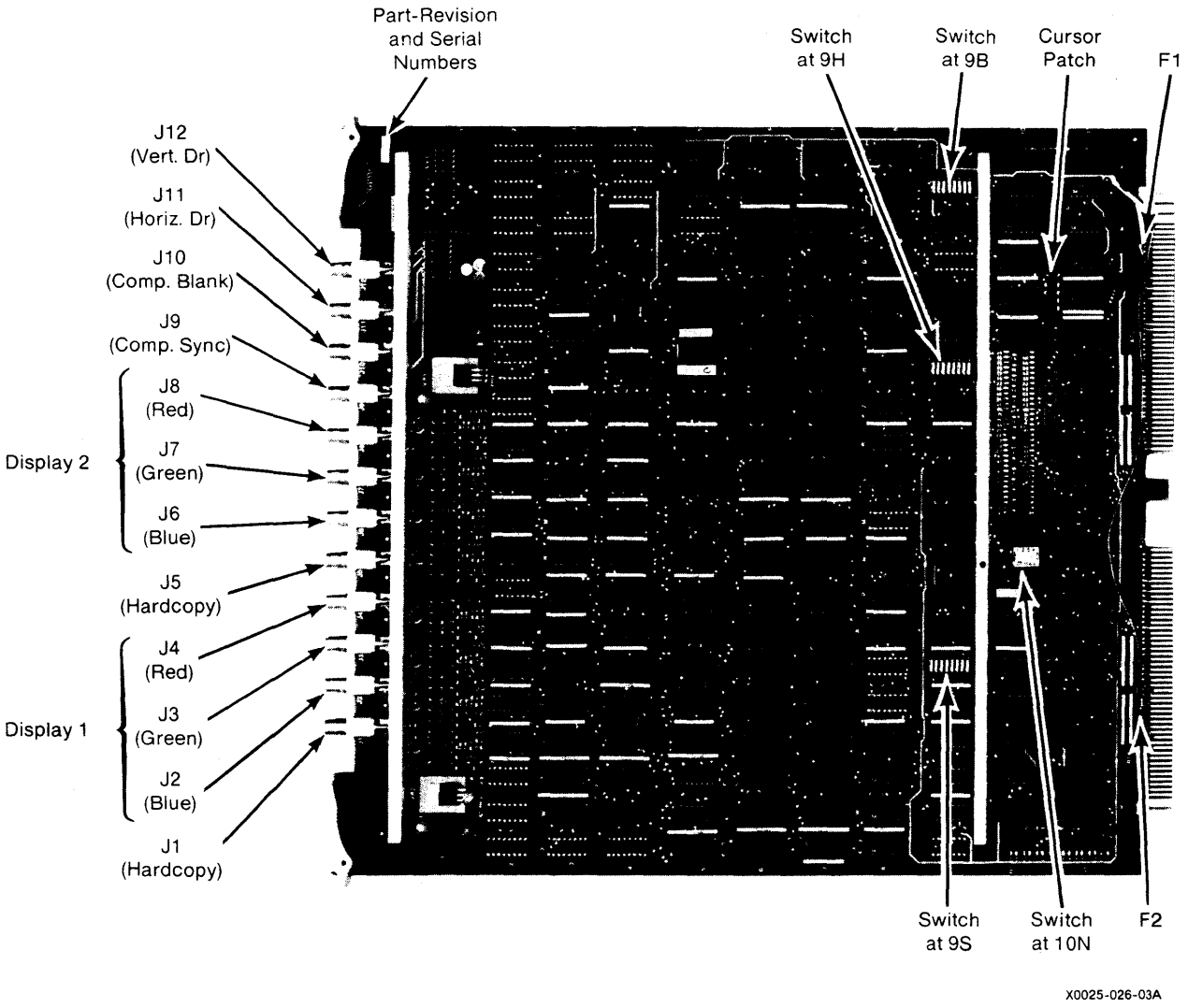


Figure 1-14. Video 8 PCB

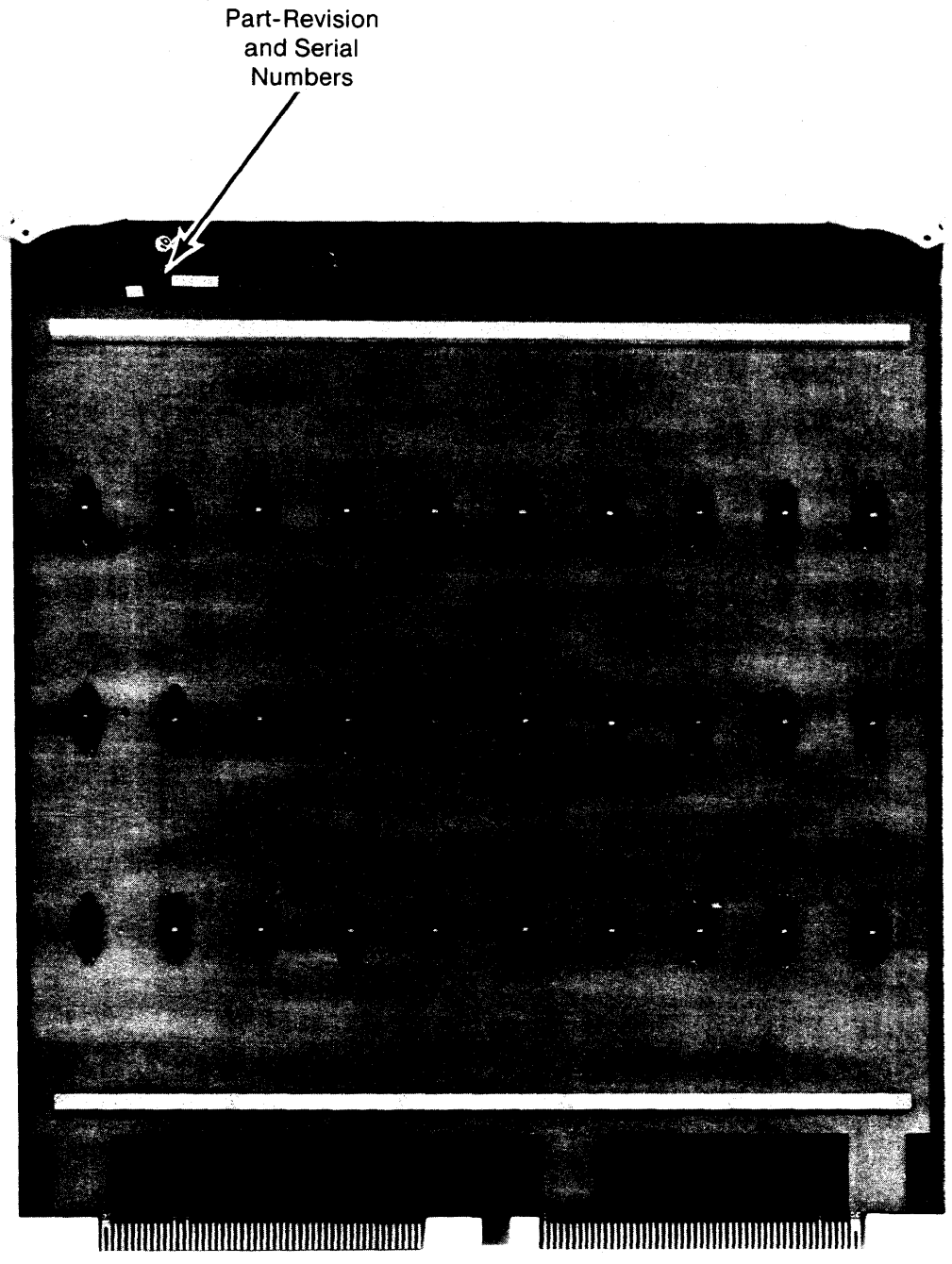
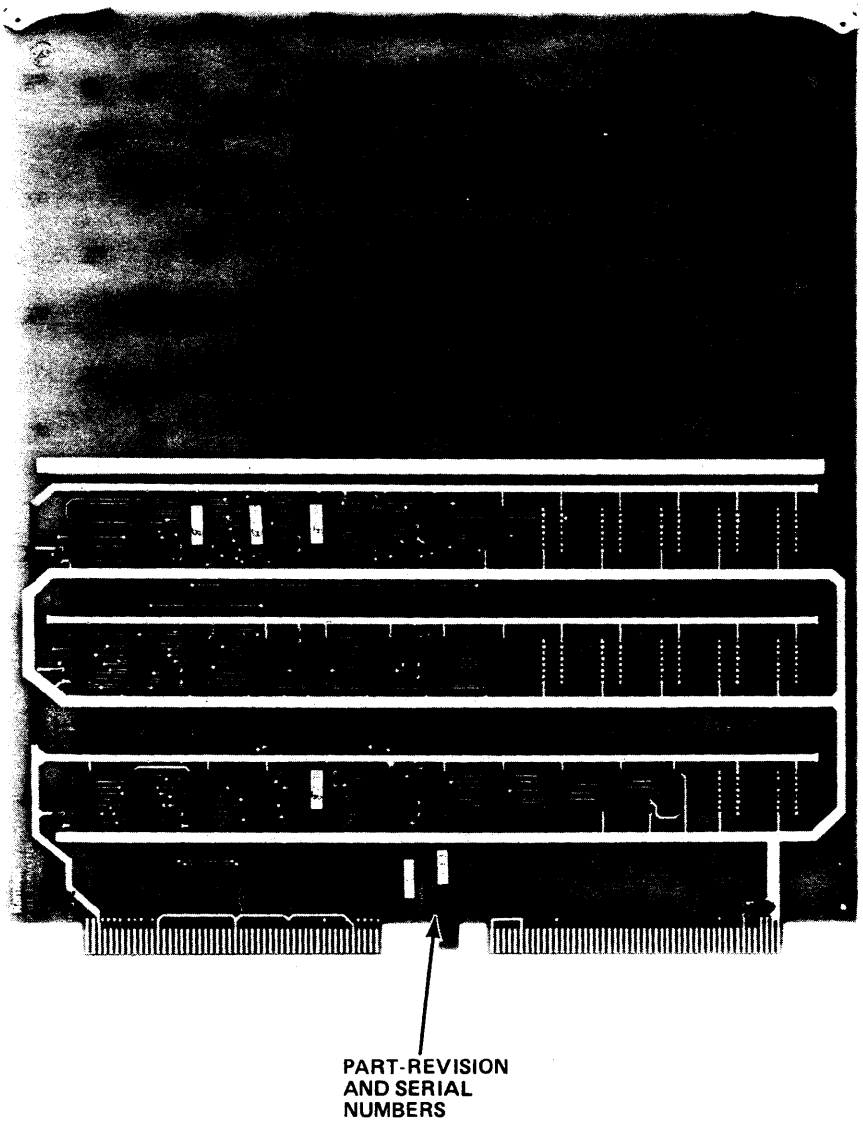


Figure 1-15. Video Load PCB



A0099-140-02A

Figure 1-16. Pixel Formatter PCB

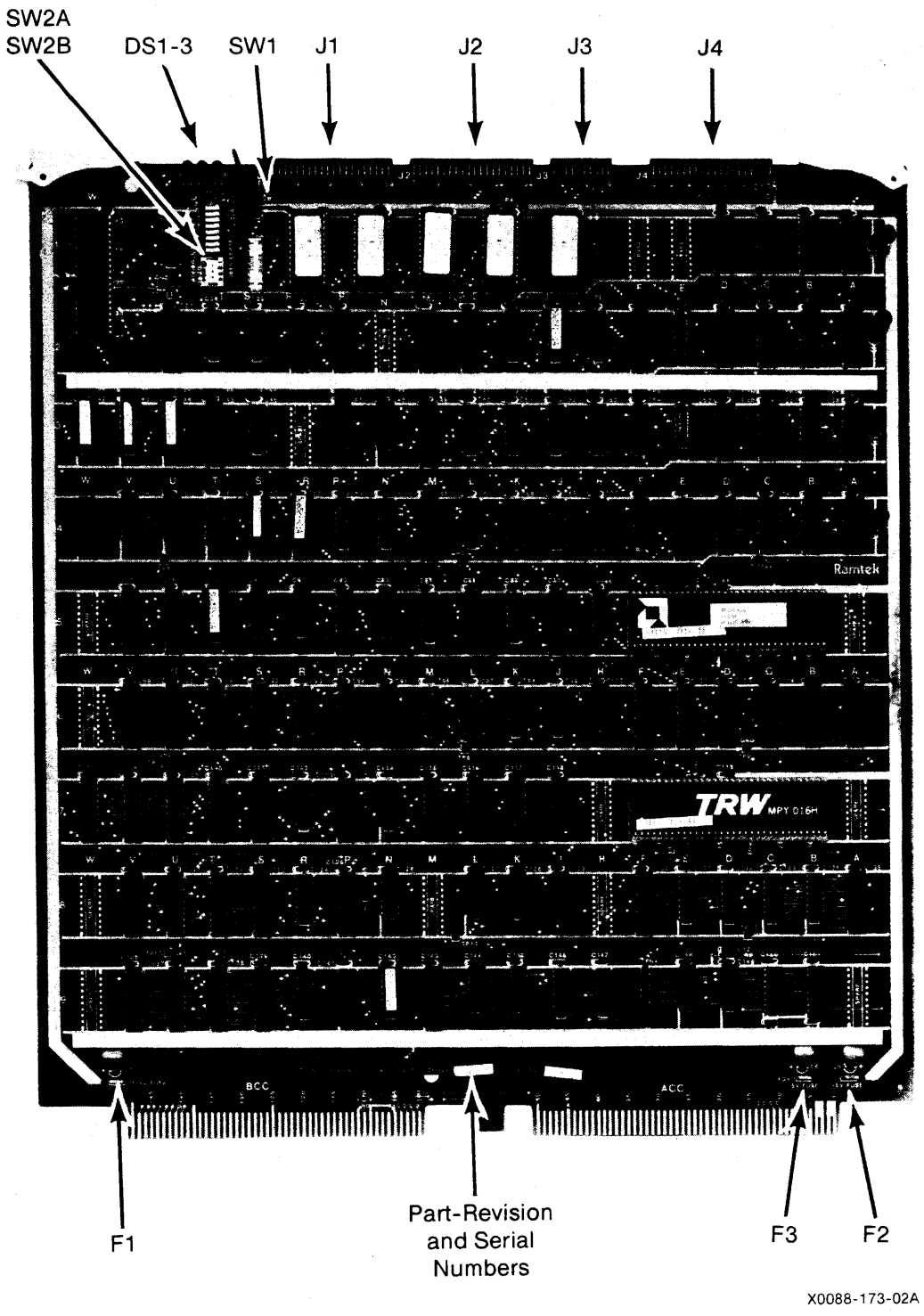


Figure 1-17. Transform PCB

1.9 APPLICATIONS

The 9465 is suitable for graphics or imaging applications. Flexibility afforded by modular design means additional capability is possible by adding selected PCBs. Users who desire information about expanding their 9465s should contact the nearest Ramtek Customer Service office.

1.10 CONFIGURATIONS

Each 9465 manufactured by Ramtek conforms to a Chassis Definition and Acceptance Record which is based upon the sales order. Strapping options are wired in accordance with the 9465 described by this document. Likewise, all configuration switches conform to the configuration ordered.

Table 1-6. Specifications

Description	Specification
Electrical Specifications	
AC service	
Voltage	
120 Vac Models:	108 to 132 Vac
240 Vac Models:	198 to 242 Vac
Current	
120 Vac Models:	TBS Maximum
240 Vac Models:	TBS Maximum
Frequency:	46 to 66 Hertz
Power	
120 Vac Models:	TBS VA
240 Vac Models:	TBS VA
Main Fuse	
120 Vac Models:	10A
240 Vac Models:	5A (two fuses)
Power Supply Fuse:	20A
Interface	
Host port:	16 bit parallel TTL
Peripheral ports:	RS232 or TTL differential
FCC Classification	
Class A Computing Device:	Complies with Subpart J, Part 15 FCC rules
Physical Characteristics	
Dimensions	
Cabinet	
Height:	30 inches
Width:	12 inches
Depth:	30 inches

Table 1-6. Specifications (Continued)

Description	Specification
Physical Characteristics	
Dimensions (Continued)	
PCBs	
Height:	14.44 inches
Width:	16.10 inches
Weight (Fully Configured):	160 pounds
Shipping Weight:	230 pounds
Functional Specifications	
Z80 Processor	
Clock cycle:	3.39 MHz
MC68000 Processor	
Clock cycle:	6.7 MHz
User RAM Space Available	
MC68000 based:	240K bytes maximum
Z80 based:	256K bytes maximum (2 expansion PCBs installed)
Environmental	
Ambient Temperature	
Operating:	0 to 40° Centigrade
Humidity	
Relative:	10 to 95% noncondensing

Chapter 2

INSTALLATION

2.1 INTRODUCTION

This chapter contains receiving and reshipping instructions, installation requirements, installation procedures, 9465 configuration setup instructions, and checkout instructions.

2.2 RECEIVING AND RESHIPPING

The following paragraphs describe how to inspect, unpack, and assemble the 9465. Reshipping procedures are also given. Receiving and reshipping procedures for peripherals and monitors are covered in separate manuals. Refer to section titled "Related Documents" in chapter 1.

2.2.1 Receiving Procedures

The 9465 is carefully inspected and packed prior to shipment from the manufacturing facility. Unpack the 9465 as follows:

1. Examine shipping cartons for external damage. If a carton is damaged, notify shipping agent. Unpack carton while agent is present.

2. Carefully unseal cartons; remove equipment and packing material. Save for possible future use.

3. Inspect equipment for scratches, dents, or chipped paint, especially in places where shipping carton may have been punctured.

4. Check that all items on packing list have been received.

5. Check major component assemblies to determine if any assemblies or screws were loosened by vibration.

6. Inspect input receptacles for foreign material that may impair electrical contact when cable connections are made. If required, remove dust using soft brush and vacuum cleaner.

7. Tighten any loose screws or mounting hardware as required.

2.2.2 Reshipping Procedures

Call Ramtek Field Engineering, (408) 988-2211, if you need to ship the 9465 to a Ramtek repair depot because of shipping damage, or for any other reason. You must obtain prior approval from Ramtek Field Engineering before returning equipment to the depot. Attach a tag to the equipment that identifies the owner and the requested service or repair. Include the model number and the

full serial number on the tag. Always identify the equipment by model and serial number in any correspondence with Ramtek. If you retained the original packing material, repack the 9465 as follows:

1. Disconnect all external cables and place in a strong shipping carton, protecting connectors with padding or cardboard.

2. Disconnect signal cables from PCBs; remove PCBs from chassis assembly. Wrap individually in anti-static bags.

3. Place the PCBs in the original shipping carton as originally packed.

4. Place cabinet in shipping carton as originally packed.

5. Seal shipping cartons with strong tape or metal bands.

If the original shipping carton is not available, proceed as follows:

1. Wrap the PCBs in an anti-static bag; place in an inner shipping carton using padding on all sides of each PCB.

2. Seal inner shipping carton.

3. Select an outer shipping carton approximately 4 inches larger in all dimensions; place packing material ("pop corn" or "flo pac") on the bottom.

4. Place inner shipping carton in the outer shipping carton.

5. Put packing material ("pop corn" or "flo pac") around all sides and the top.

6. Wrap the cabinet in protective padding and place in a strong shipping carton or wooden crate.

7. Mark the shipping cartons "DELICATE INSTRUMENT, FRAGILE."

8. Seal cartons with strong tape or metal bands.

2.3 FACILITIES REQUIREMENTS

Planning for and installing the 9465 requires a systematic evaluation of your site plan and supporting facilities. The information provided here is for guidance only and applies to domestic installations. Consult local building and electric codes for your specific area.

2.3.1 Space Requirements

The 9465 cabinet has a footprint of 2.5 square feet. Additional floor space is required for opening front and rear access panels and passage of personnel and equipment. Assuming both access panels are fully extended, a minimum space 52 by 12 inches is required. Allowing on all sides of the cabinet for movement of equipment and personnel brings the space requirement to 84 by 124 inches.

This means the cabinet would be spaced a minimum of 47 inches, front and back, from the nearest walls or other solid objects. The access panels swing out 11 inches.

2.3.1.a Cable Space Requirements. Cable space requirements are dependent upon the physical layout of the facility. You should analyze the planned 9465 location in relation to the host computer, monitor, and interactive devices, and then determine that raceways, cable troughs, or other cabling routes can support the planned cable installation. Partition, wall, subfloor, or rack openings must accommodate not only the cable cross section area but connectors as well.

2.3.1.b Shipping Carton Storage Space Requirement. The 9465 shipping carton is 38 inches high, 38 inches deep, and 21 inches wide. This translates to 17.5 cubic feet and a footprint of 15.5 square feet.

2.3.2 Floor Considerations

Surface loading, floor types, and seismic anchor requirements are three things to consider when planning installation.

2.3.3 Surface Loading

Surface loading is the total weight divided by the area of space occupied; that is, the distributed load which could collapse the floor if exceeded. Use table 2-1 to calculate total floor surface area and loading.

Size and weight information for peripherals and monitors are given in separate manuals. Refer to chapter 1, "Related Documents."

Table 2-1. Space and Weight Worksheet

Number of 9465s	Footprint Per Unit	Total Space	Weight Per Unit	Total Weight
_____	2.5 sq. ft.	_____	170 lbs.	_____lbs.

Most office floors are rated at 50 pounds per square foot (347 pounds per square inch) with an additional 20 pounds for partitions. This load rating is more than adequate for the 9465; but you must consider all equipment in the room.

2.3.3.a Floor Types. Standard floors, raised floors, and floors with subfloors are all adequate for the 9465. Raised floors are advantageous during cable installation.

2.3.3.b Floor Surfaces. The floor surface may be concrete, tile, or other material, but concrete requires treatment to prevent excessive dust accumulation. In addition, concrete requires insulation with material rated for a breakdown voltage greater than 400 volts.

WARNING

Concrete floors-on-grade (concrete laid directly on the ground) are classified as "wet locations" by the National Electric Code (NEC) and have unique grounding requirements. Consult your local building code office before installing the 9465 on such a surface.

Raised tile floors are usually constructed of plywood faced with tile adequate for floor insulation. If you install tile on a concrete surface, the tile breakdown voltage must exceed 400 volts.

Because carpeting can produce electrostatic charges capable of damaging electronic components, Ramtek does not recommend carpeting. For installations that require carpet, use specially-manufactured carpeting that has a rubber backing with a network of metal filaments between the backing and the nap. Insure the metal filaments are grounded, but do not connect this carpet ground to the 9465 ground.

CAUTION

Insure the 9465 cabinet and interconnected equipment are insulated from the metal filaments in carpeted installations.

2.3.4 Earthquake Considerations

In certain locations, seismic anchors are required (or recommended) to prevent equipment movement. Obtain seismic anchor requirements from local building code authorities.

2.3.5 AC Service

Prior to 9465 installation, you should conduct a study of ac line voltage and determine if any line-transient or abnormal voltage conditions exist. Monitor the line voltage for at least one week using a power monitor which will record all fluctuations. Primary voltage variations in excess of ±10% will preclude normal operation of the 9465. In such cases, Ramtek recommends you use an ac

line regulating transformer. Contact your Ramtek representative for the transformer recommended in your area and follow the installation instructions provided by the transformer manufacturer.

2.3.6 Grounding Considerations

The 9465 is grounded through the power cable connector. You must have a good-single point ground to provide sufficient noise immunity for normal operation and reliability. If the power cable receptacle does not provide a suitable ground, see the following information.

2.3.6.a Single-Point Grounding Electrode. Select a good earth ground for a grounding electrode. For example, use a cold water pipe, leach field, or copper rod, as specified by the National Electrical Code. If you use a water-pipe ground, ensure that expansion joint and water meter bonding straps are installed. You must verify the grounding conductor is insulated and isolated from any other incidental ground points. Properly dress this conductor; and keep the length as short as possible. Ensure all ground connections are tight, bare, metal-to-metal contacts.

2.3.6.b Grounding Wire Size. Ramtek recommends number 8 gauge copper grounding wire. If you select aluminum wire, then install number 6 gauge.

2.3.6.c Carpet Ground. Metal filaments in specially carpeted installations are brought out to an isolated ground. In this way, damage from static discharge is minimized.

CAUTION

Ensure the 9465 ground and the carpet ground are isolated.

2.4 INSTALLATION PROCEDURES

Installation procedures consist of PCB installation, signal connection, and power connection. Peripheral installation is provided in related manuals. Refer to chapter 1, "Related Documents," for peripheral manuals that describe installation procedures.

Host software installation can vary with equipment application. Consult applicable software documentation for your particular installation.

2.4.1 PCB Installation

Install PCBs as follows:

CAUTION

Installing a PCB in the wrong slot can cause severe equipment damage. Observe color markings.

Do not place PCBs on a conducting surface. Static discharge can cause permanent damage. Store and move PCBs enclosed in an anti-static bag.

1. Check that circuit breaker CB1 is off.
2. Open front access panel of cabinet using hex-wrench supplied.
3. Inspect card guide slots and backplane assembly connectors for dirt, packaging debris, or other contamination. Clean as necessary, using a soft brush and vacuum cleaner.
4. The component side of each PCB is on the left when facing the card guides. Color codes are referenced to PCB types in chapter 1. Remove PCBs from anti-static bags and loosely insert into card guides, matching PCB extraction tab color codes to color codes affixed to upper card guide.
5. With thumbs against PCB extraction tabs (in folded position), apply firm pressure until each PCB mates with backplane assembly connectors. Verify all PCBs are fully seated into backplane assembly.

2.4.2 Signal Connection

The Chassis Definition and Acceptance Record lists jack assignments for interactive devices connected to the I/O panel, and for other cabling. For this discussion, a representative configuration was chosen; cable assignments herein may not agree with the cable assignments on your Chassis Definition and Acceptance Record. A representative installation (figure 2-1) has the following signal cable connections:

- Host computer cable
- Keyboard cable
- Graphics tablet cable
- Joystick cable
- Trackball cable
- Lightpen
- Blue video
- Green video
- Red video

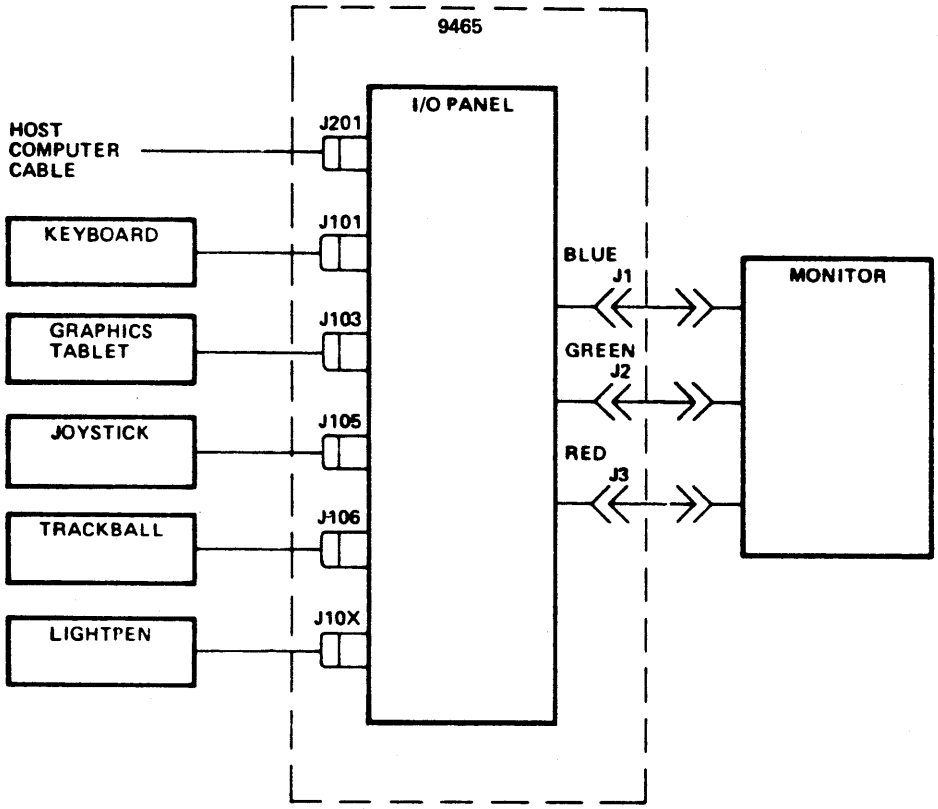


Figure 2-1. Representative Installation Signal Connections

NOTE

To minimize radio-frequency interference, you must tighten the screws holding peripheral cable plugs to the I/O panel. Ensure all BNC connectors are securely seated. These measures will ensure good cable grounding.

Install signal cables as follows:

1. Route host computer cable from host computer through bottom of cabinet to the I/O panel assembly. Plug connector into J201 and tighten connector fastener.

2. Route interactive device cables through bottom of cabinet to the I/O panel assembly. Tighten two screws on each connector.

3. Route three video cables from monitor through bottom of cabinet to the I/O panel assembly. Connect BNC connectors as illustrated.

2.4.3 Power Connection

At the ac mains circuit breaker box, verify ac voltage is 87 to 128 volts root-mean-square (VRMS) (for 120 Vac models) or is 177 to 256 VRMS (for 240 Vac models). See paragraph 1.8.3 for the main current requirements.

Connect 9465 power cable assembly as follows:

1. Check that circuit breaker CB1 is off.

2. Plug 9465 power cable assembly into mating three-wire grounded ac power distribution box receptacle.

2.5 CONFIGURATION

The 9465 is shipped with a Chassis Definition and Acceptance Record that supplies as-built configuration information. All strapping options and switch settings are factory set. Because the 9465 is suitable for many applications, PCBs are provided with straps and configuration switches to simplify changes. Only qualified maintenance personnel should perform configuration strapping or switch setting.

2.5.1 System Processor PCB (Z80)

System processor PCB (Z80) configuration switches and PROM locations are described in following paragraphs and tables. Unused switch positions are set to OFF.

2.5.1.a Switch Settings. Refer to table 2-2 for system processor PCB (Z80) configuration switch SW2 settings. Table entries marked with an asterisk are for debugger use only.

Table 2-2. System Processor PCB (Z80) Switch Settings

Switch SW2 (7W)	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Soft GPIF	OFF	OFF	-	-	-	-	-	-
Hard GPIF	ON	OFF	-	-	-	-	-	-
Serial host	OFF	ON	-	-	-	-	-	-
IEEE	ON	ON	-	-	-	-	-	-
Power-on erase	-	-	ON	-	-	-	-	-
No power-on erase	-	-	OFF	-	-	-	-	-
Not used	-	-	-	OFF	-	-	-	-
Not used	-	-	-	-	OFF	-	-	-
9460 debugger	-	-	-	-	-	ON*	-	-
9460 operating system	-	-	-	-	-	OFF	-	-
Port J1=joystick	-	-	-	-	-	-	ON*	-
Port J1=keyboard	-	-	-	-	-	-	OFF	-
Print host port	-	-	-	-	-	-	-	ON*
No print	-	-	-	-	-	-	-	OFF

Table 2-3 lists system processor PCB (Z80) configuration switch SW1 settings.

Table 2-3. System Processor PCB (Z80) Switch Settings

Switch SW1 (7X)	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Debugger program	ON*	-	-	-	-	-	-	-
System program	OFF	-	-	-	-	-	-	-
Not used	-	OFF	OFF	OFF	OFF	OFF	OFF	OFF

2.5.1.b PROM Locations. Table 2-4 lists processor PCB PROMs by location and part number. An asterisk after a part number in column three means that location is dependent upon which options are installed.

Table 2-4. System Processor PCB (Z80) PROM Locations

Description	Location	Part Number
RAMOS	2A	507763
RAMOS	2C	507764
RAMOS	2D	507765
GPIF	2E	507766
STDFW	2H	507767
STDFW	2J	507768
STDFW	2K	507769
DLPER	2M	507770
GRAF 1	2P	507772
GRAF 2	2S	507773
Init	-	507776*

2.5.2 System Processor PCB (MC68000)

Refer to table 2-5 for system processor PCB (MC68000) configuration switch SW1 settings.

Table 2-5. System Processor PCB (MC68000) Switch Settings

Switch SW1 (3X)	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Soft GPIF	OFF	OFF	-	-	-	-	-	-
Hard GPIF	ON*	OFF	-	-	-	-	-	-
Serial host	OFF	ON*	-	-	-	-	-	-
IEEE (not supported)	ON*	ON*	-	-	-	-	-	-
Power-on erase	-	-	ON*	-	-	-	-	-
No power-on erase	-	-	OFF	-	-	-	-	-
Not used	-	-	-	OFF	-	-	-	-
LUT init	-	-	-	-	ON	-	-	-
LUT not init	-	-	-	-	OFF	-	-	-
9460 debugger	-	-	-	-	-	ON*	-	-
9460 operating system	-	-	-	-	-	OFF	-	-
Port J1=joystick	-	-	-	-	-	-	ON*	-
Port J1=keyboard	-	-	-	-	-	-	OFF	-
Print host port	-	-	-	-	-	-	-	ON*
No print	-	-	-	-	-	-	-	OFF

Table entries marked with an asterisk are for debugger use only. Table 2-6 lists switch SW2 settings.

Table 2-6. System Processor PCB (MC68000) SW2 Settings

Switch SW2 (4X)	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Debugger program	ON*	-	-	-	-	-	-	-
System program	OFF	-	-	-	-	-	-	-
Not used	-	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Soft reset	-	-	-	-	-	-	-	ON
Hard reset	-	-	-	-	-	-	-	OFF

2.5.3 Video 12 PCB

Video 12 PCB switch settings control device selection and blink rate selection. Jumper strapping (figure 2-2) controls data input, graphics only selection, characters per line, vertical drive timing, and ninth-bit utilization.

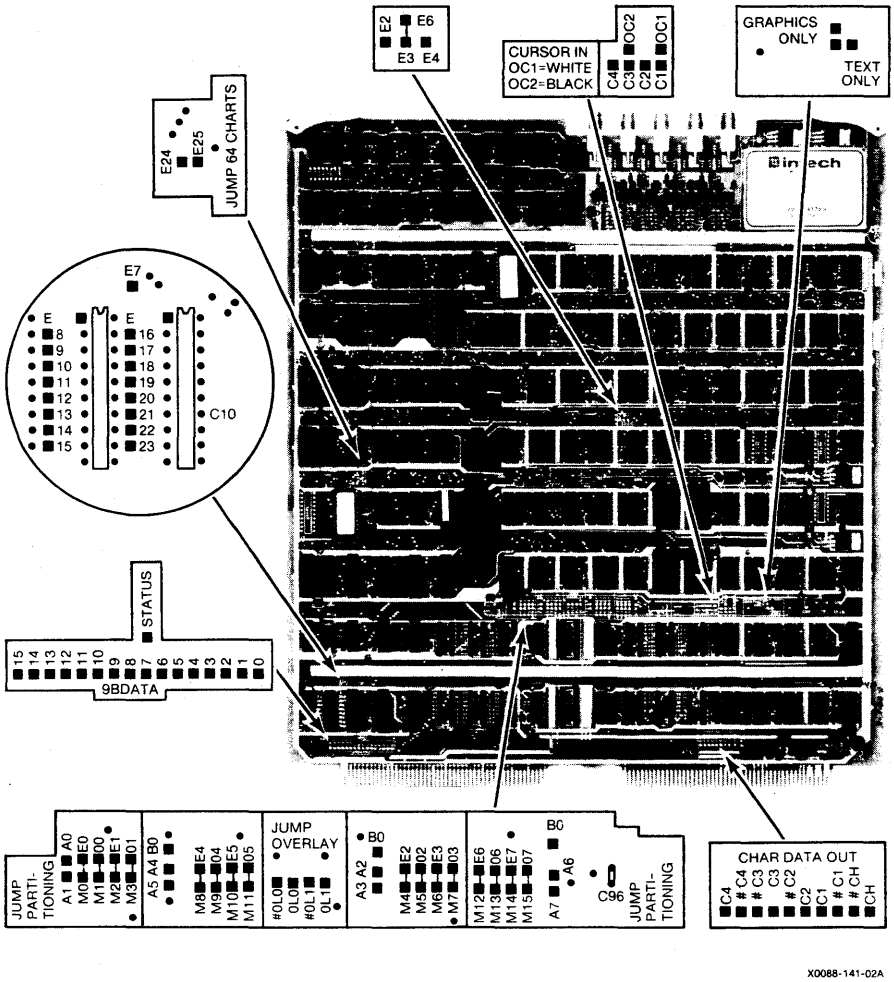


Figure 2-2. Video 12 PCB Strapping Location Diagram

2.5.3.a Device Selection. Table 2-7 lists device selection switch settings.

Table 2-7. Video 12 Device Select

PCB Number	Hexadecimal Address	Device Number	SW1 5	SW1 6
1	84 through 87	0/1	ON	ON
2	88 through 8B	2/3	OFF	ON
3	8C through 8F	4/5	ON	OFF
4	90 through 93	6/7	OFF	OFF

2.5.3.b Blink Rate Selection. Blink rate selection is controlled by four positions in switch SW1. Table 2-8 lists switch settings for 15 blink rates. Times in columns one and two are in seconds.

Table 2-8. Video 12 Blink Rate Select

Time ON	Time OFF	1	2	3	4
0.07	0.20	ON	ON	ON	ON
0.14	0.41	OFF	ON	ON	ON
0.20	0.61	ON	OFF	ON	ON
0.27	0.82	OFF	OFF	ON	ON
0.34	1.00	ON	ON	OFF	ON
0.41	1.20	OFF	ON	OFF	ON
0.54	1.60	OFF	OFF	OFF	ON
0.61	1.80	ON	ON	ON	OFF
0.68	2.00	OFF	ON	ON	OFF
0.75	2.20	ON	OFF	ON	OFF
0.82	2.40	OFF	OFF	ON	OFF
0.88	2.70	ON	ON	OFF	OFF
0.95	2.90	OFF	ON	OFF	OFF
1.00	3.10	ON	OFF	OFF	OFF
1.10	3.30	OFF	OFF	OFF	OFF

2.5.3.c Data Input Strapping. Table 2-9 lists video 12 data input strapping options for high resolution PCBs. Currently, low resolution is not supported.

2.5.3.d Resolution Select. Table 2-9 lists the video 12 strapping option for high resolution. Currently, low resolution is not supported.

Table 2-9. Video 12 Data Input

From	To	Resolution	9465 Memory Planes	Jumper Part Number
10P	10L	High	0-3	507621-05
9P	9L	High	4-7	-
10H	10L	High	8-11	507621-02
9H	9L	High	12-15	-
-	-	Low	-	-

Table 2-10. Video 12 Resolution Select

Resolution	From	To	Option Number
High	10W-5	7P-12	508336-01
Low	-	-	-

2.5.3.e Graphics Only Select. Table 2-11 lists the video 12 strapping option for graphics only operation. Currently, graphics and text is not supported.

Table 2-11. Video 12 Graphics Only Patch

Configuration	Patch Network	Option Number
Graphics and text	-	-
Graphics only	Install	508331-01

2.5.3.f Characters Per Line. Table 2-12 lists the video 12 strapping option for 80 characters per text line. Currently, 64 characters per line is not supported.

Table 2-12. Video 12 Characters Per Line

Characters Per Line	Jumper E24-25	Resolution	Option Number
80	Remove	1024 x 1280	Standard
64	-	-	-

2.5.3.g Vertical Drive Timing. Table 2-13 lists the video 12 strapping option for interlace mode. Currently, repeat mode is not supported.

Table 2-13. Video 12 Vertical Drive Timing

Field Type	Jumper	Option Number
Interlace	10V-11 to E7	Standard
Repeat	-	-

2.5.3.h Video 12 PCB Ninth-bit Strapping. Table 2-14 lists video 12 add and delete strapping for the ninth bit.

Table 2-14. Video 12 PCB MSB - 9th Bit

Mode	Add	Delete (Cut)
High resolution with blink	B0-07	MI5-07
Standard	B0-E7	MI4-E7
High resolution without blink	MI5-07	B0-07
Option 508328-01	MI4-E7	B0-E7

2.5.4 Serial Link PCB

This PCB can come with different PROMs installed. The complement of PROMs installed relates to how the PCB is configured with serial peripheral devices. Strapping is different when more than one serial link PCB is installed.

2.5.4.a PROM Sets. The following list identifies 2732 PROMs for serial link PCB installation.

- 504075-04 Serial link board (8 ports, with serial link PROMs 507968/969)
- 506817-05 Graphic tablet - cut and patch J3
- 506817-06 Graphic tablet - cut and patch J3 and J4
- 506817-07 Graphic tablet - cut and patch J3, J4, and J7
- 506817-08 Graphic tablet - cut and patch J3, J4, J7, and J8
- 507968-XX Serial link PROMs
- 507969-XX Serial link PROMs
- 506817-09 Ports 1 through 8 RS232 patch

The 2732 PROMs support keyboards, joysticks, trackballs, light pens, and graphic tablets. Serial link PCB PROM set part numbers 507968-XX and 507969-XX support 10 x 12 interlace operation. Graphic tablets are supported in menu and non-menu modes and must have an RS232 cut and patch.

2.5.4.b Conversion From RS232 To Differential. Table 2-15 lists jumpers that you must cut. Locate the port assignment and cut the corresponding jumpers. Terminal designations are omitted in the table; these terminal numbers are preceded by an "E" on the schematics and on the PCB.

Table 2-15. Cuts to Convert From Differential to RS232

Signals	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8
RD	13-16	27-30	49-51	65-66	86-87	100-101	122-123	136-137
RD	9-12	36-34	46-47	71-72	82-83	108-107	118-119	143-144
5RD-5RCDT	3-6	25-28	41-42	62-61	76-77	98-99	112-113	134-135
5CTS-5RTS	7-10	19-22	44-45	55-57	80-81	92-93	116-117	128-129
5DCD-5DTR	1-4	24-21	37-38	58-59	73-74	94-95	110-111	130-131
SD	15-18	32-33	52-53	67-68	88-89	104-103	124-125	140-139
4CS	152-153	158-159	-	-	172-173	178-179	-	-
1CS	155-156	161-162	-	-	175-176	181-182	-	-

Table 2-16 lists jumpers that you must install. Locate the port assignment and connect the corresponding jumpers. Terminal designations are omitted in the table; these terminal numbers are preceded by an "E" on the schematics and on the PCB.

Table 2-16. Jumpers to Convert From Differential to RS232

Signals	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8
CB	13-14	27-29	49-50	65-64	86-85	100-102	122-121	136-138
BB	9-11	36-35	46-48	71-70	82-84	108-106	118-120	143-142
5BB-5RCDT	3-5	25-26	41-40	62-63	76-78	98-97	112-114	134-133
5CLRS-5CTS	7-8	19-20	44-43	55-56	80-79	92-91	116-115	128-127
5RLDT-5DCD	1-2	24-23	37-39	58-60	73-75	94-96	110-109	130-132
BA	15-17	32-31	52-54	67-69	88-90	104-105	124-126	140-141
CA	152-151	158-157	163-164	167-168	172-171	178-177	183-184	187-188
CD	155-154	161-160	165-166	169-170	175-174	181-180	185-186	189-190

2.5.4.c Serial Link PCB Lightpen Port Assignments. With PROMs 507968 and 507969 installed, assign the light pen to port J1, J2, J5, and J6 only.

2.5.4.d Switch to Port Assignments. Ports are directly related to jack numbers. For example jack J1 is port assignment one and so on. Table 2-17 lists configuration switch assignments related to ports.

2.5.4.e Baud Rate Switch Settings. Baud rate switch settings for a serial link PCB with PROM sets 507968-01 and 507969-01 are in accordance with table 2-18. A graphic tablet port must run at 9600 baud. Baud rate switch settings for a serial link PCB with PROM sets 507968-02 and 507969-02 installed are in accordance with table 2-19.

Table 2-17. Serial Link PCB Switch to Port Assignments

Port (jack)	7C	7F	7K	7M	7R
J1	SW1	SW1	SW1	SW1	SW1
J2	SW2	SW2	SW2	SW2	SW2
J3	SW3	SW3	SW3	SW3	SW3
J4	SW4	SW4	SW4	SW4	SW4
J5	SW5	SW5	SW5	SW5	SW5
J6	SW6	SW6	SW6	SW6	SW6
J7	SW7	SW7	SW7	SW7	SW7
J8	SW8	SW8	SW8	SW8	SW8

Table 2-18. PROM Sets 507968-01 and 507969-01 Baud Rate Switch Settings

Baud Rate	Switch Setting 7K	7M	7R
110	OFF	OFF	OFF
300	OFF	OFF	ON
600	OFF	ON	OFF
1200	OFF	ON	ON
1800	ON	OFF	OFF
2400	ON	OFF	ON
4800	ON	ON	OFF
9600	ON	ON	ON

Table 2-19. PROM Sets 507969-02 and 507969-02 Baud Rate Switch Settings

Baud Rate	Switch Setting 7M	7R
1200	OFF	OFF
2400	ON	OFF
4800	OFF	ON
9600	ON	ON

2.5.4.f Device Selection. Table 2-20 lists device select switch settings for different serial link PCBs with options as listed. Where a 1 appears in the table, refer to baud rate switch settings for -01 PROM sets. A 2 in the table means that the graphics tablet is firmware set for 9600 baud operation. Where a 3 appears in the table, refer to baud rate switch settings for -02 PROM sets. Graphic tablet ports must have RS232 cut and patch. The following are the serial link PCB jumper numbers used with all PROMs: PCB 1 - E146 to E147 (standard run-in artwork); PCB 2 - cut E146 to E147, patch E145 to E147.

Table 2-20. Serial Link PCB Device Select Switch Settings

	Light Pen and Graphic Tablet with PN 507968-02 and PN 507969-02					Light Pen and Graphic Tablet with PN 507968-01 and PN 507969-01				
Switch 7	C	F	K	M	R	C	F	K	M	R
Keyboard	OFF	OFF	OFF	3	3	OFF	OFF	1	1	1
Joystick	ON	OFF	OFF	3	3	ON	OFF	1	1	1
Trackball	ON	OFF	OFF	3	3	ON	OFF	1	1	1
Lightpen	OFF	ON	OFF	3	3	OFF	ON	1	1	1
Graphic tablet without menu	ON	ON	OFF	3	3	ON	ON	ON	2	2
Graphic tablet with menu	OFF	OFF	ON	3	3	ON	ON	OFF	2	2

When a serial link PCB is installed in a 9465, the cursor patches must be cut at E21 to E23 and E22 to E24. If cursor patches are left in, cursor zero will break up.

2.5.5 Expansion PCB

Expansion PCBs are only installed in 9465 configurations that have a system processor PCB (Z80) installed. The expansion PCB has five configuration switches and a complement of PROMS. The complement of PROMs will vary according to customer requirements.

2.5.5.a Expansion PCB Switch Settings. Table 2-21 lists configuration switch settings. The switch at 11E is not used.

2.5.6 Video 7 PCB

In the 9465, the video 7 PCB (part number 505955-00, configuration part numbers 506959-02 and -04) can be configured two ways: high resolution with 13-bit VLT, or high resolution with 25-bit VLT. Figure 2-3 illustrates resistor pack positions. In addition, the any-to-any patches (figure 2-4) must correlate with the memory planes in the 9465. Table 2-22 lists jumper and resistor locations.

2.5.6.a High Resolution 13-Bit (part number 506959-02). Install single in-line resistor packs RP124, RP125, and RP126 (part number 3199221-01) in the upper positions (A3, A7, and A11) at 9U, 8T, and 8V. Install dual in-line resistor packs (part number 3122220-00) at 4F, 4M, and 4Y. Install single

Table 2-21. Processor Expansion PCB Switch Settings

PROM Type	Option	PCB Number	Hex. Address	SW5	SW4	SW3	SW2	SW1
		RAM Ending Address Switch 6N						
NA	-	1	50000	ON	ON	OFF	OFF	ON
NA	-	2	30000	ON	ON	OFF	ON	OFF
		RAM Starting Address Switch 5P						
NA	-	1	6FFFF	ON	ON	OFF	ON	ON
NA	-	2	4FFFF	ON	ON	OFF	OFF	ON
		ROM Starting Address Switch 10S						
2732	-	1	10000	ON	ON	OFF	OFF	OFF
		ROM Ending Address Switch 11P						
2732	-	1	1FFFF	ON	ON	ON	OFF	OFF
		ROM Type Select Switch 9N						
2732	-	-	-	-	-	-	OFF	OFF
		Options Address Range Switch 9N						
2716	2716	NA	-	-	-	ON	ON	-
2732	2732	NA	-	-	-	OFF	OFF	-
-	ROM enabled	-	-	-	-	ON	-	-
-	ROM disabled	-	-	-	-	OFF	-	-
-	range select	1	-	-	ON	-	-	-
-	range select	2	-	-	OFF	-	-	-

in-line resistor pack RP122 (part number 3199221-01) at 4C; if installed at 4C, remove resistor packs RP119, RP120, and RP121. Install the following jumpers:

E5-E6	E9-E10	E14-E15	E27-E28
E7-E8	E12-E13	E21-E22	E29-E30

Install the any-to-any jumpers after removing the following jumpers:

E3-E4	E10-E11	E17-E19	E16-E19

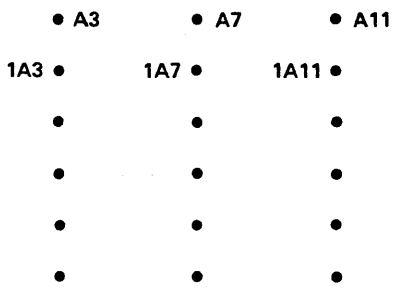


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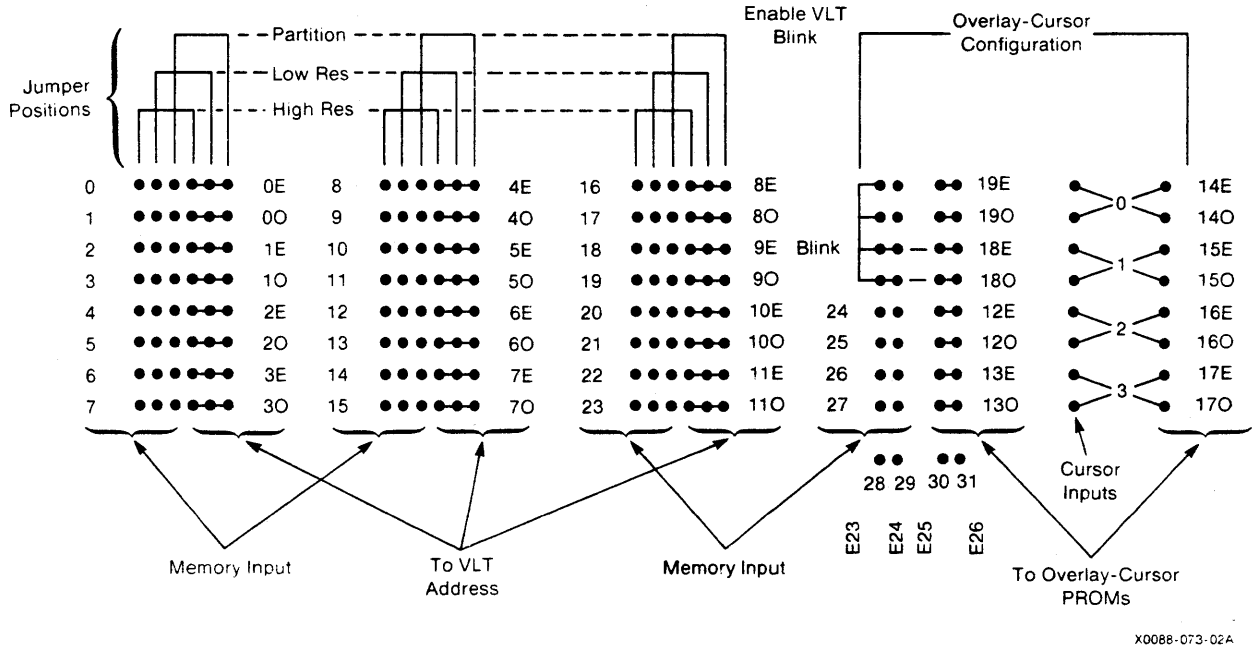
Figure 2-3. Video 7 PCB Resistor Pack Position



X0088-073-02A

Figure 2-4. Video 7 PCB Any-to-Any Patches

Table 2-22. Video 7 PCB Jumper and Resistor Locations

Resistors	Jumpers	Location
RP119	-	4C
RP120	-	4C
RP121	-	4C
RP122	-	4C
RP124	-	9U
RP125	-	8T
RP126	-	8V
-	E3 and E4	9C
-	E5 and E6	6C
-	E7 and E8	5C
-	E9, E10, and E11	8C
-	E12, E13, E14, and E15	4D
-	E16, E17, and E19	8A
-	E27, E28, E29, and E30	3D

2.5.6.b High Resolution 25-Bit (part number 506959-04). Install single in-line resistor packs RP124, RP125, and RP126 (part number 3199221-01) in the lower position (1A3, 1A7, and 1A11) at 9U, 8T, and 8V. Remove dual in-line resistor packs at 4F, 4M, and 4Y (if installed). Install single in-line resistor pack RP121 (part number 3199221-01) at 4C; if installed at 4C, remove resistor packs RP119, RP120, and RP122. Install the following jumpers:

E3-E4 E9-E10 E21-E22

Install the any-to-any jumpers after removing the following jumpers:

E5-E6	E10-E11	E16-E19	E14-E15
E7-E8	E17-E19	E12-E13	E27-E28

2.5.6.c Device Addressing. Refer to table 2-23 for address selection, PROM part number, and switch settings for the device you are installing. Switch 1 at location 11P is not used.

2.5.7 Video 8 PCB

The video 8 PCB has two independent sections because this PCB can drive two monitors. This means there are two video look-up tables (VLTs) and each VLT has a unique device number. Up to eight memory planes can feed each section; and there is a separate set of video connectors for each section. Likewise, cursor inputs are independent. Configuration switches control memory input selection, device selection, cursor blink rate (or no blink), and resolution selection. Some 9465 configurations can have multiple video 8 PCBs.

Table 2-23. Video 7 PCB Device Address

Dev.	Hex. Add.	Req. PROM 11S	Switch 11P 2	3	4	Switch 11CC 1 - 8	Switch 11DD 3 - 8
0	84-85	505565-01	ON	OFF	ON	8 ON; others OFF	All OFF
1	86-87	505565-01	ON	OFF	OFF	7 ON; others OFF	All OFF
2	88-89	505565-01	OFF	ON	ON	6 ON; others OFF	All OFF
3	8A-8B	505565-01	OFF	ON	OFF	5 ON; others OFF	All OFF
4	8C-8D	505655-01	OFF	OFF	ON	4 ON; others OFF	All OFF
5	8E-8F	505565-01	OFF	OFF	OFF	3 ON; others OFF	All OFF
6	90-91	505565-02	ON	ON	ON	2 ON; others OFF	All OFF
7	92-93	505565-02	ON	ON	OFF	1 ON; others OFF	All OFF
8	94-95	505565-02	ON	OFF	ON	All OFF	8 ON; others OFF
9	96-97	505565-02	ON	OFF	OFF	All OFF	7 ON; others OFF
10	98-99	505565-02	OFF	ON	ON	All OFF	6 ON; others OFF
11	9A-9B	505565-02	OFF	ON	OFF	All OFF	5 ON; others OFF
12	9C-9D	505565-02	OFF	OFF	ON	All OFF	4 ON; others OFF
13	9E-9F	505565-02	OFF	OFF	OFF	All OFF	3 ON; others OFF

2.5.7.a Memory Input Control. Table 2-24 lists memory input switch settings at 9H and 9S. A video 8 PCB can drive two monitors. Section 1 corresponding to monitor 1 can accept data from up to eight memory planes. Switch 9S controls memory plane selection for section 1. Switch 9H controls memory plane selection for section 2.

Table 2-24. Video 8 PCB Memory Input Selection

Planes Select	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
8	ON	ON	ON	ON	ON	ON	ON	ON
7	ON	ON	ON	ON	ON	ON	ON	OFF
6	ON	ON	ON	ON	ON	ON	OFF	OFF
5	ON	ON	ON	ON	ON	OFF	OFF	OFF
4	ON	ON	ON	ON	OFF	OFF	OFF	OFF
3	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
2	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF

2.5.7.b Status Jumper. Table 2-25 lists status jumpers for the video 8 PCB. Figure 2-5 shows how these connections are made.

2.5.7.c Device Selection. Table 2-25 lists switch 10N device select settings. Four hexadecimal addresses specify address counter and VLT for respective sections on each PCB. For example, 84(H) is the address counter for

device 0 on PCB 1; 85(H) is the VLT. Address 86(H) is the address counter for device 1; 87(H) is the VLT. This relationship applies to remaining PCBs.

Table 2-25. Video 8 PCB Status Jumper

PCB Number	Monitor	Jumper
0	1	Bit 2 to 0
0	2	Bit 1 to 1
1	1	Bit 2 to 2
1	2	Bit 1 to 3
2	1	Bit 2 to 4
2	2	Bit 1 to 5
3	1	Bit 2 to 6
3	2	Bit 1 to 7
4	1	Bit 2 to 8
4	2	Bit 1 to 9
5	1	Bit 2 to 10
5	2	Bit 1 to 11
6	1	Bit 2 to 12
6	2	Bit 1 to 13
7	1	Bit 2 to 14
7	2	Bit 1 to 15

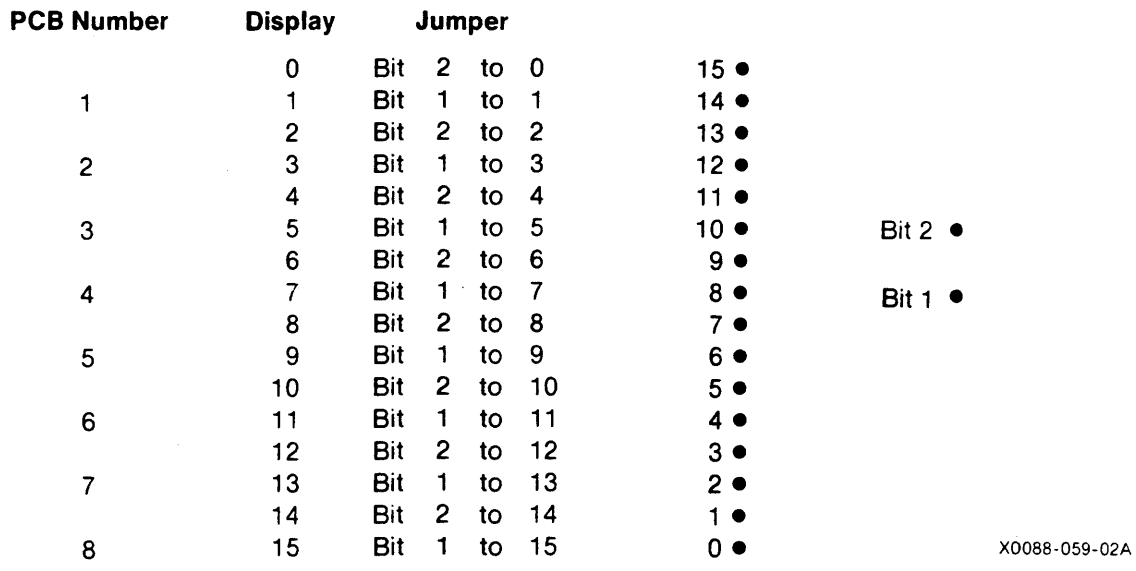


Figure 2-5. Video 8 PCB Jumper Status

Table 2-26. Video 8 PCB Device Select

PCB	Hexadecimal Address	Device	Switch 10N SW3	SW2	SW1
1	84 through 87	0 and 1	ON	ON	OFF
2	88 through 8B	2 and 3	ON	OFF	ON
3	8C through 8F	4 and 5	ON	OFF	OFF
4	90 through 93	6 and 7	OFF	ON	ON
5	94 through 97	8 and 9	OFF	ON	OFF
6	98 through 9B	10 and 11	OFF	OFF	ON
7	9C through 9F	12 and 13	OFF	OFF	OFF

2.5.7.d Cursor Blink Rate Control. Table 2-27 lists configuration control settings for switches at 9B that control cursor blink rate.

Table 2-27. Video 8 PCB Blink Generator

Blink Rate In Seconds	Switch 9B SW4	SW3	SW2	SW1
No Blink	ON	-	-	-
0.5	OFF	ON	ON	ON
1.0	OFF	ON	ON	OFF
1.6	OFF	ON	OFF	ON
2.1	OFF	ON	OFF	OFF
2.6	OFF	OFF	ON	ON
3.2	OFF	OFF	ON	OFF
3.7	OFF	OFF	OFF	ON
4.2	OFF	OFF	OFF	OFF

2.5.7.e Resolution Control. Set switch SW5 at 9B ON for high resolution. Currently, low resolution is not supported.

2.5.7.f Cursor Patching. There is only one cursor for each VLT. The patch at 11E determines cursor assignment (figure 2-6).

2.5.7.g Any-to-Any Patch. Any-to-any patching is illustrated in figure 2-7. A video 8 PCB configured for high resolution output requires two-bit data input.

2.6 CHECKOUT

This procedure tells how to verify operational performance of an installed 9465 operating with a Digital Equipment Corporation host computer.

1. Set circuit breaker CB1 to ON.

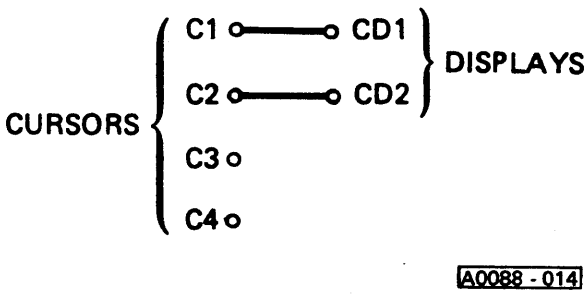


Figure 2-6. Cursor To Display Assignments

2. Open front access panel.

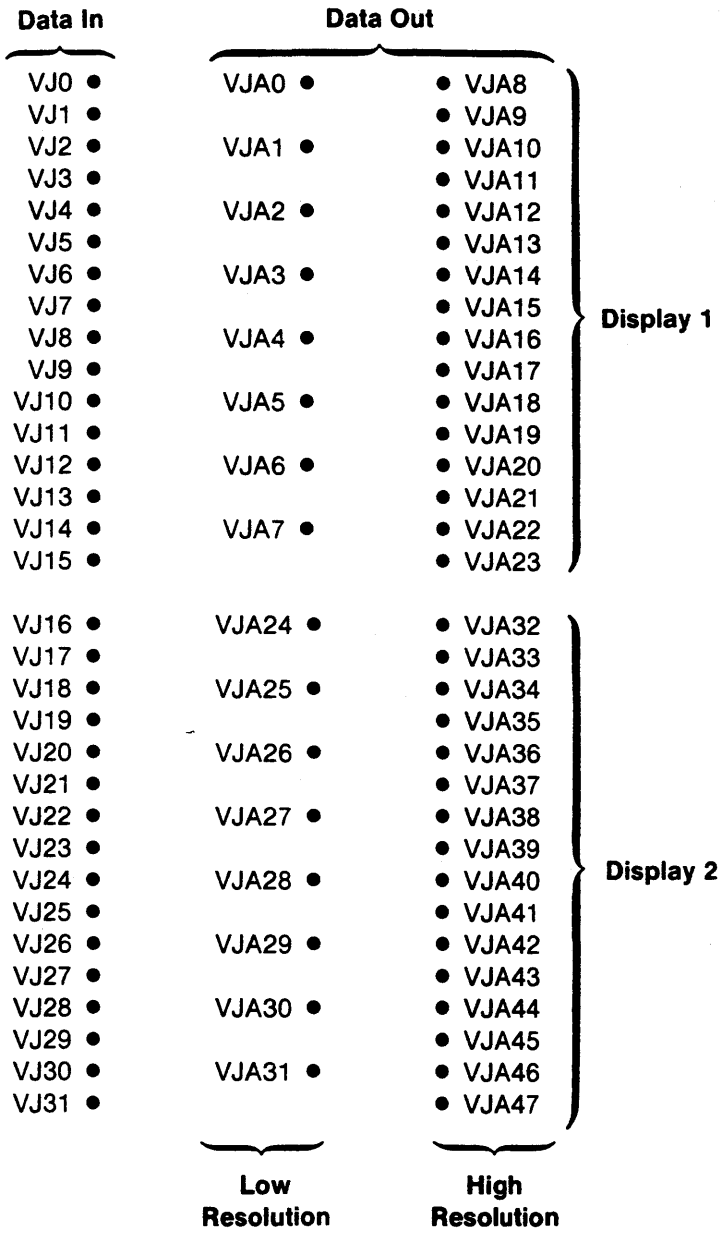
3. Set RES switch to the resolution of your 9465.

4. Close front access panel.

NOTE

To comply with FCC regulations for a Class A computing device, the cabinet front access panel must remain closed when power is applied to the 9465. The rear access panel can remain open and meet FCC regulations, but this practice may adversely affect component cooling. For these reasons the cabinet access panels should always remain shut when the 9465 is operating.

5. At host computer, load magnetic tape or diskette containing the diagnostic and acceptance tests. Run diagnostic and acceptance tests following procedures given in RM-9400/RM-9460 Diagnostic and Acceptance Test Operators Manual.



Note

Low resolution uses 1 bit for data input.
High resolution uses 2 bits for data input.

The cut-and-patch (above 11E) selects which cursor goes to which VLT.

X0088-070-02A

Figure 2-7. Video 8 PCB Any-to-Any Patching

Chapter 3

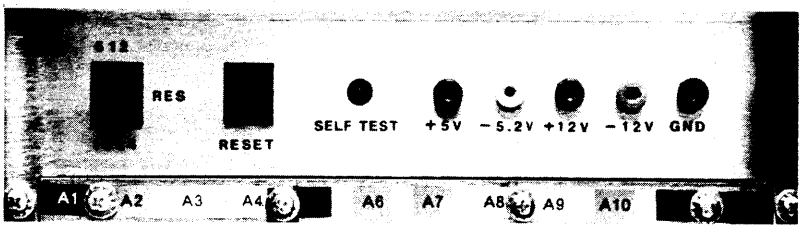
OPERATION

3.1 INTRODUCTION

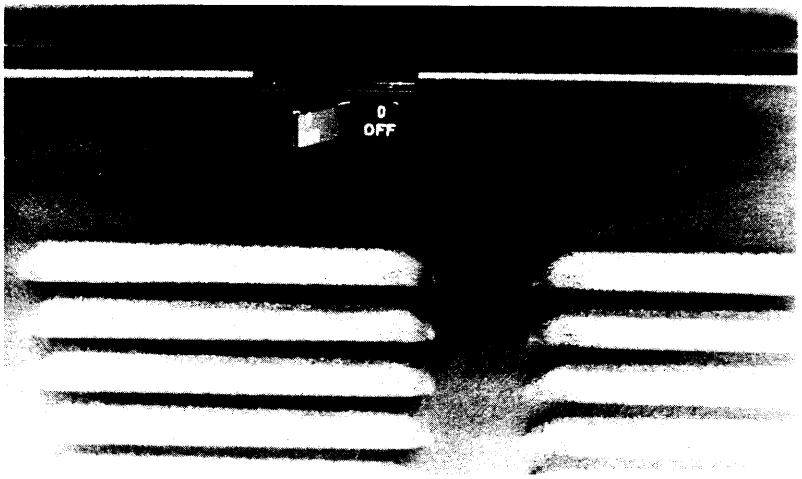
This chapter illustrates and describes 9465 controls and indicators. Operation instructions include turn-on, normal operation, emergency operation, and turn-off.

3.2 CONTROLS AND INDICATORS

The control panel (figure 3-1) mounts two controls, one indicator, and five test points. Circuit breaker CB1 mounts at the rear of the main chassis assembly. Table 3-1 lists and describes all controls and indicators.



Control Panel



Circuit Breaker

X0135-016-01A

Figure 3-1. Controls and Indicators

Table 3-1. Controls and Indicators

Control	Type	Function
RES	DPDT paddle switch	Controls resolution (512 or 1024)
RESET	Momentary SPDT paddle switch	Resets 9465 logic
SELF TEST	LED indicator	Lights during self test
+5V	Standard tip test point	+5V test point
-5.2V	Standard tip test point	-5.2V test point
+12V	Standard tip test point	+12V test point
-12V	Standard tip test point	-12V test point
GND	Standard tip test point	Ground
CB1	2-position circuit breaker	Applies power to 9465

3.3 9465 TERMINAL TURN-ON

Turn on the 9465 as follows.

1. Set circuit breaker CB1 to ON.
2. Open front access panel.
3. Verify RES switch is set to your system resolution (normally 1024)
4. Close front access panel.

NOTE

To comply with FCC regulations for a Class A computing device, the cabinet front access panel must remain closed when power is applied to the 9465. The rear access panel can remain open and meet FCC regulations, but this practice may adversely affect component cooling. For these reasons the cabinet access panels should always remain shut when the 9465 is operating.

3.4 OPERATING INSTRUCTIONS

During normal operation, the 9465 will not require operator intervention unless a reset is required or an emergency is encountered. Personnel responsible for operating the 9465 should read and understand the following information.

3.4.1 Normal Operating Instructions

If a reset is required, two methods are available; through software, or by operating the 9465 front panel RESET switch.

3.4.1.a Software Reset. In a 9465 with one MCP installed the RSET instruction performs a system-clear function identical to the power-on reset which occurs each time power is applied, or to the hardware reset accomplished with the RESET switch. All pending operations are discarded, but the video look-up table values remain in memory. In 9465 configurations with more than one MCP installed, the RSET instruction only resets the current context. Refer to the RM9460 Software Reference Manual for further details.

3.4.1.b Hardware Reset. Reset the 9465 by opening the front access panel and toggling the RESET switch. Close front access panel.

3.4.2 Emergency Operating Instructions

The 9465 is fused to prevent equipment damage should an overload condition occur. If, during any emergency that threatens equipment or personnel, you need to turn off power, set circuit breaker CB1 to OFF. Refer fuse replacement to qualified maintenance personnel.

3.5 9465 TERMINAL TURN-OFF

To turn off the 9465, set circuit breaker CB1 to OFF.

Chapter 4

FUNCTIONAL DESCRIPTION

4.1 SYSTEM CONCEPTS

This paragraph explains design concepts embodied in the 9465 and is a tutorial reference for the user. Because the 9465 is manufactured in many configurations, the discussions are necessarily generalized.

4.1.1 Raster Scan

Raster scan is a method of displaying images on a cathode ray tube (CRT) in broadcast television (TV) and TV monitors. Monitors come in two types: monochrome or color.

In a monochrome monitor a single CRT electron beam scans the CRT screen in a regular pattern, or raster. In repeat field scanning, the beam sweeps across the screen to trace a series of horizontal lines, one below the other. After completing the last line at the bottom of the screen, the beam returns to the top and repeats the scan pattern. Each set of lines is a frame. After completing each line the beam is turned off, or blanked, during the retrace period when the beam returns to begin the next line. Similarly, after completing the last line the beam is blanked during the return to the top. Images are formed by varying the beam intensity as the beam sweeps across the screen. With a sufficiently fast frame repetition rate the viewer gets the impression of a steady image.

Each horizontal line is divided into a number of picture elements (pixels), and each pixel is given an intensity value. Each image, therefore, consists of a matrix of pixels.

Interlacing is a raster scan method that minimizes image flicker. This result is achieved by replacing each frame with two interlaced fields. The beam first traces the odd-numbered lines to form the first field, then traces the even-numbered lines to form the second field.

In a color monitor three electron beams generate three rasters, one for each primary color (red, green, and blue). Each pixel is given three color values; the range of these values depends upon refresh memory capacity, and the digital-to-analog converters (DAC) installed. The three colors appear to the viewer as one blended color.

In colorgraphics applications, each color signal is transmitted to the monitor via an individual coaxial cable in contrast to color television broadcasting. Three separate cables eliminate the need to encode color information for transmission on a single carrier.

4.1.2 Refresh Memory

Refresh memory is a matrix of random access memory (RAM) cells. Digital data corresponding to display screen pixels is periodically loaded in refresh memory. Once loaded, refresh memory contents are not changed until modified by the program or by an operator acting through an interactive peripheral device.

The simplest data format that can describe an image is one refresh memory cell (or bit) for each display screen pixel. This is a two dimensional refresh memory and there is a one-to-one correspondence between x and y coordinates in refresh memory and display screen x and y coordinates. The total number of memory cells required is simply horizontal scan lines multiplied by pixels per line. With only one bit per pixel, this hypothetical device can only control on or off states of the electron beam, thus shading is impossible.

In colorgraphics, refresh memory is three dimensional, consisting of x, y values and an added z value. In the simplest colorgraphics system, three memory planes corresponding to primary colors red, green, and blue are installed. Such a system has limited color capability (eight colors) because only three bits are available per pixel. As memory planes are added, the z value increases, thus the number and variety of colors increases.

The output of refresh memory does not directly drive a display screen. Each x and y coordinate z value is actually an address for accessing a video lookup table entry.

4.1.3 Video Lookup Table (VLT) Principles

A VLT is a table of values satisfying the equation,

$$y = f(z)$$

where z is the address of the table and f is an arbitrary function. For example, given a table of four values and the function $f(z) = Z^2 + 1$, the table entries would be:

Table address (z)	Table entry [f(z)]
0	1
1	2
2	5
3	10
(etc)	(etc)

In a VLT then, a function is precomputed and values satisfying that function are later retrieved by simply accessing the appropriate table entry. This technique is normally used when "on-the-fly" computation requires too much time.

A Ramtek VLT consists of 64 to 4096 words of RAM. Total words and the bit assignments for each word depend on the video generator installed.

The advantage of a VLT is the speed and flexibility offered when a programmer can interactively change the arbitrary function "f" to achieve different color-intensity assignments instead of changing the data in refresh memory.

4.1.4 Multi-Processing

In the 9465, efficiency is achieved using multi-processing techniques. For example, the bit-slice microprocessor (BSM) in the MCP and the direct memory access (DMA) sequencer in the sync PCB perform processing tasks that would otherwise revert to the CPU on the system processor PCB. In this example, the MCP processes data for storage in refresh memory (memory PCBs), and the DMA can transfer data between devices sharing the same bus. Some examples are: from a host computer, peripheral device, or expansion PCB memory to the MCP. A microprocessor on the serial link PCB manages communication with up to eight serial devices and controls four cursors.

Multi-processing is especially useful for tasks that require complex operations such as coordinate transformation. Scale, rotate, and translate operations are carried out by a transform PCB (when installed).

4.2 SYSTEM RELATIONSHIPS

The 9465 is one part of a computer graphics system (figure 4-1). Precise system elements can vary depending upon application.

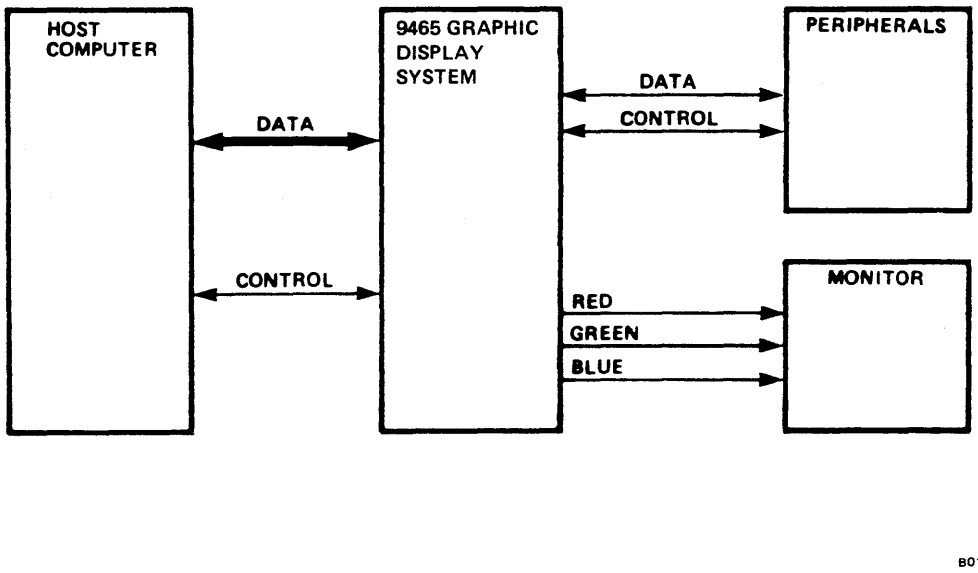


Figure 4-1. Generalized Computer Graphics System

Regardless of specific host computer model, peripherals selected, or application, a generalized system contains four elements:

- Host computer
- 9465
- Peripherals
- Monitor (or monitors)

4.2.1 Host Computer

Host computer tasks typically include storing, processing, and communicating formatted image or graphics data to the 9465. Depending upon user requirements, some computing tasks can be transferred to the 9465. These tasks might include display list processing, coordinate transformation, or pixel formatting.

4.2.2 9465

In a typical application, the 9465 accepts and interprets text, image, or graphics instructions and data from a host computer, performs CRT memory storage and CRT write operations, and supports multiple peripheral devices.

4.2.3 Peripherals

The 9465 supports serial transmission devices which operate in differential or RS232 modes. Devices include:

- Keyboards
- Graphic tablets
- Lightpens
- Joysticks
- Trackballs

With a keyboard installed, the user can interact via keystroke input. Keyboard characters are bidirectionally transmitted as 8-bit ASCII codes. Unique function codes extend the standard ASCII scheme.

A graphic tablet digitizes the position of a pointer placed in close proximity to the tablet working surface. The resulting x-y measurement is suitable for computer processing.

The lightpen is a fountain-pen-size device the operator points at the display screen to move a cursor or identify a displayed object. A light detector in the tip is enabled by the operator.

Joysticks and trackballs are cursor positioning devices. By moving a joystick shaft from the rest position, the operator can indicate direction, speed, and duration of cursor motion. Trackballs have a rotating sphere mounted on rollers. Encoders within the device sense and encode any displacement of the sphere. Both cursor positioning devices are limited in accuracy to the resolution of the display screen.

4.2.4 Monitor

The color monitor accepts red-green-blue (RGB) video signals from the 9465, amplifies and conditions these signals, and applies the result to the respective RGB electron guns of a high resolution color CRT. The CRT inner surface has a matrix of deposited phosphor tri-dots which are excited by the raster scanning motion of the RGB electron guns. An observer will see the resulting output as an image on the CRT. Since the phosphor dot matrix has a finite persistence, the 9465 must constantly refresh, or repaint the image. This CRT refreshing operation occurs at the raster scanning rate, and is fast enough to minimize flicker.

4.3 SIGNAL NAMES AND DRAWING CONVENTIONS

As an aid to understanding the PCB functional descriptions which follow, the mnemonics encountered in the 9465 are listed and described functionally. The schemes for designating components and for tracing signals through the block diagrams are also explained.

4.3.1 Signal Descriptions

Signal names appear in thirteen tables (table 4-1 through 4-13). There is one table for each 9465 PCB.

Signal mnemonics with numerical prefixes 0, 1, 2, 3, or 4 or with no prefix are high-active (logic 1). Prefixes 5, 6, 7, 8, 9, or an asterisk mean low-active (logic 0) signals. Prefixes with a pound sign mean differential signals.

4.3.2 Drawing Conventions

On the foldout block diagrams provided for each PCB, the numeral or numerals in the center of each block refer to corresponding logic diagram sheet numbers. In single sheet or foldout diagrams, a signal line identified with an ACC, ACW, BCC, or BCW number is tied to the backplane assembly. Otherwise, the numeral or numerals refer to blocks on associated logic sheets, or are reference numbers only. From and to designations are noted and connections to jacks or plugs are likewise specified.

An alphanumeric centered within a block refers to device coordinates on the PCB. The coordinate scheme is explained in chapter 1. Components within a single device are identified by output pin number. For example, 3P-2 and 3P-6 might represent inverters with outputs connected to pins 2 and 6 respectively, of device 3P.

Table 4-1. System Processor PCB (Z80) Signal Descriptions

Mnemonic	Description
A0-15	Address bits 0 through 15 (MOS bus)
8ADRP	Processor bus or display bus active*
BA	Transmit data
BAKIN	Bus acknowledge input
BAKOUT	Bus acknowledge output
BAUDCLK	Baud rate pulse
9BBUSY	Busy (display bus)*
BD3	Baud rate generator 3
9BDAT0-15	Data bits 0 through 15 (display bus)*
9BINT1-4	Interrupt requests 1-4 (display bus)*
9BIORQ	I/O request (display bus)*
4BMPT	Memory protect
8BMPT	Memory protect*
9BREAD	Read (display bus)*
4BREADY	Ready (display bus)
9BREQ	Bus request*
9BRESCLR	Reset clear (display bus)*
BUSAK	Bus acknowledge
*BUSAK	Bus acknowledge*
9BWAIT	Wait (display bus)*
9BWRT	Write (display bus)*
4BZADR0-18	Address bits 0 through 18 (processor bus)
9BZBUSY	Busy (processor bus)*
9BZDATA0-7	Data bits 0-7 (processor bus)*
BZIEO	Interrupt enable output (processor bus)
5BZIEO	Interrupt enable output (processor bus)*
9BZINT	Interrupt request (processor bus)*
9BZIORQ	I/O request (processor bus)*
9BZM1	Machine cycle 1 (processor bus)*
9BZMREQ	Memory request (processor bus)*
9BZREAD	Read (processor bus)*
9BZRFSH	Refresh (processor bus)*
9BZWAIT	Wait (processor bus)*
9BZWRITE	Write (processor bus)*
CA	Request to send data
9CAK	Acknowledge* (same as 9IOREADY)
CC	Data set ready
CD	Data terminal ready
CE	Ring
1CLINT	Clear interrupt
7CLINT	Clear interrupt*
5CLKHIRD	Clock high byte read*
CLKZ80	Clock Z80 (280-ns clock pulse)
1CLKZ80	Clock Z80 (280-ns clock pulse)
CLRSEND	Clear to send (section B)
9CLSTAT	Clear status*
9CREAD	Read* (same as 9IOREAD)
9CWRITE	Write* (same as 9IOWRT)

Table 4-1. System Processor PCB (Z80) Signal Descriptions (Continued)

Mnemonic	Description
CYSDMARY	Cycle steal DMA ready
D0-D7	Data bits 0 through 7 (MOS bus)
DCARDET	Data carrier detect
9DMADONE	DMA done*
DTERRDY	Data terminal ready (section B)
1E1-8	LED drive 1 through 8
ENADR	Enable address bus driver
6ENBAUD	Enable baud rate select register*
5ENCFS1	Enable configuration switch bank 1*
5ENCFS2	Enable configuration switch bank 2*
1ENCONTL	Enable control bus driver
5ENCYDMA	Enable cycle steal DMA*
6ENCYDMA	Enable cycle steal DMA*
5ENDAT	Enable data bus buffer*
5ENHCTC	Enable blanking interrupt controller*
5ENHSIO	Enable serial host I/O controller*
5ENICTC	Enable display bus interrupt controller*
5ENKSIO	Enable serial peripheral I/O controller*
ENMAP	Enable MAP unit
5ENMAP	Enable MAP unit*
6ENMCTC	Enable real time controller*
5ENMRD	Enable memory read*
5ENPPIO	Enable host status controller*
5ENSPIO	Enable serial interface controller*
3EQ	Eighth clock (140-ns clock pulse)
7EQ	Eighth clock (140-ns clock pulse)*
7FQ	Fourth clock (70-ns clock pulse)*
GOUSER	Change system state to user
*HALT	Halt*
5HIRD	High byte read*
5HIWR	High byte write*
6HIWR	High byte write*
7IFSTAT	Interface status*
*IINT	Interrupt request*
9IINT0-5	Interrupt requests 0 through 5*
5INTA	Interrupt acknowledge*
INTHOST	Interrupt request to host
IOBIT0-15	I/O bits 0 through 15
9IOBIT0-15	I/O bits 0 through 15*
9IOCLR	I/O clear*
IOCMD	I/O command
7IOCMD	I/O command*
9IOCMD	I/O command*
IOCMD1	I/O command 1
9IOINT	I/O interrupt request*
IOP	Address decode control
5IORD	I/O read*
1IOREAD	I/O read

Table 4-1. System Processor PCB (Z80) Signal Descriptions (Continued)

Mnemonic	Description
5IOREADY	I/O ready*
*IORQ	I/O request*
8IORQ	I/O request*
IOWDAT	I/O write data
5LDBBUA	Load configuration RAM data
5LDMA	Select MAP address*
5LDMU	Select user mode*
5LDST	Enable/disable MAP unit*
LEDOFF	LED off
5LORD	Low byte read*
6LORD	Low byte read*
5LOWR	Low byte write*
1M1	Machine cycle 1
*M1	Machine cycle 1*
*M1RES	Machine cycle 1 or reset*
6MADR1	Memory address 1*
6MADR2	Memory address 2*
5MADR5	Memory address 5*
5MADR6	Memory address 6*
MAP12-18	MAP bits 12 through 18
MAPA0-4	MAP address bits 0 through 4
5MAPS	MAP select*
*MD0-7	Memory data bits 0-7*
MEPROT	Memory protect
*MREQ	Memory request*
8MREQ	Memory request*
NTBQ	Clock pulse* (not used)
NTEQ	Eighth clock (140-ns clock pulse)*
NTFQ	Fourth clock (70-ns clock pulse)*
NTHQ	Half clock* (not used)
NTSQ	Sixteenth clock (280-ns clock pulse)*
9PORCLR	Power-on-reset clear*
PTBQ	Clock pulse (not used)
PTEQ	Eighth clock (140-ns clock pulse)
PTFQ	Fourth clock (70-ns clock pulse)
PTHQ	Half clock (not used)
PTSQ	Sixteenth clock (280-ns clock pulse)
*RD	Read*
8RD	Read*
RD1	Serial input from keyboard
*RD1	Serial input from keyboard*
RD2	Serial input from joystick
*RD2	Serial input from joystick*
5RDCRD	Read configuration RAM data*
7RDIFDAT	Read interface data*
5RDMD	Read memory data*
5RDMS	Read MAP status*
RDTLE	Read trailing edge

Table 4-1. System Processor PCB (Z80) Signal Descriptions (Continued)

Mnemonic	Description
7RDWIFD	Read or write interface data*
RDZ80	Read Z80A-CPU
5RECDAT	Serial input (section B)*
8REFSH	Refresh*
9RESET	Reset*
9RESET 1	Reset 1*
RESET1	Reset 1
6RESETH	Reset host*
RFEN	Refresh enable
8RFEN	Refresh enable*
*RFSH	Refresh*
5RFSRAS	Refresh row-address strobe*
ROD	Read output data
RQSEND	Request to send serial data (section B)
RWZ80	Read/write Z80A-CPU
SBA	Serial output (section A)
SCA	Request to send serial data (section A)
SCLRSEND	Clear to send (section A)
SD1	Serial output to keyboard
*SD1	Serial output to keyboard*
SD2	Serial output to joystick
*SD2	Serial output to joystick*
SDCARDET	Data carrier detect (section A)
SELECT	Select
SELFTST	Self-test
5SELMD	Select memory data*
5SERHA	Serial host I/O controller section A ready*
5SERHB	Serial host I/O controller section B ready*
5SERKJA	Serial peripheral I/O controller section A ready*
5SERKJB	Serial peripheral I/O controller section B ready*
SIFRDY	Soft interface data ready
5SIOCLK1	Serial I/O clock 1*
5SIOCLK3	Serial I/O clock 3*
5SIOCLK4	Serial I/O clock 4*
SRECDAT	Serial input (section A)
5SRECDAT	Serial input (section A)*
SSB	Serial input (section A)
5STXDAT	Serial output (section A)*
5SVC	Supervisor call*
8SVC	Supervisor call*
SVC1	Supervisor call#1
6SYS	Select system mode*
5SYSADR	System address*
9THBBB	Horizontal blanking*
9TVBBB	Vertical blanking*
5TXDAT	Serial output (section B)*
6USER	Select user mode*
*WAIT	Wait*

Table 4-1. System Processor PCB (Z80) Signal Descriptions (Continued)

Mnemonic	Description
7WLED	Enable LED register*
*WR	Write*
8WR	Write*
5WRCRD	Write configuration RAM data*
7WRIFDAT	Write interface data*
5WRMD	Write memory data*
WRTZ80	Write Z80A-CPU
XB	Interrupt enable
XC	Interrupt enable
XE	Interrupt enable
XF	Interrupt enable
XH	Interrupt enable
XI	Interrupt enable
XK	Interrupt enable
XL	Interrupt enable
XP	Interrupt enable
XQ	Interrupt enable
XV	Interrupt enable

Table 4-2. System Processor PCB (MC68000) Signal Descriptions

Mnemonic	Description
148NSEC	148-nanosecond clock pulse
*148NSEC	148-nanosecond clock pulse*
296NSEC	296-nanosecond clock pulse
296NSZ80	296-nanosecond Z80 clock pulse
40148(5DMAX)	DMA transfer*
A1-23	Address bits 1 through 23 (68000 bus)
ARDY	Section A ready
5AS	Address strobe*
5ASTB	Section A strobe*
4BADR0-7	Address bits 0 through 7 (display bus)
BAKIN	Bus acknowledge in
BAKOUT	Bus acknowledge out
BAUD1-4	Baud rate pulses 1 through 4
5BAUDEN	Load baud rate data* (with 5WRZ)
9BBUSY	Bus busy*
9BDAT0-15	Data bits 0 through 15 (display bus)*
9BIOREQ	I/O request (display bus)*
BRDY	Section B ready
9BREAD	Read (display bus)*
9BREQ	Bus request*
9BRESCLR	Reset clear (display bus)*
5BSTB	Section B strobe*
9BWRT	Write (display bus)*
4BZADR0-7	Address bits 0 through 7 (processor bus)*
9BZDAT0-7	Data bits 0 through 7 (processor bus)*
BZIEO	Interrupt enable output (processor bus)
9BZINT	Interrupt (processor bus)*
9BZIORQ	I/O request (processor bus)*
9BZM1	Machine cycle 1 (processor bus)*
9BZREAD	Read (processor bus)*
9BZWAIT	Wait (processor bus)*
5CAS	Column address strobe*
9CDAT0-15 (9IOBIT0-15)	Data bits 0 through 15 (interface bus)*
1CLINT	Clear processor status register
7CLINT	Clear processor status register*
CLR1-4	Clear 1 through 4
5CLREN	Interrupt reset register enable*
9CLSTAT	Clear status*
5CLSTR	Clear status register*
9CREAD (9IOREAD)	I/O read*
CTSA	J3 is ready to receive
CTSB	J4 is ready to receive
9CWRITE (9IOWRT)	I/O write*
D0-15	Data bits 0 through 15 (68000 bus)
DA0-7	Decode address bits 0 through 7

Table 4-2. System Processor PCB (MC68000) Signal Descriptions (Continued)

Mnemonic	Description
DCDA	J3 is ready to send
DCDB	J4 is ready to send
9DMADONE	DMA done*
9DMARST	DMA reset*
5DTACK	Data transfer acknowledge*
DTRA	Ready to receive from J3
DTRB	Ready to receive from J4
E1-8	LED drive 1 through 8
1ENCONTL	Enable control bus
FC0-2	Function code bits 0 through 2
H1-4	Handshake 1 through 4
HWRT	Host write
5IED04	Interrupt enable output 4*
IEI3	Interrupt enable input 3
IE03	Interrupt enable output 3
IFCOMMAND	Interface command
IFREAD	Interface read
7IFSTAT	Interface status*
IFWRITE	Interface write
9IINT0,1,4,5	Interface interrupts 0,1,4,5*
5INT	Interrupt*
INTHOST	Interrupt host
9IOBIT0-15	Data bits 0 through 15 (interface bus)*
IOCMD	I/O command
9IOCMD	I/O command*
IOCMD1	I/O command
IOCMD1	I/O command 1
IOCMD1	I/O command 1
IOD0-7	Data bits 0 through 7 (transfer bus)
IOEN	I/O request enable
9IOINT	I/O interrupt*
9IOPCLR	I/O power-on clear*
5IORD	I/O read*
5IORD	I/O read*
1IOREAD	I/O read
1IOREAD	I/O read
5IOREADY	I/O ready*
5IOREADY	I/O ready*
9IOREADY	I/O ready*
5IORQ	I/O request*
IOWDAT	I/O write data
IPL0-1	Interrupt priority lines 0 through 2
5LDS	Lower data strobe*
LEDCK	LED register clock pulse
5LEDEN	LED register enable*
5M1	Machine cycle 1*
5MREQ	Memory request*
55NSEC	55-nanosecond clock pulse

Table 4-2. System Processor PCB (MC68000) Signal Descriptions (Continued)

Mnemonic	Description
PIO2EN	Parallel I/O 2 enable
5PIODTACK	Parallel I/O data transfer acknowledge*
PIRQ	Priority interrupt request
9PORCLR	Power-on clear*
PRIO1,2	Priority interrupts 1,2
5RAMEN	RAM enable*
5RAMRD	RAM read*
5RAMWR	RAM write*
5RAS0,1	Row address strobe 0,1*
5RD	Read*
RD1	Serial input from keyboard
*RD1	Serial input from keyboard*
RD2	Serial input from joystick
*RD2	Serial input from joystick*
RD68	Read 68000
RDTLE	Read trailing edge
RDTLE	Read trailing edge
7RDWIFD	Read or write interface data*
5RDWR68	Read or write 68000
5RDZ	Read Z80*
RESET	Reset
5RESET	Reset*
1RESETRW	Reset read or write
ROD	Read output data
5ROMEN	ROM enable*
RTSA	Ready to send to J3
RTSB	Ready to send to J4
5RW68	Read or write 68000*
RWIFD	Read or write interface data
RWIFD	Read or write interface data
RXDA	Serial input from J3
RXDB	Serial input from J4
SD1	Serial output to keyboard
*SD1	Serial output to keyboard*
SD2	Serial output to joystick
*SD2	Serial output to joystick*
SIFRDY	Soft interface ready
5SIO1EN	Serial I/O 1 enable*
5SIO2EN	Serial I/O 2 enable*
SOFRST	Software reset
5SYSADR	System address*
9THBBB	Horizontal blanking timing*
9TVBBB	Vertical blanking timing*
5TXDA	Serial output to J3
5TXDB	Serial output to J4
5UDS	Upper data strobe*
5VINT	Valid interrupt*
VPA	Valid peripheral address

Table 4-2. System Processor PCB (MC68000) Signal Descriptions (Continued)

Mnemonic	Description
5WAIT	Wait*
5WE	Write enable*
5WR	Write*
WR68	Write 68000
7WRIFDAT	Write interface data*
5WRZ	Write Z80*
5XACK	Transfer acknowledge*
XMIT	Transmit
ZA0-7	Address bits 0 through 7 (Z80 bus)
ZD0-7	Data bits 0 through 7 (Z80 bus)
ZINT	Z80 interrupt
8ZWAIT	Z80 wait

Table 4-3. MCP PCB Signal Descriptions

Mnemonic	Description
7ADSL	Address select
4BADDR0-7	Address bus
9BDAT0-15	Data bits 0-15 (display bus)
BEMPTY	Buffer empty
BFULL	Buffer full
9BPORCLR	Power-on reset clear
9BREAD	Read
BREADY	Ready
4BSEL0-2	Select MCP
*BUSY	DMA in process
9BWAIT	Wait
9BWRT	Write
9C/L	Clear/load
*CLEAR	Packing control logic clear
*CLRIO	Clear input/output logic
CRBDEN	Enable MTS RAM output to internal bus
9DAD0-7	Memory address bus
9DADSL	Address select
9DAS0-4	RAM address strobe
9DCAS	Column address strobe
9DGD0-15	Data bits 0-15 (memory bus)
9DHSERS	High-speed erase
DMA	Start DMA
9DMWR	Memory write
*DONE	Read or write done
9DRAS	Row address strobe
9DRBEN	Readback enable
9DRBL	Readback load
*DRVIN	Memory bus to internal bus enable
*DRVOUT	Internal bus to memory bus enable
9DSEL	Data select
9DSRHP	Shift register hold pulse
9DSRLP	Shift register load pulse
9DSTRTCH	Stretch
9DZOOM	Zoom
9DZOOM0	Zoom 0
*ENDGWE	Enable memory write
*ENGRDET	Enable graphic entity detect mode
GDMODE	Graphic entity detect mode
9GEN	Group enable
	GRDET
4H*MX	System resolution
4H*MY	System resolution
*INT512	Interlace 512 line
8INTLC	Interlace
9INTLC	Interlace
IOCMPL	Input/output operation completed
*IPSEL	MTS RAM data select

Table 4-3. MCP PCB Signal Descriptions (Continued)

Mnemonic	Description
4L*MY	System resolution
5LCOUNT	Element zoom counter enable
*LDXORG	Load X origin register
*LDXZM	Load X zoom register
*LDYORG	Load Y origin register
*LDYZM	Load Y zoom register
*LXHI	Latch high byte
*LXLO	Latch low byte
7MADSL	Address select
4MADSL	Memory refresh enable
9MBGRANT	Memory bus request granted
MBTRIST	Disable MCP outputs
9MBUSRQ	Memory bus request
MINUSX	Decrease X
MINUSY	Decrease Y
MRMUX1	Memory refresh multiplex 1
MTSOP0-2	MTS operation code 0-2
4MY*559	System resolution
NTFQ	Fourth clock (70-ns clock pulse)
NTHQ	Half clock (35-ns clock pulse)
NTMCQ	MCP clock
*PAKIN	Enable buffer to memory bus
PL52	Instruction word bit 52 (status bit)
PLUSX	Increase X
PLUSY	Increase Y
PTD0-15	Internal bus 0-15
PTFQ	Fourth clock (70-ns clock pulse)
PTHQ	Half clock (35-ns clock pulse)
PTMCQ	MCP clock
*QCLEAR	Restart/next instruction clear
*RDMCP	Enable buffer to display bus
*RESET	Reset
*REVHI	Reverse high byte
*REVLO	Reverse low byte
9RFW	Register file write
RWCOL0-7	Read/write column addresses 0-7
RWROW0-7	Read/write row addresses 0-7
8SELX	Select X-axis resolution
9SELX	Select X-axis resolution
*STEALIT	Select MTS operation code
9THBBB	Horizontal blanking pulse
8THBLK	Horizontal blanking pulse
8THMMM	Horizontal memory pulse
9THMMM	Horizontal memory pulse
9TVBBB	Vertical blanking pulse
9TVFFF	Vertical field pulse
8TVMMM	Vertical memory pulse
9TVMMM	Vertical memory pulse

Table 4-3. MCP PCB Signal Descriptions (Continued)

Mnemonic	Description
UB0-3	MTS RAM address
*UWE	MTS RAM write enable
WAIT	Read or write in progress
*YZOOM0	Y zoom status
*ZOOM0	X zoom status

Table 4-4. Memory PCB Signal Descriptions

Mnemonic	Description
5ADSL	Address select
9C/L	Clear/load memory select logic
8CKLT	Plane selector latch
9DAD0-7	Address 0-7
9DADSL	Address select
9DAS0-4	Address strobe 1-4
9DCAS	Column address strobe
9DG0-15	Memory bus
9DHSERS	High speed erase
9DMSK	Low or high byte selector
9DMWR	Memory write
1DRAS	Row address strobe
2DRAS	Row address strobe
9DRAS	Row address strobe
8DRBEN	Read-back enable
9DRBEN	Read-back enable
8DRBL	Read-back latch
9DRBL	Read-back latch
9DSEL	Select
4DSRHP	Shift register hold pulse
9DSRLP	Shift register load pulse
9GP1-3	Group select 1-3
HP1-H	Hold pulse 1-4
7HQ4	Half basic clock frequency
7HQ5	Half basic clock frequency
7HQ6	Half basic clock frequency
7HQ6	Half basic clock frequency
MCAS1-4	Column address strobe 1-4
NTFQ	Negative fourth basic clock frequency
NTHQ	Negative half basic clock frequency
NTMCQ	Negative MCP clock
P0-7EVEN	Plane 0-7 even data out
P0-7MDIN	Plane 0-7 memory data in
P0-7MRW	Plane 0-7 memory read/write
P0-7ODD	Plane 0-7 odd data out
P0-7RBDATA	Plane 0-7 readback data
P23ADR0-7	Planes 2 and 3, address 0-7
P45ADR0-7	Planes 4 and 5, address 0-7
P67ADR0-7	Planes 6 and 7, address 0-7
PMRAS0-19	Row address strobe 0-19
P01ADR0-7	Planes 0 and 1, address 0-7
PRDMUX0-2	Readback data select
PRDSEL0-2	Readback data multiplexer select
PTFQ	Positive fourth basic clock frequency
PTHQ	Positive half basic clock frequency
PTMCQ	Positive MCP clock
RFRA (P1,P2)	Register file read A
RFRB (P1,P2)	Register file read B

Table 4-4. Memory PCB Signal Descriptions (Continued)

Mnemonic	Description
RFW	Register file write
RFW1-4	Register file write 1-4
RFWA (P1,P2)	Register file write A
RFWB (P1,P2)	Register file write B
SHFLD1-4	Shift register load 1-4
TGIS	This group is selected
6TGIS	This group is selected
9THMMM	Horizontal memory timing
VP0-15	Video data 0-15
8WEN	Write enable

Table 4-5. Video 12 PCB Signal Descriptions

Mnemonic	Description
A0-3	Character controller addresses
AL0-8	Graphics VLT address
4BADR0-7	Address bus
9BDATA00-15	Data bits 0-15 (display bus)
BLACK	Black cursor
5BLANK	Blanking
BO	Blink oscillator
9BREAD	Read
9BWAIT	Wait
9BWRT	Write
5CB	Composite blanking
CBO	Blink oscillator
CCD	Text blanking
CD0-11	Character data bus
5CDS	Character controller write
1CHARD	Delayed text data
CHCS	Character controller read
5CS	Composite sync
5CSYC	Composite sync
8CURS1-4	Cursor data
#CURS1-4	Cursor data return
4CURSOR	White cursor
D0-10	Text data bus
9DSTRCH	Stretch
9DZOOM	Zoom
9DZOOM0	Zoom 0
E35	Resolution
E70	Resolution
ED0-8	Graphics data
GREY	8-bit DAC output
4H*MX	System resolution
4H*MY	System resolution
5HI	Resolution
5INC	Increment graphics address counter
INCC	Increment text address counter
4L*MY	System resolution
5L0-7	Graphics VLT output
5LOAD	Load graphics address counter
5LOC	Load text address counter
4MY*559	System resolution
NTBQ	Base clock (17.5-ns clock pulse)
NTEQ	Eighth clock (140-ns clock pulse)
NTFQ	Fourth clock (70-ns clock pulse)
NTHQ	Half clock (35-ns clock pulse)
4OVL	Overlay
2P10	Cursor intensity
5P10	Cursor intensity
9PORCLR	Power-on reset clear

Table 4-5. Video 12 PCB Signal Descriptions (Continued)

Mnemonic	Description
PTBQ	Base clock (17.5-ns clock pulse)
PTEQ	Eighth clock (140-ns clock pulse)
PTFQ	Fourth clock (70-ns clock pulse)
PTHQ	Half clock (35-ns clock pulse)
SD13	Text data
SD23	Text data
9TCBBB	Composite blanking
9TCSSS	Composite sync
9THDDD	Horizontal drive
9TVDDD	Vertical drive
9VD0-31	Refresh memory data
#VD0-31	Refresh memory data return
7VDT	Vertical drive time
VID1-4	2-bit DAC outputs
5WC	Text VLT write control
5WLE	Odd VLT write control
5WLO	Even VLT write control
5WO	Write character video on

Table 4-6. Sync PCB Signal Descriptions

Mnemonic	Description
4ADR0-7	Address bits 0 through 7 (sync bus)
9ADRSL	Address select*
4BADR0-7	Address bits 0 through 7 (display bus)
9BBUSY	Bus busy*
9BDATA00-15	Data bits 0 through 15* (sync bus)
9BD00-15	Data bits 0 through 15 (display bus)*
7BQ	Basic clock (17-ns clock pulse)*
BREADY	Ready (display bus)
9BREQ	Bus request*
9BRESCLR	Reset clear* (display bus)
9BSWCLR	Switch clear* (display bus)
9BWAIT	Wait* (display bus)
CLKTTL	TTL clock pulse
#CURS1	Cursor 1
8CURS1	Cursor 1*
D2J-A	Decoder 2J, output A
D2J-B	Decoder 2J, output B
9DAD00-06	Address bits 0 through 6* (memory bus)
9DADSL	Address select* (memory bus)
9DCAS	Column address strobe* (memory bus)
9DCINTRL	Decoded interlace signal*
9DECODE	Decode*
9DLOC	Latch output control* (memory bus)
9DMADONE	DMA done*
9DMADSL	DMA select* (memory bus)
9DMLP	Memory load pulse* (memory bus)
9DRAS	Row address strobe* (memory bus)
9DRBL	Readback load* (memory bus)
9DSRHP	Shift register hold pulse* (memory bus)
9DSRLP	Shift register load pulse* (memory bus)
9DZOOM	Zoom (memory bus)
ELENBL	Element counter enable
6ENRDADR	Enable read address*
6ENWRADR	Enable write address*
1EQ	Eighth clock (140-ns clock pulse)
7EQ	Eighth clock (140-ns clock pulse)*
1FQ	Fourth clock (70-ns clock pulse)
7FQ	Fourth clock (70-ns clock pulse)*
7FQA	Not used
7FQSL	Fourth clock selected*
4H*MX	Horizontal resolution select bit
4H*MY	Vertical resolution select bit
1HQ	Half clock (35-ns clock pulse)
7HQ	Half clock (35-ns clock pulse)*
7HQSL	Half clock selected*
9INTLC	Interlace*
INTRL	Interlace
9IOREQ	I/O request*

Table 4-6. Sync PCB Signal Descriptions (Continued)

Mnemonic	Description
4L*MY	Vertical resolution select bit
9LDCREC	Load cursor element counter*
9LDCREL	Load cursor element register*
9LDCRLN	Load cursor line register*
*LINC	Increment line counter*
7MCQ	Memory control clock pulse*
9MRSEL	Memory select*
4MY*559	Vertical resolution select bit
NTBQ	Basic clock (17-ns clock pulse)*
NTEQ	Eighth clock (140-ns clock pulse)*
NTFQ	Fourth clock (70-ns clock pulse)*
NTHQ	Half clock (35-ns clock pulse)*
NTMCQ	Memory control clock pulse*
NTSQ	Sixteenth clock (280-ns clock pulse)*
9PLEN	Parallel load enable*
PRORAMLD	Load RAM program
PTBQ	Basic clock (17-ns clock pulse)
PTEQ	Eighth clock (140-ns clock pulse)
PTFQ	Fourth clock (70-ns clock pulse)
PTHQ	Half clock (35-ns clock pulse)
PTMCQ	Memory control clock pulse
PTSQ	Sixteenth clock (280-ns clock pulse)
R4S-Q1	Register 4S, output Q1
R6L-Q3	Register 6L, output Q3
7RDDMARM	Read DMA RAM*
9RDEN	Read enable*
9RDRES	Read resolution*
9READ	Read*
6RESETH	Reset host*
9SELX	Horizontal resolution select bit
1SQ	Sixteenth clock (280-ns clock pulse)
7SQ	Sixteenth clock (280-ns clock pulse)*
8SWCLR	Switch clear* (display bus)
7SYNCLR	Sync clear*
9SYNCLR	Sync clear*
9TCBBB	Composite blanking timing pulse*
TCS	Composite synchronization timing pulse
9TCSSS	Composite synchronization timing pulse*
9THBBB	Horizontal blanking timing pulse*
9THDDD	Horizontal drive timing pulse*
THM	Horizontal memory timing pulse
9THMMM	Horizontal memory timing pulse*
TVB	Vertical blanking timing pulse
9TVBBB	Vertical blanking timing pulse*
9TVDDD	Vertical drive timing signal*
TVF	Vertical field timing pulse
9TVFFF	Vertical field timing pulse
TVM	Vertical memory timing pulse

Table 4-6. Sync PCB Signal Descriptions (Continued)

Mnemonic	Description
9TVMMM	Vertical memory timing pulse*
5WCLEAR	Switch clear*
7WDMARM	Write DMA RAM*
7WRDM	Write DMA*
WRESET	Switch reset
9WRT	Write*
Z8Q	Z80 clock pulse

Table 4-7. Serial Link PCB Signal Descriptions

Mnemonic	Description
A0-15	Address bits 0 through 7 (MOS bus)
1BA0-15	Address bits 0 through 7 (TTL bus)
5BAUDLD	Load baud rate data*
5BD0-7	Data bits 0 through 7 (TTL bus)*
5BDREAD	Read TTL data bus*
2BLINK1	Blink
5BLKCLK	Blink
5BRSEL1-3	Baud rate select 1 through 3*
5BV1LD-4LD	Load cursor control data*
1BZADR0-7	Address bits 0 through 7 (processor bus)
4BZADR0-7	Address bits 0 through 7 (processor bus)
9BZBU6Y	Busy*
BZDAT0-7	Data bits 0 through 7 (processor bus)
9BZDAT0-7	Data bits 0 through 7 (processor bus)*
BZIEI	Interrupt enable
1BZIEI	Interrupt enable
BZIEO	Interrupt enable
9BZINT	Interrupt request*
1BZINTA	Interrupt acknowledge
7BZIOP	Processor bus address decode control*
8BZIORQ	I/O request*
9BZIORQ	I/O request*
8BZM1	Machine cycle 1*
9BZM1	Machine cycle 1*
8BZRD	Read*
9BZREAD	Read*
2CLKZ80	280-ns clock pulse
9CS1, 2, 5, 6	Composite sync 1, 2, 5, 6*
#CS1, 2, 5, 6	Composite sync return 1, 2, 5, 6
9CSSS	Composite sync *
1CUR1A0-7	Cursor address bits 0 through 7
6CUR1D0L-7L	Cursor generator 1 latched data bits 0 through 7
5CUR1D0R-7R	Cursor generator 1 RAM data bits 0 through 7
5CUR1LD-4LD	Load cursor generators 1 through 4*
5CUR1VEN-4VEN	Enable line counters 1 through 4*
1CURGEN1	Cursor generator 1 output
6CURGEN1-4	Cursor generator 1 through 4 outputs*
#CURS1-4	Cursor output returns 1 through 4
8CURS1-4	Cursor outputs 1 through 4*
5CURT1	Cursor RAM output control*
6CURT1-4	Cursor RAM output controls 1 through 4
2CZ80	280-ns clock pulse
D0-7	Data bits 0 through 7 (MOS bus)
1E1A0-2	Element address bits 0 through 2
6E1D0-9	Element counter data bits 0 through 9*
5ELSBCS	Element counter LSB*
5EMSBCS	Element counter MSB*
5ENBZCTC	Data output control*

Table 4-7. Serial Link PCB Signal Descriptions (Continued)

Mnemonic	Description
5ENBZPIO	Data output control*
5ENCTCSL	Enable blink controller
5ENPIOSL	Enable processor data bus controller*
5ENSIOA-D	Enable serial I/O controllers 1 through 4
1ESEL1	Element counter output
1EVEN	Even-numbered field
3FQ	Fourth clock (70-ns clock pulse)
7FQ	Fourth clock (70-ns clock pulse)*
3H*MY	Vertical resolution select bit
4H*MY	Vertical resolution select bit
6HBLANK	Horizontal blanking*
1HBLANKA,B	Horizontal blanking A, B
3HQ	Half clock (35-ns clock pulse)
7HQ	Half clock (35-ns clock pulse)*
8HQ	Half clock (35-ns clock pulse)*
9HQ	Half clock (35-ns clock pulse)*
*IINT	Interrupt request*
8INTLC	Interlace
9INTLC	Interlace*
6IOP	I/O request*
6IOREAD	I/O read*
*IORQ	I/O request*
5KJLSEL1	Configuration select readout 1*
5KJLSEL2	Configuration select readout 2*
3L*MY	Vertical resolution select bit
4L*MY	Vertical resolution select bit
1L1A0-4	Line address bits 0 through 4
6L1D0-9	Line counter data bits 0 through 9*
5LED	Enable LED*
5LLSBCS	Line counter LSB*
5LMSBCS	Line counter MSB*
1LSEL1	Line counter output
*M1	Machine cycle 1*
5M1	Machine cycle 1*
5MREAD	Memory read*
*MREQ	Memory request*
5MREQ	Memory request*
3MY*559	Vertical resolution select bit
4MY*559	Vertical resolution select bit
NTFQ	Fourth clock (70-ns clock pulse)*
NTHQ	Half clock (35-ns clock pulse)*
NTSQ	Sixteenth clock (280-ns clock pulse)*
9PORCLR	Power-on reset*
PSTQ	Sixteenth clock (280-ns clock pulse)
PTFQ	Fourth clock (70-ns clock pulse)
PTHQ	Half clock (35-ns clock pulse)
5RAM10-11	Dual bus address decoder enable*
1RAM1LTH	RAM register latch

Table 4-7. Serial Link PCB Signal Descriptions (Continued)

Mnemonic	Description
5RAM8-9	RAM enable*
5RAMCUR1-4	Enable cursor RAM*
*RD	Read*
5RD	Read*
RD1-8	Serial inputs 1 through 8
*RD1-8	Serial inputs 1 through 8*
8RESET	Reset*
5ROM	ROM enable*
5ROMLS6	ROM LSB*
5ROMMSB	ROM MSB*
SD1-8	Serial outputs 1 through 8
*SD1-8	Serial outputs 1 through 8*
5SELCLK	Selected clock pulse*
5SIOCLK1-8	Baud rate pulses 1 through 8*
5TESTLED	Test LED*
9THBBB	Horizontal blanking timing*
9THMMM	Horizontal memory timing*
9TVBBB	Vertical blanking timing*
8TVFFF	Vertical field timing*
9TVMMM	Vertical memory timing*
1VBLANK	Vertical blanking
8VBSHORT	Load line counter*
VIDLD	Load cursor select data
*WAIT	Wait*
*WR	Write*
5WR	Write*
WRIOP	I/O write
X1-6	Interrupt enable 1 through 6

Table 4-8. Expansion PCB Signal Descriptions

Mnemonic	Description
ADR0-18	Address bits 0 through 18
5AINEN	Port A input enable*
9AIOB0-7	Port A data bits 0 through 7*
9AREADY	Port A ready*
5ASE	Address switch enable*
9ASTROBE	Port A strobe*
9ATN	Attention*
5ATXDAT	Transmit data (J3)*
1BA	Transmit data (J3)
2BA	Transmit data (J4)
5BINEN	Port B input enable*
9BIOB0-7	Port B data bits 0 through 7*
4BMPT	Memory protect
9BREADY	Port B ready*
9BSTROBE	Port B strobe*
4BZADR0-18	Address bits 0 through 18 (processor bus)
9BZBUSY	Busy (processor bus)*
9BZDAT0-7	Data bits 0 through 7 (processor bus)*
BZIEI	Interrupt enable input (processor bus)
BZIEO	Interrupt enable output (processor bus)
9BZINT	Interrupt (processor bus)*
9BZIORQ	I/O request (processor bus)*
9BZM1	Machine cycle 1 (processor bus)*
9BZMREQ	Memory request (processor bus)*
9BZREAD	Read (processor bus)*
9BZRFSH	Refresh (processor bus)*
9BZWAIT	Wait (processor bus)*
9BZWRITE	Write (processor bus)*
1CA	Request to send (J3)
2CA	Request to send (J4)
1CAS	Column-address strobe
6CAS0-7	Column-address strobe 0 through 7
1CD	Data terminal ready (J3)
2CD	Data terminal ready (J4)
2CIE	Buffered clock pulse
3CIE	Buffered clock pulse
CLKZ80	Clock Z80 (280-ns clock pulse)
6CLKZ80	Clock Z80 (280-ns clock pulse)*
CLRSND	Clear to send (J4)
DAT0-7	Data bits 0 through 7
9DAV	Data valid*
DCARDT	Data carrier detect (J4)
9DI01-8	Parallel data bits 1 through 8*
DMARQ	DMA request
DTERRDY	Data terminal ready (J4)
8EIORQ	I/O request (expansion bus)*
8EM1	Machine cycle 1 (expansion bus)*
5EMACTC	Enable math CTC*

Table 4-8. Expansion PCB Signal Descriptions (Continued)

Mnemonic	Description
EMRQ	Memory request (expansion bus)
1EMRQ	Memory request (expansion bus)
2EMRQ	Memory request (expansion bus)
8EMRQ	Memory request (expansion bus)*
5ENBAUD	Enable baud rate generator*
5END	End of ALU operation*
5ENIEDMA	Enable IEEE DMA*
5ENIEEE	Enable IEEE interface*
6ENMATH	Enable ALU*
5ENMRD	Enable memory read*
5ENPAPI1	Enable simplified parallel port interface*
5ENSIO	Enable serial port*
5EOI	End of identity*
9EOI	End of identity*
7EQ	Eighth clock (140-ns clock pulse)*
8ERD	Read (expansion bus)*
8ERFSH	Refresh (expansion bus)*
4EWPT	Write protect (expansion bus)
6EWR	Write protect (expansion bus)*
8EWR	Write (expansion bus)*
7FQ	Fourth clock (70-ns clock pulse)*
5IEEE	IEEE controller interrupt request*
9IFC	Interface clear*
5INT	Interrupt*
5INT	Interrupt*
9NDAC	Data not accepted*
9NRFD	Not ready for data*
NTEQ	Eighth clock (140-ns clock pulse)*
NTF	Fourth clock (70-ns clock pulse)*
NTSQ	Z80 clock (280-ns clock pulse)*
9PORCLR	Power-on reset clear*
5PRECHA	Memory read or write*
5PROM10-17	Select ROMs 10 through 17*
1PSADR11	Supply voltage or address bit 11
2PSADR11	Supply voltage or address bit 11
PTEQ	Eighth clock (140-ns clock pulse)
PTFQ	Fourth clock (70-ns clock pulse)
PTSQ	Z80 clock (280-ns clock pulse)
RAMEN	RAM enable
5RAMEN	RAM enable*
6RAS1-4	Row-address strobe 1 through 4*
5RECDAT	Receive data (J4)*
9REN	Remote enable*
8RESET	Reset*
ROMEN	ROM enable
RQSND	Request to send (J4)
SCLRSND	Clear to send (J3)
SDCARD	Data carrier detect (J3)

Table 4-8. Expansion PCB Signal Descriptions (Continued)

Mnemonic	Description
SDTERRDY	Data terminal ready (J3)
5SERRDYA	Serial data ready A*
5SERRDYB	Serial data ready B*
5SIOCLK1,2	Serial I/O clock 1,2*
5SRECDAT	Receive data (J3)*
9SRQ	Service request*
SRQSND	Request to send (J3)
5TXDAT	Transmit data (J4)*
8WAITMA	ALU wait*
5WCONF	Enable parallel port control*
XB	Interrupt enable
XC	Interrupt enable
XD	Interrupt enable
XE	Interrupt enable
XI	Interrupt enable
XK	Interrupt enable

Table 4-9. Video 1 PCB Signal Descriptions

Mnemonic	Description
BLINK	Blink oscillator
8CURS1-4	Cursor data
#CURS1-4	Cursor data return
2CURS1-4	Cursors
9DSTRCH	Stretch
9DZOOM	Zoom
9DZOOM0	Zoom 0
2ESEL	Select refresh memory data
4H*MX	System resolution
7M0-23	Refresh memory data
NTBQ	Base clock (17.5-ns clock pulse)
NTFQ	Fourth clock (70-ns clock pulse)
NTHQ	Half clock (35-ns clock pulse)
PTBQ	Base clock (17.5-ns clock pulse)
PTFQ	Fourth clock (70-ns clock pulse)
PTHQ	Half clock (35-ns clock pulse)
1TCB8	Composite blanking
2TCB8	Composite blanking
3TCBBB	Composite blanking
8TCBBB	Composite blanking out
9TCBBB	Composite blanking in
3TCSSS	Composite sync
8TCSSS	Composite sync out
9TCSSS	Composite sync in
8THDDD	Horizontal drive out
9THDDD	Horizontal drive in
8TVDDD	Vertical drive out
9TVDDD	Vertical drive in
9TVMMM	Vertical memory in
#VCURS0-11	Video cursors
9VD0-31	Refresh memory data
#VD0-31	Refresh memory data return
VIDOUT0-11	2-bit DAC outputs

Table 4-10. Video 7 PCB Signal Descriptions

Mnemonic	Description
1AD0 0-9	LUT even addresses 0-9
1AD010	LUT even address 10
1AD011	LUT even address 11
1AD1 0-9	LUT odd addresses 0-9
1AD110	LUT odd address 10
5ADR	Address
5ADR	Address
ADRCNTR0-11	Address counter 0-11
1ADRCTR0-11	Address counter 0-11
AJ	24 bit select
9B+10	Blue +10% intensity
4BADR0-7	Address 0-7
9BBUSY	Busy
9BDAT0-15	Display bus
BE0-7	Blue even bits 0-7
9BLANKD	Composite blanking
9BLANKE	Composite blanking
9BLANKG	Blanking
BLINK	Cursor blink
BO0-7	Blue odd bits 0-7
9BREAD	Read
9BSTAT	Status
9BSYSEN	System enable
9BWAIT	Wait
9BWRITE	Write
CDCLK	Data clock
COMP BLANK	Composite blanking
COMP SYNC	Composite sync
9CRMWRT	RAM write
4CS0	Chip select 0
CS0E	Even chip select 0
CS0O	Odd chip select 0
4CS1	Chip select 1
CS1E	Even chip select 1
CS1O	Odd chip select 1
5CURS0-3	Cursor 0-3
#CURS1	Cursor 1 differential input
8CURS1	Cursor 1 differential input
#CURS2	Cursor 2 differential input
8CURS2	Cursor 2 differential input
#CURS3	Cursor 3 differential input
8CURS3	Cursor 3 differential input
#CURS4	Cursor 4 differential input
8CURS4	Cursor 4 differential input
9DACSYNC	Digital-to-analog converter sync
9DSTRETCH	Stretch
9DZOOM	Zoom
9DZOOM0	Zoom 0

Table 4-10. Video 7 PCB Signal Descriptions (Continued)

Mnemonic	Description
EVEN12-18	Even cursor and overlay data 12-18
9G+10	Green +10% intensity
GE0-7	Green even bits 0-7
GO0-7	Green odd bits 0-7
HOR DRIVE	Horizontal drive
INTERLEAVE	Interleave
LTCHEN	Latch enable
9LTCHEN	Latch enable
MEMIN4-24	Memory data in 4-24
MEMOUT0-24	Memory data out 0-24
NTBQ	Negative basic clock frequency
NTFQ	Negative fourth basic clock frequency
NTHQ	Negative half basic clock frequency
ODD12-18	Odd cursor and overlay data 12-18
OV00	Overlay 1
OV01	Overlay 2
OV11	Overlay 3
OVBD	Overlay blue drive
OVBE	Overlay blue enable
OVGD	Overlay green drive
OVRD	Overlay red drive
OVRGE	Overlay red and green enable
PDATAIN0-3	Data in 0-3
PIXEL CLOCK	Pixel clock
9PORCLR	Power reset clear
PTBQ	Positive basic clock frequency
PTFQ	Positive fourth basic clock frequency
PTHQ	Positive half basic clock frequency
9R+10	Red +10% intensity
RE0-7	Red even bits 0-7
RO0-7	Red odd bits 0-7
9TCBBB	Composite blanking
9TCSSS	Composite sync
9THDDD	Horizontal drive
8TVDDD	Vertical drive
9TVDDD	Vertical drive
24/12	24-or 12-bit configuration signal
1VD0-7	Video data 0-7
VERT DRIVE	Vertical drive
5VSTM	State machine
WB0	Blue and green LUT write enable 0
WB1	Blue and green LUT write enable 1
WR0	Red LUT write enable 0
WR1	Red LUT write enable 1

Table 4-11. Video 8 PCB Signal Descriptions

Mnemonic	Description
4BADR0-7	Address bus
9BDAT00-15	Data bits 0-15 (display bus)
BKCKON	Blink
6BL1,2	Blue 1,2 LSB
6BM1,2	Blue 1,2 MSB
9BREAD	Read
BREADY	Ready
9BWAIT	Wait
9BWRT	Write
COMPOSITE BLANKING	Composite blanking output
COMPOSITE SYNC	Composite sync output
6CPL1,2	Hardcopy 1,2 least-significant bit (LSB)
6CPM1,2	Hardcopy 1,2 most-significant bit (MSB)
4CURS1-4	Cursor data
CURS1-4	Cursor data return
2DBLANK	Blanking
DP1CS1E,2E	Display section 1 address counter enable
DP1CT0-10	Display section 1 address counter outputs
5DP1CT10	Display section 1 buffered address counter output
1DP1CURS	Display section 1 cursor
3DP1CURS	Display section 1 cursor intensity
1DP1EVEN	Display section 1 interleave select
5DP1LTCH	Display section 1 VLT output latch
DP1OD0-7	Display section 1 VLT output data
6DP1RWRE	Display section 1 even VLT read/write
6DP1RWRO	Display section 1 odd VLT read/write
DP2CS1E,2E	Display section 2 address counter enable
DP2CT0-10	Display section 2 address counter outputs
5DP2CT10	Display section 2 buffered address counter output
1DP2CURS	Display section 2 cursor
3DP2CURS	Display section 2 cursor intensity
1DP2EVEN	Display section 2 interleave select
5DP2LTCH	Display section 2 VLT output latch
DP2OD0-7	Display section 2 VLT output data
6DP2RWRE	Display section 2 even VLT read/write
6DP2RWRO	Display section 2 odd VLT read/write
9DSTRCH	Stretch
9DZOOM	Zoom
9DZOOM0	Zoom 0
1ECBBB	Composite blanking
1ECSSS	Composite sync
1ESBD0-10	Internal data bus
6GL1,2	Green 1,2 LSB
6GM1,2	Green 1,2 MSB
HIRES	Resolution select
HORIZONTAL DRIVE	Horizontal drive output
NTBQ	Base clock (17.5-ns clock pulse)
NTFQ	Fourth clock (70-ns clock pulse)

Table 4-11. Video 8 PCB Signal Descriptions (Continued)

Mnemonic	Description
NTHQ	Half clock (35-ns clock pulse)
9PORCLR	Power-on reset clear
PTBQ	Base clock (17.5-ns clock pulse)
PTFQ	Fourth clock (70-ns clock pulse)
PTHQ	Half clock (35-ns clock pulse)
6RL1,2	Red 1,2 LSB
6RM1,2	Red 1,2 MSB
9TCBBB	Composite blanking
9TCSSS	Composite sync
6TENBLU1,2	Cursor intensity
6TENGRN1,2	Cursor intensity
6TENRED1,2	Cursor intensity
9THDDD	Horizontal drive
9TVDDD	Vertical drive
9VD0-31	Refresh memory data
#VD0-31	Refresh memory data return
1VD0H-15H	Display section 1 video data (high resolution)
2VD0H-15H	Display section 2 video data (high resolution)
1VD0L-7L	Display section 1 video data (low resolution)
2VD0L-7L	Display section 2 video data (low resolution)
VERTICAL DRIVE	Vertical drive output
VIDBLU1,2	Blue 1,2 output
VIDCPY1,2	Hardcopy 1,2 output
VIDGRN1,2	Green 1,2 output
VIDRED1,2	Red 1,2 output
1VSMUXXE1	Display section 1 VLT address multiplex
1VSMUXE2	Display section 2 VLT address multiplex
5VSTM	Visible time

Table 4-12. Pixel Formatter PCB Signal Descriptions

Mnemonic	Description
4BADR0-7	Address bus
9BBUSY	Busy
9BDAT00-15	Data bits 0-15 (display bus)
9BREAD	Read
BUSY	DMA write in progress
9BWAIT	Wait
9BWRT	Write
C1ZERO	Counter 1 zero
C2ZERO	Counter 2 zero
C3ZERO	Counter 3 zero
DIR	Shift direction
*DMARD	DMA read
*DMAWR	DMA write
*ENP1-3	Enable counters 1-3
ILATCH	Input latch
*LD1-3	Load counters 1-3
NTFQ	Fourth clock (70-ns clock pulse)
OLATCH	Output latch
*POC	Power-on clear
9PORCLR	Power-on reset clear
PTFQ'Fourth clock (70-ns clock pulse)	
SR1A	Shift register control
SR1B	Shift register control
WAIT	DMA read in progress

Table 4-13. Transform PCB Signal Descriptions

Mnemonic	Description
4BADR0-7	Address bus
9BDATA00-15	Data bits 0-15 (display bus)
9BREAD	Read
9BWAIT	Wait
9BWRT	Write
CMAD00-09	Memory address 0-9
9DES ADR CNTR A,B	Destination is address counter A,B
9DES BSYSTEM	Destination is system bus
9DES CLR ADDER CARRY	Destination is adder carry clear
9DES CLR MUL CARRY	Destination is multiply carry clear
1DES CLR STK POINTER	Destination is clear stack pointer
9DES CONTEXT	Destination is context
9DES DEC STK POINTER	Destination is decrement stack pointer
9DES INC ADR CNTR A,B	Destination is increment address counter A,B
9DES INC STK POINTER	Destination is increment stack pointer
9DES MULTIPLY CONTROL	Destination is multiply control
9DES RAM ELEMENT	Destination is RAM element
9DES REG1,2	Destination is register 1,2
9DES STK POINTER	Destination is stack pointer
DES0-7	Destination codes 0-7
2DESX	Destination is X
2DESY0,1	Destination is Y 1,2
8DESY0,1	Destination is Y 1,2
9DONE	Operation done
9IDLE	Idle
9IMM SOURCE	Immediate source buffer enable
MAP BUS0-6	Map PROM bus
NTFQ	Fourth clock (70-ns clock pulse)
NTHQ	Half clock (35-ns clock pulse)
NTMCQ	Memory control clock
NTSQ	Sixteenth clock (280-ns clock pulse)
OV	Overflow
9POR/RESET	Power on reset/reset
9PORCLR	Power-on reset clear
PTFQ	Fourth clock (70-ns clock pulse)
PTHQ	Half clock (35-ns clock pulse)
PTMCQ	Memory control clock
PTSQ	Sixteenth clock (280-ns clock pulse)
RAM DEST	RAM is destination
RAM SOURCE	RAM is source
2REL ADR	Relative addressing
SEL ADR CNTR B	Select address counter B
SOURCE 8	Source bit 8
9SOURCE ADDER	Source is adder
9SOURCE BSYSTEM	Source is system bus
9SOURCE CSP	Source is center significant product
9SOURCE ELEMENT ADR	Source is element address
1SOURCE LSP	Source is least significant product

Table 4-13. Transform PCB Signal Descriptions (Continued)

Mnemonic	Description
9SOURCE LSP	Source is least significant product
9SOURCE MSP	Source is most significant product
9SOURCE REG1,2	Source is register 1,2
9SOURCE STK POINTER	Source is stack pointer
SOURCE0-7	Source codes 0-7
2STACK EMPTY	Stack empty
2STACK FULL	Stack full
TBUS0-15	Transform bus 0-15
UN	Underflow
YIN/LSP OUT0-15	Multiplication bus 0-15

4.4 MINIMUM AND OPTIONAL FUNCTIONAL ELEMENTS

Some 9465 elements will vary according to application. All 9465s will contain the minimum functional elements, but the user may choose a different video PCB and more than one serial link, MCP, memory, or video PCB.

4.4.1 Minimum Functional Elements

The minimum configuration (figure FO4-1) has the following functional elements:

- System processor PCB (Z80) or (MC68000)
- MCP PCB
- Memory PCB
- Video 12 PCB
- Sync PCB
- Backplane Assembly
- Power Distribution System

The system processor PCB controls 9465 operation, decodes instructions from the host, and drives the MCP.

The MCP PCB controls display operations associated with the memory PCB. Screen refresh and memory refresh are carried out under control of this PCB. In addition, the MCP draws primitives such as alphanumerics, graphics, and images and performs clipping, entity detection, pan, and zoom.

The memory PCB incorporates 64K MOS RAMs that store picture information in raster scan, dot matrix format. The memory PCB is available in 4- or 8-plane versions.

The video 12 PCB accepts digital video data from the memory PCB. Analog RGB outputs go to a video monitor and text output goes to a hardcopy device or video monitor. This PCB has two VLTs that store values loaded from the processor. Stored VLT data generates intensity and text attribute values for the DACs when addressed by refresh memory data. Under program control, the system processor PCB can read back and modify data stored in the VLTs. The video 12 PCB is available in two versions: the video 12A has four 2-bit DACs and the video 12B has one 8-bit DAC.

The sync PCB generates 9465 clocks and video timing signals. The 9465 clocks synchronize internal 9465 logic operations. The video timing signals synchronize 9465 logic with the raster scans occurring in the video monitor. This PCB also has a TTL DMA sequencer, reset logic for the 9465, a cursor pattern generator (one cursor), and terminations for the memory timing signals.

The backplane assembly distributes power and signals between PCBs and terminates 9465 clocks. Although the backplane assembly has no active electronic components, this hardware is considered a logical functional element of the 9465.

The power distribution system routes ac power to the power supply and fans, and dc power to the backplane assembly. Elements include fuse F1, line filter LF1, circuit breaker CB1, the power supply, and wiring harnesses.

4.4.2 Optional Functional Elements

Optional functional elements include:

- Serial link PCB
- Expansion PCB
- Video 1 PCB
- Video 7 PCB
- Video 8 PCB
- Video load PCB
- Pixel formatter PCB
- Transform PCB

The serial link PCB processes operator input from serial transmission peripheral devices and has a cursor generator that can generate four cursors. This PCB supports up to eight peripheral devices.

The expansion PCB can add high speed mathematic logic, additional PROM space, and additional RAM to the system processor PCB. High speed mathematic operations include fixed and floating point arithmetic and trigonometric functions. When configured, the expansion PCB works in conjunction with the system processor PCB during coordinate transformation processing.

The video PCBs provide a mix of capabilities and are chosen according to customer application. The video 1 PCB has twelve 2-bit DACs and can drive up to 12 monochrome or four color monitors. The video 7 PCB is available in two configurations: the 7A, which has three 4-bit DACs, and the 7B, which has three 8-bit DACs. The video 7 can drive one color monitor. The video 8 PCB has eight 2-bit DACs and can drive two color monitors and two hardcopy devices.

The video load PCB is required in some 9465 configurations to maintain specified voltage regulation. This PCB has voltage-dropping resistors only.

The pixel formatter speeds data transfer between the host computer and the 9465. With a pixel formatter PCB installed, received image data in a multiple-pixel-per-word format is converted to a single-pixel-per-word format. For example, a single 16-bit word might contain three 5-bit pixels, four 4-bit pixels, five 3-bit pixels, or eight 2-bit pixels. The pixel formatter puts each pixel into a separate 16-bit word.

The transform PCB acts as an internal 9465 peripheral. When this PCB is installed, the system processor PCB routes coordinate transformation or matrix operations to the transform PCB. In this way, the system processor PCB and the MCP PCB can continue to operate during coordinate transformation processing. Transformations include rotate, translate, and scale.

4.5 FUNCTIONAL DESCRIPTIONS

Detailed functional descriptions for all 9465 functional elements are contained in following paragraphs. Each PCB is divided into functional elements and each element is then analyzed in relation to overall PCB operation. Each discussion concludes with a description of the processes which occur.

4.5.1 System Processor PCB (Z80)

This PCB incorporates a Zilog Z80A-CPU microprocessor (Z80) which functions as a central processing unit (CPU) and controls system processor PCB operation. Interfaces include the host computer, 9465 PCBs, and, optionally, a keyboard and joystick. The system processor PCB decodes instructions from the host computer, stores sub-pictures (display lists), stores application programs, stores character elements, performs coordinate transformations (with the expansion PCB), drives the MCP PCB, and controls 9465 configuration.

4.5.1.a Buses. System processor buses (figure FO4-2) include data, address, and control. Data bus buffers are bidirectional. Address and control bus drivers are unidirectional. Bus buffers or drivers supply drive for functional elements served by the buses. The processor data bus buffer converts 16-bit words into 8-bit bytes in one direction, and converts 8-bit bytes into 16-bit words in the other direction.

The processor address bus driver supplies drive for devices connected to the processor address bus. The driver converts MOS address bus bits A0-11 into processor address bus bits 4BZADR0-11.

4.5.1.b Functional Elements. The system processor PCB (Z80) has the following discrete functional elements:

- CPU
- Processor and supervisor wait logic
- Supervisor call logic
- Reset driver
- Real time controller
- Blanking interrupt controller
- Serial peripheral I/O controller
- Clock driver
- MOS data bus buffer
- MOS control bus buffer
- Processor bus address decoder
- Memory allocation and protection (MAP) unit
- Refresh generator
- RAM and ROM
- Memory data driver
- I/O address decoder
- Data bus driver control logic
- Display data bus driver
- Processor data bus driver
- Display bus tester-controller
- Display address bus driver
- Configuration RAM

- Baud rate generator
- Self-test logic
- Display control bus driver
- Display bus address decoder
- System selector
- Host status controller
- LED logic
- Serial host I/O controller
- Serial interface controller
- Interface data bus buffer
- Processor status register
- Status driver
- Display bus wait logic
- Configuration selector
- Host control logic
- MAP unit
- Daisy chain interrupt logic

Three additional elements are not used:

- Cycle-steal DMA
- DMA ready logic
- Display bus interrupt controller

4.5.1.b.1 CPU. The CPU (figure F04-2) is a Z80A-CPU with supporting logic. Refer to chapter 1, "Related Documents," for manufacturer's manual. The CPU receives clock pulse 2CLKZ80 and five control signals, and generates 16 address bits and 11 control signals. Data bus lines D0-D7 are bidirectional.

The three CPU operations are memory read or write, input or output device read or write, and interrupt acknowledge. All operations are a combination of these three. A typical operation consists of three machine cycles. Cycle M1 is always the fetch cycle, which fetches the operation code of the next instruction the CPU will execute. Cycles M2 and M3 transmit data between the CPU and memory or I/O devices.

The address and data outputs and control signals *MREQ, *IORQ, *RD, and *WR are tri-state outputs. When neither active nor inactive, these outputs assume a high impedance state. Signal *MREQ is active during a memory read or write cycle; *IORQ is active during a read or write cycle with an I/O device. Signal *RD goes active when the CPU attempts to receive data; *WR goes active when the CPU transmits data. Signal *RFSH is active during a memory refresh operation. Signal *WAIT delays CPU operation while another device completes an operation. Signal *IINT is a request from another device for CPU access. Signal *M1 is active during an M1 cycle; *M1 and *IORQ go active together to indicate an interrupt acknowledge. Signal INTA and 5INTA go active when *M1 and *IORQ go active. Signal *IBUSRQ from another device requests control of the bus connected to the tri-state outputs. When the current machine cycle is complete, the CPU sets the tri-state outputs to a high impedance state and transmits bus acknowledge signals *BUSAK and 2BUSAK. The requesting device can then take control of the bus. Signal *M1RES goes active when either *M1 or 9RESET1 goes active.

4.5.1.b.2 Processor and supervisor wait logic. The processor wait logic generates *WAIT, which goes to the CPU and the refresh generator. Signal *WAIT goes active when 9BZWAIT goes active or when 9BWAIT and 1ENADR go active.

The supervisor wait logic generates *WAIT when 5SVC goes active. Signal *WAIT remains active until the third CLKZ80 clock pulse after 5SVC goes active.

4.5.1.b.3 Supervisor call logic. The supervisor call logic receives 5SVC and clock pulse 7EQ, and sends 8SVC to the real time controller. Signal 8SVC goes active at the first 7EQ pulse after 5SVC goes active, and remains active until the next 7EQ pulse.

4.5.1.b.4 Reset driver. This driver supplies reset drive for system processor PCB devices. The driver converts 9PORCLR from the sync PCB into 9RESET and 9RESET1.

4.5.1.b.5 Real time controller. This controller generates interrupt signals and real time (time-of-day) clock data. The controller has four channels that can function as counters or timers. Address bits A0 and A1 select one channel for a read or write operation. Signal 6ENMCTC enables the controller. Signal 8SVC triggers channel 0, BAUDCLK triggers channel 3, and BD3 triggers channel 2. Channels 2 and 1 are connected in cascade to generate real time clock data. When 8SVC goes active, the controller sends *IINT to the CPU. The CPU signals an interrupt acknowledge by setting *IORQ and *M1 active. The controller responds by sending a vector to the CPU on D0-7. This vector identifies real time controller channel 0 as the interrupt source. The CPU responds by switching the MAP unit from user mode to system mode.

Channels 2 and 1 count BD3 baud rate pulses and generate real time data in years, months, days, hours, minutes, and seconds. Channel 2 also generates a *IINT pulse every 100 milliseconds. The CPU can read time by sending *IORQ, *RD, and 6ENMCTC, and addressing channels 2 and 1. The controller responds by sending real time data on D0-7.

The CPU can program controller interrupts. After a specified number of BAUDCLK pulses, the CPU sends a control byte that selects counter mode, followed by a time constant byte that specifies the number of counts. When the CPU addresses channel 3, 6ENMCTC and *IORQ successively load two bytes into the controller on D0-7. The controller then counts BAUDCLK pulses, decrementing the specified count until the count reaches zero. Signal *IINT then goes active, and the count begins again. This sequence continues until the CPU reprograms the controller. Clock pulse 2CLKZ80 synchronizes controller operations. Signal XB is inactive when the controller is busy. Signal 9RESET resets the controller.

4.5.1.b.6 Blanking interrupt controller. The blanking interrupt controller receives horizontal blanking signal 9THBBB and vertical blanking signal 9TVBBB from the sync PCB. When either signal goes active, the controller sends *IINT to the CPU.

4.5.1.b.7 Serial peripheral I/O controller. This controller optionally interfaces with a keyboard and a joystick. Signal 5ENSIO enables the controller. Address bit A1 goes active to select the joystick, and inactive to

select the keyboard. Address bit A0 goes active when a control byte is on D0-7, and inactive when a data byte is on the bus. When the keyboard sends serial data on RD1 and *RD1, the controller sends interrupt request signal *IINT to the CPU. The CPU signals an interrupt acknowledge by setting *IORQ and *M1 active. Then, the controller sends an interrupt vector to the CPU on D0-7; this interrupt vector identifies the interrupt source. The CPU then sends *IORQ, *RD, and 5ENKSIO, and the controller converts the serial data to parallel form and transmits the parallel data on D0-7.

When the CPU has instructions for the keyboard, *IORQ and 5ENSIO go active and the controller performs a parallel to serial conversion. Serial instructions go to the keyboard on SD1 and *SD1. Joystick data is transferred in a similar manner except bit A1 selects the joystick. Baud rate pulses 5SIOCLK3 and 5SIOCLK4 clock keyboard and joystick data transfers, respectively. Clock pulse 2CLKZ80 synchronizes controller operations. Outputs 5SERKJA and 5SERKJB are not used. Signal 9RESET resets the controller.

4.5.1.b.8 Clock driver. This element supplies clock pulse drive for system processor PCB devices. The driver receives three pairs of differential clock pulse inputs, and supplies eight clock pulse outputs.

4.5.1.b.9 MOS data bus buffer. The MOS data bus buffer normally buffers MOS data bus bits D0-7 to become processor data bus bits 9BZDAT0-7. But the buffer reverses data flow if either of these conditions is true: 8RD and 8ADRP are active or 5BZIE0 and 5INTA are active. Signal 8RD is active when the CPU is receiving data; 8ADRP goes active when a device on the processor bus or display bus has data to send. Signal 5BZIE0 remains active as long as no device on the MOS bus generates an interrupt request ; 5INTA goes active when the CPU generates an interrupt acknowledge, which must be a response to an interrupt request from a device not on the MOS bus since 5BZIE0 is active.

4.5.1.b.10 MOS control bus buffer. This buffer (figure FO4-2) supplies drive for the central and processor control buses. The buffer converts six MOS control bus signals and 8RFEN into six central control bus signals and six processor control bus signals.

4.5.1.b.11 Processor bus address decoder. Signal 8IORQ enables this element, which decodes address bits 4BZADR0-7 and 8WR and 8RD to derive 21 control outputs. The decoder also inverts 8M1 to become 1M1. When 8M1 is inactive, the decoder inverts 8IORQ to become IOP. Signal 8M1 inhibits the decoder. Signal GOUSER inhibits outputs 5WRMD, 5WRCRD, 6ENBAUD, and 6ENMCTC.

4.5.1.b.12 MAP unit. The MAP unit is functionally described in a following detailed functional description paragraph.

4.5.1.b.13 Refresh generator. When *WAIT and *BUSAK are active, the refresh generator counts CLKZ80 clock pulses. When 8RFSH is active, the generator activates RFEN and 8RFEN at count 40. At the first 7FQ1 clock pulse after count 40, the generator activates 5RFSRAS. Signal *WAIT is active when another device is busy, and *BUSAK is active when the CPU has relinquished control of the bus. These are times when a refresh cycle does not interfere with read or write cycles.

4.5.1.b.14 RAM and ROM. RAM consists of sixteen 16K x 1-bit RAM ICs. The second 7FQ clock pulse, after 8MREQ goes active, enables RAM. During a write cycle, 8MREQ and 8WR go active, and RAM stores data received on 9BZDAT0-7 in the location specified by address bits 4BZADR0-18. Signal 4BMPT prevents loss of stored data by inhibiting the write cycle. During a read cycle 8 MREQ goes active, and RAM transmits data stored in the addressed location on memory data *MD0-7. The second CLKZ80 clock pulse after 1M1 goes active inhibits RAM operation. When 8MREQ goes active, RAM decodes address bits 4BZADR14-18 to derive 5MADR5 and 5MADR6. RAM is a dynamic memory and must be refreshed every two milliseconds to prevent loss of stored data. During a refresh cycle, 8RFSH, RFEN, and 5RFSRAS refresh the RAM chips.

ROM consists of up to sixteen 2K x 8-bit PROM chips. ROM receives address bits on 4BZADR0-18. Signals 5ENMRD and 8MREQ enable ROM, which transmits data stored in addressed locations on memory data *MD0-7. Signal RFEN inhibits ROM operation. ROM decodes address bits 4BZADR14-18 to derive output signals 6MADR1 and 6MADR2. When 8M1, 8MREQ, and either 6MADR1 or 6MADR2 go active, ROM generates *WAIT at the next CLKZ80 clock pulse. Signal *WAIT remains active until the following CLKZ80 pulse.

4.5.1.b.15 Memory data driver. This driver (figure F04-2) supplies drive for devices that connect to the processor data bus. After 8MREQ and one of signals 5MADR5, 5MADR6, 6MADR1, or 6MADR2 go active, the second 7FQ clock pulse after 8RD goes active enables the driver. Signal 5ENMRD goes active and the driver transfers data on *MD0-7 to 9BZDAT0-7.

4.5.1.b.16 I/O address decoder. Signal 8IORQ enables this decoder, which accepts address bits 4BZADR0-7 and derives control signals 8ADRP, 5LDMU, and 5SYSADR. Signal 1M1 inhibits the decoder.

4.5.1.b.17 Data bus driver control logic. This logic receives five control signals and three clock pulses, and generates seven control outputs. Signal 9RESET1 resets the logic. After reset, 8RD goes active. With 8RD active, 5LORD goes active on the next 5SYSADR pulse. The sequence continues with 5HIRD going active on the next 5SYSADR pulse. After 8WR goes active, 5LOWR goes active (at the next 5SYSADR pulse) followed by 5HIWR going active on the following 5SYSADR pulse. Signal 6LORD goes active when 5LORD and 5ENDAT go active. Signal 5CLKHIRD goes active at the first CLKZ80 clock pulse after 6LORD goes active. Signal 6HIWR goes active when 5HIWR and 5ENDAT go active. Clock pulses 7EQ and 7EQ1 control output timing. Pulse 5SYSADR goes active each time a device connected to the display data bus sends or receives data.

4.5.1.b.18 Display data bus driver. This driver supplies drive for devices served by the display data bus. The driver converts two successive 8-bit processor-data-bus bytes into one 16-bit display-data-bus word. The trailing edge of pulse 5LOWR loads the first byte received on 9BZDAT0-7 into the driver for temporary storage. When 6HIWR subsequently goes active, the driver simultaneously transmits the stored byte on 9BDAT0-7 and transfers the second byte received on 9BZDAT0-7 to 9BDAT8-15.

4.5.1.b.19 Processor data bus driver. This driver supplies drive for devices served by the processor data bus. The driver converts a 16-bit display-data-bus word into two successive 8-bit processor-data-bus bytes. When pulse 6LORD

goes active, the driver transfers the 8-bit byte received on 9BDAT0-7 to 9BZDAT0-7. At the next CLKZ80 pulse, 5CLKHIRD loads the 8-bit byte received on 9BDAT8-15 into the driver. When 5HIRD subsequently goes active, the driver transmits the stored byte on 9BZDAT0-7.

4.5.1.b.20 Display bus tester-controller. This controller sequentially tests display bus conditions and generates signals that reflect test results. Signal 9RESET resets the controller. When a device connected to the display bus transfers data to or from the CPU, RWZ80 goes active and inhibits the controller. When the transfer is complete and RWZ80 goes inactive, the controller monitors 5LORD and 5HIWR at the next 3EQ clock pulse. When the CPU attempts to transfer data, either 5LORD or 5HIWR goes active, and the controller begins a test sequence by activating *WAIT at the next 7EQ clock pulse. The controller then monitors BAKIN, 9BBUSY, and 9BREQ. If 9BBUSY or 9BREQ is active or if BAKIN is inactive, the controller continues to monitor the signals until 9BBUSY and 9BREQ are inactive and BAKIN is active. The controller then generates 9BREQ at the next 7EQ pulse and monitors 9BBUSY. After 9BBUSY goes inactive, meaning no other device is using the display bus, the controller generates 9BBUSY at the next 7EQ pulse followed by 1ENADR and 5ENDAT, then 1ENCONTL. Two 7EQ pulses later, BAKOUT goes active if BAKIN is active; all other outputs go inactive. The entire sequence then repeats.

4.5.1.b.21 Display address bus driver. This driver supplies drive for devices served by display address bus. When 1ENADR and 5ENADR go active, the driver transfers address bytes received on 4BZADR0-7 to 4BADR0-7.

4.5.1.b.22 Configuration RAM. Configuration RAM consists of a static RAM IC and supporting logic. Signal 5LDBBUA latches address data received on 9BZDAT0-7 into the RAM. When 5WRCRD goes active, the RAM stores configuration data received on 9BZDAT0-3 into locations specified by the latched data. When 5RDCRD goes active, the RAM transmits stored data on 9BZDAT0-7.

4.5.1.b.23 Baud rate generator. This generator has a crystal-controlled oscillator that provides the basic 2.4576-MHz signal. Signals 8WR and 6ENBAUD load the generator with data received on 9BZDAT0-3 in locations specified by address bits 4BZADR0 and 1. Subsequently, the generator supplies baud rate pulses 5SIOCLK1, 3, and 4 and BAUDCLK in accordance with data received, and supplies fixed baud rate pulse BD3.

4.5.1.b.24 Self-test logic. This element consists of the self-test register and the self-test LED. When 9RESET1 goes active, the register activates SELFTST and inactivates LEDOFF. This turns on the LED. When data bit 9BZDAT0 goes active followed by 5LDST, SEFLTST goes inactive, LEDOFF goes active, and the LED goes off.

4.5.1.b.25 Display control bus driver. This driver (figure FO4-2) supplies control signal drive. When 1ENCONTL and IOP go active, the driver converts 8IORQ, 8RD, and 8WR into 9BIORQ, 9BREAD, and 9BWRT, respectively.

4.5.1.b.26 Display bus address decoder. Signal 9BIORQ enables the display bus address decoder, which decodes address bits 4BADR0-7 and signals 9BWRT and 9BREAD to derive eight control outputs.

4.5.1.b.27 System selector. This element generates SELECT. Signal 7IFSTAT latches data bits 9BDAT13-15 into the selector, which decodes the latched bits to derive SELECT. The latched bits and SELECT are always active.

4.5.1.b.28 Host status controller. This controller sends host status to the CPU. Signal 5ENPPIO enables the controller. Clock pulse 3EQ latches host status signals ROD, IOWDAT, and IOCMD1 into the controller. When 5ENPPIO, *IORQ and *RD subsequently go active, the controller transfers ROD, IOWDAT, IOCMD1, WRTZ80 and RDZ80 to data bus lines D0, 1, 2, 4, and 5, which go to the CPU. Also, the controller inverts 9DMADONE from the sync PCB, and transfers the inverted signal to line D3. When 5ENPPIO and *IORQ go active and *RD remains inactive, the controller converts bit D7 from the CPU into INTHOST. Either 9RESET1 or SIFRDY clears the latched signals. Signal *M1RES inhibits the controller. Address bits A0 and A1 do not affect operation. Clock pulse 2CLKZ80 synchronizes controller operations.

4.5.1.b.29 LED logic. This element consists of the LED register and the eight status LEDs. When 7WLED goes active, the register transfers status data received on 9BZDAT0-7 to 1E1-8, which drive the eight LEDs.

4.5.1.b.30 Serial host I/O controller. This controller interfaces with a serial host computer and serves only test purposes. The controller has two sections, A and B, corresponding to I/O ports A and B. Signal 5ENHSIO enables the controller. Address bit A1 goes active to select section B, and inactive to select section A. Bit A0 goes active when a control byte is on D0-7, and inactive when a data byte is on the bus. Signal SDCARDET goes active when a host computer connected to port A has serial data to send. If XH is active, the controller sends interrupt request signal *IINT to the CPU. The CPU acknowledges an interrupt by setting *IORQ and *M1 active. In return, the controller sends CD to the host computer, which responds by sending serial data on line SSB. The controller also sends an interrupt vector to the CPU on D0-7. This vector identifies the interrupt source. As the sequence continues, the CPU sends *IORQ, *RD, and 5ENHSIO. Finally, the controller converts serial data to parallel data and sends parallel data to the CPU on D0-7. Data transfer from the CPU to the serial host computer at port A begins with the CPU setting *IORQ and 5ENSIO active and the controller sending SCA to the host computer. The host computer responds with SCLRSEND and, after converting parallel to serial, sends serial data to the host computer on SBA.

Data transfer is similar for a host computer at port B except that DCARDET, 5RECDAT, CA, CLRSEND, and BA replace SDCARDET, SSB, SCA, SCLRSEND, and SBA, respectively, and bit A1 selects section B. Signal CD is common to both ports. Baud rate pulse 5SIOCLK1 clocks serial data transfers. Clock pulse 2CLKZ80 synchronizes controller operations. Signal 9RESET resets the controller. Signals 5SERHA and 5SERHB are unused. The controller inverts SSB to become SRECDAT which goes to the serial interface controller.

4.5.1.b.31 Serial interface controller. This controller serves a test function. The controller sends control signals from the serial host computer to the CPU. Signal 5ENSPIO and address bit A1 enable the controller. When the host computer sends control signal CC or CE or serial data on SRECDAT and 5SRECDAT, the controller sends interrupt request signal *IINT to the CPU. When the CPU signals an interrupt acknowledge by setting *IORQ and *M1RES

active, the controller sends an interrupt vector to the CPU on D0-7, identifying the interrupt source. The CPU then sends *IORQ, *RD, 5ENSPIO, and bit A1, and the controller sends the received signals from the host computer to the CPU on D0-7. The CPU interprets the serial data for control purposes. Signal 5ENSPIO enables the controller which has two sections: A and B. Bit A1 selects section B. Section A is not used. Clock pulse 2CLKZ80 synchronizes controller operations.

4.5.1.b.32 Interface data bus buffer. This bidirectional buffer (figure F04-2) transfers data between the interface bus and the display bus and supplies latched data in both directions. Signal IOWDAT latches data received on 9IBOBIT0-15 into the buffer. When 7RDIFDAT subsequently goes active, the buffer transmits the data on 9BDAT0-15. Signal 7WRIRDAT latches data received on 9BDAT0-15 into the buffer. When 1IOREAD subsequently goes active and 7IOCMD remains inactive, the buffer transmits the data on 9IOBIT0-15.

4.5.1.b.33 Processor status register. This register receives interrupts on the display data bus and sends interrupts to the status driver. The register also sends interrupts to the optional interface PCB as 9IINT0, 1, 4, and 5. After 7IFSTAT goes active, the next 7EQ clock pulse clocks data received on 9BDAT0, 1, 4, and 5 into the register. The data remains latched in until cleared. Signal 1CLINT is normally active. After 7CLINT goes active, then inactive, 1CLINT goes inactive and the next 7EQ pulse clears the register.

4.5.1.b.34 Status driver. This driver receives status on the display bus. In addition, the driver receives signals 9IINT0, 9IINT1, 9IINT4, 9IINT5, and 5IOREADY. The driver sends status to the host computer on the interface data bus. Signal 7IFSTAT latches data received on 9BDAT8-15. When 1IOREAD and IOCMD subsequently go active, the driver transfers the received signals to 9IOBIT0-15, which go to the host computer.

4.5.1.b.35 Display bus wait logic. This logic generates 9BWAIT, which delays CPU operation while another device is using the display bus. When another device sends data to the system processor PCB, RDZ80 goes active, making 9BWAIT active. When the CPU reads the data, 5HIRD goes active, making 9BWAIT inactive. If another device attempts to read data from the CPU, WRTZ80 goes active, making 9BWAIT active. When the CPU sends the data, 6HIWR goes active, making 9WAIT inactive. When the CPU or another device attempts to transfer data to or from the host computer (7RDWIFD active) while the host computer is sending (5IOREADY active) or receiving data (5IORD active), 9BWAIT also goes active.

4.5.1.b.36 Configuration selector. The configuration selector consists of configuration switches SW1, SW2, and the configuration driver. When 5ENCFS1 or 5ENCFS2 goes active, the driver transfers 5S10-17 or 5S20-27, respectively, from the switches to 9BZDAT0-7.

4.5.1.b.37 Host control logic. A detailed description of host control logic follows.

4.5.1.c Detailed Functional Descriptions. Host control logic, MAP unit logic, and daisy chain interrupt logic are discussed in detail. Host control logic monitors and controls data transfer between the 9465 and the host

computer. The MAP unit expands memory addressing from 64K memory locations to 512K memory locations by generating three additional address bits. Daisy chain interrupt logic arbitrates contention between devices seeking access to the CPU.

4.5.1.c.1 Host control logic. This logic (figure FO4-3) has eight functional elements:

- Host clear logic
- Host write logic
- Host command logic
- Host read logic
- Interface ready logic
- I/O ready logic
- Clear status logic
- I/O interrupt logic

4.5.1.c.1.a Host clear logic. This logic generates 9BRESCLR when either 9IOPCLR goes active or 9IOBIT15 and IOCMD1 go active.

4.5.1.c.1.b Host write logic. This logic generates IOWRT and IOWDAT. Both signals go active at the first 7EQ clock pulse after 9IOWRITE from the host computer goes active. Signal IOWDAT remains active for one 7EQ pulse. Signal IOWRT remains active until the first 7EQ pulse after 9IOWRITE goes inactive.

4.5.1.c.1.c Host command logic. This logic generates IOCMD, IOCMD1, and 7IOCMD. Signals IOCMD and 7IOCMD go active at the first 7EQ clock pulse after 9IOCMD from the host computer goes active. When IOWRT subsequently goes active, IOCMD1 goes active.

4.5.1.c.1.d Host read logic. This logic generates 1IOREAD, 5IORD, ROD, and RDTLE. Signal 1IOREAD goes active when 9IOREAD from the host computer goes active. Signal 5IORD goes active at the second 7EQ clock pulse after 9IOREAD goes active. In soft interface 9465s RDTLE goes active at the first 7EQ pulse after 9IOREAD goes inactive and remains active for one 7EQ pulse. In hard interface 9465s RDTLE is normally active and goes inactive at the first 7EQ pulse after 9IOREAD goes active. Then, RDTLE goes active again at the following 7EQ pulse. Signal SELECT is always active.

4.5.1.c.1.e Interface ready logic. This logic generates SIFRDY and 2SIFRDY. Both signals go active when 7RDWIFD and 6RESETH from the sync PCB go active. Signal SIFRDY also goes active when 7IFSTAT and 9BDAT6 go active.

4.5.1.c.1.f I/O ready logic. This logic generates 9IOREADY and 5IOREADY. In soft interface systems 9IOREADY and 5IOREADY go active at the fourth 7EQ clock pulse after SIFRDY goes inactive, and remain active until the first 7EQ pulse after either IOWDAT or ROD goes active. In hard interface systems 9IOREADY goes inactive when 5IOREADY goes inactive. Signal SELECT is always active.

4.5.1.c.1.g Clear status logic. This logic generates 5CLINT, 1CLINT, and 7CLINT. Signal 5CLINT goes active when either 9CLSTAT goes active or IOCMD and RDTLE go active. Signal 7CLINT goes active at the second 7EQ clock pulse after either 5CLINT or 9RESET1 goes active. Signal 1CLINT is normally active

and goes inactive at the second 7EQ pulse after 9RESET1 goes active, then goes active again at the following 7EQ pulse. Signal 1CLINT also goes inactive at the first 7EQ pulse after 5CLINT goes inactive. At the following 7EQ pulse 1CLINT goes active again.

4.5.1.c.1.h I/O interrupt logic. This logic generates 9IOINT which goes to the host computer. Signal 9IOINT goes active at the first 7EQ clock pulse after either 2SIFRDY and INTHOST go active or 7IFSTAT and 9BDAT7 go active. Signal 9IOINT remains active until the first 7EQ pulse after 5CLINT goes active.

4.5.1.c.2 MAP unit. The MAP unit (figure FO4-4) expands CPU addressing capability by providing three additional address bits. The MAP unit has nine functional elements:

- MAP sequencer
- MAP multiplexer
- MAP RAM
- MAP address selector
- MAP enable flip-flop
- Mode select logic
- Write pulse generator
- MAP status register
- MAP readback register

Signal ENMAP enables the MAP sequencer. Following receipt of 8WR 8IORQ, and 5LDMU followed by three 8M1 pulses, the sequencer generates signal GOUSER at the next 7EQ clock pulse. Signal GOUSER remains active until the sequencer receives 5LDMU and 8WR followed by two more 8WR pulses. Signal GOUSER then goes inactive at the next 7EQ clock pulse. Signal 1BUSAK interrupts sequencer operation. Output 5ENMAP is GOUSER inverted. Signal 5LDMA loads data received on 9BZDAT0, 1, and 4-7 into the MAP multiplexer, which inverts bits 9BZDAT0 and 4-7 to become BZDAT0 and 4-7. When 5SELMD is inactive, the multiplexer transfers address bits received on MOS address bus lines A12-15, and signals GOUSER and *BUSAK to MAPA0-4 and 5MAPS, respectively. When 5SELMD is active, the multiplexer transfers data bits BZDAT4-7 and 0 and 9BZDAT1 to MAPA0-4 and 5MAPS, respectively.

The MAP RAM has three sections: the DMA, user, and system sections. Each section consists of two 64 x 4-bit RAM chips. The DMA section is not used. Signal 6USER enables the user section. Signal 6SYST enables the system section. Signal 5MAPS enables the DMA section. During a write cycle, 8WRMD goes active and the section selected by 6USER or 6SYST stores data received on 9BZDAT0-7 in the locations specified by address bits MAPA0-3. When 8WRMD is inactive, the selected section transmits, on MAP12-18 and MEPROT, data stored in the locations specified by address bits MAPA0-3.

The CPU checks the MAP unit each time the 9465 is turned on. When power is first turned on, 5ENMAP is inactive. The MAP address selector transfers address bits received on MOS address bus lines A12, A13, and A14 to 4BZADR12, 13, and 14; transmits the address bit received on A15 to 4BZADR16, 17, and 18;

and sets bit 4BZADR15 and signal 4BMPT inactive. After the CPU checks the MAP unit, 5ENMAP goes active, and the selector transfers data received on MAP12-18 and MEPROT to 4BZADR12-18 and 4BMPT, respectively.

After 5LDST goes active, a transition to inactive clocks the MAP enable flip-flop. After bit 9BZDAT1 goes active, ENMAP and 5ENMAP go active at the next clock pulse. Signal 9RESET resets the flip-flop.

The mode select logic generates 6SYST and 6USER. When MAPA4 and 5MAPS are inactive, 6SYST goes active. When MAPA4 goes active with 5MAPS inactive, 6USER goes active. When 5MAPS goes active, 6SYST and 6USER go inactive. The write pulse generator generates write pulse 8WRMD at the first CLKZ80 clock pulse after 5WRMD goes active. Pulse 8WRMD remains active until the following CLKZ80 pulse.

The MAP status register informs the CPU of MAP unit status. Signal 5RDMS enables the register. When INTA subsequently goes active, the register transfers 5ENMAP to line 9BZDAT0.

The MAP readback register allows the CPU to read the address data stored in the MAP RAM. Signal 5RDMD enables the register, which inverts address data received on MAP12-18 and MEPROT, and transfers the inverted data to 9BZDAT0-7, respectively.

4.5.1.c.3 Daisy chain interrupt logic. When two or more devices need to communicate with the CPU simultaneously, 99e daisy chain interrupt logic determines which device gets priority. The devices are connected in a daisy chain (figure F04-5). The real time controller gets top priority. Each of the other devices receives an interrupt enable input and generates an interrupt enable output. The serial peripheral I/O controller, for example, receives XE and generates XF. As long as XE remains active, the controller can send interrupt request *IINT to the CPU. But XE goes active when a higher priority device interrupts the CPU. This prevents the controller from activating *IINT while the higher priority device is busy. When the controller activates *IINT, XF goes inactive. Gate 2 activates XK when XE and XF are active. When XF goes inactive, XK goes inactive. This prevents the serial interface controller from sending an interrupt request. Also, XL, XH, XI, XN, XO, XP, XQ, XU, XV, 5BZIEO and BZIEO go inactive, preventing four other devices from sending interrupts. Signal BZIEO goes out on the processor bus to extend the daisy chain to devices on other PCBs. Such devices can only interrupt the CPU when BZIEO is active. Signal 5BZIEO goes to the MOS data bus buffer to control data flow when a device is busy.

4.5.1.d Process Descriptions. Typical PCB processes are host data flow and keyboard data flow. The 9465 is usually configured with a serial link PCB, but keyboard data flow is discussed for 9465s with or without a serial link PCB.

4.5.1.d.1 Host data flow. In a typical operation the system processor PCB receives data from the host computer and sends processed data to the MCP for display on the monitor. A typical operation consists of these steps:

- 9465 status readout
- Host data input
- Status read control
- Host status readout
- Data bus control
- Display bus test
- Data read control
- Host data transfer
- MAP unit control
- Data storage
- RAM access
- RAM output
- ROM access
- ROM output
- Data output

4.5.1.d.1.a 9465 status readout. The host computer receives 9IOREADY when the 9465 is ready to receive data. If 9IOREADY is active, and the host has data to send, the host first reads 9465 status by activating 9IOREAD and 9IOCMD (figure 4-2). The host read logic inverts 9IOREAD to become 1IOREAD and the host command logic inverts 9IOCMD to become IOCMD at the next 7EQ clock pulse. When 1IOREAD and IOCMD go active, the status driver converts 5IOREADY into 9IOBIT6 which signals the host that the 9465 is ready.

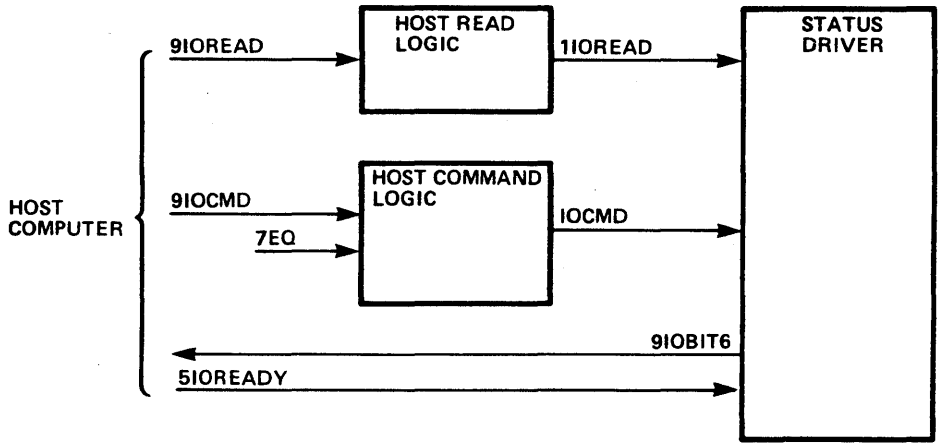


Figure 4-2. 9465 Status Readout

4.5.1.d.1.b Host data input. With the 9640 ready, the host sends data on 9IOBIT0-15 (figure 4-3) and sets 9IOWRT active. The host write logic inverts 9IOWRT to become IOWDAT at the next 7EQ clock pulse. Signal IOWDAT latches

received data into the interface data bus buffer. The next 3EQ clock pulse latches IOWDAT into the host status controller.

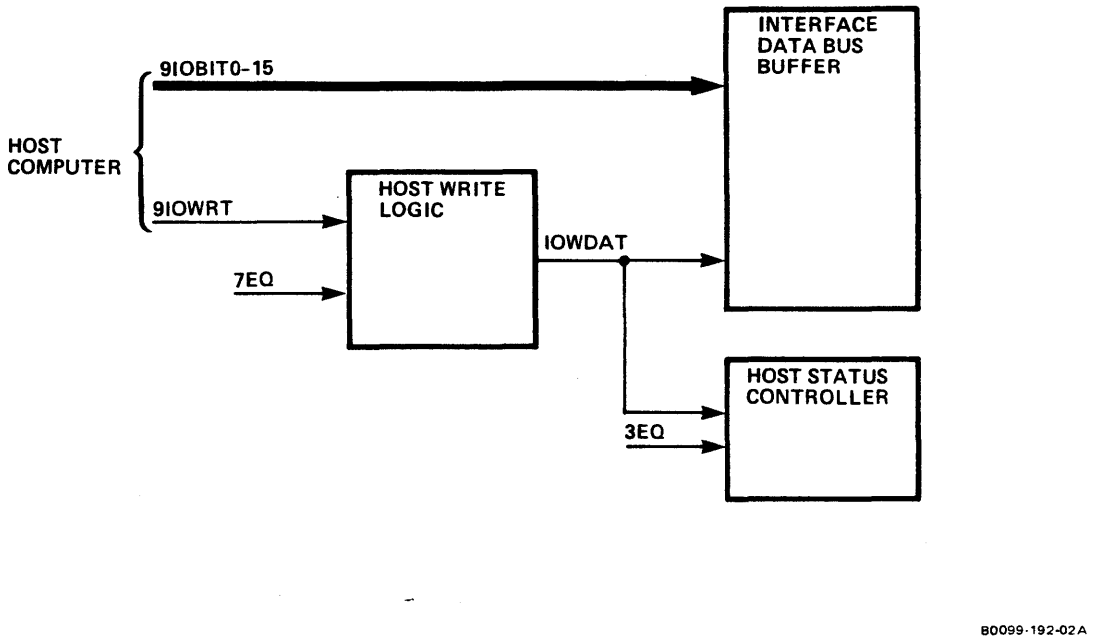


Figure 4-3. Host Data Input

4.5.1.d.1.c Status read control. The CPU routinely polls the host status controller to read host status. To develop a read control signal, the CPU transmits a control byte on address lines A0-7 and activates *IORQ and *RD (figure 4-4). The processor address bus driver transfers the byte to 4BZADR0-7, and the MOS control bus buffer converts *IORQ and *RD into 8IORQ and 8RD. When 8IORQ goes active, the processor bus address decoder decodes the byte to derive 5ENPPIO.

4.5.1.d.1.d Host status readout. The host status controller relays host status to the CPU. When 5ENPPIO, 8IORQ, and 8RD go active (figure 4-5), the controller converts latched signal IOWDAT into data bit D1 which goes to the CPU.

4.5.1.d.1.e Data bus control. To develop necessary control signals, the CPU transmits control bytes on A0-7 and activates *IORQ and *RD (figure 4-6). The processor address bus driver tranfers the bytes to 4BZADR0-7, and the MOS control bus buffer converts *IORQ and *RD into 8IORQ and 8RD. When 8IORQ goes active, the I/O address decoder decodes the bytes to derive 5SYSADR and 8ADRP.

4.5.1.d.1.f Display bus test. After 8RD and 5SYSADR go active (figure 4-7), the data bus driver control logic activates 5LORD under the control of clock pulses 7EQ1 and 2EQ and the display bus tester-controller begins a testing sequence under the control of 1CLKZ80 and 7EQ. A quiescent bus sets 5ENDAT, 1ENADR, and 1ENCONTL active.

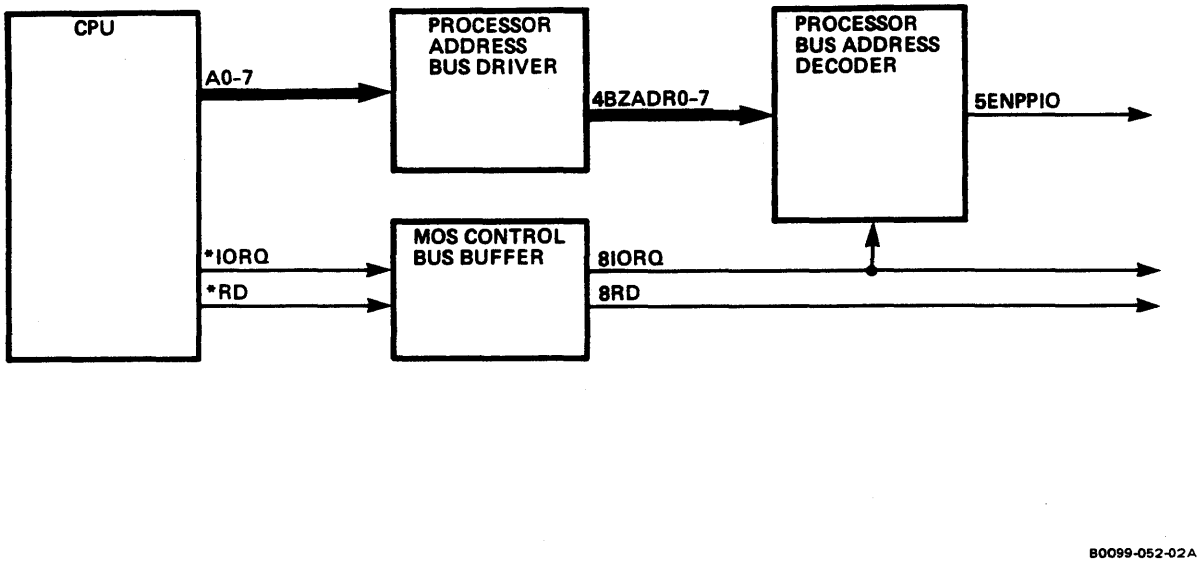


Figure 4-4. Status Read Control

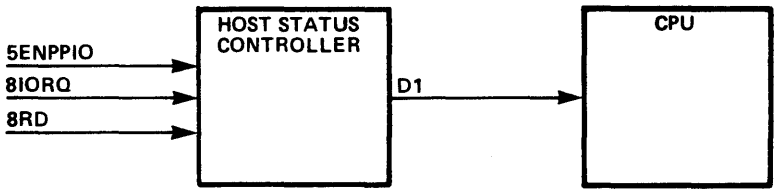


Figure 4-5. Host Status Readout

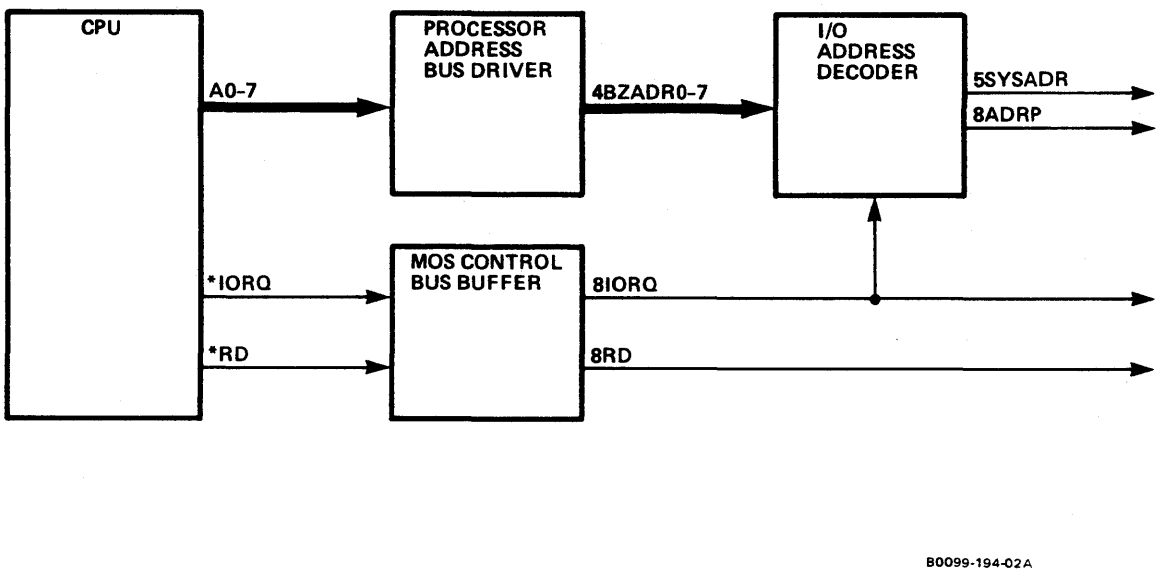


Figure 4-6. Data Bus Control

4.5.1.d.1.g Data read control. To develop a read control signal, the CPU transmits a control byte on A0-7 (figure 4-8) and sets *IORQ and *RD active. The processor address bus driver transfers the control byte to 4BZADR0-7, and the MOS control bus buffer converts *IORQ and *RD into 8IORQ and 8RD. When 1ENADR from the display bus tester-controller goes active, the display address bus driver transfers the control byte to 4BADR0-7. When 1ENCONTL goes active, the display control bus driver converts 8IORQ and 8RD into 9BIORQ and 9BREAD. With 9BIORQ active, the display bus address decoder accepts the control byte along with 9BREAD and derives 7RDIFDAT.

4.5.1.d.1.h Host data transfer. When 7RDIFDAT goes active (figure 4-9), the interface data bus buffer transmits latched host computer data on 9BDAT0-15. After 5SYSADR from the I/O address decoder, 5ENDAT from the display bus tester-controller, and 8RD go active, the data bus driver control logic activates 6LORD, 5HIRD and 5CLKHIRD under control of clock pulses 2EQ, 7EQ, and CLKZ80. The processor data bus driver multiplexes data from 9BDAT0-15 to 9BZDAT0-7 under control of 6LORD, 5HIRD, and 5CLKHIRD. When 8ADRP and 8RD go active, the MOS data bus buffer transfers data to D0-7.

4.5.1.d.1.i MAP unit control. The CPU typically stores host computer data in RAM. The MAP unit supplies address bits 12-18 for a RAM or ROM operation.

The processor address bus driver transfers control bytes from the CPU on A0-7 to 4BZADR0-7 (figure F04-6). The MOS control bus buffer converts *IORQ and *WR into 8IORQ and 8WR. With 8IORQ active, the processor bus address decoder accepts the control bytes and 8WR, and derives 5SELMD, 5WRMD, 5LDMA, and 5LDST. The MOS data bus buffer transfers address bytes from the CPU on D0-7

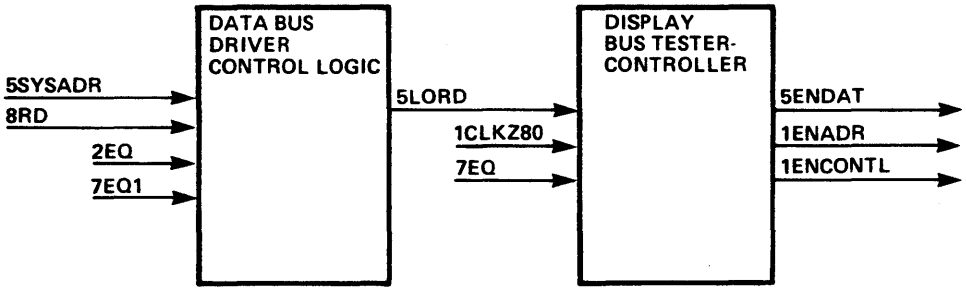


Figure 4-7. Display Bus Test

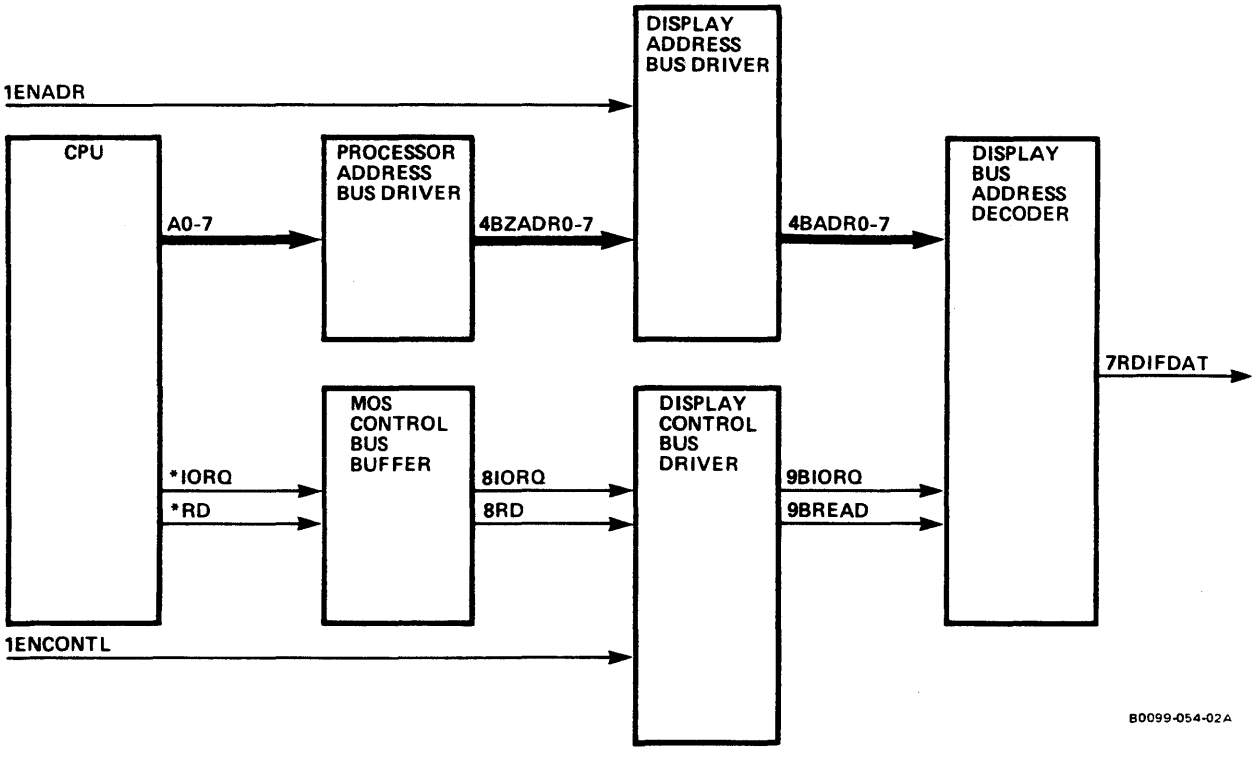


Figure 4-8. Data Read Control

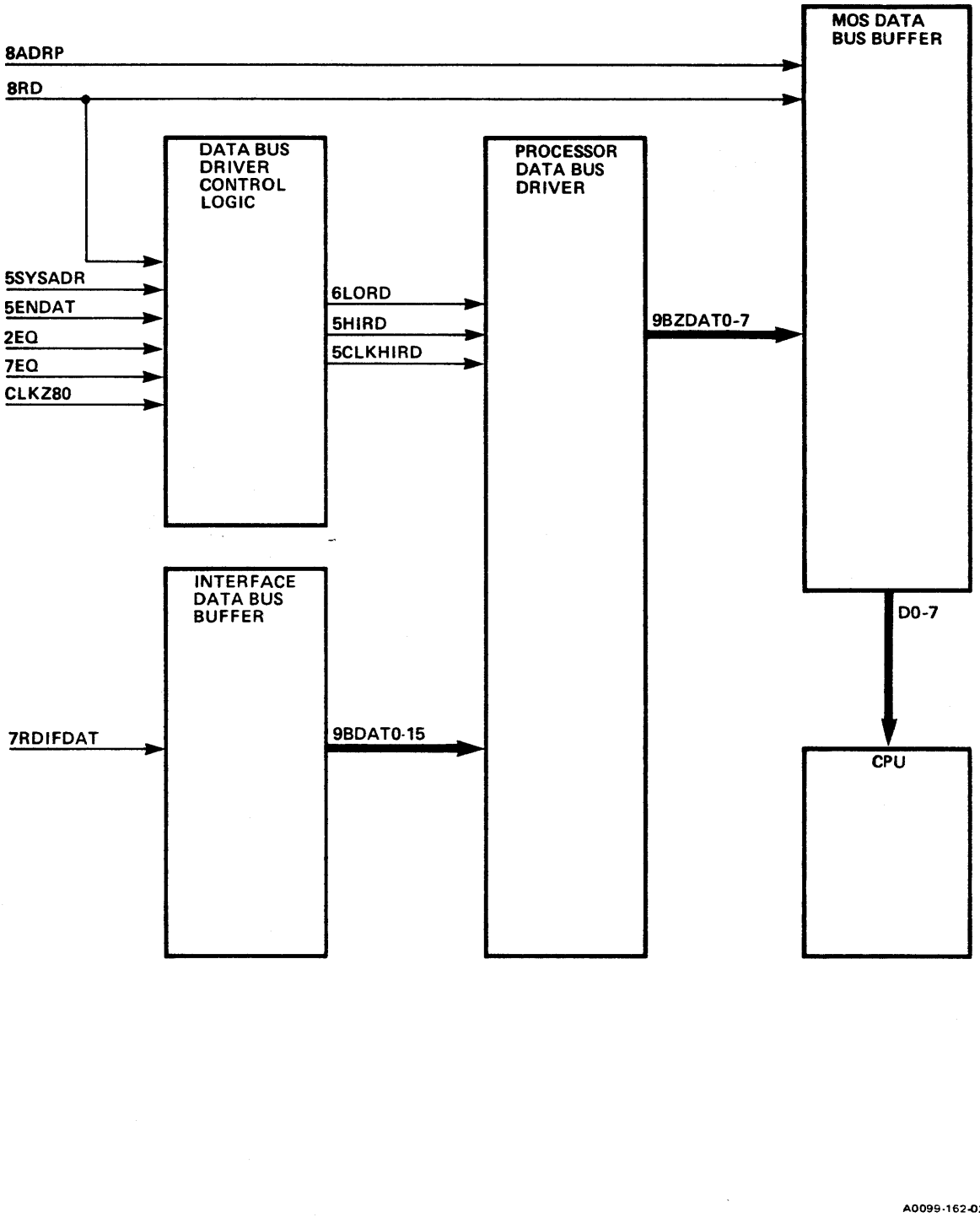


Figure 4-9. Host Data Transfer

to 9BZDAT0-7. The MAP unit accepts the address bytes and derives address bits 4BZADR12-18 under control of 5SELMD, 5WRMD, 5LDMA, 5LDST, and 8IORQ.

4.5.1.d.1.j Data storage. The CPU generates address bits A0-11, which become 4BZADR0-11 (figure 4-10). RAM receives these bits and 4BZADR12-18 from the MAP unit. After buffering, data bits D0-7 become 9BZDAT0-7; signals *MREQ and *WR become 8MREQ and 8WR. When 8MREQ and 8WR go active, RAM stores data received on 9BZDAT0-7 in locations specified by address bits 4BZADR0-18.

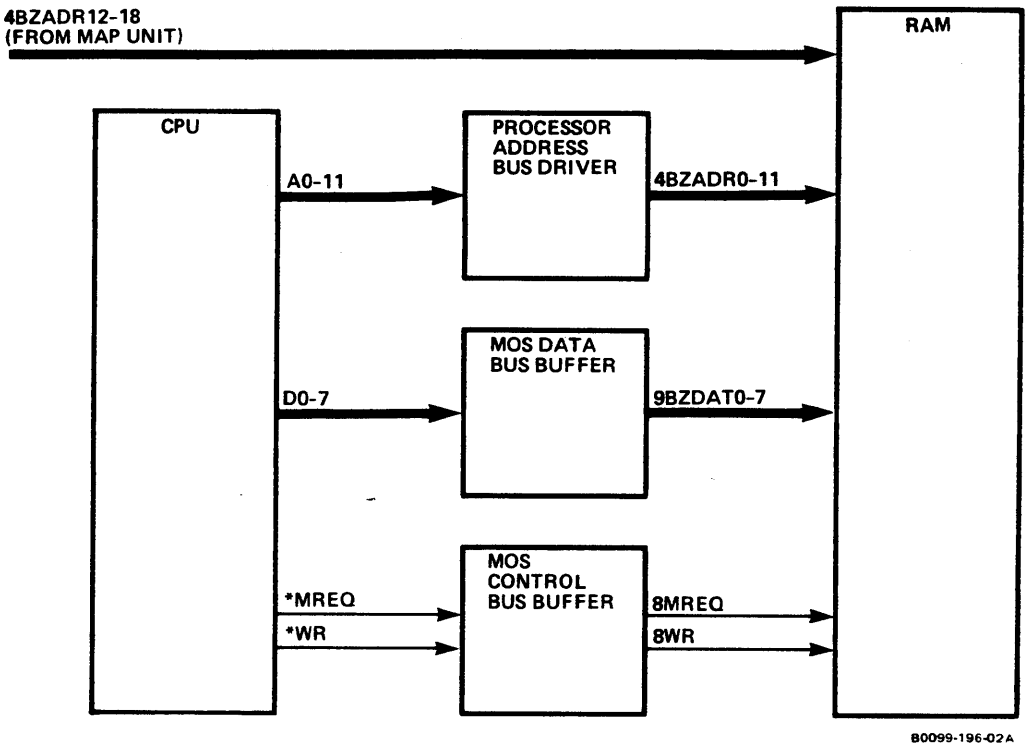


Figure 4-10. Data Storage

4.5.1.d.1.k RAM access. The CPU generates address bits A0-11 (figure 4-11) and signals *MREQ and *RD. The address bits become 4BZADR0-11; *MREQ and *RD become 8MREQ and 8RD. With 8MREQ and 8RD active, RAM transmits (on *MD0-7) data stored in locations specified by bits 4BZADR0-18. RAM also activates either 5MADR5 or 5MADR6.

4.5.1.d.1.l RAM output. After 8MREQ and either 5MADR5 or 5MADR6 go active (figure 4-10), the second 7FQ clock pulse after 8RD goes active enables the memory data driver. The memory data driver transfers data received on *MD0-7 to 9BZDAT0-7. When 8ADRP from the I/O address decoder and 8RD go active, the MOS data bus buffer transfers data to D0-7.

4.5.1.d.1.m ROM access. To access data from ROM, the CPU generates A0-11, *MREQ, and *RD (figure FO4-7). Respectively, these address and control bits become 4BZADR0-11, 8MREQ, and 8RD. ROM decodes bits 4BZADR12-18 from the MAP unit to derive either 6MADR1 or 6MADR2. After 8MREQ and either 6MADR1 or 6MADR2 go active, the memory data driver activates 5ENMRD at the second 7FQ clock pulse after 8RD goes active. Signal 5ENMRD enables ROM which transmits

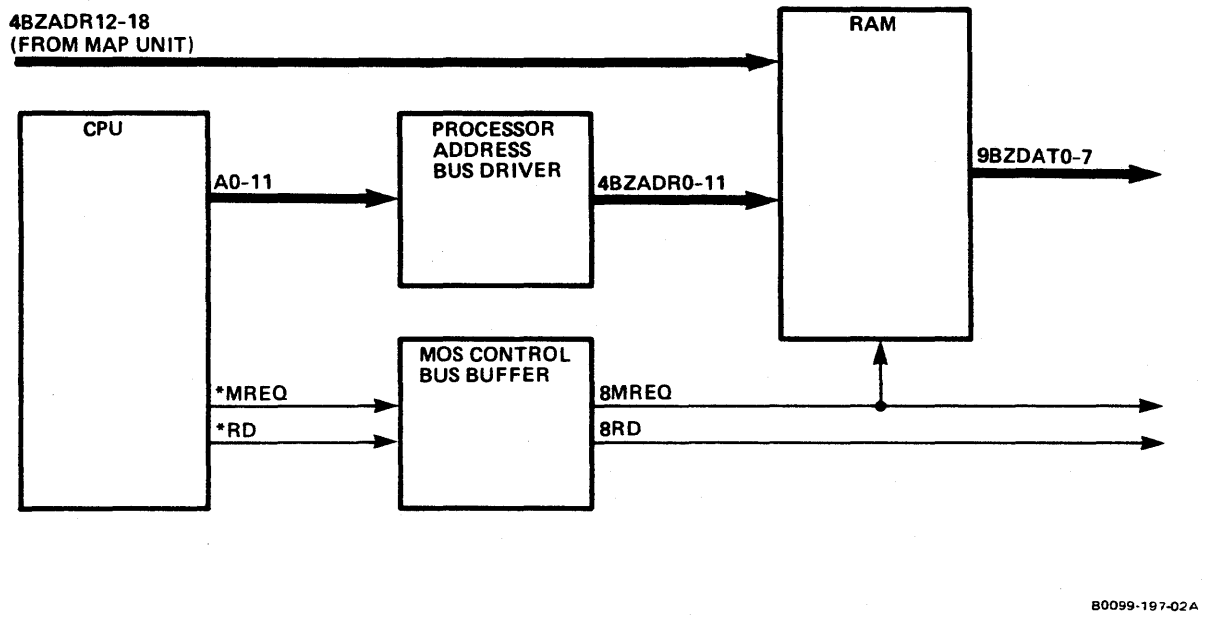


Figure 4-11. RAM Access

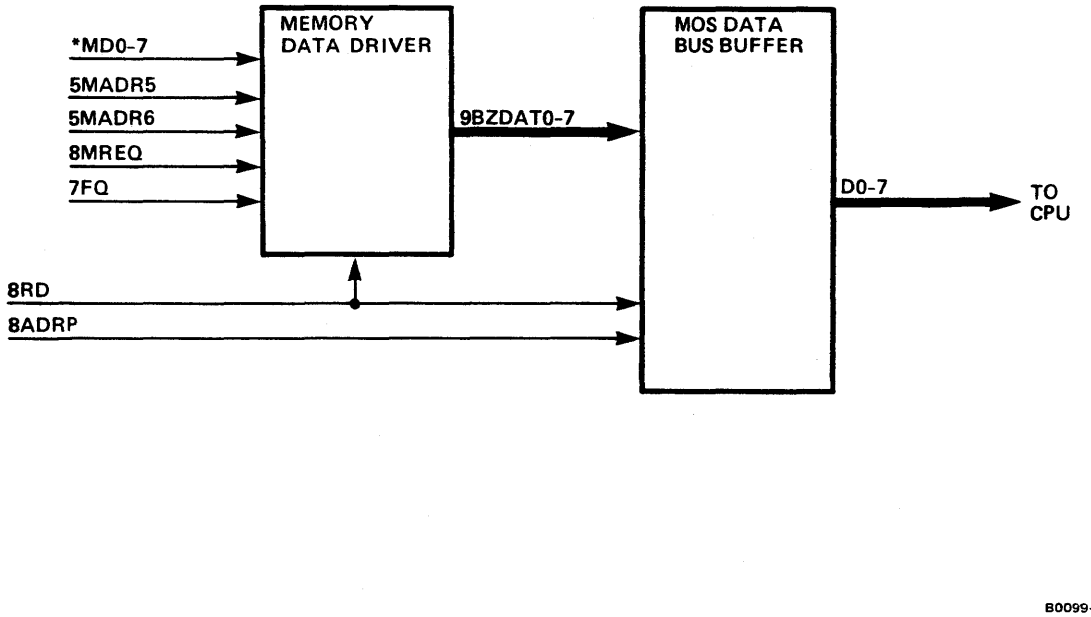


Figure 4-12. RAM Output

data on *MD0-7. Data locations are specified by bits 4BZADR0-18. The memory data driver transfers data to 9BZDAT0-7.

4.5.1.d.1.n ROM output. The MOS data bus buffer receives 8ADRP, 8RD, and data. When 8ADRP (from the I/O address decoder) and 8RD go active, the buffer transfers ROM data to the CPU on D0-7.

4.5.1.d.1.o Data output. When transferring data to the MCP PCB (figure F04-8) the CPU must generate an address and two control signals in addition to data. Bits D0-7, bits A0-7, signal *WR, and signal *IORQ become 9BZDAT0-7, 4BZADR0-7, 8WR, and 8IORQ, respectively. When 1ENCONTL from the display bus tester-controller goes active, 8WR and 8IORQ become 9BWRT and 9BIORQ, respectively. When 1ENADR goes active, 4BZADR0-7 become 4BADR0-7. After 5SYSADR from the I/O address decoder, 5ENDAT and 8WR go active, the data bus driver control logic activates 5LOWR and 6HIWR under the control of clock pulses CLKZ80, 2EQ, and 7EQ1. The display data bus driver transfers data from 9BZDAT0-7 to 9BDAT0-15 in two stages under control of 5LOWR and 6HIWR. All outputs go to the MCP PCB.

4.5.1.d.2 Keyboard data flow. Depending upon user requirements, a 9465 is configured with or without a serial link PCB. In the latter instance, a keyboard connects directly to the system processor PCB (Z80).

4.5.1.d.2.a Direct keyboard connection. A typical keyboard operation consists of these steps:

- Interrupt request
- Vector transfer
- Keyboard read control
- Keyboard data transfer

The serial peripheral I/O controller receives data from the keyboard on RD1 and *RD1 (figure 4-13) and sets interrupt request *IINT active. If ready to accept data, the CPU acknowledges the interrupt by making *M1 and *IORQ active.

When *M1 and *IORQ go active, the serial peripheral I/O controller sends a vector to the CPU on D0-7. This vector conditions the CPU to receive keyboard data.

To develop read control signals the CPU generates *IORQ, *RD, and bits A0-7 (figure 4-14). Bits A0-7 become 4BZADR0-7 and *IORQ becomes 8IORQ. Once 8IORQ goes active, the processor bus address decoder derives 5ENKSIO by decoding 4BZADR0-7.

When 5ENKSIO, *IORQ, and *RD go active (figure 4-15), the serial peripheral I/O controller converts keyboard serial data to parallel form for transfer to the CPU on D0-7. The CPU sends keyboard data to the MCP PCB in the same way as host computer data.

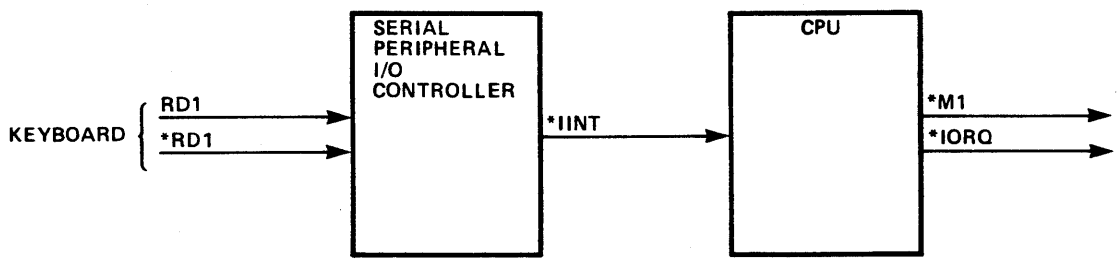


Figure 4-13. Interrupt Request

4.5.1.d.2.b Remote keyboard connection. When a serial link PCB is installed, the keyboard interfaces with the serial link PCB, and the system processor PCB receives keyboard data from the serial link PCB. A typical remote keyboard operation consists of these steps:

- Remote interrupt request
- Remote vector transfer
- Remote read control
- Remote data transfer

The serial link PCB receives data from the keyboard and sends interrupt request 9BZINT to the system processor PCB on the processor bus. The CPU receives 9BZINT (figure 4-16) and responds when ready by activating *IORQ and *M1 to signal an interrupt acknowledge. The CPU also generates address bits A0-7 and *RD. Bits A0-7 become 4BZADR0-7. Signals *M1 and *RD become 9BZM1 and 8RD, respectively. Signal *IORQ becomes 9BZIORQ and 8IORQ. Signals 9BZIORQ and 9BZM1 go to the serial link PCB. When 8IORQ goes active, the I/O address decoder accepts bits 4BZADR0-7 and derives 8ADRP.

After receiving 9BZIORQ and 9BZM1, the serial link PCB sends a vector to the system processor PCB MOS data bus buffer on 9BZDAT0-7. This vector identifies the interrupting device. When 8ADRP and 8RD go active, the MOS data bus buffer transfers the vector to the CPU on D0-7.

The CPU develops read control signals by generating *IORQ, *RD, and address bits A0-7 (figure 4-17). These signals become 9BZIORQ, 9BZREAD, and 4BZADR0-7, respectively. Signals *IORQ and *RD also become 8IORQ and 8RD. Address

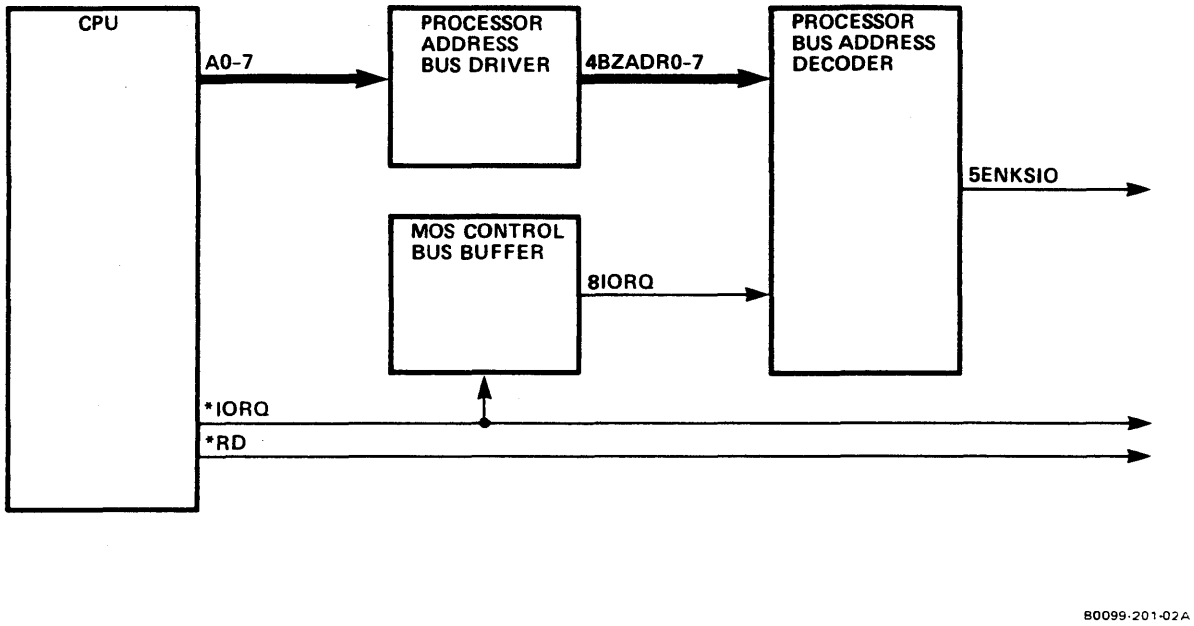


Figure 4-14. Keyboard Read Control

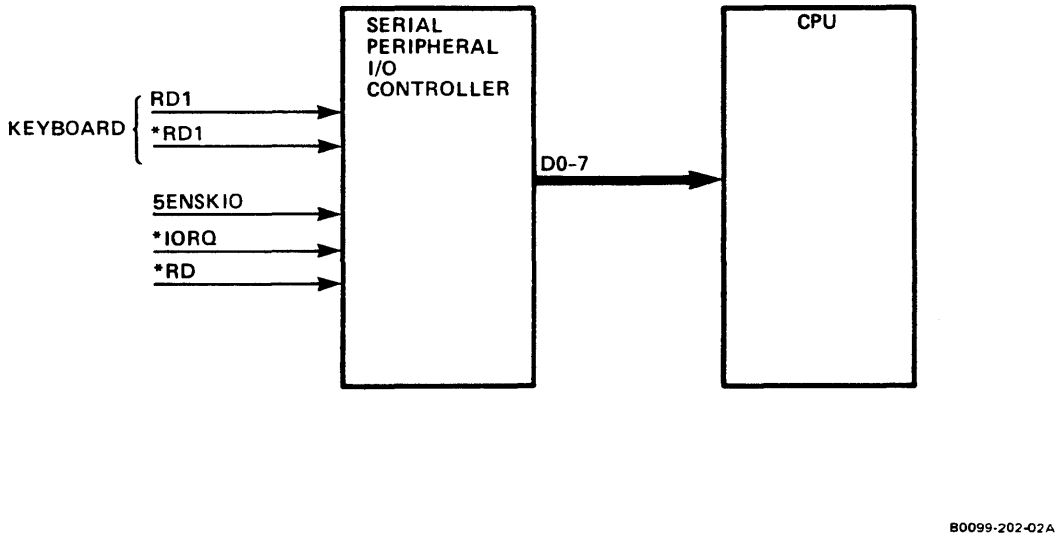


Figure 4-15. Keyboard Data Transfer

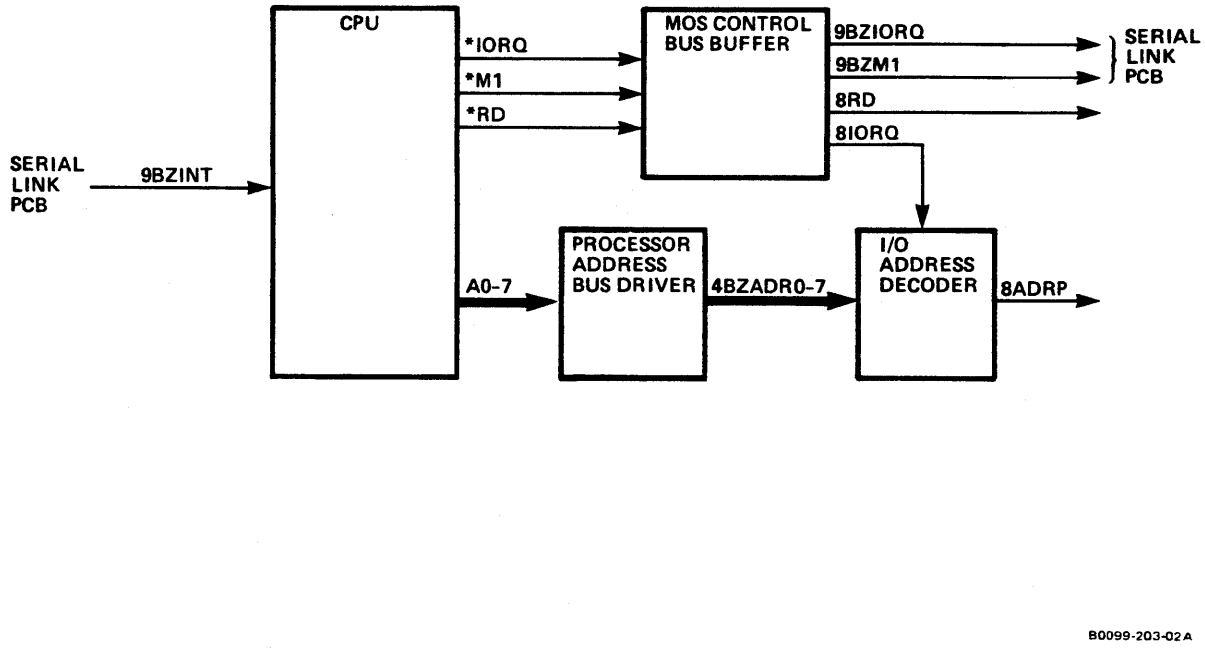


Figure 4-16. Remote Interrupt Request

bits 4BZADR0-7, signal 9BZIORQ, and signal 9BZREAD go to the serial link PCB. When 8IORQ goes active, the I/O address decoder accepts bits 4BZADR0-7 and derives 8ADRP.

After receiving an interrupt acknowledge and an address, the serial link PCB sends keyboard data on 9BZDAT0-7 to the MOS data bus buffer. When 8ADRP and 8RD go active, the MOS data bus buffer transfers keyboard data to the CPU on D0-7. The CPU then sends data to the MCP PCB in the same way as host computer data.

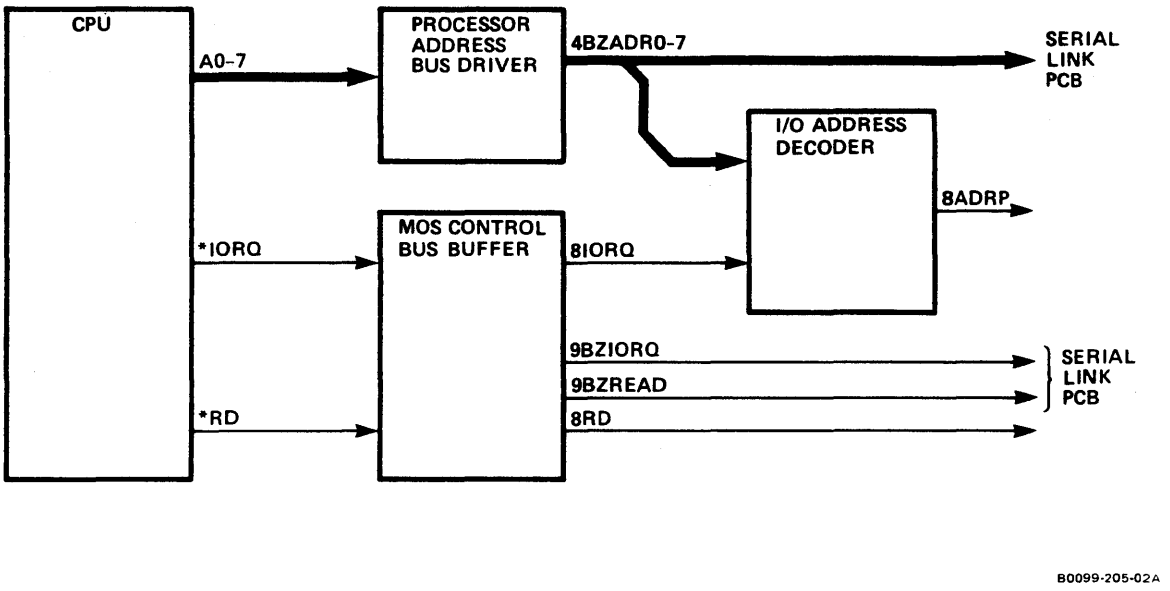


Figure 4-17. Remote Read Control

4.5.2 System Processor PCB (MC68000)

This PCB incorporates a Motorola MC68000L8 microprocessor (MC68000) and a Zilog Z80A-CPU microprocessor (Z80). The MC68000 functions as a central processing unit (CPU) and controls system processor PCB operation with the aid of the Z80.

The system processor PCB decodes instructions from the host computer, stores sub-pictures (display lists), stores application programs, stores character elements, performs coordinate transformations, drives the MCP PCB, and controls 9465 configuration. Interfaces include the host computer, 9465 PCBs and, optionally, a keyboard and joystick.

4.5.2.a Buses. Buses (figure FO4-9) include data, address, and control. Seven multiconductor buses connect to external logic; five additional buses distribute data and address information on the PCB.

The interface data bus connects the host computer to the host interface buffer and the host control logic. Data bus buffers and controllers are bidirectional. Address and control bus drivers are unidirectional. The 68000 data bus controller converts eight (D0-7) of the sixteen 68000-data-bus bits into display address bus bits 4BADR0-7. The processor address bus driver converts eight (ZA0-7) of the sixteen Z80-address-bus bits into processor address bus bits 4BZDAT0-7.

The processor bus address driver transfers address bits from the Z80 address bus to the processor address bus and supplies drive for the processor address bus. The driver converts bits ZA0-7 into 4BZADR0-7. No control signals are needed.

4.5.2.b Functional Elements. The system processor PCB (MC68000) has the following functional elements:

- CPU
- Clock generator
- Reset driver
- 68000 bus address decoder
- Display bus tester-controller
- Display address bus driver
- Display control bus driver
- RAM controller
- 68000 RAM
- 68000 ROM
- Transfer control logic
- Status LED logic
- Buffer control logic
- 68000 data bus buffer
- Display bus wait logic
- Configuration control logic
- Display bus address decoder
- Host control logic
- Host status register
- Processor status register

- Status driver
- Interface data bus buffer
- 68000 data bus controller
- Handshake control logic
- Z80 data bus controller
- Interrupt priority generator
- Interrupt reset register
- Z80 serial I/O processor
- Z80 address decoder
- Baud rate generator
- Serial peripheral I/O controller
- Serial host I/O controller
- Z80 data bus buffer
- Processor control bus driver
- Memory address decoder
- Z80 RAM
- Z80 ROM
- Daisy chain interrupt logic

4.5.2.b.1 CPU. The CPU (figure FO4-10) consists of the 68000 and supporting logic. The CPU receives clock pulse 148NSEC, three interrupt priority control bits, and two control signals, and generates 23 address bits and five control signals. The 16 data bus lines are bidirectional.

The two basic CPU operations are read and write. During a read cycle output signals 5RD and 5AS go active. During a write cycle 5WR and 5AS go active. During either a read or write cycle, 5LDS or 5UDS goes active during a lower data byte (D0-7) or upper data byte (D8-15) transfer, respectively. Both 5LDS and 5UDS go active during a word (D0-15) transfer. Input 5DTACK must also go active during a read or write cycle. The CPU operates at 6.7 MHz. Because this frequency is faster than other 9465 devices, 5DTACK delays CPU operation to allow time for a slower device to catch up. During a read cycle the CPU waits until 5DTACK goes active before reading data. During a write cycle the CPU waits until 5DTACK goes active before removing data from the data bus.

The CPU receives four 3-bit interrupt bytes, encoded for priority, on IPL0, 1, and 2. The CPU latches in each interrupt when received, then responds to the interrupts in order of priority.

Signal 5RESET resets the CPU and lights the HALT LED to indicate a halt state.

4.5.2.b.2 Clock generator. The clock generator supplies the clock pulses that synchronize system processor PCB operations. The generator receives differential clock pulse inputs from the sync PCB and generates five clock pulses that drive system processor PCB functional elements.

4.5.2.b.3 Reset driver. This driver generates signals RESET and 5RESET, which reset the system processor PCB. Signals RESET and 5RESET go active when 9PORCLR from the display bus goes active.

4.5.2.b.4 68000 bus address decoder. Signal 5AS enables this element, which decodes address bits A1-8 and 17-23 to derive eight control signals.

4.5.2.b.5 Display bus tester-controller. This controller sequentially tests bus conditions and generates control signals that reflect test results. Signal 5RDWR68 goes active when the TTL DMA attempts to communicate with the CPU and inhibits the initiation of the testing sequence. After a reset, the controller tests 5SYSADR. When the CPU needs to communicate with a device on the display bus, 5SYSADR goes active and, at the next 148NSEC clock pulse, the controller activates 5WAIT, which remains active throughout the testing sequence. Also, BAKOUT goes inactive. The controller then tests signals 9BBUSY, 9BREQ, and BAKIN. If 9BBUSY or 9BREQ is active or BAKIN is inactive, the controller continues to monitor the signals until 9BBUSY and 9BREQ are inactive and BAKIN is active. The controller then activates 9BREQ and BAKOUT at the next 148NSEC pulse and tests 9BBUSY. If 9BBUSY is still inactive, indicating that the display bus is not in use, the controller takes possession of the bus by activating 9BBUSY at the next 148NSEC pulse. After the next 296NSEC clock pulse 5ENADR goes active followed by 1ENCONTL, then BKOUT goes active if BAKIN is active, and all other outputs go inactive. The entire sequence then repeats.

4.5.2.b.6 Display address bus driver. This driver transfers address bits from the 68000 address bus to the display address bus and supplies drive for the display address bus. When 5ENADR goes active, the driver transfers bits received on A1-8 to 4BADR0-7.

4.5.2.b.7 Display control bus driver. This driver supplies drive for three display control bus signals. When signals 1ENCONTL and 5IOEN go active, the driver converts 5RD and 5WR into 9BREAD and 9BWRT, respectively. When 5AS is also active, the driver converts 5IOEN into 9BIORQ.

4.5.2.b.8 RAM controller. The RAM controller controls 68000 RAM operation. Signal 5RAMEN enables the controller, and 5RAMWR initiates a write cycle. The controller converts 16 of the 23 address bits received into memory address bits DA0-7 and either 5RAS0 or 5RAS1. These outputs and 5CAS and 5WE drive the 68000 RAM. At the end of the cycle the controller generates 5XACK, which informs the CPU, indirectly, that the cycle is complete.

Signal 5RAMRD initiates a read cycle, which is similar to a write cycle except that 5WE remains inactive. Also, 5XACK enables the 68000 RAM read register as well as informing the CPU that the read cycle is complete.

4.5.2.b.9 68000 RAM. The 68000 RAM consists of thirty-two 64K-bit dynamic RAM chips that form a 128K X 16-bit array, and supporting logic.

During a write cycle signals 5RAMEN and 5WR go active causing 5RAMWR to go active. When signals 5WE and either 5LDS or 5UDS or both also go active, RAM stores data on D0-15 in the address specified by bits DA0-7, 5CAS, and either 5RAS0 or 5RAS1.

During a read cycle signals 5XACK, 5RAMEN, and 5RD go active causing 5RAMRD to go active. RAM transmits, on D0-15, the data stored in the address specified by bits DA0-7, 5CAS, and either 5RAS0 or 5RAS1.

The 68000 RAM is a dynamic memory and must be refreshed continually to retain stored data. Signals 5RAS0 and 5RAS1 go active every 15 microseconds to refresh the RAM chips.

4.5.2.b.10 68000 ROM. The 68000 ROM (figure F04-10) consists of 16 EPROM ICs that form a 64K x 16-bit word array, which can be doubled as an option. ROM stores the system processor PCB program. When signals 5RD and 5ROMAN go active, ROM transmits, on D0-15, data stored in the address received on A1-17.

4.5.2.b.11 Transfer control logic. This logic receives status signals from seven devices and sends signal 5DTACK to the CPU. Signal 5DTACK goes active each time one of the seven devices completes an operation. That is, on each of the following seven occasions:

- When 5DTACK and 5RAMEN are active at the end of a 68000 RAM operation.
- When 5PIODTACK and 5PIO2EN go active at the end of a 68000 data bus controller operation.
- At the first 148NSEC clock pulse after 5LEDEN and either 5LDS or 5UDS go active to allow time for an LED register operation.
- At the first 148NSEC pulse after 5ROMEN and either 5LDS or 5UDS go active to allow time for 68000 ROM operation.
- At the first 148NSEC pulse after 5DMAX and either 5LDS or 5UDS go active to allow time for a TTL DMA operation.
- At the first 148NSEC pulse after 5CLREN and either 5LDS or 5UDS go active to allow time for an interrupt reset register operation and an interrupt priority generator reset.
- At the third 148NSEC pulse after 5ENADR and either 5LDS or 5UDS go active, provided 5WAIT is not active, to allow time for a device served by the display bus to complete an operation.

The DTACK logic also generates LEDCK, which clocks the LED register. Signal LEDCK goes active at the first 148NSEC pulse after either 5LDS or 5UDS goes active.

4.5.2.b.12 Status LED logic. This logic consists of the LED register and eight status LEDs. The LED register receives eight data bits from the CPU and two control signals, and supplies the drive that lights the LEDs. Signal 5LEDEN enables the register, and LEDCK latches data received on D0-7 into the register, which lights the LEDs specified by the data.

4.5.2.b.13 Buffer control logic. This logic generates 5RW68, which enables the 68000 data bus buffer. When 5RDWR68 is active, 5RW68 goes active at the second 148NSEC clock pulse after 5DMAX goes active. Signal 5RW68 also goes active when 5ENADR and 5SYSADR go active. The logic, therefore, ensures that the buffer is functioning during a DMA transfer (5DMAX active), a CPU read or write operation (5RDWR68 active), or when an address goes out on the display bus (5ENADR and 5SYSADR active).

4.5.2.b.14 68000 data bus buffer. This bidirectional buffer transfers data between the 68000 data bus and the display data bus and supplies drive in both directions. Signal 5RW68 enables the buffer, and 5WR determines the direction of data flow. When 5RW68 and 5WR go active, the buffer inverts data bits D0-15 to become 9BDAT0-15. When 5RW68 goes active and 5WR remains inactive, the buffer inverts bits 9BDAT0-15 to become D0-15.

4.5.2.b.15 Display bus wait logic. This logic generates 5WAIT, which goes to the DTACK generator and delays CPU operation by delaying 5DTACK. Signal 5WAIT goes active when 5ENADR goes active and one of the following four conditions exists:

- 9BWAIT is active.
- WR68 is active and either 5RW68, 5LDS, or 5WR is inactive.
- RD68 is active and either 5RW68, 5LDS, or 5RD is inactive.
- 7RDWIF is active and either 5IORDY or 5IORD is active.

Signal 5ENADR goes active when the CPU is attempting to communicate with a device on the display bus and has sent out an address on the display bus. Signal 9BWAIT goes active when the device is unable to respond immediately. Signal WR68 goes active when the DMA on the display bus is attempting to send data to the CPU. Signals 5RW68, 5LDS, and 5WR remain inactive until the CPU responds. Signal RD68 goes active when the DMA is attempting to receive data from the CPU. Signals 5RW68, 5LDS, and 5RD remain inactive until the CPU responds. Signal 7RDWIF goes active when the CPU or the DMA attempts to communicate with the host computer. Signal 5IORDY goes active when the host computer is attempting to send data. Signal 5IORD goes active when the host computer is attempting to receive data.

4.5.2.b.16 Configuration control logic. This logic consists of the configuration driver and configuration switches SW1 and SW2. The switches set up signals SW0-15, which reflect selected switch settings. When signals 5LEDEN and 5RD go active, the driver transfers the signals on SW0-15 to D0-15. The CPU uses the signals to configure the system.

4.5.2.b.17 Display bus address decoder. Signal 9BIORQ enables this decoder (figure F04-10). When 9IORQ goes active, this element decodes address bits 4BADR0-7 and control signals 9BWRT and 9BREAD to derive six control outputs.

4.5.2.b.18 Host control logic. Host control logic monitors and controls host computer data transfer. A detailed description follows.

4.5.2.b.19 Host status register. This register receives four host computer status signals and sends three latched status outputs to the 68000 data bus controller. When ROD, IOWDAT, or IOCMD1 goes active, the next *148NSEC clock pulse latches the signal into the register and IFREAD, IFWRITE, or IFCOMMAND goes active, respectively. When input SIFRDY goes active, all three outputs go inactive at the next *148NSEC pulse. Signal 5RESET resets the register.

4.5.2.b.20 Processor status register. This register receives interrupt signals on the display data bus and sends the signals to the status driver. The register also sends the signals out to the optional interface PCB as 9IINT0, 1, 4, and 5. After 7IFSTAT goes active, the next 148NSEC clock pulse clocks

data received on 9BDAT0, 1, 4, and 5 into the register. The data remains latched in until cleared. Signal 1CLINT is normally active. After 7CLINT goes active, then inactive, 1CLINT goes inactive, and the next 148NSEC pulse clears the register.

4.5.2.b.21 Status driver. This driver receives status signals on the display bus and signals 9BIINT0, 1, 4, and 5 and 5IOREADY, and sends the signals to the host computer on the interface data bus. Signal 7IFSTAT latches signals received on 9BDAT8-15 into the driver. When 1IOREAD and IOCMD subsequently go active, the driver transfers the received signals to 9IOBIT0-15, which go to the host computer.

4.5.2.b.22 Interface data bus buffer. This bidirectional buffer transfers data between the interface data bus and the 68000 data bus and supplies latched data in both directions. Signal IOWDAT latches data received on 9IOBIT0-15 into the buffer. When 7RDIFDAT subsequently goes active, the buffer transmits the data on 9BDAT0-15. Signal 7WRIFDAT latches data received on 9BDAT0-15 into the buffer. When 1IOREAD subsequently goes active and IOCMD remains inactive, the buffer transmits the data on 9IOBIT0-15.

4.5.2.b.23 68000 data bus controller. This controller (figure FO4-10) transfers data and control signals between the 68000 data bus and the transfer bus. The controller exchanges information with the CPU on D0-7, and with the Z80 data bus controller on IOD0-7. The first 148NSEC clock pulse after signals 5PIO2EN and 5LDS go active enables the 68000 data bus controller. Address lines A1-5 permit the CPU to monitor internal controller operations. At power-on the CPU programs the controller via address lines A1-5. Subsequently, the CPU routinely polls the controller by activating 5PIO2EN and 5LDS and sending a transfer-status byte on A1-5. The controller responds by transferring signals IFREAD, IFWRITE, IFCOMMAND, WR68, and RD68 to D0, 1, 2, 4, and 5, respectively, which go to the CPU. Also, the controller inverts signals 9DMADONE and 9TVBBB, and transfers the inverted signals to D3 and D6, respectively.

When the CPU sends signals 5WR, 5PIO2EN, and 5LDS and a transfer-status byte, the controller converts bit D7 into INTHOST, which goes to the I/O interrupt logic.

When the CPU sends 5WR and a transfer-data byte on A1-5, the controller transfers data from the CPU on D0-15 to IOD0-7, and inactivates normally-active signal H2. If the Z80 data bus controller is ready to receive data, normally-active signal H1 also goes inactive. After the Z80 data bus controller reads the data, H1 goes active again.

When 5WR is inactive, the 68000 data bus controller is ready to receive data from the Z80 data bus controller on IOD0 4-7. When the Z80 data bus controller sends data, normally-active signal H3 goes inactive and latches the data into the 68000 data bus controller, which subsequently activates H4 to signal a busy state, and activates PIRQ to request on interrupt. When the CPU responds by activating 5PIO2EN and 5LDS, the controller transfers the data to D0-7.

Input 9THBBB clocks the internal timer. The controller sends timer data to the CPU on D0-7 in response to a read-timer byte on A1-5.

4.5.2.b.24 Handshake control logic. This logic generates four signals that control the 68000 and Z80 data bus controllers. Signal 5ASTB goes active when ARDY goes active and H4 is inactive. Signals H1, 2, and 3 are normally active. Signal H1 goes inactive when H2 goes inactive and H4 is inactive. Signal H3 goes inactive at the second 296NSEC clock pulse after 5ASTB goes active. At the next 296NSEC pulse H3 goes active again. Signal 5BSTB goes active at the first 296NSEC pulse after H1 goes inactive, and remains active for one 296NSEC pulse.

4.5.2.b.25 Z80 data bus controller. This controller transfers data between the transfer bus and the Z80 data bus. The controller exchanges data with the 68000 data bus controller on IOD0-7, and exchanges data with the Z80 serial I/O processor on ZD0-7. The Z80 data bus controller also receives eight control signals and two address bits that function as control signals, and generates six control outputs. Signal 5PIOEN enables the controller. Address bit ZA1 goes active to indicate a control signal is on the Z80 data bus, and goes inactive to indicate data is on the bus. When ZA0 goes active, the controller inverts data bits ZD0 and 1 to become signals ZINT and XMIT. When ZA0 goes inactive, signals 5ASTB and 5BSTB control data transfer between the transfer bus and the Z80 data bus.

Signal 5BRDY goes active to signal that the controller is ready to receive data on the transfer bus. After data arrives, 5BSTB goes active and latches the data into the controller, which inactivates 5BRDY and sends interrupt request signal 5INT to the Z80 serial I/O processor. When 5M1 and 5IORQ from the processor go active, the controller sends an interrupt vector to the processor on the data bus to identify the controller as the interrupt source. When 5IORQ and 5RDZ from the processor subsequently go active, the controller sends the data to the processor, which then sends the signals to activate XMIT, signaling that the processor has received the data. When exchanging data with the serial link PCB, the processor sends the necessary signals to activate ZINT, signaling that an operation is in progress.

When the processor sends data to the controller, 5IORQ goes active and latches the data into the controller, which activates ARDY to signal that the controller has data to send on the transfer bus. When the 68000 data bus controller is ready to receive data, 5ASTB goes active and the Z80 data bus controller sends the data.

Signal 5MREQ prevents the controller from making an interrupt request during a memory operation.

4.5.2.b.26 Interrupt priority generator. This generator receives four interrupt signals and generates encoded 3-bit interrupts that reflect priority levels. When SOFRST, ZINT, XMIT, or PIRQ goes active, the next 148NSEC clock pulse latches the signal into the generator, which then sends an interrupt byte to the CPU on IPL0, 1, and 2. Signal SOFRST has top priority followed by ZINT, XMIT, and PIRQ. When SOFRST goes active, the generator also generates

signals 8ZWAIT and 9DMARST. Signals CLR1-4 clear the latched interrupt signals. Signal 5RESET clears all signals except SOFRST, which comes from the host computer.

4.5.2.b.27 Interrupt reset register. This register receives reset data from the CPU and generates four reset signals that clear the interrupt priority generator. Signals 5CLREN and 5WR enable the register. When 5CLREN and 5WR are active, LEDCK clocks data received on D0-7 into the register, which converts data bits D0-3 into CLR1-4.

4.5.2.b.28 Z80 serial I/O processor. This processor (figure F04-10) functions as a CPU that controls the devices on the Z80 and processor buses, and consists of a Z80A-CPU microprocessor and supporting logic. The processor receives clock pulse 296NSZ80 and three control signals, and generates 16 address bits and five control outputs. Eight data lines are bidirectional.

A typical processor operation consists of three cycles. Cycle M1 is the operation code fetch cycle, and cycles M2 and M3 are read or write cycles. Signal 5M1 is active during an M1 cycle. Signal 5MREQ is active during a memory read or write operation, and 5IORQ is active during a read or write cycle with an I/O device. Signal 5RDZ is active during a read cycle, and 5WRZ is active during a write cycle. Signals 5M1 and 5IORQ go active together to indicate an interrupt acknowledge.

4.5.2.b.29 Z80 address decoder. Signal 5IORQ enables and 5M1 inhibits this element. When 5IORQ is active and 5M1 is inactive, this element decodes address bits ZA0-7 to derive four control outputs.

4.5.2.b.30 Baud rate generator. This generator supplies baud rate pulses BAUD1-4 to the serial I/O controllers. Data received on ZD0-3 select the required baud rates. Signals 5BAUDEN and 5WRZ load the data into locations specified by address bits ZA0 and 1. The generator is crystal-controlled to stabilize baud rates.

4.5.2.b.31 Serial peripheral I/O controller. This controller interfaces with an optional keyboard and joystick when a serial link PCB is not installed. The keyboard connects to receptacle J1, the joystick to J2. Signal 5SIO1EN enables the controller. When address bit ZA0 is active, the controller transfers data between the Z80 data bus and the joystick. When ZA0 is inactive, the controller transfers data between the Z80 data bus and the keyboard. Bit ZA1 goes active to indicate control information is on the data bus, and goes inactive to indicate data is on the bus. Clock pulse 296NSEC synchronizes controller operations. Baud rate pulse BAUD1 clocks keyboard data transfers, and BAUD2 clocks joystick data transfers.

When the keyboard sends serial data on differential input lines RD1 and *RD1, the controller sends interrupt request signal 5INT to the Z80 serial I/O processor. When the processor signals an interrupt acknowledge by activating 5M1 and 5IORQ, the controller sends an interrupt vector on data ZD0-7 to identify the controller as the interrupt source. When the processor responds by activating 5RDZ, 5IORQ, and 5SIO1EN, the controller converts the serial data to parallel form and transmits the data on the data bus.

When the processor has data to send to the keyboard, 5IORQ goes active. The controller then converts the parallel data received on the data bus to serial form and sends the data to the keyboard on differential output lines SD1 and *SD1. The controller handles joystick data transfers in the same way.

4.5.2.b.32 Serial host I/O controller. This controller is used only for test purposes. Two serial RS232 I/O channels are available to interface with a host computer. Each channel has one data and two control inputs, and one data and two control outputs.

4.5.2.b.33 Z80 data bus buffer. This bidirectional inverting buffer transfers data between the Z80 data bus and the processor data bus, and supplies drive in both directions. Four control signals and four address bits determine the direction of the data flow. When 5IORQ is inactive, the buffer inverts data bits ZD0-7 to become 9BZDAT0-7.

When the Z80 serial I/O processor attempts to read data from the serial link PCB on the processor bus, 5IORQ, 5RDZ, and one of bits ZA4-7 go active. This reverses the data flow, and the buffer inverts 9BZDAT0-7 to become ZD0-7. Also, when the processor acknowledges an interrupt request from a device on the serial link PCB, 5IORQ and 5M1 go active and 5IE04 remains active. This again reverses the data flow. When a system processor PCB device makes an interrupt request, 5IE04 goes inactive, and no flow reversal occurs.

4.5.2.b.34 Processor control bus driver. This driver supplies drive for three processor control bus signals. The driver converts signals 5IORQ, 5RDZ, and 5M1 into 9BZIORQ, 9BZREAD, and 9BZM1, respectively.

4.5.2.b.35 Memory address decoder. Signal 5MREQ enables this decoder. When 5MREQ goes active, this element decodes address bits ZA13, 14, and 15 to derive memory control signals 5ZRAMEN and 5ZROMEN.

4.5.2.b.36 Z80 RAM. The Z80 RAM is a 2K x 8-bit static RAM chip. During a write cycle 5ZRAMEN and 5WRZ go active, and RAM stores data received on ZD0-7 in the locations specified by address bits ZA0-10. During a read cycle 5ZRAMEN and 5RDZ go active and 5WRZ remains inactive, and RAM transmits, on ZD0-7, data stored in the locations specified by address bits ZA0-10. Since the Z80 RAM is a static RAM, no refreshing is needed.

4.5.2.b.37 Z80 ROM. The Z80 ROM is an 8K x 8-bit erasable PROM chip that stores program data for the Z80 serial I/O processor. When signals 5ZROMEN and 5RDZ go active, ROM transmits, on ZD0-7, data stored in the locations specified by address bits ZA0-12.

4.5.2.c Detailed Functional Descriptions. Host control logic and daisy chain interrupt logic are discussed in detail. Host control logic monitors and controls data transfer between the 9465 and the host computer. Daisy chain interrupt logic arbitrates contention between devices seeking access to the CPU.

4.5.2.c.1 Host control logic. This logic (figure F04-11) consists of nine functional elements:

- Host clear logic
- Soft reset logic
- Host write logic
- Host command logic
- Host read logic
- Data transfer logic
- I/O ready logic
- Clear status logic
- I/O interrupt logic

4.5.2.c.1.a Host clear logic. This logic generates 9BRESCLR when either 9IOPCLR goes active or 9IOBIT15 and IOCMD1 go active.

4.5.2.c.1.b Soft reset logic. This logic generates SOFRST when 9IOBIT0 and IOCMD1 go active.

4.5.2.c.1.c Host write logic. This logic generates signals HWRT and IOWDAT. Both signals go active at the first 148NSEC clock pulse after 9IOWRITE from the host computer goes active. Signal IOWDAT remains active for one 148NSEC pulse. Signal HWRT remains active until the first 148NSEC pulse after 9IOWRITE goes inactive.

4.5.2.c.1.d Host command logic. This logic generates signals IOCMD and IOCMD1. Signal IOCMD goes active at the first 148NSEC clock pulse after 9IOCMD from the host computer goes active. When HWRT subsequently goes active, IOCMD1 goes active.

4.5.2.c.1.e Host read logic. This logic generates signals 1IOREAD, 5IORD, ROD, and RDTLE. Signal 1IOREAD goes active when 9IOREAD from the host computer goes active. Signal 5IORD goes active at the second 148NSEC clock pulse after 9IOREAD goes active. In soft interface systems RDTLE goes active at the first 148NSEC pulse after 9IOREAD goes inactive and remains active for one 148NSEC pulse. In hard interface systems RDTLE is normally active and goes inactive at the first 148NSEC pulse after 9IOREAD goes active, then goes active again at the following 148NSEC pulse.

4.5.2.c.1.f Data transfer logic. This logic generates signals 7RDWIFD and RWIFD. Signal 7RDWIFD goes active when either 7WRIFDAT or 7RDIFDAT goes active. Signal RWIFD goes active when 7RDWIFD goes active and 1RESETRW remains inactive.

4.5.2.c.1.g I/O ready logic. This logic generates signals SIFRDY, 9IOREADY, and 5IOREADY. Signal SIFRDY goes active when RWIFD goes active or 7IFSTAT and 9BDAT6 go active. In soft interface systems 9IOREADY and 5IOREADY go active at the fourth 148NSEC clock pulse after SIFRDY goes inactive, and remain active until the first 148NSEC pulse after either IOWDAT or ROD goes active. In hard interface systems 9IOREADY goes inactive when 5IOREADY goes inactive.

4.5.2.c.1.h Clear status logic. This logic generates signals 5CLSTR, 1CLINT, and 7CLINT. Signal 5CLSTR goes active when either 9CLSTAT goes active or IOCMD and RDTLE go active. Signal 7CLINT goes active at the second 148NSEC clock pulse after either 5CLSTR or 5RESET goes active. Signal 1CLINT is normally active and goes inactive at the second 148NSEC pulse after 5RESET goes active, then goes active again at the following 148NSEC pulse. Signal 1CLINT also goes inactive at the first 148NSEC pulse after either 5CLSTR or 5RESET goes inactive and the other remains inactive. At the following 148NSEC pulse 1CLINT goes active again.

4.5.2.c.1.i I/O interrupt logic. This logic generates 9IOINT, which goes to the host computer. Signal 9IOINT goes active at first 148NSEC clock pulse after either RWIFD and INTHOST go active or 7IFSTAT and 9BDAT7 go active. Signal 9IOINT remains active until the first 148NSEC pulse after 5CLSTR goes active.

4.5.2.c.2 Daisy chain interrupt logic. This logic (figure F04-12) determines interrupt priority when two or more devices attempt to interrupt the Z80 serial I/O processor simultaneously. The logic consists of two gates and an inverter. The daisy chain consists of three controllers. When a serial link card is installed, the chain extends to three serial link PCB controllers. When no device is busy, interrupt enable signals PRIO1, PRIO2, and IEO3 are active. Gate 1 generates IEI3, which goes active when PRIO1 and PRIO2 are active. Gate 2 generates BZIEO, which goes active when IEI3 and IEO3 are active, and goes out to the serial link PCB to the next controller on the daisy chain. After inversion BZIEO becomes 5IEO4, which goes to the Z80 data bus buffer. When the serial peripheral I/O controller needs to communicate with the Z80 serial I/O processor, the controller activates interrupt request signal 5INT and inactivates PRIO1, causing IEI3 and BZIEO to go inactive. The serial host I/O controller cannot activate 5INT while PRIO1 is inactive, and the Z80 data bus controller cannot activate 5INT while IEI3 is inactive. Similarly, no serial link PCB controller can make an interrupt request while BZIEO is inactive. The serial peripheral I/O controller has top priority. When any device on the daisy chain activates 5INT, no lower priority device can interrupt the processor until the operation is complete.

4.5.2.d Process Descriptions. Typical PCB processes include host data flow and keyboard data flow. The 9465 is usually configured with a serial link PCB, but keyboard data flow is discussed for 9465s with or without a serial link PCB.

4.5.2.d.1 Host data flow. In a typical operation the system processor PCB receives data from the host computer and sends processed data to the MCP for display on the monitor. A typical operation consists of these steps:

- 9465 status readout
- Host data input
- Status read control
- Host status readout
- Data transfer control
- Data read control
- Host data transfer
- Data storage

- RAM readout
- ROM readout
- Output control
- Data output

4.5.2.d.1.a 9465 status readout. The host computer receives 9IOREADY, which conditions the host for data transmission to the 9465. When 9IOREADY is active and the host has data to send, the host first reads 9465 status by activating signals 9IOREAD and 9IOCMD (figure 4-18).

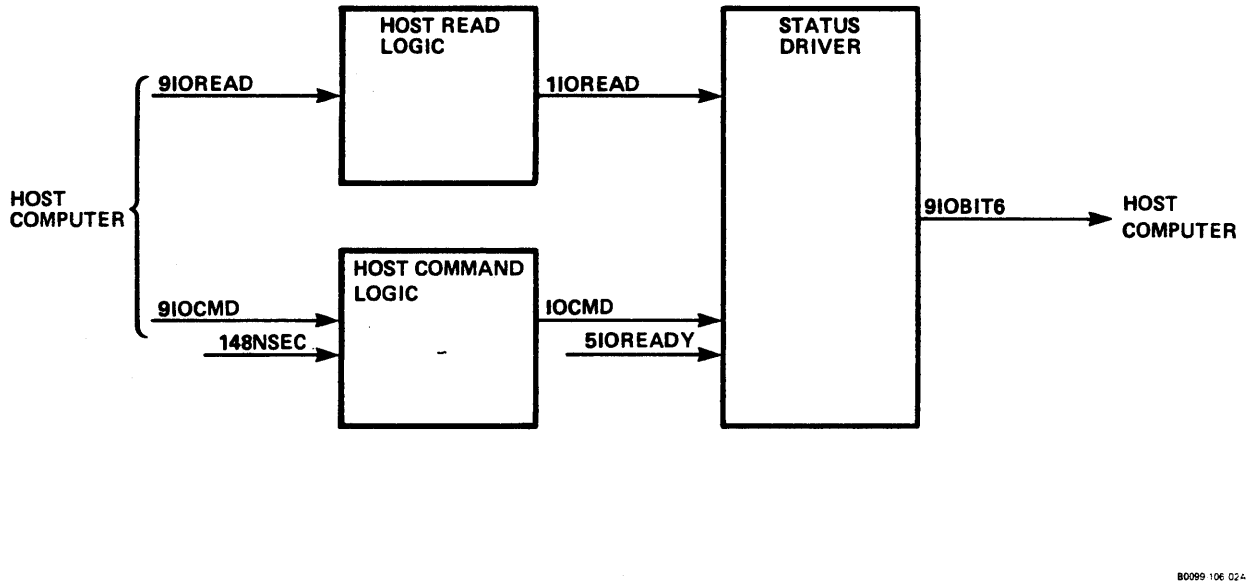


Figure 4-18. 9465 Status Readout

The host read logic inverts 9IOREAD to become 1IOREAD and the host command logic inverts 9IOCMD to become IOCMD at the next 148NSEC clock pulse. When 1IOREAD and IOCMD go active, the status driver converts 5IOREADY into 9IOBIT6, which goes to the host.

4.5.2.d.1.b Host data input. When the 9465 is ready, the host sends data on 9IOBIT0-15 (figure 4-19) and sends 9IOWRT. The host write logic inverts 9IOWRT to become IOWDAT at the next 148NSEC clock pulse, and IODAT latches the data received into the interface data bus buffer. At the following *148NSEC pulse, the host status register converts IOWDAT into IFWRITE.

4.5.2.d.1.c Status read control. The CPU routinely polls the 68000 data bus controller to read host status. To develop a read control signal, the CPU sends a control byte to the 68000 bus address decoder (figure 4-20) on A6-8 and A17-23; the control byte is followed by 5AS. The decoder then accepts the byte and derives 5PIO2EN. The CPU also sets 5LDS active and transmits a read status byte on A1-5.

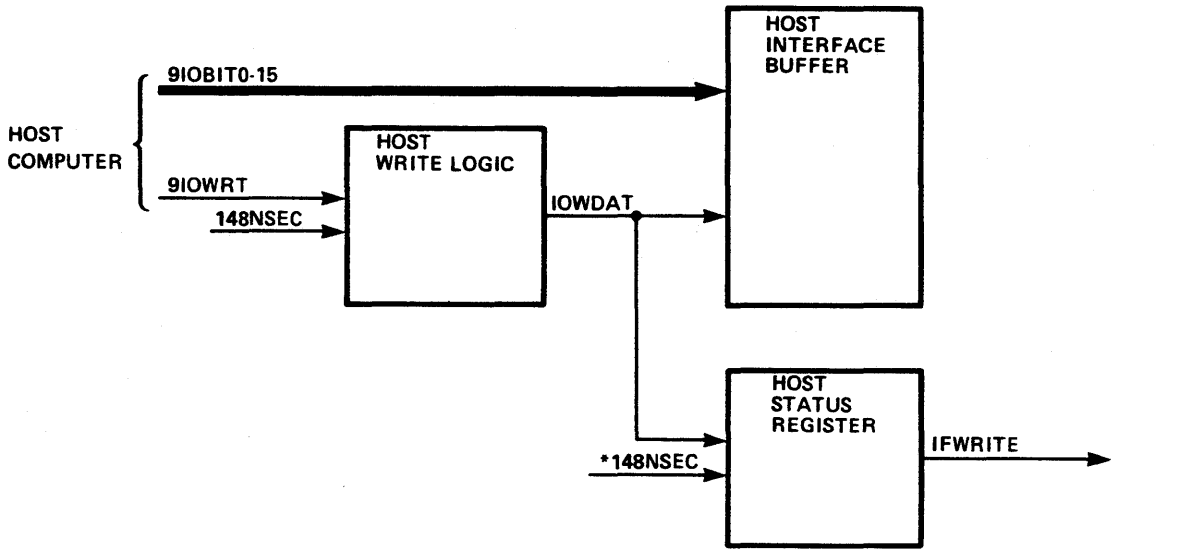


Figure 4-19. Host Data Input

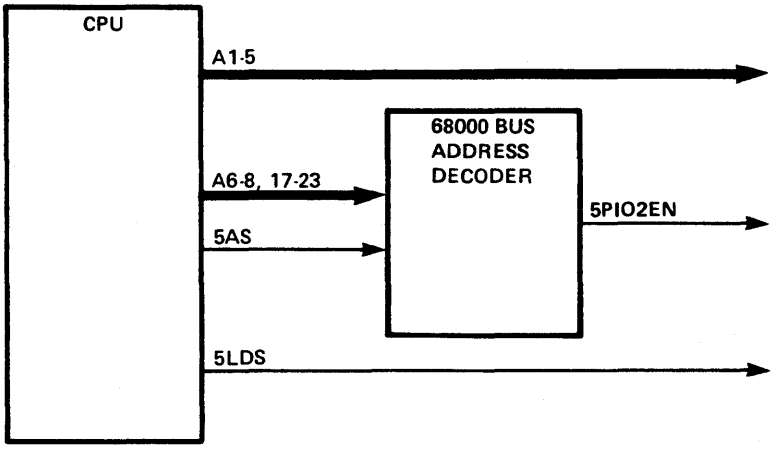


Figure 4-20. Status Read Control

4.5.2.d.1.d Host status readout. The 68000 data bus controller receives the read status byte on A1-5 (figure 4-21), signal IFWRITE from the host status register, and signals 5PIO2EN and 5LDS. When 5PIO2EN and 5LDS go active, the controller transfers IFWRITE to line D1, which goes to the CPU to inform the CPU that the host computer is sending data.

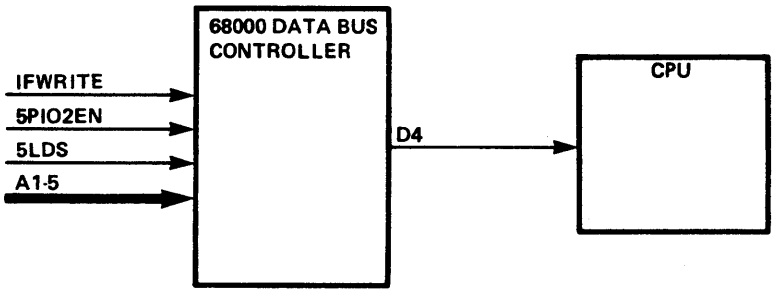


Figure 4-21. Host Status Readout

4.5.2.d.1.e Data transfer control. To develop the necessary control signals, the CPU sends 5AS and a control byte on A1-23 to the 68000 bus address decoder (figure 4-22), which decodes the byte to derive signals 5IOEN and 5SYSADR. At the first 148NSEC clock pulse after 5SYSADR goes active, the display bus tester-controller performs a complete testing sequence. If the bus is not in use, 5ENADR and 1ENCONTL go active.

4.5.2.d.1.f Data read control. To develop a read control signal, the CPU transmits a control byte on A1-8, and activates signals 5AS and 5RD (figure 4-23). When 5ENADR goes active, the display address bus driver transfers the control byte from A1-8 to 4BADR0-7. When signals 1ENCONTL, 5IOEN, 5AS, and 5RD go active, the display control bus driver converts 5IOEN and 5RD into 9BIORQ and 9BREAD. When 9BIORQ and 9BREAD go active, the display address bus decoder decodes the control byte on 9BZADR0-7 to derive signal 7RDIFDAT.

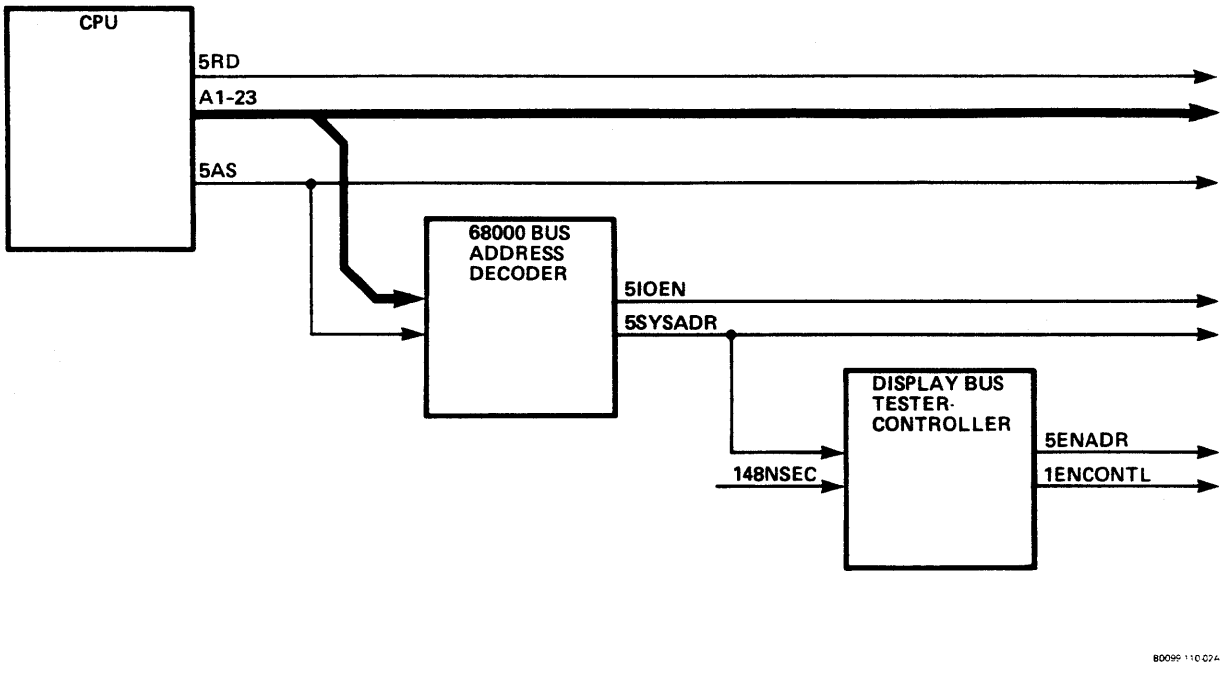


Figure 4-22. Data Transfer Control

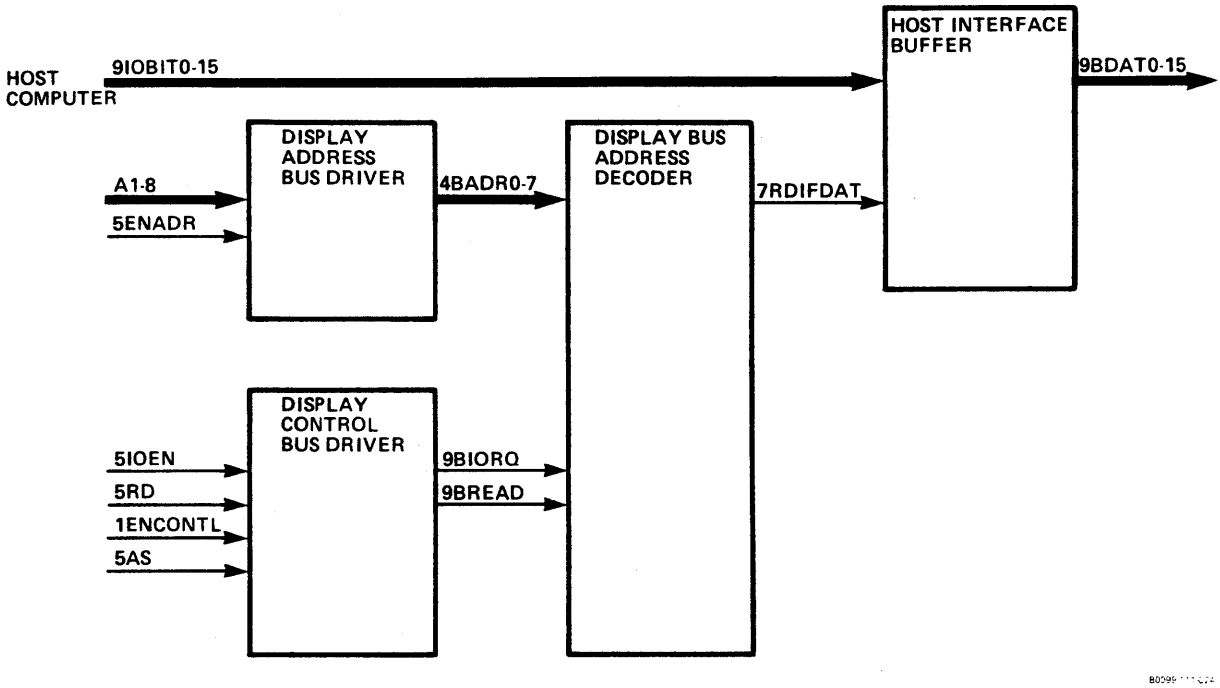


Figure 4-23. Data Read Control

4.5.2.d.1.g Host data transfer. When signals 5ENADR and 5SYSADR go active (figure 4-24), the buffer control logic activates 5RW68. When 7RDIFDAT goes active, the interface data bus buffer transmits the latched data from the host computer on 9BDAT0-15. When 5RW68 goes active, the 68000 data bus buffer transfers the host computer data on 9BDAT0-15 to D0-15, which go to the CPU.

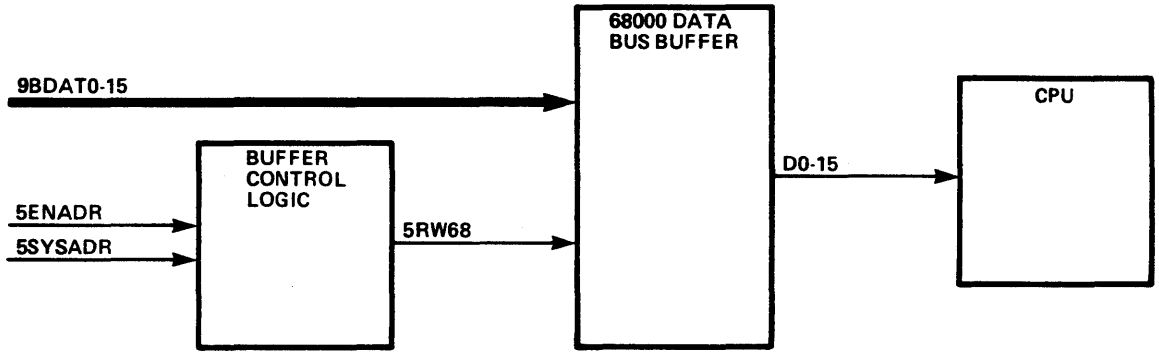


Figure 4-24. Host Data Transfer

4.5.2.d.1.h Data storage. The CPU typically stores received data in the 68000 RAM. To initiate a write cycle, the CPU sends a control byte to the 68000 bus address decoder on A17-23 (figure 4-25), followed by 5AS. The decoder then decodes the byte to derive 5RAMEN, which goes to RAM and the RAM controller. The CPU also sends 5WR to RAM and an address on A1-23 to the controller. RAM then sends 5RAMWR to the controller, which converts the received address into bits DA0-7 and either 5RAS0 or 5RAS1. When RAM receives 5WR from the controller, and 5LDS, 5UDS, or both from the CPU, RAM stores data from the CPU on D0-15 in the address specified by DA0-7, 5CAS, and either 5RAS0 or 5RAS1 from the controller. When the cycle is complete, the controller sends 5XACK to the transfer control logic, which also receives 5RAMEN and generates 5DTACK to inform the CPU that the cycle is complete.

4.5.2.d.1.i RAM readout. To initiate a read cycle, the CPU sends a control byte to the 68000 bus address decoder on A17-23 (figure 4-26) followed by 5AS. The decoder then derives 5RAMEN, which goes to RAM and the RAM controller. The CPU also sends 5RD to RAM and an address on A1-23 to the controller. RAM then sends 5RAMRD to the controller, which converts the received address into bits DA0-7 and either 5RAS0 or 5RAS1. When RAM subsequently receives 5XACK from the controller, RAM sends to the CPU (on D0-15) the data stored in the address specified by DA0-7, 5CAS, and either 5RAS0 or 5RAS1.

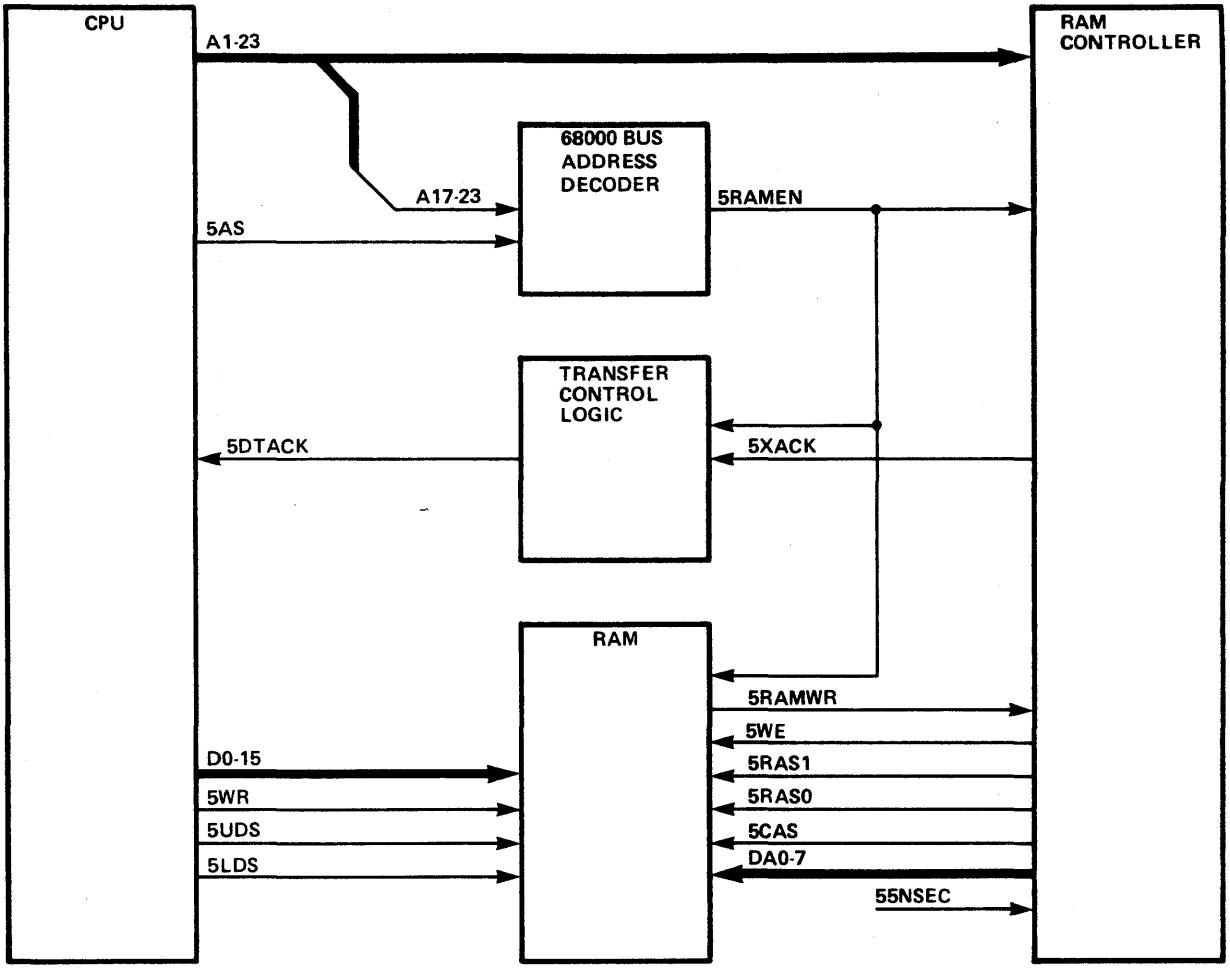


Figure 4-25. Data Storage

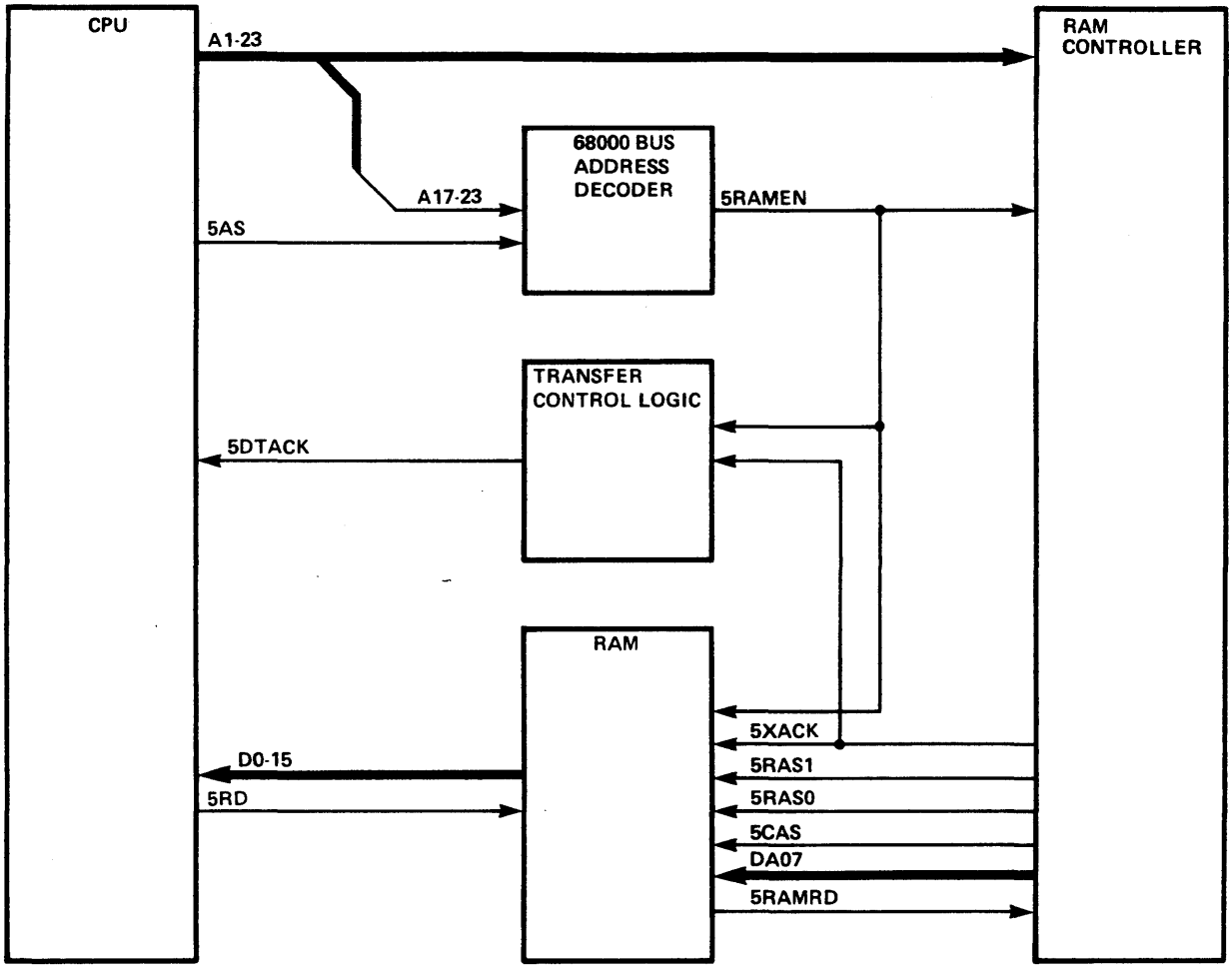


Figure 4-26. RAM Readout

Signal 5XACK also goes to the transfer control logic, which also receives 5RAMEN and generates 5DTACK to inform the CPU that the read cycle is complete.

4.5.2.d.1.j ROM readout. To access program data from ROM, the CPU sends a control byte to the 68000 bus address decoder on A17-23 (figure 4-27), followed by 5AS. The decoder then decodes the byte to derive 5ROMEN. The CPU also sends 5RD and an address on A1-17 to ROM. When 5ROMEN and 5RD go active, ROM sends to the CPU, on D0-15, the data stored in the address specified by A1-17.

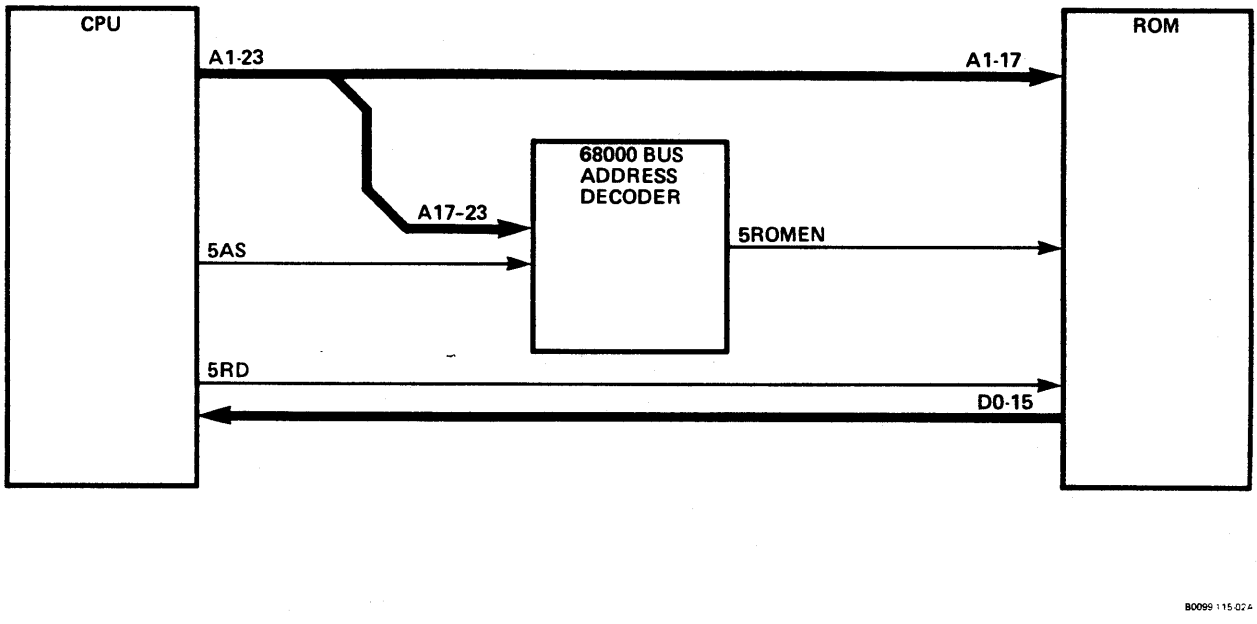


Figure 4-27. ROM Readout

4.5.2.d.1.k Output control. After processing the data from the host computer, the CPU sends the processed data to the MCP on the display bus. To generate the necessary control signals, the CPU sends a control byte to the 68000 bus address decoder on A1-8 and A17-23 (figure 4-28), followed by 5AS. The decoder then decodes the byte to derive 5SYSADR. After 5SYSADR goes active, the display bus tester-controller performs a complete testing sequence. If the bus is not in use, 5ENADR goes active.

4.5.2.d.1.l Data output. When signals 5SYSADR and 5ENADR go active, the buffer control logic generates 5RW68 (figure 4-29). When 5WR from the CPU and 9RW68 go active, the 68000 data bus buffer transfers data from the CPU on D0-15 to 9BDAT0-15, which go to the MCP. The CPU also transmits the MCP address on A1-8. When 5ENADR goes active, the display address bus driver transfers the address on A1-8 to 4BADR0-7, which go to the MCP.

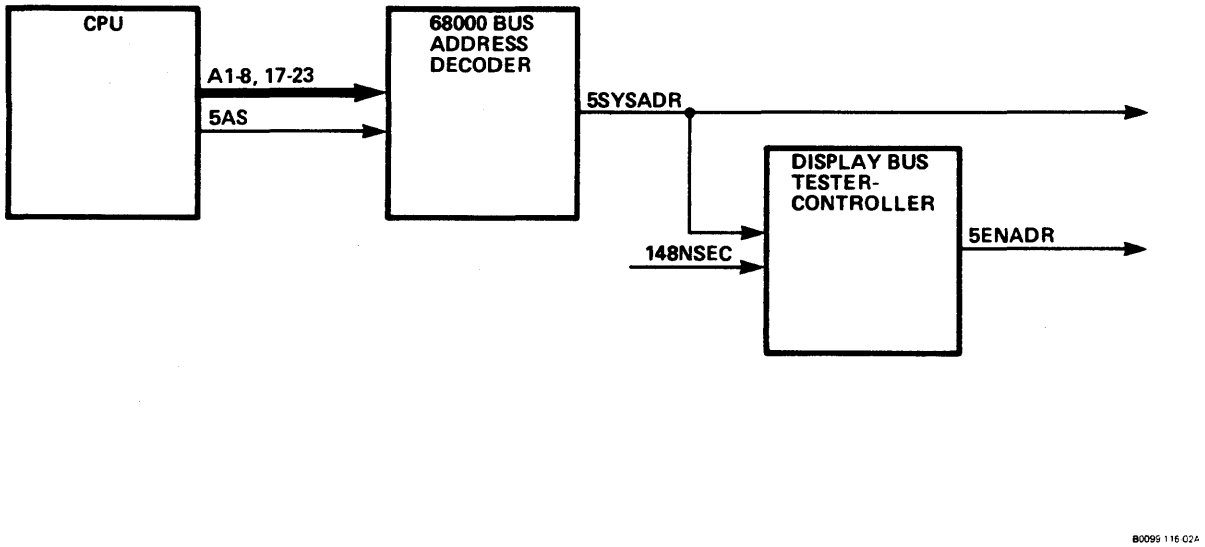


Figure 4-28. Output Control

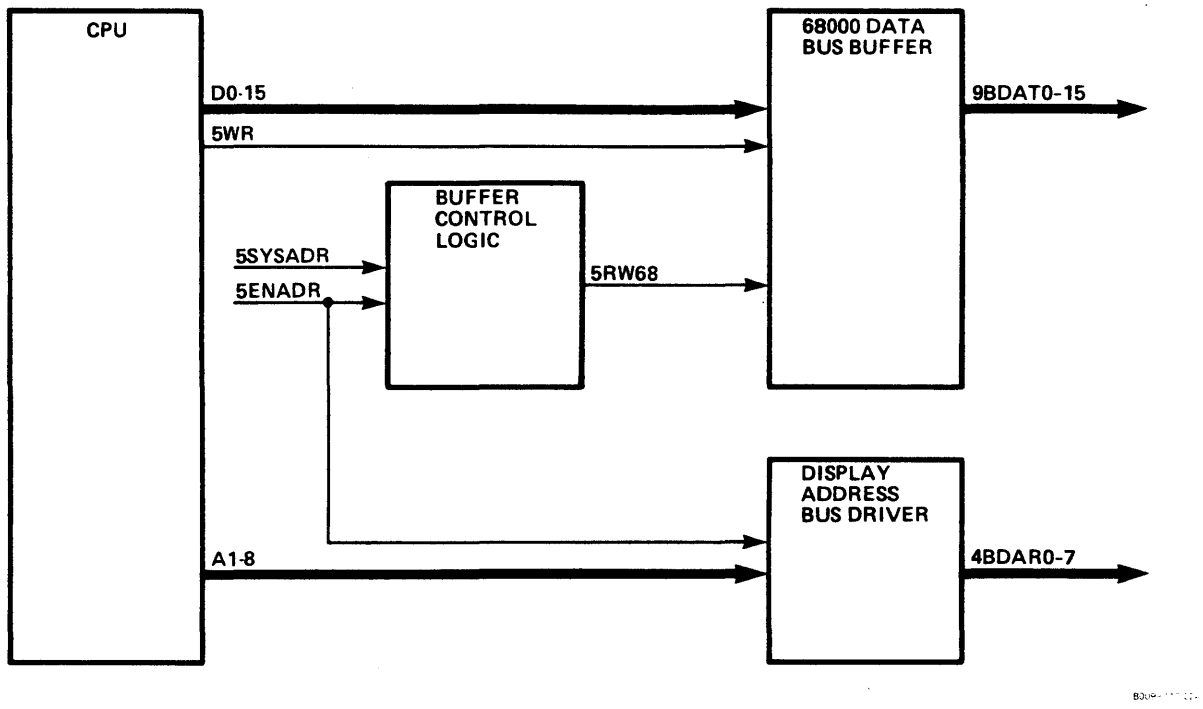


Figure 4-29. Data Output

4.5.2.d.2 Keyboard data flow. Depending upon user requirements, a 9465 is configured with or without a serial link PCB. In the latter instance, a keyboard connects directly to the system processor PCB (Z80).

4.5.2.d.2.a Direct keyboard connection. A typical keyboard operation consists of these steps:

- Z80 interrupt request
- Vector transfer
- Keyboard data transfer
- Data transfer to Z80 Data Bus Controller
- Data transfer to 68000 Data Bus Controller
- Data transfer to CPU

When the keyboard sends data to the serial peripheral I/O controller on RD1 and *RD1 (figure 4-30), the controller sends interrupt request signal 5INT to the Z80 serial I/O processor. When ready to accept data, the processor activates signals 5M1 and 5IORQ to signal an interrupt acknowledge.

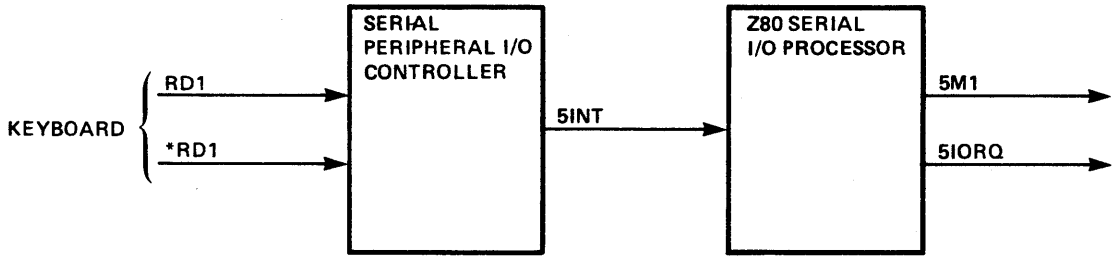


Figure 4-30. Z80 Interrupt Request

After receiving signals 5M1 and 5IORQ, the serial peripheral I/O controller sends a vector to the Z80 serial I/O processor on ZD0-7 (figure 4-31) to identify the controller as the interrupt source. The processor then activates signals 5IORQ and 5RDZ and sends a control byte on ZA0-7 to the Z80 address decoder, which decodes the byte to derive 5SIO1EN.

The serial peripheral I/O controller (figure 4-33) receives signals 5SIO1EN, 5IORQ, and 5RDZ. When these signals go active, the controller converts the

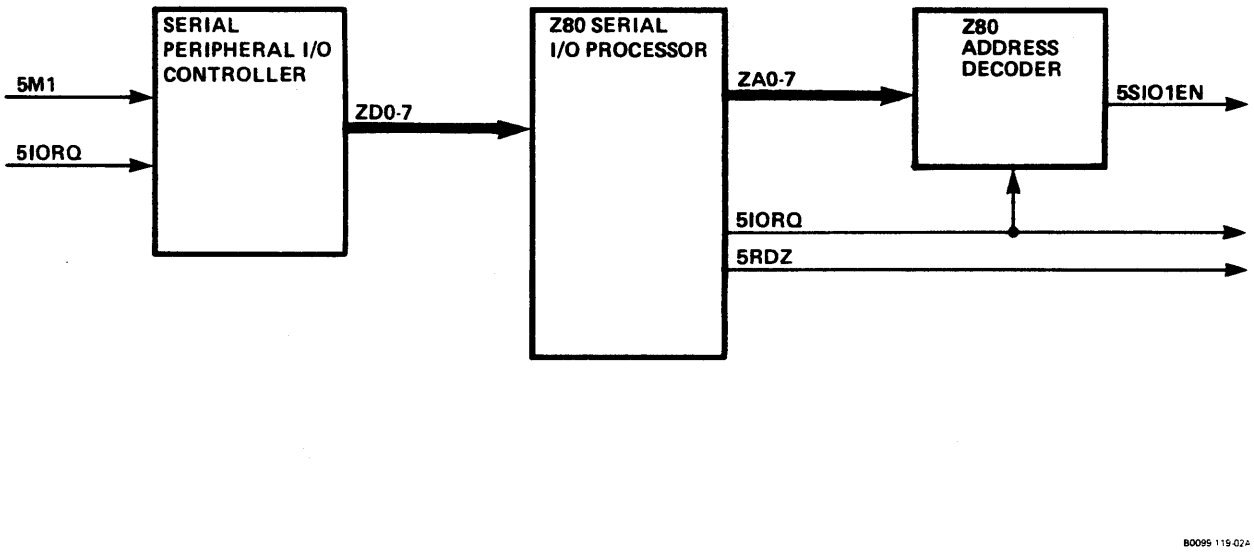


Figure 4-31. Vector Transfer

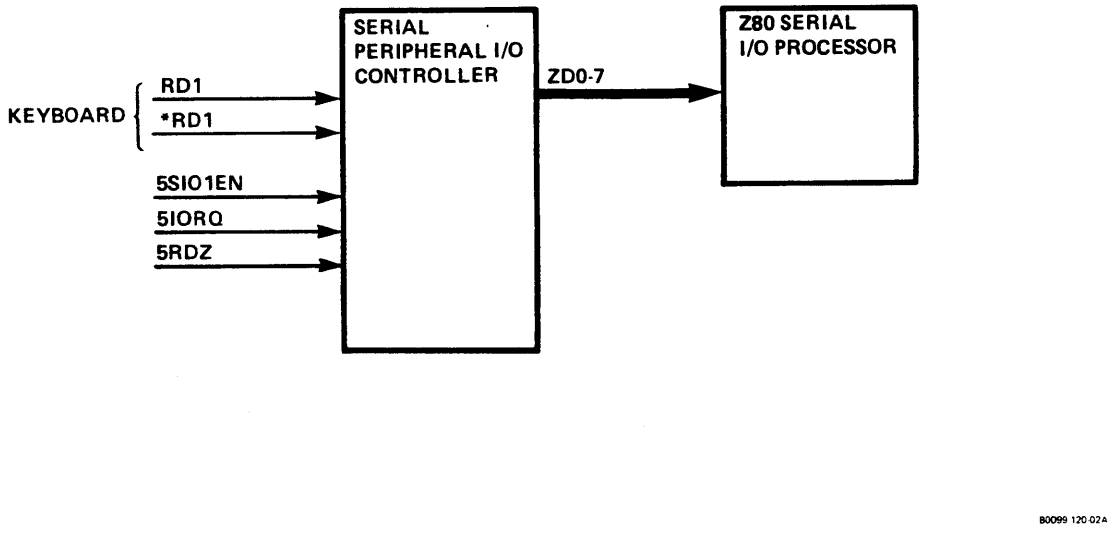


Figure 4-32. Keyboard Data Transfer

serial keyboard data into parallel form and sends the parallel data to the Z80 serial I/O processor on ZD0-7.

The Z80 serial I/O processor sends a control byte to the Z80 address decoder on ZA0-7 (figure 4-33) followed by signal 5IORQ, which also goes to the Z80 data bus controller.

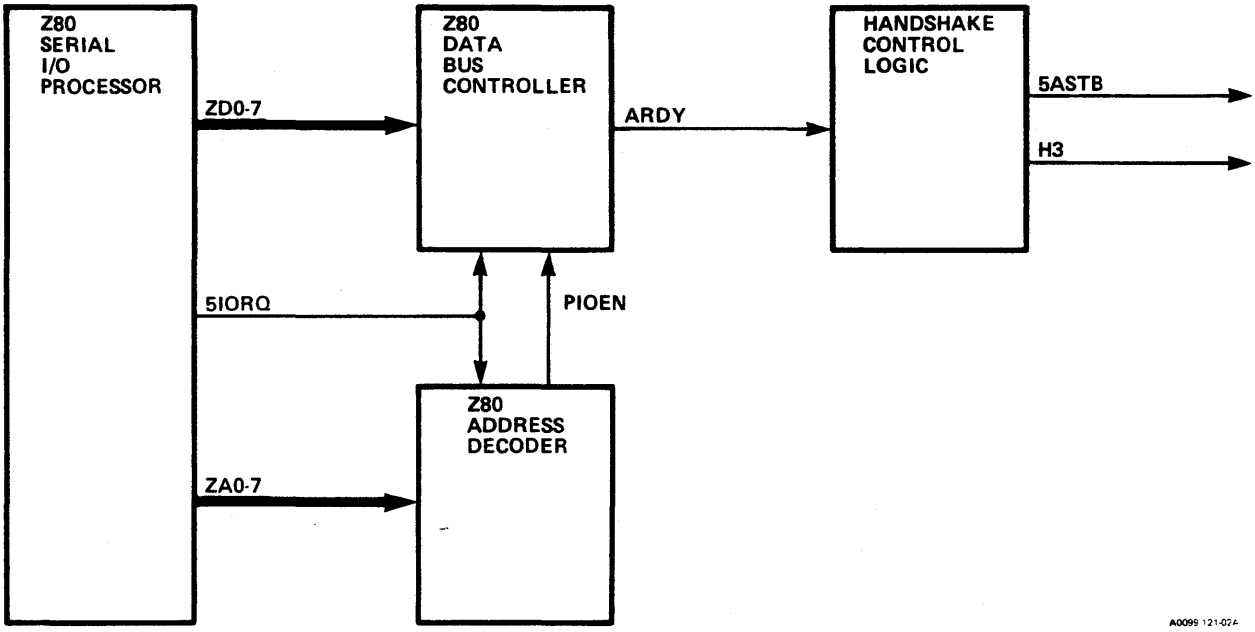


Figure 4-33. Data Transfer to Z80 Data Bus Controller

The decoder then decodes the byte to derive PIOEN. When PIOEN goes active, 5IORQ latches data from the processor on ZD0-7 into the controller, which then sends ARDY to the handshake control logic. If the 68000 data bus controller is ready to accept data, the logic activates 5ASTB followed by H3.

When 5ASTB goes active, the Z80 data bus controller sends the latched data to the 68000 data bus controller (figure 4-34). Signal H3 latches the data into the 68000 data bus controller, which then sends interrupt request PIRQ to the interrupt priority generator. At the next 148NSEC clock pulse, the generator transmits an interrupt request byte on IPL0-2.

The CPU receives the interrupt request byte on IPL0-2 (figure 4-35) and responds, when ready, by activating signals 5AS and 5LDS and sending a control byte on A6-8 and A17-23 to the 68000 bus address decoder, which decodes the byte to derive 5PIO2EN. The CPU also sends a read data byte on A1-5 to the 68000 data bus controller, which also receives 5PIO2EN and 5LDS, and responds by sending the latched data to the CPU on D0-15. The CPU then sends the data to the MCP in the same way as host computer data.

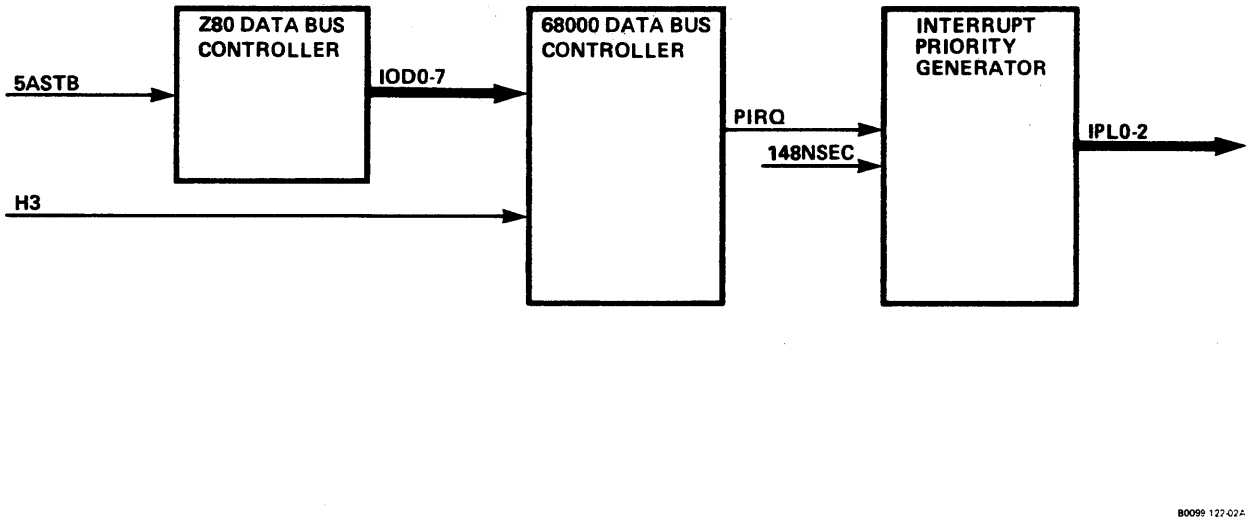


Figure 4-34. Data Transfer to 68000 Data Bus Controller

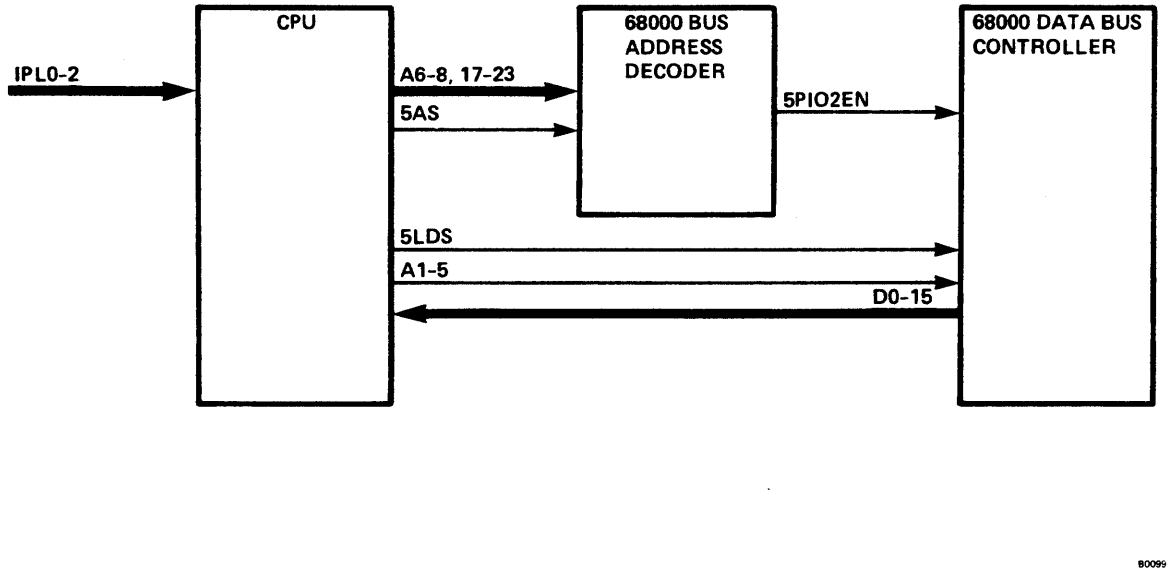


Figure 4-35. Data Transfer to CPU

4.5.2.d.2.b Indirect keyboard connection. When a serial link PCB is installed in the 9465, the keyboard interfaces with the serial link PCB, and the system processor PCB receives keyboard data from the serial link PCB. A typical remote keyboard operation consists of these steps:

- Remote interrupt request
- Remote vector transfer
- Remote read control
- Remote data transfer

The serial link PCB receives data from the keyboard and sends interrupt request 9BZINT to the system processor PCB on the processor bus. The Z80 serial I/O processor receives 9BZINT (figure 4-36) and responds, when ready, by activating signals 5IORQ and 5M1 to signal an interrupt acknowledge. The processor control bus driver converts 5IORQ and 5M1 into 9BZIORQ and 9BZM1, respectively, which go to the serial link PCB.

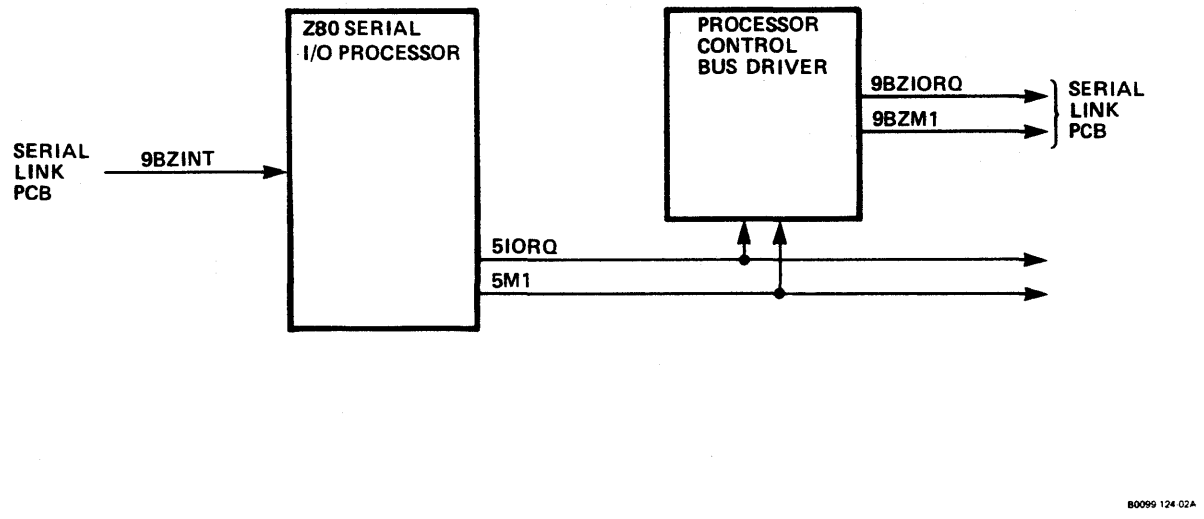


Figure 4-36. Remote Interrupt Request

After receiving 9BZIORQ and 9BZM1, the serial link PCB sends a vector to the system processor PCB, on 9BZDAT0-7, to identify the interrupting source. When signals 5IORQ and 5M1 go active, the Z80 data bus buffer (figure 4-37) transfers the vector on 9BZDAT0-7 to ZD0-7, which go to the Z80 serial I/O processor.

To read remote keyboard data the Z80 serial I/O processor activates signals 5IORQ and 5RDZ and transmits an address on ZA0-7 (figure 4-38). The processor address bus driver transfers the address from lines ZA0-7 to 4BZADR0-7, which go to the serial link PCB. The processor control bus driver converts 5IORQ

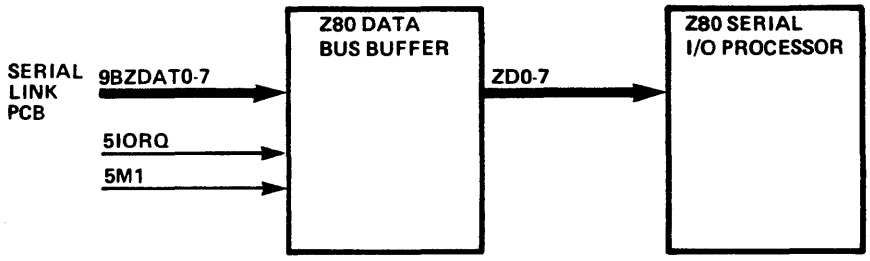


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Figure 4-37. Remote Vector Transfer

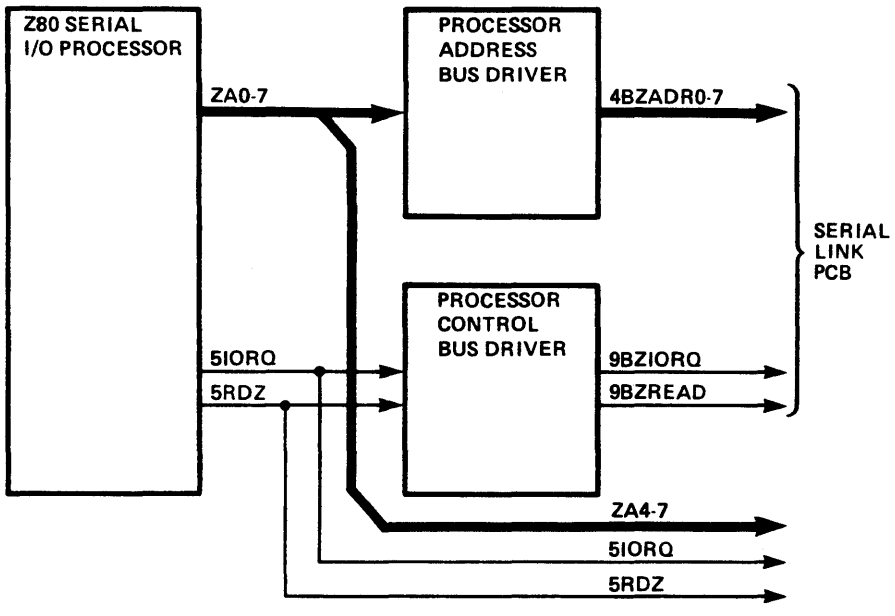

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Figure 4-38. Remote Read Control

and 5RDZ into 9BZIORQ and 9BZREAD, respectively, which also go to the serial link PCB.

After receiving signals 9BZIORQ and 9BZREAD and the address on lines 4BZADR0-7, the serial link PCB sends keyboard data on ZD0-7 (figure 4-39). When the Z80 data bus buffer receives signals 5IORQ and 5RDZ and address bits ZA4-7, the buffer transfers the data on lines 9BZDAT0-7 to ZD0-7, which go to the Z80 serial I/O processor. The processor then sends the data to the MCP in the same way as host computer data.

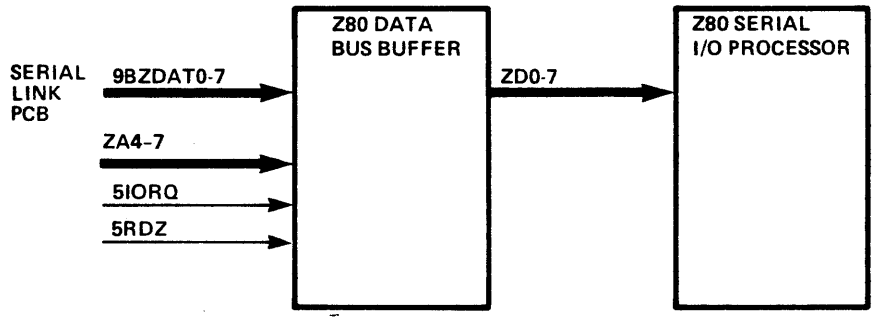

Figure 4-39. Remote Data Transfer

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4.5.3 MCP PCB

The MCP PCB (figure F04-13) has five functional elements:

- Interface logic
- Input-output logic
- Bit-slice microprocessor (BSM)
- Memory timing sequencer (MTS)
- Zoom-pan-refresh (ZPR) logic

The interface logic controls communications between the BSM and the system backplane assembly. Input-output logic routes data to and from display bus 9BDAT 0-15, memory bus 9DGD 0-15, and internal bus PTD0-15. The BSM controls refresh memory. The MTS executes one of eight memory operations on command from the BSM. The ZPR logic generates zoom, pan, screen refresh, and memory refresh control signals.

4.5.3.a Interface Logic. Depending upon configuration ordered, a 9465 can have up to three MCP PCBs. Select lines 4BSEL0-2, hardwired on the backplane assembly, assign an address to an MCP depending on backplane assembly slot position. The system processor selects an MCP via address lines 4BADR0-7.

Read signal 9BREAD and write signal 9BWRT start memory read and write operations controlled by the MCP. The interface logic generates buffer full signal BFULL and read MCP signal *RDMCP during read operations and buffer empty signal BEMPTY during write operations. Wait signal WAIT sets 9BWAIT active, preventing further read or write operations until the present one is completed. Operation done signal *DONE drives BFULL or BEMPTY inactive when the current operation is finished. Direct memory access (DMA) control signals *BUSY and DMA drive ready signal BREADY active when the BSM is ready for a DMA read or write operation.

One of data lines 9BDAT0-7 is a status read and common data port select on each MCP. Status bit signal PL52 sends the BSM status to the system processor during a status read.

Reset signal *RESET from the ZPR logic causes the interface logic to issue a *CLEAR signal immediately and a *QCLEAR signal on the next MCP clock cycle. Clear signal *CLRIO clears the interface logic handshake circuits that generate BFULL and BEMPTY.

4.5.3.b Input-Output Logic. Buffer-drivers route clock signals TMCQ, TFQ, and THQ to the rest of the MCP. Bus translators connect memory bus 9DGD0-15 with MCP internal bus PTD0-15. The BSM controls transfers between these buses with *DRVIN and *DRVOUT.

The packing logic transfers data between display bus 9BDAT0-15 and memory bus 9DGD0-15. The BSM controls the data, using *REVHI and *REVLO to swap high and low data bytes and *LXHI and LXLO to latch data. Data in signal *PAKIN loads display bus data onto the memory bus. Read signal *RDMCP loads memory bus data onto the display bus.

4.5.3.c Bit-slice Microprocessor. The BSM (figure FO4-14) has five functional elements:

- Controller logic
- Microprogram memory
- Pipeline registers
- Arithmetic logic unit (ALU)
- Decoder logic

The controller logic addresses microprogram memory and controls BSM operation. Microprogram memory stores microprogram instructions that control the MCP. Pipeline registers store microprogram instructions between the microprogram memory and the ALU. This scheme makes the BSM run faster. Data from internal bus PTDO-15 is manipulated by the ALU under microprogram memory control. Decoder logic converts coded outputs from the pipeline registers into control signals routed to the controller logic, the ZPR logic, and the system backplane assembly.

4.5.3.c.1 Controller logic. System resolution signals 4H*MX, 4H*MY, 4L*MY, and 4MY*559, hardwired on the backplane assembly, and interlace signal 8INTLC configure the controller logic. Select signal *INT512 controls a screen refresh bit on the ZPR logic. Control signal BRDCST enables the MTS screen refresh timing circuit. 9lear signal *QCLEAR clears the controller logic restart-next instruction register. The restart-next instruction register stores instruction word bits PL18-21 from the microprogram memory.

The sequence controller monitors status signals and selects the current BSM instruction from the microprogram memory with address signals CMADO-10. Instruction word signals PLO-11 and internal bus signals PTDO-15 provide the next instruction address to the sequence controller. The sequence controller monitors interface logic status signals BFULL and BEMPTY; ALU status signals ALUN, ALUZ, and ALUC; MTS graphic detect mode signal GRDET; and handshake signal IOCMPL. Multiplex control signals CSELO-3, *TSTCC, and *CCINV select the status signals for the sequence controller.

The controller logic stores data from internal bus PTDO-15 in a scratchpad RAM. Read signal *RDRAM, increment address signal *INCRAD, write signal *WRRAM, and address load signal *LDRAD control the scratchpad RAM read, write, and address functions. Control signals DISREG and RASDAT define scratchpad RAM contents as either foreground or background display data.

The packing control logic generates control signals for the input-output logic. Enable signal *ENPAKC, reverse latch signal TLXLH, reverse byte swap signal TREVLH, clear signal *CLEAR, and load signal *LDPAKC control the loading and manipulation of data onto internal bus PTDO-3. High and low byte latch signals *LXHI and *LXLO, and high and low byte swap signals *REVHI and *REVLO control data loading on the input-output logic.

Raster control logic performs the raster scaler function. Load signal *REPREG loads data from internal bus PTDO-7 into the raster control register. Load signal *REPCNT loads the raster control counters. Enable signal *ENSHIFT enables the raster control counters.

The update-write logic controls display and vector updates, background-foreground switching, graphic detect mode, and DMA operations. Load signals *LDOCT and *LDUPWR latch data from internal bus PTD0-7 into the update-write logic. Update direction signals PLUSX, MINUSX, PLUSY, AND MINUSY control operations on the MTS. Graphic detect signal GRMODE puts the MTS into the graphic detection mode. Enable signals *ENGRDET and *ENDGWE route graphic detection and memory write signals from the MTS to the BSM and the backplane assembly, respectively. Direct memory access signal DMA enables the DMA handshake circuit on the interface logic during DMA operations.

4.5.3.c.2 Microprogram memory. When addressed by CMAD0-10, the microprogram memory outputs a 56-bit instruction word to the pipeline registers, the controller logic, and the interface logic. Load signals *LDCR0, *LDCR1, and *LDOR respectively load:

- Instruction word bits PL0-11 and PL40-47 into the ALU instruction register
- Instruction word bits PL40-47 into the MTS control register
- Output register to internal bus PTD0-15

Condition select signals CSEL0-2 route BSM condition status signals to the controller logic. Condition invert signal *CCINV complements the condition status signals. Status signal PL52 sends BSM status to the interface logic.

4.5.3.c.3 Pipeline register. The pipeline register latches instruction word bits PL0-11,16,17, and 22-51 from the microprogram memory. Control signals ALA0-3, ALB0-3, and ALI0-8, and clock enable signal *ENALCK control the ALU. Load signals *LDCR0, *LDCR1, and *LDOR latch instruction word bits PL0-11 and PL40-47 into the ALU instruction register, and instruction word bits PL40-47 into the MTS control register and the output register to internal bus PTD0-15, respectively.

Coded instructions CDS0-2, CDE0, and CDE1 provide 19 additional control signals. Output drive signal *DRVOUT loads data from internal bus PTD0-15 to memory bus 9DGD0-15. Input drive signal *DRVIN loads data from memory bus 9DGD0-15 to internal bus PTD0-15. Input packing signal *PAKIN loads data from display bus 9BDAT0-15 to memory bus 9DGD0-15.

Operation code signals MTSOP0-2 select one of eight MTS operations. Address signals UB0-3, and RAM select signal *IPSEL control MTS RAM addressing. Read-back enable signal CRBDEN controls MTS RAM read operations. Handshake signal *STEALIT disables the MTS control register until the MTS completes the current operation.

Busy signal *BUSY controls DMA operations to the display bus, along with DMA enable signal DMA from the controller logic. Wait signal WAIT prevents the system processor from requesting a new operation until the BSM finishes the current operation. Operation done signal *DONE clears the interface logic buffer status registers after each read or write operation.

Condition test signal *TSTCC and condition select signal CSEL3 enable the controller logic status-monitoring logic. Read signal *RDRAM and increment address signal *INCRAD operate the controller logic scratchpad RAM, along with write signal *WRRAM and load address signal *LDRAD from the decoder logic.

Display register signal DISREG defines the scratchpad RAM as the foreground-background register.

Enable signal *ENPAKC routes packing control signals from the controller logic to the input-output logic. Latch reverse signal TLXLH and byte swap reverse signal TREVLH complement the latch and byte swap signals from the controller logic to the input-output logic.

4.5.3.c.4 Arithmetic logic unit. The ALU reads data from internal bus PTD0-15, manipulates the data, and returns the data to the bus. Control signals ALA0-3, ALB0-3, and ALI0-8, and clock enable signal *ENALCK control ALU operation. Status signals ALUN, ALUZ, and ALUC report ALU status to the controller logic. Raster data signal RASDAT selects the foreground or background address from the controller logic scratchpad RAM.

4.5.3.c.5 Decoder logic. The decoder logic generates additional commands from coded instructions CDS0-2, CDE0, and CDE1. Disable signal 9DSEL resets selected memory groups via the backplane assembly. Latch signal 9C/L latches plane mask data onto memory PCBs via the backplane assembly. Signal 9GEN is not used in the 9465.

Zoom load signals *LDYZM and *LDXZM and origin load signals *LDYORG and *LDXORG load ZPR logic registers. Clear signal *CLRIO clears the interface logic buffer status registers. Write signal *UWE enables the MTS RAM during write operations.

Load signal *LDPAKC loads data from internal bus PTD0-3 into the controller logic packing control circuit. Latch signal *INSTLX latches data from internal bus PTD4-7 into the controller logic instruction register.

Write signal *WRRAM and load address signal *LDRAD operate the controller logic scratchpad RAM, along with read signal *RDRAM and increment address signal *INCRAD from the pipeline registers.

Load signals *LDOCT and *LDUPWR load data from internal bus PTD0-7 into the controller logic octant register and update-write register, respectively. Clear signal *CLRGD clears the controller logic graphic detect mode register.

Load signal *REGLD loads data from either internal bus PTD0-15 or instruction word bits PL0-11 into the controller logic sequence controller. Latch signal *REPREG clocks data from internal bus PTD0-7 into the controller logic raster control register. Load signal *REPCNT loads the controller logic raster control counter. Reset signal *RESET clears the selftest LED controlled by the decoder logic.

4.5.3.d Memory Timing Sequencer. The MTS (figure F04-15) has five functional elements:

- Control logic
- Microprogram memory
- Random-access memory (RAM)
- Arithmetic logic unit (ALU)
- Address registers

Control logic addresses microprogram memory and responds to requests for memory bus control. Microprogram memory stores instructions executed by the MTS. The RAM stores data from internal bus PTD0-15 for the ALU. The ALU manipulates data under microprogram memory control. The address registers store memory address data.

4.5.3.d.1 Control logic. Control request signal 9MBUSRQ requests control of the memory bus from the MCP. Request granted signal 9MBGRANT releases the memory bus to the requesting device when vertical memory signal 8TVMMM is active. Disable signal MBTRIST puts memory bus output circuits on the MCP into a high impedance state. Reset signal *RESET drives 9MBGRANT and MBTRIST inactive, returning control of the memory bus to the MCP.

Operation code signals MTSOP0-2, configuration signal 8SELX, and horizontal memory timing signal 8THMMM generate microprogram memory address signals MTSAD0-7 and high-speed erase signal 9HSERS. Load signal 5LDNWI and MTS control register enable signal *STEALIT load operation code signals MTSOP0-2 into the control logic. Address select signal 6ADSL, zoom status signals *YZOOM0 and *ZOOM0, horizontal blanking signal 8THBLK, and resolution signal BRDCST generate refresh control signals *MRMUX1 and MRMUX2, and MTS control register enable signal *STEALIT.

4.5.3.d.2 Microprogram memory. When addressed by MTSAD0-7, the microprogram memory outputs a 28-bit instruction word to the RAM, the ALU, the address register, the BSM, the ZPR logic, and the backplane assembly. Control signal *MRMUX2 enables refresh control signal 7ADSL.

The microprogram memory sends memory address control signals 9DRAS, 9DCAS, 9DADSL, and 9DMADSL, memory load signal 9DMLP, and readback control signals 9DRBL and 9DRBEN to the backplane assembly. Handshake signal IOCMPL notifies the BSM when the MTS completes an operation. Refresh control signals 5LCOUNT, 4MADSL, 7ADSL, and 7MADSL control the ZPR logic.

Address signals ADDRA0-2, APADD3, and PORTB0-3 address RAM ports A and B, and select the column or row address register. Write signal 5WRCOP writes data from the ALU to the address register. Control signals FNCTN0-3, 5COUNTLP, 6COUNTLP, 5WE1, and *MWREN control ALU operation. Write signal 5WE1 controls RAM write operations, together with 5WE2 from the ALU. Latch signal 5NLATCH latches data at the RAM outputs.

4.5.3.d.3 Random access memory. Address signals ADDRA0-2 and APADD3 address RAM port A. Address signals PORTB0-3 and UB0-3 address port B. Output port signals APD0-15 and BPD0-15 send data to the ALU. The RAM stores data from internal bus PTD0-15 and ALU outputs ALUDAT0-15. Write signals 5WE1 and 5WE2 together control memory write operations. Latch signal 5NLATCH latches data from the addressed location in memory to output ports A and B.

Select signal *IPSEL allows the BSM to write data from internal bus PTD0-15 into the memory location addressed by UB0-3. Enable signal *CRBDEN allows the BSM to read data from the RAM on internal bus PTD0-15. Graphic detect signal GDMODE puts the MTS into the graphic detect mode.

4.5.3.d.4 Arithmetic logic unit. The ALU manipulates data outputs APD0-15 and BPD0-15 from the RAM. Update direction signals PLUSX, MINUSX, PLUSY, and MINUSY, and control signals FNCTN0-3 control ALU operation.

Counter load signals 5COUNTLP and 6COUNTLP, write enable signal 5WE1, memory write enable signal *MWREN, graphic detect enable signal *ENGRDET, high-speed erase signal 9DHSERS, and memory write enable signal *ENDGWE generate memory write signal DMWR and graphic detect signal GRDET. Write signal DMWR controls memory PCB write operations. Graphic detect flag signal GRDET notifies the BSM when the current operating point reaches a boundary.

4.5.3.d.5 Address register. The address register stores the column (X-axis) and row (Y-axis) memory read-write addresses. Address signals PORTB0-2 and write signal 5WRCOP load data outputs ALUDAT0-10 into the address register.

Column and row addresses RWCOL0-7 and RWROW0-7 address the memory PCB during read and write operations. Write signal 9DMWR controls write operations on the memory PCB. Address strobe signals 9DAS0-4 strobe the row addresses into the memory PCB together with 9DRAS. Reset signal MBTRIST puts the 9DMWR and 9DAS0-4 outputs in a high impedance state when another device controls the memory bus.

4.5.3.e Zoom-Pan-Refresh Logic. The ZPR logic (figure FO4-16) has four functional elements:

- Line control logic
- Element control logic
- Buffer logic
- Refresh multiplexer logic

Line control logic generates row (Y-axis) address signals for the refresh multiplexer logic and puts out a zoom status signal for the MTS. Element control logic generates column (X-axis) address signals for the refresh multiplexer logic, zoom control signals for the video PCB, and a zoom status signal for the MTS. Buffer logic routes timing signals from the backplane assembly to MCP functional elements. Refresh multiplexer logic generates memory address signals and zoom control signals for the memory PCB.

4.5.3.e.1 Line control logic. Load signals *LDYZM and *LDYORG load line zoom and origin registers with data from internal bus PTD0-15. Reset signal *RESET resets the line zoom register. Interlace signal *INT512 controls screen refresh signals SRC0L6 and SRROW7. Zoom signal *YZOOM0 indicates Y-axis zoom status. Timing signals TVBBB, 8TVFFF, 8INTLC, 8TVMMM, and 8THMMM synchronize line control logic operation with the video display. The screen refresh line counter generates screen refresh signals SRROW0-6 and SRC0L5.

4.5.3.e.2 Element control logic. Load signals *LDXZM and *LDXORG load element zoom and origin registers with data from internal bus PTD0-15. Reset signal *RESET resets the element zoom register. Enable signal 5LCOUNT enables the element zoom counter. Zoom signal *ZOOM0 indicates X-axis zoom status. Timing signals 8THMMM and 8THBLK synchronize element control logic operation with the video display. Zoom control signals 9DZOOM, 9DZOOM0, and 9DSTRTCH control zoom operations on the video PCB. Control signals 9DSRLP, 9DSRHP, and

9RFW control screen refresh and zoom operations on the memory PCB. The screen refresh element counter generates screen refresh signals SRCOL0-4 and SRCOL7.

4.5.3.e.3 Buffer logic. The buffer logic reclocks system resolution signals 9SELX and 9INTLC, system timing signals 9TVFFF, 9TVBBB, 9TVMMM, 9THBBB, and 9THMMM, and power-on reset signal 9BPORCLR.

4.5.3.e.4 Refresh multiplexer logic. Select signals 7ADSL and 7MADSL control the multiplexing of screen refresh addresses SRROW0-7 and SRCOL0-7, and read-write addresses RWROW0-7 and RWCOL0-7. Refresh control signal MRMUX1 and address select signal 4MADSL enable the memory refresh counter. The refresh multiplexer logic routes read-write addresses RWROW0-7 and RWCOL0-7, screen refresh addresses SRROW0-7 and SRCOL0-7, or memory refresh counter outputs to the backplane assembly as memory address signals 9DAD0-7. Disable signal MBTRIST disables the refresh multiplexer logic outputs when the MCP releases control of the memory bus.

4.5.3.f Process Description. The MCP performs the following operations:

- Memory read
- Memory write
- Screen refresh
- Memory refresh
- Zoom
- Pan

Memory read operations place data from the memory PCB on memory bus 9DGD0-15 and transfer the data to display bus 9BDAT0-15. Memory write operations transfer data from display bus 9BDAT0-15 onto memory bus 9DGD0-15 and write the data into addressed locations on the memory PCB. Screen refresh operations address the memory data actually being displayed each time the CRT screen is scanned. Memory refresh operations address all the memory data regularly to maintain the data in dynamic RAMs on the memory PCBs. Memory refresh differs from screen refresh only during zoom operations when the memory data is not all being displayed. A zoom operation replicates pixels as they are projected from refresh memory onto the display screen. A pan operation moves the display from the original operating point to show parts of a picture outside the initial display window.

4.5.3.f.1 Memory read. The system processor starts a memory read operation by driving 9BREAD active and selecting the MCP with address signals 4BADDR0-7. Buffer status signal BEMPTY tells the BSM that the display bus is ready to receive data. The BSM sends a read operation code to the MTS on MTSOP0-2 and selects a specific memory PCB with 9DSEL and 9C/L. The MTS sends read address signals RWROW0-7 and RWCOL0-7, and multiplexer control signals 7ADSL and 7MADSL, to the ZPR logic. The ZPR logic multiplexes RWROW0-7 and RWCOL0-7 together and sends resulting address signals 9DAD0-7 to the memory PCB. The MTS strobes the row and column addresses into the memory PCB with 9DADSL, 9DCAS, 9DRAS, and 9DAS0-4 and puts the read data on memory bus 9DGD0-15 with control signals 9DRBL and 9DRBEN. The BSM latches the read data from memory bus 9DGD0-15 into the input-output logic with *LXHI and *LXLO. Interface logic read signal *RDMCP puts the read data on display bus 9BDAT0-15.

4.5.3.f.2 Memory write. The system processor starts a memory write operation by driving 9BWRT active and selecting the MCP with address signals 4BADDR0-7. Buffer status signal BFULL tells the BSM that display bus data is present at the input-output logic. Load signals *LXHI and *LXLO latch data from display bus 9BDAT0-15 into the input-output logic and *DRVIN routes the data onto internal bus PTD0-15. The BSM sends a write operation code to the MTS on MTSOP0-2 and selects a specific memory PCB with 9DSEL and 9C/L. The MTS sends write address signals RWROW0-7 and RWCOL0-7, and multiplexer control signals 7ADSL and 7MADSL, to the ZPR logic. The ZPR logic multiplexes RWROW0-7 and RWCOL0-7 together and sends resulting address signals 9DAD0-7 to the memory PCB. The MTS strobes the row and column addresses into the memory PCB with 9DADSL, 9DCAS, 9DRAS, and 9DAS0-4. The BSM latches the write data from display bus 9BDAT0-15 into the input-output logic with *LXHI and *LXLO and routes the data onto memory bus 9DGD0-15 with enable signal *PAKIN.

4.5.3.f.3 Screen refresh. The screen refresh operation constantly reads screen data from the memory PCB to the video PCB. The ZPR logic generates screen refresh addresses 9DAD0-7 starting with the origin values loaded from internal bus PTD0-15 by *LDXORG and *LDYORG. Memory control signals 9DADSL, 9DCAS, 9DRAS, and 9DAS0-4 strobe the addresses onto the memory PCB. Memory output control signals 9RFW and 9DSRLP read data from addresses in memory to the video PCB.

4.5.3.f.4 Memory refresh. Memory refresh operations occur only during zoom operations. The memory refresh counter generates address signals for those parts of memory not refreshed by the screen refresh signals. The MTS monitors zoom status signals *YZOOM0 and *ZOOM0. During zoom operations, memory refresh multiplex signal MRMUX1 and address select signal 4MADSL enable the memory refresh counter and multiplex the memory refresh addresses with the screen refresh addresses and the read-write addresses. Memory control signals 9DADSL, 9DCAS, 9DRAS, and 9DAS0-4 strobe the addresses onto the memory PCB.

4.5.3.f.5 Zoom. The system processor starts a zoom operation by driving 9BWRT active and selecting the MCP with address signals 4BADDR0-7. Buffer status signal BFULL tells the BSM that display bus data is present at the input-output logic. Load signals *LXHI and *LXLO latch data from display bus 9BDAT0-15 into the input-output logic and *DRVIN routes the data onto internal bus PTD0-15. The BSM loads zoom data into the X and Y zoom registers on the ZPR logic with load signals *LDXZM and *LDYZM. The ZPR logic sends zoom status signals *YZOOM0 and *ZOOM0 to the MTS and the MTS enables the memory refresh counter on the ZPR logic with MRMUX1 and 4MADSL. The ZPR logic generates zoom control signals 9DZOOM, 9DZOOM0, and 9DSTRTCH for the video PCB and modifies memory addresses 9DAD0-7 and memory control signals 9DSRLP, 9DSRHP, and 9RFW according to the zoom value selected.

4.5.3.f.6 Pan. The system processor starts a pan operation by driving 9BWRT active and selecting the MCP with address signals 4BADDR0-7. Buffer status signal BFULL tells the BSM that display bus data is present at the input-output logic. Load signals *LXHI and *LXLO latch data from display bus

9BDAT0-15 into the input-output logic and *DRVIN routes the data onto internal bus PTD0-15. The BSM loads pan data into the line and element origin registers with load signals *LDYORG and *LDXORG. The ZPR logic modifies the screen and memory refresh addresses according to the pan data in the origin registers. Memory addresses 9DAD0-7 determine the operating point for displayed (screen refresh) data.

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4.5.4 Memory PCB

The Memory PCB (figure FO4-17) has six functional elements:

- Memory select logic
- Group select and address driver logic
- Line drivers
- Interface logic
- Data control logic
- Memory planes 0-7

The memory select logic selects memory plane RAMs and controls readback data multiplexing. The group select and address driver logic decodes input select signals and buffers memory address inputs. The line drivers convert display data from TTL levels to line levels for transmission to other PCBs. The interface logic buffers clock and control inputs and generates register file address values. The data control logic writes data to the memory planes and routes readback data to the bidirectional data bus. Memory planes 0-7 store display data, convert display data from parallel to serial format, and multiplex readback data.

4.5.4.a Memory Select Logic. The memory select logic selects memory plane RAMs and controls readback data multiplexing. The 9DAS0-4, 5ADSL, 1DRAS, and 2DRAS signals generate PMRAS0-19 to select one of twenty RAMs or all twenty RAMs within one memory plane. The 9DAS0-4 and 5ADSL signals also generate PRDSEL0-2 and PRDMUX0-2 to select one of twenty readback data signals from each memory plane.

4.5.4.b Group Select and Address Driver Logic. The group select and address driver logic decodes input signals to select the 10 X 12 memory PCB and routes address signals to memory planes 0-7. The 9DSEL, 9C/L, and 9GP1-3 signals decode plane mask data on data lines 9DG0-7 and send 8CKLT, 6TGIS, and TGIS signals to the data control logic. Clock signals PTMCQ and NTMCQ synchronize the signals. Address signals 9DAD0-7, after being clocked by 7HQ6, go to memory planes 0-7 as P01ADR0-7, P23ADR0-7, P45ADR0-7, and P67ADR0-7.

4.5.4.c Line Drivers. The line drivers convert the TTL level signals from memory planes 0-7 to differential signals for transmission to other PCBs. Memory planes 0-7 send serial display data signals P0-7 ODD and P0-7 EVEN to the line drivers. Clock signal 7HQ6 reclocks the signals. Differential drivers split the 16 inputs into positive and negative outputs.

4.5.4.d Interface Logic. The interface logic (figure 4-40) has three functional elements:

- Reclock logic
- Clock buffers
- Read/write address counters

The reclock logic synchronizes input control signals with input clock signals and boosts signal drive currents. The clock buffers convert differential clock signals to TTL levels. The read/write address counters generate address values for the register files of memory planes 0-7.

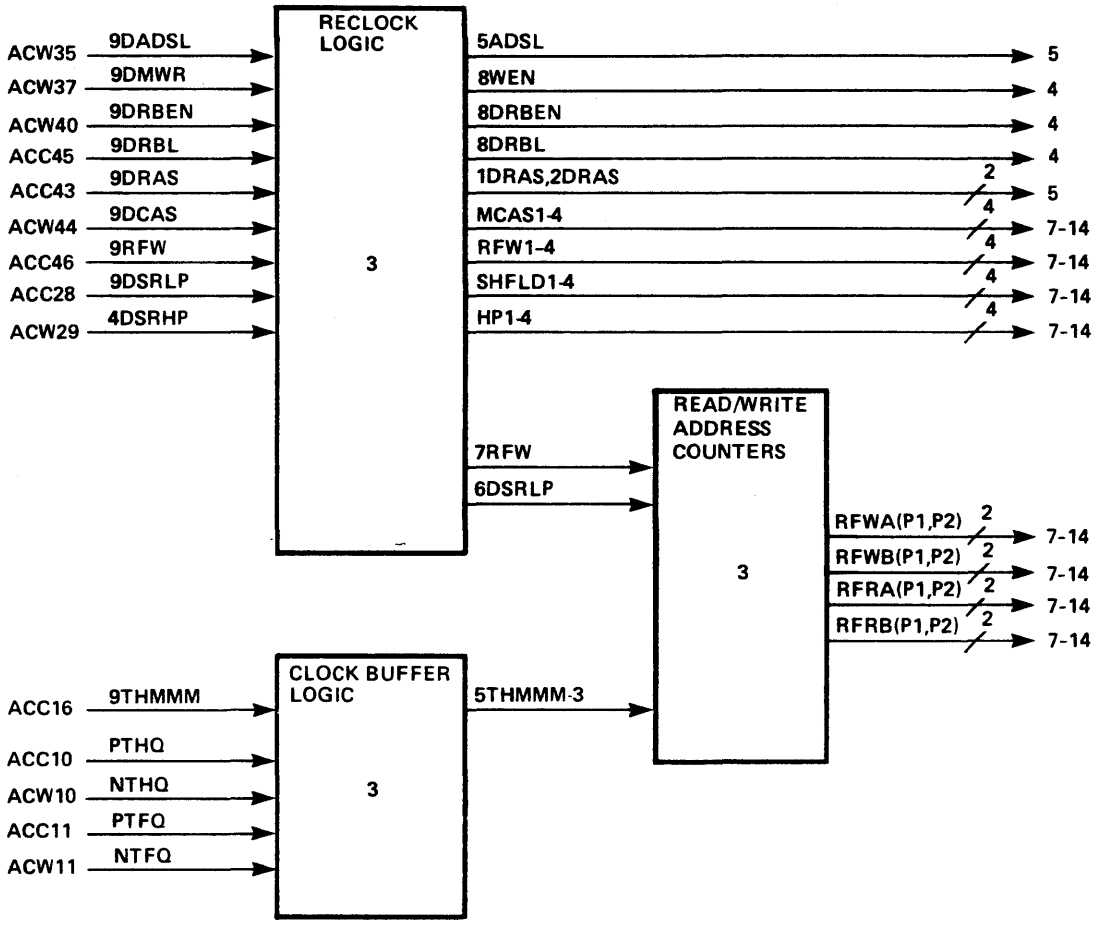

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Figure 4-40. Interface Logic

4.5.4.d.1 Reclock logic. The reclock logic synchronizes input signals with the 7HQ3 clock signal from the clock buffers. The 9DADSL, 9DMWR, 9DRBEN, and 9DRBL signals become 5ADSL, 8WEN, 8DRBEN, and 8DRBL, respectively. The 9DRAS, 9DCAS, 9RFW, 9DSRLP, and 4DSRHP signals become 1DRAS and 2DRAS, MCAS1-4, RFW1-4, SHFLD1-4, and HP1-4, respectively. The 9RFW signal becomes 7RFW and increments the write address counter. The 9DSRLP signal becomes 6DSRLP and increments the read address counter.

4.5.4.d.2 Clock buffers. The clock buffers convert the clock inputs from positive and negative differential signals to TTL level signals. The PTHQ and NTHQ signals become 7HQ3, 7HQ4, 7HQ5, and 7HQ6. Horizontal memory timing signal 9THMMM, clocked by the PTFQ and NTFQ signals, becomes 5THMMM-3 and loads the read/write address counters.

4.5.4.d.3 Read/write address counters. The read/write address counters use the 7RFW and 6DSRLP signals to generate address values for the register files of memory planes 0-7. The 7RFW signal increments the write address counter and the 6DSRLP signal increments the read address counter. The 5THMMM-3 signal loads the counters and 7HQ3 clocks the counters. Counter outputs RFWA (P1,P2), RFWB (P1,P2), RFRA (P1,P2), and RFRB (P1,P2) go to memory planes 0-7.

4.5.4.e Data Control Logic. The data control logic (figure 4-41) has three functional elements:

- Data in select logic
- Plane mask logic
- Readback data select logic

The data in select logic routes signals from 8 of the 16 data bus lines to memory planes 0-7. The plane mask logic generates read, write, and clear signals for the selected memory plane. The readback data select logic routes data from memory planes 0-7 to 8 of the 16 data bus lines.

4.5.4.e.1 Data in select logic. The 10 X 12 Memory PCB sends and receives data on 8 of the 16 lines of data bus 9DG0-15. Byte select signal 9DMSK selects the high or low data byte. Memory data in signals P0-7 MDIN go to the plane mask logic and memory planes 0-7.

4.5.4.e.2 Plane mask logic. One or more of the eight memory planes can be masked to prevent data from being written to or read from them. The plane mask logic loads masking data from P0-7 MDIN when clocked by 8CKLT and enabled by 6TGIS. Write enable signal 8WEN sends memory read/write signals P0-7 MR/W to memory planes 0-7. High speed erase signal 9HSPER sends clear signals P0-7 CLEAR to memory planes 0-7. Masking signals P0-7 SELECT go to the readback data select logic.

4.5.4.e.3 Readback data select logic. Readback load signal 8DRBL latches readback data signals P0-7 RBDATA from memory planes 0-7. Readback enable signal 8DRBEN routes P0-7 RBDATA onto 9DG0-7 or 9DG8-15, as selected by 9DMSK. When the plane mask logic loads masking data, the TGIS signal disables readback data select logic outputs on 9DG0-15. Masking signals P0-7 SELECT mask one or more of the eight readback data lines P0-7 RBDATA.

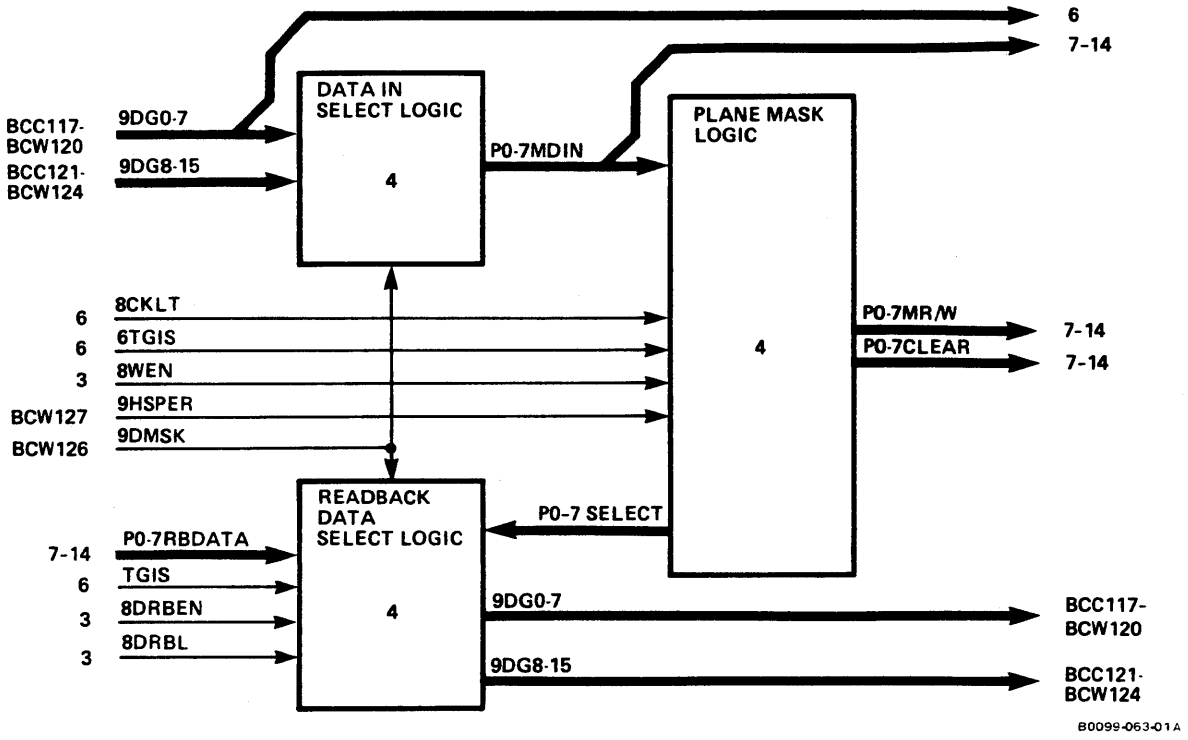

Figure 4-41. Data Control Logic

4.5.4.f Memory Planes 0-7. The 10 X 12 Memory PCB has eight memory planes. The following description of memory plane 0 applies to memory planes 1-7 also. Memory plane 0 (figure 4-42) has four functional elements:

- RAM memory
- Register files
- Shift registers
- Readback multiplexer

The RAM memory stores display data. The register files store data being read out from RAM memory. The shift registers send even and odd data serially to the line drivers. The readback multiplexer sends data serially to the data control logic.

4.5.4.f.1 RAM memory. The RAM memory consists of twenty 64K RAMs addressed by eight row and eight column address signals. Address lines P01ADR0-7 carry both row and column addresses while row address select signals PMRAS0-19 latch the row address into one or all of the RAMs and column address select signal MCAS1 latches the column address into all the RAMs. Data input signal P0MDIN routes serial data to all 20 RAMs and read/write signal P0MR/W controls memory read and write operations. Memory data signals DATA0-19 go to the readback multiplexer and the register files.

4.5.4.f.2 Register files. The four register files store 20 bits of data each from RAM memory. Register file write signal RFW1 stores the DATA0-19 signals into the register selected by register file write address signals RFWA and RFWB. Register file read address signals RFRA and RFRB select one of the four registers and send register data signals DATAOUT0-19 to the shift registers.

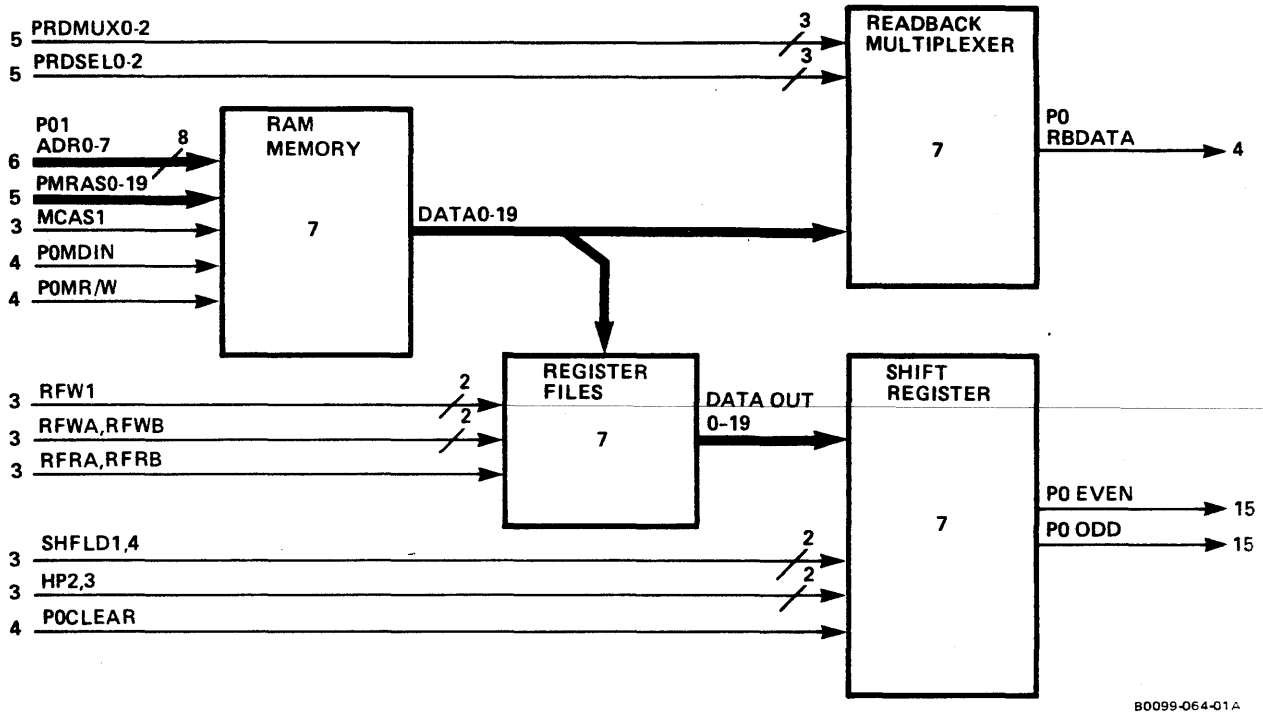

Figure 4-42. Memory Plane 0

4.5.4.f.3 Shift registers. The even and odd shift registers convert DATAOUT0-19 from parallel to serial format. Shift register load signals SHFLD1 and SHFLD4 load the odd and even shift registers. Hold pulses HP2 and HP3 provide zoom capability by causing the shift registers to repeat bits. Clear signal P0CLEAR clears the shift registers in the high-speed erase mode. Clock signal 7H05 clocks data through the shift registers. Output signals P0EVEN and P0ODD go to the line drivers.

4.5.4.f.4 Readback multiplexer. The readback multiplexer converts the DATA0-19 signals from parallel to serial format. Readback multiplex signals PRDMUX0-2 and readback select signals PRDSEL0-2 enable the readback multiplexer and select one of the DATA0-19 signals. Readback data signal P0RBDATA goes to the data control logic.

4.5.4.g Process Description. The 10 X 12 Memory PCB performs the following operations:

- Processor cycle read
- Processor cycle write
- Screen cycle read
- Screen cycle write

- Zoom
- Pan
- Plane mask

The processor cycle read operation sends display data from memory planes 0-7 through the data control logic to bidirectional data bus 9DG0-15. The processor cycle write operation sends display data from bidirectional data bus 9DG0-15 through the data control logic to memory planes 0-7. The screen cycle read operation sends display data from memory planes 0-7 through the line drivers to outputs VP0-15. The screen cycle write operation (high speed erase) sends display erase data from bidirectional data bus 9DG0-15 through the data control logic to memory planes 0-7. The zoom operation repeats display data bits to magnify the displayed image. The pan operation moves the screen origin to allow views of a zoomed image. The plane mask operation allows data to be written only to selected memory planes.

4.5.4.g.1 Processor cycle read. The processor cycle read operation takes place during processor cycle time determined by address select 9DADSL. Row address strobe signal 9DRAS, column address strobe 9DCAS, RAM select signals 9DAS0-4, and row/column address signals 9DAD0-7 read data from memory planes 0-7. Readback multiplex enable signals PRDMUX0-2 and readback multiplex select signals PRDSEL0-2 route readback data signals P0-7 RBDATA from memory planes 0-7 to the data control logic. Readback latch signal 9DRBL and readback enable signal 9DRBEN route P0-7 RBDATA through the data control logic to bidirectional data bus 9DG0-15.

4.5.4.g.2 Processor cycle write. The processor cycle write operation takes place during processor cycle time determined by 9DADSL. Row address strobe signal 9DRAS, column address strobe signal 9DCAS, RAM select signals 9DAS0-4, row/column address signals 9DAD0-7, and memory write signal 9DMWR write data from 9DG0-15 to memory planes 0-7.

4.5.4.g.3 Screen cycle read. The screen cycle read operation takes place during screen cycle time determined by 9DADSL. Row address strobe signal 9DRAS, column address strobe signal 9DCAS, RAM select signals 9DAS0-4, row/column address signals 9DAD0-7, register file write signal 9RFW, shift register load pulse 9DSRLP, and horizontal memory pulse 9THMMM read even data signals P0-7 EVEN and odd data signals P0-7 ODD to the line drivers. The line drivers send the data out on VP0-15.

4.5.4.g.4 Screen cycle write. The screen cycle read operation (also known as high-speed erase) takes place during screen cycle time determined by 9DADSL. Row address strobe signal 9DRAS, column address strobe signal 9DCAS, RAM select signals 9DAS0-4, row/column address signals 9DAD0-7, and high-speed erase signal 9HSPER write display erase data from 9DG0-15 to memory planes 0-7.

4.5.4.g.5 Zoom. The zoom operation repeats display data bits to magnify the displayed image. The 10 X 12 Memory PCB can zoom from 1 to 15 times in the horizontal (X-axis) and/or vertical (Y-axis) directions. Shift register hold pulse 9DSRHP and shift register load pulse 9DSRLP provide X-axis zoom. Row/column address signals 9DAD0-7 provide Y-axis zoom.

4.5.4.g.6 Pan. The pan operation moves the screen origin to allow views of a zoomed image. Shift register load pulse 9DSRLP and row/column address signals 9DAD0-7 provide X-axis pan. Row/column address signals 9DAD0-7 provide Y-axis pan.

4.5.4.g.7 Plane mask. The plane mask operation allows data to be written only to selected memory planes. Memory select signal 9DSEL, clear/load signal 9C/L, group select signals 9GP1-3, and clock signals PTMCQ and NTMCQ load plane mask data from 9DG0-7 into the data control logic.

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4.5.5 Video 12 PCB

The video 12 PCB (figure F04-18) has five functional elements:

- Input logic
- Buffer logic
- Text logic
- Graphics logic
- Video logic

The input logic routes data between the video 12 and the display bus, and controls video lookup table read and write operations. The buffer logic buffers system clocks, cursors, and sync signals, and decodes resolution signals. Text logic generates text data using a VLT. Graphics logic generates intensity values for refresh memory data using a VLT and zoom control signals. The video logic mixes the text and graphics data, when required, and converts digital signals to analog signals. The video 12A has four 2-bit digital-to-analog converters (DACs), while the video 12B has one 8-bit DAC.

4.5.5.a Input Logic. Address signals 4BADR0-7, read signal 9BREAD, and write signal 9BWRT control text and graphics VLTs. Composite sync signal 5 CSYC synchronizes input logic commands with video sync timing. Bus handshake signal 9BWAIT prevents further operations until the current display bus operation is completed. Display bus 9BDATA00-15 routes data to and from text and graphics VLTs.

Text data bus D0-10 routes programming data to the text control logic and starting addresses to the text VLT address counter. Address signals A0-3, read signal CHCS, and write signal 5CDS program the text control logic. Load signal 5LOC and increment signal INCC control the text VLT address counter. Character data bus CD0-11 routes data to the text VLT. Write control signal 5WC controls text VLT read and write operations. Write character signal 5WO controls text logic output.

Graphics data signals ED0-8 route starting addresses to the graphics VLT address counter and data to the graphics VLT. Load signal 5LOAD and increment signal 5INC control the graphics VLT address counter. Write control signals 5WLO and 5WLE control graphics VLT read and write operations. Resolution signal 5HI controls 5WLO and 5WLE, as required by system resolution.

4.5.5.b Buffer Logic. The buffer logic (figure 4-43) has four functional elements:

- Clock logic
- Blink oscillator
- Sync logic
- Cursor logic

The clock logic buffers system clock signals and routes resolution signals to video 12 functional elements. The blink oscillator generates the blink frequency used with text and graphics data. The sync logic buffers video timing inputs to the video 12. The cursor logic buffers cursor inputs.

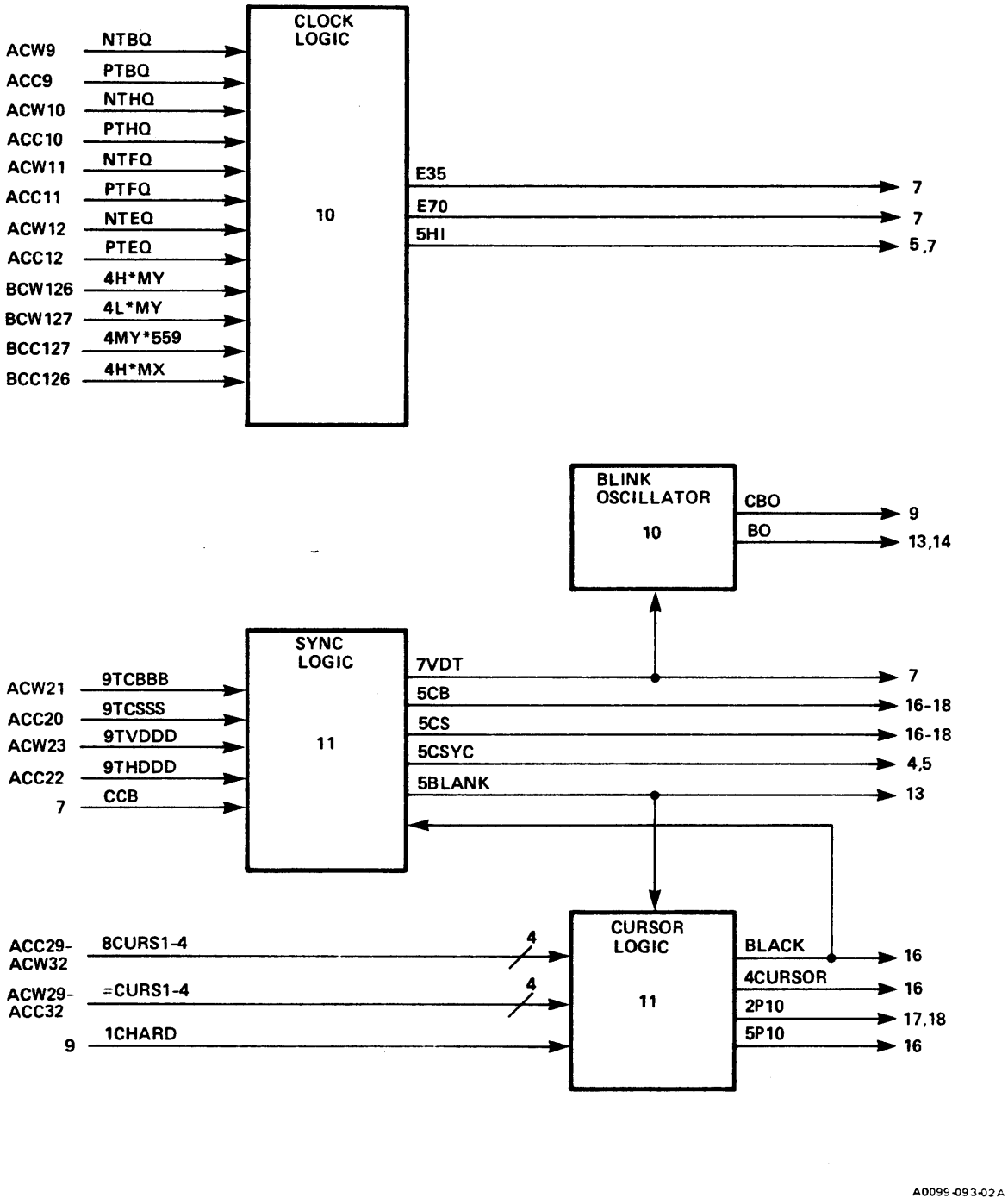

Figure 4-43. Buffer Logic

4.5.5.b.1 Clock logic. The clock logic buffers differential system clock signals NTBQ, PTBQ, NTHQ, PTHQ, NTFQ, PTFQ, NTEQ, and PTEQ. The buffered clock signals (not shown) synchronize video 12 operations. System resolution signals 4H*MY, 4L*MY, 4MY*559, and 4H*MX configure the video 12 for system screen resolution. The clock logic generates resolution signals E35, E70, and 5HI.

4.5.5.b.2 Blink oscillator. The blink oscillator generates complementary blink signals CBO and BO. Vertical drive time signal 7VDT clocks the blink oscillator.

4.5.5.b.3 Sync logic. Composite blanking signal 9TCBBB, character blanking signal CCB, and black cursor signal BLACK generate composite blanking signals 5CB and 5BLANK. Composite sync signal 9TCSSS generates composite sync signals 5CSYC and 5CS. Vertical drive signal 9TVDDD and horizontal drive signal 9THDDD generate vertical drive time signal 7VDT.

4.5.5.b.4 Cursor logic. Receivers convert differential cursor signals 8CURS1 through 8CURS4 and #CURS1 through #CURS4 into single-ended signals. A patching network selects two cursors from the four inputs. These cursors generate white cursor signal 4CURSOR, black cursor signal BLACK, and cursor intensity signals 2P10 and 5P10. Delayed text signal 1CHARD can be routed to another video PCB via the patching network and one of the cursor inputs.

4.5.5.c Text Logic. The text logic (figure 4-44) has four functional elements:

- Control logic
- Address select logic
- Video lookup table (VLT)
- Output logic

The control logic generates addresses for the VLT and controls the output logic. The address select logic multiplexes addresses from the control logic and the input logic to the VLT. The VLT stores character and character attribute data. The output logic generates characters and mixes character and attribute data.

4.5.5.c.1 Control logic. The input logic programs the control logic using data bus D0-7, write signal 5CDS, and address signals A0-3. The input logic reads data from the control logic using data bus D0-7, read signal CHCS, and address signals A0-3. The control logic generates character counter signals H0-6, row counter signals 1DR0-4, scan select signals 1R0-3, and character blanking signals CCB, 5CCBL, and 1CBL. Resolution signals E35 and E70 select character counter and row counter signals to match system resolution. Power-on reset clear signal 9PORCLR, write character video signal 5WO, and vertical drive time signal 7VDT control character blanking signals CCB, 5CCBL, and 1CBL.

4.5.5.c.2 Address select logic. Load signal 5LOC loads the starting address for the VLT address counter with data signals D0-10. Increment address counter signal INCC increases the address value by one after each read and before each write operation. Character blanking signal 1CBL controls

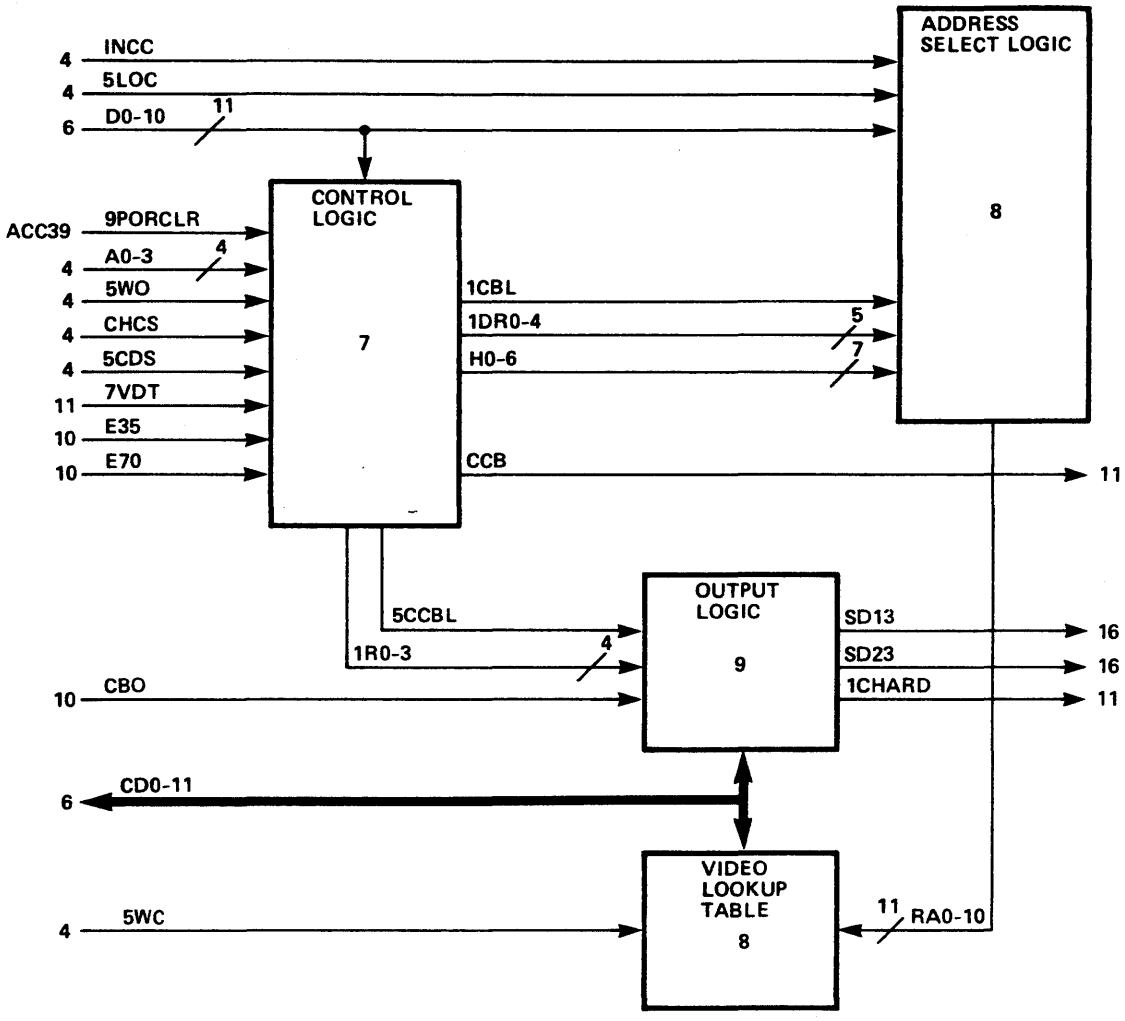

Figure 4-44. Text Logic

selection of VLT address signals RA0-10. During blanking, the VLT address counter outputs address the VLT. During screen write, character counter signals H0-6 and row counter signals 1DR0-4 address the VLT.

4.5.5.c.3 Video lookup table. Write control signal 5WC controls read and write operations from the VLT to character data bus CD0-11. Address signals RA0-10 select the location being written to or read from.

4.5.5.c.4 Output logic. Character data bus CD0-6, from the VLT, defines the ASCII characters. Character data bus CD7-11 defines the following character attributes: reverse video, blink, underline, and intensity level (off, one-third, two-thirds, and full intensity). Blink oscillator signal CB0 provides the blink signal turned on or off by the blink attribute. Scan select signals 1R0-3 control character generation. The output logic mixes the ASCII characters and the character attributes into character signals SD13 and SD23, and delayed text signal 1CHARD.

4.5.5.d Graphics Logic. The graphics logic (figure 4-45) has four functional elements:

- Multiplex logic
- Address logic
- Zoom logic
- Video lookup table (VLT)

The multiplex logic selects between refresh memory signals and address logic signals for the VLT. The address logic generates address values for reading from or writing to the VLT. The zoom logic controls VLT outputs during zoom operations. The VLT stores pixel intensity values used to create graphics displays.

4.5.5.d.1 Multiplex logic. A patching network selects 16 pairs from refresh memory signals 9VD0-31 and #VD0-31. Receivers convert the differential refresh memory signals to single-ended signals. Composite blanking signal 5BLANK controls VLT addressing. During blanking, address counter signals AL0-7 generate even and odd VLT address signals EEMA0-7 and OEMA0-7. During screen write, selected refresh memory signals generate EEMA0-7 and OEMA0-7. Select signal SELUT and unused refresh memory signals generate overlay signal 4OVL. Address signal AL8, blink oscillator signal B0, or unused refresh memory signals generate VLT partition signal PAR.

4.5.5.d.2 Address logic. Graphics data signals ED0-8 and load signal 5LOAD load a starting address into the address logic. Address increment signal 5INC increases output address signals AL0-8.

4.5.5.d.3 Zoom logic. Resolution signal 5HI and zoom zero signal 9DZOOM0 select VLT control signal SELUT. Zoom status signals 9DZOOM and 9DSTRCH, partition signal PAR, and clock signal 6EC35 (not shown) generate SELUT.

4.5.5.d.4 Video lookup table. Write signals 5WLE and 5WLO, and data signals ED0-7 write data into the VLT. Address signals EEMA0-7 and OEMA0-7 address VLT locations. Select signal SELUT controls VLT output signals 5L0-7.

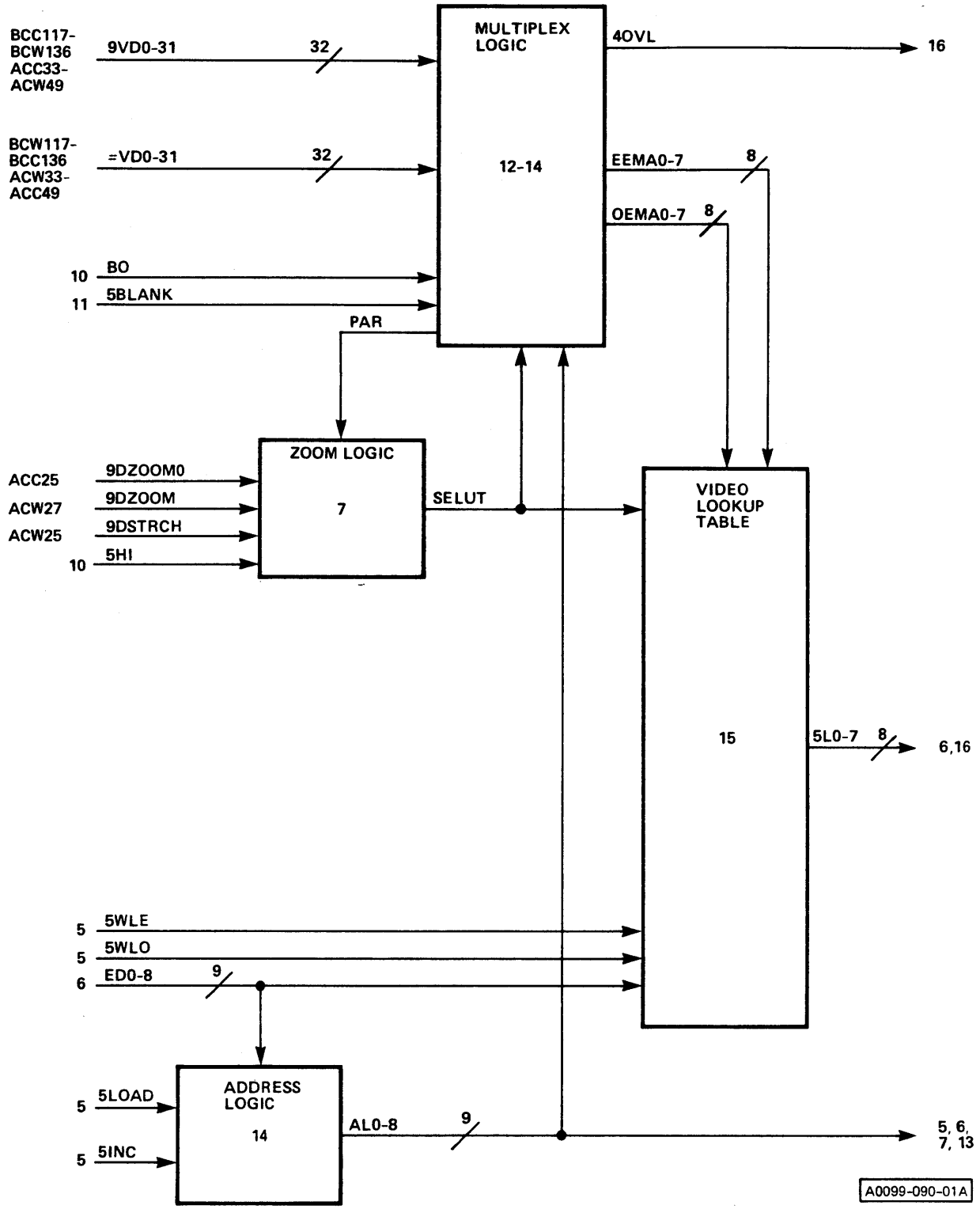

Figure 4-45. Graphics Logic

4.5.5.e Video Logic. The video logic mixes graphics signals 5L0-7, overlay signal 40VL, white cursor signal 4CURSOR, black cursor signal BLACK, and text signals SD13 and SD23. Composite sync signal 5CS and composite blanking signal 5CB control the DACs. The video 12A has four 2-bit DACs with outputs D1-4. For the video 12B, with one 8-bit DAC, the corresponding output is GREY. Cursor intensity signals 2P10 and 5P10 increase white cursor brightness 10 percent for 2-bit and 8-bit DACs, respectively.

4.5.5.f Process Description. The video 12 PCB performs the following operations:

- VLT read
- VLT write
- Text conversion
- Graphics conversion

Video lookup table read operations place data from the text or graphics VLT on display bus 9BDATA00-15. Video lookup table write operations place data from display bus 9BDATA00-15 into the text or graphics VLT. Text conversion operations generate text characters and convert digital character data to analog video signals. Graphics conversion operations convert digital graphics data from the memory PCB to analog video signals.

4.5.5.f.1 Video lookup table read. The system processor starts a VLT read operation by driving 9BREAD active. Address signals 4BADDR0-7 select the video 12 and the text VLT or graphics VLT. For a text VLT read, load signal 5LOC loads the starting address from display bus 9BDATA00-15 into the text logic via data bus D0-10. Address increment signal INCC increases the address by one after each byte is read from the text VLT. Character blanking signal 1CBL selects the read address during video blanking. The input logic drives write control signal 5WC inactive to route the VLT data onto display bus 9BDATA00-15 via character data bus CD0-7.

For a graphics VLT read, load signal 5LOAD loads the starting address from display bus 9BDATA00-15 into the graphics logic via data signals ED0-8. Address increment signal 5INC increases the address by one after each byte is read from the graphics VLT. Blanking signal 5BLANK selects the read address during video blanking. The input logic drives even and odd write control signals 5WLE and 5WLO inactive to route the VLT data onto display bus 9BDATA00-15 via output data signals 5L0-7.

4.5.5.f.2 Video lookup table write. The system processor starts a VLT write operation by driving 9BWRT active. Address signals 4BADDR0-7 select the video 12 and the text VLT or graphics VLT. For a text VLT write, load signal 5LOC loads the starting address from display bus 9BDATA00-15 into the text logic via data bus D0-10. Address increment signal INCC increases the address by one before each byte is written into the text VLT. Character blanking signal 1CBL selects the write address during video blanking. The input logic routes new data from display bus 9BDATA00-15 onto character data bus CD0-7. Write control signal 5WC writes new data from character data bus CD0-7 into the VLT.

For a graphics VLT write, load signal 5LOAD loads the starting address from display bus 9BDATA00-15 into the graphics logic via data signals ED0-8. Address increment signal 5INC increases the address by one before each byte is written to the graphics VLT. Blanking signal 5BLANK selects the write address during video blanking. The input logic routes new data from display bus 9BDATA00-15 onto data signals ED0-7. Even and odd write control signals 5WLE and 5WLO write new data from data signals ED0-7 into the VLT.

4.5.5.f.3 Text conversion. The system processor programs the text logic for system resolution and text format requirements. Address signals A0-3, read signal CHCS, write signal 5CDS, and data bus D0-7 allow the system processor to program the text logic. The text logic addresses the text VLT to generate text outputs SD13 and SD23. The video logic mixes text outputs SD13 and SD23 with graphics data for a combined display or sends text data to a separate device.

4.5.5.f.4 Graphics conversion. A patching network selects graphics and overlay inputs from refresh memory signals 9VD0-31 and #VD0-31. Selected graphics signals address the graphics VLT. A second patching network selects cursor inputs from cursor signals 8CURS1-4 and #CURS1-4.

The video logic mixes graphics VLT outputs 5L0-7 and overlay signal 4OVL with text data signals SD13 and SD23, and white and black cursors 4CURSOR and BLACK. On the video 12A, the VLT outputs drive three 2-bit DACs to a color monitor. From the video 12B, the VLT outputs drive one 8-bit DAC to a monochrome monitor.

4.5.6 Sync PCB

The sync PCB (figure F04-19) has 16 functional elements:

- Clock generator
- Sync generator
- Cursor generator
- TTL DMA sequencer
- Resolution status buffer
- Three decoders
- Three bus buffers
- Sync reset generator
- Display bus reset logic
- Wait generator
- Memory bus terminators (not shown on block diagram)
- Bus ready generator

4.5.6.a Clock Generator. This element (figure F04-20) generates clock pulses that control timing throughout the 9465. The clock generator has five functional elements:

- Oscillator
- Frequency divider
- Pulse driver
- Test inverter
- Functional inverter

The 54.227-MHz oscillator generates a nominal 17-ns clock pulse. The frequency divider divides this pulse to produce five symmetrical clock pulses, including the 17-ns pulse, and their complements (figure 4-46) and asymmetrical memory control pulse PTMCQ and complement NTMCQ. The pulse driver receives these 12 pulses and supplies six outputs. The test inverter inverts the six driver outputs to provide six test pulses. The functional inverter inverts 1S2, 1EQ, and 1FQ to become 7SQ, 7EQ, and 7FQ, respectively. Pulses 1SQ, 1EQ, 1FQ, 1HQ, 7SQ, 7EQ, and 7FQ control logic throughout the sync PCB. Pulse 7FQA is not used.

4.5.6.b Sync Generator. This logic (figure F04-21) generates the timing signals that control CRT operation and supplies control signals to the cursor generator. Signal origins and destinations in figure F04-21 are referenced by block number. The sync generator has 23 functional elements:

- Sync controller
- Four PROMs
- Vertical counter
- Sync output driver 9E
- Dot counter generator
- Three signal selectors
- Test register 3D
- Three buffers
- Horizontal memory control
- Vertical memory control
- Vertical field generator

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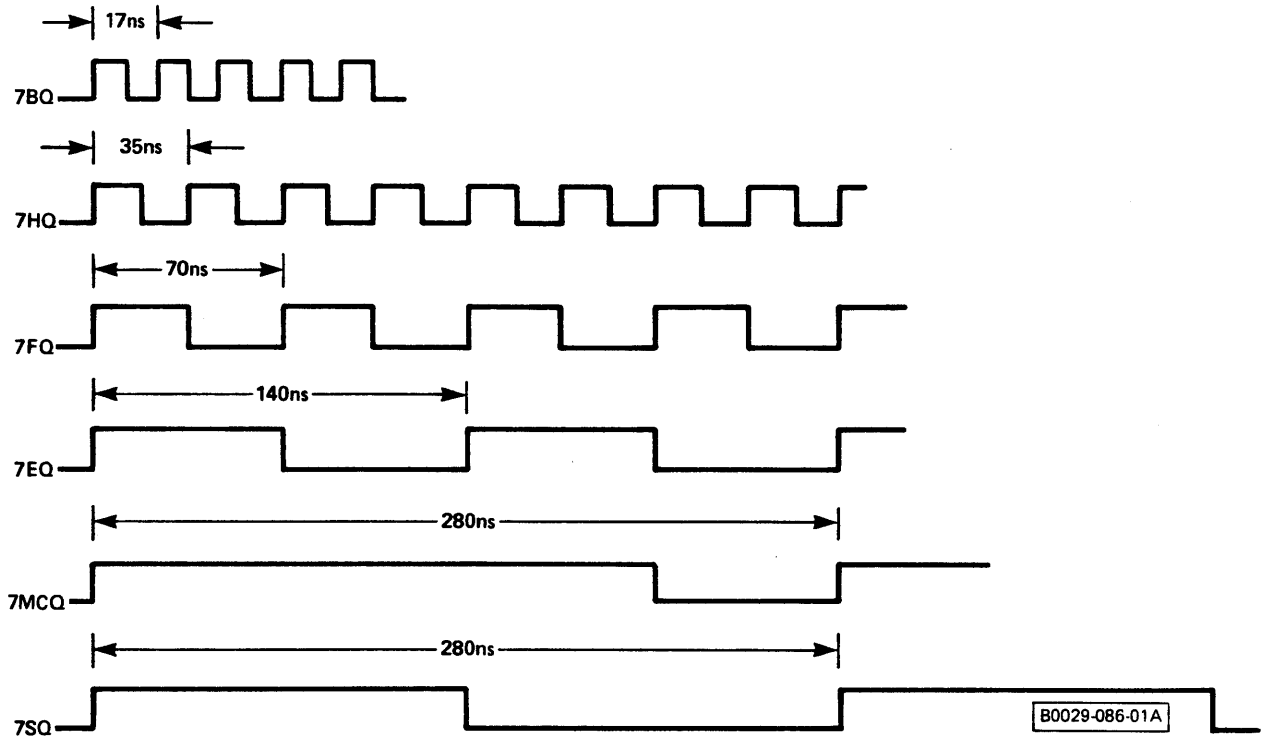

Figure 4-46. Clock Pulse Timing Diagram

- Composite sync generator
- Composite blanking generator
- Interlace control
- Counter load control
- Timing control generator

The resolution PROM (block 16) receives four fixed resolution-control signals from the backplane assembly and generates four control signals. The clock selector receives 1FQ, 1HQ, and 9SWCLK and generates clock pulses 7FQSL and 7HQSL. The dot counter generator receives 7FQSL, 7HQSL, and fixed resolution control signal 9SELX, and generates five outputs.

When signals 9DECODE, 9WRT, 9ADRSL, and 9PLEN go active, the sync controller (block 1) decodes the data received on lines 9BDATA08-15 under the control of signal CLK and generates address bits 1MA0-4 and 1RA0 and three control signals. The memory address PROM (block 22) receives 1MA0-4, 5HENB, and four dot counter generator signals and generates three control signals. The timing control generator (block 13) receives DISPL, VSYNC, STEN, *CLEN, 5CLK, 7FQSL, and 9SYNCLR and generates CRT timing signal 5TVBBB and three control signals. The vertical blanking buffer converts 5TVBBB into 6TVBBB and sync output driver 9E converts 6TVBBB into 9TVBBB. Driver 9E supplies drive for logic that receives CRT timing signals.

Signal 5HENB enables the horizontal PROM (block 2) which receives 1MA0-4, CLK, CTR1, and CTR2, and generates 5THBBB, 5THDDD, 7THMMM, and 6THXR. Dot counter generator signals CLK, CTR1, and CTR2 determine the timing of the four PROM outputs. The horizontal buffer converts 5THBBB and 5THDDD into 6THBBB and

6THDDD, respectively. Driver 9E converts 6THBBB and 6THDDD into 9THBBB and 9THDDD, respectively. The horizontal memory control logic receives 7THMMM, and generates the 6THMMM signal required for the resolution specified by signals 9SWCLK and 5SEL1. Driver 9E converts 6THMMM into 9THMMM. The counter load control logic converts 6THXR into 9LDCREC which goes to the TTL DMA sequencer.

The interlace control logic (block 19) receives 9BDATA08 and CLKTTL and generates 9INTLC, INTRL, and 5INTRL. Signal INTRL goes to the cursor generator; 9INTLC goes out to other PCBs. When signal 5LDVC goes active the vertical counter (block 8) starts counting 1FQ or 1EQ pulses under the control of STEN, CTR3, and 7FQ. Signal 5SEL1 determines whether the counter counts 1FQ or 1EQ pulses. The counter generates PROM address bits PRMA0-7. The vertical PROM receives address inputs PRMA0-6, 1RA0, and 5INTRL. A logic 0 on line PRMA7 and signal 5VPREN enable the PROM, which generates outputs 5TVMMM, 4TVSSS, and 5TVDDD. The address inputs determine the timing of the outputs. The vertical memory control logic receives 6TVMMM and horizontal memory signal 5THMMM, and generates vertical memory signal 6TVMMM, locking the vertical signal to the horizontal. The composite sync generator combines vertical sync signal 4TVSSS with horizontal sync signal HSYNC from the sync controller to produce composite sync signal 6TCSSS. Driver 9E converts 6TVMMM and 6TCSSS into 9TVMMM and 9TCSSS, respectively. The vertical drive buffer converts 5TVDDD into 9TVDDD.

The vertical field generator (block 7) receives address bit 1RA0, and signals INTRL and INLEN, and generates 6TVFFF which becomes 9TVFFF. The composite blanking generator (block 12) converts DISPL from the sync controller into 6TCBBB under the control of 5CLK and 7FQ. Driver 9E converts 6TCBBB into 9TCBBB. The counter control selector selects either LDCREC from the cursor generator or 9LDCREC to become 9LDCECSL, which goes to the cursor generator. Resolution control signal 5SEL1 determines which input becomes 9LDCECSL. The interlace selector selects either LDCREC from the cursor generator or 8LDCREC from the TTL DMA sequencer to become INLSL, which goes to the cursor generator. Signal 5SEL1 determines which input becomes INLSL. Test register 3D (block 23) converts six CRT timing signals into six test outputs which appear at sync PCB test points.

4.5.6.c Cursor Generator. This logic (figure F04-22) generates the cursor pattern. The logic has nine functional elements:

- ¤ Cursor line register
- ¤ Cursor line counter
- ¤ Cursor PROM
- ¤ Cursor shift register
- ¤ Cursor element register
- ¤ Cursor element counter
- ¤ Blink counter
- ¤ Cursor control logic
- ¤ Gate 4K-11

Signal 9LDCRLN loads data bits 9BDATA00-09 into the cursor line register. Vertical blanking signal 9TVBBB loads bits 1-9 from the register into the cursor line counter. Bit 0 goes to the sync generator as LDCREC. Horizontal memory signal 9THMMM enables the counter which counts 7FQ clock pulses and

generates outputs A-E. Gate 4K-11 receives vertical field signal 9TVFFF and interlace control signal INLSL from the sync generator, and generates output F. Output A enables the cursor PROM, which receives outputs B-F and resolution control signals 4H*MY, 4L*MY, and INTRL, and sends four outputs to the cursor shift register.

Signal 9LDCREL loads the cursor element register with data bits 9BDATA00-09, 11, and 12. Signal 9LCECSL loads register outputs CXPOS2-10 into the cursor element counter, which counts 7FQSL clock pulses and generates signal CXCZ at the last count. Signal 9TVMMM enables the blink counter, which counts 7FQ clock pulses and generates a carry output at the last count. The cursor control logic receives the element and blink counter outputs, three signals from the element register, and two clock signals, and generates signal LDCPAT.

The cursor shift register converts the parallel data from the cursor PROM into serial form. Signal LDCPAT loads the parallel data into the register. Clock pulse 7HQSL shifts the data out of the register to appear at serial outputs 8CURS1 and #CURS1.

4.5.6.d TTL DMA Sequencer. The TTL DMA sequencer (DMA) transfers data between devices connected to the display bus. The DMA (figure F04-23) has a RAM that can store up to 14 device port addresses and can make up to 4096 transfers between specified ports. The DMA has 16 functional elements:

- Condition selector
- Next address selector
- PROM address register 6L
- DMA PROM
- Control register
- DMA enable logic
- Reset driver
- RAM address selector 3T
- Address control logic
- RAM address counter
- DMA RAM
- Readout register
- Port address register
- Sequence counter
- Transfer counter
- Temporary data register

4.5.6.e DMA Elements. The next-address selector, PROM address register, and DMA PROM (blocks 2, 3, and 4) form a closed loop. Clock pulse 7EQ clocks the 5-bit address byte from the selector into register 6L. The PROM receives the address byte from 6L and responds by sending two 5-bit address bytes, a low byte and a high byte, to the selector which selects one of the bytes and sends the selected byte to 6L to be clocked in by the next 7EQ clock pulse in place of the previous byte. When signal SELNA is inactive, the low byte (AB10, 20, 40, 80, and 160) goes to 6L. When SELNA is active, the high byte (AB11, 21, 41, 81, and 161) goes to 6L. The PROM also generates 17 control signals in response to the address byte from 6L. The control register receives nine of

these signals, two additional control signals, and clock pulse 7EQ, and generates 11 control outputs. Clock pulse 7EQ clocks signal 9LDCREC from the sync generator into register 6L to become 8LDCREC, which goes back to the sync generator.

The condition selector (block 1) receives six control signals, two clock pulses, and three address bits from the PROM, and selects one of the control signals to become SELNA in response to the address bits received.

When data bit 9BDATA07 goes inactive and signal 7WRDM goes active, the DMA enable logic generates DMAON at the next 7EQ clock pulse. When either 6SEQDON or 5WRESET goes active, DMAON goes inactive, and 9DMADONE goes active at the next 7EQ clock pulse. The reset driver supplies drive for circuits that receive 6WRESET.

When signal DMARAMLD is inactive, RAM address selector 3T (block 8) inverts data bits 9BDATA00-03 to become bits LDR1, 2, 4, and 8. When DMARAMLD goes active, 3T inverts 5RAMLSB to become LDR1, and sets LDR2, 4, and 8 to zero.

When signal INCRAMDM goes active, the address control logic (block 12) generates signal INCRADR. When 7WRDMARM or 7RDDMARM goes active, the address control logic generates INCRADR after two 7EQ clock pulses.

Signal DMARAMLD or PRORAMLD loads the data from selector 3T into the RAM address counter. When INCRADR goes active, the counter increments one count at the next 7EQ clock pulse.

When signal 7WRDARM goes active, the DMA RAM stores data received on lines 9BDATA00-15 in the location specified in the four-bit address byte from the RAM address counter. The DMA RAM transmits, on lines RAMD0-15, the data stored in the address received from 6L.

The readout register receives RAM data on lines RAMD0-5. When signal 7RDDMARM goes active, the register transmits the received data on lines 9BDATA00-15.

After signal ADRLD goes active, the next 1EQ clock pulse clocks the data on lines RAMD0-15 into the port address register. When signal 6ENRDADR goes active, the register transmits, on lines 4BADR0-7, the data received on lines RAMD0-7. This is the source port address. When 6ENWRADR goes active, the register transmits, on lines 4BADR0-7, the data received on lines RAMD8-15. This is the destination port address.

After signal 5SEQLD goes active, the next 1EQ clock pulse loads the sequence counter with data received on lines RAMD0-15. This is the sequence count. Each sequence consists of a number of transfers between two specified ports. After 5SEQDC goes active, the next 1EQ clock pulse decrements the counter one count.

After signal 5TRFLD goes active, the next 1EQ clock pulse loads the transfer counter with data received on lines RAMD0-15. This is the number of transfers to be made from a given source to a given destination. After 5TRFDC goes active, the next 1EQ clock pulse decrements the counter one count.

After signal 8DMARD goes active, a transition to the inactive state loads the temporary data register (block 16) with data received from a source port on lines 9BD00-15. When 8DMAWR subsequently goes active, the register transmits the stored data to a destination port on lines 9BD00-15.

4.5.6.f DMA Operation. In a typical DMA operation, the DMA RAM stores up to 15 control words which specify up to 7 pairs of port addresses and the number of transfers required for each pair. The first word (address 0) gives the number of sequences (sequence count). Each sequence consists of a number of transfers from a specified source port to a specified destination port. The stored words control DMA operation. RAM address selector 3T (block 8) receives a zero byte on lines 9BDATA00-03 and sends the zero byte to the RAM address counter. Signal PRORAMLD loads the zero byte into the counter, which sends the zero byte to the DMA RAM. The RAM then receives signal 7WRDMARM and stores the control word received on lines 9BDATA00-15 in address location zero. This is the sequence count. The address control logic also receives 7WRDMARM and sends INCRADR to the counter, which increments one count and generates an address-1 byte. The RAM then stores the second control word received on the data lines in address 1. This is the first transfer count. This sequence repeats an additional 13 times. The RAM stores the first source and destination addresses in address 2, the second transfer count in address 3, the second source and destination addresses in address 4, and so on until the RAM has stored up to seven transfer counts and 14 addresses (7 pairs).

After signal 6WRESET resets PROM address register 6L (block 3) to zero, 6L sends an address-0 byte to the DMA PROM which generates an address-0 low byte, an address-1 high byte, and an address-0 condition-select byte. As long as signal SELNA remains inactive, the next-address selector sends the address-0 byte to 6L and the address-0 byte circulates around the closed loop. This is the normal inactive state. The address-0 condition-select byte selects the DMAON input to the condition selector. As long as DMAON remains inactive, SELNA also remains inactive and the PROM remains at address 0.

After the RAM stores the control words, the DMA enable logic (block 7) receives a logic 0 on line 9BDATA07 and active signal 7WRDM, and generates signal DMAON. The condition selector receives DMAON and sends SELNA to the next-address selector, which then selects the address-1 high byte and sends the address-1 byte to 6L. The PROM receives the address-1 byte from 6L and generates address-2 low and high bytes and signals DMARAMLD and 1BUSY. The control register inverts 1BUSY to become 9BBUSY, which goes out on the display bus.

RAM address selector 3T (block 8) receives DMARAMLD and generates an address-0 four-bit byte since 5RAMLSB is normally inactive. Signal DMARAMLD loads the address-0 byte into the RAM address counter, which sends the address-0 byte to the DMA RAM and the RAM transmits the control word stored in address 0 on lines RAMD0-15. This is the sequence count.

Since the low and high bytes from the PROM are both address 2, the next-address selector sends an address-2 byte to 6L. The PROM receives the address-2 byte from 6L and generates address-3 low and high bytes and signals 5SEQLD and INCRAMDM. Signal 5SEQLD loads the sequence count from the RAM into the sequence counter (block 14). The address control logic (block 12)

receives INCRAMDM and generates INCRADR, which increments the RAM address counter to count 1. The counter then sends an address-1 byte to the RAM. The RAM generates the first transfer count.

The next-address selector sends an address-3 byte to 6L. The PROM receives the address-3 byte and generates address-4 low and high bytes and signals 5TRFLD and INCRAMDM. Signal 5TRFLD loads the transfer counter with the first transfer count from the RAM. Signal INCRAMDM becomes INCRADR and increments the RAM address counter to 2. The RAM then receives an address-2 byte and generates the first source and destination addresses.

The PROM receives the address-4 byte and generates address-5 low and high bytes and signals ADRLD and INCRAMDM. Signal ADRLD loads the source and destination addresses from the RAM into the port address register (block 13). The RAM address counter increments to 3 and the RAM generates the second transfer count.

The PROM receives the address-5 byte and generates an address-5 low byte, an address-6 high byte, an address-1 condition-select byte, and signals 7DMAIORQ and 5ENRDADR. The control register converts 7DMAIORQ and 5ENRDADR into 9BIORQ and 6ENRDADR, respectively. Signal 9BIORQ goes out on the display bus. The port address register receives 6ENRDADR and transmits the source address on lines 4BADR0-7.

The address-1 condition-select byte selects the 7SQ input to the condition selector, and SELNA goes active at the next 7SQ pulse. The next-address selector then selects the address-6 high byte. The PROM receives the address-6 byte and generates address-7 low and high bytes, and signals 7DMAIORQ, SETBRD, and 5TRFDC. The control register inverts SETBRD to become 8DMARD at the next 7EQ clock pulse, and converts SETBRD and 7DMAIORQ into 9BREAD and 9BIORQ at the 7EQ pulse. Signals 9BREAD and 9BIORQ go out on the display bus. Signal 8DMARD clocks data from the source into the temporary data register (block 16). Signal 5TRFDC decrements the transfer counter one count.

The PROM receives an address-7 byte and generates an address-13 low byte, an address-8 high byte, and an address-2 condition-select byte. The address-2 byte selects the 5TRFZERO input to the condition selector. If 5TRFZERO is inactive, SELNA goes active and the next-address selector selects the address-8 high byte.

The PROM receives the address-8 byte and generates an address-8 low byte, an address-9 high byte, and an address-3 condition-select byte. The address-3 byte selects the 9BWAIT input to the condition selector. If 9BWAIT is active, SELNA remains inactive, and the next-address selector selects the address-8 low byte which circulates around the loop until 9BWAIT goes inactive. Signal SELNA then goes active and the next-address selector selects the address-9 high byte.

The PROM receives the address-9 byte and generates an address-9 low byte, an address-10 high byte, and an address-1 condition-select byte. The address-1 byte selects the 7SQ input to the condition selector, and SELNA goes active at the next 7SQ pulse. The next-address selector then selects the address-10 high byte.

The PROM receives the address-10 byte and generates address-11 low and high bytes, and signals 5ENWRADR, and SETBWR. Signal 5ENWRADR becomes 6ENWRADR, 7DMAIORQ becomes BIORQ, and SETBWR becomes 8DMAWR and 9BWRT. The port address register receives 6ENWRADR and transmits the destination address on lines 4BADR0-7. Signals 9BIORQ and 9BWRT go out on the display bus. The temporary data register receives 8DMAWR and sends the stored data from the source to the destination on lines 9BD00-15.

The PROM receives the address-11 byte and generates an address-23 low byte, an address-12 high byte, and an address-5 condition-select byte which selects the BAKIN input to the condition selector.

If another device is using the display bus, the DMA waits until the bus is clear. If no other device is using the bus, the DMA makes another transfer and again decrements the transfer counter. This continues until no more first-sequence transfers remain and the transfer count reaches zero. The DMA then decrements the sequence counter, reloads the transfer counter, and makes all the second-sequence transfers. After the DMA completes the last sequence, the sequence count reaches zero, and signal 5SEQZERO goes active.

After receiving an address-20 byte, the PROM generates an address-22 low byte, an address-21 high byte, and an address-4 condition-select byte, which selects the 5SEQZERO input to the condition selector. If 5SEQZERO is inactive, SELNA goes active, and the next-address selector selects the address-21 high byte.

The PROM receives the address-21 byte and generates address-3 low and high bytes and signals 5SEQDC, DMARAMLD, and 5RAMLSB. Signal 5SEQDC decrements the sequence counter. RAM address selector 3T receives 5RAMLSB and DMARAMLD, and generates an address-1 byte. Signal DMARAMLD loads the address-1 byte into the RAM address counter, which sends the address-1 byte to the RAM. The DMA then continues making the required transfers.

When 5SEQZERO goes active after the PROM receives an address-20 byte, SELNA remains inactive and the next-address selector selects the address-22 low byte. The PROM then receives the address-22 byte and generates an address-0 low byte, an address-22 high byte, an address-0 condition-select byte, and signals DMARAMLD and 5SEQDON, which becomes 6SEQDON. The DMA enable circuit receives 6SEQDON and generates 9DMADONE, which goes out on the display bus. Signal DMAON goes inactive. RAM address selector 3T receives DMARAMLD and generates an address-0 byte. Signal DMARAMLD loads the address-0 byte into the RAM address counter, which sends the address-0 byte to the RAM. The address-0 condition-select byte selects the DMAON input to the condition selector. With DMAON inactive, SELNA remains inactive, and the next-address selector selects the address-0 low byte. The PROM then receives the address-0 byte, and the DMA remains in an inactive state until DMAON again goes active.

4.5.6.g Resolution Status Buffer. This buffer receives six resolution control signals and transmits inverted outputs on six data bus lines. When signal 9RDRES from the sync address bus decoder goes active, the buffer transmits the inverted signals on lines 9BD08-13. Data bit 9BD14 is active in 60-Hz 9465s, and inactive in 50-Hz 9465s.

4.5.6.h Decoders. Each of the three decoders decodes address bits 4ADR0-7 and control signals 9IOREQ, 9WRT, and 9READ. The DMA address decoder generates four DMA control signals. The cursor address decoder generates two cursor control signals and 9RDRES. The sync address decoder generates five sync control signals and 9DCINTRL.

4.5.6.i Bus Buffers. The bidirectional data bus buffer supplies drive for circuits connected to the data buses. When signal 7RDDMARM or 9RDEN goes active, the buffer transfers data received on lines 9BDATA00-15 to lines 9BD00-15. When any one of the seven other input control signals goes active, the buffer transfers data received on lines 9BD00-15 to lines 9BDATA00-15.

The address bus buffer supplies drive for circuits connected to address bus lines 4ADR0-7. The buffer transfers address bytes received on lines 4BADR0-7 to lines 4ADR0- 7.

The control bus buffer supplies drive for circuits connected to the control bus. The buffer converts incoming control signals 9BIORQ, 9BWRT, and 9BREAD into control signals 9IOREQ, 9WRT, and 9READ, respectively.

4.5.6.j Sync Reset Generator. This circuit (figure 4-47) generates reset signals that are synchronized with the system clock, and supplies drive for the circuits that receive the reset signals. The sync reset generator has six functional elements:

- Internal reset circuit
- External reset circuit
- Reset output logic
- Sync clear logic
- Reset clock selector
- Reset switch SW1

The internal reset circuit receives signal WNCC and clock pulse 1RSTCLK, and generates reset signal 5WCLEAR at the second 1RSTCLK pulse after WNCC goes active. Signal 5WCLEAR remains active for 15 1RSTCLK pulses.

The external reset circuit receives three reset signals and two clock pulses. When signals 9BSWCLR and BSWCLR go active, the external reset circuit generates signal 6BSWCLR at the next 1RSTCLK pulse. When 9BRESCLR goes active, the circuit generates 6BSWCLR at the first 1RSTCLK pulse after the next 7FQ pulse. Signal 6BSWCLR remains active for 15 1RSTCLK pulses.

After receiving signal 5WCLEAR or 6BSWCLR, the reset output logic generates reset signal 5WRESET at the next 1RSTCLK clock pulse.

After receiving data bit 9BDATA10, the sync clear logic generates reset signal 7SYNCLR at the next 1RSTCLK clock pulse followed by 9SYNCLR at the next 7FQ

clock pulse. Signal CLKTTL inhibits the sync clear logic. The reset clock selector receives resolution control signals 9SELX, 4L*MY, 4MY*559, and three clock pulses, and generates the 1RSTCLK clock pulse required for the resolution specified by the control signals.

Reset switch SW1 is a momentary two-position manual switch. When actuated, SW1 generates signal WNCC.

4.5.6.k Display Bus Reset Logic. After receiving signal 5WCLEAR, the display bus reset logic generates display data bus bit 9BD02 at the next 7EQ clock pulse. Signal CLKTTL inhibits the display bus reset logic.

4.5.6.l Wait Generator. When signal 9DECODE goes active, this logic generates signal 9BWAIT. The fourth 7SQ clock pulse after 9DECODE goes inactive sets 9BWAIT inactive and inhibits the wait generator. The fourth 7SQ pulse after 9DECODE goes active enables the wait generator again.

4.5.6.m Memory Bus Terminators. Twenty memory bus lines terminate on the sync PCB. The terminators (not shown on block diagrams) are passive elements with no logic functions.

4.5.6.n Bus Ready Generator. This is a passive circuit that generates a constant BREADY signal. The circuit has no logic function.

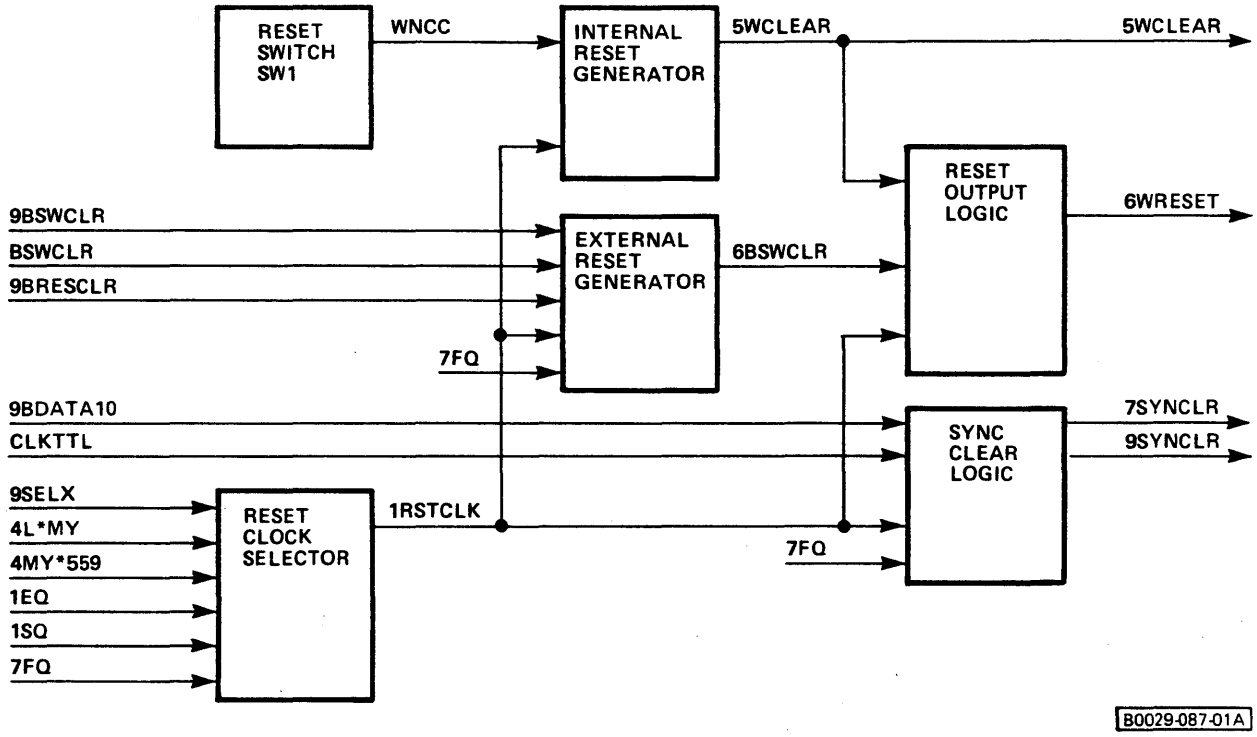

Figure 4-47. Sync Reset Circuit

4.5.7 Backplane

The backplane assembly has two functions:

- ¤ Signal and power distribution
- ¤ Clock termination

4.5.7.a Signal and Power Distribution. Backplane layout (figure 4-48) is organized to accommodate multiple serial link, MCP, memory, and video PCBs. Video, memory, and MCP PCB positions are interrelated. The backplane assembly can support up to two MCP PCBs and divides memory PCBs into memory groups 1 and 2.

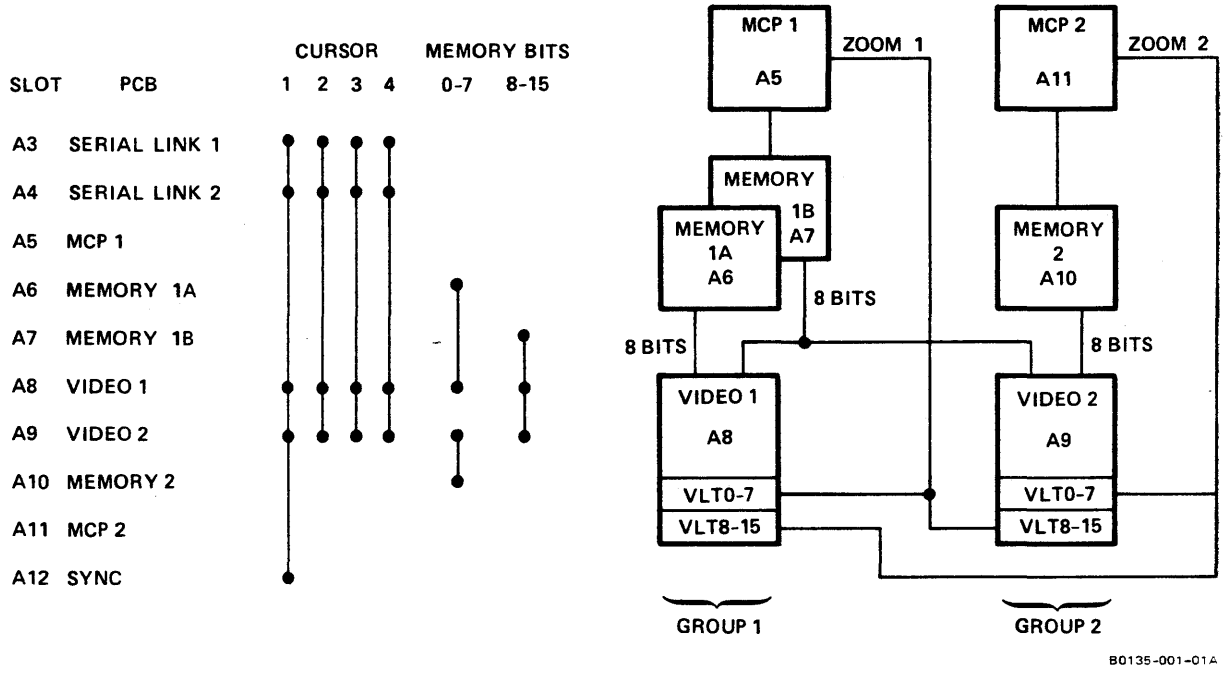

Figure 4-48. Backplane Layout

The maximum number of memory bits available to respective video PCBs is a function of backplane assembly layout. Although a maximum of 16 memory bits per video PCB is possible, a given video PCB will actually use only the bits selected by PCB strapping options. Backplane connectors (figure 4-49) interconnect signals between the host computer (jack J201) and the backplane assembly. Two internal cable assemblies are manufactured: a software interface cable assembly and a hardware interface cable assembly. Commonly, a software interface is installed, and interface PCB position A1 is empty.

Ten conductors route to the control panel from backplane assembly jack J1. Jacks J2 and J3 are not presently used.

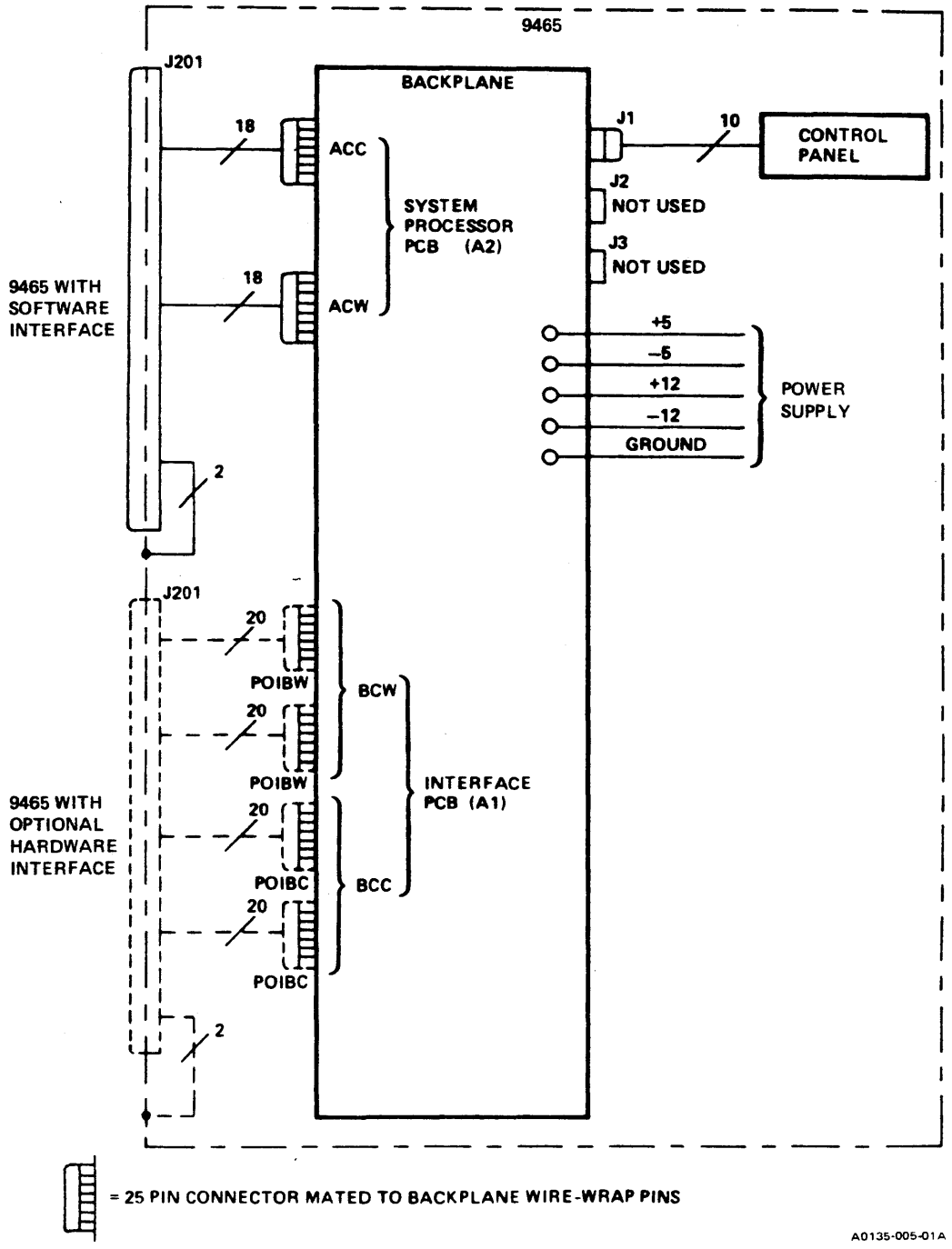

Figure 4-49. Backplane Connectors

The output of the power supply terminates on backplane assembly terminal lugs. Voltages are as follows: +5 V, -5 V, +12 V, and -12 V. Power and ground are distributed via backplane assembly printed circuit traces.

4.5.7.a.1 Software interface. When a 9465 is configured with a software interface, internal cable conductors route to system processor PCB backplane assembly position A2. Table 4-14 illustrates conductor assignments. One 25-pin plug connects to ACW wire wrap pins; one 25-pin plug connects to ACC wire wrap pins. Pin 25 on the ACW side is keyed to ACW44. Likewise, pin 25 on the ACC side is keyed to ACC44.

CAUTION

Serious equipment damage will result if plugs are miskeyed during maintenance or checkout.

4.5.7.a.2 Hardware interface. With a hardware interface, internal cable conductors route to interface PCB backplane assembly position A1. Table 4-14 lists conductor assignments. Four ribbon cables attach via plugs to BCC and BCW wire wrap pins. Plugs are designated P01BC (101-120), P01BC (121-140), P01BW (101-120), and P01BW (121-140). Plugs with a BC designation are keyed to respective BCC wire wrap pins. Likewise, plugs marked BW are keyed to respective BCW wire wrap pins.

CAUTION

Serious equipment damage will result if plugs are miskeyed during maintenance or checkout.

4.5.7.a.3 Control panel interface. Jack J1 is an interconnection point for 10 conductors wired to the control panel. Table 4-16 lists connector J1 pin assignments referenced to control panel destinations.

4.5.7.b Clock Termination. Six clocks (BQ, HQ, FQ, EQ, MCQ, and SQ) terminate in a backplane assembly resistor network. This passive network has resistors selected and arranged to present a characteristic impedance of 72 ohms to each differential clock circuit transmission line. The voltage at the junction of the transmission line and the resistor network is maintained at -2 V.

Table 4-14. Software - Internal Cable Conductor Assignments

J201 Pin	Backplane Pin		Signal	Function
505	ACC42		GROUND	-
605	ACC38		9IOBIT15	Data bit 15
504	ACC42		GROUND	-
604		ACW38	9IOBIT14	Data bit 14
503		ACW42	GROUND	-
603	ACC37		9IOBIT13	Data bit 13
502		ACW42	GROUND	-
602		ACW37	9IOBIT12	Data bit 12
501	ACC41		GROUND	-
601	ACC36		9IOBIT11	Data bit 11
214	ACC41		GROUND	-
410		ACW36	9IOBIT10	Data bit 10
310		ACW41	GROUND	-
409	ACC35		9IOBIT09	Data bit 09
309		ACW41	GROUND	-
408		ACW35	9IOBIT08	Data bit 08
108		ACW30	GROUND	-
208	ACC34		9IOBIT07	Data bit 07
107		ACW30	GROUND	-
207		ACW34	9IOBIT06	Data bit 06
106	ACC30		GROUND	-
206	ACC33		9IOBIT05	Data bit 05
105	ACC30		GROUND	-
205		ACW33	9IOBIT04	Data bit 04
104		ACW29	GROUND	-
204	ACC32		9IOBIT03	Data bit 03
103		ACW29	GROUND	-
203		ACW32	9IOBIT02	Data bit 02
102	ACC29		GROUND	-
202	ACC31		9IOBIT01	Data bit 01
101	ACC29		GROUND	-
201		ACW31	9IOBIT00	Data bit 00
112		ACW28	GROUND	-
212	ACC28		9IOREAD	I/O read (same as 9CREAD)
111		ACW27	GROUND	-
211	ACC27		9IOWRT	I/O write (same as 9CWRITE)
303		ACW26	GROUND	-
403	ACC26		9IOREADY	I/O ready (same as 9CACK)
113		ACW25	GROUND	-
213	ACC25		9IOCMD	I/O command
301		ACW24	GROUND	-
401	ACC24		9IOCLR	I/O clear (same as 9IOPCLR)
302		ACW22	GROUND	-
402	ACC22		9IOINT	I/O interrupt

Table 4-15. Hardware - Internal Cable Conductor Assignments

J201 Pin	Backplane Pin	Signal	Function
101	BCC 101	#IOBIT00	Return, Bit00
201	BCC 102	IOBIT00	Data, Bit00
102	BCC 103	#IOBIT01	Return, Bit01
202	BCC 104	IOBITol	Data, Bit01
103	BCC 105	#IOBIT02	Return, Bit02
203	BCC 106	IOBIT02	Data, Bit02
104	BCC 107	#IOBIT03	Return, Bit03
204	BCC 108	IOBIT03	Data, Bit03
105	BCC 109	#IOBIT04	Return, Bit04
205	BCC 110	IOBIT04	Data, Bit04
106	BCC 111	#IOBIT05	Return, Bit05
206	BCC 112	IOBIT05	Data, Bit05
107	BCC 113	#IOBIT06	Return, Bit06
207	BCC 114	IOBIT06	Data, Bit06
108	BCC 115	#IOBIT07	Return, Bit07
208	BCC 116	IOBIT07	Data, Bit07
109	BCC 117	-	-
209	BCC 118	-	-
110	BCC 119	-	-
210	BCC 120	-	-
309	BCW 101	#IOBIT08	Return, Bit08
408	BCW 102	IOBIT08	Data, Bit08
310	BCW 103	#IOBIT09	Return, Bit09
409	BCW 104	IOBIT09	Data, Bit09
214	BCW 105	#IOBIT10	Return, Bit10
410	BCW 106	IOBIT10	Data, Bit10
501	BCW 107	#IOBIT11	Return, Bit11
601	BCW 108	IOBIT11	Data, Bit11
502	BCW 109	#IOBIT12	Return, Bit12
602	BCW 110	IOBIT12	Data, Bit12
503	BCW 111	#IOBIT13	Return, Bit13
603	BCW 112	IOBIT13	Data, Bit 13
504	BCW 113	#IOBIT14	Return, Bit14
604	BCW 114	IOBIT14	Data, Bit14
505	BCW 115	#IOBIT15	Return, Bit15
605	BCW 116	IOBIT15	Data, Bit15
506	BCW 117	-	-
607	BCW 118	-	-
507	BCW 119	-	-
608	BCW 120	-	-
111	BCC 121	#IOWRT	Return, Write
211	BCC 122	IOWRT	Control, Write
112	BCC 123	#IOREAD	Return, Read
212	BCC 124	IOREAD	Control, Read
113	BCC 125	#IOCMD	Return, Command Select
213	BCC 126	IOCMD	Control, Command Select
301	BCC 127	#IOCLR	Return, Clear

Table 4-15. Hardware - Internal Cable Conductor Assignments (Continued)

J201 Pin	Backplane Pin	Signal	Function
401	BCC 128	IOCLR	Control, Clear
302	BCC 129	#IOINT	Return, Interrupt
402	BCC 130	IOINT	Control, Interrupt
303	BCC 131	#IOREADY	Return, Ready
403	BCC 132	IOREADY	Control, Ready
304	BCC 133	-	-
404	BCC 134	-	-
305	BCC 135	-	-
405	BCC 136	-	-
307	BCC 137	-	-
406	BCC 138	-	-
308	BCC 139	-	-
407	BCC 140	-	-
508	BCW 121	-	-
609	BCW 122	-	-
509	BCW 123	-	-
610	BCW 124	-	-
701	BCW 125	-	-
801	BCW 126	-	-
702	BCW 127	-	-
802	BCW 128	-	-
703	BCW 129	-	-
803	BCW 130	-	-
704	BCW 131	-	-
804	BCW 132	-	-
705	BCW 133	-	-
805	BCW 134	-	-
706	BCW 135	-	-
806	BCW 136	-	-
707	BCW 137	-	-
807	BCW 138	-	-
708	BCW 139	-	-
808	BCW 140	-	-

Table 4-16. Jack J1 Signals

Pin Number	Signal	Control Panel Destination
1	not used	-
2	not used	-
3	not used	-
4	not used	-
5	INLCKY,4H*MY	Resolution switch NO contact
6	GROUND	Resolution switch common
7	4L*MY	Resolution switch NC contact
8	9SELEFT (system processor ACC17)	Self test LED
9	+5 V	Not used
10	9BSWCLR (sync ACC49)	Reset switch NC contact
11	BSWCLR (sync ACW49)	Reset switch NO contact
12	GROUND	Test point ground
13	+12 V	Test point
14	-5 V	Test point
15	-12 V	Test point
16	+5 V	Test point

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4.5.8 Power Distribution System

With the exception of how strapping links are installed on the power supply, power distribution (figure F04-24) is the same for the 120 Vac and 220 Vac versions. Strapping links are preconfigured to suit these operating voltages; refer to illustration notes.

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4.5.9 Serial Link PCB

The serial link PCB can accommodate up to eight peripheral input devices. The PCB has 24 functional elements:

- Processor address bus driver
- Dual bus address bus decoder
- Processor data bus inverter
- Processor data bus controller
- Serial link CPU
- TTL address bus driver
- MOS data bus buffer
- System control logic
- Memory address decoder
- RAM
- ROM
- Wait logic
- TTL bus address decoder
- Clock pulse driver
- Blink controller
- Cursor control logic
- Sync driver
- Four cursor generators
- Cursor pattern selector
- Baud rate generator
- Self-test logic
- Configuration logic
- Baud rate select logic
- Four serial I/O controllers

Figure F04-25 is a simplified block diagram of the data and address buses. The MOS bus controllers consist of the blink controller and serial I/O controllers 1-4. Memory consists of the memory address decoder, RAM, and ROM.

Figure F04-26 shows control signal distribution except for the interrupt priority daisy chain signals, which are omitted for clarity and are shown separately.

4.5.9.a Processor Address Bus Driver. This driver supplies address bus drive. The driver converts address bits 4BZADR0-7 into bits 1BZA0-7.

4.5.9.b Dual Bus Address Decoder. When address bits 1BZA4-6 and signal 7BZIOP are active and 1BZA7 is inactive, this decoder derives signals 5ENBZCTC and 5ENBZPIO by decoding 1BZA2 and 3. When signal 5RAM10-11 goes active, the decoder derives 5RAMCUR1-4 by decoding 1BA8 and 9.

4.5.9.c Processor Data Bus Inverter. This bidirectional inverter supplies processor data bus drive. The inverter normally inverts bits 9BZDAT0-7 to become BZD0-7. But the inverter reverses direction and inverts BZD0-7 (to become 9BZDAT0-7) when: signals 8BZRD and either 5ENBZCTC or 5ENBZPIO go active, or 1BZINTA and 1BZIEI go active and BZIE0 remains inactive.

4.5.9.d Processor Data Bus Controller. This controller transfers data between the processor data bus and the MOS data bus, and consists of two Z80A-PIO ICs and supporting logic. The controller receives 11 control signals, a clock pulse, and four address bits that function as control signals, and generates two interrupt request signals. The 16 data bus lines are bidirectional. Address bit 1BZA0 goes active when a control byte is on data lines BZD0-7, and goes inactive when a data byte is on the data lines. Address bit A0 goes active when a control byte is on data lines D0-7, and goes inactive when a data byte is on the data lines.

When the system processor PCB has data for the serial link PCB, the system processor sends data bits 9BZDAT0-7, which become BZD0-7 after inversion. Also, signals 5ENBZPIO and 8BZIORQ go active latching the byte into the controller, which then activates *IINT. When *IORQ and 5M1 subsequently go active, signaling an interrupt acknowledge from the serial link CPU, the controller sends a vector on D0-7 identifying the controller as the interrupt source. The CPU then activates 5ENPIOSL, *IORQ, and *RD and the controller responds by sending the data byte to the CPU on D0-7.

When the CPU has data for the system processor PCB, the CPU activates signals 5ENPIOSL, *IORQ, and *RD and bit A1 to read controller status. The controller returns a control byte on D0-7, and activates signals 5ENPIOSL and *IORQ. The controller then sends 9BZINT to the system processor. When 8BZIORQ and 8BZM1 subsequently go active, the controller transmits an identifying vector on BZD0-7. Signals 5ENBZPIO, 8BZIORQ, and 8BZRD go active, and the controller transmits the data byte on BZD0-7. The system processor can read controller status by activating 5ENBZPIO, 8BZIORQ, 8BZRD, and bit 1BZA1.

If the DMA on the sync PCB communicates with the serial link PCB, the controller activates signal 9BZBUSY. In this state the system processor PCB cannot use the bus.

4.5.9.d.1 Serial link CPU. The serial link CPU consists of the Z80A-CPU and supporting logic. The CPU receives clock pulse 2CLKZ80 and three control signals, and generates 16 address bits and five control signals. The eight data bus lines, D0-7, are bidirectional.

The three basic CPU operations are memory read or write, input or output device read or write, and interrupt acknowledge. All operations are a combination of these three. A typical operation consists of three machine cycles. Cycle M1 is always the fetch cycle that fetches the operation code of the instruction to be executed. Cycles M2 and M3 transmit data between the CPU and memory or I/O devices.

The address and data outputs and control signals *MREQ, *IORQ, *RD, and *WR are tri-state outputs. When neither active nor inactive, these outputs assume a high impedance state. Signal *MREQ is active during a memory read or write cycle; *IORQ is active during a read or write cycle with an I/O device. Signal *RD goes active when the CPU attempts to receive data; *WR goes active when the CPU transmits data. Signal *WAIT delays CPU operation to allow time for another device to complete an operation. Signal *IINT is a request from another device for CPU access. Signal *M1 is active during an M1 cycle; *M1 and *IORQ go active together to indicate an interrupt acknowledge.

4.5.9.e TTL Address Bus Driver. This driver provides drive for the TTL address bus. The driver converts MOS address bus bits A0-15 into TTL address bus bits 1BA0-15.

4.5.9.f MOS Data Bus Buffer. This bidirectional buffer transfers data between the MOS data bus and the TTL data bus and supplies drive in both directions. When signal 5BDREAD is inactive, the buffer transfers data from D0-7 to 5BD0-7. When 5BDREAD goes active, the buffer reverses direction and transfers data from 5BD0-7 to D0-7.

4.5.9.g System Control Logic. This logic supplies control signal drive. The logic derives 12 control signals from eight inputs.

4.5.9.h Memory Address Decoder. Signal 5MREQ enables this decoder. When 5MREQ is active and 1A14 and 15 are inactive, the decoder derives five control signals by decoding bits 1BA11-13. Bits 1A14 and 15 inhibit the decoder.

4.5.9.i RAM. RAM consists of two 1K x 4-bit static RAM ICs. Signal 5RAM8-9 enables RAM. When 5RAM8-9 and 5WR go active, RAM stores data received on 5BD0-7 in locations specified by address bits 1BA0-9. When 5RAM8-9 goes active and 5WR remains inactive, RAM transmits, on 5BD0-7, data stored in locations specified by 1BA0-9.

4.5.9.j ROM. ROM consists of two 4K x 8-bit erasable PROM chips. When address bit 1BA11 and signals 5RD, 5ROM, and either 5ROMMSB or 5ROMLSB go active, ROM transmits, on 5BD0-7, data stored in locations specified by 1BA0-10 and either 5ROMMSB or 5ROMLSB.

4.5.9.k Wait Logic. This logic generates signal *WAIT which goes active at the first 2CZ80 clock pulse after either 5RAM8-9 or 5ROM goes active, and remains active for two more 2CZ80 pulses. Signal 8RESET resets the logic. Signal *WAIT goes active when a memory operation is in progress. In this state the CPU waits until *WAIT goes inactive.

4.5.9.l TTL Bus Address Decoder. This decoder supplies 27 signals that control serial link PCB operations. The decoder derives the signals by decoding address bits 1BA0-7 under control of five input control signals.

4.5.9.m Clock Pulse Driver. The clock pulse driver supplies clock pulse drive for serial link PCB ICs. The driver develops eight outputs from six differential inputs from the sync PCB.

4.5.9.n Blink Controller. This controller consists of a Z80A-CTC chip and a flip-flop. The controller receives seven control signals, two address bits that function as control signals, and clock pulse 2CLKZ80. The controller generates two outputs. The eight data lines are bidirectional.

The controller has four channels that can function as counters or timers. Address bits A0 and A1 select one of the four channels. Channel 1 receives pulse 1HBLANKA, and channels 2 and 3 receive 1VBLANK. Channel 0 is not used. At power ON the serial link CPU programs channels 1, 2, and 3 to generate an interrupt at a specified count. Each time 1VBLANK goes active, the controller activates interrupt signal *IINT which goes to the CPU. After counting 255

1HBLANK pulses, the controller also activates *IINT. The CPU uses these interrupts to keep track of the vertical and horizontal blanking. Signal 5BLKCLK goes active after 20 1VBLANK pulses and continues to change state at each succeeding 20th pulse. This is the signal that makes the cursor blink. When the CPU activates *M1 and *IORQ to signal an interrupt acknowledge, the controller sends a vector on D0-7 to identify one of the channels as the interrupt source. The CPU then activates 5ENCTCSL, *IORQ, and *RD and selects the identified channel with A0 and A1. The controller responds by sending a data byte on D0-7.

4.5.9.o Cursor Control Logic. This logic derives 12 control signals from nine inputs and three clock pulses. The logic derives 1HBLANKA and 1HBLANKB from 9THBBB, 7FQ, and 7HQ; 5CURT1, 6CURT1, and 6CURT4 from 9THMMM and 7FQ; 5SELCLK and 6SELCLK from 3H*MY, 3L*MY, 3MY*559, 2FQ, and 2HQ; 8VBSHORT from 9TVMMM, 1VBLANK, and 3HQ; and 5CUR1VEN through 5CUR4VEN from 9THMMM, 8INTLC, 3H*MY, 9TVMMM, 9TVBBB, 1EVEN, 7FQ, and 3HQ. The 12 outputs control the four cursor generators.

4.5.9.p Sync Driver. This driver supplies sync control signal drive. The driver converts 9PORCLR into 8RESET, 9TVFFF into 1EVEN, and 9CSSS into differential outputs 9CS1, 2, 5, and 6 and returns #CS1, 2, 5, and 6. Five other conversions leave the mnemonic unchanged except for the numerical prefix.

4.5.9.q Cursor Generators. Cursor generators 1-4 are functionally identical but signal names vary. The following description is for generator 1 followed by a listing of signal differences for 2, 3, and 4. The programmer can program each generator independently to generate a selected cursor pattern. Each generator (figure F04-27) consists of 7 functional elements:

- Element register
- Element counter
- Line register
- Line counter
- Cursor address selector
- Cursor RAM logic
- Cursor output register

4.5.9.q.1 Element register. This register receives initial-horizontal-position data on 5BD0-7. After signals 5EMSBCS and 5ELSBCS go active, the next 5CUR1LD pulse loads the data into the register. After 5ELSBCS goes active, the register converts bits 5BD0-7 into bits 6E1D0-7. After 5EMSBCS goes active, the register converts 5BD0 and 1 into 6E1D8 and 9.

4.5.9.q.2 Element counter. This binary counter controls horizontal cursor position. After signal 5CURT1 goes active, the next 5SELCLK pulse loads initial-position data received on 6E1D0-9 into the counter. After 5CURT1 goes inactive, the counter counts 5SELCLK pulses. Signal 1HBLANKA inhibits the counter. When 6HBLANK1 is active, 1RAM1LTC goes active after count 7. Signal 1RAM1LTH also goes active at the first 5SELCLK pulse after 6CURT4 goes active. At the last count, 1ESEL1 goes active.

4.5.9.q.3 Line register. This register receives initial-vertical-position data on 5BD0-7. After signals 5LMSBCS and 5LLSBCS go active, the next 5CUR1LD pulse loads the data into the register. After 5LLSBCS goes active, the register converts bits 5BD0-7 into 6L1D0-7. After 5LMSB goes active, the register converts 5BD0 and 1 into 6L1D8 and 9.

4.5.9.q.4 Line counter. This binary counter controls vertical cursor position. After signal 8VBSHORT goes active, the next 7FQ clock pulse loads initial-position data received on 6L1D0-9 into the counter. After 5CUR1VEN goes active, the next 7FQ pulse increments the counter. At the last count, 1LSEL1 goes active.

4.5.9.q.5 Cursor address selector. This selector supplies the address for the cursor RAM. When signal 5RAMCUR1 is inactive, the selector transfers address data from 1E1A3 and 4 and 1L1A0-4 to 1CUR1A0-6, respectively, and converts signal 2BLINK1 into bit 1CUR1A7. During a cursor RAM write cycle, 5RAMCUR1 goes active, and the selector transfers address data from 1BA0-7 to 1CUR1A0-7.

4.5.9.q.6 Cursor RAM logic. This logic (figure 4-50) has three functional elements:

- Cursor RAM
- RAM register
- Cursor data selector

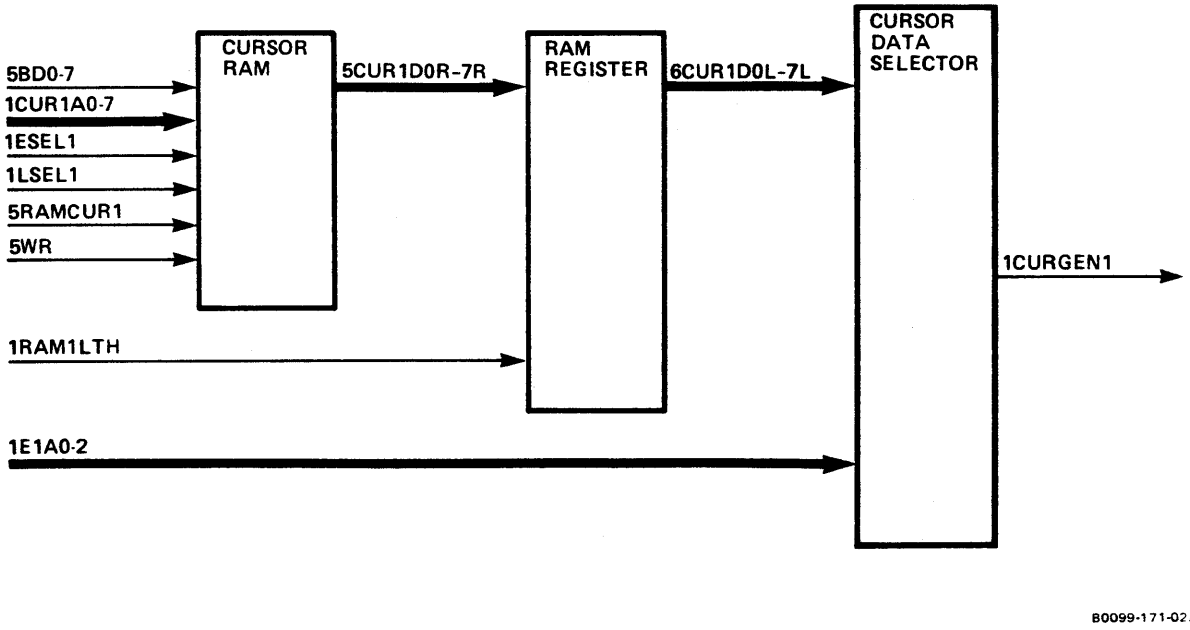

Figure 4-50. Cursor RAM Logic

Cursor RAM consists of two 256 x 4-bit static RAM ICs and supporting logic. When signals 5RAMCUR1 and 5WR go active, the RAM stores cursor pattern data received on 5BD0-7 in the locations specified by address bits 1CUR1A0-7. With 1ESEL1 and 1LSEL1 active and 5WR inactive, the RAM sends data stored in locations specified by bits 1CUR1A0-7. The RAM register receives this data on 5CUR1D0R-7R. Signal 1RAM1LTH latches the data into the register, which transfers the data to 6CUR1D0L-7L. The cursor data selector converts the data to serial form. Element address bits 1E1A0-2 sequentially select the data bits for transmission as serial data on line 6CURGEN1.

4.5.9.q.7 Cursor output register. This register synchronizes cursor data received on 1CURGEN1 with clock pulse 8HQ, and transmits the synchronized data on 6CURGEN1. Data bits 5BD0-7 control register operation. Signal 5BV1LD latches the data bits into the register. Bits 1 and 2 override data received on 1CURGEN1. When latched bit 5BD1 is active, 6CURGEN1 goes inactive, blanking the cursor pattern. When 5BD2 is active, 6CURGEN1 goes active. This lights the entire CRT screen so the lightpen can detect a signal. When 5BD0 is active, the register converts signal 5BLKCLK into 2 BLINK1, which goes to the cursor address selector.

4.5.9.q.8 Signal variations. Table 4-17 lists equivalent signals for cursor generators 1-4.

Table 4-17. Cursor Generator Equivalent Signals

1	2	3	4
5CUR1LD	5CUR2LD	5CUR3LD	5CUR4LD
5CUR1VEN	5CUR2VEN	5CUR3VEN	5CUR4VEN
5RAMCUR1	5RAMCUR2	5RAMCUR3	5RAMCUR4
5BV1LD	5BV2LD	5BV3LD	5BV4LD
6CURGEN1	6CURGEN2	6CURGEN3	6CURGEN4
1HBLANKA	1HBLANKA	1HBLANKB	1HBLANKB
5CURT1	5CURT1	6CURT1	6CURT1
8HQ	8HQ	9HQ	9HQ

4.5.9.r Cursor Pattern Selector. This selector can transmit the cursor pattern from any of the four cursor generators on any of the four cursor output channels. Data bits 5BD0-7 make the selections. Signal 5VIDLD latches the data into the selector. Clock pulse 7HQ synchronizes the outputs. The selector converts the selected serial cursor data to ECL levels and transmits the data on differential output 8CURS1-4 and #CURS1-4.

4.5.9.s Baud Rate Generator. A 2.4576-MHz crystal oscillator generates the basic baud rate signal. The generator divides the frequency to rates selected by data bits 5BD0-7. Signal 5BAUDLD loads bits 5BD0-7 into locations selected by address bits 1BA0 and 1. The generator supplies baud rate pulses 5SIOCLK1-8.

4.5.9.t Self-Test Logic. This logic consists of the self-test register and the self-test LED. When signal 8RESET goes active, 5LED goes active, lighting the LED. When 5TESTLED goes inactive after going active, 5LED goes inactive, and the LED goes off.

4.5.9.u Configuration Select Logic. This logic consists of two banks of switches and two line drivers. The switches select the desired configuration. The CPU can read switch status by sequentially activating 5JKSEL1 and 5JKSEL2. When 5JKSEL1 goes active, the logic transmits data from switchbank on 5BD0-7. When 5JKSEL2 goes active, the logic transmits data from switchbank 2.

4.5.9.v Baud Rate Select Logic. This logic consists of three banks of switches and three line drivers. The switches select the desired baud rate for each peripheral device. The CPU can read switch status by sequentially activating signals 5BRSEL1, 2, and 3. When these signals go active, the logic transmits data from switchbanks 1, 2, and 3, respectively, on 5BD0-7.

4.5.9.w Serial I/O Controllers. Serial I/O controllers 1-4 can interface with up to eight peripheral devices. All inputs and outputs are differential, but can be changed to RS232 if desired. Each controller receives five control signals, two address bits that function as control signals, clock pulse 2CLKZ80, two baud rate pulses, and four differential inputs. The controllers generate signal *IINT and four differential outputs. The eight data lines are bidirectional. Controllers 2 and 4 each have two additional inputs and four outputs that are not used but are available for conversion to RS232. Controllers 1 and 3 each use two of the outputs not used by 2 and 4. Each controller has a Z80-SIO IC and supporting logic. Each Z80-SIO has two serial I/O channels, ports A and B. Connectors J1 and J2 connect, through logic, to ports A and B, respectively, of controller 1.

Signal 5ENSIOA enables controller 1. Address bit A1, when active, selects port B. When inactive, address bit A1 selects port A. Bit A0 goes active when a control byte is on data lines D0-7; bit A0 goes inactive when a data byte is on the data lines.

When a device connected to J1 sends serial data on differential input lines RD1 and *RD1, controller 1 activates interrupt request signal *IINT, which goes to the serial link CPU. Signals *M1 and *IORQ go active to signal an interrupt acknowledge and the controller subsequently transmits a vector on D0-7 identifying port A as the interrupt source. Once the CPU is ready to accept data, 5ENSIOA, *IORQ, and *RD go active, and the controller converts the serial data to parallel data. The controller transmits this parallel data on D0-7.

When the CPU has data for the device at J1, 5ENSIOA and *IORQ go active, and the controller converts data received on D0-7 to serial form. The controller then sends the data to the device on SD1 and *SD1. In addition, the controller sends composite sync signal 9CS1, which is needed by a lightpen, but is not used by other devices. Baud rate pulse 5SIOCK1 clocks serial data transfers. Signals 9CS1 and #CS1 come from the sync driver. Signal #CS1 is not used. Operation is the same for a device connected to J2 except that bit A1 is active and 5SIOCK2 replaces 5SIOCK1.

Controller 3 is functionally identical to 1. Controllers 2 and 4 do not receive composite sync signals, thus controllers 2 and 4 cannot accept a lightpen. Otherwise, 2 and 4 are functionally identical to 1. Table 4-18 lists corresponding signals for controllers 1-4.

Table 4-18. Serial I/O Controller Corresponding Signals

1	2	3	4
5ENSIOA	5ENSIOB	5ENSIOC	5ENSIOD
RD1	RD2	RD3	RD4
*RD1	*RD2	*RD3	*RD4
SD1	SD2	SD3	SD4
*SD1	*SD2	*SD3	*SD4
9CS1	--	9CS5	--
9CS2	--	9CS6	--
5SIOCK1	5SIOCK3	5SIOCK5	5SIOCK7
5SIOCK2	5SIOCK4	5SIOCK6	5SIOCK8

4.5.9.x Interrupt Priority Daisy Chain. The processor data bus controller, blink controller, and serial I/O controllers 1-4 are connected in a daisy chain (figure 4-51) that determines which controller gets priority when two or more controllers have data for the serial link CPU at the same time. The processor data bus controller gets top priority. Each of the other controllers receives an interrupt enable signal that is normally active. But when a controller sets interrupt request signal *IINT active, no lower-priority controller can activate *IINT while the higher-priority controller is busy. For example, when serial I/O controller 2 activates *IINT, interrupt enable signals X3 and X4 go inactive and serial I/O controllers 3 and 4 cannot activate *IINT until X3 and X4 go active again.

4.5.9.y Data Flow. In a typical operation, a peripheral device sends data to the serial link PCB for transfer to the system processor PCB. A typical operation consists of these steps:

- Internal interrupt request
- Internal vector transfer
- Data input control
- Serial data input
- RAM control
- RAM storage
- RAM readout control
- RAM readout
- ROM readout control
- ROM readout
- Data transfer control
- Controller status readout

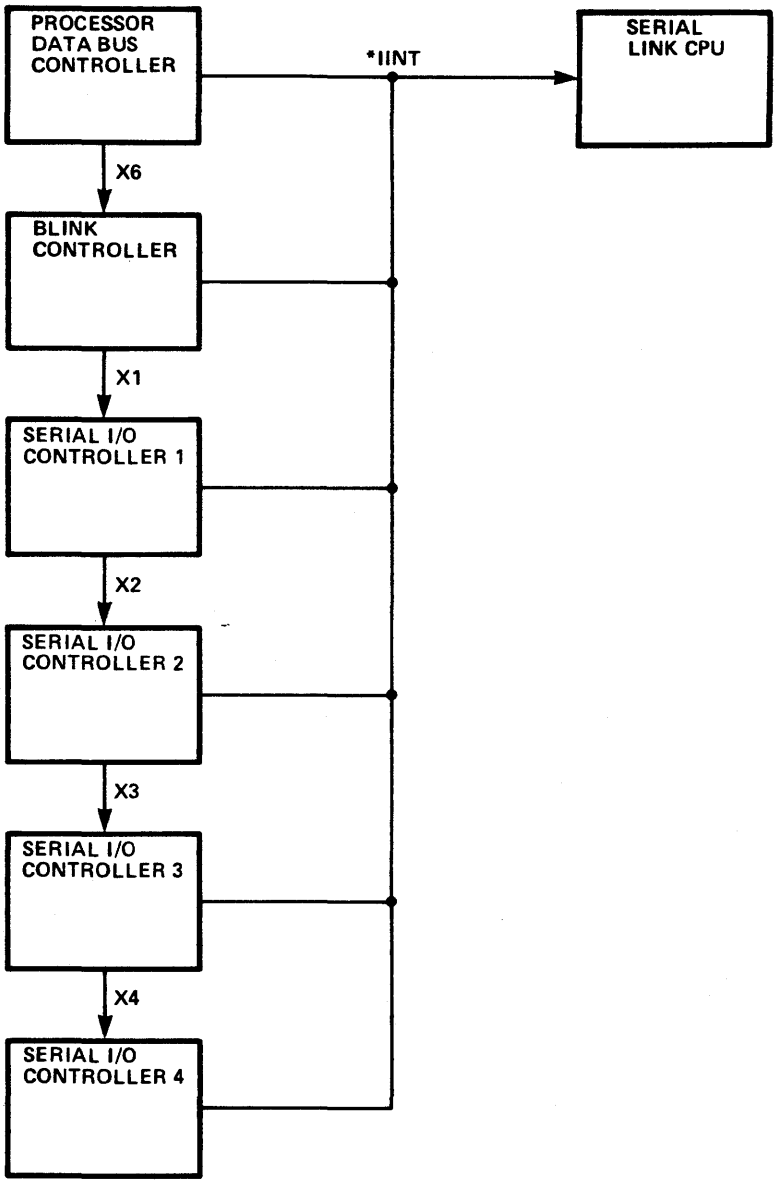

Figure 4-51. Interrupt Priority Daisy Chain

- ¤ External interrupt request
- ¤ External vector transfer
- ¤ Data output control
- ¤ Data output

4.5.9.y.1 Internal interrupt request. When a peripheral device connected to J1 sends serial data on RD1 and *RD1 (figure 4-52), serial I/O controller 1 responds by sending interrupt request signal *IINT to the serial link CPU. Once the CPU is ready to accept data, *M1 and *IORQ go active, signaling an interrupt acknowledge.

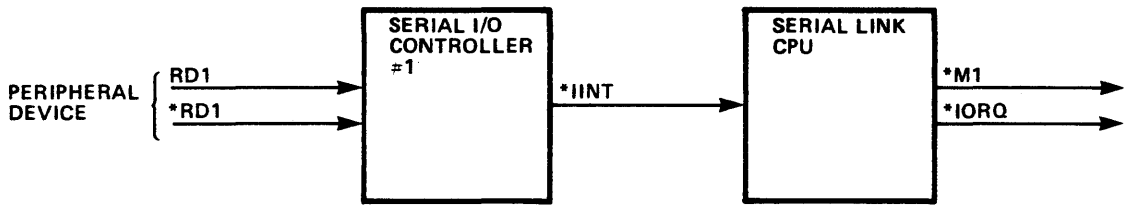

Figure 4-52. Internal Interrupt Request

4.5.9.y.2 Internal vector transfer. After receiving an interrupt acknowledge, serial I/O controller 1 generates a vector that identifies controller port A as the interrupt source. Signals *M1 and *IORQ then go active and the controller sends a vector to the serial link CPU on D0-7.

4.5.9.y.3 Data input control. To develop controller enable signal 5ENSIOA (figure 4-53), the serial link CPU transmits a control byte on address lines A2-7. The TTL address bus driver transfers this byte to 1BA2-7. The CPU also activates *IORQ and *RD, and the system control logic converts *IORQ into 6IOP if *M1 remains inactive. When 6IOP goes active, the TTL bus address decoder derives 5ENSIOA by decoding the byte on 1BA2-7.

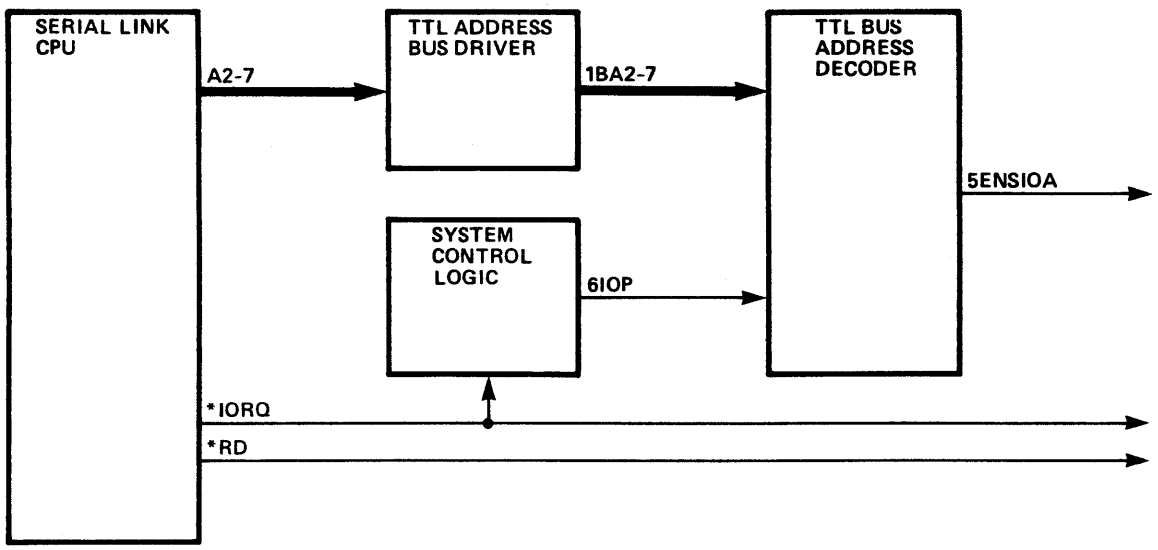

Figure 4-53. Data Input Control

4.5.9.y.4 Serial data input. Serial I/O controller 1 transfers data from the peripheral device to the serial link CPU. When signals 5ENSIOA (figure 4-54), *IORQ, and *RO go active, the controller converts the serial data received on RD1 and *RD1 to parallel data. The controller then sends the parallel data to the CPU on DO-7.

4.5.9.y.5 RAM control. Typically, the serial link CPU stores received data in RAM. To develop RAM control signal 5RAM8-9 (figure 4-55), the CPU transmits a control byte on A11-15, and activates *MREQ. The TTL address bus driver transfers the byte to 1BA11-15, and the system control logic converts *MREQ to 5MREQ. When 5MREQ goes active, the memory address decoder derives signal 5RAM8-9 by decoding the control byte.

4.5.9.y.6 RAM storage. The serial link CPU transmits data on DO-7 (figure 4-56) for storage in RAM and transmits a RAM address on AO-9. In addition, the CPU activates *WR, which becomes 5WR. RAM receives the data on 5BDO-7, and the address on 1BAO-9. When 5WR and 5RAM8-9 go active, RAM stores the data in the addressed location.

4.5.9.y.7 RAM readout control. Once the system processor PCB is ready to accept data, the serial link CPU reads out data stored in RAM. To develop readout control signal 5BDREAD (figure 4-57), the CPU activates signals *MREQ and *RD. As a consequence, the system control logic activates 5MREAD, which becomes 5BDREAD.

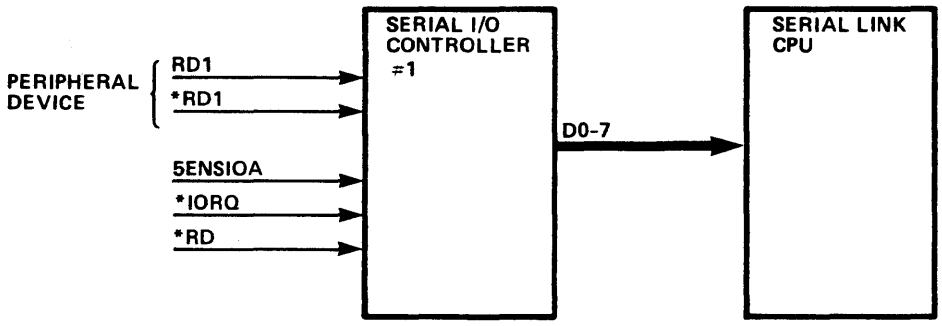

Figure 4-54. Serial Data Input

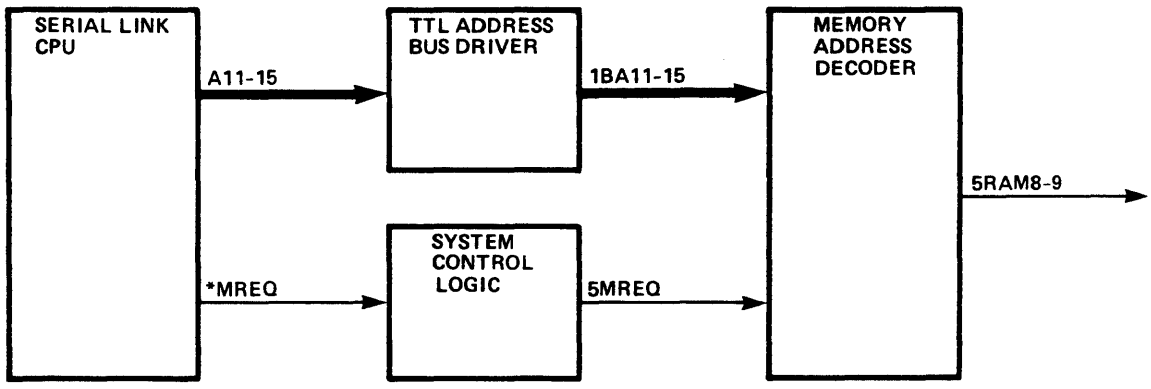

Figure 4-55. Serial Link RAM Control

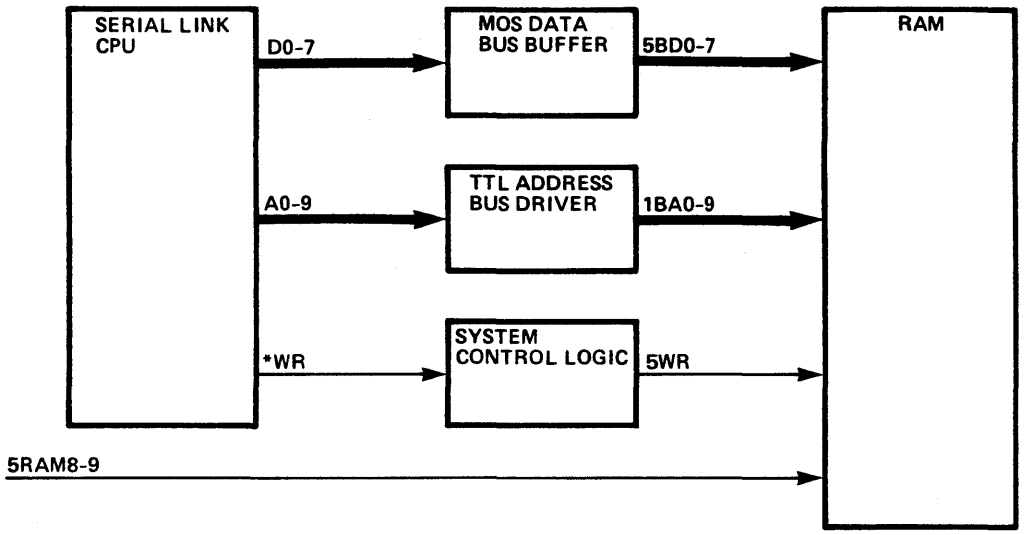

Figure 4-56. Serial Link RAM Storage

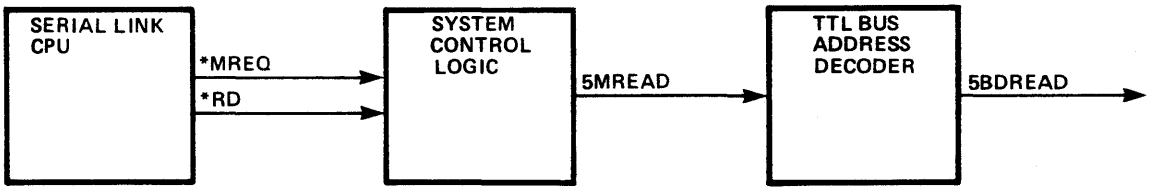

Figure 4-57. Serial Link RAM Readout Control

4.5.9.y.8 RAM readout. With 5RAM8-9 (figure 4-58) active, RAM transmits stored data as specified by address bits 1BA0-9. As soon as 5BDREAD goes active, the MOS data bus buffer transfers data over D0-7 to the serial link CPU.

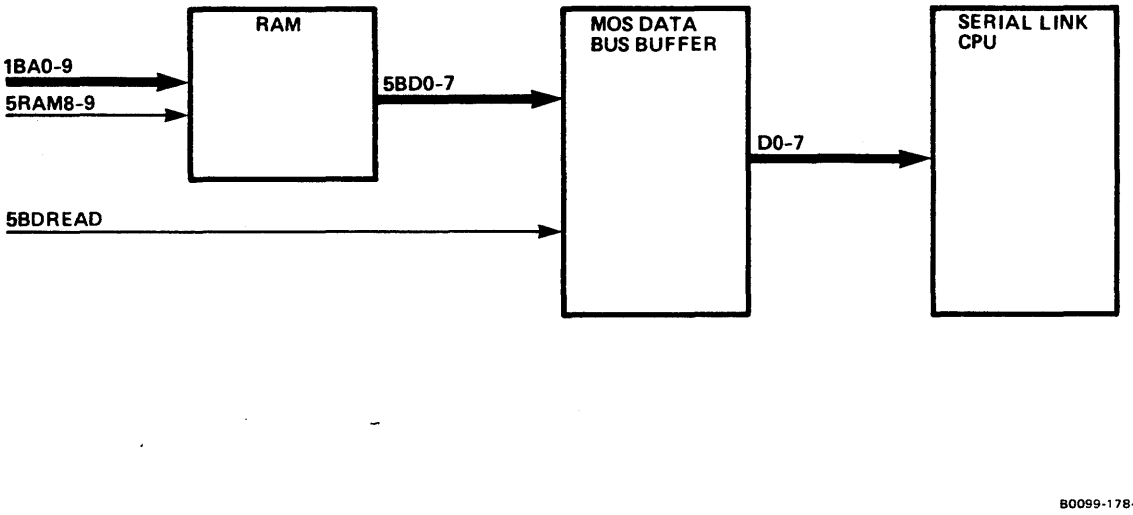

Figure 4-58. Serial Link RAM Readout

4.5.9.y.9 ROM readout control. The serial link CPU obtains program data from ROM. To develop the necessary ROM control signals, the CPU transmits a ROM address over A0-11 and a control byte on A11-15 (figure 4-59). In addition, the CPU activates signals *MREQ and *RD. The TTL address bus driver transfers the address and the control byte to 1BA0-15. When *MREQ and *RD go active, the system control logic activates 5MREQ, 5RD, and 5MREAD. Signal 5MREAD becomes 5BDREAD. With 5MREQ active, the memory address decoder derives signals 5ROMMSB, 5ROMLSB, and 5ROM by decoding the control byte on 1BA11-15.

4.5.9.y.10 ROM readout. With signals 5ROM (figure 4-60), 5RD, and either 5ROMMSB or 5ROMLSB active, ROM transmits stored data over 5BD0-7. Data is specified by address bits 1BA0-11 and either 5ROMMSB or 5ROMLBS. After 5BDREAD goes active, the MOS data bus buffer transfers data over D0-7 to the serial link CPU.

4.5.9.y.11 Data transfer control. To communicate with the processor data bus controller, the serial link CPU transmits a control byte over A2-7 (figure 4-61). At the same time, the CPU activates bit A1 and signals *RD and *IORQ, and *IORQ becomes 6IOP. Once 6IOP goes active, the TTL bus address decoder derives signal 5ENPIOSL by decoding the control byte, received on 1BA2-7.

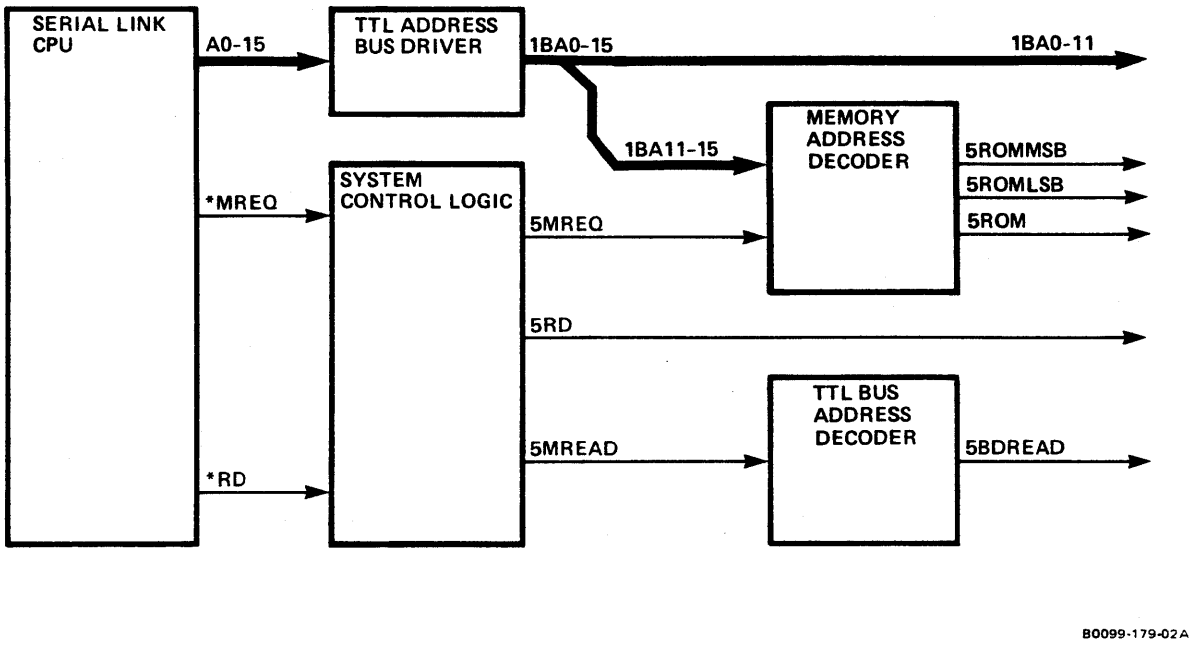

Figure 4-59. ROM Readout Control

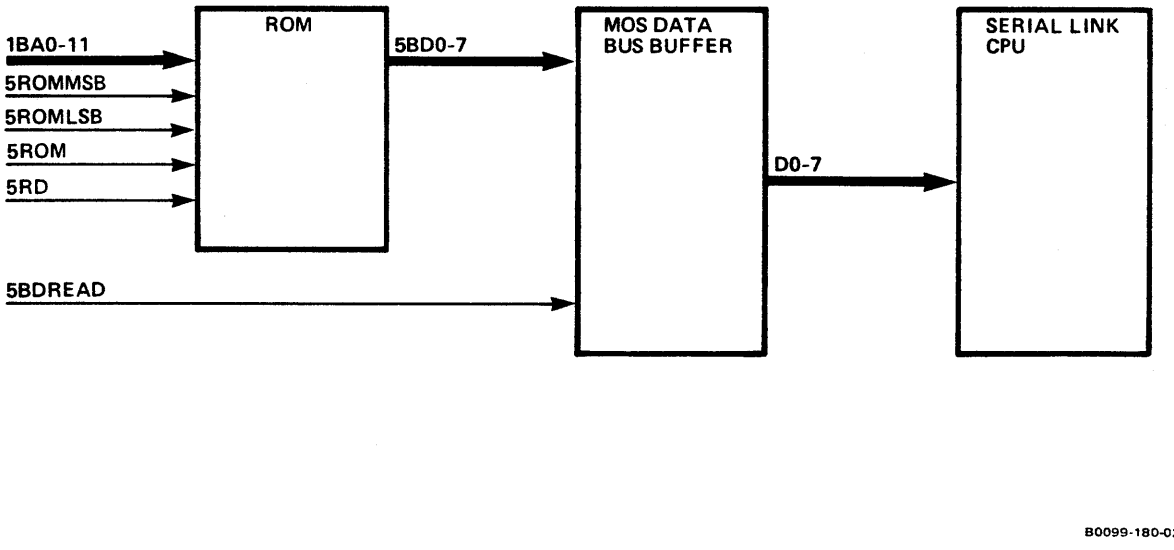

Figure 4-60. Serial Link ROM Readout

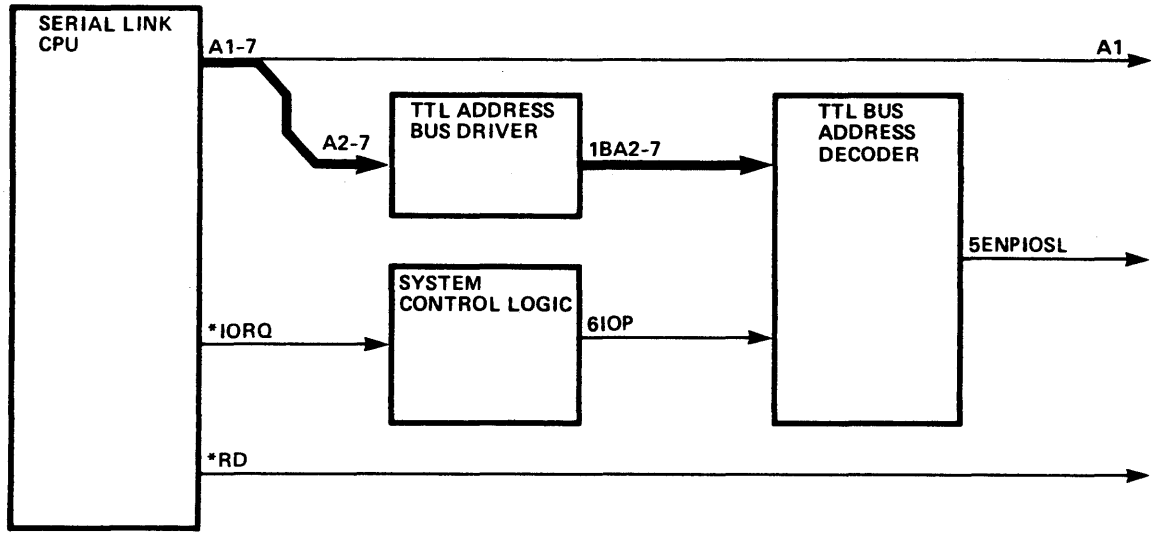

Figure 4-61. Data Transfer Control

4.5.9.y.12 Controller status readout. To determine processor data bus controller status, the serial link CPU sets bit A1 and signals 5ENPIOSL, *IORQ, and *RD active (figure 4-62). The controller responds by sending status data to the CPU to indicate whether the controller is ready to accept data.

4.5.9.y.13 External interrupt request. With the processor data bus controller ready to accept data, the serial link CPU sends peripheral device data on D0-7 (figure 4-63). Signals *IORQ and 5ENPIOSL go active, latching the data into the controller. Subsequently the controller sends interrupt request signal 9BZINT to the system processor PCB.

4.5.9.y.14 External vector transfer. The system processor acknowledges an interrupt by setting 9BZM1 and 9BZIORQ active (figure 4-64). The system control logic then responds by activating 8BZM1, 8BZIORQ, and 1BZINTA. Once 8BZM1 and 8BZIORQ go active, the processor data bus controller transmits a vector on BZD0-7, identifying the serial link PCB as the interrupt source. After 1BZINTA goes active, the processor data bus inverter transfers the vector to 9BZDAT0-7, going to the system processor PCB.

4.5.9.y.15 Data output control. After receiving a vector, the system processor PCB sends a control byte on address lines 4BZADR0-7 (figure 4-65) and activates signals 9BZIORQ and 9BZRD. As a consequence, the system control logic activates 7BZIOP, 8BZIORQ, and 8BZRD. Once 7BZIOP goes active, the dual bus address decoder derives signal 5ENBZPIO by decoding the control byte, which the decoder receives on 1BZADR0-7.

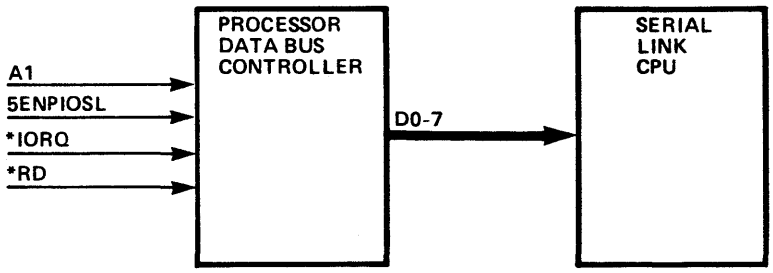

Figure 4-62. Controller Status Readout

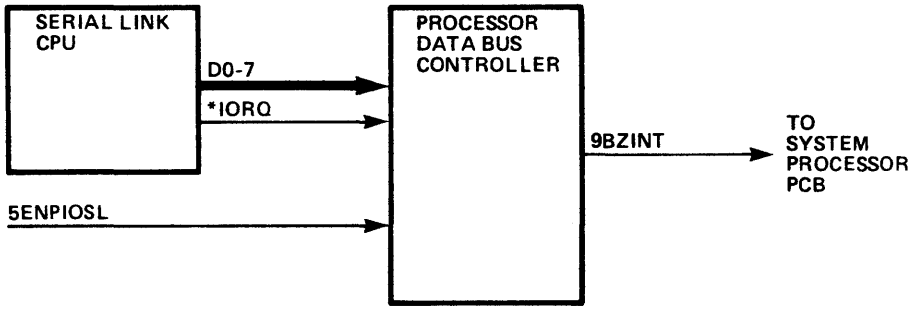

Figure 4-63. External Interrupt Request

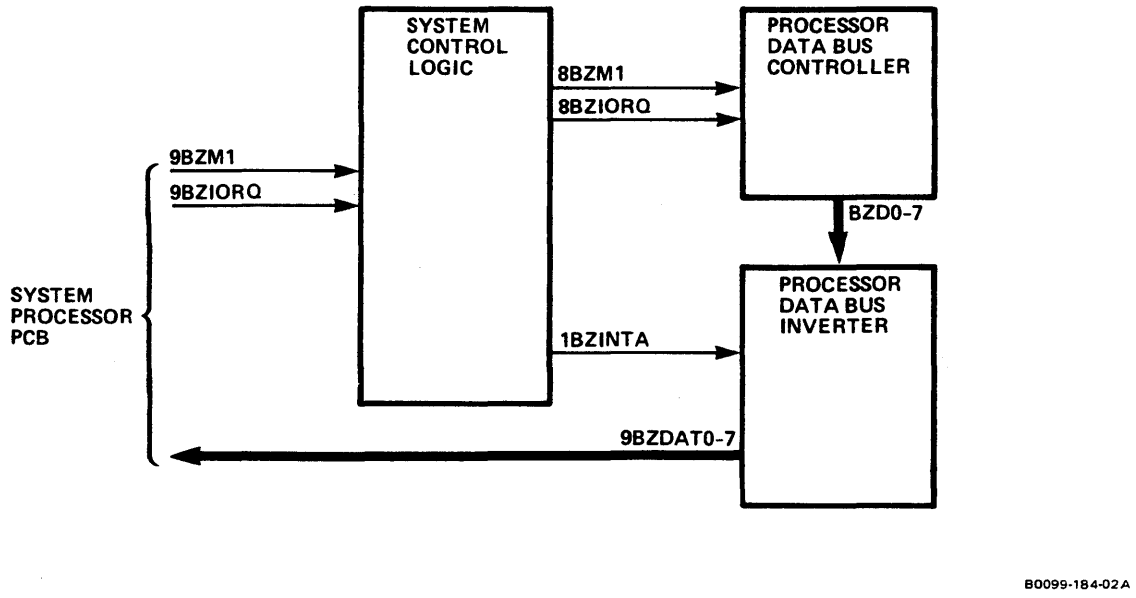

Figure 4-64. External Vector Transfer

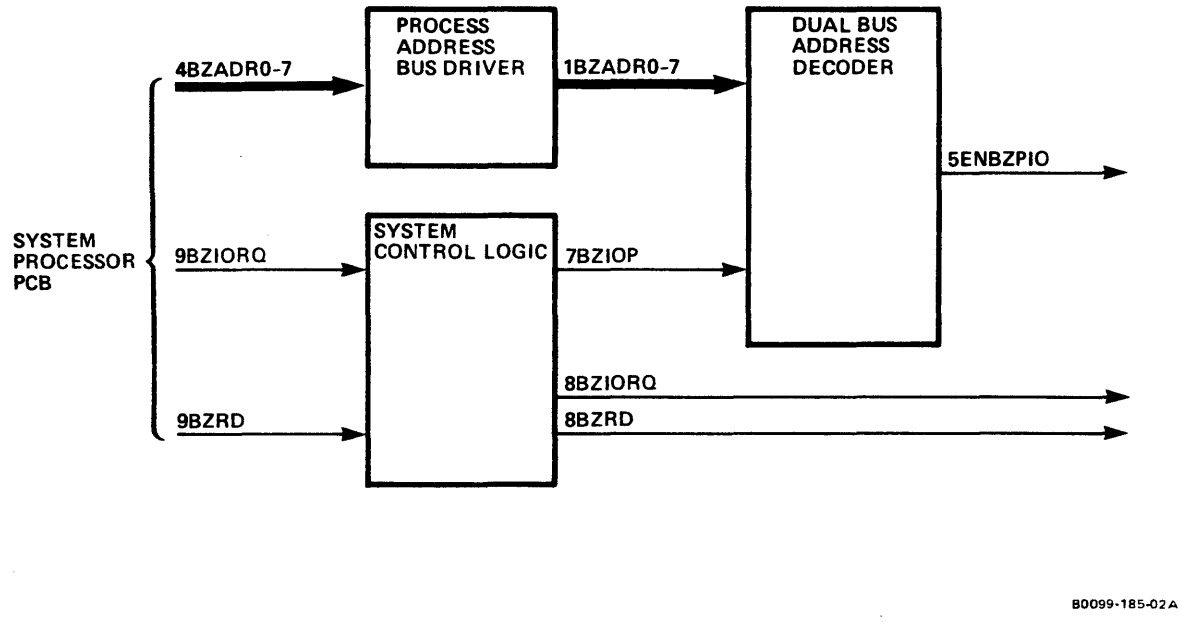

Figure 4-65. Data Output Control

4.5.9.y.16 Data output. The processor data bus controller receives signals 5ENBZPIO, 8BZIORQ, and 8BZRD (figure 4-66), and transmits the latched data on BZD0-7. The processor data bus inverter, which also receives 5ENBZPIO and 8BZRD, inverts the data, and sends the inverted data to the system processor PCB on 9BZDAT0-7.

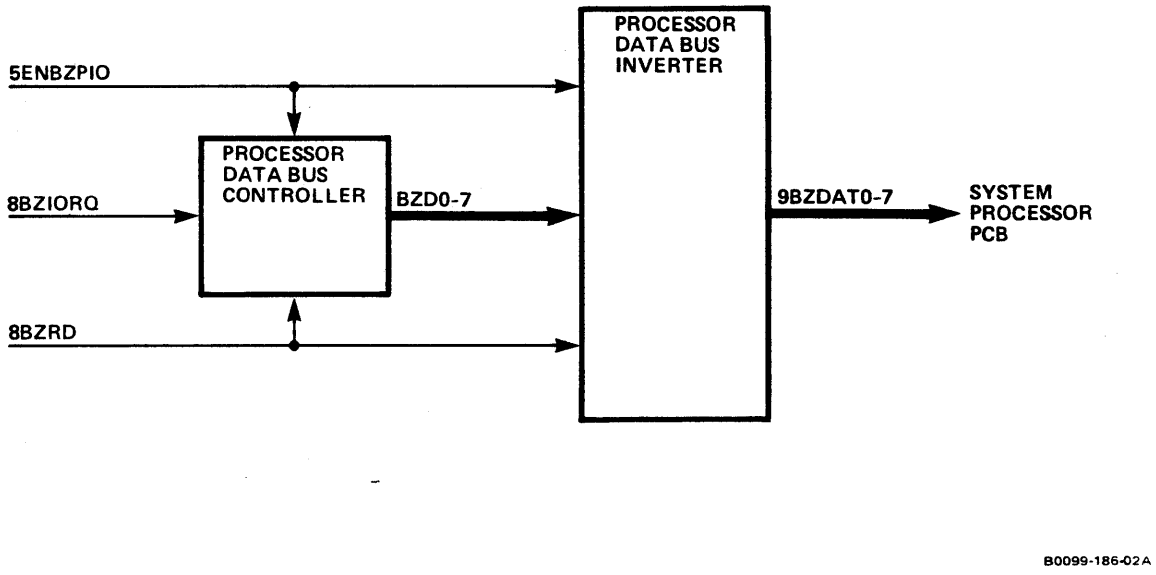

Figure 4-66. Data Output

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4.5.10 Expansion PCB

The expansion PCB (figure F04-28) has 17 functional elements in use and four installed but not used. The expansion schematic diagram shows four additional elements that are not installed. The 17 functional elements in use are:

- Bus driver
- Control logic
- CAS logic
- RAS logic
- Wait logic
- Interrupt driver
- RAM control
- RAM
- ROM control
- ROM
- Address decoder
- Data bus buffer
- Clock driver
- Daisy chain interrupt logic
- Baud rate generator
- Busy logic
- Serial I/O controller

The four elements that are installed but not used are:

- IEEE I/O buffer
- Address generator
- Simplified parallel I/O buffer
- Timing control

The four elements that are not installed are:

- ALU
- CTC
- IEEE I/O controller
- Simplified parallel I/O controller

4.5.10.a Bus Driver. This logic (figure 4-67) converts processor bus address bits and control signals into expansion bus address bits and control signals, and supplies the drive for the logic served by the expansion bus. Address bits 4BZADR0-18 become ADR0-18.

4.5.10.b Control Logic. This logic receives two control signals and two clock pulses and generates five control signals.

4.5.10.c CAS Logic. This logic (figure 4-68) generates RAM control signal 1CAS when input signals 2EMRQ and EMRQ are active and 8ERFSH is inactive. This means that 1CAS is active during a RAM read or write operation but not during a refresh cycle.

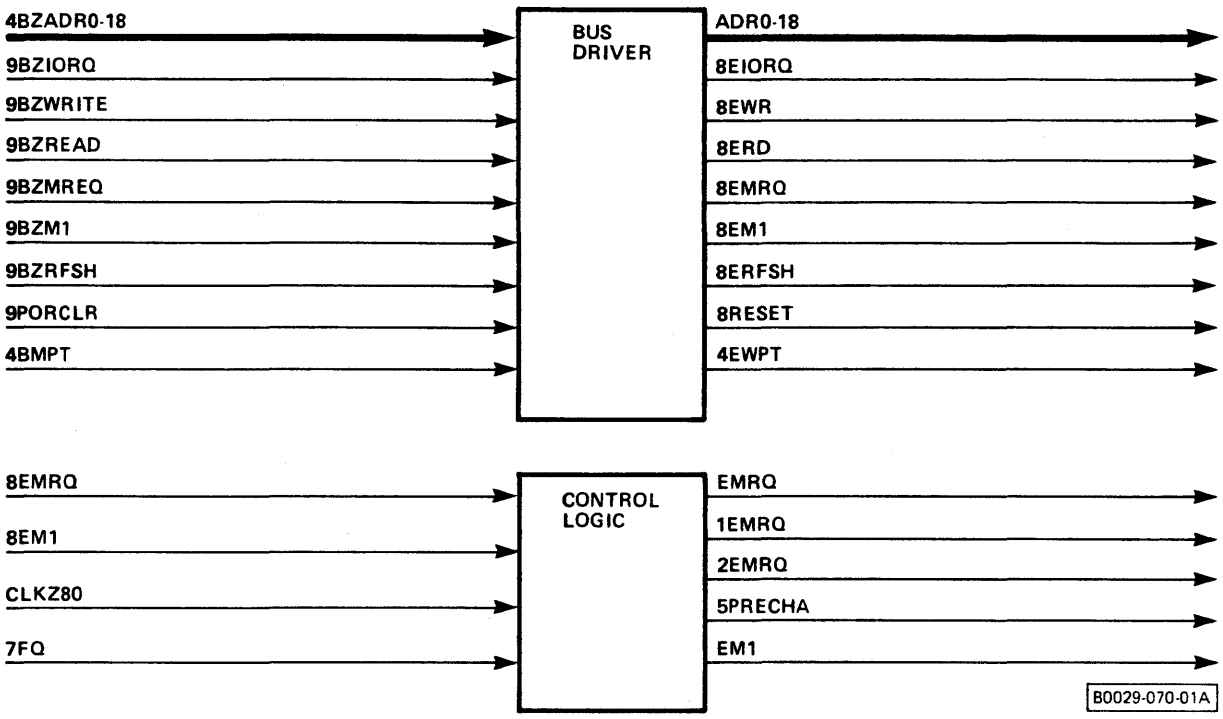

Figure 4-67. Bus Driver and Control Logic

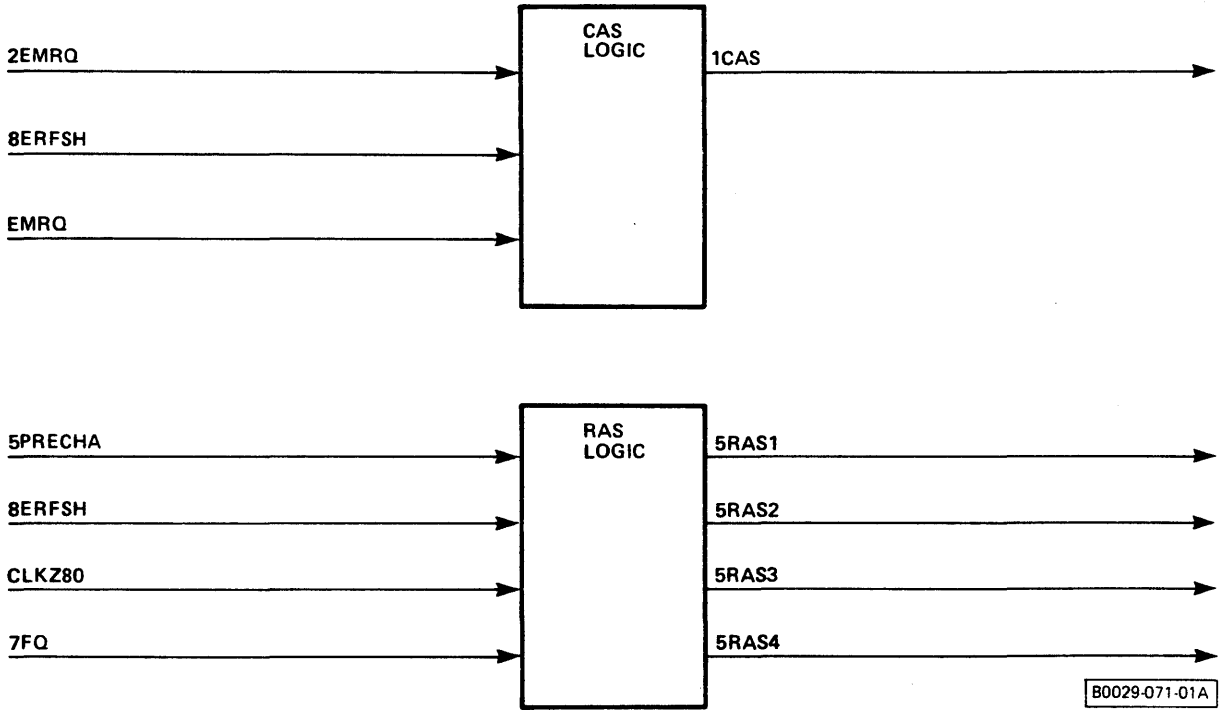

Figure 4-68. CAS and RAS Logic

4.5.10.d RAS Logic. When signal 5PRECHA becomes active, the RAS logic generates four RAM control signals. When 8ERFSH becomes active, the four outputs become active at the next 7FQ clock pulse and remain active until the second subsequent CLKZ80 pulse. This means that the outputs are active during a RAM read or write operation or a refresh cycle, since 5PRECHA is active during memory operations.

4.5.10.e Wait Logic. During a CPU fetch cycle when the CPU wants to read data out of ROM, signals 8EMRQ, 8EM1, and ROMEN (figure 4-69) become active, and the wait logic generates 9BZWAIT at the next CLKZ80 clock pulse. At the following CLKZ80 pulse, 9BZWAIT becomes inactive again. Signals 5ENIEEE and 8WAITMA are not used.

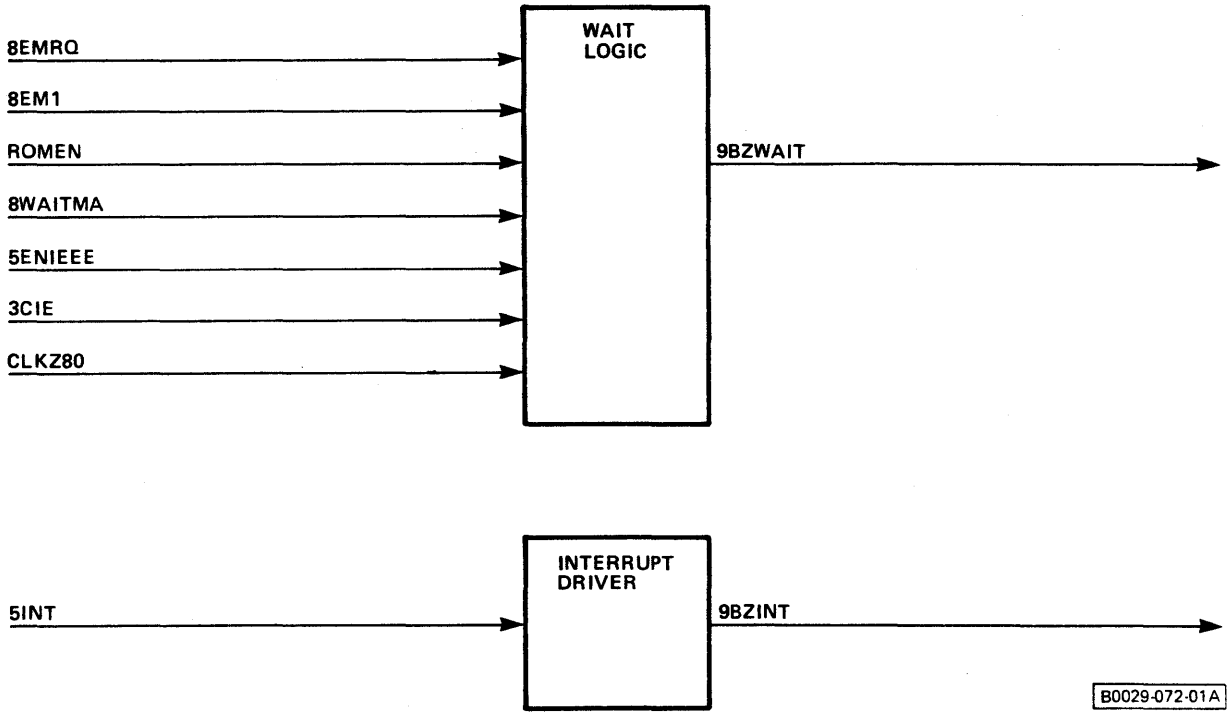

Figure 4-69. Wait and Interrupt Logic

4.5.10.f Interrupt Driver. This logic converts signal 5INT into 9BZINT, which goes out on the processor bus. The circuit supplies the drive for the logic served by the bus.

4.5.10.g RAM Control. This logic receives address bits ADR14-18 and generates eight column-address-strobe signals and 5RAMEN which control RAM operation. RAM control has switches that select the starting and ending RAM address locations in accordance with the number and capacity of RAM chips installed.

4.5.10.h RAM. RAM consists of sixty-four 16K x 1-bit dynamic RAMS. During a read cycle RAM receives signals 1EMRQ, 8ERD, 5RAMEN, 6RAS1-4, and 7FQ, an address byte on lines ADR0-13, and one of the eight column-address-strobe signals from RAM control. RAM responds by transmitting, on data lines DAT0-7, the bit contained in the addressed location.

During a write cycle RAM receives all the read-cycle signals plus 8EWR and data bits on lines DAT0-7. RAM responds by storing the received data bit in the addressed location. Memory protect signal 4EWPT inhibits write operation.

RAM is a dynamic memory and must be refreshed every 2 milliseconds. Signal 8ERFSH initiates a refresh cycle. During all read and write cycles RAM sends signal RAMEN to the data bus buffer.

4.5.10.i ROM Control. ROM control receives address bits ADR11-18 and control signal 8ERD, and generates signals ROMEN 1PSADR11, 2PSADR11, 5ROM10-17, and 5ROM20-27. ROM control has switches that select the starting and ending ROM address locations according to the number and capacity of ROM chips installed. Signals 5ROM10-17 and 5ROM20-27 select a ROM chip for readout. Signal 8ERFSH inhibits ROM control operation. ROM needs no refreshing, but a RAM refresh cycle takes precedence over all other memory operations.

4.5.10.j ROM. ROM consists of up to 16 optional EPROM chips. Each chip can have a capacity of 2K or 4K x 8-bit bytes, depending on the type of chip installed. During readout ROM receives an address byte on address lines ADR0-7, signals 8EMRQ, 8ERD, ROMEN, 1PSADR11, and 2PSADR11, and one of signals 5ROM10-17 or 20-27, which select a chip for readout. Signals 1PSADR11 and 2PSADR11 can be either +5 volts or address bit 11 depending on the ROM control switch settings. EPROM chips with a 2K-byte capacity require switch settings that select +5 volts, and 4K-byte chips require settings that select address bit 11. ROM responds by transmitting, on lines DAT0-7, the data stored in the addressed location.

4.5.10.k Address Decoder. This logic (figure 4-70) decodes address bytes received on lines ADR0-7 and generates eight control signals. Switch 5SW3 inhibits the logic when set to OFF. Switch 5SW4 selects the address range of the address bytes. Signal 8EIORQ enables the circuit. Signal 8EMRQ or 8EM1 inhibits the circuit. This means that the address decoder is inactive during any operation involving memory, and active during any other data transfer operation.

4.5.10.l Data Bus Buffer. The bidirectional data bus buffer (figure 4-71) supplies drive for devices served by the processor and expansion data buses. The data bus buffer inverts data received on expansion data bus lines DAT0-7, and transfers the inverted data to processor data bus lines 9BZDAT0-7 during memory readout, or when the serial I/O controller wants to send out data on the processor data bus. During a RAM write cycle, or when the serial I/O controller wants to receive data from the processor data bus, the data bus buffer inverts data received on processor data bus lines 9BZDAT0-7 and transfers the inverted data to expansion data bus lines DAT0-7. Signals BZIEI, BZIEO, EM1, 8EIORQ, 5ENSIO, EMRQ, ROMEN, RAMEN, and 8ERD control the direction of data transfer. Signals 5ENMACTC, 6ENMATH, 5ENPAPI1, and 5ENIEEE are not used.

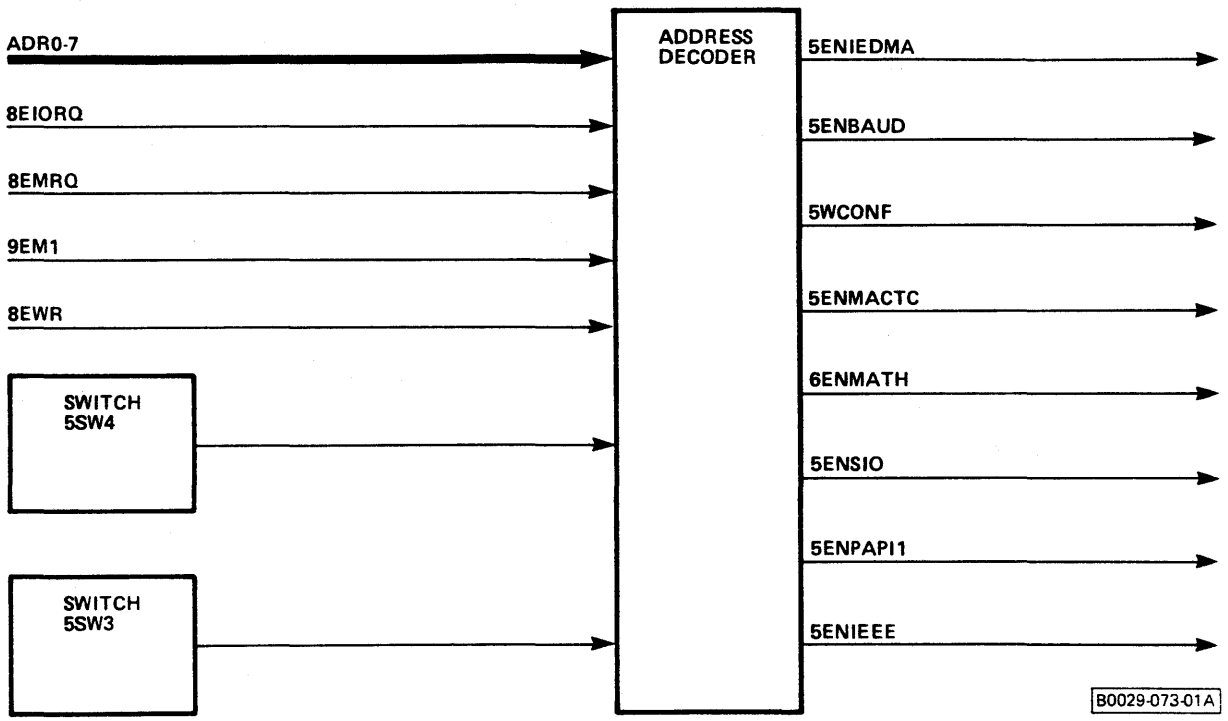

Figure 4-70. Address Decoder Logic

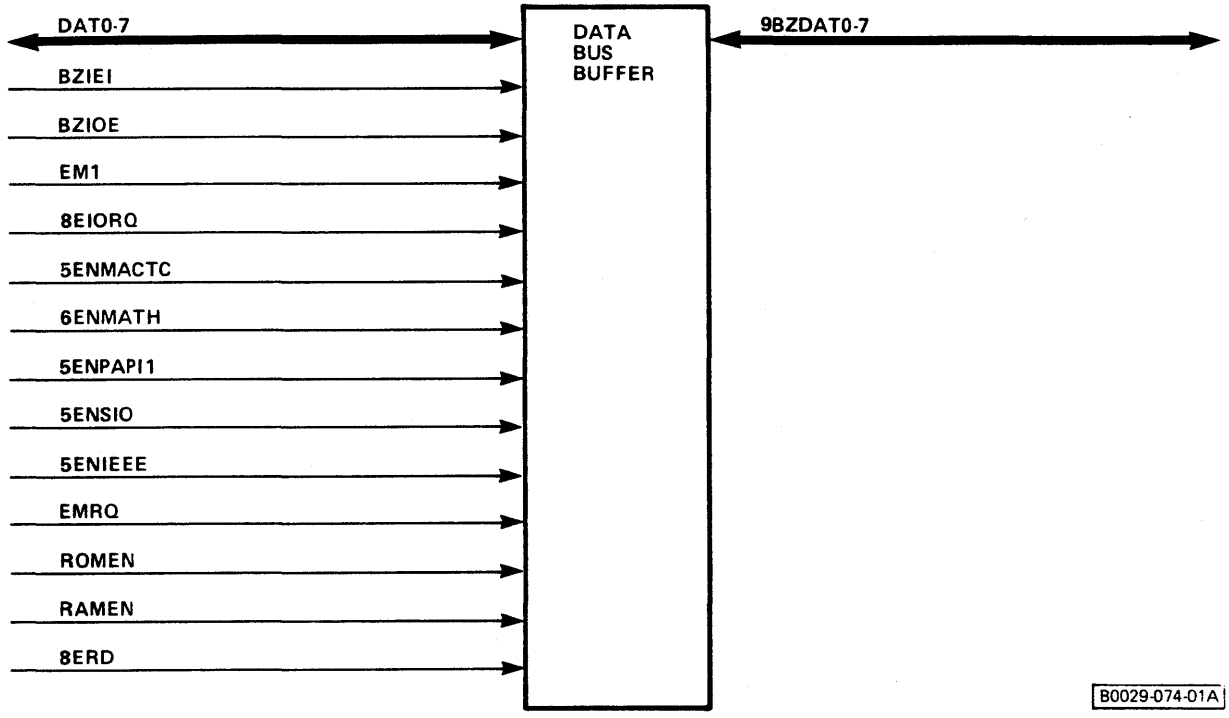

Figure 4-71. Data Bus Buffer Logic

4.5.10.m Clock Driver. The clock driver (figure 4-72) supplies the drive for processor-expansion-II-PCB logic that receives clock pulses 7FQ, CLKZ80, and 6CLKZ80. The clock driver receives six clock pulse inputs and generates five outputs. Signals 7EQ and 1CLKZ80 are not used.

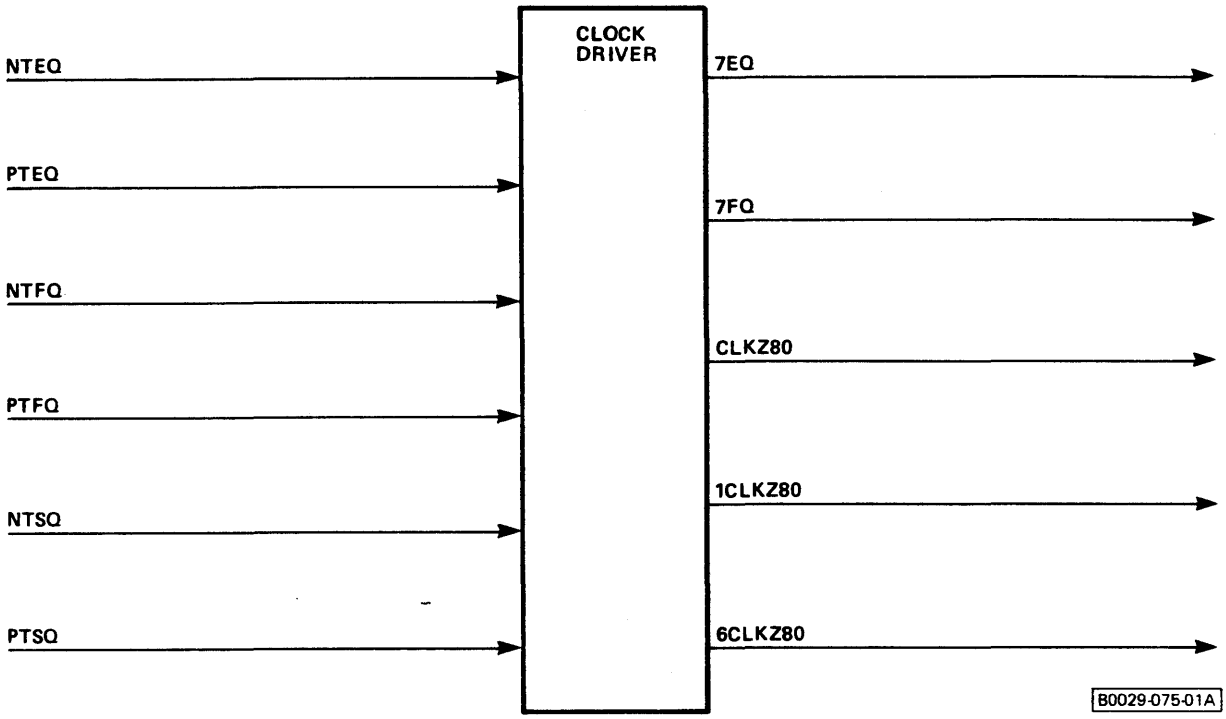

Figure 4-72. Clock Driver

4.5.10.n Daisy Chain Interrupt Logic. This logic (figure 4-73) allows the serial I/O controller to transmit interrupt requests when no device with higher priority is using the processor bus. When this condition exists, signal BZIEI is active, and the daisy chain interrupt logic sends signal XI to the serial I/O controller. This allows the controller to transmit interrupt requests. Signal XK from the controller is active when the controller is not using the processor bus. As long as BZIEI and XK remain active, the daisy chain interrupt logic sends out signal BZIEO on the processor bus. This allows any lower priority device to transmit interrupt requests. When the controller starts to use the bus, XK and BZIEO become inactive. When BZIEI becomes inactive, XI and BZIEO become inactive and the controller can no longer transmit interrupt requests. Inputs XB and XE are always active. Output XC is not used.

4.5.10.o Baud Rate Generator. The baud rate generator (figure 4-74) has a 2.46-MHz crystal oscillator, and uses the oscillator output to generate the selected baud rate. Data bits DAT0-3 and address bits ADR0 and ADR1 select the 1200-baud rate that the serial I/O controller uses to control serial transmit and receive rates. Signals 8EWR and 5ENBAUD enable the generator, which supplies 1200-baud clock pulses 5SIOCLK1 and 5SIOCLK2 to the serial I/O controller.

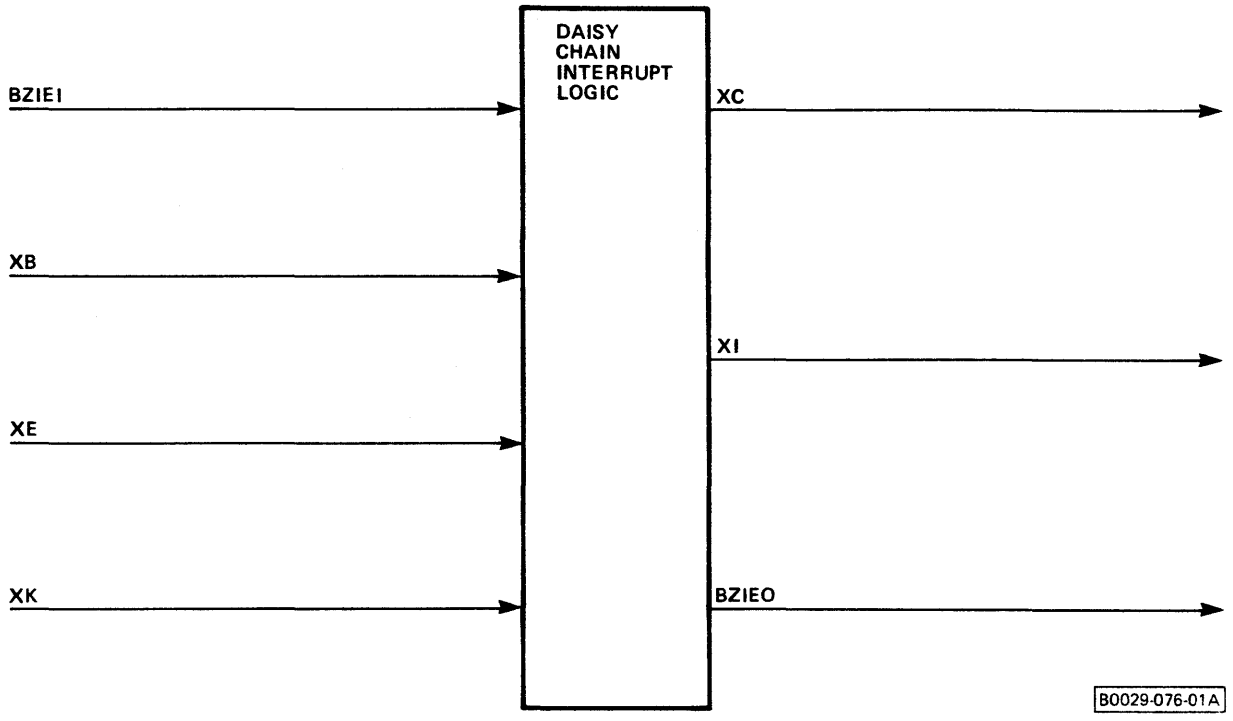

Figure 4-73. Daisy Chain Interrupt Logic

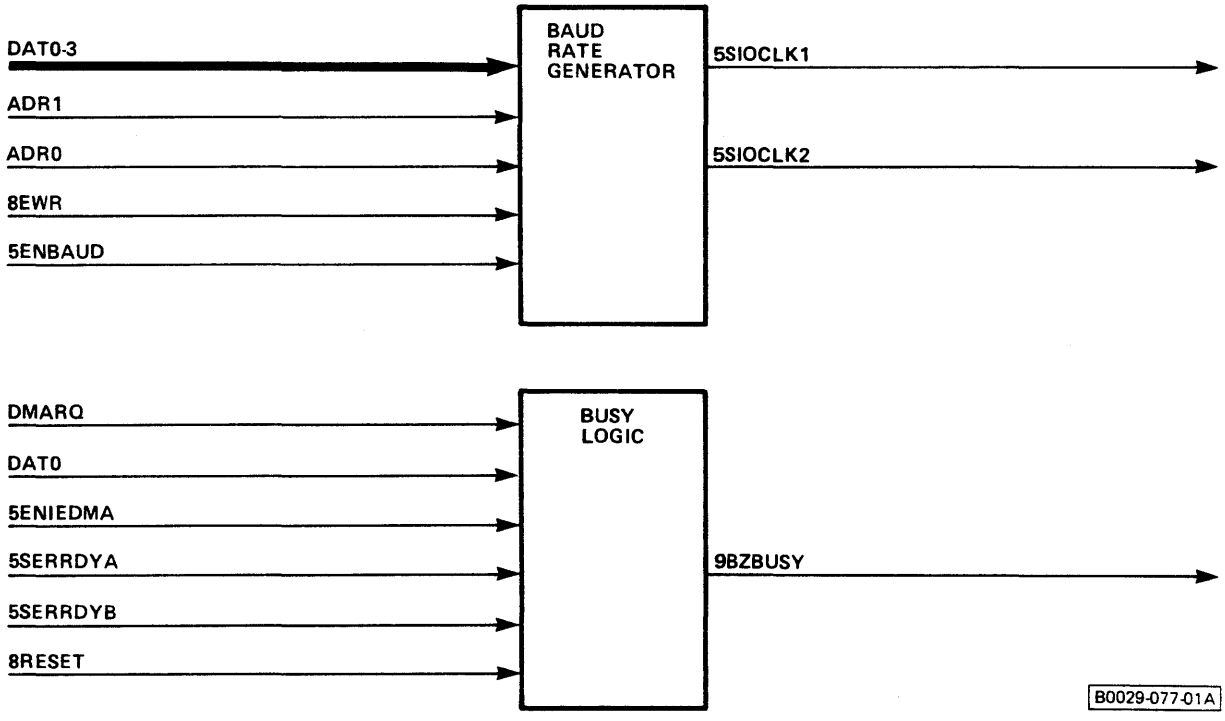

Figure 4-74. Baud Rate Generator and Busy Logic

4.5.10.p Busy Logic. This logic supplies the drive for the logics that receive signal 9BZBUSY. When the serial I/O controller is busy, either 5SERRDYA or 5SERRDYB becomes active and the busy logic sends out 9BZBUSY on the processor bus. Signals DMARQ, DAT0, 5ENIEDMA, and 8RESET are not used.

4.5.10.q Serial I/O Controller. The serial I/O controller (figure 4-75) transfers data between the expansion data bus and serial ports J3 and J4. Since the bus data is in parallel form, the controller must convert the parallel data to serial form for transmission to the ports, and convert the serial data from the ports to parallel form for transmission on the bus lines.

Signal 5ENSIO enables the controller. Address bit ADR0 becomes active when a control byte is on data bus lines DAT0-7, and becomes inactive when a data byte is on the bus lines. Address bit 1 becomes active to select port J3, and inactive to select J4.

When 8EIORQ becomes active, the controller converts data received on bus lines DAT0-7 to serial form. If ADR1 is active, the controller sends request-to-send signal SRQSND to J3. When the device connected to J3 is ready to accept data, SCLRSND becomes active, and the controller sends the serial data to J3 on line 5ATXDAT. If ADR1 is inactive, the controller sends RQSND to J4, and when CLRSND becomes active, the data goes to J4 on line 5TXDAT. When the device connected to J3 has data to send, signal SDCARDT becomes active, and when 5ENSIO and ADR1 also become active, the controller responds. When the bus is not in use, signal XV is active, and the controller sends interrupt-request signal 5INT to the CPU on the system processor PCB. Signal XK becomes inactive to inform other devices that the bus is in use. If the CPU is not busy, 8EIORQ, 8EM1, and 8ERD become active, and the controller sends SDTERRDY to J3 to inform the device that the controller is ready for data. The device then sends serial data on line SRECDAT. The controller converts the data to parallel form and transmits the data on lines DAT0-7.

When ADR1 becomes inactive and DCARDT becomes active, the controller sends 5INT to the CPU, receives 8EIORQ, 8EM1, and 8ERD, and sends DTERRDY to J4. The device connected to J4 then sends serial data on line RECDAT. The controller converts the data to parallel form and transmits the data on lines DAT0-7. Signal 5SERRDYA or 5SERRDYB becomes active when the controller is busy with J3 or J4, respectively. Baud clock pulses SIOCLK2 and SIOCLK1 control receive and transmit operations with J3 and J4, respectively. Clock pulse CLKZ80 controls other internal controller operations. Signal 8RESET resets the controller.

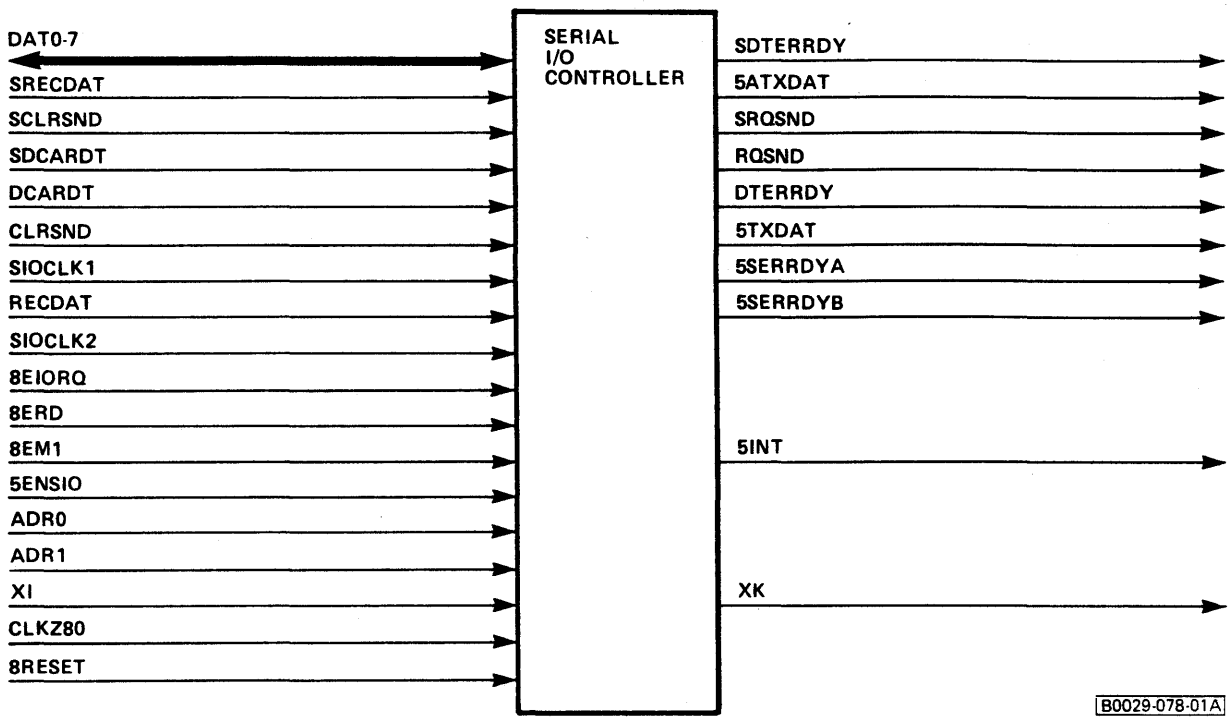

Figure 4-75. Serial I/O Controller

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4.5.11 Video 1 PCB

The video 1 PCB (figure FO4-29) has three functional elements:

- Input logic
- Control logic
- Video logic

The input logic mixes overlay and cursor inputs with refresh memory signals, and multiplexes data. The control logic generates a blink signal and buffers system clocks, cursors, and video timing signals. The video logic converts display data from digital to analog format for use with monochrome or color monitors.

4.5.11.a Input Logic. The input logic (figure 4-76) has two functional elements:

- Mixing logic
- Element select logic

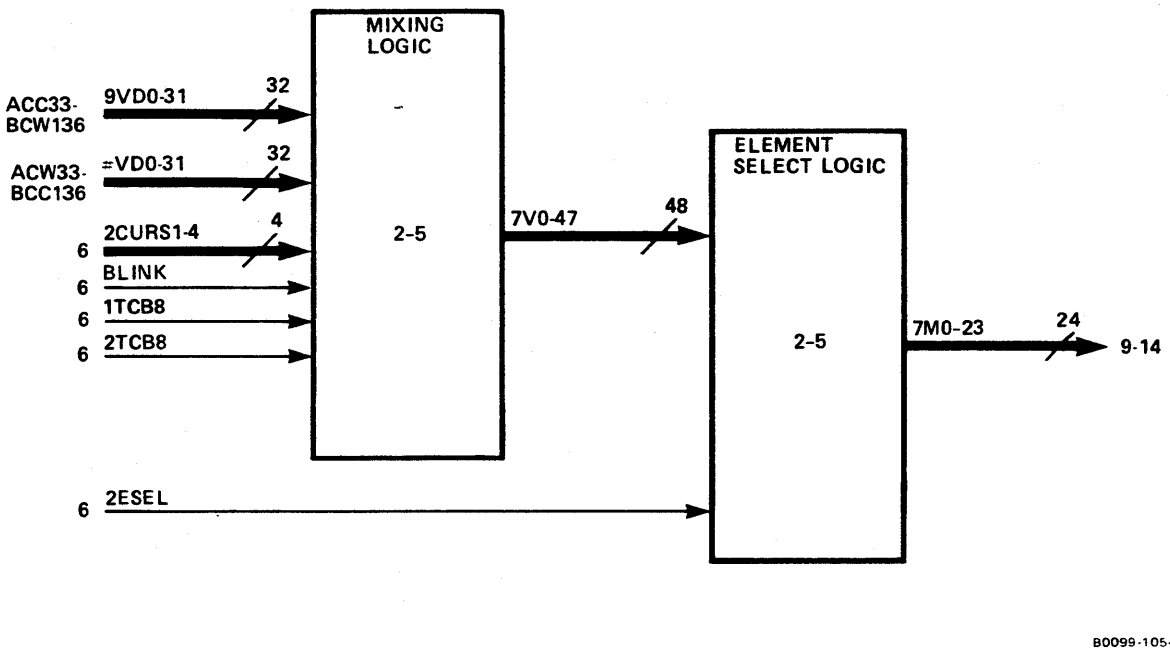


Figure 4-76. Input Logic

The mixing logic mixes cursor and overlay inputs with refresh memory signals. The element select logic multiplexes mixing logic output data, when required by system resolution.

4.5.11.a.1 Mixing logic. Receivers convert refresh memory signals 9VD0-31 and ≠VD0-31 from differential to single-ended format. A patch network combines selected refresh memory signals, cursor signals 2CURS1-4, and blink

signal BLINK. Composite blanking signals 1TCB8 and 2TCB8 select mixing PROMs to generate display signals 7V0-47.

4.5.11.a.2 Element select logic. The element select logic generates display signals 7M0-23. Select signal 2ESEL multiplexes display signals 7V0-47, as required by system resolution.

4.5.11.b Control Logic. The control logic (figure 4-77) has three functional elements:

- Multiplex logic
- Cursor logic
- Driver logic

The multiplex logic generates a signal to multiplex the display data, depending on system resolution. The cursor logic buffers and routes cursor inputs to the input logic and the video amplifiers. The driver logic buffers system clock and video timing signals.

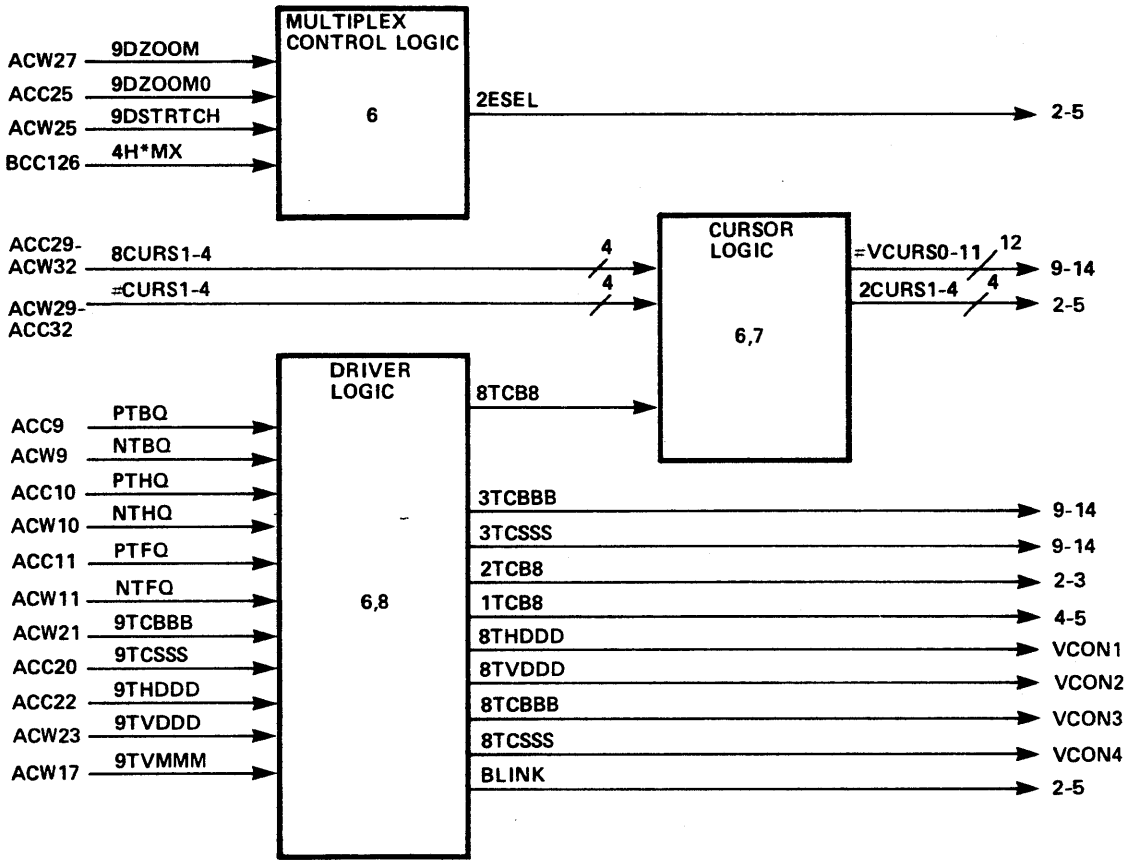
4.5.11.b.1 Multiplex logic. Zoom control signals 9DZOOM, 9DZOOM0, and 9DSTRTCH generate select signal 2ESEL. Resolution signal 4H*MX enables 2ESEL, as required by system resolution.

4.5.11.b.2 Cursor logic. The cursor logic converts differential cursor signals 8CURS1-4 and #CURS1-4 to single-ended signals 2CURS1-4. A patching network routes video cursor signals #VCURS0-11 to the video logic. Composite blanking signal 8TCB8 disables video cursor signals during blanking.

4.5.11.b.3 Driver logic. The driver logic converts differential clock signals PTBQ, NTBQ, PTHQ, NTHQ, PTFQ, and NTFQ to single-ended signals (not shown). Composite blanking and sync signals 9TCBBB and 9TCSSS generate output signals 8TCBBB and 8TCSSS. Horizontal and vertical drive signals 9THDDD and 9TVDDD generate output signals 8THDDD and 8TVDDD. Vertical memory timing pulse 9TVMMM generates blink signal BLINK.

4.5.11.c Video Logic. The video logic mixes cursor signals #VCURS0-11 with display signals 7M0-23. Twelve 2-bit DACs generate analog outputs VIDOUT0-11. Composite sync and blanking signals 3TCSSS and 3TCBBB control DAC operation.

4.5.11.d Process Description. The video 1 PCB converts refresh memory and cursor signals from digital to analog format. The input logic combines refresh memory signals 9VD0-31 and #VD0-31 with cursor signals 2CURS1-4 and blink signal BLINK. The video logic converts display signals 7M0-23 and video cursor signals #VCURS0-11 into analog signals VIDOUT0-11. The control logic buffers video signals 8THDDD, 8TVDDD, 8TCBBB, and 8TCSSS.



A0099-104-02A

Figure 4-77. Control Logic

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4.5.12 Video 7 PCB

The video 7 PCB (figure FO4-30) can process general image data or graphics data. A video 7A has three 4-bit DACs while the video 7B has three 8-bit DACs. This PCB operates in one of three modes: read, write, or refresh memory. Functional elements include:

- Interface and control logic
- Data output multiplexer
- Data input logic
- Timing and control
- Differential receivers
- Any-to-any patch
- Video lookup table (VLT)
- Overlay logic
- Sync, blanking, and control
- Three video channels (blue video channel is discussed)

4.5.12.a Interface and Control. Interface and control logic performs status read and write, address counter read and write, and VLT read and write upon command from the system processor PCB. This logic consists of an address decoder, a status logic, a fixed-state machine (FSM), and an edge detector.

The address decoder receives signals from system processor PCB address bus 4BADR0-7 and issues commands for either status or VLT operations, depending on the address values. Switches on the video 7 PCB select a pair of addresses for the VLT address and data operations. The even address selects VLT address counter read or write operations. The odd address selects VLT data read or write operations. Hexadecimal address 80 selects status operations on all video PCBs. Signal 9BSYSEN goes to the data out multiplexer during a VLT data read operation.

The status logic sends video 7 PCB status to the system processor PCB during status read and write operations. Signal 9PORCLR from the system processor PCB enables 9BBUSY to write video 7 PCB status to the system processor PCB when power is first applied to the 9465. The 9BSTAT line enables 9BBUSY during a status write operation and routes an internal busy signal to the data input logic during a status read operation. The status logic monitors the FSM and issues 9BWAIT when a VLT address counter write, VLT data read, or VLT data write operation is in progress.

The FSM controls the VLT address counter write, VLT data read, and VLT data write operations. Signal 5ADR routes the VLT address counter output onto data bus 9BDAT0-15 during an address read operation. The FSM performs address write, data read, and data write operations only during monitor screen blanking time. The 5VSTM signal from the sync, blanking, and control logic enables the FSM only during blanking time. The FSM responds to an address write command by enabling the VLT address counter with 4CS0 and 4CS1. A data write command sends 9CRMWRT to logic that enables VLT RAMs. Data read sends a 9LTCHEN signal to the data out multiplexer logic. Read command 9BREAD and write command 9BWRITE start the read and write operations when the video 7 PCB is addressed for either an address counter or a VLT data operation. Clock 7FQ clocks read and write commands out of the FSM.

The edge detector generates CDCLK when an address read or write, or a data read or write command is issued. The CDCLK signal goes to the data input logic. The edge detector also generates a signal to enable the FSM during a read or write operation. Clock signal 7FQ synchronizes edge detector output signals.

4.5.12.b Data Output Multiplexer. The data output multiplexer has a 24/12 data selector, a data/address multiplexer, an ECL-to-TTL converter, and a tri-state output buffer. The data output multiplexer routes VLT output data or the VLT address counter value onto the system data bus during a read operation.

The 24/12 data selector routes VLT output data to the data/address multiplexer. A jumper on the video 7B PCB selects 24-bit mode. The video 7A PCB operates in the 12-bit mode with no jumper installed.

The data/address multiplexer selects either VLT output data or the VLT address counter value. Signal 5ADR, from the interface and control logic, selects VLT output data during a read operation and the VLT address counter value during a write operation.

The output of the data/address multiplexer goes to the ECL-to-TTL converter. The ECL-to-TTL converter routes TTL signals to the tri-state output buffer. Under control of 9BSYSEN, the tri-state output buffer gates TTL signals onto display bus 9BDAT00-15 interface and control logic.

4.5.12.c Data Input. Data input logic includes:

- Input data register
- TTL-to-ECL converter
- Address counter
- 24/12 bit data selector

Data input logic stores VLT data from the system display processor, generates VLT address values, and formats VLT data to work with the video 7 PCB as configured. The input data register stores VLT write data on data bus 9BDAT0-15, when clocked by CDCLK from interface and control logic. A set of switches selects one bit from data bus 9BDAT0-15 for status read line 9BSTAT. This line sends a signal to interface and control logic during a status write operation and routes a signal onto data bus 9BDAT0-15 during a status read operation. The TTL-to-ECL converter translates VLT write data and interface and control signals from TTL to ECL levels.

An address counter generates address values used during VLT data read and write operations. The system processor PCB programs the address counter for a specific starting address during an address counter write operation. The address counter continues to count up when data is being written to successive addresses. Timing and control logic signals 4CS0 and 4CS1 enable the address counter. Address counter output signals 1ADRCTR0-11 go to the data out multiplexer. A 24/12 bit selection patch routes ADRCTR0-11 to the any-to-any patch. The AJ signal goes to the timing and control logic and the data output multiplexer only when 24-bit operation is selected.

The 24/12 bit data selector divides the input data into two 13-bit words or one 25-bit word, depending how the 24/12 signal from the data output multiplexer is wired.

4.5.12.d Timing and Control. The timing and control logic includes:

- ¤ System clock buffers
- ¤ Cursor buffers
- ¤ Link generator
- ¤ Write enable logic
- ¤ Chip select logic

Timing and control logic buffers input signals and generates a blink signal, write enable signals, and chip select signals. Three system clocks, TBQ, THQ, and TFQ, enter the video 7 PCB from the backplane assembly as differential pairs. The timing and control logic buffers these clocks and provides 11 clocks (8BQE, 7BQE, 7BQ, 9HQE, 8HQE, 7HQE, #HQE, 7FQ, 4FQE, and 3FQE) to the rest of the video 7 PCB and the PIXEL CLOCK signal to the RGB monitor. Cursor buffers accept four differential cursor input signals (8CURS1-4) from the 9465 backplane assembly and route them to the any-to-any patch as 5CURS0-3. Vertical drive signal, 8TVDDD, from the sync, blanking, and control logic, clocks the blink generator, a divide-by-64 logic, for a 1-Hz BLINK signal. The timing and control logic accepts VLT address signals 1ADR010, 1ADR011, and 1ADR110, from the any-to-any patch and generates chip select signals (CS0E, CS1E, CS00, and CS10) for the VLT RAMs. Signals 9CRMWRT and AJ from the interface and control logic and 1AD010 or 1AD011 from the any-to-any patch are logically manipulated to generate write enable signals WR0, WR1, WB0, and WB1, used by the VLT RAMs during the write mode. Jumpers determine whether the write enable signals operate at 12 or 24 bits.

4.5.12.e Differential Receivers. Thirty-two differential receivers buffer up to 32 input signals (VD0-VD31) from refresh memory and route the signals to the any-to-any patch. Each differential receiver has a single-sided output buffer.

4.5.12.f Any-To-Any Patch. The any-to-any patch has jumper selection points, a VLT address select logic, and reclock/buffer latches. The any-to-any patch allows the video 7 PCB to use 12 or 24 bits of refresh memory data, up to four cursor inputs, and the blink generator output from the timing and control logic, all selectable by jumpers. Jumpers on the any-to-any-patch determine VLT partitioning. The EVEN12-18 and ODD12-18 signals route overlay, cursor, and blink data to the overlay logic.

The VLT address select logic routes refresh memory data to the VLT address inputs except during screen blanking. The 9BLANK D signal from the sync, blanking, and control logic selects the VLT address counter output from the interface and control logic to address the VLT during a read or write operation. These operations occur only during vertical or horizontal blanking. The VLT address select logic splits the VLT address data stream into even and odd data streams with slower bit rates. The slower bit rate allows sufficient time for the VLT RAMs to output valid data to the following stage.

The reclock/buffer latches use clock #HQE to synchronize address data. Even address data goes to the even VLT RAMs on lAD00-9. Odd address data goes to the odd VLT RAMs on lines lAD10-9. The remaining address lines, lAD010, lAD011, and lAD110, go to the timing and control logic and the sync, blanking, and control logic.

4.5.12.g Video Lookup Table. The video lookup table (VLT) has fifty-two 1024 X 1 RAMs organized into two display data tables and two overlay data tables. Users can organize the VLT for 13-bit high resolution, 13-bit low resolution, 25-bit high resolution, or 25-bit low resolution operation.

The two display data tables accept PDATIN0-3 and MEMIN4-23 from the data input logic. Signals lAD00-9 from the any-to-any patch address the even display data table. Signals lAD10-9 address the odd display data table. The WB0 and WB1 signals enable the RAM data inputs during a VLT data write operation. Signals CS0E, CS1E, CS00, and CS10 enable the RAM data outputs during a VLT data read operation. The even display data table sends BE0-7, GE0-7, and RE0-7 to the blue, green, and red video channels, respectively. The odd display data table sends B00-7, G00-7, and R00-7 signals to the blue, green, and red video channels, respectively.

The two overlay data tables accept the MEMIN24 signal from the data input logic. Signals lAD00-9 from the any-to-any patch address the even overlay data table. The lAD10-9 signals address the odd overlay data table. The WR0 and WR1 signals from the timing and control logic enable the overlay table RAM data inputs during a VLT data write operation. The CS0E, CS1E, CS00, and CS10 signals from the timing and control logic enable the overlay table RAM outputs during a VLT data read operation. The even overlay data table sends the OV00 and OV01 signals to the overlay logic. The odd overlay data table sends the OV10 and OV11 signals to the overlay logic logic.

4.5.12.h Overlay Logic. Overlay logic includes reclock latches, overlay PROMs, and an interleave multiplexer. The overlay logic outputs three +10% brightness signals (9B+10, 9G+10, 9R+10), overlay signals for the video channels, and a VLT output signal for the data output multiplexer.

Reclock latches synchronize the EVEN12-18 and ODD12-18 signals from the any-to-any patch using the 8BQE and 7HQE clock signals from the timing and control logic. The EVEN12-18 and ODD12-18 signals contain overlay, cursor, and blink data.

Overlay PROMs provide intensity values for the overlay and cursor data. The 9BLANKE signal enables the overlay PROMs only when the monitor screen is not blanked.

The interleave multiplexer combines the even and odd data streams with the OV00, OV01, OV10, and OV11 signals from the video lookup table. Signal INTERLEAVE controls the interleave multiplexer. The interleave multiplexer recombines the OV00, OV01, OV10, and OV11 signals into the MEMOUT24 signal.

4.5.12.i Sync, Blanking, and Control Logic. The sync, blanking, and control logic has buffers, reclock latches, interleave logic, and RS-170 video drivers. The sync, blanking, and control generates an interleave signal for

combining even and odd data streams, routes blanking signals throughout the video 7 PCB, and converts the video drive signals to RS-170 levels. The buffer logic receives the screen size definition signals (9DZOOM, 9DSTRTCH, and 9DZOOM0) and the composite blanking signal (9TCBBB). Reclock latches synchronize the incoming signals to the local clocks and route (9TCBBB) to the rest of the video 7 PCB as 9BLANKD, 9BLANKE, 9BLANKG, and 5VSTM.

The interleave logic has a multiplexer and a data selector. The multiplexer selects either the 1AD010 or 1AD011 address signal from the any-to-any patch and either the 9DZOOM or the #HQE signal. The data selector selects either the address signal or the 9DZOOM and clock signal, depending on whether the hi-res jumper is installed. The output of the data selector becomes the INTERLEAVE signal and goes to the overlay logic and the three video channels. The RS-170 video drivers convert the composite blanking signal (9TCBBB), the composite sync (TCSSS), the vertical drive (9TVDDD), and the horizontal drive (9THDDD) from TTL levels to standard video levels.

4.5.12.j Blue Video Channel. This description of the blue video channel applies equally to the green video channel and the red video channel. The blue video channel has reclock latches, an interleave multiplexer, an overlay multiplexer, and a 4-bit (video 7A) or 8-bit (video 7B) digital-to-analog converter (DAC). The blue video channel converts the outputs of the VLT and the overlay PROMs from digital format into an analog signal which drives a color video monitor.

The reclock latches synchronize the VLT output data (BE0-7 and BO0-7). For video 7AS, a patch jumpers bits 0-3 to inputs 4-7. The interleave multiplexer combines the eight even bits with the eight odd bits, using INTERLEAVE. The output of the interleave multiplexer goes to the data out multiplexer as MEMOUT0-7. The overlay multiplexer combines the output of the interleave multiplexer with the overlay and cursor data from the overlay logic. The DAC converts the 8-bit video signal into an analog signal. The 9B+10 signal boosts the cursor brightness 10%. The 9DACSYNC and 9BLANKG signals synchronize the DAC output to the composite sync and blank signals during vertical and horizontal blanking.

4.5.12.k Processes. The video 7 PCB can drive one red-green-blue (RGB) color monitor. Jumpers on the PCB determine the number of bits per primary color and display resolution. The video 7 PCB mixes up to four cursors and two overlays with the video outputs.

Overall signal flow is as follows: the system processor PCB addresses the video 7 PCB on inputs 4BADR0-7 and initiates a read or write operation on 9BREAD or 9BWRITE respectively. Read and write data enter and leave on data bus 9BDAT0-15. Timing and control logic buffers system clocks and cursor inputs, and generates the blink signal. Differential receivers buffer input data from refresh memory and route the data to the any-to-any patch. Solder terminal jumper points on the any-to-any patch allow the user to configure the PCB in different ways. The video lookup table (VLT) stores values loaded from the system processor PCB during a read operation and sends intensity values to the DACs when addressed by data from refresh memory. The overlay logic routes overlay and cursor signals to the video channels. Sync, blanking, and control logic outputs COMP SYNC, COMP BLANK, HOR DRIVE, and VERT DRIVE in RS-170

format for the video monitor, and generates sync (9DACSYNC), blank (9BLANKE, 9BLANKG, 9BLANKD) and INTERLEAVE signals for the overlay logic and video channels. Each of the three video channels mixes intensity data from the VLT with cursor and overlay data from the overlay logic. The DACs then convert digital data to analog format for the color monitor. The data out multiplexer sends data from the VLT back to the system processor for verification during a read cycle.

4.5.13 Video 8 PCB

The video 8 PCB has two channels with blue, green, red, and hardcopy video outputs for each channel. Each channel contains a video lookup table (VLT) divided into even and odd halves. Intensity values stored in the VLTs may be changed by the operator. Video data from memory PCBs addresses the VLTs. Two-bit digital-to-analog converters change the VLT outputs into video signals to drive two color monitors and two hardcopy devices.

The video 8 PCB (figure FO4-31) has four functional elements:

- Input logic
- Buffer logic
- Graphics logic
- Video logic

The input logic routes data between the display bus and the graphics logic, and controls VLT read and write operations. The buffer logic buffers refresh memory, cursor, zoom, system clock, and sync signals. The graphics logic generates intensity values for refresh memory data using a VLT. The video logic converts digital VLT outputs to analog video outputs.

4.5.13.a Input Logic. Display bus 9BDAT00-15 routes data to and from the graphics logic VLTs. Address signals 4BADR0-7, read signal 9BREAD, and write signal 9BWRT control VLT read and write operations. Handshake signal 9BWAIT and status signal BREADY control the display bus during VLT read and write operations. Power-on reset clear signal 9PORCLR resets the input logic.

Data signals 1ESBD0-10 route starting addresses to the graphics logic address counters and write data to the graphics logic VLTs. Control signals DP1CS1E, DP1CS2E, DP2CS1E, and DP2CS2E control the address counters. Write control signals 6DP1RWR0, 6DP1RWRE, 6DP2RWR0, and 6DP2RWRE control VLT read and write operations. Resolution signal HIRES controls the write control signals as required by system resolution.

Output latch signals 5DP1LTCH and 5DP2LTCH control VLT output signals DP1OD0-7 and DP2OD0-7. The control logic multiplexes DP1OD0-7 and DP2OD0-7 with address counter signals DP1CT0-10 and DP2CT0-10 during read operations. Visible time signal 5VSTM synchronizes the control logic with system blanking.

4.5.13.b Buffer Logic. The buffer logic (figure 4-78) has three functional elements:

- Receiver logic
- Sync logic
- Zoom logic

The receiver logic converts differential refresh memory and cursor signals to single-ended signals. The sync logic generates video, clock, and blink signals. The zoom logic generates multiplex and resolution signals.

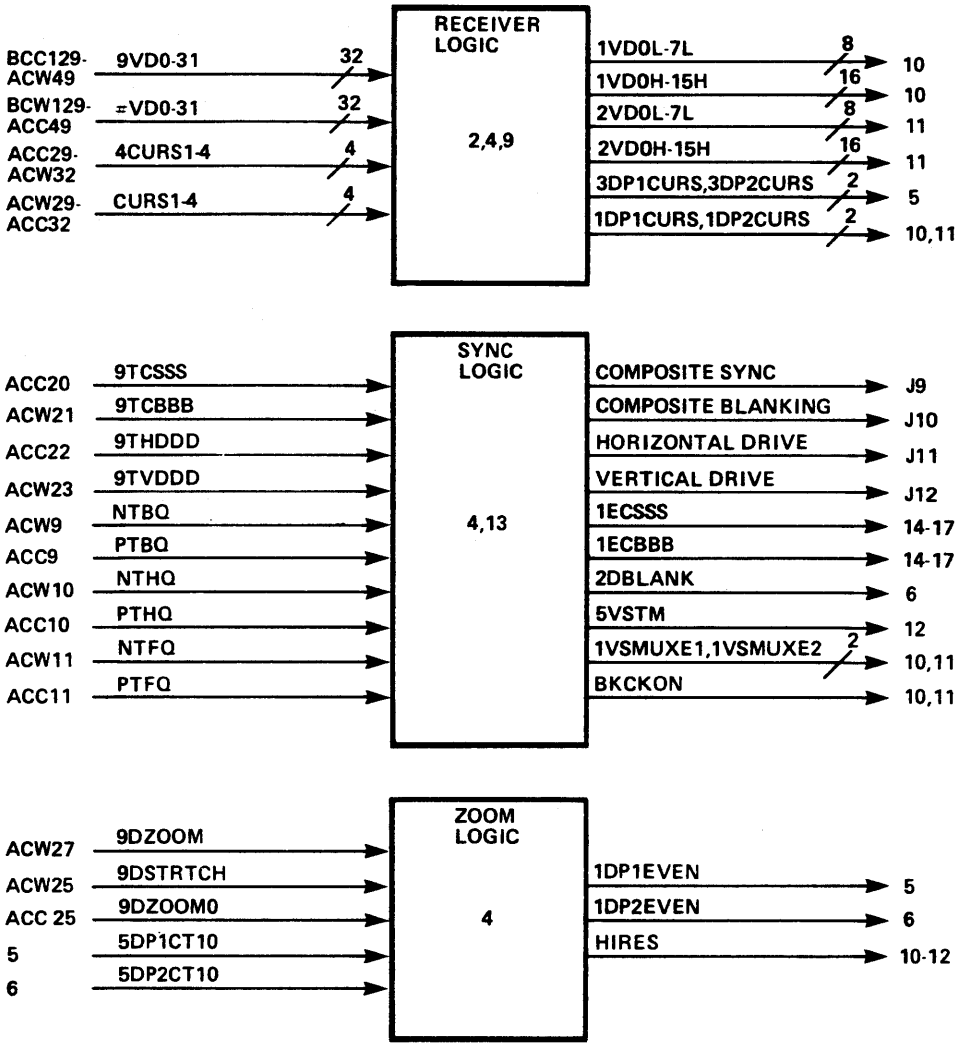

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Figure 4-78. Buffer Logic

4.5.13.b.1 Receiver logic. Refresh memory signals 9VD0-31 and #VD0-31 generate video data signals that address the graphics logic VLTs. A patching network selects low-resolution signals 1VD0L-7L and 2VD0L-7L, or high-resolution signals 1VD0H-15H and 2VD0H-15H, depending on system resolution. Cursor signals 4CURS1-4 and CURS1-4 generate cursor signals that address the VLTs and cursor intensity signals that modify the video outputs. A patching network selects two of the four cursor inputs as cursor signals 1DP1CURS and 1DP2CURS. Cursor signals 1DP1CURS and 1DP2CURS generate cursor intensity signals 3DP1CURS and 3DP2CURS.

4.5.13.b.2 Sync logic. Composite sync signal 9TCSSS generates output signal COMPOSITE SYNC and composite sync signal 1ECSSS. Composite blanking signal 9TCBBB generates output signal COMPOSITE BLANKING, blanking signals 1ECBBB and 2DBLANK, VLT address multiplex signals 1VSMUXE1 and 1VSMUXE2, and visible time signal 5VSTM. Horizontal drive signal 9THDDD and vertical drive signal 9TVDDD generate output signals HORIZONTAL DRIVE and VERTICAL DRIVE, respectively.

System clock signals NTBQ, PTBQ, NTHQ, PTHQ, NTFQ, and PTFQ generate video 8 internal clock signals (not shown). A blink oscillator generates blink signal BKCKON.

4.5.13.b.3 Zoom logic. Zoom signal 9DZOOM and buffered address counter signals 5DP1CT10 and 5DP2CT10 generate VLT output multiplex signals 1DP1EVEN and 1DP2EVEN. Zoom control signals 9DSTRTCH and 9DZOOM0 select the VLT output multiplex signals. Switch-selected resolution signal HIRES configures the video 8 to match system resolution.

4.5.13.c Graphics Logic. The graphics logic has two identical sections, display section 1 and display section 2. The following description of display section 1 applies to both display sections.

Display section 1 (figure 4-79) has four functional elements:

- Address logic
- Input multiplex logic
- Video lookup table (VLT)
- Output multiplex logic

The address logic generates address values for reading from or writing to the VLT. The input multiplex logic selects refresh memory signals or address logic signals to address the VLT. The VLT stores pixel intensity values used to create graphics displays. The output multiplex logic converts the VLT output signals into readback, hardcopy, color, and intensity signals.

4.5.13.c.1 Address logic. Control signals DP1CS1E and DP1CS2E load the starting address from data signals 1ESBD0-10 into the address logic. The address logic generates address signals DP1CT1-10.

4.5.13.c.2 Input multiplex logic. Address multiplex signal 1VSMUXE1 routes address signals to the VLT. Address signals DP1CT1-10 address the VLT during read and write operations. Memory refresh signals 1VD0L-7L or 1VD0H-15H, cursor signal 1DP1CURS, and blink signal BKCKON address the VLT during graphics conversion operations. Address signals 2DP1RA0E-7E address the even section

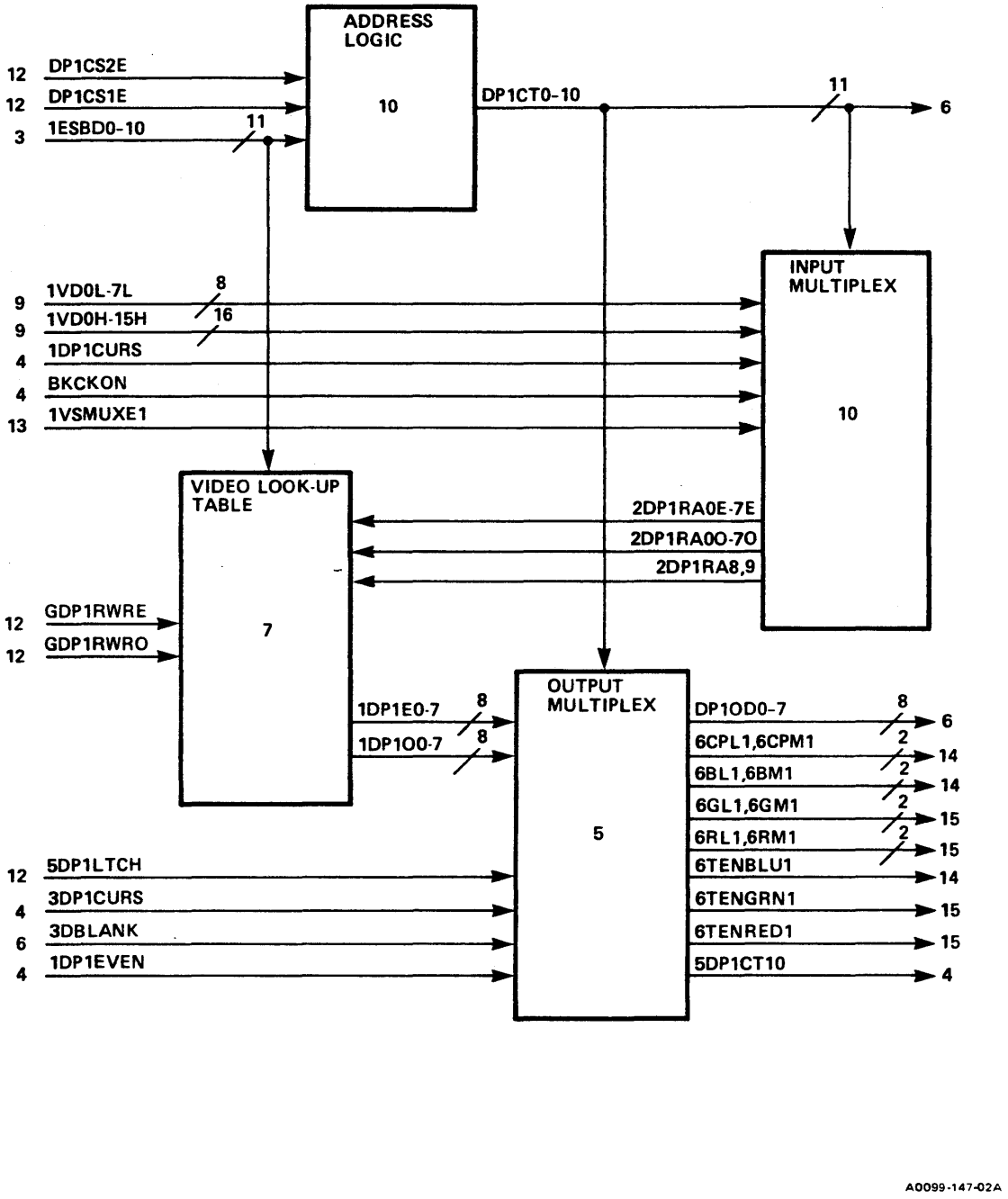

Figure 4-79. Graphics Logic

of the VLT. Address signals 2DP1RA00-70 address the odd section of the VLT. Address signals 2DP1RA8 and 2DP1RA9 address both sections.

4.5.13.c.3 Video lookup table. Read/write signals 6DP1RWRE and 6DP1RWRO write data from signals 1ESBD0-10 into the VLT during write operations. The read/write signals read output signals 1DP1E0-7 and 1DP100-7 from the VLT during read operations. Address signals 2DP1RA0E-7E, 2DP1RA00-70, 2DP1RA8, and 2DP1RA9 address VLT locations.

4.5.13.c.4 Output multiplex logic. Latch signal 5DP1LTCH loads VLT output signals 1DP1E0-7 and 1DP100-7 into the output multiplex logic. Address signal DP1CT10 multiplexes the VLT output signals to generate readback data signals DP10D0-7. Address signal DP1CT10 also generates buffered address signal 5DP1CT10. Blanking signal 3DBLANK and interleave signal 1DP1EVEN generate hardcopy signals 6CPL1 and 6CPM1, blue signals 6BL1 and 6BM1, green signals 6GL1 and 6GM1, and red signals 6RL1 and 6RM1. Cursor intensity signal 3DP1CURS generates intensity signals 6TENBLU1, 6TENGRN1, and 6TENRED1.

4.5.13.d Video Logic. The video logic has two identical sections, each made up of four 2-bit DACs. The following description of section 1 applies to both sections.

Hardcopy intensity signals 6CPL1 and 6CPM1 generate hardcopy output signal VIDCPY1. Blue intensity signals 6BL1 and 6BM1, and blue cursor intensity signal 6TENBLU1 generate blue video output signal VIDBLU1. Green intensity signals 6GL1 and 6GM1, and green cursor intensity signal 6TENGRN1 generate green video output signal VIDGRN1. Red intensity signals 6RL1 and 6RM1, and red cursor intensity signal 6TENRED1 generate red video output signal VIDRED1. Composite sync signal 1ECSSS and composite blanking signal 1ECBBB mix with all four output signals.

4.5.13.e Process Description. The video 8 PCB performs the following operations:

- VLT read
- VLT write
- Graphics conversion

Video lookup table read operations route data from the graphics logic VLTs to display bus 9BDAT00-15. Video lookup table write operations route data from display bus 9BDAT00-15 into the graphics logic VLTs. Graphics conversion operations convert digital refresh memory data from the memory PCB to analog video signals.

4.5.13.e.1 Video lookup table read. The following description of a VLT read operation discusses display section 1 but applies to both display sections.

The system processor starts a VLT read operation by driving 9BREAD active. Address signals 4BADR0-7 select either display section 1 or display section 2 of the graphics logic. Control signals DP1CS1E and DP1CS2E load a starting address from display bus 9BDAT00-15 into the address counter via data signals 1ESBD0-10. Multiplex signal 1VSMUXE1 routes the address counter output to the VLT during blanking time. Read/write control signals 6DP1RWRE and 6DP1RWRO

route VLT output data DP1ODO-7 to the input logic readback multiplex. The input logic readback multiplexer routes DP1ODO-7 or address counter outputs DP1CTO-10 to display bus 9BDATOO-15.

4.5.13.e.2 Video lookup table write. The following description of a VLT write operation discusses display section 1 but applies to both display sections.

The system processor starts a VLT write operation by driving 9BWRT active. Address signals 4BADRO-7 select either display section 1 or display section 2 of the graphics logic. Control signals DP1CS1E and DP1CS2E load a starting address from display bus 9BDATOO-15 into the address counter via data signals 1ESBDO-10. Multiplex signal 1VSMUXE1 routes the address counter output to the VLT during blanking time. Read/write control signals 6DP1RWRE and 6DP1RWRO route data from display bus 9BDATOO-15 to the VLT via data signals 1ESBDO-7.

4.5.13.e.3 Graphics conversion. The following description of a VLT write operation discusses display section 1 but applies to both display sections.

A patching network selects graphics inputs from refresh memory signals 9VDO-31 and #VDO-31. Low-resolution graphics signals 1VDOL-7L or high-resolution graphics signals 1VDOH-15H address the VLT. A second patching network selects cursor inputs from cursor signals 4CURS1-4 and CURS1-4. Cursor signal 1DP1CURS and blink signal BKCKON address the VLT with the graphics signals. The VLT outputs from the VLT locations addressed drive the video logic. Video logic output VIDCPY1 drives an external hardcopy device. Video logic outputs VIDBLU1, VIDGRN1, and VIDRED1 drive a color monitor.

4.5.14 Video Load PCB

The video load PCB (figure 4-80) has thirty 15-ohm 30-watt resistors across the -5 V source and ground. This PCB is only installed in 9465 configurations that have a single video 1 PCB installed. The added load is required in this configuration to hold power supply regulation within specifications.

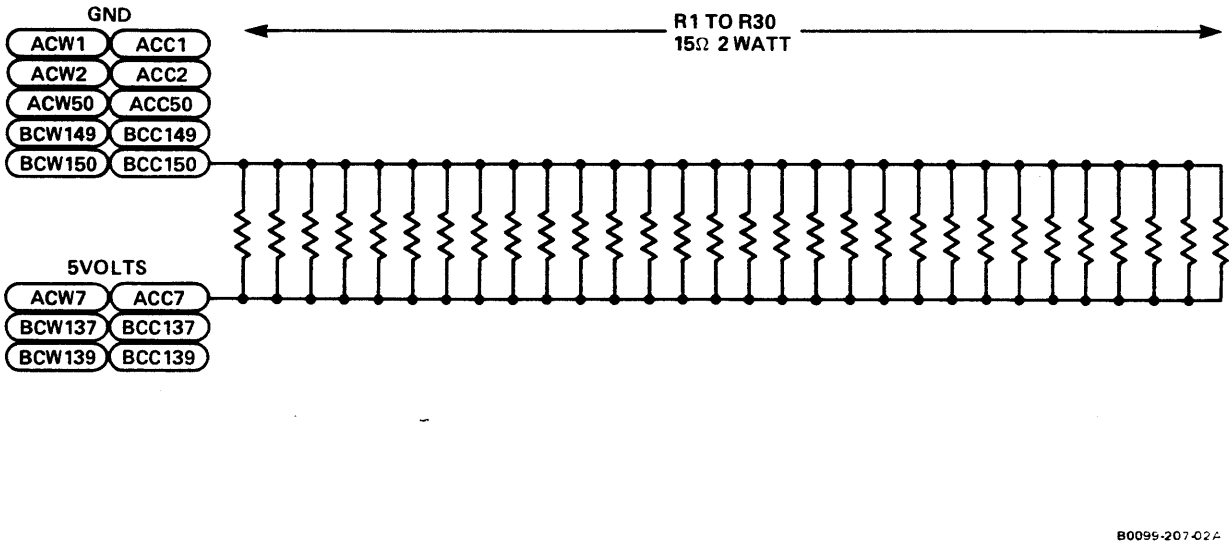

Figure 4-80. Video Load PCB Schematic Diagram

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4.5.15 Pixel Formatter PCB

The pixel formatter PCB receives image data in a multiple-pixel-per-word format and converts the data to a single-pixel-per-word format. A host computer combines groups of pixels 2 to 5 bits long into 16-bit words to speed data transfer. A single 16-bit word can contain three 5-bit pixels, four 4-bit pixels, five 3-bit pixels, or eight 2-bit pixels. The pixel formatter puts each pixel into a separate 16-bit word.

The pixel formatter PCB (figure 4-81) has four functional elements:

- Control logic
- Input logic
- Control store logic
- Output logic

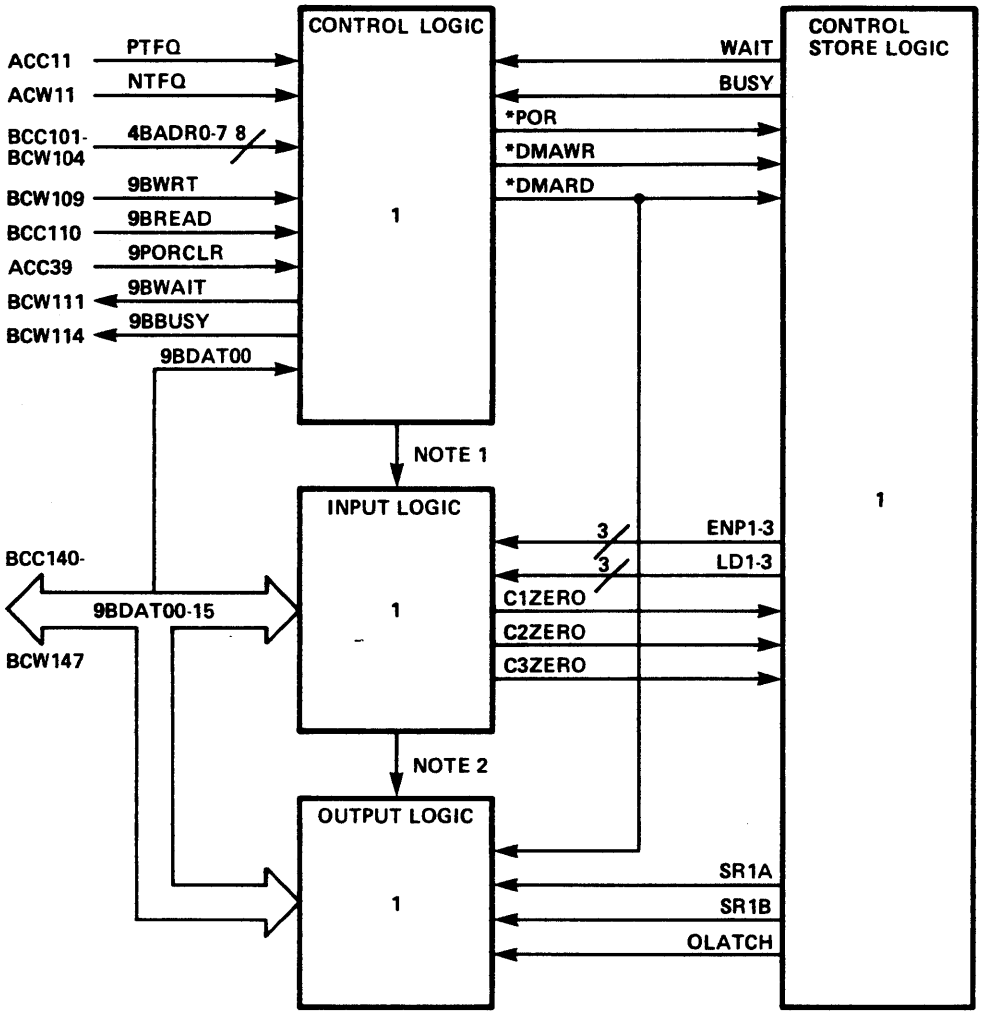
The control logic decodes address signals, routes read and write signals, and sends handshake and status signals to the control bus. The input logic latches command values from the display bus and generates control signals. The control store logic controls pixel formatter PCB operation using a PROM-based routine. The output logic shifts image data transferred from the display bus and transfers shifted data back to the display bus.

4.5.15.a Control Logic. Address signals 4BADR0-7 combine with read signal 9BREAD and write signal 9BWRT to generate control signals. Read signal 9BREAD generates direct memory access (DMA) signal *DMARD and, with wait signal WAIT, handshake signal 9BWAIT. Write signal 9BWRT generates input latch signal ILATCH and DMA write signal *DMAWR. Display bus signal 9BDAT00 and busy signal BUSY generate status signal 9BBUSY. Power-on reset clear signal 9PORCLR clears busy signal 9BBUSY and generates power on clear signal *POC. Clock signals PTFQ and NTFQ generate internal timing signal 7FQ (not shown).

4.5.15.b Input Logic. Display bus signals 9BDAT00-11 transfer command values to input logic latches. Display bus signal 9BDAT12 generates direction signal DIR. Input logic counters generate status signals *C1ZERO, *C2ZERO, and *C3ZERO. Enable signals *ENP1-3 and load signals *LD1-3 control input logic counters.

4.5.15.c Control Store Logic. Power-on clear signal *POC clears control store logic latches. Direct memory access read and write signals *DMARD and *DMAWR, and counter status signals *C1ZERO, *C2ZERO, and *C3ZERO generate control signals. Shift register control signals SR1A and SR1B load or inhibit output logic shift registers. Enable signals *ENP1-3 and load signals *LD1-3 control input logic counters. Wait signal WAIT and busy signal BUSY control handshake and status signals 9BWAIT and 9BBUSY, respectively. Output latch signal OLATCH loads output logic latches with shifted image data.

4.5.15.d Output Logic. Display bus signals 9BDAT00-15 transfer image data to output logic shift registers. Shift register control signals SR1A and SR1B, and shift direction signal DIR control shift register loading and operation. Output latch signal OLATCH loads shift register outputs into output logic latches. Direct memory access read signal *DMARD transfers shifted image data to the display bus.



NOTES: 1. ILATCH
2. DIR

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Figure 4-81. Pixel Formatter PCB

4.5.15.e Process Description. The pixel formatter PCB performs the following operations:

- Command write
- DMA write
- Data shift
- DMA read

A command write operation loads command values into input logic latches. A DMA write operation loads command values into input logic counters and image data into output logic shift registers. A data shift operation shifts image data loaded into output logic shift registers during a DMA write operation. A DMA read operation transfers shifted image data from the output logic to the display bus.

4.5.15.e.1 Command write. The system processor PCB starts a command write operation by selecting the pixel formatter PCB with address signals 4BADR0-7. Write signal 9BWRT combines with the decoded address to generate input latch signal ILATCH. The ILATCH signal transfers command values from display bus 9BDAT00-12 into input logic latches. Command values specify pixel length, pixel count, initial shift, and shift direction.

4.5.15.e.2 Direct memory access write. The system processor PCB starts a DMA write operation by selecting the pixel formatter PCB with address signals 4BADR0-7. Write signal 9BWRT combines with the decoded address to generate DMA write signal *DMAWR. The *DMAWR signal generates load signals *LD1-3, busy signal BUSY, and shift register control signals SR1A and SR1B. Load signals *LD1-3 load command values into input logic counters. The BUSY signal combines with the decoded address and 9BWRT to generate status signal 9BBUSY. The SR1A and SR1B signals load image data from display bus 9BDAT00-15 into the output logic shift registers.

4.5.15.e.3 Data shift. The control store logic starts a data shift operation after a DMA write operation. Enable signals *ENP1-3 and control signals SR1A and SR1B enable the input logic counters and output logic shift registers, respectively. The control store logic monitors counter status signals *C1ZERO, *C2ZERO, and *C3ZERO during data shift operations. The output logic shift registers shift image data left or right under the control of shift direction signal DIR. The DIR signal shifts data right when active and left when inactive.

4.5.15.e.4 Direct memory access read. The system processor PCB starts a DMA read operation by selecting the pixel formatter PCB with address signals 4BADR0-7. Read signal 9BREAD combines with the decoded address to generate DMA read signal *DMARD. The *DMARD signal generates wait signal WAIT and enables the output logic latches. The WAIT signal combines with the decoded address and 9BREAD to generate handshake signal 9BWAIT. The control store logic monitors counter status signals *C1ZERO, *C2ZERO, and *C3ZERO when generating output latch signal OLATCH. The OLATCH signal loads shifted image data from the output logic shift registers into the output logic latches.

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4.5.16 Transform PCB

The optional transform PCB handles all system matrix operations and coordinate transformations. The system processor PCB detects the presence of the transform PCB and sends transform operations to the transform PCB for execution. This arrangement frees the system processor PCB and MCP PCB to continue operating during transformation operations.

The transform PCB (figure F04-32) has five functional elements:

- Interface logic
- Processor logic
- Memory logic
- Register logic
- Multiplier logic

The interface logic buffers clock and control signals from the system and generates internal control signals. Processor logic generates control signals that control matrix operations and coordinate transformations. The memory logic stores data being manipulated by the transform PCB. The register logic stores and adds data from internal bus TBUS0-15. The multiplier logic multiplies and adds data from internal bus TBUS0-15.

4.5.16.a Interface Logic. Power-on reset clear signal 9PORCLR generates internal clear signal 9POR/RESET. Write signal 9BWRT routes data from display bus 9BDATA00-15 onto internal data bus TBUS0-15. Read signal 9BREAD routes PCB internal data onto display bus 9BDATA00-15. Address signals 4BADR0-7 select one of three output ports. Bus handshake signal 9BWAIT prevents further operations until the current display bus operation is completed.

Display bus 9BDATA00-15 routes instructions, data, and status signals between the transform PCB and the system. The interface logic buffers differential system clock signals NTHQ, PTHQ, NTFQ, PTFQ, NTMCQ, PTMCQ, NTSQ, and PTSQ. The buffered clock signals (not shown) synchronize transform PCB operations.

4.5.16.b Processor Logic. The processor logic (figure F04-33) has a microprogrammed sequencer with a PROM control memory. The PROM control memory loads 40-bit-wide instruction words into a pipeline register. Individual instruction bits and decoded additional signals route data and start operations within the transform PCB.

4.5.16.c Memory Logic. The memory logic (figure 4-82) has 4096 x 16-bit static RAM, partitioned into sixteen 256 x 16-bit blocks. The memory logic adds the address specified by the processor logic with the output from one of two address counters to generate the current address. Data loaded into the context latch selects the active block of memory.

4.5.16.d Register Logic. The register logic stores data from internal bus TBUS0-15. Two 16-bit words can be stored and added together under processor logic control. Adder status signals UN and OV, and matrix stack counter status signals 2 STACK FULL and 2 STACK EMPTY set interface logic status registers.

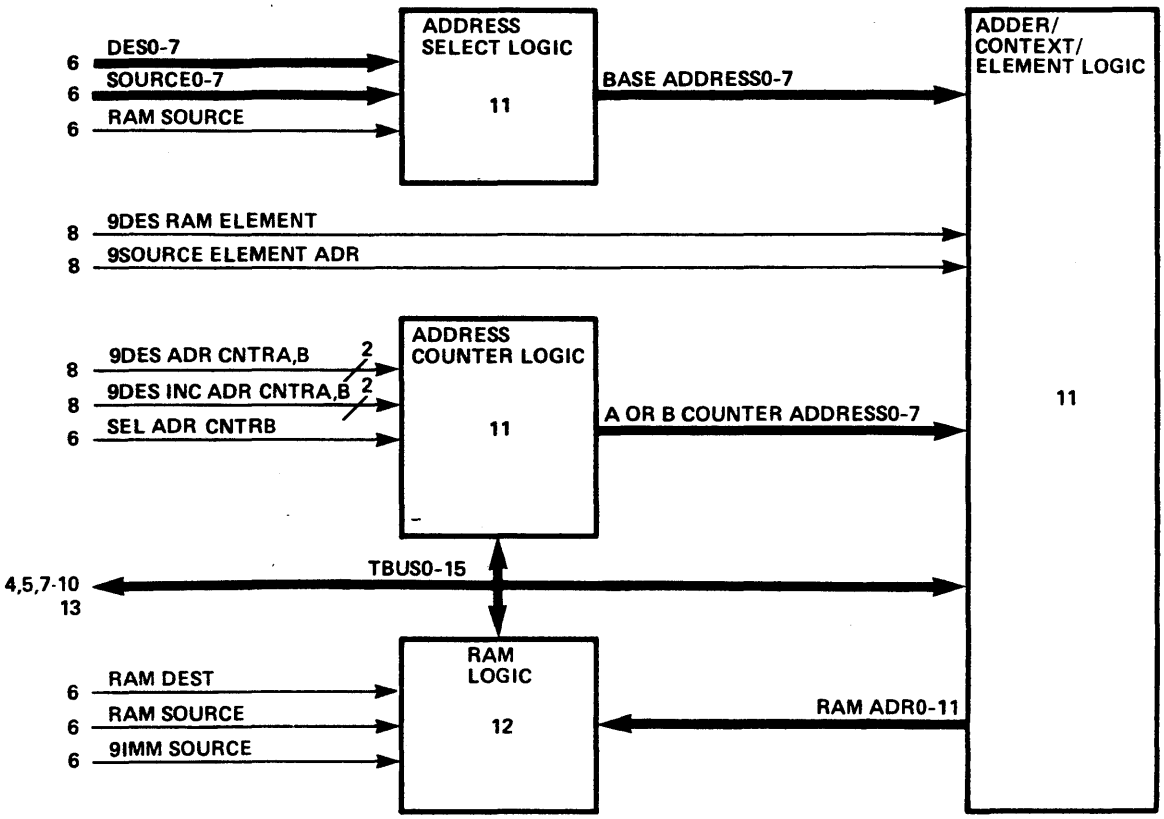


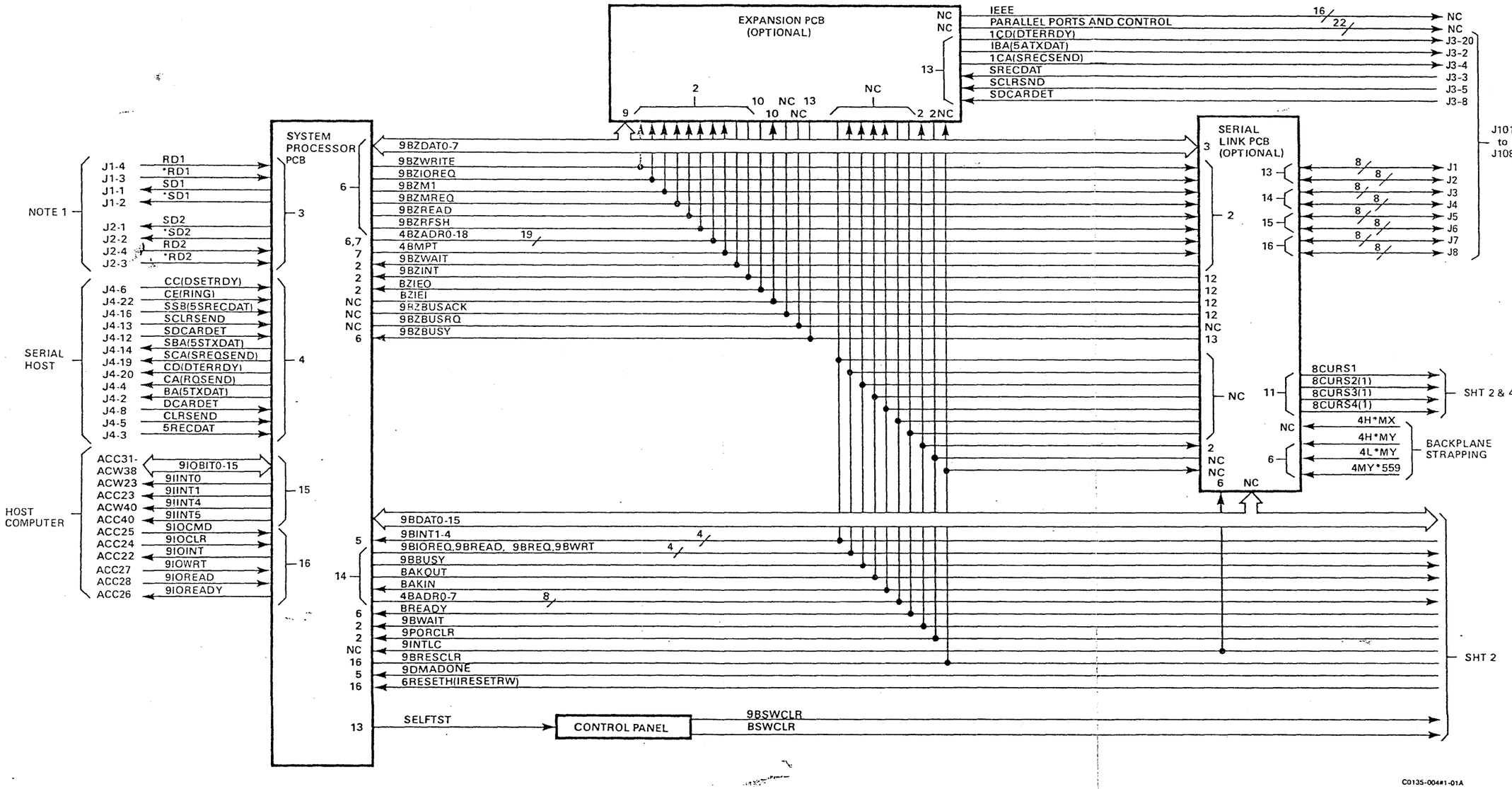
Figure 4-82. Memory Logic

4.5.16.e Multiplier Logic. The multiplier logic multiplies one 16-bit value and one 32-bit value or two 32-bit values. An adder generates the most significant product (MSP) and central significant product (CSP).

4.5.16.f Process Description. The transform PCB performs the following operations:

- Matrix-matrix multiplication
- Vector-matrix multiplication
- Matrix loading
- Matrix relocation
- General arithmetic
- Set parameters
- Input/output

Matrix-matrix multiplication multiplies matrix A times matrix B and stores the result in location A, B, or C. Vector-matrix multiplication multiplies a coordinate pair (vector) times the current matrix or the inverse matrix. The matrix loading operation loads any matrix (0 through 7) with operator-specified values. Matrix relocation moves matrices from one location to another, onto the matrix stack, or off the matrix stack. General arithmetic operations include multiplication of a specific multiplier with a signed 32-bit multiplicand and addition of two 16-bit signed integers. The set parameters operation sets an index value and sets or clears the relative addressing flag. Input/output operations include reading transformed coordinates, reading the local current operating point, and reading or writing to a specified block of RAM.



NOTE 1: CONNECT TO J101 AND J102 WHEN NO SERIAL LINK PCB IS INSTALLED

Figure F04-1. 9465 Block Diagram (Sheet 1 of 4)

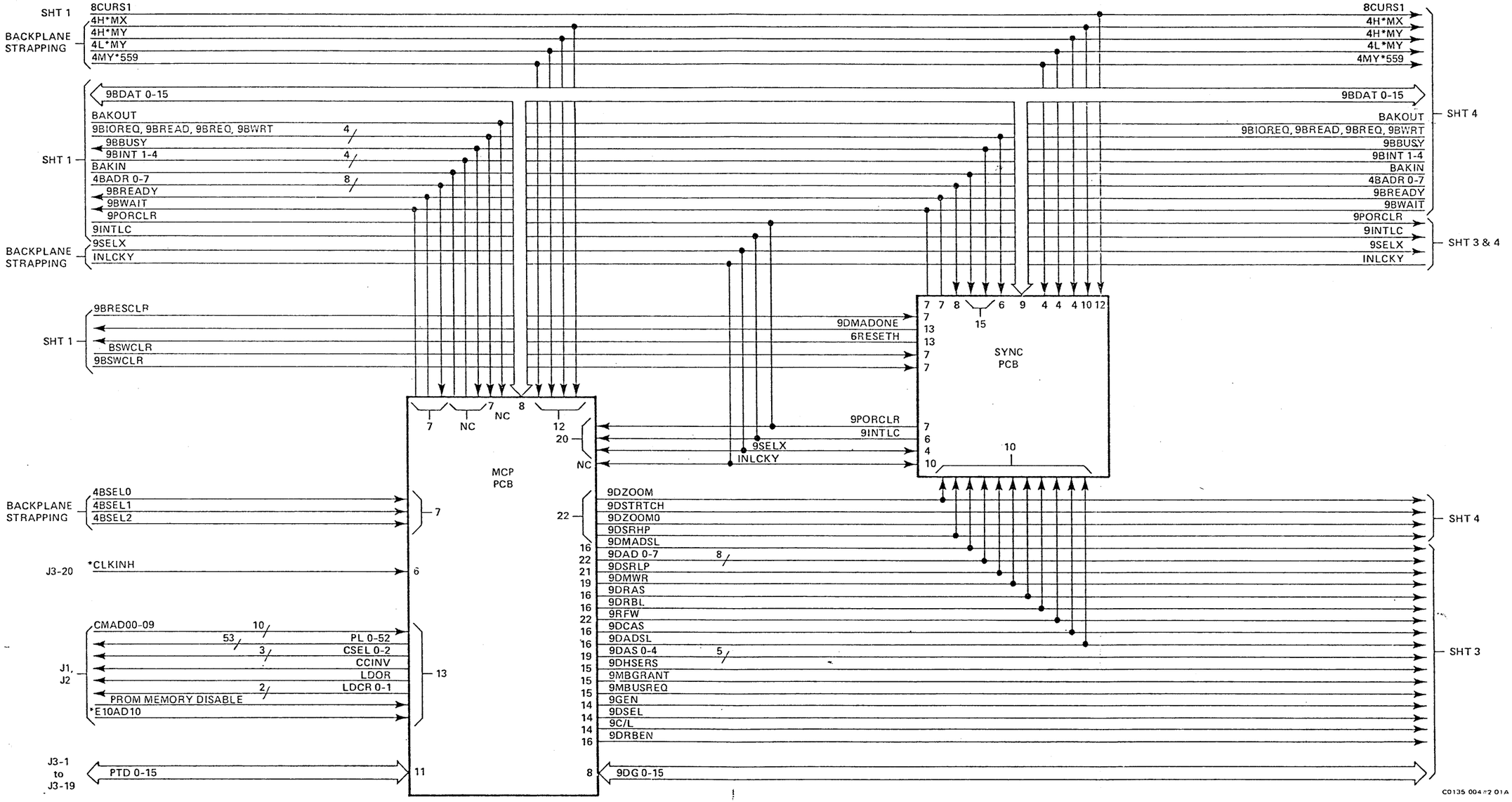


Figure F04-1. 9465 Block Diagram (Sheet 2 of 4)

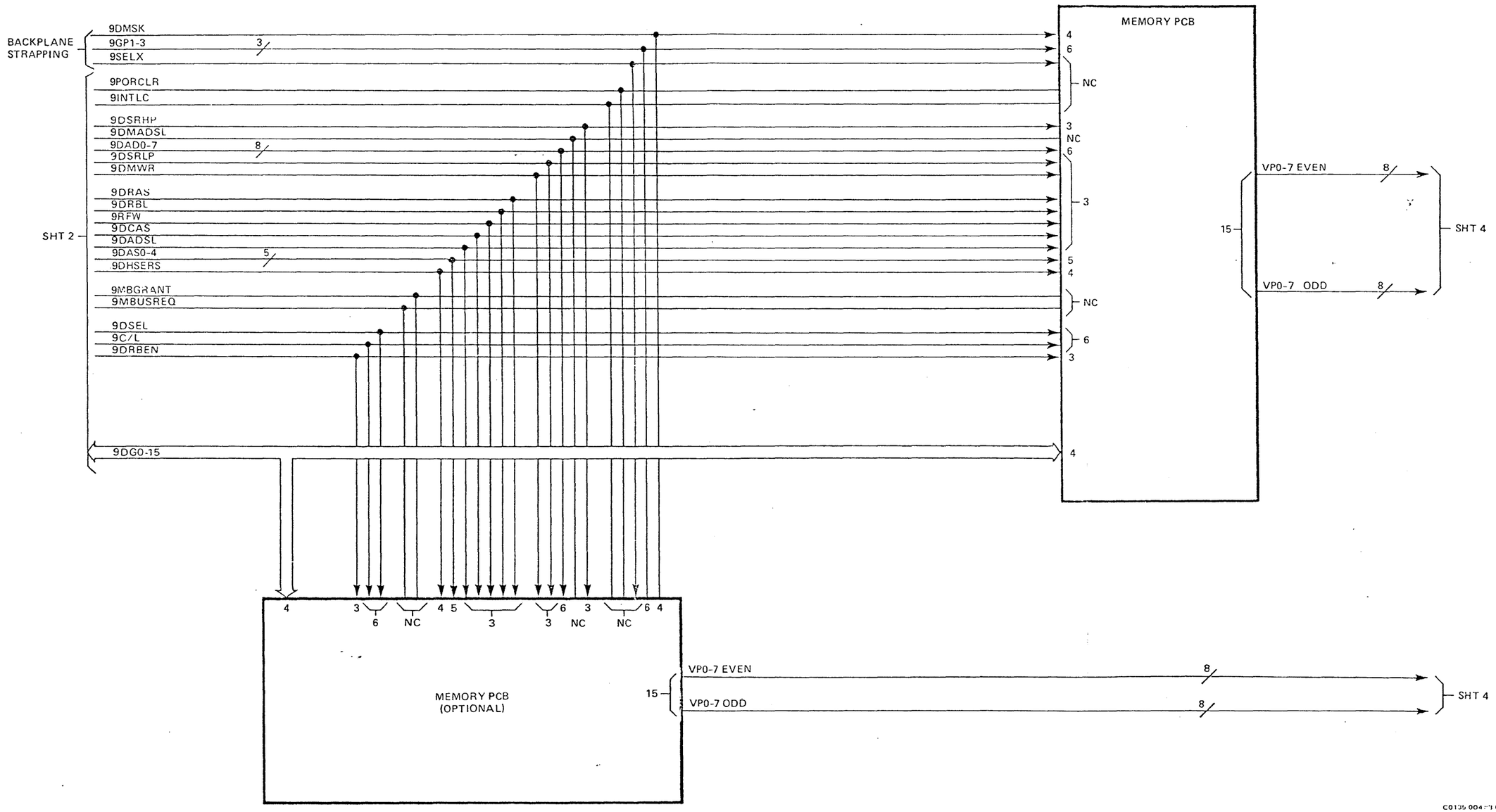


Figure F04-1. 9465 Block Diagram
(Sheet 3 of 4)

8000110-01A

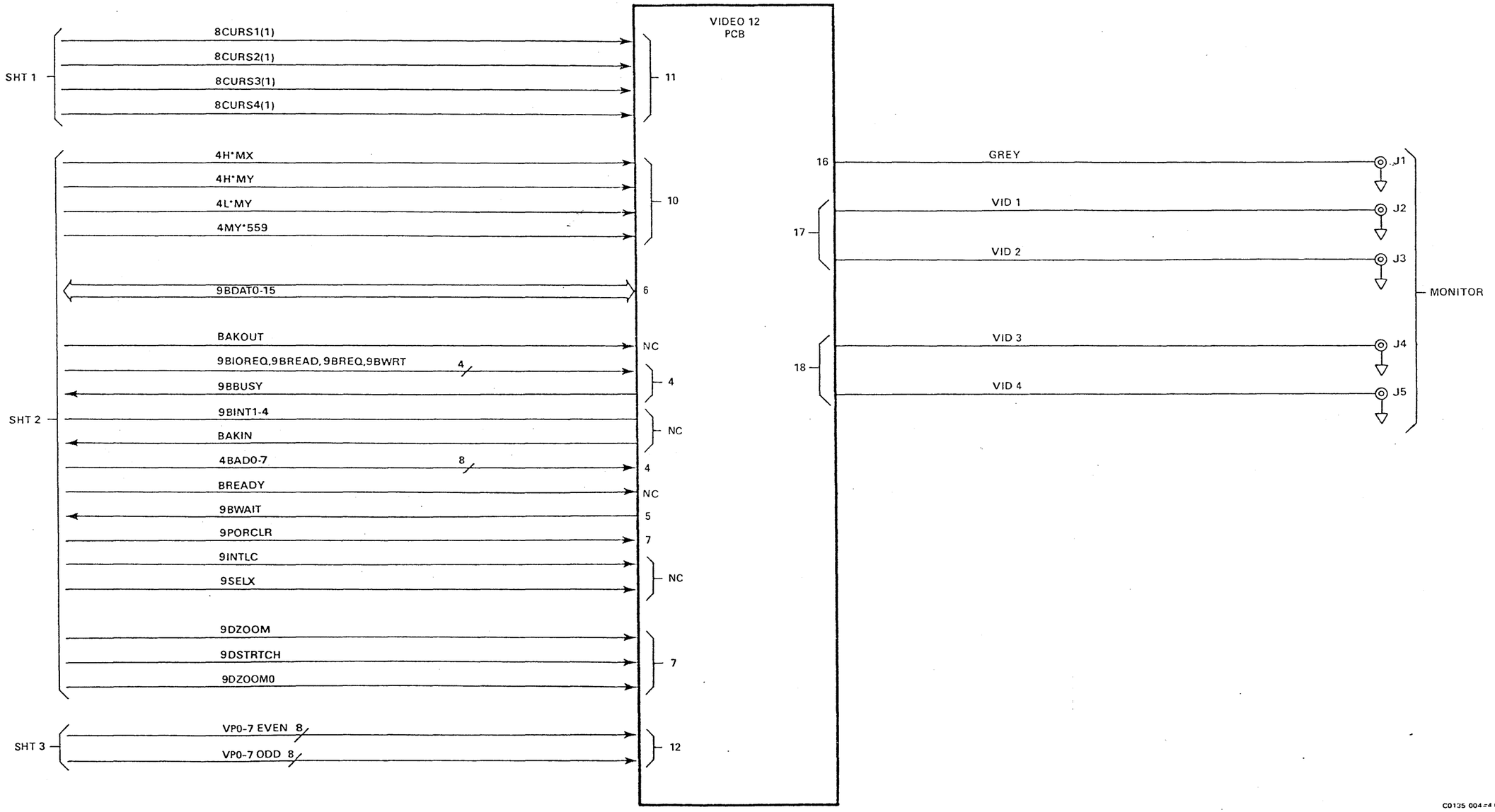


Figure F04-1. 9465 Block Diagram
(Sheet 4 of 4)

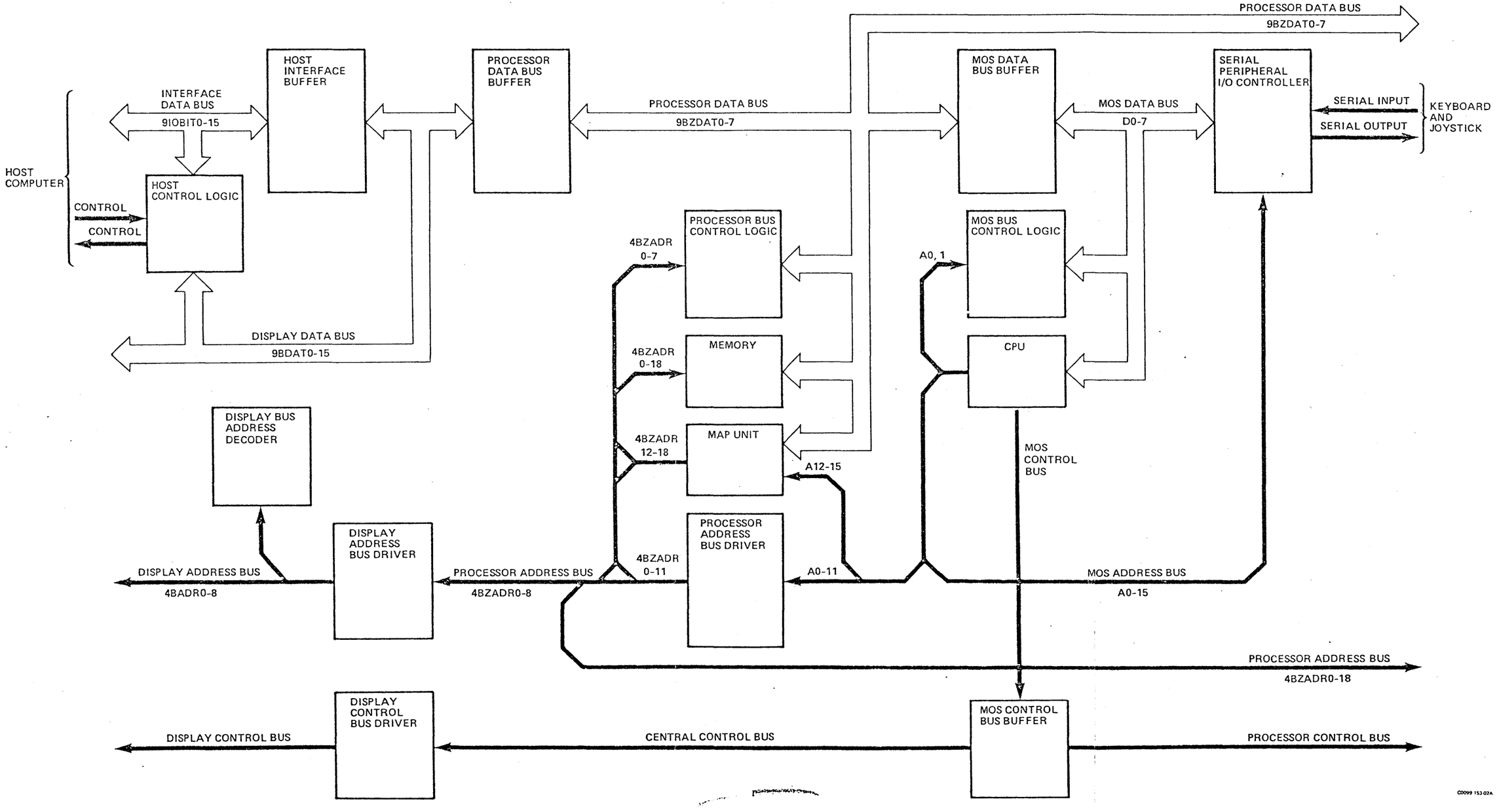


Figure F04-2. System Processor PCB (Z80) Buses

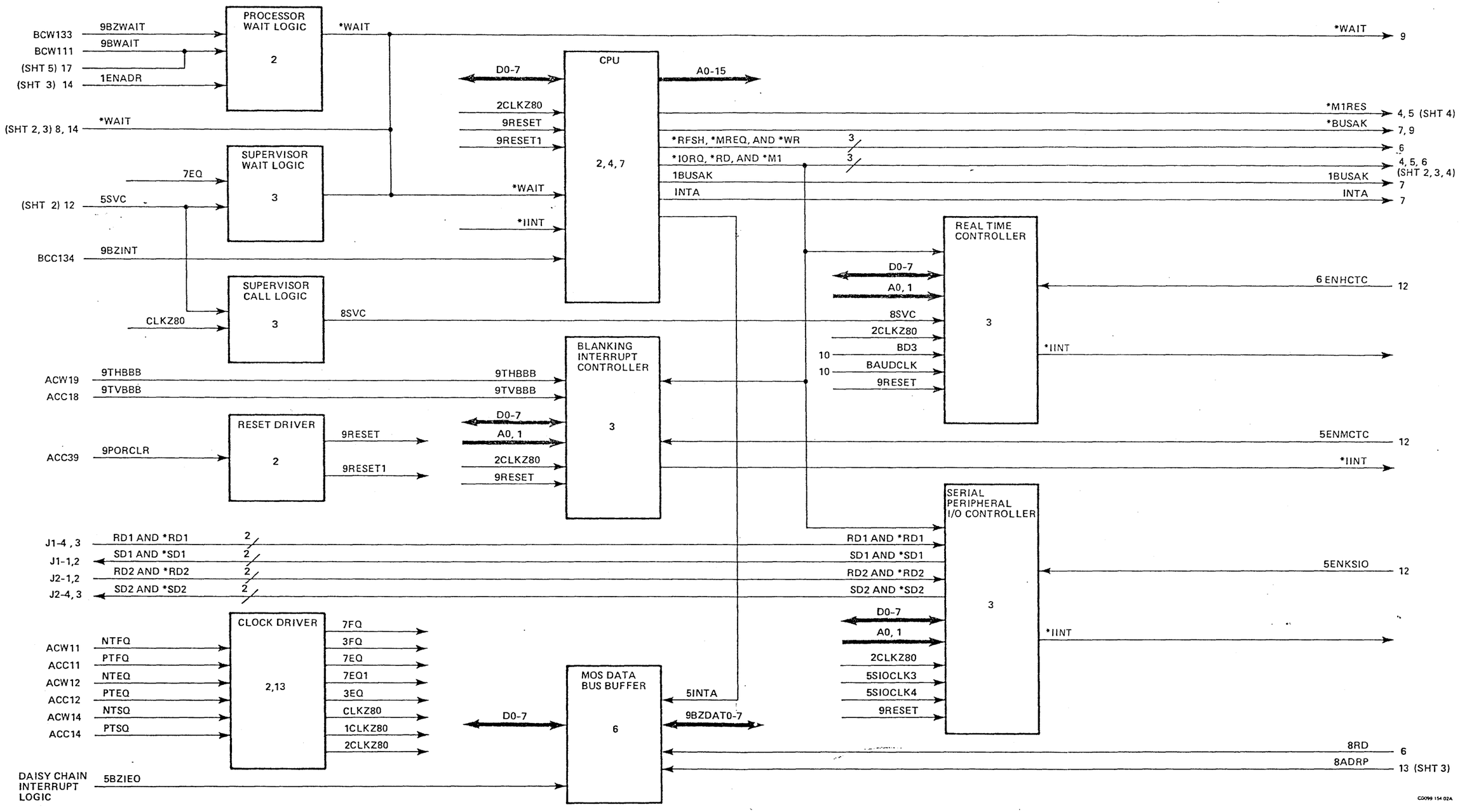
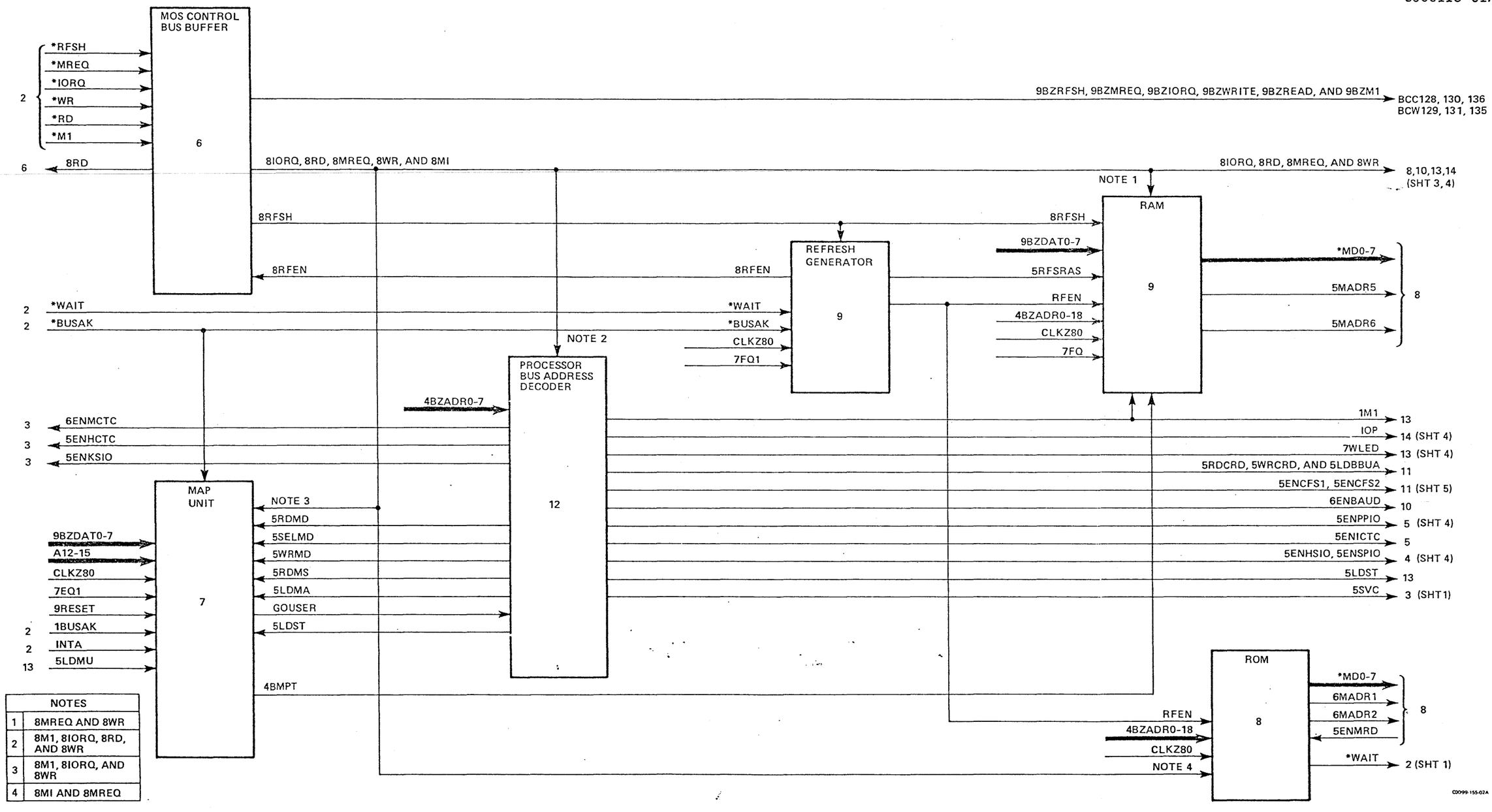


Figure F04-3. System Processor PCB (Z80) Control Signals (Sheet 1 of 5)



NOTES	
1	8MREQ AND 8WR
2	8M1, 8IORQ, 8RD, AND 8WR
3	8M1, 8IORQ, AND 8WR
4	8MI AND 8MREQ

Figure F04-3. System Processor PCB (Z80) Control Signals (Sheet 2 of 5)

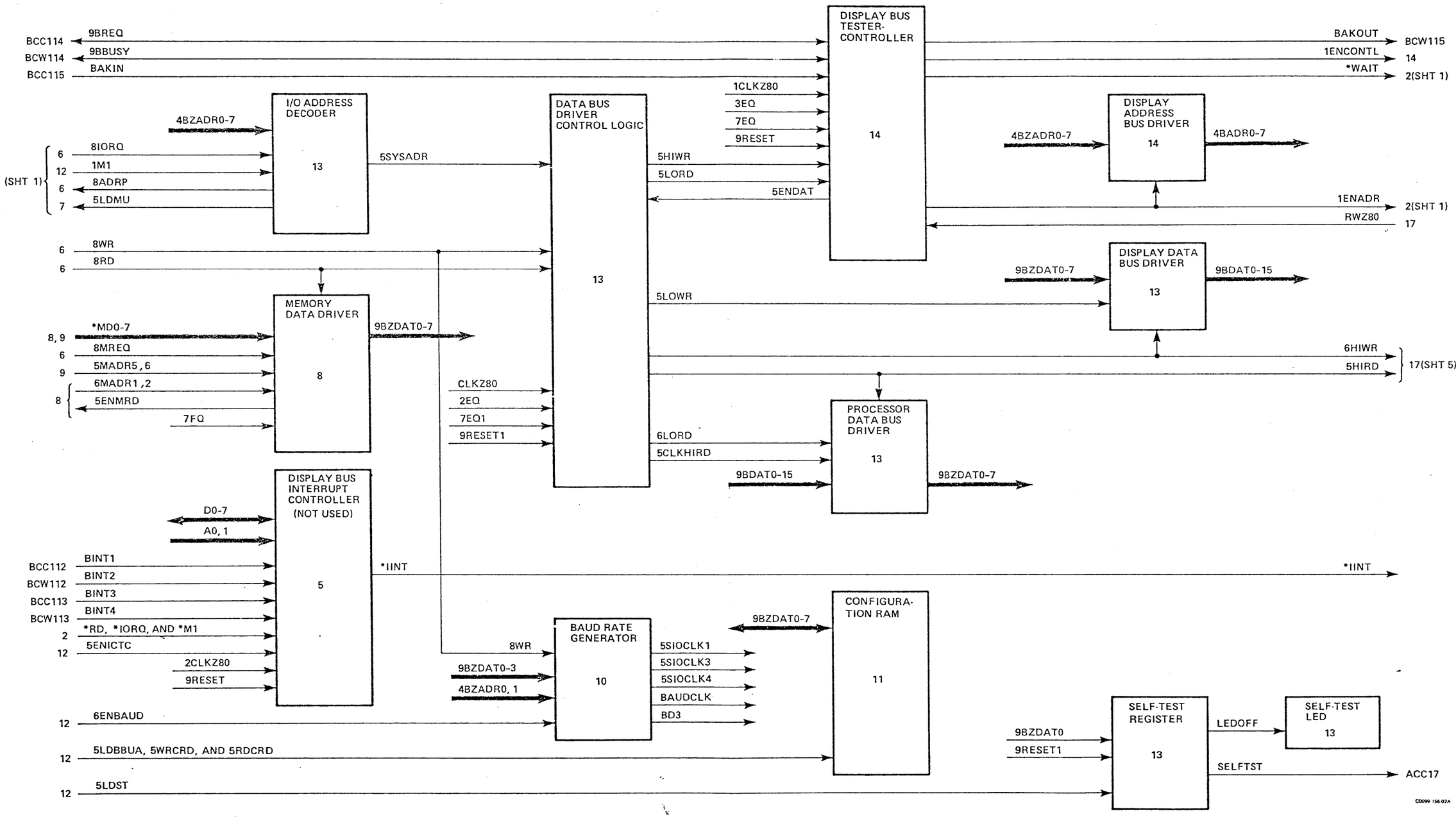


Figure F04-3. System Processor PCB (Z80) Control Signals (Sheet 3 of 5)

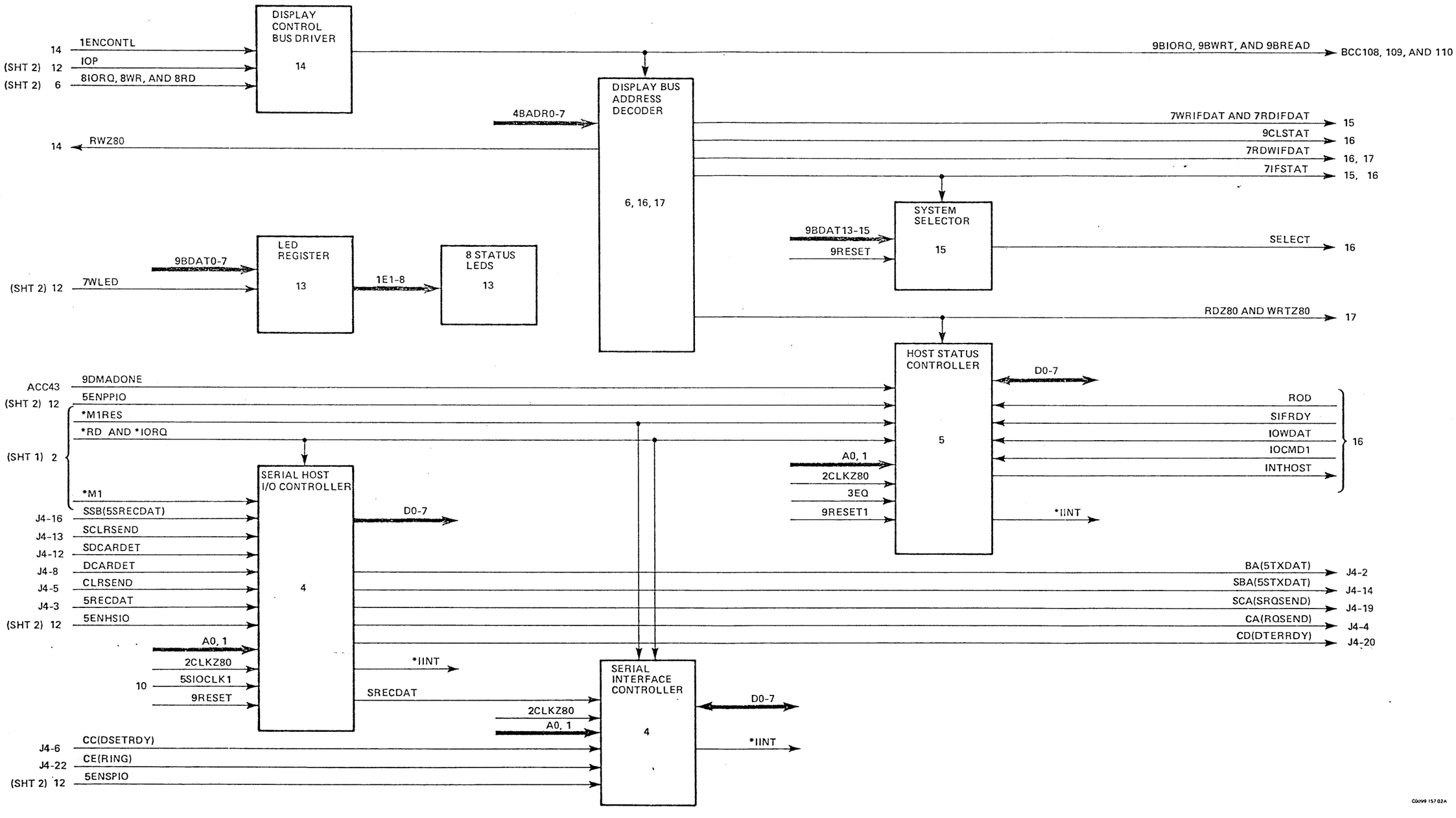


Figure F04-3. System Processor PCB (Z80) Control Signals (Sheet 4 of 5)

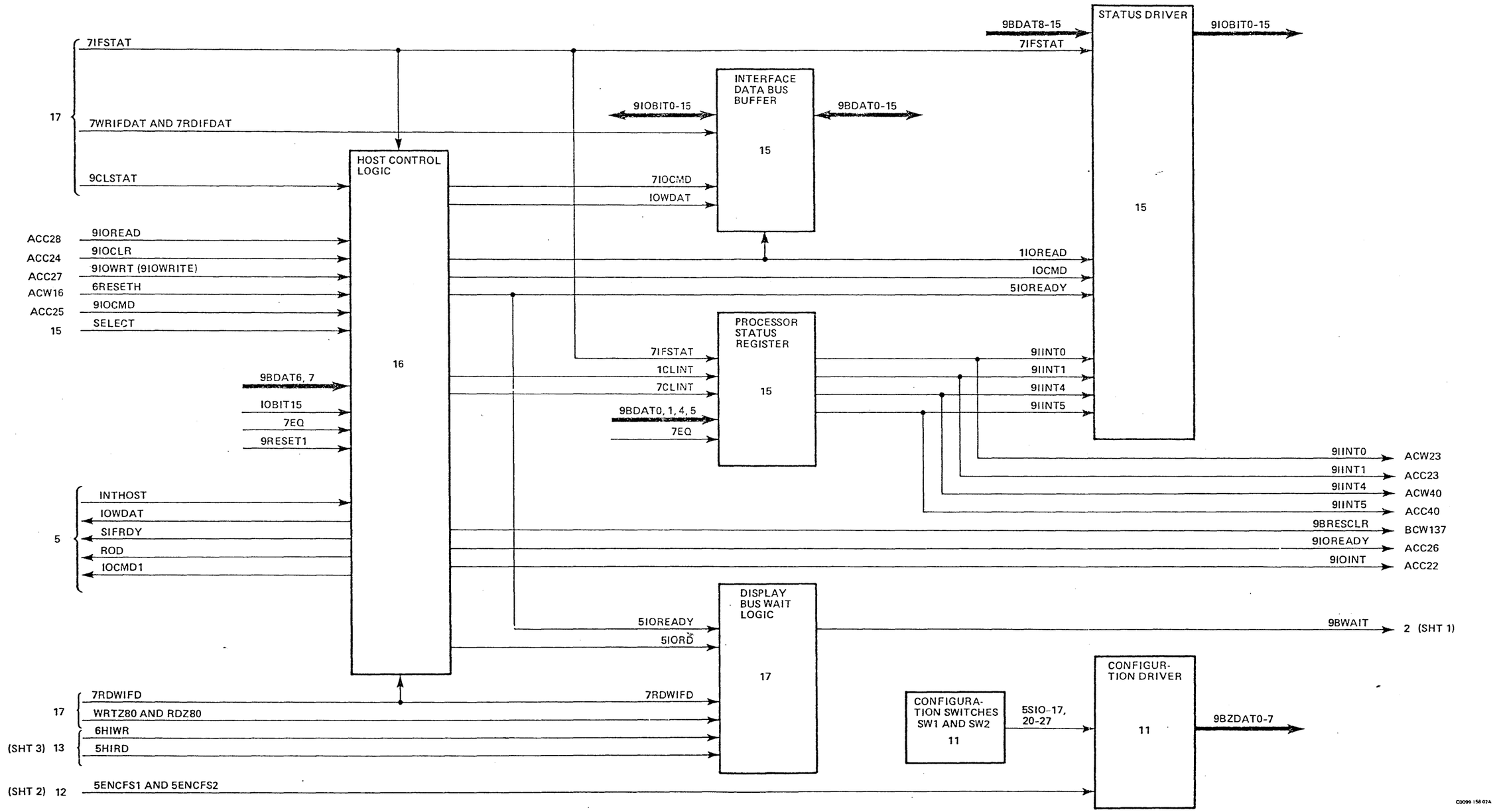


Figure F04-3. System Processor PCB (Z80) Control Signals (Sheet 5 of 5)

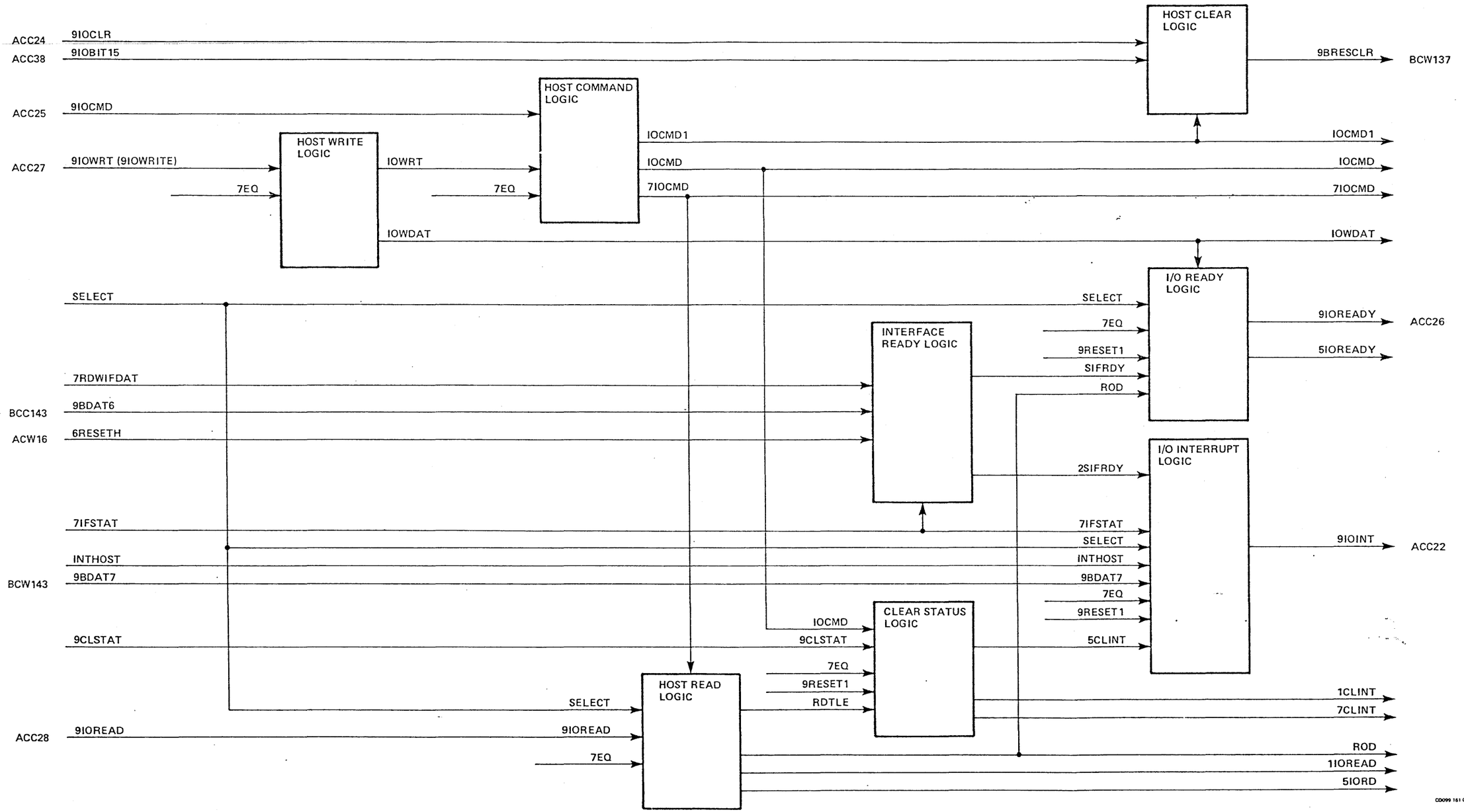


Figure F04-4. Host Control Logic

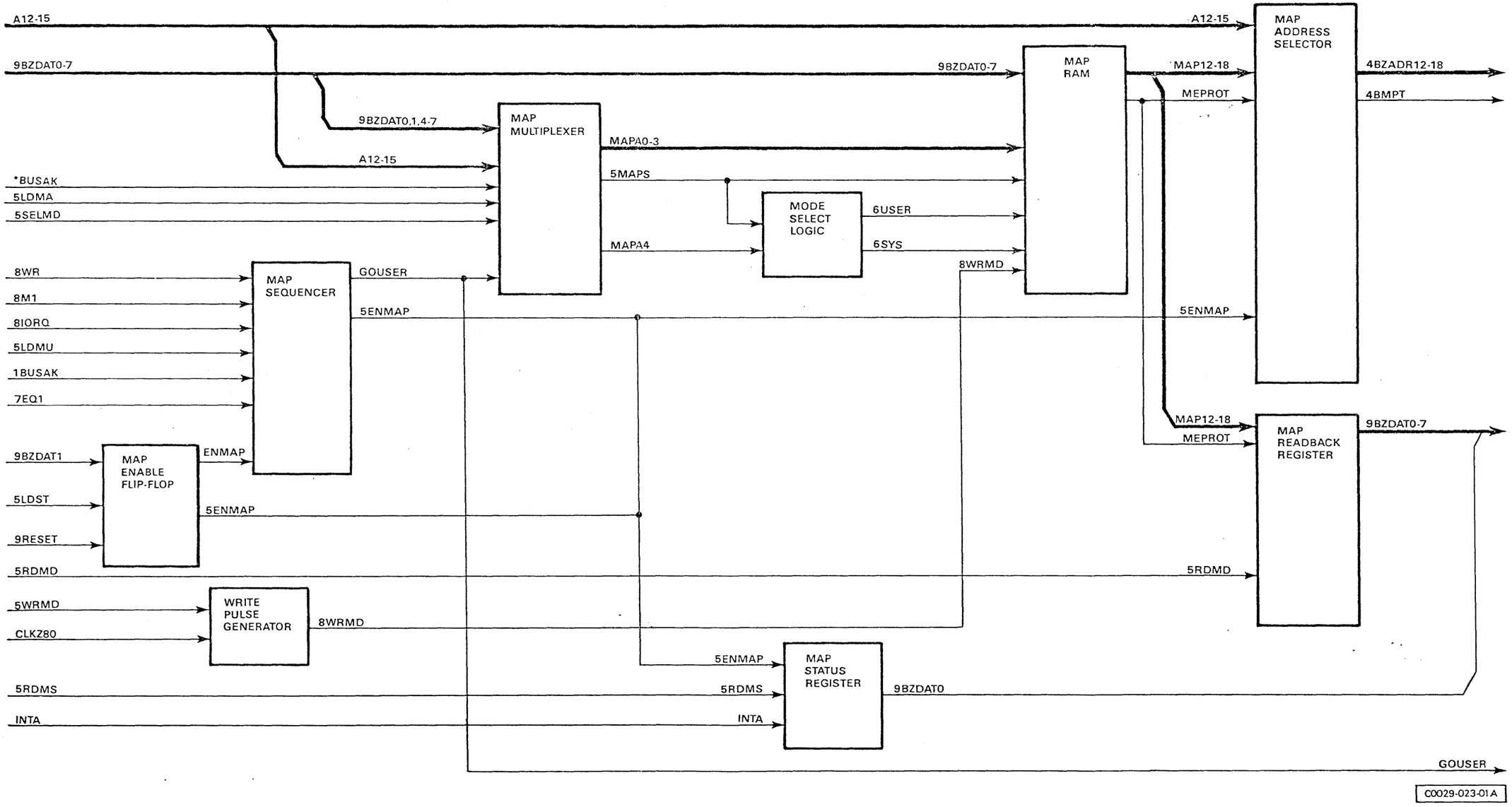


Figure F04-5. MAP Unit

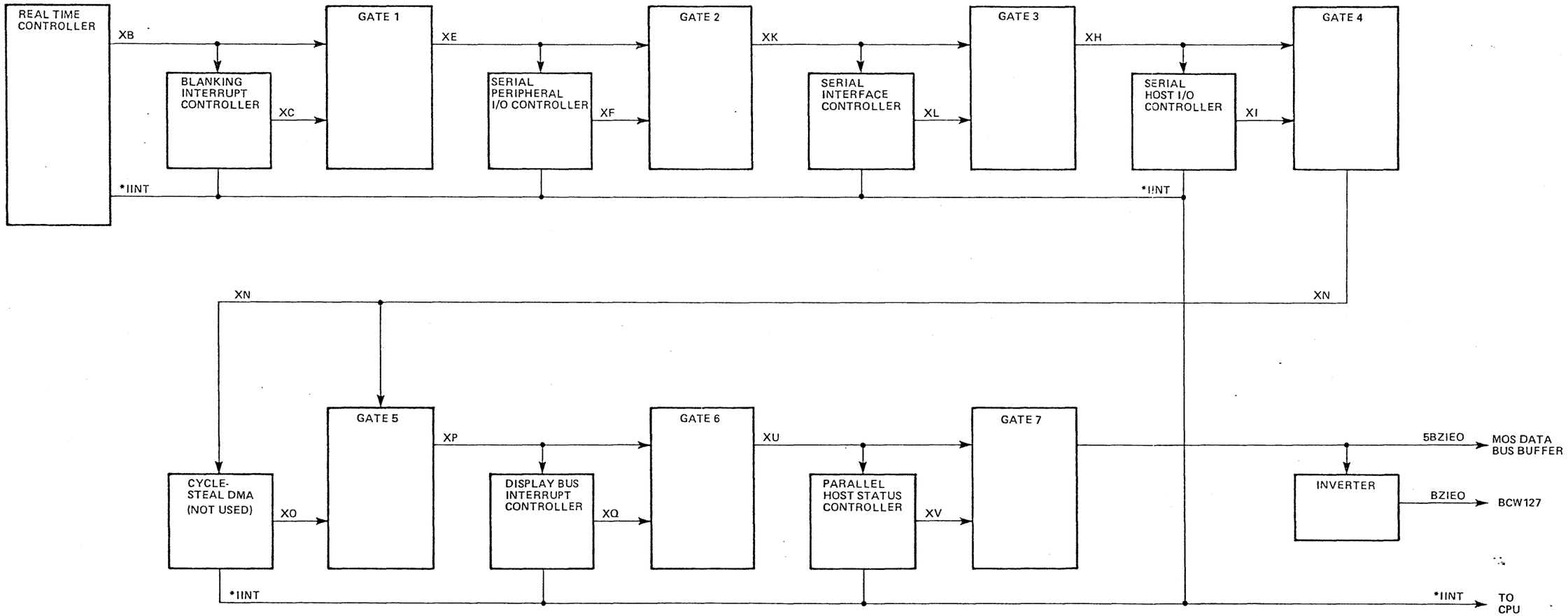


Figure F04-6. Daisy Chain Interrupt Logic

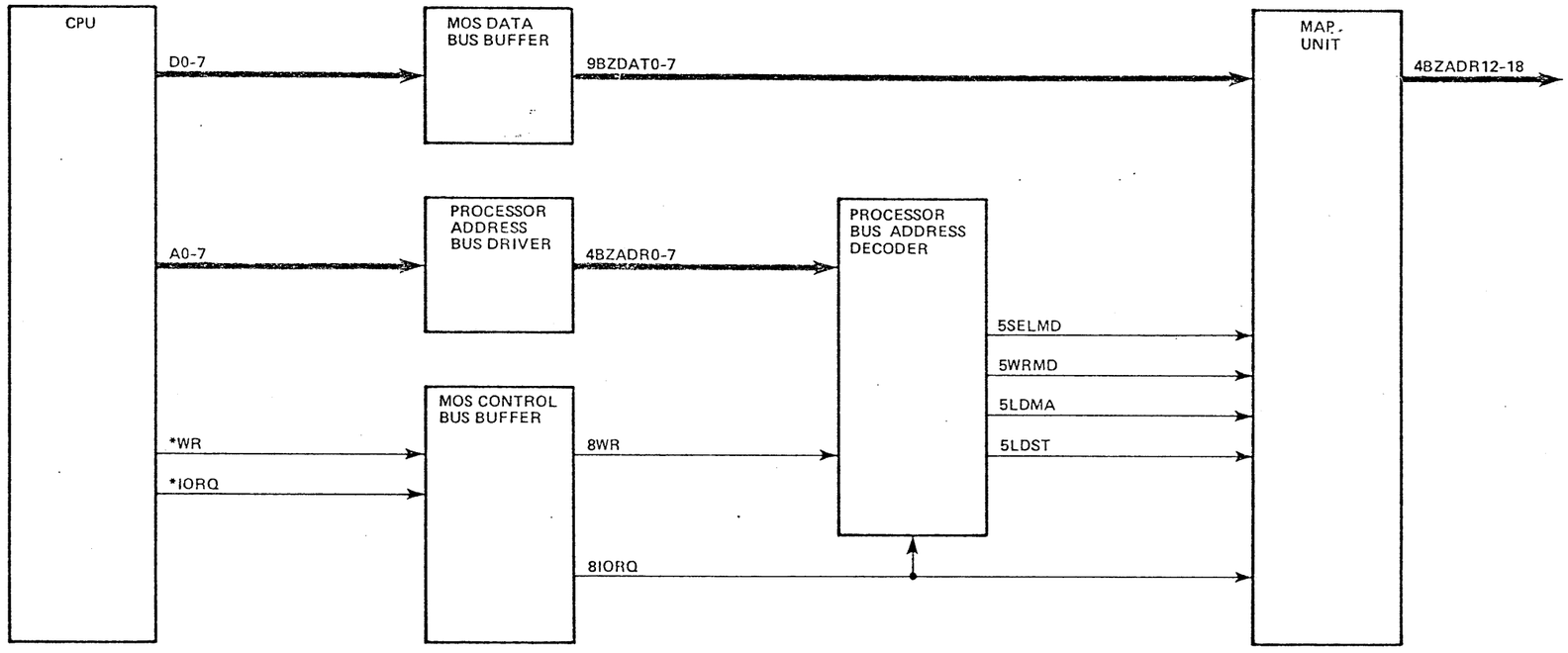


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Figure FO4-7. MAP Unit Control

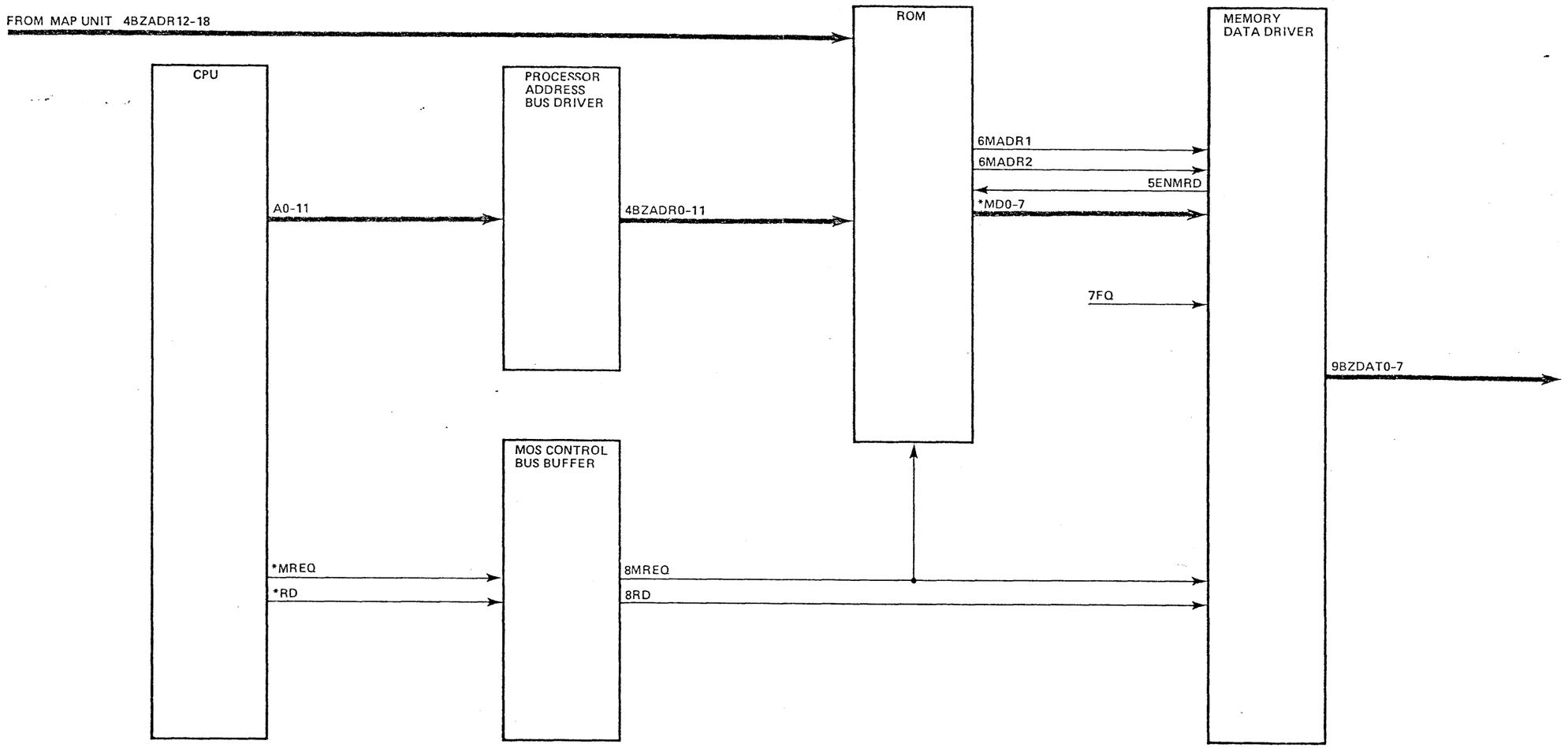


Figure FO4-8. ROM Access

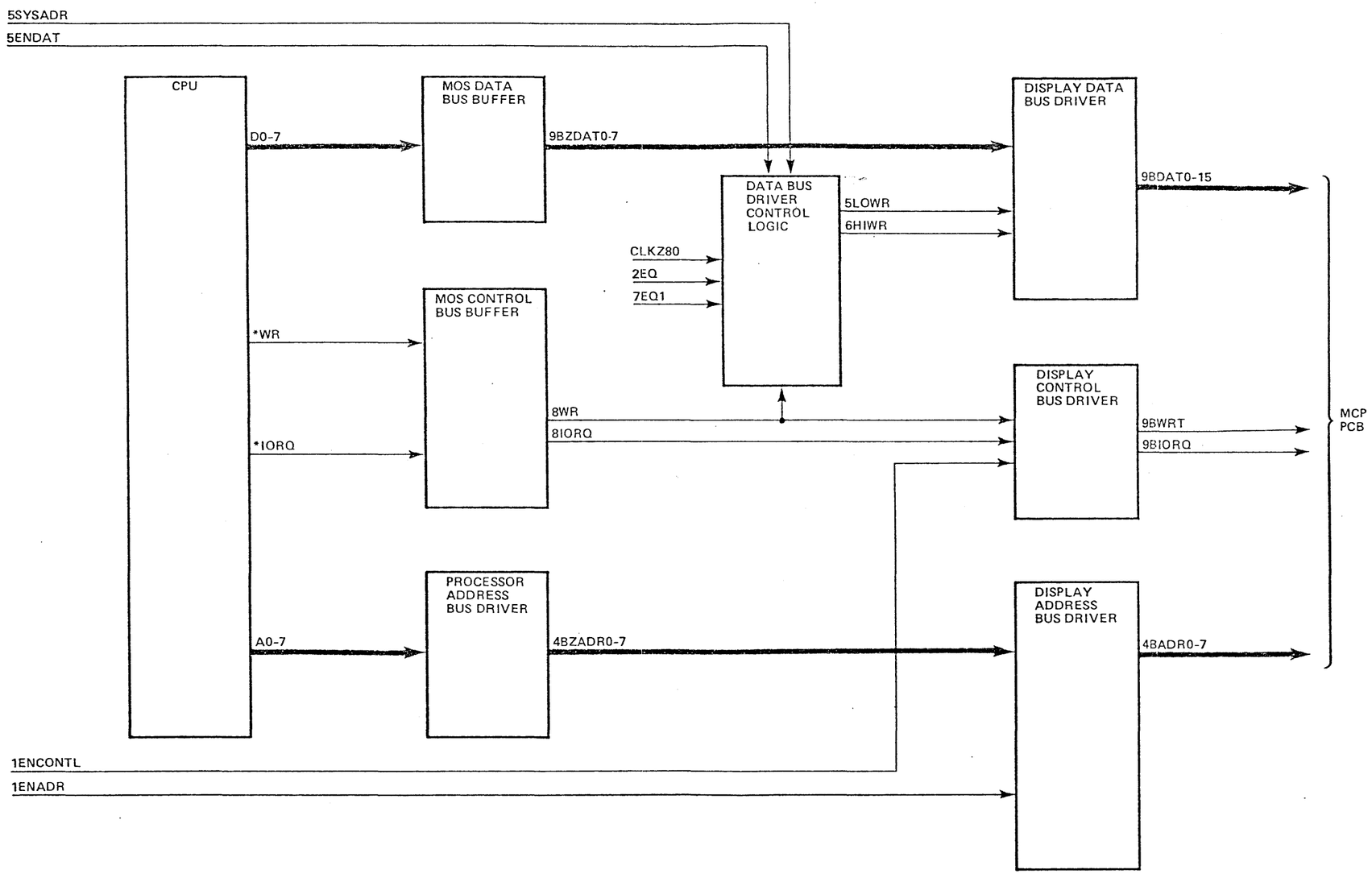


Figure FO4-9. Data Output

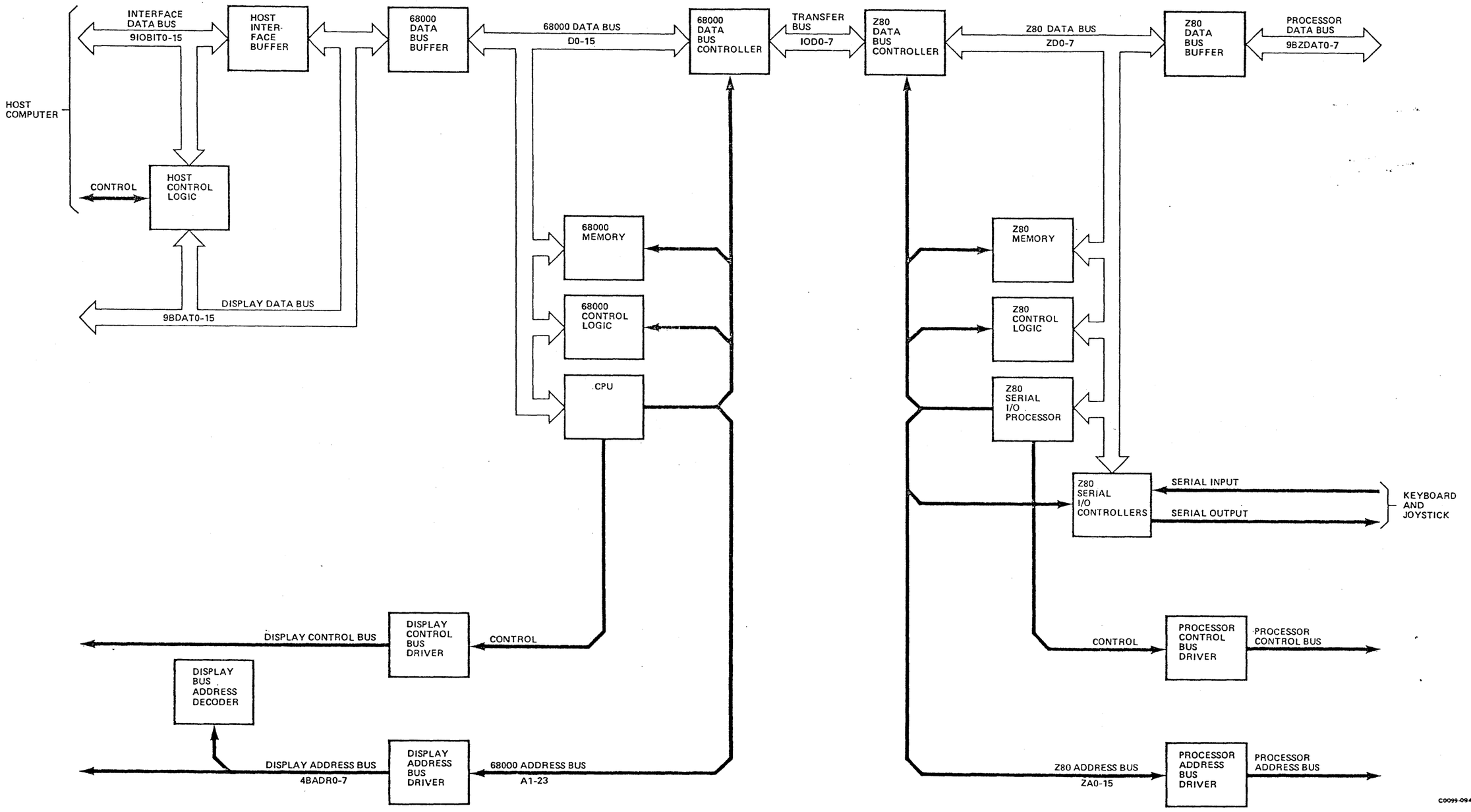


Figure F04-10. System Processor PCB (MC68000) Buses

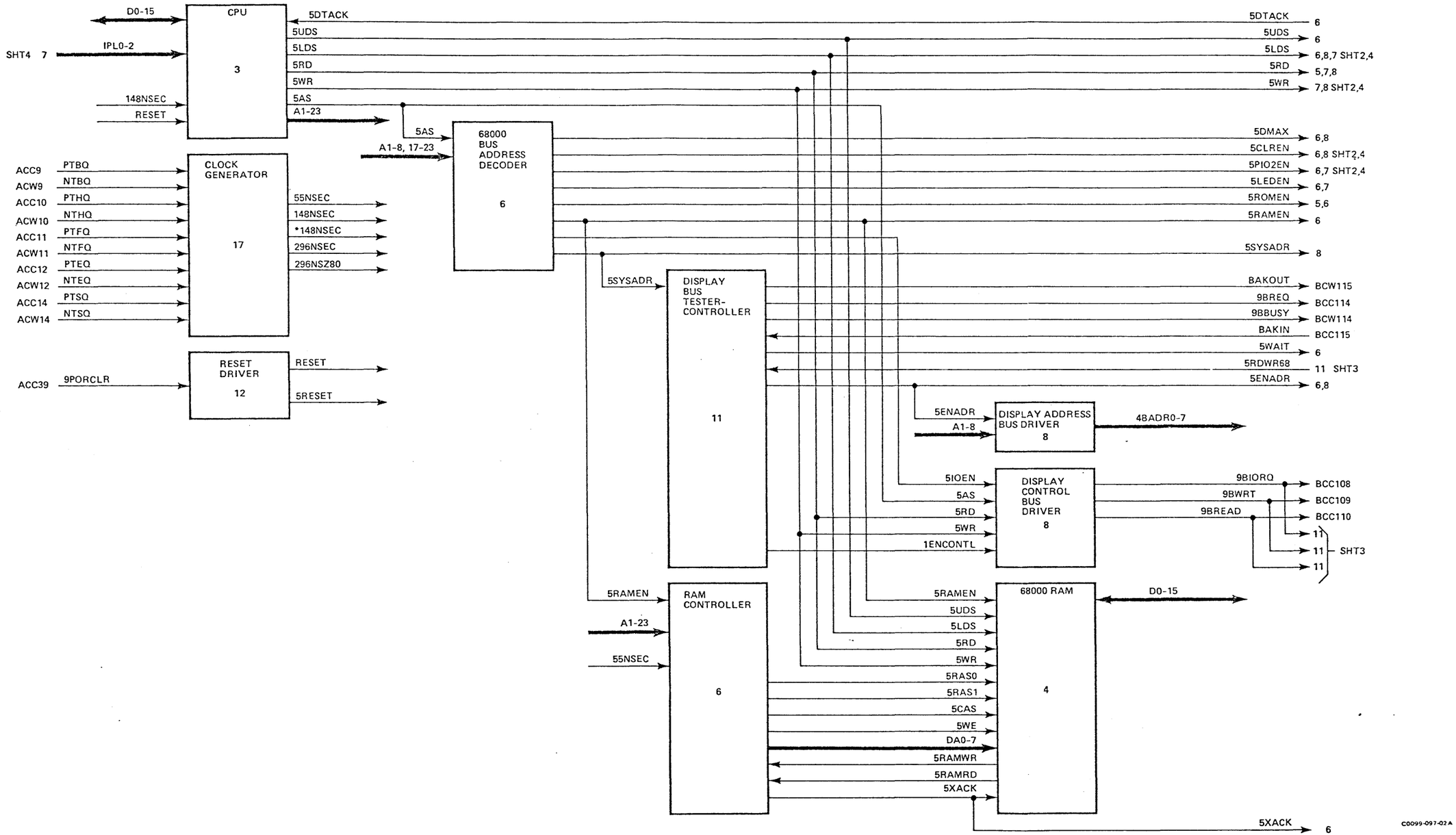


Figure F04-11. System Processor PCB (MC68000) Control Signals (Sheet 1 of 5)

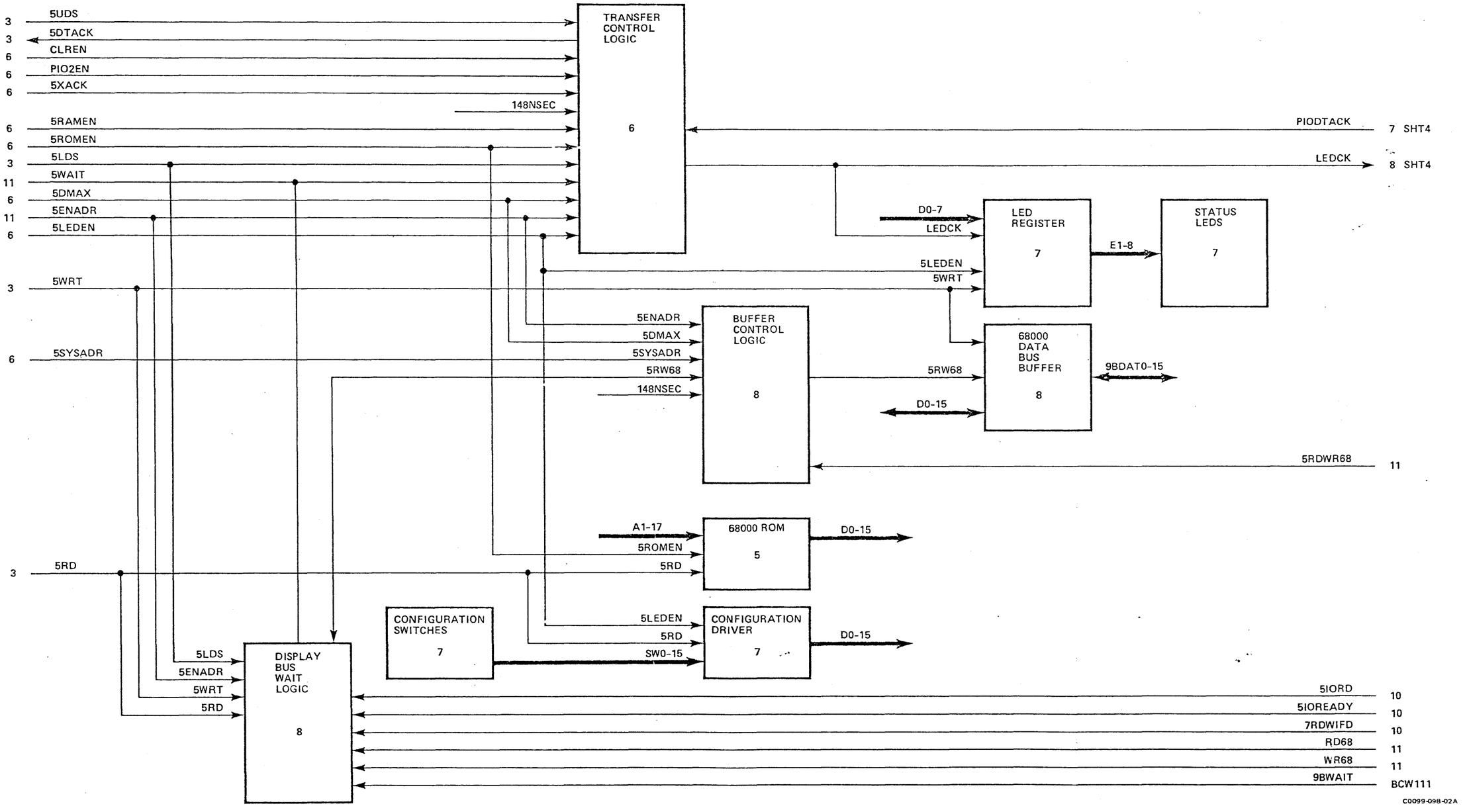


Figure FO4-11. System Processor PCB (MC68000) Control Signals (Sheet 2 of 5)

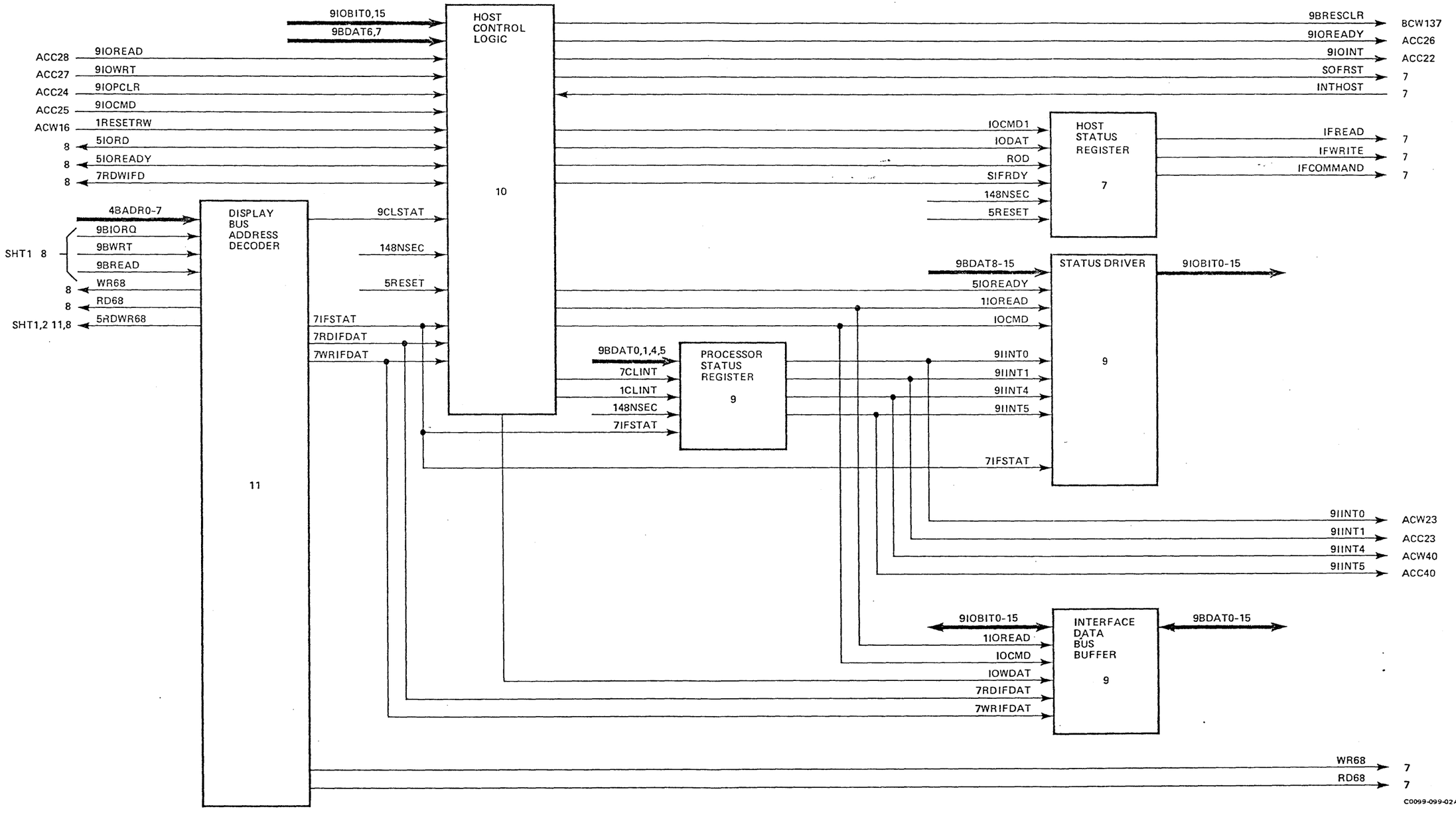


Figure F04-11. System Processor PCB (MC68000) Control Signals (Sheet 3 of 5)

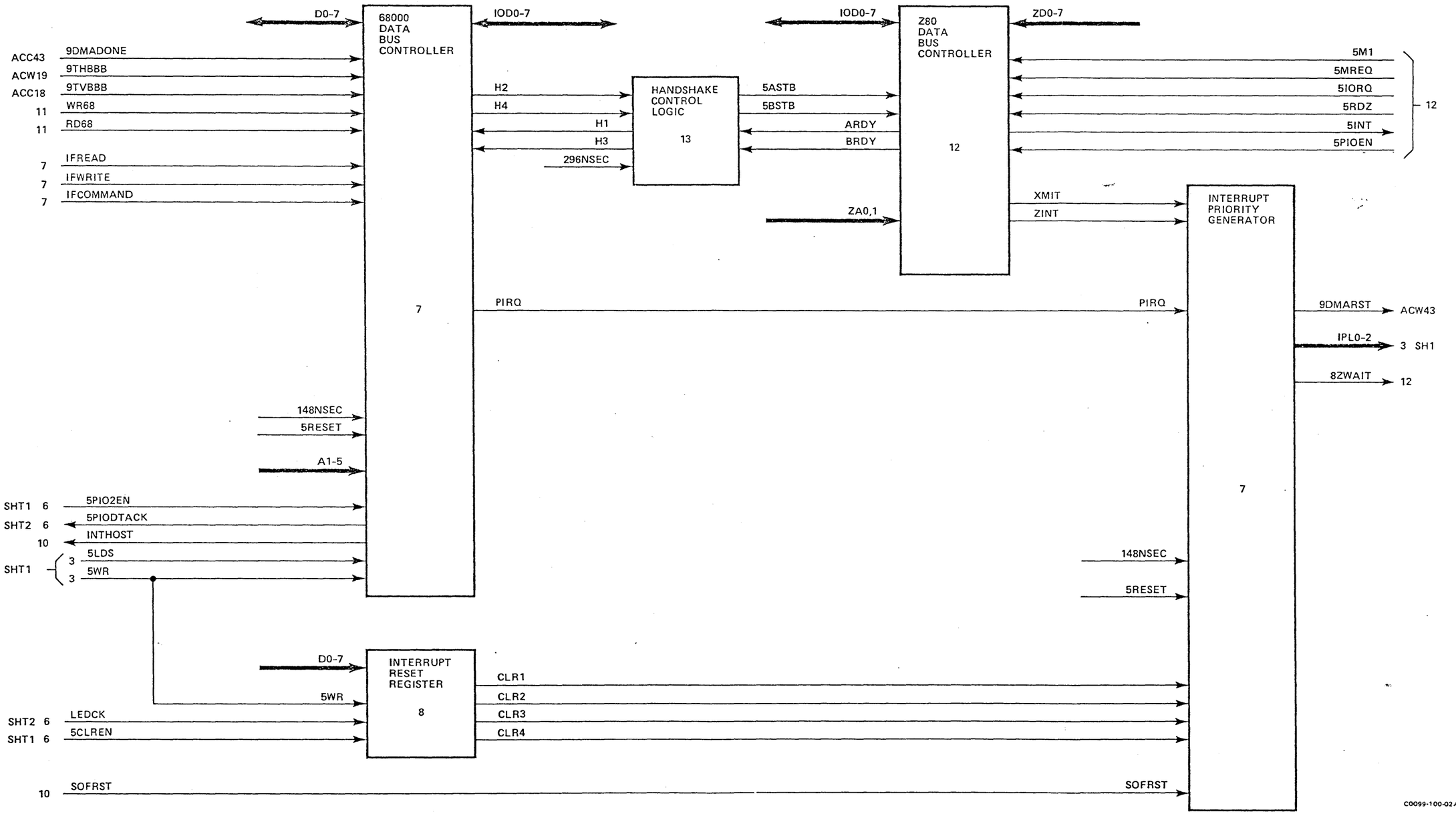


Figure F04-11. System Processor PCB (MC68000) Control Signals (Sheet 4 of 5)

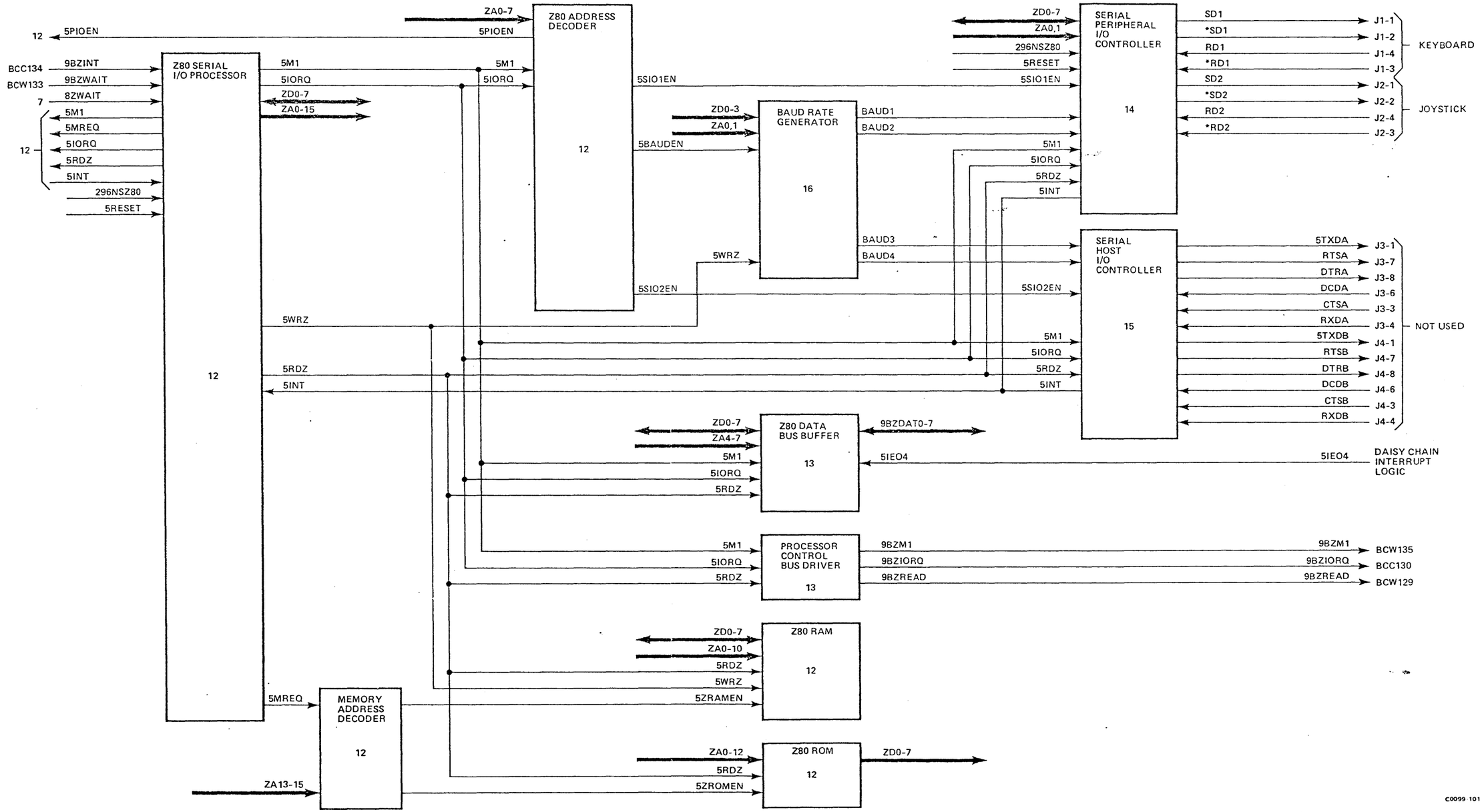


Figure F04-11. System Processor PCB (MC68000) Control Signals (Sheet 5 of 5)

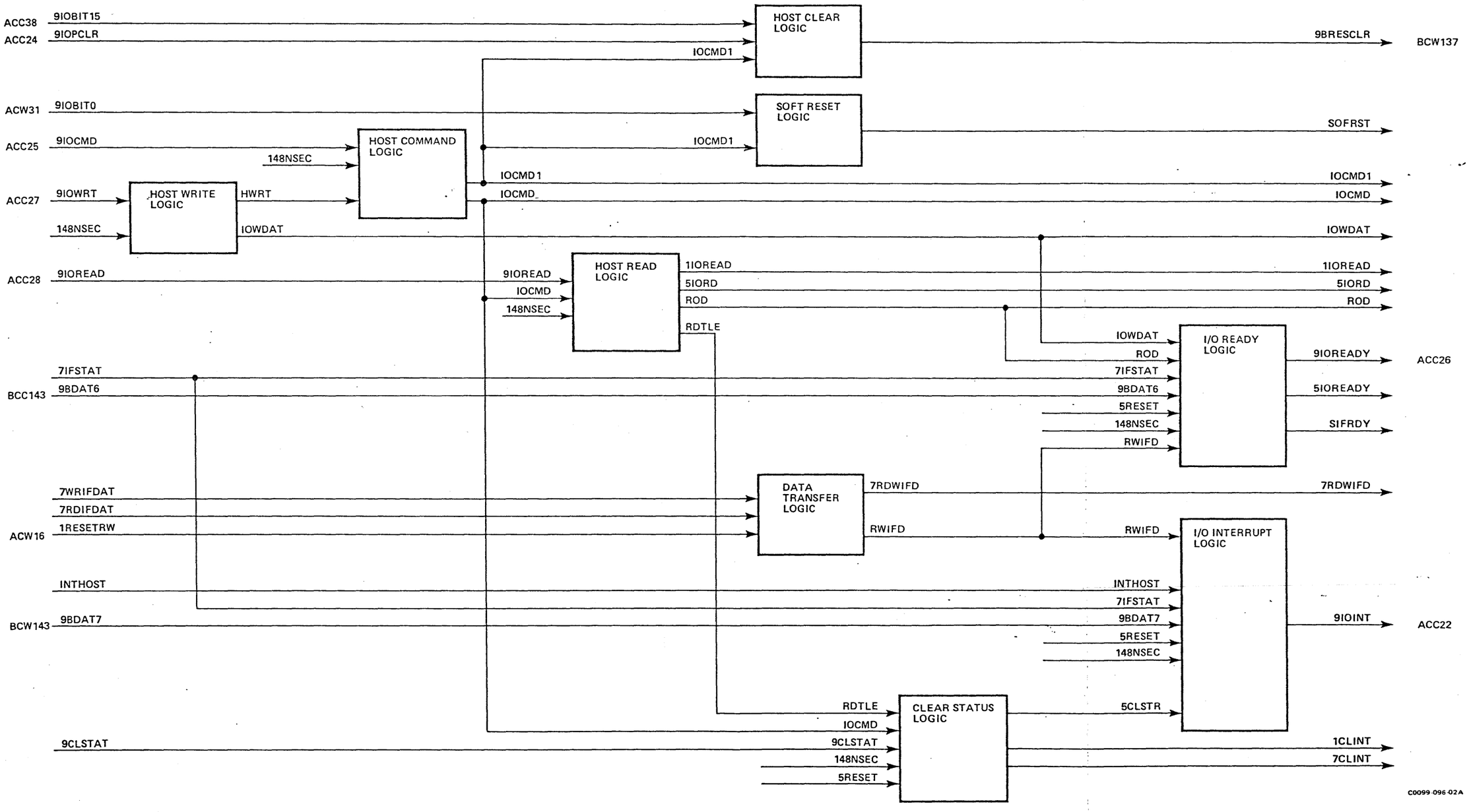
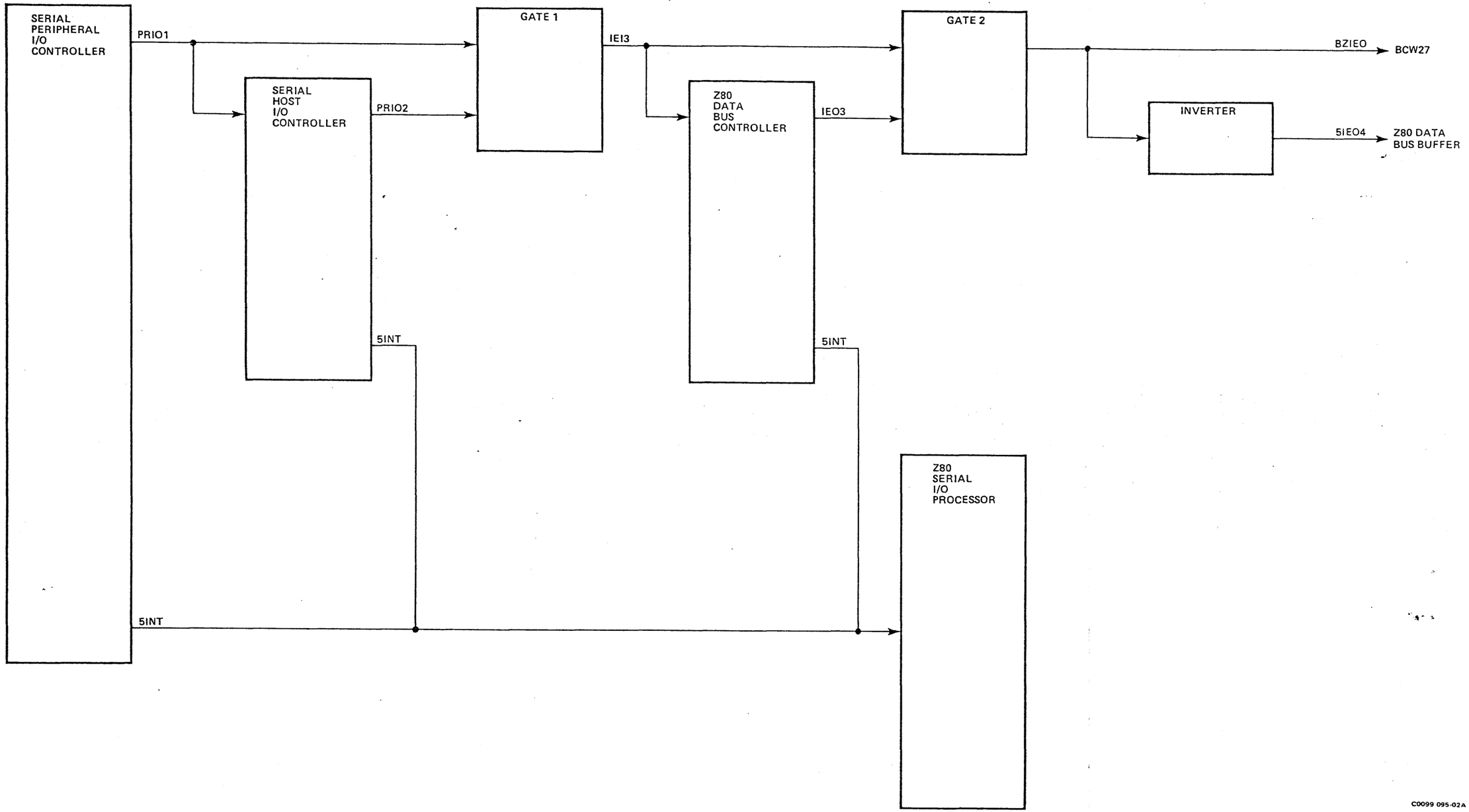


Figure F04-12. Host Control Logic

8000110-01A



C0099 095-02A

Figure F04-13. Daisy Chain Interrupt Logic

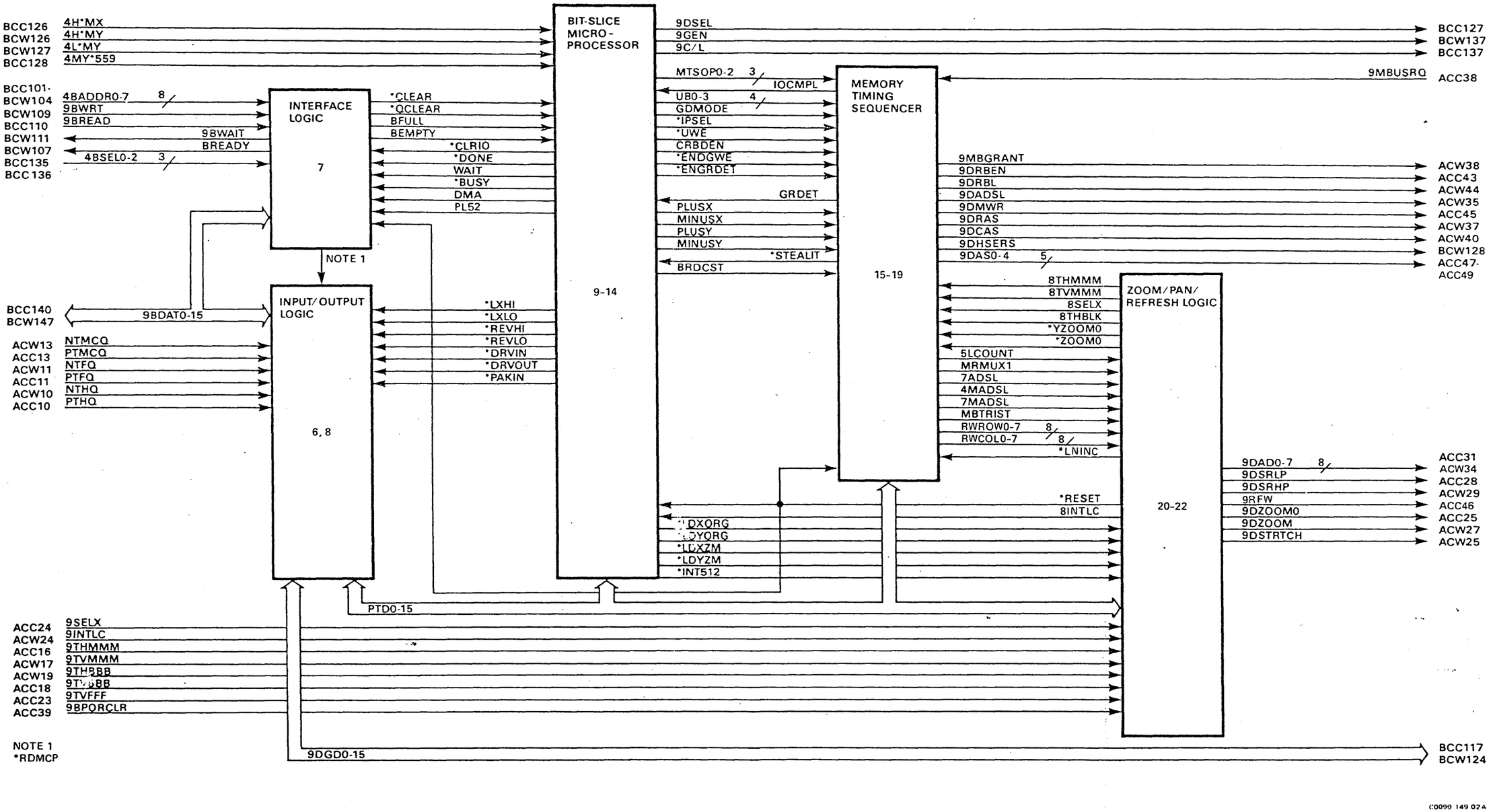


Figure FO4-14. MCP PCB

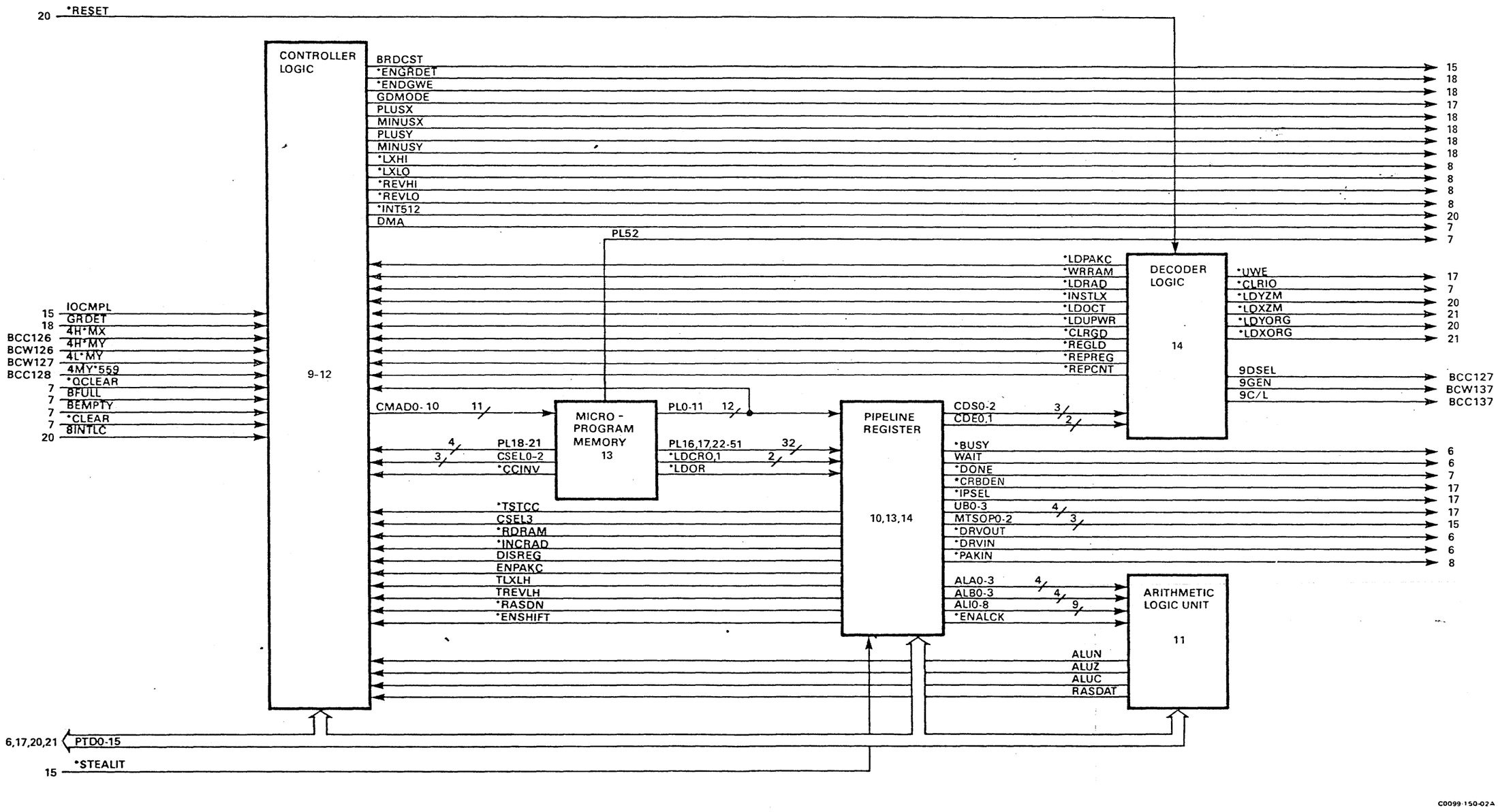


Figure F04-15. BSM

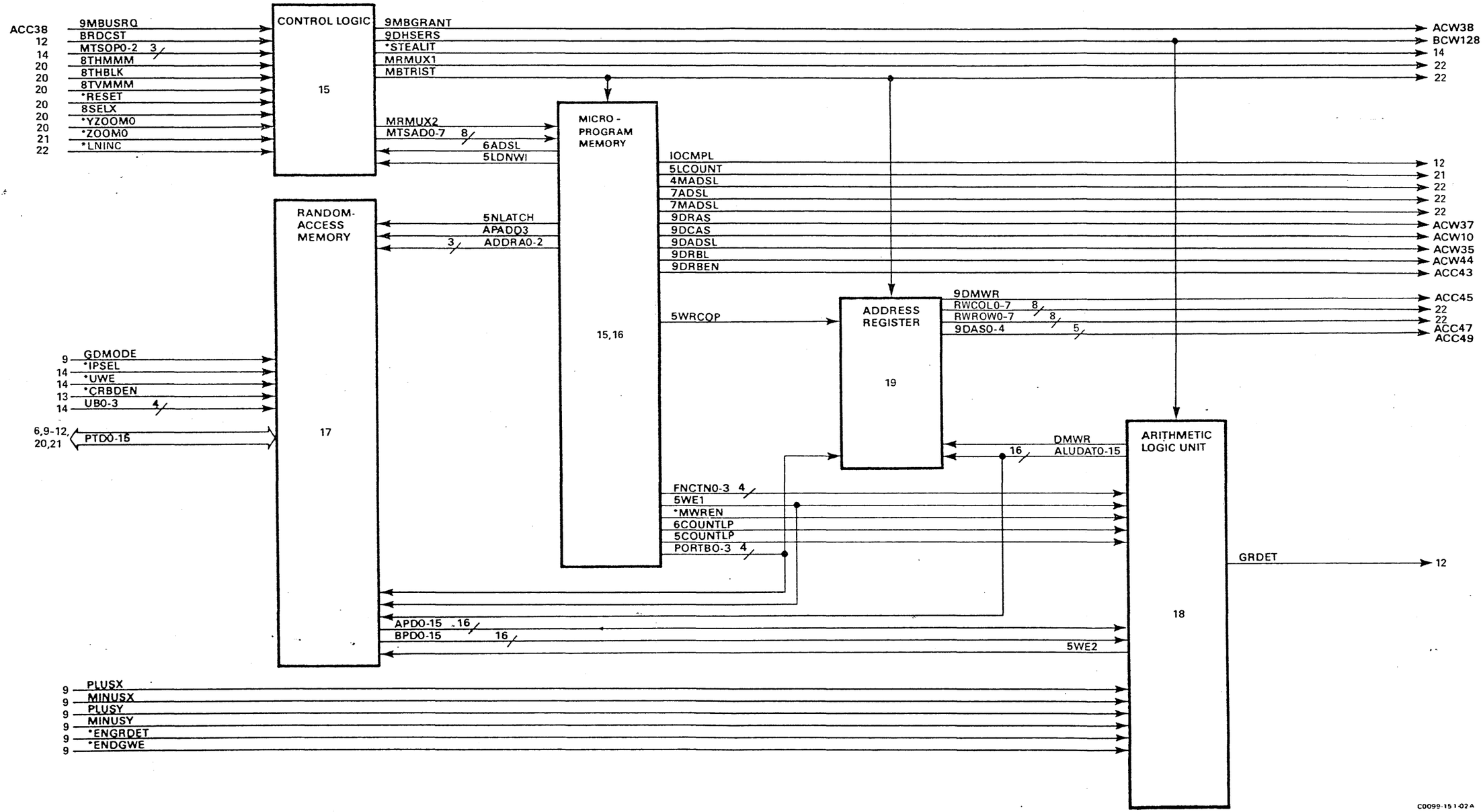


Figure F04-16. MTS

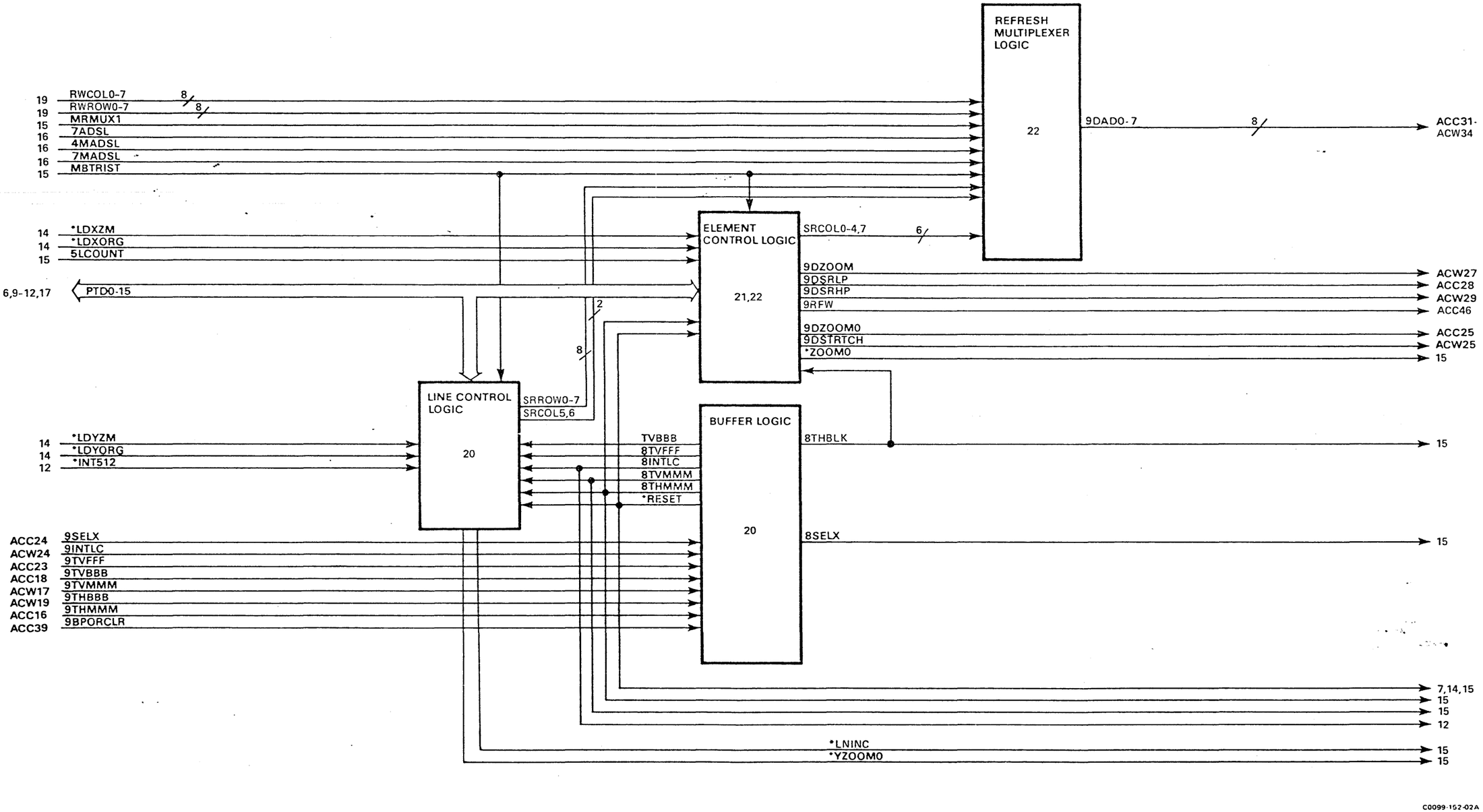


Figure F04-17. ZPR Logic

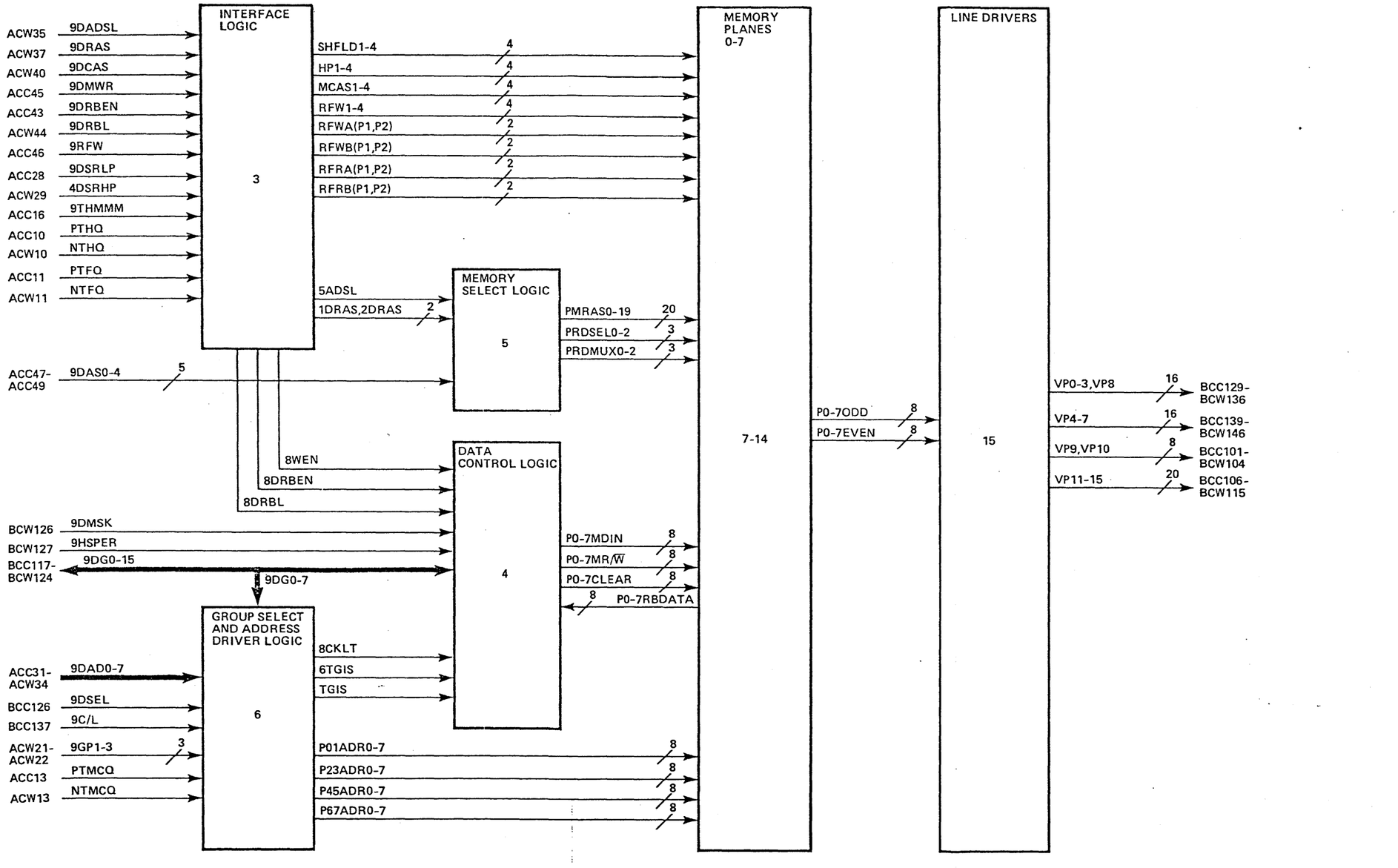


Figure F04-18. Memory PCB

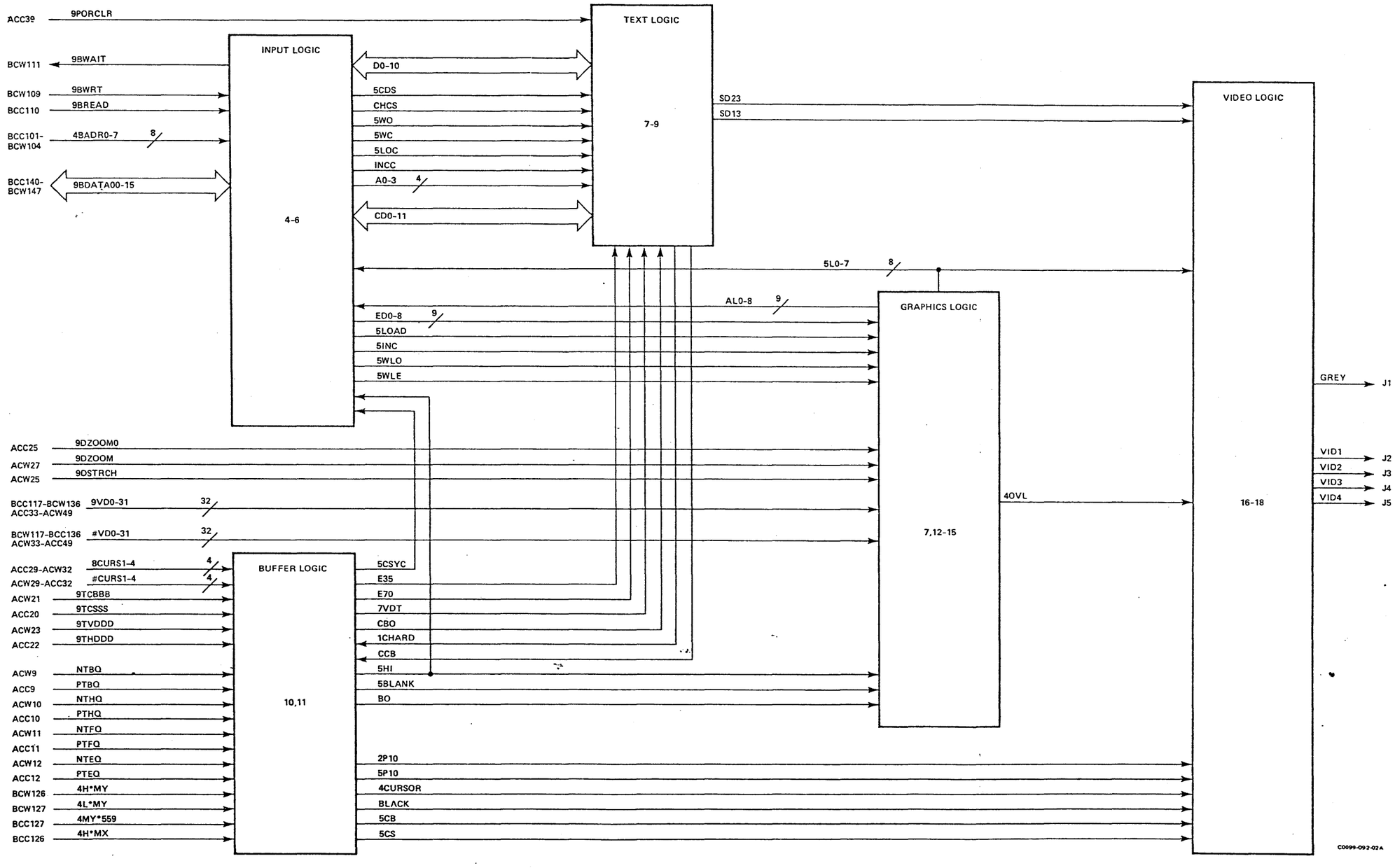


Figure F04-19. Video 12 PCB

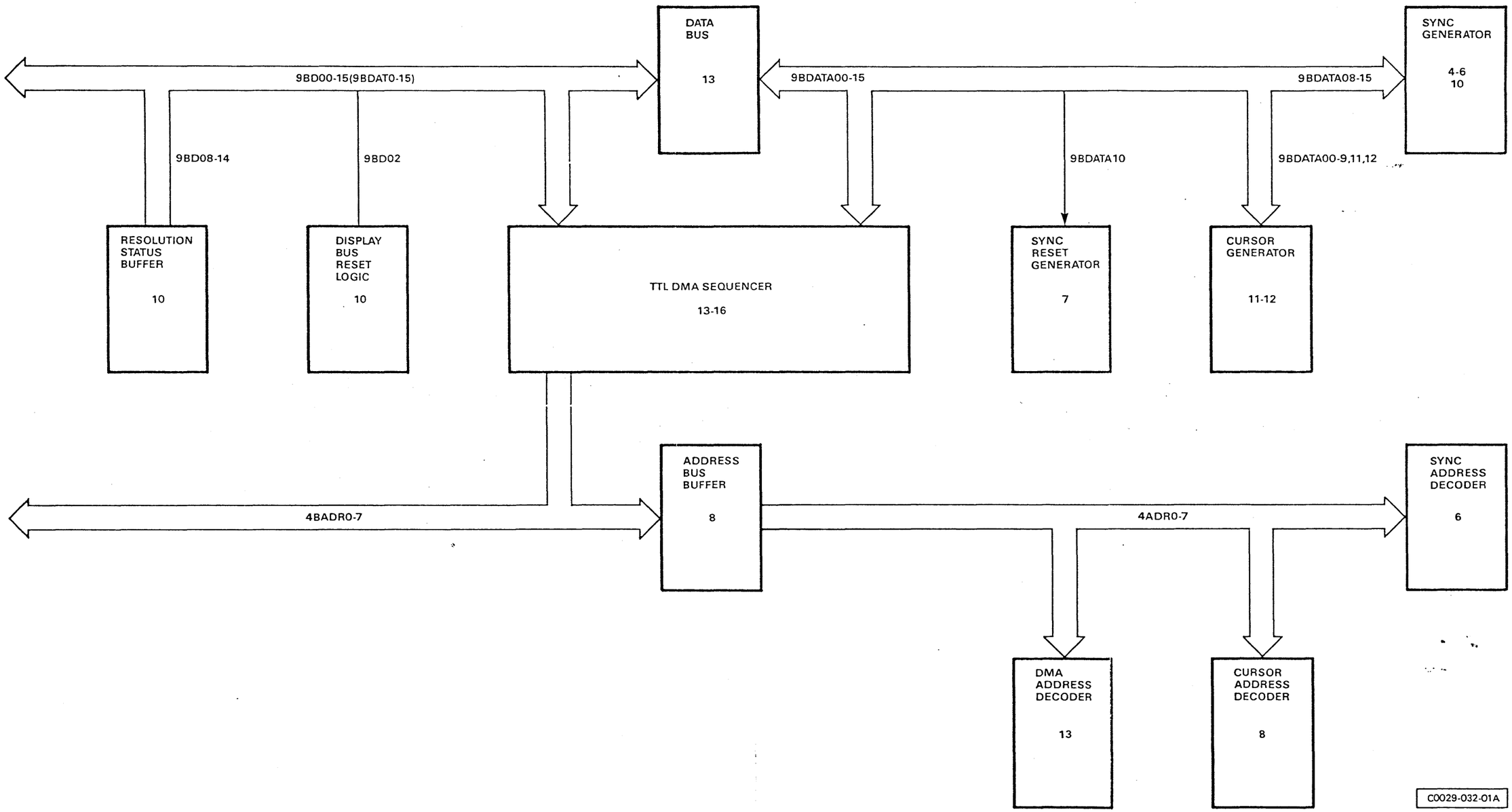


Figure F04-20. Sync PCB (Sheet 1 of 3)

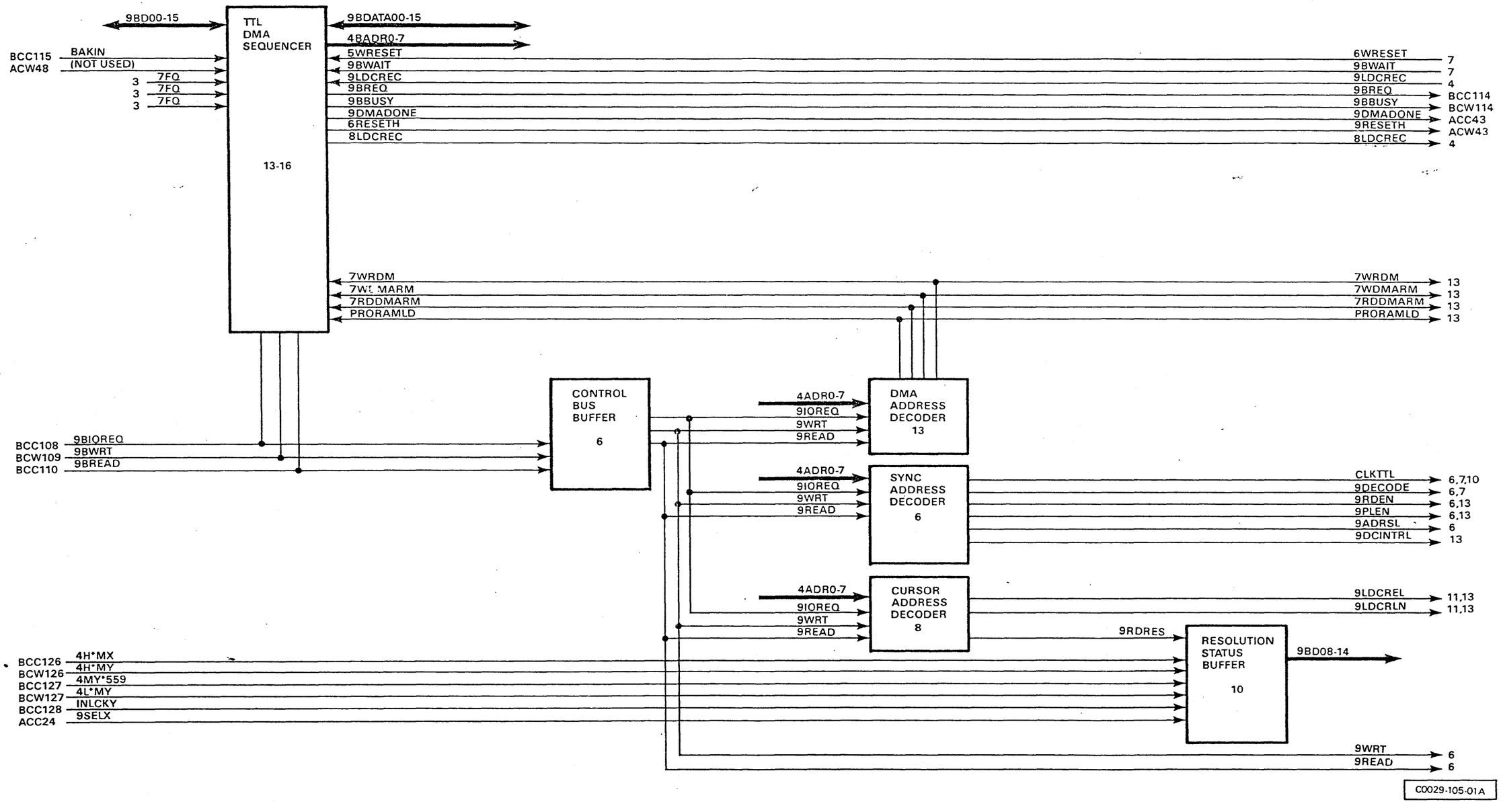


Figure F04-20. Sync PCB (Sheet 2 of 3)

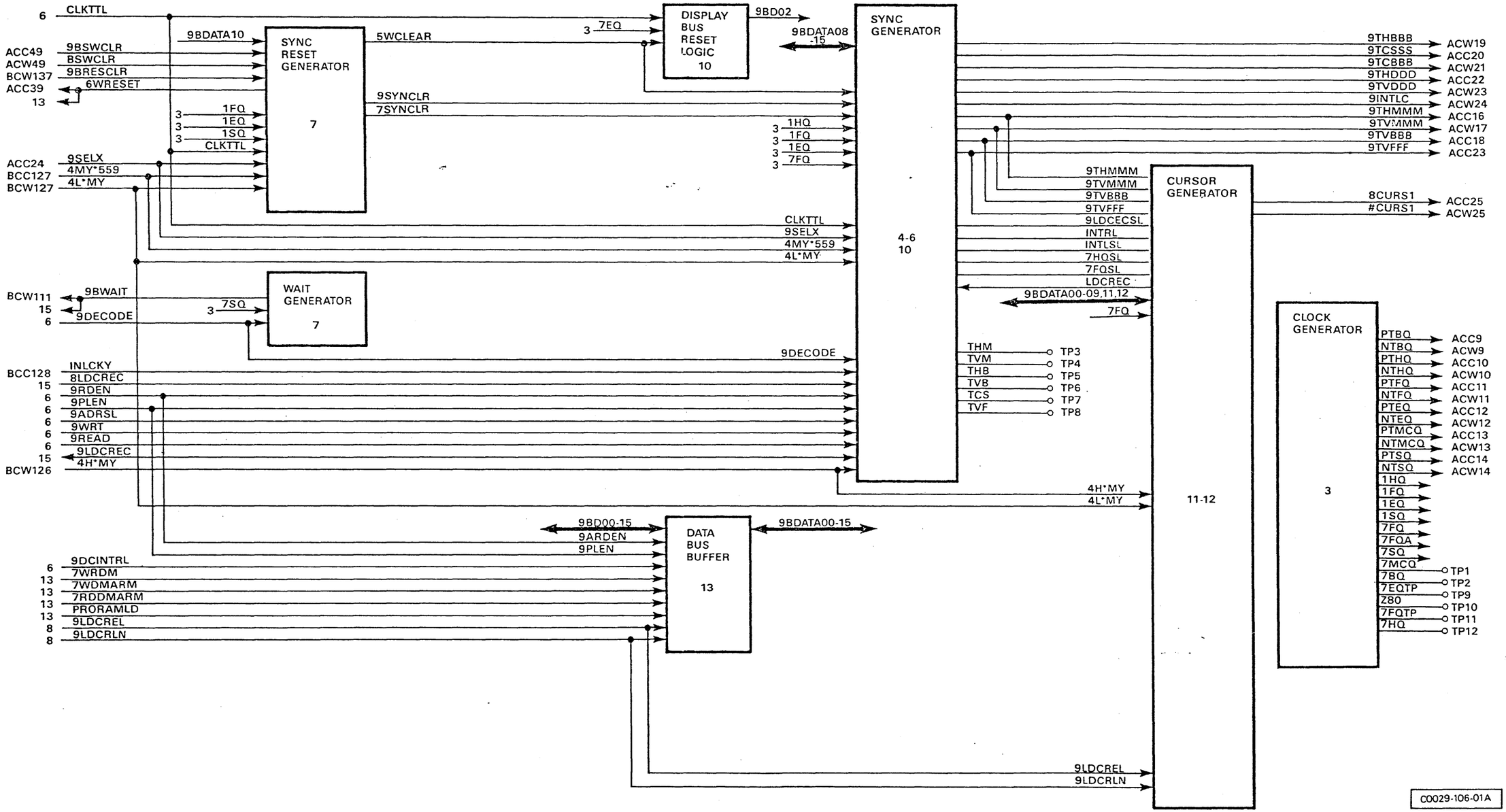


Figure F04-20. Sync PCB (Sheet 3 of 3)

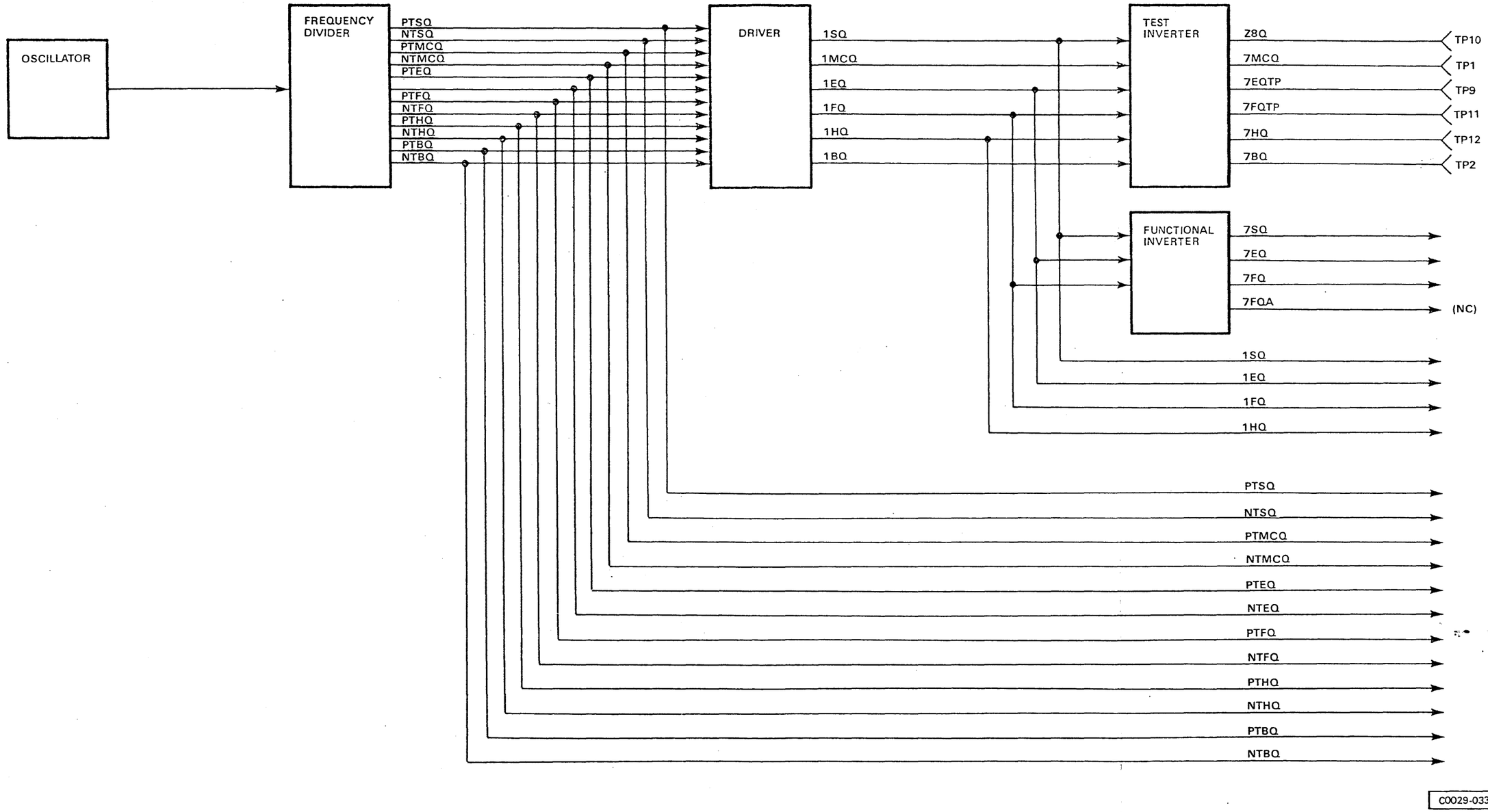


Figure F04-21. Clock Generator

8000110-01A

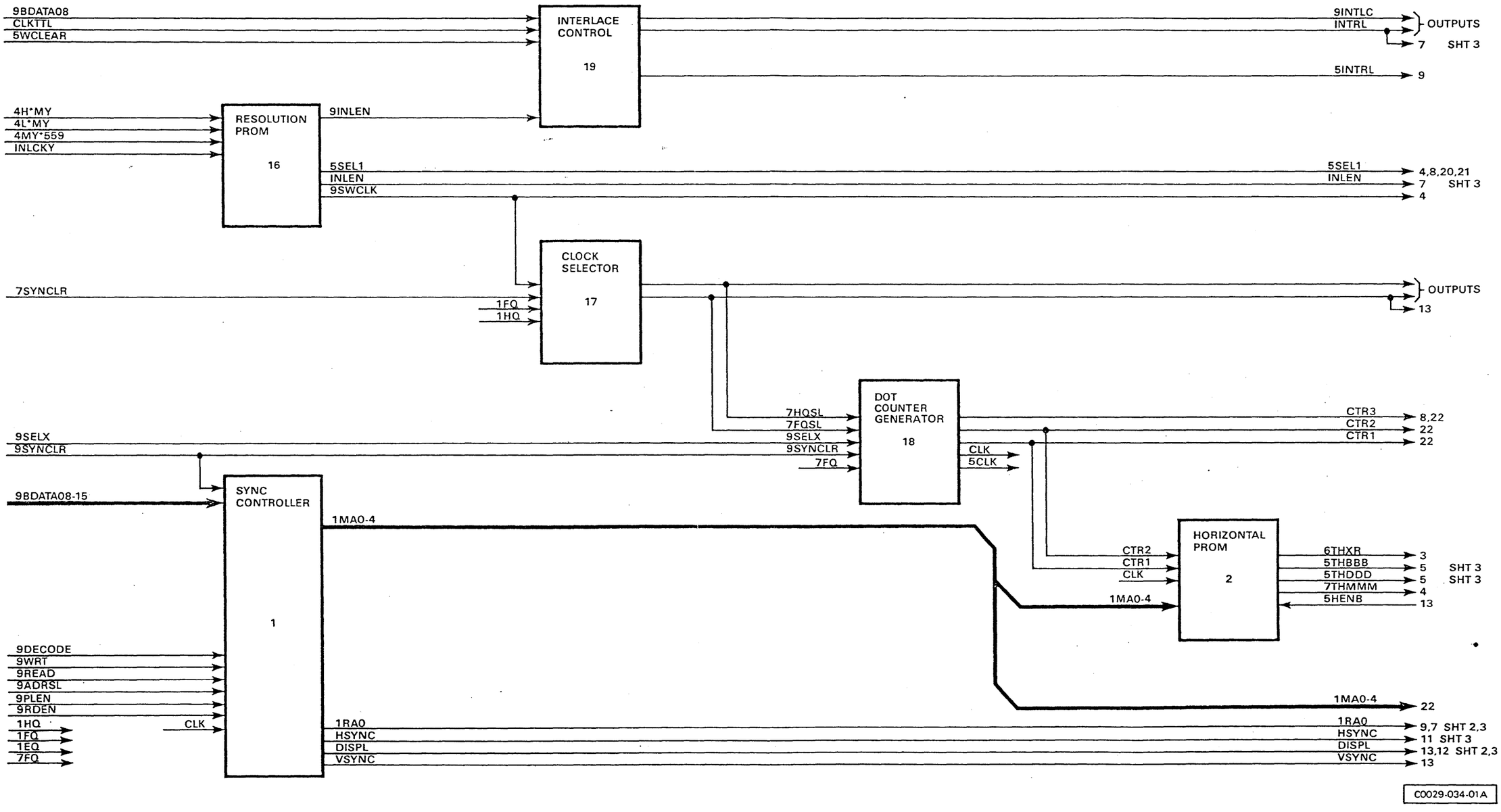


Figure F04-22. Sync Generator (Sheet 1 of 3)

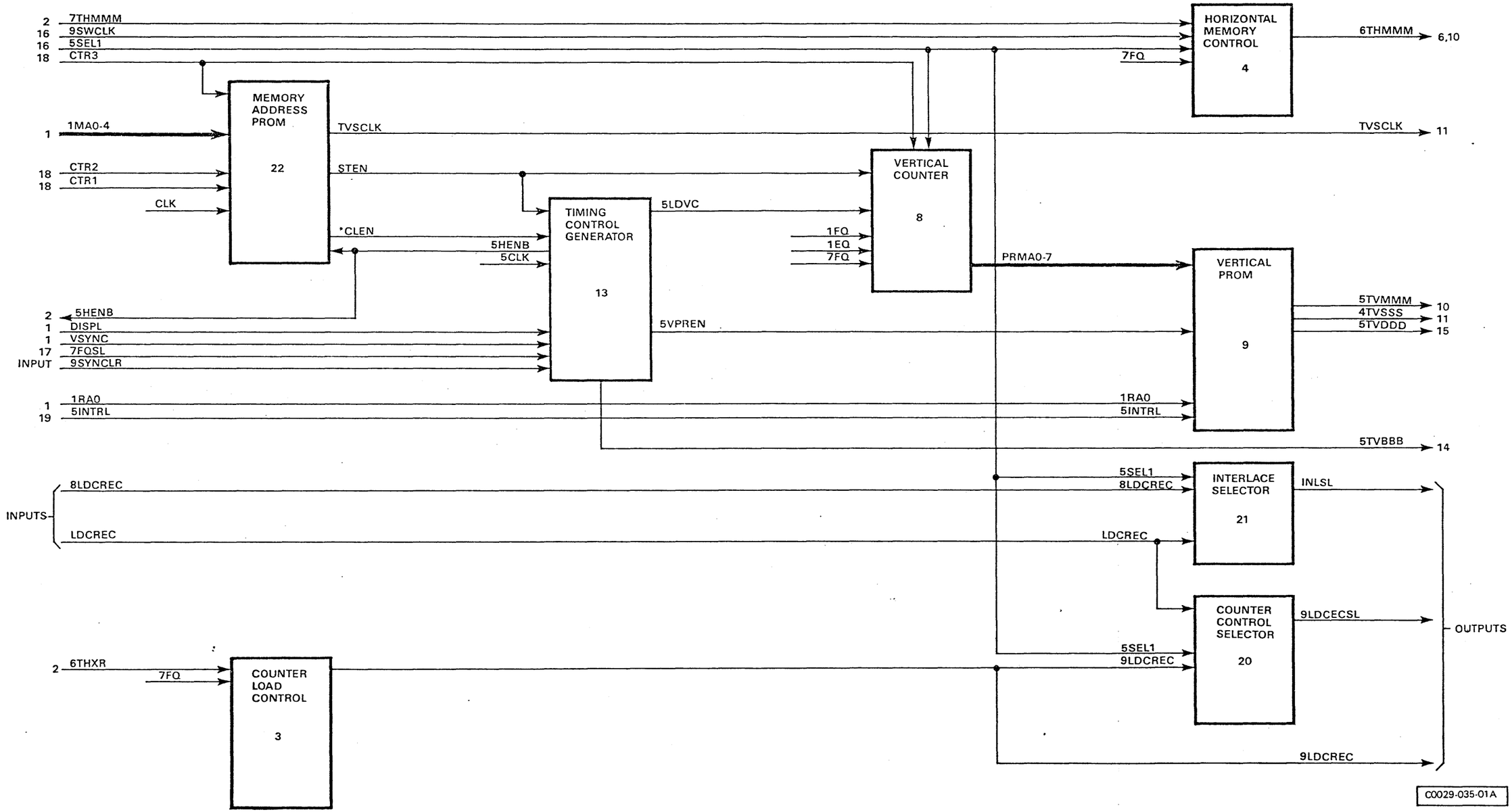


Figure F04-22. Sync Generator
(Sheet 2 of 3)

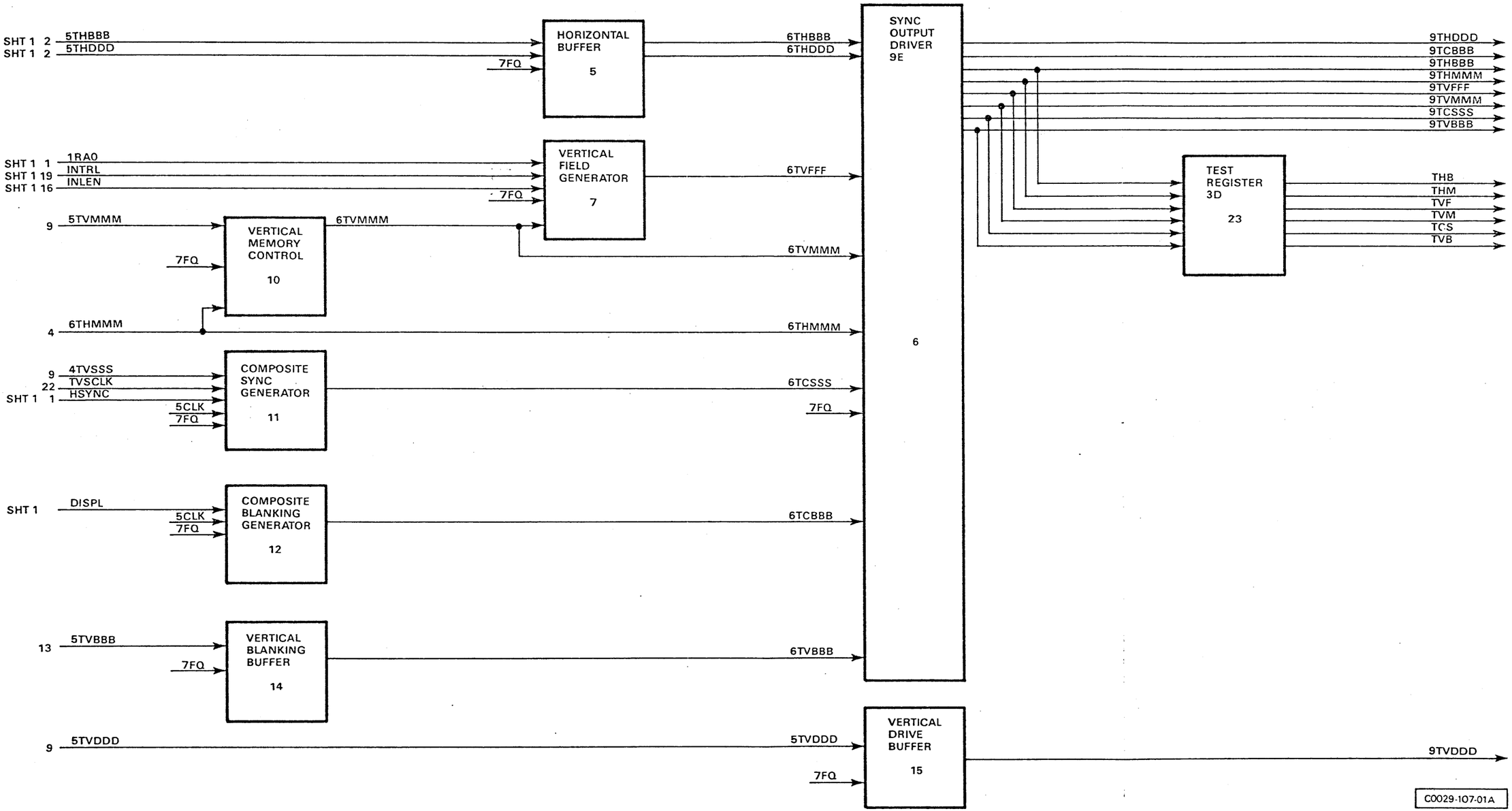


Figure F04-22. Sync Generator (Sheet 3 of 3)

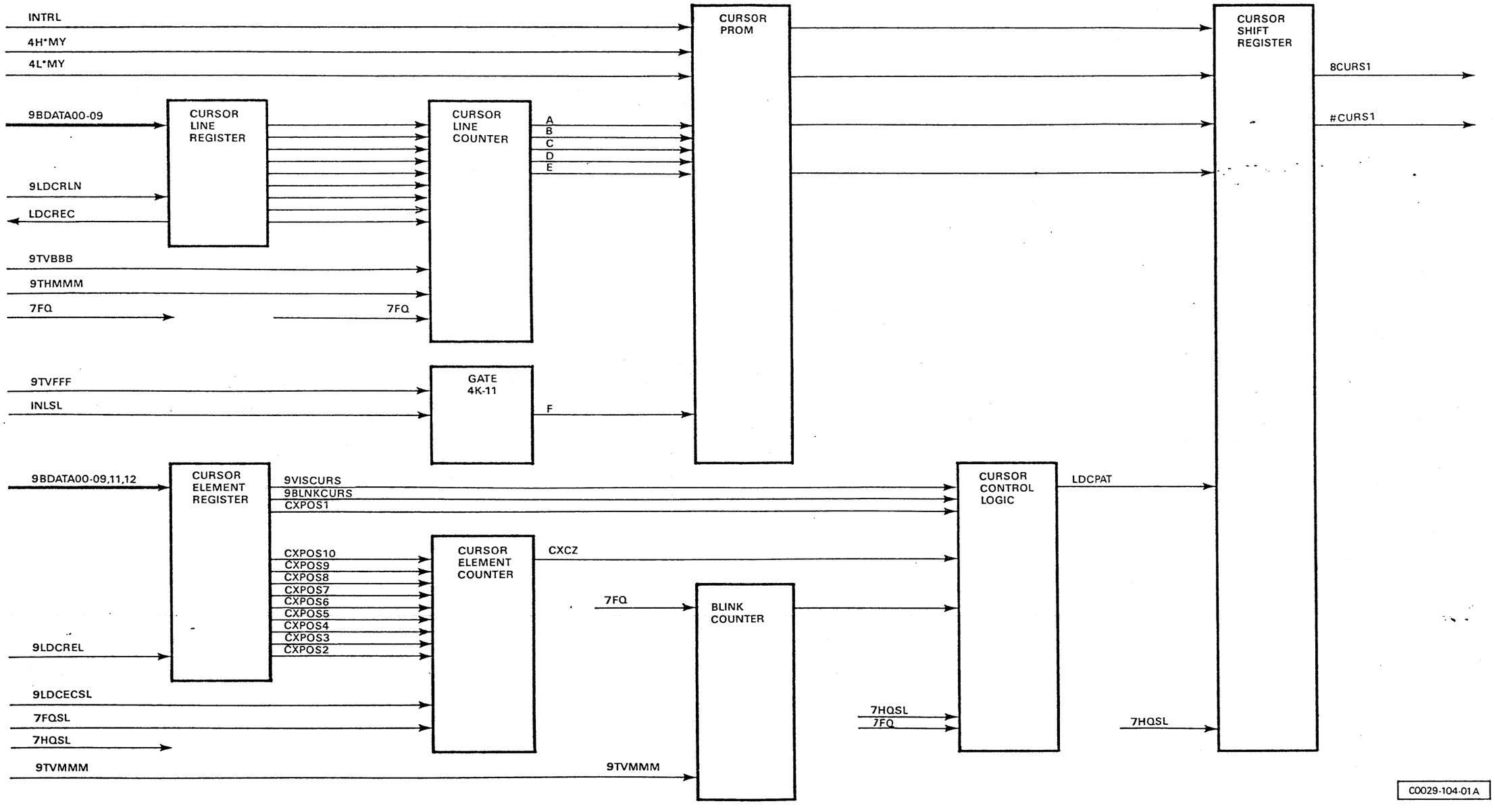


Figure F04-23. Cursor Generator

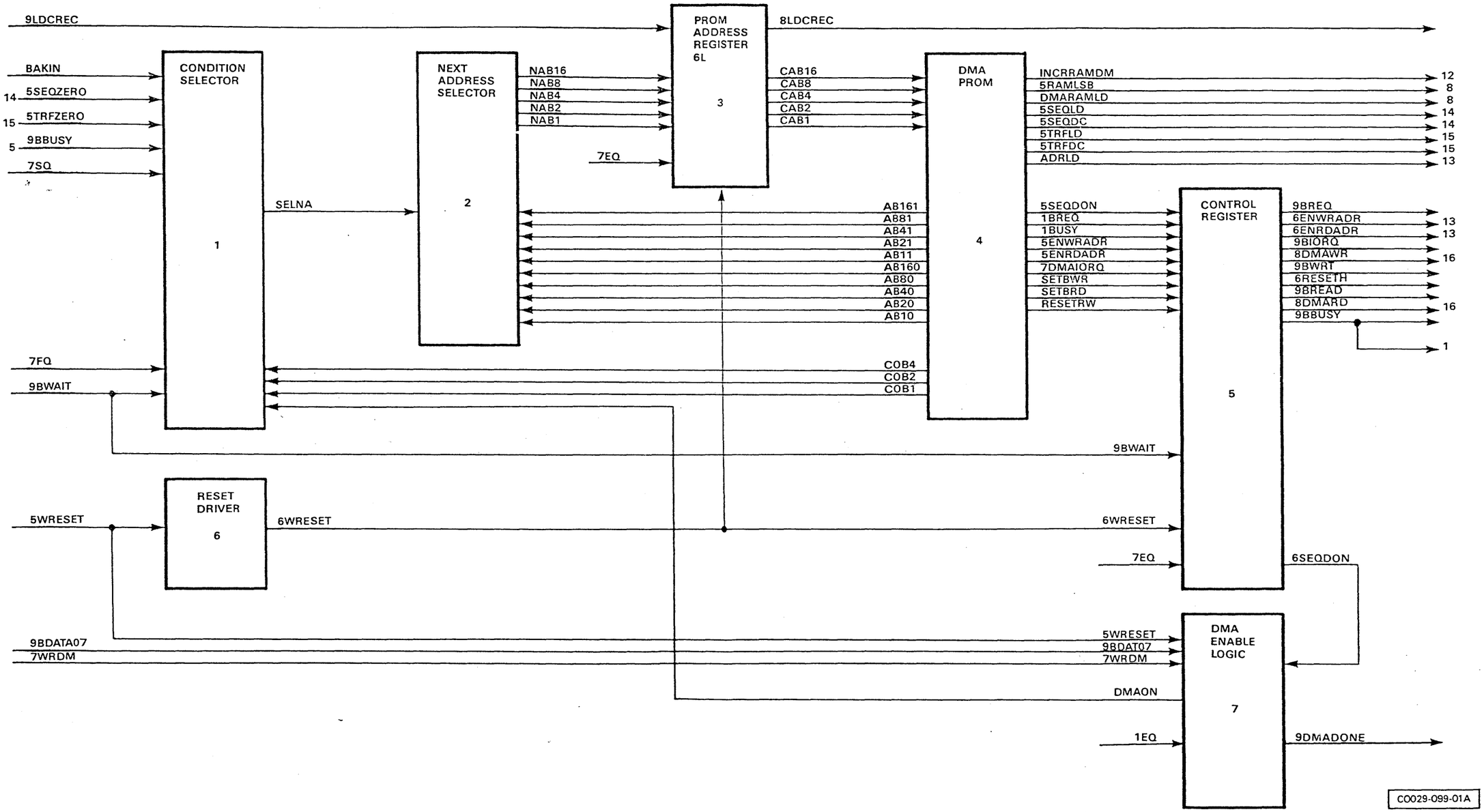


Figure FO4-24. TTL DMA (Sheet 1 of 2)

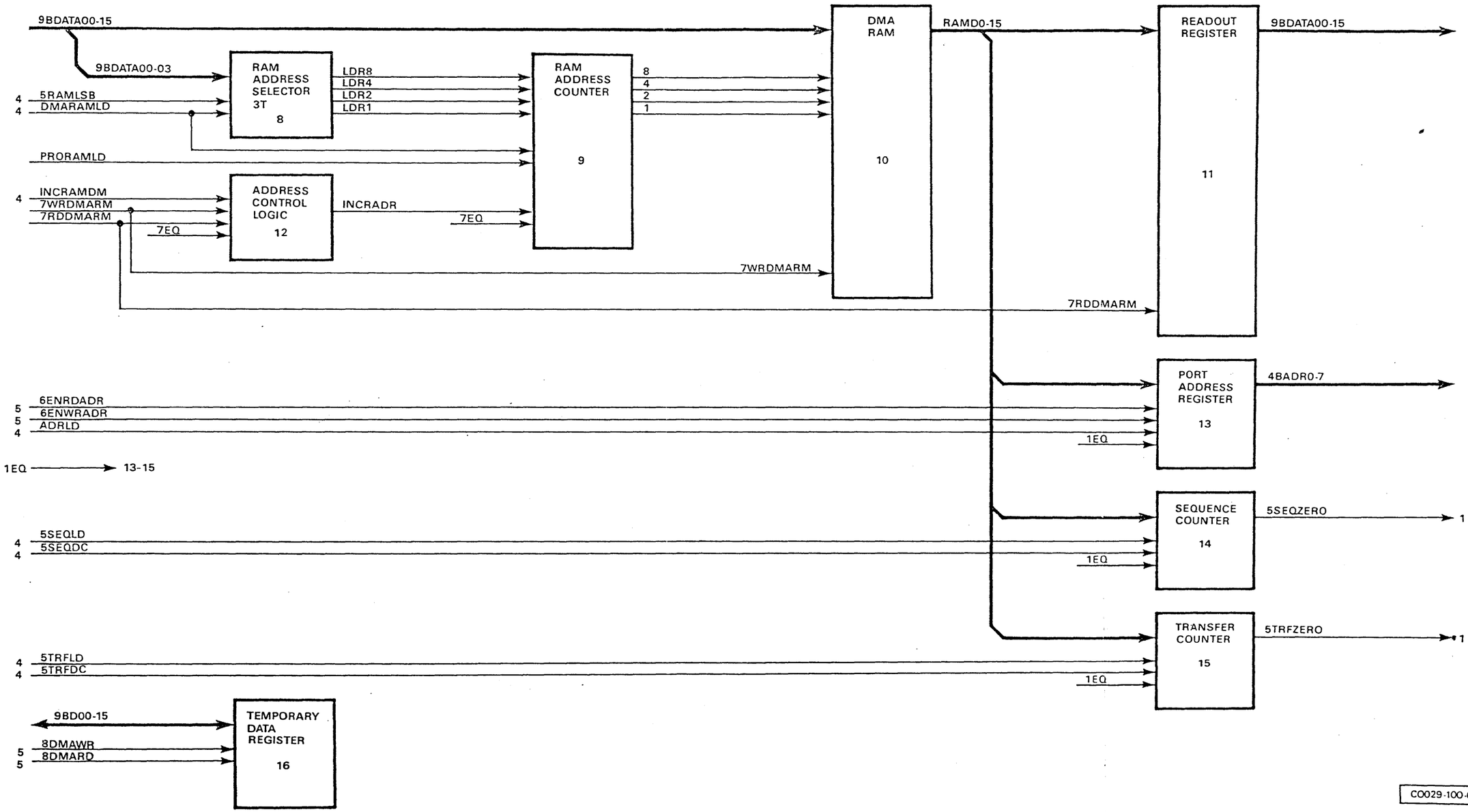


Figure F04-24. TTL DMA (Sheet 2 of 2)

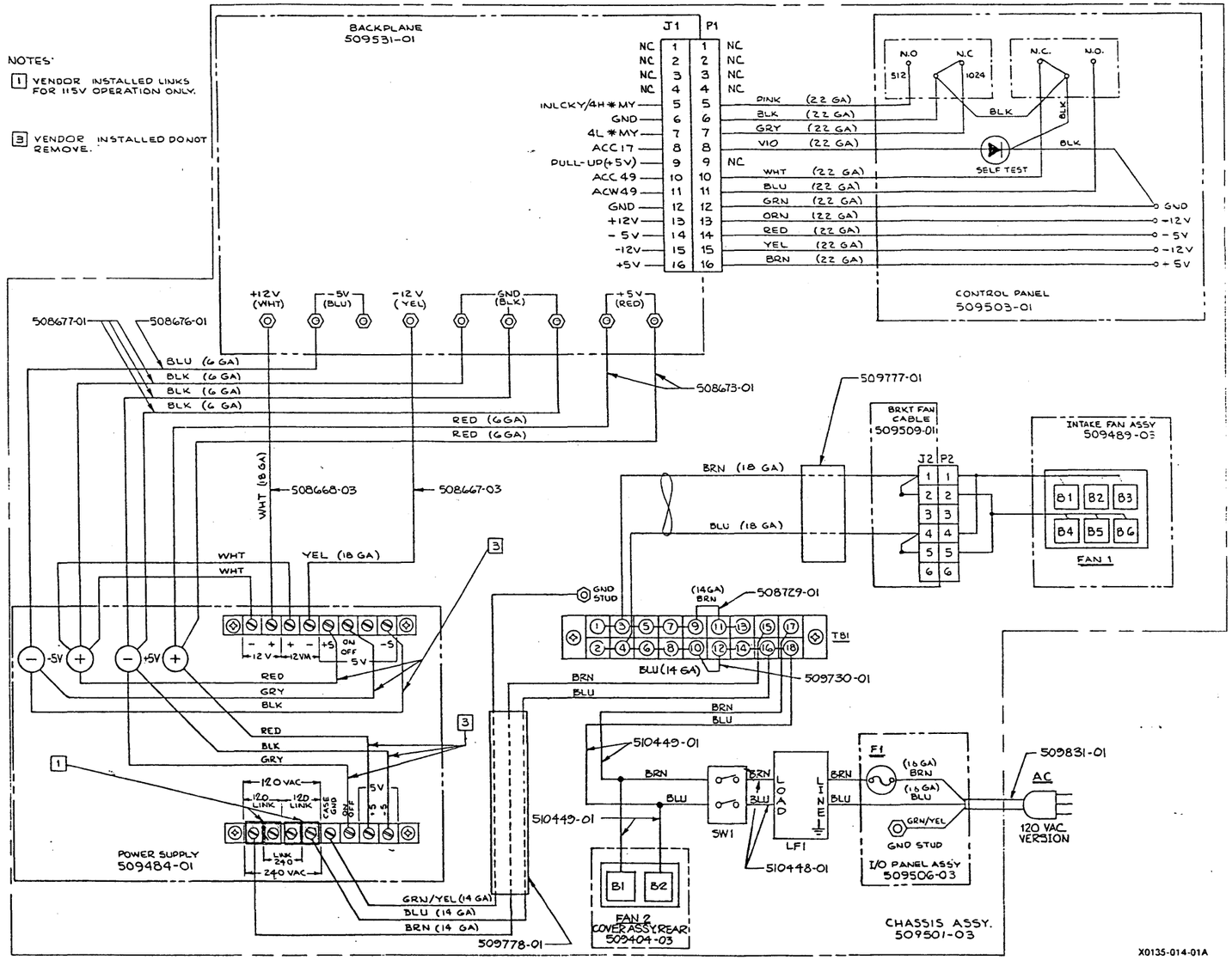


Figure F04-25. Power Distribution - 120v

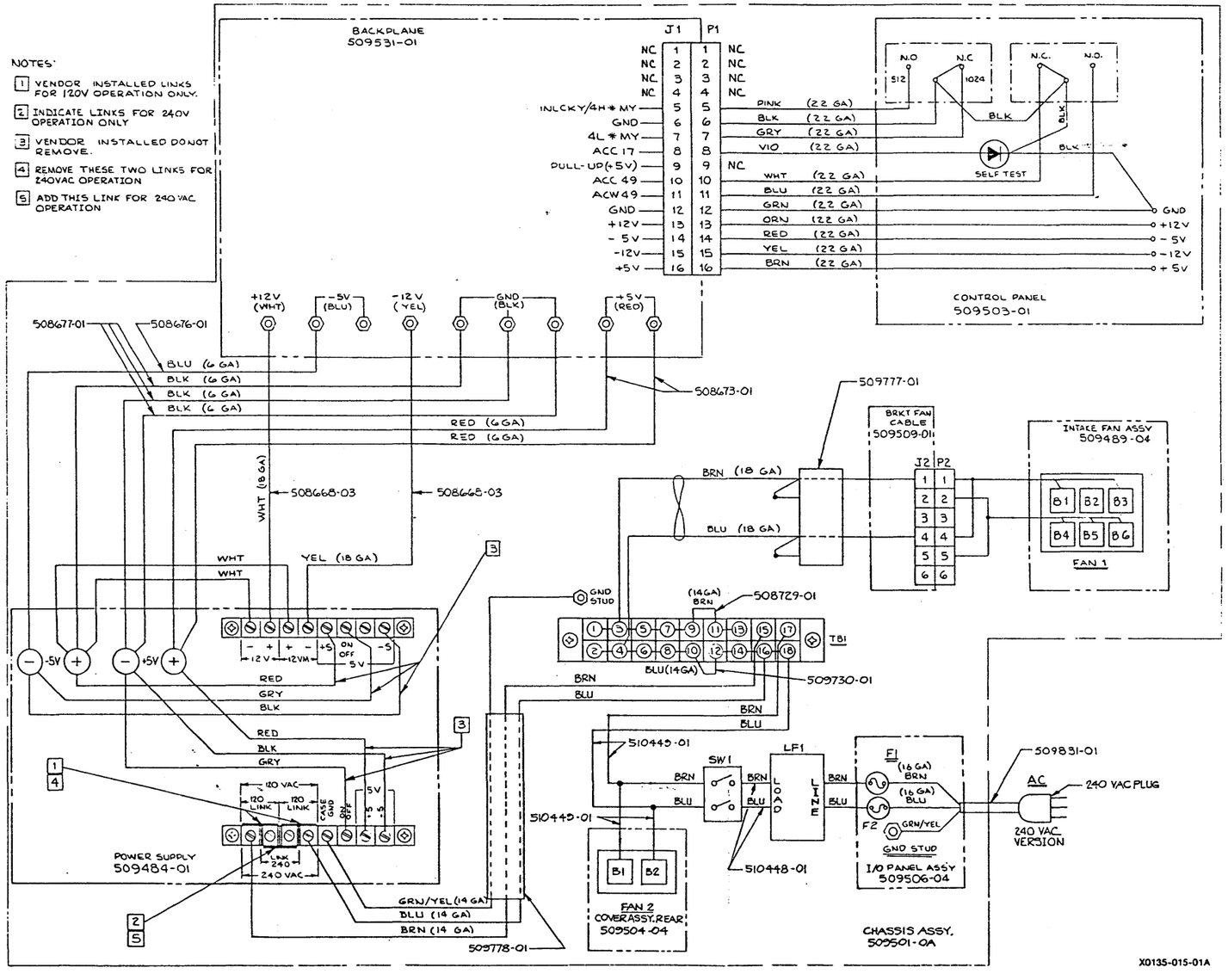


Figure F04-26. Power Distribution - 240v

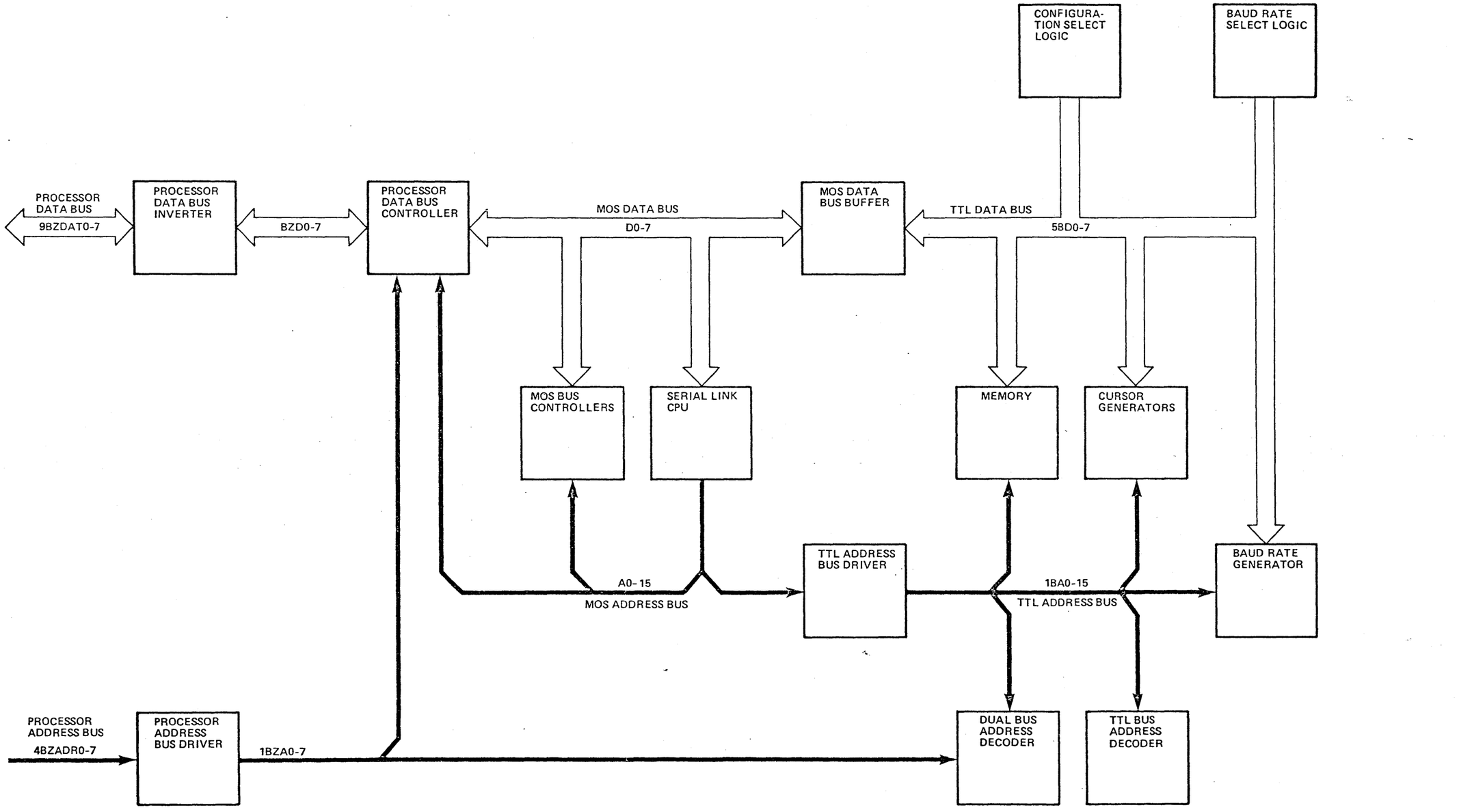


Figure F04-27. Serial Link PCB Data and Address Buses

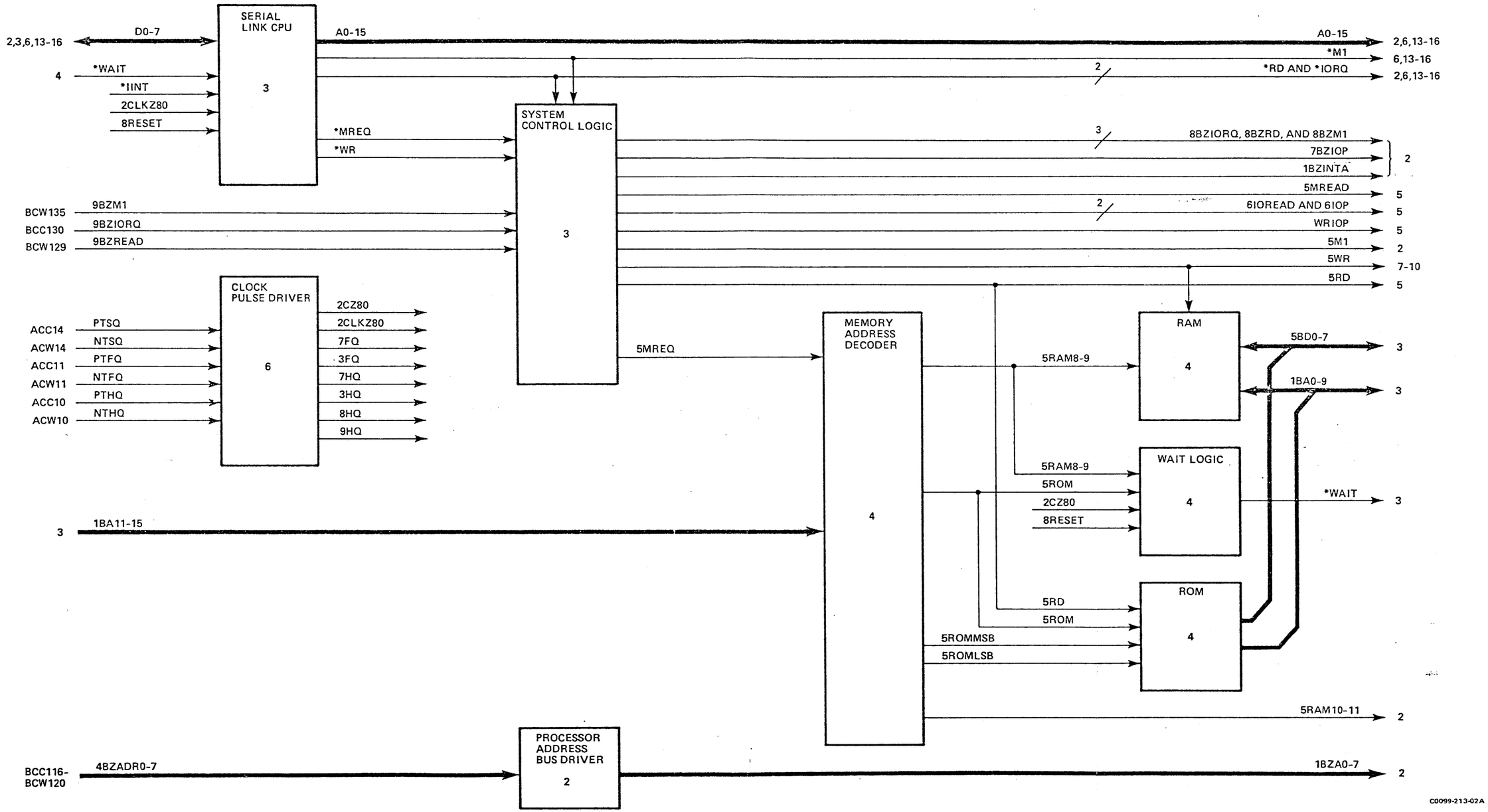


Figure F04-28. Serial Link PCB Control Signals (Sheet 1 of 5)

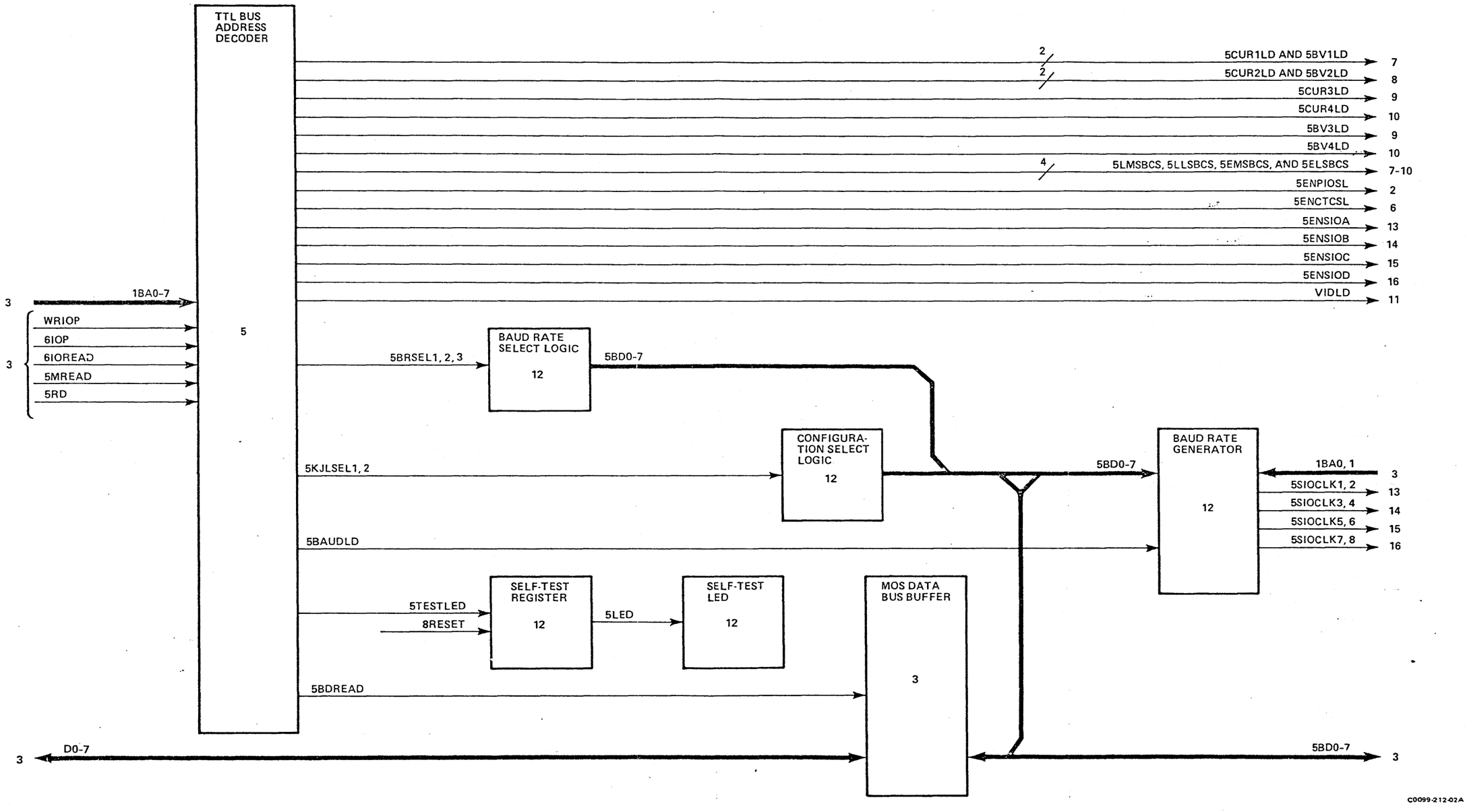


Figure F04-28. Serial Link PCB Control Signals (Sheet 2 of 5)

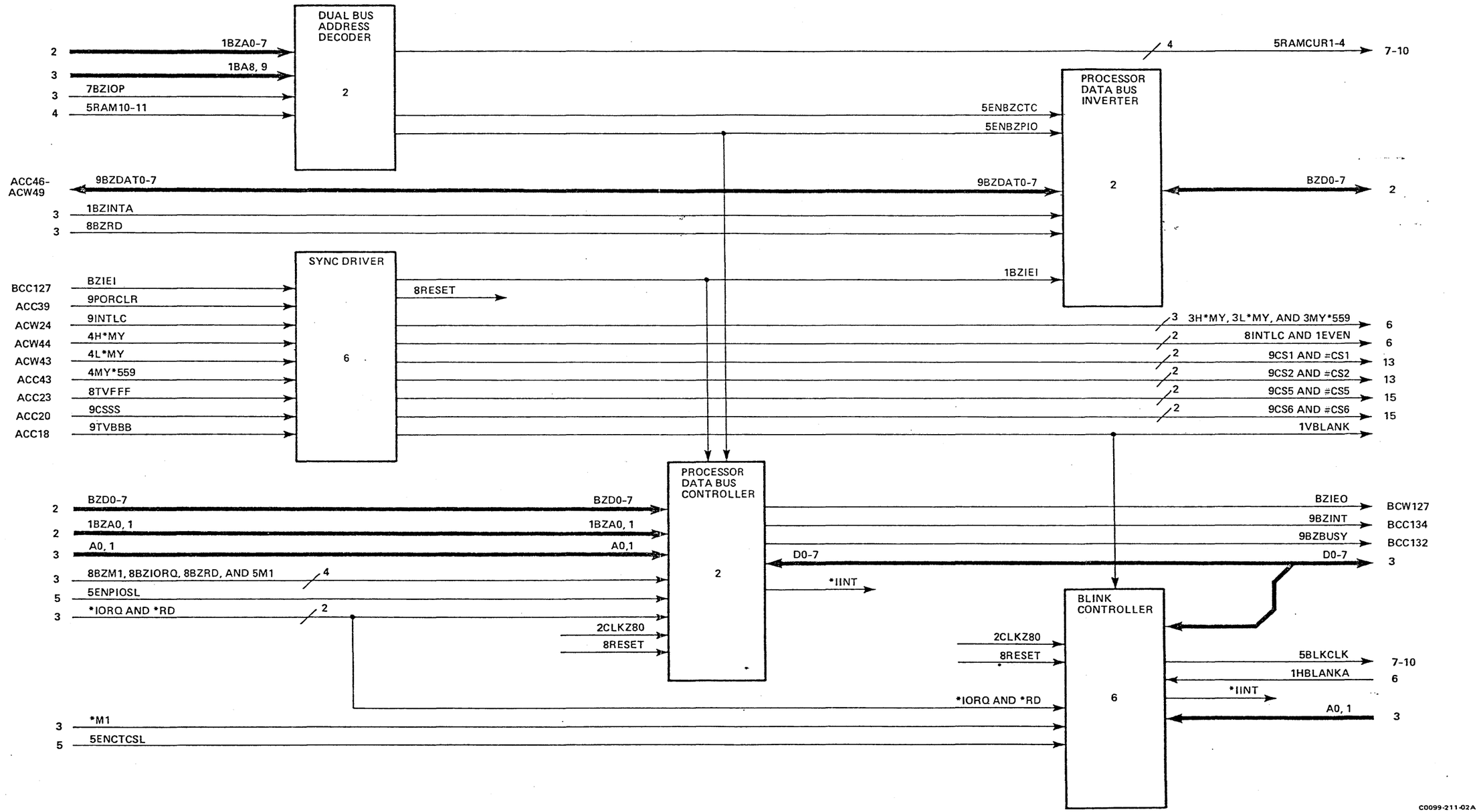
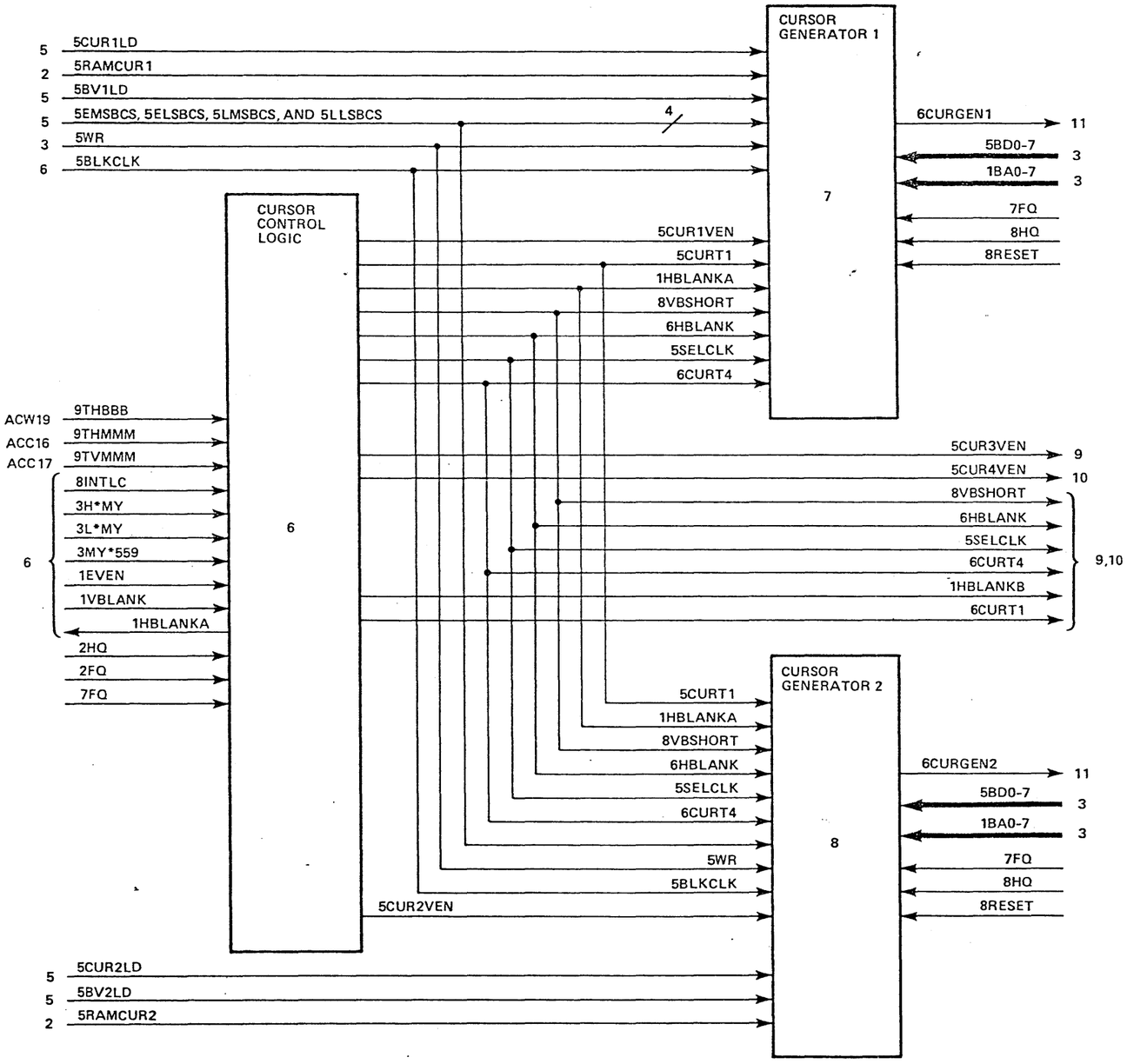
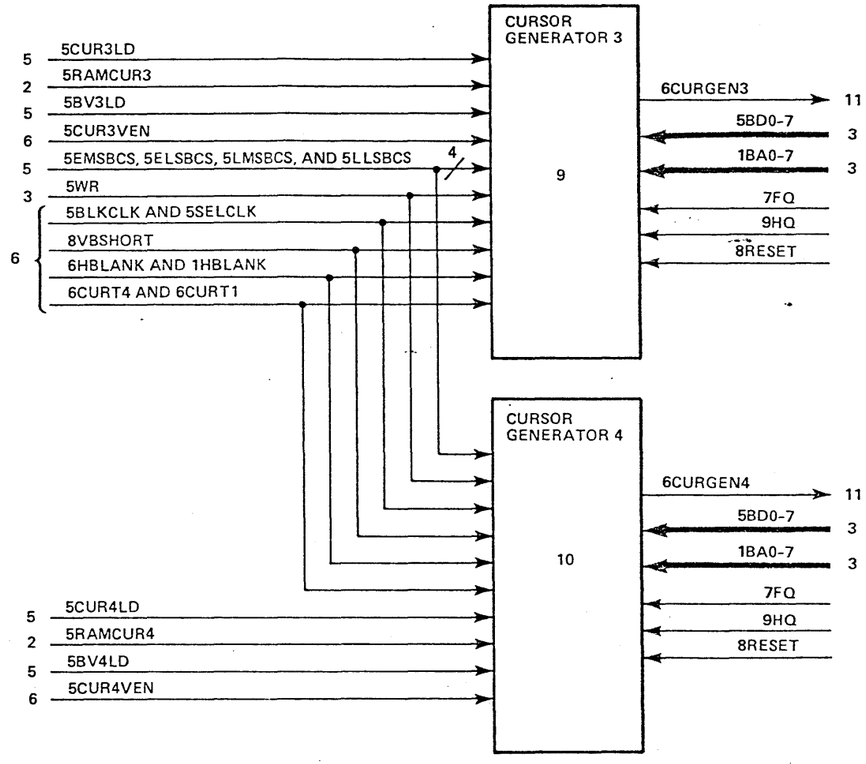


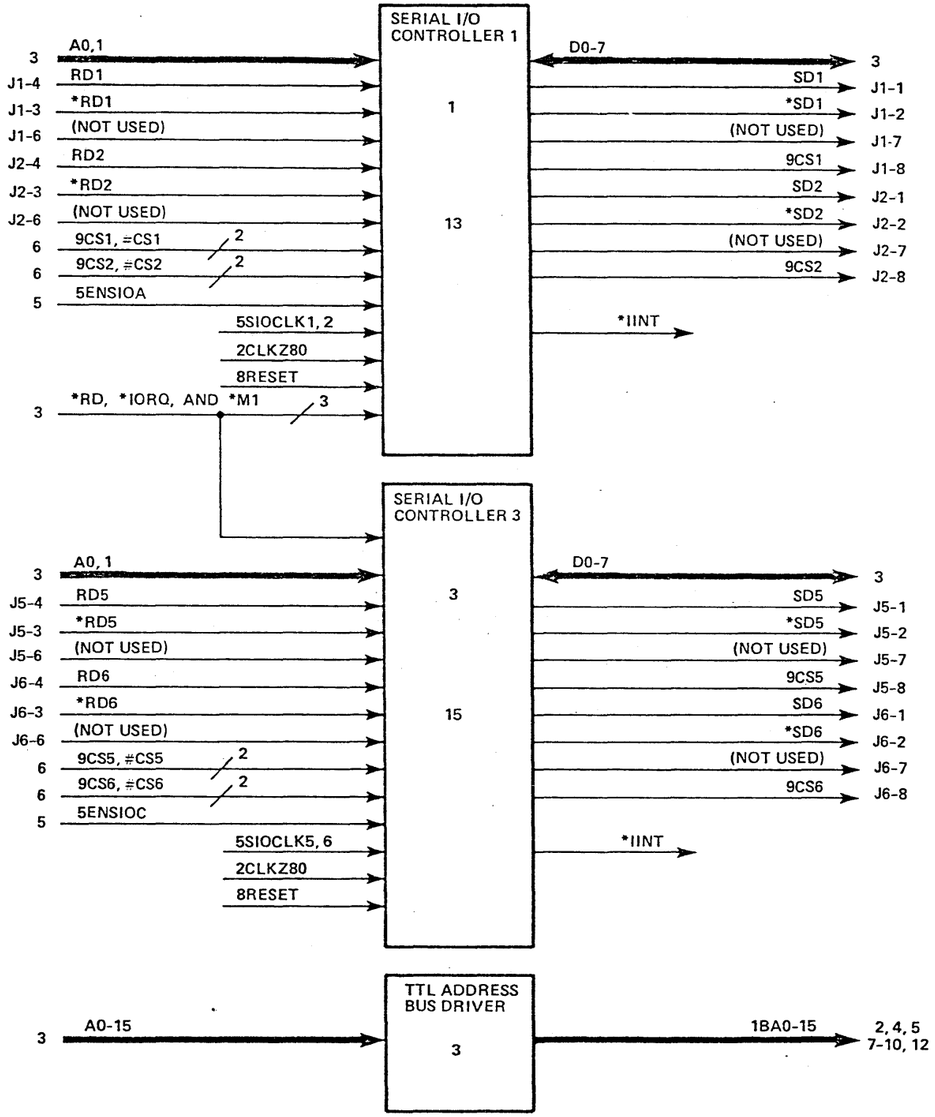
Figure FO4-28. Serial Link PCB Control Signals (Sheet 3 of 5)

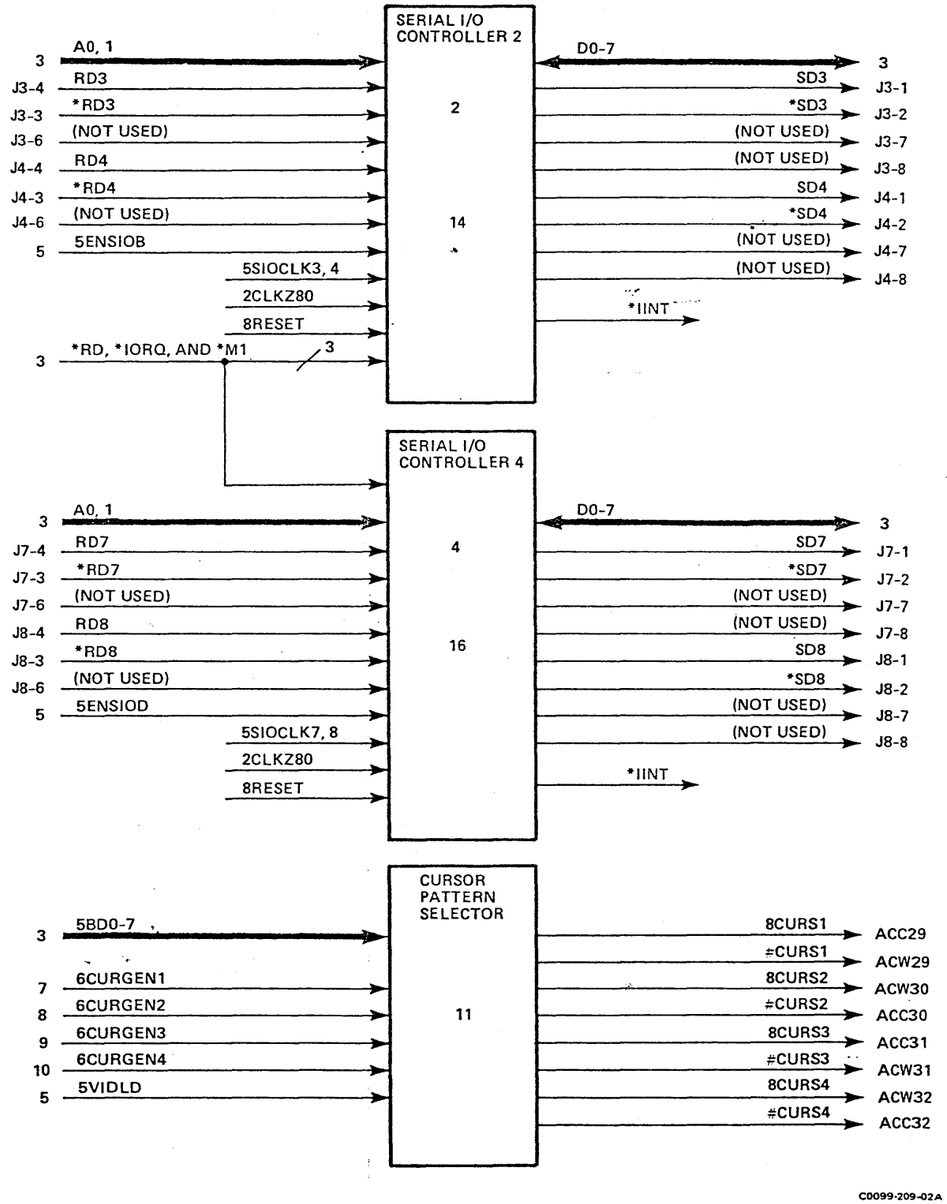




C0099-210-02A

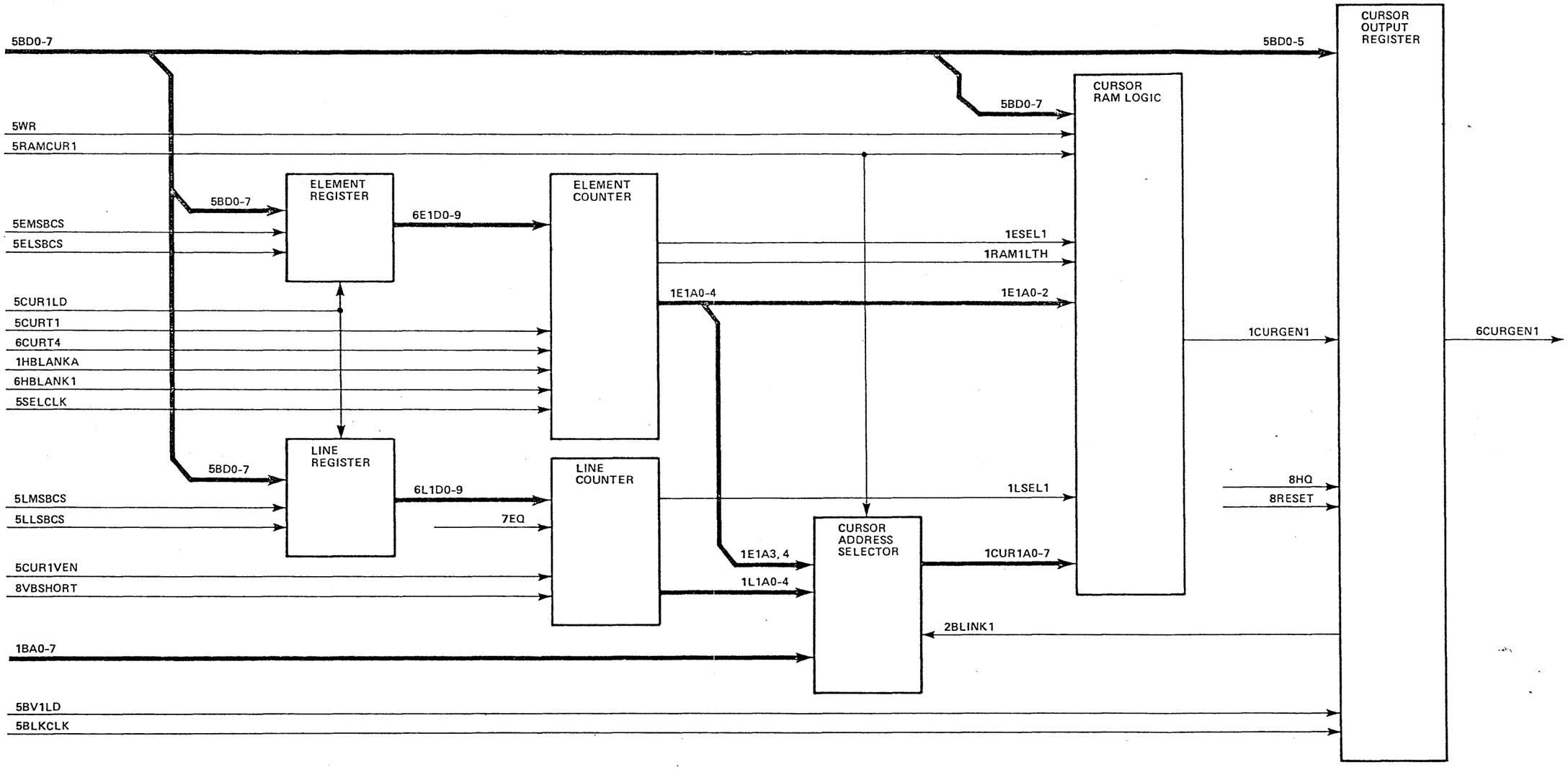
Figure FO4-28. Serial Link PCB Control Signals (Sheet 4 of 5)





C0099-209-02A

Figure F04-28. Serial Link PCB Control Signals (Sheet 5 of 5)



C0099-208-02A

Figure F04-29. Cursor Generator

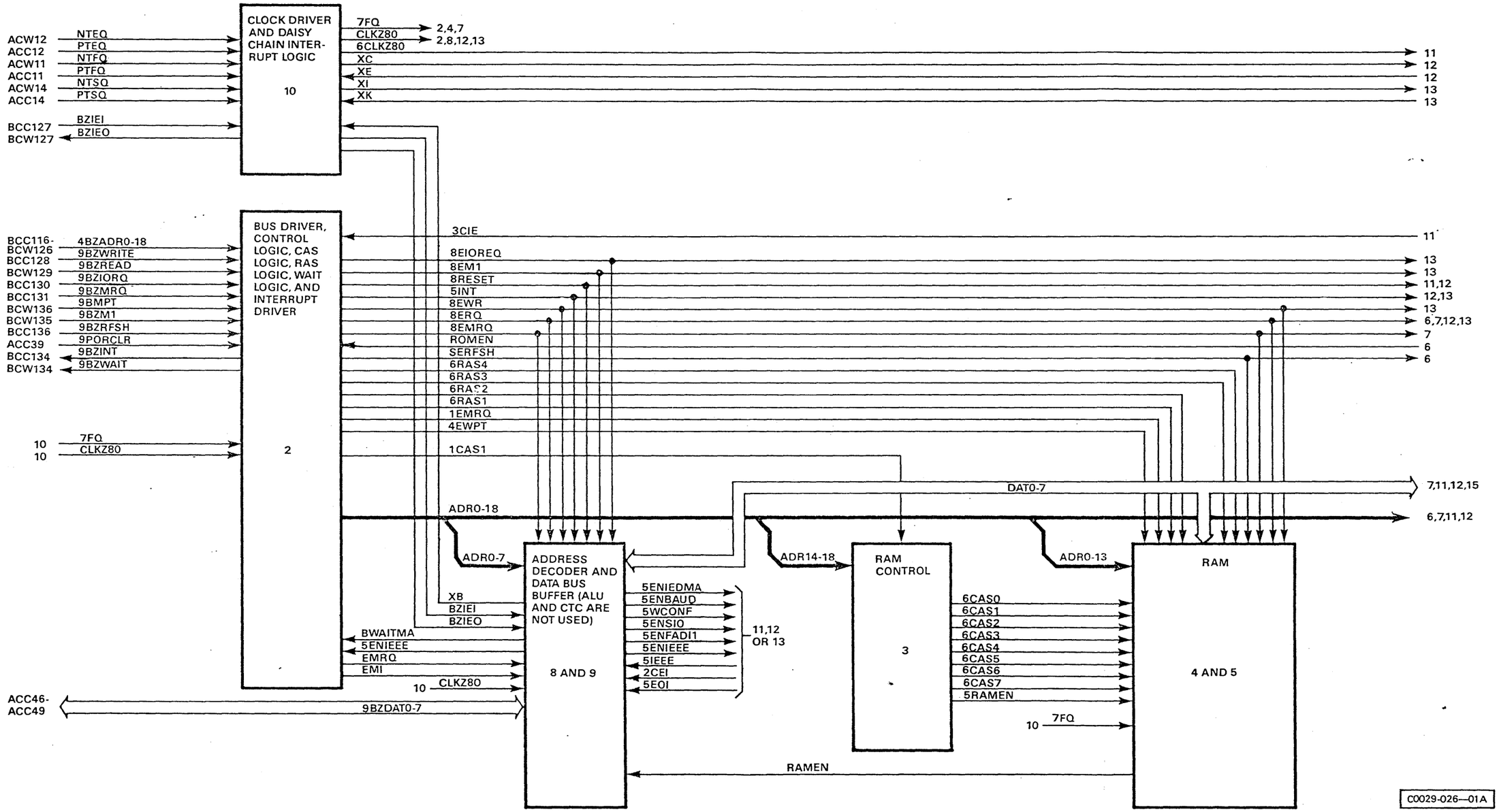


Figure F04-30. Expansion PCB (Sheet 1 of 2)

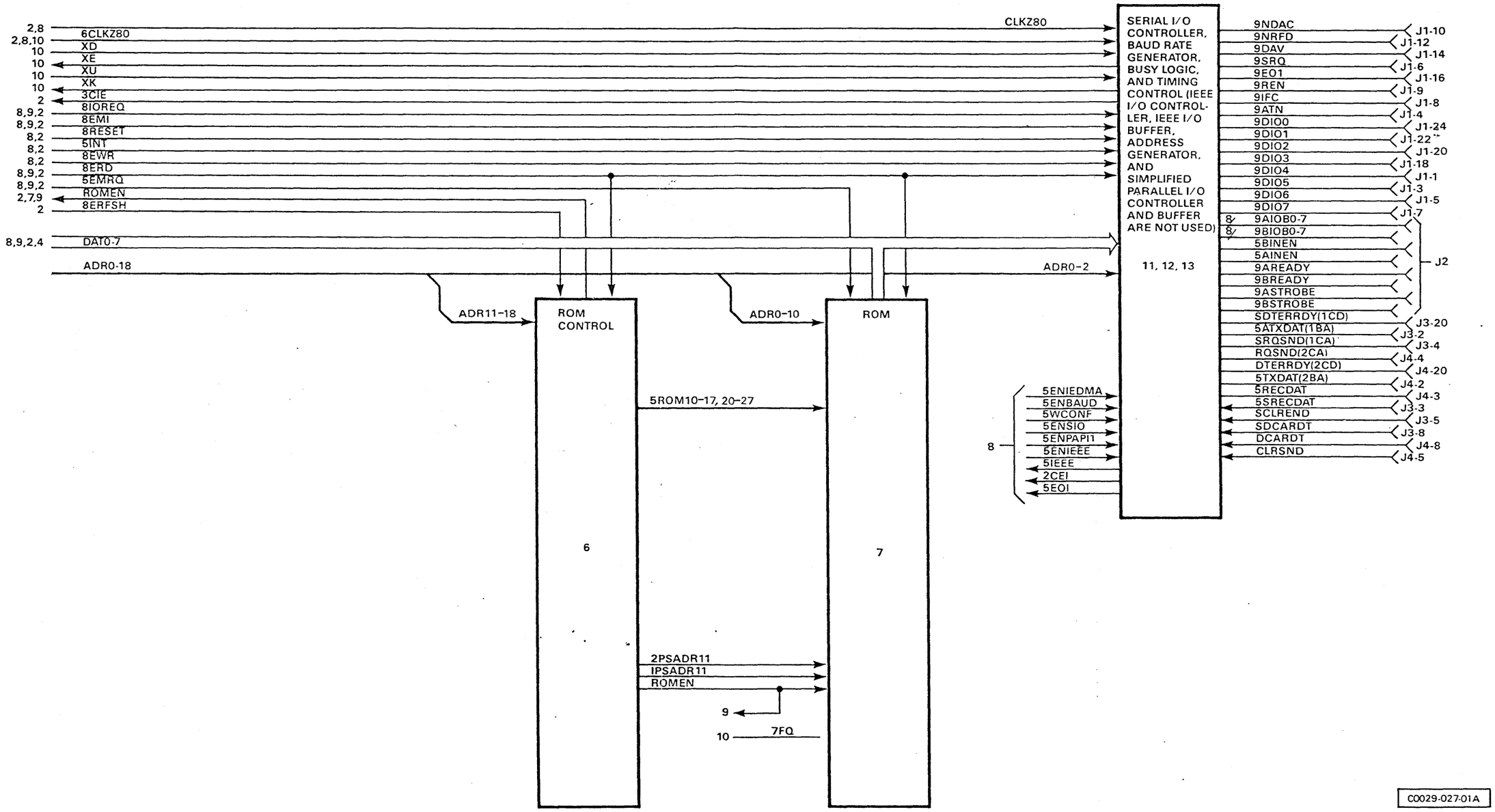


Figure F04-30. Expansion PCB (Sheet 2 of 2)

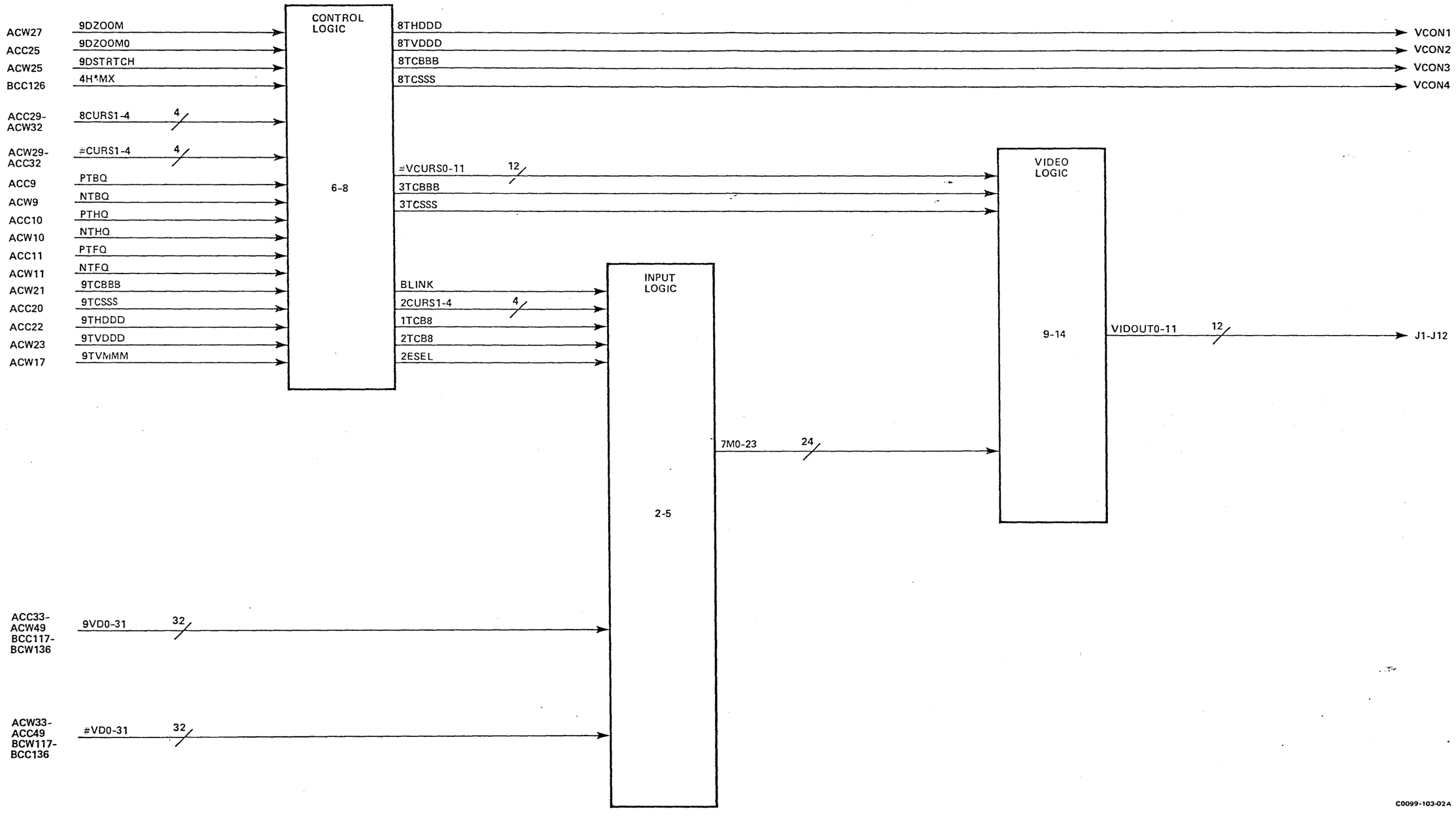


Figure F04-31. Video 1 PCB

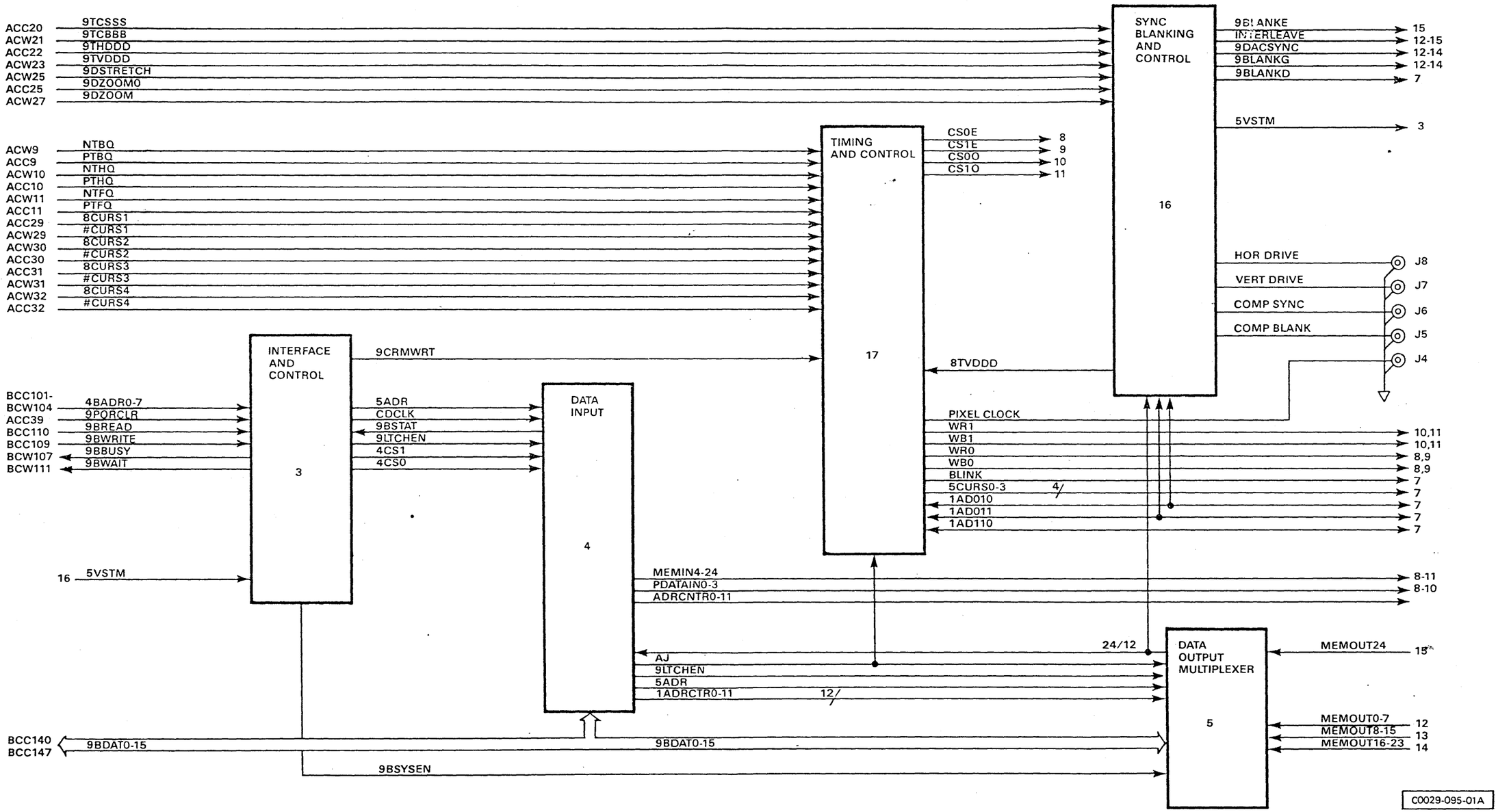


Figure F04-32. Video 7 PCB (Sheet 1 of 2)

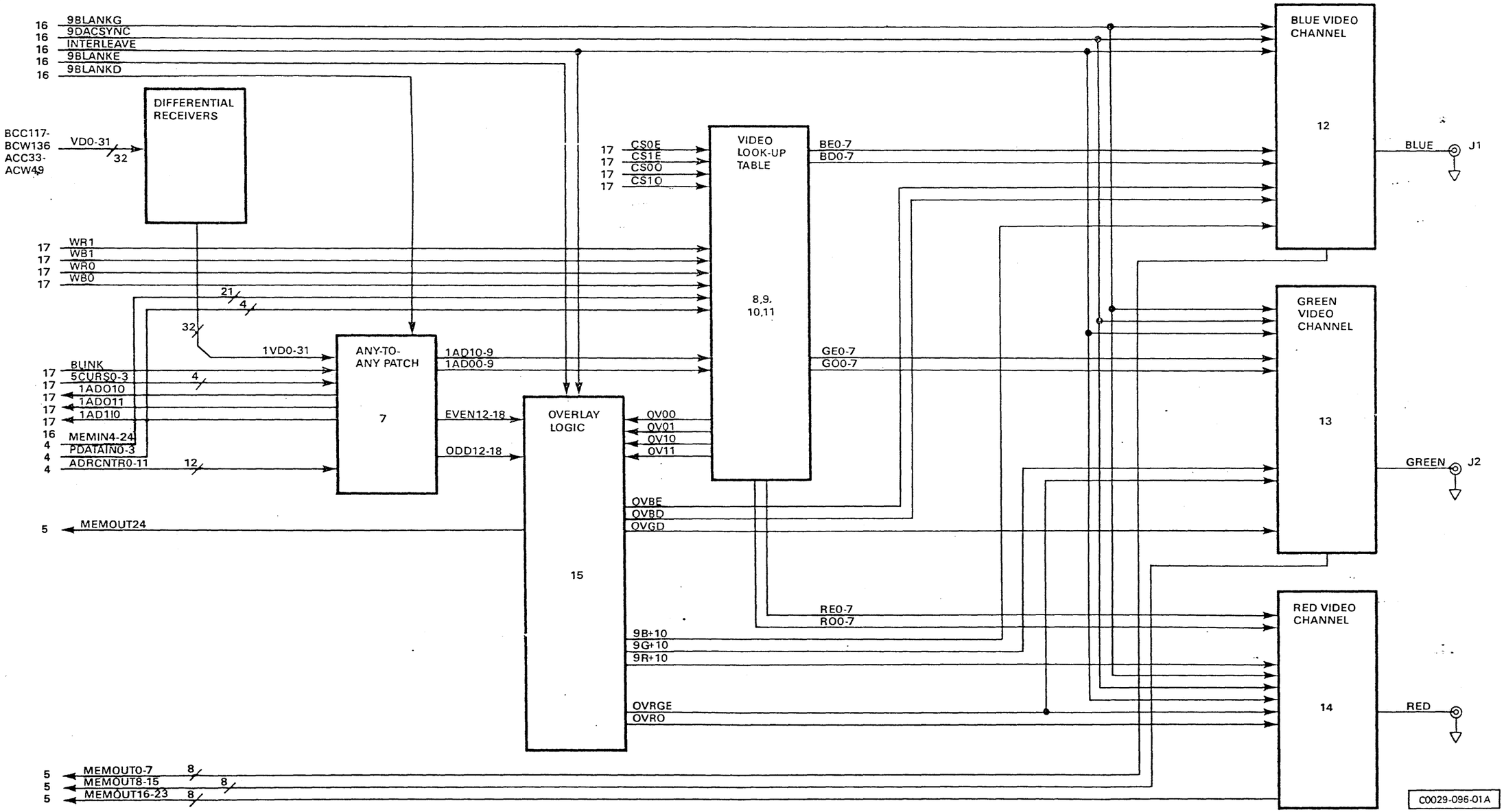


Figure F04-32. Video 7 PCB (Sheet 2 of 2)

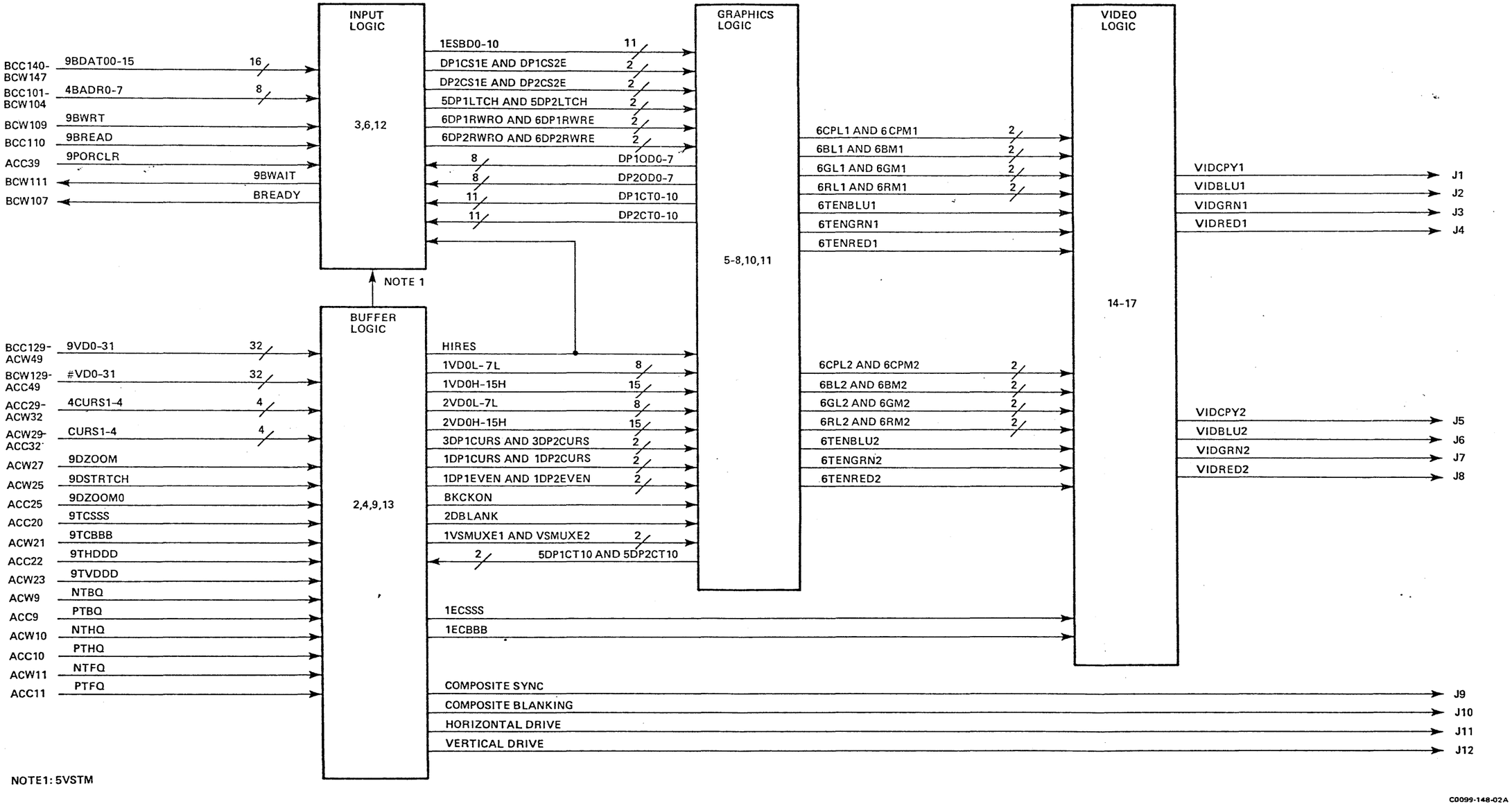


Figure F04-33. Video 8 PCB

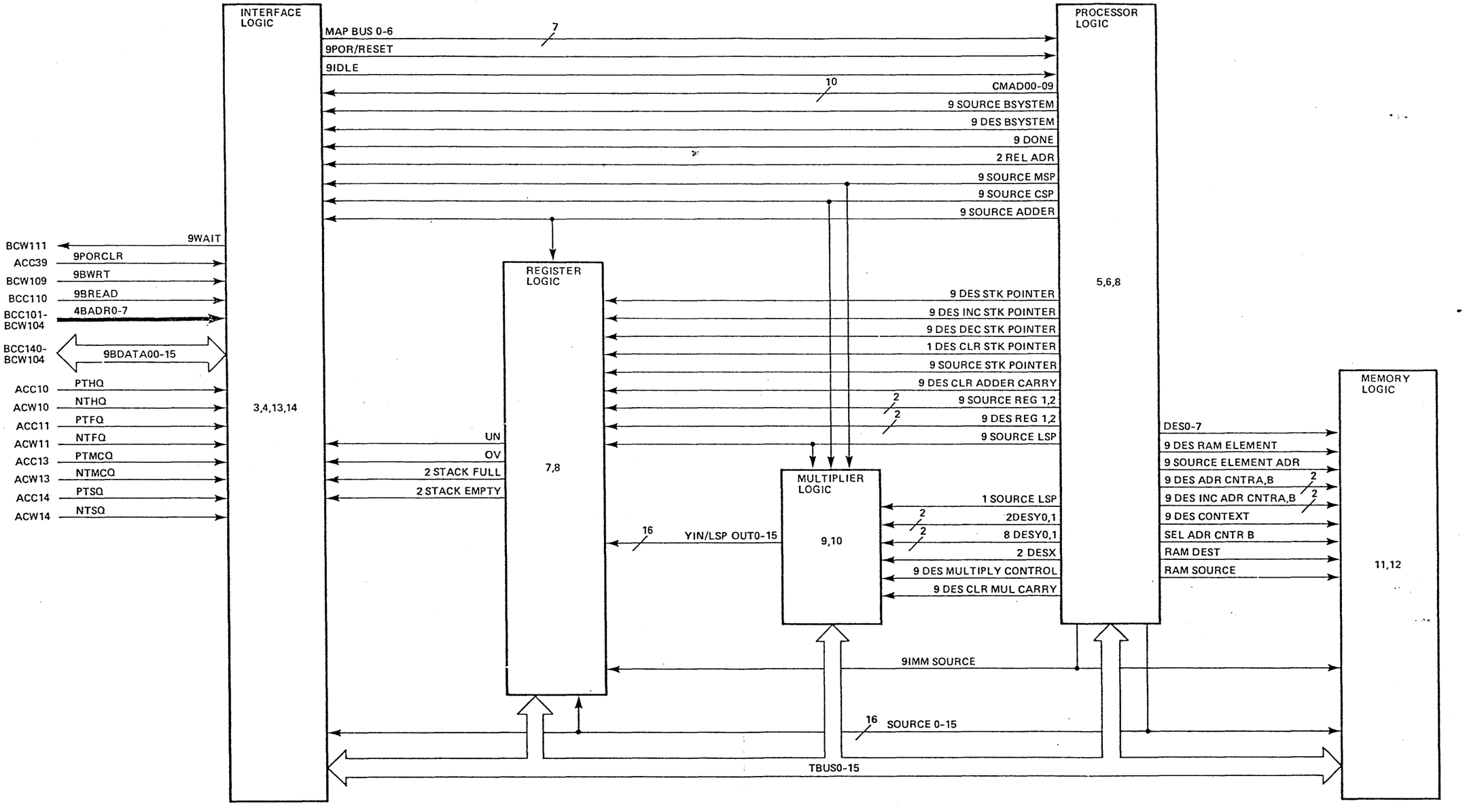


Figure F04-34. Transform PCB

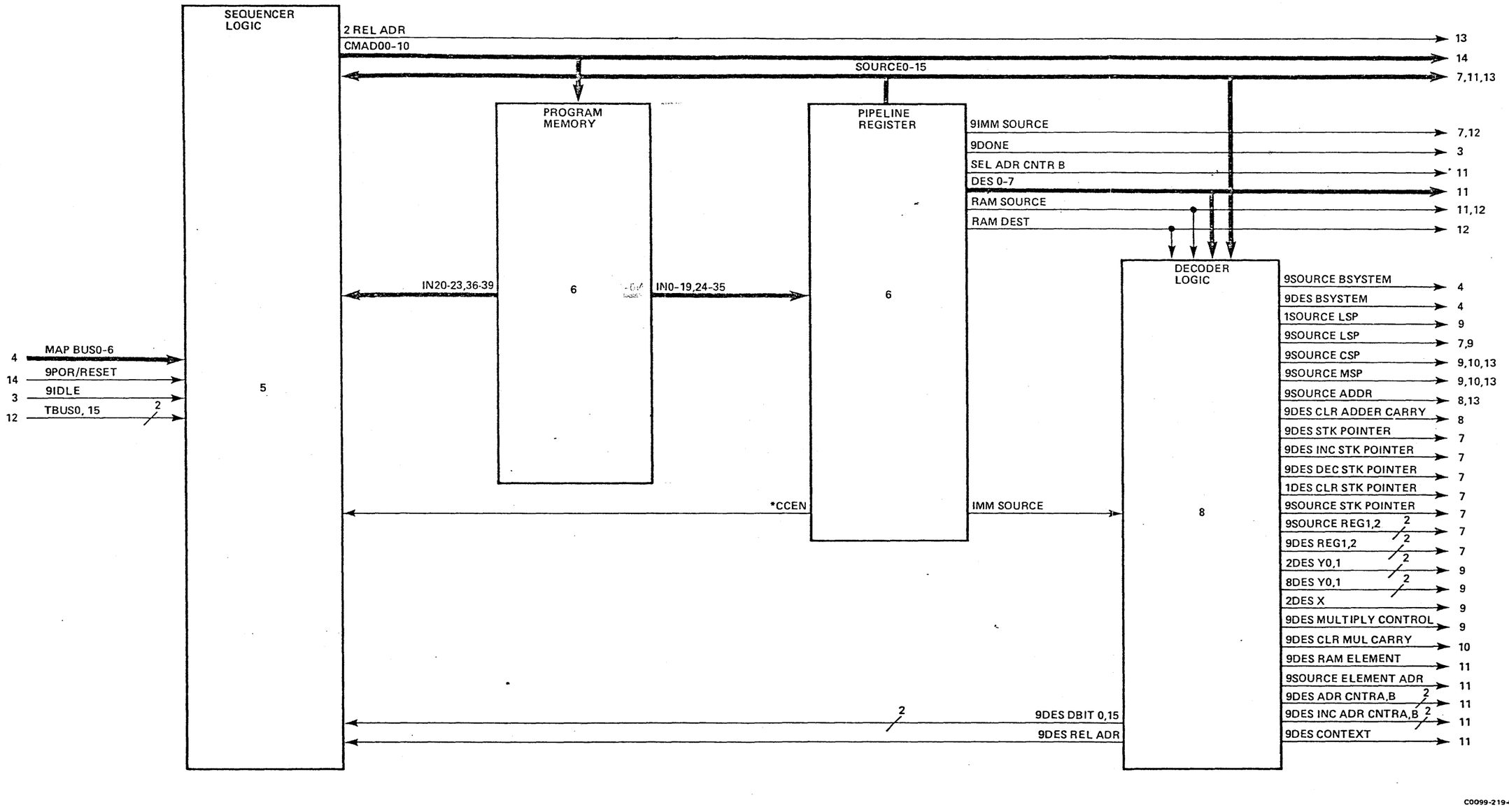


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Figure F04-35. Processor Logic

Chapter 5

MAINTENANCE

5.1 INTRODUCTION

This chapter explains how to service and maintain the 9465. Preventive and corrective maintenance procedures are set forth along with removal and replacement procedures. Following corrective maintenance procedures, accomplish the performance verification procedures as given. Refer to chapter 1, "Related Documents," for peripheral equipment or monitor maintenance documentation.

5.2 TOOLS AND TEST EQUIPMENT

A standard electronics tool kit is adequate for 9465 maintenance. Required test equipment includes a Fluke 8000A digital multimeter (or equivalent) and a Tektronix 465 oscilloscope (or equivalent).

5.3 PREVENTIVE MAINTENANCE

Preventive maintenance is limited to periodically inspecting and cleaning 9465 components. Periodic cleaning can help assure continued service because accumulations of dust and dirt prevent efficient heat dissipation; unless removed, dust and dirt can cause component failure. The interval between inspections will vary because of local environmental conditions; but, Ramtek suggests a 90-day inspection schedule until experience proves otherwise.

WARNING

To prevent personal injury or damage to equipment, disconnect the 9465 from the ac power source before inspecting or cleaning.

Use a soft brush and vacuum cleaner to remove dust gently. Clean the chassis exterior with a soft cloth moistened in a mild soap and water solution. While cleaning, visually inspect for problems such as bent or broken connectors, damaged insulation, improperly seated components, or discoloration that implies heat damage. Unless excessive dust accumulation is obviously implicated, heat damage usually warrants further examination to find and correct the cause.

5.4 CORRECTIVE MAINTENANCE

Corrective maintenance requires a step-by-step approach to fault isolation. The following troubleshooting hints and diagnostic procedures will help isolate problems to a line replaceable unit (LRU).

5.4.1 Troubleshooting Hints

If you encounter a system problem and you suspect a 9465 fault, check all the dc voltages at the control panel test points. If you find a voltage out of tolerance (±1%), adjust corresponding power supply. If you find voltages in tolerance, check the status of the following LED indicators:

- Video 7 PCB DS1-DS3 on
- Transform processor PCB DS1 and DS2 on
- MCP PCB DS1 (self test) off, DS2 on
- Serial link PCB LD1 off

After you check dc voltages and PCB indicators, locate the symptom in table 5-1 and perform the suggested procedure. This table only lists single fault conditions.

WARNING

To prevent personal injury, avoid contact with exposed terminals while performing the following checks with power on.

5.4.2 Diagnostics

Customers who operate with a Digital Equipment Corporation VAX/VMS host computer can troubleshoot the 9465 with the diagnostic procedures documented in RM-9400/RM-9460 Diagnostic and Acceptance Test Operators Manual for VAX/VMS System.

5.5 REMOVAL AND REPLACEMENT

Instructions for removing and replacing power supply, PCBs, and fan plate assembly are ordered in step-by-step sequence. To simplify the procedures, references to washers are omitted; if you encounter washers during removal, save them and reinstall as before. Perform respective removal and replacement steps in the order given.

5.5.1 Power Supply Removal and Replacement

The power supply fastens to the power-supply mounting bracket with six machine screws. Six corresponding threaded inserts receive these screws.

Table 5-1. Fault Isolation Procedures

Step	Symptom	Procedure
1.	System processor PCB (Z80) LD8 off, LD0-7 all on.	At sync PCB, check clock outputs at test points. If clocks are absent, problem is the oscillator; replace sync PCB.
2.	System processor PCB (MC68000) DS9 off, DS1-8 all on.	At sync PCB, check clock outputs at test points. If clocks are absent, problem is the oscillator; replace sync PCB.
3.	System processor PCB (Z80) LD8 stays on and LD0-7 cycle inside out.	Indication is memory checksum error; replace system processor.
4.	System processor PCB (MC68000) DS9 stays on.	Indication is memory checksum error; replace system processor.
5.	System processor PCB (Z80) LD8 goes off after reset, but LD0-7 do not cycle.	Turn power off. Remove all PCBs except sync and system processor. Turn power on; indicators LD0-7 should roll in one direction. If indicators do not roll in one direction, replace processor.
6.	Monitor raster absent.	At sync PCB check horizontal and vertical timing pulses; if bad, replace sync PCB. If horizontal and vertical timing are good, replace video PCB.
7.	Display rolls vertically.	At sync PCB check vertical timing pulse; if bad, replace sync PCB. If vertical timing is good, replace video PCB.
8.	Display tears horizontally.	At sync PCB check horizontal timing pulse; if bad, replace sync PCB. If horizontal timing is good, replace video PCB.
9.	Monitor raster present, but display of data fails (screen remains blank).	Perform hardware reset while observing MCP indicator DS2 (ready). Indicator DS2 should flash off then go back on; system processor PCB indicators LD0-7 should roll from inside out. Indicator DS2 should flash off, then go back on; if not, replace MCP PCB. If indicator DS2 is normal, one-by-one replace memory PCB then video PCB until problem clears.
10.	Monitor display has vertical bars.	Replace memory PCB.

Table 5-1. Fault Isolation Procedures (Continued)

Step	Symptom	Procedure
11.	The monitor does not display keyboard or cursor control inputs.	Perform hardware reset while observing serial link PCB indicator LD1. Indicator LD1 should go on momentarily then go off; if not, replace serial link PCB. If indication is normal, check peripheral connection continuity to serial link PCB.
12.	The monitor does not display input from a single peripheral device.	Check continuity between peripheral device and serial link PCB input port. If correct, try swapping the suspected peripheral device with an identical device that is working on another serial link PCB port. If the working device fails, the problem is a bad port; replace serial link PCB. If the substitute operation succeeds, the problem is a bad peripheral device; replace bad peripheral device.

5.5.1.a Power Supply Removal. Remove the power supply as follows (figure FO5-1):

1. Set circuit breaker CB1 to OFF.
2. Remove cabinet rear access panel by removal of eight screws.
3. Disconnect the two snap-on connectors in wires supplying ac power to the exhaust fan.
4. Remove four screws from the protective cover on top of the power supply.
5. Remove two screws holding the power supply bracket to the chassis frame.
6. Pull outward on the top edge of the power supply bracket to slowly lower the bracket and attached power supply to the position shown.
7. Cover the slots in the top of the power supply with tape in order to prevent loose hardware from falling into the supply.
8. Remove the hex nuts and large machine screws fastening the conductors to terminal blocks. Remove the yellow plastic barrier to get access to the wiring under it. All conductors passing through the opening in the power supply bracket must be disconnected in order to remove the power supply. **When removing cabling, note cable markings and color codes in relation to terminals.**

9.

CAUTION

Power supply is heavy. This procedural step results in the power supply becoming free to fall; therefore, provide adequate support to prevent injury or damage.

Disengage two cable clamps by removing two screws from each. One of these screws attaches the cable which limits the fall of the power supply; removal of this screw will allow the power supply to fall unless support is provided. Lift power supply away from chassis frame.

10. Power supply is now mechanically and electrically detached from the power supply bracket and all connecting wiring, so this completes the removal procedure.

5.5.1.b Power Supply Replacement. Replace power supply as follows:

1. Support power supply (or have assistant support power supply); finger tighten four screws holding power supply to power supply mounting bracket. Don't forget the restraint cable attachment. This is a reverse of step 9 above.

2. Tighten all four screws.

3. Reconnect cables to terminals; replace barrier strip cover. Remove the tape installed in step 7 above.

4. Push the power supply to an upright position. Insert two screws through the power supply bracket and into the chassis frame.

5. Replace power supply protective cover and attach with screws.

6. Replace rear panel and in the process engage the snap-on electrical connectors. Insert eight screws to fasten the rear panel in place.

7. Set circuit breaker CB1 to ON.

5.5.2 PCB Removal and Replacement

Connector hardware can vary between PCBs. Some PCBs lack cable connectors, some have BNCs, some have multipin connectors, and some have a combination of connectors. Ensure you securely fasten multipin connector screws and BNCs when replacing PCBs.

NOTE

To minimize radio-frequency interference, you must tighten any screws that fasten a PCB cable connector to the PCB. Also, securely fasten BNCs.

CAUTION

Do not place PCBs on a conducting surface. Static discharge can cause permanent damage. Store and move PCBs enclosed in an anti-static bag.

5.5.2.a PCB Removal. Remove a PCB as follows:

1. Open cabinet rear access panel.
2. Set circuit breaker CB1 to OFF.
3. Open front access panel. Before you remove PCB, record cable identification data for future reference.
4. Remove any cable connectors fastened to PCB connectors.
5. Grasp PCB extraction tab, extend outwards and apply firm but steady leverage. You will note a decrease in resistance when PCB is free of the backplane assembly connectors.
6. Carefully slide PCB out of PCB cage assembly.
7. Place PCB on a piece of foam or other nonconducting padded surface.

5.5.2.b PCB Replacement. Replace a PCB as follows:

CAUTION

Installing a PCB in the wrong slot can cause severe equipment damage. Observe color markings.

1. The PCB component side is on the left when facing PCB cage assembly. Grasp PCB edges and align top and bottom edges with PCB cage assembly slots.

2. Insert PCB in PCB cage assembly until you encounter resistance. Fold PCB extraction tabs. With thumbs against folded PCB extraction tabs, apply firm pressure. PCB fully seats when rearward travel ends.

3. Observe cable identification data recorded during removal. Replace any connectors.

4. Close cabinet front access panel.

5. Set circuit breaker CB1 to ON.

6. Close cabinet rear access panel.

5.5.3 Fan Plate Assembly Removal and Replacement

The 9465 has one fan plate assembly (figure FO5-2) with six fans. The fan plate assembly has a single six-position power plug.

5.5.3.a Fan Plate Assembly Removal. Remove the fan plate assembly as follows:

1. Set circuit breaker CB1 to OFF.

2. Open cabinet front access panel.

3. Remove machine screw that fastens fan plate assembly to lower card guide.

4. Reach into air intake and unplug fan plate assembly cable, plug P5. (There is one plastic detent on either side of the plug; squeeze plug P5 to free these detents and pull straight up.)

5. Slide fan plate assembly out of chassis.

5.5.3.b Fan Plate Assembly Replacement. Replace the fan plate assembly as follows:

1. Slide fan plate assembly into chassis.

2. Replace machine screw that fastens fan plate assembly to lower card guide.

3. Reach into air intake under lower card guide and plug fan plate assembly cable, plug P5, into mating connector.

4. Close cabinet front access panel.

5. Set circuit breaker CB1 to ON.

5.6 PERFORMANCE VERIFICATION

This paragraph tells how to verify operational performance of an installed 9465 operating with a Digital Equipment Corporation host computer.

8000110-01A

1. Set CB1 to ON.
2. Open cabinet front access panel.
3. Set RES switch to the resolution of your monitor.
4. Close front access panel.

NOTE

To comply with FCC regulations for a Class A computing device, the cabinet front access panel must remain closed when power is applied to the 9465. The rear access panel can remain open and meet FCC regulations, but this practice may adversely affect component cooling. For these reasons the cabinet access panels should always remain shut when the 9465 is operating.

5. At host computer, load magnetic tape or diskette containing the diagnostic and acceptance tests. Run diagnostic and acceptance tests following procedures given in RM-9400/RM-9460 Diagnostic and Acceptance Test Operators Manual for VAX/VMS System.

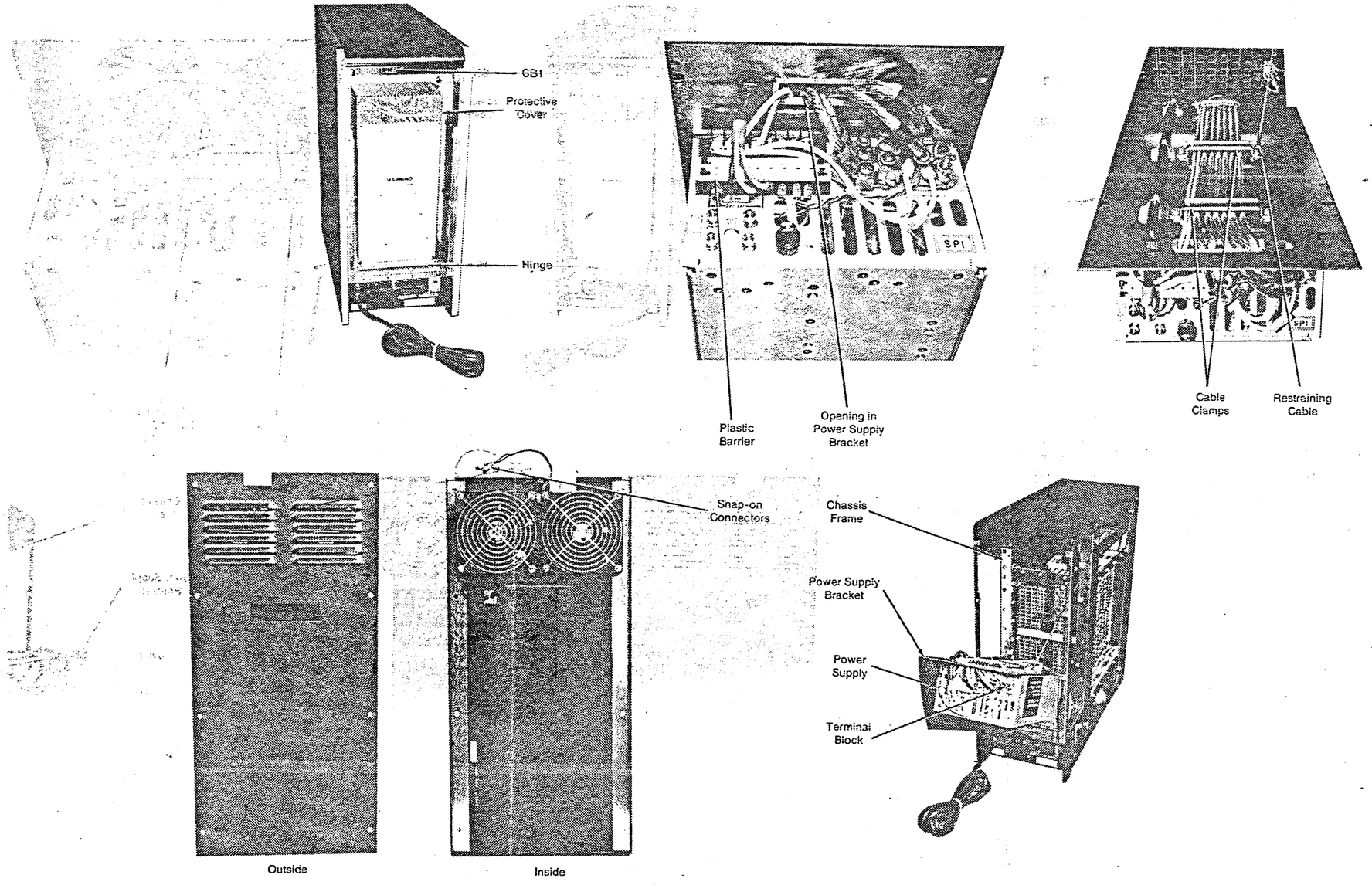

Figure F05-1. Power Supply Assembly Removal And Replacement

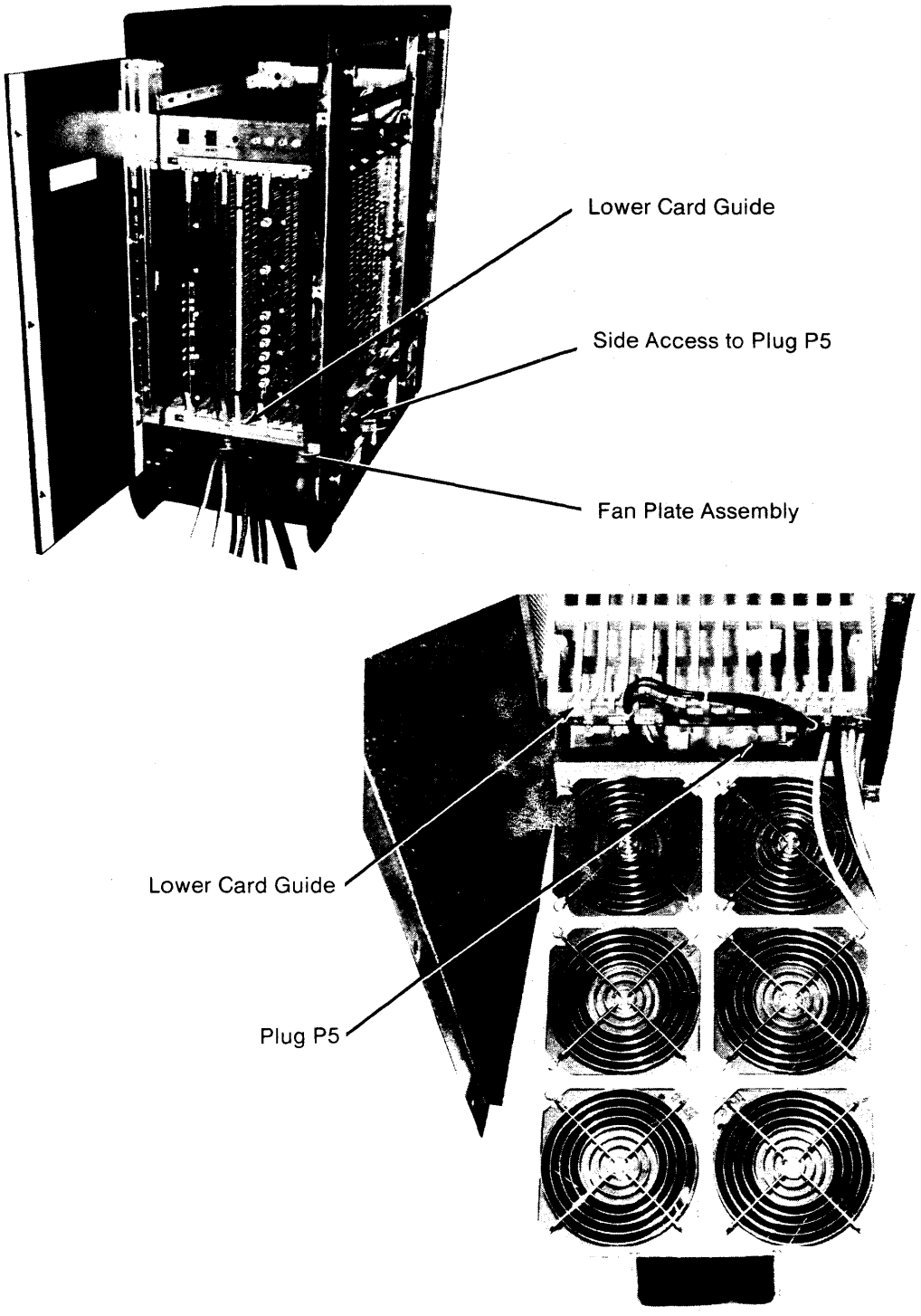

Figure F05-2. Fan Plate Assembly Removal and Replacement