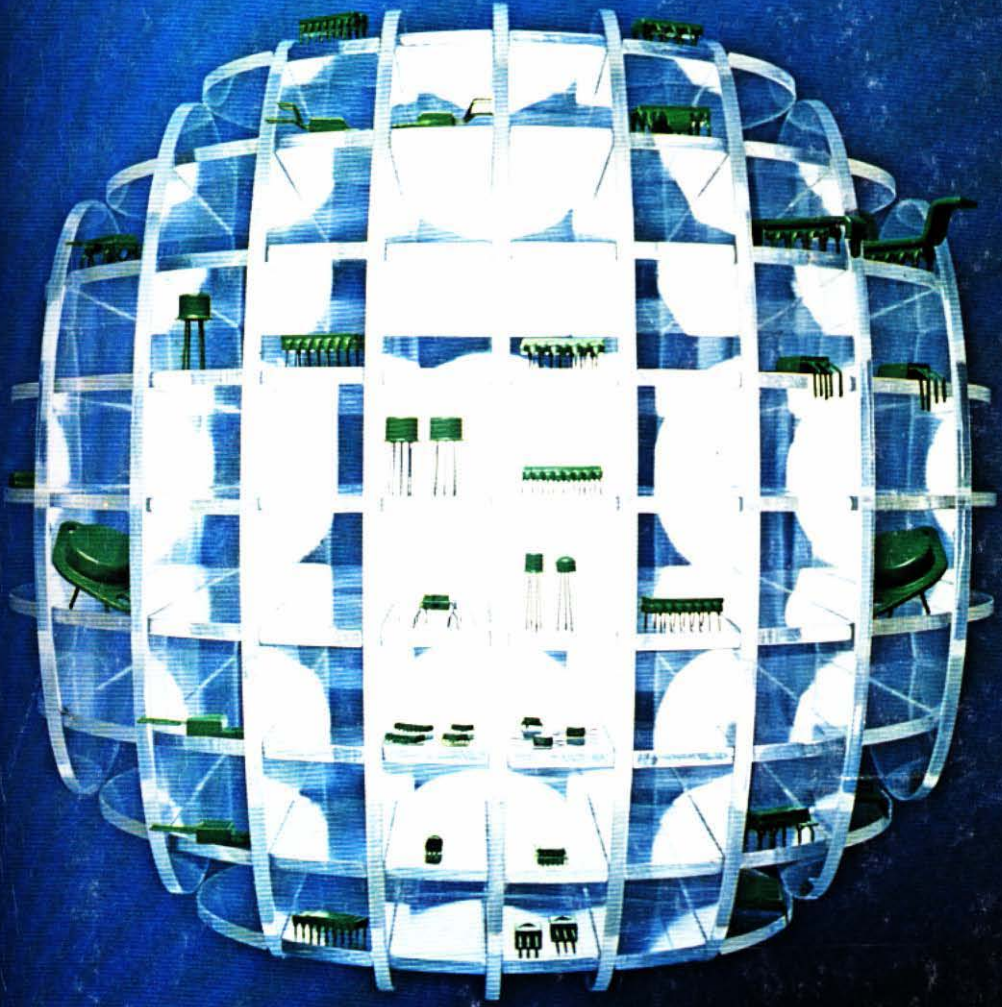
databook

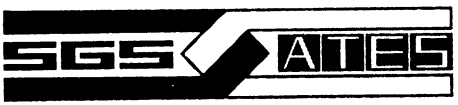
SGS ATES

MOS AND SPECIAL COS/MOS

1st EDITION



databook



MOS AND
SPECIAL
COS/MOS
1st EDITION
ISSUED
NOV. 1979

INTRODUCTION

This databook contains data sheets on the SGS-ATES range of products in MOS and COS/MOS technology.
The information on each product has been specially presented in order that the performance of the product can be readily evaluated within any required equipment design.
The databook also contains a summary of the processes available in SGS-ATES for the development and production of the products listed.

FUNCTIONAL INDEX

FUNCTIONAL INDEX (continued)

SGS-ATES MOS processes history and summary

SGS-ATES entered the MOS market in 1969 with the newly developed Planox process. This was followed by development of the P-channel Silicon Gate process in 1971 and the N-channel Silicon Gate process in 1973.

In 1976 the company began development of the N-channel process with double polycrystalline silicon which is extremely important for the realization of very high complexity circuits or memories.

In 1977 SGS-ATES developed electrically programmable read-only memories and in 1978 Non-Volatile read and write memories.

Concerning COS/MOS technologies, in 1974 SGS-ATES put the type A Aluminium Gate Process into production followed in 1976 by the type B process with ion implantation.

The Low Voltage Aluminium Gate process was developed in 1978 and put into production in 1979.

SGS-ATES MOS processes

1. P-channel enhancement mode with a P-type polycrystalline silicon gate
   - Threshold voltage: 1.5 to 2.5V
   - Supply voltages: V_{CC} = +5V, V_{GG} = -12V
   - Used in static and dynamic 2 Ø applications
   - Compatible with bipolar circuits
2. Low threshold N-channel enhancement/depletion mode with an N-type polycrystalline silicon gate
   - Threshold voltage: 0.6 to 1.2V
   - Supply voltage: V_{CC} = +5V
   - Used in static and dynamic systems
   - Compatible with bipolar circuits
3. N-channel enhancement/depletion mode with an N-type polycrystalline silicon gate
   - Threshold voltage: 0.8 to 1.2V with V_{BB} = -5V
   - Supply voltages: V_{DD} = +12V, V_{BB} = -5V, V_{CC} = 5V
   - Used in static and dynamic systems
   - Compatible with bipolar circuits
4. N-channel enhancement/depletion mode with an N-type polycrystalline silicon gate
   - Threshold voltage: 0.8 to 1.2V
   - Supply voltages: V_{DD} = +12V, V_{CC} = 5V
   - Used in static and dynamic systems
   - Compatible with bipolar circuits
5. N-channel enhancement/depletion mode with double N-type polycrystalline silicon gate
   - Threshold voltage: 0.8 to 1.2V with V_{BB} = -5V
   - Supply voltages: V_{DD} = +12V, V_{BB} = -5V, V_{CC} = 5V
   - Used for UV erasable and electrically programmable ROMs
   - Compatible with bipolar circuits
6. N-channel enhancement/depletion mode with double N-type polycrystalline silicon gate
   - Threshold voltage: 0.8 to 1.2V
   - Supply voltage: V_{DD} = +12V, V_{CC} = 5V
   - Used for UV erasable and electrically programmable ROMs
   - Compatible with bipolar circuits
7. COS/MOS Aluminium Gate A & B process
   - Threshold voltage: 1 to 2V
   - Supply voltage: V_{DD} = +3 to +18V
8. COS/MOS Aluminium gate - low threshold voltage
   - Threshold voltage: 0.5V to 1V
   - Supply voltage: V_{DD} = 1.5 to 5V

DATA-SHEETS

MOS INTEGRATED CIRCUITS

4 CHANNEL MULTIPLEXER

The M005 is a 4 channel multiplexer constructed on a single monolithic chip using P-channel low threshold silicon gate technology. The device is available in 10-lead metal case similar to Jedec TO-100.

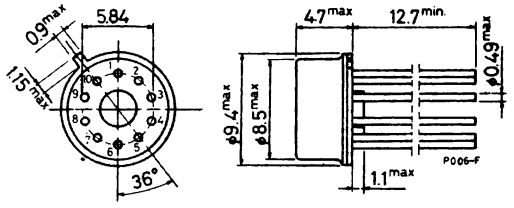
ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain to source voltage	-10 to 0.3	V
V_{GS}	Gate to source voltage	-35 to 0.3	V
V_{GD}	Gate to drain voltage	-25 to 0.3	V
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

ORDERING NUMBER: M 005 T1

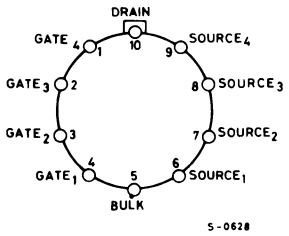
MECHANICAL DATA

Dimensions in mm

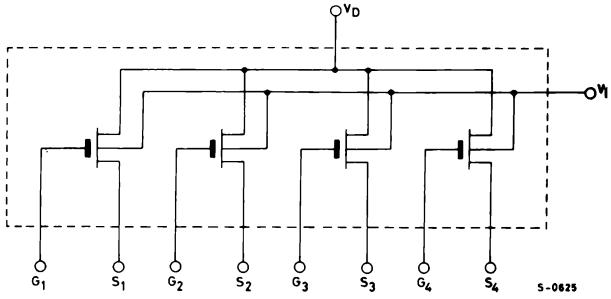


M 005

PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
V_i	Analog input voltage	V_{GS}= -20V	V_{BULK}= 10V			± 10	V
V_{THO}	Threshold voltage	V_{DS}= V_{GS} V_{BS}= 0	I_{DS}= 100 μA	-1		-2.5	V
R_{DS}	Drain to source on resistance	V_{GS}= -10V V_{BS}= 0	I_{DS}= 10 mA		20	50	Ω
		V_{GS}= -20V V_{BS}= 0	I_{DS}= 10 mA		13	30	Ω
I_{GL}	Gate leakage current	V_{GS}= -10V V_{BS}= 0	V_{DS}= 0			-1	nA
I_{DL}	Drain leakage current	V_{DS}= -5V V_{BS}= 0	V_{GS}= 0			-20	nA
I_D	Drain current	V_{GS}= V_{DS}= -5V	V_{BS}= 0		-60		mA

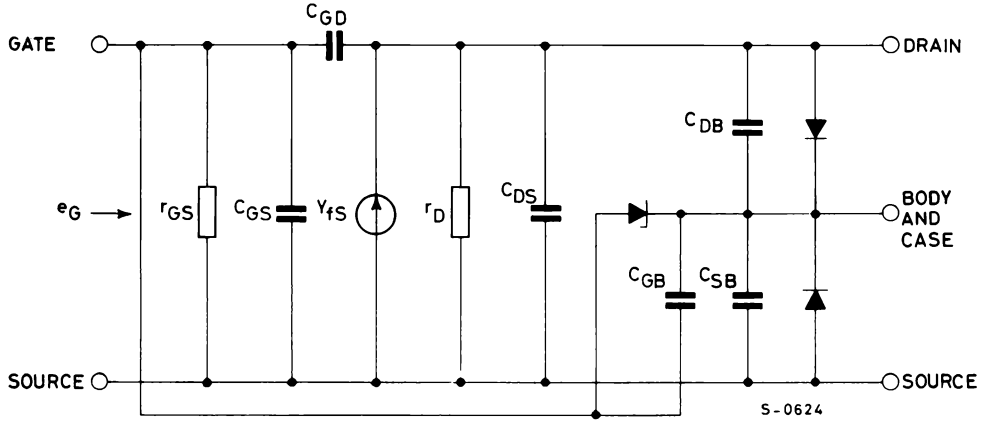
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
Y_{fs}	Forward transadmittance	V_{DS}= -3V V_{BS}= 0V	V_{GS}= -10V		12.000		μmho
C_{DS}*	Drain to source capacitance	V_{DS}= 0 V_{IPP}= 15 mV	f = 1 MHz		0.15	0.20	pF
C_{GD}*	Gate to drain capacitance	V_{GD}= 0 V_{IPP}= 15 mV	f = 1 MHz		2	3	pF
C_{GS}*	Gate to source capacitance	V_{GS}= 0 V_{IPP}= 15 mV	f = 1 MHz		2	3	pF
C_{SB}*	Source to body capacitance	V_{SB}= 0 V_{IPP}= 15 mV	f = 1 MHz		8	10	pF
C_{DB}*	Drain to body capacitance	V_{DB}= 0 V_{IPP}= 15 mV	f = 1 MHz		32	40	pF
C_{GB}*	Gate to body capacitance	V_{GB}= 0 V_{IPP}= 15 mV	f = 1 MHz		4	6	pF

* This parameter is periodically sampled and not 100% tested.

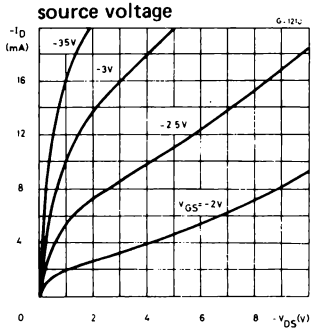
SMALL SIGNAL EQUIVALENT CIRCUIT

(conditions: V_{GS}= -10V, V_{DS}= -3V, V_{BS}= 0) I ≃ 150 mA

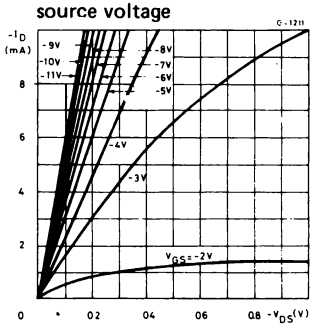


Symbol	Characteristics	Typical values	Unit
Diodes	All diodes are to be considered perfect diodes		
r_{GS}	Gate to source leakage resistance and diode leakage resistance	10^{10}	Ω
r_D	Dynamic drain resistance	0.5	kΩ
C_{GS}	Gate to source capacitance	2	pF
C_{GD}	Gate to drain capacitance	2	pF
C_{DS}	Drain to source capacitance	0.15	pF
C_{GB}	Gate to body capacitance	6	pF
C_{DB}	Drain to body capacitance	40	pF
C_{SB}	Source to body capacitance	10	pF
Y_{fs}	Forward transadmittance	12.000	μmho

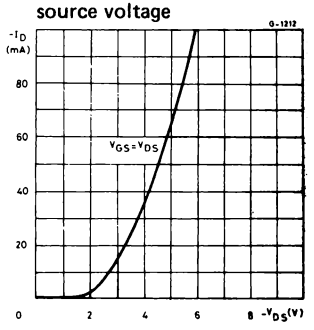
Drain current vs. drain to source voltage



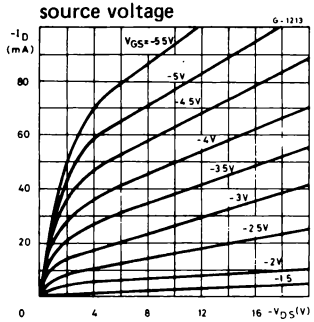
Drain current vs. drain to source voltage



Drain current vs. drain to source voltage

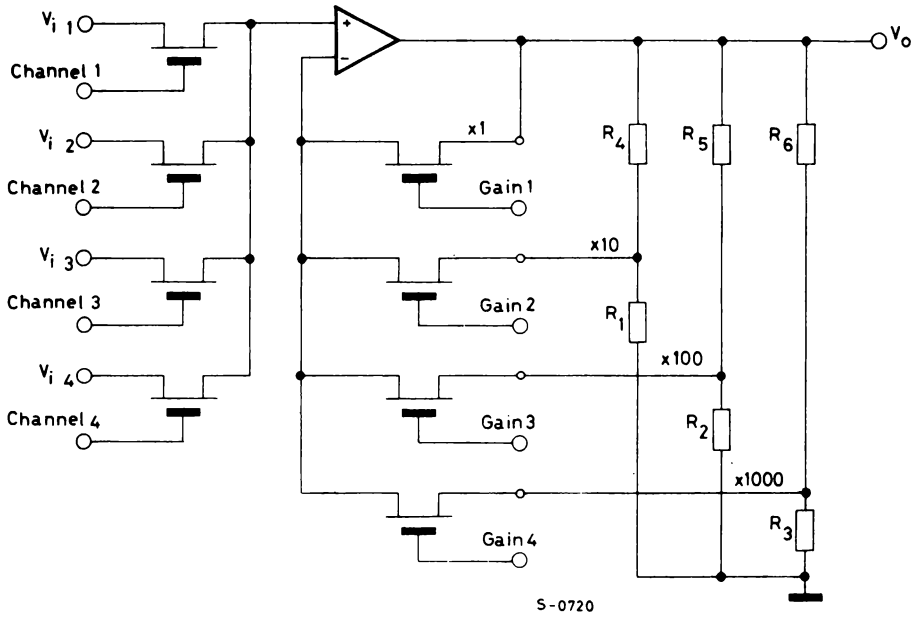


Drain current vs. drain to source voltage

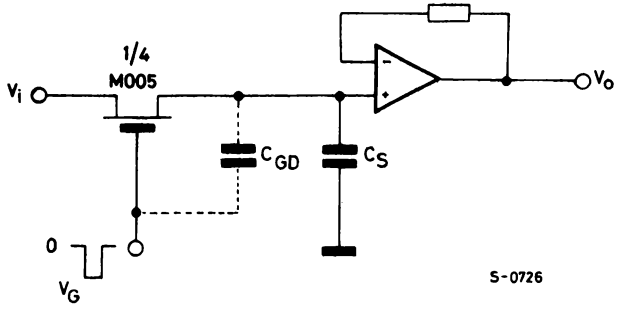


TYPICAL APPLICATIONS

Variable gain amplifier with multiplexed inputs

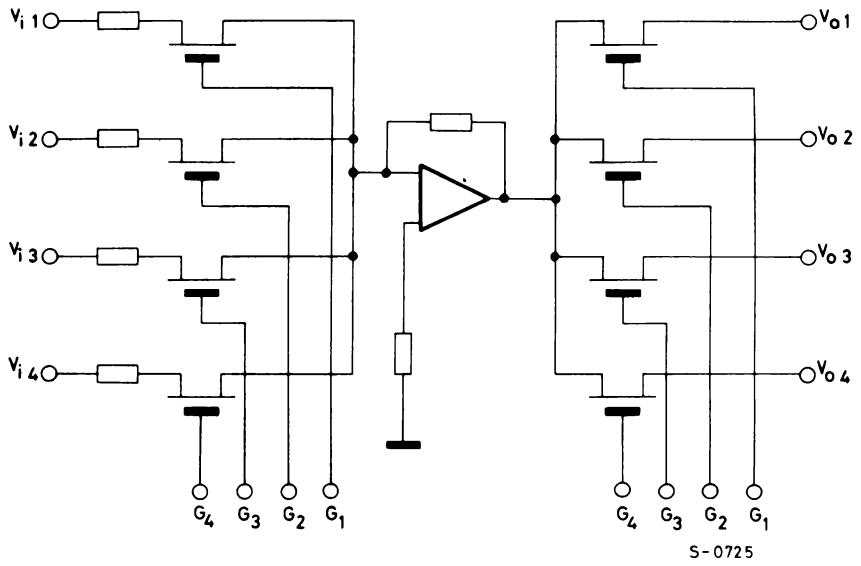


Sample and hold



TYPICAL APPLICATIONS(continued)

Multiplexing - demultiplexing



MOS INTEGRATED CIRCUIT

COUNTER-CONTROLLED 8-CHANNEL SEQUENTIAL MULTIPLEXER

- LOW ON RESISTANCE
- LOW CAPACITANCE BETWEEN IN/OUT CHANNELS
- FULLY TTL or DTL COMPATIBLE
- LOW POWER DISSIPATION: 70 mW TYP.

The M006 is a monolithic integrated circuit using low threshold P-channel silicon gate MOS technology. It is supplied in a 16-pin dual in-line plastic or ceramic package. Functionally the device consists of a modulo-8 counter, sequentially controlling the opening or closing of 8 analogic switches. Each of the switches is formed by two transistors T1 and T2 with their drains connected together. The closure of each in/out switch occurs on the rising edge of the clock and has a duration of half the clock period. The inputs to the device are:

clock input, to drive the counter;
reset input, to return the counter to zero;
matrix enable, to enable the logic network which decodes the counter states and drives the eight switches shunt enable, which determines whether transistors T2 can switch or not.

The eight transistors T1 have their sources connected together and brought out on the "Serial Bus". Similarly the sources of transistors T2 are commoned and brought out on the "Parallel Bus".

ABSOLUTE MAXIMUM RATINGS

V_{GG} *	Source supply voltage	-20 to 0.3	V
V_I	Analog input voltage (distortion < 70 dB)	± 2	V
V_I *	Input voltage	-20 to 0.3	V
$V_{I/O}$ *	Bus voltage	-20 to 0.3	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

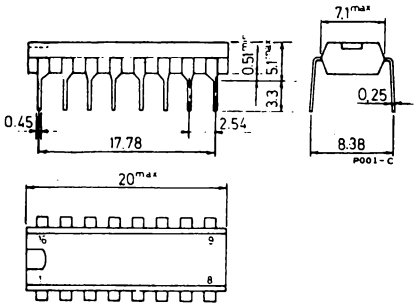
* This voltage is with respect to V_{SS} (GND) pin voltage.

ORDERING NUMBERS:

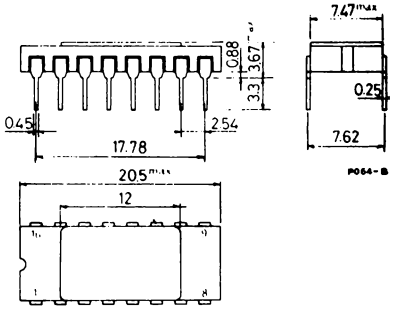
M006 B1 for dual in-line plastic package
M006 D1 for dual in-line ceramic package

MECHANICAL DATA (dimensions in mm)

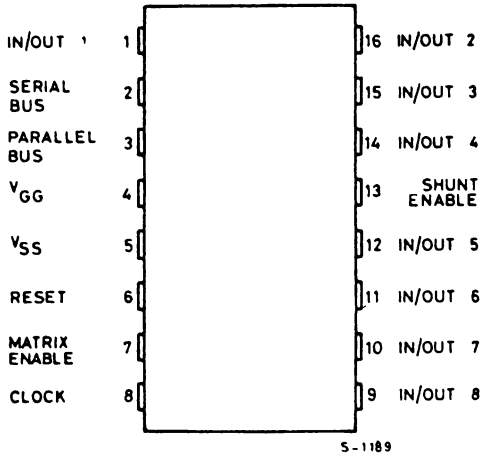
Dual in-line plastic package



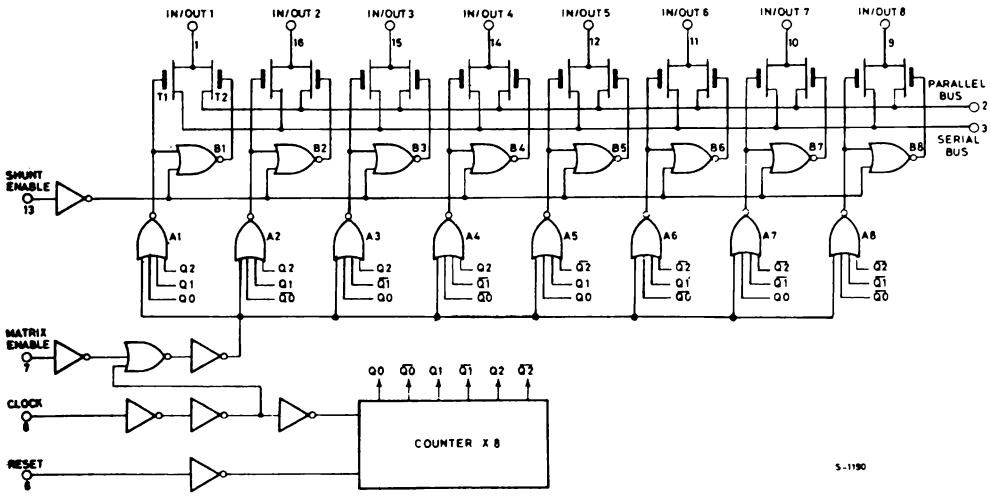
Dual in-line ceramic package



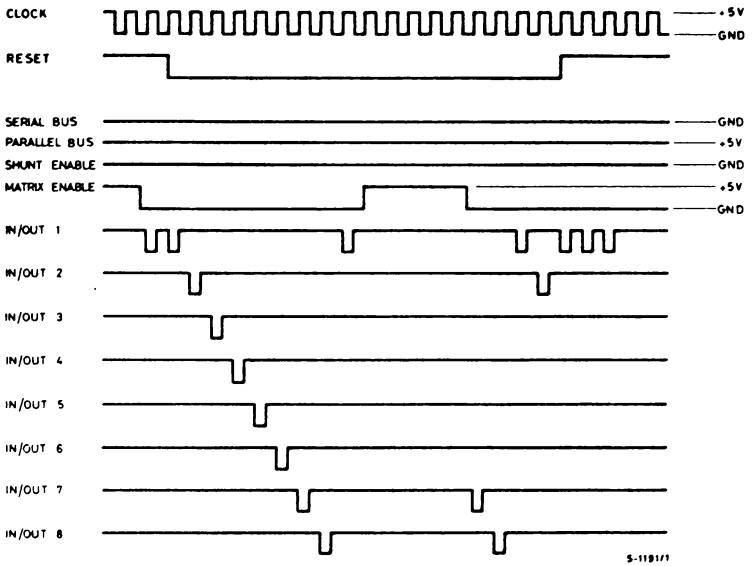
PIN CONNECTIONS



LOGIC DIAGRAM



TIMING DIAGRAM



TRUTH TABLE (negative logic)

To simplify the description of the functional operation of the device this truth table has been compiled assuming the serial and parallel bus terminals as inputs, and the eight in/out terminals as outputs.
Closure of the switches T1 and T2 is controlled by the signals Shunt Enable, Matrix Enable and Reset, and the counter states.

S. E.	M.E.	RESET	COUNTER STATES Q0 Q1 Q2	PARALLEL BUS	SERIAL BUS	IN/OUT 1	IN/OUT 2	IN/OUT 3	IN/OUT 4	IN/OUT 5	IN/OUT 6	IN/OUT 7	IN/OUT 8
0	0	0	0 0 0	X	X	F	F	F	F	F	F	F	F
0	0	1	COUNTING	X	X	F	F	F	F	F	F	F	F
0	1	0	0 0 0	X	Y	**Y/F	F	F	F	F	F	F	F
0	1	1	1* 1 0	X	Y	F	F	F	Y	F	F	F	F
1	0	0	0 0 0	Z	Y	Z	Z	Z	Z	Z	Z	Z	Z
1	0	1	COUNTING	Z	Y	Z	Z	Z	Z	Z	Z	Z	Z
1	1	0	0 0 0	Z	Y	**Y/Z	Z	Z	Z	Z	Z	Z	Z
1	1	1	0* 0 1	Z	Y	Z	Z	Z	Z	Y	Z	Z	Z

* For example
** In synchronism with the clock

0 = V_{SS}
1 = GND
X = Don't care

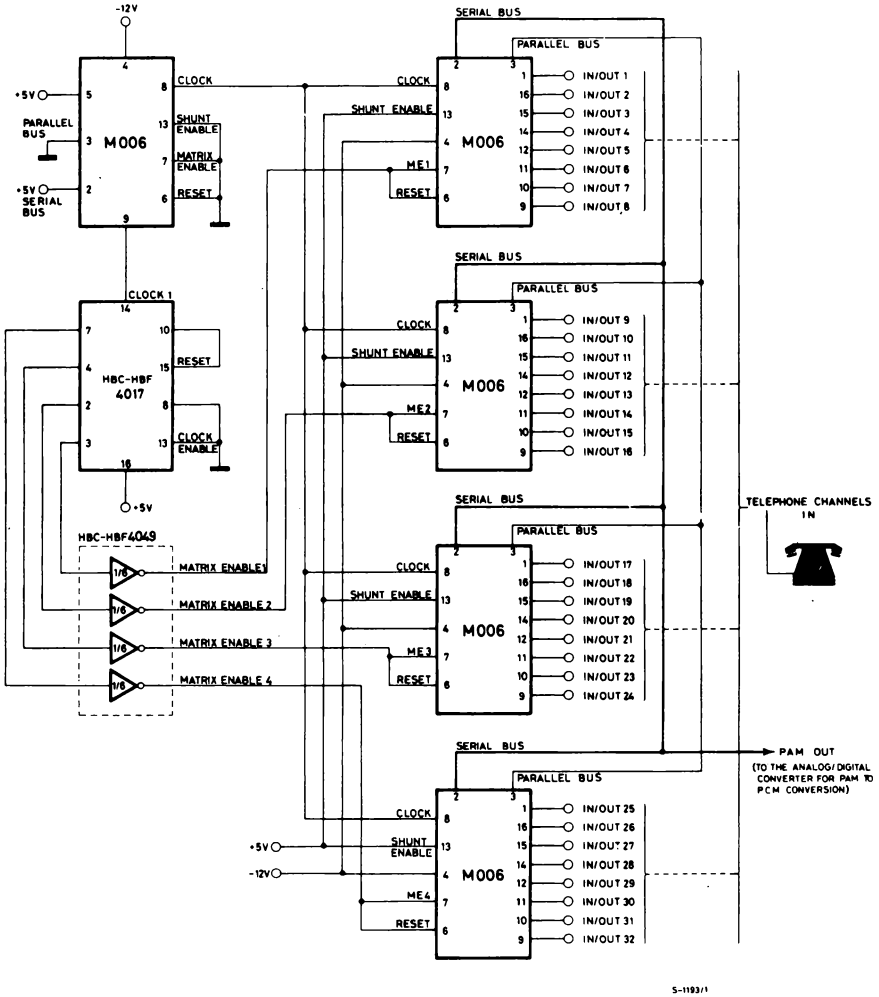
F = Floating
Y = Digital or analog signal
Z = Logic level

TIMING AND DYNAMIC ELECTRICAL CHARACTERISTICS (V_{SS} = 4.75 to 5.25V, V_{GG} = -11.5 to -12.5V, T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Values Min.	Values Typ.	Values Max.	Unit
$V_{\phi H}$	Clock high voltage		V_{SS}-1.5		V_{SS}	V
$V_{\phi L}$	Clock low voltage		V_{GG}		0.4	V
R_{D5}	Drain to source on resistance	I_{D5}= 100 µA -2V T1 serial IN/OUT 5V T2 parallel IN/OUT			300 250	Ω
f_{CL}	Maximum clock frequency			1		MHz
$t_{\phi pw}$	Clock pulse width			0.5		µs
	Shunt enable, matrix enable, reset to high		V_{SS}-1.5		V_{SS}	V
	Shunt enable, matrix enable, reset to low		V_{GG}		0.4	V
C_I	Input capacitance	V_I= V_{SS} f = 1 MHz		6		pF
$C_{I/O}$	Capacitance between adjacent channels	V_{IPP}= 15 mV f = 1 MHz			0.5	pF

TYPICAL APPLICATIONS

PAM section of 32-channel PCM terminal in transmit mode. (Negative logic)



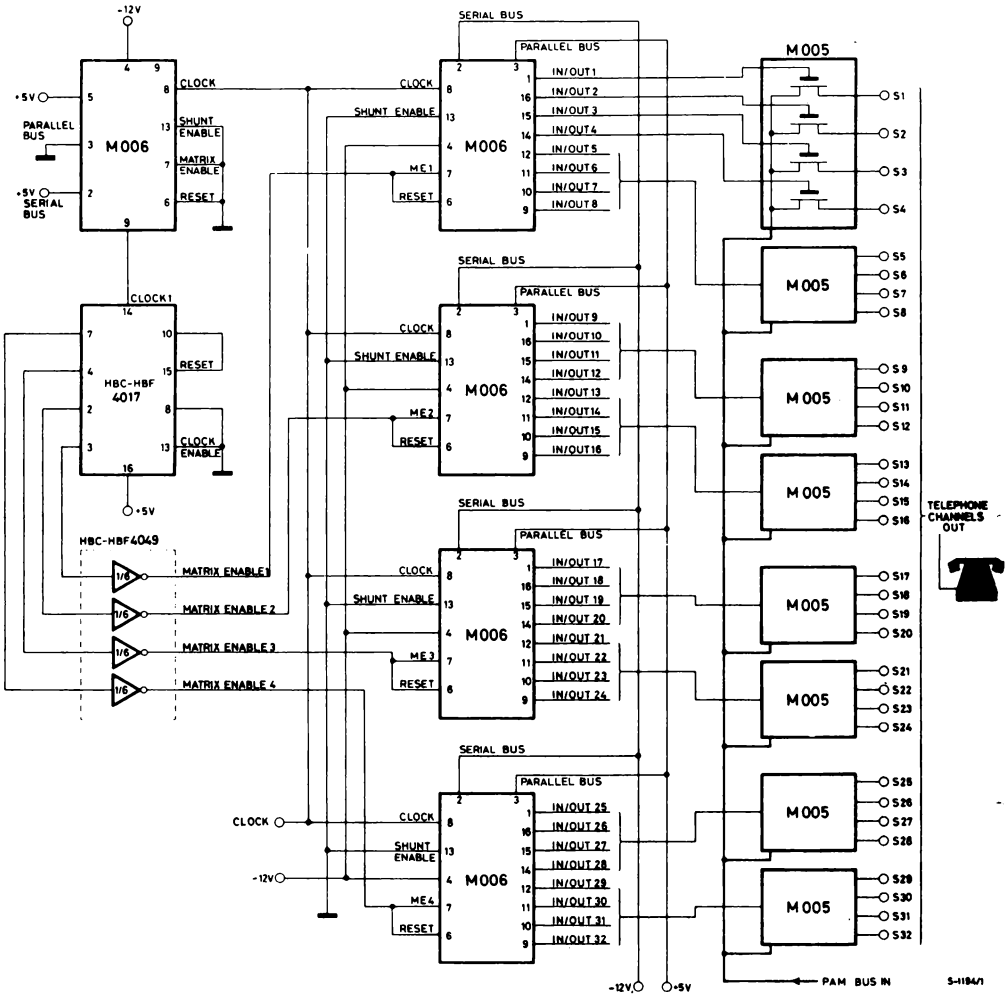
The "parallel bus" is floating since transistors T2 are hold off by the shunt enable input. The telephone inputs are IN/OUT 1 . . . . . IN/OUT 32.

The output is obtained on the "serial bus" as a train of pulses on a single line sequentially combining all the input signals.

The 300 Ω on resistance of T1 is acceptable in the transmit mode.

TYPICAL APPLICATIONS (continued)

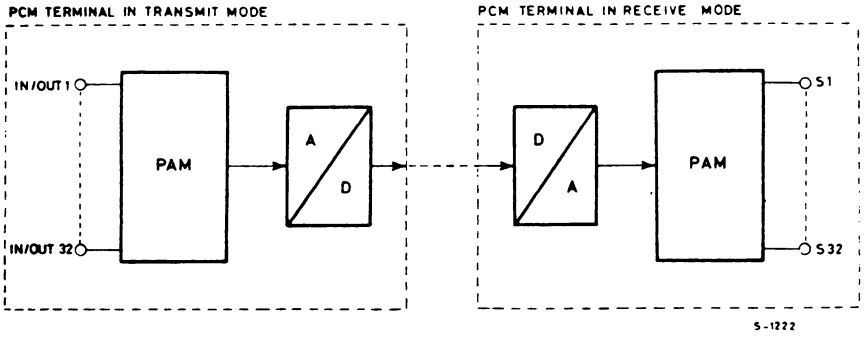
PAM section of a 32-channel PCM terminal in receive mode. (Negative logic)



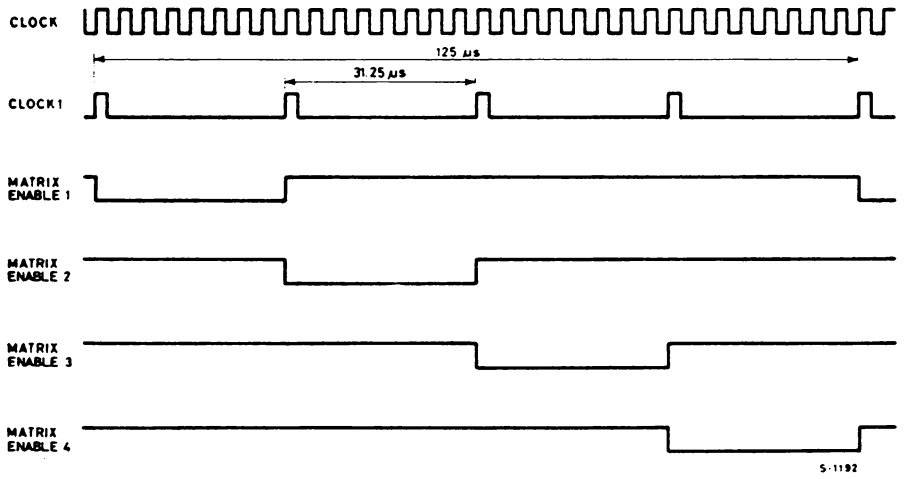
In reception a train of amplitude modulated pulses on the input bus is demultiplexed into 32 channel outputs S1 . . . . . S32. Since a low series resistance is essential the M005 ($R_{DS/ON} \cong 20\Omega$) has been used.

TYPICAL APPLICATIONS (continued)

Block diagram



Timing waveforms refer to a.m. 32-channel PAM telephone system



2 CHANNEL MULTIPLEXER

The M009 is a 2 channel multiplexer constructed on a single monolithic chip using P-channel low threshold silicon gate technology. The device is available in 8-lead metal case similar to Jedec TO-99.

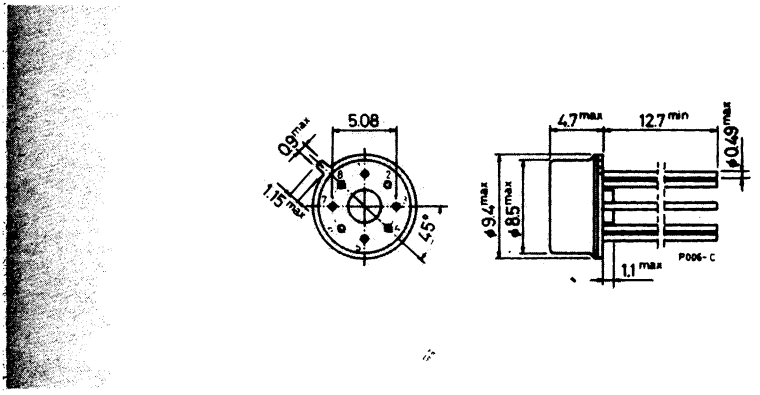
ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain to source voltage	-10 to 0.3	V
V_{GS}	Gate to source voltage	-35 to 0.3	V
V_{GD}	Gate to drain voltage	-25 to 0.3	V
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

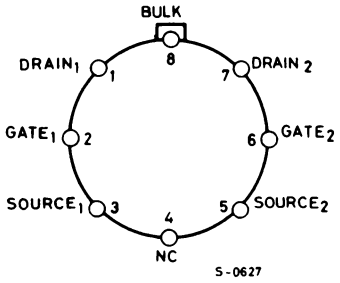
ORDERING NUMBER: M 009 T1

MECHANICAL DATA

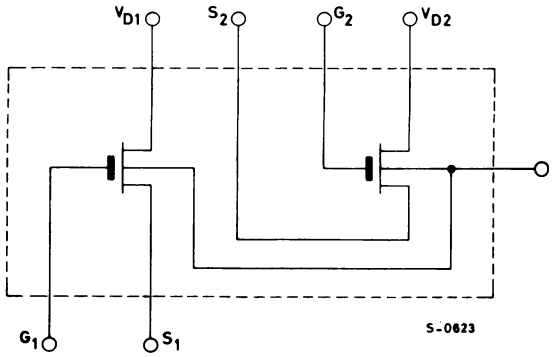
Dimensions in mm



PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
V_i	Analog input voltage	V_{GS}= -20V	V_{BULK}= 10V			± 10	V
V_{THO}	Threshold voltage	V_{DS}= V_{GS} V_{BS}= 0	I_{DS}= 100 µA	-1		-2.5	V
R_{DS}	Drain to source on resistance	V_{GS}= -10V V_{BS}= 0	I_{DS}= 10 mA		20	50	Ω
		V_{GS}= -20V V_{BS}= 0	I_{DS}= 10 mA		13	30	Ω
I_{GL}	Gate leakage current	V_{GS}= -10V V_{BS}= 0	V_{DS}= 0			-1	nA
I_{DL}	Drain leakage current	V_{DS}= -5V V_{BS}= 0	V_{GS}= 0			-20	nA
I_D	Drain current	V_{GS}= V_{DS}= -5V	V_{BS}= 0		-60		mA

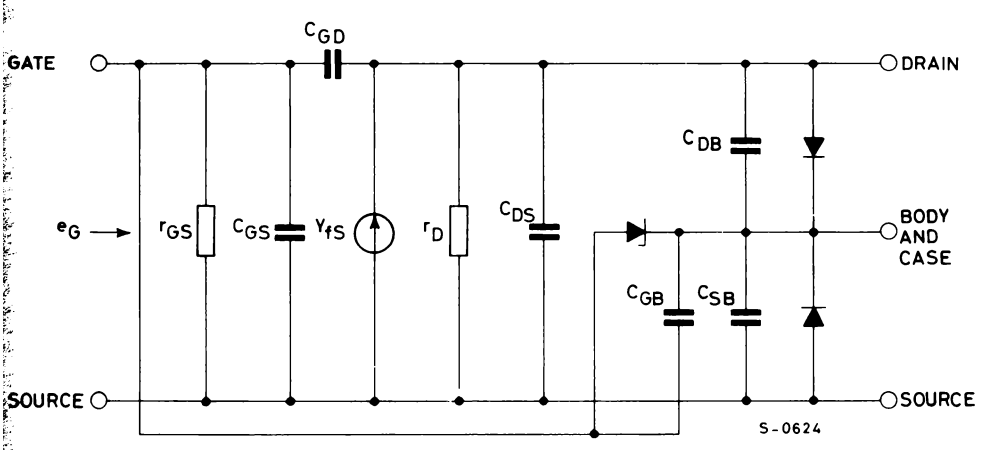
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
Y_{fs}	Forward transadmittance	V_{DS}= -3V V_{BS}= 0V	V_{GS}= -10V		12.000		µmho
C_{DS}*	Drain to source capacitance	V_{DS}= 0 V_{IPP}= 15 mV	f = 1 MHz		0.15	0.20	pF
C_{GD}*	Gate to drain capacitance	V_{GD}=0 V_{IPP}= 15 mV	f = 1 MHz		2	3	pF
C_{GS}*	Gate to source capacitance	V_{GS}= 0 V_{IPP}= 15 mV	f = 1 MHz		2	3	pF
C_{SB}*	Source to body capacitance	V_{SB}= 0 V_{IPP}= 15 mV	f = 1 MHz		8	10	pF
C_{DB}*	Drain to body capacitance	V_{DB}= 0 V_{IPP}= 15 mV	f = 1 MHz		8	10	pF
C_{GB}*	Gate to body capacitance	V_{GB}= 0 V_{IPP}= 15 mV	f = 1 MHz		4	6	pF

* This parameter is periodically sampled and not 100% tested.

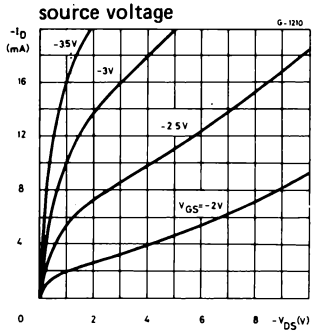
SMALL SIGNAL EQUIVALENT CIRCUIT

(conditions: V_{GS}= -10V, V_{DS}= -3V, V_{BS}= 0) I ≃ 150 mA)

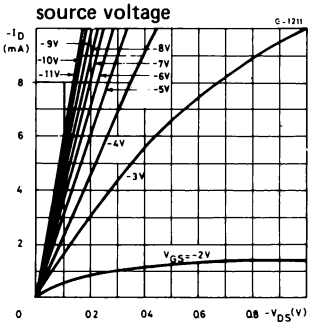


Symbol	Characteristics	Typical values	Unit
Diodes	All diodes are to be considered perfect diodes		
r_{GS}	Gate to source leakage resistance and diode leakage resistance	10^{10}	Ω
r_D	Dynamic drain resistance	0.5	kΩ
C_{GS}	Gate to source capacitance	2	pF
C_{GD}	Gate to drain capacitance	2	pF
C_{DS}	Drain to source capacitance	0.15	pF
C_{GB}	Gate to body capacitance	6	pF
C_{DB}	Drain to body capacitance	40	pF
C_{SB}	Source to body capacitance	10	pF
Y_{fs}	Forward transadmittance	12.000	µmho

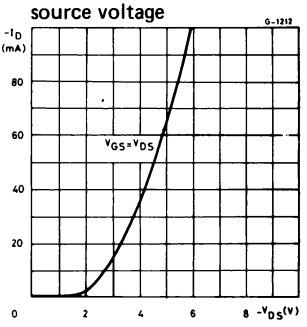
Drain current vs. drain to source voltage



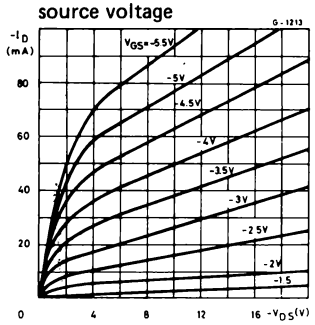
Drain current vs. drain to source voltage



Drain current vs. drain to source voltage

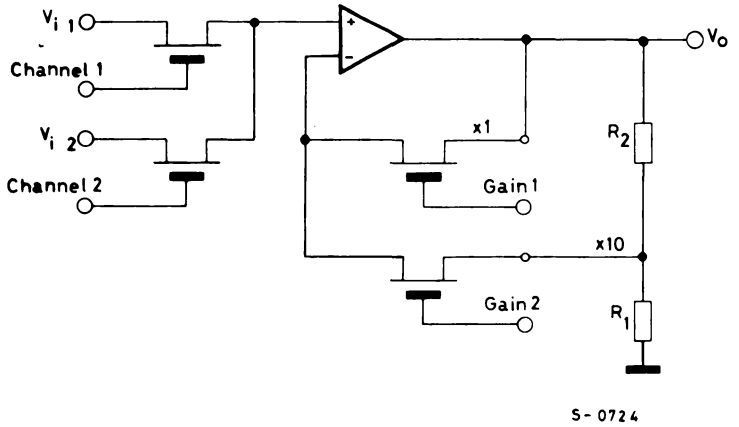


Drain current vs. drain to source voltage



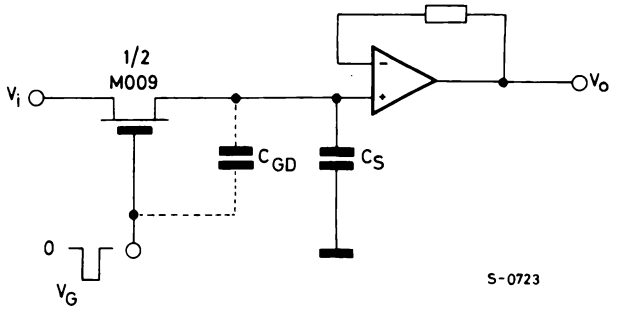
TYPICAL APPLICATIONS

Variable gain amplifier with multiplexed inputs



S-0724

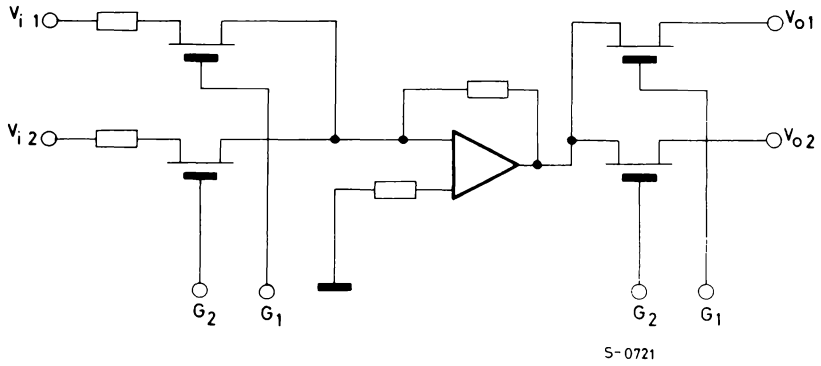
Sample and hold



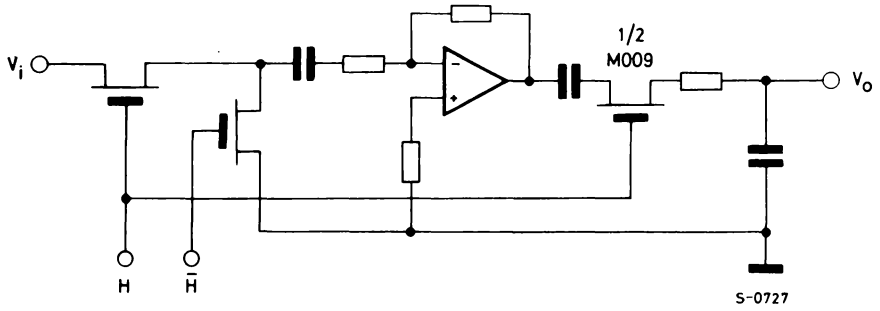
S-0723

TYPICAL APPLICATIONS (continued)

Multiplexing - demultiplexing



Series parallel chopper (low direct voltage amplification)



MOS INTEGRATED CIRCUITS

M 054
M 055

1 OF 16 DECODER

- SPECIFICALLY DESIGNED FOR TV APPLICATION
- MINIMIZATION OF THE EXTERNAL COMPONENTS
- INTERNAL PULL-UP FOR USE WITH LIGHT PRESSURE SWITCHES (M054)
- OPEN DRAIN OUTPUTS FOR TOUCH CONTROL (M055)

The M 054, M 055 are monolithic integrated circuits specifically designed to act as interface between M 1025 (30 channel ultrasonic receiver) and H 580/590 (quad analog switch) in TV applications. The inputs A,B,C,D,E are driven directly from the corresponding outputs of the M 1025. If G input is high the circuits decode the binary combinations from 0 to 15, if G is low the combinations from 16 to 31 are decoded instead. The M 054 has an internal pull-up circuit on the outputs to minimize the number of external components when light pressure switches are used. The M 055 has open drain outputs for touch control applications. The circuits are constructed with N-channel silicon gate technology and are supplied in a 24-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to 20	V
$V_{O(off)}$	Off state output voltage (M 055 type)	20	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

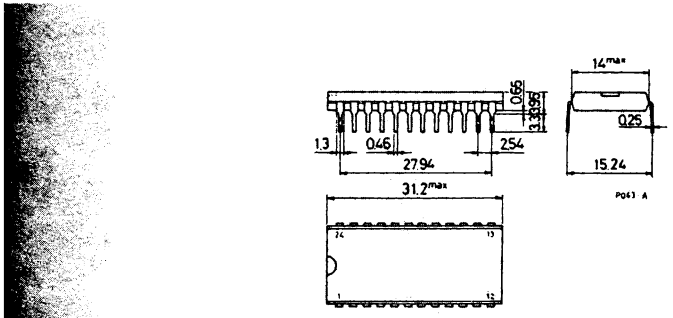
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages values are refered to V_{SS} pin voltage.

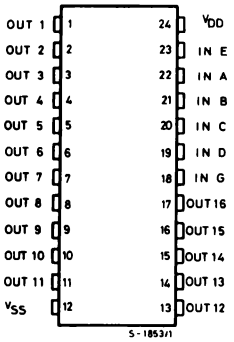
ORDERING NUMBERS: M 054 B1
M 055 B1

MECHANICAL DATA

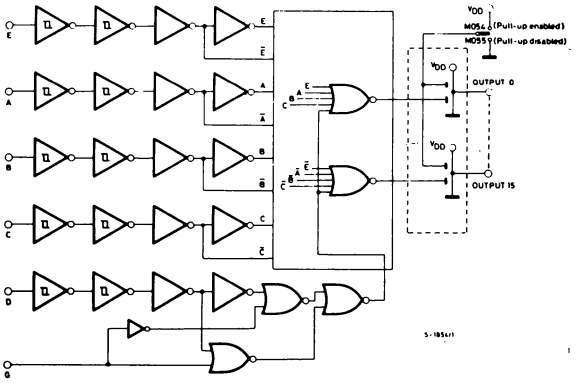
Dimensions in mm



PIN CONNECTIONS



BLOCK DIAGRAM



TRUTH TABLE (positive logic)

INPUTS						OUTPUTS														
M 1025 output code																				
E	A	B	C	D	G	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	0	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
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1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
X	X	X	X	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	17 to 19	V
V_I	Input voltage	0 to V_{DD}	V
$V_{O(off)}$	Off state output voltage (M055 type)	19	V
T_{op}	Operating temperature	0 to 70	°C

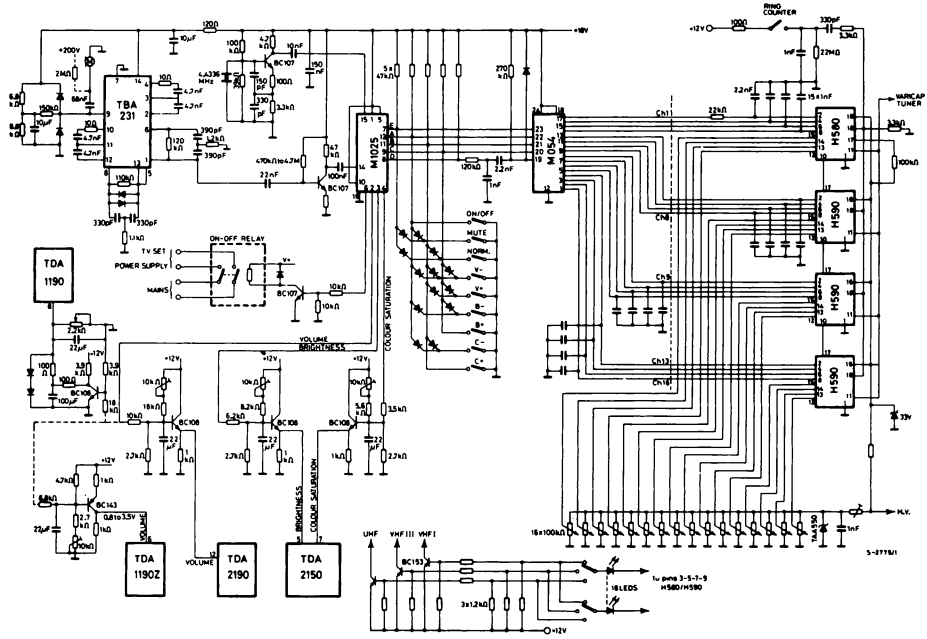
STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions	Values at 25°C			Unit
				Min.	Typ.	Max.	
V_{IH}	High level input voltage	A-B-C-D-E Inputs		V_{DD}-1		V_{DD}	V
		G Input		3		V_{DD}	
V_{IL}	Low level input voltage	A-B-C-D-E Inputs		0		V_{DD}-4	V
		G Input		0		0.3	
I_{OL}	Low level output current		V_{DD}= 17V V_{OL}= 0.4V	1.6			mA
I_{OH}	High level output current (M 055 Type)		M 054 Type V_{DD}= 19V V_{OH}= 8V			-200	µA
$I_{O(off)}$	Off state output current (M 054 Type)		M 055 Type V_{DD}= 19V $V_{O(off)}$= 8V			1	µA
I_{DD}	Supply current		V_{DD}= 19V All input to V_{SS}			25	mA

TYPICAL APPLICATIONS

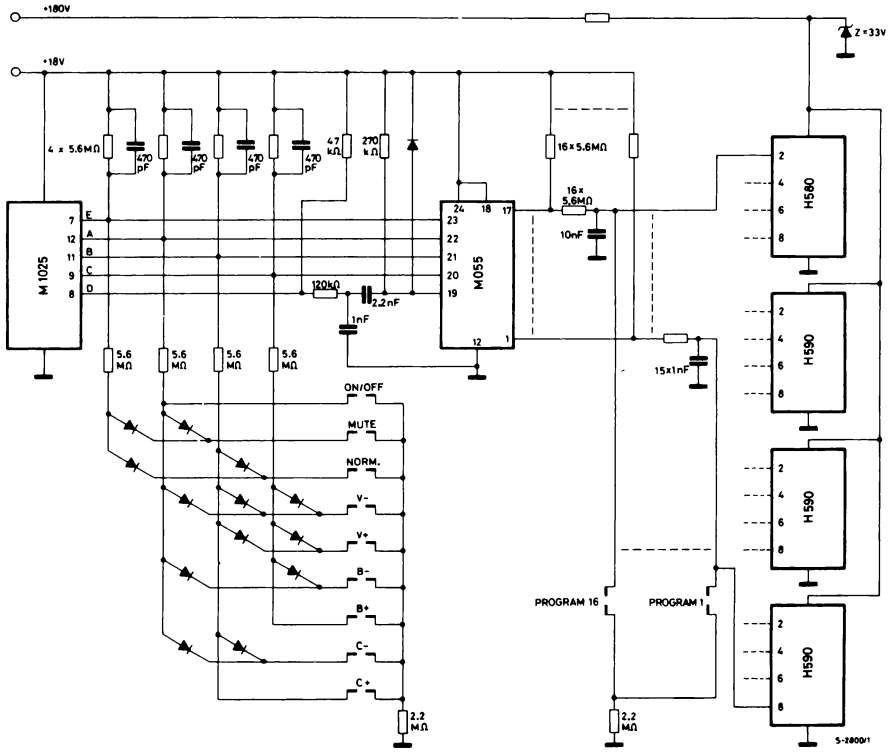
Fig. 1 and 2 show a typical application of M 054 and M 055 respectively in a TV remote control system.

Fig. 1 - M054 with light pressure switches



TYPICAL APPLICATIONS (continued)

Fig. 2 - M055 with direct touch controls



MOS INTEGRATED CIRCUITS

M 082
M 083
M 086

PRELIMINARY DATA

TONE GENERATOR

- M 082 (30% Duty Cycle) 13 TONE OUTPUTS
- M 083 (50% Duty Cycle) 13 TONE OUTPUTS
- M 086 (50% Duty Cycle) 12 TONE OUTPUTS
- SINGLE POWER SUPPLY
- WIDE SUPPLY VOLTAGE OPERATING RANGE
- LOW POWER DISSIPATION < 500 mW
- HIGH OUTPUT DRIVE CAPABILITY
- HIGH ACCURACY OF OUTPUT FREQUENCIES: ERROR LESS THAN ± 0.069%
- INPUT PROTECTED AGAINST STATIC CHARGES
- LOW INTERMODULATION

The M 082, M 083 and M 086 are monolithic tone generators specifically designed for electronic organs. Constructed on a single chip using low threshold N-channel silicon gate technology they are supplied in a 16 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

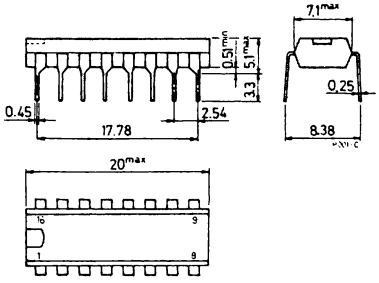
V_I	Voltage on any pin relative to V_{SS} (GND)	+20 to -0.3	V
T_{op}	Operating temperature	0 to 50	°C
T_{stg}	Storage temperature	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS: M 082 B1
M 083 B1
M 086 B1

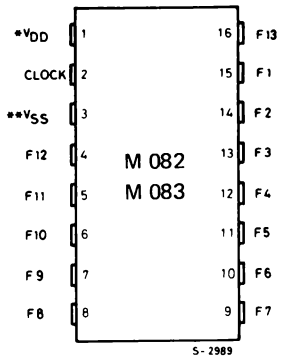
MECHANICAL DATA

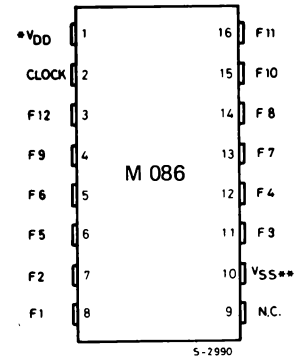
Dimensions in mm



M 082
M 083
M 086

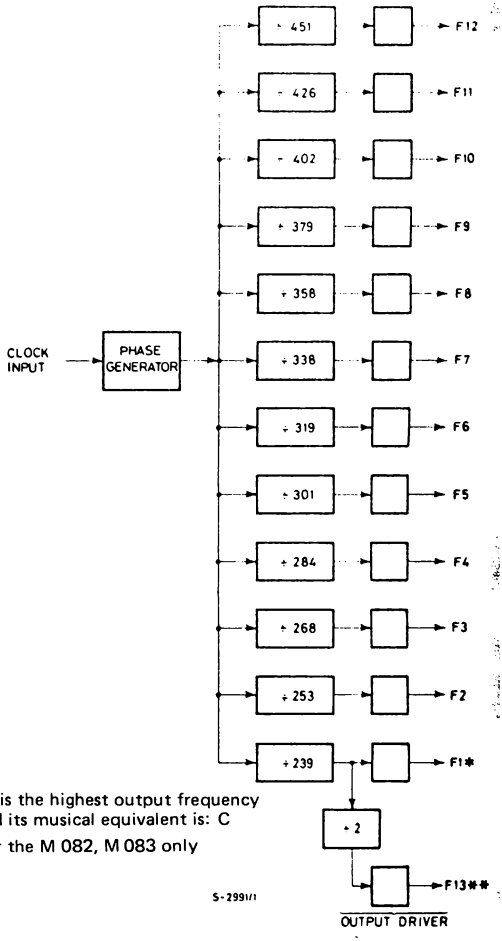
CONNECTION DIAGRAMS





* V_{DD} is the highest supply voltage
** V_{SS} is the lowest supply voltage

BLOCK DIAGRAM



* F1 is the highest output frequency and its musical equivalent is: C
** For the M 082, M 083 only

RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		+10	+12	+14	V

ELECTRICAL CHARACTERISTICS ($0°C \leq T_{amb} \leq 50°C; V_{SS}=0V; V_{DD}=+10V$ to $+14V$ unless otherwise specified)

Parameter		Test conditions	Values			Unit	Fig.
			Min.	Typ.	Max.		
V_{IL}	Input clock, low		V_{SS}		$V_{SS}+1$	V	1
V_{IH}	Input clock, high		$V_{DD}-1$		V_{DD}	V	
t_r, t_f	Input clock rise and fall times 10%to 90%	4.5 MHz			30	ns	1
t_{on}, t_{off}	Input clock on and off times	4.5 MHz		111		ns	1
C_I	Input capacitance			5	10	pF	
V_{OH}	Output high	0.75 mA	$V_{DD}-1$		V_{DD}	V	2
V_{OL}	Output low	0.70 mA	V_{SS}		$V_{SS}+1$	V	2
t_{ro}, t_{fo}	Output rise and fall times 500 pF load		250		2500	ns	3
t_{on}, t_{off}	Output duty cycle	M 082		30		%	
		M 083, M 086		50			
I_{DD}	Supply current			24	35	mA	*
f_I	Input clock frequency		100	4000.48	4500	kHz	

* Output unloaded.

Fig. 1 Input clock waveform

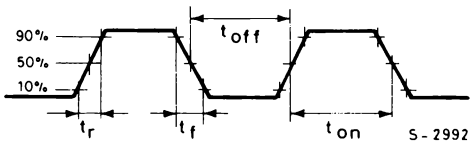


Fig. 2 - Output signal d.c. loading

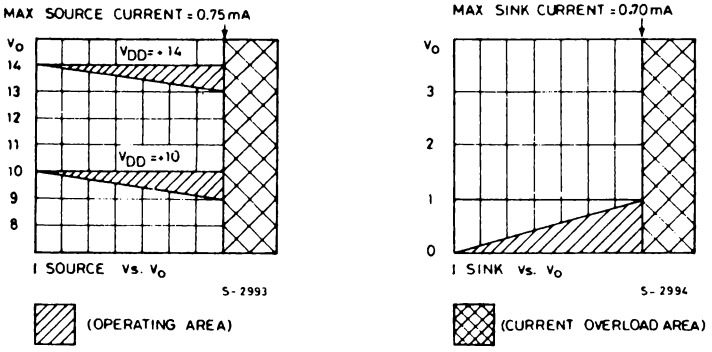
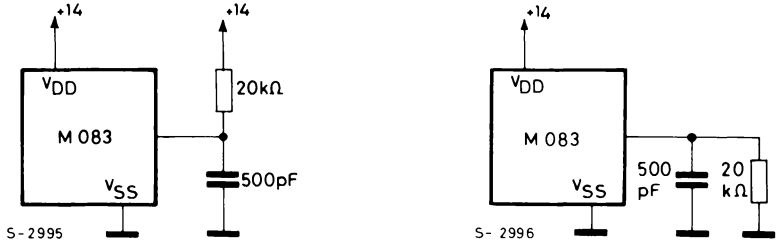


Fig. 3 - Output loading



MOS INTEGRATED CIRCUIT

M 087

TONE GENERATOR

- 12 TONE OUTPUTS TTL COMPATIBLE
- HIGH ACCURACY OF OUTPUT FREQUENCIES: ERROR LESS THAN ± 0.069%
- LOW IMPEDANCE PUSH-PULL OUTPUTS
- LOW POWER DISSIPATION: < 400 mW
- INPUT PROTECTED AGAINST STATIC CHARGES
- LOW INTERMODULATION

The M 087 is a monolithic tone generator specifically designed for electronic organs.
Constructed on a single chip using low threshold P-channel silicon gate technology it is supplied in a 16-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS

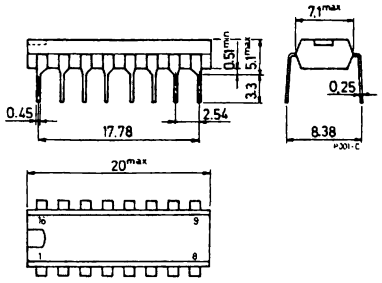
V_{GG} *	Source supply voltage	-20 to 0.3	V
V_i *	Input voltage	-20 to 0.3	V
I_o	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

* This voltage is referred to V_{SS} pin voltage

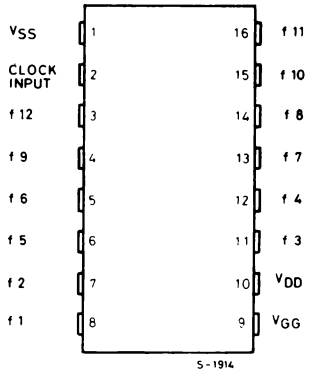
ORDERING NUMBER: M 087 B1 for dual in-line plastic package

MECHANICAL DATA

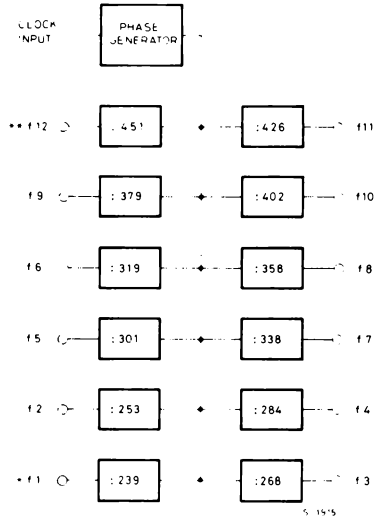
Dimensions in mm



CONNECTION DIAGRAM



BLOCK DIAGRAM



* f1 is the highest output frequency and its musical equivalent is : C
** f12 is the lowest output frequency and its musical equivalent is: C #

STATIC ELECTRICAL CHARACTERISTICS (positive logic, V_{GG}= V_{SS} -16.15 to -18.75V, V_{DD}=V_{SS}-9 to -10V, V_{SS}= 4.75 to 5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

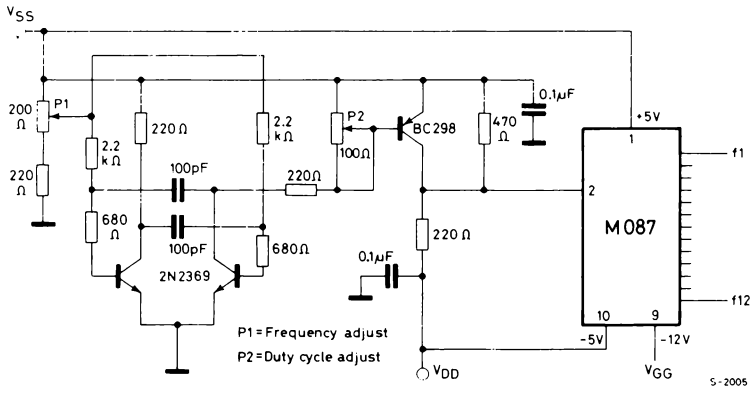
Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK INPUT						
V_{IH}	Clock high voltage		V_{SS}-0.5		V_{SS}	V
V_{IL}	Clock low voltage		V_{SS}-6		V_{SS}-4.5	V
DATA OUTPUTS						
V_{OL}	Output low voltage	I_L= 0 mA	V_{DD}			V
V_{OH}	Output high voltage	I_L= 1 mA	V_{SS}-0.5		V_{SS}	V
I_{LO}	Output leakage current	V_O=V_{SS}-10V T_{amb}= 25°C			10	μA
POWER DISSIPATION						
I_{GG}	Supply current	T_{amb}= 25°C		11	13	mA
I_{DD}	Supply current	T_{amb}= 25°C		13	16	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (positive logic, V_{GG}=V_{SS}-16.15 to -18.75V, V_{DD}=V_{SS}-9 to -10V, V_{SS}= 4.75 to 5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK INPUT						
f	Clock repetition rate		15	2000.24		kHz
t_{pw}*	Pulse width (clock high)	f = 2000.24 kHz	170			ns
t_{pw}**	Pulse width (clock low)		150			ns
DATA OUTPUTS						
R_{DH}	High level output dynamic impedance	V_O=V_{SS}-0.5V		1		kΩ
R_{DL}	Low level output dynamic impedance	V_O= V_{DD}		1		kΩ

* Measured at 90% of the swing.
** Measured at 10% of the swing.

TYPICAL APPLICATION



MOS INTEGRATED CIRCUIT

M 089

PRELIMINARY DATA

2 x 8 CROSS-POINT MATRIX

- VERY LOW ON-RESISTANCE
- HIGH CROSS-TALK AND OFF-STATE-ISOLATION
- SERIAL SWITCH ADDRESSING, MICROPROCESSOR COMPATIBLE

The M089 2x8 cross-point matrix is realized with 16 n-channel MOS transistors. The device has been specially designed to provide switches with low on-reistance. Cross-talk and off-state-isolation are guaranteed less than -90 dBm. The device is designed for PABX applications and is fully microprocessor compatible. It is available in 16 lead dual-in-line plastic and ceramic packages.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.5 to 17	V
V_I	Input voltage pins 4, 5, 12, 13	-0.5 to 17	V
V_{IN}-V_{OUT}	Differential voltage across any disconnected switch	10	V
P_{tot}	Total power dissipation	640	mW
T_{op}	Operating temperature range: for plastic	0 to 70	°C
	for ceramic	-40 to 70	°C
T_{stg}	Storage temperature range	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

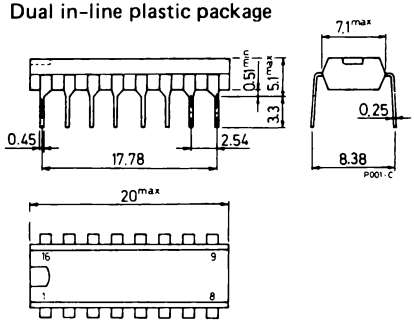
** With respect to V_{SS} (GND) pin.

ORDERING NUMBERS:

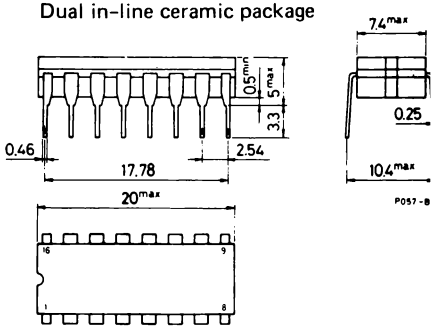
M089 B1 for dual-in-line plastic package
M089 D1 for dual-in-line ceramic package
M089 F1 for dual-in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

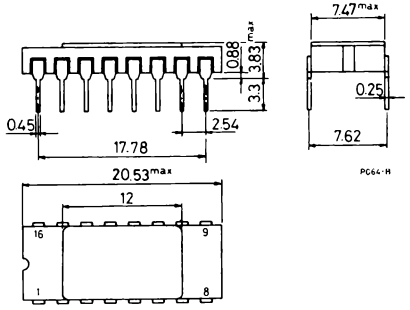
Dual in-line plastic package



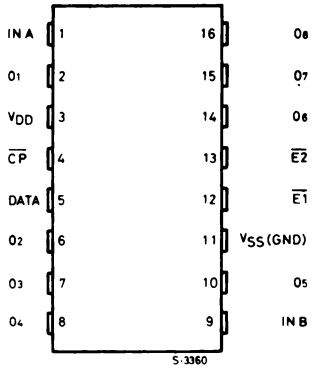
Dual in-line ceramic package



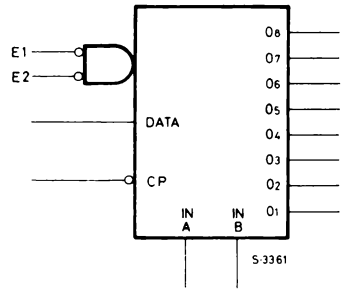
Dual in-line ceramic packege frit-seal



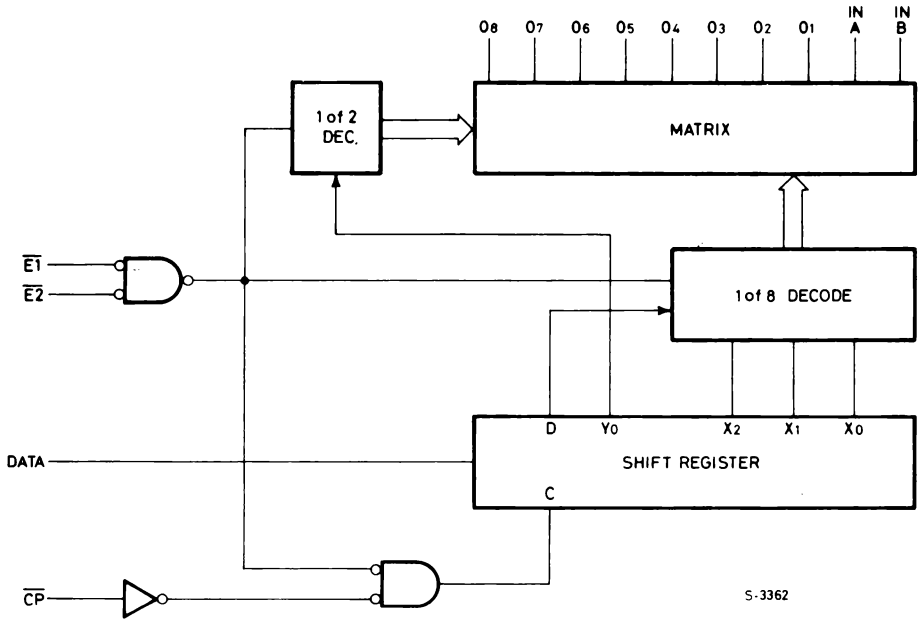
PIN CONNECTIONS



LOGIC DIAGRAM



BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The M089 2x8 cross-point matrix is made up of 16 switches realized with low on-resistance n-channel MOS transistors.

A latch maintains each switch in the previous state. Switches are addressed when both enable inputs $\overline{E1}$ and $\overline{E2}$ are low.

The address is loaded into a 5 bit internal shift register which holds the contents.

D	Y_0	X_2	X_1	X_0

where X_0 to X_2 are used to select 1 of 8 outputs, Y_0 is to select one of two inputs and D defines whether the addressed switch is connected or disconnected.

The data bits are loaded on the high to low transition of the $\overline{CP}$ clock input. The status of the switches is changed on the low to high transition of one or both enable inputs. If more than 5 clock transitions are applied during loading of the shift register, only the last 5 data bits are loaded into the register.

ENABLE INPUTS TRUTH TABLE

$\overline{E1}$	$\overline{E2}$	Function
L	L	data load
		addressed switch changed

DATA INPUT TRUTH TABLE

Data	Switch status
L	disconnect
H	connect

TRUTH TABLE FOR SWITCH SELECTION (positive logic 1 = High, 0 = Low)

The table shows the hexadecimal code for the bits X_0 X_1 X_2 Y_0 which must be loaded to address the inputs and outputs shown.

	0_1	0_2	0_3	0_4	0_5	0_6	0_7	0_8
IN A	F 1111	D 1101	B 1011	9 1001	7 0111	5 0101	3 0011	1 0001
IN B	E 1110	C 1100	A 1010	8 1000	6 0110	4 0100	2 0010	0 0000

For example to address the switch connecting INA to 05 the shift register must be loaded with the address code 0111 (7)

- to connect, D = High (1)
- to disconnect, D = Low (0)

X_0	X_1	X_2	Y_0	D
0	1	1	1	1
0	1	1	1	0

Custom options

There are two possible custom options for the M089 chip. These implement on "all switches reset" function in two ways:

Option 1. The "all switches reset" function could be implemented by an additional data bit in the switch register. The new 6-bit word would be made up as follows.

D	Y_0	X_2	X_1	X_0	R

With R low (0) the circuit would function as previously described with R high (1) all the switches would be disconnected in the low to high transition of one or both of the enable inputs.

Option 2. The function could alternatively be implemented by modifying the enable input truth table as follows.

$\overline{E1}$	$\overline{E2}$	Function
L	L	data load
	L	addressed switch
L		changed
H	H	all switches disconnected

ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C for M089 B1, -40 to 70°C for M089 F1, D1, V_{DD}= 14V to 16V)

Parameter			Test conditions	Values			Unit
				Min.	Typ.	Max.	
R_{ON}	ON-resistance		$V_{i\,(A,\,B)}$= 3.5V $V_{O(1,8)}$= 3.75V V_{DD}= 14V $I_{D(min)}$= 10 mA			25	Ω
I_{DD}	Supply current					7	mA
I_{LI}	Input leakage	pins 4, 5 12, 13	V_i = 5V			1	µA
		pins 1, 9	V_{iA}, V_{iB}= 4.5V V_{O1}, V_{O8}= 1.5V			0.2	µA
		pin 0	V_{iA}, V_{iB}= 6V V_{O1}, V_{O8}= 1.5V			1	µA
I_{LO}	Output leakage	pins 2, 6, 7 8, 10, 14 15, 16	V_{O1}, V_{O8}= 4.5V V_{iA}, V_{iB}= 1.5V			0.2	µA
			V_{O1}, V_{O8}= 6V V_{iA}, V_{iB}= 1.5V			1	µA
V_{low}	Logic 0 input level		All inputs	-0.3		0.8	V
V_{high}	Logic 1 input level		All inputs	4.5		V_{DD}	V
CT	Cross-talk		See fig. 1			-90	dB
I_O	Off insulation		See fig. 2			-90	dB
f_{CL}	Maximum clock input frequency					1	MHz
T_{LG}	Lag time		See fig. 3	100			ns
T_{LD1}	Lead time		See fig. 3	400			ns
T_{LD2}				150			
T_{WR}	Write time		See fig. 3			3	µs
t_W	Clock pulse width		See fig. 3	0.4		100	µs

TEST CIRCUIT

Fig. 1 - Crosstalk measurements

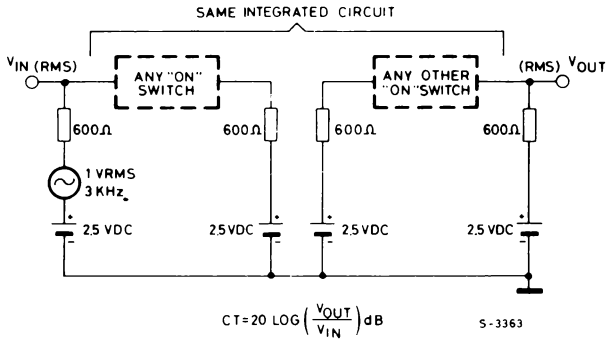
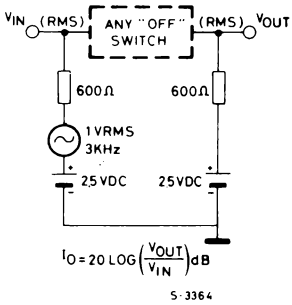
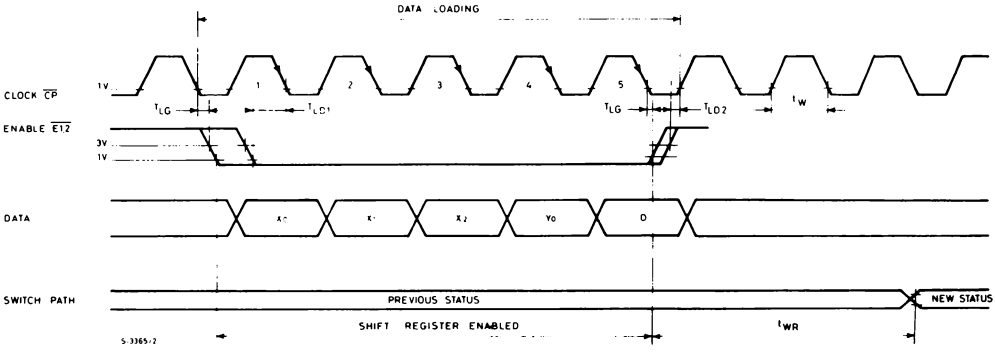


Fig. 2 - Off isolation measureme



TIMING DIAGRAM

Fig. 3



TV MICROPROCESSOR INTERFACE

- 6 PWM D/A CONVERTERS, WITH 64 STEP RESOLUTION, FOR ANALOGUE CONTROLS
- 13 BIT (8192 STEP) PULSE WIDTH-RATE MULTIPLIER D/A CONVERTER FOR TUNING VOLTAGE. BUILT IN ANALOGUE SWITCH.
- CRT DISPLAY SECTION BASED ON A 64 x 64 FULLY PROGRAMMABLE MATRIX, UNDER SOFTWARE CONTROL, WORKS WITH ANY TV STANDARD
- OPEN DRAIN OUTPUTS RATED UP TO 13.2V
- MAIN 5V POWER SUPPLY (12V USED FOR BIAS)
- STANDARD 40 PIN PLASTIC PACKAGE

The M 106 is a programmable LSI device for microprocessor controlled applications in TV and industrial control fields. The M 106 uses state-of-the-art N-Channel MOS Silicon gate technology, with a single +5V power supply and TTL compatible inputs and outputs. A +12V supply is used for bias of the analogue switch circuit built on the chip.
The microprocessor interface includes a single phase clock input, a bidirectional 8 bit system bus, two strobe inputs and an interrupt request output. A total of 7 variable duty cycle output signals are available. After simple RC filtering these signals become the analogue outputs of the system. One blanking and three colour outputs are provided to display alphanumeric or graphic data on a CTV screen. Eight general purpose digital outputs are provided with open-drain configuration.
The M 106 is available in a standard 40 pin dual-in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

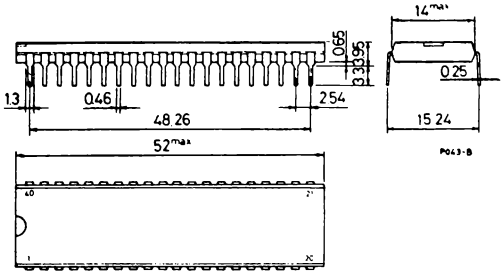
V_{DD} **	Supply voltage	-0.3 to 7	V
V_{ref}	Reference voltage	-0.3 to 7	V
V_{GG}	Bias voltage	-0.3 to 14	V
V_I	Input voltage	-0.3 to 7	V
$V_{O(off)}$	Off-state output voltage: P0 to P6; Q0 to Q7	-0.3 to 14	V
	all other outputs	-0.3 to 7	V
I_O	Output current: all outputs except pins 25, 26, 27, 28	max. 5	mA
	pins 25, 26, 27, 28	max. 15	mA
P_{tot}	Total package power dissipation	0.8	W
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

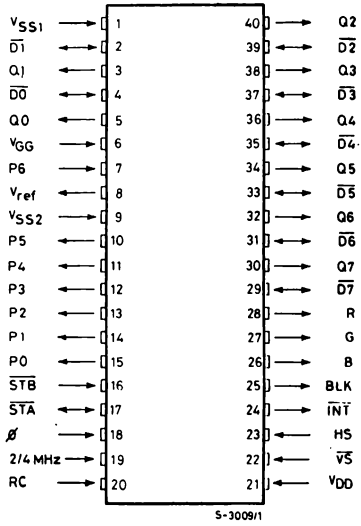
** All voltage are referred to $V_{SS1} = V_{SS2}$.

ORDERING NUMBER : M 106 B1

MECHANICAL DATA (dimensions in mm)



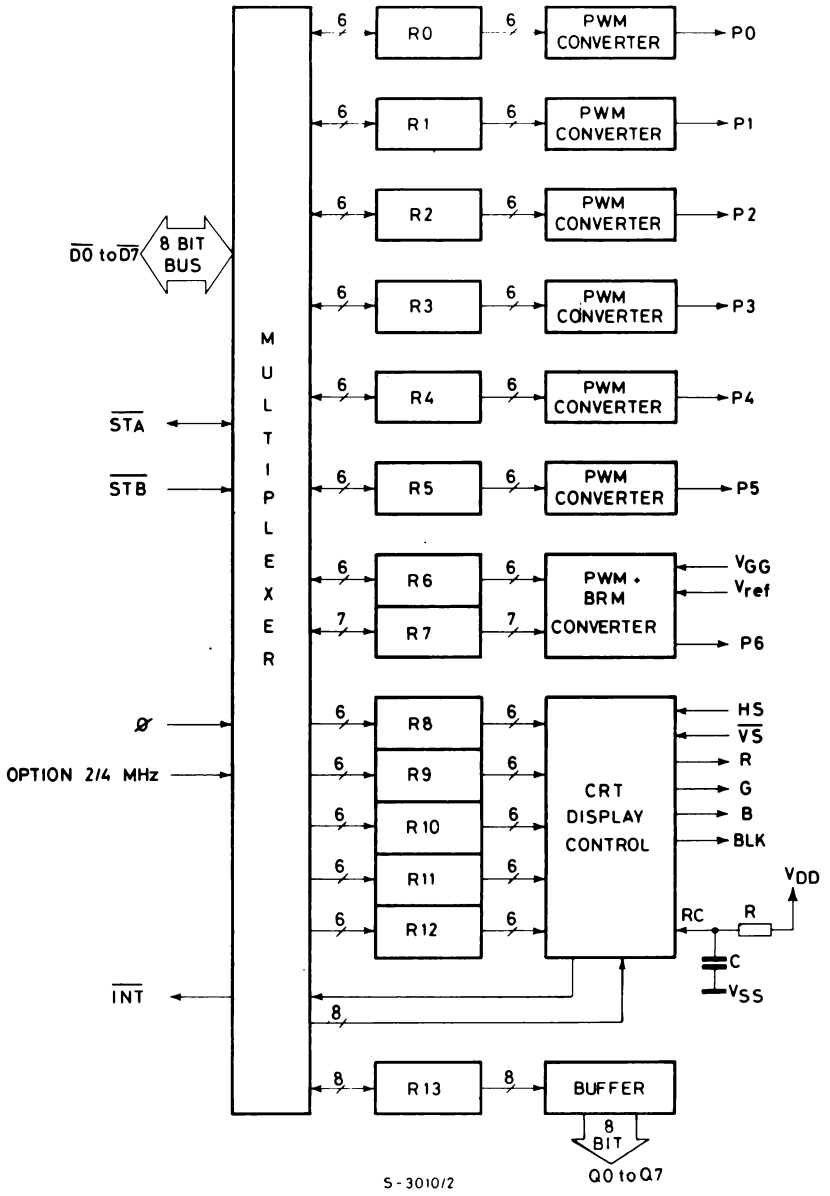
CONNECTION DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	4.5 to 5.5	V
V_{ref}	Reference voltage	5 to 6	V
V_{GG}	Bias voltage	10.8 to 13.2	V
V_I	Input voltage	0 to V_{DD}	V
$V_{O(off)}$	Output off voltage: P0 to P6; Q0 to Q7	max 13.2	V
	all other outputs	max V_{DD}	V
I_O	Output current: all outputs except pins 25, 26, 27, 28	max 2	mA
	pins 25, 26, 27, 28	max 8	mA
ϕ	Clock frequency (selectable)	(pin 19 at V_{DD}) 2	MHz
		(pin 19 at V_{SS}) 4	MHz
f	Oscillator frequency	3.2	MHz
R	Resistance of the clock oscillator	2.2 to 10	kΩ
C	Capacitance of the clock oscillator	10 to 30	pF
T_{op}	Operating temperature	0 to 70	°C

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions

Typ. values are at T_{amb}= 25°C, V_{DD}= 5V; V_{Ref}= 5V; V_{GG}= 12V)

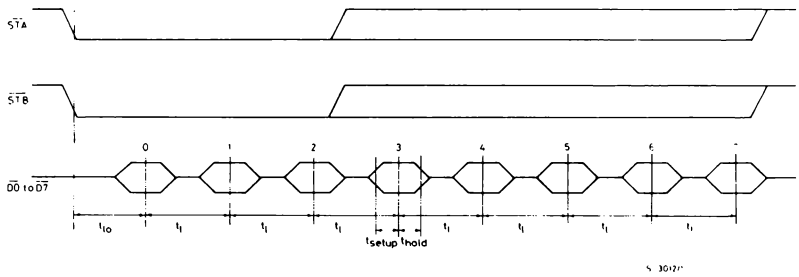
Parameter			Test conditions	Values			Unit
				Min.	Typ.	Max.	
V_{IH}	Input high voltage	All input pins except 22-23 (H_S-$\overline{V}_S$)		2.5		V_{DD}	V
		pins 22-23 (H_S-$\overline{V}_S$)		3		V_{DD}	
V_{IL}	Input low voltage	All inputs excepts pins 22-23 (H_S-$\overline{V}_S$))		0		0.8	V
		pins 22-23 (H_S-$\overline{V}_S$)		0		0.4	
I_I	Input leakage current	All inputs except pin 18	V_I = 0 to 5.5V			10	μA
I_ϕ	Input bias current	pin 18	V_ϕ = 5.5V	10		70	μA
V_{OL}	Output low voltage	All outputs except pins 25-26-27-28-7	I_{OL}= 1.6 mA			0.4	V
		pins 25-26-27-28	I_{OL}= 8 mA			1	V
		pin 7	I_{OL}= 0.25 mA		30	45	mV
V_{OH}	Output high voltage	pin 7	I_{OH}= -0.25 mA		V_{DD}-30	V_{DD}-45	mV
$I_{O(off)}$	Leakage current	All output except pins 3-5-25-26-27-28 30-32-34-36-38-40	$V_{O(off)}$= 5.5V			10	μA
		pins 3-5-25-26-27-28 30-32-34-36-38-40	$V_{O(off)}$= 13.2V			50	μA
I_{DD}	Supply current	pins 3-5-25-26-34	V_{DD}= 5.5V			60	mA
I_{GG}	Bias current		V_{GG}= 13.2V			300	μA

Note: The $\overline{V}_S$ and H_S inputs have Schmitt-trigger action for accepting slow transition time signals.

DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
t_{I0}	Loading time of the first byte from the strobe display command (STA and STB both low)	see fig. 1		26		μs
t_I	Loading time of any successive byte from the end of the previous load time			24		μs
t_{setup}	Setup time			4		μs
t_{hold}	Hold time			4		μs

Fig. 1



DESCRIPTION

ϕ - System clock

The ϕ input (pin 18) must be connected to the microprocessor clock, or to the clock oscillator pin in the case where the microprocessor has a built in clock generator.
The clock signal can be 2 or 4 MHz. Pin 19 must be connected to V_{DD} if the frequency is 2 MHz, to V_{SS} if it is 4 MHz.

Internal registers load and read operations

M 106 can be fully programmed by loading a set of internal registers.
Table 1 shows the binary address code and function of each internal register.
The loading of each register, as shown by fig. 2, is performed in two steps: in the first phase, the four bit address code ($\overline{D0}$ to $\overline{D3}$) is sent on the bus, and latched by the $\overline{STA}$ strobe signal; in the second phase the bus carries the 6 to 8 bit register content which is transferred to the addressed register by the $\overline{STB}$ strobe signal.
When both $\overline{STA}$ and $\overline{STB}$ are in the HIGH state, the content of the addressed register will be read back to the bus. The read operation is not allowed for registers 8 to 12.

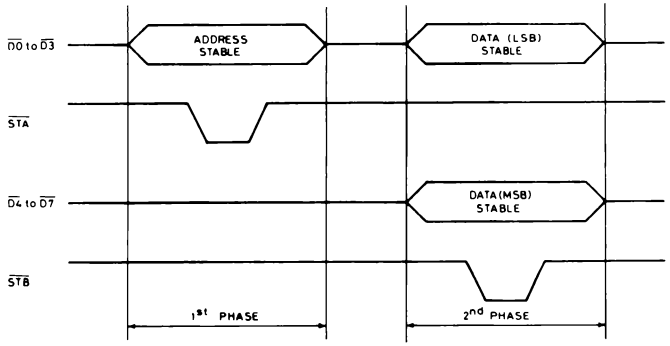
Table 1 - Summary of the internal registers

N°	ADDRESS $\overline{D3}$	$\overline{D2}$	$\overline{D1}$	$\overline{D0}$	Number of bit	Function
0	H	H	H	H	6	Converter n. 0 (PWM)
1	H	H	H	L	6	Converter n. 1 (PWM)
2	H	H	L	H	6	Converter n. 2 (PWM)
3	H	H	L	L	6	Converter n. 3 (PWM)
4	H	L	H	H	6	Converter n. 4 (PWM)
5	H	L	H	L	6	Converter n. 5 (PWM)
6	H	L	L	H	6	Converter n. 6 MSB (PWM)
7	H	L	L	L	7	Converter n. 7 LSB (BRM)
8	L	H	H	H	6	Window upper side position
9	L	H	H	L	6	Window lower side position
10	L	H	L	H	6	Window left side position
11	L	H	L	L	6	Window right side position
12	L	L	H	H	6	CRT display control
13	L	L	H	L	8	Open drain digital outputs
14	L	L	L	H	–	Reset (only for testing)
15	L	L	L	L	–	Not used

Table 2 - Loading and reading of the internal registers

$\overline{STA}$	$\overline{STB}$	Function
H	H	the content of the addressed register is read back (except for R8 to R12)
L	H	address loading
H	L	data loading
L	L	pattern loading for CRT display

Fig. 2



NOTE: TIMING IS NOT CRITICAL; EVERY µP HAS INSTRUCTION CYCLE LARGER THAN MINIMUM SET UP AND HOLD TIMES FOR THE SHOWN OPERATION.

S-3011/2

D/A converters for analogue controls

The 6 bit contents of registers 0 to 5, after a pulse-width conversion and external filtering, are used for analogue commands as volume, brightness, colour saturation, contrast, tone and fine tuning.
The pulse width modulated output has a fixed period of 64 microseconds and variable width. The output is open drain, can be filtered by a simple RC network and can be varied from 0V to the reference voltage (13.2V max) in $2^6 = 64$ steps.

Tuning voltage D/A converter

Registers 6 and 7 may be considered as a single 13 bit register. The corresponding outputs value is normally used as a tuning voltage for a varicap tuner. The conversion uses a double modulation system, in order to minimize the ripple after the filter. The 6 most significant bits (register 6) are converted using the same pulse width modulation technique as registers 0 to 5.
The 7 least significant bits (register 7) generate a series of pulses with variable width and frequency (bit rate multiplier).
This approach greatly reduces the amplitude of the low frequency components in the output voltage, and allows an easier and more efficient filtering.
The converter's output, P6, uses an internal analogue switch, operating in a push-pull mode, and switches a very precise reference voltage, which is connected to the V_{ref} pin.
The 0 volt level, in order to minimize the ground noise, is supplied through a dedicated pin V_{SS2}, that is externally connected to ground.
A 12V bias voltage must be connected to the V_{GG} pin in order to operate the output stage in the push-pull mode.

On screen display

The on-screen display interface uses a vertical sync signal applied to the $\overline{V}_S$ input and horizontal sync signal applied to the H_S input.
A "vertical clock" is internally generated by dividing the line frequency H_S by a number N which defines the height of the matrix element.
Assigning to N a value of 4/5/6 the height of the corresponding matrix element becomes 4/5/6 lines.
The choice of one of these values of N will adapt the M 106 to display on any video standard.
An internal RC oscillator, synchronized by the H_S input, gives a "horizontal clock", whose period

DESCRIPTION (continued)

defines the width of the matrix element. The frequency must be adjusted in order to have a width equal to 1/64th of the actual width of the screen.
The data to be displayed on the screen is normally contained in a rectangular "window". Inside the window the BLK output generates a blanking signal, thus creating a black rectangular background for the image. Position, height and width of the window are programmable by loading in registers 8-9-10-11 a 6 bit position value of each side of the window. The value is calculated in terms of the number of vertical or horizontal clock pulses from an origin.
The origin (0, 0) corresponds to the trailing edge of the $\overline{V}_S$ and H_S pulses and is therefore located in the upper left corner of the screen.
Inside the M 106, a dual 64 bit shift register synchronized by the horizontal clock, repeats the same pattern over N lines using the first shift register, while the μP can load the second one with the new pattern to be used in the next lines. Afterwards the new pattern content is transferred in parallel into the first register. The loading of the second shift register is synchronized by the ϕ clock. This takes 8 sequential bytes, with the timing shown in fig. 1. The loading time for each byte is 24 microseconds.
The loading begins when both $\overline{STA}$ and $\overline{STB}$ go LOW. The corresponding state is decoded as a "strobe display" command.
If the "strobe display" state is terminated by the μP before the internal shift register is completely loaded, the remaining bits are zero-filled.
The display control register (12) defines the start and the end of the display function, the combination of the colour outputs enabled (and therefore the colour of the image) and the timing signals used during the load operation.
Table 3 shows the function of each bit of the display control register.
No timing signals are used if the pattern doesn't change from line to line of the display (vertical or horizontal bands). In this case the pattern can be loaded asynchronously only at the beginning, and will be automatically repeated until the window is completely scanned.
The timing signals must be enabled for displaying character, because the line pattern is variable and must be loaded in synchronism with the screen scan. The $\overline{STA}$ pin, normally used as a strobe input, becomes bidirectional and generates for each frame a single pulse, negative going, and approximately 45 microseconds long, N lines before the beginning of the window.
This signal is used by μP to initiate the first load operation.
The $\overline{INT}$ gives a series of pulses for each frame, with a period of N lines, starting N lines before the beginning of the window and stopping N lines before the end of the window.
During the $\overline{STA}$ output pulse no control register loading is permitted and only the "strobe display" state is accepted.

Table 3 - CRT display control register (N° 12)

Bit	Function	Logic level L	Logic level H
0	Output R (Red)	disabled	enabled
1	Output B (Blue)	disabled	enabled
2	Output G (Green)	disabled	enabled
3	Nr. of lines each dot	5 (4*)	6
4	Timing outputs $\overline{INT}$-$\overline{STA}$	disabled	enabled
5	Display control	stop	start

* Available with metal option (contact local SGS-ATES sales office).

MOS INTEGRATED CIRCUIT

M 108

PRELIMINARY DATA

SINGLE CHIP ORGAN (SOLO + ACCOMPANIMENT)

- SIMPLE KEY SWITCH REQUIREMENTS FOR 61 KEYS, IN A MATRIX OF 12 x 6
- LOW TIME REQUIRED FOR A SCANNING CYCLE OF 576 μsec.
- ACCEPTANCE OF ALL KEYS PRESSED
- TWO KEYBOARD FORMATS: 61 KEYS (SOLO) OR 24+37 KEYS (ACC. + SOLO) WITH POSSIBILITY OF AUTOMATIC CHORDS OF THE "ACCOMPANIMENT" SECTION
- TOP OCTAVE SYTHESIZER INCORPORATED FOR GENERATION OF 3 "FOOTAGES"
- MORE THAN ONE CHIP CAN BE EMPLOYED WITH SYNCHRONIZATION THROUGH THE RESET INPUT
- SEPARATED ANALOG OUTPUTS (FOR EACH FOOT) FOR "SOLO", "ACC." AND "BASS" SECTIONS (SQUARE WAVE 50% D.C.) WITH AVERAGE VALUE CONSTANT
- INTERNAL ANTI-BOUNCE CIRCUITS
- KEY DOWN AND TRIGGER OUTPUTS FOR "SOLO", "ACC." AND "BASS" SECTIONS
- SUSTAIN FOR THE LAST KEYS RELEASED IN THE "SOLO" SECTION (61 OR 37 KEYS)
- CHOICE OF OPERATING MODE IN "ACC." SECTION
  - MANUAL, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEYS (FREE CHORDS WITH ALTERNATE BASS)
  - AUTOMATIC, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEY (PRIORITY TO THE LEFT FOR AUTOMATIC CHORDS AND BASS ARPEGGIO)
- MULTIPLE CHOICE POSSIBILITY ON THE CHORDS IN AUTOMATIC MODE
  - MAJOR OR MINOR THIRD
  - WITH OR WITHOUT SEVENTH
- LOW DISSIPATION OF ⩽ 600 mW
- STANDARD SINGLE SUPPLY OF +12V ± 5%
- INPUTS PROTECTED FROM ELECTROSTATIC DISCHARGES

The M 108 is realized on a single monolithic silicon chip using N-channel silicon gate technology. It is available in a 40 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Source supply voltage	-0.3 to +20	V
V_i **	Input voltage	-0.3 to +20	V
I_o	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

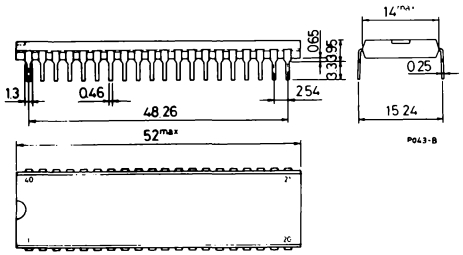
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** This voltage is with respect to V_{SS} (GND) pin voltage.

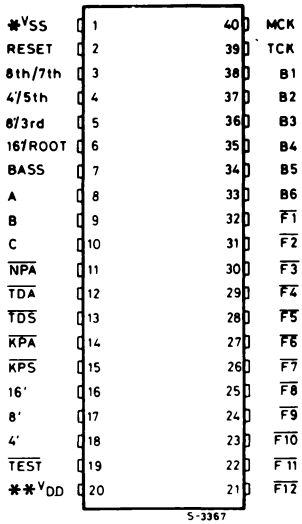
ORDERING NUMBERS: M 108 B1 for dual in-line plastic package

MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package



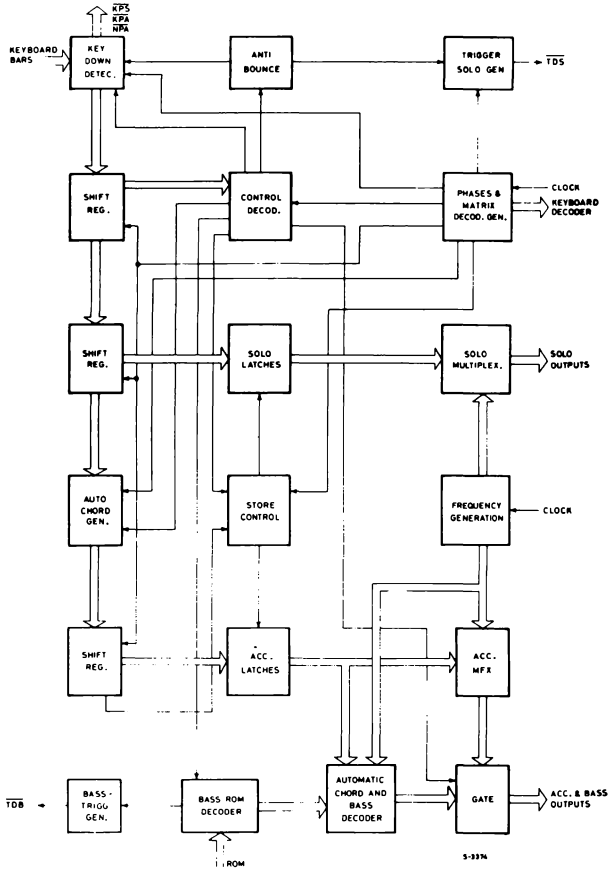
PIN CONNECTIONS



* V_{SS} is the lowest supply voltage

** V_{DD} is the highest supply voltage

BLOCK DIAGRAM



GENERAL CHARACTERISTICS

The circuit comprises:

a) 2 pins for clock input: one for the matrix scanning, the other for the incorporated T.O.S.; by connecting both the clock inputs to the same matrix scanning clock (1000.12 KHz), the three "footages" generated are 16', 8' and 4'.

b) 6 inputs from the octave bars (keyboard and control scanning

c) 3 multiplexed data inputs for addressing the bass selection. These inputs normally come from the outputs of an external memory (negative or positive logic with control inside the chip)

d) 8 signal outputs divided by section: 3 for the "SOLO" section (16', 8', 4'), 4 for the "ACC." section (16' or root, 8' or 3rd, 4' or 5th, 8th/7th according to operating mode), 1 for the bass

e) 12 outputs for the matrix scanning

f) 5 "trigger" and "key down" outputs: $\overline{KPS}$ (key pressed "SOLO"), $\overline{TDS}$ (trigger decay "SOLO"), $\overline{KPA}$ (key pressed "ACC."), $\overline{NPA}$ (pitch present in "ACC." outputs), $\overline{TDB}$ (trigger decay "BASS") respectively. These outputs, in conjunction with an external time constant, allow the formation of the envelope of the sustain and percussion effects. The duration of the trigger pulses is $\cong$ 9 msec.

g) 1 input (reset) to synchronize the device or more than one device (with the same keyboard scanning and using a single contact per key).
The reset action, provided by an external circuit, is of the "POWER ON RESET" (high active) type and its duration must be $\cong$ 0.5 msec.

h) 1 $\overline{TEST}$ pin (in use it must be connected to V_{DD})

i) 2 supply pins.

MATRIX ORGANIZATION (Keyboard and controls)

M 108 Matrix outputs	M 108 Octave bar inputs					
	B_1	B_2	B_3	B_4	B_5	B_6
$\overline{F_1}$	C_1	C_2	C_3	C_4	C_5	C_6
$\overline{F_2}$	C_1#	C_2#	C_3#	C_4#	C_5#	7th OFF/7th ON
$\overline{F_3}$	D_1	D_2	D_3	D_4	D_5	3rd+/3rd-
$\overline{F_4}$	D_1#	D_2#	D_3#	D_4#	D_5#	Sust. OFF/Sust. ON
$\overline{F_5}$	E_1	E_2	E_3	E_4	E_5	$\overline{Latch}$/Latch
$\overline{F_6}$	F_1	F_2	F_3	F_4	F_5	Man/Auto
$\overline{F_7}$	F_1#	F_2#	F_3#	F_4#	F_5#	61/24 + 37
$\overline{F_8}$	G_1	G_2	G_3	G_4	G_5	Antibounce ON/Antibounce OFF
$\overline{F_9}$	G_1#	G_2#	G_3#	G_4#	G_5#	ROM Low/ROM High
$\overline{F_{10}}$	A_1	A_2	A_3	A_4	A_5	--------
$\overline{F_{11}}$	A_1#	A_2#	A_3#	A_4#	A_5#	--------
$\overline{F_{12}}$	B_1	B_2	B_3	B_4	B_5	--------

C_1 is the first key on the left, C_6 is the last key on the right of the keyboard.

The main feature of this chip is the possibility of formating the keyboard either with 61 keys (only "SOLO" without automatism) or separating it into two sections of 24 and 37 keys respectively ("ACCOMPANIMENT + SOLO") with the possibility of chord and bass automatic in the first section.

B) **AUTOMATIC**

The chip recognizes in the "ACC." section only the first on the left of the keys pressed and, according to the setting of the following controls,produces a major or minor chord with or without seventh only the 4' footage but with separated outputs for root, third, fifth and eighth (or seventh if the chord is with seventh).

The bass section gives the bass arpeggio among root, third, fourth, fifth, sixth, seventh and eighth with pitch switching dependent on an external ROM (3 bits).

In automatic mode the two octaves of the "ACC." section inside the chip are connected in parallel both for the chord and for the bass; therefore by pressing anyone of the two keys of the same note the chip generates the same chord.

The "LATCH" control stores the major chord and the bass pitches (until new keys are pressed); the modification of the chord stored (from major to minor, addition of seventh) is always possible by operating the proper controls: by releasing these controls the chord becomes major again.

It is possible to delete the stored pitches both is manual and in "AUTOMATIC" mode by a $\overline{\text{Latch}}$ control signal.

Once again there are $\overline{\text{KPA}}$, $\overline{\text{NPA}}$, and $\overline{\text{TDB}}$ information; however the $\overline{\text{TDB}}$ pulse, which normally appears at each arrival of the ROM codes, does not appear if there are no pitches in the "ACC." (and bass) outputs or, in the case of alternate bass (in manual mode) if the codes indicate conditions of indifference.

RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		11.4	12	12.6	V

STATIC ELECTRICAL CHARACTERISTICS (Positive Logic, V_{DD}=+12V±5%, V_{SS}= 0V, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
INPUT SIGNALS						
V_{IH}	Input high voltage	Note 1	V_{DD}-1		V_{DD}	V
		Note 2	4		18	V
		Note 3	V_{DD}-2		V_{DD}	V
V_{IL}	Input low voltage	Note 1	V_{SS}		V_{SS}+1	V
		Note 2	V_{SS}		V_{SS}+0.6	V
		Note 3	V_{SS}		V_{SS}+2	V
I_{LI}	Input leakage current	V_I= +14V T_{amb}= 25°C			10	µA
LOGIC SIGNAL OUTPUTS						
R_{ON}	Output resistance with respect to V_{SS}			300	500	Ω
R_{ON}	Output resistance with respect to V_{DD}	V_{OUT}= V_{DD}-1 (driver off)		15	25	kΩ
V_{OH}	Output high voltage		V_{DD}-0.4		V_{DD}	V
V_{OL}	Output low voltage			V_{SS}+0.2	V_{SS}+0.4	V
POWER DISSIPATION						
I_{DD}	Supply current	T_{amb} 25°C		30	45	mA
ANALOG SIGNAL OUTPUTS (the external load must be connected to V_{DD}/2)						
I_{OH}	Output current with respect to V_{DD}/2	Outputs loaded with 1 KΩ resistor versus V_{DD}/2	35	50	70	µA
I_{OL}	Output current with respect to V_{SS}	Outputs loaded with 1 KΩ resistor versus V_{DD}/2	-35	-50	-70	µA

Note 1 : Refers only to the clock inputs.
Note 2 : Refers only to the inputs from the external memory.
Note 3 : Refers only to the reset input.

FEATURES

a) The "61/24+ 37" control chooses the keyboard operating mode, i.e. the whole keyboard dedicated to "SOLO" or 24 keys (dedicated) to "ACCOMPANIMENT" and 37 to "SOLO".

b) The "Man/Auto" control, which operates only in case of "ACC.+ SOLO", chooses the manual or the automatic accompaniment.

c) The "Sust OFF/Sust ON" allows the storage of the "SOLO" section and handles the whole keyboard or 37 keys depending on the operating mode.

d) The "$\overline{\text{Latch}}$/Latch" similarly allows the storage of the "ACC." section and operates in "ACC.+ SOLO" only.

e) The "3rd+/3rd-" which operates only in case of "ACC.+ SOLO" and "AUTOMATIC", changes the automatic chord generated from major to minor or viceversa.

f) The "7th OFF/7th ON" adds the seventh to the automatic chord generated.

g) The "Antibounce ON/Antibounce OFF" disables the antibounce circuit which is usually enabled.

h) The "ROM Low/ROM High" selects between ROMs with return to "1" (Low active) or with return to "0" (High active). Usually the chip is enabled for ROMs with return to "1" (Low active).

"SOLO" Operation

In this case the chip recognizes the whole keyboard as "SOLO" and does not read the controls which concern the "ACC.+ SOLO" operation.
The chip identifies all the keys pressed and transfers to the outputs of each section (24 and 37 keys) the analog sum of corresponding pitches.
The outputs are current generators with average value constant, therefore it is sufficient to connect the pins to one load and send the signals on to the filters.
In the case of "Sustain OFF" each new key pressed or released is accepted or deleted in a time $\leqslant 576\ \mu$sec.
In the case of "Sustain ON" the chip has a different operation according to whether the new key (keys) is pressed or released: each new key pressed is always accepted in a time $\leqslant 576\ \mu$sec., whereas each key released is deleted with a delay of 73 msec. and only if there are still keys pressed.
In fact, if after the 73 msec. there are no keys pressed, the last key (or keys) released remains stored until new keys are pressed.
In this mode it is possible to have Sustain, with external envelope shaping, for the last keys (or key) released.
The pitch envelope is controlled by a D.C. signal $\overline{\text{KPS}}$ (any key pressed) and there is also an A.C. signal $\overline{\text{TDS}}$ (trigger decay "SOLO") which provides a pulse whenever a key is pressed.
An appropriate antibounce circuit, inside the chip, solves the problems associated with the keyboard contacts.

"SOLO + ACCOMPANIMENT" Operation

In this case the chip identifies the "ACCOMPANIMENT" on the first 24 keys on the left, and the "SOLO" on the remaining 37 keys and reads all the controls which concern the "ACC." section.
The "SOLO" function is identical to "61 keys" mode, but for the "ACC." section there are two possibilities:

A) **MANUAL**
The chip identifies which keys are pressed in the "ACC." section, and transfers to the "ACC." outputs the analog sum of the corresponding pitches.
The "ACC." section is fully independent of the "SOLO" section and the signals (if there is no "LATCH") remain at the output only while the keys are pressed even if there is "SUSTAIN ON".

The "BASS" section gives at the bass output an alternating bass between the first on the left and the first on the right of the keys pressed in the "ACC." section; the pitch switching timing is dependent on an external ROM (3 bits).
The "LATCH" control stores the last keys released and the output signals, including the bass output, remain until new keys are pressed.
The $\overline{TDB}$ (trigger decay "BASS") output gives a pulse corresponding to every output change; there are also two D.C. signals, $\overline{KPA}$ (any key pressed accompaniment) and $\overline{NPA}$ (pitches in output accompaniment) relative only to the "ACC." section.
The first of these signals (analogous to $\overline{KPS}$) concerns the keyboard and does not consider the "LATCH" condition.
The second on the contrary concerns the "ACC." output and considers the "LATCH" condition.

BASS TRUTH TABLES

NEGATIVE LOGIC

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
1	1	1	No change	No change
1	1	0	Root	1st on the left
1	0	1	3rd	– – –
1	0	0	4th	– – –
0	1	1	5th	1st on the right
0	1	0	6th	– – –
0	0	1	7th	– – –
0	0	0	8th	– – –

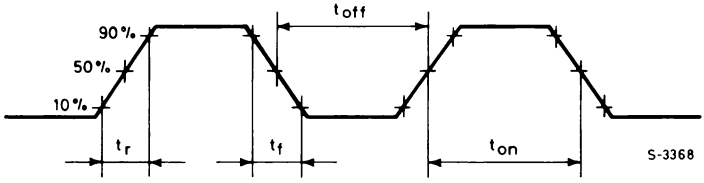
POSITIVE LOGIC

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
0	0	0	No change	No change
0	0	1	Root	1st on the left
0	1	0	3rd	– – –
0	1	1	4th	– – –
1	0	0	5th	1st on the right
1	0	1	6th	– – –
1	1	0	7th	– – –
1	1	1	8th	– – –

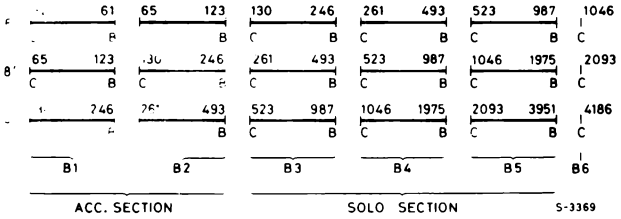
DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
MASTER CLOCK INPUT						
f_i	Input clock frequency			1000.12		KHz
t_r, t_f	Input clock rise and fall time 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	1000 KHz		500		ns
T.O.S. CLOCK INPUT						
f_i	Input clock frequency		100	1000.12	2500	KHz
t_r, t_f	Input clock rise and fall times 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	2000 KHz		250		ns
$\overline{TDS}$ and $\overline{TDB}$ OUTPUTS						
t_{on}	Pulse duration	1000 KHz		9.216		ms
t_r, t_f	Outputs rise and fall times 10% to 90%	1000 KHz		100		ns

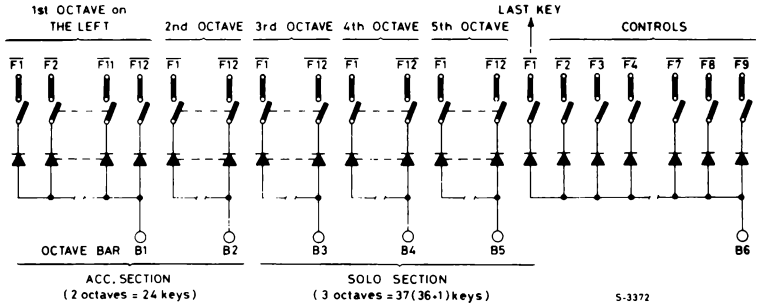
INPUT CLOCK WAVEFORM



FREQUENCY RANGE OF EACH OCTAVE (16', 8', 4' footages)

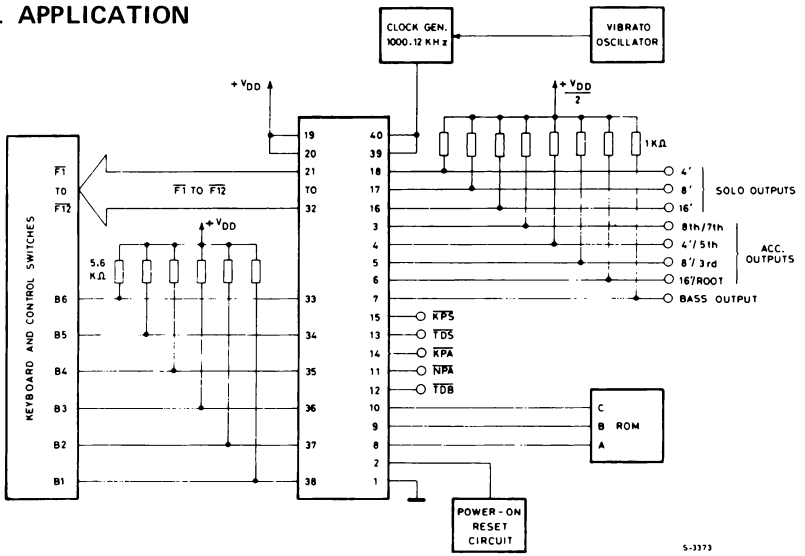


CONNECTION OF THE KEYBOARD AND CONTROL SWITCHES

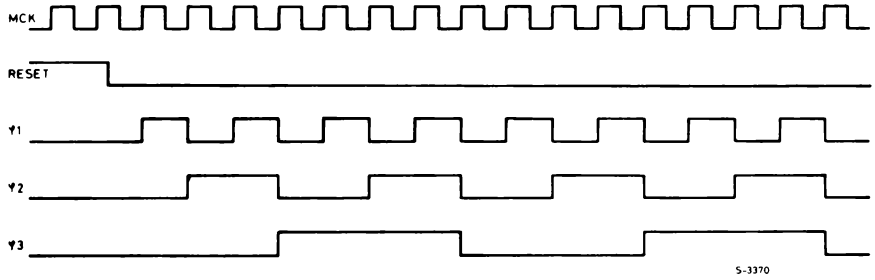


Note: The switch "OPEN" corresponds to "KEY NOT PRESSED" or "CONTROL IN THE FIRST CONDITION" (see the drawing "MATRIX ORGANIZATION").

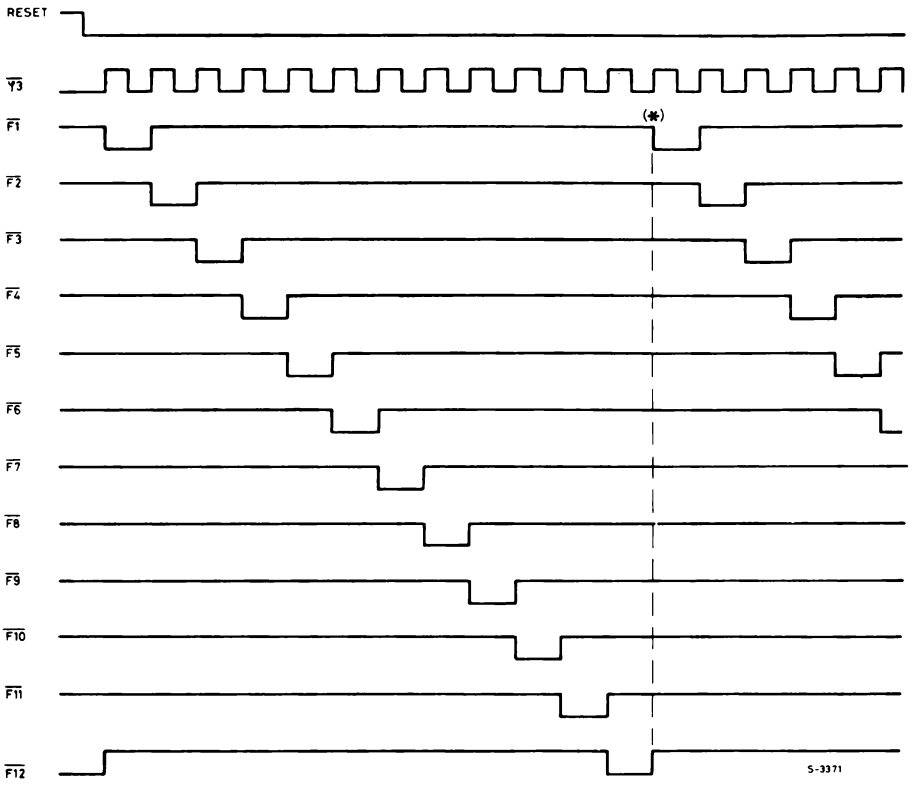
TYPICAL APPLICATION



TIMING DIAGRAMS



Note: MCK is the master clock input (matrix scanning), $\varphi 1$, $\varphi 2$, $\varphi 3$ are internal phases to generate $\overline{F1} \div \overline{F12}$.



Note: The matrix scanning starts (after the power on reset) at the second arrival in output of $\overline{F1}$ (*) from B1 to B6 in continuous sequence.

PRELIMINARY DATA

1024 BIT - NON VOLATILE RANDOM ACCESS MEMORY

- 256 x 4 ORGANIZATION, FULLY DECODED
- OPERATING MODES: READ, MODIFY
- MODIFY MODE PERFORMS SIMULTANEOUS WRITING AND ERASURE ON THE ADDRESSED WORD
- INPUT LATCHES FOR ADDRESSES AND DATA IN
- OUTPUT DATA LATCHED
- ACCESS TIME: M 120-2: 450 ns — M 120: 700 ns
- WORD MODIFY TIME: LESS THAN 100 msec. END OF MODIFY OPERATION IS INDICATED BY A FLAG (MODIFY END)
- 10^4 MODIFY CYCLES PER WORD
- DATA RETENTION ONE ORDER OF MAGNITUDE HIGHER THAN MNOS TECHNOLOGY
- N-CHANNEL, SI-GATE, DOUBLE POLY-SILICON MOS TECHONOLOGY
- TTL-COMPATIBLE, OPEN DRAIN OUTPUTS
- POWER SUPPLY V_{DD}= 12V ± 10% , V_{PP}= 25V ± 5%
- LOW POWER CONSUMPTION: 300 mW PEAK POWER FROM V_{PP} (DURING WRITE OPERATION ONLY)
  350 mW ACTIVE POWER FROM V_{DD}
  STANDBY POWER LESS THAN 100 mW

The M 120 is a non volatile memory which the user can consider as a RAM with a fast access time and an much slower write cycle.The device operates with an address strobe control ($\overline{AS}$) and has no limit on the maximum period of $\overline{AS}$. The $\overline{AS}$ control performs the Chip Select (CS) function as well; the device is de-selected (standby mode) by a high level on $\overline{AS}$. Both read and modify cycles begin on the falling edge of $\overline{AS}$; if R/$\overline{W}$ remains true, while $\overline{AS}$ is active, a read cycle occurs; if, instead, R/$\overline{W}$ is false while $\overline{AS}$ is active a modify cycle starts. Data on the data bus are latched during the rising edge of R/$\overline{W}$, then an internal circuitry performs a comparison between "old", and "new" data and, according to the result, writes or erases or leaves unchanged each single bit of the word. If writing is necessary on one bit and an erasure on another, both operations are performed simultaneously. After the rising edge of R/$\overline{W}$, addresses and data are latched internally and no external holding is necessary during the modify time. Since modify time lengthens during the device lige, the "modify end" control, which outputs a high level at the end of the cycle, can be used to speed up system operations. As long as ME is low the device is internally disconnected from buses and controls. The device is available in 18-lead dual in-line ceramic package (metal seal) and ceramic package (frit seal).

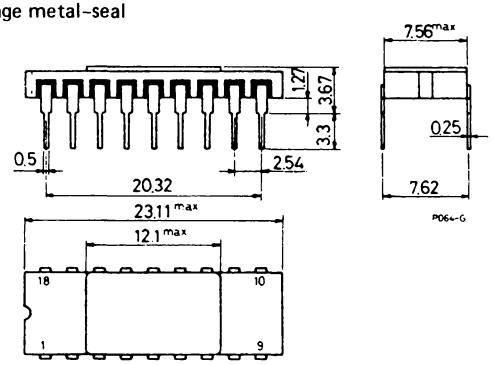
ABSOLUTE MAXIMUM RATINGS

V_I	Input voltage	-0.5 to 20	V
P_{tot}	Total power dissipation	0.5	W
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

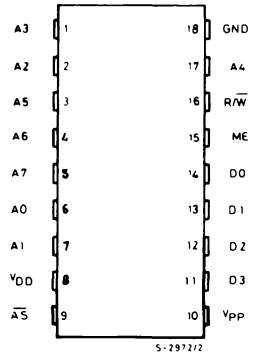
ORDERING NUMBERS: M 120 F1 for dual in-line ceramic package (frit seal)
M 120 D1 for dual in-line ceramic package (metal seal)
M 120-2 F1 for dual in-line ceramic package (frit seal)
M 120-2 D1 for dual in-line ceramic package (metal seal)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package metal-seal



PIN CONNECTIONS



DC AND OPERATING CHARACTERISTICS (T_{amb} = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{PP} = 25V ± 5%)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{DD1}	V_{DD} supply current				30	mA
I_{PP1}	V_{PP} supply current				12	mA
I_{DD2}	Standby V_{DD} supply current				10	mA
I_{PP2}	Standby V_{PP} supply current				5	mA
V_{IH}	Input high voltage		2.4	5		V
V_{IL}	Input low voltage		-0.3	0	0.6	V
V_{OL}	Output low voltage	I_L = 1.6 mA			0.4	V
I_{LI}	Input load current				10	µA
I_{LO}	Output leakage current				10	µA

AC CHARACTERISTICS

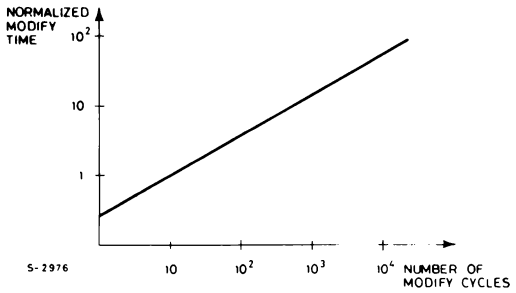
Parameter		M 120-2		M 120		Unit
		Min.	Max.	Min.	Max.	
t_{ACC}	Access time from address strobe		450		700	ns
t_{ASL}	Address strobe active time	450		700		ns
t_{ASH}	Address strobe inactive time	160		300		ns
t_{OFF}	Output buffer turn-off delay		100		150	ns
t_s	Set-up time		20		40	ns
t_h	Hold time		80		150	ns
t_{WR}	Write time (1)	2	100	2	100	ms
t_{D1}	$\overline{AS}$ to R/$\overline{W}$ delay (2) (3) (4)	100	350	200	600	ns
t_P	Modify pulse width (3) (4)	200		300		ns
t_{SW}	R/$\overline{W}$ to $\overline{AS}$ rising edge	200		300		ns
t_{D2}	ME turn-on delay		100		200	ns

Notes:
1) $t_{WR\ max}$ is 2 ms for the first 10 modify cycles and increases to 100 ms according to Figure 1.
2) R/$\overline{W}$ is internally disabled up to $t_{D1\ min}$ but can change before $t_{D1\ min}$ and even before the falling edge of $\overline{AS}$.
3) If $t_{D1} \leq t_{D1\ max}$ then D_{OUT} remains floating and there is no conflict between D_{OUT} and D_{IN}; in this mode, D_{IN} can be stable within $t_{ASL\ min}$; otherwise it must be

$$t_P \ t_{OFF} + t_{tr} + t_s$$

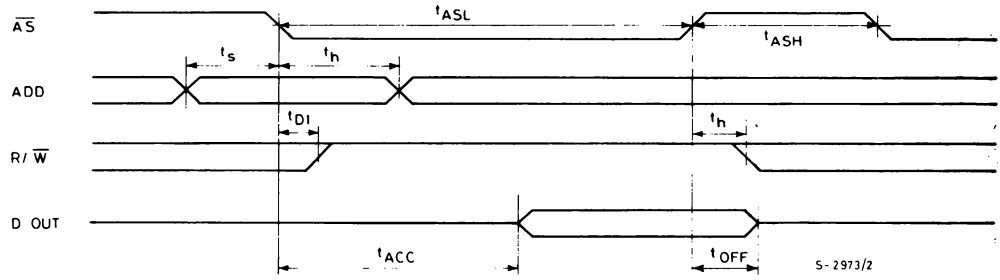
where
t_{tr} is the transition time for the data bus.
4) It must be $t_P + t_{D1} \geq t_{ASL\ min}$.

Fig. 1 - Plot of modify time vs. number of modify cycles

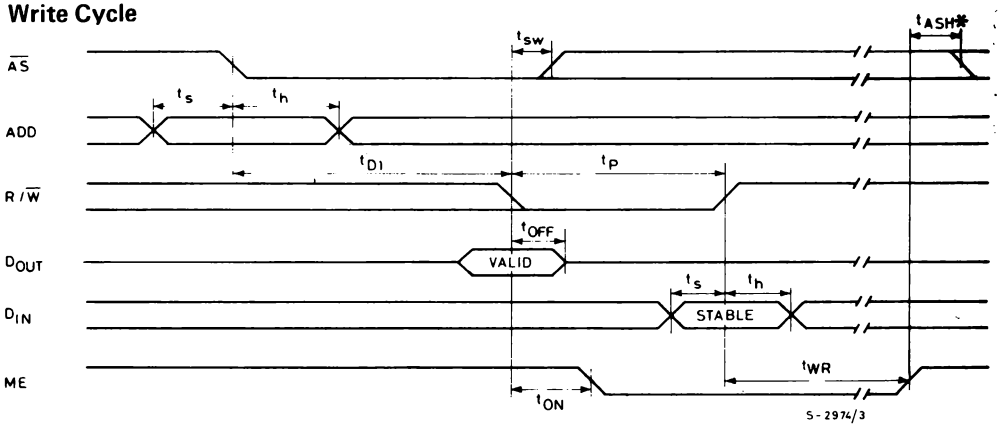


TIMING WAVEFORMS

Read Cycle



Write Cycle



* The first negative edge of $\overline{AS}$ following the end of a modify cycle must commence at least t_{ASH} after the positiv edge of ME.

QUAD 80-BIT STATIC SHIFT REGISTER

- SINGLE VOLTAGE SUPPLY: $V_{CC} = 5V \pm 5\%$
- DC to 3 MHz OPERATION GUARANTEED
- FULLY TTL COMPATIBLE
- FULLY DC OPERATION
- SINGLE LINE CLOCK
- PIN-FOR-PIN REPLACEMENT for MK 1007P-TMS 3409 - 2532 - 3347
- LOW POWER DISSIPATION: 250 mW (TYP.)
- INPUT GATE PROTECTION
- M142A IS A HIGH SPEED SELECTION

The M142 and M142A are quad 80-bit fully DC shift register constructed on a single chip using very low threshold N-channel silicon gate technology which allows high speed (3 MHz guaranteed) and fully TTL compatibility without using any external resistor.
Each of the four 80-bit registers has an independent input, output and recirculate control. The single clock line is common to all four registers.
Transferring data into the register is accomplished when the clock is high (logic "1") Shifting of data occurs when the clock goes low. Output data appears on the negative going edge of the clock.
When the recirculate line is high, data recirculates, while input is inhibited. When data is entered, the recirculate line is at logic "0".
Output data attain the same logic state that was shifted into the register 80 clocks prior. Available in 16-lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{CC}	Supply voltage	-0.5 to 7	V
V_I	Input voltage on any pin	-0.5 to 7	V
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

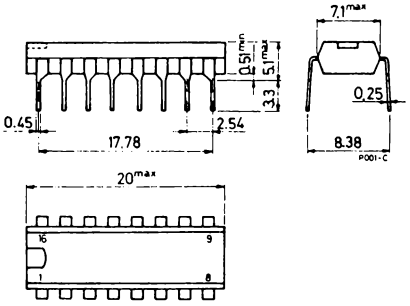
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS:

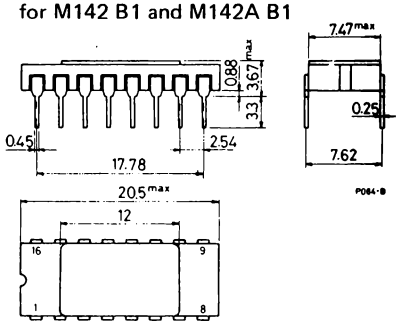
M142 B1 for dual in-line plastic package
M142 D1 for dual in-line ceramic package
M142A B1 for dual in-line plastic package
M142A D1 for dual in-line ceramic package

MECHANICAL DATA (dimensions in mm)

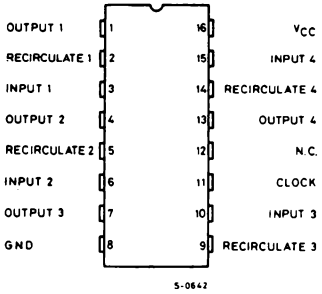
Dual in-line plastic package
for M142 D1 and 142A D1



Dual in-line ceramic package
for M142 B1 and M142A B1

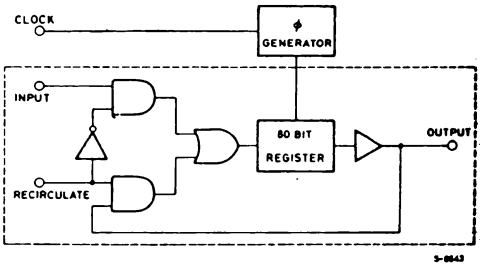


PIN CONNECTIONS



BLOCK DIAGRAM

(one of four shown)



TRUTH TABLE
(positive logic)

Recirculate	Input	Function
"0"	"0"	"0" is written
"0"	"1"	"1" is written
"1"	"0"	Recirculate
"1"	"1"	Recirculate

"0" = 0V, "1" = 5V

STATIC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ± 5%, T_{amb}= 0 to 70°C unless otherwise specified)

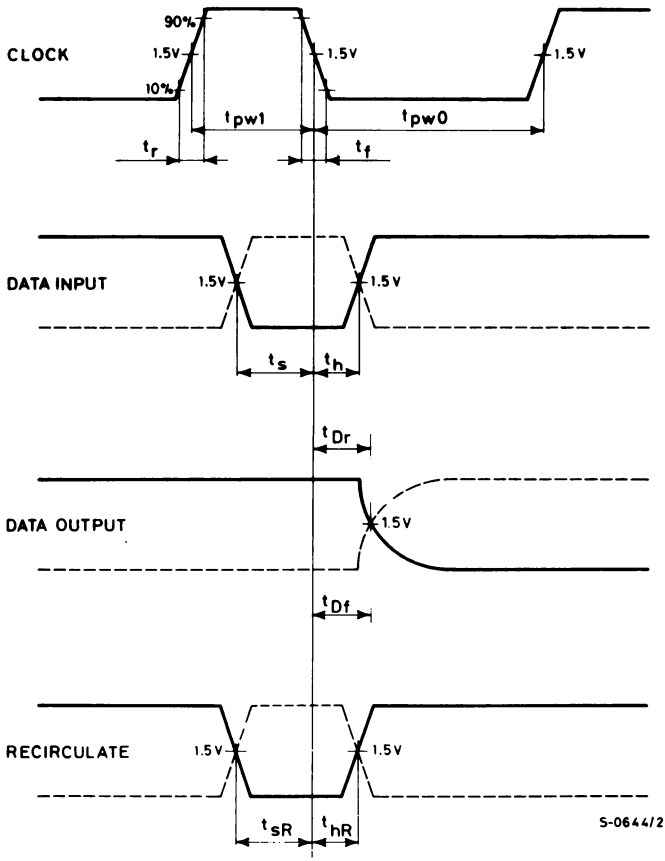
Parameter		Test conditions	Values**			Unit
			Min.	Typ.	Max.	
V_{IH}*	Input high voltage		2		V_{CC}	V
V_{IL}*	Input low voltage		-0.3		0.8	V
V_{OH}	Output high voltage	I_{OH}= -100 μA	2.4			V
V_{OL}	Output low voltage	I_{OL}= 1.6 mA			0.4	V
I_{LI}*	Input leakage current	$V_i = V_{CC}$			10	μA
I_{CC}	Supply current			48		mA

* These parameters apply to all inputs including clock.
** Typical values at T_{amb}= 25°C and V_{CC}= 5V.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ± 5%, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
f	Clock repetition rate					3	MHz
$t_{\phi\,pw1}$	Clock high pulse width			110			ns
$t_{\phi\,pw0}$	Clock low pulse width			220			ns
t_r, t_f	Clock rise and fall time					5	μs
t_{setup}	Setup time			100			ns
t_{hold}	Hold time			80			ns
t_{sR}	Recirculate setup time			100			ns
t_{hR}	Recirculate hold time			80			ns
t_{Dr}, t_{Df}	Delay time to rise and fall	TTL load C_L= 10 pF	for **M142** type for **M142A** type			230 160	ns ns
C_{iR}	Recirculate input capacitance	V_i = 0V	f = 1 MHz			8	pF
C_ϕ	Clock capacitance	V_ϕ= 0V	f = 1 MHz			12	pF

WAVEFORMS


CLOCK
90%
1.5V
10%
1.5V
1.5V
tpw1
tpw0
tr
tf
DATA INPUT
1.5V
1.5V
ts
th
tDr
DATA OUTPUT
1.5V
tDf
RECIRCULATE
1.5V
1.5V
tsR
thR
S-0644/2

MOS INTEGRATED CIRCUIT

M 147

13-BIT LATCH PEDAL SUSTAIN

- PRIORITY OF THE FIRST LEFT PEDAL
- PRIORITY PEDAL FREQUENCY MEMORIZATION
- TRIGGER OUTPUT FOR ENVELOPE CIRCUITS
- CHOICE BETWEEN TWO DIFFERENT INPUT FREQUENCIES (2.00024 MHz or 500.06 kHz)
- ANTIBOUNCE INTERNAL CIRCUIT ON BOTH TOUCH AND RELEASE SITUATION
- STANDARD POLYPHONIC KEYBOARDS
- P-CHANNEL SILICON GATE PROCESS

The M 147 is a monolithic integrated circuit for pedal sustain specifically designed for electronic organs and other musical instruments.
Constructed on a single chip using P-channel Silicon Gate technology it is supplied in a 24-lead dual in line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{GG}**	Source supply voltage	-20 to 0.3	V
V_I**	Input voltage	-20 to 0.3	V
I_O	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

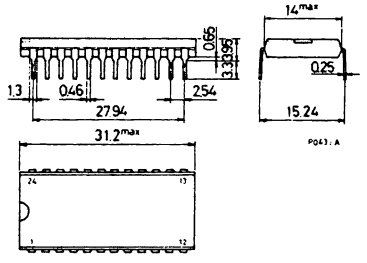
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltage values are referred to V_{SS} pin voltage.

ORDERING NUMBER: M 147 B1

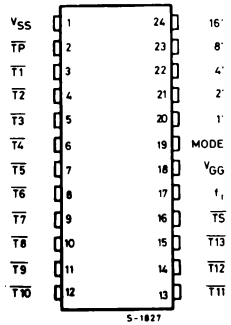
MECHANICAL DATA

Dimensions in mm

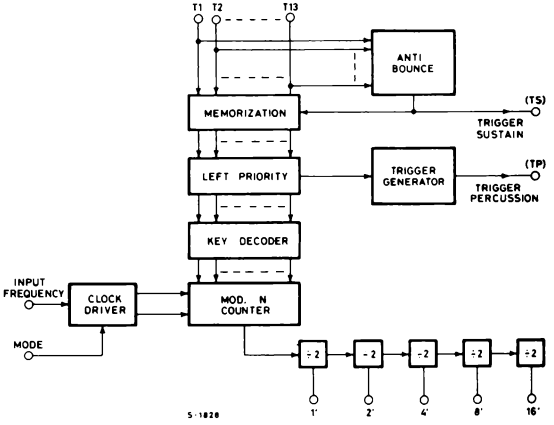


M 147

CONNECTION DIAGRAM



BLOCK DIAGRAM



GENERAL CATACTERISTICS

The circuit comprises
a) 13 pins for input pedals
b) 1 clock pin for input frequency
c) 1 input for MODE selection
d) 5 frequency outputs
e) 1 output for trigger sustain (TS)
f) 1 output for trigger percussion (TP)
g) 2 supply pins

DESCRIPTION OF OPERATION

The first negative front, which is obtained by pressing any key, starts a delay circuit whose duration is a function of the key pressed and varies from 4 to 8 ms in normal mode (with the MODE input at V_{SS} and f_I= 500 kHz or with the MODE input at V_{GG} and f_I= 2 MHz (note 1)).
If the key is released before this delay time has passed, it will not be memorized.
Releasing the key retriggers the delay circuit, and not until the end of the delay will any further keys to the right be accepted, unless the new key was already pressed **before** the release of the first key then the new key is accepted immediately.
Any key to the left will be accepted immediately it is pressed. Re-pressing the same key will output the same frequency but with a jump of phase as the internal counters will be reset to zero.
When a pedal is depressed, the corresponding frequency (square wave, 50% of duty cycle) in 5 octaves is present in parallel at the 5 outputs.
These outputs remain when the pedal is released, until a new pedal is depressed. When two or more pedals are depressed, only the left one is accepted (corresponding to the lowest, frequency).
A TP output pulse is present whenever a pedal with priority is depressed. If the pedal is again depressed, successive TP pulses are generated.
A pulse appears at the TP output if, when two pedals are depressed, the left one is released.
The TS output is activated only when one or more pedals are depressed. An internal circuit provides bounce suppression on this output.

Note 1: With MODE at V_{SS} and f_I= 1 MHz the time is halved (2 to 4 ms)
With MODE at V_{GG} and f_I= 1 MHz the time is doubled (8 to 16 ms).

MODE OF OPERATION

If the MODE input is connected to V_{SS}, the input frequency must be 500.06 kHz.
If the MODE input is connected to V_{GG}, the input frequency must be 2.00024 MHz.

STATIC ELECTRICAL CHARACTERISTICS (V_{GG} = -16 to -18V, V_{SS} = 0V, T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage		V_{SS}-1		V_{SS}	V
V_{IL}	Input low voltage		V_{GG}		V_{SS}-5	V
R_{ON}	Output resistance	V_O=V_{SS}-1V to V_{SS}		1	1.6	κΩ
$I_{O(off)}$	Output leakage current	V_I=V_{IH}, V_O=V_{SS}-10V T_{amb}= 25°C			10	μA
I_L	Input leakage current	V_I=V_{SS}-14V T_{amb}= 25°C			10	μA
I_{GG}	Supply current	T_{amb}= 25°C		35	45	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{GG} = -16 to -18V, V_{SS}=0V, T_{amb}= 0 to 70°C unless otherwise specified; f_I= 2.00024 MHz if MODE input is connected to V_{GG}; f_I= 500.06 kHz if MODE input is connected to V_{SS}).

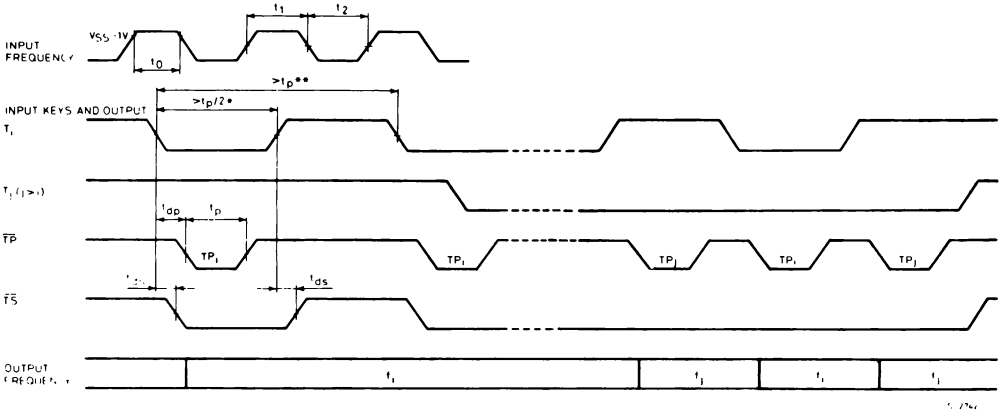
Parameter		Test conditions	Min.	Typ.	Max.	Unit	Notes
t_0	Input frequency "1" time		150			ns	
t_{1A}	Input frequency positive half period		0.8	1		μs	1-3
t_{2A}	Input frequency negative half period		0.8	1		μs	1-3
t_{1B}	Input frequency positive half period		200	250		ns	2-3
t_{2B}	Input frequency negative half period		200	250		ns	2-3
t_{ds}	Delay time of TS			300	1000	ns	3
t_{dp}	Delay time of TP				10	μs	3
t_p	Width of TP			10	22	ms	3

Notes: 1) With MODE connected to V_{SS}
2) With MODE connected to V_{GG}
3) All these delay and width times are measured at 50% of the swing.

OUTPUT FREQUENCIES (Hz)

Input	Outputs				
	1'	2'	4'	8'	16'
T1	523.075	261.538	130.769	65.384	32.692
T2	554.390	277.195	138.598	69.299	34.649
T3	586.925	293.462	146.731	73.366	36.683
T4	621.965	310.983	155.491	77.746	38.873
T5	659.710	329.855	164.927	82.464	41.232
T6	698.408	349.204	174.602	87.301	43.650
T7	739.734	369.867	184.933	92.467	46.233
T8	783.793	391.897	195.948	97.974	48.987
T9	830.664	415.332	207.666	103.833	51.917
T10	880.387	440.194	220.097	110.048	55.024
T11	932.948	466.474	233.237	116.618	58.309
T12	988.261	494.130	247.065	123.533	61.766
T13	1046.151	523.075	261.538	130.769	65.384

TIMING WAVEFORMS

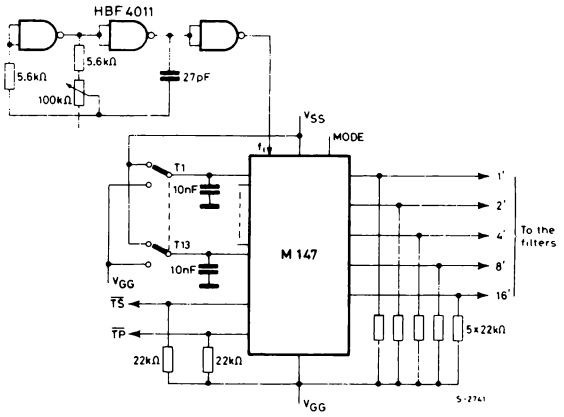


* In order to obtain memorization the key must be pressed for more than Tp/2.

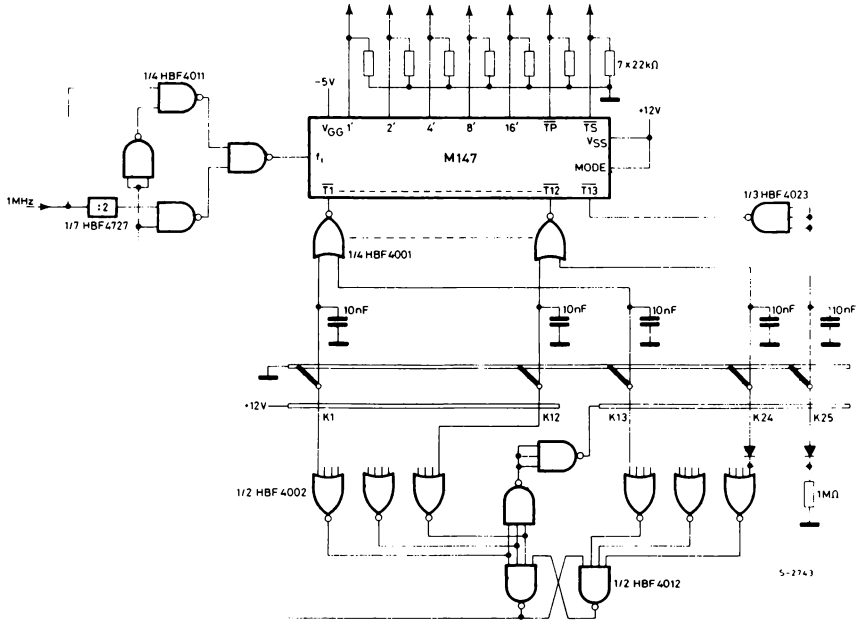
** If the key is pressed twice for a time less than Tp only a single percussion trigger Tp output will be available.

TYPICAL APPLICATIONS

Typical application circuit



Circuit for a 25 pedal system using the M 147



MOS INTEGRATED CIRCUIT

M 190

PRELIMINARY DATA

16 KEY KEYBOARD ENCODER AND LATCH

- ANTIBOUNCE AND ANTINOISE CIRCUITRY
- INTERLOCK PREVENTS INCORRECT SELECTION
- OPERATES WITH SINGLE POLE PUSH-BUTTONS
- SELECTION OF PROGRAM 1 AT POWER ON
- MUTING OUTPUT AVAILABLE DURING PROGRAM CHANGES AND POWER SUPPLY SWITCHING
- STEP-BY-STEP PROGRAM CHANGE INPUT
- KEYBOARD LOCKING
- OUTPUTS DIRECTLY COMPATIBLE WITH M 193 (ELECTRONIC PROGRAM MEMORY), M 192 (7-SEGMENT DECODER DRIVER), H 770/1/2/3 (QUAD ANALOG SWITCHES)

The M 190 is a monolithic integrated circuit which automatically scans an up to 16 Key keyboard, generating continuous sequential pulses on X outputs and detecting key closure on Y inputs.
A key closure is retained as valid when the key remains closed for all the time corresponding to one scan pulse (i.e. when the bounce is over).
When it occurs an internal flip-flop is set but the key closure is accepted only if it is detected on a second scan cycle. At this point a 4 bit word corresponding to the key closed is internally latched and a pulse is available on the Muting output.
During the time this pulse lasts, no other key closure will be recognized. The new output code follows the Mute signal with a delay.
All the timing for the circuits is determined by the clock oscillator whose frequency is externally fixed by an RC network.
The M 190 also includes a "step-by-step" program change input that, when connected to V_{SS} (GND), advances by one the selected channel and a Lock which blocks the circuit on the last selected channel.
The circuit is produced in N-channel silicon gate technology and is available in a 18 pin dual in-line plastic package.

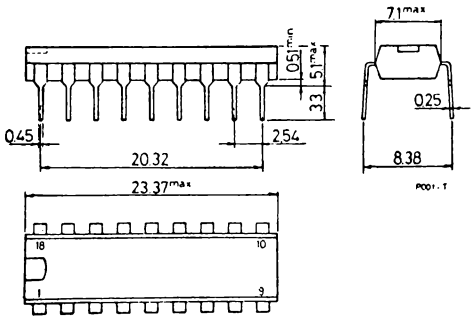
ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to 20	V
$V_{O(off)}$	Off state output voltage (pins 1-2-3-4-11)	20	V
J_O	Output current	|5|	mA
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 125	°C
T_{op}	Operating temperature	0 to 70	°C

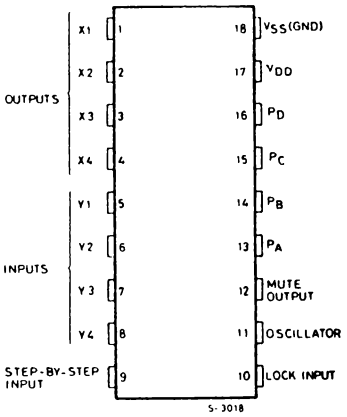
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
** All voltage are referred to V_{SS} pin voltage.

ORDERING NUMBER: M 190 B1

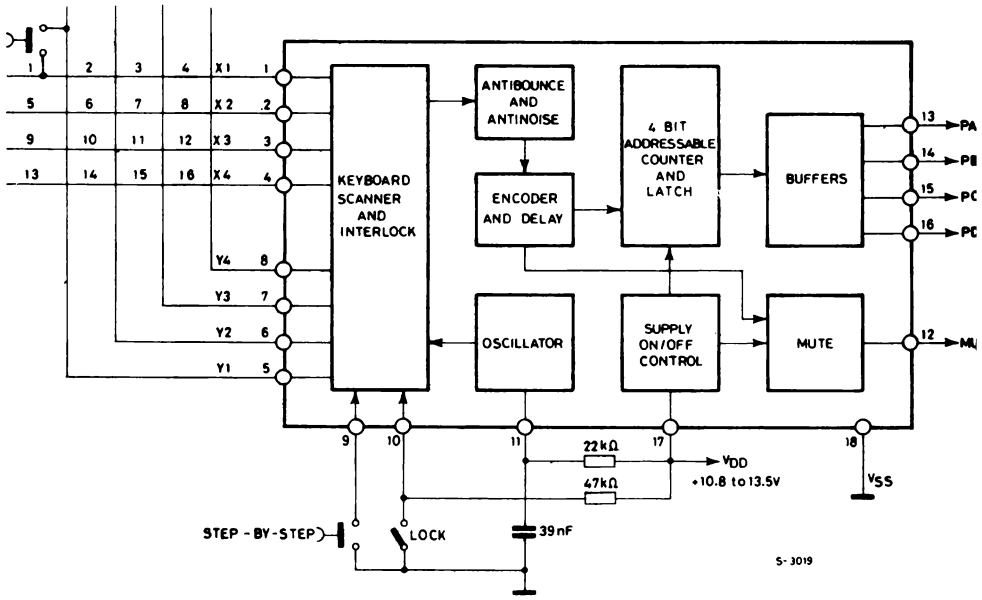
MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	10.8 to 13.5	V
V_I	Input voltage	0 to 13.5	V
$V_{O(off)}$	Off state output voltage (pins 1-2--3-4-11)	max 13.5	V
I_O	Output current	max |2|	mA
T_{op}	Operating temperature	0 to 70	°C
R_t	Timing resistor	8 to 47	KΩ
C_t	Timing capacitor	1 to 330	nF

STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

	Parameter	Test conditions	Values at 25°C			Unit
			Min.	Typ.	Max.	
V_{IH}	High level input voltage	pins 5, 6, 7, 8, 9, 10	3.5			V
V_{IL}	Low level input voltage	pins 5, 6, 7, 8, 9, 10			0.8	V
I_{IH}	High level input current	V_{DD}= 13.5V, V_{IH}= 13.5V pins 5, 6, 7, 8, 9, 10			10	μA
I_{IL}	Low level input current	V_{DD}= 13.5V, V_{IL}= 0.8V pins 5, 6, 7, 8, 9, 10	0.1		0.8	mA
V_{OH}	High level output voltage	V_{DD}= 10.8V I_{OH}= -1 mA, pin 12	2.4			V
		V_{DD}= 10.8V I_{OH}= -1 mA, pins 13. 14, 15, 16	4			
V_{OL}	Low level output voltage	V_{DD}= 10.8V I_{OL}= 0.8 mA pins 1, 2, 3, 4, 11			0.4	V
		V_{DD}= 10.8V I_{OL}= 2 mA, pins 13, 14, 15, 16			0.4	
$I_{O(off)}$	Output leakage current	V_{DD}= $V_{O(off)}$= 13.5V, pins 1, 2, 3, 4, 11			20	μA
I_{DD}	Supply current	V_{DD}= 13.5V (all inputs and outputs open)			18	mA

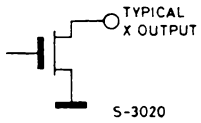
TRUTH TABLE

Key	Connection	Output code (positive logic)			
		PA	PB	PC	PD
1	$X_1 - Y_1$	L	L	L	L
2	$X_1 - Y_2$	H	L	L	L
3	$X_1 - Y_3$	L	H	L	L
4	$X_1 - Y_4$	H	H	L	L
5	$X_2 - Y_1$	L	L	H	L
6	$X_2 - Y_2$	H	L	H	L
7	$X_2 - Y_3$	L	H	H	L
8	$X_2 - Y_4$	H	H	H	L
9	$X_3 - Y_1$	L	L	L	H
10	$X_3 - Y_2$	H	L	L	H
11	$X_3 - Y_3$	L	H	L	H
12	$X_3 - Y_4$	H	H	L	H
13	$X_4 - Y_1$	L	L	H	H
14	$X_4 - Y_2$	H	L	H	H
15	$X_4 - Y_3$	L	H	H	H
16	$X_4 - Y_4$	H	H	H	H

DESCRIPTION

Pins 1, 2, 3, 4 - X_1, X_2, X_3, X_4 outputs

The internal open drain transistors on these outputs are sequentially switched on.

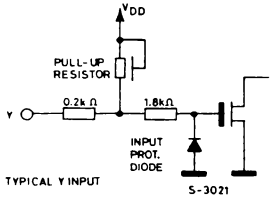


Pins 5, 6, 7, 8 - Y_1, Y_2, Y_3, Y_4 inputs

These inputs correspond to the columns of the keyboard matrix. When a key is pushed, one of the X output signal is present on one of the 4 rows, putting a low level on the Y input.
An interlock circuit rejects more than one key pressed at the same time.
To increase the noise immunity of the system and to avoid bouncing problems, the key closure is considered valid only when it is present for all the time corresponding to the scan pulse. With this system spurious noise signals are also rejected.
Another increase in the noise immunity is given by detecting key closure over two consecutive scanning cycles.

DESCRIPTION (continued)

After the key bounce time, the acceptance time of a command is between 35T and 63T, where T is the period of the clock pulse.
When any input is open it is pulled-up to logic H by an integrated MOS load of about 50 KΩ and protected by a diode.



Pin 9 - Step-by-step program change

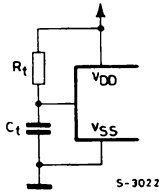
This input advances by one the previously selected channel every time ti is connedted to ground.
This input can be considered as a 17th key and follows all the rules of command acceptance time and partially of interlock.
The unput is pulled-up to logic H by an integrated resistor of about 50 KΩ ; if the input is not used, it should be connected to V_{DD}.

Pin 10 - Lock

If this input is connected to V_{SS} (GND) the circuit is locked on the selected channel.
If the input is not used, it must be connected to V_{DD}.

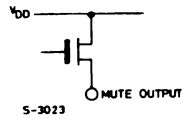
Pin 11 - RC network (clock oscillator input)

An internal clock provides all the timing for the circuits.
The frequency of the clock oscillator is controlled by two external components, resistor R_t and capacitor C_t.
The period of the clock pulse is approximately given by $T = R_tC_t$.
The oscillator works in the following way: assuming the capacitor C_t is discharged, the resistor R_t charges the capacitor till an internal threshold is reached. At this point the capacitor is discharged by an internal transistor.
Afterwards the internal transistor is switched off and the cycle can restart.
With R_t= 22 KΩ and C_t= 39 nF a clock frequency of about 800 Hz is obtained, corresponding to a scan cycle of the keyboard of about 40 ms.
In these conditions the mute signal will be present for about 100 ms before the program changing and will last 300 ms.

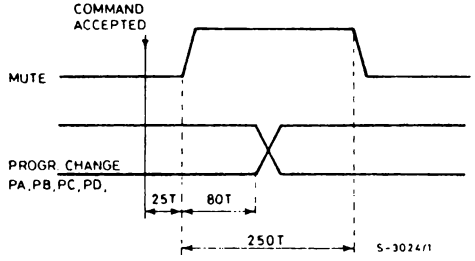


Pin 12 - Mute

The mute signal is available as a high level output (source follower transistor).
It is present during power ON/OFF and program changes.



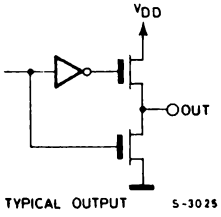
When a command is given the Mute signal and the program information are available in the following way:



The Mute signal is not available when the same program is selected again.

Pins 13, 14, 15, 16 - PA, PB, PC, PD outputs

These static outputs select the program according to the truth table.
They interface directly with the inputs of M 193 (Electronic Program Memory), M 192 (7 segment Decoder/Driver), H 770/1/2/3 (Quad Analog Switches).
The program 1 is internally selected at power ON.



ON-SCREEN TUNING SCALE AND BAND DISPLAY

- DIGITAL TUNING BAR DISPLAY WITH MINIMUM EXTERNAL PRESETS
- ON-SCREEN DISPLAY OF THE BAND
- VERTICAL POSITION ON THE SCREEN EXTERNALLY ADJUSTABLE
- AUTOMATIC DISPLAY AT SEARCH COMMAND
- DESIGNED FOR USE WITH THE M193 ELECTRONIC PROGRAM MEMORY

The M191 is a monolithic integrated circuit designed to display on the screen of the television receiver a variable length strip corresponding to the voltage applied to the varicap tuner.
A variable number of rectangles symbolizing the selected band can also be displayed.
The circuit operates in conjunction with the M193 Electronic Program Memory, from which it takes the voltage and band information in a digital serial mode.
The 7 most significant digits of voltage information coming from the M193 are digitally converted into a 64 step variable pulse width giving either positive and negative polarity outputs for easy and versatile interfacing.
The variable length strip is displayed over 11 lines of a half frame picture with nine vertical graduations of 31 lines.
The vertical position of the strip can be adjusted with an external potentiometer over the whole screen.
The 2 digits of band information determine the number of rectangles appearing on the screen under the tuning strip. The rectangles are displayed over 11 lines of a half frame picture.
Automatic display is provided when the Electronic Program Memory is in the Search Mode; display on command is always possible.
The M191 is constructed in N-channel silicon gate technology and is available in a 16 pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

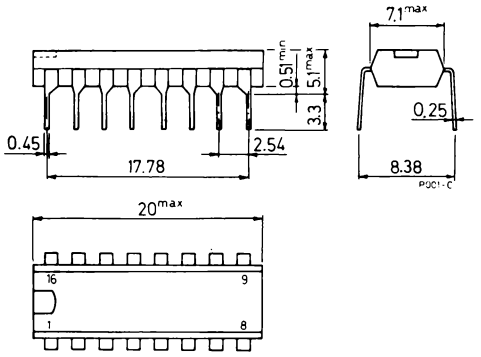
V_{DD} **	Supply voltage	-0.3 to 20	V
V_I	Input voltage	-0.3 to 20	V
I_I	Input current	-5	mA
$V_{O(off)}$	Off-state output voltage	20	V
I_O	Output current (except pins 12-13)	5	mA
	(pins 12-13)	15	mA
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

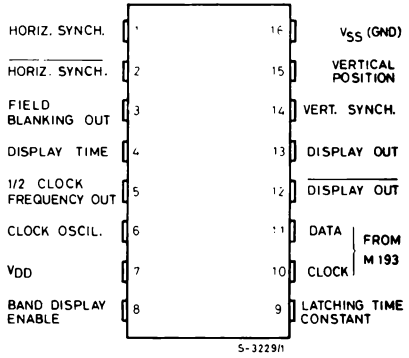
** All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS: M191 B1

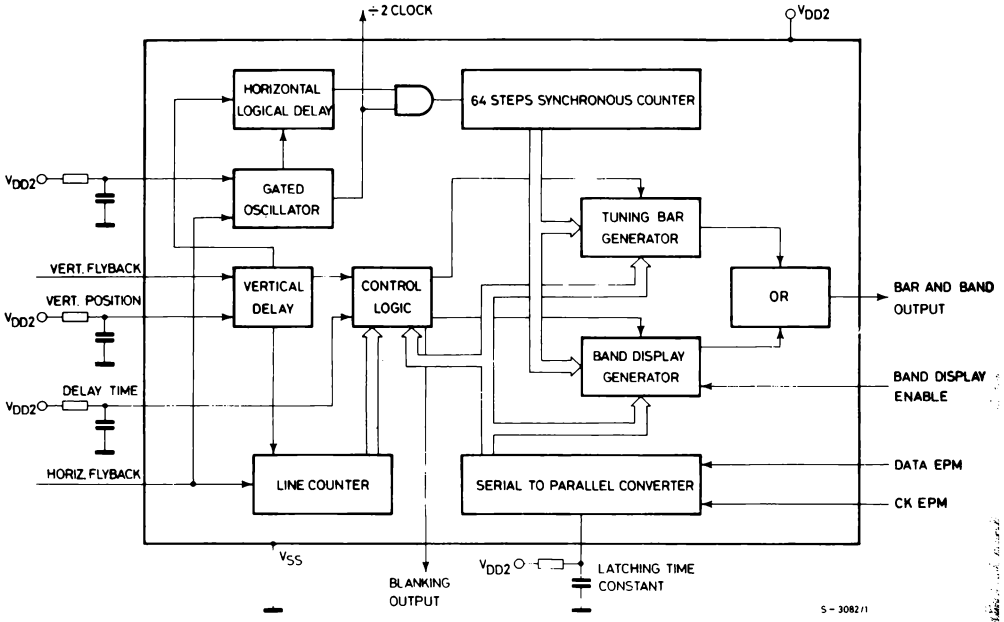
MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter		Min.	Typ.	Max.	
V_{DD}	Supply voltage	11.5	13	14.5	V
V_I	Input voltage			14.5	V
$V_{O\,(off)}$	Off-state output voltage			14.5	V
I_O	Output current (all pins except 4-6-12-13)*			1	mA
	(pin 6)			3	mA
	(pins 12-13)			10	mA
f	Clock frequency		1.8	2.2	MHz
T_{op}	Operating temperature	0		70	°C
P_{tot}	Total package power dissipation			500	mW
C_9	Capacitance at pin 9		330	390	pF
C_6	Capacitance at pin 6		68	100	pF
C_{15}	Capacitance at pin 15		270	330	nF
C_4	Capacitance at pin 4**		10	12	μF
$R_{4,\,15}$	Resistance at pins 4-15		220	270	KΩ

* I_{O4} The output current of pin 4 is internally limited.
** C_4 Values up to 100 μF are allowed using a 1KΩ resistor in series with pin 4.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions).

Typical values are at T_{amb} = 25°C, V_{DD} = 13V.

Parameter		Test conditions	Pins	Values			Unit
				Min.	Typ.	Max.	
V_{IL}	Low level input voltage	V_{DD} = 11.5 to 14.5V	1-2-10-11-14			0.8	V
V_{IH}	High level input voltage	V_{DD} = 11.5 to 14.5V	1-2-10-11-14	3.5			V
V_{OL}	Low level output voltage	V_{DD} = 11.5V I_{OL} = 10 mA	12-13			1	V
		V_{DD} = 11.5V I_{OL} = 1 mA	3			1	V
V_T	Threshold voltage	V_{DD} = 11.5 to 14.5V	6-9-15		4		V
			4-8		2		
I_I	Input current	V_I = 14.5V				10	μA
$I_{O\,(off)}$	Off-state output current	V_{DD} = 14.5V	3-4-5-9-15			20	μA
			12-13			100	
I_{DD}	Supply current	V_{DD} = 14.5V				25	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C)

Parameter	Test conditions	Values			Unit
		Min.	Typ.	Max.	
t_{TLH}, t_{THL} Transition time	Pins 12-13 See fig. 3		80		ns
t_D Delay time			50		ns

TYPICAL APPLICATION

Fig. 1

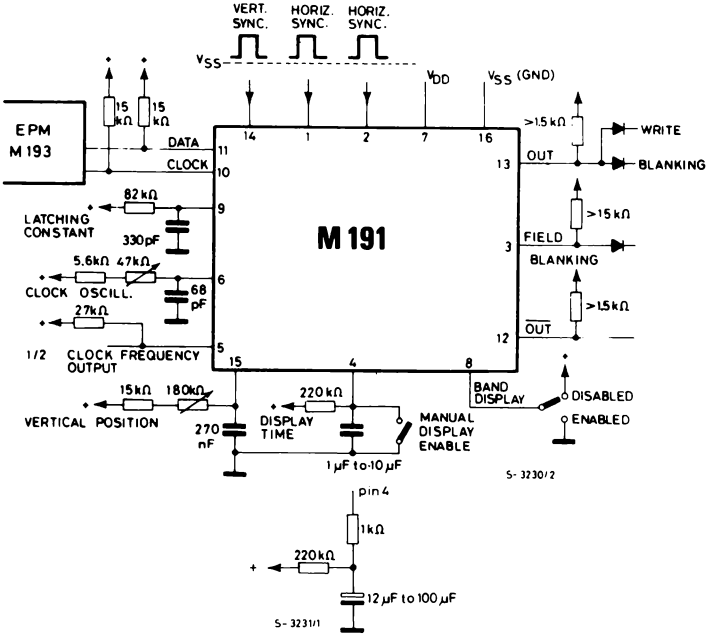
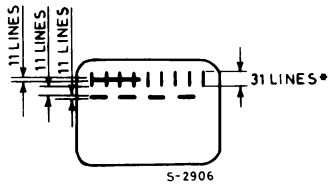
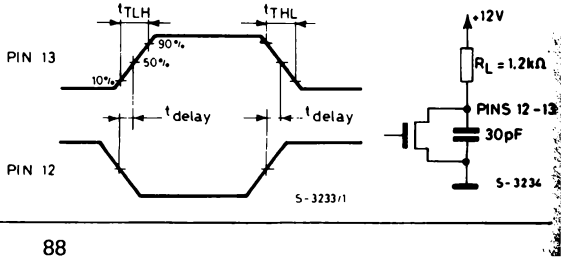


Fig. 2



* : THE LINES CORRESPOND TO A HALF FRAME

Fig. 3

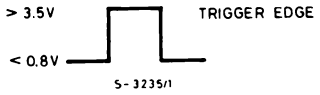


DESCRIPTION

Pins 1, 2 - Horizontal synchronization

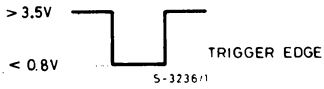
Two Horizontal sync inputs are provided to allow for positive or negative pulses from the TV receiver.
Pin 1 is designed to accept a positive pulse deroved from the line flyback through an interface.
The circuit is triggered on the negative edge of the incoming pulse.

Fig. 4 - Pin 1



The negative flyback pulses must be applied to pin 2. In this case the circuit is triggered on the positive edge of the pulse.

Fig. 5 - Pin 2



The display is delayed for a time corresponding to 32 clock periods after the triggering.
With a clock frequency of 1.8 MHz the delay is 9 μsec.
When pin 1 is used, pin 2 must be connected to V_{SS} (GND), when using pin 2, pin 1 must be at V_{DD}.

Pin 3 - Field blanking output

An open drain transistor is disabled during the lines which correspond to the display of the tuning scale and band information. This makes it possible to write the tuning scale and the band identification rectangles on a dark or alternative colour area. The signal is present for the full line period.

Pin 4 - Display time input

The display is automatically enabled when the M193 electronic program memory is in the Search mode.
The RC network applied to pin 4 determines the time the display will last after a station is found.
When identification occurs the capacitor is unclamped and allowed to charg no the external resistor. The display is disabled when an internal threshold is reached.
The opposite applies when the capacitor is discharged by connecting this pin to V_{SS} (GND) with an external clamp.
If a capacitor $> 10\ \mu F$ is used a 1 KΩ resistor must be placed in series with pin 4.

Pin 5 - 1/2 frequency clock output

The clock frequency divided by two is present on this pin for measurement purposes. To allow this, connect temporarily pin 1 to V_{SS} and pin 2 to V_{DD}. The output is open drain and an external pull-up resistor is needed.
If the output is not used it must be connected to V_{SS}.

DESCRIPTION (continued)

Pin 6 - Clock oscillator input

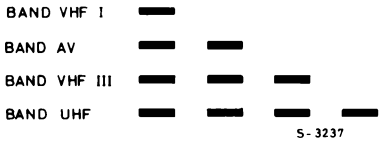
This pin is connected to a RC network as shown in fig. 1.
The clock frequency determines the horizontal width on the screen of the tuning scale, of the rectangles and the distance of the display from the left edge of the screen.
Fine adjustment of the clock frequency is obtained by the trimming resistor. Typical clock frequency is 1.8 MHz.

Pin 7 - V_{DD}

Pin 8 - Band display enable

When this pin is connected to V_{SS} (GND) a band display with the following format is enabled, on command, together with the tuning voltage display.

Fig. 6

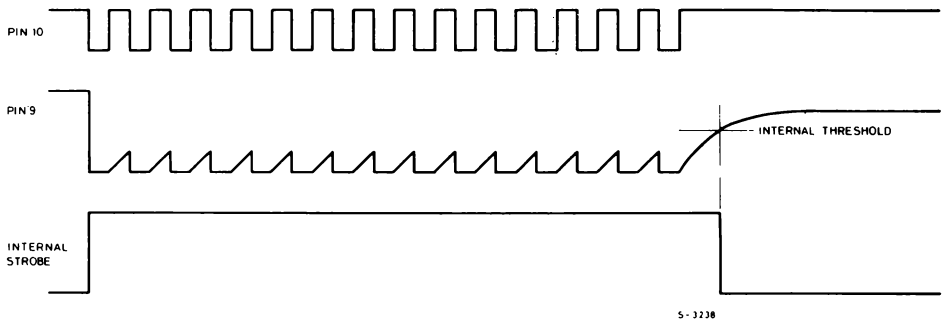


If this pin is connected to V_{DD} only the tuning voltage will be displayed.

Pin 9 - Latching time constant

An RC time constant must be applied to this pin to generate the internal latching signal.
The content of the internal shift register is transferred to the internal decoding circuit only at the end of the clock burst to avoid noise on the display during data transfer.
This is made by integrating the incoming clock burst with the RC time constant connected to pin 9 as shown in fig. 7.

Fig. 7

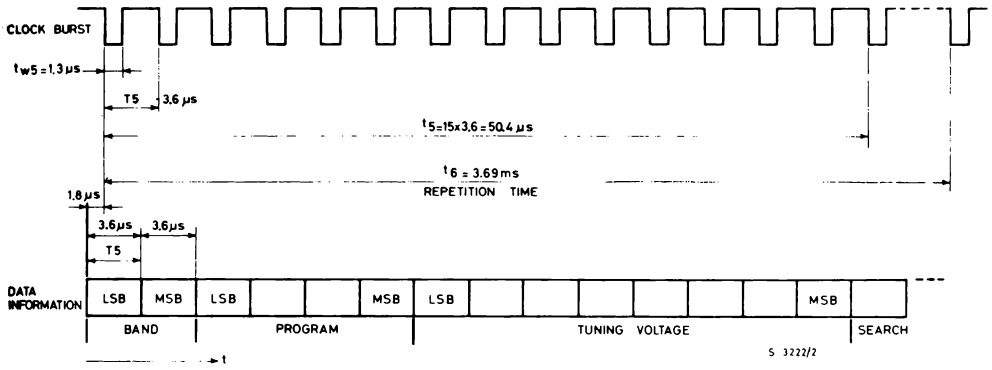


DESCRIPTION (continued)

Pin 10 - Clock input

This pin accepts the burst containing the 15 clock pulses available from the M193. The burst is used to load the serial Data on pin 11 into the internal 15 bit shift register (see fig. 8).

Fig. 8



Pin 11 - Data input

This pin accepts the 15 bit serial Data information available from the M193 EPM.
The burst contains 2 bits for band information, 4 bits for program, 8 bits for tuning voltage and 1 bit which indicates if the system is in the Search mode.

Pin 12 - Inverted video signal output

The signals of pin 13 are inverted and presented on this pin to allow easy interfacing in some chroma kits. The output is open drain.

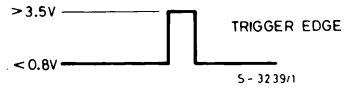
Pin 13 - Video signal output

The tuning scale and band information video signal is available on this pin, a load resistor is connected between the open drain output transistor and V_{DD}. White level corresponds to disable of the internal transistor.

Pin 14 - Vertical synchronization

The frame flyback pulse must be applied to this pin by means of an interface. The signal must be positive. The circuit is triggered by the negative edge of the pulse.

Fig. 9



DESCRIPTION (continued)

Pin 15 - Vertical position input

An internal monostable is triggered by the frame pulse applied on pin 14.
The display is allowed at the end of the cycle of the monostable. The RC network applied to this pin gives the time constant of the monostable determining the position of the display on the screen.

Pin 16 - V_{SS} (GND)

All voltages quoted are referred to Pin 16.

COS/MOS INTEGRATED CIRCUIT

M 192

PRELIMINARY DATA

4-BIT BINARY 7-SEGMENT DECODER DRIVER

- 4-BIT BINARY CODE INPUT GENERATES 1 TO 16 NUMBERS ON OUTPUT
- DIRECT DRIVING OF 1 AND 1/2 DIGIT 7-SEGMENT (COMMON CATHODE) LED DISPLAY
- WIDE SUPPLY VOLTAGE RANGE
- TTL COMPATIBLE INPUTS
- SMALL QUIESCENT SUPPLY CURRENT
- SPECIFICALLY DESIGNED FOR TV OR RADIO APPLICATIONS

The M 192 is a monolithic integrated circuit which direct drives a 1 and 1/2 digit 7-segment LED (common cathode) display to present the numbers 1 to 16. The inputs accept a 4-bit binary code having TTL levels. This device is especially designed to show the program number in TV or radio sets in conjunction with M 190 keyboard encoder, M 1130 ultrasonic remote control receiver, M 193 electronic program memory or H 770/1/2/3 analog switches. All outputs are designed to supply and sink current, except the additional "r" output (pin 1) which is designed for a brightness control in a current generator configurations. The circuit is produced in COS/MOS technology and is supplied in a 16-pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to	16.5	V
V_I	Input voltage	-0.5 to V_{DD}	+0.5	V
V_O	Output voltage (pin 1)		V_{DD} +0.5	V
I_{OH}	Output source current		-25	mA
I_{OL}	Output sink current (except pin 1)		10	mA
P_{tot}	Total package power dissipation		400	mW
T_{stg}	Storage temperature	-65 to	150	°C
T_{op}	Operating temperature	0 to	70	°C

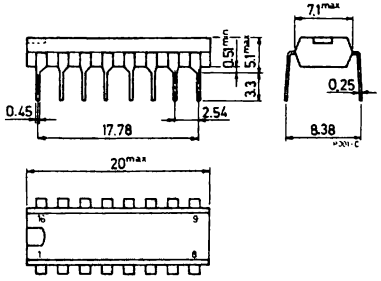
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

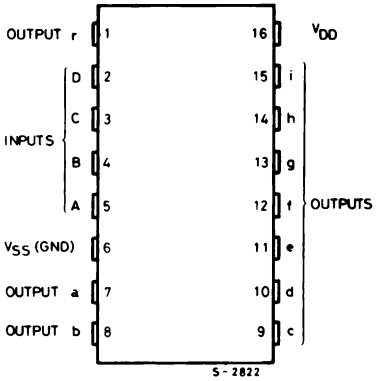
ORDERING NUMBER: M 192 B1

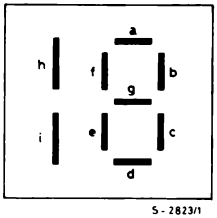
MECHANICAL DATA

Dimensions in mm



PIN CONNECTIONS

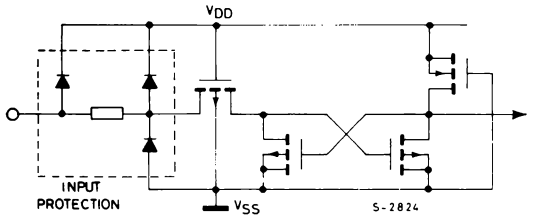




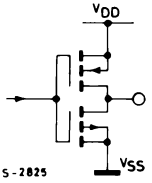
TRUTH TABLE

INPUTS				Number displayed	OUTPUTS									
A	B	C	D		a	b	c	d	e	f	g	h	i	r
L	L	L	L	1	L	H	H	L	L	L	L	L	L	H
H	L	L	L	2	H	H	L	H	H	L	H	L	L	H
L	H	L	L	3	H	H	H	H	L	L	H	L	L	H
H	H	L	L	4	L	H	H	L	L	H	H	L	L	H
L	L	H	L	5	H	L	H	H	L	H	H	L	L	H
H	L	H	L	6	H	L	H	H	H	H	H	L	L	H
L	H	H	L	7	H	H	H	L	L	L	L	L	L	H
H	H	H	L	8	H	H	H	H	H	H	H	L	L	H
L	L	L	H	9	H	H	H	H	L	H	H	L	L	H
H	L	L	H	10	H	H	H	H	H	H	L	H	H	H
L	H	L	H	11	L	H	H	L	L	L	L	H	H	H
H	H	L	H	12	H	H	L	H	H	L	H	H	H	H
L	L	H	H	13	H	H	H	H	L	L	H	H	H	H
H	L	H	H	14	L	H	H	L	L	H	H	H	H	H
L	H	H	H	15	H	L	H	H	L	H	H	H	H	H
H	H	H	H	16	H	L	H	H	H	H	H	H	H	H

INPUT CONFIGURATION



OUTPUT CONFIGURATION



Note: pin 1 has not the pull down N-channel transistor.

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	10.8 to 15 V
V_I	Input voltage	0 to V_{DD} V
V_O	Output voltage (pin 1)	V_{DD} V
I_{OH}	Output source current	max -10 mA
I_{OL}	Output sink current	max 0.5 mA
T_{op}	Operating temperature	0 to 70 °C

ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

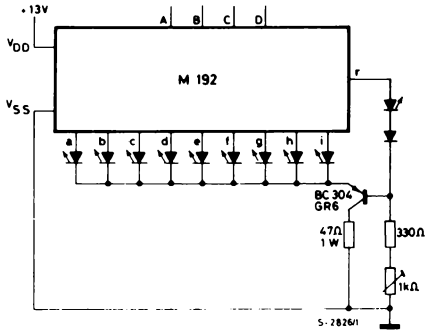
typical values are at T_{amb}= 25°C unless otherwise specified

Parameter		Test conditions		Values Min.	Values Typ.	Values Max.	Unit
V_{IH}	High level input voltage			3.5		V_{DD}	V
V_{IL}	Low level input voltage			0		0.8	V
I_{IH}	High level input current	V_{DD}= 15V	V_{IH}= 15V			10	µA
I_{T+}	Input current at positive threshold	V_{DD}= 15V				200	µA
V_{OH}	High level output voltage	I_{OH}= -10 mA	V_{DD}= 10.8V V_{DD}= 13V V_{DD}= 13V, T_{amb}= 70°C V_{DD}= 15V	V_{DD} -3	V_{DD}-3 V_{DD}-2 V_{DD}-2.5 V_{DD}-1.5		V V V V
V_{OL}	Low level output voltage (except pin 1)	V_{DD}= 13V	I_{OL}= 0.5 mA		1	1.5	V
I_{DD}	Supply current Input to V_{DD} Outputs open	V_{DD}= 15V			2	2,4	mA

APPLICATION INFORMATION

Fig. 1 - Light emitting diode readout

a - Current generator configuration



b - Standard configuration

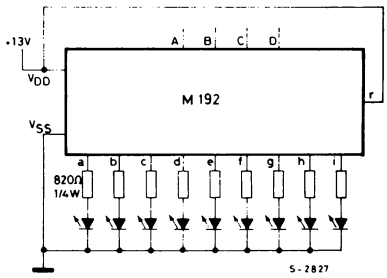


Fig. 2 - Liquid crystal readout

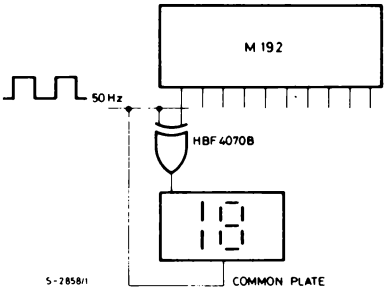


Fig. 3 - Fluorescent readout

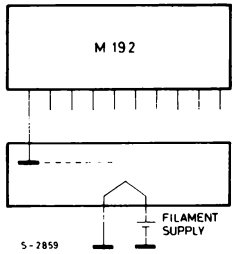


Fig. 4 - Incandescent redout

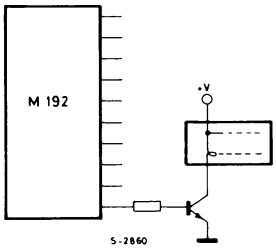
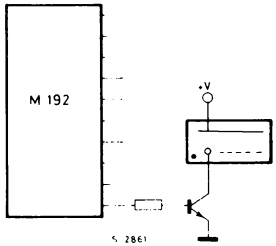


Fig. 5 - Gas discarge readout



TYPICAL APPLICATIONS (continued)

Program display with stand-by indication

This application is useful in a remote controlled set. The stand-by condition of the set, i.e. when only the remote control is supplied, is shown by two dots.

The program display number is controlled by the same output of the remote control receiver as that which drives the mains relay.

Fig. 6

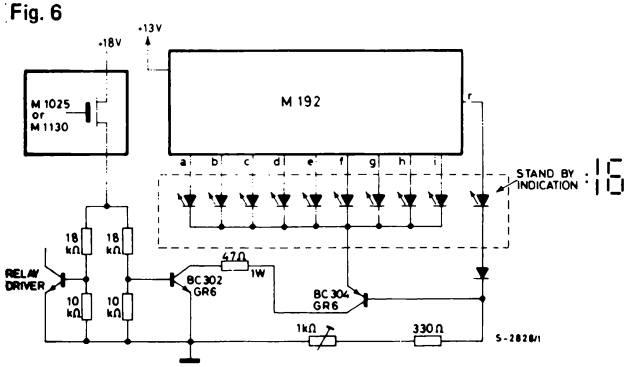
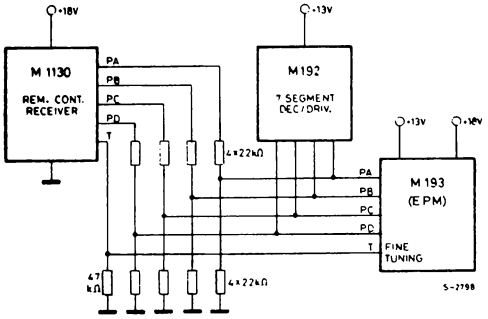
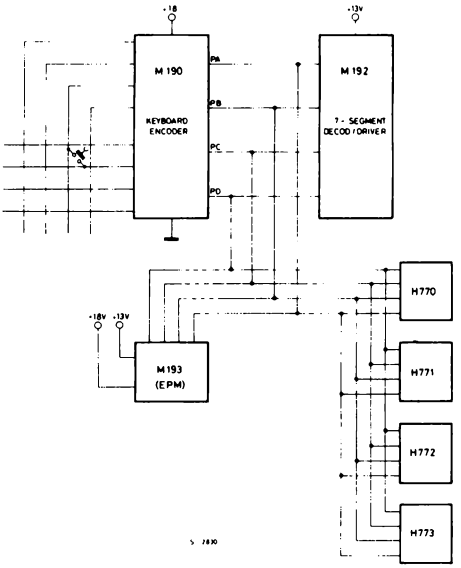


Fig. 7 - M 192 interfacing

a



b



ELECTRONIC PROGRAM MEMORY

- ONE CHIP SOLUTION INCLUDING CONTROL AND NON VOLATILE MEMORY FOR 16 PROGRAMS
- 10 YEARS MEMORY RETENTION
- UNLIMITED NUMBERS OF READ CYCLES
- AUTOMATIC AND MANUAL STATION SEARCH
- EXTERNALLY ADJUSTABLE SEARCH SPEED
- FINE TUNING IN 8 STEPS, STORABLE FOR EACH PROGRAM SEPARATELY
- MUTE OUTPUT
- 4.43 MHz QUARTZ or LC REFERENCE FREQUENCY

The M193 is a monolithic integrated circuit constructed in N-channel silicon gate technology, designed to control digitally via a D/A converter, with a resolution of 8192 steps, a TV or Radio varicap tuner. It also contains a 17 bit x 16 words NVRAM, whose control timing is internally generated, and after having been externally buffered, is returned to the integrated circuit to drive the memory. Each memory word contains information for 1 program, i.e. band (2 bit), tuning voltage (12 bit) and fine tuning offset (3 bit). The circuit is able to operate either in automatic or manual search. The search speed is externally controlled by a simple RC network. In the automatic mode the M193 works in conjunction with the TDA 4431, which provides TV station recognition and converts the AFC-S-curve into a digital command. This command controls the 13 bit up/down counter in the M193, whose position determines the tuning voltage. A mute output is provided to avoid noise on the audio during automatic search, program change or when the supply voltage is switched on/off. The circuit accepts standard program selection on 4 bus lines. 7-segment program display is possible by using the M192 circuit connected at the same lines. A serial information output is provided to display on the screen, via the M191 integrated circuit, the varicap voltage in the form of a linear tuning bar and the band. The M193 is available in a 28 lead dual in-line plastic package. Two different types are available which differ as specified below.

M193 - Standard type.

M193A - As M193 but the fine tuning is also reset during a manual search.

ORDERING NUMBERS: M193 B1
M193A B1

M 193
M 193 A

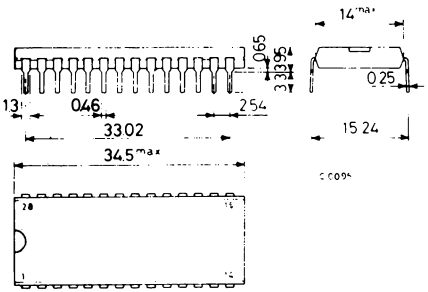
ABSOLUTE MAXIMUM RATINGS*

V_{DD1}, V_{DD2} **	Supply voltages	-0.3 to 20	V
V_{PP}	Memory supply voltage (pin 9)	-0.3 to 31	V
V_I	Input voltage	-0.3 to 20	V
$V_{O\ (off)}$	Off-state output voltage (except pin 14)	20	V
	(pin 14)	31	V
I_{OL}	Output current (except pins 15-19)	5	mA
	(pins 15-19)	15	mA
I_{OH}	Output current (pin 27)	-5	mA
P_{tot}	Total package power dissipation	1	W
T_{stg}	Storage temperature	-25 to 125	°C
T_{op}	Operating temperature	0 to 70	°C

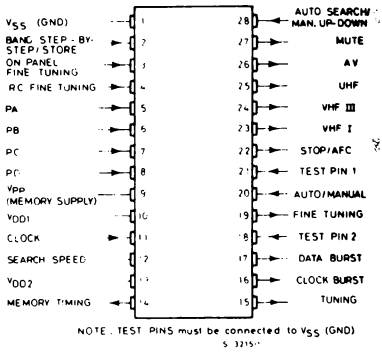
* Stresses above those listed under "Absolute Maximum Ratings"may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND)

MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS

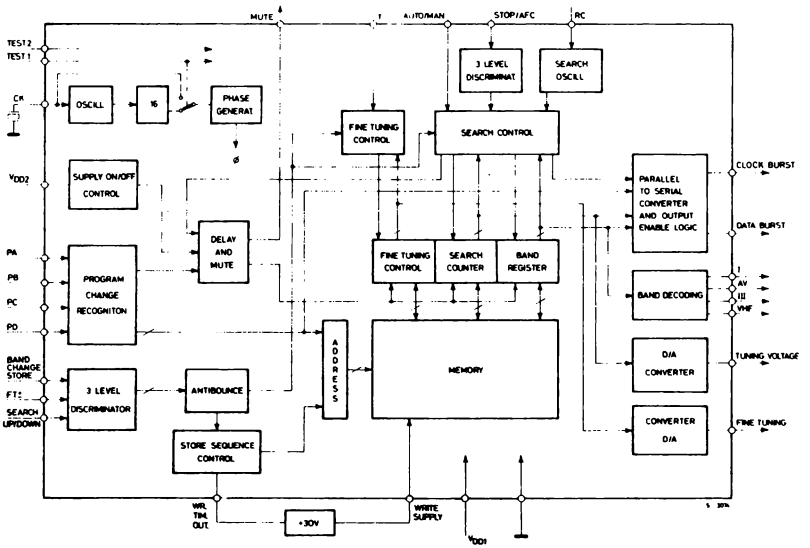


NOTE : TEST PINS must be connected to V_{SS} (GND)

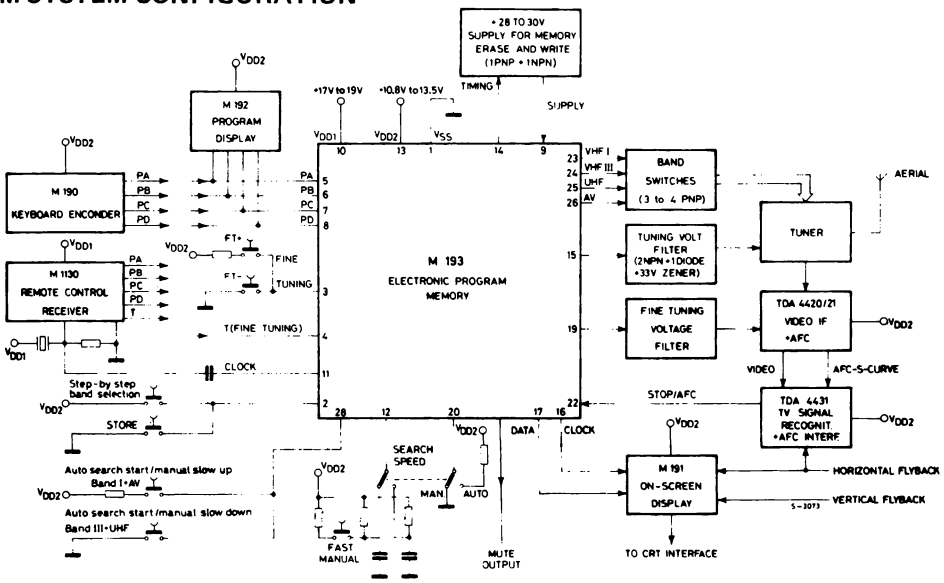
RECOMMENDED OPERATING CONDITIONS

V_{DD1}	Supply voltage	17 to 19	V
V_{DD2}	Supply voltage	10.8 to 13.5	V
V_{PP}	Memory supply voltage (pin 9)	28 to 30	V
V_I	Input voltage	0 to 19	V
$V_{O\ (off)}$	Off-state output voltage (except pin 14)	max. 19	V
	Off-state output voltage (pin 14)	max. 30	V
I_{OL}	Output current (except 15-19)	max. 2.5	mA
	(pins 15-19)	max. 10	mA
I_{OH}	Output current (pin 27)	max. -2.5	mA
t_{pd}	Delay between memory timing and memory supply pulses	max. 5	µs
f	Clock frequency	4.43	MHz
t_{w1}	Fine tuning + pulse width (pin 4)	> 1.8	ms
t_{w2}	Fine tuning - pulse width (pin 4)	< 1.7	ms
T_{op}	Operating temperature	0 to 70	°C
R_{12}	Search speed resistance (pin 12)	18 to 330	KΩ
C_{12}	Search speed capacitor (pin 12)	max. 100	nF

BLOCK DIAGRAM



EPM SYSTEM CONFIGURATION



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at T_{amb}= 25°C, V_{DD1}= 18V, V_{DD2}= 12V unless otherwise specified

Parameter		Pins	Test conditions	Values			Unit
				Min.	Typ.	Max.	
V_{IL}	Low level input voltage	4-5-6-7-8				0.8	V
		2-3-20-22-28				1.3	
V_{IH}	High level input voltage	4-5-6-7-8		3.5			V
		2-3-28-20		V_{DD2}-2			
		22		V_{DD2}-1			
V_{IM}	Middle level input voltage	22	V_{DD2}= 10.8V	4,5		7.5	V
			V_{DD2}= 13.5V	5		9	
V_{OL}	Low level output voltage	23-24-25-26	V_{DD2}= 10.8V I_{OL}= 1 mA			3	V
		15-19	V_{DD2}= 10.8V I_{OL}= 10 mA			1	
		16-17	V_{DD2}= 10.8V I_{OL}= 1 mA			0.5	
		14	V_{DD1}= 17V, V_{DD2}= 10.8V I_{OL}= 2.5 mA			8	
V_{OH}	High level output voltage	27	V_{DD2}= 10.8V I_{OH}= -1 mA	2.4			V
$I_{O(off)}$	Output leakage current	27	V_{DD2}= 13.5V $V_{O(off)}$= V_{SS}			-50	µA
		23-24-25-26	V_{DD2}= 13.5V $V_{O(off)}$= 19V			100	
		15-16-17-19	V_{DD2}= 13.5V, $V_{O(off)}$= 13.5V			50	
		14	V_{DD1}= 19V V_{DD2}= 13.5V, $V_{O(off)}$= 30V			100	
I_I	Input current	4-5-6-7-8-22	V_I = 0 to 19V			|25|	µA
I_{DD1}	Supply current	10	V_{DD1}= 19V			3	mA
I_{DD2}	Supply current	13	V_{DD2}= 13.5V		32	45	mA
I_{PP}	Memory supply current	9	V_I = 30V writing			65	mA
			V_I = 30V erasure			1	
R_I	Input resistance	2-3-28	See Fig. 1a		0.5		MΩ

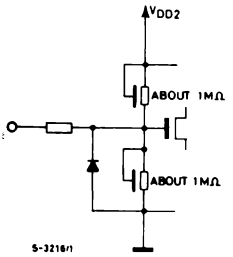
DYNAMIC ELECTRICAL CHARACTERISTICS (f_{clock} = 4.43 MHz)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
f_o	Fine tuning output repetition rate	Pin 19 (see also fig. 9)		17305		Hz
D	Fine tuning output duty cycle		1/8		8/8	
t_{w3}	Width of erase pulses	Pin 14		115		µs
T_3	Period of erase pulses	See also fig. 3 and 6		231		µs
t_3	Total time for one erase cycle (about 500 pulses)			115		ms
t_{w4}	Width of write pulses	Pin 14		115		µs
T_4	Period of,write pulses	See also fig. 2 and 5		462		µs
t_4	Total time for one write cycle about 950 pulses)			440		ms
t_{w5}	Width of clock pulses	Pin 16		1.3		µs
T_5	Period of data and clock pulses	Pin 17 See also fig. 8		3.6		µs
t_5	Total time for one display burst (15 pulses)			54		µs
t_6	Burst repetition time			3.69		ms
t_7	Acceptance time of the commands	Pins 2-3-28		31		ms
t_8	Acceptance time of the commands	Pin 20		3.6		µs

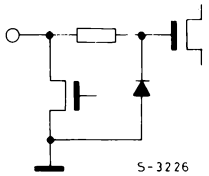
Input and output configurations
All outputs (except the Mute one) have open drain configuration.
The Mute output has a source follower.
Inputs have the following configurations:

Fig. 1

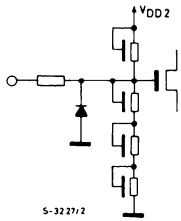
a) Pins 2, 3, 28



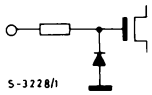
b) Search speed (pin 12)



c) Clock input (pin 11)



d) Other inputs (pin 4-8-12-20-21-22)



DESCRIPTION

The circuit description will be made following both pin sequence and pin function.

Pin 1 - V_{SS} (GND)

The substrate of the integrated circuit is connected to this pin. It is the reference point for all voltage parameters of the device and must be connected to the lowest potential of the supply voltage, normally ground.

Pin 2 - Store/sequential band change input

If this input pin is briefly connected to V_{SS} the 12 bits of the digitized tuning voltage, the 2 bits for band selection and the 3 bits of fine tuning information are stored.
The command is disabled during search and the execution of the store cycle.
The store cycle consists of two operations: at first the old word is cancelled and afterwards the new content is written.
If this input pin is briefly connected to V_{DD}, the selected band output changes in the sequence written below, to obtain a step-by-step band selection.

VHF III
UHF
VHF I
AV
VHF III and so on

Pin 3 - Fine tuning +/— (on panel)

This input accepts the Fine tuning +/— commands given from the panel.
The commands are accepted according to the following rules:

Input levels	Command
M (input floating)	No command
H	FT +
L	FT —

Each command corresponds to one step change; to have more changes the key must be released and the command repeated.

Pin 4 - T input (fine tuning +/— from remote control)

The Fine tuning +/— commands given from Remote control are applied to this input in the form of a series of positive pulses.
Short pulses ($\gtrsim$ 1.8 ms) correspond to the FT—command while long pulses ($\lesssim$ 1.8 ms) correspond to the FT + command.
This input is compatible with the T output of M 1130 Remote control receiver.
When the Fine tuning command is given, the duty cycle of the output of pin 19 (Fine tuning output) is changed at the rate of one step every 0.56 sec.
If the pulses are present for less than 0.56 sec. step-by-step operation can be obtained.
If this input is not used it must be connected to V_{SS} (GND).

Pins 5-6-7-8 - Program inputs

This 4-line bus selects the program according to the truth table given below:

Program	PA	PB	PC	PD
1	L	L	L	L
2	H	L	L	L
3	L	H	L	L
4	H	H	L	L
5	L	L	H	L
6	H	L	H	L
7	L	H	H	L
8	H	H	H	L
9	L	L	L	H
10	H	L	L	H
11	L	H	L	H
12	H	H	L	H
13	L	L	H	H
14	H	L	H	H
15	L	H	H	H
16	H	H	H	H

Pin 9 - V_{PP} - Memory supply

A series of pulses is applied to this pin during the store cycle. The timing of these pulses is given by the output of pin 14 and it is different during erase and write cycle as shown in fig. 2 and 3.
During a store cycle the old word is at first cancelled and the new one is written afterwards.

Fig. 2 - Memory Erase supply

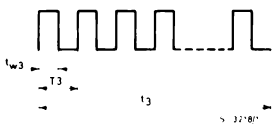
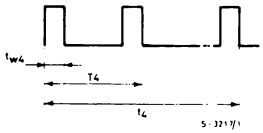


Fig. 3 - Memory Write supply



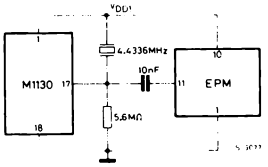
Pin 10 - V_{DD1}

This pin has to be connected to a power supply with the characteristics shown in the recommended operating conditions.

Pin 11 - Clock input

When the device is used alone the internal oscillator operates with a 4.43 MHz crystal or parallel LC network connected between pin 11 and ground.
It can also operate with a single crystal together with M1130 as shown in fig. 4.

Fig. 4



Pin 12 - Search speed

An external RC network is connected to this pin in order to set the frequency of the internal oscillator which, in turn, sets the scan speed during Search mode.
The scan speed can be adjusted over a wide range.
The relationship of search speeds between UHF, VHF and AV is a follows:

Automatic:

FAST UP VHF = the frequency externally fixed
FAST UP UHF = AV = 1/2 FAST UP VHF
MEDIUM DOWN VHF = 1/4 FAST UP VHF
MEDIUM DOWN UHF = AV = 1/4 FAST UP UHF (1/8 FAST UP VHF)
SLOW UP VHF = UHF = AV = 67.7 Hz
SLOW DOWN VHF = UHF = AV = 8.4 Hz

Manual: UP or DOWN UHF = AV = 1/2 UP or DOWN VHF

The manual Fast up or down speed is obtained by changing the frequency of the oscillator. The maximum capacitance which should be connected to this pin is 100 nF.

Pin 13 - V_{DD2}

This pin has to be connected to a power supply with the characteristics indicated in the recommended operating conditions.

Pin 14 - Memory write timing output

This output gives the timing for the pulses to be applied on pin 9 during the store cycle. The output consists of an open drain transistor.
The waveforms are shown in fig. 5 and 6, and are different during erase and write cycle, as already described for pin 9.

Fig. 5 - Memory Erase Current

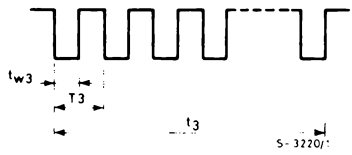
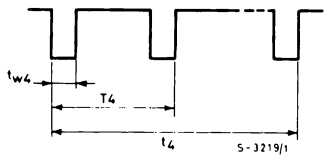


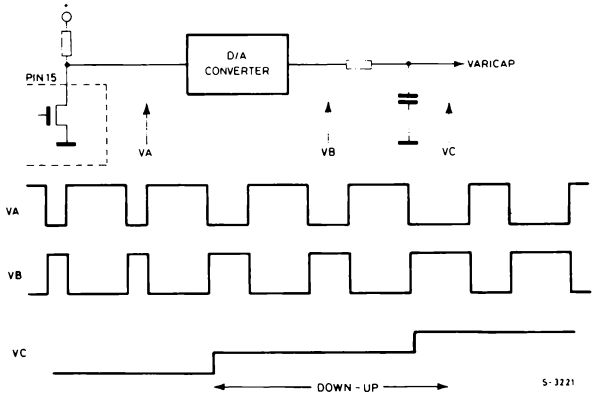
Fig. 6 - Memory Write Current



Pin 15 - Digitized tuning voltage output

The output consists of a variable frequency/variable width pulse train which, after filtering, provides the tuning voltage to the varicaps.
This signal carries 13 bits of information (only 12 bits however are stored in the memory).
The output circuit consists of an open drain transistor which offers a low impedance to ground when in the ON state.
The output waveforms are shown in fig. 7.

Fig. 7



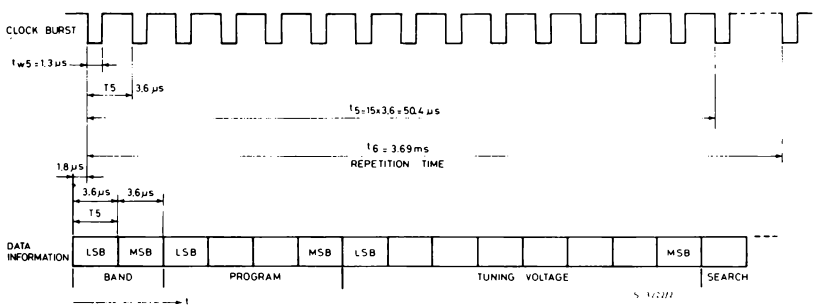
Pin 16 - Clock output for external display

A burst containing 15 clock pulses is available on this pin. These clock pulses are synchronized with Data Information as described in fig. 8.

Pin 17 - Data information output for external display

A 15 bit burst is available on this pin.
It contains the 8 most significant bits of the digitized tuning voltage, 2 bits for band information, 4 bits for program information and 1 bit which indicates whether the system is in the Search mode (both in automatic and manual). The Data Information is complementary form (see fig. 8).
These two outputs (pins 16 and 17) work in connection with the M191 (On screen tuning bar display).
When the burst is not transmitted, the output transistor is in the off position.

Fig. 8



Pins 18 - 21 - Test pins

These pins must be connected to V_{SS} (GND).

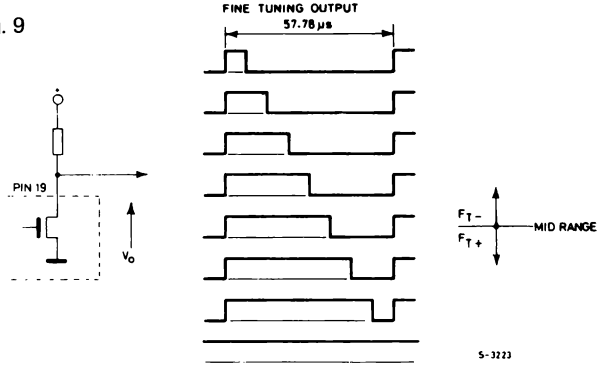
Pin 19 - Fine tuning output

Fine tuning information is available on this pin in the form of a square wave having a frequency of 17305 Hz and duty cycle variable in 8 positions as indicated in fig. 9.
The voltage generated after filtering is fed to the AFC loop and detunes the receiver by a small Δf while maintaining the action of the AFC.
The Fine tuning function operates as follows:

- during the search the output is set at mid-range (see fig. 9). (In the M193 only in automatic mode).
- when the search has been completed it is possible to operate on the Fine tuning +/− commands (pin 3 for Remote control operation or pin 4 for panel operation). The Store command memorizes this information together with the 12 bit tuning voltage and 2 bit band information
- when a memorized program is recalled it is still possible to act on the Fine tuning commands.

Any change in Fine tuning is only memorized by the Store command.

Fig. 9



Pin 20 - Automatic/manual selection

This pin is used to change the Search mode. When it is connected to V_{DD} the system operates in Automatic mode; when it is at V_{SS} (GND) the system works manually. The change Auto-manual or viceversa can be made at every time without precluding the right operation of the system.

Pin 22 - Stop/afc input

This pin is used only in automatic search mode.
When the EPM is manual operation this pin is internally disabled.
The Stop/afc is also internally disabled during any program change for the time the Mute signal lasts. This input can have three different levels: high (H), middle (M), low (L). The middle level, unlike the other three level inputs of the circuit, is not internally generated and has to be externally determined according to the recommended operating conditions. If this input is not used it has to be connected to V_{SS} (GND) or to V_{DD2}.

The input has two different functions depending on whether the system is in the search or in normal operation (AFC control).

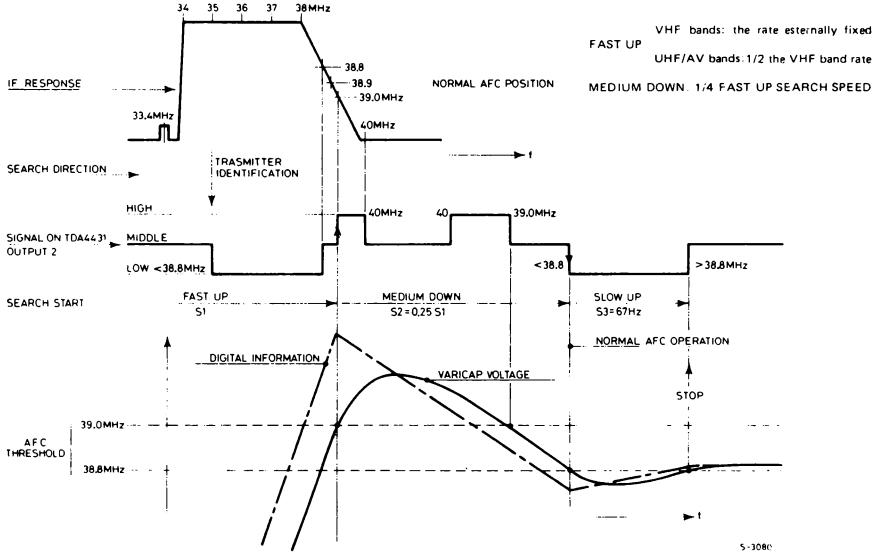
A) **Search mode:** after depressing the Search start key, the transitions and levels of the signals coming from the TDA 4431, applied to this pin, control the search function and determine when the search must stop, i.e. a TV station has been recognized.
The circuit operates with the following sequence (see fig. 10 for reference and explanation of pin 12 for speed definition):

1 - after pressing the search start key the search occurs in the Fast up mode

2 - subsequent transitions on pin 22 Stop/afc input are ignored during the first 15 search steps. After that the first M-H transition on the input preceded by at least one M-L transition will set the search into the Medium down (fast up/4) mode.
The acceptance delay of 15 search steps has been introduced to avoid the condition where the system could stop on the previous station (for example in the case the search start command has been given just before an AFC control command).

3 - the next M-L transition will switch the search to Slow up speed (67.7 Hz).
At this point the system is in normal AFC operation.

Fig. 10 -- Automatic station capture diagram



B) **AFC operation:** when a station is perfectly tuned, the input signal coming from TDA 4431 is at middle level.
If the tuning moves lower than the threshold (below 38.9 MHz), the pin 22 goes low and the 13 bit internal counter is moved with Slow up speed to determine an increasing of the varicap voltage. When a detuning occurs in the opposite direction the input will go high and the tuning voltage is decreased with Slow down speed (8.4 Hz).
The increase or decrease of the tuning voltage is stopped as soon as the input returns to M level. Therefore during normal operation pin 22 acts as AFC control command.

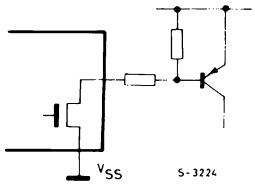
C) **Recall from memory:** when the circuit is in automatic operation mode and a pre-memorized program is recalled from Memory, a fixed value of 8 steps (≅ 31.2 mV) is subtracted from the tuning voltage. This corresponds to a detuning of about 0.6 MHz (UHF) and of 0.3 MHz in VHF III into that part of the IF response curve which corresponds to the fully transmitted sideband.
At this point the AFC operation takes over as described in point B) above and the exact tuning is reached in about 0.2 sec.
Due to this feature the AFC capture ratio will be increased and the requirements for stability of the tuner, of the reference voltage sources and of stability of the D/A converter are less severe.
In manual operation mode the memory content is instead read without any change.

Pins 23-24-25-26 - Band drive outputs

The information for band selection is present on these outputs, consisting of open drain transistors, one of which, in connection with the selected band, is conducting (see fig. 11).
The relations between pins and bands are as follows:

Pin 23 = VHF I
Pin 24 = VHF III
Pin 25 = UHF
Pin 26 = AV

Fig. 11



Pin 27 - Mute output

A source follower transistor is provided to give a high level output during mute function.
The mute is present in the following cases:

- during automatic search. The mute is present 110 msec before the start of the search.
- during any program change for 320 msec.
  The mute is active 110 msec before the program change takes place.
- when the supply voltage V_{DD2} is applied, for about 320 msec.
- when the supply voltage V_{DD2} is removed.

Pin 28 - A) Automatic operation: search start
B) Manual operation: up/down search

This input is a three level one, i.e. it is normally in the middle level and the above mentioned functions are activated when it is connected to V_{DD2} or to GND.
The input is kept at a voltage corresponding to about the half of the supply voltage by an internal divider made with two resistors of about 1 Mohm.

A) Automatic operation

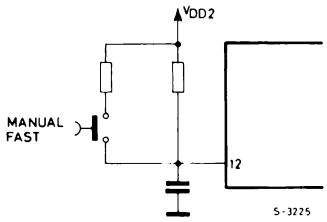
When the pin 28 is briefly connected to GND the search starts on the bands VHF III-UHF which are scanned in sequence. If it is connected to V_{DD2} the search is made on band VHF I and AV.
If the key is kept pushed, another search can start only by releasing the key and connecting it again to GND or V_{DD2}.
If a Search start command is given while the system is already in search operation, the search is immediately stopped and after restarted on the new group of selected bands; the band where the system will search is that which has the same search speed of the previous one.
During the search the tuning voltage is always changing from lower to higher voltage levels.
The search is automatically stopped when the first station is found.
The search is also stopped whenever a program change command is given.
When the upper limit of the tuning voltage is reached, the search restarts from the lower limit of another band after 210 msec of temporary stop.
The search speed is determined by the RC network connected to pin 12.

B) Manual operation

When the input is connected to V_{DD2} the content of the internal counter is changed in such a way to have an increasing of the varicap voltage.
If the input is connected to GND the varicap voltage is decreased.
The search speed is determined by the RC network applied on pin 12.

Fast/low search speed is possible by changing the value of the same RC network (see fig. 12).
In manual operation the search is always made in the same band.
No inhibit of the search is provided when the lower or the upper limits of the varicap voltage are reached.
Step-by-step band selection is possible by temporarily connecting pin 2 to V_{DD2}.

Fig. 12



GENERAL INFORMATION

Command acceptance rules

1) When a manual command at pin 2, 3, 28 is given, an internal counter is immediately started. The command is accepted only after about 31 msec. of its continuous presence. If the command disappears before (for example in consequence of contact bouncing), the counter is immediately reset. When a command has been accepted, no other manual command is accepted until the previous command has been released.

2) Program change commands are immediately accepted and if the circuit is in the automatic search position, the search is stopped.
Manual commands given during the execution of the program change are not accepted except the automatic search start command.
This one is internally stored and executed at the end of the program change.

3) During the store cycle only the program change and the search start commands are accepted and executed at the end of the cycle.
The other commands are ignored.

MOS INTEGRATED CIRCUIT

M 251

ARPEGGIO, CHORD AND BASS ACCOMPANIMENT GENERATOR

CHOICE OF OPERATING MODE:
- AUTOMATIC WITH MEMORIZATION OF THE SELECTED KEY
- SEMIAUTOMATIC WITH MEMORIZATION OF THE SELECTED KEYS
- SEMIAUTOMATIC WITHOUT MEMORIZATION OF THE SELECTED KEYS

SIMPLE KEY SWITCH REQUIREMENTS (24 NOTE KEYBOARD WITH ONE SWITCH PER KEY)
INTERNAL ANTI-BOUNCE CIRCUITS
THREE OUTPUTS FOR THE ARPEGGIOS
ANALOG OUTPUT FOR CHORDS
BASS OUTPUT (AUTOMATIC OR ALTERNATE)
TRIGGER OUTPUTS FOR PERCUSSION EFFECT ON BOTH ARPEGGIO AND BASS SECTIONS
MULTIPLE CHOICE POSSIBILITY ON THE CHORDS IN AUTOMATIC MODE:
- MAJOR OR MINOR THIRD
- FIFTH OR DIMINISHED FIFTH
- SIXTH OR SEVENTH

LOW DISSIPATION: $<$400 mV TYP.
STANDARD SUPPLIES (+ 5V AND - 12V)
INPUTS PROTECTED FROM ELECTROSTATIC DISCHARGE

The M 251 is realized on a single monolithic silicon chip using low threshold P-channel silicon gate MOS technology. It is available in a 40-lead ceramic or plastic package.

ABSOLUTE MAXIMUM RATINGS

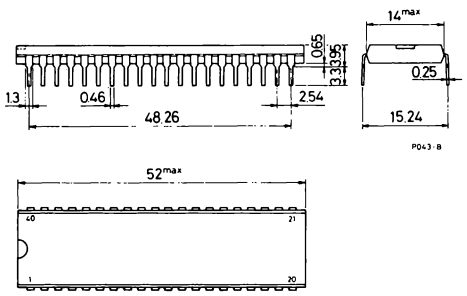
V_{GG}*	Source supply voltage	-20 to 0.3	V
V_I*	Input voltage	-20 to 0.3	V
I_O	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

* This voltage is with respect to V_{SS} pin voltage

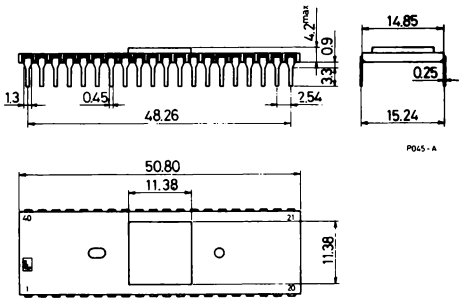
ORDERING NUMBERS: M 251 B1 AC for dual in-line plastic package
M 251 D1 AC for dual in-line ceramic package

MECHANICAL DATA (dimensions in mm)

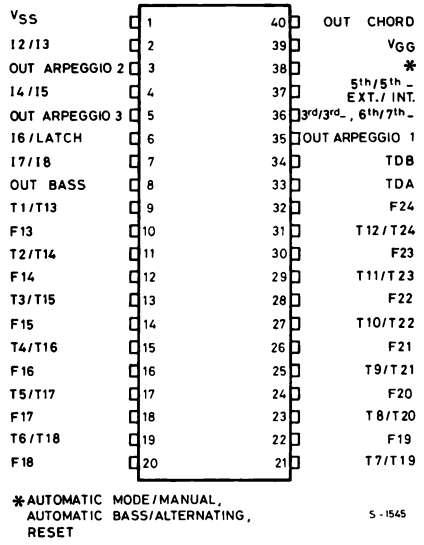
M 251 B1 AC



M 251 D1 AC



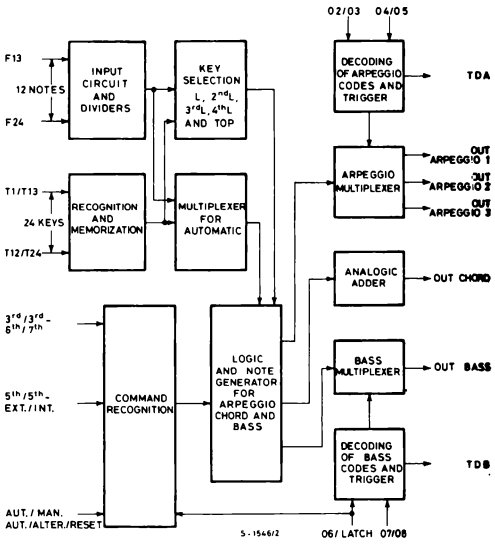
CONNECTION DIAGRAM



*AUTOMATIC MODE/MANUAL, AUTOMATIC BASS/ALTERNATING, RESET

S-1545

BLOCK DIAGRAM



GENERAL CHARACTERISTICS

The circuit comprises:

a) 12 pins for input frequencies

b) 12 inputs from the keyboard with the possibility to provide the control of two octaves (in semiautomatic modes only) by multiplexing the two octaves. In automatic mode the second octave repeats the first

c) 4 multiplexed data inputs for addressing the internal selection circuits. These inputs are normally coming from the outputs of an external memory

d) 5 signal outputs: arpeggio 1, arpeggio 2, arpeggio 3, bass and chord respectively

e) 2 trigger outputs: arpeggio (TDA), and bass (TDB), respectively. These outputs, in conjunction with an external time-constant, allow the formation of the envelope of the arpeggio and bass notes.
The duration of the trigger pulses is equivalent to one period of the external memory clock line

f) 3 inputs for mode selection

g) 2 supply pins.

M 251 is normally used in conjunction with an external self-scanning ROM (such as the M 252 - 3 or 4) which performs the selection of the various notes in the arpeggio/chord/bass accompaniment.

AUTOMATIC OPERATION

When a number of keys in the two available octaves are played, the lowest key is taken as a reference by the circuit and this note is memorized internally. When the lowest key played changes, the memory is erased and the new information from the keyboard is now fed into the circuit and memorized. When all the keys are released the last "update" is held in the memory and is only changed when a different lowest key is played. If keys in the upper octave only are played then the two octaves act in parallel. The memorized key by means of the internal multiplexer selects the corresponding tonic and all the other notes programmed for arpeggio, chord and bass accompaniment in the correct relationship of intervals. Internal dividers provide all the octaves we need as shown in the tables below. By means of the external commands it is possible to choose between major third and minor third, between fifth and diminished fifth and between sixth and seventh. To reset the key memorized at the end of a piece played the automatic signal must be interrupted for a moment while none of the keys on the two available octaves is played.

ARPEGGIO TRUTH TABLE (positive logic)

EXTERNAL MEMORY CODE				SELECT 6th			SELECT 7th		
05	04	03	02	ARP. I	ARP. II	ARP. III	ARP. I	ARP. II	ARP. III
1	1	1	1	TONIC	3rd	5th	TONIC	3rd	5th
1	1	1	0	3rd	5th	TONIC x 2	3rd	5th	7th
1	1	0	1	5th	TONIC x 2	3rd x 2	5th	7th	3rd x 2
1	1	0	0	6th	—	—	7th	—	—
1	0	1	1	TONIC x 2	3rd x 2	5th x 2	7th	3rd x 2	5th x 2
1	0	1	0	3rd x 2	5th x 2	TONIC x 4	3rd x 2	5th x 2	TONIC x 4
1	0	0	1	5th x 2	TONIC x 4	3rd x 4	5th x 2	TONIC x 4	3rd x 4
1	0	0	0	6th x 2	—	—	7th x 2	—	—
0	1	1	1	TONIC x 4	3rd x 4	5th x 4	TONIC x 4	3rd x 4	5th x 4
0	1	1	0	3rd x 4	5th x 4	TONIC x 8	3rd x 4	5th x 4	7th x 4
0	1	0	1	5th x 4	TONIC x 8	3rd x 8	5th x 4	7th x 4	3rd x 8
0	1	0	0	6th x 4	—	—	7th x 4	—	—
0	0	1	1	TONIC x 8	3rd x 8	5th x 8	7th x 4	3rd x 8	5th x 8
0	0	1	0	3rd x 8	5th x 8	TONIC x 8	3rd x 8	5th x 8	7th x 8
0	0	0	1	5th x 8	TONIC x 8	3rd x 8	5th x 8	6th x 8	3rd x 8
0	0	0	0	No Change	No Change	No Change	No Change	No Change	No Change

VERY IMPORTANT NOTE: TONIC is the input note, corresponding to the selected key, divided by 16. 3rd is the correct third corresponding to this TONIC. And so on.

BASS and CHORD TRUTH TABLES (positive logic)

EXTERNAL MEMORY CODE 08	07	06	AUTOMATIC BASS
1	1	1	2nd/2
1	1	0	8ve/2
1	0	1	9th/2
1	0	0	6th or 7th/2
0	1	1	5th/2
0	1	0	3rd/2
0	0	1	TONIC/2
0	0	0	NO CHANGE

"NO CHANGE" is interpreted as an instruction to sustain the previous notes until new information is presented.

EXTERNAL MEMORY CODE 07	06	ALTERNATE BASS
1	1	–
1	0	TONIC/2
0	1	5th/2
0	0	NO CHANGE

EXTERN. MEMORY CODE 01	CHORD	
	SELECT 6th	SELECT 7th
1	TONIC +3rd +5th	TONIC +3rd +5th +7th
0	NO CHANGE	NO CHANGE

SEMIAUTOMATIC OPERATION WITH MEMORIZATION OF THE KEYS

When any number of keys are played within the two available octaves they are memorized and sent to an internal recognition circuit which selects the lowest four keys, the top key played and their respective frequencies. This information is updated every time a different group of keys is played. Between the playing of two groups of keys there must be a pause during which none of the keys is down, otherwise the new group of keys is memorized without the previous group being cancelled. Again the keys recognized can be extended to more octaves by means of the internal divider. The following are positive logic truth tables showing the actual keys,instead of the notes.Top is the first key from the right(the top key played), L the lowest key played, and 2L the second lowest and so on. The relationship between keys and input frequencies is as follows: L in the first octave to the left represents corresponding input note divided by 16, while in the second octave it is divided by 8. And so on. To erase the memorization at the end of a piece played it is necessary to select "automatic" for a moment and then return to semiautomatic while none of the keys is played. The trigger signals, TDA and TDB, are sent out only if 3 or more keys are played.

ARPEGGIO TRUTH TABLE (positive logic)

EXTERNAL MEMORY CODE 05	04	03	02	MEANING OF THE CODES ARP. I	ARP. II	ARP. III
1	1	1	1	L	2nd L	3rd L
1	1	1	0	2nd L	3rd L	L x 2
1	1	0	1	3rd L	L x 2	2nd L x 2
1	1	0	0	4th L	–	–
1	0	1	1	L x 2	2nd L x 2	3rd L x 2
1	0	1	0	2nd L x 2	3rd L x 2	L x 4
1	0	0	1	3rd L x 2	L x 4	2nd L x 4
1	0	0	0	4th L x 2	–	–
0	1	1	1	L x 4	2nd L x 4	3rd L x 4
0	1	1	0	2nd L x 4	3rd L x 4	L x 8
0	1	0	1	3rd L x 4	L x 8	2nd L x 8
0	1	0	0	4th L x 4	–	–
0	0	1	1	L x 8	2nd L x 8	3rd L x 8
0	0	1	0	2nd L x 8	3rd L x 8	L x 8
0	0	0	1	3rd L x 8	L x 8	2nd L x 8
0	0	0	0	NO CHANGE	NO CHANGE	NO CHANGE

BASS and CHORD TRUTH TABLES (positive logic)

EXTERNAL MEMORY CODE 08 07 06	AUTOMATIC BASS OUTPUT	ALTERNATE BASS OUTPUT
1 1 1	TWO 8ve BELOW TOP	–
1 1 0	L	–
1 0 1	ONE 8ve BELOW TOP	–
1 0 0	ONE 8ve BELOW 4th L	–
0 1 1	ONE 8ve BELOW 3rd L	–
0 1 0	ONE 8ve BELOW 2nd L	ONE 8ve BELOW L
0 0 1	ONE 8ve BELOW L	ONE 8ve BELOW TOP
0 0 0	NO CHANGE	NO CHANGE

EXTERN. MEMORY CODE 01	CHORD OUTPUT
1	L +2nd L +3rd L +4th L
0	NO CHANGE

"NO CHANGE" is interpreted as an instruction to sustain the previous notes until a new information is presented.

SEMIAUTOMATIC OPERATION WITHOUT MEMORIZATION OF THE KEYS

This method of operation is the same as the previous one except that the keys are not memorized.

CHARACTERISTICS COMMON TO ALL 3 MODES OF OPERATION

The signals from the keyboards, those from the external memory and those for selecting the mode of operation have to be multiplexed into the M 251 since the number of pins available is not enough. The method used to differentiate between the two distinct commands applied to the multiplexed input pins is as follows: two anti-phase pulse trains are generated internally from the highest note in the upper octave (pin 32). These two pulse trains are used to separate the input information during the "1" and "0" status of F24. With AUTOMATIC mode and EXTERNAL command selected the four frequencies of the highest octave can be made available at pins 2, 3, 4 and 5 as the 8 x tonic, 8 x major 3rd or 8 x minor 3rd, 8 x 5th or 8 x diminished 5th and 8 x 6th or 8 x 7th. Likewise in semiautomatic mode, the L x 8, 2nd x 8, 3rd x 8, 4th x 8 notes selected appear at the respective pins. These signals give the designer considerable flexibility in the formation of accompaniments not directly produced by the M 251 itself.

EXTERNAL MODE OUTPUTS

T1 is the key farthest to the left of the keyboard. For "L" see SEMIAUTOMATIC OPERATION WITH MEMORIZATION OF THE KEYS. In the external mode the four frequencies of the highest octave appear at pins 2, 3, 4 and 5 as shown in the table.

PIN N°	AUTOMATIC MODE	SEMI-AUTOM.
2	8 x TONIC	8 x L
3	8 x FIFTH DIMINISHED FIFTH	8 x 3rd L
4	8 x MAJOR THIRD OR MINOR THIRD	8 x 2nd L
5	8 x SIXTH OR SEVENTH	8 x 4th L

STATIC ELECTRICAL CHARACTERISTICS (positive logic, V_{GG}= -11 to -13V, V_{SS}= 4.75 to 5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
INPUT SIGNALS							
V_{IH}	Input high voltage	note 1		V_{SS}-2.5		V_{SS}	V
		note 2		V_{SS}-1		V_{SS}	V
V_{IL}	Input low voltage	note 1		V_{GG}		V_{SS}-6	V
		note 2		V_{GG}		V_{SS}-4	V
I_{LI}	Input leakage current	V_i=V_{SS}-14V	T_{amb}= 25°C			10	μA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OUTPUT SIGNALS*						
R_{ON}	Output resistance	V_o=V_{SS}-1 to V_{SS}		300	500	Ω
V_{OH}	Output high voltage	I_o = 1 mA	V_{SS}-0.5		V_{SS}	V
$I_{o(off)}$	Output leakage current	$V_i = V_{IH}$ V_o=V_{SS}-10V T_{amb}= 25°C			10	µA
POWER DISSIPATION						
I_{GG}	Supply current	T_{amb}= 25°C		20	30	mA
CHORD OUTPUT SIGNAL						
ΔV_o	Variation in output voltage (for each note)	R_L = 5 kΩ	1	1.5	2	V
R_L	External resistance connected between the output and V_{GG}				5	kΩ
R_O	Output dynamic resistance		10			MΩ
V_O	Output voltage when no note is present	R_L = 5 kΩ	V_{GG}+8		V_{GG}	V

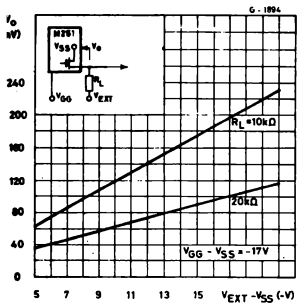
Note 1: Refers only to the F13 - F24 inputs
Note 2: Refers to the other inputs
* With the exception of the chord output

DYNAMIC ELECTRICAL CHARACTERISTICS (positive logic V_{GG}= -11 to -13V, V_{SS}= 4.75 to 5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

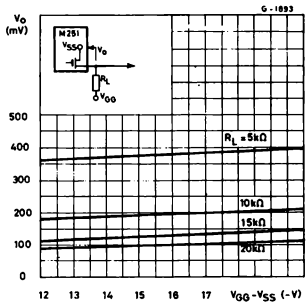
Parameter		Min.	Typ.	Max.	Unit
f_i	High input frequency (F 24)	1	4	12	kHz
t_1	Delay time of the internal phases	0.5	0.7	1	µs
t_2	Length of the internal phases	3	6	15	µs
t_3	Set-up time between data IN and F24	10		T/4	µs
t_4	Hold time between F24 and data IN	30		T/4	µs
t_5	Delay time between falling edge of external memory code and TDA or TDB	1.5T		2.5T	µs
t_6	Delay time of the internal strobe pulse	T		2T	µs
t_7	Length of the internal strobe pulse		T/2		µs
T_1	Period of external code pulses	3T			µs
T_2	Return to zero or no significant external code	2T			µs

T is the period of F24 with duty-cycle of 50%
All the times are measured at 50% of the swing

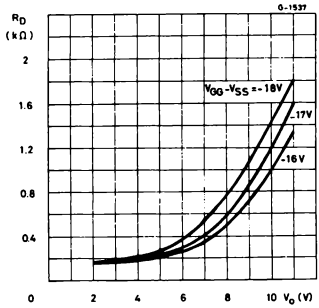
*Output voltage vs. external supply voltage (V_{EXT}-V_{SS})



*Output voltage vs. supply voltage (V_{GG}-V_{SS})



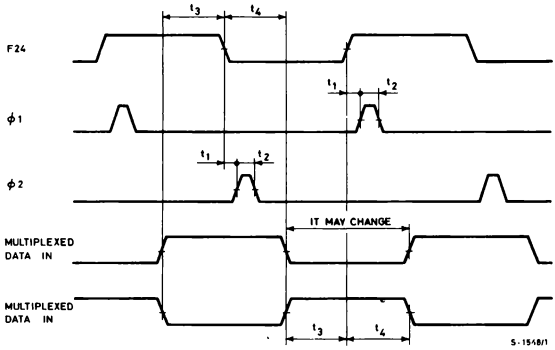
*Output dynamic resistance vs. output voltage



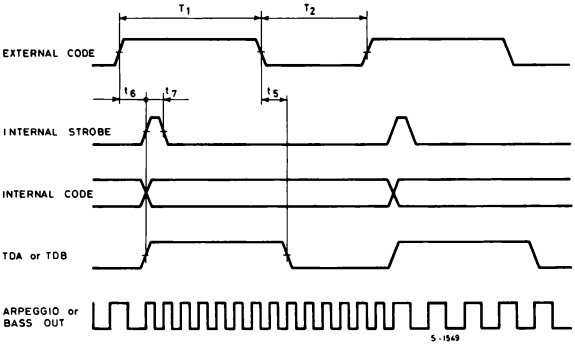
* With the exception of the chord output

TIMING WAVEFORMS (positive logic)

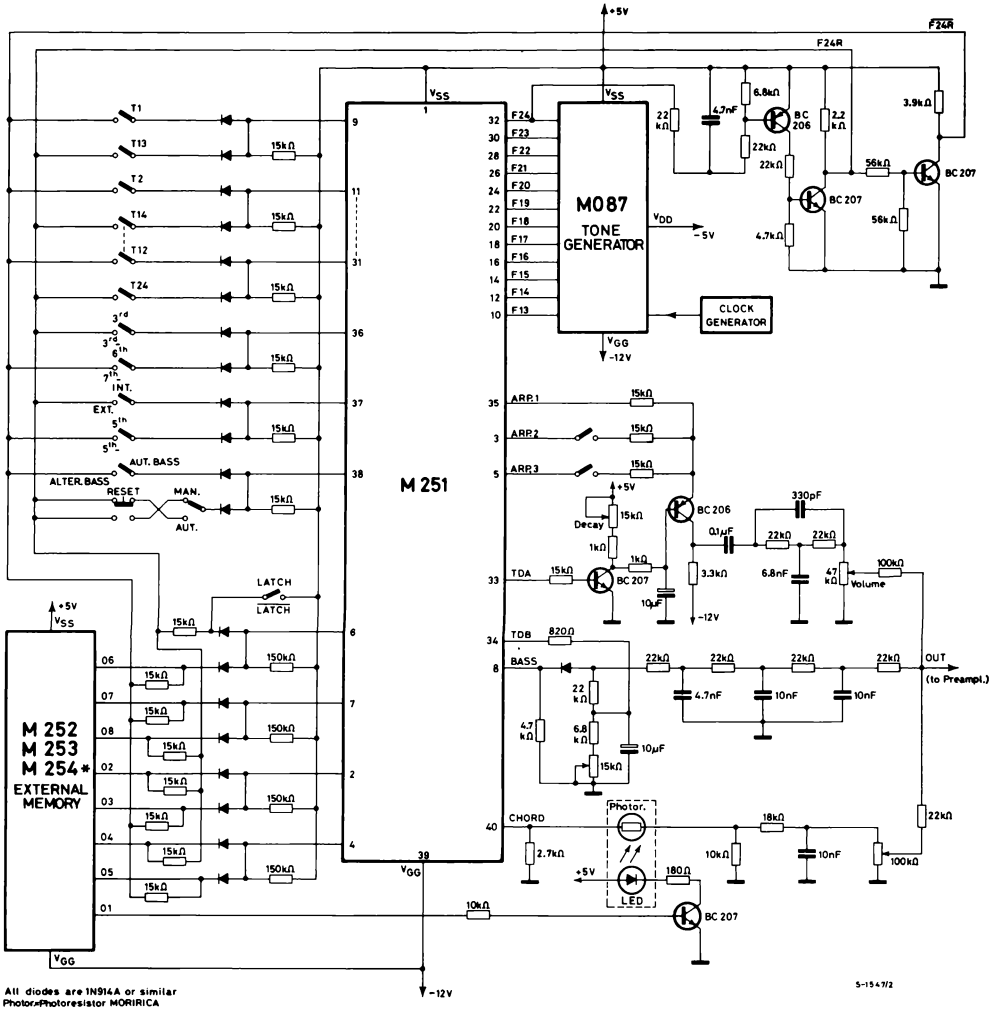
Internal phases (ϕ 1 and ϕ 2) and timing for data inputs



Internal strobe, internal code and TDA or TDB as a function of the external code



TYPICAL APPLICATION



* For this application a version of the M 254 with standard memory content is available both for interfacing with the M 251 and for driving 4 instrument simulators (8 rhythms). Ordering number is M 254 AD.

MOS INTEGRATED CIRCUIT

M 252

RHYTHM GENERATOR

- LOW POWER DISSIPATION: < 120 mW
- DRIVES 8 COUND GENERATORS (INSTRUMENTS)
- 15 PROGRAMMABLE RHYTHMS (NOT AVAILABLE IN COMBINATION)
- MASK PROGRAMMABLE RESET COUNTS: 24 or 32
- DOWN BEAT OUTPUT
- EXTERNAL RESET
- OPEN DRAIN OUTPUTS
- STANDARD MUSIC CONTENT AVAILABLE
- TECHNICAL NOTE NO 131 AVAILABLE FOR FULL INFORMATION

The M252 is a monolithic rhythm generator specifically designed for electronic organs and other musical instruments.
Constructed on a single chip using low threshold P-channel silicon gate technology it is supplied in a 16-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{GG} **	Source supply voltage	-20 to 0.3	V
V_I **	Input voltage	-20 to 0.3	V
I_o	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

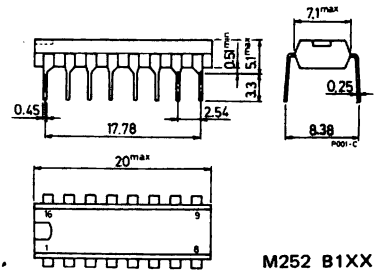
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** This voltage is with respect to V_{SS} pin voltage.

ORDERING NUMBERS: M252 B1 XX for dual in-line plastic package
M252 B1 AA and AD for standard music content

MECHANICAL DATA

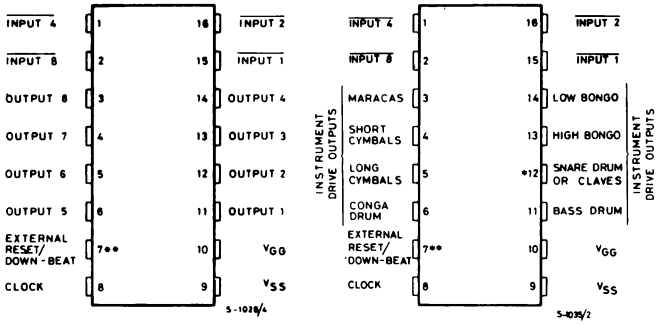
Dimensions in mm



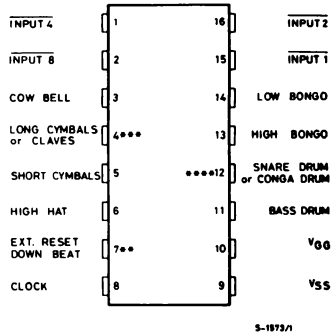
M252 B1XX

CONNECTION DIAGRAMS

Standard content configuration
M252 B1 AA



Standard content configuration
M252 B1 AD



* This output must be connected so as to drive the "snare drum" when the rhythms from 1 to 9 (see rhythm selection) are selected, and the "claves" when the rhythms from 10 to 15 (see rhythm selection) are selected.

** This pin generates a down-beat trigger which can be used to drive an external lamp to indicate the first beat of the first bar of each rhythm.

*** This output must be connected so as to drive the "long cymbals" when the rhythms number 1, 3, 4, 12 and 14 are generated, and the "claves" when the rhythms number 5, 8, 9, 10, 11 and 13 are generated.

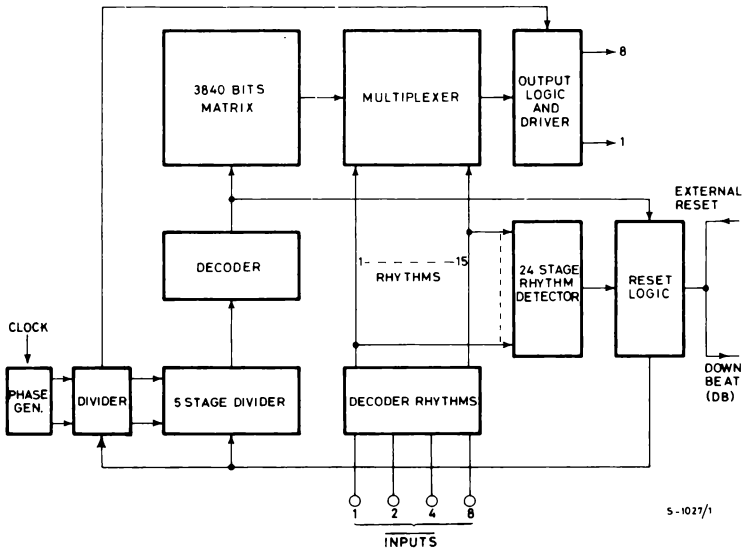
**** This output must be connected so as to drive the "snare drum" when the rhythms number 1, 3, 4, 6, 7, 9, 12, 14 and 15 are generated, and the "conga drum" when the rhythms number 5, 8, 10, 11 and 13 are generated.

RHYTHM SELECTION

The following binary code must be generated to select each rhythm (positive logic)

RHYTHM	CODE				STANDARD CONTENT-AA		STANDARD CONTENT-AD	
	$\overline{\text{INPUT 8}}$	$\overline{\text{INPUT 4}}$	$\overline{\text{INPUT 2}}$	$\overline{\text{INPUT 1}}$				
1	1	1	1	0	Waltz	3/4	Waltz	3/4
2	1	1	0	1	Jazz Waltz	3/4	Tango	2/4
3	1	1	0	0	Tango	2/4	March	2/4
4	1	0	1	1	March	2/4	Swing	4/4
5	1	0	1	0	Swing	4/4	Mambo	4/4
6	1	0	0	1	Foxtrot	4/4	Slow Rock	6/8
7	1	0	0	0	Slow Rock	6/8	Beat	4/4
8	0	1	1	1	Pop Rock	4/4	Samba	4/4
9	0	1	1	0	Shuffle	2/4	Bossa Nova	4/4
10	0	1	0	1	Mambo	4/4	Cha Cha	4/4
11	0	1	0	0	Beguine	4/4	Rhumba	4/4
12	0	0	1	1	Cha Cha	4/4	Beguine	4/4
13	0	0	1	0	Bajon	4/4	Bajon	4/4
14	0	0	0	1	Samba	4/4	Foxtrot	4/4
15	0	0	0	0	Bossa Nova	4/4	Shuffle	2/4
No selected rhythm	1	1	1	1				

BLOCK DIAGRAM

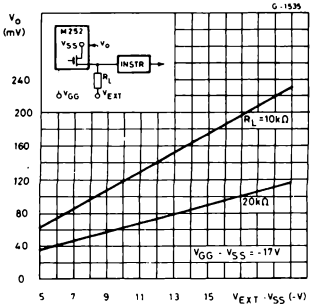


STATIC ELECTRICAL CHARACTERISTICS

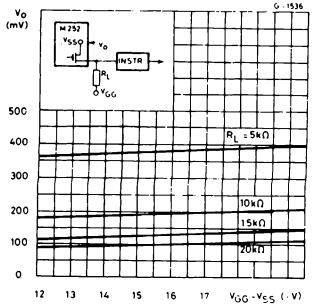
(positive logic, V_{GG} = -11.4 to -12.6V, V_{SS} = 4.75 to 5.25V, T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
CLOCK INPUT						
V_{IH}	Clock high voltage		V_{SS}-1.5		V_{SS}	V
V_{IL}	Clock low voltage		V_{GG}		V_{SS}-4.1	V
DATA INPUTS ($\overline{IN1}$ . . . . . $\overline{IN8}$)						
V_{IH}	Input high voltage		V_{SS}-1.5		V_{SS}	V
V_{IL}	Input low voltage		V_{GG}		V_{SS}-4.1	V
I_{LI}	Input leakage current	$V_i = V_{SS}$-10V T_{amb}= 25°C			10	µA
EXTERNAL RESET						
V_{IH}	Input high voltage		V_{SS}-1.5		V_{SS}	V
V_{IL}	Input low voltage		V_{GG}		V_{SS}-4.1	V
R_{IN}	Internal resistance to V_{GG}	$V_o = V_{SS}$-5V	400	600		KΩ
DATA OUTPUTS						
R_{ON}	Output resistance (ON state)	$V_o = V_{SS}$-1 to V_{SS}		250	500	Ω
V_{OH}	Output high voltage	I_L = 1 mA	V_{SS}-0.5		V_{SS}	V
I_{LO}	Output leakage current	$V_i = V_{IH}$ $V_o = V_{SS}$-10V T_{amb}= 25°C			10	µA
POWER DISSIPATION						
I_{GG}	Supply current	T_{amb}= 25°C		7	15	mA

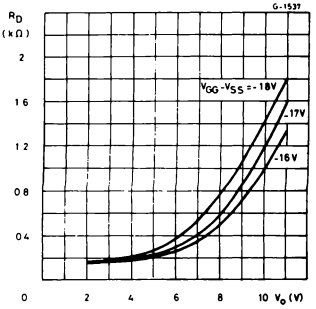
Output voltage vs. external supply voltage (V_{EXT}-V_{SS})



Output voltage vs. supply voltage (V_{GG}-V_{SS})



Output dynamic resistance vs. output voltage



DYNAMIC ELECTRICAL CHARACTERISTICS

(positive logic V_{GG} = -11.4 to -12.6V, V_{SS} = 4.75 to 5.25V, T_{amb} = 0 to 70°C unless otherwise specified)

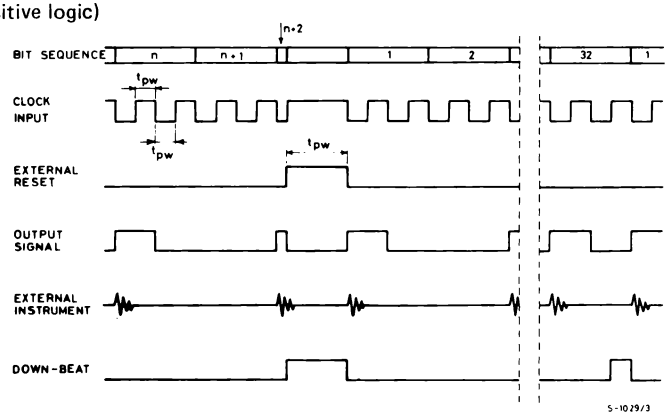
Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
CLOCK INPUT						
f	Clock repetition rate		DC		100	kHz
t_{pw}*	Pulse width		5			µs
t_r**	Rise time				100	µs
t_f**	Fall time				100	µs
EXTERNAL RESET						
t_{pw}	Pulse width		5			µs

* Measured at 50% of the swing.

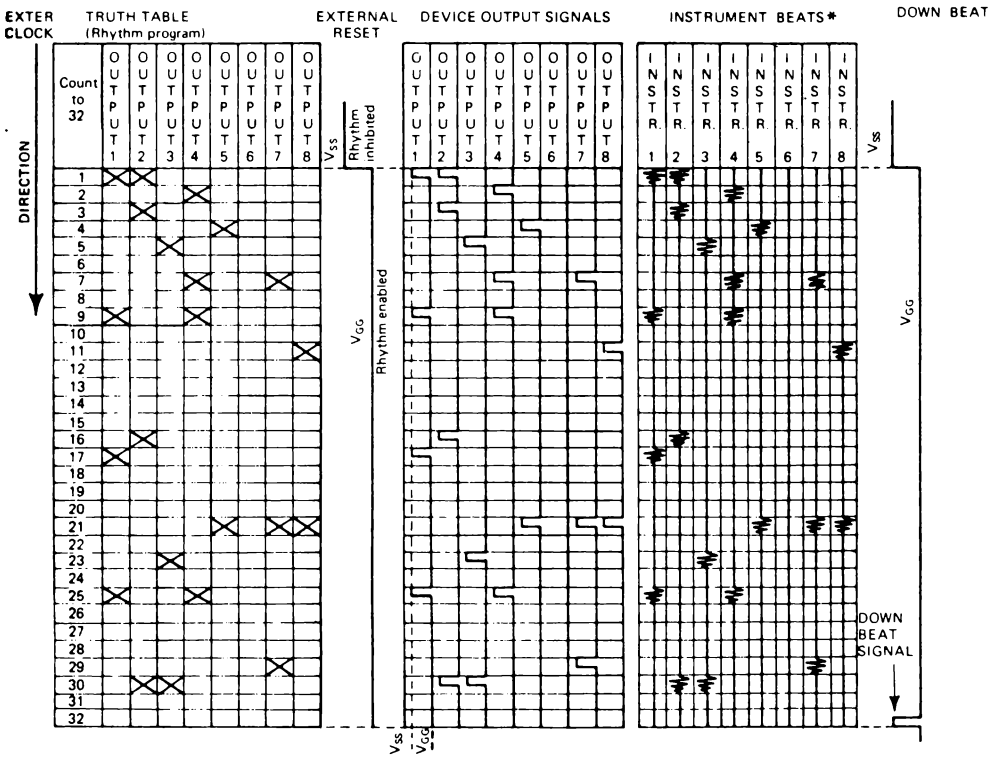
** Measured between 10% and 90% of the swing.

TIMING WAVEFORMS (positive logic)

Note: In these timing waveforms it has been assumed, for example, that in the truth table bits n + 1 and 2 have not been programmed i.e. the musical instrument has not been introduced. All the other bits have been programmed for the introduction of the instruments.



INSTRUMENT BEATS VERSUS RHYTHM PROGRAM



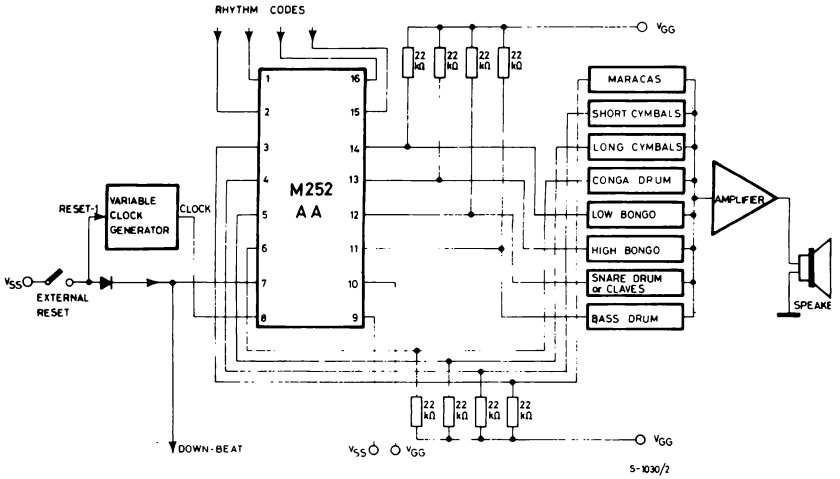
The lowering of the music signals depends on the intrinsic decay time of the sound generator and not on the length of the enable pulses. Each beat can therefore last for more than one elementary time.

TYPICAL APPLICATIONS

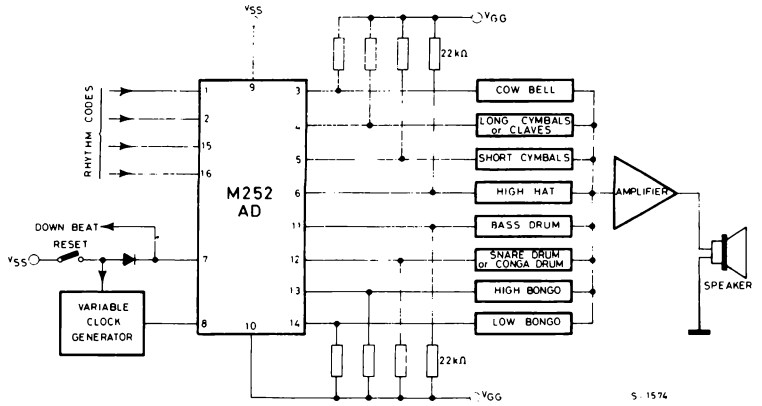
Figure 1 shows the typical application of the M252 (AA) and M252 (AD).
With two M252 devices it is possible to increase the number of rhythms or the number of instruments available, or the number of elementary times, as shown in figures 2, 3 and 4 respectively.
The use of a memory matrix allows the customer complete flexibility, since modification of the memory is quick and relatively cheap.

Fig. 1 - Rhythm system (standard contents)

a) M252 AA



b) M252 AD



TYPICAL APPLICATIONS (continued)

Fig. 2 - Increase in number of rhythms (positive logic)

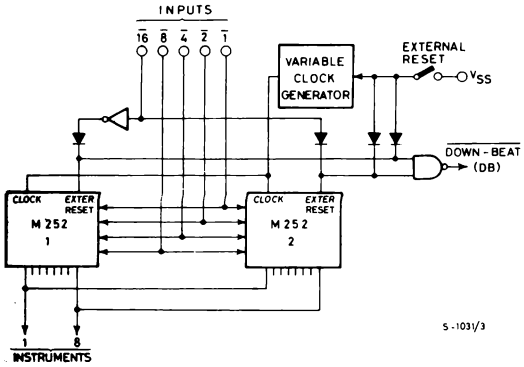


Fig. 3 - Increase in number of instruments

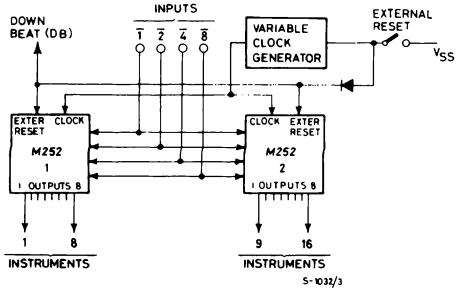
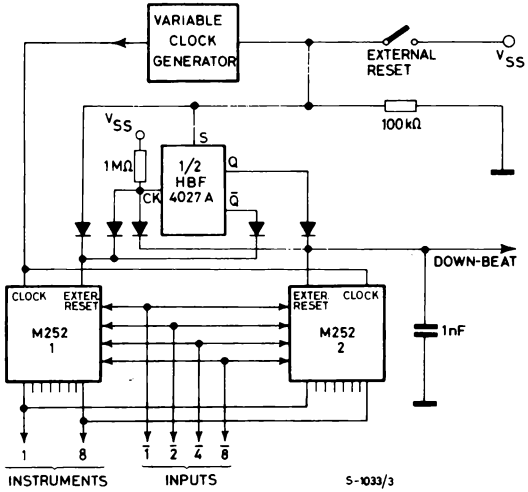
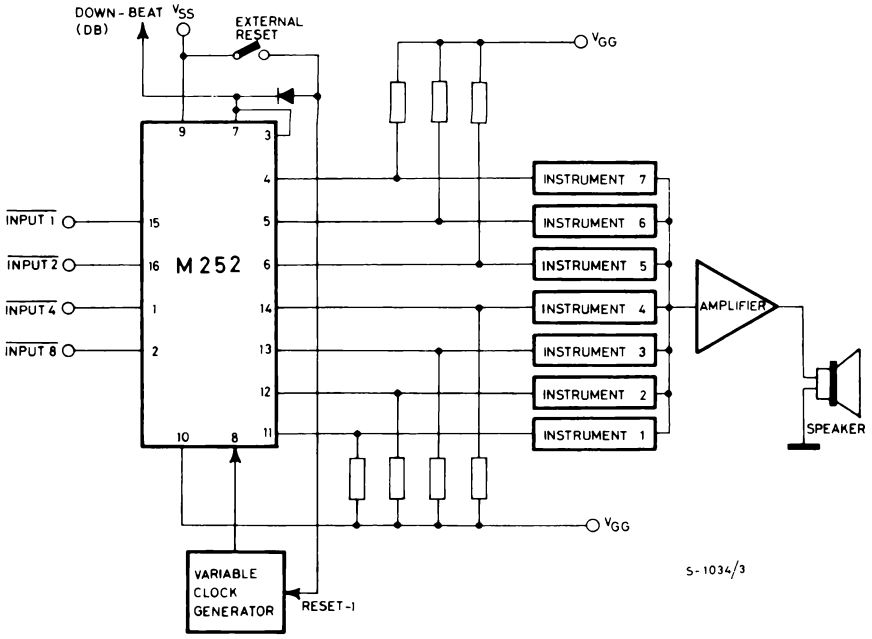


Fig. 4 - Increasing the number of elementary times



Note: The total number of elementary times is given by the sum of the elementary times of the individual devices.

CIRCUIT FOR CHANGING THE NUMBER OF ELEMENTARY TIMES



To obtain a required number of elementary times "N" simply put a cross in the "N + 1" position of the column which now represents the reset output, rather than the 8th instrument.
The DB output can be used as down-beat because it apperas at the beginning of each measure. Since the pulse is only 2 - 3 μs long it must, however, be stretched and buffered to enable it to drive a lamp.
Full information on the use of the M252 in electronic organs and other applications will be found in Technical Note no. 131 available on request.

COMPLETING THE TRUTH TABLE

The ROM truth table has been organized in 32 rows which represent elementary times and 120 columns (15 groups of 8) where each group represents a rhythm which has as its disposition 8 programmable instruments. To programme each rhythm one indicates (with a cross) in the appropriate boxes the timing for each beat required for each instrument.
Each cross corresponds to a beat of the indicated instrument or, in logic terms, to the presence of a "1" level (positive logic) at the output.
The absence of a cross indicates that the corresponding instrument is not used in that part of the rhythm.
Table 1 and 2 show the standard music content programmed into M252 AA and M252 AD respectively.

TABLE 1(M252 AA)

COUNT FOR 32	RHYTHM 1								RHYTHM 2								RHYTHM 3								RHYTHM 4								RHYTHM 5							
	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1	X					X			X								X	X							X					X			X					X		
2																																								
3																																								
4										X																														
5		X								X							X	X								X								X					X	
6																																								
7																																								
8																																							X	
9		X								X				X			X	X							X					X			X					X		
10																																								
11																																								
12																																								
13	X					X			X								X	X								X								X					X	
14																																								
15		X															X	X				X																		
16										X																													X	
17		X								X							X	X							X					X			X					X		
18																																								
19																																								
20										X																														
21		X								X				X			X	X								X								X						
22																																								
23																																								
24										X					X																								X	
25	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	X	X							X					X			X						X	
26	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨																								
27	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨																								
28	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨																							X	
29	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	X	X								X								X					X	
30	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨		X								X														
31	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	X	X				X				X														
32	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨		X								X													X	

COUNT FOR 32	RHYTHM 6								RHYTHM 7								RHYTHM 8								RHYTHM 9								RHYTHM 10							
	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1	X							X	X						X		X							X	X	X					X		X	X		X				X
2																																								
3															X		X							X		X									X					X
4																									X	X					X									
5		X				X									X			X					X	X										X		X				X
6																										X														
7										X					X									X	X	X					X		X		X					X
8																		X																						
9	X							X							X		X							X		X								X		X				X
10																		X							X	X					X									
11									X						X		X							X										X	X					X
12																										X														
13		X					X		X						X			X					X	X	X	X					X		X			X	X			X
14																																								
15		X					X								X		X							X		X								X	X		X			X
16															X										X	X					X									
17	X							X							X		X							X									X			X				X
18																										X														
19										X					X		X							X	X	X					X			X	X					X
20																																								
21		X				X									X			X					X	X		X										X				X
22																									X	X					X									
23									X						X									X									X	X	X					X
24																		X								X														
25	X							X	▨	▨	▨	▨	▨	▨	▨	▨	X							X	▨	▨	▨	▨	▨	▨	▨	▨		X		X				X
26									▨	▨	▨	▨	▨	▨	▨	▨		X							▨	▨	▨	▨	▨	▨	▨	▨								
27							X		▨	▨	▨	▨	▨	▨	▨	▨	X							X	▨	▨	▨	▨	▨	▨	▨	▨			X					X
28									▨	▨	▨	▨	▨	▨	▨	▨									▨	▨	▨	▨	▨	▨	▨	▨								
29		X							▨	▨	▨	▨	▨	▨	▨	▨		X					X	X	▨	▨	▨	▨	▨	▨	▨	▨	X	X		X	X			X
30									▨	▨	▨	▨	▨	▨	▨	▨									▨	▨	▨	▨	▨	▨	▨	▨								
31							X		▨	▨	▨	▨	▨	▨	▨	▨	X							X	▨	▨	▨	▨	▨	▨	▨	▨			X		X			X
32									▨	▨	▨	▨	▨	▨	▨	▨		X							▨	▨	▨	▨	▨	▨	▨	▨								

COUNT FOR 32	RHYTHM 11								RHYTHM 12								RHYTHM 13								RHYTHM 14								RHYTHM 15							
	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1	X							X	X	X	X					X	X	X		X				X	X	X		X				X	X	X						X
2																																								
3		X	X	X			X	X								X								X								X								X
4							X																																	
5							X	X		X	X					X								X		X		X			X	X							X	X
6																																								
7		X	X			X		X	X							X		X		X				X								X	X	X					X	X
8																																								
9	X							X	X	X	X					X		X		X				X	X	X		X				X	X							X
10																																								
11		X	X					X								X								X								X								X
12																																								
13	X							X	X	X	X	X				X	X		X					X			X				X	X		X					X	X
14																																								
15		X	X					X		X	X	X				X			X					X		X	X					X	X						X	X
16																																								
17	X							X	X	X	X					X	X	X		X				X	X			X				X	X							X
18																																								
19		X	X	X			X	X								X								X		X		X				X								X
20							X																																	
21							X	X		X	X					X								X							X	X		X					X	X
22																																								
23		X	X			X		X	X							X		X		X	X			X		X		X				X	X						X	X
24																																								
25	X							X	X	X	X					X		X		X	X			X	X	X		X				X	X							X
26																																								
27		X	X					X								X								X								X		X						X
28																																								
29	X							X	X	X	X	X				X	X		X					X			X				X	X							X	X
30																																								
31		X	X					X		X	X	X				X			X					X								X	X						X	X
32																																								

TABLE 2(M252 AD)

COUNT FOR 32	RHYTHM 1 (WALTZ)								RHYTHM 2 (TANGO)								RHYTHM 3 (MARCH)								RHYTHM 4 (SWING)								RHYTHM 5 (MAMBO)							
	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1	X						X		X					X			X						X		X	X	X		X				X				X		X	X
2																																								
3																																	X			X				
4																																				X				
5		X																X							X	X	X		X				X			X	X			
6																																				X				
7																																				X			X	
8																													X					X		X				
9		X							X					X			X	X					X		X				X					X			X			X
10																																								
11																																	X	X			X			
12																																								
13	X						X											X							X	X	X		X				X	X					X	
14																																								
15																																		X			X			
16		X																											X											
17		X							X					X			X						X		X				X				X							X
18																																								
19																																	X			X	X			
20																																								
21		X																X							X	X	X		X				X			X			X	
22																																								
23																																		X		X	X			
24																													X											
25									X					X			X						X		X				X								X		X	X
26																																								
27																																	X	X			X			
28																																		X						
29												X	X	X				X			X				X				X				X				X			
30												X	X																											
31												X	X					X			X										X			X						
32												X	X												X	X	X		X											

COUNT FOR 32	RHYTHM 6 (SLOW ROCK)								RHYTHM 7 (BEAT)								RHYTHM 8 (SAMBA)								RHYTHM 9 (BOSSA NOVA)								RHYTHM 10 (CHA-CHA)							
	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1	X				X	X			X				X				X			X	X		X		X	X	X	X	X		X	X	X	X		X	X		X	X
2																																								
3					X								X	X							X			X	X				X					X		X	X			
4																																								
5					X					X			X					X			X			X					X	X			X				X		X	X
6																																								
7		X			X	X			X				X				X	X		X	X		X			X	X	X	X	X		X					X			
8																																								
9					X				X				X				X				X				X			X	X	X			X			X	X		X	X
10																																								
11	X				X								X	X							X			X	X				X		X						X			
12																																								
13	X				X	X				X			X					X		X	X		X	X		X	X	X	X			X	X			X	X		X	X
14																																								
15					X								X				X	X			X								X		X					X	X			
16																																								
17					X				X				X				X				X				X				X				X	X		X	X		X	X
18																																								
19		X			X	X							X	X							X				X				X	X						X	X			
20																																								
21					X					X			X					X		X	X		X	X		X	X	X	X			X	X				X		X	X
22																																								
23		X			X				X				X				X				X								X	X							X			
24																																								
25									X				X				X	X			X				X				X				X			X	X		X	
26																																								
27													X	X				X		X	X		X	X	X	X	X	X	X		X	X	X			X	X		X	
28																																								
29										X			X					X			X								X		X		X			X	X		X	
30																																								
31										X			X				X	X		X	X								X		X					X	X			
32																																		X		X				

COUNT FOR 32	RHYTHM 11 (RUMBA)								RHYTHM 12 (BEGUINE)								RHYTHM 13 (BAJON)								RHYTHM 14 (FOX TROT)								RHYTHM 15 (SHUFFLE)							
	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1	X	X					X	X	X				X			X	X			X	X		X		X				X				X	X				X		
2																																								
3					X					X	X	X	X		X						X													X						
4													X																				X	X				X		
5					X								X								X					X					X									
6																																						X		
7	X				X		X					X	X			X				X	X		X										X	X				X		
8																																								
9					X			X				X	X							X	X		X		X				X					X						
10												X																					X	X				X		
11					X						X	X	X								X																			
12												X																												
13	X						X		X				X			X	X		X		X					X				X			X	X				X		
14																																								
15					X						X		X						X		X					X				X				X						
16																																	X	X				X		
17	X						X	X	X				X				X			X	X		X		X				X											
18																																						X		
19					X					X	X	X	X		X						X												X	X				X		
20													X																											
21		X			X								X			X					X					X					X		X	X						
22																																		X				X		
23	X											X	X					X		X	X		X											X						
24																																		X						
25		X			X		X		X				X			X		X		X	X		X		X				X											
26																																								
27					X						X		X								X									X										
28																																								
29	X			X				X	X				X				X		X		X					X														
30																																								
31				X	X						X		X						X		X									X										
32																																								

RHYTHM GENERATOR

LOW POWER DISSIPATION: < 120 mW
DRIVES 8 SOUND GENERATORS (INSTRUMENTS)
12 PROGRAMMABLE RHYTHMS (ALSO AVAILABLE IN COMBINATION)
MASK PROGRAMMABLE RESET COUNTS: 24 or 32
DOWN BEAT OUTPUT
EXTERNAL RESET
OPEN DRAIN OUTPUT
STANDARD MUSIC CONTENT AVAILABLE
TECHNICAL NOTE NO 131 AVAILABLE FOR FULL INFORMATION

The M253 is a monolithic rhythm generator specifically designed for electronic organs and other musical instruments.
Constructed on a single chip using low threshold P-channel silicon gate technology it is supplied in a 24-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{GG} **	Source supply voltage	-20 to 0.3	V
V_I **	Input voltage	-20 to 0.3	V
I_O	Output current (at any pin)	3	mA
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

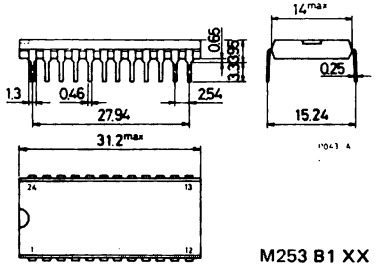
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions foe extended periods may affect device reliability.

** This voltage is with respect to V_{SS} pin voltage.

ORDERING NUMBERS: M253 B1 XX for dual in-line plastic package
M253 B1 AA and AC for standard music content

MECHANICAL DATA

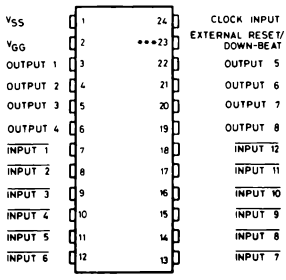
Dimensions in mm

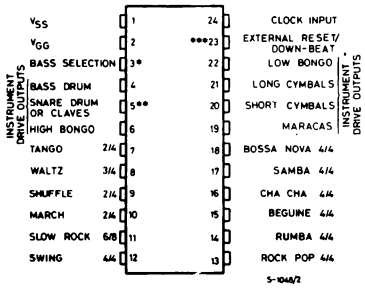


M253 B1 XX

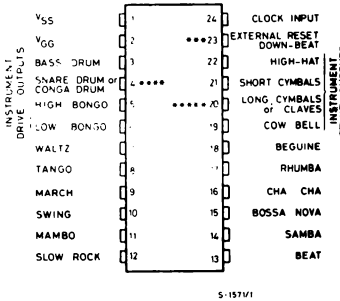
CONNECTOR DIAGRAMS

Standard content configuration
M253 B1 AA





Standard content configuration
M253 B1 AC



* This output allows the musician to obtain a "basso alternato" accompaniment using two notes of his choice.

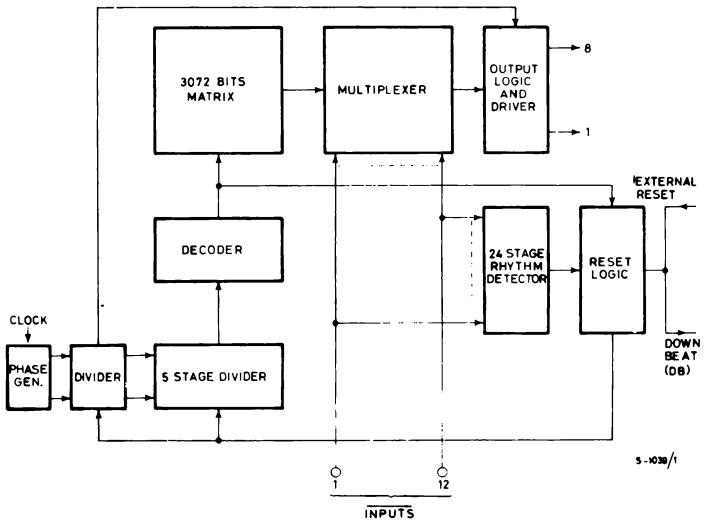
** This output must be connected so as to drive the "snare drum" when the rhythms corresponding to pins 7, 8, 9, 10, 11, 12 and 13 are generated, and the "claves" when the rhythms corresponding to pins 14, 15, 16, 17 and 18 are generated. It can also be used to modulate a chord played on the organ.

*** This pin generates a down-beat trigger which can be used to drive an external lamp to indicate the first beat of the first bar of each rhythm.

**** This output must be connected so as to drive the "snare drum" when the rhythms corresponding to pins 7, 9, 10, 12, 13, 15 and 18 are generated, and the "conga drum" when the rhythms corresponding to pins 11, 14, 16 and 17 are generated.

***** This output must be connected so as to drive the "long cymbals" when the rhythms corresponding to pins 7, 9, 10 and 18 are generated, and the "claver" when the rhythms corresponding to pins 11, 14, 15, 16 and 17 are generated.

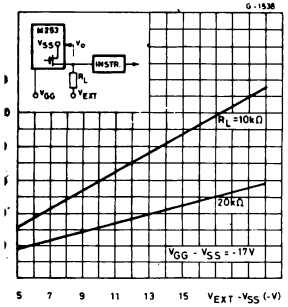
BLOCK DIAGRAM



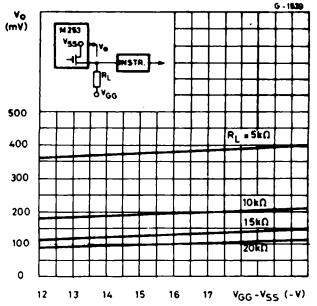
STATIC ELECTRICAL CHARACTERISTICS (positive logic, V_{GG} = -11.4 to -12.6V, V_{SS} = 4.75 to 5.25V, T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
CLOCK INPUT						
V_{IH}	Clock high voltage		V_{SS}-1.5		V_{SS}	V
V_{IL}	Clock low voltage		V_{GG}		V_{SS}-4.1	V
DATA INPUTS ($\overline{IN1}$ ..... $\overline{IN12}$)						
V_{IH}	Input high voltage		V_{SS}-1,5		V_{SS}	V
V_{IL}	Input low voltage		V_{GG}		V_{SS}-4.1	V
I_{LI}	Input leakage current	$V_i = V_{SS}$-10V T_{amb}= 25°C			10	µA
EXTERNAL RESET						
V_{IH}	Input high voltage		V_{SS}-1.5		V_{SS}	V
V_{IL}	Input low voltage		V_{GG}		V_{SS}-4.1	V
R_{IN}	Internal resistance to V_{GG}	$V_o = V_{SS}$-5V	400	600		kΩ
DATA OUTPUTS						
R_{ON}	Output resistance (ON state)	$V_o = V_{SS}$-1 to V_{SS}		250	500	Ω
V_{OH}	Output high voltage	I_L = 1 mA	V_{SS}-0.5		V_{SS}	V
I_{LO}	Output leakage current	$V_i = V_{IH}$ $V_o = V_{SS}$-10V T_{amb}= 25°C			10	µA
POWER DISSIPATION						
I_{GG}	Supply current	T_{amb}= 25°C		7	15	mA

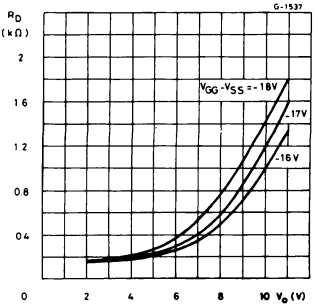
Output voltage vs. external supply voltage (V_{EXT}-V_{SS})



Output voltage vs. supply voltage (V_{GG}-V_{SS})



Output dynamic resistance vs. output voltage

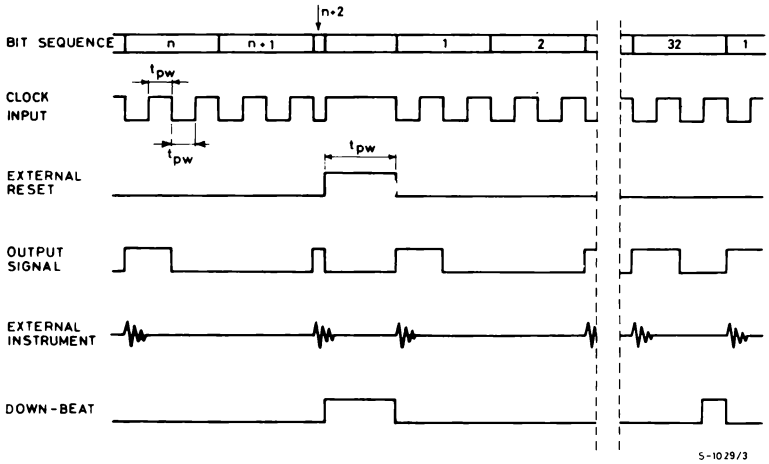


DYNAMIC ELECTRICAL CHARACTERISTICS (positive logic, V_{GG} = -11.4 to -12.6V, V_{SS} = 4.75 to 5.25V, T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
CLOCK INPUT						
f	Clock repetition rate		DC		100	kHz
t_{pw}*	Pulse width		5			µs
t_r**	Rise time				100	µs
t_f**	Fall time				100	µs
EXTERNAL RESET						
t_{pw}	Pulse width		5			µs

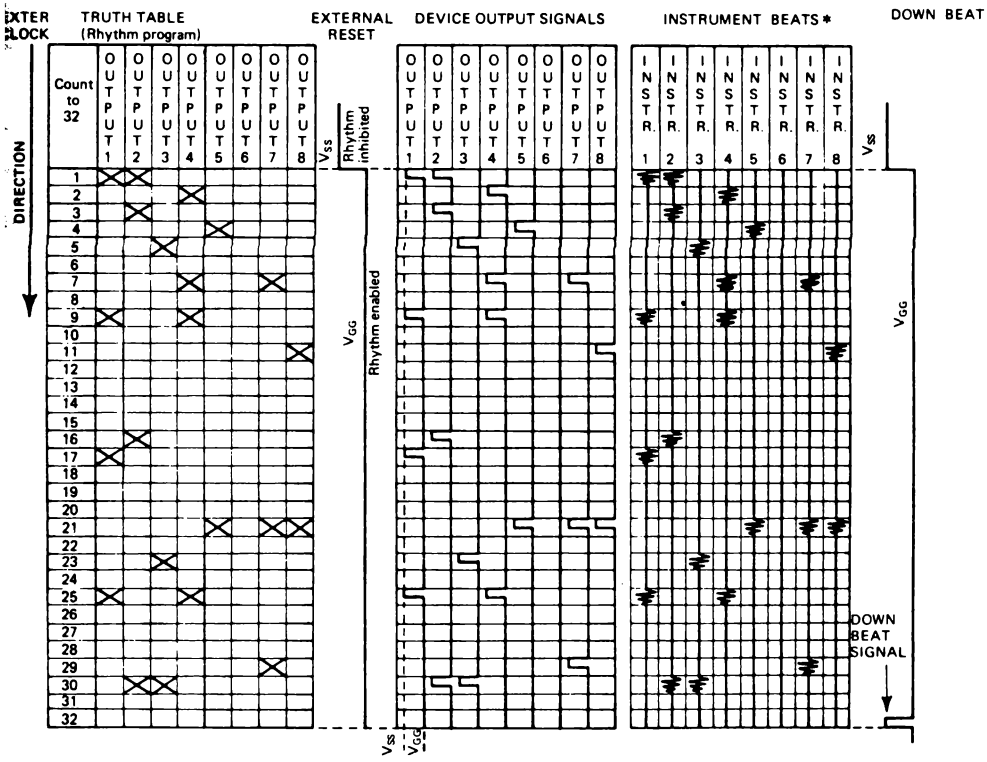
* Measured at 50% of the swing.
** Measured between 10% and 90% of the swing

TIMING WAVEFORMS (positive logic)



Note: In these timing waveforms it has been assumed, for example, that in the truth table bits n + 1 and 2 have not been programmed i.e. the musical instrument has not been introduced.
All the other bits have been programmed for the introduction of the instrument.

INSTRUMENT BEATS VERSUS RHYTHM PROGRAM



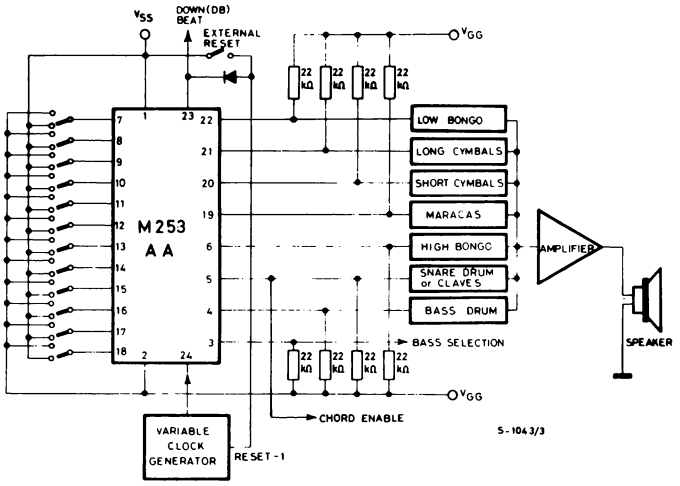
The lowering of the music signals depends on the intrinsic decay time of the sound generator and not on the length of the enable pulses. Each beat can therefore last for more than one elementary time.

TYPICAL APPLICATIONS

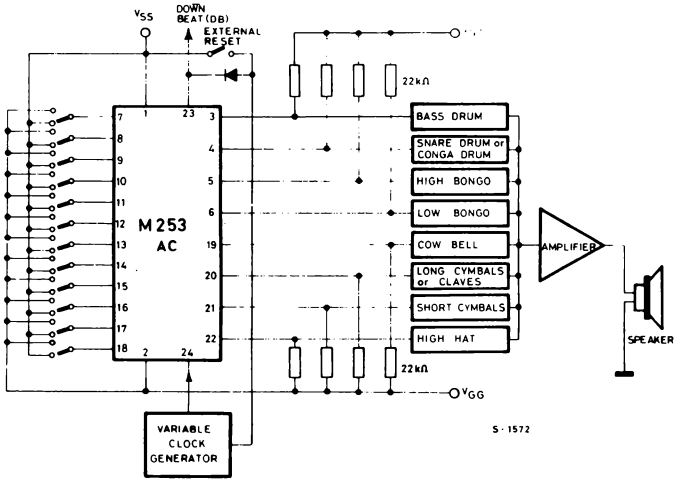
Figure 1 shows the typical application of the M253 (AA) and M253 (AC).
With two M253 devices it is possible to increase the number of rhythms or the number of instruments available, or the number of elementary times, as shown in figures 2, 3 and 4 respectively.
The use of a memory matrix allows the customer complete flexibility, since modification of the memory is quick and relatively cheap.

Fig. 1 - Rhythm ststem (standard contents)

a) M253 AA



b) M253 AC



TYPICAL APPLICATIONS (continued)

Fig. 2 - Increase in number of rhythms

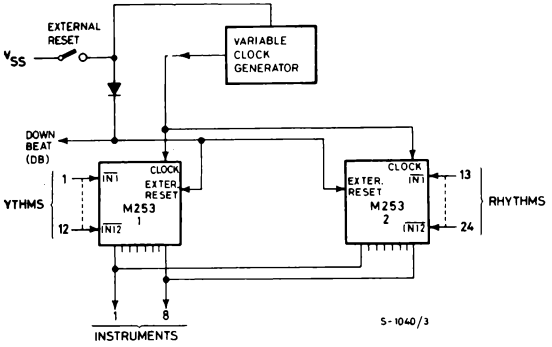
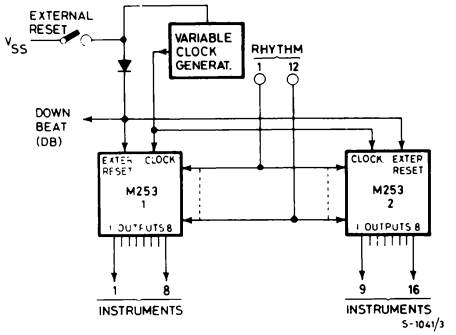
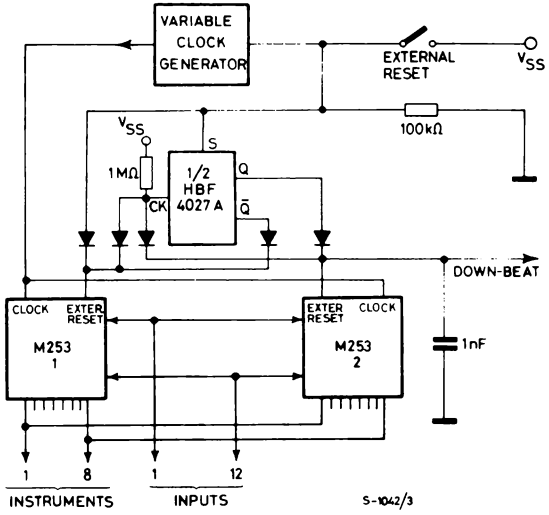


Fig. 3 - Increase in number of instruments



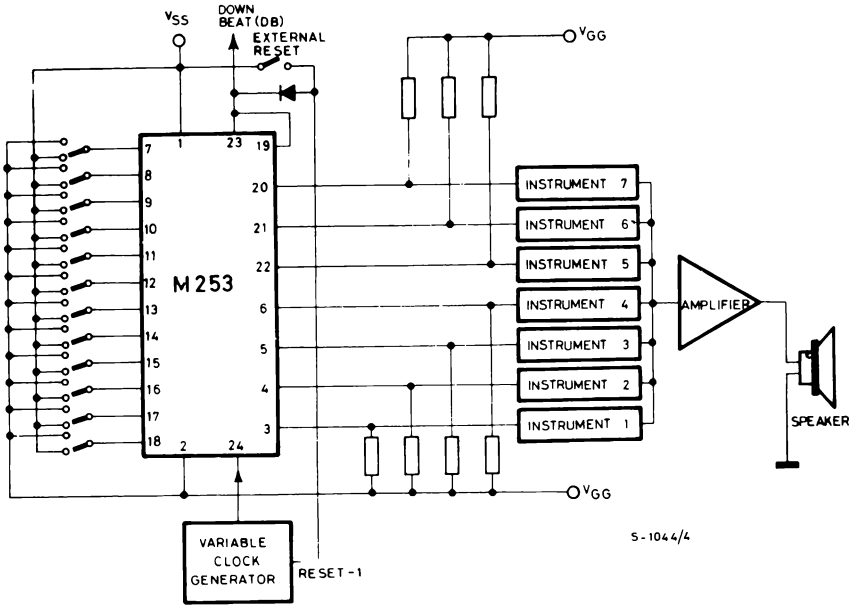
The rhythms may be selected from both devices simultaneously.

Fig. 4 - Increasing the number of elementary times



Note: The total number of elementary times is given by the sum of the elementary times of the individual devices.

CIRCUIT FOR CHANGING THE NUMBER OF ELEMENTARY TIMES



To obtain a required number of elementary times "N" simply put a cross in the "N + 1" position of the column which now represents the reset output, rather than the 8th instrument.
The DB output can be used as down-beat because it appears at the beginning of each measure. Since the pulse is only 2-3 μs long it must, however, be stretched and buffered to enable it to drive a lamp.
Full information on the use of the M253 in electronic organs and other applications will be found in Technical Note no. 131 available on request.

COMPLETING THE TRUTH TABLE

The ROM truth table has been organized in 32 rows which represent elementary times and 96 columns (12 groups of 8) where each group represents a rhythm which has at its disposition 8 programmable instruments. To programme each rhythm one indicates (with a cross) in the appropriate boxes the timing for each beat required for each instrument.
Each cross corresponds to a beat of the indicated instrument or, in logic terms, to the presence of a **"1"** level (positive logic) at the output.
The absence of a cross indicates that the corresponding instrument is not used in that part of the rhythm.
Table 1 and 2 show the standard music content programmed into M253 AA and M253 AC respectively.

TABLE 1 (M253 AA)

COUNT FOR 32	RHYTHM 1								RHYTHM 2								RHYTHM 3								RHYTHM 4								RHYTHM 5							
	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1		X	X				X			X				X				X	X				X			X				X				X					X	
2																																								
3																			X																				X	
4																	X	X	X				X																	
5		X	X								X																X												X	
6																			X																					
7							X											X	X				X												X				X	
8																																								
9		X	X				X				X								X						X	X				X									X	
10																	X	X	X				X																	
11																																		X					X	
12																			X																					
13		X	X				X		X	X				X				X	X				X				X						X	X					X	
14																																								
15	X	X	X			X													X																				X	
16																	X	X	X				X																X	
17		X	X				X				X															X				X									X	
18																			X																					
19																		X	X				X												X				X	
20																																								
21		X	X								X								X								X												X	
22																	X	X	X				X																	
23							X																										X	X					X	
24																			X																					
25		X	X				X																		X	X				X										
26																																								
27																																								
28																																								
29		X	X				X																				X													
30																											X													
31	X	X	X			X																					X													
32																											X													

COUNT FOR 32	RHYTHM 6								RHYTHM 7								RHYTHM 8								RHYTHM 9								RHYTHM 10							
	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1		X				X				X						X		X	X		X			X		X						X		X	X	X				X
2																																								
3										X						X					X			X			X	X	X		X	X								X
4																								X							X									
5			X				X				X				X	X				X				X							X	X			X	X				X
6																																								
7																X		X	X		X			X			X	X		X		X	X	X						X
8							X				X																													
9	X	X				X			X	X						X	X	X			X			X	X	X						X			X	X				X
10											X																													
11									X	X						X				X				X			X	X				X			X					X
12																																								
13			X				X				X				X	X	X	X	X		X			X	X	X						X	X	X	X	X	X			X
14																																								
15									X	X						X				X				X			X	X				X					X			X
16							X																																	
17		X				X				X						X		X			X			X		X						X		X	X	X				X
18																																								
19										X						X					X			X			X	X	X		X	X								X
20																								X							X									
21			X								X				X	X			X	X				X							X	X			X	X				X
22																																								
23																X		X			X			X			X	X		X		X	X	X						X
24							X				X																													
25	X	X					X		X	X						X	X	X	X		X			X	X	X						X			X	X				X
26											X																													
27									X	X						X				X				X			X	X				X			X					X
28							X																																	
29			X				X				X				X	X	X	X			X			X	X	X						X	X	X	X	X	X			X
30																																								
31										X						X				X				X			X	X				X					X			X
32							X				X																													

	RHYTHM 11								RHYTHM 12							
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1		X		X				X		X	X					X
2																
3			X					X								X
4																
5				X			X	X							X	X
6																
7			X					X		X	X				X	X
8																
9	X	X			X			X	X	X						X
10																
11			X					X								X
12			X													
13							X	X			X				X	X
14																
15			X		X			X	X	X					X	X
16																
17		X		X				X		X						X
18																
19			X	X				X								X
20																
21							X	X			X				X	X
22																
23			X	X				X		X					X	X
24																
25	X	X			X			X	X	X						X
26																
27			X					X			X					X
28			X													
29					X		X	X							X	X
30																
31			X					X	X	X					X	X
32																

TABLE 2 (M253 AC)

	RHYTHM 1 (WALTZ)								RHYTHM 2 (TANGO)								RHYTHM 3 (MARCH)								RHYTHM 4 (SWING)								RHYTHM 5 (MAMBO)							
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1	X						X		X					X			X						X		X	X	X		X				X				X		X	X
2																																								
3																																	X			X				
4																																				X				
5		X																X							X	X	X		X				X			X	X			
6																																				X				
7																																				X			X	
8																													X					X		X				
9		X							X					X			X	X					X		X				X					X			X			X
10																																								
11																																	X	X			X			
12																																								
13	X						X											X							X	X	X		X				X	X					X	
14																																								
15																																		X			X			
16		X																											X											
17		X							X					X			X						X		X				X				X							X
18																																								
19																																	X			X	X			
20																																								
21		X																X							X	X	X		X				X			X			X	
22																																								
23																																		X		X	X			
24																													X											
25									X					X			X						X		X				X								X		X	X
26																																								
27																																	X	X			X			
28																																		X						
29												X	X	X				X			X				X				X				X				X			
30												X	X																											
31												X	X					X			X										X			X						
32												X	X												X	X	X		X											

	RHYTHM 6 (SLOW ROCK)								RHYTHM 7 (BEAT)								RHYTHM 8 (SAMBA)								RHYTHM 9 (BOSSA NOVA)								RHYTHM 10 (CHA-CHA)							
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1	X				X	X			X				X				X			X	X		X		X	X	X	X	X		X	X	X	X		X	X		X	X
2																																								
3					X								X	X							X			X	X				X					X		X	X			
4																																								
5					X					X			X					X			X			X					X	X			X				X		X	X
6																																								
7		X			X	X			X				X				X	X		X	X		X			X	X	X	X	X		X					X			
8																																								
9					X				X				X				X				X				X			X	X	X			X			X	X		X	X
10																																								
11	X				X								X	X							X			X	X				X		X						X			
12																																								
13	X				X	X				X			X					X		X	X		X	X		X	X	X	X			X	X			X	X		X	X
14																																								
15					X								X				X	X			X								X		X					X	X			
16																																								
17					X				X				X				X				X				X				X				X	X		X	X		X	X
18																																								
19		X			X	X							X	X							X				X				X	X						X	X			
20																																								
21					X					X			X					X		X	X		X	X		X	X	X	X			X	X				X		X	X
22																																								
23		X			X				X				X				X				X								X	X							X			
24																																								
25									X				X				X	X			X				X				X				X			X	X		X	
26																																								
27													X	X				X		X	X		X	X	X	X	X	X	X		X	X	X			X	X		X	
28																																								
29										X			X					X			X								X		X		X			X	X		X	
30																																								
31										X			X				X	X		X	X								X		X					X	X			
32																																		X		X				

	RHYTHM 11 (RUMBA)								RHYTHM 12 (BEGUINE)							
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8
1	X	X					X	X	X				X			X
2																
3					X					X	X	X	X		X	
4													X			
5					X								X			
6																
7	X				X		X					X	X			X
8																
9					X			X				X	X			
10												X				
11					X						X	X	X			
12												X				
13	X						X		X				X			X
14																
15					X						X		X			
16																
17	X						X	X	X				X			
18																
19					X					X	X	X	X		X	
20													X			
21		X			X								X			X
22																
23	X											X	X			
24																
25		X			X		X		X				X			X
26																
27					X						X		X			
28																
29	X			X				X	X				X			
30																
31				X	X						X		X			
32																

MOS INTEGRATED CIRCUIT

M 254

RHYTHM GENERATOR

- DRIVES 12 SOUND GENERATORS (INSTRUMENTS) OR SOME INSTRUMENTS AND M 251 OR M 108
- 5 BIT COUNTER
- 8 RHYTHMS PER INSTRUMENT
- EXTERNAL RESET

The M 254 is a monolithic rhythm generator specifically designed for electronic organs and other musical instruments. Constructed on a single chip using P-channel silicon gate technology, it is supplied in a 24-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{GG} **	Source supply voltage	-20 to 0.3	V
V_I **	Input voltage	-20 to 0.3	V
I_O	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

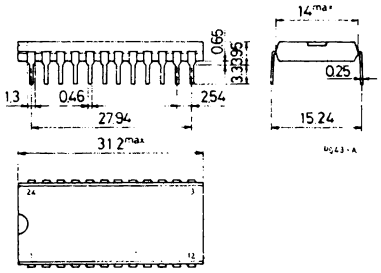
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages value are referred to V_{SS} pin voltage.

ORDERING NUMBERS: M 254 XX for dual in-line plastic package
M 254 B1AD for standard music content
M 254 B1AM for standard music content

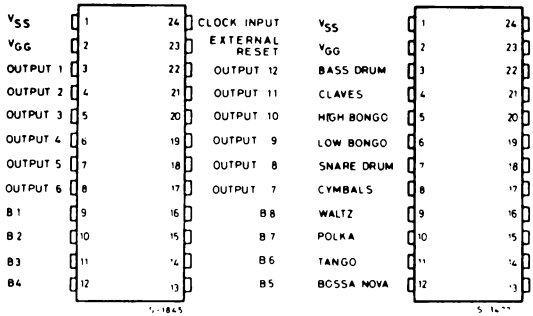
MECHANICAL DATA

Dimensions in mm

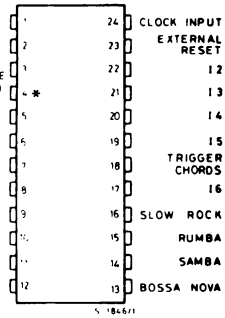


CONNECTION DIAGRAMS

M 254 B1AM Standard content configuration



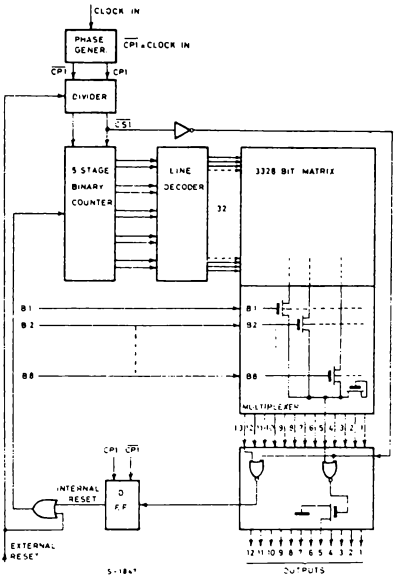
M 254 B1AD Standard content configuration



* This output must be connected so as to drive the "snare drum" when the rhythms corresponding to pins 9, 10, 11, 12 and 16 are generated, and the "claves" when the rhythms corresponding to pins 13, 14 and 15 are generated. I2 to I8 drive the corresponding inputs of the M 251.

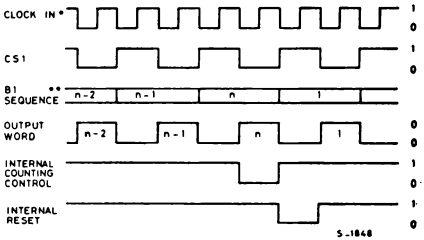
** These outputs must be connected so as to drive the bass switching inputs A, B, C of the M 108.

BLOCK DIAGRAM

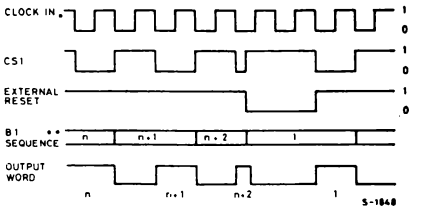


TIMING WAVEFORMS (positive logic)

Output words versus external reset



Output words versus internal reset



* External gating allows resetting of the variable clock generator to ensure that the beat starts exactly at the right moment.

** i= 1.....8; in this timing waveform it has been assumed that in the truth table all bits have been programmed.

DEVICE DESCRIPTION

The M 254 contains a ROM which can drive 12 sound generators (instruments) with a selection of 8 rhythms for each generator. An external clock drives a phase generator which produces complementary outputs, these signals are then divided-by-2, to produce the signals to enable the output buffers and drive a 5-stage binary counter.
The outputs of the counter are decoded, being the 32 rows of the memory matrix which has 104 columns. The 104 columns are divided into 13 groups of 8. A multiplexer is used such that any number of columns in the 13 groups can be selected from 1 to 8. Of the 13 groups in the memory matrix, 12 have buffered outputs via an enabling circuit (the enabling conditions being CS1 = "0" and at least one multiplex input at logic "1").
The 13th group in the matrix controls the internal reset which is synchronised with the counter and controls the counting sequence.

STATIC ELECTRICAL CHARACTERISTICS (positive logic, V_{GG} = GND; V_{SS} = 14 to 18V; T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK INPUT						
V_{IH}	Clock high voltage		V_{SS}-1			V
V_{IL}	Clock low voltage				V_{SS}-10	V
DATA INPUTS (B1 . . . . . B8)						
V_{IH}	Input high voltage		V_{SS}-1			V
V_{IL}	Input low voltage				V_{SS}-10	V
I_{LI}	Input leakage current	V_i=V_{SS}-14V T_{amb}= 25°C			10	µA
DATA OUTPUTS						
R_{ON}	Output resistance (ON state)	V_o=V_{SS}-2V		1	2	kΩ
I_{OH}	Output high current	V_{SS}= 18V			100	µA
POWER DISSIPATION						
I_{GG}	Supply current	V_{GG}=V_{SS}-18V T_{amb}= 25°C		10		mA

DYNAMIC ELECTRICAL CHARACTERISTICS (positive logic, V_{GG} = GND; V_{SS} = 14 to 18V; T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK INPUT						
f	Clock repetition rate		DC		100	kHz
t_{pw}*	Pulse width	Duty cycle = 50%	5			µs
t_d	Pulse delay		5			µs
t_r**	Rise time	T_{amb} = 25°C			5	µs
t_f**	Fall time				5	µs

* Measured at 50% of the swing
** Measured between 10% and 90% of the swing

TYPICAL APPLICATIONS

Figure 1 shows the typical application of the M 254 AD.
Figure 2 shows the typical application of the M 254 AM.
With two M 254 devices it is possible to increase the number of rhythms or the number of instruments available, as shown in figures 3 and 4 respectively.

Fig. 1 - Rhythm and accompaniment system (standard contents). M 254 AD

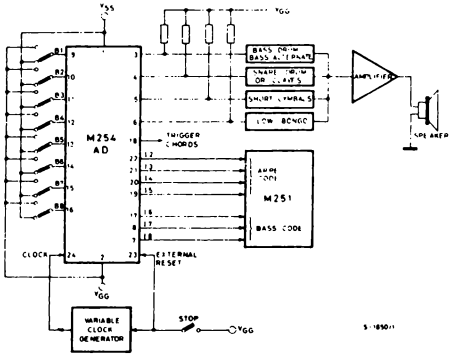
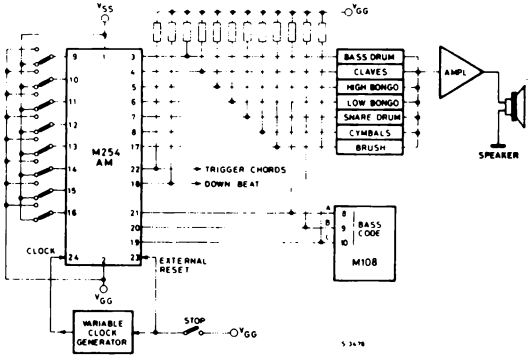


Fig. 2 - Rhythm and accompaniment system (standard contents). M 254 AM



TYPICAL APPLICATIONS (continued)

Fig. 3 - Increase in number of rhythms

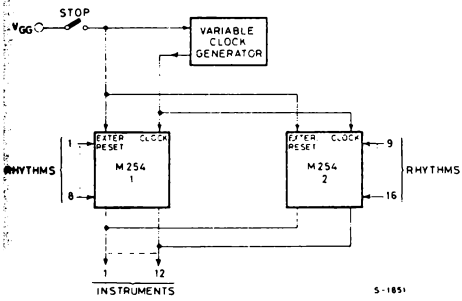
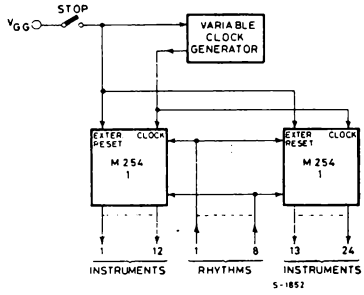


Fig. 4 - Increase in number of instruments



COMPLETING THE TRUTH TABLE

The ROM truth table has been organized in 32 rows which represent the elementary times and 104 columns.

The first 8 groups of 12 columns represent the rhythms which have 12 programmable outputs. The timing for the beats required for each instrument is programmed by crossing the appropriate box.

The 9th group of 8 columns represents the COUNTING control information which specifies the number of elementary times in a given rhythm.

If count N is crossed for rhythm X this rhythm will have N elementary times. If the counting control column for a particular rhythm does not contain a cross that rhythm will have 32 elementary times.

Table 1 and 2 show the truth tables of the M 254 AD and M 254 AM, standard contents, respectively.

It can be seen that in the table 1 the rhythms 1 and 8 and in the table 2 the rhythms 1,6 and 7, have 24 elementary times.

M 254

M 254 AD (standard)

	RHYTHM 1 (WALTZ)												RHYTHM 2 (TANGO)												RHYTHM 3 (SWING)											
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12
1	X		X				X		X	X	X		X	X					X	X	X	X	X		X		X				X		X	X	X	
2																																				
3									X	X		X									X		X	X									X		X	X
4																																				
5		X				X		X	X		X	X									X	X		X		X	X			X		X	X	X		X
6																																				
7									X		X										X	X	X										X	X	X	
8																											X									
9		X				X	X	X	X			X	X	X				X		X	X		X	X	X		X			X	X		X		X	X
10																																				
11										X	X	X																					X	X	X	
12																																				
13	X		X		X	X				X	X										X		X	X		X	X		X			X	X	X		X
14																																				
15										X	X	X									X	X		X									X		X	X
16		X																									X									
17		X				X	X	X	X			X	X	X				X	X	X	X		X		X		X		X	X			X		X	
18																																				
19									X		X																							X	X	X
20																																				
21		X				X		X	X		X	X									X		X			X	X		X			X	X			X
22																																				
23									X	X		X									X		X	X									X		X	
24																											X									
25													X	X				X		X		X	X	X	X		X			X	X			X	X	X
26																																				
27																					X			X									X		X	
28																										X	X									
29														X	X			X	X	X	X		X			X	X			X		X	X			X
30														X																						
31														X							X		X	X										X	X	X
32														X												X	X									

	RHYTHM 4 (BEAT)												RHYTHM 5 (BOSSA NOVA)												RHYTHM 6 (SAMBA)											
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12
1	X		X		X	X		X	X	X	X	X	X	X	X		X	X		X	X	X	X		X		X	X			X	X	X	X	X	
2																																				
3			X						X	X	X				X				X							X	X						X	X		X
4																																				
5		X	X		X	X		X	X	X		X			X	X				X	X		X	X	X		X	X				X	X		X	X
6																																				
7	X		X						X		X	X	X	X	X			X			X	X		X		X	X			X			X	X		X
8					X	X																														
9	X		X				X		X		X		X		X					X	X		X		X		X	X		X	X	X	X		X	X
10																																				
11			X				X	X	X			X			X			X	X	X	X		X	X		X	X						X		X	
12																										X										
13		X	X			X				X	X	X		X	X	X	X	X			X			X			X			X		X	X		X	X
14																																				
15			X			X	X		X			X	X		X			X	X	X		X	X	X	X	X	X	X					X		X	
16																																	X			X
17	X		X		X	X		X	X		X		X		X		X	X							X		X	X	X	X		X		X	X	X
18																																				
19	X		X						X			X			X			X	X	X	X			X	X	X	X	X				X	X			X
20																																				
21		X	X		X	X			X		X			X	X	X											X			X	X		X		X	
22																																				
23	X		X					X	X		X	X			X			X		X	X			X	X	X	X	X	X	X		X	X			X
24					X	X			X	X		X																								
25	X		X				X		X		X	X	X		X										X		X	X				X				
26																																				
27		X	X				X		X	X		X		X	X			X	X	X	X		X			X	X			X			X		X	
28																										X										
29			X			X			X	X	X		X		X	X		X		X	X		X	X			X	X				X	X		X	X
30																																				
31	X	X	X			X	X		X	X		X	X		X				X		X	X		X		X	X			X	X	X	X	X		X
32																																				

	RHYTHM 7 (RUMBA)												RHYTHM 8 (SLOW ROCK)												COUNTING CONTROL											
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	RHYTHM 1	RHYTHM 2	RHYTHM 3	RHYTHM 4	RHYTHM 5	RHYTHM 6	RHYTHM 7	RHYTHM 8	RHYTHM 9	RHYTHM 10	RHYTHM 11	RHYTHM 12
1	X	X	X				X		X	X	X	X	X		X				X		X	X	X	X												
2																																				
3			X												X						X	X	X													
4									X		X	X																								
5			X	X				X	X	X		X			X						X	X		X												
6																																				
7	X	X	X			X			X		X			X				X		X	X		X	X												
8																																				
9			X	X				X							X						X		X													
10																																				
11			X	X				X	X		X	X	X		X			X	X		X			X												
12																																				
13	X	X	X			X	X		X			X	X		X		X	X				X	X	X												
14																																				
15			X	X					X		X				X						X			X												
16																																				
17	X		X	X	X	X		X		X	X	X			X						X		X													
18																																				
19			X						X			X		X				X		X	X		X	X												
20																																				
21		X	X						X		X				X						X	X		X												
22																																				
23	X		X	X		X	X	X	X			X	X		X			X	X		X	X	X													
24																									X							X				
25		X	X						X		X																									
26																																				
27			X	X				X	X		X	X																								
28																																				
29	X		X	X	X	X			X	X		X																								
30																																				
31			X	X					X	X	X																									
32																																				

M 254 AM (standard)

	RHYTHM 1 (WALTZ)												RHYTHM 2 (POLKA)												RHYTHM 3 (TANGO)											
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12
1	X					X		X			X		X					X		X			X		X				X		X	X			X	X
2																																				
3					X		X					X					X		X					X												
4																																				
5					X		X					X	X					X		X	X				X				X		X			X		X
6																																				
7	X					X		X	X								X		X					X												
8																																				
9					X		X					X	X					X		X			X		X				X		X		X			X
10																																				
11					X		X					X					X		X					X												
12																																				
13	X					X		X			X		X					X		X	X				X				X		X		X	X	X	X
14																																				
15					X		X					X					X		X					X					X	X	X					X
16																	X												X							
17					X		X					X	X					X		X			X		X				X		X	X			X	X
18																																				
19	X					X		X	X								X		X					X												
20																																				
21					X		X					X	X					X		X	X				X				X		X			X		X
22																																				
23					X		X					X					X		X					X												
24																																				
25													X					X		X			X		X				X		X		X			X
26																																				
27																	X		X					X												
28																	X																			
29													X				X			X	X				X				X		X		X	X	X	X
30																																				
31																	X		X					X					X	X	X					X
32																																				

	RHYTHM 4 (BOSSA NOVA)												RHYTHM 5 (SAMBA)												RHYTHM 6 (SLOW ROCK)											
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12
1	X	X		X			X	X			X	X	X	X		X	X		X	X			X		X					X	X	X			X	X
2																			X																	
3							X											X	X	X					X							X					X
4															X				X																			
5							X						X	X	X		X		X		X											X					X
6																			X																	
7		X	X				X					X						X	X					X					X	X	X					X
8														X		X	X		X																		
9	X		X				X		X					X			X			X				X								X					X
10																	X	X		X																		
11							X												X	X					X	X						X			X		X
12																			X		X																		
13		X					X					X	X		X		X		X		X		X				X					X	X	X	X			X
14																			X																	
15	X			X			X											X	X					X							X					X
16																X			X																			
17	X			X			X	X			X		X	X		X	X		X	X			X							X					X
18																			X																	
19							X										X	X	X					X					X	X	X			X		X
20															X				X																			
21		X					X					X	X	X	X		X		X		X											X					X
22																			X																	
23			X				X												X	X					X	X						X		X			X
24														X		X	X		X																		
25	X						X		X				X			X			X				X														
26																	X	X		X																		
27		X	X				X					X						X	X					X												
28																			X		X																		
29							X						X	X	X		X		X		X																
30																			X																	
31	X			X			X											X	X					X												
32																X			X																			

	RHYTHM 7 (BOOGIE)												RHYTHM 8 (DISCO)												COUNTING CONTROL											
COUNT FOR 32	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7	OUTPUT 8	OUTPUT 9	OUTPUT 10	OUTPUT 11	OUTPUT 12
1	X					X		X			X		X			X			X	X			X													
2																			X																	
3							X					X						X	X					X												
4					X	X				X					X				X																			
5														X				X		X		X																	
6							X					X							X																	
7	X					X			X							X		X	X		X	X	X	X												
8																			X																	
9							X					X	X						X				X														
10					X	X			X		X									X																	
11																			X	X					X												
12							X					X			X				X																			
13	X					X		X	X	X			X		X		X		X		X															
14																			X																	
15							X					X				X		X	X		X	X	X	X												
16					X	X			X		X									X																	
17														X			X			X	X			X													
18							X					X							X																	
19	X					X			X										X	X					X												
20															X				X																			
21					X		X					X	X				X		X		X																	
22					X	X				X									X																	
23																	X		X	X		X	X	X	X												
24							X					X							X						X					X	X					
25														X						X				X														
26																			X																	
27																			X	X					X												
28															X				X																			
29														X		X		X		X		X															
30																			X																	
31																	X		X	X		X	X	X	X												
32																			X																	

MOS INTEGRATED CIRCUIT

M 255

RHYTHM GENERATOR

- INTERNAL TEMPO OSCILLATOR
- 6 PROGRAMMABLE RHYTHMS
- DRIVES 5 SOUND GENERATORS
- MASK PROGRAMMABLE RESET COUNTS: 12 or 16
- DOWN BEAT OUTPUT
- EXTERNAL RESET
- LOW POWER DISSIPATION: < 100 mW
- PIN-TO-PIN COMPATIBLE WITH MM 5871
- PUSH-PULL OR OPEN DRAIN OUTPUTS AVAILABLE
- STANDARD CONTENT AVAILABLE

The M 255 is a monolithic rhythm generator specifically designed for electronic organs and other musical instruments. Constructed on a single chip using P-channel silicon gate technology it is supplied in a 16-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{GG} **	Source supply voltage	-20 to 0.3	V
V_I **	Input voltage	-20 to 0.3	V
I_o	Output current for down beat (pin 3)	20	mA
I_o	Output current (at other pins)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

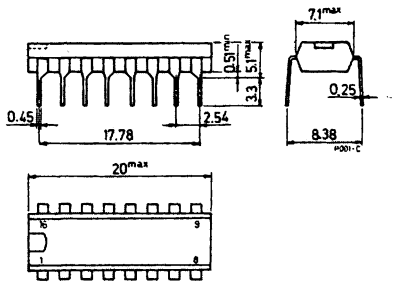
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages value are referred to V_{SS} pin voltage.

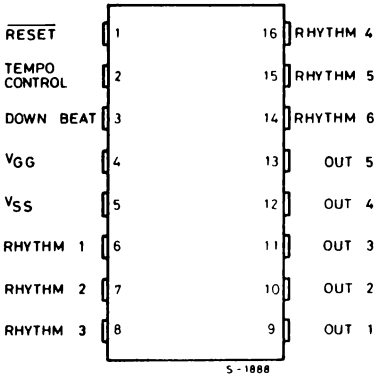
ORDERING NUMBERS: M 255 B1 XX for dual in-line plastic package
M 255 B1 AB for standard music content

MECHANICAL DATA

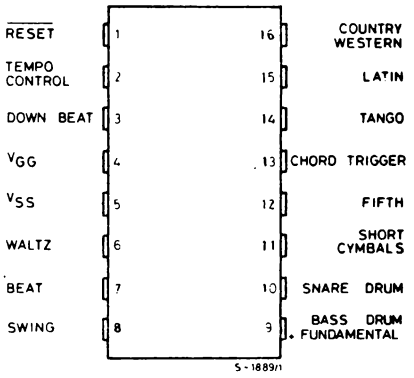
Dimensions in mm



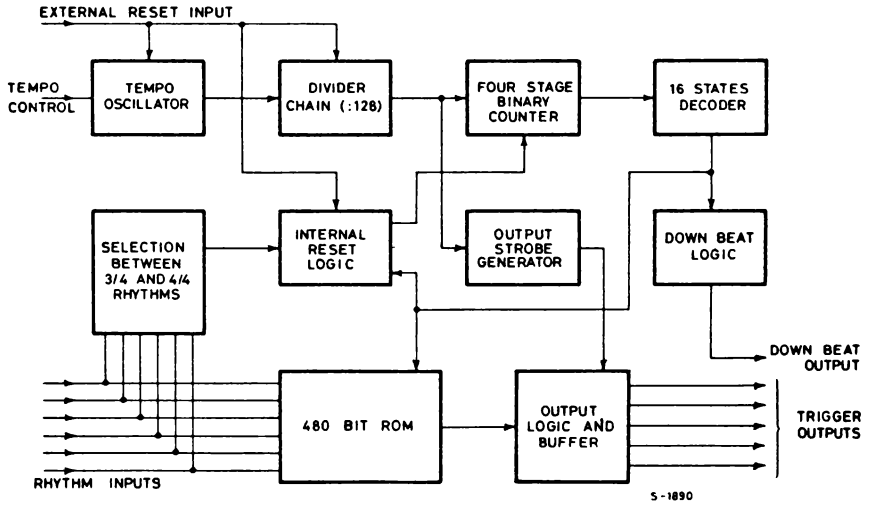
CONNECTION DIAGRAMS



Standard content configuration
M 255 B1 - AB



BLOCK DIAGRAM



GENERAL CHARACTERISTICS

The M 255 circuit comprises:

a) One pin for tempo control. The external network employs a capacitor and two resistors: one fixed and the other variable.

b) Six pins for rhythm selection. Internal pull-down is provided for all inputs. Rhythms are selected by connecting to V_{SS} the corresponding inputs.

c) One pin for external reset. The reset is applied when pin 1 is connected to V_{GG}. During normal operation pin 1 is connected to V_{SS}.

d) Five output pins. The following options are available:
- push-pull outputs
- open drain outputs
- trigger outputs (no external pulse shaping required)
- continuous outputs
- active high or active low outputs.

Full details concerning these options are given later.

e) Low impedance down beat output through which a LED can be driven.

f) 2 supply pins.

OPERATION

When the power supply is connected to the V_{GG} pin, the internal oscillator starts driving the counter and strobe generator. As long as no rhythm is selected no signal can flow from the output section. The output signal is present when one or more rhythms are selected. The internal counter has a 16 state (i.e. 16 elementary times) cycle and an internal reset signal is generated when the sixteenth state is decoded. Rhythms with a 3/4 time originate the internal reset when the 12th state is decoded. The down beat output is synchronized with the counter state 1 and its duration equals that of one elementary time. Rhythms with 8 or 6 elementary times are also programmable, in which case they are written twice in the ROM. The associated down beat signal can flow either every 8 (6) or every 16 (12) elementary times according to the option chosen. When the external reset is applied the counter is reset to state 1 and the oscillator and strobe generator are stopped. The down beat output is ON during the entire external reset condition since the first elementary time is decoded. For the same reason the content of the first elementary time is immediately available on the outputs as soon as the external reset is removed. The trigger outputs are pulse shaped and their width equals 1/32 of one elementary time. Pulse width is proportional to clock period but always remains 1/32 of a beat time. The clock frequency can be controlled by the external 1 Mohm potentiometer; the control range is greater than one decade.

PROGRAMMING THE OPTIONS

The five outputs of the M 255 may have different options which must be specified together with the ROM truth table. This can be done as shown in the table below:

Line		OUT. 1	OUT. 2	OUT. 3	OUT. 4	OUT. 5
1	Continuous or Trigger Output	T	T	C	T	T
2	Open drain or Push Pull	O	O	O	O	O
3	Posit. or Negat. Trigger Edge	+	+	+	–	–

T : Trigger: The output is in the form of a pulse whose width equals 1/32 of one elementary time. The pulse can be either positive or negative going according to the option chosen in line 3.

C : Continuous. No pulse shaping is provided and the output goes high or low according to line 3 choice for the duration of one elementary time. If such an output is selected in two or more consecutive elementary times it will stay continuously high (low).
O : Open drain output.
P : Push-pull output.
+ : The output is normally at V_{GG} and goes high when active.
– : The output is normally at V_{SS} and goes low when active.

The following constraints must be observed:
1) Only one of the five outputs may be continuous (C); the other four must be trigger (T).
2) If the open drain solution is used all outputs must be open drain (O).
3) If the push-pull solution is used all outputs labelled T must be push-pull (P) and the one labelled C must be open drain (O).

The down beat signal can be programmed to occur either every 8 (6) or every 16 (12) elementary times. The choice is made as shown in the example below:

	16 (12)	8 (6)
Down beat		X

In this case the down beat signal occurs every 8 (6) elementary times irrespective of the fact that there might be some 1x16 or 1 x 12 rhythms.

STATIC ELECTRICAL CHARACTERISTICS

(Positive logic, V_{GG} = -11.5 ± 20%, V_{SS} = +5 ± 20%, T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
RHYTHM AND RESET INPUTS						
V_{IH}	High voltage		V_{SS}-1		V_{SS}	V
V_{IL}	Low voltage		V_{GG}		V_{SS}-4.1	V
INSTRUMENT OUTPUTS Open Drain configuration						
R_{ON}	Output resistance (ON state)	R_L = 10 KΩ		125	250	Ω
V_{OH}	Output high voltage	R_L = 10 KΩ	V_{SS}-0.3		V_{SS}	V
I_{LO}	Output leakage current	$V_{EXT.RES.}$ = V_{IH} T_{amb} = 25°C			-10	µA
Push-Pull configuration						
R_{ON}	Output resistance at high output level	I_{OH} = -1 mA V_o = V_{OH}		250	500	Ω
V_{OL}	Output low voltage	Capacitive load	V_{SS}-15.2		V_{SS}-7.5	V
V_{OH}	Output high voltage	Capacitive load	V_{SS}-0.6			V

RC Input: this input oscillates between two negative levels whose value depends on the supply voltage level.
With V_{GG} = -17 and V_{SS} = 0V, V_{RC} low = -8.7V and V_{RC} high = -3.2V.
This input is protected, like the others, from electrical discharges.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DOWN BEAT OUTPUT						
R_{IN}	Internal resistance to V_{GG}	$V_o=V_{SS}-5V$		400	600	kΩ
R_{ON}	Output resistance (ON state)	$V_o=V_{SS}-0.5V$		250	500	Ω
V_{OH}	Output high voltage	Capacitive load	$V_{SS}-0.6$			V
V_{OL}	Output low voltage	Capacitive load	$V_{SS}-17.7$		$V_{SS}-10.7$	V
POWER DISSIPATION						
I_{GG}	Supply current	$T_{amb}=25°C$ I_o (pin 3)= 0		5	10	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (Positive logic $V_{GG}=-11.5 \pm 20\%$, $5 \pm 20\%$, $T_{amb}=0$ to 70°C unless otherwise specified)

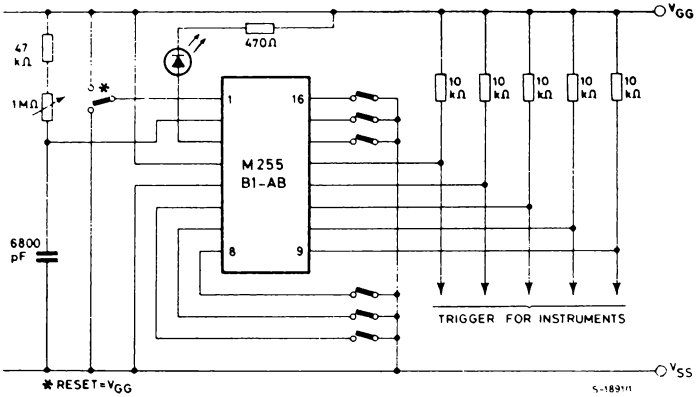
Parameter	Test conditions	Min.	Typ.	Max.	Unit
TEMPO CONTROL (RC)					
Minimum tempo	C to V_{SS}= 6800 pF R to V_{GG}= 1.05 MΩ	2.5*			Hz
Maximum tempo	C to V_{SS}= 6800 pF R to V_{GG}= 47 KΩ			35*	Hz

* These values depend on power supply voltages and temperature.

PERCENTAGE VARIATIONS of MAX. and MIN. TEMPO DUE TO V_{GG} and TEMPERATURE CHANGES

Parameter	Test conditions	Min.	Typ.	Max.
Max. tempo variation due to V_{GG} change	$V_{SS}-V_{GG}$ from 13 to 20V		4%	6%
Min. tempo variation due to V_{GG} change	$V_{SS}-V_{GG}$ from 13 to 20V		4%	6%
Max. tempo variation due to temperature change	T from 25°C to 70°C		2%	3%
Min. tempo variation due to temperature change	T from 25°C to 70°C		2%	3%

TYPICAL APPLICATION FOR M 255 B1-AB



COMPLETING THE TRUTH TABLE

The ROM truth table has been organized in 16 rows which represent the elementary times and 30 columns (6 groups of 5). The timing for the beats required for each instrument is programmed by crossing the appropriate box. The options for outputs and down beat must also be filled in as explained. Table 1 shows the content and the options programmed in the M 255 B1-AB standard content.

TRUTH TABLE of M 255 B1-AB (standard content)

	RHYTHM 1					RHYTHM 2					RHYTHM 3					RHYTHM 4					RHYTHM 5					RHYTHM 6				
Counter state	OUTPUT1	OUTPUT2	OUTPUT3	OUTPUT4	OUTPUT5	OUTPUT1	OUTPUT2	OUTPUT3	OUTPUT4	OUTPUT5	OUTPUT1	OUTPUT2	OUTPUT3	OUTPUT4	OUTPUT5	OUTPUT1	OUTPUT2	OUTPUT3	OUTPUT4	OUTPUT5	OUTPUT1	OUTPUT2	OUTPUT3	OUTPUT4	OUTPUT5	OUTPUT1	OUTPUT2	OUTPUT3	OUTPUT4	OUTPUT5
1	X		X			X		X		X	X		X			X		X			X	X	X			X	X			X
2								X										X					X		X					
3		X			X		X	X		X								X			X		X							
4						X		X			X	X	X		X		X	X		X	X	X	X		X					
5		X			X	X		X										X					X			X	X			X
6								X		X			X			X		X					X		X					
7	X		X	X			X	X			X		X	X		X		X	X		X	X	X	X	X					
8								X										X					X							
9		X			X	X		X		X								X			X		X		X	X	X			X
10						X		X			X	X	X	X	X		X	X		X			X							
11		X			X		X	X										X				X	X		X					
12						X		X		X			X			X		X	X				X							
13						X		X															X		X	X	X			X
14							X	X														X	X		X					
15						X		X													X		X	X		X	X	X	X	X
16						X	X	X	X												X		X	X	X					
Option on the Outputs											O1		O2		O3		O4		O5							16 (12)		8 (6)		
Continuous or Trigger Output											T		T		T		T		T		Down beat					X				
Open drain or push-pull											O		O		O		O		O											
Positive or Negative Trigger Edge											+		+		+		+		+											

PRELIMINARY DATA

RHYTHM GENERATORS

- 16 PROGRAMMABLE RHYTHMS (CODED FOR THE M258; ALSO AVAILABLE IN COMBINATION FOR THE M259
- 16 OUTPUTS (2 SECTIONS BY 8)
- MASK PROGRAMMABLE RESET COUNTS (24 or 32)
- DOWN BEAT OUT
- SYNC OUT
- EXTERNAL RESET
- TWO CHIP SELECTS (CS1, CS2) FOR SEPARATE TRISTATE CONDITION OF THE TWO OUTPUT SECTIONS
- INTERNAL PULL-UP ON THE INPUTS
- OPEN DRAIN OUTPUTS WITH RETURN TO "1" STATUS
- CHOICE BETWEEN RETURN TO "1" OR NOT ON 8 OUTPUTS (OUT 1, 2, 3, 4, 9, 10, 11, 12) SEPARATELY
- ONLY ONE POWER SUPPLY (+5V)
- VERY LOW POWER CONSUMPTION (150 mW TYP.)

The M258, M259 are monolithic rhythm generators specifically designed for electronic organs and other musical instruments.
Constructed on a single chip using MOS N-channel silicon gate technology, they are supplied in a 28 lead for (M258) or 40 lead for (M259) dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Source supply voltage	-0.3 to +7	V
V_i**	Input voltage	-0.3 to +7	V
I_o	Output current (at any pin)	3	mA
V_{OH}	Output voltage	12	V
T_{stg}	Storage temperature range	-65 to +125	°C
T_{op}	Operating temperature range	0 to 70	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

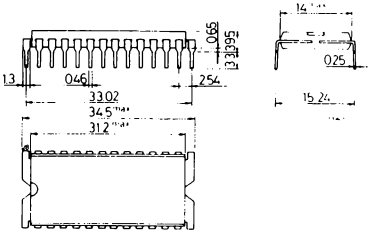
** All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS: M258 B1 for dual in-line plastic package
M259 B1 for dual in-line plastic package

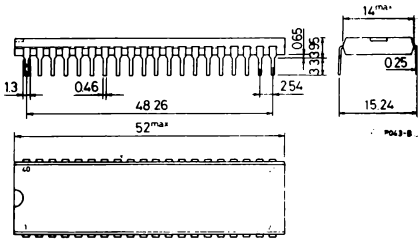
M 258
M 259

MECHANICAL DATA (dimensions in mm)

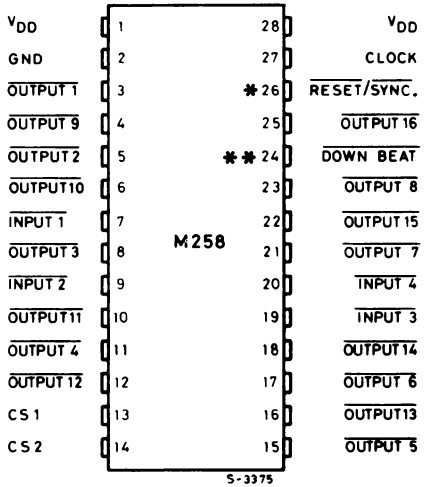
Dual in-line plastic package (28 lead)



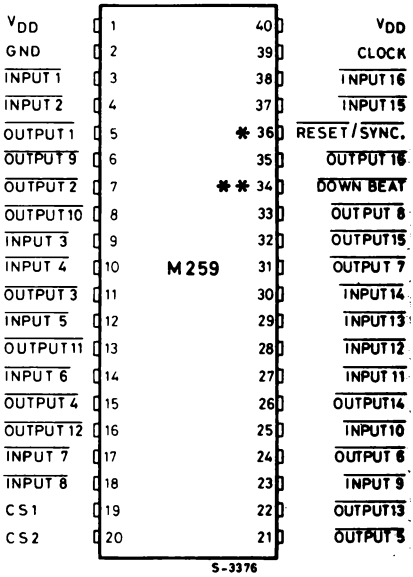
Dual in-line plastic package (40 lead)



CONNECTION DIAGRAMS



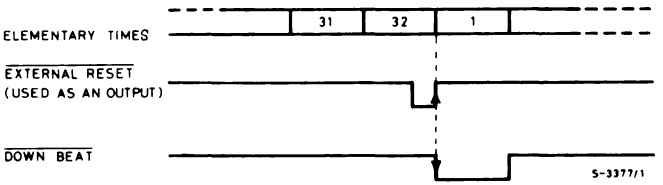
CS1 enables the outputs 01 to 08
CS2 enables the outputs 09 to 16



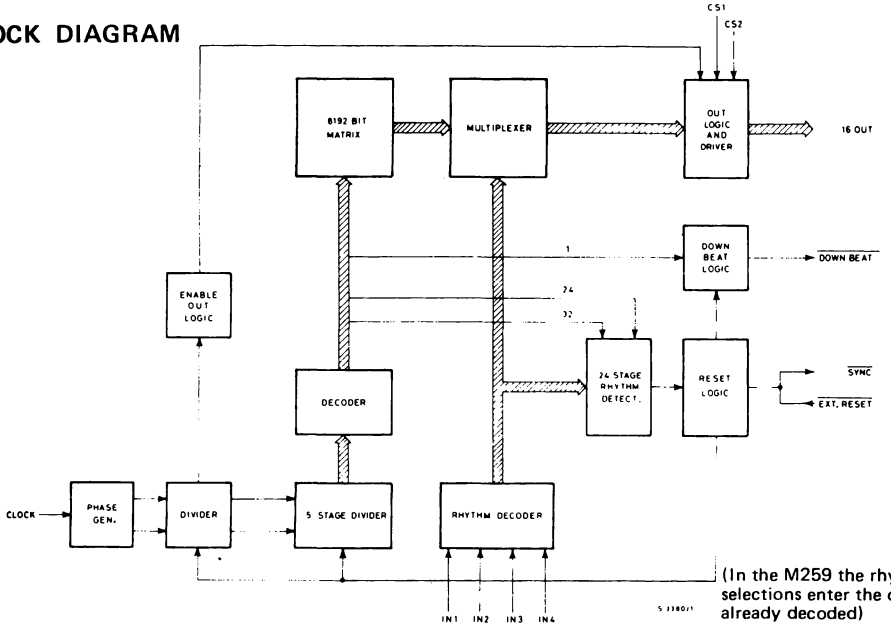
* This is a bidirectional pin. Used as an input it allows the chip reset; used as an output it can reset other devices.

** This pin generates a down beat trigger which can be used to drive an external lamp to indicate the first beat of the first bar of each rhythm.

RESET AND DOWN BEAT TIMING WAVEFORMS (POSITIVE LOGIC)



BLOCK DIAGRAM



(In the M259 the rhythm selections enter the chip already decoded)

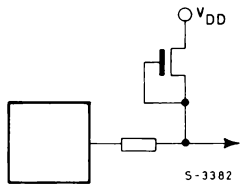
RHYTHM, SELECTION (for M258 only)

Rhythm	$\overline{IN4}$	$\overline{IN3}$	$\overline{IN2}$	$\overline{IN1}$
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

STATIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD}= 4.75 to 5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
CLOCK INPUT							
V_{IH}	Clock high voltage			2.4		V_{DD}	V
V_{IL}	Clock low voltage			0		0.4	V
DATA INPUTS ($\overline{IN1}$ to $\overline{IN4}$)							
V_{IH}	Input high voltage			2.4		V_{DD}	V
V_{IL}	Input low voltage			0		0.4	V
R_{IN}	Internal resistance to V_{DD}	V_I = 0V	V_{DD}= 5V	100	180		KΩ
I_{OL}(*)	Input load current	$V_I = V_{IL}$			-50		µA
EXT. RESET							
V_{IH}	Input high voltage			4.5		V_{DD}	V
V_{IL}	Input low voltage			0		1.5	V
R_{OFF}	Internal resistance to V_{DD} (inactive sync)	V_O= 0	V_{DD}= 5V	100	180		KΩ
R_{ON}	Internal resistance to V_{DD} (active sync)	V_O= 1V	V_{DD}= 4.75V		260	300	Ω
OUTPUTS (O_i, Down beat)							
R_{ON}	Input internal pull-up	V_O= 1V			260	300	Ω
V_{OL}	Input internal pull-up	Source current = 1 mA			0.26	0.3	V
I_{LO}		V_O= 12V	T_{amb}= 25°C			10	µA
POWER DISSIPATION							
I	Supply current	T_{amb}= 25°C			30		mA

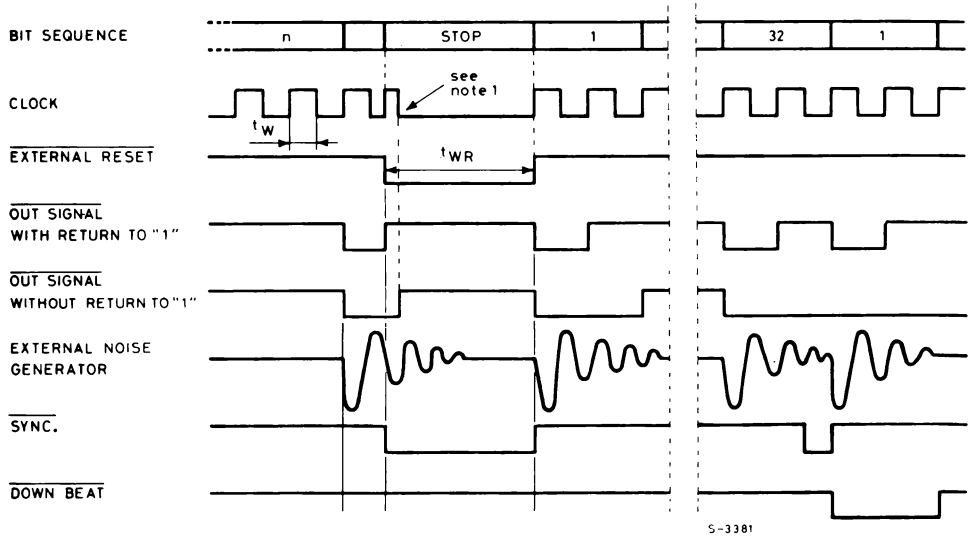
(*) The "High Level" is clamped by the internal pull-up.



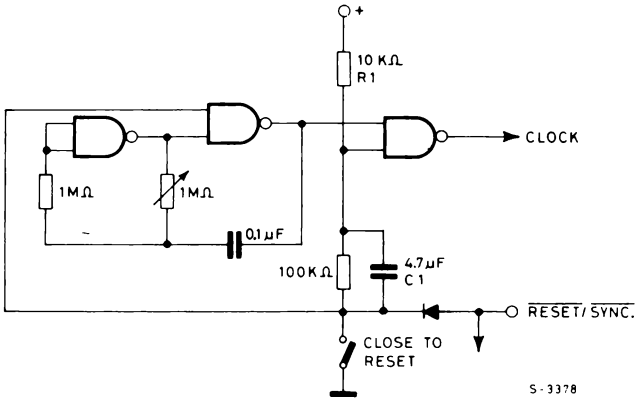
DYNAMIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD}= 4.75 to 5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test condistions	Values			Unit
			Min.	Typ.	Max.	
CLOCK INPUT						
f	Clock repetition rate		DC		100	KHz
t_w	Pulse width	Measured at 50% of the swing	5			µs
t_r	Rise time	Measured between 10% and 90% of the swing			100	µs
t_f	Fall time	Measured between 10% and 90% of the swing			100	µs
EXT. RESET						
t_{wR}	Pulse width		100			µs
t_{CR}	Clock delay with respect to reset		0			µs

TIMING WAVEFORMS

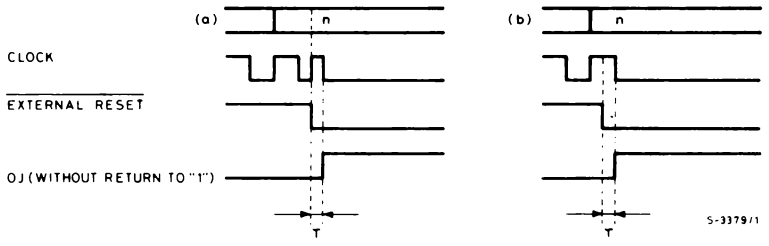


Note 1: This additional pulse, to reset the outputs without return to "1", can be obtained by using a clock generator as shown in the following diagram:



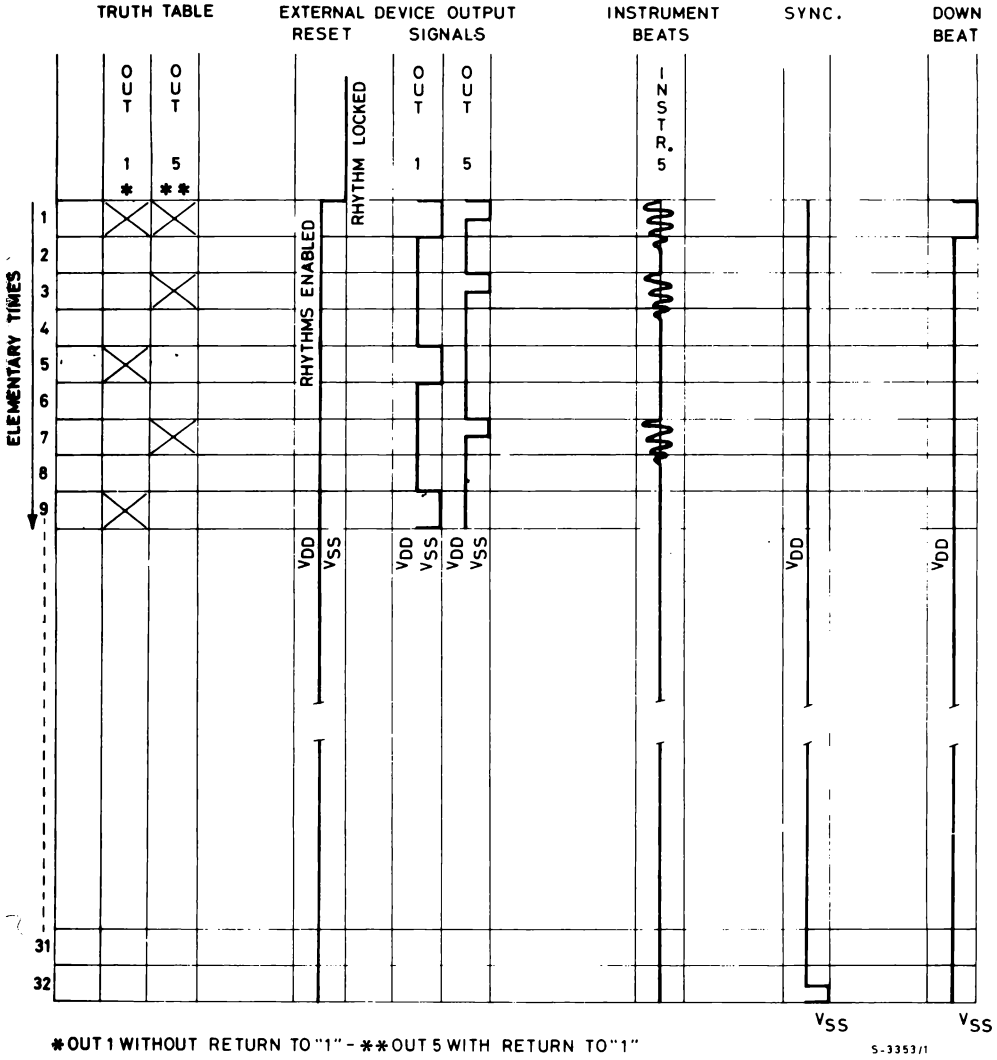
Ext. Reset/Sync. is a bidirectional pin. Used as an input it can reset the circuit as shown in the timing diagram and used as an output it can drive the reset of other devices.

Using the clock generator shown in the above figure, when the switch is closed asynchronous with respect to the clock, it is possible to have to two cases (see the following diagrams); in both the cases the output reset can be obtained by CS1 and CS2.



In both the cases the delay τ (in the outputs without return to "1") is defined through the constant R1 C1 $\geqslant$ 10 μsec.

INSTRUMENT BEATS VERSUS RHYTHM PROGRAM



Note: The outputs 01 to 08 are enabled by CS1; the outputs 09 to 16 are enabled by CS2. The outputs 01 to 04 and 09 to 12 are programmable separately without return to "1".

16-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{CC} (TYP.)
- INPUTS FULLY PROTECTED
- INVERTER AVAILABILITY IN CRYSTAL OSCILLATOR IMPLEMENTATION FOR TIMING APPLICATIONS

The M 702 D2 (extended temperature range) and **M 702 D1/B1** (intermediate temperature range) are **16**-stage binary countes constructed with COS/MOS technology in a single monolithic chip. The devices **may** be used as timing circuits the chips consists of 16-flip-flop, input inverter for use in a cristal oscilla**tor**, and an output buffer capable of driving standard stepping motors.
The device is available in 8-lead dual in-line miniature plastic package and 8-lead metal-can.

ABSOLUTE MAXIMUM RATINGS *

V_{DD}**	Supply voltage	-0.5 to	15	V
V_I	Input voltage (at any pin)	-0.5 to V_{DD}	+0.5	V
P_{tot}	Total power dissipation (per package)		200	mW
T_{stg}	Storage temperature	-65 to	150	°C
T_{op}	Operating temperature: for **D2** type	-55 to	125	°C
	for **D1/B1** type	-40 to	85	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** This voltage value are referred to V_{SS} pin voltage.

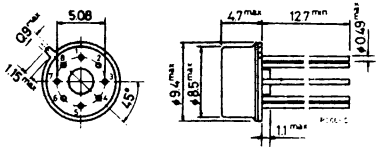
ORDERING NUMBERS:

M 702 D2 for TO-99 metal can
M 702 D1 for TO-99 metal can
M 702 B1 for dual in-line plastic package

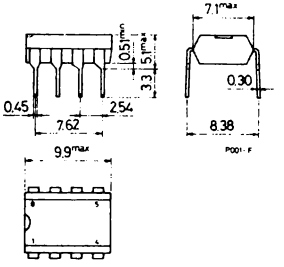
MECHANICAL DATA

Dimensions in mm

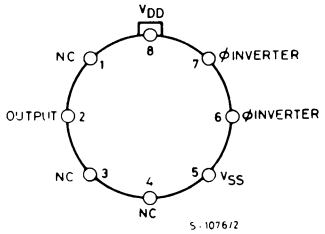
TO-99 metal can

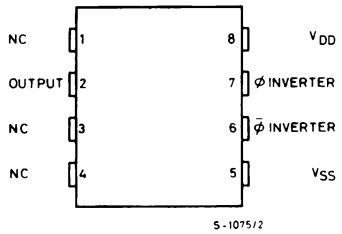


Dual in-line plastic package

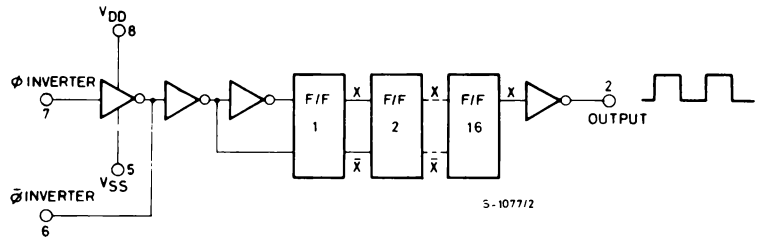


CONNECTION DIAGRAMS





LOGIC BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 15	V
	for crystal oscillator in clock applications	7 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **D2** type	-55 to 125	°C
	for **D1/B1** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

D2 type (extended temperature range)

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-55°C			25°C			125°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_L	Quiescent supply current			5			15		0.5	15			900	µA
				10			25		1	25			1500	
				15			50		1	50			2000	
V_{OH}	Output high voltage	$I_O = 0$		5	4.99			4.99	5		4.95			V
				10	9.99			9.99	10		9.95			
V_{OL}	Output low voltage	$I_O = 0$		5			0.01		0	0.01			0.05	V
				10			0.01		0	0.01			0.05	
V_{NH}	Noise immunity			5	1.4			1.5	2.25		1.5			V
				10	2.9			3	4.5		3			
V_{NL}	Noise immunity			5	1.5			1.5	2.25		1.4			V
				10	3			3	4.5		2.9			
I_{DN}	Output drive current N-channel		0.5	5	12.5			12	15		8			mA
			0.5	10	18.5			18	20		14			
I_{DP}	Output drive current P-channel		4.5	5	-12.5			-12	-15		-8			mA
			9.5	10	-18.5			-18	-20		-14			
I_{IH},I_{IL}	Input leak.current	Any input		15			±1		$\pm 10^{-5}$	±1			±1	µA

D1/B1 types (intermediate temperature range)

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_L	Quiescent supply current			5			50		1	50			700	µA
				10			100		2	100			1400	
				15			900		10	900			5000	
V_{OH}	Output high voltage	I_{OH}=0		5	4.99			4.99	5		4.95			V
				10	9.99			9.99	10		9.95			
V_{OL}	Output low voltage	I_{OL}=0		5			0.01		0	0.01			0.05	V
				10			0.01		0	0.01			0.05	
V_{NH}	Noise immunity			5	1.4			1.5			1.5			V
				10	2.9			3	4.5		3			
V_{NL}	Noise immunity			5	1.5			1.5	2.25		1.4			V
				10	3			3	4.5		2.9			
I_{DN}	Output drive current N-channel		0.5	5	12.5			12	15		8			mA
			0.5	10	18.5			18	20		14			
I_{DP}	Output drive current P-channel		4.5	5	-12.5			-12	-15		-8			mA
			9.5	10	-18.5			-18	-20		-14			
I_{IH},I_{IL}	Input leak.current	Any input		15			±1		$\pm 10^{-5}$	±1			±1	µA

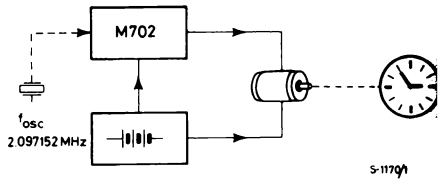
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

Parameter		Test conditions	V_{DD} (V)	Values						Unit
				M 702 D2			M 702 D1/B1			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{WH}, t_{WL}	Minimum input pulse width		5		100	115		100	140	ns
			10		50	60		50	75	
t_r, t_f	Input clock rise and fall time		5			15			15	µs
			10			10			10	
f_{max}	Maximum clock frequency		5	4.4	5		8.5	10		MHz
			10	3.5	5		6.5	10		
C_I	Input capacitance	Any input			5			5		pF

TYPICAL APPLICATIONS

Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.
Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs.
Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.

Electronic watch application circuit



COS/MOS INTEGRATED CIRCUIT

M 706

PRELIMINARY DATA

16-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 16V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY IN CRISTAL OSCILLATOR IMPLEMENTATION FOR TIMING APPLICATION

The **M 706** is a 16-stage binary counter constructed with COS/MOS technology on a single monolithic chip. The device may be used as timing circuit. It consists of 16 flip-flops, input inverter for use in a crystal oscillator and two output buffers providing push-pull bridge operation. The device is available in 8-lead minidip.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to 16	V
V_I	Input voltage (at any pin)	-0.5 to V_{DD} +0.5	V
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	-40 to 85	°C

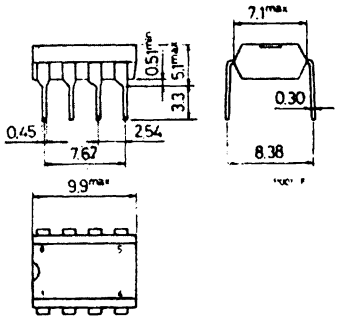
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** This voltage is with respect to V_{SS} (GND) pin voltage.

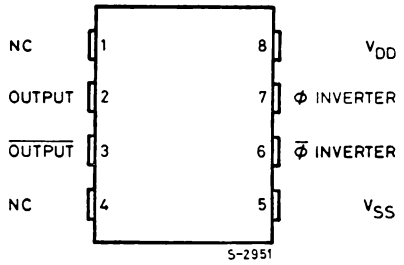
ORDERING NUMBER: M 706 B1

MECHANICAL DATA

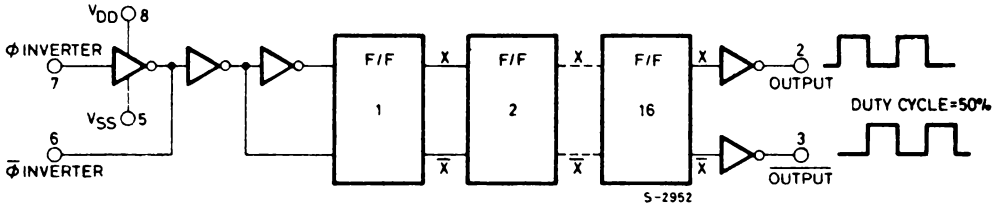
Dimensions in mm



CONNECTION DIAGRAM



LOGIC BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

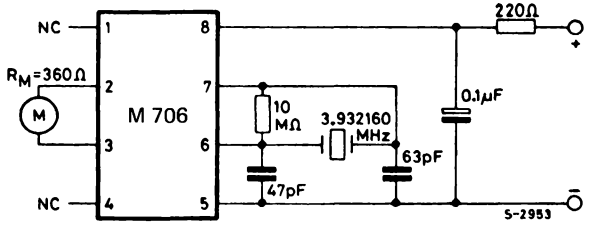
V_{DD}	Supply voltage: for general applications	3 to 15	V
	for crystal oscillator in clock application	7 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions			Values at 25°C			Unit
			V_O (V)	V_{DD}(V)	Min.	Typ.	Max.	
I_L	Quiescent supply current			5		1	50	µA
				10		2	100	
V_{OH}	High output voltage	I_O= 0		5	4.99	5		V
				10	9.99	10		
V_{OL}	Low output voltage	I_O= 0		5		0	0.01	V
				10		0	0.01	
I_{DN}	Output drive current N-channel		0.5	5	6	7.5		mA
			0.5	10	9	10		
I_{DP}	Output drive current P-channel		4.5	5	-6	-7.5		mA
			4.5	10	-9	-10		

TYPICAL APPLICATION

Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.
Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile blocks, and digital timing references in any circuit requiring accurately timed outputs.
Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.



COS/MOS INTEGRATED CIRCUIT

M 714

PRELIMINARY DATA

23-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- INPUTS FULLY PROTECTED
- OUTPUT WAVEFORMS SHAPED for a 25% DUTY CYCLE

The M714 (standard temperature range) is 23-stage binary counter constructed with MOS-P channel and N-channel enhancement mode devices in a single monolithic chip. The device may be used as timing circuit. It consist of 23 flip-flops, two output buffers, providing push-pull operation one zener diode providing transient protection at ~ 10V, and input inverters for use in a crystal oscillator. The device is available in 14-lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.5 to 15 V
V_I	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$
P_{tot}	Total power dissipation (per package, including zener diode)	200 mW
T_{stg}	Storage temperature	-65 to 150 °C
T_{op}	Operating temperature	-40 to 85 °C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

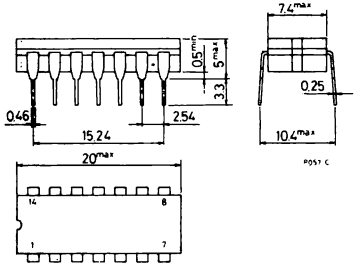
** With respect to V_{SS} (GND) pin.

ORDERING NUMBERS: M714 D1 for dual in-line ceramic package frit seal
M714 B1 for dual in-line plastic package

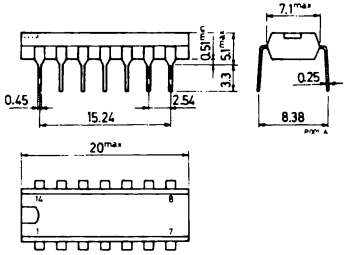
MECHANICAL DATA

Dimensions in mm

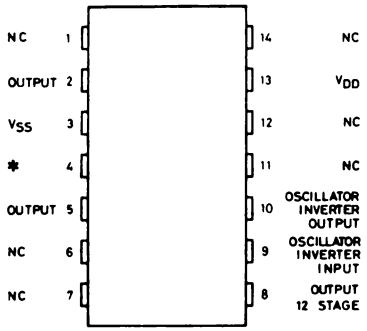
Dual in-line ceramic package, frit seal



Dual in-line plastic package



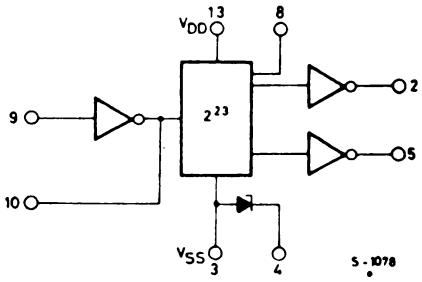
PIN CONNECTIONS



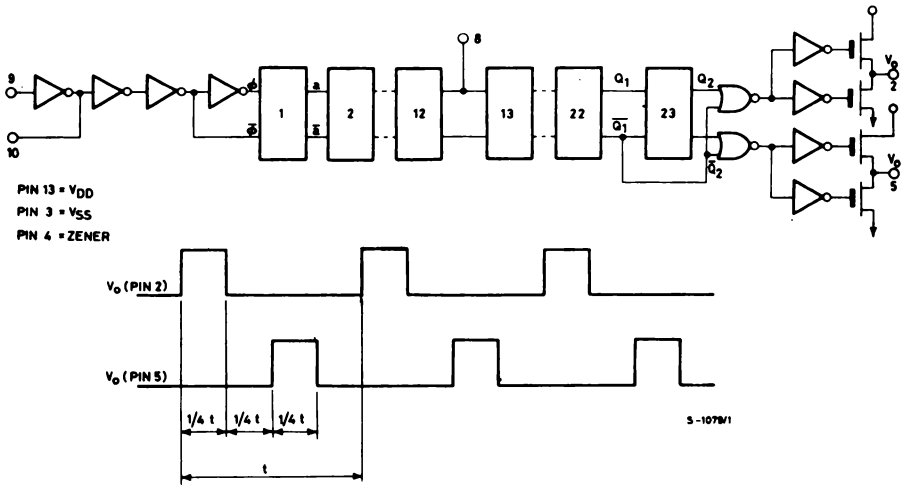
* ZENER CATHODE

5-1080/1

LOGIC DIAGRAM



BLOCK DIAGRAM and OUTPUT WAVEFORMS



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 15	V
	for oscillator starting	6 to 15	V
V_I	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

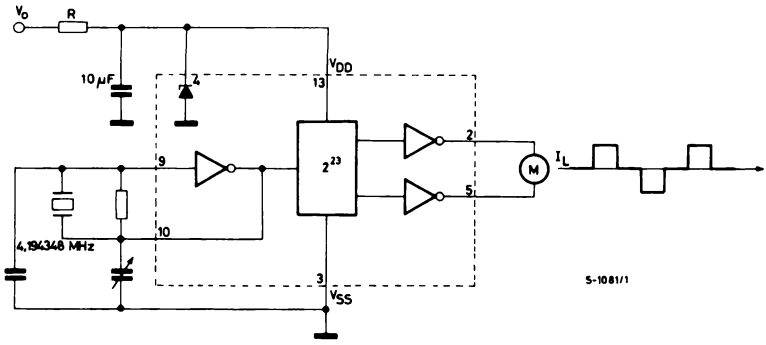
Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_L	Quiescent supply current			5			50		1	50			700	µA
				10			100		2	100			1400	
				15										
V_{OH}	Output high voltage	I_O= 0		5	4.99			4.99	5		4.95			V
				10	9.99			9.99	10		9.95			
V_{OL}	Output low voltage	I_O= 0		5			0.01		0	0.01			0.05	V
				10			0.01		0	0.01			0.05	
V_{NH}	Noise immunity			5	1.4			1.5	2.25		1.5			V
				10	2.9			3	4.5		3			
V_{NL}	Noise immunity		1	5	1.5			1.5	2.25		1.4			V
			1	10	3			3	4.5		2.9			
I_{DN}	Output drive current N-channel		0.5	5	2.2			1.8	4		1.3			mA
			0.5	10	3.5			2.8	8		2			
I_{DP}	Output drive current P-channel		4.5	5	-1.6			-1.3	-4		-0.9			mA
			9.5	10	-2.8			-2.3	-8		-1.6			
V_Z	Zener voltage	I_Z=100µA							10.5					V
		I_Z=10 mA							11.2					
I_{IH},I_{IL}	Input leakage curr.								10					pA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 15 pF, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns.

Parameter		Test conditions		Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_r, t_f	Input clock rise and fall time		5			15	µs
			10			10	
f_{CL}	Maximum clock input frequency		5	3.5	5		MHz
			10	6.5	10		
C_I	Input capacitance	Any input			5		pF

TYPICAL APPLICATIONS

Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.
Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs.
Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.



COS/MOS INTEGRATED CIRCUIT

M 730

PRELIMINARY DATA

23-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABLE
- MOTOR DRIVE STAGE OUTPUT

The M730 (standard temperature range) is a 23 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose, seven adjustment terminals are provided on the M730: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 14. If one or more adjustment terminals are grounded (taken to pin 13), the output frequency decreases. The by-four-divided oscillator frequency may be checked at a separate test output (pin 8) non-reactive with respect to the oscillator. Based on this check the output frequency and consequently the accuracy of the clock may be adjusted at the terminal 1 to 7 by means of the variable frequency divider. With an oscillator frequency of 4.194812 MHz, the series-connected push-pull output stage supplies a symmetrical square wave signal with a pulse duty factor of 0.5 and a repetition frequency of 0.5 Hz if the variable frequency divider is set to its medium value. The device is available in 14 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.3 to +17	V
I_{11}	Output current	60	mA
P_{tot}	Power dissipation at T_{amb} = 25°C	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

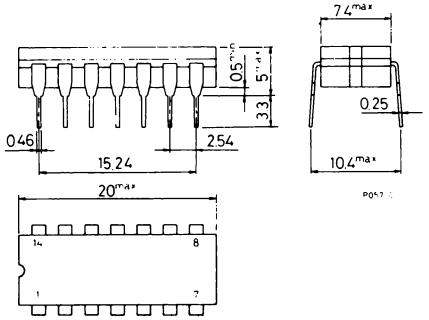
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

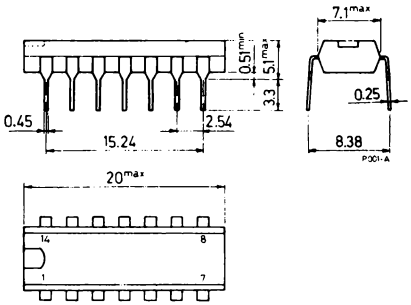
ORDERING NUMBERS: M730 B1 for dual in-line plastic package
M730 D1 for dual in-line ceramic package frit seal

MECHANICAL DATA (dimensions in mm)

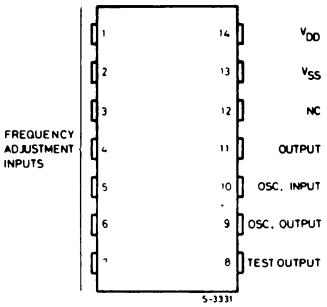
Dual in-line ceramic package frit seal



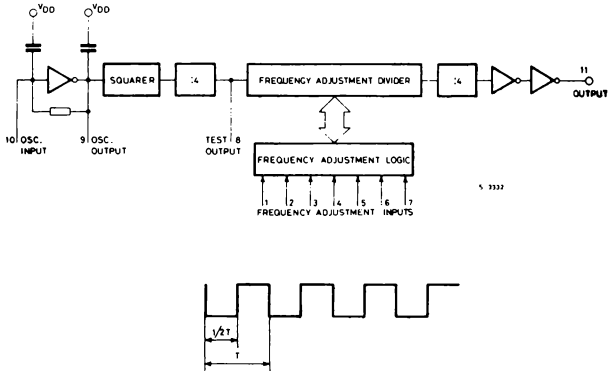
Dual in-line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
I_{11}	Output current	40	mA
T_{op}	Operating temperature	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions			Values									Unit
					-40°C			25°C			85°C			
			V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output high voltage	I_{OH}= 0		6	5.99			5.99	6		5.95			V
				12	11.99			11.99	12		11.95			
V_{OL}	Output low voltage	I_{OL}= 0		6			0.01		0	0.01			0.05	V
				12			0.01		0	0.01			0.05	
I_{DN}	Output drive current N-channel		2	6	21			20	25		13			mA
			2	12	34			33	40		22			
I_{DP}	Output drive current P-channel		4	6	21			20	25		13			mA
			10	12	34			33	40		22			
I_{ON}	Current consump.	I_O= 0*		12					3					mA

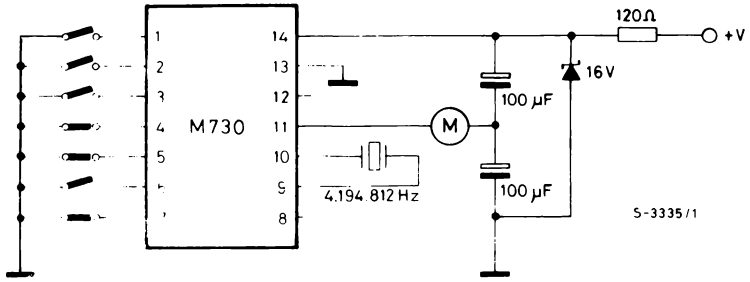
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter		Test conditions	V_{DD} (V)	Values						Unit
				M730 D1 type			M730 B1 type			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
f_T	Frequency test output		12		1.048703			1.048703		Hz
f_o**	Output frequency		12		0.5			0.5		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment		12		± 121			± 121		ppm
R_o	Output resistance	R_L= 300Ω	12			100			100	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUIT

M 731

PRELIMINARY DATA

16-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABLE
- MOTOR DRIVE STAGE OUTPUT

The M731 (standard temperature range) is a 16 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose seven adjustment terminals are provided on the M731: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 14. If one or more adjustment terminals are grounded (taken to pin 13), the output frequency decreases. The by-four-divided oscillator frequency may be checked at a separate test output (pin 8) non-reactive with respect to the oscillator. With an oscillator frequency of 4.194812 MHz, the series-connected push-pull output stage supplies a symmetrical square wave signal with a pulse duty factor of 0.5 and a repetition frequency of 64 Hz if the variable frequency divider is set to its medium value. The device is available in 14 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.3 to +17	V
I_{11}	Output current	60	mA
P_{tot}	Power dissipation at T_{amb} = 25°C	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

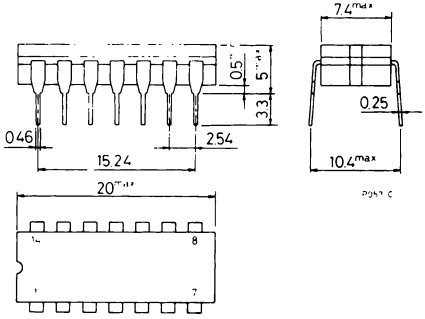
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

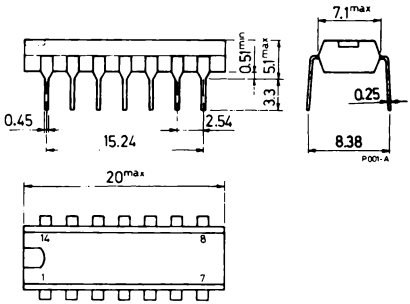
ORDERING NUMBERS: M731 B1 for dual in-line plastic package
M731 D1 for dual in-line ceramic package frit seal

MECHANICAL DATA (dimensions in mm)

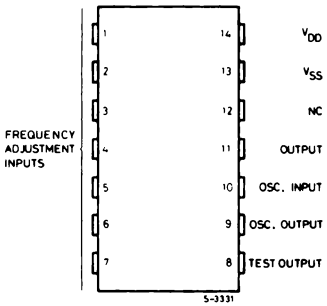
for dual in-line ceramic package, frit seal



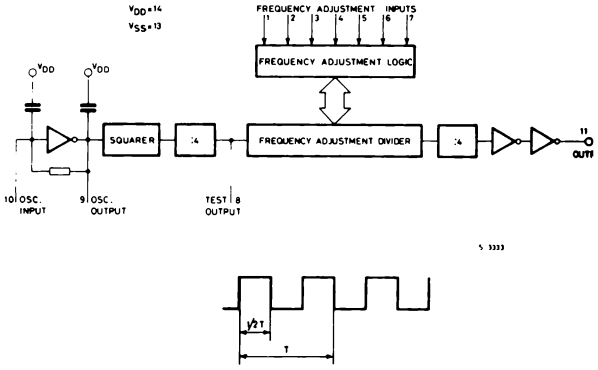
for dual in-line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
I_{11}	Output current	40	mA
T_{op}	Operating temperature	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output high voltage	I_{OH}= 0		6	5.99			5.99	6		5.95			V
				12	11.99			11.99	12		11.95			
V_{OL}	Output low voltage	I_{OL}= 0		6			0.01		0	0.01			0.05	V
				12			0.01		0	0.01			0.05	
I_{DN}	Output drive current N-channel		2	6	21			20	25		13			mA
			2	12	34			33	40		22			
I_{DP}	Output drive current P-channel		4	6	-21			-20	-25		-13			mA
			10	12	-34			-33	-40		-22			
I_{ON}	Current consump.	I_O= 0*		12					3					mA

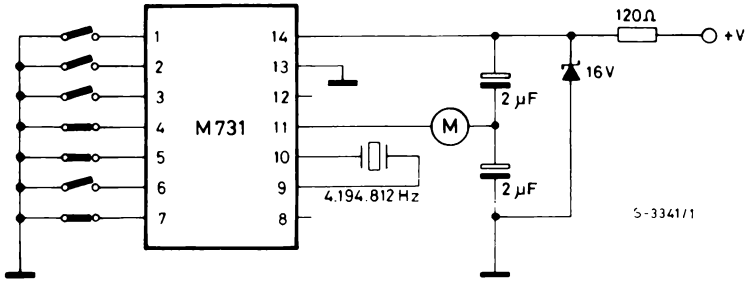
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter		Test conditions	V_{DD} (V)	Values						Unit
				M731 D1			M731 B1			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
f_T	Frequency test output		12		1.048703			1.048703		Hz
f_o**	Output frequency		12		64			64		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment		12		± 121			± 121		ppm
R_o	Output resistance	R_L= 300Ω	12			100			100	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

7-STAGE DIVIDER

- LOW POWER DISSIPATION
- LOW OUTPUT IMPEDANCE ON BOTH HIGH AND LOW STATE
- WIDE SUPPLY VOLTAGE RANGE: 5 to 15V
- HIGH NOISE IMMUNITY
- INPUTS FULLY PROTECTED

The M738/M740/M741/M747 are integrated circuits constructed in COS/MOS technology for use as frequency dividers in electronic organs. All the devices consist of 7 stages of binary division connected to give five divider blocks for the M741/M747 and four divider blocks for the M738/M740. The information transfer occurs on the positive going edge of the clock, for M740 and M747, and the negative going edge of the clock for M738/M741, and each output features a symmetrical impedance buffer (300Ω typ. at V_{DD}= 10V). They are available in 14 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS *

V_{DD} **	Supply voltage	-0.5 to	15	V
V_I	Input voltage (at any pin)	-0.5 to V_{DD} +0.5		V
P_{tot}	Total power dissipation (per package)		200	mW
T_{stg}	Storage temperature	-65 to	150	°C
T_{op}	Operating temperature	-40 to	85	°C

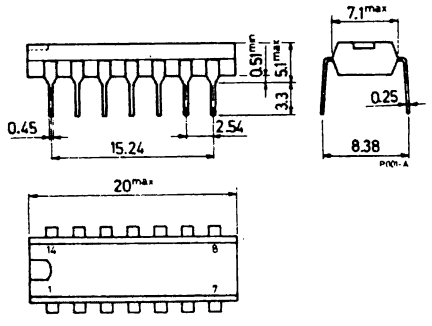
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages values are refered to V_{SS} pin voltage.

ORDERING NUMBERS: M 7XX B1 for dual in-line plastic package

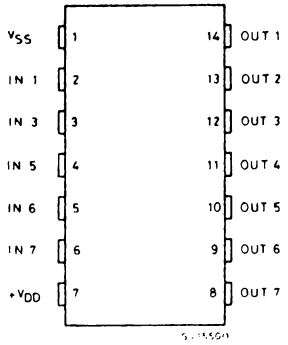
MECHANICAL DATA

Dimensions in mm

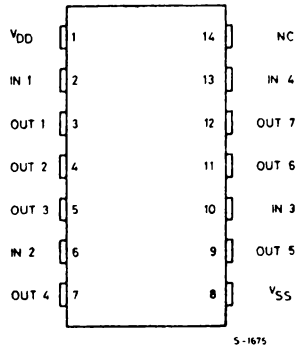


CONNECTION DIAGRAMS

For M741/M747

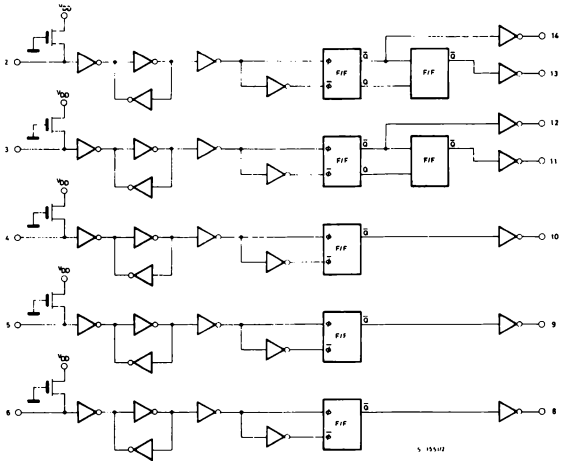


For M738/M740

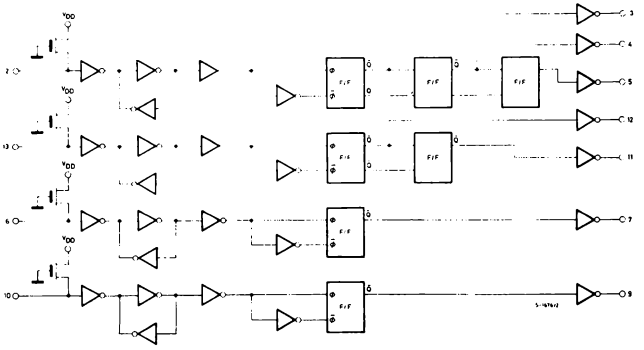


FUNCTIONAL DIAGRAMS

For M741/M747



For M738/M740



RECOMMENDED OPERATING CONDITIONS

Parameter		V_{DD}(V)	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		5		15	V
V_I	Input voltage		-0.5		V_{DD}+0.5	V
T_{op}	Operating temperature		-40		85	°C
t_w	Width of clock pulse (high or low)	5		200		ns
		10		100		

STATIC ELECTRICAL CHARACTERISTICS (over recomended operating conditions)

Typical values are at T_{amb} = 25°C

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CCL}	Quiescent supply current	V_i=V_{DD}		5			5			5			300	μA
				10			10			10			600	
				15			50			50			2000	
V_{OH}	High level output voltage	I_o= 0		5	4.99			4.99			4.95			V
				10	9.99			9.99			9.95			
				15	14.99			14.99			14.95			
V_{OL}	Low level output voltage	I_o= 0		5			0.01			0.01			0.05	V
				10			0.01			0.01			0.05	
				15			0.01			0.01			0.05	
I_{OL}	Output drive current N-channel		0.5	5	0.5			0.5	0.8		0.45			mA
			0.5	10	1			1	1.6		0.95			
			0.5	15	1.6			1.6	2.5		1.55			
I_{OH}	Output drive current P-channel		4.5	5	-0.5			-0.5	-0.8		-0.45			mA
			9.5	10	-1			-1	-1.6		-0.95			
			14.5	15	-1.6			-1.6	-2.5		-1.55			
I_{IL}	Input current	V_i= 0		15				3	30	100				μA
I_{IH}	Input current	V_i=V_{DD}		15			1			1			1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Parameter			Test conditions	Values				Unit
				V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time from inputs to:	1 division stage outputs	C_L = 15 pF on all outputs see timing diagram	5			500	ns
				10			250	
		2 division stage outputs		5			1000	ns
				10			500	
		3 division stage outputs		5			1500	ns
				10			750	
t_{TLH}, t_{THL}	Output transition time			5			500	ns
				10			250	
f_{max}	Maximum toggle frequency		C_L= 15 pF on all outputs	5	0.6	2.5		MHz
				10	2	5		
*	Cross talk immunity level					70		dB
C_I	Input capacitance					5		pF

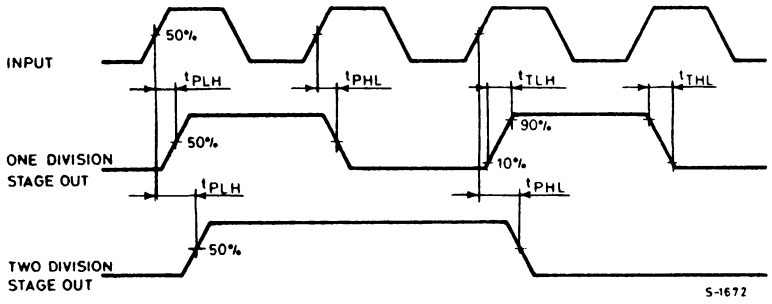
* Send a frequency of 20 kHz to input V_{I1} charge output V_{O1} with 5 kΩ and 15 pF, measure the level of the 10 kHz frequency present at all outputs.

Cross talk level = $20 \log \frac{V_{O1}\ (10\ kHz)}{V_{OX}\ (10\ kHz)}$.

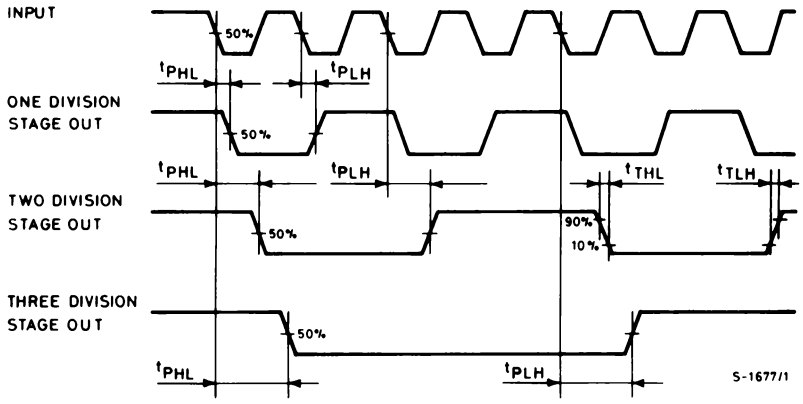
With the exception of V_{O1}, the output where the 10 kHz signal is greatest is V_{OX}.
This operation is repeated for all the inputs.

TIMING DIAGRAM

For M740/M747



For M738/M741



COS/MOS INTEGRATED CIRCUIT

M 750

PRELIMINARY DATA

23 STAGE COUNTER WITH INTERMEDIATE OUTPUT AT THE 16th STAGE

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABLE
- MOTOR DRIVE BRIDGE CONFIGURATION OUTPUT

The M750 is a 23 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose seven adjustment terminals are provided on the M750: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 16. If one or more adjustment terminals are grounded (taken to pin 14), the output frequency decreases. With an oscillator frequency of 4.194812 MHz the bridge configuration outputs supply two symmetrical square wave signals whose frequency is 0.5 Hz; the pulse duty factor is 0.5 and their relative delay is of half period. The intermediate output provides a 64 Hz signal with pulse duty cycle of 50%. The by-four-divided oscillator frequency may be checked at a separate test output (pin 9) non-reactive with respect to the oscillator. The device is available in 16 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.3 to +17	V
I_{12}, I_{13}	Output current	30	mA
P_{tot}	Power dissipation at T_{amb}= 25°C	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

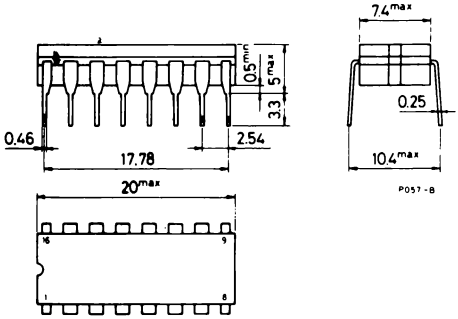
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages values are refered to V_{SS} pin voltage.

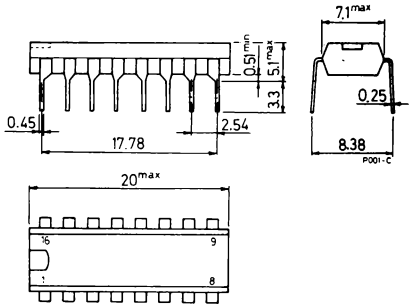
ORDERING NUMBERS: M750 B1 for dual in-line plastic package
M750 D1 for dual in-line ceramic package frit seal

MECHANICAL DATA (dimension in mm)

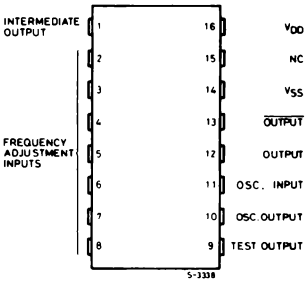
For dual in-line ceramic package, frit seal



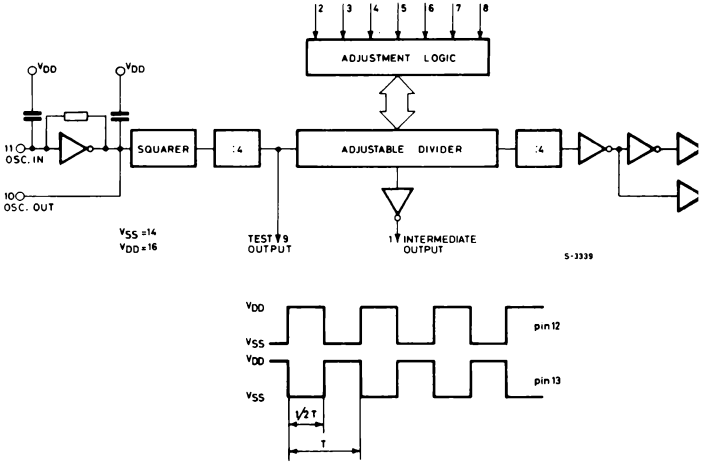
For dual in-line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
R_L	Output load resistance between pin 12 and 13	300	Ω
T_{op}	Operating temperature	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter	Test conditions	V_O (V)	V_{DD} (V)	Values									Unit
				-40°C			25°C			85°C			
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH} Output high voltage	I_{OH}= 0		6	5.99			5.99	6		5.95			V
			12	11.99			11.99	12		11.95			
V_{OL} Output low voltage	I_{OL}= 0		6			0.01		0	0.01			0.05	V
			12			0.01		0	0.01			0.05	
I_{ON} Output drive current N-chan.	pin 12-13	2	6	10.5			10	12.5		6.5			mA
		2	12	17			16.5	20		6.5			
I_{OP} Output drive current P-chan.	pin 12-13	4	6	-10.5			-10	-12.5		-6.5			mA
		10	12	-17			-16.5	-20		-6.5			
I_{ON} Current consumption	I_O= 0*		12					3					mA

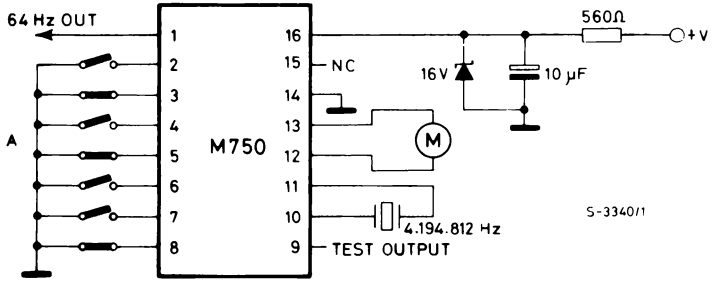
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter	Test conditions	V_{DD} (V)	Values						Unit
			M750 D1			M750 B1			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
f_T Frequency test output		12	1.048703			1.048703			Hz
f_o** Output frequency		12		0.5			0.5		Hz
$\frac{\Delta f_o}{f_o}$ Range output frequency adjustment		12		± 121			± 121		ppm
R_o Total bridge output resistance	R_L= 300Ω	6			300			300	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUIT

M 751

PRELIMINARY DATA

TOUCH TONE GENERATOR

- 2.5 to 5V SUPPLY
- INTERNAL PULL-UP WITH DIODE PROTECTION ON ALL INPUTS
- ON CHIP CRYSTAL CONTROLLED OSCILLATOR: 4.433619 MHz
- INTERNAL CAPACITORS FOR THE CRYSTAL OSCILLATOR
- LOW HARMONIC DISTORTION
- HIGH BAND TONES PRE-EMPHASIS

The M751 can provide all tone frequency pairs required for the Touch Tone Dialling System. The output frequencies are obtained from an internal crystal controlled oscillator whose frequency is reduced in two independent programmable counters. The dividing ratio is controlled by the selected key. The circuit is to be used with 4 x 4 matrix keyboard which generates 4 rows and 4 columns input signals in a 2 by 8 contacts closed to ground format. If two or more keys are activated simultaneously no-illegal tones are sent on the line; if only one contact per each key is grounded, the selected column or row tone is generated. An internal buffer is provided to achieve a 2 pole low-pass active filter requiring only 4 external passive components. The filtered output tone must be adequately interfaced to the telephone line. The device can be supplied in plastic or ceramic 16 pin dual in-line package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.5 to V_{DD}	+5.5	V
V_I	Input voltage	-0.3 to V_{DD}	+5.5	V
T_{op}	Operating temperature range	-25 to	+50	°C
T_{stg}	Storage temperature range	-55 to	+125	°C
P_{tot}	Power dissipation		400	mW

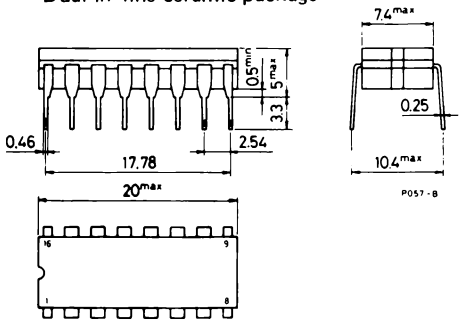
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are refered to V_{SS} pin voltage.

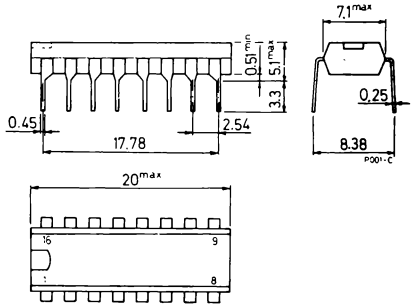
ORDERING NUMBERS: M751 B1 for dual in-line plastic package
M751 D1 for dual in-line ceramic package

MECHANICAL DATA (dimensions in mm)

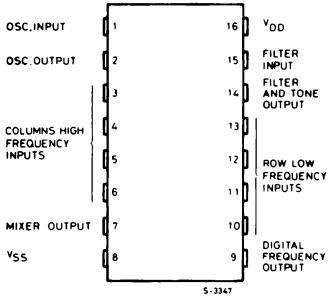
Dual in-line ceramic package



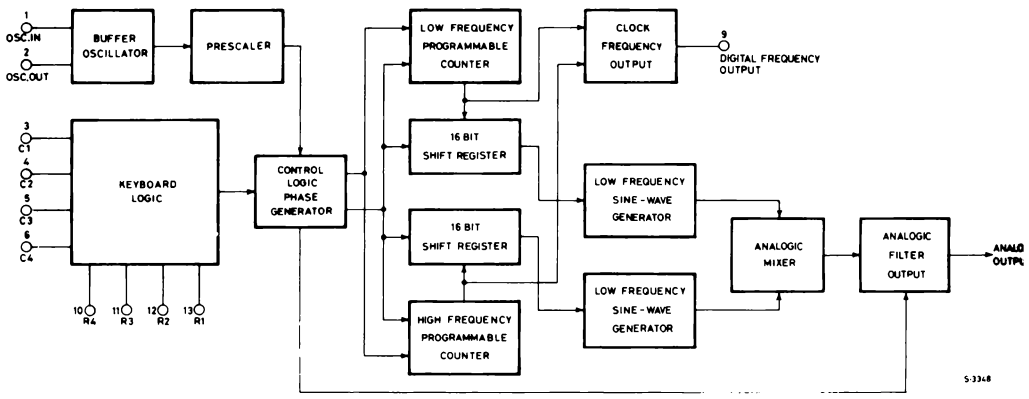
Dual in-line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (All parameters are 100% tested at 25°C, T_{amb}= 25°C)

	Parameter	Test conditions	Values			Unit
			Min.	Typ.	Max.	
DC CHARACTERISTICS						
Supplies	V_{DD} Voltage supply range		2.5	3	5	V
	V_{DD} Operating supply range	V_{DD}= 3V		2.5	3.5	mA
Inputs	I_{INH} Input high current	V_{DD}= 3V V_{IH} = 3V			1	µA
	I_{INL} Input low current	V_{DD}= 3V V_{IL} = 0V	-1		-25	µA
Outputs	I_{OL} Output sink current at digital frequency output	V_{DD}= 3V See note 1 V_{OL}= 1V	200			µA
AC CHARACTERISTICS						
$\Delta f/f$	Maximum output tones frequency tolerance	At crystal frequency f_o = 4.433619 MHz		0.4	1.2	%
V_{LF}	Nominal output amplitude lower tones at filter tone output; pin 14	V_{DD}= 3V See note 2	150	175	200	mVpp
V_{HF}	Nominal output amplitude high tones at filter tone output; pin 14	V_{DD}= 3V See note 2	195	220	245	mVpp
	Preeamphasis		1	2	3	dB
V_{DC}	Continuous output at filter tone output; two tones activated	V_{DD}= 3V See note 3		1.1		V
	Unwanted frequency components	f = 3.4 KHz			-33	dB m
		f = 50 KHz			-80	dB m
	Total harmonic distortion for single frequency				2	%
t_s	Start-up time	V_{DD}= 3V See fig. 2		3	5	ms
t_r	Maximum voltage supply rise time	V_{DD}= 3V See fig. 2			0.5	ms

Note 1 : Digital frequency output is open drain.

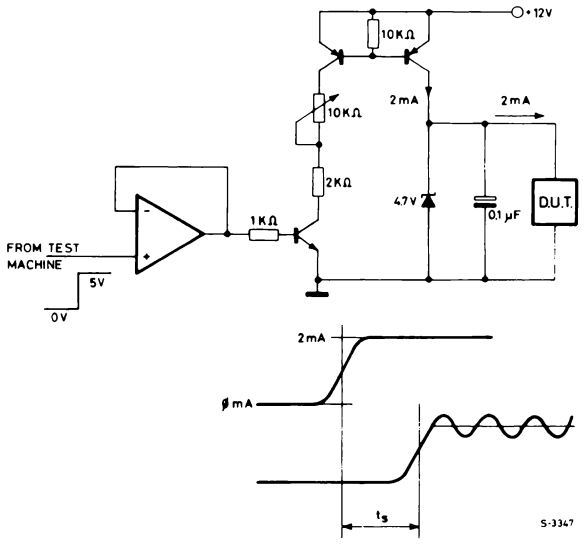
2 : The value of the alternative output component (VLF, VHF) at two different conditions of supply voltages can be related as follows:

$$V_{LF'(HF)}\ (mVpp) = V_{LF\ (HF)}\ (mVpp)\ \frac{V_{DD'}}{V_{DD}}$$

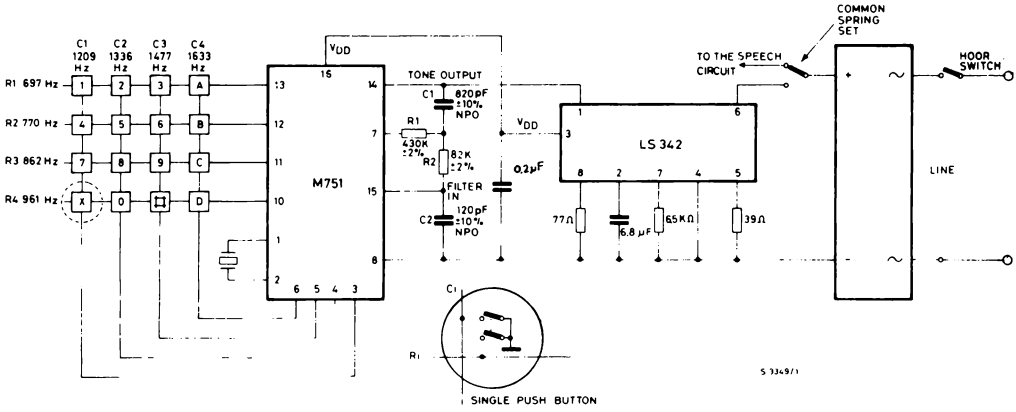
3 : The value of the continuous output component (V_{DC}) at two different conditions of supply voltages can be related as follows:

$$V_{DC'}\ (V) = V_{DC}\ (V)\ \frac{V_{DD'}}{V_{DD}}$$

TEST CIRCUIT AND START UP TIME DEFINITION



APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUIT

M 752

PRELIMINARY DATA

16 STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABEL
- MOTOR DRIVE BRIDGE CONFIGURATION OUTPUT

The M752 (standard temperature range) is a 16 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose seven adjustment terminals are provided on the M752: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. With an oscillator frequency of 4.194812 MHz the bridge configuration outputs supply two symmetrical square wave signals whose frequency is 64 Hz; duty cycle is 50% and their relative delay is of half period. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 16. If one or more adjustment terminals are grounded (taken to pin 14), the output frequency decreases. If all adjustment terminals are grounded, the output frequency is reduced by 242 ppm. The by-four-divided oscillator frequency may be checked at a separate test output (pin 9) non-reactive with respect to the oscillator. Based on this check the output frequency and consequently the accuracy of the clock may be adjustable at the terminals 2 . . . 8 by means of the variable frequency divider. The device is available in 16 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.3 to +17	V
I_{12}, I_{13}	Output current	30	mA
P_{tot}	Power dissipation at T_{amb} = 25°C	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

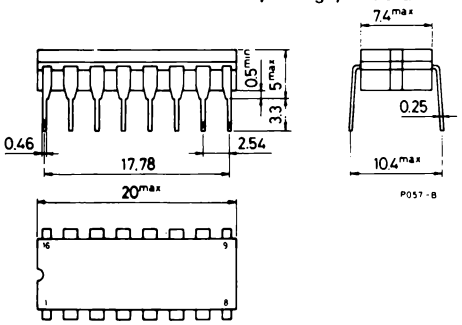
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are referred to V_{SS} pin voltage.

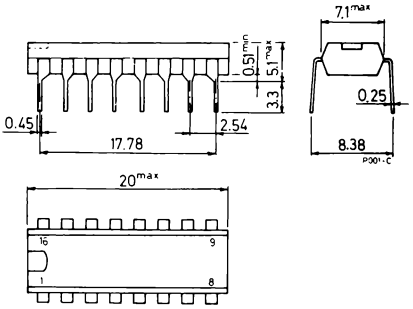
ORDERING NUMBERS: M752 B1 for dual in-line plastic package
M752 D1 for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimension in mm)

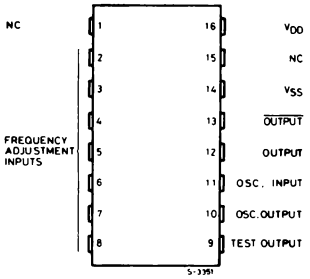
For dual in-line ceramic package, frit seal



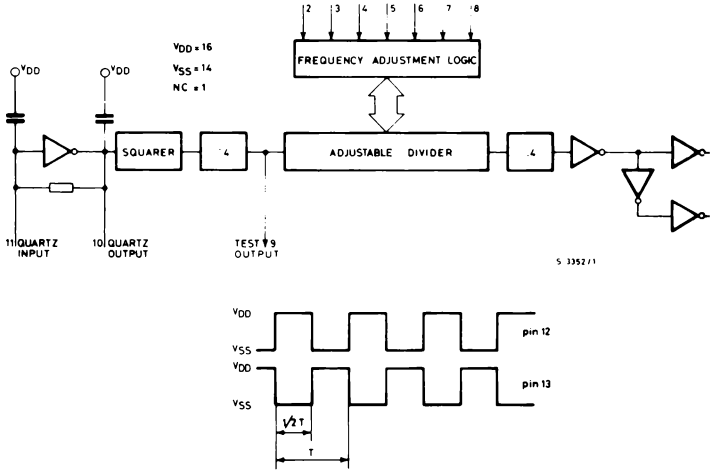
For dual in-line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
V_{DD}	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
R_L	Output load resistance between pins 12 and 13	1	KΩ
T_{op}	Operating temperature	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output high voltage	I_{OH}= 0		6	5.99			5.99	6		5.95			V
				12	11.99			11.99	12		11.95			
V_{OL}	Output low voltage	I_{OL}= 0		6			0.01		0	0.01			0.05	V
				12			0.01		0	0.01			0.05	
I_{DN}	Output drive current N-channel	pin 12-13	2	6	10.5			10	12.5		6.5			mA
			2	12	17			16.5	20		6.5			
I_{DP}	Output drive current P-channel	pin 12-13	4	6	-10.5			-10	-12.5		-6.5			mA
			10	12	-17			-16.5	-20		-6.5			
I_{ON}	Current consumption	I_O= 0*		12					3					mA

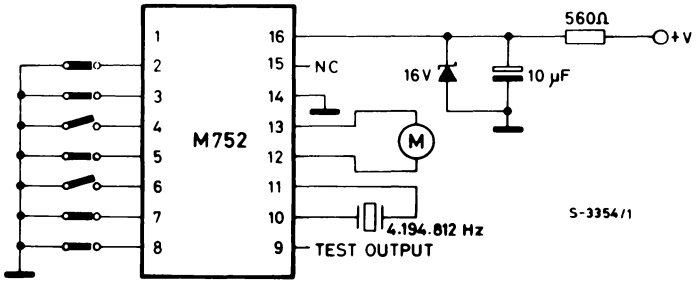
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter		Test conditions		Values						Unit
			V_{DD} (V)	M752 D1			M752 B1			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
f_T	Frequency test output		12		1.048703			1.048703		Hz
f_o **	Output frequency		12		64			64		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment		12		± 121			± 121		ppm
R_o	Total bridge output resistance	R_L= 300Ω	6			300			300	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUIT

M 754

PRELIMINARY DATA

23 STAGE COUNTER WITH INTERMEDIATE OUTPUT AT THE 16th STAGE

- LOW QUIESCENT POWER DISSIPATION
- 25% OUTPUT PULSE DUTY CYCLE
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABLE
- MOTOR DRIVER BRIDGE CONFIGURATION OUTPUT

The M754 (standard temperature range) is a 23 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose seven adjustment terminals are provided on the M754; they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 16. If one or more adjustment terminals are grounded (taken to pin 14), the output frequency decreases. With an oscillator frequency of 4.194812 MHz the bridge configuration outputs supply two square wave signals whose frequency is 0.5 Hz; the pulse duty factor is 0.25 and their relative delay is of half period. The intermediate output provides a 64 Hz signal with pulse duty cycle of 50%. The by-four-divider oscillator frequency may be checked at a separate test output (pin 9) non-reactive with respect to the oscillator. The device is available in 16 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.3 to +17	V
I_{12}, I_{13}	Output current	30	mA
P_{tot}	Power dissipation at T_{amb} = 25°C	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

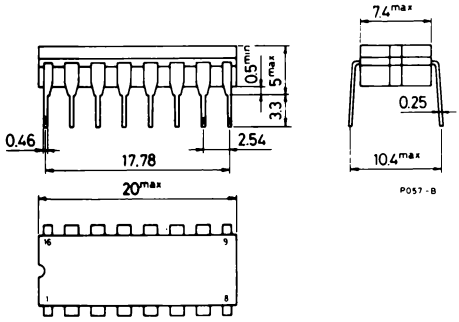
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are referred to V_{SS} pin voltage.

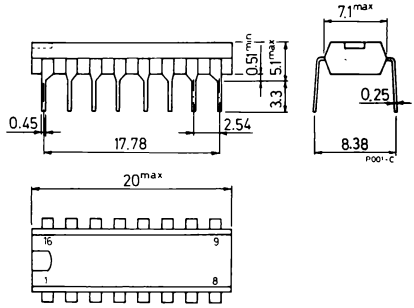
ORDERING NUMBERS: M754 B1 for dual in-line plastic package
M754 D1 for dual in-line ceramic package frit seal

MECHANICAL DATA (dimension in mm)

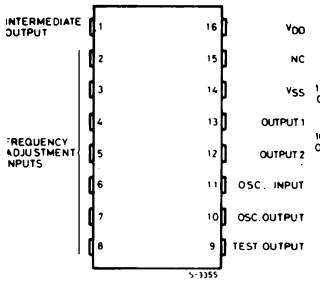
For dual in-line ceramic package, frit seal



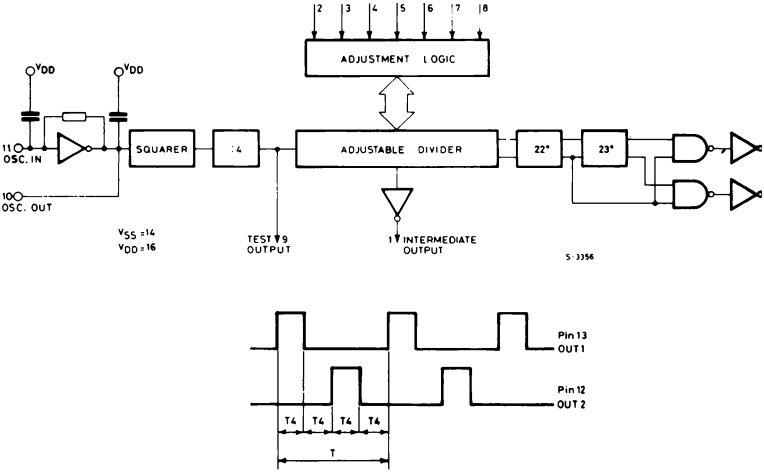
For dual in--line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
R_L	Output load resistance between pins 12 and 13	300	Ω
T_{op}	Operating temperature range	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions	V_O (V)	V_{DD} (V)	Values -40°C Min.	-40°C Typ.	-40°C Max.	25°C Min.	25°C Typ.	25°C Max.	85°C Min.	85°C Typ.	85°C Max.	Unit
V_{OH}	Output high voltage	I_{OH}= 0		6	5.99			5.99	6		5.95			V
				12	11.99			11.99	12		11.95			
V_{OL}	Output low voltage	I_{OL}= 0		6			0.01		0	0.01			0.05	V
				12			0.01		0	0.01			0.05	
I_{DN}	Output drive current P-channel	pin 12-13	2	6	10.5			10	12.5		6.5			mA
			2	12	17			16.5	20		6.5			
I_{DP}	Output drive current N-channel	pin 12-13	4	6	-10.5			-10	-12.5		-6.5			mA
			10	12	-17			-16.5	-20		-6.5			
I_{ON}	Current consumption	I_O= 0*		12					3					mA

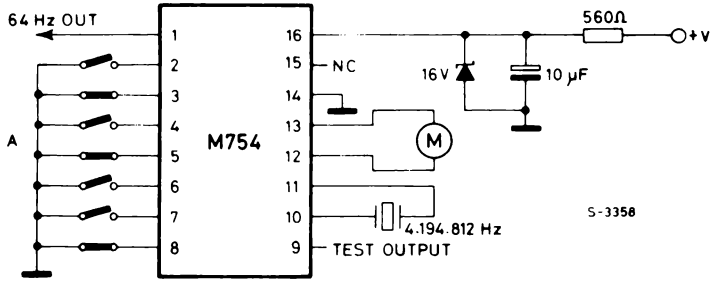
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter		Test conditions	V_{DD} (V)	Values M754 D1 Min.	M754 D1 Typ.	M754 D1 Max.	M754 B1 Min.	M754 B1 Typ.	M754 B1 Max.	Unit
f_T	Frequency test output		12		1.048703			1.048703		Hz
f_o**	Output frequency		12		0.5			0.5		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment		12		± 121			± 121		ppm
R_o	Total bridge output resistance	R_L= 300Ω	6			300			300	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUIT

M 1024

30-CHANNEL REMOTE CONTROL TRANSMITTER

- LOW POWER DISSIPATION IN TRANSMISSION
- QUASI-ZERO STAND-BY CURRENT
- WIDE SUPPLY VOLTAGE RANGE
- INPUTS FULLY PROTECTED
- HIGH NOISE IMMUNITY
- INTERLOCK PREVENTS INCORRECT SELECTION

The M 1024 is a monolithic integrated circuit intended for remote controlled systems in which 30 different ultrasonic frequencies are used to transmit 30 commands.
The M 1024 comprises an oscillator circuit, a variable and a fixed frequency divider, a decoder and a command error protection. The circuit is produced in COS/MOS technology. In conjunction with the ultrasonic Receiver M 1025 a complete remote control system can be realized. The device is available in a 16-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to 12	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
$\|I_O\|$	Output current	10	mA
P_{tot}	Total power dissipation	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	-25 to 70	°C

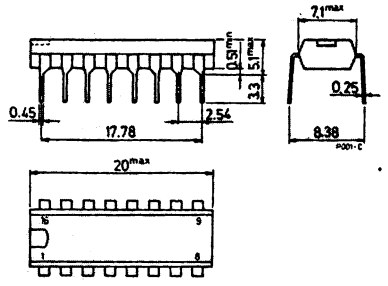
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages value are referred to V_{SS} pin voltage.

ORDERING NUMBER: M 1024 B5

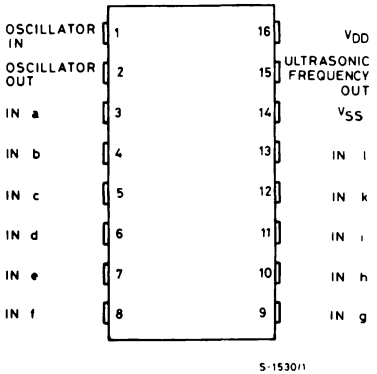
MECHANICAL DATA

Dimensions in mm

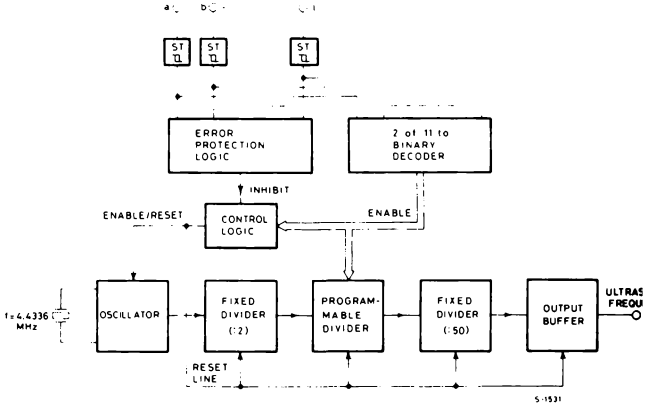


M 1024

PIN CONNECTIONS



BLOCK DIAGRAM



TRUTH TABLE (f_i = 4.4336 MHz)

Channel Number	Inputs											Output Frequency
	a	b	c	d	e	f	g	h	i	k	l	
1	H	H	H	H	L	H	H	L	H	H	H	33 945 Hz
2	H	H	H	H	L	H	H	H	H	H	L	34 291 Hz
3	H	H	H	H	L	H	L	H	H	H	H	34 638 Hz
4	H	H	H	H	L	H	H	H	H	L	H	34 984 Hz
5	H	H	H	H	L	L	H	H	H	H	H	35 330 Hz
6	H	H	H	H	L	H	H	H	L	H	H	35 677 Hz
7	L	H	H	H	H	L	H	H	H	H	H	36 023 Hz
8	L	H	H	H	H	H	H	H	L	H	H	36 370 Hz
9	H	L	H	H	H	L	H	H	H	H	H	36 716 Hz
10	H	L	H	H	H	H	H	H	L	H	H	37 062 Hz
11	H	H	L	H	H	L	H	H	H	H	H	37 409 Hz
12	H	H	L	H	H	H	H	H	L	H	H	37 755 Hz
13	H	H	H	L	H	L	H	H	H	H	H	38 101 Hz
14	H	H	H	L	H	H	H	H	L	H	H	38 448 Hz
15	L	H	H	H	H	H	L	H	H	H	H	38 794 Hz
16	L	H	H	H	H	H	H	H	H	L	H	39 141 Hz
17	H	L	H	H	H	H	L	H	H	H	H	39 487 Hz
18	H	L	H	H	H	H	H	H	H	L	H	39 833 Hz
19	H	H	L	H	H	H	L	H	H	H	H	40 180 Hz
20	H	H	L	H	H	H	H	H	H	L	H	40 526 Hz
21	H	H	H	L	H	H	L	H	H	H	H	40 872 Hz
22	H	H	H	L	H	H	H	H	H	L	H	41 219 Hz
23	L	H	H	H	H	H	H	L	H	H	H	41 565 Hz
24	L	H	H	H	H	H	H	H	H	H	L	41 912 Hz
25	H	L	H	H	H	H	H	L	H	H	H	42 258 Hz
26	H	L	H	H	H	H	H	H	H	H	L	42 604 Hz
27	H	H	L	H	H	H	H	L	H	H	H	42 951 Hz
28	H	H	L	H	H	H	H	H	H	H	L	43 297 Hz
29	H	H	H	L	H	H	H	L	H	H	H	43 643 Hz
30	H	H	H	L	H	H	H	H	H	H	L	43 990 Hz

DESCRIPTION

The truth table shows the 30 ultrasonic transmission frequencies used in the wireless transmission of remote control commands to the receiver. These frequencies are derived from the frequency of a quartz controlled oscillator with the aid of a variable frequency divider operating on the blaking principle. This is accomplished by blanking out between 1 and 30 out of every 128 pulses of the oscillator frequency (4.4336 MHz). The variable divider is preceded by a flip flop which halves the quartz frequency. The variable divider is followed by a fixed divider which divides by 50. It reduces the jitter, which is unavoidable when using the blanking principle, to negligible values. The expression for the ultrasonic output frequency is

$$f_o = \frac{f_i\,(97 + N)}{12\,800}$$

wherein N is the channel number and f_i = 4.4336 MHz (sub-carrier frequency). The space between two adiacent ultrasonic frequencies is 346.4 Hz.

The inputs accept a 2 of 11 code: by connecting simultaneously to V_{SS} one of a to e and one of f to l input, a 5 bit word is generated internally and applied to the variable divider. The relative frequency is thus available at the output.

An error protection circuit prevents incorrect operation. Under these conditions the oscillator will not start to operate, and the frequency divider is held in a defined position.

Since consumption under standby conditions is very low, the ultrasonic transmitter need never be switched off. The selected frequency appears at the output when the threshold voltage is exceeded at the two control inputs. A threshold voltage hysteresis ensures that AC voltages which may be superimposed on the input voltage cannot falsify the actuation.

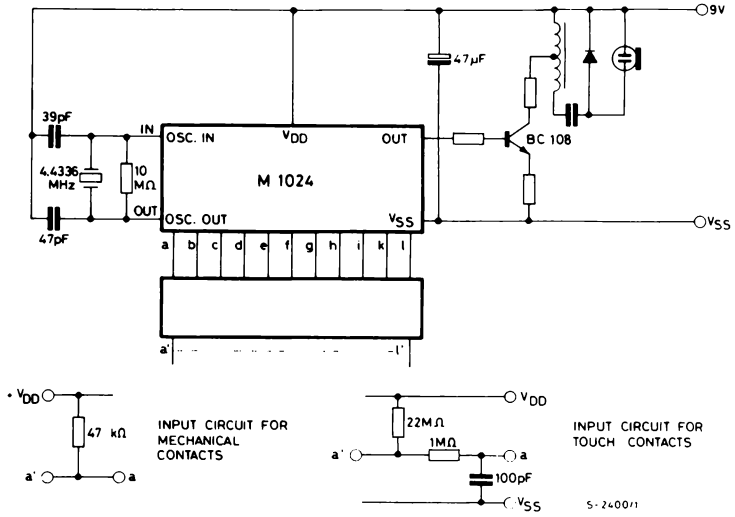
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	7 to 9	V
V_I	Input voltage	0 to V_{DD}	V
f_i	Oscillator frequency	4.4336	MHz
T_{op}	Operating temperature	-25 to 70	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions	Values at 25°C			Unit
			Min.	Typ.	Max.	
I_{CCL}	Quiescent supply current	V_{DD}= 9V all inputs at V_{DD}		2	10	µA
I_{CC}	Supply current	V_{DD}= 9V - oscillator running - ultrasonic freq. output open		1.5	3	mA
I_I	Input current	V_{DD}= 9V V_I= 0 ÷ V_{DD}		|0.01|	|1|	µA
r_{on}	High level output resistance (on state)	V_{DD}= 7V I_{OH}= -1 mA		0.5	1	kΩ
r_{on}	Low level output resistance (on state)	V_{DD}= 7N I_{OL}= 0.2 mA		1.5	3	kΩ
V_{TLH}	Positive going threshold voltage at the inputs a to l	V_{DD}= 9V		4.5		V
V_{THL}	Negative going threshold voltage at the inputs a to l	V_{DD}= 9V		4.1		V

TYPICAL APPLICATION



INPUT CIRCUIT FOR MECHANICAL CONTACTS

INPUT CIRCUIT FOR TOUCH CONTACTS

S-2400/1

MOS INTEGRATED CIRCUIT

M 1025

30-CHANNEL REMOTE CONTROL RECEIVER

- 3 ANALOG OUTPUT SIGNALS
- 5 BINARY-CODED INPUT/OUTPUT LINES
- MAINS SWITCH OUTPUT
- MUTING FUNCTION
- NORMALIZATION OF ANALOG SIGNALS
- STORAGE AVAILABILITY OF ANALOG SIGNALS

The M 1025 is a monolithic integrated circuit intended for a remote-controlled system in which 30 different ultrasonic frequencies are used to transmit 30 control commands. The recommended transmitters are the M 1024 or the M 1124. The M 1025 measures the frequency of the arriving signal by counting the cycles during a fixed measuring time determined by a 4.433 MHz quartz crystal. All ultrasonic commands are converted into a coded 5-bit output signal and issued in pulsed form on 5 parallel lines. Nine of the thirty commands are memorized and used inside the M 1025; they can also be selected directly by a 5-bit word applied to the input/output binary lines (A to E). The further 21 commands are for free application; different TV channels are selectable if a decoder is connected to the outputs. Six of the nine memorized commands give output signals for controlling three analog values, e.g. volume, brightness and colour saturation. These signals are continuously delivered in square waveform; the duty cycle can be varied so determining the level of the analog value. Even when the mains voltage is not available, the latest analog value may be stored with a minimum of power by means of a battery or accumulator. The M 1025 is constructed in low-threshold P-channel silicon gate technology and is supplied in a 16-lead dual in-line plastic package with copper insert. Three different types are available, CA, CB, CAZ, which differ as specified in the table below.

Type	MAINS ON by commands (see truth table for the definition of N)
CA	N = 1 and N = 15 to 30 (program selection)
CB	N = 15 to 30 (program selection)
CAZ	N = 1

ABSOLUTE MAXIMUM RATINGS*

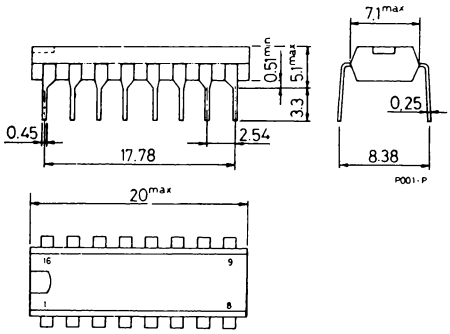
V_{DD}, V_{DDI}**	Supply voltages	-20 to 0.3	V
V_I	Input voltage	-20 to 0.3	V
I_O	Output current (pins 2, 3, 4, 6, 7, 8, 9, 11, 12)	$\|5\|$	mA
P_{tot}	Total package power dissipation	1	W
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	-25 to 70	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

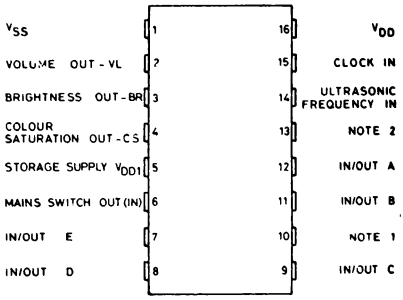
** All voltages values are refered to V_{SS} pin voltage.

ORDERING NUMBERS: M 1025 B5 CA
M 1025 B5 CB
M 1025 B5 CAZ

MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS

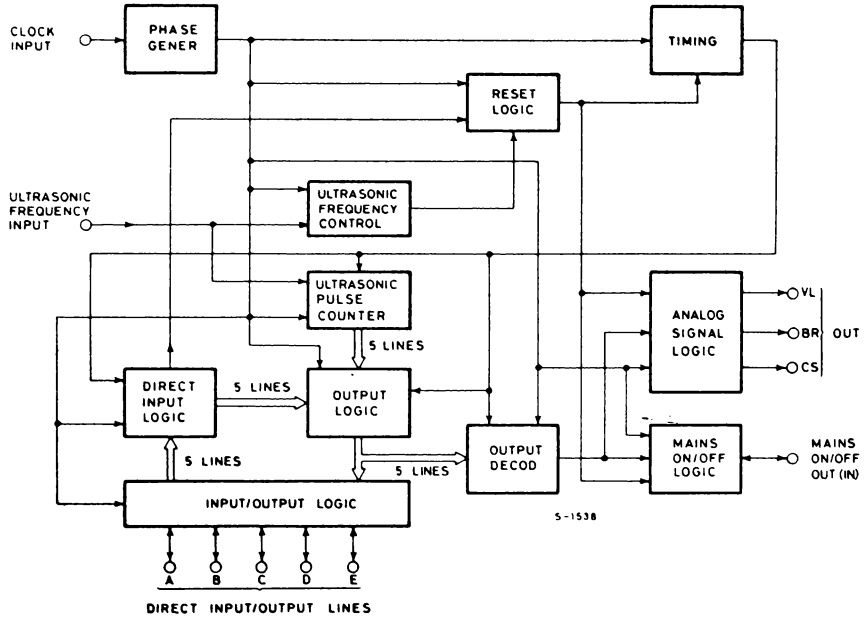


NOTE 1: THIS PIN MUST BE LEFT OPEN OR CONNECTED TO V_{SS}

NOTE 2: THIS PIN MUST BE LEFT OPEN

S-1537

BLOCK DIAGRAM



TRUTH TABLE (Clock frequency, f = 4.4336 MHz)

N	Ultrasonic Frequency	Command	Code				
			E	A	B	C	D
1	33 945 Hz	CA, CAZ types: MAINS ON/OFF** / CB type: MAINS OFF**	H	L	H	H	H
2	34 291 Hz	MUTING ON/OFF	L	L	H	H	H
3	34 638 Hz	Colour saturation (CS)+	H	H	L	H	H
4	34 984 Hz	Normalisation (*)	L	H	L	H	H
5	35 330 Hz	Colour saturation (CS) –	H	L	L	H	H
6	35 677 Hz	S1	L	L	L	H	H
7	36 023 Hz	Brightness (BR)+	H	H	H	L	H
8	36 370 Hz	S2	L	H	H	L	H
9	36 716 Hz	Brightness (BR) –	H	L	H	L	H
10	37 062 Hz	S3	L	L	H	L	H
11	37 409 Hz	Volume (VL) +; MUTING OFF	H	H	L	L	H
12	37 755 Hz	S4	L	H	L	L	H
13	38 101 Hz	Volume (VL) –	H	L	L	L	H
14	38 448 Hz	S5	L	L	L	L	H
15	38 794 Hz	Program 1	H	H	H	H	L
16	39 141 Hz	Program 2	L	H	H	H	L
17	39 487 Hz	Program 3	H	L	H	H	L
18	39 833 Hz	Program 4	L	L	H	H	L
19	40 180 Hz	Program 5	H	H	L	H	L
20	40 526 Hz	Program 6	L	H	L	H	L
21	40 872 Hz	Program 7	H	L	L	H	L
22	41 219 Hz	Program 8	L	L	L	H	L
23	41 565 Hz	Program 9	H	H	H	L	L
24	41 912 Hz	Program 10	L	H	H	L	L
25	42 258 Hz	Program 11	H	L	H	L	L
26	42 604 Hz	Program 12	L	L	H	L	L
27	42 951 Hz	Program 13	H	H	L	L	L
28	43 297 Hz	Program 14	L	H	L	L	L
29	43 643 Hz	Program 15	H	L	L	L	L
30	43 990 Hz	Program 16	L	L	L	L	L

CA, CB types: all these commands act also as MAINS ON**

S1 to S5 are additional commands.

* The Normalisation command sets the colour saturation to a pulse duty cycle of 16/31 and the brightness to a pulse duty cycle of 18/31; this command has no effect on volume, unless MUTING has been inserted: in this case the volume is restored, without changing the duty cycle.

** If MUTING has been commanded, each MAINS OFF or MAINS ON command also acts on MUTING to restore the previous volume level.

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	-18 ± 1	V
V_{DD1}	Storage supply voltage: - D/A signal storing	-10 to V_{DD}	V
	- No storing	0	V
V_I	Input voltage	0 to V_{DD}	V
f_i	Input clock frequency	4.4336	MHz
T_{op}	Operating temperature	-25 to 70	°C
t_r	Supply voltage rise time	max 100	ms
I_o	Output current (pins 2-3-4-6-7-8-9-11-12)	max |2.5|	mA

STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)
(Typical values are at T_{amb} = 25°C)

	Parameter	Test conditions and notes	Values			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply current	V_{DD} = -19V		22	35	mA
I_{DD1}	Storage supply current	V_{DD1} = -19V		0.2		mA
r_{on}	Output resistance (on state) pins 2, 3, 4, 6	V_{DD} = -18V, R_L = 2 kΩ			1	kΩ
r_{on}	Output resistance (on state) pins 7, 8, 9, 11, 12	V_{DD} = -18V, R_L = 3.9 kΩ			5	kΩ

DIRECT INPUTS (7, 8, 9, 11, 12, 6)

V_{IH}	High level input voltage		-1		V_{SS}	V
V_{IL}	Low level input voltage		V_{DD}		-4	V

CLOCK INPUT (pin 15)

V_{IPP}	Input peak to peak voltage swing (sinusoidal)	Signal applied without DC voltage	4		8	V

ULTRASONIC FREQUENCY INPUT (pin 14)

V_{IPP}	Input peak to peak voltage swing	Signal applied without DC voltage	500		V_{DD}	mV

DYNAMIC ELECTRICAL CHARACTERISTICS (Clock frequency f = 4.4336 MHz)

	Parameter	Min.	Typ.	Max.	Unit
t_1	Ultrasonic input acceptance time (except MAINS and MUTING commands)		115.5		ms
t_2	Ultrasonic input acceptance time (for MAINS and MUTING commands)		669.8		ms
t_3	Direct inputs acceptance time (except MAINS and MUTING commands)		69.3		ms
t_4	Direct inputs acceptance time (for MAINS and MUTING commands)		600.6		ms
t_5	Output activation delay (including acceptance time) for all commands except MAINS and MUTING		115.5		ms
t_6	Output activation delay (including acceptance time) for MAINS and MUTING commands		669.8		ms
t_7	Analog-output step to step response time		184.8		ms
t_8	MAINS OFF to ON acceptance time plus activation time from MAINS input-output	10			µs
f	Analog-output frequency		8.9		kHz
D	Analog-output frequency duty-cycle	1/31		30/31	–

DESCRIPTION

The function of the M 1025 is explained by reference to the various pins as follows:

Pin 1 - V_{SS}

The substrate of the integrated circuit is connected to this pin. It is the reference point for all voltage parameters of the device, and is to be connected to the highest potential of the supply voltage.
Examples: V_{SS}= 0V V_{DD}= -18V or V_{SS}= +18V V_{DD}= 0V

Pin 5 - V_{DD1} storage supply voltage

If the last-stored D/A information is to be preserved when the mains plug has been disconnected, -10V at least should be fed to pin 5. The current consumption of the memory is typically 0.2 mA. The voltage V_{DD1} should be applied before $|V_{DD}|$ falls below 16V. If the storing function is not required, V_{DD1} has to be connected to V_{SS}: in this case, when V_{DD} is applied, the analog control signals are set at the normalized position.

Pin 14 - Ultrasonic frequency input

The amplified ultrasonic signals of 500 mV peak to peak at minimum are applied to this pin via a capacitor to remove DC voltage. The input waveform must be present for more then 115.5 ms to allow the command to be accepted. Exceptions are the MAINS and MUTING commands which have a 669.8 ms acceptance time. Internal control logic suppresses input frequencies greater than 55.4 kHz and lower than 27.7 kHz. Due to the recognition system, the ultrasonic transmission frequency of 33.9 kHz may fluctuate by ± 0.51% and the frequency of 44.0 kHz by ± 0.39% without causing errors.

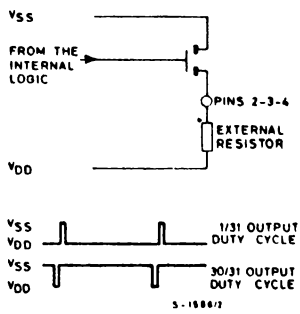
Pin 15 - Clock input

The clock input has to be connected via a capacitor to a 4.4336 MHz quartz controlled oscillator, whose output peak to peak voltage has to be comprised between 4 and 8V.

Pins 2 - 3 - 4 - D/A outputs

The outputs CS (colour saturation), BR (brightness) and VL (volume) are the drain of the output transistors. A square wave output voltage is produced when resistors are inserted between the outputs and V_{DD}. The frequency of these square waves is 8.93 kHz. The pulse duty cycle is variable in 30 steps between 1/31 and 30/31 (see fig. 1). 115.5 ms after the onset of an ultrasonic or direct binary command, the pulse duty cycle is advanced by one step. In the case of a continuous command, further advances follow at intervals of 184.8 ms until the final value is reached. The time needed to make the entire variation is 5.543 seconds. When the supply voltage is applied, with V_{DD1}= 0, the D/A outputs are normalized with the following pulse duty cycles: output colour saturation = 16/31; output brightness = 18/31; output volume = 10/31; if V_{DD1} pin has been maintained at its correct voltage, the last stored information is preserved. The command N = 2 switches on or off, the VL output transistor, with a delay time of 669.8 ms acting as a sound ON/OFF-switch. The command N = 4 (normalisation) sets outputs CS and BR to a pulse duty cycle of 16/31 and 18/31, but this command has no effect on the output VL, unless MUTING has been previously commanded. In this case the command N=4 restores the volume. If the MUTING has been commanded, the volume can also be restored with the command VL+, provided that the circuit is not in the stand-by position. In any case the MUTING command is cancelled by a MAINS ON or OFF command.

Fig. 1

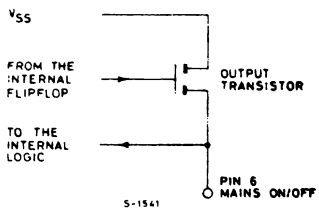


DESCRIPTION (continued)

Pin 6 - MAINS ON/OFF output/input

For the purpose of switching the TV set ON or OFF ultrasonically, the input signal must be present at least for 669.8 ms. Thereafter the mains flip flop toggles, controlling an open drain transistor (see fig. 2). After power supply is applied, the mains flip flop is set independently of V_{DD1} so that the output transistor is off. When the output transistor is off, the D/A-converters are locked, i.e. the output signals at pins 2,3 and 4 cannot be varied. With M 1025 CA type, switching ON can be obtained either by selecting one of the 16 stations or by the power ON/OFF command. With M 1025 CB type, switching ON can be achieved only by using one of the 16 station control commands; with M 1025 CAZ type, only by the Power ON/OFF command. In all types, switching ON can also be obtained connecting pin 6 to V_{SS} for at least 10 μs and switching OFF is obtained only by the command N = 1 (see truth table).

Fig. 2



Pins 7 - 8 - 9 - 11 - 12 - Direct input/output lines

These pins serve as inputs for commands on the TV set and, also as outputs for ultrasonic transmitted commands. Fig. 3 shows the input/output stage of one line of the circuit. The commands may be introduced directly in the form of a 5-bit word applied to the Input/Output lines A, B, C, D and E. An input signal is only recognized as valid if it exceeds the threshold voltage at least once in each of three successive 23.1 ms periods, for at least 10 μs. When this happens, an output pulse of 23.1 ms duration is generated after a processing time of 46.2 ms. (Total delay time 115.5 ms). In the case of MAINS ON/OFF and MUTING input commands the acceptance time is 600.6 ms; the output pulse will appear with a delay of 69.3 ms after the acceptance time (total delay time 669.8 ms). Evidently the output signals act on the inputs again, but this does not cause interferences because the inputs are locked while an output signal is available. If commands are issued either from the remote control or locally to the television set, the local command will always override the remote command.

Fig. 3

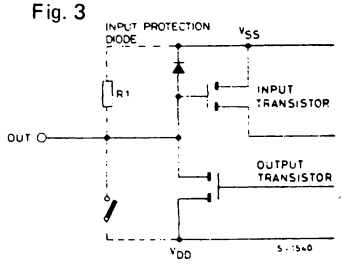
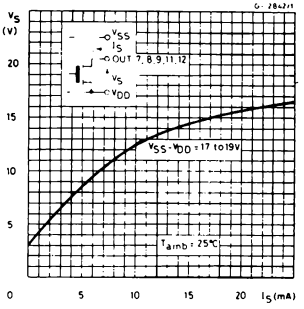


Fig. 4 - Typical output characteristics of the open source transistor at pins 7,8,9,11,12



COS/MOS INTEGRATED CIRCUIT

M 1124

30-CHANNEL REMOTE CONTROL TRANSMITTER

- FEW EXTERNAL COMPONENTS
- INTERLOCK PREVENTS INCORRECT SELECTION
- QUASI-ZERO STAND-BY CURRENT
- WIDE SUPPLY VOLTAGE RANGE
- INPUTS FULLY PROTECTED

The M 1124 is a monolithic integrated circuit intended for remote controlled systems in which 30 different ultrasonic frequencies are used to transmit 30 commands.
The M 1124 comprises on oscillator circuit which does not require external components except the quartz. Further it comprises a fixed and a variable frequency divider, a decoder and a command error protection. All the command inputs are pulled-up to V_{DD} by integrated resistors, to reduce the number of external components. Due to the relative low input impedances, the M 1124 is not suited for touch contacts. The circuit is produced in COS/MOS technology. In conjunction with the ultrasonic receivers M 1025 or M 1130, a complete remote control system can be realized. The device is available in a 16-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to	12	V
V_I	Input voltage	-0.5 to V_{DD}	+0.5	V
$\|I_O\|$	Output current		10	mA
P_{tot}	Total power dissipation		200	mW
T_{stg}	Storage temperature	-65 to	150	°C
T_{op}	Operating temperature	0 to	70	°C

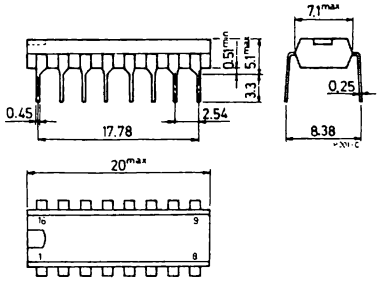
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicate in the "Recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

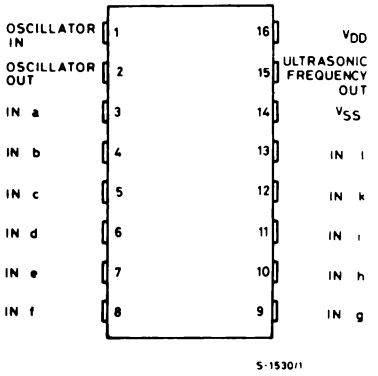
ORDERING NUMBER: M 1024 B1

MECHANICAL DATA

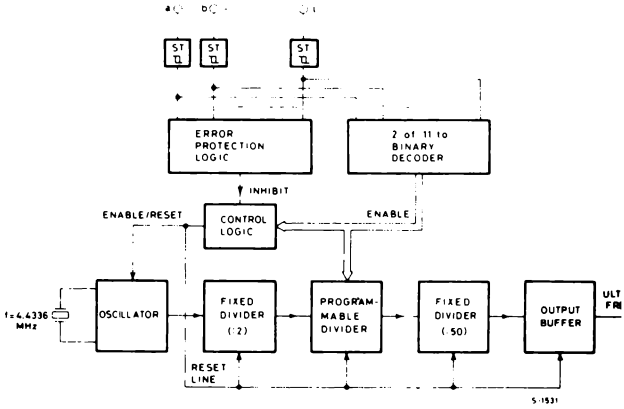
Dimensions in mm



PIN CONNECTIONS



BLOCK DIAGRAM



TRUTH TABLE (f_i = 4.4336 MHz)

Channel Number	Inputs											Output Frequency
	a	b	c	d	e	f	g	h	i	k	l	
1	H	H	H	H	L	H	H	L	H	H	H	33 945 Hz
2	H	H	H	H	L	H	H	H	H	H	L	34 291 Hz
3	H	H	H	H	L	H	L	H	H	H	H	34 638 Hz
4	H	H	H	H	L	H	H	H	H	L	H	34 984 Hz
5	H	H	H	H	L	L	H	H	H	H	H	35 330 Hz
6	H	H	H	H	L	H	H	H	L	H	H	35 677 Hz
7	L	H	H	H	H	L	H	H	H	H	H	36 023 Hz
8	L	H	H	H	H	H	H	H	L	H	H	36 370 Hz
9	H	L	H	H	H	L	H	H	H	H	H	36 716 Hz
10	H	L	H	H	H	H	H	H	L	H	H	37 062 Hz
11	H	H	L	H	H	L	H	H	H	H	H	37 409 Hz
12	H	H	L	H	H	H	H	H	L	H	H	37 755 Hz
13	H	H	H	L	H	L	H	H	H	H	H	38 101 Hz
14	H	H	H	L	H	H	H	H	L	H	H	38 448 Hz
15	L	H	H	H	H	H	L	H	H	H	H	38 794 Hz
16	L	H	H	H	H	H	H	H	H	L	H	39 141 Hz
17	H	L	H	H	H	H	L	H	H	H	H	39 487 Hz
18	H	L	H	H	H	H	H	H	H	L	H	39 833 Hz
19	H	H	L	H	H	H	L	H	H	H	H	40 180 Hz
20	H	H	L	H	H	H	H	H	H	L	H	40 526 Hz
21	H	H	H	L	H	H	L	H	H	H	H	40 872 Hz
22	H	H	H	L	H	H	H	H	H	L	H	41 219 Hz
23	L	H	H	H	H	H	H	L	H	H	H	41 565 Hz
24	L	H	H	H	H	H	H	H	H	H	L	41 912 Hz
25	H	L	H	H	H	H	H	L	H	H	H	42 258 Hz
26	H	L	H	H	H	H	H	H	H	H	L	42 604 Hz
27	H	H	L	H	H	H	H	L	H	H	H	42 951 Hz
28	H	H	L	H	H	H	H	H	H	H	L	43 297 Hz
29	H	H	H	L	H	H	H	L	H	H	H	43 643 Hz
30	H	H	H	L	H	H	H	H	H	H	L	43 990 Hz

DESCRIPTION

The truth table shows the 30 ultrasonic transmission frequencies used in the wireless transmission of remote control commands to the receiver. These frequencies are derived from the frequency of a quartz controlled oscillator with the aid of a variable frequency divider operating on the blanking principle. This is accomplished by blanking out between 1 to 30 out of every 128 pulses of the oscillator frequency (4.4336 MHz) divided by 2.

The variable divider is followed by a fixed divider which divides by 50. It reduces the jitter, which is unavoidable when using the blanking principle, to negligible values. The expression for the ultrasonic output frequency is

$$f_o = \frac{f_i\,(97 + N)}{12\,800}$$

wherein N is the channel number and f_i = 4.4336 MHz (sub-carrier frequency). The space between two adjacent ultrasonic frequencies is 346.4 Hz.

The inputs accept a 2 of 11 code: by connecting simultaneously to V_{SS} one of a to e and one of f to l input, a 5 bit word is generated internally and applied to the variable divider. The relative frequency is thus available at the output.

An error protection circuit prevents incorrect operation. Under these conditions the oscillator will not start to operate, and the frequency divider is held in a defined position.

Since consumption under standby conditions is very low, the ultrasonic transmitter need never be switched off. The selected frequency appears at the output when the threshold voltage is exceeded at the two control inputs.

RECOMMENDED OPERATING CONDITIONS

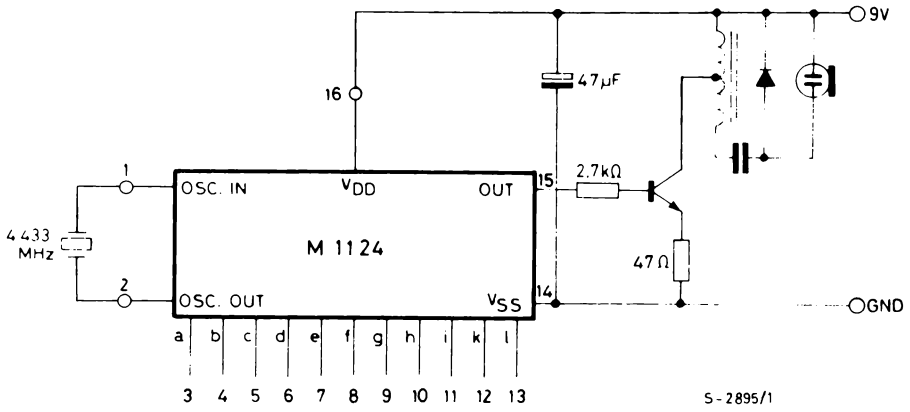
V_{DD}	Supply voltage	6 to 9	V
V_I	Input voltage	0 to V_{DD}	V
f_p	Parallel resonance frequency of the quartz at C_L = 10 pF	4.433	MHz
r_S	Series resistance of the quartz at CL= 10 pF	< 200	Ω
T_{op}	Operating temperature	0 to 70	°C

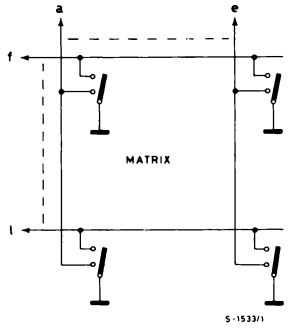
STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at T_{amb} = 25°C, unless otherwise specified.

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{DDL}	Quiescent supply current	All inputs at V_{DD}		2	10	µA
I_{DD}	Supply current	V_{DD} = 9 V - oscillator running - ultrasonic freq. output open		1.5	3	mA
I_I	Input current	V_I = 0		-20		µA
r_{on}	High level output resistance (on state)	I_{OH} = -1 mA		0.5	1	kΩ
r_{on}	Low level output resistance (on state)	I_{OL} = 0.2 mA		1.5	3	kΩ
V_{TH}	Threshold voltage of the control inputs			4.1		V

TYPICAL APPLICATION





MOS INTEGRATED CIRCUIT

M 1130

30-CHANNEL REMOTE CONTROL RECEIVER

- PROGRAM MEMORY OUTPUTS
- INTEGRATED CLOCK OSCILLATOR
- SEQUENTIAL PROGRAM CHANGE COMMAND
- 5 BINARY CODED INPUT/OUTPUT LINES

The M 1130 is a monolithic integrated circuit intended for a remote-controlled system in which 30 different ultrasonic frequencies are used to transmit 30 control commands. Both the M 1024 and the M 1124 can be used as transmitter. The M 1130 measures the frequency of the incoming signal by counting the cycles during a fixed measuring time determined by a 4.4336 MHz quartz crystal. The accepted ultrasonic commands are converted into a coded signal and issued on 5 input/output lines (A to E). The 30 commands can be given not only ultrasonically, but also by applying a 5-bit word to the above mentioned lines. An additional "sequential program change" command is available only on the receiver. Signals to control three analog values, e.g. volume, brightness and colour saturation are internally stored by the M 1130 and continuously delivered in the shape of square wave voltages. The duty cycle of these signals determines the level of the analog value. An output is provided to drive a relay which switches the TV set ON or OFF. The program output lines are provided to drive all the circuits which need a 4-bit binary code such as the H 770/1/2/3 quad analog switches, or the M 193 electronic program memory. The M 1130 is constructed in a low threshold P-channel silicon gate technology and is supplied in an 18-lead dual-in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-20 to 0.3	V
V_I	Input voltage	-20 to 0.3	V
I_O	Output current (pins 2 to 14 and 16)	| 5 |	mA
P_{tot}	Total power dissipation (per package)	800	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

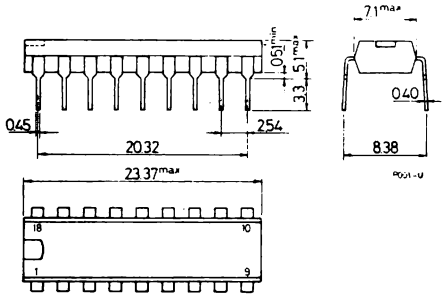
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages values are refered to V_{SS} pin voltage.

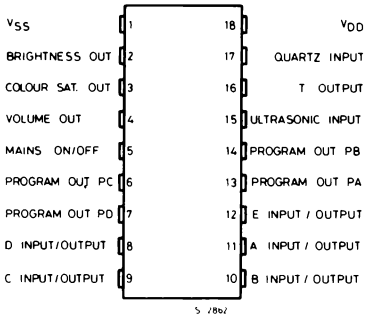
ORDERING NUMBER: M 1130 B1

MECHANICAL DATA

Dimensions in mm



PIN CONNECTIONS



TRUTH TABLES

Table 1 (Clock frequency = 4.4336 MHz)

Channel no.	Ultrasonic frequency (Hz)	Command	Code				
			E	A	B	C	D
–	–	Sequential progr. change - Mains ON	L	H	H	H	H
1	33 945	Mains OFF	H	L	H	H	H
2	34 291	Muting ON/OFF	L	L	H	H	H
3	34 638	Colour saturation +	H	H	L	H	H
4	34 984	Normalisation	L	H	L	H	H
5	35 330	Colour saturation -	H	L	L	H	H
6	35 677	S1	L	L	L	H	H
7	36 023	Brightness +	H	H	H	L	H
8	36 370	S2	L	H	H	L	H
9	36 716	Brightness -	H	L	H	L	H
10	37 062	S3	L	L	H	L	H
11	37 409	Volume + (Muting OFF)	H	H	L	L	H
12	37 755	S4 (Fine tuning –)	L	H	L	L	H
13	38 101	Volume - (Muting OFF)	H	L	L	L	H
14	38 448	S5 (Fine tuning +)	L	L	L	L	H
15	38 794	Program 1	H	H	H	H	L
16	39 141	Program 2	L	H	H	H	L
17	39 487	Program 3	H	L	H	H	L
18	39 833	Program 4	L	L	H	H	L
19	40 180	Program 5	H	H	L	H	L
20	40 526	Program 6	L	H	L	H	L
21	40 872	Program 7	H	L	L	H	L
22	41 219	Program 8 (all these commands act	L	L	L	H	L
23	41 565	Program 9 also as Mains ON)	H	H	H	L	L
24	41 912	Program 10	L	H	H	L	L
25	42 258	Program 11	H	L	H	L	L
26	42 604	Program 12	L	L	H	L	L
27	42 951	Program 13	H	H	L	L	L
28	43 298	Program 14	L	H	L	L	L
29	43 643	Program 15	H	L	L	L	L
30	43 990	Program 16	L	L	L	L	L

Note: S1 to S3 are additional commands.

Table 2: Output code at pins 6, 7, 13, 14

Program no.	PA	PB	PC	PD
1	L	L	L	L
2	H	L	L	L
3	L	H	L	L
4	H	H	L	L
5	L	L	H	L
6	H	L	H	L
7	L	H	H	L
8	H	H	H	L
9	L	L	L	H
10	H	L	L	H
11	L	H	L	H
12	H	H	L	H
13	L	L	H	H
14	H	L	H	H
15	L	H	H	H
16	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	-18 ±1 V
V_I	Input voltage	0 to V_{DD} V
I_O	Output current (pins 2 to 14 and 16)	max |2.5| mA
	Input clock frequency	4.4336 MHz
T_{op}	Operating temperature	0 to 70 °C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at T_{amb} = 25°C)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply current	V_{DD}=-19V		-25		mA
V_{IH}	High level input voltage	pins 8-9-10-11-12	-1		V_{SS}	V
V_{IL}	Low level input voltage		V_{DD}		-4	V
V_{IPP}	Ultrasonic input peak to peak voltage (pin 15)	The signal must be applied without D.C. voltage	500		V_{DD}	mV
V_{OH}	High level output voltage	I_{OH}=-1 mA pins 2 to 7-13-14			V_{SS}-0.6	V

DYNAMIC ELECTRICAL CHARACTERISTICS (Clock frequency = 4.4336 MHz)

	Parameter	Min.	Typ.	Max.	Unit
f	Analog output frequency		17.6		kHz
D	Analog output duty cycle	1/63		62/63	
t_1	Mains ON/OFF command delay time		669.8		ms
t_2	Program stepping delay time with continuous command		692.9		ms
t_3	Analog output delay time with continuous command		138.6		ms
t_{w1}	Pulse width at pin 16 with command 12 (FT-)		21.6		µs
t_{w2}	Pulse width at pin 16 with command 14 (FT +)		23.1		ms

DESCRIPTION

The function of the M 1130 is explained with reference to the various pins as follows:

Pin 1 - V_{SS}

The substrate of the integrated circuit is connected to this pin. It is the reference point for all the voltag parameters of the device and has to be connected to the highest potential of the supply voltage.
Examples: V_{SS}= 0V V_{DD}= -18V
or
V_{SS}= +18V V_{DD}= 0V

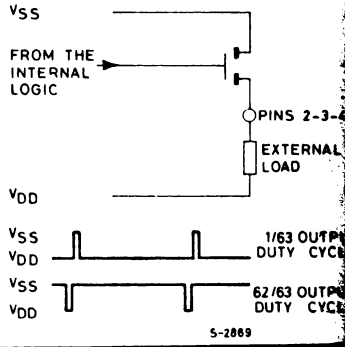
Pin 18 - V_{DD}

Negative pole of the supply voltage.

Pins 2, 3, 4 - D/A Outputs

These outputs are designed to control brightness, colour saturation and volume respectively. A square wave is produced when resistors are inserted between the outputs and V_{DD} (see fig. 1). The frequency o the square wave is about 17.5 kHz, the duty cycle is variable between 1/63 to 62/63. The information i contained in the pulse duty cycle and D.C. voltages are obtained by integrating the output signals wit RC networks. Approximately 115 ms after the switch-on of an ultrasonic command, the pulse duty cycle is advanced by one step. In the case of a continuous signal, further steps follow at intervals of 138.5 ms until the final value is reached. The time needed to traverse the entire range of variation is 8.5 seconds. During the pulse duration, the open drain output transistor is turned on and has a voltage drop of max 0.6V at 1 mA output current. When the supply is switched on the analog outputs are normalized to the pulse duty cycle of 32/63. A Mute command switches the open drain output transistor at pin 4 OFF and ON after a delay of 0,7 sec. The sound is also restored after a normal delay when one of the commands "Volume +" or "Volume -" is given. The sound is unmuted when the TV set is switched ON.

Fig. 1



DESCRIPTION (continued)

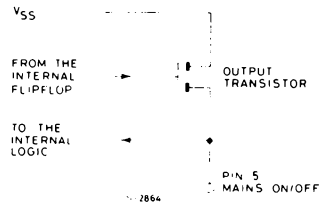
Pin 5 - Mains switch output

This output is provided to control the ON/OFF switching of the TV set via a transistor and a relay. When the supply voltage is applied to the M 1130 the output transistor is automatically biased off. In this "stand-by" condition, the analog outputs cannot be changed; this lasts until a mains ON command is given in one of the following modes:

- by any of the 16 program commands for 0.7 sec.
- by the command "sequential program change" (available only on direct inputs) for 0.7 sec.
- by connecting the pin 5 to V_{SS} for at least 10 μs.

The TV set can only be switched off by a "Mains OFF" command.

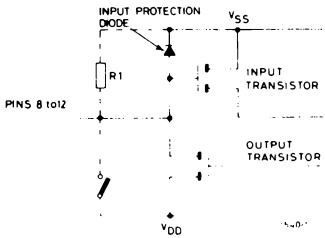
Fig. 2



Pins 8, 9, 10, 11, 12 - Direct inputs/outputs

These pins are provided as inputs for commands on the TV set and also as outputs for ultrasonic transmitted commands. The command may be introduced directly in the form of a 5 bit word applied to the input/output lines A-B-C-D-E, according to the code indicated in the truth table. An input signal is recognized as valid after an acceptance time of 69.3 ms (for Mains ON/OFF and Muting ON 0.6 sec.), after which a further processing period of 46.2 ms occurs before the 23.1 ms output signal appears. During the 23.1 ms pulse the output transistor shown in fig. 3 is conducting. The same pulse will appear when the circuit is receiving coded commands from the ultrasonic input according to the truth table. Although the output signals are felt on the input again this does not cause interference because the inputs are locked while an output signal is available. If commands are issued either ultrasonically or normally to the television set, the manual command will always override the ultrasonic command. Concerning the "touch" command, this type of operation is possible due to the very high impedance of the MOS input. The only major point of consideration is in the choice of diode matrix; this must have such a high reverse leakage current in even the worst conditions that an incorrect command situation is avoided.

Fig. 3



Pins 6, 7, 13, 14 - Program outputs PA-PB-PC-PD

The information of the selected program is statically available in a binary coded form. The code is shown in table 2. TV programs are chosen either selectively (by the commands "Program 1 . . Program 16") or sequentially upwards on the command "Sequential program change". If the "Sequential program change" command is given continuously, the first change of program takes place after 115 ms and every further change at 0.7 sec intervals. After program 16 has been reached it is followed again by program 1. When the supply voltage is applied to the M 1130, the program outputs are automatically set to program 1. If the TV set is switched on by the command "Sequential program change" this command is made ineffective until it is released.

The output configurations is similar to that shown in fig. 2.

An external load of min 47 KΩ is to be connected to these outputs even if they are not used.

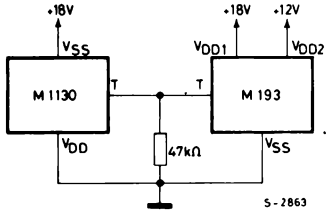
DESCRIPTION (continued)

Pin 15 - Ultrasonic input
Ultrasonic signals of at least 500 mV peak to peak have to be applied to this input via a capacitor. The integrated input amplifier is automatically biased and has an input resistance exceeding 1 Mohm. The first ultrasonic pulses arriving at pin 15 are followed by a preparation period of 23.1 ms. After a measuring time and a delay time of 46.2 ms a pulse of 23.1 ms will appear on the input/output lines according to truth table 1. If a continuous signal is present at the ultrasonic input, the interval between the output pulses amounts to 138.5 ms.

Pin 16 - T output

When commands S4 or S5 are given, in addition to the binary coded output signals at the I/O lines, a further signal in the shape of a pulse is available at this pin. The pulse which has a duration of 21.6 μs in the case of command S4 and of 23.1 ms in the case of command S5, is used for remote control of the fine tuning via the SGS-ATES M 193 Electronic Program Memory as shown in fig. 4.

Fig. 4



Pin 17 - Quartz terminal
A 4.4336 MHz quartz crystal has to be connected between this pin and V_{SS}. A resistor of 5.6 Mohm has to be connected between the input and V_{DD} to bias the integrated oscillator. The accuracy of the frequency determines the evaluation accuracy of the ultrasonic receiver.

1024 - BIT STATIC RANDOM ACCESS MEMORY

POWER SUPPLY V_{CC}= 5V
TTL COMPATIBLE ALL INPUTS AND OUTPUTS
THREE-STATE OUTPUT
INPUTS PROTECTED AGAINST STATIC CHARGE
ORGANIZATION 1024 x 1 BIT IN 16 PIN STD PACKAGE

TYPE	STANDBY PWR (mW)	OPERATING PWR (mW)	ACCESS TIME (ns)
M 2102 AL - 2	42	342	250
M 2102 AL	35	174	350
M 2102 AL - 4	35	174	450
M 2102 A - 2	–	342	250
M 2102 A	–	289	350
M 2102 A - 4	–	289	450
M 2102 A - 6	–	289	650

The M 2102A is a high speed 1024 word by 1 static N-channel silicon-gate MOS RAM. The device is fully static and therefore does not require clocks or refreshing to operate. The data is read out non destructively and has the same polarity as the input data.
A low standby power version (M 2102 AL) is also available. It has all the same operating characteristics of the M 2102A with the added feature of 35 mW maximum power dissipation in standby and 174 mW in operations. The device is available in 16 lead dual in-line ceramic package, metal-seal or frit-seal and plastic package.

ABSOLUTE MAXIMUM RATINGS

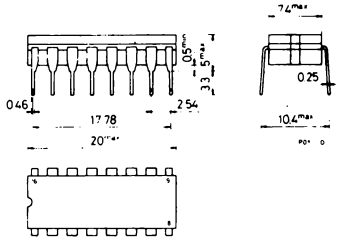
V_i*	Input voltage (at any pin)	-0.5 to 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature under bias	0 to 70	°C

* All voltage are referred to GND pin voltage

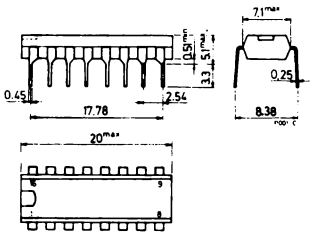
ORDERING NUMBERS:
M 2102A - B1 for dual-in-line plastic package
M 2102A - D1 for dual-in-line ceramic package, metal-seal
M 2102A - F1 for dual-in-line ceramic package, frit-seal
M 2102AL - B1 for dual-in-line plastic package
M 2102AL - D1 for dual-in-line ceramic package, metal-seal
M 2102AL - F1 for dual-in-line ceramic package, frit-seal

MECHANICAL DATA (dimensions in mm)

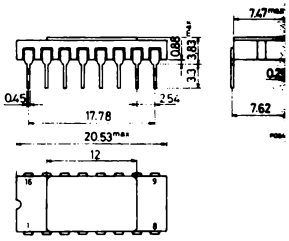
Dual in-line ceramic package frit-seal for M2102A/AL-F1



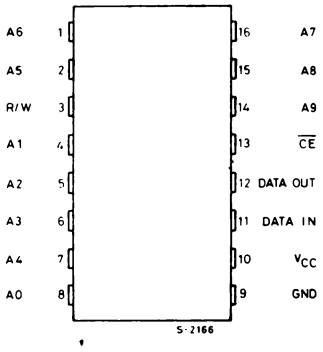
Dual in-line plastic package for M 2102A/AL-B1



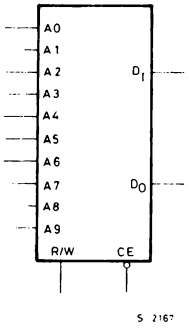
Dual in-line ceramic package metal-seal for M 2102A/AL-D



CONNECTION DIAGRAM



LOGIC DIAGRAM



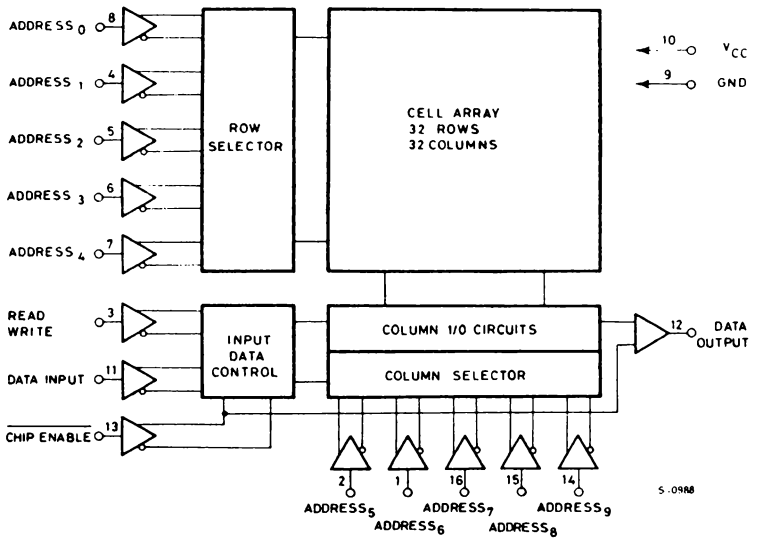
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (V_{CC}= 4.75 to 5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions	M 2102 A M 2102 AL M 2102 A -4 M 2102 AL-4			M 2102 A -2 M 2102 AL-2			M 2102 A-6			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
V_{IH}	Input high voltage		2		V_{CC}	2		V_{CC}	2.2		V_{CC}	V
V_{IL}	Input low voltage		-0,5		0.8	-0.5		0.8	-0.5		0.65	V
V_{OH}	Output high voltage	I_{OH}= -100 µA	2.4			2.4			2.2			V
V_{OL}	Output low voltage	I_{OL}= 2.1 mA			0.4			0.4			0.45	V
I_{LI}	Input load current	V_I= 0 to 5.25V		1	10		1	10		1	10	µA
I_{OH}	Output leakage current	$\overline{CE}$= 2V. V_O= V_{OH}		1	5		1	5		1	5	µA
I_{OL}	Output leakage current	$\overline{CE}$= 2V V_O= 0.4V		-1	-10		-1	-10		-1	-10	µA
I_{CC}	Supply current	V_I= 5.25V T_{amb}= 0°C Data out open		33	**		45	65		33	55	mA

* Typical values for T_{amb}= 25°C and nominal supply voltage.
** The maximum I_{CC} value is 55 mA for the M 2102A and M 2102A-4, and 33 mA for the M 2102AL and M 2102AL-4.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C, V_{CC}= 5V ± 5% unless otherwise specified)

Parameter		Test condition	M 2102 A -2 M 2102 AL-2		M 2102 A - M 2102 AL		M 2102 A -4 M 2102 AL-4		M 2102 A-6		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
t_{rc}	Read cycle	t_R, t_F= 10 ns Load = 1 TTL gate and C_L= 100 pF	250		350		450		650		ns
t_a	Access time			250		350		450		650	ns
t_E	CE to output time			130		180		230		400	ns
t_{OH1}	Previous read data valid with respect to address		40		40		40		50		ns
t_{OH2}	Previous read data valid with respect to chip enable		0		0		0		0		ns
Write Cycle											
t_{WC}	Write cycle	t_R, t_F= 10 ns Load = 1 TTL gate and C_L= 100 pF	250		350		450		650		ns
t_{AW}	Address to with setup time		20		20		20		200		ns
t_{WP}	Write pulse width		180		250		300		400		ns
t_{WR}	Write recovery time		0		0		0		50		ns
t_S	Data setup time		180		250		300		450		ns
t_h	Data hold time		0		0		0		20		ns
t_{CW}	Chip enable to write setup time		180		250		300		550		ns

CAPACITANCE (T_{amb}= 25°C, f= 1 MHz)

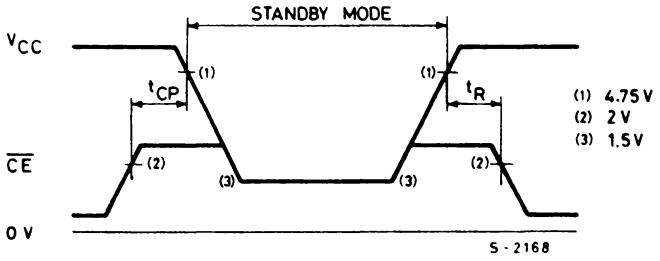
Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I = 0V		3	5	pF
C_O	Output capacitance	V_O = 0V		7	10	pF

STANDBY CHARACTERISTICS (T_{amb}= 0°C to 70°C)

Parameter		Test conditions	M 2102 AL-4 M 2102 AL			M 2102 AL-2			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
V_{PD}	V_{CC} in standby		1.5			1.5			V
V_{CES}**	CE bias in standby	$2V \leqslant V_{PD} \leqslant V_{CC}$ Max.	2			2			V
		$1.5V \leqslant V_{PD} < 2V$	V_{PD}			V_{PD}			V
I_{PD1}	Standby current	All inputs = V_{PD1} = 1.5V		15	23		20	28	mA
I_{PD2}	Standby current	All inputs = V_{PD2} = 2V		20	30		25	38	mA
t_{CP}	Chip deselect to standby time		0			0			ns
t_R***	Standby recovery time		t_{RC}			t_{RC}			ns

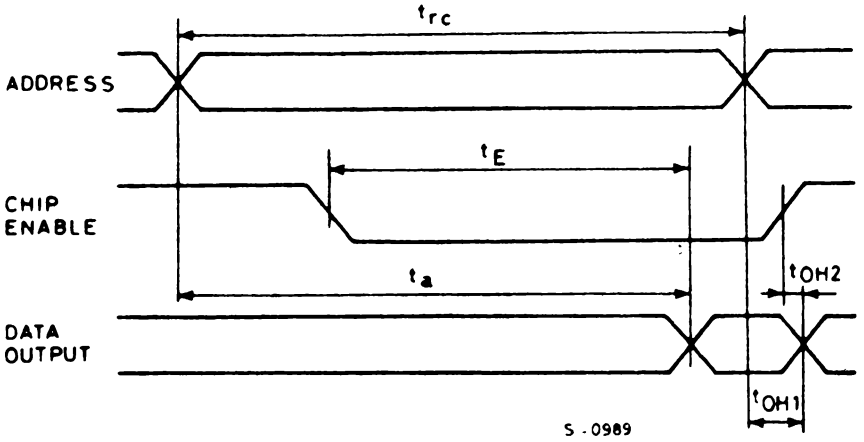
* Typical values are for T_{amb}= 25°C.
** Consider the test conditions as shown: if the standby voltage (V_{PD}) is between 5.25V (V_{CC} max) and 2V, then $\overline{CE}$ must be held at 2V Min. (V_{IH}). If the standby voltage is than 2V but greater than 1.5V (V_{PD} min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
***$t_R = t_{RC}$ (READ CYCLE TIME).

STANDBY WAVEFORMS

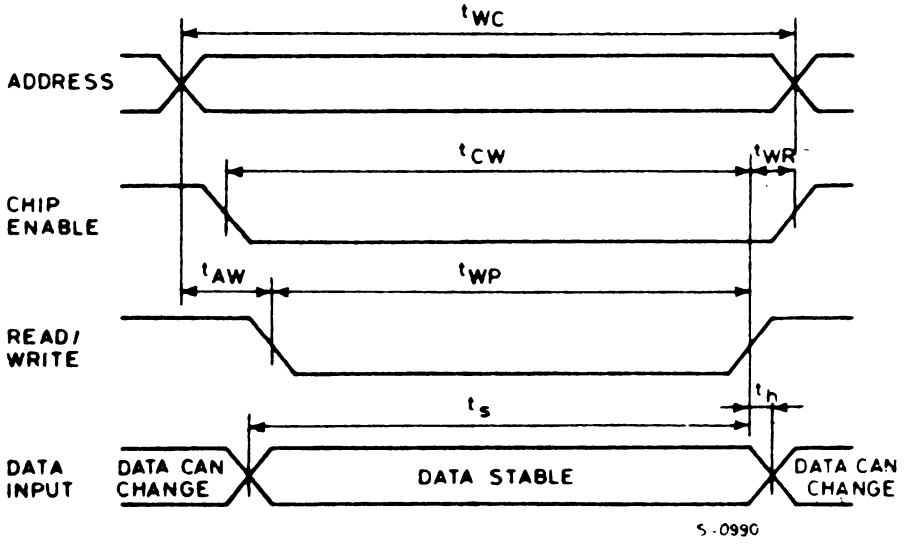


WAVEFORMS

Read cycle



Write cycle



MOS INTEGRATED CIRCUIT

M 2316E

16384 BIT READ ONLY MEMORY

- SINGLE +5V ± 10% POWER SUPPLY
- ACCESS TIME 450 ns (MAX.)
- INPUTS AND OUTPUTS TTL COMPATIBLE
- THREE PROGRAMMABLE CHIP SELECTS FOR SIMPLE MEMORY EXPANSION AND SYSTEM INTERFACE
- COMPLETLY STATIC OPERATION
- THREE-STATE OUTPUT FOR DIRECT BUS INTERFACE

The M 2316E is a 16384 bit static Read Only Memory N-channel Si-Gate MOS organized as 2048 words by 8 bits. Its high bit density is ideal for large, non-volatile data storage applications such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures.
The M 2316E is available in 24-lead dual-in-line plastic package.

ABSOLUTE MAXIMUM RATINGS

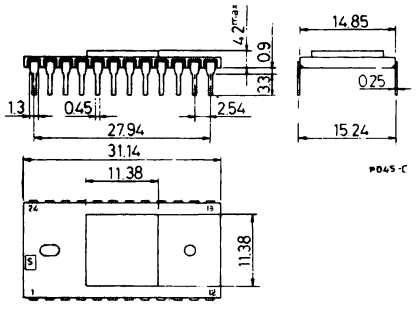
V_i*	Input voltage (at any pin)	-0.5 to 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	-55 to +125	°C
T_{op}	Operating temperature under bias	-10 to 80	°C

* This voltage is with respect to Ground

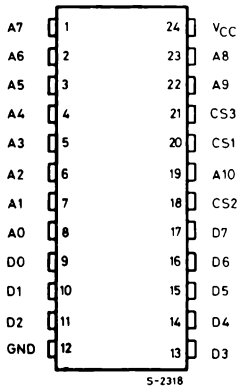
ORDERING NUMBER: M 2316E B1 for dual in-line plastic package

MECHANICAL DATA

Dimensions in mm



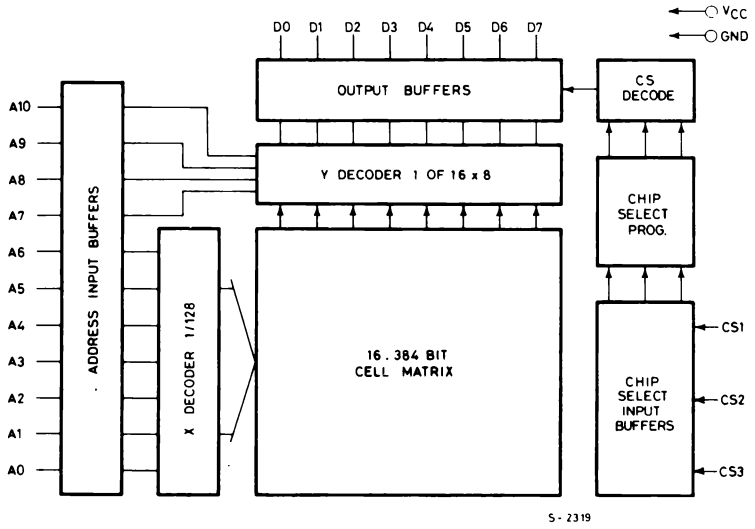
PIN CONNECTIONS



PIN NAMES

A0 - A10	ADDRESS INPUTS
D0 - D7	DATA OUTPUTS
CS1 - CS3	CHIP SELECT INPUTS

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0°C to +70°C, V_{CC}= 5V ± 10% unless otherwise specified)

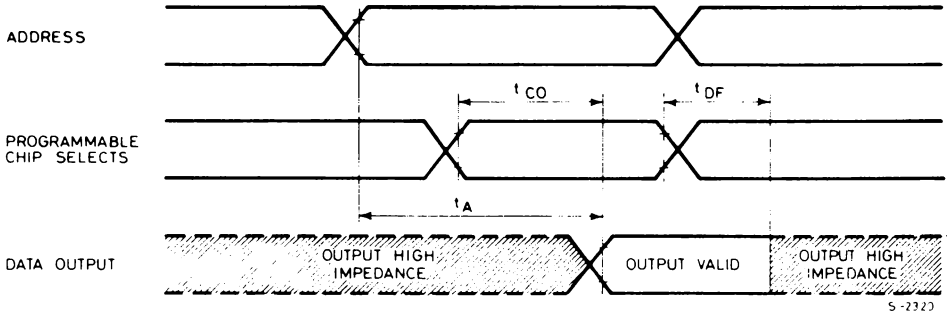
Parameter		Test conditions	Min.	Typ.(1)	Max.	Unit
I_{LI}	Input load current(All input pins)	V_I= 0 to 5.25V			10	μA
I_{LOH}	Output leakage current	Chip deselected V_O= 4V			10	μA
I_{LOL}	Output leakage current	Chip deselected V_O= 0.4V			-20	μA
I_{CC}	Power supply current	All inputs 5.25V Data out open		70	120	mA
V_{IL}	Input low voltage		-0.5		0.8	V
V_{IH}	Input high voltage		2.4		V_{CC}+1V	V
V_{OL}	Output low voltage	I_{OL}= 2.1 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}= -400 μA	2.4			V

Note: 1 Typical values for T_{amb}= 25°C and nominal supply voltage.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0°C to 70°C, V_{CC}= +5V ± 10%unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_A	Address to output delay time	Output load = 1 TTL gate and C_L= 100 pF Input pulse levels -0.8 to 2.4V Input pulse rise and fall times (10% to 90%) -20 ns Timing Measurement Reference level: Input = 1V and 2.2V Output = 0.8V and 2.2V			850	ns
t_{CO}	Chip select to output enable delay time				120	ns
t_{DF}	Chip deselect to output data float delay time		10		100	ns
C_I	Input capacitance	T_{amb}= 25°C f = 1 MHz All pins except pin under test tied to AC ground		5	10	pF
C_O	Output capacitance	T_{amb}= 25°C f = 1 MHz All pins, except pin under test tied to AC ground		10	15	pF

A.C. Waveforms



MOS INTEGRATED CIRCUITS

M 2708
M 2704

PRELIMINARY DATA

M 2708-8K BIT (1024 X 8) UV ERASABLE PROM
M 2704-4K BIT (512 X 8) UV ERASABLE PROM

- STANDARD POWER SUPPLES: +12V, +5V, -5V
- TTL COMPATIBLE: ALL INPUTS AND OUTPUTS DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT
- ORGANIZATION: M 2708-1024 X 8-BIT IN A 24-LEAD DUAL IN-LINE PACKAGE
  M 2704-512 X 8-BIT IN A 24-LEAD DUAL IN-LINE PACKAGE
- ACCESS TIME: 450 ns MAX.
- FAST PROGRAMMING: TYP. 100 sec. FOR ALL 8K BITS
- LOW POWER CONSUMPTION DURING PROGRAMMING

The M 2708 and the M 2704 are high-speed 1024 x 8/512 x 8-bit erasable and electrically reprogrammable static ROMs (EPROM) manufactured in N-channel silicon gate MOS technology. They are supplied in 24-lead dual in-line ceramic package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices. The devices are fully static and therefore require no clocks to operate.

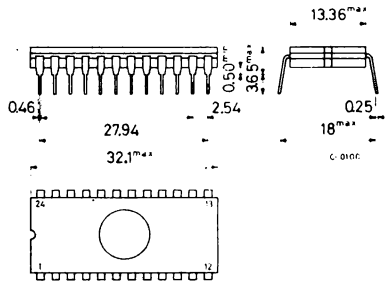
ABSOLUTE MAXIMUM RATINGS

V_{DD}	V_{DD} with respect to V_{BB}	+20V to -0.3	V
V_{CC}, V_{SS}	V_{CC} and V_{SS} with respect to V_{BB}	+15V to -0.3	V
V_{BB}	All input or output voltages with respect to V_{BB} during read	+15V to -0.3	V
$\overline{CS}$/WE	Input with respect to V_{BB} during programming	+20V to -0.3	V
	Program input with respect to V_{BB}	+35V to -0.3	V
P_{tot}	Power dissipation	1.5	W
T_{amb}	Ambient temperature under bias	-25 °C to + 85	°C
T_{stg}	Storage temperature	-65 °C to +125	°C

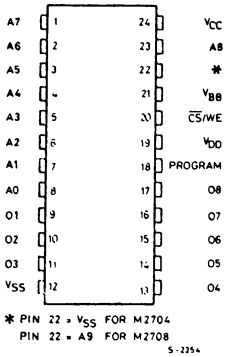
ORDERING NUMBERS: M 27 XX F1 for dual in-line ceramic package, frit seal

MECHANICAL DATA

dimensions in mm



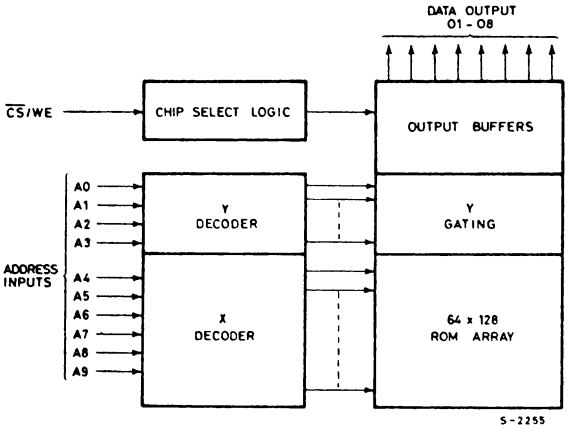
PIN CONNECTIONS



PIN NAMES

A0-A9	ADDRESS INPUTS
01-08	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

BLOCK DIAGRAM



MODE	PIN NUMBER						
	9,11,13,17	12	18	19	20	21	24
READ	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
PROGRAM	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

READ OPERATION

D.C. AND OPERATING CHARACTERISTICS (V_{CC} = +5V ± 5%, V_{DD} = +12V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.*	Max.	
I_{LI}	Address and chip select input sink current	V_I = 5.25V or $V_I = V_{IL}$		1	10	µA
I_{LO}	Output leakage current	V_O = 5.25V, $\overline{CS}$/WE = 5V		1	10	µA
I_{DD}	V_{DD} supply current	Worst case supply current: all inputs high $\overline{CS}$/WE = 5V T_{amb} = 0°C		50	65	mA
I_{CC}	V_{CC} supply current			6	10	mA
I_{BB}	V_{BB} supply current			30	45	mA
V_{IL}	Input low voltage		V_{SS}		0.65	V
V_{IH}	Input high voltage		3		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA			0.45	V
V_{OH1}	Output high voltage	I_{OH} = -100 µA	3.7			V
V_{OH2}	Output high voltage	I_{OH} = -1 mA	2.4			V
P_{tot}	Power dissipation	T_{amb} = 70°C			800	mW

* Typical values are for T_{amb} = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS (V_{CC} = +5V ± 5%, V_{DD} = +12V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 70 °C unless otherwise specified)

Parameter		M 2708-1			M 2708			M 2708-4			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{ACC}	Address to output delay		280	350		280	450		350	700	ns
$t_{\overline{CO}}$	Chip select to output delay		60	120		60	120		80	170	ns
t_{DF}	Chip de-select to output float	0		120	0		120	0		170	ns
t_{OH}	Address to output hold	0			0			0			ns

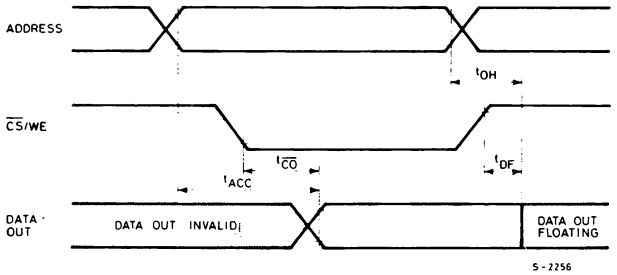
CAPACITANCE (T_{amb} = 25°C, f = 1 MHz)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I = 0V		4	6	pF
C_O	Output capacitance	V_O = 0V		8	12	pF

DYNAMIC TEST CONDITIONS:

Output load = 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times = ⩽ 20 ns
Timing Measurement Reference Levels = 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs.
Input Pulse levels = 0.65V to 3V.

WAVEFORMS



PROGRAMMING

Initially, and after each erasure, all bits of the M 2708/2704 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for the programming operation by raising the $\overline{CS}$/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8-bits in parallel, to the data output lines (01-08). The logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse for address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{pw}) according to $Nxt_{pw} \geqslant 100$ ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{pw}= 1 ms) to greater than 1000 (t_{pw}= 0.1 ms). There must be N successive loops through all 1024 address. It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.

Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small current (I_{PL}) when $\overline{CS}$/WE is at V_{IHW} (12V) and the program is at V_{ILP}. Truth table formats for printed cards and paper tape must be compatible with Intel ones.

ERASURE CHARACTERISTICS

The erasure characteristics of the M 2708 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical M 2708 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight.

The recommended erasure procedure for the M 2708 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The M 2708 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

PROGRAM CHARACTERISTICS

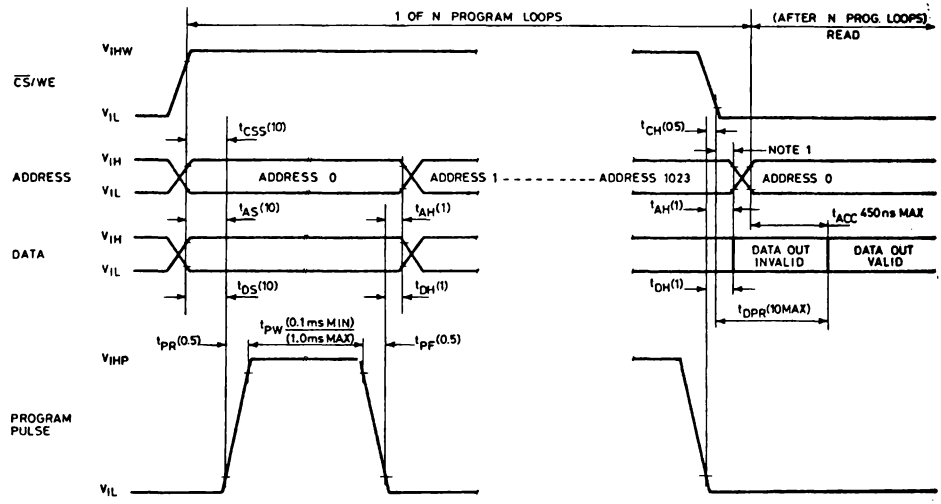
D.C. PROGRAMMING CHARACTERISTICS (T_{amb}= 25°C, V_{CC}= +5V ± 5%, V_{DD}= +12V ± 5%, V_{BB}= -5V ± 5%, V_{SS}= 0V unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Address CS/W input sink current	V_i = 5.25V			10	µA
I_{IPL}	Program pulse source current				3	mA
I_{IPH}	Program pulse sink current				20	mA
I_{DD}	V_{DD} supply current	Worst case supply current all inputs high $\overline{CS}$/WE= 5V; T_{amb}= 0° C		50	65	mA
I_{CC}	V_{CC} supply current			6	10	mA
I_{BB}	V_{BB} supply current			30	45	mA
V_{IL}	Input low level (except program)		V_{SS}		0.65	V
V_{IH}	Input high level for all address or data		3		V_{CC}+1	V
V_{IHW}	$\overline{CS}$/WE input high level	referenced to V_{SS}	11.4		12.6	V
V_{IHP}	Program pulse high level	referenced to V_{SS}	25		27	V
V_{ILP}	Program pulse low level	V_{IHP}-V_{ILP}= 25V min.	V_{SS}		1	V

A.C. PROGRAMMING CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address setup time		10			µs
t_{CSS}	$\overline{CS}$/WE setup time		10			µs
t_{DS}	Data setup time		10			µs
t_{AH}	Address hold time		1			µs
t_{CH}	$\overline{CS}$/WE hold time		0.5			µs
t_{DH}	Data hold time		1			µs
t_{DF}	Chip deselect to output float delay		0		120	ns
t_{DPR}	Program to read delay				10	µs
t_{PW}	Program pulse width		0.1		1	ms
t_{PR}	Program pulse rise time		0.5		2	µs
t_{PF}	Program pulse fall time		0.5		2	µs

PROGRAMMING WAVEFORMS



NOTE 1: THE $\overline{CS}/WE$ TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION
NOTE 2: NUMBERS IN ( ) INDICATE MINIMUM TIMING IN μs UNLESS OTHERWISE SPECIFIED

S-2257

MOS INTEGRATED CIRCUIT

M 4027

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

- POWER SUPPLY V_{DD}= 12V, V_{CC}= 5V, V_{BB}= -5V (ALL WITH ± 10% TOLERANCE)
- ALL INPUTS ARE LOW CAPACITANCE AND TTL COMPATIBLE
- INPUT LATCHES FOR ADDRESSES, CHIP SELECT AND DATA IN
- INPUTS PROTECTED AGAINST STATIC CHARGE
- THREE-STATE TTL COMPATIBLE OUTPUT
- OUTPUT DATA LATCHED AND VALID INTO NEXT CYCLE
- ECL COMPATIBLE ON V_{BB} POWER SUPPLY (-5.7V)
- LOW POWER CONSUMPTION: ACTIVE POWER UNDER 470 mW
  STANDBY POWER UNDER 27 mW
- ORGANIZATION 4096 x 1 BIT IN 16-PIN STD PACKAGE
- FUNCTIONAL AND PIN COMPATIBLE WITH MK4027
- ACCESS TIME: TYPE M 4027-2 150 ns
  TYPE M 4027-3 200 ns
  TYPE M 4027-4 250 ns

The M 4027 is a 4096 word by 1 bit dynamic N-channel silicon gate MOS RAM. The M 4027 uses a single transistor cell utilizing a dynamic storage technique and dynamic control circuitry with low power dissipation. A unique multiplexing and latching technique for the address inputs permits the M 4027 to be mounted in a standard 16-pin package. The M 4027 incorporates several flexible operating modes. In addition to the usual read and write cycles, read modify write, page mode and RAS-only refresh cycles are available with the M 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA). The device is available in 16-lead dual in-line plastic or ceramic package (metal-seal), and ceramic package (frit-seal).

ABSOLUTE MAXIMUM RATINGS*

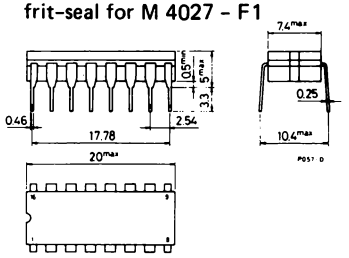
	Voltage on any pin relative to V_{BB}	-0.5 to +20	V
	Voltage on V_{DD}, V_{CC} relative to V_{SS}	-1 to +15	V
	V_{BB}-V_{SS} (V_{DD}-$V_{SS} > 0$)	0	V
T_{op}	Operating temperature	0 to +70	°C
T_{stg}	Storage temperature for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
I_o	Short circuit output current	50	mA
P_{tot}	Total power dissipation	1	W

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

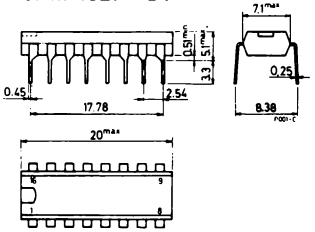
ORDERING NUMBERS: M 4027-2/3/4 B1 for dual in-line plastic package
M 4027-2/3/4 D1 for dual in-line ceramic package, metal-seal
M 4027-2/3/4 F1 for dual in-line ceramic package, frit-seat

MECHANICAL DATA (dimensions in mm)

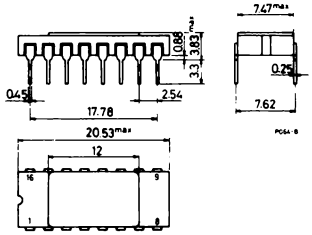
Dual in-line ceramic package
frit-seal for M 4027 - F1



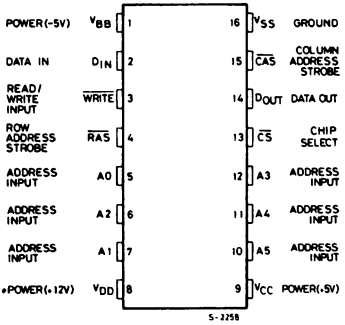
Dual in-line plastic package
for M 4027 - B1



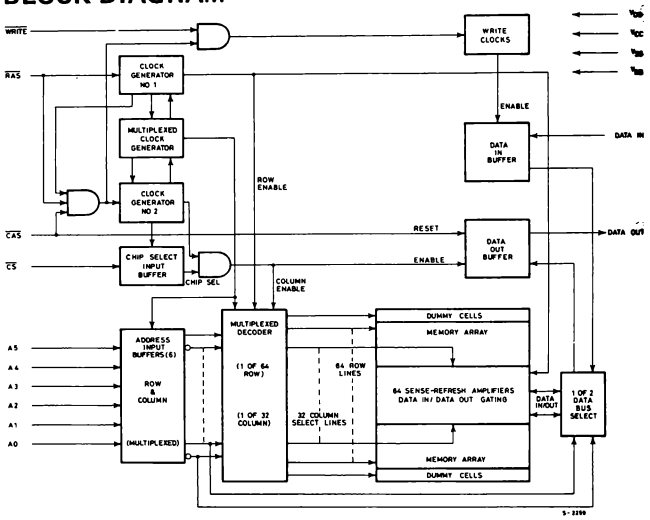
Dual in-line ceramic package
metal-seal for M 4027 - D1



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS[1] (T_{amb}= 0 to 70°C)[4]

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply voltage	10.8	12	13.2	V	2
V_{CC}	Supply voltage	4.5	5	5.5	V	2, 3
V_{SS}	Supply voltage	0	0	0	V	2
V_{BB}	Supply voltage	-4.5	-5	-5.7	V	2
V_{IHC}	Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V	2
V_{IH}	Input high voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7	V	2
V_{IL}	Input low voltage, all inputs	-1		0.8	V	2

DC ELECTRICAL CHARACTERISTICS[1] (T_{amb}= 0 to 70°C)[4] (V_{DD}= 12V ± 10%, V_{CC}= 5V ± 10%, V_{SS}= 0V, V_{BB}= - 5.7 to -4.5V)

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
I_{DD1}	Average V_{DD} power supply current			35	mA	5
I_{DD2}	Standby V_{DD} power supply current			2	mA	8
I_{DD3}	Average V_{DD} power supply current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} power supply current				mA	6
I_{BB}	Average V_{BB} power supply current			150	µA	
$I_{I(L)}$	Input leakage current (any input)			10	µA	7
$I_{O(L)}$	Output leakage current			10	µA	8, 9
V_{OH}	Output high voltage (I_{SOURCE}= -5 mA)	2.4			V	
V_{OL}	Output low voltage (I_{SINK}= 3.2 mA)			0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[1, 10, 15]

(T_{amb} = 0 to 70°C)[4], (V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

Parameter		Types						Unit	Notes
		M 4027-2		M 4027-3		M 4027-4			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random read or write cycle time	320		375		380		ns	
t_{RWC}	Read write cycle time	320		375		395		ns	
t_{RMW}	Read modify write cycle time	320		405		470		ns	
t_{RAC}	Access time from row address strobe		150		200		250	ns	11-13
t_{CAC}	Access time from column address strobe		100		135		165	ns	12-13
t_{OFF}	Output buffer turn-off delay		40		50		60	ns	
t_{RP}	Row address strobe precharge time	100		120		120		ns	
t_{RAS}	Row address strobe pulse width	150	10000	200	10000	250	10000	ns	
t_{RSH}	Row address strobe hold time	100		135		165		ns	
t_{CAS}	Column address strobe pulse width	100		135		165		ns	
t_{CSH}	Column address strobe hold time	150		200		250		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	35	85	ns	14
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	-10		-10		-10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CSC}	Chip select set-up time	-10		-10		-10		ns	
t_{CH}	Chip select hold time	45		55		75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_T	Transition time (rise and fall)	3	35	5	50	5	50	ns	15
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to row strobe lead time	50		70		85		ns	
t_{CWL}	Write command to column strobe lead time	50		70		85		ns	
t_{DS}	Data in set-up time	0		0		0		ns	16

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (cont.)

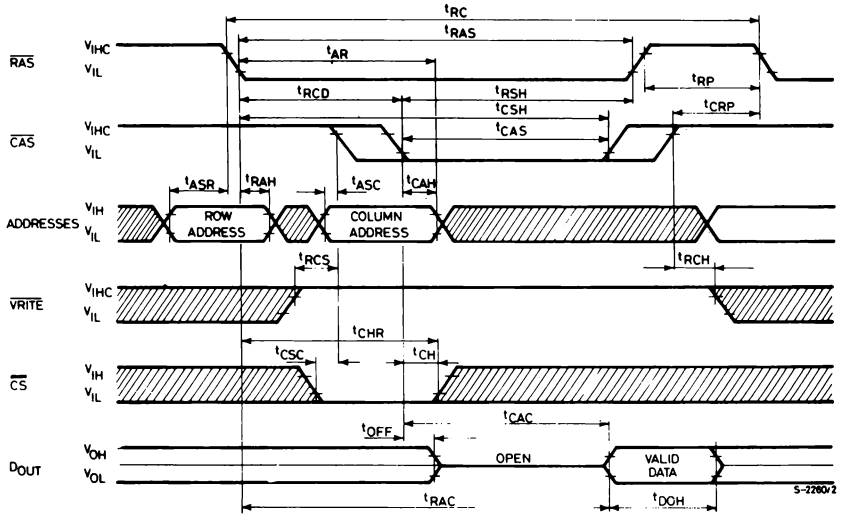
Parameter		Types						Unit	Notes
		M 4027-2		M 4027-3		M 4027-4			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{DH}	Data in hold-time	45		55		75		ns	16
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CRP}	Column to row strobe precharge time	0		0		0		ns	
t_{CP}	Column precharge time	60		80		110		ns	
t_{RFSH}	Refresh period		2		2		2	ms	
t_{WCS}	Write command set-up time	0		0		0		ns	17
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	17
t_{RWD}	RAS to WRITE delay	110		145		175		ns	17
t_{DOH}	Data out hold time	10		10		10		μs	

CAPACITANCES (T_{amb}= 0 to 70°C, V_{DD}= 12V ± 10%; V_{SS}= 0V; V_{BB}= -5.7 to -4.5V)

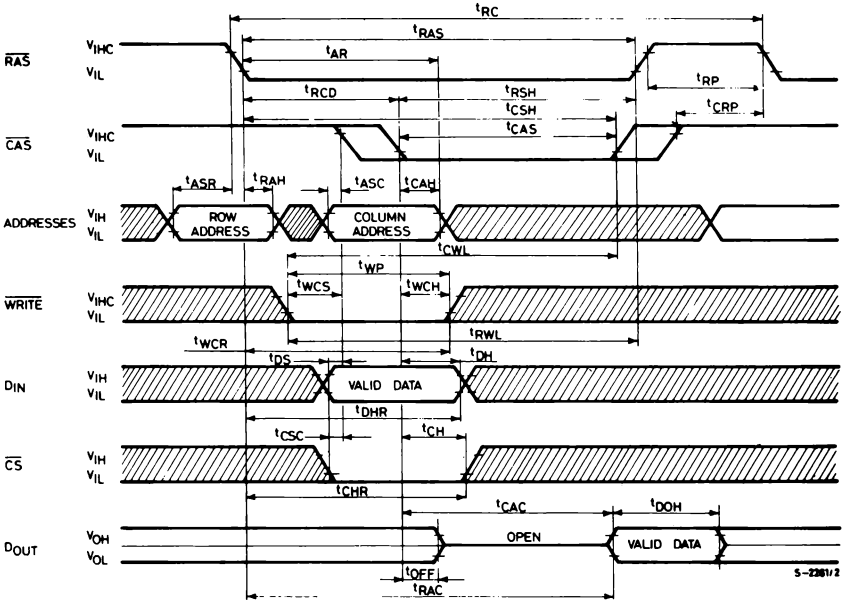
Parameter		Values		Unit	Notes
		Typ.	Max.		
C_{I1}	Input capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	18
C_{I2}	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	18
C_O	Output capacitance (D_{OUT})	5	7	pF	8-18

1. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
2. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. T_{amb} is specified for operation at frequencies to $t_{RC} \geqslant t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min).
6. I_{CC} depends on output loading. The V_{CC} supply is connected to the output buffer only.
7. All device pins at 0 volts except V_{BB} which is at -5V and the pin under test which is at +10V.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leqslant V_{out} \leqslant +10V$.
10. AC measurements assume t_T= 5 ns.
11. Assumes that $t_{RCD} \leqslant t_{RCD}$ (max).
12. Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).
13. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geqslant t_{CWD}$ (min) and $t_{RWD} \geqslant t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.
18. Effective capacitance is calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts.

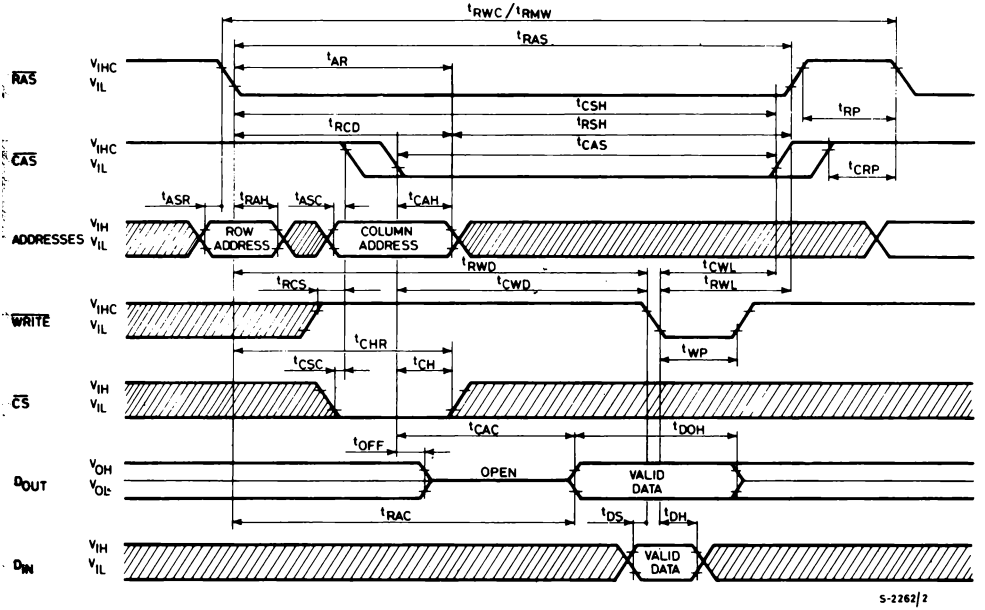
READ CYCLE



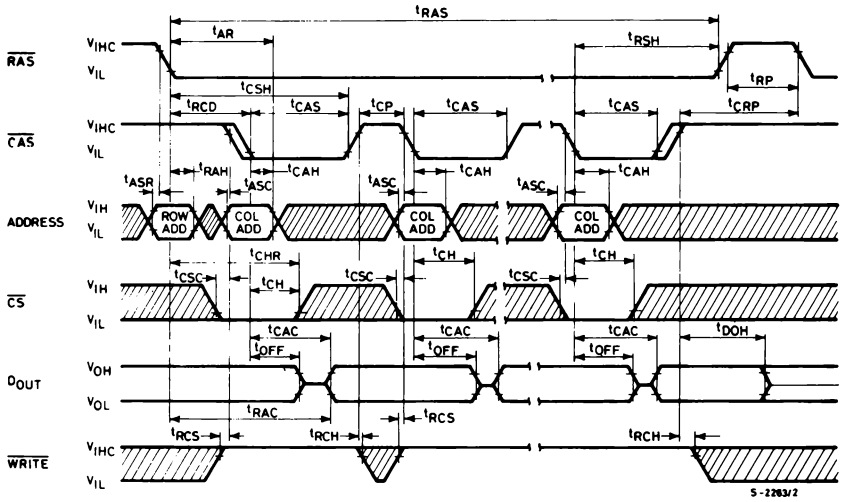
WRITE CYCLE
(early write)



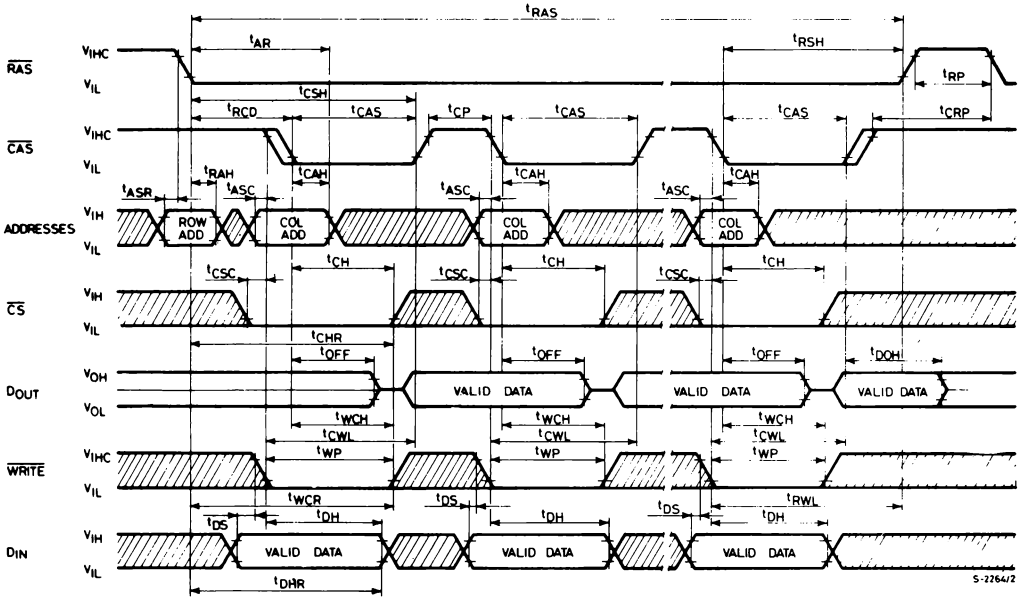
READ WRITE/READ MODIFY-WRITE CYCLE



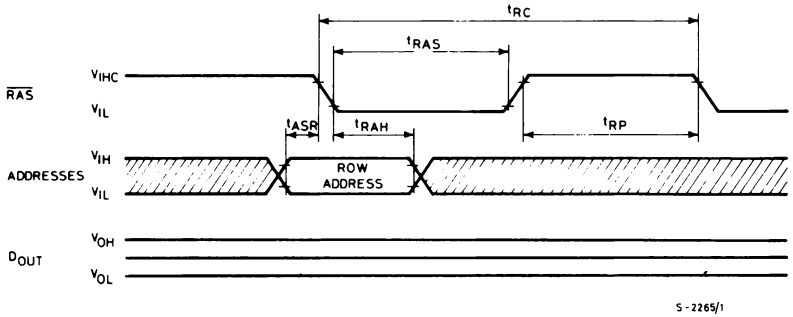
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



RAS ONLY REFRESH CYCLE



ADDRESSING

The 12 address bits required to decode one of 4096 cell locations within the M 4027 are multiplexed onto the 6 address inputs and latched into the on-chip row and column address latches.
Row Address Strobe ($\overline{RAS}$) latches the six row address bits onto the chip. Column Address Strobe ($\overline{CAS}$) latches the six column address bits plus Chip Select ($\overline{CS}$) onto the chip.
Since the internal circuitry allows the columns information to be externally applied to the chip before it is actually required, the hold time requirements for column address and $\overline{CS}$ are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the systems designer to compensate for timing skews that may be encountered in the multiplexing operation.
Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.
Additional timing margin is gained because column address is not required until $\overline{CAS}$ makes its negative transition.
The timing is further simplified by the positive transition of $\overline{CAS}$ not being referenced to the positive transition of $\overline{RAS}$. In fact, $\overline{CAS}$ need not go HIGH until the beginning of the next cycle.

DATA INPUT/OUTPUT

Data to be written into selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active.
The later of this signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In into the latch. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is activated prior to $\overline{CAS}$, the Data In is strobe by $\overline{CAS}$, and set-up time and hold time are referenced to $\overline{CAS}$. If the Data In input is not available at $\overline{CAS}$ time or the cycle is a read-write or read-modify-write, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$)
Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected. Data is retrieved from the memory in read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

At the beginning of a memory cycle, the state of the Data Out latch and buffer depend on the previous memory cycle.
Changes in the condition of Data Out latch are initiated by $\overline{CAS}$. The negative transition of $\overline{CAS}$ causes the Data Output (D_{OUT}) to unconditionally go to its open-circuit state. If will remain open-circuited until after the access D_{OUT} time, the will assume the proper state for the type of cycle performed.
If the cycle is a read, read-modify-write, or a delayed write and the chip is selected, then the D_{OUT} latch and buffer will contain the data from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then D_{OUT} will contain the input data.
Once the D_{OUT} goes active, it will remain active until the next negative transition of $\overline{CAS}$.
If the cycle is a $\overline{CAS}$ only cycle (no $\overline{RAS}$ signal), then D_{OUT} will assume the open - circuit state.
The same istrue for normal cycles (both $\overline{RAS}$ and $\overline{CAS}$ present-when the chip is unselected D_{OUT} remains in the open-circuit state until the next negative transition of $\overline{CAS}$.
$\overline{RAS}$ only refresh cycles (no $\overline{CAS}$) have no effect on the D_{OUT}.
However, when $\overline{RAS}$ only refresh cycles are continued for extended periods of time, D_{OUT} may eventually go open-circuit.
If the chip unselected, it will not accept a write command and the D_{OUT} will remain in the open-circuit state.

INPUT/OUTPUT LEVELS

All inputs, including the two address strobes, interface directly with TTL.
The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements.
The 3-state output buffer is a low impedance to V_{CC} for a logic "1" and a low impedance to V_{SS} for a logic "0".
The output resistance to V_{CC} (logic "1" state) is 420 ohm maximum and 135 ohm tipically.
The output resistance to V_{SS} (logic "0" state) is 125 ohm maximum and 35 ohm tipically.
The separate V_{CC} pin allows the output buffer to be powered from supply voltage of the logic to which chip is interfaced.
During battery stand-by operation, the V_{CC} pin may be unpowered without effecting the M 4027 refresh operation.
This allows all system logic, except $\overline{RAS}$ timing circuitry and refresh address logic, to be turned off during battery stand-by to save power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row address every two millisecond or less.
Any cycle in which a $\overline{RAS}$ signal occurs, accomplished a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input.
A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.
If, during a refresh cycle, the M 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (when $\overline{RAS}$ is the only signal applied to the chip) are contained for extended periods, the output buffer may eventually lose proper data and go open-circuit.
The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the M 4027 and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle.
Tipically, the power is 170 mW at 1 μsec cycle rate for M 4027 with a worse case power of less than 470 mW at 320 μsec cycle time.
To reduce the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips.
The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output).
Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs.
If the $\overline{RAS}$ signal is decoded and supplied only the selected chips, then the chip select ($\overline{CS}$) input of all chips can be at a logic 0.
Then chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input.
For refresh cycles, however, either the $\overline{CS}$ input for all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR" outputs from turning on with opposing force. Note that the M 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page mode" feature of the M 4027 allows for successive memory operations at multiple column location of the same row address with increased speed without an increase in power.
This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at logic 0 throughout all successive memory cycles in which the row address is common.
This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. The time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page made cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles.
This feature allows the page boundary to be extended beyond the 64 column location in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and deconding $\overline{CS}$ to select the proper block.

POWER UP

The M 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, SGS-ATES recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.
Under system failure condiction in which one or more supplied exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state. After power is applied to the device, the M 4027 requires several cycles before proper device operation is achieved.
Any 8 cycles which perform refresh are adequate for this purpose.

MOS INTEGRATED CIRCUIT

M 4116

PRELIMINARY DATA

16384-BIT DYNAMIC RANDOM ACCESS MEMORY

- RECOGNIZED INDUSTRY STANDARD 16-PIN CONFIGURATION
- 150ns ACCESS TIME, 320ns CYCLE (M 4116-2)
  200ns ACCESS TIME, 375ns CYCLE (M 4116-3)
  250ns ACCESS TIME, 410ns CYCLE (M 4116-4)
- ± 10% TOLERANCE ON ALL POWER SUPPLIES (+12V, ±5V)
- LOW POWER: 462 mW ACTIVE, 20 mW STANDBY (MAX)
- OUTPUT DATA CONTROLLED BY $\overline{CAS}$ AND UNLATCHED AT END OF CYCLE TO ALLOW TWO DIMENSIONAL CHIP SELECTION AND EXTENDED PAGE BOUNDARY
- COMMON I/O CAPABILITY USING "EARLY WRITE" OPERATION
- READ-MODIFY-WRITE, $\overline{RAS}$-ONLY REFRESH, AND PAGE-MODE CAPABILITY
- ALL INPUTS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC CHARGE
- 128 REFRESH CYCLES
- MOSTEK 4116 PIN TO PIN REPLACEMENT
- ECL COMPATIBLE ON V_{BB} POWER SUPPLY (-5.7V)

The M 4116 is a new generation MOS dynamic random access memory circuit organized as 16384 words by 1 bit. The technology used to fabricate the M 4116 is double-poly N-channel silicon gate.
This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry through-out, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin.
Multiplexed address inputs permits the M 4116 to be packaged in a standard 16-pin DIP. The device is available in 16-lead dual in-line ceramic package.

ABSOLUTE MAXIMUM RATINGS*

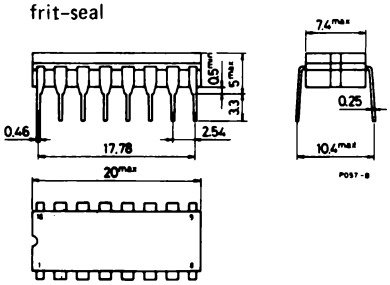
	Voltage on any pin relative to V_{BB}	-0.5 to +20	V
	Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}	-1 to +15	V
	V_{BB}-V_{SS} (V_{DD}-$V_{SS} > 0V$)	0	V
T_{op}	Operating temperature	0 to +70	°C
T_{stg}	Storage temperature for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
I_o	Short circuit output current	50	mA
P_{tot}	Total power dissipation	1	W

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

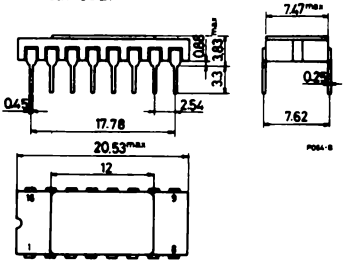
ORDERING NUMBERS: M 4116-2/3/4 D1 for dual in-line ceramic package, metal-seal
M 4116-2/3/4 F1 for dual in-line ceramic package, frit-seal

MECHANICAL DATA (dimensions in mm)

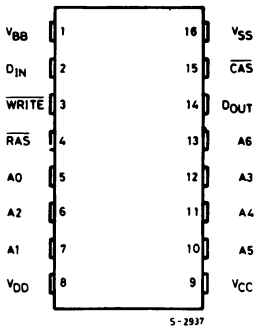
Dual in-line ceramic package
frit-seal



Dual in-line ceramic package
metal-seal



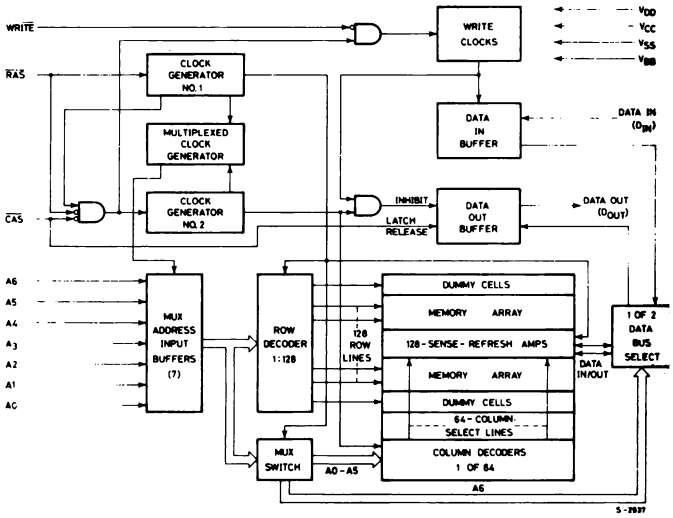
PIN CONNECTIONS



PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (-5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS (T_{amb}= 0 to 70°C)[1]

Parameter		Types			Unit	Note
		Min.	Typ.	Max.		
V_{DD}	Supply voltage	10.8	12	] 13.2	V	2
V_{CC}	Supply voltage	4.5	5	5.5	V	2,3
V_{SS}	Supply voltage	0	0	0	V	2
V_{BB}	Supply voltage	-4.5	-5	-5.7	V	2
V_{IHC}	Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	–	7	V	2
V_{IH}	Input high voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	–	7	V	2
V_{IL}	Input low voltage, all inputs	-1	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C)[1], V_{DD}= 12V±10% V_{CC}= 5V±10%; V_{BB}= -5.7 to -4.5V; V_{SS}= 0V)

Parameter		Test conditions	Types				Unit	Note
			M 4116-2/3		M 4116-4			
			Min.	Max.	Min.	Max.		
I_{DD1}	Average operating current	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}= t_{RC} (min)		35		35	mA	4
I_{CC1}	Average operating current							5
I_{BB1}	Average operating current			200		200	µA	
I_{DD2}	Standby current	$\overline{RAS}$ = V_{IHC} D_{OUT}= High impedance		1.5		1.5	mA	
I_{CC2}	Standby current		-10	10	-10	10	µA	
I_{BB2}	Standby current			100			µA	
I_{DD3}	Refresh average current	Refresh mode: $\overline{RAS}$ cycling $\overline{CAS}$ = V_{IHC} t_{RC}= t_{RC} (min)		27		27	mA	4
I_{CC3}	Refresh average current		-10	10	-10	10	µA	
I_{BB3}	Refresh average current			200			µA	
I_{DD4}	Page mode average current	Page mode: $\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC}= t_{PC} (min)		27		27	mA	4
I_{CC4}	Page mode average current							5
I_{BB4}	Page mode average current			200			µA	
$I_{I(L)}$	Input leakage current	V_{BB}= -5V 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0 volts	-10	10	-10	10	µA	
$I_{O(L)}$	Output leakage current	D_{OUT} in disabled 0V ≤ V_{OUT} ≤ +5.5V	-10	10	-10	10	µA	
V_{OH}	Output high voltage	I_{OUT}= -5 mA	2.4		2.4		V	3
V_{OL}	Output low voltage	I_{OUT}= 4.2 mA		0.4		0.4	V	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDIT.

(T_{amb} = 0 to 70°C)[1], V_{DD} = 12V ± 10%; V_{CC} = 5V ± 10%; V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

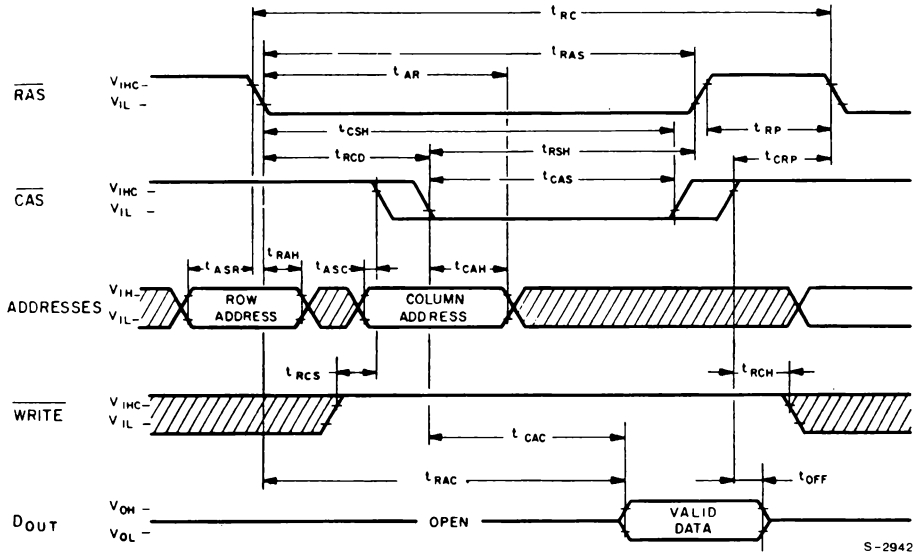
Parameter		Types						Unit	Note
		M 4116-2		M 4116-3		M 4116-4			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random read or write cycle time	320		375		410		ns	9
t_{RWC}	Read-write cycle time	320		375		425		ns	9
t_{RMW}	Read modify write cycle time	320		405		500		ns	9
t_{PC}	Page mode cycle time	170		225		275		ns	9
t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	10, 12
t_{CAC}	Access time from $\overline{CAS}$		100		135		165	ns	11, 12
t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	13
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ precharge time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	150	10000	200	10000	250	10000	ns	
t_{RSH}	$\overline{RAS}$ hold time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{RCD}	$\overline{RAS}$ to CAS delay time	20	50	25	65	35	85	ns	14
t_{CAS}	$\overline{CAS}$ pulse width	100		135		165		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	-20		-20		-20		ns	
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	-10		-10		-10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	50		70		85		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	50		70		85		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	15
t_{DH}	Data-in hold time	45		55		75		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page mode cycle only)	60		80		100		ns	
t_{REF}	Refresh period		2		2		2	ns	
t_{WCS}	$\overline{WRITE}$ command set-up time	-20		-20		-20		ns	16
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	16
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		175		ns	16

Notes:
1. T_{amb} is specified here for operation at frequencies to $t_{RC} \geq t_{RC\,(min)}$. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3} and I_{DD4} depend on cycle rate.
5. I_{CC1} and I_{CC4} depend upon output loading. During read out of high level data V_{CC} is connected through a low impedance to data out. At all other times I_{CC} consists of leakage currents only.
6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume t_T = 5 ns.
8. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
9. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_{amb} \leq 70°C$) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100 pF.
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta v}$ with Δv = 3 volts and power supplies at nominal levels.
18. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.

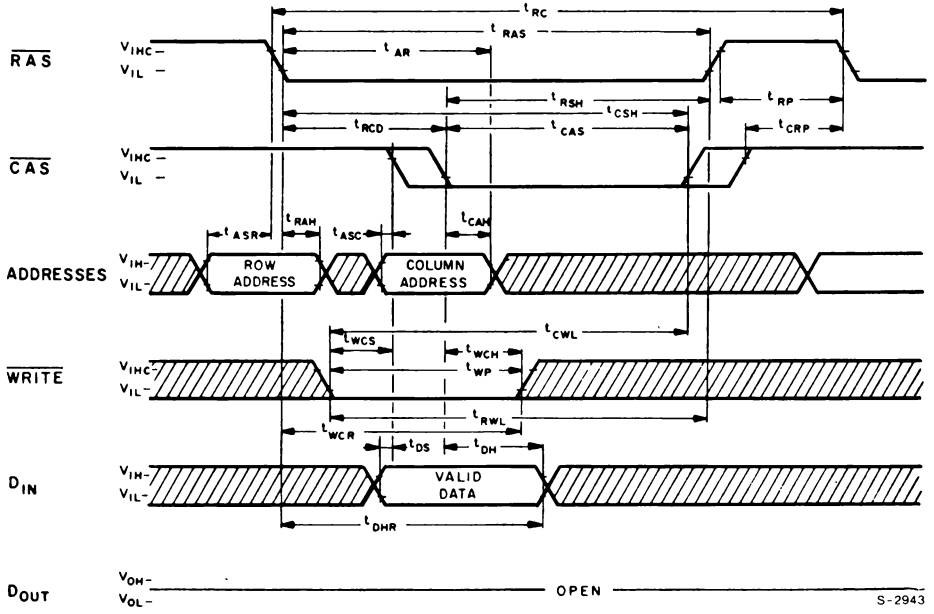
CAPACITANCES (T_{amb} = 0 to 70°C; V_{DD} = 12V ± 10%; V_{SS} = 0V; V_{BB} = -5.7 to -4.5V)

	Parameter	Min.	Typ.	Max.	Unit	Notes
C_{I1}	Input capacitance (A_0-A_6) DIN		4	5	pF	17
C_{I2}	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		8	10	pF	17
C_o	Output capacitance (D_{OUT})		5	7	pF	17, 18

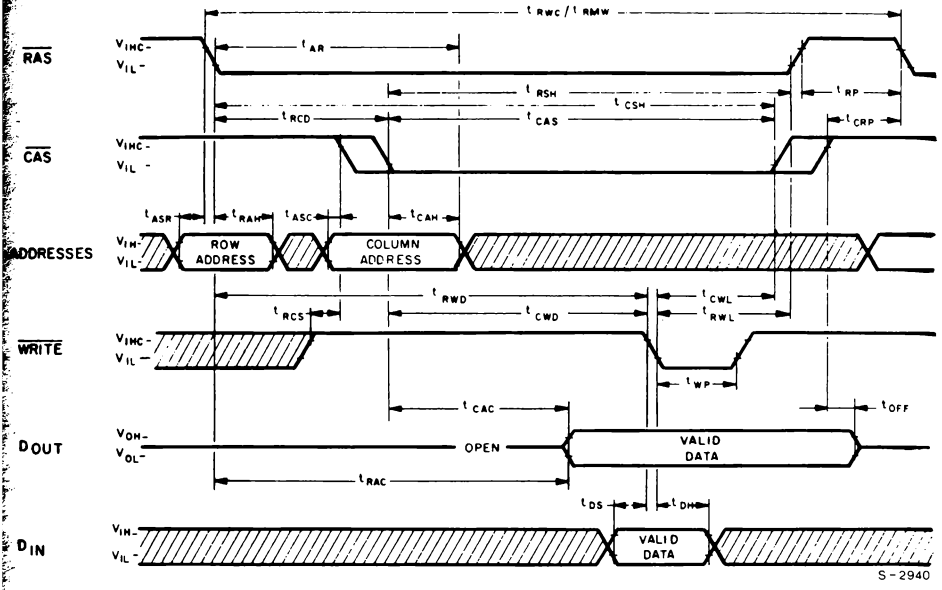
READ CYCLE



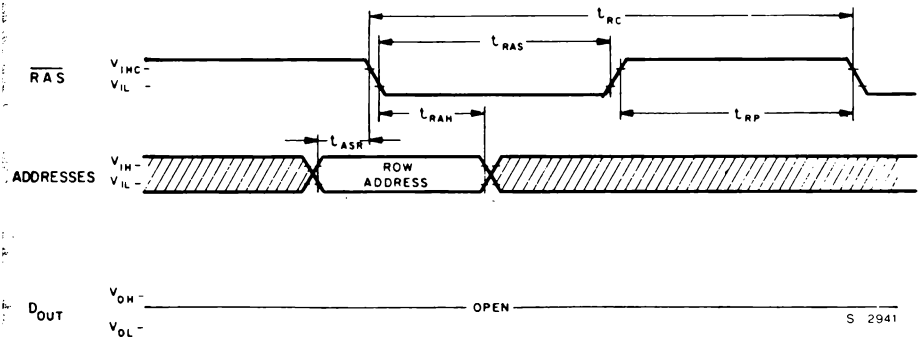
WRITE CYCLE (EARLY WRITE)



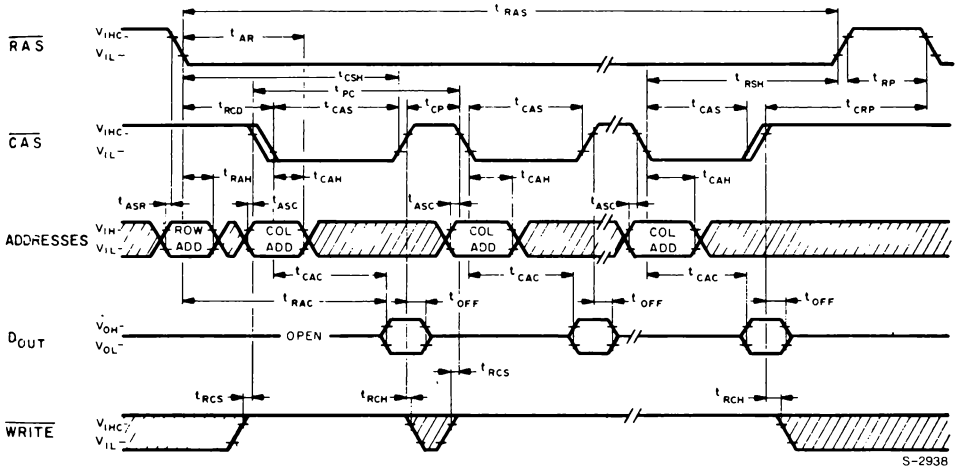
EAD-WRITE/READ-MODIFY-WRITE CYCLE



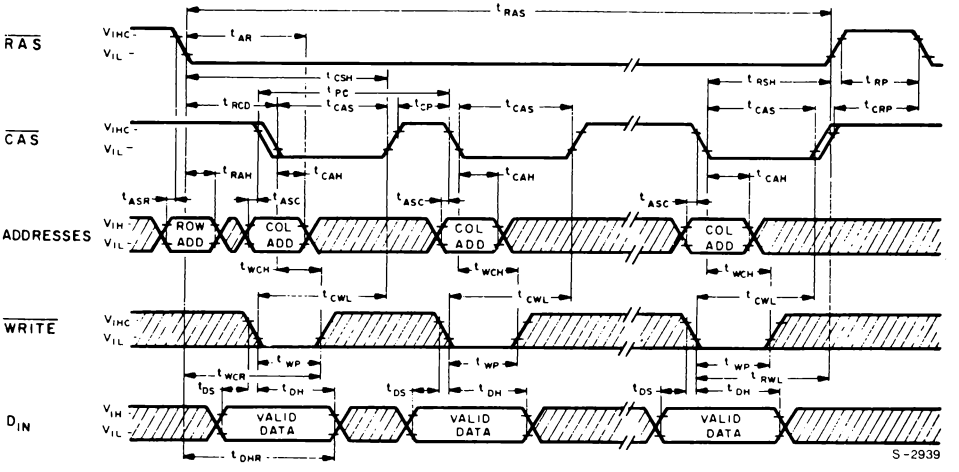
RAS-ONLY" REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DESCRIPTION

System oriented features include ±10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The M 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the M 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the M 4116 are multiplexed into the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information. Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the M 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the M 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

DATA OUTPUT CONTROL (continued)

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until CAS is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.
If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even through data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).
This type of output operation results in some very significant system implications.

Common I/O Operation – If all write operations are handled in the "early write" mode, then D_{IN} can be connected dorectly to D_{OUT} for a common I/O data bus.
D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the RAS/CAS clock timing relationship very flexible.
Two Methods of Chip Selection - Since D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X, Y) chip select array can be realized.
Extended Page Boundary - Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column location in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420Ω maximum and 135Ω typically. The resistance to V_{SS} (logic 0 state) is 95Ω maximum and 35Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the M 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the M 4116 allows for successive memory operations at multiplie column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.
The page boundary of a single M 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and the $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

EFRESH

efresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 w addresses within each 2 millisecond time interval. Although any normal memory cycle will perform e refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only fresh results in a substantial reduction in operating power. This reduction in power is reflected in the $_{D\,3}$ specification.

OWER CONSIDERATIONS

ost of the circuitry used in the M 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather an active duty cycle. This current characteristic of the M 4116 precludes inadverten burn out of the vice in the event that the clock inputs become shorted to ground due to system malfunction.
lthough no particular power supply noise restriction exists other than the supply voltages remain within e specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise sulting from the transient current of the device. This insures optimum system performance and reibility. Bulk capacitance requirements are minimal since the M 4116 draws very little steady state (DC) rrent.
n system applications requiring lower power dissipations, the operating frequency (cycle rate) of the 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be wered in accordance with the I_{DD1} (max) spec limit equation.

ote : The M 4116-4 is guaranteed to have a maximum I_{DD1} requirement of 35 mA @ 410 ns cycle with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20 mA with an ambient temperature range from 0° to 70°C.

lthough $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the M 4116 overall sysm power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state f $\overline{CAS}$.

OWER UP

he M 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating onditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, GS-ATES recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.
nder system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).
fter power is applied to be device, the M 4116 requires several cycles before proper device operation is chieved. Any 8 cycles which perform refresh are adequate for this purpose.

MOS INTEGRATED CIRCUIT

M 36000

PRELIMINARY DATA

4K-BIT READ ONLY MEMORY

8K x 8 ORGANIZATION - EDGE ENABLED OPERATION ($\overline{CE}$)
250 ns ACCESS TIME, 375 ns CYCLE TIME FOR M36000-4
300 ns ACCESS TIME, 450 ns CYCLE TIME FOR M36000-5
SINGLE +5V ±10% POWER SUPPLY
LOW POWER DISSIPATION: 220 mW MAX ACTIVE
LOW STANDBY POWER DISSIPATION: 35 mW MAX ($\overline{CE}$ HIGH)
ON CHIP LATCHES FOR ADDRESSES (CONTROLLED BY $\overline{CE}$ INPUT)
INPUTS AND THREE-STATE OUTPUTS - TTL COMPATIBLE
OUTPUT DRIVE 2 TTL LOADS AND 100 pF
STANDARD 24 PIN DIP (EPROM PIN OUT COMPATIBLE)

The M36000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. This device incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating *margins. The M36000* utilizes a static storage cell with clocked control periphery which allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 5 mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. The edge enabled operation means greater system flexibility and an increase in system speed, making this device ideally suited for 8 bit microprocessor systems such as those which utilize the Z80. It can offer significant cost advantages over PROM. The M36000 is available in 24-lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_i	Voltage on any pin with respect to Ground	-1 to +7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
T_{op}	Operating temperature	0 to +70	°C

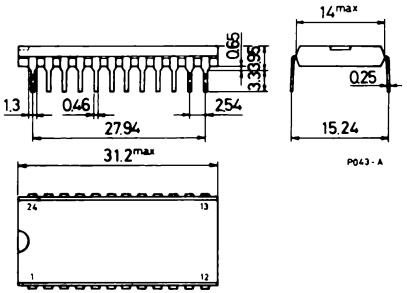
* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS:

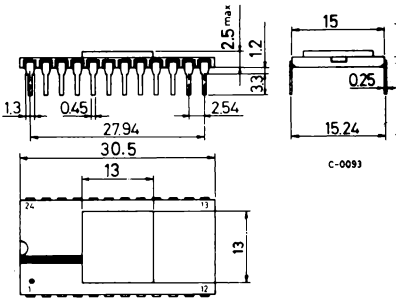
M36000 - 4 B1	for dual in-line plastic package
M36000 - 4 D1	for dual in-line ceramic package
M36000 - 4 F1	for dual in-line ceramic package, frit-seal
M36000 - 5 B1	for dual in-line plastic package
M36000 - 5 D1	for dual in-line ceramic package
M36000 - 5 F1	for dual in-line ceramic package, frit-seal

MECHANICAL DATA (dimensions in mm)

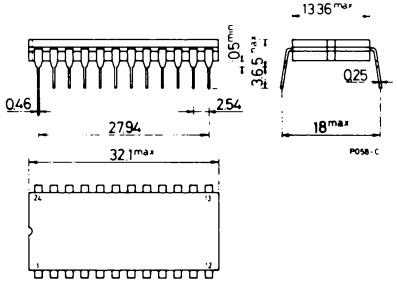
Dual in-line plastic package



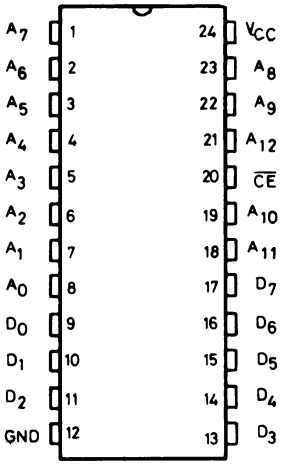
Dual in-line ceramic package



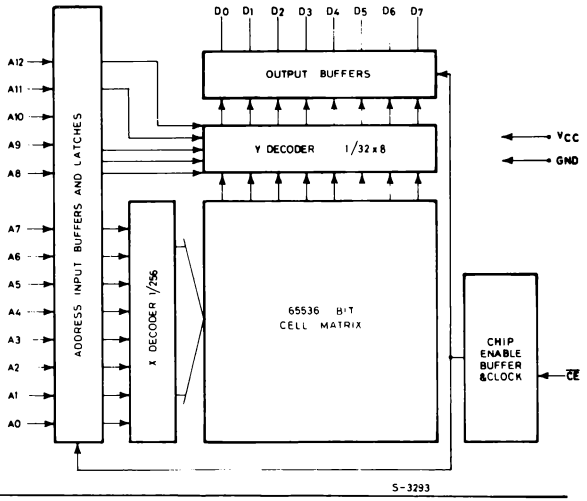
Dual in-line ceramic package, frit-seal



CONNECTION DIAGRAM



BLOCK DIAGRAM



ECOMMENDED DC OPERATING CONDITIONS[1] (T_{amb} = 0 to 70° C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	Input high voltage		2		V_{CC}	V
V_{IL}	Input low voltage		-1		0.8	V

TATIC ELECTRICAL CHARACTERISTICS[1] (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{OH}	Output high voltage	I_{OH} = -220 μA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 3.3 mA			0.4	V
I_{LI}	Input leakage current	V_I = 0 to 5.5V	-10		10	μA
I_{LO}	Output leakage current	Device unselected; V_o = 0 to 5.5V	-10		10	μA
I_{CC1}	Supply current (active)[2]				40	mA
I_{CC2}	Supply current (standby)	$\overline{CE}$ high			8	mA

YNAMIC ELECTRICAL CHARACTERISTICS[1] (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	M36000 - 4		M36000 - 5		Unit
			Min.	Max.	Min.	Max.	
t_C	Cycle time	Output load = 2 TTL gate and 100 pF, transition times = 20 ns	375		450		ns
t_{CE}	$\overline{CE}$ pulse width		250		300		ns
t_{AC}	$\overline{CE}$ access time			250		300	ns
t_{OFF}	Output turn off delay			60		75	ns
t_{AH}	Address hold time		60		75		ns
t_{AS}	Address setup time		0		0		ns
t_P	$\overline{CE}$ precharge time		125		150		ns

otes:

A minimum 100 μs time delay is required after the application of V_{CC} (+5V) before propex device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.

Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time.

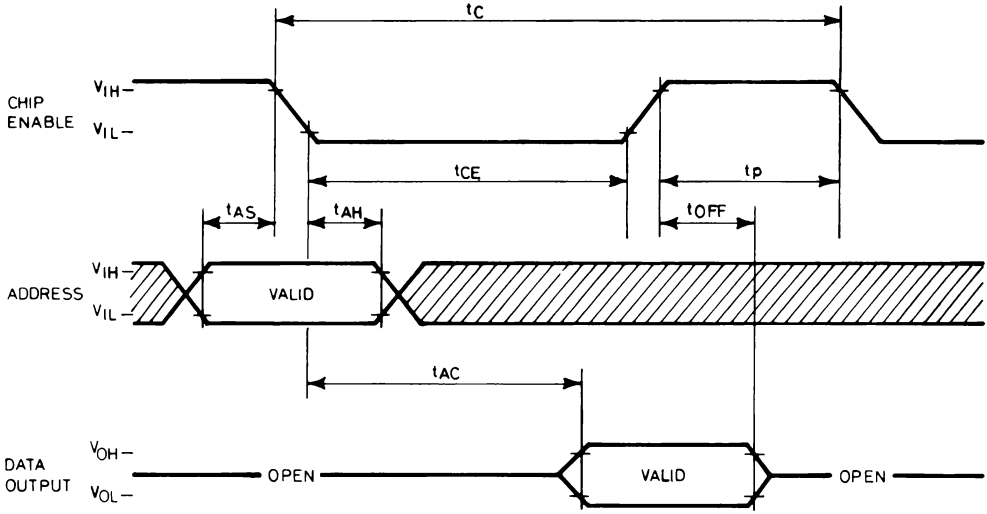
CAPACITANCE (T_{amb}= 0 to 70°C)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	Capacitance measured with Boonton Meter or effective value calculated from: $C=\frac{\Delta Q}{\Delta V}$ with $\Delta V = 3V$		5	8	pF
C_O	Output capacitance			7	15	pF

DESCRIPTION OF OPERATION

The M36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the onchip address registers. New address data can be applied in anticipation of the next cycle once the address hold time specification has been met. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

WAVEFORMS (One cycle)



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