1.0 INTRODUCTION

This specification defines the physical and electrical interface of the SA1200 Data Separator. The physical interface specifies the mechanical requirements as well as lists the recommended parts. The electrical interface describes the function and timing relationship of each I/O pin. The SA1200 may be used to interface as many as four SA1000 fixed disk drives.

2.0 PHYSICAL INTERFACE

There are six connector ports available on the SA1200: The first four connectors (J1, J2, J3, J4) provide radial SA1000 drive interface of read/write data signals; the fifth connector (J5) provides controller interface of control and data signals; and the sixth connector (J6) provides for DC power. Refer to Figure 3 for connector locations.

2.1 J1/P1, J2/P2, J3/P3, and J4/P4 CONNECTORS

Connections to J1 thru-J4 are through four 20 pin PCB edge connectors. The dimensions for one of these connectors are shown in Figure 1. The pins are numbered 1 through 20 with the even numbered pins on the component side of the PCB. The recommended mating connectors (P1, P2, P3, and P4) are either Scotchflex ribbon connector P/N 3461-0001 or AMP P/N 583717-1 with AMP contacts P/N 1-583616-1. A KEY SLOT is provided between pins 4 and 6.

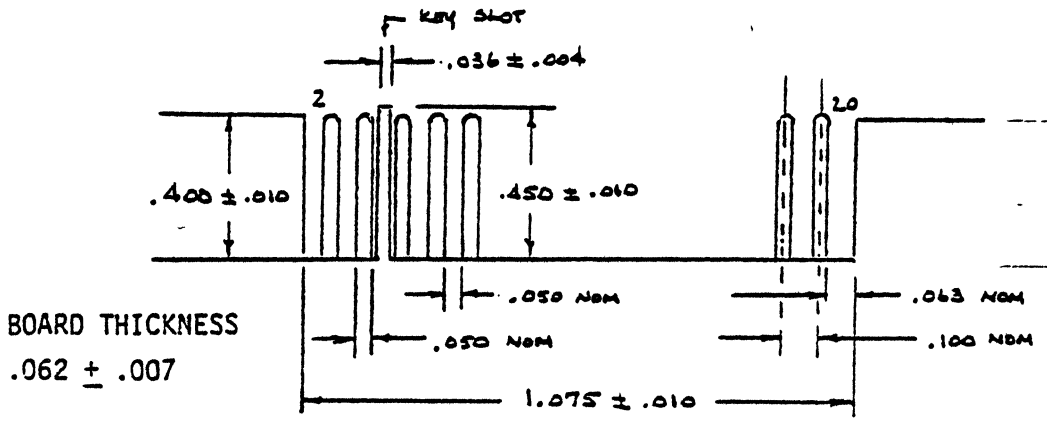


Figure 1. J1, J2, J3, and J4 CONNECTOR DIMENSIONS

Although any SA1000 drive/connector combination may be used, the following connector assignment is recommended:

J1/P1 = Drive 1
J2/P2 = Drive 2
J3/P3 = Drive 3
J4/P4 = Drive 4

2.2 J5/P5 CONNECTOR

Connection to J5/P5 is through a 20 pin PCB edge connector as described in paragraph 2.1. The physical dimensions are identical, except the KEY SLOT is provided between pins 8 and 10.

2.3 J6/P6 CONNECTION

DC power connector (J6) is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0 mounted on the component side of the PCB. The recommended mating connector (P6) is AMP P/N 1-480270 utilizing AMP pins P/N 60619-1. J5 pins are labeled on J5 connector, and shown in Figure 2.

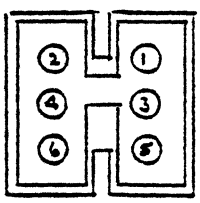


Figure 2. J5 CONNECTOR (COMPONENT SIDE)

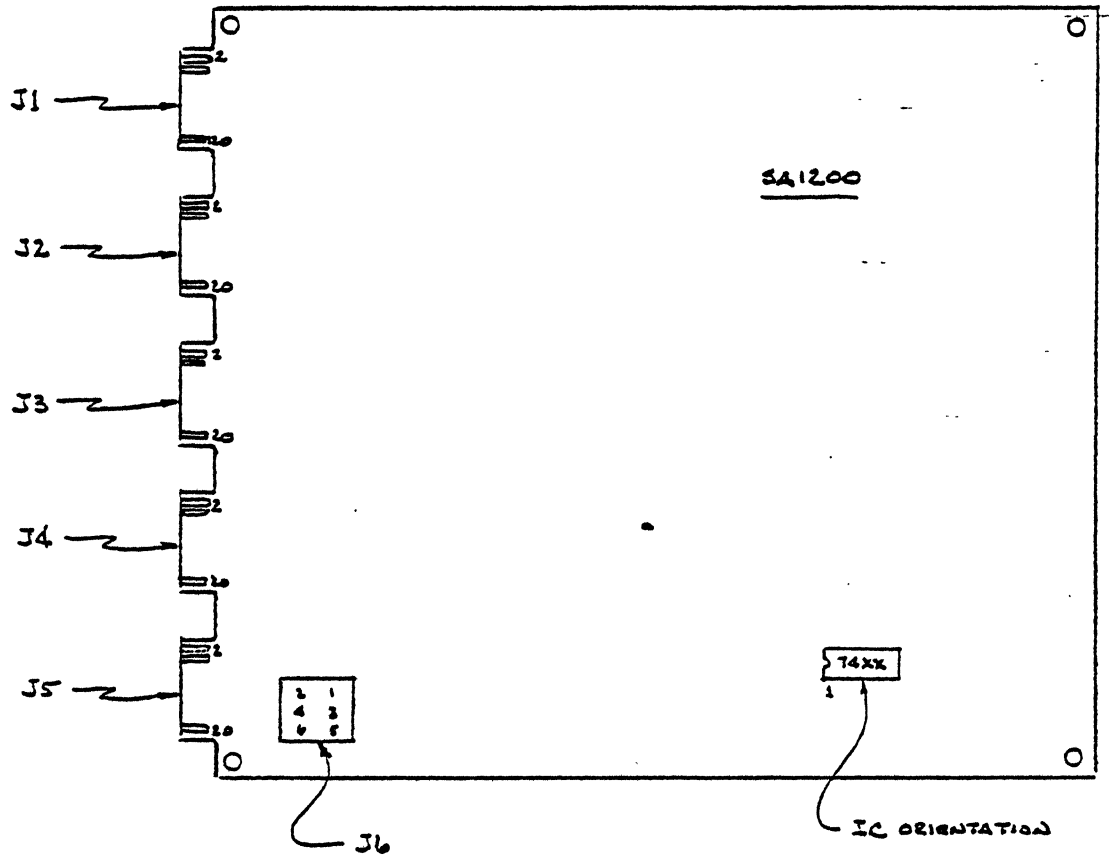


Figure 3. INTERFACE CONNECTOR PHYSICAL LOCATION

3.0 INTERFACE LINES AND PIN ASSIGNMENTS

The data separator interface may be divided into two categories: Signal, and DC power. Tables I, II, and III define the pin assignments for these interface lines. Table IV shows the recommended cable types. A typical four SA1000 drive system is diagrammed in Figure 4.

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	- DRIVE SELECTED
4	3	SPARE
6	5	SPARE
	7	SPARE
8		GND
	9	+ TIMING CLK
	10	- TIMING CLK
11		GND
12		GND
	13	+ MFM WRITE DATA
	14	- MFM WRITE DATA
15		GND
16		GND
	17	+MFM READ DATA
	18	-MFM READ DATA
19		GND
20		GND

TABLE I.

J1/P1, J2/P2, J3/P3, J4/P4

CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	- READ GATE
4	3	- AMF
6	5	- WRAM
	7	- EWC
8		GND
	4	+ NRZ WRITE DATA
	10	- NRZ WRITE DATA
11		GND
	12	+ WRITE CLOCK
	13	- WRITE CLOCK
14		GND
	15	+ READ CLOCK
	16	- READ CLOCK
17		GND
	18	+ NRZ READ DATA
	19	- NRZ READ DATA
20		GND

TABLE II.

J5/P5 CONNECTOR PIN ASSIGNMENT

	VOLTAGE		GROUND
PIN 1	+24 VOLTS DC	PIN 2	+24 VOLT RETURN
PIN 4	-7 to -16 (-5 OPT) VOLTS	PIN 3	-7 to -16 (-5 OPT) VOLT RETURN
PIN 5	+5 VOLTS	PIN 6	+5 VOLT RETURN

TABLE III.

P6 - DC CONNECTOR PIN ASSIGNMENTS

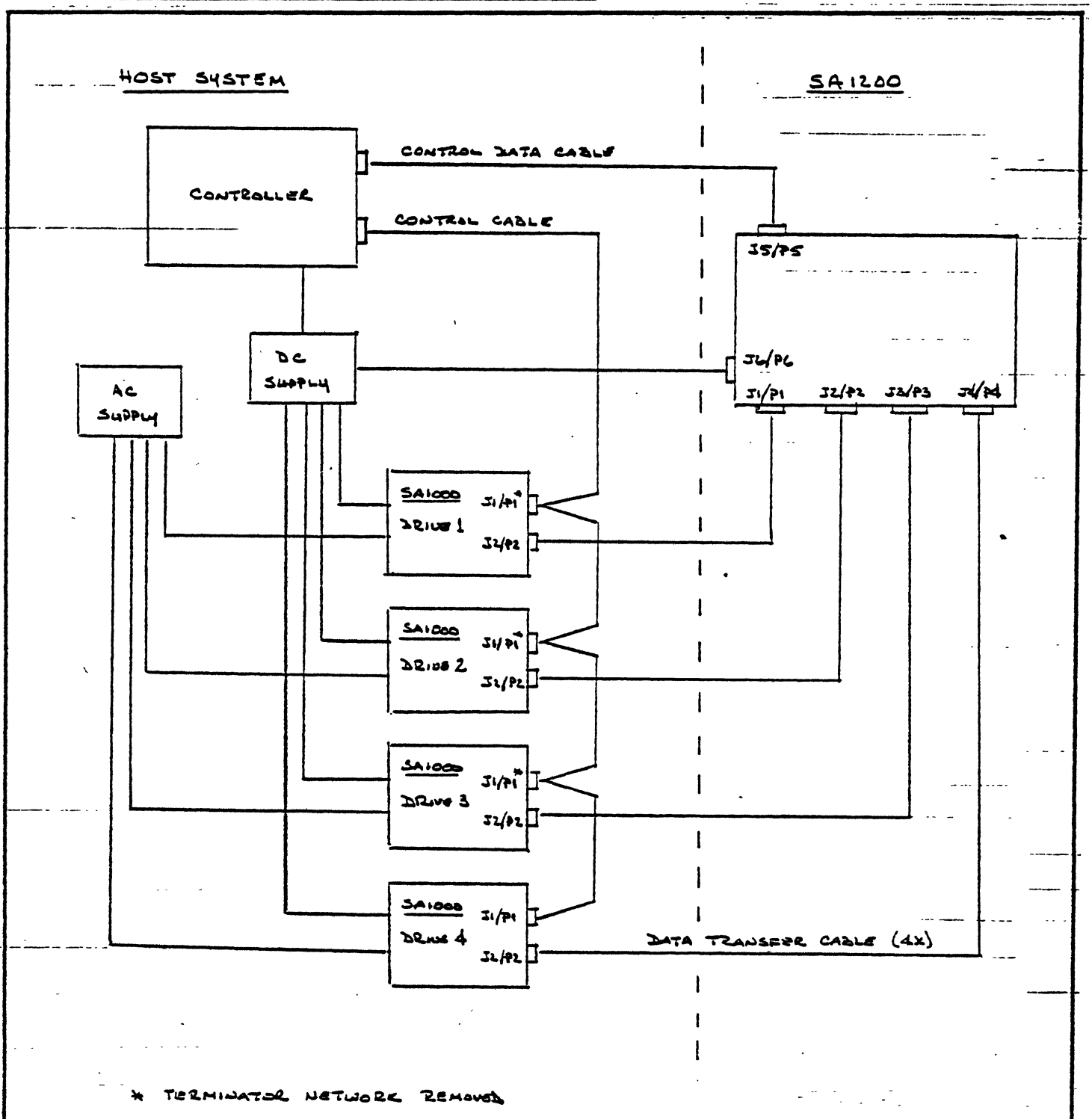


Figure 4. TYPICAL CONNECTION - 4 DRIVE SYSTEM

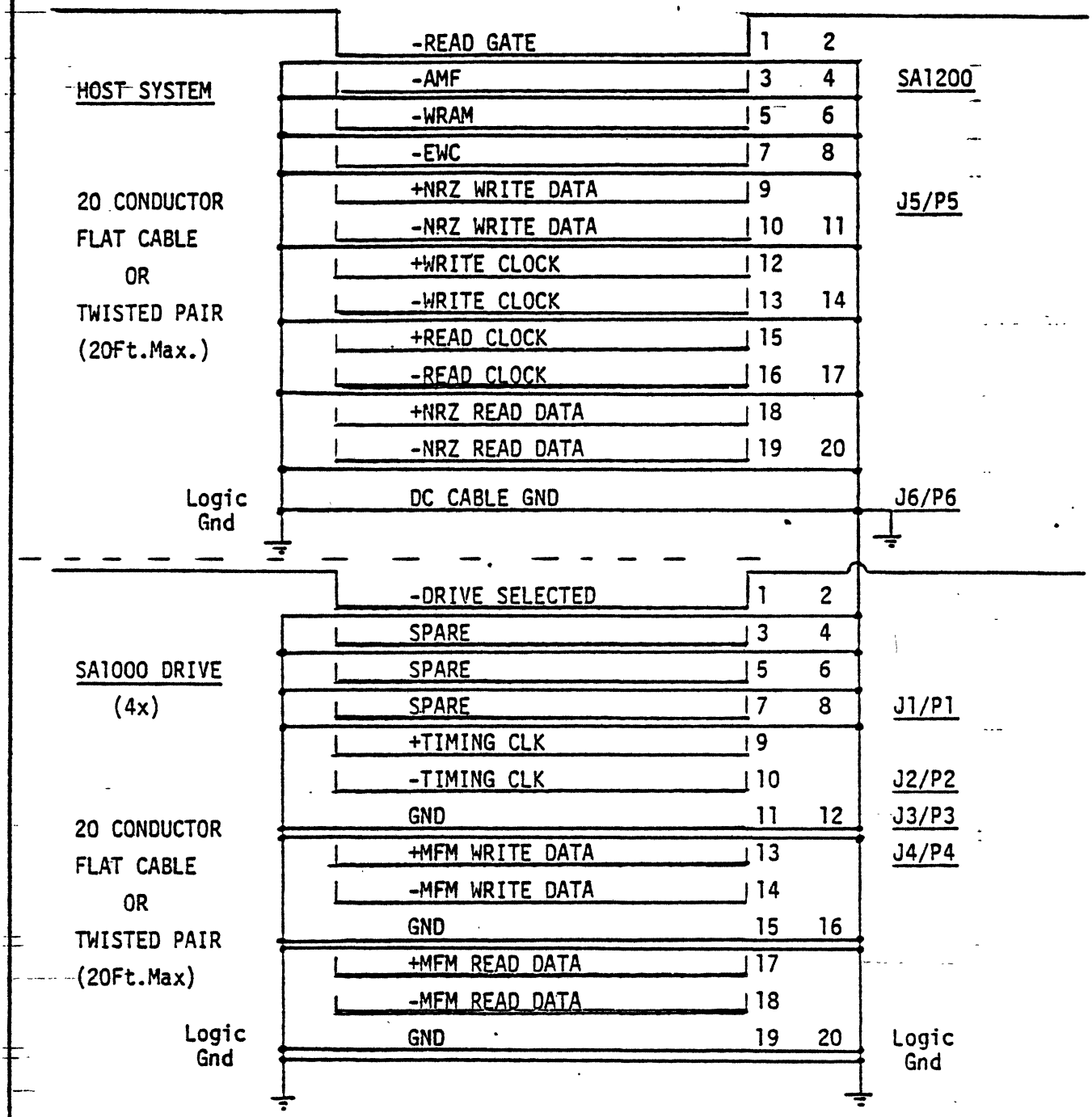


TABLE IV. INTERFACE CONNECTION -
CONTROLLER/DATA SEPARATOR/MULTIPLE DRIVE SYSTEM

4.0 SIGNAL INTERFACE

The signal interface consists of two categories: Control, and data transfer. All control lines are TTL in nature and either provide signals to the SA1200 (input), or provide signals from the SA1200 (output). The data transfer signals are differential in nature, and provide data and clock signals either to or from the SA1200. Both categories of signals are present at all signal connector ports.

4.1 CONTROL INPUT LINES

The control input lines have the following electrical specifications:

True = 0.0 VDC to 0.4 VDC @I in. = 40 mA (max)

False = 2.5 VDC to 5.25 VDC @I in. = 0 mA (open)

Figure 5 shows the recommended control signal driver/receiver combination.

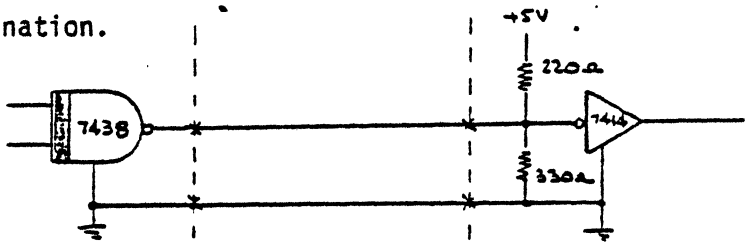


Figure 5. CONTROL SIGNAL DRIVER/RECEIVER COMBINATION

4.1.1 DRIVE SELECTED

This signal is present at the J1, J2, J3, and J4 connector ports and is an input control signal to the SA1200 from each of the SA1000 drives. The true state of DRIVE SELECTED enables the read data receiver for that particular drive, so that the SA1200 would be locked to and separating the data of the selected drive alone. Conversely, the false state inhibits that particular read data receiver so no data would be present at the SA1200 for that particular drive.

4.1.2 READ GATE

The active state of this signal, or logical zero level, enables the read operation of the data separator for the selected SA1000 drive by activating the read data receivers, enabling the VFO, and inhibiting the write data receivers. Conversely, the inactive state of this signal, or logical one level, enables write data to be transferred from the controller, as well as inhibits read data to be accepted by the SA1200.

4.1.3 WRAM (WRITE ADDRESS MARK)

This signal is requested from the controller to set the write address mark FF whenever an address mark is to be encoded on the SA1000 drive. The write address mark FF is set at each logical one to logical zero transition or leading edge of this signal pulse. The recommended address mark for the SA1000 drive is the following: DATA = $(A1)_{16}$, and CLOCK = $(0A)_{16}$. See Appendix A for WRITE ADDRESS MARK timing.

4.1.4 EWC (ENABLE WRITE COMPENSATION)

The active state of this control line provides for write data precompensation of both data and clock bits. It is recommended that this line is set true whenever writing on any SA1000 drive for cylinder locations 128 through 255, and is set false for cylinder locations ØØØ to 127. The recommended early/late precompensation time is 12 ns. See Appendix A for write precompensation analysis.

4.2 CONTROL OUTPUT LINE

The control output signals are driven with an open collector output stage capable of sinking a maximum of 40 mA at logical zero or true state with a maximum voltage of 0.4 v measured at the driver. When the line driver is in logical one or false state, the driver transistor is off and the collector cutoff current is a maximum of 250 microamperes. See Figure 5 for the recommended control signal driver/receiver combination.

4.2.1 AMF (ADDRESS MARK FOUND)

This interface signal is provided by the SA1200 to indicate that an address mark of the following format has been detected: DATA = $(A1)_{16}$, and CLOCK = $(0A)_{16}$. This signal is an output of a FF with each logical one to logical zero transition or leading edge may be used to indicate detection of an address mark and will remain in this true state until READ GATE becomes false. See Appendix B for timing requirements. Note that there is a one cell delay until the NRZ Data will indicate the proper address mark of $(A1)_{16}$. In addition, if the address mark is not found after sixteen bytes of zeros, the start logic is reset and search for AM is restarted.

4.3 DATA TRANSFER LINES

All lines associated with the transfer of data either between the SA1200 and the SA1000 drive(s) or the SA1200 and the host system are differential in nature and may not be multiplexed. These data lines are present on connectors J1/P1, J2/P2, J3/P3, J4/P4, and J5/P5.

Three pairs of balanced signals are used for data transfer for each SA1000 drive at connectors J1/P1, J2/P2, J3/P3, and J4/P4. They are MFM WRITE DATA, MFM READ DATA, and TIMING CLK.

The host system interface connector, J5/P5, has four differential data transfer pairs. These are NRZ WRITE DATA, WRITE CLOCK, READ CLOCK, and NRZ READ DATA. Figure 6 illustrates the driver/receiver combination used in the SA1200 data separator.

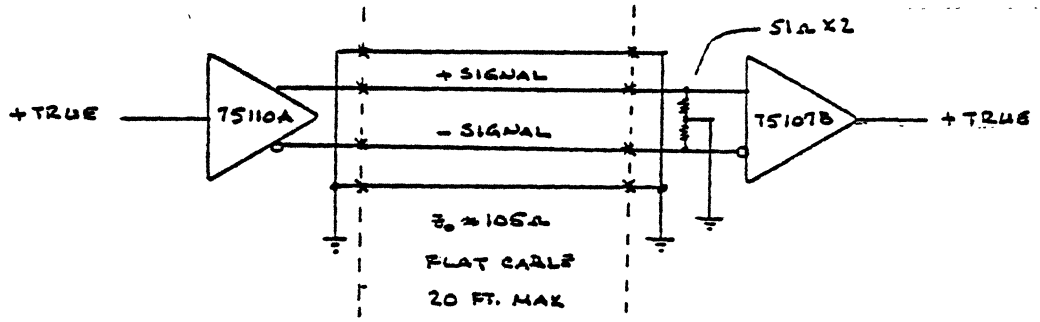


Figure 6. DATA LINE DRIVER/RECEIVER (POSITION LOGIC)

4.3.1 MFM WRITE DATA

This differential pair defines the transitions to be written on the track by the SA1000 drive. The transition of +MFM WRITE DATA line going more positive than the -MFM WRITE DATA line will cause a flux reversal at the SA1000 drive provided the proper write sequence is instituted. This signal must be disabled and quiet during any read operation. Figure 7 shows the timing for MFM WRITE DATA. The actual occurrence of the flux reversals may differ due to write precompensation. The recommended write precompensation time is ± 12 ns. Also, see Appendix A for write address mark timing.

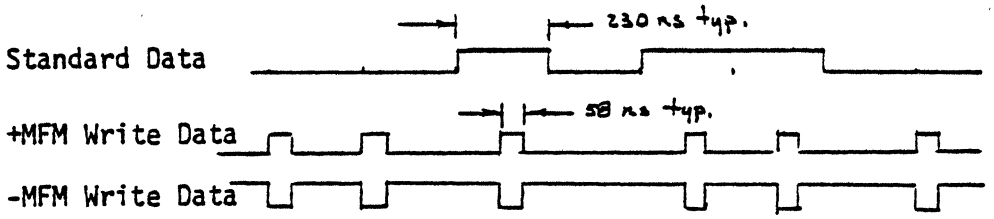


Figure 7. MFM WRITE DATA TIMING

4.3.2 MFM READ DATA

The serial decoded data stream is received at the SA1200 from the SA1000 drive via the differential pair of MFM READ DATA lines. The transition of the +MFM READ DATA line going more positive than the -MFM READ DATA line represents a flux reversal provided that READ GATE is active. The timing for MFM READ DATA is shown in Figure 8.

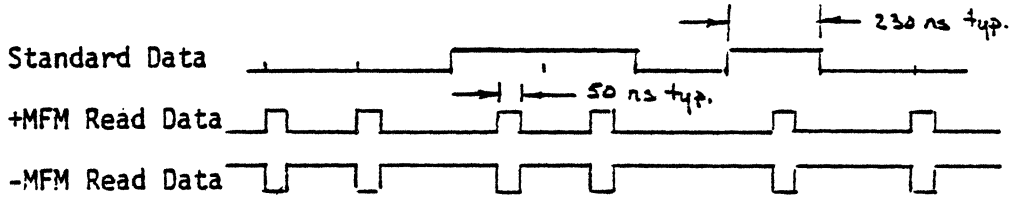


Figure 8. MFM READ DATA TIMING

4.3.3 TIMING CLK

The differential pair of TIMING CLK consists of clock signals with 50% duty cycle and 3.6866 µs ± 0.1% period. This clock is generated at the SA1200 and sent to the SA1000 drive(s) at a frequency of 1/16 times the standard write data bit frequency. The phase relationship between the TIMING CLK and MFM WRITE DATA may not be maintained, since this signal is utilized by the SA1000 drive(s) for other than data encode/decode functions. However, it is imperative to maintain this frequency change to less or equal to ± 0.1%.

4.3.4 NRZ WRITE DATA

This differential pair provides the drive with data to be written on the track in standard (non-return to zero) format. When the +NRZ WRITE DATA line is more positive than the -NRZ WRITE DATA line, a logical "one" is present on the line; the inverse is a logical "zero". This signal is sampled by the SA1200 on the trailing edge of each WRITE CLOCK pulse. See Figure 9 for MFM encoding timing relationships.

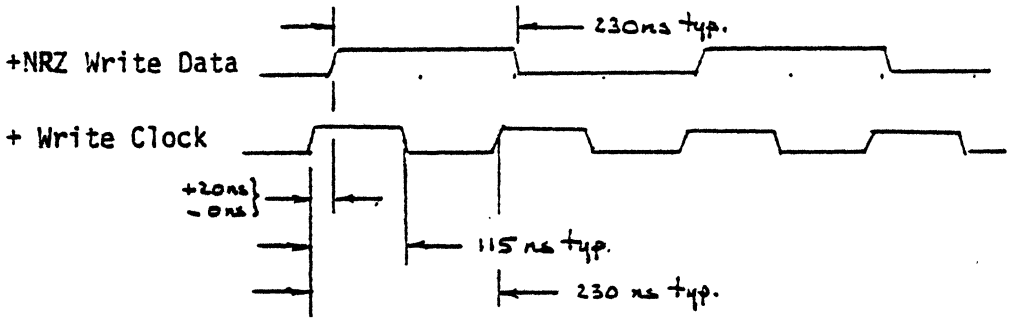


Figure 9. MFM ENCODE TIMING

4.3.5 WRITE CLOCK

This differential pair is used by the SA1200 to sample the NRZ WRITE DATA. The host system is requested to change the NRZ WRITE DATA lines at the leading edge of WRITE CLOCK, since the SA1200 utilizes the trailing edge to sample the NRZ WRITE DATA. See Figure 9 for timing relationship.

4.3.6 READ CLOCK

When READ GATE is false, or logical one, this differential pair carries to the host system a crystal clock signal of 4.34 MHz and 50% duty cycle which may be used as the host's WRITE CLOCK, as well as the NRZ WRITE DATA strobe. The host must be careful to insure proper timing and delays to meet the MFM encoding timing requirements.
When READ GATE is true, or logical zero, this differential pair will carry the SA1200 separator clock of 25% duty cycle derived from the actual read data bits, provided that the start logic has correctly sunk up, ie +CNT 80 high at the SA1200. See Appendix B for timing requirements, as well as Figure 10.

4.3.7 NRZ READ DATA

This differential pair provides the host system with the read data in standard format. The NRZ READ DATA will not be valid until 20.3 µs after activating READ GATE, provided that the READ GATE is enabled in a known area of all zeros or all ones. See Appendix B for timing requirements, and Figure 10. NRZ READ DATA should be clocked with the leading edge, or high to low transition of READ CLOCK at the host system.

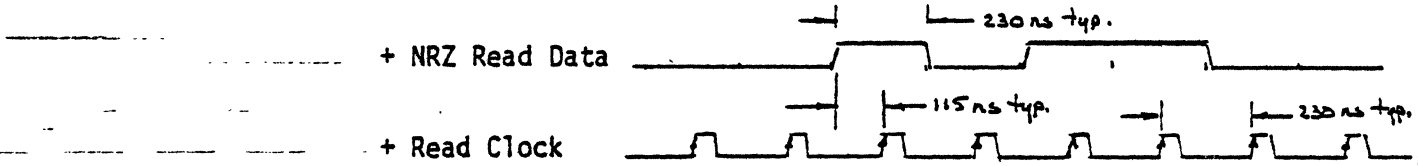


Figure 10. NRZ READ DATA DECODE TIMING

5.0 GENERAL TIMING REQUIREMENTS

The timing requirements found in Appendixes A and B show the general sequence of events for proper operation.

6.0 POWER INTERFACE

The SA1200 data separator requires the following DC voltages via connector J6/P6.

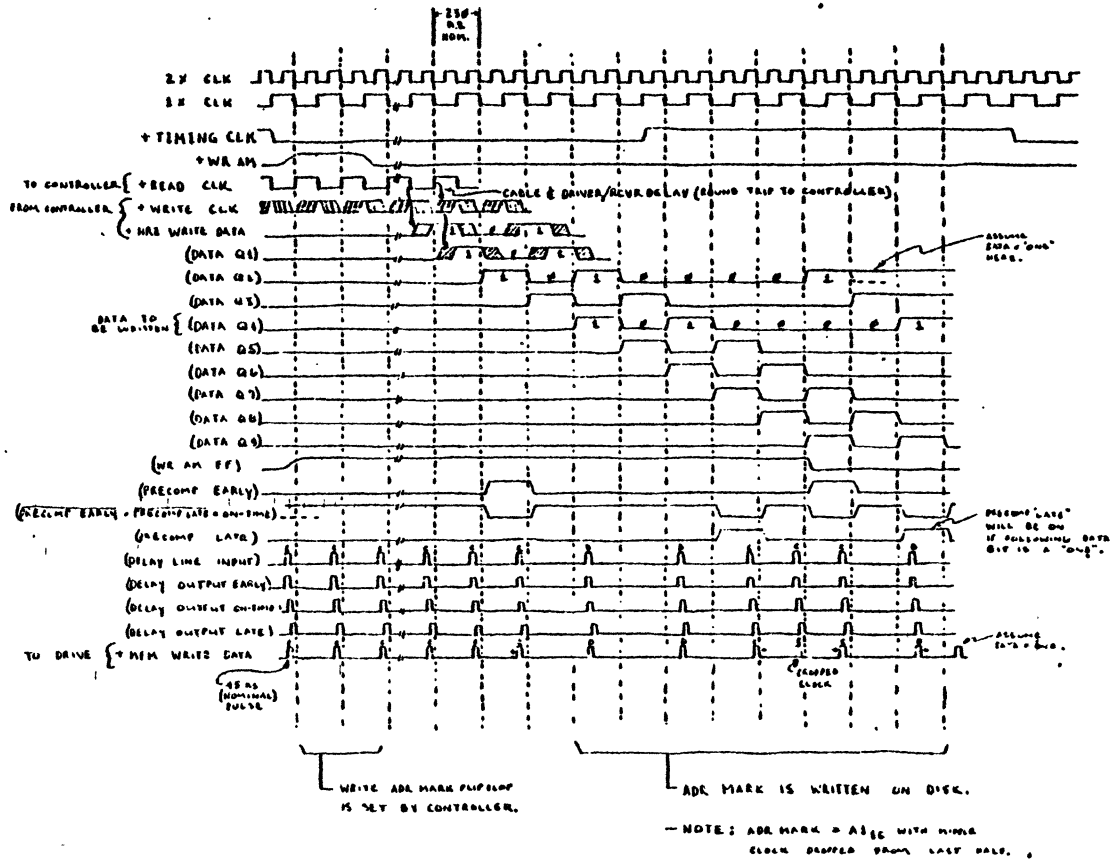
(1) +5.00 ± 0.25 VDC @ 2.04 max, i.5A typical, 50 mVpp max, ripple,

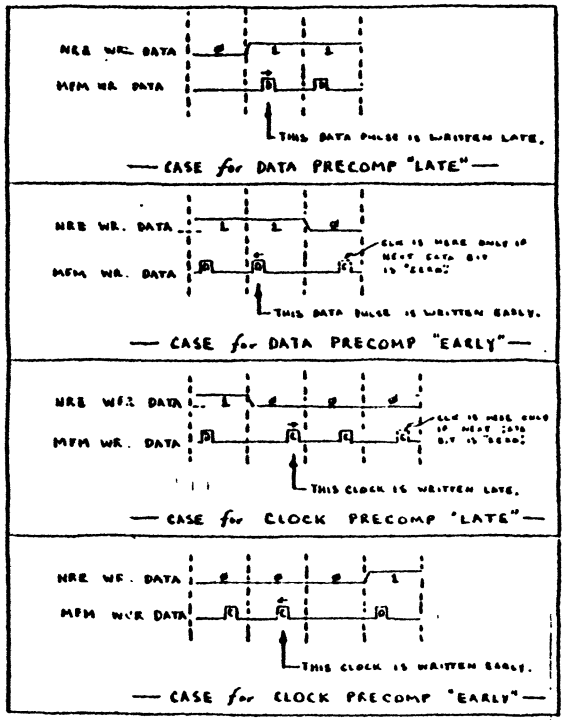
(2) -7 to -16 VDC @ 0.50A max., 0.35 A typical, 100 mVpp, max. ripple.
Optional: -5V ± 0.25 VDC @ 0.50 A max., 0.35 A typical, 50 mVpp, max. ripple

(3) +24V ± 2.4 VDC @ 0.20 A max., 0.15 A typical, 1Vpp max. ripple.

7.0 PHYSICAL OUTLINE

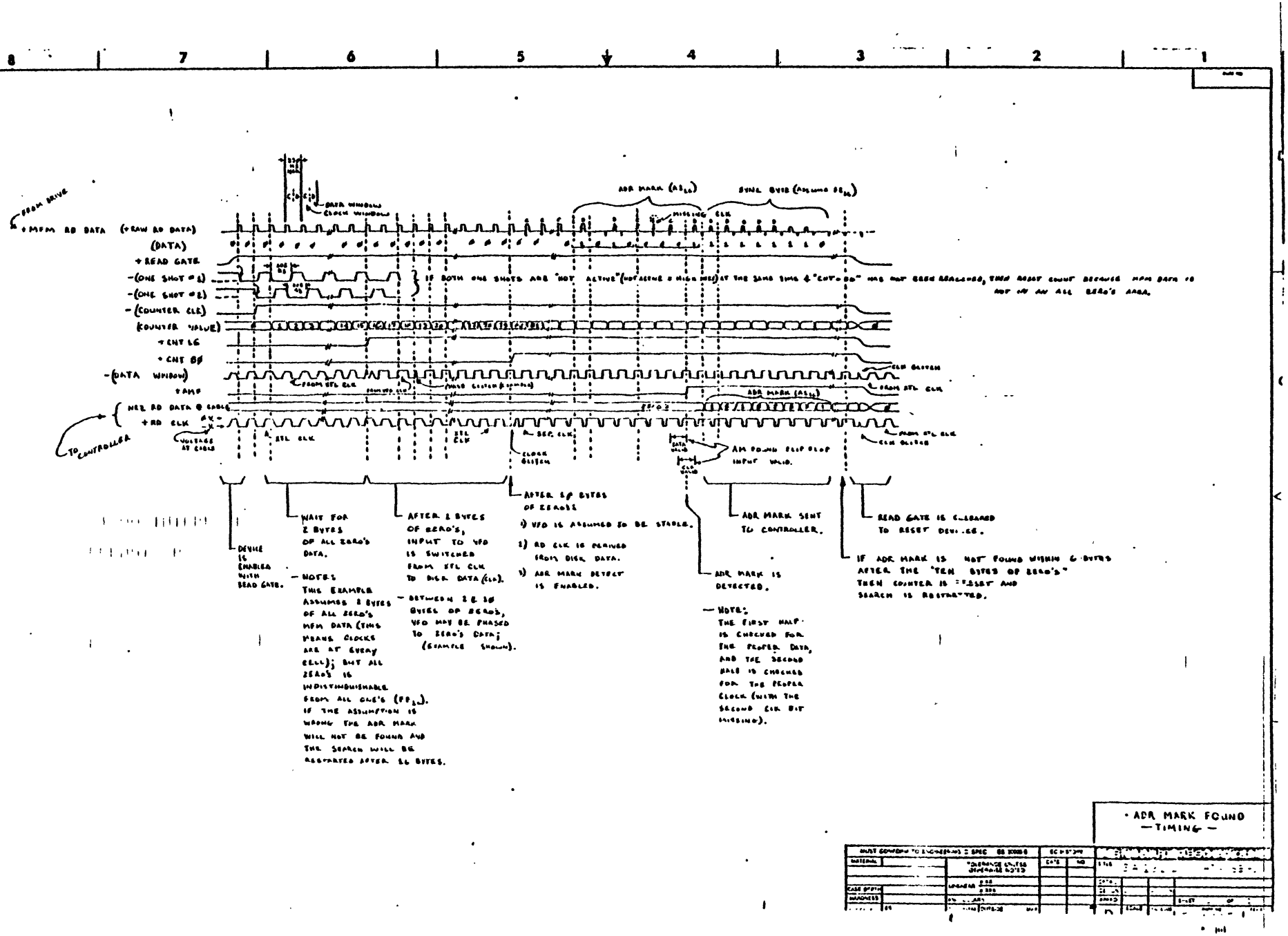
The physical dimensions for the SA1200 is shown on Appendix C.

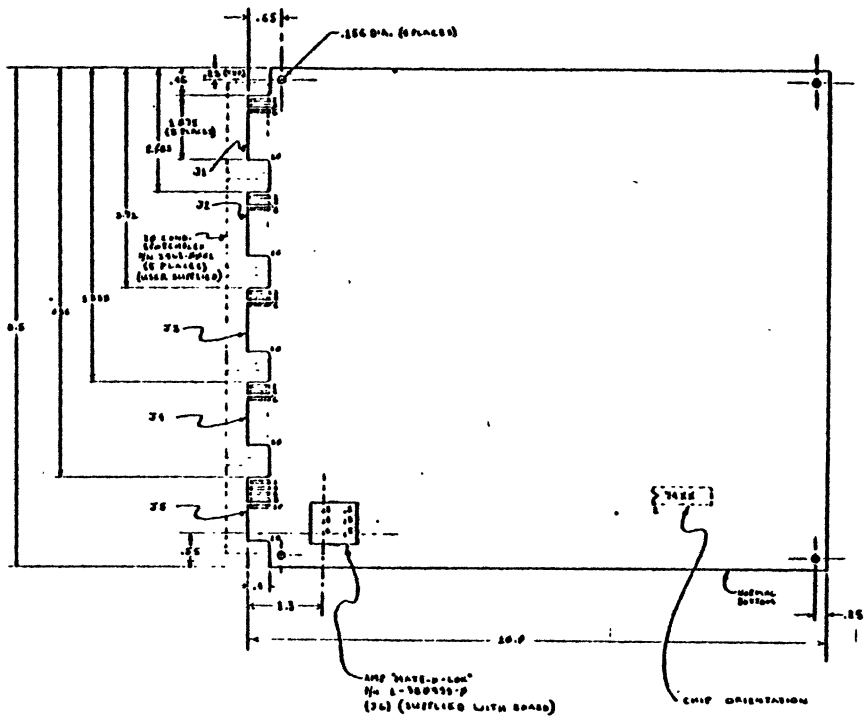




— WRITE PRECOMP ANALYSIS —

+WRITE ADR MARK —TIMING—
+WRITE PRECOMP ANALYSIS


8
7
6
5
4
3
2
1
D
C
B
A
FROM DRIVE
+MFM RD DATA (+RAW RD DATA)
(DATA)
+READ GATE
-(ONE SHOT #1)
-(ONE SHOT #2)
-(COUNTER CLK)
(COUNTER VALUE)
+CNT 16
+CNT 80
-(DATA WINDOW)
+AMP
NRZ RD DATA & CABLE
+RD CLK
TO CONTROLLER
VOLTAGE AT CABLE
DATA WINDOW
CLOCK WINDOW
ADR MARK (AS16)
SYNC BYTE (ASSUME FB16)
MISSING CLK
IF BOTH ONE SHOTS ARE "NOT ACTIVE" (NOT ACTIVE = HIGH HERE) AT THE SAME TIME & "CNT=80" HAS NOT BEEN REACHED, THIS MUST COUNT BECAUSE MFM DATA IS NOT AN ALL ZERO'S AREA.
FROM VFO CLK
FROM STL CLK
CLOCK GLITCH
ADR MARK (AS16)
AM FOUND FLIP FLOP INPUT VALID.
DATA VALID
CLK VALID
STL CLK
STL CLK
SEC CLK
CLOCK GLITCH
DENIBE IS ENABLED WITH READ GATE.
WAIT FOR 2 BYTES OF ALL ZERO'S DATA.
- NOTE: THIS EXAMPLE ASSUMES 2 BYTES OF ALL ZERO'S MFM DATA (THIS MEANS CLOCKS ARE AT EVERY CELL); BUT ALL ZERO'S IS INDISTINGUISHABLE FROM ALL ONE'S (FF16). IF THE ASSUMPTION IS WRONG THE ADR MARK WILL NOT BE FOUND AND THE SEARCH WILL BE RESTARTED AFTER 16 BYTES.
AFTER 2 BYTES OF ZERO'S, INPUT TO VFO IS SWITCHED FROM STL CLK TO DISK DATA (CLK).
- BETWEEN 2 & 10 BYTES OF ZERO'S, VFO MAY BE PHASED TO ZERO'S DATA; (EXAMPLE SHOWN).
AFTER 10 BYTES OF ZEROS
1) VFO IS ASSUMED TO BE STABLE.
2) RD CLK IS DERIVED FROM DISK DATA.
3) ADR MARK DETECT IS ENABLED.
ADR MARK IS DETECTED.
- NOTE: THE FIRST HALF IS CHECKED FOR THE PROPER DATA, AND THE SECOND HALF IS CHECKED FOR THE PROPER CLOCK (WITH THE SECOND CLK BIT MISSING).
ADR MARK SENT TO CONTROLLER.
READ GATE IS CLEARED TO RESET DEVICE.
IF ADR MARK IS NOT FOUND WITHIN 6 BYTES AFTER THE "TEN BYTES OF ZERO'S" THEN COUNTER IS RESET AND SEARCH IS RESTARTED.
• ADR MARK FOUND —TIMING—



NOTES:

1) EVEN EDGE PIN #'S ON COMPONENT SIDE OF BOARD.

2) J1 =
J2 =
J3 =
J4 = } CONNECTIONS for DRIVES #1,2,3 & 4 (UNIT #USER)
J5 = CONTROLLER CONNECTION
J6 = POWER CONNECTION

3) ALL DIMENSIONS FOR REFERENCE ONLY.

— COMPONENT SIDE —

* PCB FAB NOTES