SA 1000

DATA SEPARATOR GUIDE

AND

RECOMMENDED TRACK FORMAT

1.0 Track Format

The purpose of a format is to organize a data track into smaller, sequentially numbered, blocks of data called sectors. The SA1000 format is a soft sectored type of format which means that the beginning of each sector is defined by a prewritten identification (I.D.) field which contains the physical sector address, plus cylinder and head information. The I.D. field is then followed by a user data field.

The soft sectored format is a slightly modified version of the I.B.M. system 34 double density which is commonly used on 8 inch floppy disk drives. The encoding method used here is modified frequency modulation (MFM).

In the example shown (figure 1), each track is divided into 32 sectors. Each sector has an adjacent data field of 256 bytes in length.

The beginning of both the I.D. field and the data field are flagged by unique characters called address marks.

An address mark is 2 bytes in length. The first byte is always an "A1" data pattern. This is followed by either an "FE" pattern which is the pattern used to define an I.D. address mark, or an "F8" which is a data address mark pattern.

The "A1" pattern is made unique by violating the encode rules of MFM by omitting one clock bit. This makes the address mark pattern

unique to any other serial bit combination.

Each I.D. and data field are followed by a 16 bit cyclic redundancy check (CRC) character used for data verification. Each CRC polynomial is unique for a particular data pattern.

Surrounding the I.D. and data fields are gaps called Interrecord gaps.

1.1 Gap Length Calculations

1.1.1 Gap 1

Gap 1's purpose is to provide a head switching recovery period so that when switching from one track to another, sequential sectors may be read without waiting the rotational latency time. Gap 1 should be at least 11 bytes long which corresponds to the head switching time of 20 microseconds. Gap 1 is immediately followed by a sync field for the I.D. field of the first sector.

1.1.2 Gap 2

Following the I.D. field, and separating the I.D. field from the data field, is gap 2. Gap 2 provides a known area for the data field write update splice to occur. The remainder of this gap also serves as the sync up area for the data field address mark. The length of gap 2 is determined by the data separator lock up performance (see section 2.2).

1.1.3 Gap 3

Gap 3, following the data field, is a speed variation tolerance area. This allows for a situation where a track has been formatted

while the disk is running 3% slower than nominal, then write updated with the disk running 3% faster than nominal (power line variations).

Gap 3 should be at least 15 bytes in length.

1.1.4 Gap 4

Gap 4 is a speed tolerance buffer for the entire track. This allows the disk to rotate at least 3% faster than normal without overflowing the track during the format operation. The format operation which writes the I.D. fields, begins with the first encountered index and continues to the next index.

2.0 Data Separator Design Considerations

The current scheme for reliable data separation of MFM encoding is an analog phase lock loop (PLL) which locks to the serial data stream and creates a window around the expected position of the data/clock bit.

The PLL should be designed to track and aquire a data frequency variation of at least $\pm$3% from nominal. The nominal data transfer rate is 4.34 megabits/ second.

During the time that the PLL is not locked to the read data, it should be locked to a stable frequency equal to the basic data rate. This is done to insure that when the PLL is required to lock on to read data, the PLL is running at the nominal frequency which minimizes the PLL lock up time.

2.1 Loop Characteristics

The PLL loop characteristics should result in a critically

damped response to a step change in input frequency. Pole-zero ratios for this type of design are typically in the range of 10-20 to 1. Loop gain can then be optimized to the desired transient response.

2.2 Sync Up Fields

The minimum length of the sync up field are directly related to loop bandwidth.

In the format example in figure 1, the lock up time to a step frequency change should be accomplished in less than 80 bit times, or approximately 19 microseconds.

3.0 Data Separator circuit discussion (see figure 2)

3.1 Start Logic

The purpose of the start logic is to search for a possible address mark area. Each address mark is preceeded by a sync up field.

When the PLL switched to acquire lock to the read data, it should be done in an area of a stable data pattern. For this reason the snyc up fields contain a pattern of all zero data bits. In MFM encoding this results in a clock bit being written at the beginning of every bit cell. The fact that the clocks occur at regular intervals results in a stable pattern-minimum bit shift.

The task of the start logic then is to detect a string of clock bits before allowing the PLL to lock. Normally, 16 successive clock bits are detected before lock is allowed. Within 80 bit times, after being enabled the PLL should be locked to the clock pattern.

In MFM encoding an all 1's data pattern appears the same as the clock pattern. This means that sometimes the start logic will lock onto data bits instead of clock bits. However no address marks will be encountered following this condition.

The search for an address mark is a trial and error procedure.

3.2 Phase Detector, Filter, And Voltage Controlled Oscillator (VCO)

These components form the heart of the PLL. Generally speaking, the phase detector simply provides a pulse whose duty cycle is proportional to the phase difference between the incoming data and the output of the VCO. This pulse is then integrated by an active filter to provide an analog voltage feedback to the VCO which controls the VCO frequency.

The VCO output is divided by the ÷2 counter to be the same frequency as the input data.

The operating characteristics of the PLL depend largely on two factors; the loop gain, and the response of the filter. These are manipulated to yield the best trade off between acquistion time and immunity to disturbances. Fast acquisition results in low immunity to disturbances. Increased high frequency filtering can cause decreased phase margin which results in an underdamped system.

3.3 Data Separator and Address Mark Detector

The data separator essentially strips data bits and clock bits into two separate lines. These lines are fed into the address mark detector. As mentioned earlier, an address mark is made unique by the

fact that one clock bit is ommitted when the address mark was written. The address mark detector outputs an "Address Mark Found" signal when a clock bit, which according to MFM encode rules should have been there, is missing. This in conjunction with the "A1" data pattern constitutes an address mark.

4.0 Write Precompensation

Whenever two bits are written in close proximity to each other, a phenomenon called pulse superpositon occurs, which tends to cause the two bits to move away from each other. This is a large factor of bit shift.

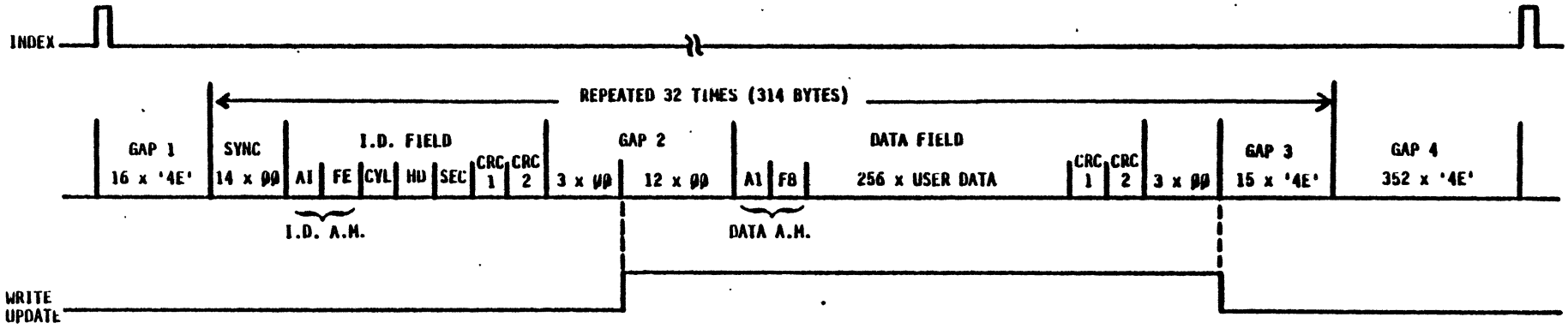
Other phenomenon such as random noise, speed variation, etc., will also cause bit shift, but to a lesser degree.

The effect of bit shift can be reduced by a technique called pre-compensation which, by detecting which bits will occur early and which bits will occur late, can be done by writing these bits in the oppositer direction of the expected shift.

Bit shift is more apparent on the innermost data tracks due to pulse crowding. There-fore pre-compensation should only be done at track number greater than 128.

The optimum amount of pre-compensation for the SA 1000 is 10 nanoseconds for both early and late written bits.

Figure 3 shows various bit patterns for pre-compensation.



NOTES:

1. NOMINAL TRACK CAPACITY - 10416 BYTES.
2. MINIMUM TRACK CAPACITY - (NOMINAL - 3% SPEED VARIANCE) 10102 Bytes.
3. WRITE TO READ RECOVERY TIME = 20 MICROSECONDS.
4. HEAD SWITCHING TIME = 20 MICROSECONDS.

FIGURE 1. SUGGESTED SA1000 TRACK FORMAT

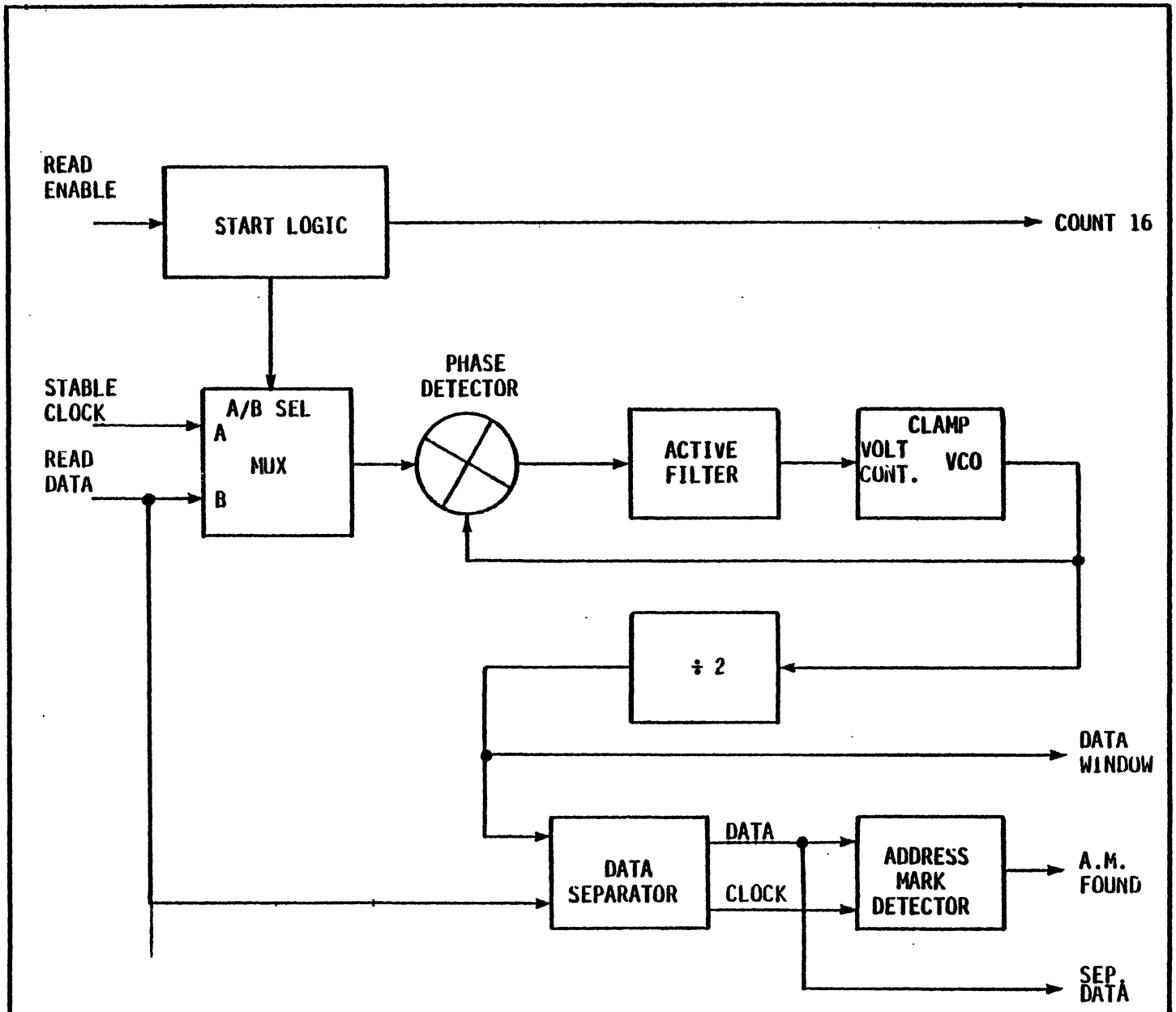
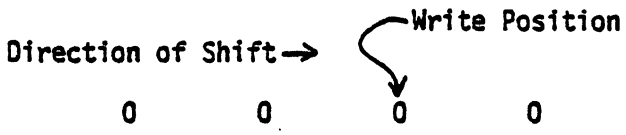


FIGURE 2 - BLOCK DIAGRAM OF PHASE LOCK LOOP DATA SEPARATOR.



0	0	0	0	= On Time Clock
0	0	0	1	= Late Clock
0	0	1	0	= On Time Data
0	0	1	1	= Early Data
0	1	0	0	-------
0	1	0	1	-------
0	1	1	0	= Late Data
0	1	1	1	= On Time Data
1	0	0	0	= Early Clock
1	0	0	1	= On Time Clock
1	0	1	0	= On Time Data
1	1	0	0	-------
1	1	0	1	-------
1	1	1	0	= Late Data
1	1	1	1	= On Time Data

FIGURE 3--Precompensation Pattern Detection bits are shifted through a 4 bit shift register. Bit is written out of the the third position.