SCD-DZ11

Asynchronous Multiplexor

Manual

Sigma Information Systems

SCD-DZ11

Asynchronous Multiplexor

Manual

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Section 1
General Information

1.1 INTRODUCTION

This manual provides the information needed to install and operate the SCD-DZ11 multiplexed asynchronous serial line interface manufactured by Sigma Information Systems, Anaheim, California. The SCD-DZ11 provides a buffered, program controlled interface between a PDP-11 and multiple local or remote asynchronous terminals.*

The material in this manual is arranged into the following sections.

Section 1 - GENERAL INFORMATION. This section contains a brief description of the SCD-DZ11, its configurations, and a list of specifications.

Section 2 - INSTALLATION. This section explains the requirements and procedures for equipment installation. Interface information and switch settings are provided. Diagnostic testing information is included.

Section 3 - PROGRAMMING. A description of the SCD-DZ11 control registers and programming features is presented to aid the user in programming the multiplexer.

*PDP-11, DEC, and Unibus are registered trademarks of Digital Equipment Corporation.

1.2 GENERAL DESCRIPTION

The SCD-DZ11 provides a buffered, program controlled interface between a PDP-11 and multiple local or remote asynchronous terminals. The compact multiplexer is available in EIA or 20mA versions, and an EIA/20mA combination. Typical applications include real-time/ transaction/communication processing and timesharing operations.

Local operation to terminals or computers is possible at speeds up to 9600 baud using EIA RS232C interfaces or 20mA current loop. Remote operation using public switched telephone lines is possible with EIA models. Data set control is provided to permit auto answer (dial-up) operation with modems capable of full-duplex oeration such as Bell Models 103 or 113. Remote operation over private lines for full duplex point-to-point, or full duplex multipoint (as a master control station), is also possible. The SCD-DZ11 does not support half-duplex operations with secondary transmit and receive. Half duplex modems, such as Bell 202, can be used on leased lines with these latter restrictions. Figure 1-1 illustrates possible applications of the SCD-DZ11.

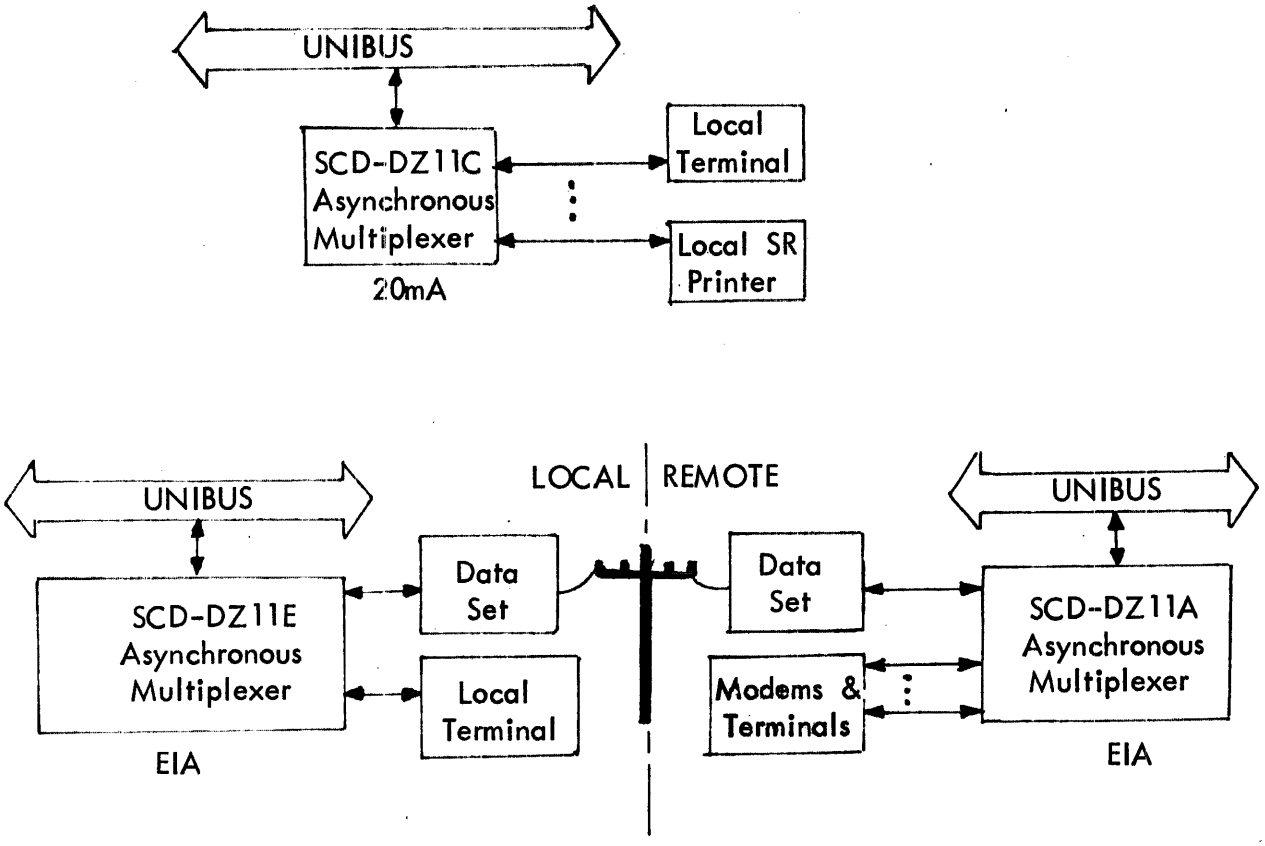


FIGURE 1-1: POSSIBLE APPLICATIONS FOR THE SCD-DZ11

1.3 FEATURES

- Software compatible with DEC's DZ11 and diagnostics and operating systems designed for the DZ11.
- Mixed line arrangement provides EIA and 20mA interfacing on a single multiplexer.
- Provides programmable speeds up to 9600 baud and formats on a per line basis.
- Data set control allows auto answer (dial-up) operation for full duplex modems with EIA versions.
- FIFO buffered input transfers reduce interrupt overhead and improve latency.
- Static filters on distribution panel eliminate extra panel and cable, and conserves cabinet space.
- 8-line configurations can be upgraded with the minimum number of components.

1.4 CONFIGURATIONS

The SCD-DZ11 is available in 8 or 16-line versions. An 8-line version consists of a single hexwide control board, cable assembly, and distribution panel with EIA or 20mA PCBA. It can be expanded to 16 lines by adding a second control board and cable assembly.

A 16-line configuration consists of two hexwide control boards and cable assemblies, and a distribution panel with 16 channel EIA or 20mA PCBAs, or 8 channels each EIA and 20mA PCBAs. Configurations are listed below:

SCD-DZ11A	8-line EIA
SCD-DZ11B	8-line EIA expansion
SCD-DZ11C	8-line 20mA
SCD-DZ11D	8-line 20mA expansion
SCD-DZ11E	16-line EIA
SCD-DZ11F	16-line 20mA
SCD-DZ11G	8-line EIA + 8-line 20mA

The maximum configuration allows for eight SCD-DZ11E/F/G modules per Unibus* for 128 lines of communication.

1.4.1 EIA Models

The SCD-DZ11A is an 8-line configuration with EIA RS232C interface. It consists of a control module, 8-line distribution panel, and interconnecting cable with an EIA communication module. The SCD-DZ11B consists of an additional control module and 50-conductor ribbon cable with an EIA communication module. The SCD-DZ11E is a 16-line configuration and is a combination of the SCD-DZ11A and SCD-DZ11B. Figure 1-2 illustrates the required hardware for the various EIA configurations.

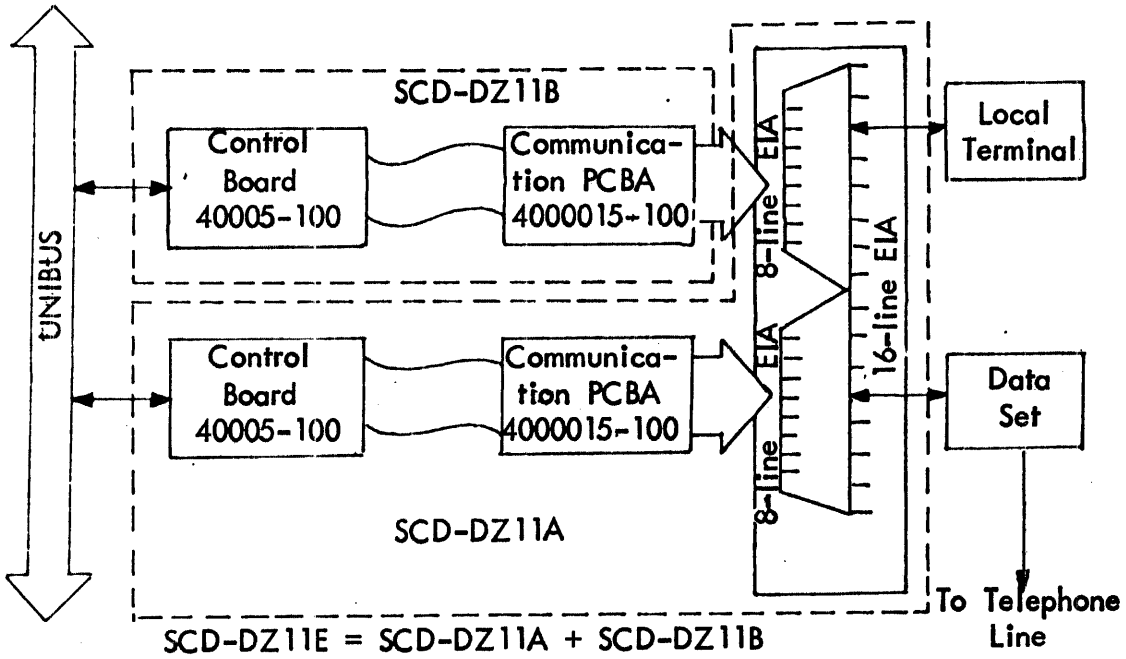


FIGURE 1-2: REQUIRED HARDWARE FOR EIA CONFIGURATIONS

1.4.2 20mA Current Loop Models

The SCD-DZ11C is an 8-line configuration with a 20mA current loop interface. It consists of a control module, distribution panel, and an interconnecting cable with a 20mA communications module. The SCD-DZ11D consists of an additional control module and 50-conductor cable with a 20mA communication module. The SCD-DZ11F is a 16-line configuration and is a combination of the SCD-DZ11C and SCD-DZ11D. Figure 1-3 illustrates the required hardware for the 20mA configurations.

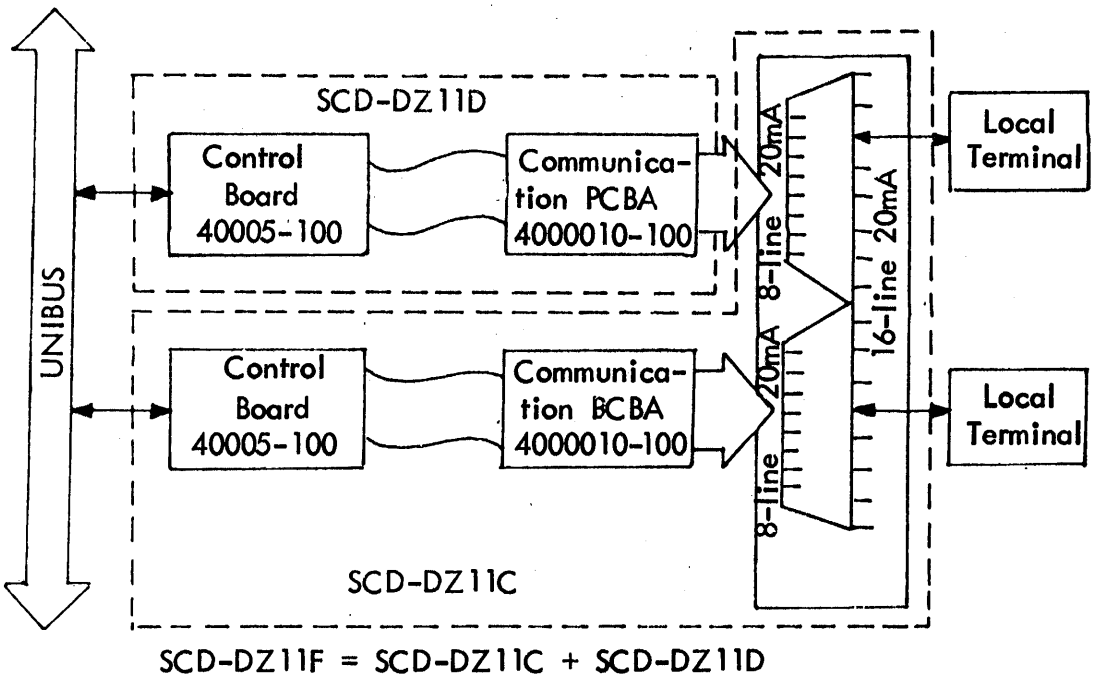


FIGURE 1-3: REQUIRED HARDWARE FOR EIA CONFIGURATIONS

1.4.3 EIA/20mA Combination Model

The SCD-DZ11G is a 16-line configuration with an 8-line EIA RS232C and an 8-line 20mA current loop interface. It consists of a control module, distribution panel, and two 50-conductor interconnecting ribbon cables with EIA and 20mA communication modules. Figure 1-4 illustrates the required hardware for the EIA and 20mA combination configurations.

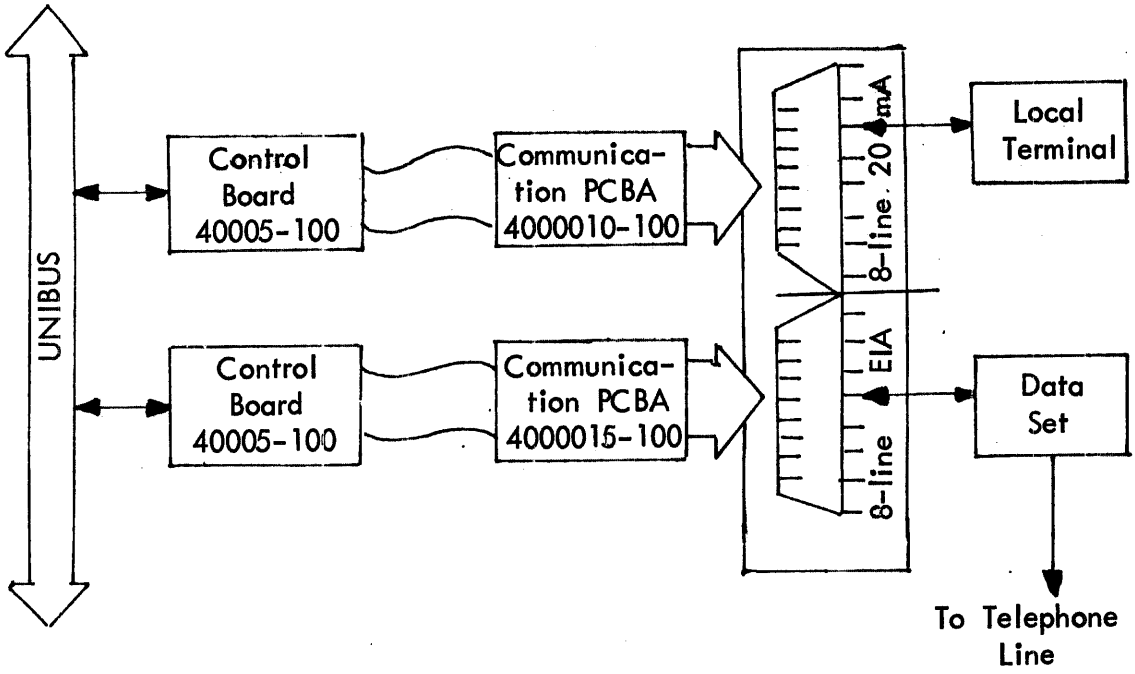


FIGURE 1-4: REQUIRED HARDWARE FOR EIA/20mA COMBINATION CONFIGURATION

1.5 PHYSICAL DESCRIPTION

The basic 8-line SCD-DZ11 consists of a single hex-wide control PCBA, a 5.25 inch distribution panel, and a 12-foot interconnecting cable with EIA or 20mA communication PCBA that mount on the distribution panel. A 16-line configuration uses two control PCBAs, a single distribution panel, and two ribbon cables with EIA or 20mA communication PCBAs. The EIA DZ11A and E versions include a loop back test adapter. All versions include a turn around test adapter. The basic SCD-DZ11 is illustrated in Figure 1-5.

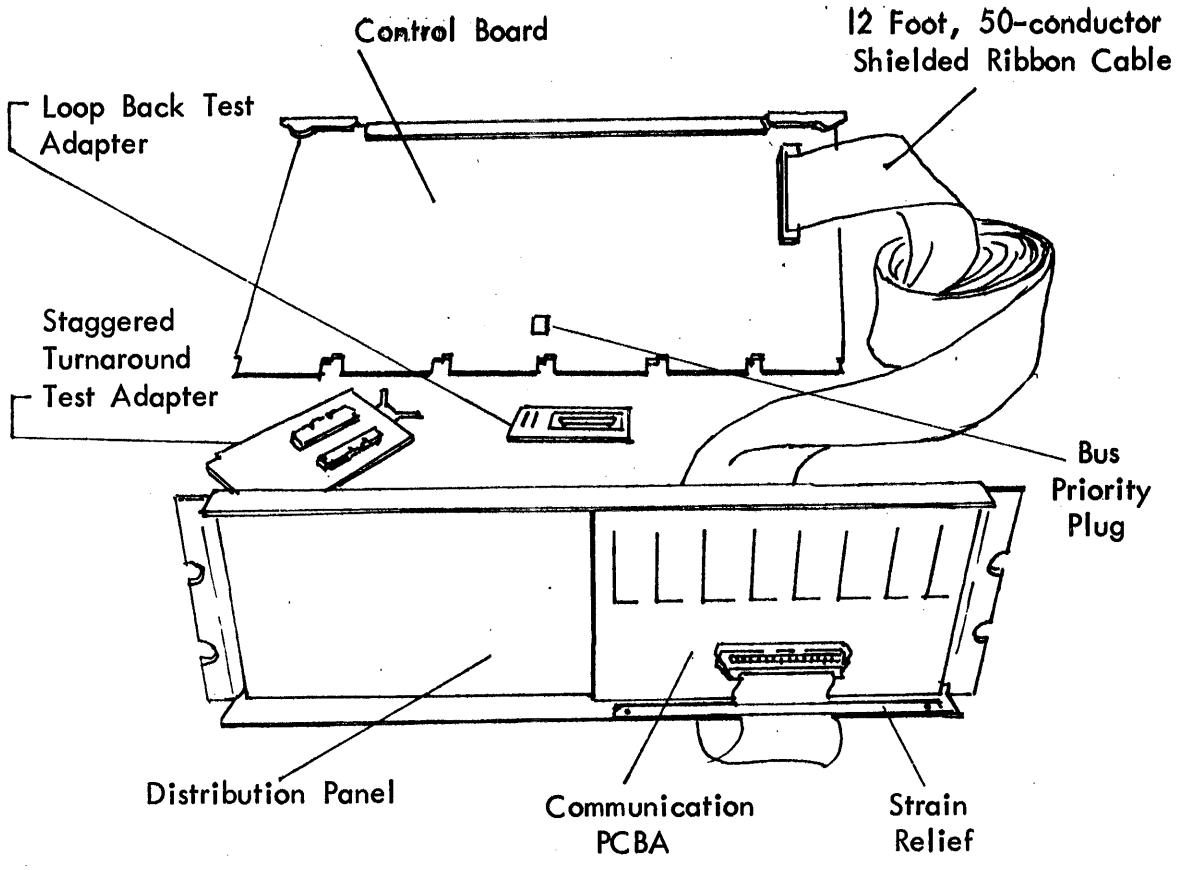


FIGURE 1-5: PHYSICAL DESCRIPTION OF BASIC SCD-DZ11

1.5.1 Hardware Descriptions

The distribution panel provides up to 16 communication lines with modules of 8 lines each. The EIA communication module is provided with a DB25P connector and is included with the SCD-DZ11A, B and E configurations. The SCD-DZ11 control module plugs into a CPU or expansion chassis hex SPC slot. The distribution panel can be mounted in a standard 19-inch wide RETMA rack. The communication module includes static filters to prevent problems caused by electrostatic discharge. A 50-conductor, flat, shielded cable connects the control module to the distribution panel. The cables to local devices are not provided with the SCD-DZ11 configurations.

1.5.2 Test Connectors

The loop back test adapter, provided with SCD-DZ11A/E/G, plugs into an EIA connector on the distribution panel or on the end of the modem cable to loop back data and modem signals on a single line. The loop back test adapter is illustrated in Figure 1-6.

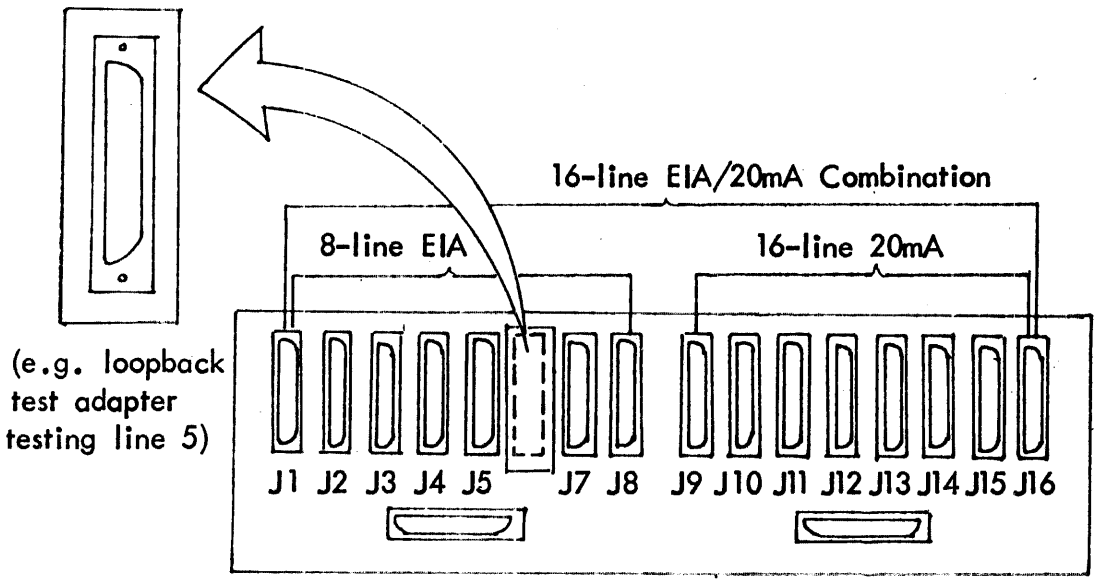
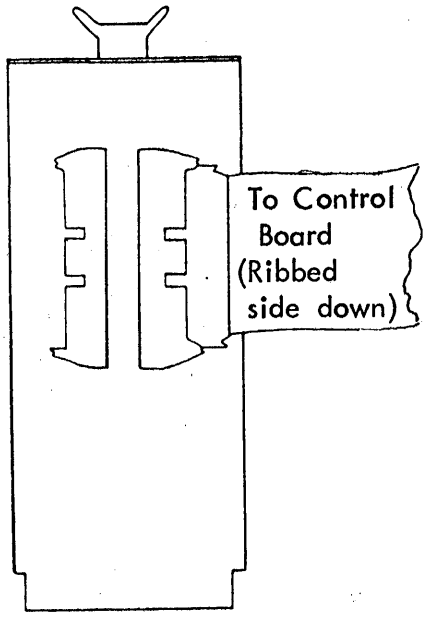
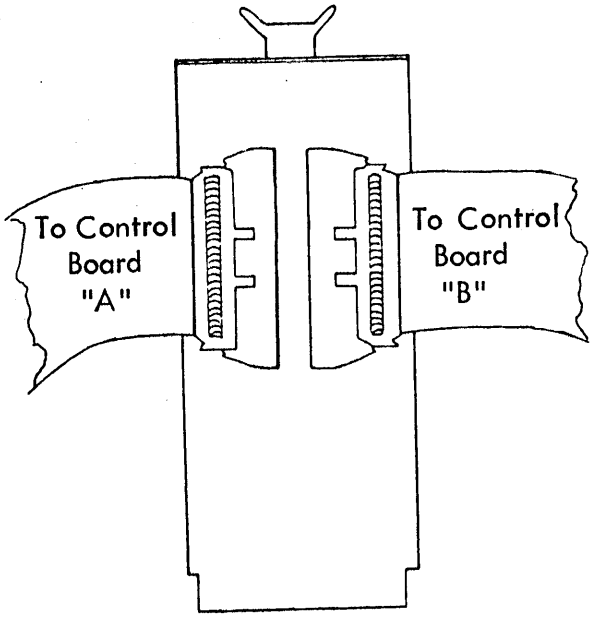


FIGURE 1-6: LOOP BACK TEST ADAPTER FOR EIA CONFIGURATIONS

The staggered turnaround test adapter, provided with all configurations, is shown in Figure 1-7. It connects to the 50-conductor shielded cable and staggers the data and modem lines as shown in Figure 1-8.

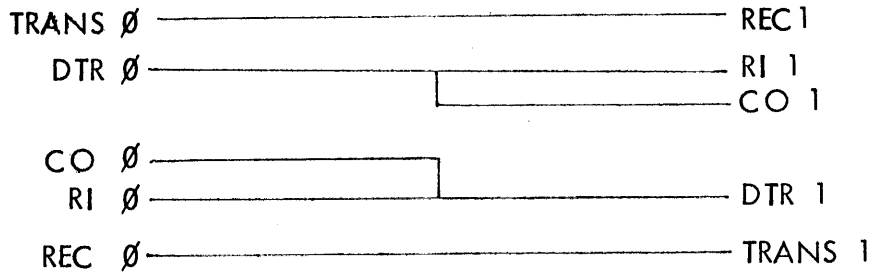


Staggered Turnaround
Test Adapter for SCD-
DZ11A/B/C/D/G.



Staggered Turnaround
Test Adapter for SCD-
DZ11E/F

FIGURE 1-7: STAGGERED TURNAROUND TEST ADAPTER



NOTE: Lines 2 and 3, 4 and 5, 6 and 7 are staggered the same way.

FIGURE 1-8: STAGGERED TURNAROUND DATA AND MODEM LINES

1.6 FUNCTIONAL DESCRIPTION

The SCD-DZ11 consists of three basic components: Unibus interface, control logic, and line interface, as defined in Figure 1-9.

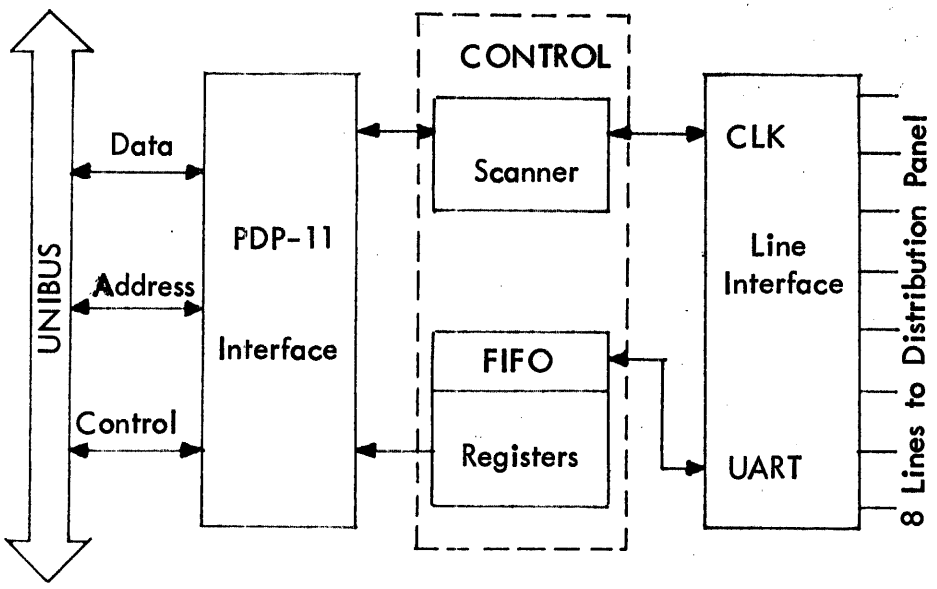


FIGURE 1-9: GENERAL FUNCTIONAL BLOCK DIAGRAM

1.6.1 Unibus Interface

All transactions between the Unibus and the SCD-DZ11 control logic are dependent on the PDP-11 Unibus interface which performs data handling, address recognition, and interrupt control.

DATA HANDLING. The Unibus sends data to/from registers via the control logic and provides the voltage signals which determine transmission/reception of data to/from the Unibus.

ADDRESS RECOGNITION. Preselected Unibus address recognition activates the proper load (Write and Read signals) which is used to route the I/O data to the desired locations.

INTERRUPT CONTROL. This function initiates and controls interrupt processing between the SCD-DZ11 and the central processor.

1.6.2 Control Logic

The control logic, which consists of the scanner and registers, generates receiver/transmitter timing and control signals. The scanner, which produces data flow to/from the appropriate line, continuously analyzes information from the line interface and registers. The scanner consists of generating logic including a clock and a four-phase clocking network.

Four device registers are utilized to provide six 16-bit accessible registers. The registers store I/O data, monitor control signal conditions, and determine operating status. The registers are accessible in bytes and/or words and, depending on the operation, can be read or written.

1.6.3 Line Interface

The SCD-DZ11 is located between the Unibus parallel data path and serial data paths (terminals or telephone lines). The line interface provides serial-to-parallel and parallel-to-serial data format conversion. Each line is converted by independent universal asynchronous receiver/transmitter integrated circuits (UARTs). The line interface also allows the line receiver or driver to convert TTL voltage levels in the SCD-DZ11 to correspond to external device input lines.

1.7 SPECIFICATIONS

PERFORMANCE

Operating Mode:	Full-duplex
Data Format:	Asynchronous, serial by bit, 1 start and 1, 1 1/2 (5-level codes only) or 2 stop bits by hardware under program control.
Character Size:	5, 6, 7 or 8 bits. Program selectable. No parity bit.
Parity	Even, odd or none. Program selectable.

Bit Polarities:	UNIBUS	INTERFACE	EIA OUT
Data Signal:	Low = 1	High = 1	Low = 1 = Mark
	High = Ø	Low = Ø	High = Ø = Space
Control Signal:	Low = 1	High = 1	Low = OFF
	High = Ø	Low = Ø	High = ON

Order of Bit:	Transmission/reception low-order bit first.
Break:	Can be generated and detected on each line.
Baud Rates:	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 4800, 7200, and 9600.

Throughput:	21,940 characters/second = (bits/second x number of lines x direction)/(bits/character).
Example:	(9600 x 8 x 2)/7 = 21,940 characters/second.
NOTE:	The theoretical maximum is 21,940. Actual throughput depends on other factors, such as type of CPU, system software, etc.

OUTPUTS

EIA — Each line provides voltage levels and connector pins that conform to Electronic Industries Association (EIA) standard RS232C and CCITT recommendation V.24. The leads supported by this option are:

Circuit AA (CCITT 101)	Pin 1	*Protective Ground
Circuit AB (CCITT 102)	Pin 7	*Signal Ground
Circuit BA (CCITT 103)	Pin 2	Transmitted Data
**Circuit CD (CCITT 108.2)	Pin 20	Data Terminal Ready
Circuit CF (CCITT 109)	Pin 8	Carrier

*NOTE: Signal ground and protective ground are connected.

**NOTE: Circuit CA (CCITT 105 - Request to Send) is connected to circuit CD (DTR) through a jumper on the distribution panel. This allows control of the Request to Send line for full-duplex modem applications that use the RTS circuit.

20mA — Each 20mA channel provides the current for the two pairs of signal lines (transmit and receive). The signals and associated pins are:

Receive +	Pin 1
Receive -	Pin 2
Transmit +	Pin 3
Transmit -	Pin 4

The 20mA line is connected to local terminals (no data set control). The line is active and drives only passive devices.

POWER REQUIREMENTS (MAXIMUM)

	+5VDC	-15VDC	+15VDC
SCD-DZ11A,B	2.5A	0.15A	0.13A
SCD-DZ11C,D	3.0A	0.30A	0.13A
SCD-DZ11E	5.0A	0.30A	0.26A
SCD-DZ11F	6.0A	0.60A	0.26A
SCD-DZ11G	5.5A	0.60A	0.26A

DISTORTION	MAX
"Space to Mark" and "Mark to Space" in a received character	40%
Speed distortion in a received character for 2000 baud	3.8%
All other baud rates	4%
Speed distortion from transmitter for 2000 baud	2.2%
All other baud rates	(Less than 2%)

INTERRUPTS

RDONE Occurs each time a character appears at the FIFO output.

SA FIFO alarm. Occurs after 16 characters enter the FIFO. Rearmed by reading the FIFO. This interrupt disables the RDONE interrupt.

TRDY Occurs when the scanner finds a line ready to transmit on.

There are no modem interrupts. Normally, a level 5 priority plug is supplied. The interface level can be modified to level 4, 6, or 7 by using the proper priority plug.

LINE SPEED

The baud rate for a line (transmitter/receiver) is program selectable. Also, the receiver for each line can be individually turned on or off under program control.

ENVIRONMENTAL REQUIREMENTS

Operating Temperature:	5°C to 50°C (41°F to 122°F). Reduce 1.8°C/1000 meters (1.0°F/1000 feet) for operation at altitudes above sea level.
Relative Humidity:	10% to 95% with maximum wet bult of 32°C (90°F) and a minimum dewpoint of 2°C (36°F).

Section 2
Installation and Operation

2.1 GENERAL INFORMATION

This section provides information for the installation and operation of the SCD-DZ11 multiplexed asynchronous serial line interface.

2.2 UNPACKING AND INSPECTION

The SCD-DZ11 is shipped in a special packing carton designed to keep the equipment from vibrating and to give it maximum protection during shipment. The packing carton should be retained in the event the product requires reshipment.

To unpack the SCD-DZ11, remove any packing material and visually inspect for damage. Inventory of items that are supplied for EIA versions is listed in Table 2-1; for 20mA versions in Table 2-2; and for the EIA/20mA combination version in Table 2-3. Verify that all items have been received.

PART NUMBER	DESCRIPTION	QUANTITY SCD-DZ11		
		A	B	E
400005-100	Control Board Assembly	1	1	2
500001-100	Distribution Panel Assembly	1		1
400015-100	EIA Communication Module	1	1	2
500002-100	Cable Assembly, 12'	1	1	2
400025-100	Loop Back Test Adapter	1		1
400020-100	Turnaround Test Adapter	1	1	1
500008-100	Strain Relief Bar	1	1	2
500027	Hardware Mounting Kit	1		1
500028	Bus Priority Plug	1	1	2
MA400005	SCD-DZ11 Manual	1		1

TABLE 2-1: ITEMS SUPPLIED FOR EIA CONFIGURATIONS

PART NUMBER	DESCRIPTION	QUANTITY SCD-DZ11 C	D	F
400005-100	Control Board Assembly	1	1	2
500001-100	Distribution Panel Assembly	1		1
400010-100	20mA Communication Module	1	1	2
500002-100	Cable Assembly, 12'	1	1	2
400020-100	Turnaround Test Adapter	1	1	1
500008-100	Strain Relief Bar	1	1	2
500027	Hardware Mounting Kit	1		1
500028	Bus Priority Plug	1	1	2
MA40005	SCD-DZ11 Manual	1		1

TABLE 2-2: ITEMS SUPPLIED FOR 20mA CONFIGURATIONS

PART NUMBER	DESCRIPTION	QUANTITY SCD-DZ11G
400005-100	Control Board Assembly	2
500001-100	Distribution Panel Assembly	1
400015-100	EIA Communications Module	1
400010-100	20mA Communication Module	1
500002-100	Cable Assembly, 12'	2
400025-100	Loop Back Test Adapter	1
400020-100	Turnaround Test Adapter	1
500027	Hardware Mounting Kit	1
500028	Bus Priority Plug	2
50008-100	Strain Relief Bar	2
MA40005	SCD-DZ11 Manual	1

TABLE 2-3: ITEMS SUPPLIED FOR EIA/20mA CONFIGURATION

2.3 INSTALLATION

The procedures described below should be followed for equipment installation. Refer to Figure 2-1 for component locations.

Note that, on the EIA communication module, W1 and W2 for each line are soldered in place. W1 connects DTR to pin 4 (Request to Send). This allows the SCD-DZ11 to assert both DTR and RTS when using a modem which requires control of RTS. Pin K, W2 jumper, is also connected to the DTR lead for use in modems that implement the Force Busy function. Both jumpers should be in for diagnostic purposes. Remove if there is interference with modem operation.

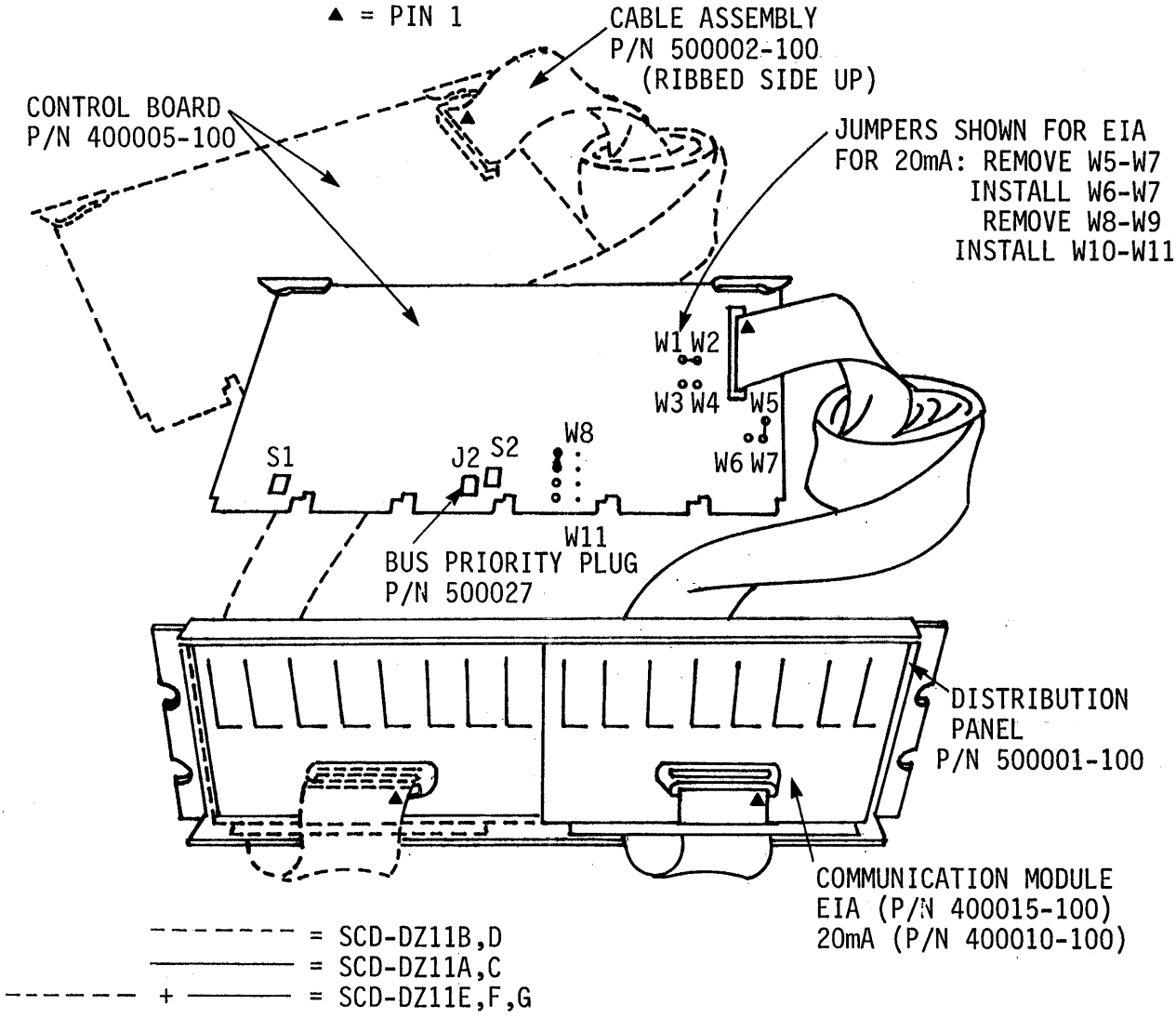


FIGURE 2-1: SCD-DZ11 COMPONENTS

2.3.1 Distribution Panel Installation

A distribution panel is supplied with all configurations except SCD-DZ11B and SCD-DZ11D. The distribution panel normally mounts on the back rails of a standard 19 inch wide RETMA rack. Using the supplied hardware, mount the panel so that the cable connectors face outwards toward the back of the cabinet.

The distribution panel should be mounted to provide convenient access for terminal cable installation. Allow access with service loop for the 12 foot 50-conductor ribbon cable connecting to the control PCBA.

2.3.2 Communication Module Installation

SCD-DZ11 versions are shipped with the communication module installed with the exception of the SCD-DZ11B and SCD-DZ11D. These expansion units consist of an additional control board, cable assembly, and communication module. Mount the communication module onto the distribution panel using the nine #6-32 1/2 inch screws supplied with the unit. Refer to the following sections for control board and cable installation.

2.3.3 Device and Vector Addressing

The SCD-DZ11 device and vector addresses are selected from floating device and vector address spaces that allow the multiplexer to be assigned the lowest space in a defined sequence of addressable options. The device floating address space is 160010_8 to 163776_8, and the vector space is 300_8 to 776_8. The sequence for the floating spaces are defined in Table 2-4. Examples illustrating the vector/device address assignments are included.

EXAMPLE 1: The simples case where there is one SCD-DZ11 and no options.

OPTION	DEVICE ADDRESS	VECTOR ADDRESS	NUMBER OF DEVICES	COMMENTS
DJ11	160010	N/A	None	
DH11	160020	N/A	None	
DQ11	160030	N/A	None	
DU11	160040	N/A	None	
DUP11	160050	N/A	None	
LK11	160060	N/A	None	
DMC11	160070	N/A	None	
SCD-DZ11	160111	300	One	
SCD-DZ11	160110		None	No more SCD-DZ11s

Therefore, device address is assigned 160111 and vector address is assigned 300.

DEVICE/VECTOR STATUS	FLOATING SPACE SEQUENCE ADDRESS	VECTOR
Highest		DC11
		KL11/DL11A,B
		DP11
		DM11A
		DN11
		DM11BB
		DR11A,C
		PA611
		DT11
		DX11
		DL11C,D,E
	DJ11	DJ11
	DH11	DH11
		GT40
		LPS11
	DQ11	DQ11
		KW11W
	DU11	DU11
	DUP11	DUP11
		DV11
	LK11	LK11A
		DWUn
	DMC11	DMC11
Lowest	SCD-DZ11	SCD-DZ11

TABLE 2-4: DEVICE/VECTOR ADDRESS SPACE SEQUENCE

EXAMPLE 2: One DJ11, one LPS11, one KW11-W, and one SCD-DZ11.

OPTION	DEVICE ADDRESS	VECTOR ADDRESS	NUMBER OF DEVICES	COMMENTS
DJ11	160010	300	One	
DJ11	160020	N/A	None	No more DJ11s
DH11	160030	N/A	None	
LPS11		310	One	*
KW11-W		320	One	*
DQ11	160040	N/A	None	
DU11	160050	N/A	None	
DUP11	160060	N/A	None	
LK11	160070	N/A	None	
DMC11	160100	N/A	None	
SCD-DZ11	160110	330	One	
SCD-DZ11	160120	N/A	None	No more SCD-DZ11s

*Device address not assigned since device is not in floating device address space.

Therefore, device address is 160110 and vector address is 330.

EXAMPLE 3: One DJ11, one DH11, one KW11-W, one DV11, one DMC11, and two SCD-DZ11s.

OPTION	DEVICE ADDRESS	VECTOR ADDRESS	NUMBER OF DEVICES	COMMENTS
DJ11	160010	300	One	
DJ11	160020	N/A	None	No more DJ11s
DH11	160040	310	One	*
DH11	160050	N/A	None	No more DH11s
DQ11	160060	N/A	None	
KW11-W		320	One	**
DU11	160070	N/A	None	
DUP11	160100	N/A	None	
DV11	160110	330	One	
DV11	160120	N/A	None	No more DV11s
DMC11	160130	340	One	
DMC11	160140	N/A	None	No more DMC11s
SCD-DZ11	160150	350	One	
SCD-DZ11	160160	360	One	
SCD-DZ11	160170	N/A	None	No more SCD-DZ11s

*DH11 must start on address space that is a multiple of 20.
**Device address not assigned since device is not in floating device address space.

Therefore, device addresses are 160150 and 160160 and vector address is 350 and 360.

ONCE DEVICE AND VECTOR ADDRESSES ARE DETERMINED, SET SWITCHES S1 AND S2 ACCORDING TO TABLE 2-5 AND 2-6.

2.3.4 Control Board and Cable Installation

Ensure that the priority plug is properly seated in socket J2 on the control board. Refer to Figure 2-1 for location.

Insert the control module(s) into an SPC slot. Connect the flat shielded cable RIBBED SIDE UP to J1 on the module. Ensure that pin 1 indicators are lined up on J1 and the cable. Connect the other end of the cable to the communication module as shown in Figure 2-1.

CAUTION

Install and remove modules carefully to avoid snagging components on the card guides and accidentally changing switch settings.

ADDRESS	SWITCH S1 POSITIONS									
	10	9	8	7	6	5	4	3	2	1
160000										
160010										X
160020									X	
160030									X	X
160040								X		
160050								X		X
160060								X	X	
160070								X	X	X
160100							X			
160110							X			X
⋮ 16020						X				
⋮ 160300						X	X			
⋮ 160400					X					
⋮ 160500					X		X			
⋮ 160600					X	X				
⋮ 160700					X	X	X			
⋮ 161000				X						
⋮ 162000			X							
⋮ 163000			X	X						
⋮ 164000		X								
⋮ 165000		X		X						
⋮ 166000		X	X							

X = ON
BLANK = OFF

TABLE 2-5: SWITCH S1 ADDRESS SELECTION

VECTOR	SWITCH S2 POSITIONS					
	8	7	6	5	4	3
300	X			X	X	X
310	X			X	X	
320	X			X		X
330	X			X		
340	X				X	X
350	X				X	
360	X					X
370	X					
400		X	X	X	X	X
⋮						
500		X		X	X	X
⋮						
600			X	X	X	X
⋮						
700				X	X	X
710				X	X	
720				X		X
730				X		
740					X	X
750					X	
760						X
770						

X = ON
BLANK = OFF

TABLE 2-6: SWITCH S2 VECTOR SELECTION

2.3.5 NPR Enhancement

The SCD-DZ11 has special logic which monitors the Bus NPR line. If a bus grant line is asserted while bus NPR is asserted, this circuitry will block the grant and return SACK. When BBSY becomes unasserted from the last Bus Master, the device will clear SACK off the bus. The processor will then be able to service the NPR, improving latency time for NPR devices. Since only some PDP-11 processors will work with this special circuitry, a switch (S2) is provided to enable or disable it. If S2, position 2 is ON, NPR enhancement is disabled. If S2-2 is OFF, NPR enhancement is enabled.

NOTE

Switch S2, position 1 is not used.

2.4 DIAGNOSTIC TESTING

Plug the staggered turnaround test adapter (P/N 400020-100) into the control board via the 50-conductor cable. Run the SCD-DZ11 in staggered mode to verify module operation. Refer to MAINDEC-11 DZDZA. Run at least two passes without error.

The loop back test adapter (P/N 400025-100) is used for EIA testing only. Omit this step for 20mA models. Connect the test adapter on the first line (J1) and run the cable test diagnostics. Repeat this step for each line.

NOTE

Ensure that no devices are connected to any of the remaining lines. Remove the loop back test adapter when cable testing is completed.

Run the DEC/X11 system exerciser to verify the absence of Unibus interference with other system devices.

When possible, run the echo test diagnostic to verify the cable connections to terminal equipment.

Section 3
Programming

3.1 INTRODUCTION

This section provides programming information for the SCD-DZ11. A description of each register, including bit assignments and program limits, is provided for programming and maintenance.

3.2 REGISTER BIT ASSIGNMENTS

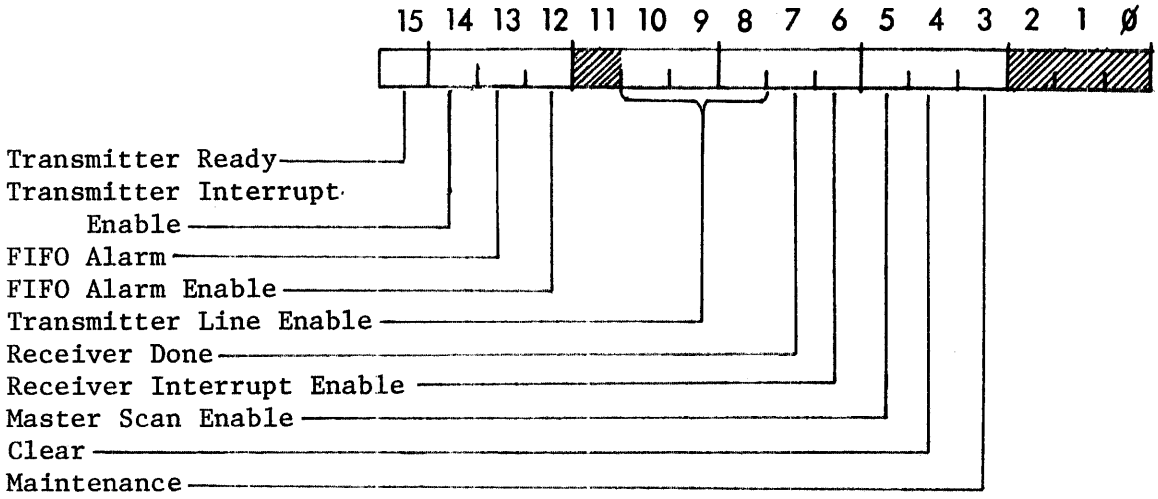
The SCD-DZ11 consists of four discrete device registers:

RØ	Control Status	CSR	Read/Write
R2	Receiver Buffer	RBUF	Read Only
	Line Parameter	LPR	Write Only
R4	Transmit Control	TCR	Read/Write
R6	Transmit Data	TDR	Write Only
	Modem Status	MSR	Read Only

The four registers are expanded to six registers by assigning a Read Only or Write Only status to R2 and R6. The PDP-11 processor instructions that perform a Read-Modify-Write (DATIP) bus cycle cannot be utilized with R2 and R6. R2 permits only word instructions but byte or word instructions may be used with R6. RØ and R4 have no programming restraints. For all registers, Read Only bits are not affected by a Write operation, and a Read operation results in binary Ø for Write Only or Not Used bits.

3.2.1 Control and Status Register (CSR) 16XXX0

The Control and Status register has no programming restraints. Write Only and Not Used bits are read as zero. Read Only bits are not affected by Write attempts.



15 TRANSMITTER READY. This bit is set when a line with the LINE ENB bit set also has an empty transmit buffer. Cleared by CLR, BUS INIT, or by loading the transmit buffer. Read Only.

14 TRANSMIT INTERRUPT ENABLE. When set, this bit permits an interrupt if Transmitter Ready is set. Read/Write.

13 FIFO ALARM. This bit is set after 16 characters enter FIFO. An interrupt is generated if bit 6 is set. FIFO must be emptied when FIFO flag occurs since the flag will not set again until another 16 characters enter FIFO. Cleared by CLR, BUS INIT, and reading RBUF. Read Only.

12 FIFO ALARM ENABLE. This bit allows bit 13 to cause an interrupt after 16 characters enter the FIFO, providing bit 6 is set. If bit 6 is not set, FIFO Alarm can be used as a flag. This bit can prevent Receiver Done from causing interrupts. Cleared by CLR and BUS INIT.

11 Not Used

10-8 TRANSMIT LINE ENABLE. When bit 15 is set, these bits indicate which line is ready to transmit a character. When the character is loaded into the transmit buffer, bit 15 clears. If a second line is ready, bit 15 sets again. After a CLR or

or BUS INIT, these bits return to line Ø. These bits are relavent only if bit 15 is true. Read Only.

7 RECEIVER DONE. If bit 6 is set and bit 12 is clear, this bit generates RCV INT, and clears when the receive buffer is read. Resets when another word reaches the FIFO output. This bit can be used as a flag to indicate the FIFO contains a character if bit 6 is clear.

6 RECEIVER INTERRUPT ENABLE. This bit enables receiver interrupts. Cleared by CLR and BUS INIT. Read/Write.

5 MASTER SCAN ENABLE. This bit activates the scanner to enable the receiver transmitter and FIFO. Cleared by CLR and BUS INIT. Read/Write.

4 CLEAR. This bit generates a reset which clears the receiver FIFO, all UARTs, and the CSR. The CSR and line parameters must be reset after CLR is issued. Bits Ø through 14 of RBUF and modem control registers are not affected. CLR = 1 indicates a Clear operation is in progress. Read/Write.

3 MAINTENANCE. When this bit is set, serial output data from the transmitter is looped back as input data to the receiver, which permits running diagnostics without disturbing any connectors. Cleared by BUS INIT and CLR. Read/Write.

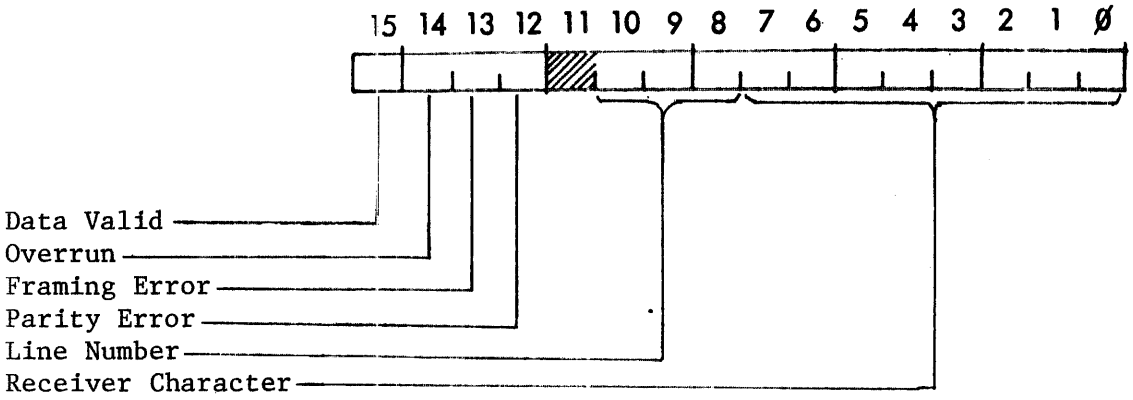
2-Ø Not Used.

3.2.2 Receive Buffer Register (RBUF) 16XXX2

The Receive Buffer register is the Read Only portion of register R2. Programming restraints are:

Byte, TST, or BIT instructions cannot be used.

CSR bit 5 (Master Scan Enable) must be set or else bit 14-Ø of RBUF are invalid regardless of the status of Data Valid (bit 15) and the FIFO held empty. Each reading advances the FIFO and presents the next character to the program. Although bits14-Ø do not go to zero, they become invalid and the FIFO is emptied after a CLR or BUS INIT. Data Valid (bit 15) goes to zero.



15 DATA VALID. This bit indicates that the character read from FIFO (RBUF) is valid. The RBUF is read until the Data Valid = Ø, indicating an invalid character and an empty FIFO. Cleared by CLR and BUS INIT.

14 OVERRUN. This bit indicates a Receiver Buffer overflow. When overflow occurs a received character is replaced by another received character before storage in the FIFO. One character is lost and the received character, put in the FIFO, is valid.

13 FRAMING ERROR. This bit indicates improper framing (Stop bit is not a Mark) of received character. It is also used for break detection.

12 PARITY ERROR. This bit does not appear in the RBUF and is generated by the SCD-DZ11. It indicates that the received bit had a parity error when set.

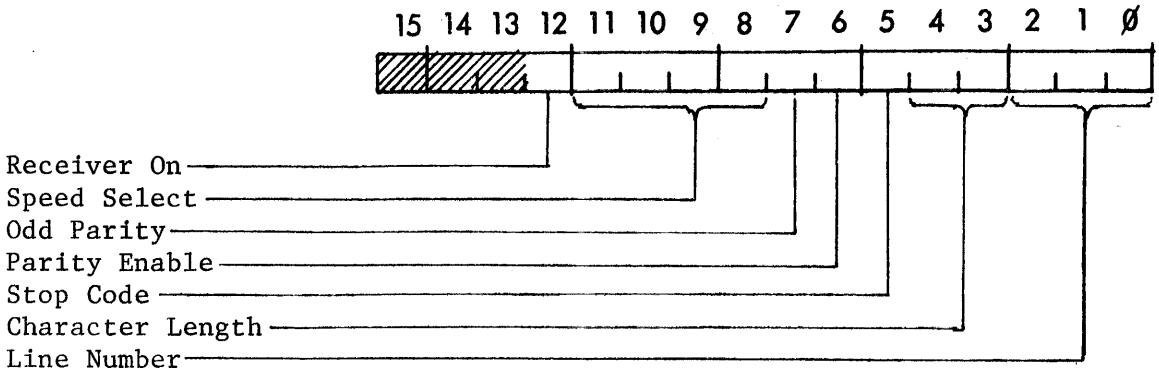
11 Not Used.

1Ø-8 LINE NUMBER. This bit indicates the line number on which the character is received.

7-Ø RECEIVED CHARACTER. These bits contain the received character. High-order bits are forced to zero when the selected code level is less than 8 bits wide.

3.2.3 Line Parameter Register (LPR) 16XXX2

The line parameter register is the Write Only part of register R2. After a CLR (bit 4 of CSR) or BUS INIT operation, line parameters for each line must be reloaded. Programming restraints do not allow byte operations, BIS or BIC instructions and the Read Only status of the line parameter register.



15-13 Not Used.

12 RECEIVER ON. This bit activates the receiver clock. It must be set when loading parameters. CLR or BUS INIT burns the receiver clock off.

11-8 SPEED SELECT. These bits select the baud rates as defined by the TRAN and RCV speed for the line determined by bits ØØ-Ø2. See Table 3-1 for applicable baud rates.

BITS				BAUD RATE
11	10	Ø9	Ø8	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Not Used

NOTE

Transmit and Receive speeds must be the same.

TABLE 3-1: BAUD RATE SELECTION CHART

7 PARITY. This bit determines even or odd parity (Ø = even, 1 = odd). Bit 6 must be set for this bit to be effective.

6 PARITY ENABLE. This bit enables the parity option. If no parity is desired, this bit should not be set.

5 STOP CODE. This bit sets the Stop Code length (Ø = 1 unit stop, 1 = 2 unit stop or 1.5 unit stop if a 5-level code is used).

4-3 CHARACTER LENGTH. These bits define the character length for the selected line as shown in Table 3-2.

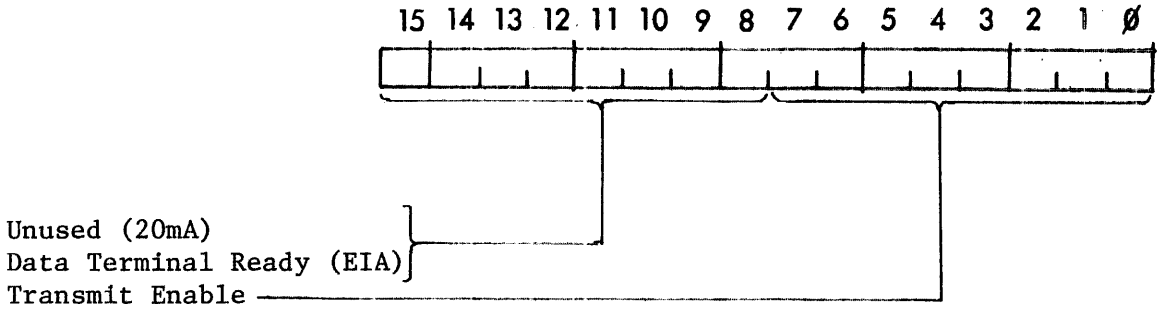
BIT 3	BIT 4	CHARACTER LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

TABLE 3-2: CHARACTER LENGTH SELECT

2-0 LINE NUMBER. These bits determine the line for parameter loading.

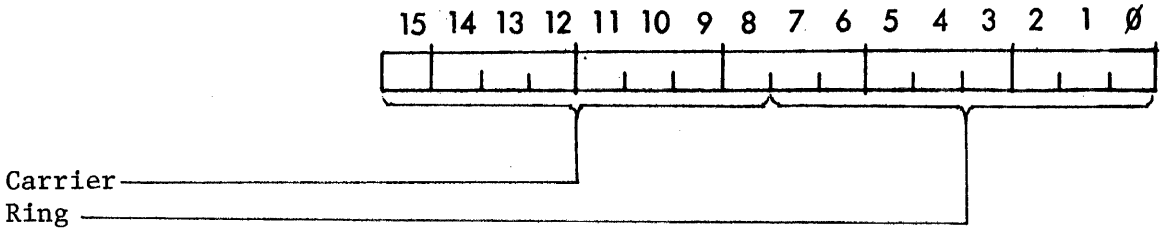
3.2.4 Transmit Control Register (TCR) 16XXX4

This Transmit Control register is a Read/Write register. For EIA operation, the high byte contains DTR for each line and is cleared by BUS INIT only, not CLR. For 20mA current loop operation, the high byte is unused and read as zero. The low byte has a line enable bit for each line. Transmission on the corresponding line is accomplished with a set bit. The low byte is cleared by CLR and BUS INIT.



3.2.5 Modem Status Register (MSR) 16XXX6

The Modem Status register is the Read Only part of register R6. It is used for EIA operation only. The low byte of the register monitors the state of each line's ring indicator lead (R1). The high byte monitors the state of each line's carrier lead (CO). Programming considerations should include the register format below, the Read Only status of the register, and the fact that CLR and BUS INIT have no effect on the register.



3.2.6 Transmit Data Register (TDR) 16XXX6

The Transmit Data register is the Write Only part of register R6. The low byte is the Transmit Buffer (TBUF) that stores the character that is to be transmitted. The high byte is the Break register with each line controlled by an individual bit (7-Ø). When a break is set, the associated line transmits zeros immediately and continuously. Programming considerations should include the Write Only status of the register, the fact that BIS and BIC instructions cannot be used, and the realization that this register is cleared by CLR and BUS INIT. The character loaded into the TBUF must be right justified for character lengths less than 8 bits since the hardware induces the most significant bits to zero.