SIGNETICS DIGITAL

DESIGNER'S CHOICE LOGIC SSI 8400/8800 TTL/DTL DATA BOOK

DCL®

DESIGNER'S CHOICE LOGIC SPECIFICATIONS HANDBOOK

VOL.I LOGIC ELEMENTS

DCL SERIES

DCL SPECIFICATIONS HANDBOOK, Vol. I

Multivibrator, Low Power Elements, High Speed Elements,
Ultra High Speed Elements, Interface Elements

DCL SPECIFICATIONS HANDBOOK, Vol. II

MSI Arrays

25% to 50% recycled paper

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*Systematic Uniformity and Reliability Evaluation

INTRODUCTION

The Designers Choice Logic (DCL) handbooks provide the the reader with a software package that clearly explains the performance and use of the DCL Series 8000 family. Volume I covers basic logic elements including multivibrators, low power elements, standard elements, high speed elements and interface elements. Volume II covers MSI arrays including shift and buffer registers, synchronous and asynchronous counters, adders and arithmetic elements, multiplexers and conditional complementors, gating steering and decoding arrays, and decoders/display drivers.

This handbook is divided into five sections for easy reference:

Section 1 -- "Design Considerations" provides all the information necessary to design a reliable, working system.

Section 2 -- "Electrical Characteristics" contains detailed test limit and test condition information for simplified device evaluation and incoming inspection. Compatibility between the various product types is guaranteed by these tests. The material is organized in a format which lends itself to generation of device specifications with a minimum of cost and time.

Section 3 -- "AC Testing" and Section 2 provide complete AC test methods and procedures to ensure accurate specification guarantees.

Section 4 -- "Applications" contains straightforward information on the use and operation of DCL devices. In addition, several time-saving device applications are provided to help speed system design and minimize costs.

Section 5 -- "SURE Program" consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability in Signetics products. This program, along with the individual device data sheets, provides a complete procurement specification, thus saving procurement cycle time and cost.

If the reader desires more information, he should contact the Signetics representative in his area.

SECTION 1
DESIGN CONSIDERATIONS

ABOUT THIS SECTION

This section is intended to provide all of the required information necessary to allow reliable System Design. The tables and charts presented here are derived from the test guarantees in the circuit characteristics section. The information covered is as follows:

Table 1-1 — Temperature Range and Package Type
Table 1-2 — Absolute Maximum Ratings
Table 1-3 — Guaranteed Worst Case DC Noise Margins
Table 1-4 — Guaranteed Worst Case DC Loading
Table 1-5 — Guaranteed Worst Case AC Loading
Table 1-6 — Guaranteed Propagation Delay Limits
Table 1-7 — Guaranteed Power Consumption Limits Per Gate

TEMPERATURE RANGES AND PACKAGE TYPES

DCL elements are available in two temperature ranges and several packages. Temperature ranges and package types are specified as shown in Table 1-1.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit currents and voltages in accordance with Table 1-2.

NOISE IMMUNITY

The two most significant types of noise commonly encountered in digital systems can be characterized as being of the slow drift type or of the fast narrow pulse type. Slow drift noise is generally traceable to changes in power supply and ground levels produced by variations in load and temperature demands on the power supply. This is usually designated as DC noise. The ability of a circuit to maintain a prescribed logic state in the presence of DC noise is measured in terms of DC noise margin. DC noise margin is defined as the difference between the output voltage level of a driving gate and the input threshold voltage of a driven gate for both the "1" and the "0" states. The input threshold voltage is specified as a test condition in guaranteeing "1" and "0" output voltages in the data tables in Section 2. The margins tabulated in Table 1-3 are calculated from those data tables and constitute guaranteed worst case DC noise margins for all combinations of driving and driven elements over the full temperature range and the power supply range of 4.75V to 5.25V with full temperature differential and power supply differential of 0.5V between driving and driven elements.

Noise which displays a rate of change which is fast relative to the response capability of the device is defined as AC noise. Noise of this type is usually generated within a subsystem by high speed switching. Such noise, whether it be internally or externally generated, may be propagated directly along signal lines, or may be capacitively or inductively coupled into them. Switching transients also appear prominently on power supply lines, particularly in very high speed systems.

AC noise immunity is a measure of a circuit's ability to maintain the prescribed logic state in the presence of such noise. AC noise immunity is defined in terms of the amplitude and pulse width of an input noise signal to which the element will not respond. Rejection of positive-going AC noise on the ground line is required for the "0" input state of the device and of negative-going AC noise on the power supply line for the "1" input state of the device. As the pulse width of the noise signal increases, the amplitude of that noise signal which will be rejected by a device approaches the DC noise margin for that device.

Low circuit impedances will, naturally, minimize noise coupling. For all elements in the 8000 Series, a saturated switching transistor provides a desirable low output impedance in the output "0" state. The active output pull-up configuration provides low output impedance in the output "1" state.

Since the prime source of AC noise within a system is the switching transient associated with all very high speed circuitry, proper design attention to layout, termination, and board fabrication should be exercised, when very high speed elements are used.

In general, the 8400 group of elements is less susceptible to AC noise than is the 8800 group, as illustrated in Figure 1. This is attributable to the faster response of the 8800.

Typical AC noise immunity curves are furnished to provide the systems designer with a relative descrip-

tion of the AC noise immunity of the devices available in the 8000 family.

DC LOADING

Table 1-4 is a DC loading chart containing normalized fan-out information. All DC load factors are normalized with respect to an 8480 input which is considered as one DC load (0.8 mA). The chart also provides a fan-out capability for each element based on its ability to drive multiples of the normalized input load. The loading chart is guaranteed by data table test limits and conditions covering "1" Output Voltage, "0" Output Voltage, "1" Input Current, and "0" Input Current. It is applicable over the temperature range and power supply range of 4.75V to 5.25V with full temperature differential and power supply differential of 0.5V between driving and driven elements. Note in Table 1-4 the S_C, R_C inputs of the 8424 and 8425 are rated at a normalized DC load of 1.5 instead of .75 as would be indicated by the test limit in Section 2. The additional load rating is required due to transient current which will flow during the positive-going transition of the clock input signal of the 8424 and 8425.

To Use The Normalized DC Loading Chart

In Table 1-4, sum the normalized load rating of the driven elements under consideration. In the same table, find the normalized fan-out rating of the driving unit under consideration. The sum of the load ratings of the driven elements should not exceed the normalized fan-out of the driving element.

The chart presents the worst case loading rules over the temperature range and power supply range of 4.75V to 5.25V.

AC vs DC LOADING

The effect that AC loads have on turn-off and turn-on times is to increase the rise and fall times. If the designer wishes to stay within the maximum switching times guaranteed on the data sheet, he should use the emperically arrived at relationship that one AC load is approximately equivalent to three DC loads. It must be pointed out, however, that even though DC loads have approximately 3pF per load, the prime effect on the output is a decrease in "0" and "1" level noise immunity, whereas, AC loads only increase the switching times.

AC LOADING

The clock inputs of the 8424 and 8425, dual RS/T binaries, and the 8826 and 8827, dual J-K binaries, being capacitively coupled, are defined as AC loads.

The AC fan-out ratings shown in Table 1-5 are provided to assure compatibility, under worst case conditions, between driving elements and AC binary clock lines. AC fan-out is guaranteed by virtue of the output fall-time test in each of the test tables in Section 2. The fall-time test is conducted under the specific conditions of load capacitance, voltage transition and allowable transition time necessary to assure reliable triggering of the binary under worst case conditions. The relevant test procedures are given in Section 3.

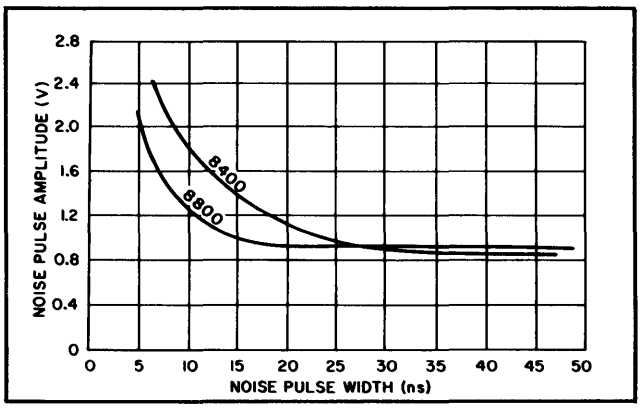
To Use The AC Loading Chart

The system designer need only follow the AC fan-out loading rules in Table 1-5 when driving AC clock lines. This will assure reliable system operation under worst case conditions.

PROPAGATION DELAY

Table 1-6 provides propagation delay information which is guaranteed under test conditions specified in Section 2. Propagation delay for the 8400 gates is defined in terms of pair delay, or the delay through two gates. The condition of the pair delay tests represents system conditions producing maximum system delays. The first gate, whose rising output waveform is under consideration, drives a full-rated capacitance and minimum current load.

FIGURE 1 – AC NOISE CHARACTERISTICS



The second gate, whose falling output waveform is under consideration, drives a full-rated capacitance and current load. This test method provides repeatability which is unattainable with other common methods of specifying propagation delay since the measurement is made between two sharply falling waveforms.

Propagation delay for the 8000 series elements is presented in terms of T_{on} and T_{off} which provides a figure of merit by which to compare similar products tested under the same conditions. The guaranteed delay times in the chart take into consideration the "1" and "0" input current and the load capacitance associated with the information presented in Table 1-4. Test conditions for the propagation delay guarantees are presented in Section 3.

POWER CONSUMPTION

Power consumption in the 8400 group is primarily DC in nature and power supply designs should take the DC power consumption limits into consideration. The 8800 group, like all high speed designs, has an AC power consumption component in addition to the DC power consumption. Increases in system operating frequency produces increases in the magnitude of the AC power consumption. Typical AC power consumption curves are provided in Section 2 and should be considered in power supply designs for high frequency subsystems.

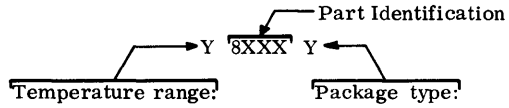
Table 1-7 provides guaranteed DC power consumption and current drain limits for the 8000 family for conditions presented in Section 2.

CLAMP DIODES

All 8800 and 8H00 gates have input clamp diodes which present a very low impedance to negative voltage swings and minimize the effects of ringing.

TABLE 1-1 – TEMPERATURE RANGES AND PACKAGE TYPES

Example: S8829A



"S" = -55°C to +125°C

"N" = 0°C to +75°C

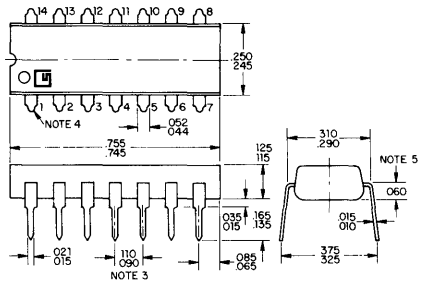
"A" = 14-pin dual in-line silicone package (TO-116)

"B" = 16-pin dual in-line silicone package

"J" = 14-pin flat-pak, glass-kovar (TO-88)

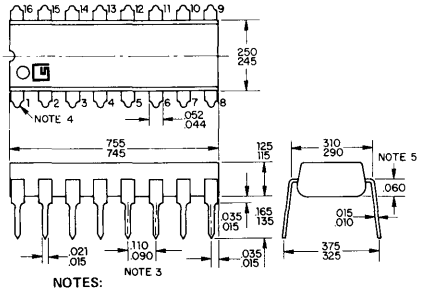
"Q" = 14-pin flat-pak, ceramic (TO-88)

A PACKAGE (TO-116)



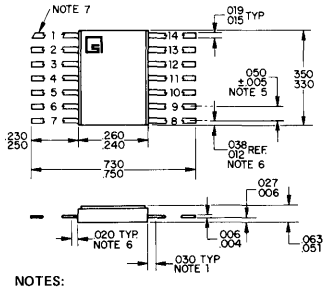
NOTES:
1. Lead material: Kovar, solder coated.
2. Body material: Silicone molded.
3. Tolerances non-cumulative.
4. Signetics symbol denotes lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal resistance: Θ_{J-A} = 0.160°C/mW.

B PACKAGE



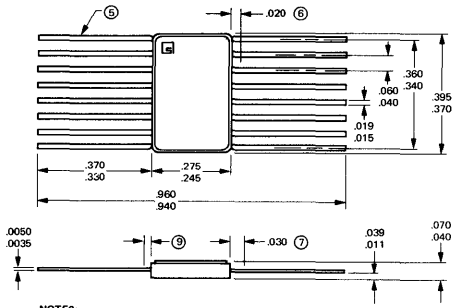
NOTES:
1. Lead material: Kovar, solder coated.
2. Body material: Silicone molded.
3. Tolerances non-cumulative.
4. Signetics symbol denotes lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ_{J-A} = 0.16°C/mW.

J PACKAGE (TO-88)



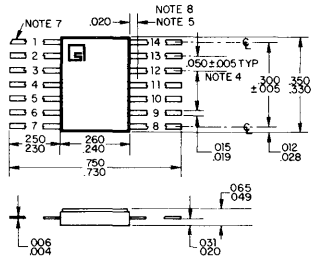
NOTES:
1. Recommended minimum offset before lead bend.
2. All leads weldable and solderable.
3. Thermal resistance: Θ_{J-A} = 0.3°C/mW.
4. All dimensions in inches.
5. Tolerances are non-cumulative.
6. Lead spacing dimensions apply to this area only.
7. Signetics symbol or angle cut identifies lead No. 1.

R PACKAGE



NOTES:
1. Lead Material: Kovar or equivalent, gold plated
2. Body Material: Top ring & base – Kovar or equivalent, gold plated, glass body
3. Lid Material: Kovar or equivalent, gold plated, alloy seal
4. Tolerances non cumulative
5. Signetics symbol denotes Lead #1
6. Lead spacing shall be measured within this zone
7. Recommended minimum offset before lead bend
8. Thermal Resistance: θJ_A = .155°C/mW, θJ_C = .070°C/mW
9. Maximum glass climb: .010

Q PACKAGE (TO-88)



NOTES:
1. Lead material: Kovar or Rodar, Gold plated.
2. Body material: Ceramic with glass seals.
3. Lid material: Kovar or Rodar.
4. Tolerances non-cumulative.
5. Lead spacing controlled within this distance, 2 sides.
6. .010 maximum glass climb allowed on leads, 2 sides.
7. Signetics symbol or angle cut identifies lead No. 1.
8. Recommended minimum offset before lead bend.
9. Thermal resistance: Θ_{J-A} = 0.1°C/mW.

RECOMMENDED OPERATING VOLTAGE FOR ALL DCL ELEMENTS: 5V ±5%

TABLE 1-2 – ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 6)

ELEMENT (NOTE 2)	INPUT VOLTAGE	OUTPUT VOLTAGE	V_{CC} (NOTE 4)	INPUT CURRENT	OUTPUT CURRENT
8162	+ 5.5V	+ 7.0V	+7.0V	±30 mA	±100 mA
841X	+ 5.5V	+ 7.0V	+7.0V	±10 mA	± 30 mA
842X	+ 5.5V	+ 7.0V	+7.0V	±10 mA	+ 30, -10 mA
8440	+ 5.5V	+ 7.0V	+7.0V	±10 mA	+ 30, -10 mA
8455	+ 5.5V	+ 7.0V	+7.0V	±10 mA	±100 mA
847X	+ 5.5V	+ 7.0V	+7.0V	±10 mA	+ 30, -10 mA
848X	+ 5.5V	+ 7.0V	+7.0V	±10 mA	+ 30, -10 mA
87XX	+ 5.5V	+ 7.0V	N/A	±10 mA	NOTE 5
88XX	+ 5.5V	+ 7.0V	+7.0V	±30 mA	±100 mA
8HXX	+ 5.5V	+ 7.0V	+7.0V	±30 mA	±100 mA
8T18	+50.0V	+ 6.0V	NOTE 3	±30 mA	+ 30, -10 mA
8T80	+ 5.5V	+40.0V	+7.0V	±10 mA	+100, -10 mA
8T90	+ 5.5V	+40.0V	+7.0V	±10 mA	+100, -10 mA

Notes:

1. All devices must be derated at elevated temperatures based on the following:

   Junction Temperature:
   150°C for J package.
   200°C for Q and R packages.
   175°C for A and B packages.
   Thermal Resistance:
   300°C/W for J package.
   160°C/W for A and B packages.
   136°C/W for Q package.

2. These device designations are for all package configureations (A,B,J,Q or R) and all rated temperature ranges (-55°C to +125°C,or 0%C to +75°C).

3. For the 8T18, V_{CC} is V_{CC_1}= 7.0V and V_{CC_2}= +35V.

4. Operating V_{CC} for the 8000 Series is specified at +5.0V ±5% .

5. See data sheet.

6. Storage temperature for all DCL elements are from -65°C to maximum junction temperatures as defined in Note 1.

TABLE 1-3 – GUARANTEED WORST CASE DC NOISE MARGIN

DRIVING ELEMENT	OUTPUT STATE	DRIVEN INPUT (mV)						
		ALL 8400 GATES	8424, 8425 $S_D R_D S_C R_C$	ALL 8800 GATES	8821/22/24/25 8828/29 ALL INPUTS	8826/27 S_D, R_D/J, K	8H16/70/80	8H20/21/22
ALL 8400 GATES	"0"	350	350	450	450	350/450	450	450
	"1"	1400	1400	1400	1400	1400/1400	1400	1400
8424 8425	"0"	350	350	350	450	350/450	450	450
	"1"	1400	1400	1400	1400	1400/1400	1400	1400
ALL 8800 GATES	"0"	300	300	400	400	300/400	400	400
	"1"	600	600	600	600	600/600	600	600
8821/22/24/25 8828, 8829	"0"	300	300	400	400	300/400	400	400
	"1"	600	600	600	600	600/600	600	600
8826 8827	"0"	300	300	400	400	300/400	400	400
	"1"	600	600	600	600	600/600	600	600
8162	"0"	300	300	400	400	300/400	400	400
	"1"	1400	1400	1400	1400	1400/1400	1400	1400

TABLE 1-3 – GUARANTEED WORST CASE DC NOISE MARGIN (Cont.)

DRIVING ELEMENT	OUTPUT STATE	DRIVEN INPUT (mV)						
		ALL 8400 GATES	8424, 8425 $S_D R_D S_C R_C$	ALL 8800 GATES	8821/22/24/25 8828/29 ALL INPUTS	8826/27 S_D, R_D/J, K	8H16/70/80	8H20/21/22
8H16 8H70 GATES 8H80 8H90	"0"	300	300	400	400	300/400	400	400
	"1"	600	600	600	600	600/600	600	600
8H20 8H21 8H22	"0"	300	300	400	400	300/400	400	400
	"1"	600	600	600	600	600/600	600	600

TABLE 1-4 – GUARANTEED WORST CASE DC LOADING

PART NUMBER	NORMALIZED LOAD RATING	NORMALIZED FAN-OUT RATING
8162		12.0
8415	1.5	9.0
8416	1.5	9.0
8417	1.5	9.0
8424	RESET: 1.0 R_C, S_C: 1.5	9.0
8425	RESET: 2.0 SET: 1.0 R_C, S_C: 1.5	9.0
8440	1.0	9.0
8455	1.5	25.0
8470/80/90	1.0	9.0
8471/81	1.0	9.0
8706/8731	1.5	Expander
8806	2.0	Expander
8808	2.0	20.0
8816	2.0	20.0
8821	RESET: 8.0 SET: 4.0 J, K: 2.0 CLOCK: 8.0	20.0

TABLE 1-4 – GUARANTEED WORST CASE DC LOADING (Cont.)

PART NUMBER	NORMALIZED LOAD RATING	NORMALIZED FAN-OUT RATING
8822/24	RESET: 4.0 SET: (8824 only) 4.0 J, K: 2.0 CLOCK: 4.0	20.0
8825	SET, RESET: 4.0 J_1, J_2, $\overline{J}$: 2.0 K_1, K_2, $\overline{K}$: 2.0 CLOCK: 2.0	20.0
8826	RESET: 2.5 J, K: 3.0	10.0
8827	RESET: 5.0 SET: 2.5 J, K: 3.0	10.0
8828	SET: 4.0 RESET: 6.0 DATA: 2.0 CLOCK: 4.0	20.0
8829	SET, RESET: 6.0 J_1, J_2, J_3: 2.0 K_1, K_2, K_3: 2.0 CLOCK: 2.0	20.0
8840/48	2.0	20.0
8855	2.0	60.0
8815/75/85	2.0	20.0
8870/80	2.0	20.0
8881	2.0	20.0
8H16/70/80/90	3.0	30.0
8H20/22	SET: 3.0 RESET: 3.0 J, K: 3.0 CLOCK: 3.0	30.0
8H21	SET: 3.0 RESET: 6.0 J, K: 3.0 CLOCK: 6.0	30.0

TABLE 1-4 – GUARANTEED WORST CASE DC LOADING (Cont.)

PART NUMBER	NORMALIZED LOAD RATING	NORMALIZED FAN-OUT RATING
8T18	High Voltage Input (See Data Sheet)	10.0
8T80	2.0	High Voltage Output (See Data Sheet)
8T90	2.0	High Voltage Output (See Data Sheet)

TABLE 1-5 – GUARANTEED WORST CASE AC LOADING

ELEMENT	DRIVEN CLOCK INPUTS				
	8162	8424	8425	8826	8827
8162	2	3	1	3	1
8415*	-	-	-	-	0
8416	1	2	1	1	0
8417*	-	-	-	-	0
8424	1	2	1	1	0
8425	1	2	1	1	0
8440	1	2	1	1	0
8455	4	9	4	3	1
8470	1	2	1	1	0
8480/90	1	2	1	1	0
8471*	-	-	-	-	0
8481*	-	-	-	-	0
8808	3	6	3	6	3
8816	3	6	3	6	3
8870	3	6	3	6	3
8880	3	6	3	6	3
8881*	-	-	-	-	-
8815	3	6	3	6	3
8875	3	6	3	6	3
8885	3	6	3	6	3
8821	3	6	3	6	3
8822	3	6	3	6	3
8824	3	6	3	6	3
8825	3	6	3	6	3

*Not recommended due to pull-up resistor requirements.

TABLE 1-5 – GUARANTEED WORST CASE AC LOADING (Cont.)

ELEMENT	DRIVEN CLOCK INPUTS				
	8162	8424	8425	8826	8827
8826	1	2	1	2	1
8827	1	2	1	2	1
8828	3	6	3	6	3
8829	3	6	3	6	3
8840	3	6	3	6	3
8848	3	6	3	6	3
8855	5	10	5	10	5
8H16	3	6	3	6	3
8H70	3	6	3	6	3
8H80/90	3	6	3	6	3
8H20	3	6	3	6	3
8H21	3	6	3	6	3
8H22	3	6	3	6	3
8T18	1	2	1	1	0

TABLE 1-6 – GUARANTEED PROPAGATION DELAY LIMITS

ELEMENT	MAXIMUM PAIR DELAY **	TYPICAL PAIR DELAY **	MINIMUM TOGGLE RATE †	TYPICAL TOGGLE RATE †	MAXIMUM		TYPICAL	
					TURN ON **	TURN OFF **	TURN ON **	TURN OFF **
8162					45	60	27	30
8415	150	85			40	50	30	30
8416	95	60			60	40	30	30
8417	150	85			40	50	30	30
8424			8	11	60	60	30	30
8425			8	11	60	60	30	30
8440	95	60			40	50	30	30
8455	95	60			40	40	30	30
8470	95	60			40	40	30	30
8480	95	60			40	40	30	30
8471	150	85			40	40	30	30
8481	150	85			40	40	30	30
8806*					15	30	10	20
8808					13	13	8	8
8816					13	13	8	8

* Times include 8840 gate delay.
** All times are in nanoseconds.
† Toggle rates are in megahertz.

TABLE 1-6 – GUARANTEED PROPAGATION DELAY LIMITS (Cont.)

ELEMENT	MAXIMUM PAIR DELAY **	TYPICAL PAIR DELAY **	MINIMUM TOGGLE RATE †	TYPICAL TOGGLE RATE †	MAXIMUM		TYPICAL	
					TURN ON **	TURN OFF **	TURN ON **	TURN OFF **
8870					13	13	8	8
8880					13	13	8	8
8881					20	30	15	20
8815					13	13	8	8
8875					13	13	8	8
8885					13	13	8	8
8821			10	25	50	50	25	15
8822			10	25	50	50	25	15
8824			10	25	50	50	25	15
8825			15	25	50	50	27	32
8826			25	30	35	20	17	8
8827			25	30	35	20	17	8
8828				25	50	35	28	20
8829			15	25	50	50	16	25
8840					13	13	8	8
8848					13	13	8	8
8855					15	15	10	10
8H16					10	10	5	5
8H70					10	10	5	5
8H80					10	10	5	5
8H90					10	10	5	5
8H20			50	75			10	8
8H21			50	75			10	8
8H22			50	75			10	8
8T18					20	70	12	35
8T80					55	95	35	40
8T90					55	95	35	40

** All times are in nanoseconds

† Toggle rates are in megahertz..

TABLE 1-7 – GUARANTEED POWER CONSUMPTION LIMITS PER GATE OR BINARY

V_{CC} = +5.25V T_A = 25°C

ELEMENT	OUTPUT STATE	POWER CONSUMPTION (mW)	CURRENT DRAIN (mA)	AVERAGE POWER CONSUMPTION (mW)	AVERAGE CURRENT DRAIN (mA)
8162	"0"	85	16.2	92.5	17.6
	"1"	100	19.0		
8415	"0"	22.6	4.3	15.0	2.8
	"1"	7.3	1.4		
8416	"0"	25.2	4.8	16.3	3.1
	"1"	7.3	1.4		
8417	"0"	22.6	4.3	15.0	2.8
	"1"	7.3	1.4		
8424		24.7	4.7	24.7	4.7
8425		24.7	4.7	24.7	4.7
8440	"0"	29.4	5.6	19.4	3.7
	"1"	9.5	1.8		
8455	"0"	28.4	5.4	17.8	3.4
	"1"	7.3	1.4		
8470	"0"	16.8	3.2	11.0	2.1
	"1"	5.2	1.0		
8471	"0"	16.8	3.2	11.0	2.1
	"1"	5.2	1.0		

TABLE 1-7 – GUARANTEED POWER CONSUMPTION LIMITS PER GATE OR BINARY (Cont)

V_{CC} = +5.25V T_A = 25°C

ELEMENT	OUTPUT STATE	POWER CONSUMPTION (mW)	CURRENT DRAIN (mA)	AVERAGE POWER CONSUMPTION (mW)	AVERAGE CURRENT DRAIN (mA)
8480/90	"0"	16.8	3.2	11.0	2.1
	"1"	5.2	1.0		
8481	"0"	16.8	3.2	11.0	2.1
	"1"	5.2	1.0		
8806	"0"	6.3	1.2	7.6	1.4
	"1"	8.9	1.7		
8808	"0"	31.0	5.9	20.0	3.8
	"1"	8.9	1.7		
8815	"0"	49.7	9.5	42.8	8.1
	"1"	35.6	6.8		
8816	"0"	31.0	5.9	19.1	3.8
	"1"	8.9	1.7		
8821		72	13.7	72	13.7
8822		72	13.7	72	13.7
8824		72	13.7	72	13.7
8825		132	25.1	132	25.1
8826		64	12.2	64	12.2
8827		64	12.2	64	12.2

TABLE 1-7 – GUARANTEED POWER CONSUMPTION LIMITS PER GATE OR BINARY (Cont)

V_{CC} = +5.25V T_A = 25°C

ELEMENT	OUTPUT STATE	POWER CONSUMPTION (mW)	CURRENT DRAIN (mA)	AVERAGE POWER CONSUMPTION (mW)	AVERAGE CURRENT DRAIN (mA)
8828		60	11.2	60	11.2
8829		132	25.1	132	25.1
8840	"0"	37.3	7.1	27.6	5.3
	"1"	17.9	3.4		
8848	"0"	48.8	9.3	42.3	8.1
	"1"	35.7	6.8		
8855	"0"	56.8	10.8	35.7	6.8
	"1"	14.7	2.8		
8870	"0"	31.0	5.9	20.0	3.8
	"1"	8.9	1.7		
8875	"0"	43.7	8.3	35.4	6.8
	"1"	27.1	5.2		
8880	"0"	31.0	5.9	20.0	3.8
	"1"	8.9	1.7		
8881	"0"	31.0	5.9	20.0	3.8
	"1"	8.9	1.7		
8885	"0"	37.3	7.1	27.6	5.2
	"1"	17.8	3.4		
8H16	"0"	46.2	8.8	34.6	6.4
	"1"	21.0	4.0		
8H20 8H21 8H22		90	17.2	90	17.2

TABLE 1-7 – GUARANTEED POWER CONSUMPTION LIMITS PER GATE OR BINARY (Cont)

V_{CC} = +5.25V T_A = 25°C

ELEMENT	OUTPUT STATE	POWER CONSUMPTION (mW)	CURRENT DRAIN (mA)	AVERAGE POWER CONSUMPTION (mW)	AVERAGE CURRENT DRAIN (mA)
8H70	"0"	46.2	8.8	34.6	6.4
	"1"	21.0	4.0		
8H80/90	"0"	46.2	8.8	34.6	6.4
	"1"	21.0	4.0		
8T18	"0"	44.6	8.5	22.8	4.4
	"1"	1.0	0.2		
8T80	"0"	20.0	3.8	14.0	2.7
	"1"	7.9	1.5		
8T90	"0"	20.0	3.8	14.0	2.7
	"1"	7.9	1.5		

MOS

Signetics offers a broad line of MOS products including Dynamic and Static Shift Registers, Random Access Memories and Read-only Memories. The 2500 series is fabricated using Signetics' advanced P-Channel SILICON-GATE PROCESS which provides compatibility with 5 volt TTL/DTL, high speed, and low power dissipation. Also available are the 2000 and 2400 series which are P-Channel metal gate devices. MOS products are available in commercial temperature ranges. All silicon gate devices are available in silicone dual in-line packages.

DYNAMIC SHIFT REGISTERS

2502
Quad 256-Bit
10MHz Typ. Data Rate
C_{CL} = 140pF max.
Power Supplies +5, -5V
40μW/bit/MHz
Multiplexed Data

2503
Dual 512-Bit
10MHz Typ. Data Rate
C_{CL} = 140pF max.
Power Supplies +5, -5V
40μW/bit/MHz
Multiplexed Data

2504
Single 1024-Bit
10MHz Typ. Data Rate
C_{CL} = 140pF max.
Power Supplies +5, -5V
40μW/bit/MHz
Multiplexed Data

2505/2524
512-Bit
5MHz Typ. Clock Rate
C_{CL} = 80pF
Power Supplies +5, -5V
100μW/bit/MHz
Recirculate Logic

2506
Dual 100-Bit
5MHz Typ. Clock Rate
C_{CL} = 40pF max.
Power Supplies +5, -5V
400μW/bit/MHz
Bare Drain Output

2507
Dual 100-Bit
5MHz Typ. Clock Rate
C_{CL} = 40pF max.
Power Supplies +5, -5V
400μW/bit/MHz
Resistor Pull-down (7.5K)

2512/2525
1024-Bit
5MHz Typ. Clock Rate
C_{CL} = 140 pF
Power Supplies +5, -5V
150μW/bit/MHz
Recirculate Logic

2515
Dual 512-Bit DSR
5MHz Clock Rate
C_{CL} = 140pF
Power Supplies +5, -5
100μW/bit/MHz
Recirculate +CS logic

2517
Dual 100-Bit
5MHz Typ. Clock Rate
C_{CL} = 40pF max.
Power Supplies +5, -5V
400μW/bit/MHz
Resistor Pull-down (20K)

STATIC SHIFT REGISTERS

2509
Dual 50 Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Tri-State Outputs
Recirculate Logic
Power Supplies +5, -5, -12V

2510
Dual 100-Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Tri-State Outputs
Recirculate Logic
Power Supplies +5, -5, -12V

2511
Dual 200-Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Tri-State Outputs
Recirculate Logic
Power Supplies +5, -5, -12V

2518
Hex 32-Bit
2MHz Typ. Clock Rate
Data & Clock TTL Compatible
Recirculate Logic
Power Supplies +5, -12V

2519
Hex 40-Bit
2MHz Typ. Clock Rate
Data & Clock TTL Compatible
Recirculate Logic
Power Supplies +5, -12V

2521
Dual 128-Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Recirculate Logic
Power Supplies +5, -12V

2522
Dual 132-Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Recirculate Logic
Power Supplies +5, -12V

2000 SERIES
Static Shift Registers
C_L = 5pF
-14, -28V Power Supplies

2001
Dual 16-Bit SSR
0-1MHz

2002
Dual 25-Bit SSR
0-1MHz

2003
Dual 32-Bit SSR
0-1MHz

2004
Dual 50-Bit SSR
0-1MHz

2005
Dual 100-Bit SSR
0-1MHz

2010
Dual 100-Bit SSR
0-3MHz

RANDOM ACCESS MEMORIES

2501
256x1 Static RAM
Decoded
Access Time 1us Max.
1mW/bit Typ.
Power Supplies +5, -7, -10V or
+5, -9, -9V

2508
1024 x 1 Dynamic RAM
Decoded
Access Time 330ns
Cycle Time 500ns
3 Chip Selects
2.7mA
4 Clocks
+5, -12V
TTL Compatible Inputs
100mW

READ-ONLY MEMORIES

2513
64x8x5 Static Character Generator
Row Output
600ns Max. Access Time
ASCII Font Std.
Power Supplies +5, -5, -12V
350mW

2514
512x5 Read-Only Memory
600ns Max. Access Time
Power Supplies +5, -5, -12V
350mW

2516
64x6x8 Static Character Generator
Column Output
750ns Max. Access Time
Power Supplies +5, -5, -12V
415mW

2400 SERIES
Static Read-Only Memories
550ns Access Time
250mW
+12, -12V Power Supplies
Bare Drain or MOS Pull-Down
Resistor

2410
256x4
16-pin DIP

2420
256x4, 128x8
Single or 3-line Chip Enable
24-pin DIP

2430
256 x 8, 512 x 4
Single or 3-line Chip Enable
24-pin DIP

SECTION 2-ELECTRICAL CHARACTERISTICS

This section contains specific test limit and test condition information for use in device evaluation and incoming inspection for DC parameters. AC test circuits are contained in the following section.

Circuit diagrams and product descriptions are also contained in this section to provide assistance in evaluating specific devices and total 8000 Series flexibility.

For many devices, typical curves, describing the product's operating characteristics, are included. These curves are not guaranteed, but are intended to provide additional, useful information for device evaluation.

Unless otherwise specified, all devices are available in the "S" and "N" temperature ranges ("S" = -55°C to +125°C, "N" = 0°C to +75°C), and in the silicone dual in-line package (A or B), and the flat package (J Q or R).

TTL/MOS INTERFACE

The Darlington-type output structure of most 8800 Series gates and flip-flops provides a high logic "1" output level at low output currents. These circuits typically offer an unloaded output voltage separated from V_{CC} by only one diode drop. Since the Signetics 2500 Series Silicon Gate MOS has a minimum threshold of 3.2V, the 8800 Series elements can drive the 2500 Series directly without the need for an external pull-up resistor.

The devices listed in Table 2-1 are all guaranteed to provide 3.6V at 10uA output current. Under worst case conditions, this results in a minimum guaranteed "1" level noise margin of 400mV when the MOS and TTL V_{CC} supplies are tied together.

GATE		FLIP-FLOPS	
8808	Single 8-Input Nand Gate	8821	Dual Master-Slave J-K Binary
8815	Dual 4-Input Nor Gate	8822	Dual Master-Slave J-K Binary
8816	Dual 4-Input Nand Gate	8824	Dual Master-Slave J-K Binary
8840	Dual Expandable and-or-Invert Gate	8825	DC Clocked J-K Binary
8848	Expandable and-or-Invert Gate	8826	Dual J-K Binary
8870	Triple 3-Input Nor Gate	8827	Dual J-K Binary
8875	Triple 3-Input Nor Gate	8829	High Speed J-K Binary
8880	Quad 2-Input Nand Gate		
8885	Quad 2-Input Nor Gate		

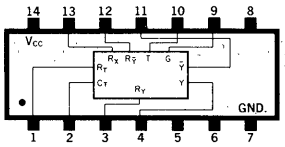
SIGNETICS

DCL

INTEGRATED CIRCUITS

8162 MONOSTABLE MULTIVIBRATOR

A PACKAGE



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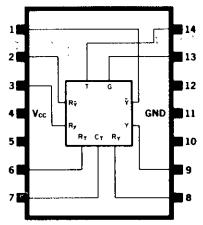


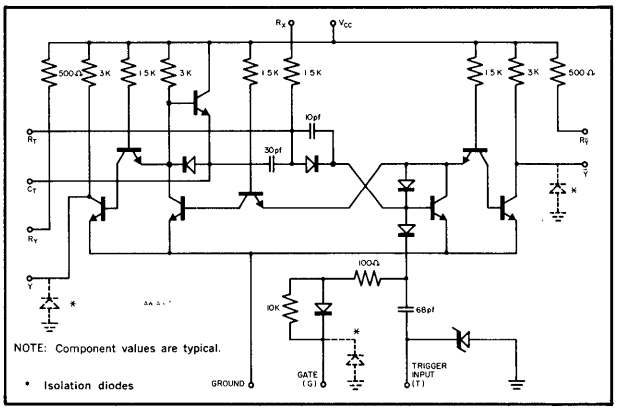
8162

The 8162 Monostable Multivibrator is intended for use in high-speed, low-power digital systems.

Among the features of this device are complementary buffered outputs, high noise immunity, excellent pulse width tolerance capability and high duty cycle (to 75%). The unit is very versatile in pulse-shaping and delay applications, and provides delays over the range of 80ns to 2 seconds by using appropriate external components. Complete isolation of the timing stage and the output stage allows very fast fall times, even at wide pulse widths. If the internal timing resistor (R_X) is used, pulse width is approximately 1ms per microfarad of external capacitance.

Applications and usage information is provided in Section 4 of this handbook.

BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (NOTES: 1,2,3,4,5) STANDARD CONDITIONS: $R_X = V_{CC}$, GATE = GROUND

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8162	TEMP. N8162	V_{cc}	R_T	TOGGLE INPUT	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE (Y)	3.4			V	-55°C	0°C	4.75V	0V		-300μA	6
A-3		3.6			V	+25°C	+25°C	5.00V	0V		-300μA	6
A-4		3.4			V	+125°C	+75°C	4.75V	0V		-300μA	6
A-5	"1" OUTPUT VOLTAGE ($\overline{Y}$)	3.4			V	-55°C	0°C	4.75V			-300μA	6
A-3		3.6			V	+25°C	+25°C	5.00V			-300μA	6
A-4		3.4			V	+125°C	+75°C	4.75V			-300μA	6
A-5	"0" OUTPUT VOLTAGE (Y)			0.35	V	-55°C	0°C	4.75V			9.6mA	8
A-3				0.35	V	+25°C	+25°C	5.00V			9.6mA	8
A-4				0.40	V	+125°C	+75°C	4.75V			9.6mA	8
C-1				0.35	V	-55°C	0°C	4.75V			1.6mA	8, 13
A-5	"0" OUTPUT VOLTAGE ($\overline{Y}$)			0.35	V	-55°C	0°C	4.75V	0V		9.6mA	8
A-3				0.35	V	+25°C	+25°C	5.00V	0V		9.6mA	8
A-4				0.40	V	+125°C	+75°C	4.75V	0V		9.6mA	8
C-1				0.35	V	-55°C	0°C	4.75V	0V		1.6mA	8, 13
A-3	CLOCK INPUT "1" CURRENT			150	nA	+25°C	+25°C	5.00V		5.0V		
A-4				15	μA	+125°C	+75°C	5.25V		5.25V		
A-3	LOAD RESISTOR CURRENT (R_Y)	-7.8		-12.3	mA	+25°C	+25°C	5.00V				12
A-3	LOAD RESISTOR CURRENT ($R_{\overline{Y}}$)	-7.8		-12.3	mA	+25°C	+25°C	5.00V				12
A-3	TIMING RESISTOR CURRENT	-2.75		-4.2	mA	+25°C	+25°C	5.00V	0V			
A-2	OUTPUT "1" POWER DISSIPATION (Y)			100	mW	+25°C	+25°C	5.25V	0V			
A-2	OUTPUT "0" POWER DISSIPATION (Y)			85	mW	+25°C	+25°C	5.25V				
C-2	EFFECTIVE TRIGGER INPUT CAPACITANCE			75	pf	+25°C	+25°C	5.00V		2.0V		7, 11
A-6	TURN-OFF DELAY (Y)			60	ns	+25°C	+25°C	5.00V			D.C. F.O. = 1	9, 14
A-6	TURN-ON DELAY ($\overline{Y}$)$_L$			45	ns	+25°C	+25°C	5.00V			D.C. F.O. = 12	9, 14
A-6	OUTPUT PULSE WIDTH (Y)	25		80	ns	+25°C	+25°C	5.00V			D.C. F.O. = 12	9, 14
A-6	OUTPUT PULSE WIDTH ($\overline{Y}$)	25		80	ns	+25°C	+25°C	5.00V			D.C. F.O. = 12	9, 14
A-6	OUTPUT PULSE WIDTH (Y) WITH C EXTERNAL = 250pf	175			ns	+25°C	+25°C	5.00V			D.C. F.O. = 12	9, 14
C-2	OUTPUT FALL TIME ($\overline{Y}$)			50	ns	-55°C	0°C	4.75V			A.C. F.O. = 3	10, 14
A-2	OUTPUT SHORT CIRCUIT CURRENT (Y)	-1.25		-2.25	mA	+25°C	+25°C	5.00V	0V			
A-2	OUTPUT SHORT CIRCUIT CURRENT ($\overline{Y}$)	-1.25		-2.25	mA	+25°C	+25°C	5.00V				

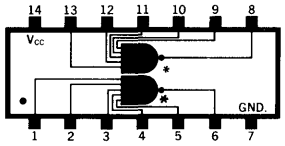
Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV$_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Due to input falling rate requirements, the trigger input represents two standard AC loads or 100pf.
12. Tie resistor pins R_Y and $R_{\overline{Y}}$ to zero volts.
13. Tie resistor R_Y and $R_{\overline{Y}}$ to Y and $\overline{Y}$ respectively.
14. Detailed test conditions for AC testing are in Section 3.

SIGNETICS DCL INTEGRATED CIRCUITS

8415 DUAL 5-INPUT NAND GATE

A PACKAGE



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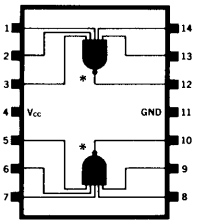


* No pull-up provided

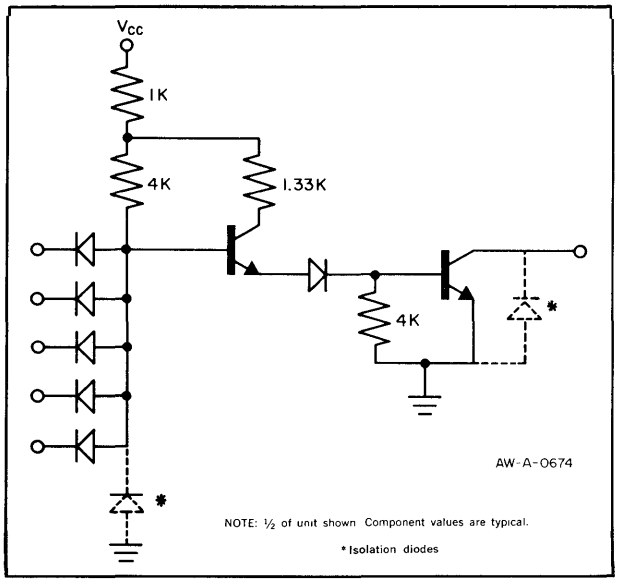
8415

The 8415 is a Dual 5-Input NAND Gate with bare output collectors. Absence of an output pull-up structure allows the user complete freedom in the use of the 8415 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 30 outputs to be tied together.

Collector logic, using the 8415, can provide increased system flexibility and lower system cost due to reduced can count.

Section 4 of this handbook provides detailed usage rules and collector-logic information for this element.

BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (NOTES: 1,2,3,4,5,6,12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8415	TEMP. N8415	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			40	μA	+125°C	+75°C	5.0V	0.7V			11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	8.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	8.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	8.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-1.2	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-1.2	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-1.2	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	0V			
A-6	PAIR DELAY	50		150	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9
C-2	FALL TIME			75	ns	-55°C	0°C	4.75V			A.C. F.O. = 2	10
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9,14
C-2	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.0V			D.C. F.O. = 1	9,14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			22.6	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			7.3	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT VOLTAGE RATING	7.0			V	+25°C	+25°C	5.0V	0V			13

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Connect an external 1K ±1% resistor from V_{cc} to the output terminal for this test.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Connect an external 1K ±1% resistor from 6.3V to the output terminal.
14. Detailed test conditions for AC testing are in Section 3.

SIGNETICS DCL INTEGRATED CIRCUITS

8416 DUAL 4-INPUT EXPANDABLE NAND GATE

The 8416 Dual 4-Input Expandable NAND Gate implements the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

The DTL input structure provides an expansion node for logic flexibility. The compatibly characterized 8731 diode expander is recommended for this purpose.

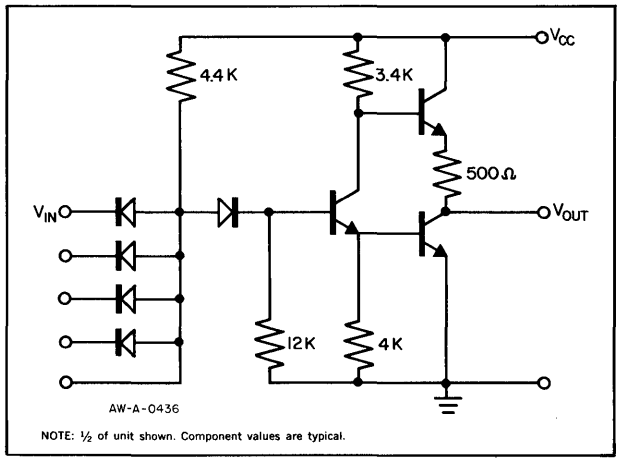
The active output structure of the 8416 provides high AC noise immunity due to it's low output impedance in both the "1" and "0" output states.

Output short circuit protection is provided by a current limiting resistor.

The values chosen for the collector and emitter resistors of the phase-splitter transistor, ensure optimum on-off relationships of the totem-pole output pair.

Section 4 of this handbook provides helpful usage rules and applications for the 8416.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

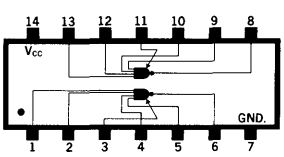
ELECTRICAL CHARACTERISTICS (NOTES: 1,2,3,4,5,6,12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8416	TEMP. N8416	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	3.4			V	-55°C	0°C	4.75V	0.7V		-225μA	8
A-3		3.6			V	+25°C	+25°C	5.0V	0.7V		-225μA	8
A-4		3.4			V	+125°C	+75°C	4.75V	0.7V		-225μA	8
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	9
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	9
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.2	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-1.2	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-1.2	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-3	EXPANDER NODE	-0.1			mA	+25°C	+25°C	5.0V	0V			
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	30		95	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 13
C-2	FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 2	11, 13
C-2	TURN-ON DELAY			60	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 13
C-2	TURN-OFF DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 1	10, 13
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			25.2	mW	+25°C	+25°C	5.25V				
A-2	(Per Gate) OUTPUT "1"			7.3	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-4.0		-12.0	mA	+25°C	+25°C	5.0V	0V		0V	

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50 pf.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.

A PACKAGE



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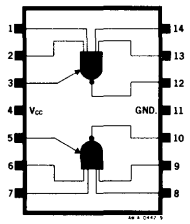
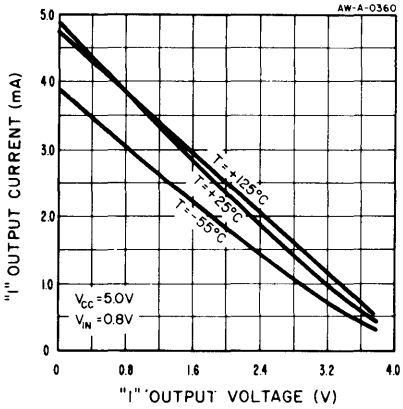
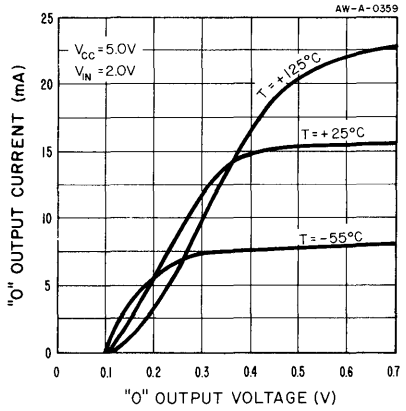
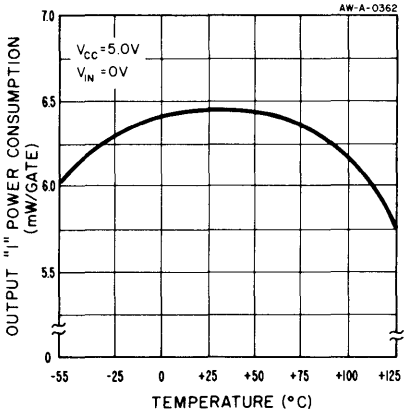
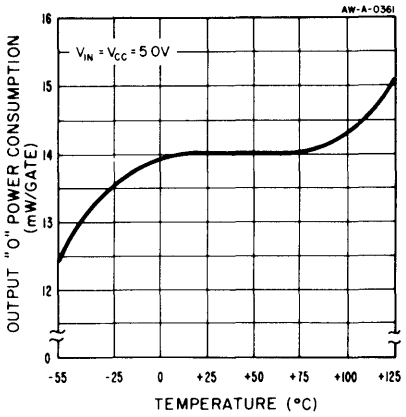


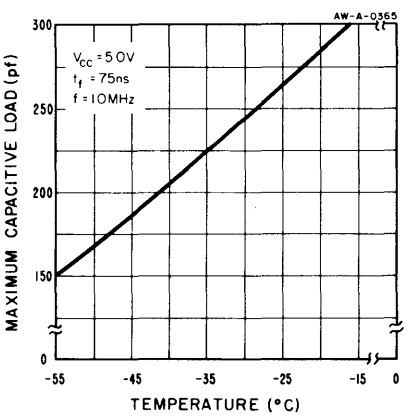
8416

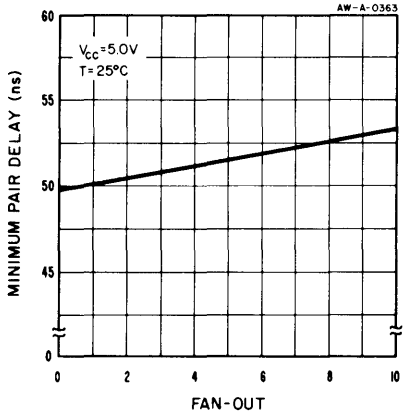


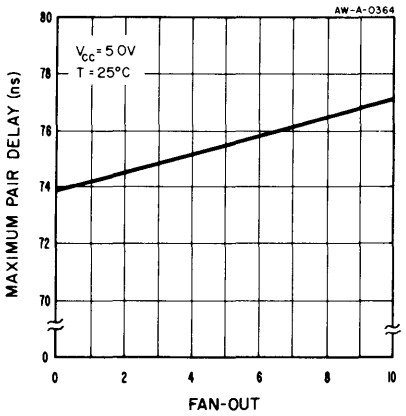


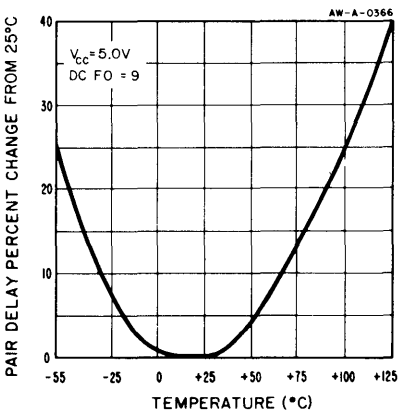












SIGNETICS DCL INTEGRATED CIRCUITS

8417 DUAL 3-INPUT EXPANDABLE NAND GATE

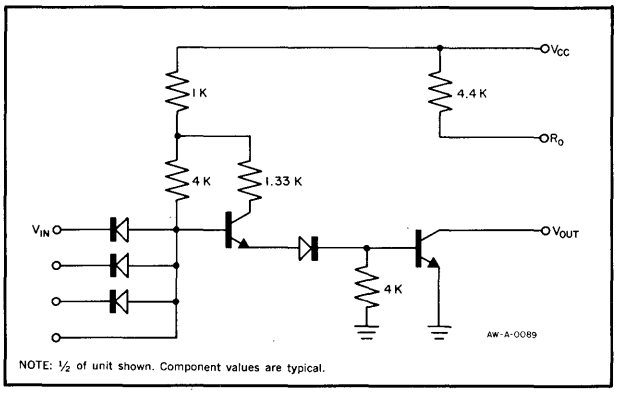
The 8417 Dual 3-Input Expandable NAND Gate implements the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

The optional pull-up resistor allows collector logic, or wired-AND, to be easily implemented. By paralleling optional pull-up resistors of two or more gates or by selecting discrete external pull-up resistors, more than 30 collectors may be tied together. The optional resistor is brought out at the pin adjacent to the output pin to simplify board layout when it is used.

An expansion node is provided for system flexibility. The compatibly characterized 8731 Diode Expander is recommended for this purpose.

Section 4 of this handbook provides helpful usage rules, including collector logic techniques, and applications for the 8417.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8417	TEMP. N8417	V_{CC}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			40	µA	+125°C	+75°C	5.0V	0.7V			11, 12
	OUTPUT LOAD RESISTOR	3.5	4.4	5.3	KΩ	+25°C	+25°C	5.0V				11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-1.2	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-1.2	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-1.2	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-3	EXPANDER NODE	-0.1			mA	+25°C	+25°C	5.0V	0V			
A-4	"1" INPUT CURRENT			25	µA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	50		150	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	9, 14
C-2	FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 2	10, 14
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	9, 14
C-2	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.0V			D.C.F.O. = 1	9, 14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			22.6	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			7.3	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50µA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-0.94		-1.45	mA	+25°C	+25°C	5.0V	0V		0V	

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Optional pull-up resistor not connected to output.
12. Connect an external 1K ±1% resistor from V_{cc} to the output terminal for this test.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.

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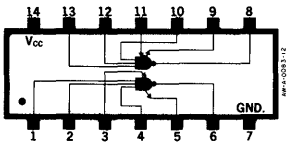

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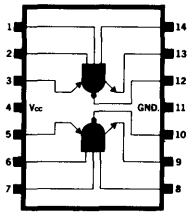

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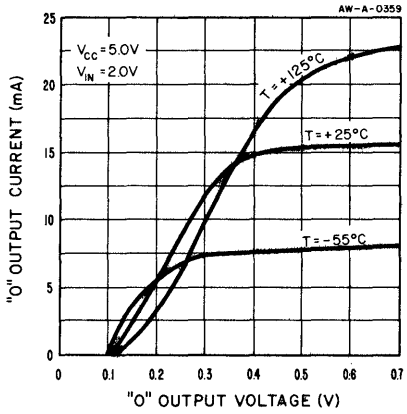
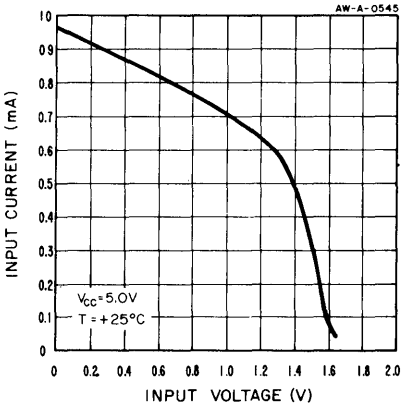
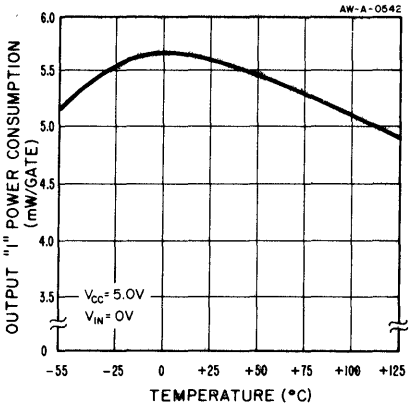
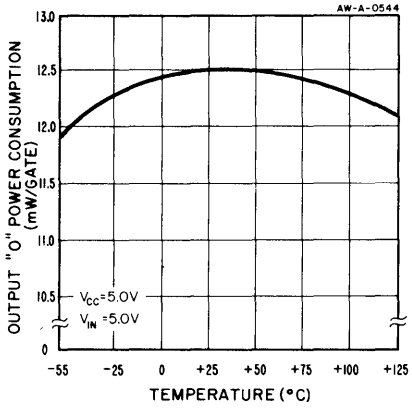








SIGNETICS DCL INTEGRATED CIRCUITS

8424 DUAL RS/T BINARY

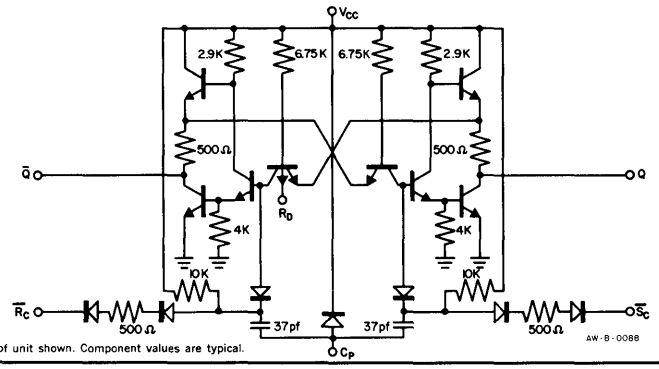
The 8424 is a low power, capacitively coupled Dual RS/T Binary.

This element responds to the trailing or negative-going transition of the clock pulse. The asynchronous RESET input, $\overline{R}_D$, may be activated independent of the state of the clock. The synchronous inputs ($\overline{R}_C$ and $\overline{S}_C$) are especially adaptable to NAND logic systems since they respond to low levels. The $\overline{R}_C$ and $\overline{S}_C$ inputs have no effect when the clock line is stationary.

Each logic element in the 8000 series is characterized to provide guarantees for driving the 8424. A convenient summary of these AC loading rules is provided in Table 1-5, Section 1.

Usage rules and applications information and suggestions are included in Section 4 of this handbook.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

TRUTH TABLE

$\overline{R}_{Cn}$	$\overline{S}_{Cn}$	Q_{n+1}
1	0	1
0	1	0
1	1	Q
0	0	?

$\overline{R}_D = 0 \Rightarrow Q = 0$

n is time prior to clock
n+1 is time following clock

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 15)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	TEST LIMITS				TEST CONDITIONS								
		MIN.	TYP.	MAX.	UNITS	TEMP. S8424	TEMP. N8424	V_{cc}	$\overline{R}_D$	CLOCK	$\overline{R}_C$	$\overline{S}_C$	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE (Q)	3.4			V	-55°C	0°C	4.75V	2.0V				-225µA	12, 8
A-3	(Q)	3.6			V	+25°C	+25°C	5.0V	2.0V				-225µA	12, 8
A-4	(Q)	3.4			V	+125°C	+75°C	4.75V	2.0V				-225µA	12, 8
A-5	"1" OUTPUT VOLTAGE ($\overline{Q}$)	3.4			V	-55°C	0°C	4.75V	0.7V				-225µA	8
A-3	($\overline{Q}$)	3.6			V	+25°C	+25°C	5.0V	0.7V				-225µA	8
A-4	($\overline{Q}$)	3.4			V	+125°C	+75°C	4.75V	0.7V				-225µA	8
A-5	"0" OUTPUT VOLTAGE (Q)			0.35	V	-55°C	0°C	4.75V	0.7V				7.2mA	9
A-3	(Q)			0.35	V	+25°C	+25°C	5.0V	0.7V				7.2mA	9
A-4	(Q)			0.35	V	+125°C	+75°C	4.75V	0.7V				7.2mA	9
A-5	"0" OUTPUT VOLTAGE ($\overline{Q}$)			0.35	V	-55°C	0°C	4.75V	2.0V				7.2mA	12, 9
A-3	($\overline{Q}$)			0.35	V	+25°C	+25°C	5.0V	2.0V				7.2mA	12, 9
A-4	($\overline{Q}$)			0.35	V	+125°C	+75°C	4.75V	2.0V				7.2mA	12, 9
C-1	"0" INPUT CURRENT ($\overline{R}_D$)	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V					13
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V					13
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V					13
C-1	"0" INPUT CURRENT ($\overline{R}_C$, $\overline{S}_C$)	-0.1		-0.6	mA	-55°C	0°C	5.25V			0.35V	0.35V		
A-3		-0.1		-0.6	mA	+25°C	+25°C	5.25V			0.35V	0.35V		
C-1		-0.1		-0.6	mA	+125°C	+75°C	5.25V			0.35V	0.35V		
A-4	"0" INPUT CURRENT (CLOCK)			25	µA	+125°C	+75°C	5.25V		0V				
A-4	"1" INPUT CURRENT ($\overline{R}_D$)			25	µA	+125°C	+75°C	4.75V	4.5V					14
A-4	"1" INPUT CURRENT ($\overline{R}_C$, $\overline{S}_C$)			25	µA	+125°C	+75°C	4.75V			4.5V	4.5V		
A-6	CLOCKED MODE HOLDING TEST (C)			10	ns	+25°C	+25°C	5.0V		PULSE				16
A-6	CLOCKED MODE SWITCHING TEST (C)			50	ns	+25°C	+25°C	5.0V		PULSE				16
A-6	(C)			75	ns	+25°C	+25°C	5.0V		PULSE				
A-6	CLOCKED MODE TURN-ON DELAY			60	ns	+25°C	+25°C	5.0V					D.C.F.O. = 9	10, 16
A-6	CLOCKED MODE TURN-OFF DELAY			60	ns	+25°C	+25°C	5.0V					D.C.F.O. = 9	10, 16
A-6	TOGGLE RATE	8			MHz	+25°C	+25°C	5.0V			$\overline{Q}$	Q		16
C-2	OUTPUT FALL TIME			75	ns	-55°C	0°C	4.75V					A.C.F.O. = 2	11, 16
C-2	INPUT CAPACITANCE (CLOCK)			50	pf	+25°C	+25°C	5.0V		2.0V				7
C-2	($\overline{R}_D$)			3.0	pf	+25°C	+25°C	5.0V	2.0V					7
C-2	($\overline{R}_C$, $\overline{S}_C$)			3.0	pf	+25°C	+25°C	5.0V			2.0V	2.0V		7
A-2	POWER CONSUMPTION (PER BINARY)			24.7	mW	+25°C	+25°C	5.25V			$\overline{Q}$	Q		
A-2	INPUT VOLTAGE RATING (CLOCK)	5.0		6.0	V	+25°C	+25°C	5.0V		10µA	0V	0V		
	($\overline{R}_D$)	5.5			V	+25°C	+25°C	5.0V	50µA					14
	($\overline{R}_C$, $\overline{S}_C$)	5.5			V	+25°C	+25°C	5.0V		0V	10µA	10µA		
A-2	OUTPUT SHORT CIRCUIT CURRENT ($\overline{Q}$)	-5.0		-12.0	mA	+25°C	+25°C	5.0V	0V				0V	

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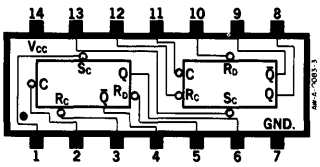

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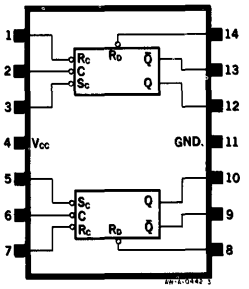
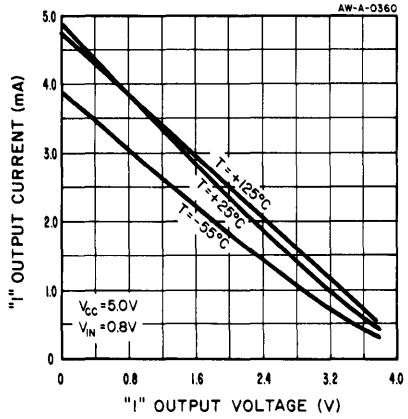
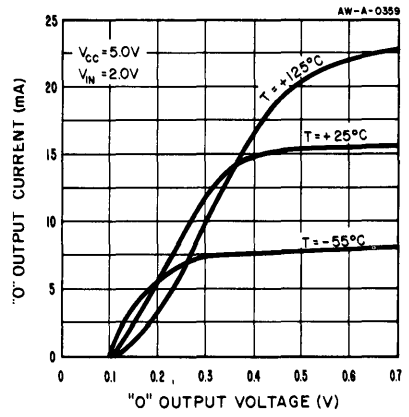


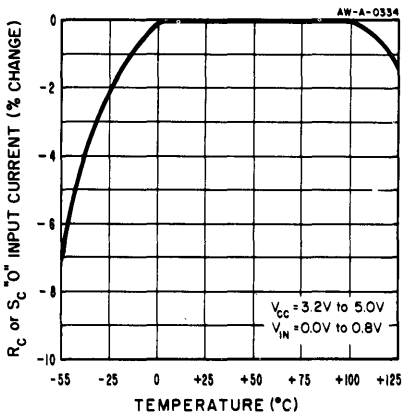
8424

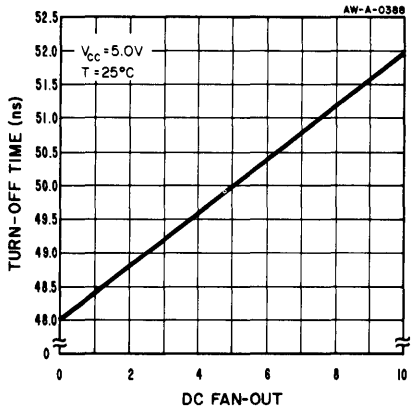
Notes:

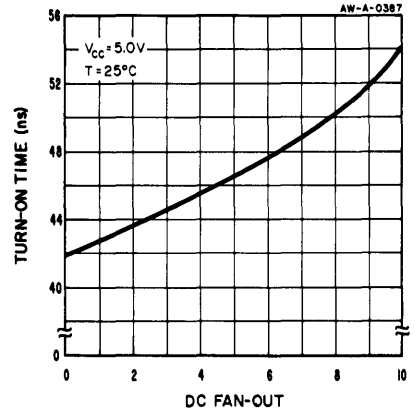
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. Momentarily apply zero volts to $\overline{Q}$ and V_{CC} to Q to ensure the state of the flip-flop prior to measurement.
13. Apply 0.5V to the Q output terminal.
14. Apply V_{CC} to $\overline{Q}$ output terminal and zero volts to Q output terminal.
15. Manufacturer reserves the right to make design and process changes and improvements.
16. Detailed test conditions for AC testing are in Section 3.

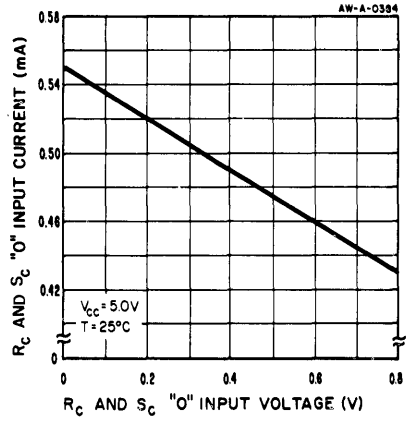


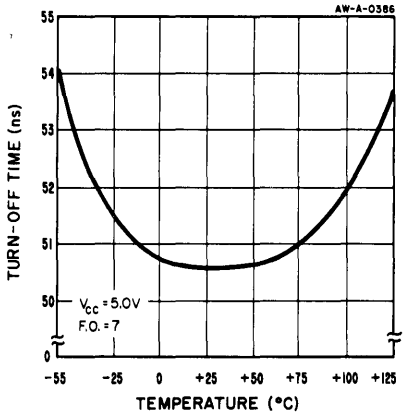


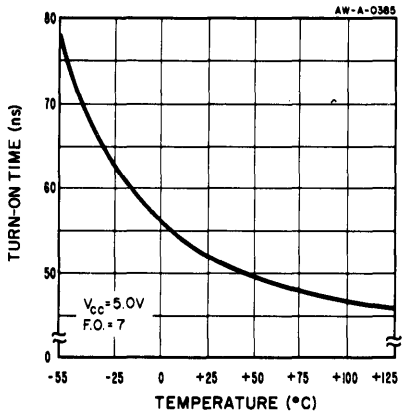












SIGNETICS DCL INTEGRATED CIRCUITS

8425 DUAL RS/T BINARY

The 8425 is a low-power, capacitively coupled Dual RS/T AC Binary.

This element responds to the trailing or negative-going transition of the clock pulse and features a common-clock, common RESET ($\overline{R}_D$) and separate SET ($\overline{S}_D$) which provide maximum usage of all inputs in synchronous systems such as shift registers and synchronous counters. The asynchronous RESET inputs, $\overline{R}_D/\overline{S}_D$, may be activated independent of the state of the clock, thus providing random access to synchronous systems. The synchronous inputs ($\overline{R}_C$ and $\overline{S}_C$) are especially adaptable to NAND logic systems since they respond to low levels. The $\overline{R}_C$ and $\overline{S}_C$ inputs have no effect when the clock line is stationary.

Each logic element in the 8000 series is characterized to provide guarantees for driving the 8425. A convenient summary of these AC loading rules is provided in Table 1-5, Section 1.

Usage rules and applications information are included in Section 4 of this handbook.

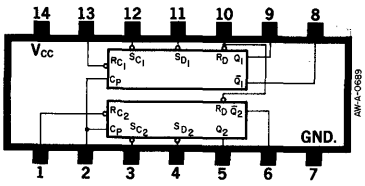
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 15)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS			TEST CONDITIONS									
		MIN.	MAX.	UNITS	TEMP. S8425	TEMP. N8425	V_{CC}	$\overline{S}_D$	$\overline{R}_D$	CLOCK	$\overline{R}_C$	$\overline{S}_C$	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE ($\overline{Q}$)	3.4		V	-55°C	0°C	4.75V	0.7V	2.0V				-225μA	8
A-3	($\overline{Q}$)	3.6		V	+25°C	+25°C	5.0V	0.7V	2.0V				-225μA	8
A-4	($\overline{Q}$)	3.4		V	+125°C	+75°C	4.75V	0.7V	2.0V				-225μA	8
A-5	"1" OUTPUT VOLTAGE (Q)	3.4		V	-55°C	0°C	4.75V	2.0V	0.7V				-225μA	8
A-3	(Q)	3.6		V	+25°C	+25°C	5.0V	2.0V	0.7V				-225μA	8
A-4	(Q)	3.4		V	+125°C	+75°C	4.75V	2.0V	0.7V				-225μA	8
A-5	"0" OUTPUT VOLTAGE (Q)		0.35	V	-55°C	0°C	4.75V	2.0V	0.7V				7.2mA	9
A-3	(Q)		0.35	V	+25°C	+25°C	5.0V	2.0V	0.7V				7.2mA	9
A-4	(Q)		0.35	V	+125°C	+75°C	4.75V	2.0V	0.7V				7.2mA	9
A-5	"0" OUTPUT VOLTAGE ($\overline{Q}$)		0.35	V	-55°C	0°C	4.75V	0.7V	2.0V				7.2mA	9
A-3	($\overline{Q}$)		0.35	V	+25°C	+25°C	5.0V	0.7V	2.0V				7.2mA	9
A-4	($\overline{Q}$)		0.35	V	+125°C	+75°C	4.75V	0.7V	2.0V				7.2mA	9
C-1	"0" INPUT CURRENT ($\overline{R}_D$)	-0.1	-1.6	mA	-55°C	0°C	5.25V		0.35V					12
A-3	($\overline{R}_D$)	-0.1	-1.6	mA	+25°C	+25°C	5.25V		0.35V					12
C-1	($\overline{R}_D$)	-0.1	-1.6	mA	+125°C	+75°C	5.25V		0.35V					12
C-1	"0" INPUT CURRENT ($\overline{S}_D$)	-0.1	-0.8	mA	-55°C	0°C	5.25V	0.35V						12
A-3	($\overline{S}_D$)	-0.1	-0.8	mA	+25°C	+25°C	5.25V	0.35V						12
C-1	($\overline{S}_D$)	-0.1	-0.8	mA	+125°C	+75°C	5.25	0.35V						12
C-1	"0" INPUT CURRENT ($\overline{R}_C$, $\overline{S}_C$)	-0.1	-0.6	mA	-55°C	0°C	5.25V				0.35V	0.35V		
A-3	($\overline{R}_C$, $\overline{S}_C$)	-0.1	-0.6	mA	+25°C	+25°C	5.25V				0.35V	0.35V		
C-1	($\overline{R}_C$, $\overline{S}_C$)	-0.1	-0.6	mA	+125°C	+75°C	5.25V				0.35V	0.35V		
A-4	"0" INPUT CURRENT (CLOCK)		-50	μA	+125°C	+75°C	5.25V			0V				
A-4	"1" INPUT CURRENT ($\overline{S}_D$)		25	μA	+125°C	+75°C	4.75V	4.5V						13
A-3	($\overline{S}_D$)		25	μA	+25°C	+25°C	4.75V	4.5V						13
A-4	($\overline{R}_D$)		50	μA	+125°C	+75°C	4.75V		4.5V					13
A-3	($\overline{R}_D$)		50	μA	+25°C	+25°C	4.75V		4.5V					13
A-6	CLOCKED MODE HOLDING TEST		10	ns	+25°C	+25°C	5.0V			PULSE				15
A-6	CLOCKED MODE SWITCHING TEST		50	ns	+25°C	+25°C	5.0V			PULSE				15
A-6			75	ns	+25°C	+25°C	5.0V			PULSE				15
A-6	CLOCKED MODE TURN-ON DELAY		60	ns	+25°C	+25°C	5.0V						D.C.F.O. = 9	10, 15
A-6	CLOCKED MODE TURN-OFF DELAY		60	ns	+25°C	+25°C	5.0V						D.C.F.O. = 9	10, 15
A-6	TOGGLE RATE	8		MHz	+25°C	+25°C	5.0V				$\overline{Q}$	Q		15
C-2	OUTPUT FALL TIME		75	ns	-55°C	0°C	4.75V						A.C.F.O. = 2	11, 15
C-2	INPUT CAPACITANCE (CLOCK)		100	pf	+25°C	+25°C	5.0V			2.0V				7
C-2	($\overline{S}_D$)		3.0	pf	+25°C	+25°C	5.0V	2.0V						7
C-2	($\overline{R}_D$)		6.0	pf	+25°C	+25°C	5.0V		2.0V					7
C-2	($\overline{R}_C$, $\overline{S}_C$)		3.0	pf	+25°C	+25°C	5.0V				2.0V	2.0V		7
A-2	POWER CONSUMPTION (Per Binary)		24.7	mW	+25°C	+25°C	5.25V				$\overline{Q}$	Q		
A-2	INPUT VOLTAGE RATING (CLOCK)	5.0	6.0	V	+25°C	+25°C	5.0V			10μA	0V	0V		
A-2	($\overline{S}_D$, $\overline{R}_D$)	5.5		V	+25°C	+25°C	5.0V	50μA	50μA					13
A-2	($\overline{R}_C$, $\overline{S}_C$)	5.5		V	+25°C	+25°C	5.0V			0V	10μA	10μA		
A-2	OUTPUT SHORT CIRCUIT CURRENT ($\overline{Q}$)	-5.0	-12	mA	+25°C	+25°C	5.0V		0V				0V	
A-2	(Q)	-5.0	-12	mA	+25°C	+25°C	5.0V	0V					0V	

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV rms. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. Apply 0.5V to the Q output terminal for $\overline{R}_D$ test and 0.5V to $\overline{Q}$ for $\overline{S}_D$ test.
13. Apply V_{CC} to $\overline{Q}$ output terminal and zero volts to Q output terminal for $\overline{R}_D$ test and V_{CC} to Q and zero volts to $\overline{Q}$ for $\overline{S}_D$ test.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.

A PACKAGE



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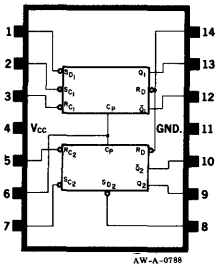
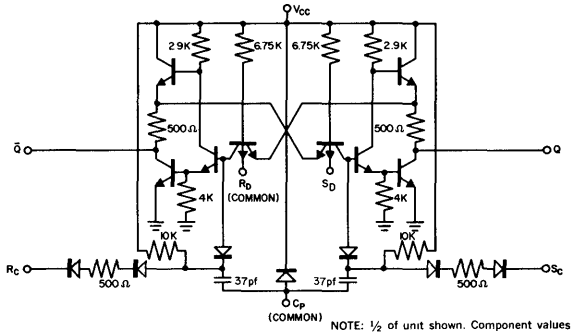


8425

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

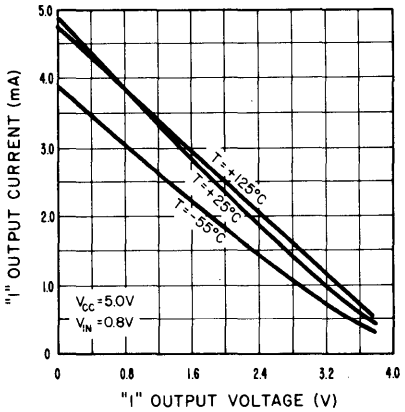
TRUTH TABLE

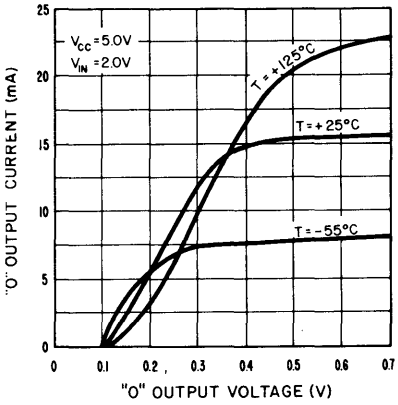
$\overline{R}_{C_n}$	$\overline{S}_{C_n}$	Q_{n+1}
1	0	1
0	1	0
1	1	Q
0	0	?

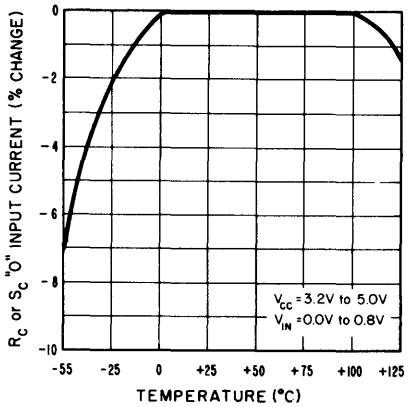
n is time prior to clock

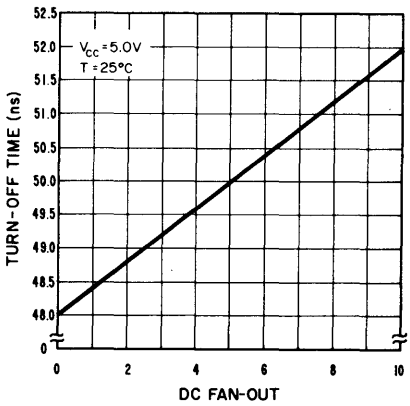
$\overline{R}_D$	$\overline{S}_D$	Q
1	0	1
0	1	0
1	1	Q
0	0	*

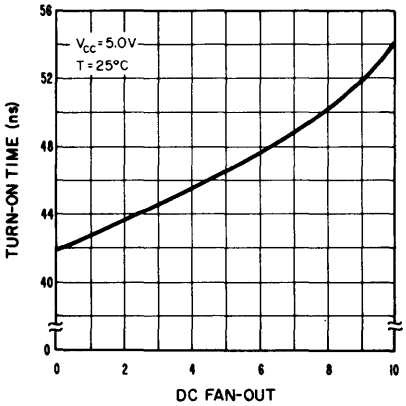
*Both outputs go to "1" state until R_D or S_D rises.

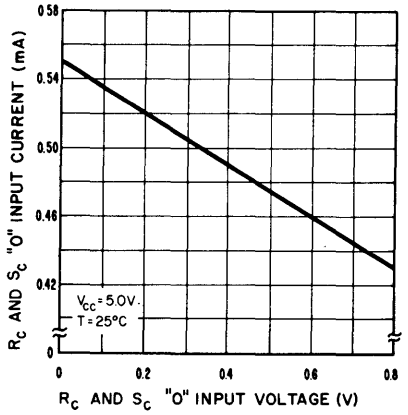


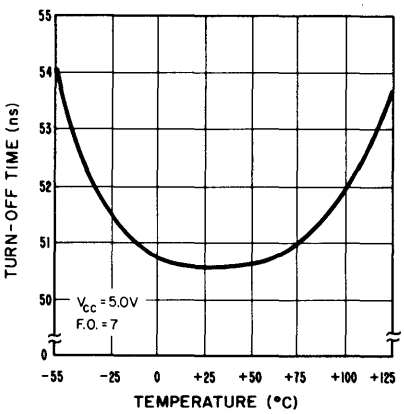


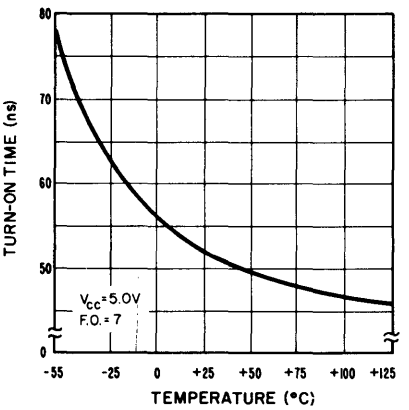












SIGNETICS DCL INTEGRATED CIRCUITS

8440 DUAL AND-OR-INVERT GATE

The 8440 Dual AND-OR-INVERT Gate implements the Exclusive-OR function.

The active output structure of the 8440 provides high AC noise immunity due to its low output impedance in both the "1" and "0" output states.

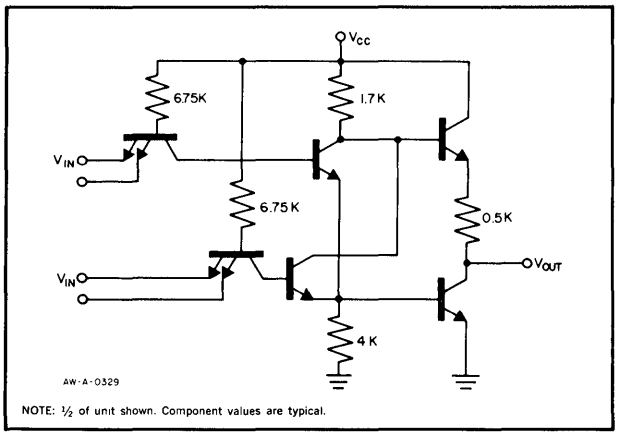
Output short circuit protection is provided by a current limiting resistor.

Values chosen for the collector and emitter resistors of the phase-splitter transistor ensure optimum on-off relationships of the totem-pole output pair.

General areas of application for the 8440 include half and full adders, digital comparators, and AND-OR control logic for inputs to binary clock steering lines.

Section 4 of this handbook contains helpful applications information and usage rules for the 8440.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 14)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8440	TEMP. N8440	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OURPUT VOLTAGE	3.4			V	-55°C	0°C	4.75V	0.7V		-225μA	8
A-3		3.6			V	+25°C	+25°C	5.0V	0.7V		-225μA	8
A-4		3.4			V	+125°C	+75°C	4.75V	0.7V		-225μA	8
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	9, 12
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	9, 12
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	9, 12
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	30		95	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 15
C-2	OUTPUT FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 2	11, 15
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 15
C-2	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.0V			D.C.F.O. = 1	10, 15
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			29.4	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			9.5	mW	+25°C	+25°C	5.25V	0V			13
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-4.0		-12	mA	+25°C	+25°C	5.0V	0V		0V	

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground. Apply 0.7V to one input terminal of associated AND gate.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. To test "0" output voltage, apply 2.0V to the input terminal of one input AND gate and apply zero volts to the input terminals of the associated input AND gate. Reverse input conditions and measure again.
13. For output "1" power consumption test, apply zero volts to one input terminal of associated input AND gates.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.

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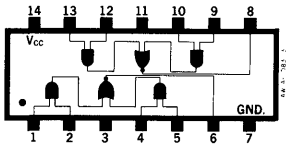

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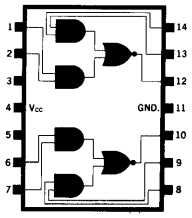
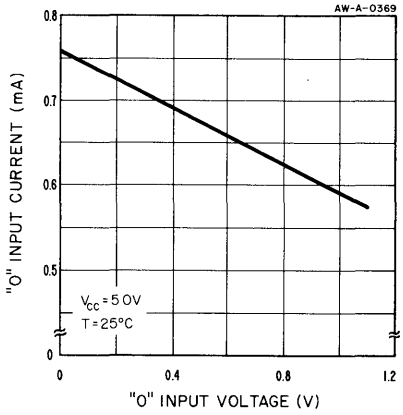
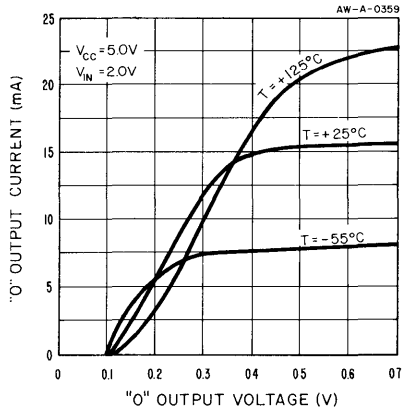
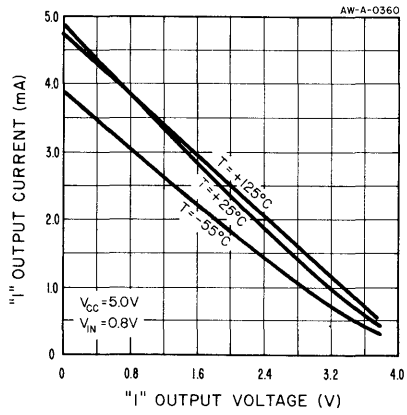
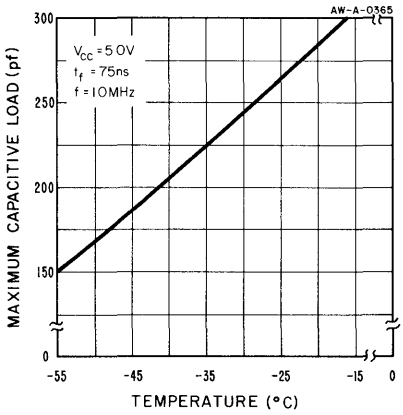










SIGNETICS DCL INTEGRATED CIRCUITS

8455 DUAL 4-INPUT NAND GATE DRIVER

The 8455 Dual 4-Input TTL NAND Gate Driver is used in high fan-out applications involving either AC or DC loads. The device implements the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

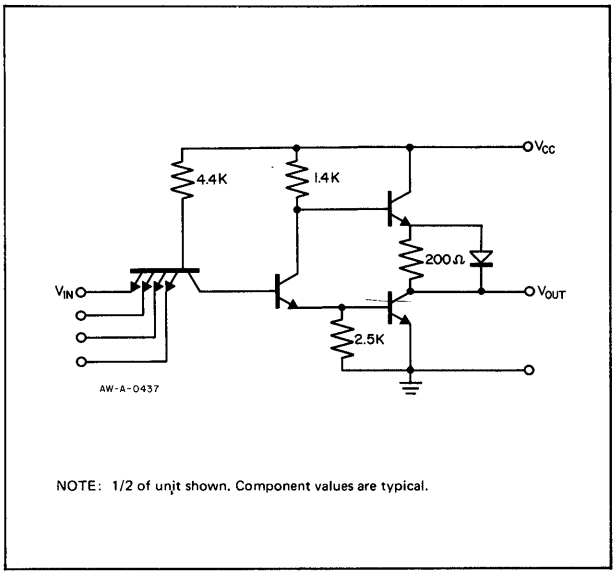
This element utilizes an active output structure which provides high AC noise immunity due to its low output impedance in both the "1" and "0" output states.

The current limiting resistor between the active pull-up and the output terminal features a parallel diode which displays extremely low impedance in the output "1" state. The design ensures optimum rise time when driving high capacitance loads encountered in high fan-out situations, and when driving AC binaries or long lines.

The values chosen for the collector and emitter resistors of the second stage transistor provide an optimum on-off relationship of the totem-pole output pair to minimize transient current spikes.

Section 4 of this handbook contains helpful usage rules and applications for the 8455.

BASIC CIRCUIT SCHEMATIC



NOTE: 1/2 of unit shown. Component values are typical.

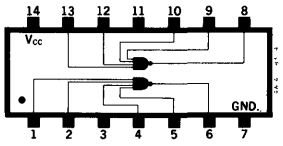
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8455	TEMP. N8455	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	3.4			V	-55°C	0°C	4.75V	0.7V		-625μA	8
A-3		3.6			V	+25°C	+25°C	5.0V	0.7V		-625μA	8
A-4		3.4			V	+125°C	+75°C	4.75V	0.7V		-625μA	8
A-5	"0" OUTPUT VOLTAGE			0.35V	V	-55°C	0°C	4.75V	2.0V	2.0V	20mA	9
A-3				0.35V	V	+25°C	+25°C	5.0V	2.0V	2.0V	20mA	9
A-4				0.35V	V	+125°C	+75°C	4.75V	2.0V	2.0V	20mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.2	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-1.2	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-1.2	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	30		95	ns	+25°C	+25°C	5.0V			D.C.F.O. = 25	10, 13
C-2	FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 9	11, 13
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 25	10, 13
C-2	TURN-OFF DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 1	10, 13
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			28.4	mW	+25°C	+25°C	5.25V				
A-2	(Per Gate) OUTPUT "1"			7.3	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-20		-95	mA	+25°C	+25°C	5.0V	0V		0V	

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.

A PACKAGE



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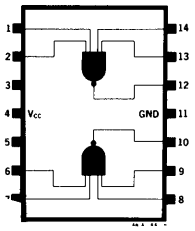
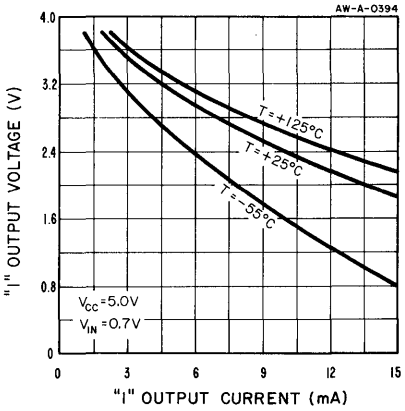
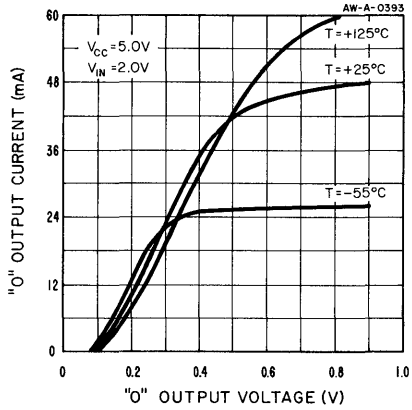
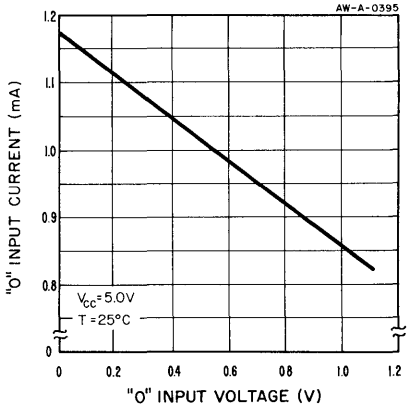
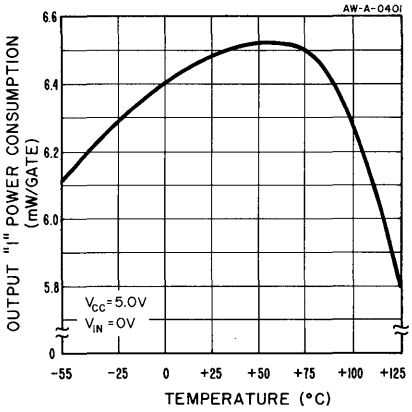


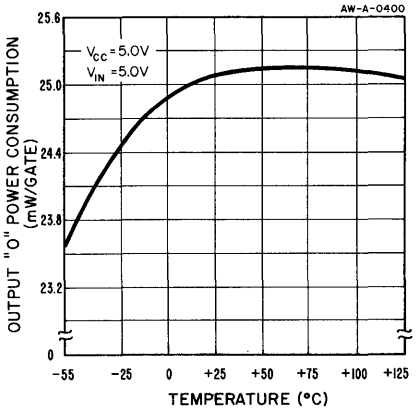
8455

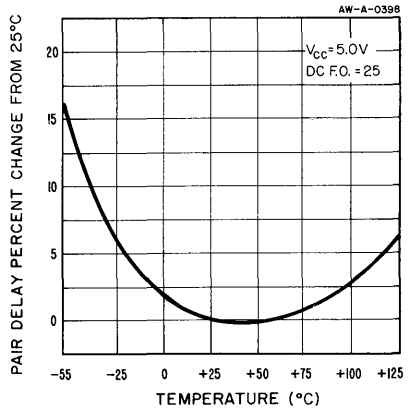


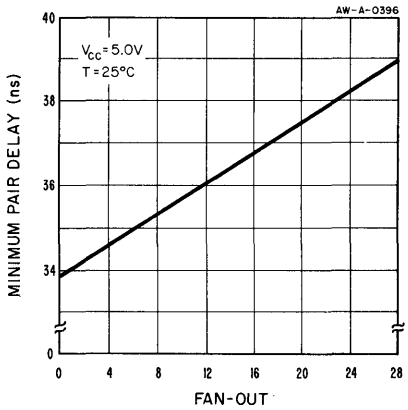


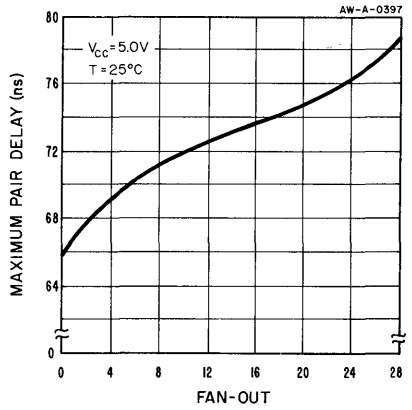


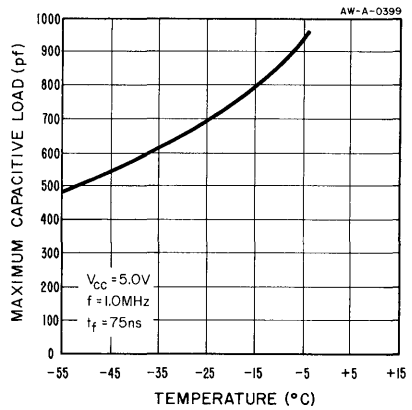












SIGNETICS

DCL

INTEGRATED CIRCUITS

8470 TRIPLE 3-INPUT NAND GATE
8480 QUAD 2-INPUT NAND GATE
8490 HEX INVERTER

The 8470 Triple 3-Input NAND Gate and the 8480 Quad 2-Input NAND Gate implement the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

The 8490 Hex Inverter is an addition to the 8470/8480 group of NAND gates.

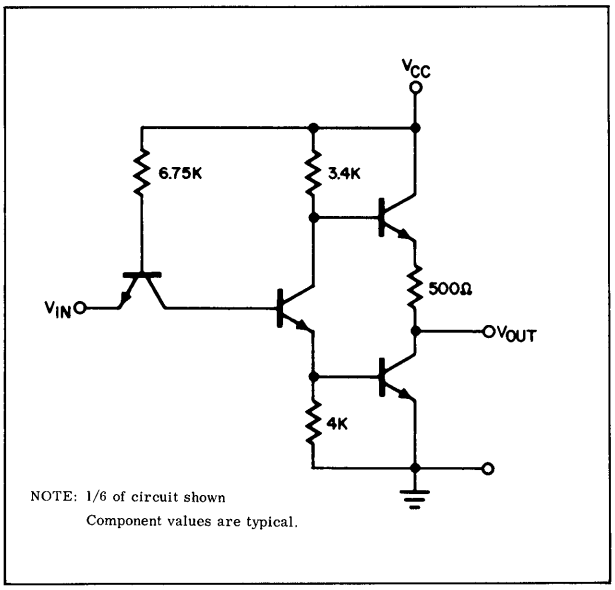
The active output structure of these elements provides high AC noise immunity due to its low output impedance in both the "1" and "0" output states. This output configuration is particularly suited for driving high capacitive loads such as those encountered in high fan-out situations and line driving applications.

Output short circuit protection is provided by a current limiting resistor.

The values chosen for the collector and emitter resistors of the phase-splitter transistor ensure optimum on-off relationships of the totem-pole output pair.

Section 4 of this handbook contains helpful usage rules and applications for the 8470 and 8480.

BASIC CIRCUIT SCHEMATIC



NOTE: 1/6 of circuit shown
Component values are typical.

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12)

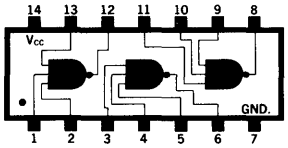
ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8470 S8480	TEMP. N8470 N8480	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	3.4			V	-55°C	0°C	4.75V	0.7V		-225μA	8
A-3		3.6			V	+25°C	+25°C	5.0V	0.7V		-225μA	8
A-4		3.4			V	+125°C	+75°C	4.75V	0.7V		-225μA	8
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	9
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	9
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	9
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	25		95	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 13
C-2	OUTPUT FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 2	11, 13
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 13
C-2	TURN-OFF DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 1	10, 13
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			16.8	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			5.2	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-4.0		-12.0	mA	+25°C	+25°C	5.0V	0V		0V	

NOTES:

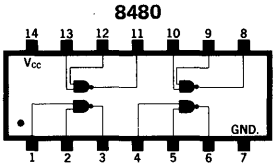
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV$_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.

A PACKAGE

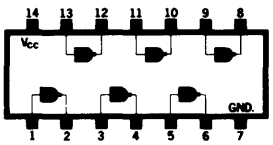
8470



8480



8490



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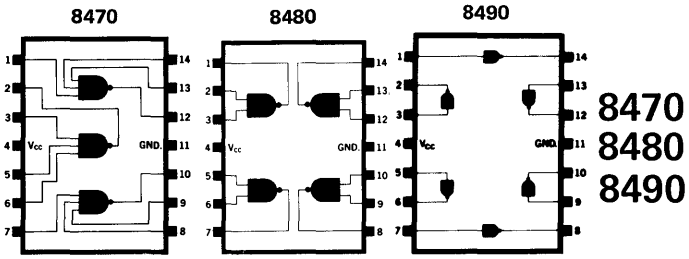
8470 8480 8490



8470
8480
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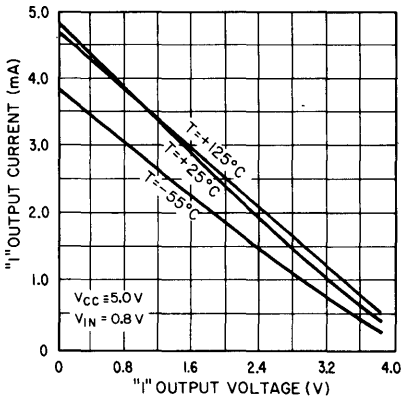

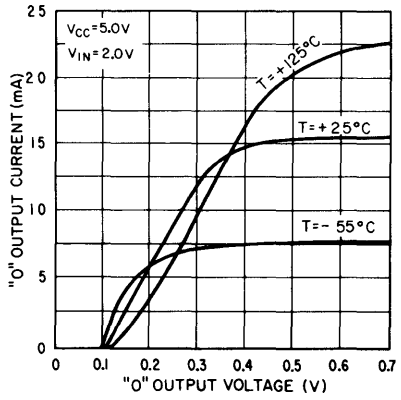

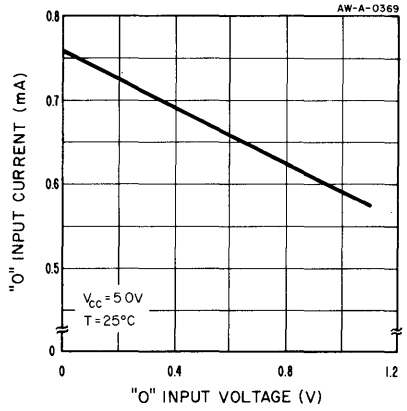

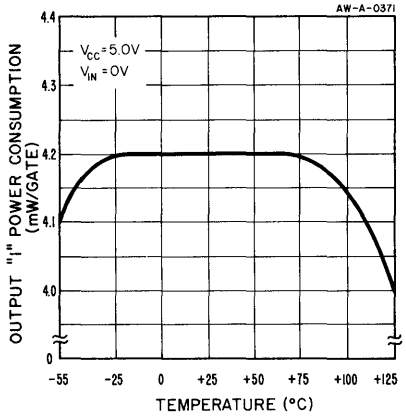

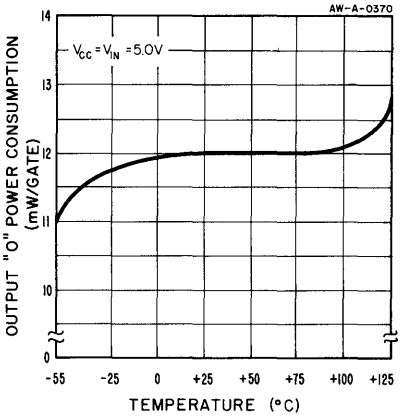

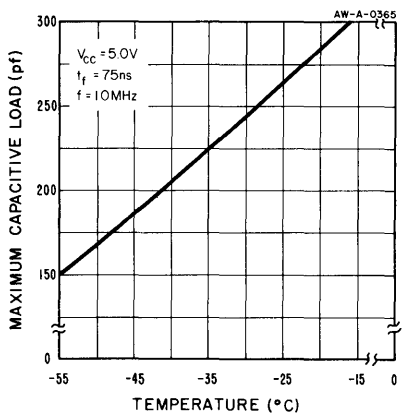

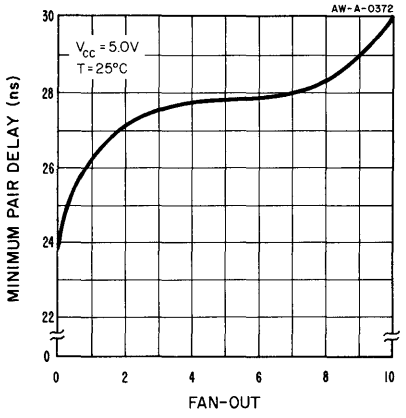

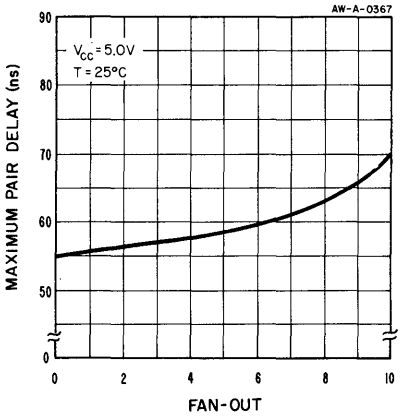

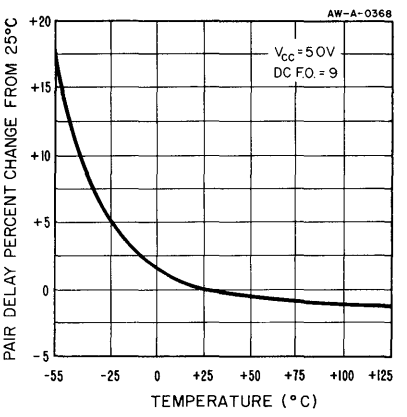

SIGNETICS

DCL

INTEGRATED CIRCUITS

8471
TRIPLE 3-INPUT NAND GATE

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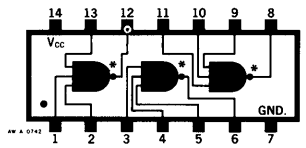

*NO PULL-UP PROVIDED

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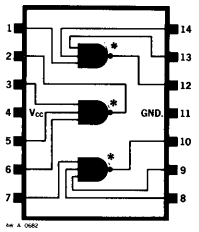
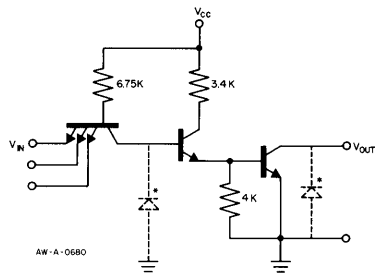


The 8471 is a Triple 3-Input NAND Gate with bare output collectors. Absence of an output pull-up structure allows the user complete freedom in the use of the 8471 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 30 outputs to be tied together.

Collector-logic, using the 8471, can provide increased system flexibility and lower system cost due to reduced can count.

Section 4 of this handbook contains detailed usage rules and collector-logic information for this element.

BASIC CIRCUIT SCHEMATIC



NOTE: 1/3 of unit shown. Component values are typical.

*Isolation diode

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8471	TEMP. N8471	Vcc	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			25	μA	+125°C	+75°C	5.0V	0.6V			11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	8.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	8.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	8.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	50		150	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	9, 13
C-2	FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 2	10, 13
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	9, 13
C-2	TURN-OFF DELAY			50	ns	++25°C	+25°C	5.0V			D.C.F.O.= 1	9, 13
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			16.8	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			5.2	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0"
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Connect an external 1K ±1% resistor from V_{cc} to the output terminal for this test.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.

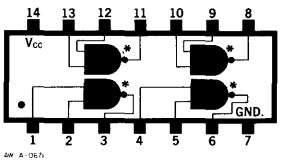
SIGNETICS

DCL

INTEGRATED CIRCUITS

8481 QUAD 2-INPUT NAND GATE

A PACKAGE



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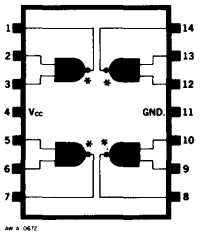


*No pull-up provided

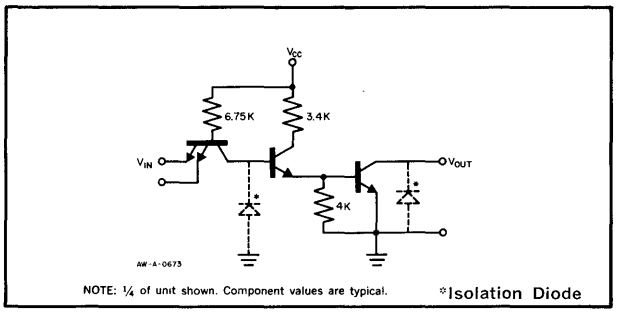
8481

The 8481 is a Quad 2-Input NAND Gate with bare output collectors. Absence of an output pull-up structure allows the user complete freedom in the use of the 8481 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 30 outputs to be tied together.

Collector logic, using the 8481, can provide increased system flexibility and lower system cost due to reduced can count.

Section 4 of this handbook provides detailed usage rules and collector-logic information for this element.

BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (NOTES: 1,2,3,4,5,6,12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8481	TEMP. N8481	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			25	μA	+125°C	+75°C	5.0V	0.6V			11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	8.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	8.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	8.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	50		150	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9,13
C-2	FALL TIME			75	ns	-55°C	0°C	4.75V			A.C. F.O. = 2	10,13
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9,13
C-2	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.0V			D.C. F.O. = 1	9,13
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			16.8	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			5.2	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Connect an external 1K resistor from V_{cc} to the output terminal for this test.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.

SIGNETICS DCL INTEGRATED CIRCUITS

8706 DUAL 5–INPUT DIODE EXPANDER ELEMENT

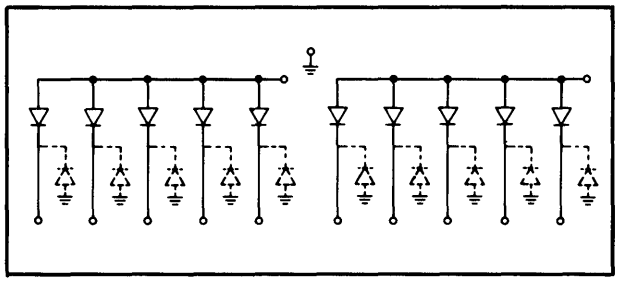
8731 QUAD 2–INPUT DIODE EXPANDER ELEMENT

The 8706 Dual 5-Input and the 8731 Quad 2-Input Diode Expander Elements complete the full range of diode input expansion capacility for the 8400 series expandable gate (8415, 8416 and 8417).

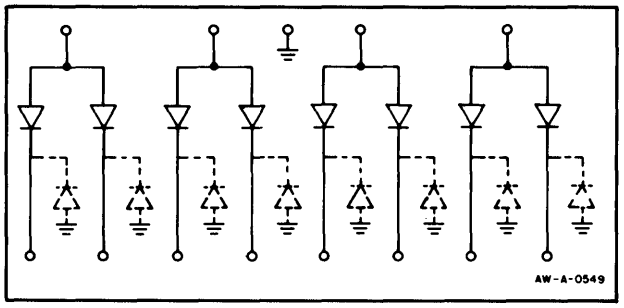
The 8706 and the 8731 provide optimum flexibility for the most efficient utilization of pin and package configurations in achieving a desired number of additional input term and input combinations.

Applications information on the 8706 and 8731 is included in Section 4 of this handbook.

BASIC CIRCUIT SCHEMATIC 8706



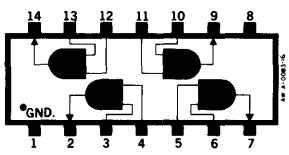
BASIC CIRCUIT SCHEMATIC 8731



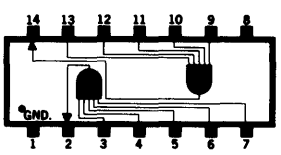
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 9)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS			TEST CONDITIONS					
		MIN.	MAX.	UNITS	TEMP. S8731	TEMP. N8731	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" INPUT CURRENT		25	μA	+125°C	+75°C	4.5V	0V	0V	
C-1	DIODE FORWARD VOLTAGE		0.95	V	-55°C	0°C	0V	Open	1.2mA	
A-3			0.85	V	+25°C	+25°C	0V	Open	1.2mA	
C-1			0.68	V	+125°C	+75°C	0V	Open	1.2mA	
A-2	INPUT VOLTAGE RATING	6.5		V	+25°C	+25°C	10μA	Open	0V	
C-2	INPUT CAPACITANCE		3	pf	+25°C	+25°C	2.0V		0V	7
C-2	DIODE RECOVERY TIME		4	ns	+25°C	+25°C	±2mA	Open		8

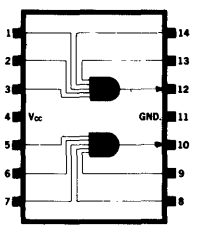
8731A



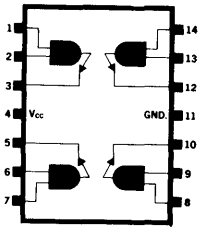
8706A



8706J



8731J



Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.
6. Measurements apply to each diode cluster independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1Mc, V = 25mV$_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Recovery to 0.2mA, Loop Resistance = 100 ohms. Measure with Tektronix Type 291 Diode Switching Time Tester.
9. Manufacturer reserves the right to make design and process changes and improvements.

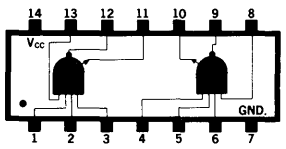
SIGNETICS

DCL

INTEGRATED CIRCUITS

8806 DUAL 4-INPUT EXPANDER ELEMENT

A PACKAGE



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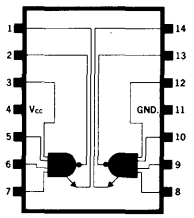
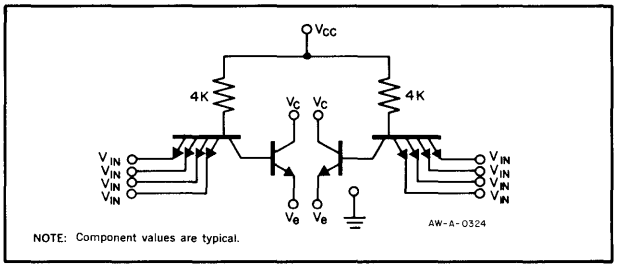


The 8806 Dual 4-Input Expander Element is compatibly designed and characterized for use with the 8840 and 8848 AND-OR-INVERT Gates, thereby providing increased system usefulness for the 8840 and the 8848.

Applications information on the 8806 is included in Section 4 of this handbook.

BASIC CIRCUIT SCHEMATIC



NOTE: Component values are typical.

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS							NOTES
		MIN.	TYP.	MAX.	UNITS	TEMP. S8806	TEMP. N8806	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS V_C	OUTPUTS V_E	
A-3	OUTPUT "ON" VOLTAGE AT V_C (1, 2)*			1.25	V	+25°C	+25°C	4.75V	2.0V	2.0V	7.2mA	0.85V	9
A-3	OUTPUT "ON" CURRENT AT V_E (2, 3)*	-2.5			mA	+25°C	+25°C	4.75V	2.0V	2.0V	2.2mA	0.85V	8, 9
A-3	OUTPUT "OFF" CURRENT AT V_E(4, 5)*			-50	μA	+25°C	+25°C	5.25V	0.8V		4.75V	0.59V	9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.40V	5.25V			
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.40V	5.25V			
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.40V	5.25V			
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V			
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V				7
A-2	POWER CONSUMPTION OUTPUT "ON"			6.3	mW	+25°C	+25°C	5.25V				0.59V	
A-2	(Per Expander) OUTPUT "OFF"			8.9	mW	+25°C	+25°C	5.25V	0V				
C-1	INPUT LATCH VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	10mA	0V			10
A-6	TURN-ON DELAY			20	ns	+25°C	+25°C	5.0V					13
A-6	TURN-OFF DELAY			34	ns	+25°C	+25°C	5.0V					13

*8840 Node Test Correlation Note 11

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output current is supplied through a resistor to ground.
9. Output current is supplied through a resistor to V_{cc}. For output "OFF" current at V_C use 2.5K ±1% resistor.
10. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
11. Compatibility between the 8806, the 8840 and 8848 are proved by this series of tests for corresponding tests performed on the 8840 and 8848. Check those tests enclosed in special box on 8840 and 8848 data tables.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.

SIGNETICS

DCL

INTEGRATED CIRCUITS

8808 SINGLE 8-INPUT NAND GATE
8816 DUAL 4-INPUT NAND GATE
8870 TRIPLE 3-INPUT NAND GATE
8880 QUAD 2-INPUT NAND GATE

These NAND gates provide high switching speed while maintaining high fan-out and noise margin. They perform the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

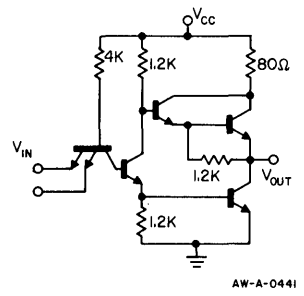
The output structure utilizes a totem-pole arrangement which employs a Darlington Pair for active pull-up. This configuration provides extremely low output impedance for the "1" output state. As a result, switching times are relatively insensitive to capacitive loads when compared to single transistor active pull-ups. The saturating output switching transistor provides a low impedance driving source in the output "0" state, enhancing turn-on times and providing high fan-out capability.

Because of the low output impedance of these gates, they exhibit high AC noise immunity at the output which is extremely important in high speed systems in eliminating erroneous cross-coupled signals.

Output short-circuit protection is provided by a current limiting resistor.

Section 4 of this handbook provides usage rules and application information for these gates.

BASIC CIRCUIT SCHEMATIC



NOTE: Component values are typical.

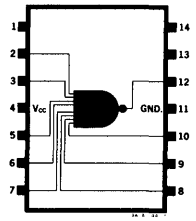
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8800	TEMP. N8800	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V		-500μA	8
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V		-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V		-500μA	8
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V	2.0V	16mA	9
A-3				0.40	V	+25°C	+25°C	5.0V	2.0V	2.0V	16mA	9
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V	2.0V	16mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.40V	5.25V		
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.40V	5.25V		
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.40V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	TURN-ON DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O.=20	10, 14
A-6	TURN-OFF DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O. = 20	10, 14
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C. F.O. = 6	11, 14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION "0"			31	mW	+25°C	+25°C	5.25V				
	(Per Gate) "1"			8.9	mW	+25°C	+25°C	5.25V	0V			
C-1	INPUT LATCH VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	10mA	0V		12
A-2	OUTPUT SHORT CIRCUIT CURRENT	-20		-70	mA	+25°C	+25°C	5.0V	0V		0V	

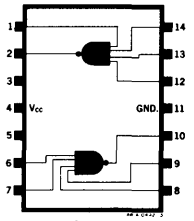
Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to Vcc.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.

J PACKAGES



8808



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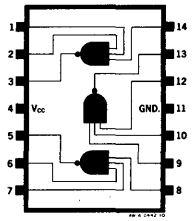

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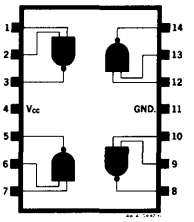

8880

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8816
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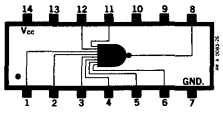

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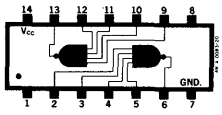

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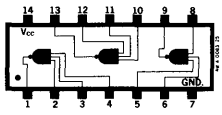

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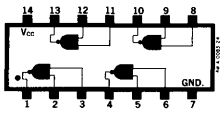

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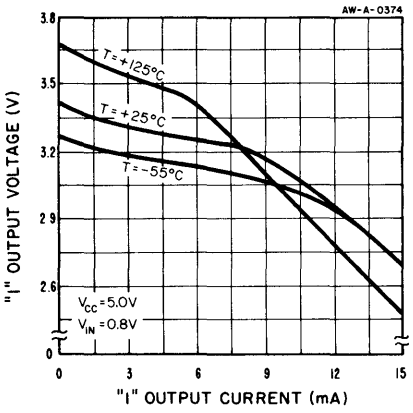
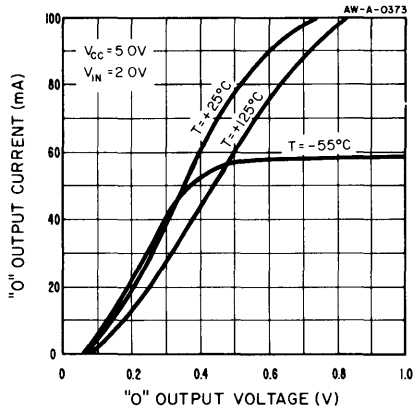
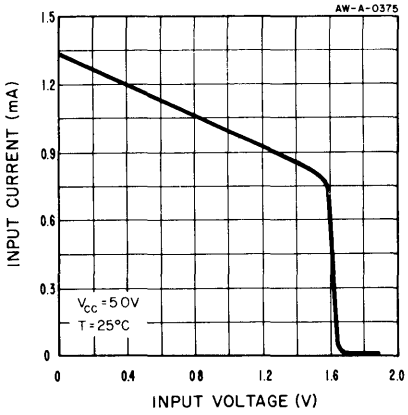






SIGNETICS

DCL

INTEGRATED CIRCUITS

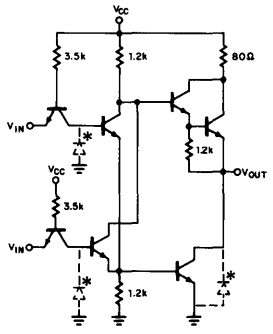
8815 DUAL 4-INPUT NOR GATE
8875 TRIPLE 3-INPUT NOR GATE
8885 QUAD 2-INPUT NOR GATE

The 8815, 8875 and 8885 gates perform the logic NOR function for positive logic (the logic "ONE" is assigned to the highest voltage level) and complement the NAND gate elements 8816, 8870 and 8880.

These gates are all designed for high speed application while maintaining high fan-out and noise margin.

The parallel transistor structure forms the NOR function. All unused inputs must be tied to ground. The output arrangement is basically the same as the NAND implementation providing low impedance for both logic levels.

BASIC CIRCUIT SCHEMATIC



NOTE: COMPONENT VALUES ARE TYPICAL.
* ISOLATION DIODE

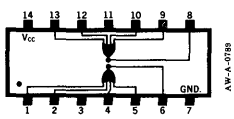
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

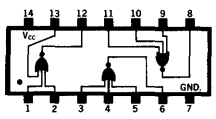
ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8815 S8875 S8885	TEMP. N8815 N8875 N8885	V_{CC}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V	0.8V	-500μA	8
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V	0.8V	-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V	0.8V	-500μA	8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V	0V	16mA	9
A-3				0.4	V	+25°C	+25°C	5.0V	2.0V	0V	16mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	0V	16mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.4V			
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.4V			
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.4V			
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V			
A-6	TURN-ON DELAY		8.0	13	ns	+25°C	+25°C	5.0V			D.C.F.O. = 20	10,14
A-6	TURN-OFF DELAY		10	13	ns	+25°C	+25°C	5.0V			D.C.F.O. = 20	10,14
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C.F.O. = 6	11,14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION (Per Gate)											
	8815 "1"			35.6	mW	+25°C	+25°C	5.25V	0V	0V		
	8875 "1"			27.1	mW	+25°C	+25°C	5.25V	0V	0V		
	8885 "1"			17.8	mW	+25°C	+25°C	5.25V	0V	0V		
	8815 "0"			49.7	mW	+25°C	+25°C	5.25V				
	8875 "0"			43.7	mW	+25°C	+25°C	5.25V				
	8885 "0"			37.3	mW	+25°C	+25°C	5.25V				
C-1	INPUT LATCH VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	10mA			12
A-2	OUTPUT SHORT CIRCUIT CURRENT	-20		-70	mA	+25°C	+25°C	5.0V	0V	0V	0V	

NOTES:

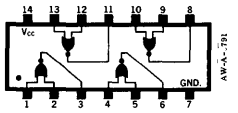
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.

8815A A PACKAGE 8875A



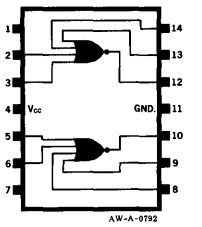


8885A

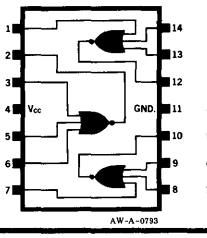


J PACKAGES

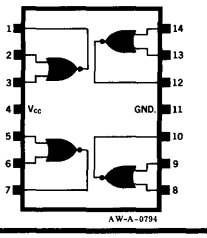
8815J



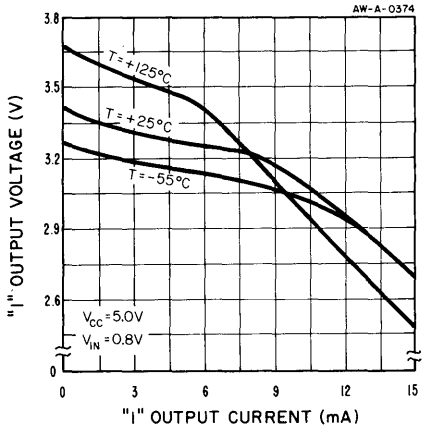
8875J

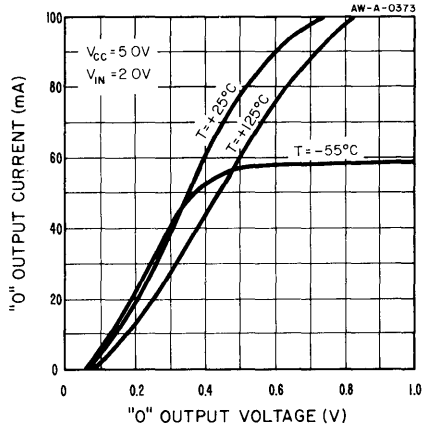


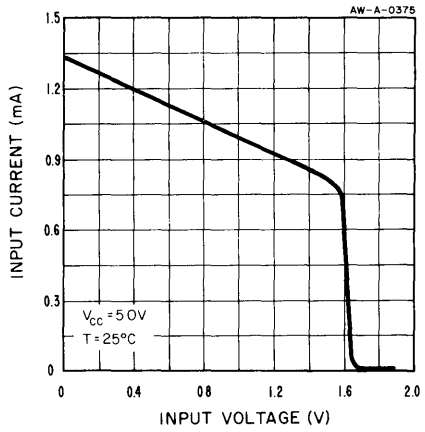
8885J



8815
8875
8885







SIGNETICS DCL INTEGRATED CIRCUITS

PRELIMINARY SPECIFICATIONS

8821 DUAL MASTER-SLAVE J-K BINARY
8822 DUAL MASTER-SLAVE J-K BINARY
8824 DUAL MASTER-SLAVE J-K BINARY

The 8821, 8822 and 8824 Dual Master-Slave J-K Binaries provide pin configuration and logic input variations of the same basic device to obtain maximum board layout convenience and design flexibility.

The 8821, available in the J package only, provides common clock and $\overline{R}_D$ inputs and separate $\overline{S}_D$ inputs. This configuration is especially useful in synchronous counter and shift register applications. Where a dual in-line package is required, the 8824 is recommended.

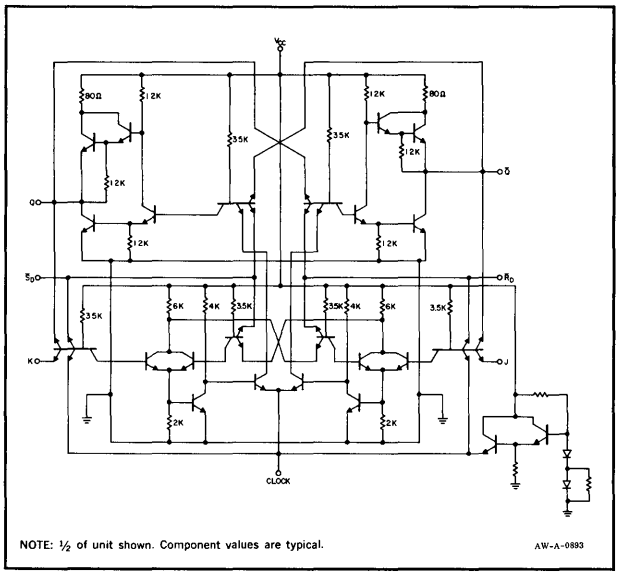
The 8822 provides separate clock and separate $\overline{R}_D$ inputs and is in the dual in-line (A) package and has V_{CC} at pin 14 and ground at pin 7 for consistency with other dual in-line pin configurations. This pin configuration can significantly simplify board layout. The 8822 is also available in the J package.

The 8824 is available in the 16 pin dual in-line (B) package. This unit provides two separate binaries with full synchronous and asynchronous access. The 8824 provides V_{CC} and ground pin orientation which is consistent with other dual in-line devices and thus simplifies board layout.

Triggering is accomplished on the negative transition (falling edge) of the clock pulse. Set up time must be greater than or equal to the clock pulse width. There is no hold time requirement for the inputs. Set up time is defined as the time prior to a negative transition of the clock line.

For optimum reliability, all three devices are fabricated from a single monolithic die.

BASIC CIRCUIT SCHEMATIC



TRUTH TABLES

8821 AND 8824

J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

$\overline{S}_D$	$\overline{R}_D$	Q
0	0	†
1	0	0
0	1	1
1	1	Q

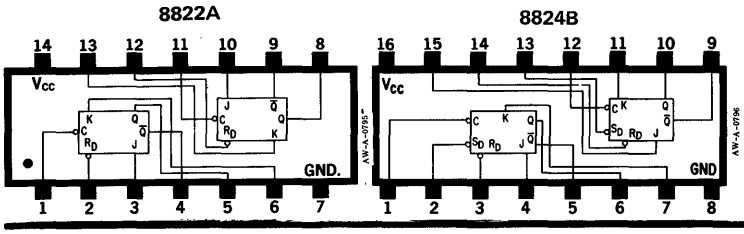
† $Q = \overline{Q} = 1$

8822

J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

$\overline{R}_D = 0 \Rightarrow Q = 0$

A PACKAGE B PACKAGE



8821
8822
8824

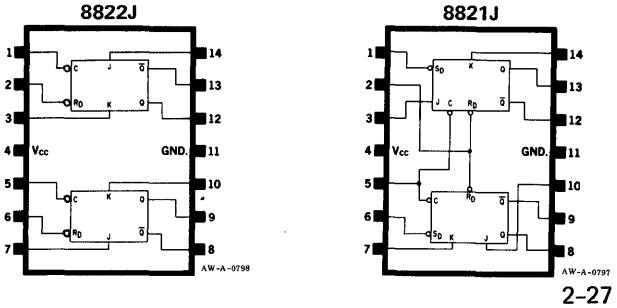
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 15)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS TEMP. S8821 S8822 S8824	TEMP. N8821 N8822 N8824	V_{cc}	SET	RESET	DRIVEN INPUT	J	K	CLOCK	OUTPUT	NOTES
A-4	"1" OUTPUT VOLTAGE (Q)	2.6			V	-55°C	0°C	4.75V	0.8V	2.0V					-500μA	8,16
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V	2.0V					-500μA	8,16
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V	2.0V					-500μA	8,16
A-5	"1" OUTPUT VOLTAGE ($\overline{Q}$)	2.6			V	-55°C	0°C	4.75V	2.0V	0.8V					-500μA	8
A-3		2.8			V	+25°C	+25°C	5.0V	2.0V	0.8V					-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V	0.8V					-500μA	8
A-5	"0" OUTPUT VOLTAGE (Q)			0.4	V	-55°C	0°C	4.75V	2.0V	0.8V					16mA	9
A-3				0.4	V	+25°C	+25°C	5.0V	2.0V	0.8V					16mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	0.8V					16mA	9
A-5	"0" OUTPUT VOLTAGE ($\overline{Q}$)			0.4	V	-55°C	0°C	4.75V	0.8V	2.0V					16mA	9,16
A-3				0.4	V	+25°C	+25°C	5.0V	0.8V	2.0V					16mA	9,16
A-4				0.4	V	+125°C	+75°C	4.75V	0.8V	2.0V					16mA	9,16
C-1	"0" INPUT CURRENT (J,K)			-1.6	mA	-55°C	0°C	5.25V			0.4V					
A-3				-1.6	mA	+25°C	+25°C	5.25V			0.4V					
C-1				-1.6	mA	+125°C	+75°C	5.25V			0.4V					
C-1	"0" INPUT CURRENT			-3.2	mA	-55°C	0°C	5.25V			0.4V					
A-3	(CLOCK, S_D, R_D)			-3.2	mA	+25°C	+25°C	5.25V			0.4V					
C-1				-3.2	mA	+125°C	+75°C	5.25V			0.4V					
C-1	"0" INPUT CURRENT			-6.4	mA	-55°C	0°C	5.25V			0.4V					
A-3	(CLOCK, R_D, 8821 only)			-6.4	mA	+25°C	+25°C	5.25V			0.4V					
C-1				-6.4	mA	+125°C	+75°C	5.25V			0.4V					
A-4	"1" INPUT CURRENT (J,K)			25	μA	+125°C	+75°C	5.0V			4.5V			0V		17
A-4	(CLOCK, S_D, R_D)			50	μA	+125°C	+75°C	5.0V			4.5V					
A-4	(CLOCK, R_D, 8821 only)			100	μA	+125°C	+75°C	5.0V			4.5V	0V	0V			
A-2	POWER CONSUMPTION (Per Binary)			72	mW	+25°C	+25°C	5.25V								
	OUTPUT SHORT CIRCUIT CURRENT															
A-2	Q (except 8822)	-20		-70	mA	+25°C	+25°C	5.0V	0V						0V	
A-2	$\overline{Q}$	-20		-70	mA	+25°C	+25°C	5.0V		0V					0V	
C-1	INPUT LATCH VOLTAGE (All Inputs)	5.5			V	+25°C	+25°C	5.0V			10mA					12,17
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V							A.C.F.O. = 6	11,14
A-6	CLOCKED MODE TURN-ON DELAY	10	25	50	ns	+25°C	+25°C	5.0V							D.C.F.O. = 20	10,14
A-6	CLOCKED MODE TURN-OFF DELAY	7	15	50	ns	+25°C	+25°C	5.0V							D.C.F.O. = 20	10,14
A-6	DIRECT MODE TURN-ON DELAY		25	50	ns	+25°C	+25°C	5.0V							D.C.F.O. = 20	10,14
A-6	DIRECT MODE TURN-OFF DELAY		15	50	ns	+25°C	+25°C	5.0V							D.C.F.O. = 20	10,14
A-6	TOGGLE RATE	10	25		MHz	+25°C	+25°C	5.0V								14
	INPUT CAPACITANCE															
C-2	(J, K)			3.0	pf	+25°C	+25°C	5.0V			2.0V					7
C-2	(R_D, S_D)			6.0	pf	+25°C	+25°C	5.0V			2.0V					7
C-2	(R_D, 8821 only)			12	pf	+25°C	+25°C	5.0V			2.0V					7
C-2	(CLOCK)			8.0	pf	+25°C	+25°C	5.0V			2.0V					7
C-2	(CLOCK, 8821 only)			16	pf	+25°C	+25°C	5.0V			2.0V					7

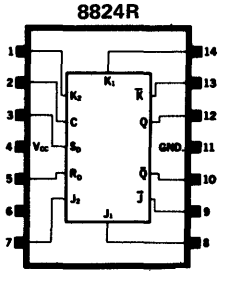
NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV$_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.
15. Test conditions and limits for the Set input are not applicable to the 8822.
16. For 8822, momentarily apply zero volts to $\overline{Q}$ and V_{cc} to Q to ensure state of the binary element prior to test measurement.
17. For clock tests, ground J and K. For J,K and S_D tests, ground clock. For R_D tests, ground J on 8821 and clock on 8822 and 8824.

J PACKAGE



R PACKAGE



SIGNETICS

DCL

INTEGRATED CIRCUITS

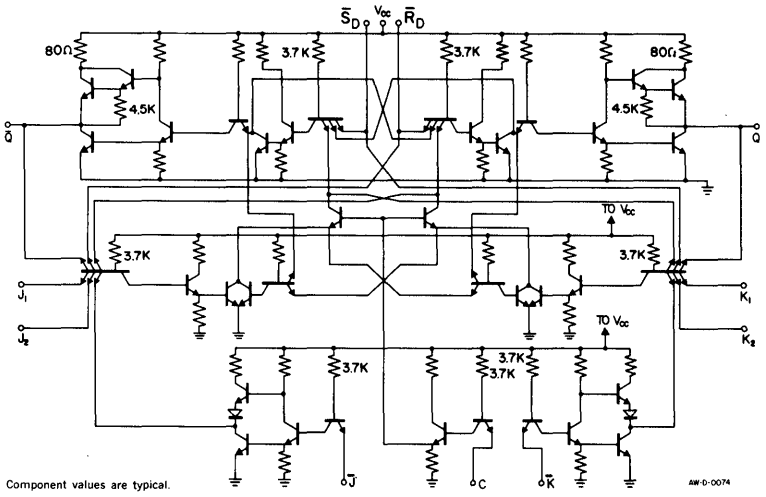
8825 DC CLOCKED J-K BINARY

The 8825 is a high-speed, direct-coupled, J-K Binary which responds to the positive transition (rising edge) of the clock pulse. For logic flexibility, two J, two K, an inverting J and an inverting K, inputs are provided. Separate set (S_D) and reset (R_D) lines are available when asynchronous operation is required. To prevent system errors, logic inputs are locked out approximately 10ns after the clock threshold voltage is reached. This feature prevents more than one logic transition per clock pulse.

The characterization of each logic element in the 8000-Series includes loading rules for driving the 8825. A convenient summary of these DC loading rules is provided in Table 1-4, Section 1.

Applications and usage rules for the 8825 may be found in Section 4.

BASIC CIRCUIT SCHEMATIC



NOTE: Component values are typical.

TRUTH TABLE

J_n	K_n	Q_{n+1}	$\bar{S}_D$	$\bar{R}_D$	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\bar{Q}_n$	1	1	Q

$J = J_1 J_2 \bar{J}$ $\quad K = K_1 K_2 \bar{K}$

n is time prior to clock

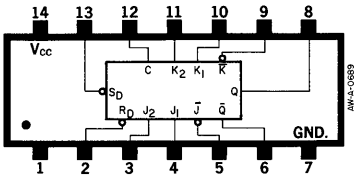
n + 1 is time following clock

† Both outputs in 0 state

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 14)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS											
		MIN.	TYP.	MAX.	UNITS	TEMP. S8825	TEMP. N8825	V_{cc}	SET	RESET	DRIVEN INPUT	J_1, J_2	$\bar{J}$	K_1, K_2	$\bar{K}$	CLOCK	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V	2.0V						0V	-500μA	8
A-3	(Q)	2.8			V	+25°C	+25°C	5.0V	0.8V	2.0V						0V	-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V	2.0V						0V	-500μA	8
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	2.0V	0.8V						0V	-500μA	8
A-3	($\bar{Q}$)	2.8			V	+25°C	+25°C	5.0V	2.0V	0.8V						0V	-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V	0.8V						0V	-500μA	8
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V	0.8V						0V	16mA	9
A-3	(Q)			0.40	V	+25°C	+25°C	5.0V	2.0V	0.8V						0V	16mA	9
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V	0.8V						0V	16mA	9
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	0.80V	2.0V						0V	16mA	9
A-3	($\bar{Q}$)			0.40	V	+25°C	+25°C	5.0V	0.80V	2.0V						0V	16mA	9
A-4				0.40	V	+125°C	+75°C	4.75V	0.80V	2.0V						0V	16mA	9
C-1	"0" INPUT CURRENT			-1.6	mA	-55°C	0°C	5.25V			0.40V							12
A-3	$J_1, J_2, \bar{J}, K_1, K_2, \bar{K}$, CLOCK			-1.6	mA	-25°C	+25°C	5.25V			0.40V							12
C-1				-1.6	mA	+125°C	+75°C	5.25V			0.40V							12
C-1	"0" INPUT CURRENT			-3.2	mA	-55°C	0°C	5.25V			0.40V		0V		0V	0V		
A-3	SET, RESET			-3.2	mA	+25°C	+25°C	5.25V			0.40V		0V		0V	0V		
C-1				-3.2	mA	+125°C	+75°C	5.25V			0.40V		0V		0V	0V		
A-4	"1" INPUT CURRENT $J_1, J_2, \bar{J}, K_1, K_2, \bar{K}$, CLOCK			40	μA	+125°C	+75°C	5.0V			4.5V							
A-4	"1" INPUT CURRENT SET, RESET			80	μA	+125°C	+75°C	5.0V			4.5V					0V		
A-6	TURN-ON DELAY			50	ns	+25°C	+25°C	5.0V									D.C. F.O.=20	15
A-6	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.0V									D.C. F.O. = 20	15
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V									A.C. F.O.=6	11, 15
A-6	TOGGLE RATE	15			mHz	+25°C	+25°C	5.0V										15
	MINIMUM INPUT SET-UP TIME		15		ns	+25°C	+25°C	5.0V										15
	MINIMUM INPUT HOLD TIME		10		ns	+25°C	+25°C	5.0V										15
C-2	INPUT CAPACITANCE $J_1, J_2, \bar{J}, K_1, K_2, \bar{K}$, CLOCK			3.0	pf	+25°C	+25°C	5.0V			2.0V							7
C-2	INPUT CAPACITANCE SET, RESET			6.0	pf	+25°C	+25°C	5.0V			2.0V							
A-2	POWER CONSUMPTION		70	132	mW	+25°C	+25°C	5.25V								0V		
C-1	INPUT LATCH VOLTAGE ALL INPUTS	5.5			V	+25°C	+25°C	5.0V			10mA							13
A-2	OUTPUT SHORT CIRCUIT CURRENT Q	-20		-70	mA	+25°C	+25°C	5.0V	0V							0V	0V	
	$\bar{Q}$	-20		-70	mA	+25°C	+25°C	5.0V		0V						0V	0V	

A PACKAGE



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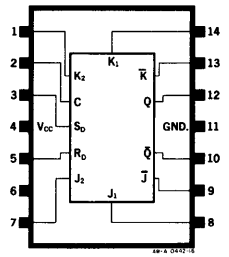
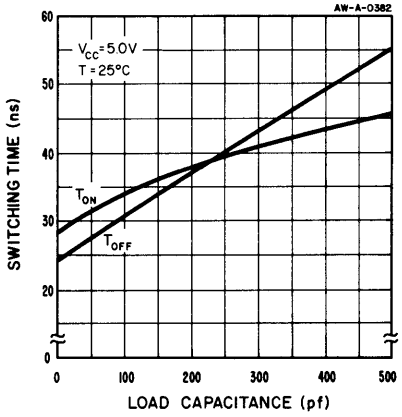
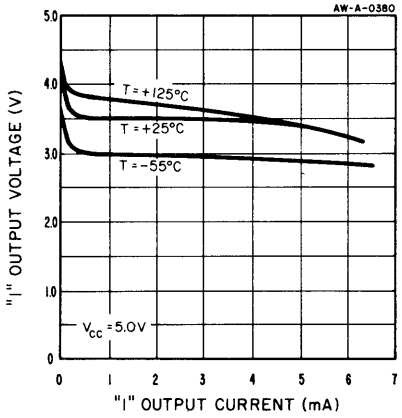


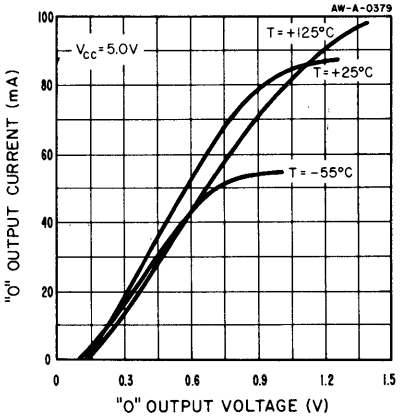
8825

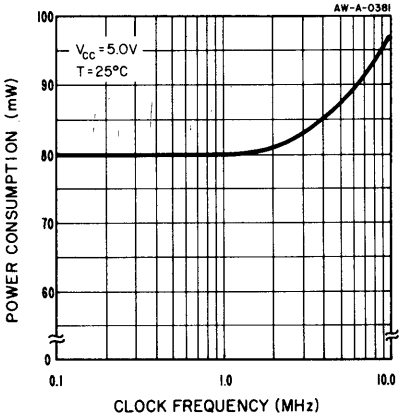
Notes:

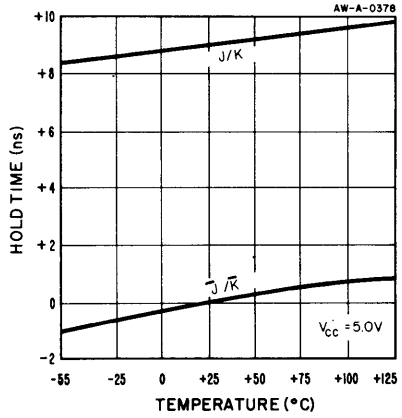
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV rms. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. Input current measurements at J_1, J_2 require $\overline{J}$ = CLOCK = zero volts and momentarily ground RESET. Input current measurements at K_1, K_2 require $\overline{K}$ = CLOCK = zero volts and momentarily ground SET.
13. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.

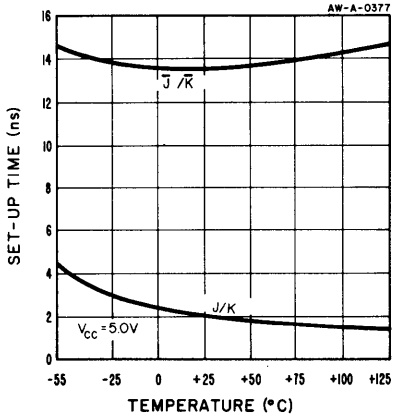


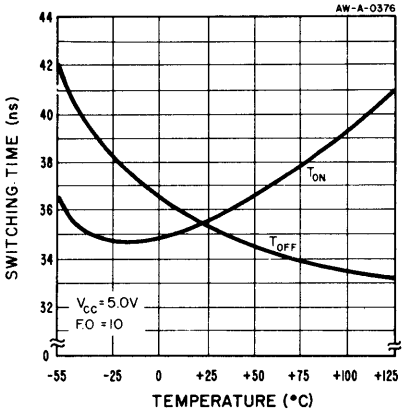












SIGNETICS DCL INTEGRATED CIRCUITS

8826 DUAL J-K BINARY

The 8826 is a capacitively coupled, high-speed, Dual J-K Binary intended for use in systems requiring storage and counting rates up to 25MHz. Two completely separate binaries are provided with common connections only at V_{CC} and ground. Separate J, K, Clock, Q and $\overline{Q}$, and Reset lines are provided for each binary. The AC clock steering network provides high speed operation with low power consumption.

This element responds to the trailing or negative-going transition of the clock pulse. The Reset line may be activated regardless of the state of the clock.

Characterization of each logic element in the 8800 group includes loading rules for driving the 8826. A convenient summary of these AC loading rules is provided in Table 1-5, Section 1.

Detailed usage and applications information may be found in Section 4.

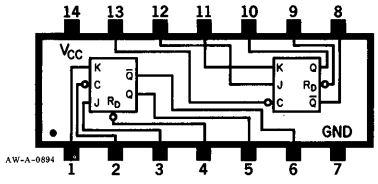
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 15)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS								
		MIN.	TYP.	MAX.	UNITS	TEMP. S8826	TEMP. N8826	Vcc	RESET	CLOCK	J	K	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	2.0V				-250μA	8, 12
A-3	Q_1, Q_2	2.8			V	+25°C	+25°C	5.0V	2.0V				-250μA	8, 12
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V				-250μA	8, 12
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V				-250μA	8
A-3	$\overline{Q}_1, \overline{Q}_2$	2.8			V	+25°C	+25°C	5.0V	0.8V				-250μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.7V				-250μA	8
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	0.8V				8.0mA	9
A-3	Q_1, Q_2			0.40	V	+25°C	+25°C	5.0V	0.8V				8.0mA	9
A-4				0.40	V	+125°C	+75°C	4.75V	0.7V				8.0mA	9
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V				8.0mA	9, 12
A-3	$\overline{Q}_1, \overline{Q}_2$			0.40	V	+25°C	+25°C	5.0V	2.0V				8.0mA	9, 12
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V				8.0mA	9, 12
C-1	"0" INPUT CURRENT			-2.4	mA	-55°C	0°C	5.25V			0.40V	0.40V		
A-3	J_1, K_1, J_2, K_2			-2.4	mA	+25°C	+25°C	5.25V			0.40V	0.40V		
C-1				-2.4	mA	+125°C	+75°C	5.25V			0.40V	0.40V		
C-1	"0" INPUT CURRENT			-2.0	mA	-55°C	0°C	5.25V	0.40V					
A-3	$RESET_1, RESET_2$			-2.0	mA	+25°C	+25°C	5.25V	0.40V					
C-1				-2.0	mA	+125°C	+75°C	5.25V	0.40V					
C-1	"0" INPUT CURRENT			-10	μA	+25°C	+25°C	5.25V		0.40V				
A-3	C_{P_1}, C_{P_2} (CLOCK)			-10	μA	+25°C	+25°C	5.25V		0.40V				
C-1				-10	μA	+125°C	+75°C	5.25V		0.40V				
A-4	"1" INPUT CURRENT $J_1, J_2, K_1, K_2, RESET_1, RESET_2$			25	μA	+125°C	+75°C	5.0V	4.5V		4.5V	4.5V		13
A-4	"1" INPUT CURRENT C_{P_1}, C_{P_2} (CLOCK)			25	μA	+125°C	+75°C	5.0V		4.5V				
A-2	POWER CONSUMPTION (Per Binary)			64	mW	+25°C	+25°C	5.25V						
A-2	OUTPUT SHORT CIRCUIT CURRENT $\overline{Q}_1, \overline{Q}_2$ ONLY	-20		-70	mA	+25°C	+25°C	5.0V	0V				0V	
C-1	INPUT LATCH VOLTAGE $J_1, J_2, K_1, K_2, RESET_1, RESET_2$	5.5			V	+25°C	+25°C	5.0V	10mA		10mA	10mA		13, 14
	C_{P_1}, C_{P_2}	5.0		6.0	V	+25°C	+25°C	5.0V		10μA				
A-6	TURN-ON DELAY			35	ns	+25°C	+25°C	5.0V					D.C. F.O.-10	10, 16
A-6	TURN-OFF DELAY			20	ns	+25°C	+25°C	5.0V					D.C. F.O. -10	10, 16
A-6	TOGGLE RATE	25			MHz	+25°C	+25°C	5.0V						16
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V					A.C. F.O.-2	11, 16
C-2	INPUT CAPACITANCE $J_1, J_2, K_1, K_2, RESET_1, RESET_2$			3.0	pf	+25°C	+25°C	5.0V	2.0V		2.0V	2.0V		7
C-2	INPUT CAPACITANCE C_{P_1}, C_{P_2} (CLOCK)			50	pf	+25°C	+25°C							7
A-6	CLOCK MODE HOLDING TEST			10	ns	+25°C	+25°C	5.0V		PULSE				16
A-6	CLOCK MODE SWITCHING TEST			50	ns	+25°C	+25°C	5.0V		PULSE				16

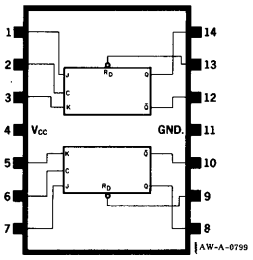
Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. One DC fan-out is defined as 0.8mA
11. One AC fan-out is defined as 50pf.
12. Momentarily apply zero volts to $\overline{Q}$ and V_{CC} to Q to ensure state of the binary element prior to test measurement.
13. To test "1" INPUT CURRENT AND LATCH VOLTAGE RATING for J and RESET, ensure Q = "0". To test "1" INPUT CURRENT AND LATCH VOLTAGE RATING for K, ensure $\overline{Q}$ = "0".
14. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
15. Manufacturer reserves the right to make design and process changes and improvements.
16. Detailed test conditions for AC testing are in Section 3.

A PACKAGE

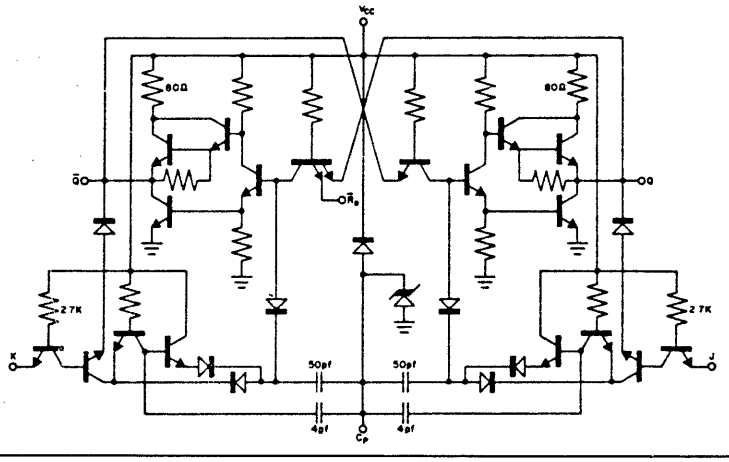


J PACKAGE



8826

BASIC CIRCUIT SCHEMATIC

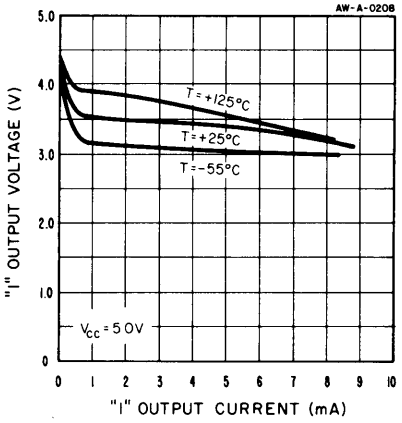


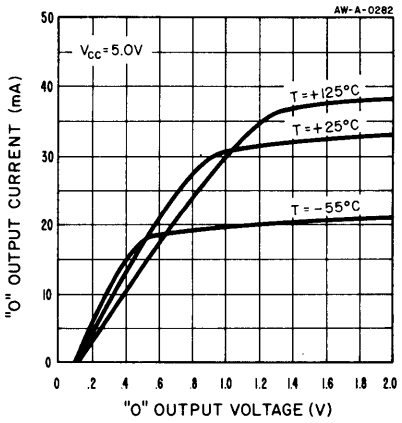
TRUTH TABLE

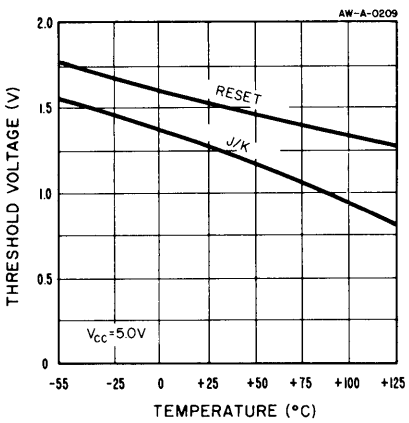
J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

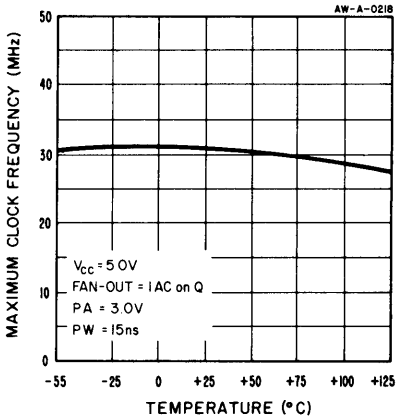
$\overline{R}_D = 0 \Rightarrow Q = 0$

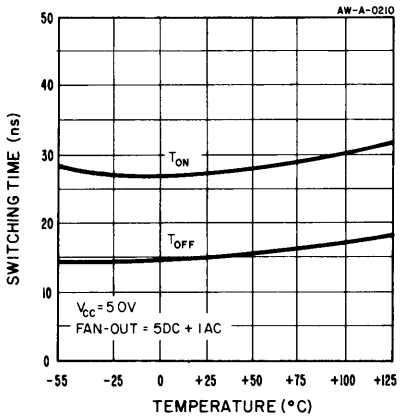
n is time prior to clock
n+1 is time following clock

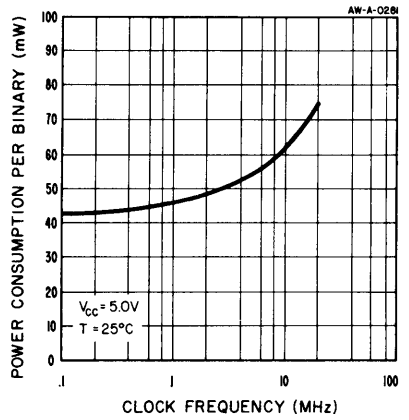












SIGNETICS DCL INTEGRATED CIRCUITS

8827 DUAL J-K BINARY

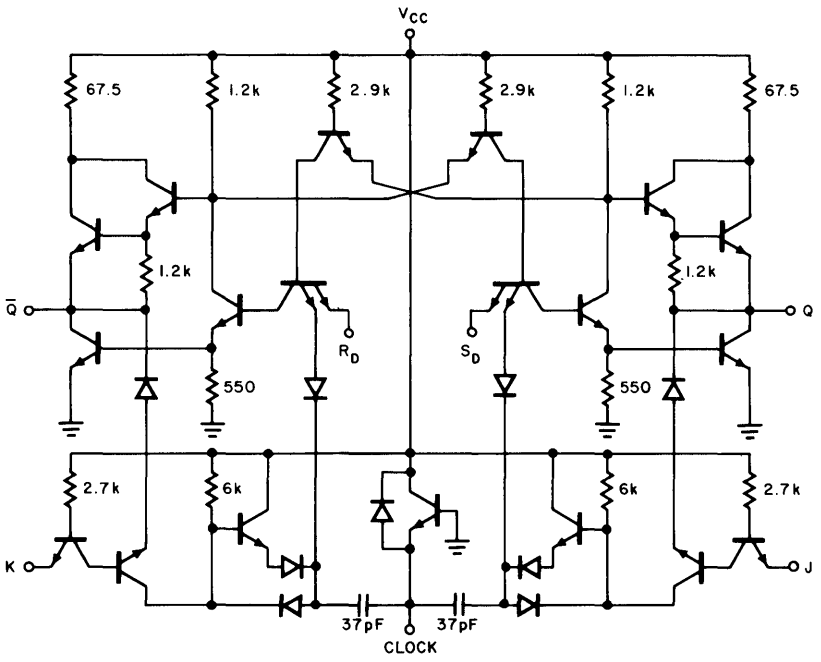
The 8827 is a Dual J-K Binary especially suited to high-speed parallel load counter and shift register applications. The clock and asynchronous reset inputs on the two binaries are common to allow separate Q, $\overline{Q}$, S_D (asynchronous set) and J and K. The S_D/R_D lines may be activated regardless of the state of the clock.

The clock input of the 8827 is capacitively coupled; clocking is effected on the negative-going transition of the clock pulse. All elements in the 8000 Series are characterized for AC fan-out to assure compatible operation under worst case conditions.

Table 1-5 of Section 1 summarizes AC loading guarantees for the 8827.

Section 4 provides detailed usage suggestions and applications.

BASIC CIRCUIT SCHEMATIC



TRUTH TABLE

J_n	K_n	Q_{n+1}	$\overline{S}_D$	$\overline{R}_D$	Q
0	0	Q_n	1	1	Q
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	0	0	†

n is time prior to clock
n+1 is time following clock
† = both outputs in "1" state

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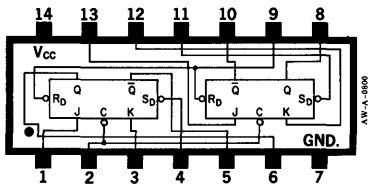

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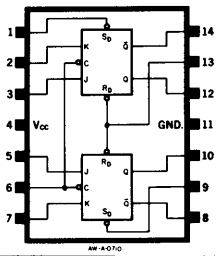


8827

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 14)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS									
		MIN.	TYP.	MAX.	UNITS	TEMP. S8827	TEMP. N8827	V_{CC}	RESET	SET	CLOCK	J	K	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	2.0V	0.8V				-250μA	8
A-3	Q_1, Q_2	2.8			V	+25°C	+25°C	5.00V	2.0V	0.8V				-250μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V	0.7V				-250μA	8
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V	2.0V				-250μA	8
A-3	$\overline{Q}_1$, $\overline{Q}_2$	2.8			V	+25°C	+25°C	5.00V	0.8V	2.0V				-250μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.7V	2.0V				-250μA	8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	0.8V	2.0V				8.0mA	9
A-3	Q_1, Q_2			0.4	V	+25°C	+25°C	5.00V	0.8V	2.0V				8.0mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	0.7V	2.0V				8.0mA	9
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V	0.8V				8.0mA	9
A-3	$\overline{Q}_1$, $\overline{Q}_2$			0.4	V	+25°C	+25°C	5.00V	2.0V	0.8V				8.0mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	0.7V				8.0mA	9
C-1	"0" INPUT CURRENT	-0.1		-2.4	mA	-55°C	0°C	5.25V				0.4V	0.4V		
A-3	J_1. K_1. J_2. K_2	-0.1		-2.4	mA	+25°C	+25°C	5.25V				0.4V	0.4V		
C-1		-0.1		-2.4	mA	+125°C	+75°C	5.25V				0.4V	0.4V		
C-1	"0" INPUT CURRENT	-0.1		-4.0	mA	-55°C	0°C	5.25V	0.4V						
A-3	RESET	-0.1		-4.0	mA	+25°C	+25°C	5.25V	0.4V						
C-1		-0.1		-4.0	mA	+125°C	+75°C	5.25V	0.4V						
C-1	"0" INPUT CURRENT	-0.1		-2.0	mA	-55°C	0°C	5.25V		0.4V					
A-3	SET_1, SET_2	-0.1		-2.0	mA	+25°C	+25°C	5.25V		0.4V					
C-1		-0.1		-2.0	mA	+125°C	+75°C	5.25V		0.4V					
C-1	"0" INPUT CURRENT	-0.1		-20	μA	-55°C	0°C	5.25V			0.4V				
A-3	CLOCK	-0.1		-20	μA	+25°C	+25°C	5.25V			0.4V				
C-1		-0.1		-20	μA	+125°C	+75°C	5.25V			0.4V				
A-4	"1" INPUT CURRENT J_1, J_2, K_1, K_2, SET_1, SET_2			25	μA	+125°C	+75°C	5.00V		4.5V		4.5V	4.5V		12
A-4	"1" INPUT CURRENT RESET			50	μA	+125°C	+75°C	5.00V	4.5V						
A-4	"1" INPUT CURRENT CLOCK			50	μA	+125°C	+75°C	5.00V			4.5V				
A-2	POWER CONSUMPTION (Per Binary)			64	mW	+25°C	+25°C								
A-2	OUTPUT SHORT CIRCUIT CURRENT $\overline{Q}_1$, $\overline{Q}_2$	-20		-70	mA	+25°C	+25°C	5.00V	0V					0V	
A-2	OUTPUT SHORT CIRCUIT CURRENT Q_1, Q_2	-20		-70	mA	+25°C	+25°C	5.00V		0V				0V	
C-1	INPUT LATCH VOLTAGE J_1, J_2, K_1, K_2, RESET, SET_1, SET_2,	5.5			V	+25°C	+25°C	5.00V	10mA	10mA		10mA	10mA		12, 13
	CLOCK	5.0		6.0	V	+25°C	+25°C	5.00V			10μA				
A-6	TURN-ON DELAY			35	ns	+25°C	+25°C	5.00V						D.C.F.O=10	10, 15
A-6	TURN-OFF DELAY			20	ns	+25°C	+25°C	5.00V						D.C.F.O=10	10, 15
A-6	TOGGLE RATE	25			MHz	+25°C	+25°C	5.00V							15
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V						A.C.F.O=2	11, 15
C-2	INPUT CAPACITANCE J_1, J_2, K_1, K_2, SET_1, SET_2			3.0	pf	+25°C	+25°C	5.00V		2.0V		2.0V	2.0V		7
C-2	INPUT CAPACITANCE RESET			6.0	pf	+25°C	+25°C	5.00V	2.0V						7
C-2	INPUT CAPACITANCE CLOCK			100	pf	+25°C	+25°C								7
A-6	CLOCK MODE HOLDING TEST			10	ns	+25°C	+25°C	5.00V			PULSE				15
A-6	CLOCK MODE SWITCHING TEST			50	ns	+25°C	+25°C	5.00V			PULSE				15

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. F = 1 MHz, V_{ac} = 25 mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8 mA.
11. One AC fan-out is defined as 50 pf.
12. To test "1" INPUT CURRENT and LATCH VOLTAGE RATING for J and RESET, ensure Q = "0". To test "1" INPUT CURRENT and LATCH VOLTAGE RATING for K and SET, ensure $\overline{Q}$ = "0".
13. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.

SIGNETICS DCL INTEGRATED CIRCUITS

8828 DUAL D BINARY

The 8828 is a Dual Delay (D) Binary which responds to the positive-going transition of the clock pulse. Each binary has one synchronous logic input (D), a clock line, complementary outputs, and asynchronous set and reset lines. The logic level defined at the D input, prior to activation of the clock, appears at the Q output upon activation of the clock.

The delay binary is ideally suited for general application in shift registers and ripple counters.

Detailed usage rules and suggested applications for the 8828 may be found in Section 4 of the handbook.

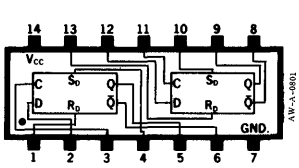
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS								
		MIN.	TYP.	MAX.	UNITS	TEMP. S8828	TEMP. N8828	V_{cc}	RESET	SET	CLOCK	D	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE (Q_1, Q_2)	2.6	2.8		V	-55°C	0°C	4.75V	2.0V	0.8V			-500μA	7
A-3		2.8	3.1		V	+25°C	+25°C	5.0V	2.0V	0.8V			-500μA	7
A-4		2.6	3.4		V	+125°C	+75°C	4.75V	2.0V	0.8V			-500μA	7
A-5	"1" OUTPUT VOLTAGE ($\bar{Q}_1$, $\bar{Q}_2$)	2.6	2.8		V	-55°C	0°C	4.75V	0.8V	2.0V			-500μA	7
A-3		2.8	3.1		V	+25°C	+25°C	5.0V	0.8V	2.0V			-500μA	7
A-4		2.6	3.4		V	+125°C	+75°C	4.75V	0.8V	2.0V			-500μA	7
A-5	"0" OUTPUT VOLTAGE (Q_1, Q_2)		0.30	0.40	V	-55°C	0°C	4.75V	0.8V	2.0V			16mA	8
A-3			0.30	0.40	V	+25°C	+25°C	5.0V	0.8V	2.0V			16mA	8
A-4			0.30	0.40	V	+125°C	+75°C	4.75V	0,8V	2.0V			16mA	8
A-5	"0" OUTPUT VOLTAGE ($\bar{Q}_1$, $\bar{Q}_2$)		0.30	0.40	V	-55°C	0°C	4.75V	2.0V	0.8V			16mA	8
A-3			0.30	0.40	V	+25°C	+25°C	5.0V	2.0V	0.8V			16mA	8
A-4			0.30	0.40	V	+125°C	+75°C	4.75V	2.0V	0.8V			16mA	8
C-1	"0" INPUT CURRENT (D_1, D_2)	-0.1	-1.3	-1.6	mA	-55°C	0°C	5.25V			0V	0.40V		
A-3		-0.1	-1.3	-1.6	mA	+25°C	+25°C	5.25V			0V	0.40V		
C-1		-0.1	-1.3	-1.6	mA	+125°C	+75°C	5.25V			0V	0.40V		
C-1	"0" INPUT CURRENT	-0.1	-2.5	-3.2	mA	-55°C	0°C	5.25V	0V	0.40V				9
A-3	(SET_1, SET_2)	-0.1	-2.5	-3.2	mA	+25°C	+25°C	5.25V	0V	0.40V				9
C-1		-0.1	-2.5	-3.2	mA	+125°C	+75°C	5.25V	0V	0.40V				9
C-1	"0" INPUT CURRENT	-0.1	-2.5	-3.2	mA	-55°C	0°C	5.25V			0.40V			
A-3	($CLOCK_1$, $CLOCK_2$)	-0.1	-2.5	-3.2	mA	+25°C	+25°C	5.25V			0.40V			
C-1		-0.1	-2.5	-3.2	mA	+125°C	+75°C	5.25V			0.40V			
C-1	"0" INPUT CURRENT	-0.1	-3.3	-4.8	mA	-55°C	0°C	5.25V	0.40V	0V				10
A-3	($RESET_1$, $RESET_2$)	-0.1	-3.3	-4.8	mA	+25°C	+25°C	5.25V	0.40V	0V				10
C-1		-0.1	-3.3	-4.8	mA	+125°C	+75°C	5.25V	0.40V	0V				10
C-1	"1" INPUT CURRENT		10	25	μA	-55°C	0°C	5.0V	0V			4.5V		
C-1	(D_1, D_2)		10	25	μA	+25°C	+25°C	5.0V	0V			4.5V		
A-4			10	25	μA	+125°C	+75°C	5.0V	0V			4.5V		
C-1	"1" INPUT CURRENT		20	50	μA	-55°C	0°C	5.0V		4.5V				11
C-1	(SET_1, SET_2)		20	50	μA	+25°C	+25°C	5.0V		4.5V				11
A-4			20	50	μA	+125°C	+75°C	5.0V		4.5V				11
C-1	"1" INPUT CURRENT		20	50	μA	-55°C	0°C	5.0V	0V		4.5V			
C-1	($CLOCK_1$, $CLOCK_2$)		20	50	μA	+25°C	+25°C	5.0V	0V		4.5V			
A-4			20	50	μA	+125°C	+75°C	5.0V	0V		4.5V			
C-1	"1" INPUT CURRENT		30	75	μA	-55°C	0°C	5.0V	4.5V		0V	0V		12
C-1	($RESET_1$, $RESET_2$)		30	75	μA	+25°C	+25°C	5.0V	4.5V		0V	0V		12
A-4			30	75	μA	+125°C	+75°C	5.0V	4.5V		0V	0V		12
A-2	POWER CONSUMPTION (Per Binary)			610	mW	+25°C	+25°C	5.25V			0V	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT (Q_1, Q_2)	-10		-55	mA	+25°C	+25°C	5.0V		0V			0V	
A-2	OUTPUT SHORT CIRCUIT CURRENT ($\bar{Q}_1$, $\bar{Q}_2$)	-10		-55	mA	+25°C	+25°C	5.0V	0V				0V	
C-1	INPUT LATCH VOLTAGE (D_1, D_2, $CLOCK_1$, $CLOCK_2$, $CLEAR_1$, $CLEAR_2$, $PRESET_1$, $PRESET_2$)	5.5			V	+25°C	+25°C	5.0V	10mA	10mA	10mA	10mA		13
A-6	TURN-ON DELAY		28	50	ns	+25°C	+25°C	5.0V					D.C. F.O.=20	14, 16
A-6	TURN-OFF DELAY		20	35	ns	+25°C	+25°C	5.0V					D.C. F.O.=20	14, 16
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V					A.C. F.O.=6	16, 17

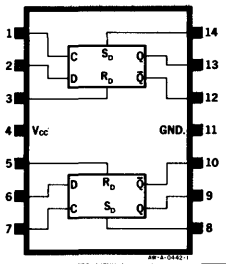
Notes:

1. All voltage and capcitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electricallv open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{cc}.
9. The SET input is specified at two standard loads because if $\bar{Q}$ = "1" when SET goes to "0", the output driving the SET line must be capable of sinking the current from 4 standard loads to make the flip-flop change state. Once the binary state is changed, less than 4 loads will be seen by the driving gate; i.e., when Q = "0".
10. This test simulates worst case transient condition. If SET, RESET, DATA, CLOCK and Q = "1" prior to activating the RESET line, the gate driving RESET must be capable of sinking the current from 6 standard loads. Once the flip-flop changes state, i.e., Q = "0", less than 6 standard loads will be seen by the driving gate.
11. To test "1" Input Current for SET input, momentarily ground SET to ensure Q = "1" and $\bar{Q}$ = "0".
12. To test "1" Input Current for RESET input, momentarily ground RESET to ensure Q = "0".
13. This test guarantees operation free of input latch-up over the specified operating power supply range.
14. One DC fan-out is defined as 0.8mA.
15. Manufacturer reserves the right to make design and process changes and improvements.
16. Detailed test conditions for AC testing are in Section 3.
17. One AC fan-out is defined as 50pf.

A PACKAGE

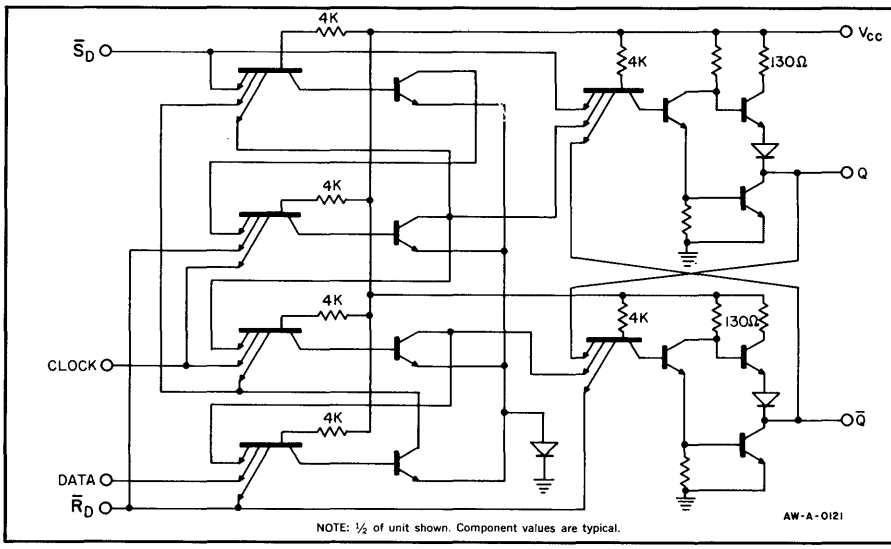


J PACKAGE



8828

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

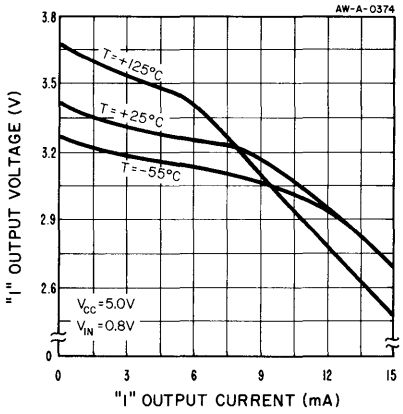
TRUTH TABLE

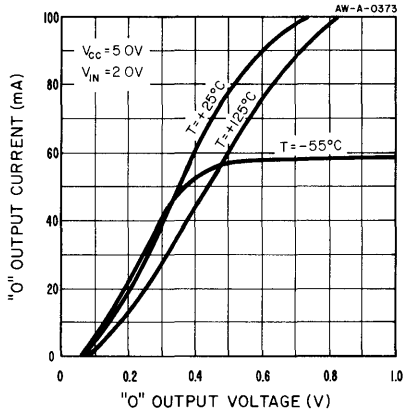
D_n	Q_{n+1}	$\bar{Q}_{n+1}$
1	1	0
0	0	1

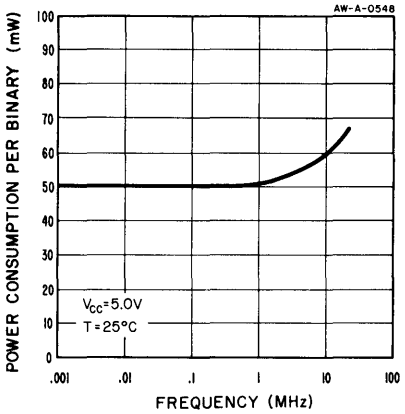
$\bar{S}_D$	$\bar{R}_D$	Q
1	1	Q
1	0	0
0	1	1
0	0	†

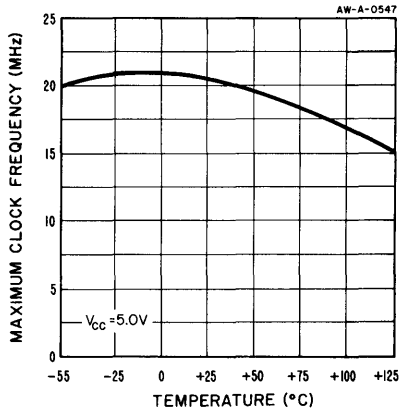
† Both outputs in 1 state

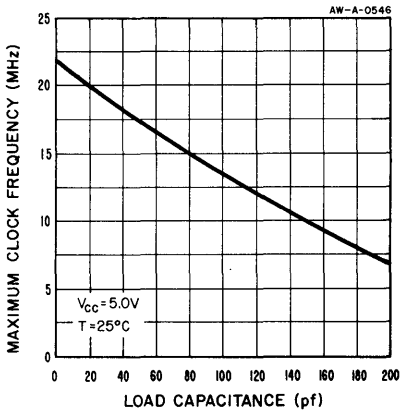
n is time prior to clock
n+1 is time following clock











SIGNETICS DCL INTEGRATED CIRCUITS

8829 HIGH SPEED J-K BINARY

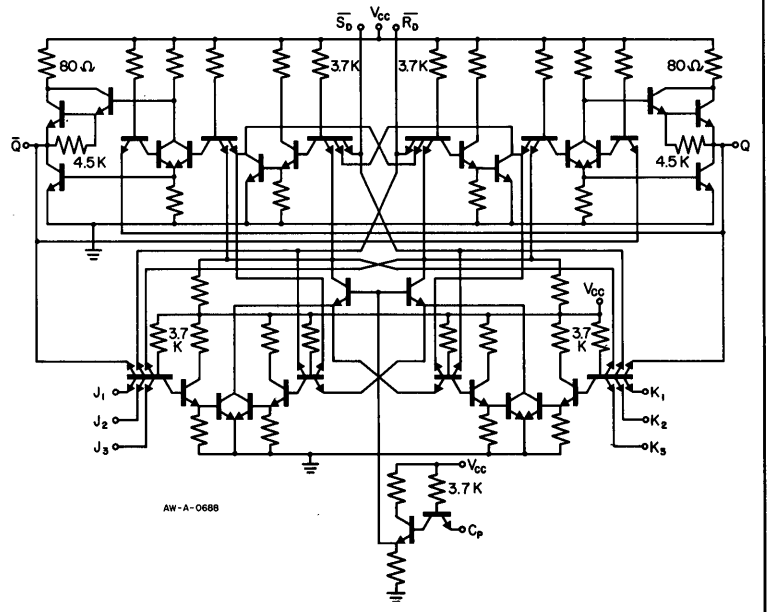
The 8829 is a high speed, direct-coupled J-K Binary which responds to the negative transition (falling edge) of the clock pulse. For logic flexibility, three J and three K inputs and asynchronous $\overline{SET}$ and $\overline{RESET}$ control lines are provided.

To prevent system errors, the 8829 features clock skew tolerances approximately equal to the clock pulse width. This feature is the result of "lock-out" of the logic inputs on the positive transition of the clock signal while the outputs are not activated until the negative transition of the clock signal.

The characterization of each logic element in the 8000 series includes loading rules for driving the 8829. A convenient summary of these DC loading rules is provided in Table 1-4, Section 1.

Detailed usage rules and application information may be found in Section 4.

BASIC CIRCUIT SCHEMATIC



TRUTH TABLE

J_n	K_n	Q_{n+1}	$\overline{S}_D$	$\overline{R}_D$	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	Q

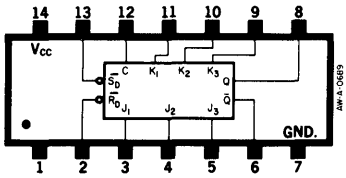
$J = J_1 J_2 J_3$ $\quad K = K_1 K_2 K_3$

n is time prior to clock

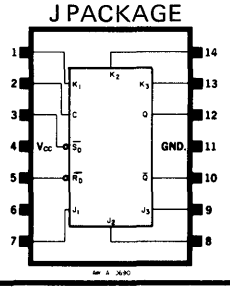
n + 1 is time following clock

† Both outputs in 0 state

A PACKAGE



J PACKAGE



8829

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 14)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	TEST LIMITS				TEST CONDITIONS										
		MIN.	TYP.	MAX.	UNITS	TEMP. S8829	TEMP. N8829	V_{cc}	$\overline{SET}$	$\overline{RESET}$	DRIVEN INPUT	J_1, J_2, J_3	K_1, K_2, K_3	CLOCK	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V	2.0V				OV	-500μA	7
A-3	(Q)	2.8			V	+25°C	+25°C	5.00V	0.8V	2.0V				OV	-500μA	7
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V	2.0V				OV	-500μA	7
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	2.0V	0.8V				OV	-500μA	7
A-3	($\overline{Q}$)	2.8			V	+25°C	+25°C	5.00V	2.0V	0.8V				OV	-500μA	7
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V	0.8V				OV	-500μA	7
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V	0.8V				OV	16mA	8
A-3	(Q)			0.4	V	+25°C	+25°C	5.00V	2.0V	0.8V				OV	16mA	8
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	0.8V				OV	16mA	8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	0.8V	2.0V				OV	16mA	8
A-3	($\overline{Q}$)			0.4	V	+25°C	+25°C	5.00V	0.8V	2.0V				OV	16mA	8
A-4				0.4	V	+125°C	+75°C	4.75V	0.8V	2.0V				OV	16mA	8
C-1	"0" INPUT CURRENT			-1.6	mA	-55°C	0°C	5.25V			0.4V					11
A-3	$J_1, J_2, J_3, K_1, K_2, K_3$, CLOCK	-0.1		-1.6	mA	+25°C	+25°C	5.25V			0.4V					11
C-1				-1.6	mA	+125°C	+75°C	5.25V			0.4V					11
C-1	"0" INPUT CURRENT			-4.8	mA	-55°C	0°C	5.25V			0.4V			OV		
A-3	$\overline{S}_D, \overline{R}_D$	-0.1		-4.8	mA	+25°C	+25°C	5.25V			0.4V			OV		
C-1				-4.8	mA	+125°C	+75°C	5.25V			0.4V			OV		
A-4	"1" INPUT CURRENT $J_1, J_2, J_3, K_1, K_2, K_3$, CLOCK			40	μA	+125°C	+75°C	5.00V			4.5V					
A-4	"1" INPUT CURRENT $\overline{S}_D, \overline{R}_D$			80	μA	+125°C	+75°C	5.00V			4.5V			OV		
A-6	TURN-ON DELAY			50	ns	+25°C	+25°C	5.00V							D.C. F.O. = 20	15
A-6	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.00V							D.C. F.O. = 20	15
A-6	TOGGLE RATE	15			mHz	+25°C	+25°C	5.00V								15
C-2	OUTPUT FALL TIME			50	ns	-55 C	0°C	4.75V							A.C. F.O. = 6	10, 15
	INPUT SET-UP TIME		10		ns	+25°C	+25°C	5.00V								13, 15
	INPUT TIME, T_x		10		ns	+25°C	+25°C	5.00V								13, 15
C-2	INPUT CAPACITANCE $J_1, J_2, J_3, K_1, K_2, K_3$, CLOCK			3.0	pf	+25°C	+25°C	5.00V			2.0V					6
C-2	INPUT CAPACITANCE $\overline{S}_D, \overline{R}_D$			6.0	pf	+25°C	+25°C	5.00V			2.0V					6
A-2	POWER CONSUMPTION		75	132	mW	+25°C	+25°C	5.25V						OV		
C-1	INPUT LATCH VOLTAGE ALL INPUTS	5.5			V	+25°C	+25°C	5.00V			10mA					
A-2	OUTPUT SHORT Q	-20		-70	mA	+25°C	+25°C	5.00V		OV				OV	OV	
	CIRCUIT CURRENT $\overline{Q}$	-20		-70	mA	+25°C	+25°C	5.00V	OV					OV	OV	

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Capacitance as measured on Boonton Electronic Corporation Model 75A-58 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
7. Output current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Input current measurements at J_1, J_2, J_3 require that Clock = 0V and R_D be momentarily grounded. Input current measurements at K_1, K_2, K_3 require that Clock = 0V and S_D be momentarily grounded.
12. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
13. Since logic "lock-out" occurs on the positive going transition of the clock pulse, the logic level present prior to that edge of the clock need only remain present for an additional 10ns (typ.). The logic inputs need not be stabilized again until 10ns (typ.) prior to the next positive transition of the clock. The clock skew tolerance is therefor typically the clock pulse width minus 10ns.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.

SIGNETICS DCL INTEGRATED CIRCUITS

8840 DUAL EXPANDABLE AND-OR-INVERT GATE

The 8840 Expandable AND-OR-INVERT Gate may be used to implement the Exclusive-OR, NOR, or any AND-OR-INVERT function. It is designed for highest switching speed while maintaining high fan-out and noise margin.

Nodes are provided at the collector and emitter of the second stage pair. This allows expansion of the number of input AND terms and hence increased system usefulness.

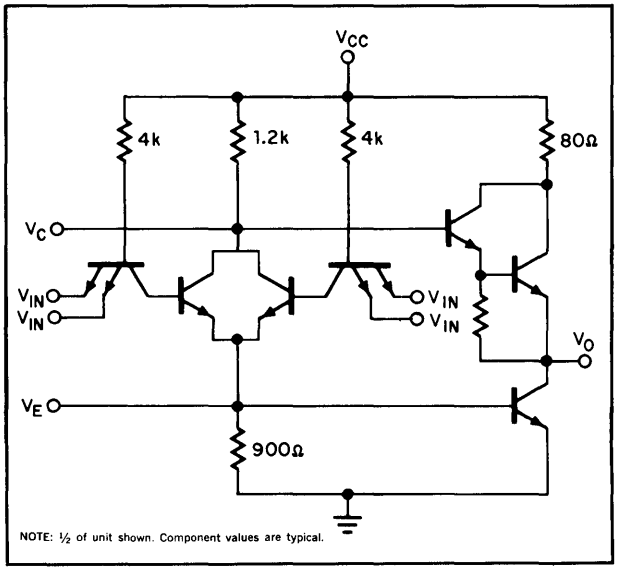
The compatibly characterized 8806 Expander is recommended for expansion of the 8840. See correlation table, opposite page.

Low output impedance in the "1" and "0" output states ensures maximum AC noise immunity at the output.

General areas of application for the 8840 include half and full adders, digital comparators, and AND-OR control logic for inputs to binary clock steering lines.

Detailed usage rules and specific applications are provided in Section 4 of this handbook.

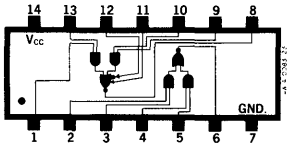
BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 19)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8840	TEMP. N8840	V_{cc}	DRIVEN AND INPUTS	OTHER AND INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V		-500μA	8, 14, 21
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V		-500μA	8, 14, 21
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V		-500μA	8, 14, 21
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V	2.0V	16mA	9, 12, 14
A-3				0.40	V	+25°C	+25°C	5.0V	2.0V	2.0V	16mA	9, 12, 14
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V	2.0V	16mA	9, 12, 14
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.40V			13, 14
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.40V			13, 14
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.40V			13, 14
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		14, 15
A-6	TURN-ON DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O.=20	10, 22
A-6	TURN-OFF DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O. = 20	10, 22
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C. F.O. = 6	11, 22
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION "0"			37.3	mW	+25°C	+25°C	5.25V				
A-2	(Per Gate) "1"			17.9	mW	+25°C	+25°C	5.25V	0V			14, 16
C-1	INPUT LATCH VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	10mA	0V		14, 18
A-2	OUTPUT SHORT CIRCUIT CURRENT	-20		-70	mA	+25°C	+25°C	5.0V	0V		0V	

A PACKAGE



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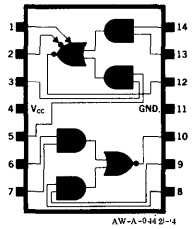


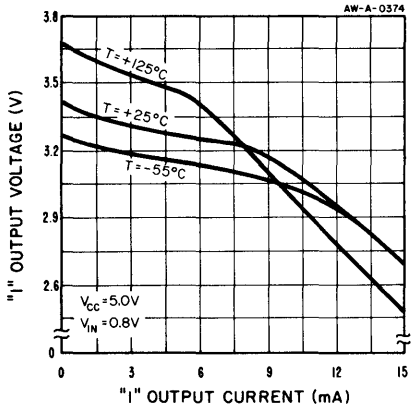
8840

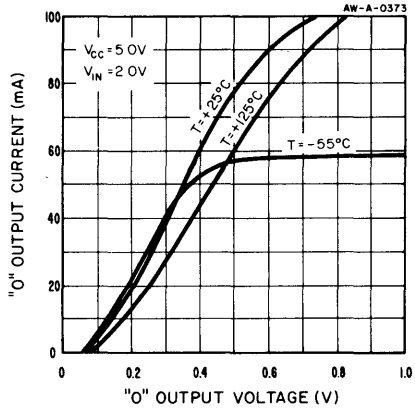
CORRELATION TABLE (8806)

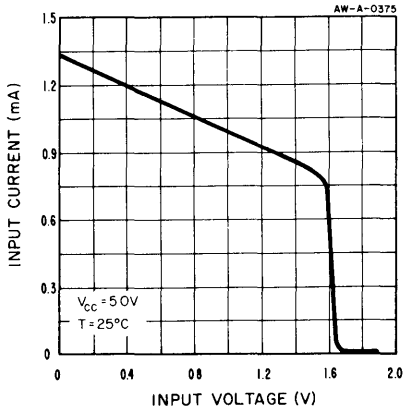
ACCEPTANCE TEST SUB-GROUP	TEST NO.	CHARACTERISTIC	LIMITS				TEST CONDITIONS					
			MIN.	TYP.	MAX.	UNITS	TEMP. S8806 N8806	V_{cc}	V_C	V_E	OUTPUTS	NOTES
A-2	1	"0" INPUT CURRENT AT V_C	-2.2		-3.65	mA	+25°C	4.75V	1.25V			20
A-2	2	TURN-ON VOLTAGE AT V_E			0.85	V	+25°C	4.75V	1.25V	2.5 mA	16mA	9, 21
A-2	3	"0" OUTPUT VOLTAGE			0.40	V	+25°C	4.75V	1.25V	2.5 mA	16mA	9, 20
A-2	4	"1" OUTPUT VOLTAGE	2.8			V	+25°C	5.0V	-200μA	+500μA	-500μA	8, 21
A-2	5	"1" OUTPUT VOLTAGE	2.8			V	+25°C	5.0V	-200μA	0.59V	-500μA	8, 21

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. AC fan-out is defined as 50pf.
12. To measure "0" output voltage, apply 2.0V to the input terminals of one of the input AND gates and apply zero volts to the input terminals of the associated input AND gate. Reverse the input conditions and repeat the measurement.
13. To test "0" input current apply 0.4V to terminal under test and apply 5.25V to the remaining terminal of that input AND gate. Apply 5.25V to the input terminals of the associated input AND gate.
14. Expander terminals are left electrically open.
15. To test "1" input current apply 4.5V to one input terminal of the input AND gate and apply zero volts to the other input terminal of that input AND gate. Apply 0V to the input terminals of the associated input AND gate.
16. To test output "1" power consumption, apply zero volts to both input terminals of each input AND gate.
17. To test input latch voltage rating, apply 10mA to one input terminal of the input AND gate and apply zero volts to the other input terminal of the input AND gate. Apply zero volts to the input terminals of the associated input AND gate.
18. This test guarantees operation free of input latch-up over the specified operating voltage supply range.
19. Manufacturer reserves the right to make design and process changes and improvements.
20. Apply zero volts to both input terminals of the associated input AND gates.
21. Apply 0.8V to both input terminals of the associated input AND gates.
22. Detailed test conditions for AC testing are in Section 3.







SIGNETICS DCL INTEGRATED CIRCUITS

8848 EXPANDABLE AND-OR-INVERT GATE

The 8848 Expandable AND-OR-INVERT Gate is designed for the highest switching speed while maintaining high fan-out and noise margin.

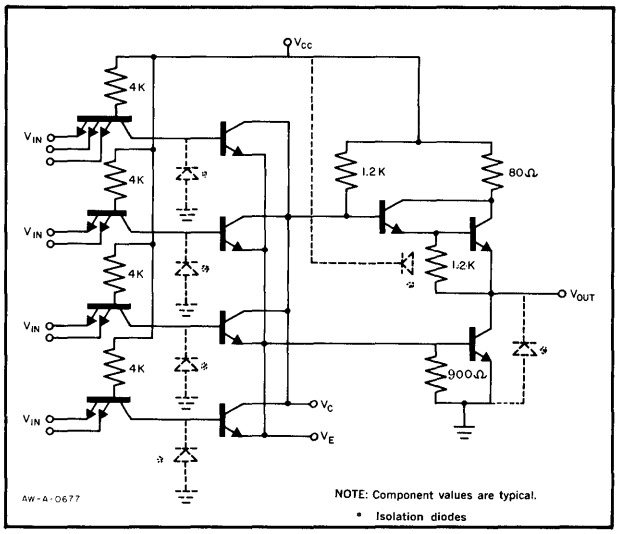
Nodes are provided at the collector and emitter of the second stage. This allows expansion of the number of input AND terms and hence increased system usefulness.

The compatibly characterized 8806 expander is recommended for expansion of the 8848. See correlation table, opposite page.

Low output impedance in the "1" and "0" output states ensures maximum AC noise immunity at the output. General areas of application for the 8848 include half and full adders, digital comparators and AND-OR control logic for inputs to binary clock steering lines.

Detailed usage rules and specific applications are provided in Section 4 of this handbook.

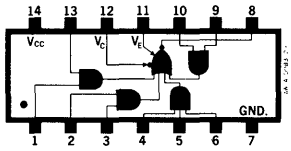
BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 19)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8848	TEMP. N8848	V_{cc}	DRIVEN AND INPUTS	OTHER AND INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V		-500μA	8, 14, 21
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V		-500μA	8, 14, 21
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V		-500μA	8, 14, 21
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V	2.0V	16mA	9, 12, 14
A-3				0.40	V	+25°C	+25°C	5.0V	2.0V	2.0V	16mA	9, 12, 14
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V	2.0V	16mA	9, 12, 14
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.40V			13, 14
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.40V			13, 14
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.40V			13, 14
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		14, 15
A-6	TURN-ON DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O. = 20	10, 22
A-6	TURN-OFF DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O. = 20	10, 22
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C. F.O. = 6	11, 22
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			48.8	mW	+25°C	+25°C	5.25V				
A-2	(Per Gate) OUTPUT "1"			35.7	mW	+25°C	+25°C	5.25V	0V			14, 16
C-1	INPUT LATCH VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	10mA	0V		14, 17, 18
A-2	OUTPUT SHORT CIRCUIT CURRENT	-20		-70	mA	+25°C	+25°C	5.0V	0V		0V	

A PACKAGE



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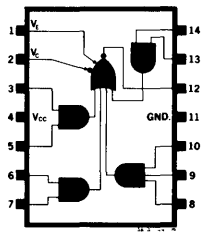


8848

CORRELATION TABLE (8806)

ACCEPTANCE TEST SUB-GROUP	TEST NO.	CHARACTERISTIC	LIMITS				TEST CONDITIONS					
			MIN.	TYP.	MAX.	UNITS	TEMP. S8806 N8806	V_{cc}	V_C	V_E	OUTPUTS	NOTES
A-2	1	"0" INPUT CURRENT AT V_C	-2.2		-3.65	mA	+25°C	4.75V	1.25V			20
A-2	2	TURN-ON VOLTAGE AT V_E			0.85	V	+25°C	4.75V	1.25V	2.5mA	16mA	9, 21
A-2	3	"0" OUTPUT VOLTAGE			0.40	V	+25°C	4.75V	1.25V	2.5mA	16mA	9, 20
A-2	4	"1" OUTPUT VOLTAGE	2.8			V	+25°C	5.0V	-200μA	+500μA	-500μA	8, 21
A-2	5	"1" OUTPUT VOLTAGE	2.8			V	+25°C	5.0V	-200μA	0.59V	-500μA	8, 21

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. 1 AC fan-out is defined as 50pf.
12. To measure "0" output voltage, apply 2.0V to the input terminals of one of the input AND gates and apply zero volts to the input terminals of the associated input AND gates. Reverse the input conditions and repeat the measurement.
13. To test "0" input current apply 0.4V to terminal under test and apply 5.25V to the remaining terminal of that input AND gate. Apply 5.25V to the input terminals of the associated input AND gates.
14. Expander terminals are left electrically open.
15. To test "1" input current apply 4.5V to one input terminal of the input AND gate and apply zero volts to the other input terminal of that input AND gate. Apply 0V to to the input terminals of the associated input AND gates.
16. To test output "1" power consumption, apply zero volts to both input terminals of each input AND gates.
17. To test input latch voltage rating, apply 10mA to one input terminal of the input AND gate and apply zero volts to the other input terminal of the input AND gate. Apply zero volts to the input terminals of the associated input AND gates.
18. This test guarantees operation free of input latch-up over the specified operating voltage supply range.
19. Manufacturer reserves the right to make design and process changes and improvements.
20. Apply zero volts to the input terminals of the associated input AND gates.
21. Apply 0.8V to the input terminals of the associated input AND gates.
22. Detailed test conditions for AC testing are in Section 3.

SIGNETICS DCL INTEGRATED CIRCUITS

8855 DUAL 4-INPUT DRIVER

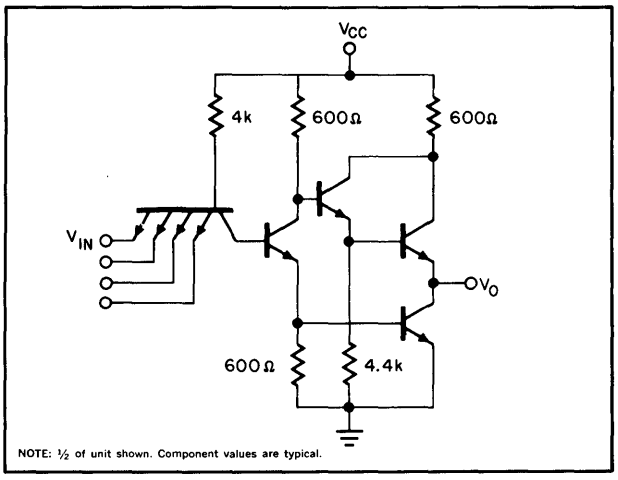
The 8855 is a Dual 4-Input Driver designed specifically for use in applications requiring high fan-out to either AC or DC loads. This device implements the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

An active output structure provides high AC noise immunity due to its low output impedance in both the "1" and "0" output states. This output configuration is particularly suited for driving high capacitive loads such as those encountered in high fan-out situations and line driving applications.

Output short circuit protection is provided by a current limiting resistor.

Section 4 of this handbook provides usage rules and applications information for this element.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

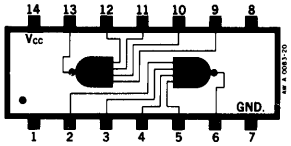
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8855	TEMP. N8855	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V		-1.5mA	8
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V		-1.5mA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V		-1.5mA	8
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V	2.0V	48mA	9
A-3				0.40	V	+25°C	+25°C	5.0V	2.0V	2.0V	48mA	9
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V	2.0V	48mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.40V	5.25V		
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.40V	5.25V		
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.40V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	TURN-ON DELAY			15	ns	+25°C	+25°C	5.0V			D.C. F.O.=60	10,14
A-6	TURN-OFF DELAY			15	ns	+25°C	+25°C	5.0V			D.C. F.O. = 60	10,14
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C. F.O.=10	11,14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION "0"			56.8	mW	+25°C	+25°C	5.25V				
A-2	(Per Gate) "1"			14.7	mW	+25°C	+25°C	5.25V	0V			
C-1	INPUT LATCH VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	10mA	0V		12
A-2	OUTPUT SHORT CIRCUIT CURRENT	-20		-80	mA	+25°C	+25°C	5.0V	0V		0V	

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.

A PACKAGE



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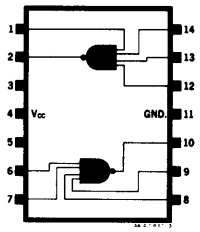
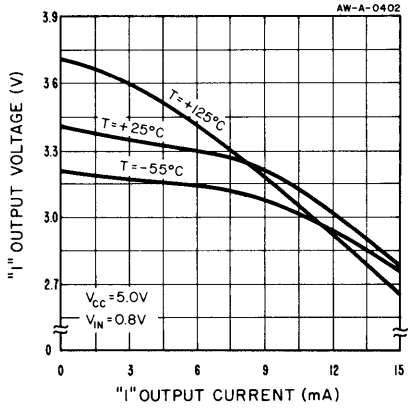
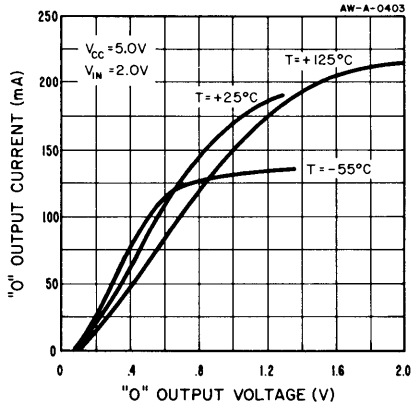
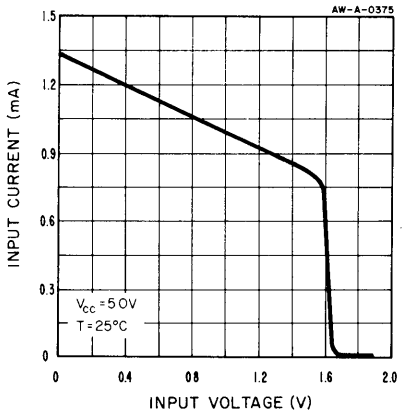


8855







SIGNETICS DCL INTEGRATED CIRCUITS

8881 QUAD 2-INPUT NAND GATE

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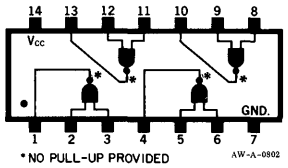

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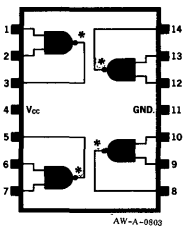
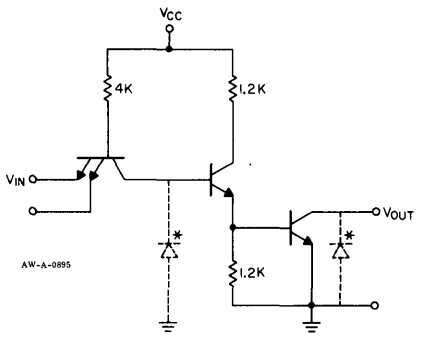


The 8881 is a Quad 2-Input NAND Gate with bare output collectors. Absence of an output pull-up structure allows the user complete freedom in the use of the 8881 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 50 outputs to be tied together.

Collector-logic, using the 8881, can provide increased system flexibility and lower system cost due to reduced can count.

Section 4 of this handbook provides detailed usage rules and collector-logic information for this element.

BASIC CIRCUIT SCHEMATIC



NOTE: 1/4 of unit shown. Component values are typical.
*Isolation diode

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8881	TEMP. N8881	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			25	μA	+125°C	+75°C	5.0V	0.6V			8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V	2.0V	17mA	9
A-3				0.4	V	+25°C	+25°C	5.0V	2.0V	2.0V	17mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	2.0V	17mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.4V	5.25V		
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.4V	5.25V		
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.4V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	TURN-ON DELAY			20	ns	+25°C	+25°C	5.0V			D.C.F.O. = 20	10,14
A-6	TURN-OFF DELAY			30	ns	+25°C	+25°C	5.0V			D.C.F.O. = 20	10,14
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C.F.O. = 6	11,14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			31	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			8.9	mW	+25°C	+25°C	5.25V	0V			
C-1	INPUT LATCH VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	10mA	0V		12

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Connect an external 1K ±1% resistor from V_{cc} to the output terminal for this test.
9. Output sink current is supplied through a resistor V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.

SIGNETICS

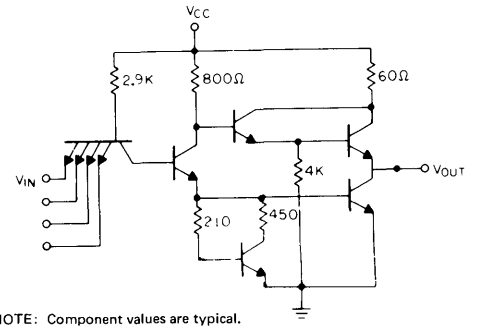
DCL

INTEGRATED CIRCUITS

8H16 DUAL 4-INPUT NAND GATE
8H70 TRIPLE 3-INPUT NAND GATE
8H80 QUAD 2-INPUT NAND GATE

These gate elements are all designed for ultra-high switching speed while maintaining high fan-out and noise margin. All of the 8H00 gates perform the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

The output structure utilizes a totem-pole arrangement which employs a Darlington Pair for active pull-up. This configuration provides extremely low output impedance for the "1" output state. As a result, switching times are relatively insensitive to capacitive loads when compared to single transistor active pull-ups. The saturating output switching transistor provides a low impedance driving source in the output "0" state, enhancing turn-on times and providing high fan-out capability.



NOTE: Component values are typical.

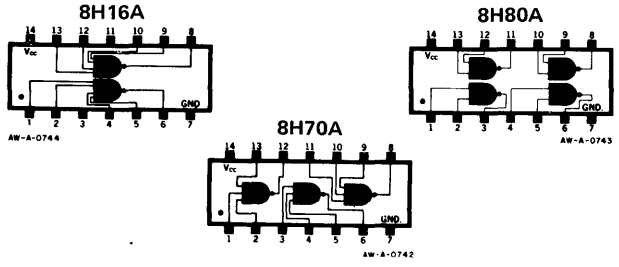
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	LIMITS UNITS	TEST CONDITIONS TEMP. S8H16 S8H70 S8H80	TEST CONDITIONS TEMP. N8H16 N8H70 N8H80	TEST CONDITIONS V_{cc}	TEST CONDITIONS DRIVEN INPUT	TEST CONDITIONS OTHER INPUTS	TEST CONDITIONS OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V		-750μA	8
A-3		2.8			V	+25°C	+25°C	5.00V	0.8V		-750μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V		-750μA	8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V	2.0V	24mA	9
A-3				0.4	V	+25°C	+25°C	5.00V	2.0V	2.0V	24mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	2.0V	24mA	9
C-1	"0" INPUT CURRENT	-0.1		-2.4	mA	-55°C	0°C	5.25V	0.4V	5.25V		
A-3		-0.1		-2.4	mA	+25°C	+25°C	5.25V	0.4V	5.25V		
C-1		-0.1		-2.4	mA	+125°C	+75°C	5.25V	0.4V	5.25V		
A-4	"1" INPUT CURRENT			50	μA	+125°C	+75°C	5.00V	4.5V	0V		
A-6	TURN-ON DELAY		7.0	10	ns	+25°C	+25°C	5.00V			D.C. F.O. = 30	10, 14
	TURN-ON DELAY		5.0		ns	+25°C	+25°C	5.00V			D.C. F.O. = 3	10, 14
A-6	TURN-OFF DELAY		7.0	10	ns	+25°C	+25°C	5.00V			D.C. F.O. = 30	10, 14
	TURN-OFF DELAY		5.0		ns	+25°C	+25°C	5.00V			D.C. F.O. = 3	10, 14
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C F.O. = 6	11, 14
	INPUT CAPACITANCE		2.0		pf	+25°C	+25°C	5.00V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			46.2	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			21	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT LATCH VOLTAGE RATING	6.0			V	+25°C	+25°C	5.00V	10mA	0V		12
A-2	OUTPUT SHORT CIRCUIT CURRENT	-40		-90	mA	+25°C	+25°C	5.00V	0V		0V	

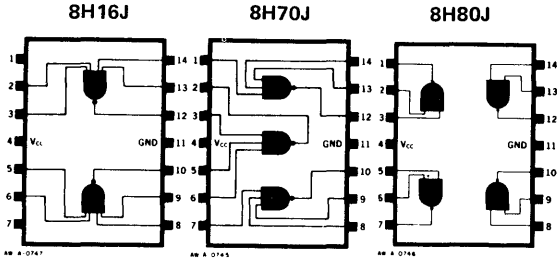
NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV$_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section III.

A PACKAGE



J PACKAGE



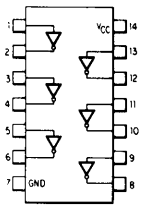
SIGNETICS

DCL

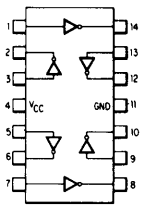
INTEGRATED CIRCUITS

8890 / 8891 HEX INVERTER

A AND F PACKAGE



Q PACKAGE



DESCRIPTION

The 8890 HEX INVERTER provides high switching speed while maintaining high fan-out and noise margin.

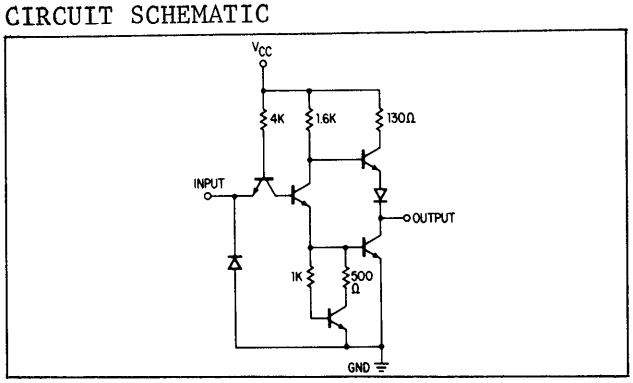
The Totem-Pole output structure provides extremely low output impedance which provides high AC noise immunity. The saturating output switching transistor provides a low impedance driving source in the "0" output state enhancing turn-on times and providing high fan-out capability.

Output short-circuit protection is provided by a current limiting resistor.

The 8891 HEX INVERTER provides high switching speed while maintaining high fan-out and noise margin.

The bare collector output allows collector logic (WIRED-AND) to be easily implemented.

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (NOTES: 1,2,3,4,5, & 10)

8890

ACCEPTANCE TEST SUBGROUP	CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
		MIN	TYP	MAX	UNIT	TEMP °C S	TEMP °C N	V_{cc} (Volts)	DRIVEN INPUT	OUTPUTS	
A-5	"1" Output Voltage	2.6	–	–	V	-55	0	4.75	0.8V	-500μA	6
A-3		2.8	–	–	V	+25	+25	5.00	0.8V	-500μA	6
A-4		2.6	–	–	V	+125	+75	4.75	0.8V	-500μA	6
A-5	"0" Output Voltage	–	–	0.4	V	-55	0	4.75	2.0V	16mA	7
A-3		–	–	0.4	V	+25	+25	5.00	2.0V	16mA	7
A-4		–	–	0.4	V	+125	+75	4.75	2.0V	16mA	7
C-1	"0" Input Current	-0.1	–	-1.6	mA	-55	0	5.25	0.4V	–	–
A-3		-0.1	–	-1.6	mA	+25	+25	5.25	0.4V	–	–
C-1		-0.1	–	-1.6	mA	+125	+75	5.25	0.4V	–	–
A-4	"1" Input Current	–	–	25	μA	+125	+75	5.00	4.5V	–	–
A-6	Turn-On Delay	–	–	15	ns	+25	+25	5.00	–	DCFO = 20	8, 13
A-6	Turn-Off Delay	–	–	22	ns	+25	+25	5.00	–	DCFO = 20	8, 13
C-2	Output Fall Time	–	–	50	ns	-55	0	4.75	–	ACFO = 6	9, 13
A-2	Power/Current Consumption Per Inverter: Output "0"	–	–	31/6	mW/mA	+25	+25	5.25	–	–	–
A-2	Per Inverter: Output "1"	–	–	9/1.7	mW/mA	+25	+25	5.25	0V	–	–
A-2	Input Latch Voltage	6.0	–	–	V	+25	+25	5.00	10mA	–	11
A-2	Output Short Circuit Current	-20	–	-70	mA	+25	+25	5.00	0V	0V	–
A-2	Input Clamp Voltage	–	–	-1.5	V	+25	+25	5.00	-12mA	–	–

8891

A-4	"1" Output Leakage Current	–	–	250	μA	+125	+75	5.00	0.8V	–	12
A-5	"0" Output Voltage	–	–	0.4	V	-55	0	4.75	2.0V	16mA	7
A-3		–	–	0.4	V	+25	+25	5.00	2.0V	16mA	7
A-4		–	–	0.4	V	+125	+75	4.75	2.0V	16mA	7
C-1	"0" Input Current	-0.1	–	-1.6	mA	-55	0	5.25	0.4V	–	–
A-3		-0.1	–	-1.6	mA	+25	+25	5.25	0.4V	–	–
C-1		-0.1	–	-1.6	mA	+125	+75	5.25	0.4V	–	–
A-4	"1" Input Current	–	–	25	μA	+125	+75	5.00	4.5V	–	–
A-6	Turn-On Delay	–	–	15	ns	+25	+25	5.00	–	DCFO = 20	8, 13
A-6	Turn-Off Delay	–	–	45	ns	+25	+25	5.00	–	DCFO = 20	8, 13
A-2	Power Current Consumption Per Inverter: Output "0"	–	–	31/6	mW/mA	+25	+25	5.25	–	–	–
	Per Inverter:Output "1"	–	–	9/1.7	mW/mA	+25	+25	5.25	0V	–	–
A-2	Input Latch Voltage	6.0	–	–	V	+25	+25	5.00	10mA	–	11
A-2	Input Clamp Voltage	–	–	-1.5	V	+25	+25	5.00	-12mA	–	–

SIGNETICS DCL INTEGRATED CIRCUITS

8H20 DUAL J-K BINARY ELEMENT
8H21 DUAL J-K BINARY ELEMENT
8H22 DUAL J-K BINARY ELEMENT

The 8H20 is a high speed J-K Binary which uses stored charge techniques to effect the toggling action. This type of clocking technique provides all the advantages of level sensitive binaries and retains all the speed/power advantages of rate sensitive binaries. This binary is designed to toggle at frequencies from near DC to greater than 50MHz.

The change of state is caused by the negative logic transition of the clock input and is effectively carried out with a clock pulse width of 7ns minimum and up to a maximum 200ns fall time.

There is no hold time requirement for the inputs. This means that logic transistions to a logic "1" or "0" can occur coincidentally with the logic "1" transition of the clock input.

The logic states of the J and K inputs must be stable when the clock input reaches 2.0V. These must remain stable until the clock falls if maximum utilization of the binary speed is desired.

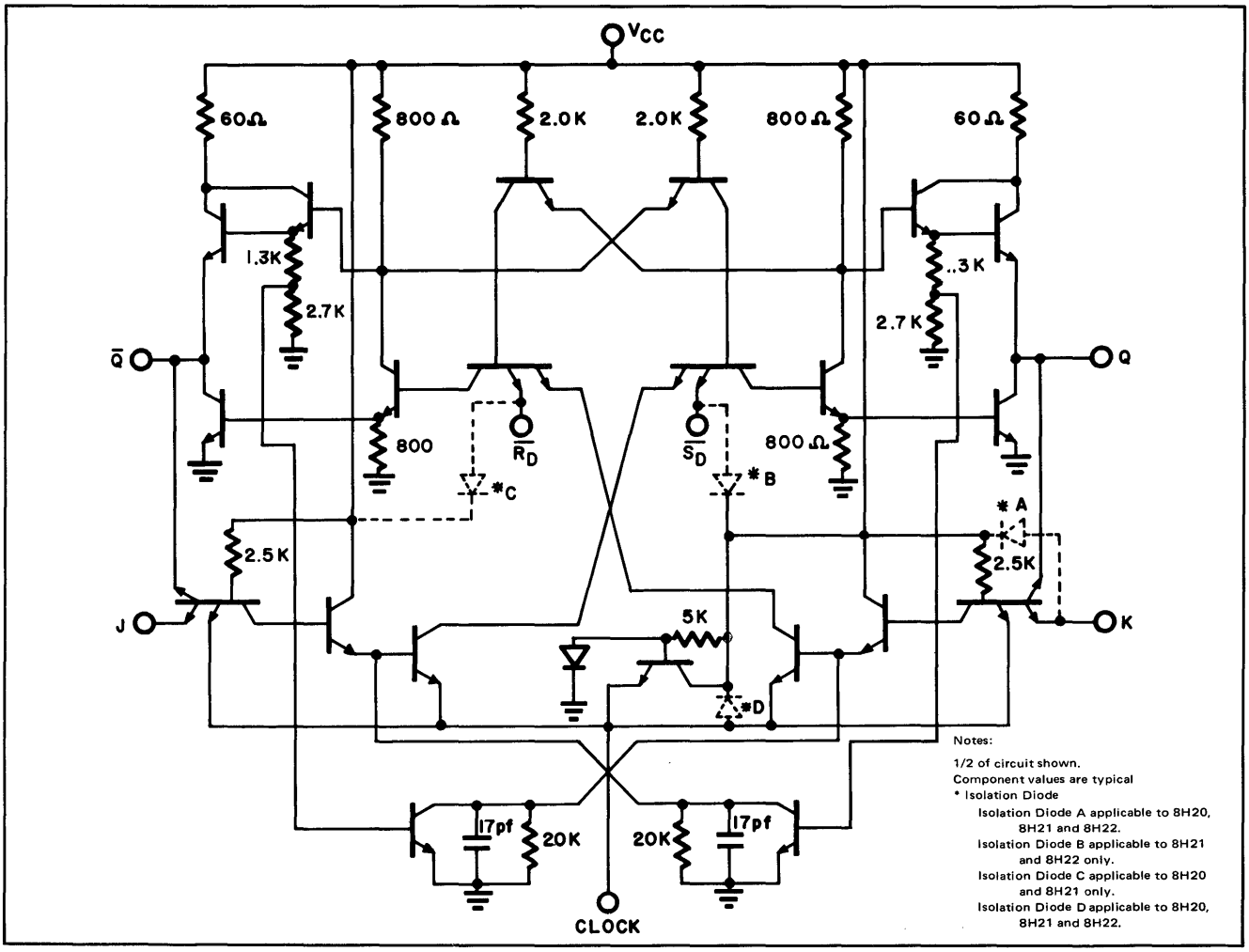
Clocking transitions should be avoided when the asynchronous lines are activated and the J and K inputs are at logic "1" levels. If this condition exists, a positive transient will be generated on the output which is normally at the logic "0" state. The duration of this transient may be about 20ns.

The 8H21 features common clock and common $\overline{R}_D$ lines.

The 8H22 provides separate inputs for clock, J, K, $\overline{R}_D$ and $\overline{S}_D$ on each binary and is available only in the 16-pin dual-in-line package.

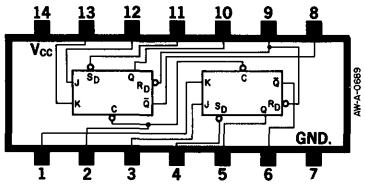
Applications information and usage rules for these devices are included in Section 4 of this handbook.

BASIC CIRCUIT SCHEMATIC



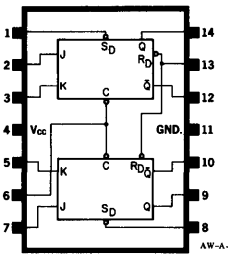
A, F PACKAGE

8H21A

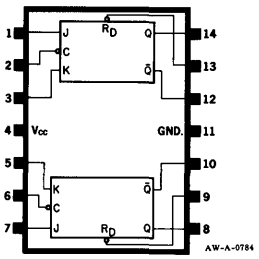


(8H22B package on next page)

8H21Q Q PACKAGES



8H20Q



8H20
8H21
8H22

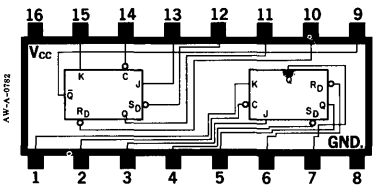
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 14)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS									
		MIN.	TYP.	MAX.	UNITS	TEMP. S8H21 S8H22 S8H20	TEMP. N8H21 N8H22 N8H20	V_{cc}	$\overline{R}_D$	$\overline{S}_D$	J	K	CLOCK	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE (Q)	2.6	3.0		V	-55°C	0°C	4.75V	2.0V	0.8V	2.0V	0.8V	PULSE	1.0mA	7, 10, 17
A-3		2.8	3.2		V	+25°C	+25°C	5.0V	2.0V	0.8V	2.0V	0.8V	PULSE	1.0mA	7, 10, 17
A-4		2.6	3.0		V	+125°C	+75°C	4.75V	2.0V	0.8V	2.0V	0.8V	PULSE	1.0mA	7, 10, 17
A-5	"1" OUTPUT VOLTAGE ($\overline{Q}$)	2.6	3.0		V	-55°C	0°C	4.75V	0.8V	2.0V				1.0mA	7
A-3		2.8	3.2		V	+25°C	+25°C	5.0V	0.8V	2.0V				1.0mA	7
A-4		2.6	3.0		V	+125°C	+75°C	4.75V	0.8V	2.0V				1.0mA	7
A-5	"0" OUTPUT VOLTAGE (Q)		0.3	0.4	V	-55°C	0°C	4.75V	0.8V	2.0V				24mA	8
A-3			0.3	0.4	V	+25°C	+25°C	5.0V	0.8V	2.0V				24mA	8
A-4			0.3	0.4	V	+125°C	+75°C	4.75V	0.8V	2.0V				24mA	8
A-5	"0" OUTPUT VOLTAGE ($\overline{Q}$)		0.3	0.4	V	-55°C	0°C	4.75V	2.0V	0.8V	2.0V	0.8V	PULSE	24mA	8, 10, 17
A-3			0.3	0.4	V	+25°C	+25°C	5.0V	2.0V	0.8V	2.0V	0.8V	PULSE	24mA	8, 10, 17
A-4			0.3	0.4	V	+125°C	+75°C	4.75V	2.0V	0.8V	2.0V	0.8V	PULSE	24mA	8, 10, 17
	"0" INPUT CURRENT														
C-1	(CLOCK, 8H21 only)	-0.1		-4.8	mA	-55°C	0°C	5.25V			5.25V	5.25V	0.4V		
A-3		-0.1		-4.8	mA	+25°C	+25°C	5.25V			5.25V	5.25V	0.4V		
C-1		-0.1		-4.8	mA	+125°C	+75°C	5.25V			5.25V	5.25V	0.4V		
C-1	(CLOCK, 8H20 and 8H22 only)	-0.1		-2.4	mA	-55°C	0°C	5.25V			5.25V	5.25V	0.4V		
A-3		-0.1		-2.4	mA	+25°C	+25°C	5.25V			5.25V	5.25V	0.4V		
C-1		-0.1		-2.4	mA	+125°C	+75°C	5.25V			5.25V	5.25V	0.4V		
C-1	(J)	-0.1		-2.4	mA	-55°C	0°C	5.25V	0V	5.25V	0.4V	5.25V	5.25V	$\overline{Q}/\overline{Q}$ = "1"	
A-3		-0.1		-2.4	mA	+25°C	+25°C	5.25V	0V	5.25V	0.4V	5.25V	5.25V	$\overline{Q}/\overline{Q}$ = "1"	
C-1		-0.1		-2.4	mA	+125°C	+75°C	5.25V	0V	5.25V	0.4V	5.25V	5.25V	$\overline{Q}$ = "1"	
C-1	(K)	-0.1		-2.4	mA	-55°C	0°C	5.25V	5.25V	0V	5.25V	0.4V	5.25V	Q = "1"	10
A-3		-0.1		-2.4	mA	+25°C	+25°C	5.25V	5.25V	0V	5.25V	0.4V	5.25V	Q = "1"	10
C-1		-0.1		-2.4	mA	+125°C	+75°C	5.25V	5.25V	0V	5.25V	0.4V	5.25V	Q = "1"	10
C-1	($\overline{R}_D$ 8H21 only)	-0.1		-4.8	mA	-55°C	0°C	5.25V	0.4V	0V			5.25V		
A-3		-0.1		-4.8	mA	+25°C	+25°C	5.25V	0.4V	0V			5.25V		
C-1		-0.1		-4.8	mA	+125°C	+75°C	5.25V	0.4V	0V			5.25V		
C-1	($\overline{R}_D$ 8H22 only)	-0.1		-2.4	mA	-55°C	0°C	5.25V	0.4V	0V			5.25V		
A-3		-0.1		-2.4	mA	+25°C	+25°C	5.25V	0.4V	0V			5.25V		
C-1		-0.1		-2.4	mA	+125°C	+75°C	5.25V	0.4V	0V			5.25V		
C-1	($\overline{R}_D$ 8H20 only)			-2.4	mA	-55°C	0°C	5.25V	0.4V				5.25V		
A-3				-2.4	mA	+25°C	+25°C	5.25V	0.4V				5.25V		
C-1				-2.4	mA	+125°C	+75°C	5.25V	0.4V				5.25V		
C-1	($\overline{S}_D$ 8H21 and 8H22 only)	-0.1		-2.4	mA	-55°C	0°C	5.25V	0V	0.4V			5.25V		
A-3		-0.1		-2.4	mA	+25°C	+25°C	5.25V	0V	0.4V			5.25V		
C-1		-0.1		-2.4	mA	+125°C	+75°C	5.25V	0V	0.4V			5.25V		
	"1" INPUT CURRENT														
A-4	(J)			50	μA	+125°C	+75°C	5.0V			4.5V		0.4V		
A-4	(K)			50	μA	+125°C	+75°C	5.0V				4.5V	0.4V		
A-4	($\overline{R}_D$ 8H21 only)			100	μA	+125°C	+75°C	5.0V	4.5V	0V			0.4V	$\overline{Q}$ = "0"	
A-4	($\overline{R}_D$ 8H20 and 8H22 only)			50	μA	+125°C	+75°C	5.0V	4.5V	0V				$\overline{Q}$ = "0"	10
A-4	($\overline{S}_D$ 8H21 and 8H22 only)			50	μA	+125°C	+75°C	5.0V	0V	4.5V				Q = "0"	
A-4	(CLOCK 8H21 only)			400	μA	+125°C	+75°C	5.0V			0V	0V	4.5V		
A-4	(CLOCK 8H20 and 8H22 only)			200	μA	+125°C	+75°C	5.0V			0V	0V	4.5V		
	INPUT LATCH VOLTAGE RATING														
C-1	(CLOCK 8H21 only)	6.0			V	+25°C	+25°C	5.5V			0V	0V	10mA		12
C-1	(CLOCK 8H20 and 8H22 only)	6.0			V	+25°C	+25°C	5.5V		0V	0V	0V	10mA		12
C-1	(J)	6.0			V	+25°C	+25°C	5.5V		0V	10mA		0.4V		12
C-1	(K)	6.0			V	+25°C	+25°C	5.5V	0V			10mA	0.4V		12
C-1	($\overline{R}_D$ 8H21 only)	6.0			V	+25°C	+25°C	5.5V	10mA				0.4V	$\overline{Q}$ = "0"	10
C-1	($\overline{R}_D$ 8H20 and 8H22 only)	6.0			V	+25°C	+25°C	5.5V	10mA				0.4V	$\overline{Q}$ = "0"	10
C-1	($\overline{S}_D$ 8H21 and 8H22 only)	6.0			V	+25°C	+25°C	5.5V	0V	10mA			0.4V	Q = "0"	
	OUTPUT SHORT CIRCUIT CURRENT														
A-2	(Q)	-40		-90	mA	+25°C	+25°C	5.0V		0V				0V	11
A-2	($\overline{Q}$)	-40		-90	mA	+25°C	+25°C	5.0V	0V					0V	11
A-2	POWER CONSUMPTION (Per Binary)		65	90	mW	+25°C	+25°C	5.25V			0V	0V			
	TURN-ON DELAY														
	(CLOCK to Q, $\overline{Q}$)		10		ns	+25°C	+25°C	5.0V						D.C.F.O. = 30	9, 13
	($\overline{R}_D$ to Q)		10		ns	+25°C	+25°C	5.0V						D.C.F.O. = 30	9, 13
	($\overline{S}_D$ to $\overline{Q}$)		10		ns	+25°C	+25°C	5.0V						D.C.F.O. = 30	9, 13
	TURN-OFF DELAY														
	(CLOCK to Q, $\overline{Q}$)		8		ns	+25°C	+25°C	5.0V						D.C.F.O. = 30	9, 13
	($\overline{R}_D$ to $\overline{Q}$)		8		ns	+25°C	+25°C	5.0V						D.C.F.O. = 30	9, 13
	($\overline{S}_D$ to Q)		8		ns	+25°C	+25°C	5.0V						D.C.F.O. = 30	9, 13
A-6	TOGGLE RATE	50	75		MHz	+25°C	+25°C	5.0V						D.C.F.O. = 3	9, 13
C-2	MINIMUM CLOCK PULSE WIDTH		3.0	7	ns	+25°C	+25°C	5.0V						D.C.F.O = 3	9, 13
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V						A.C.F.O. = 6	13, 15
	INPUT CAPACITANCE														
C-2	J, K			3.0	pf	+25°C	+25°C	5.0V			2.0V	2.0V			16
C-2	$\overline{S}_D$ (8H21, 8H22)			3.0	pf	+25°C	+25°C	5.0V		2.0V					16
C-2	$\overline{R}_D$ (8H20, 8H22)			3.0	pf	+25°C	+25°C	5.0V	2.0V						16
C-2	C (8H20, 8H22)			3.0	pf	+25°C	+25°C	5.0V					2.0V		16
C-2	C, $\overline{R}_D$ (8H21)			6.0	pf	+25°C	+25°C	5.0V	2.0V				2.0V		16
	CLOCK MODE SWITCHING TEST		200		ns	+25°C	+25°C	5.0V					PULSE		

8H20
8H21
8H22

B PACKAGE

8H22B



8H20			8H21 and 8H22					
J_n	K_n	Q_{n+1}	J_n	K_n	Q_{n+1}	$\overline{S}_D$	$\overline{R}_D$	Q
0	0	Q_n	0	0	Q_n	0	0	†
1	0	1	1	0	1	1	0	0
0	1	0	0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	$\overline{Q}_n$	1	1	Q

$\overline{R}_D = 0 \Rightarrow Q = 0$

† Not Allowed

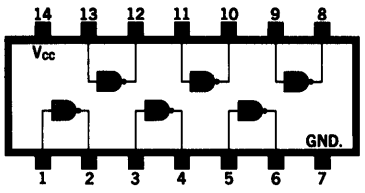
Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. One DC fan-out is defined as the input of an 8480 or 0.8mA.
10. When testing the 8H20, apply a clock pulse prior to measurement to ensure Q = "1" and $\overline{Q}$ = "0". Clock pulse characteristics are: PW = 100ns; Pulse Amplitude = 3.0V; t_r = 10ns; t_f = 10ns.
11. For output short circuit current, test one output at a time. For 8H20, test $\overline{Q}$ only.
12. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
13. Detailed test conditions for AC testing are in Section 3.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. One AC fan-out is defined as 50pf.
16. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
17. Conditions shown under J, K, and Clock apply to S/N8H20 only.

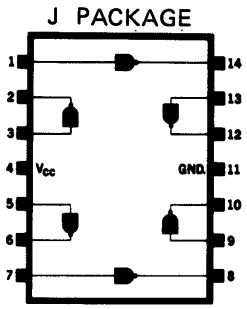
SIGNETICS DCL INTEGRATED CIRCUITS

8H90 HEX INVERTER

A PACKAGE



J PACKAGE



The 8H90 Hex Inverter is designed for ultra-high switching speed while maintaining high fan-out and noise margin.

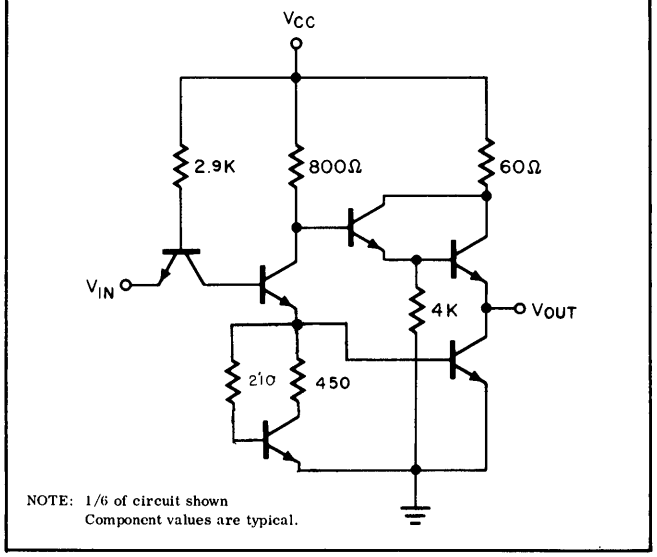
The output structure utilizes a totem-pole arrangement which employs a Darlington Pair for active pull-up. This configuration provides extremely low output impedance for the "1" output state. As a result, switching times are relatively insensitive to capacitive loads when compared to single transistor active pull-ups. The saturating output switching transistor provides a low impedance driving source in the output "0" state, enhancing turn-on times and providing high fan-out capability.

Because of the low output impedance of this element, it exhibits high AC noise immunity at the output which is extremely important in high speed systems in eliminating erroneous cross-coupled signals.

Output short circuit protection is provided by a current limiting resistor.

(Package drawings are on the reverse side.)

BASIC CIRCUIT SCHEMATIC



NOTE: 1/6 of circuit shown
Component values are typical.

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	LIMITS UNITS	TEST CONDITIONS TEMP. S8H16 S8H70 S8H80	TEST CONDITIONS TEMP. N8H16 N8H70 N8H80	TEST CONDITIONS V_{cc}	TEST CONDITIONS DRIVEN INPUT	TEST CONDITIONS OTHER INPUTS	TEST CONDITIONS OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V		-750μA	8
A-3		2.8			V	+25°C	+25°C	5.00V	0.8V		-750μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V		-750μA	8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V		24mA	9
A-3				0.4	V	+25°C	+25°C	5.00V	2.0V		24mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V		24mA	9
C-1	"0" INPUT CURRENT	-0.1		-2.4	mA	-55°C	0°C	5.25V	0.4V			
A-3		-0.1		-2.4	mA	+25°C	-25°C	5.25V	0.4V			
C-1		-0.1		-2.4	mA	+125°C	+75°C	5.25V	0.4V			
A-4	"1" INPUT CURRENT			50	μA	+125°C	+75°C	5.00V	4.5V			
	TURN-ON DELAY		7.0		ns	+25°C	+25°C	5.00V			D.C. F.O. = 30	10,14
	TURN-ON DELAY		5.0		ns	+25°C	+25°C	5.00V			D.C. F.O. = 3	10,14
	TURN-OFF DELAY		7.0		ns	+25°C	+25°C	5.00V			D.C. F.O. = 30	10,14
	TURN-OFF DELAY		5.0		ns	+25°C	+25°C	5.00V			D.C. F.O. = 3	10,14
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C F.O. = 6	11,14
	INPUT CAPACITANCE		2.0		pf	+25°C	+25°C	5.00V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			46.2	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			21.0	mW	+25°C	+25°C	5.25V	0V			
C-1	INPUT LATCH VOLTAGE RATING	6.0			V	+25°C	+25°C	5.00V	10mA			12
A-2	OUTPUT SHORT CIRCUIT CURRENT	-40		-90	mA	+25°C	+25°C	5.00V	0V		0V	

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV$_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Test conditions for AC testing are the same as for 8H80. See Section 3 of Signetics DCL Handbook.

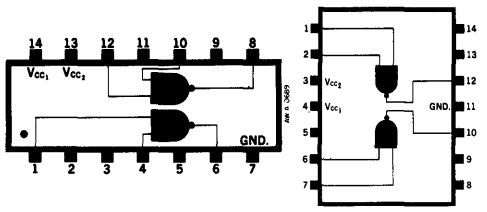
SIGNETICS

DCL

INTEGRATED CIRCUITS

8T18 DUAL 2-INPUT NAND INTERFACE GATE

A PACKAGE J PACKAGE



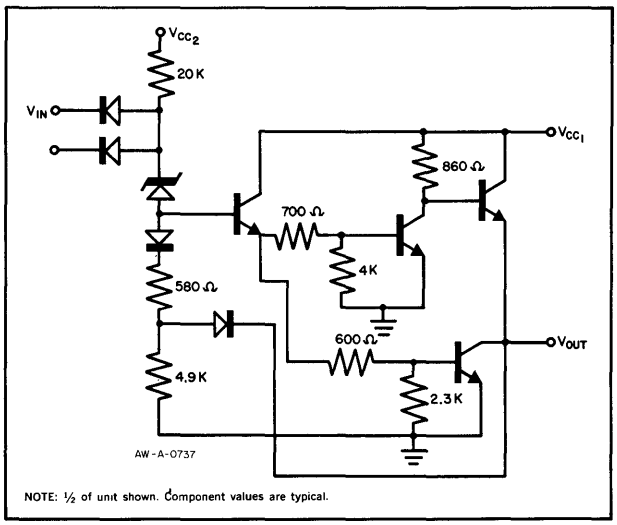
BASIC CIRCUIT SCHEMATIC

The 8T18 is a Dual 2-Input NAND Interface Gate. It is a high to low voltage interface gate which provides translation from up to 30-volt logic levels to standard logic levels of 5 volts.

The basic gate operates from two power supplies. The input structure functions from a high voltage supply between 20V and 30V and the second stage transistors and output structure operate from a standard 5V power supply.

The output structure features active pull-up and pull-down, providing a low impedance driving source in both "1" and "0" output states. This configuration is particularly suited for driving the high capacitance loads encountered in high fan-out and line driving applications.

Section 4 provides usage rules and applications information for the 8T18.



NOTE: ½ of unit shown. Component values are typical.

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS							
		MIN.	TYP.	MAX.	UNITS	TEMP. S8T18	TEMP. N8T18	V_{cc_1}	V_{cc_2}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	3.4			V	-55°C	0°C	4.75V	24.0V	6.5V		-225μA	7
A-3		3.6			V	+25°C	+25°C	5.00V	24.0V	6.5V		-225μA	7
A-4		3.4			V	+125°C	+75°C	4.75V	24.0V	6.5V		-225μA	7
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	20.0V	9.0V	9.0V	7.2mA	8
A-3				0.35	V	+25°C	+25°C	5.00V	20.0V	9.0V	9.0V	7.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	20.0V	9.0V	9.0V	7.2mA	8
A-5	"0" INPUT CURRENT	-0.1		-1.8	mA	-55°C	0°C	5.25V	24.0V	0.35V	30V		
A-3		-0.1		-1.8	mA	+25°C	+25°C	5.25V	24.0V	0.35V	30V		
C-1		-0.1		-1.8	mA	+125°C	+75°C	5.25V	24.0V	0.35V	30V		
A-4	"1" INPUT CURRENT			50	μA	+125°C	+75°C	5.00V	24.0V	30V	0V		
A-6	TURN-ON DELAY		12	20	ns	+25°C	+25°C	5.00V	24.0V			D.C. F.O. = 9	9,11
A-6	TURN-OFF DELAY		35	70	ns	+25°C	+25°C	5.00V	24.0V			D.C. F.O. = 9	9,11
C-2	OUTPUT FALL TIME			75	ns	-55°C	0°C	4.75V	24.0V			A.C F.O. = 2	10,11
A-2	POWER CONSUMPTION (V_{cc_1} OUTPUT "0") (Per Gate)			44.0	mW	+25°C	+25°C	5.25V	24.0V				
	(V_{cc_1} OUTPUT "1")			1.0	mW	+25°C	+25°C	5.25V	24.0V	0V			
	(V_{cc_2} OUTPUT "0")			38.4	mW	+25°C	+25°C	5.25V	24.0V				
	(V_{cc_2} OUTPUT "1")			37.2	mW	+25°C	+25°C	5.25V	24.0V	0V			
A-2	INPUT VOLTAGE RATING	50			V	+25°C	+25°C	5.00V	24.0V	100μA	0V		
	OUTPUT SHORT CIRCUIT CURRENT		-75		mA	+25°C	+25°C	5.00V	24.0V	0V		0V	

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Detailed test conditions for AC testing are in Section 3.

SIGNETICS DCL INTEGRATED CIRCUITS

8T80 QUAD 2-INPUT NAND INTERFACE GATE
8T90 HEX INVERTER INTERFACE ELEMENT

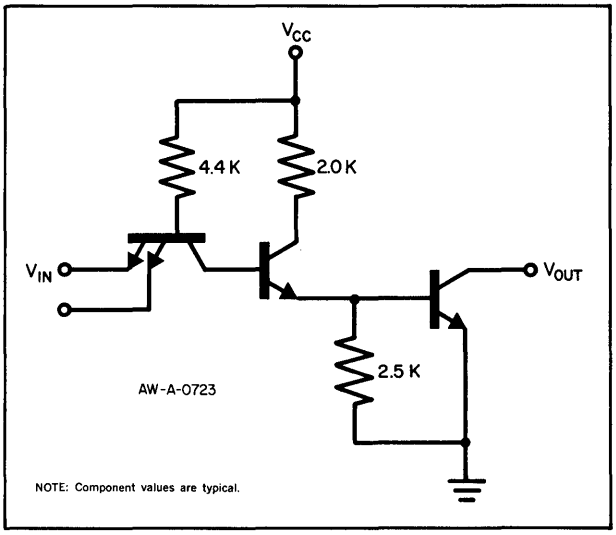
The 8T80 Quad 2-Input NAND Interface Gate and the 8T90 Hex Inverter Interface Element are low to high voltage elements which provide translation from standard logic levels of 5 volts to voltage levels of up to 30 volts.

The 8T80 performs the NAND function for positive logic (highest voltage level = "1") and the 8T90 performs the inverting function.

The output structure of each element features a high voltage transistor with bare collector which allows logic swings up to 30 volts. The bare collector allows collector logic or wired-AND to be easily implemented.

Usage and applications information for these devices is included in Section 4 of this handbook.

BASIC CIRCUIT SCHEMATIC



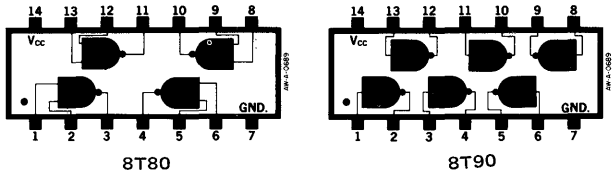
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 10, 12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8T80 S8T90	TEMP. N8T80 N8T90	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			100	μA	+125°C	+75°C	5.0V	0.6V			7
A-5	"0" OUTPUT VOLTAGE			1.0	V	-55°C	0°C	4.75V	2.0V	2.0V	20mA	8
A-3				1.0	V	+25°C	+25°C	5.0V	2.0V	2.0V	20mA	8
A-4				1.0	V	+125°C	+75°C	4.75V	2.0V	2.0V	20mA	8
C-1	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	8,9
C-1				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	8,9
C-1				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	8,9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	TURN-ON DELAY		35	55	ns	+25°C	+25°C	5.0V				13
A-6	STORAGE TIME		40	95	ns	+25°C	+25°C	5.0V				13
A-2	POWER CONSUMPTION OUTPUT "0"			20.0	mW	+25°C	+25°C	5.25V				
A-2	(Per Gate) OUTPUT "1"			7.9	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT VOLTAGE RATING	40			V	+25°C	+25°C	5.0V	0V			11

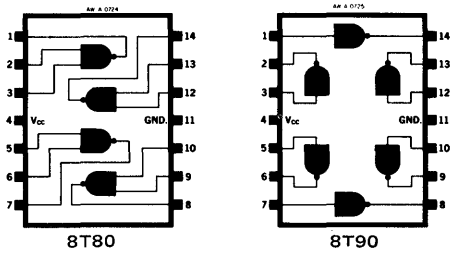
Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output leakage current is supplied through a 2KΩ resistor to 30V.
8. Output sink current is supplied through a resistor to 30V.
9. This test applies to 8T90 only.
10. "OTHER INPUTS" applies to 8T80 only.
11. For this test, connect a 2KΩ resistor from output under test to 41V and a 10pf capacitor from output to ground.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.

A PACKAGE



J PACKAGES



SECTION 3-AC TESTING

Verification of the AC parameters guaranteed in the Electrical Characteristics tables in Section 2 can be obtained by using the test circuits and loading conditions specified in this section. The test circuit and loading conditions appropriate to each device in the 8000-series can be determined from Table 3-1. Please note that the test limits guaranteed apply only when the specific circuits and loading conditions indicated in this section are used.

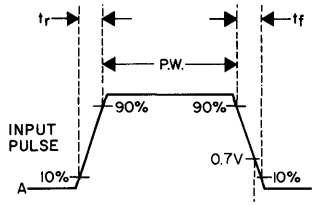
TABLE 3-1 – AC TEST CIRCUITS AND LOADING INFORMATION

ELEMENT	T_{ON} - T_{OFF}							PAIR DELAY					TOGGLE RATE	OUTPUT FALL TIME		SWITCHING AND HOLDING LEVEL
	FIG. NO.	LOADING VALUES						FIG. NO	LOADING VALUES				FIGURE NUMBER	FIG. NO.	LOADING VALUES	FIGURE NUMBER
		T_{ON}			T_{OFF}											
		R1	R2	C1	R1	R2	C1		R1	R2	C1	C2			C1	
8162	2J	NOTE 4												5A	150	
8415	2B	11K	210	27	11K	1.91K	18	1B	15K	210	47	44		5B	100	
8416	2A	16K	210	27	16K	1.91K	18	1A	15K	210	47	44		5C	100	
8417	2B	11K	210	27	11K	1.91K	18	1B	15K	210	47	44		5B	100	
8424	2K	16K	226	24	16K	1.91K	18						4A	5F	100	3A
8425	2K	16K	226	24	16K	1.91K	18						4A	5F	100	3A
8440	2C	16K	210	27	16K	1.91K	18	1C	15K	210	47	44		5D	100	
8455	2A	5K	70	75	5K	1.91K	18	1A	5K	70	95	92		5C	450	
8470	2A	16K	210	27	16K	1.91K	18	1A	15K	210	47	44		5C	100	
8471	2B	11K	210	27	11K	1.91K	18	1B	15K	210	47	44		5B	100	
8480/90	2A	16K	210	27	16K	1.91K	18	1A	15K	210	47	44		5C	100	
8481	2B	11K	210	27	11K	1.91K	18	1B	15K	210	47	44		5B	100	
8806	2D	5K	84.5	30	5K	84.5	30									
8808	2A	5K	84.5	30	5K	84.5	30							5C	300	
8815	2A	5K	84.5	30	5K	84.5	30							5C	300	
8816	2A	5K	84.5	30	5K	84.5	30							5C	300	
8821	2P	5K	84.5	30	5K	84.5	30						4D	5G	300	
8822	2P	5K	84.5	30	5K	84.5	30						4B	5G	300	

TABLE 3-1 – AC TEST CIRCUITS AND LOADING INFORMATION (Cont.)

ELEMENT	T_{ON} - T_{OFF}							PAIR DELAY		TOGGLE RATE	OUTPUT FALL TIME		SWITCHING AND HOLDING LEVEL
	FIG. NO.	LOADING VALUES						FIG. NO.	LOADING VALUES	FIGURE NUMBER	FIG. NO.	LOADING VALUES	FIGURE NUMBER
		T_{ON}			T_{OFF}								
		R1	R2	C1	R1	R2	C1					C1	
8824	2P	5K	84.5	30	5K	84.5	30			4B	5G	300	
8825	2F	5K	84.5	30	5K	84.5	30			4E	5G	300	
8826	2G	5K	169	18	5K	169	18			4B	5G	100	3A
8827	2G	5K	169	18	5K	169	18			4D	5G	100	3A
8828	2I	5K	84.5	30	5K	84.5	30				5H	300	
8829	2H	5K	84.5	30	5K	84.5	30			4E	5G	300	
8840	2C	5K	84.5	30	5K	84.5	30				5D	300	
8848	2M	5K	84.5	30	5K	84.5	30				5E	300	
8855	2A	5K	24.9	90	5K	24.9	90				5C	500	
8870	2A	5K	84.5	30	5K	84.5	30				5C	300	
8875	2A	5K	84.5	30	5K	84.5	30				5C	300	
8880	2A	5K	84.5	30	5K	84.5	30				5C	300	
8881	2B	1M	84.5	30	1M	84.5	30				5B	300	
8885	2A	5K	84.5	30	5K	84.5	30				5C	300	
8H16	2A	5K	56	18	5K	56	18				5C	300	
8H20	2G	1.6K	56	18	1.6K	56	18			4D	5G	300	
8H21	2G	1.6K	56	18	1.6K	56	18			4D	5G	300	
8H22	2G	1.6K	56	18	1.6K	56	18			4D	5G	300	
8H70	2A	5K	56	18	5K	56	18				5C	300	
8H80	2A	5K	56	18	5K	56	18				5C	300	
8T18	2L	16K	210	27	16K	210	27				5I	100	
8T80	2E	Open	1.43K	30	NOTE 5								
8T90	2E	Open	1.43K	30	NOTE 5								

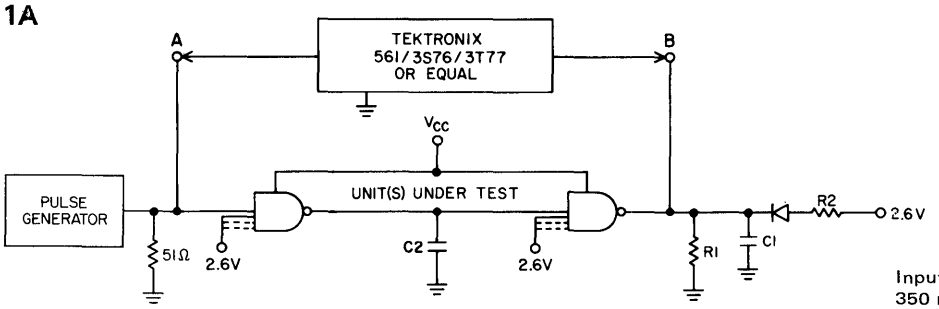
FIGURE A – MEASURING POINTS: t_r, t_f and PW

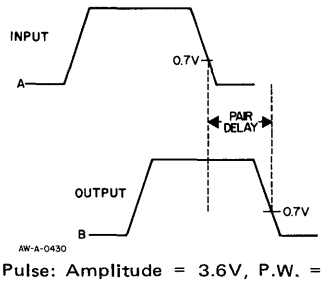


NOTE: Input pulse notations apply thru this section unless otherwise specified.

FIGURE 1 – PAIR DELAY

1A

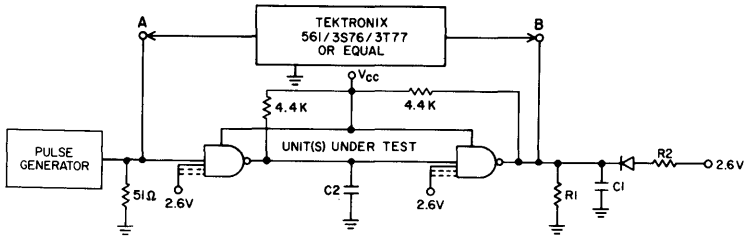




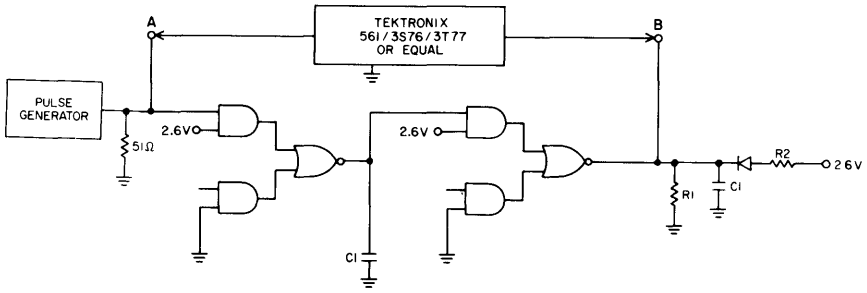
Input Pulse: Amplitude = 3.6V, P.W. = 350 ns, $t_r = t_f = 10$ ns.

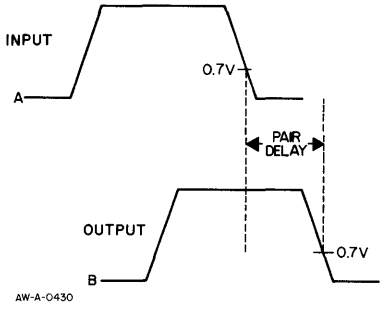
Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.
4. Fig. 2J also contains pulse width test conditions.
5. Fig. 2E also contains storage time test conditions.

1B



1C

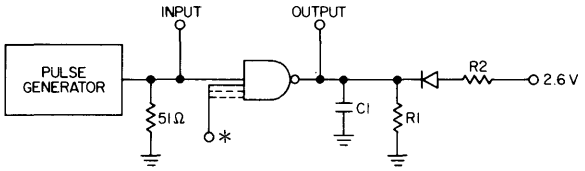




Input Pulse: Amplitude = 3.6V, P.W. = 350 ns, t_r = t_f = 10 ns.

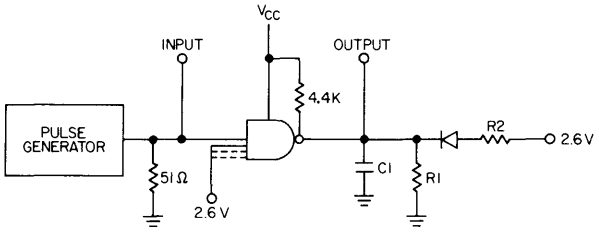
FIGURE 2 – TURN-ON AND TURN-OFF DELAY

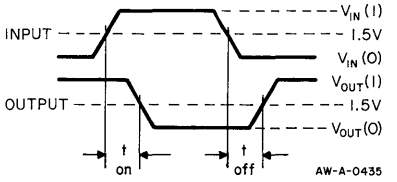
2A



* 2.6V for all gates except, 0.8V for 8815, 8875, and 8885.

2B

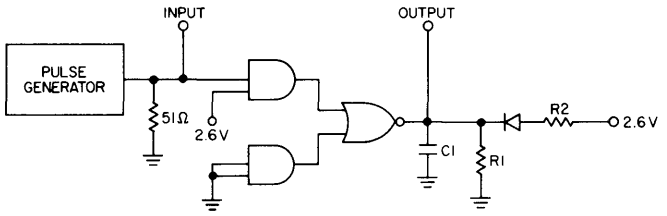


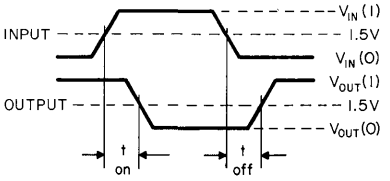


Input Pulse: Amplitude = 3.6V, P.W. = 200 ns, t_r = t_f = 10 ns for 8400 devices. Amplitude = 2.6V, P.W. = 50 ns, t_r = t_f = 5 ns for 8800 and 8H00 devices. PW measured at 50% points.

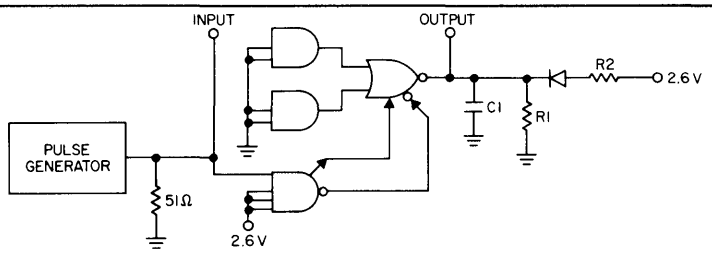
Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.
4. Input measuring points are per Figure A, Page 3-2.

2C



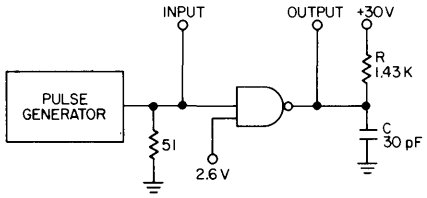


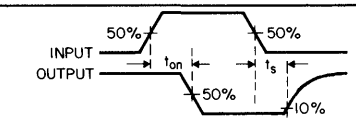
2D



Input Pulse: Amplitude = 3.6V, P.W. = 200 ns, $t_r = t_f = 10$ ns for 8400 devices. Amplitude = 2.6V, P.W. = 200 ns, $t_r = t_f = 5$ ns for 8800 devices.
P.W. measured at 50% points.

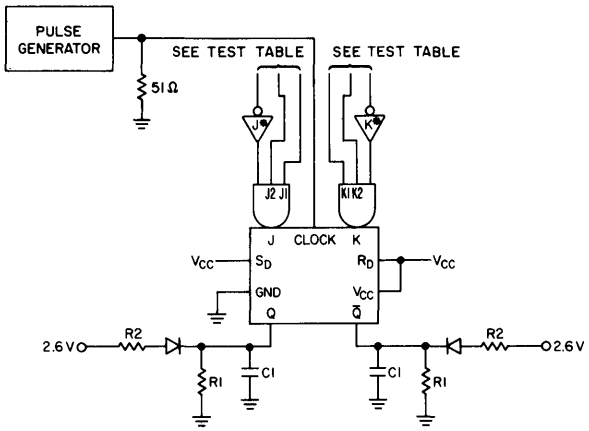
2E



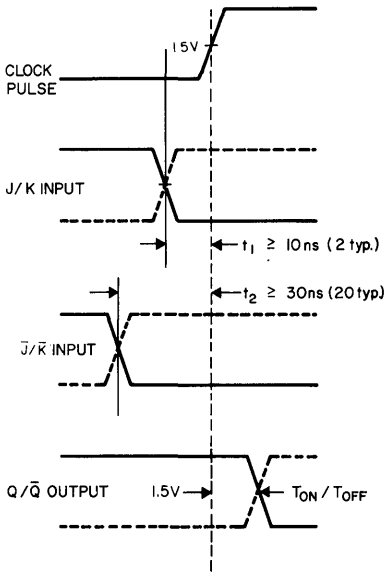


Input Pulse: Amplitude = 3.6V, P.W. = 1 μsec, $t_r = t_f = 10$ nsec.

2F

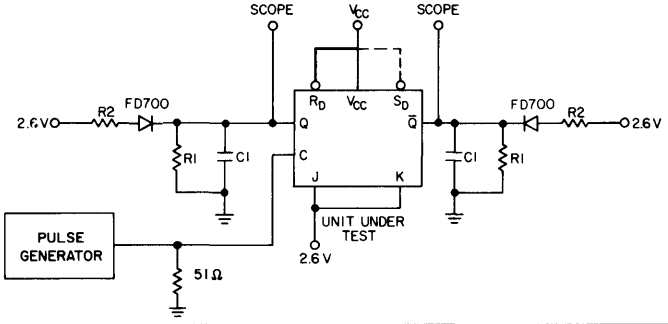


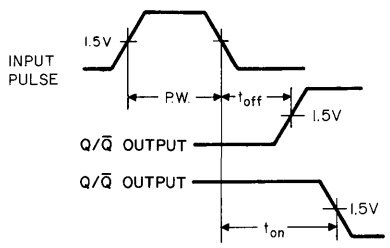
TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	+2.4V	GND
1	t_{on} ($\bar{Q}$)	$\bar{J}$	J1, J2	K1, K2	$\bar{K}$
2	t_{off} ($\bar{Q}$)	$\bar{K}$	K1, K2	J1, J2	$\bar{J}$
3	t_{on} (Q)	$\bar{K}$	K1, K2	J1, J2	$\bar{J}$
4	t_{off}(Q)	$\bar{J}$	J1, J2	K1, K2	$\bar{K}$



Input Pulse: Amplitude = 2.6V, P.W. = 200 ns, $t_r = t_f = 5$ ns.

2G

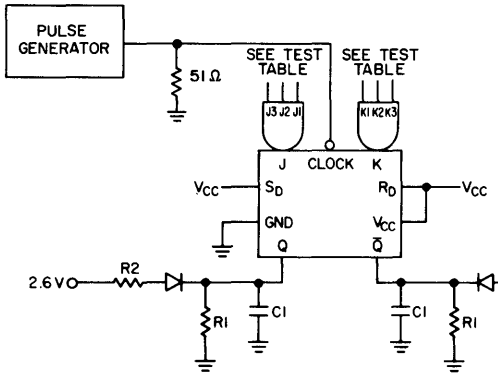




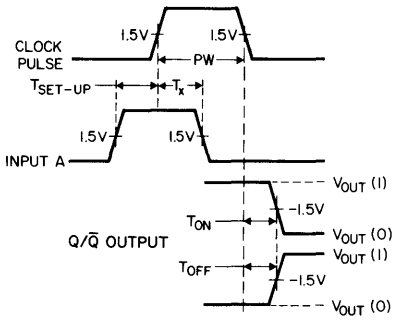
Input Pulse: Amplitude = 2.6V, P.W. = 50 ns, $t_r = t_f = 3$ ns.

Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.
4. Input measuring points are per Figure A, Page 3-2.

2H

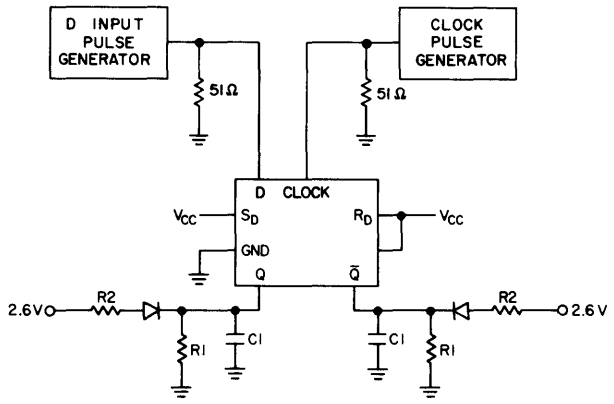


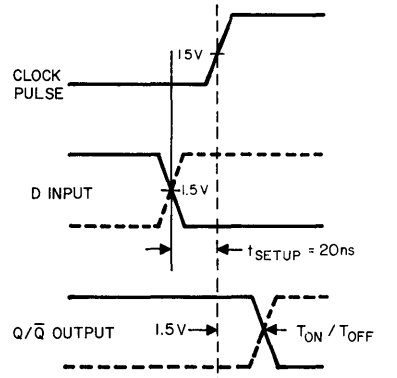
TEST TABLE			
TEST NO.	TEST	INPUT A	+2.6V
1	t_{on} (Q̄)	J1, J2, J3	K1, K2, K3
2	t_{off} (Q̄)	K1, K2, K3	J1, J2, J3
3	t_{on} (Q)	K1, K2, K3	J1, J2, J3
4	t_{off} (Q)	J1, J2, J3	K1, K2, K3



Input Pulse: Amplitude = 2.6V, P.W. = 200 ns, $t_r = t_f = 5$ ns.

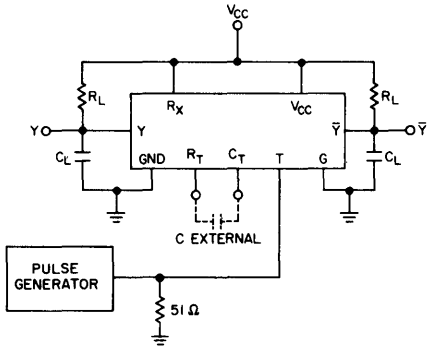
2I

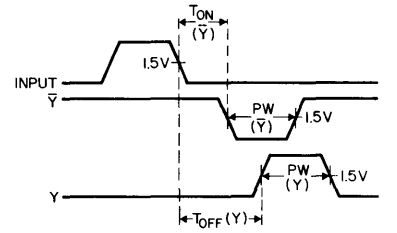




Clock Pulse: Amplitude = 2.6V, P.W. = 200ns, $t_r = t_f = 5$ns, f = 2 MHz.
D Input: Amplitude = 2.6V, P.W. = 500ns, $t_r = t_f = 5$ns, f = 1 MHz.

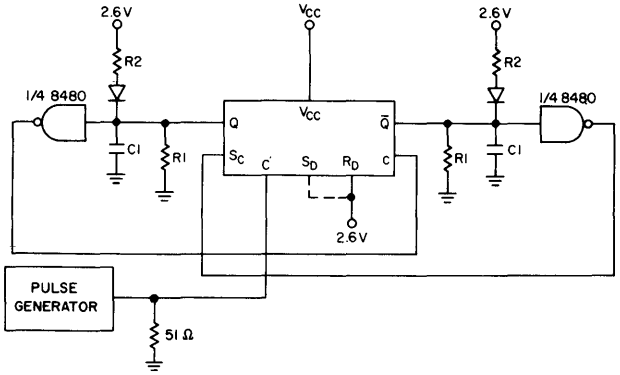
2J

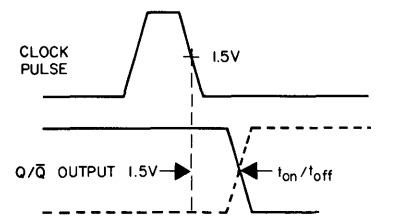




Loads for t_{on}, t_{off} and Pulse Width are as follows:
Fan-out = 1; R_L = 6 KΩ; C_L = 22 pF
Fan-out = 12; R_L = 500Ω; C_L = 60 pF
Input Pulse: Amplitude = 3.6V, Width = 200ns, $t_r = t_f$ = 10 ns, f = 1.0 MHz

2K

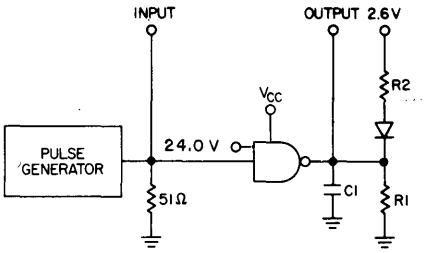


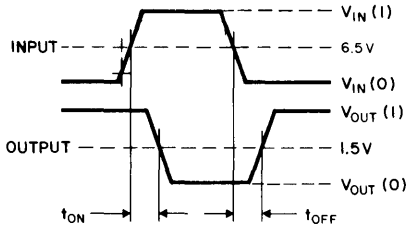


Input Pulse: Amplitude = 3.6V, P.W. = 200 ns, $t_r = t_f$ = 10 ns.

Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.
4. Input measuring points are per Figure A, Page 3-2.

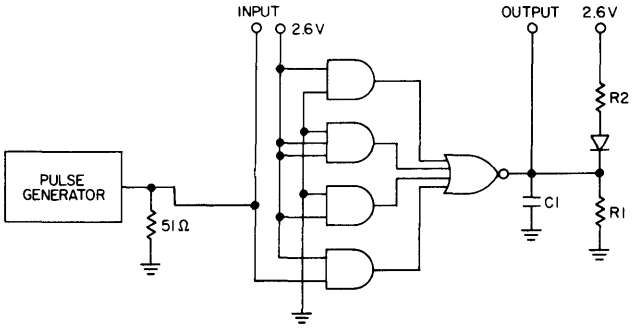
2L

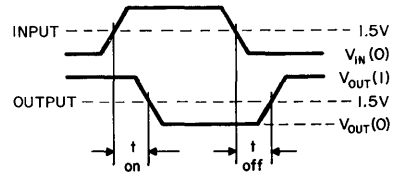




Input Pulse: Amplitude = 24.0V, P.W. = 200 ns, $t_r = t_f = 10$ ns.

2M

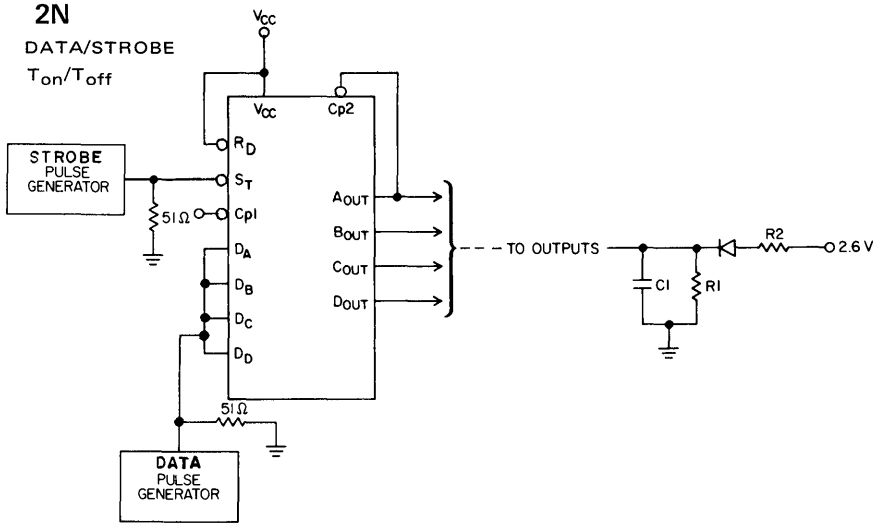


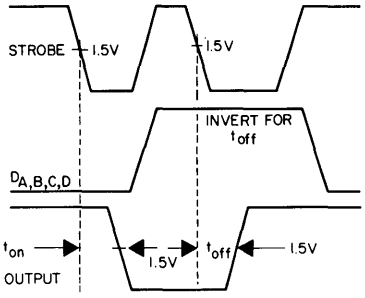


Input Pulse: Amplitude = 2.6V, P.W. = 350 ns, $t_r = t_f = 5$ ns.
P.W. measured at 50% points.

2N

DATA/STROBE
T_{on}/T_{off}

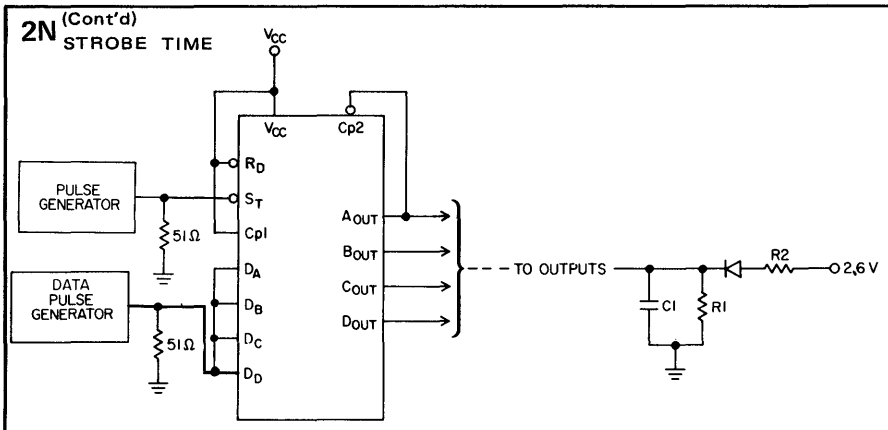


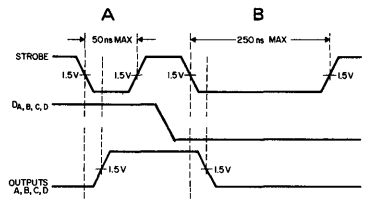


Strobe, P.A. = 2.6V
P.W. = 300ns, 50% to 50%
PRR = 1 MHz
$t_r = t_f = 5$ ns
Data, P.A. = 2.6V
P.W. = 500ns
PRR = 500 KHz
$t_r = t_f = 5$ ns.

Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.
4. Input measuring points are per Figure A, Page 3-2.

2N (Cont'd) STROBE TIME





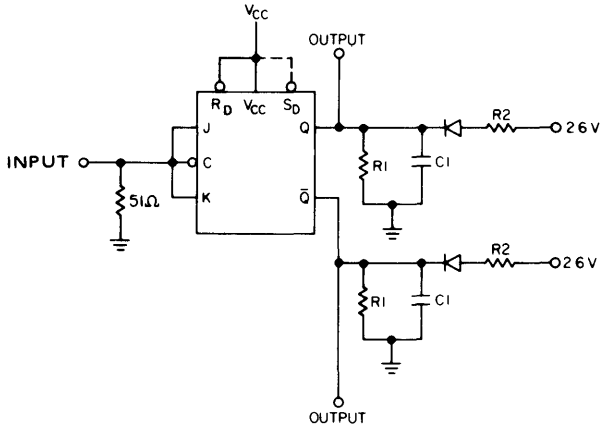
A With all outputs initially "0", output shall have a "0" to "1" transition.

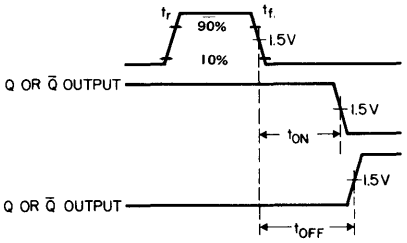
B With all outputs initially "1", outputs shall have a "1" to "0" transition.

Amplitude = 2.6V (from Pulse Generator)

$t_r = t_f = 5ns$

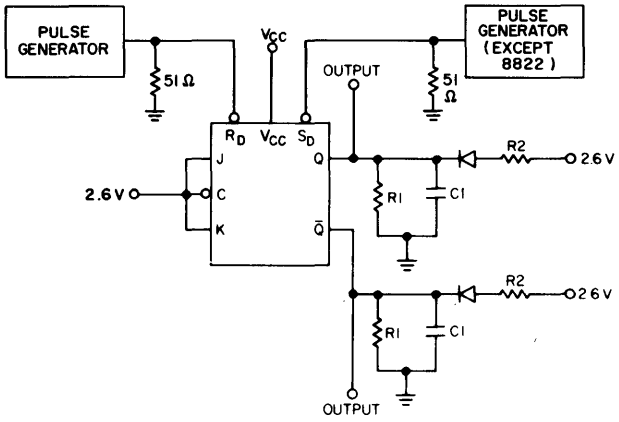
2P CLOCKED MODE

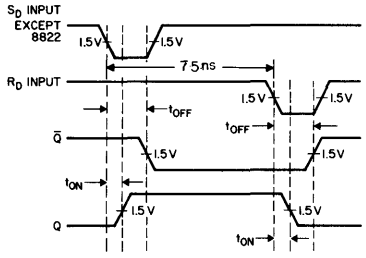




Input: Pulse Amplitude = 2.6V
Pulse Width = 25 ns
$t_r = t_f = 5$ ns

2P (Cont'd) DIRECT MODE

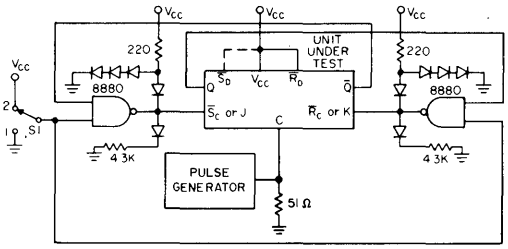




Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.
4. Input measuring points are per Figure A, Page 3-2.

FIGURE 3 – CLOCKED MODE SWITCHING AND HOLDING LEVEL

3A



SWITCHING TEST FOR 8424 and 8425
Apply Step 1 S1 Position 2
SWITCHING TEST FOR 8826 and 8827
Apply Step 1 S1 Position 1

HOLDING TEST
Apply Step 2 only.
S1 Position 1 (8424 & 8425)
S1 Position 2 (8826 & 8827)

STEP 1
Apply a single pulse: Amplitude = 3.4V, P.W. = 200ns, $t_r = t_f = 75$ns.
Outputs shall change state.

STEP 2
Apply input pulses: Amplitude = 4.5V, P.W. = 200ns, $t_r = t_f = 10$ns.
Output shall not change state.

Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.
4. Input measuring points are per Figure A, Page 3-2.

FIGURE 4 – TOGGLE RATE

4A

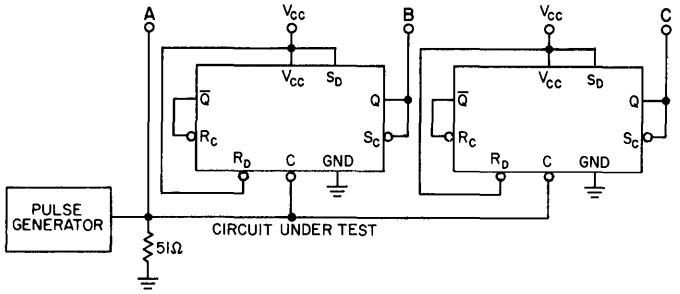
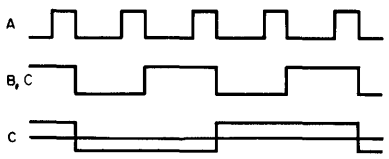


Figure 4A 8424 only.
Input Pulse: Amplitude = 3.6V, P.W. = 60 ns, $t_r = t_f = 5$ ns.



4B

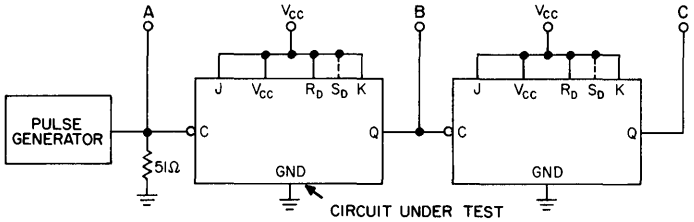
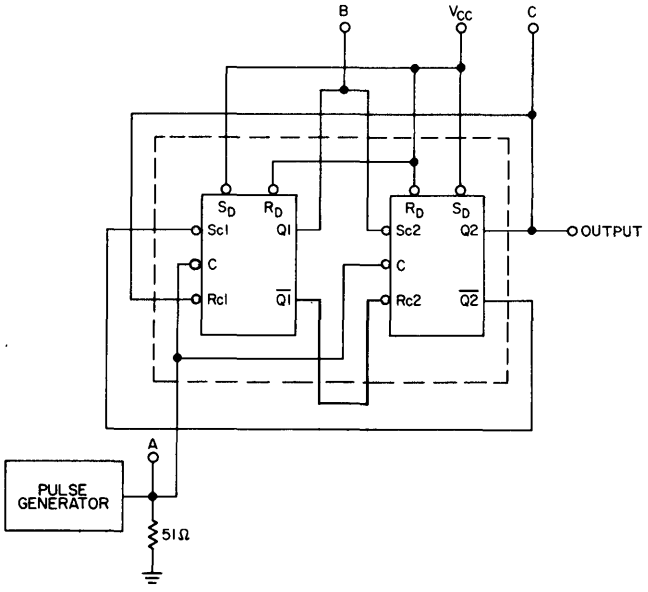
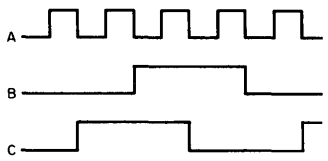


Figure 4B

Input Pulse: Amplitude = 2.6V, 8826 P.W. = 10ns, $t_r = t_f = 5$ns; 8822 and 8824 P.W. = 20ns; $t_r = t_f = 5$ns.

4C

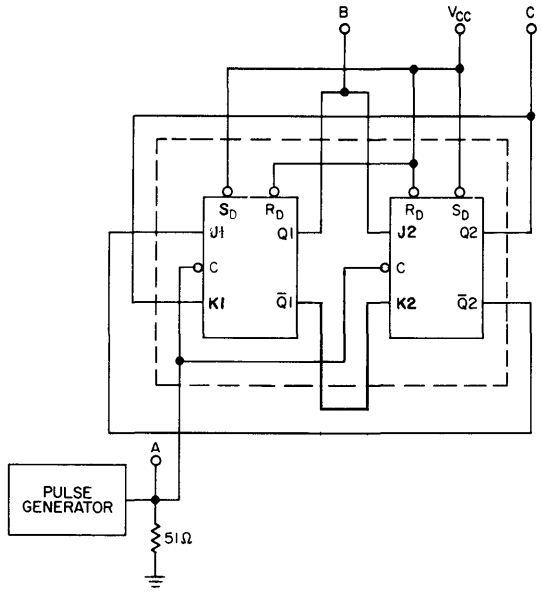


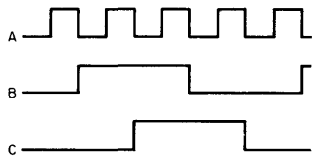


Input Pulse: Amplitude = 3.6V, P.W. = 60 ns, $t_r = t_f = 10$ ns.

Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.

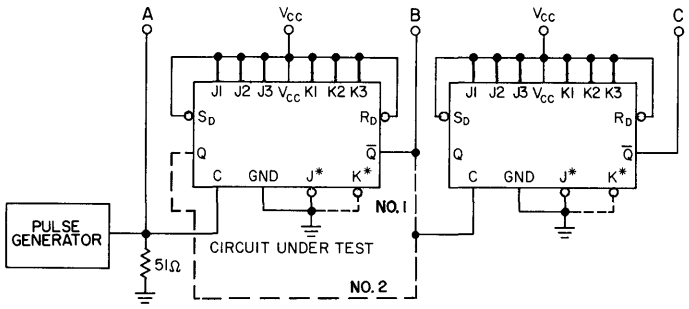
4D



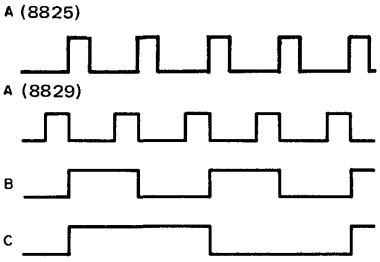


Input Pulse: Amplitude = 2.6V
8827 P.W. = 10 ns $t_r = t_f = 5$ ns
8821 P.W. = 20 ns $t_r = t_f = 5$ ns
8H20, 8H21, 8H22 P.W. = 7 ns
$t_r = t_f = 3$ ns

4E



#1. 8825 CONNECTION: $\bar{Q} = C_L$
#2. 8829 CONNECTION: $Q_B = C_L$

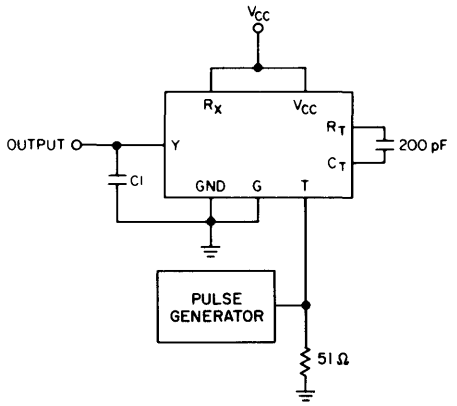


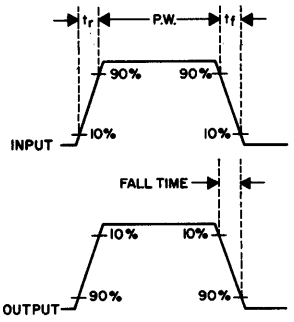
Input Pulse: Amplitude = 2.6V, P.W. = 33 ns, $t_r = t_f = 5$ ns.

Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.

FIGURE 5 – OUTPUT FALL TIME

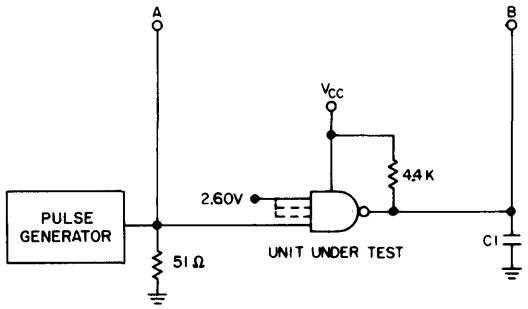
5A



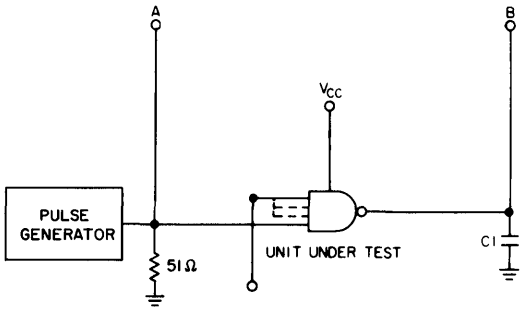


Apply the following input pulse to trigger input: Amplitude = 3.6V, Width = 200 ns, $t_r = t_f = 10$ ns, f = 100 KHz.

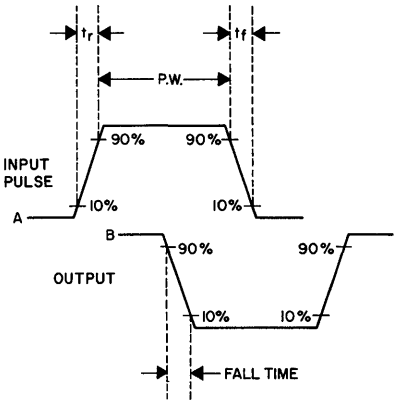
5B



5C

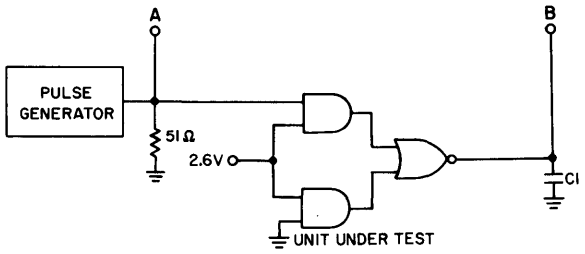


2.6V for all gates except 0.8V for 8815, 8875, and 8585.



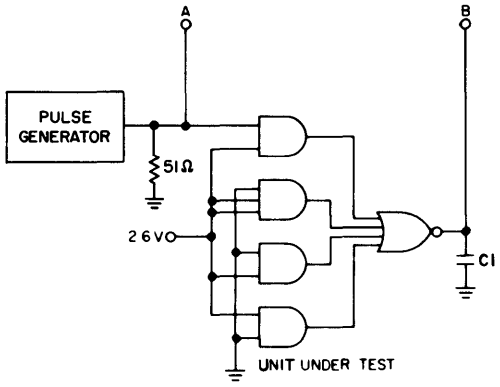
Input Pulse: Amplitude = 3.6V, P.W. = 200 ns, $t_r = t_f = 10$ ns, Repetition Rate = 500 KHz.

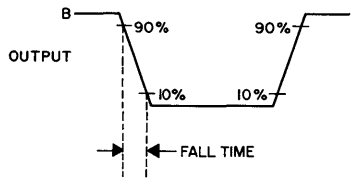
5D



Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.

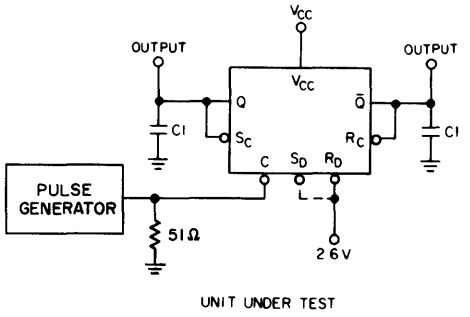
5E



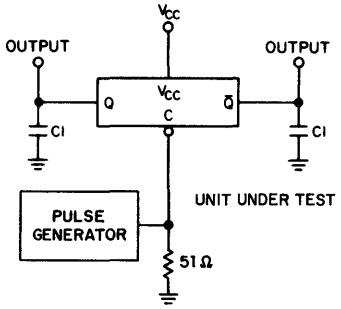


Input Pulse: Amplitude = 3.6V, P.W. = 200 ns, $t_r = t_f = 10$ ns.

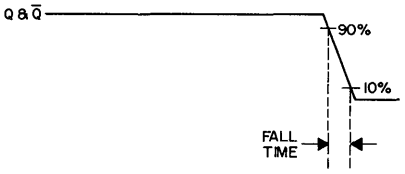
5F



5G

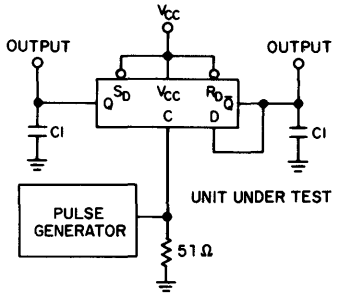


R_D, S_D, J, and K inputs tie to V_{CC}, $\bar{J}$ and $\bar{K}$ inputs tie to 0V.



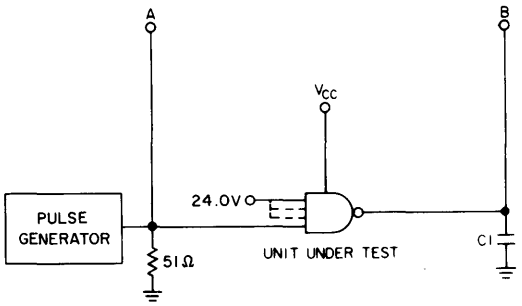
Input Pulse: Amplitude = 3.6V, P.W. = 200 ns, $t_r = t_f = 10$ ns.

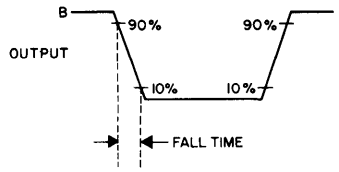
5H



Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.
4. Input measuring points are per Figure A, Page 3-2.

5I





Input Pulse: Amplitude = 24.0V, P.W. = 200 ns, $t_r = t_f = 10$ ns.

Notes: 1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, Vac = 25 mV rms.
3. All diodes are 1N916.
4. Input measuring points are per Figure A, Page 3-2.

SECTION 4 - APPLICATIONS

GATES

This part of Section IV is devoted to 8000 Series gates. Input structures, output structures, collector logic and AND-OR-INVERT gates are discussed. For quick reference, a table of typical propagation delays and power consumptions for the 8000 Series gates is given here:

Group	Typical Propagation Delay	Typical Power Consumption
8400's	25ns	7 to 9mW
8800's	8ns	17 to 19mW
8H00's	6ns	25mW

INPUTS

TTL Input Structure

The TTL input features the multiple emitter input structure (Q_1) with a phase-splitting transistor (Q_2) as shown in Figure 4-1.

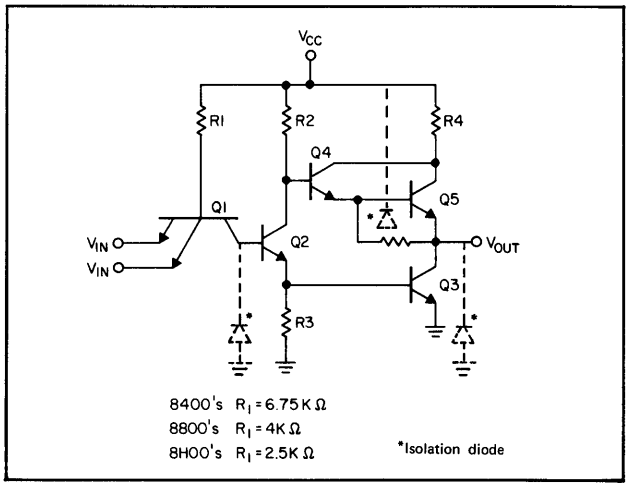


Figure 4-1

The only difference between the TTL input structures of the 8400, 8800 and 8H00 gates is the value of the input resistor R1 (shown in Figure 4-1). Thus the "0" level input current for the 8400's is 1/2 that of the 8800's, and 1/3 that of the 8H00's.

The phase-splitting transistor, Q_2, serves two functions: first, it supplies sufficient base drive to Q_3 to cause Q_3 to turn on rapidly and saturate. Second, it ensures that the upper transistors, Q_4 and Q_5, and the lower transistor, Q_3, remain in opposite states. This prevents the large power supply current drain which would result if they all happened to be on at the same time -- in such a case, the only impedance in the power-supply-to-ground path would be the 80-ohm current limiting resistor, R_4.

DTL Input Structure

The DTL input, whose structure is shown in Figure 4-2, is available in the 8415, 8416 and 8417 gates.

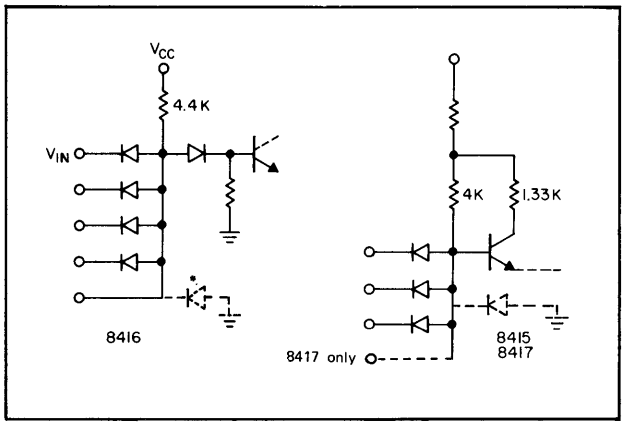


Figure 4-2

The 8416 and the 8417 allow for input expansion with either diodes or diode arrays. Input expansion influences both DC noise margins and switching times. Therefore, allowable maximum fan-ins may be set by switching speed requirements in one application, and by DC noise margins in another. Turn-on delays for the expanders increase about 3ns per picofarad of capacitance on the expansion input; this is because the input resistor of the gate must charge this additional capacitance before the gate may be switched. The capacitance of the expanders (8706/8731) is 1pf per input plus 3pf per diode cluster. Turn-off time is not appreciably influenced by the capacitance, since it will be discharged through the input diode and low output impedance of the driving gate.

Fan-in will be limited by the leakage current of the expanders (8706/8731). This current will decrease the "1" DC noise margin as a function of number of expander diodes as shown in Figure 4-3.

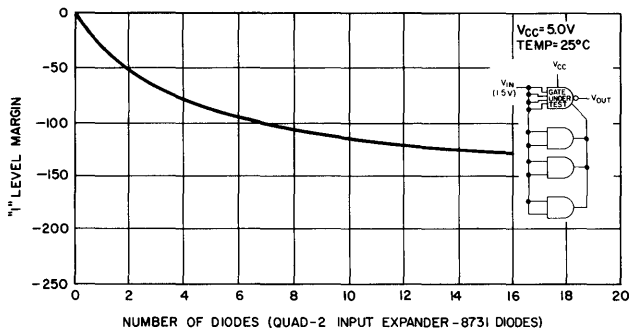


Figure 4-3 — "1" Level DC Margin as a Function of Number of Expander Diodes

Unused Inputs

It is recommended that all unused inputs of 8000 Series gates be connected to driven inputs. This not only provides the best switching speed, by virtue of the shunted capacitance, but also facilitates board layout, since shorting of adjacent pins is all that is necessary. The "1" level input current will increase by a maximum of 25μA for each input which is connected to a driven input, but the "0" level input current is not affected.

Unused inputs may also be tied to V_{CC}. Connecting unused inputs to V_{CC} gives the best noise immunity and results in some speed improvement over open inputs. If unused inputs of the 8400 gates are connected to V_{CC}, the connection should be made through a resistor (5K to 20K).

OUTPUTS

8000 Series gates have two kinds of outputs: active pull-up and bare collector. Bare collector devices are primarily intended for collector logic applications. Among the active pull-up outputs there are five types, each of which will be treated separately.

It should be kept in mind that, at interfaces where non-operating (V_{CC} off) gates may be connected to an operating system, due regard must be given the isolation diode associated with the resistor at the output of the gate. Power supply outputs frequently become a low impedance to ground when the input power is removed. In this case, gate outputs will be clamped positive (one diode drop) with respect to ground by virtue of diode R. (See Figure 4-4.) In the case of the 8855 power buffer (Figure 4-8), the resistor which is tied to the output acts as a reversed bias diode to ground. This resistor diode in conjunction with the collector isolation diode of the output pull-down transistor provides an effective diode clamp to negative excursions at the output.

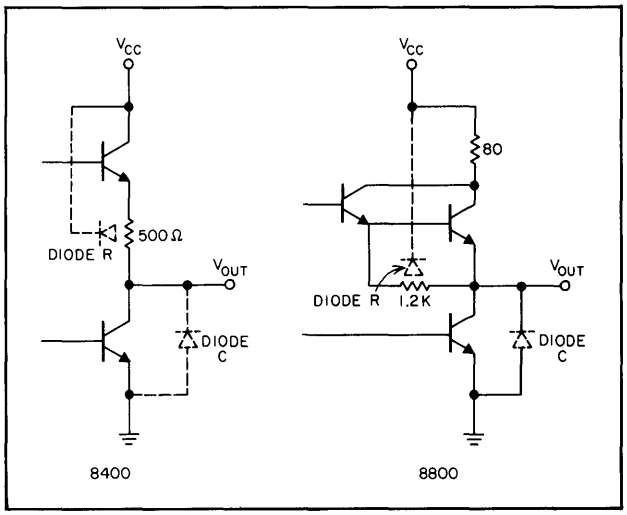


Figure 4-4

8416, 8440, 8470, 8480 Outputs (Active Pull-Up)

The outputs of these types have a 500-ohm series current-limiting resistor, as shown in Figure 4-5.

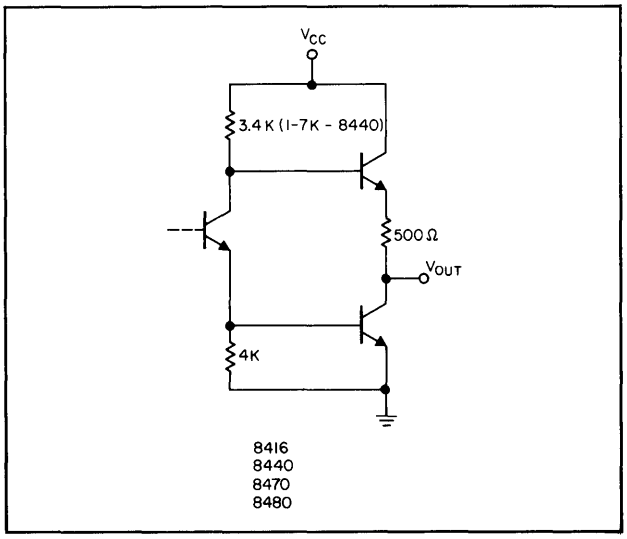


Figure 4-5

This output structure enables these elements to achieve DTL performance (speed) at lower than normal DTL power levels. The effective output impedance of less than 600 ohms results in rise times which are much faster than in conventional DTL (2K to 6K-ohm output impedance). However, when the gate is in the "0" state, the upper stage is off and the power consumption is less than would result if a passive 600-ohm resistor were used.

The curve of power vs. frequency for the 8480 is almost flat, which means that virtually the same low power is used at all frequencies. This characteristic is typical of 8400 gates. The "flat" characteristic is achieved through the special design of the output structure.

8455 Output (Active Pull-Up)

The second type of active pull-up has a diode by-pass around a 200-ohm resistor. This structure results in higher fan-out, with fast rise-times into heavy capacitive loads such as the 8424 clock input. (See Figure 4-6.)

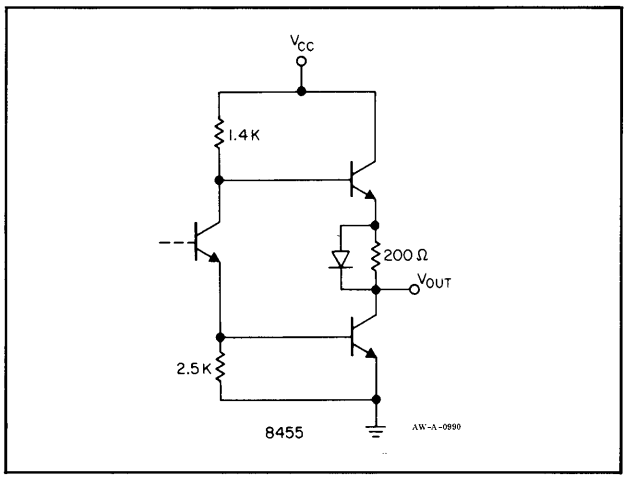


Figure 4-6

8800's Output (Active Pull-Up)

The third type of active pull-up output structure is the classical TTL design and is found in the 8800 gates. The Darlington configuration provides a low output impedance.

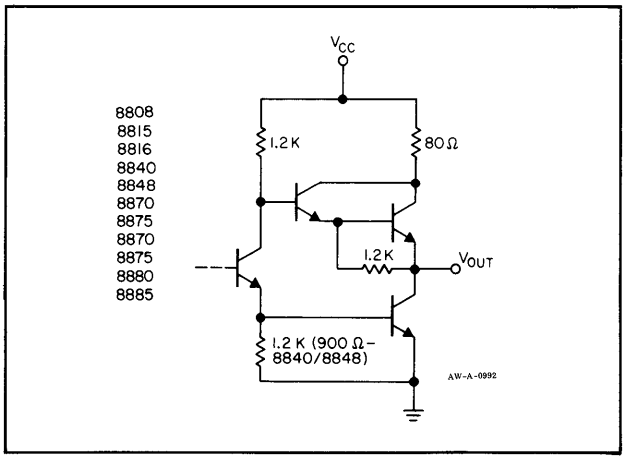


Figure 4-7

The low impedance output structure of the 8800s results in fast turn-off even when driving capacitive loads. Elements will not be damaged if their outputs are momentarily shorted to ground.

The 8855 has a lower current-limiting resistor value (namely 60 ohms) and a 4.4K-ohm resistor to ground.

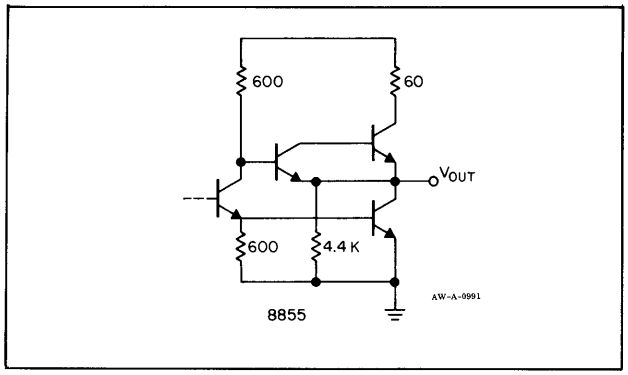


Figure 4-8

The "1" level output impedance of one of the 8800 gates may be determined from the slope of the curves below. The output impedance (slope) is dependent upon the output current. Note that there are two regions of constant slope. The output impedance is essentially that of an emitter-follower in the lower current region. In the higher current region the output impedance is primarily that of the collector resistor (80 ohms).

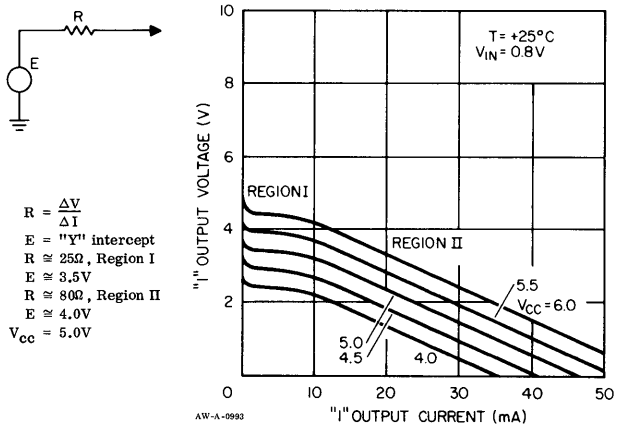


Figure 4-9

The equivalent voltage source may be determined from the "Y" intercept of the curves for a given power supply voltage (V_{CC}). A "1" level equivalent output circuit for a typical case is shown in Figure 4-9.

8H00 Outputs (Active Pull-Up)

The output structure of these gates is essentially the same as that for the 8800's, except for the lower resistor values and the 4K resistor to ground. These changes provide the higher speeds of the 8H00 gates.

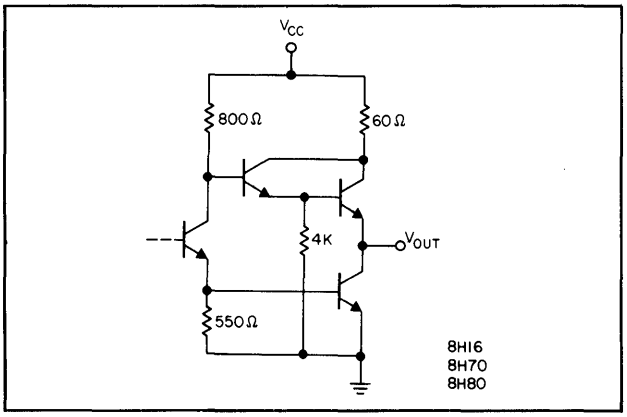


Figure 4-10

8415, 8417, 8471, 8481, 8881 Outputs (Bare-Collector or Passive Pull-Up)

The second general class of 8000 Series outputs is the bare collector type. Five gates, the 8415, 8417, 8471, 8481 and 8881 provide this output structure. The bare collectors permit the elements to be paralleled (i.e. collector logic) with other bare collector elements. The 8417 also has an optional 4.4K-ohm pull-up resistor available. A detailed explanation of collector logic and its implementation follows.

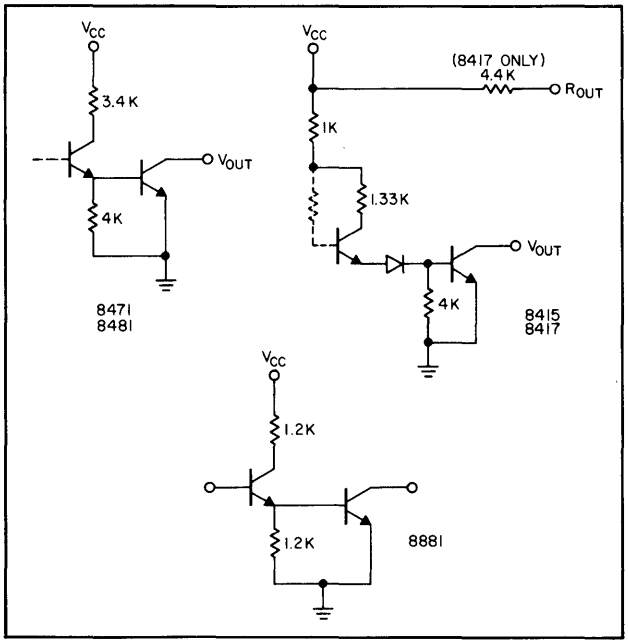


Figure 4-11

Expansion of 8000 Series Outputs (Collector Logic)

"Wired-AND" is the nomenclature used by Signetics to indicate the collector logic function formed by connecting two or more passive pull-up elements. The significant advantage of collector logic is that it provides a new "free" logic function, as illustrated below:

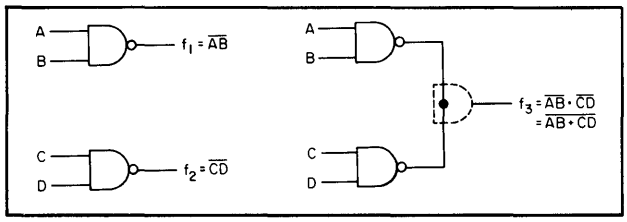


Figure 4-12

Because the new function, $f_3 = \overline{AB + CD}$ is equivalent to the AND-NOR gate, it is also frequently known as "wired-OR."

Allowed Values of R_L for Collector Logic Elements

Collector logic can be implemented using the bare collector elements 8415, 8417, 8471, 8481 and 8881. The 8417 element contains an optional 4.4 K ohm pull-up resistor.

1. The maximum value of load resistance ($R_{L\ MAX}$) is determined by the maximum voltage drop across R_L caused by the total leakage current which will still ensure a minimum logical "1" at the common collector node.

   Total leakage current $I(1)_{total} = n\ I(1)_o + m\ I(1)_i$

   n = Number of commoned collectors (driving gates)

   m = Number of fan-outs (driven gates)

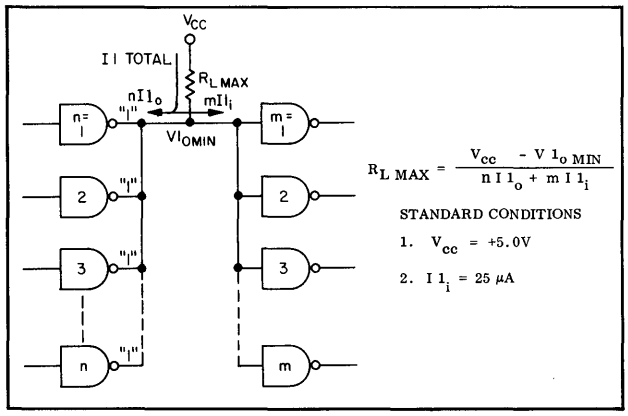


Figure 4-13

2. The minimum value of load resistance ($R_{L\ MIN}$) is determined from the worst case maximum logical "0" state in which only one element is sinking current. This condition is illustrated below:

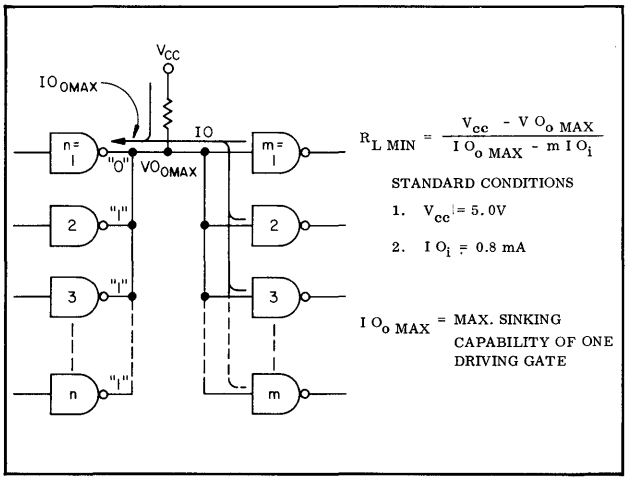


Figure 4-14

3. Knowledge of the range of possible values of R_L for any combination of commoned collectors and total fan-outs (F.O.'s) is of extreme importance in any collector logic oriented system. Figures 4-15 through -17 for the bare collector gates 8415/17, the 8471/81 and the 8881, respectively, will enable the system designer to choose R_L for any combination of commoned collectors, number of fan-outs, speed and power consumption.

The maximum load resistance minimizes power consumption, but at the expense of decreased AC noise immunity and slow switching speeds. The choice of the minimum load resistance produces maximum AC noise immunity and minimum switching speed or minimum propagation delay. The guaranteed DC noise margins are not effected if the value of R_L is within its absolute limits.

To use the curves in Figures 4-15 through -17, draw a horizontal line out from the vertical axis at the level of the required number of fan-outs (m). Extend the line until it intersects the $R_{L\ MAX}$ line for the required number of commoned collectors (n). The line will also intersect the $R_{L\ MIN}$ curve. Drop a vertical from where it intersects the $R_{L\ MIN}$ curve and another from where it intersects the $R_{L\ MAX}$ curve. The range of values between these verticals on the Load Resistor axis is the full range of R_L for those n and m values. (Example: for the 8415, Figure 4-15, if m = 5 and n = 4, R_L ranges from 1.1 KΩ to 4.9 KΩ.)

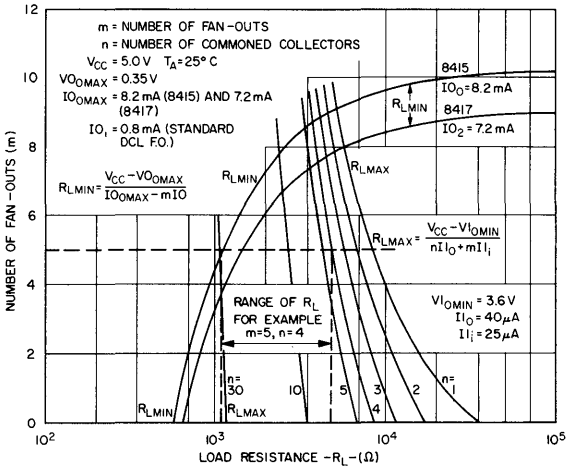


Figure 4-15 — Allowed Values of R_L for the 8415 and 8417

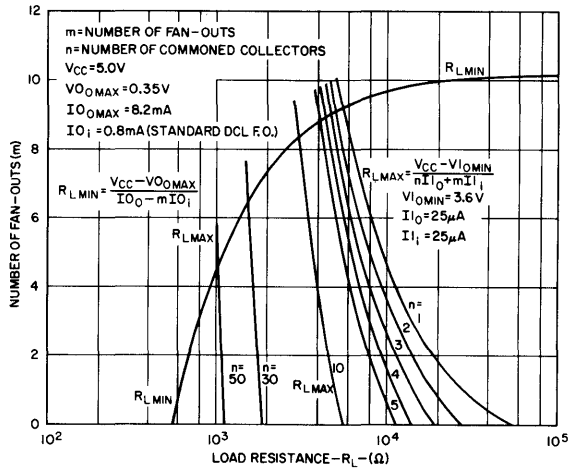


Figure 4-16 — Allowed Values of R_L for the 8471 and 8481

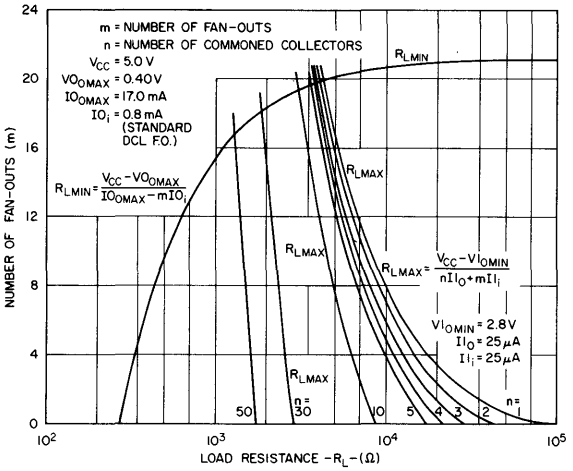


Figure 4-17 — Allowed Values of R_L for the 8881

8440, 8840, 8848 AND-OR-INVERT Gates

These gates provide the collector logic function, that is, they give an output $f = \overline{AB + CD}$. The 8806 input expander may be used with the 8840 and the 8848 (but not the 8440) to expand logic capability. Input expansion of these devices will decrease the "0" input threshold voltage in accordance with this curve.

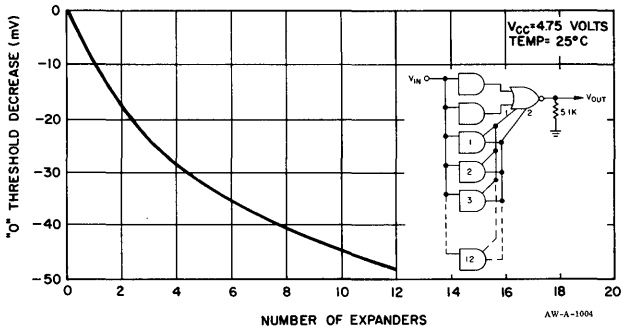


Figure 4-18

Care should be taken when laying out the lines for the 8840 and 8848 expansion points to minimize capacitance and noise pick-up.

The elements can be paralleled, as shown in Figure 4-19 below. Because of the capacitance pick-up and the current gain of the elements, it is recommended that only one additional 8840 and 8848 be connected to another 8840 or 8848.

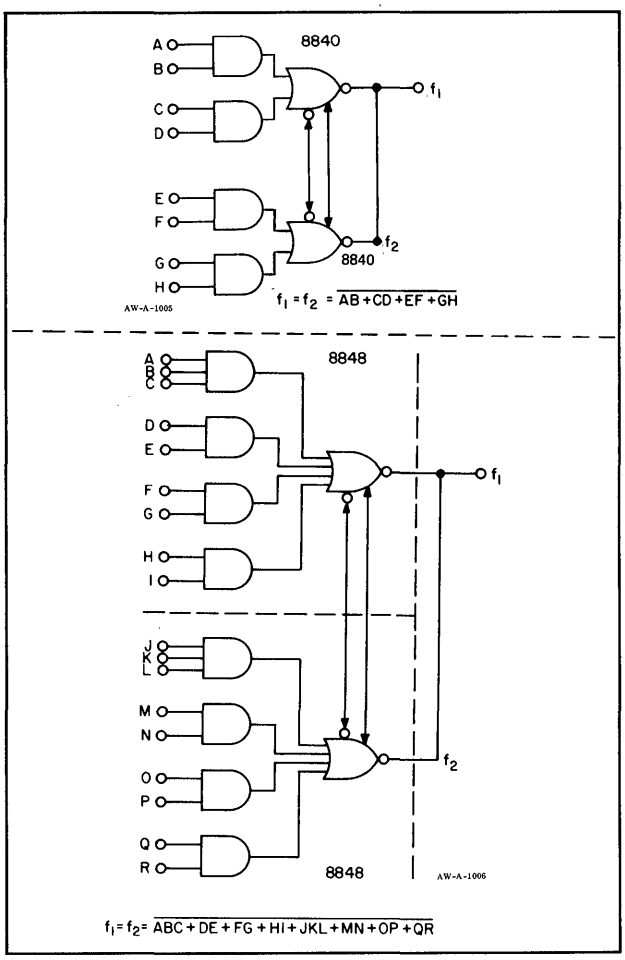


Figure 4-19

BINARIES

8000 SERIES BINARY REFERENCE TABLE

NO.	FUNCTION	ORGANIZATION *	CLOCK		SYNC INPUTS **	ASYNC INPUTS ***	USAGE
			TRIGGERING SLOPE	SEPARATE/ COMMON			
8424	RS/T	Dual AC	Negative	Separate	$\overline{R}_c$ $\overline{S}_c$	$\overline{R}_D$	General Purpose
8425	RS/T	Dual AC	Negative	Common	$\overline{R}_c$ $\overline{S}_c$	$\overline{R}_D$ (Common), S_D	General Purpose
8821	JK	Dual M-S	Negative	Common	J K	$\overline{R}_D$ (Common), $\overline{S}_D$	Sync Counters Control F/F
8822	JK	Dual M-S	Negative	Separate	J K	$\overline{R}_D$	Sync Counters Control F/F
8824	JK	Dual M-S	Negative	Separate	J K	$\overline{R}_D$ $\overline{S}_D$	Sync Counters Control F/F
8825	JK	Single DC	Positive	—	JJ$\overline{J}$ KK$\overline{K}$	$\overline{R}_D$ $\overline{S}_D$	Control F/F
8826	JK	Dual AC	Negative	Separate	J K	$\overline{R}_D$	High Speed Sync Counters
8827	JK	Dual AC	Negative	Common	J K	$\overline{R}_D$ (Common), $\overline{S}_D$	High Speed Sync Counters
8828	D	Dual DC	Positive	Separate	D	$\overline{R}_D$, $\overline{S}_D$	Shift Reg Sync Reg
8829	JK	Single DC	Negative	—	JJJ KKK	$\overline{R}_D$, $\overline{S}_D$	Control F/F
8H20	JK	Dual SC	Negative	Separate	J K	$\overline{R}_D$	Very High Speed
8H21	JK	Dual SC	Negative	Common	J K	$\overline{R}_D$ (Common) $\overline{S}_D$	Very High Speed
8H22	JK	Dual SC	Negative	Separate	J K	$\overline{R}_D$, $\overline{S}_D$	Very High Speed

NOTES:

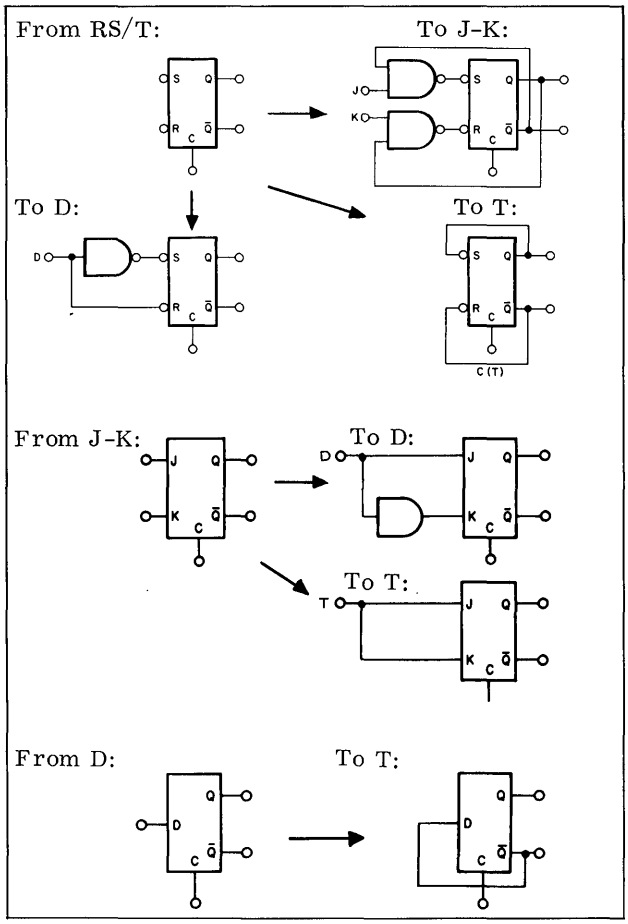
* Dual — Two Binaries per pkg.
Single — One Binary per pkg.
AC — Capacitive Coupled Input
DC — Gated Input (Threshold)
M-S — Master Slave
SC — Stored Charge

** Unused J-K, RS, D Inputs should be handled the same as unused gate inputs, except 8825 $\overline{J}$ and $\overline{K}$ should be tied to ground.

*** Unused $\overline{S}_D$ and $\overline{R}_D$ inputs should be handled the same as unused gate inputs.

RELATIONSHIP OF BINARY TYPES

The various binaries can be thought of as an evolution of the original RS/T which subsequently resulted in the J-K, the D, and the T, in that order. Each successive type is produced through the addition of NAND gates and connections as shown below:



CLOCKING

8424, 8425

The 8424 and 8425 binaries (shown in Figure 4-20) respond to the negative-going edge of the clock pulse. The recommended clock pulse waveform is a normally low-riding, positive-going pulse of 2.5 volts amplitude, 100 nanoseconds wide, with a fall time of less than 75 nanoseconds. A protective diode is included at the clock input to limit positive excursions of the clock line to about 0.5 volts above the power supply, and to limit negative excursions to about -30 volts. The current in this diode should be limited to 10 milliamps on positive excursions and 1 milliamp on negative excursions.

In counters and shift registers, the 8424 and 8425 will typically operate to frequencies of 12 MHz.

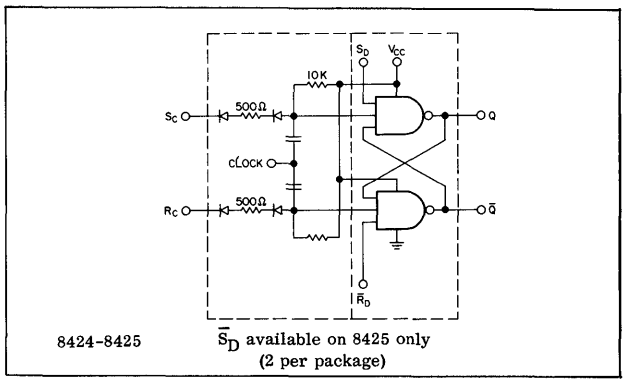


Figure 4-20 — Binary Logic Equivalent

8821, 8822, 8824

These binaries (shown in Figure 4-21) are DC coupled, master-slave J-K binaries which respond to the negative-going edge of the clock pulse. The clock pulse should be a minimum ow 20ns wide. Triggering is independent of clock pulse fall time. The master section of the binary is enabled when the clock is high and will accept the J and K information at its inputs which must remain stable while the clock line is high. The information is transferred from the master to the slave when the clock pulse falls.

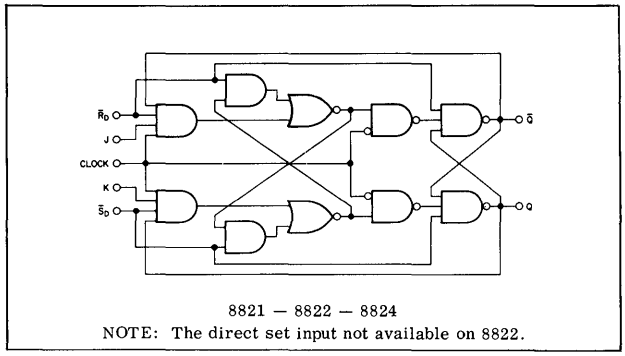


Figure 4-21

8825, 8828

The 8825 (Figure 4-22) and 8828 (Figure 4-23) respond to the positive-going edge of the clock pulse. The logic inputs are locked out once the clock is high, thus preventing more than one transition of the binary per clock pulse.

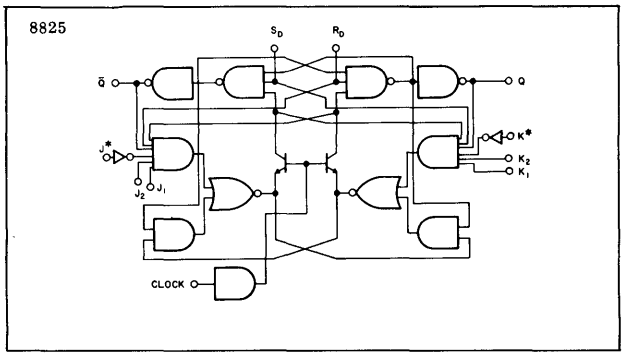


Figure 4-22

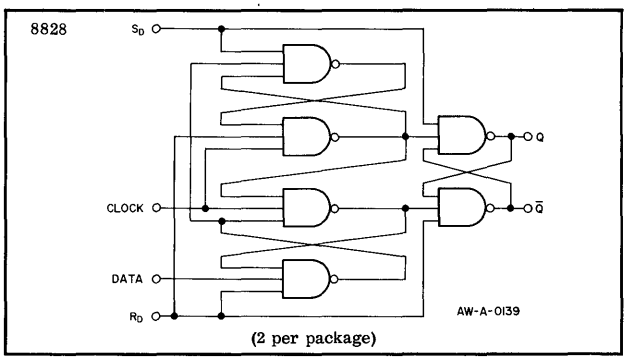


Figure 4-23

8826, 8827

The 8826 and 8827 (Figure 4-24) respond to the negative-going edge of the clock input. The recommended clock pulse waveform is a positive-going pulse that is at least 10 nanoseconds wide at the 2.4-volt level, and has a fall time of less than 50 nanoseconds. If the amplitude is 3.6 volts, the fall time should be less than 75 nanoseconds. The clock pulse width must be limited to 1.0 microseconds maximum when the J and/or K inputs are a logical "0". For example, there is no restriction on the maximum pulse width of the 8826 when it is being used as a ripple counter, since the J and K inputs are both at a logical "1" level.

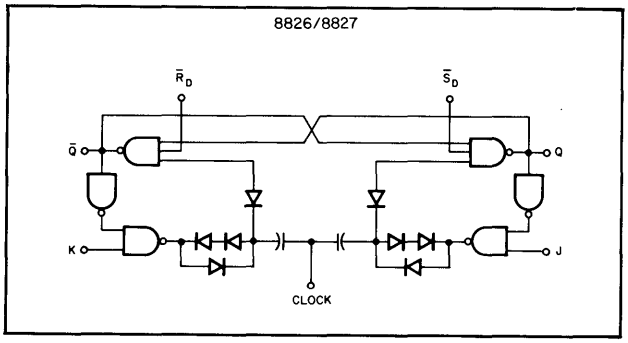


Figure 4-24

8829

The 8829 binary (Figure 4-25) responds to the negative-going edge of the clock pulse. J-K information is locked out of the master once the clock has risen, thus preventing system errors due to clock skew. The recommended clock pulse waveform is a positive-going pulse at least 15 nanoseconds wide at the 2 volt level with rise and fall times less than 150 nanoseconds.

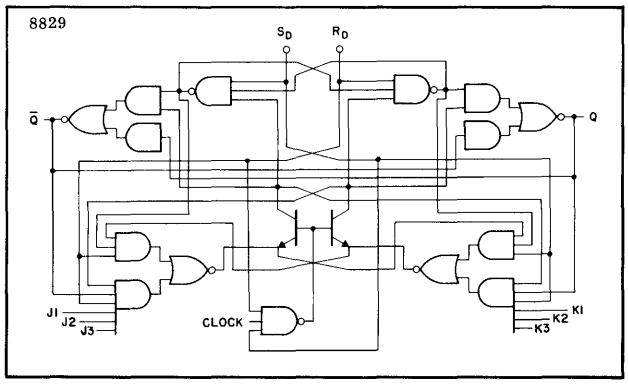


Figure 4-25

8H20, 8H21, 8H22

These binaries are triggered on the negative-going edge of the clock pulse. The recommended waveform is a positive-going pulse at least 10 nanoseconds wide at the 2.4 volt level, with a maximum fall time of 200 nanoseconds. A typical logic diagram for these devices is shown in Figure 4-26.

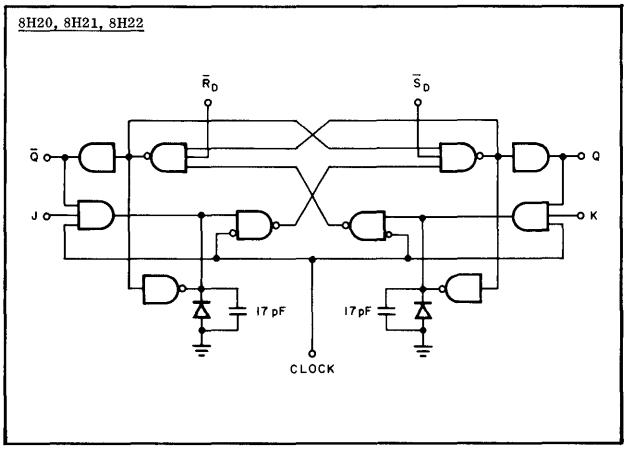


Figure 4-26

SYNCHRONOUS INPUTS

8424, 8425

The logic levels to $\bar{R}_c$ and $\bar{S}_c$ inputs should be at their final values before the clock pulse rises and should remain stable while the clock pulse is high. (For logic diagram, see Figure 4-20.)

If the $\overline{R}_C$ and $\overline{S}_C$ logic is to be changed when the clock is high (refer to Figure 4-27), two factors must be considered: the device driving the clock must have a low enough source impedance to supply sufficient charging current so that changing the $\overline{S}_C$ and $\overline{R}_C$ inputs will not cause false triggering through the capacitors. (Devices in the 8000 Series with active pull-up outputs are recommended.) Second, if the clock line is normally high, the logic lines should be stable for at least 1.5 microseconds before the fall of the clock.

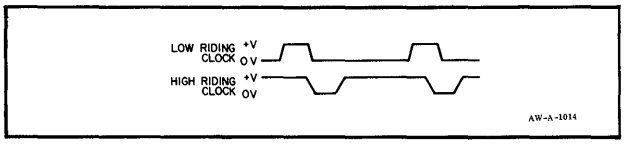


Figure 4-27

Because the 8424 and 8425 have inverting logic synchronous inputs, the AND function is available at the NAND gate outputs, and the AND-OR functions are directly available at the AND-NOR gates, as can be seen from the figure below.

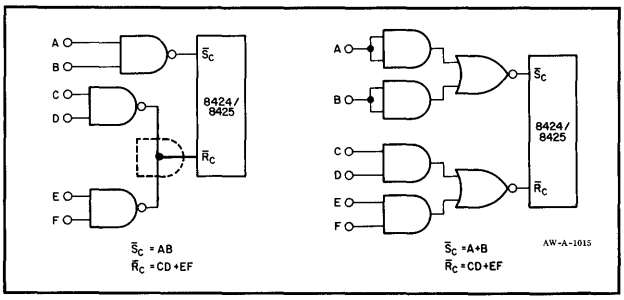


Figure 4-28

8821, 8822, 8824

The J and K inputs must remain stable while the clock is high, but they may change coincidentally with the rise and fall of the clock pulse. (For logic diagram see Figure 4-21.)

8825, 8829

Logic levels at the J and K inputs should be stabilized at a logical "1" or "0" level at least 10 nanoseconds before and after the clock pulse rises. Logic levels at the $\overline{J}$ and $\overline{K}$ inputs should be stabilized at the logical "1" or "0" level 25 nanoseconds before the clock pulse rises and should remain stable for 10 nanoseconds after the clock pulse rises. Unused $\overline{J}$ and $\overline{K}$ must be tied to ground. (For logic diagram, see Figure 4-22 and 4-25.)

8826, 8827

Logic levels at the J and K inputs should be stabilized at a logical "1" or "0" level before the clock pulse rises and should remain stable until the clock pulse falls. (For logic diagrams see Figure 4-24.)

8828

Logic levels to the D input must be stabilized at a logical "1" or "0" 20 nanoseconds before the clock pulse rises. The D input is locked out approximately 10ns (one gate delay) after the clock pulse exceeds the clock input threshold. The D input must therefore remain stable for 10 nanoseconds after the clock pulse rises. (For logic diagram see Figure 4-23.)

8H20, 8H21, 8H22

The logic states of the J and K inputs must be stable when the clock input rises, and must remain stable until the clock falls.

ASYNCHRONOUS INPUTS

8424, 8425

The direct SET (S_D) and RESET (R_D) inputs are activated by the "0" logic level. (For logic diagram see Figure 4-20.) If the clock falls when S_C and R_D are both low, a positive-going spike of approximately 120 nanoseconds and 2.6 volts amplitude will appear on the Q output. Conversely, if the clock falls when both R_C and S_D are low, a positive-going spike will appear on $\overline{Q}$. When not used the R_D or S_D input should be tied to V_{CC}. The R_D input may also be connected to the Q output if this is more convenient. This connection must be considered a loss of 1 for the "1" level fan-out and negates the output isolation.

8821, 8822, 8824

Asynchronous inputs are activated by a "0" level and are independent of the state of the clock. (For logic see Figure 4-21.)

8825

A logical "0" on the S_D line sets the Q output to a logical "1". (For logic diagram see Figure 4-22.) A logical "0" on the R_D line resets the Q output to logical "0". The clock input must be low when activating S_D and R_D. If the clock is high when activating these two inputs, both outputs may go to logical "0". In addition, when S_D or R_D are subsequently reactivated, the binary will return to its original state (prior to R_D or S_D activation).

8826, 8827

A logical "0" on the RESET (R_D) line resets the Q output to a logical "0". (For logic diagram see Figure 4-24.) For the 8827, the SET (S_D) line sets the Q output to a logical "1". The R_D and S_D lines may be activated regardless of the state of the clock. If the clock falls while R_D is a logical "0" and J is a logical "1", a positive-going spike approximately 150 nanoseconds wide will appear at the Q output. If the clock falls when K is a logical "1" and S_D is a logical "0", the positive-going spike occurs on $\overline{Q}$.

8828, 8829

A logical "0" on the SET line sets the Q output to a logical "1". (Logic diagrams in Figures 4-23 and 4-25.) A logical "0" on the RESET line sets the Q output to a logical "0". The SET and RESET lines may be activated regardless of the state of the clock or the J and K inputs.

8H20, 8H21, 8H22

The S_D and R_D inputs are activated by logical "0"'s. They may be activated when the clock line is high or low; if the J and K inputs are at a logical "1" (both or either), a positive-going spike will occur at the output. The duration of this spike will normally be about 20 nanoseconds.

MONOSTABLE MULTIVIBRATOR

8162 MULTIVIBRATOR

The 8162 is a one-shot multivibrator with complementary outputs and optional 500-ohm load resistors. The output pulse width can be conveniently adjusted to conform to most one-shot application requirements. The 8162 provides high output duty cycle (75%) and complete isolation of the timing stage and the output stage, resulting in good fall time even with wide pulse width.

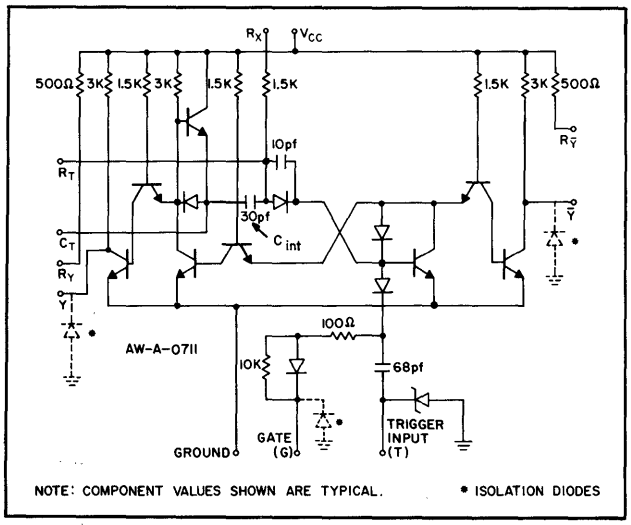


Figure 4-29

The 8162's clock can be driven by an 8000 Series element; the input is considered to be 2 AC loads (100 picofarad). The clock pulse width should be at least 50 nanoseconds wide, with a fall time of less than 75 nanoseconds.

When the gate input is low, the clock line is enabled. The clock is inhibited whenever the gate input is more positive than the clock input. Therefore gate input driver must have a higher output voltage than the clock driver.

The 8162 provides complementary outputs with passive 3K-ohm pull-up resistors. This allows collector logic with the DCL bare collector gates (see discussion of 8415, 8417, 8471, 8481 and 8881 gates).

An optional 500-ohm pull-up resistor is provided at each output, to be used when driving heavy capacitance loads where rise times must be maintained.

The 8162 design employs a 30 picofarad timing capacitor and an optional 1.5K-ohm timing resistor. The output pulse width may be varied by appropriate connections at the C_t, R_t, R_y and $R_{\overline{y}}$ terminals.

Use the following equations to obtain a desired pulse width:

A. with internal resistor R_X connected to V_{CC}:

$$PW \approx (0.85)(C_X + C_{int})(10^{-3} \text{ sec}/\mu f)$$

B. with external resistor R_X' (> 1KΩ) paralled with internal resistor R_X connected to V_{CC}:

$$PW \approx \frac{(0.85)(C_X + C_{int})(R_X') \text{ msec}/\mu f)}{1.5K + R_X'}$$

C. with external resistor R_X' (0.5KΩ < R_X' < 4.7KΩ) connected between R_T and V_{CC}, internal resistor R_X not connected:

$$PW \approx \frac{(0.85)(C_X + C_{int})(R_X') \text{ msec}/\mu f}{1.5K}$$

where:

PW = pulse width. Pulse width tolerance using the internal resistor R_X is about ±25% (unit to unit variations). Using external timing resistor R_X', a tolerance of less than ±10% may be obtained.

C_{int} = internal capacitance, typically 30pf.

C_X = external capacitance in microfarads connected between C_T and R_T.

R_X' = external resistor connected between R_T and V_{CC}.

INTERFACE ELEMENTS

8T18 Interface Element

The 8T18 provides an interface from high level (30-volt) inputs to low level (5-volt) outputs, and thus complements the 8T80 and 8T90. A typical application is shown below:

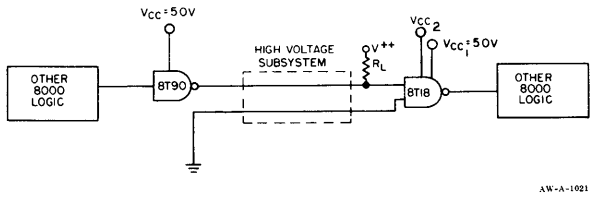


Figure 4-35 *

The V_{CC} is returned to a power supply of 20 volts or more. If V^{++} voltage exceeds 30 volts, a series current limiting resistor (to limit current to less than 2 milliamps) or a 20 to 30-volt Zener diode (shunt) must be used. The inputs of the 8T18 are rated at 50 volts reverse breakdown. The threshold voltage of the 8T18 (6.5 volt minimum) is independent of temperature since the various internal junctions are equal in number and opposite in polarity. Thus the 8T18 can be used as an accurate high-level threshold detector.

*Figures 4-30 through 4-34 have been deleted.

8T80, 8T90 Interface Element

The 8T80 Quad 2-Input NAND Gate and the 8T90 Hex Inverter provide low level (5-volt) inputs and high level (30-volt) outputs. A curve of typical output currents vs. saturation voltages at three temperatures is shown below:

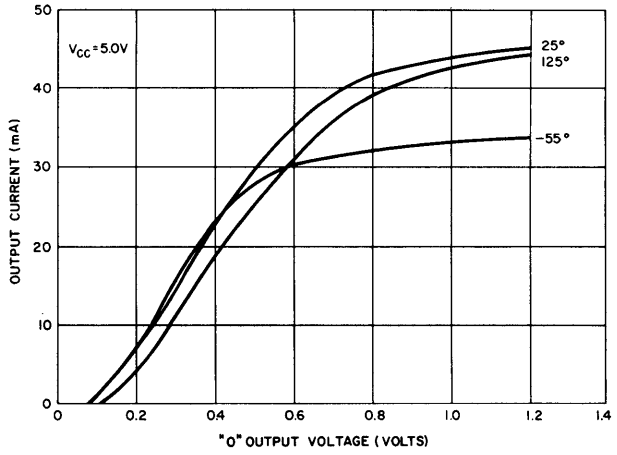


Figure 4-36

In designing for maximum current, the maximum device dissipation rating of 167 milliwatts at 125°C must not be exceeded. Each gate draws 20 milliwatts from the V_{CC} power supply when turned on with "0" level collector current. If all six inverters are on at the same time, the device is dissipating 6 times 20 = 120 milliwatts. Therefore 167 minus 120 or 47 milliwatts are available for collector circuit dissipation. The sensitivity is typically 5mA/volt at a 1 volt collector saturation level. Additional applications may be found in the "Sub-Systems" portion of this section.

SUB-SYSTEMS

Following are some typical sub-systems which can be implemented with 8000 Series elements. Further information on sub-systems may be obtained from Signetics Applications Department.

COUNTERS

Synchronous BCD Decade Up Counter

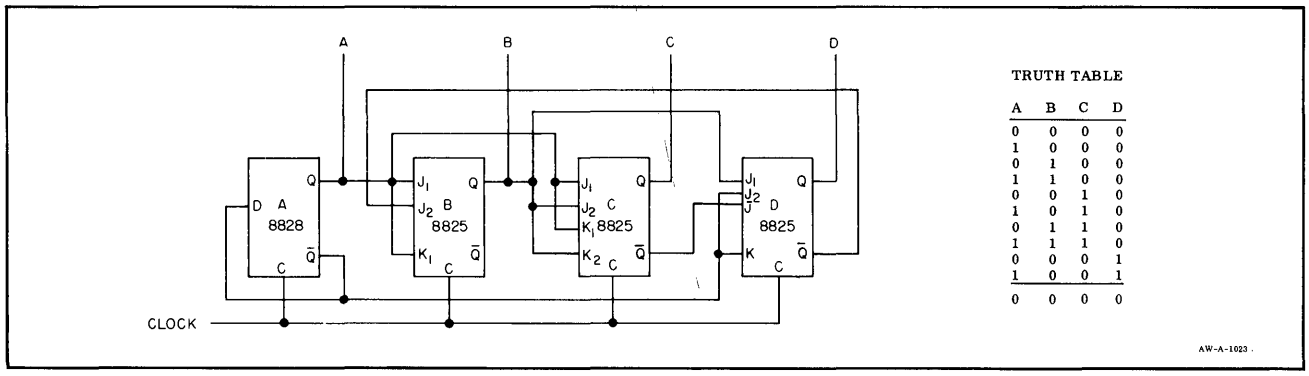
This design (shown in Figure 4-38) utilizes the built-in AND gates of the 8825. The first stage is implemented with one-half 8828 (D) binary as a part saving. Both the 8825 and 8828 are positive edge triggered binaries.

Synchronous BCD Decade Up-Down Counter

Any J-K binary may be used in this design (shown in Figure 4-39), although dual binaries are recommended in order to minimize part count.

Asynchronous BCD Decade Up Counter (Low Power)

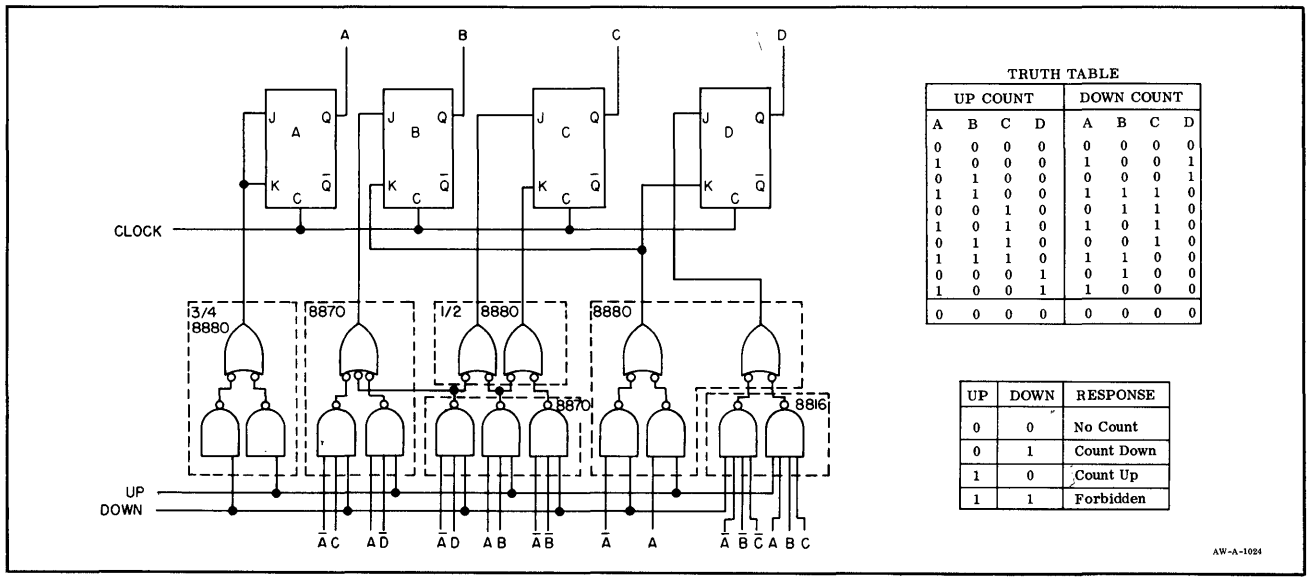
8400 elements can be used for low-power BCD decade counters. This one (shown in Figure 4-40) incorporates 8424 Dual RS/T Binaries and an 8480 Quad 2-Input NAND Gate.



TRUTH TABLE

A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	0	0	0

Figure 4-38



TRUTH TABLE

UP COUNT				DOWN COUNT			
A	B	C	D	A	B	C	D
0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1
0	1	0	0	0	0	0	1
1	1	0	0	1	1	1	0
0	0	1	0	0	1	1	0
1	0	1	0	1	0	1	0
0	1	1	0	0	0	1	0
1	1	1	0	1	1	0	0
0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	0
0	0	0	0	0	0	0	0

UP	DOWN	RESPONSE
0	0	No Count
0	1	Count Down
1	0	Count Up
1	1	Forbidden

Figure 4-39

Asynchronous Divide-By-16 Up Counter

This counter (shown in Figure 4-41) makes use of the 8828 Binary which is leading edge triggered. The clock must therefore be driven by the $\overline{Q}$ output of the previous stage to perform the up count. If a down count is required, the clock must be driven by the Q output of the previous stage. This applies to all leading edge triggered systems. Speeds of this 8828 counter are typically 25MHz.

Synchronous Divide-By-32 Up Counter

In this counter (see Figure 4-42), the first two stages are implemented with dual J-K flip-flops as a part savings. The third and fourth stages utilize the 8829, which requires no external gating because of its built-in AND gates. The fifth stage, another 8829, requires only one external NOR gate.

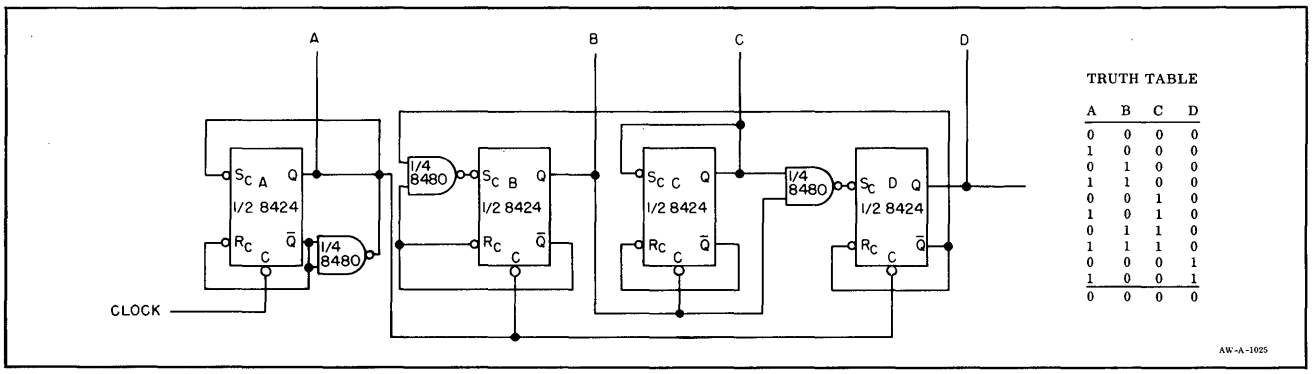


Figure 4-40

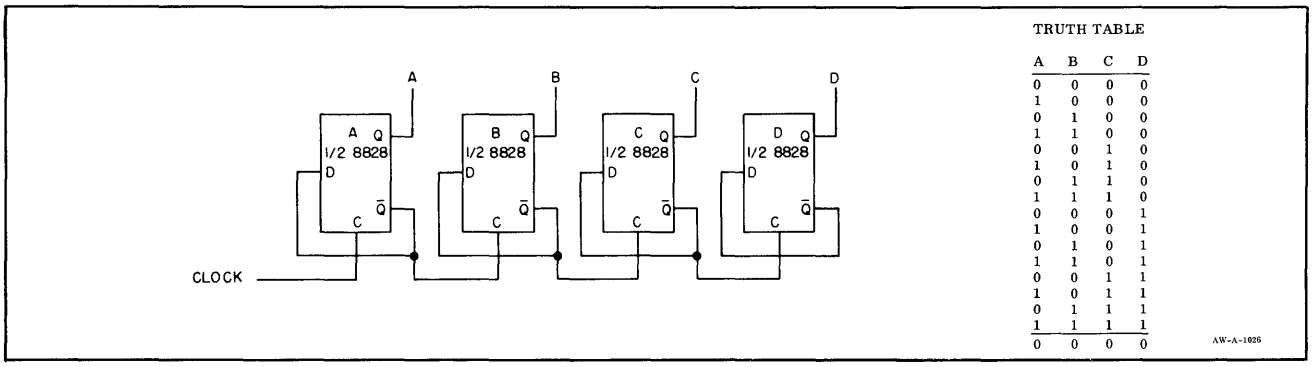


Figure 4-41

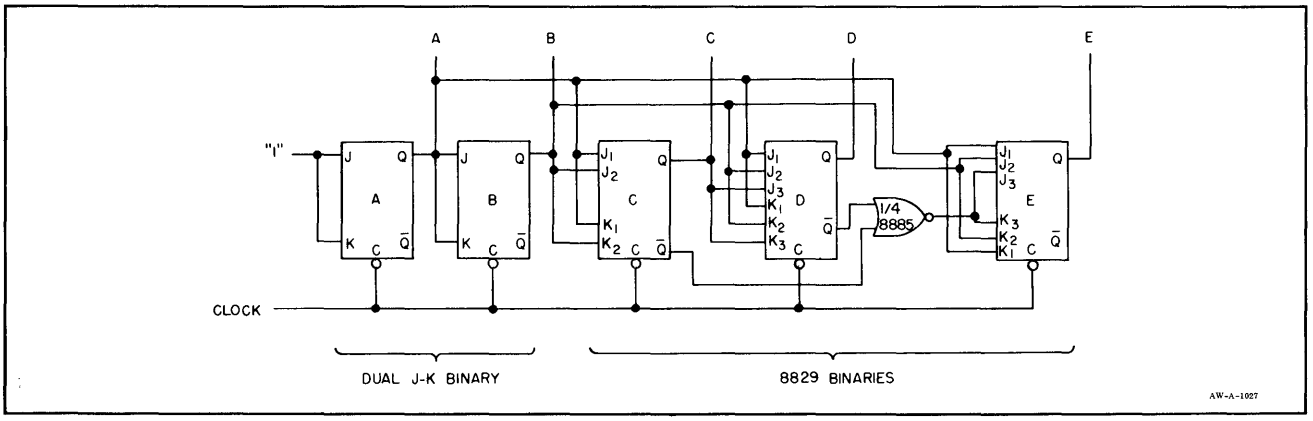


Figure 4-42

Binary Up-Down Counter

This counter (see Figure 4-43) is a modified ripple type counter which can be switched from up to down, or down to up, without causing incorrect counts. Whenever the clock line is logical "0", all flip-flop clock inputs are unconditionally logical "0". The gating structure for each flip-flop is the same, hence it is very simple to add stages to the counter.

Dual J-K, or RS/T, binaries may be used. They must be connected in the T configuration discussed under "Binaries."

5-Bit Ring Counter, Self-Starting and Correcting

This ring counter (see Figure 4-44) features low package count, high speed operation, and self-starting and correcting. Self-starting and correcting is accomplished by the gating structure in the feedback loop. The gates enter "0"s into the A binary until all inputs to the 8816 gate are "1"s. At that time, all binaries are in the "0" state except the binary that is not connected in the feedback loop. The next clock pulse loads a "1" into the A binary which is the first state in the truth table. The counter can be implemented with any dual J-K or RS/T binaries.

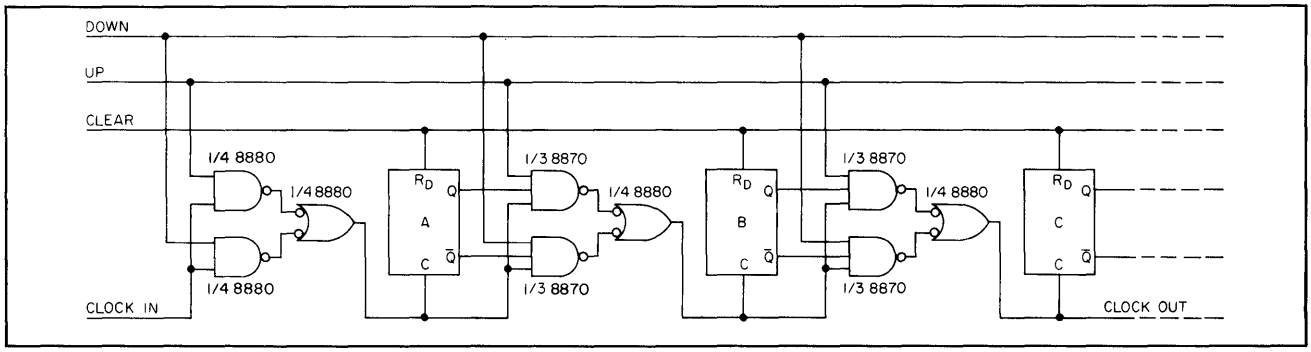
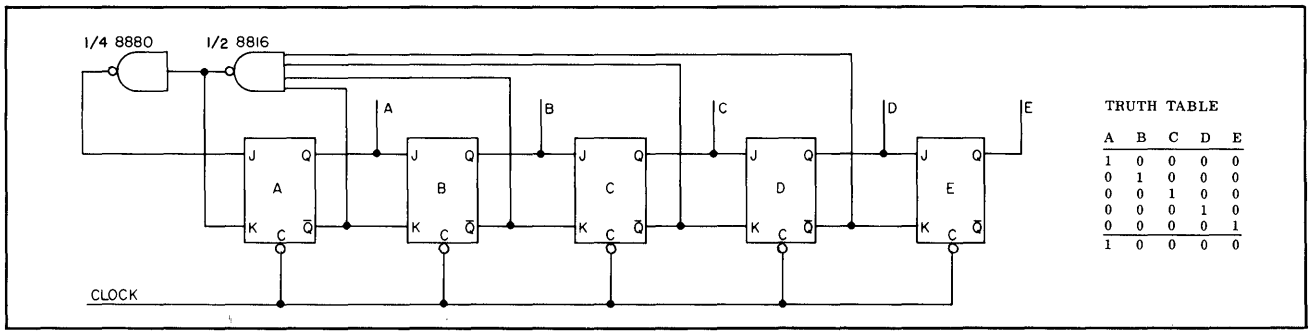


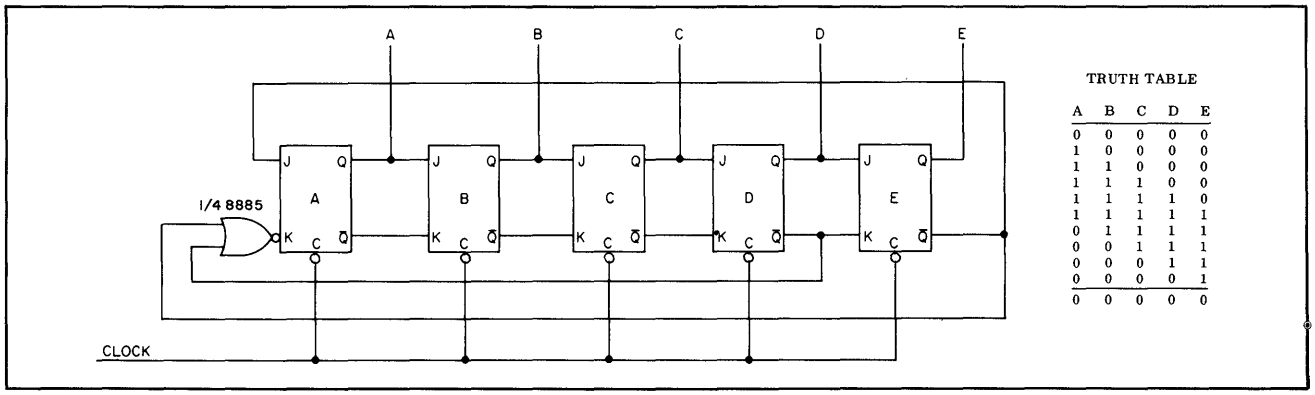
Figure 4-43



TRUTH TABLE

A	B	C	D	E
1	0	0	0	0
0	1	0	0	0
0	0	1	0	0
0	0	0	1	0
0	0	0	0	1
1	0	0	0	0

Figure 4-44



TRUTH TABLE

A	B	C	D	E
0	0	0	0	0
1	0	0	0	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0
1	1	1	1	1
0	1	1	1	1
0	0	1	1	1
0	0	0	1	1
0	0	0	0	1
0	0	0	0	0

Figure 4-45

Twisted Ring Counters

Twisted ring counters provide a count of 2N for N binary bits. This is generally accomplished by feeding back Q to K and $\overline{Q}$ to J. In some instances, the counter may have sub-loop conditions other than those shown in the truth table. To avoid these conditions, a self-correcting configuration such as that shown in Figure 4-45 should be used.

To arrive at this configuration, use the following procedure:

1. Run one feedback loop from the last bit $\overline{Q}$ to the first bit J.
2. Take the next largest integer above $\frac{N}{3}$, where N is the number of binary bits, and run that many feedback loops from $\overline{Q}$ to the NOR gate. The loops are connected by starting with the last bit and working back. In Figure 4-45, N is 5, so 5/3 is 1-2/3, and the number of feedbacks required is 2. Hence, feedback loops are connected from the last and next to the last $\overline{Q}$s. If N were 6, the number would be 3.

Counters in Cascade

The cascade configuration is applicable for either the 8280 or the 8281 (BCD mode shown in Figure 4-46). Some applications require a counter which counts a foreshortened sequence on the first cycle, but on subsequent cycles counts the full sequence. The 8280 and 8281 are well suited to these applications: the starting count is simply preset, then the normal modulus feedback is allowed to occur for modulus counting.

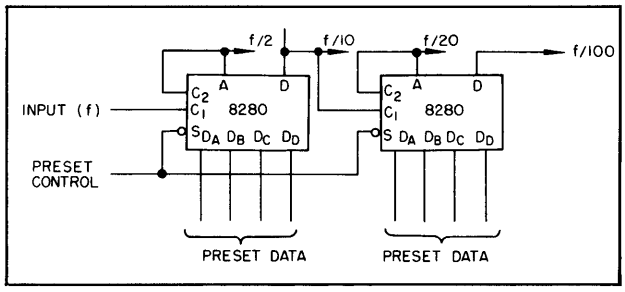


Figure 4-46

Count, Store and Decode

The count, store, and decode operation illustrated in Figure 4-47 shows the suitability of the 8280, 8281, 8270, 8271, and the 8T01 for these purposes. The parallel transfer to the storage element can be made synchronous with the clock and accomplish a parallel transfer during the normal counting interval of the counter. This technique is sometimes used to obtain time differences since the count stored can later be subtracted from the final count of the counter; or it can be decoded and displayed as shown.

Variable Modulus Counter

Both the counting and the unique parallel entry capabilities of the 8280 and 8281 counters are utilized in the variable modulus counter as shown in Figure 4-48. A variable modulus counter is one which can be made to count by any number. For the counter shown, any modulus between 1 and 160 may be used. Larger moduli require only an increase in the number of counting elements.

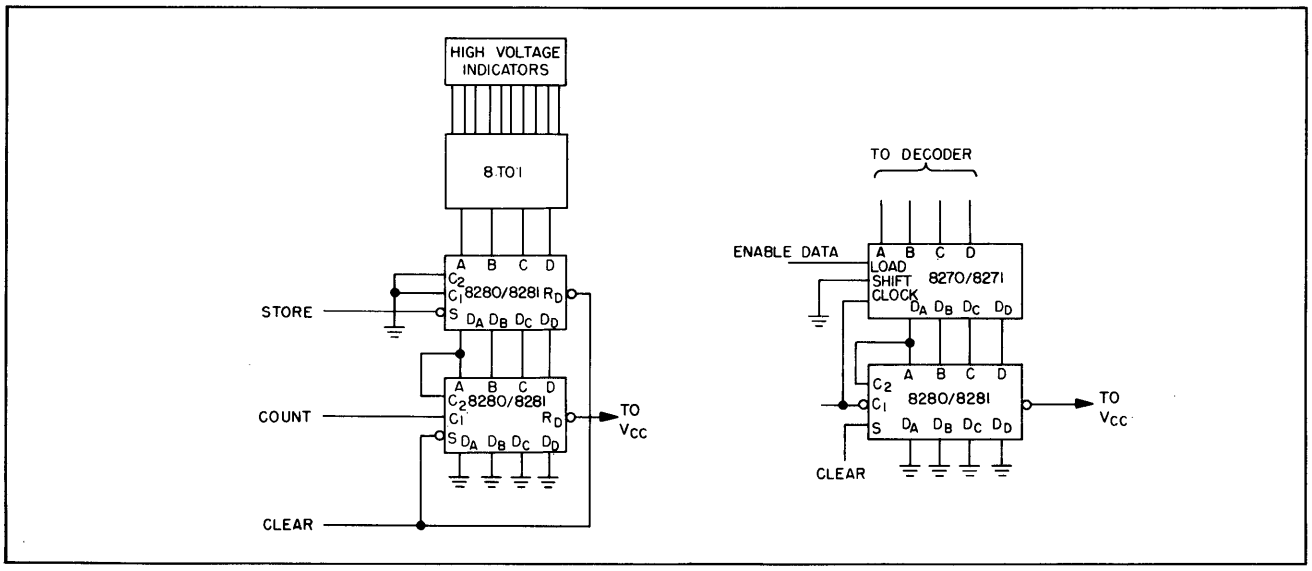
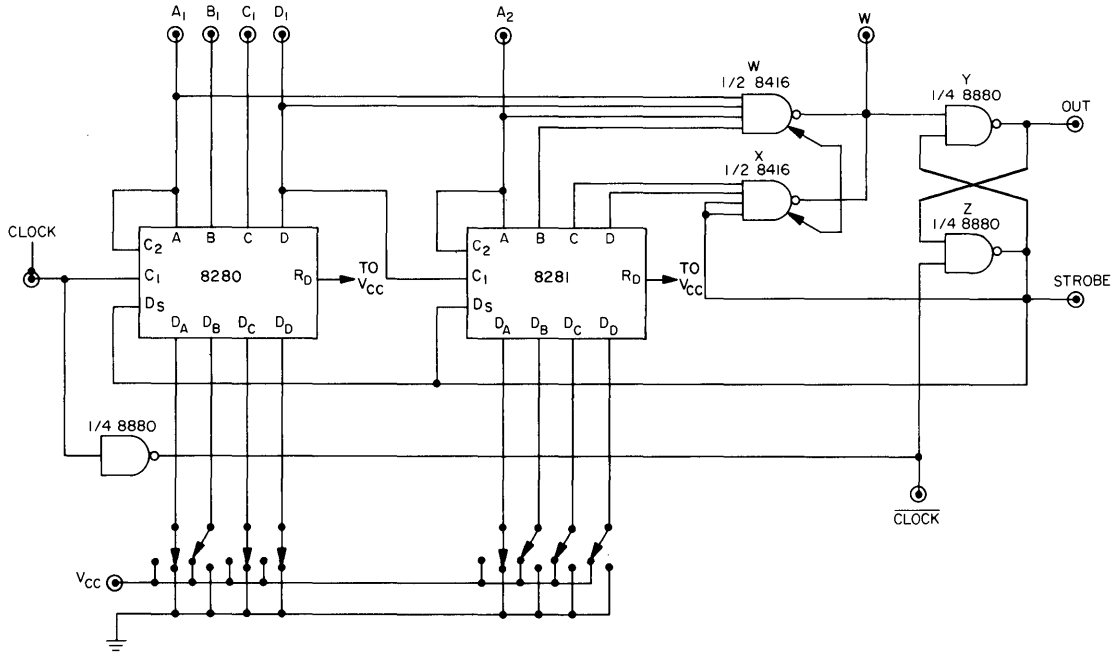
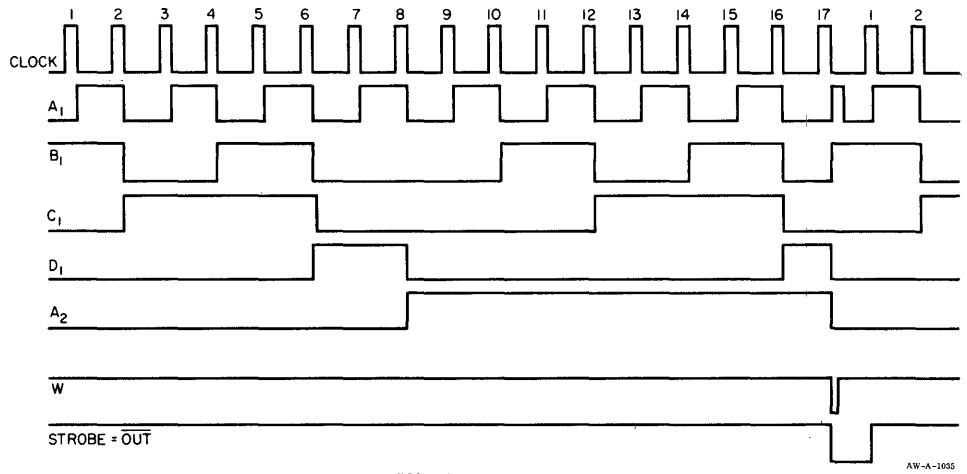


Figure 4-47

The variable modulus is attained by using the last count in the natural sequence of the counter to force the counter to a state corresponding to the first count in the sequence of the desired length. For example, if we want to divide (count) by 17, we would have to detect the 159th count and force the counter to reset to 142 before the next clock. To do this, we make use of the parallel inputs by simply coding the desired starting number into them. The specific operation is as follows: As indicated earlier, the natural sequence length of the counter shown in 160 (i.e., modulo 10 times modulo 16). Gates W and X constitute a detector for state 159, their output going low on that count. This causes the latch formed by Y and Z to be set. The output of the latch drives the strobe inputs of the 8280 and 8281 permitting the levels that were coded into the parallel inputs (corresponding to the number 142) to enter. The next clock pulse resets the latch and the counter picks up its natural sequence starting in this example with 142. Maximum speed is typically 4MHz.



Variable Modulus Counter



Timing Diagram

Figure 4-48

SHIFT REGISTERS

Serial-In, Parallel-Out

In Figure 4-49, shift registers are implemented with RS/T, J-K, or D binaries. This function may also be implemented with the 8270 or 8271 shift register.

Left-Right, Parallel Entry

Figure 4-50 shows a left-right shift register, with parallel entry that is implemented with the 8270 and 8271 shift registers, and 8840 and 8880 gates.

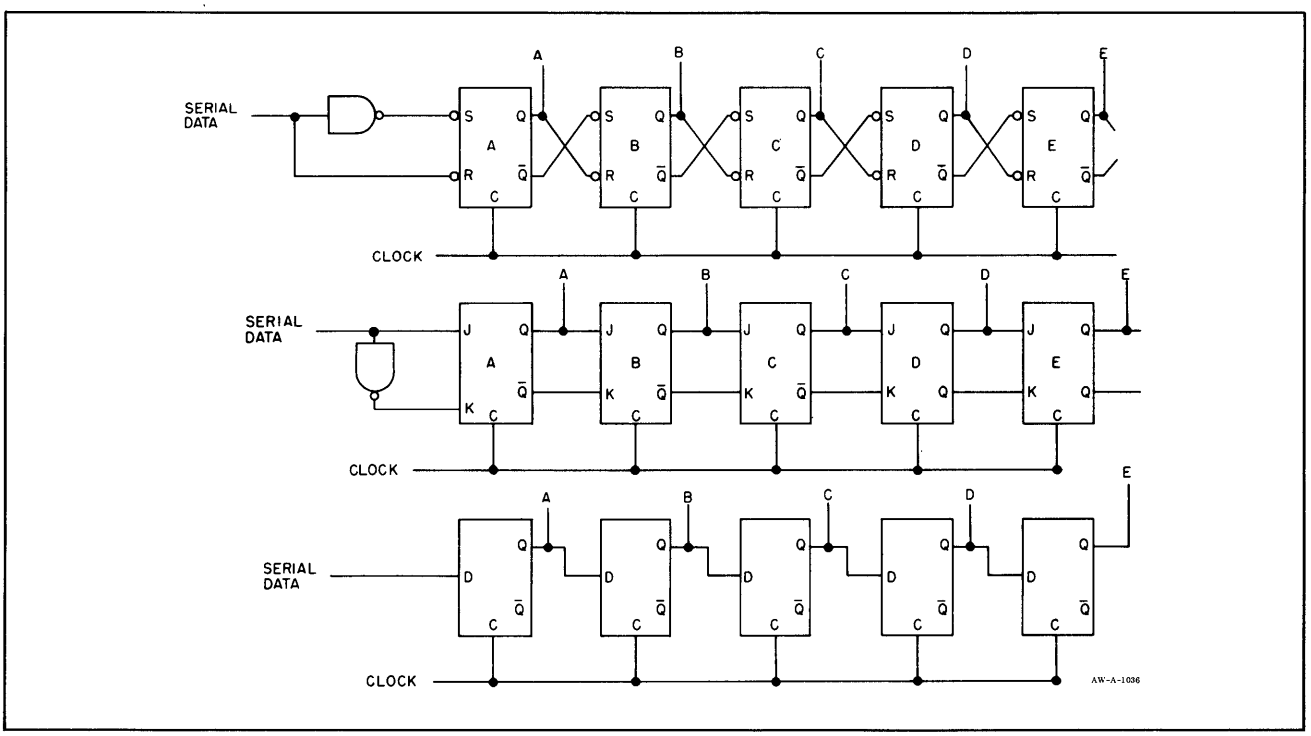


Figure 4-49

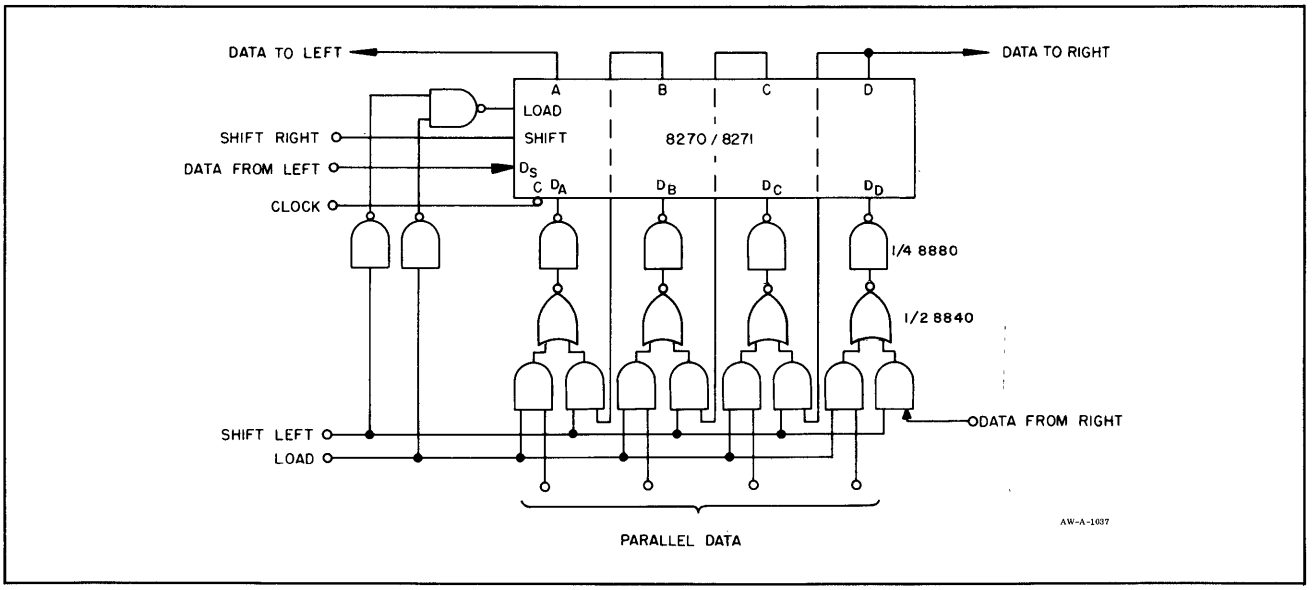


Figure 4-50

PARALLEL BINARY ADDER

The carry propagation delay is minimized by alternating between Carry and $\overline{\text{Carry}}$ in the carry propagation delay path as shown in Figure 4-51. It is necessary to alternate the polarity of inputs A and B from stage to stage to do this. The carry propagation delay is determined by the 8840. The 8840 delay is equivalent to one level of logic; therefore, the carry propagation per stage is one gate delay. Alternating the Q and $\overline{Q}$ of the 8828 flip-flop eliminates the need for inverting Sum outputs.

PARALLEL COMPARATOR

The parallel comparator (Figure 4-52) is most useful in high speed systems. All bits are compared simultaneously and the speed is limited only by two propagation delays per stage. The appropriate output (less than, equal to, greater than) will be a logical "1", and the other two outputs will be a logical "0" upon completion of the comparison.

DECODERS

Serial and Parallel Gray-To-Binary Decoders

In Figure 4-53, the serial gray-to-binary conversion must begin with the most significant bit. Also a Clear pulse must be provided prior to the first serial bit.

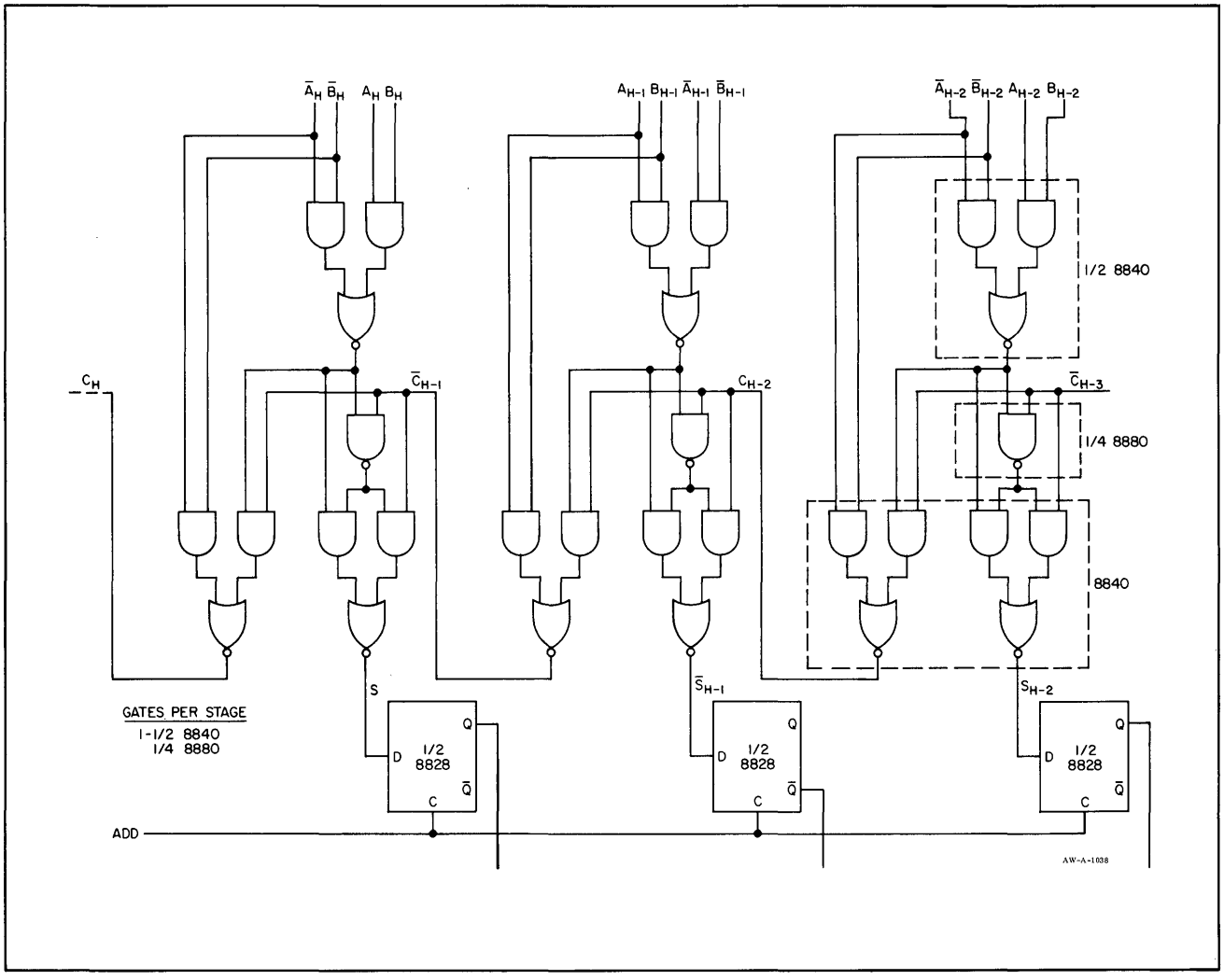
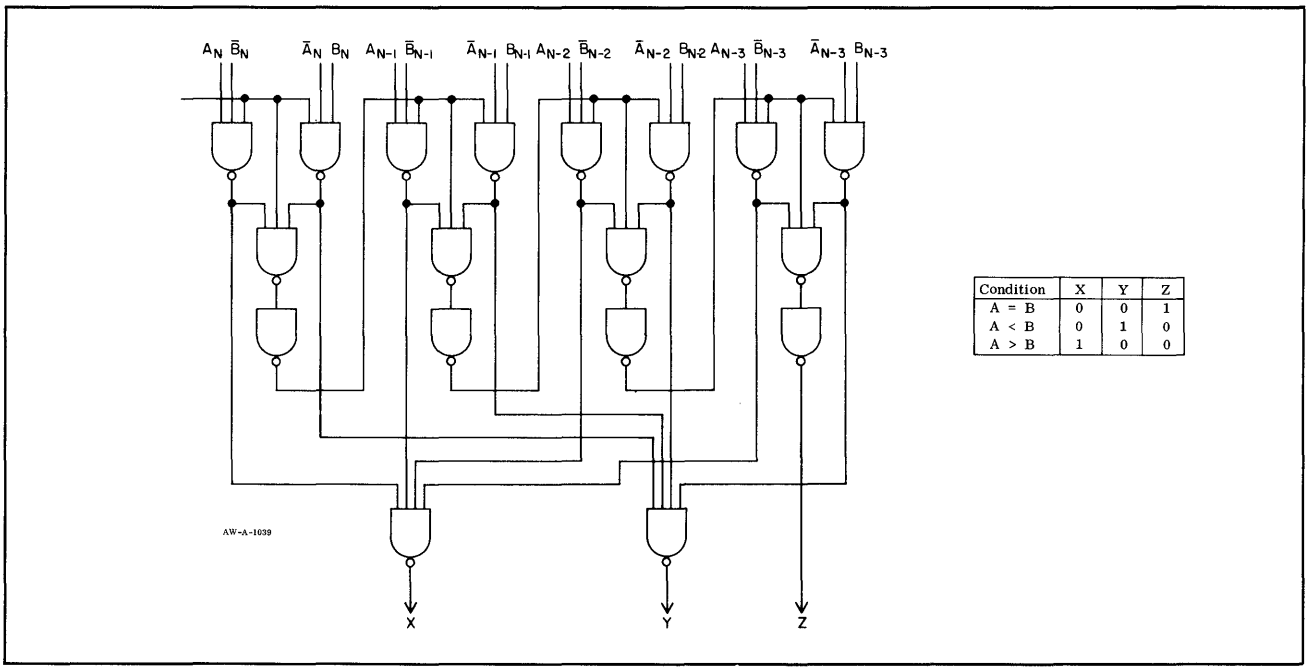
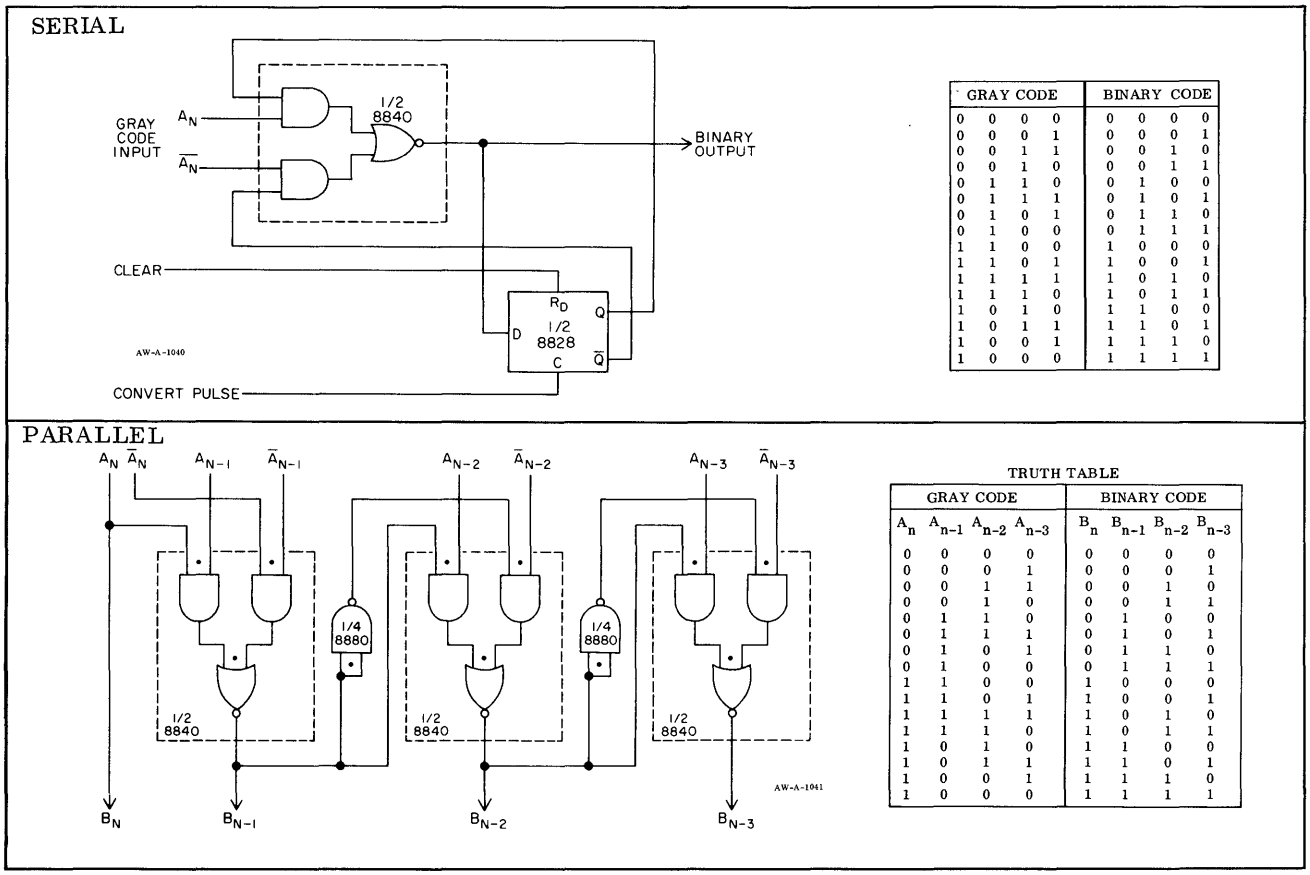


Figure 4-51



Condition	X	Y	Z
A = B	0	0	1
A < B	0	1	0
A > B	1	0	0

Figure 4-52



GRAY CODE				BINARY CODE			
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

TRUTH TABLE

GRAY CODE				BINARY CODE			
A_n	A_{n-1}	A_{n-2}	A_{n-3}	B_n	B_{n-1}	B_{n-2}	B_{n-3}
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Figure 4-53

LINEAR

The Signetics Linear Product Line provides all of the most frequently required circuit functions.
Linear products are generally available in both Military and Commercial temperature ranges and in a wide variety of package types.

SENSE AMPLIFIERS

528 (4 Channel Plated Wire)
7520 through 7525 (Core)

COMPARATORS

518 (Adjust Sinking)
526 (High Speed)
529 (Ultra High Speed)
5710 (μA710)
5711 (μA711)

CORE DRIVERS

75324 (SN75324)
75450 (SN75450)
75451 (SN75451)
75452 (SN75452)

VOLTAGE REGULATORS

550
5109 (LM109)
5723 (μA723)

OPERATIONAL AMPLIFIERS

516 (Differential IN/OUT)
531 (High Slew Rate)
533 (Micro Power)
536 (FET Input)
537 (Precision)
51A1 (LM101A)
5101 (LM101)
5107 (LM107)
51A8 (LM108A)
5108 (LM108)
5556 (MC1556)
5558 (Dual)
5709 (μA709)
5740 (μA740)
5741 (μA741)
5748 (μA748)

AMPLIFIERS

VIDEO
501
5733 (μA733)
DIFFERENTIAL
515
511 (Dual)
RF/IF
510 (Dual)
POWER DRIVER
540

PHASE LOCKED LOOP

560, 561, 562 — Operating Frequency .01Hz to > 30MHz, Sensitivity 300μV
565 — Operating Frequency .001Hz to 500kHz, Sensitivity 1 mV
566 (Function Generator)
567 (Tone Decoder)

MULTIPLIERS/DEMODULATORS

5595 (MC1595) 4 Quad multiplier
5596 (MC1596) Balanced modulator
5111 (LM2111) Limiter-Detector

SECTION V-SURE* PROGRAM

The Signetics SURE* Program consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability in Signetics products. These tests are made regularly at no extra cost to the user and are performed in addition to the 17 quality assurance inspections and tests to which every circuit is subjected before final seal. The tests, tabulated below for the specifier's convenience, are performed in accordance with the following conditions, sequence, and schedules on equipment calibrated to meet all requirements of MIL-Q-9858A and MIL-C-45662A.

Every circuit of every lot is processed to the environmental screens shown in Table I. These screens are performed in production, subsequent to assembly and just prior to 100 percent final production electrical tests. Any unit failing either the environmental screens or the final production electrical tests is rejected and removed from the lot.

After completion of Table I tests, each manufacturing lot is sampled and tested by Quality Assurance for conformance to the requirements of Table II. The unsampled portion of the lot is held pending acceptance of the lot sample. Detailed electrical test limits and conditions applicable to each subgroup are shown in the Electrical Characteristics table of the individual part type data sheets.

Group B Inspection shown in Table III is a complete environmental series in accordance with MIL-S-19500 and MIL-STD-750. These tests are performed once in every 28-day manufacturing period on a production lot of a representative circuit type. The circuit type selected each period is changed routinely and is representative of all structurally similar devices produced on the same line by the same processes during that period. A summary of these test results is available on request at the time of order placement.

Group C tests (Table IV) are intended to verify design parameters that are not specifically measured in Group A or B but are guaranteed by consideration of related measurements in those two series. These tests are performed every 90 days on at least one lot of every circuit type produced during that period.

For those with ultra-high reliability requirements, an additional preconditioning series, including operating burn-in and X-Ray, applicable to every circuit to be shipped, is available at extra cost. Details are given under Optional Preconditioning Series (Table V).

*Systematic Uniformity and Reliability Evaluation

TABLE I – 100% PRODUCTION SCREEN TESTS

Thermal Shock:	5 cycles; 60 seconds at 0°C, 60 seconds at 100°C, transfer time 5 seconds (J, Q, and R packages only)
Centrifuge:	y_1 axis; 30,000 g minimum (J, Q, and R packages only)
Hermeticity:	Gross leak test (J, Q, and R packages only)
	Above series performed prior to FINAL ELECTRICAL TESTS

TABLE II – GROUP A, PRODUCT ACCEPTANCE TESTS

SUB-GROUP	TEST	CONDITIONS	LIMITS	AQL	INSPECTION LEVEL
A-1	Visual and Mechanical Inspection	Per MIL-STD-750, Method 2071	Note 2	1.0%	II
A-2	DC Parameters	T = +25°C; Note 1	Note 2	1.0%	II
A-3	DC Parameters	T = +25°C; Notes 1, 3	Note 2	1.0%	II
A-4	DC Parameters	T = +125°C; Note 1	Note 2	1.0%	II
A-5	DC Parameters	T = -55°C; Note 1	Note 2	1.0%	II
A-6	AC Parameters	T = +25°C; Note 1	Note 2	1.0%	II

TABLE III – GROUP B, ENVIRONMENTAL QUALIFICATION TESTS PER MIL-S-19500D

SUB-GROUP	TEST	CONDITIONS	MIL-STD-750 METHOD	LIMITS	LTPD	MAX. ACCEPTANCE NUMBER
B-1	Physical Dimensions		2066		15	1
B-2	DC Parameters	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	Solderability	All terminals	2026			
	Temperature Cycling	10 cycles, T_{max}=+175°C	1051			
	Thermal Shock	T_{min}=-70°C T_{max}=+100°C 5 cycles, 1 minute at each extreme Transfer time = 5 sec. max.	1056			
	Moisture Resistance	Omit initial conditioning	1021		15	1
	Electrical End Points	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	FAILURE CRITERIA	"1" Input Current		10X Initial Value for DTL 5X Initial Value for TTL		
		"1" Output Voltage		±20% Initial Value		
		"0" Input Current		±20% Initial Value		
		"0" Output Voltage		±0.1V		
		Expansion Node Current (as applicable)		±20% Initial Value		

SUB-GROUP	TEST	CONDITIONS	MIL-STD-750 METHOD	LIMITS	LTPD	MAX. ACCEPTANCE NUMBER
B-3	DC Parameters	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	Shock	1500g; 5 blows ea. x_1, y_1, z_1; 0.5ms	2016			
	Vibration Fatigue	30 g; non-operating	2046			
	Vibration, Var. Freq.	30 g;	2056		15	1
	Acceleration	30,000 g; 1 min. ea. x_1, y_1, z_1	2006			
	Electrical End Points	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	FAILURE CRITERIA	Same as B-2				
B-4	Terminal Strength	Test Condition E; weight = 4 oz.	2036			
	Hermeticity *	Per MIL-STD-202, Method 112C				
	Small Leak	Condition C; Procedure 111A		5×10^{-8} cc/sec. max.	15	1
	Large Leak	Condition A; Ethylene Glycol				
B-5	Salt Atmosphere		1041		15	1
B-6	DC Parameters	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	Storage Life	1000 hours at T_{min}=+150°C	1031		λ=15	
	Electrical End Points	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	FAILURE CRITERIA	Same as B-2				
B-7	DC Parameters	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	Operating Life	1000 hours at T_{min}=+125°C; Dynamic operating at 100 KHz	1026		λ=10	
	Electrical End Points	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	FAILURE CRITERIA	Same as B-2				

TABLE IV – GROUP C, DESIGN TESTS

SUB-GROUP	TEST	CONDITIONS	LIMITS	AQL	INSPECTION LEVEL
C-1	DC Parameters	Note 1	Note 2	1.0%	II
C-2	AC Parameters	Note 1	Note 2	1.0%	II

OPTIONAL HIGH RELIABILITY SCREENING

To maximize reliability in critical applications the Optional High Reliability Screening Series of Table V provides for 100 percent screening at extra cost. This series eliminates the necessity for special specifications, minimizes cost and provides the shortest possible delivery time. This series is applied after the normal GROUP A acceptance tests. Circuits subjected to this PRECONDITIONING SERIES are clearly distinguishable from standard products in the following ways:

1. Individual serial number on each circuit.
2. First letter of part number is R, i.e., RE180J.
3. Individual device variable parameter test data supplied with each shipment.

Consult your local representative for price information. Device types should be specified with R prefixes when ordering.

TABLE V – OPTIONAL HIGH RELIABILITY SCREENING

TEST	CONDITIONS	MIL-STD-750 METHOD	LIMITS	LEVEL
Thermal Shock	T_{min} = -70°C T_{max} = +100°C 5 cycles; 1 minute at each extreme Transfer Time = 5 sec. max.	1056		100%
Mechanical Shock	1500 g; 5 blows y_1; 0.5ms (G, J, K packages only)	2016		100%
Centrifuge	30,000 g, y_1 (G, J, K packages only)	2006		100%
Hermeticity *	Per MIL-STD-202, Method 112C			100%
Small Leak	Condition C, Procedure III a		5×10^{-8} cc/sec.	
Large Leak	Condition A, Ethylene Glycol			
Visual Inspection		2071		100%
DC Parameters	Per GROUP A, SUB-GROUP 3; Record Data		Notes 2, 3	100%
Capacitor Stress	24 hours; T_{min} = +125°C; DC Condition		Note 4	100%
Operating Burn-In	168 hours, +12 hrs. - 0 hr.; T_{min} = +125°C Dynamic operation at 100KHz	1026		100%
DC Parameters	Per GROUP A, SUB-GROUP 3; Record Data Apply failure criteria		Notes 2, 3	100%
GROUP A	Sample lot per Table II and perform A-2, A-4, A-5 and A-6 tests.		Note 2	A.Q.L. = 1.0% Level II
X-Ray	Per Signetics Specification 871004			100%
Visual Inspection		2071		100%

Notes:

1. All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL-C-45662A.
2. Detailed tests, conditions, and limits applicable to each sub-group are given in data sheet ELECTRICAL CHARACTERISTICS table.
3. These specific tests are used to determine Electrical End Points as required in GROUP B and OPTIONAL PRECONDITIONING SERIES.
4. Applicable only to device types incorporating MOS capacitors.

* For silicone molded package integrated circuits, the MIL-STD-202, Method 112 hermeticity tests are not employed due to the product's solid package construction. For subgroup B4, a 1-hour, 50 psi detergent bomb test has been incorporated into the SURE Program for this product. Test methods are being evaluated in order to determine a suitable nondestructive seal integrity test for inclusion into the Table V 100% screening series.

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