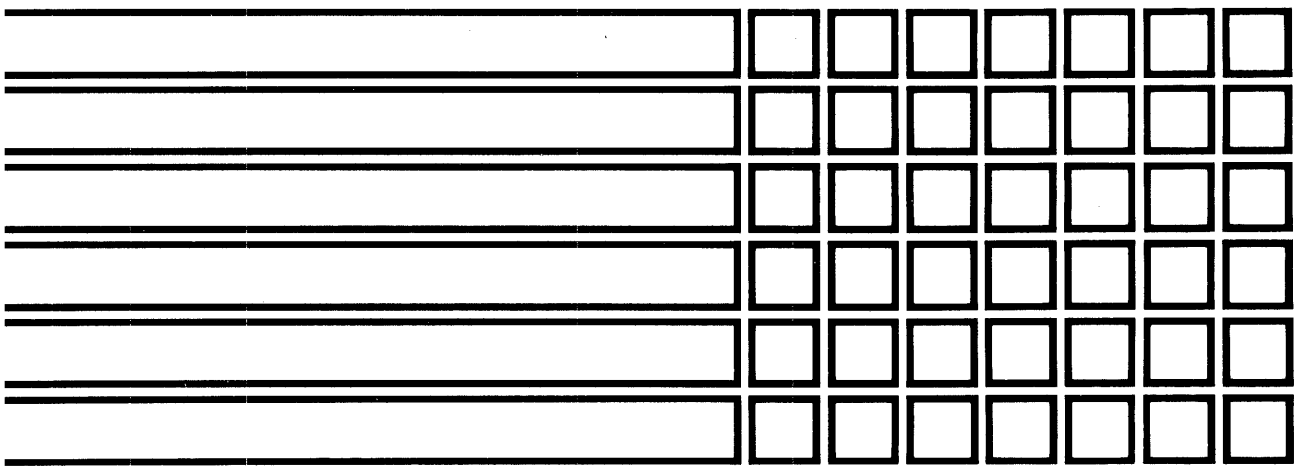
SIGNETICS BIPOLAR/MOS MICROPROCESSOR DATA MANUAL



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The present rapid growth of the electronic design revolution is being fueled by the microprocessor/microcomputer. As one of the industry leaders, Signetics gives new impetus to advancing the state-of-the-art with its technological strength, product depth and manufacturing know-how. We continue to develop all aspects of the microprocessor/microcomputer area, simultaneously providing products, ready-to-use training, software and development tools that help you to understand and apply Signetics advanced products.

This Microprocessor Data Manual will enable you to examine Signetics complete line of Bipolar and MOS Microprocessors, as well as a full line of support products. Each data sheet fully explains the operation of each product and contains application hints on how to best utilize the products' design advantages.

You will also find a variety of development systems, educational products, prototyping kits and software for both bipolar and MOS. And with a team of field application engineers throughout the country you will find that Signetics can provide you with the answer to your design problems.

We offer one of the broadest selections available of both bipolar and MOS microprocessor/microcomputers. Combined with our complete line of logic, analog, bipolar and MOS memories, a design engineer can select one source that will provide him with the best possible, cost effective solution to his design problems.

This book contains a compilation of all products currently available. Signetics is continuously developing new products. As you see new product announcements, you should contact your local Signetics sales office, representative or authorized distributor or write Signetics directly at 811 East Arques Avenue, Sunnyvale, California, 94086, for the latest technical information.

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CHAPTER 1
BIPOLAR Microprocessors, Peripherals and Development Products

Microcontrol and Arithmetic Units

The introduction of the Signetics Bit-Slice Microprocessors has brought new levels of high performance to microprocessor applications not previously possible with MOS technology. Combining the Schottky bipolar microprocessors with industry standard memory and support circuits, microinstruction cycle times of 100ns are possible.

In the majority of cases, the choice of a bipolar microprocessor slice, as opposed to an MOS device, is based on speed or flexibility of microprogramming. Starting with these characteristics, the design of the Signetics slice microprocessors has been optimized around the following objectives:

- Fast cycle time
- All memory and support chips are industry standard
- Cooler operation
- Lower total system cost

Furthermore, systems built with large-scale integrated circuits are much smaller and require less power than equivalent systems using medium and/or small scale integrated circuits.

Typically, slice microprocessors are employed in the realization of the Central Processing Unit (CPU) of a computer or for implementing dedicated smart controllers. The generalized and simplified structure of a CPU or "Smart" controller can be typically classified into 3 distinct but interactively related functional sections. These sections are generally referred to as the Processing section, the Control section, and the I/O and Memory Interface section. A simplified block diagram of a CPU is illustrated in Figure 1.

The major functions of the Processing section are to:

- provide data transfer paths;
- manipulate data through logic and arithmetic operations;
- provide storage facilities such as a register file; and
- generate necessary status flags based on the kind of operation performed by the ALU.

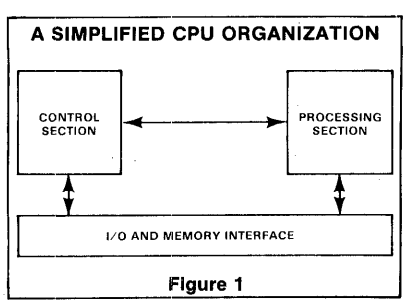


Figure 1

The major functions of the Control section are to:

- initiate memory or I/O operations;
- decode macroinstructions;
- control the manipulation and transfer of data;
- test status conditions; and
- sample and respond to interrupts.

The major functions of the I/O and Memory Interface section are to:

- multiplex data to the proper destination;
- provide bus driving/receiving capability; and
- provide latching capability.

With state-of-the-art bipolar Schottky technology, high-performance microprocessors are designed to perform functions of the Processing section. Due to the limitation on the number of pins and chip size, the overall Processing section is partitioned into several functionally equivalent slices. In today's bipolar microprocessor market, 2-bit and 4-bit slice architecture predominates. Each architecture type has its uniqueness but, in general, a slice contains a group of general purpose registers, an accumulator, special-purpose register(s) ALU and related status flags. All of these elements constitute the Processing section of a CPU. The flexibility of slice components allows the designer to construct a processing section of any desired width as required by his application.

The Control section of the CPU is more complex in design. Typically this section includes the macroinstruction decode logic, test-branch decode, microprogram sequencing logic, and the control store where the microprogram resides. Aside from the microprogram, the remaining portion of the Control section (macroinstruction decode and test-branch decode and sequencing logic), does not lend itself to efficient partitioning into vertical slices. This is due to the random nature of the logic usually found in the Control section. However, horizontal functional grouping is possible. For example, the macroinstruction decode and test-branch decode logic can now be replaced by the FPLA (Field Programmable Logic Array); the random logic traditionally needed to implement the microprogram sequencing can now be replaced by the Microprogram Control Unit; and, of course, the microprogram can be stored in high density PROMs or ROMs. Since the designer must define his own microstructure, the slice microprocessors permit fundamental optimizations to be made. With slice hardware, the designer may have no macroinstructions at all, placing all of the program in PROM for dedicated control applications. Or he may define, as required, any number of macroinstructions selected specifically for his particular processor purpose. Various minicomputers and several MOS microprocessors have been emulated using slice hardware.

The I/O and Memory Interface section consists mainly of I/O ports, high power bus drivers, receivers, and some temporary register storage facilities. Bidirectional and tri-state devices are the most popular logic elements for implementing this interface structure.

Figure 2 shows an LSI approach to the implementation of the same generalized CPU structure indicated earlier.

Data specifications for Signetics' line of slice microprocessor components are contained within this chapter. Included is the popular 3000 series Microprogram Control Unit and the 2-bit slice Central Processing Element. These Signetics devices feature improved performance specifications over 3000 series components available on the general market. Moreover, the unique Signetics XL plastic package design results in significantly cooler operation of the chip than was previously possible with other plastic package designs. This section also features the 8X02 Control Store Sequencer. This device may be used with any TTL compatible slice processing elements and features extreme ease of use. The 8 simple, yet powerful, instructions permit subroutining and looping (using internal stack), unrestricted jumping, unrestricted conditional branching and conditional instruction skipping.

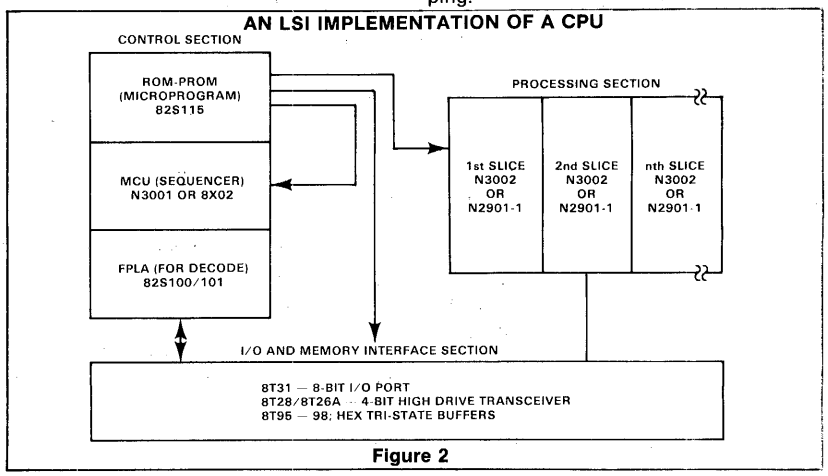


Figure 2

DESCRIPTION

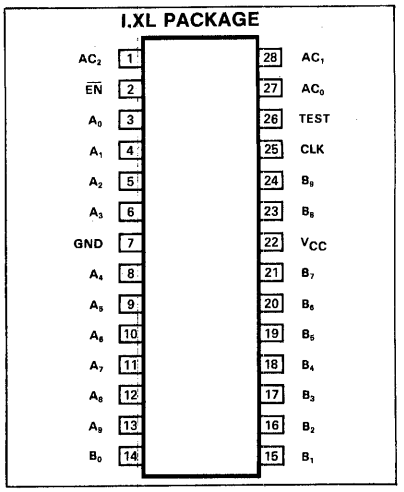
The Signetics 8X02 is a low power Schottky LSI device intended for use in high performance microprogrammed systems to control the fetch sequence of microinstructions. When combined with standard ROM or PROM, the 8X02 forms a powerful microprogrammed control section for computers, controllers, or sequential logic.

FEATURES

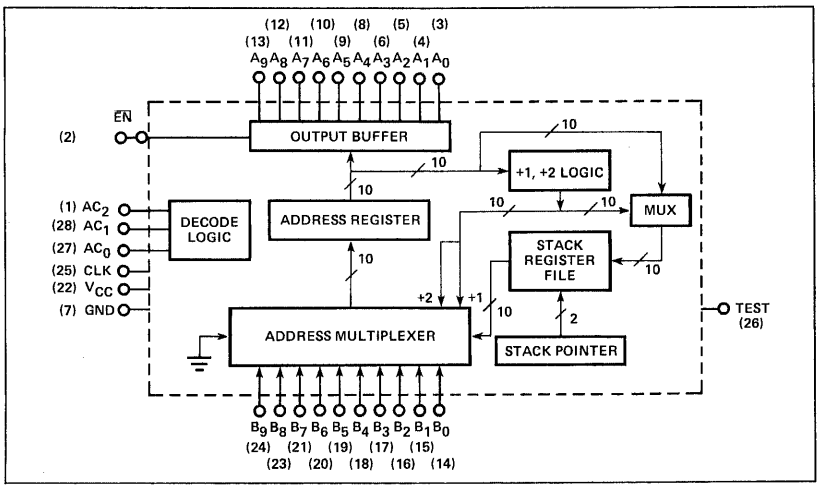
- **Low power Schottky process**
- **1024 microinstruction addressability**
- **N-way branch**
- **4-level stack register file (LIFO type)**
- **Automatic push/pop stack operation**
- **"Test and skip" operation on test input line**
- **3-bit command code**
- **Tri-state buffered outputs**
- **Auto-reset to address 0 during power-up**
- **Conditional branching, pop stack, and push stack**

PIN CONFIGURATION

I,XL PACKAGE



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
5-6 8-13	A_0-A_9	Microprogram Address outputs	Three-state Active high
1,28,27	AC_0-AC_2	Next Address Control Function inputs All addressing control functions are selected by these command lines.	Active high
14-21 23-24	B_0-B_9	Branch Address inputs Determines the next address of an N-way branch when used with the BRANCH TO SUBROUTINE (BSR) or BRANCH ON TEST (BRT) command.	Active high
2	$\overline{EN}$	Enable input When in the low state, the Microprogram Address outputs are enabled.	Active low
25	CLK	Clock Input—High to Low transition for stack operations, Low to High transition for address modification.	⊓
26	TEST	Test input Used in conjunction with four NEXT ADDRESS CONTROL FUNCTION commands to effect conditional skips, branches, and stack operations.	Active high
7	GND	Ground	
22	V_{CC}	+5 Volt supply	

FUNCTIONAL DESCRIPTION

The Signetics 8X02 Control Store Sequencer is an LSI device using low power Schottky technology and is intended for use in high performance microprogrammed applications. When used alone, the 8X02 is capable of addressing up to 1K words of microprogram. This may be expanded to any microprogram size by conventional paging techniques.

The Address Register consists of 10 D-type, edge-triggered flip-flops with a common clock. A new address is entered into the Address Register on the low-to-high transition of the clock. The next address to be entered into the Address Register is supplied via the Address Multiplexer.

The Address Multiplexer is a 5-input device that is used to select either the branch input, +1 adder, +2 adder, stack register file, or ground (all zeros) as the source of the next microinstruction address. The proper multiplexer channel is automatically selected via the Decode Logic according to the Address Control Function Input and Test Input line.

The +1, +2 logic is used to increment the present contents of the Address Register by 1 or 2, depending on the function input command. Thus, the next address to the Control Store ROM/PROM may be either the current address plus 1 (N+1) or the current address plus 2 (N+2). If the same Microprogram Address is to be used on successive occasions, the clock to the 8X02 must simply be disabled; therefore, no new address is loaded into the Address Register.

The Stack File Register is used to provide a return address linkage whenever a subroutine or loop is executed. The 4X10 stack operates in a last-in, first-out (LIFO) mode, with the stack pointer always pointing to the next address to be read. Operation of the stack pointer is automatically controlled by the Address Control Function Inputs. Since the stack is 4 words deep, up to 4 loops and/or subroutines may be nested.

The branch input is a 10-bit field of direct inputs to the multiplexer which can be selected as the next control store address. Using the appropriate branch command, an N-way branch is possible where N is the address of any microinstruction within the 1024 word microcode page. Likewise, the RESET command is a special case of an N-way branch in which the multiplexer selects an all zeros input, forcing the next microinstruction address to be zero.

The Test Input line is used in conjunction with the conditional execution of 4 Address Control Function commands. When the Test Input is false (low), the sequencer simply increments to the next address (N+1). When it is true (high), the sequencer executes a branch as defined by the input command, thereby transferring control to another portion of the microprogram.

All Address Output lines of the 8X02 are three-state buffered outputs with a common enable line ($\overline{EN}$). When the Enable line is high, all outputs are placed in a high-impedance state, and external access to the control store ROM/PROM is possible. This allows a preprogrammed set of microinstructions to be executed from external or built-in test equipment (BITE), vectored interrupts, and Writable Control Store if implemented.

NEXT ADDRESS CONTROL FUNCTION TABLE

MNEMONIC	DESCRIPTION	FUNCTION AC_2 1 0	TEST	NEXT ADDRESS	STACK	STACK POINTER
TSK	Test and skip	0 0 0	False True	Current + 1 Current + 2	N.C. N.C.	N.C. N.C.
INC	Increment	0 0 1	X	Current + 1	N.C.	N.C.
BLT	Branch to loop if test input true	0 1 0	False True	Current + 1 Stack reg file	X POP (read)	Decr Decr
POP	POP stack	0 1 1	X	Stack reg file	POP (read)	Decr
BSR	Branch to subroutine if test input true	1 0 0	False True	Current + 1 Branch address	N.C. PUSH (Curr + 1)	N.C. Incr
PLP	Push for looping	1 0 1	X	Current + 1	PUSH (Curr Addr)	Incr
BRT	Branch if test input true	1 1 0	False True	Current + 1 Branch address	N.C. N.C.	N.C. N.C.
RST	Set microprogram address output to zero	1 1 1	X	All O's	N.C.	N.C.

X = Don't care
N.C. = No change

FUNCTIONAL DESCRIPTION

The following is a description of each of the eight Next Address Control Functions (AC_2-AC_0)

MNEMONIC	FUNCTION DESCRIPTION
TSK	AC_{2-0} = 000: TEST AND SKIP Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer unchanged If test is True (High): Next Address = Current Address + 2 (i.e. Skip next microinstruction) Stack Pointer unchanged
INC	AC_{2-0} = 001: INCREMENT Next Address = Current Address + 1 Stack Pointer unchanged
BLT	AC_{2-0} = -010: BRANCH TO LOOP IF TEST CONDITION TRUE. Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer decremented by 1 If test is True (High): Next Address = Address from Stack Register File (POP) Stack Pointer decremented by 1
POP	AC_{2-0} = 011: POP STACK Next Address = Address from Stack Register File (POP) Stack Pointer decremented by 1
BSR	AC_{2-0} = 100: BRANCH TO SUBROUTINE IF TEST CONDITION TRUE. Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer unchanged If test is True (High): Next Address = Branch Address Input (B_{0-9}) Stack Pointer incremented by 1 PUSH (write) Current Address + 1 → Stack Register File
PLP	AC_{2-0} = 101: PUSH FOR LOOPING Next Address = Current Address + 1 Stack Pointer incremented by 1 PUSH (write) Current Address → Stack Register File
BRT	AC_{2-0} = 110: BRANCH ON TEST CONDITION TRUE Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer unchanged If test is True (High): Next Address = Branch Address Input (B_{0-9}) Stack Pointer unchanged
RST	AC_{2-0} = 111: RESET TO ZERO Next Address = 0 Stack Pointer unchanged

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-State output voltage	+5.5	Vdc
T_A	Operating temperature range	0° to +70°	°C
T_{STG}	Storage temperature range	-65° to +150°	°C

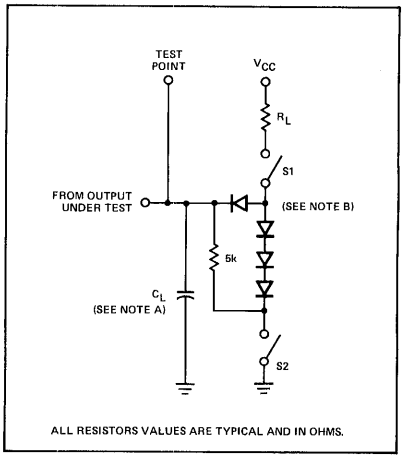
DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, $4.75 \le V_{CC} \le 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = 4.75V, I_I = -18mA			-1.5	V
V_{OH}	High level output voltage	V_{CC} = 4.75V, I_{OH} = -2.6mA	2.4			V
V_{OL}	Low level output voltage	V_{CC} = 4.75V, I_{OL} = 8mA			0.5	V
I_I	Input current at maximum Input voltage	V_{CC} = 5.25V, V_I = 5.5V			100	μA
I_{IH}	High level input current	V_{CC} = 5.25V, V_I = 2.7V				
	AC_2-AC_0, $\overline{EN}$, TEST				40	μA
	B_9-B_0				20	μA
	CLK				60	μA
I_{IL}	Low level input current	V_{CC} = 5.25V, V_I = 0.4V				
	AC_2-AC_0, $\overline{EN}$, TEST				-0.72	mA
	B_9-B_0				-0.36	mA
	CLK				-1.08	mA
I_{OS}	Short-circuit output current	V_{CC} = 5.25V	-15		-100	mA
I_{OZH}	High-Z state output current	V_{OUT} = 2.7V			20	μA
I_{OZL}	High-Z state output current	V_{OUT} = 0.4V			-20	μA
I_{CC}	Supply current	V_{CC} = 5.25V		165	200	mA

NOTE
1. All typical values are at V_{CC} = 5V, T_A = 25°C.

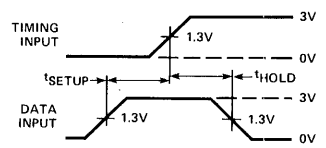
TEST LOAD CIRCUIT



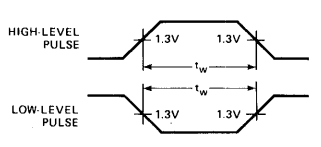
NOTES
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. R_L = 2k, C = 15pF.

VOLTAGE WAVEFORMS

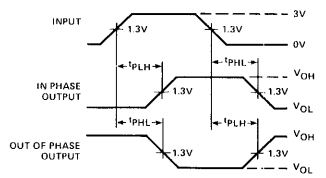
SETUP AND HOLD TIMES



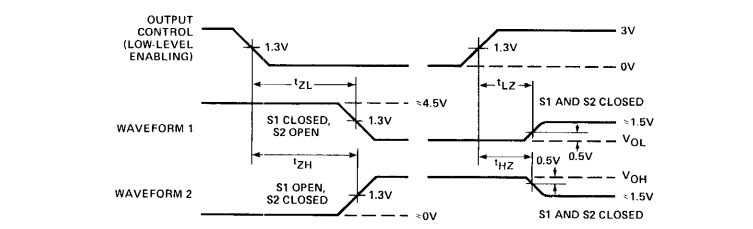
PULSE WIDTHS



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS



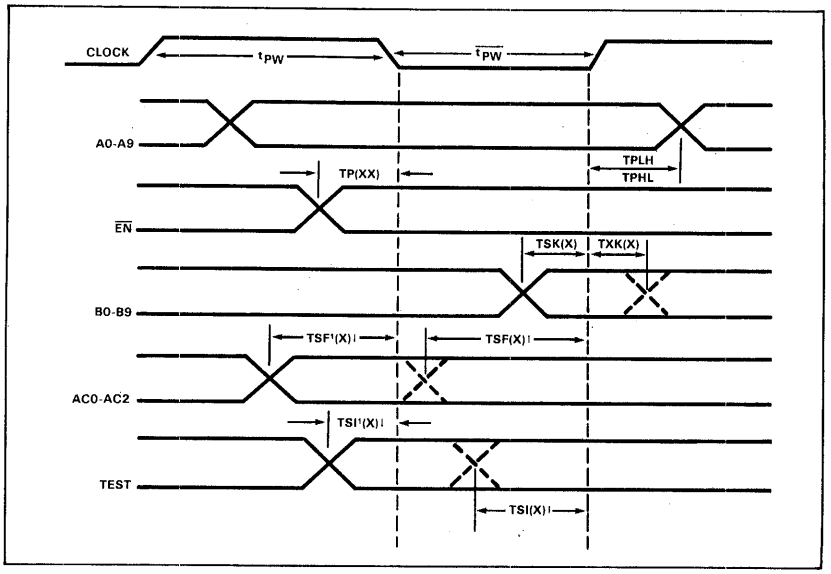
AC ELECTRICAL CHARACTERISTICS T_A = 0° -70°C, V_{CC} = 5.0V ± 5%

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
t_{HI} (1)	Test			0	-10		ns
(0)				0	-24		
	Control and data input setup times with respect to CLK (↓) for stack related functions (BLT, POP, BSR, PLP) (2)						ns
t_{SF}[1] (1)	AC_0-AC_2			35	23		
(0)				35	22		
t_{SI}[1] (1)	Test			28	23		
(0)				28	22		
	Propagation delay	A_0-A_9	EN				ns
t_{PLZ}	Low to high Z				12	35	
t_{PHZ}	High to high Z				16	35	
t_{PZL}	High to low				14	25	
t_{PZH}	High Z to high				15	35	
	Propagation delay	A_0-A_9	Clock				
t_{PHL}	High to low				33	40	
t_{PLH}	Low to high				33	40	
	Clock pulse width						ns
t_{PW}	High			50	36		
t_{PW}	Low			60	42		
	Control and data input setup times with respect to CLK (↓) for non-stack related functions (TSK, INC, BRT, RST)						ns
t_{SF} (1)	AC_0-AC_2			90	70		
(0)				90	70		
t_{SK} (1)	B_0-B_9[2]			27	22		
(0)				29	24		
t_{SI} (1)	Test			60	45		
(0)				60	45		
	Control and data input hold times with respect to CLK (↓)						ns
t_{HF} (1)	AC_0-AC_2			0	-7		
(0)				0	-12		
t_{HK} (1)	B_0-B_9[2]			0	-12		
(0)				0	-10		

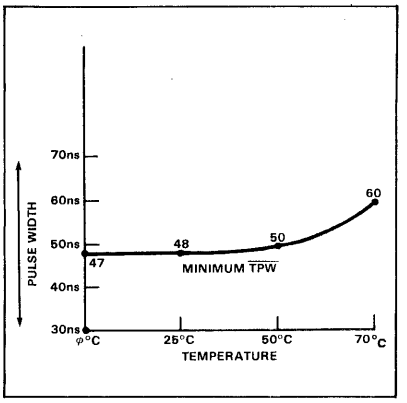
NOTES

1. Typical values are to T_A = 25°C and V_{CC} = 5.0 volts
2. B_0-B_9 inputs are required to Clock (↓) only. See TSK (1) and TSK (0).

TIMING WAVEFORM



PULSE WIDTH ($\overline{TPW}$) vs TEMPERATURE



DESCRIPTION

The 4-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPUs, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the 2901-1 will allow efficient emulation of almost any digital computing machine.

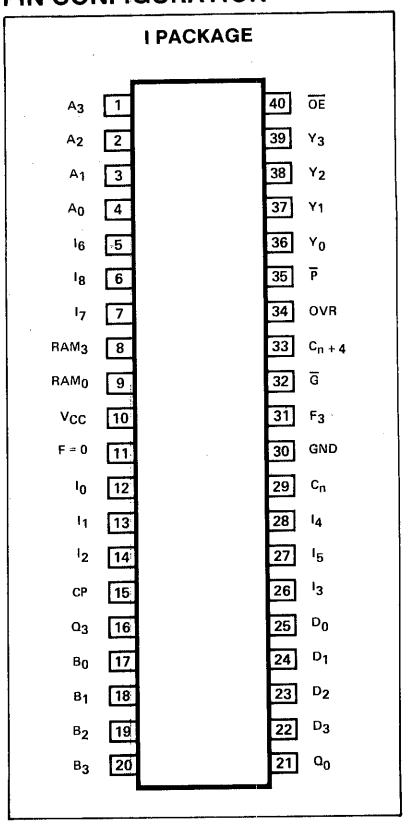
The device, as shown in the block diagram below, consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The 9-bit microinstruction word is organized into 3 groups of 3 bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

FEATURES

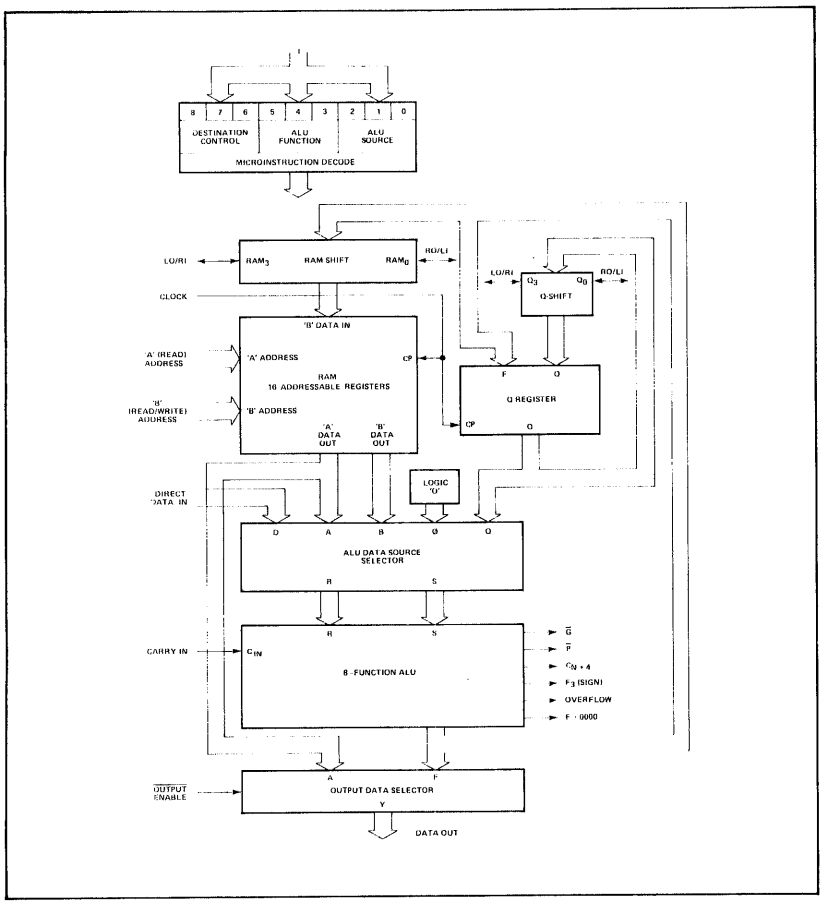
- **80ns cycle time**
- **2-address architecture**
  Independent simultaneous access to 2 working registers saves machine cycles
- **8-function ALU**
  Performs addition, 2 subtraction operations, and 5 logic functions on 2 source operands
- **Flexible data source selection**
  ALU data is selected from 5 source ports for a total of 203 source operand pairs for every ALU function
- **Left/right shift independent of ALU**
  Add and shift operations take only 1 cycle
- **4 status flags**
  Carry, overflow, zero, and negative
- **Expandable**
  Connect any number of 2901-1's together for longer word lengths
- **Microprogrammable**
  3 groups of 3 bits each for source operand, ALU function, and destination control

PIN CONFIGURATION

I PACKAGE



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-4	A_0-A_3	**A Address** The 4 address inputs to the register stack used to select 1 register whose contents are displayed through the A port. A_0 is the LSB.	Active high
17-20	B_0-B_3	**B Address** The 4 address inputs to the register stack used to select 1 register whose contents are displayed through the B port and into which new data can be written when the clock goes LOW. B_0 is the LSB.	Active high
12-14, 26-28, 5-7	I_0-I_8	**Instruction Control** The 9 instruction control lines to the 2901-1 used to determined what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q register or the register stack (I_{678}).	Active high
8 16	RAM_3 Q_3	**Shift Line** A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the 2901-1. When the destination code on I_{678} indicates a left (up) shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are off (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a right (down) shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).	Three-state Active high
9 21	RAM_0 Q_0	**Shift Line** Shift lines similar to Q_3 and RAM_3, at the LSB of the Q register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device and are used to transfer data between devices for left and right shifts of the Q register and ALU data.	Active high
22-25	D_0-D_3	**Direct Data Inputs** A 4-bit data field which may be selected as one of the ALU data sources for entering data into the 2901-1. D_0 is the LSB.	Active high
36-39	Y_0-Y_3	**Data Out** The 4 data outputs of the 2901-1. These are three-state output lines. When enabled, they display either the 4 outputs of the ALU or the data on the A port of the register stack, as determined by the destination code I_{678}. Y_0 is the LSB.	Three-state Active high
40	$\overline{OE}$	**Output Enable** When $\overline{OE}$ is High, the Y outputs are disabled; when $\overline{OE}$ is Low, the Y outputs are active (high or low).	Active low
32, 35	$\overline{G}$, $\overline{P}$	**Carry Generate, Propagate** The carry generate and propagate outputs of the 2901-1. These signals are used with the N74S182 for carry-lookahead. See Table 7 for the logic equations.	Active low
34	OVR	**Overflow** This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit. See Table 7 for logic equation.	Active high
11	F = 0	**F = 0** This is an open collector output which goes High (off) if the data on the 4 ALU outputs F_{0-3} are all low. In positive logic, it indicates the result of an ALU operation is zero.	Active high
29	C_n	**Carry In**	Active high
33	C_{n+4}	**Carry Out** (See Table 7 for logic equations.)	Active high
15	CP	**Clock** The Q register and register stack outputs change on the clock Low-to-High transition. The clock Low time is internally the write enable to the 16X4 RAM which comprises the "master" latches of the register stack. While the clock is Low, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.	Active high

SYSTEM DESCRIPTION

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a 4-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are 4 bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A port and B port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This 3-input multiplexer scheme allows the data to be shifted up (left) 1 bit position, shifted down (right) 1 bit position, or not shifted in either direction.

The RAM A port data outputs and RAM B port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is low. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform 3 binary arithmetic and 5 logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A port and the direct data inputs (D) connected as inputs. Likewise, the ALU S input multiplexer has the RAM A port, the RAM B port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These 5 inputs, when taken 2 at a time, result in 10 possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only 7 completely non-redundant source operand pairs for the ALU. The 2901-1 microprocessor implements 8 of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the 8 source operand combinations are as shown in Table 1. Also shown is the octal code for each selection.

DETAILED 2901-1 BLOCK DIAGRAM

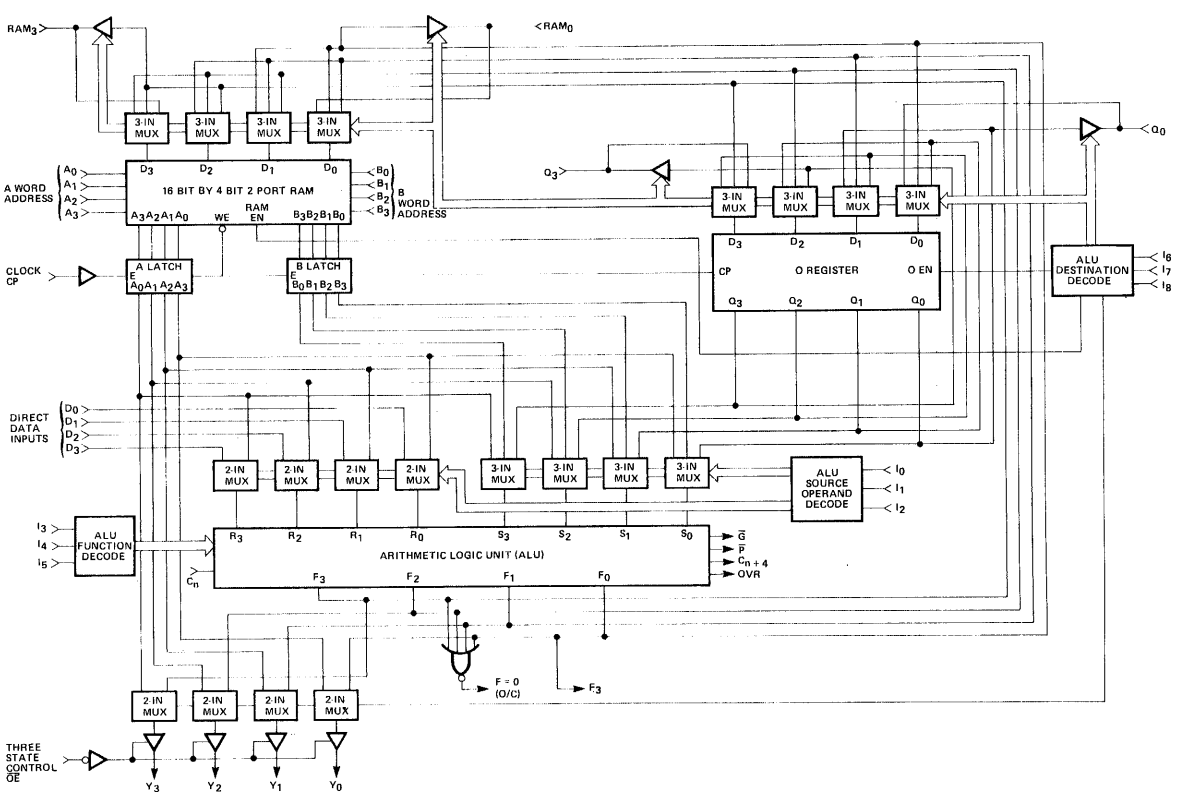


Figure 1

MICRO CODE				ALU SOURCE OPERANDS	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

Table 1 ALU SOURCE OPERAND CONTROL

The 2 source operands not fully described as yet are the D input and Q input. The D input is the 4-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing 3 binary arithmetic and 5 logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Table 2. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, G, and carry propagate, P, are outputs of the device for use with a carry-look-ahead-generator such as the N74S182. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active high.

MICRO CODE			ALU	
I_5	I_4	I_3	Octal Code	Function	Symbol
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S - R
L	H	L	2	R Minus S	R - S
L	H	H	3	R OR S	$R \vee S$
H	L	L	4	R AND S	$R \wedge S$
H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
H	H	L	6	R EX-OR S	$R \forall S$
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Table 2 ALU FUNCTION CONTROL

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is high when all F outputs are low. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is high when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstructon inputs. These combinations are shown in Table 3.

The 4-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is high, the Y outputs are in the high-impedance state.

A 2-input multiplexer is also used at the data output such that either the A port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Table 3 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a 3-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up (left) one position (X2) or shifted down (right) one position (÷2). The shifter has 2 ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7, and I_8 microinstruction inputs as defined in Table 3.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has 2 ports; one is labeled Q_0 and the other is Q_3. The operation of these 2 ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Table 3.

The clock input to the 2901-1 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the low-to-high transition of the clock. When the clock input is high, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is low, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is low.

MICRO CODE				RAM FUNCTION		Q REGISTER FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0 LO/RI	RAM_3 LI/RO	Q_0 LO/RI	Q_3 LI/RO
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Right (Down)	F/2 → B	Right (Down)	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	Right (Down)	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Left (Up)	2F → B	Left (Up)	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Left (Up)	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.

Table 3 ALU DESTINATION CONTROL

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Table 4 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Table 5 defines the various logic operations that the 2901-1 can perform and Table 6 shows the arithmetic functions of the device. Both carry-in low (C_n = 0) and carry-in high (C_n = 1) are defined in these operations.

OCTAL I_{543}, I_{210}	GROUP	FUNCTION
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \veebar Q$
6 1		$A \veebar B$
6 5		$D \veebar A$
6 6		$D \veebar Q$
7 0	EX-NOR	$\overline{A \veebar Q}$
7 1		$\overline{A \veebar B}$
7 5		$\overline{D \veebar A}$
7 6		$\overline{D \veebar Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Table 5 ALU LOGIC MODE FUNCTIONS (C_n Irrelevant)

OCTAL I_{543}	I_{210} OCTAL	0	1	2	3	4	5	6	7
	ALU Source	A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L	A + Q	A + B	Q	B	A	D + A	D + Q	D
	R Plus S								
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L	Q-A-1	B-A-1	Q-1	B-1	A-1	A-D-1	Q-D-1	-D-1
	S Minus R								
	C_n = H	Q-A	B-A	Q	B	A	A-D	Q-D	-D
2	C_n = L	A-Q-1	A-B-1	-Q-1	-B-1	-A-1	D-A-1	D-Q-1	D-1
	R Minus S								
	C_n = H	A-Q	A-B	-Q	-B	-A	D-A	D-Q	D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; - = Minus, $\vee$= OR; $\wedge$= AND, $\veebar$= EX-OR

Table 4 SOURCE OPERAND AND ALU FUNCTION MATRIX

OCTAL	C_n = 0 (LOW)		C_n = 1 (HIGH)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6 ALU ARITHMETIC MODE FUNCTIONS

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4}, AND OVR

The four signals $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the 2901-1 is in the add or subtract mode. Table 7 indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

I_{543}	FUNCTION	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S - R	← Same as R+S equations, but substitute $\overline{R}_i$ for R_i in definitions →			
2	R - S	← Same as R+S equations, but substitute $\overline{S}_i$ for S_i in definitions →			
3-7	All logic operations	High	Low	High	High

Table 7 LOGIC EQUATIONS

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

DC ELECTRICAL CHARACTERISTICS $0°C \leq +70°C$, 4.75V, $V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OH}	High level output voltage	V_{CC} = 4.75V, I_{OH} = 1.6mA	2.4			V
I_{CEX}	Output leakage current for F = 0 output	V_{CC} = 4.75V, V_{OH} = 5.25V, $V_{IN} = V_{IH}$ or V_{IL}			250	μA
V_{OL}	Low level output voltage	V_{CC} = 4.75V				
	Y	I_{OL} = 20mA			0.5	V
	$\overline{G}$	I_{OL} = 16mA			0.5	V
	C_{n+4}, F = 0, OVR, $\overline{P}$, F_3	I_{OL} = 10mA			0.5	V
	$RAM_{3,0}$, $Q_{3,0}$	I_{OL} = 6mA			0.5	V
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_I = -18mA			-1.5	V
I_I	High level input current at maximum input voltage	V_{CC} = 5.25V, V_I = 5.5V			1.0	mA
I_{IH}	High level input current	V_{CC} = 5.25V, V_I = 2.7V				
	Clock, $\overline{OE}$, A, B, D, I, C_n				20	μA
	$RAM_{3,0}$, $Q_{3,0}$ (Note 1)				20	μA
I_{IL}	Low level input current	V_{CC} = 5.25V, V_I = 0.5V				
	Clock, DE, A, B, D, I, C_n				50	μA
	$RAM_{3,0}$, $Q_{3,0}$ (Note 1)				-100	μA
I_{OS}	Short circuit output current (Note 2)	V_{CC} = 5.25V	-10		-40	mA
I_{OZ}	High-Z state output current $Y_0 - Y_3$	V_0 = 2.4V			50	μA
		V_0 = 0.5V			-50	μA
	$RAM_{3,0}$, $Q_{3,0}$	V_0 = 2.4V			100	μA
		V_0 = 0.5V			-100	μA
I_{CC}	Supply current	V_{CC} = 5.25V		165	265	mA

NOTES

1. LO/RI and RO/LI are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
2. Not more than 1 output should be shorted at a time. Duration of the short-circuit test should not exceed 1 second.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_A	Operating temperature range	0° to +70°	°C
T_{STG}	Storage temperature range	-65° to +150°C	°C

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
	Clock Times[1]				
t_{CY}	Clock cycle time	80	65		ns
t_{RMW}	Ready-modify-write cycle	70	55		ns
f_Q	Clock frequency to shift Q register	25	30		MHz
t_{CL}	Clock low period	30	22		ns
t_{CH}	Clock high period	30	13		ns
	Hold Times[1]				
t_H	Any input	0	-3		ns
	Setup Times[1]				
t_{SAB}	A, B, setup time[2, 3, 4]	90	65		ns
		t_{CL} + 30	t_{CL} + 15		ns
t_{SBD}	B destination setup time[2, 3, 4]	t_{CL} + 15	t_{CL} + 5		ns
t_{SD}	D input setup time	60	45		ns
t_{SCn}	Cn input setup time	50	35		ns
t_{SI012}	ALU source control setup time	80	60		ns
t_{SI345}	ALU function setup time	75	58		ns
t_{SI678}	ALU destination control setup time[5]	t_{CL} + 25	t_{CL} + 15		ns
t_{SS}	$RAM_{3,0}$, input setup time	30	20		ns
	$Q_{3,0}$	15	10		

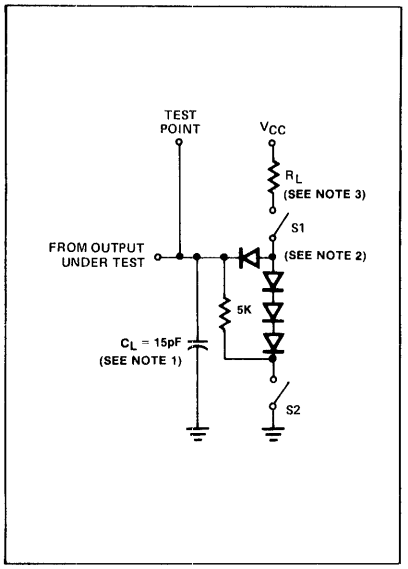
NOTES

1. Setup and hold times are defined relative to the clock low-to-high edge. Inputs must be steady at all times from the setup time prior to the clock until the hold after the clock. The setup times allow sufficient time to perform the correct operation on the correct operation on the correct data so that the correct ALU data can be written into one of the registers.
2. If the B address is used as a source operand, allow for the A, B source setup time; if it is used only for the destination address, use the B dest. setup time.
3. Where 2 numbers are shown, both must be met.
4. t_{CL} is the clock low time.

PROPAGATION DELAYS (ns) C_L = 15pF T_A = 0° to +70°C, V_{CC} = 5.0V ± 5%

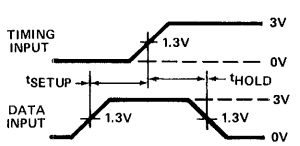
From Input \ To Output	Y	F_3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0 RL = 470	OVR	SHIFT OUTPUTS	
							RAM	Q
Clock	60	55	45	50	65	50	65	45
A, B	75	65	60	70	80	60	80	—
D (arithmetic mode)	40	30	30	40	55	40	55	—
D(I = X37, logic mode)	40	30	—	—	55	—	55	—
C_n	40	25	25	—	45	30	50	—
I_{012}	60	50	45	50	60	45	65	—
I_{345}	55	40	40	50	50	45	60	—
I_{678}	30	—	—	—	—	—	45	45
$\overline{OE}$ Enable/Disable	25/30	—	—	—	—	—	—	—
A bypassing ALU (I = 2xx)	45	—	—	—	—	—	—	—

TEST LOAD CIRCUIT

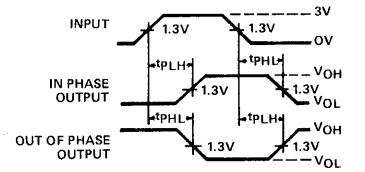


VOLTAGE WAVEFORMS

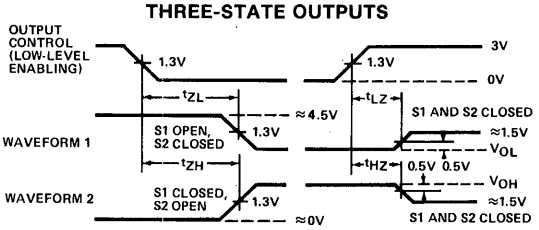
SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS

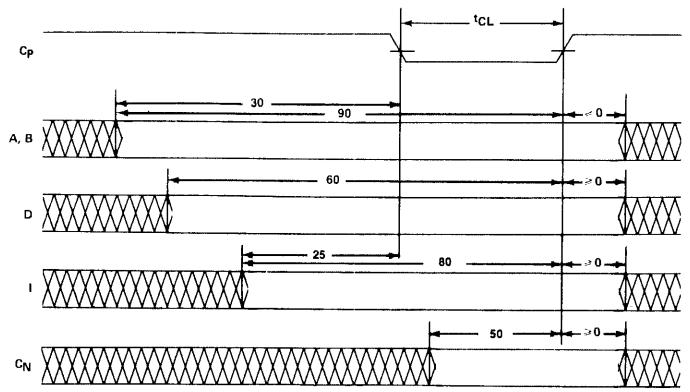


NOTES

1. C_L includes probe and jig capacitance.
2. All diodes 1N916 or 1N3064.
3. R_L = 2K

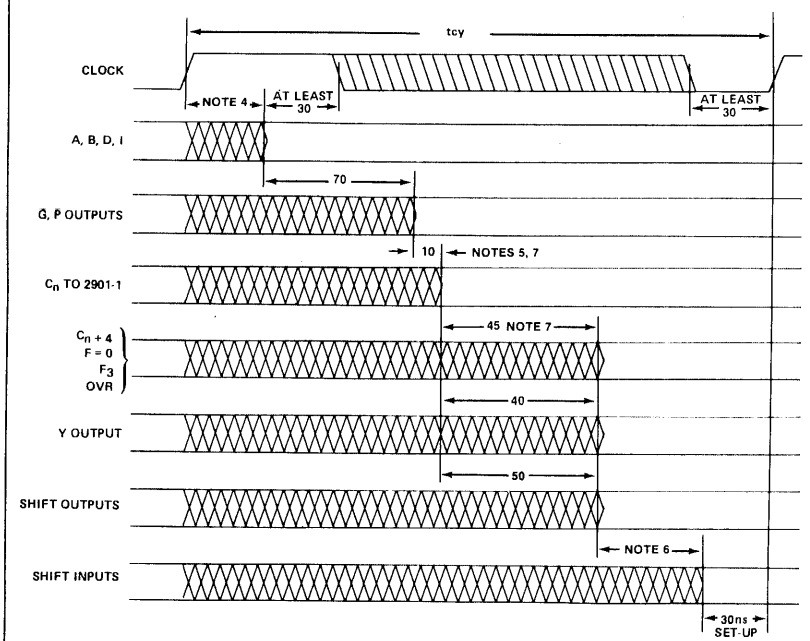
VOLTAGE WAVEFORMS (Cont'd) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

MINIMUM CYCLE TIMES FROM INPUTS



Numbers Shown Are Minimum Data Stable Times for 2901-1, DC, in ns.

SWITCHING WAVEFORMS FOR 16-BIT SYSTEM



Assuming A, B, D, and I are all Driven from Registers with the same Propagation Delay, Clocked by the 2901-1 Clock.

NOTES

4. This delay is the max. tpd of the register containing A, B, D, and I.
5. 10ns for lookahead carry. For ripple carry over 16 bits use 2 x (Cn → Cn + 4).
6. This is the delay associated with the multiplexer between the shift outputs and shift inputs on the 2901-1s. Normally applicable only for double length or circular shifts.
7. Not applicable for logic operations.

INTRODUCTION

The 2 components of the Series 3000 chip set, when combined with industry standard memory and peripheral circuits, allows the design engineer to construct high-performance processors and/or controllers with a minimum amount of auxillary logic. Features such as the multiple independent address and data buses, tri-state logic, and separate output enable lines eliminate the need for time-multiplexing of buses and associated hardware.

Each Central Processing Element represents a complete 2-bit slice through the data processing section of a computer. Several CPEs may be connected in parallel to form a processor of any desired word length. The Microprogram Control Unit controls the sequence in which microinstructions are fetched from the microprogram memory (ROM/PROM), with these microinstructions controlling the step-by-step operation of the processor.

Each CPE contains a 2-bit slice of 5 independent buses. Although they can be used in a variety of ways, typical connections are:

Input M-bus:	Carries data from external memory
Input I-bus:	Carries data from input/output device
Input K-bus:	Used for microprogram mask or literal (constant) value input
Output A-bus:	Connected to CPE Memory Address Register
Output D-bus:	Connected to CPE accumulator.

As the CPEs are paralleled together, all buses, data paths, and registers are correspondingly expanded.

The microfunction input bus (F-bus) controls the internal operation of the CPE, selecting both the operands and the operation to be executed upon them. The arithmetic logic unit (ALU), controlled by the microfunction decoder, is capable of over 40 Boolean and binary operations as outlined in the Function Description section of the N3002 data sheet. Standard carry look-ahead outputs (X and Y) are generated by the CPE for use with industry standard devices such as the 74S182.

A typical processor configuration is shown in Figure 1. It should be remembered that in working with slice-oriented microprocessors, the final configuration may be varied to enhance speed, reduce component count, or increase data-processing capability. One method of maximizing a processor's performance is called pipelining. To accomplish this, a group of D-type flip-flops or latches (such as the 74174 Hex D-type Flip-Flop) are connected to the microprogram memory outputs (excluding the address control field AC_0-AC_8) to buffer the current microinstruction and allow the MCU to overlap the fetch of the next instruction with the execution of the current one. The time saved in pipelining operations is the shorter of either the address set-up time to the microprogram memory (ROM/PROM) or the access time of the ROM/PROM. A convenient way of implementing pipelining is to use ROMs with on-board latches, such as the Signetics 82S115.

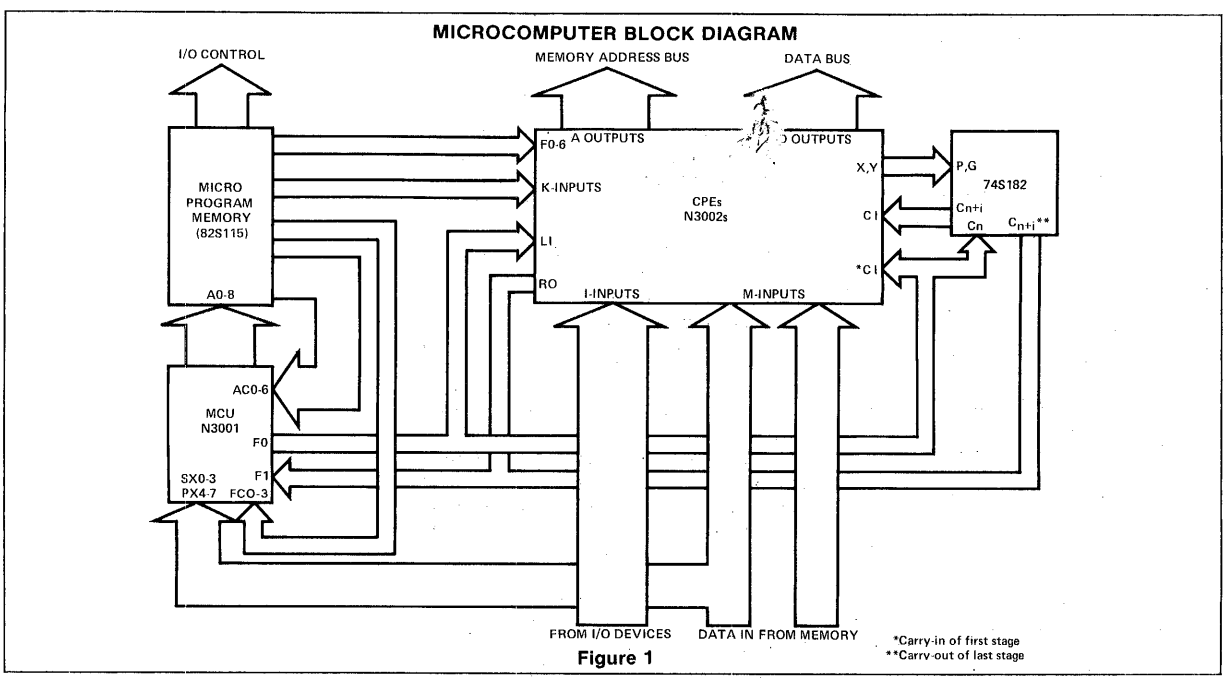


Figure 1

Figure 2 shows a typical microinstruction format using the 82S114 PROMs contained in the Signetics 3000 Microprocessor Designer's Evaluation Kit. Although this particular example is for a 48-bit word (6 PROMs), the allocation of bits for the mask (K-bus) and optional processor functions depends on the specific application of the system and the trade offs which the designer wishes to make.

In using the K-bus, it should be kept in mind that the K inputs are always ANDed with the B-multiplexer outputs into the ALU. Bit masking, frequently done in computer control systems, can be performed with the mask supplied to the K-bus directly from the microinstruction.

By placing the K-bus in either the all-one or all-zero condition (done with a single control bit in the microinstruction), the accumulator will either be selected or deselected, respectively, in a given operation. This feature nearly doubles the amount of microfunctions in the CPE. A description of these various microfunctions can be found in the N3002 data sheet under the heading Function Description by referring to the K-bus conditions of all-ones (11) and all-zeros (00).

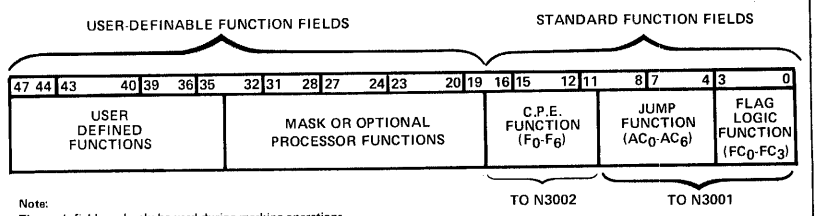
The MCU controls the sequence in which microinstructions are fetched from the microprogram memory (ROM/PROM). In its classical form, the MCU would use a next-address field in each microinstruction. However, the N3001 uses a modified classical approach in which the microinstruction field specifies conditional tests on the MCU bus inputs and registers. The next-address logic of the MCU also makes extensive use of a row/column addressing scheme, whereby the next address is defined by a 5-bit row address and 4-bit column address. Thus, from a particular address location, it is possible to jump unconditionally to any location within that row or column, or conditionally to other specified locations in one operation. Using this method, the processor functions can be executed in parallel with program branches.

As an example of this flexibility, let us assume a disk controller is being designed. As part of the sequence logic, 3 bits of the disk drive status word must be tested and all 3 must be true in order to proceed with the particular sequencing operation. In any sequencing operation using a status word for conditional branch information, there are innumerable combinations of bits which must be tested throughout the sequencing operation. Using discrete logic techniques, this would involve several levels of gating.

However, the entire operation can be done in two microinstructions. First, the mask (K-bus) field in the microinstruction format is encoded with a one for each corresponding status bit to be tested and a zero for each bit to be discarded. The status word is input via the I-bus and ANDed with the K-bus mask using the CPE microfunction operation from F-Group 2, R-Group III. Assuming we are using low-true logic (true = 0 volts), we now test the result, which is located in the accumulator AC, for all zeros using the CPE microfunction operation from F-Group 5, R-Group III. Depending on the zero/non-zero status of AC, a one or zero will be loaded into the carryout CO bit. This bit can now be used as a condition for the next address jump calculation within the N3001 MCU. If the AC was zero (status word was true), we will jump to the next address within our controller sequence. If the AC was non-zero (status word not true), then a jump would be made back to the beginning of this 2-microinstruction loop and the test sequence repeated until the status word (all 3 bits) is true.

Figure 3 shows a typical timing diagram for a system operating in the non-pipelined mode. Keep in mind that the maximum clock rate is dependent upon the total of propagation delay times plus required set-up times. It is at the designer's discretion to resolve the speed versus complexity trade-offs.

TYPICAL MICROINSTRUCTION FORMAT



Note:
The mask field need only be used during masking operations.
At other times, it is entirely user definable.

Figure 2

SYSTEM TIMING—NON-PIPELINED CONFIGURATION

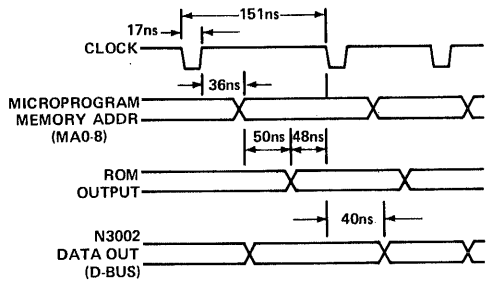


Figure 3

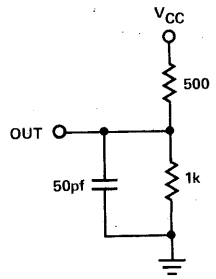
ABSOLUTE MAXIMUM RATINGS

PARAMETER	N3001/N3002	S3001/S3002	UNIT
Temperature under bias	0 to +70	-55 to +125	°C
Storage temperature	-60 to +160	-65 to +150	°C
All output and supply voltages	-0.5 to +7	-0.5 to +7	V
All input voltages	-1.0 to +5.5	-1.0 to +5.5	V
Output currents	100	100	mA

*NOTE

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

TEST LOAD CIRCUIT



NOTE: All resistor values are typical and in ohms.
TEST CONDITIONS:
Input pulse amplitude of 2.5 volts
Input rise and fall times of 5ns between 1 volt and 2 volts
Output load of 10mA and 50pF
Speed measurements are taken at the 1.5 volt level

DC ELECTRICAL CHARACTERISTICS

N3001/N3002 T_A = 0°C to +70°C
S3001/S3002 T_A = -55°C to +125°C

PARAMETER		TEST CONDITIONS	N3001/N3002			S3001/S3002			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								
V_{IL}	Low level	V_{CC} = 5.0V			0.8			0.8	V
V_{IH}	High level	V_{CC} = 5.0V	2.0			2.0			V
V_{IC}	Clamp	V_{CC} = 4.75V, I_C = -5mA		-0.55	-1.0		-0.8	-1.2	V
	Output voltage								
V_{OL}	Low level	V_{CC} = 4.75V, I_{OL} = 10mA		0.35	0.45		0.35	0.45	V
V_{OH}	High level	V_{CC} = 4.75V, I_{OH} = -1mA		2.4	3.0		2.4	3.0	V
		mA_0 - mA_8, ISE, FO							
	Input current								
I_F	Load N3001	V_{CC} = 5.25V, V_F = 0.45V							
		CLK input		-0.21	-0.75		-0.21	-0.75	mA
		EN input		-0.12	-0.50		-0.12	-0.50	mA
		All other inputs		-0.05	-0.25		-0.05	-0.25	mA
I_F	Load N3002	V_{CC} = 5.25V, V_F = 0.45V							
		F_0-F_6, CLK, K_0, K_1, EA, ED		-0.05	-0.25		-0.05	-0.25	mA
		I_0, I_1, M_0, M_1, LI		-0.85	-1.5		-0.85	-1.5	mA
		CI		-2.3	-4.0		-2.3	-4.0	mA
I_R	Input leakage N3001	V_{CC} = 5.25, V_R = 5.25V					V_R = 5.5V		
		CLK input			120			120	μA
		EN input			80			80	μA
		All other inputs			40			40	μA
I_R	Input leakage N3002	V_{CC} = 5.25V, V_R = 5.25V							
		F_0-F_6, CLK, K_0, K_1, EA, ED			40			40	μA
		I_0, I_1, M_0, M_1, LI			60			60	μA
	Output current	CI			180			180	μA
I_{OS}	Short circuit	V_{CC} = 5.0V							
		mA_0 - mA_8, ISE, FO	-15	-28	-60	-15	-28	-60	mA
I_O (off)	Off-state	V_{CC} = 5.25V							
		PR_0 - PR_2, mA_0 - mA_2, FO							
		V_{OUT} = 0.45V			-100			-100	μA
		mA_0 - mA_8, FO					V_{OUT} = 5.5V		
		V_{OUT} = 5.25V			+100			+100	μA
I_{CC}	Power supply current N3001	V_{CC} = 5.25V[2]		170	240		170	250	mA
	Power supply current N3002			145	190		145	210	mA

NOTES

1. SN3001 typical values are for T_A = 25°C, V_{CC} = 5.0V
2. SN3002 EN input grounded, all other inputs and outputs open.
   SN3002 CLK input grounded, other inputs open.

INTRODUCTION

Signetics family of Bipolar Bit Slice Microprocessor products consists of the 8X02 Control Store Sequencer, the 3001 microprogram control unit (MCU), the 2901-1 four bit central processing element and the 3002 two bit central processing element. These devices, all manufactured with low power Schottky technology, can be readily and efficiently interfaced with all other industry standard components, including the 7400, 74LS, 74S and Signetics' 82S and 8T families.

Figure 1 is a generalized functional block diagram of a typical Bipolar Microprocessor based system. This applications memo categorizes various components that can be used to implement each of the major functional blocks shown in Figure 1.

THE PROCESSING SECTION

The Processing Section of a computer, or "smart" controller, as shown in Figure 2, provides facilities for the transfer of data, logical and arithmetic manipulation of data, and temporary storage of data, address and status information. Cache memories are frequently used to enhance system performance by providing immediately available information and data to the CPU at high speed.

Signetics devices that can be used to implement the Processing Section of the CPU or controller are listed below in Tables 1 and 2.

DEVICE	DESCRIPTION
2901-1	4-Bit Register and ALU Central Processing Element
N3002	Central Processing Element
74S182	Carry-Look-Ahead Generator

Table 1 ALU, GENERAL PURPOSE REGISTERS, AND CARRY-LOOK-AHEAD CIRCUITS

DEVICE	DESCRIPTION
3101A	RAM (16 words by 4 bits)
82S25	Write-While-Read RAM (32 words by 2 bits)
82S25	RAM (16 words by 4 bits)
82S09	RAM (64 words by 9 bits)
82S116/117	RAM (256 words by 1 bit)
74S200/201	RAM (256 words by 1 bit)
74S301	RAM (256 words by 1 bit)
93415A	RAM (1024 words by 1 bit)
93425A	RAM (1024 words by 1 bit)
82S10/11	RAM (1024 words by 1 bit)

Table 2 HIGH SPEED BIPOLAR CACHE MEMORIES

BLOCK DIAGRAM OF TYPICAL BIPOLAR MICROPROCESSOR SYSTEM

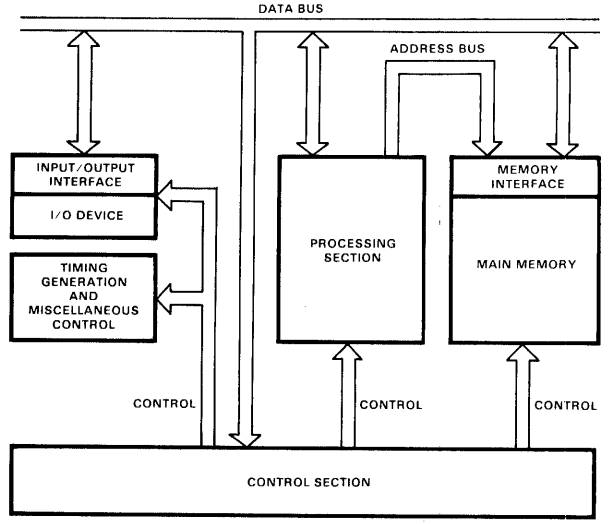


Figure 1

THE PROCESSING SECTION

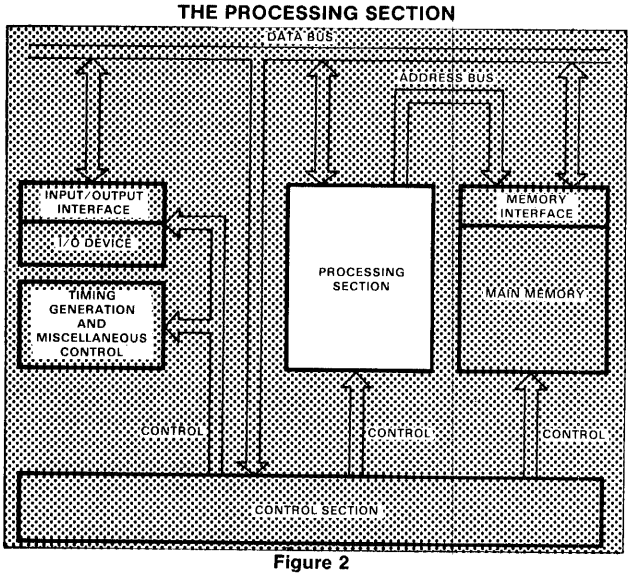


Figure 2

THE CONTROL SECTION

The Control Section logic as shown in Figure 3, handles most, if not all, of the control functions. These functions are typified by operations such as decoding macro-instructions, testing of hardware or program status, initializing memory and I/O operations, manipulating data, and sampling and responding to external and internal interrupts. These control functions are implemented by executing a single microinstruction or a series of microinstructions. Through microprogramming, a structured form of control can be realized.

Reference Tables 3 through 6 for hardware selection.

DEVICE	DESCRIPTION
82S100/101	Field Programmable Logic Array (FPLA)
82S102/103	Field Programmable Gate Array

NOTE

In addition to the FPLA, all ROMs and PROMs listed below under Conditional Test and Branch Decoding and Microprogram Memory can also be used.

Table 3 MACRO INSTRUCTION DECODING

DEVICE	DESCRIPTION
82S123	PROM (32 words by 8 bits)
82S23	PROM (32 words by 8 bits)
82S229	PROM (256 words by 4 bits)
82S226	ROM (256 words by 4 bits)
82S129	PROM (256 words by 4 bits)
82S126	PROM (256 words by 4 bits)
82S27	PROM (256 words by 4 bits)

Table 4 CONDITIONAL TEST AND BRAND DECODING

DEVICE	DESCRIPTION
N3001	Microprogram Control Unit (512-word addressability)
8X02	Control Store Sequencer (1024-word addressability)

NOTE

In addition, all ROMs and PROMs listed in Conditional Test and Branch Decoding can also be used.

Table 5 MICROPROGRAM SEQUENCING

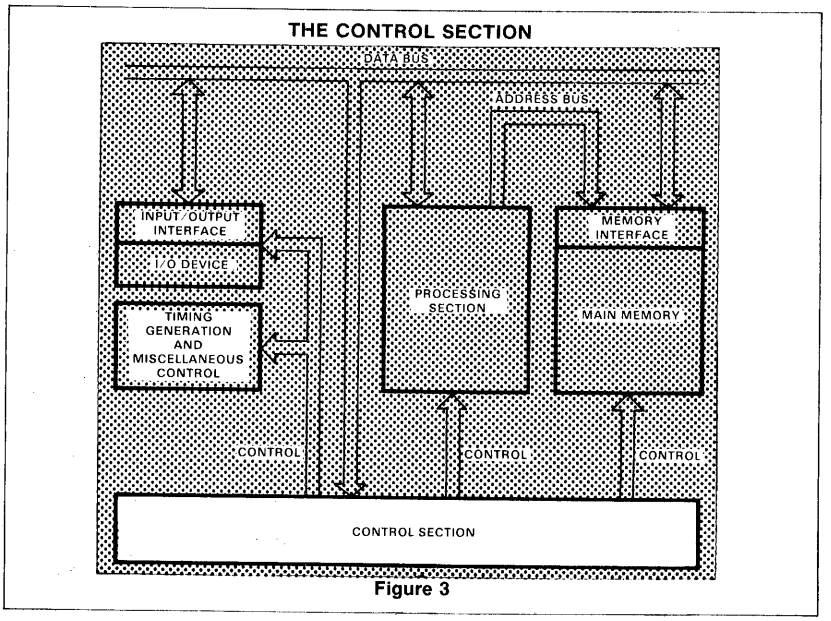


Figure 3

DEVICE	DESCRIPTION
82S130	PROM (512 words by 4 bits)
82S131	PROM (512 words by 4 bits)
82S114	PROM with output latches (256 words by 8 bits)
82S214	ROM with output latches (256 words by 8 bits)
82S215	ROM with output latches (512 words by 8 bits)
82S230/231	ROM (512 words by 4 bits)
8228	ROM (1024 words by 4 bits)
82S115	PROM with output latches (512 words by 8 bits)
82S136/137	PROM (1024 words by 4 bits)
82S236/237	ROM (1024 words by 4 bits)
82S280/281	ROM (1024 words by 8 bits)
82S184/185	PROM (2048 words by 4 bits)
82S284/285	ROM (2048 words by 4 bits)

Table 6 MICROPROGRAM MEMORY

I/O INTERFACE LOGIC

There are many different types of bus structures (see Figure 4). To save hardware and the number of signal lines, the use of a bidirectional bus is an excellent solution for handling the data bus problem, while a tri-state bus structure is ideal for the address bus, (see Table 7). In many instances, when systems of different logic families need to be interfaced with each other, logic level translators are required, (see Table 8).

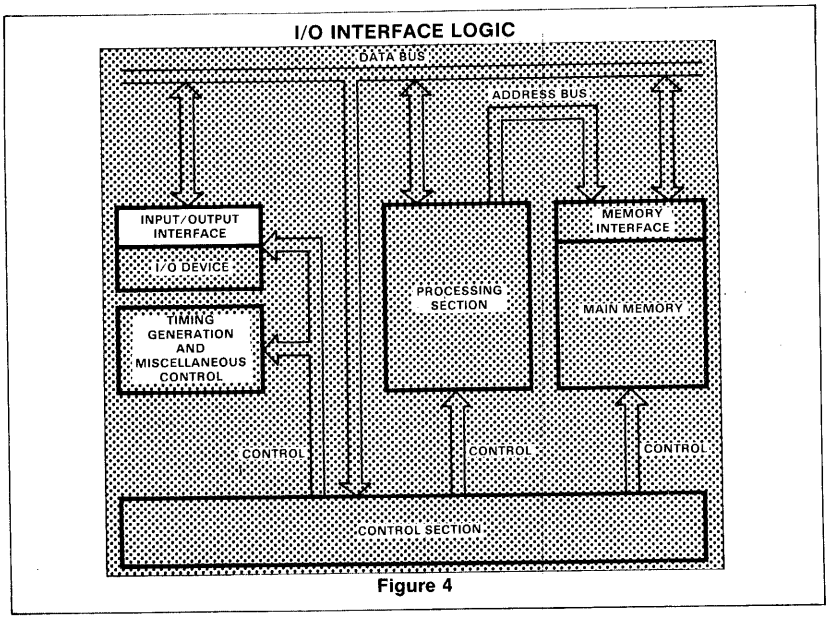


Figure 4

DEVICE	DESCRIPTION
8T26A	Tri-state, inverting quad bus transceiver.
8T28	Tri-state, non-inverting quad bus transceiver.
8T31	Tri-state 8-bit bidirectional I/O port.
8T09	Tri-state quad bus driver (40mA), with individual enable/disable
8T10	Tri-state quad D-type bus (FF) with high drive capability
8T13	Dual-line driver
8T14	Triple line receiver with hysteresis
8T15	Dual Communications EIA/MIL line driver
8T16	Dual Communication EIA/MIL line receiver with hysteresis.
8T23	Dual-line driver
8T24	Triple-line receiver with hysteresis
8T38	Quad bus transceiver
8T95	Tri-state, non-inverting hex buffer
8T96	Tri-state, non-inverting hex buffer
8T97	Tri-state, inverting hex buffer
8T98	Tri-state, inverting hex buffer
8T100	Quad differential line drivers
8T110	Quad differential line receivers

Table 7 BUS BUFFERS AND DRIVERS

DEVICE	DESCRIPTION
10124	Quad TTL-to-ECL driver
10125	Quad ECL-to-TTL receiver
8T80	Quad gate TTL to High-voltage
8T90	Hex buffer TTL to High-voltage
8T25	MOS-to-TTL translator
8T18	High-voltage to TTL

Table 8 LOGIC LEVEL TRANSLATORS

MEMORY INTERFACE AND MAIN MEMORY

When dynamic MOS memory devices are used as main memory, see Figure 5, a memory refresh scheme will be needed. Usually sense amplifiers, address and data buffers, and parity generators and checkers are considered as part of the memory interface logic, (see Table 9-12).

DEVICE	DESCRIPTION
7520	Dual core-memory sense amplifiers
7521	Dual core-memory sense amplifiers
7522	Dual core-memory sense amplifiers
7523	Dual core-memory sense amplifiers
7524	Dual core-memory sense amplifiers
7525	Dual core-memory sense amplifiers
3207A-1	Quad TTL-MOS clock drivers
3207A	Quad TTL-MOS clock drivers
8T09	Tri-state quad bus driver
8T380	Tri-state bus receiver, with:
8T25	Tri-state dual sense amplifier/latch

Table 9 SENSE AMPLIFIERS AND DRIVERS

DEVICE	DESCRIPTION
8262	9-bit parity
74180	8-bit parity

Table 10 PARITY GENERATOR AND CHECKER

DEVICE	DESCRIPTION
8281	Binary counter
8291	Binary counter
74123	Dual one-shot
82S33	Quad 2-to-1 multiplexer
82S34	Quad 2-to-1 multiplexer

Table 11 MEMORY REFRESH LOGIC

DEVICE	DESCRIPTION
1103	1K (1024X1) RAM
1103-1	1K (1024X1) RAM
2602-1	1K (256X4) RAM, static
2606	1K (256X4) RAM, static
2102	1K (1024X1) RAM
2680	4K (4096X1) RAM
2660	4K (4096X1) RAM

Table 12 MOS MEMORY

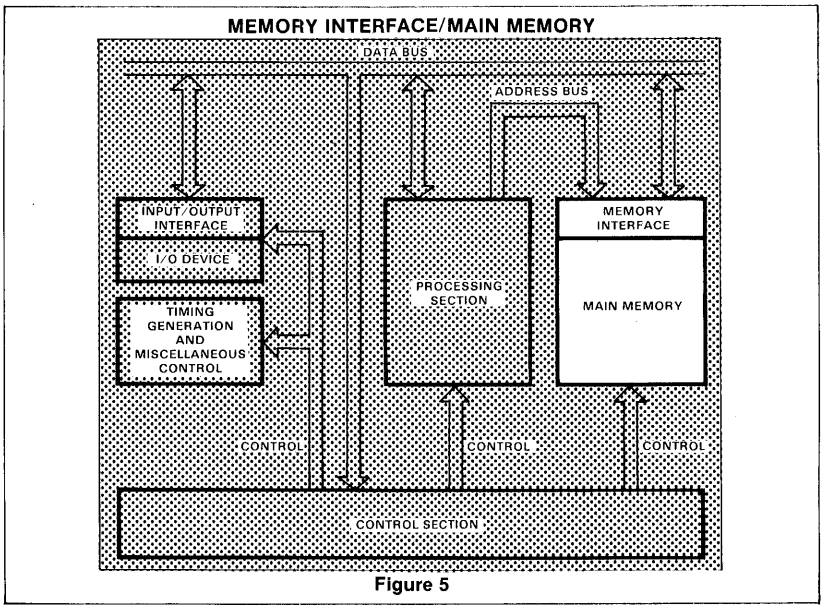


Figure 5

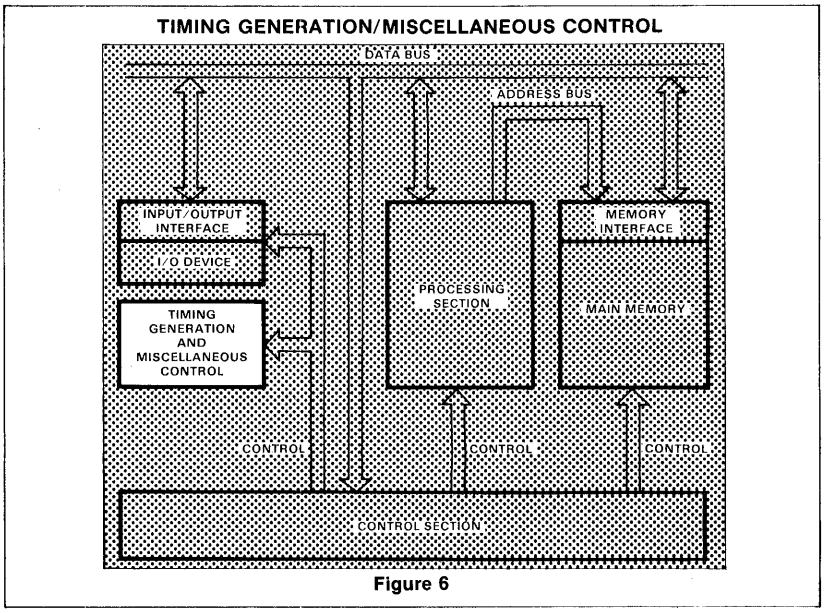


Figure 6

TIMING GENERATION AND MISCELLANEOUS CONTROL

Most timing generation requirements as shown in Figure 6 can be met by using a one-shot (retriggerable monostable multivibrator). If a multiple-phase clocking system is required, additional shift registers may be used.

DEVICE	DESCRIPTION
74123	Dual-monostable multivibrator
9602	Dual-monostable multivibrator
74S194	4-bit bidirectional universal shift register
74S195	4-bit parallel-access shift registers
74S178	4-bit shift register
74S179	4-bit shift register

S/N3001-I

DESCRIPTION

The S/N3001 MCU is 1 element of a bipolar microcomputer set. When used with the S/N3002, 54/74S182, ROM or PROM memory, a powerful microprogrammed computer can be implemented.

The 3001 MCU controls the fetch sequence of microinstructions from the microprogram memory. Functions performed by the 3001 include:

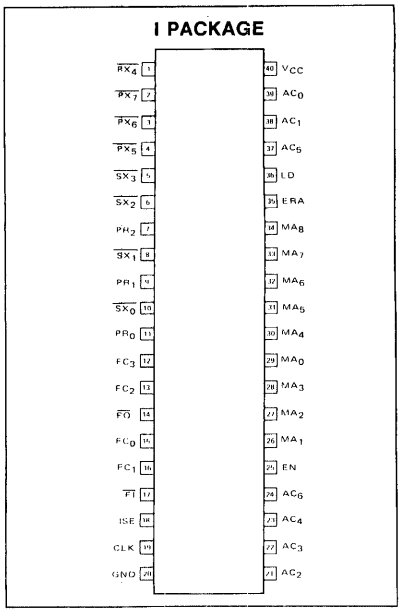
- Maintenance of microprogram address register
- Selection of next microinstruction address
- Decoding and testing of data supplied via several input buses
- Saving and testing of carry output data from the central processing (CP) array
- Control of carry/shift input data to the CP array
- Control of microprogram interrupts

FEATURES

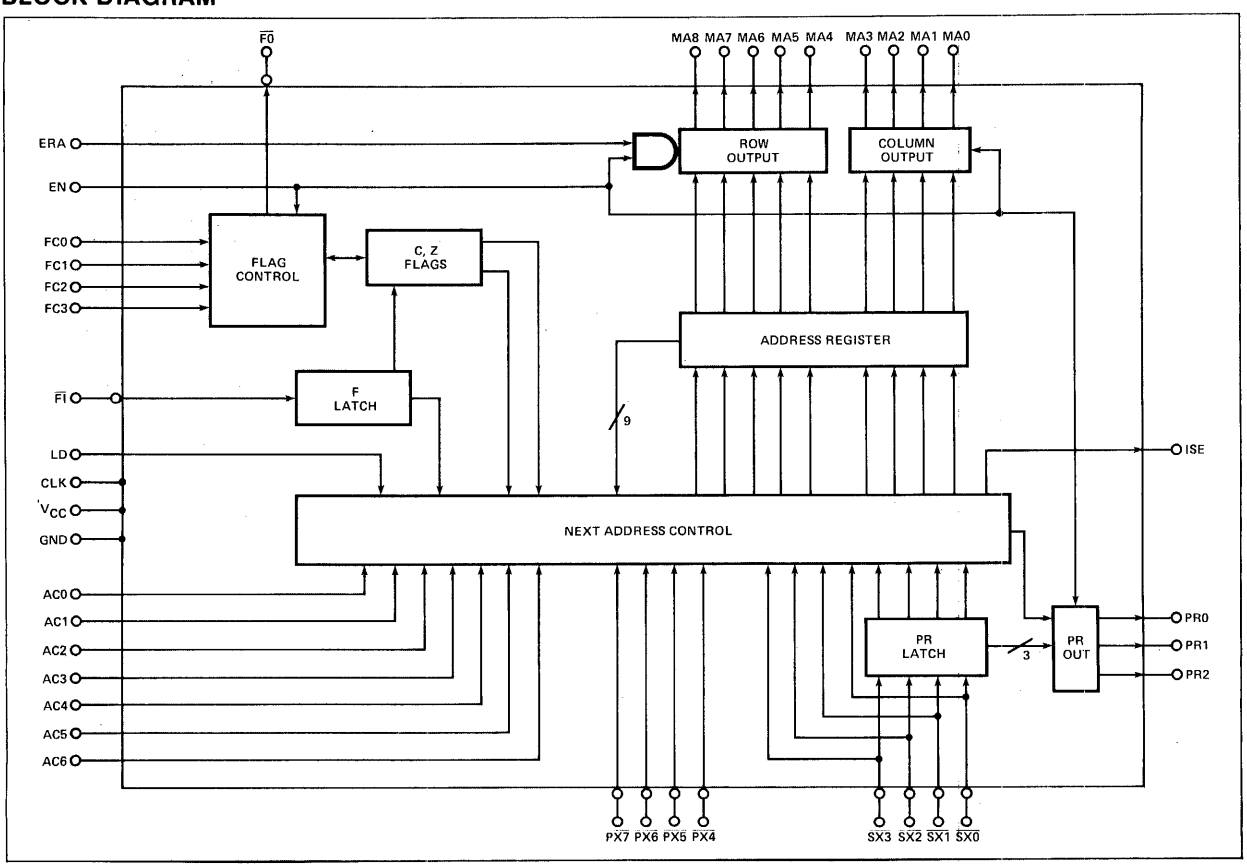
- **Schottky TTL process**
- **45ns cycle time (typ.)**
- **Direct addressing of standard bipolar PROM or ROM**
- **512 microinstruction addressability**
- **Advanced organization:**
  - **9-bit microprogram address register and bus organized to address memory by row and column**
  - **4-bit program latch**
  - **2-flag registers**
- **11 address control functions:**
  - **3 jump and test latch function**
  - **16 way jump and test instruction**
- **8 flag control functions:**
  - **4 flag input functions**
  - **4 flag output functions**

PIN CONFIGURATION

I PACKAGE



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-4	$\overline{PX_4}$-$\overline{PX_7}$	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	Active low
5,6,8,10	$\overline{SX_0}$-$\overline{SX_3}$	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	Active low
7,9,11	PR_0-PR_2	PR-Latch Outputs The PR-latch outputs (SX_0-SX_2) are synchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	Open Collector
12,13 15,16	FC_0-FC_3	Flag Logic Control Inputs The flat logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	Active high
14	$\overline{FO}$	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	Active low Three-state
17	$\overline{FI}$	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: The flag input data is saved in the F-latch when the clock input (CLK) is low.	Active low
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description). It can be used to provide the strobe signal required by interrupt circuits.	Active high
19	CLK	Clock Input	
20	GND	Ground	
21-24 37-39	AC_0-AC_6	Next Address Control Function Inputs All jump functions are selected by these control lines.	Active high
25	EN	Enable Input When in the high state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26-29	MA_0-MA_3	Microprogram Column Address Outputs	Three-state
30-34	MA_4-MA_8	Microprogram Row Address Outputs	Three-state
35	ERA	Enable Row Address Input When in the low state, the enable row address input independently disables the microprogram row address outputs. It can be used to facilitate the implementation of priority interrupt systems.	Active high
36	LD	Microprogram Address Load Input When the active high state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction buses into the microprogram address register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	Active high
40	V_{CC}	+5 Volt supply	

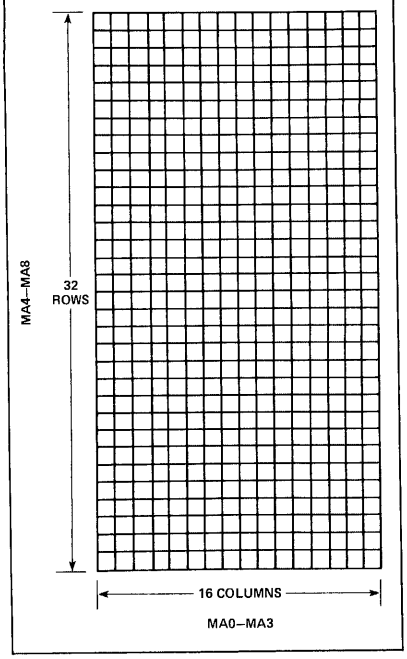
THEORY OF OPERATION

The MCU controls the sequence of microinstructions in the microprogram memory. The MCU simultaneously controls 2 flip-flops (C, Z) which are interactive with the carry-in and carry-out logic of an array of CPEs.

The functional control of the MCU provides both unconditional jumps to new memory locations and jumps which are dependent on the state of MCU flags or the state of the "PR" latch. Each instruction has a "jump set" associated with it. This "jump set" is the total group of memory locations which can be addressed by that instruction.

The MCU utilizes a two-dimensional addressing scheme in the microprogram memory. Microprogram memory is organized as 32 rows and 16 columns for a total of 512 words. Word length is variable according to application. Address is accomplished by a 9-bit address organized as a 5-bit row and 4-bit column address.

ADDRESSING ORGANIZATION



FUNCTIONAL DESCRIPTION

The following is a description of each of the eleven address control functions. The symbols shown below are used to specify row and column addresses.

MNEMONIC	FUNCTION
row_n	5-bit next row address where n is the decimal row address.
col_n	4-bit next column address where n is the decimal column address.

Unconditional Address Control (Jump) Functions

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs (AC0-AC6) to generate the next microprogram address.

Flag Conditional Address Control (Jump Test) Functions

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

JUMP FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JCC	Jump in current column. AC_0-AC_4 are used to select 1 of 32 row addresses in the current column, specified by MA_0-MA_3, as the next address.
JZR	Jump to zero row. AC_0-AC_3 are used to select 1 of 16 column addresses in row_0, as the next address.
JCR	Jump in current row. AC_0-AC_3 are used to select 1 of 16 addresses in the current row, specified by MA_4-MA_8, as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7-MA_8, as the next row address. The current column is specified by MA_0-MA_3. The PR-latch outputs are asynchronously enabled.

JUMP/TEST FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JFL	Jump/test F-latch. AC_0-AC_3 are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is col_0-col_7, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the F-latch is used to select col_{10} or col_{11} as the next column address.
JCF	Jump/test C-flag. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_3 is col_0-col_7, the C-flag is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the C-flag is used to select col_{10} or col_{11} as the next column address.
JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.
JPR	Jump/test PR-latch. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The 4 PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test leftmost PR-latch bits. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to select 1 of 4 column addresses in col_4 through col_7 as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC_0 and AC_1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} through col_{16} as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by MA_6-MA_8, as the next row address. PX_4-PX_7 are used to select 1 of 16 possible column addresses as the next column address. SX_0-SX_3 data is locked in the PR-latch at the rising edge of the clock.

PX-Bus and PR-Latch Conditional Address Control (Jump/Test) Functions

The PX-bus jump/test function uses the data on the primary instruction bus (PX_4-PX_7), the current microprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Flag Control Functions

The flag control functions of the MCU are selected by the 4 input lines designated FC_0-FC_3. Function code formats are given in "Flag Control Function summary."

The following is a detailed description of each of the 8 flag control functions.

Flag Input Control Functions

The flag input control functions select which flag or flags will be set to the current value of the flag input ($\overline{FI}$) line.

Data on $\overline{FI}$ is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Flag Output Control Functions

The flag output control functions select the value to which the flag output ($\overline{FO}$) line will be forced.

FLAG CONTROL FUNCTION TABLE

MNEMONIC	FUNCTION DESCRIPTION
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z-flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTION TABLE

MNEMONIC	FUNCTION DESCRIPTION
FF0	Force FO to 0. FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC_1	0
Flag Input	SCZ	Set C-flag and Z-flag to f	0	0
	STZ	Set Z-flag to f	0	1
	STC	Set C-flag to f	1	0
	HCZ	Hold C-flag and Z-flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC_3	2
Flag Output	FF0	Force FO to 0	0	0
	FFC	Force FO to C-flag	1	0
	FFZ	Force FO to Z-flag	0	1
	FF1	Force FO to 1	1	1

LOAD FUNCTION	NEXT ROW					NEXT COL			
LD	MA_8	7	6	5	4	MA_3	2	1	0
0 / 1	See Address Control Function Summary								
	0	X_3	X_2	X_1	X_0	X_7	X_6	X_5	X_4

NOTE

f = Contents of the F-latch xn = Data on PX- or SX-bus line n (active low)

ADDRESS CONTROL FUNCTION SUMMARY

MNEMONIC	DESCRIPTION	FUNCTION							NEXT ROW					NEXT COL			
		AC_6	5	4	3	2	1	0	MA_8	7	6	5	4	MA_3	2	1	0
JCC	Jump in current column	0	0	d_4	d_3	d_2	d_1	d_0	d_4	d_3	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JZR	Jump to zero row	0	1	0	d_3	d_2	d_1	d_0	0	0	0	0	0	d_3	d_2	d_1	d_0
JCR	Jump in current row	0	1	1	d_3	d_2	d_1	d_0	m_8	m_7	m_6	m_5	m_4	d_3	d_2	d_1	d_0
JCE	Jump in column/enable	1	1	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JFL	Jump/test F-latch	1	0	0	d_3	d_2	d_1	d_0	m_8	d_3	d_2	d_1	d_0	m_3	0	1	f
JCF	Jump/test C-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	c
JZF	Jump/test Z-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	Z
JPR	Jump/test PR-latch	1	1	0	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	p_3	p_2	p_1	p_0
JLL	Jump/test left PR bits	1	1	0	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	0	1	p_3	p_2
JRL	Jump/test right PR bits	1	1	1	1	1	d_1	d_0	m_8	m_7	1	d_1	d_0	1	1	p1	p_0
JPX	Jump/test PX-bus	1	1	1	1	0	d_1	d_0	m_8	m_7	m_6	d_1	d_0	x_7	x_6	x_5	x_4

NOTE

dn = Data on address control line n
mn = Data in microprogram address register bit n
Pn = Data in PR-latch bit n
xn = Data on PX-bus line n (active low)
f,c,z = Contents of F-latch, C-flag, or Z-flag, respectively

STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active high at the rising edge of the clock, the data on the primary and secondary instruction buses, PX_4-PX_7 and SX_0-SX_3, is loaded into the microprogram address register. PX_4-PX_7 are loaded into MA_0-MA_7 and SX_0-SX_3 are loaded into MA_4-MA_7. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

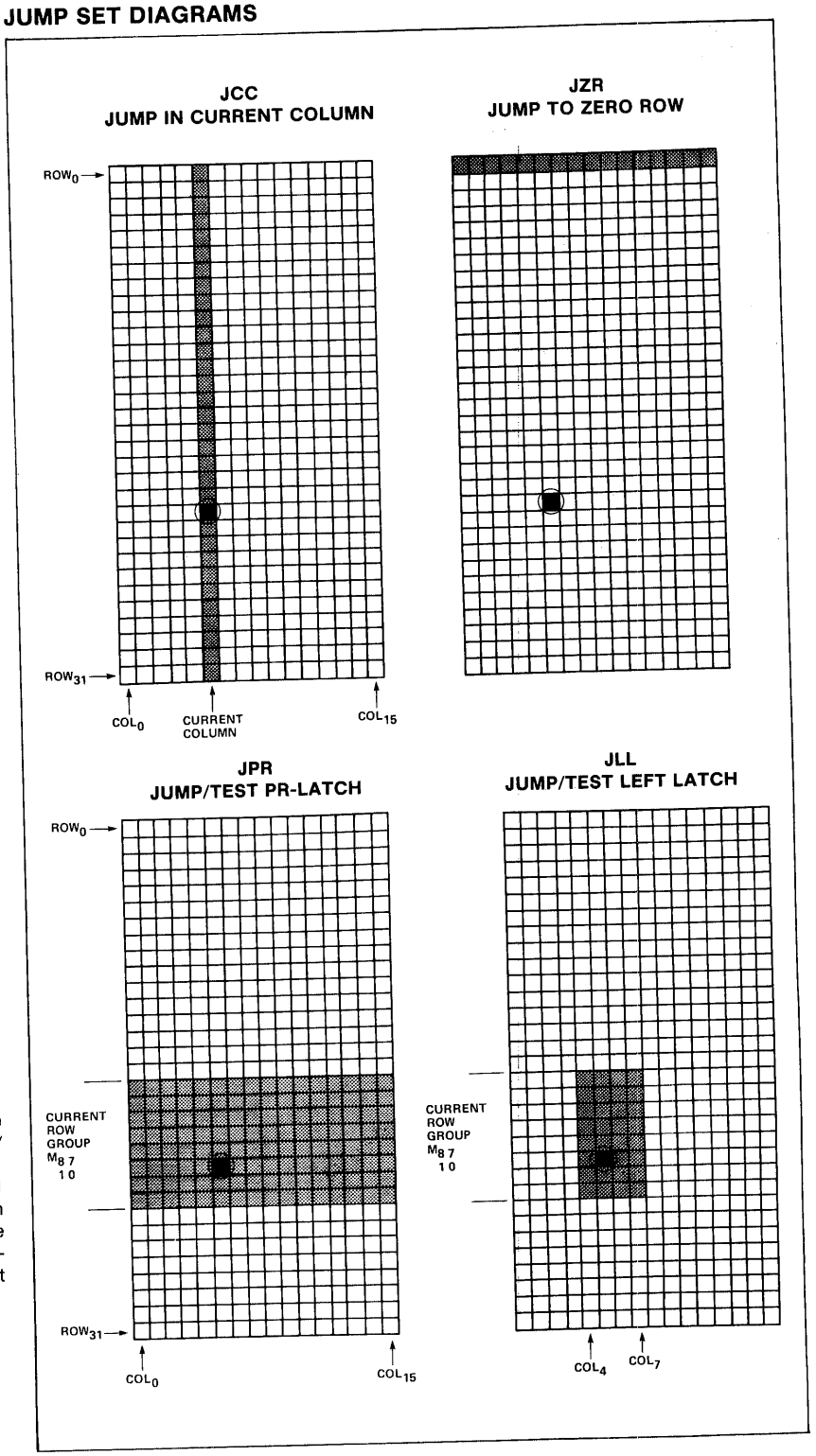
The MCU generates an interrupt strobe enable on the output line designated ISE. The line is placed in the active high state whenever a JZR to col_{15} is selected as the address control function. Generally, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so the interrupt control may be enabled at the beginning of the fetch/execute cycle. The interrupt control responds to the interrupt by pulling the enable row address (ERA) input line low to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC_0-AC_6. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

JUMP SET DIAGRAMS

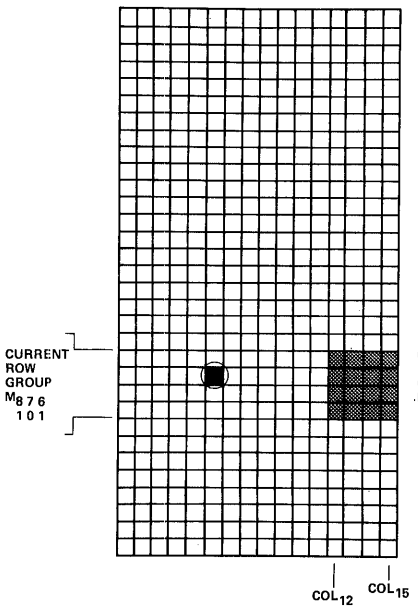
The following 10 diagrams illustrate the jump set for each of the 11 jump and jump/test functions of the MCU. Location 341 indicated by the circled square, represents 1 current row (row_{21}) and current column (col_5) address. The dark boxes indicate the microprogram locations that may be selected by the particular function as the next address.

JUMP SET DIAGRAMS

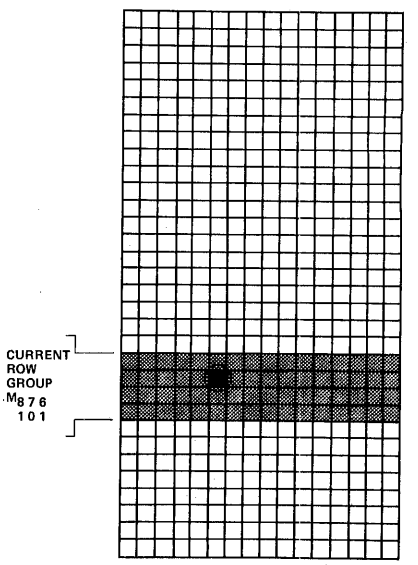


JUMP SET DIAGRAMS (Cont'd)

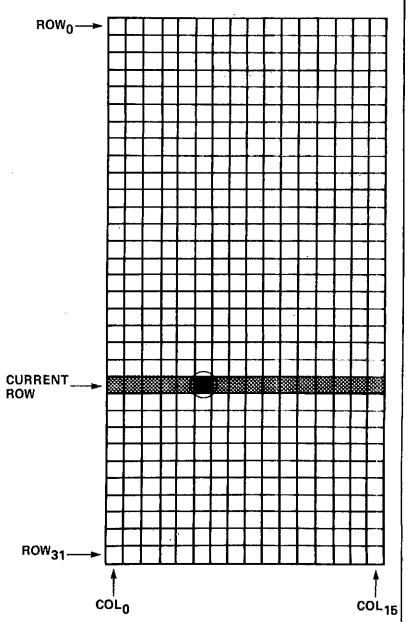
JRL
JUMP/TEST RIGHT LATCH



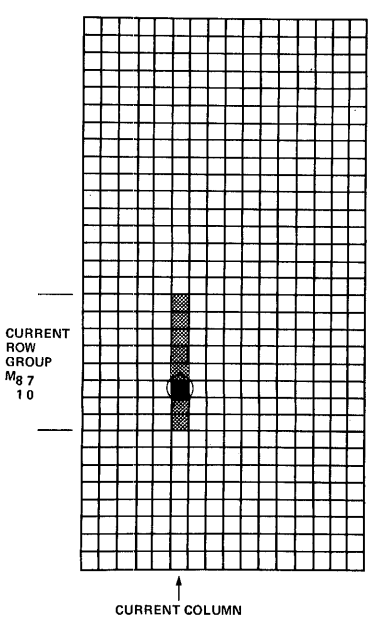
JPX
JUMP/TEST PX-BUS



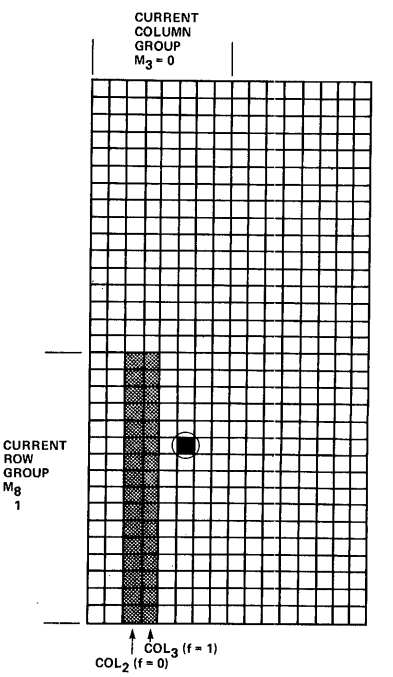
JCR
JUMP IN CURRENT ROW



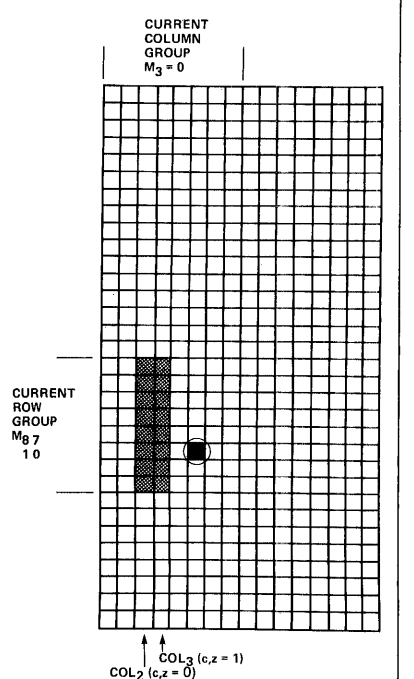
JCE
JUMP COLUMN/ENABLE



JFL
JUMP/TEST F-LATCH



JCF, JZF
JUMP/TEST C-FLAG
JUMP/TEST Z-FLAG



S/N3001-I

AC ELECTRICAL CHARACTERISTICS

N3001 T_A = 0°C to +70°C, V_{CC} = 5.0V, ± 5%

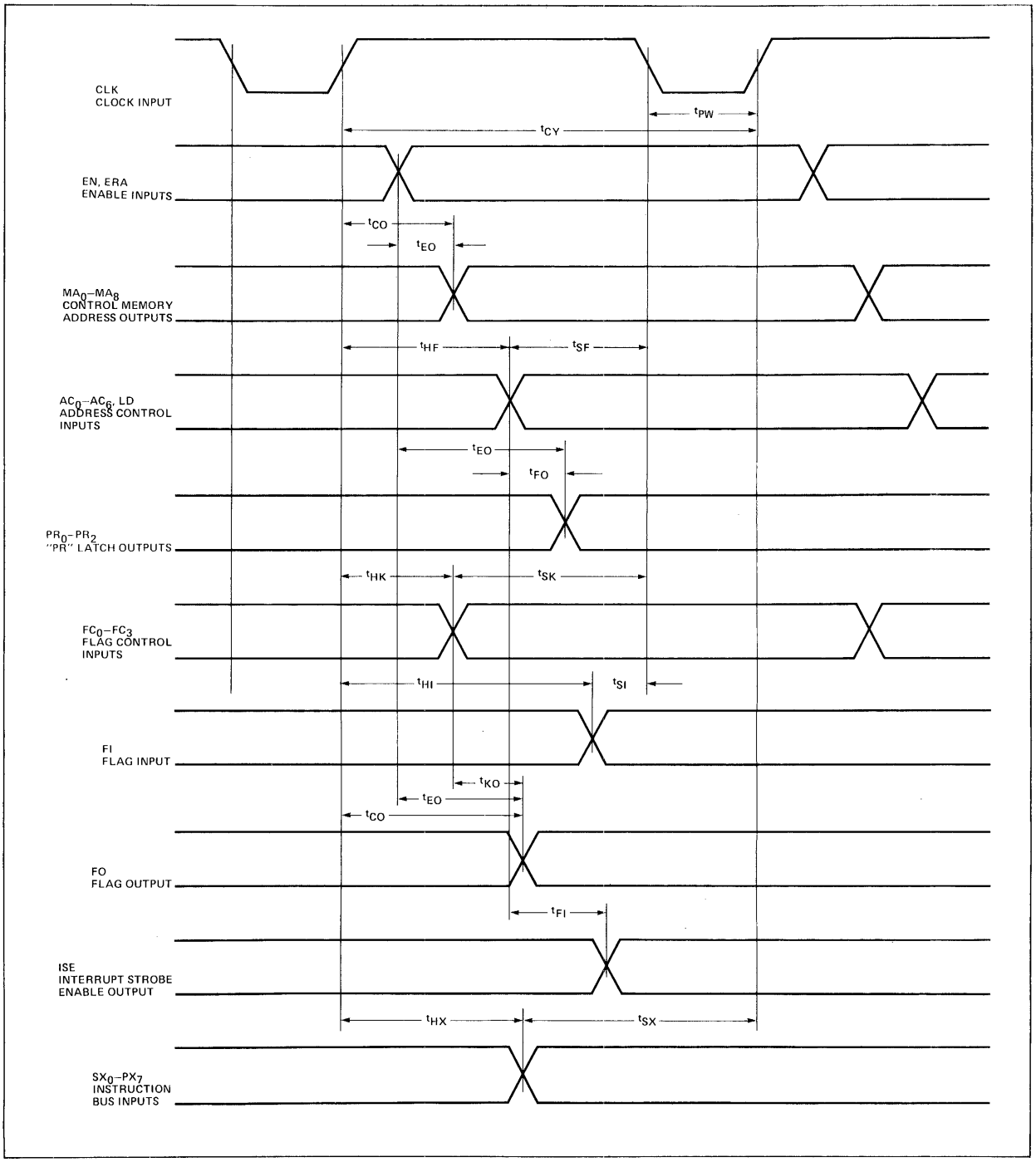
S3001 T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

PARAMETER		N3001			S3001			UNIT
		Min	Typ[1]	Max	Min	Typ[1]	Max	
t_{CY}	Cycle Time[2]	60	45		95	45		ns
t_{PW}	Clock Pulse Width	17	10		40	10		ns
	Control and Data Input Set-Up Times:							
t_{SF}	LD, AC_0-AC_6 (Set to "1"/"0")	20	3/14		20	3/14		ns
t_{SK}	FC_0, FC_1	7	5		10	5		ns
t_{SX}	PX_4-PX_7 (Set to "1"/"0")	28	4/13		35	4/13		ns
t_{SI}	FI (Set to "1"/"0")	12	-6/0		15	-6/10		ns
t_{SX}	SX_0-SX_3	15	5		35	5		ns
	Control and Data Input Hold Times:							
t_{HF}	LD, AC_0-AC_6 (Hold to "1"/"0")	4	-3/-14		5	-3/-14		ns
t_{HK}	FC_0, FC_1	4	-5		10	-5		ns
t_{HX}	PX_4-PX_7 (Hold to "1"/"0")	0	-4/-13		25	-4/-13		ns
t_{HI}	FI (Hold to "1"/"0")	16	6.5/0		22	6.5/0		ns
t_{HX}	SX_0-SX_3	0	-5		25	-5		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (mA_0-mA_8, FO) (tPHL/tPLH)		17/24	36	10	17/24	45	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		13	24		13	50	ns
t_{FO}	Propagation Delay from Control Inputs AC_0-AC_6 to Latch Outputs (PR_0-PR_2)		21	32		21	50	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (mA_0-mA_8, FO, PR_0-PR_2)		17	26		17	35	ns
t_{FI}	Propagation Delay from Control Inputs AC_0-AC_6 to Interrupt Strobe Enable Output (ISE)		20	32		20	40	ns

NOTE

1. Typical values are for TA = 25°C and 5.0 supply voltage.
2. S3001: tCY = tWP + tSF + tCO

VOLTAGE WAVEFORMS



DESCRIPTION

The N3002 Central Processing Element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by microinstructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM memory.

FEATURES

- **45ns cycle time (typ)**
- **Easy expansion to multiple of 2 bits**
- **11 general purpose registers**
- **Full function accumulator**
- **Useful functions include:**
  - **2's complement arithmetic**
  - **Logical AND, OR, NOT, exclusive-NOR**
  - **Increment, decrement**
  - **Shift left/shift right**
  - **Bit testing and zero detection**
  - **Carry look-ahead generation**
  - **Masking via K-bus**
  - **Conditioned clocking allowing non-destructive testing of data in accumulator and scratchpad**
- **3 input buses**
- **2 output buses**
- **Control bus**

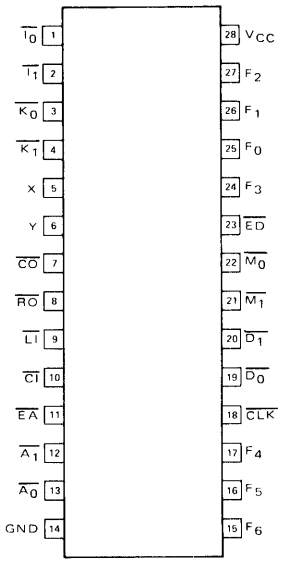
FUNCTION TRUTH TABLE

FUNCTION GROUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

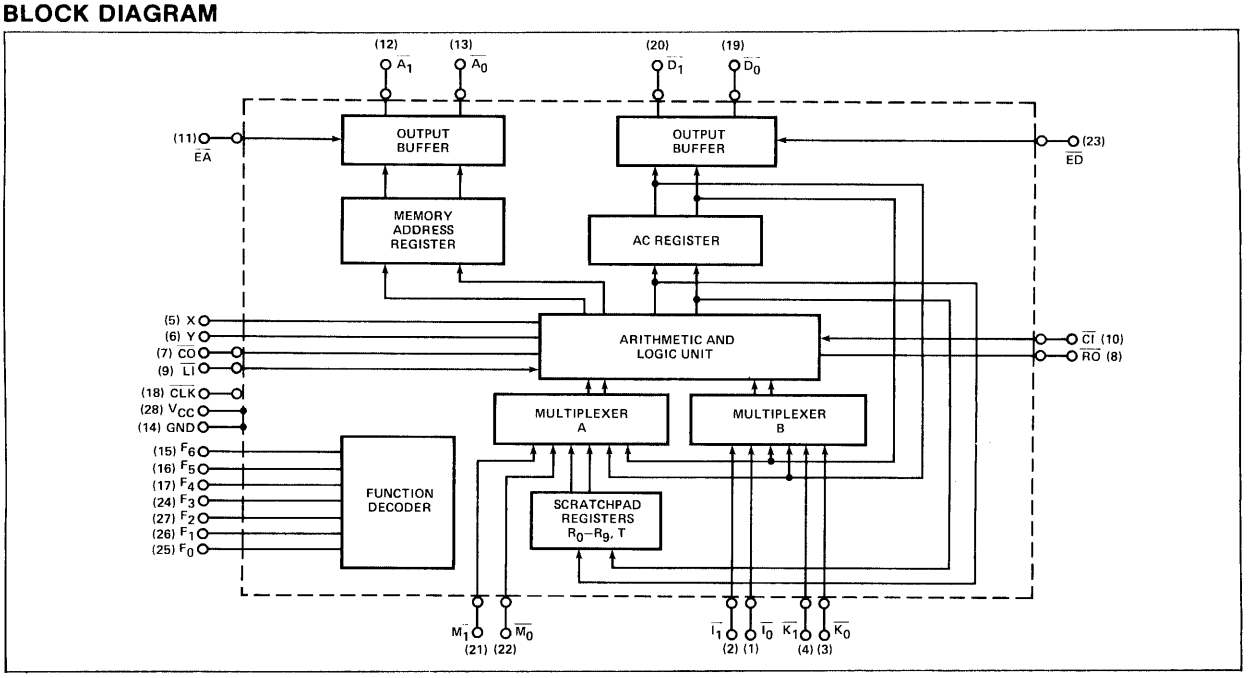
REGISTER GROUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

PIN CONFIGURATION

I,XL PACKAGE



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1, 2	$\overline{I_0}$-$\overline{I_1}$	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active low
3, 4	$\overline{K_0}$-$\overline{K_1}$	Mask Bus Inputs The mask bus inputs provide a separate input port from the microprogram memory, to allow mask or constant entry.	Active low
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the 74S182 Look-Ahead Carry Generator	Active high
7	$\overline{CO}$	Ripple Carry Out The ripple carry output is only disabled during shift right operations.	Active low Three-state
8	$\overline{RO}$	Shift Right Output The shift right output is only enabled during shift right operations.	Active low Three-state
9	$\overline{LI}$	Shift Right Input	Active low
10	$\overline{CI}$	Carry Input	Active low
11	$\overline{EA}$	Memory Address Enable Input When in the low state, the memory address enable input enables the memory address outputs (A_0-A_1).	Active low
12-13	$\overline{A_0}$-$\overline{A_1}$	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active low Three-state
14	GND	Ground	
14-17, 24-27	F_0-F_6	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	Active high
18	$\overline{CLK}$	Clock Input	
19-20	$\overline{D_0}$-$\overline{D_1}$	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active low Three-state
21-22	$\overline{M_0}$-$\overline{M_1}$	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active low
23	$\overline{ED}$	Memory Data Enable Input When in the low state, the memory data enable input enables the memory data outputs (D_0-D_1).	Active low
28	V_{CC}	+5 Volt Supply	

SYSTEM DESCRIPTION

Microfunction Decoder and K-Bus

Basic microfunctions are controlled by a 7-bit bus (F_0-F_6) which is organized into 2 groups. The higher 3 bits (F_4-F_6) are designated as F-Group and the lower 4 bits (F_0-F_3) are designated as the R-Group. The F-Group specifies the type of operation to be performed and the R-Group specifies the registers involved.

The F-Bus instructs the microfunction decoder to:
- Select ALU functions to be performed
- Generate scratchpad register address
- Control A and B multiplexer

The resulting microfunction action can be:
- Data transfer
- Shift operations
- Increment and decrement
- Initialize stack
- Test for zero conditions
- 2's complement addition and subtraction
- Bit masking
- Maintain program counter

A and B Multiplexers

A and B multiplexers select the proper 2 operands to the ALU.

A multiplexer selects inputs from one of the following:
- M-bus (data from main memory)
- Scratchpad registers
- Accumulator

B multiplexer selects inputs from one of the following:
- I-bus (data from external I/O devices)
- Accumulator
- K-bus (literal or masking information from micro-program memory)

Scratchpad Registers

- Contains 11 registers (R_0-R_9, T)
- Scratchpad register outputs are multiplexed to the ALU via the A multiplexer
- Used to store intermediate results from arithmetic/logic operations
- Can be used as program counter

Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations of the CPE.

Arithmetic operations are:
- 2's complement addition
- Incrementing
- Decrementing
- Shift left
- Shift right

Logical operations are:
- Transfer
- AND
- Inclusive-OR
- Exclusive-NOR
- Logic complement

ALU operation results are then stored in the accumulator and/or scratchpad registers. For easy expansion to larger arrays, carry look-ahead outputs (X and Y) and cascading shift inputs (LI, RO) are provided.

Accumulator

- Stores results from ALU operations
- The output of accumulator is multiplexed into ALU via the A and B multiplexer as one of the operands

Input Buses

M-bus: Data bus from main memory
- Accepts 2 bits of data from main memory into CPE
- Is multiplexed into the ALU via the A multiplexer

I-bus: Data bus from input/output devices
- Accepts 2 bits of data from external input/output devices into CPE
- Is multiplexed into the ALU via the B multiplexer

K-bus: A special feature of the N3002 CPE
- During arithmetic operations, the K-bus can be used to **mask** portions of the field being operated on
- Select or remove accumulator from operation by placing K-bus in all "1" or all "0" state respectively
- During non-arithmetic operation, the carry circuit can be used in conjunction with the K-bus for word-wise-OR operation for bit testing
- Supply literal or constant data to CPE

Output Buses

A-bus and Memory Address Register
- Main memory address is stored in the memory address register (MAR)
- Main memory is addressed via the A-bus
- MAR and A-bus may also be used to generate device address when executing I/OO instruc-instructions
- A-bus has Tri-State outputs

D-bus: Data bus from CPE to main memory or to I/O devices
- Sends buffered accumulator outputs to main memory or the external I/O devices
- D-bus has Tri-State outputs

FUNCTION DESCRIPTION

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
0	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	**Logically AND AC with the K-bus.** Add the result to R_n and carry input (CI). Deposit the sum in AC and R_n.
		OO	ILR	$R_n + CI \rightarrow R$, AC	Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the result in AC.
		11	ALR	$AC + R_n + CI \rightarrow R_n, AC$	Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.
0	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
0	III	XX	—	$AT_L \wedge (\overline{I_L \wedge K_L}) \rightarrow RO$ $LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)]$ $[AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	None
		OO	SRA	$AT_L \rightarrow RO$ $AT_H \rightarrow AT_L$ $L_I \rightarrow AT_H$	Shift AC or T, as specified, right one bit position. Place the previous low order bit value on RO and fill the high order bit from the data on LI. Used to shift or rotate AC or T right one bit.
1	I	XX	—	$K \vee R_n \rightarrow MAR$ $R_n + K + CI \rightarrow R_n$	**Logically OR R_n with the K-bus.** Deposit the result in MAR. Add the K-bus to Rn and CI. Deposit the result in R_n.
		OO	LMI	$Rn \rightarrow MAR$, $Rn + CI \rightarrow Rn$	Load MAR from R_n. Conditionally increment R_n. Used to maintain a macro-instruction program counter.
		11	DSM	$11 \rightarrow MAR$, $Rn - 1 + CI \rightarrow Rn$	Set MAR to all ones. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement Rn.
1	II	XX	—	$KVM \rightarrow MAR$ $M + K + CI \rightarrow AT$	**Logically OR the M-bus with the K-Bus.** Deposit the result in MAR. Add the K-bus to the M-bus and CI. Deposit the sum in AC or T.
		OO	LMM	$M \rightarrow MAR$, $M + CI \rightarrow AT$	Load MAR from the M-bus. Add CI to the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.
		11	LDM	$11 \rightarrow MAR$ $M - 1 + CI \rightarrow AT$	Set MAR to all ones. Subtract one from the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
1	III	XX	—	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	**Logically OR the K-bus with the complement of AC or T, as specified.** Add the result to the logical AND of specified register with the K-bus. Add the sum to CI. Deposit the result in the specified register.
		OO	CIA	$\overline{AT} + CI \rightarrow AT$	Add CI to the complement of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.
		11	DCA	$\overline{AT} - 1 + CI \rightarrow AT$	Subtract one from AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.
2	I	XX	—	$(AC \wedge K) - 1 + CI \rightarrow R_n$	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in R_n.
		OO	CSR	$CI - 1 \rightarrow R_n$ (See Note 1)	Subtract one from CI and deposit the difference in Rn. Used to conditionally clear or set R_n to all 0's or 1's, respectively.
		11	SDR	$AC - 1 + CI \rightarrow R_n$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in R_n. Used to store AC in R_n or to store the decremented value of AC in R_n.
2	II	XX	—	$(AC \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$ (See Note 1)	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	SDA	$AC - 1 + CI \rightarrow AT$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in AC or T. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.
2	III	XX	—	$(I \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the data of the K-bus with the data on the I-bus.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	LDI	$I - 1 + CI \rightarrow AT$	Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified. Used to load input bus data or decremented input bus data in the specified register.
3	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n$	**Logically AND AC with the K-bus.** Add R_n and CI to the result. Deposit the sum in R_n.
		OO	INR	$R_n + CI \rightarrow R_n$	Add CI to R_n and deposit the sum in R_n. Used to increment R_n.
		11	ADR	$AC + R_n + CI \rightarrow R_n$	Add AC to R_n. Add the result to CI and deposit the sum in R_n. Used to add the accumulator to a register or to add the incremented value of the accumulator to a register.
3	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.

NOTE

1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
3	III	XX	—	AT + (I ∧ K) + CI → AT	**Logically AND the K-bus with the I-bus.** Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.
		OO	INA	AT + CI → AT	Conditionally increment AC or T. Used to increment AC or T.
		11	AIA	I + AT + CI → AT	Add the I-bus to AC or T. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.
4	I	XX	—	CI ∨ (R_n ∧ AC ∧ K) → CO R_n ∧ (AC ∧ K) → R_n	**Logically AND the K-bus with AC.** Logically AND the result with the contents of R_n. Deposit the final result in R_n. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.
		OO	CLR	CI → CO, O → R_n	Clear R_n to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	ANR	CI ∨ (R_n ∧ AC) → CO R_n ∧ AC → R_n	Logically AND AC with R_n. Deposit the result in R_n. Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.
4	II	XX	—	CI ∨ (M ∧ AC ∧ K) → CO M ∧ (AC ∧ K) → AT	**Logically AND the K-bus with AC.** Logically AND the result with the M-bus. Deposit the final result in AC or T. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANM	CI ∨ (M ∧ AC) → CO M ∧ AC → AT	Logically AND the M-bus with AC. Deposit the result in AC or T. Force CO to one if the result is non-zero. Used to AND M-bus data to the accumulator and test for a zero result.
4	III	XX	—	CI ∨ (AT ∧ 1 ∧ K) → CO AT ∧ (I ∧ K) → AT	**Logically AND the I-bus with the K-bus.** Logically AND the result with AC or T. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANI	CI ∨ (AT ∧ I) → CO AT ∧ 1 → AT	Logically AND the I-bus with AC or T, as specified. Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.
5	I	XX	—	CI ∨ (R_n ∧ K) → CO K ∧ R_n → R_n	**Logically AND the K-bus with R_n.** Deposit the result in Rn. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLR	CI → CO, O → R_n	Clear Rn to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	TZR	CI ∨ R_n → CO R_n → R_n	Force CO to one if Rn is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register for masking and, optionally, testing for a zero result.
5	II	XX	—	CI ∨ (M ∧ K) → CO K ∧ M → AT	**Logically AND the K-bus with the M-bus.** Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	LTM	CI ∨ M → CO M → AT	Load AC or T, as specified, from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for a zero result. Also used to AND the K-bus with the M-bus for masking and, optionally, testing for a zero result.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
5	III	XX	—	CI ∨ (AT ∧ K) → CO K ∧ AT → AT	Logically AND the K-bus with AC or T, as specified. Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	TZA	CI ∨ AT → CO AT → AT	Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND the K-bus to the specified register for masking and, optionally, testing for a zero result.
6	I	XX	—	CI ∨ (AC ∧ K) → CO R_n ∨ (AC ∧ K) → R_n	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the result of the carry OR on CO. Logically OR R_n with the logical AND of AC and the K-bus. Deposit the result in R_n.
		OO	NOP	CI → CO, R_n → R_n	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORR	CI ∨ AC → CO R_n ∨ AC → R_n	Force CO to one if AC is non-zero. Logically OR AC with R_n. Deposit the result in R_n. Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.
6	II	XX	—	CI ∨ (AC ∧ K) → CO M ∨ (AC ∧ K) → AT	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the carry OR on CO. Logically OR the M-bus, with the logical AND of AC and the K-bus. Deposit the final result in AC or T.
		OO	LMF	CI → CO, M → AT	Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to CI.
		11	ORM	CI ∨ AC → CO M ∨ AC → AT	Force CO to one if AC is non-zero. Logically OR the M-bus with AC. Deposit the result in AC or T, as specified. Used to OR M-bus with the AC and, optionally, test the previous value of AC for zero.
6	III	XX	—	CI ∨ (I ∧ K) → CO AT ∨ (I ∧ I) → AT	Logical OR CI with the word-wise OR of the logical AND of the I-bus and the K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Logically OR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	NOP	CI → CO, AT → AT	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORI	CI ∨ I → CO I ∨ AT →	Force CO to one if the data on the I-bus is non-zero. Logically OR the I-bus to AC or T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.
7	I	XX	—	CI ∨ (R_n ∧ AC ∧ K) → CO R_n $\overline{\oplus}$ (AC ∧ K) → R_n	Logically OR CI with the word-wise OR of the logical AND of R_n and AC and the K-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive-NOR the result with R_n. Deposit the final result in R_n.
		OO	CMR	CI → CO, Rn → Rn	Complement the contents of R_n. Force CO to CI.
		11	XNR	CI ∨ (R_n ∧ AC) → CO R_n $\overline{\oplus}$ AC → R_n	Force CO to one if the logical AND of AC and Rn is non-zero. Exclusive-NOR AC with R_n. Deposit the result in R_n. Used to exclusive-NOR the accumulator with a register.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
7	II	XX	—	CI ∨ (M ∧ AC ∧ K) → CO M $\overline{\oplus}$ (AC ∧ K) → AT	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus and M-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive NOR the result with the M-bus. Deposit the final result in AC or T.
		OO	LCM	CI → CO, $\overline{M}$ → AT	Load the complement of the M-bus into AC or T, as specified. Force CO to CI.
		11	XNM	CI ∨ (M ∧ AC) → CO M $\oplus$ AC → AT	Force CO to one if the logical AND of AC and the M-bus is non-zero. Exclusive-NOR AC with the M-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR memory data with the accumulator.
7	III	XX	—	CI ∨ (AT ∧ I ∧ K) → CO AT $\overline{\oplus}$ (I K) → AT	Logically OR CI with the word-wise OR of the logical AND of the specified register and the I-bus and K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Exclusive-NOR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	CMA	CI → CO $\overline{AT}$ → AT	Complement AC or T, as specified. Force CO to CI.
		11	XNI	CI ∨ (AT ∧ I) → CO I $\overline{\oplus}$ AT → AT	Force CO to one if the logical AND of the specified register and the I-bus is non-zero. Exclusive-NOR AC with the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

FUNCTION DESCRIPTION KEY

SYMBOL	MEANING
I,K,M	Data on the I, K, and M buses, respectively
CI,LI	Data on the carry input and left input, respectively
CO,RO	Data on the carry output and right output, respectively
Rn	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L,H	As subscripts, designate low and high order bit, respectively
+	2's complement addition
-	2's complement subtraction
∧	Logical AND
∨	Logical OR
⊕	Exclusive-NOR
→	Deposit into

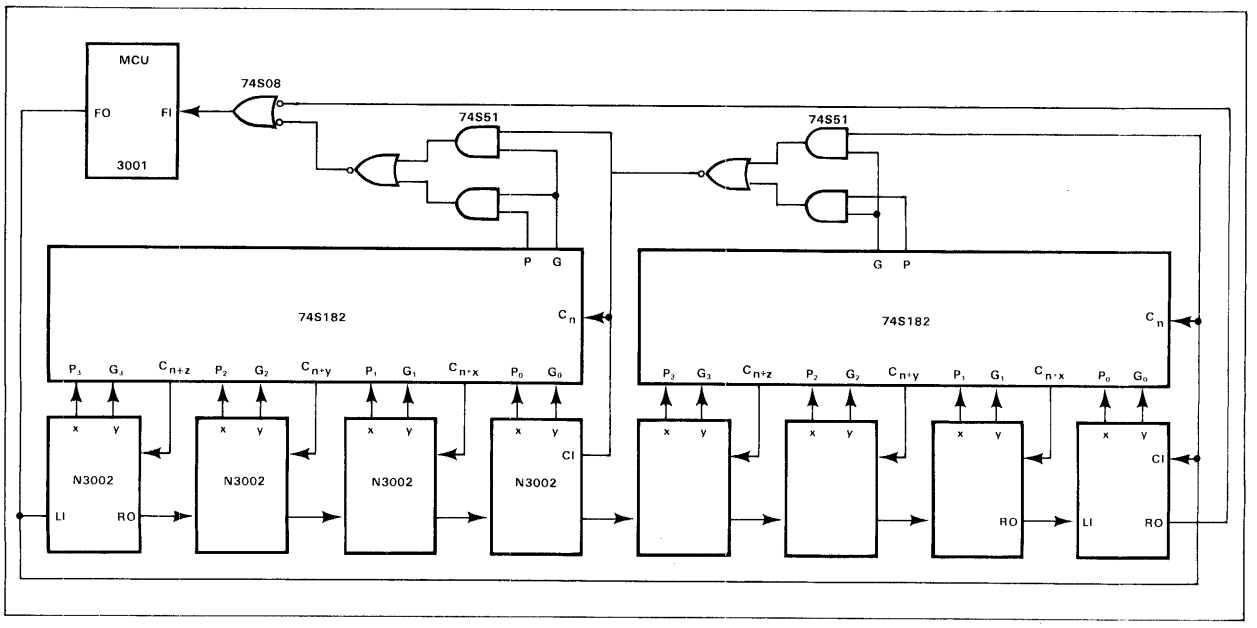
AC ELECTRICAL CHARACTERISTICS

N3001 = T_A = 0°C to +70°C, V_{CC} = 5V ± 5%
S3001 = T_A = -55°C to +125°C, V_{CC} = 5V ± 10%

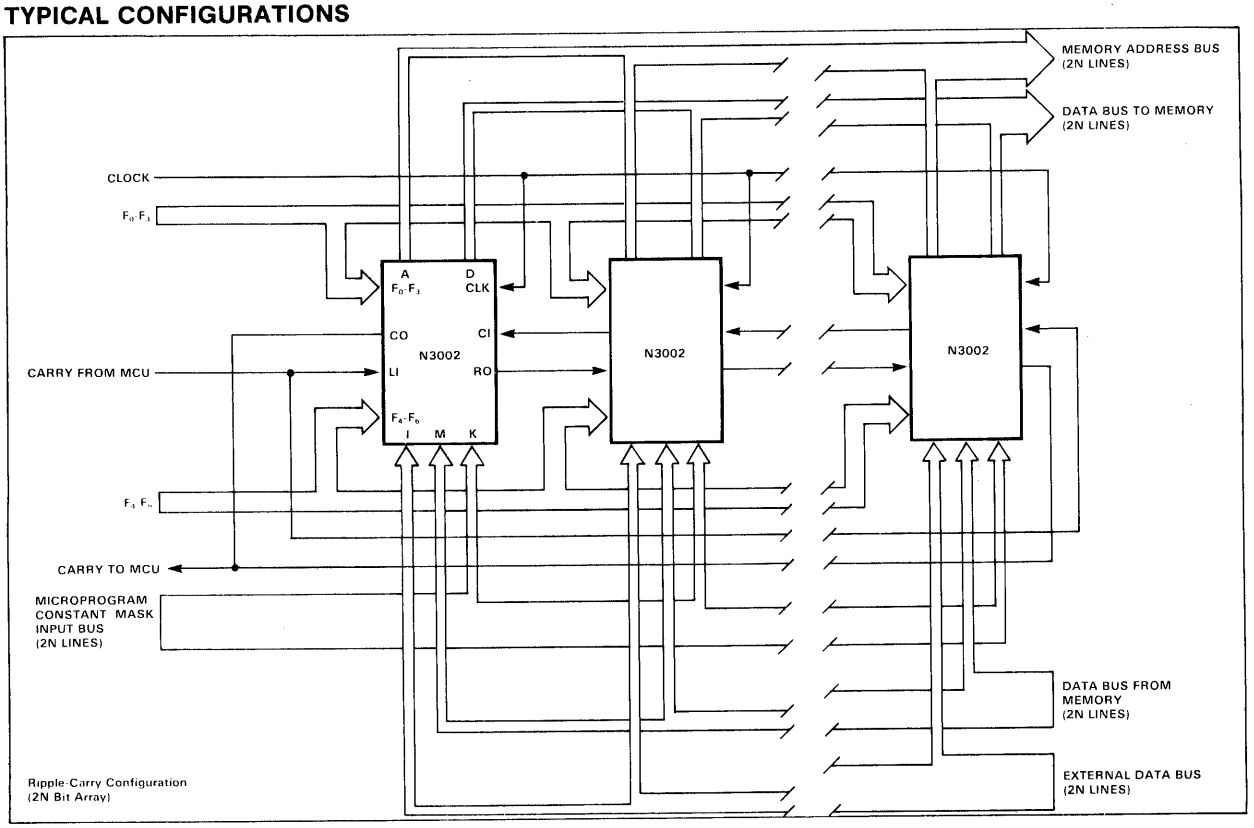
PARAMETER	N3002			S3002			UNIT
	Min	Typ*	Max	Min	Typ*	Max	
tCY Clock Cycle Time	70	45		120	45		ns
tWP Clock Pulse Width	17	10		42	10		ns
tFS Function Input Set-Up Time (F_0 through F_6)	48	-23 → 35		70	-23 → 35		ns
Data Set-Up Time:							
tDS I_0, I_1, M_0, M_1, K_0, K_1	40	12 → 29		60	12 → 29		ns
tSS LI, CI	21	0 → 7		30	0 → 7		ns
Data and Function Hold Time:							
tFH F_0 through F_6	4	0		5	0		ns
tDH I_0, I_1, M_0, M_1, K_0, K_1	4	-28 → -11		5	-28 → -11		ns
tSH LI, CI	12	-7 → 0		15	-7 → 0		ns
Propagation Delay to X, Y, RO from:							
tXF Any Function Input		28	52		28	65	ns
tXD Any Data Input		16 → 20	33		16 → 20	65	ns
tXT Trailing Edge of CLK		33	48		33	75	ns
tXL Leading Edge of CLK	13	18 → 40	70	13	18 → 40	90	ns
Propagation Delay to CO from:							
tCL Leading Edge of CLK	16	24 → 44	70		24 → 44	90	ns
tCT Trailing Edge of CLK		30 → 40	56		30 → 40	100	ns
tCF Any Function Input		25 → 35	52		25 → 35	75	ns
tCD Any Data Input		17 → 23	55		17 → 23	65	ns
tCC CI (Ripple Carry)		9 → 13	20		9 → 13	30	ns
Propagation Delay to A_0, A_1, D_0, D_1 from:							
tDL Leading Edge of CLK		17 → 25	40		17 → 25	75	ns
tDE Enable Input ED, EA		10 → 12	20		10 → 12	35	ns

* NOTE
Typical values are for T_A = 25°C and typical supply voltage.

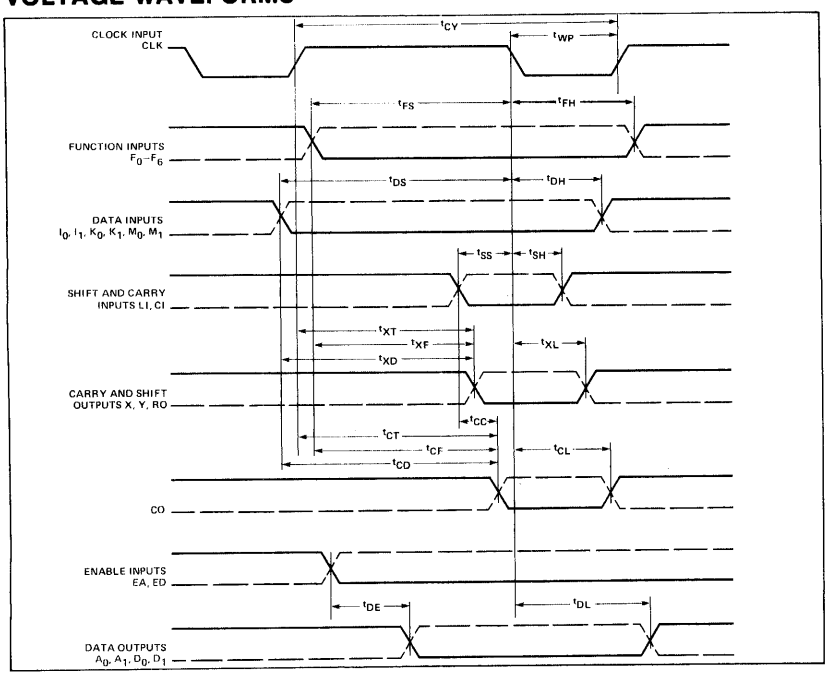
CARRY LOOK-AHEAD CONFIGURATION



TYPICAL CONFIGURATIONS



VOLTAGE WAVEFORMS



INTRODUCTION

A Microcomputer Designed for Control

The 8X300 is a microcomputer designed for control. It features:

Execution Speed

- 250ns instruction execution time
- Direct address capability—up to 8192 16-bit words of program memory
- Eight 8-bit general purpose registers
- Simultaneous data transfer and data edit in a single instruction cycle time
- n-way branch or n-entry table lookup in 2 instruction cycle times
- 8X300 instructions operate with equal speed on 1-bit, 2-bit, 3-bit, 4-bit, 5-bit, 6-bit, 7-bit, or 8-bit data formats

The 8X300 instruction set features control-oriented instructions which directly access variable length input/output and internal data fields. These instructions provide very high performance for moving and interpreting data. This makes the 8X300 ideal in switching, controlling, and editing applications.

Direct Processing of External Data

The 8X300 I/O system is treated as a set of internal registers. Therefore data from external devices may be processed (tested, shifted, added to, etc.) without first moving them to internal storage. In fact, the entire concept is to treat data at the I/O interface no differently than internal data. This concept extends to the software which allows variables at the input/output system to be named and treated in the same way as data in storage.

Separate Program Storage and Data Storage

The storage concept of the 8X300 is to separate program storage from data storage. Program storage is implemented in read-only memory in recognition of the fact that programs for control applications are fixed and dedicated. The benefits of using read-only memory are that great speeds may be obtained at lower cost than if read/write memory were used, and that program instructions reside in a non-volatile medium and cannot be altered by system power failures.

8X300 Architecture

Figure 1 of the 8X300 data sheet illustrates the 8X300 architecture. The 8X300 contains an Arithmetic Logic Unit (ALU), Program Counter, and an Address Register. Eight 8-bit general purpose registers are also provided, including 7 working registers and an auxiliary register which performs as a working register and also provides an implied operand for many instructions. The 8X300 registers are shown in Figure 1 of the 8X300 data sheet and are summarized below:

Control Registers include:

- Instruction—A 16-bit register containing the current instruction
- Program Storage Address Register (AR)—A 13-bit register containing the address of the current instruction being accessed from Program Storage
- Program Counter (PC)—A 13-bit register containing the address of the next instruction to be read from Program Storage

Data Registers include:

- Working Registers (WR)—Seven 8-bit registers for data storage
- Overflow (OVF)—A 1-bit register that retains the most significant bit position carry from ALU addition operation. Arithmetically treated as 2^0.
- Auxiliary (AUX)—An 8-bit register. Source of implied operand for arithmetic and logical instructions. May be used as a working register.

A crystal external to the CPU may be used to generate the CPU system clock. The CPU executes 8 instruction types.

DESCRIPTION

The Signetics 8X300 Microcontroller is a monolithic, high-speed microprocessor implemented with bipolar Schottky technology. As the central processing unit, CPU, it allows 16-bit instructions to be fetched, decoded and executed in 250ns. A 250ns instruction cycle requires maximum memory access of 65ns, and maximum I/O device access of 35ns.

Microcontroller instructions operate on 8-bit, parallel data. Logic is distributed along the data path within the Microcontroller. Input data can be rotated and masked before being subject to an arithmetic or logical operation; and output data can be shifted and merged with the input data, before being output to external logic. This allows 1- to 8-bit I/O and data memory fields to be accessed and processed in a single instruction cycle.

PROGRAM STORAGE INTERFACE

Program Storage is typically connected to the A0-A12 (A12 is least significant bit) and I0-I15 signal lines. An address output on A0-A12 identifies one 16-bit instruction word in program storage. The instruction word is subsequently input on I0-I15 and defines the Microcontroller operations which are to follow.

The Signetics 82S115 PROM, or any TTL compatible memory, may be used for program storage.

I/O DEVICES INTERFACE

An 8-bit I/O bus, called the Interface Vector (IV) data bus, is used by the Microcontroller to communicate with 2 fields of I/O devices. The complementary $\overline{LB}$ and $\overline{RB}$ signals identify which field of the I/O devices is selected.

Both I/O data and I/O address information can be output on the IV bus. The SC and WC signals are typically used to distinguish between I/O data and I/O address information as follows:

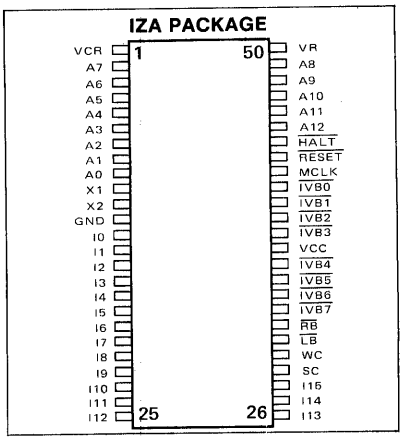
SC	WC	
1	0	I/O address is being output on IV bus
0	1	I/O data is being output on IV bus
0	0	I/O data is expected on the IV, bus, as input to the Microcontroller
1	1	Not generated by the Microcontroller

The Signetics 82SXXX series RAM, and the 8T32/33 may be attached to the IV bus.

FEATURES

- **185ns instruction decode and execute delay (with Signetics 8T32/33 I/O port)**
- **Eight 8-bit working registers**
- **Single instruction access to 1-bit, 2-bit, 3-bit or 8-bit field on I/O bus**
- **Separate instruction address, instruction, and I/O data buses**
- **On-chip oscillator**
- **Bipolar Schottky technology**
- **TTL inputs and outputs**
- **Tri-state output on I/O data bus**
- **+5 volt operation from 0° to 70°C**

PIN CONFIGURATION



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
2-9, 45-49	A0-A12:	Instruction address lines. A high level equals "1." These outputs directly address up to 8192 words of program storage. A12 is least significant bit.	Active high
13-28	I0-I15:	Instruction lines. A high level equals "1." Receives instructions from Program Storage. I_{15} is least significant bit.	Active high
33-36, 38-41	$\overline{IVB0}$-$\overline{IVB7}$	Interface Vector (IV) Bus. A low level equals "1." Bidirectional tri-state lines to communicate with I/O devices. $\overline{IVB7}$ is least significant bit.	Three-state Active low
42	$\overline{MCLK}$:	Master Clock. Output to clock I/O devices, and/or provide synchronization for external logic	
30	WC:	Write Command. High level output indicates data is being output on the IV Bus.	Active high
29	SC:	Select Command. High level output indicates that an address is being output on the IV Bus.	Active high
31	$\overline{LB}$:	Left Bank. Low level output to enable one of two sets of I/O devices ($\overline{LB}$ is the complement of RB).	Active low
32	$\overline{RB}$:	Right Bank. Low level output to enable one of two sets of I/O devices ($\overline{RB}$ is the complement of $\overline{LB}$).	Active low
44	$\overline{HALT}$:	Low level is input to stop the Microcontroller.	Active low
43	$\overline{RESET}$:	Low level is input to initialize the Microcontroller.	Active low
10-11	X1, X2:	Inputs for an external frequency determining crystal. May also be interfaced to logic or test equipment.	
50	VR	Reference voltage to pass transistor.	
1	VCR	Regulated output voltage from pass transistor.	
37	V_{CC}:	5V power connection.	
12	GND:	Ground.	

MICROCONTROLLER ARCHITECTURE

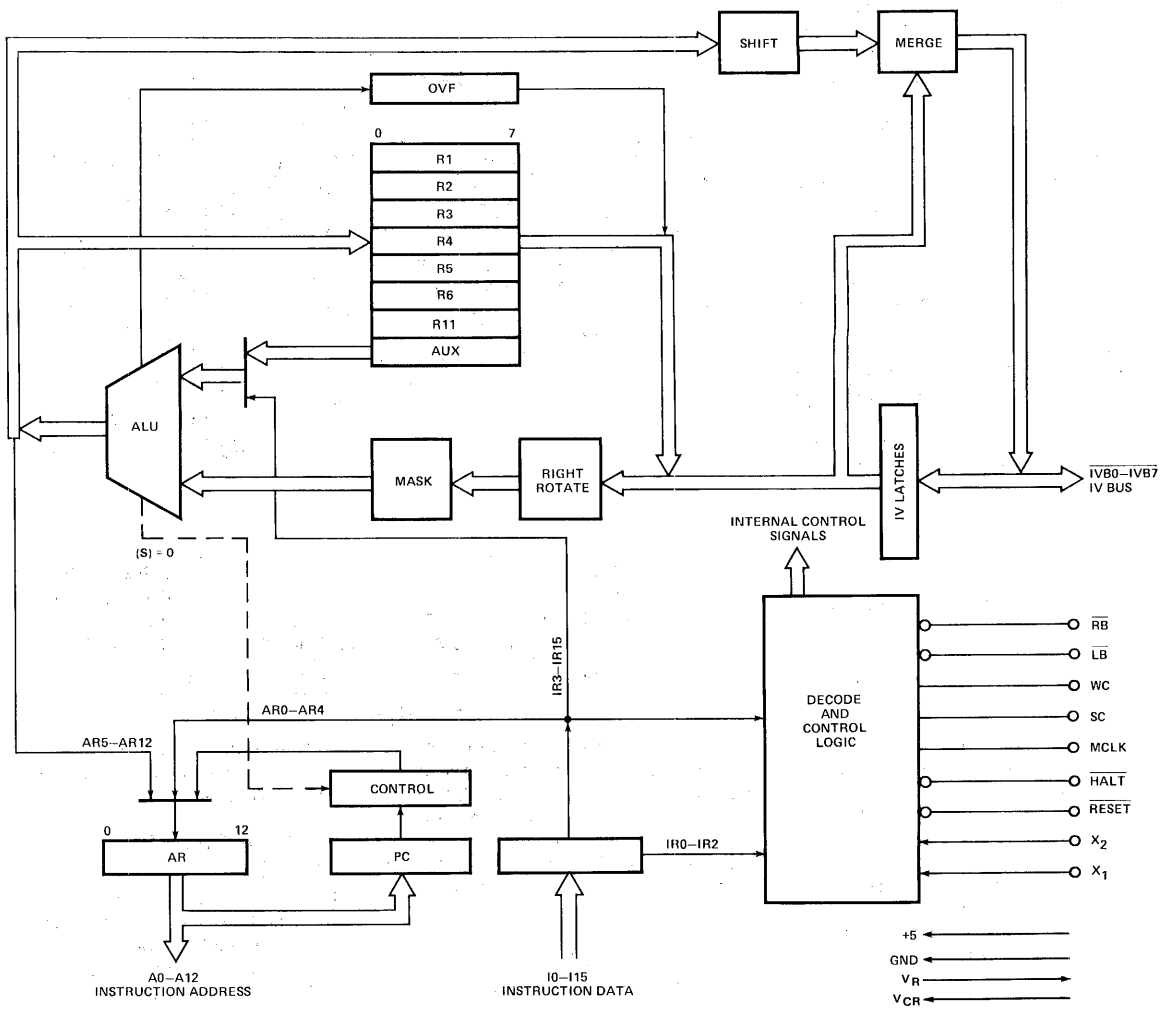


Figure 1

R1 — General working register
R2 — General working register
R3 — General working register
R4 — General working register
R5 — General working register
R6 — General working register
R11 — General working register
AUX — General working register. Contains second term for arithmetic or logical operations.

OVF — The least-significant bit of this register is used to reflect overflow status resulting from the most recent ADD operation (see Instruction Set Summary).

Instruction Register (IR)
— Holds the 16-bit instruction word currently being executed.

Program Counter (PC)
— Normally contains the address of the current instruction and is incremented to obtain the next instruction address.

Address Register (AR)
— A 13-bit register containing the address of the current instruction.

Table 1 INTERNAL REGISTERS

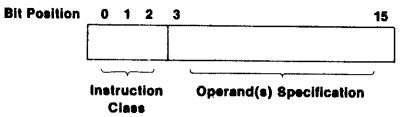
INSTRUCTION CYCLE

Each Microcontroller operation is executed in 1 instruction cycle, which may be as short as 250ns. The Microcontroller generates MCLK to synchronize external logic to the instruction cycle. Instruction cycles are subdivided into quarter cycles. MCLK is an output during the last quarter cycle.

During the third quarter cycle of an instruction, an address is output on A0-A12, identifying the location in program storage of the next instruction word. This instruction word defines the next instruction, which must be input on I0-I15 during the first quarter cycle of the next instruction cycle (see Table 2).

Instruction Set Summary

The 16-bit instruction word input on I0-I15 is decoded by the instruction decode logic to implement events that are to occur during the remainder of the instruction cycle. Generally the 16-bit instruction word is decoded as follows:



A detailed usage of the 13 "operand(s) specification" bits is given in following sections.

Three operation code bits allow for 8 instruction classes. The 8 instruction classes are summarized in Table 3. Each entry is referred to as an "instruction class" because the unique architecture of the Interpreter allows a number of powerful variations to be specified by the 13 operand(s) specification bits. A complete description of instruction formats and some instruction examples are provided in the Microprocessor Applications manual.

Data Processing

The Microcontroller architecture includes eight 8-bit working registers, an arithmetic logic unit (ALU), an overflow register, and the 8-bit IV Bus. Internal 8-bit data paths connect the registers and IV Bus to the ALU inputs, and the ALU output to the registers and IV Bus. Data processing logic is distributed along these internal 8-bit data paths. Rotate and mask logic precedes the ALU on the data entry path. Shift and merge logic follows the ALU on the data output path. All 4 sets of logic can operate on 8 data bits in a single instruction cycle (See Figure 1).

When less than 8 bits of data are specified for output to the IV bus by the ALU, the data field (shifted if necessary) is inserted into the prior contents of the IV bus latches. The IV bus latches contain data input at the start of an instruction. This data in the IV bus latches will be specified in the instruction as a) IV bus source data or b) data from an automatic read when the IV bus is specified as a destination. Therefore, IV bus bit positions outside an inserted bit field are unmodified.

TYPICAL SYSTEM CONFIGURATION

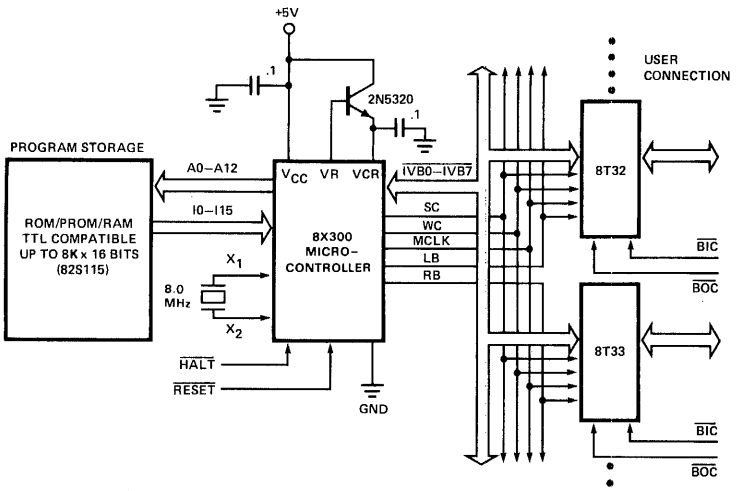


Figure 2

INSTRUCTION AND IV BUS DATA INPUT	DATA PROCESSING	ADDRESS AND IV BUS CHANGING	ADDRESS AND IV BUS DATA VALID MCLK=HIGH
← ¼ cycle →	← ¼ cycle →	← ¼ cycle →	← ¼ cycle →

Table 2 INSTRUCTION CYCLE

Data Addressing

Sources and destinations of data are specified using a 5-bit octal number. The source and/or destination of data to be operated upon is specified in a single instruction word.

Referring to Figure 1, the Auxiliary register (address 00) is the implied source of the second argument for ADD, AND or XOR operations.

IVL and IVR are write-only registers used only as a destination. They have addresses and are treated as registers, but in reality they do not exist. When IVL is specified as a destination or the D field = $20\text{-}27_8$, then LB = 'low', RB = 'high' are generated; when IVR is specified as a destination or the D field = $30\text{-}37_8$, then RB = low, LB = 'high' are generated.

When IVL or IVR is specified as the destination in an instruction, SC is also activated and data is placed on the IV bus. If IVL or IVR is specified as a source of data, the source data is all zeroes.

INSTRUCTION SEQUENCE CONTROL

The Address Register and Program Counter are used to generate addresses for accessing an instruction. The Address Register is used to form the instruction address, and in all but 3 instructions (XEC, NZT, and JMP) the address is copied into the Program Counter. The instruction address is formed in 1 of 3 ways:

1. For all instructions but the JMP, XEC, and a satisfied NZT, the Program Counter is incremented by 1 and placed in the Address Register.
2. For the JMP instruction, the full 13-bit address field from the JMP instruction is placed into the Address Register and copied into the Program Counter.
3. For the XEC and NZT instructions, the high order 5- or 8-bits of the Program Counter are combined with 8- or 5-lower-order bits of ALU output (XEC or NZT) and placed in the Address Register. For the NZT instruction, it is also copied into the Program Counter.

INSTRUCTION SET

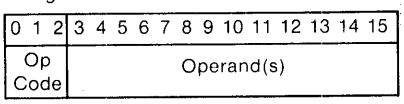
The 8X300 Microcontroller has a repertoire of 8 instruction classes which allow the user to test input status lines, set or reset output control lines, and perform high speed input/output data transfers. All instructions are 16 bits in length and each is fetched, decoded and executed in 250ns.

Data is respresented as an 8-bit byte; bit positions are numbered from left to right, with the least significant bit in position 7.

Within the 8X300, all operations are performed on 8-bit bytes. Arithmetic operations use 8-bit, unsigned 2's complement arithmetic.

INSTRUCTION FORMATS

The general 8X300 instruction format is:



All instructions are specified by a 3-bit Operation (Op Code) field. The operand may consist of the following fields: Source (S) field, Destination (D) field, Rotate/Length (R/L) field, Immediate (I) field, or (Program Storage) Address (A) field.

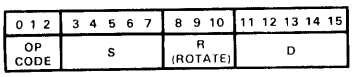
The instructions are divided into 5 format types, based on the Op Code and the Operand(s), as shown in Figure 3.

OPERATION	FORMAT	RESULT	NOTES
MOVE	I,II	Content of data field specified by {S, R/L} replaces data in field specified by {D, R/L.}	If S and D both are registers, then R/L specifies a right rotate of the register specified by S.
ADD	I,II	Sum of AUX and data specified by {S, R/L} replaces data in field specified by {D, R/L}.	
AND	I,II	Logical AND of AUX and data specified by {S, R/L} replaces data in field specified by {D, R/L.}	
XOR	I,II	Logical exclusive OR of AUX and data specified by {S, R/L} replaces data in field specified by {D, R/L.}	
XMIT	III,IV	The literal value I replaces the data in the field specified by {S,L.}	If S is an I/O address then I is limited to range 00-37. Otherwise I is limited to range 000-377.
NZT	III,IV	If the data in the field specified by {S, L} equals zero, perform the next instruction in sequence. If the data specified by {S,L} is not equal to zero, execute the instruction at address determined by using the literal I as an offset to the Program Counter.	If S is an I/O address then I is limited to range 00-37. Otherwise I is limited to range 000-377.
XEC	III,IV	Perform the instruction at address determined by applying the sum of the literal I and the data specified by {S, L} as an offset to the Program Counter. If that instruction does not transfer control, the program sequence will continue from the XEC instruction location.	The offset operation is performed by reducing the value of PC to the nearest multiple of 32 (if I = 00-37) or 256 (if I = 000-377) and adding the offset.
JMP	V	The address value A replaces contents of the Program Counter.	A limited to the range $0\text{-}17777_8$.

Table 3 8X300 INSTRUCTION SUMMARY

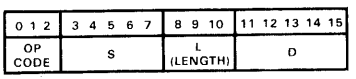
INSTRUCTION FORMATS

OPERATIONS
(REGISTER TO REGISTER)
MOVE AND
ADD XOR



Type I

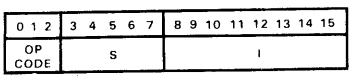
OPERATIONS
(REGISTER TO I/O, I/O TO REGISTER, I/O TO I/O)
MOVE ADD
AND XOR



Type II

OPERATIONS

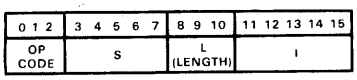
XEC XMIT* NZT



Type III

OPERATIONS

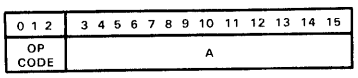
XEC XMIT* NZT



Type IV

OPERATIONS

JMP



Type V

*NOTE
If XMIT, S actually represents the destination.

Figure 3

INSTRUCTION FIELDS

Op Code Field (3-Bit Field)

The Op Code field is used to specify 1 or 8 8X300 instructions as shown in Table 4.

OP CODE OCTAL VALUE	INSTRUCTION	
0	MOVE	S,R/L,D
1	ADD	S,R/L,D
2	AND	S,R/L,D
3	XOR	S,R/L,D
4	XEC	I,R/L,S or I,S
5	NZT	I,R/L,S or I,S
6	XMIT	I,R/L,D or I,D
7	JMP	A

Table 4 OP CODE FIELD OCTAL ASSIGNMENTS

S,D Fields (5-Bit Fields)

The S and D fields specify the source and destination of data for the operation defined by the Op Code field. The Auxiliary Register is an implied second source for the instructions ADD, AND and XOR, each of which require two source fields. That is, instructions of the form,

ADD X, Y

imply a third operand, say Z, located in the Auxiliary Register so that the operation which takes place is actually X + Z, with the result stored in Y.

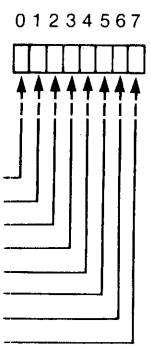
The S and/or D fields may specify a register, or a 1 to 8-bit I/O field. S and D field value assignments in octal are shown in Table 5.

0_8-17_8 is used to specify 1 of 7 working registers (R1-R6, R11), the Auxiliary Register, the Overflow Register, or IVL and IVR write-only registers.

OCTAL VALUE		OCTAL VALUE	
00	AUX-Auxiliary Register	10	OVF-Overflow register-Used only as a source
01	R1	11	R11
02	R2	12	Unassigned
03	R3	13	Unassigned
04	R4	14	Unassigned
05	R5	15	Unassigned
06	R6	16	Unassigned
07	IVL Register-Left Bank I/O address register. Used only as a destination.	17	IVR Register-Right Bank I/O address register. Used only as a destination.

a. Register Specification

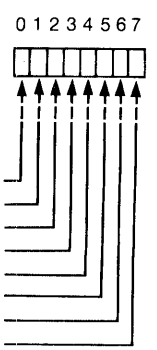
20_8-27_8 is used to specify the least significant bit of a variable length field within the I/O Port previously selected by the IVL register. The length of the field is determined by R/L.



OCTAL VALUE	
20	Field within previously selected Port; position of LSB = 0
21	Field within previously selected Port; position of LSB = 1
22	Field within previously selected Port; position of LSB = 2
23	Field within previously selected Port; position of LSB = 3
24	Field within previously selected Port; position of LSB = 4
25	Field within previously selected Port; position of LSB = 5
26	Field within previously selected Port; position of LSB = 6
27	Field within previously selected Port; position of LSB = 7

b. Left Bank I/O Field Specification

30_8-37_8 is used to specify the least significant bit of a variable length field within the I/O Port previously selected by the IVR Register. The length of the field is determined by R/L.



OCTAL VALUE	
30	Field within previously selected Port; position of LSB = 0
31	Field within previously selected Port; position of LSB = 1
32	Field within previously selected Port; position of LSB = 2
33	Field within previously selected Port; position of LSB = 3
34	Field within previously selected Port; position of LSB = 4
35	Field within previously selected Port; position of LSB = 5
36	Field within previously selected Port; position of LSB = 6
37	Field within previously selected Port; position of LSB = 7

c. Right Bank I/O Field Specification

Table 5 S AND D FIELD OCTAL ASSIGNMENTS

R/L Field (3-Bit Field)

The R/L field performs one of two functions, specifying either a field length (L) or a right rotation (R). The function it specifies for a given instruction depends upon the contents of the S and D fields:

A. When both S and D specify registers, the R/L field is used to specify a right rotation of the data specified by the S field. (Rotation occurs on the bus and not in the source register.) The register source data is right rotated within one instruction cycle time independent of the number of bit positions specified in the R/L field.
B. When either or both the S and D fields specify a variable length I/O data field, the R/L field is used to specify the length of that data field.
C. R/L field assignments are shown in Table 6.

R/L FIELD OCTAL VALUE	SPECIFICATION
0	Field Length = 8 Bits
1	Field Length = 1 Bit
2	Field Length = 2 Bits
3	Field Length = 3 Bits
4	Field Length = 4 Bits
5	Field Length = 5 Bits
6	Field Length = 6 Bits
7	Field Length = 7 Bits

Table 6 R/L FIELD OCTAL ASSIGNMENTS

I Field (5/8-Bit Field)

The I field is used to load a literal value (contained in the instruction) into a register, or a variable I/O data field, or to modify the low order bits of the Program Counter.

The length of the I field is based on the S field in XEC, NZT, and XMIT instructions, as follows:

A. When S specifies a register, the literal I is an 8-bit field (Type III format).
B. When S specifies variable I/O data field, the literal I is a 5-bit field (Type IV format).

A Field (13-Bit Field)

The A field is a 13-bit Program Storage address field. This allows the 8X300 to directly address 8192 instructions.

REGISTER OPERATIONS

When a register is specified as the source and a variable I/O data field is specified as the destination, the low order bits of the results of the instructions MOVE, ADD, XOR are merged with the original destination data.

When an I/O data field of 1 to 8 bits is specified as the source, and a register as the destination, the 8-bit result of the operations MOVE, ADD, AND, XOR is stored in the register. The operations ADD, AND, XOR actually use the I/O data field (1 to 8 bits) with leading zeros to obtain 8-bit source data for use with the 8-bit AUX data during the operation.

IVL and IVR are write-only pseudo registers, and therefore can be specified as destination fields only. Operations involving IVL and IVR as sources are not possible. For example, it is not possible to increment IVR or IVL in a single instruction, and the contents of IVL or IVR cannot be transferred to a working register, or I/O Port.

The OVF (Overflow) Register can only be used as a source field; it is set or reset *only* by the ADD instruction.

ADDRESSING DATA ON THE INTERFACE VECTOR

I/O data fields are implemented via general purpose 8-bit I/O registers called Interface Vector (IV) Bytes. The IV registers serve to select IV bytes. In order for an instruction to access (read or write) an I/O data field, the address must be output to the IVL or IVR registers.

Thus, two instructions are required to operate on an Interface Vector byte.

```
XMIT    ADDRESS, IVL
MOVE    LB, RB
```

Each of the two IV registers (IVL and IVR) may be set to select an IV byte, therefore two I/O ports may be active at one time—one on the Right Bank (IVR) and one on the Left Bank (IVL). Data may be input and output in one instruction following the selection of IV bytes:

```
XMIT    ADDRESS1, IVL
XMIT    ADDRESS2, IVR
ADD     LB, RB
```

Once the IV byte is selected (addressed) it will remain selected until another address is output to the same IV register. Since an IV register (IVL, IVR) can be used only as a destination field of an instruction, any instruction sending data to IVL or IVR can be used to select an IV byte.

From the user's standpoint, however, all IV byte outputs can be read by an external device regardless of whether they are selected or not.

The address range of IVL and IVR is $0\text{-}255_{10}$.

INSTRUCTION DESCRIPTIONS

The following instruction descriptions employ MCCAP (the 8X300 Cross Assembly Program) programming notation. This notation varies somewhat from the instruction descriptions provided in Tables 3 through 5. Thus, for example, explicit L field definition, as shown in Table 3 and Table 4 is not required by MCCAP instructions; MCCAP can create appropriate variable field addresses from information contained in Data Declaration statements which may be provided by the programmed at the beginning of his program.

The 8X300 instruction set is described below with examples shown in Figures 4 through 11.

MOVE S,D or MOVE S(R),D

Format: Type I, Type II

Operation: (S)→(D)

Description

Move data. The contents of S are transferred to D; the contents of S are unaffected. If both S and D are registers, R/L specifies a right rotate of the source data before the move. Otherwise, R/L specifies the length of the source and/or destination I/O data field. If the MOVE is between Left Bank and Right Bank I/O field, an 8-bit field must always be moved.

Example

Store the least significant 3 bits of register 5 (R5) in bits 4, 5 and 6 of the I/O Port previously addressed by the IVL register. See Figure 4.

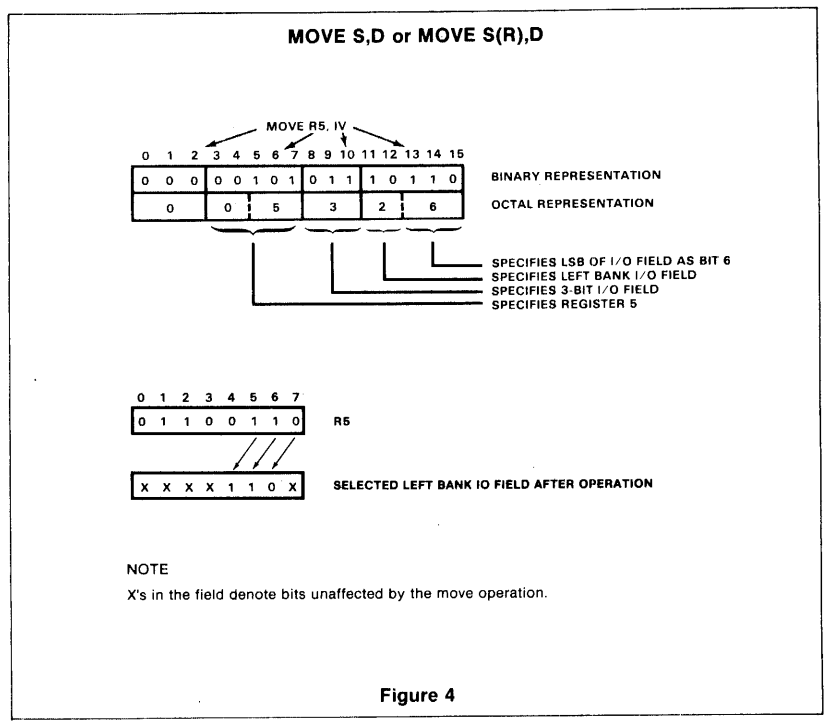


Figure 4

ADD S,D or ADD S(R),D

Format: Type I, Type II

Operation: (S) + (AUX)→D
Carry→OVF

Description

Unsigned 2's complement 8-bit addition. The contents of S are added to the contents of the Auxiliary Register. The result is stored in D; OVF is set to the value of the carry. If both S and D are registers, R/L specifies a right rotate of the source (S) data before the operation. Otherwise, R/L specifies the length of the source and/or destination I/O data fields. S and AUX are unaffected unless specified as the destination.

Example

Add the contents of R1 rotated 4 places to AUX and store the result in R3. See Figure 5.

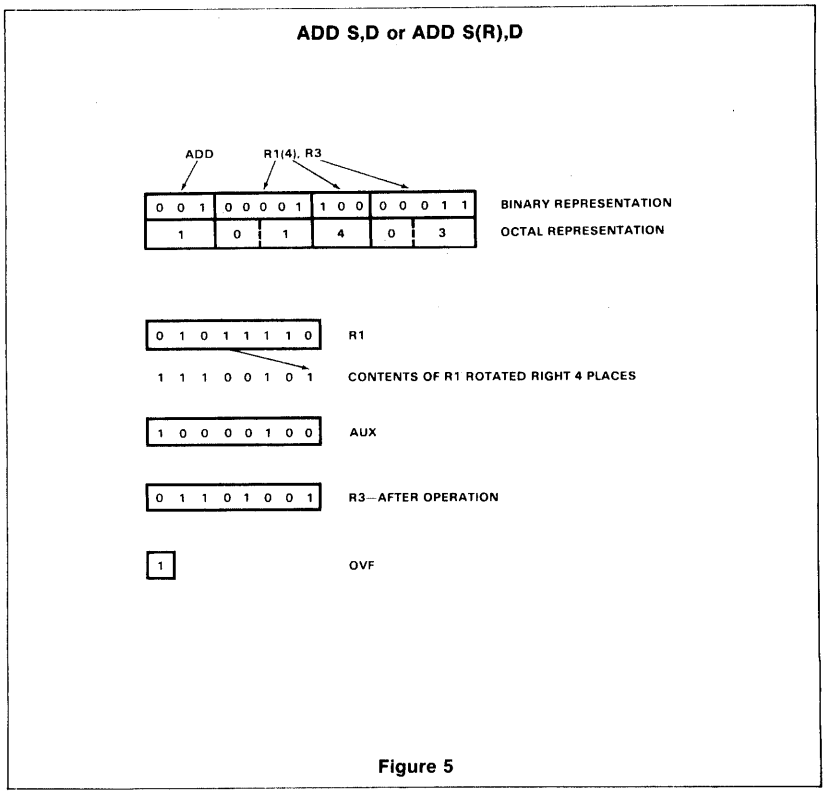


Figure 5

AND S,D or AND S(R),D

Format: Type I, Type II

Operation: (S) ∧ (AUX)➔D

Description

Logical AND. The AND of the source field and the Auxiliary Register is stored into the destination. If both S and D are registers, R/L specifies a right rotate of the source (S) data before the AND operation. Otherwise R/L specifies the length of the source and/or destination I/O data fields. S and AUX are unaffected unless specified as a destination.

Example

Store the AND of the selected right bank I/O field and AUX in R4. The right bank data field is called WSBCD and is 4 bits long and located in bits 2, 3, 4 and 5. See Figure 6.

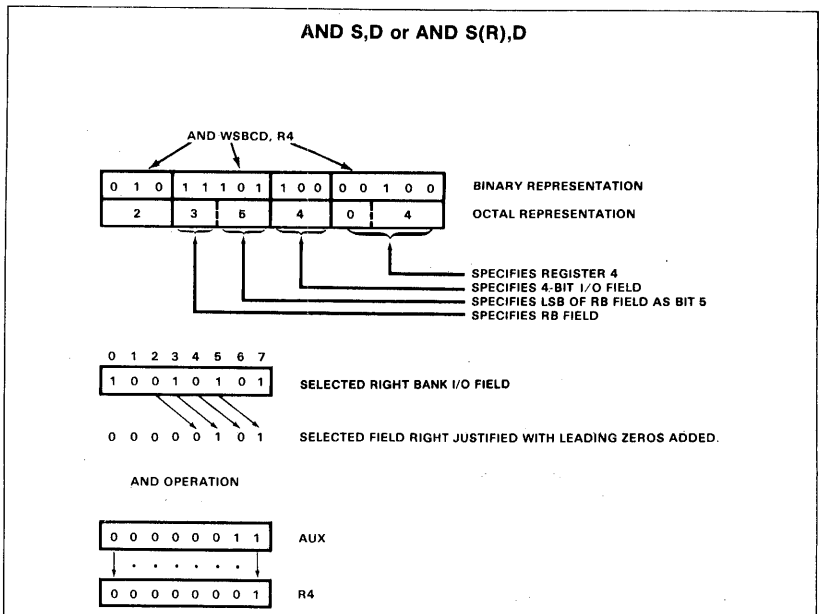


Figure 6

XOR S,D or XOR S(R),D

Format: Type I, Type II

Operation: (S) ⊕ (AUX)➔D

Description

Exclusive-OR. The Exclusive-OR of the source field and the Auxiliary Register is stored in the destination. If both S and D are registers, R/L specifies a right rotate of the source (S) data before the XOR operation. Otherwise R/L specifies the length of the source and/or destination I/O data fields. S and AUX are unaffected unless specified as a destination.

Example

Replace the selected I/O data field with the XOR of the field and AUX. The I/O data field is called STATUS and is 5 bits in length and located in bits 3, 4, 5, 6 and 7 of left bank. See Figure 7.

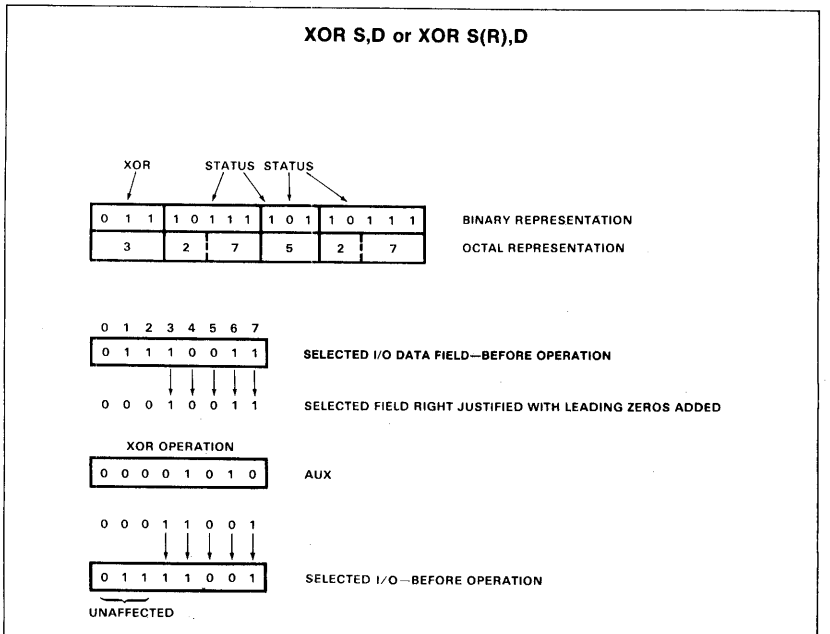


Figure 7

XEC I(S)

Format: Type III, Type IV

Operation

Execute instruction at the address specified by the Address Register with lower 5 or 8 bits replaced by (S) + I.

Description

Execute the instruction at the address determined by replacing the low order bits of the Address Register (AR) with the low order bits of the sum of the literal I and the contents of the source field. If S is a register, the low order 8 bits of AR are replaced; if S is an I/O data field, the low order 5 bits of AR are replaced, resulting in an execute range of 256 and 32 respectively. The Program Counter is not affected unless the instruction executed is a JMP or NZT (whose branch is taken).

Example

Execute one of n JMPs in a table of JMP instructions determined by the value of the selected I/O data field on the left bank. The table follows immediately after the XEC instruction and the I/O field is called INTERPT and is a 3-bit field located in bits 4, 5 and 6. See Figure 8.

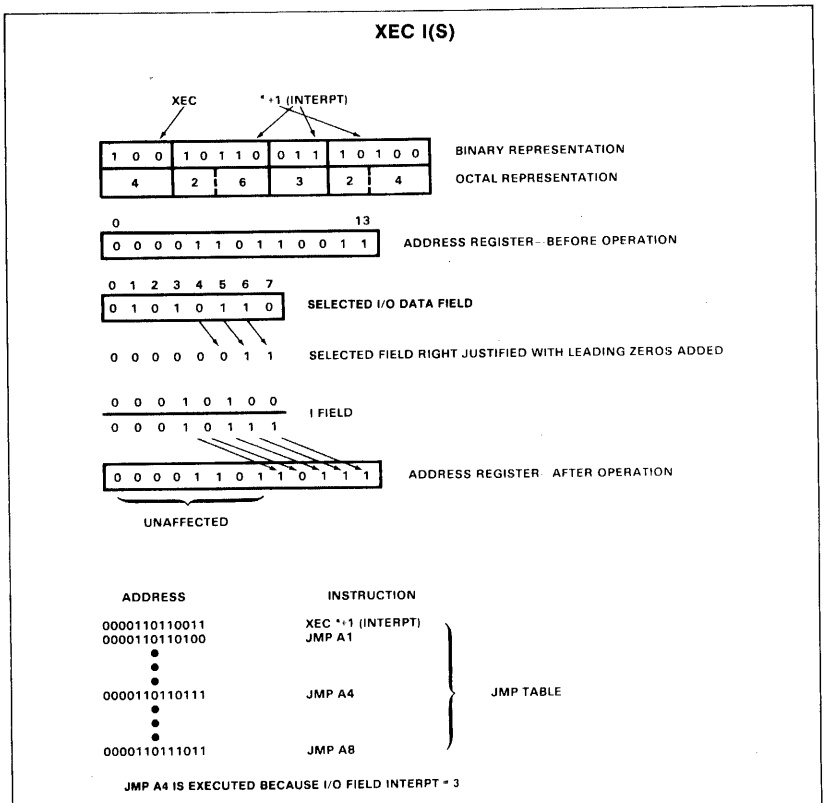


Figure 8

XMIT I,D

Format: Type III, Type IV

Operation: I→(D)

Description

Transmit literal. The literal field I is stored in D. If D is a register, an 8-bit field is transferred; if D is an I/O data field, up to a 5-bit field is transferred.

Example

Store the bit pattern 110 in the selected I/O data field on the right bank. The field name is VALUE and is located in bits 3, 4 and 5. See Figure 9.

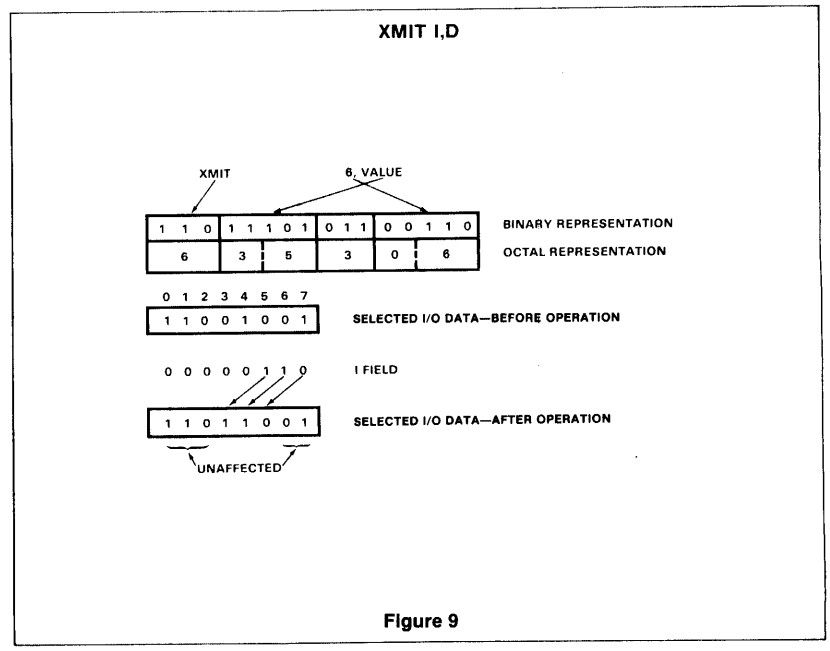


Figure 9

NZT S,I

Format: Type III, Type IV

Operation:

Non-Zero Transfer. If (S) ≠ 0, PC offset by I → PC; otherwise PC + 1 → PC.

Description

If the data specified by the S field is non-zero, replace the low order bits of the Program Counter with I. Otherwise, processing continues with the next instruction in sequence. If S is a register, the low order 8 bits of the PC are replaced; if S is an I/O data field, the low order 5 bits of the PC are replaced, resulting in an NZT range of 256 and 32 respectively.

Example

Jump to Program Address ALPHA if the selected right bank I/O field is non-zero. The field name is OVERFLO and it is a 1-bit field located in bit 3. See Figure 10.

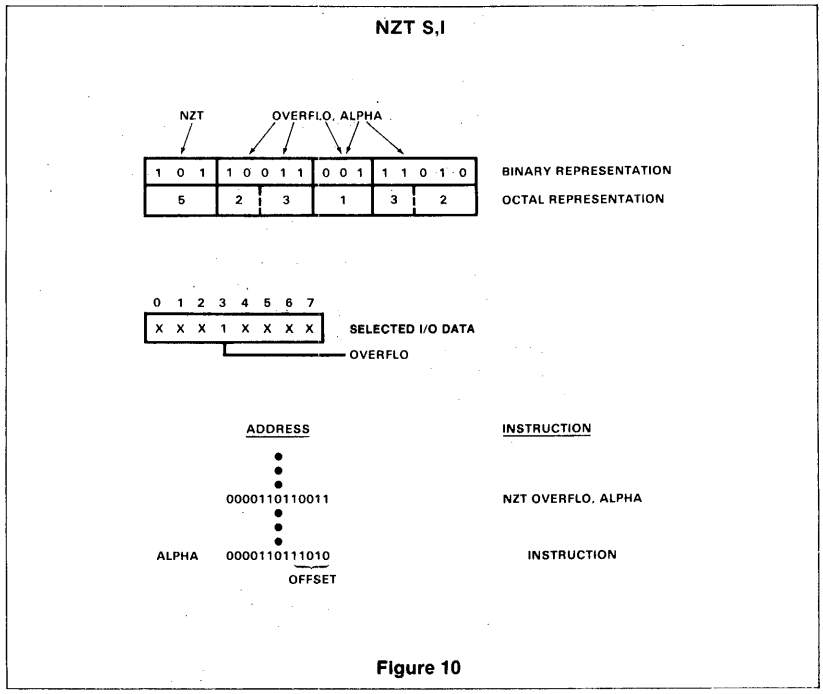


Figure 10

JMP A

Format: Type V

Operation: A → PC

Description

The literal value A is placed in the Program Counter and Address Register, and processing continues at location A. A has a range of 0-17777_8 (0-8191).

Example

Jump to location ALPHA (0000101110001). See Figure 11.

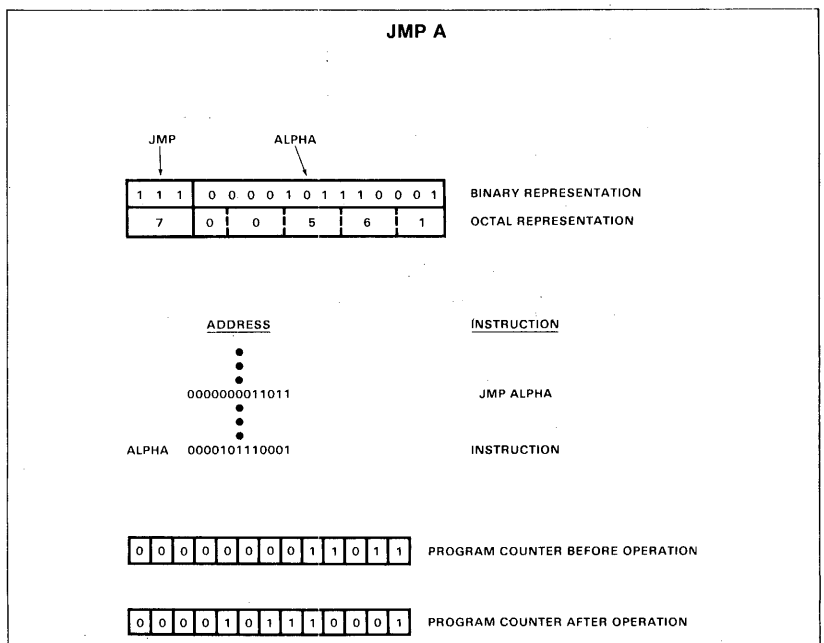


Figure 11

SYSTEM DESIGN USING THE 8X300 MICROCONTROLLER

Designing hardware around the 8X300 Interpreter reduces to selecting a program storage devicer (ROM, PROM, etc.), selecting I/O devices (IV byte, multiplexers, RAM, etc.), selecting clock mode (system driven or crystal controlled) and interfacing the Microcontroller to these components.

A specific example of a control system using the 8X300 Microcontroller is shown in Figure 12. Only 8 components—four 8T32 I/O Ports, one 82S208 RAM, two 82S215 ROMs, and an 8X300 are required to build this system which contains 512 words of program storage, 32 TTL I/O connection points, 256 bytes of working storage, and operates at a 250ns instruction cycle time.

Halt, Reset Signals

$\overline{\text{HALT}}$:
A low level at the $\overline{\text{HALT}}$ input stops internal operation of the Microcontroller at the start of the next instruction after $\overline{\text{HALT}}$ is applied (quarter cycle after MCLK). Since $\overline{\text{HALT}}$ is sampled at the start of each instruction cycle it is possible to prevent a cycle by applying $\overline{\text{HALT}}$ early in that cycle. $\overline{\text{HALT}}$ does not inhibit MCLK or affect any internal registers. Normal operation begins with the next complete cycle after the $\overline{\text{HALT}}$ input goes high.

$\overline{\text{RESET}}$:
A low level at the $\overline{\text{RESET}}$ input sets the program counter and address register to zero. While $\overline{\text{RESET}}$ is low MCLK is inhibited. If $\overline{\text{RESET}}$ is applied during the last 2 quarter cycles, the MCLK during that cycle may be shortened. $\overline{\text{RESET}}$ should be applied for 1 full instruction cycle time to assure proper operation. When $\overline{\text{RESET}}$ input goes high an MCLK occurs prior to the resumption of normal processing. $\overline{\text{RESET}}$ does not affect the other internal registers.

SYSTEM TIMING

In systems with fast instruction cycle times, most Microcontroller delays are strictly determined by internal gate propagation delays.

EXAMPLE OF CONTROL SYSTEM

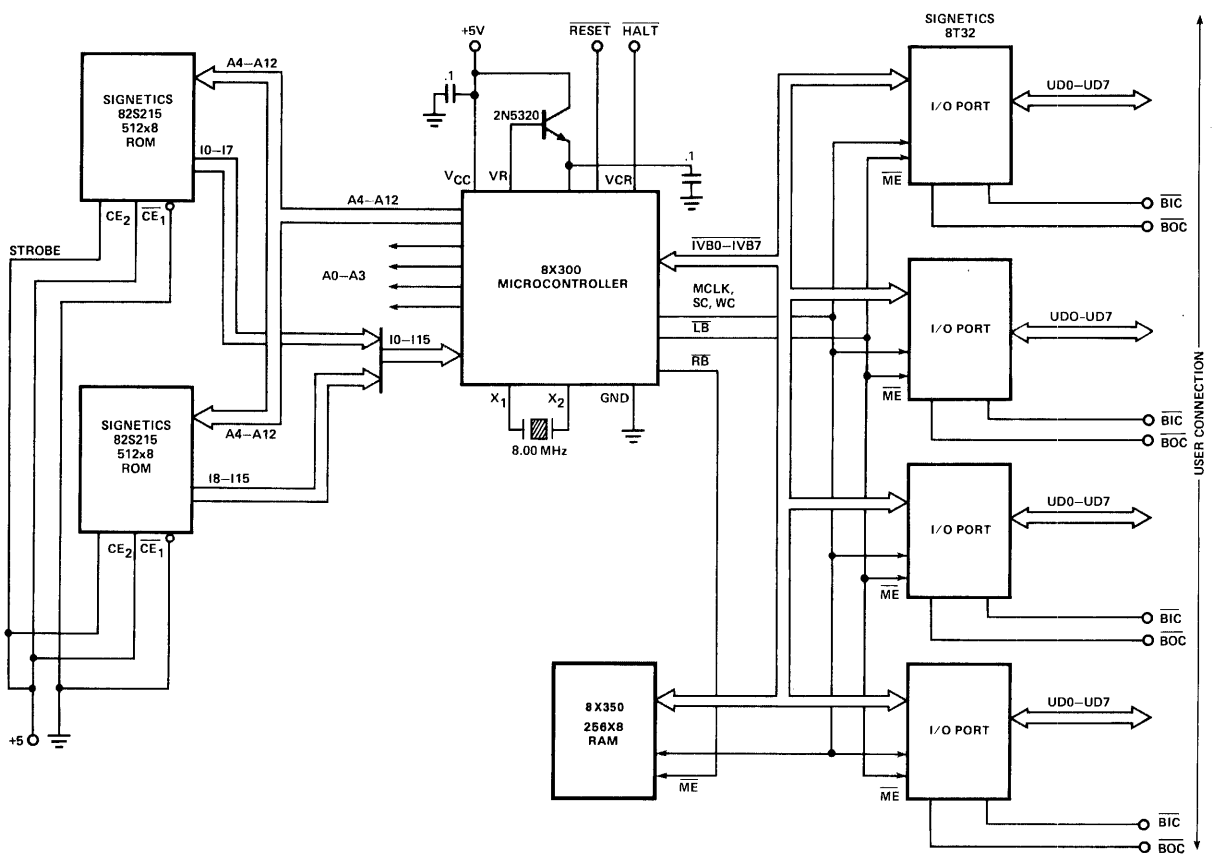


Figure 12

Since some events are constrained to occur in certain quarter cycles, as system cycle times become slower, the delays will appear to increase due to gating with internal clocks. In the table of AC Electrical Characteristics, 2 columns are used: 1 to denote times which occur due to internal clock intervention and 1 to denote minimum delays for fast cycle times.

When using Signetics 8T32 I/O Ports, selection of instruction cycle time involves calculating the maximum program storage access time. Assuming the instruction is available when MCLK falls, the I/O control lines are stable 35ns later. Signetics 8T32's require another 35ns to disable a previously selected port and enable the desired port (assumes a change in bank signals). A 10ns margin has been added to the 8T32 enable for this evaluation to reflect the fact that most systems will have more capacitive loading than the 50pF test condition in the 8T32 specification and to allow for line delays.

The system instruction cycle time for normal systems such as shown in Figure 12 is determined by Microcontroller propagation delays, program storage access time, and port output enable times. Instruction cycle time is normally constrained by one or more of the following conditions:

1. Instruction to LB/RB (input phase) and I/O Port output enable:
   $T_{OE} \leq \frac{1}{2}$ cycle - 55ns (Figure 13).
2. Program storage access time and instruction to LB/RB (input phase) and I/O Port output enable and IV data (input phase) to address $\leq$ instruction cycle time (Figure 14).
3. Program storage access time and instruction to address $\leq$ instruction cycle time (Figure 15).

The first constraint can be used to determine the minimum cycle time. Using the inequality 35ns + 35ns $\leq$ ½ cycle - 55ns implies ½ cycle $\geq$ 125ns or an instruction time of 250ns.

Program storage access time for a 250ns instruction cycle can be calculated from the second constraint. Noting that the specification for IV data (input phase) to address is 115ns: Program storage access time + 35ns + 35ns + 115ns $\leq$ 250ns implies program storage access time $\leq$ 65ns.

The third constraint can be used to verify the maximum program storage access time. Noting that the specification for instruction to address is 185ns: Program storage access time + 185ns $\leq$ 250ns confirms that program storage access time 65ns is satisfactory.

SYSTEM INSTRUCTION CYCLE TIME

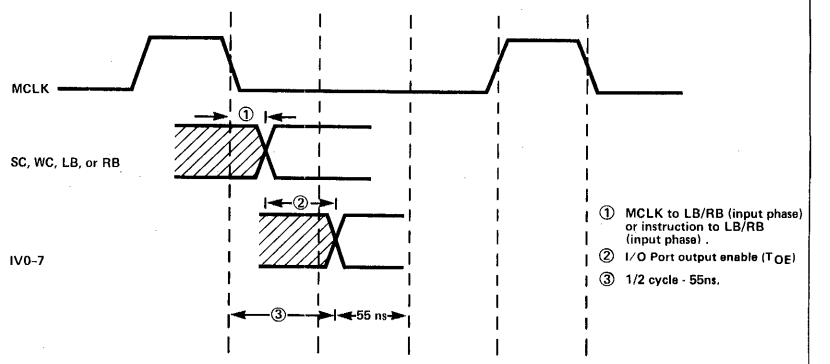


Figure 13

SYSTEM INSTRUCTION CYCLE TIME

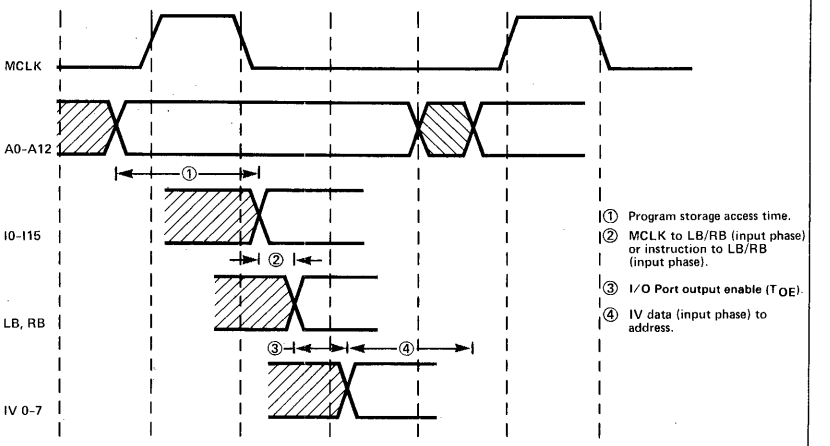


Figure 14

SYSTEM INSTRUCTION CYCLE TIME

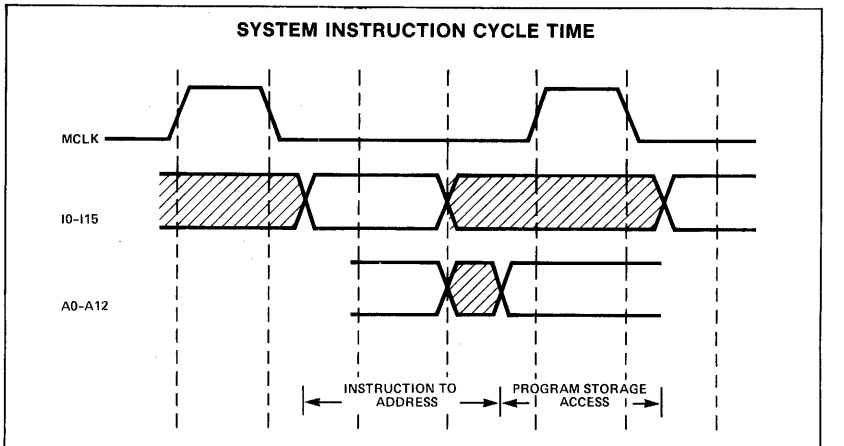


Figure 15

System Clock

The Micrcontroller has an integrated oscillator which generates all necessary clock signals. The oscillator is designed to connect directly to a series resonant quartz crystal via pins X1 and X2. The crystal resonant frequency, f, is related to the desired cycle time, T, by the relationship f = 2/T. For a 250ns system, f = 8.00MHz.

Type:	Fundamental mode, series resonant
Impedance at Fundamental:	35 ohms maximum
Impedance at harmonics and spurs:	50 ohms minimum

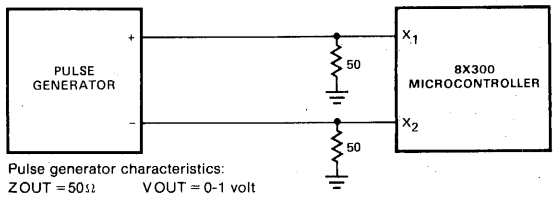
Table 7 CRYSTAL CHARACTERISTICS

In lower speed applications where the cycle time need not be precisely controlled, a capacitor may be connected between X1 and X2 to drive the oscillator. Approximate capacitor values are given in Table 8. If cycle time is to be varied, X1 and X2 should be driven from complementary outputs of a pulse generator. Figure 16 shows a typical configuration. For systems where the Interpreter is to be driven from a master clock the X1 and X2 lines may be interfaced to TTL logic as shown in Figure 17.

Cx,pF	CYCLE TIME
100	300ns
200	500ns
500	1.1μs
1000	2.0μs

Table 8 CLOCK CAPACITOR VALVES

CLOCKING WITH A PULSE GENERATOR

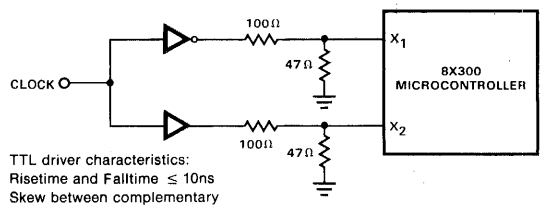


Pulse generator characteristics:
ZOUT = 50Ω VOUT = 0-1 volt
Risetime ≤ 10ns ≤ Skew ≤ 10ns
Complementary outputs

NOTE: All resistors values are typical and in ohms.

Figure 16

CLOCKING WITH TTL



TTL driver characteristics:
Risetime and Falltime ≤ 10ns
Skew between complementary outputs ≤ 10ns

Figure 17

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5% and 0°C ≤ T_A < 70°C

DELAY DESCRIPTION	PROPAGATION DELAY TIME	CYCLE TIME LIMIT
X1 falling edge to MCLK (driven from external pulse generator)	75ns	
MCLK to SC/WC falling edge (input phase)	25ns	
MCLK to SC/WC rising edge (output phase)		½ cycle + 25ns
MCLK to LB/RB (input phase)	35ns	
Instruction to LB/RB output (input phase)	35ns	
MCLK to LB/RB (output phase)		¼ cycle + 35ns
MCLK to IV data (output phase)	185ns	½ cycle + 60ns
IV data (input phase) to IV data (output phase)	115ns	
Instruction to Address	185ns	½ cycle + 40ns
MCLK to Address	185ns	½ cycle + 40ns
IV data (input phase) to Address	115ns	
MCLK to IV data (input phase)		½ cycle - 55ns
MCLK to Halt falling edge to prevent current cycle		¼ cycle - 40ns
Reset rising edge to first MCLK		0 to 1 cycle

NOTE
1. Reference to MCLK is to the falling edge when loaded with 300pF.
2. Loading on Address lines is 150pF.

TYPICAL INSTRUCTION CYCLE TIMING

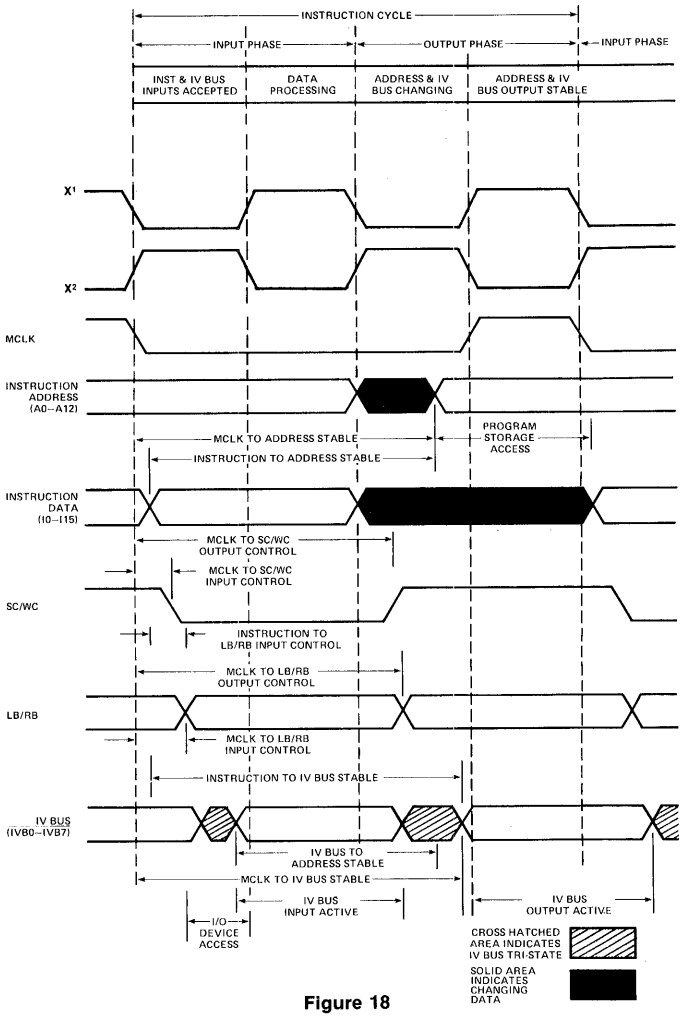


Figure 18

DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	High level input voltage					
	X1,X2		.6			V
	All others		2			V
V_{IL}	Low level input voltage					
	X1,X2				.4	V
	All others				.8	V
V_{IC}	Input clamp voltage (Note 1)	V_{CC} = 4.75V, I_I = -10mA			-1.5	V
I_{IH}	High level input current					
	X1,X2	V_{CC} = 5.25V, V_{IH} = .6V		2700		μA
	All others	V_{CC} = 5.25V, V_{IH} = 4.5V		<1	50	μA
I_{IL}	Low level input current					
	X1,X2	V_{CC} = 5.25V, V_{IL} = .4V		-2500		μA
	$\overline{IVBO}$-7			-140	-200	μA
	IO-I15	V_{CC} = 5.25V, V_{IL} = .4V		-880	-1600	μA
	$\overline{HALT}$, $\overline{RESET}$	V_{CC} = 5.25V, V_{IL} = .4V		-230	-400	μA
V_{OL}	Low level output voltage	V_{CC} = 5.25V, V_{IL} = .4V				
	A0-A12	V_{CC} = 4.75V, I_{OL} = 4.25mA		.35	.55	V
	All others	V_{CC} = 4.75V, I_{OL} = 16mA		.35	.55	V
V_{OH}	High level output voltage	V_{CC} = 4.75V, I_{OH} = 3mA	2.4			V
I_{OS}	Short circuit output current (Note 2)	V_{CC} = 5.25V	-30		-140	mA
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{CC}	Supply current	V_{CC} = 5.25V			1.60	mA
I_{REG}	Regulator control	V_{CC} = 5.0V	-14		-21	mA
I_{CR}	Regulator current (Note 3)				290	mA
V_{CR}	Regulator voltage (Note 3)		2.2		3.2	V

NOTES
1. Crystal inputs X1 and X2 do not have clamp diodes.
2. Only one output may be grounded at a time.
3. (Limits apply for V_{CC} = 5V ± 5% and 0°C < T_A < 70°C unless specified otherwise.)

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	7	V
	Logic input voltage	5.5	V
	Crystal input voltage	2	V

INTRODUCTION

Recent trends in system design are focusing on significantly lower costs and greater reliability while simultaneously maintaining or improving system preformance. Consequently, second generation as well as new system designs demand alternatives to conventional logic realizations which substantially reduce the system manufacturing costs. Signetics' LSI Logic Family provides this alternative by employing state-of-the-art technology to produce Large-Scale-Integrated, system oriented building blocks. By replacing a relatively large number of conventional logic circuits with a few LSI Logic components, system costs are reduced in proportion to system printed circuit board area, total number of circuits and power requirements. Moreover, system reliability is increased in direct proportion to the decrease in the number of integrated circuits within the system.

SYSTEM LOGIC FAMILY

Signetics' LSI Logic offers the designer a dual technology logic family to achieve cost objectives. First, where speed is a primary objective, low power Schottky TTL technology is employed to yield devices which feature high speed, low power, and medium density. Therefore, significant reduction in the number of high speed logic components is possible without any sacrifice in performance. The distinct advantages of low power Schottky TTL give it one of the best technologies for high performance LSI design. The particular features of LS are:

- Comparable propagation delay to standard TTL 7-10ns/gate average
- Low power dissipation—2mW per gate typical at 50% duty cycle
- Low speed power product—19pj typical
- 45MHz typical maximum J-K flip-flop clock frequency
- High fan-out capability—22 unit load—LS input current requirement is 1/4 that of standard TTL (0.36mA/input). Outputs are capable of sinking 8mA.
- High logic density—70 gates/mm^2 of silicon
- Higher system reliability due to reduced power density.

Secondly, while lower power Schottky offers increased density at high speeds, substantial component reduction is achieved with devices employing Integrated Injection Logic (I^{2}L). The very high density and low power of I^{2}L makes it extremely attractive for use in realizing relatively large system building blocks. System level functions may each be accomplished at 10MHz speeds by a single I^{2}L integrated circuit. I^{2}L features are:

- Speed—comparable to TTL (10-20ns propagation delay)
- Power—1-2 orders lower than any technology power down mode
- Density—40% smaller than PMOS—comparable to NMOS
- Interface—capability of mixing TTL, ECL circuits on the same chip.

The LSI Logic series of products are specially designed to aid system logic designers in the design of high performance, cost effective systems with a minimal number of parts. This is achieved through a line of standard products which are designed with the following objectives:

- Large Scale Building Blocks—devices are partitioned by function with high-level complexity and sophistication. These one chip building blocks are equivalent to 400 to 1500 elementary logic gates.
- Highest Performance Possible—devices in each category are optimized in performance according to their requirements. Devices requiring highest speed are designed using low power Schottky TTL and devices requiring medium speed are designed using I^{2}L to minimize device power dissipation and maximize logic density.
- Off-the shelf items—system logic devices are designed to allow general purpose usage. Devices in this series can be used as stand-alone items to enhance performance on a certain system design or to utilize several components within the family to design a minimal cost system with minimum number of components, such as in microprocessor based systems.

SIGNETICS CAPABILITIES

Signetics is a leader in the development of bipolar LSI logic circuits using both LS and I^{2}L technologies. Our capabilities are demonstrated by an 8-bit Fixed Instruction Microprocessor that Signetics is presently manufacturing with low power Schottky technology.

This circuit, the 8X300 Microcontroller, contains the equivalent of 700 logic gates on a 250X250 mil chip. This capability is being used to develop the LSI Logic Family and produce the substantial cost reduction offered by LSI without paying a penalty in performance.

Signetics is a leader in I^{2}L technology. Signetics has been researching I^{2}L as a standard product technology for over three years. Presently, Signetics possesses one of the fastest I^{2}L processes in the industry. Recognizing the vast potential of I^{2}L technology, Signetics is heavily committed to develop this high-speed line of LSI products using this technology. Signetics' I^{2}L process is basically the same process as its low power Schottky process that utilizes a thin expitaxial layer for speed improvement. Since this process is a highly reliable standard process in Signetics, the confidence level of producing such LSI circuits is extremely high. In addition to its own development activities, Signetics has access to N.V. Philips' vast development resources for continued development and enhancement of its present capabilities. This massive investment will result in continued improvement in speed/power performance of I^{2}L products.

Table 1 shows expected trends in I^{2}L speed/power curves during the next five years. Clearly I^{2}L will play a major role in the innovation of faster and possibly more complex LSI Logic functions in the support of a continued exploitation of LSI circuitry in systems design.

ADVANTAGES

The advantages of using LSI in system design are multifold. First, note that the cost of an LSI chip is no more than the sum cost of the circuits it replaces, consequently there is a direct saving in manufacturing costs as a result of a net reduction in the number of parts. Moreover an LSI system offers economic advantages over an SSI or MSI approach besides lowering direct manufacturing costs. Some important considerations are:

- Power supply costs are reduced because logic cells internal to the device require less drive capability and consequently consume less power.
- Field repair costs are reduced because reliability is higher with an LSI implementation. This higher reliability is achieved because IC failure rates are largely proportional to number of devices rather than device complexity.
- Another factor to be considered is that the development cost of printed circuit boards will decrease because of smaller number of ICs and that to some extent, this reduction offsets the cost of layout on the LSI devices.
- Applications requiring medium speed performance are often forced to use lower density, high speed semiconductor devices due to lack of availability of medium speed LSI devices. I^{2}L has changed this picture significantly. With the capability of controlling the amount of device injection current into an LSI circuit, the device can be controlled to operate at the desired speed and power for that particular application; thus, power consumption is minimized.

USING STANDARD LS PROCESS		
Average Propagation Delay	10-20ns at 200μA/Gate Injection Current	
Density (Dual Layer Metal)	Shift Register etc.	320 gates/mm^2
	Random Logic	150 gates/mm^2
	Single Inverter	1.5 mil^2
Chip Complexity	2000 gates at maximum speed (Random Logic) 4000 gates at maximum speed (Regular Arrays)	
Speed-Power	3pj @ maximum speed 0.35pj @ < 1MHz	

Table 1 SIGNETICS I^{2}L CAPABILITY

DESCRIPTION

The "182" is a high speed Look-Ahead Carry Generator ordinarily used with the "181" 4-Bit ALU or other arithmetic processing elements. This combination provides high speed Look-Ahead over word lengths of more than 4 bits.

The "182" accepts up to 4 pairs of active Low Carry Propagate and Carry Generate signals, an active High Carry input, and provides anticipated active High carries across 4 groups of binary adders.

Logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$

$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$

$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$

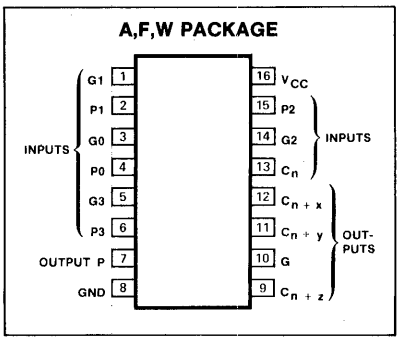
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$

$$\overline{P} = \overline{P_3P_2P_1P_0}$$

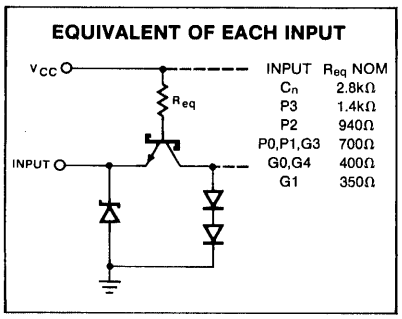
FEATURES

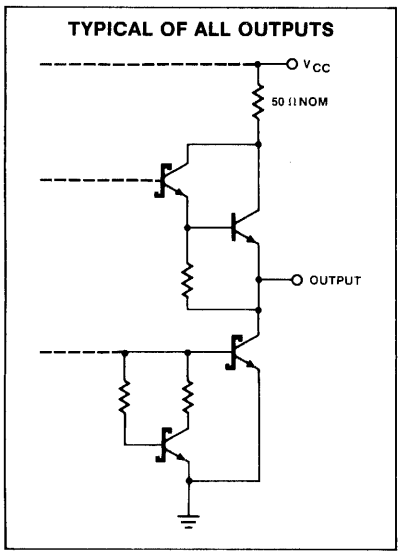
- **Provides look-ahead carries across a group of 4 ALU's**
- **Multi-level look-ahead for high speed arithmetic operation over long word lengths**

PIN CONFIGURATION



INPUT/OUTPUT SCHEMATICS





PIN DESIGNATION

PIN NOS.	DESIGNATION	FUNCTION
G0,G1,G2,G3	3,1,14,5	Active-Low Carry Generate Inputs
P0,P1,P2,P3	4,2,15,6	Active-Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12,11,9	Carry Outputs
G	10	Active-Low Carry Generate Output
P	7	Active-Low Carry Propagate Output
VCC	16	Supply Voltage
GND	8	Ground

DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	74S182			74S183			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Low voltage	V_{CC} = Min			0.8		0.8		V
V_{IH}	Input High voltage	V_{CC} = Min	2.0			2.0			V
V_{CD}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -12mA			-1.5			-1.2	V
V_{OL}	Output Low voltage	V_{CC} = Min, I_{OL} = 16mA			0.4			0.5	V
V_{OH}	Output High voltage	V_{CC} = Min, I_{OH} = -800μA	2.4			2.7			V
I_{IH}	Input High current	V_{CC} = Max, V_{IN} = 2.4V							
	C_n input				80			50	μA
	P_2 input				160			150	μA
	P_3 input				120			100	μA
	P_0, P_1, G_3 input				200			200	μA
	G_0, G_2 input				360			350	μA
	G_1 input				400			400	μA
I_{IL}	Input Low current	V_{CC} = Max, V_{IN} = 0.4V							
	C_n input				-3.2			-2.0	mA
	P_2 input				-6.4			-6.0	mA
	P_3 input				-4.8			-4.0	mA
	P_9, P_1, G_3 input				-8.0			-8.0	mA
	G_0, G_2 input				-14.4			-14	mA
	G_1 input				-16			-16	mA
I_{OS}	Output short circuit current	V_{CC} = Max	-40		-100	-40		-100	mA
I_{CC}	Power supply current	V_{CC} = Max, V_{IN} = 5V			72			109	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = +5V unless otherwise specified.

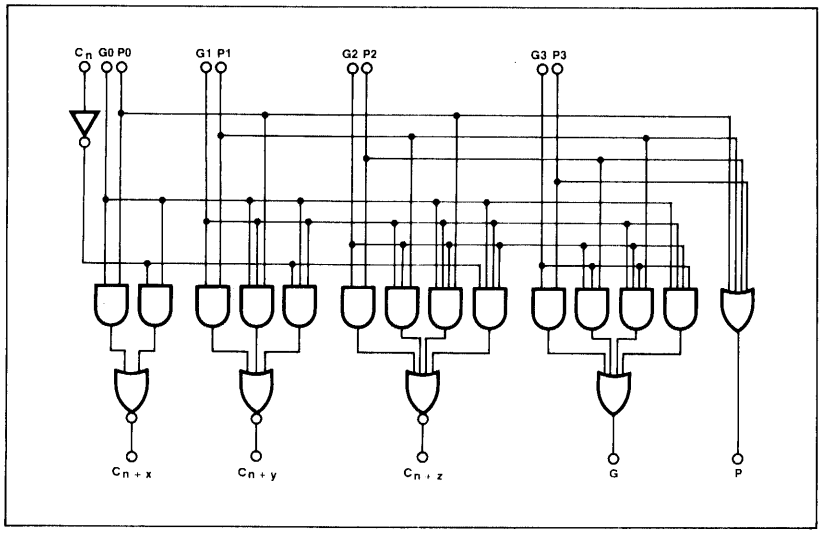
PARAMETER		TO	FROM	TEST CONDITIONS	54/74			54/74S			UNIT
					Min	Typ	Max	Min	Typ	Max	
	Propagation delay time										
t_{PLH}	Low to high					11	17				ns
t_{PHL}	High to low					15	22				
t_{PLH}	Low to high	G0, G1, G2	C_{n+x},						4.5	7	
		G3, P0, P1	C_{n+y}						4.5	7	
t_{PHL}	High to low	P2, P3	C_{n+z}	C_L = 15pF							
t_{PLH}	Low to high	G0, G1, G2,	G	R_L = 400Ω[1]					5	7.5	
		G3, P1, P2		R_L = 280Ω[2]					7	10.5	
t_{PHL}	High to low	P3									
t_{PLH}	Low to high	P0, P1, P2	P						4.5	6.5	
		P3									
t_{PHL}	High to low								6.5	10	
t_{PLH}	Low to high	C_n	C_{n+x},						6.5	10	
			C_{n+y}								
t_{PHL}	High to low		C_{n+z}						7	10.5	

NOTES

Load circuit and typical waveforms are shown at the front of section.

1. R_L = 400Ω for 54/74.
2. R_L = 280Ω for 54/74S.

LOGIC DIAGRAM



OCTAL D FLIP-FLOP — 54/74LS273

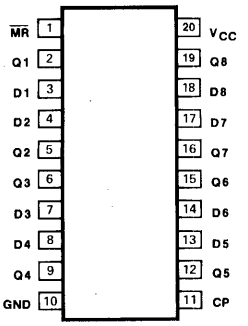
54LS273-N • 74LS273-N

DESCRIPTION

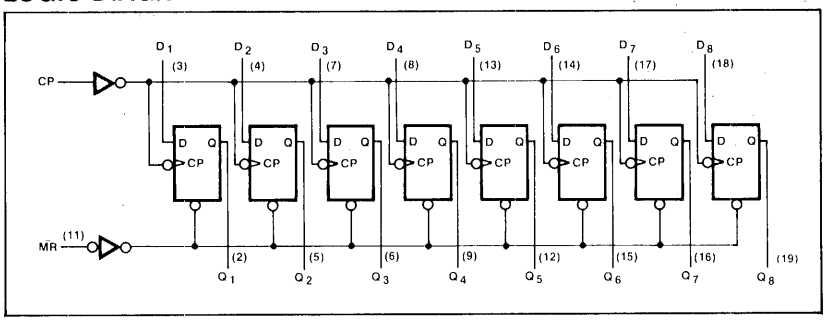
The 54/74LS273 is an Octal D Flip-Flop used primarily as an 8-bit positive edge-triggered storage register. D input information is transferred to storage during the Low to High transition of the clock pulse. The Master Reset ($\overline{MR}$) input simultaneously clears all flip-flops when low.

PIN CONFIGURATION

N PACKAGE



LOGIC DIAGRAM



OCTAL D FLIP-FLOP — 54/74LS377

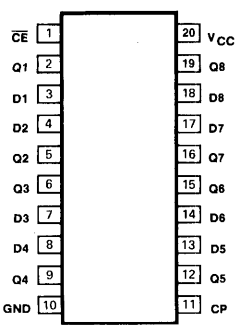
54LS273-N • 74LS273-N

DESCRIPTION

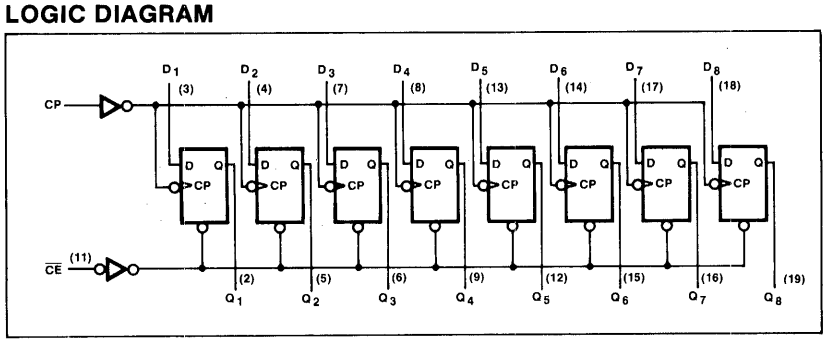
The 54/74LS377 is an Octal D Flip-Flop used primarily as an 8-bit positive edge-triggered storage register. D input information is transferred to storage during the Low to High transition of the clock pulse. The edge-triggered Clock Enable ($\overline{CE}$) input enables the clock when Low and holds data when High.

PIN CONFIGURATION

N PACKAGE



LOGIC DIAGRAM



DESCRIPTION

The 82S100 (tri-state outputs) and the 82S101 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-high (Fp), or true active-low (F). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are field programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

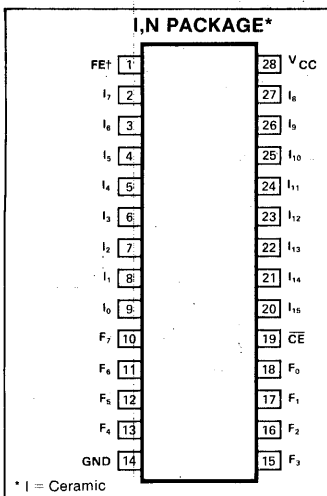
Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S100/101,I or N, and for the military temperature range (-55°C to +125°C) specify S82S100/101,I.

APPLICATIONS

- **CRT display systems**
- **Random logic**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Sequential controllers**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**

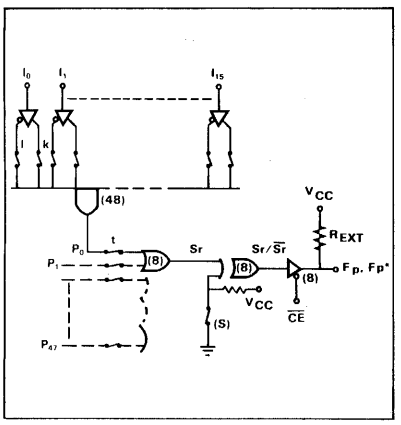
PIN CONFIGURATION

I,N PACKAGE*



* I = Ceramic
N = Plastic
†Open during normal operation

FPLA EQUIVALENT LOGIC PATH



LOGIC FUNCTION

Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions:
$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2)$ @ S = Closed
$F_0^* = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ S = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or $F\dot{p}$ (active low) is available, but not both. The required function polarity is programmed via link (S).

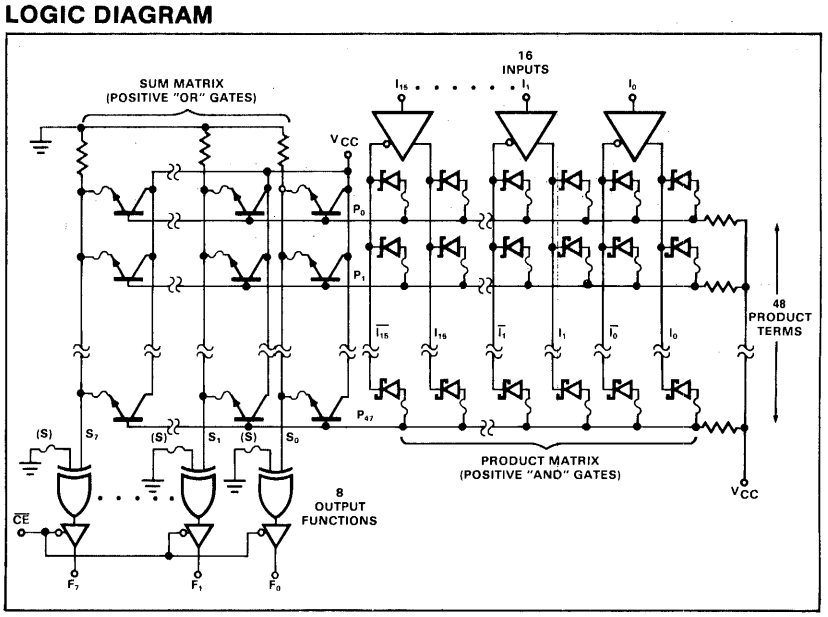
TRUTH RATINGS

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	F_p^*
Disabled (82S101)	X	1	X	1	1
Disabled (82S100)				Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

THERMAL TABLE

TEMPERATURE	MILI-TARY	COM-MER-CIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S100/101	0	+75	
	S82S100/101	-55	+125	
T_{STG}	Storage	-65	+150	

DC ELECTRICAL CHARACTERISTICS

N82S100/101: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S100/101 Min	N82S100/101 Typ	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ	S82S100/101 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-12	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S100)[3,6]	I_{OL} = 9.6mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OH} = -2mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S100)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S100)[4,8]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V		8			8		pF
C_{IN}	Input	V_{IN} = 2.0V		17			17		
C_{OUT}	Output	V_{OUT} = 2.0V							

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S100/101: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

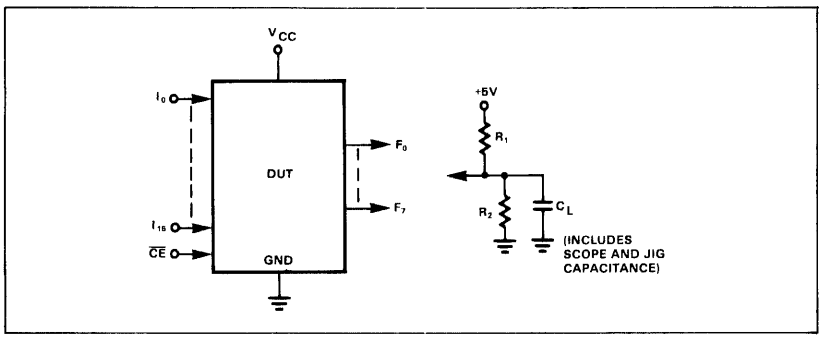
PARAMETER		TO	FROM	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Access time									ns
T_{IA}	Input	Output	Input		35	50		35	80	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	40	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	40	

NOTES on following page.

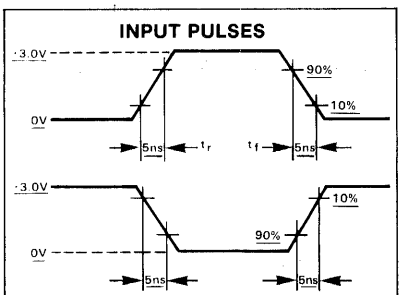
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied thru a resistor to V_{CC}.
7. Measured with: V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

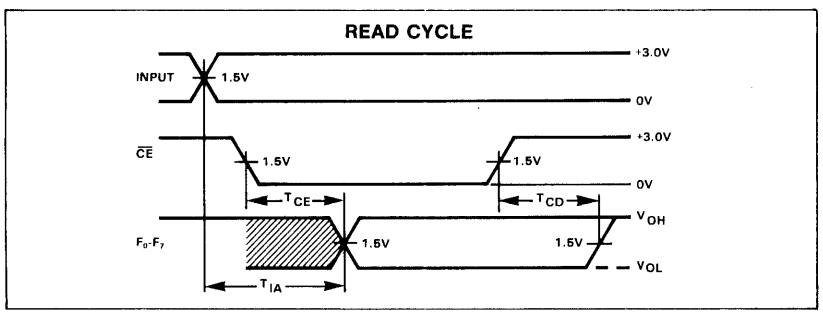
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAM



TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).

T_{IA} Delay between beginning of valid Input (with Chip Enable low) and when Data Output becomes valid.

VIRGIN DEVICE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "false").
3. The "OR" Matrix contains all 48-P-terms.
4. The polarity of each output is set to active high (Fp function).
5. All outputs are at a low logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the "AND" matrix, "OR" matrix, and output polarity outlined below. To maximize recovery from programming errors, leave all links in unused device areas intact.

SET-UP

Terminate all device outputs with a 10K resistor to +5V. Set GND (pin 14) to 0V.

Output Polarity

PROGRAM ACTIVE LOW ($F\dot{p}$ FUNCTION)

Program output polarity before programming "AND" matrix and "OR" matrix. Program 1 output at the time. (S) links of unused outputs are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Set V_{CC} (pin 28) to V_{CCL}.
3. Set $\overline{CE}$ (pin 19), and I_0 through I_{15} to V_{IH}.
4. Apply V_{OPH} to the appropriate output, and remove after a period t_p.
5. Repeat step 4 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCS}.
2. Enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Address a non-existent P-term by applying V_{IH} to all inputs I_0 through I_{15}.
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a high logic level are programmed active low (F_p function), while all outputs at a low logic level are programmed active high (F_p function).
5. Return V_{CC} to V_{CCP} or V_{CCL}.

"AND" Matrix

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set FE (pin 1) to V_{FEL}, and V_{CC} (pin 28) to V_{CCP}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels V_{OHF} and V_{OLF}.

5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.

5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step 6.

5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step 6.

6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.

6c. After t_D delay, return FE input to V_{FEL}.

7. Disable programmed input by returning I_0 to V_{IX}.
8. Repeat steps 5 through 7 for all other input variables.
9. Repeat steps 4 through 8 for all other P-terms.
10. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCP}.
2. Enable F_7 output by setting $\overline{CE}$ to V_{IX}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be verified (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5.
5. Interrogate input variable I_0 as follows:
   A. Lower the input voltage at I_0 from V_{IX} to V_{IH}, and sense the logic state of output F_7.
   B. Lower the input voltage at I_0 from V_{IH} to V_{IL}, and sense the logic state output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	INPUT VARIABLE STATE CONTAINED IN P-TERM
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Don't Care
0 1	0 0	(I_0), $(\overline{I_0})$

Note that 2 tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Disable verified input by returning I_0 to V_{IX}.
7. Repeat steps 5 and 6 for all other input variables.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{IX} from all input variables.

"OR" MATRIX

PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links in the "OR" matrix corresponding to unused outputs and unused P-terms are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_6 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB.

5a. If the P-term is contained in output function F_0 ($F_0 = 1$ or $F_0^* = 0$), got to step 6, (fusing cycle not required).

5b. If the P-term is **not** contained in output function F_0 ($F_0 = 0$ or $F_0^* = 1$), set to fuse the P_n link by forcing output F_0 to V_{OPF}.

6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.

6c. After t_D delay, return FE input to V_{FEL}.

6d. After t_D delay, remove V_{OPF} from output F_0.

7. Repeat steps 5 and 6 for all other output functions.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{CCS} from V_{CC}.

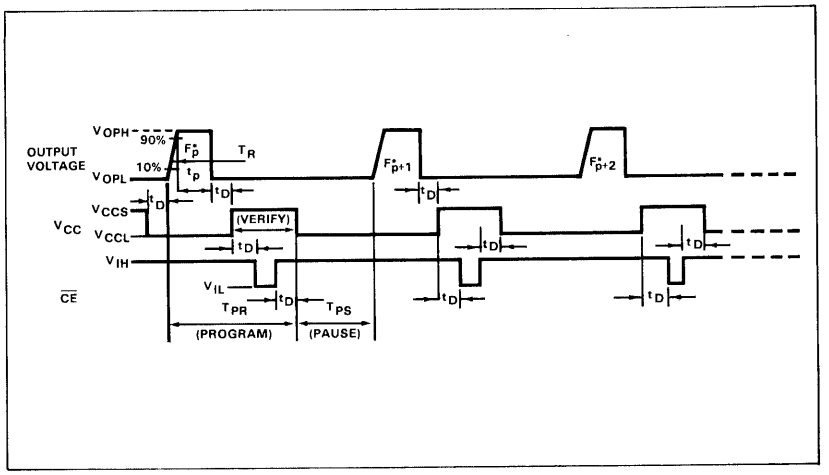
VERIFY PRODUCT TERM

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_0 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5.
5. After t_D delay, enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
6. To determine the status of the P_n link in the "OR" matrix for each output function F_p or F_p^*, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

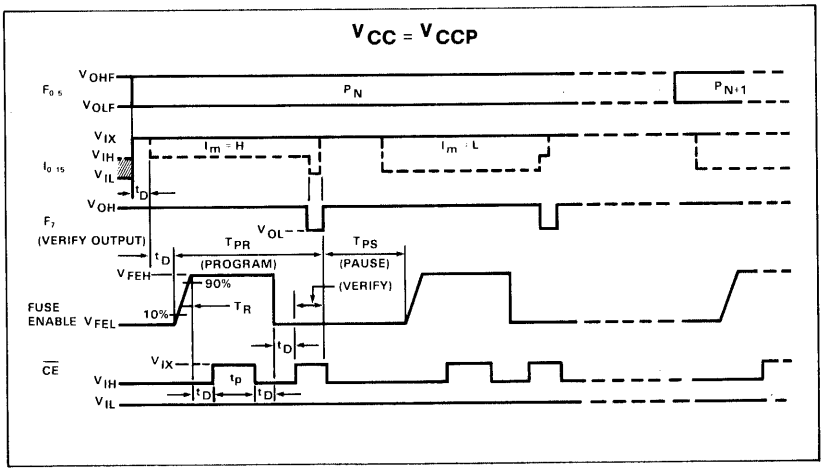
OUTPUT		P-TERM LINK
Active High (F_p)	Active Low (F_p^*)	
0 1	1 0	**Fused** **Present**

7. Repeat steps 4 through 6 for all other P-terms.
8. Remove V_{CCS} from V_{CC}.

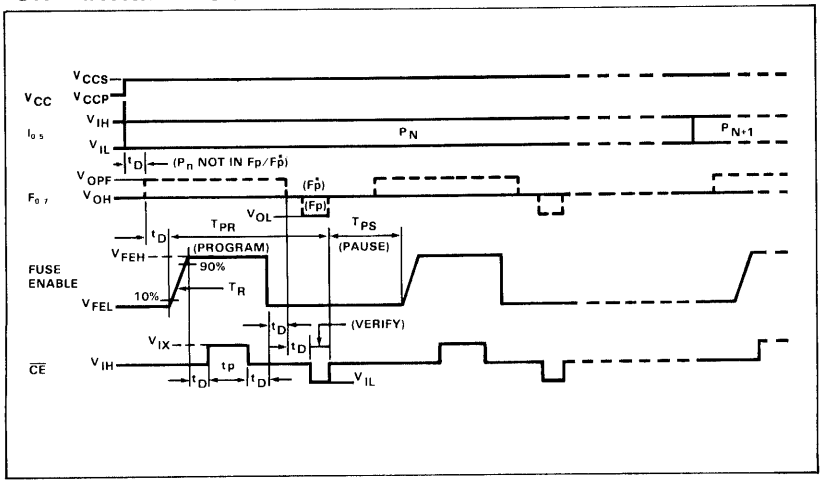
OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



"AND" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



"OR" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



PROGRAMMING SYSTEM SPECIFICATIONS[1] (T_A = +25°C)

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{CCS}	V_{CC} supply (program/verify "OR", verify output polarity)[2]	I_{CCS} = 550mA, min, Transient or steady state	8.5	8.75	9.0	V
V_{CCL}	V_{CC} supply (program output polarity)		0	0.4	0.8	V
I_{CCS}	I_{CC} limit (program "OR")	V_{CCS} = +8.75 ± .25V	550		1,000	mA
	Output voltage					V
V_{OPH}	Program output polarity[3]	I_{OPH} = 300 ± 25mA	16.0	17.0	18.0	
V_{OPL}	Idle		0	0.4	0.8	
I_{OPH}	Output current limit (Program output polarity)	V_{OPH} = +17 ± 1V	275	300	325	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
	Forced output voltage					V
V_{OHF}	High		2.4		5.5	
V_{OLF}	Low		0	0.4	0.8	
	Output current					
I_{OHF}	High	V_{OHF} = +5.5V			100	μA
I_{OLF}	Low	V_{OLF} = 0V			-1	mA
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10V			2.5	mA
I_{IX2}	$\overline{CE}$ input current	V_{IX} = +10V			5.0	mA
V_{FEH}	FE supply (program)[3]	I_{FEH} = 300 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
V_{FEL}	FE supply (idle)	I_{FEL} = -1mA, max	1.25	1.5	1.75	V
I_{FEH}	FE supply current limit	V_{FEH} = +17 ± 1V	275	300	325	mA
V_{CCP}	V_{CC} supply (program/verify "AND")	I_{CCP} = 550mA, min, Transient or steady state	4.75	5.0	5.25	V
I_{CCP}	I_{CC} limit (program "AND")	V_{CCP} = +5.0 ± .25V	550		1,000	mA
V_{OPF}	Forced output (program)		9.5	10	10.5	V
I_{OPF}	Output current (program)				10	mA
T_R	Output pulse rise time		10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms[5]
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle				50	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

1. These are specifications which a Programming System must satisy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01μf capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of the FPLA output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
5. These are new limits resulting from device improvements, and which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

16X48X8 FPLA PROGRAM TABLE

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____

REV _____ DATE _____

PROGRAM TABLE ENTRIES

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	$\overline{Im}$	Don't Care	Prod. Term Present in F_P	Prod. Term Not Present in F_P	Active High	Active Low
H	L	— (dash)	A	• (period)	H	L

NOTE
Enter (—) for unused inputs of used P-terms.

NOTES
1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

NOTES
1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

NO.	PRODUCT TERM* INPUT VARIABLE*																ACTIVE LEVEL* OUTPUT FUNCTION*							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																								
1																								
2																								
3																								
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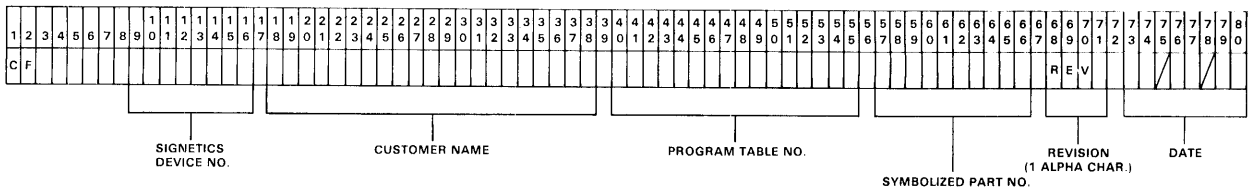
45																								
46																								
47																								

* Input and Output fields of unused P-terms can be left blank. Unused inputs and outputs are FPLA terminals left floating.

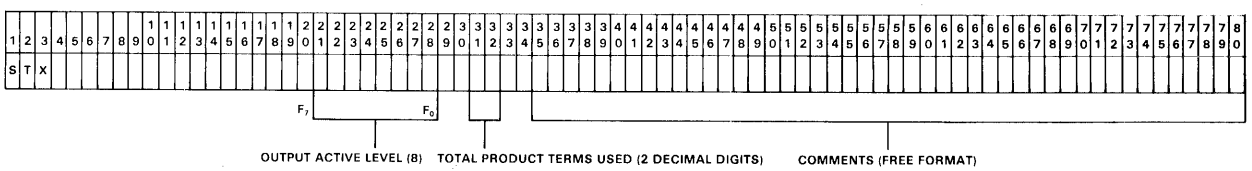
PUNCHED CARD CODING FORMAT

The FPLA Program Table can be supplied directly to Signetics in punched card form, using standard 80-column IBM cards. For each FPLA Program Table, the customer should prepare in input card deck in accordance with the following format. Product Term cards 3 through 50 can be in any order. Not all 48 Product Terms need to be present. Unused Product Terms require no entry cards, and will be skipped during the actual programming sequence:

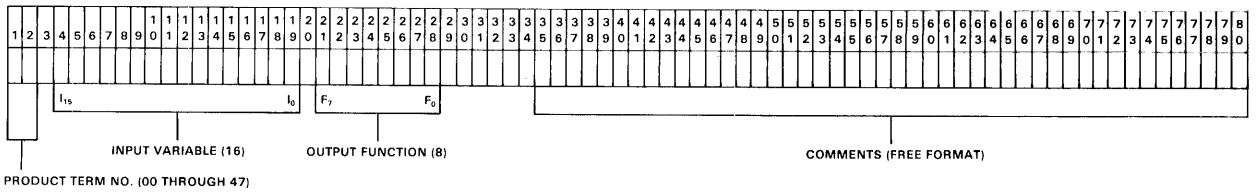
CARD NO.1—Free format within designated fields.



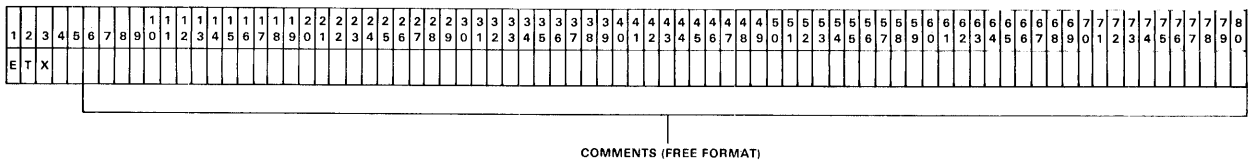
CARD NO. 2—



CARD NO. 3 through NO. 50



CARD NO. 51



Output Active Level entries are determined in accordance with the following table:

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

Input Variable entries are determined in accordance with the following table:

INPUT VARIABLE		
Im H	$\overline{Im}$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

Output Function entries are determined in accordance with the following table:

OUTPUT FUNCTION	
Product term present in FP A	Product term *not* present in FP • (period)

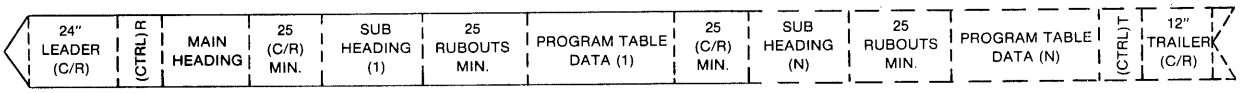
NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

TWX TAPE CODING FORMAT

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



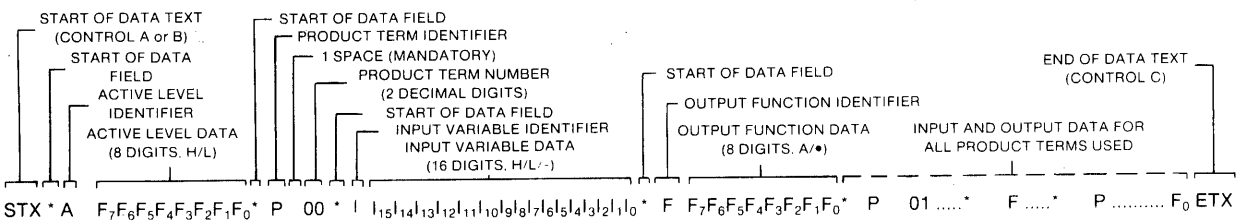
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following format:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE		
I_m H	$\overline{I_m}$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

OUTPUT FUNCTION	
Product term present in Fp A	Product term not present in Fp • (period)

NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

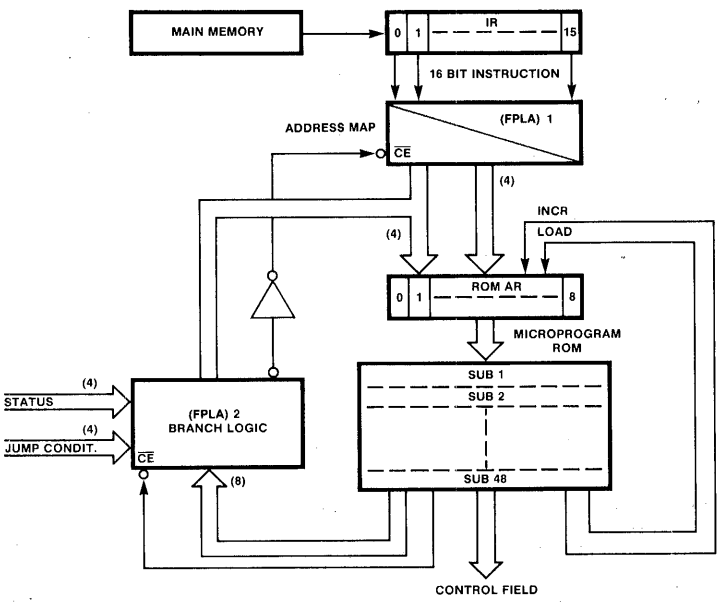
Although the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

NOTES

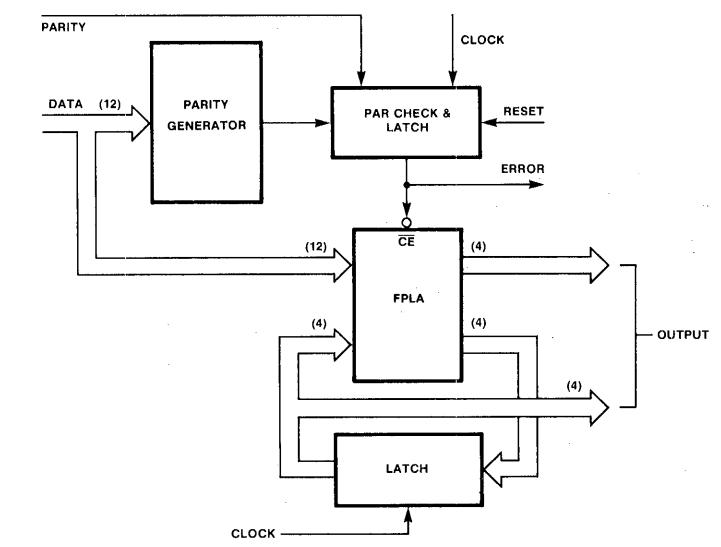
1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. P-Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. Any P-Term can be deleted entirely by inserting the character (E) immediately following the P-Term number to be deleted, i.e., *P 25E deletes P-Term 25.
4. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups, but only preceding an asterisk (*).
5. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

TYPICAL APPLICATIONS

SUBROUTINE ADDRESS MAP



SEQUENTIAL CONTROLLER



DESCRIPTION

The 82S200 (tri-state outputs) and the 82S201 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR tems). Each OR term controls an output function which can be programmed either true active-high (F_P), or true active-low (F_P*). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are mask programmable by supplying to Signetics Program Table data in one of the formats specified in this data sheet.

The 82S200 and 82S201 are fully TTL compatible, and include chip enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S200/201, I or N, and for the military temperature range (-55°C to +125°C) specify S82S200/201, I.

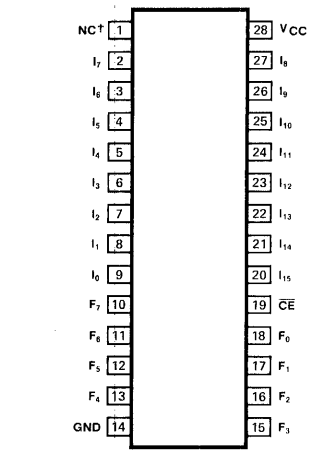
APPLICATIONS*

- **CRT display systems**
- **Random logic**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Sequential controllers**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**

*For diagrams of Typical Applications reference 82S100 (T.S.)/82S101 (O.C.) Data Sheet.

PIN CONFIGURATION

I,N PACKAGE*



*I = Ceramic
N = Plastic
†Open during normal operation

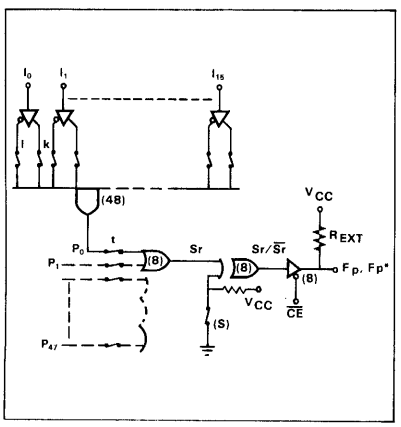
TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	F_P^*
Disabled (82S201)	X	1	X	1	1
Disabled (82S200)				Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

THERMAL RATINGS

TEMPERATURE	MILI-TARY	COM-MER-CIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

PLA EQUIVALENT LOGIC PATH



LOGIC FUNCTION

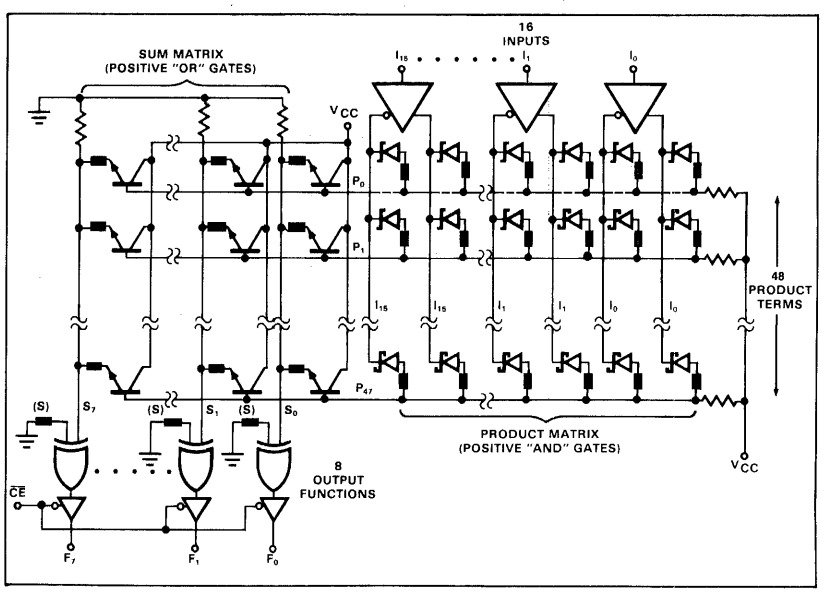
Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions:
$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2)$ @ S = Closed
$F_0^* = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ S = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or $F\dot{p}$ (active low) is available, but not both. The required function polarity is programmed via link (S).

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER		RATING		UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S200/201	0	+75	
	S82S200/201	-55	+125	
T_{STG}	Storage	-65	+150	

DC ELECTRICAL CHARACTERISTICS

N82S200/201: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S200/201: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82S200/201			S82S200/201			UNIT
			Min	Typ [2]	Max	Min	Typ [2]	Max	
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} 7 -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S200)[3,5]	I_{OH} = -2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S200)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S200)[4,8]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

N82S200/201: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

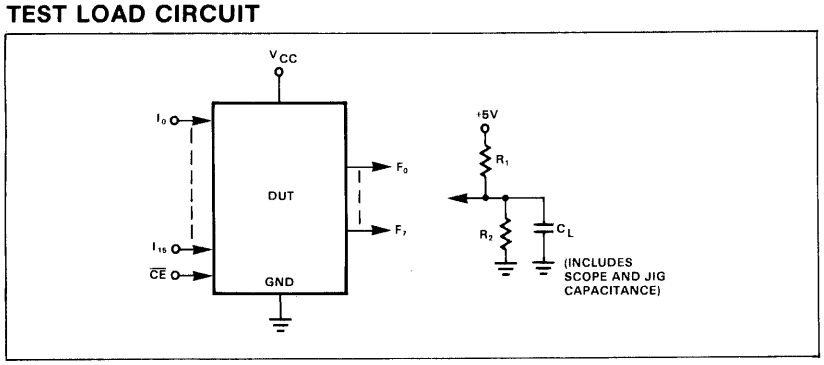
S82S200/201: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TO	FROM	N82S200/201			S82S200/201			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{IA}	Input	Output	Input		35	50		35	80	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	50	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	50	

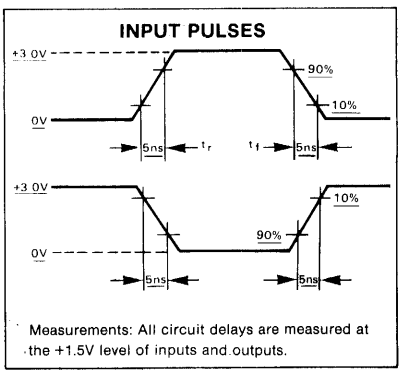
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied thru a resistor to V_{CC}.
7. Measured with: V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

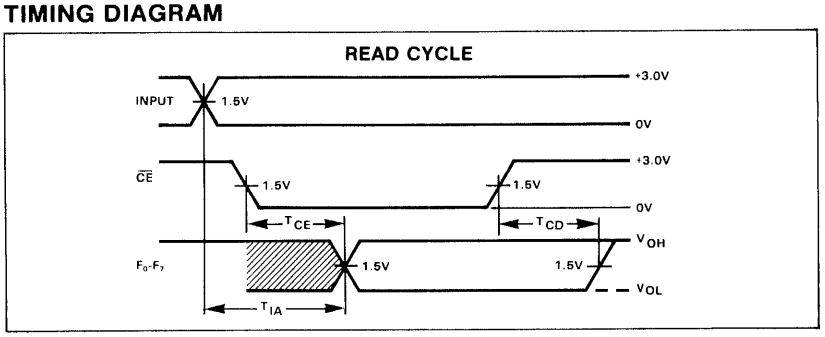
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAM



TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).

T_{IA} Delay between beginning of valid Input (with Chip Enable low) and when Data Output becomes valid.

16X48X8 PLA PROGRAM TABLE

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____

REV _____ DATE _____

PROGRAM TABLE ENTRIES

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	$\overline{Im}$	Don't Care	Prod. Term Present in F_P	Prod. Term Not Present in F_P	Active High	Active Low
H	L	— (dash)	A	• (period)	H	L

NOTE

Enter (—) for unused inputs of used P-terms.

NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

	PRODUCT TERM*															
	INPUT VARIABLE*															
NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																
1																
2																
3																
4																
5																
6																
7																
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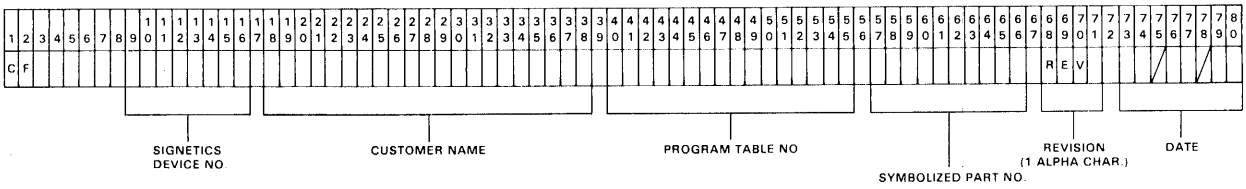
42																
43																
44																
45																
46																
47																

ACTIVE LEVEL*							
OUTPUT FUNCTION*							
7	6	5	4	3	2	1	0

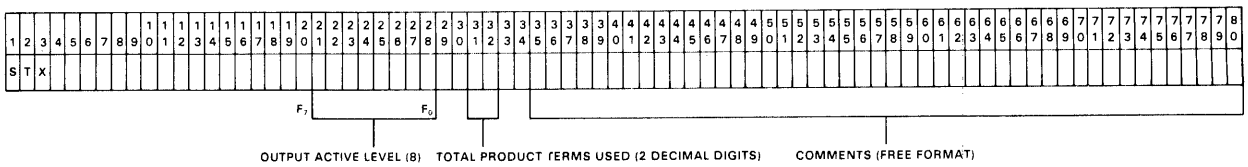
PUNCHED CARD CODING FORMAT

The PLA Program Table can be supplied directly to Signetics in punched card form, using standard 80-column IBM cards. For each PLA Program Table, the customer should prepare an input card deck in accordance with the following format. Product Term cards 3 through 50 can be in any order. Not all 48 Product Terms need to be present. Unused Product Terms require no entry cards, and will be skipped during the actual programming sequence:

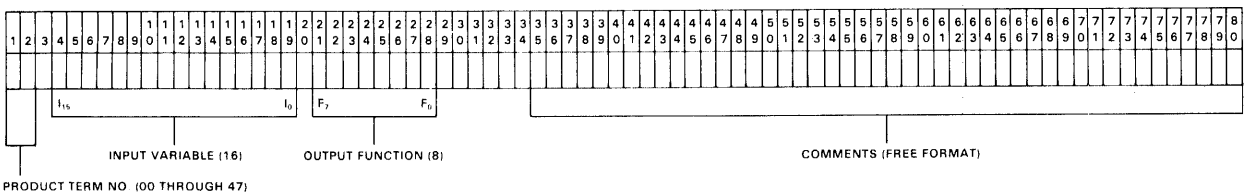
CARD NO.1—Free format within designated fields.



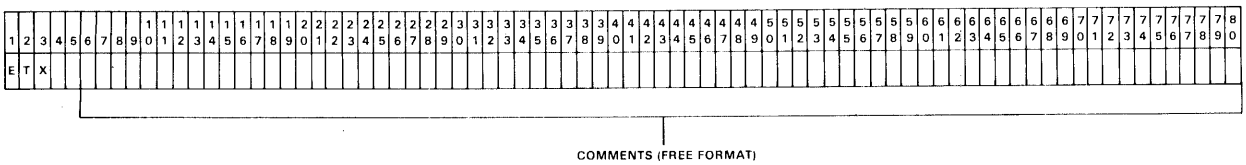
CARD NO. 2—



CARD NO. 3 through NO. 50



CARD NO. 51



Output Active Level entries are determined in accordance with the following table:

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

Input Variable entries are determined in accordance with the following table:

INPUT VARIABLE		
Im H	$\overline{\text{Im}}$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

Output Function entries are determined in accordance with the following table:

OUTPUT FUNCTION	
Product term present in Fp A	Product term not present in Fp • (period)

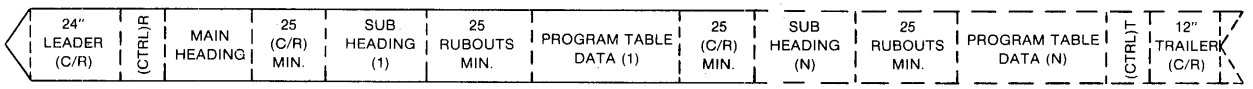
NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

TWX TAPE CODING FORMAT

The PLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



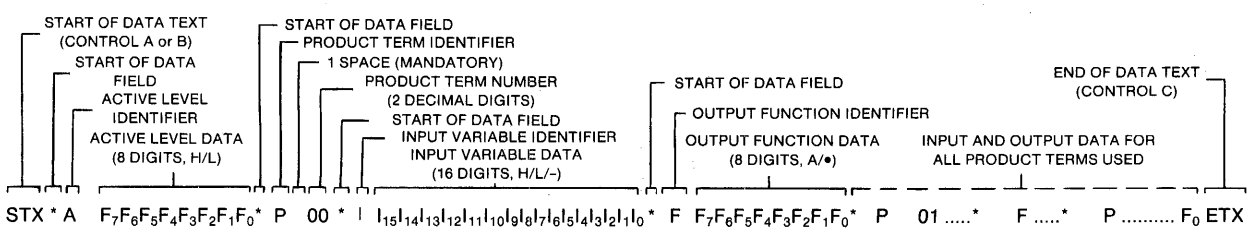
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following format:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE		
I_m H	$\overline{I}_m$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

OUTPUT FUNCTION	
Product term present in Fp A	Product term not present in Fp • (period)

NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

Although the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

NOTES

1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. P-Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. Any P-Term can be deleted entirely by inserting the character (E) immediately following the P-Term number to be deleted, i.e., *P 25E deletes P-Term 25.
4. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups, but only preceding an asterisk (*).
5. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

DESCRIPTION

The 82S102 and 82S103 are Bipolar programmable AND/NAND gate arrays, containing 9 gates sharing 16 common inputs. On-chip input buffers enable the user to individually program for each gate either the True (I_m), Complement ($\overline{I_m}$), or Don't Care (X) logic state of each input. In addition, the polarity of each gate output is individually programmable to implement either AND or NAND logic functions.

Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its input variables, and output (DeMorgan theorem).

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S102 and 82S103 include chip-enable control for output strobing and inhibit. They feature either open collector or tri-state outputs for ease of expansion of input variables and application in bus-organized systems.

Both devices are available in the commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S102/103, I or N, and for the military range (−55°C to +125°C) specify S82S102/103, I.

FEATURES

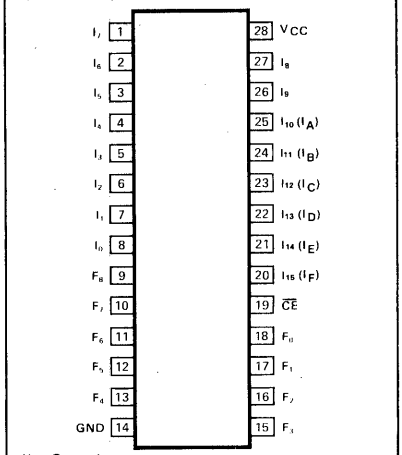
- **Field programmable (NI-Cr link)**
- **16 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay:**
  N82S102/103: 30ns max
  S82S102/103: 50ns max
- **Power dissipation: 600mW typ**
- **Input loading:**
  N82S102/103: −100μA max
  S82S102/103: −150μA max
- **Output options:**
  82S102: Open collector
  82S103: Tri-state
- **Output disable function:**
  82S102: HI
  82S103: HI-Z
- **Fully TTL compatible**

APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

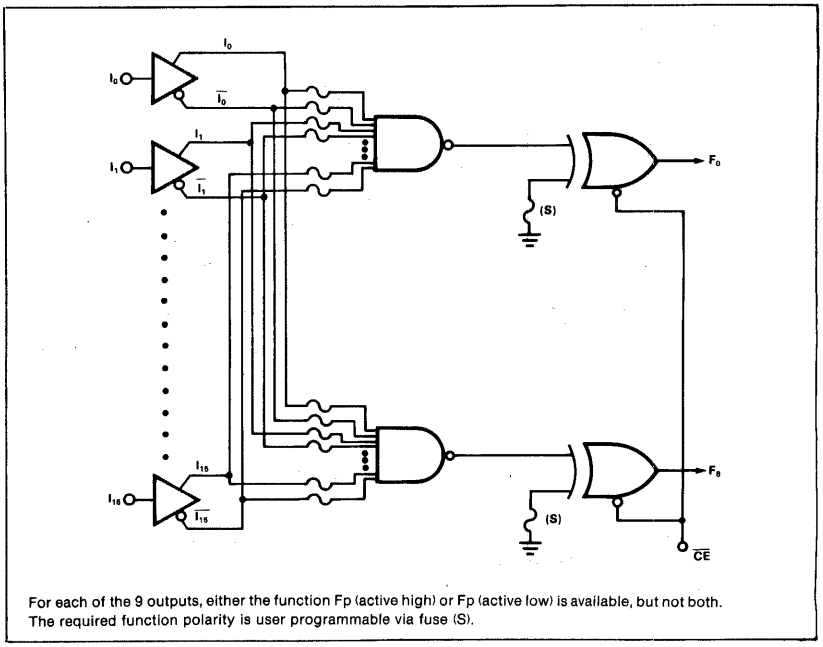
PIN CONFIGURATION

I,N PACKAGE*



*I = Ceramic
N = Plastic

LOGIC DIAGRAM

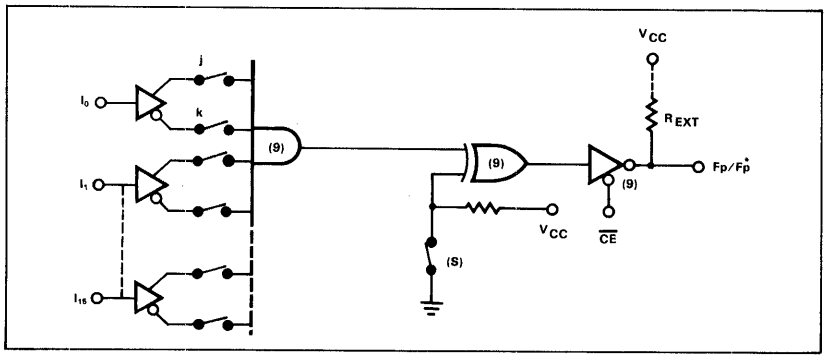


For each of the 9 outputs, either the function Fp (active high) or Fp (active low) is available, but not both. The required function polarity is user programmable via fuse (S).

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S102)	+5.5	
V_O	Off-state (82S103)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating		
	N82S102/103	0 to +75	
	S82S102/103	-55 to +125	
T_{STG}	Storage	-65 to +150	

EQUIVALENT LOGIC PATH



The Field Programmable Gate Array consists of 9 gates with individually programmable inputs and outputs.

The inputs to each gate can be programmed either True (I_m), Complement ($\overline{I_m}$), or Don't Care via corresponding links (j) and (k). The outputs of each gate can be programmed active-high (F_p) or active-low (F_p^*) via corresponding links (S). Thus, each gate provides either of 2 output logic functions in terms of *external* input logic variables X_m as defined below (positive logic):

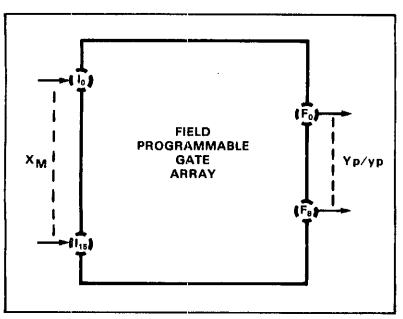
At S = Open:

$F_p = \overline{CE} + (X_0 \bullet X_1 \bullet X_2 \bullet \ldots . X_m) = Y_p$

At S = Closed:

$F_p^* = \overline{CE} + (\overline{X}_0 + \overline{X}_1 + \overline{X}_2 + \ldots . X_m) = y_p$

$m = 0, 1, 2, \ldots . 15$



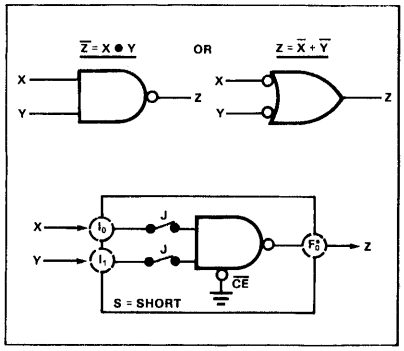
$p = 0, 1, 2, \ldots . 8$

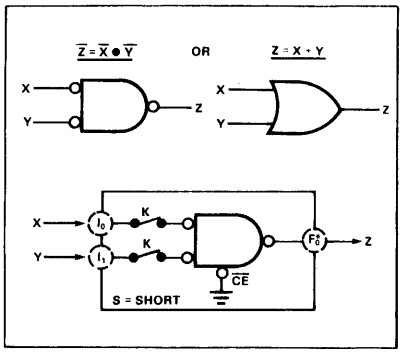
and where $X_m = I_m, \overline{I_m}$, Don't Care, as assigned by programming polarity of inputs I_0–I_{15}.

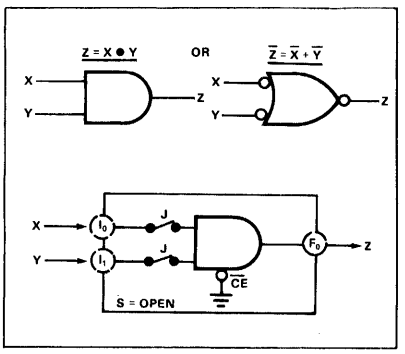
When $\overline{CE}$ = low, all gates are enabled, and $F_p^* = \overline{F}_p$ giving $y_p = \overline{Y}_p$.

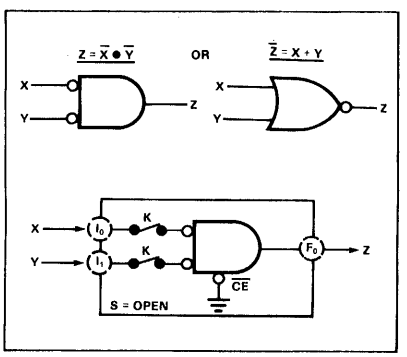
PROGRAMMABLE LOGIC FUNCTIONS

All internal links of virgin FPGAs are intact. Therefore, as shown in the Equivalent Logic Path, all symbolic switches are initially closed. Selective programming (opening) of links (J), (K), and (S) enables the user to assign input and output polarities to each gate for implementing NAND, NOR, AND, OR logic functions without changing the routing of input and output wires. This is shown in the following diagrams for a typical gate in terms of 2 input variables, which can be readily extended up to 16.









DC ELECTRICAL CHARACTERISTICS

N82S102/103: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S102/103: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER[1]		TEST CONDITIONS	N82S102/103			S82S102/103			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S103)[1,5]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S102)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S103)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S103)[3,7]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170		120	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15			15		

AC ELECTRICAL CHARACTERISTICS

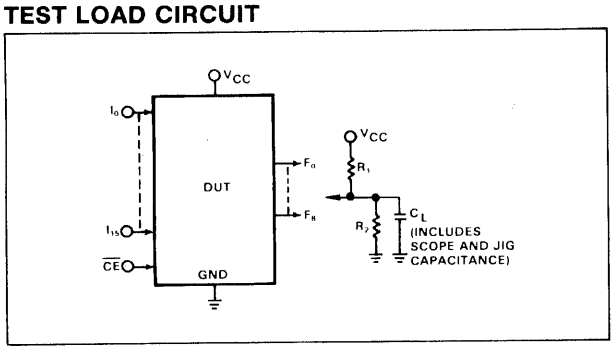
R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S102/103: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S102/103: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TO	FROM	N82S102/103			S82S103/103			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{IA}	Input	Output	Input		20	30		20	50	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	40	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	40	

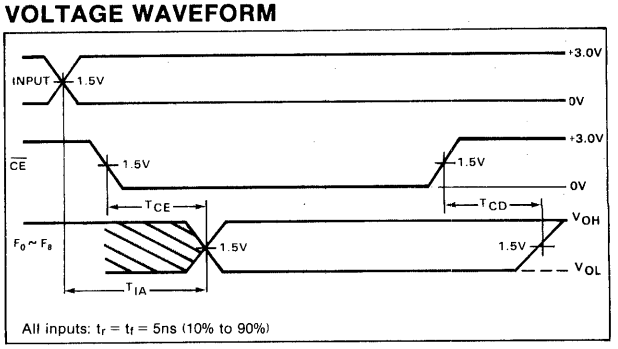
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test each output one at a time.
4. Measured with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

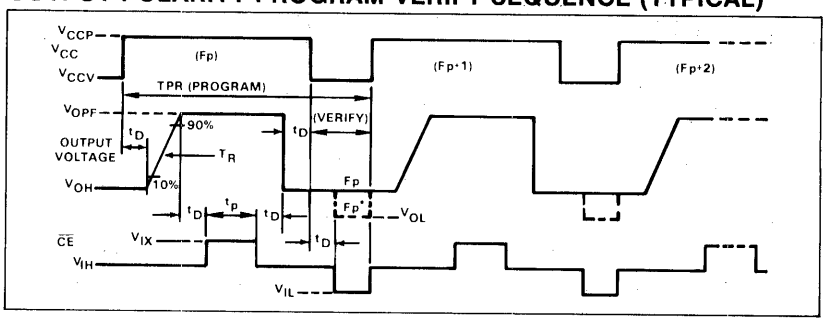
TEST LOAD CIRCUIT



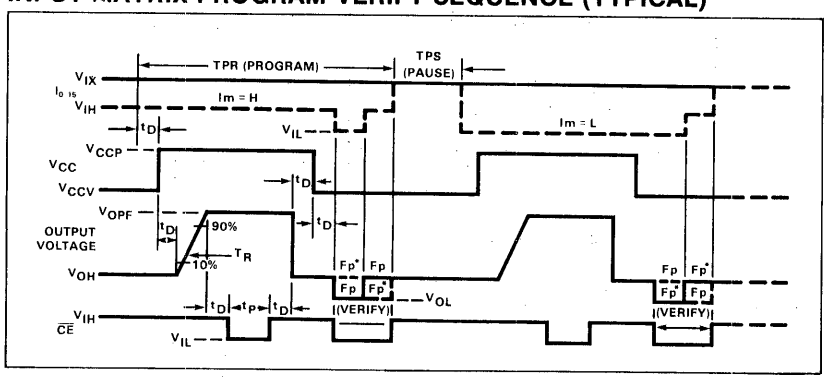
VOLTAGE WAVEFORM



OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



INPUT MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



VIRGIN DEVICE

The 82S102/103 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each gate contains both true and complement values of every input variable I_m (logic Null state).
3. The polarity of each output is set to active low (F_p^* function).
4. All outputs are at a high logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 9 Boolean logic functions of 16 True, Complement, or Don't Care input variables follow the program/verify procedures for the Input Matrix and Output Polarity outlined below. To maximize recovery from programming errors, leave all links of unused gates intact.

SET-UP

Terminate all device outputs with a 10KΩ resistor to +5V.

Output Polarity

PROGRAM ACTIVE HIGH (Fp FUNCTION)

Program output polarity before programming inputs (for convenience). Program one output at a time. (S) links of unused outputs are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Raise V_{CC} (pin 28) from V_{CCV} to V_{CCP}.
B. After t_D delay, force output to be programmed to V_{OPF}.
C. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.
D. After t_D delay, remove V_{OPF} voltage source from output being programmed.
E. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
F. Repeat steps A through E for any other output.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. After t_D delay, set the $\overline{CE}$ input to V_{IL}.
B. Verify output polarity by sensing the logic state of outputs F_0 through F_8. All outputs at a low logic level are programmed active low (F_p^* function), while all outputs at a high logic level are programmed active high (F_p function).

Input Matrix

PROGRAM INPUT VARIABLE

Program one input at a time for one gate at a time. Input variable links of unused gates are not required to be fused. However, unused input variables must be programmed at Don't Care for all used gates.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A-1. If a gate contains nether I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both j and k links by executing both steps A-2 and A-3, before continuing with step C.
A-2. If a gate contains I_0, set to fuse the k link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step B.
A-3. If a gate contains $\overline{I_0}$, set to fuse the j link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step B.
B-1. After t_D delay, raise V_{CC} from V_{CCV} to V_{CCP}.
B-2. After t_D delay, force output of gate to be programmed to V_{OPF}.
B-3. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IL} for a period t_p.
B-4. After t_D delay, remove V_{OPF} voltage source from output of gate being programmed.
B-5. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
C. Disable programmed input by returning I_0 to V_{IX}.
D. Repeat steps A through C for all other input variables.
E. Repeat steps A through D for all other gates to be programmed.
F. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

Unambiguous verification of the logic state programmed for the inputs of each gate requires prior knowledge of its programmed output polarity. Therefore, the output polarity verify procedure must precede input variable verify.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Enable all outputs by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Interrogate input variable I_0 as follows: Lower the input voltage to I_0 from V_{IX} to V_{IL}, and sense the logic state of outputs F_{0-8}.

Raise the input voltage to I_0 from V_{IL} to V_{IH} and sense the logic state of outputs F_{0-8}.

The state of I_0 contained in each gate is determined in accordance with the given truth table. Note that 2 tests are required to uniquely determine the state of the input variable contained in each gate.

B. Disable verified input by returning I_0 to V_{IX}.

C. Repeat steps A and B for all other input variables.

D. Remove V_{IX} from all input variables.

TRUTH TABLE FOR INPUT VERIFICATION

I_0	Fp	$F\dot{p}$	INPUT VARIABLE STATE	LINK FUSED
0	1	0	$\overline{I_0}$	j
1	0	1		
0	0	1	I_0	k
1	1	0		
0	1	0	Don't care	Both
1	1	0		
0	0	1	(I_0), $(\overline{I_0})$	Neither
1	0	1		

PROGRAMMING SYSTEMS SPECIFICATIONS[1] $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	V_{CC} supply					V
V_{CCP}	Program[2]	I_{CCP} = 350 ± 50mA, Transient or steady state	8.5	8.75	9.0	
V_{CCV}	Verify		4.75	5.0	5.25	
I_{CCP}	I_{CC} limit (program)	V_{CCP} = +8.75 ± .25V, Transient or steady state	400	450	500	mA
V_{OPF}	Forced output voltage[3] (program)	I_{OP} = 150 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
I_{OPF}	Output current limit (program)	V_{OP} = +17 ± 1V, Transient or steady state	125	150	175	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10V			5.0	mA
I_{IX2}	$\overline{CE}$ input current	V_{IX} = +10V			10.0	mA
T_R	Output pulse rise time		10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle				100	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

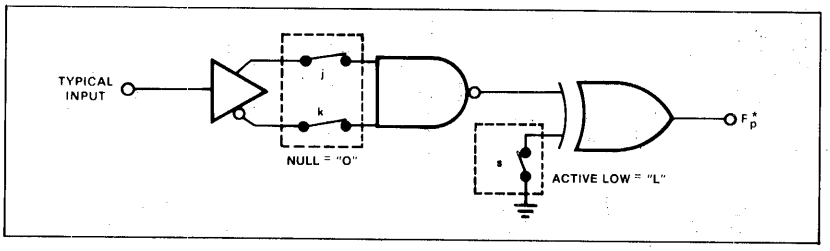
1. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of a gate output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

PROGRAMMING

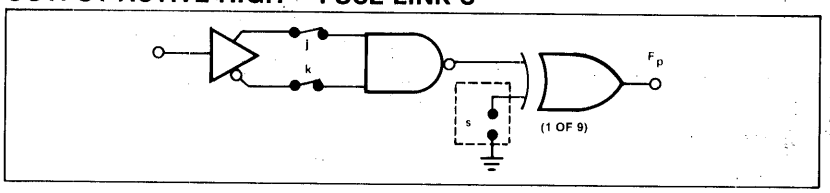
In a virgin device all Ni-Cr links are intact. The initial programmed state of each gate is shown in the Typical Gate illustration.

To program inputs and outputs of each gate for implementing the desired logic function, fuse Ni-Cr links as indicated in the fuse link diagrams.

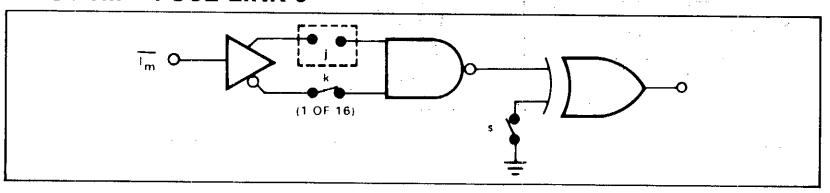
TYPICAL GATE



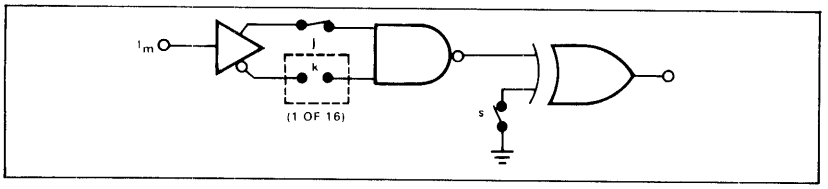
OUTPUT ACTIVE HIGH = FUSE LINK S



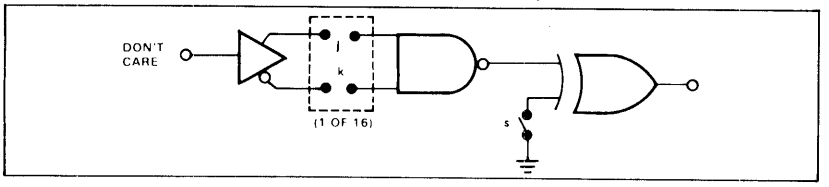
INPUT $\overline{I}m$ = FUSE LINK J



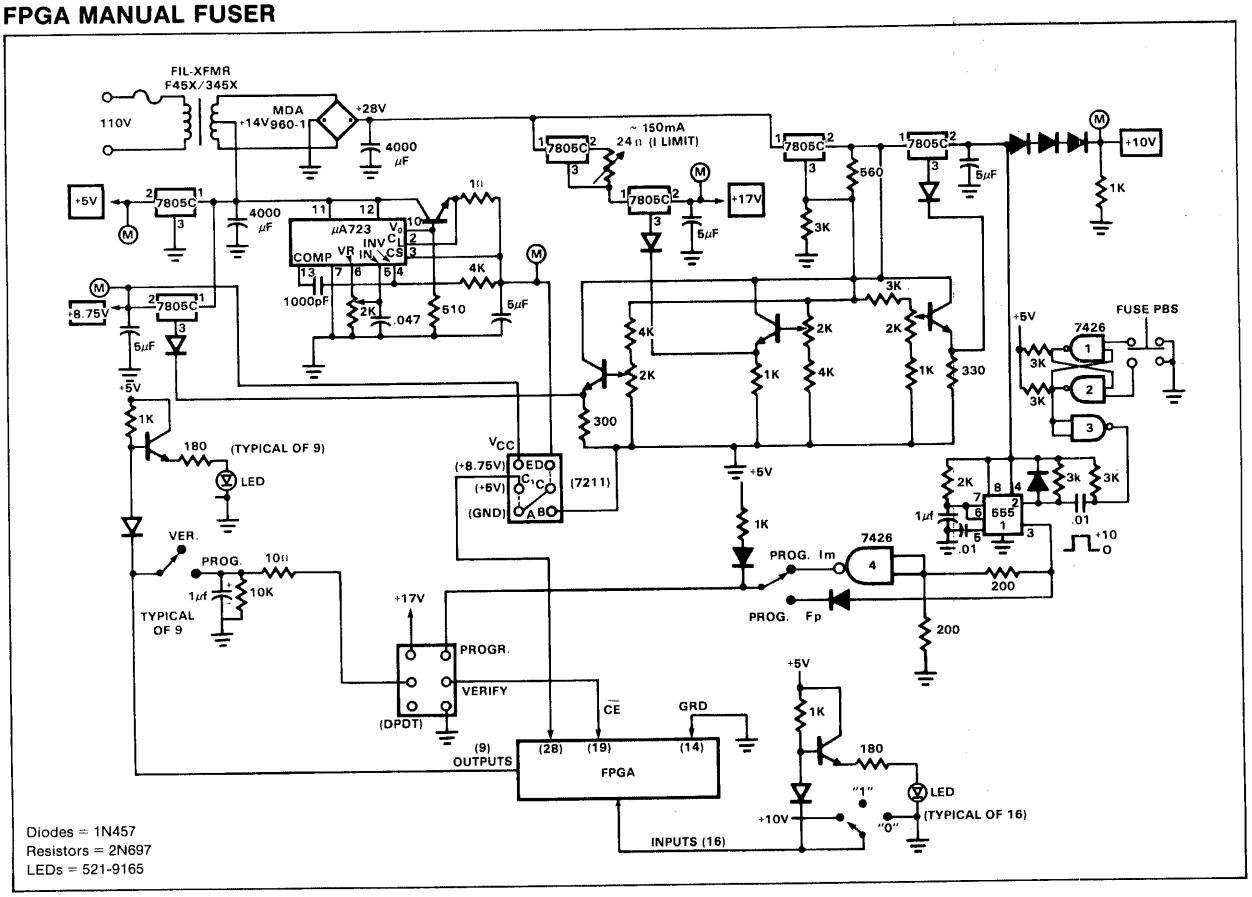
INPUT Im = FUSE LINK K



INPUT DON'T CARE = FUSE BOTH LINKS J, K



FPGA MANUAL FUSER



Diodes = 1N457
Resistors = 2N697
LEDs = 521-9165

16X9 FPGA PROGRAM TABLE

CUSTOMER NAME _____	*THIS PORTION TO BE COMPLETED BY SIGNETICS*
PURCHASE ORDER # _____	*CF (XXXX)* _____
SIGNETICS DEVICE # _____	*CUSTOMER SYMBOLIZED PART #* _____
TOTAL NUMBER OF PARTS _____	*DATE RECEIVED* _____
PROGRAM TABLE # _____	*COMMENTS* _____

F_0 = _____

F_1 = _____

F_2 = _____

F_3 = _____

F_4 = _____

F_5 = _____

F_6 = _____

F_7 = _____

F_8 = _____

OUTPUT POLARITY		INPUT VARIABLE															
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_A	I_B	I_C	I_D	I_E	I_F
F_0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
F_1	16	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
F_2	32	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
F_3	48	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
F_4	64	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
F_5	80	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
F_6	96	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
F_7	112	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
F_8	128	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
Active-high = H Active-low = L		I_m = H $\overline{I_m}$ = L Don't Care = —															

The number in each cell in the table denotes its address for programmers with a decimal address display.

DESCRIPTION

The I/O Port is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 clocked data latches accessible from either a microprocessor port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the I/O Port. In this case, the user port has priority.

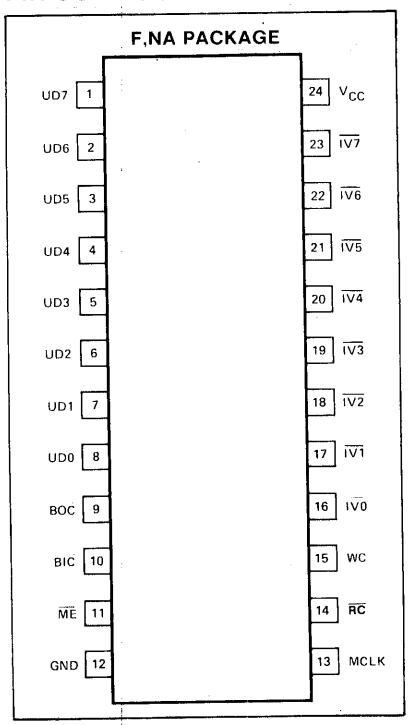
A master enable (ME) is provided that enables or disables the μP bus regardless of the state of the other inputs, but has no effect on the user bus.

A unique feature of this family is its ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, the user port will always be all logic 1 levels, while the microprocessor port will be all logic 0 levels.

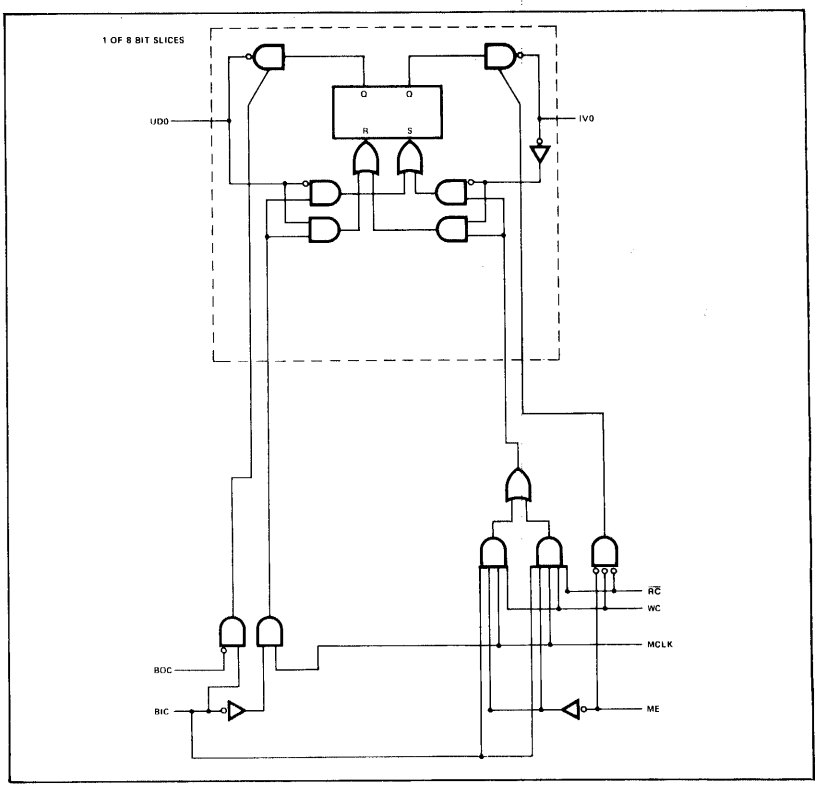
FEATURES

- **Each device has 2 ports, one to the user, the other to a microprocessor. I/O Ports are completely bidirectional**
- **Ports are independent, with the user port having priority for data entry**
- **User data input synchronous**
- **The user data bus is available with tri-state (8T32, 8T36) or open collector (8T33, 8T35) outputs**
- **At power up, the user port outputs are high**
- **Tri-state TTL outputs for high drive capability**
- **Directly compatible with the 8X300 Microcontroller**
- **Operates from a single 5V power supply over a temperature range of 0°C to +70°C**

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	UD0-UD7:	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment.	Acitve high three-state
16-23	$\overline{IV0}$-$\overline{IV7}$:	Microprocessor Bus. Bidirectional data lines to communicate with controlling digital system.	Active low three-state
10	$\overline{BIC}$:	Input Control. User input to control writing into the I/O Port from the user data lines.	Active low
9	$\overline{BOC}$:	Output Control. User input to control reading from the I/O Port onto the user data lines.	Active low
11	$\overline{ME}$:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	Active low
15	WC:	Write Command. When WC is high, stores contents of IV0-IV7 as data.	Active high
14	$\overline{RC}$	Read Command. When RC is low, data is presented on IV0-IV7.	Active low
13	MCLK:	Master Clock. Input to strobe data into the latches. See function tables for details.	Active high
24	V_{CC}:	5V power connection.	
12	GND:	Ground.	

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS FUNCTION
H	L	X	Output Data
L	X	H	Input Data
H	H	X	Inactive

H = High Level L = Low Level X = Don't care

Table 1 USER PORT CONTROL FUNCTION

$\overline{ME}$	$\overline{RC}$	WC	MCLK	$\overline{BIC}$	MICROPROCESSOR BUS FUNCTION
L	L	L	X	X	Output Data
L	X	H	H	H	Input Data
X	H	L	X	X	Inactive
X	X	H	X	L	Inactive
H	X	X	X	X	Inactive

Table 2 MICROPROCESSOR PORT CONTROL FUNCTION

USER DATA BUS CONTROL

The activity of the user data bus is controlled by the BIC and BOC inputs as shown in Table 1.

The user data input is a synchronous function with MCLK. A low level on the BIC input allows data on the user data bus to be written into the data latches only if MCLK is at a high level. A low level on the BIC input allows data on the user data bus to be latched regardless of the level of the MCLK input.

To avoid conflicts at the data latches, input from the microprocessor port is inhibited when BIC is at a low level. Under all other conditions the 2 ports operate independently.

MICROPROCESSOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port is controlled by the ME, RC, WC and BIC inputs, as well as the state of an internal status latch. BIC is included to show user port priority over the microprocessor port for data input.

BUS OPERATION

Data written into the I/O Port from one port will appear inverted when read from the other port. Data written into the I/O Port from one port will not be inverted when read from the same port.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ TA ≤ 70°C unless otherwise specified.

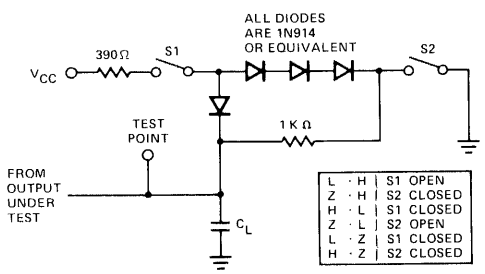
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Min	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				.8	
V_{IC}	Clamp	I_I = -5mA			-1	
	Output voltage	V_{CC} = 4.75V				V
V_{OH}	High		2.4			
V_{OL}	Low				.55	
	Input current[1]	V_{CC} = 5.25V				μA
I_{IH}	High	V_{IH} = 5.25V		<10	100	
I_{IL}	Low	V_{IL} = .5V		-350	-550	
	Output current[2]					mA
I_{OS}	Short circuit	V_{CC} = 4.75V				
	UD bus		10			
	IV bus		20			
I_{CC}	VCC supply current	V_{CC} = 5.25V		100	150	mA

NOTES

1. The input current includes the tri-state/open collector leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.

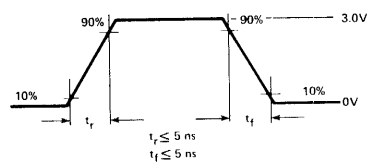
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR TRI-STATE OUTPUTS

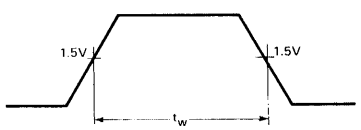


NOTE: C_L includes fixture capacitance.

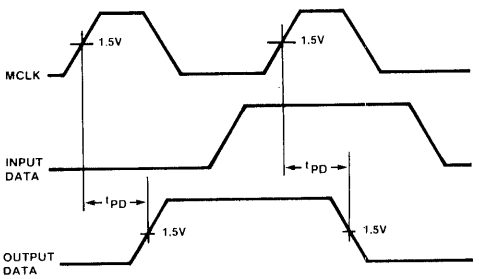
INPUT WAVEFORM



CLOCK PULSE WIDTH



DATA DELAY TIMES
Clock Referenced



AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 5\%$

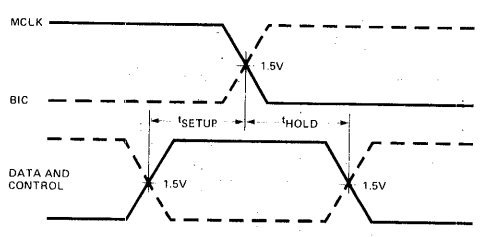
PARAMETER	INPUT	TEST CONDITION	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_{PD} User data delay[1]	UDX	$C_L = 50pF$		25	38	ns
	MCLK			45	61	ns
t_{OE} User output enable	BOC	$C_L = 50pF$	18	26	47	ns
t_{OD} User output disable	BIC	$C_L = 50pF$	18	28	35	ns
	BOC		16	23	33	ns
t_{PD} μP data delay[1]	IVBX	$C_L = 50pF$		38	53	ns
	MCLK			48	61	ns
t_{OE} μP output enable	ME RC WC	$C_L = 50pF$	14	19	25	ns
t_{OD} μP output disable	ME RC WC	$C_L = 50pF$	13	17	32	ns
t_W Minimum pulse width	MCLK		40			ns
t_{SETUP} Minimum setup time[2]	UDX[3]		15			
	BIC		25			
	IVX		55			
	ME		30			ns
	RC		30			
	WC		30			
t_{HOLD} Minimum hold time[2]	UDX[3]		25			
	BIC		10			
	IVX		10			
	ME		5			ns
	RC		5			
	WC		5			

NOTES

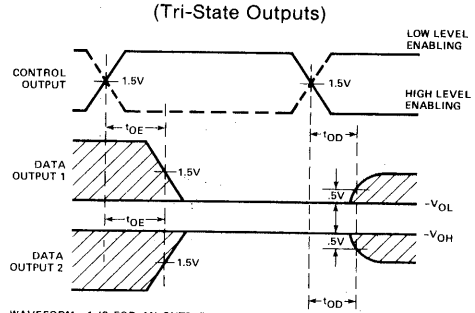
1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Set up and hold times given are for "normal" operation. BIC setup and hold times are for a user write operation. RC setup and hold times are for an I/O Port select operation. ME and WC setup and hold times are for a microprocessor bus write operation.
3. Times are referenced to MCLK

VOLTAGE WAVEFORMS

SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(Tri-State Outputs)



WAVEFORM #1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW WHEN THE TRI-STATE DRIVER IS ENABLED. WAVEFORM #2 IS FOR THE OPPOSITE CONDITION.

TYPES

8T32 Tri-State, Synchronous User Port
8T33 Open Collector, Synchronous User Port
8T35 Open Collector, Asynchronous User Port
8T36 Tri-State, Asynchronous User Port

DESCRIPTION

The Addressable I/O Port is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 data latches accessible from either a microprocessor port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the I/O Port. In this case, the user port has priority.

A unique feature of the I/O Port is the way in which it is addressed. Each device has an 8-bit, field programmable address, which is used to enable the microprocessor port. When the SC control signal is high, data at the microprocessor port is treated as an address. If the address matches the I/O Port's internally programmed address, the microprocessor port is enabled, allowing data transfer through it.

The port remains enabled until an address which does not match is presented, at which time the port is disabled (data transfer is inhibited). A Master Enable input (ME) can serve as a ninth address bit, allowing 512 I/O Ports to be individually selected on a bus, without decoding. The user port is accessible at all times, independent of whether or not the microprocessor port is selected.

A unique feature of this family is their ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, the user port will always be all logic 1 levels, while the port will be all logic 0 levels.

ORDERING

The 8T32/33/35/36 may be ordered in preaddressed form. To order a preaddressed device use the following part number format:

N8TYY-XXX P

- P = F Ceramic package, NA Plastic package
- XXX = Any address from 000 through 255 (decimal) - 256 available addresses
- YY = I/O Port version (32, 33, 35, 36)

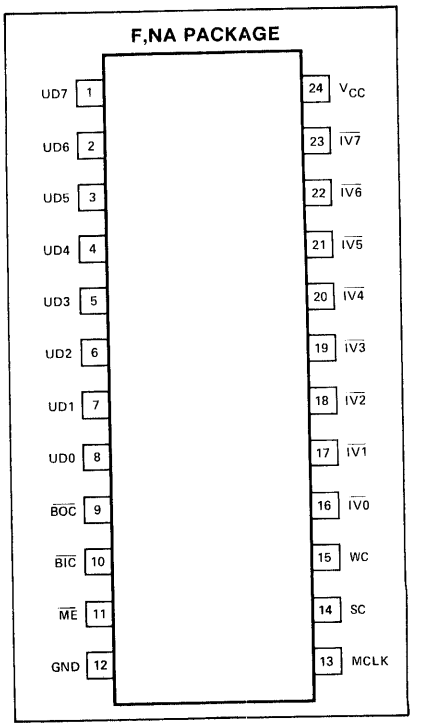
A stock of 8T32s and 8T36s with addresses 1 through 10 will be maintained. A small quantity of addresses 11 through 50 will also be available with a longer lead time.

FEATURES

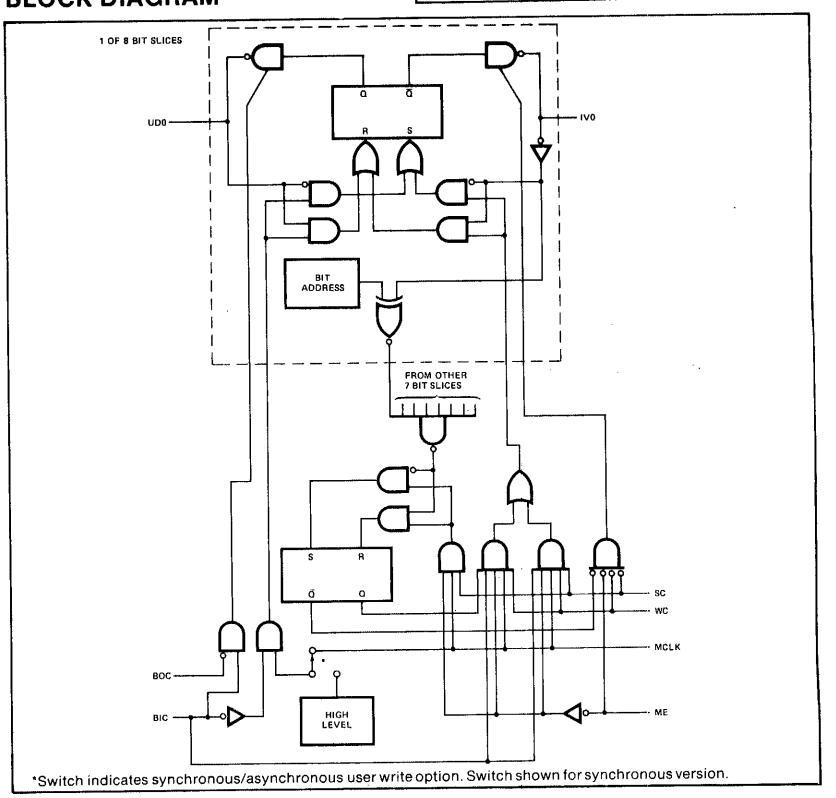
- **A field-programmable address allows 1 of 512 I/O Ports on a bus to be selected, without decoders.**
- **Each device has 2 ports, one to the user, the other to a microprocessor.**
- **Completely bidirectional.**
- **Ports are independent, with the user port having priority for data entry.**
- **A selected I/O Port de-selects itself when another I/O Port address is sensed.**
- **User data input available as synchronous (8T32, 8T33) or as asynchronous (8T35, 8T36) function.**
- **The user data bus is available with tri-state (8T32, 8T36) or open collector (8T33, 8T35) outputs.**
- **At power up, the I/O Port is not selected and the user port outputs are high.**
- **Tri-state TTL outputs for high drive capability.**
- **Directly compatible with the 8X300 Microcontroller.**
- **Operates from a single 5V power supply over a temperature range of 0° C to 70° C.**

PIN CONFIGURATION

F,NA PACKAGE



BLOCK DIAGRAM



*Switch indicates synchronous/asynchronous user write option. Switch shown for synchronous version.

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	UD0-UD7:	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment. Either tri-state or open collector outputs are available.	Active high
16-23	$\overline{IV0}$-$\overline{IV7}$:	Microprocessor Bus. Bidirectional data lines to communicate with controlling digital system (microprocessor).	Active low three-state
10	$\overline{BIC}$:	Input Control. User input to control writing into the I/O Port from the user data lines.	Active low
9	$\overline{BOC}$:	Output Control. User input to control reading from the I/O Port onto the user data lines.	Active low
11	$\overline{ME}$:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	Active low
15	WC:	Write Command. When WC is high and SC is low, I/O Port, if selected, stores contents of IV0-IV7 as data.	Active high
14	SC:	Select Command. When SC is high and WC is low, data on IV0-IV7 is interpreted as an address. I/O Port selects itself if its address is identical to μP bus data; it de-selects itself otherwise.	Active high
13	MCLK:	Master Clock. Input to strobe data into the latches. See function tables for details.	Active high
24	VCC:	5V power connection.	
12	GND:	Ground.	

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS FUNCTION	
			8T32, 8T33	8T35, 8T36
H	L	X	Output Data	Output Data
L	X	H	Input Data	Input Data
L	X	L	Inactive	Input Data
H	H	X	Inactive	Inactive

H = High Level L = Low Level X = Don't care

Table 1 USER PORT CONTROL FUNCTION

$\overline{ME}$	SC	WC	MCLK	$\overline{BIC}$	STATUS LATCH	I/O PORT FUNCTION
L	L	L	X	X	SET	Output Data
L	L	H	H	H	SET	Input Data
L	H	L	H	X	X	Input Address
L	H	H	H	L	X	Input Address
L	H	H	H	H	X	Input Data and Address
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	Not Set	Inactive
H	X	X	X	X	X	Inactive

Table 2 MICROPROCESSOR PORT CONTROL FUNCTION

USER DATA BUS CONTROL

The activity of the user data bus is controlled by the BIC and BOC inputs as shown in Table 1.

For the 8T32 and 8T33, user data input is a synchronous function with MCLK. A low level on the BIC input allows data on the user data bus to be written into the data latches only if MCLK is at a high level. For the 8T35 and 8T36, user data input is an asynchronous function. A low level on the BIC input allows data on the user data bus to be latched regardless of the level of the MCLK input. Note that when 8T35 or 8T36 are used with the 8X300 Microcontroller care must be taken to insure that the Microprocessor bus is stable when it is being read by the 8X300 Microcontroller.

To avoid conflicts at the Data Latches, input from the Microprocessor Port is inhibited when BIC is at a low level. Under all other conditions the 2 ports operate independently.

MICROPROCESSOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port is controlled by the ME, SC, WC and BIC inputs, as well as the state of an internal status latch. BIC is included to show user port priority over the microprocessor port for data input.

Each I/O Port's status latch stores the result of the most recent I/O Port select; it is set when the I/O Port's internal address matches the Microprocessor Bus. It is cleared when an address that differs from the internal address is presented on the Microprocessor Bus.

In normal operation, the state of the status latch acts like a master enable; the microprocessor port can transfer data only when the status latch is set.

When SC and WC are both high, data on the Microprocessor Bus is accepted as data, whether or not the I/O Port was selected. The data is also interpreted as an address. The I/O Port sets its select status if its address matches the data read when SC and WC were both high; it resets its select status otherwise.

BUS OPERATION

Data written into the I/O Port from one port will appear inverted when read from the other port. Data written into the I/O Port from one port will not be inverted when read from the same port.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER	INPUT	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
t_{PD} User data delay (Note 1)	UDX MCLK* BIC†	C_L = 50pF		25 45 40	38 61 55	ns
t_{OE} User output enable	BOC	C_L = 50pF	18	26	47	ns
t_{OD} User output disable	BIC BOC	C_L = 50pF	18 16	28 23	35 33	ns
t_{PD} µP data delay (Note 1)	IVBX MCLK	C_L = 50pF		38 48	53 61	ns
t_{OE} µP output enable	ME SC WC	C_L = 50pF	14	19	25	ns
t_{OD} µP output disable	ME SC WC	C_L = 50pF	13	17	32	ns
t_W Minimum pulse width	MCLK BIC†		40 35			ns
t_{SETUP} Minimum setup time	UDX□ BIC* IVX ME SC WC	(Note 2)	15 25 55 30 30 30			ns
t_{HOLD} Minimum hold time	UDX□ BIC* IVX ME SC WC	(Note 2)	25 10 10 5 5 5			ns

* Applies for 8T32 and 8T33 only.
† Applies for 8T35 and 8T36 only.
□ Times are referenced to MCLK for 8T32 and 8T33, and are referenced to BIC for 8T35 and 8T36.

NOTES:

1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Set up and hold times given are for "normal" operation. BIC setup and hold times are for a user write operaton. SC setup and hold times are for an I/O Port select operation. WC setup and hold times are for an Microprocessor Bus write operation. ME setup and hold times are for both IV write and select operations.

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				.8	V
V_{CL}	Input clamp voltage	$I_I = -5mA$			-1	V
I_{IH}	High-level input current[1]	$V_{CC} = 5.25V$ $V_{IH} = 5.25V$		<10	100	μA
I_{IL}	Low level input current[1]	$V_{CC} = 5.25V$ $V_{IL} = .5V$		-350	-550	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$ $I_{OL} = 16mA$			.55	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$ $I_{OH} = -3.2mA$	2.4			V
I_{OS}	Short-circuit output current[2] UD bus IV bus	 $V_{CC} = 4.75V$ $V_{CC} = 4.75V$	 10 20			 mA mA
I_{CC}	Supply current	$V_{CC} = 5.25V$		100	150	mA

NOTES

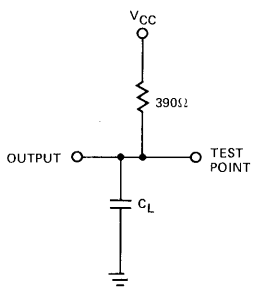
1. The input current includes the Tri-state/Open Collector leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.
3. These limits do not apply during address programming.

Absolute Maximum Ratings:

Supply voltage[3] 7V

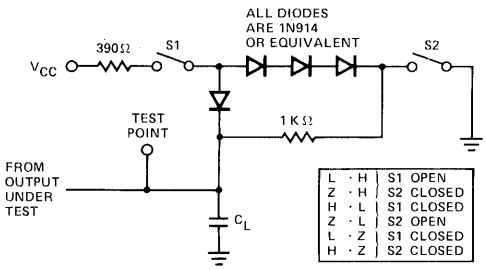
Input voltage[3] 5.5V

TEST LOAD CIRCUIT (OPEN COLLECTOR OUTPUTS)



NOTE: C_L includes fixture capacitance.

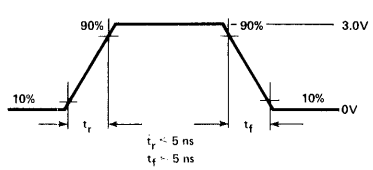
TEST LOAD CIRCUIT (TRI-STATE OUTPUTS)



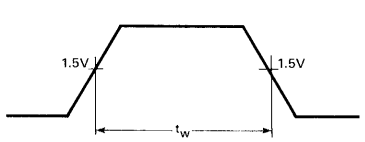
NOTE: C_L includes fixture capacitance.

VOLTAGE WAVEFORMS

INPUT WAVEFORM

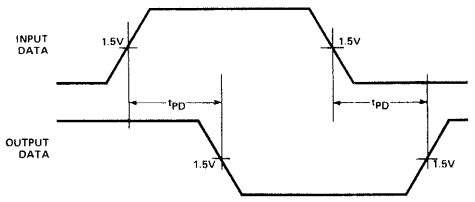


CLOCK PULSE WIDTH

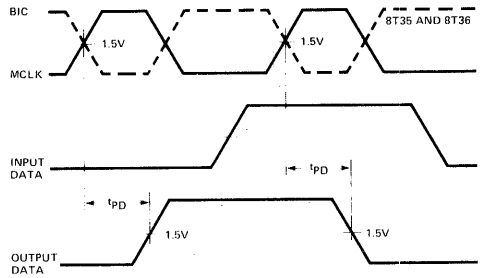


VOLTAGE WAVEFORMS (Cont'd)

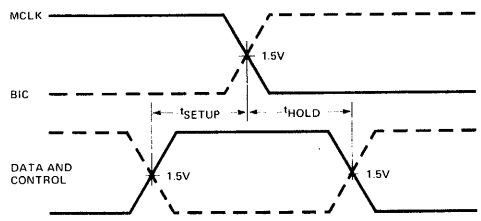
DATA DELAY TIMES
Input Data Reference



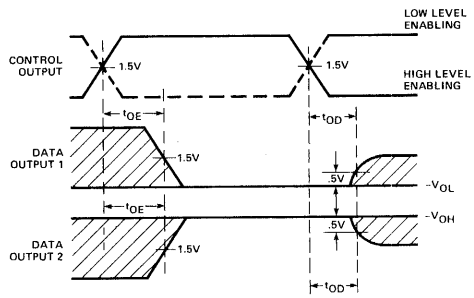
DATA DELAY TIMES
Clock Referenced



SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(Tri-State Outputs)



Waveform #1 is for an output with internal conditions such that the output is Low when the tri-state driver is enabled. Waveform #2 is for the opposite condition.

ADDRESS PROGRAMMING

The I/O Port is manufactured such that an address of all high levels (>2V) on the Microprocessor Bus inputs matches the Port's internal address. To program a bit so a low-level input (<0.8V) matches, the following procedure should be used:

1. Set all control inputs to their inactive state (BIC = BOC = ME = V_{CC}, SC = WC = MCLK = GND). Leave all Microprocessor Bus I/O pins open.
2. Raise V_{CC} to 7.75V ± .25V.
3. After V_{CC} has stabilized, apply a single programming pulse to the user data bus bit where a low-level match is desired. The voltage should be limited to 18V; the current should be limited to 75mA. Apply the pulse as shown in Figure 1.
4. Return V_{CC} to 0V. (Note 1).
5. Repeat this procedure for each bit where a low-level match is desired.
6. Verify that the proper address is programmed by setting the Port's status latch (IV0-IV7 = desired address, ME = WC = L, SC = MCLK = H). If the proper address has been programmed, data presented at the µP bus will appear inverted on the user bus outputs. (Use normal V_{CC} and input voltage for verification.)

After the desired address has been programmed, a second procedure must be followed to isolate the address circuitry. The procedure is:

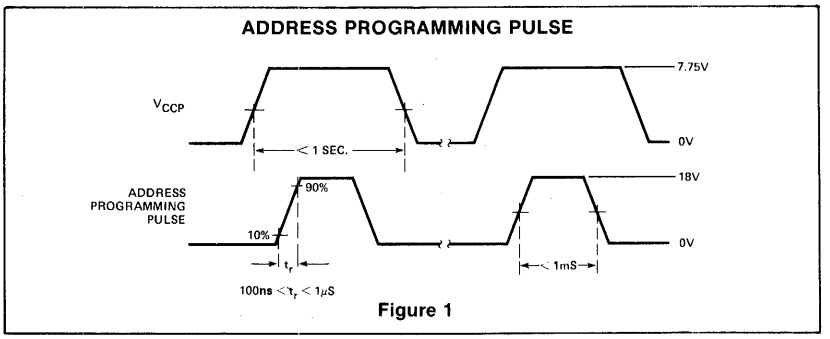


Figure 1

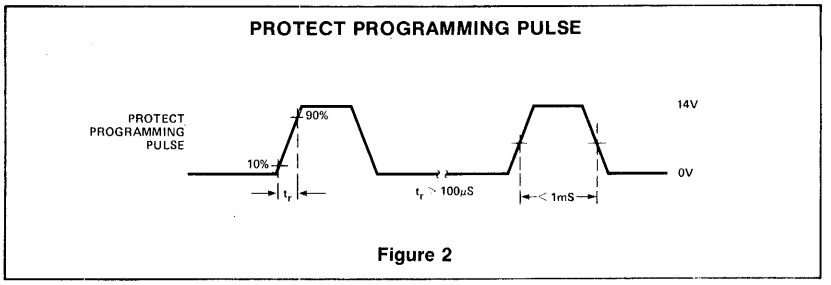


Figure 2

1. Set V_{CC} and all control inputs to 0V. (V_{CC} = BIC = BOC = ME = SC = WC = MCLK = 0V). Leave all Microprocessor Bus I/O pins open.
2. Apply a protect programming pulse to every user data bus pin, one at a time. The voltage should be limited to 14V; the current should be limited to 150mA. Apply the pulse as shown in Figure 2.
3. Verify that the address circuitry is isolated by applying 7V to each user data bus pin and measuring less than 1mA of input current. The conditions should be the same as in step 1 above. The rise time on the verification voltage must be slower than 100µs.

PROGRAMMING SPECIFICATIONS[1]

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{CCP}	Programming supply voltage					
	Address		7.5		8.0	V
	Protect			0		V
I_{CCP}	Programming supply current	V_{CCP} = 8.0V			250	mA
	Max time V_{CCP} > 5.25V				1.0	s
	Programming voltage					
	Address		17.5		18.0	V
	Protect		13.5		14.0	V
	Programming current					
	Address				75	mA
	Protect				150	mA
	Programming pulse rise time					
	Address		.1		1	µs
	Protect		100			µs
	Programming pulse width		.5		1	ms

NOTE

1. If all programming can be done in less than 1 second, V_{CC} may remain at 7.75V for the entire programming cycle.

APPLICATIONS

Figure 3 shows some of the various ways to use the I/O Port in a system. By controlling the BIC and BOC lines, the device may be used for the input and output of data, control, and status signals. I/O Port 1 functions bidirectionally for data transfer and I/O Port 2 provides a similar function for discrete status and control lines. I/O Ports 3 and 4 serve as dedicated output and input ports, respectively.

8T32 APPLICATIONS

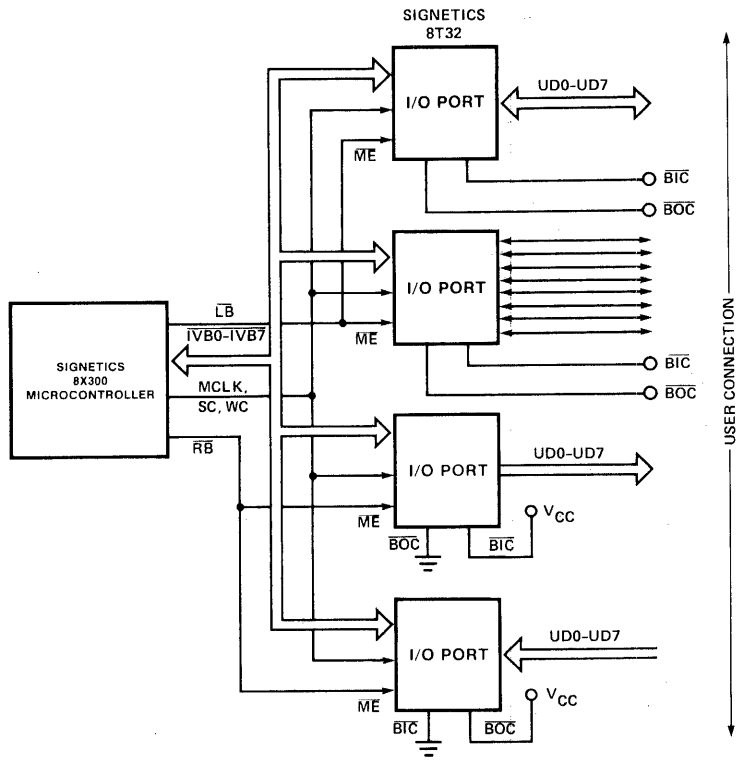


Figure 3

DESCRIPTION

The Bus Expander is specifically designed to increase the I/O capability of 8X300 systems previously limited by fanout considerations. The bus expander serves as a buffer between the 8X300 and blocks of I/O devices. Each bus expander can buffer a block of 16 I/O ports while only adding a single load to the 8X300.

FEATURES

- **15ns max propagation delay**
- **Bidirectional**
- **Three-state outputs on both ports**
- **Pre-programmed address range**

APPLICATIONS

The 8T39 Bus Expander is designed to be used with the 8X300 microprocessor to allow increased I/O capability in those systems previously limited by fanout considerations. Figure 1 shows a typical arrangement of the bus expander in an 8X300 system. Each expander services I/O ports whose address is within the range of the expander. Other I/O ports or working storage may be directly connected to the bus as shown.

The bus expander is not limited to use with the 8X300, but may be applied in any system which uses a combined address/data bus.

8T39 ADDRESSING

During normal operation of the 8X300 when an I/O port address is being sent on the IV Bus (SC is high), the I/O port will examine all eight bits of the microprocessor bus for an address compare. Since the 8T39 is used to buffer blocks of I/O ports, only the four most significant bits are examined by the 8T39 for an address compare.

Note that redundant addresses are not programmed into separate devices. Rather, a discrete device (such as the 8T39-03) may be wired for any address requiring two 1 bits and two 0 bits in the address. The various address ranges for this same device are obtained by permuting the high order (DI0 and DO0 are MSB) data lines accordingly. Both input and output lines must be redefined in order to maintain data and address integrity on the extended bus. Table 1 summarizes the 8T39 addressing.

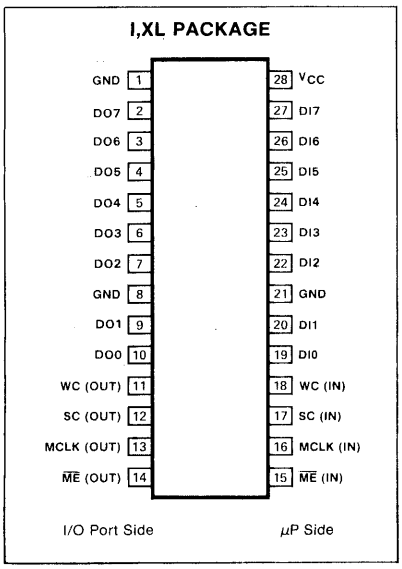
Address functions are specified with the convention that bit 0 is the MSB and bit 7 is the LSB. The DI microprocessor bus address decoding is active low.

FUNCTIONAL DESCRIPTION

The Bus Expander contains eight sets of non-inverting bidirectional tri-state drivers for the bus data bits, four non-inverting unidirectional drivers for I/O port control, and necessary control logic. The control logic is required to maintain the proper directional transfer of bus data as dictated by the states of the I/O port control signals and the currently enabled I/O port. Each bus expander is programmed during manufacturing to respond to a specific block of I/O port addresses. Only I/O ports with addresses in the range of a given bus expander may be connected to that expander. A bus expander may be used on either left bank or right bank. Multiple expanders on the same bank must have different address ranges; however, expanders with the same address range can be connected if they are on different banks. Systems may be configured with I/O ports connected directly to the 8X300, as well as I/O ports connected through a bus expander; however, no unbuffered I/O port may have an address within the span of a bus expander on the same bank.

Addition of bus expanders may impact system cycle time due to the added delay in the data path. For the purposes of calculating allowable cycle time as described in the 8X300 data sheet, the bus expander delays may be considered additive to the I/O port delays so that a buffered I/O port simply appears as a slower I/O port.

PIN CONFIGURATION



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
2-7,9,10	DO0-DO7	I/O port data bus	Active low, three-state
11	WC(OUT)	Write command output	Active high
12	SC(OUT)	Select command output	Active high
13	MCLK(OUT)	Master clock output	Acitve high
14	$\overline{ME}$(OUT)	Master enable output	Active low
15	$\overline{ME}$(IN)	Master enable input	Active low
16	MCLK(IN)	Master clock input	Active high
17	SC(IN)	Select command output	Active high
18	WC(IN)	Write command output	Active high
19,20,22-27	DI0-DI7	Microprocessor data bus	Active low, three-state
1,8,21	GND	Ground	
28	V_{CC}	+5 volt supply	

PART TYPE	ADDRESS PATTERN MSB(0) LSB(7)	ADDRESS BLOCKS Octal
8T39-00	0000XXXX	0-17
8T39-01	0001XXXX	20-37, 40-57, 100-117, 200-217
8T39-03	0011XXXX	60-77, 120-137, 220-237, 140-157, 240-257, 300-317
8T39-07	0111XXXX	160-177, 260-277, 320-337, 340-357
8T39-17	1111XXXX	360-377

Table 1 8T39 ADDRESSING SUMMARY

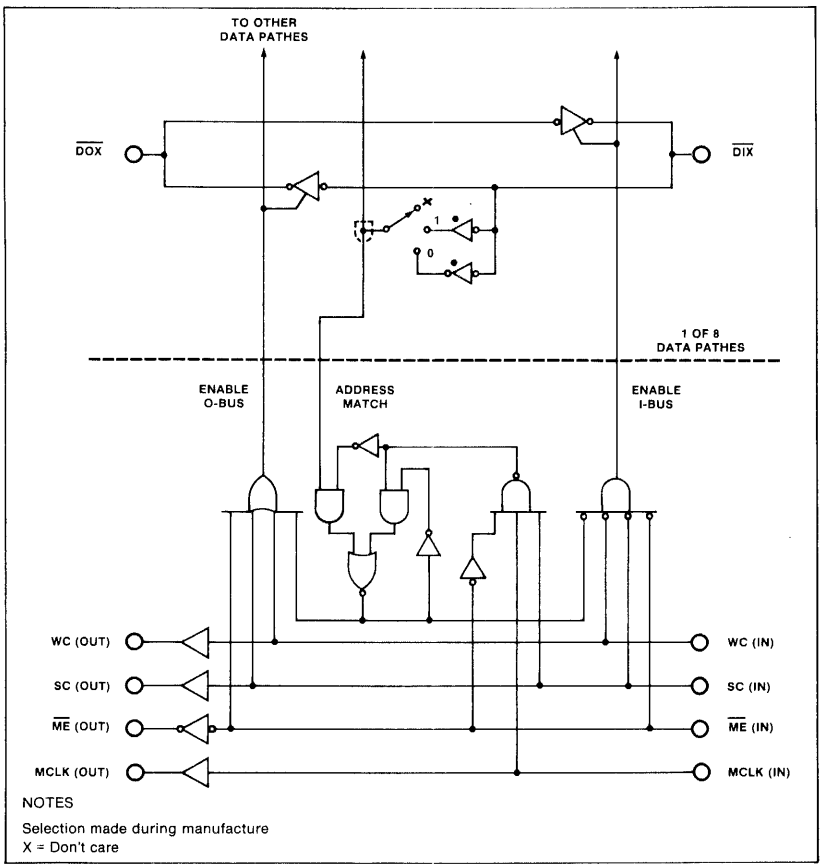
TRUTH TABLE

$\overline{ME}$	SC	WC	MCLK	SELECT LATCH	DATA TRANSFER DIRECTION	ADDRESS* COMPARISON
L	L	L	X	Set	DI Bus ← DO Bus	No
L	L	L	X	Not set	DI Bus → DO Bus	No
L	L	H	X	X	DI Bus → DO Bus	No
L	H	X	L	X	DI Bus → DO Bus	No
L	H	X	H	X	DI Bus → DO Bus	Yes
H	X	X	X	X	DI Bus - DO Bus	No

NOTES

*When an address comparison is made, the select latch is set if the data on the DI Bus is within the manufactured address range of the IV Bus Expander. Otherwise, the select latch is cleared.

FUNCTIONAL BLOCK DIAGRAM



NOTES

Selection made during manufacture

X = Don't care

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

ORDERING INFORMATION

The Bus Expander is ordered by specifying the following part number:

N8T39-XX P

- P = { I - Ceramic Package; XL - Epoxy Package }
- Address Range As Determined From Table 1

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage					V
V_{IL}	Low				.8	
V_{IH}	High	-5mA at V_{CC} min	2.0			
V_{IC}	Clamp				-1	
	Output voltage	V_{CC} = 4.75V				V
V_{OL}	Low	I_{OL} = 16mA			.55	
V_{OH}	High	I_{OH} = -3.2mA	2.4			
	Input current	V_{CC} = 5.25V				uA
I_{IL}	Low*	V_{IL} = .5V			-250	
I_{IH}	High*	V_{IH} = 5.25V		< 10	100	
I_{OS}	Short circuit output current	V_{CC} = 4.75V	-40			mA
I_{CC}	Supply current	V_{CC} = 5.25V			200	mA

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C, C_L[1] = 300pF[2]

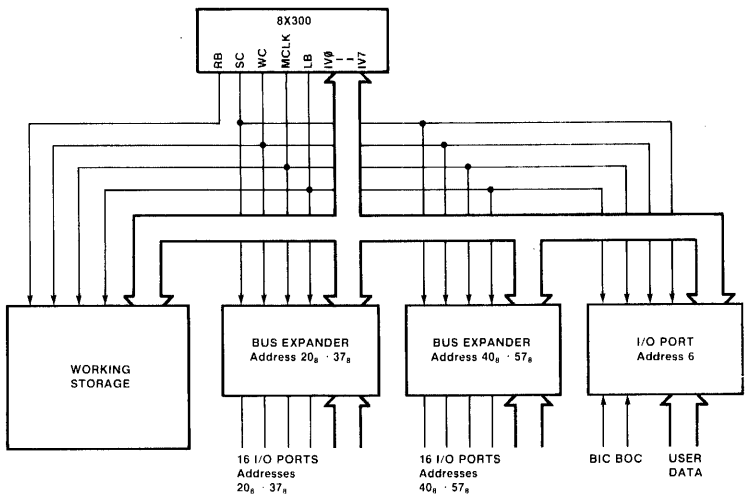
PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_{pd}	Propagation Delay Data	DOX DIX	DIX DOX				15	ns
t_{pd}	Control Propagation Delay	$\overline{ME}$ (out) MCLK (out) SC (out) WC (out)	$\overline{ME}$ (in) MCLK (in) SC (in) WC (in)				15	
t_{oe}	Data Output Enable	DIX DOX	$\overline{ME}$ (in) SC (in) WC (in)		28		56	ns
t_{od}	Data Output Disable	DIX DOX	$\overline{ME}$ (in) SC (in) WC (in)		15			ns
t_{setup}	Adverse Setup Time[3]	DIX DOX	DIX $\overline{ME}$ (in) MCLK (in) SC (in) WC (in)		54			ns
t_{hold}	Address Hold Time[3]	DIX DOX	DIX $\overline{ME}$ (in) MCLK (in) SC (in) WC (in)		3			ns

NOTES

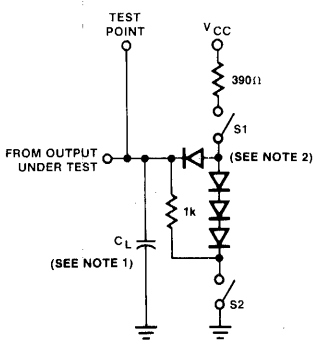
1. Includes tri-state leakage.
2. Minimum clock width ≈ 50ns.
3. All set up and hold times are referenced to the trailing edge of the clocking input MCLK.

TYPICAL APPLICATIONS

USING 2 BUS EXPANDERS TO GIVE 33 I/O PORTS PLUS WORKING STORAGE



TEST LOAD CIRCUIT



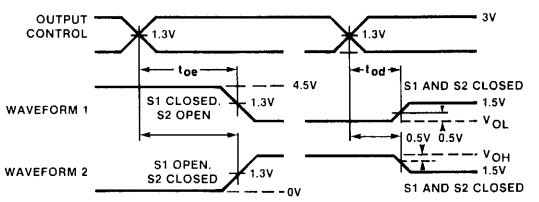
All resistors values are typical and in ohms.

NOTES

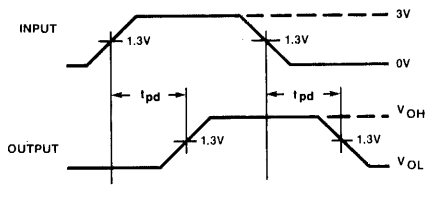
1. C_L includes probe and jig capacitance.
2. All diodes are 1N916 or 1N3064.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TO THREE-STATE OUTPUTS



PROPAGATION DELAY TIMES



PRELIMINARY SPECIFICATION
Manufacturer reserves the right to make design changes and improvements.

DESCRIPTION

The Bus Expander is specifically designed to increase the I/O capability of 8X300 systems previously limited by fanout considerations. The bus expander serves as a buffer between the 8X300 and blocks of I/O devices. Each bus expander can buffer a block of 16 I/O ports while only adding a single load to the 8X300.

FEATURES

- **15ns max propagation delay**
- **Bidirectional**
- **Three-state outputs on both ports**

FUNCTIONAL DESCRIPTION

The Bus Expander contains eight sets of non-inverting bidirectional tri-state drivers for the bus data bits, four non-inverting undirectional drivers for I/O port control, and necessary control logic. The control logic is required to maintain the proper directional transfer of bus data as dictated by the states of the I/O port control signals. A bus expander may be used on either left bank or right bank. Systems may be configured with I/O ports connected directly to the 8X300, as well as I/O ports connected through a bus expander.

Addition of bus expanders may impact system cycle time due to the added delay in the data path. For the purposes of calculating allowable cycle time as described in the 8X300 data sheet, the bus expander delays may be considered additive to the I/O port delays so that a buffered I/O port simply appears as a slower I/O port.

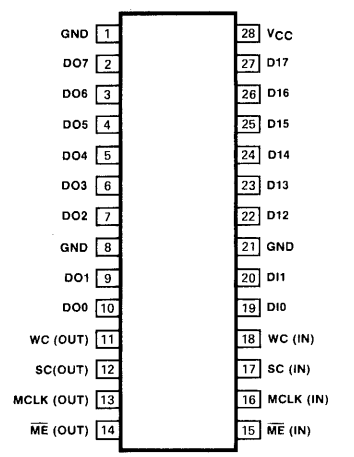
APPLICATIONS

The 8T39 Bus Expander is designed to be used with the 8X300 microprocessor to allow increased I/O capability in those systems previously limited by fanout considerations. Figure 1 shows a typical arrangement of the bus expander in an 8X300 system. Other I/O ports or working storage may be directly connected to the bus as shown.

The bus expander is not limited to use with the 8X300, but may be applied in any system which uses a combined address/data bus.

PIN CONFIGURATION

I,XL PACKAGE



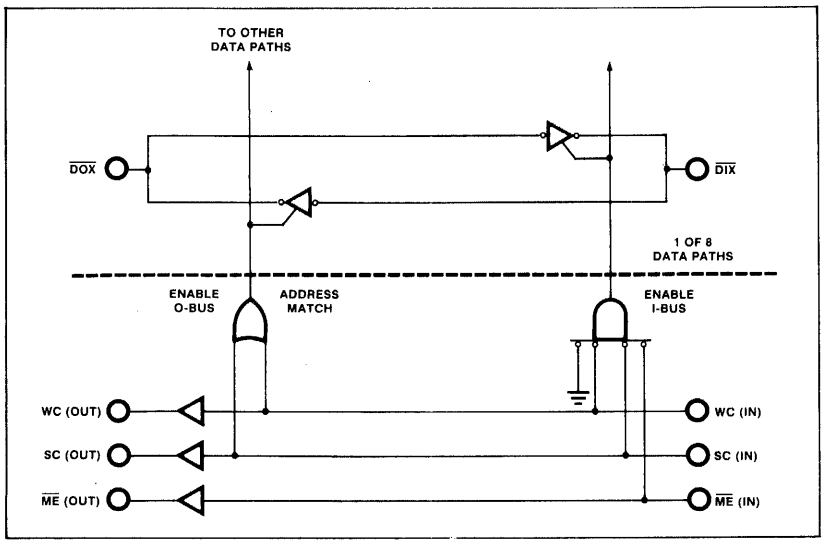
TRUTH TABLE

$\overline{ME}$	SC	WC	DATA TRANSFER DIRECTION	ADDRESS COMPARISON
L	L	L	DI Bus ← DO Bus	No
L	L	H	DI Bus → DO Bus	No
L	H	X	DI Bus → DO Bus	No
H	X	X	DI Bus → DO Bus	No

PIN DESIGNATION

PIN NO.	SYMBOL	NAME & FUNCTION	TYPE
2-7,9,10	DO0-DO7	I/O port data bus	Active low, three-state
11	WC(OUT)	Write command output	Active high
12	SC(OUT)	Select command output	Active high
13	MCLK(OUT)	Master clock input	Active high
14	$\overline{ME}$(OUT)	Master enable output	Active low
15	$\overline{ME}$(IN)	Master enable input	Active low
16	MCLK(IN)	Master clock input	Active high
17	SC(IN)	Select command output	Active high
18	WC(IN)	Write command output	Active high
19,20,22-27	DI0-DI7	Microprocessor data bus	Active low, three-state
1,8,21	GND	Ground	
28	V_{CC}	+5 volt supply	

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE Includes tri-state leakage.

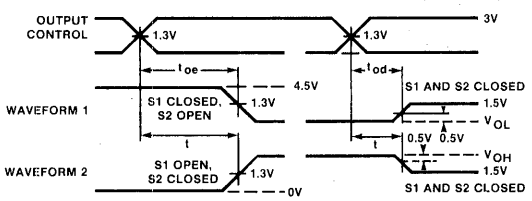
AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C, C_L = 300pF

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{pd}	Path delay Data	DOX DIX	DIX DOX				15	ns
t_{pd}	Control	$\overline{ME}$(OUT) MCLK(OUT) SC(OUT) WC(OUT)	$\overline{ME}$(IN) MCLK(IN) SC(IN) WC(IN)				15	ns
t_{oe}	Data Output Enable	DIX DOX	$\overline{ME}$(IN) SC(IN) WC(IN)		28		56	ns
t_{od}	Data Output Disable	DIX DOX	$\overline{ME}$(IN) SC(IN) WC(IN)		15			

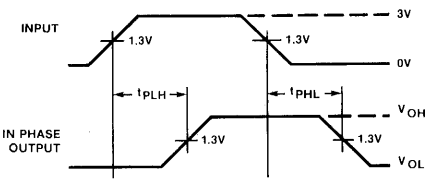
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low				.8	
V_{IH}	High		2.0			
V_{IC}	Clamp	-5mA at V_{CC} min			-1	
	Output voltage	V_{CC} = 4.75V				V
V_{OL}	Low	I_{OL} = 50mA			.55	
V_{OH}	High	I_{OH} = -3.2mA	2.4			
	Input current	V_{CC} = 5.25V				μA
I_{IL}	Low[1]	V_{IL} = .5V			-250	
I_{IH}	High[1]	V_{IH} = 5.25V		<10	100	
I_{OS}	Short circuit output current	V_{CC} = 4.75V	-40			mA
I_{CC}	Supply current	V_{CC} = 5.25V			200	mA

VOLTAGE WAVEFORMS

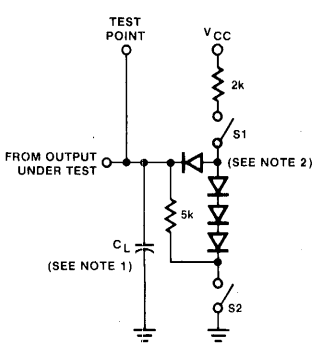
PROPAGATION DELAY TO THREE-STATE OUTPUTS



PROPAGATION DELAY TIMES



TEST LOAD CIRCUIT



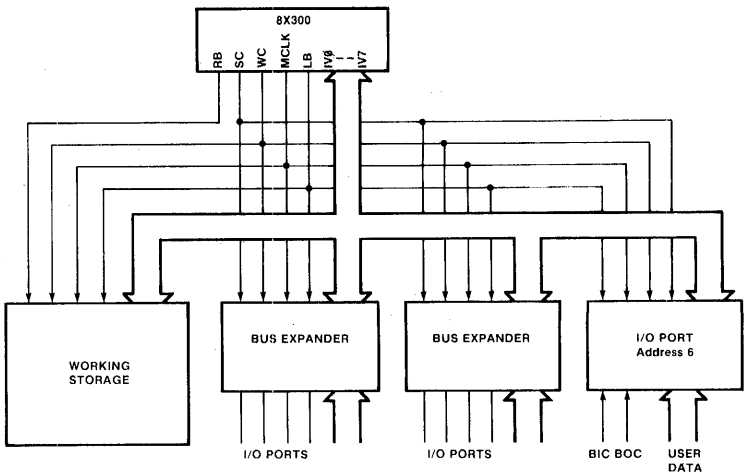
All resistors values are typical and in ohms.

NOTES

1. C_L includes probe and jig capacitance.
2. All diodes are 1N916 or 1N3064.

TYPICAL APPLICATION

USING 2 BUS EXPANDERS TO CREATE 33 I/O PORTS PLUS WORKING STORAGE



DESCRIPTION

The CRC Generator/Checker circuit is used to provide an error detection capability for serial digital data handling system. The serial data stream is divided by a selected polynomial and the division remainder is transmitted at the end of the data stream, as a Cyclic Redundancy check character (CRCC). When the data is received, the same calculation is performed. If the received message is error-free, the calculated remainder should satisfy a predetermined pattern. In most cases, the remainder is zero except in the case where Synchronous Data Link Control type protocols are used whereby the correct remainder is checked for 1111000010111000 ($x^0 - x^{15}$).

8 polynomials are provided and can be selected via a 3-bit control bus. Popular polynomials such as CRC-16 and CCITT are implemented. Polynomials can be programmed to start with either all zeros or all ones.

Automatic right justification for polynomials of degree less than 16 is provided.

FUNCTIONAL DESCRIPTION

The CRC Generator/Checker circuit provides a means of detecting errors in a serial data communications environment. A binary message can be interpreted as a binary polynomial H(x). This polynomial can be divided by a generator polynomial P(x) such that H(x) = P(x) Q(x) + R(x) whereby Q(x) is the quotient and P(x) is the remainder. During transmission, the remainder is appended to the end of the message as check bits. For a given message, a unique remainder is generated. Hardware implementation of division is simply a feedback shift register with Exclusive-OR gating. Subtraction and addition in modulo 2 is implemented by the Exclusive-OR function. The number of shift register stages is equal to the degree of the divisor polynomial.

Table 1 shows the polynomials implemented in the CRC circuit. Each polynomial can be selected via the 3-bit polynomial control inputs S_0, S_1 and S_2. To generate the check bits, the data stream is entered via the Data (D) input, using the high to low transition of the Clock (CP) input. This data is gated with the most significant output (Q) of the register, and controls the exclusive OR gates. The Check Word Enable (CWE) must be held high while the data is being entered. After the last data bit is entered, the CWE is brought low and the check bits are shifted out of the register and appended to the data bits using external gating.

FEATURES

- **I^2L technology**
- **TTL inputs/outputs**
- **10MHz (max) data rate**
- **Total power dissipation = 175mw (max)**
- **V_{CC} = 5.0V**
- **V_{JJ} = 1.0V**
- **Separate preset and reset controls**
- **SDLC specified pattern match**
- **Automatic right justification**

TYPICAL APPLICATIONS

- **Floppy and other disc systems**
- **Digital cassette and cartridge systems**
- **Data communication systems**

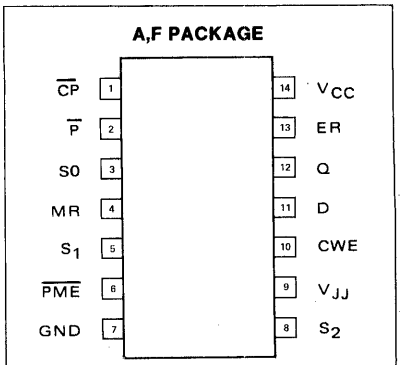
To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held high. The 8X01 is not in the data path, but only monitors the message. The Error output becomes valid after the last check bit has been entered into the 8X01 by a high to low transition of CP. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all low and the Error output (ER) is low. If a detectable error has occurred, ER is high. ER remains valid until the next high to low transition of CP or until the device has been preset or reset. PME must be high if ER output is used to reflect all zero result.

For data communications using the Synchronous Data Link Control protocol (SDLC), the 8X01 is first preset to all ones before any accumulation is done. This applies to both transmitter and receiver.

A special pattern of 1111000010111000 ($x^0 - x^{15}$) is used in place of all zeros during receiving for valid message check. PME is incorporated to select this option. If PME is low during the last bit time of the message, ER output is low if result matches this special pattern. When ER is high, error has occurred.

PIN CONFIGURATION

A,F PACKAGE



PIN DESIGNATION

PIN NO.	FUNCTION
S_0, S_1, S_2	Polynominal Select inputs
D	Data input
$\overline{CP}$	Clock (operates on high to low transition) input
CWE	Check Word Enable
$\overline{P}$	Preset (active low) input
MR	Master Reset (active high) input
Q	Data output
ER	Error (active high) output
$\overline{PME}$	Pattern match enable (active low)

A high level on the Master Reset (MR) input asynchronously clears the register. A low level on the Preset (P) input asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of the 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

For SDLC, the user must invert the check sum shifted out of the 8X01.

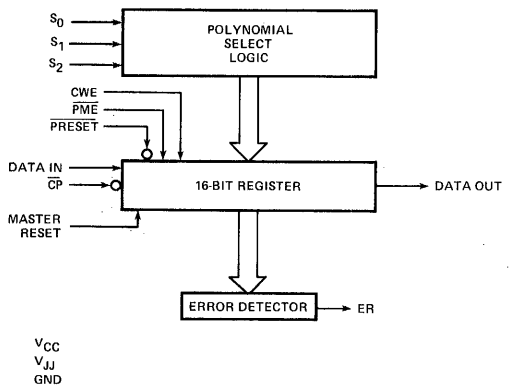
RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{JJ}	Supply current	40		100	mA
$\overline{CP}$	Clock input	0		5	MHz

TRUTH TABLE

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

LOGIC DIAGRAM

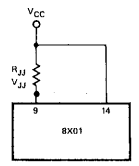


DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

(Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp diode voltage	V_{CC} = MIN, I_{IN} = -18mA			-1.5	V
V_{OH}	Output high voltage	V_{CC} = MIN, I_{OH} = -400μA, I_{JJ} = MIN	2.7			V
V_{OL}	Output low voltage	V_{CC} = MIN, I_{OL} = 8mA, I_{JJ} = MIN			0.5	V
I_{IL}	Input low current	V_{CC} = MAX, V_{IN} = 0.4V			-0.36	mA
I_{IH}	Input high current	V_{CC} = MAX, V_{IN} = 2.7V			20	μA
I_{IH}	Max. input current	V_{CC} = MAX			0.1	mA
I_{OS}	Output short circuit current	V_{CC} = MAX, V_{OUT} = OV, I_{JJ} = MIN	-10		-42	mA
I_{CC}	Supply current	V_{CC} = MAX, inputs open	10		18	mA
I_{JJ}	Injection current	V_{CC} = MAX, inputs open	60		100	mA

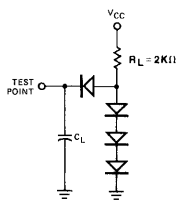
I^2L INJECTOR CURRENT SOURCE



$$R_{JJ} = \frac{V_{CC} - V_{JJ}}{I_{jj}} = \frac{(5.0 - 0.8)\ V}{60mA}$$

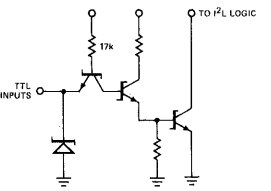
$$= \frac{4.20V}{60mA} = 70\Omega$$

TEST CIRCUIT

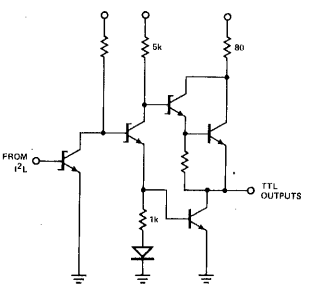


INPUT/OUTPUT CIRCUITS

INPUT STRUCTURE



OUTPUT STRUCTURE

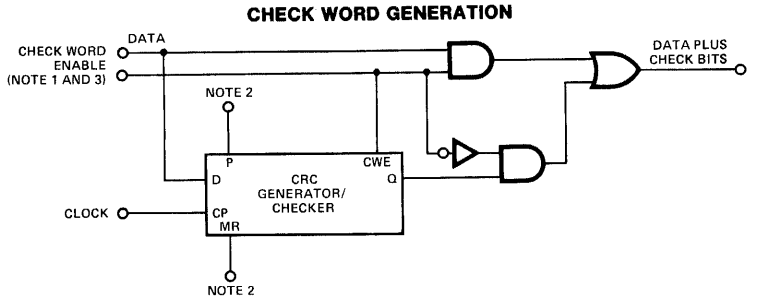


NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
f_{max}	Maximum clock frequency				5	7		MHz
	Pulse width							ns
$t_W CP(L)$	Clock low			See Figure 2	100			
$t_W P(L)$	Preset low			See Figure 3	120			
$t_W MR(H)$	Master reset high			See Figure 4	150			
	Setup and hold time							ns
$t_S D$	Setup time	Clock	Data	See Figure 5		120	150	
$t_S CWE$	Setup time	Clock	CWE			75	100	
t_n	Hold time	Clock	Data, CWE		0	-30	0	
	Propagation delay							ns
t_{PLH}	Low to high	Data output	Clock, preset	See Figures 1,2,3		100	160	
t_{PHL}	High to low							
t_{PLH}	Low to high	Data output	MR	See Figure 4		75	100	
t_{PHL}	High to low							
t_{PLH}	Low to high	Error output	Clock, MR, preset	See Figures 2,3,4		150	200	
t_{PHL}	High to low							
t_{REC}	Recovery time	Clock	MR, preset	See Figures 3,4		60	90	ns

CHECK WORD GENERATION



NOTES
1. Check word Enable is High while data is being clocked, Low during transmission of check bits.
2. 8X01 must be reset or preset before each computation
3. CRC check bits are generated and appended to data bits.

Figure 1

VOLTAGE WAVEFORMS

PROPAGATION DELAYS $\overline{CP}$ TO Q AND $\overline{CP}$ TO ER

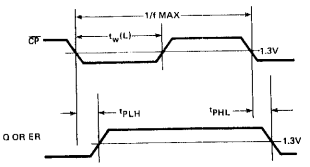


Figure 2

PROPAGATION DELAYS, $\overline{P}$ TO Q AND ER PLUS RECOVERY TIME P TO $\overline{CP}$

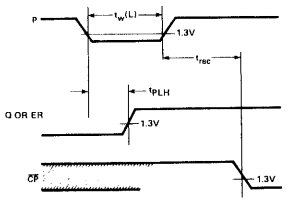


Figure 3

PROPAGATION DELAYS, MR TO Q AND ER PLUS RECOVERY TIME, MR TO $\overline{CP}$

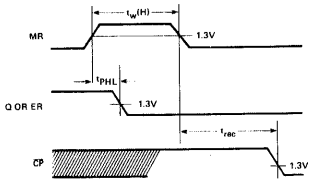


Figure 4

SET UP AND HOLD TIMES D TO $\overline{CP}$ and CWE TO $\overline{CP}$

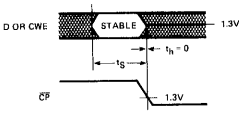


Figure 5

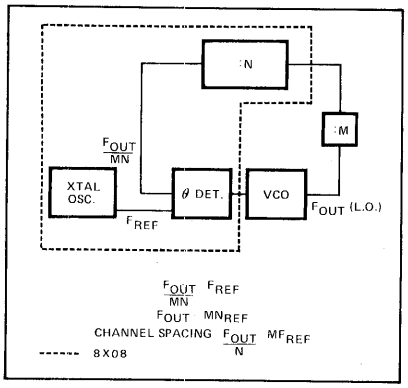
DESCRIPTION

This LSI integrated circuit performs the digital control functions required for generating AM/FM radio frequency local oscillator signals using digital phase locked loop techniques. By the use of low power Schottky and ECL technologies on the same substrate it is possible to operate at 80MHz input frequencies with an average system power of 1.6mW per gate typical.

FEATURES

- **80MHz input frequency**
- **ECL prescaler**
- **LS process**
- **Single 5V supply**
- **Power dissipation—600mW (max)**
- **External components—**
  - **1 crystal**
  - **2 capacitors**

PHASE LOCKED LOOP BLOCK DIAGRAM



PHASE LOCKED LOOP PRINCIPLES

Digital phase locked loops are comprised of 4 basic building blocks: A fixed reference frequency generator (crystal oscillator and divider), a phase comparator, a voltage controlled oscillator (VCO) and a programable counter (÷N).

In cases where very high frequencies must be generated, a fixed prescaler (÷M) is employed to divide the local oscillator frequency down to a frequency compatible with the programmable counter. Fout from the VCO is divided down by the prescaler and programmable counters and compared to the reference frequency by the phase detector. If $\frac{Fout}{MN}$ is not equal to Fref in phase and frequency, the phase detector generates a signal which causes the VCO frequency to increase or decrease until Fref = $\frac{Fout}{MN}$. When this occurs, the local oscillator is essentially as stable as the crystal reference oscillator.

The local oscillator frequency (Fout) is changed by programming a different number into the programmable counter. The distance between discrete frequencies or the channel spacing is determined by the reference frequency.

For the AM/FM circuit, up to 200 channels are possible with selectable channel spacing of 10kHz for AM operation and 2000 channels at 100kHz for FM operation.

AM/FM Frequency Synthesizer Circuit Description

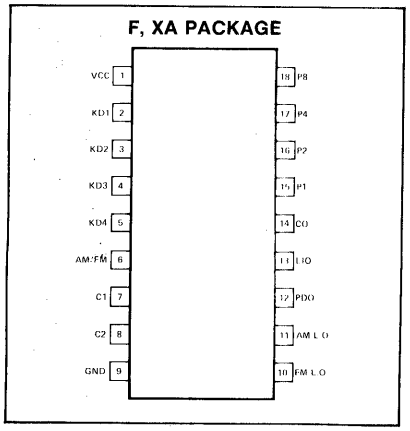
The frequency synthesizer circuit logic diagram is shown below. Following is a description of each of the major blocks.

Programmable Counter

The programmable counter consists of 3 stages of decade counter plus a divide by 1 or 0 counter to divide by numbers up to 1999. BCD programming data is presented to the dividers in parallel form, one digit at a time. Parallel data is strobed into internal latches via strobe signals; one strobe for each digit. A ÷ 5 80MHz ECL prescaler precedes the programmable counter for FM operation. This prescaler plus an external 160MHz ÷ 2 flip-flop provide a ÷ 10 160MHz prescaler (÷M) function to scale the programmable counter input frequency down to 16MHz maximum. A logic control circuit bypasses the ÷M prescaler and the first decade counter for AM operation. By this technique, the channel spacing is programmable to 10kHz for AM operation and 100kHz for FM operation.

PIN CONFIGURATION

F, XA PACKAGE



VCO

An externally provided integrator and voltage controlled oscillator must be provided to perform the complete frequency synthesizer function. The integrator converts the pulses that come from the phase detector into a dc signal that controls the output frequency of the voltage controlled oscillator. It is in the integrator part of the circuit that the critical loop constants are determined. The voltage controlled oscillator is normally a LC tuned oscillator with varactor diode tuning that is controlled by the dc signals from the integrator. In this case, two are required, one for the AM band and one for the FM band. The FM oscillator output must be +5V ECL compatible while the AM oscillator must be TTL compatible.

RECOMMENDED OPERATING CONDITIONS

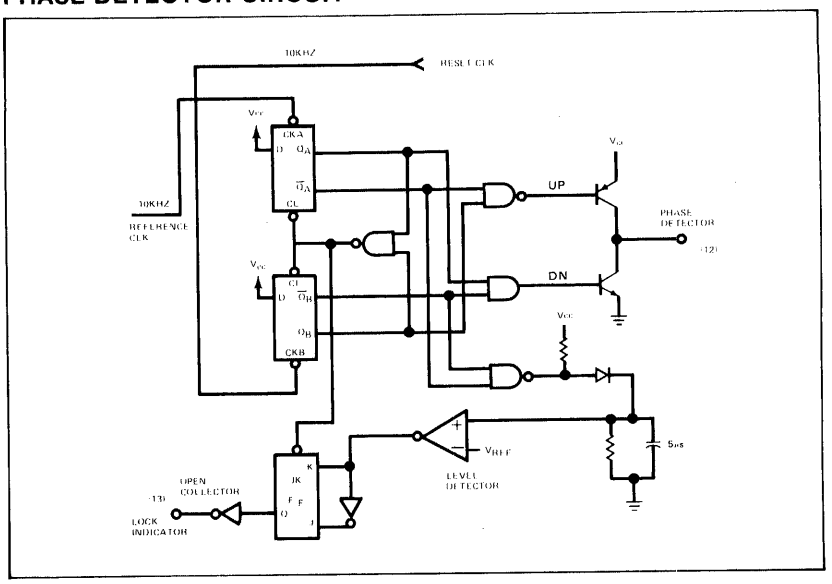
PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_A	Operating free air temperature	-40		+85	°C
V_{CC}	Supply voltage	4.75	5.0	5.25	V
	Max input voltage data, strobe			16	V
	Max AM local oscillator input operating frequency (Pin 11)		20		MHz
	Max FM local oscillator input operating frequency (Pin 10)		100	80	MHz
	Maximum reference frequency oscillator operating frequency		6		MHz

Phase Detector Circuit

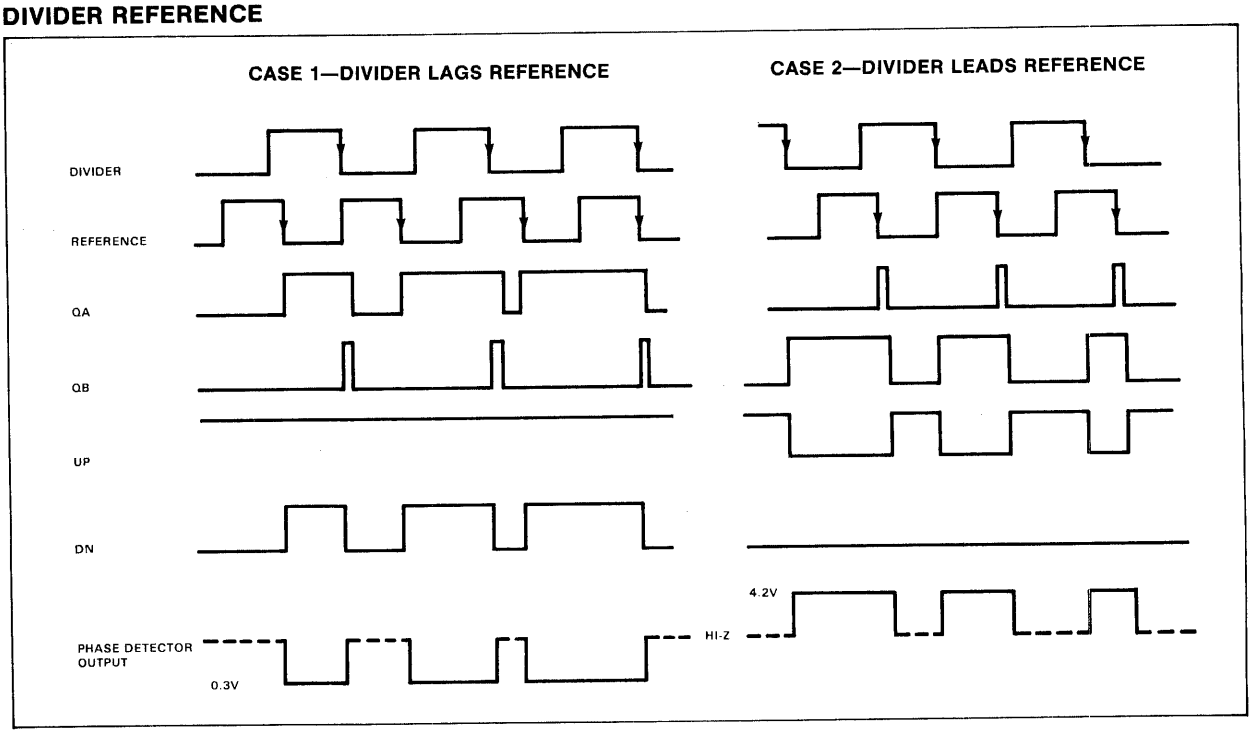
The phase detector is a digital edge-detecting device that provides an output three-state signal that is in a high impedance state when the 2 input signals are equal in phase and/or frequency. The output of the phase detector is a series of pulses that swing from the high impedance state to .3V typical or from the high impedance state to 4.2V typical. If the positive edge of the divider input leads the reference, the pulses will go to 4.2V. If it lags they will go to .3V.

The width of the output pulses is a function of the time between the positive edges (phase) of the 2 signals. An example of the operation of the device is shown where the reference signal is twice the frequency of the divider signal and has a phase lead of 270°. The output pulses are converted to a dc signal by integrating amplifiers causing the output frequency of the voltage controlled oscillator to increase or decrease (increase in this case) until the divider output and the reference output are equal in phase and frequency.

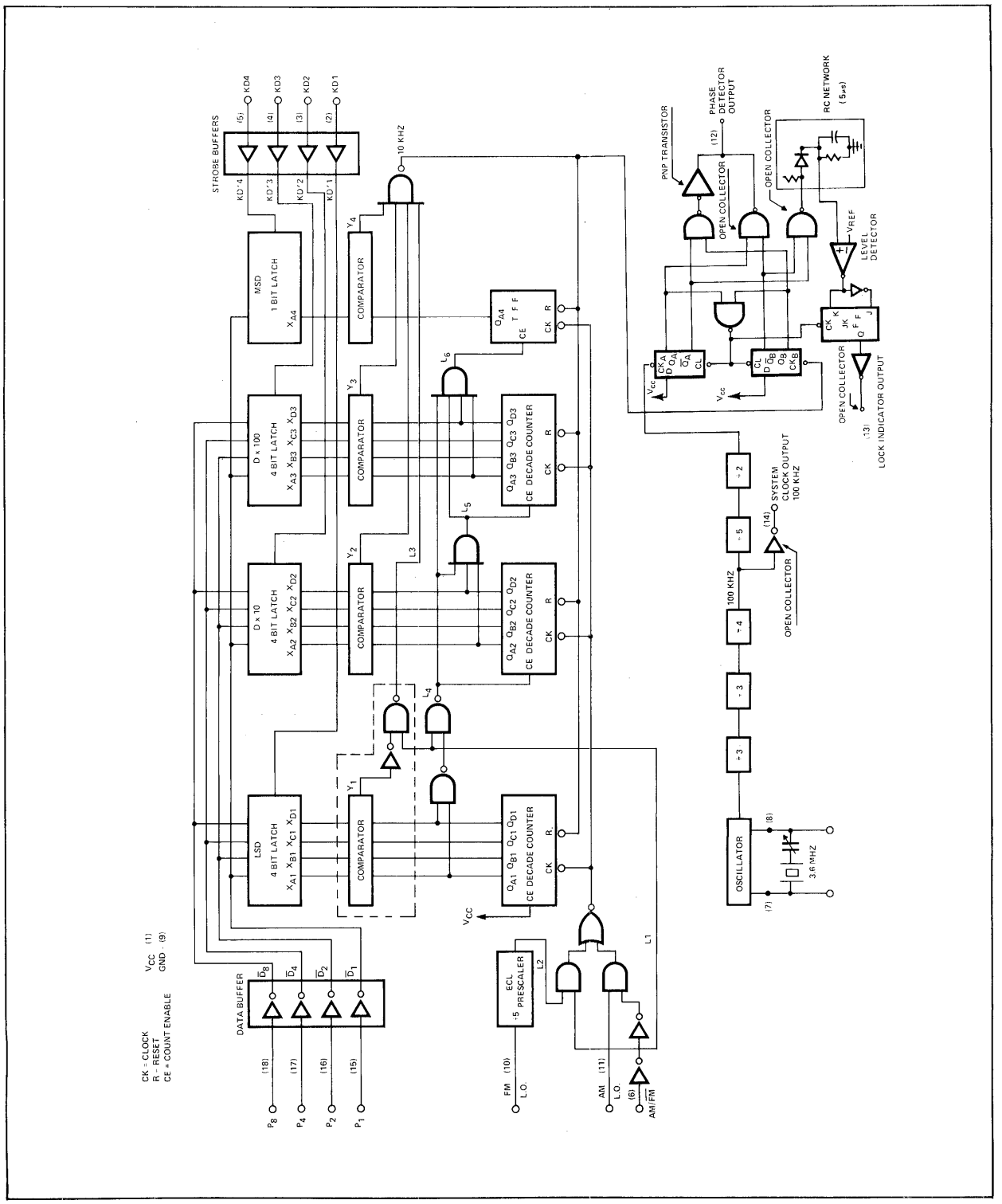
PHASE DETECTOR CIRCUIT



DIVIDER REFERENCE



LOGIC DIAGRAM



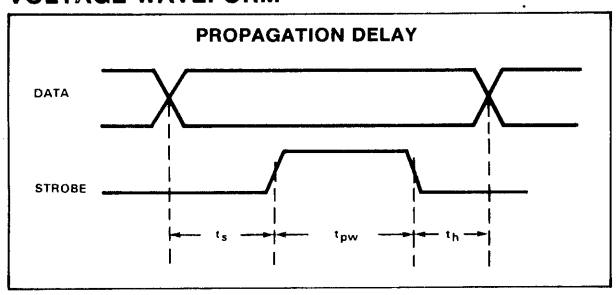
DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{IH}	High level input voltage					
	P, K_D, AM/$\overline{FM}$ inputs		5.25			V
	AM L.O. input		2			V
	FM L.O. input		4.1		5.25	V
V_{IL}	Low level input voltage					
	P, K_D, AM/$\overline{FM}$ inputs				3.75	V
	AM L.O. input				0.8	V
	FM L.O. input				3.3	V
I_{IH}	High level input current					
	P, K_D, AM/$\overline{FM}$ inputs	V_{CC} = max, V_I = 16V			200	μA
		V_{CC} = max, V_I = 5.25V			40	μA
	AM L.O. input					
	(with 5kΩ pullup to V_{CC})	V_{CC} = max, V_I = 5.25V			200	μA
	FM L.O. input	V_{CC} = max, V_I = 5.25V			400	μA
I_{IL}	Low level inputs current					
	P, K_D, AM/$\overline{FM}$ inputs	V_{CC} = max, V_I = 3.75V			-40	μA
	AM L.O. input					
	(with 5kΩ pullup to V_{CC})	V_{CC} = max, V_I = 0.4V	-.7		-1.6	mA
	FM L.O. input	V_{CC} = max, V_I = 0.4V			-40	μA
V_{OL}	Low level output voltage					
	System clock output	V_{CC} = min, I_{OL} = 16mA			0.8	V
	Lock indicator output	V_{CC} = min, I_{OL} = 16mA			0.8	V
	Phase detector output	V_{CC} = min, I_{OL} = 40μA			0.5	V
V_{OH}	High level output voltage					
	Phase detector output	V_{CC} = min, I_{OH} = -40μA	V_{CC} -0.5V			
I_{OL}	High level output current					
	System clock output	V_{CC} = min, V_{OH} = 16V			250	μA
	Lock indicator output	V_{CC} = min, V_{OH} = 16V			250	μA
I_{CC}	Supply current	V_{CC} = max			150	mA

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Strobe pulse width			200	100		ns
	Setup and hold time						ns
t_s	Logic high	Strobe	Data	150			
	Logic low			50			
t_h	Logic high	Strobe	Data	40			
	Logic low			0			

VOLTAGE WAVEFORM



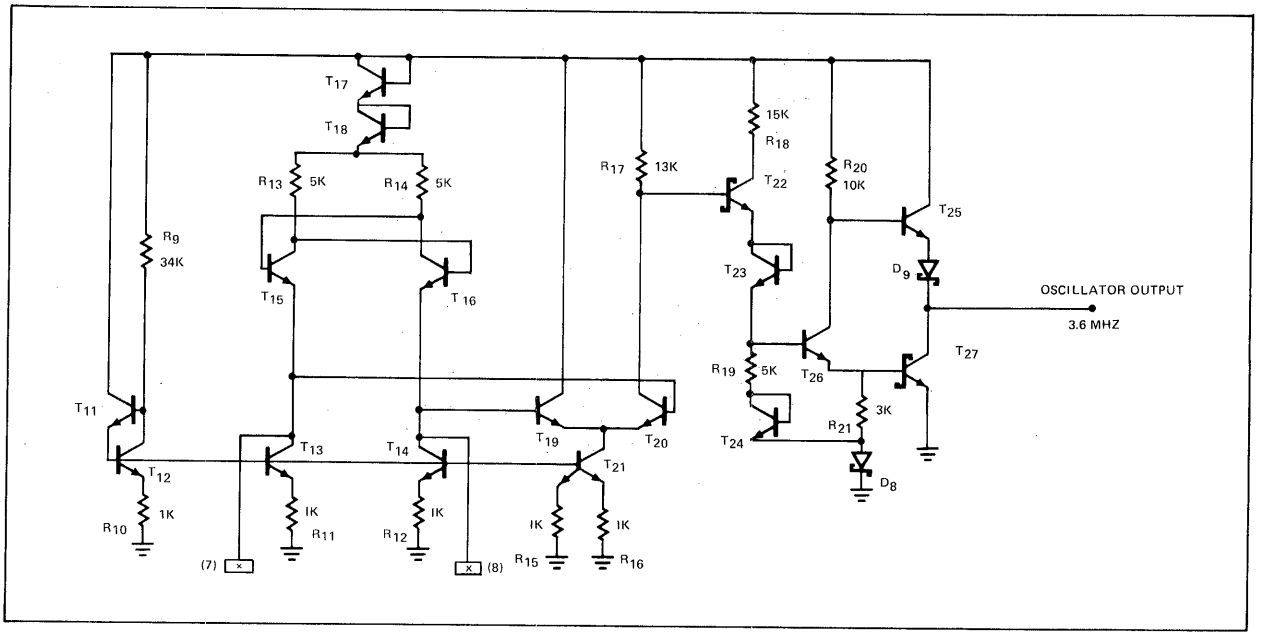
Crystal Oscillator Circuit

In this circuit, the cross-coupled transistor pair form a bistable circuit. The crystal provides positive feedback between the emitters of T_{15} and T_{16} which causes the circuit to oscillate at the crystal frequency.

Recommended Crystal Characteristics

Type	Fundamental Mode Series Resonant
Series resistance	< 100 Ω

CRYSTAL OSCILLATOR CIRCUIT



DESCRIPTION

The Signetics Series 3000 Bipolar Microprocessor Chip Set provides new levels of high performance to microprocessor applications not previously possible with MOS technology. Combining the Schottky bipolar N3001 Microprogram Control Unit (MCU) and N3002 Central Processing Element (CPE) with industry standard memory and support circuits microinstruction cycle times of 100ns are possible.

In the majority of cases, the choice of a bipolar microprocessor slice, as opposed to an MOS device, is based on speed or flexibility of microprogramming. Starting with these characteristics, the design of the Signetics Series 3000 Microprocessor has been optimized around the following objectives:

- Fast cycle time
- All memory and support chips are industry standard
- Cooler operation
- Lower total system cost

Systems built with large-scale integrated circuits are much smaller and require less power than equivalent systems using medium and/or small scale integrated circuits.

The 2 components of the Series 3000 chip set, when combined with industry standard memory and peripheral circuits, allows the design engineer to construct high-performance processors and/or controllers with a minimum amount of auxiliary logic. Features such as the multiple independent address and data buses, tri-state logic, and separate output enable lines eliminate the need for time-multiplexing of buses and associated hardware.

Each Central Processing Element represents a complete 2-bit slice through the data processing section of a computer. Several CPEs may be connected in parallel to form a processor of any desired word length. The Microprogram Control Unit controls the sequence in which microinstructions are fetched from the microprogram memory (ROM/PROM), with these microinstructions controlling the step-by-step operation of the processor.

Each CPE contains a 2-bit slice of 5 independent buses. Although they can be used in a variety of ways, typical connections are:

Input M-bus:	Carries data from external memory
Input I-bus:	Carries data from input/output device
Input K-bus:	Used for microprogram mask or literal (constant) value input
Output A-bus:	Connected to CPE Memory Address Register
Output D-bus:	Connected to CPE accumulator.

As the CPEs are paralleled together, all buses, data paths, and registers are correspondingly expanded.

The microfunction input bus (F-bus) controls the internal operation of the CPE, selecting both the operands and the operation to be executed upon them. The arithmetic logic unit (ALU), controlled by the microfunction decoder, is capable of over 40 Boolean and binary operations as outlined in the FUNCTION DESCRIPTION section of the N3002 data sheet. Standard carry look-ahead outputs (X and Y) are generated by the CPE for use with industry standard devices such as the 74S182.

FEATURES

- **Bipolar Schottky Technology**
- **Multiple Input/Output Bus Structure**
- **Fastest Microprocessor Available**
- **512 Microinstruction Addressibility**
- **Full Function Accumulator**

AVAILABILITY

Immediate delivery for Signetics Rep. or Distributors.

CONTENTS

1 ea—N3001 Microprogram Control Unit
4 ea—N3002 Central Processing Element
1 ea—74S182 Look-Ahead Carry
3 ea—82S114 256 × 8 PROM
1 ea—8T31 Bidirectional I/O Port
2 ea—8T26A Quad Bus Transceiver
1 ea—Introductory Manual

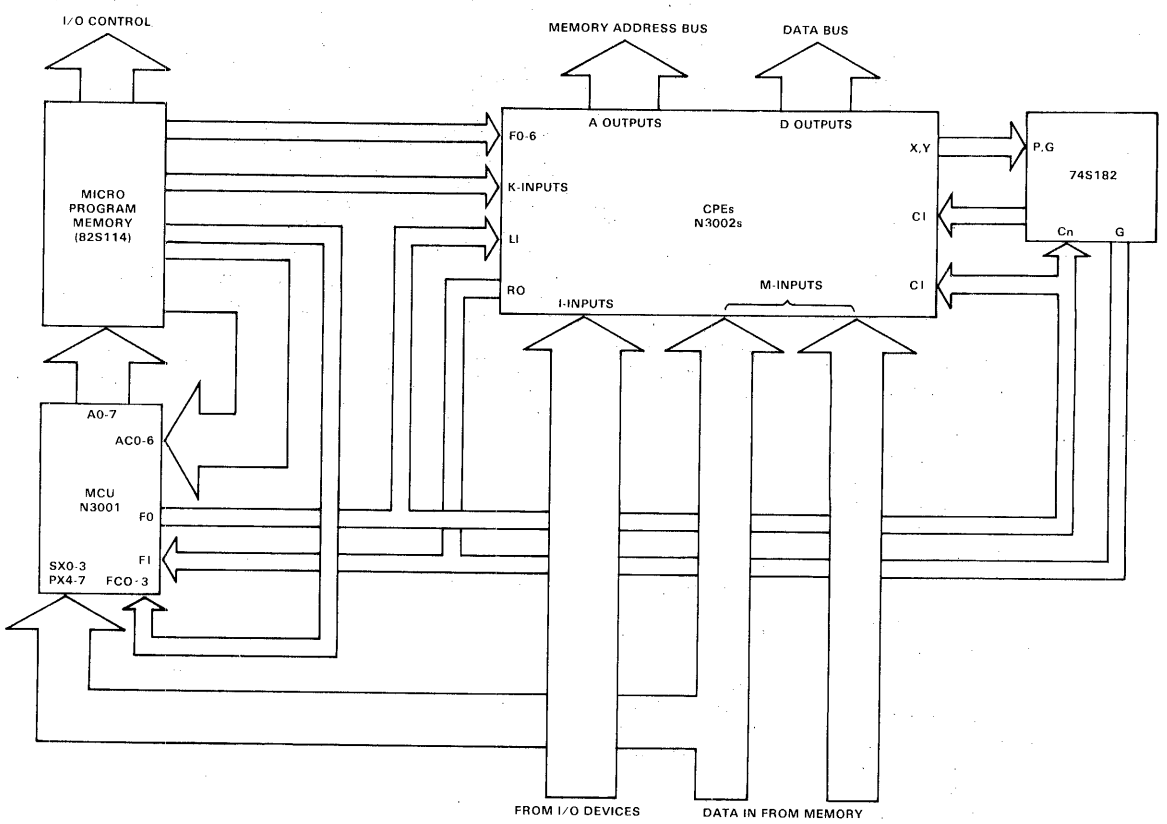


Figure 1

COMPATIBLE PRODUCTS

82S100, 82S101 FPLA

- Field programmable (Ni-Cr Link)
- Input variables—16
- Output functions—8
- Product terms—48
- Address access time—50ns
- Tri-state (82S100) or open collector (82S101) outputs
- 28-pin ceramic dip

82S115/123/129 PROMs

- Schottky TTL technology
- Single +5V power supply
- 32 × 8 organization (82S123)
- 256 × 8 organization (82S129)
- 512 × 8 organization (82S115)
- Field programmable (Nichrome)
- On-chip storage latches (82S115 only)
- Low current pnp inputs
- Tri-state outputs
- 35ns typical access time
- Standard 24-pin DIP (82S115)
- Standard 16-pin DIP (82S123, 82S129)

82S25/82S116/82S11 RAMs

- Schottky TTL technology
- 16 × 4 organization (82S25)
- 256 × 1 organization (82S116)
- 1024 × 1 organization (82S11)
- On-chip address decoding
- 16-pin ceramic dip

8T26A/8T28 Quad Transceiver

- Schottky TTL technology
- 4 pairs of bus drivers/receivers
- Separate drive and receive enable lines
- Tri-state outputs
- Low current pnp inputs
- High fan out-driver sinks 40mA
- 20ns maximum propagation delay
- Standard 16-pin DIP

8T31 8-Bit Bidirectional Port

- Schottky TTL technology
- 2 independent bidirectional buses
- 8-bit latch register
- Independent read, write controls for each bus
- Bus A overrides if a write conflict occurs
- Register can be addressed as a memory location
- via Bus B Master Enable
- 30ns maximum propagation delay
- Low input current: 500μA
- High fan out-sinks 20mA
- Standard 24-pin DIP

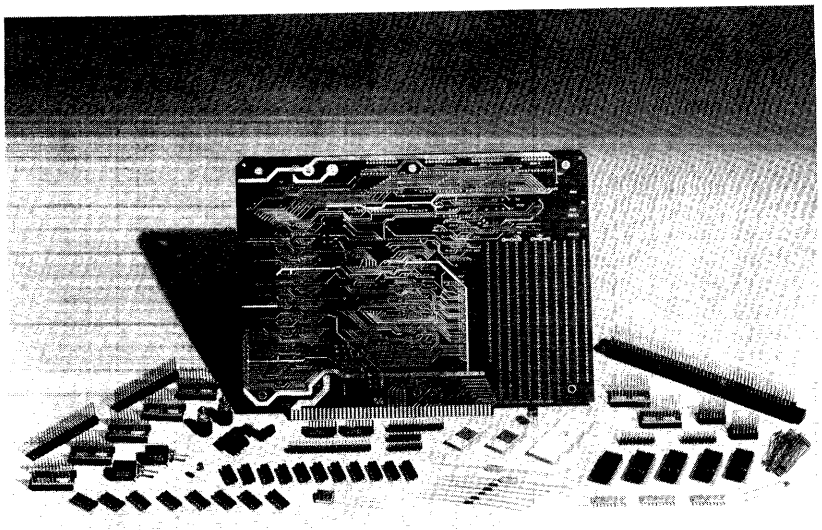
BIPOLAR EMULATION KIT FOR THE SERIES 3000 AN 8080 SYSTEM EMULATOR

3000KT8080SK

DESCRIPTION

The 8080 Emulation Kit is a microprogrammable microprocessor utilizing Schottky LSI components to implement an emulation of an Intel 8080A microcomputer system. The emulation is functionally equivalent to a microprocessor system incorporating the following Intel devices: 8080A, 8228, 8224 and 8212. The kit provides the standard address, data, status and control buses as defined in the Intel 8080 Microcomputer System Manual. Since the kit uses bipolar LSI elements, the emulator lacks the two-phase non-overlapping clock. Furthermore, those signals emanating from the 8080 during SYNC time are not provided, but rather the useful status signals provided by the 8228 system controller are implemented. The emulation also provides an extension of the 8228 operation during multi-byte interrupts. This is realized by allowing any 8080 program branch instruction to be inserted during interrupts rather than restricting multi-byte instructions to CALL during interrupts. Finally, a nonstandard status signal, RTRAP, is provided which indicates that the present instruction is a reserved or undefined instruction. After this indication, the processor will enter the normal HALT routine and await an interrupt. (Intel 8080A operation during undefined instructions is undefined.) Thus all 12 of the unused instructions in the 8080 instruction set are reserved for future instruction set expansion. These unused codes may be used at any time to extend the usual instruction set without requiring any reprogramming of the bipolar PROMs used for microprogram memory. Finally, the emulator is fully static so that the clock may be adjusted from a typical cycle time of 150ns to dc.

The kit contains all the parts necessary to construct the emulator and includes preprogrammed PROMs. The kit is designed to be assembled by a skilled technician in about 8 hours.



FEATURES

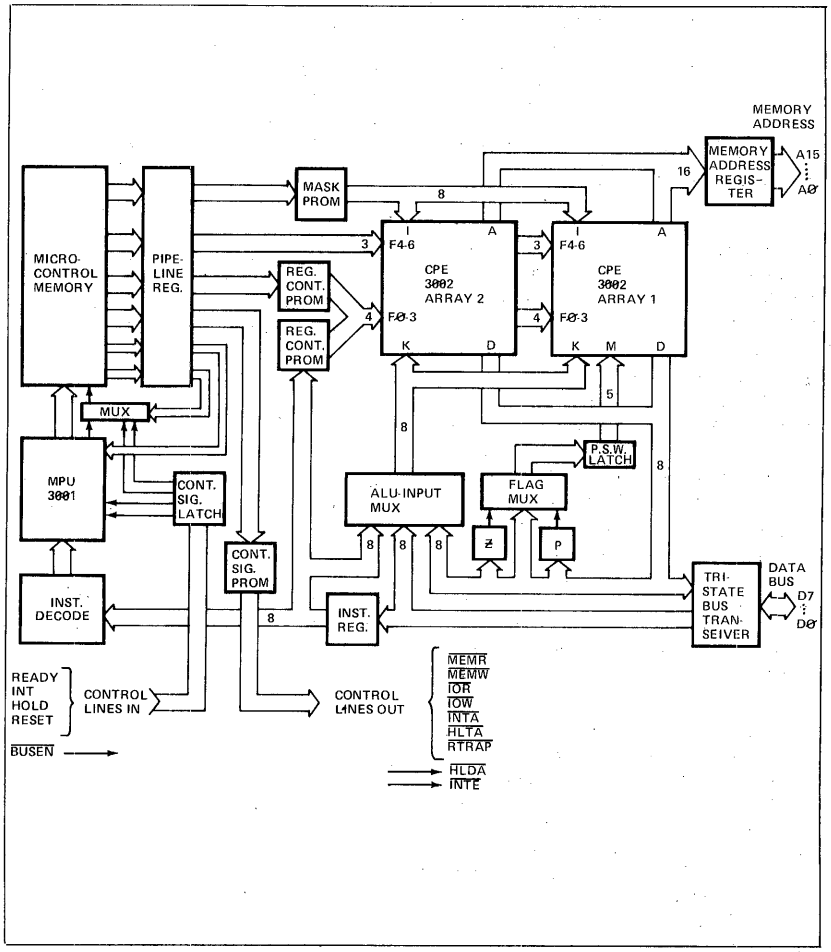
- **Full emulation of 8080A system**
- **Speed increase by factor of 2 to 9.2 over 8080A system**
- **Static operation; microcycle time dc to 150ns**
- **Operation from single +5V supply**
- **Executes all 8080 instructions**
- **Hardware multiply and divide**
- **Microprogram expandable**
- **Includes single phase clock**
- **Full vectored interrupt to any location within 64K memory**

Part Number: 3000KT8080SK
Availability: Immediate delivery from Signetics, Rep or Distributors

KIT CONTENTS

1 each	N74123
1 each	N3001
8 each	N3002
7 each	N82S115
1 each	N82S23
2 each	N82S123
2 each	N82S126
3 each	N8263
3 each	N74S182
1 each	N74S280
2 each	N7475
1 each	DM8613
11 each	N74S174
2 each	N8T28
3 each	N8T97
1 each	N74S153
2 each	N74S157
1 each	N7400
1 each	N74S02
3 each	N74S04
1 each	N74S08
1 each	N74S10
1 each	N74S133
2 each	Resistor networks 1K, 16-pin
1 each	P.C. board
1 each	Manual
1 each	Schematic
1 each	Set of microprogram listings
Plus:	Over 25 miscellaneous resistors, capacitors and other parts

BLOCK DIAGRAM



INSTRUCTION EXECUTION TIMES (150ns microinstruction cycle time, 150ns RAM access time)

INSTRUCTION	CY-CLES	EXECUTION TIME (μs)
LXI	7	1.05
PUSH	9	1.35
PUSH PSW	9	1.35
POP	9	1.35
POP PSW	8	1.20
STA	9	1.35
LDA	8	1.20
XCHG	7	1.05
XTHL	13	1.95
SPHL	3	.45
PCHL	6	.90
DAD	4	.60
STAX	6	.90
LDAX	5	.75
INX	2	.30
DCX	3	.45
CMA	2	.30
STC	3	.45
CMC	4	.60
DAA	10	1.50
SHLD	11	1.65
LHLD	12	1.80
EI	2	.30
DI	2	.30
NOP	2	.30
MUL	26	3.90
MOV r1, r2	3	.45
MOV M, r	6	.90
MOV r, M	6	.90
HLT	4	.60
MVI r	4	.60
MVI M	7	1.05
INR	3	.45
DCR	4	.60
INR M, DCR M	8	1.20
Arithmetic reg	4	.60
Arithmetic mem	7	1.05
Arithmetic immed.	4	.60
RLC	4	.60
RRC	3	.45
RAL	4	.60
RAR	3	.45
JMP	6	.90
$\overline{\text{JMP}}$[1]	4	.60
CALL	13	1.95
$\overline{\text{CALL}}$[1]	4	.60
RET	8	1.20
$\overline{\text{RET}}$[1]	2	.30
RST	13	1.95
IN	8	1.20
OUT	8	1.20

	Min	Typ[2]	Max
DIV	4.80	6.60	8.40

NOTES

1. Conditional branch with condition not met.
2. Depends upon value of divisor.

DESCRIPTION

The Signetics Microassembler is a complete software package designed to support general slice system architectures which employ Signetics bipolar microprocessor components. It provides a flexible microassembler language which is adaptable to the numerous configurations and formats of systems using bipolar microprocessor chips. The Microassembly language allows specification of the microinstruction formats and bipolar devices utilized in a user system. This enables the Microassembly language to be tailored to the specific configuration for which the microprogram is written. In particular, the Mircoassembly language provides intrinsic support for the 3002 and 2901 Central Processing Elements and the 8X02 Control Store Sequencer. Through the inclusion of explicit definitions, similar support can be obtained for the 3001 Microprogram Control Unit, as well as other bipolar chips. Although specifically intended for use with Signetics' bipolar microprocessor products, the flexibility of the Microassembler enables it to handle virtually all microprogrammed applications.

The Microassembler consists of two independent programs. The first reads the microprogram and the appropriate configuration and format descriptions written in the Microassembly language. It produces a listing of the source input and the resulting binary form of the microinstructions in the microprogram. The listing also includes diagnostics for any errors found in the source and a cross reference for symbols used in the microprogram.

The second program punches paper tapes that can be used to program microcontrol store PROMS. It reads an object form of the microprogram produced by the first program. The microprogram object is partitioned into PROM modules and separate output is produced for each PROM.

MICROASSEMBLY LANGUAGE

The Microassembly language input to the Microassembler is divided into two sections. The first section defines the microinstruction formats and device configurations of the user system. The second section is the microprogram in the form of symbolic microinstructions.

The definition section specifies the name and length of each field in the microinstruction. Microinstructions may be any length, and multiple microinstruction formats may be defined. In addition, the definition section allows definition of opcodes used in writing symbolic microinstructions.

The microprogram section is the sequence of symbolic microinstructions which comprise the microprogram. A symbolic microinstruction is a statement specifying values for each field in the microinstruction. User defined opcodes allow mnemonic specification of field values. Field values not specified may be defaulted.

The Microassembly language also supports the standard assembler directives—ORG, EQU, SET, SPACE, TITLE, EJECT. Values in the Microassembly language may be decimal, hexadecimal, octal or binary constants, ASCII character constants, or symbolic values. These may also be combined into expressions using arithmetic, binary shift, and logical operators. The supported operators include +, -, SHR, SHL, NOT, AND, OR, XOR.

PROM FORMATTING

The microprogram object is formatted into paper tapes for programming microcontrol store PROMS using a microformat command file. The microformat commands specify the partitioning of the microprogram into PROMS and specify the format of the paper tape output. Each bit of a microinstruction may be individually allocated to a PROM and optionally inverted. The addressing space of the microprogram may also be partitioned with provisions for inverted addresses. A typical application would be the allocation of a 1024X40 microprogram to ten 512X8 PROMS.

The following paper tape formats are supported—2650 Absolute Object Code SMS format and various BNPF formats. The 2650 Absolute Object Code, can read by the Signetics TWIN (Test Ware Instrument—A microprocessor system development instrument) when it is used to program PROMS.

USING THE MICROASSEMBLER

The Microassembler is written in ANSI FORTRAN IV and it may be run on any machine of sufficient memory size which has the requisite standard FORTRAN compiler. It is available in source form on magnetic tape. Or, if desired, the Microasssembler may be accessed via TYMSHARE, GE or NCSS Timesharing Services. The Microassembler also provides special commands called toggles which adapt the Microassembler to specific operating environments.

A full description of the Microassember is contained in the Signetics Microassembler Reference Manual.

DESCRIPTION

The Signetics 8X300 Fixed Instruction Bipolar Microprocessor provides new levels of high performance to microprocessor applications not previously possible with MOS technology.

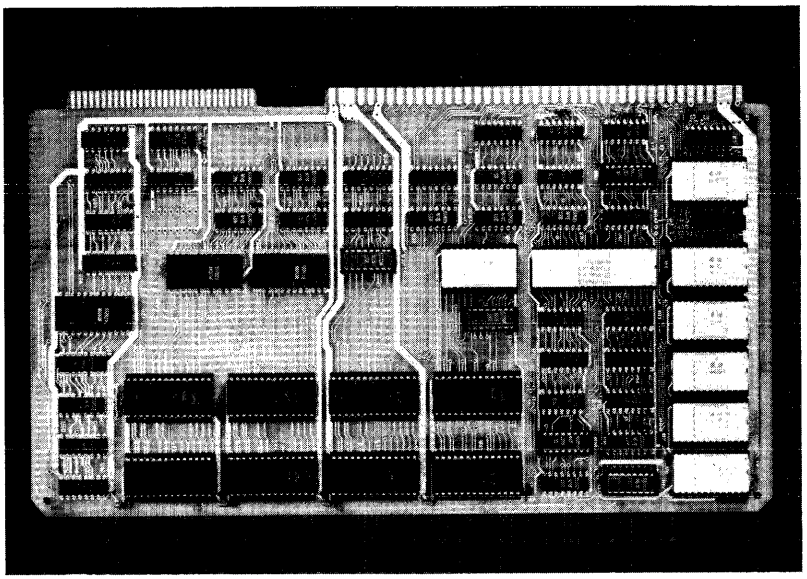
In the majority of cases, the choice of a bipolar microprocessor slice, as opposed to an MOS device, is based on speed. The 8X300 processor, combined with high-speed memory and I/O devices, is capable of executing all instruction in 250ns.

The 8X300 is optimized for control and data movement applications. It has a 13-bit address bus for selecting instructions from program storage and a separate input bus for entering a 16-bit instruction words. Data handling and I/O device addressing are accomplished via the 8-bit Interface Vector (IV) bus. The IV bus is supported by four additional control lines and a clock.

The unique features of the 8X300 IV bus and instruction set permit 8-bit parallel data to be rotated or masked before undergoing arithmetic or logical operations. Then, the data may be shifted and merged into any set of from 1 to 8 contiguous bits at the destination. The entire process of input, shifting, processing and output is done in 1 instruction cycle time. The 250ns cycle time makes the 8X300 ideally suited for high-speed applications.

The evaluation board contains all the elements which a designer needs to judge the suitability of the 8X300 for his systems applications. Included with the 8X300 are 4 I/O ports for external device interface, 256 bytes of temporary (working) data storage, and 512 words of program storage, all properly connected to the 8X300 to allow immediate exercising of the board. For this purpose, the PROMs are preprogramed with the I/O control, RAM control, and RAM integrity diagnostic programs. With the remaining PROM space, the designer may enter his own benchmark, test, or development routines.

The board design allows complete flexibility in access to the address, instruction, and IV busses as well as all controls and signals of the 8X300. The IV bus, I/O port user connection, clock signals control lines, address bus and instruction bus are wired to output pins, the board edge connector and flat cable connectors.
The board layout permits variations and/or expansions of the basic design. In addition to the access to all signals for transfer off the board, a wire wrap area is provided so that the designer may add to the board circuitry as he desires. The addition may include memory, additional interfaces, or special circuits which meet specific user requirements.



Controls are also provided for diagnostic and instructional purposes by allowing various operating modes. In the WAIT mode, the program may be single stepped for ease of checkout. The one-shot instruction jamming allows control of the program start location, changes of program flow, changing or examining the internal registers, or testing of simple sequences. The repeated instruction jamming provides a means of repetitive execution of an instruction so that the I/O bus and the control lines may be examined without software changes. In both of these jam cases, the jammed instruction is selected by board-mounted switches.

FEATURES

- **250ns CPU with Crystal**
- **4 I/O Ports (32 Lines)**
- **256 Bytes Data Storage**
- **512 Words Program Storage**
- **Run/Wait Control**
- **Single Step**
- **Instruction Jamming**
  One Shot Instruction Jam
  Repeated Jam
- **All Buses to Output Pins**
- **Firmware Diagnostics**
- **Wire-Wrap Area**
- **Edge Connector**
- **Flat Cable Connectors**
- **Wire Wrap Posts for Bus Lines**

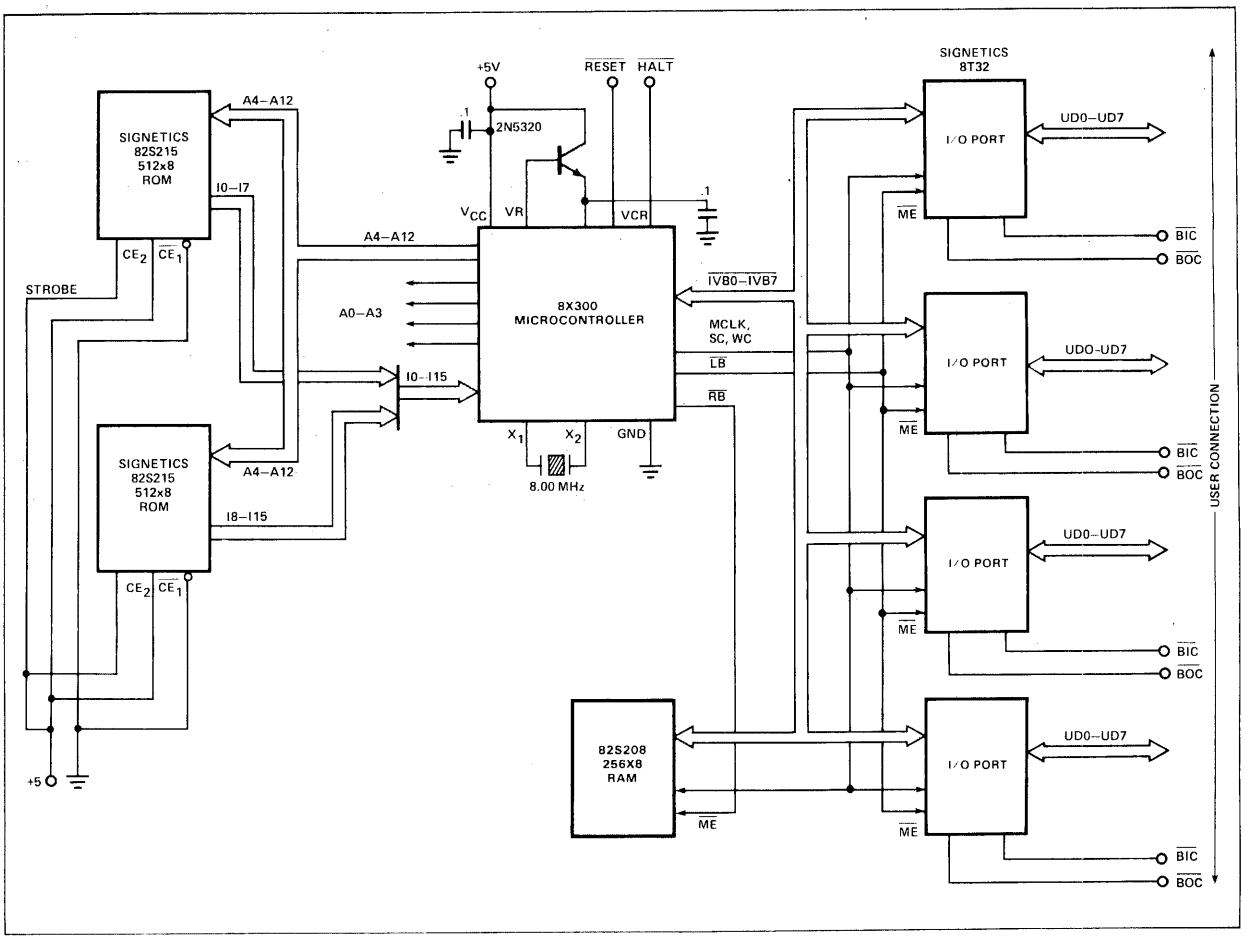
CONTENTS

1 ea— 8X300
8 ea— 82S116 (256 x 1 RAM)
2 ea— 82S115 (512 x 8 PROM)
4 ea— 8T32 Addressable Bidirectional I/O Port
1 ea— 8T31 (Bidirectional I/O Port)
2 ea— 8T26A (Quad Bus Transceiver)
4 ea— 74157 (Quad 2-Input Data Selector)
2 ea— 7474 (Dual D Flip Flop)
2 ea— 7400 (Quad Nand Gate)
1 ea— 7427 (3-Input NOR Gate)
1 ea— P.C. Board
Misc. Parts
1 ea— Introductory Manual, assembly instructions, code listings and schematics

AVAILABILITY

Immediate delivery from Signetics Rep. or Distributors.

BLOCK DIAGRAM



Auxiliary Circuits

The 8X300 can be used with any bipolar (or TTL-compatible) ICs. It can directly address 8192 program instruction locations and up to 512 I/O ports. The memory paging feature may be employed for larger working storage. Typical auxiliary circuits include:

Program Storage		82S115 (512x8 PROM)
I/O	8T32/33	(8-Bit Synchronous Bidirectional I/O Port)
	8T35/36	(8-Bit Asynchronous Bidirectional I/O Port)
	8T31	(8-Bit Bidirectional I/O Port)
	8T39	(Quad Bus Extender)
Working Storage		82S116 RAM

8T32KT1000SK

DESCRIPTION

A new kit has been developed which allows for convenient programming of the select addresses for the 8T32 family of devices, including the 8T33, 8T35 and 8T36. The kit consists of all parts necessary for the construction of the kit including voltage regulators, address program switches and status lights. All that is required is to construct the kit, apply +5 volts and approximately +28 volts and the 8T32 may be programmed. The programming sequence consists of three steps. First, the 8T32 select address is programmed. Second, the kit verifies the programming by testing for positive response to the address as well as the disable for the address complement. After verification, the programmer is switched to the protect mode in which the isolation is performed. This step prevents further address alteration. The kit includes documentation on assembly and use.

The kit is made available for those designers using 8T32 family devices so that they may easily program the address in their lab or at a conveniently located Signetics or Distributer facility. For prototyping, the designer may order unprogrammed devices and then put in addresses as required rather than ordering several addresses of the preprogrammed type. This will save the designer time and money.

AVAILABILITY

Immediate delivery from Signetics Rep. or Distributors

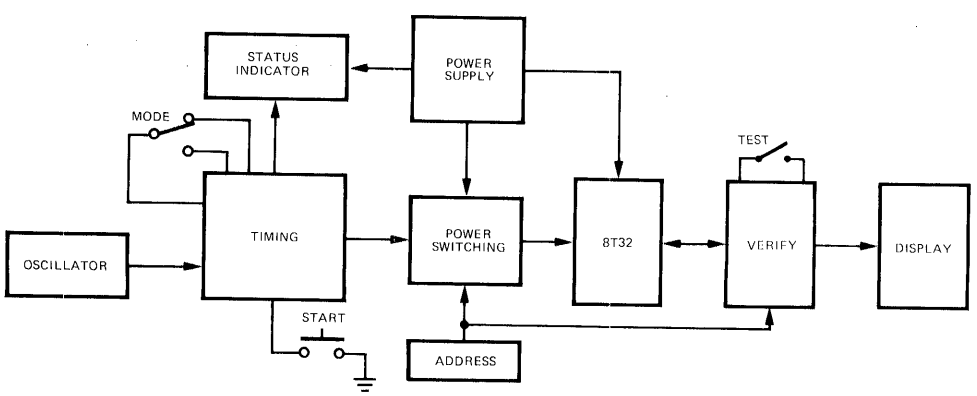
CONTENTS

PC board
All IC's, discrete parts, and hardware
Assembly instruction manual

FEATURES

- **Programs, isolates, and verifies select addresses for 8T32 family**
- **Kit contains all components necessary to build programmer**
- **Two hour assembly time**

BLOCK DIAGRAM



DESCRIPTION

The 8X300 Assembler is a program which accepts source code written in the 8X300 assembly language and which produces both a listing of the symbolic program and an object module in one of three formats: MCSIM, ROM Simulator or BPNF.

The assembler is written in ANSI standard Fortran and is approximately 2800 card images in length. It requires some rewindable I/O medium such as disk or tape for temporary storage, an input device to read source code and two output devices, one to output the assembler listing and one to output the object module. If desired, the assembler may be compiled and linked to execute in overlays.

The assembler consists of two passes which build a symbol table, issue helpful error messages, produce an easily readable program listing and output a computer readable object module.

FEATURES

- **Macros nested to three levels**
- **Conditional assembly**
- **Address arithmetic**
- **Automatic procedure/subroutine handling**
- **Reserved symbols for registers**
- **Multiple entry to procedures**
- **Symbolic machine operation codes**
- **Symbolic address assignment references**
- **Symbolic data creation statements (IV Byte References)**
- **Free format source code**
- **Syntax error checking**
- **Self-defining constants**
- **Assembly listing control statements**
- **ASCII character code**
- **Comment statements and comment areas**
- **Forward referencing**

MCCAP LANGUAGE

The assembler recognizes three types of statements: comment statements, machine instructions, and pseudo-ops (directives).

Comment statements are used to document a listing. They must contain an asterisk in column 1 and may contain any legal character in the other 79 columns.

Machine instruction statements are those statements that generate instruction(s) to be executed by the 8X300 processor. Machine instruction statements include:

MOVE	Move byte from one location to another.
ADD	Add the byte in one location to the byte in the auxiliary register and store the result in another location.
AND	AND the byte in one location with the byte in the auxiliary register and store the result in another location.
XOR	Exclusive OR the byte in one location with the byte in the auxiliary register and store the result in another location.
XEC	Execute the instruction at the specified address.
XMIT	Transmit the literal (immediate data) contained in this instruction to the specified location.
NZT	Jump to the specified address if the value in the specified location is not zero.
JMP	Jump to the specified address.
CALL	Transfer control to a procedure or an entry point.
RTN	Returns control from a procedure or an entry point.
SEL	Places the address of an IV Byte variable into the IVL or the IVR register.

Pseudo-Ops (or Directives) are commands to the assembler, but have no meaning to the 8X300 processor.

EQU	Assigns a value to the symbol in the label field.
SET	Identical to EQU, except that the symbol may be redefined by another SET statement.
LIV	Assigns a symbolic name to the address, position and precision of the "left bank" Interface Vector Byte variable.
RIV	Identical to LIV, except that the assignment is made to the "right bank" I/O Field.
PROG	Introduces and names the main program.
PROC	Introduces and names a procedure.
ENTRY	Specifies an additional entry point to a procedure.
END	Terminates a procedure, a program or a MACRO.
ORG	Changes the value of the location counter.
OBJ	Specifies the format of the object module.
IF	Introduces source statements subject to conditional assembly.
ENDIF	Terminates the source statements subject to conditional assembly.
LIST	Specifies the list and punch options.
NLIST	Negates the list and punch options.
EJCT	Advances listing to next page.
SPAC	Advances listing to next line.
MACRO	Defines the source statements generated a macro call.

AVAILABILITY

The assembler is available on NCSS, GE and TYMSHARE timesharing services. It is also available from Signetics on 9-track magnetic tape written in EBCDIC in 80-character unblocked records at a density of 800 bpi.

FEATURES

- **Totally self-contained with keyboard alpha-numeric display, tape reader, TTY output**
- **Dual MicroControllers: one to run instrument, one dedicated to execute user's program**
- **Real time instruction execution**
- **Control of program execution-Halt Single Step and Run Modes**
- **Direct program/register/IV examination and modification through keyboard**
- **Three breakpoint types—Normal, Halt and Insert Instruction**
- **Up to 4k words of high speed read/write program storage**
- **Format compatible with papertape output of MicroController Cross Assembly Program**

DESCRIPTION

The SMS MicroController Simulator, MCSIM, is a hardware development instrument designed to perform in the user's system exactly as an SMS MicroController. It directly supports the SMS 300 (8X300) as well as MicroController prototyping systems. MCSIM gives the user an Interpreter system with a modifiable Program Storage and a Control Panel which together provide a means of entering, running, monitoring, debugging and changing a program. It features ease of use due to its high level interactive display/keyboard and simple operating system. MCSIM allows the user to run his program on-line in real time. Through the Control Panel, data stored in internal registers, Working Storage and IV Bytes can be examined and modified. An extensive breakpoint capability permits the user to quickly locate program faults.

MCSIM contains two MicroControllers: one for running the instrument and a second totally dedicated to the user's program and prototyping system. This insures that when program development is complete and the design specifications have been met, production systems will perform identically with the prototype.

OPERATION

MCSIM operation is separated into six modes, each mode consisting of a related set of functions and status displays. Access to a mode is made using one of the six mode selection keys. (See Table 1). The currently selected mode is displayed at the extreme left part of the display; the currently selected function is displayed at the extreme right of the display. Selection among the available functions is made using the ↑ and ↓ keys, incrementing and decrementing to the next function. The function selected at last exit is automatically re-selected when the mode is re-entered except for the Breakpoint Mode which selects the Current display.

An operation is generally performed using the following four steps:

1. Select a mode by depressing one of the six Mode Select Keys.
2. Select a function in that mode by positioning the function roll with one of the two Function Select Keys.
3. Set up any necessary conditions, such as entering data or readying papertape in the reader.
4. Activate the function by depressing the Function Acknowledge Key (FCN/ACK).

MODE	FUNCTIONS
Manual Examination and alteration of Program Storage	Change Address Store Instruction
Tape Load or dump all or part of Program Storage	Load Verify Begin Punch Address End Punch Address Punch Program Identification
Register Examination and alteration of the Interpreter's internal registers	Change Address Store Octal Data Store Binary Data Complement Overflow
Interface Vector Examination and alteration of the locations on the IV Bus	Display Current Enabled Bytes Change IV Address Store Binary Data in IV Location
Breakpoint Set one of three types of breakpoint for program debugging	Display Currently Active Breakpoint Set Normal (Sync) Breakpoint Set Stop Breakpoint Replace Instruction at Breakpoint
Execute Control and monitor execution of a program	Halt Run Program Insert Instruction Single Step

Table 1 MCSIM OPERATOR CONTROLLED FUNCTIONS

SPECIFICATIONS

Control Panel

The Mode Select Keys and the Function Select Keys used in combination give the user 26 possible functions to accomplish complete loading and testing of the program. Each Mode Select Key accesses a set of functions, one of which is chosen using the Function Select Keys.

Status Messages

Message displays are used to indicate special conditions which may result from the operation of MCSIM:

POWER ON, MCSIM SYSTEM START
???MORE THAN ONE KEY PRESSED
UNABLE TO READ TAPE. RESTART
UNDEFINED MEMORY ADDRESS (octal address)
INVALID INSTRUCTION (instruction code)
LOADING INTERRUPTED, RESTART,
V'FYING INTERRUPTED, RESTART
P'CHING INTERRUPTED, RESTART
NO VERIFY (octal address, tape data, memory data)
CLEAR RESET LINE TO START RUNNING
CLEAR HALT LINE TO START RUNNING
INVALID 8-BIT OCTAL VALUE (octal value)
UNDEFINED IV BYTE ADDRESS (octal address)

Sync Output

Output pulse whenever address breakpoint is reached.

System Interface

MCSIM is connected to the user's prototyping system via a single ribbon cable. This cable terminates in either a MicroController Simulation Module or a dual in-line plug which is pin for pin compatible with the SMS 300 Interpreter. There are two different simulation modules to exactly match presently available MicroController systems. Selection of the proper input/output connector makes a MCSIM appear to be physically and electrically equivalent to a production MicroController or Interpreter.

Data Input/Output

COMPONENTS	DESCRIPTION
Panel	36 character self scan display for messages and data readout 12 key numeric keyboard for data entry/modification
Tape Reader	120 character/second tape reader for high speed data entry (ASCII format)
TTY	20mA current loop output for listing of program code on Teletype® terminal

PHYSICAL CHARACTERISTICS

Power	115V or 230V ± 10% 50 or 60Hz ± 10% 350 watts/min. to 750 watts/max. (Power dissipation dependent on the number of Simulation Modules configured in the system)
Dimensions	7 inches high x 17 inches wide x 19 inches deep
Installation	May be used on table or may be installed in standard 19 inch rack with mount adapters
Weight	65 lbs. net, 75 lbs. shipping
Ventilation	Air Flow 120 CFM
Environmental	0° to 55°C, Relative Humidity to 90%.

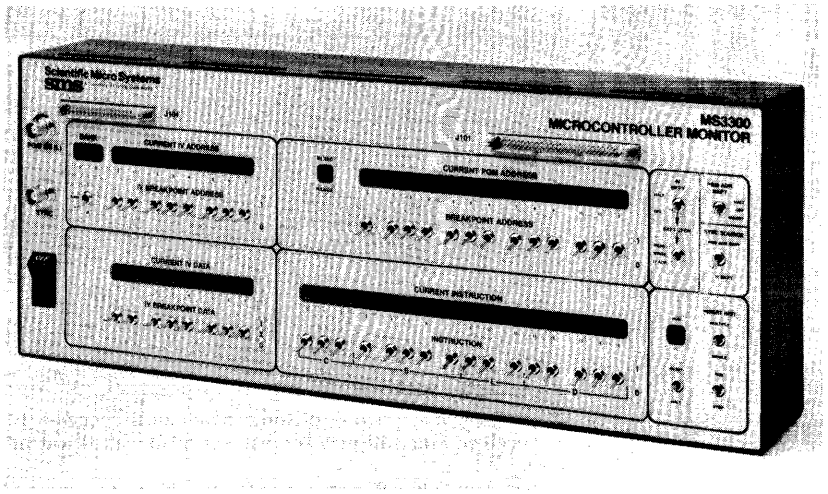
MCCAP

The MicroController Cross Assembly Program (MCCAP) is designed to translate symbolic instructions into object code that can be executed by the SMS 300. This program will run on most computers that have a FORTRAN compiler with a computer word length of at least 16 bits and a random access capability. MCCAP features:

- **Symbolic address assignment and references**
- **Automatic Procedure Handling**
- **Predefined System Procedures**
- **Forward References**
- **Expression Evaluation**
- **Flexibility to handle MicroController component configurations as well as standard systems**
- **Generation of object code for MCSIM, and SMS ROM Simulator, or most PROM programmers**

FEATURES

- **Real time monitoring instrument for SMS 300**
- **Totally self contained**
- **Displays IV address and data**
- **Displays current program address**
- **Displays current instruction**
- **Control of RESET and HALT**
- **Single step capability**
- **Real time instruction insertion**
- **Two real time breakpoints**
- **Breakpoint output signal**

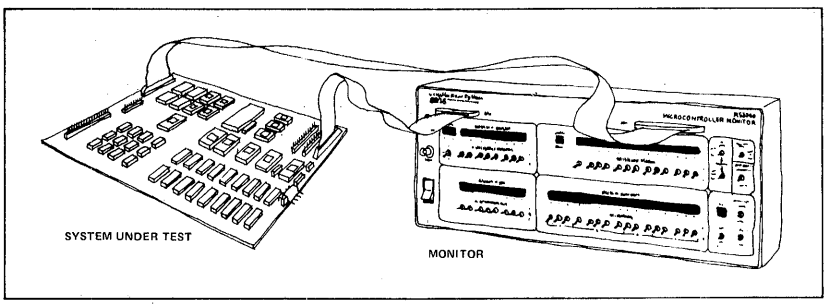


DESCRIPTION

The MicroController Monitor is a self contained debug and maintenance tool for use with all systems containing the SMS 300 (8X300). It provides a control panel allowing an operator to observe, modify, and control program execution in real time permitting system faults to be rapidly traced. The Monitor displays the status of the Address, Instruction, and IV Bus of an Interpreter. Switch registers associated with each display can be used to set breakpoint addresses and enter instructions or data from the Monitor. Program execution can be halted, single stepped, or altered from Monitor controls.

The Monitor can be used to insert instructions thereby examining or modifying the contents of internal registers, Working Store, and IV Bytes. In addition, it can be used to start program execution from any address and enable the operator to set program loops allowing a program segment to be checked independently of normal program flow. Breakpoints on IV data and program address allow the operator to halt program execution or insert instructions in real time.

As shown in the diagram below, the Monitor connects to the system under test through flat ribbon cables (provided) or an adaptor (optional) which plugs into an Interpreter socket. These connections are buffered and present a negligible load to the system. Other features include a Sync output which provides pulses at a selectable program address or Interface Vector event.



OPERATION

The MicroController Monitor provides the user with two basic modes of system operation, RUN and STEP. When in the RUN mode, indicator LED's provide a continuous real time display of the three major system busses: Address, Instruction, and Data. Program execution can be halted by one of two actions: depressing the Halt switch or selecting the Halt on Breakpoint function. When halted, it is possible to execute one instruction at a time by pressing the RUN/STEP control to the STEP position. The readout shows the current (static) bus information and the next instruction to be executed.

For checkout purposes it is useful to be able to set a program loop or modify the normal progam flow in some other manner. This is accomplished by inserting in real time the instruction set up on the Instruction Switch Register whenever the Program Address Breakpoint is reached. To check for system noise or similar malfunction a separate Insert Instruction switch can be set to the Multiple position, forcing one instruction repetitively. When halted, a single instruction can be inserted by toggling the Insert Instruction switch to the Single position. When an instruction is being inserted, system ROM is temporarily disabled.

To aid in the diagnosis of a malfunction an advanced breakpoint capability is provided. In addition to the Halt and Insert functions when a Program Address Breakpoint is reached, a breakpoint can be generated on the Interface Vector (IV) Bus data or address. This permits program execution to be halted or a Sync pulse generated in response to external data or the contents of RAM. Three modes of IV Breakpoint generation are selectable: Breakpoint on IV Address; Breakpoint on IV Address and IV Write Data; and Breakpoint on IV Address and IV Read Data. The IV Breakpoint Data switches have a "don't care" position to permit generation of a breakpoint on a data subfield. A Sync pulse output is provided on either the IV Breakpoint or Program Address Breakpoint (switch selectable).

SPECIFICATIONS

Controls	Function
RUN/STEP	Sets operation mode, continuous execution (RUN) or single step (STEP).
INSERT INST	Unconditionally causes execution of the instruction in the Instruction Switch Register.
RESET/HALT	Three position switch used to unconditionally HALT program execution or RESET Interpreter's Program Counter to zero.
PGM ADR BKPT	Selects appropriate function to be performed when Program Address Breakpoint is reached: HALT—halt on breakpoint, INSERT—replace normal instruction with instruction set into Instruction Switch Register, OFF—program execution unchanged by breakpoint.
IV BKPT	Selects appropriate function to be performed when IV Breakpoint is reached: HALT—halt on breakpoint, OFF—program execution unchanged by breakpoint.
BKPT UPON	Selects IV Breakpoint on one of three conditions: specified IV address, specified write data at IV address, specified read data at the IV address.
SYNC SOURCE	Selects source for output Sync pulse, IV Breakpoint or Program Address Breakpoint. Sync pulse always available at breakpoint regardless of function selected by breakpoint controls.
Switch Registers	
INSTRUCTION	Sixteen two position switches for entering instruction to be inserted (during breakpoint or insert instruction control).
BREAKPOINT ADDRESS	Thirteen two position switches to select program breakpoint address.
IV BREAKPOINT ADDRESS	Eight two position switches to select IV byte breakpoint address or Working Store breakpoint address.
BANK	Selects display of LB (Left Bank) or RB (Right Bank) IV address information. Also selects either LB or RB for IV breakpoint.
IV BREAKPOINT DATA	Eight three position switches, 0, 1, X (don't care), to select IV Data Breakpoint.
Displays	
RUN	LED display indicating when Interpreter not halted.
CURRENT INSTRUCTION	LED display of the binary value of next instruction to be executed.
CURRENT PROGRAM ADDRESS	LED display of the binary address of the next instruction to be performed.
IN XEC RANGE	LED display indicating that the value of the Interpreter's program counter and address register may not match because the previous instruction command was "Execute."
BANK	Displays band addressed by the current instruction (left bank or right bank).
CURRENT IV ADDRESS	Shows the binary address of the currently enabled IV Byte or Working Store location.
CURRENT IV DATA	Binary display of the data on the IV bus.
Outputs	
SYNC PGM EN(L)	Pulse output whenever the switch selected breakpoint occurs. A low true signal used to enable or disable system program ROM (required only when Interpreter adaptor is used).
Cycle Time	
The Monitor can be adjusted to work with any MicroController-based system with a cycle time of 200ns to 2μs.	

PHYSICAL CHARACTERISTICS

Power	115Vac ± 10% at 0.75 amp max. 230Vac ± 10% at 0.38 amp max. (optional) 47-63Hz
Dimensions	7" H x 17.5" W x 3" D
Installation	May be used on table or may be installed in standard 19 inch rack (using optional adaptors).
Weight	10 lbs. net, 13 lbs. shipping
Ventilation	Forced air, 120 CFM.
Environmental	0° to+ 50°C, relative humidity to 90%
Cables	2 provided, 3 feet long

CHAPTER 2
MOS Microprocessors, Peripherals and Development Products

DESCRIPTION

The 2650A and -1 are additional members of the Signetics family of 8-bit, NMOS microprocessors.

The 2650A is a functional equivalent of the 2650 with a new mask design which provides improved device operating margins.

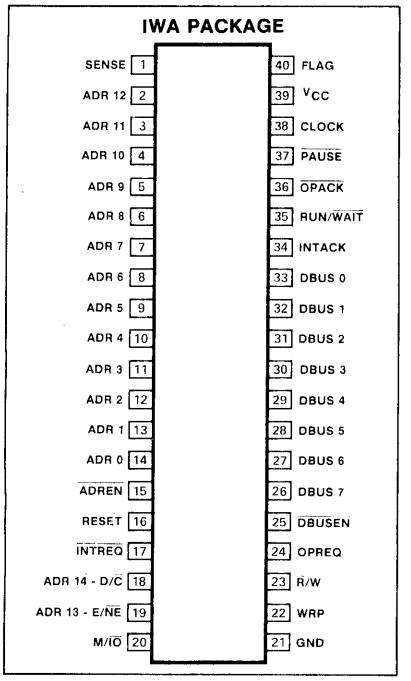
The 2650A-1 is a high speed version of the 2650A.

FEATURES

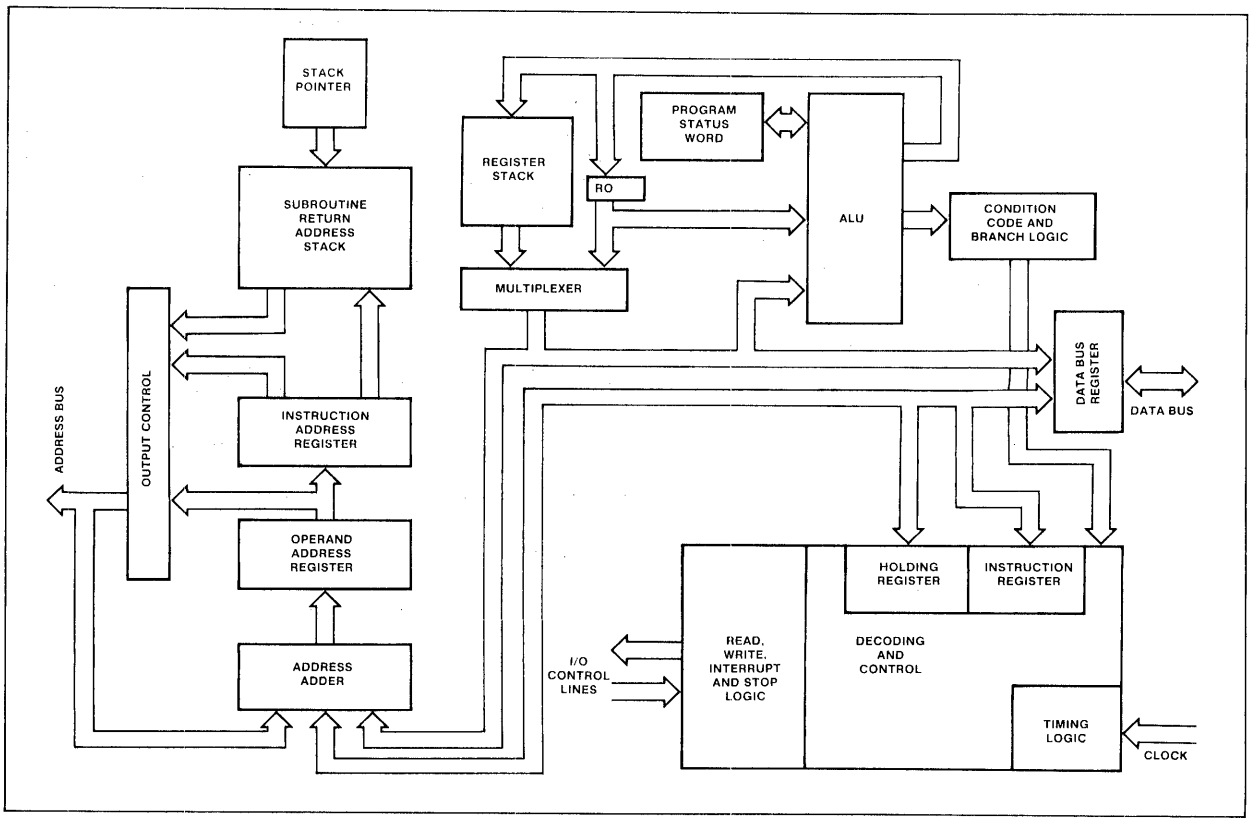
- **Static 8-bit parallel NMOS microprocessor**
- **Single power supply of +5 volts**
- **TTL level single phase clock**
- **Standard 40 pin dual in-line package**
- **TTL compatible inputs and outputs**
- **75 variable length instructions of 1, 2 or 3 bytes**
- **32k byte address range**
- **Coding efficiency with multiple addressing modes**
- **Synchronous or asynchronous memory and I/O interface**
- **Interfaces directly with industry standard memories**
- **Single bit serial I/O path**
- **Seven 8-bit addressable general purpose registers**
- **Vectored interrupt**
- **Subroutine return address stack**
- **2.4μs machine cycle time (2650A)**
- **1.5μs machine cycle time (2650A-1)**

PIN CONFIGURATION

IWA PACKAGE



BLOCK DIAGRAM



PIN DESIGNATION

MNEMONIC	NUMBER	NAME	TYPE	FUNCTION
ADR0-ADR12	14-2	Address lines	O	Low order memory address lines for instruction or operand fetch. ADR0 is the least significant bit and ADR12 is the most significant bit. ADR0 through ADR7 are also used as the I/O device address for extended I/O instructions.
ADR13-E/$\overline{NE}$	19	Address 13-Extended/Non Extended	O	Low order memory page address line during memory reference instructions. For I/O instructions this line discriminates between extended and non-extended I/O instructions.
ADR14-D/$\overline{C}$	18	Address 14-Data/Control	O	High order memory page address line during memory reference instructions. It also serves as the I/O device address for non-extended I/O instructions.
$\overline{ADREN}$	15	Address enable	I	Active low input allowing tri-state control of the address bus ADR0-ADR12.
DBUS0-DBUS7	33-26	Data bus	I/O	These lines provide communication between the CPU, Memory, and I/O devices for instruction and data transfers.
$\overline{DBUSEN}$	25	Data bus enable	I	This active low input allows tri-state control of the data bus.
OPREQ	24	Operation request	O	Indicates to external devices that all address, data and control information is valid.
$\overline{OPACK}$	36	Operation acknowledge	I	Active low input indicating completion of an external operation. This allows asynchronous functioning of external devices.
M/$\overline{IO}$	20	Memory/input-output	O	Indicates whether the current operation references memory or I/O.
$\overline{R}$/W	23	Read/Write	O	Indicates a read or a write operation.
WRP	22	Write pulse	O	This is a timing signal from the 2650 that provides a positive-going pulse during each requested write operation (memory or I/O) and a high level during read operations.
SENSE	1	Sense	I	The sense bit in the PSU reflects the logic state of the sense input to the processor at pin #1.
FLAG	40	Flag	O	The flag bit in the PSU is tied to a latch that drives the flag output at pin #40.
$\overline{INTREQ}$	17	Interrupt request	I	This active low input line indicates to the processor that an external device is requesting service. The processor will recognize this signal at the end of the current instruction if the interrupt inhibit status bit is zero.
INTACK	34	Interrupt acknowledge	O	This line indicates that the 2650 is ready to receive the interrupt vector (relative address byte) from the interrupting device.
$\overline{PAUSE}$	37	Pause	I	This active low input is used to suspend processor operation at the end of the current instruction.
RUN/$\overline{WAIT}$	35	Run/Wait	O	This output is a processor status indicator. During normal operation this line is high. If the processor is halted either by executing a halt instruction or by a low input on the pause line, the run/wait line will go low.
RESET	16	Reset	I	Resets the instruction address register to zero and clears the interrupt inhibit bit.
CLOCK	38	Clock	I	A positive going pulse train that determines the instruction execution time.
V_{CC}	39	+5V	I	+5V power
GND	21	GND	I	Ground

FUNCTIONAL DESCRIPTION

The 2650 series processors are general purpose, single chip, fixed instruction set, parallel 8-bit binary processors. A general purpose processor can perform any data manipulations through execution of a stored sequence of machine instructions. The processor has been designed to closely resemble conventional binary computers, but executes variable length instructions of one to three bytes in length.

The 2650 series contains a total of seven general purpose registers, each eight bits long. They may be used as source or destination for arithmetic operations, as index registers, and for I/O transfers.

The processor can address up to 32,768 bytes of memory in four pages of 8,192 bytes each. The processor instructions are one, two, or three bytes long, depending on the instruction. Variable length instructions tend to conserve memory space since a one-or-two byte instruction may often be used rather than a three byte instruction. The first byte of each instruction always specifies the operation to be performed and the addressing mode to be used. Most instructions use six of the first eight bits for this purpose, with the remaining two bits forming the register field. Some instructions use the full eight bits as an operation code.

The Data Bus and Address signals are tri-state to provide convenience in system design. Memory and I/O interface signals are asynchronous so that Direct Memory Access (DMA) and multiprocessor operations are easy to implement.

The block diagram for the 2650 series shows the major internal components and the data paths that interconnect them. In order for the processor to execute an instruction, it performs the following general steps:

1. The Instruction Address Register provides an address for memory.
2. The first byte of an instruction is fetched from memory and stored in the Instruction Register.
3. The Instruction Register is decoded to determine the type of instruction and the addressing mode.
4. If an operand from memory is required, the operand address is resolved and loaded into the Operand Address Register.
5. The operand is fetched from memory and the operation is executed.
6. The first byte of the next instruction is fetched.

The Instruction Register (IR) holds the first byte of each instruction and directs the subsequent operations required to execute each instruction. The IR contents are decoded and used in conjunction with the timing information to control the activation and sequencing of all the other elements on the chip. The Holding Register is used in some multiple-byte instructions to contain further instruction information and partial absolute addresses.

The Arithmetic Logic Unit (ALU) is used to perform all of the data manipulation operations, including Load, Store, Add, Subtract, And, Inclusive Or, Exclusive Or, Compare, Rotate, Increment and Decrement. It contains and controls the Carry bit, the Overflow bit, the Interdigit Carry and the Condition Code Register.

The Register Stack contains six registers that are organized into two banks of three registers each. The Register Select bit picks one of the two banks to be accessed by instructions. In order to accommodate the register-to register instructions, register zero (R0) is outside the array. Thus, register zero is always available along with one set of three registers.

The Address Adder is used to increment the instruction address and to calculate relative and indexed addresses.

The Instruction Address Register holds the address of the next instruction byte to be accessed. The Operand Address Register stores operand addresses and sometimes contains intermediate results during effective address calculations.

The Return Address Stack (RAS) is a Last In, First Out (LIFO) storage which receives the return address whenever a Branch-to-Subroutine instruction is executed. When a Return instruction is executed, the RAS provides the last return address for the processor's IAR. The stack contains eight levels of storage so that subroutines may be nested up to eight levels deep. The Stack Pointer is a three bit wraparound counter that indicates the next available level in the stack. It always points to the current address.

PROGRAM STATUS WORD

The Program Status Word (PSW) is a major feature of the 2650 which greatly increases its flexibility and processing power. The PSW is a special purpose register within the processor that contains status and control bits.

It is divided into two bytes called the Program Status Upper (PSU) and Program Status Lower (PSL). The PSW bits may be tested, loaded, stored, preset, or cleared using the instructions which affect the PSW. The bits are utilized as shown in Table 1.

BYTE	MNEMONIC	FUNCTION
PSU0,1,2	SP	Pointer for the Return Address Stack.
PSU3,4		Not used. These bits are always zero.
PSU5	II	Used to inhibit recognition of additional Interrupts.
PSU6	F	Flag is a latch directly driving the flag output.
PSU7	S	Sense equals the state of the sense input.
PSL0	C	Carry stores any carry from the high-order bit of ALU.
PSL1	COM	Compare determines if a logical or arithmetic comparison is to be made.
PSL2	OVF	Overflow is set if a two's complement overflow occurs.
PSL3	WC	With Carry determines if the carry is used in arithmetic and rotate instructions.
PSL4	RS	Register Select identifies which bank of 3 GP registers is being used.
PSL5	IDC	Inter Digit Carry stores the bit-3 to-bit-4 carry in arithmetic operations.
PSL6,7	CC	Condition Code is affected by compare, test and arithmetic instructions.

PSU

7	6	5	4	3	2	1	0
S	F	II			SP2	SP1	SP0

S Sense
F Flag
II Interrupt Inhibit
SP2 Stack Pointer Two
SP1 Stack Pointer One
SP0 Stack Pointer Zero

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

CC1 Condition Code One
CC0 Condition Code Zero
IDC Interdigit Carry
RS Register Bank Select
WC With/Without Carry
OVF Overflow
COM Logical/Arithmetic Compare
C Carry/Borrow

Table 1 PROGRAM STATUS WORD

INPUT/OUTPUT INTERFACE

The 2650 series microprocessor has a set of versatile I/O instructions and can perform I/O operations in a variety of ways. One- and two-byte I/O instructions are provided, as well as a special single-bit I/O facility. The I/O modes provided by the 2650 are designated as Data, Control, and Extended I/O.

Data or Control I/O instructions, also called Non-Extended I/O instructions, are one byte long. Any general purpose register can be used as the source or destination. A special control line indicates if either a Data or Control instruction is being executed.

Extended I/O is a two-byte read or write instruction. Execution of an extended I/O instruction will cause a 8-bit address, taken from the second byte of the instruction, to be placed on the low order eight address lines. The data, which can originate or terminate with any general purpose register, is placed on the data bus. This type of I/O can be used to simultaneously select a device and send data to it.

Memory reference instructions that address data outside of physical memory may also be used for I/O operations. When an instruction is executed, the address may be decoded by the I/O device rather than memory.

MEMORY INTERFACE

The memory interface consists of the address bus, the 8-bit data bus and several signals that operate in an interlocked or handshaking mode.

The Write Pulse signal is designed to be used as a memory strobe signal for any memory type. It has been particularly optimized to be used as the Chip Enable or Read/Write signal.

INTERRUPT HANDLING CAPABILITY

The 2650 series has a single level hardware vectored interrupt capability. When an interrupt occurs, the processor finishes the current instruction and sets the Interrupt Inhibit bit in the PSW. The processor then executes a Branch to Subroutine Relative to location Zero (ZBSR) instruction and sends out Interrupt Acknowledge and Operation Request signals. On receipt of the INTACK signal the interrupting device inputs an 8-bit address, the interrupt vector, on the data bus. The relative and relative indirect addressing modes combined with this 8-bit address allow interrupt service routines to begin at any addressable memory location.

INSTRUCTION SET

It may be seen from examination of the 2650 instruction set that there are many powerful instructions which are all easily understood and are typical of larger computers. There are one-, two-, and three-byte instructions as a result of the multiplicity of addressing models. See Table 2 for a complete listing and Block Diagram for instruction formats.

Automatic incrementing or decrementing of an index register is available in the arithmetic indexed instructions. All of the branch instructions except indexed branching can be conditional.

Register-to-register instructions are one byte; register-to-storage instructions are two or three bytes long. The two-byte register-to-memory instructions are either immediate or relative addressing types.

	MNE-MONIC	DESCRIPTION OF OPERATION	OP CODE R or CC 3 2 1 0	PSW BITS AFFECTED CC	IDC	C	OVF	SP	II	F	BYTES	CYCLES	FOR-MAT*	NOTE
LOAD/STORE	LODZ	Load register zero	03 02 01 —	•							1	2	Z	1
	LODI	Load immediate	07 06 05 04	•							2	2	I	1
	LODR	Load relative	0B 0A 09 08	•							2	3	R	1,6
	LODA	Load absolute	0F 0E 0D 0C	•							3	4	A	6
	STRZ	Store register zero	C3 C2 C1 —	•							1	2	Z	1
	STRR	Store relative	CB CA C9 C8								2	3	R	6
	STRA	Store absolute	CF CE CD CC								3	4	A	6
ARITHMETIC	ADDZ	Add to register zero w/wo carry	83 82 81 80	•	•	•	•				1	2	Z	1
	ADDI	Add immediate w/wo carry	87 86 85 84	•	•	•	•				2	2	I	1
	ADDR	Add relative w/wo carry	8B 8A 89 88	•	•	•	•				2	3	R	1,6
	ADDA	Add absolute w/wo carry	8F 8E 8D 8C	•	•	•	•				3	4	A	1,6
	SUBZ	Subtract from register zero w/wo borrow	A3 A2 A1 A0	•	•	•	•				1	2	Z	1
	SUBI	Subtract immediate w/wo borrow	A7 A6 A5 A4	•	•	•	•				2	2	I	1
	SUBR	Subtract relative w/wo borrow	AB AA A9 A8	•	•	•	•				2	3	R	1,6
	SUBA	Subtract absolute w/wo borrow	AF AE AD AC	•	•	•	•				3	4	A	1,6
	DAR	Decimal adjust register	97 96 95 94	•							1	3	Z	1,10
LOGICAL	ANDZ	AND to register zero	43 42 41 —	•							1	2	Z	1
	ANDI	AND immediate	47 46 45 44	•							2	2	I	1
	ANDR	AND relative	4B 4A 49 48	•							2	3	R	1,6
	ANDA	AND absolute	4F 4E 4D 4C	•							3	4	A	1,6
	IORZ	Inclusive-OR to register zero	63 62 61 60	•							1	2	Z	1
	IORI	Inclusive-OR immediate	67 66 65 64	•							2	2	I	1
	IORR	Inclusive-OR relative	6B 6A 69 68	•							2	3	R	1,6
	IORA	Inclusive-OR absolute	6F 6E 6D 6C	•							3	4	A	1,6
	EORZ	Exclusive-OR to register zero	23 22 21 20	•							1	2	Z	1
	EORI	Exclusive-OR immediate	27 26 25 24	•							2	2	I	1
	EORR	Exclusive-OR relative	2B 2A 29 28	•							2	3	R	1,6
	EORA	Exclusive-OR absolute	2F 2E 2D 2C	•							3	4	A	1,6
ROTATE/COMPARE	COMZ	Compare to register zero arithmetic/logical	E3 E2 E1 E0	•							1	2	Z	2
	COMI	Compare immediate arithmetic/logical	E7 E6 E5 E4	•							2	2	I	3
	COMR	Compare relative arithmetic/logical	EB EA E9 E8	•							2	3	R	3,6
	COMA	Compare absolute arithmetic/logical	EF EE ED EC	•							3	4	A	3,6
	RRR	Rotate register w/wo carry	53 52 51 50	•	•	•	•				1	2	Z	1
	RRL	Rotate register left w/wo carry	D3 D2 D1 D0	•	•	•	•				1	2	Z	1
BRANCH	BCTR	Branch on condition true relative	1B 1A 19 18								2	3	R	7,8
	BCTA	Branch on condition true absolute	1F 1E 1D 1C								3	3	B	7,8
	BCFR	Branch on condition false relative	— 9A 99 98								2	3	R	7
	BCFA	Branch on condition false absolute	— 9E 9D 9C								3	3	B	7
	BRNR	Branch on register non-zero relative	5B 5A 59 58								2	3	R	7,8
	BRNA	Branch on register non-zero absolute	5F 5E 5D 5C								3	3	B	7,8
	BIRR	Branch on incrementing register relative	DB DA D9 D8								2	3	R	7,8
	BIRA	Branch on incrementing register absolute	DF DE DD DC								3	3	B	7,8

Table 2 INSTRUCTION SET SUMMARY

	MNE-MONIC	DESCRIPTION OF OPERATION	OP CODE R or CC 3 2 1 0	PSW BITS AFFECTED CC	IDC	C	OVF	SP	II	F	BYTES	CYCLES	FOR-MAT*	NOTE
BRANCH (Cont'd)	BDR R	Branch on decrementing register relative	FB FA F9 F8								2	3	R	7,8
	BDR A	Branch on decrementing register absolute	FF FE FD FC								3	3	B	7,8
	ZBRR	Zero branch relative, unconditional	9B — — —								2	3	ER	6
	BXA	Branch indexed absolute, unconditional	9F — — —								3	3	EB	5,6
SUBROUTINE BRANCH/RETURN	BST R	Branch to subroutine on condition true, relative	3B 3A 39 38					•			2	3	R	7,8
	BST A	Branch to subroutine on condition true, absolute	3F 3E 3D 3C					•			3	3	B	7,8
	BSF R	Branch to subroutine on condition false, relative	— BA B9 B8					•			2	3	R	7
	BSF A	Branch to subroutine on condition false, absolute	— BE BD BC					•			3	3	B	7
	BSN R	Branch to subroutine on non-zero register, relative	7B 7A 79 78					•			2	3	R	7,8
	BSN A	Branch to subroutine on non-zero register, absolute	7F 7E 7D 7C					•			3	3	B	7,8
	ZBSR	Zero branch to subroutine relative, unconditional	BB — — —								2	3	ER	6
	BSXA	Branch to subroutine, indexed, absolute unconditional	BF — — —								3	3	EB	5,6
	RET C	Return from subroutine, conditional	17 16 15 14					•			1	3	Z	8
	RET E	Return from subroutine and enable interrupt, conditional	37 36 35 34					•	•		1	3	Z	8
INPUT/OUTPUT	WRTD	Write data	F3 F2 F1 F0								1	2	Z	
	REDD	Read data	73 72 71 70	•							1	2	Z	1
	WRTC	Write control	B3 B2 B1 B0								1	2	Z	
	REDC	Read control	33 32 31 30	•							1	2	Z	1
	WRTE	Write extended	D7 D6 D5 D4								2	3	I	
	REDE	Read extended	57 56 55 54	•							2	3	I	1
MISC.	HALT	Halt, enter wait state	— — — 40								1	1	E	
	NOP	No operation	— — — C0								1	1	E	
	TMI	Test under mask immediate	F7 F6 F5 F4	•							2	3	I	4
PROGRAM STATUS	LPS U	Load program status, upper	92					•	•	•	1	2	E	
	LPS L	Load program status, lower	93	•	•	•	•				1	2	E	9
	SPS U	Store program status, upper	12	•							1	2	E	1
	SPS L	Store program status, lower	13	•							1	2	E	1
	CPS U	Clear program status, upper, masked	74					•	•	•	2	3	EI	
	CPS L	Clear program status, lower, masked	75	•	•	•	•				2	3	EI	9
	PPS U	Preset program status, upper, masked	76					•	•	•	2	3	EI	
	PPS L	Preset program status, lower, masked	77	•	•	•	•				2	3	EI	9
	TPS U	Test program status, upper, masked	B4	•							2	3	EI	4
	TPS L	Test program status, lower, masked	B5	•							2	3	EI	4

*See Figure 1

Table 2 INSTRUCTION SET SUMMARY (Cont'd)

NOTES

1. Condition code (CC1, CC0): 01 if positive, 00 if zero, 10 if negative.
2. Condition code (CC1, CC0): 01 if R0 > r, 00 if R0 = r, 10 if R0 < r.
3. Condition code (CC1, CC0): 01 if r > V, 00 if r = V, 10 if r < V.
4. Condition code (CC1, CC0): 00 if all selected bits are 1s, 10 if not all the selected bits are 1s.
5. Index register must be register 3 or 3.
6. Requires two additional cycles if indirection is specified.
7. Requires two additional cycles if indirection is specified and branch is taken.
8. Specify CC = 11 for unconditional branch.
9. RS, WC and COM bits in PSW are also affected.
10. CC assumes number in register is a binary number.

ADDRESSING MODES

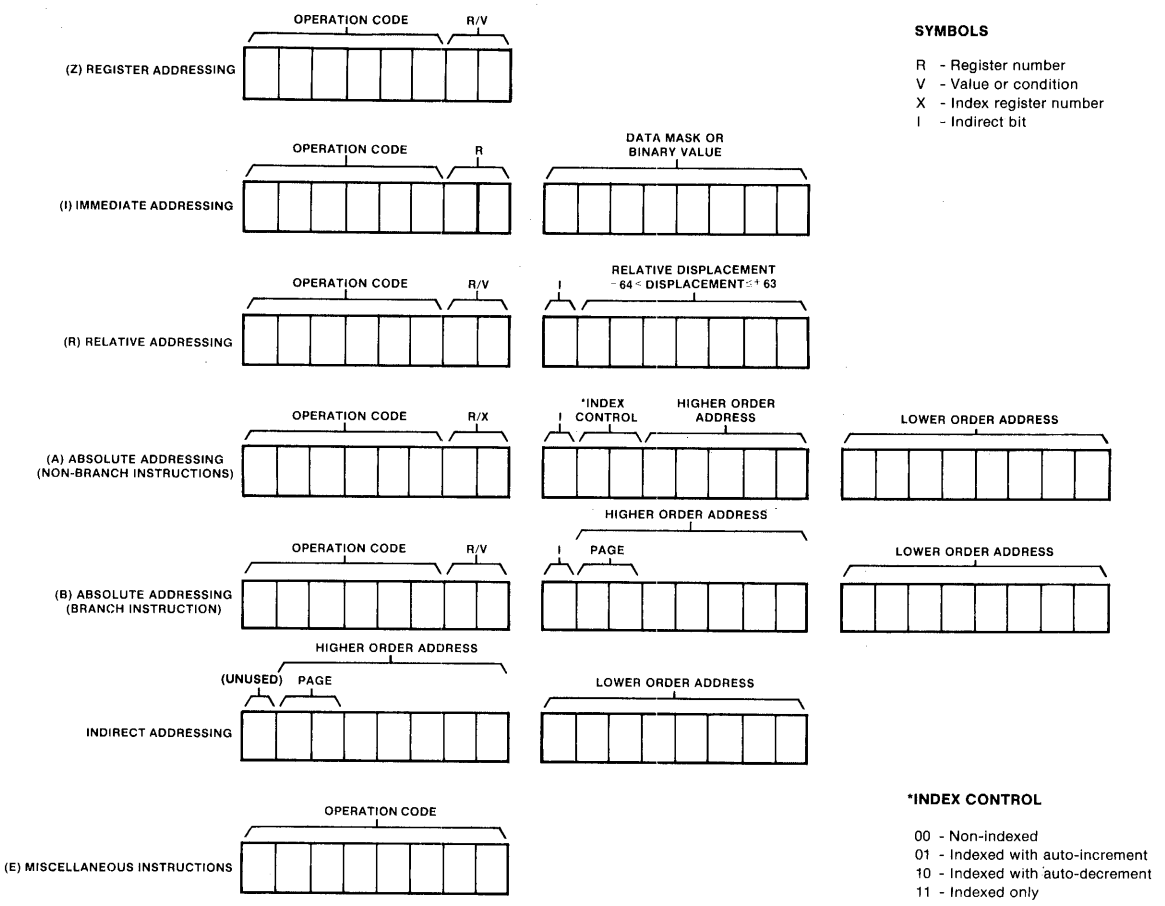


Figure 1

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
T_A	Operating temperature	0 to 70	°C
T_{STG}	Storage temperature	-65 to +150	°C
P_D	Package power dissipation[2]	1.6	W
	All input, output, and supply voltages with respect to GND[3]	-.5 to +6	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Current					μA
I_{IL}	Input load	V_{IN} = 0 to 5.25V			10	
I_{LOH}	Output high leakage	ADREN, DBUSEN = 2.2V V_{OUT} = 4V			10	
I_{LOL}	Output low leakage	ADREN, DBUSEN = 2.2V V_{OUT} = 0.45V			10	
	Voltage levels					V
V_{IH}	Input high		2.2		V_{CC}	
V_{IL}	Input low		-0.5		0.8	
V_{OH}	Output high	I_{OH} = -100μA	2.4			
V_{OL}	Output low	I_{OL} = 1.6ma	0.0		0.45	
I_{CC}	Power supply current	V_{CC} = 5.25V $T_A = 0°C$			150	mA
	Capacitance					pf
C_{IN}	Input	V_{IN} = 0V			10	
C_{OUT}	Output	V_{OUT} = 0V			10	

NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and thermal resistance of 50°C/W junction to ambient (40 pin IW package).
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. However, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.

PRELIMINARY SPECIFICATION: Manufacturer reserves the right to make design and process changes and improvements

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$.

PARAMETER		2650A			2650A-1			UNIT
		Min	Typ	Max	Min	Typ	Max	
T_{CH}	Clock high phase	400			250			ns
T_{CL}	Clock low phase	400			250			ns
T_{CP}	Clock period	800			500			ns
T_{PC}	Processor cycle time[5,7]	2400			1500			ns
T_{OR}	OPREQ pulse width[7]	$2T_{CH}+T_{CL}-100$		$2T_{CH}+T_{CL}+50$	$2T_{CH}+T_{CL}-100$		$2T_{CH}+T_{CL}+50$	ns
T_{COR}	Clock to OPREQ time	100		300	100		200	ns
T_{AS}	Address stable	50			50			ns
T_{AD}	Address delay	50	50					ns
T_{CS}	Control signal stable	50			50			ns
T_{DIS}	Data in setup	0			0			ns
T_{DIH}	Data in hold	10			10			ns
T_{DD}	Data out delay	50			50			ns
T_{DS}	Data out stable	50			50			ns
T_{OAS}	OPACK setup time	100			100			ns
T_{OAH}	OPACK hold time	150			150			ns
T_{WPD}	Write pulse delay	100		450	100		300	ns
T_{WPW}	Write pulse width[7]	$T_{CL}-100$		T_{CL}	$T_{CL}-100$		T_{CL}	ns
T_{IRS}	INTREQ setup time			150			150	
T_{IRH}	INTREQ hold time	0			0			
T_{ABD}	Address bus tri-state delay			180			180	ns
T_{DBD}	Data bus tri-state delay			150			150	ns

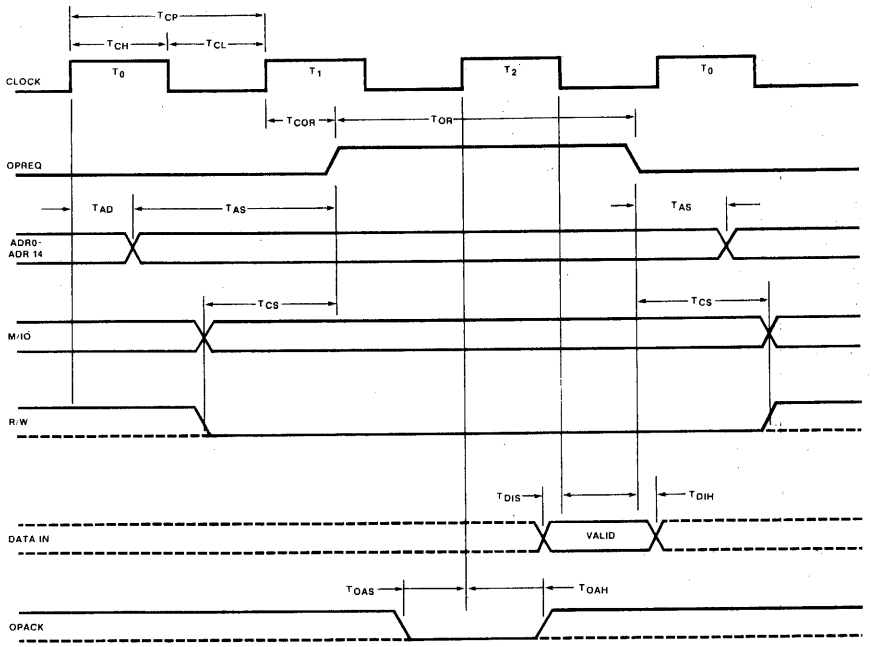
NOTES

1. Input levels swing between 0.80 and 2.2 volts.
2. Input signal transition times are 20ns.
3. Timing reference level is 1.5 volts.
4. Output load is $-100\mu A$ at 100pF and 1 TTL load.
5. Processor cycles time consists of three clock periods.
6. Output buffer rise time is 150ns maximum.
7. These values assume that OPACK is returned in time to not cause the processor to idle. Otherwise, the specified maximum will increase by an integral number of clock cycles.

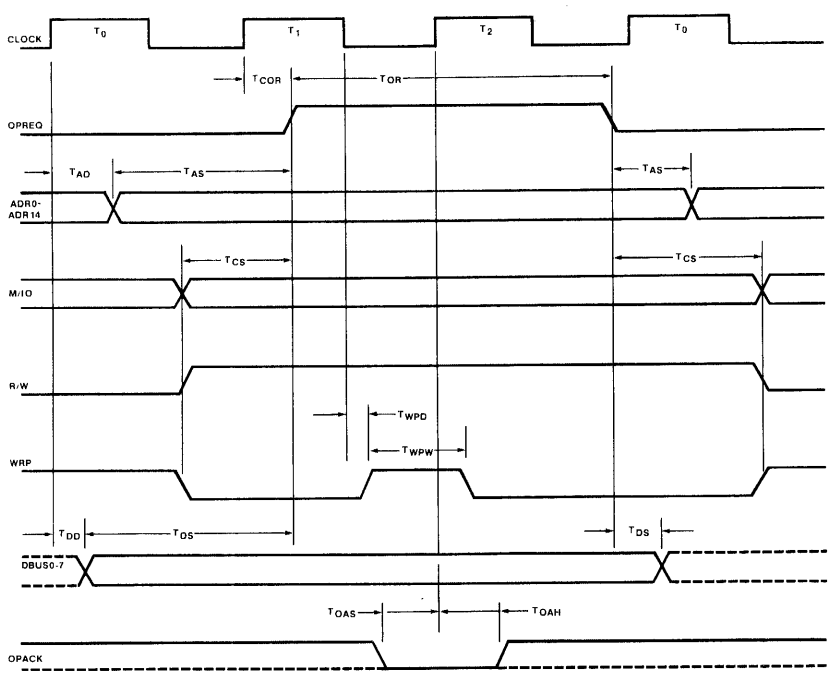
PRELIMINARY SPECIFICATION: Manufacturer reserves the right to make design and process changes and improvements

VOLTAGE WAVEFORMS

READ TIMING

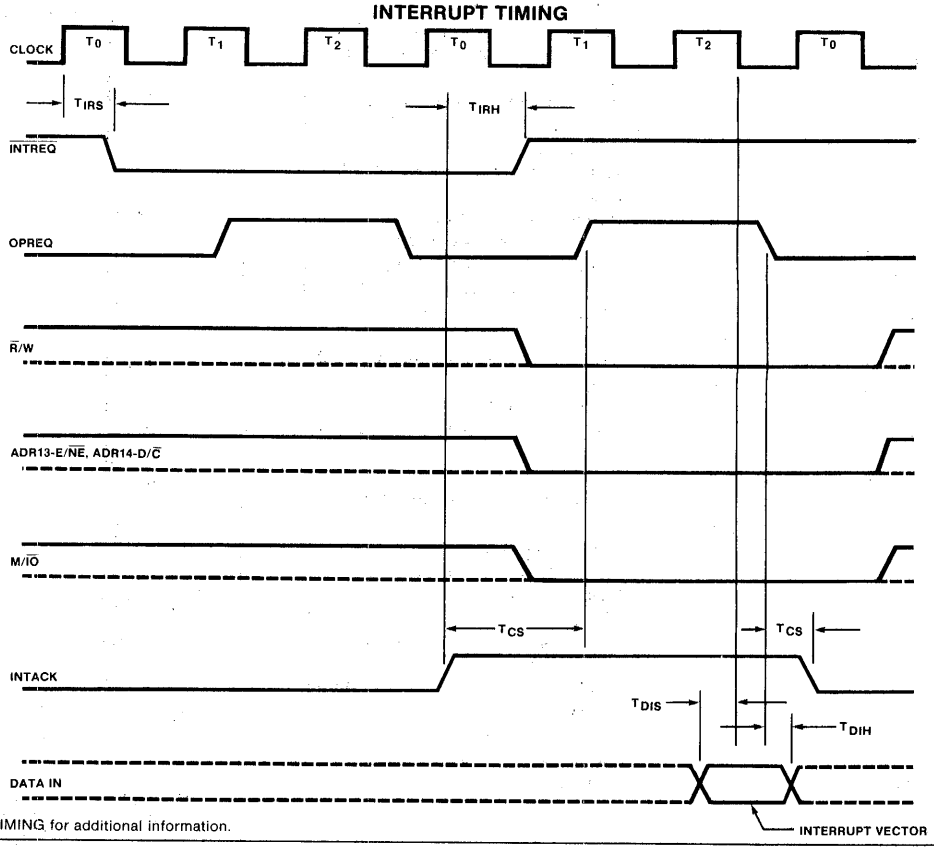


WRITE TIMING



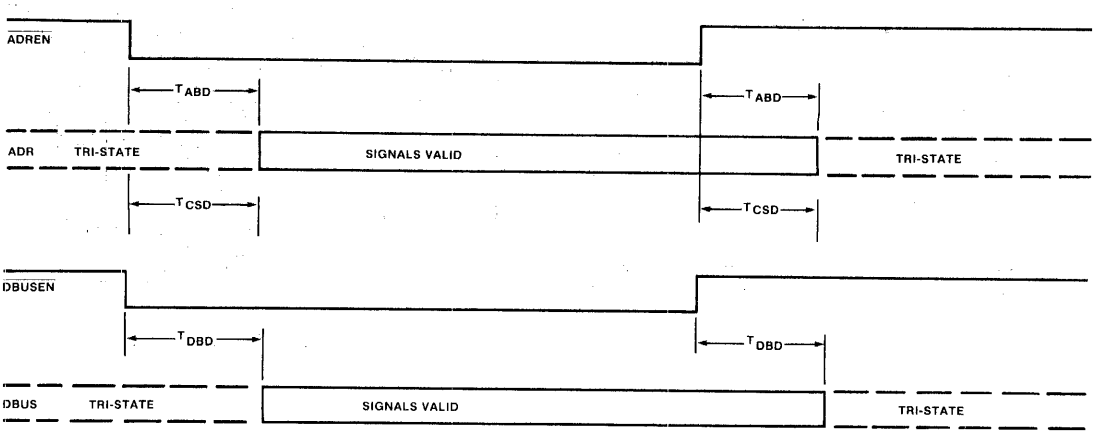
VOLTAGE WAVEFORMS (Cont'd)

INTERRUPT TIMING



NOTE: See READ TIMING for additional information.

TRI-STATE TIMING



DESCRIPTION

SC/MP (Simple Cost-effective MicroProcessor) is a single-chip 8-bit microprocessor packaged in a standard, 40-pin, dual-in-line package.

N-channel, silicon gate, depletion mode standard-process technology ensures high performance, high reliability, and high producibility.

SC/MP is intended for use in general-purpose applications where cost per function is a most significant criterion. But cost efficiency is only a part of SC/MP's story. It goes on to include a variety of useful functions that are not even provided by some of the expensive microprocessors, like self-contained timing circuitry, 16-bit (65K) addressing capability, serial or parallel data-transfer capability and common memory/peripheral instructions. The built-in features in conjunction with the low initial cost describe what SC/MP really is—a microprocessor specifically designed to provide the simplest and most efficient solution to many application requirements.

APPLICATIONS

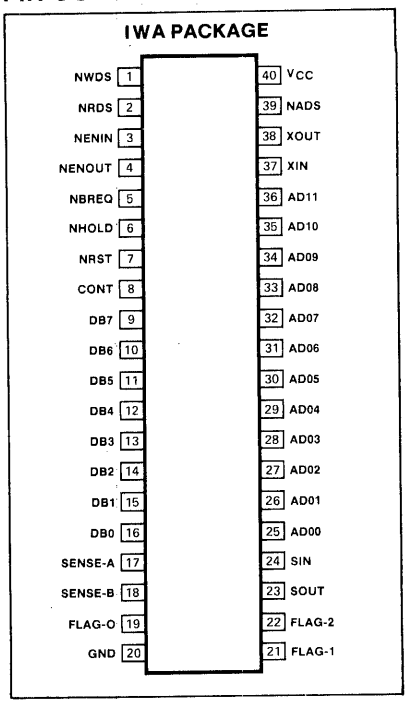
- **Test systems and instrumentation**
- **Machine tool control**
- **Small business machines**
- **Word processing systems**
- **Educational systems**
- **Multiprocessor systems**
- **Process controllers**
- **Terminals**
- **Traffic controls**
- **Laboratory controllers**
- **Sophisticated games**
- **Automotive**

FEATURES

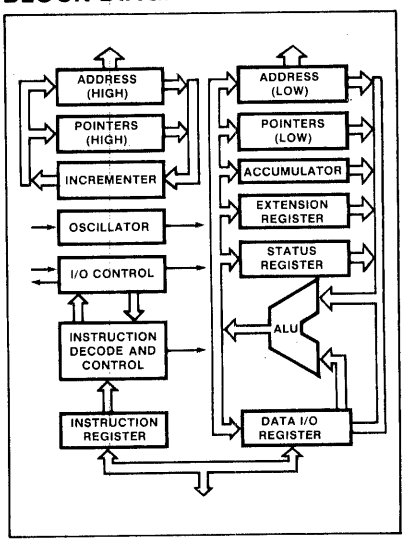
- **Simpler interfacing**
  - **Bidirectional Tri-state 8-bit data bus**
  - **TTL-compatible input/output interface**
- **SI-gate N-channel ion-implant process**
- **Direct Memory Access (DMA) and multiprocessor capabilities**
  - **Handshake bus-access control on chip**
- **Simplified programming**
  - **Multiple addressing modes—program-counter-relative, immediate data, indexed, auto-indexed, and implied**
- **Direct control output**
  - **Three user-accessible control-flag outputs**
- **Simpler I/O hardware**
  - **Separate serial-data input and output ports**
  - **Two sense inputs**
  - **Direct interfacing to standard memory parts**
- **Simplified timing hardware**
  - **On-chip clock generator**
- **Interface flexibility**
  - **Capability to interface with memories or peripherals of any speed**
- **Large system capability**
  - **Address capability to 65K bytes of memory**
- **Simplified power requirements**
  - **Single 5-volt supply**
  - **Low power**

PIN CONFIGURATION

IWA PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

PARAMETER		RATING	UNIT
	Voltage at any pin	-0.5 to +7.0	V
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 10 sec)	+300	°C

*NOTE

Maximum ratings indicate limits beyond which damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under electrical characteristics.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
INPUT SPECIFICATIONS					
All input pins except V_{CC} and GND					
Logic "1" input		2.0		V_{CC}	V
Logic "0" input		-0.5		0.8	V
Capacitance (All pins except V_{CC} and GND)				10	pF
Supply current I_{CC}	$T_A = 25°C$ outputs unloaded			45	mA
	$T_A = 0°C$ outputs unloaded			50	mA
OUTPUT SPECIFICATIONS					
TRI-STATE pins (NWDS, NRDS, DB0-DB7, AD00-AD11)					
Logic "1" output	$I_{OUT} = -100\mu A$	2.4			V
Logic "0" output	$I_{OUT} = 2.0mA$			0.4	V
NADS, FLAG 0-2, SOUT, NENOUT					
Logic "1" output	$I_{OUT} = -100\mu A$	$V_{CC} - 1$			V
Logic "1" output	$I_{OUT} = -1mA$	1.5			V
Logic "0" output	$I_{OUT} = 2.0mA$			0.4	V
NBREQ[1]					
Logic "0" output	$I_{OUT} = 2.0mA$			0.4	V
Logic "1" output	$0 \leq V_{OUT} \leq V_{CC}$			± 10	μA
XOUT					
Logic "1" output	$I_{OUT} = -100\mu A$	2.4			V
Logic "0" output	$I_{OUT} = 1.6mA$			0.4	V

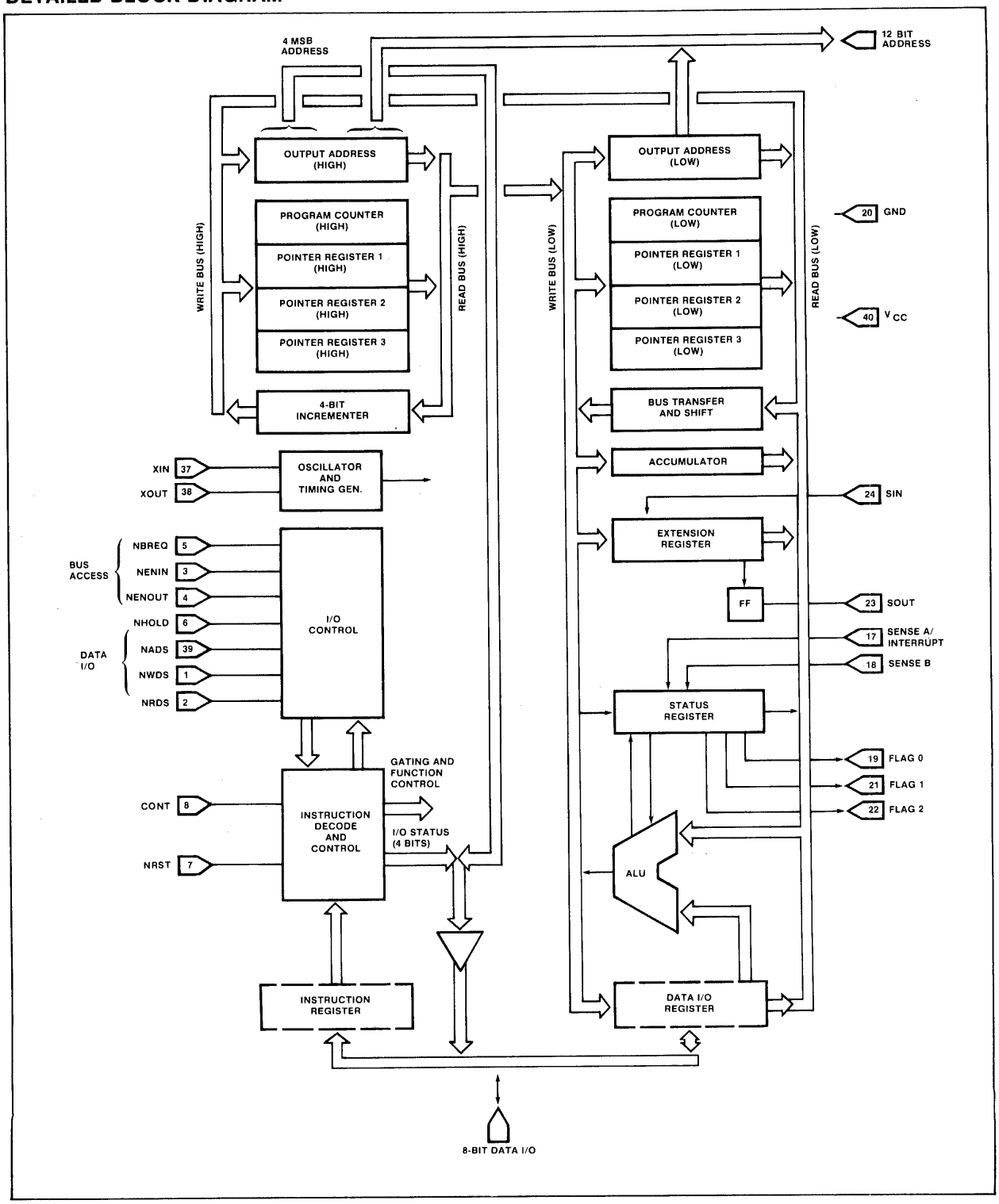
FUNCTIONAL DESCRIPTION

SC/MP is a self-contained general-purpose microprocessor designed for ease of implementation in stand-alone, DMA (Direct Memory Access), and multiprocessor applications. Communications between SC/MP and external memory/peripheral devices are effected via a 12-bit dedicated address bus and an 8-bit bidirectional data bus. During the address interval of each input/output cycle, SC/MP employs both buses to provide a 16-bit address output: the 12 least significant address bits are sent out over the 12-bit address bus and the 4 most significant address bits are sent out over the 8-bit data bus along with 4 status bits. Separate strobe outputs from SC/MP (NADS, NWDS, NRDS) indicate when valid address information is present on the two buses, and when valid input/output memory or peripheral data are present on the 8-bit bus. To further extend flexibility of application, serial data input/output ports are also provided so that serial data transfers can be effected under program control. The remaining input/output signals shown in the Detailed Block Diagram are dedicated to general-purpose control and status functions, including initialization, bus management, microprocessor halt, interrupt request, input/output cycle extension, and user-specified hardware/software interface functions. A detailed description of each input/output signal is provided in Table 1.

*NOTE

NBREQ is an input/output signal that requires an external resistor to V_{CC}.

DETAILED BLOCK DIAGRAM



AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, 1 TTL Load.[1,3]

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
f_X	R = 240Ω ± 5% (Figure 2B) C = 300pF ±10%	0.1 2.0		4.0 4.0	MHz MHz
T_C[2] Microcycle		500 1			ns μs
External clock input T_{W0} T_{W1} XOUT/ADS timing relationship $T_{H(ADS)}$	See Figure 2A See Figure 3	 120 120 100		 225	ns ns
Address and input/output status $T_{D1(ADS)}$ $T_{W(ADS)}$ $T_{S(ADDR)}$ $T_{H(ADDR)}$ $T_{S(STAT)}$ $T_{H(STAT)}$ $T_{H(NBREQ)}$	See Figures 5 and 6	 $(T_C/2) - 50$ $(T_C/2) - 165$ 50 $(T_C/2) - 150$ 50 0		 $3T_C/2$	ns
Data input cycle $T_{D(RDS)}$ $T_{W(RDS)}$ $T_{S(RD)}$ $T_{H(RD)}$ $T_{ACC(RD)}$	See Figure 5	 0 $T_C + 50$ 175 0 $2T_C - 200$			ns
Data output cycle $T_{D(WDS)}$ $T_{W(WDS)}$ $T_{S(WD)}$ $T_{H(WD)}$	See Figure 6	 $T_C - 50$ $T_C - 75$ $(T_C/2) - 200$ 100			ns
Input/output cycle extend $T_{S(HOLD)}$ $T_{D1(HOLD)}$ $T_{D2(HOLD)}$ $T_{W(HOLD)}$ $T_{H(HOLD)}$	See Figure 7	 200 130 0		 275 350 ∞	ns
Bus access $T_{D(NENOUT)}$ $T_{D2(ADS)}$ $T_{H(NENIN)}$	See Figure 4	 $T_C/2$ 0		 150 $3T_C/2$	ns
Output load capacitance XOUT All other output pins				 30 75	pF

NOTES

1. All times measured from valid Logic "0" level = 0.8V or valid Logic "1" level = 2.0V.
2. T_C is the time period for two clock cycles of the on-chip or external oscillator ($T_C = 2/f_X$). Refer to paragraph titled Timing Control for detailed definition.
3. All times measured with a 50% duty cycle on the external clock.

PIN DESIGNATIONS*

SIGNAL MNEMONIC	FUNCTIONAL NAME	DESCRIPTION
NRST	Reset input	Set high for normal operation. When set low, aborts in-process operations. When returned high, internal control circuit zeroes all programmer-accessible registers; then, first instruction is fetched from memory location 0001_{16}.
CONT	Continue input	When set high, enables normal execution of program stored in external memory. When set low, SC/MP operation is suspended (after completion of current instruction) without loss of internal status.
NBREQ	Bus request input/output	Associated with SC/MP internal allocation logic for system bus. Can be used as bus request output or bus busy input. Requires external load resistor to V_{CC}.
NENIN	Enable input	Associated with SC/MP internal allocation logic for system bus. When set low, SC/MP is granted access to system buses. When set high, places system buses in high-impedance (Tri-state) mode.
NENOUT	Enable output	Associated with SC/MP internal allocation logic for system bus. Set low when NENIN is low and SC/MP is not using system buses (NBREQ-high). Set high at all other times.
NADS	Address strobe output	Active-Low strobe. While low, indicates that valid address and status output are present on system buses.
NRDS	Read strobe output	Active-Low strobe. On trailing edge, data are input to SC/MP from 8-bit bidirectional data bus. High-impedance (Tri-state) output when input/output cycle not in progress.
NWDS	Write strobe output	Active-Low strobe. On trailing edge, data are input to SC/MP from 8-bit bidirectional data bus. High-impedance (Tri-state) output when input/output cycle not in progress.
NHOLD	Input/ouput cycle extend input	When set low prior to trailing edge of NRDS or NWDS strobe, stretches strobe to extend input/output cycle; that is, strobe is held low until NHOLD signal is returned high.
SENSE A	Sense/interrupt request input	Serves as interrupt request input when SC/MP internal IE (Interrupt Enable) flag is set. When IE flag is reset, serves as user-designated sense condition input. Sense condition testing is effected by copying status register to accumulator.
SENSE B	Sense input	User-designated sense-condition input. Sense-condition testing is effected by copying status register to accumulator.
SIN	Serial input to E register	Under software control, data on this line are right-shifted into E register by execution of SIO instruction.
SOUT	Serial output from E register	Under software control, data are right-shifted onto this line from E register by execution of SIO instruction. Each data bit remains latched until execution of next SIO instruction.
FLAGS 0, 1, 2	Flag outputs	User-designated general-purpose flag outputs of status register. Under program control, flags can be set and reset by copying accumulator to status register.
AD00-AD11	Address bit 00 through address bit 11	Twelve Tri-state address output lines. SC/MP outputs 12 least significant address bits on this bus when NADS strobe is low. Address bits are then held valid until trailing edge of read (NRDS) or write (NWDS) strobes. After trailing edge of NRDS or NWDS strobe, bus is set to high-impedance (Tri-state) mode until next NADS strobe.

PIN DESIGNATIONS[1] (Cont'd)

MNEMONIC	FUNCTIONAL NAME Output at NADS Time 2,3,4	DESCRIPTION
DB0	Address Bit 12	Fourth most significant bit of 16-bit address.
DB1	Address Bit 13	Third most significant bit of 16-bit address.
DB2	Address Bit 14	Second most significant bit of 16-bit address
DB3	Address Bit 15	Most significant bit of 16-bit address.
DB4	R-Flag	When high, data input cycle is starting; when low, data output cycle is starting.
DB5	I-Flag	When high, first byte of instruction is being fetched.
DB6	D-Flag	When high, indicates delay cycle is starting; that is, second byte of DLY instruction is being fetched.
DB7	H-Flag	When high, indicates that Halt instruction has been executed. (In some system configurations, the H-Flag output is latched and, in conjunction with the Continue input, provides a programmed Halt.)

NOTES

1. The 8-bit bidirectional data bus is set to the high-impedance (tri-state) mode except when it is actually in use by SC/MP (NADS, NRDS, or NWDS low). During the addressing interval of each input/output cycle (NADS low), SC/MP provides address and status outputs over the bus. During the ensuing data-transfer interval (NRDS or NWDS low), 8-bit input or output data bytes are routed over the bus.
2. The DB0 through DB7 (AD12-HFLG) lines are a high-impedance (open circuit) load when SC/MP does not have access to the input/output bus.
3. Input at NRDS time: Input data are expected on the eight (DB0-DB7) lines.
4. Output at NWDS time: Output data are valid on the eight (DB0-DB7) lines.

DRIVERS AND RECEIVERS

Equivalent circuits for SC/MP drivers and receivers are shown in Figure 2. All inputs have static charge protection circuits consisting of an RC filter and voltage clamp. These devices still should be handled with care, as the protection circuits can be destroyed by excessive static charge.

SC/MP-II DRIVER AND RECEIVER EQUIVALENT CIRCUITS

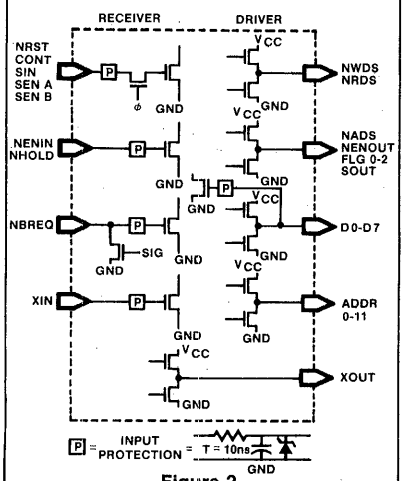


Figure 2

TIMING CONTROL

All necessary timing signals are provided by a three-stage inverter ring oscillator contained on the SC/MP chip. Two control pins, XIN and XOUT, permit the frequency of the oscillator to be controlled by any of the following methods:

1. By leaving the XOUT pin unterminated and driving the XIN pin with an externally generated TTL clock that conforms to the parameters shown in Figure 3A. For this method, the frequency of the oscillator is equalt to the frequency of the external clock input.
2. By connecting a resistor-capacitor feedback network between the XIN and XOUT pins and GND as shown in Figure 3B.
3. By connecting a crystal with low-pass filter network between the XIN and XOUT pins and GND as shown in Figure 3C (for above 1MHz or Figure 3D (for 1MHz or below). For this method, the frequency of the oscillator is equal to the resonant frequency of the crystal and the low-pass filter prevents unwanted harmonic oscillations.

In addition to illustrating appropriate frequency-control networks for the on-chip oscillator, Figures 3A through 3D also show how an optional driver may be used to derive a system clock from the oscillator signal present at the XOUT pin. For reference purposes, the timing relationship between the XOUT signal and the NADS strobe is shown in Figure 5.

In the discussions that follow, instruction execution and input/output timing are described in terms of microcycles.

The time interval of a microcycle is four times the period of the oscillator, that is:

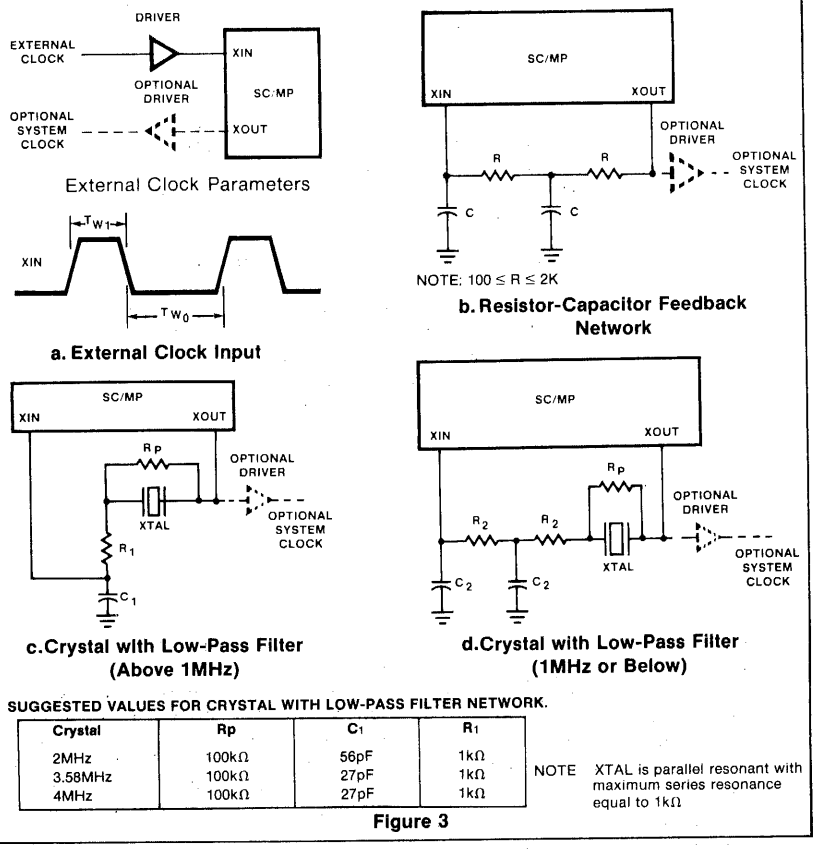
$$\text{period of one microcycle} = 2T_C$$

$$T_C = 2\left(\frac{1}{f_{osc}}\right) = 2\left(\frac{1}{f_{res}}\right) = 2\left(\frac{1}{f_{XIN}}\right)$$

Where:

T_C = time period for two cycles of on-chip or external oscillator
f_{osc} = frequency of on-chip oscillator
f_{res} = resonant frequency of crystal connected between XIN and XOUT pins
f_{XIN} = frequency of external clock applied to XIN pin

TIMING DIAGRAMS



SUGGESTED VALUES FOR CRYSTAL WITH LOW-PASS FILTER NETWORK.

Crystal	Rp	C_1	R_1
2MHz	100kΩ	56pF	1kΩ
3.58MHz	100kΩ	27pF	1kΩ
4MHz	100kΩ	27pF	1kΩ

NOTE XTAL is parallel resonant with maximum series resonance equal to 1kΩ

Figure 3

FREQUENCY CONTROL NETWORKS FOR ON-CHIP OSCILLATOR

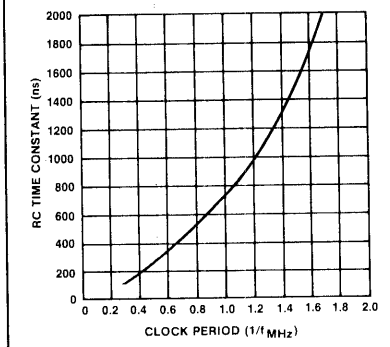


Figure 4

XOUT/NADS TIMING RELATIONSHIP

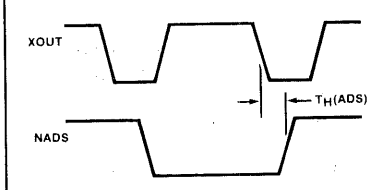


Figure 5

INSTRUCTION FORMAT

The SC/MP instruction repertoire includes both single-byte and double-byte instructions. A single-byte instruction consists of an 8-bit operation code that specifies an operation that SC/MP can execute without further reference to memory. A double-byte instruction consists of an 8-bit operation code and an 8-bit data or displacement field. When the second byte represents a data field, the data are processed by SC/MP during execution of the instruction, thereby eliminating the need for further memory references. When the second byte represents a displacement value, it is used to calculate a memory address that will be accessed (written into or read from) during execution of the instruction (refer to Addressing).

DATA STORAGE

As shown in the Detailed Block Diagram, SC/MP provides ten internal registers, seven of whivh are accessible to the programmer. The purpose and function of these registers are described below.

Program Counter—The program counter is a 16-bit register that contains the address of the instruction being executed. The contents of this register are automatically incremented by one just before each instruction is fetched from memory to enable sequential execution of the stored instructions. Under program control, the contents of this register also may be modified or exchanged with the contents of a pointer register to effect subroutine calls and program branches.

NOTE

The 16-bit address output of the program counter consists of a 4-bit high-order address and a 12-bit low-order address. When the program counter is incremented at the start of each instruction fetch input/output cycle, only the 12 low-order bits are affected; no carry is provided to the 4 high-order bits. For systems employing memories of 4K or less, the high-order bits can be ignored as they are set to 0000_{16} following initialization. For systems employing larger memories, the contents of a pointer register can be modified to select the desired 4K block of memory.

Pointer Registers—The pointer registers are 16-bit general-purpose registers that normally are loaded under program control with reference addresses that serve as page pointers, stack pointers, and subroutine pointers. In applications having minimal memory addressing requirements, these registers may be used alternately as data storage registers.

NOTE

When interrupt requests are enabled, pointer register 3 is automatically referenced by the internal microprogram for formation of the starting address of the user-generated interrupt service routine. (See Figure 10.) In this case, the contents of pointer register 3 must be set to one less than the memory location of the first instruction in the interrupt service routine.

Accumulator—The 8-bit accumulator (AC) is the primary working register of SC/MP. It is used for performing and storing the results of arithmetic and logic operations as well as for data transfers, shifts, rotates, and data exchanges with the program counter, the pointer registers, and the status register.

Extension Register—The extension register is used both for serial input/output data transfers and with the accumulator to effect arithmetic, logic, and data-transfer operations. If the second byte of an indexed or auto-indexed memory reference instruction

(refer to Addressing) equals -128_{10}, the contents of the extension register are used as the displacement value for address formation.

Status Register—The status register provides storage for arithmetic, control, and software status flags. For more detailed information on the function of this register, refer to Status Register under the description of the Arithmetic and Logic Unit.

Instruction Register—The 8-bit instruction register is not accessible to the programmer. During the fetch phase of each instruction cycle, this register is loaded with the 8-bit instruction operation code retrieved from memory (for a single-byte instruction or the first byte of a double-byte instruction).

Data Input/Output Register—The data input/output register is not accessible to the programmer. It is used for temporary storage of all input/output data received via or transmitted over the 8-bit bidirectional data bus during the data-transfer interval of each input/output cycle (NRDS or NWDS low).

Address Register—The 16-bit address register is not accessible to the programmer. It is used for temporary storage of the 16-bit address transmitted during an input/output cycle.

ARITHMETIC AND LOGIC UNIT

The Arithmetic and Logic Unit (ALU) provides the data-manipulation capability that is an essential feature of any microprocessor. The operations provided by the ALU include OR, XOR, increment, decrement, binary addition, and decimal addition. For decimal addition, the data inputs to the ALU are treated as two 4-bit BCD digits, thereby eliminating the program-storage and execution time required to perform BCD to binary conversion.

BUS TRANSFER LOGIC

The bus transfer logic processes the gating and function control outputs of the instruction-decode logic to provide the shift-right (with link, without link, or with serial input data), rotate (with or without link), and bus-exchange functions necessary for data movement between the SC/MP internal read and write buses. A general summary of the data-manipulation capabilities available to the programmer follows.

1. Either the low-order or the high-order byte of any pointer register can be exchanged with the contents of the 8-bit accumulator. Thus, data exchanges between the pointer registers can be effected one byte at a time via the accumulator.

2. The contents of the program counter can be directly exchanged with the contents of any pointer register.

3. The contents of the extension register can be loaded into the accumulator or can be exchanged with the contents of the accumulator. When the accumulator is loaded from the extension register, the original contents of the accumulator are lost.

4. The contents of the status register can be copied into the accumulator to enable status modification or conditional branch testing. When the status register is copied into the accumulator, the contents of the status register are not altered but the original contents of the accumulator are lost.

5. The contents of the accumulator can be copied into the status register to change the outputs of the status register, except for status bits 4 and 5 (Sense A and B inputs to SC/MP). Since these are read-only bits, they are not affected by data movements internal to SC/MP. Copying the accumulator into the status register does not alter the contents of the accumulator.

NOTE

The flag 0, 1, and 2 outputs of the status register serve as latched flags, in other words, they are set to the specified state when the contents of the accumulator are copied into the status register, and they remain in the specified state until the contents of the status register are modified again under program control.

STATUS REGISTER

The function of each bit in the status register is described briefly below.

7	6	5	4	3	2	1	0
CY/L	OV	S_B	S_A	IE	F_2	F_1	F_0

User Flag 0—User-assigned general-purpose status bit for implementation as software status bit or in system control applications. This status bit is available as an external output from SC/MP.

User Flag 1—Same as User Flag 0.

User Flag 2—Same as User Flag 0.

Interrupt Enable Flag—Internal status bit that is set and reset under program control. When set, SC/MP recognizes external interrupt requests received via Sense A input. When reset, inhibits SC/MP from recognizing interrupt requests.

Sense A—General purpose status input for sensing external conditions. When IE flag is reset, this bit can be tested by copying status register to accumulator. When IE flag is set, this bit serves as interrupt request input causing SC/MP to automatically branch to user-generated interrupt-service routine in response to high input.

Sense B—Same as Sense A except that it is not tested for interrupt status.

NOTE

Sense A and B inputs are read-only bits. Thus, they are not affected when the contents of the accumulator are copied into the status register.

Overflow (OV)—This bit is set if an arithmetic overflow occurs during an add (ADD, ADI, or ADE) or a complement-and-add instruction (CAD, CAI, or CAE). It is not affected by the decimal-add instructions (DAD, DAI, or DAE).

Carry/Link (CY/L)—This bit is set if a carry from the most significant bit occurs during an add, complement-and-add, or decimal-add instruction. Thus, it serves as a carry input to the next add instruction. In addition, it is included in the Shift Right with Link (SRL) and Rotate Right with Link (RRL) instructions.

CONTROL

The operation of the SC/MP microprocessor consists of repeatedly accessing or fetching instructions from the program stored in external memory and executing the operations specified by the instructions. These two steps are carried out under the control of an internal microprogram. (SC/MP is not user-microprogrammable.) The microprogram is similar to a state table specifying the series of states of system control signals necessary to carry out each instruction. Microprogram storage is provided in the instruction decode and control logic, and microprogram routines are implemented to fetch and execute instructions. The fetch routine first increments the program counter, and then causes the instruction address to be transferred from the program counter to the system buses via the output address register. The microprogram next initiates an input data transfer. When the instruction operation code is subsequently placed on the 8-bit data bus (single-byte instruction or first byte of double-byte instruction), the operation code is loaded into the instruction register. The operation code is then partially decoded to determine whether the instruction contains a second byte. If it does, a second input data transfer is effected to load the next byte in the data input/output register.

After the complete instruction is stored in the instruction and/or data input/output register(s), the instruction decoder transforms the instruction operation code into the address of the appropriate instruction-execution routine contained in the internal microprogram. The microprogram then branches to the specified internal address to initiate execution of the instruction. The

resulting execution routine comprises one or more microinstructions that implement the required functions. For example, the first microcycle of an Extension Register Add Instruction (ADE) causes the contents of the extension register to be gated onto the read bus, transferred to the write bus via the bus control logic, and then written into the data input/output register. The next microcycle causes the contents of the accumulator to be gated onto the read bus, the contents of the read bus to be added to the contents of the data input/output register via the ALU, and the resultant output of the ALU to be written into the accumulator via the write bus. The final step of the execution routine is a jump back to the fetch routine to access the next instruction.

INITIALIZATION

Since SC/MP may power up in a random condition, the following power-up and initialization procedure is recommended.

1. Apply power (GND and V_{CC}) and set NRST low.

NOTE

Allow ample time (typically, 250ms) for the oscillator and the internal clocks to stabilize. In systems where NRST is set low after turning on power, NRST must remain low for a minimum of $4T_C$. While NRST is low, any in-process operations are aborted automatically. When NRST is low, strobes and address and data buses are in the Non-I/O state (high-Z state).

2. Set NRST high. If the rise time of this input is too slow, the processor, first, will initialize and execute a few instructions and, then, will reinitialize. If the application is such that multiple initialization is undesireable, NRST should be brought high at a minimum rate of 2 volts per microcycle.

NOTE

This causes the SC/MP internal control circuit to set the contents of all programmer-accessible registers to zero. Thus, when SC/MP is granted access to the system buses following initialization, the first instruction is fetched *always* from memory location 0001_{16}. The NBREQ output goes low, indicating the start of this input/output cycle; this occurs at a time within $13T_C$ after NRST is set high. Normal execution of the program continues as long as NRST remains high.

PARALLEL DATA TRANSFERS

Parallel data transfers occur during each instruction fetch and during the ensuing read/write cycle associated with execution of the memory-reference instructions. This class of instruction could perhaps more properly be called the "Input/Output Reference Class" in the case of the SC/MP microprocessor, since all data tranfers, whether with memory, peripheral devices, or a central processor data bus, occur through the execution of these instructions. This unified bus structure is in contrast with many other microprocessors and minicomputers that have one instruction type (input/output class) for communication with peripheral devices and another instruction type (memory reference class) for communication with memories. The advantage of the approach taken by SC/MP is that a wider variety of instructions (the entire memory-reference class) is available for communications with peripherals. Thus, the LD and ST (Load and Store) instructions can be used for basic transfers, the ILD and DLD (increment/decrement and load) instructions can be used for indexing peripheral registers, and the remaining memory reference instructions can be used, as required, for "one-step" retrieval and processing of peripheral input data.

BUS UTILIZATION

The bus utilization of SC/MP is shown in Table 2.

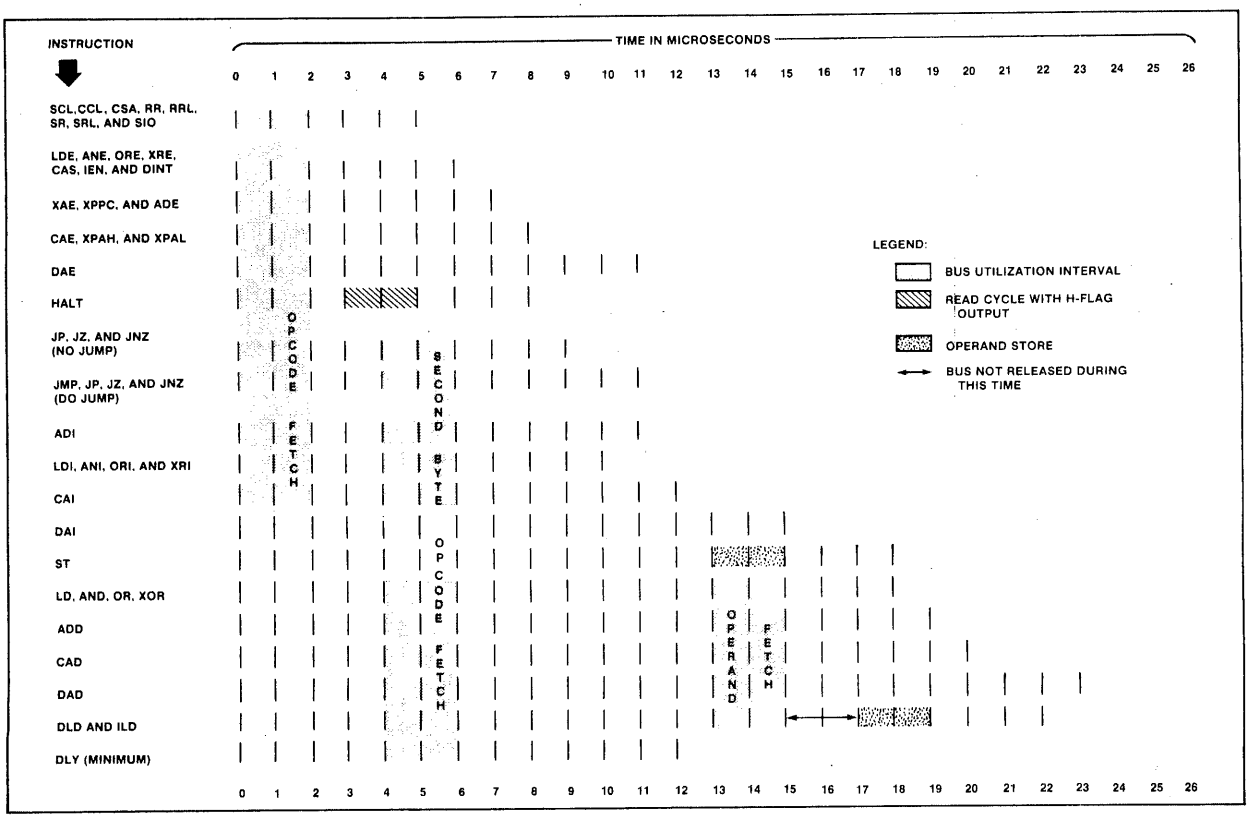


Table 2 BUS UTILIZATION OF EACH INSTRUCTION

NBREQ, NENIN, and NENOUT are active and bus access is controlled as shown in Figure 5. If NENIN is returned high during an input/output cycle, the input/output cycle is repeated when NENIN is again returned low.

During an ILD or DLD instruction, SC/MP does not relinquish the bus between the loading of the data and the storing of the modified data. If NENIN is brought high after the data have been loaded, the load portion of the cycle is not repeated when NENIN is returned low.

BUS ACCESS

Before SC/MP can initiate parallel data transfers with memory or peripheral devices, it must have access to the system address and data buses. Three of the SC/MP input/output signals are associated with bus control: NBREQ, NENIN, and NENOUT. For simple stand-alone applications, the NENOUT signal can be ignored and the NENIN signal can be tied to GND to allow the SC/MP microprocessor to have continual access to the system buses. The NBREQ input/output line then goes low during each input/output cycle as shown in Figures 6 and 7 to indicate when SC/MP is actually using the system buses.

NOTE

The NBREQ input/output line must be tied to V_{CC} via an external load resistor to allow normal operation of the SC/MP microprocessor.

For DMA and multiprocessor applications, the NBREQ, NENIN, and NENOUT signals can be interconnected in various configurations to allow bus access to be granted to requesting devices according to user-specified priorities. Figure 5 illustrates the general sequence in which these signals are processed by SC/MP to gain access to the system buses and to indicate when the buses are actually being used.

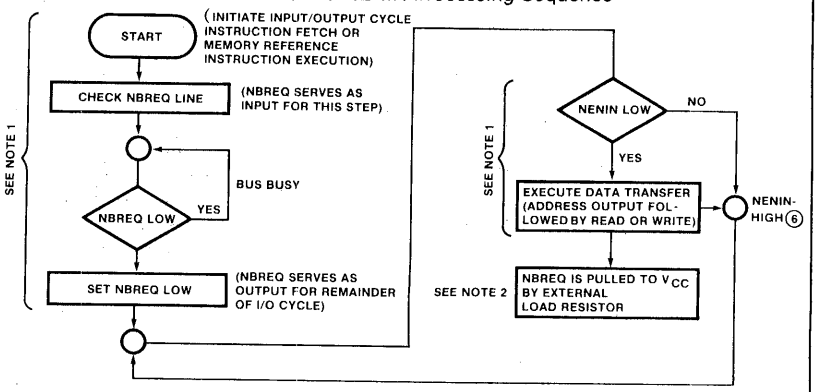
INPUT/OUTPUT CYCLE

Once SC/MP has control of the system buses, the actual input/output cycle begins. As shown in Figures 6 and 7, the functions of memory addressing, data reading, and data writing are implemented, respectively, by the address strobe (NADS), the read strobe (NRDS), and the write strobe (NWDS). Note that the NBREQ signal is reset high at the end of the input/output cycle to indicate that the system buses are now free for use by the highest-priority requesting device.

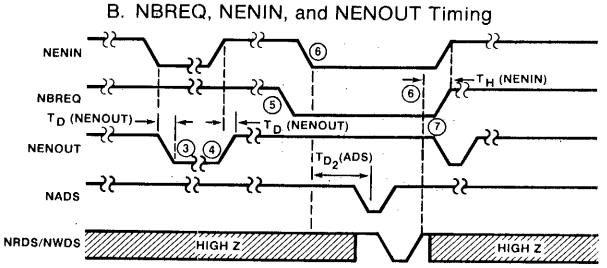
The first operation that SC/MP performs for each input/output cycle is to load the 12 least significant address bits onto the 12-bit address bus, and the 4 most significant

BUS ACCESS CONTROL

A. NBREQ and NENIN Processing Sequence



B. NBREQ, NENIN, and NENOUT Timing

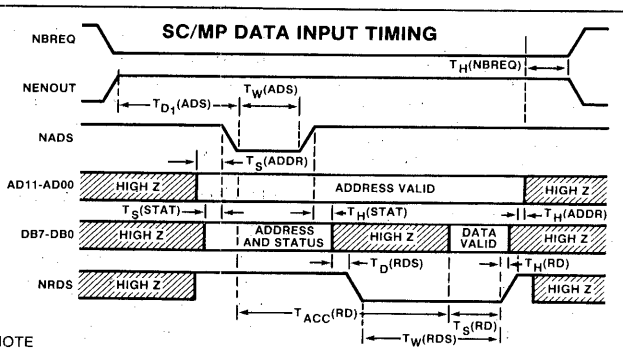


NOTES

1. NENOUT is always high while SC/MP is actually using bus; that is, NENIN input and NBREQ output are low.
2. When SC/MP is not using bus (NBREQ output or NENIN input high), NENOUT is held in same state as NENIN input.
3. NENOUT goes low to indicate that SC/MP was granted access to bus (NENIN low) but is not using bus.
4. NENOUT goes high in response to high NENIN input.
5. SC/MP generates bus request; bus access not granted because NENIN high.
6. NENIN goes low. Bus access now granted and input/output cycle actually initiated. If NENIN is set high while SC/MP has access to the bus, the address and data ports will go to the high-impedance (Tri-State) state, but NBREQ will remain low. When NENIN is subsequently set low, the input/output cycle will begin again.
7. Input/output cycle completed. NENOUT goes low to indicate that SC/MP granted access to bus but not using bus. If NENIN had been set high before completion of input/output cycle. NENOUT would have remained high.

Figure 5

SC/MP DATA INPUT TIMING



NOTE

Timing is valid when NENIN is low before NBREQ is set low by SC/MP; see Figure 5 for NADS timing when NENIN is set low after NBREQ.

Figure 6

address bits along with 4 status bits onto the 8-bit data bus. At the same time, SC/MP sets the NADS output low to indicate that the address and the status information are valid. The low-order address on the 12-bit bus is then held valid for the duration of the input/output cycle; the high-order address and the status information on the 8-bit bus remain valid only while NADS is low. While valid, the status bits have the following significance:

RFLG—When high, indicates that input/output cycle is read cycle; when low, indicates that input/output cycle is write cycle.

IFLG—Set high to indicate that instruction operation code (single-byte instruction or first byte of double-byte instruction) will be output from memory following NADS.

DFLG—Set high only when second byte of Delay Instruction is to be read from memory following NADS. Execution of the Delay Instruction then starts at trailing edge of NRDS. Upon completion, SC/MP provides NADS output to initiate next input/output cycle if bus access is granted. Time in microcycles from leading edge of delay flag to leading edge of subsequent NADS output is computed from the following formula:

Delay = [9 + 2(AC) + 2 disp + 2^9 disp] microcycles

where:
(AC) = unsigned contents of accumulator
disp = unsigned displacement value contained in second byte of Delay Instruction

The time derived from the above formula does not include the four microcycles required to fetch the first byte of the Delay Instruction. Thus, when the Delay Instruction is used for software timing, total instruction execution time equals [13 + 2(AC) + 2 disp + 2^9 disp] microcycles.

NOTE

When Halt Instruction is executed, instruction decode and control logic inhibits incrementing of program counter for one input/output cycle. Thus, Halt Instruction is read from memory a second time to enable generation of HFLG output, but no further processing of Halt Instruction occurs. In effect, this procedure ensures HFLG is output in advance of the next instruction to be fetched from memory.

HFLG—Set high only during addressing interval of read cycle that follows Halt Instruction. HFLG may be used to cause user-provided external logic to set the CONT input low, and thereby to effect a programmed halt. Since HFLG read cycle precedes the next instruction fetch, termination of programmed halt enables fetch of first instruction that follows Halt Instruction.

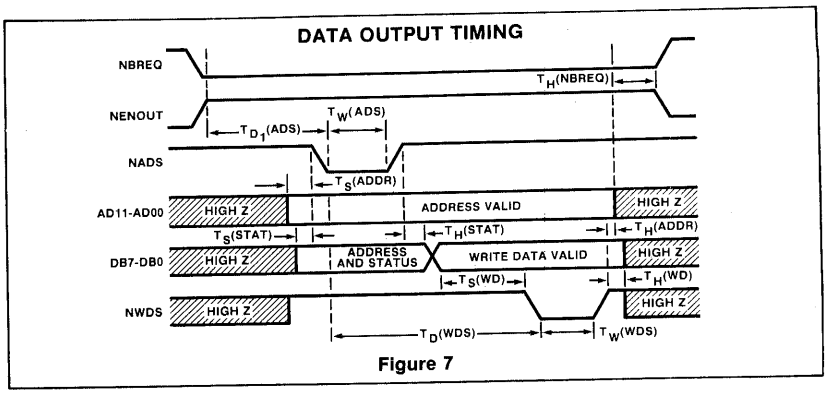
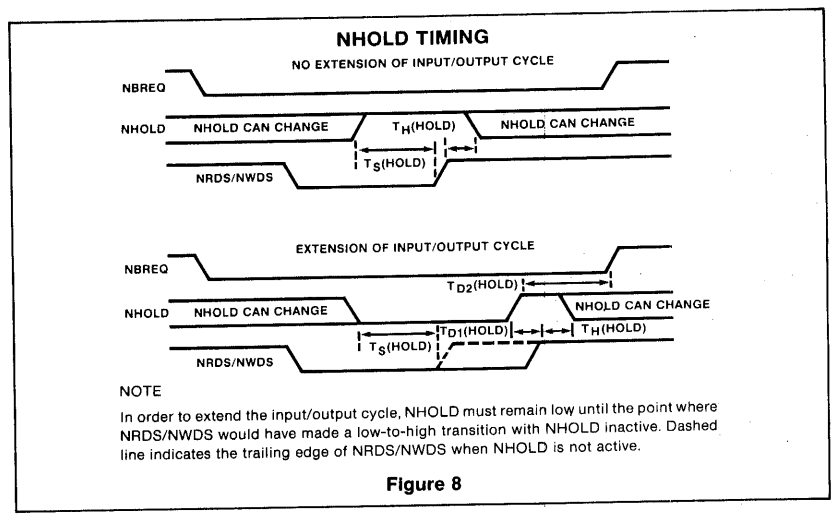


Figure 7



NOTE

In order to extend the input/output cycle, NHOLD must remain low until the point where NRDS/NWDS would have made a low-to-high transition with NHOLD inactive. Dashed line indicates the trailing edge of NRDS/NWDS when NHOLD is not active.

Figure 8

After resetting the NADS output, SC/MP generates an NRDS or NWDS strobe, respectively, to initiate a data-input (read) or data-output (write) operation. For a read operation, input data are strobed into SC/MP from the 8-bit bus on the trailing edge of the NRDS strobe. For a write operation, SC/MP places valid output data on the 8-bit bus on the leading edge of the NWDS strobe. After resetting the NRDS or NWDS strobe to complete the data transfer, SC/MP then resets the NBREQ signal to indicate that the system buses are free for use by another controller.

INPUT/OUTPUT CYCLE EXTENSION

As shown in Figure 8, the NHOLD signal may be set low prior to the trailing edge of the NRDS or NWDS strobe to cause SC/MP to lengthen the input/output cycle by holding the strobe active until after the NHOLD signal is returned high. Since there is no restriction on the maximum duration of the NHOLD signal, it can be used in a variety of applications ranging from accommodation of memories/peripherals with long access times to single-cycle control of the operating program for software debug purposes.

Figure 9 illustrates a typical circuit that may be used to generate an NHOLD signal of repeatable duration. The circuit shown employs an N74165 8-Bit Parallel In/Serial Out Shift Register to allow selection of an input/output cycle extend time that ranges from $T_C/2$ to $2T_C$ in increments of $T_C/2$. Functional operation of the circuit is controlled by the NADS strobe and XOUT signals. Each time that the NADS strobe goes low, the data present at the A through H terminals are loaded into the shift register in parallel. When the NADS strobe subsequently returns high, the data are then shifted out serially on the positive-to-negative transitions of XOUT. Thus, the NHOLD output of the circuit is set low on the leading edge of each NADS strobe and, as shown in the chart that accompanies the circuit diagram, it remains low for a time period ranging from three clock cycles minimum (B, C,

D, and E inputs = Logic "1") to seven clock cycles maximum (B, C, D, and E inputs = Logic "0").

It is important to note that instruction execution time is increased whenever an input/output cycle is extended via the NHOLD signal. For purposes of computing the increase in instruction execution time, it is necessary to distinguish between the terms Input/Output Cycle Delay Period and Input/Output Cycle Extend Time. The term Input/Output Cycle Delay Period refers to the time that the NRDS/NWDS strobe is actually "stretched" to provide the required memory or peripheral access time. The term Input/Output Cycle Extend Time refers to the additional number of microcycles required by the internal SC/MP microprogram to complete the extended input/output cycle; that is:

INPUT/OUTPUT CYCLE	
Delay Period	**Extend Time**
$T_C/2$ through $2T_C$ (> 0 ≤ 1μcycle)	1μcycle
$5T_C/2$ through $4T_C$ (> 1 ≤ 2μcycles)	2μcycles
$9T_C/2$ through $6T_C$ (> 2 ≤ 3μcycles)	3μcycles
etc.	etc.

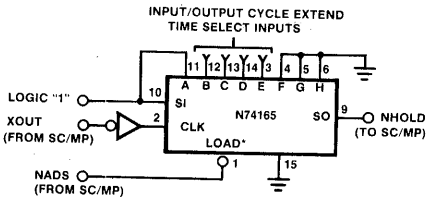
The total increase in instruction execution time, therefore, is equal to the Input/Output Cycle Extend Time multiplied by the total number of input/output cycles associated with the instruction. For example, a DLD Instruction is normally executed in 22 microcycles. Since this instruction employs three read input/output cycles and one write input/output cycle, an Input/Output Cycle Extend Time of one microcycle would increase total DLD Instruction execution time to 26 microcycles.

SERIAL DATA TRANSFERS

Serial input/output data transfers can be used efficiently with very slow input/output peripherals such as X-Y plotters, teletypewriters, slow-speed printers, and so forth. Such transfers can be effected in any of the following manners:

1. By assigning serial input/output functions to the extension register via the SIO (Serial Input/Output) Instruction. When this instruction is executed, the contents of the extension register are shifted right one bit. At the same time, data present on the SIN line are shifted into bit position 7 of the extension register and the original contents of bit position 0 are shifted into a flip-flop to provide a latched output of the SOUT line. The SOUT data are then held latched until the next SIO instruction is executed.

TYPICAL NHOLD CONTROL CIRCUIT



DATA INPUTS B C D E	NHOLD DURATION (in clock cycles)	INPUT/OUTPUT CYCLE		REQUIRED MEMORY ACCESS TIME [T_{ACC} (RD)]
		DELAY PERIOD	EXTEND TIME IN MICROCYCLES	
1 1 1 1	3	0	0	$2T_C$ - 200
1 1 1 0	4	$T_C/2$	1	$(5T_C/2)$ - 200
1 1 0 0	5	T_C	1	$3T_C$ - 200
1 0 0 0	6	$3T_C/2$	1	$(7T_C/2)$ - 200
0 0 0 0	7	$2T_C$	1	$4T_C$ - 200

Figure 9

2. By using one of the status flags as an output data bit and one of the sense lines as an input data bit.

3. By implementing external logic such that only one line of the 8-bit data input/output bus is used.

For synchronous systems, serial data input/output timing may be provided by program loops that employ the delay instruction, or by using one or more of the transfer instructions (see Table 2) to test the output of an external timing circuit. For asynchronous systems, one of the sense inputs can be used for testing bit-received/ready status and a pulsed flag output can be provided, under program control, for peripheral indexing each time that a data bit is actually shifted in or out.

Systems that have several input/output devices must be multiplexed, device selection can then be accomplished using the status flag outputs of SC/MP, or by using parallel input/output commands to load an external latch. Systems that do not require serial input/output capability can employ the SIN and SOUT lines as a sense input and flag output, respectively.

INTERRUPTS

When the internal interrupt enable (IE) flag is set under program control, the Sense A line is enabled to serve as an interrupt request input; when the IE flag is reset, SC/MP is inhibited from detecting interrupts. Thus, while the IE flag is set, the Sense A input is tested prior to the fetch phase of each instruction as shown in Figure 10. Upon detection of an interrupt request (Sense A high), the following events occur automatically.

MICROPROCESSOR HALT AND INTERRUPT REQUEST INPUT PROCESSING

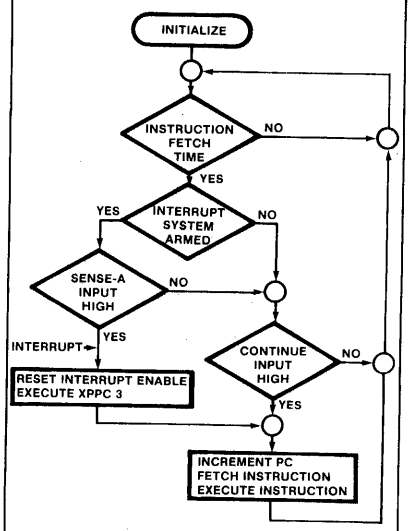


Figure 10

1. The status register IE flag is reset to prevent SC/MP from responding to any further interrupt requests. Interrupt request capability can then be reenabled during or at the end of the ensuing user-generated interrupt service routine via the IEN (Enable Interrupt) Instruction or by copying the accumulator into the status register.

2. The contents of the program counter are exchanged with the contents of the pointer register 3.

3. The contents of the program counter are incremented by one to address the first instruction of the user-generated interrupt service routine.

The interrupt system must be armed before interrupts are enabled. This is accomplished as follows:

1. First, the Interrupt Enable Bit in the Status Register is set true by executing either an Enable Interrupt Instruction (IEN) or a Copy Accumulator to Status Register Instruction (CAS).
2. Second, one additional instruction is fetched and executed.

A return from interrupt is accomplished by executing two instructions: Enable Interrupt (IEN) immediately followed by Exchange Pointer 3 with Program Counter (XPPC 3).

MICROPROCESSOR HALT

The CONT input to SC/MP is provided to enable suspension of operation without loss of internal status. Processing of the CONT input is shown in Figure 9. Since this is an asynchronous input, it can be controlled by external timing logic, or as stated previously, the HALT flag output that appears on the 8-bit data bus (during the read cycle that follows execution of a Halt Instruction) can be used with an external circuit to effect a programmed halt condition. Note that when an interrupt request is detected while the CONT input is low, the first instruction of the user-generated interrupt service routine is automatically executed. Thus, the first instruction of the interrupt service routine can be used to reset the external CONT input logic and, thereby, to terminate the microprocessor halt condition if so desired.

After execution of an instruction, the CONT input must be high for a minimum time of $2T_C$ (1 microcycle) in order to fetch and execute the next instruction.

INSTRUCTION SET

The SC/MP instruction set provides the general-purpose user of microprocessors a powerful programming capability along with above-average flexibility and speed. The instruction set consists of 46 instructions, which comprise eight general categories. A listing of the complete instruction set is provided in Table 2; typical instruction execution times are given in Table 3, and notations and symbols used as shorthand expressions of instruction capability are defined in Table 4.

DOUBLE-BYTE INSTRUCTIONS

MNEMONIC	DESCRIPTION	OBJECT FORMAT	OPERATION	MICRO-CYCLES
	Memory reference instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
LD	Load	1 1 0 0 0 m ptr | disp	(AC)←(EA)	18
ST	Store	1 1 0 0 1	(EA)←(AC)	18
AND	AND	1 1 0 1 0	(AC)←(AC) Λ (EA)	18
OR	OR	1 1 0 1 1	(AC)←(AC) V (EA)	18
XOR	Exclusive-OR	1 1 1 0 0	(AC)←(AC) ∀ (EA)	18
DAD	Decimal add	1 1 1 0 1	$(AC)\leftarrow(AC)_{10}+(EA)_{10}+(CY/L)$; (CY/L)	23
ADD	Add	1 1 1 1 0	(AC)←(AC) + (EA) + (CY/L); (CY/L), (OV)	19
CAD	Complement and add	1 1 1 1 1	(AC)←(AC) + ~(EA) + ((CY/L); (CY/L), (OV)	20
	Memory increment/ decrement instructions	7 6 5 4 3 2 | 1 0 | 7 6 5 4 3 2 1 0		
ILD	Increment and load	1 0 1 0 1 0 | ptr | disp	(AC), (EA)←(EA) + 1	22
DLD	Decrement and load	1 0 1 1 1 0	(AC), (EA)←(EA) - 1	22
	Immediate instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
LDI	Load immediate	1 1 0 0 0 1 0 0 | data	(AC)←data	10
ANI	AND immediate	1 1 0 1 0 1 0 0	(AC)←(AC) Λ data	10
ORI	OR immediate	1 1 0 1 1 1 0 0	(AC)←(AC) V data	10
XRI	Exclusive-OR immediate	1 1 1 0 0 1 0 0	(AC)←(AC) ∀ data	10
DAI	Decimal add immediate	1 1 1 0 1 1 0 0	$(AC)\leftarrow(AC)_{10}+data_{10}+(CY/L)$; (CY/L)	15
ADI	Add immediate	1 1 1 1 0 1 0 0	(AC)←(AC) + data + (CY/L); (CY/L), (OV)	11
CAI	Complement and add immediate	1 1 1 1 1 1 0 0	(AC)←(AC) + ~data + (CY/L); (CY/L), (OV)	12
	Transfer instructions	7 6 5 4 3 2 | 1 0 | 7 6 5 4 3 2 1 0		
JMP	Jump	1 0 0 1 0 0 | ptr | disp	(PC)←EA	11
JP	Jump if positive	1 0 0 1 0 1	If (AC) ≥ 0, (PC)←EA	9, 11
JZ	Jump if zero	1 0 0 1 1 0	If (AC) = 0, (PC)←EA	9, 11
JNZ	Jump if not zero	1 0 0 1 1 1	If (AC) ≠ 0, (PC)←EA	9, 11
	Double-byte miscellaneous instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
DLY	Delay	1 0 0 0 1 1 1 1 | disp	count AC to -1. delay = 13 + 2(AC) + 2 disp + 2^9 disp microcycles	13 to 131, 593

Table 3 SC/MP INSTRUCTION SUMMARY

SINGLE-BYTE INSTRUCTIONS				
MNEMONIC	**DESCRIPTION**	**OBJECT FORMAT**	**OPERATION**	**MICRO-CYCLES**
	Extension register instructions	7 6 5 4 3 2 1 0		
LDE	Load AC from extension	0 1 0 0 0 0 0 0	(AC)←(E)	6
XAE	Exchange AC and extension	0 0 0 0 0 0 0 1	(AC)←(E)	7
ANE	AND extension	0 1 0 1 0 0 0 0	(AC)←(AC) $\wedge$ (E)	6
ORE	OR extension	0 1 0 1 1 0 0 0	(AC)←(AC) V (E)	6
XRE	Exclusive-OR extension	0 1 1 0 0 0 0 0	(AC)←(AC) $\forall$ (E)	6
DAE	Decimal add extension	0 1 1 0 1 0 0 0	$(AC)\leftarrow(AC)_{10}+(E)_{10}+(CY/L)$; (CY/L)	11
ADE	Add extension	0 1 1 1 0 0 0 0	(AC)←(AC)+(E)+(CY/L); (CY/L), (OV)	7
CAE	Complement and add extension	0 1 1 1 1 0 0 0	(AC)←(AC)+$\bar{}$(E)+(CY/L); (CY/L), (OV)	8
	Pointer register move instructions	7 6 5 4 3 2 1 0		
XPAL	Exchange pointer low	0 0 1 1 0 0 ptr	$(AC)\leftarrow(PTR_{7:0})$	8
XPAH	Exchange pointer high	0 0 1 1 0 1	$(AC)\leftarrow(PTR_{15:8})$	8
XPPC	Exchange pointer with PC	0 0 1 1 1 1	(PC)←(PTR)	7
	Shift, rotate, serial I/O instructions	7 6 5 4 3 2 1 0		
SIO	Serial input/output	0 0 0 1 1 0 0 1	$(E_i)\rightarrow(E_{i-1})$, SIN→$(E_7)$, (E_0)→SOUT	5
SR	Shift right	0 0 0 1 1 1 0 0	$(AC_i)\rightarrow(AC_{i-1})$, 0→$(AC_7)$	5
SRL	Shift right with link	0 0 0 1 1 1 0 1	$(AC_i)\rightarrow(AC_{i-1})$, (CY/L)→$(AC_7)$	5
RR	Rotate right	0 0 0 1 1 1 1 0	$(AC_i)\rightarrow(AC_{i-1})$, $(AC_0)\rightarrow(AC_7)$	5
RRL	Rotate right with link	0 0 0 1 1 1 1 1	$(AC_i)\rightarrow(AC_{i-1})$, (AC_0)→(CY/L)→(AC_7)	5
	Single-byte miscellaneous instructions	7 6 5 4 3 2 1 0		
HALT	Halt	0 0 0 0 0 0 0 0	Pulse H-flag	8
CCL	Clear carry/link	0 0 0 0 0 0 1 0	(CY/L)←0	5
SCL	Set carry/link	0 0 0 0 0 0 1 1	(CY/L)←1	5
DINT	Disable interrupt	0 0 0 0 0 1 0 0	(IE)←0	6
IEN	Enable interrupt	0 0 0 0 0 1 0 1	(IE)←1	6
CSA	Copy status to AC	0 0 0 0 0 1 1 0	(AC)←(SR)	5
CAS	Copy AC to status	0 0 0 0 0 1 1 1	(SR)←(AC)	6
NOP	No operation	0 0 0 0 1 0 0 0	None	5

Table 3 SC/MP INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	READ CYCLES	WRITE CYCLES	TOTAL MICROCYCLES
ADD	3	0	19
ADE	1	0	7
ADI	2	0	11
AND	3	0	18
ANE	1	0	6
ANI	2	0	10
CAD	3	0	20
CAE	1	0	8
CAI	2	0	12
CAS	1	0	6
CCL	1	0	5
CSA	1	0	5
DAD	3	0	23
DAE	1	0	11
DAI	2	0	15
DINT	1	0	6
DLD	3	1	22
DLY	2	0	13 - 131593
HALT	2	0	8
IEN	1	0	6
ILD	3	1	22
JMP	2	0	11
JNZ	2	0	9,11 for Jump
JP	2	0	9,11 for Jump
JZ	2	0	9,11 for Jump
LD	3	0	18
LDE	1	0	6
LDI	2	0	10
NOP	1	0	5
OR	3	0	18
ORE	1	0	6
ORI	2	0	10
RR	1	0	5
RRL	1	0	5
SCL	1	0	5
SIO	1	0	5
SR	1	0	5
SRL	1	0	5
ST	2	1	18
XAE	1	0	7
XOR	3	0	18
XPAH	1	0	8
XPAL	1	0	8
XPPC	1	0	7
XRE	1	0	6
XRI	2	0	10

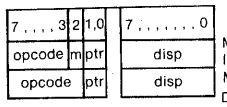
NOTE

If slow memory is being used, the appropriate delay should be added for each read or write cycle.

Table 4 INSTRUCTION EXECUTION TIME

ADDRESSING

During execution, instructions and data defined in a program are stored into and loaded from specific memory locations, the accumulator, or selected registers. Because SC/MP, memory (read/write and read-only), and peripherals are on a common data bus, any instruction used to address memory may be used to address the peripherals. The formats of the instruction groups that reference memory are shown below.



Memory Reference Instructions
Memory Increment/ Decrement Instructions and Transfer Instructions

Memory-reference instructions use the PC-relative, indexed, or auto-indexed methods of addressing memory. The memory-increment/decrement instructions and the transfer instructions use the PC-relative or indexed methods of addressing.

The various methods of addressing memory and peripherals are shown below.

Immediate addressing is an addressing format specific to the immediate instruction group.

TYPE OF ADDRESSING	OPERAND FORMATS		
	m	ptr	disp
PC-relative	0	0	-128 to +127
Indexed	0	1,2, or 3	-128 to +127
Immediate	1	0	-128 to +127
Auto-indexed	1	1,2, or 3	-128 to +127

For PC-relative, indexed, and auto-indexed memory-reference instructions, another feature of the addressing architecture is that the contents of the extension register are substituted for the displacement if the instruction displacement equals -128 (-X'80).

NOTE

All arithmetic operations associated with address formation affect only the 12 low-order address bits; no carry is provided to the 4 high-order bits. For systems employing memories of 4K or less, the high-order bits can be ignored as they are set to 0000 following initialization. For systems employing larger memories, the high-order bits must be set to the starting address of the desired 4K block of memory. For example:

0001_2 enables memoory locations 1000_{16} - $1FFF_{16}$ to be addressed.

0010_2 enables memory locations 2000_{16} - $2FFF_{16}$ to be addressed and so forth.

PC-Relative Addressing—A PC-relative address is formed by adding the displacement value specified in the operand field of the instruction to the current contents of the program counter. The displacement is an 8-bit twos-complement number, so the range of the PC-relative addressing format is -128_{10} to $+127_{10}$ locations from the current contents of the program counter.

Immediate Addressing—Immediate addressing uses the value in the second byte of a double-byte instruction as the operand for the operation to be performed (see below).

For example, compare a Load (LD) instruction to a Load Immediate (LDI) instruction. The Load instruction uses the contents of

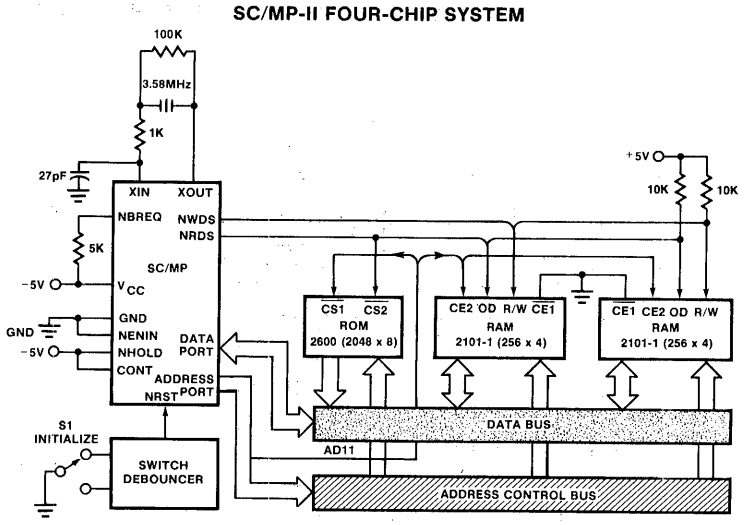
the second byte of the instruction in computing the effective address of the data to be loaded. The Load Immediate instruction uses the contents of the second byte as the data to be loaded.

Indexed Addressing—Indexed addressing enables the programmer to address any location in memory through the use of the pointer register and the displacement. When indexed addressing is specified in an instruction, the contents of the designated pointer register are added to the displacement to form the effective address. The contents of the pointer register are not modified by indexed addressing.

Auto-Indexed Addressing—Auto-indexed addressing provides the same capabilities as indexed addressing along with the ability to increment or decrement the designated pointer register by the value of the displacement. If the displacement is less than zero, the pointer register is decremented by the displacement before the contents of the effective address are fetched or stored. If the displacement is equal to or greater than zero, the pointer register is used as the effective address, and the pointer register is incremented by the displacement after the contents of the effective address are fetched or stored.

SYSTEM IMPLEMENTATION

Figures 11 and through 13 illustrate typical SC/MP system configurations. In Figure 10, SC/MP is shown interconnected to three memory devices to form a stand-alone 4-device system that provides 256 words of read/write memory and 2,048 words for program storage. Figure 12 shows SC/MP interconnected to an external controller for Direct Memory Access (DMA) operation, and Figure 13 illustrates a multiprocessor application using SC/MP's built-in logic to control bus access.



NOTE

Part numbers are shown only for information purposes. Other memory components with suitable characteristics can be used.

Figure 11

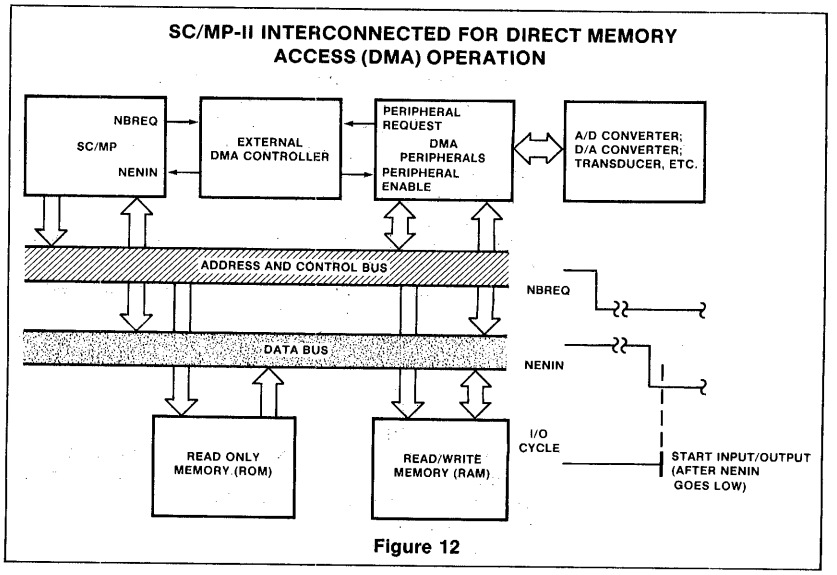


Figure 12

MULTIPROCESSOR SYSTEM USING SC/MP-II BUILT-IN LOGIC FOR BUS CONTROL

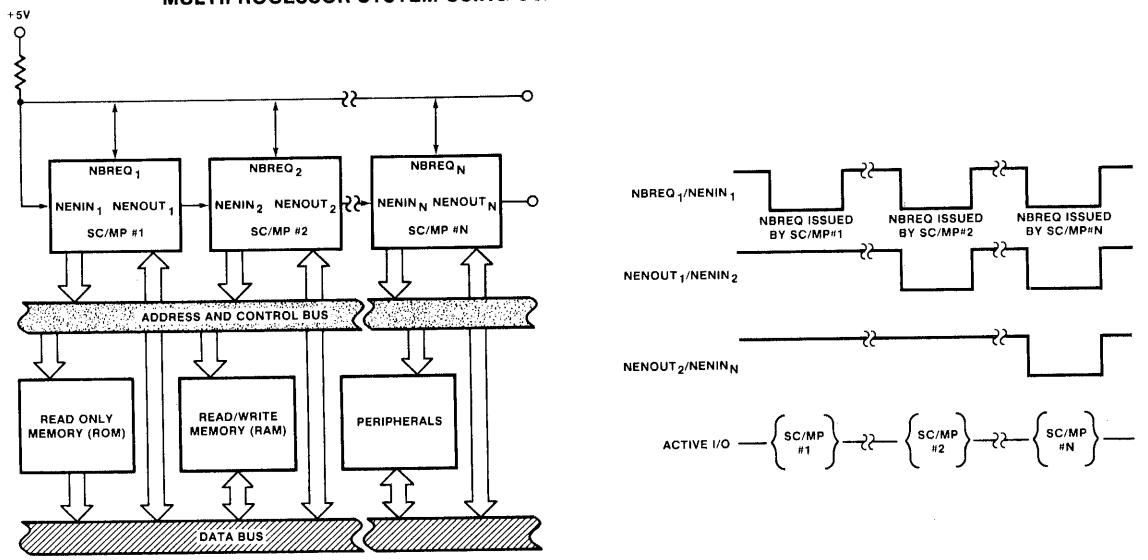


Figure 13

SYMBOL AND NOTATION	MEANING
AC	8-bit Accumulator.
CY/L	Carry/Link Flag in the Status Register.
data	Signed, 8-bit immediate data field.
disp	Displacement; represents an operand in a nonmemory reference instruction or an address modifier field in a memory reference instruction. It is a signed twos-complement number.
EA	Effective Address as specified by the instruction.
E	Extension Register; provides for temporary storage, variable displacements and separate serial input/output port.
i	Unspecified bit of a register.
IE	Interrupt Enable Flag.
m	Mode bit, used in memory reference instructions. Blank parameter sets m = 0, at sets m = 1.
OV	Overflow Flag in the Status Register.
PC	Program Counter (Pointer Register 0); during address formation, PC points to the last byte of the instruction being executed.
ptr	Pointer Register (ptr = 0 through 3). The register specified in byte 1 of the instruction.
$ptr_{n:m}$	Pointer register bits; n:m = 7 through 0 or 15 through 8.
SIN	Serial Input pin.
SOUT	Serial Output pin.
SR	8-bit Status Register.
( )	Means "contents of." For example, (EA) is contents of Effective Address.
[ ]	Means optional field in the assembler instruction format.
~	Ones complement of value to right of ~.
→	Means "replaces."
←	Means "is replaced by."
↔	Means "exchange."
@	When used in the operand field of the instruction, sets the mode bit (m) to 1 for auto-incrementing/auto-decrementing indexing.
10+	Modulo 10 addition.
Λ	AND operation.
V	Inclusive-OR operation.
∀	Exclusive-OR operation.
≥	Greater than or equal to.
=	Equals.
≠	Does not equal.

Table 5 GLOSSARY

MP8080A-I

DESCRIPTION

The MP8080A is an 8-bit microprocessor housed in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, functions as the central processing unit (CPU) in Signetics' 8080 microcomputer family.

The MP8080A has a 16-bit address bus that is capable of addressing up to 65k bytes of memory and up to 256 input and 256 output devices. Data is routed to and from the MP8080A on a separate bidirectional 8-bit bus. This data bus is also Tri-State, making direct memory addressing (DMA) and multiprocessing applications possible. The MP8080A directly provides signals to control the interface to memory and I/O ports. All buses, including control, are TTL compatible.

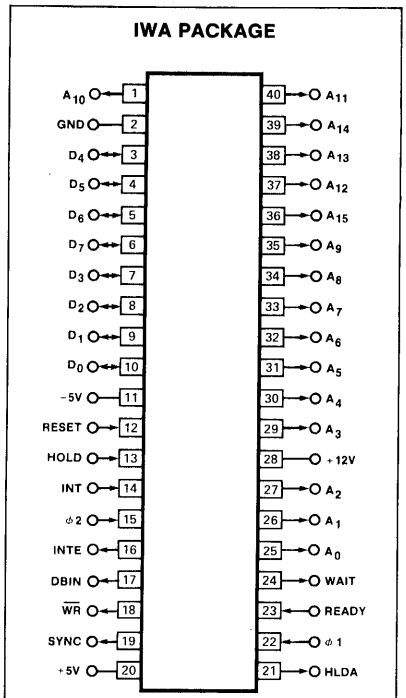
An asynchronous interrupt capability is included in the MP8080A to allow external signals to change the instruction sequence. The interrupting device may vector the program to a particular service routine location (or some other direct function) by specifying an interrupt instruction to be executed.

FEATURES

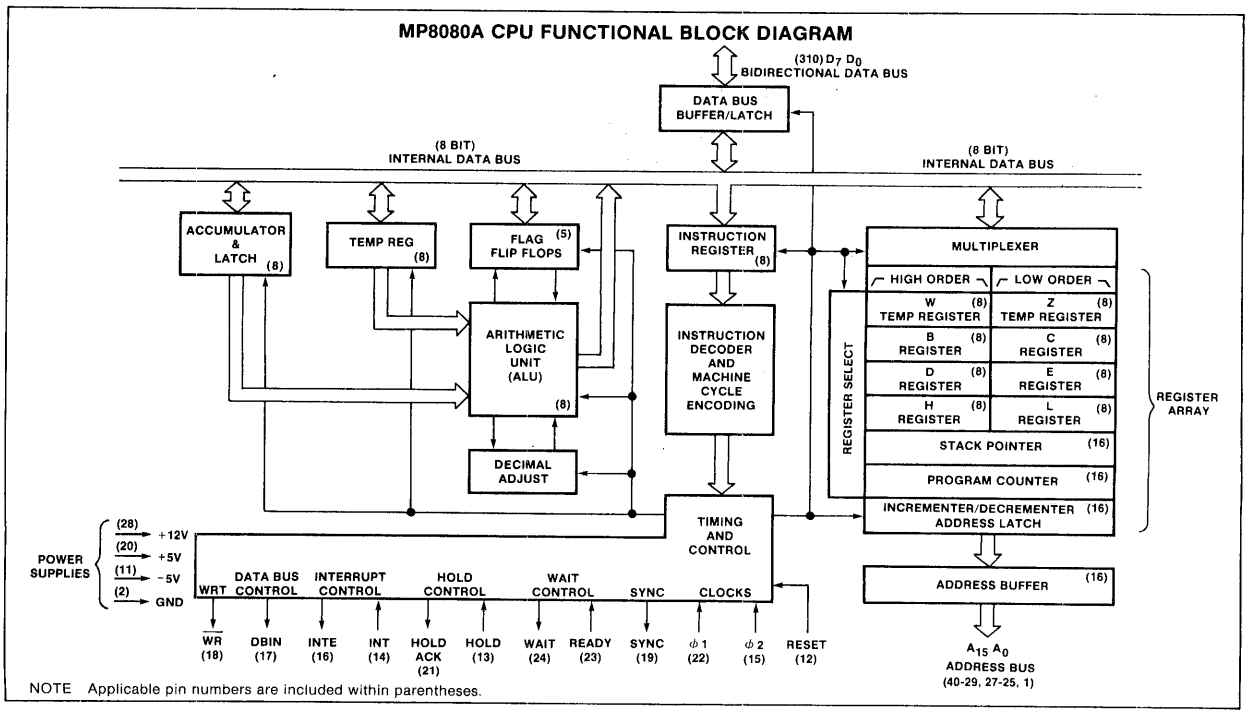
- **2μs instruction cycle**
- **Variable length instructions**
- **General purpose registers—six plus an accumulator**
- **Direct addressing up to 65k bytes**
- **Variable length stack accessed by 16-bit stack pointer**
- **Addresses 256 input and 256 output ports**
- **Provisions for vectored interrupts**
- **Tri-state bus for DMA and multiprocessing capability**
- **Tri-state TTL drive capabilities for address and data buses**
- **Decimal arithmetic capability**
- **Multiple addressing modes**
  - **Direct**
  - **Register**
  - **Register indirect**
  - **Immediate**
- **Direct plug-in replacement for Intel MP8080A**

PIN CONFIGURATION

IWA PACKAGE



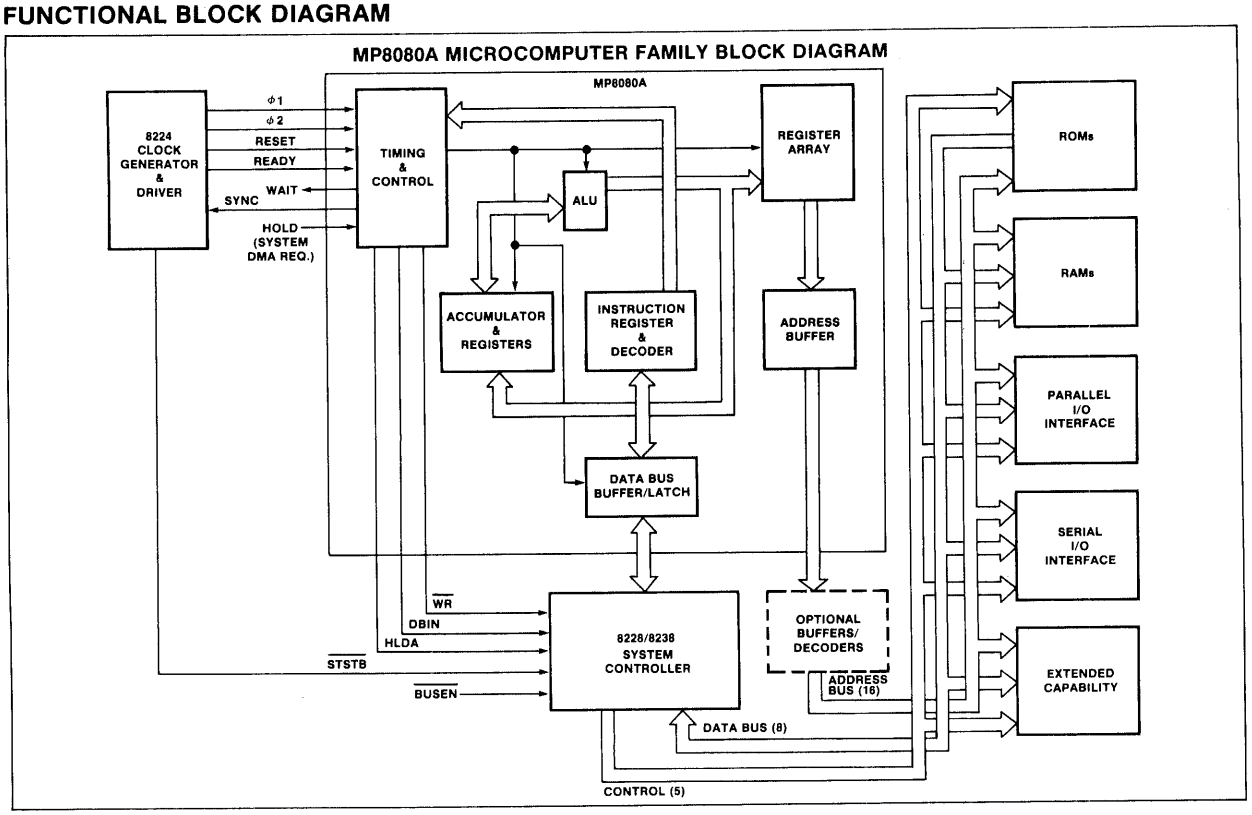
FUNCTIONAL BLOCK DIAGRAM



NOTE Applicable pin numbers are included within parentheses.

2

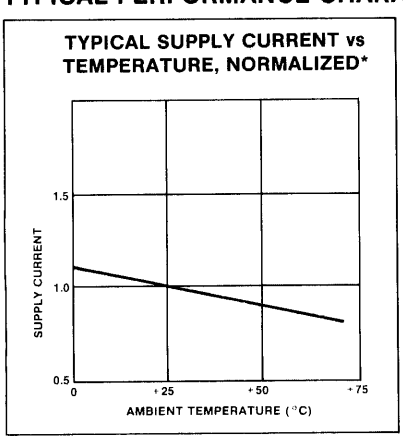
FUNCTIONAL BLOCK DIAGRAM

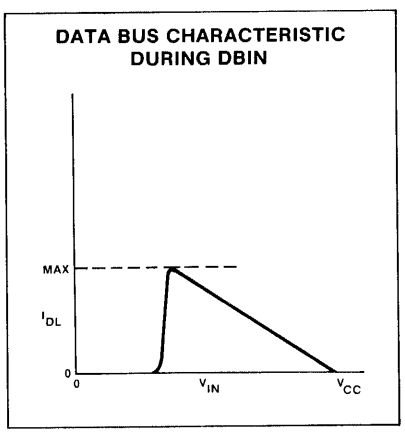


*NOTE

$\Delta 1$ supply/ΔT_A = 0.45%/°C.

TYPICAL PERFORMANCE CHARACTERISTICS





PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
READY	23	I	**Ready:** When high (logic 1), indicates that valid memory or input data are available to the CPU on the MP8080A data bus. The Ready signal is used to synchronize the CPU with slower memory or input/output devices. If the MP8080A does not receive a high Ready input after sending out an address to memory or an input/output device, the MP8080A enters a Wait mode for as long as the Ready input remains low (logic 0). The CPU may also be single stepped by the use of the Ready signal.
HOLD	13	I	**Hold:** When high, requests that the CPU enter the Hold mode. When the CPU is in the Hold mode, the CPU address and the data buses both will be in the high-impedance state. The Hold mode allows an external device to gain control of the MP8080A address and data buses immediately following the completion of the current machine cycle by the CPU. The CPU acknowledges the Hold mode via the HLDA output line. The Hold request is recognized under the following conditions: 1. The CPU is in the Halt mode. 2. The Ready signal is active and the CPU is in the t_2 or t_w state.
INT	14	I	**Interrupt Request:** When high, the CPU recognizes an interrupt request on this line after completing the current instruction or while in the *Halt* mode. An interrupt request is not honored if the CPU is in the Hold mode (HLDA = logic 1) or the INTE Flip-flop is reset (logic 0).
RESET	12	I	**Reset:** When activated (high) for a minimum of three clock periods, the content of the Program Counter is cleared and the Interrupt Enable and HLDA Flip-flops are reset. Following a Reset, program execution starts at memory location 0. It should be noted that the status flags, accumulator, stack pointer, and registers are not cleared during the Reset sequence.
ϕ_1, ϕ_2	22,15	I	**ϕ_1 and ϕ_2 Clocks:** Two non-TTL compatible clock phases which provide nonoverlapping timing references for internal storage elements and logic circuits of the CPU.
SYNC	19	O	**Sychronizing Signal:** When activated (high), the beginning of a new machine cycle is indicated and the status word is outputted on the Data Bus.
A_{15}-A_0	25-27, 29-40	O	**Address Bus:** This bus comprises sixteen tri-state output lines. The bus provides the address to memory (up to 65k bytes) or denotes the input/output device number for up to 256 input and 256 output peripherals.
WAIT	24	O	**Wait:** When high, acknowledges that the CPU is in the Wait mode.
WR	18	O	**Write:** When low, the data on the data bus are stable for Write memory or output operation.
HLDA	21	O	**Hold Acknowledge:** Goes high in response to a logic 1 on the Hold line and indicates that the data and address bus will go to the high-impedance state. The HLDA begins at one of the following times: 1. The t_3 state of the Read memory input operation. 2. The clock period following the t_3 state of a Write memory output operation. In both cases, the HLDA signal starts after the rising edge of the ϕ_1 clock, and high impedance occurs after the rising edge of the ϕ_2 clock.
INTE	16	O	**Interrupt Enable:** Indicates the content of the internal INTE Flip-flop. The Enable and Disable Interrupt (EI and DI) Instructions cause the INTE Flip-flop to be set and reset, respectively. When the Flip-flop is reset (INTE = logic 0), it inhibits interrupts from being accepted by the CPU. In addition, the INTE Flip-flop is automatically reset (thereby disabling further interrupts) at the t_1 state of the instruction fetch cycle, when an interrupt is accepted; it is also reset by the Reset Signal.
D_7-D_0	3-10	I/O	**Data Bus:** This bus comprises eight tri-state input/output lines. The bus provides bidirectional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on the data bus during the first state of each machine cycle (SYNC = logic 1).
+12V	28	I	**+2 Volts:** V_{DD} Supply.
+5V	20	I	**+5 Volts:** V_{CC} Supply.
-5V	11	I	**-5 Volts:** V_{BB} Supply.
GND	2	I	**Ground:** V_{SS} (0 volt) reference.

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All input or output voltages with respect to V_{BB}	-0.3 to +20	V
V_{CC}	V_{DD} and V_{SS} with respect to V_{BB}	-0.3 to 20	V
	Power dissipation	1.5	W

NOTE Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = \pm 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$ $V_{SS} = 0V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IHC}	Clock high		9.0		V_{DD} +1	
V_{ILC}	Clock low		V_{SS} -1		V_{SS} +0.8	
V_{IH}	High		3.3		V_{CC} +1	
V_{IL}	Low		V_{SS} -1		V_{SS} +0.8	
	Output voltage					V
V_{OH}	High	$I_{OH} = 150\mu A$	3.7			
V_{OL}	Low	$I_{OL} = 1.9mA$ on all inputs			0.45	
	Supply current					mA
$I_{DD(AV)}$	Avg. (V_{DD})	Operation $t_{CY} = 0.48\mu s$		40	70	
$I_{CC(AV)}$	Avg. (V_{CC})	Operation $t_{CY} = 0.48\mu s$		60	80	
$I_{BB(AV)}$	Avg. (V_{BB})			0.01	1	
	Leakage current					μA
I_{IL}	Input	$V_{SS} \le V_{IN} \le V_{CC}$			± 10	
I_{CL}	Clock	$V_{SS} \le V_{CLOCK} \le V_{DD}$			± 10	
	Data bus					μA
I_{DL}*	(in input mode)	$V_{SS} \le V_{IN} \le V_{SS} + 0.8V$			-100	
		$V_{SS} \le +0.8V \le V_{IN} \le V_{CC}$			-2.0	
	Address and data bus					μA
I_{FL}	(during hold)	$V_{ADDR/DATA} = V_{CC}$			+10	
		$V_{ADDR/DATA} = V_{SS} + 0.45V$			-100	
	Capacitance	($T_A = 25°C$, $V_{CC} = V_{DD} = V_{SS} = 0V$, $V_{BB} = -5V$)				pF
C_ϕ	Clock	$f_c = 1MHz$		17	25	
C_{IN}	Input	Unmeasured pins		6	10	
C_{OUT}	Output	Returned to V_{SS}		10	20	

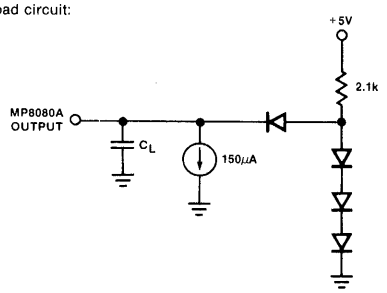
*NOTE
When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.

AC ELECTRICAL CHARACTERISTICS (Cont'd) T_A = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = ±5V ± 5%, V_{BB} = -5V ± 5% V_{SS} = 0V, unless otherwise specified.

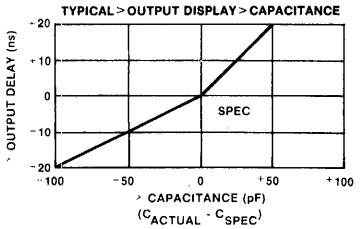
	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{CY}[3]	Clock period		0.48		2.0	μs
$t_{r,tf}$	Clock rise and fall time		0		50	ns
$t_{\phi 1}$	ϕ_1 Pulse width		60			ns
$t_{\phi 2}$	ϕ_2 Pulse width		220			ns
t_{D1}	Delay ϕ_1 to ϕ_2		0			ns
t_{D2}	Delay ϕ_2 to ϕ_1		70			ns
t_{D3}	Delay ϕ_1 to ϕ_2 leading edges		80			ns
t_{DA}[2]	Address output delay from ϕ_2	C_L = 100pF			200	ns
t_{DD}[2]	Data output delay from ϕ_2	C_L = 100pF			220	ns
t_{DC}[2]	Signal output delay from ϕ_1 or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)	C_L = 50pF			120	ns
t_{DF}[2]	DBIN delay from ϕ_2	C_L = 50pF	25		140	ns
t_{DI}[1]	Delay for input bus to enter input mode				t_{DF}	ns
t_{DS1}	Data setup time during ϕ_1 and DBIN		30			ns
t_{DS2}	Data setup time to ϕ_2 during DBIN		150			ns
t_{DH}[1]	Data hold time from ϕ_2 during DBIN		1			ns
t_{IE}[2]	INTE output delay from ϕ_2	C_L = 50pF			200	ns
t_{RS}	Ready setup time during ϕ_2		120			ns
t_{HS}	Hold setup time to ϕ_2		140			ns
t_{IS}	INT setup time during ϕ_2 (during ϕ_1 in halt mode)		120			ns
t_H	Hold time from ϕ_2 (READY, INT, HOLD)		0			ns
t_{FD}	Delay to float during hold (address and data bus)	C_L = 100pF: Address, data			120	ns
t_{AW}[2]	Address stable prior to $\overline{WR}$[5]		(Note 5)		(Note 5)	ns
t_{DW}[2]	Output data stable prior to $\overline{WR}$[6]	C_L = 50pF: $\overline{WR}$, HLDA, DBIN	(Note 6)		(Note 6)	ns
t_{WD}[2]	Output data stable from $\overline{WR}$[7]		(Note 7)		(Note 7)	ns
t_{WA}[2]	Address stable from $\overline{WR}$[7]		(Note 7)		(Note 7)	ns
t_{HF}[2]	HLDA to float delay[8]		(Note 8)		(Note 8)	ns
t_{WF}[2]	$\overline{WR}$ to float delay[9]		(Note 9)		(Note 9)	ns
t_{AH}[2]	Address hold time after DBIN during HLDA		-20			ns

NOTES

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50ns or t_{DF}, whichever is less.
2. Typical load circuit:

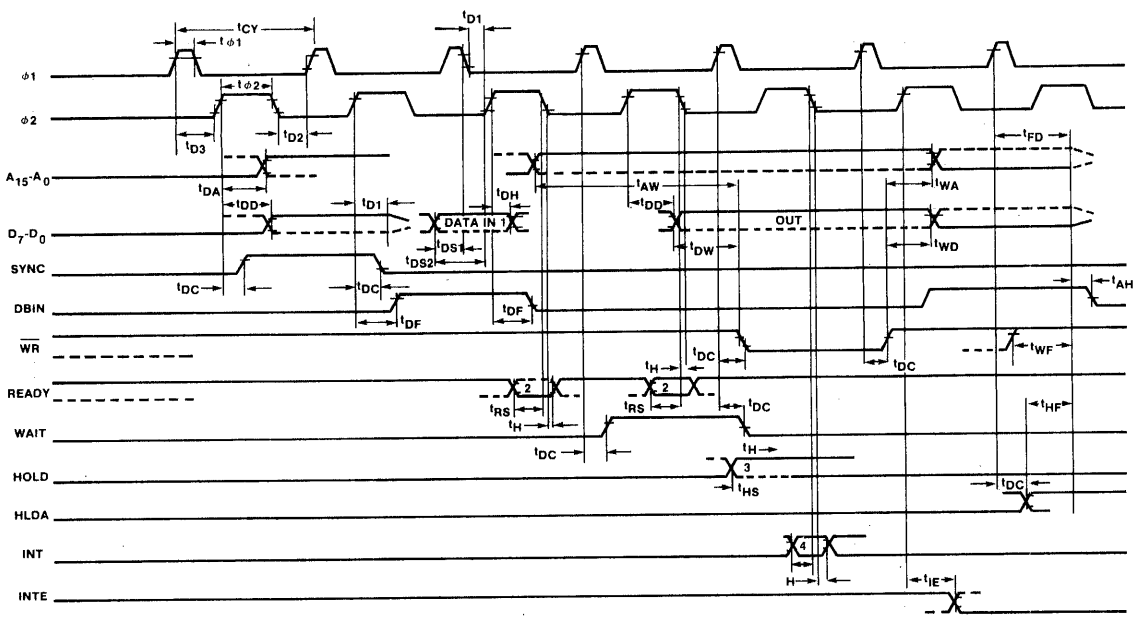


3. $t_{CY} = t_{D3} + t_{r\phi 2} + t_{\phi 2} + t_{D2} + t_{f\phi 2} + t_{r\phi 1} \geq 480ns$.



4. The following are relevant when interfacing the MP8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from 0.8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output Delay when measured to 3.0V = SPEC + 60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add 0.6ns/pF if $C_L > C_{SPEC}$, subtract 0.3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2t_{CY} - t_{D3} - t_{r\phi 2} - 140ns$.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi 2} - 170ns$.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi 2} + 10ns$. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi 2} - 50ns$.
9. $t_{WF} = t_{D3} + t_{r\phi 2} - 10ns$.

VOLTAGE WAVEFORMS



NOTE Timing measurements are made at the following reference voltages: Clock '1' = 8.0V, '0' = 1.0V; Inputs '1' = 3.3V, '0' = 0.8V; Outputs '1' = 2.0V, '0' = 0.8V.

SYMBOLS	DATA BUS BIT	DEFINITION
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when WR is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle of the first byte of an instruction.
INP*	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR*	D_7	Designates that the data bus will be used for memory read data.
INTA*	D_0	Acknowledge signal for Interrupt request. Signal should be used to gate a restart instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a Write memory or Output function (WO = 0). Otherwise, a Read memory or Input operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for Halt Instruction.

Table 1 STATUS INFORMATION DEFINITION

*These three status bits can be used to control the flow of data onto the MP8080A data bus.

NOTES

1. Data in must be stable for this period during DBIN-T_3. Both t_{DS1} and t_{DS2} must be satisfied.
2. Ready signal must be stable for this period during t_2 or T_W. (Must be externally synchronized.)
3. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5, and T_{WH} when in hold mode. (External synchronization is not required.)
4. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)

MACHINE CYCLE	TYPE	DATA BUS BIT							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction fetch	1	1	0	1	0	0	0	1	0
Memory read	2	1	0	0	0	0	0	1	0
Memory write	3	0	0	0	0	0	0	0	0
Stack read	4	1	0	0	0	0	1	1	0
Stack write	5	0	0	0	0	0	1	0	0
Input read	6	0	1	0	0	0	0	1	0
Output write	7	0	0	0	1	0	0	0	0
Interrupt acknowledge	8	0	0	1	0	0	0	1	1
Halt acknowledge	9	1	0	0	0	1	0	1	0
Interrupt acknowledge while halt	10	0	0	1	0	1	0	1	1

Table 2 STATUS WORD CHART

MNEMONIC	DESCRIPTION	OPERATION	OP CODE								No. of Bytes	No. of Machine (M) Cycles	No. of States (T)	CONDITION FLAGS				
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				S	Z	AC	P	CY
DATA TRANSFER GROUP																		
LDA	Load Accumulator Direct	(A) ← ((byte 3) (byte 2))	0	0	1	1	1	0	1	0	3	4	13					
LDAX B	Load Accumulator Indirect	(A) ← ((B) (C))	0	0	0	0	1	0	1	0	1	2	7					
LDAX D	Load Accumulator Indirect	(A)← ((D) (E))	0	0	0	1	1	0	1	0	1	2	7					
LHLD	Load H and L Direct	(L) ← ((byte 3) (byte 2)) (H) ← ((byte 3) (byte 2) + 1)	0	0	1	0	1	0	1	0	3	5	16					
LXI B	Load Immediate, Registers B and C	(B) ← (byte 3) (C) ← (byte 2)	0	0	0	0	0	0	0	1	3	3	10					
LXI D	Load Immediate, Registers D and E	(D) ← (byte 3) (E) ← (byte 2)	0	0	0	1	0	0	0	1	3	3	10					
LXI H	Load Immediate, Registers H and L	(H) ← (byte) (L) ← (byte 2)	0	0	1	0	0	0	0	1	3	3	10					
LXI SP	Load Immediate, Stack Pointer	(SPH) ← (byte 3) (SPL) ← (byte 2)	0	0	1	1	0	0	0	1	3	3	10					
MOV M,r	Move to Memory	((H) (L)) ← (r)	0	1	1	1	0	S	S	S	1	2	7	(Flags Not Affected)				
MOV r,M	Move from Memory	(r) ←((H) (L))	0	1	D	D	D	1	1	0	1	2	7					
MOV r1, r2	Move Registers	(r1) ← (r2)	0	1	D	D	D	S	S	S	1	1	5					
MVI M	Move to Memory Immediate	((H) (L)) ← (byte 2)	0	0	1	1	0	1	1	0	2	3	10					
MVI r	Move Immediate	(r) ← (byte 2)	0	0	D	D	D	1	1	0	2	2	7					
SHLD	Store H and L Direct	((byte 3) (byte 2)) ← (L) ((byte 3) (byte 2) + 1) ← (H)	0	0	1	0	0	0	1	0	3	5	16					
STA	Store Accumulator Direct	((byte 3) (byte 2)) ← (A)	0	0	1	1	0	0	1	0	3	4	13					
STAX B	Store Accumulator Indirect	((B) (C)) ← (A)	0	0	0	0	0	0	1	0	1	2	7					
STAX D	Store Accumulator Indirect	((D) (E)) ← (A)	0	0	0	1	0	0	1	0	1	2	7					
XCHG	Exchange H and L with D and E	(H) ↔ (D) (L) ↔ (E)	1	1	1	0	1	0	1	1	1	1	4					
ARITHMETIC GROUP																		
ACI	Add Immediate with Carry	(A) ← (A) + (byte 2) + (CY)	1	1	0	0	1	1	1	0	2	2	7	↕	↕	↕	↕	↕
ADC M	Add Memory with Carry	(A) ← (A) + ((H) (L))+ (CY)	1	0	0	0	1	1	1	0	1	2	7	↕	↕	↕	↕	↕
ADC r	Add Register with Carry	(A) ← (A) + (r) + (CY)	1	0	0	0	1	S	S	S	1	1	4	↕	↕	↕	↕	↕
ADD M	Add Memory	(A) ← (A) + ((H) (L))	1	0	0	0	0	1	1	0	1	2	7	↕	↕	↕	↕	↕
ADD r	Add Register	(A) ← (A) + (r)	1	0	0	0	0	S	S	S	1	1	4	↕	↕	↕	↕	↕
ADI	Add Immediate	(A) ← (A) + (byte 2)	1	1	0	0	0	1	1	0	1	2	7	↕	↕	↕	↕	↕
DAA	Decimal Adjust Accumulator	8-bit number in Accumulator is converted to two 4-bit BCD digits	0	0	1	0	0	1	1	1	1	1	4	↕	↕	↕	↕	↕
DAD B	Add B and C to H and L	(H) (L) ← (H) (L) + (B) (C)	0	0	0	0	1	0	0	1	1	3	10	·	·	·	·	↕
DAD D	Add D and E to H and L	(H) (L) ← (H) (L) + (D) (E)	0	0	0	1	1	0	0	1	1	3	10	·	·	·	·	↕
DAD H	Add H and L to H and L	(H) (L) ← (H) (L) + (H) (L)	0	0	1	0	1	0	0	1	1	3	10	·	·	·	·	↕
DAD SP	Add Stack Pointer to H and L	(H) (L) ← (H) (L) + (SP)	0	0	1	1	1	0	0	1	1	3	10	·	·	·	·	↕
DCR M	Decrement Memory	((H) (L)) ← ((H) (L)) - 1	0	0	1	1	0	1	0	1	1	3	10	↕	·	↕	↕	·
DCR r	Decrement Register	(r) ← (r) - 1	0	0	D	D	D	1	0	1	1	1	5	↕	·	↕	↕	·
DCX B	Decrement Registers B and C	(B) (C) ← (B) (C) - 1	0	0	0	0	1	0	1	1	1	1	5	·	·	·	·	·
DCX D	Decrement Registers D and E	(D) (E) ← (D) (E) - 1	0	0	0	1	1	0	1	1	1	1	5	·	·	·	·	·
DCX H	Decrement Registers H and L	(H) (L) ← (H) (L) - 1	0	0	1	0	1	0	1	1	1	1	5	·	·	·	·	·
DCX SP	Decrement Stack Power	(SP) ← (SP) - 1	0	0	1	1	1	0	1	1	1	1	5	·	·	·	·	·
INR M	Increment Memory	((H) (L)) ← ((H) (L)) + 1	0	0	1	1	0	1	0	0	1	3	10	↕	↕	↕	↕	·
INR r	Increment Register	(r) ← (r) + 1	0	0	D	D	D	1	0	0	1	1	5	↕	↕	↕	↕	·
INX B	Increment Registers B and C	(B) (C) ← (B) (C) + 1	0	0	0	0	0	0	1	1	1	1	5	·	·	·	·	·
INX D	Increment Registers D and E	(D) (E) ← (D) (E) + 1	0	0	0	1	0	0	1	1	1	1	5	·	·	·	·	·
INX H	Increment Registers H and L	(H) (L) ← (H) (L) + 1	0	0	1	0	0	0	1	1	1	1	5	·	·	·	·	·

Table 3 INSTRUCTION SET

MNEMONIC	DESCRIPTION	OPERATION	OP CODE								No. of Bytes	No. of Machine (M) Cycles	No. of States (T)	CONDITION FLAGS				
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				S	Z	AC	P	CY
ARITHMETIC GROUP (Cont'd)																		
INX SP	Increment Stack Pointer	(SP) ← (SP) + 1	0	0	1	1	0	0	1	1	1	1	5	·	·	·	·	·
SBB M	Subtract Memory with Borrow	(A) ← (A) - ((H) (L)) - (CY)	1	0	0	1	1	1	1	0	1	2	7	↕	↕	↕	↕	↕
SBB r	Subtract Register with Borrow	(A) ← (A) - (r) - (CY)	1	0	0	1	1	S	S	S	1	1	4	↕	↕	↕	↕	↕
SBI	Subtract Immediate with Borrow	(A) ← (A) - (byte 2) - (CY)	1	1	0	1	1	1	1	0	2	2	7	↕	↕	↕	↕	↕
SUB M	Subtract Memory	(A) ← (A) - ((H) (L))	1	0	0	1	0	1	1	0	1	2	7	↕	↕	↕	↕	↕
SUB r	Subtract Register	(A) ← (A) - (r)	1	0	0	1	0	S	S	S	1	1	4	↕	↕	↕	↕	↕
SUI	Subtract Immediate	(A) ← (A) - (byte 2)	1	1	0	1	0	1	1	0	2	2	7	↕	↕	↕	↕	↕
LOGICAL GROUP																		
ANA M	AND Memory	(A) ← (A) ((H) (L))	1	0	1	0	0	1	1	0	1	2	7	↕	↕	↕d	↕	0
ANA r	AND Register	(A) ← (A) (r)	1	0	1	0	0	S	S	S	1	1	4	↕	↕	↕d	↕	0
ANI	AND Immediate	(A) ← (A) (byte 2)	1	1	1	0	0	1	1	0	2	2	7	↕	↕	↕d	↕	0
CMA	Complement Accumulator	(A) ← $(\overline{A})$	0	0	1	0	1	1	1	1	1	1	4	·	·	·	·	·
CMC	Complement Carry	(CY) ← $(\overline{CY})$	0	0	1	1	1	1	1	1	1	1	4	·	·	·	·	↕
CMP M	Compare Memory	(A)—((H) (L))	1	0	1	1	1	1	1	0	1	2	7	↕	↕a	↕	↕	↕a
CMP r	Compare Register	(A)—(r)	1	0	1	1	1	S	S	S	1	1	4	↕	↕b	↕	↕	↕b
CPI	Compare Immediate	(A)—(byte 2)	1	1	1	1	1	1	1	0	2	2	7	↕	↕c	↕	↕	↕c
ORA M	OR Memory	(A) ← (A) V ((H) (L))	1	0	1	1	0	1	1	0	1	2	7	↕	↕	0	↕	0
ORA r	OR Register	(A) ← (A) V (r)	1	0	1	1	0	S	S	S	1	1	4	↕	↕	0	↕	0
ORI	OR Immediate	(A) ← (A) V (byte 2)	1	1	1	1	0	1	1	0	2	2	7	↕	↕	0	↕	0
RAL	Rotate Left through Carry	$(A_{n+1}) \leftarrow (A_n)$; (CY) ← (A_7) (A_0) ← (CY)	0	0	0	1	0	1	1	1	1	1	4	·	·	·	·	↕
RAR	Rotate Right through Carry	$(A_n) \leftarrow (A_{n+1})$; (CY) ← (A_0) (A_7) ← (CY)	0	0	0	1	1	1	1	1	1	1	4	·	·	·	·	↕
RLC	Rotate Left	$(A_{n+1}) \leftarrow (A_n)$; $(A_0) \leftarrow (A_7)$ (CY) ← (A_7)	0	0	0	0	0	1	1	1	1	1	4	·	·	·	·	↕
RRC	Rotate Right	$(A_n) \leftarrow (A_{n-1})$; $(A_7) \leftarrow (A_0)$ (CY) ← (A_0)	0	0	0	0	1	1	1	1	1	1	4	·	·	·	·	↕
STC	Set Carry	(CY) ← 1	0	0	1	1	0	1	1	1	1	1	4	·	·	·	·	1
XRA M	Exclusive OR Memory	(A) ← (A) ∀ ((H) (L))	1	0	1	0	1	1	1	0	1	2	7	↕	↕	0		0
XRA r	Exclusive OR Register	(A) ← (A) ∀ (r)	1	0	1	0	1	S	S	S	1	1	4	↕	↕	0		0
XRI	Exclusive OR Immediate	(A) ← (A) ∀ (byte 2)	1	1	1	0	1	1	1	0	2	2	7	↕	↕	0		0
BRANCH GROUP																		
CALL	Call Unconditional	((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3) (byte 2)	1	1	0	0	1	1	0	1	3	5	17	(Flags Not Affected)				
CC	Call on Carry	If CY = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3) (byte 2)	1	1	0	1	1	1	0	0	3	3/5	11/17					
CM	Call on Minus	If S = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3) (byte 2)	1	1	1	1	1	1	0	0	3	3/5	11/17					
CNC	Call on No Carry	If CY = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) -2 (PC) ← (byte 3) (byte 2)	1	1	0	1	0	1	0	0	3	3/5	11/17					
CNZ	Call on Not Zero	If Z = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3) (byte 2)	1	1	0	0	0	1	0	0	3	3/5	11/17					
CP	Call on Positive	If S = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3) (byte 2)	1	1	1	1	0	1	0	0	3	3/5	11/17					
CPE	Call on Parity Even	If P = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3) (byte 2)	1	1	1	0	1	1	0	0	3	3/5	11/17					
CPO	Call on Parity Odd	If P = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3) (byte 2)	1	1	1	0	0	1	0	0	3	3/5	11/17					

Table 3 INSTRUCTION SET (Cont'd)

MNEMONIC	DESCRIPTION	OPERATION	OP CODE								No. of Bytes	No. of Machine (M) Cycles	No. of States (T)	CONDITION FLAGS				
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				S	Z	AC	P	CY
BRANCH GROUP (Cont'd)																		
CZ	Call on Zero	If Z = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3) (byte 2)	1	1	0	0	1	1	0	0	3	3/5	11/17					
JC	Jump on Carry	If CY = 1, (PC) ← (byte 3) (byte 2)	1	1	0	1	1	0	1	0	3	3	10					
JM	Jump on Minus	If S = 1, (PC) ← (byte 3) (byte 2)	1	1	1	1	1	0	1	0	3	3	10					
JMP	Jump Unconditional	(PC) ← (byte 3) (byte 2)	1	1	0	0	0	0	1	1	3	3	10					
JNC	Jump on No Carry	If CY = 0, (PC) ← (byte 3) (byte 2)	1	1	0	1	0	0	1	0	3	3	10					
JNZ	Jump on Lot Zero	If Z = 0, (PC) ← (byte 3) (byte 2)	1	1	0	0	0	0	1	0	3	3	10					
JP	Jump on Positive	If S = 0, (PC) ← (byte 3) (byte 2)	1	1	1	1	0	0	1	0	3	3	10					
JPE	Jump on Parity Even	If P = 1, (PC) ← (byte 3) (byte 2)	1	1	1	0	1	0	1	0	3	3	10					
JPO	Jump on Parity Odd	If P = 0, (PC) ← (byte 3) (byte 2)	1	1	1	0	0	0	1	0	3	3	10					
JZ	Jump on Zero	If Z = 1, (PC) ← (byte 3) (byte 2)	1	1	0	0	1	0	1	0	3	3	10					
PCHL	H and L to Program Counter	(PCH) ← (H) (PCL) ← (L)	1	1	1	0	1	0	0	1	1	1	5					
RC	Return on Carry	If CY = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	1	0	0	0	1	1/3	5/11	(Flags Not Affected)				
RET	Return	(PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2;	1	1	0	0	1	0	0	1	1	3	10					
RM	Return on Minus	If S = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	1	0	0	0	1	1/3	5/11					
RNC	Return on No Carry	If CY = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	0	0	0	0	1	1/3	5/11					
RNZ	Return on Not Zero	If Z = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	0	0	0	0	1	1/3	5/11					
RP	Return on Positive	If S = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	0	0	0	0	1	1/3	5/11					
RPE	Return on Parity Even	If P = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	1	0	0	0	1	1/3	5/11					
RPO	Return on Parity Odd	If P = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	0	0	0	0	1	1/3	5/11					
RST	Restart	((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← 8* (NNN)	1	1	N	N	N	1	1	1	1	3	11					
RZ	Return on Zero	If Z = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	1	0	0	0	1	1/3	5/11					

Table 3 INSTRUCTION SET (Cont'd)

MNEMONIC	DESCRIPTION	OPERATION	OP CODE								No. of Bytes	No. of Machine (M) Cycles	No. of States (T)	CONDITION FLAGS				
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				S	Z	AC	P	CY
STACK, I/O, AND MACHINE CONTROL GROUP																		
DI	Disable Interrupts	The Interrupt system is disabled following the execution of the DI instruction.	1	1	1	1	0	0	1	1	1	1	4	·	·	·	·	·
EI	Enable Interrupts	The interrupt system is enabled following the execution of next instruction.	1	1	1	1	1	0	1	1	1	1	4	·	·	·	·	·
HLT	Halt	Processor is stopped; registers and flags are unaffected.	0	1	1	1	0	1	1	0	1	1	7	·	·	·	·	·
IN	Input	(A) ← (data).	1	1	0	1	1	0	1	1	2	3	10	·	·	·	·	·
NOP	No operation	No operation is performed; registers and flags are unaffected.	0	0	0	0	0	0	0	0	1	1	4	·	·	·	·	·
OUT	Output	(data) ← (A)	1	1	0	1	0	0	1	1	2	3	10	·	·	·	·	·
POP B	Pop Registers B and C off Stack	(C) ← ((SP)) (B) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	0	0	0	1	1	3	10	·	·	·	·	·
POP D	Pop Registers D and E off Stack	(E) ← ((SP)) (D) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	0	0	0	1	1	3	10	·	·	·	·	·
POP H	Pop Registers H and L off Stack	(L) ← ((SP)) (H) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	0	0	0	1	1	3	10	·	·	·	·	·
POP PSW	Pop Accumulator and Flags off Stack	(CY) ← $((SP))_0$ (P) ← $((SP))_2$ (AC) ← $((SP))_4$ (Z) ← $((SP))_6$ (S) ← $((SP))_7$ (A) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	0	0	0	1	1	3	10	↕	↕	↕	↕	↕
PUSH B	Push Registers B and C on Stack	((SP) - 1) ← (B) ((SP) - 2) ← (C) (SP) ← (SP) - 2	1	1	0	0	0	1	0	1	1	3	11	·	·	·	·	·
PUSH D	Push Registers D and E on Stack	((SP) - 1) ← (D) ((SP) - 2) ← (E) (SP) ← (SP) - 2	1	1	0	1	0	1	0	1	1	3	11	·	·	·	·	·
PUSH H	Push Registers H and L on Stack	((SP) - 1) ← (H) ((SP) - 2) ← (L) (SP) ← (SP) - 2	1	1	1	0	0	1	0	1	1	3	11	·	·	·	·	·
PUSH PSW	Push Accumulator and Flags on Stack	((SP) - 1) ← (A) $((SP) - 2)_0$ ← (CY) $((SP) - 2)_1$ ←1 $((SP) - 2)_2$ ← (P) $((SP) - 2)_3$ ← 0 $((SP) - 2)_4$ ← (AC) $((SP) - 2)_5$ ← 0 $((SP) - 2)_6$ ← (Z) $((SP) - 2)_7$ ← (S) (SP) ← (SP) - 2	1	1	1	1	0	1	0	1	1	3	11	·	·	·	·	·
SPHL	Move H and L to Stack Pointer	(SP) ← (H) (L)	1	1	1	1	1	0	0	1	1	1	5	·	·	·	·	·
XTHL	Exchange Top of Stack with H and L	(L) ↔ ((SP)) (H) ↔ ((SP) + 1)	1	1	1	0	0	0	1	1	1	5	18	·	·	·	·	·

NOTES

a. Z = 1 if (A) = (H) (L);
CY = 1 if (A) < (H) (L)
b. Z = 1 if (A) = (r);
CY = 1 if (A) < (r)
c. Z = 1 if (A) = (byte 2);
CY = 1 if (A) < (byte 2)
d. As if an arithmetic operation were performed.

Table 3 INSTRUCTION SET (Cont'd)

CONDITION FLAGS AND STANDARD RULES

There are five condition flags associated with the execution of instructions on the MP8080A. They are Zero, Sign, Parity, Carry, and Auxiliary Carry, and each flag is represented by a 1-bit register in the CPU. A flag is "set" by forcing the bit to 1, "reset" by forcing the bit to 0. The bit positions of the flags are indicated in the PUSH and POP PSW instructions.

Unless indicated otherwise, when an instruction affects a flag, it affects it in the following manner:

ZERO (Z) — If the result of an instruction has the value 0, this flag is set; otherwise, it is reset.

SIGN (S) — If the most significant bit of the result of the operation has the value 1, this flag is set; otherwise, it is reset.

PARITY (P) — If the modulo 2 sum of the bits of the result of the operation is 0 (that is, if the result has even parity), this flag is set; otherwise, it is reset (that is, if the result has odd parity).

CARRY (CY) — If the instruction resulted in a carry (from addition) or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set; otherwise, it is reset.

AUXILIARY CARRY (AC) — If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise, it is reset. This flag is affected by single-precision additions, subtractions, increments, decrements, comparisons, and logical operations; however, AC is used principally with additions and increments preceding a DAA (Decimal Adjust Accumulator) Instruction.

SYMBOLS AND ABBREVIATIONS

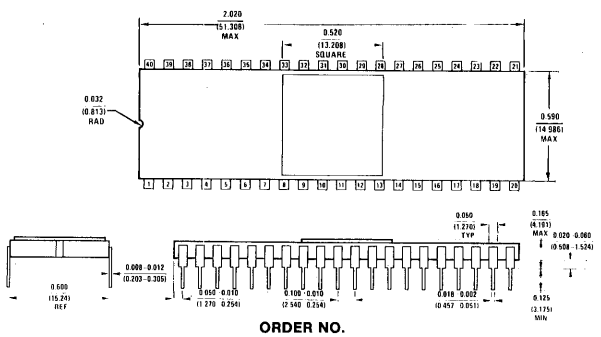
The following symbols and abbreviations are used in the subsequent description of the MP8080A instructions:

Symbols	Meaning
A	Register A (Accumulator)
B	Register B
C	Register C
D	Register D
H	Register H
L	Register L
DDD, SSS	The bit pattern designating one of the registers A, B, C, D, E, H, L (DDD = destination, SSS = source):
	DDD or SSS — Register Name: 111 A; 000 B; 001 C; 010 D; 011 E; 100 H; 101 L
byte 2	The second byte of the instruction
byte 3	The third byte of the instruction
port	8-bit address of an I/O device
r,r1,r2	One of the registers A, B, C, D, E, H, L

Symbols	Meaning
PC	16-bit program counter register (PCH and PCL are used to refer to the high-order and low-order 8 bits respectively.)
SP	16-bit stack pointer register (SPH and SPL are used to refer to the high-order and low-order 8 bits respectively.)
( )	The contents of the memory location or registers enclosed in the parentheses
←	"Is replaced by"
∧	Logical AND
∀	Exclusive-OR
∨	Inclusive-OR
+	Addition
-	Twos complement subtraction
*	Multiplication
↔	"Exchange"
—	The ones complement (for example, $(\overline{A})$)
n	The restart number 0 through 7
NNN	The binary representation 000 through 111 for restart number 0 through 7 resepctively
•	"Not affected"
0	"Reset"
1	"Set"
X	Unknown
↕	Flags affected according to Standard Rules, except as noted.

PHYSICAL DIMENSIONS

40-LEAD CERAMIC DUAL-IN-LINE PACKAGE (I)



ORDER NO.
MP8080A

DESCRIPTION

The Signetics 2651 PCI is a universal synchronous/asychronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Signetics 2650 microprocessor and may be used in a polled or interrupt driven system environment. The 2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- **Synchronous operation**
  - **5 to 8-bit characters**
  - **Single or double SYN operation**
  - **Internal character synchronization**
  - **Transparent or non-transparent mode**
  - **Automatic SYN or DLE-SYN insertion**
  - **SYN or DLE stripping**
  - **Odd, even, or no parity**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 0.8M baud (1X clock)**
- **Asynchronous operation**
  - **5 to 8-bit characters**
  - **1, 1 1/2 or 2 stop bits**
  - **Odd, even, or no parity**
  - **Parity, overrun and framing error detection**
  - **Line break detection and generation**
  - **False start bit detection**
  - **Automatic serial echo mode**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 0.8M baud (1X clock)**
    - **dc to 50k baud (16X clock)**
    - **dc to 12.5k baud (64X clock)**

OTHER FEATURES

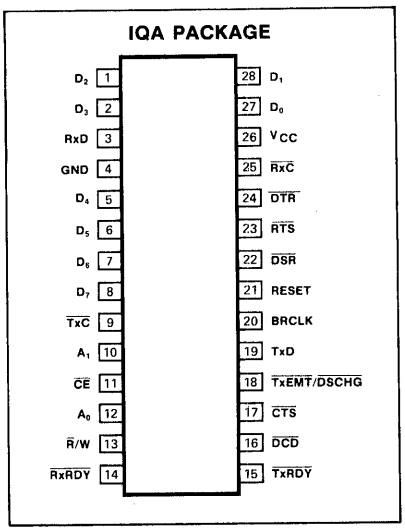
- **Internal or external baud rate clock**
- **16 internal rates-50 to 19,200 baud**
- **Double buffered transmitter and receiver**
- **Full or half duplex operation**
- **Fully compatible with 2650 CPU**
- **TTL compatible inputs and outputs**
- **Single 5V power supply**
- **No system clock required**
- **28-pin dual in-line package**

APPLICATIONS

- **Intelligent terminals**
- **Network processors**
- **Front end processors**
- **Remote data concentrators**
- **Computer to computer links**
- **Serial peripherals**

PIN CONFIGURATION

IQA PACKAGE



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
27,28,1,2, 5-8	D_0-D_7	8-bit data bus	I/O
21	RESET	Reset	I
12,10	A_0-A_1	Internal register select lines	I
13	$\overline{R}/W$	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT/DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +6.0	V

PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design and process changes and improvements.

BAUD RATE	THEORETICAL FREQUENCY 16X CLOCK	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
50	0.8 KHz	0.8 KHz	--	6336
75	1.2	1.2	--	4224
110	1.76	1.76	--	2880
134.5	2.152	2.1523	0.016	2355
150	2.4	2.4	--	2112
300	4.8	4.8	--	1056
600	9.6	9.6	--	528
1200	19.2	19.2	--	264
1800	28.8	28.8	--	176
2000	32.0	32.081	0.253	158
2400	38.4	38.4	--	132
3600	57.6	57.6	--	88
4800	76.8	76.8	--	66
7200	115.2	115.2	--	44
9600	153.6	153.6	--	33
19200	307.2	316.8	3.125	16

NOTE

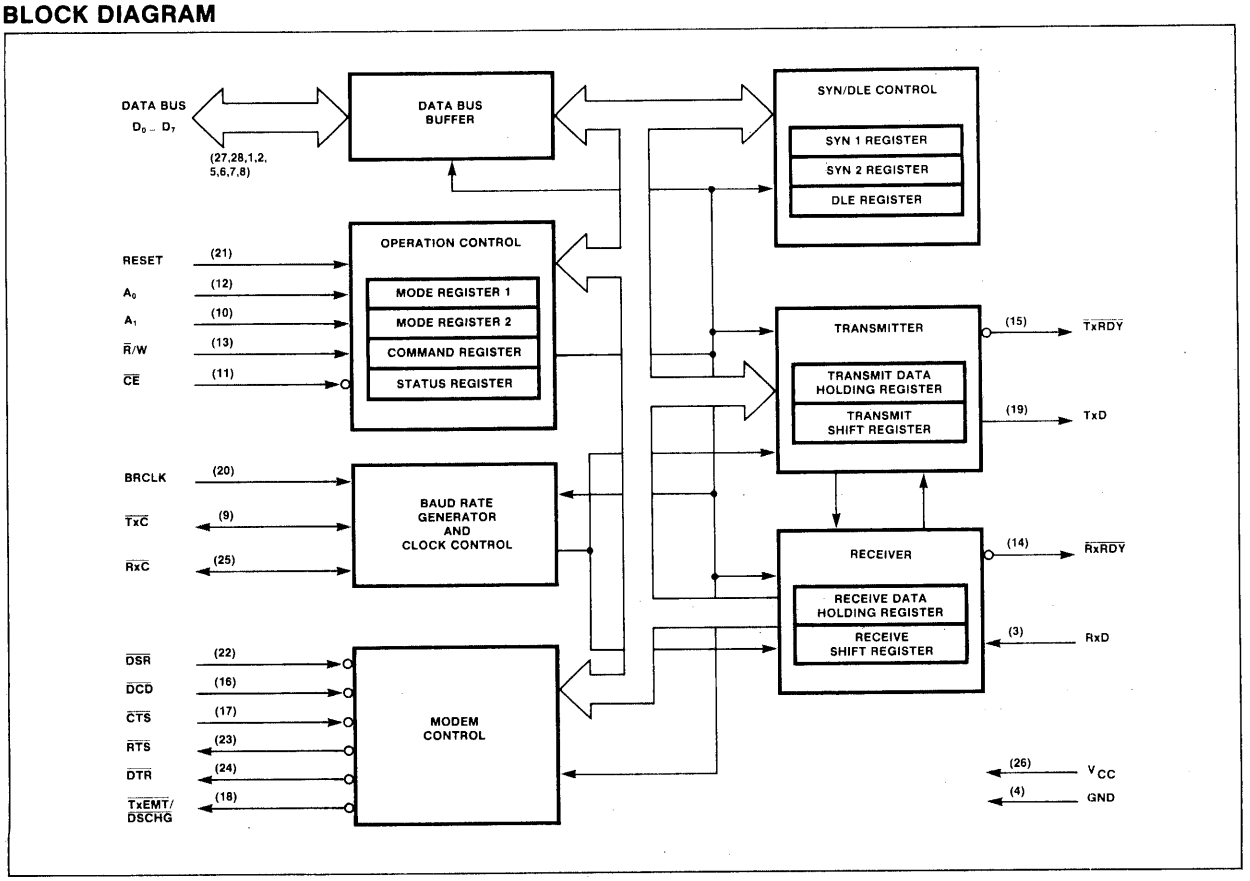
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X.

Table 1 BAUD RATE GENERATOR CHARACTERISTICS
Crystal Frequency = 5.0688MHz

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
V_{CC}	26	I	+5V supply input
GND	4	I	Ground
RESET	21	I	A high on this input performs a master reset on the 2651. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A_1-A_0	10,12	I	Address lines used to select internal PCI registers.
$\overline{R}/W$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command. When low, indicates that control and data lines to the PCI are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the tri-state condition.
D_7-D_0	8,7,6,5, 2,1,28,27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of Status Register bit SR0. When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of Status Register bit SR1. When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT/DSCHG}$	18	O	This output is the complement of Status Register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

Table 2 CPU-RELATED SIGNALS

BLOCK DIAGRAM



BLOCK DIAGRAM

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains Mode Registers 1 and 2, the Command Register, and the Status Register. Details of register addressing and protocol are presented in the PCI Programming section of this data sheet.

Timing

The PCI contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. See Table 1.

Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The Transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

INTERFACE SIGNALS

The PCI interface signals can be grouped into two types: the CPU-related signals (shown in Table 2), which interface the 2651 to the microprocessor system, and the device-related signals (shown in Table 3), which are used to interface to the communications device or system.

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
BRCLK	20	I	5.0688MHz clock input to the internal baud rate generator. Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by Mode Register 1. Data is sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1X the programmed baud rate.
$\overline{TxC}$	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by Mode Register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin becomes an output at 1X the programmed baud rate.
RxD	3	I	Serial data input to the receiver. "Mark" is high, "Space" is low.
TxD	19	O	Serial data output from the transmitter. "Mark" is high, "Space" is low. Held in Mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for Data Set Ready or Ring Indicator condition. Its complement appears as Status Register bit SR7. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{DCD}$	16	I	Data Carrier Detect input. Must be low in order for the receiver to operate. Its complement appears as Status Register bit SR6. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{CTS}$	17	I	Clear to Send input. Must be low in order for the transmitter to operate.
$\overline{DTR}$	24	O	General purpose output which is the complement of Command Register bit CR1. Normally used to indicate Data Terminal Ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of Command Register bit CR5. Normally used to indicate Request to Send.

Table 3 DEVICE-RELATED SIGNALS

OPERATION

The functional operation of the 2651 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the PCI Programming section of this data sheet.

After programming, the PCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The 2651 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and the stop bit(s) have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are set if required. If a break condition is detected (RxD is low for the entire character as well as the stop bit (s)), only one character consisting of all zeros (with the FE status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

When the PCI is initialized into the synchronous mode, the receiver first enters the hunt mode. In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the PCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been achieved, the PCI continues to assemble characters and transfer them to the Holding Register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

Transmitter

The PCI is conditioned to transmit data when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The 2651 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the Transmit Data Holding Register, these conditions are negated. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDI conditions are then asserted

again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the stop bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the 2651 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the PCI unless the CPU fails to send a new character to the PCI by the time the transmitter has completed sending the previous character. Since synchronous communications does not allow gaps between characters, the PCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the command mode. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character.

PCI PROGRAMMING

Prior to initiating data communications, the 2651 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The PCI can be reconfigured at any time during program execution. However, the receiver and transmitter should be disabled if the change has an effect on the reception or transmission of a character. A flowchart of the initialization process appears in Figure 1.

The internal registers of the PCI are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in Table 4.

2651 INITIALIZATION FLOW CHART

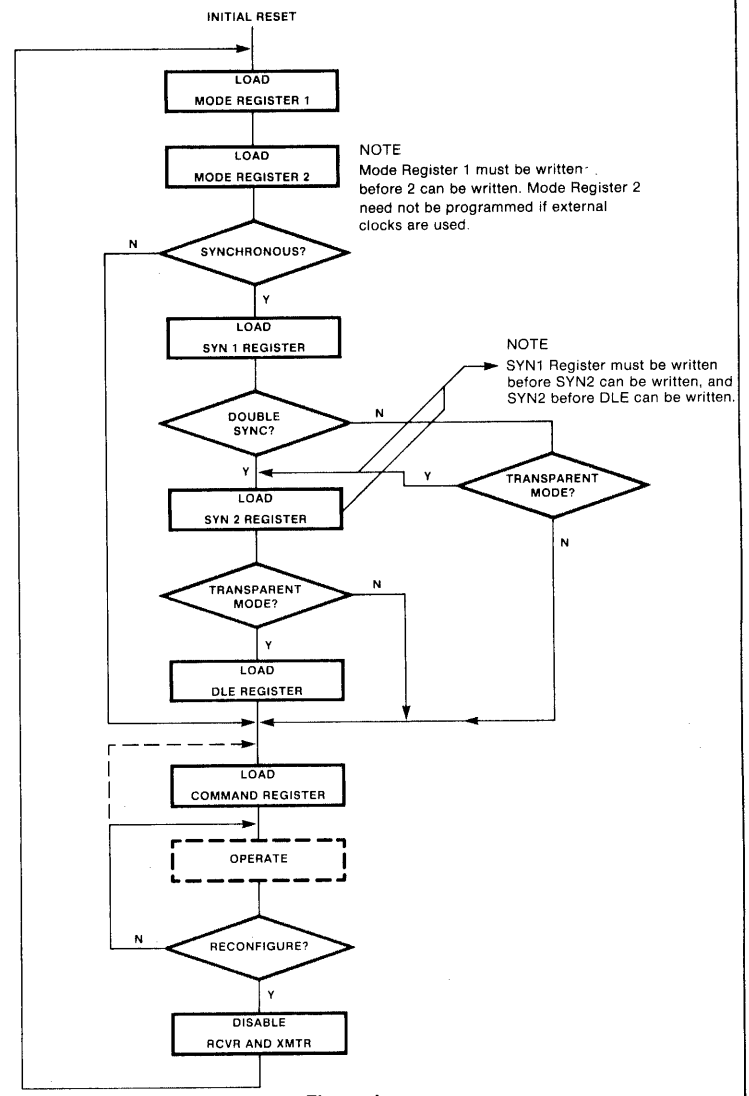


Figure 1

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	FUNCTION
1	X	X	X	Tri-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1/2
0	1	0	1	Write mode registers 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE
See AC Characteristics section for timing requirements.

Table 4 2651 REGISTER ADDRESSING

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions $A_1 = 0$, $A_0 = 1$, and $\overline{R}/W = 1$. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The 2651 register formats are summarized in Tables 5, 6, 7 and 8. Mode Registers 1 and 2 define the general operational characteristics of the PCI, while the Command Register controls the operation within this basic frame-work. The PCI indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asychronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 1X baud rate is programmed, 1.5 stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1-SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill, but the normal synchronization sequence is used.

Mode Register 2 (MR2)

Table 6 illustrates Mode Register 2. MR23, MR22, MR21, and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable. When driven by a 5.0688 MHz input at the BRCLK input (pin 20), the BRG output has zero error except at 134.5, 2000, and 19,200 baud, which have errors of +0.016%, +0.235%, and +3.125% respectively.

MR25 and MR24 select either the BRG or the external inputs $\overline{TxC}$ and $\overline{RxC}$ as the clock source for the transmitter and receiver, respectively. If the BRG clock is selected, the baud rate factor in asynchronous mode is 16X regardless of the factor selected by MR11 and MR10. In addition, the corresponding clock pin provides an output at 1X the baud rate.

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
ASYNCH: STOP BIT LENGTH 00 = INVALID 01 = 1 STOP BIT 10 = 1 1/2 STOP BITS 11 = 2 STOP BITS		0 = ODD 1 = EVEN	0 = DISABLED 1 = ENABLED	00 = 5 BITS 01 = 6 BITS 10 = 7 BITS 11 = 8 BITS		00 = SYNCHRONOUS 1X RATE 01 = ASYNCHRONOUS 1X RATE 10 = ASYNCHRONOUS 16X RATE 11 = ASYNCHRONOUS 64X RATE	
SYNCH: NUMBER OF SYN CHAR 0 = DOUBLE SYN 1 = SINGLE SYN	SYNCH: TRANSPARENCY CONTROL 0 = NORMAL 1 = TRANSPARENT						

NOTE
Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected.

Table 5 MODE REGISTER 1 (MR1)

MR27	MR26	MR25	MR24	MR23	MR22	MR21	MR20
		Transmitter Clock	Receiver Clock	Baud Rate Selection			
NOT USED		0 = EXTERNAL 1 = INTERNAL	0 = EXTERNAL 1 = INTERNAL	0000 = 50 BAUD 0001 = 75 0010 = 110 0011 = 134.5 0100 = 150 0101 = 300 0110 = 600 0111 = 1200		1000 = 1800 BAUD 1001 = 2000 1010 = 2400 1011 = 3600 1100 = 4800 1101 = 7200 1110 = 9600 1111 = 19,200	

Table 6 MODE REGISTER 2 (MR2)

Command Register (CR)

Table 7 illustrates Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected.

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs is the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for a least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. CR3 should be reset in response to the next TxRDY.

Setting CR4 causes the error flags in the Status Register (SR3, SR4, and SR5) to be cleared. This bit resets automatically.

The PCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6 = 01 places the PCI in the Automatic Echo mode. Clocked, regenerated received data is automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. $\overline{TxRDY}$ output = 1.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6 = 01 places the PCI in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16 = 10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR. However, only the first SYN1 of an SYN1-SYN1 pair is stripped.
3. In transparent mode (MR16 =1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. Receive clock = transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the PCI.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6 = 11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. No data is sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the Status Register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the CPU and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the CPU. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{TxRDY}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error		Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = NORMAL OPERATION 01 = ASYNCH: AUTOMATIC ECHO MODE SYNCH: SYN AND/OR DLE STRIPPING MODE 10 = LOCAL LOOP BACK 11 = REMOTE LOOP BACK		0 = FORCE $\overline{RTS}$ OUTPUT HIGH 1 = FORCE $\overline{RTS}$ OUTPUT LOW	0 = NORMAL 1 = RESET ERROR FLAG IN STATUS REG (FE, OE, PE/DLE DETECT)	**ASYNCH: FORCE BREAK** 0 = NORMAL 1 = FORCE BREAK **SYNCH: SEND DLE** 0 = NORMAL 1 = SEND DLE	0 = DISABLE 1 = ENABLE	0 = FORCE $\overline{DTR}$ OUTPUT HIGH 1 = FORCE $\overline{DTR}$ OUTPUT LOW	0 = DISABLE 1 = ENABLE

Table 7 COMMAND REGISTER (CR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrrun**	**PE/DLE Detect**	**TxEMT/DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ INPUT IS HIGH 1 = $\overline{DSR}$ INPUT IS LOW	0 = $\overline{DCD}$ INPUT IS HIGH 1 = $\overline{DCD}$ INPUT IS LOW	**ASYNCH:** 0 = NORMAL 1 = FRAMING ERROR **SYNCH:** 0 = NORMAL 1 = SYN CHAR DETECTED	0 = NORMAL 1 = OVERRUN ERROR	**ASYNCH:** 0 = NORMAL 1 = PARITY ERROR **SYNCH:** 0 = NORMAL 1 = PARITY ERROR OR DLE CHAR RECEIVED	0 = NORMAL 1 = CHANGE IN $\overline{DSR}$ OR $\overline{DCD}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	0 = RECEIVE HOLDING REG EMPTY 1 = RECEIVE HOLDING REG HAS DATA	0 = TRANSMIT HOLDING REG BUSY 1 = TRANSMIT HOLDING REG EMPTY

Table 8 STATUS REGISTER (SR)

SR1, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set, it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the CPU. If equal to zero, there is no new character in the Holding Register. This bit is cleared when the CPU reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{RxRDY}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. It is cleared when the transmitter is enabled by CR0 and does not indicate transmitter condition until at least one character is transmitted. It is also cleared when the Status Register is read by the CPU. When SR2 is set, the $\overline{TxEMT/DSCHG}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching the DLE Register has been received. However, only the first DLE of two successive DLEs will set SR3. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

The Overrun Error status bit, SR4, indicates that the previous character loaded into the Receive Holding Register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by the programmed number of stop bits. (If 1.5 stop bits are programmed, only the first stop bit is checked.) In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character is single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, and when the Status Register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. A low input sets its corresponding status bit and a high input clears it.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$ [4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low			0.8		
V_{IH}	High			2.0		
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA		0.25		
V_{OH}	High	I_{OH} = -100uA		2.8		
I_{IL}	Input load current	V_{IN} = 0 to 5.5V		10		μA
Tristate	Output leakage current					μA
I_{LH}	Data bus high	V_O = 4.0V		10		
I_{LL}	Data bus low	V_O = 0.45V		10		
I_{CC}	Power supply current			90		mA

PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design and process changes and improvements.

CAPACITANCE $T_A = 25°C$, $V_{CC} = 0V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Capacitance					pF
C_{IN} Input	fc = 1MHz			20	
C_{OUT} Output	Unmeasured pins tied to ground			20	
$C_{I/O}$ Input/Output				20	

PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design and process changes and improvements.

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6]

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Pulse width					ns
t_{RES} Reset			1000		
t_{CE} Chip enable			200		
Setup and hold time					ns
t_{AS} Address setup			10		
t_{AH} Address hold			10		
t_{CS} $\overline{R}/W$ control setup			10		
t_{CH} $\overline{R}/W$ control hold			10		
t_{DS} Data setup for write			150		
t_{DH} Data hold for write			80		
t_{RXS} Rx data setup			150		
t_{RXH} Rx data hold			280		
t_{DD} Data delay time for read	$C_L = 100pF$		180		ns
t_{DF} Data bus floating time for read	$C_L = 100pF$		70		ns
Input clock frequency					MHz
f_{BRG} Baud rate generator		5.0637	5.0688	5.0738	
$f_{R/T}$ $\overline{TxC}$ or $\overline{RxC}$		dc	1.0		
Clock state					ns
t_{BRH} Baud rate high			90		
t_{BRL} Baud rate low			90		
$t_{R/TH}$ $\overline{TxC}$ or $\overline{RxC}$ high (duty cycle)		44%	50%	56%	
$t_{R/TL}$ $\overline{TxC}$ or $\overline{RxC}$ low (duty cycle)		44%	50%	56%	
t_{TXD} TxD delay from falling edge of $\overline{TxC}$	$C_L = 100pF$		300		ns
t_{TCS} Skew between TxD changing and falling edge of $\overline{TxC}$ output[8]	$C_L = 100pF$		0		ns

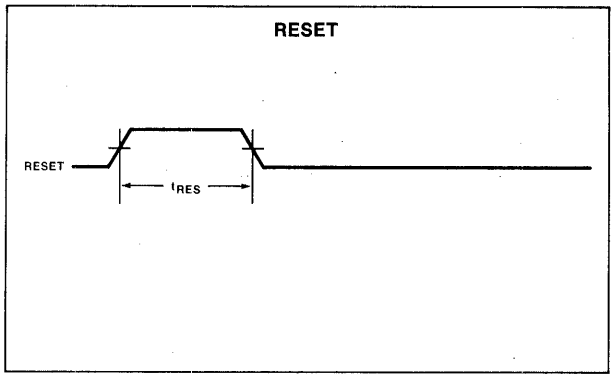
NOTES

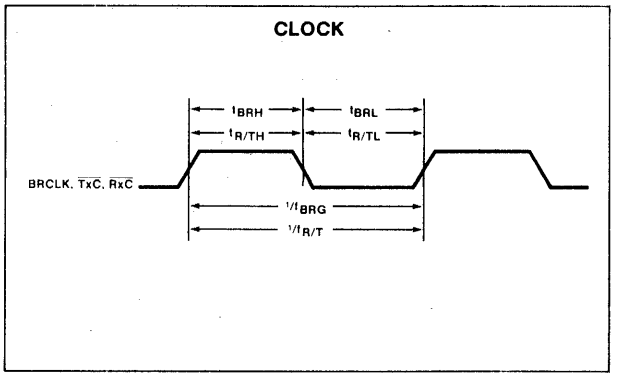
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (IQ ceramic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. All time measurements are at the V_{OH}, V_{OL}, V_{IH}, V_{IL} levels as appropriate.
6. Typical values are at +25°C, typical supply voltages and typical processing parameters.
7. $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT/DSCHG}$ outputs are open drain.
8. Parameter applies when internal transmitter clock is used.

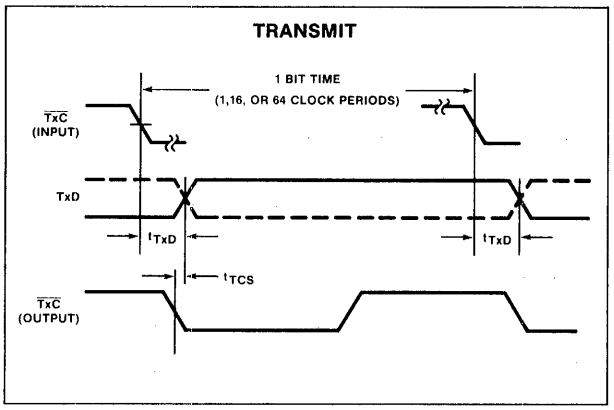
PRELIMINARY SPECIFICATION

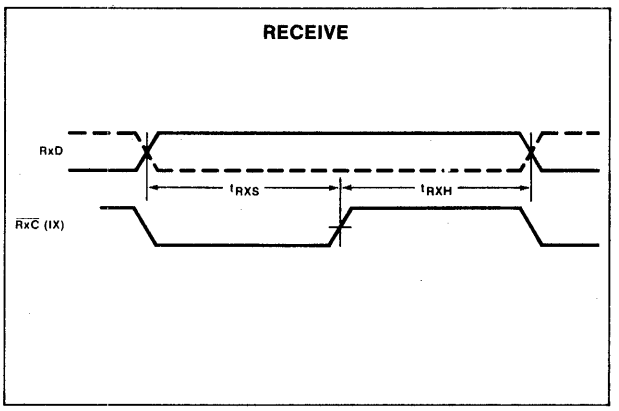
Manufacturer reserves the right to make design and process changes and improvements.

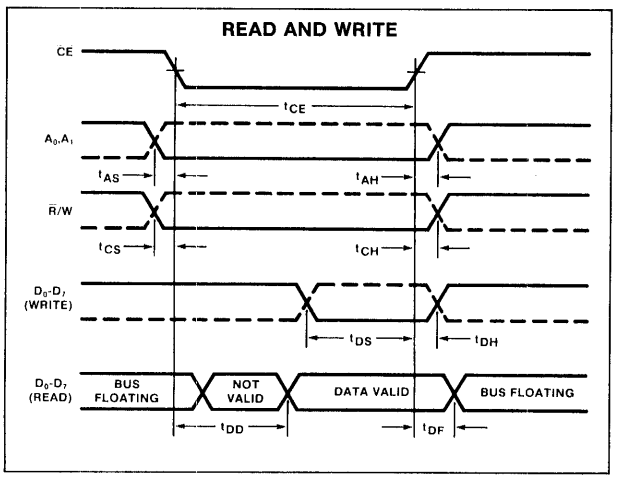
TIMING DIAGRAMS





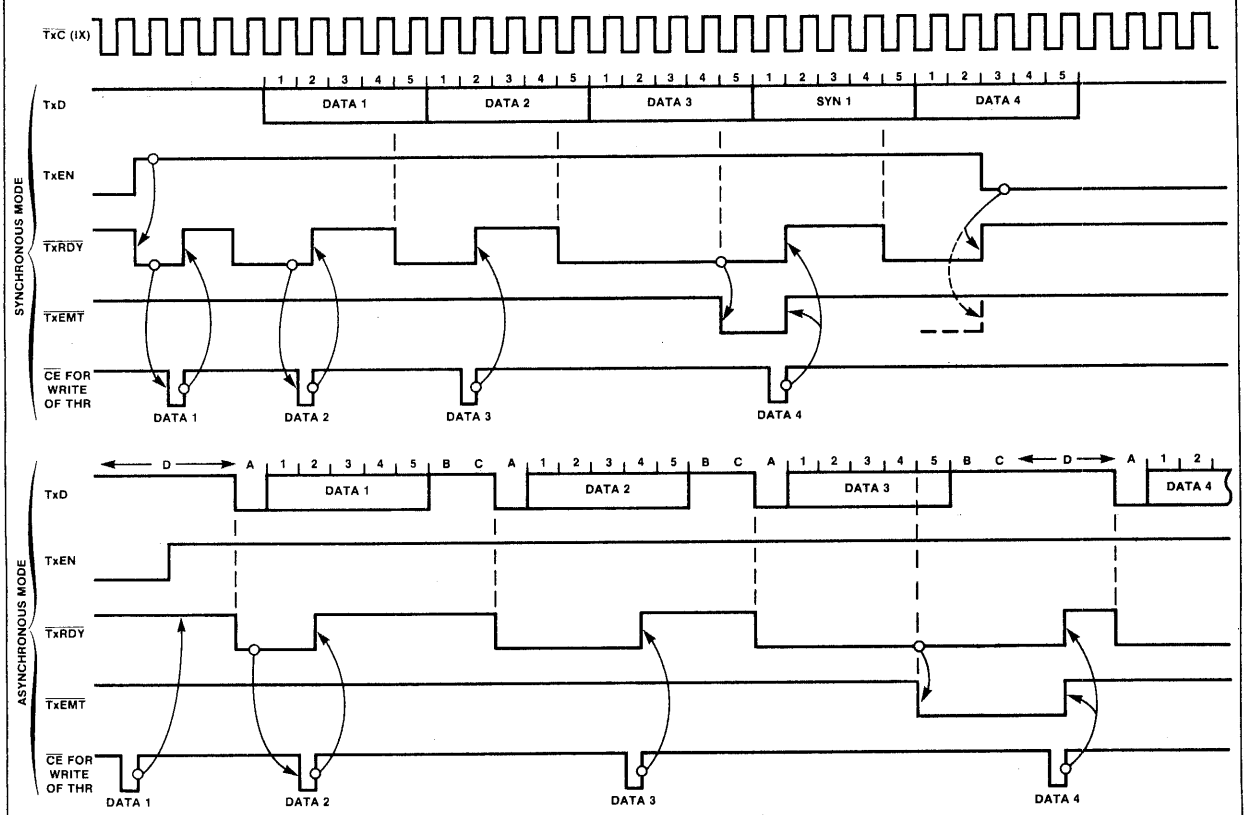






TIMING DIAGRAMS (Cont'd)

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



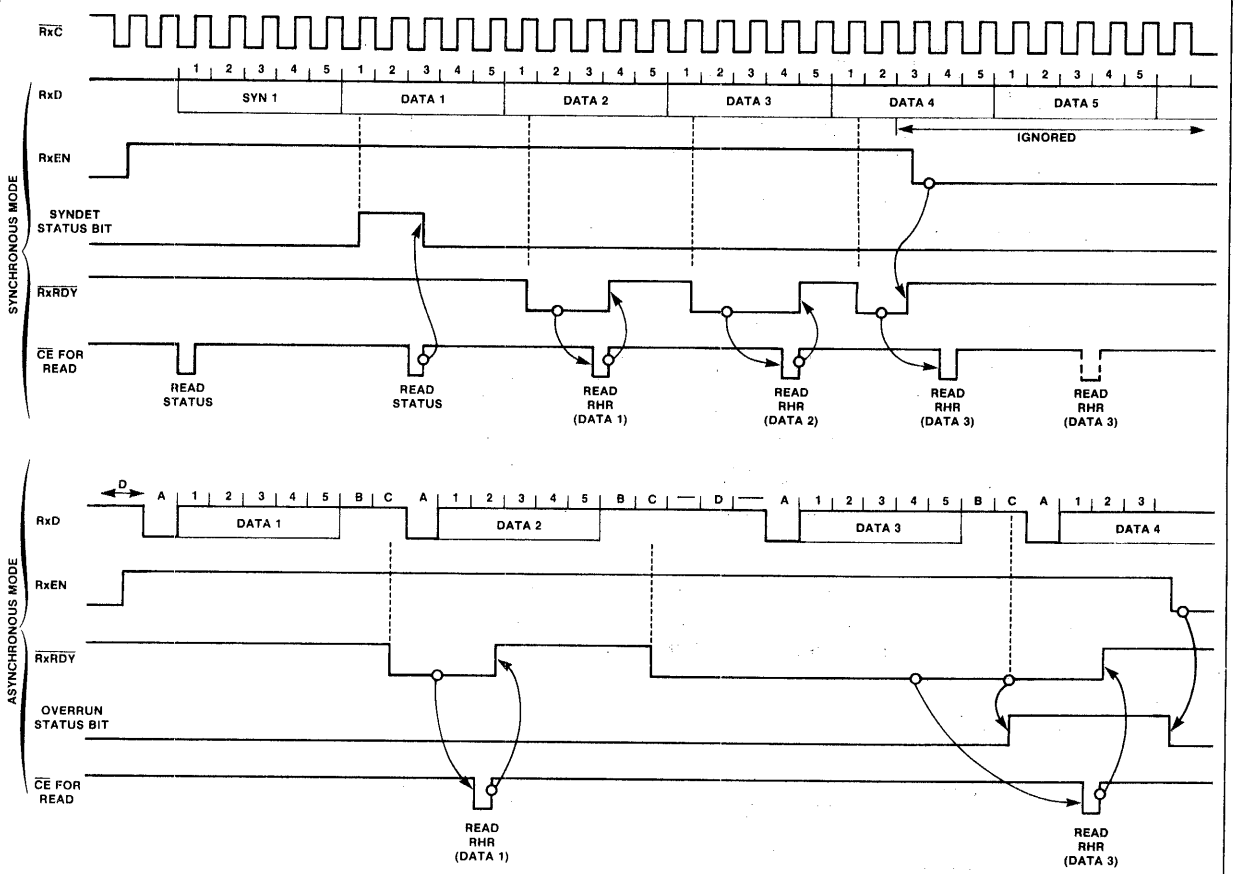
NOTES

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Cont'd)

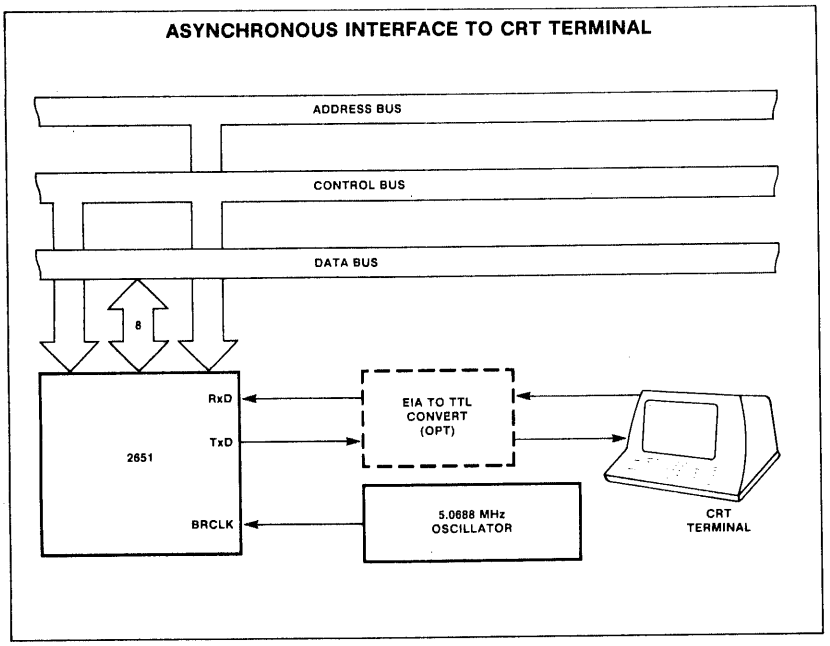
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

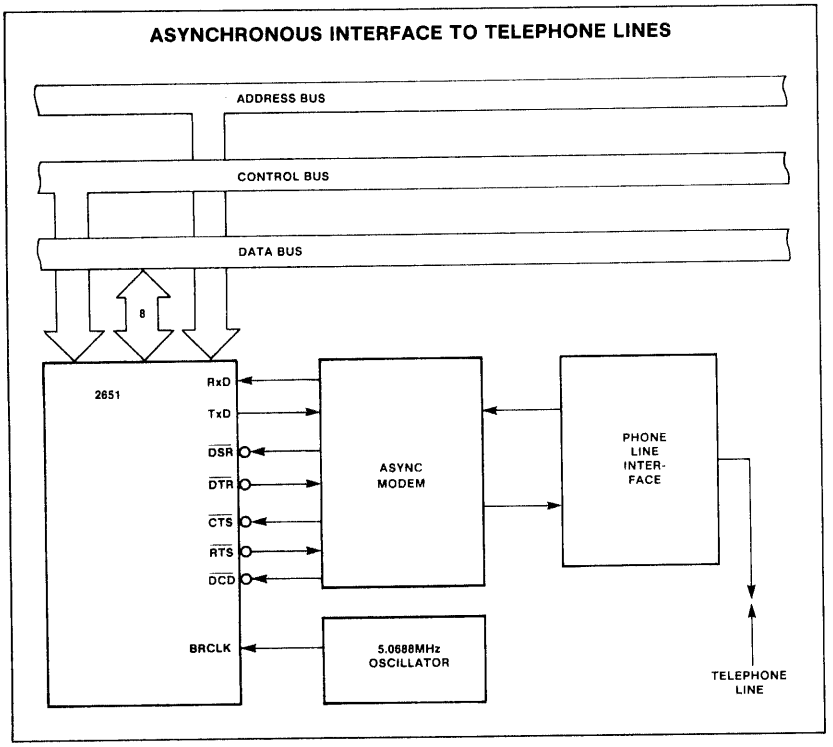


NOTES

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

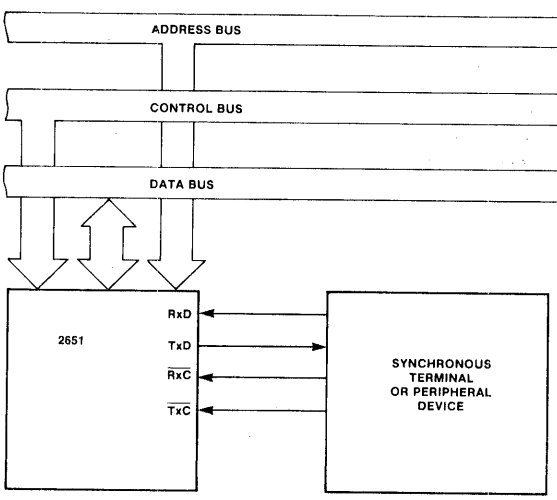
TYPICAL APPLICATIONS



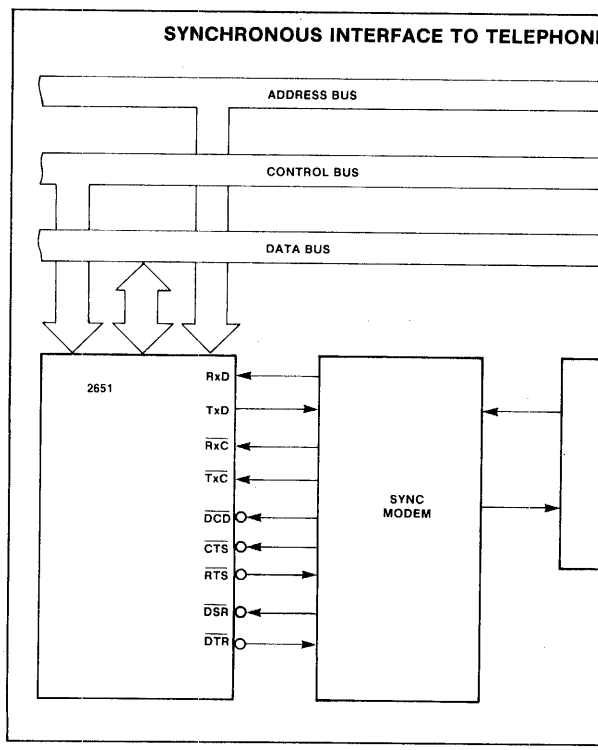


TYPICAL APPLICATIONS (Cont'd)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



DESCRIPTION

The 2652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

FEATURES

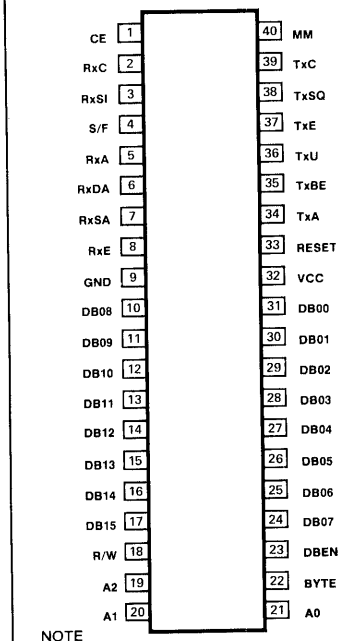
- **DC to 500K bps data rate**
- **Protocol management**
  Bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
  Byte-control protocols (BCP): BI-SYNC, DDCMP
- **Programmable operation**
  8 or 16-bit tri-state data bus
  Protocol selection—BOP or BCP
  Error control—CRC or VRC or no error check
  Character length—1 to 8 bits for BOP or 5 to 8 bits for BCP
  SYNC or secondary station address comparison for BCP-BOP
  Idle transmission of SYNC/FLAG or MARK for BCP-BOP
- **Automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA**
- **Zero insertion and deletion for BOP**
- **Short character detection for last BOP data character**
- **SYNC generation, detection, and stripping for BCP**
- **Maintenance Mode for self-testing**
- **Common parameter control registers**
- **Independent status and data registers for receive and transmit**
- **Status indicator signals can be used as CPU interrupts**
- **TTL compatible**
- **40-pin package**
- **Single +5V supply**

APPLICATIONS

- **Intelligent terminals**
- **Line controllers**
- **Network processors**
- **Front end communications**
- **Remote data concentractors**
- **Communication test equipment**
- **Computer to computer links**

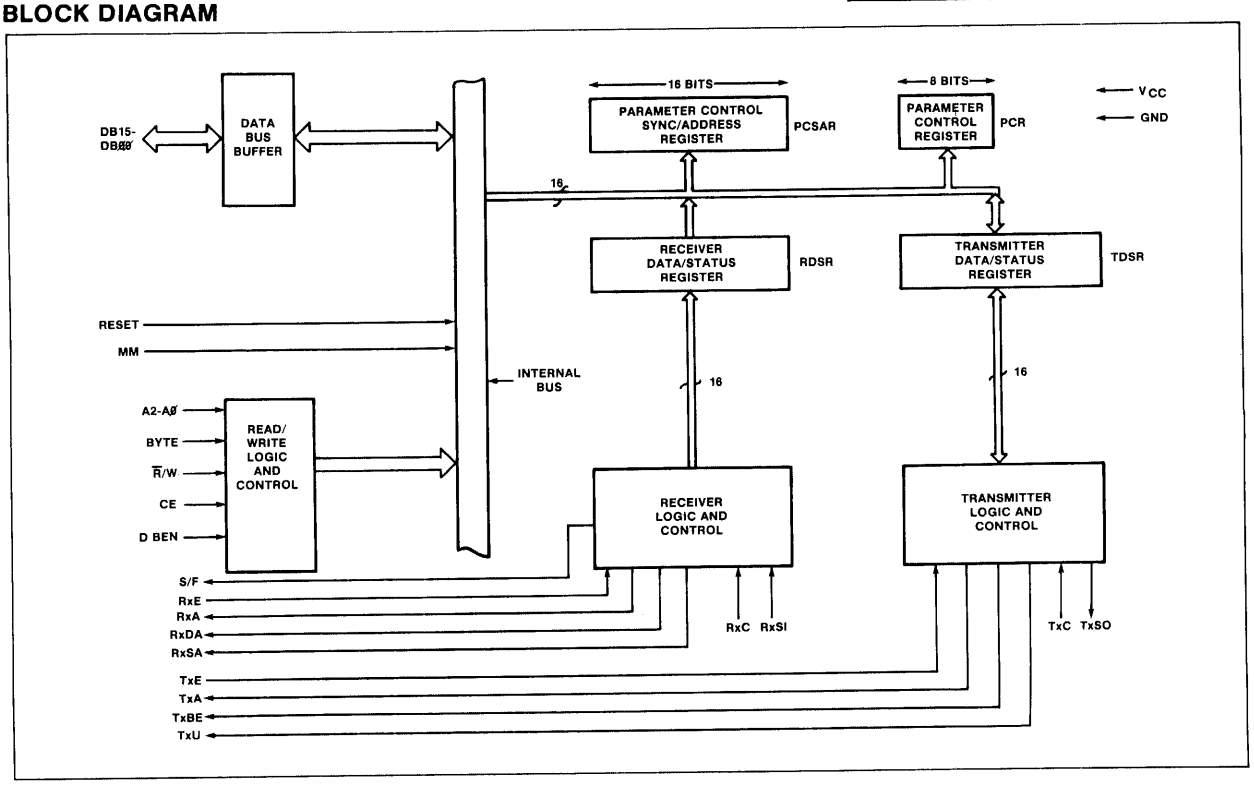
PIN CONFIGURATION

IWA PACKAGE



NOTE
00 is least significant bit, highest number (that is, DB15, A2) is most significant bit.

BLOCK DIAGRAM



PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB15-DB00	17-10 24-31	I/O	**Data Bus:** DB07-DB00 contain bidirectional data while DB15-DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be WIRE OR'ed onto an 8-bit data bus.
A2-A0	19-21	I	**Address Bus:** A2-A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	**Byte:** Single byte (8 bit) data bus transfers are specified when this input is high. A low level specifies 16 bit data bus transfers.
CE	1	I	**Chip Enable:** A high input permits a data bus operation when DBEN is activated.
$\overline{R}$/W	18	I	**Read/Write:** $\overline{R}$/W controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	**Data Bus Enable:** After A2-A0, CE, BYTE and $\overline{R}$/W are set up, DBEN may be strobed. During a read, the tri-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	**Reset:** A high level initializes all internal registers and timing.
MM	40	I	**Maintenance Mode:** MM internally gates TxSO back to RxSI and $\overline{TxC}$ to RxC for off line diagnostic purposes. The RxC input is disabled when MM is asserted.
RxE	8	I	**Receiver Enable:** A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	**Receiver Active:** RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC ($PCSAR_{13}$) is set, the first non-SYNC character is the first data character; if strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	**Receiver Data Available:** RxDA is asserted when an assembled character is in $RDSR_L$ and is ready to be presented to the processor. This output is reset when $RDSR_L$ is read.
RxC	2	I	**Receiver Clock:** RxC(1X) provides timing for the receiver logic. The positive going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	**SYNC/FLAG:** S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	**Receiver Status Available:** RxSA is asserted when there is a zero to one transition of any bit in $RDSR_H$ except for RSOM. It is cleared when $RDSR_H$ is read.
RxSI	3	I	**Receiver Serial Input:** RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	**Transmitter Enable:** A high level input enables the transmitter data path between $TDSR_L$ and TxS0. At the end of a message, a low level input causes TxS0 = 1 (mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output on TxS0.
TxA	34	O	**Transmitter Active:** TxA is asserted when TxE is high and TSOM ($TDSR_8$) is set. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxS0.
TxBE*	35	O	**Transmitter Buffer Empty:** TxBE is asserted when the TDSR is ready to be loaded with new control information or data. The processor should respond by loading the TDSR which resets TxBE.
TxU*	36	O	**Transmitter Underrun:** TxU is asserted during a transmit sequence when the service of TxBE has been delayed for more than one character time. This indicates the processor is not keeping up with the transmitter (TxS0 depends on $PCSAR_{11}$). TxU is reset by RESET or setting of TSOM ($TDSR_8$).
TxC	39	I	**Transmitter Clock:** TxC (1X) provides timing for the transmitter logic. The positive going edge shifts data out of the TxSR to TxS0.
TxSO	38	O	**Transmitter Serial Output.** TxS0 is the transmitted serial data. Mark = '1', space = '0'.
V_{CC}	32	I	**+5V:** Power supply.
GND	9	I	**Ground:** 0V reference ground.

*Indicates possible interrupt signal.

REGISTERS		NO. OF BITS	DESCRIPTION*
Addressable			
PCSAR	Parameter Control Sync/Address Register	16	PCSARH and PCR contain parameters common to the receiver and transmitter. $PCSAR_L$ contains a programmable SYNC character (BCP) or secondary station address (BOP).
PCR	Parameter Control Register	8	
RDSR	Receive Data/Status Register	16	$RDSR_H$ contains receiver status information. $RDSR_L$ = RxDB contains the received assembled character.
TDSR	Transmit Data/Status Register	16	$TDSR_H$ contains transmitter command and status information. $TDSR_L$ = TxDB contains the received assembled character.
Internal			
CCSR	Control Character Shift Register	8	These registers are used for character assembly (CCSR, HSR, RxSR), disassembly (TxSR), and CRC accumulation/generation (RxCRC, TxCRC).
HSR	Holding Shift Register	16	
RxSR	Receiver Shift Register	8	
TxSR	Transmitter Shift Register	8	
RxCRC	Receiver CRC Accumulation Register	16	
TxCRC	Transmitter CRC Generation Register	16	

NOTE

*H = High byte - bits 15-8
L = Low byte - bits 7-0

Table 1 GLOSSARY

CHARACTER	DESCRIPTION
FCS	Frame Check Sequence is transmitted/received as 16 bits following the last data character of a BOP message and is usually CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) with dividend preset to 1's.
BCC	Block Check Character is transmitted/received as two successive characters following the last data character of a BCP message. Either CRC-16 ($X^{16} + X^{15} + X^2 + 1$) with dividend preset to 0's or LRC ($X^8 + 1$) as computed by the processor, is polynomial. CRC-16 is used with 8-bit EBC DIC. LRC is used with 7-bit ASCII in conjunction with VRC. The CRC-16 is computed on all characters beginning with the first non-sync character at the start of the message.

Table 2 ERROR CONTROL

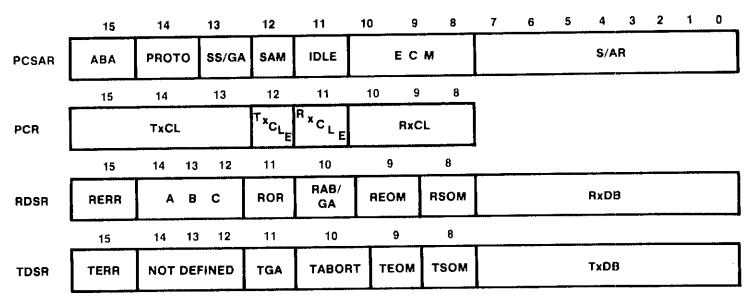
OPERATION	BIT PATTERN	FUNCTION
BOP		
FLAG	01111110	Frame message
ABORT	11111111 generation 01111111 detection	Terminate communication
GA	01111111	Terminate loop mode repeater function
Address	($PCSAR_L$)[1]	Secondary station address
BCP		
SYNC	($PCSAR_L$) or (TxDB)[2] generation	Frame message

NOTES

1. (α) refers to contents of α
2. For IDLE = 0 or 1 respectively

Table 3 SPECIAL CHARACTERS

SHORT FORM REGISTER BIT FORMATS



NOTE
Refer to Register Formats for mneumonics and description.

Figure 1

FUNCTIONAL DESCRIPTION

The MPCC can be functionally partitioned into receiver logic, transmitter logic, registers that can be read or loaded by the processor, and data bus control circuitry. The MPCC block diagram is shown in Figure 1 while the receiver and transmitter data paths are depicted in Figures 2 and 3.

MPCC RECEIVER DATA PATH

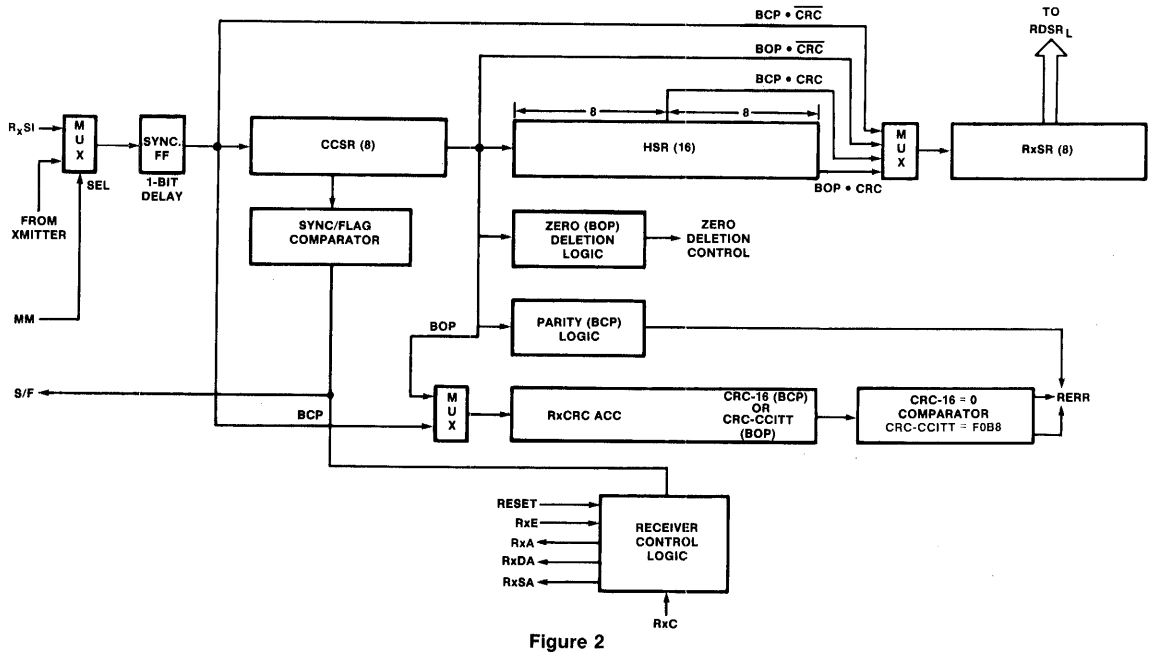
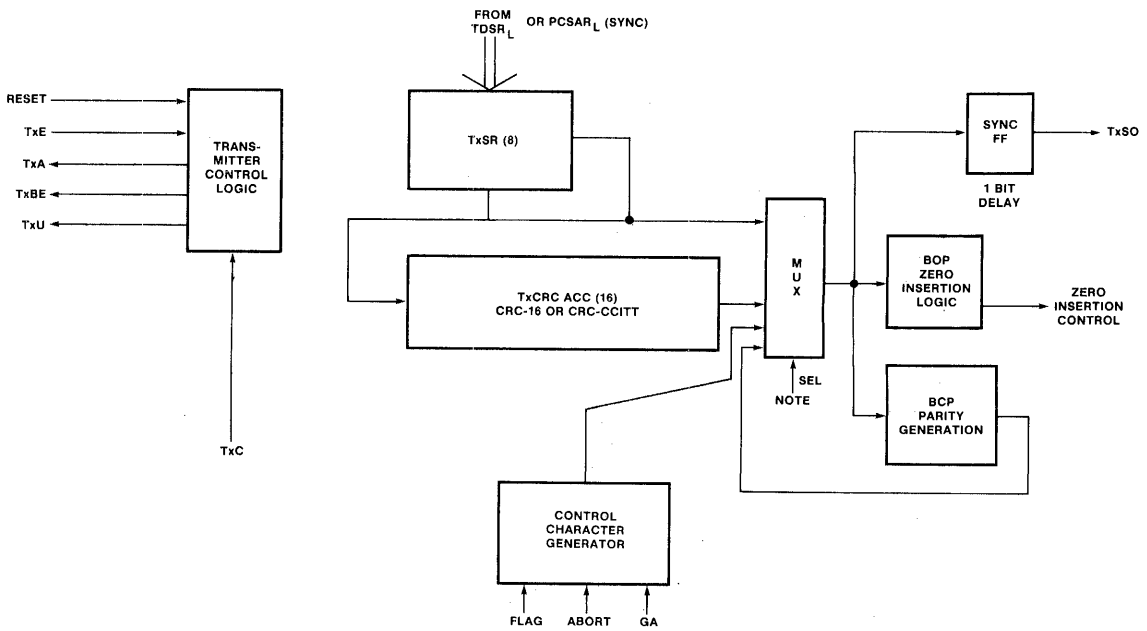


Figure 2

MPCC TRANSMITTER DATA PATH



NOTES

1. TxCRC selected if TEOM = 1 and the last data character has been shifted out of TxSR.
2. In BCP, parity selected will be generated after each character is shifted out of TxSR.

Figure 3

RECEIVER OPERATION

General

After initializing the parameter control registers (PCSAR and PCR), the RxE input must be set high to enable the receiver data path. The serial data on the RxSI is synchronized and shifted into an 8-bit Control Character Shift Register (CCSR) on the rising edge of RxC. A comparison between CCSR contents and the FLAG (BOP) or SYNC (BCP) character is made until a match is found. At that time, the S/F output is asserted for one RxC time and the 16-bit Holding Shift Register (HSR) is enabled. The receiver then operates as described below.

BOP Operation

A flow chart of receiver operation in BOP mode appears in Figure 4. Zero deletion (after five ones are received) is implemented on the received serial data so that a data character will not be interpreted as a FLAG, ABORT, or GA. Bits following the FLAG are shifted through the CCSR, HSR, and into the Receiver Shift Register (RxSR). A character will be assembled in the RxSR and transferred to the $RDSR_L$ for presentation to the processor. At that time the RxDA output will be asserted and the processor must take the character before the next character is assembled in the RxSR. If not, an overrun ($RDSR_{11}$ = 1) will occur and succeeding characters will be lost.

The first character following the FLAG is the secondary station address. If the MPCC is a secondary station ($PCSAR_{12}$ = 1), the contents of RxSR are compared with the address stored in $PCSAR_L$. A match indicates the forthcoming message is intended for the station; the RxA output is asserted, the character is loaded into $RDSR_L$, RxDA is asserted and the Receive Start of Message bit (RSOM) is set. No match indicates that another station is being addressed and the receiver searches for the next FLAG.

If the MPCC is receiving data from a secondary station ($PCSAR_{12}$ = 0), no secondary address check is made; RxA is asserted and RSOM is set once the first non-FLAG character has been loaded into $RDSR_L$ and RxDA has been asserted.

When the 8 bits following the address character have been loaded into $RDSR_L$ and RxDA has been asserted, RSOM will be cleared. The processor should read this 8-bit character and interpret it as the Control field.

Received serial data that follows is read and interpreted as the Information field by the processor. It will be assembled into character lengths as specified by PCR_{8-10}. As

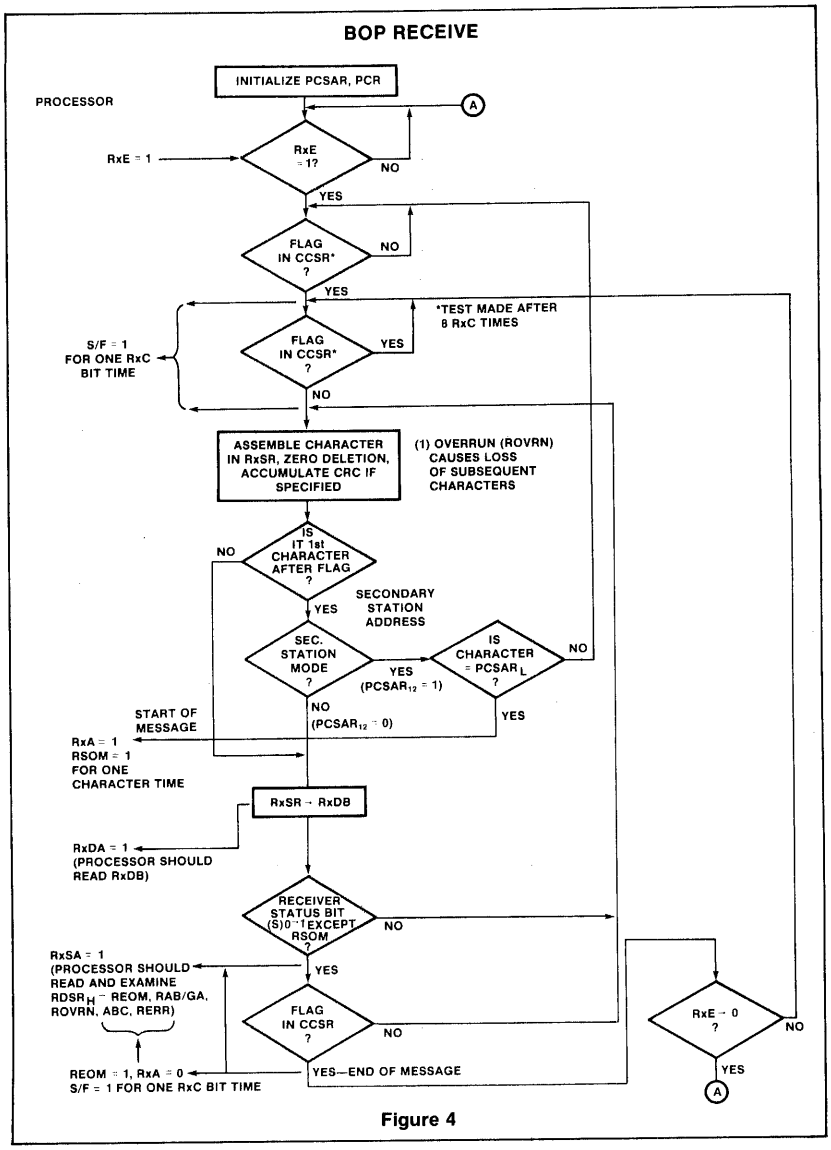


Figure 4

before, RxDA is asserted each time a character has been transferred into $RDSR_L$ and is cleared when $RDSR_L$ is read by the processor. RxSA is asserted when there is a zero to one transition for any bit in $RDSR_H$ except for RSOM. RxSA and all bits in $RDSR_H$ except RSOM are cleared when $RDSR_H$ is read. The processor should check $RDSR_{9-15}$ each time RxSA is asserted. If $RDSR_9$ is set, then $RDSR_{12-15}$ should be examined.

Receiver character length may be changed dynamically in response to RxDA: read the character in RxDB and write the new character length into RxCL. The character length will be changed on the next RxC positive going edge.

The CRC-CCITT, if specified by $PCSAR_{8-10}$, is accumulated in RxCRC on each character following the FLAG. When the closing FLAG is detected in the CCSR, the received CRC is in the 16-bit HSR. At that time, the Receive End of Message bit (REOM) will be set; RxSA and RxDA will be asserted. The processor should read the last data character in $RDSR_L$ and the receiver status in $RDSR_{9-15}$. If $RDSR_{15}$ = 1, there has been a

transmission error; the accumulated CRC-CCITT is incorrect. If $RDSR_{12-14} \neq 0$, the last data character is not of prescribed length. Neither the received CRC nor closing FLAG are presented to the processor. The processor may drop RxE or leave it active at the end of the received message.

BCP Operation

The operation of the receiver in BCP mode is shown in Figure 5. The receiver initially searches for two successive SYNC characters, of length specified by PCR_{8-10}, that match the contents of $PCSAR_L$. The next non-SYNC character or next SYNC character if stripping is not specified ($PCSAR_{13} = 0$), causes RxA to be asserted and enables the receiver data path from CCSR through HSR_L to RxSR. All characters following the first non-SYNC are assembled in RxSR and loaded into $RDSR_L$. RxDA is active when a character is available in $RDSR_L$. RxSA is active on a 0 to 1 transition of any bit in $RDSR_H$. The signals are cleared when $RDSR_L$ or $RDSR_H$ are read respectively.

If CRC-16 error control is specified by $PCSAR_{8-10}$, the processor must determine the last character received prior to the CRC field. When that character is loaded into $RDSR_L$ and RxDA is asserted, the received CRC will be in CCSR and HSR_L. To check for a transmission error, the processor must read the receiver status ($RDSR_H$) and examine $RDSR_{15}$. This bit will be set for one character time if an error free message has been received. If $RDSR_{15} = 0$, the CRC-16 is in error. Note that this bit should be examined only at the end of a message and that the accumulated CRC will include all characters starting with the first non-SYNC character at the start of the message. In particular, SYNC's in the middle of a message, DLE characters, and the first SOH or STX after line turn around are subject to CRC.

If VRC had been selected for error control, parity (odd or even) is regenerated on each character and check with the parity bit received. A discrepancy causes $RDSR_{15}$ to be set and RxSA to be asserted. This must be sensed by the processor. The received parity bit is stripped before the character is presented to the processor. The processor should compute and check LRC if required.

When the processor has read the last character of the message, it should drop RxE which disables the receiver logic and initializes all receiver registers and timing.

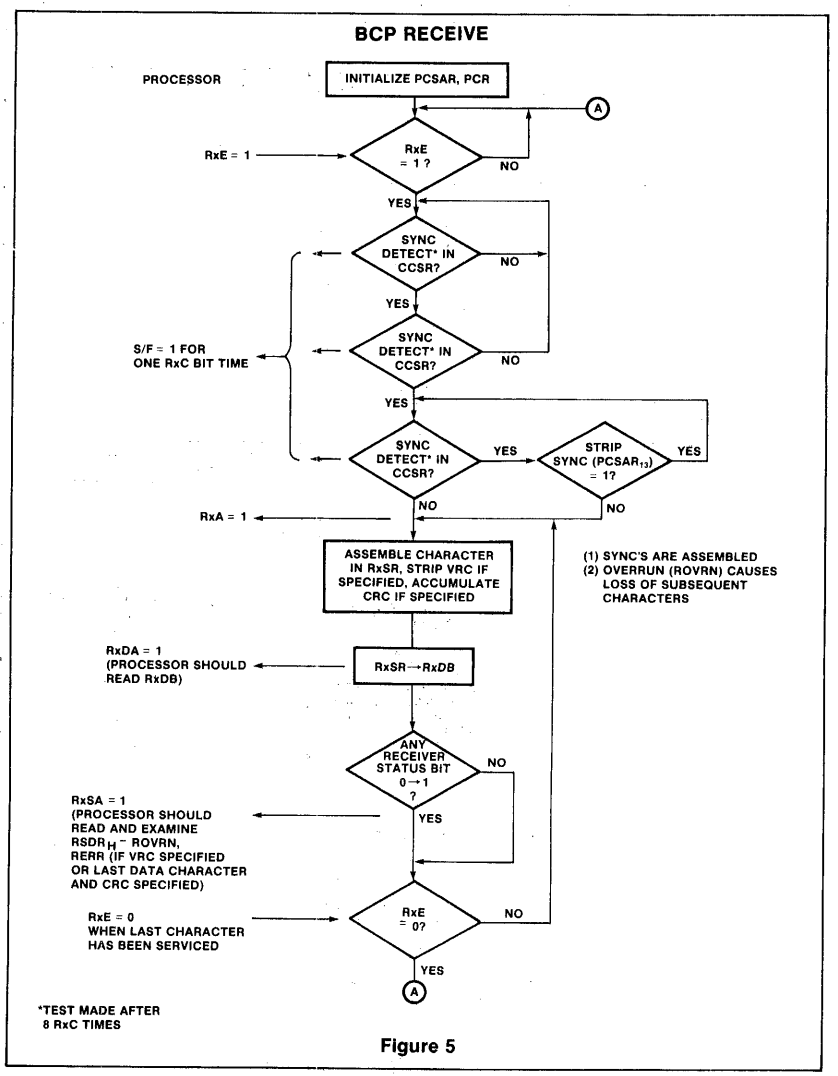


Figure 5

TRANSMITTER OPERATION

General

After the parameter control register (PCSAR and PCR) have been initialized, TxE must be set high to enable the transmitter data path. TxSO is held to mark until TSOM ($TDSR_8$) is set. Then, transmitter operation depends on protocol mode.

BOP Operation

Transmitter operation for BOP is shown in Figure 6. A FLAG is sent when the processor sets the Transmit Start of Message bit (TSOM). The FLAG is used to synchronize the message that follows. TxA will be asserted after TSOM is set. When TxBE is asserted by the MPCC, the processor should load $TDSR_L$ with the first character of the message. TSOM should be cleared at the same time $TDSR_L$ is loaded (16-bit data bus) or immediately thereafter (8-bit data bus). FLAGs are sent as long as TSOM = 1.

All succeeding characters are loaded into $TDSR_L$ by the processor when TxBE =1. Each character is serialized in TxSR and transmitted on TxSO. Internal zero insertion logic stuffs a "0" into the serial bit stream after five successive "1s" are sent. This insures a data character will not match a FLAG, ABORT, or GA reserved control character. As each character is transmitted, the Frame Check Sequence (FCS) is generated as specified by Error Control Mode ($PCSAR_{8-10}$). The FCS should be the

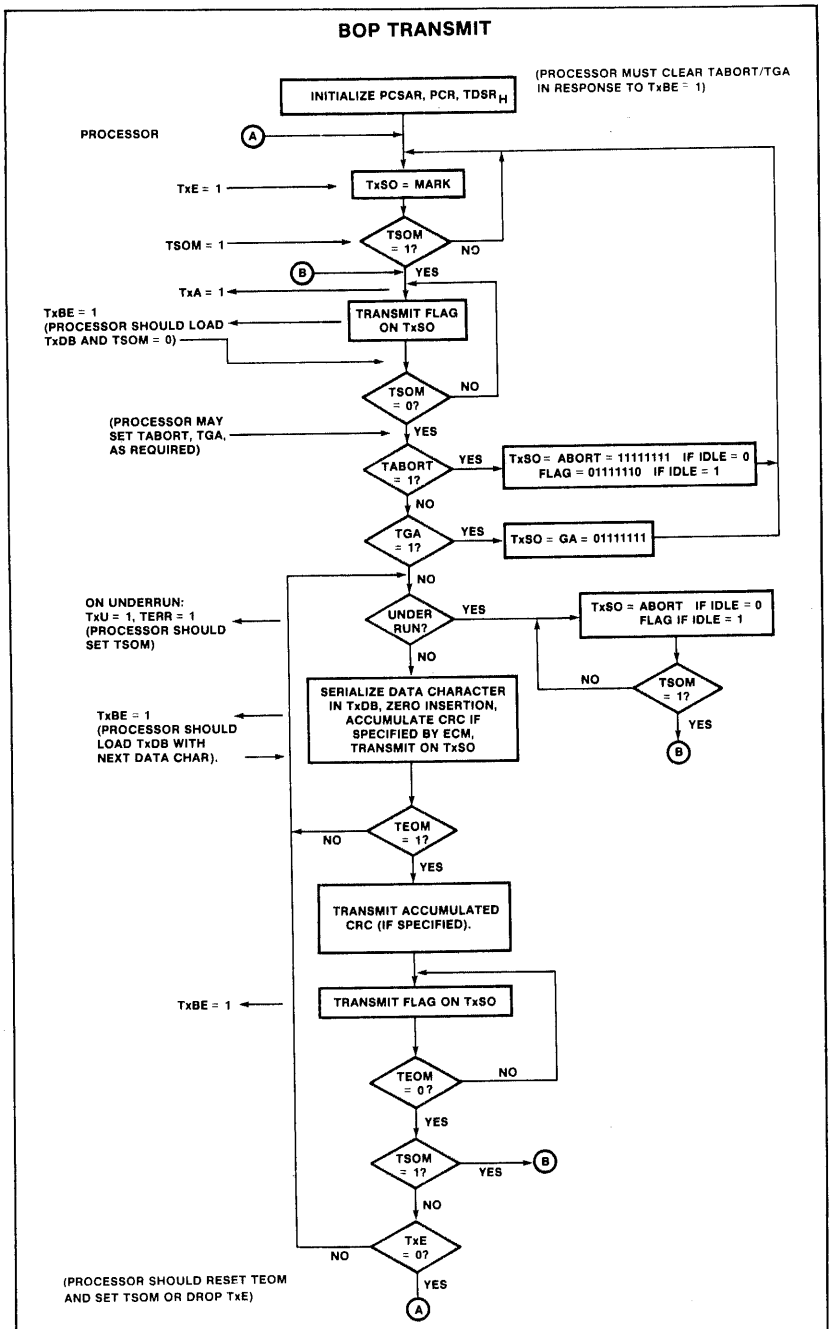


Figure 6

CRC-CCITT polynomial)$X^{16} + X^{12} + X^5 + 1$) preset to 1s. If an underrun occurs (processor is not keeping up with the transmitter), TxU and TERR ($TDSR_{15}$) will be asserted with ABORT or FLAG used as the TxSO line fill depending on the state of IDLE ($PCSAR_{11}$). The processor must set TSOM and retransmit the message to recover.

A residual character of 3 to 7 bits may be transmitted at the end of BOP information field to make sure that field is a multiple of 8 bits. In response to TxBE, write the residual character length into TxCL and load TxDB with the residual character. Dynamic alteration of character length should be done in exactly the same sequence.

After the last data character has been loaded into $TDSR_L$ and sent to TxSR (TxBE = 1), the processor should set TEOM ($TDSR_9$). The MPCC will finish transmitting the last character followed by the FCS and the closing FLAG. The processor should clear TEOM and drop TxE when the next TxBE is asserted. This corresponds to the start of closing FLAG transmission. When TxE has been dropped, TxA will be low $1\frac{1}{2}$ bit times after the last bit of the closing FLAG has been transmitted. TxSO will be marked after the closing FLAG has been transmitted.

If TxE and TEOM are high, the transmitter continues to send FLAGs. The processor may initiate the next message by resetting TEOM and setting TSOM, or by loading $TDSR_L$ with a data character and then simply resetting TEOM (without setting TSOM).

BCP Operation

Transmitter operation for BCP mode is shown in Figure 7. If TxE is high, TxA will be asserted when TSOM = 1. At that time SYNC characters are sent from $PCSAR_L$ or $TDSR_L$ (IDLE = 0 or 1) as long as TSOM = 1. TxBE is asserted at the start of transmission of the first SYNC character. For more than one SYNC, the processor should reassert TSOM in response to the assertion of TxBE. When TSOM = 0 transmission is from $TDSR_L$, which must be loaded with characters from the processor each time TxBE is asserted. If this loading is delayed for more than one character time, an underrun results: TxU and TERR are asserted and the TxSO line fill depend on IDLE ($PCSAR_{11}$). The processor must set TSOM and retransmit the message to recover.

CRC-16, if specified by $PCSAR_{8-10}$, is generated on each character transmitted from $TDSR_L$ when TSOM = 0. The processor must set TEOM = 1 after the last data character has been sent to TxSR (TxBE = 1). The MPCC will finish transmitting the last data

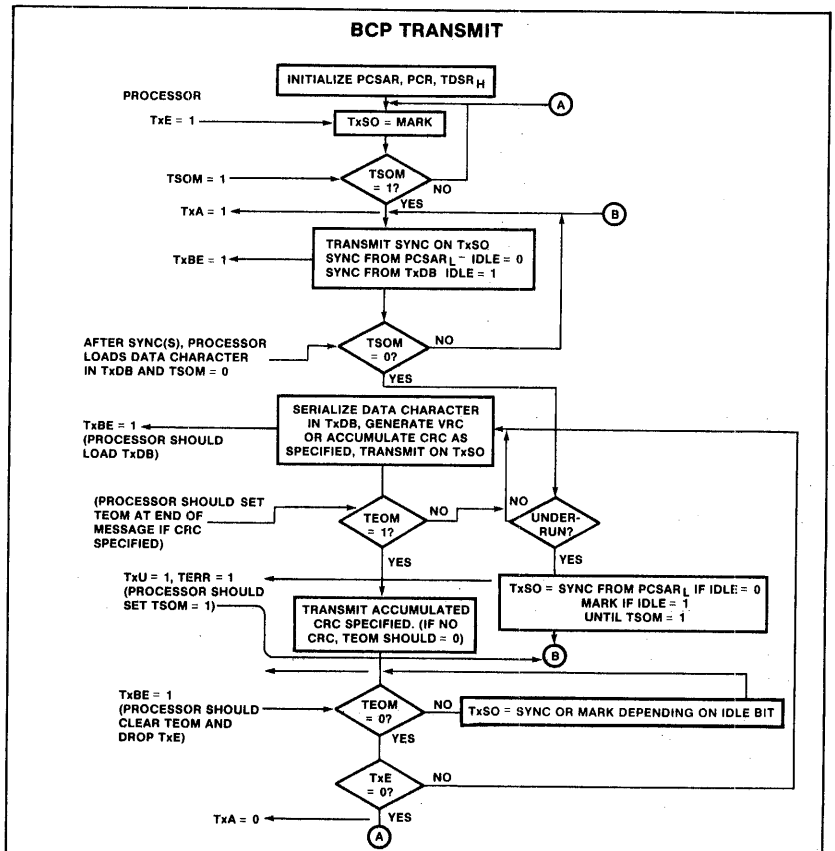


Figure 7

character and the CRC-16 field before sending SYNC characters which are transmitted as long as TEOM = 1. If SYNCs are not desired after CRC-16 transmission, the processor should clear TEOM and lower TxE when the TxBE corresponding to the start of CRC-16 transmission is asserted. When TEOM = 0, the line is marked and a new message may be initiated by setting TxE and TSOM.

If LRC is required, it must be generated by the processor and transmitted after the last data character. TEOM should not be set under this condition. If VRC is specified, it is generated on each data character and the data character length must not exceed 7 bits. For software LRC or CRC TEOM should be set only if SYNCs are required at the end of the message block.

SPECIAL CASE

The capability to transmit 16 spaces is provided for line turnaround in half duplex mode or for a control recovery situation. This is achieved by setting TSOM and TEOM, clearing TEOM when TxBE = 1, and proceeding as required.

PROGRAMMING

Prior to initiating data transmission or reception, PCSAR and PCR must be loaded with control information from the processor. The contents of these registers (see Register Format section) will configure the MPCC for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is disabled.

The default value for all registers is zero. This corresponds to BOP, primary station mode, 8-bit character length, FCS = CRC-CCITT preset to 1s.

For BOP mode the character length register (PCR) may be set to the desired values during system initialization. The address and control fields will automatically be 8-bits. If a residual character is to be transmitted, TxCL should be changed to the residual character length prior to transmission of that character.

DATA BUS CONTROL

The processor must set up the MPCC register address (A2-A0), chip enable (CE), byte select (BYTE), and read/write ($\overline{R}$/W) inputs before each data bus transfer operation.

During a read operation ($\overline{R}$/W = 0), the leading edge of DBEN will initiate an MPCC read cycle. The addressed register will place its contents on the data bus. If BYTE = 1, the 8-bit byte is placed on DB15-08 or DB07-00 depending on the H/L status of the register addressed. Unused bits in RDSR$_L$ are zero. If BYTE = 0, all 16 bits (DB15-00) contain MPCC information. The trailing edge of DBEN will reset RxDA and/or RxSA if RDSR$_H$ or RDSR$_L$ is addressed respectively.

DBEN acts as the enable and strobe so that the MPCC will not begin its internal read cycle until DBEN is asserted.

During a write operation ($\overline{R}$/W = 1), data must be stable on DB$_{15-08}$ and/or DB$_{07-00}$ prior to the leading edge of DBEN. The stable data is strobed into the addressed register by DBEN. TxBE will be cleared if the addressed register was TDSR$_H$ or TDSR$_L$.

	A2	A1	A0	REGISTER
BYTE = 0	**16-BIT DATA BUS = DB_{15} - DB_{00}**			
	0	0	X	RDSR
	0	1	X	TDSR
	1	0	X	PCSAR
	1	1	X	PCR*
BYTE = 1	**8-BIT DATA BUS = DB_{7-0} or DB_{15-8}****			
	0	0	0	$RDSR_L$
	0	0	1	$RDSR_H$
	0	1	0	$TDSR_L$
	0	1	1	$TDSR_H$
	1	0	0	$PCSAR_L$
	1	0	1	$PCSAR_H$
	1	1	0	PCR_L*
	1	1	1	PCR_H

NOTES

* PCR lower byte does not exist. It will be all "0"s when read.

** Corresponding high and low order pins should be tied together.

Table 4 MPCC REGISTER ADDRESSING

BIT	NAME	MODE	FUNCTION
00-07	Not Defined		
08-10	RxCL	BOP/BCP	Receiver Character Length is loaded by the processor depending on RxBC when RxCLE = 0. **10 9 8 — Char. length (bits)** 0 0 0 — 8 0 0 1 — 1 0 1 0 — 2 0 1 1 — 3 1 0 0 — 4 1 0 1 — 5 1 1 0 — 6 1 1 1 — 7
11	RxCLE	BOP/BCP	Receiver Character Length Enable should be zero when the processor loads RxCL. The remaining bits of PCR are not affected during loading.
12	TxCLE	BOP/BCP	Transmitter Character Length Enable should be zero when the processor loads TxCL. The remaining bits of PCR are not affected during loading.
13-15	TxCL	BOP/BCP	Transmitter Character Length is loaded by the processor when TxCLE = 0. Character bit length specification format is identical to RxCL.

Table 5 PARAMETER CONTROL REGISTER (PCR)-(R/W)

BIT	NAME	MODE	FUNCTION
00-07	S/AR	BOP	SYNC/ADDRESS Register. Contains the secondary station address if the MPCC is a secondary station. The contents of this register is compared with the first received non-FLAG character to determine if the message is meant for this station.
		BCP	SYNC character is loaded into this register by the processor. It is used for receive and transmit bit synchronization with bit length specified by RxCL and TxCL.
08-10	ECM	BOP/BCP	**Error Control Mode** / **10** / **9** / **8** / **Mode** / **Char. length** CRC-CCITT preset to 1's / 0 / 0 / 0 / BOP / 1-8 CRC-CCITT preset to 0's / 0 / 0 / 1 / BOP / 1-8 Not used / 0 / 1 / 0 / --- / CRC-16 preset to 0's / 0 / 1 / 1 / BCP / 8 VRC old / 1 / 0 / 0 / BCP / 5-7 VRC even / 1 / 0 / 1 / BCP / 5-7 Not used / 1 / 1 / 0 / --- / No error control / 1 / 1 / 1 / BCP / 5-8 ECM should be loaded by the processor during initialization or when both data paths are idle.
11	IDLE		Determines line fill character to be used if transmitter underrun occurs (TxU asserted and TERR set) and transmission of special characters for BOP/BCP.
		BOP	IDLE = 0, transmit ABORT characters during underrun and when TABORT = 1. IDLE = 1, transmit FLAG characters during underrun and when TABORT = 1.
		BCP	IDLE = 0 transmit initial SYNC characters and underrun line fill characters from the S/AR. IDLE = 1 transmit initial SYNC characters from TxDB and marks TxSO during underrun.
12	SAM	BOP	Secondary Address Mode = 1 if the MPCC is a secondary station. This facilitates automatic recognition of the received secondary station address. When transmitting, the processor must load the secondary address into TxDB. SAM = 0 inhibits the received secondary address comparison which serves to activate the receiver after the first non-FLAG character has been received.
13	SS/GA	BOP	Strip SYNC/Go Ahead. Operation depends on mode. For loop mode only. SS/GA = 1 permits GA character to terminate a received message. When a GA is detected REOM and RAB/GA will be set and the processor should terminate the repeater function. SS/GA = 0 permits only a FLAG or ABORT character to terminate a message.
		BCP	SS/GA = 1, causes the receiver to strip SYNC's immediately following the first two SYNC's detected. SYNC's in the middle of a message will not be stripped. SS/GA = 0, presents any SYNC's after the initial two SYNC's to the processor.
14	PROTO		Determines MPCC Protocol mode
		BOP	PROTO = 0 BOP
		BCP	PROTO = 1 BCP
15	APA	BOP	All Parties Address. If this bit is set, the receiver data path is enabled by an address field of '11111111' as well as the normal secondary station address.

Table 6 PARAMETER CONTROL SYNC/ADDRESS REGISTER (PCSAR)-(R/W)

BIT	NAME	MODE	FUNCTION
00-07	TxDB	BOP/BCP	Transmit Data Buffer. Contains processor loaded characters to be serialized in TxSR and transmitted on TxSO.
08	TSOM	BOP	Transmitter Start of Message. Set by the processor to initiate message transmission provided TxE = 1. TSOM = 1 generates FLAGs. When TSOM = 0 transmission is from TxDB and FCS generation begins. FCS, as specified by $PCSAR_{8-10}$, should be CRC-CCITT preset to 1's.
		BCP	TSOM = 1 generates SYNCs from $PCSAR_L$ or transmits from TxDB for IDLE = 0 or 1 respectively. When TSOM = 0 transmission is from TxDB and CRC generation (if specified) begins.

Table 7 TRANSMIT DATA/STATUS REGISTER (TDSR) (R/W except TDSR 15)

BIT	NAME	MODE	FUNCTION
09	TEOM	BOP	Transmit End of Message. Used to terminate a transmitted message when CRC error checking is used. TEOM = 1 causes the FCS and the closing FLAG to be transmitted following the transmission of the data character in TxSR. FLAGs are transmitted until TEOM = 0. ABORT or GA are transmitted if TABORT or TGA are set when TEOM = 1.
		BCP	TEOM = 1 causes CRC-16 to be transmitted (if selected) followed by SYNCs from $PCSAR_L$ or TxDB (IDLE = 0 or 1). Clearing TEOM prior to the end of CRC-16 transmission (when TxBE = 1) causes TxSO to be marked following the CRC-16. TxE must be dropped before a new message can be initiated. If CRC is not selected, TEOM should not be set.
10	TABORT	BOP	Transmitter Abort = 1 will cause ABORT or FLAG to be sent (IDLE = 0 or 1) after the current character is transmitted. (ABORT = 11111111)
11	TGA	BOP	Transmit Go Ahead (GA) instead of FLAG when TEOM = 1. This facilitates repeater termination in loop mode. (GA = 01111111)
12-14	Not Defined		
15	TERR	Read only BOP BCP	Transmitter Error = 1 indicates the TxDB has not been loaded in time to maintain continous transmission. TxU will be asserted to inform the processor of this condition. TERR is cleared by setting TSOM. ABORT's or FLAG's are sent as fill characters (IDLE = 0 or 1) SYNC's or MARK's are sent as fill characters (IDLE = 0 or 1). For IDLE = 1 the last character before underrun is not valid.

Table 7 TRANSMIT DATA/STATUS REGISTER (TDSR) (R/W except TDSR 15) (Cont'd)

BIT	NAME	MODE	FUNCTION
00-07	RxDB	BOP/BCP	Receiver Data Buffer. Contains assembled characters from the RxSR. If VRC is specified, the parity bit is stripped.
08	RSOM	BOP	Receiver Start of Message = 1 when a FLAG followed by a non-FLAG has been received and the latter character matches the secondary station address if SAM = 1. RxA will be asserted when RSOM = 1. RSOM resets itself after one character time and has no effect on RxSA.
09	REOM	BOP	Receiver End of Message = 1 when the closing FLAG is detected and the last data character is loaded into RxDB or when an ABORT/GA character is received. REOM is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
10	RAB/GA	BOP	Received ABORT or GA character = 1 when the receiver senses an ABORT character if SS/GA = 0 or a GA character if SS/GA = 1. RAB/GA is cleared on reading $RDSR_H$, reset operation, or dropping of RxE. A received ABORT inhibits RxDA.
11	ROR	BOP/BCP	Receiver Overrun = 1 indicates the processor has not read the last character in the RxDB within one character time. Subsequent characters will be lost. ROR is cleared on reading $RDSR_H$, reset operation, or dropping or RxE.
12-14	ABC	BOP	Assembled Bit Count. Specifies the number of bits in the last received data character of a message and should be examined by the processor when REOM = 1 (RxDA and RxSA asserted). ABC = 0 indicates the message was terminated (by a FLAG or GA) on a character boundary as specified by $PCSCR_{8-10}$. Otherwise, ABC = number of bits in the last data character. ABC is cleared when $RDSR_H$ is read, reset operation, or dropping RxE. The residual character is right justified in $RDSR_L$.
15	RERR	BOP BCP	Receiver Error indicator should be examined by the processor when REOM = 1 in BOP, or when the processor determines the last data character of the message in BCP with CRC or when RxSA is set in BCP with VRC. CRC-CCITT preset to 1's should be specified by $PCSAR_{8-10}$: RERR = 1 indicates FCS error (CRC ≠ F0B8) RERR = 0 indicates FCS received correctly (CRC = F0B8) CRC-16 preset to 0's on 8-bit data characters specified by $PCSAR_{8-10}$: RERR = 1 indicates CRC-16 received correctly (CRC-0). RERR = 0 indicates CRC-16 error (CRC ≠ 0) VRC specified by $PCSAR_{8-10}$: RERR = 1 indicates VRC error RERR = 0 indicates VRC is correct

Table 8 RECEIVER DATA/STATUS REGISTER (RDSR)-(Read Only)

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
	Input or output voltages with respect to GND[3]	-0.3 to +15	V
V_{CC}	With respect to GND	-0.3 to+7	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low				0.8	
V_{IH}	High		2.0			
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.4	
V_{OH}	High	$I_{OH} = -100\mu A$	2.4			
I_{CC}	Power supply current	$V_{CC} = 5.25V$, $T_A = 0°C$			150	mA
	Leakage current					μA
I_{IL}	Input	$V_{IN} = 0$ to 5.25V			10	
I_{OL}	Output	$V_{OUT} = 0$ to 5.25V			10	
	Capacitance					pF
C_{IN}	Input	$V_{IN} = 0V$, f = 1MHz			20	
C_{OUT}	Output	$V_{OUT} = 0V$, f = 1MHz			20	

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V \pm 5\%$, AC timing indicated is with outputs unloaded.[4,5,6]

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
	Setup and hold time				ns
t_{ACS}	Address/control setup	50			
t_{ACH}	Address/control hold	0			
t_{DS}	Data bus setup (write)	50			
t_{DH}	Data bus hold (write)	0			
t_{RXS}	Receiver serial data transfer	150			
t_{RxH}	Receive serial data hold	150			
	Pulse width				ns
t_{RES}	RESET	250			
t_{DBEN}	DBEN	250			
	Delay time				ns
t_{DD}	Data bus (read)			200	
t_{TxD}	Transmit serial data			300	
t_{DF}	Data bus float time (read)			150	ns
f	Clock (RxC, TxC) frequency			500	kHz
t_{CLK1}	Clock high	1000			ns
t_{CLK0}	Clock low	1000			ns

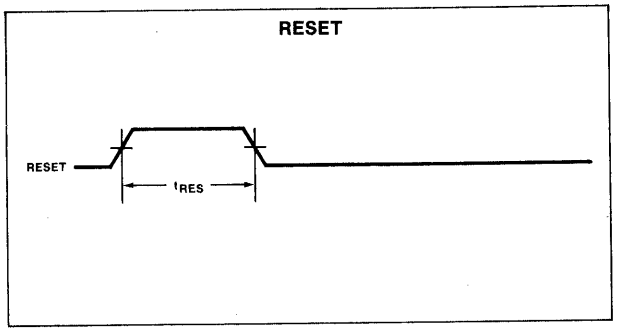
NOTES

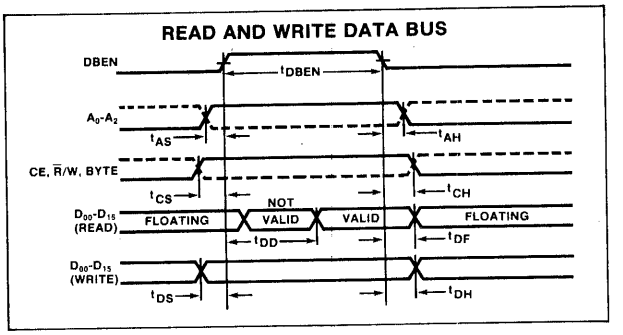
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60° C/W junction to ambient (IQ ceramic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. All time measurements are at the V_{OH}, V_{OL}, V_{IH}, or V_{IL} levels as appropriate.
6. Typical values are at +25°C, nominal supply voltages, and nominal processing parameters.

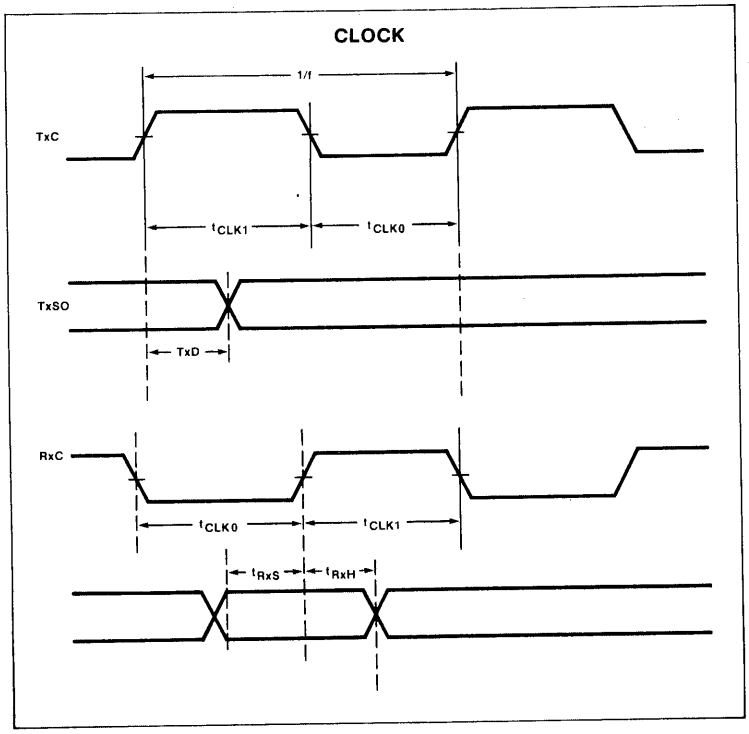
PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design and process changes and improvements.

TIMING DIAGRAMS

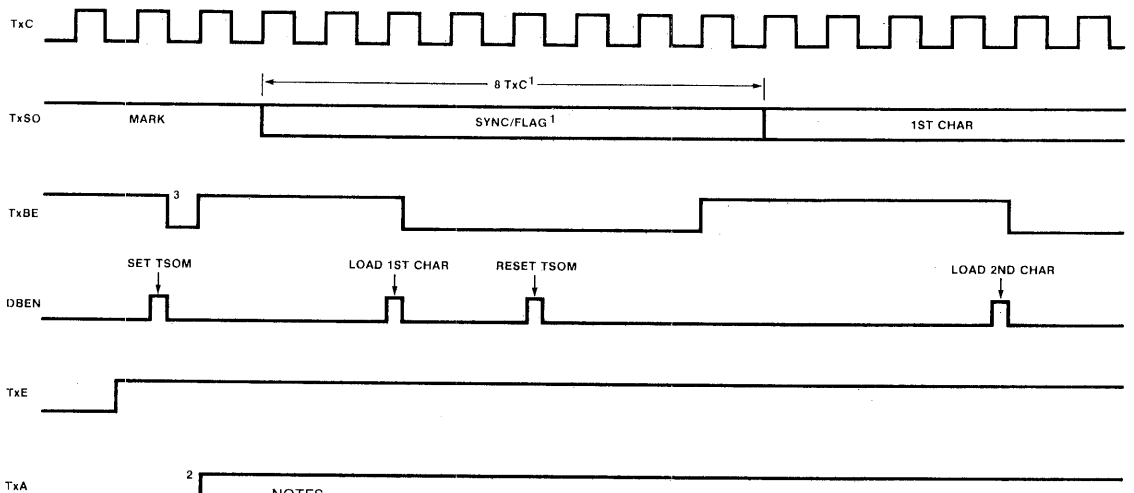






TIMING DIAGRAMS (Cont'd)

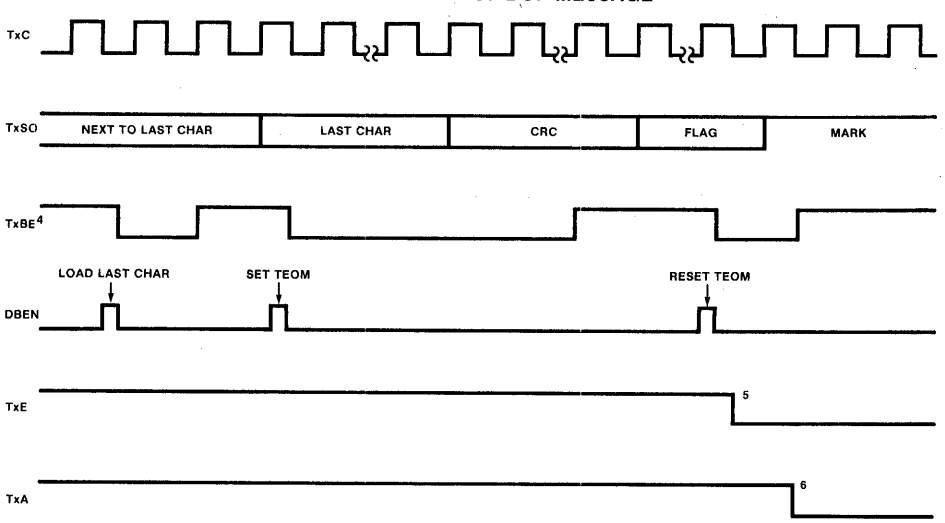
TRANSMIT—START OF MESSAGE



NOTES

1. SYNC may be 5 to 8 bits and will contain parity bit as specified.
2. TxA goes high relative to TxC rising edge after TxE has been raised and TSOM has been set.
3. TxBE goes low relative to DBEN falling edge on the first write transfer into TSDR after TxE has been raised. It is reasserted 1 TxC time before the first bit of the transmitted SYNC/FLAG. TxBE then goes low relative to DBEN falling edge when writing into $TDSR_H$ and/or $TDSR_L$. It is reasserted on the rising edge of the TxC that corresponds to the transmission of the last bit of each character; except in BOP mode when the CRC is to be sent as the next character (see Transmit Timing-End of Message).

TRANSMIT—END OF BOP MESSAGE

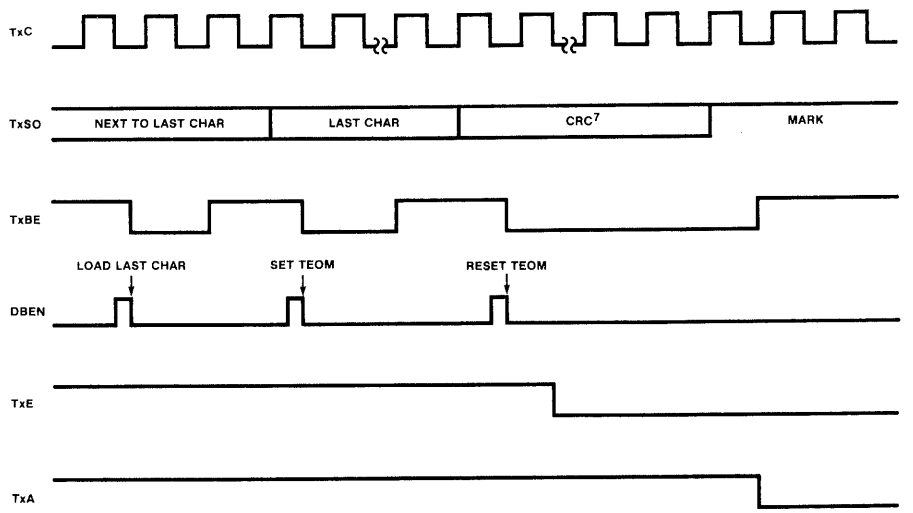


NOTES

4. TxBE goes low relative to the falling edge of DBEN corresponding to loading $TDSR_{H/L}$. It goes high one TxC before character transmission begins and also when TxA has been dropped.
5. TxE can be dropped before resetting TEOM if TxBE (corresponding to the closing FLAG) is high. Alternatively TxE can remain high and a new message initiated.
6. TxA goes low after TxE has been dropped and 1 1/2 TxC's after the last bit of the closing FLAG has been transmitted.

TIMING DIAGRAMS (Cont'd)

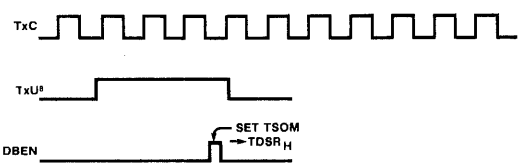
TRANSMIT TIMING—END OF BCP MESSAGE



NOTES

7. When 2652 generated CRC is not required, TEOM should only be set if SYNCs are to follow the message block. In that case, TxE should be dropped in response to TxBE (which corresponds to the start of transmission of the last character). When CRC is required, TxE must be dropped before CRC transmission is complete. Otherwise, the contents of TxDB will be shifted out on TxSO.

TRANSMIT UNDERRUN

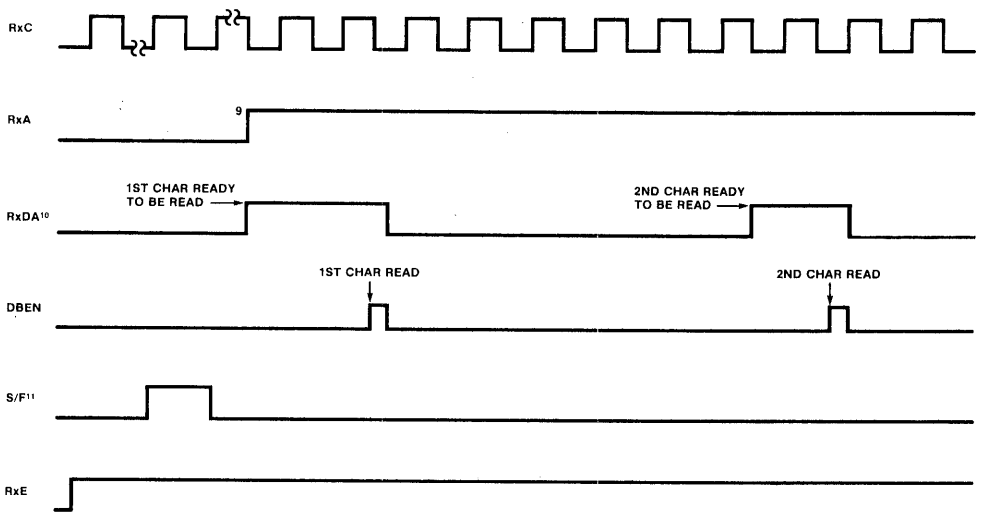


NOTES

8. TxU goes active relative to TxC falling edge if TxBE has not been serviced after n-1/2 TxC times (where n = transmit character length).

TIMING DIAGRAMS (Cont'd)

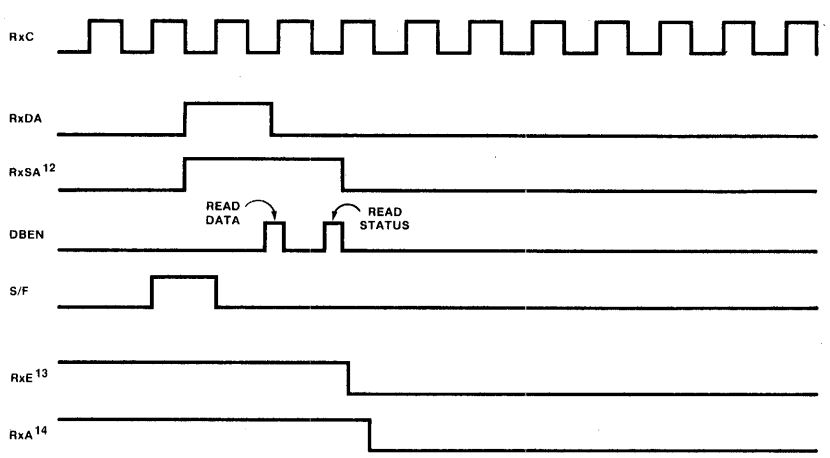
RECEIVE—START OF MESSAGE



NOTES

9. RxA goes high relative to falling edge of RxC when RxE is high and:
   a. A data character following two SYNC's is in RxDB (BCP mode)
   b. Character following FLAG is in RxDB (BOP primary station mode)
   c. Character following FLAG is in RxDB and character matches the secondary station address or All Parties Address (BOP secondary station mode).
10. RxDA goes high when a character in RxDB is ready to be read. It goes low on the falling edge of DBEN when RxDB is read.
11. S/F goes high relative to rising edge of RxC anytime a SYNC (BCP) or FLAG (BOP) is detected.

RECEIVE END OF MESSAGE

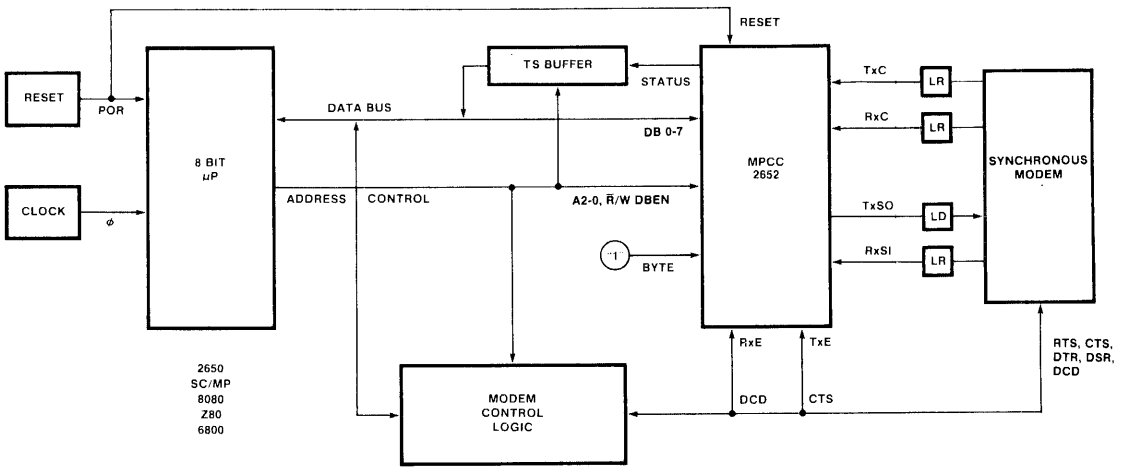


NOTES

12. At the end of a BOP message, RxSA goes high when FLAG detection (S/F = 1) forces REOM to be set. Processor should read the last data character ($RDSR_L$) and status ($RDSR_H$) which resets RxDA and RxSA respectively. For BCP end of message, RxSA may not be set. The processor should read the last data character and the status.
13. RxE must be dropped for BCP but may be left on at the end of a BOP message (see BOP Receive Operation).
14. RxA is reset relative to the falling edge of RxC after the closing FLAG of a BOP message; or when RxE is dropped.

TYPICAL APPLICATIONS

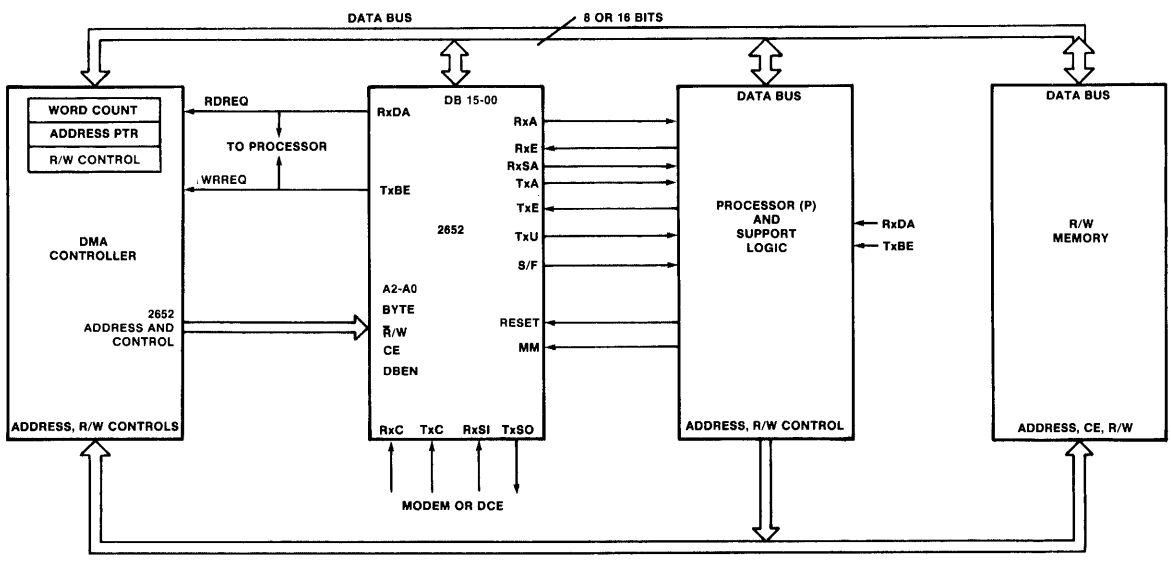
2652 MPCC/UP INTERFACE



NOTES

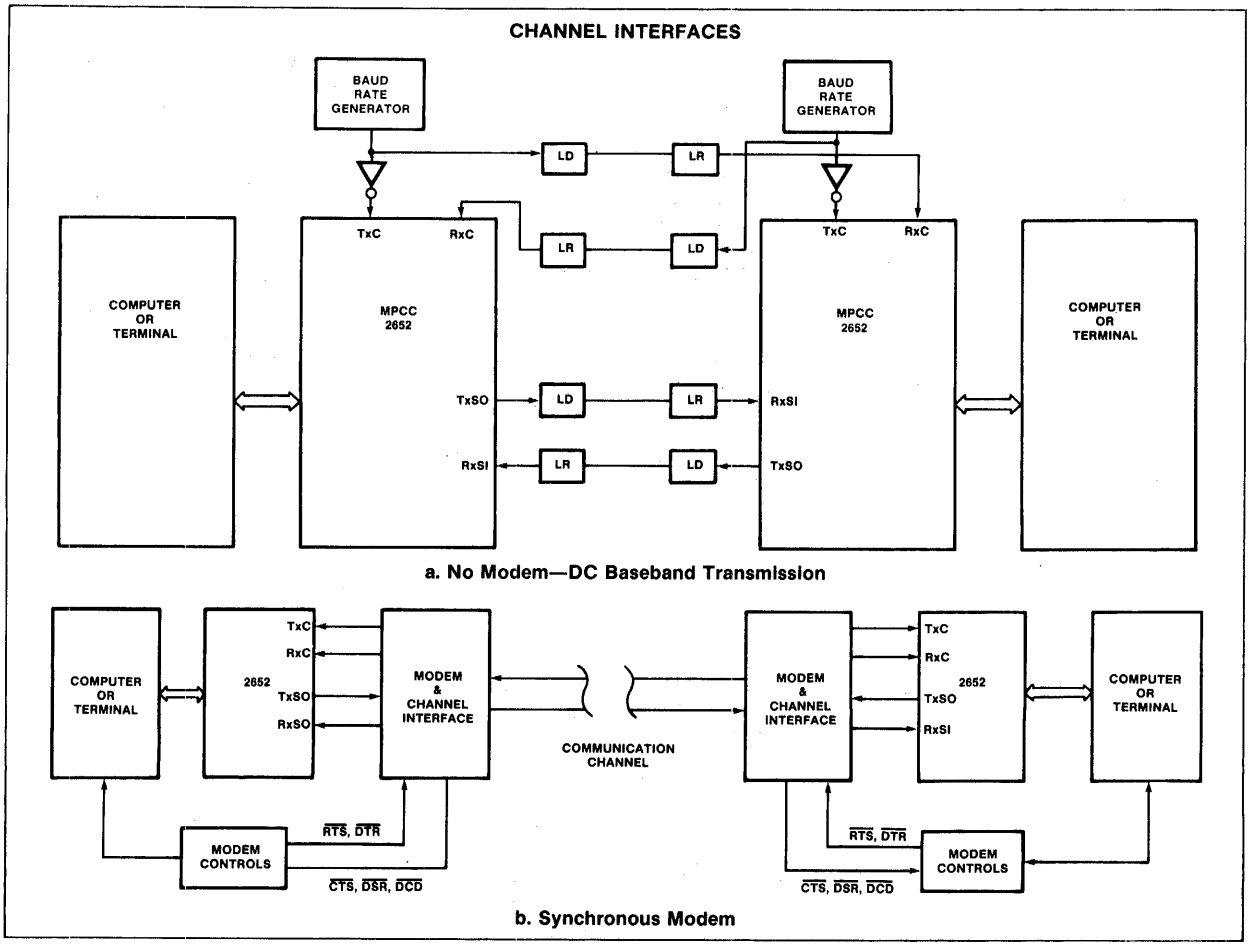
1. Possible μP interrupt requests are:
   RxDA, RxSA, TxBE, TxU.
2. Other 2652 status signals and possible uses are:
   S/F line: idle indicator, frame delimeter.
   RxA handshake on RxE, line turn around control
   TxA handshake on TxE, line turn around control.
3. Line Drivers/Receivers (LD/LR) convert EIA to TTL voltages and vice-versa
4. RTS should be dropped after the CRC (BCP) or FLAG (BOP) has been transmitted. This forces CTS low and TxE low.

DMA/PROCESSOR INTERFACE



For non-DMA operation, TxBE and RxDA are sent to the processor which then loads or reads data characters as required.

TYPICAL APPLICATIONS (Cont'd)



DESCRIPTION

The Signetics 2655 PPI is designed for 2650 microcomputer systems. It consists of three ports (24 I/O pins), which can be individually programmed to function as input, output or bidirectional ports. Interface with the 2650 is via an eight-bit bidirectional data bus.

The PPI may be programmed for five major modes of operation: static I/O, strobed I/O, bidirectional I/O, serial I/O, or serial/timer I/O. In the serial/timer mode, parallel to serial or serial to parallel conversion of data operates simultaneously with the timer on one of the three ports.

FEATURES

- **Five selectable major operating modes:**
  - **Static I/O**
  - **Strobed I/O**
  - **Bidirectional**
  - **Serial I/O**
  - **Serial/timer I/O**
- **Three ports (A, B, and C) with 24 programmable I/O pins**
- **Completely TTL compatible**
- **Three MHz programmable timer or event counter**
- **Fully compatible with the 2650 microprocessor**
- **Direct bit set/reset capability of each bit for all three ports**
- **300ns port read/write access time**
- **Operates in a polled or interrupt driven system environment**
- **Forty pin dual in-line package**
- **Single +5 volt supply**

OPERATION

The following is a functional description of the five operating modes of the PPI. Each mode is selected via a mode control word. Interrupt generation and interrupt enable/disable functions are available with each mode except the static mode which operates entirely under program control.

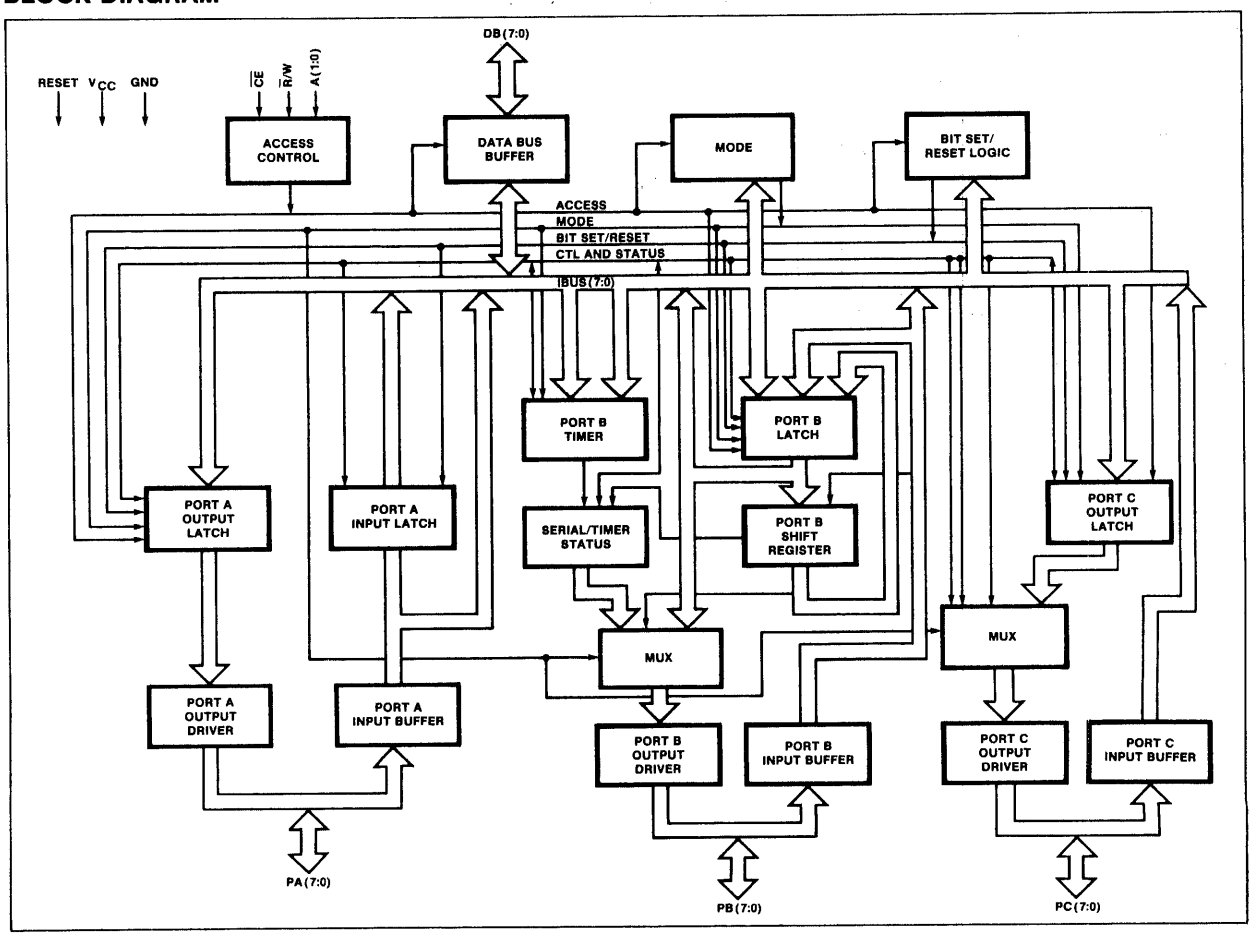
STATIC MODE

All three ports can operate in the static I/O mode. This mode allows each pin of each port to be either an input pin or an output pin. A logic "1" written to a pin of a selected port from the 2650 will condition that pin to be an input or output pin. Writing a logic "0" to the pin conditions that pin to be an output pin only. Outputs are latched while inputs are not. Each pin may be set or reset on an individual basis by a "set/reset" command.

STROBED I/O MODE

In this mode, data may be transferred to or from a specified port in conjunction with strobe or "handshaking" signals. Ports A and B can operate in the strobed I/O mode and port C bits are used as control and status bits. In this mode both inputs and outputs are latched, and each port can be either an input or output.

BLOCK DIAGRAM



BIDIRECTIONAL I/O MODE

This mode provides a means for communicating with a peripheral device over a single eight-bit bus with both transmitting and receiving capability. Port A operates in this mode with Port C pins providing "handshaking" signals for status and control. Both inputs and outputs are latched and port direction is determined by a control signal from the peripheral.

SERIAL I/O MODE

This mode provides a means for communicating with a peripheral device on a bit serial basis through Port B. Parallel data from the CPU will be shifted out to the peripheral over the least significant bit of Port B (PB0). Eight clocks will be required for a complete character transfer. The eight-bit character will be repeatedly shifted out until the CPU presents another character to Port B.

For the serial in mode, data is input from the peripheral at the most significant bit of Port B (PB7). Eight clocks will be required to assemble the eight-bit character. An interrupt request will signal the CPU for character transfer.

TIMER MODE

This mode enables the PPI to perform time interval measurements, pulse width measurements, and event counting. This timing function is performed during the serial/timer mode, and is restricted to Port B only. The mode is initiated by selecting the desired operation and loading a 16-bit down counter with an initial value. The counter does not start counting until the upper eight bits have been loaded. An interrupt can be generated to signal the CPU when the timer reaches a zero count.

PIN DESIGNATION

PIN NO.	MNEMONIC	TYPE	NAME AND FUNCTION
27-34	D7-D0	I/O	**Data Bus:** Eight-bit tri-state bidirectional data bus. All data and command transfers are made using this bus. D0 is the least-significant bit; D7 is the most-significant bit.
35	RESET	I	**Reset:** Resets all internal storage elements, including the data latches and command registers. Resets ports A, B and C to accept input data, and operating mode to Static mode. A functionally equivalent on chip power-on reset is also provided.
8,9	A1, A0	I	**Address:** Address lines used to select internal PPI modes or registers. Indicates control or data words to be placed on the data bus. Used in conjunction with the $\overline{R}$/W line.
5	$\overline{R}$/W	I	**Read/Write:** When low, gates the selected register to the data bus. When high, gates the contents of the data bus into the selected register.
6	$\overline{CE}$	I	**Chip Enable:** When low, identifies that control and data lines to the PPI are valid.
36	$\overline{SCLK}$	I	**Serial Clock:** Provides a serial clock for the parallel-to-serial or serial-to-parallel conversion.
37-40 1-4	I/O PA7-PA0	I/O	**Port A:** An eight-bit tri-state quasi-bidirectional port.* PA0 is the least-significant bit; PA7 is the most-significant bit.
25-18	I/O PB7-PB0	I/O	**Port B:** An eight-bit quasi-bidirectional port.* PB0 is the least-significant bit; PB7 is the most-significant bit. Port B also has parallel-to-serial, or serial-to-parallel conversion capability with PB0, 7 being either the serial output or input respectively. Data is double buffered. Port B can also operate as a 16-bit binary timer, as an event counter, or as a pulse width indicator. An output is generated whenever the counter is decremented to the all-zero state.
10-13 17-14	I/O PC7-PC0	I/O	**Port C:** An eight-bit quasi-bidirectional port.* PC0 is the least-significant bit; PC7 is the most significant bit. Port C bits are also used as control and status signals in conjunction with ports A and B. When a pin is used as a strobe input, the line receives an external strobe input which clocks information from port A or port B into the port A or port B data latches. When a pin is used as a status line, the line indicates port A or port B status condition which may be used as an interrupt input to the 2650.
26		I	**+5 Volt:** Power supply.
7		I	**Ground:** 0V reference.

*A quasi-bidirectional port allows each bit to be designated as input or output under program control. If any bit of the port is set to a '1,' that bit becomes an input or output depending on the usage of the port pin. If the peripheral is driving the port bit (i.e., overriding the logic "1" condition produced by the internal port pull up resistor), then the bit is an input. If the peripheral is receiving from the port bit, then a "0" or "1" written to the port will be transmitted to the peripheral.

DESCRIPTION

The Signetics 2656 System Memory Interface (SMI) is a mask programmable circuit with on-chip memory, I/O, and timing (clock) functions. It is useable either in 2-chip or multi-chip microcomputer systems. Used with the 2650 microprocessor, it provides a 2-chip microcomputer. This 2-chip microcomputer offers the user 2KX8 bits of ROM, 128X8 bits of RAM, and an 8-bit input-output port.

Used as a system interface in a multi-chip microcomputer, with larger memory and/or additional peripheral requirements, the programmable versatility of the SMI provides decoded chip enable outputs. These outputs connect directly to other memory or I/O functional blocks with few and often no requirement for additional interfacing chips. This reduces both chip count and cost in complex microcomputer systems.

The 2656 is processed using Signetics n-channel silicon gate technology. Only a single power supply of +5 volts is needed for operation.

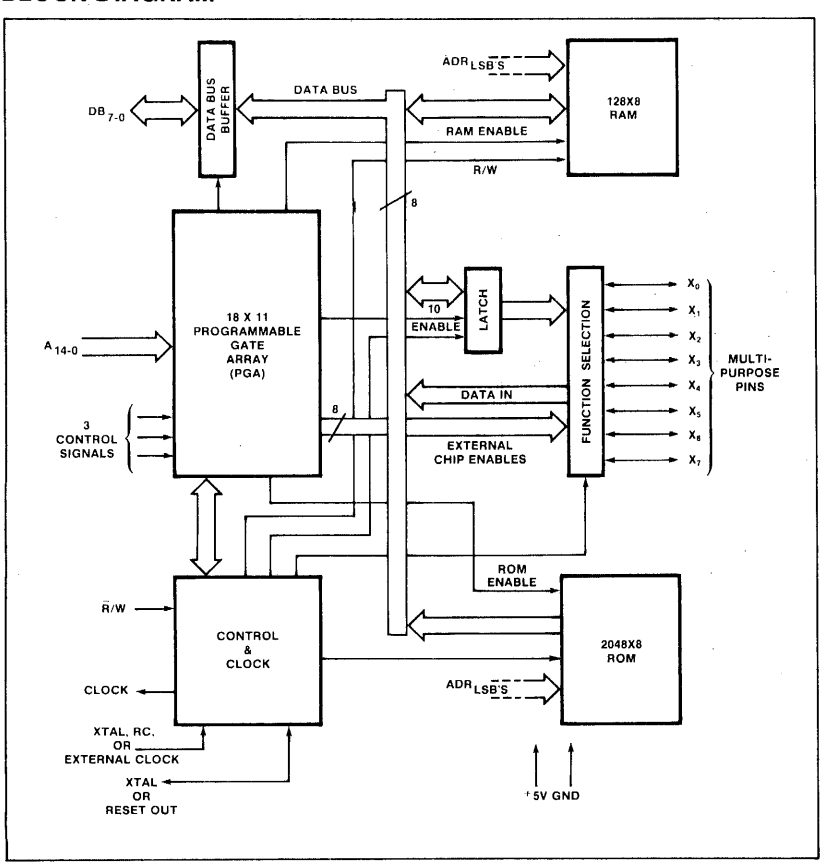
FEATURES

- **2KX8 mask programmable ROM**
- **128X8 static RAM**
- **8 multi-purpose pins for either chip enables or I/O bits**
- **8-bit latch for either I/O or MPU storage**
- **Internal clock generator with crystal, RC, or external timing source**
- **System power-on reset**
- **40-pin dual-in-line package**
- **Single +5 volt supply**

APPLICATIONS

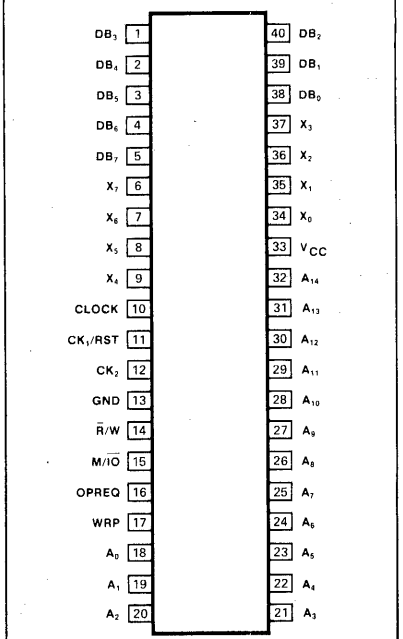
- **2-chip microcomputer**
- **System control for multi-chip microcomputers—eliminates or reduces TTL suppport circuitry for memory and I/O device selection.**
- **From small (2K-2 chip) to 32K microprocessor-based systems**

BLOCK DIAGRAM



PIN CONFIGURATION

IWA PACKAGE



FUNCTIONAL BLOCK DESCRIPTIONS

Data Bus Buffer

A tri-state bidirectional 8-bit bus transceiver for data transfer between the SMI and MPU.

Programmable Gate Array (PGA)

Provides select signal outputs for the internal ROM, RAM, Latch, and up to 8 multi-purpose I/O pins that are mask programmed as Chip Enables. A PGA output is active when the input variables match any one of 11 corresponding mask programmed product terms. The 18 input variables are normally address and control bus signals from the MPU and may be programmed as "1", "0", and "don't care." Each product term is a specified combination of the input variables.

Control and Clock

Generates the Clock output signal to the MPU and control signals for the ROM, RAM, and Latch. A mask programmable frequency divider provides input frequency division by 1, 2, 3, or 4. The timing source is mask programmable and may be a crystal, RC, or external oscillator. If either of the latter two are designated as a timing source, the second timing pin becomes a Reset output to the MPU.

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB_0-DB_7	38-40 1-5	I/O	**8-bit Bidirectional Data Bus:** All data transfers between the MPU and ROM, RAM, Latch, and X pins are made using this bus.
A_0-A_{14}	18-32	I	**MPU Address Bus:** Address bus inputs occupy contiguous bit positions with A_0 as the least significant address bit.
OPREQ	16	I	**Control Signal:** A signal that specifies the valid state of address and control bus.
M/$\overline{IO}$, WRP	15, 17	I	**Optional Signals:** Possibilities include Memory or I/O (M/$\overline{IO}$), Write Pulse (WRP), external control signals, or additional high order address bits.
$\overline{R}$/W	14	I	**Read/Write Control:** A control signal from the MPU that indicates whether the requested operation is to be a Read or Write (0 or 1 respectively). This signal must not change while OPREQ is true.
CLOCK	10	0	**Clock Output to the MPU:** The frequency is determined by the timing element and the mask programmable divisor (divided by 1, 2, 3, 4).
CK_1/RST, CK_2	11,12	I/O, I	**Connections for the Timing Element:** Only CK_2 is necessary for an RC or external timing source. The CK_1/RST pin then becomes a power-on Reset output. Two pins are necessary for direct connection of a crystal.
V_{CC}	33	I	**+5V:** Power supply.
GND	13	I	**Ground:** 0V reference ground.
X_0-X_7	34-37 9-6	I/O	**Multi-purpose I/O Pins:** These pins can be mask programmed as external memory or I/O chip enables, or bidirectional I/O port data bits, or any combination of the two.

ROM

2,048 bytes of mask-programmable Read Only Memory for storage of instructions and constants. The ROM base address is PGA mask programmable over the entire MPU address range. The ROM can be disabled by a mask option.

RAM

128 bytes of Read/Write Memory for MPU data storage and retrieval. The RAM base address is PGA mask programmable over the entire MPU address range. RAM dominates over ROM if address overlap is intentionally mask programmed. The RAM can be disabled by a mask option.

Function Select

A 1X8 Function Select array of mask-programmable contacts determine the function of each of the multi-purpose I/O pins (X_0-X_7). Two modes exist:

1. CE - The X pin is an active low Chip Enable ($\overline{CE}$) for either external memory or an I/O port. PGA inputs receive the external address and MPU control signals required to generate the $\overline{CE}$ output.
2. P - The X pin is a bidirectional I/O port data bit. A portion of the PGA provides the control signal to select the port.

Latch

Holds output data for the multi-purpose I/O pins mask programmed as a mode P. The latch continues to function as a read/write element even if all multi-purpose I/O pins are programmed as chip enables. Thus, any X pin that is programmed as an external chip enable can have corresponding latch bits available for temporary data storage or software flags. To read an input pin, the corresponding latch bit must first be written to a "one" by the MPU program. This is done to disable all active outputs, changing them to passive pullup outputs. This permits inputs to be sensed on the same pin. Subsequent reads of the same pin do not have to be preceeded by a write if the state of the latch pin remains a "one."

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES

1. Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operations section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 55° C/W junction to ambient (IWA ceramic package.)
3. This product includes circuitry specifically designed for this protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%[1,2,3,4,10]

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage					V
V_{IL}	Low		-.5		0.8	
V_{IH}	High		2.2			
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.45	
V_{OH}	High	I_{OH} = -100μA[6]	2.4			
V_{OHP}	I/O port output high voltage	I_{OHP} = -50μA[7]	2.4			V
I_{IL}	Input load current	V_{IN} = 0 to 5.5V			10	μA
I_{LD}	Data bus leakage current	V_{OUT} = 4.0V			10	μA
I_{CC}	Power supply current				150	mA
	Capacitance	T_A = 25°C, V_{CC} = 0V				
C_{IN}	Input	f_c = 1MHz		4	10	pF
C_{OUT}	Output	Unmeasured pins		4	10	pF
$C_{I/O}$	I/O	tied to ground		6	10	pF

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%.[1,2,3,4,9,10]

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_S	Address and control setup time		0			ns
t_H	Address and control hold time		0			ns
t_{PD1}	Propagation delay time - high to low[5]	C_L = 100pF	50		230	ns
t_{PD2}	Propagation delay time - low to high[5]	C_L = 100pF	50		230	ns
t_{WRP}	Write pulse width		200			ns
t_{DD}	Data bus delay time for read	C_L = 100pF	200		580	ns
t_{DF}	Data bus floating time for read	C_L = 100pF			580	ns
t_{DBS}	Data bus setup time for write		200			ns
t_{DBH}	Data bus hold time for write		200			ns
t_{OD}	Output delay time	C_L = 100pF	100		400	ns
f_C	Crystal or external clock frequency				4.0	MHz
t_C	External clock high or low state		110			ns
t_{RST}	Reset output pulse width[8]		30		300	μs
t_{AWS}	Address to write pulse setup time		50			ns

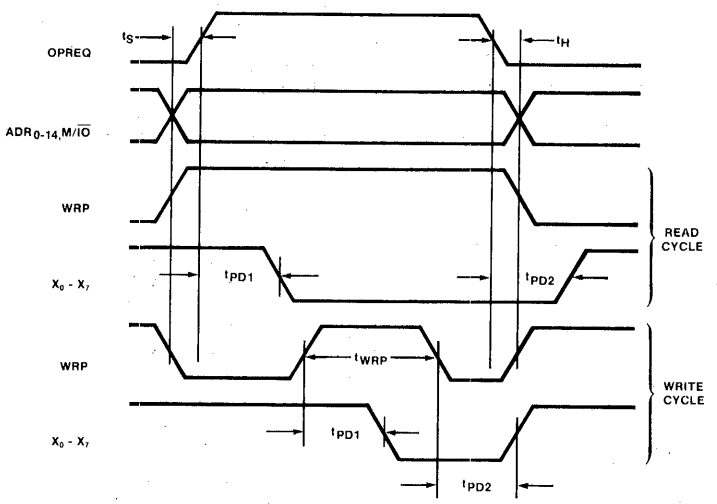
NOTES

1. Parameters are valid over operating temperature range unless otherwise specified.
2. All voltage measurements are referenced to ground. All time measurements are at the V_{OH}, V_{OL}, V_{IH}, V_{IL} levels as appropriate.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. AC characteristics assume the following input signals from a Signetics 2650 microprocessor:

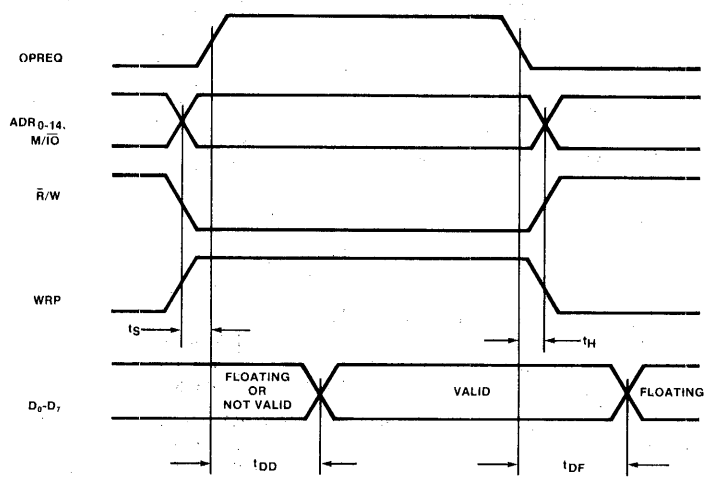
   Pins 18-32 = ADR_0-ADR_{14} Pin 15 = M/$\overline{IO}$
   Pin 16 = OPREQ Pin 17 = WRP
5. For X_0-X_7, time reference is OPREQ or time input changes, whichever is later.
6. Data Bus, Chip Enable, CK_1/RST or Clock outputs.
7. Port outputs only.
8. V_{CC} rise time must be less than 100 microseconds.
9. The delay times (Minima and Maxima) tend to track each other for any single device.
10. This is not a final specification. Parametric limits are subject to change.

TIMING DIAGRAMS

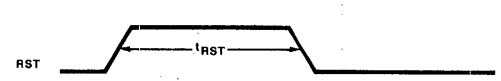
X_0-X_7 PINS USED AS CHIP ENABLES



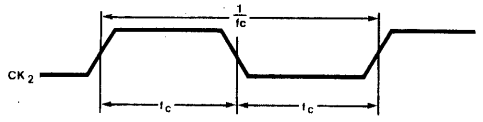
READ CYCLE (FOR ROM, RAM, LATCH, OR X_0-X_7 PINS USED AS INPUTS)



RESET OUTPUT

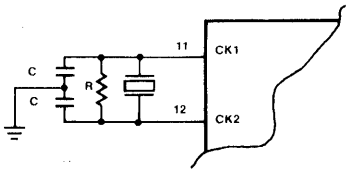


EXTERNAL CLOCK INPUT



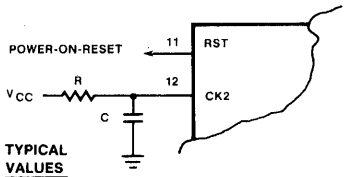
CLOCK CONFIGURATIONS

CRYSTAL CONNECTION



C = 15pF typical R = 1MΩ typical

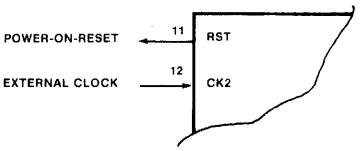
R-C CONNECTION



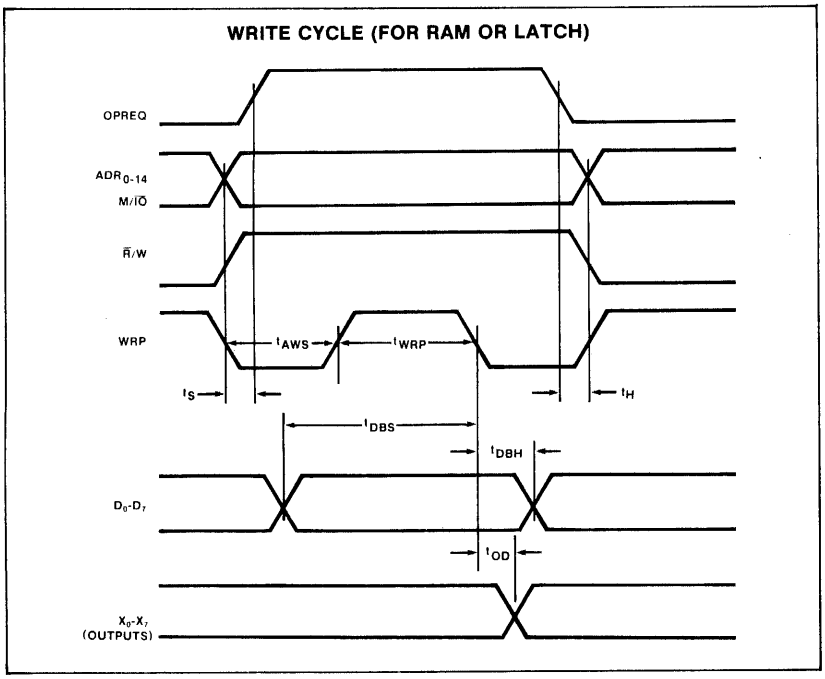
TYPICAL VALUES

f	R	C
2MHz	20K	20pF

EXTERNAL CLOCK CONNECTION



TIMING DIAGRAMS (Cont'd)



CUSTOM PATTERN PROGRAMMING INSTRUCTIONS

A computer-aided technique utilizing punched computer cards is employed to specify a custom version of the 2656. This technique requires that the customer supply Signetics with a deck of standard 80-column computer cards describing the data to be stored in the ROM array, the Programmable Gate Array (PGA), and the Function Select Array.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer-Aided Design (CAD) facility. The truth table will then be sent to the customer for final approval. On receipt of final approval, Signetics will produce masks and proceed with manufacturing.

The contents of each card in the deck are:

Customer Identification Cards are always labeled with a "C" in column 1. For customer identification any number of cards is permitted. A 4-card example is shown below. The following data should be included:

COLUMN	DATA
1	C
2	Blank
3-66	Company name (Card #1) Street address (Card #2) City, State, Zip (Card #3) Contact person name (Card #4)
67	Blank
68-70	SMI
71	Blank
72-75	2656
76-78	Blank
79-80	2-digit decimal number indicating the truth table number. Must be the same on all cards in the deck.

(Explanatory Note: The next card for this example is card No. 5)

CARD #5—SMI FUNCTIONAL PARAMETERS

COLUMN	DATA
1-9	Blank

The next eight columns specify whether multi-purpose pins (X_0-X_7) are to be chip enables or I/O port data bits. Each column must contain either the character "E" for chip enable or the character "P" for I/O port. Card column 10 specifies X_0, card column 17 specifies X_7.

COLUMN	DATA
10	E or P for X_0
11	E or P for X_1
12	E or P for X_2
13	E or P for X_3
14	E or P for X_4
15	E or P for X_5
16	E or P for X_6
17	E or P for X_7
18-19	Blank

Select one of the next three columns to specify the type of clock source; crystal, external or R/C network. An "X" designates the selected clock source. The other two columns must be blank.

COLUMN	DATA
20	X or blank (Crystal)
21	X or blank (R/C Network)
22	X or blank (External)
23-29	Blank

Select one of the next four columns to specify the clock source divider value to divide by 1, 2, 3 or 4. An "X" designates the selected divisor. The other three columns must be blank.

COLUMN	DATA
30	X or blank (÷ 1)
31	X or blank (÷ 2)
32	X or blank (÷ 3)
33	X or blank (÷ 4)
34-39	Blank

Access to ROM, RAM or I/O Port bits may be disabled. The next three columns are used to disable ROM, RAM or I/O Port. Specify an "X" (disable) or blank (do not disable).

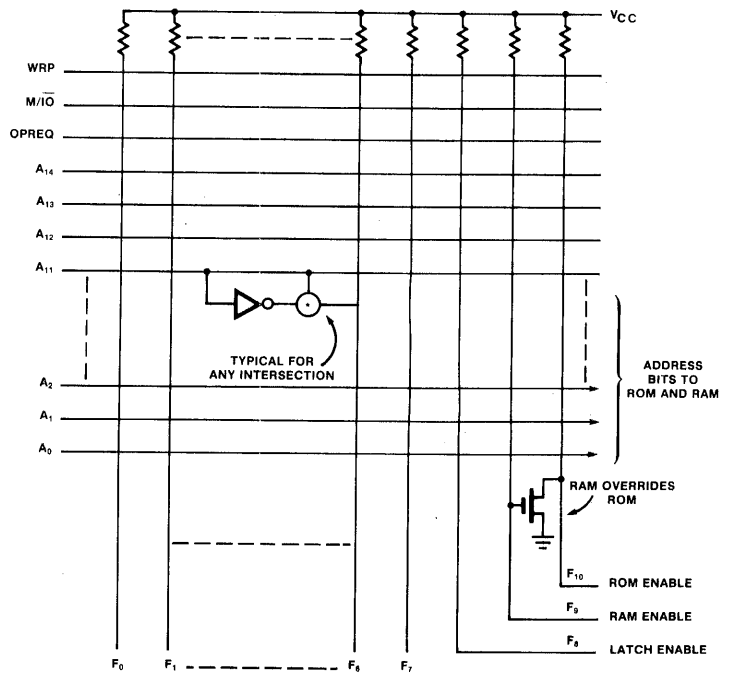
COLUMN	DATA
40	X or blank (ROM)
41	X or blank (RAM)
42	X or blank (PORT)
43-78	Blank
79-80	Two-digit decimal number indicating the truth table number.

CARD #6—PGA SPECIFICATION

The PGA is an 18 X 11 input-output structure. The first eight outputs are available as chip enables (if selected by the appropriate function—select parameters on card #5). The last three outputs are internally connected to enable the SMI internal I/O Port, RAM and ROM. (See Figure 1.) Ascending order of card columns correspond to ascending PGA outputs. Thus, columns 5 through 15 correspond, respectively, to PGA chip enable outputs 0 through 7, the latch enable, the RAM enable and the ROM enable. Valid characters are 1, 0 or X. "1" indicates active high, "0" indicates active low, and "X" indicates don't care.

COLUMN	DATA
1	A
2	0
3-4	Blank
5-15	1, 0 or X (A_0 for F_0 to F_{10})
16	Blank
17-27	1, 0 or X (A_1 for F_0 to F_{10})
28	Blank
29-39	1, 0 or X (A_2 for F_0 to F_{10})
40	Blank
41-51	1, 0 or X (A_3 for F_0 to F_{10})
52	Blank
53-63	1, 0 or X (A_4 for F_0 to F_{10})
64	Blank
65-75	1, 0 or X (A_5 for F_0 to F_{10})
76-78	Blank
79-80	2-digit decimal number indicating the truth table number.

PROGRAMMABLE GATE ARRAY (PGA)



NOTE

Each intersection can be programmed as active low (0), active high (1), or "don't care"(X).

Figure 1

CARD #7—PGA SPECIFICATION (Cont'd)

COLUMN	DATA
1	A
2	6
3-4	Blank
5-15	1, 0 or X (A_6 for F_0 to F_{10})
16	Blank
17-27	1, 0 or X (A_7 for F_0 to F_{10})
28	Blank
29-39	1, 0 or X (A_8 for F_0 to F_{10})
40	Blank
41-51	1, 0 or X (A_9 for F_0 to F_{10})
52	Blank
53-63	1, 0 or X (A_{10} for F_0 to F_{10})
64	Blank
65-75	1, 0 or X (A_{11} for F_0 to F_{10})
76-78	Blank
79-80	2-digit decimal number indicating the truth table number.

CARD #8—PGA SPECIFICATION (Cont'd)

COLUMN	DATA
1	A
2-3	12
4	Blank
5-15	1, 0 or X (A_{12} for F_0 to F_{10})
16	Blank
17-27	1, 0 or X (A_{13} for F_0 to F_{10})
28	Blank
29-39	1, 0 or X (A_{14} for F_0 to F_{10})
40	Blank
41-51	1, 0 or X ($M/\overline{IO}$ for F_0 to F_{10})
52	Blank
53-63	1,0 or X (OPREQ for F_0 to F_{10})
64	Blank
65-75	1, 0 or X (WRP for F_0 to F_{10})
76-78	Blank
79-80	2-digit decimal number indicating the truth table number.

BINARY ROM CODE FORMAT

CARD #9 THROUGH CARD #264

These remaining cards specify the 2048 8-bit locations of the SMI ROM. The first data field of card #9 is ROM location 0, the last data field of card #264 is ROM location 2047. For each field, the leftmost character is the MSB, the rightmost character is the LSB. Valid characters are 1 or 0. Alternately, P or N characters may be used. A "1" or "P" represents a logic high at the SMI data bus connection. A "0" or "N" represent a logic low. Each of these cards is configured as follows:

COLUMN	DATA
1-5	Right justified decimal address of first data field of the card (columns 7-14).
6	Blank
7-14	1 or 0; or, P or N

COLUMN	DATA
15	Blank
16-23	1 or 0; or, P or N
24	Blank
25-32	1 or 0; or, P or N
33	Blank
34-41	1 or 0; or, P or N
42	Blank
43-50	1 or 0; or, P or N
51	Blank
52-59	1 or 0; or, P or N
60	Blank
61-68	1 or 0; or, P or N
69	Blank
70-77	1 or 0; or, P or N
78	Blank
79-80	2-digit decimal number indicating the truth table number.

HEXADECIMAL ROM CODE FORMAT

CARD #9 THROUGH CARD #72

The customer may also submit ROM code in hexadecimal format. 32 locations (bytes) are specified on each card. Columns 7 and 8 of card #9 contain the data for ROM location 0 while columns 69 and 70 of card #72 contain the data for ROM location H'7EF'. In each data pair, the left character is the hexadecimal equivalent of bits D_7 to D_4; the right character is the hexadecimal equivalent of bits D_3 to D_0. Table 1 shows the conversion from binary to hexidecimal.

Each of these cards is configured as follows:

COLUMN	DATA
1-4	Right justified hexadecimal address of first data pair of the card (columns 7-8). For example, card #9 will contain '0000,' card #10 will contain '0020' and so forth until card #72, which contains '07E0.'
5-6	Blank
7-8	First data pair
9-10	Next data pair
11-12	Next data pair
11-12	Next data pair
11-12	Next data pair
11-12	Next data pair
67-68	Next to last data pair
69-70	Last data pair of card
71-78	Blank
79-80	2-digit decimal number indicating the truth table number.

BINARY COMBINATION D_7-D_4 OR D_3-D_0				HEXADECIMAL CHARACTER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

Table 1 BINARY TO HEXADECIMAL CONVERSION

APPLICATION EXAMPLES

A TWO CHIP MICROCOMPUTER

The minimum system depicted in Figure 2 is composed of the 2650 MPU, a 2656 SMI, and a resistor/capacitor network for a timing input. The SMI provides MPU CLOCK and RESET signals and eight I/O Port bits (X_0-X_7).

Note that because all eight I/O bits share the same device address, the MPU program must "housekeep" unwanted bits when reading or writing to any of them. If a one-bit write operation is desired, the MPU must preserve the state of all other output pins. This can be done by reading the latch, changing the state of the selected bit, and outputing the result.

Any latch bit used for input must first be written to a Logic "1" before a read operation. After reading the data, the bits not desired must be masked out by the program.

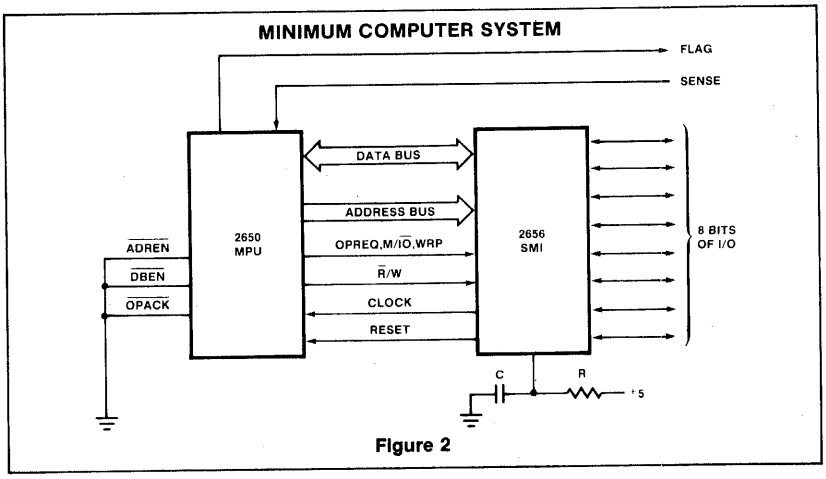


Figure 2

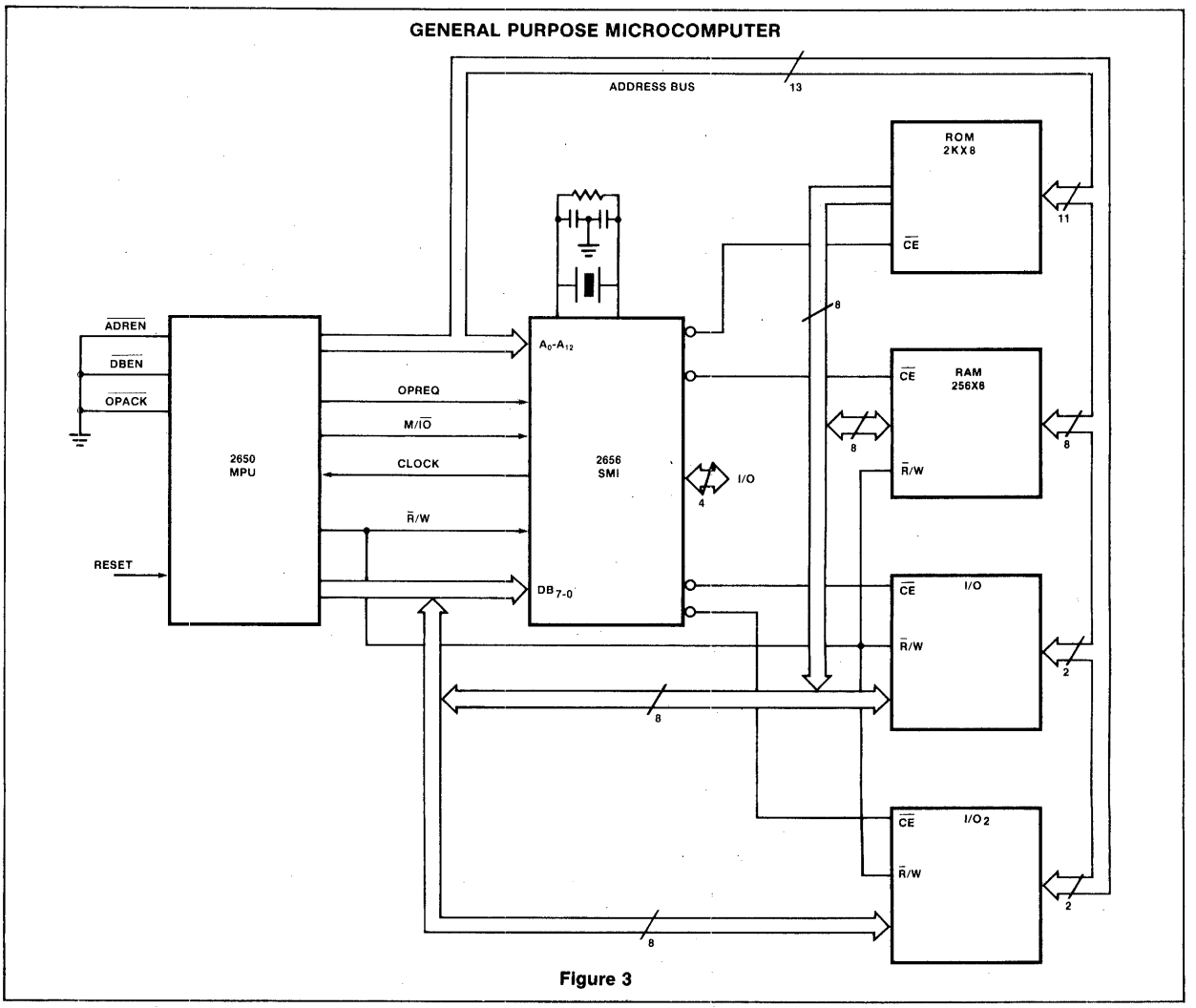


Figure 3

A GENERAL PURPOSE MICROCOMPUTER

A general purpose microcomputer is illustrated in Figure 3. The SMI provides ROM RAM and the MPU clock from a crystal source. It also provides chip enables for external ROM, RAM and LSI peripheral controllers 1 and 2 as well as four bidirectional data bits.

The state of M/$\overline{IO}$ in the Address Map (Table 6) indicates that I/O_1 and I/O_2 are memory mapped while the SMI port is referenced using any I/O instruction (extended or non-extended) on the 2650. See the SMI Program Table (Table 7).

The 2650 addresses the SMI port to input or output data on X_4-X_7. SMI latch bits 0-3 are available for MPU temporary storage since the corresponding X pins are used for external chip enables.

Note that the 13 MPU address bits are assigned to the first 13 PGA inputs (A_0-A_{12}) and that only two MPU control signals (OPREQ, M/$\overline{IO}$) are input to the PGA (WRP is not required).

The SMI uses the $\overline{R}$/W signal from the 2650 to read or write from the internal RAM and port. External devices are enabled when their address (A_0-A_{12}, M/$\overline{IO}$) have been decoded by the SMI and OPREQ is valid.

	PIN	# BYTES	ADDRESS	M/$\overline{IO}$
Internal ROM	—	2K	0000-07FF	1
External ROM	X_0	2K	0800-0FFF	1
*Spare ROM	—	1K	1000-13FF	1
External RAM	X_1	256	1400-14FF	1
Internal RAM	—	128	1500-157F	1
*Spare RAM	—	512	1600-17FF	1
I/O_1	X_2	4	1800-1803	1
I/O_2	X_3	4	1804-1807	1
SMI Port	—	—	ANY	0

*Space left for possible system expansion.

Table 6
ADDRESS MAP FOR GENERAL PURPOSE MICROCOMPUTER

	PRODUCT TERM																		
NO.	WRP	A14	A13	M/$\overline{IO}$	OPREQ	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	FS*
0	X	X	X	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	E X_0
1	X	X	X	1	1	1	0	1	0	0	X	X	X	X	X	X	X	X	E X_1
2	X	X	X	1	1	1	1	0	0	0	0	0	0	0	0	0	X	X	E X_2
3	X	X	X	1	1	1	1	0	0	0	0	0	0	0	0	1	X	X	E X_3
4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_4
5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_5
6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_6
7	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_7
8	X	X	X	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	PORT
9	X	X	X	1	1	1	0	1	0	1	0	X	X	X	X	X	X	X	RAM
10	X	X	X	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	ROM

DISABLE			PGA	XTL	R/C	EXT	1	2	3	4
			TIMING SOURCE	√				√		
ROM	RAM	PORT					CK Divide by			

*P = Port E = Enable

Table 7 SMI PROGRAM TABLE FOR GENERAL PURPOSE MICROCOMPUTER

HIGH PERFORMANCE MICROCOMPUTER SYSTEM

The six-chip high performance system of Figure 4 contains a 2655 Programmable Peripheral Interface and a 2651 Programmable Communication Interface. Two SMIs are used in the system. The first SMI provides CLOCK and RESET signals to the 2650, initial increments of ROM and RAM, and eight bits of bidirectional I/O to the user's external interface. The second SMI provides a crystal controlled clock for the PCI, additional amounts of ROM and RAM, read (RDS) and write (WRS) strobes for the first SMI's eight-bit port, chip enables for PPI and PCI, and four bits of bidirectional I/O data.

The PPI and PCI addresses are decoded by SMI #2 to generate the chip selects on X_7 and X_6. The two least significant MPU address bits specify one of three PPI eight bit I/O ports or one of four PCI internal registers. Three PCI interrupt conditions are WIRE-ORed (active low) to the 2650 interrupt request input (INTREQ). The interrupt acknowledge (INTACK) is inverted and used to enable the interrupt vector onto the data bus through the 74LS240 tri-state buffer.

	PRODUCT TERM																		
NO.	M/$\overline{IO}$	A_{14}	A_{13}	WRP	OPREQ	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	FS*
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_0
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_1
2	X	X	X	1	1	1	1	0	1	0	0	0	0	0	1	X	X	X	E X_2
3	X	X	X	1	1	1	1	0	1	0	0	0	0	0	0	0	1	1	E X_3
4	X	X	X	1	1	1	1	0	1	0	0	0	0	0	0	0	1	0	E X_4
5	X	X	X	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	E X_5
6	X	X	X	X	1	1	0	1	0	0	X	X	X	X	X	X	X	X	E X_6
7	X	X	X	X	1	0	1	0	X	X	X	X	X	X	X	X	X	X	E X_7
8	X	X	X	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	PORT
9	X	X	X	1	1	1	0	1	0	1	0	X	X	X	X	X	X	X	RAM
10	X	X	X	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	ROM

DISABLE			PGA	XTL	R/C	EXT	1	2	3	4
			TIMING SOURCE			√		√		
ROM	RAM	PORT					CK Divide by			

*P = Port E = Enable

Table 8 SMI PROGRAM TABLE FOR HIGH PERFORMANCE MICROCOMPUTER SYSTEM

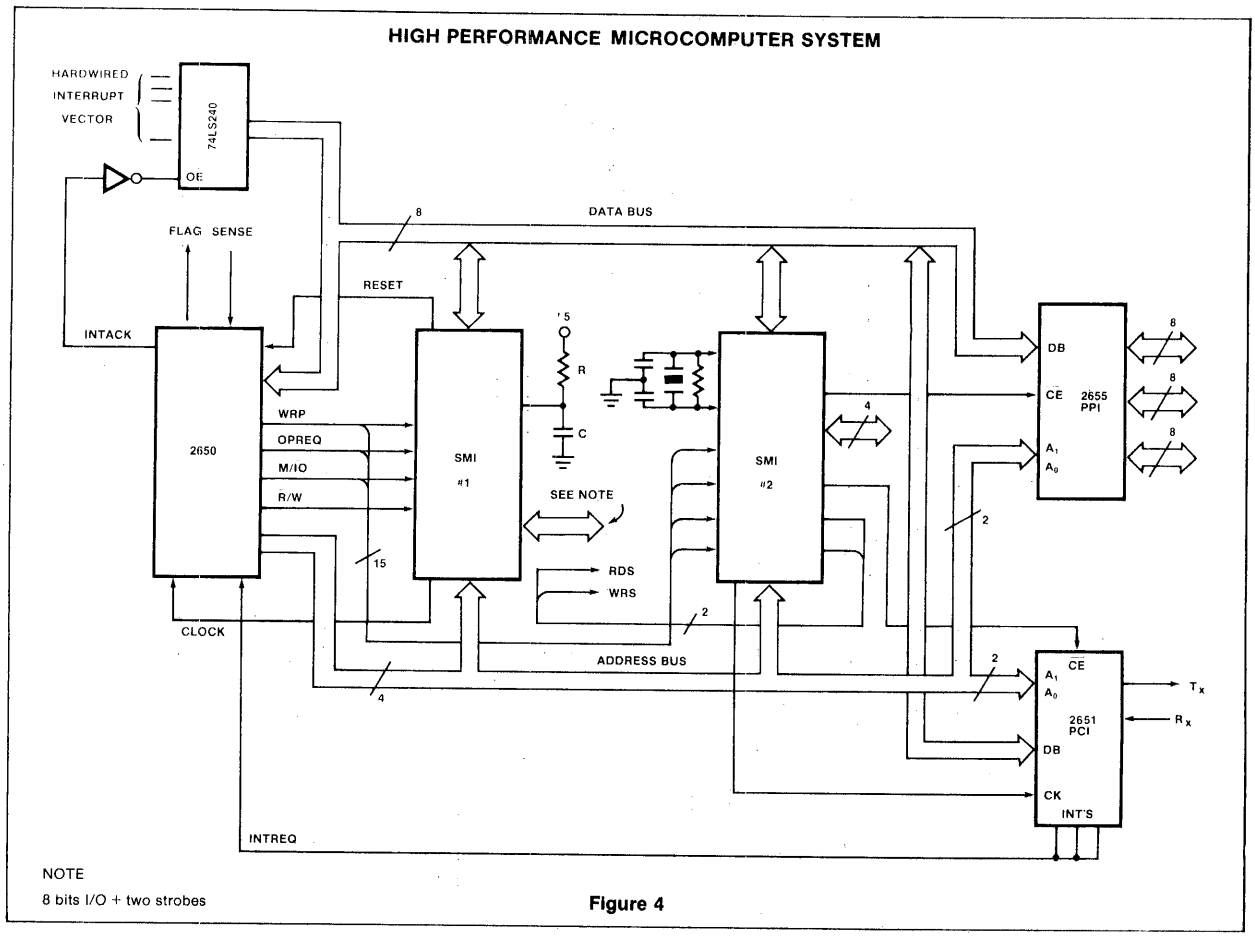


Figure 4

MICROCOMPUTER SYSTEM WITH MSI INPUT-OUTPUT

The system of Figure 5 incorporates MSI integrated circuits for input and output. It contains a total of 3k bytes of ROM/PROM, 384 bytes of RAM, six bits of SMI latch storage, one latching input port (74LS374), one gated input port (74LS240), one byte-oriented output port (74LS374), one bit-oriented output port (74LS259/93L34), two single bit inputs and two single bit outputs (one each from the SMI and the 2650). The SMI divides the external clock frequency by 1, 2, 3, or 4 and provides CLOCK and RESET outputs to the 2650. Six X pins are used for chip enables and two for data bits.

Included are system memory map (Table 9) and the SMI Program Table. The I/O device and the SMI port are all memory mapped; thus, the 2650 M/$\overline{IO}$ signal is not connected to the SMI.

WRP from the 2650 is connected to the SMI to control the two output ports:

1. When output-port-1's address and OPREQ are valid, the WRP input provides a gated chip enable on X_3. The trailing edge of this signal is used to clock 2650 data into the 74LS374.
2. One bit of 2650 data is gated into the 74LS259/93L34 addressable latch (output port 2) by means of X_2 which serves as the enable input. This signal is active when output port 2 has been selected. At the same time, three address bus lines select the latch to be written into.

	PIN	BYTES	ADDRESS
Internal ROM	—	2k	0000-07FF
External PROM (82S181)	X_7	1k	0800-0BFF
External RAM (2-2112's)	X_6	256	1400-14FF
Internal RAM	—	128	1500-157F
SMI Port	—	1	1A00
Input Port 1 (74LS374)	X_5	1	1A01
Input Port 2 (74LS240)	X_4	1	1A02
Output Port 1 (74LS374)	X_3	1	1A03
Output Port 2 (74LS259/93L34)	X_2	8	1A08 - 1A0F

Table 9 ADDRESS MAP FOR MSI I/O SYSTEM

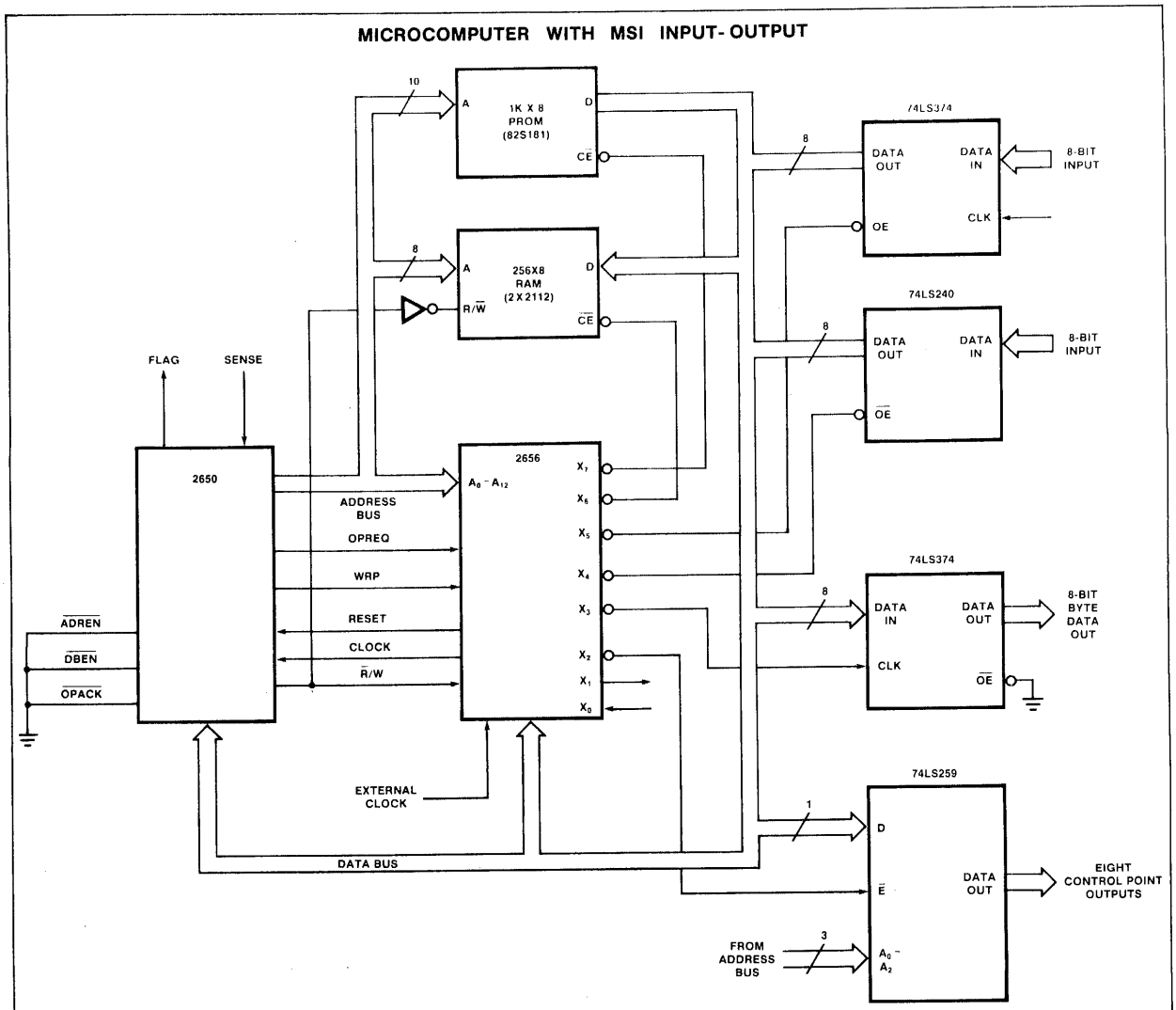

MICROCOMPUTER WITH MSI INPUT-OUTPUT
1K X 8 PROM (82S181)
256X8 RAM (2X2112)
2650
2656
74LS374
74LS240
74LS374
74LS259
DATA OUT
DATA IN
8-BIT INPUT
CLK
OE
8-BIT BYTE DATA OUT
EIGHT CONTROL POINT OUTPUTS
FROM ADDRESS BUS
FLAG
SENSE
ADDRESS BUS
OPREQ
WRP
RESET
CLOCK
R/W
ADREN
DBEN
OPACK
EXTERNAL CLOCK
DATA BUS

Figure 5

DESCRIPTION

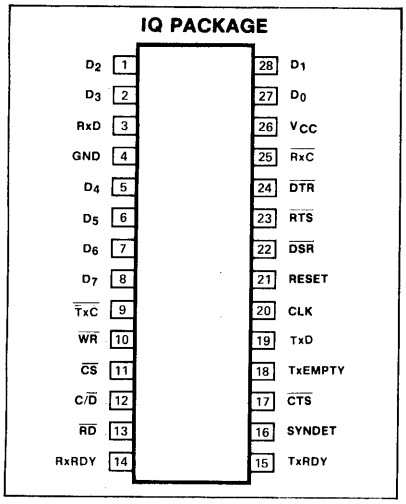
The MP8251 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in the MP8080A microcomputer family. The functional configuration of the MP8251 is programmed by the system software for maximum flexibility, thereby allowing the system to receive and transmit virtually any serial data communication signal presently in use (including IBM Bisync).

The MP8251 can be programmed to receive and transmit either synchronous or asynchronous serial data. The MP8251 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the MP8251 at any time during the functional operation. Status information reported includes the type and the condition of the transfer operations being performed by the MP8251, as well as any transmission error conditions (parity, overrun, or framing).

FEATURES

- **Synchronous and asynchronous full duplex operations**
- **Synchronous Mode Capabilities**
  - **Selectable 5- to 8-Bit characters**
  - **Internal or external character synchronization**
  - **Automatic sync insertion**
- **Asynchronous mode capabilities**
  - **Selectable 5- to 8-Bit characters**
  - **3 selectable clock rates (1x, 16x or 64x the baud rate)**
  - **Line break detection and generation**
  - **1-, 11/2-, or 2-Stop bit detection and generation**
  - **False start bit detection**
- **Baud rates**
  - **DC to 56k baud (synchronous mode)**
  - **DC to 9.6k baud (asynchronous mode)**
- **Transmission error detection capabilities**
  - **Parity**
  - **Overrun**
  - **Framing**

PIN CONFIGURATION



- **Double buffering of data**
- **TTL compatible**
- **Single TTL clock**
- **Reduces system component count**

PIN DESIGNATION

MNEMONIC	TYPE	NAME AND FUNCTION
$\overline{CS}$	I	**Chip select:** When low (logic 0), the chip is selected. This enables communication between the MP8251 and the MP8080A microprocessor.
$\overline{RD}$	I	**Read:** When low, allows the MP8080A to read data or status information from the MP8251.
$\overline{WR}$	I	**Write:** When low, allows the MP8080A to write data or control words into the MP8251.
C/$\overline{D}$	I	**Control/data:** Used in conjunction with an active RD or WR input (logic 0) to determine overall device operation as indicated below.
RESET	I	**Reset:** When high (logic 1), places the MP8251 in the idle mode. The device remains in this mode until a new set of control words is written into the MP8251 to program its functional definition. Minimum Reset pulse width is 6 t_{CY}.
CLK	I	**Clock:** TTL clock that is used to generate internal timing signals for the MP8251. The minimum frequency of the CLK input is 30 times the receiver/transmitter clock frequency for the synchronous mode, and 4.5 times the receiver/transmitter clock frequency for the asynchronous mode. The CLK input is normally connected to the ϕ_2 (TTL) output of the 8224 Clock Generator and Driver device.
$\overline{DSR}$	I	**Data set ready:** General purpose input whose condition can be tested by the MP8080A using a status read operation. However, a low level DSR input is normally used to test data set ready conditions.
$\overline{CTS}$	I	**Clear to send:** If low when the TxEn bit (D_0) of the command Instruction Control Word (see figure) is set high, enables the MP8251 to transmit serial data.

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	OPERATION
0	0	0	1	Data character read from MP8251
0	0	1	0	Data character written into MP8251
0	1	0	1	Status information read from MP8251
0	1	1	0	Control word written into MP8251
1	x	x	x	Device not selected

PIN DESIGNATION (Cont'd)

MNEMONIC	TYPE	NAME AND FUNCTION
$\overline{TxC}$	I	**Transmitter Clock:** This clock input controls the rate at which a data character is to be transmitted. The frequency of the TxC input is equal to the baud rate for the synchronous mode, and is a multiple (1x, 16x or 64x) of the baud rate for the asynchronous mode. A portion of the Mode Instruction Word (see figure) selects the value of the baud rate factor when in the asynchronous mode. Transmitter data are clocked out of the MP8251 on the falling edge of the TxC input.
RxD	I	**Receiver data:** Serial data input from a MODEM or an input/output device.
$\overline{RxC}$	I	**Receiver clock:** This clock input controls the rate at which a data character is to be received. The frequency and selection of the RxC input is as described above for the TxC input. Receiver data are clocked into the MP8251 on the rising edge of the RxC input.
V_{CC}		+5V power supply.
GND		**Ground:** 0-V reference.
$\overline{DTR}$	O	**Data terminal ready** General purpose output which can be set to an active low by programming the DTR bit (D_1) of the Command Instruction Control Word. However, a low level DTR output is normally used for data terminal ready or rate select control.
$\overline{RTS}$	O	**Request to send:** General purpose output which can be set to an active low by programming the RTS bit (D_5) of the Command Instruction Control Word. However, the RTS output is normally used for request to send control in the transmit mode.
TxD	O	**Transmitter data:** Composite serial data output to a MODEM or input/output device. The TxD output is held in the marking state (logic 1) upon a Reset operation.
TxRDY	O	**Transmitter ready:** When high, alerts the MP8080A that the transmitter is ready to accept a data character. The TxRDY output, which is automatically reset whenever a character is written into the MP8251, can be used as an interrupt to the system. For polled operation, the condition of the TxRDY signal can be tested by the MP8080A using a status read operation.
TxE	O	**Transmitter empty:** Goes high to indicate the end of a transmit mode. The TxE output is automatically reset whenever a character is written into the MP8251. In the synchronous mode, a high-level TxE output indicates that a character has not been loaded, the transmitter buffer is empty, and the sync character(s) of a data block are soon to be transmitted automatically as fillers.
RxRDY	O	**Receiver ready:** When high, alert the MP8080A that the receiver contains a data character that is ready to be input to the CPU. The RxRDY output, which is automatically reset whenever a character is read from the MP8251, can be used as an interrupt to the system. For polled operation, the condition of the RxRDY signal can be tested by the MP8080A using a status read operation.
D_7-D_0	I/O	**Data bus:** This bus comprises eight Tri-state input/output lines. The bus provides bidirectional communications between the MP8251 and the MP8080A. Data are routed to or from the internal data bus buffer upon execution of an MP8080A OUT or IN instruction, respectively. In addition, control words, command words and status information are transferred through the data bus buffer.
SYNDET	I/O	**Sync detect:** This pin may be used in the synchronous mode only. System software can program SYNDET as either an input or an output. When used as an output (Internal sync detect mode), a high level SYNDET output is automatically reset upon a status read operation by the MP8080A. When used as an input (external sync detect mode) a high level SYNDET causes the MP8251 to start assembling data characters on the falling edge of the next RxC input.

ABSOLUTE MAXIMUM RATINGS*

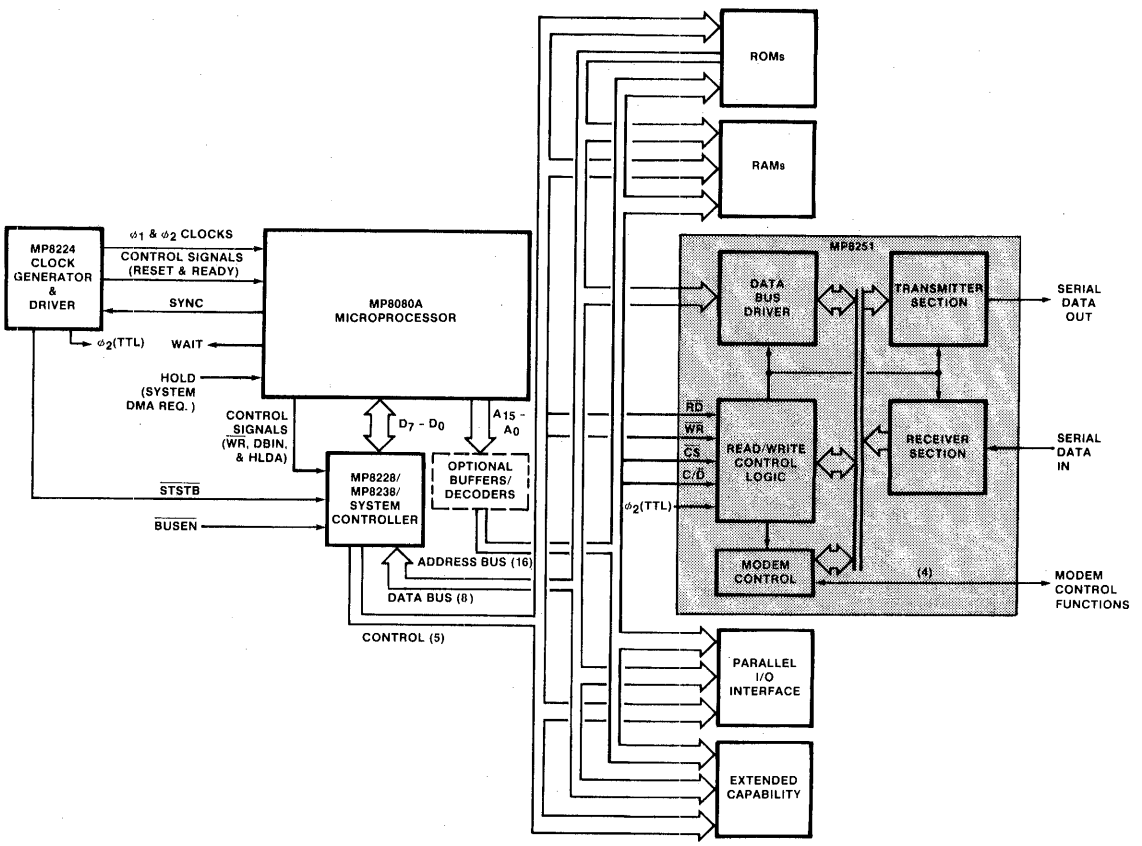
PARAMETER		RATING	UNIT
T_A	Ambient temperature under bias	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
	Voltage on any pin with respect to ground	-0.5 to +7	V
P_D	Power dissipation	1	W

*NOTE

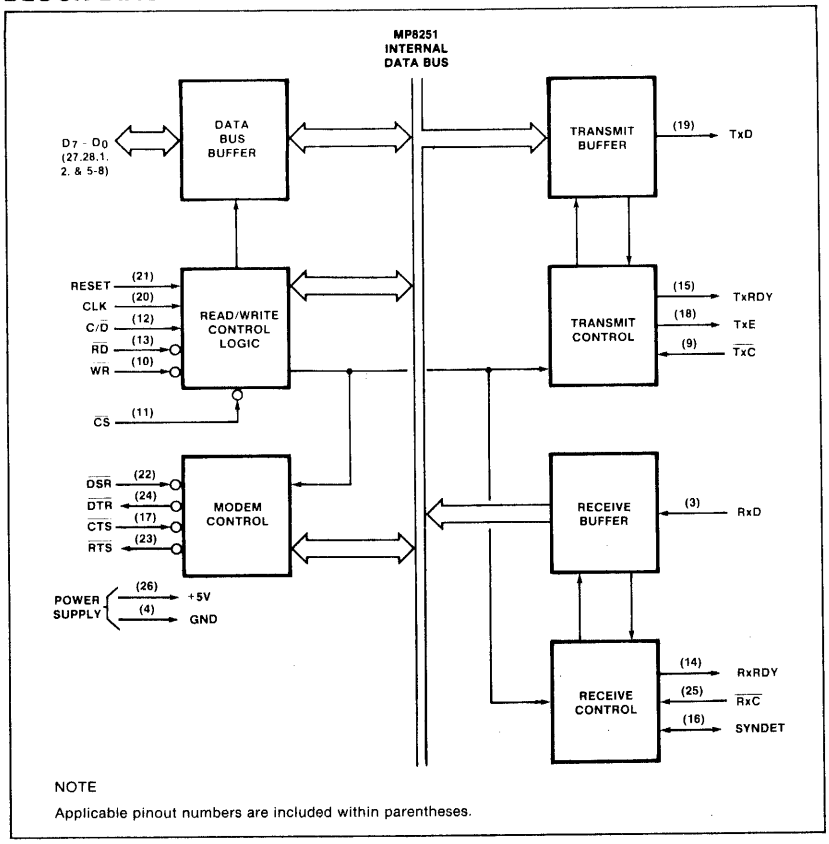
Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

BLOCK DIAGRAMS

MP8080A MICROCOMPUTER FAMILY BLOCK DIAGRAM



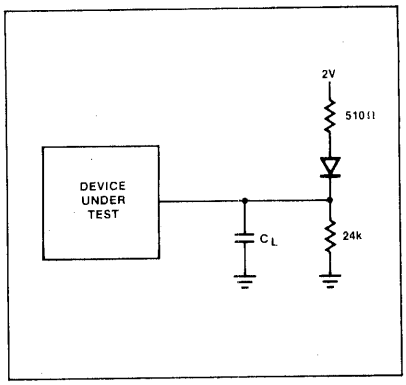
BLOCK DIAGRAMS (Cont'd)

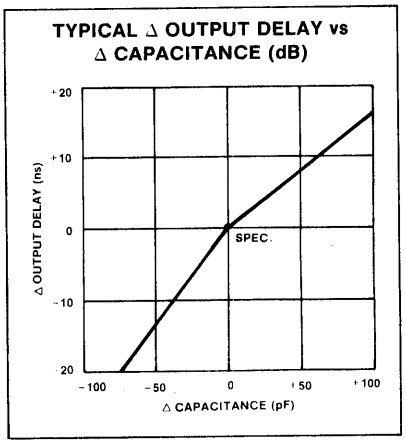


NOTE

Applicable pinout numbers are included within parentheses.

TEST LOAD CIRCUIT





DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0		V_{CC}	
V_{IL}	Low		-0.5		0.8	
	Output voltage					V
V_{OH}	High	$I_{OH} = -100\mu A$	2.4			
V_{OL}	Low	$I_{OL} = 1.6mA$			0.45	
	Leakage					μA
I_{DL}	Data bus	$V_{OUT} = 0.45V$			-50	
I_{IL}	Input	$V_{OUT} = V_{CC}$ $V_{IN} = V_{CC}$			10 10	
I_{CC}	Power supply current			45	80	mA
	Capacitance	$T_A = 25°C$; V_{CC} = GND = 0V				pF
C_{IN}	Input	$f_c = 1MHz$			10	
$C_{I/O}$	I/O	Unmeasured pins returned to GND			20	

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V.

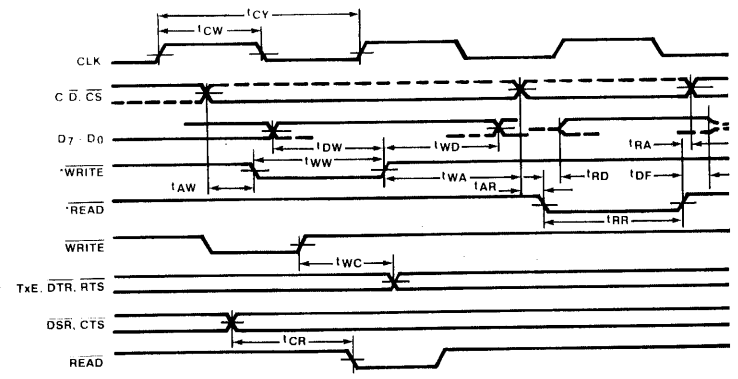
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
BUS PARAMETERS[1]						
Read Cycle						
t_{AR}	Address stable before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)		50			ns
t_{RA}	Address hold time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)		5			ns
t_{RR}	$\overline{READ}$ pulse width		430			ns
t_{RD}	Data delay from $\overline{READ}$	$C_L = 100pF$			350	ns
t_{DF}	$\overline{READ}$ to data floating	$C_L = 100pF$			200	ns
		$C_L = 15pF$	25			ns
t_{RV}	Recovery time between WRITES[2]		6			t_{CY}
Write Cycle						
t_{AW}	Address stable before $\overline{WRITE}$		20			ns
t_{WA}	Address hold time for $\overline{WRITE}$		20			ns
t_{WW}	$\overline{WRITE}$ pulse width		400			ns
t_{DW}	Data set-up time for $\overline{WRITE}$		200			ns
t_{WD}	Data hold time for $\overline{WRITE}$		40			ns
OTHER TIMINGS						
t_{CY}	Clock period[3]		0.420		1.35	μs
$t_{\phi W}$	Clock pulse width		220		0.7t_{CY}	ns
t_R, t_F	Clock rise and fall time		0		50	ns
t_{DTx}	TxD delay from falling edge of $\overline{TxC}$	$C_L = 100pF$			1	μs
t_{SRx}	Rx data set-up time to sampling pulse	$C_L = 100pF$	2			μs
t_{HRx}	Rx data hold time to sampling pulse	$C_L = 100pF$	2			μs
f_{Tx}	Transmitter input clock frequency					
	1x baud rate		DC		56	kHz
	16x and 64x baud rate		DC		520	kHz
t_{TPW}	Transmitter input clock pulse width					
	1x baud rate		12			t_{CY}
	16x and 64x baud rate		1			t_{CY}
t_{TPD}	Transmitter input clock pulse delay					
	1x baud rate		15			t_{CY}
	16x and 64x baud rate		3			t_{CY}
f_{Rx}	Receiver input clock frequency					
	1x baud rate		DC		56	kHz
	16x and 64x baud rate		DC		520	kHz
t_{RPW}	Receiver input clock pulse width					
	1x baud rate		12			t_{CY}
	16x and 64x baud rate		1			t_{CY}
t_{RPD}	Receiver input clock pulse delay					
	1x baud rate		15			t_{CY}
	16x and 64x baud rate		3			t_{CY}
t_{Tx}	TxRDY delay from center of data bit	$C_L = 50pF$			16	t_{CY}
t_{Rx}	RxRDY delay from center of data bit				20	t_{CY}
t_{IS}	Internal SYNDET delay from center of data bit				25	t_{CY}
t_{ES}	Internal SYNDET set-up time before falling edge of $\overline{RxC}$				16	t_{CY}
t_{TxE}	TxEMPTY delay from center of data bit	$C_L = 50pF$			16	t_{CY}
t_{WC}	Control delay from rising edge of $\overline{WRITE}$ ($\overline{TxE}$, $\overline{DTR}$, $\overline{RTS}$)				16	t_{CY}
t_{CR}	Control to $\overline{READ}$ set up time ($\overline{DSR}$, $\overline{CTS}$)				16	t_{CY}

NOTES

1. AC timings measured at $V_{OH} = 2.0V$, $V_{OL} = 0.8V$, and with test load circuit.
2. This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
3. The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitations with respect to CLK:
   for 1x baud rate, f_{Tx} or $f_{Rx} \leq 1/30\ t_{CY}$)
   for 16x and 64x baud rate, f_{Tx} or $f_{Rx} \leq 1/4.5\ t_{CY}$)

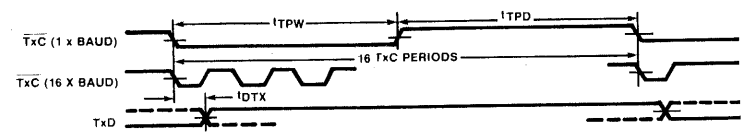
TIMING WAVEFORMS

READ AND WRITE TIMING

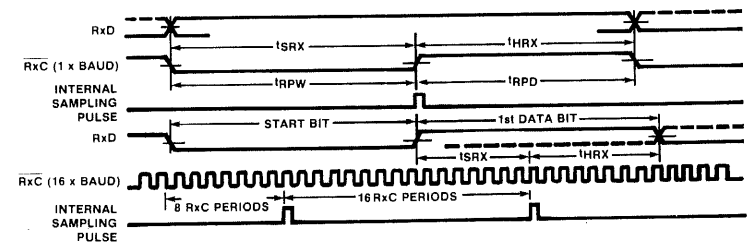


*Write and read pulses have no timing limitation with respect to CLK.

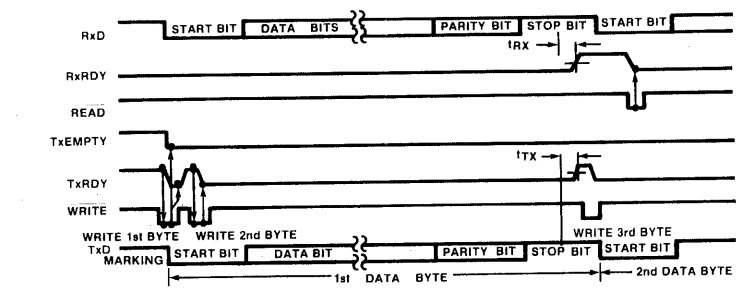
TRANSMITTER CLOCK AND DATA



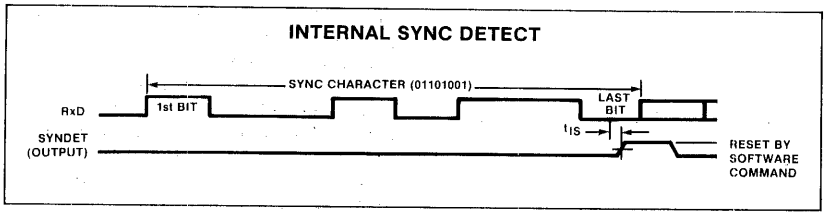
RECEIVER CLOCK AND DATA

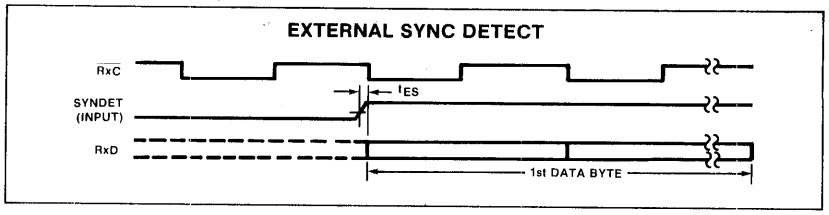


TxRDY AND RxRDY TIMING (ASYNC MODE)

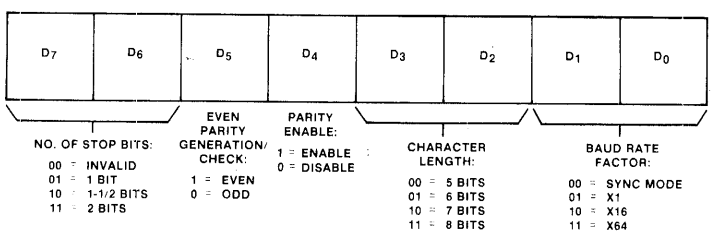


TIMING WAVEFORMS (Cont'd)

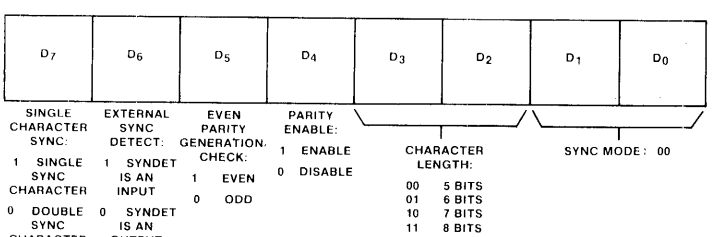




MODE INSTRUCTION CONTROL WORD FORMAT

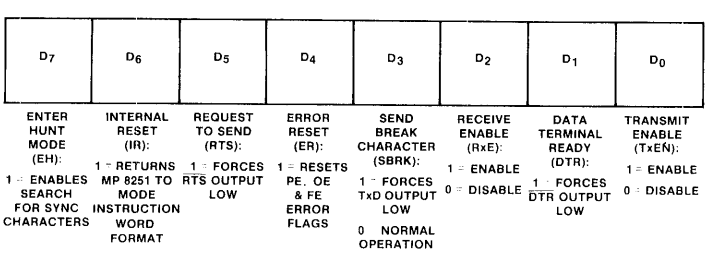


a. Asynchronous Mode

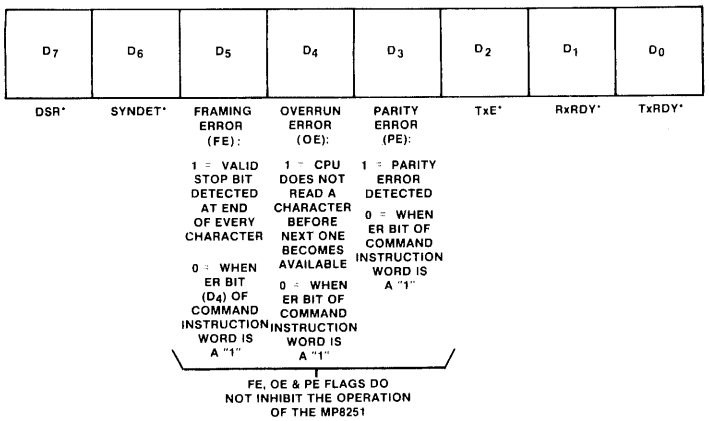


b. Synchronous Mode

COMMAND INSTRUCTION CONTROL WORD FORMAT

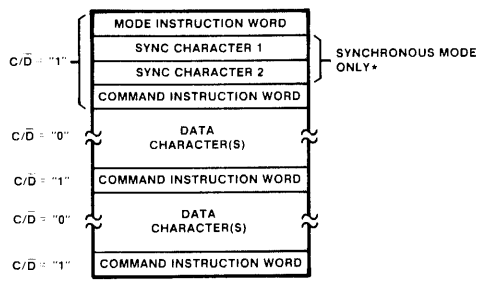


STATUS READ WORD FORMAT



*NOTE
Bits D_0-D_2, D_6 & D_7 have identical meanings to external output pins.

TYPICAL DATA BLOCK TRANSFER



*NOTE
When the mode instruction word has programmed the MP8251 to single sync character (bit D_7 = "1"), sync character 2 is omitted. Both sync characters are omitted in the asynchronous mode.

MP8251 STATUS

The MP8251 has provisions for allowing the programmer to read the status of the device at any time during the functional operation. When the C/$\overline{D}$ input is a high-level, a normal read operation is executed to read this status information. The figure below shows the bits in the Status Read Word format. Since some of the status word bits have identical meaning to external output pins, the MP8251 can be used in a completely polled environment or in an interrupt driven environment.

DESCRIPTION

The MP8255 is a programmable peripheral interface contained in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a general-purpose parallel input/output interface in Signetics MP8080A microcomputer family. The functional configuration of the MP8255 is programmed by the system software so that normally no external logic is required to interface peripheral devices.

The MP8255 has three basic modes of operation that can be selected by the system software. In the first mode (Mode 0), the MP8255 provides simple input and output operations for three 8-bit ports. Data is simply written to or read from a specified port (Port A, B, or C) without the use of "handshaking" signals. In the second mode (Mode 1), the MP8255 enables the transfer of input/output data to or from a specified 8-bit port (Port A or B) in conjunction with strobes or "handshaking" signals. Ports A and B use the lines of Port C in this mode to generate or accept the "handshaking" signals with the peripheral device. In the third mode (Mode 2), the MP8255 enables communications with a peripheral device or structure via one bidirectional 8-bit bus port (Port A). "Handshaking" signals are provided over the lines of Port C in this mode to maintain proper bus flow discipline.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
T_A	Ambient temperature under-bias	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
	Voltage on any pin with respect to ground	-0.5 to +7	V

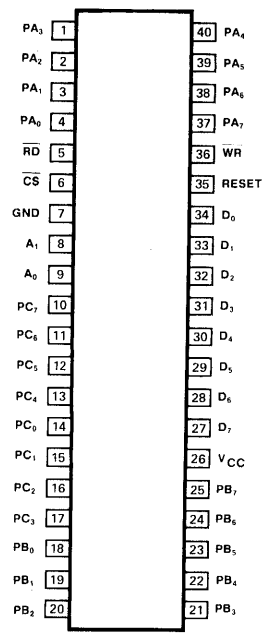
AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V ± 5%; V_{SS} = 0V

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t_{WP}	Pulse width of $\overline{WR}$	430			ns
t_{DW}	Time D.B. stable before $\overline{WR}$	10			ns
t_{WD}	Time D.B. stable after $\overline{WR}$	65			ns
t_{AW}	Time address stable before $\overline{WR}$	20			ns
t_{WA}	Time address stable after $\overline{WR}$	35			ns
t_{CW}	Time CS stable before $\overline{WR}$	20			ns
t_{WC}	Time CS stable after $\overline{WR}$	35			ns
t_{WB}	Delay from $\overline{WR}$ to output			500	ns
t_{RP}	Pulse width of $\overline{RD}$	430			ns
t_{IR}	$\overline{RD}$ set-up time	50			ns
t_{HR}	Input hold time	50			ns
t_{RD}	Delay from $\overline{RD}$ = 0 to system bus			350	ns
t_{OD}	Delay from $\overline{RD}$ = 1 to system bus	150			ns
t_{AR}	Time address stable before $\overline{RD}$	50			ns
t_{CR}	Time $\overline{CS}$ stable before $\overline{RD}$	50			ns
t_{AK}	Width of $\overline{ACK}$ pulse	500			ns
t_{ST}	Width of $\overline{STB}$ pulse	350			ns
t_{PS}	Set-up time for peripheral	150			ns
t_{PH}	Hold time for peripheral	150			ns
t_{RA}	Hold time for A_1, A_0 after $\overline{RD}$ = 1	379			ns
t_{RC}	Hold time for $\overline{CS}$ after $\overline{RD}$ = 1	5			ns
t_{AD}	Time from $\overline{ACK}$ = 0 to output (Mode 2)			500	ns
t_{KD}	Time from $\overline{ACK}$ = 1 to output floating			300	ns
t_{WO}	Time from $\overline{WR}$ = 1 to $\overline{OBF}$ = 0			300	ns
t_{AO}	Time from $\overline{ACK}$ = 0 to $\overline{OBF}$ = 1			500	ns
t_{SI}	Time from $\overline{STB}$ = 0 to IBF			600	ns
t_{RI}	Time from $\overline{RD}$ = 1 to IBF = 0			300	ns

PIN CONFIGURATION

IWA PACKAGE



FEATURES

- **Outputs source 1mA at 1.5 volts**
- **24 programmable input/output pins**
- **Direct bit set reset capability**
- **TTL compatible**
- **Reduces system component count**

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
$\overline{CS}$	6	I	**Chip Select:** When low, the chip is selected. This enables communication between the MP8255 and the MP8080A microprocessor.
$\overline{RD}$	5	I	**Read:** When low, allows the MP8080A to read data or status information from the MP8255.
$\overline{WR}$	36	I	**Write:** When low, allows the MP8080A to write data or control words into the MP8255.
A_0,A_1	9,8	I	**Port Select:** These two inputs, which are normally connected to the least significant bits of the A_{15} - A_0 Address Bus, control the selection of one of three 8-bit ports (A, B, and C) or the internal control word register as indicated below.
RESET	35	I	**Reset:** When high, clears all the internal registers of the chip and sets Ports A, B and C to the input high impedance mode.
D_7 - D_0	27 - 34	I/O	**Data Bus:** This bus comprises eight tri-state input/output lines. The bus provides bidirectional communication between the MP8255 and the MP8080A. Data is routed to or from the internal data bus buffer upon execution of an Out or In instruction, respectively, by the MP8080A. In addition, control words and status information are transferred through the data bus buffer.
PA_7 - PA_0	37 - 40, 1 - 4	I/O	**Port A:** This 8-bit input/output port comprises one 8-bit data output latch/buffer and the 8-bit data input latch.*
PB_7 - PB_0	25 - 18	I/O	**Port B:** This 8-bit input/output port comprises one 8-bit data input and output latch/buffer and 8-bit data buffer.
PC_7 - PC_4 PC_3 - PC_0	10 - 13 17 - 14	I/O	**Port C:** This 8-bit input/output port comprises one 8-bit data output latch/buffer and one 8-bit data input buffer. The port can be split into two 4-bit ports under the mode control. Each of these 4-bit ports contains a 4-bit latch that may be used for the control and status signals, in conjunction with Ports A and B. The system software includes a Bit Set/Reset Control Word (see figure) for setting or resetting any of the eight bits of Port C. When Port C is being used as a status/control for Port A and B, the Port C bits can be set or reset by using the Bit Set/Reset Control Word as the second byte of OUT Instruction(s).
V_{CC} GND	26 7	I I	**V_{CC} Supply:** +5 volts **Ground:** 0-volt reference

A_1	A_0	Selected
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control word register

*NOTE

The system software uses a Mode Definition Control Word (see figure) as the second byte of OUT Instruction(s) to program the functional configuration of Ports A through C. Whenever the mode is changed, all output registers (and status flip flops) are reset.

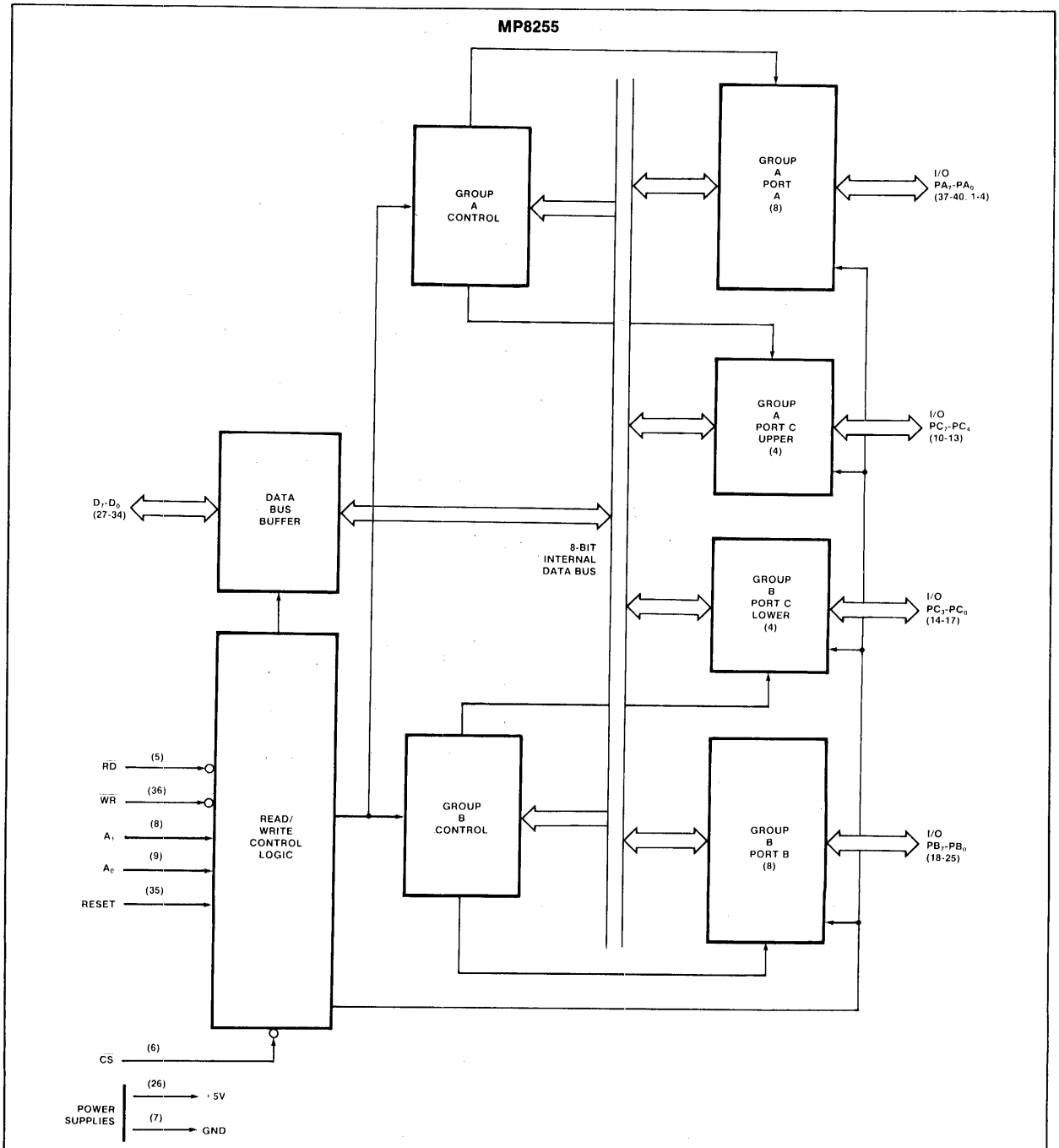
DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = ±5V ±5%; V_{SS} = 0V

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				0.8	
	Output voltage					V
V_{OH}	High	I_{OH} = -50μA (-100μA for D,B, Port)	2.4			
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
I_{OH}*	Darlington drive current	V_{OH} = 1.5V, R_{EXT} = 390Ω		2.0		mA
I_{CC}	Power supply current			40		mA

*NOTE

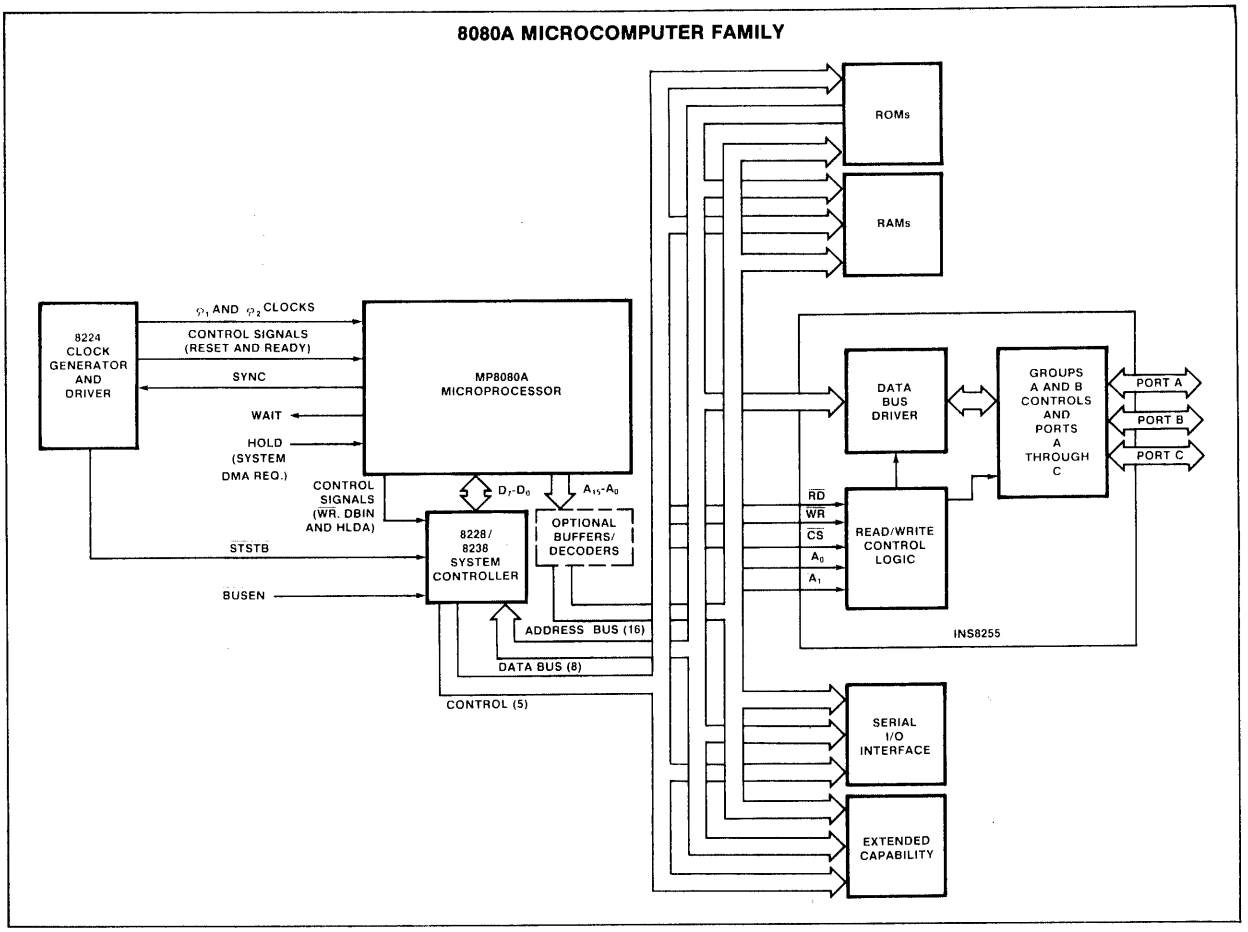
Available on 8 pins only of ports A and C, selected randomly.

BLOCK DIAGRAMS

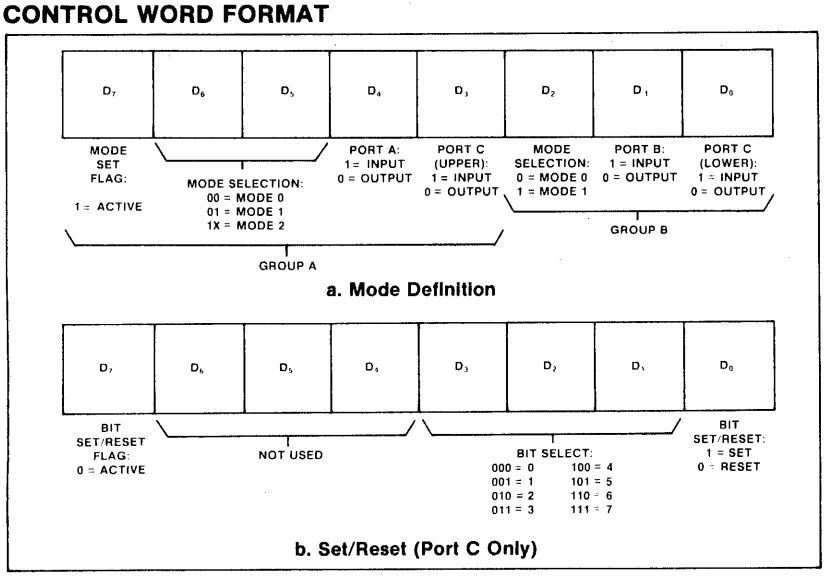


NOTE:
Applicable pinout numbers are included within parentheses.

BLOCK DIAGRAMS



CONTROL WORD FORMAT



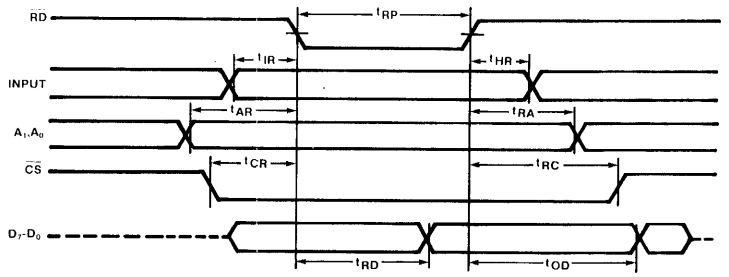
OPERATING MODES

Mode 0 (Basic Input/Output)

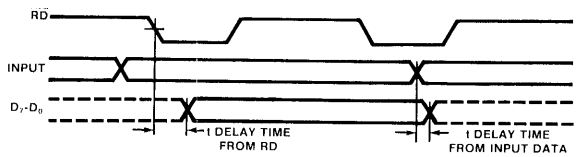
In this mode, simple input and output operations for each of the three ports are provided. No "handshaking" is required; data is simply written to or read from a specified port.

TIMING DIAGRAMS

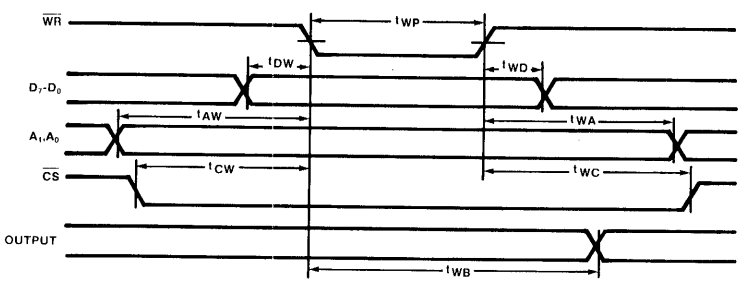
MODE 0 (BASIC INPUT)



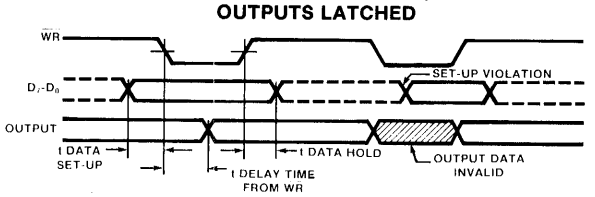
MODE 0 (BASIC INPUT)
D7-D0 FOLLOWS INPUT-NO LATCHING



MODE 0 (BASIC OUTPUT)



MODE 0 (BASIC INPUT)
OUTPUTS LATCHED



MODE 0 PORT DEFINITION CHART

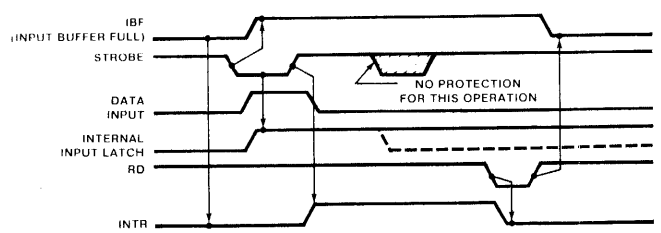
NO.	CONTROL WORD BITS								GROUP A		GROUP B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	Port C (Upper)	Port B	Port C (Lower)
0	1	0	0	0	0	0	0	0	Output	Output	Output	Output
1	1	0	0	0	0	0	0	1	Output	Output	Output	Input
2	1	0	0	0	0	0	1	0	Output	Output	Input	Output
3	1	0	0	0	0	0	1	1	Output	Output	Input	Input
4	1	0	0	0	1	0	0	0	Output	Input	Output	Output
5	1	0	0	0	1	0	0	1	Output	Input	Output	Input
6	1	0	0	0	1	0	1	0	Output	Input	Input	Output
7	1	0	0	0	1	0	1	1	Output	Input	Input	Input
8	1	0	0	1	0	0	0	0	Input	Output	Output	Output
9	1	0	0	1	0	0	0	1	Input	Output	Output	Input
10	1	0	0	1	0	0	1	0	Input	Output	Input	Output
11	1	0	0	1	0	0	1	1	Input	Output	Input	Input
12	1	0	0	1	1	0	0	0	Input	Input	Output	Output
13	1	0	0	1	1	0	0	1	Input	Input	Output	Input
14	1	0	0	1	1	0	1	0	Input	Input	Input	Output
15	1	0	0	1	1	0	1	1	Input	Input	Input	Input

Mode 1 (Strobed Input/Output)

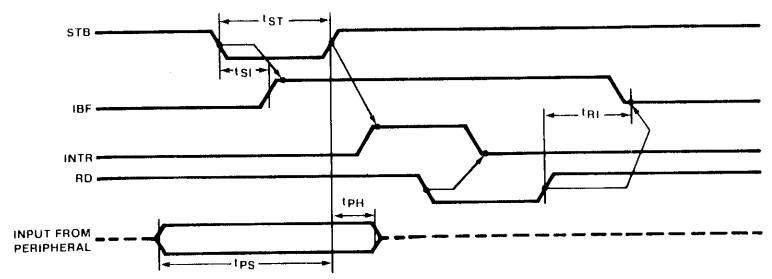
In this mode, a means for transferring input/output data to or from a specified port in conjunction with strobes or "handshaking" signals is provided. Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals in Mode 1. The programmer can read the contents of Port C to test or verify the status of each peripheral device. Since no special instruction is provided in the MP8080A microcomputer system to read the Port C status information, a normal read operation must be executed to perform this function.

TIMING DIAGRAMS

MODE 1 INPUT TIMING

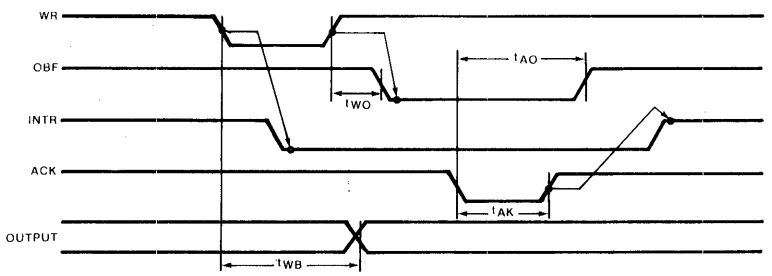


MODE 1 (STROBED INPUT)

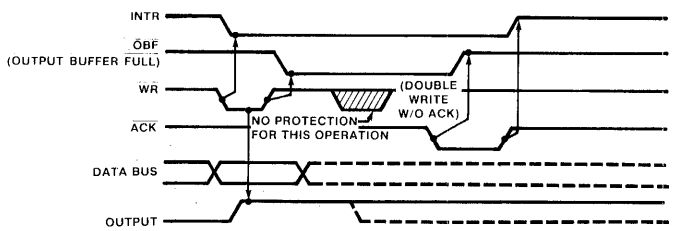


TIMING DIAGRAMS (Cont'd)

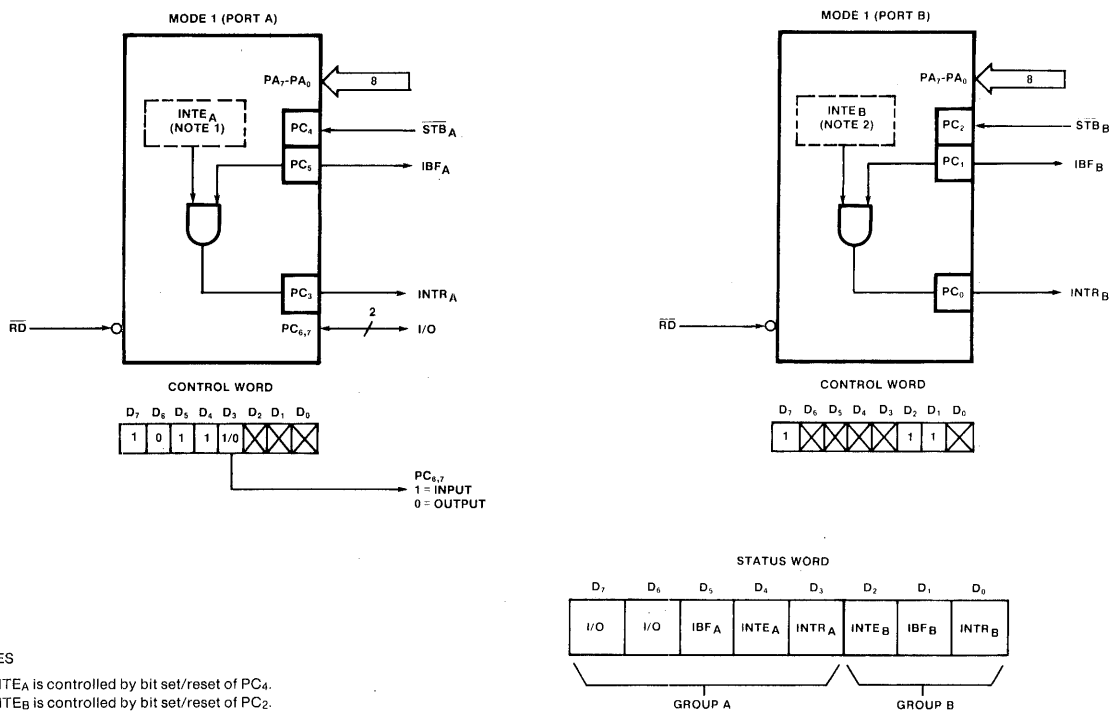
MODE 1 (STROBED OUTPUT)



MODE 1 OUTPUT TIMING



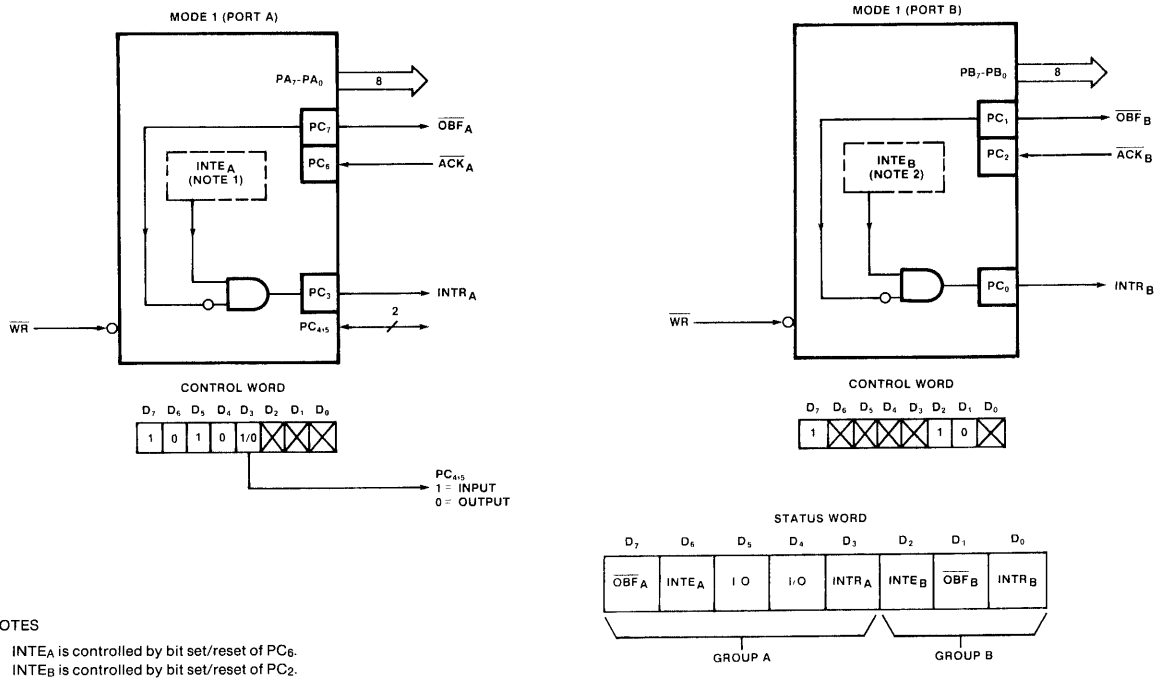
MODE 1 INPUT



NOTES

1. $INTE_A$ is controlled by bit set/reset of PC_4.
2. $INTE_B$ is controlled by bit set/reset of PC_2.

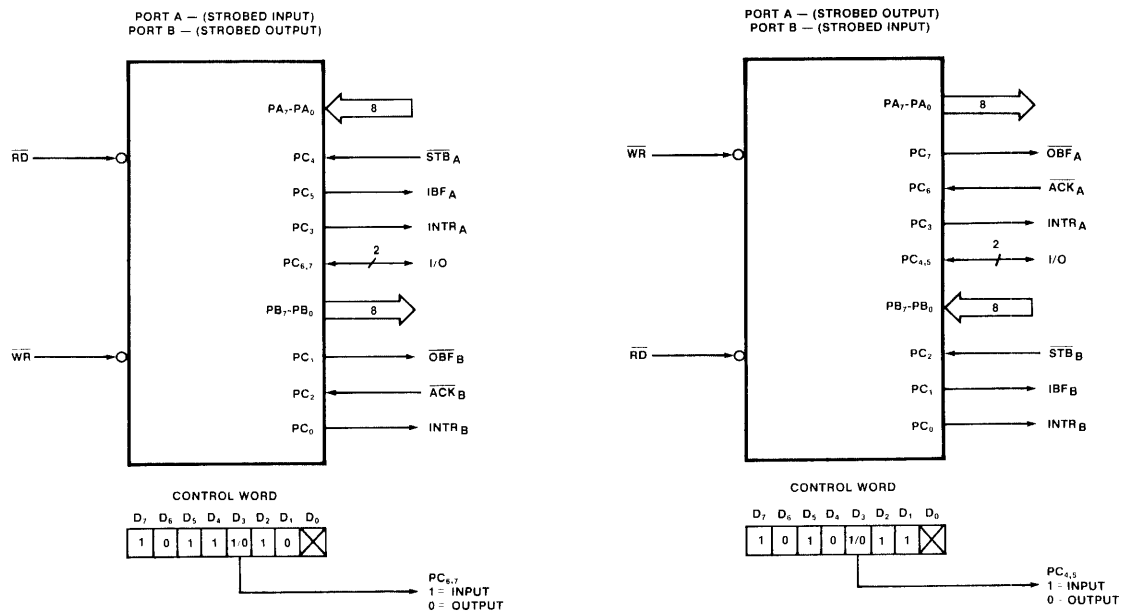
MODE 1 OUTPUT



NOTES

1. $INTE_A$ is controlled by bit set/reset of PC_6.
2. $INTE_B$ is controlled by bit set/reset of PC_2.

MODE 1 COMBINATIONS

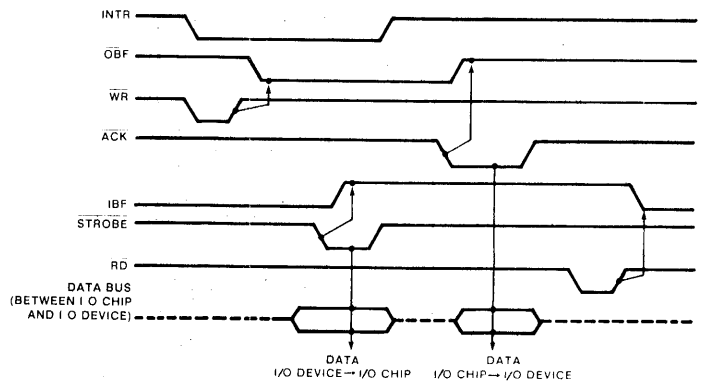


Mode 2 (Strobed Bidirectional Bus Input/Output)

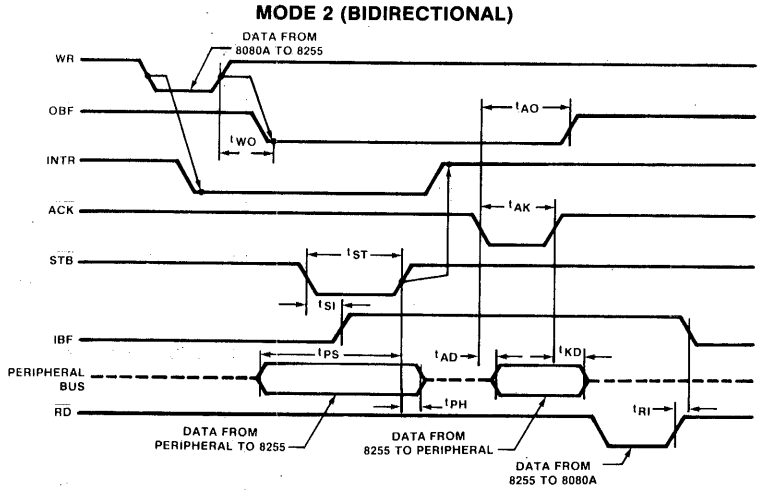
This mode enables communication with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus input/output). "Handshaking" signals are provided to maintain proper bus flow discipline in a manner similar to Mode 1. In addition, interrupt generation and enable/disable functions are available in Mode 2.

TIMING DIAGRAMS

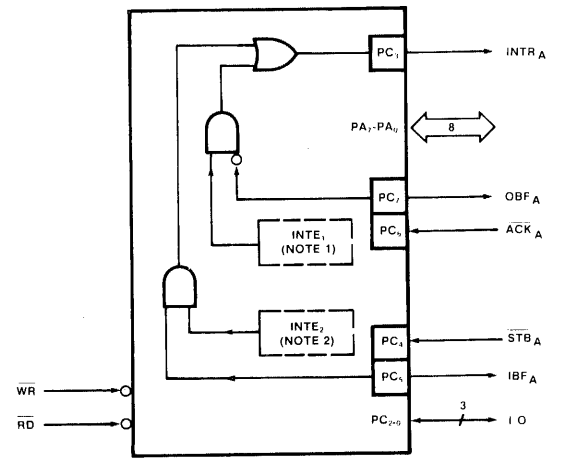
MODE 2 TIMING



MODE 2 (BIDIRECTIONAL)



MODE 2



CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	X	X	X	1/0	1/0	1/0

PC7-6
1 INPUT
0 OUTPUT

PORT B
1 INPUT
0 OUTPUT

GROUP B MODE
0 MODE 0
1 MODE 1

STATUS WORD

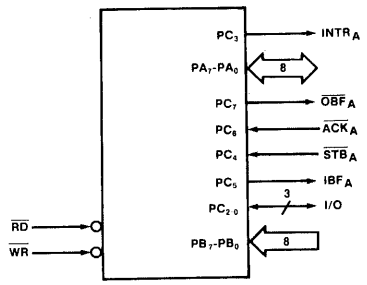
D7	D6	D5	D4	D3	D2	D1	D0
$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	X	X	X

GROUP A — GROUP B (DEFINED BY MODE 0 OR MODE 1 SELECTION)

NOTES
1. $INTE_1$ is controlled by bit set/reset of PC6.
2. $INTE_2$ is controlled by bit set/reset of PC4.

MODE 2 COMBINATIONS

MODE 2 AND MODE 0 (INPUT)

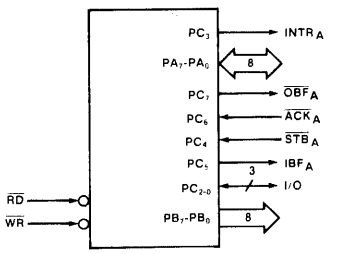


CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	X	X	X	0	1	1/0

PC2-0
1 = INPUT
0 = OUTPUT

MODE 2 AND MODE 0 (OUTPUT)

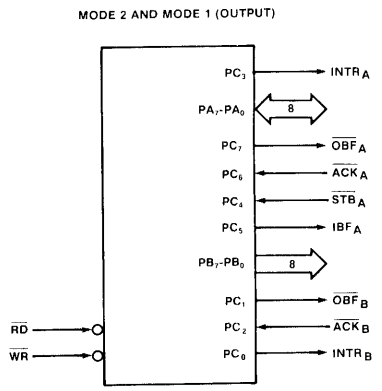


CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	X	X	X	0	0	1/0

PC2-0
1 = INPUT
0 = OUTPUT

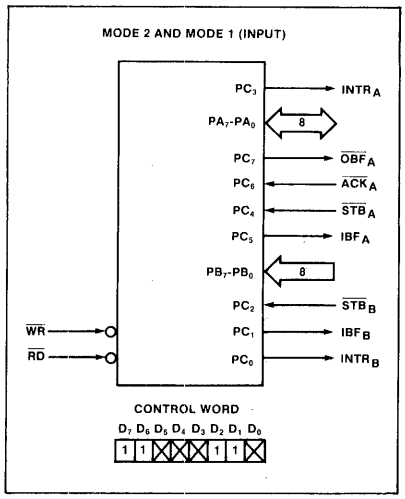
MODE 2 AND MODE 1 (OUTPUT)



CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	X	X	X	1	0	X

MODE 2 COMBINATIONS (Cont'd)



MODE DEFINITION SUMMARY TABLE

PORT BITS	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	In	Out	In	Out	Bidirectional
PA_1	In	Out	In	Out	
PA_2	In	Out	In	Out	
PA_3	In	Out	In	Out	
PA_4	In	Out	In	Out	
PA_5	In	Out	In	Out	
PA_6	In	Out	In	Out	
PA_7	In	Out	In	Out	Bidirectional
PB_0	In	Out	In	Out	
PB_1	In	Out	In	Out	
PB_2	In	Out	In	Out	
PB_3	In	Out	In	Out	(Mode 0 or Mode 1 only)
PB_4	In	Out	In	Out	
PB_5	In	Out	In	Out	
PB_6	In	Out	In	Out	
PB_7	In	Out	In	Out	
PC_0	In	Out	$INTR_B$	$INTR_B$	I/O
PC_1	In	Out	IBF_B	$\overline{OBF}_B$	I/O
PC_2	In	Out	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	In	Out	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	In	Out	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	In	Out	IBF_A	I/O	IBF_A
PC_6	In	Out	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	In	Out	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

2

DESCRIPTION

The KT9000 kit contains a 2650 microprocessor and enough chips to allow for the implementation of a small developmental system. Since the interface requirements of the 2650 are completely TTL compatible, no attempt has been made to limit the user's flexibility by dictating a fixed logic configuration. There is complete freedom in using standard SSI or MSI logic to adapt the microprocessor to the memory, I/O devices, or clock.

Several minimal system examples are presented to enable quick set up and evaluation. Other configurations to adapt to individual requirements should become evident from these examples.

PARTS DESCRIPTIONS

2112: The 2112 is a static 1024-bit Random Access Memory organized as 256 words by 4 Bits/Word. It is fabricated with N-Channel, Silicon Gate, MOS technology and achieves an access time of less than 800 nanoseconds. No clocks are required, and the chip is powered from a single 5 volt source.

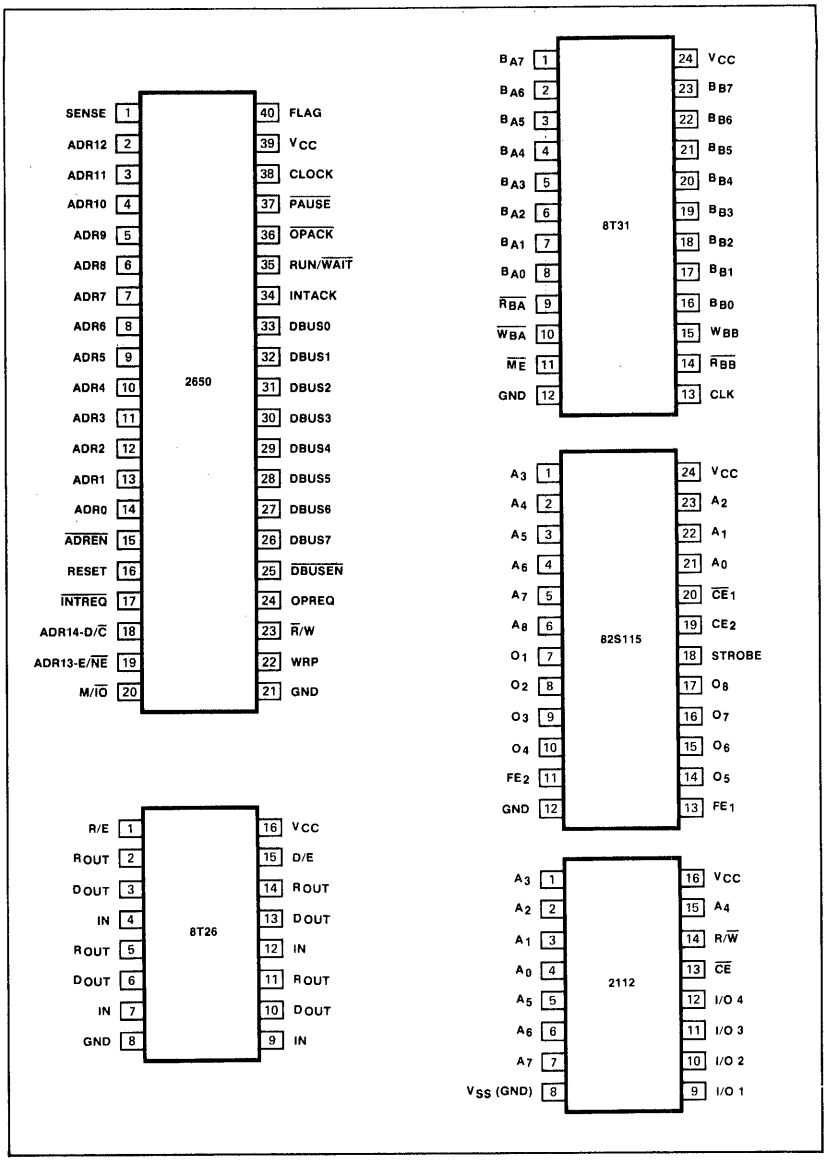
82S115I: The 82S115I is a 4096-bit Schottky-Clamped, Bipolar Read Only Memory, incorporating on-chip data output registers. It is field-programmable and fully TTL compatible with on-chip decoding and two chip enable inputs for ease of memory expansion. Inputs to the device are PNP transistors with a maximum current requirement of 100μA.

8T31: The 8T31 is an 8-bit Bidirectional I/O Port designed to function as a general purpose I/O interface element. It consists of 8 clocked latches with two sets of bidirectional Inputs/Outputs. The capability exists for various hook-up schemes allowing master control from either the microprocessor or from the I/O device.

8T26B: The 8T26B consists of four pairs of inverting Tri-State Logic elements configured as a Quad Bus Drivers/Receivers with separate buffered receiver enable and driver enable lines. Both the driver and receiver gates have Tri-State outputs and low-current PNP inputs.

CIRCUIT EXAMPLES

Two circuit configurations are presented to indicate a possible program checkout approach. Figure 1 is hooked up to allow the use of RAM for program debugging. The second figure represents a possible final system configuration with the program fixed in PROM. Both circuits use the 8T26's as bus buffers.



PARTS LIST

PART NO.	QTY	DESCRIPTION	REFERENCE DATA SHEET
2650	1	CPU	—
2112	4	256X4 RAM	MOS Products
82S115I	1	4K PROM (Unprogrammed) 512X8	Bipolar Memories
8T31I	2	8-bit Bidirectional I/O Port	8000 Product
8T26B	4	Quad Bus DR/REC	8000 Product
2650BM1000	1	Basic Manual	—

EXAMPLE OF INITIAL PROGRAM CHECKOUT CONFIGURATION

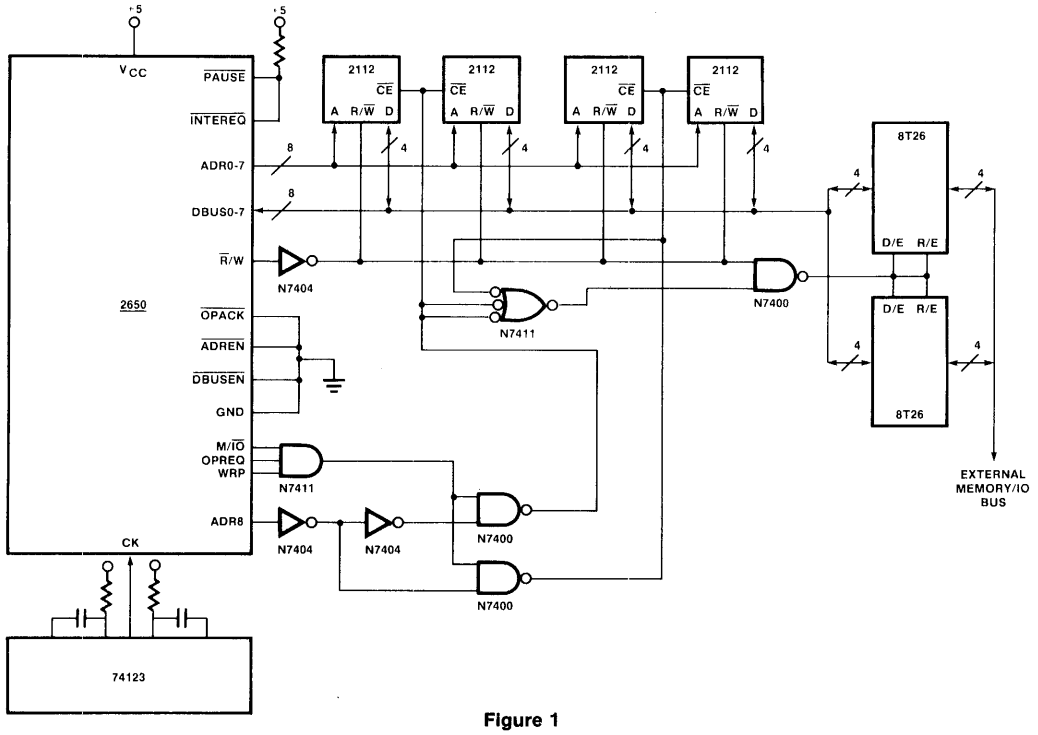


Figure 1

FINALIZED CONFIGURATION WITH PROGRAM FIXED IN PROM

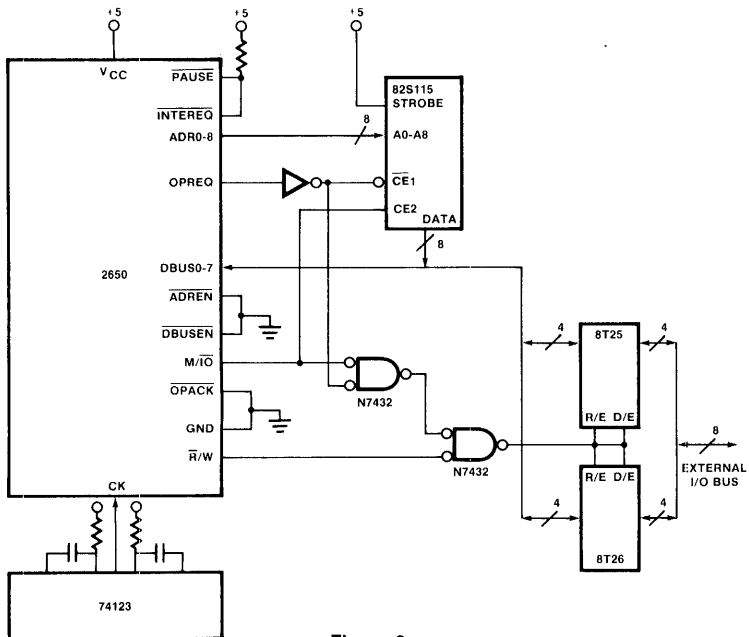
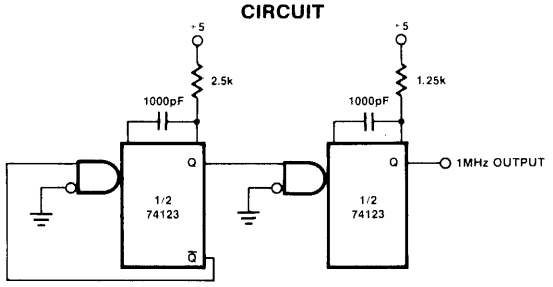


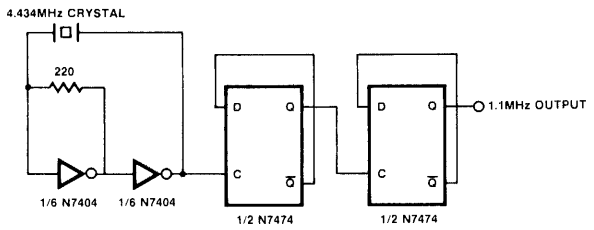
Figure 2

TYPICAL APPLICATIONS

ONESHOT CLOCK OSCILLATOR CIRCUIT



CRYSTAL OSCILLATOR CIRCUIT



DESCRIPTION

The Signetics Adaptable Board Computer, ABC 1500, is a modular microcomputer containing a CPU, memory, I/O ports and support circuitry. It is designed to cover a broad range of applications from software development to system hardware prototyping. Cost performance trade offs have been carefully considered to achieve maximum flexibility and allow the card to be tailored to a variety of individual requirements.

The basic configuration consists of the 2650 8-bit microprocessor, 512 bytes of read/write memory (four 2112 static RAM's), 1K bytes of 2608 ROM with PIPBUG*, two 8T31 I/O ports and buffering on data, address and control lines. A single +5 volt supply will be required to power the card and communicate with a serial 20mA current loop terminal.

Modifications to the basic system can be easily made to allow for various memory configurations and operating modes. Unused plated through holes are provided for the PROM memory chips (82S115's). Other options are jumper selectable.

The ABC 1500 is sold either as a completely assembled and tested card (2650PC1500) or in kit form (2650KT9500).

*PIPBUG is a loader, editor, and debug program. See Table 1.

FEATURES

- **Expandable printed circuit card: Unused area on card filled with plated through holes on .300 in. centers for wirewrap sockets**
- **1K bytes of PIPBUG* ROM (in socket)**
- **512 bytes of RAM**
- **Two latched I/O ports —four non-extended I/O read/write user strobes**
- **Tri-state buffers on data, address and control lines**
- **Serial input/output port**
- **Single +5 volt supply requirement (1.7A max) for card and 20mA current loop interface (±12 volt supply for RS232 interface)**
- **Interrupt and single step capability**
- **Simple clock configured from dual monostable multivibrator**
- **24K memory expansion capability**
- **Directly compatible with 4K RAM card (2650PC2000) and power supply demonstration base (2650DS2000)**
- **Card dimensions: 8 in. by 6.875 in. with a 100 pin connector along the 8 in. dimension**

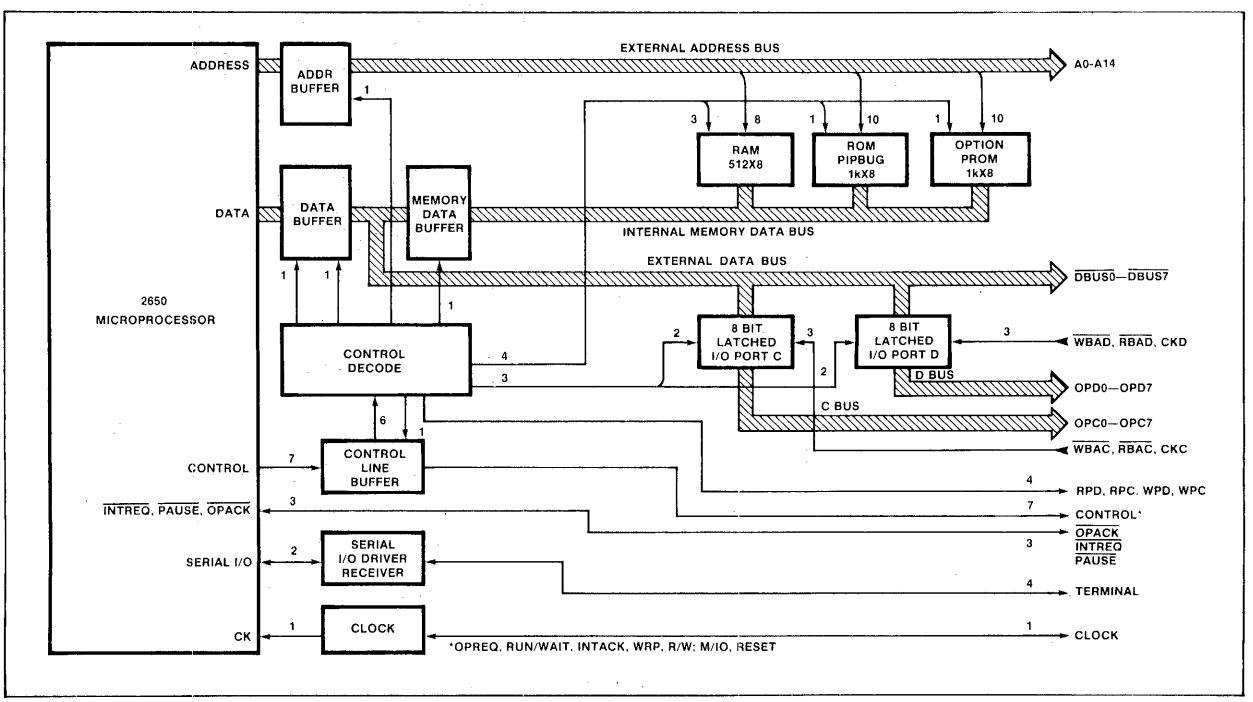
OPTIONS

- **1K bytes of PROM in place of ROM**
- **512 bytes of PROM or ROM in place of RAM**
- **Asynchronous operation capability**
- **External clock input**
- **Interrupt vector from Port C**

INTERFACE

- **Terminal interface jumper selectable**
  A. W4 to W5 and W6 to W7 jumpers select the 20mA current loop mode
  B. W3 to W4 and W7 to W8 jumpers select the RS232 mode
- **Normally high input lines (10k pull up resistor on each): $\overline{\text{INTREQ}}$, $\overline{\text{PAUSE}}$, $\overline{\text{RESET}}$, $\overline{\text{WBAC}}$, $\overline{\text{WBAD}}$, CKC, CKD**
- **Plated through holes are available at each connector pin to allow for insertion of wirewrap pins.**
- **Edge connector supplied with card**
- **To allow for external clock input, remove jumper W9-W10**
- **Asynchronous operation by removing jumper W1 to W2 and driving $\overline{\text{OPACK}}$**
- **During vectored interrupts, it is possible to allow port C to place the interrupt address on the data bus by removing jumper W21-W22 and jumpering W22-W23**

ABC 1500 BLOCK DIAGRAM



ALPHA CHARACTER INPUT	COMMAND
A	Alter memory
B	Set breakpoint
C	Clear breakpoint
D	Dump memory to papertape
G	Go to address
L	Load memory from papertape
S	See and alter registers

NOTE
The program is entered by resetting the card.
The terminal will then respond with an asterisk (*).

Table 1 PIPBUG COMMANDS

MEMORY CONFIGURATION

All of page 0 is reserved for on card memory (0 to 8191_{10}). Address lines A9, A11 and A12 are not decoded (Don't care signals) allowing two IC's to perform not only memory decoding but also I/O port decoding. As an added benefit, usable memory space exists at the top of page 0 (see Table 2) due to the interleaving effect between the ROM and RAM memories. This memory space can be used as interrupt vector address locations in a negative direction from address location "0" (a negative relative instruction from address location "0" wraps around the first 8K page).

There are a total of two blocks in the RAM structure, each of which contains 256 bytes of RAM. Since PIPBUG uses the first 63 RAM locations for temporary storage, the first actual user location is 1087_{10} ($43F_{16}$) (there are seven other address locations corresponding to the first user location—see memory map). Starting at $43F_{16}$, the range for on card RAM extends to address 1535_{10} ($5FF_{16}$), giving a total usable on-card space of 449 bytes.

The first external memory location for add-on memory is 8192_{10} (2000_{16}). All of page 1, 2, and 3 are available, giving a total memory expansion capability of 24K.

MEMORY OPTIONS

Modifications to the basic configuration can be made to provide a mix of RAM/PROM/ROM memories. PROM memories can be used in place of the PIPBUG ROM by removing the ROM from its socket and adding one or two 82S115 PROMs (512X8). Area and plated through holes are provided on the card for insertion of sockets for the PROMs or the PROMs themselves. Decoding for the PROMs has been provided by ABC 1500 logic.

Data and address lines for 2112 RAMs and 82S129 PROMs or 82S229 ROMs are identical. It is, therefore, possible to use PROMs and/or ROMs in place of RAM. This option will require removal of the RAMs (two per block), and changing the jumper for each 256 byte block of PROM or ROM added. The jumper needed for each block of memory is as follows:

MEMORY SECTION	RAM JUMPER	PROM/ROM JUMPER
First Block	W12-W13	W11-W13
Second Block	W15-W16	W14-W16

I/O PORT CONFIGURATION

Two ports (C and D) are implemented with 8T31 bidirectional ports and can be used for general purpose I/O. Each consist of 8 clocked latches with two sets of bidirectional inputs/outputs. Data written into one side of the port will appear inverted at the other side.

One side of each port (Bus B of the 8T31) is tied to the external data bus ($\overline{DBUSX}$). The 2650 communicates with each port over this

ADDRESS LINES						DECIMAL ADDRESS	ORGANIZATION	HEX ADDRESS
A14	A13	* A12	* A11	A10	** A9			
						8K		1FFF
0	0	X	X	1	X		Second block RAM	
							First block RAM	
						7K	Second block RAM	
0	0	X	X	0	X		First block RAM	1BFF
							PIPBUG ROM	17FF
						6K		
0	0	X	X	1	X		Second block RAM	
							First block RAM	
						5K	Second block RAM	
0	0	X	X	0	X		First block RAM	13FF
							PIPBUG ROM	0FFF
						4K		
0	0	X	X	1	X		Second block RAM	
							First block RAM	
						3K	Second block RAM	
0	0	X	X	0	X		First block RAM	0BFF
							PIPBUG ROM	07FF
						2K		
0	0	X	X	1	X		Second block RAM	06FF
							First block RAM	05FF
						1K	Second block RAM	04FF
0	0	X	X	0	X		First block RAM	03FF
							PIPBUG ROM	
						0		0000

NOTES
1. * = Don't care for ROM and RAM; ** = Don't care for RAM.
2. Each block of RAM = 256 bytes.

Table 2 PAGE 0 MEMORY MAP

bus with one byte, non-extended I/O instructions. During 2650 activity with the ports, the ABC 1500 will provide four output strobes indicating the nature of the operation.

STROBE	FUNCTION	STROBE PULSE WIDTH
WPC	Write to Port C	Duration of WRP
WPD	Write to Port D	Duration of WRP
RPC	Read Port C	Duration of OPREQ
RPD	Read Port D	Duration of OPREQ

The other side of each port (Bus A of the 8T31) is controlled by the user. Four control lines are used to read, write or tri-state the buses.

CONTROL LINE		FUNCTION
$\overline{WBAD}$ (1)	$\overline{RBAD}$ (0)	Read Port D
$\overline{WBAD}$ (0)	$\overline{RBAD}$ (0)	Write to Port D
$\overline{WBAD}$ (1)	$\overline{RBAD}$ (1)	Tri-state D Bus
$\overline{WBAC}$ (1)	$\overline{RBAC}$ (0)	Read Port C
$\overline{WBAC}$ (0)	$\overline{RBAC}$ (0)	Write to Port C
$\overline{WBAC}$ (1)	$\overline{RBAC}$ (1)	Tri-state C Bus

If no external logic is connected each port will be in the "read" mode ($\overline{WBAX}$ lines pulled high). The $\overline{RBAX}$ lines are tied to ground to allow read/write control of the buses with just the $\overline{WBAX}$ lines. To allow control for tri-stating the buses, the following jumpers must be removed:

LINE	JUMPER
$\overline{RBAC}$	W19-W20
$\overline{RBAD}$	W17-W18

The clock for each port (CKC—Port C clock, CKD—Port D clock) is available at a connector pin for external control. These normally "high" lines can be pulled low to disable writing to the ports from either the 2650 or the external device.

ABC 1500 EDGE CONNECTOR SIGNAL LIST

PIN #	FUNCTION
1	GND
2	GND
3	NC*
4	$\overline{DBUS0}$
5	$\overline{DBUS1}$
6	$\overline{DBUS2}$
7	$\overline{DBUS3}$
8	$\overline{DBUS4}$
9	$\overline{DBUS5}$
10	$\overline{DBUS6}$
11	$\overline{DBUS7}$
12	NC*
13	A14—D/$\overline{C}$
14	NC*
15	A13—E/$\overline{NE}$
16	INTACK
17	$\overline{R}$/W
18	$\overline{WRP}$
19	RUN/$\overline{WAIT}$
20	OPREQ
21	$\overline{M/IO}$
22	$\overline{OPACK}$
23	CLOCK
24	$\overline{TS}$
25	$\overline{RESET}$
26	$\overline{INTREQ}$
27	$\overline{PAUSE}$
28	NC*
29	$\overline{RBAD}$
30	NC*
31	$\overline{RBAC}$
32	NC*
33	All
34	A13—E/$\overline{NE}$
35	A12
36	A14—D/$\overline{C}$
37	A9
38	A10
39	A8
40	A7
41	A6
42	A5
43	A3
44	A0
45	A1
46	A4
47	A2
48	+12V
49	-12V
50	+5V

PIN #	FUNCTION
A	GND
B	GND
C	NC*
D	OPD 0
E	OPD 1
F	OPD 2
H	OPD 3
J	OPD 4
K	OPD 5
L	OPD 6
M	OPD 7
N	NC*
P	TTY SERIAL IN +
R	TTY SERIAL IN -
S	TTY SERIAL OUT +
T	TTY SERIAL OUT -
U	RS232 GROUND
V	RS232 OUTPUT
W	NC*
X	NC*
Y	RS232 INPUT
Z	NC*
a	OPC 0
b	OPC 1
c	OPC 2
d	OPC 3
e	OPC 4
f	OPC 5
g	OPC 6
h	OPC 7
j	NC*
k	$\overline{RPD}$
m	$\overline{WBAD}$
n	WPD
p	CKD
r	NC*
s	NC*
t	NC*
u	NC*
v	$\overline{RPC}$
w	$\overline{WBAC}$
x	WPC
y	CKC
z	NC*
$\overline{a}$	NC*
$\overline{b}$	NC*
$\overline{c}$	NC*
$\overline{d}$	+12V
$\overline{e}$	-12V
$\overline{f}$	+5V

*NC = No connection

ABC 1500 PARTS LIST

QUANTITY	DESCRIPTION
1	PC1500 printed circuit board
1	Edge connector - AMP 225-804-50
1	2650 8-bit static microprocessor
1	N7402 quad 2 input NOR gate - I/O strobe logic
1	N7416 hex inverter buffer - current loop interface
1	N74123 monostable multivibrator - clock for 2650
1	N74S138 3 line to 8 line decode - control decode
1	8T15—EIA line driver - RS232 driver
4	8T26 quad Tri-state driver/receiver - data and memory data buffer
2	8T31 8-bit latched bidirectional I/O port
4	8T97 hex Tri-state driver - address and control line buffer
1	2608 static ROM (1024X8) - PIPBUG ROM - CN0035
4	2112 static RAM (256X4) - organized as 512 byte RAM
1	82S123 PROM (32X8) coded PROM CD 1500 - control decode
4	1N914 diode
1	2N2222 transistor
1	50pF capacitor
1	300pF capacitor
13	.1μF capacitor
3	4.7μF capacitor
2	220 OHM resistor
6	1K resistor
2	2K resistor
1	3.3K resistor
8	10K resistor
1	20K resistor
1	24 pin 2608 ROM socket - Robinson-Nugent ICN 246-54

NOTE
All resistors 1/4 watt.

PRELIMINARY SPECIFICATION

DESCRIPTION

The Signetics PC-4000 is an emulation of the Signetics 2656, a 40-pin NMOS-LSI system memory interface chip. The PC-4000, in circuit board form, offers the engineer a system design aid. By designing with the PC-board emulator the specific ROM and PGA (programmable gate array) patterns required for the user's application, can be determined.

In utilizing the PC-4000, the engineer-designer is able to implement the same functions as the 2656. Through a 40-pin plug and cable attached to the PC-4000, which has identical pin-outs to the 2656, the user connects the PC-4000 directly into his prototype system. He can access the 128X8 RAM and the PROM. The user can use the eight multi-function ports either as I/O ports or chip enables. Also he may use the power-on reset, and the clock generator and divider which are included on the PC-4000.

This data sheet contains:

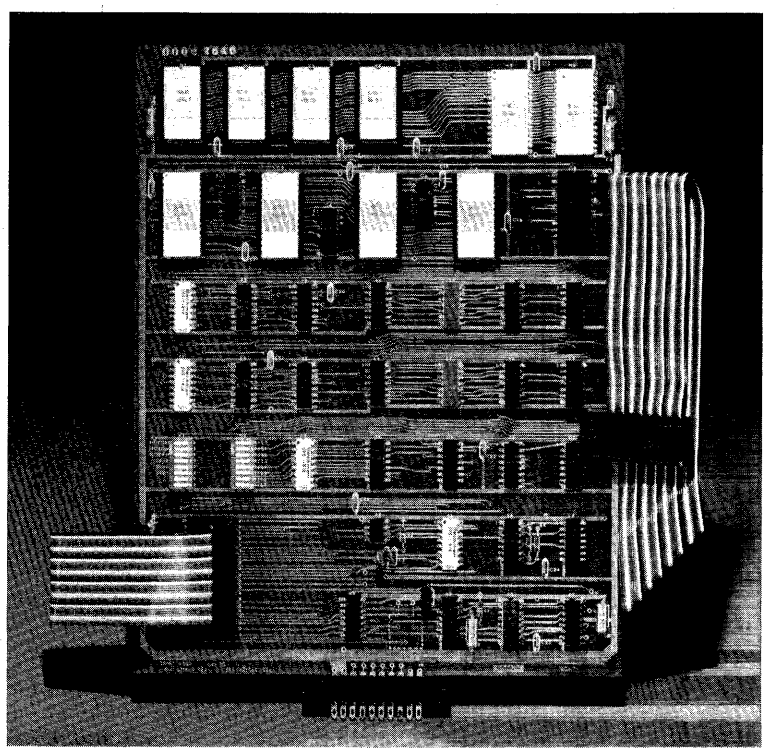
- **Circuit Emulation Description**
- **Functional Block Diagram**
- **Functional Block Descriptions**
- **Operation and Use**
  - **Load and Drive Characteristics**
  - **PC-4000 and 2656 Timing Comparisons**
  - **PC-4000 Component Positioning Diagram**
- **Programming**
  - **System Address Map for Coding the FPLAs**
  - **FPLA Coding Forms**
  - **Coding Switches and Jumpers**
- **Circuit Diagram and Connectors**
- **Parts List**
- **Shipping Configuration**

CIRCUIT EMULATION DESCRIPTION

The PC-4000 emulator contains the same circuits that are available to the user on the 2656 Systems Memory Interface chip. Functionally the PC-4000 replaces the 2656 in the user's prototyping system through a pin-for-pin compatible plug and its 40-wire ribbon cable attached to the PC-4000.

In emulating the 2656, the speed of the board circuitry is equivalent to or faster than the on-chip circuitry. ROM is implemented with bipolar PROMs and on-chip RAM is implemented with bipolar RAM packages. The programmable gate array (PGA) for selecting of the ROM and RAM enables and the I/O function selects are implemented with field programmable logic arrays (FPLAs).

PC-4000 CABLE AND CONNECTOR ASSEMBLY



The oscillator provided on the PC-4000 has the same frequency dividers available as on the 2656. The oscillator divide ratio is selected by toggle switch settings.

FUNCTIONAL BLOCK DESCRIPTIONS

Input Buffer: This circuitry buffers the incoming signals from the MPU (specifically for the 2650 MPU, the addresses, A0-A14, and the 4 control signals, OPREQ, WRP, $\overline{R}/W$ and M/$\overline{IO}$).

Data Bus Transceiver: This circuitry buffers the incoming 8-bit data bus from the MPU, and provides output drivers to the data bus.

FPLAs 1 and 2: FPLAs 1 and 2 represent a portion of the programmable gate array of the 2656 SMI chip. These 2 FPLAs decode the chip enable signals.

FPLAs 3 and 4: These FPLAs represent the remainder of the gate array. FPLA 3 and a portion of FPLA 4 generate the on-board ROM, RAM and port enable signals. The remainder of FPLA 4 is used to generate the data bus control signals.

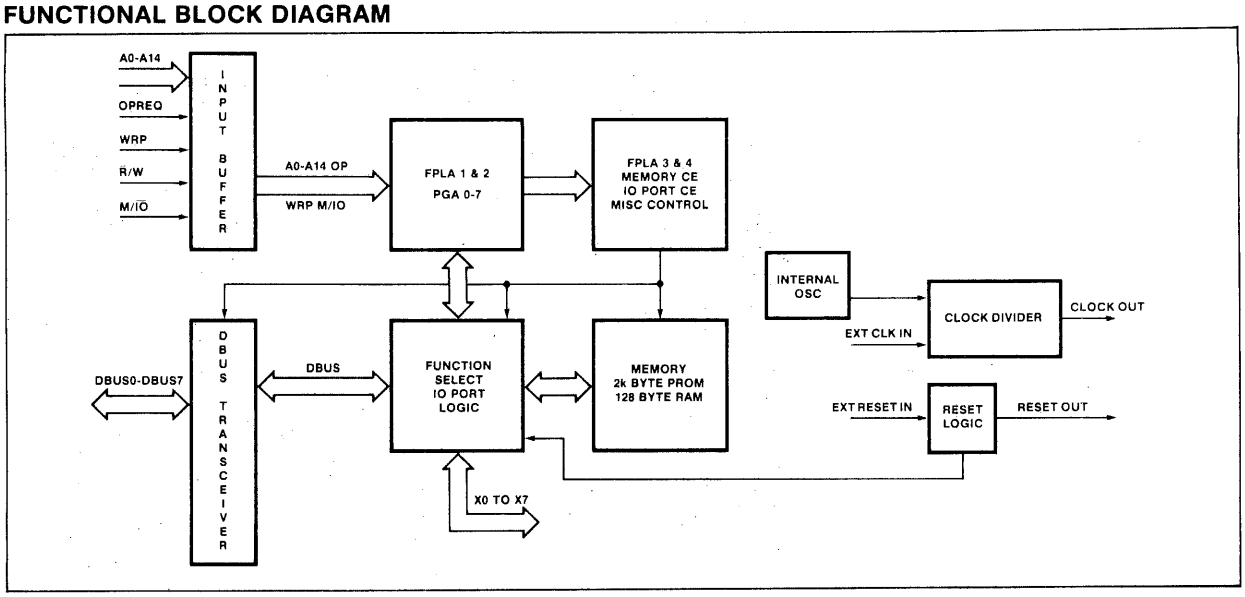
Function Select and I/O Port Logic (Via FPLAs 1-4): The function select and I/O port logic allow each of the multi-purpose pins of the 2656, to be individually selected as either an I/O port or a chip enable via eight switches, FS0-FS7. When assigned as chip enables, they must be programmed in FPLAs 1 and 2. When a multi-purpose pin is assigned as I/O or as an input port, the port address is programmed in FPLAs 1 and 2.

When the FS switch is On, the corresponding pin of the 2656 is selected as an I/O port. When the FS switch is On, the corresponding pin is selected as a chip enable.

Memory: Both ROM and RAM memory functions are implemented in bipolar PROM and RAM respectively. The memory chip enables are programmed in FPLAs 3 and 4. (See the Programming section)

Clock Divider, Reset Logic, and Internal Oscillator: This circuitry provides an internal oscillator with switches for frequency divide by 1, 2, 3, or 4. Reset logic is provided on the PC-4000 to allow the user to reset the system during debug via an external switch

FUNCTIONAL BLOCK DIAGRAM



closure, without the need for powering down. The reset logic is used when the RC or external oscillator modes are selected.

If the RC or crystal internal oscillator mode is desired, the frequency determining components must be installed on the emulator PCB. The pins on the header that correspond to the RC and Crystal pins are not used in this mode, and only the external Reset function is provided.

OPERATION AND USE

After preprogramming the on-board PROMs and FPLA with the desired user data, the operation of the PC-4000 consists of supplying electrical power from the external source and connecting into the user's system.

Power Supply Requirements: The PC-4000 requires 5Vdc at 2.2Adc typical. The maximum current requirement is 3.5Adc.

Load and Drive Characteristics: The load characteristics of PC-4000 inputs presented to any bus input are 400μAdc for a zero and 40μAdc for a 1. The PC-4000's output lines will drive a minimum of 5 TTL loads, which far exceeds the drive characteristics of the 2656 SMI. Thus the user must exercise care when changing from the emulator to the 2656 to avoid inadvertent loading problems.

PC-4000 and 2656 Timing Comparisons: The PC-4000 is implemented in TTL logic. All timing delays and Rise/Fall times are less than those of corresponding signals in the 2656.

Component Positioning Diagram: The components, sockets, switches, and jumper connections that allow the user to adapt the PC-4000 to his specific system requirements are shown in Figure 1. Positioning Diagram. Each section of the PC-board containing components that the user must either insert, adjust, or program are shown as callouts. Only pins, 1,2/A, B (GND) and 9, 10/K,L (+5Vdc) of the edge connector should be used. All other pins must be left open.

Programming and Operating Summary

1. Programming Address Functions:
   - A. Define Memory and I/O address map for system.
   - B. Program FPLA 1 and FPLA 2 with minimum programming configuration and X pin chip select information. See Coding Table for FPLA 1 and FPLA 2.
   - C. Program FPLA 3 and FPLA 4 with Memory ROM and RAM and I/O port addresses and minimum programming configuration. See Coding table for FPLA 3 and FPLA 4.

   See Tables for Coding Switches:
   - D. Is there ROM on SMI?
     If yes, program switch S2-2 (No ROM) OFF.
     If no, program switch S2-2 (No ROM) ON.
   - E. Is there RAM on SMI?
     If yes, program switch S2-3 (No RAM) OFF.
     If no, program switch S2-3 (No RAM) ON.
   - F. Is the I/O Port on SMI used?
     If yes, program switch S2-1 (No Port) OFF.
     If no, program switch S2-1 (No Port) ON.
   - G. Program Switch S2-4 (1k2k) Off if using 2656 SMI chip.
2. Clock Divider and Reset Programming:
   - A. Is SMI Oscillator XTAL Driven?
     If yes, attach XTAL to board at W6 and W7. Jumper W8 to W2, skip to Step 2E.
   - B. Is SMI Oscillator RC Driven?
     If yes, calculate capacitor value and attach capacitor to board at W6 and W7. Jumper W1 to W2, skip to Step 2D.
   - C. Is SMI Oscillator Driven by an external source?
     If yes, jumper W2 to W3.
   - D. Is SMI to provide system power on reset?
     If yes, jumper W4 to W5.
   - E. Set Frequency Divider Switches
     Divide Oscillator Frequency by 1 set switches S2-5 Off, S2-6 Off
     Divide Oscillator Frequency by 2 set switches S2-5 On, S2-6 Off
     Divide Oscillator Frequency by 3 set switches S2-5 Off, S2-6 On
     Divide Oscillator Frequency by 4 set switches S2-5 On, S2-6 On
3. Programming X Pin Functions:
   - A. Is X0 Pin chip Select?
     If yes, program switch S1-1 Off.
     Is X0 Pin I/O Port?
     If yes, program switch S1-1 On.
   - B. Is X1 Pin chip Select?
     If yes, program switch S1-2 Off.

COMPONENT POSITIONING DIAGRAM

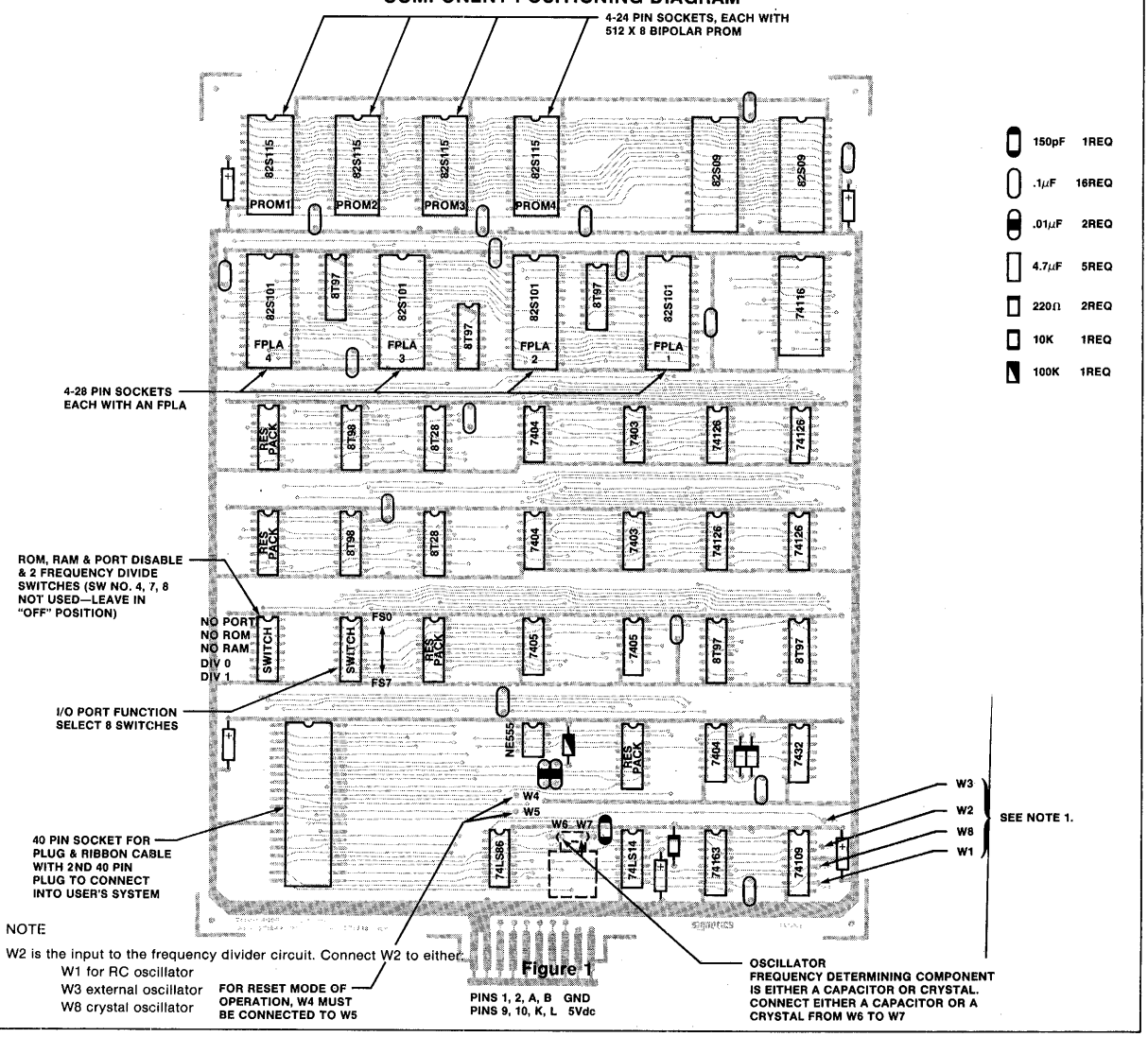


Figure 1

Is X1 Pin I/O Port?
If yes, program switch S1-2 On.

C. Is X2 Pin chip Select?
If yes, program switch S1-3 Off.
Is X2 Pin I/O Port?
If yes, program switch S1-3 On.

D. Is X3 Pin chip Select?
If yes, program switch S1-4 Off.
Is X3 Pin I/O Port?
If yes, program switch S1-4 On.

E. Is X4 Pin chip Select?
If yes, program switch S1-5 Off.
Is X4 Pin I/O Port?
If yes, program switch S1-5 On.

F. Is X5 Pin chip Select?
If yes, program switch S1-6 Off.
Is X5 Pin I/O Port?
If yes, program switch S1-6 On.

G. Is X6 Pin chip Select?
If yes, program switch S1-7 Off.
Is X6 Pin I/O Port?
If yes, program switch S1-7 On.

H. Is X7 Pin chip Select?
If yes, program switch S1-8 Off.
Is X7 Pin I/O Port?
If yes, program switch S1-8 On.

4. PROM Programming:

A. Develop Application Software
B. Program PROMS

5. Actual Use

A. Connect power to Edge Connector
B. Connect umbilical cable to socket of 2656 in system
C. Turn power on and debug system

PROGRAMMING

To program the PC-4000 the user must have available both FPLA programming equipment and PROM programming equipment. Equipment for programming the PROMs and FPLAs may be obtained from Data I/O Corporation, Curtis Electro Devices, and Signetics, among others. Normally, in defining the user's system hardware, the information needed to program the FPLAs, the Function Select Switches, the Clock and the Reset emerge from the system design. The following programming procedures are suggested for each of the programmable functions. The PGA in its FPLA implementation is considered first. It consists of:

- PGA input and output signal definitions. (See Table 1)
- System Address Map for coding the FPLAs
- FPLA Coding Forms

For detailed instructions on the programming procedures and equipment required for using FPLAs refer to "Signetics Field Programmable Logic Arrays," February 1976.

The Programmable Gate Array (PGA): The PGA decodes the X0 thru X7 chip select signals in FPLA 1 and FPLA 2. The memory chip enable signals are decoded in FPLA 3. The I/O port select signals are decoded in FPLA 3 and FPLA 4, and the Data Bus Control Signal in FPLA 4. The PGA has a minimum programming configuration as shown in the coding tables. (Reference: Coding Forms and Schematic Diagram)

System Address Map for Coding the FPLAs: The system address map is used in conjunction with the FPLA coding forms that follow. These two sets of documents provide the source information for direct transfer into the customer pattern selected for the Programmable Gate Array (PGA) of the 2656. (Note: The specifics of programming the punch card deck for all programmable functions of the 2656 are covered in the Signetics 2656 data sheet. See CUSTOM PATTERN PROGRAMMING INSTRUCTIONS)

FPLA Coding Forms: (Tables 2-6) Four coding forms are provided respectively for FPLAs #1, #2, #3, and #4. These forms show the minimum coding required to make the PC-4000 functional. When additional coding from the systems address map is inserted on the FPLA coding forms, the PGA of the PC-4000 is defined.

MNEMONIC	FPLA NO.	TYPE	FUNCTION
A0 to A14	—	I	Address Input
MEM	—	I	Memory or $\overline{I/O}$
OP	—	I	Operation Request
WRPB	—	I	Write Pulse
FS0 to FS7	—	I	Function Select for Pins X0 to X7
NOROMN	—	I	Disable the ROM Chip enables
NORAMN		I	Disable the RAM Chip enable
NOPORTN	—	I	Disable the I/O Port
1k2k	—	I	Sets the configuration of the ROM Memory to 2k (should be true for 2656 emulation)
READ	—	I	Read Signal
SELROM	—	I	Enable the Data Bus. A ROM operation has been selected.
PORT	—	I	The I/O Port operation has been selected.
RAMCEN	—	I	The RAM Chip enable.
PGA0 to PGA7	1,2	O	Chip Enable Decode for Pins X0 to X7
ROMCE0N	3	O	Chip Enable for ROM 0
ROMCE1N	3	O	Chip Enable for ROM 1
ROMCE2N	3	O	Chip Enable for ROM 2
ROMCE3N	3	O	Chip Enable for ROM 3
SELROM	3	O	ROM Operation has been selected
PORT	3,4	O	An I/O Operation has been selected
RAMCEN	3	O	Chip Enable for the RAM
RE	4	O	Enable the Data Bus Receiver
DE	4	O	Enable the Data Bus Driver
PWCN	4	O	Port Write Clock
REDPORTN	4	O	Enable the Port Read Driver to the Internal Data Bus.
REDRAMN	4	O	Turn on the RAM output Driver

NOTE

Signals ending in . . . N are active low.

OPTIONS

NORAM, NOROM, NOPORT disable the control signals for these functions. The Switch is on to disable these functions.

Table 1 PGA SIGNAL DESIGNATION

If the RAM, ROM and Port addresses are not programmed in the FPLAs (don't care all terms) the output signals will always be valid. The switch options along with the minimum programming of the FPLA prevent these signals from causing bus conflicts.

The symbols for the entries on the FPLA coding forms 1 through 4 (Tables 2-6) are:

Input Variable
H = Input High
L = Input Low
- = Don't Care
Blank = User Option

Output Function
A - Active
* - Not Present in Term

Active Level
H - Active High
L - Active Low

The tables that follow all use the standard coding format used for Signetics FPLAs. The format provides a matrix expression for logical expressions of the forms:

$$\text{Output Signals} = (I_1 \bullet I_2 \bullet I_3 \text{---} I_n)_1 + (I_1 \bullet I_2 \bullet I_3 \bullet \text{---} I_n)_2 + (I_1 \bullet I_2 \bullet I_3 \text{--} I_n)_k$$

Where:
n = 18 (for the 2656)
k = 1-4 depending upon the particular use
I_i = an input signal or its complement

Example:
The output function:

$$\overline{\text{Output}} = A \bullet B \bullet D + D \bullet \overline{A} + C \bullet \overline{B} \bullet E$$

would be shown in the table as:

PRELIMINARY SPECIFICATION

Signal Name or No.	INPUT VARIABLE A	B	C	D	E					OUTPUT FUNCTION					
	PRODUCT TERM									ACTIVE LEVEL					
											L				
										7	6	5			
00	-	-	-	-	-						*				
01	H	H	-	H	-						A				
02	L	-	-	H	-						A				
03	-	L	H	-	H						A				
04	H	H	H	-	-						*				

Asterisks indicate that these terms are not present in this output.

The minimum necessary fixed programming for a 2650 application is shown below:

DEVICE	MEMORY ADDRESS	I/O PORT ADDRESS	WRP	OP	M/IO	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
X0																				
X1																				
X2																				
X3																				
X4																				
X5																				
X6																				
X7																				
I/O Port																				
RAM					1									X	X	X	X	X	X	X
PROM					1					X	X	X	X	X	X	X	X	X	X	X

NOTE

Memory address and I/O Port address columns remain blank, unless X-pins are chip enables. The memory I/O columns for memory are programmed as "1" and for I/O are programmed as "0." For extended I/O operation A13 = 1, A12 thru A8 and A14 are programmed Don't Care and A7 thru A0 as I/O address. For non-extended I/O operation, there are two modes, data and control. For data A13 = 0, A14 = 1, A12 thru A0 are Don't Care. For control, A13 = 0, A14 = 0, A12 thru A0 are Don't Care.

Table 2 · SYSTEM ADDRESS MAP FOR CODING FPLA

PRELIMINARY SPECIFICATION

Signal Name or No.	INPUT VARIABLE																OUTPUT FUNCTION							
			FS3	FS2	FS1	FS0	A8	A7	A6	A5	A4	A3	A2	A1	A0		CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
	PRODUCT TERM																ACTIVE LEVEL							
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	H	H	H	H	H	H	H	H
																	7	6	5	4	3	2	1	0
00																	*	*	*	*	*	*	*	A
01																	*	*	*	*	*	*	A	*
02																	*	*	*	*	*	A	*	*
03																	*	*	*	*	A	*	*	*
04																	*	*	*	A	*	*	*	*
05																	*	*	A	*	*	*	*	*
06																	*	A	*	*	*	*	*	*
07																	A	*	*	*	*	*	*	*

Table 3 CODING TABLE FOR FPLA NO. 1

Signal Name or No.	INPUT VARIABLE																OUTPUT FUNCTION							
			FS7	FS6	FS5	FS4	WRP	OP	MEM	A14	A13	A12	A11	A10	A09		CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
	PRODUCT TERM																ACTIVE LEVEL							
				12	11	10	09	08	07	06	05	04	03	02	01	00	H	H	H	H	H	H	H	H
																	7	6	5	4	3	2	1	0
00																	*	*	*	*	*	*	*	A
01																	*	*	*	*	*	*	A	*
02																	*	*	*	*	*	A	*	*
03																	*	*	*	*	A	*	*	*
04							H										*	*	*	A	*	*	*	*
05						H											*	*	A	*	*	*	*	*
06					H												*	A	*	*	*	*	*	*
07				H													A	*	*	*	*	*	*	*

Table 4 CODING TABLE FOR FPLA NO. 2

PRELIMINARY SPECIFICATION

Signal Name or No.	INPUT VARIABLE: 1k2k	READ	NORAM	NOROM	WRP	OP	MEM	A14	A13	A12	A11	A10	A09	A08	A07	RAMCEN	OUTPUT FUNCTION: RAMCEN	PORT	SELROM	ROMCE3N	ROMCE2N	ROMCE1N	ROMCE0N
	PRODUCT TERM																ACTIVE LEVEL						
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	L	H	H	H	L	L	L	L
																	7	6	5	4	3	2	1	0
00	-	H	-	H	H	H	H					L	L	-	-	H	*	*	*	A	*	*	*	A
01	-	H	-	H	H	H	H					L	H	-	-	H	*	*	*	A	*	*	A	*
02	H	H	-	H	H	H	H					H	L	-	-	H	*	*	*	A	*	A	*	*
03	H	H	-	H	H	H	H					H	H	-	-	H	*	*	*	A	A	*	*	*
04	-	-	H	-	H	H	H									-	A	*	*	*	*	*	*	*
05	-	-	-	-												-	*	*	A	*	*	*	*	*

Table 5 CODING TABLE FOR FPLA NO. 3

Signal Name or No.	INPUT VARIABLE: NOPORT	RAMCEN	PORT	SELROM	READ	A6	A5	A4	A3	A2	A1	A0	OUTPUT FUNCTION: REDPORTN	PWCN	REDRAMN	DE	RE	PORT	
	PRODUCT TERM												ACTIVE LEVEL						
	11	10	09	08	07	06	05	04	03	02	01	00	L	L	L	H	L	H	
													7	6	5	4	3	2	1	0	
00	H	-	-	-	-								*	*	*	*	*	*	*	A	WRITE RAM
01	-	L	L	L	L	-	-	-	-	-	-	-	*	*	*	*	*	*	A	*	READ ROM
02	-	H	L	H	H	-	-	-	-	-	-	-	*	*	*	*	*	A	*	*	READ PORT
03	-	H	H	L	H	-	-	-	-	-	-	-	*	*	A	*	*	A	*	*	WRITE PORT
04	-	H	H	L	L	-	-	-	-	-	-	-	*	*	*	A	*	*	A	*	READ RAM
05	-	L	L	L	H	-	-	-	-	-	-	-	*	*	*	*	A	A	*	*	

Table 6 CODING TABLE FOR FPLA NO. 4

CODING SWITCHES AND JUMPERS: The switches and jumpers are set by the user for the particular application of the 2656 in his system. Purposes of the switches and jumpers are described in the functional block descriptions. Specifics of coding are given in 3 groups.

Tables 7, 8 and 9 show the switch positions and jumper connections for:

1. Memory and clock divider functions.
2. Select port or chip enable.
3. Jumpers

These tables, when properly filled-in, may be used as source data for the codes to be transferred into the 2656 coding forms.

Oscillator Frequency: output clock frequency equals oscillator frequency:

÷ 1 set S2-5 Off, S2-6 Off
÷ 2 set S2-5 On, S2-6 Off
÷ 3 set S2-5 Off, S2-6 On
÷ 4 set S2-5 On, S2-6 On

SWITCH	ON	OFF	FUNCTION
S2-2			NO ROM
S2-3			NO ROM
S2-1			NO I/O PORT
S2-4		x	1k/2k
S2-5			DIV0
S2-6			DIV1

Table 7 MEMORY AND CLOCK DIVIDER

SWITCH NO.	I/O PORT SWITCH ON	CHIP ENABLE SWITCH OFF	X PIN
S1-1			X0
S1-2			X1
S1-3			X2
S1-4			X3
S1-5			X4
S1-6			X5
S1-7			X6
S1-8			X7

Table 8 PORT OR CHIP ENABLE

	JUMPER	COMPONENT
XTAL OSC	W2 to W8	XTAL FROM W6 to W7
RC OSC	W1 to W2	CAPACITOR FROM W6 to W7
EXT DRIVEN RESET OUTPUT	W2 to W3 W4 to W5	

Table 9 JUMPERS AND ADDITIONAL COMPONENTS

40-Conductor Cable Pin-Out: The Interface from the PC-4000 to the users system is a 40-pin cable with 40-pin dip plugs on both ends.

NO.	MNEMONIC	STATE	OPERATION
SWITCHES			
S1-2	FS0	ON	Select X0 As I/O Port Bit
		OFF	Select X0 As Chip Select
S1-3	FS1	ON	Select X1 As I/O Port Bit
		OFF	Select X1 As Chip Select
S1-1	FS2	ON	Select X2 As I/O Port Bit
		OFF	Select X2 As Chip Select
S1-4	FS3	ON	Select X3 As I/O Port Bit
		OFF	Select X3 As Chip Select
S1-5	FS4	ON	Select X4 As I/O Port Bit
		OFF	Select X4 As Chip Select
S1-6	FS5	ON	Select X5 As I/O Port Bit
		OFF	Select X5 As Chip Select
S1-7	FS6	ON	Select X6 As I/O Port Bit
		OFF	Select X6 As Chip Select
S1-8	FS7	ON	Select X7 As I/O Port Bit
		OFF	Select X7 As Chip Select
S2-1	NOROM	ON	ROM Chip Selects Disabled
		OFF	ROM Chip Selects Enable
S2-2	NORAM	ON	RAM Chip Selects Disabled
		OFF	RAM Chip Selects Enable
S2-3	NOPORT	ON	Port Select Disabled
		OFF	Port Select Enabled
S2-4	1k2k	ON	ROMCE2N AND ROMCE3N Disabled
		OFF	ROMCE2N AND ROMCE3N Enabled
S2-5	CLKDIV0		
S2-6	CLKDIV1		
JUMPERS			
W2 to W8			Use Internal Xtal Oscillator
W1 to W2			Use Internal RC Oscillator
W2 to W3			CK2 Pin is External Clock Input
W4 to W5			CK1 is Reset Output

Table 10 SWITCH AND JUMPER SUMMARY

MNEMONIC	NO.	MNEMONIC	NO.
DBUS3	1	DBUS2	40
DBUS4	2	DBUS1	39
DBUS5	3	DBUS0	38
DBUS6	4	X3	37
DBUS7	5	X2	36
X7	6	X1	35
X6	7	X0	34
X5	8	NC[2]	33
X4	9	ADDR14	32
CLK OUT	10	ADDR13	31
CLK 1	11	ADDR12	30
CLK 2	12	ADDR11	29
VSS GND	13	ADDR10	28
R/W	14	ADDR9	27
M/I/O	15	ADDR8	26
OPREQ	16	ADDR7	25
WRP	17	ADDR6	24
ADDR0	18	ADDR5	23
ADDR1	19	ADDR4	22
ADDR2	20	ADDR3	21

Table 11 SMI CABLE PINOUTS[1]

NOTES

1. Timing element pins have alternate functions Clock 1 is external reset out. To use, connect W (4) to W (5). Clock 2 is external Clock in. To use, connect W (2) to W (3). Clock 2 not used: to use RC oscillator connect W (1) to W (2). To use internal XTAL oscillator connect W (2) to W (8).
2. V_{DD} for chip, no connect for board.

SMI PROTOTYPING CARD LOGIC DIAGRAM PART 1

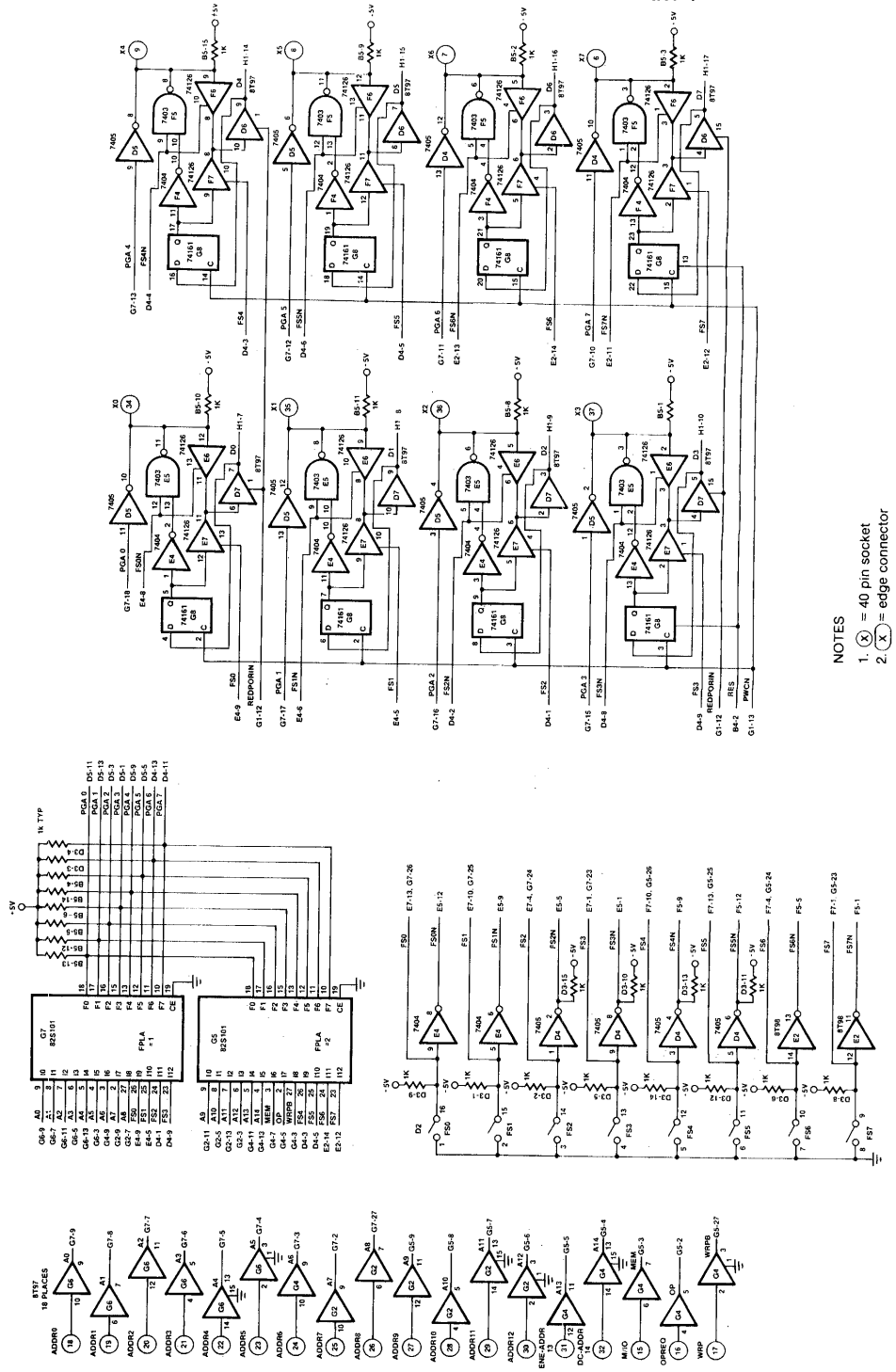


Figure 2

SMI PROTOTYPING CARD LOGIC DIAGRAM PART 2

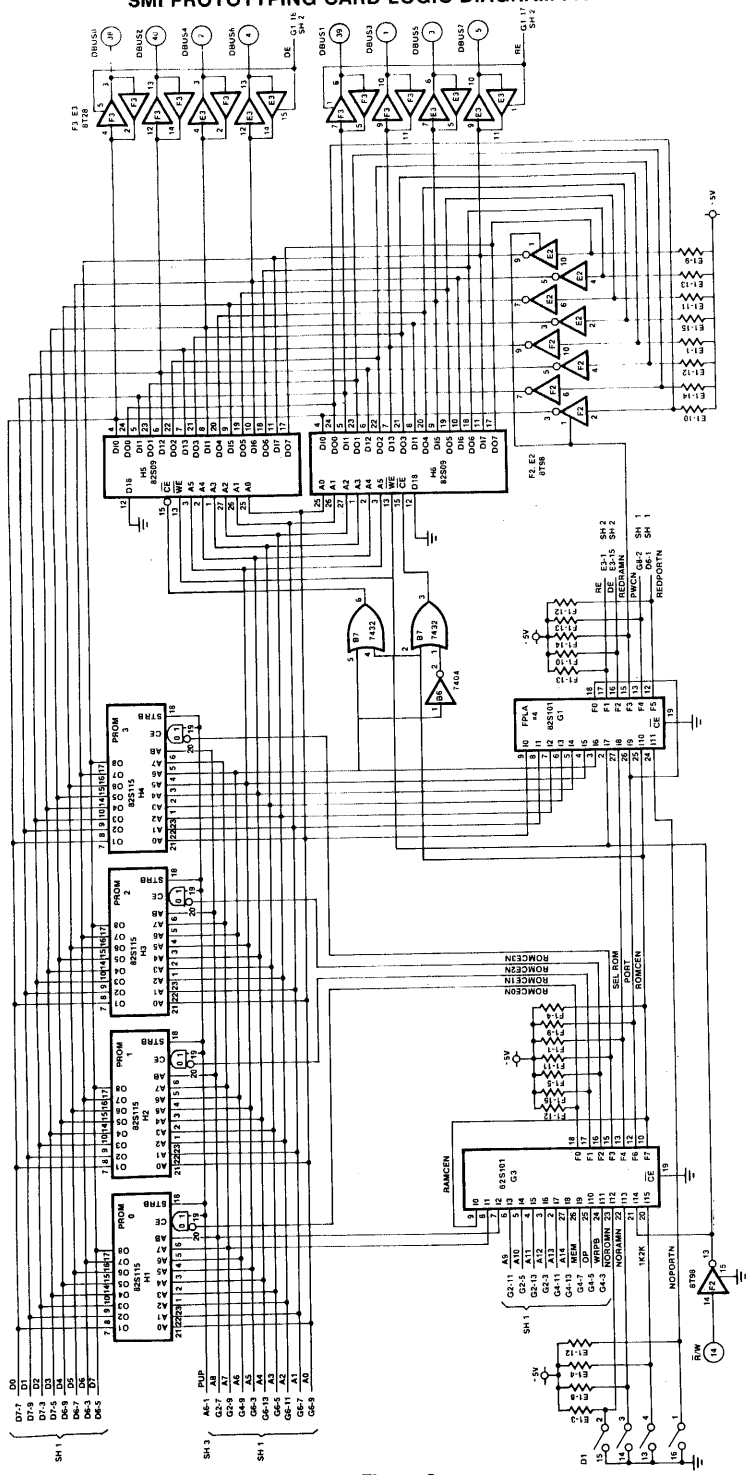
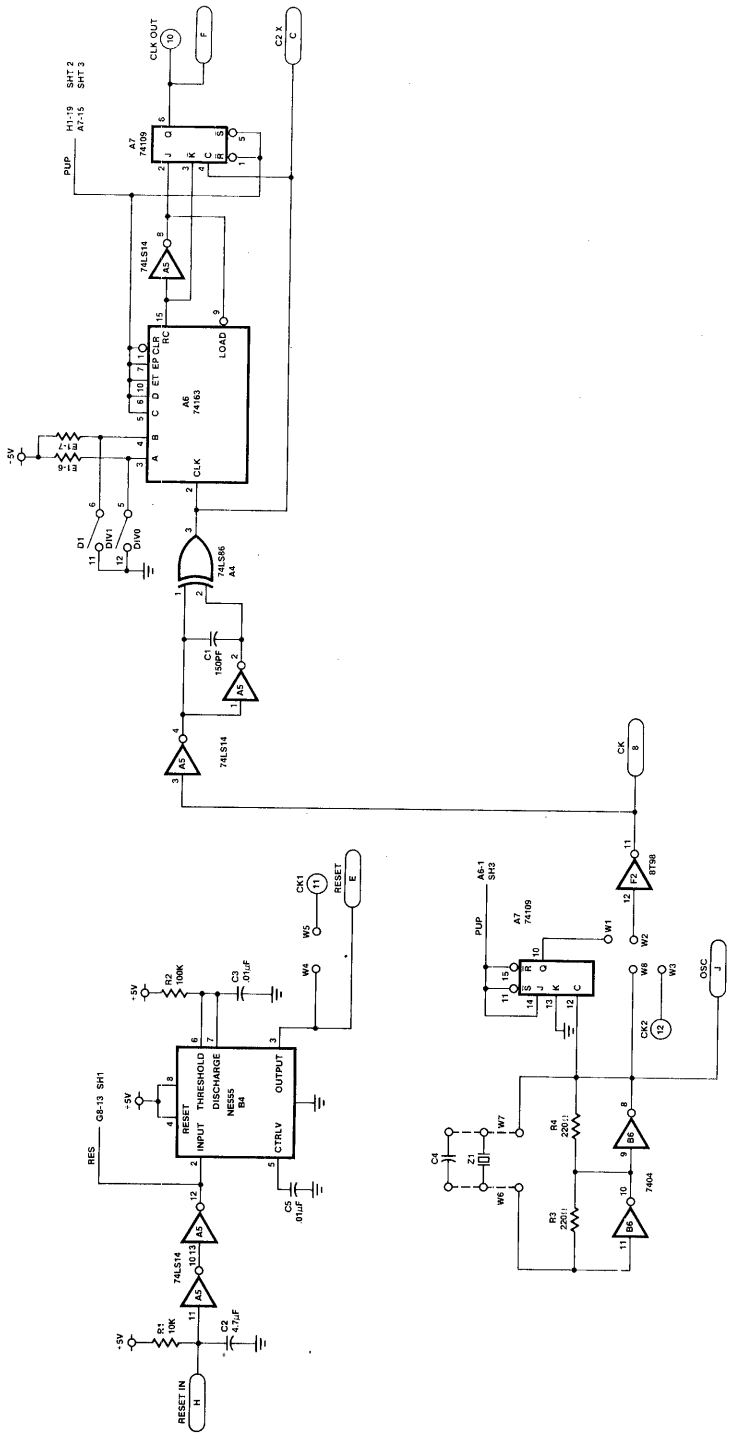


Figure 3

SMI PROTOTYPING CARD LOGIC DIAGRAM PART 3



POWER AND GROUND TABLE

IC	PART	VCC	GND
A4	74LS86	14	7
A5	74LS14	14	7
A6	74163	16	8
A7	74109	16	8
B4	NE555	8	1
B6,E4,F4	7404	14	7
B7	7432	14	7
D4,D5	7405	14	7
D6,D2,G2,G6,G4	8T97	16	8
E2,F2	8T98	16	8
E3,F3	8T28	16	8
E5,F5	7403	14	7
E6,E7,F6,F7	74126	14	7
G1,G3,G5,G7	825101	28	14
G8	74116	24	12
H1,H2,H3,H4	825115	24	12
H5,H6	82509	28	14
B5,D3,E1,F1	RES PACK	16	—

Figure 4

PRELIMINARY SPECIFICATION

EDGE CONNECTOR

The edge connector for the 2650/PC-4000 is an AMP 225-21021-4-01-117 edge connector. This edge connector has 20 pins on 0.156 inch centers.

EDGE CONNECTOR PIN-OUT

GND	1	A	GND
GND	2	B	GND
	3	C	C2X
	4	D	
	5	E	RESET OUT*
	6	F	CLK OUT*
	7	H	RESET IN*
CK	8	J	OSC
Vcc	9	K	Vcc
Vcc	10	L	Vcc

*Factory Test Only Do not Use

Figure 5

SHIPPING CONFIGURATION

Included with the PC-4000:
Blank 82S115 PROMS 4 Each.
Blank 82S101 FPLAS 4 Each.
Edge Connector
2-foot cable with 40 pin headers on each end.
PC-4000 Data Sheet

REQUIRED BUT NOT SUPPLIED

Timing element for oscillator

PART NUMBER	QUANTITY	DESCRIPTION
7403	2	Open Collector Quad Nand
7404	3	Hex Inverter
7405	2	Open Collector Hex Inverter
74LS14	1	Hex Schmitt Trigger Inverter
7432	1	Quad 2 Input or Gate
74LS86	1	Quad 2 Input XOR
74109	1	Dual JK Flop
74116	1	Dual Quad D Latch with Clear
74126	4	Quad Tristate Buffer
74163	1	4 Bit Binary Counter
8T28B	2	Bidirectional Data Bus Driver Receiver
8T97B	5	Tristate Hex Buffer
8T98B	2	Tristate Hex Inverter Buffer
82S101	4	Open Collector FPLA
82S115	4	512X8 PROM
82S09	2	64X9 BIPOLAR RAM
NE555	1	Timer
761-1-51.0KOHM	4	Resistor Dip Pak
	1	10k OHM Resistor
	1	100k OHM Resistor
	2	220 OHM Resistor
		Note: All Resistors 1/4 Watt
	1	150pF Capacitor
	2	0.01μF Capacitor
	5	4.7μF Capacitor
	14	0.1μF Capacitor
XTAL or Capacitor	1	Timing Element for Oscillator (Not Supplied)
	1	Edge Connector AMP 225-21021-401-117
	2	8 Position Dip Switch
	1	PC Board 2650/PC-4000
	4	24 Pin Dip Socket
	4	28 Pin Dip Socket
	1	40 Pin Dip Socket
	1	Cable Assembly

Table 12 PARTS LIST

DESCRIPTION

The 2650PC1001 is a complete microcomputer on a single printed circuit board. The heart of this computer is Signetics' 2650 Microprocessor; a single chip, N-Channel MOS Integrated Circuit which contains the CPU and control sections of the classical general purpose computer architecture.

In addition to the Microprocessor, the 2650PC1001 contains both control and read/write memory, I/O ports, clock, and all the necessary buffering and interface circuits to permit data transfer both on and off the p.c.b.

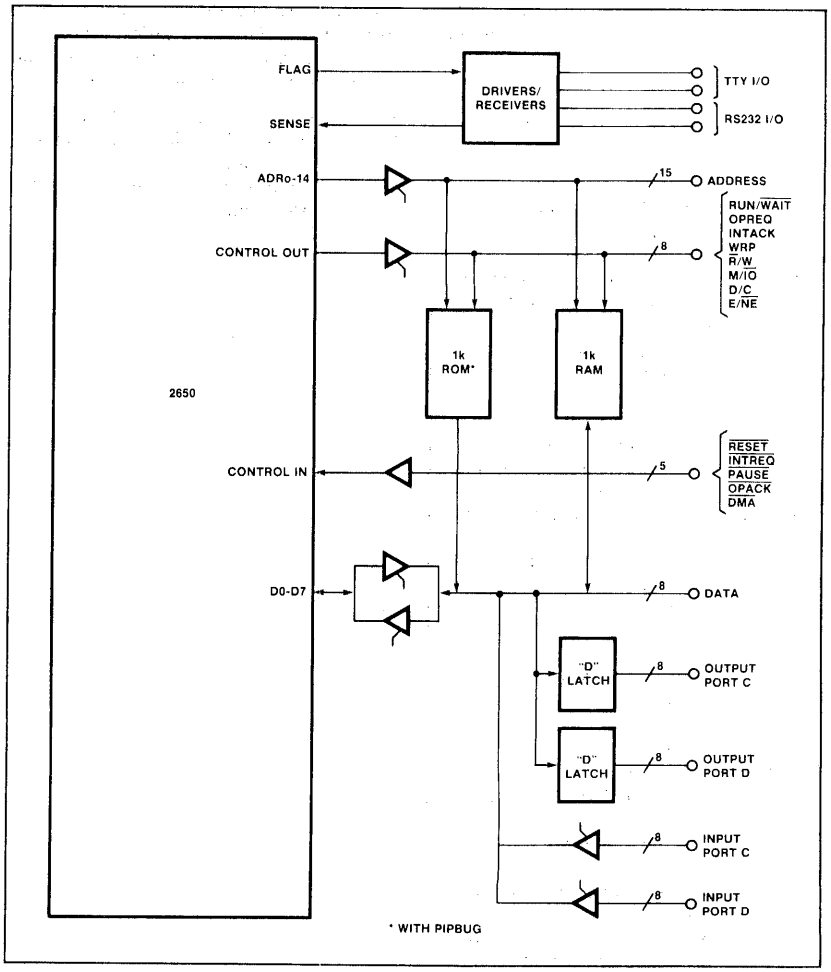
FEATURES

- **2650 Microprocessor**
- **1K bytes of ROM with PIPBUG***
- **1K bytes of RAM (off-board expandable)**
- **1MHz crystal oscillator**
- **Serial I/O (either TTY 20mA current loop or RS232—selectable by jumper wire)**
- **Two 8-bit output ports**
- **Two 8-bit input ports**
- **DMA capability**
- **LED display indicators**
- **Data bus and address bus test points**
- **Buffered data and address outputs**
- **Single power supply (+5 volts)****

*Signetics Loader and Debugging Program. (See appl. note SS50)

**Assumes RS232 I/O port is not used.

BLOCK DIAGRAM



MEMORY

The memory of the 2650PC1001 is divided into two segments:

a. ROM with PIPBUG
b. RAM (Read/Write Memory)

The Read-Only Memory (ROM) supplied with the card is the Signetics' 82S129 Field Programmable type (PROM). Eight of these 256X4 devices are arranged to provide a 1KX8 memory array. The 2650PC1001 is supplied with the PIPBUG loader and debugger already programmed into the ROM. Since the devices are loaded into sockets, however, they can be easily replaced with other ROMs or PROMs programmed by the user.

The 1KX8 array is constructed with Signetics' 2606 NMOS RAM devices. Since the 2606 is a 256X4 device, again 8 devices are used in the array.

SERIAL I/O

The serial I/O capability of the 2650PC1001 utilizes a unique serial I/O feature of the basic 2650 microprocessor. This feature allows serial data to be transferred directly into the 2650 under program control by using the sense and flag pins on the microprocessor.

Two types of serial I/O ports are available. The first is a teletype interface which can be directly connected to a teletype 20mA current loop. The second is an RS232 interface which provides a connection for voltage driven peripheral equipment. The selection of the particular interface to be used is made by connecting a jumper wire directly from the microprocessor flag and sense lines to the appropriate output port. If the RS232 interface is used, +12 and -12 volt supplies are required in addition to the +5 volt supply which operates the rest of the board.

PARALLEL I/O

Parallel I/O channels using the 2650's unique Non-Extended I/O mode are also provided. This mode allows a single byte instruction to select one of two distinct I/O devices. On the 2650PC1001, these two devices are represented by four separate data channels; two for reading and two for writing. The output (or write) channels are fully latched and buffered. The input (or read) channels are fully buffered. One read and one write channel represents a single I/O device. In addition to the Non-Extended I/O ports, the data and address buses, plus the appropriate control signals, are also available to provide the full extended I/O capability.

OTHER I/O

A complete listing of the I/O pins, plus a brief description of any I/O signal not detailed above, is as follows:

PIN	DESCRIPTION
1,2	Ground
4-11	*Processor Data Bus*
12	Strobe to Enable Input Data Port
13	*D/C* Output
14	DMA Control Input
15	*Extended/Non-Extended* Output
16	*Interrupt Acknowledge* Output
17	*R/W* Output
18	*Write Pulse* Output
19	*Run/Wait* Output
20	*Operation Request* Output
21	*Memory/IO* Output
22	*Operation Acknowledge* Input
23	Clock Output (or Input if on-board clock not used)
24	Operation Request Input for DMA
25	*Reset* Input
26	*Interrupt Request* Input
27	*Pause* Input
28-32	Unused
33-47	*Address Bus*
48	+12 Volts for RS232
49	-12 Volts for RS232
50	+5 Volts
A,B	Ground
C	Not used
D-M	Non-Extended Output Port "D"
N	Clock to load data into Output Port "D"
P	TTY serial data input (+)
R	TTY serial data input (-)
S	TTY serial data Output pull up resistor (current loop +)
T	TTY serial data Output; TTL Level, open collector (current loop return)
U	RS232 ground
V	RS232 Output
W	TTY tape reader Output; TTL Level, open collector (+)
X	TTY tape reader Output pull up resistor (-)
Y	RS232 Input
Z	Clock to load data into Output Port "C"
a-h	Non-Extended Output Port "C"
j	Strobe to enable input Port Control
k-u	Non-Extended Input Port "D"
v-c	Non-Extended Input Port "C"
d	+12 for RS232
e	-12 for RS232
f	+5 Volts

NOTE
Italic items indicate buffered 2650 Microprocessor Outputs.

SUMMARY

The above is intended to provide a brief description of Signetics' 2650PC1001 Prototyping Board. More detailed information can be obtained from the following:

M20 PIPBUG Application Note
M14 2650PC1001 Manual (Detailed Description)
M1 Serial I/O using Sense and Flag Application Note

DESCRIPTION

The 2650 PC2000 is a 4K Memory Card designed to be compatible with the 2650 microprocessor. It is composed of 32, 21L02 NMOS, 1K by 1 bit static RAMs, and organized in four groups of one kilo-byte each. Decoding is provided to select one of the four groups and also distinguish the card in multi-card configurations. In a system application utilizing up to 8 cards (32K), each card is uniquely identified by hardwired jumpers. No external decoding is required.

The decoding logic is sectioned into two blocks. The first block determines if the address identifies that card as being part of the 8K page address. (The 2650 memory scheme is organized into 4 pages of 8K each.) The second block uniquely locates 1K bytes of memory on the board in the 8K bytes of memory of the selected page. Each 1K bank is individually selected by hardwired jumpers to the decoder.

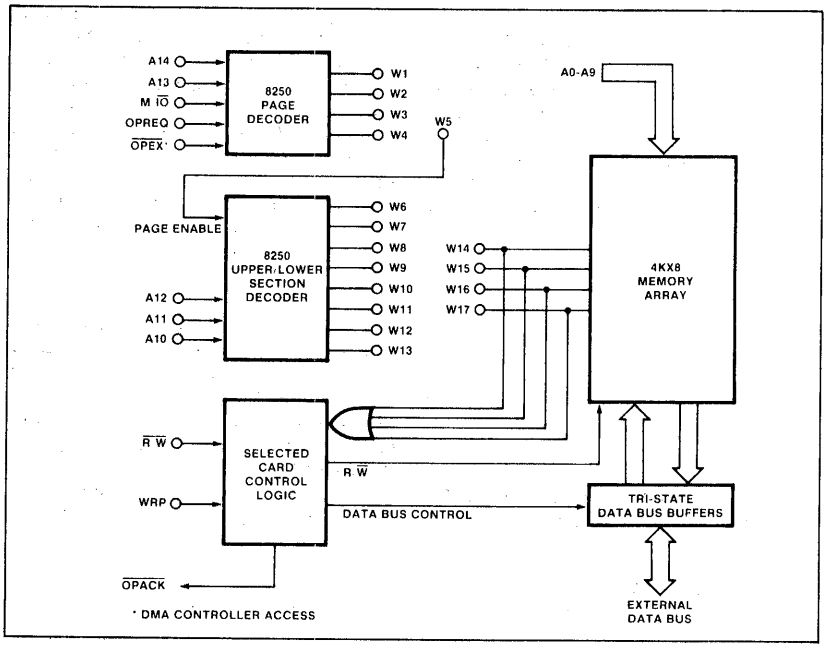
FEATURES

- **Requires only single +5V supply**
- **Industry standard 21L02 memories**
- **Fully decoded for 32K memory organization**
- **Data bus buffered with tri-state drivers/receivers**
- **Accessible from microprocessor or DMA controller**
- **TTL compatible**
- **Dimensions are 8" X 6.875" with a 50 pin edge connector along the 8" dimension**
- **Typical power consumption of 4.5 watts**

SIGNAL DEFINITION

Memory control signals and address lines between the 2650 microprocessor and the 2650 PC2000 are indicated in the block diagram. The $\overline{OPEX}$ control line is reserved for use with DMA controllers. Its function is similar to that of the OPREQ line from the 2650. When either of these lines are true and a memory operation is specified ($M/\overline{IO}$ = High) the memory card is enabled to decode address lines A0 through A14. When a bank is selected, the selected card control logic block allows the read-write line ($\overline{R}/W$) and write pulse (WRP) to pass to the memory array and also enable the external data bus drivers. When the operation is complete the memory card responds with a true condition on $\overline{OPACK}$.

BLOCK DIAGRAM



JUMPER ADDRESS DECODING

Jumpers are applied to designated plated-through holes identified by a 'Wn' mnemonic. To identify the card to be part of a particular page, jumper point W5 to one of the following:

W1 for page 0
W2 for page 1
W3 for page 2
W4 for page 4

To locate each of the 1K bytes of the memory card in the selected memory page, four bank jumpers are required. The outputs of the decoder used to select one of eight 1K byte memory segments (W6-W13) must be connected to the selected 1K bytes of memory on the 2650 PC2000 (W14-W17).

Factory installed jumpers allow for immediate hook-up to a Demo System (DS1000/2000) which has 2K of memory. These jumpers have been hooked-up as follows:

W1 to W5 (page 0)
W8 to W14
W9 to W15
W10 to W16
W11 to W17

PIN	NAME	PIN	NAME
1,2,A,B	GROUND	34	ABUS13
4	$\overline{DBUS0}$	35	ABUS12
5	$\overline{DBUS1}$	36	ABUS14
6	$\overline{DBUS2}$	37	ABUS9
7	$\overline{DBUS3}$	38	ABUS10
8	$\overline{DBUS4}$	39	ABUS8
9	$\overline{DBUS5}$	40	ABUS7
10	$\overline{DBUS6}$	41	ABUS6
11	$\overline{DBUS7}$	42	ABUS5
17	$\overline{R}/W$	43	ABUS3
18	WRP	44	ABUS0
20	OPREQ	45	ABUS1
21	$M/\overline{IO}$	46	ABUS4
22	$\overline{OPACK}$	47	ABUS2
24	$\overline{OPEX}$	50,f	Vcc +5V
33	ABUS11		

Table 1 EDGE CONNECTOR TABLE

DESCRIPTION

The Demo System 2000 (2650 DS2000) is a hardware base for use with the 2650 CPU printed circuit board (PC1001) and allows the exercising of this card with user defined options. When the DS2000 is combined with a CPU board (PC1001) and a TTY, the user is equipped with everything he needs to exercise any of the software or hardware features of the 2650. The DS2000 has a built in power supply.

FEATURES

- **User defined expansion capability from connector supplying address, data and control lines.**
- **RS232 and TTY interface**
- **Two extended and two non-extended I/O ports**
- **Single step capability for program debugging**
- **Display of address bus, data bus and the two non-extended I/O ports**

CONNECTORS

The 2650 CPU Board (PC1001) is inserted into the J8 connector to complete the demo system. The user printed circuit board is inserted into the J7 connector. Both connectors are the same type (100 Pin Amphenol, series 225) and the numbered pins of J7 and J8 have the same signals (except pin 12). The lettered pins of J7 (pins A through $\bar{g}$) are not used. The sockets and connectors of the DS2000 and their associated signals are provided in this data sheet.

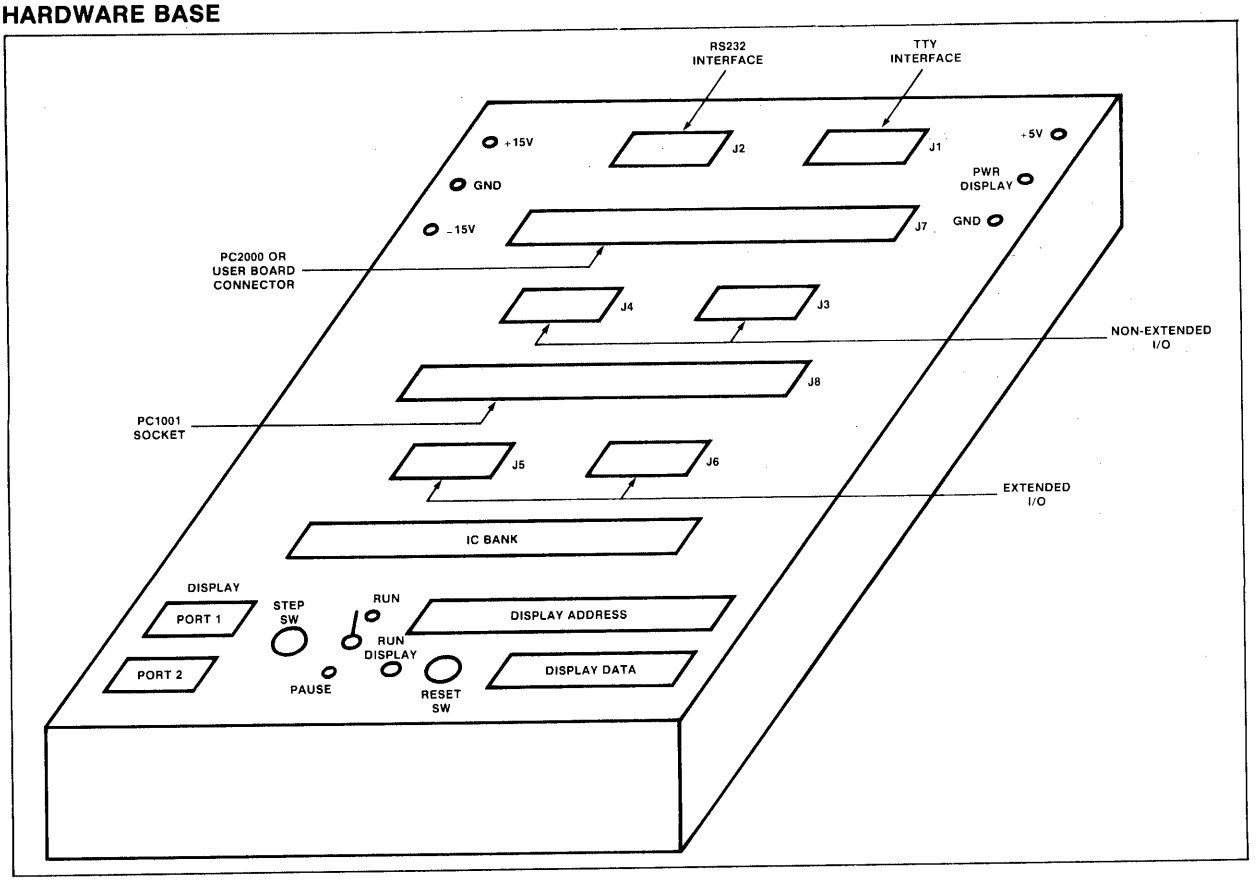
DISPLAYS

The address and data bus LED displays reeach OPREQ (beginning of an external operation). Latches store the information until another OPREQ is received. The two non-extended port displays represent data on channel C (port 2) and channel D (port 1) during the OPREQ for each I/O operation. A logic one one these displays will turn "on" the LED and a logic zero will turn them "off."

CONTROLS

The pause and step logic allows one instruction to be executed at a time by pushing the 'step' button when the Run/Pause switch is in the pause position. In this mode the Run/Wait display LED will go off. The reset switch will reset the display latches and place all zeros in the 2650 instruction address register.

HARDWARE BASE



SIGNAL NAMES FOR CONNECTORS 17 AND 18

PIN NO.	FUNCTION (J7 & J8)	PIN NO.	FUNCTION (J8 ONLY)[1]
1	GND	A	GND
2	GND	B	GND
3	NC[2]	C	NC
4	$\overline{\text{DBUS0}}$	D	OPD0
5	$\overline{\text{DBUS1}}$	E	OPD1
6	$\overline{\text{DBUS2}}$	F	OPD2
7	$\overline{\text{DBUS3}}$	H	OPD3
8	$\overline{\text{DBUS4}}$	J	OPD4
9	$\overline{\text{DBUS5}}$	K	OPD5
10	$\overline{\text{DBUS6}}$	L	OPD6
11	$\overline{\text{DBUS7}}$	M	OPD7
12[1]	EIPD	N	COPD
13	D/$\overline{\text{C}}$	P	TTY SERIAL IN +
14	$\overline{\text{DMA}}$	R	TTY SERIAL IN -
15	E/$\overline{\text{NE}}$	S	TTY SERIAL OUT +
16	INTACK	T	TTY SERIAL OUT -
17	$\overline{\text{R}}$/W	U	RS232 GROUND
18	$\overline{\text{WRP}}$	V	RS232 OUTPUT
19	RUN/$\overline{\text{WAIT}}$	W	TTY TAPE READER OUT +
20	OPREQ	X	TTY TAPE READER OUT -
21	M/$\overline{\text{IO}}$	Y	RS232 INPUT
22	$\overline{\text{OPACK}}$	Z	COPC
23	CLOCK	a	OPC0
24	$\overline{\text{OPEX}}$	b	OPC1
25	$\overline{\text{RESET}}$	c	OPC2
26	$\overline{\text{INTREQ}}$	d	OPC3
27	$\overline{\text{PAUSE}}$	e	OPC4
28	NC	f	OPC5
29	NC	g	OPC6
30	NC	h	OPC7
31	NC	j	EIPC
32	NC	k	IPD0
33	ABUS11	m	IPD1
34	ABUS13	n	IPD2
35	ABUS12	p	IPD3
36	ABUS14	r	IPD4
37	ABUS9	s	IPD5
38	ABUS10	t	IPD6
39	ABUS8	u	IPD7
40	ABUS7	r	IPC0
41	ABUS6	w	IPC1
42	ABUS5	x	IPC2
43	ABUS3	y	IPC3
44	ABUS0	z	IPC4
45	ABUS1	a	IPC5
46	ABUS4	b	IPC6
47	ABUS2	c	IPC7
48	+12V	d	+12V
49	-12V	e	-12V
50	+5V	g	+5V

NOTES

1. J7 has no connections to these pins.
2. NC = no connection.

EXTENDED INPUT/OUTPUT DIP SOCKETS

PIN NO.	FUNCTION J5	FUNCTION J6
1	$\overline{\text{DBUS0}}$	ABUS0
2	$\overline{\text{DBUS1}}$	ABUS1
3	$\overline{\text{DBUS2}}$	ABUS2
4	$\overline{\text{DBUS3}}$	ABUS3
5	$\overline{\text{DBUS4}}$	ABUS4
6	$\overline{\text{DBUS5}}$	ABUS5
7	$\overline{\text{DBUS6}}$	ABUS6
8	$\overline{\text{DBUS7}}$	ABUS7
9	$\overline{\text{OPACK}}$	ABUS8
10	M/$\overline{\text{IO}}$	ABUS9
11	$\overline{\text{OPREQ}}$	ABUS10
12	RUN/$\overline{\text{WAIT}}$	ABUS11
13	WRP	ABUS12
14	$\overline{\text{R}}$/W	ABUS13
15	INTACK	ABUS14
16	E/$\overline{\text{NE}}$	$\overline{\text{PAUSE}}$
17	$\overline{\text{DMA}}$	$\overline{\text{INTREQ}}$
18	D/$\overline{\text{C}}$	CLOCK

NON-EXTENDED INPUT/OUTPUT DIP SOCKETS

PIN NO.	FUNCTION J3		FUNCTION J4	
1	(Output Port C)	0	(Output Port D)	0
2	OPC	1	OPD	1
3	OPC	2	OPD	2
4	OPC	3	OPD	3
5	OPC	4	OPD	4
6	OPC	5	OPD	5
7	OPC	6	OPD	6
8	OPC	7	OPD	7
9	Clock Output Port	C	Clock Output Port	D
10	Enable Input Port	C	Enable Input Port	D
11	(Input Port C)	7	(Input Port D)	7
12	IPC	6	IPC	6
13	IPC	5	IPC	5
14	IPC	4	IPC	4
15	IPC	3	IPC	3
16	IPC	2	IPC	2
17	IPC	1	IPC	1
18	IPC	0	IPC	0

DESCRIPTION

The 2650 PC3000 is a basic text generating system requiring only six integrated circuits including one 2650 microprocessor. The serial communication link between the 2650 and the users terminal is accomplished with the flag and sense lines on the microprocessor. The 2650 PC3000 is used to control the storage of characters entered from a terminal with either a current loop or voltage swing capability (±7.5V min).

Control Characters allow the text to be printed out on the terminal with the capability for inserting unique characters at locations identified during text generation. When the text is printed out the entire text will be output unless a control character is detected. The microprocessor then stops the print-out and the operator enters the desired unique information. Another control character is then given to continue printing the text until all characters stored in memory are printed, or until another stop character is detected. The stop character is recorded in memory just like any other character; however, it is not printed during text print-out.

Additional control characters allow for the erasure of the previous character typed or the erasure of the entire memory.

FEATURES

- **Total of six IC packages**
- **Operates at +5V at a max of 500mA**
- **Interface to either current loop or device capable of sending and receiving a minimum voltage swing of ±7.5 volts referenced to signal ground**
- **250 character storage capability**
- **Card size less than 3" X 4" with four screwed-on stand-offs at corners**
- **1MHz clock implemented with 74123 oneshot**
- **Variable baud rate between 110 and 300 baud by trimmer pot adjustment of clock**
- **PROM mounted in 24 pin socket**
- **Card edge connector supplied with each card**
- **Inputs provided for an external system reset**

TERMINAL INTERFACE

Voltage Mode Terminal Connection

The voltage mode interface is very similar to the standard RS232 interface except that the "signal" ground cannot be connected to "protective" ground. When a Cinch type 25-pin connector (DB25P or DB25S) is used on an RS232 compatible terminal, the PC3000 should be connected as shown in Table 1.

Current Loop Terminal Connection

When a terminal is used that employs current loop transmission techniques the four wires from the terminal should be connected to the corresponding four pins on the PC3000 card: TTY OUT +, TTY OUT –, TTY IN +, and TTY IN –.

On card jumper point 'A' to 'B' and point 'D' to 'F.'

PC3000 COMMAND SUMMARY

KEY	FUNCTION
Rubout (delete)	Erase last character in memory and echo the erased character. Additional preceding characters can be erased by continuing to depress the delete key.
Control and E	Erase entire memory.
Control and B	Used to indicate beginning of inserted message. Is not printed but stored in memory. Stops print-out when read from memory. Required once from each unique information entry.
Control and C	Continues print-out of memory after entry of unique information.
Control and P	Prints out contents of terminal memory.
Control and R	Software reset.

NOTE

Bell will ring if any of the following are true.

1. Entering more than 250 characters in memory.
2. Requesting print-out of an empty buffer.
3. Attempting to delete more characters than there are in memory.

DB25P (DB25S) PIN NO.	PC3000 EDGE CONNECTOR PIN NO.	PC3000 SIGNAL NAME
1	No connection	—
3	6	VS OUT +
2	J	VS IN +
7	K	VS OUT—(Signal GND)
5,6,8,20	Connect Together	—

On card jumper point 'A' to 'C' and point 'D' to 'E.'

Table 1 VOLTAGE MODE TERMINAL PIN DESCRIPTION

PART DESCRIPTIONS

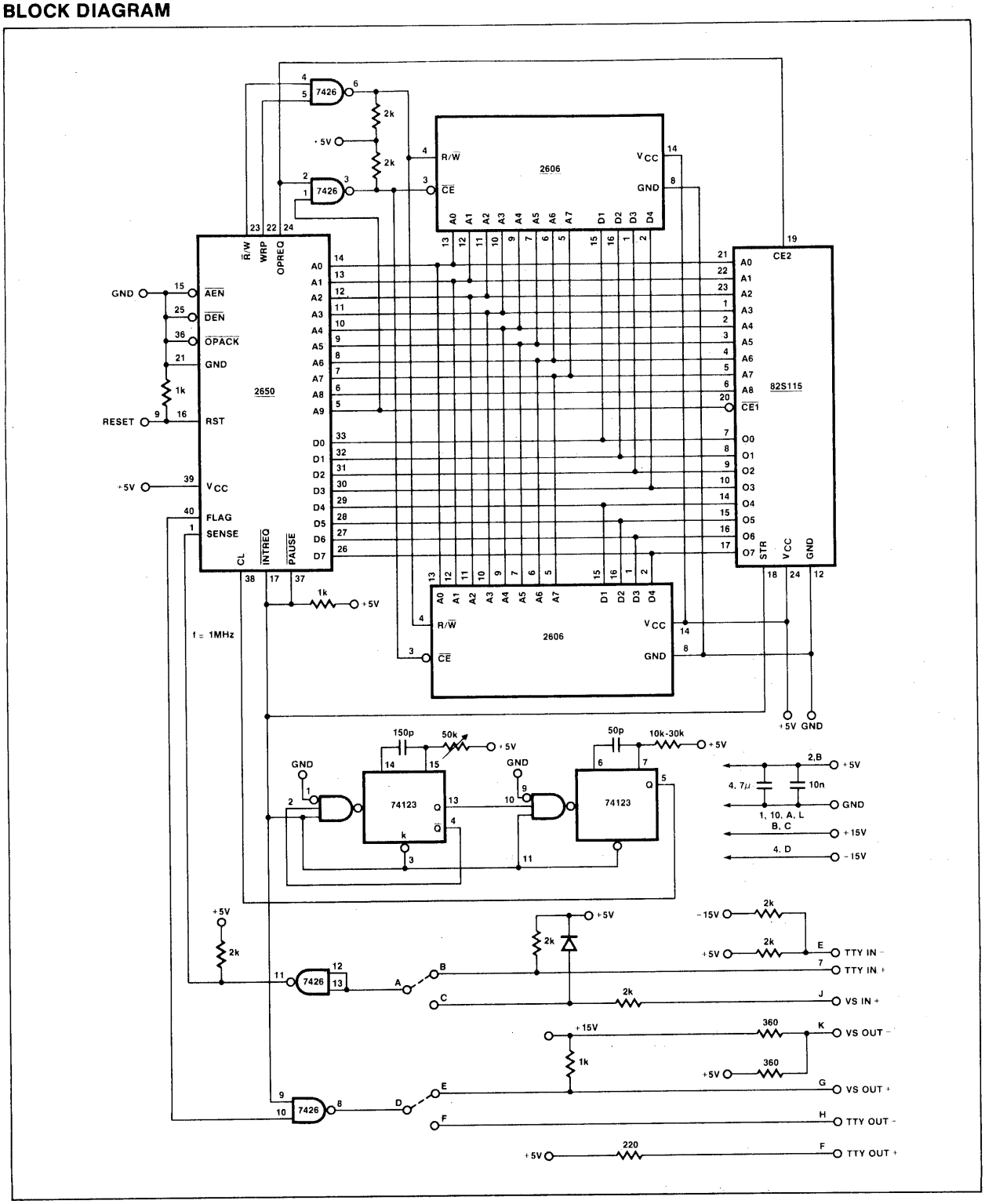
PART	FUNCTION
2650	8-bit TTL compatible N-Channel Microprocessor incorporating a serial I/O Port. (See 2650 Hardware Specification Manual for complete description—2650 BM1000.)
2606	1024-bit static MOS, TTL compatible RAM memory organized as 256 words by 4 bits/word.
82S115	4096-bit Bipolar TTL compatible PROM organized as 512 words by 8 bits/word.
N7426	Quad 2-input high voltage NAND gate with open collector capable of driving voltage and current loop interfaces (20mA maximum).
74123	Dual retriggerable monostable multivibrator with clear configured as a clock for 2650.
Potentiometer	Hellpot series 91C, 50K, ohm 3/8" cermet trimming potentiometer.
PC Edge Connector	Ampnenol—225-21021-401-117 Cinch—251-10-30-160

Miscellaneous components consist of 11 (1/4) watt and two (1/2) watt resistors, and two mica, one ceramic and one tantilum capacitor.

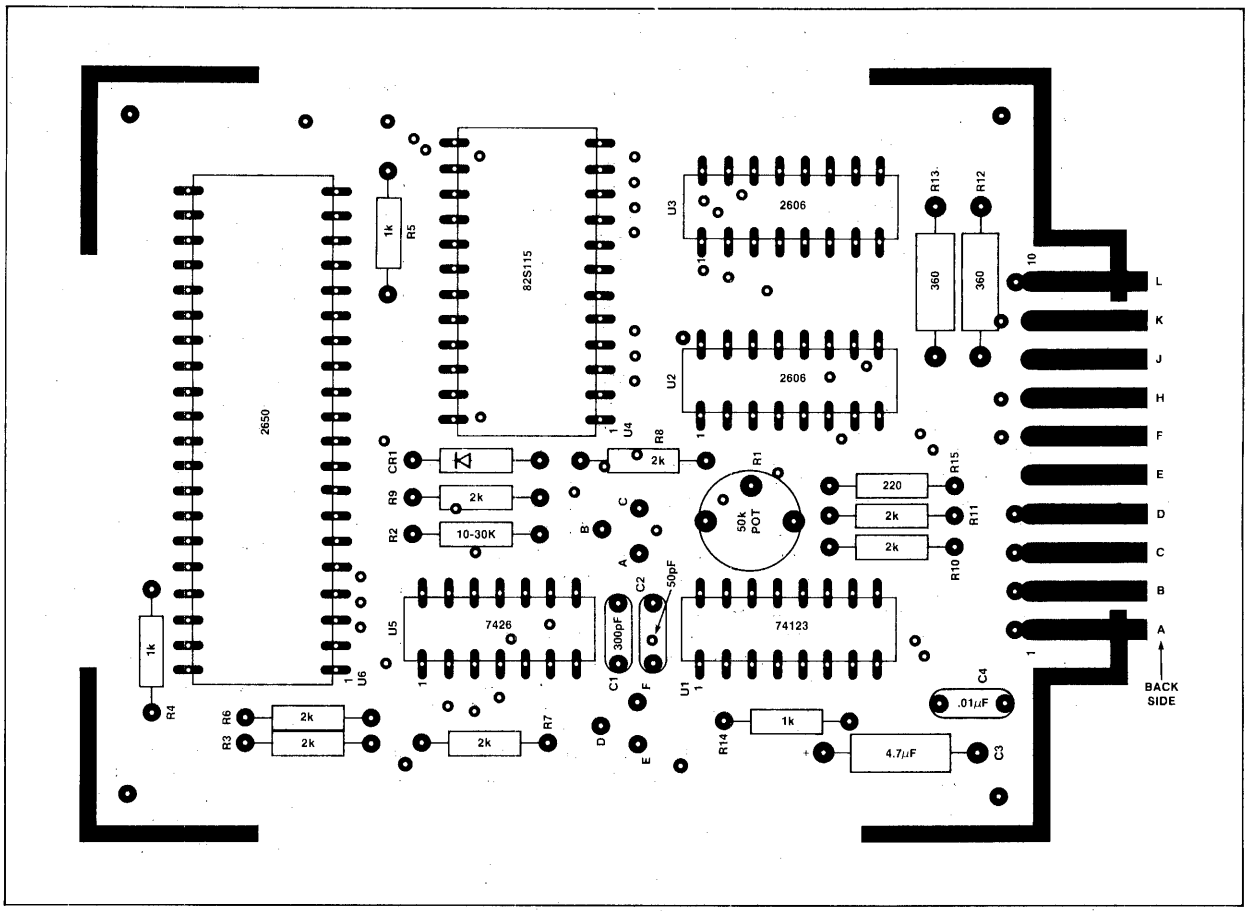
The following are required to make the board functional but are not supplied with the card:

RS232 type connector for voltage swing interface: DB25P or DB25S
Reset switch—(normally open, connected to +5V)
Power supplies: +5V
±15V

BLOCK DIAGRAM



BOARD LAYOUT



PC3000 CONNECTOR PIN ASSIGNMENT

PIN	FUNCTION	PIN	FUNCTION
1	GND	A	GND
2	+5	B	+5
3	+15	C	+15V
4	-15	D	-15
5	—	E	TTY IN -
6	VS OUT +	F	TTY OUT +
7	TTY IN +	H	TTY OUT -
8	—	J	VS IN +
9	RESET	K	VS OUT - (Signal Ground)
10	GND	L	GND
VS-	Voltage Swing		

2

DESCRIPTION

The 2650 assembly language (PIPHASM) is a symbolic language designed specifically to facilitate the writing of programs for the Signetics 2650 microprocessor.

The AS1000 is configured to operate on 32-bit or larger machines and the AS1100 is configured to operate on 16-bit machines.

The 2650 assembler is a program which accepts symbolic source code as input and produces a listing and/or an object module "Hexadecimal" format compatible to the two tape punching programs PIPHTAP (for acceptance by PIPBUG), PIPSTAP (for PROMs) and also to the simulator, PIPSIM.

The assembler is written in standard Fortran IV and is approximately 1,250 Fortran card images in length. It is modular and may be executed in an overlay mode should memory restrictions make that necessary. It operates in a two pass mode to build a symbol table, to issue helpful error messages, produce an easily readable program listing and output a computer readable object module. This version of the assembler compiles into a 12K word load module on the PDP-11/40 (16-bit words) and executes under DOS (8K) within a 28K memory.

AVAILABILITY

The 2650 assembler is available on both NCSS and GE timeshare. It is also available from Signetics on 9 track magnetic tape written in EBCDIC in 80 character unblocked records at a density of 800 bpi.

FEATURES

- **Forward references**
- **Pseudo-Ops to aid programming**
- **Self-defining constants**
- **Symbolic machine operation codes**
- **Free format source code**
- **Syntax error checking**
- **Symbolic address assignment and references**
- **Data creation statements**
- **Storage reservation statements**
- **Assembly listing control statements**
- **Addresses can be generated as constants**
- **Character codes may be specified as ASCII or EBCDIC**
- **Comments and remarks may be encoded for documentation**

LANGUAGE REQUIREMENTS

Input Requirements

Input to the assembler consists of a sequence of characters combined to form assembly language elements. These language elements include symbols, instruction mnemonics, constants and expressions which make up the individual program statements that comprise a source program.

CHARACTERS

Alphabetic:	A through Z
Numeric:	0 through 9
Special Characters:	blank
	(left parenthesis
	) right parenthesis
	+ add or positive value
	- subtract or negative value
	* asterisk
	' single quote
	, comma
	/ slash
	$ dollar sign
	< less than sign
	> greater than sign

SYMBOLS

Symbols are formed from combination or characters. Symbols provide a convenient means of identifying program elements so they can be referenced by other elements.

CONSTANTS

A constant is a self-defining language element. Unlike a symbol, the value of a constant is its own "face" value and is invariant. Internal numbers are represented in 2's complement notation. There are two forms in which constants may be written: the Self-Defining Constant and the General Constant.

Self-Defining Constant

The self-defining constant is a form of constant which is written directly in an instruction and defines a decimal value.

General Constant

The general constant is also written directly in an instruction, but the interpretation of its value is dictated by a code character and delimited by quotation marks. Its form can be binary, octal, decimal, hexadecimal, EBCDIC or ASCII.

EXPRESSIONS

An expression is an assembly language element that represents a value. It consists of a single term or combination of terms separated by arithmetic operators. A term may be a valid symbolic reference, a self-defining constant or a general constant.

Fields

A statement prepared for processing by the assembler is logically divided into four fields, as indicated below. They are free form and are separated by at least one blank character. The name must begin in logical column 1.

LABEL OPERATION OPERAND COMMENTS
name opcode operand(s)

Where:

FIELD	DESCRIPTION
Label	Contains an optional label which the assembler will assign as the symbolic address of the first byte of the instruction.
Operation	Contains any of the 2650 processor mnemonic operation codes as detailed in Appendix A, or any assembler Directive. This field may include an expression which specifies a register or value as required by the instruction. All symbols used in this field must have been previously defined, i.e., no symbolic forward references are allowed.
Operand	Contains one or more operand elements such as indirect address indicator, operand expression, index register specification, auto-increment/auto-decrement indicator, constant specification, etc., depending on the requirements of the particular instruction.
Comments	Any characters following the argument field will be reproduced in the assembly listing without processing. The Comments Field must be separated from the argument field by at least one blank.

Directives

There are eleven directives which the assembler will recognize. These assembler directives, although written much like processor instructions, are simply commands to the assembler instead of to the processor. They direct the assembler to perform specific tasks during the assembly process, but have no meaning to the 2650 processor. These assembler directives are:

MNEMONIC	FUNCTION
ORG	Set location counter
EQU	Specify a symbol equivalence
ACON	Define address constant
DATA	Defines memory data
RES	Reserve memory storage
END	End of assembly
EJE	Eject the listing page
PRT	Printer control
SPC	Space control
TITL	Title
PCM	Punch control

DESCRIPTION

The 2650 Simulator (PIPSIM) is a Fortran IV program which allows a user to simulate the execution of his program without utilizing the 2650 processor. The simulator executes the 2650 program via host computer software by maintaining its own internal Fortran storage registers to describe the 2650 program, the microprocessor registers, the ROM/RAM memory configuration, and the input data to be read dynamically from I/O devices. Inputs to the simulator are the object module (or the 2650 program in object format) produced by the 2650 assembler and a deck of user commands. The simulator can accommodate an object module of up to 8,192 bytes.

The output consists of a listing of the user's commands and a printout of both static and dynamic information as requested by the commands. The user may request traces of the processor status, dumps of the contents of memory, and recording of program timing statistics. Multiple simulations of the same program with different parameters may be executed during one simulation run.

FEATURES

- **Cycle counter for timing estimates**
- **Instruction fetch break points**
- **Operand fetch break points**
- **Trace facilities**
- **Snapshot dumps**
- **Patching facility**
- **Statistical information generated**
- **Easy-to-use command language**
- **Optionally selected start and end addresses**
- **Simulated registers may be displayed while the simulation program is executed**
- **Simulated registers may be altered while the program is executing**
- **Maintain a 8K cell to simulate a read/write RAM**
- **Capability exists for configuring parts of simulator memory to look like ROM**
- **Incorporates a 200-byte first in, first out (FIFO) buffer to store the data read from a simulated input device**
- **Establishes initial program conditions**
- **Monitors execution sequences**

AVAILABILITY

The 2650 Simulator is available on NCSS, TYMSHARE and GE timesharing services. It is also available from Signetics on a 9 track magnetic tape written in EBCDIC in 80 character unblocked records at a density of 800bpi.

The Simulator available on tape is configured to execute 16-bit machines (2650 SM1100) and 32-bit machines (2650 SM1000).

DESCRIPTION

The Signetics higher level language is designed for use with the 2650 microprocessor. This language allows the programmer to to reduce programming effort while retaining the control and efficiency of assembly language. It is written in ANSI standard Fortran IV and will execute on most machines without alteration. Programs written in this language tend to be self-documenting and are easily altered.

AVAILABILITY

The Signetics higher level language is available on both NCSS and GE timeshare. It is also available from Signetics on magnetic tape for 32-bit machines.

FEATURES

- **Written in free-form**
- **Block structured**
- **Employs procedure calls**
- **Byte and address data elements**
- **Based variables**
- **In line assembly language**
- **Macro capability**
- **Generates relocatable code supported by a relocating loader**
- **Includes PL/M as a subset**
- **Allows separate compilation of program modules**
- **Has improved control structure over PL/M**
- **Conditional compilation**
- **Compile time expression evaluation**

OVERVIEW OF THE LANGUAGE

The higher level language is a sequence of "Declarations" and "Executable Statements."

The declarations allow the programmer to control allocation of storage, define simple textual substitutions (Macros), and define procedures. The language is "Block Structured": Procedures may contain further declarations which control storage allocation and define other procedures.

The procedure definition facility of the language allows modular programming: A program can be divided into sections (e.g. teletype input, conversion from binary to decimal forms, and printing output messages). Each of these sections is written as a language procedure. Such procedures are conceptually simple, easy to formulate and debug, and easily incorporated into a large program. They may form a basis for a procedure library, if a family of similiar programs is being developed. Procedures may be individually compiled.

The language handles two kinds of data, its two basic "Data Types": Byte and address. A byte variable or constant is one that can be represented as an 8-bit quantity; an address variable or constant is a 16-bit or double-byte quantity. The programmer can declare variable names to represent byte or address values. One can also declare vectors (or arrays) or type byte or address.

In general, executable statements specify the computational processes that are to take place. To achieve this, arithmetic, logical (Boolean), and comparison (relational) operations are defined for variables and constants of both types (BYTE and ADDRESS). These operators and operands are combined to form EXPRESSIONS, which resemble those of elementary algebra. Expressions are a major component of language statements.

A simple statement form is the assignment statement, which computes a result and stores it in a memory location defined by a variable name. Other statements in the language perform conditional tests and branching, loop control, and procedure invocation with parameter passing. The flow of program execution is specified by means of powerful control structures that take advantage of the block-structured nature of the language. Input and output statements read and write 8-bit values from and to input and output ports. Procedures can be defined which use these basic input and output statements to perform more complicated I/O operations.

A method of automatic text-substitution (more specifically, a "compile-time macor facility") is also provided. A programmer can declare a symbolic name to be completely equivalent to an arbitrary sequence of characters. As each occurrence of the name is encountered by the compiler, the declared character sequence is substituted, so the compiler actually processes the substituted character string instead of the symbolic name.

The compiler supports compile time expression evaluation and conditional compilation which allows selective compilation of code depending on an input parameter at compile time.

The language generates absolute and/or relocatable code. The relocatable modules may be linked by a powerful linkage editor at load time.

Additionally the language contains all machine independent features of the PL/M language as a subset, thereby enhancing portability of programs.

DESCRIPTION

The 2650 assembly language is a symbolic language designed specifically to facilitate the writing of programs for the Signetics 2650 Microprocessor.

The 2650 relocatable assembler is a program which accepts symbolic source code as input and produces a listing, cross-reference table of symbols, and an object module. The object module may be in absolute format compatible with the simulator (PIPSIM), PIPBUG and the 2650 TWIN system, or it may be a relocatable format for use with PLμS and the relocating loader.

The assembler is written in ANSI standard Fortran IV and is approximately 3200 Fortran card images in length. It operates in a two-pass mode to build a symbol table, issue helpful error messages, produce an easily readable program listing and cross-reference listing, and output a computer readable object module.

AVAILABILITY

The 2650 relocatable assembler is available on NCSS, GE, and TYMSHARE timesharing services. It is also available from Signetics on 9-track magnetic tape written in EBCDIC in 80 character unblocked records at a density of 800 bpi.

FEATURES

- **Pseudo-ops to aid programming**
- **Self-defining constants**
- **Symbolic machine operation codes**
- **Free format source code**
- **Syntax error checking**
- **Symbolic address assignment and references**
- **Data creation statements**
- **Storage reservation statements**
- **Assembly listing control statements**
- **Address constants**
- **ASCII character codes**
- **Comments and remarks for documentation**
- **Six-character symbols**
- **Cross-reference listing of symbols**
- **Automatic formatting of the listing**
- **Complex expression evaluation**
- **Conditional assembly**
- **Boolean operators**
- **Relocatable output compatible with the PLμS compiler output**

LANGUAGE REQUIREMENTS

Input Requirements

Input to the assembler consists of a sequence of chartacters combined to form assembly language elements. These language elements include symbols, instruction mnemonics, constants and expressions which make up the individual program statements that comprise a source program.

CHARACTERS

Alphabetic:	A through Z
Numeric:	0 through 9
Special Characters:	blank
	(left parenthesis
	) right parenthesis
	+ add or positive value
	- subtract or negative value
	* asterisk
	' single quote
	, comma
	/ slash
	$ dollar sign
	< less than sign
	> greater than sign
	# pound sign
	@ at sign
	? question mark
	! exclamation
	" double quote
	% percent sign
	= equal
	; semicolon
	¬ not symbol
	: colon
	. period

SYMBOLS

Symbols are formed from combinations of characters. Symbols provide a convenient means of identifying program elements so they can be referenced by other elements.

CONSTANTS

A constant is a self-defining language element. Unlike a symbol, the value of a constant is its own "face" value and is invariant. Internal numbers are represented in 2's complement notation. There are two forms in which constants may be written: the Self-Defining Constant and the General Constant.

SELF-DEFINING CONSTANT

The self-defining constant is a form of constant which is written directly in an instruction and defines a decimal value.

GENERAL CONSTANT

The general constant is also written directly in an instruction, but the interpretation of its value is dictated by a code character and delimited by quotation marks. Its form can be binary, octal, decimal, hexadecimal, or ASCII.

EXPRESSIONS

An expression is an assembly language element that represents a value. It consists of a single term or combination of terms separated by arithmetic or boolean operators. A term may be a valid symbolic reference, a self-defining constant or a general constant.

FIELDS

A statement prepared for processing by the assembler is logically divided into four fields, as indicated below. They are free form and are separated by at least one blank character. The name must begin in logical column 1.

LABEL	OPERATION	OPERAND
name	opcode	operand(s)

Where:

FIELD	DESCRIPTION
Label	Contains an optional label which the assembler will assign as the symbolic address of the first byte of the instruction.
Operation	Contains any of the 2650 processor mnemonic operation codes as detailed in Appendix A of the reference manual, or any assembler directive. This field may include an expression which specifies a register or value as required by the instruction. All symbols used in this field must have been previously defined, i.e., no symbolic forward references are allowed.
Operand	Contains one or more operand elements such as indirect address indicator, operand expression, index register specification, auto-increment/auto-decrement indicator, constant specification, etc., depending on the requirements of the particular instruction.
Comments	Any characters following the argument field will be reproduced in the assembly listing without processing. The Comments Field must be separated from the argument field by at least one blank.

Directives

There are fifteen directives which the assembler will recognize. These assembler directives, although written much like processor instructions, are simply commands to the assembler instead of to the processor. They direct the assembler to perform specific tasks during the assembly process, but have no meaning to the 2650 processor. These assembler directives are:

MNEMONIC	FUNCTION
ORG	Set location counter
EQU	Specify a symbol equivalence
ACON	Define address constant
DATA	Defines memory data
RES	Reserve memory storage
END	End of assembly
EJE	Eject the listing page
PRT	Printer control
SPC	Space control
TITL	Title
PCH	Punch control

IF
ENDIF
ELSE
	Conditional assembly

SEG	Begin a relocatable segment
ENDS	End a relocatable segment
ENTRY	Define an entry point
EXTRN	Define an external reference

DESCRIPTION

The TWIN (TestWare Instrument) system, shown in the block diagram of Figure 1, consists of interdependent subsystems, each contributing to the total task of implementing user microprocessor applications from initial concept to actual hardware operation. The system closely resembles a general-purpose minicomputer during the initial stages of product development, and allows source programs to be entered, edited and assembled into object programs. Object programs may be executed simply as programs, or as part of a user's product emulation. When programs have been run and debugged to the user's satisfaction, the TWIN system is capable of programming PROM devices for inclusion in the user's prototype hardware.

The program development computer is configured using plug-in modules, each dedicated to a specific task within the system. Each module interacts with the others by use of a common bus structure. The major buses include a data bus, an address bus, and a control bus. The program development computer acts as the controller for the entire system, and performs the necessary functions of transferring data to and from system peripherals.

To facilitate system operation, a dual-drive floppy disk subsystem is provided in all TWIN configurations. This subsystem, with integral controller, stores user program "files" and allows retrieval of these files for operations by the editor and assembler. The Signetics Disk Operating System (SDOS) software is loaded from the disk system into the development computer. SDOS provides complete control over all portions of the TWIN system.

A CRT console is the standard device for entering user programs. It is equipped with a full ASCII keyboard for data entry and a CRT display to allow the operator to view the results of his program manipulations during editing, assembly, and debug operations. The display and keyboard can be separated for user convenience. An interface is provided for an ASR-33 teletypewriter, which can be used in place of the CRT console. An optional line printer provides hard copy output.

Other system I/O devices can be added to the system to enhance its capabilities. Physical interface to the system bus is accomplished by use of the optional General-Purpose I/O card. Addition of a peripheral device requires addition of its software driver to the TWIN operating system.

TWICE (TestWare In-Circuit Emulation) denotes hardware/software elements of the TWIN system that support the integration and check-out of the user's prototype product. A number of different TWICE operation modes support product development, integration, and production.

THE TWIN SYSTEM

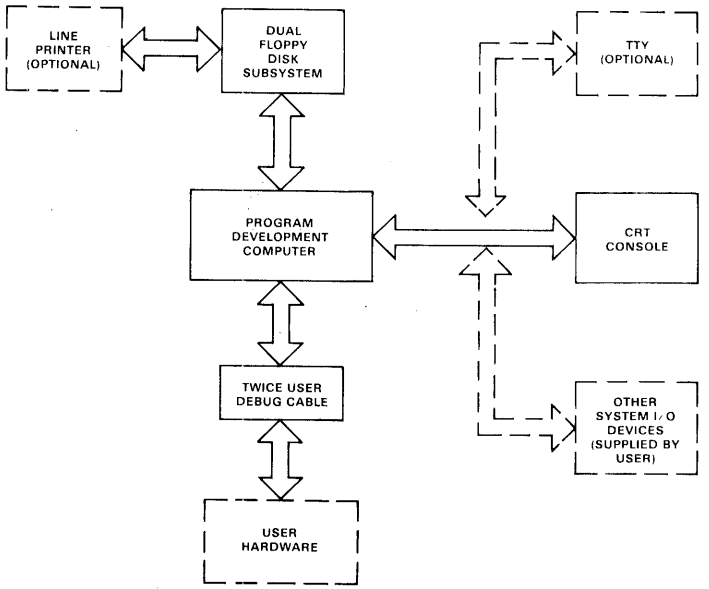


Figure 1

TWIN HARDWARE

The TWIN system is available in two configurations: the BASIC TWIN and the SUPER TWIN.

Basic TWIN Configuration

Program Development Computer consisting of:
- Master CPU—16K Master Memory
- Slave CPU—16K Slave Memory
- Debug Logic Card

TWICE Cable
Dual-Drive Floppy Disk Subsystem

Super TWIN Configuration

Basic TWIN configuration plus:
- 1702A PROM Program card
- 82S115 PROM Program card
- General-Purpose I/O Card

CRT Console
Line Printer

Program Development Computer

The Program Development Computer (PDC) is the principal subsystem of the TWIN. The PDC employs dual-processor architecture operating on a common bus structure.

The Master/Slave architectural concept provides the following features:

1. Protected operating system memory and I/O.
2. Complete user access to slave memory address space and I/O address space.
3. Operating system and Debug software are independent of user programs.
4. Use of future Slave processors by adding boards and supplying additional software only.
5. Multiple Slave CPUs of different types can be accommodated.
6. Debug and TWICE hardware.

The PDC can be divided into four distinct areas as shown in Figure 2.

1. The master CPU provides access to all support peripherals (Floppy Disk, Line Printer and CRT console). By way of the common bus, the slave side of the system can make requests of these system peripherals. In addition, via the General Purpose I/O Board, the user has the option of adding system peripherals on the master side.
2. The master CPU controls PROM programming by transferring data from the slave memory to the PROM sockets. Both erasable (1702A) and nonerasable (82S113) PROMs can be programmed through sockets controlled by the operating system.

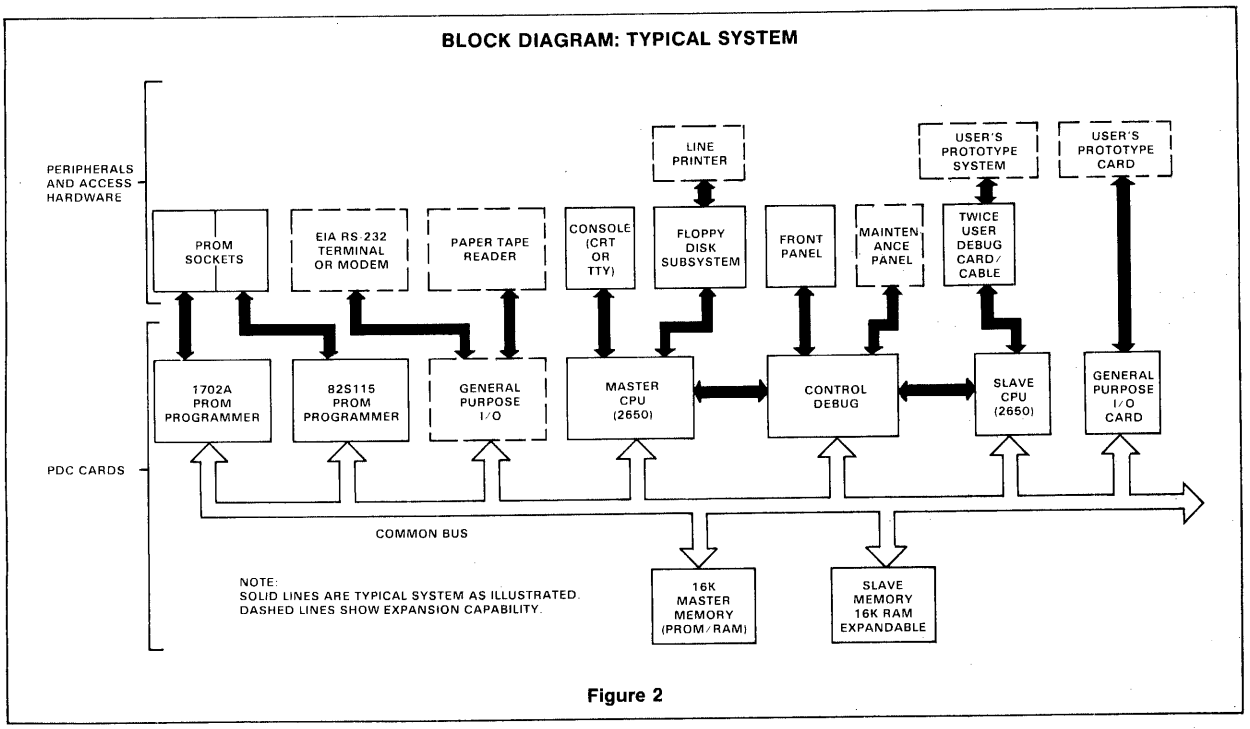


Figure 2

3. The third functional area, known as TWICE, provides interface from the Program Development Computer (PDC) to the prototyping world. TWICE consists of a cable and driver/receiver hardware that allow in-circuit emulation of the user programs in the TWIN system. The user's microprocessor is unplugged from the prototype and replaced by the TWICE cable plugged directly into the vacant socket. The other end of the Program Development Computer cable connects to the slave CPU board. This board contains multiplexing and other logic to support the TWICE operating modes. The slave CPU thus becomes the CPU for the prototype system, allowing programs to be executed in a hardware environment nearly identical to that of the user's final product.

   In addition, a General-Purpose I/O card or prototype card may be added to the system bus to provide interface with user prototype peripherals.
4. The fourth subsystem is built around the control debug card that links the master CPU to the slave CPU. This card, in conjunction with the front panel and maintenance panel on the PDC, allows for Master/Slave communication under SDOS.

PROGRAM DEVELOPMENT COMPUTER SUBASSEMBLIES

Master CPU

Provides a resident microcomputer for the operating system software. Prioritizes and services all interrupts regardless of whether they were initiated from the master or slave partitions.

- Responsible for system I/O

Master Memory

This memory is reserved for the resident monitor and the overlays from disk necessary to service any valid user request. A minimum of 16K bytes of memory is required.

- Protected from slave access
- Four 4K statis RAM cards (or 16K dynamic card)
- 256 bytes of PROM—expandable to 2K bytes on one of the master memory cards.

Slave CPU

Provides an isolated microprocessor that enables the user to write and debug his program without endangering the operating system. The slave CPU also executes the user's program in his prototype via the TWICE cable.

- While the slave CPU is presently a 2650 microprocessor, future designs will support other microprocessors.
- Enables real-time execution of the user's programs in his prototype system.

Slave Memory

The primary function of the slave memory is to store programs. During PROM programming, the debugged software logic in the slave memory is sent via the common bus to the PROM programming cards on the master side. During in-circuit emulation, the TWICE cable is connected through the Slave CPU to the Slave memory.

- Four 4K static RAM cards (or 16K dynamic card)
- Base address selectable in 4K increments
- Expandable from 16K to 64K bytes.

Common Bus

These data, address and control channels provide communications between slave and master partitions as well as communications to other boards for outside world interfacing.

Debug Board

Designed to provide communications between slave and master partitions; it also supplies interface capability to the front panel.

- Two address breakpoint registers
- Two program counter registers
- Single cycle, halt, and diagnostic interrupts

PROM Programmer Boards

These cards, placed in two reserved slots of the master partition, provide access to front-panel PROM sockets on the PDC. They provide either erasable or nonerasable PROM programming of Signetics 82S115 bipolar PROMs and 1702A MOS PROMs.

- Read, write and compare functions
- Checks validity, power, and addresses
- Interfaces directly to bus
- Current limiting amplifier
- On-card rectifier/regulator

General-Purpose I/O Card

This card may be placed on the master side to support additional system peripherals and/or on the slave side to provide an interface to the user's hardware I/O simulator boards.

- Compatible with 20mA, 110 baud TTY interface
- Compatible with EIA/RS-232 interfaces
- Baud rates—110/150/300/600/1200, jumper selectable
- Four 8-bit input ports and four 8-bit output ports
- Eight interrupts

Disk/Printer Controller Board

This card supports parallel I/O transfers to the floppy disk subsystem and to the optional printer. This board is contained in the floppy disk subsystem.

FUNCTIONAL HARDWARE/ SOFTWARE INTEGRATION

The TWIN system's operating functions can be grouped into three major modes as shown in Figure 3.

Software Development

Using the TWIN Assembler and Text Editor, the designer clears his programs of any syntax errors. The system I/O devices interfaced through the master side of the TWIN enable the user to develop and debug his software. The software is verified as much as possible before actually running it in the user's prototype system. All memory and I/O are contained in the TWIN. As shown in Figure 3A, there is no interconnection with the user's prototype system.

Software/Hardware Integration

The final development phases are accomplished using the TWICE capability. In these phases, the user can easily complete the normally complex function of hardware/ software system debugging.

PROTOTYPE HARDWARE INTERFACE (TWICE): The TWIN memory is used by the Slave, but I/O is provided to the user's system via the TWICE cable as shown in Figure 3B. The user's program that had been loaded into Slave Memory by SDOS is executed by the user's prototype circuits.

PROM INTEGRATION (TWICE): All program memory and prototype I/O are contained in the user's system as shown in Figure 3C. The operator can still control breakpoints, starting addresses and obtain a partial Trace. This mode is used after PROMs and ROMs have been prepared. This mode verifies the final system configuration in real-time operation.

TWIN DEVELOPMENT SOFTWARE

System software provided with the Prototype Development System includes the Signetics Disk Operating System (SDOS), Text Editor, Assembler, and Debug Package.

SDOS

SDOS relieves the user of the necessity of understanding the detailed internal operation of the TWIN. It provides complete control over operation of all portions of the Prototype Development System. All functions relating to file handling, loading and execution are monitored and controlled by SDOS, including the in-circuit emulation and the PROM programming functions. SDOS is written in 2650 assembly language and resides in a dedicated memory consisting of a 256-byte PROM and 16K RAM running under the master CPU.

The SDOS software allows the user to create, edit, and assemble files; obtain object and listing outputs; load and execute programs; and, through the debug system, check out programs in an efficient manner.

SDOS provides a powerful command file capability that enables the user to create customized operating system commands.

SDOS controls the multi-drive floppy disk subsystem, a line printer, and the CRT console, which may be an ASR-33 TTY or an RS-232 compatible device. Software drivers are provided within SDOS for these I/O devices. The SDOS software provides a flexible input/output system that enables the user to dynamically assign any logical channel to any physical device or file within the system. Thus, system I/O devices may be dynamically assigned using SDOS commands either from the console or from within a user's program. Thus, the user may write his own driver for other peripheral devices and link them into the SDOS system by use of the optional General-Purpose I/O Card.

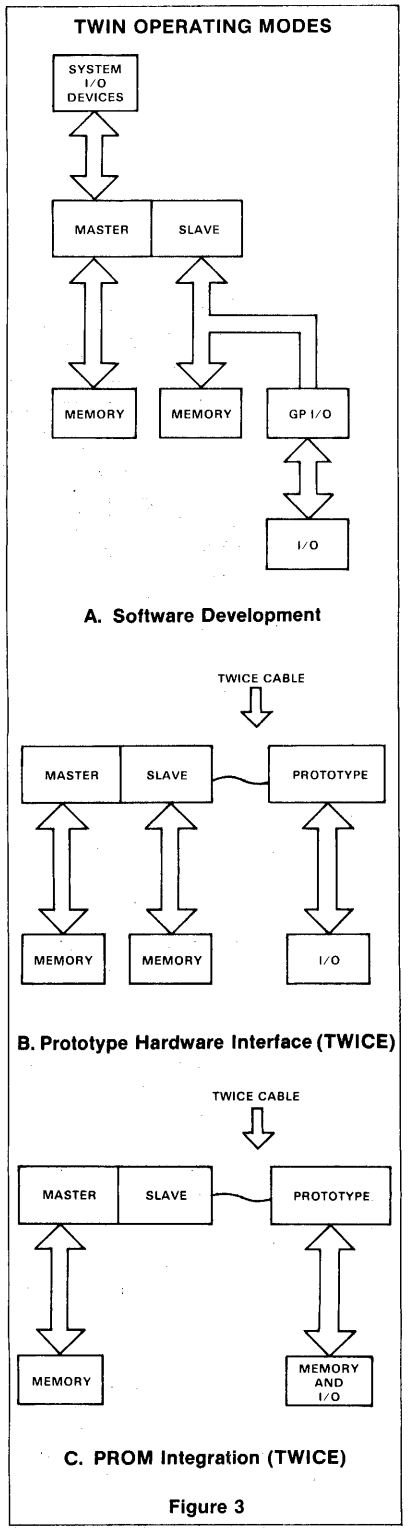


Figure 3

THE TWIN SYSTEM

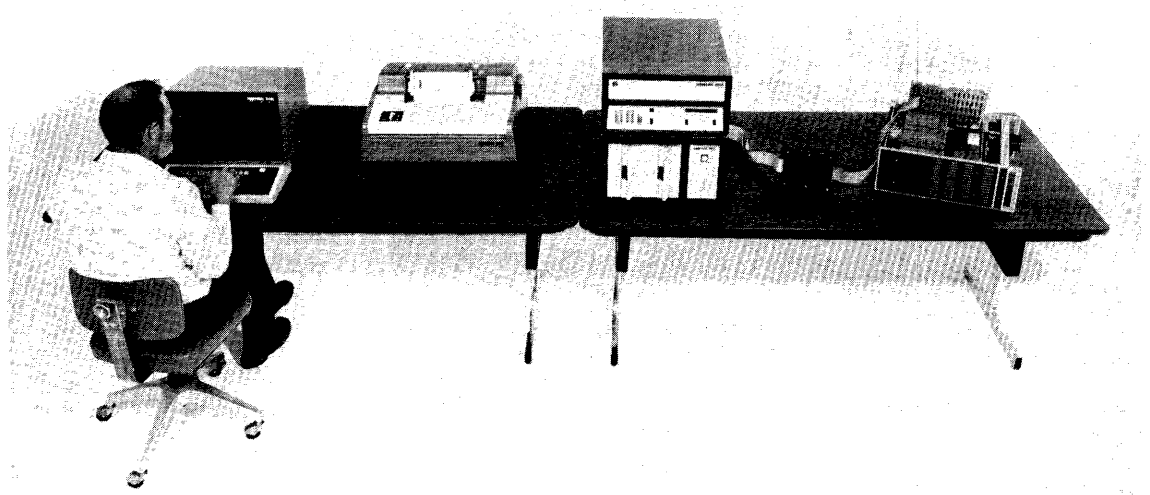


Figure 4

Text Editor

The Text Editor is a comprehensive software package that allows the user to enter and modify text files. The Text Editor is line oriented and accepts inputs from the terminal or a diskette file, performs modifications in a work space, and outputs the revised text to diskette file.

Assembler

The Prototype Development System Resident Assembler translates symbolic assembly language instructions into appropriate machine language code.

The Assembler is written in the Signetics Higher-Level Language (PLμS) and generates absolute object code. This code is in hexadecimal format and may be loaded into the system for direct execution or may be converted by an SDOS command to SMS format for PROM or ROM programming.

Debug

The debug system is a software program which provides the user with real-time program debug capabilities within both a software and hardware environment. It uses special hardware features built into the program development system to control the execution of the user's program. User programs operating under the debug system have dynamic program trace, breakpoint capabilities, and memory modification capabilities. Status reporting on the memory, the program, and the processor is also provided.

PHYSICAL AND ENVIRONMENTAL SPECIFICATIONS

	VOLTAGE	VOLT AMPERES	LINE FREQUENCY (HERTZ)	WEIGHT (POUNDS)	DIMENSIONS (INCHES)
Development Computer	115 ± 10%	230	47 — 63	65	8 x 17 x 22
Dual-Drive Floppy Disk	115 ± 10%	400	59.5 — 60.5	85	10 x 17 x 22
CRT Console	115 ± 10%	130	47 — 63	52	14 x 17 x 22
Printer	115 ± 10%	375	59.5 — 60.5	66	12 x 23 x 19

NOTE

Export version will operate from other line voltages and frequencies.

Table 1 SUBSYSTEM CHARACTERISTICS

Total System Characteristics

Operating Temperature Range:	15° — 37°C
Operating Humidity Range:	50% — 80% NC
Basic system shipping weight:	180 pounds

Card Cage—Mother Board Assembly

7 x 11 cards/20 slots in PDC

Common Bus Structure

External +5V ground bus (spare with rear panel terminals)

Front Panel Switches and Indicators

Key-operated primary power On/Off switch

PROM power switch

Reset switch that initializes system and sets both CPUs to location zero, enables master, and pauses slave.

Diagnostic interrupt switch

Power indicator

Run indicator

Master indicator

Slave indicator

PROM power indicator

SDOS COMMAND SUMMARY

System Utilities

COMMAND	FUNCTION
FORMAT D	Formats the diskette on drive D.
VERIFY D	Verifies the diskette on drive D.
RENAME D	Re-identifies the diskette on drive D.
DUP	Duplicates a diskette.
LDIR (D)	Lists the directory of the diskette.
DELETE	Deletes a diskette file.
COPY	Copies data from a specified input device or file to a specified output device or file.
PRINT (L)	Prints from a disk file to a specified output device. If (L) is included, the lines are numbered.

System Control

COMMAND	FUNCTION
SUSPEND	Suspends execution of an active program.
CONT	Continues execution of a suspended program.
ABORT	Aborts an active SDOS or user program.
ESCAPE*	Interrupts the execution of a program.
DOUBLE ESCAPE*	Suspends execution of all programs.
SPACE*	Stops or starts the console output.
STATUS	Gives the status of the program being executed by the Slave CPU.
ASSIGN	Connects a logical channel to a specified device.
CLOSE	Closes the specified channels.
	*Keys on console

Object Program Utilities

COMMAND	FUNCTION
RHEX	Loads an absolute hexadecimal object file into slave memory.
WHEX	Outputs an absolute hexadecimal data file from slave memory.
WSMS	Outputs a 512-byte block of memory in SMS format.
CSMS	Reads an SMS file and compares it with the contents of memory.
MODULE	Creates an absolute binary program load module from the Slave CPUs memory.

Debug Commands

COMMAND	FUNCTION
DEBUG	Enables debug mode for user programs.
BKPT	Selects a program breakpoint.
CLBP	Clears breakpoint.
SET	Modifies Slave CPU register(s).
DSTAT	Displays the Slave CPU registers and the selected breakpoints.
TRACE	Sets program trace control.
PATCH	Alters slave memory.
DUMP	Dumps slave memory.
EXAM	Examines and optionally alters slave memory.
SLAVE	Designates the active Slave CPU and sets its mode of operation.
RESET	Resets the Slave CPU.
LOAD	Loads a program load module into the Slave CPUs memory.
XEQ	Loads and executes a program load module.
GO	Executes a previously loaded load module or transfers control to an absolute memory location in slave memory.

Command File

COMMAND	FUNCTION
TYPE	Controls command line typeout during execution of a command file.
KILL	Aborts or continues a command file if an error is encountered.
*	Implements comments within a command file.

Editor

COMMAND	FUNCTION
EDIT	Loads and executes the Text Editor.

Assembler

COMMAND	FUNCTION
ASM	Loads and executes the 2650 assembler.

PROM Utilities

COMMAND	FUNCTION
RPROM	Reads the contents of PROM into slave memory.
CPROM	Compares the contents of slave memory with the contents of PROM
WPROM	Burns a PROM with the contents of slave memory.

System Options

COMMAND	FUNCTION
SYSTEM	Designates the system drive.
DEVICE	Informs SDOS of device status.
SEARCH	Specifies file search option.

TEXT EDITOR COMMAND SUMMARY

COMMAND	FUNCTION
AGAIN	Repeats the last "repeatable" command entered.
BEGIN	Sets the current line pointer to the first line of the work space.
BRIEF	Reverses the initial mode of operation.
COPY N	Copies n lines, or lines p through q, from the input file FILENAME$_1$ to the output file FILENAME$_2$.
DOWN n	Moves the current line pointer down n lines.
END	Sets the current line pointer to the end of text (last line plus one).
FILE	Transfers all workspace text and remaining primary input file text to the primary output file and quits the editor.
FIND	Moves the current line pointer down to the line containing the first occurrence of a character string.
GET N	Gets n lines or lines p through q into the workspace.
INPUT	Establishes the "input" mode.
INSERT	Inserts a given string above the current line.
KILL N	Deletes n lines starting with the current line, or deletes lines p through q.
LIST N	Lists n lines or lines p through q on the line printer.
MACRO	Creates a macro.
MACRO m	Executes the previously defined macro m.
N	Types the current line printer position on the console.
PUT(K) N	Puts n lines starting at the current line or puts lines p through q from the workspace to the primary output file.
QUIT	Closes the primary input and primary output files and quits the editor.
REPLACE	Replaces the current line with a character string.
SDOS	Suspends the text editor and returns control to SDOS.
SUBSTITUTE	Substitutes text on the current line.
TAB C	Defines the character C as the tab character.
TABS	Sets tab positions to specified columns.
TYPE N	Types n lines or lines p through q on the console.
UP n	Moves the current line pointer up n lines.
m<>	Repeats the command string enclosed by the brackets m times.
?	Types the current I/O status on the console.

CHAPTER 3
Standard Support Circuits

INTRODUCTION

In addition to the dedicated support circuits available for the various Signetics microprocessors, Signetics offers a complete line of standard circuits to complete the design of a microcomputer system.

A complete line of Schottky-clamped TTL, read/write memory arrays is offered. All feature open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, chip enable function and PNP input transistors which reduce input loading requirements. All devices offer high performance read access and write cycle times making these devices ideally suited in high speed memory applications such as "cache," buffers, scratch pads, writable control store, main store, etc.

Signetics offers the industry's broadest line of bipolar high performance ROMs, PROMs and FPLAs. The PROMs and FPLAs are field programmable, which means that custom patterns are immediately available by following the provided fusing procedures. Signetics PROMs are supplied with all outputs at logical 0. Outputs are programmed to a logic 1 at any specified address by fusing a Ni-Cr link matrix. All bipolar ROMs, PROMs and FPLAs are fully TTL compatible, and include on-chip decoding and chip enable functions for ease of memory expansion. Tri-state and open collector output functions are available, and low input currents reduce input buffer requirements. Most Signetics PROMs and FPLAs also have pin and performance compatible ROMs and PLAs, offering the user the ultimate in flexibility and cost reduction.

Signetics n-channel MOS products include a complete family of 1k static RAMs and 8k static ROMs. These feature TTL compatible inputs and outputs, and require only a single +5V power supply. A variety of 4k dynamic RAMs is also available for system configurations requiring large amounts of read/write memory.

The 8T series of interface devices includes display drivers, bus drivers, input/output ports, level converters, and special purpose devices. A complete line of standard and low power Schottky (LS) 74 series devices is available in addition to the 8200 series of MSI devices. Many devices from the Signetics analog product line are also suitable for use in microcomputer systems. These include voltage regulators, operational amplifiers, comparators and timers.

This chapter provides product line summaries and data for a representative selection of Signetics standard support circuits.

BIPOLAR MEMORY SELECTION GUIDE

DEVICE	ORGANI-ZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME [ns][4]	TEMPERATURE RANGE[3]	PACKAGE	NO. OF PINS	MAX. I_{CC} [mA][4]
CAMS								
10155	8X2	OE	—	13	C	F,N	18	140
SAMS								
82S12	8X4	OC	T	40	C	F,N	24	160
82S112	8X4	TS	T	40	C	F,N	24	160
RAMS								
82S25	16X4	OC	B	50	M,C	F,N	16	105
3101A	16X4	OC	B	35	M,C	F,N	16	105
54/74S89	16X4	OC	T	50	M,C	F,N	16	105
54/74S189	16X4	TS	B	35	M,C	F,N	16	110
82S21	32X2	OC	T	50	C	F,N	16	130
82S16	256X1	TS	T	50	M,C	F,N	16	115
82S116	256X1	TS	T	40	C	F,N	16	115
82S17	256X1	OC	T	50	M,C	F,N	16	115
82S117	256X1	OC	T	40	C	F,N	16	115
54/74S200	256X1	TS	B	50	M,C	F,N	16	130
54/74S201	256X1	TS	B	50	M,C	F,N	16	130
54/74S301	256X1	OC	B	50	M,C	F,N	16	130
82S09	64X9	OC	T	45	M,C	I,N	28	190
82S10	1024X1	OC	B	45	M,C	F,N	16	170
82S110	1024X1	OC	B	35	C	F,N	16	170
82S11	1024X1	TS	B	45	M,C	F,N	16	170
82S111	1024X1	TS	B	35	C	F,N	16	170
93415A	1024X1	OC	B	45	M,C	F,N	16	170
93425A	1024X1	TS	B	45	M,C	F,N	16	170
82S208*	256X8	TS	B	60	C	F	22	185
82S210*	256X9	TS	B	60	C	F,N	24	185
82S400*	4096X1	OC	B	70	C	I	18	155
82S401*	4096X1	TS	B	70	C	I	18	155
ROMS								
82S226	256X4	OC	—	50	M,C	F,N	16	120
82S229	256X4	TS	—	50	M,C	F,N	16	120
82S214	256X8	TS	—	60	M,C	F,N	24	175
82S230	512X4	OC	—	50	M,C	F,N	16	140
82S231	512X4	TS	—	50	M,C	F,N	16	140
82S215	512X8	TS	—	60	M,C	F,N	24	175
82S240	512X8	OC	—	60	M,C	F,N	24	175
82S241	512X8	TS	—	60	M,C	F,N	24	175
8228	1024X4	TTL	—	50	C	F	16	170
82S280	1024X8	OC	—	70	M,C	F,N	24	140
82S281	1024X8	TS	—	70	M,C	F,N	24	140
82S290	2048X8	OC	—	80	M,C	F,N	24	170
82S291	2048X8	TS	—	80	M,C	F,N	24	170

*To be announced

NOTES

1. Output circuit:
   OE = Open emitter
   OC = Open collector
   TS = Tri-state
2. Output logic:
   T = Transparent—input data appears on output during Write
   B = Blanked—output is blanked during Write
3. Temperature range:
   C = Commercial (0° C to +75° C)
   M = Military (-55° C to +125° C)
   All ECL 10,000 series (-30° C to +85° C)
4. Commercial (0° C to +75° C)

BIPOLAR MEMORY SELECTION GUIDE (Cont'd)

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME (ns)	TEMPERATURE RANGE[3]	PACKAGE	NO. OF PINS	MAX. I_{CC} (mA)	EQUIVALENT ROM
PROMS									
82S23	32X8	OC	—	50	M,C	F,N	16	77	—
82S123	32X8	TS	—	50	M,C	F,N	16	77	—
10139	32X8	OE	—	15	C	F,N	16	145	—
82S27	256X4	OC	—	40	C	F	16	140	—
82S126	256X4	OC	—	50	M,C	F,N	16	120	82S226
82S129	256X4	TS	—	50	M,C	F,N	16	120	82S229
10149	256X4	OE	—	20	C	F	16	150	—
82S114	256X8	TS	—	60	M,C	F,N	24	175	82S214
82S130	512X4	OC	—	50	M,C	F,N	16	140	82S230
82S131	512X4	TS	—	50	M,C	F,N	16	140	82S231
82S115	512X8	TS	—	60	M,C	F,N	24	175	82S215
82S140	512X8	OC	—	60	M,C	F,N	24	175	82S240
82S141	512X8	TS	—	60	M,C	F,N	24	175	82S241
82S136	1024X4	OC	—	60	M,C	F,N	18	140	—
82S137	1024X4	TS	—	60	M,C	F,N	18	140	—
82S180	1024X8	OC	—	70	M,C	F,N	24	175	82S280
82S181	1024X8	TS	—	70	M,C	F,N	24	175	82S281
82S2708	1024X8	TS	—	70	M,C	F,N	24	175	—
82S184	2048X4	OC	—	100	M,C	I	18	120	—
82S185	2048X4	TS	—	100	M,C	I	18	120	—
82S190	2048X8	OC	—	70	M,C	I	24	175	82S290
82S191	2048X8	TS	—	70	M,C	I	24	175	82S291
FPLAS									
82S100	16X48X8	TS	—	50	M,C	I,N	28	170	—
82S101	16X48X8	OC	—	50	M,C	I,N	28	170	—
PLAS									
82S200	16X48X8	TS	—	50	M,C	I,N	28	170	—
82S201	16X48X8	OC	—	50	M,C	I,N	28	170	—
FPGAS									
82S102	16X9	OC	—	30	M,C	I,N	28	170	—
82S103	16X9	TS	—	30	M,C	I,N	28	170	—

*To be announced

NOTES

1. Output circuit:
   OE = Open emitter
   OC = Open collector
   TS = Tri-state
2. Output logic:
   T = Transparent—input data appears on output during Write
   B = Blanked—output is blanked during Write
3. Temperature range:
   C = Commercial (0° C to +75° C)
   M = Military (-55° C to +125° C)
   All ECL 10,000 series (-30° C to +85° C)
4. Commercial (0° C to +75° C)

MOS MEMORY SELECTION GUIDE

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	ACCESS/CYCLE TIME (ns)	TEMPERATURE RANGE[2]	PACKAGE	NO. OF PINS	CLOCK/CE/TTL COMPATABILITY	POWER SUPPLIES (V)
RAMS								
Static								
2501	256X1	TTL	1000/1000	C	I, N	16	Yes	+5, -9
25L01	256X1	TTL	1000/1000	C	I, N	16	Yes	±5, -12
2101	256X4	TS	1000/1000	C	F, N	22	Yes	+5, Gnd
2101-1	256X4	TS	500/500	C	F, N	22	Yes	+5, Gnd
2101-2	256X4	TS	650/650	C	F, N	22	Yes	+5, Gnd
2111	256X4	TS	1000/1000	C	I, N	18	Yes	+5, Gnd
2111-1	256X4	TS	500/500	C	I, N	18	Yes	+5, Gnd
2111-2	256X4	TS	650/650	C	I, N	18	Yes	+5, Gnd
2112	256X4	TS	1000/1000	C	F, N	16	Yes	+5, Gnd
2112-1	256X4	TS	500/500	C	F, N	16	Yes	+5, Gnd
2112-2	256X4	TS	650/650	C	F, N	16	Yes	+5, Gnd
2606	256X4	TS	750/750	C	F, I, N	16	Yes	+5, Gnd
2606-1	256X4	TS	500/500	C	F, I, N	16	Yes	+5, Gnd
2102	1024X1	TS	1000/1000	C	F, I, N	16	Yes	+5, Gnd
2102-1	1024X1	TS	500/500	C	F, I, N	16	Yes	+5, Gnd
2102-2	1024X1	TS	650/650	C	F, I, N	16	Yes	+5, Gnd
2102A	1024X1	TS	350/350	C	F, I, N	16	Yes	+5, Gnd
2102AL	1024X1	TS	350/350	C	F, I, N	16	Yes	+5, Gnd
2102A-2	1024X1	TS	250/250	C	F, I, N	16	Yes	+5, Gnd
2102AL-2	1024X1	TS	250/250	C	F, I, N	16	Yes	+5, Gnd
2102A-4	1024X1	TS	450/450	C	F, I, N	16	Yes	+5, Gnd
2102AL-4	1024X1	TS	450/450	C	F, I, N	16	Yes	+5, Gnd
2102A-6	1024X1	TS	650/650	C	F, I, N	16	Yes	+5, Gnd
21F02	1024X1	TS	350/350	C	F, I, N	16	Yes	+5, Gnd
210F02-2	1024X1	TS	250/250	C	F, I, N	16	Yes	+5, Gnd
21F02-4	1024X1	TS	450/450	C	F, I, N	16	Yes	+5, Gnd
21L02	1024X1	TS	1000/1000	C	F, I, N	16	Yes	+5, Gnd
21L02-1	1024X1	TS	500/500	C	F, I, N	16	Yes	+5, Gnd
21L02-2	1024X1	TS	650/650	C	F, I, N	16	Yes	+5, Gnd
21L02-3	1024X1	TS	400/400	C	F, I, N	16	Yes	+5, Gnd
2115*	1024X1	OD	45/45	C	F, I, N	16	Yes	+5, Gnd
2115L*	1024X1	OD	45/45	C	F, I, N	16	Yes	+5, Gnd
2125*	1024X1	TS	45/45	C	F, I, N	16	Yes	+5, Gnd
2125L*	1024X1	TS	45/45	C	F, I, N	16	Yes	+5, Gnd
2614*	1024X4	TS	200/200	C	F, I, N	18	—	+5, Gnd
2613*	4096X1	TS	200/200	C	F, I, N	18	—	+5, Gnd
Dynamic								
1103	1024X1	OD	300/480	C	I, N	18	No	+20, +16, Gnd
2660	4096X1	TS	250/375	C	F, I, N	16	Yes	+12, ±5, Gnd
2660-1	4096X1	TS	300/425	C	F, I, N	16	Yes	+12, ±5, Gnd
2660-2	4096X1	TS	350/500	C	F, I, N	16	Yes	+12, ±5, Gnd
2660-3	4096X1	TS	140/375	C	F, I, N	16	Yes	+12, ±5, Gnd
2680	4096X1	TS	200/400	C	F, I, N	22	No	+12, ±5, Gnd
2680-1	4096X1	TS	270/470	C	F, I, N	22	No	+12, ±5, Gnd
2680-2	4096X1	TS	350/800	C	F, I, N	22	No	+12, ±5, Gnd
2627*	4096X1	—	150/320	C	F	16	—	+12, ±5, Gnd
2627-1*	4096X1	—	200/200	C	F	16	—	+12, ±5, Gnd
2627-2*	4096X1	—	250/250	C	F	16	—	+12, ±5, Gnd
2690*	16,384X1	—	150/375	C	—	16	—	+12, ±5, Gnd

*To be announced

NOTES

1. Output circuit:
   TS = Tri-state
   OD = Open drain
   BD = Bare drain
   PD = Pull down
   PP = Push-pull
2. Temperature range:
   C = Commercial (0 °C to +75 °C)
   M = Military (-55 ° C to +125 °C)

MOS MEMORY SELECTION GUIDE (Cont'd)

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	ACCESS/CYCLE TIME (ns)	TEMPERATURE RANGE[2]	PACKAGE	NO. OF PINS	CLOCK/CE/TTL COMPATABILITY	POWER SUPPLIES (V)
ROMS								
Static								
2530	512X8	TS	700/700	C	I, N	24	Yes	±5, -12
2609	128X9X7	TS	500/500	C	F, I, N	24	Yes	+5, Gnd
2607	1024X8	TS	500/500	C	F, I, N	24	Yes	+5, Gnd
2608	1024X8	TS	550/550	C	F, I, N	24	Yes	+5, Gnd
2608-1	1024X8	TS	450/450	C	F, I, N	24	Yes	+5, Gnd
2580	2048X4	TS	950/950	C	I, N	24	Yes	+5, -12
2600	2048X8	TS	500/500	C	F, I, N	24	Yes	+5, Gnd
2600-1	2048X8	TS	300/300	C	F, I, N	24	Yes	+5, Gnd
2616	2048X8	TS	450	C	F, I, N	24	Yes	+5, Gnd
2616-1	2048X8	TS	350	C	F, I, N	24	Yes	+5, Gnd
2617	2048X8	TS	450	C	F, I, N	24	Yes	+5, Gnd
2617-1	2048X8	TS	350	C	F, I, N	24	Yes	+5, Gnd
2632*	4096X8	—	500/500	C	I, N	24	—	+5, Gnd
2633*	4096X8	—	450/450	C	I, N	24	—	+5, Gnd
CHARACTER GENERATORS								
2513	64X8X5	TS	600/600	C	I, N	24	Yes	±5, -12
2516	64X6X8	TS	600/600	C	I, N	24	Yes	±5, -12
2526	64X9X9	TS	700/700	C	I, N	24	Yes	+5, -12
UV EPROMS								
1702A	256X8	TS	1000/1000	C	I	24	Yes	+5, -9
2704	512X8	TS	450/450	C	I	24	Yes	+12, ±5, Gnd
2708	1024X8	TS	450/450	C	I	24	Yes	+12, ±5, Gnd

STANDARD ROM CODE

DEVICE	CODE NO.	DESCRIPTION
STATIC ROM		
2530	CM3530	Code Converter, ASCH to EBCDIC and EBCDIC to ASCII
2608	CN0000	10X7 Upper and Lower Case ASCII Character Generator
2609	CN6571	128 ASCII Characters in 7X9 Matrix Count Down
	CN6571A	128 ASCII Characters in 7X9 Matrix Count Up
	CN6575	128 ASCII Characters in 7X9 Matrix Count Up with Special Characters
2580	CMXXXX	Random code pattern for evaluation purposes
CHARACTER GENERATOR		
2513	CM2140	New ASCII Character Generator, Upper Case, 7X5, Horizontal Scan
	CM2170	ASCII Character Generator, Upper Case with Yen Sign, 7X5, Horizontal Scan
	CM3021	ASCII Character Generator, Lower Case, 7X5, Horizontal Scan
	CM3030	Old ASCII Character Generator, Upper Case, 7X5, Horizontal Scan
	CM4800	Katakana Character Generator, 7X5, Horizontal Scan
2516	CM2150	ASCII Character Generator, Upper Case, 5X7, Vertical Scan
	CM3001/3010	ASCII Character Generator, Upper Case, 10X7, Vertical Scan (2 chips)
	CM3041	ASCII Character Generator, Lower Case, 10X7, Vertical Scan
	CM3970/3980	ASCII Character Generator, Upper Case, 12X8, Vertical Scan (2 chips)
2526	CM3400	ASCII Character Generator with EBCDIC and BAUDOT code translations, Upper Case, 7X9, Vertical Scan
	CM3940	ASCII Character Generator, Upper Case, 7X9, Horizontal Scan
	CM6760	Katakana Character Generator, 7X9, Horizontal Scan

*To be announced

NOTES

1. Output circuit:
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2. Temperature range:
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MOS MEMORY SELECTION GUIDE (Cont'd)

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	ON CHIP RECIRCULATE	TEMPERATURE RANGE[2]	PACKAGE	NO. OF PINS	NO. OF CLOCKS	TYPICAL SPEED (MHz)	CLOCK/CE/TTL COMPATABILITY	POWER SUPPLIES (V)
SHIFT REGISTERS										
Static										
2518	32X6	BD	Yes	C	N	16	1	3.0	Yes	+5, -12
2519	40X6	BD	Yes	C	N	16	1	3.0	Yes	+5, -12
2509	50X2	TS	Yes	C	N, K	14/10	1	3.0	Yes	+5, -5, -12
2532	80X4	PP	Yes	C	N	16	1	3.0	Yes	+5, -12
2510	100X2	TS	Yes	C	N, K	14/10	1	3.0	Yes	+5, -5, -12
2521	128X2	PP	Yes	C	N	8	1	3.0	Yes	+5, -12
2522	132X2	PP	Yes	C	N	8	1	3.0	Yes	+5, -12
2511	200X2	TS	Yes	C	N, K	14/10	1	3.0	Yes	+5, -5, -12
2527	240X2	PP	Yes	C	N	8	1	2.5	Yes	+5, -12
2528	250X2	PP	Yes	C	N	8	1	2.5	Yes	+5, -12
2529	256X2	PP	Yes	C	N	8	1	3.0	Yes	+5, -12
2533	1024X1	PP	Jumper	C	N	8	1	2.0	Yes	+5, -12
Dynamic										
2506	100X2	BD	No	C	T, N	8	2	4.0	No	+5, -5
2507	100X2	7.5KPD	No	C	T, N	8	2	4.0	No	+5, -5
2517	100X2	20KPD	No	C	T, N	8	2	4.0	No	+5, -5
2505	512X1	BD	Yes	C	K	10	2	3.0	No	+5, -5
2524	512X1	BD	Yes	C	N	8	2	5.0	No	+5, -5
2502	256X4	BD	No	C	N	16	2	10.0	No	+5, -5
2503	512X2	BD	No	C	TA, N	8	2	10.0	No	+5, -5
2504	1024X1	BD	No	C	TA, N	8	2	10.0	No	+5, -5
2512	1024X1	BD	Yes	C	K	10	2	5.0	No	+5, -5
2525	1024X1	BD	Yes	C	N	8	2	3.0	No	+5, -5

*To be announced

NOTES

1. Output circuit
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   M = Military (-55 °C to +125 °C)

7400 SERIES

DEVICE	DESCRIPTION	7400		74H		74LS		74S	
		PLASTIC	CERDIP	PLASTIC	CERDIP	PLASTIC	CERDIP	PLASTIC	CERDIP
74178	4-Bit Parallel Access Shift Reg (8270)	N	F	—	—	—	—	N	F
74179	4-Bit Parallel Access Shift Register (8271)	N	F	—	—	—	—	N	F
74180	8-Bit Odd/Even Parity Checker	N	F	—	—	—	—	—	—
74181	4-Bit Arithmetic Logic Unit	N	F	—	—	N	F	N	F
74182	Look-Ahead Carry Generator	N	F	—	—	—	—	N	F
74190	Synchronous Up/Down Counter (BCD)	N	F	—	—	N	F	—	—
74191	Synchronous Up/Down Counter (Binary)	N	F	—	—	N	F	—	—
74192	Synchronous Decade Up/Down Counter	N	F	—	—	N	F	—	—
74193	Synchronous 4-Bit Binary Up/Down Counter	N	F	—	—	N	F	—	—
74194	4-Bit Bidirectional Universal Shift Reg.	N	F	—	—	N	F	N	F
74195	4-Bit Parallel-Access Shift Register	N	F	—	—	N	F	N	F
74196	Presettable Decade Counter/Latch (8290)	N	F	—	—	N	F	N	F
74197	Presettable Binary Counter/Latch (8291)	N	F	—	—	N	F	N	F
74198	8-Bit Shift Register	N	F	—	—	—	—	—	—
74199	8-Bit Shift Register	N	F	—	—	—	—	—	—
74221	Dual Monostable Multivibrator	N	F	—	—	N	F	—	—
74251	Data Selector/Mux with 3-State Outputs	—	—	—	—	N	F	N	F
74253	Dual 4-Line to 1-Line Data Selector/Mux	—	—	—	—	N	F	N	F
74257	Quad 2-Line to 1-Line Data Selector/Mux	—	—	—	—	N	F	N	F
74258	Quad 2-Line to 1-Line Data Selector/Mux	—	—	—	—	N	F	N	F
74260	Dual 5-Input NOR Gate	—	—	—	—	N	F	N	F
74261	2X4 Parallel Binary Multiplier	—	—	—	—	N	F	—	—
74266	Quad Exclusive NOR Gate	—	—	—	—	N	F	—	—
74273	Octal D Flip-Flop	—	—	—	—	N	F	—	—
74279	Quad S-R Latch	N	F	—	—	—	—	—	—
74280	9-Bit Odd/Even Parity Generator/Checker	—	—	—	—	—	—	N	F
74283	4-Bit Adder	—	—	—	—	N	F	—	—
74290	Decade Counter	—	—	—	—	N	F	—	—
74293	4-Bit Binary Counter	—	—	—	—	N	F	—	—
74295A	4-Bit Right-Shift Left-Shift Register	—	—	—	—	N	F	—	—
74298	Quad 2-Input Mux with Storage	N	F	—	—	N	F	—	—
74365	Hex Buffer w/Common Enable (3-State)	N	F	—	—	N	F	—	—
74366	Hex Buffer w/Common Enable (3-State)	N	F	—	—	N	F	—	—
74367	Hex Buffer, 4-Bit and 2-Bit (3-State)	N	F	—	—	N	F	—	—
74368	Hex Inverter, 4-Bit and 2-Bit (3-State)	N	F	—	—	N	F	—	—
74375	Quad Latch	—	—	—	—	N	F	—	—
74377	Octal D Flip-Flop	—	—	—	—	N	F	—	—
74386	Quad Exclusive-OR Gate	—	—	—	—	N	F	—	—
74395	4-Bit Cascadeable Shift Register (3-State)	—	—	—	—	N	F	—	—
74670	4X4 Register File (Tri-state)	—	—	—	—	N	F	—	—

LOGIC—8200/9300/9600 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED*		JAN PROCESSED		MIL REL/883 MIL TEMP	
			Dip	Flat Pack	Dip	Flat Pack	Dip	Flat Pack
8200	Dual 5-Bit Buffer Register	—	—	—	—	—	I	Q
8201	Dual 5-Bit Buffer Register with D Inputs	—	—	—	—	—	I	Q
8202	10-Bit Buffer Register	—	—	—	—	—	I	Q
8203	10-Bit Buffer Register with D Inputs	—	—	—	—	—	I	Q
8230	8-Input Digital Multiplexer	/01402	*	*	F	W	F	W
8231	8-Input Digital Multiplexer	—	—	—	—	—	F	W
8232	8-Input Digital Multiplexer	—	—	—	—	—	F	W
8233	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8234	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8235	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8241	Quad Exclusive-OR Gate	—	—	—	—	—	F	W
8242	Quad Exclusive-NOR Gate	—	—	—	—	—	F	W
8243	8-Bit Position Scaler	—	—	—	—	—	I	Q
8250	Binary-to-Octal Decoder	/15204	2	2	F	W	F	W
8251	BCD-to-Decimal Decoder	/15205	2	2	F	W	F	W
8252	BCD-to-Decimal Decoder	/15206	2	2	F	W	F	W
8260	Arithmetic Logic Unit	—	—	—	—	—	I	Q
8261	Fast Carry Extender	—	—	—	—	—	F	W
8262	9-Bit Parity Generator and Checker	—	—	—	—	—	F	W
8263	3-Input 4-Bit Digital Multiplexer	—	—	—	—	—	I	Q
8264	3-Input 4-Bit Digital Multiplexer		—	—	—	—	I	Q
8266	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8267	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8268	Gated Full Adder	—	—	—	—	—	F	Q
8269	4-Bit Comparator	—	—	—	—	—	F	W
8270	4-Bit Shift Register	—	—	—	—	—	F	W
8271	4-Bit Shift Register	—	—	—	—	—	F	W
8273	10-Bit Serial-In, Parallel-Out Shift Register	—	—	—	—	—	F	W
8274	10-Bit Parallel-In, Serial-Out Shift Register	—	—	—	—	—	F	W
8275	Quad Bistable Latch	—	—	—	—	—	F	W
8276	8-Bit Serial Shift Register	—	—	—	—	—	F	—
8277	Dual 8-Bit Shift Register	—	—	—	—	—	F	—
8280	Presettable Decade Counter	—	—	—	—	—	F	W
8281	Presettable Binary Counter	—	—	—	—	—	F	W
8284	Binary Up/Down Counter	—	—	—	—	—	F	W
8285	Decade Up/Down Counter	—	—	—	—	—	F	W
8288	Divide-by-Twelve Counter	—	—	—	—	—	F	W
8290	Presettable High Speed Decade Counter	—	—	—	—	—	F	W
8291	Presettable High Speed Binary Counter	—	—	—	—	—	F	W
8292	Presettable Low Power Decade Counter	—	—	—	—	—	F	W
8293	Presettable Low Power Binary Counter	—	—	—	—	—	F	W
9300	4-Bit Shift Register	/15901	*	*	F	W	F	W
9301	BCD to Decimal Decoder	/15206	2	2	F	W	F	W
9308	Dual 4-Bit Latch w/Clear	—	—	—	—	—	I	Q
9309	Dual 4-Input Multiplexer	/01404	I	I	F	W	F	W
9310	4-Bit Decade Counter	—	—	—	—	—	F	W
9312	8-Input Digital Multiplexer	/01402	*	*	F	W	F	W
9316	4-Bit Binary Counter	—	—	—	—	—	F	W
9322	Data Selector-Multiplexer	—	—	—	—	—	F	W
9324	5-Bit Comparator	/15002	*	*	F	WF	W	—
9334	8-Bit Addressable Latch	/16001	—	—	—	—	F	W
9602	Dual Monostable Multivibrator	—	*	*	F	W	F	W

NOTE

Per QFL 38510-28 dated 1 Apr. 1977
1 = Level 1 Qualification
2 = Level 2 Qualification

8T00 SERIES INTERFACE

The 8T00 Series provide a line of integrated circuits for applications such as line driving and receiving, level shifting and tri-state bus interfacing. Both Gold Doped and Schottky technologies are used to produce these devices.

DEVICE	DESCRIPTION	PLASTIC	CERAMIC
8T04	7-Segment Decoder Display Driver (Active-Low Outputs)	N	F
8T05	7-Segment Decoder Display Driver (Active-Hi Outputs)	N	F
8T06	7-Segment Decoder Display Driver (Active-Low Outputs)	N	F
8T09	Quad Bus Driver with Tri-State Outputs	N	F
8T10	Quad D-Type Bus Latch (Tri-State)	N	F
8T13	Dual Line Driver	N	F
8T14	Triple Line Receiver/Schmitt Trigger	N	F
8T15	Dual Communications EIA/MIL Line Driver	N	F
8T16	Dual Communications EIA/MIL Line Receiver	N	F
8T18	Dual 2-Input NAND (High Voltage to TTL Interface)	N	F
8T20	Bidirectional Monostable Multivibrator (Diff. Input)	N	F
8T22	Retriggerable Monostable Multivibrator (74122/9601)	N	F
8T23	Dual Line Driver for IBM 360/370 Interface (75123)	N	F
8T24	Triple Line Receiver for IBM 360/370 Interface (75124)	N	F
8T25	Dual MOS Sense Amplifier with Latch (Tri-State Outputs)	V	—
8T26A	Quad Bus Driver/Receiver (Tri-State Outputs)	N	F
8T28	Quad Non-Inverting Bus Driver/Receiver (Tri-State Outputs)	N	F
8T30	Dual TTL/DTL to MOS Transceiver/Port Controller	N	F
8T31	8-Bit Bidirectional I/O Port	N	F
8T32	Programmable 8-Bit I/O Port (3-State)	N	F
8T33	Programmable 8-Bit I/O Port (Open Collector)	N	F
8T34	Quad Bus Transceiver (DM8834)	N	F
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	N	F
8T36	Asynchronous Programmable 8-Bit I/O Port (3-State)	N	F
8T37	Hex Bus Receiver with Hysteresis—Schmitt Trigger (DM8837)	N	F
8T38	Quad Bus Transceiver (Open Collector) (DM8838)	N	F
8T39	Bus Extender/Repeater	N	F
8T40	Pipeline I/O Port	N	F
8T58	Working Storage Bus Extender	N	F
8T80	Quad 2-Input NAND Gate (High Voltage)	N	F
8T90	Hex Inverter (High Voltage)	N	F
8T95	High Speed Hex Buffers/Inverters (74365/DM8095)	N	F
8T96	High Speed Hex Buffers/Inverters (74366/DM8096)	N	F
8T97	High Speed Hex Buffers/Inverters (74367/DM8097)	N	F
8T98	High Speed Hex Buffers/Inverters (74368/DM8098)	N	F
8T363	Dual Zero Crossing Detector	N	—
8T380	Quad Bus Receiver with Hysteresis	N	F

ANALOG (LINEAR)

CONSUMER/COMMUNICATION CIRCUITS	
NE/SE540	Power Driver
NE541	Power Driver
NE542	Dual Preamp
NE543	Servo Amplifier
NE544/644	Servo Amplifier
NE546	AM Radio
NE570/571	Analog Compandor
N/S5596	Balanced Modulator/Demodulator
μA758	Stereo Decoder
ULN2111	FM Detector/Limiter
ULN2208	FM Gain Block
ULN2209	FM Gain Block
ULN2211	TV Sound Channel
TBA120S/U	TV Sound IF
TBA1440	TV Video IF
TBA327/395/396	TV PAL Chroma Set
TCA440	AM Receiver
TDA2541	TV Video IF
CA3089	FM IF System
PA239	Dual Preamp
LM381, 381A	Dual Preamp
LM382	Dual Preamp
LM387	Dual Preamp
MC1496/1596	Balanced Modulator/Demodulator

Also see D-MOS FETs

OP AMPS	
NE/SE531	High Slew Rate Op Amp
*NE/SE/SA532	Dual Op Amp
NE/SE532A	Dual Op Amp
*NE/SE535	High Slew Rate Op Amp
NE/SU536	FET Input Op Amp
NE/SE538	High Slew Rate Op Amp
NE/SE5534	Low Noise Op Amp
*MC1456/1556	High Performance Op Amp
*MC1458/1558/SA1458	Dual Op Amp
*μA709/709C/SA709C	Op Amp
μA740C	FET Input Op Amp
*μA741/741C/SA741C	General Purpose Op Amp
*μA747/747C/SA747C	Dual Op Amp
*μA748/748C/SA748C	General Purpose Op Amp
LF155/255/355	BIFET Input Op Amp
LF156/256/356	BIFET Input Op Amp
LF157/257/357	BIFET Input Op Amp
*LM101/201	High Performance Op Amp
*LM101A/201A/301A	High Performance Op Amp
*LM107/207/307	General Purpose Op Amp
*LM108/208/308	Precision Op Amp
*LM108A/208A/308A	Precision Op Amp
*LM124/224/324	Quad Op Amp
LM124A/224A/324A	Quad Op Amp
*LM158/258/358	Dual Op Amp
SA1458	Dual Op Amp
SA534	Quad Op Amp
*SA709	Op Amp
*SA741	General Purpose Op Amp
*SA747	Dual Op Amp

PERIPHERAL INTERFACE	
NE/SE501	Video Amp
NE/SE592	Video Amp
*μA733/733C	Video Amp
55450B/51B/52B/53B/54B	Dual Peripheral Drivers
75450B/51B/52B/53B/54B	Dual Peripheral Drivers
DS3611/12/13/14	Dual Peripheral Drivers—80V Output
UDN5711/12/13/14	Dual Peripheral Drivers—80V Output
MC1488	Quad Line Driver
MC1489/1489A	Quad Line Receiver
75S107/108	Dual Line Receiver
*DM7820/8820	Dual Differential Line Receiver
*DM7820A/8820A	Dual Differential Line Receiver
*DM7830/8830	Dual Differential Line Driver

DISPLAY INTERFACE	
DM8880	Display Decoder Driver
DM8880-1	Display Decoder Driver—100V Outputs
NE584	Gas Discharge Segment Driver
NE585	Gas Discharge Digit Driver
NE582	LED Digit Driver

MEMORY INTERFACE	
3207A	MOS Clock Driver
3207A-1	MOS Clock Driver
7520	Dual Core Memory Sense Amp
7522	Dual Core Memory Sense Amp
7524	Dual Core Memory Sense Amp
7528	Dual Core Memory Source Amp
75232	Dual Core Memory Source Amp
75234	Dual Core Memory Source Amp
75S207/208	Dual MOS Memory Sense Amp
75324	Core Memory Driver
55/75325	Switched Paid Quad Core Driver

MOSFET-ANALOG/DIGITAL SWITCHES (D-MOS)	
*SD210/211	Switch Driver
*SD212/213	Switch
*SD214/215	Switch
*SD5000/5001/5002	Quad Switch Array IC
*SD5100/5101	Quad Multiplexer IC
*SD5200	Quad Switch Driver IC
*SD5301	8x2 Crosspoint Switch
SD5350	8 Channel Multiplexer w/Shift Register Control
DMP/DMS4025	Power FET

D/A/D CONVERTERS	
MC1408-7	8-Bit D/A Converter, 1 LSB Accuracy
MC1408-8	8-Bit D/A Converter, ½ LSB Accuracy
MC1508-8	8-Bit D/A Converter, ½ LSB Accuracy
NE5007	8-Bit D/A Converter, 1 LSB Accuracy
NE/SE5008	8-Bit D/A Converter, ½ LSB Accuracy
NE/SE5009	8-Bit D/A Converter, ¼ LSB Accuracy

*Available with Military processing (see Military section)

ANALOG (LINEAR) (Cont'd)

MOSFET-RF (D-MOS)	
SD200/201	Single Gate UHF
SD202/203	Single Gate UHF
SD300	Dual Gate UHF
SD303	Dual Gate UHF
SD304	Dual Gate VHF
SD305	Dual Gate VHF Mixer
SD306	Dual Gate VHF Amp
SD6000	VHF Mixer/Amp IC
DMP/DMS4025	Power FET

TIMERS	
NE/SE/SA558	Quad Timer
NE/SE/SA559	Quad Timer
*NE/SE/SA555	Timer
*NE/SE/SA556	Dual Timer

PHASE LOCKED LOOPS	
NE560	Phase Locked Loop
NE561	Phase Locked Loop
NE562	Phase Locked Loop
NE/SE564	Phase Locked Loop
NE/SE565	Phase Locked Loop
NE/SE566	Function Generator
*NE/SE567	Tone Decoder PLL

HYBRIDS	
*LH2101AF	Dual Op Amp
*LH2108F	Dual Precision Op Amp
*LH2108AF	Dual Precision Op Amp
*LH2111AF	Dual Comparator

TRANSISTOR ARRAYS	
ULN2001/2/3/4	Darlington Transistor Array
N5501/2/3/4	High Voltage Darlington Transistor Array

DIFFERENTIAL AMPLIFIERS	
*NE/SE510	Dual Differential Amp
*NE/SE511	Dual Differential Amp
*NE/SE515	Differential Amp
*μA733	Video Amp

VOLTAGE REGULATORS	
*LM109/209/309	5V Voltage Regulator
NE/SE550	Precision Voltage Regulator
*μA723/723C/SA723	Precision Voltage Regulator
μA78L02/05/06/08/12/15	Three-Terminal Positive Voltage Regulators
μA7805/06/08/12/14 15/18/24	Three-Terminal Positive Voltage Regulators
μA78HV05/06/08/12/14/15/18/24	High Input Breakdown (1 Amp) Positive Voltage Regulators
μA78M05/06/08/12/15/20/24	Three-Terminal Positive Voltage Regulators
μA78MHV05/06/08/12/15/20/24	High Input Breakdown (500mA) Positive Voltage Regulators
μA7905/5.2/06/08/12/15/18/24	Three Terminal Negative Voltage Regulator
μA79M05/06/08/12/15/20/24	Three Terminal Negative Voltage Regulator (500mA)
μA78G	1 Amp Adjustable Positive Voltage Regulator
μA78MG	500mA Adjustable Positive Voltage Regulator
μA79G	1 Amp Adjustable Negative Voltage Regulator
μA79MG	500mA Adjustable Negative Voltage Regulator
*LM340-05/06/08/12/15/18/24	Voltage Regulator
SE/NE5554	Dual Tracking Regulator

COMPARATORS	
*NE521/522	High Speed Dual Differential Comparator
*NE/SE526	Analog Voltage Comparator
*NE/SE527	High Speed Voltage Comparator
*NE/SE529	High Speed Voltage Comparator
*μA710/710C	Voltage Comparator
*μA711/711C	Dual Voltage Comparator
*LM111/211/311	Voltage Comparator
*LM119/219/319	Dual Voltage Comparator
*LM139/239/339	Quad Voltage Comparator
*LM139A/239A/339A	Quad Voltage Comparator
LM193/293/393	Dual Voltage Comparator
LM2903	Dual Voltage Comparator
MC3302	Quad Voltage Comparator
SA539	Quad Voltage Comparator

*Available with Military processing (see Military section).

MILITARY

INTRODUCTION

Manufacturing integrated circuits to the stringent requirements of the Defense and Aerospace industries has been a dedication of Signetics since its founding in 1961. Today, Signetics remains unchanged in charter and continues to produce integrated circuits for this market segment with state-of-the-art process technologies which result in unequalled overall reliability.

Signetics' dedicated approach to the military market is evidenced by the fact that it is the only major semiconductor manufacturer with a separate Military Products Division—with its own production facilities, engineering staff and marketing organization. Rather than dealing with each individual product division, as they must at many companies, Signetics' military customers can deal with one group of personnel familiar with the company's broad product capability as well as with the special requirements of the military market.

Assessing the individual products of any high-reliability supplier is enhanced by a complete understanding of the company's technological processes and the degree of its commitment to quality control and reliability.

PROCESSING LEVELS AND REQUIREMENTS

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics Mil 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customers to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3 and 4.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES				
			Dual-In-Line		
	8-Pin	10-Pin	14-Pin	16-Pin	24-Pin
CB	—	—	F	—	—
EB	—	—	—	F	—
JB	—	—	—	—	I/F*
DB	—	—	W	—	—
FB	—	—	—	W	—
ZC	—	—	—	—	Q
GC	T	—	—	—	—
IC	—	K	—	—	—

*The gold plated versions of these packages will be available for a limited time.
All products listed in Military section are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	JBX	RBX	RB	S
	JAN Qualified	JAN Processed	JAN Rel	/883	Mil Temp
54/54H	X	X	X	X	X
54LS	X	X	X	X	X
54S	X	X	X	X	X
82/8T	X	X	X	X	X
93XX	X	X	X	X	X
96XX	—	—	X	X	X
Linear	Planned	X	X	X	X
Bipolar Memory	Planned	—	X	X	X
Microprocessor	—	—	X	X	X

Table 2 MILITARY SUMMARY

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

JAN PROCESSING (JBX)

This option is extremely useful when the reliability and screening of a JAN device is required, however, Signetics is not listed on the QPL for the product needed. Processing is performed to Mil-Std-883 Method 5004, and product is 100% electrically tested to the appropriate JAN slash sheet.

Group B, C and D data for JAN processed and the other military processing levels which follow, consist of Group B, C and D testing performed per Mil-Std-883 Method 5005, in accordance with the Signetics Military Data Program. Offshore assembly is allowed.

JAN REL (RBX)

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets.

/883B (RB)

This is a lower priced version of the JAN Rel option described above. Processing is identical with the only exceptions being the dc electrical testing over the temperature range and ac electrical testing at room temperature are performed as a part of Group A instead of 100%.

MIL TEMP/883C (S/RC)

If you need a Military temp. range device, but do not require all the high reliability screening performed in the other processing options, our Mil-Temp. product is ideal. Mil-Temp. parts are the standard full Mil-Temperature range product guaranteed to a 1% AQL to the Signetics data sheet parameters.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet
- Mil-M-38510 and customer reliability requirements.
  Provides an attributes summary to the customer backed by lot identity and traceability.

PROCESS LEVEL AND MARKING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFF SHORE
JB JM38510/XXXXX	883B	Yes	100%	100%	100%	Yes	No
JBX M38510/XXXXX	883B	Yes	100%	100%	100%	No	Yes
RBX M38510/P/N	883B	Yes	100%	100%	100%	No	Yes
RB SXXXX/883B	883B	Yes	100%	100% dc Sample ac	Sample dc only	No	Yes
RC/S SXXXX/883C	883B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied.	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*
Group A is performed on each lot or sublot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS					
			CLASS A	JAN Qualified (JB)	JAN Processed (JBX)	JAN Rel (RBX)	/883B (RB)	/883C (RC)
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program Plan B. Manufacturer's Certification	The manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A	N/A	N/A
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A	N/A	N/A
Screening Per Method 5004 of Mil-Std-883								
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X	X	X
8. Temperature Cycling* *For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)	1010, Cond. C; (10 cycles, -65°C to +150°C)	100%	X	X	X	X	X	X
9. Constant Acceleration	2001, Cond. E; (30_{kg} in YI Plane)	100%	X	X	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X	X	X
11. Seal (Hermeticity) A. Fine B. Gross	1014 Cond. A or B (5.0 X 10^{-8}CC/Sec) Cond. C2 Min.	 100% 100%	 X X	 X X	 X X	 X X	 X X	 X X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Slash Sheet	Data Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Slash Sheet	Data Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	X	N/A	N/A
C. Static Tests @ -55°C	Sub Group 3		X	X	X	X	N/A	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS					
			CLASS A	JAN Qualified (JB)	JAN Processed (JBX)	JAN Rel (RBX)	/883B (RB)	/883C (RC)
D. Dynamic Test @ 25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X	X	X
E. Functional Test @ 25°C	Sub Group 7		X	X	X	X	X	X
F. Switching Test @ 25°C	Sub Group 9		X	X	X	X	N/A	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @ 25°C (A-1). This is controlled by the slash sheets for JB & JBX products. For RBX & RB 10% is standard.	10%	5%	X	X	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/ XXXX Slash Sheet #	M38510/ XXXX Slash Sheet #	M38510/ SXXXX Sig. Basic #	SXXXX/ 883B Sig. Basic #	SXXXX/ 883C Sig. Basic #
17. X-Ray	2012		100%	N/A	N/A	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std-883								
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per microcircuit group	X	X	Generic Data Available			
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constant acceleration.	Every 3 months per package type	X	X	Generic Data Available			
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available			

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS (Cont'd)

LOGIC

LOGIC—54LS SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54LS00	Quad 2-Input NAND Gate	/30001	2	2	F	W	F	W
54LS01	Quad 2-Input NAND Gate with o/c	—	—	—	F	W	F	W
54LS02	Quad 2-Input NOR Gate	/30301	2	2	F	W	F	W
54LS03	Quad 2-Input NAND Gate with o/c	/30002	1	1	F	W	F	W
54LS04	Hex Inverter	/30003	1	1	F	W	F	W
54LS05	Hex Inverter with o/c	/30004	1	1	F	W	F	W
54LS08	Quad 2-Input AND Gate	/31004	2	2	F	W	F	W
54LS09	Quad 2-Input AND Gate with o/c	—	—	—	—	—	F	W
54LS10	Triple 3-Input NAND Gate	/30005	1	1	F	W	F	W
54LS11	Triple 3-Input NAND Gate	/31001	2	2	F	W	F	W
54LS12	Triple 3-Input NAND Gate with o/c	/30006	1	1	F	W	F	W
54LS13	Dual NAND Schmitt Trigger	/31301	*	*	F	W	F	W
54LS14	Hex Schmitt Trigger	/31302	*	*	F	W	F	W
54LS15	Triple 3-Input AND Gate with o/c	/31002	2	2	F	W	F	W
54LS20	Dual 4-Input NAND Gate	/30007	1	1	F	W	F	W
54LS21	Dual 4-Input AND Gate	/31003	2	2	F	W	F	W
54LS22	Dual 4-Input NAND Gate with o/c	/30008	1	1	F	W	F	W
54LS26	Quad 2-Input NAND Gate with o/c	/32101	*	*	F	W	F	W
54LS27	Triple 3-Input NOR Gate	/30302	2	2	F	W	F	W
54LS28	Quad 2-Input NOR Buffer	/30204	*	*	F	W	F	W
54LS30	8-Input NAND Gate	/30009	2	2	F	W	F	W
54LS32	Quad 2-Input OR Gate	/30501	2	2	F	W	F	W
54LS33	Quad 2-Input NOR Buffer with o/c	—	—	—	—	—	F	W
54LS37	Quad 2-Input NAND Buffer	/30202	2	2	F	W	F	W
54LS38	Quad 2-Input NAND Buffer with o/c	/30203	*	*	F	W	F	W
54LS40	Dual 4-Input NAND Buffer	/30201	2	2	F	W	F	W
54LS42	BCD-to-Decimal Decoder	/30703	*	*	*	*	F	W
54LS51	Dual 2-Wide 2-Input A01 Gate	/03401	2	2	F	W	F	W
54LS54	4-Wide 2-Input A01 Gate	/30402	2	2	F	W	F	W
54LS55	2-Wide 4-Input A01 Gate	—	—	—	—	—	F	W
54LS73	Dual J-K Master-Slave Flip-Flop	/30101	—	—	—	—	F	W
54LS74	Dual D-Type Edge-Triggered Flip-Flop	/30102	*	*	F	W	F	W
54LS75	Quad Bistable Latch	—	—	—	F	W	F	W
54LS76	Dual J-K Master-Slave Flip-Flop	/30110	*	*	F	W	F	W
54LS78	Quad Bistable Latch	—	—	—	—	—	F	W
54LS83A	4-Bit Binary Full Adder	/31201	*	*	F	W	F	W
54LS85	4-Bit Magnitude Comparator	/31101	*	*	F	W	F	W
54LS86	Quad 2-Input Exclusive-OR Gate	/30502	*	*	F	W	F	W
54LS90	Decade Counter	/31501	*	*	F	W	F	W
54LS92	Divide-by-Twelve Counter	/31510	*	*	F	W	F	W
54LS93	4-Bit Binary Counter	/31502	*	*	F	W	F	W
54LS95	4-Bit Left-Right Shift Register	/30603	*	*	F	W	F	W
54LS96	5-Bit Shift Register	/30604	*	*	F	W	F	W

NOTE

Per QPL 38510-28 dated 1 April 1977.

1 = Level 1 Qualification
2 = Level 2 Qualification
* = In Process

LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54LS107	Dual J-K Master-Slave Flip-Flop	/30108	*	*	F	W	F	W
54LS109	Dual J-K Positive Edge-Triggered Flip-Flop	/30109	*	*	F	W	F	W
54LS112	Dual J-K Negative Edge-Triggered Flip-Flop	/30103	*	*	F	W	F	W
54LS113	Dual J-K Negative Edge-Triggered Flip-Flop	/30104	*	*	F	W	F	W
54LS114	Dual J-K Negative Edge-Triggered Flip-Flop	/30105	*	*	F	W	F	W
54LS122	Retriggerable Monostable Multivibrator	/31403	—	—	—	—	—	—
54LS125	Quad Bus Buffer Gate w/Tri-State Outputs	/32301	*	*	*	*	F	W
54LS126	Quad Bus Buffer Gate w/Tri-State Outputs	/32302	*	*	*	*	F	W
54LS132	Quad Schmitt Trigger	/31303	*	*	F	W	F	W
54LS136	Quad Exclusive-OR with o/c	—	—	—			F	W
54LS138	3-to-8 Line Decoder/Demux	/30701	*	*	*	*	F	W
54LS139	Dual 2-to-4 Line Decoder/ Demux	/30702	*	*	*	*	F	W
54LS145	BCD to Decimal Decoder/Dye	—	—	—	—	—	F	W
54LS151	8-Line to 1-Line Mux	/30901	*	*	*	*	*	*
54LS153	Dual 4-Line to 1-Line Mux	/30902	*	*	F	W	F	W
54LS154	4-Line to 16-Line Decoder/ Demux	—	—	—	—	—	I	Q
54LS155	Dual 2-Line to 4-Line Decoder/Demux	—	—	—	—	—	F	W
54LS157	Quad 2-Input Data Selector (non-inv.)	/30903	*	*	F	W	F	W
54LS158	Quad 2-Input Data Selector (inv.)	/30904	*	*	F	W	F	W
54LS160	Synchronous 4-Bit Decade Counter	/31503	*	*	*	*	F	W
54LS161	Synchronous 4-Bit Binary Counter	/31504	*	*	F	W	F	W
54LS162	Synchronous 4-Bit Decade Counter	/31511	*	*	*	*	F	W
54LS163	Synchronous 4-Bit Binary Counter	/31512	*	*	*	*	F	W
54LS164	8-Bit Parallel-Out Serial Shift Register	/30605	*	*	F	W	F	W
54LS170	4X4 Register File	—	—	—	—	—	F	W
54LS173	Quad D-Type Flip-Flop (Tri-State) (8T10)	—	—	—	—	—	F	W
54LS174	Hex D-Type Flip-Flop with Clear	/30106	*	*	F	W	F	W
54LS175	Quad D-Type Edge-Triggered Flip-Flop	/30107	*	*	F	W	F	W
54LS181	4-Bit Arithmetic Logic Unit	/30801	2	—	I	—	I	Q
54LS190	Synchronous Up/Down Counter (BCD)	/31513	*	*	F	W	F	W
54LS191	Synchronous Up/Down Counter (Binary)	/31509	*	*	F	W	F	W

NOTE
Per QPL 38510-28 dated 1 April 1977.
1 = Level 1 Qualification
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* = In Process

LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54LS192	Synchronous Decade Up/Down Counter	/31507	*	*	F	W	F	W
54LS193	Synchronous 4-Bit Binary Up/Down Counter	/31508	*	*	F	W	F	W
54LS194	4-Bit Bidirectional Universal Shift Register	/30601	*	*	*	*	*	*
54LS195	4-Bit Parallel-Access Shift Register	/30602	*	*	*	*	*	*
54LS196	Presettable Decade Counter/ Latch (8290)	/31601	*	*	*	*	*	*
54LS197	Presettable Binary Counter/ Latch (8291)	/31602	*	*	*	*	*	*
54LS221	Dual Monostable Multivibrator	/31402	*	*	*	*	*	*
54LS251	Data Selector/Mux with 3-State Outputs	/30905	*	*	*	*	*	*
54LS253	Dual 4-Line to 1-Line Data Selector/Mux	/30908	*	*	F	W	F	W
54LS257	Quad 2-Line to 1-Line Data Selector/Mux	/30906	*	*	F	W	F	W
54LS258	Quad 2-Line to 1-Line Data Selector/Mux	/30907	*	*	*	*	F	W
54LS260	Dual 5-Input NOR Gate	—	—	—	—	—	F	W
54LS261	2X4 Parallel Binary Multiplier	—	—	—	—	—	F	W
54LS266	Quad Exclusive-NOR Gate	/30303	2	2	F	W	F	W
54LS279	Quad S-R Latch	—	—	—	—	—	F	W
54LS280	9-Bit Odd/Even Parity Generator/Checker	—	—	—	—	—	*	*
54LS283	4-Bit Adder	/31202	*	*	*	*	F	W
54LS290	Decade Counter	/32003	*	*	F	W	F	W
54LS293	4-Bit Binary Counter	/32004	*	*	F	W	F	W
54LS295A	4-Bit Right-Shift Left-Shift Register	/30606	*	*	*	*	F	W
54LS298	Quad 2-Input Mux with Storage	—	—	—	—	—	F	W
54LS365	Hex Buffer w/Common Enable (3-State)	/32201	*	*	*	*	F	W
54LS366	Hex Buffer w/Common Enable (3-State)	/32202	*	*	*	*	F	W
54LS367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32203	*	*	*	*	F	W
54LS368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32204	*	*	*	*	F	W
54LS375	Quad Latch	—	—	—	—	—	F	W
54LS386	Exclusive-OR Gate	—	—	—	—	—	F	W
54LS395	4-Bit Cascadeable Shift Register (3-State)	/30607	*	*	*	*	F	W
54LS445	BCD to Decimal Decoder/Dye	—	—	—	—	—	F	W
54LS670	4X4 Register File (Tri-State)	—	—	—	—	—	F	W

NOTE

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1 = Level 1 Qualification
2 = Level 2 Qualification
* = In Process

LOGIC—54S SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54S00	Quad 2-Input NAND Gate	/07001	1	1	F	W	F	W
54S02	Quad 2-Input NOR Gate	/07301	2	2	F	W	F	W
54S03	Quad 2-Input NAND Gate with o/c	/07002	2	2	F	W	F	W
54S04	Hex Inverter	/07003	1	1	F	W	F	W
54S05	Hex Inverter with o/c	/07004	1	1	F	W	F	W
54S08	Quad 2-Input AND Gate	/08003	*	*	F	W	F	W
54S09	Quad 2-Input AND Gate with o/c	/08004	—	—	—	—	F	W
54S10	Triple 3-Input NAND Gate	/07005	2	2	F	W	F	W
54S11	Triple 3-Input NAND Gate	/08001	2	2	F	W	F	W
54S15	Triple 3-Input AND Gate with o/c	/08002	2	2	F	W	F	W
54S20	Dual 4-Input NAND Gate	/07006	2	2	F	W	F	W
54S22	Dual 4-Input NAND Gate with o/c	/07007	1	1	F	W	F	W
54S30	8-Input NAND Gate	/07008	—	—	—	—	—	—
54S32	Quad 2-Input OR Gate	—	—	—	—	—	F	W
54S40	Dual 4-Input NAND Buffer	/07201	2	2	F	W	F	W
54S51	Dual 2-Wide 2-Input A01 Gate	/07401	2	2	F	W	F	W
54S64	4-2-3-2 Input A01 Gate	/07402	2	2	F	W	F	W
54S65	4-2-3-2 Input A01 Gate	/07403	2	2	F	W	F	W
54S74	Dual D-Type Edge-Triggered Flip-Flop	/07101	2	2	F	W	F	W
54S85	4-Bit Magnitude Comparator	/08201	*	—	F	—	F	—
54S86	Quad 2-Input Exclusive-OR Gate	/07501	2	2	F	W	F	W
54S112	Dual J-K Negative Edge-Triggered Flip-Flop	/07102	—	—	—	—	F	W
54S113	Dual J-K Negative Edge-Triggered Flip-Flop	/07103	—	—	—	—	F	W
54S114	Dual J-K Negative Edge-Triggered Flip-Flop	/07104	—	—	—	—	F	W
54S133	13-Input NAND Gate	/07009	2	2	F	W	F	W
54S134	12-Input NAND Gate w/Tri-State Outputs	/07010	2	2	F	W	F	W
54S135	Quad Exclusive-OR/NOR Gate	/07502	—	—	—	—	—	—
54S138	3-to-8 Line Decoder/Demux	/07701	—	—	—	—	—	—
54S139	Dual 2-to-4 Line Decoder/ Demux	/07702	—	—	—	—	F	W
54S140	Dual 4-Input NAND Line Driver	/08101	2	2	F	W	F	W
54S151	8-Line to 1-Line Mux	/07901	2	2	F	W	F	W
54S153	Dual 4-Line to 1-Line Mux	/07902	2	2	F	W	F	W
54S157	Quad 2-Input Data Selector (non.inv.)	/07903	2	2	F	W	F	W
54S158	Quad 2-Input Data Selector (inv.)	/07904	*	*	F	W	F	W
54S174	Hex D-Type Flip-Flop with Clear	/07106	—	—	—	—	*	*
54S175	Quad D-Type Edge-Triggered Flip-Flop	/07105	—	—	—	—	*	*
54S181	4-Bit Arithmetic Logic Unit	/07801	*	—	I	—	I	*
54S182	Look-Ahead Carry Generator	/07802	—	—	—	—	*	*
54S194	4-Bit Bidirectional Universal Shift Register	/07601	—	—	—	—	—	—
54S195	4-Bit Parallel-Access Shift Register	/07602	—	—	—	—	—	—

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LOGIC—54S SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54S251	Data Selector/Mux with 3-State Outputs	/08905	—	—	—	—	—	—
54S253	Dual 4-Line to 1-Line Data Selector/Mux	—	—	—	—	—	F	W
54S257	Quad 2-Line to 1-Line Data Selector/Mux	/07906	—	—	—	—	—	—
54S258	Quad 2-Lint to 1-Line Data Selector/Mux	/07907	—	—	—	—	—	—
54S260	Dual 5-Input NOR Gate	—	—	—	—	—	F	W
54S280	9-Bit Odd/Even Parity Generator/Checker	/07703	—	—	—	—	—	—
54S350	4/6 Bit Shifter-Tri-State	—	—	—	—	—	F	—

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LOGIC—8200/9300/9600 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED*		JAN PROCESSED		MIL REL/883 MIL TEMP	
			Dip	Flat Pack	Dip	Flat Pack	Dip	Flat Pack
8200	Dual 5-Bit Buffer Register	—	—	—	—	—	I	Q
8201	Dual 5-Bit Buffer Register with D Inputs	—		—	—	—	I	Q
8202	10-Bit Buffer Register	—	—	—	—	—	I	Q
8203	10-Bit Buffer Register with D Inputs	—	—	—	—	—	I	Q
8230	8-Input Digital Multiplexer	/01402	*	*	F	W	F	W
8231	8-Input Digital Multiplexer	—	—	—	—	—	F	W
8232	8-Input Digital Multiplexer	—	—	—	—	—	F	W
8233	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8234	2-Input 4-Bit Digital Multiplexer		—	—	—	—	F	W
8235	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8241	Quad Exclusive-OR Gate	—	—	—	—	—	F	W
8242	Quad Exclusive-NOR Gate	—	—	—	—	—	F	W
8243	8-Bit Position Scaler	—	—	—	—	—	I	Q
8250	Binary-to-Octal Decoder	/15204	2	2	F	W	F	W
8251	BCD-to-Decimal Decoder	/15205	2	2	F	W	F	W
8252	BCD-to-Decimal Decoder	/15206	2	2	F	W	F	W
8260	Arithmetic Logic Unit	—	—	—	—	—	I	Q
8261	Fast Carry Extender	—	—	—	—	—	F	W
8262	9-Bit Parity Generator and Checker	—	—	—	—	—	F	W
8263	3-Input 4-Bit Digital Multiplexer	—	—	—	—	—	I	Q
8264	3-Input 4-Bit Digital Multiplexer		—	—	—	—	I	Q
8266	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8267	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8268	Gated Full Adder	—	—	—	—	—	F	Q
8269	4-Bit Comparator	—	—	—	—	—	F	W
8270	4-Bit Shift Register	—	—	—	—	—	F	W
8271	4-Bit Shift Register	—	—	—	—	—	F	W
8273	10-Bit Serial-In, Parallel-Out Shift Register	—	—	—	—	—	F	W
8274	10-Bit Parallel-In, Serial-Out Shift Register	—	—	—	—	—	F	W
8275	Quad Bistable Latch	—	—	—	—	—	F	W
8276	8-Bit Serial Shift Register	—	—	—	—	—	F	—
8277	Dual 8-Bit Shift Register	—	—	—	—	—	F	—
8280	Presettable Decade Counter	—	—	—	—	—	F	W
8281	Presettable Binary Counter	—	—	—	—	—	F	W
8284	Binary Up/Down Counter	—	—	—	—	—	F	W
8285	Decade Up/Down Counter	—	—	—	—	—	F	W
8288	Divide-by-Twelve Counter	—	—	—	—	—	F	W
8290	Presettable High Speed Decade Counter	—	—	—	—	—	F	W
8291	Presettable High Speed Binary Counter	—	—	—	—	—	F	W
8292	Presettable Low Power Decade Counter	—	—	—	—	—	F	W
8293	Presettable Low Power Binary Counter	—	—	—	—	—	F	W
9300	4-Bit Shift Register	/15901	*	*	F	W	F	W
9301	BCD to Decimal Decoder	/15206	2	2	F	W	F	W
9308	Dual 4-Bit Latch w/Clear	—	—	—	—	—	I	Q
9309	Dual 4-Input Multiplexer	/01404	I	I	F	W	F	W
9310	4-Bit Decade Counter	—	—	—	—	—	F	W
9312	8-Input Digital Multiplexer	/01402	*	*	F	W	F	W
9316	4-Bit Binary Counter	—	—	—	—	—	F	W
9322	Data Selector-Multiplexer	—	—	—	—	—	F	W
9324	5-Bit Comparator	/15002	*	*	F	WP	W	—
9334	8-Bit Addressable Latch	/16001	—	—	—	—	F	W
9602	Dual Monostable Multivibrator	—	*	*	F	W	F	W

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LOGIC—8T INTERFACE SERIES

DEVICE	DESCRIPTION	JAN M38510 SHEET	MIL REL/883 MIL TEMP	
			Dip	Flat Pack
8T04	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T05	7-Segment Decoder Display Driver (Active-Hi Outputs)	—	F	W
8T06	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T09	Quad Bus Driver with Tri-State Outputs	—	F	W
8T10	Quad D-Type Bus Latch (Tri-State)	—	F	W
8T13	Dual Line Driver	—	F	W
8T14	Triple Line Receiver/Schmitt Trigger	—	F	W
8T18	Dual 2-Input NAND (High Voltage to TTL Interface)	—	F	W
8T20	Bidirectional Monostable Multivibrator (Diff. Input)	—	*	*
8T22	Retriggerable Monostable Multivibrator (54122/9601)	—	F	W
8T26A	Quad Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T28	Quad Non-Inverting Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T31	8-Bit Bidirectional I/O Port	—	*	*
8T32	Programmable 8-Bit, I/O Port (3-State)	—	I	*
8T33	Programmable 8-Bit, I/O Port (Open Collector)	—	I	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	—	I	*
8T37	Hex Bus Receiver with Hysteresis—Schmitt Trigger (DM8837)		F	W
8T38	Quad Bus Transceiver (Open Collector) (DM8838)	—	F	W
8T80	Quad 2-Input NAND Gate (High Voltage)	—	F	W
8T90	Hex Inverter (High Voltage)	—	F	W
8T95	High Speed Hex Buffers/Inverters (74365/DM8095)	—	F	W
8T96	High Speed Hex Buffers/Inverters (74366/DM8096)	—	F	W
8T97	High Speed Hex Buffers/Inverters (74367/DM8097)		F	W
8T98	High Speed Hex Buffers/Inverters (74368/DM8098)		F	W

* = Qualification planned

LOGIC—5400 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL*		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
5400	Quad 2-Input NAND Gate	/00104	1	1	F	W	F	W
5401	Quad 2-Input NAND Gate with o/c	/00107	1	1	F	W	F	W
5402	Quad 2-Input NOR Gate	/00101	1	1	F	W	F	W
5403	Quad 2-Input NAND Gate with o/c	/00109	1	1	F	*	F	—
5404	Hex Inverter	/00105	1	1	F	W	F	W
5405	Hex Inverter with o/c	/00108	1	1	F	W	F	W
5406	Hex Inverter w/Buffer/Driver with o/c	/00801	—	—	F	W	F	W
5407	Hex Buffer/Driver with o/c	/00803	—	—	F	W	F	W
5408	Quad 2-Input AND Gate	/01601	1	1	F	W	F	W
5409	Quad 2-Input AND Gate with o/c	/01602	1	1	F	W	F	W
5410	Triple 3-Input NAND Gate	/00103	1	1	F	W	F	W
5411	Triple 3-Input NAND Gate	—	—	—	—	—	F	W
5412	Triple 3-Input NAND Gate wih o/c	/00106	—	—	—	—	F	W
5413	Dual NAND Schmitt Trigger	/15101	*	*	F	W	F	W
5414	Hex Schmitt Trigger	/15102	*	*	F	W	F	W
5416	Hex Inverter Buffer/Driver with o/c	/00802	—	—	F	W	F	W
5417	Hex Buffer/Driver with o/c	/00804	—	—	F	W	F	W
5420	Dual 4-Input NAND Gate	/00102	1	1	F	W	F	W
5421	Dual 4-Input AND Gate	—	—	—	—	—	F	W
5426	Quad 2-Input NAND Gate with o/c	/00805	1	—	F	—	F	—
5427	Triple 3-Input NOR Gate	/00404	*	*	F	W	F	W
5428	Quad 2-Input NOR Buffer	/16201	—	—	—	—	F	W
5430	8-Input NAND Gate	/00101	1	1	F	W	F	W
5432	Quad 2-Input OR Gate	/16101	*	*	—	—	F	W
5433	Quad 2-Input NOR Buffer with o/c	—	—	—	—	—	F	W
5437	Quad 2-Input NAND Buffer	/00302	1	1	F	W	F	W
5438	Quad 2-Input NAND Buffer with o/c	/00303	1	1	F	W	F	W
5439	Quad 2-Input NAND Buffer	—	—	—	—	—	F	W
5440	Dual 4-Input NAND Buffer	/00301	1	1	F	W	F	W
5442	BCD-to-Decimal Decoder	/01001	1	1	F	W	F	W
5443	Excess 3-to-Decimal Decoder	/01002	1	1	F	W	F	W
5444	Excess 3-Gray-to-Decimal Decoder	/01003	1	1	F	W	F	W
5445	BCD-to-Decimal Decoder/Driver with o/c	/01004	—	—	F	W	F	W
5446A	BCD-to-7 Segment Decoder/ Driver	/01006	—	—	F	W	F	W
5447A	BCD-to-7 Segment Decoder/ Driver	/01007	—	—	F	W	F	W
5448	BCD-to-7 Segment Decoder/ Driver	/01008	—	—	F	W	F	W
5450	Expandable Dual 2-Wide 2-Input A01	/00501	1	1	F	W	F	W
5451	Dual 2-Wide 2-Input A01 Gate	/00502	1	1	F	W	F	W
5453	4-Wide 2-Input A01 Gate (Expandable)	/00503	1	1	F	W	F	W
5454	4-Wide 2-Input A01 Gate	/00504	1	1	F	W	F	W
5455	2-Wide 4-Input A01 Gate	/04005	—	—	—	—	—	—

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LOGIC—5400 SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL*		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
5460	Dual 4-Input Expander	—	—	—	—	—	F	W
5470	J-K Flip-Flop	/00206	1	1	F	W	F	W
5472	J-K Master-Slave Flip-Flop	/00201	1	1	F	W	F	W
5473	Dual J-K Master-Slave Flip-Flop	/00202	1	1	F	W	F	W
5474	Dual D-Type Edge-Triggered Flip-Flop	/00205	1	1	F	W	F	W
5475	Quad Bistable Latch	/01501	1	1	F	W	F	W
5476	Dual J-K Master-Slave Flip-Flop	/00204	1	1	F	W	F	W
5477	Quad Bistable Latch	/01502	—	1	—	W	—	W
5480	Gated Full Adder	—	—	—	—	—	F	W
5483	4-Bit Binary Full Adder	/00602	1	1	F	W	F	W
5485	4-Bit Magnitude Comparator	/15001	1	1	F	W	F	W
5486	Quad 2-Input Exclusive-OR Gate	/00701	1	1	F	W	F	W
5490	Decade Counter	/01307	*	*	F	W	F	W
5491	8-Bit Shift Register	—	—	—	—	—	F	W
5492	Divide-by-Twelve Counter	/01301	1	1	F	W	F	W
5493	4-Bit Binary Counter	/01302	1	1	F	W	F	W
5494	4-Bit Shift Register (PISO)	—	—	—	—	—	F	W
5495	4-Bit Left-Right Shift Register	/00901	1	—	F	—	F	W
5496	5-Bit Shift Register	/00902	1	1	F	W	F	W
54100	4-Bit Bistable Latch (Dual)	—	—	—	—	—	F	W
54107	Dual J-K Master-Slave Flip-Flop	/00203	1	—	F	—	F	—
54109	Dual J-K Positive Edge-Triggered Flip-Flop	—	—	—	—	—	F	W
54116	Dual 4-Bit Latch with Clear	/01503	2	—	I	—	I	—
54121	Monostable Multivibrator	/01201	1	1	F	W	F	W
54122	Retriggerable Monostable Multivibrator	/01202	—	—	—	—	—	—
54123	Retriggerable Monostable Multivibrator	/01203	1	1	F	W	F	W
54125	Quad Bus Buffer Gate w/Tri-State Outputs	/15301	2	2	F	W	F	W
54126	Quad Bus Buffer Gate w/Tri-State Outputs	/15302	2	2	F	W	F	W
54128	Quad 2-Input NOR Buffer	—	—	—	—	—	F	W
54132	Quad Schmitt Trigger	/15103	*	*	F	W	F	W
54145	BCD-to-Decimal Decoder/Driver with o/c	/01005	—	—	F	W	F	W
54147	10-Line to 4-Line Priority Encoder	/15601	*	*	F	W	F	W
54148	8-Line to 3-Line Priority Encoder	/15602	*	*	F	W	F	W
54150	16-Line to 1-Line Mux	/01401	2	—	I	—	I	—
54151	8-Line to 1-Line Mux	/01406	2	2	F	W	F	W
54152	8-Line to 1-Line Mux	—	—	—	—	—	F	W
54153	Dual 4-Line to 1-Line Mux	/01403	2	2	F	W	F	W
54154	4-Line to 16-Line Decoder/Demux	/15201	*	—	I	—	I	Q
54155	Dual 2-Line to 4-Line Decoder/Demux	/15202	2	2	F	W	F	W
54156	Dual 2-Line to 4-Line Decoder/Demux	/15203	2	2	F	W	F	W
54157	Quad 2-Input Data Selector (non-inv.)	/01405	1	1	F	W	F	W
54158	Quad 2-Input Data Selector (inv.)	—	—	—	—	—	F	W
54160	Synchronous 4-Bit Decade Counter	/01303	1	1	F	W	F	W

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LOGIC—5400 SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54161	Synchronous 4-Bit Binary Counter	/01306	1	1	F	W	F	W
54162	Synchronous 4-Bit Decade Counter	/01305	1	1	F	W	F	W
54163	Synchronous 4-Bit Binary Counter	/01304	1	1	F	W	F	W
54164	8-Bit Parallel-Out Serial Shift Register	/00903	1	—	F	—	F	—
54165	Parallel-Load 8-Bit Shift Register	/00904	*	*	F	W	F	W
			—	—	—	—	F	W
54166	8-Bit Shift Register	—	—	—	—	—	F	—
54170	4X4 Register File	/01801						
54174	Hex D-Type Flip-Flop with Clear	/01701	1	1	F	W	F	W
54175	Quad D-Type Edge-Triggered Flip-Flop	/01702	1	1	F	W	F	W
54180	8-Bit Odd/Even Parity Checker	/01901	—	2	F	W	F	W
54181	4-Bit Arithmetic Logic Unit	/01101	1	—	I	—	I	—
54182	Look-Ahead Carry Generator	/01102	1	1	F	W	F	W
54190	Synchronous Up/Down Counter (BCD)	—	—	—	—	—	*	*
54191	Synchronous Up/Down Counter (Binary)	—	—	—	—	—	*	*
54192	Synchronous Decade Up/Down Counter	/01308	*	*	F	W	F	W
54193	Synchronous 4-Bit Binary Up/Down Counter	/01309	*	*	F	W	F	W
54194	4-Bit Bidirectional Universal Shift Register	/00905	*	*	F	W	F	W
54195	4-Bit Parallel-Access Shift Register	/00906	*	*	F	W	F	W
54198	8-Bit Shift Register	—	—	—	—	—	I	Q
54199	8-Bit Shift Register	—	—	—	—	—	—	—
54221	Dual Monostable Multivibrator	—	—	—	—	—	F	W
54279	Quad S-R Latch	—	—	—	—	—	F	W
54298	Quad 2-Input Mux with Storage	—	—	—	—	—	F	W
54365	Hex Buffer w/Common Enable (3-State)	/16301	*	*	*	*	*	*
54366	Hex Buffer w/Common Enable (3-State)	/16302	*	*	*	*	F	W
54367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16303	*	*	*	*	F	W
54368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16304	*	*	*	*	F	W

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LOGIC—54H SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54H00	Quad 2-Input NAND Gate	/02304	1	1	F	W	F	W
54H01	Quad 2-Input NAND Gate with o/c	/02306	1	1	F	W	F	W
54H04	Hex Inverter	/02305	1	1	F	W	F	W
54H05	Hex Inverter with o/c	—	—	—	—	—	F	W
54H08	Quad 2-Input AND Gate	/15501	2	—	F	—	F	W
54H10	Triple 3-Input NAND Gate	/02303	1	1	F	W	F	W
54H11	Triple 3-Input NAND Gate	/15502	2	—	F	—	F	W
54H20	Dual 4-Input NAND Gate	/02302	1	1	F	W	F	W
54H21	Dual 4-Input AND Gate	/15503	2	—	F	—	F	W
54H22	Dual 4-Input NAND Gate with o/c	/02307	1	—	F	W	F	W
54H30	8-Input NAND Gate	/02301	1	1	F	W	F	W
54H40	Dual 4-Input NAND Buffer	/02401	1	1	F	W	F	W
54H50	Expandable Dual 2-Wide 2-Input A01	/04001	1	1	F	W	F	W
54H51	Dual 2-Wide 2-Input A01 Gate	/04002	1	1	F	W	F	W
54H52	Expandable 4-Wide 2-2-2-3 Input AND-OR Gate	—	—	—	—	—	F	W
54H53	4-Wide 2-Input A01 Gate (Expandable)	/04003	1	1	F	W	F	W
54H54	4-Wide 2-Input A01 Gate	/04004	1	1	F	W	F	W
54H55	2-Wide 2-Input A01 Gate	/04005	1	1	F	W	F	W
54H60	Dual 4-Input Expander	—	—	—	—	—	F	W
54H61	Triple 3-Input Expander	—	—	—	—	—	F	W
54H62	3-2-2-3 Input AND-OR Expander	—	—	—	—	—	F	W
54H71	J-K Master-Slave Flip-Flop with AND-OR Inputs	—	—	—	—	—	F	W
54H72	J-K Master-Slave Flip-Flop	/02201	1	1	F	W	F	W
54H73	Dual J-K Master-Slave Flip-Flop	/02202	1	1	F	W	F	W
54H74	Dual D-Type Edge-Triggered Flip-Flop	/02203	1	1	F	W	F	W
54H76	Dual J-K Master-Slave Flip-Flop	/02204	1	1	F	W	F	W
54H101	J-K Negative Edge-Triggered Flip-Flop	/02205	1	1	F	W	F	W
54H102	J-K Negative Edge-Triggered Flip-Flop	—	—	—	—	—	F	W
54H103	Dual J-K Negative Edge-Triggered Flip-Flop	/02206	1	1	F	W	F	W
54H106	Dual J-K Negative Edge-Triggered Flip-Flop	—	—	—	—	—	F	W
54H108	Dual J-K Negative Edge-Triggered Flip-Flop	—	—	—	—	—	F	—

NOTE

Per QPL 38510-28 dated 1 April 1977.
1 = Level 1 Qualification
2 = Level 2 Qualification
* = In Process

BIPOLAR MEMORY

BIPOLAR MEMORY

DEVICE	ORGANIZATION	PACKAGE*		OUTPUT CIRCUIT	NUMBER OF PINS
PROMs					
82S23	32X8	F	R	OC	16
82S115	512X8	I	R	TS	24
82S123	32X8	F	R	TS	16
82S126	256X4	F	R	OC	16
82S129	256X4	F	R	TS	16
82S130	512X4	F	R	OC	16
82S131	512X4	F	R	TS	16
82S136	1024X4	F,I	R	OC	18
82S137	1024X4	F,I	R	TS	18
82S140	512X8	I	R	OC	24
82S141	512X8	I	R	TS	24
82S180	1024X8	I	R	OC	24
82S181	1024X8	I	R	TS	24
82S184	2048X4	I	R	OC	18
82S185	2048X4	I	R	TS	18
82S2708	1024X8	I	R	TS	24
FPLAs					
82S100	16X48X8	I	R	TS	28
82S101	16X48X8	I	R	OC	28
PLAs					
82S200	16X48X8	I	R	TS	28
82S201	16X48X8	I	R	OC	28
RAMs					
3101A	16X4	F	R	OC	16
54S89	16X4	F	R	OC	16
54S189	16X4	F	R	TS	16
54S200	256X1	F	R	TS	16
54S201	256X1	F	R	TS	16
54S301	256X1	F	R	OC	16
82S09	64X9	I	R	TS	28
82S10	1024X1	F,I	R	OC	16
82S11	1024X1	F,I	R	TS	16
82S16	256X1	F	R	TS	16
82S17	256X1	F	R	OC	16
82S25	16X4	F	R	OC	16
ROMs					
82S215	512X8	I	R	TS	24
82S223	32X8	F	R	OC	16
82S224	32X8	F	R	TS	16
82S226	256X4	F	R	OC	16
82S229	256X4	F	R	TS	16
82S230	512X4	F	R	OC	16
82S231	512X4	F	R	TS	16
82S280	1024X8	I	R	OC	24
82S281	1024X8	I	R	TS	24

*NOTE

R = BeO Flat Pack
F = Cerdip
I = Ceramic DIP

BIPOLAR MEMORY CROSS REFERENCE

AMD	SIGNETICS
2700/27LS00	82S16
2701/27LS01	82S17
27S08/27LS08	82S23
27S09/27LS09	82S123
27S10	82S126
27S11	82S129
3101	82S25
3101A/27S02	3101A
93415	82S10
93415A	82S10
93425	82S11
93425A	82S11

FAIRCHILD	SIGNETICS
93403	82S25
93406	82S226
93411	82S17
93415	82S10
93415A	82S10
93417	82S126
93419	82S09
93421	82S16
93425A	82S11
93427	82S129
93431	82S130
93436	82S130
93438	82S140
93441	82S131
93442	82S240
93446	82S131
93448	82S141
93452	82S136
93453	82S137
93454	82S280
93457	82S126
93464	82S281
93467	82S129

HARRIS	SIGNETICS
0064	82S25
HM7602-2	82S23
HM7603-2	82S123
HM7608-2	82S2708
HM7610-2	82S126
HM7611-2	82S129
HM7620-2	82S130
HM7621-2	82S131
HM7640-2	82S140
HM7641-2	82S141
HM7642-2	82S136
HM7643-2	82S137
HM7647-2	82S115
HM7680-2	82S180
HM7681-2	82S181
HM7684-2	82S184
HM7685-2	82S185

INTEL	SIGNETICS
2708	82S2708
2716	82S2716
3101	82S25
3101A	3101A
3106/A	82S16
3107/A	82S17
3301A	82S226
3302	82S230
3322	82S231
3601	82S126
3602	82S130
3604	82S140
3605	82S136
3608	82S180
3622	82S131
3624	82S141
3625	82S137
3628	82S181

INTERSIL	SIGNETICS
5501	82S25
5508	82S10
5508A	82S10
5518	82S11
5518A	82S11
5523	74S201
5523A	82S16
5533	74S301
5533A	82S17
5600	82S23
5603A	82S126
5604	82S130
5605	82S140
5610	82S123
5623A	82S129
5624	82S131
5625	82S141
56506	82S136
56526	82S137

MOTOROLA	SIGNETICS
4004A	82S226
4064	82S25
4256	82S16
5005	82S126

MMI	SIGNETICS
5200	82S226
5201	82S229
5205	82S230
5206	82S231
5300-1	82S126
5301-1	82S129
5305-1	82S130
5306-1	82S131
5330	82S23
5331	82S123

MMI	SIGNETICS
5340-1	82S140
5341	82S141
5348	82S146
5349	82S147
5352	82S136
5353	82S137
5380	82S180
5381	82S181
5385	82S2708
5530	82S17
5531	82S16
5560	82S25/3101A

NATIONAL	SIGNETICS
54187	82S226
54S188	82S23
54S287	82S129
54S288	82S123
54S387	82S126
54S570	82S130
54S571	82S131
54S572	82S136
54S573	82S137
8582	82S17
86L99	82S25
87S295	82S140
87S296	82S141

T.I.	SIGNETICS
54187	82S226
54S188	82S23
54S189	74S189
54S200	74S200
54S201	74S201
54S209	82S11
54S270	82S230
54S287	82S129
54S288	82S123
54S289	3101A
54S301	74S301
54S309	82S10
54S370	82S231
54S387	82S126
54S472	82S147
54S473	82S146
54S474	82S141
54S475	82S140
54S476	82S137
54S477	82S136

NOTE
Parts are pin for pin functional replacements except where noted.

BIPOLAR MICROPROCESSOR

BIPOLAR MICROPROCESSORS

PRODUCT	DESCRIPTION	AVAILABILITY	
		Dip	Flat Pack
3001	Microprogram Control Unit	I	R
3002	Central Processing Element (2-bit slice)	I	R
8X300	Interpreter/Microcontroller	I	*
2901-1	Central Processing Element (4-bit slice)	*	*

*Under development

MICROPROCESSOR SUPPORT CIRCUITS

PRODUCT	DESCRIPTION	AVAILABILITY	
		Dip	Flatpack
LOGIC			
54123	Retriggerable Monostable Multivibrator	F	W
54180	8-Bit Odd/Even Parity Checker	F	W
54298	Quad 2-Input Mux with Storage	F	W
54S182	Look-Ahead Carry Generator	*	*
54S194	4-Bit Bidirectional Shift Register	*	*
54S195	4-Bit Parallel Access Shift Register	*	*
54LS365	High Speed Hex Tri-State Buffer	F	*
54LS366	High Speed Hex Tri-State Buffer	F	*
54LS367	High Speed Hex Tri-State Buffer	F	*
54LS368	High Speed Hex Tri-State Buffer	F	*
8262	9-Bit Parity Generator Checker	F	W
8281	Presettable Binary Counter	F	W
8291	Presettable High Speed Binary Counter	F	W
9602	Dual Monostable Multivibrator	F	W
INTERFACE			
8T09	Quad Bus Driver with Tri-State Output	F	W
8T10	Quad D-Type Bus Latch (Tri-State Outputs)	F	W
8T13	Dual Line Driver	F	W
8T14	Triple Line Receiver/Schmitt Trigger	F	W
8T26A	Quad Bus Driver/Receiver (Tri-State)	F	W
8T28	Quad Bus Non-Inverting Driver/Receiver (Tri-State)	F	W
8T32	Programmable 8-Bit I/O Port (3-State)	I	*
8T33	Programmable 8-Bit I/O Port (Open Collector)	I	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	I	*
8T95	High Speed Hex Buffer (Tri-State)	F	*
8T96	High Speed Hex Inverter (Tri-State)	F	*
8T97	High Speed Hex Buffer (Tri-State)	F	*
8T98	High Speed Hex Inverter (Tri-State)	F	*

*Under development

ANALOG

LINEAR INDUSTRY CROSS REFERENCE

FAIRCHILD	SIGNETICS
μA111	LM111
μA139	LM139
μA710	μA710
μA711	μA711
μA733	μA733
μAF155/156	LF155/156
μA101	LM101
μA101A	LM101A
μA107	LM107
μA108	LM108
μA108A	LM108A
MC1556	MC1556
μA1558	MC1558
μA709	μA709
μA709A	μA709A
μA741	μA741
μA747	μA747
μA748	μA748
MC1555	SE555
μA556	SE556
μA109	LM109
μA79XX	79XX (7)
μA723	μA723

MOTOROLA	SIGNETICS
MLM111	LM111
MC1710	μA710
MC1711	μA711
MC1733	μA733
LF155/56	LF155/156
MLM101	LM101
MLM101A	LM101A
MLM107	LM107
MC1558	MC1558
MC1709	μA709
MC1709P2	μA709A
MC1741	μA741
MC1747	μA747
MC1748	μA748
MC3556	SE556
MLM109	LM109
MC78XX	78XX (7)
MC79XX	79XX (7)
MC1723	μA723
MC1508	MC1508-8

NATIONAL	SIGNETICS
LM161	SE527
LH2111	LH2111
LM111	LM111
LM119	LM119
LM139	LM139
LM193	LM193/193A
LM710	μA710
LM711	μA711
LM733	μA733
LF155/56	LM155/156
LH2101A	LH2101A
LH2108A	LH2108A
LM101A	LM101
LM101	LM101A
LM107	LM107
LM108	LM108
LM108A	LM108A
LM124	LM124
LM158	LM158
LM1558	MC1558
LM1581	SE532
LM709	μA709
LM741	μA741
LM747	μA747
LM748	μA748
LM567	SE567
DM7820	DM7820
DM7830	DM7830
LM555	SE555
LM109	LM109
LM723	μA723

PMI	SIGNETICS
SSS1508	MC1508-8
DAC-08	SE5008

RAYTHEON	SIGNETICS
LM111	LM111
LM139	LM139
RM710	μA710
RM711	μA711
RM733	μA733
LF155/56	LF155/156
LM101	LM101
LM101A	LM101A
LM107	LM107
LM108	LM108
LM108A	LM108A
LM124	LM124
RM1556	MC1556
RM1558	MC1558
RM709	μA709
RM741	μA741
RM747	μA747
RM555	SE555
LM109	LM109
RM723	μA723

T.I.	SIGNETICS
LM111	LM111
SN52710	μA710
SN52711	μA711
SN52733	μA733
LF155/56	LF155/156
SN52101A	LM101A
SN52107	LM107
SN52709	μA709
SN52741	μA741
SN52748	μA748
SN55182	DM7820
SN55183	DM7830
SN52555	SE55
SE556	SE556
LM109	LM109
μA79XX	μA79XX (7)
SN52723	μA723

LINEAR PRODUCTS

DEVICE	DESCRIPTION	PACKAGE*	
	COMPARATORS		
SE521	Dual Comparator	F	
SE526	Analog Voltage Comparator	F	K
SE527	Analog Voltage Comparator	F	K
SE529	Analog Voltage Comparator	F	K
LH2111	Dual Comparator	F	
LM111	Comparator	F	T
LM119	Dual Comparator	F	K
LM139	Quad Comparator	F	
LM193/193A	Dual Comparator		T
μA710	Differential Voltage Comparator	F	T
μA711	Comparator	F	K
	DIFFERENTIAL AMPLIFIERS		
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
SE515	Differential Amplifier	F	K
μA733	Video Amplifier	F	K
	OPERATIONAL AMPLIFIERS		
LF155/156	FET Op Amp	T	
LH2101A	Dual Op Amp	F	
LH2108A	Dual Op Amp	F	
LM101	High Perf. Op Amp	F	T
LM101A	High Perf. Op Amp	F	T
LM107	General Purpose Op Amp	F	F
LM108	Precision Op Amp	F	T
LM108A	Precision Op Amp	F	T
LM124	Quad Op Amp	F	
LM158	Dual Op Amp		T
MC1556	Op Amp	F	T
MC1558	Dual Op Amp	F	T
SE532	Dual Op Amp	—	T
SE535	Hi Slew Rate Op Amp	T	
SE538	Hi Slew Rate Op Amp	T	
μA709	Op Amp	F	T
μA709A	Op Amp	F	T
μA741	General Purpose Op Amp	F	T
μA747	Dual Op Amp	F	K
μA748	General Purpose Op Amp	F	T

*NOTE
F = Cerdip
K/T/L = Metal can
DA/DB = TO-3 can
Flat pack available—special request

DEVICE	DESCRIPTION	PACKAGE	
	PHASE LOCKED LOOPS		
SE567	Tone Decoder P11	F	T
	LINE RECEIVERS		
DM7820	Dual Differential Line Receiver	F	
DM7830	Dual Differential Line Receiver	F	
	TIMERS		
SE555	Timer	F	T
SE556	Dual Timer	F	
SE558/9	Quad Timer	F	
	VOLTAGE REGULATORS		
LM109	5 Volt Regulator	DA	
SE5554	Dual Track Reg	F	
78XX (7)	Positive Reg	DA	
79XX (7)	Negative Reg	DA	
79MXX (7)	Med Power Reg	DB	
μA723	Precision Voltage Regulator	F	L
	DRIVERS		
DS1611-1614	Peripheral Drivers		T
	D/A		
MC1508-8	8-Bit D/A	F	
SE5008	8-Bit D/A	F	
SE5009	8-Bit D/A	F	

CHIP PROGRAM

CHIP PROGRAM

Signetics recognizes the industry need for integrated circuit die requirements. All standard military and commercial products can be supplied in chip form.

The matrix below outlines process options available for all chip products. Refer to Signetics Die Program catalog for additional information regarding: testing, lot qualification, product pin-outs and ordering information.

FLOW DESIGNATOR	VIS LEVEL	GLASS	GOLD BACKING
CB	H	Yes	No
CD	X	Yes	No
CE	H	Yes	Yes
CF	X	Yes	Yes
CG	S	No	Yes
CH	X	No	Yes
CJ	H	No	Yes
CK	S	Yes	No
CN	S	Yes	Yes
CP	X (SEM)	Yes	No
CW	H	No	No
CX	S	No	No
CY	X	No	No

Table 6 PROCESS MATRIX

NOTES

1. Visual levels:
   X = Mil std 883 2010.2 cond. A
   H = Mil std 883 2010.2 cond. B
   S = Signetics standard criteria
2. Temperature options:
   0°C to +70°C
   -55°C to +125°C

PACKAGES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across VCC and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Alloy 42 or equivalent, solder dipped.
6. Body material: Plastic
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

9. Lead material
   a. Alloy 52—gold plated, or solder dipped.
   b. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
   c. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated.
   d. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
   e. ASTM alloy F-15 (KOVAR) or equivalent—tin plated.
10. Body Material
   a. 1010 Steel—nickel plated or tin plate over nickel.
   b. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated.
   c. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
   d. Ceramic with glass seal at leads.
   e. BeO ceramic with glass seal at leads.
   f. Ceramic with ASTM alloy F-15 or equivalent.
11. Lid Material
   a. 1010 steel, nickel plated, or tin-plate over nickel, weld seal.
   b. Nickel or tin plated nickel, weld seal.
   c. Ceramic, glass seal.
   d. ASTM alloy F-15 or equivalent, gold plated.
   e. BeO Ceramic with glass seal.
   f. Translucent $A1_2O_3$, glass seal.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc} (°C/W)	DESCRIPTION[1]	PAGE
Standard Dual-in-Line				
8	NE	162/65		3
14	NH	150/65	TO-116/MO-001	3
16	NJ	137/53	MO-001	3
18	NK	135/53		3
20	NL	135/53		3
22	NM	120/53		3
24	NN	116/53	MO-015	4
28	NQ	116/53	MO-015	4
40	NW[3]	110/50	MO-015	4
Power Dual-in-Line				
14	NHA[2]	95/33	Butterfly	3
16	NJA[2]	95/33	Butterfly	3
18	NKA[2,3]	90/26	Butterfly	3
20	NLA[2,3]	90/26	Butterfly	3
24	NNA[2]	60/23	Butterfly	4
28	NQA[2]	56/21	Butterfly	4
Power				
3	S	200/70	TO-92	5
3	U	75/3	TO-220	5
3 + GND	GB[3]	95/15	Single-in-Line (SIL)	5
4 + GND	GC[3]	95/15	Single-in-Line (SIL)	5
12 + GND	PH/PHA[3]	95/15	Batwing	5

12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb .010 inches.
15. Maximum glass climb or lid skew is .010 inches.
16. Typical four places.
17. Dimension also applies to seating plane.

HERMETIC PACKAGES

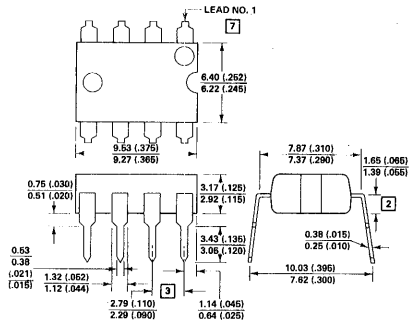
NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc} (°C/W)	DESCRIPTION[1]	PAGE
Metal Headers				
2	DA	TBD	TO-3 Solid Header	6
3	DB	TBD	TO-39 Solid Header, Short Can	6
4	DC	TBD	TO-72 Solid Header	6
4	DE	TBD	TO-72 Glass Filled Header	6
8	T	150/25	TO-99 Header (.200 Dia.)	7
10	K	150/25	TO-100 Header, Short Can	7
10	L	150/25	TO-100 Header, Tall Can	7
Flat Packs				
10	WF	240/50	Flat Ceramic	8
14	WH	205/50	Flat Ceramic	8
16	WJ	200/50	Flat Ceramic	8
24	WN	155/40	Flat Ceramic	8
16	RJ/RJA	133/30	Flat Ceramic, BeO	8
18	RKA[3]	TBD	Flat Ceramic, BeO	—
24	RNA	TBD	Flat Ceramic, BeO	8
28	RQA	TBD	Flat Ceramic, BeO	9
40	RWA	TBD	Flat Ceramic, BeO	9
10	QF	230/55	Flat Ceramic	9
14	QH	185/45	Flat Ceramic	9
16	QJ	170/45	Flat Ceramic	9
24	QN	155/44	Flat Ceramic	9
10	QFA	230/55	Flat Ceramic Laminate	10
14	QHA	185/45	Flat Ceramic Laminate	10
16	QJA	170/45	Flat Ceramic Laminate	10
24	QNA	155/44	Flat Ceramic Laminate	10
Cerdip Family				
14	FH	110/30	Dual in-Line Ceramic	11
16	FJ	100/30	Dual-in-Line Ceramic	11
18	FK	93/27	Dual-in-Line Ceramic	11
22	FM	75/27	Dual-in-Line Ceramic	11
24	FN	60/26	Dual-in-Line Ceramic	11
Laminated Ceramic, Side Brazed Lead				
8	IEA	100/30	Dip Laminate	12
14	IHA	95/25	Dip Laminate	12
16	IJA	90/25	Dip Laminate	12
18	IKA	88/25	Dip Laminate	12
22	IMA	80/25	Dip Laminate	12
24	INC/IND	65/25	Dip Laminate	12
28	IQA	60/25	Dip Laminate	13
40	IWA	55/25	Dip Laminate	13
50	IZA	TBD	Dip Laminate	13

NOTES

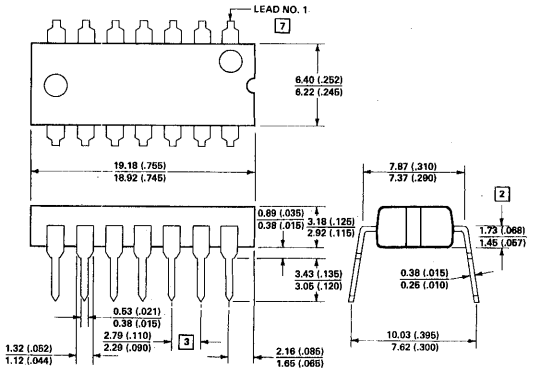
1. Dual-in-Line packages unless otherwise described
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads
3. Package not yet available, scheduled for 1977 release

PLASTIC: Standard and Power Dual-In-Line

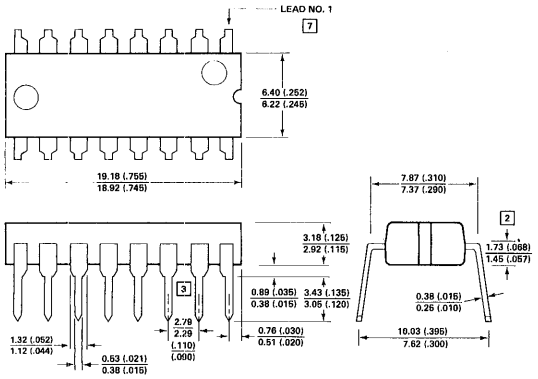
NE Package



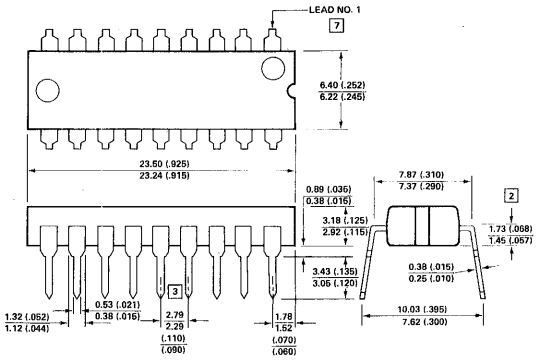
NH Package and NHA Package



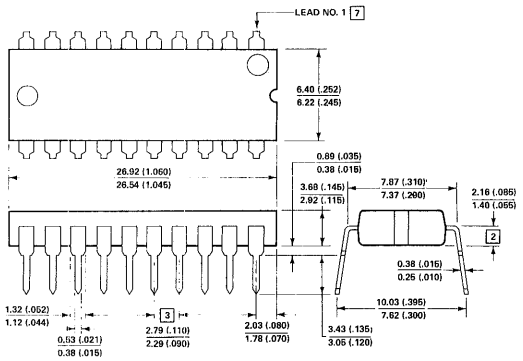
NJ Package and NJA Package



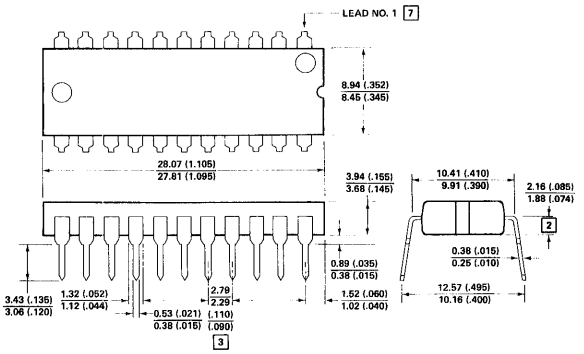
NK Package and NKA Package



NL Package and NLA Package

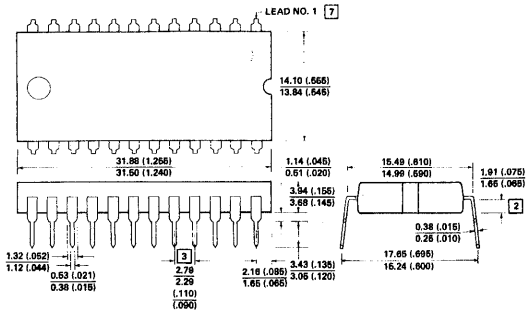


NM Package

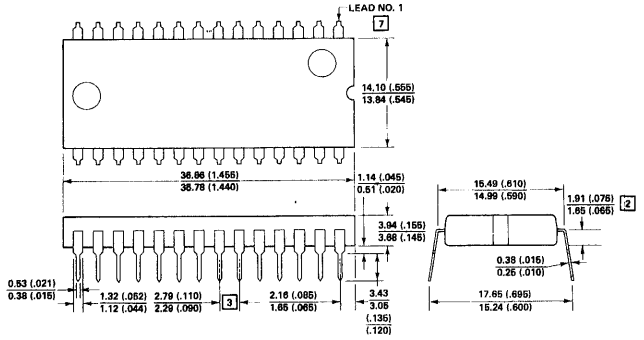


PLASTIC: Standard and Power Dual-In-Line (cont'd.)

NN Package and NNA Package



NQ Package and NQA Package

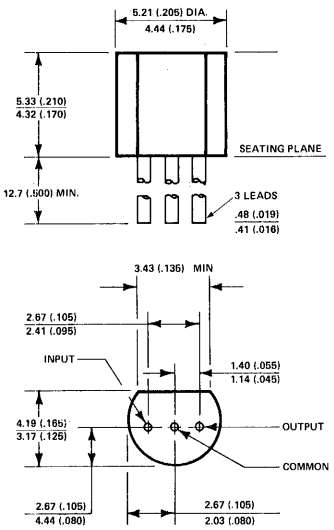


NW Package

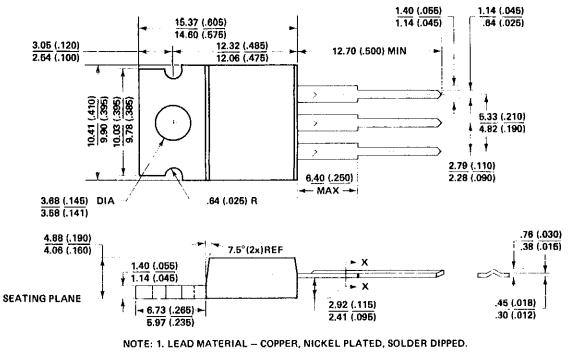
Package not yet available
Scheduled for 1977 release

PLASTIC: Power (Not Dual-In-Line)

S Package



U Package



NOTE: 1. LEAD MATERIAL – COPPER, NICKEL PLATED, SOLDER DIPPED.

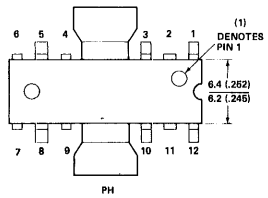
GB Package

Package not yet available
Scheduled for 1977 release

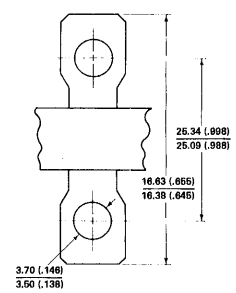
GC Package

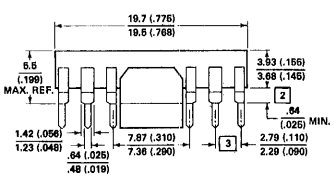
Package not yet available
Scheduled for 1977 release

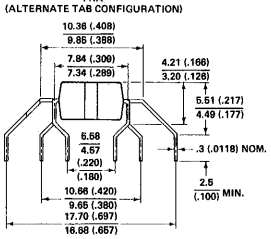
PH/PHA Package



NOTE: 1. FRAME MATERIAL – COPPER, SILVER PLATED.

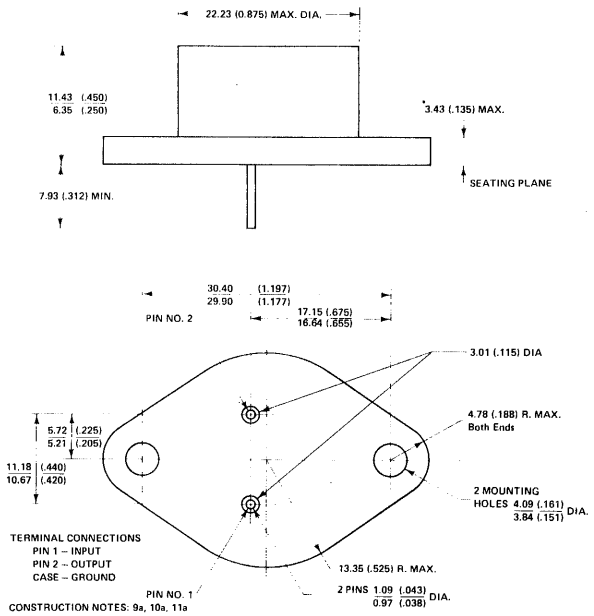






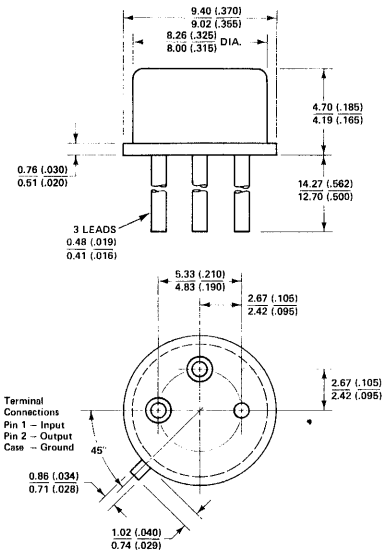
HERMETIC: Metal Headers

DA Package



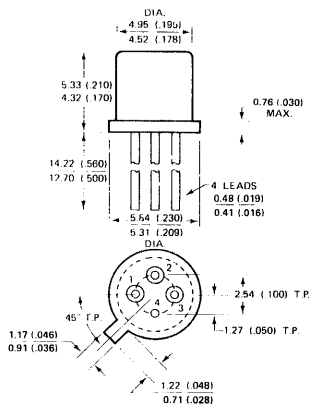
CONSTRUCTION NOTES: 9a, 10a, 11a

DB Package



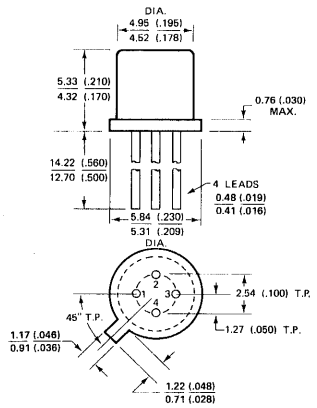
CONSTRUCTION NOTES: 9b, 10b, 11b

DC Package



CONSTRUCTION NOTES: 9b, 10b, 11b

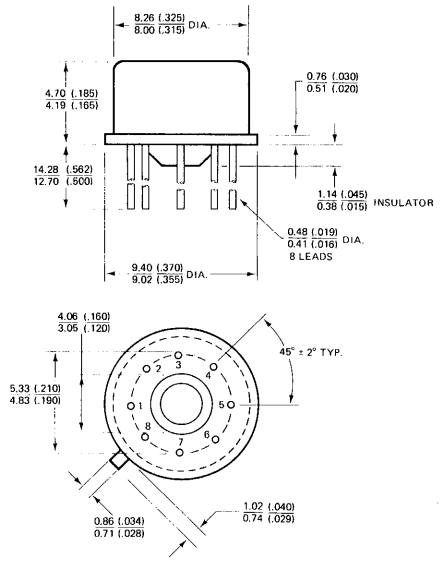
DE Package



CONSTRUCTION NOTES: 9b, 10c, 11b

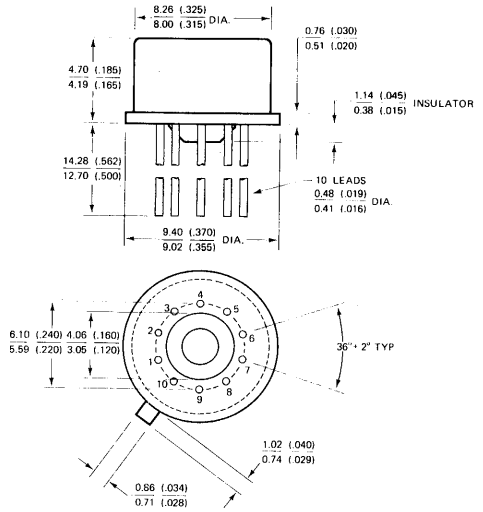
HERMETIC: Metal Headers (cont'd.)

T Package



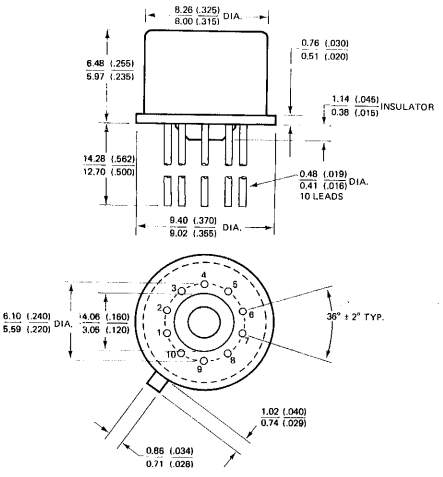
CONSTRUCTION NOTES: 9b, 10c, 11b

K Package



CONSTRUCTION NOTES: 9b, 10c, 11b

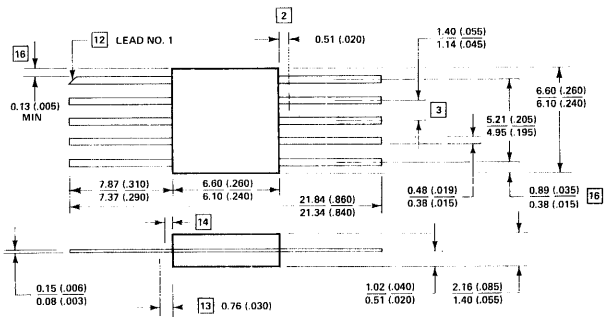
L Package



CONSTRUCTION NOTES: 9b, 10c, 11b

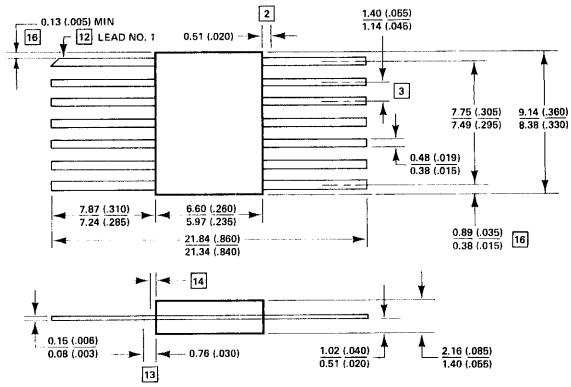
HERMETIC: Flat Packs

WF Package



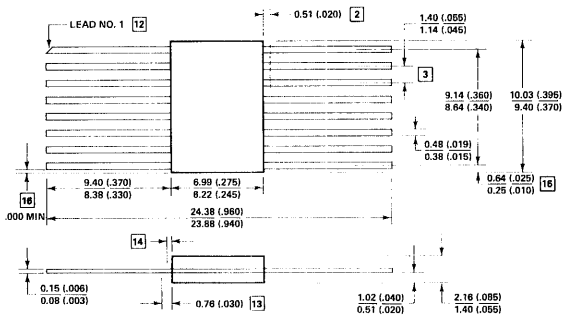
CONSTRUCTION NOTES: 9c, 10d, 11c

WH Package



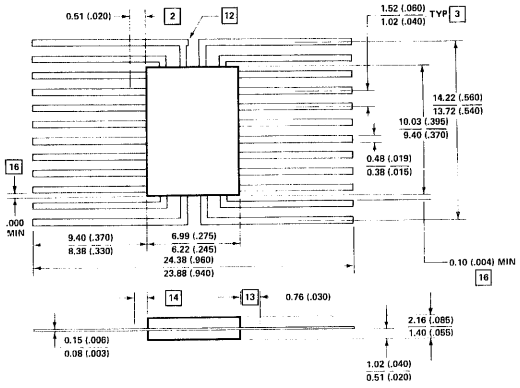
CONSTRUCTION NOTES: 9c, 10d, 11c

WJ Package



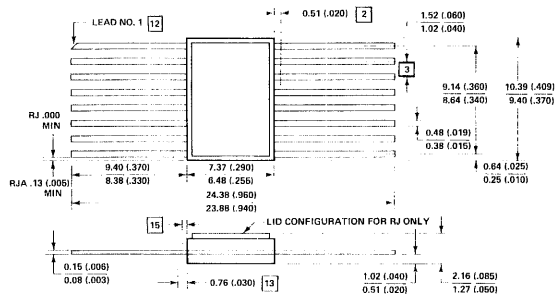
CONSTRUCTION NOTES: 9c, 10d, 11c

WN Package



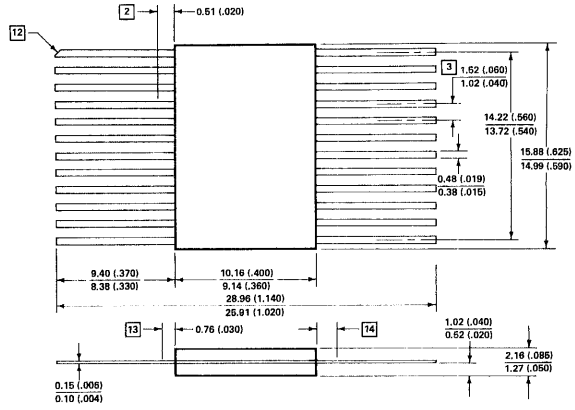
CONSTRUCTION NOTES: 9c, 10d, 11c

RJ and RJA Package



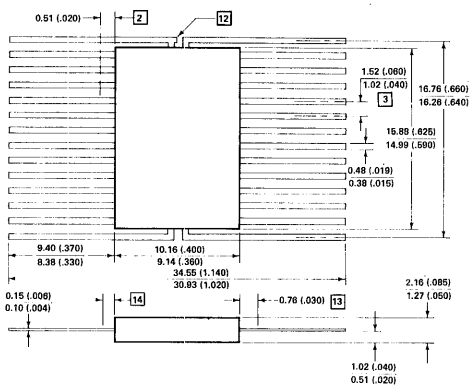
RJA CONSTRUCTION NOTES: 9c, 10e, 11e
RJ CONSTRUCTION NOTES: 9d, 10e, 11d

RNA Package



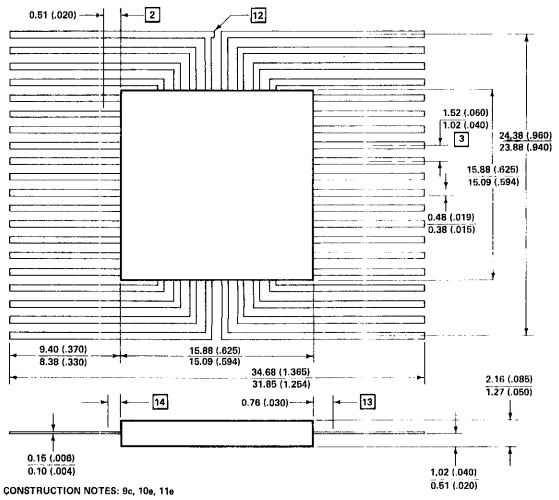
HERMETIC: Flat Packs (cont'd.)

RQA Package



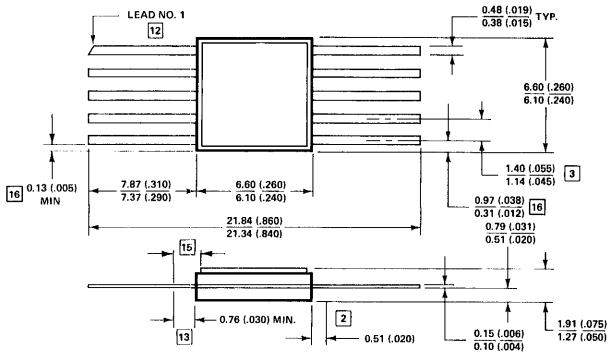
CONSTRUCTION NOTES: 9c, 10e, 11e

RWA Package



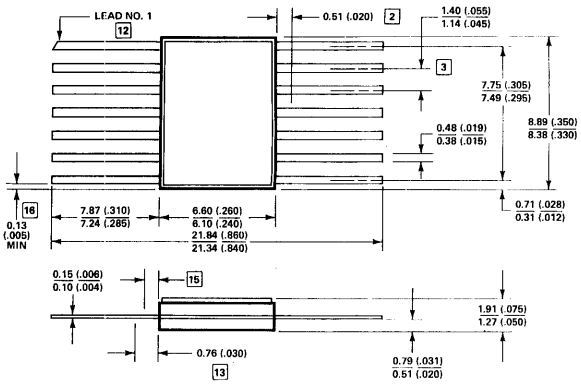
CONSTRUCTION NOTES: 9c, 10e, 11e

QF Package



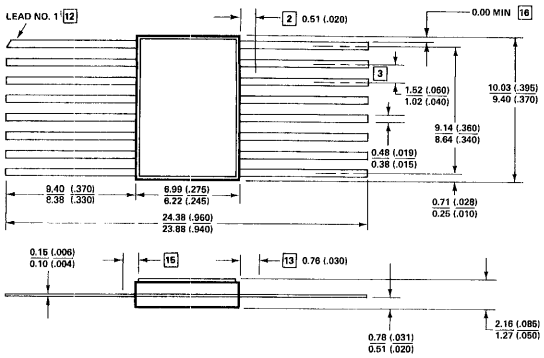
CONSTRUCTION NOTES: 9d, 10d, 11c

QH Package



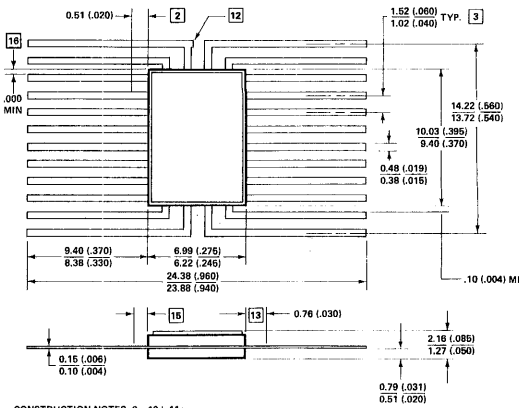
CONSTRUCTION NOTES: 9d, 10d, 11c

QJ Package



CONSTRUCTION NOTES: 9d, 10d, 11c

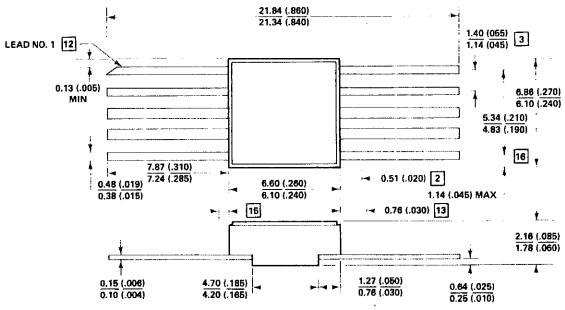
QN Package



CONSTRUCTION NOTES: 9c, 10d, 11c

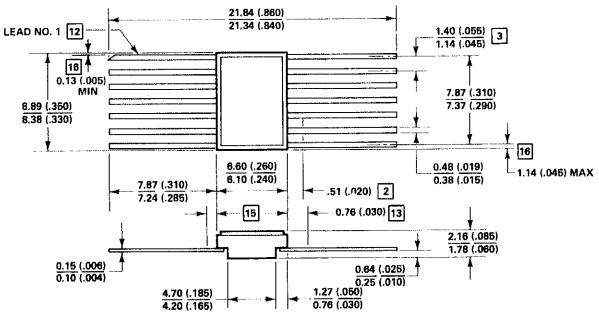
HERMETIC: Flat Packs (cont'd.)

QFA Package



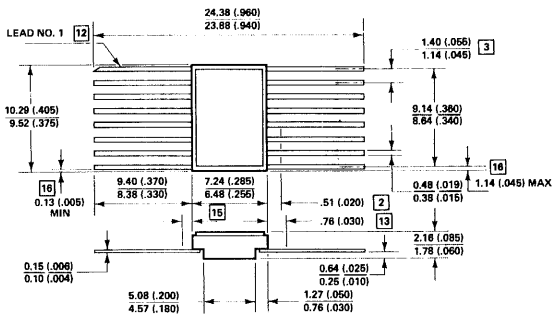
CONSTRUCTION NOTES: 9d, 10f, 11c

QHA Package



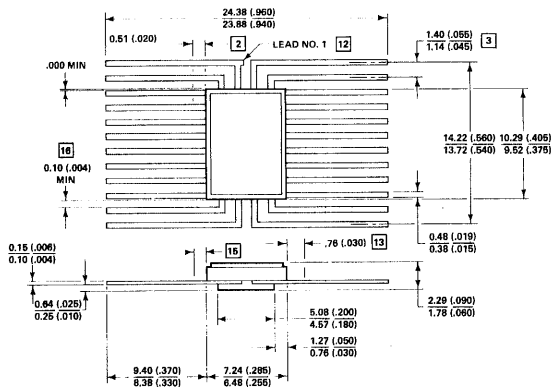
CONSTRUCTION NOTES: 9d, 10f, 11c

QJA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

QNA Package



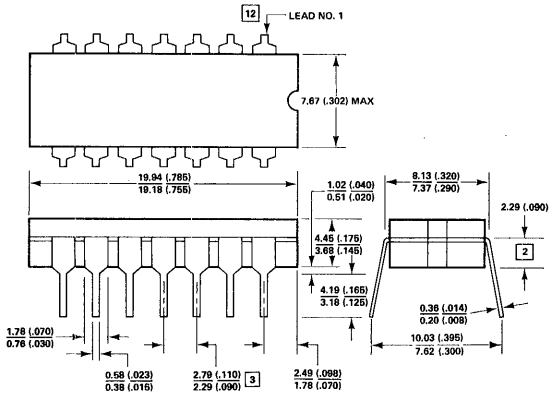
CONSTRUCTION NOTES: 9d, 10f, 11c

RKA Package

Package not yet available
Scheduled for 1977 release

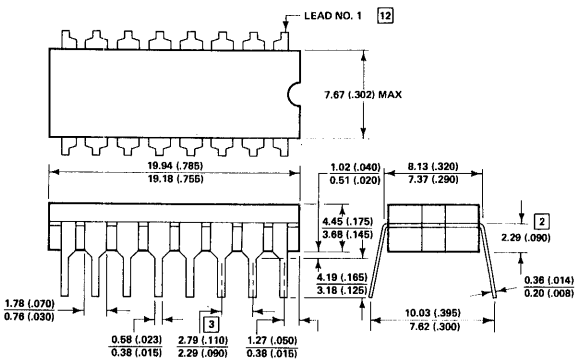
HERMETIC: Cerdip

FH Package



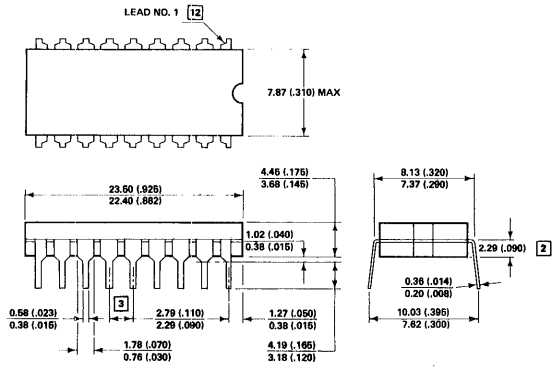
CONSTRUCTION NOTES: 9c, 10d, 11c

FJ Package



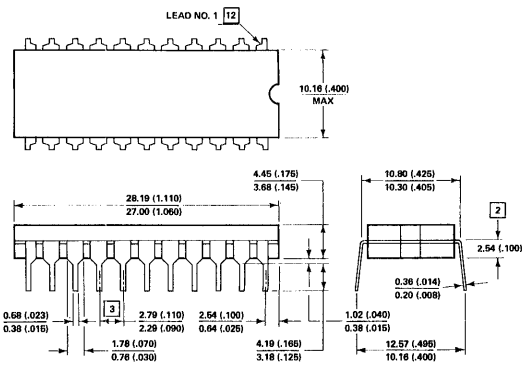
CONSTRUCTION NOTES: 9c, 10d, 11c

FK Package



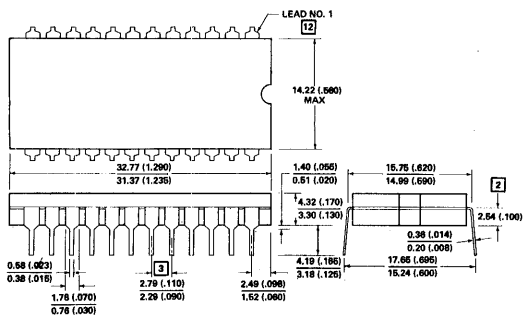
CONSTRUCTION NOTES: 9c, 10d, 11c

FM Package



CONSTRUCTION NOTES: 9c, 10d, 11c

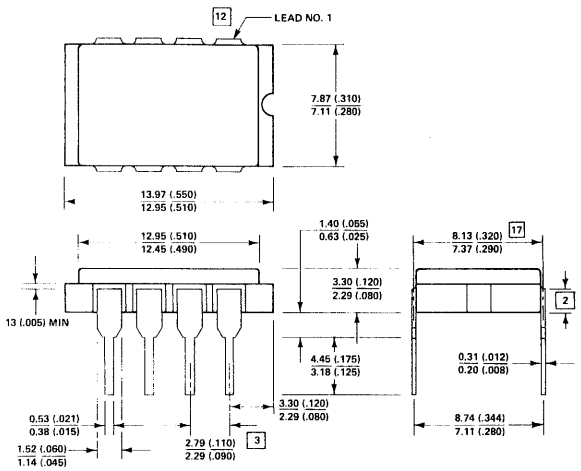
FN Package



CONSTRUCTION NOTES: 9c, 10d, 11c

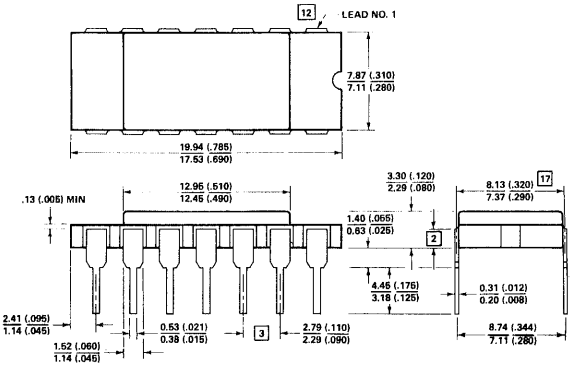
HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA Package



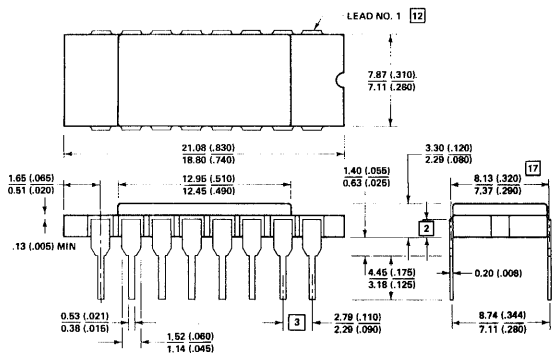
CONSTRUCTION NOTES: 9e, 10f, 11c

IHA Package



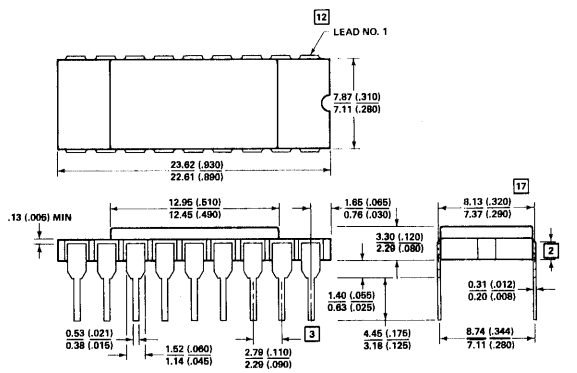
CONSTRUCTION NOTES: 9e, 10f, 11c

IJA Package



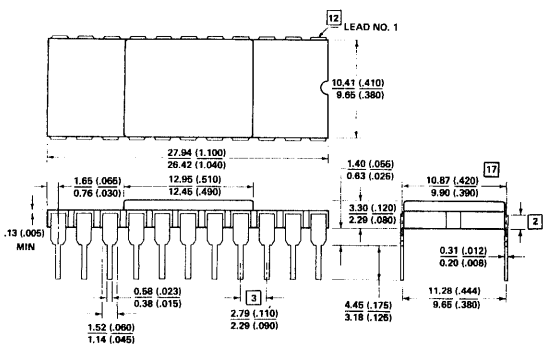
CONSTRUCTION NOTES: 9e, 10f, 11c

IKA Package



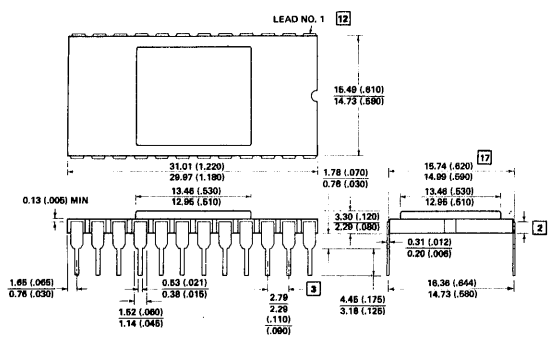
CONSTRUCTION NOTES: 9e, 10f, 11c

IMA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

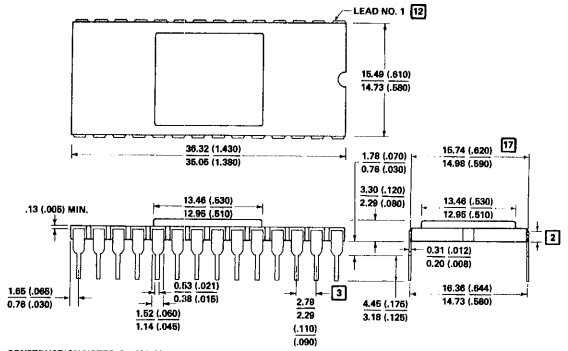
INC Package and IND Package



CONSTRUCTION NOTES: 9e, 10f, 11c, 11f (IND)

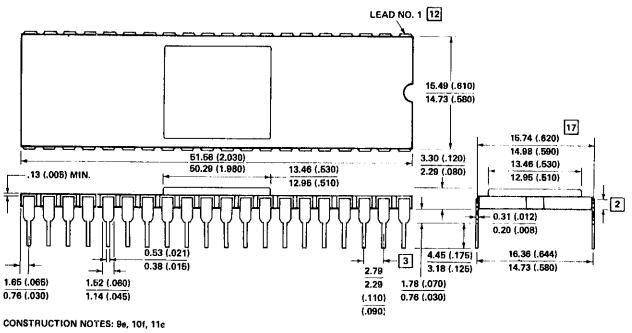
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IQA Package



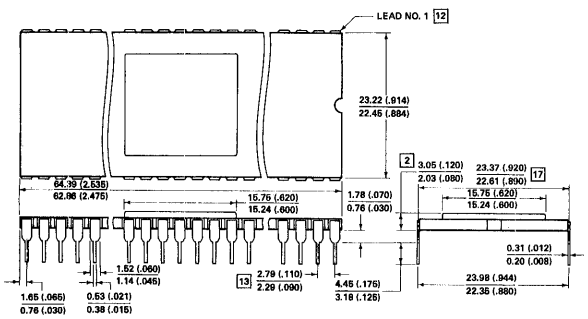
CONSTRUCTION NOTES: 9e, 10f, 11c

IWA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

IZA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

SALES OFFICES

SIGNETICS

HEADQUARTERS

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Sunnyvale, California 94086
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Irvine
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(213) 924-1668
San Diego
Phone: (714) 560-0242
Sunnyvale
Phone: (408) 736-7565

COLORADO
Parker
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FLORIDA
Pompano Beach
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ILLINOIS
Rolling Meadows
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KANSAS
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MARYLAND
Columbia
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